DEVELOPMENT AND EVALUATION OF LASER PROCESSED LIGHT MANAGEMENT INTERFACES FOR GRAPHENE/SILICON SCHOTTKY SOLAR CELLS

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ABSTRACT

DEVELOPMENT AND EVALUATION OF LASER PROCESSED LIGHT MANAGEMENT INTERFACES FOR GRAPHENE/SILICON SCHOTTKY SOLAR CELLS

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Graphene/silicon Schottky solar cells are one of the extensively studied topics during the last decade due to the high conductivity, high transparency, and mechanical flexibility properties of graphene. One of the most efficient and long-lasting methods used for performance enhancement for graphene/silicon Schottky solar cells is silicon surface texturing. It significantly increases the light absorption of silicon by controlling the incoming light through multiple interactions which is called light trapping. Rather than the well-established random pyramids, nanostructures such as freestanding nanoholes and nanowires which are applicable for thin films, are promising effective light trapping. In this thesis, three different surface texturing methods of metal-assisted chemical etching, femtosecond laser-induced periodic surface structuring, and photochemical etching are used to texture the silicon surface for graphene/silicon Schottky solar cell application. The attempt is targeting the development of laser-assisted fabrication of light management interfaces using laser-induced periodic surface structuring and photochemical etching methods. Diode-pumped solid-state high-power 532 nm CW laser and a femtosecond 1030 nm

wavelength laser are used as a source for photochemical etching and laser-induced periodic surface structuring methods, respectively. In addition, the well-established metal-assisted chemical etching method is used to compare the results related to the other two methods. Partially etched and fully etched surfaces are fabricated to study the relation between the enhanced light trapping and the recombination rate of the majority carrier in presence of defects. The main finding and results show that the surfaces textured by the photochemical etching method outperform the surfaces textured by metal-assisted chemical etching and laser-induced periodic surface structuring methods.

Keywords: photon management, solar cell, photochemical etching, metal-assisted chemical etching, laser texturing, graphene

ÖZ

GRAFEN/SİLİSYUM SCHOTTKY GÜNEŞ HÜCRELERI İÇİN LAZERLE İŞLENMİŞ IŞIK YÖNETİM ARAYÜZLERİNİN GELİŞTİRİLMESİ VE DEĞERLENDİRİLMESİ

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Grafen/silisyum Schottky güneş hücreleri, grafenin yüksek iletkenliği, yüksek şeffaflığı ve mekanik esneklik özellikleri nedeniyle son on yılda yoğun olarak çalışılan konulardan biridir. Grafen/silisyum Schottky güneş hücrelerinin performansını artırmak için kullanılan en verimli ve uzun ömürlü yöntemlerden biri silisyum yüzey yapılandırmasıdır. Işık tuzaklama adı verilen yöntem, çoklu etkileşimler yoluyla gelen ışığı kontrol ederek silisyumun ışık soğurumunu önemli ölçüde artırır. İyi bilinen rastgele piramitler yerine, ince filmlerde de uygulanabilir olan bağımsız nano delikler ve nano teller gibi nanoyapılar, etkili bir ışık tuzaklama vaat etmetkedir. Bu tezde, grafen/silisyum Schottky güneş hücreleri uygulaması için silisyum yüzeyin dokulandırılması için metal destekli aşındırma, lazerle periyodik yüzey yapılandırma ve fotokimyasal aşındırma olmak üzere üç farklı yüzey yapılandırma yöntemi kullanılmıştır. Bu çalışma, lazer destekli fotokimyasal aşındırma ve lazerle periyodik yüzey yapılandırma yöntemini kullanarak ışık yönetimi arayüzlerinin fabrikasyonunun geliştirilmesini hedeflemektedir. Diyot pompalı katı hal yüksek güçlü 532 nm CW lazer ve femtosaniye 1030 nm dalga

boyunda lazer, sırasıyla fotokimyasal aşındırma ve lazerle periyodik yüzey yapılandırma yöntemleri için kaynak olarak kullanılmıştır. Ayrıca, diğer iki yöntemle ilgili sonuçları karşılaştırmak için iyi bilinen metal destekli aşındırma yöntemi kullanılmıştır. Kısmen yapılandırılmış ve tamamen yapılandırılmış yüzeyler, kusurların mevcudiyetinde çoğunluk taşıyıcının rekombinasyon oranı ve ışık soğurumu arasındaki ilişkiyi incelemek için üretilmiştir. Ana bulgu ve sonuçlar fotokimyasal aşındırma yöntemiyle dokulandırılan yüzeylerin, metal destekli aşındırma ve femtosaniye lazer aşındırma yöntemleriyle dokulandırılan yüzeylerden daha iyi performansa sahip olduğunu göstermektedir.

Anahtar Kelimeler: foton yönetimi, güneş hücresi, fotokimyasal aşındırma, metal destekli aşındırma, lazer dokulandırma, grafen

To my family.

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TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

LIST OF ABBREVIATIONS

ABBREVIATIONS

3D	Three Dimensions
2D	Two Dimensions
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
b-Si	Black Silicon
CVD	Chemical Vapor Deposition
DMD	Digital Micromirror Device
LIPSS	Laser-Induced Periodic Surface Structuring
MACE	Metal-Assisted Chemical Etching
MLG	Multilayer Graphene
NPs	Nanoparticles
PCE	Photochemical Etching
PR	Photoresist
PV	Photovoltaic
SERS	Surface Enhanced Raman Spectroscopy
SEM	Scanning Electron Microscope
SLG	Single-Layer Graphene

CHAPTER 1

INTRODUCTION

In this thesis work, laser-based surface texturing methods of photochemical etching (PCE) and laser-induced periodic surface structuring (LIPSS) are used to texture the silicon surface for light-trapping purposes. The metal-assisted chemical etching (MACE) method which is widely studied in literature is also used to fabricate black silicon (b-Si) with a reflectance of less than 5% to compare the results. Current work on silicon surface texturing by nanostructures utilizing laser-based methods has indicated that the reflectance decreases significantly however it is still higher than the reflectance of the b-Si. Both LIPSS and PCE methods were studied in the literature however, the selective and partial etching in form of specific patterns aspect has not been studied so far. This thesis hypothesizes that when the silicon surface is partially etched in specific patterns, it would benefit the lower majority carrier recombination rate which results in a higher lifetime and improved electrical properties however, it degrades the light-trapping. The research strategy was to approach the problem with three different alternative structuring techniques. Our findings show that on the one hand, the MACE technique optimizes photon management and the LIPSS technique allows the selective surface texturing directly where it gives rise to elevated structural damage that costs valuable photocurrent extraction. On the other hand, the PCE technique gives minimal damage to the materials however at a cost of a lower level of photon management compared to MACE. From the comparison of the three texturing techniques, we find that the PCE technique combines the benefits of photon management and photocurrent extraction thus it can be used for optimal photon and electronically managed photoactive device fabrication such as in IR photodetector and photovoltaic cells. It is suggested that in case the partial surface structuring approach is taken to exploit the optimized photon and current management in optoelectronic devices, then special care has to be given

to maintain low structural damage, planarity of contacts, and inverted photon trap geometries such as hole arrays, inverted pyramids, etc.

Graphene/Silicon Schottky solar cells and photodetectors are one of the tens of Schottky diode types that is a research topic for researchers during the last decade due to the extraordinary properties of graphene such as high conductivity, high transparency, and mechanical flexibility [1]. In this thesis, three different surface structuring methods of MACE, LIPSS, and PCE are utilized for surface texturing of graphene/silicon Schottky solar cells to enhance light-trapping.

1.1 Background and Research Motivation

Graphene/silicon Schottky solar cells become into interest since one of the most important parameters for solar cells is being cost-effective. In the case of the Schottky junction, there will be no need for silicon doping which is a high-temperature and high-cost process. Although graphene is highly transparent and conductive which makes it a potential material to be used as transparent conductive oxide (TCO) [2]. Graphene is introduced as an alternative to Indium Tin Oxide (ITO) which is typically used as TCO and contains expensive and limited indium material [3]. Over years different strategies were used to increase the performance of the graphene/silicon Schottky solar cells. Some of the well-known strategies are molecular doping of graphene [4], degrading the silicon reflectivity by introducing micro- or nanostructures utilizing surface texturing methods [5], enhancing layer number of graphene [6], using an antireflection coating [7], and interface engineering by adding an interfacial barrier [8]. Among the methods used for performance enhancement of graphene/silicon solar cells, silicon surface texturing is one of the easiest and long-lasting methods. It is possible to control the incoming light and increase the traveling path of the light inside the silicon by multiple interactions which is called light tapping.

This thesis focuses on the silicon surface texturing strategy which results in a reduction of silicon reflectivity by light trapping. The Gr/Si Schottky solar cell was

first reported in 2010 by Li et al. [9] with an efficiency of 1.65 %, J_{sc} of 6.5 mA.cm^{-2}, and V_{oc} of 0.42 V . Later in 2011, Fan et al. [10] introduced Gr/Si nanowire Schottky junction for enhanced light harvesting. They reported energy conversion efficiency of up to 2.6%. the V_{oc} was enhanced to 0.46 V and J_{sc} to 9.2 mA.cm^{-2}. Feng et al [11], reported Schottky solar cells with arrays of silicon pillars on the substrate. The cell performance was improved to 3.55 % after p-type chemical doping of graphene by HNO_3. Xie et al. [12], reported cells with silicon surfaces etched in form of micro-hole arrays with 12 um depth by RIE. 4 layer of graphene doped by $AuCl_3$ was used to form the Schottky junction solar cell which resulted in a high efficiency of 10.40 %. The V_{oc} value was reported as 0.52 V and J_{sc} as 31.56 mA.cm^{-2}.

Light trapping to enhance the device performance by increasing the incident light absorption is the motivation of this study to texture the silicon surface with three different methods of MACE, LIPSS, and PCE. The problems associated with the MACE method which is one of the well-known methods to produce black silicon [13] are the high recombination rate due to the high aspect ratio of the structures and the metallic contamination that can be remained after the process. Therefore, laser-based etching methods of LIPSS and PEC are suggested to be used for the surface texturing purpose in this thesis. The metallic contamination is eliminated in the case of laser-based methods, however, the reflectance of the structures produced by laser-based etching methods is higher than the MACE structures. Where both LIPSS and PCE are non-contact laser-based texturing methods, the PCE is a solution-based wet texturing process and LIPSS is a dry process.

The idea of partial etching rises from the fact that the majority carrier recombination rate is high for nanostructures with a high aspect ratio. From the selective etching point of view, the LIPSS method which is a direct laser texturing method has the advantage of periodic patterning directly utilizing a femtosecond laser. This method is easy, fast, and controllable however, it has the disadvantage of causing significant damage to the silicon surface [14]. The PCE method which uses a visible range CW-

laser causes less damage which results in a better material quality of the textured silicon [15]. For partial texturing by the PCE method, the laser beam was patterned using a digital micromirror device (DMD).

Although each method results in the formation of different nanostructures. The MACE method results in the formation of Si nanowires, the LIPSS method forms arrays of nanoripples, and the nanoholes like inverted pyramids can be fabricated by the PCE method. From the graphene/silicon junction point of view, suspended graphene that covers the cavities shows significantly different physical properties than the graphene bonded to the substrate. On one hand, the suspended graphene has mobility more than ten times higher than the mobility of the graphene bonded to silicon [16]. On the other hand, in the case of the graphene/silicon Schottky junction the graphene on the silicon substrate is the one that forms the Schottky junction. It means that partial surface texturing can also provide the opportunity to catch a trade-off between the better electrical behavior of the suspended graphene and the graphene bonded to silicon. To provide a comprehensive study of the graphene/silicon Schottky solar cell performances, we have employed the abovementioned three different surface texturing techniques yielding different device specifications.

1.2 Outline of Thesis

The purpose of this thesis is to evaluate the applicability of the laser-based etching methods of PCE and LIPSS for full and partial surface texturing for Gr/Si Schottky solar cell applications. The properties of the fabricated nanostructures are compared to widely studied silicon nanowires fabricated by MACE. The advantages, disadvantages, and performance of each method are studied and evaluated. The obtained nanostructures are used to fabricate cost-effective, stable, and high-performance Gr/Si Schottky junction solar cells. For this purpose, the state-of-the-art of Gr/Si Schottky junction solar cells has been studied. This lends credence to the idea that a unique structure of the Gr/Si Schottky junction solar cell can be developed

to address the problems currently encountered with the architectures that have been reported.

The outline of this thesis is presented as follows:

In chapter 2 the silicon solar cells and their working principles are reviewed. The photovoltaic effect, possible loss mechanisms of photovoltaics, and the strategies to overcome the loss mechanisms are discussed. It also delves into the current developments in silicon solar cell technology and the obstacles standing in the way of silicon-based solar cells with high efficiencies.

In chapter 3, graphene, its characteristics, and its employment in Schottky solar cells are reviewed. It also describes the different fabrication methods of graphene and explains graphene growth by chemical vapor deposition (CVD). The characterization methods used for graphene characterization are reviewed. Finally, the difficulties encountered during the wet transfer procedure of the CVD-grown graphene are discussed. In addition, it shows the state of the art for solar cells that use graphene/Si Schottky junctions.

Chapter 4 presents the laser-based photochemical etching and laser-induced periodic surface structuring methods used for surface texturing. The well-known metal-assisted chemical etching method is applied to provide black silicon by texturing the silicon surface to compare the results. The important parameters for the etching methods are optimized, analyzed, and discussed in detail. This chapter highlights the advantages, disadvantages, and difficulties of each method

Chapter 5 provides the Gr/Si Schottky solar cell fabrication steps in detail. It includes surface texturing, photolithography steps, metal deposition steps, and graphene wet transferring processes. The fabrication steps, parameters, and utilized devices are presented in this chapter.

Chapter 6 presents the I-V measurements and the device performances of the fabricated Gr/Si Schottky solar cells with silicon surfaces fully and partially etched

by laser-induced periodic surface structuring, photochemical etching, and metal-assisted chemical etching methods. The results are discussed and compared in detail. The conclusion of this study and possible future works are presented in this chapter.

CHAPTER 2

SILICON SOLAR CELL TECHNOLOGY

Solar cells are more appealing to the world's future energy needs because they directly convert sunlight to electricity without harming the environment or producing any harmful byproducts. Also, what makes photovoltaics interesting is the fact that they can be readily integrated into a power plant or a single residence. It's also possible to use solar cells anywhere that sunlight can reach, from the remotest rural regions to outer space. As a result, solar cells hold even more promise because they circumvent many of the complexities associated with transporting electricity from a power plant to a residence. Although solar panels have become substantially more affordable due to advancements in photovoltaic technology and the effect of scientific research that have resulted in improved solar cell efficiency, they are still performing below their potential. To make solar cells more affordable, it is necessary to increase the efficiency of solar cells while reducing manufacturing costs.

2.1 Why Silicon?

The most common semiconductor in photovoltaic manufacturing is silicon, which is the second most abundant element on the planet. As a result, crystalline silicon solar cells account for 85 percent of the market share [17]. One of the well-known advantages of silicon is the fact that it can be easily cleansed since most of the renowned efficiency-reducing contaminants have low solid solubility in crystalline silicon [18]. Furthermore, p-n junctions can be formed by doping silicon with n- and p-type dopants. Although, A protective passivation layer forms when silicon oxidizes naturally, keeping the device from deteriorating. A warranty on device performance of 80% is possible even 25 years after installation due to the material's inherent stability [17].

In recent years, new renewable energy candidates like as thin film photovoltaics, organic photovoltaics, and photovoltaics based on innovative material systems have been studied in laboratories throughout the world. In the meantime, research and development efforts to minimize the cost of energy production are being intensified for mature technologies such as silicon-based solar cells.

Almost 60 years ago, the first crystalline silicon solar cell with an efficiency of 6% was developed [3]. Research and development have been flourishing for decades. Industrial-scale production of the 25 percent efficient commercial crystalline solar cell has been made possible by rapid advances in technology from the laboratory [17]. While other materials may be more difficult to come by, silicon's non-toxicity and well-developed support technology make it an attractive alternative. Crystalline silicon solar cells continue to dominate the PV market despite extensive research into several other types of solar cells. Figure 2.1 shows that crystalline silicon solar cells account for the vast majority of currently deployed solar cell modules [19].

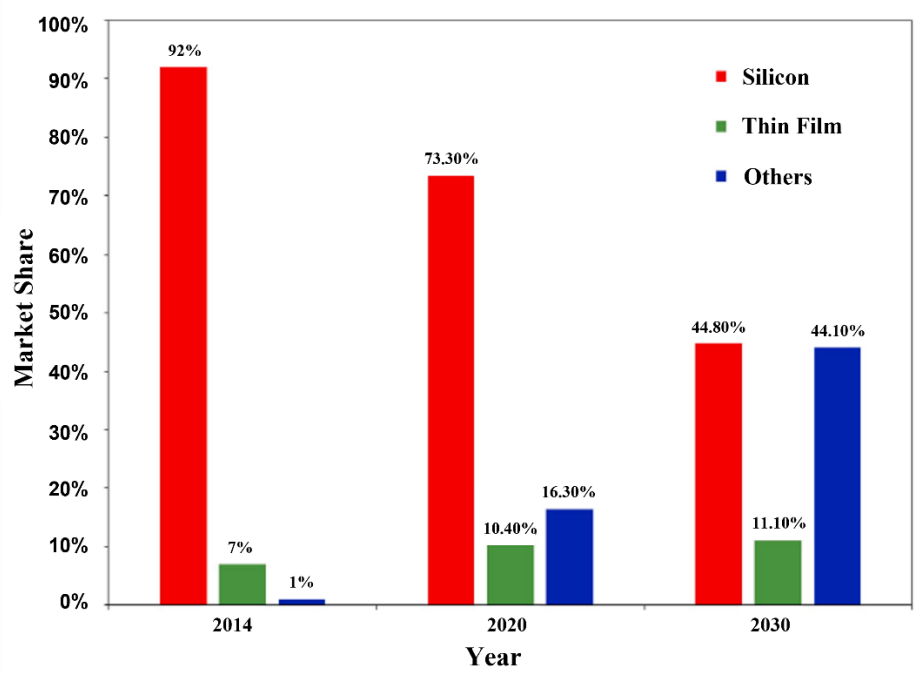

Figure 2.1. PV module market share by the material system (2014-2030) [19].

2.2 Photovoltaic Effect and the Working Principle of the Photovoltaics

The photovoltaic effect is the mechanism through which a solar cell transforms sunlight into electricity. Overall, the photovoltaic effect is the result of a series of three processes:

a) Photon absorption by substance

b) Separation of photogenerated carriers

c) Collection of separated charge carriers at the junction's terminals [20].

When a semiconductor absorbs a photon with sufficient energy ($h\upsilon$) higher than its bandgap (E_g), an electron will be excited from an initial energy level of E_i to a higher level of E_f, ($h\upsilon = E_f - E_i$). The excited electron moves from the valence band (E_v) to the conduction band (E_c) in a semiconductor and left behind a hole in the valance band. Accordingly, an electron-hole pair will be generated as shown in Figure 2.2 and this phenomenon is called electron-hole pair generation.

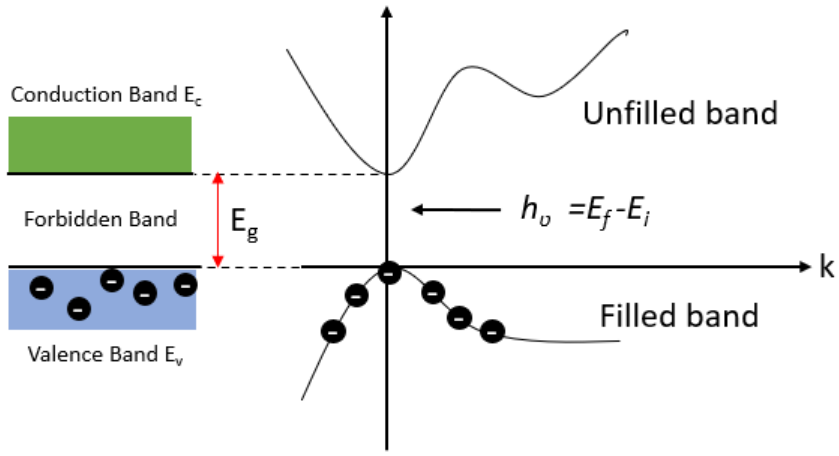

Figure 2.2. Electron-hole pair generation in a semiconductor by absorbing sufficient photon energy.

A typical solar cell is made of two layers with different doping types which results in different majority carriers at each layer. This layer with the electron majority carrier is called the n-type layer and the other layer with the hole as the majority carrier is known as the p-type layer. The n-type and p-type layers can be different materials which are known as heterojunctions or the same material which is known as a homojunction solar cell. For both kinds of cells, the working principle is the same. In presence of the incident light, the semiconductor will absorb the photons with higher energy than the bandgap and electron-hole pairs will be generated. After electron-hole pair generation, the generated carriers should be separated to prevent the electron from returning to the initial level, valance band, and recombining with holes. At this step n-type and p-type layers play the role and separates the photogenerated carriers before they become recombined. The built-in electric field in the depletion region at the interface of the two layers will separate the carriers. Accordingly, photogenerated carriers move to the layer where they are the majority. The photogenerated hole in the n-type layer move to the p-type region and the generated electrons in the p-type region move to the n-type. This implies that the separation process should take less time than the electron lifetime [21]. After the separation step, the carriers moved to n-type and p-type layers should be collected by electrical contacts. Finally, The chemical energy of the electron-hole pairs is subsequently transformed into electric energy when these electrons recombine with the holes generated in the valence band [21]. The whole process is shown in Figure 2.3.

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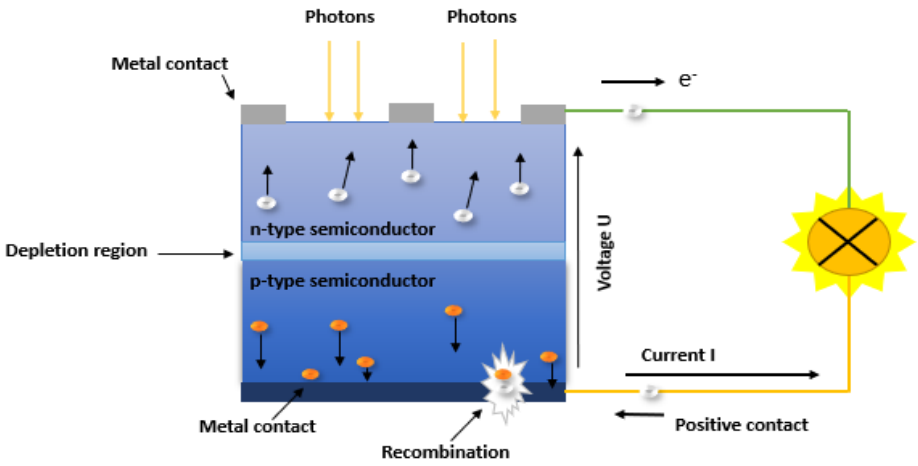

Figure 2.3. Electron-hole pair generation, separation, and collection by an external circuit for a typical single-junction solar cell.

2.3 Current Density-Voltage (J-V) Characteristics of Solar Cell

In solar cells, the more common word "current density" (J), which is the current per area value, is commonly used as an alternative to current (I), and the I-V curve of a solar cell is usually referred to as the J-V curve.

In dark conditions without any illumination, a typical single-junction solar cell works like a diode. There will be a current which flows through the solar cell and is related to the majority carriers of electrons in the n-type layer diffusing to the p-type layer where holes are the majority carriers. This current is called I_{Dark} and defines the I-V characteristic of a forward-biased diode. On the other hand, for a solar cell under illumination, there will be a flow of photo-generated carriers toward the electrical contacts. This current is called drift current and flows in the opposite direction of the diffusion current. Accordingly, by illuminating a solar cell under the standard test conditions (STC) of air mass (AM) 1.5 and an incident power density of 100 mW/cm^2 at 25 °C, the current density-voltage (J-V) characteristics of the solar cell can be achieved. The output current of a solar cell is defined as [21], [22];

$$I = I_{Dark} - I_L = I_0\left(e^{qv/nkT} - 1\right) - I_L \tag{2-1}$$

Where I_{Dark} is related to the carrier flow through the solar cell in a dark situation, I_L is the current flow of photogenerated carriers under illumination, I_0 is defined as the saturation current density, n is the ideality factor, v is the applied voltage, q is the electronic charge, k is the Boltzmann's constant, and T is the temperature in degrees Kelvin. Since photocurrent has a negative value since it flows in the opposite direction of the electrons, equation 2.1 is can be rewritten as [21], [22]:

$$J = J_L - J_0\left(e^{qv/nkT} - 1\right) \tag{2-2}$$

A typical J-V curve of a standard solar cell under dark and light conditions is presented in Fig. 2.3. The important parameters for solar cell characteristics such as the short-circuit current density (J_{SC}) and the open circuit voltage (V_{OC}) are also indicated in Figure 2.4.

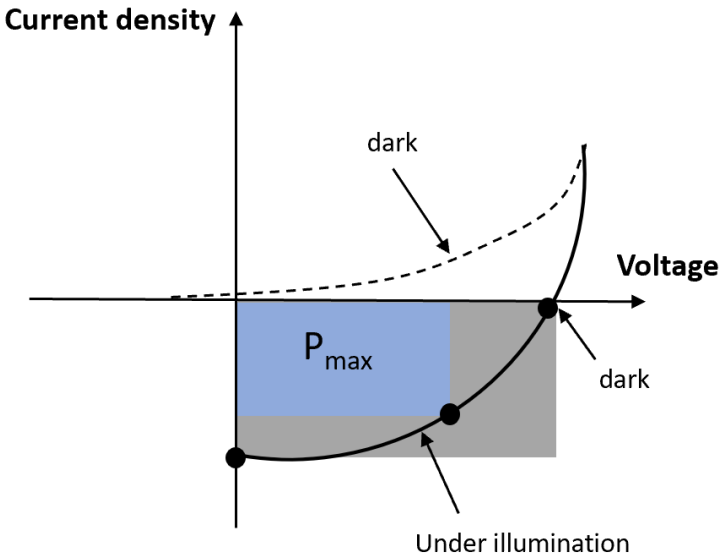

Figure 2.4. The *J-V* characteristics of a typical solar cell in dark and light conditions.

The J_{SC} is the maximum current density when the electrical contacts of the solar cell are short-circuited and there is not any applied potential. The active area of the solar cell affects the value of the J_{SC}. V_{OC} is defined as the maximum voltage that can be supplied by a solar cell where there is not any current density.

By assuming zero current density, V_{OC} can be defined as [21], [22]:

$$V_{OC} = \frac{kT}{e} ln\left(\frac{J_L}{J_0} + 1\right) \tag{2-3}$$

According to the equation. 2.3 it can be concluded that the saturation current and the photocurrent densities control the value of the V_{OC}. Both J_{SC} and V_{OC} values decreases as the dark diffusion current or recombination rate increases.

fill factor (*FF*) which is the other important parameter for photovoltaic characterization is defined as [21], [22],

$$FF = \frac{P_{max}}{V_{OC}J_{SC}} = \frac{V_{MPP}J_{MPP}}{V_{OC}J_{SC}} \tag{2-4}$$

Where P_{max} is the maximum power density which is indicated in Figure 2.3 as the rectangle area. The value of the P_{max} can be obtained from two parameters of the current density (J_{MPP}) and voltage (V_{MPP}) which are related to a maximum power point (*MPP*).

The last and most important parameter for solar cell characterization is the power conversion efficiency (*PCE)* which is the ratio of the generated electrical energy to the input solar energy. The power conversion efficiency (*PCE*) or common efficiency (η) is defined as [21], [22],

$$PCE = \frac{P_{max}}{P_{in}} = \frac{V_{OC}J_{SC}FF}{P_{in}} \tag{2-5}$$

Where P_{max} is the maximum output power of a solar cell which can be obtained as a product of the voltage and current of the system and P_{in} is the incident light power on the solar cell (100 mW/cm^2).

2.4 Loss Mechanisms

In photovoltaic technology, the cost of crystalline solar cells needs to fall below 0.5-0.75 dollars per watt of peak power to be competitive without government subsidies. For this goal, it is critical to decreasing solar cell losses as much as possible. The loss mechanism in solar cells can be classified as electronic and optical losses. Optical losses reduce the absorption of solar radiation by surface or rear reflection and shading of the top contacts. The electrical losses refer to majority carrier recombination mechanisms which result in the annihilation of the photogenerated carriers.

2.4.1 Electronic Losses

Electronic losses are related to electron-hole pair recombination processes which decrease the both J_{SC} and V_{OC} values. The recombination processes can be divided into four mechanisms,

- Radiative recombination
- Auger recombination
- Shockley-Read-Hall (SRH) recombination
- Surface recombination

The schematics of each recombination mechanism are provided in Figure 2.5.

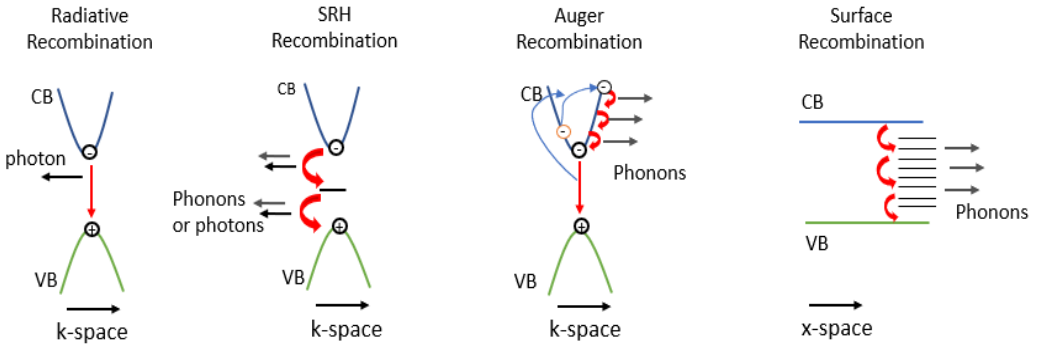

Figure 2.5. Schematic of electronic loss mechanisms for a photovoltaic.

Radiative recombination refers to a process in which a free electron in the conduction band releases energy and drops to a lower energy level of the valance band. During the process, a photon will result as a result of the energy loss of the electron. The recombination rate for this process is directly related to the concentration of carriers in the conduction and valance band. It is shown by U_{rad} and is defined as [21], [22],

$$U_{rad} = Bnp = B(\Delta n + n_0)(\Delta p + p_0) \tag{2-6}$$

Where B is the radiative recombination coefficient, n is the electron concentration in n-type and p is the hole concentration in p-type layers. Δn and n_0 refer to the concentration of photogenerated and thermally equilibrium free electrons, respectively. Same as, Δp and p_0 indicate the concentration of photogenerated and thermally equilibrium free electrons, respectively.

Auger recombination refers to a situation where an electron drops to the valence band from the conduction band recombining with a hole and resulting in the excitation of a third carrier which absorbs the released energy. The third carrier can be an electron or hole. Accordingly, the Auger recombination rate can be defined as [23],

$$U_{Auger} = C_n n^2 p + C_p n p^2 \tag{2-7}$$

Where C_n and C_p are the coefficient of Auger recombination for electrons and holes, respectively. According to equations 2.6 and 2.7, since the radiative recombination is linearly dependent on carrier density and the Auger recombination rate is proportional to carrier density squared, it can be concluded that the Auger recombination will be stronger and more dominant at higher doping concentrations.

Shockley-Read-Hall (SRH) recombination is related to defects in the material. Crystal defects and impurities introduce energy levels in the bandgap. In the SRH recombination process, an excited electron is trapped in the defect stated which causes energy loss. As a result of energy loss, the electron will recombine with a hole in the valence band. The SRH recombination rate can be written as [21]–[23],

$$U_{SRH} = \frac{np - n_i^2}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)} \tag{2-8}$$

Where τ_{p0} and τ_{n0} are the carrier lifetimes, and n_1 and p_1 are the concentration of the trapped electrons and holes, respectively. The value of the n_1 and p_1 depends on the defect parameters and can be defined as,

$$n_1 = n_i exp^{\frac{(E_t - E_i)}{KT}} \quad \text{and} \quad p_1 = p_i exp^{\frac{(E_t - E_i)}{KT}} \tag{2-9}$$

Where n_i and p_i are the concentration of the intrinsic carriers and the E_i is the intrinsic energy level. The E_t is the energy level of the trap, K is the Boltzmann constant and the T is the temperature.

Surface recombination has an undeniable role in solar cell performance. Surface dangling bonds that exist due to the surface roughness or discontinuity in the structure of the crystal are the main source of this recombination as illustrated in Figure 2.6. They can create a large density of trap states in the bandgap [21]–[23].

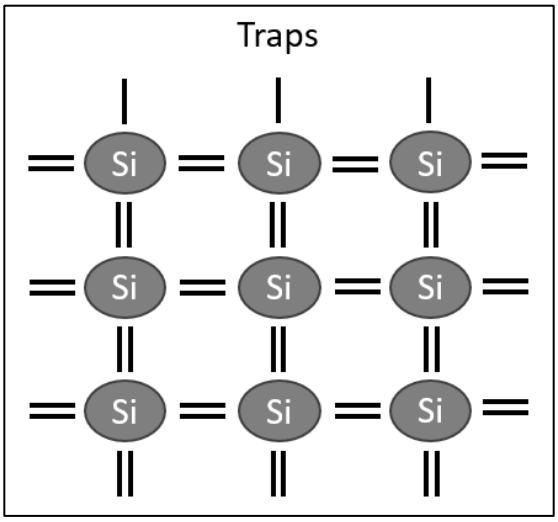

Figure 2.6. Dangling bonds act as traps at the silicon surface.

The surface recombination rate U_s can be defined as [21]–[23],

$$U_S = \frac{n_s p_s - n_i^2}{\frac{n_s + n_1}{S_{p0}} + \frac{p_s + p_1}{S_{n0}}} \tag{2-10}$$

Where n_s and p_s are the electron and hole concentrations at the surface of the substrate. S_{p0} and S_{n0} are the recombination velocity of the carriers which is related to the thermal velocity of the carrier, capture cross-section of carriers, and density state of conduction and valence band.

2.4.2 Optical Losses

Optical losses for a common photovoltaic cell reduce the solar cell performance by decreasing the J_{sc}. The main sources of optical losses can be listed as,

- Surface Reflection.
- Shading by the top contacts.
- Reflection of the rear surface.

The schematic of the optical losses is illustrated in Figure 2.7.

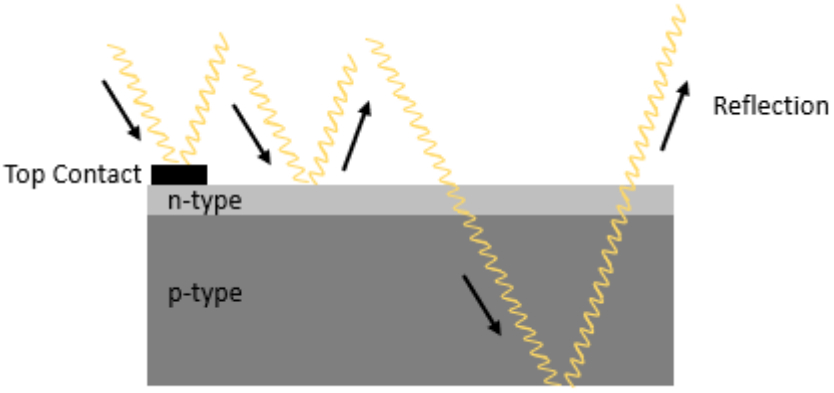

Figure 2.7. Schematic of optical loss mechanisms in a typical solar cell.

For Si semiconductors with a bandgap of 1.1 eV, the whole visible spectrum 350-780nm can be absorbed and generate electron-hole pair. But silicon has a high reflectance due to its high coefficient index within the wavelength range of 300-1000 nm. The high reflection of silicon results in a great optical loss since nearly 40% of the incident light which could generate electron-hole pairs is reflected [24].

The other optical loss is related to the shading of the front contacts which presents part of the incident light to be absorbed. Also, the part of the incident light which goes through the junction and reaches the rear contact can be reflected again and leaves the junction without absorbing [24].

2.5 Strategies to Overcome the Loss Mechanisms

Over the years many research groups introduced new strategies to overcome the loss mechanisms in solar cell technology to increase efficiency. Some of the well-known and common strategies are surface passivation, anti-reflection coating, and surface

texturing [25]. Using these strategies, new solar cell structures such as PERC [26], IBC [27], DASH [28], tandem [29], etc, are reported with improved performance.

2.5.1 Passivation

There are two well-known methods for minimizing surface recombination, Surface passivation and excess concentration of minority carriers [21]. For surface passivation, dielectric layers such as SiO_2, Si_3N_4, or Al_2O_3 can be deposited on the Si surface by different techniques such as ALD, PECVD, and APCVD to passivate the dangling bonds at the surface [30], [31]. Accordingly, the density of interlayer states will be decreased which results in less recombination. The second method is the excess concentration of the minority carriers. In this method, the interface can be heavily doped to push away the minority carriers at the substrate surface [30].

A silicon surface passivated by an atomic layer deposited (ALD) Al_2O_3 is presented in Figure 2.8. A complete deposition cycle starts with the formation of Si-OH (hydroxyl bonds). The first precursur TMA ($Al(CH_3)_3$) is then sent. The hydroxyl bonds react with TMA forming CH_4 molecules and accordingly, there won't be another reaction due to the self-limiting. Then an inert gas is sent to remove the excess TMA. The second precursor H_2O is then introduced which reacts with Si-O-$Al(HO)_2$ to facilitate the adjacent Al-O bonding. Finally, another inert gas is sent to take away the CH_4 byproduct and H_2O molecules. Since a single layer will be deposited by a complete single cycle, the number of cycles controls the thickness of the deposited layer [32].

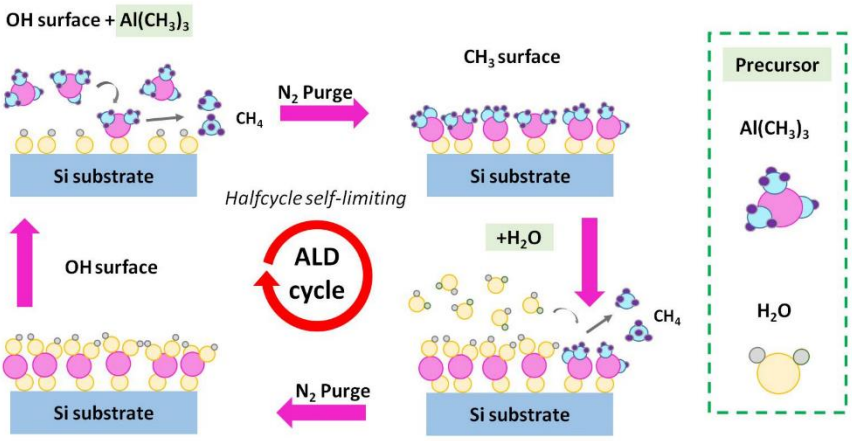

Figure 2.8. Silicon surface passivation with atomic layer deposition of Al_2O_3 [32].

2.5.2 Antireflection Coating

Over the years, different methods were introduced to decrease optical losses. Above them, there are two main well-known strategies to decrease the reflection of the silicon: antireflection coating (ARC) and surface texture [33].

By depositing the ARC layer it is possible to decrease the reflection significantly which depends on the reflective index and thickness of the ARC material. The mechanism is illustrated in Figure 2.9. By using multiple ARC layers it is possible to achieve even zero reflectance. The reflectivity for a single-layer ARC can be calculated by [21],

$$R = |r^2| = \frac{r_1^2 + r_2^2 + 2r_1 r_2 cos2\theta}{1 + r_1^2 r_2^2 + 2r_1 r_2 cos2\theta} \tag{2-11}$$

Where,

$$r_1 = \frac{n_0 - n_1}{n_0 + n_1} \quad and \quad r_2 = \frac{n_1 - n_2}{n_1 + n_2} \tag{2-12}$$

$$\theta = \frac{2\pi n_1 t_1}{\lambda} \tag{2-13}$$

Where n_0 is the reflective index of the surrounding region which is air, n_1 and t_1 are reflective index and thickness of the ARC and n_2 is the reflective index of the silicon.

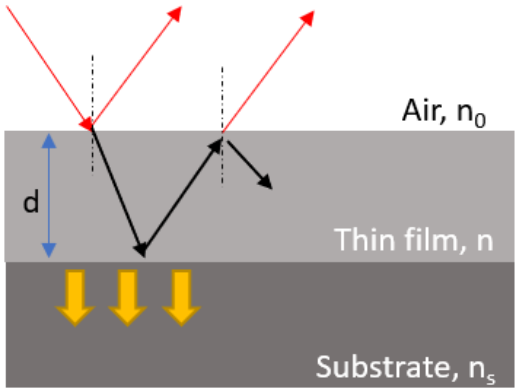

Figure 2.9. Schematic of multiple reflections of light in the single-layer antireflection coating.

2.5.3 Surface Texturing

The other well-known strategy to reduce silicon reflectance is surface texturing. This structure increases the optical path inside the cell through multiple light reflections. The incident light bounces inside the material and nearly 33 % of the light will be absorbed. This phenomenon is called “Light trapping” [34]. The most commonly used method for this approach is fabricating random pyramids by chemical etching of silicon. However, this method has disadvantages such as high material consumption and also the height of the pyramids which is about 5-10 micrometers which is comparable to the thickness of the thin film solar cells. Accordingly, for years lots of methods such as nanoholes, nano-cones, nano-pillars, etc. used for surface texturing [35]. Principles of the different strategies used for light trappings, such as random pyramids, nanostructures, and reflecting back-layer are presented in Figure 2.10. The surface texturing method is discussed in detail in Chapter 4.

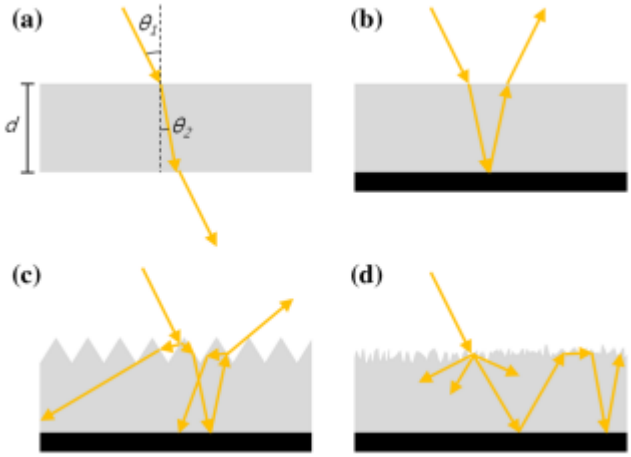

Figure 2.10. Light path through a) single layer b) multilayer with a reflecting layer on the back and light trapping through multiple reflections in c) periodic pyramid structures and d) irregular micro-nanostructure on top [35].

2.6 Schottky Junction Solar Cells

In the previous section, the solar cells based on the p-n junction were discussed in detail. Over the years many different structures and various strategies are reported for p-n junction solar cells and high efficiencies are achieved as well. But since the doping process is a high-temperature and high-cost process, it increases the manufacturing cost of the p-n junctions. Accordingly, the focus is on finding a technique to mass-produce solar cells at a reduced cost. The manufacture of Schottky junction solar cells is shown to be easier than that of p-n junction solar cells. When a metal and a semiconductor like silicon come together, in case of a sufficient energy difference between their work functions, a Schottky junction will be formed [27]. The schematic of a Schottky junction is presented in Figure 2.11.

In the case of the Schottky junction, the carrier generation process takes place in the silicon substrate. The advantage of this structure is the fact that the optical loss decreases due to the high absorption of the metal.

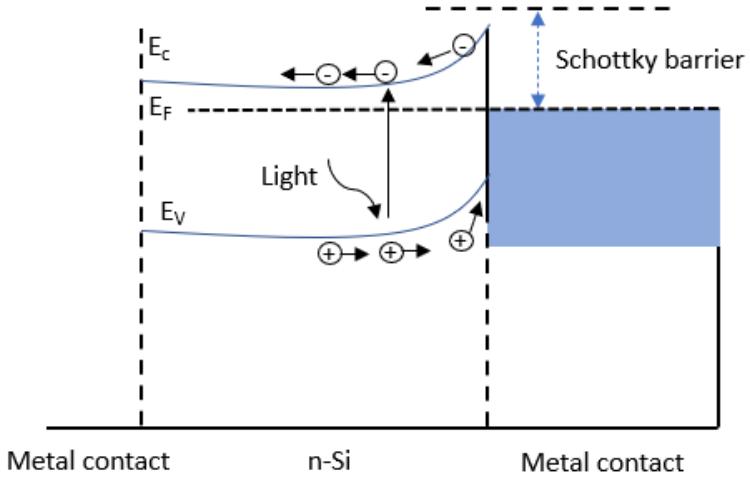

Figure 2.11. Energy band diagram of a Schottky junction solar cell.

For the first introduced Schottky junction solar cell, indium-tin-oxide (ITO) film is used as the metal layer to decrease the optical loss [36], [37]. On the other hand, the indium resources are limited which again results in the high-cost manufacturing of Schottky junction solar cells. The other issue related to indium is the diffusion of indium ions which degrades the performance of the device. Also, the application of ITO in flexible solar cells is limited due to its brittle nature [38]. Due to all these reasons, the need for better material arises, and CVD-grown graphene, which has excellent physical and chemical properties attracted the attention of the researchers. The properties of graphene and its application in Schottky junction solar cells are described in detail in the next chapter later. For Gr/Si Schottky junctions, the optical loss is also eliminated due to the near-zero band-gap nature of graphene [38]. As a result, using graphene to make low-cost, flexible, and high-performance solar cells is a viable option. However, the production of large-scale Gr/Si Schottky solar cells with high efficiency is still a great challenge. The graphene properties and the principle of Gr/Si Schottky junctions are presented in detail in the next chapter.

CHAPTER 3

GRAPHENE, ITS PROPERTIES AND APPLICATION IN GRAPHENE/SILICON SCHOTTKY JUNCTION SOLAR CELLS

Carbon, one of the most prevalent elements in the crust of the Earth and the whole universe, is essential for the survival of all life forms on the planet. Materials like graphite, diamond, and amorphous carbon are all naturally available three-dimensional allotropes of carbon that have been utilized for thousands of years [39]. Scientists have only recently started to study and synthesize reduced-dimension Carbon allotropes. It was in 1985 that the Zero-dimension allotrope of carbon, Fullerenes (buckyballs), was first introduced [40]. Later in 1991, a one-dimension carbon allotrope named carbon nanotubes was introduced [41]. As a result of their unusual physical and electrical properties, these allotropes attracted a great deal of scientific attention [42].

Novoselov et al. in 2004 [43], isolated a two-dimensional (2D) allotrope of carbon, known as a single layer of graphene, from bulk graphite successfully for the first time and demonstrated to exist in a stable state. A mechanical exfoliation method known as “Scotch tape” was used for this process. Graphene has a wide range of applications in a variety of fields ranging from optoelectronics to biomedical research. It is a two-dimensional material with remarkable mechanical, electrical, optical, and thermal capabilities [44]. Optical absorption of graphene is frequency independent and is defined just by the fine structure constant through the whole visible and near-infrared spectrum ($\lambda < 2\mu m$) and beyond. Moreover, single-layer graphene was shown to have a tunable bandgap [45]. Because of its unique features, graphene is likely the most researched material, having applications in electronics, optoelectronics, energy storage, composite materials, and biomedicine [44]–[48]. This chapter introduces the physical and electrical structure of graphene, as well as how these qualities lead to unique electronic and optical capabilities.

3.1 Characteristics of Graphene

Graphene is a monolayer of carbon atoms and consists of densely packed sp^2-hybridized carbon atoms. According to the single sheet structure of graphene, it can be concluded that its thickness will be equal to the thickness of a single carbon atom which is about 0.335 nm [44]. This makes graphene the thinnest film synthesized ever. The 2D honeycomb structure of graphene is illustrated in Figure 3.1.

There are four electrons available in the outer shell of the carbon which can bond to create bonds with other atoms. In graphene, since it is a single layer of carbon atoms bonded to each other, three of the four outer shell electrons are bonded to the neighbor atoms forming σ-bonds. Graphene's extraordinary mechanical robustness and elasticity are due in large part to these incredibly strong -bonds. Except for ionized hydrogen, graphene without defects in its structure is shown to be impermeable to all standard gases, including helium [49].

It is possible to depict the graphene structure as a triangular lattice with two sublattices of A and B. In real space the two lattice unit vectors a_1 and a_2 are defined as [50];

$$a_1 = \frac{a}{2}\left(3, \sqrt{3}\right) \quad and \quad a_2 = \frac{a}{2}\left(3, -\sqrt{3}\right) \tag{3-1}$$

where a is the distance between two neighbor carbon atoms which is 0.142 nm. The lattice constant is defined as the distance from one carbon atom to the second nearest carbon atom and it is equal to 0.246 nm. The lattice constant is also the same as the length of the lattice vectors which defines the first Brillouin zone (Fig. 2.1(b)) and can be shown as [50];

$$b_1 = \frac{2\pi}{3a}\left(1, \sqrt{3}\right) \quad and \quad b_2 = \frac{2\pi}{3a}\left(1, -\sqrt{3}\right) \quad with \quad |b_1| = |b_2| = \frac{4\pi}{\sqrt{3}a} \tag{3-2}$$

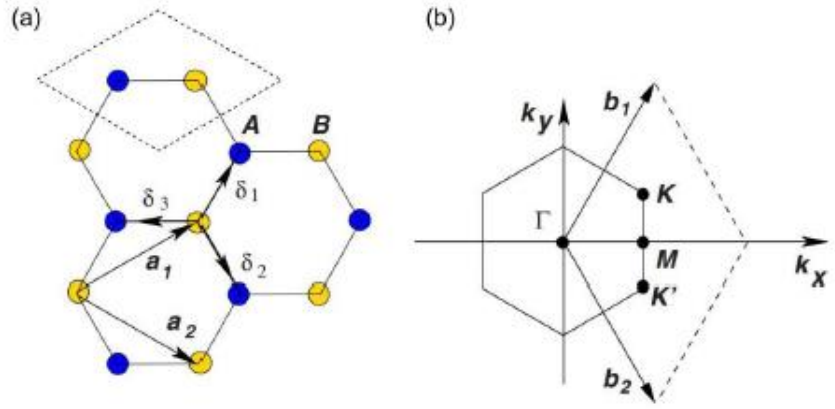

Figure 3.1. Lattice structures of graphene. (a) Honeycomb lattice in real space with a basis of two atoms shown as A and B. (b) Honeycomb lattice in the reciprocal space. Lattice vectors are b_1 and b_2 and Dirac points are K and K′.[39].

3.1.1 Electronic Properties

Graphene has extraordinary electrical properties. Since the band structure of graphene is characterized by an approximation of the Dirac equation at the low energy limit, charge carriers in graphene act like massless Dirac fermions. When tested on a SiO_2 substrate at room temperature, it was discovered that graphene's massless charge carriers had a mobility of up to 15,000 cm^2/V_s [51]. Increasing the suspended device improvement by a factor of up to 2×10^5 cm^2/V_s [16]. All these properties attract the interest of scientists to use graphene for electronic devices.

3.1.1.1 Bandgap

The key element which is the source of the unique electrical properties of graphene is its free fourth electron in the outer shell which is oriented out-of-plane. The orbital of one atom overlaps with the orbital of its neighbor atom because of the small lattice constants of graphene. Accordingly, bonds can be formed due to the hybridization of these orbitals. The phase non-bonded electrons of higher energy create the conduction band whereas in phase bonding-electrons with lower energy create the

valence band. As illustrated in Figure 3.2 the conduction and valence band meet each other at a point known as Dirac point (K-points) and makes a cone-shape [52]. It makes graphene a semiconductor with a zero-band gap and a linear dispersion relation. In the case of the increased number of layers, the band structure deviates from the linear dispersion. The valence and conduction bands overlap slightly in graphite, which is typical of semimetals. By employing the tight-binding model, the electronic band structure of graphene was accurately shown. A detailed calculation is provided in [52], which leads to the band structure of graphene as depicted in Figure 3.2.

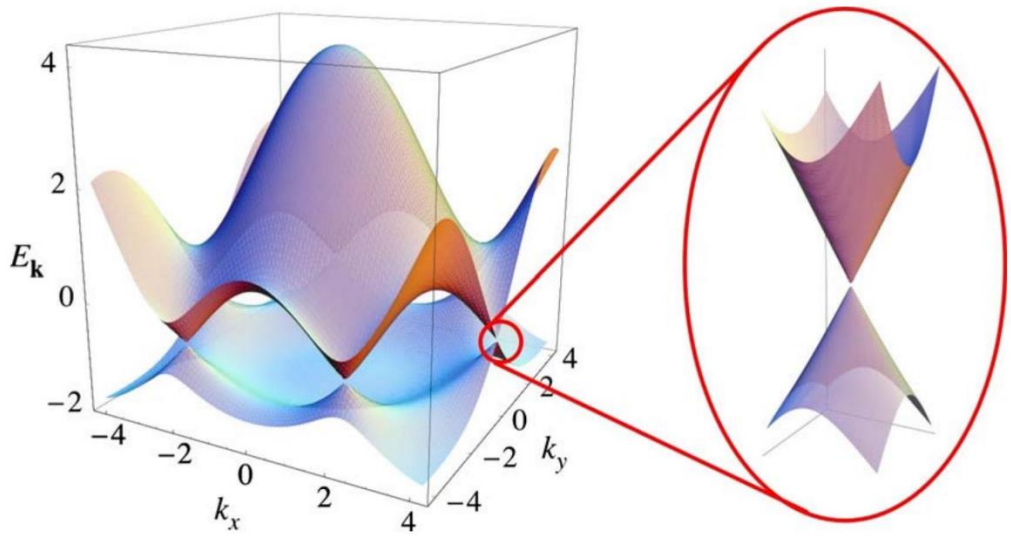

Figure 3.2. Electronic band structure of graphene, indicating the energy bands of one of the Dirac points [52].

Graphene has six Dirac points placed at corners of the Brillouin zone where the low energy dispersion relation would be represented as a linear equation [52]:

$$E_{\pm}(k) \approx \hbar v_f \sqrt{k_x^2 + k_y^2} = \pm \hbar v_f k \tag{3-3}$$

Where k is the wave vector in the Brillouin zone, h is the Planck constant and v_f is the Fermi velocity which is nearly 10^6 ms^{-1}.

3.1.1.2 Density of States and Doping Density

The number of possible states at a specific energy interval that can be occupied by an electron is called the density of states (DoS). The number of states that are occupied by electrons per unit area is the carrier density which is also referred to as doping density. According to the zero-bandgap behavior of graphene and its linear dispersion, the DoS is very low near the Dirac point. However, it increases as moving away from the Dirac point and is directly proportional to the energy difference. At an energy level of 1 eV away from the Dirac point density of the state reaches $10^{14}cm^{-2}$ eV^{-1}. For stable and undoped graphene, the Fermi level is located at the Dirac point at charge neutrality and separates the occupied and unoccupied states. The position of the Fermi level changes as carrier concentration changes by doping. Like as a typical semiconductor, by doping the graphene with electrons or holes (n-type or p-type), the Fermi level shifts to higher or lower energy states and moves up or down with respect to Dirac point [53]. The change of Fermi level by doping is presented in Figure 3.3.

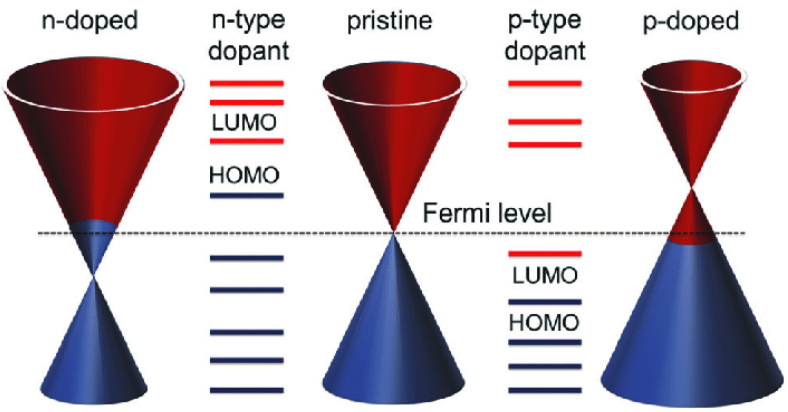

Figure 3.3. Band diagram and work function of doped and un-doped graphene [54].

3.1.1.3 Carrier Mobility

As mentioned before, the charge carriers in graphene act like massless Dirac fermions because of the low energy linear dispersion relation. It results in extraordinarily high carrier mobilities which makes graphene an ideal material for

high-speed electronic and optoelectronic devices. The carrier density, grain size, density of defects, cleanliness, contact with the substrate, temperature, and the number of layers are all variables that could affect the mobility of charge carriers in graphene [55]–[57]. The maximum carrier mobility value for mobility in graphene is theoretically calculated as $2x10^5$ cm^2/Vs at room temperature [16], [57]. For devices with graphene akes enclosed by hexagonal boron-nitride (h-BN) capping layers, mobility values of 10^5 cm^2/Vs are reported [58], [59]. The high mobilities for such devices are related to the flat surface of h-BN and discarding the interaction with the ambient atmosphere. For graphene layers deposited on SiO_2 substrate the room temperature mobility is decreased to values less than 10^4 cm^2/Vs. This degradation is related to the roughness of the substrate surface, impurities, and the charged surface states [60].

3.1.2 Optical Properties

Graphene has unique optical properties owing to its perfectly symmetric and zero bandgap energy band structure. The interface-like contrast makes it possible to find and recognize the graphene transferred or deposited on the SiO_2 substrate however, it has one atom thickness of 0.34 nm. This contrast can be easily detected by the naked eye. The real part of the optical conductance of graphene depends on the wavelength and can be shown as by [61]:

$$G_0 = \frac{q^2}{4\hbar} \approx 6.08 \times 10^{-5}\ \Omega^{-1} \tag{3-4}$$

The fine structure constant is the only physical factor that affects the graphene's optical absorption and transmission in theory and can be calculated as [61],

$$\alpha = \frac{q^2}{\hbar c} = \frac{1}{137} \tag{3-5}$$

By applying Fresnel equations in the limit of the thin film the graphene transmittance can be defined as [61]:

$$T = \frac{1}{(1 + \frac{2\pi G_0}{c})^2} = \frac{1}{(1 + \frac{\pi\alpha}{2})^2} \approx 1 - \pi\alpha \approx 97.7\% \quad (3\text{-}6)$$

For suspended graphene, the absorption of 97.7% is approved. It means 2.3% of incident light can be absorbed by mono-layer graphene within the whole visible spectrum (400-750 nm) [43]. Since graphene has a linear band structure at low energies close to the Dirac point, its absorption is nearly flat within the 300 nm to 2500 nm wavelength range [43]. On the other hand, for higher energy states away from the Dirac point, the nonlinearities in the bandgap increase. Accordingly, for higher frequencies, there will be a slight deviation from the absorption. The other parameter which affects the absorption of the graphene is the number of layers since every single layer absorbs 2.3 % of incident light over the visible spectrum [43].

Electrons excited by light have two possible optical transitions: interband and intraband, depending on whether or not they pass the Dirac point, owing to graphene's linear dispersion and zero bandgap. A graphene sheet's doping level and light intensity determine how much each process takes place. Single-layer graphene absorption of 2.3 % is constant at photon frequencies higher than the far-infrared range, which is defined by interbond transitions that are frequency-independent. Low-frequency spectrum regions, such as the far infrared and the terahertz (THz) range, are dominated by intraband transitions [43].

3.2 Fabrication Methods

Layered materials are synthesized using a variety of processes, which can be divided into two categories: "top-down" and "bottom-up" approaches, similar to the synthesis of all nanomaterials. The top-down technique is based on breaking the non-covalent bonds between layers to exfoliate the necessary 2D materials from the bulk material. In terms of exfoliation methods, mechanical and liquid phase exfoliation are the most common methods. In contrast to the bottom-up approach, a 2D structure is formed from small molecule precursors on a substrate such as well-known

chemical vapor deposition (CVD), physical vapor deposition (PVD), or epitaxial growth.

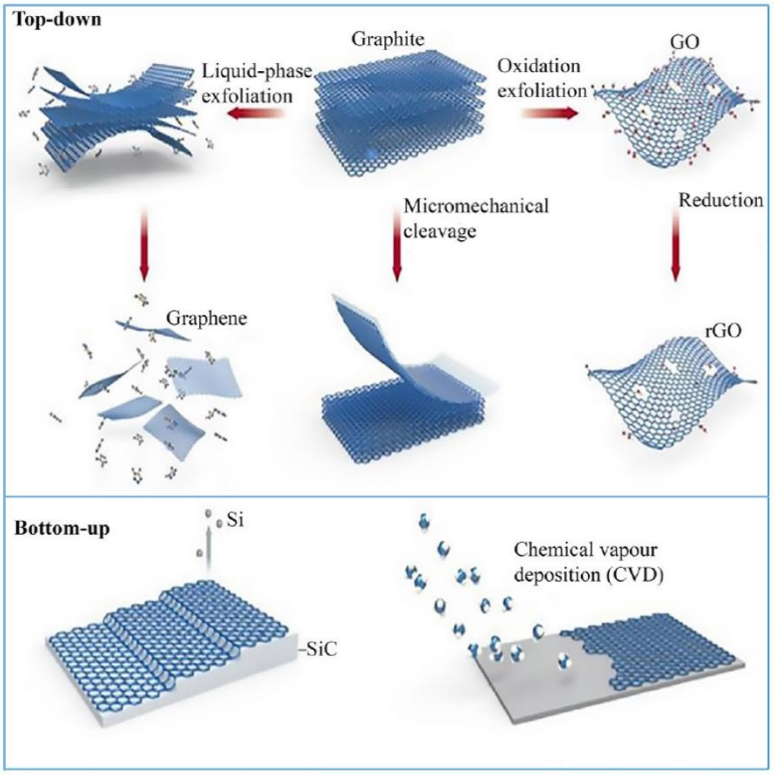

Figure 3.4. Fabrication of graphene can be divided into two categories: top-down and bottom-up approaches [62].

3.2.1 Mechanical exfoliation

There are many layers of graphene held together by weak out-of-plane van der Waals interactions in Graphite. To separate individual graphene layers from the bulk graphite, Vander Waals bonds must be broken [43]. Micromechanical exfoliation involves repeatedly peeling a piece of natural graphite between adhesive tapes to create a random combination of akes, which is then put on a SiO_2 substrate so that possible monolayers may be identified using an optical microscope. Single-crystalline graphene akes with a small density of defects and the greatest charge carrier mobility are produced by micromechanical exfoliation. Due to a lack of throughput and the small size of the akes, this method is not viable from an industrial

standpoint. To conduct basic research and proof-of-concept studies, micromechanical exfoliation has been widely used [59].

3.2.2 Liquid Phase Exfoliation

When compared to mechanical exfoliation, the key advantages of liquid phase exfoliation (LPE) are its high yield and scalability, however, the uniformity and quality of flakes degrade [63]. To reduce the force of van der Walls bonds between neighboring graphene layers, liquid phase exfoliation of graphite uses external pressures such as fast heating, shear mixing, or sonication. LPE is a two-step process that is typically done in aqueous solutions or organic solvents. In the first step, ultrasonic is used to detach layers from graphite powder distributed in a solvent, at the second step, akes of various sizes and thicknesses are subsequently separated from the unexfoliated material by performing sedimentation-based centrifugation [63].

Process factors like sonication intensity and time, as well as centrifugation rate and time, have a significant impact on the overall quality, yield, and also thickness distribution of exfoliated graphene akes in the resulting dispersion. Increasing the sonication period, for example, would result in a higher concentration of resultant but in a smaller size of the akes. Exfoliation of graphite in the LPE method can be improved by utilizing inorganic salts like NaCl, KCl, and LiCl. This improvement in the exfoliation process is due to the increase in the interlayer gap caused by the intercalation of anions and cations between graphite layers in presence of salts [64]–[66]. Accordingly, High power and long sonication process is not required fort his kind of LPE process which results in the final few-layer graphene akes as small as 100 microns. Note that, the presence of salts in solvent doesn't have any effect on the graphene purity, since they are dissolved in water and can be easily separated and cleaned just by a regular washing process in DI water. The salts can then be recycled for multiple uses [64]–[66].

In the end, LPE is an efficient and scalable method for producing graphene at a low cost. Although LPE graphene exhibits excellent electrical properties, the presence of chemical impurities and a narrow size distribution make it unsuitable for use in electronic devices.

3.2.3 Chemical Vapor Deposition (CVD)

In the semiconductor sector, CVD is a widely utilized and adaptable technology because it allows for a wide range of control over the synthesis process and the features of the deposited layer. In a common CVD growth process, one or more volatile precursors are exposed to a substrate, and their reaction causes the development of a thin film. A typical system for chemical vapor deposition is illustrated in Figure 3.5. It includes three main components of a transition metal foil which acts as a catalyst substrate, gas supplies, and reaction chamber capable of operating between 1000 and 1200C. The gas supplies contain inert gas as a carrier, a gas that contains carbon such as methane and hydrogen supply to control the reaction [67], [68].

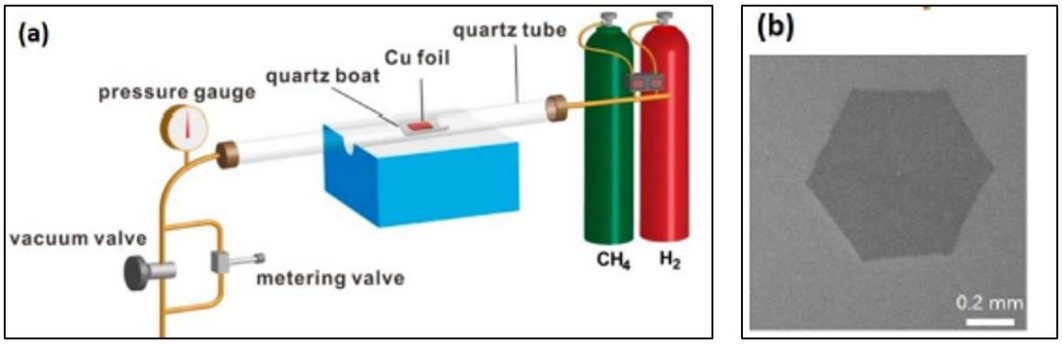

Figure 3.5. a) Schematic of a typical CVD growth process for graphene. (b) SEM image of a single crystalline graphene synthesized by CVD [68].

There are essentially six steps involved in the chemical vapor deposition method for the growth of graphene on a transition metal substrate. (i) adsorption and pyrolysis of CH4 on the metal surface; (ii) dehydrogenation of methane; (iii) diffusion/precipitation of carbon atoms to the metal surface; (iv) carbon nucleation

on the active sites of the metal surface; (v) growth of carbon domains through adsorbing carbon species on their edges; (vi) merging of neighbor graphene domains until the whole substrate is covered with polycrystalline graphene [67]. The synthesizing steps are provided in Figure 3.6

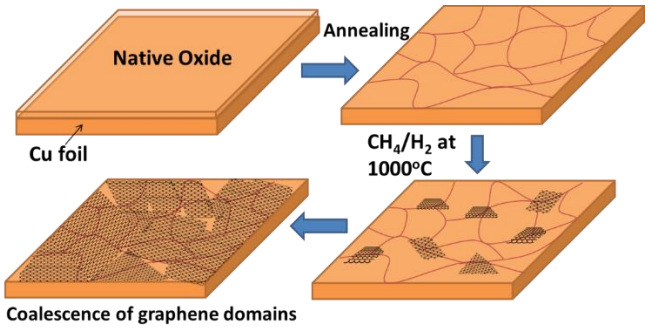

Figure 3.6 Schematic of the steps of the CVD growth of graphene films on metal substrates [69].

Conventionally, nickel (Ni) and copper (Cu) are the substrates of choice for the chemical vapor deposition of graphene [68]. for both of these substrates, the pyrolysis of methane happens at a lower temperature due to the catalytic function of their surfaces. However, because of their different carbon solubility, the produced graphene exhibits significant structural and thickness uniformity differences [68]. When the temperature is dropped, the carbon atoms dissolved in the Ni can diffuse or precipitate on the surface. As a result multilayer graphene can be synthesized. Accordingly, Ni substrate is favored for multilayer graphene growth. Due to the limited carbon solubility of Cu foil, decomposed carbon atoms are forced to remain on the surface to produce graphene. Also, Cu foil has self-limiting growth behavior. Accordingly, in the case of single-layer graphene growth, Cu foil is preferred [70]. CVD is a highly scalable technology, and it has been used to synthesize 60 cm CVD-grown graphene on copper foil using roll-to-troll procedures [70].

To achieve high carrier mobility, CVD graphene must exhibit polycrystalline nature and have a distribution of bigger domain sizes. CVD graphene's electronic properties vary from device to device because of the variable density of domain borders, which

is a critical issue that should be noted. To generate a big single-crystal graphene or polycrystalline graphene with a greater domain size distribution, the number of nucleation sites should be limited and the growth time should be increased.

3.3 Characterization Methods

As mentioned before graphene has a thickness of 0.335nm which makes it difficult to characterize. The quality and uniformity of the graphene depend on the fabrication process and steps. There are many different ways to detect the characteristics of graphene such as the optical microscope, Raman spectroscopy, scanning electron microscope (SEM), atomic force microscope (AFM), transmission electron microscope (TEM), infrared spectrum (IR), X-ray photoelectron spectroscopy (XPS) and ultraviolet-visible spectra (UV-Vis). But overall, the two well-known and most used methods which are unique for graphene are optical microscopes and Raman spectroscopy.

3.3.1 Optical Microscope

Graphene transferred or synthesized on SiO_2 substrates can be studied via optical imaging, which is easy, fast, and non-destructive. For the preliminary characterization of atomically thin materials, such as graphene, the optical microscope is used to determine the probable number of layers and any discontinuities in the structure, like artifacts, defects, and residues. Even a single layer of graphene on a SiO_2 substrate creates a distinct contrast with the background color of the oxide as the substrate layer. Using Fresnel equations, we may pinpoint the genesis of this contrast. Graphene sheets over oxidized silicon substrates can be made more visible by adjusting the thickness of the oxide layer and the wavelength of the light or filter used. The contrast between the graphene monolayer and SiO_2 substrate can be calculated by the Fresnel equation as a function of oxide thickness and light wavelength and the resulting color plot is presented in Figure 3.7. The maximum contrast at the 500-550 nm range, which is almost the middle of the visible

spectrum where the human eye is highly sensitive, can be achieved for oxide thickness is around 90 nm or 290 nm [71].

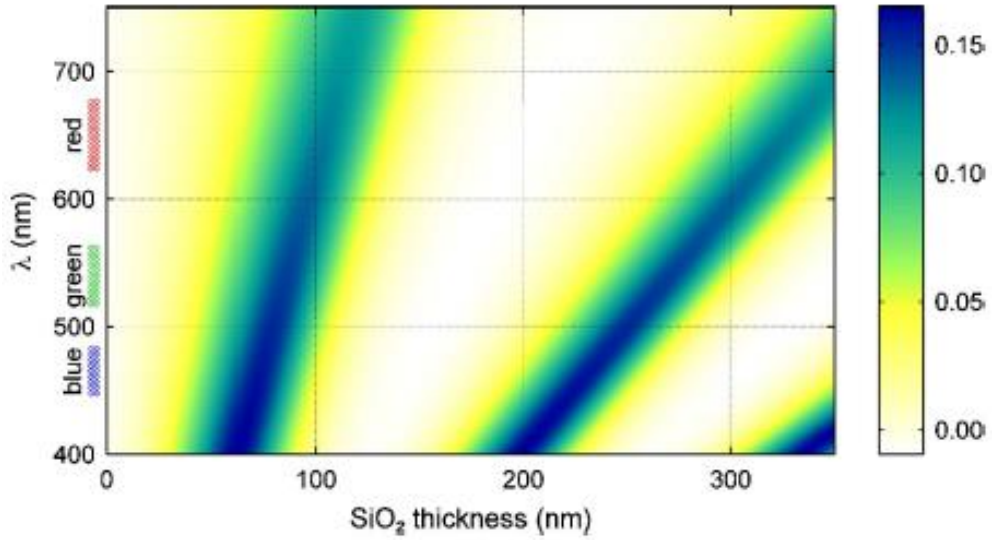

Figure 3.7. Optical contrast for graphene as a function of wavelength and SiO_2 thickness [71].

3.3.2 Raman Spectroscopy

Graphene and other layered materials can be characterized using Raman spectroscopy which is a strong non-destructive technique. Phonons are quasiparticles that quantize the inelastically scattered light from the material, which is caused by atomic vibrations. Wavenumbers (1cm) are commonly used to express the energy shift between the incoming and scattered light in energy analysis, making it possible to determine the number of graphene layers, doping, defects, and chemical changes [50], [71].

A common Raman spectrum of single-layer graphene has three major peaks of D, G, and 2D and is illustrated in Figure 3.8. The first peak is the D peak which is related to defects contributing to double resonance Raman scattering close to the Dirac point of the Brillouin zone as shown in Figure 3.9.a. Depending on the frequency of the laser and the presence of discontinuities and defects in the structure of graphene, the

position, and form of the D peak changes. It is commonly located at about 1350 cm-1 and has a low intensity [71], [72].

The double resonance Raman scattering occurs when an electron-hole pair is generated by a photon near the Dirac point in the first Brillouin zone (FBZ). In the next step, an electron absorbs a phonon and scatters into the second conduction band in the second Brillouin zone. To preserve energy and momentum, this electron must return to *K* before being recombined with a hole. In presence of a defect state, the electron scatters back elastically to the first conduction band [73]. Any fault in graphene structure such as asymmetries and vacancies, sp3-defects, and grain boundaries forms defects and defect levels [72]–[74]. In the end, a photon will be emitted because of the recombination of the electron with a hole. The process is shown in Figure 3.9. a.

The second peak which appears at about 1580 cm^{-1} is the G peak. It arises from the stretching of carbon bonds [75]. G peaks appear for whole sp2 carbon allotropes such as amorphous carbon, carbon nanotubes, and graphite [75]. The G peak arises in the frequency range of 1518 cm^{-1} to 1630 cm^{-1}, depending on the graphene's doping level [76]. In addition, as the number of graphene layers increases, the G peak energy decreases. This shows that the G peak provides information on the number of graphene layers. As illustrated in Figure 3.9.b an incident photon resonantly excites a virtual electron-hole pair in graphene, which leads to the formation of the G peak. At the next step, the electron recombines by a hole and a photon will be emitted. The energy amount transferred to the photon results in a redshift [77].

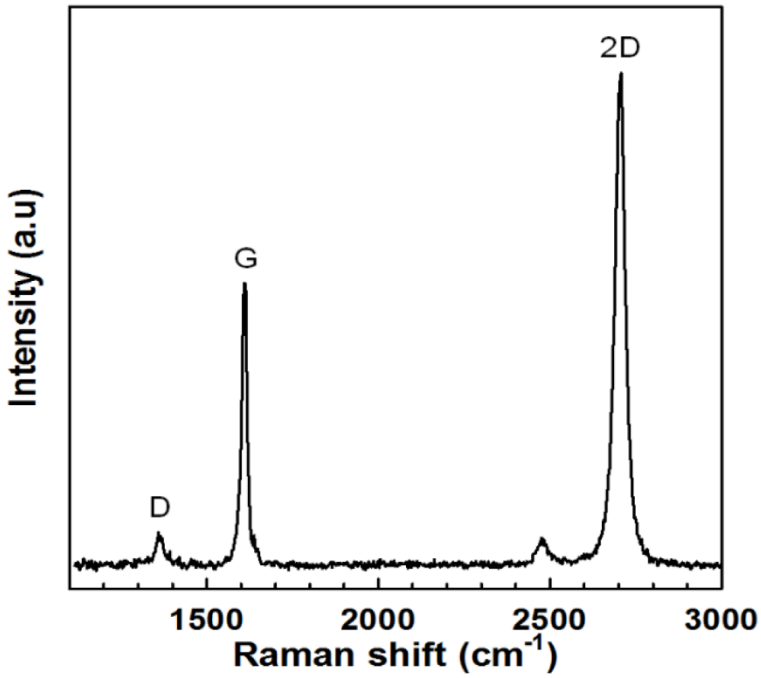

Figure 3.8. Raman spectrum of CVD- grown graphene transferred on SiO_2/Si substrate [24].

The last Raman peak of the graphene spectrum is the strongest one which is known as the 2D peak located near 2700 cm^{-1}. For a lower number of layers, the energy of this peak will be lower too. Also, the doping level of graphene changes the position of the 2D peak too. The mechanism of the 2D peak which is also known as the double resonant process is illustrated in Figure 3.9c. The electron which is excited by a photon at K point absorbs a phonon and scatters to the second conduction band at K′. Before becoming recombined with a hole, the excited electron should scatter back to the first conduction band by absorbing a second phonon. Accordingly, two phonons are needed for this process. Finally, a photon is emitted as a result of electron recombination in the valence band by a hole [72]. As it is illustrated in Figure 3.9c, the 2D peak mechanism can be triple resonant when the electron at the second Brillouin zone scatters by absorbing a second phonon and them recombines at the valence band of the first zone [72].

The intensity ratio between 2D and G peaks gives information about the monolayer nature and also the quality of the carbon. For single-layer graphene with high quality, 2D peak intensity is twice the G peak [78].

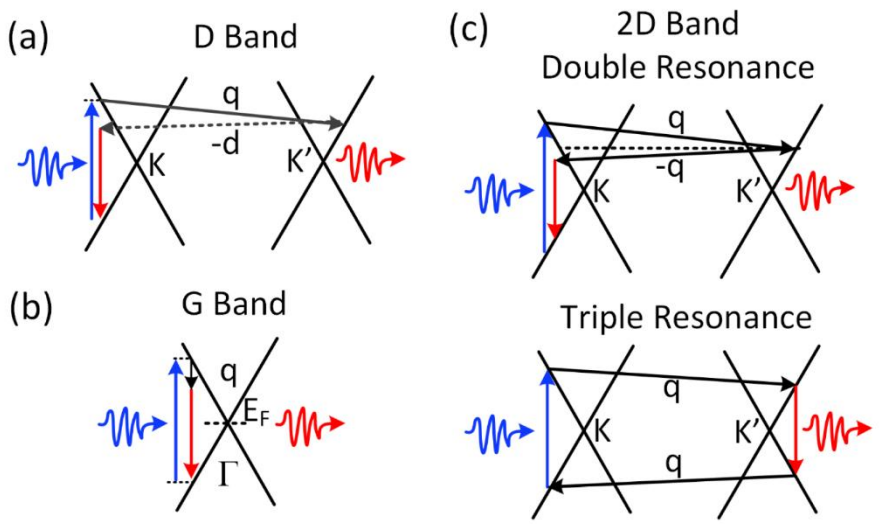

Figure 3.9. Mechanism of main Raman processes in graphene. (a) D band double resonant process scattering by a defect (b) G peak and (c) 2D peak generated through a second-order process, respectively [24].

3.4 Wet Transfer Process

To be used in electronic devices, graphene must be placed on insulating substrates like Si/SiO_2 wafers and glass. As a result, plasma-enhanced CVD is being used to grow graphene directly on insulating substrates like h-BN and Silicon dioxide, as well as on the interface of semiconducting crystals like Si [79] and Ge [80]. But in the case of CVD-grown graphene on a foil, a transfer method known as the wet transfer process is commonly used to transfer graphene on different substrates. This process has three main steps. In the first step, a thin film of Poly methyl methacrylate (PMMA) $(C_5O_2H_8)_n$ is spin-coated on CVD-grown graphene-on-metal. In the second step, the metal film beneath the graphene is etched in the proper etchant. After the metal is dissolved in the etchant, the PMMA/graphene stack is moved to DI water to

clean up the etching residues. As a final step, the graphene with the PMMA layer on it is transferred on the desired substrate. Finally, the PMMA layer is removed in acetone. The main issue associated with this transfer process the that it is not possible to get rid of PMMA residues with a standard acetone treatment. The PMMA residues increase the recombination, sheet resistance, and shift in the *K* point [24]. This process is discussed in detail in Chapter 5.

3.5 Graphene/Silicon Schottky Junction

As it is discussed in detail in the previous section, a single layer of graphene with atomic thickness has high transmittance of 97% which makes it transparent through the wavelength range of 300-1000nm which includes the whole visible spectrum. In addition to this transparency, graphene has super-high carrier mobility and conductivity. The combination of transparency and conductivity suggested that it may be used as a transparent conductive electrode (TCE) [9]. Furthermore, graphene's mechanical flexibility is favorable when compared to brittle TCE employed in industry, such as indium-tin-oxide (ITO). Because of the aforementioned reasons, graphene was considered a viable replacement for the ITO. Although the single-layer graphene has an order of magnitude greater sheet resistance compared to the industrial TCEs, the electrical characteristic adjustment has been demonstrated to be potential for such applications. While large-scale production of SLG was a challenge, a substantial advancement in large-area graphene synthesis and the first TCE implementation in a device was demonstrated in 2010 [9]. These advancements in science suggested that it may be used in photovoltaic applications.

In the case of a metal and a semiconductor with an appropriate potential energy barrier being brought together, a Schottky junction is formed. Due to the energy difference between the working function of the metal and the Fermi level of the semiconductor an energy barrier is formed at the metal-semiconductor (MS) interface. This barrier is known as the Schottky barrier and is referred to MS

Schottky junction. MS junction solar cells were intensively explored in the early 1970s due to their easy and low-cost manufacturing process [81]. Nevertheless, low barrier height hindered solar cell efficiency, and it is frequently stated that the Fermi level at the interface is not dependent on the work function of the metal, limiting the controllability of the Schottky barrier [82]. The energy band diagram of a Schottky junction is presented in Figure 3.10.

Improved efficiency was achieved by inserting a thin (less than 3nm) oxide layer at the metal/semiconductor interface that acts as an insulator, which is known as an MIS junction [83]. According to scientific reports, a thin oxide layer generates an inversion layer at the interface, resulting in the first generation of so-called metal-insulator-semiconductor inversion layer semiconductors (MIS-IL) [84]. A diffused emitter and excellent surface passivation processes resulted in a 20% efficiency increase [85].

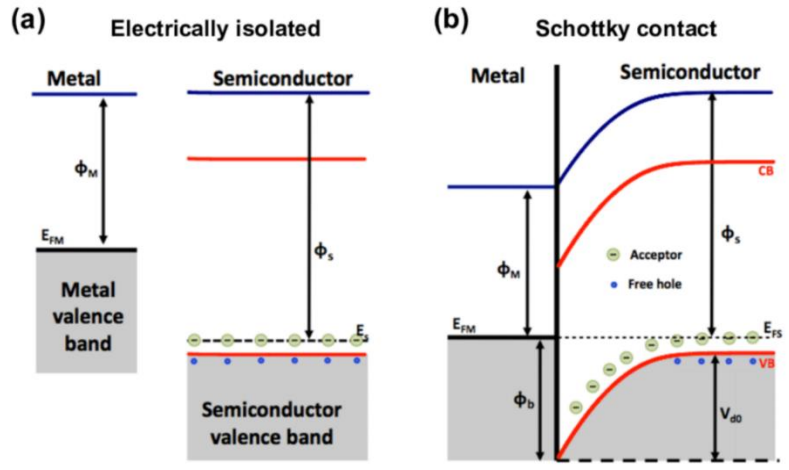

Figure 3.10. Schottky junction band structure for a metal/p-type semiconductor at a) electrically isolated and b) thermal equilibrium conditions [84].

MIS-IL solar cells were attractive because of their inexpensive production costs, but their V_{oc} was limited by the Schottky barrier height. Because of this, the total efficiency of the device was much lower than that of p-n junction devices. The cost of a p-n junction solar cell has dropped dramatically due to improvements in the

manufacturing process, and as a result, photovoltaic research has largely focused on p-n junctions.

3.5.1 Gr/Si Schottky Junction Solar Cells

A zero-bandgap feature of graphene due to the overlapped conduction and valance band and also its high conductivity, suggests that it can be regarded as a metal. In this scenario, a Schottky junction is formed when graphene is incorporated with a semiconductor. A built-in voltage (V_{in}) is generated in this situation by the difference between the graphene work function (W_{Gr}) and the semiconductor electron affinity (X_s), and this potential is used to separate the electrons and holes produced in the semiconductor as a result of photon absorption.

The Schottky barrier height (Φ_b) is determined by the electrostatic potential differences between W_{Gr} graphene and semiconductors, which are in equilibrium and is defined as;

$$\Phi_b = W_{Gr} - X_S \tag{3-7}$$

Higher W_{Gr} would offer a higher barrier since X_S is constant. Since the junction must be functioning at equilibrium, a built-in voltage (Vin) is created as a result of the Φ_b effect on the band which is known as band bending. It is possible to express the correlation between the b and Vin as follows [86]:

$$\Phi_b = V_{in} + e^{-1} n k_b T ln(\frac{N_C}{N_D}) \tag{3-8}$$

Where, N_C is the density of states in the conduction band and N_D is the doping concentration of the semiconductor. Accordingly, there is a linear relation between V_{in} and Φ_b since the second part in equation (3-8) is constant.

The current density will be a function of Φ_b as [87],

$$J = J_s\left[\left(exp\frac{eV}{nk_bT}\right) - 1\right] \tag{3-9}$$

Where the saturation current J_s is defined:

$$J_s = A^*T^2 exp\frac{\Phi_b}{k_bT} \tag{3-10}$$

where, A^* as the effective Richardson's constant, n is the diode ideality factor, k_b is the Boltzmann constant, and T is the temperature.

Figure 3.11 presents the reported Gr/Si solar cell performances and the relation between the V_{oc} value and the Schottky barrier Φ_b. Accordingly, they are linearly proportional and higher Φ_b results in higher V_{oc} and improved efficiency. However various parameters such as surface recombination, bulk lifetime, current density, and series resistance affect V_{oc} as well.

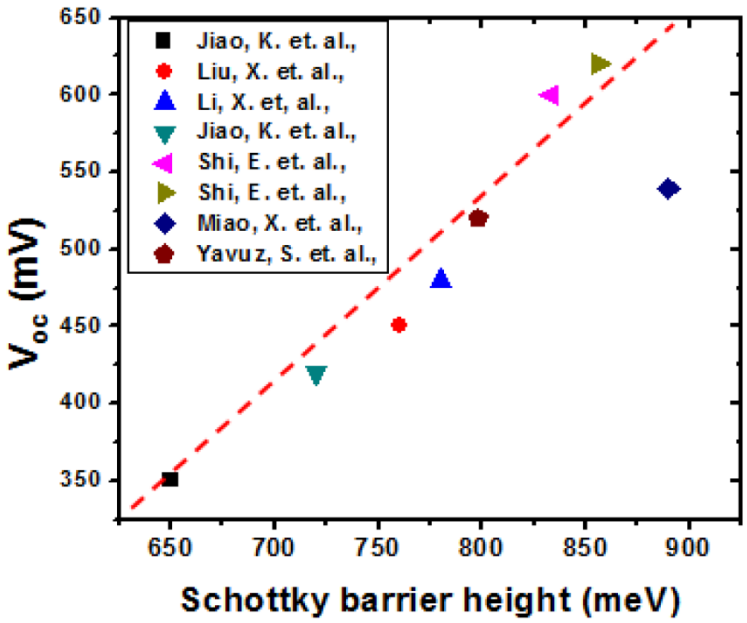

Figure 3.11. Relation between the V_{oc} and Schottky barrier height (Φ_b) for Graphene/n-Si Schottky solar cells. A linear dependence shows that a higher Φ_b leads to a higher V_{oc} [9], [86], [88]–[91].

3.5.2 Gr/Si Schottky Junction for Photodetection

As mentioned, in conventional Schottky photodiodes, spectrum response is restricted to the bandgap of the semiconductor used. The metal side is passive and it was simply used to carry the charge and acts as an electrode. Although, when highly reactive metal layers such as Au and Al are used in conventional systems, the responsiveness is restricted because less light can pass through to the semiconductor. As a transparent electrode in Schottky photodiodes, graphene is a suitable material because of its high optical transparency (> 97%) and high carrier mobility as mentioned. Furthermore, unlike traditional photodetectors, graphene/semiconductor photodetectors have multiple working regimes, which means that both the semiconductor and graphene act as light absorbers for separate wavelength ranges. The related Gr/Si Schottky junction is presented in Figure 3.12. the photons with energy higher than the bandgap of the semiconductor, are absorbed by the semiconductor side. The electron-hole pairs generated in the depletion region due to the photon absorption are separated by built-in voltage. On the other hand photons with energy $\Phi_B < h\upsilon < E_g$ are absorbed in the graphene side and the photogenerated e-h pair in graphene gain sufficient energy to overcome the barrier and flow to the semiconductor. The schematic of the processes is presented in Figure 3.12.

Graphene's excellent optical transparency makes it possible to achieve high responsivities in the wavelength range where photon energy is greater than the semiconductor bandgap. In addition, graphene-semiconductor photodiodes have a spectral range that is larger than the semiconductor's bandgap. Graphene's broad absorption range makes it possible to detect radiation with energy below the semiconductor's bandgap. Planar junctions of graphene with group-IV semiconductors like Si have been shown to function as photodetectors across a wide range of wavelengths [92], [93] and Ge [94] as well as compound semiconductors like InSb [95], GaN [96], and GaAs [97]. It is crucial to building high-performance, cost-effective CMOS-compatible broadband photodetectors, and the Gr-Si junction platform is ideally suited for this purpose [98], [99].

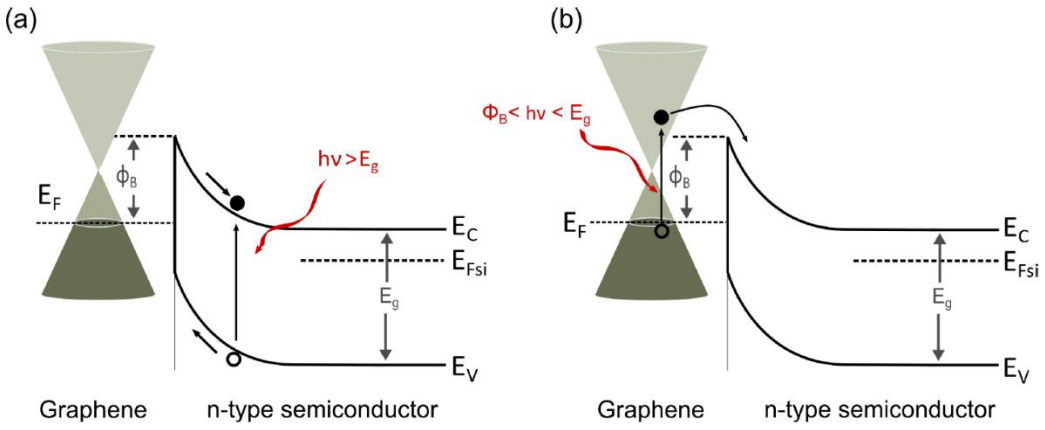

Figure 3.12. Operation modes and band structure in Gr/Si photodiodes. a) photons with energies higher than the bandgap E_g are absorbed in the semiconductor. b) photons of energies $\Phi_B < h\upsilon < E_g$ are absorbed in graphene.

CHAPTER 4

SILICON SURFACE TEXTURING FOR LIGHT MANAGEMENT

One of the main strategies to enhance the efficiency of silicon-based solar cells is reducing the reflection loss of the silicon as much as possible to maximize the absorption of the material. This idea is the origin of the production of "Black Silicon" which has a reflection of less than 5%. The surface of the black silicon is textured in form of nanostructures which makes it applicable to thin films. Note that, thin films are preferred for solar cell applications due to their less material consumption and as a result reduced feedstock cost. On the other hand, the high aspect ratio of these structures results in higher defect density at the surface which results in higher majority carrier recombination. In this chapter three different methods of Metal-assisted chemical etching, femtosecond laser-induced periodic surface structuring, and photochemical etching methods are discussed and used to texture the silicon surface with nanostructures. The aim is to compare the performance of the different structures and catch a trade-off between the electrical properties and optical properties of the surfaces.

4.1 Light Trapping for Silicon-based Solar Cells

To enhance the conversion efficiency of the photovoltaics, the reflection should be decreased to near zero values across a wide spectral and angular range. Increasing the optical path of the incident light inside the semiconductor, known as "light trapping", is introduced as a solution to overcome the high absorption and short diffusion length limits of silicon [100], [101]. Increasing the optical path of absorbed photons is possible by surface texturing which results in numerous light reflections. With proper surface texturing by random pyramids, it is possible to catch multiple reflections and at each reflection, nearly 33% of the incident light is absorbed. The

typical wet chemical etching method is the well-known method for surface texturing of silicon solar cells [102], [103].

The 'Yablonovitch Limit' for semiconductor sheets which indicates the intensity enhancement factor limit was first calculated by Eli Yablonovitch and George D. Cody [104]. The limit was determined as '$4n^2$' where n is the semiconductor's refractive index. The enhancement is close to 50 for wavelengths near the band gap, meaning that the optical performance achieved for a 200 µm thick wafer with sufficient light trapping will be comparable with the optical performance of a 10mm slab of silicon without light trapping. The schematics illustrated in Figure 4.1, determine how surface structuring causes light trapping. Pyramidal structures are dispersed randomly throughout the silicon surface as a result of chemical etching processes. This depends on one crystallographic plane being etched more thoroughly than others.

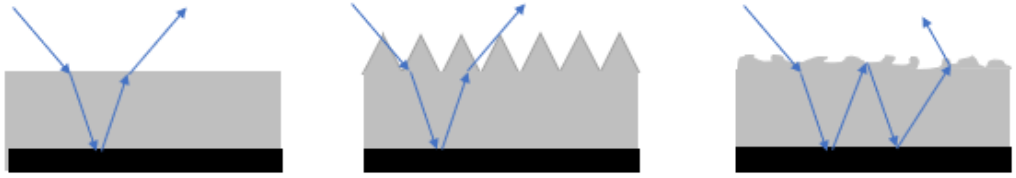

Figure 4.1. Effect of surface texture on the optical path of the incident photon for a) flat surface, b) pyramid textured surface, and c) isotropically etched surface.

Antireflection coating (ARC) can be used to decrease the reflection of silicon in addition to surface texturing. Silicon nitride (SiN_x) and titanium dioxide are the well-known antireflection coatings used for silicon solar cells. By using both random pyramids in micro range dimension as a surface texturing and ARC the reflection of silicon decreases to 5-10%. Although reaching 2% reflectance is feasible [105], [106].

On the other hand, these techniques are not compatible with new-generation silicon solar cells such as thin-film silicon solar cells or multi-crystalline silicon solar cells. Due to the less material consumption, thin-film silicon solar cells with a thickness

less than 100 μm are preferred for solar cell technology however the micro range height of the random pyramids are very high for these films. The orientation selective etching method is also not appropriate in the case of widely used multi-crystalline wafers which consist of grains with different orientations. All these factors together made it necessary to look for an alternative to random pyramids. Recently structures such as porous silicon wafers, nanoholes, nanowires, nanocones, thin films covered with nanoparticles and plasmonics, nanopyramids etched by laser, etc. are introduced as alternatives [107]–[110].

Although, the majority carrier recombination rate increases in the case of silicon surface textured in form of nanostructures due to the high aspect ratio of the structures and accordingly increase in the intensity of the surface defects. As a result, it is crucial to optimize the nanostructures and the texturing processes to obtain nanostructures with lower defect density in the vicinity of the surface.

In this thesis, the direct laser texturing method by utilizing a femtosecond laser named laser-induced periodic surface structuring (LIPSS) and the laser-assisted wet chemical etching method named photochemical etching (PCE) are used to texture the silicon surface for solar cell application. Both of the methods are laser-based etching methods. Since the most important problem in nanostructures is the weak electrical properties and low carrier lifetime, it is aimed to prevent electrical losses as much as possible while increasing the absorption and improving the optical properties of the solar cell. Well-established MACE method is also used to etch the silicon surface and produce black silicon for comparing the results. In this study, fully and partially textured c-Si surfaces by MACE, LIPSS, and PCE are achieved and studied in detail.

4.2 Chemical Texturing

Multiple light-trapping structures and anti-reflective coatings have been developed to improve absorption. This section goes through some of the most used methods for surface texturing.

4.2.1 Mono-c Silicon Texturing

Alkaline etching is frequently used to texturize mono-c silicon. The anisotropic etching capability of KOH along the (100) and (111) crystallographic planes is utilized in this procedure. With the reaction below, the etch rate of KOH for the (100) plane can be up to 600 times higher than that for the (111) direction [111].

$$Si+2KOH+H_2O \rightarrow K_2SiO_3+H_2 \quad (4\text{-}1)$$

The schematic of the reaction and the achieved micro-pyramid structures with (111) oriented planes is shown in Figure 4.2. Figure 4.3 illustrates the SEM image of the random pyramids achieved by the alkaline etching method.

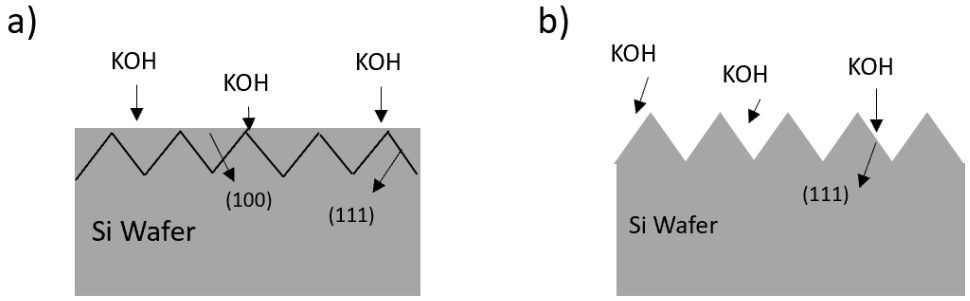

Figure 4.2. a) Flat (100) oriented wafer is placed in KOH solution, (b) pyramids with (111) orientation faces are formed after the chemical reaction takes place.

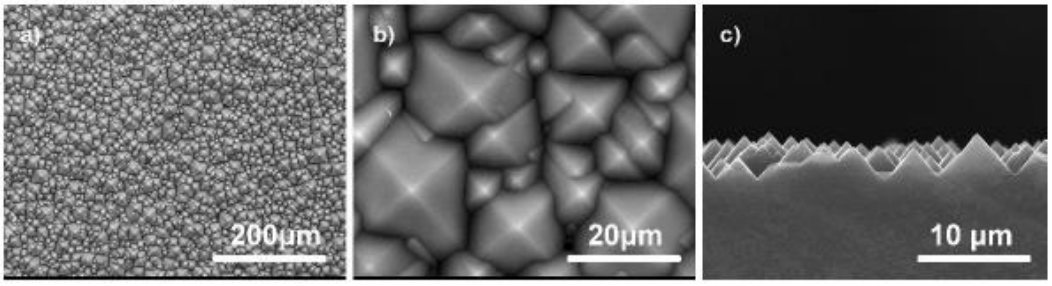

Figure 4.3. SEM image of Si random pyramids formed by an alkaline etching process with different magnifications a), b) top view, and c) side view [112].

4.2.2 Multi-c Silicon Texturing

Anisotropic alkaline texturing is not suitable for multi-c silicon because its surface contains several grains with various crystal orientations. Instead, random roughness is created on the surface using isotropic stain etching solutions containing HF, HNO_3, and H_2O_2 [111]. During this procedure, Si is oxidized with HNO_3 and then SiO_2 is etched with HF.

$$Si+HNO_3+6HF \rightarrow H_2SiF_6+HNO_3H_2O+H_2 \quad (4\text{-}2)$$

Figure 4.4 refers to the SEM image of the isotropic surface texturing of the multi-crystalline silicon [108].

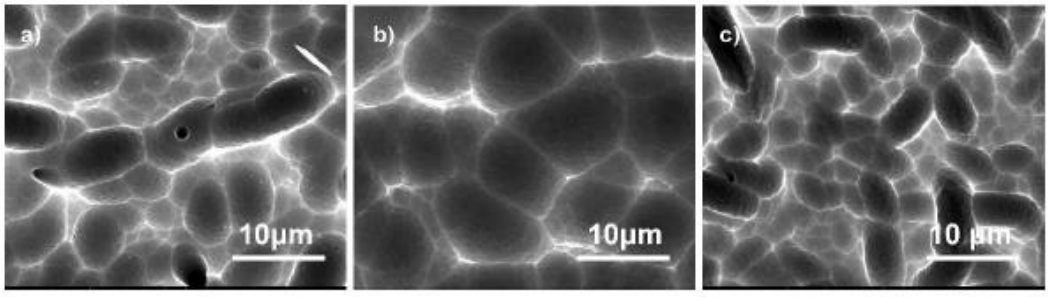

Figure 4.4. SEM images of isotropic surface texturing of the different multi-crystalline silicon [111].

4.2.3 Other Texturing Methods

For texturing of c-Si wafers, new methodologies have also been developed in addition to the earlier conventional methods. The following are the key justifications for the need for different texturing methods.

1) *Improving the optical performance:*

Although the surface texturing for mono and multi-c silicon is technically feasible using the prior techniques, in both instances an anti-reflective coating is required to enhance the optical qualities of the surface. Although PECVD-grown SiN is typically

employed as an ARC, new ideas have been presented such as the formation of nanostructures on the silicon surface with reflectance decreased to 2% [113]–[115]. An increase in short circuit current density and conversion efficiency follow a decrease in reflection. These cells are referred to as "Black Silicon" solar cells since they essentially have near-zero surface reflection [116]–[118]. However, the fundamental disadvantage of nanotextured solar cells is significant surface recombination due to the increased surface area. For black silicon solar cells, improved passivation techniques result in an efficiency of 22.1% [119], [120].

2) Applicability to thin wafers:

Random pyramids formed by the alkaline etching method are not suitable for thin-film silicon solar cells for mechanical reasons. The thickness of the thin-film crystalline solar cells is less than 100 μm which is close to the height of the random pyramids. Although material loss is more for micro dimension features compared to nanostructures. Also, the reflectance for nano-structures is very low. As a result, the need for nano texturing rises, and new fabrication methods are reported. Some of the well-known methods for achieving nano-structures are the bottom-up method of Vapor-Liquid-Solid (VLS) Growth, and top-down processes of Reactive Ion Etching (RIE), photolithography, Nano-sphere Array Lithography, laser texturing and Metal-assisted chemical etching (MACE) [113]–[115]

3) Crystallographic orientation independence:

Despite the mono-crystalline silicon which has constant surface orientation, multi-crystalline silicon surface consists of grains with different orientations. Accordingly, the orientation-selective etching method is not suitable for multi-c silicon. Novel methods such as laser texturing, dry etching, and plasma texturing are preferred for surface texturing of multi-c silicon wafers which are widely used for solar cell applications [112], [121].

4.3 Metal-assisted Chemical Etching (MACE)

MACE is a promising technique among the various fabrication techniques that can be applied to different types of silicon solar cells. It is a simple, highly adaptable method for fabricating different Si structures with sizes varying from nano to micro dimension. Since the wet chemical process of MACE is a top-down approach it is possible to control the features of the nanostructures such as the crystal direction, size, and doping. Also, it allows controlling the etching process by changing the parameters which result in the formation of different structures such as nano-holes, nano-wires, or nano-cones. The combination of the MACE process with other techniques such as photolithography is also possible to achieve different surface features [122]–[124].

MACE was first reported by Li et. al. [125] in 2000 as an electroless wet chemical etching technique for the formation of porous silicon and porous III–V compound semiconductors. this process consists of metal particles and a proper oxidant medium which is an acidic solution that contains an oxidant like as hydrogen peroxide (H_2O_2) and an etchant such as hydrofluoric acid (HF). Generally in the MACE process, noble metal particles start the reduction reaction at the surface and as a result the local oxidation. Holes (h^+) are injected into the Si substrate or electrons (e^-) are transported from the Si substrate to the metal catalyst. As the concentration of holes is highest in the Si surface under the metal catalyst, which is also where the Si is most readily oxidized. The oxidized silicon is then etched by the etchant in the solution. The parameters such as solution ratio, etching time, and metal nanoparticle size, control the morphology of the achieved structures. Silver, gold, platinum, copper, and nickel are noble metals that can be used as a catalyst for MACE [126]–[130]. Metals can be used in form of salts, nano-particles, or deposited layers. Figure 4.5 shows the MACE process utilizing Ag metal as a catalyst.

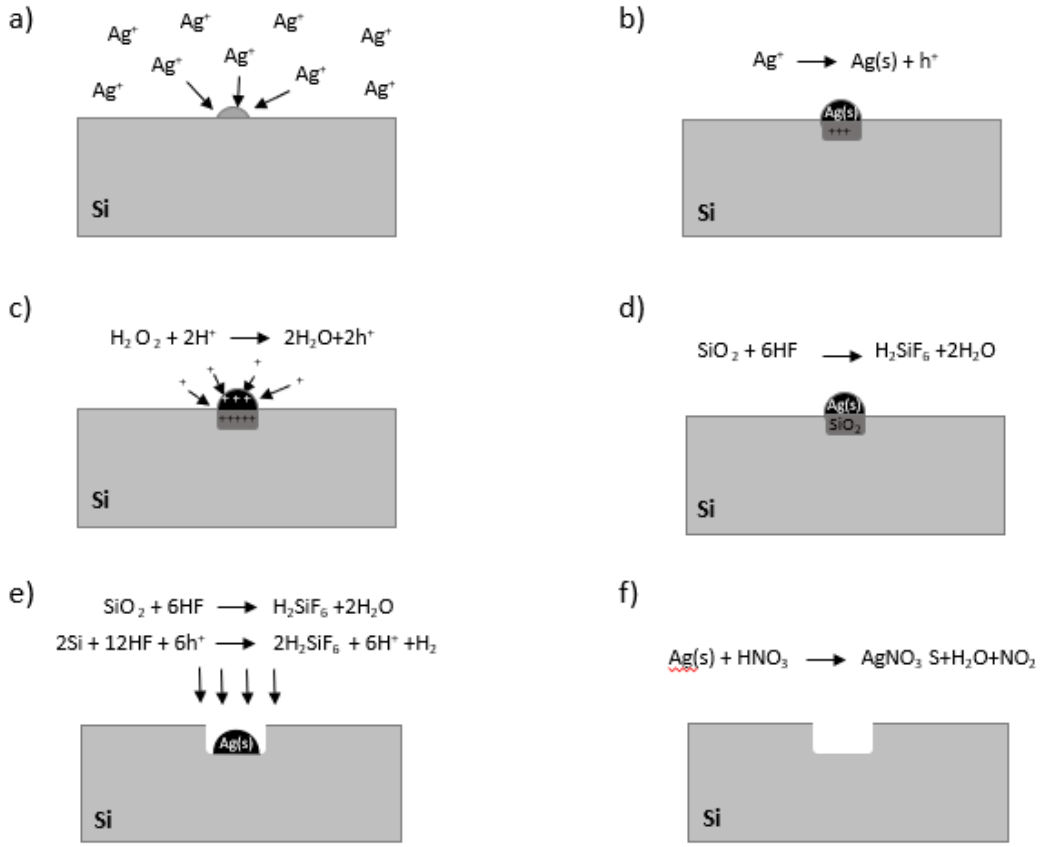

Figure 4.5. Schematic illustrating the process step for metal-assisted chemical etching using silver as a metal. a) Silicon wafer is placed inside the solution. b) Ag donates a hole to the silicon and Ag nanoparticle nucleation starts on the silicon surface. c) additional hole injection to silicon due to H_2O_2 reduction. d) Si beneath the metal is oxidized, e) HF attacks the oxidized silicon and etches the SiO_2 formed under the Ag nanoparticle f) metal residuals are removed and etching is completed.

In this thesis, two different methods were optimized for the Metal-assisted chemical etching process. The first method was the standard MACE process utilizing a metal salt. Firstly, Czochralski-grown, mono-crystalline n-type Si wafers with (100) orientation, 250 μm thickness, and 1-1.3 Ω-cm resistivity is used. Standard RCA1 and RCA2 cleaning processes are applied to remove the organic and metallic contaminations, respectively. After the cleaning process by RCA1 and RCA2 an oxide layer with a thickness of 1-2 μm forms as a by-product. The oxide layer is then

removed by dipping the wafer in a dilute HF: HCl. The next step is the formation of the metal nanoparticles which will assist the etching process. For this purpose, the preferred noble metal and the related salt are silver and $AgNO_3$. A solution of 0.14 M HF: 0.005 M $AgNO_3$ is used for the MACE process. For a metalization time of 5 min, the solution results in the creation of Ag nanoparticles (AgNPs) with a diameter of 60-80 nm with a surface coverage of about 40-50 %. For the etching process, a solution of HF-H_2O_2-H_2O was used. Finally, the etched sample is immersed in a concentrated HNO_3 solution to remove the silver dendrites. The etch rate of this process depends on the solution ratio of the etching step and is defined as ρ [131].

$$\rho = \frac{HF}{HF + H_2O_2} \tag{4-3}$$

Chartier et al. [131] Revealed that the ρ ratio affects the morphology of the etched silicon and the formation of the structures. They applied a NaOH treatment step after the etching process to dissolve a porous silicon layer and reported the resulting morphology of the etched silicon in Figure 4.6.

In this thesis, a solution of 30 ml HF: 5 ml H_2O_2: 100 ml H_2O, is used for the etching process. The depth of the structures etched in different etching times is presented in Figure 4.7. According to the results, the etching ratio for this solution is 1 $\mu m.min^{-1}$. The achieved plot indicates that the etching ratio is not perfectly linearly dependent on time, and the etching rate decreases as the etching time increases which is due to the reduction in the amount of the fluoride HF and H_2O_2 in the solution.

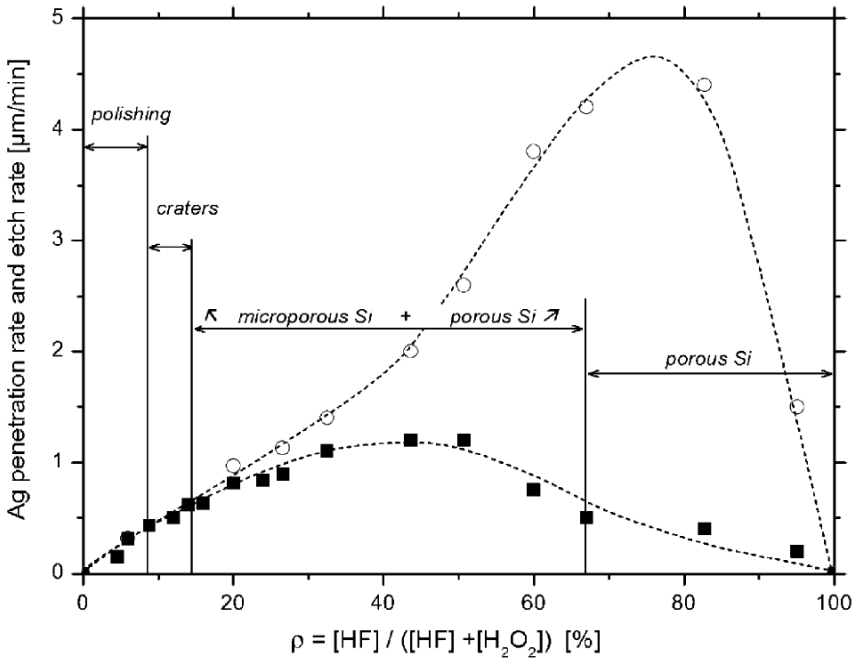

Figure 4.6. The etch ratio and surface structures with respect to the ρ ratio before a NaOH treatment (unfilled cycles) and after a NaOH treatment (filled cycles) [131].

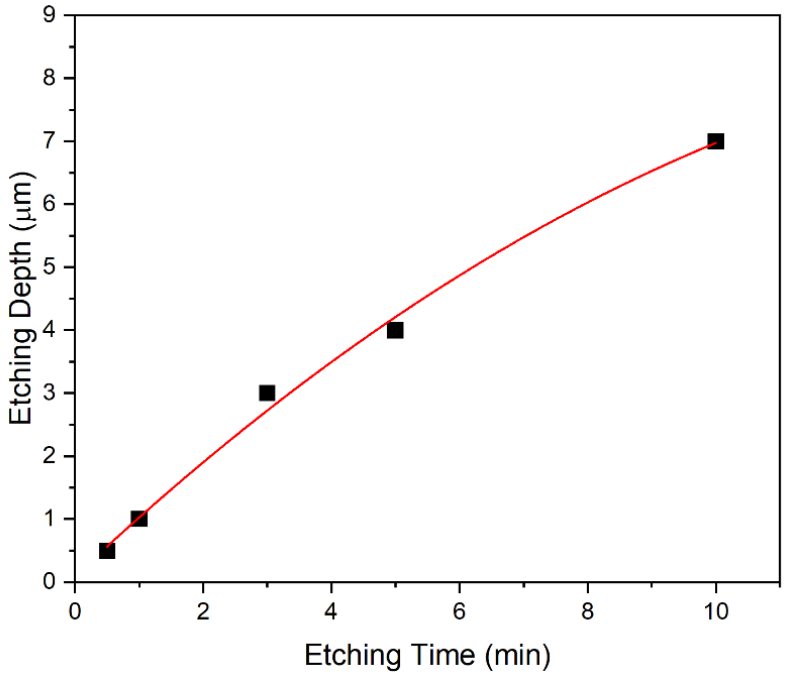

Figure 4.7. Etching depth as a function of etching time deduced from SEM images.

The SEM image of the silicon surface etched by using $AgNO_3$ salt for metallization which assists the etching process is presented in Figure 4.8. The top view and side view images are provided for the structures. Note that, the structures with a length of 1µm are achieved for 1-minute etching.

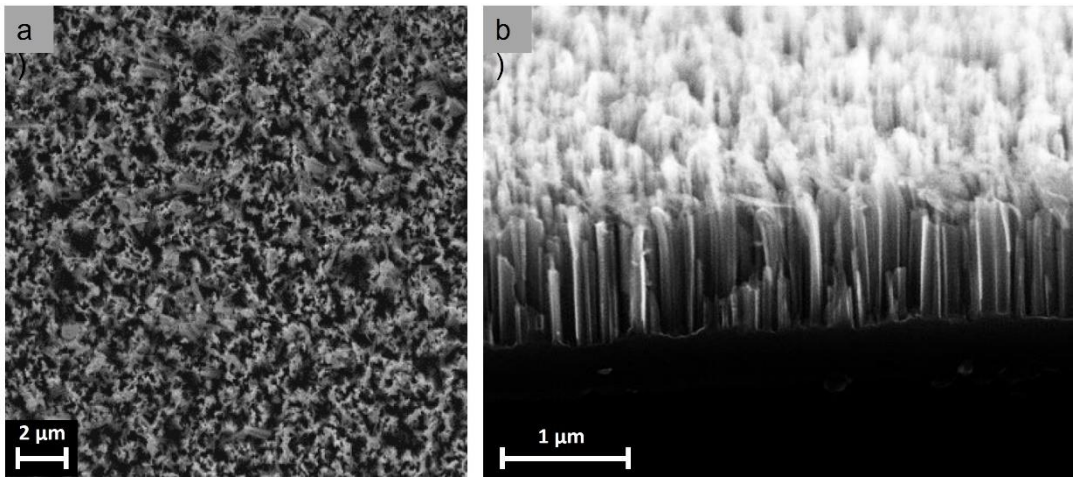

Figure 4.8. SEM images for a) top view and b) side view of silicon nanowires achieved by MACE process using $AgNO_3$.

Although this method is very easy, fast, and low cost, it is not very easy to control the process, and selective etching is not possible. In case of the need to etch a certain percentage of the surface, it is not possible with the metal salt-based MACE process. Another alternative to solve the problem is depositing Ag thin film physically instead of using chemicals. The difference is that AgNPs are formed mechanically instead of forming by chemical reactions in solutions. The thermal evaporation deposition method is used to deposit a thin metal film. An annealing step after the deposition of a thin Ag film results in the generation of randomly localized AgNPs on the Si surface. The pattern and size of the AgNP can be altered by changing the thickness of the Ag film during evaporation and the annealing temperature[132]. Next, the Si surface covered by AgNP is immersed in the etchant solution of $HF/H_2O_2/H_2O$. And finally, the Ag residues are removed in a concentrated HNO_3 solution. In this study, an Ag film of 10 nm is deposited by thermal evaporation and annealed at 300°C for 60 min. The annealing process results in the formation of AgNPs of 80-100 nm

diameter and this process is called dewetting. The SEM image of the AgNPs produced by dewetting of 10nm Ag film is presented in Figure 4.9. The SEM image of the silicon surface and the related nanostructures after the etching process is presented in Figure 4.10.

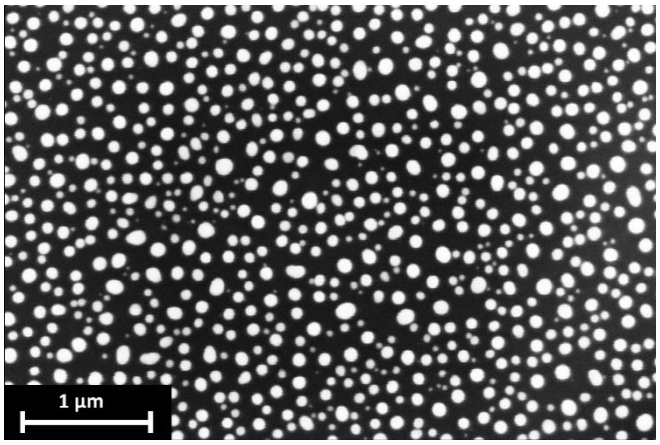

Figure 4.9. SEM image of AgNPs fabricated by dewetting a 10 nm Ag thin-film at 300°C for 60 minutes.

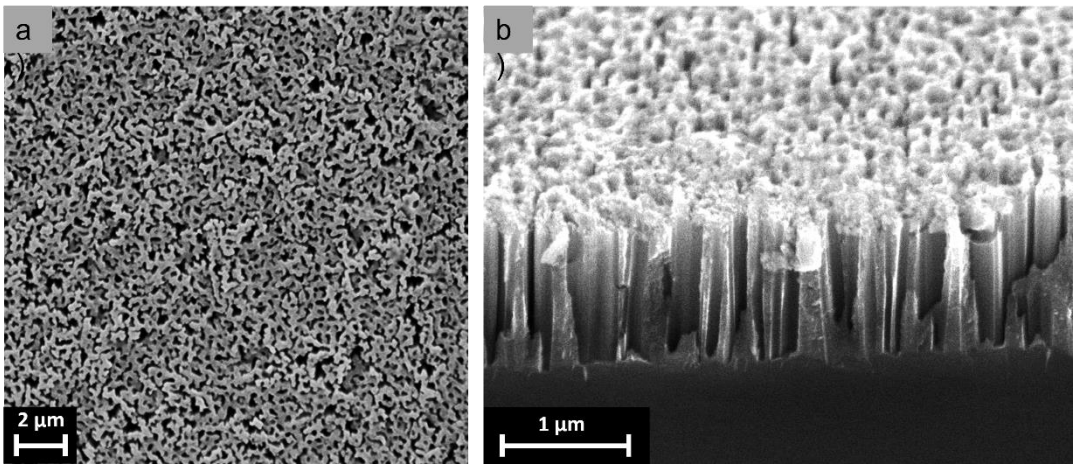

Figure 4.10. SEM images of a) top view and b) side view of silicon nanowires fabricated by MACE process using physically deposited thin film silver.

As it is obvious from the SEM images, the aspect ratio is very high for these structures, which means that there is high defect density at the vicinity of the surface and it requires high-quality passivation. On the other hand again due to the high aspect ratio, high roughness, and very small dimension of the structures, the only

passivation method which can be used for these structures is ALD [133], [134]. Accordingly, without proper passivation, the majority carrier recombination rate will be very high which results in performance degradation. The other important factor is that, for better device performance, the area beneath the electrodes should have remained untextured. To catch a trade-off between the carrier recombination rate and light trapping and also selective etching of the silicon surface, I tried to etch the silicon surface in a specific pattern. For this approach, a shadow mask was designed and cut out from a monocrystalline silicon wafer by using a laser setup. Two different patterns with 70% surface coverage were designed. The patterns were in form of 4-windows and 9-windows. The aim is to find out if the size of the textured area affects the performance of the etched sample while the overall etched surface ratio is the same. For the cutting process, EO Technics- Supermarket GF 311 nanosecond IR laser with a wavelength of 1064nm and a maximum power of 30W is used. The laser setup, the designed patterns, and the prepared shadow masks are presented in Figure 4.11. The shadow masks are aligned on silicon samples and then the wafer with a mask on it will be placed in the deposition chamber for Ag thin film deposition. Accordingly, after removing the shadow mask, the Ag film will be deposited only in the open windows. After removing the mask and dewetting the sample, AgNPs form only in specific regions. After immersing the sample into the etching solution the desired regions will be etched. Note that for both of the patterns almost 70% of the surface is etched and the only difference is the size of the etched region. The desired regions such as the region beneath the electrodes remain smooth. The SEM image of the partially etched Si wafers with two different patterns is presented in Figure 4.12

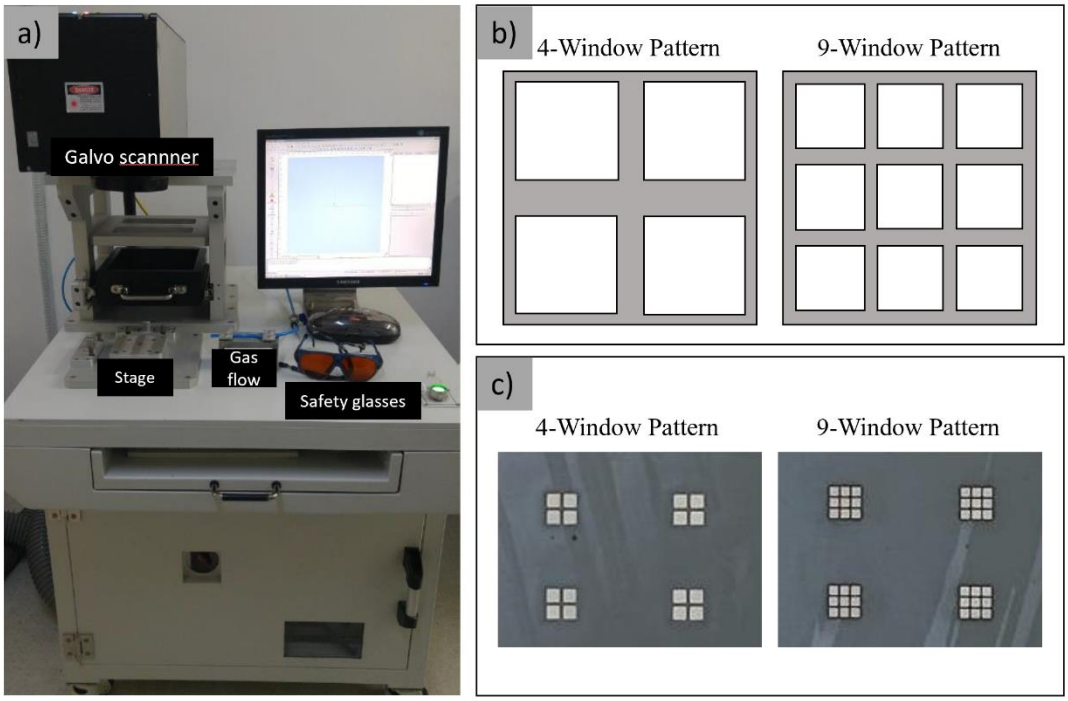

Figure 4.11. Photograph of a) nanosecond IR laser setup and b) patterns designed for shadow masks and, c) prepared shadow masks.

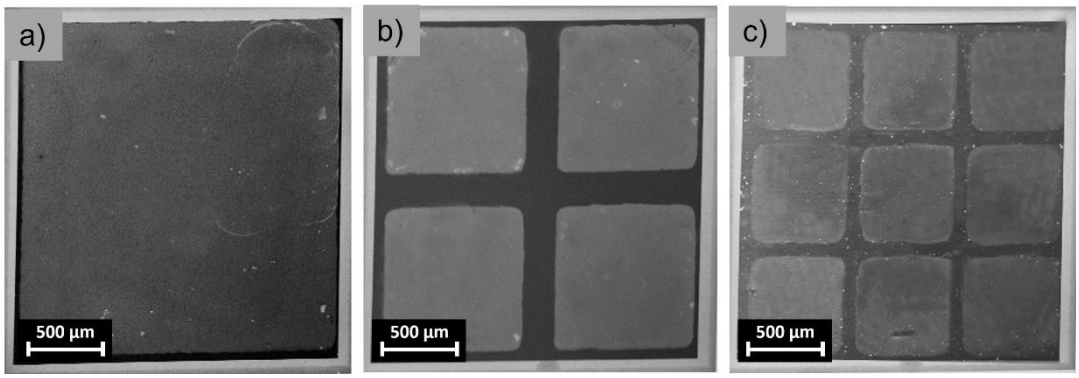

Figure 4.12. SEM image silicon surfaces a) fully etched and b,c) partially etched with 4-windows and 9-windows patterns by MACE.

For reflectance measurements, a 1cm^2 area was fully etched and partially etched (in 70% coverage) with two different patterns. The reflectance of the samples was measured by Bentham PVE300 Photovoltaic EQE (IPCE) which is presented in Figure 4.13. Reflectance, transmittance, and quantum efficiency can be measured by this setup. The reflection measurements for prepared samples are presented in Figure 4.14. For all

the reflectance measurements in this chapter, the measurement for each sample is measured from three different points on the surface and then the average value of the three measurements is calculated and reported. The reflectance in the visible range was measured as ~4% for the silicon surface fully etched by MACE which means near-zero reflectance. The reflectance values for the partially etched silicon surfaces with 9-window and 4-window patterns are increased to values of about 7% And 10% respectively, as was expected. The higher reflectance value of the 4-window pattern compared to the 9-windows pattern is probably due to the light diffraction. The etched regions close to each other with smaller flat areas in length result in more light-trapping. It approves that the reflectance values measured for the partially etched samples are close since both patterns result in etching of the 70% of the surface.

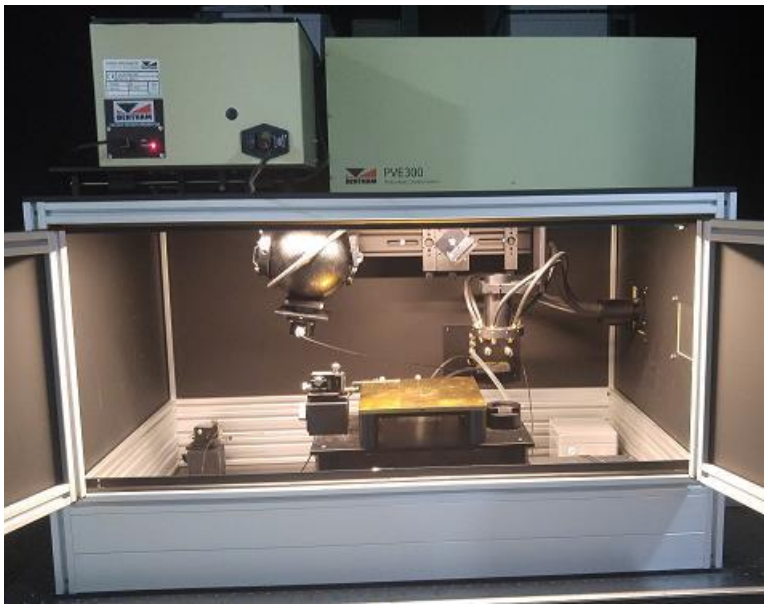

Figure 4.13. Bentham PVE300 Photovoltaic EQE (IPCE) is used for reflection/transmission measurements.

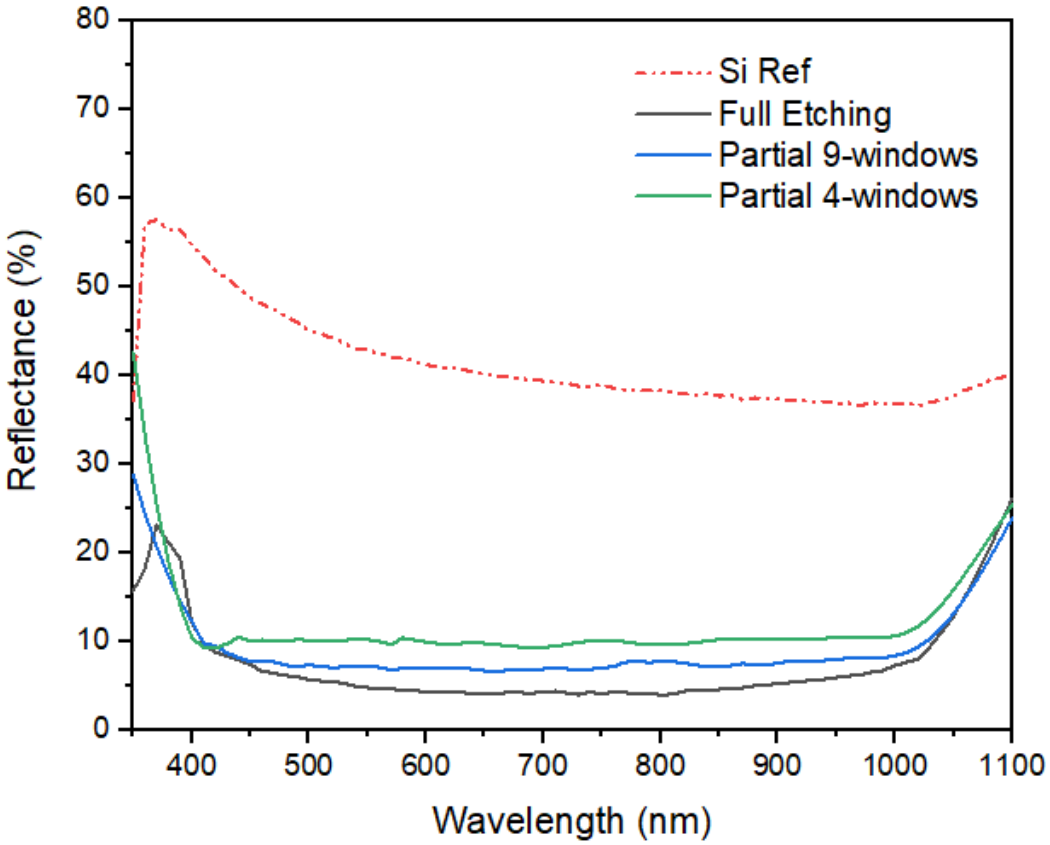

Figure 4.14. Reflectance measurement for fully and partially etched silicon surfaces by MACE method.

In addition to recombination due to the high aspect ratio of the structures, the other important reason for the high recombination rate of these structures is the fact that it is not easy to get rid of metallic contaminations. Accordingly, two steps of the RCA2 cleaning process were applied as a final step to clean the metallic contamination as much as possible.

4.4 Direct Laser Texturing

Direct laser texturing is a non-contact process introduced by Zolper et al. [135] for silicon surface texturing. This method is based on laser ablation and it was already used for some solar cell processes like dielectric layer ablation, edge isolation, and emitter formation. The laser-textured, buried contact polycrystalline silicon solar cell

reported by Zolper had an enhanced efficiency of 16.7%. Later, its application for surface texturing of silicon solar cells was studied by Zielke et al [136] and high efficiency of up to 19.3% was reported [136]. Figure 4.15 shows the SEM image of the silicon surface textured by nanosecond Nd: YVO_4 laser with a 355 nm wavelength by Zielke et al [136]. They reported PERC silicon solar cells with a multi-crystalline silicon surface textured with laser and enhanced efficiency up to 17.9%. They also reported an FZ-grown monocrystalline PERC solar cell with an enhanced efficiency of 19.9 %. The J_{sc} and V_{oc} values for monocrystalline solar cells were reported as 40.6 $mA.cm^{-2}$ and 0.665 V, respectively.

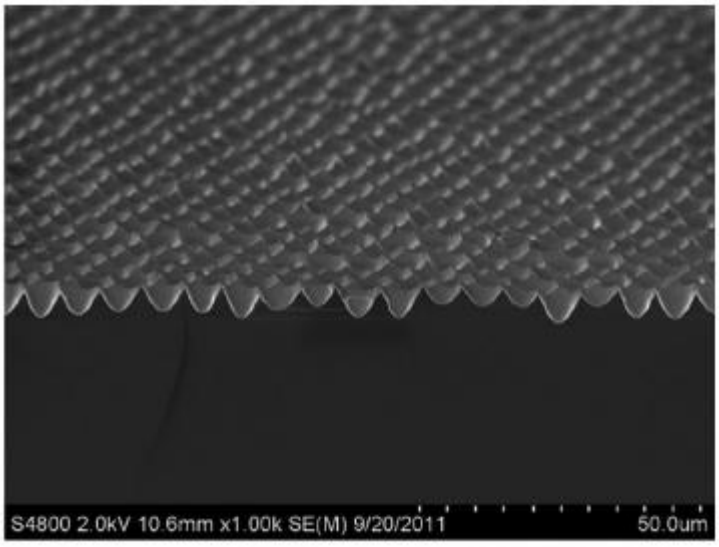

Figure 4.15. SEM image of the final structure reported by nanosecond Nd: YVO_4 laser with a 355 nm wavelength [136].

Later, the Mazur research group reported another direct laser etching method using a femtosecond laser pulse in a chamber that contains SF_6 gas inside. As a product of the process, nano-cones formed on the silicon surface and a type of black silicon with a reflection of less than 5% was achieved [137], [138].

Laser-induced periodic surface structuring (LIPSS) was first introduced by Birnbaum in 1965 [139]. LIPSS is the name of phenomena that can be seen on the material surface after they are irradiated by linearly polarized laser beams with

ultrashort laser pulses with a duration from picosecond to femtosecond. It is a simple, quick, and cost-effective etching technique compared to other well-known lithography methods such as photolithography, electron beam lithography, and nanoimprint lithography. Various parameters such as the irradiation wavelength, the polarization direction of the beam, the number of pulses on the spot, repetition rate, the fluence of the ultrafast laser, and the scanning speed control the formation of the nano-ripples on semiconductors [14] [140] [141]. The LIPSS nanostructures can be used as surfaces for cell growth, antibacterial surfaces, and SERS substrates [14] [142]. Recently silicon surfaces structured by LIPSS were used for p-n junction c-Si solar cell fabrication which resulted in an efficiency of more than 16% [143]. Oz Orhan et al [144] reported Gr/p-Si Schottky diodes with silicon surface textured by LIPSS and the vertically oriented 3D graphene nanosheets deposited by Radio-Frequency Plasma Enhanced Chemical Vapor Deposition (RF-PECVD) technique on the silicon surface.

In this thesis, a 1030 nm femtosecond laser with an average power of 1100 mW on the sample surface, a scan speed of 2 m/s, and a beam size of 15-16 μm is used. The setup is presented in Figure 4.16. The aim of this method is the formation of periodic nano-pyramids on the silicon surface with fs-laser radiation. the SEM image of the etched silicon in form of nano pyramids is presented in Figure 4.17. The depth of the nanostructures is about 200nm. For the partial etching process by direct laser texturing, there is no need for any shadow mask. It is possible to etch the surface in a specific pattern directly by controlling the stage and laser presented in Figure 4.16. b. The SEM image of the samples with the partially etched surface (70% of surface coverage) with different etched region dimensions which are the same as the patterns used for the MACE process are presented in Figure 4.18.

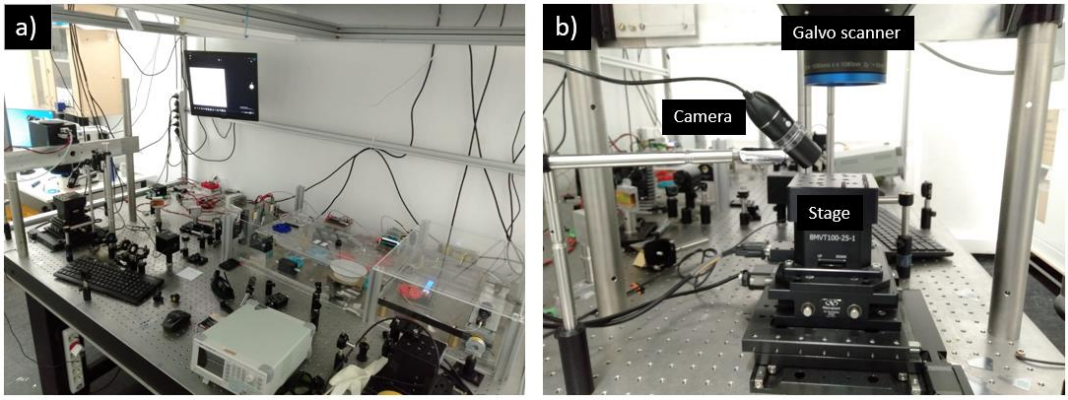

Figure 4.16. The photograph of a) fs-laser setup and b) the galvo scanner, stage, and camera used for the LIPSS process.

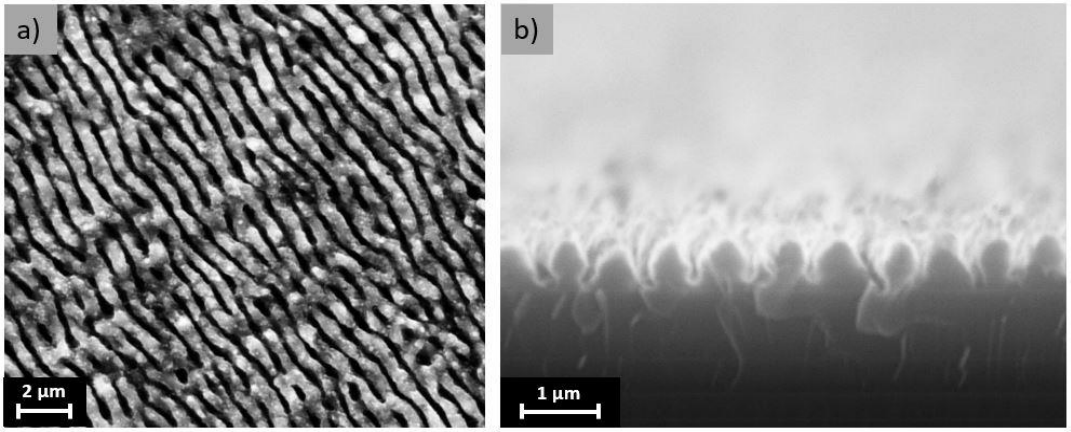

Figure 4.17. SEM images of a) top view and b) side view of arrays of nanostructures formed by LIPSS.

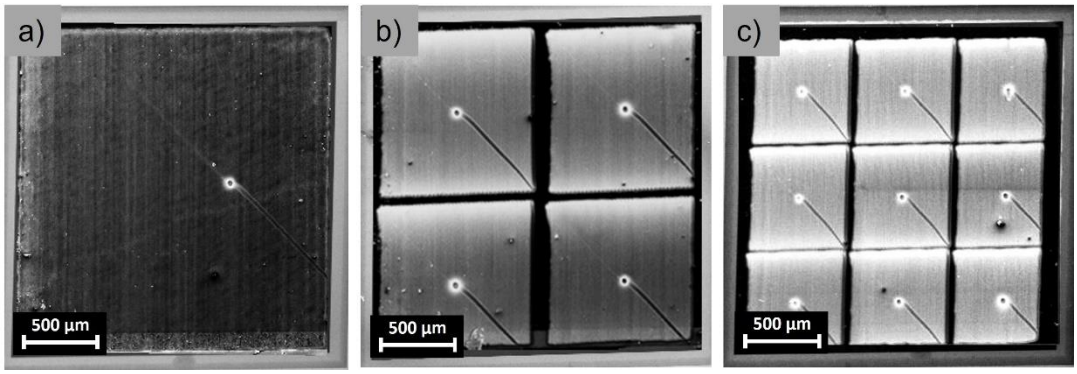

Figure 4.18. SEM image of silicon surfaces a) fully etched and b,c) partially etched in 4-windows and 9- windows patterns by LIPSS.

The reflectance measurement for fully and partially etched silicon surfaces by the LIPSS method in two different patterns of 4 windows and 9 windows are presented in Figure 4.19. Same to the reflectance measurements for the silicon surfaces etched by MACE, the reflectance values reported in Figure 4.19 are the average value of the three different measurements for each sample. The reflectance for the fully etched silicon surface by LIPSS is reported about 11-12% for the visible range. The reflectance increased to values of 14% and 16% for silicon surfaces etched with 9-windows and 4-windows patterns. According to the reflectance plots, there is not a significant difference between the reflectance measured for partially etched samples in the 4-windows and 9-windows pattern since both patterns result in etching of the almost 70% of the surface.

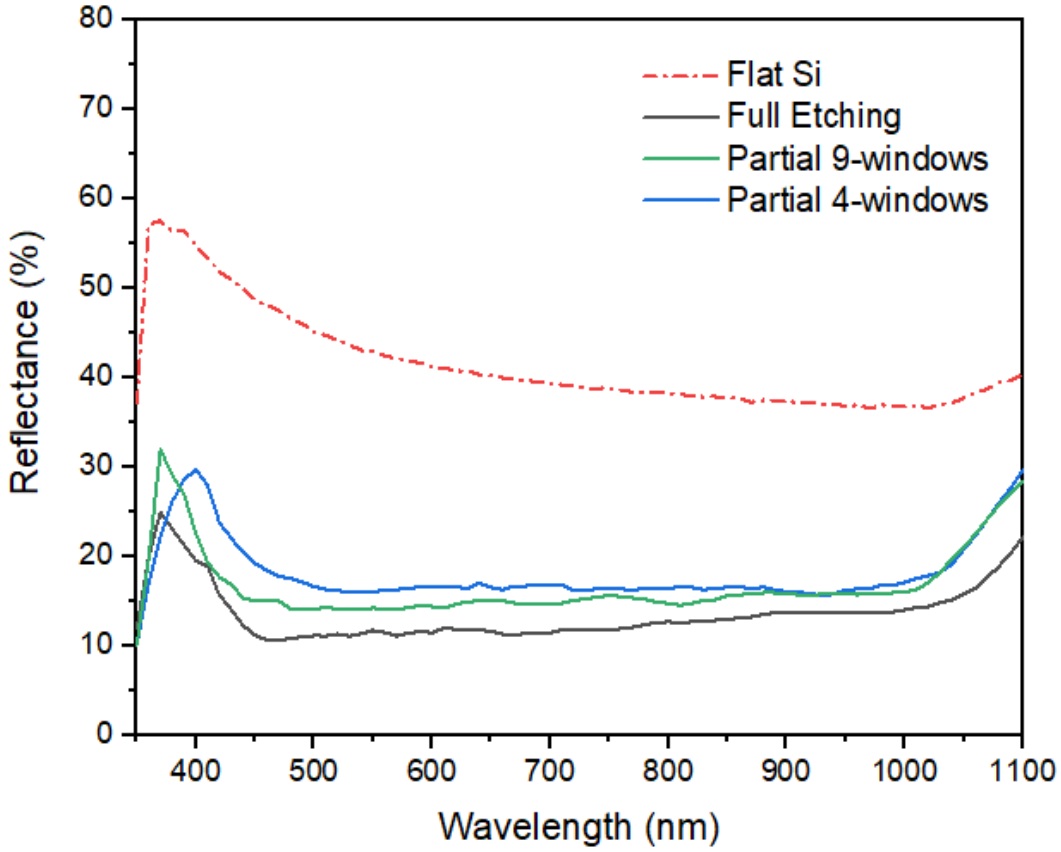

Figure 4.19. Reflectance measurement for silicon surface fully and partially etched by LIPSS method.

4.5 Photochemical Etching (PCE)

Laser-assisted wet chemical etching method called “Photochemical Etching” is another laser-based texturing method. Photochemical etching is a wet process that happens inside an acidic solution and laser illumination. Despite the photoelectrochemical etching (PEC-etching) method which is a controlled photocorrosion performed under anodic polarization in an electrolyte, there is no need for any applied voltage in the photochemical method. Charge transfer and exchange between the Si and the solution initiates the etching process. The porous silicon achieved by photochemical etching of silicon in HF solution was first introduced by Noguchi and Suemune [145]. Lim et al. [146] achieved a textured silicon surface with etch pits by applying a laser intensity of 2500 W cm^{-2}. The reported etch pits by the research group were generally in Gaussian shape. Probst and Kohl [147] used HF^- acetonitrile instead of aqueous HF in the solution of the photochemical etching process and the achieved Gaussian shape etch pits on an n-type silicon surface.

There are lots of parameters that control the etching process such as fluoride concentration, pH, type of semiconductor, carrier density, wafer orientation, and light intensity. The common photochemical process for Por-Si formation is started by hole generation. The Si-H bound at the silicon surface is assumed as the hole acceptor. Due to the surface reaction with HF, SiF_4 or $SiHF_3$ is produced which are not stable in water. H_2SiF_6 is assumed to be the product of the terminal etch. The overall reaction can be written as [148];

$$Si + 6HF + 2h^- \rightarrow SiF_6^{2-} + H_2 + 4H^+ \qquad (4\text{-}4)$$

The essential parts of the chemical reaction can be summarized as;

(1) hole injection initiates the reaction

(2) Si reacts with fluoride species

A reduction step must also take place on the crystal if a counter electrode is not present. Both anodic and cathodic sites must be present on the sample, just as they are in the case of metal corrosion. The counter-reaction is assumed to be the Hydrogen ion reduction [148];

$$2H^+ + 2e^- \rightarrow H_2 \qquad (4\text{-}5)$$

Band bending at the Si/electrolyte interface can explain the first stages of etching on a flat silicon surface. Below the electropolishing regime, this model is used to describe laser-assisted electrochemical and photoelectrochemical etchings of Si in acidic fluoride solutions (Figure 4.20). Where the illumination is constant, the rate-determining step (RDS) in this mechanism is the fourth step, where HF attacks. Accordingly, the composition of fluoride solutions has generated much controversy and fluctuates in a very nonlinear fashion based on its components.

The solution used for PEC-etching has the general formula of fluoride+oxidant +water. Fluoride can be provided by HF or NH_4HF_2. The oxidant is HNO_3, $FeCl_3$, or $NaMnO_4$. Note that when NH_4HF_2 is used, HCl should be added to make the solution acidic. The solution ratio is a significant parameter since it controls the rate of the etching rate. The hole injection depends on the oxidant and the etching process is controlled by fluoride [149]. For example, NH_4HF_2 results in the formation of larger pores compared to the HF [148]. The SEM images illustrate the porous silicon achieved by the photoelectrochemical etching process utilizing 0.8 or 15 mW HeNe laser (633 nm) in HF and NH_4HF_2.

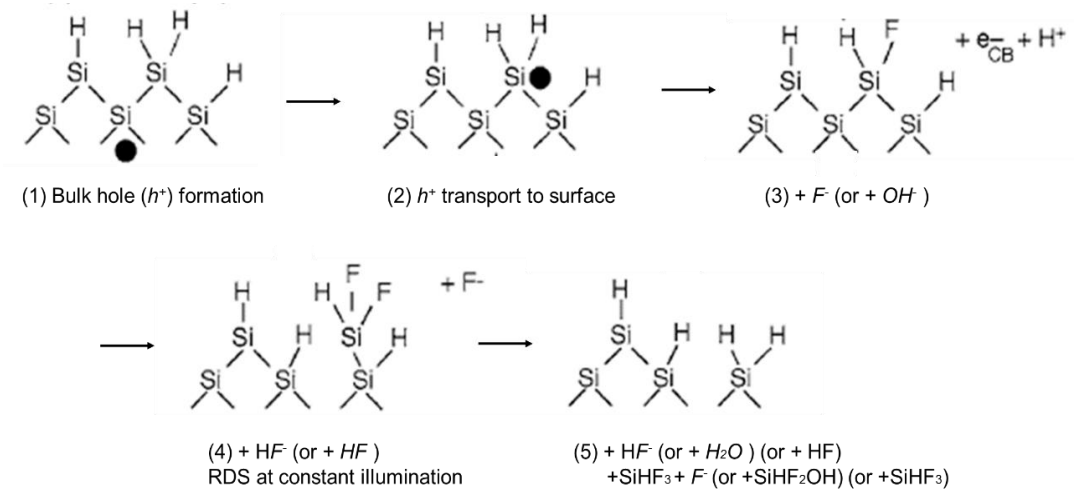

Figure 4.20. Proposed mechanism of photoelectrochemical Si etching in fluoride solutions. Alternative reactants for a given step are enclosed within brackets [148].

In this thesis photochemical etching (PCE) method is used to etch the silicon surface and form nanoholes on the surface for light-trapping purposes. The difference between PEC-etching and PCE methods is that there is no need for any electrical bias to start the etching process in the PCE method. The process is applied to achieve fully etched and partially etched silicon surfaces. The optical setup, optimization of parameters, and results are reported in detail in the following sections.

4.5.1 Optical Setup for Photochemical Etching Process

An optic setup was settled for the photochemical etching process. The overall block diagram of the setup is presented in Figure 4.21. Diode-pumped solid-state high-power CW output at 532 nm laser was used as the source. A set of silver-coated 1.00-inch mirrors and lenses are used to guide the light to Digital Micromirror Device (DMD). The output light of the DMD is modified and patterned. The modified beam is then guided toward the sample which is immersed inside an acidic solution using a set of optics.

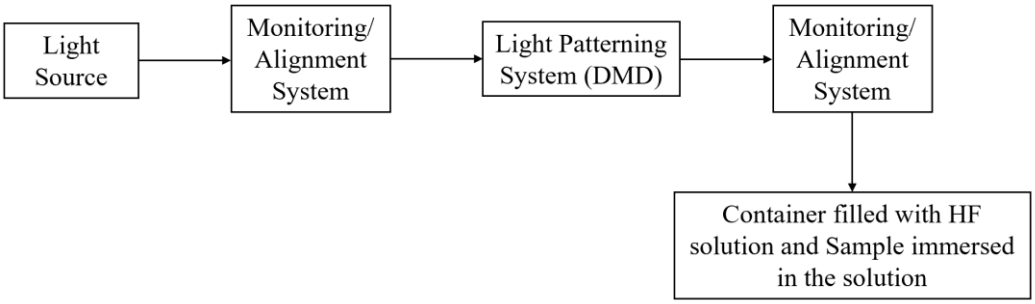

Figure 4.21. Block diagram of the optic setup.

The digital micromirror device, or DMD, is the micro-opto-electromechanical system (MOEMS) which is the main part of Texas Instruments (TI)'s patented DLP projection technology. A DMD device includes many hundred thousand micro-mirrors on its surface that are organized in a rectangular array and relates to the pixels in the displayed image. Each mirror can be turned on or off separately by a rotation of 10-12 degrees. When the projector is turned on, the lens reflects light from the bulb onto the screen, making that particular pixel look illuminated. When turned off, the pixel appears dark because the light is being redirected away from it (often onto a heatsink). The switching speed of the mirror between on and off positions determines the range of greyscales that can be generated (binary pulse-width modulation). The latest DMD chips are capable of rendering 1024 levels of grayscale (10 bits). Figure 4.22 illustrates the operation of a single micro-mirror with a 12-Degree tilt.

The rotation of the mirrors is controlled by electrostatic attraction between two sets of electrodes. By applying bias, the programmed SRAM cells rotate the mirrors making them on and off. The bias technique is utilized because it allows for the pixels to be driven directly from the SRAM cell. Although the bias voltage may be removed simultaneously for the entire chip, causing the mirrors to all shift in position at the same time. It results in more accurate timing and a more cinematic image. Accordingly, this technology has a wide application field such as 3D modeling and

design, 3D printing, high-resolution display projectors, and medical imaging systems like MRI and X-ray marking.

The DMD used for the setup in this work is DLP LightCrafter 6500. The device includes two parts, the screen part which includes the micromirrors, and the connection board which controls the micromirrors. Figure 4.22 presents the module of the DLP LightCrafter 6500 and its main parts. The micromirrors used for DLP LightCrafter 6500 are made of Aluminium and the dimension of each mirror is about 16 micrometers.

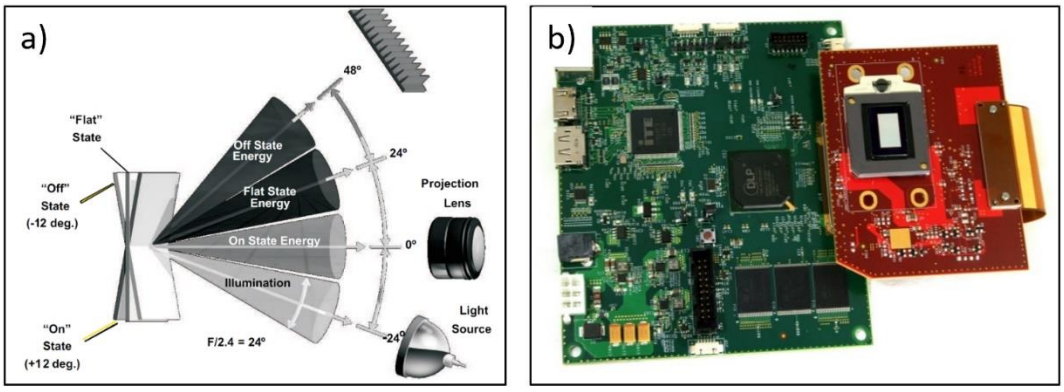

Figure 4.22. a) Operation of a single micro-mirror with 12-Degree tilt rotation and b) DLP LightCrafter 6500 Evaluation Module [150].

In overall, it is possible to achieve a patterned output light by DMD. The output light of the DMD will be modified and changed to the pattern that is designed and introduced to the SRAM of the DMD utilizing a computer. This means that light is manipulated to obtain the desired output. The desired output of the DLP is quidded by a set of aluminum mirrors and periscope toward a Polypropylene container which includes a chemical solution and bare Si sample. The image and schematic of the setup are provided in Figure 4.23.

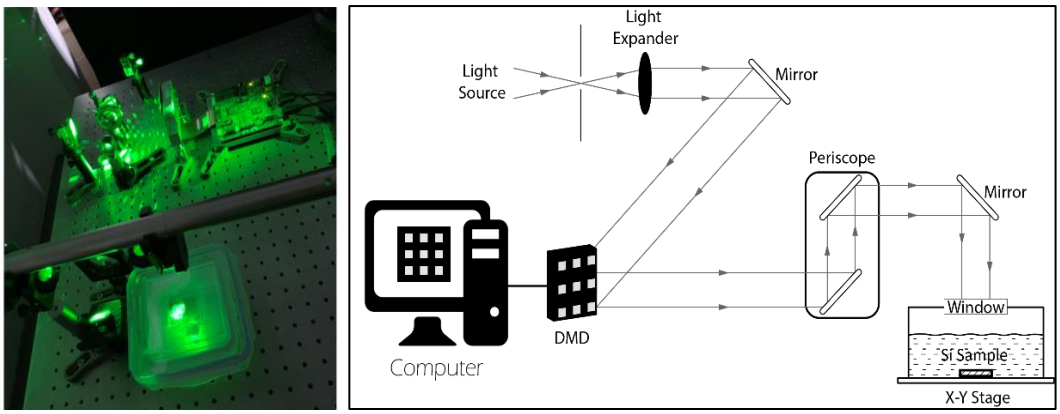

Figure 4.23. Optical photograph and schematic of the optic setup used for the photochemical etching process.

4.6 Silicon Surfaces Etched by Photochemical Etching Method

As mentioned in the previous section, the photochemical etching process takes place in an acidic medium in presence of a laser beam that injects photons which results in hole generation. The Acidic solution has the generic formula of fluoride + oxidant + water. Although the composition ratio plays a crucial role in the etching rate of the process. In this study, HF is used as the fluoride, and H_2O_2 is the oxidant. Therefore, different ratios were calculated and applied. As listed in Table 4-1 different mole ratios are used for achieving the best etching profile. Different laser powers were applied for each solution but the etching process didn't even start for solution1,2 and 3. The best etching under the illumination of a CW 532 nm wavelength laser at 500 mW power was achieved for the solution ratio of 1.02 M HF: 0.33 M H_2O_2: 4.25 M DI water. The other point is that we found out that immersing the samples into the HF solution before starting the process affects the etching rate. According to that, the samples are immersed in 50% HF solution for 15 minutes before the etching process. The SEM image of the Si surfaces etched at 500 mW power illumination and solution 4 and 5 are presented in Figure 4.24. The other parameters which can affect the etching process such as laser power and illumination time are discussed in detail in this chapter.

Table 4-1. The solution ratios used for the photochemical etching process.

Solution	HF	H_2O_2	DI water	Result
1.	0.45 M	0.2 M	3.67 M	Etching didn't start
2.	0.68 M	0.3 M	3.83 M	Etching didn't start
3.	0.68 M	0.35 M	3.75 M	Etching didn't start
4.	0.9 M	0.33 M	4.1 M	Etching started partially
5.	1.02 M	0.33 M	4.25 M	Etching started

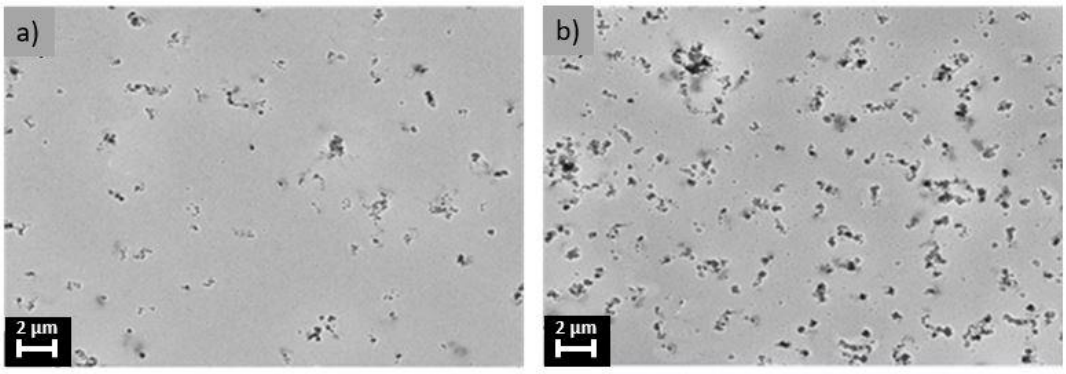

Figure 4.24. Si surfaces are etched a) in solution 4 and b) in solution 5 under the illumination of a 500 mW laser power.

4.6.1 Optimization of Fully Etched Silicon Surfaces

Firstly the whole surface of the sample was illuminated without introducing any pattern to DMD. For this purpose, a 25 mm^2 square on the DMD screen was illuminated. Accordingly, the output light of the DMD that is guided to the sample will be in the shape of a square with a dimension of 5 mm. the laser power and illumination times are optimized in the next sections.

4.6.1.1 Illumination Time Optimization

To optimize the illumination time, samples were illuminated with the same laser power but for different durations of 5 minutes, 15 minutes, and 30 minutes. The achieved results prove that the etching profile does not change too much after 15 minutes and results are not different for 15 minutes and 30 minutes of etching. The etched n-type Si surfaces at a laser power of 500mW for 5, 15, and 30 minutes are presented in Figure 4.25. According to the achieved results, 15 minutes of etching is chosen for the rest of the experiment.

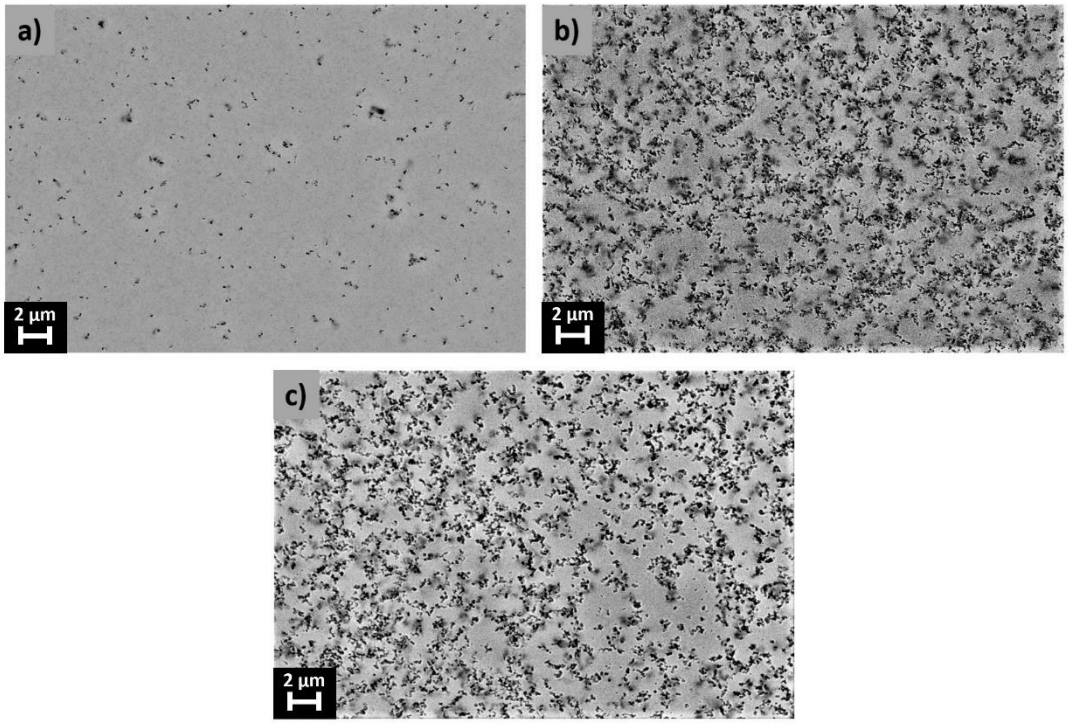

Figure 4.25. SEM images of the n-type Si surface etched by photochemical etching method at a laser power of 500mW for a) 5, b) 15 and c) 30 minutes.

4.6.1.2 Laser Power Optimization

For the first attempt, different laser powers are applied to the Si wafers which are immersed in the chemical solution. Laser power from 700 mW to 400 mW is applied

with steps of 50 mW for 15 minutes. The proper etching was not achieved for laser powers less than 400 mW. On the other hand, at 700 mW surface is damaged and etched at different angles. The SEM images of 700 mW, 650 mW, 500 mW, and 400 mW laser powers are provided in Figure 4.26 a-d. Obviously at high powers etching is much denser which causes better light trapping. According to the reflectance measurements presented in Figure 4.27, the minimum reflectance is about 10% and it is achieved for Si wafer irradiated at 650 mW power. As it is illustrated the reflectance decreases as irradiation power increases. But after 650 mW reflectance is increased for 700 mW which can be due to the higher diffused reflection.

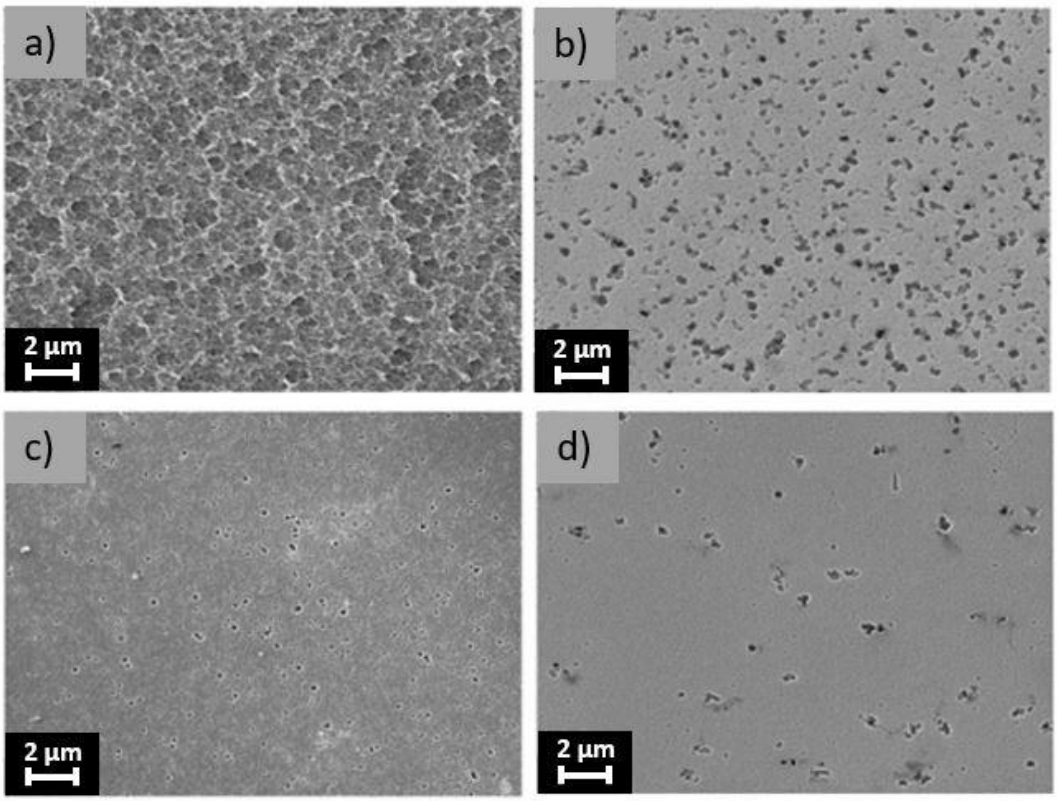

Figure 4.26. SEM images of full surface etched with laser power of a) 700 mW, b) 650 mW, c) 500 mW, d) 400 mW.

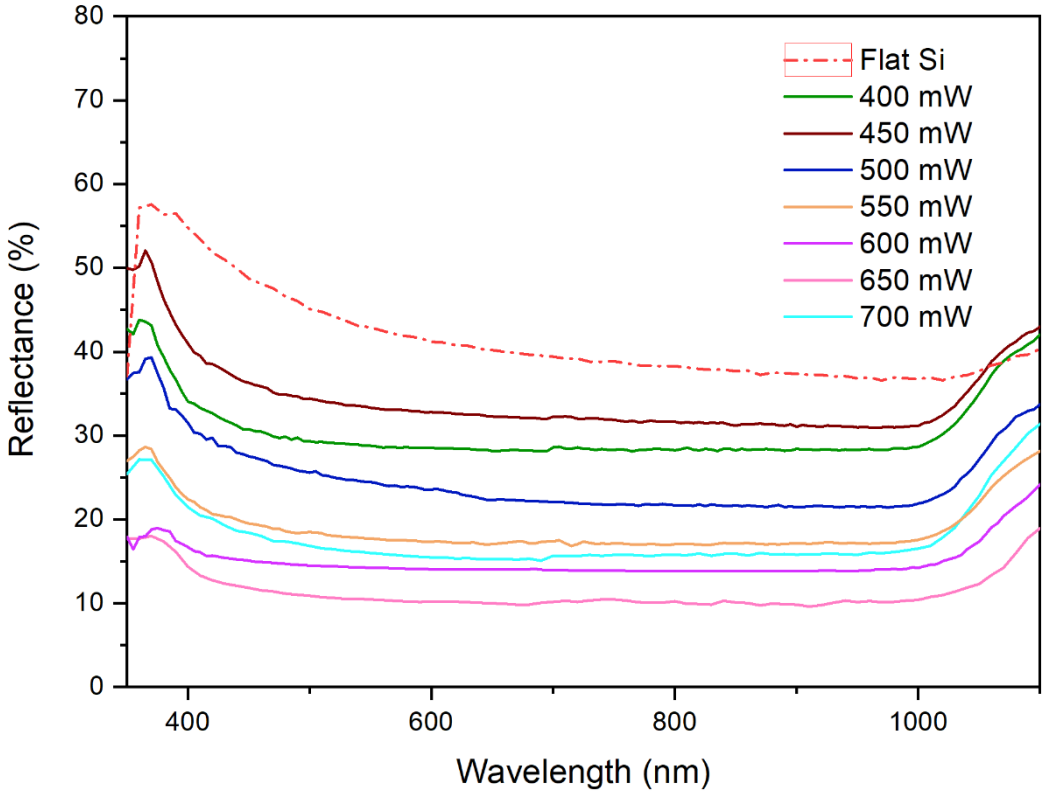

Figure 4.27. The reflectance of silicon surfaces etched by the PCE method at different laser powers.

4.6.2 Optimization of Partially Etched Silicon Surfaces

As mentioned in the previous section it is possible to apply a certain pattern and modify the laser beam by using a DMD. Accordingly, it is possible to illuminate a certain part of the silicon surface and etch a certain percentage of the surface. For the first attempt, a classic checkerboard is designed and applied. Using such a pattern 50% of the surface will be illuminated and etched. The designed pattern and the image of a beam with a checkerboard pattern with 150 µm dimension of squares captured by a DCC1545M Camera are presented in Figure 4.28. The dark squares are related to the off-mirrors meaning that there is not any light projected on the pixels. The white squares, on the other hand, are related to the on-mirrors which reflect the light.

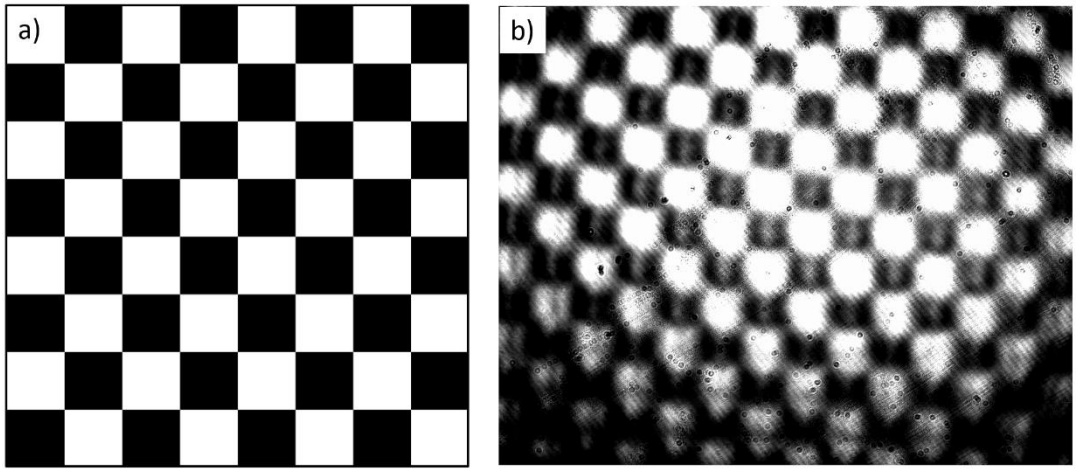

Figure 4.28. a) introduced checkerboard pattern to the DMD and b) the modified output light of the DMD captured by the camera.

The SEM image for the fully etched and partially (checkerboard pattern) etched silicon surfaces are presented in Figure 4.29. Surfaces are etched in the same solution with the formula of 1.02M HF: 0.33 M H_2O_2: 3.67 M H_2O and laser power of 500 mW for 15 minutes. Note that since the patterned light lost about half of its intensity due to the off mirrors, the overall laser power decreases to 270 mW, however, the intensity/pixel and the power on each mirror are not changed.

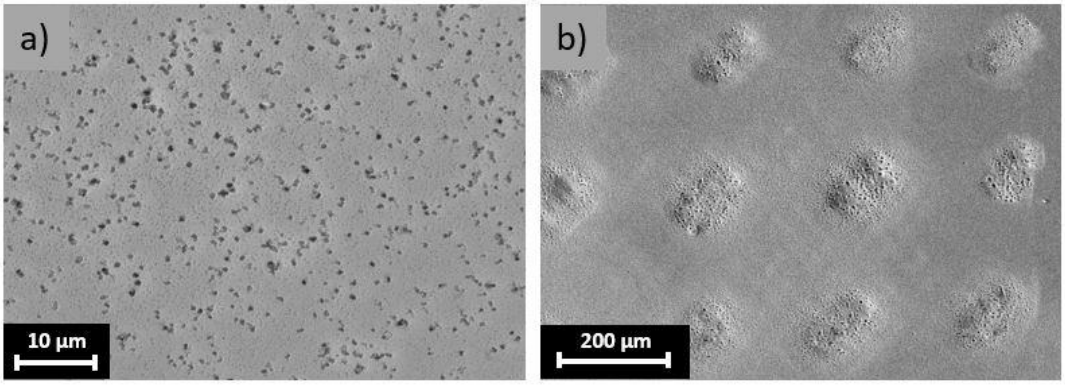

Figure 4.29. SEM image of a) fully etched and b) 50% etched silicon surfaces by photochemical etching method.

SEM image of the silicon surface etched with laser power of 300 mW utilizing a checkerboard pattern and the magnified SEM image related to a single illuminated region is presented in Figure 4.30. The point is that however the off-regions (the

squares which are not illuminated with light) are expected to remain smooth, the regions are also etched due to the light diffusion. But the point is that the density of the nanoholes created at the off regions is much less than the irradiated regions. The border between the on and off regions is obvious in Figure 4.30. b.

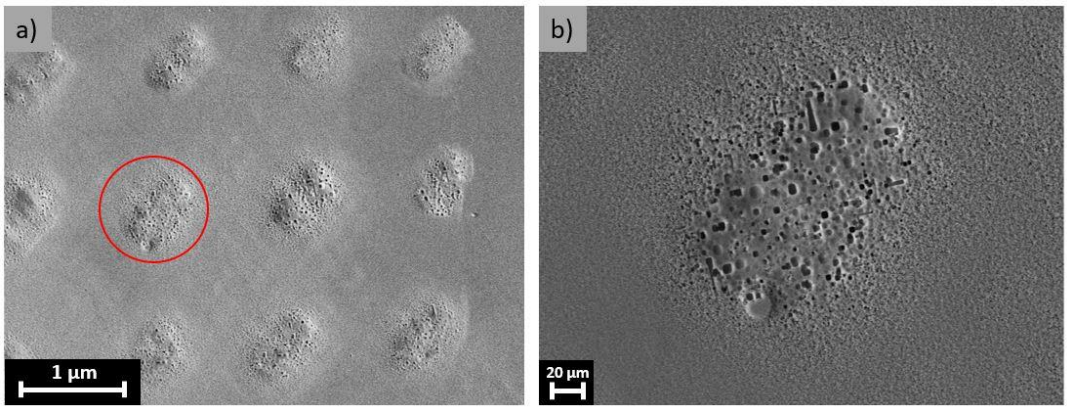

Figure 4.30. SEM image of a) silicon surface etched by DMD in a checkerboard pattern and b) magnified image of the illuminated area

4.6.2.1 Laser Power Optimization

The SEM images of the on regions achieved for periodically etched samples for different powers of 350 mW, 300 mW, 250 mW, and 200 mW are provided in Figure 4.31 a-d. Higher powers results in denser etching and higher roughness which causes higher light trapping. The reflectance measurements for each sample are also provided in Figure 4.32. As expected, the reflectance decreases as power increases, and the lowest reflectance of 18% is achieved for 350 mW. nanoholes with the dimension of 600 nm up to 1 µm were achieved for samples etched at the highest laser power of 350 mW.

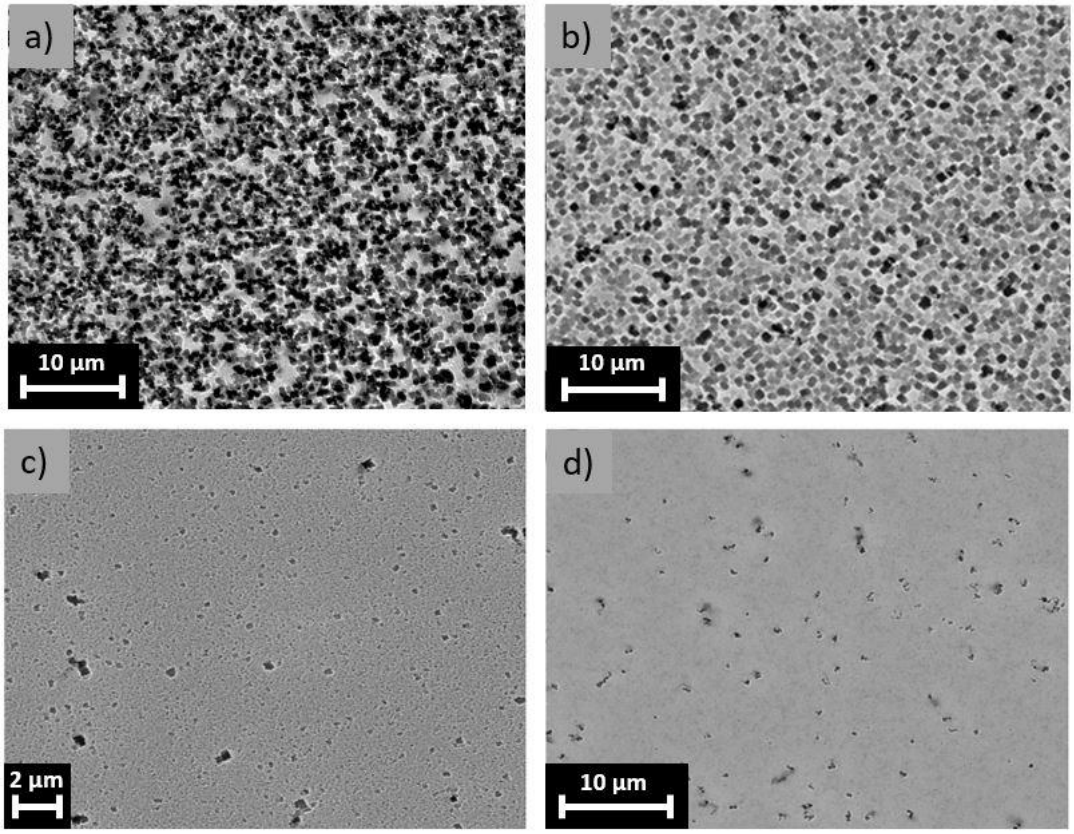

Figure 4.31. SEM images of periodically etched Si wafers with laser power of a) 350 mW, b) 300 mW, c) 250 mW, d) 200 mW. e) Reflectance of each sample.

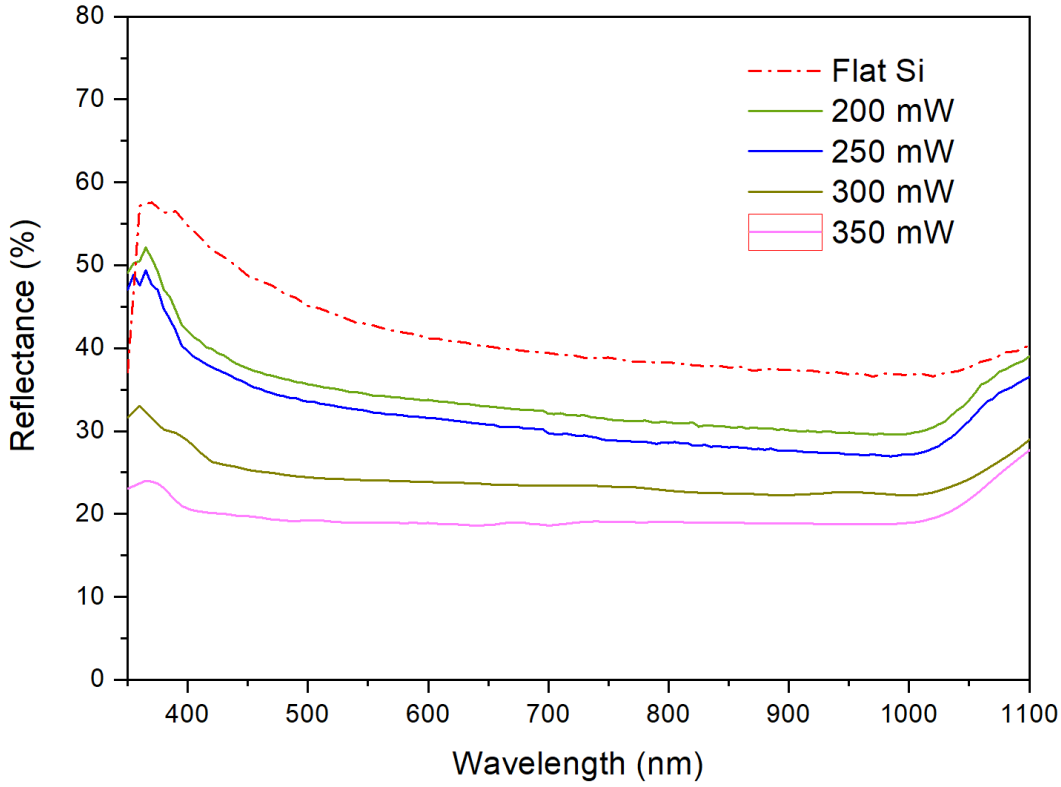

Figure 4.32. The reflectance of silicon surfaces partially etched in a checkerboard pattern by the PCE method at different laser powers.

Accordingly, the lowest reflectance was measured as 10% for silicon surfaces fully etched at 650 mW laser power and 18% for silicon surfaces partially etched (50% surface coverage in form of a checkerboard) at 350 mW laser power. The difference in reflectance of the two surfaces with respect to untextured flat silicon is presented in Figure 4.33.

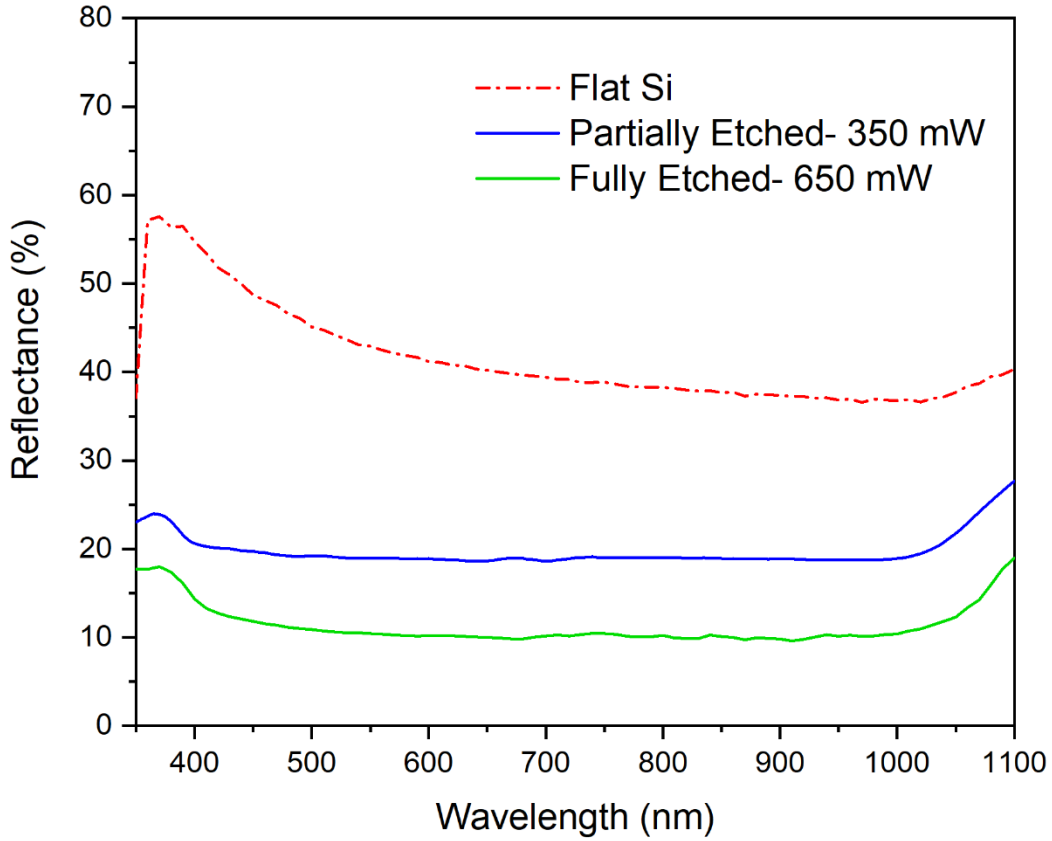

Figure 4.33. The reflectance measured for fully and partially (50% coverage in a checkerboard pattern) etched Si and flat Si.

4.6.2.2 Periodic Pattern Dimension Optimization

According to the fact that the unilluminated regions are also etched due to the light diffusion, we tried different patterns to achieve the best etching profile. The checkerboard pattern with a dimension of 100 µm, 150 µm, and 250 µm are designed and applied to the DMD. Etching results are presented in Figure 4.34. According to the results, there is an optimum value for the dimension of the squares. For 100 µm, the squares are very close to each other which results in the high-density etching of the off regions which is not required. On the other hand, in the case of large squares of 250 µm, the light is spread and results in smaller nanoholes where the off region I smoother compared to the other ones. Accordingly, it seems that the dimension periodic pattern is one of the critical parameters for pattern designing.

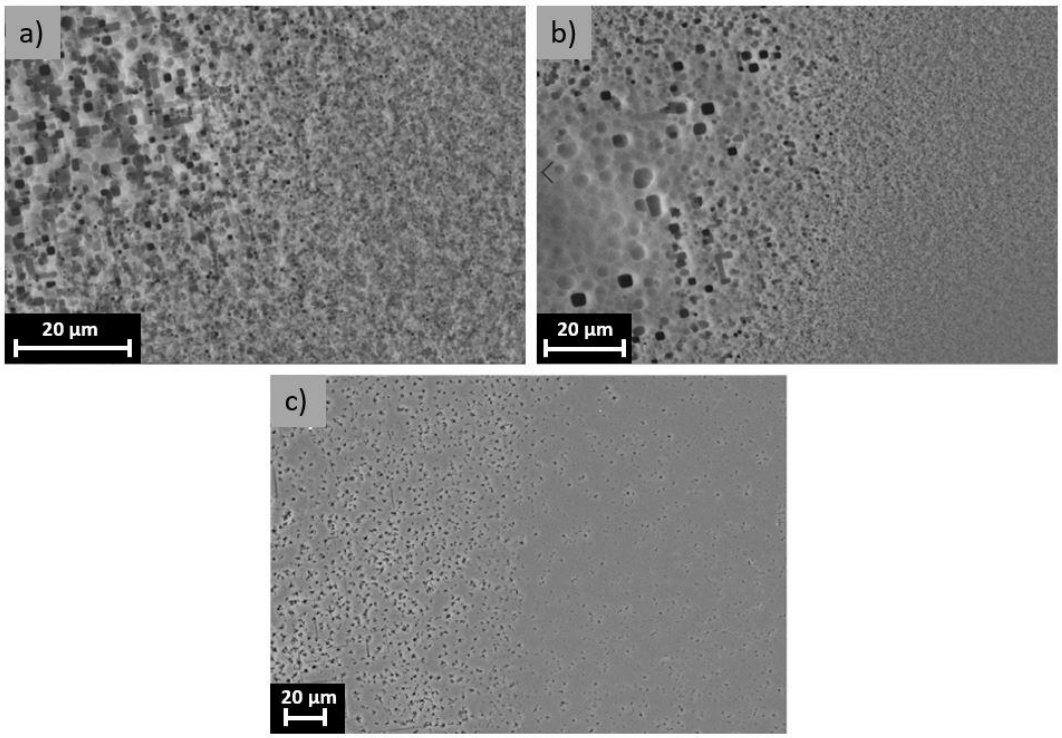

Figure 4.34. SEM image of silicon surfaces etched in a checkerboard pattern with periodic dimensions of a) 100 µm, b) 150 µm and c) 250 µm.

4.6.2.3 Duty-Cycle Optimization

One of the parameters that can be controlled by DMD is the duty cycle. It means that the illumination time can be arranged in form of on and off durations. All the previous optimizations were done at an illumination with a duty cycle of 100%. To find out the best etching profile, as a final step, samples are illuminated at different duty cycles. It means that the samples are not continuously illuminated and the illumination time is arranged with duty cycles of 50%, 70%, and 90% which is illustrated in Figure 4.35. d. The SEM images of the etched silicon surfaces related to each duty cycle are also presented in Figure 4.35.

The histograms presented in Figure 4.36 shows the distribution of holes with respect to their dimensions. According to the results, the distribution peak achieved for 70% duty-cycle seems to be broader with larger nanoholes which means that nanoholes

with similar dimensions are more for 70% duty cycle. It shows that the etching profile for 70% illumination duty-cycle is better than both 50% and 90% illumination duty-cycles.

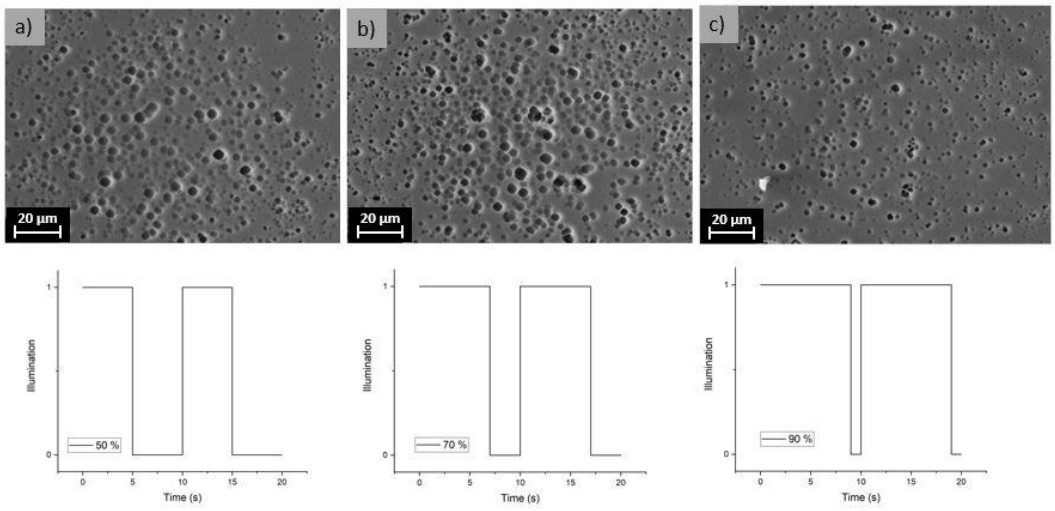

Figure 4.35. Laser-assisted etched Si Surface illuminated at duty-cycles of a)50%, b)70% and c)90% d)plots indicating the illumination duration for each duty-cycle.

To see the difference between the different regions of the etched silicon surface, the SEM images related to the illumination of 70% duty-cycle for the on-region (illuminated area), off-region (unilluminated area), and the border between on and off regions are presented in Figure 4.37. Where the nanoholes with dimensions about 1-2 µm are formed at the center of the on-region, the dimension decreases toward the edges. The off-region which is supposed to remain smooth is etched less compared to the samples etched at 100% duty-cycle. The off-region is covered with nanoholes with very small dimensions of less than 100 nm. Figure 4.38 presents the histograms for the related regions. The histograms confirm the achieved results by SEM images. The nanoholes in the middle of the on-region seem to be larger than the nanohole etched in the border of the on- and off-region. Note that the off region is not perfectly smooth and the silicon in the off region became porous due to the light diffusion. Also, the chemical itself can etch the silicon surface with a very small etching ratio. The illumination speeds up the etching process more than 10 times.

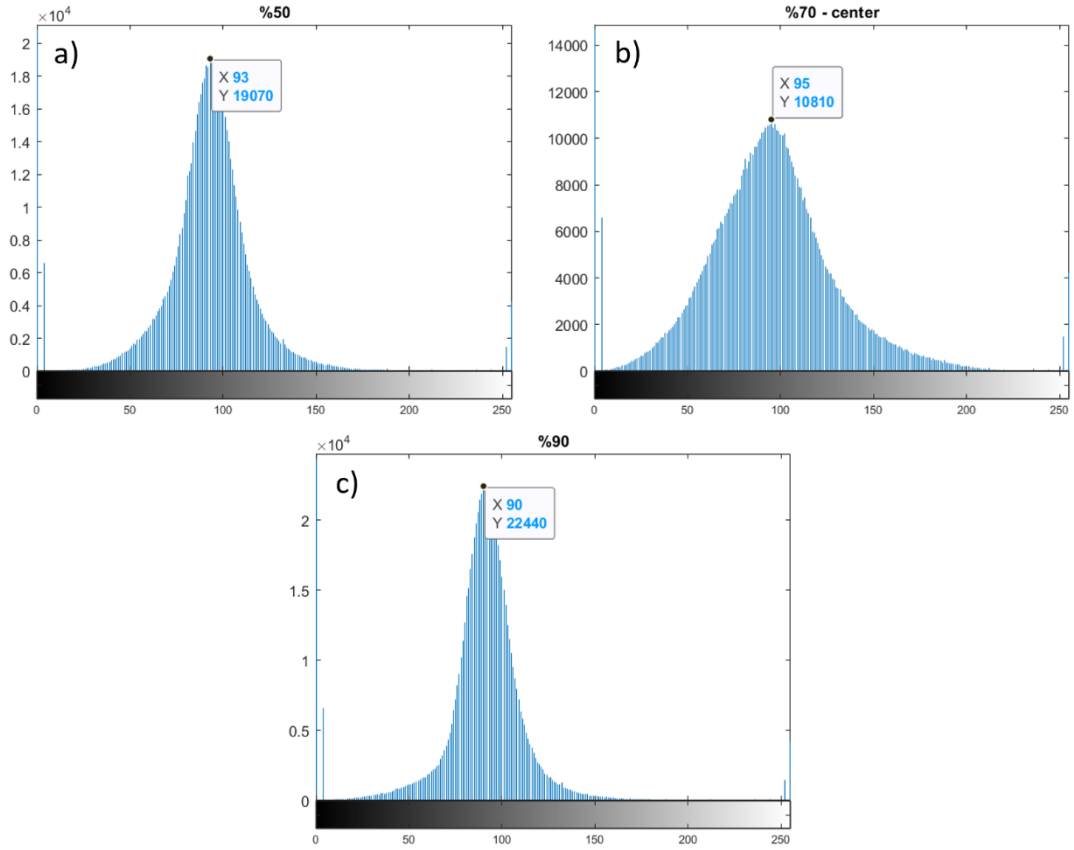

Figure 4.36. Greyscale histograms for etched Si samples illuminated with different duty cycles of a) 50%, b)70% and c)90%.

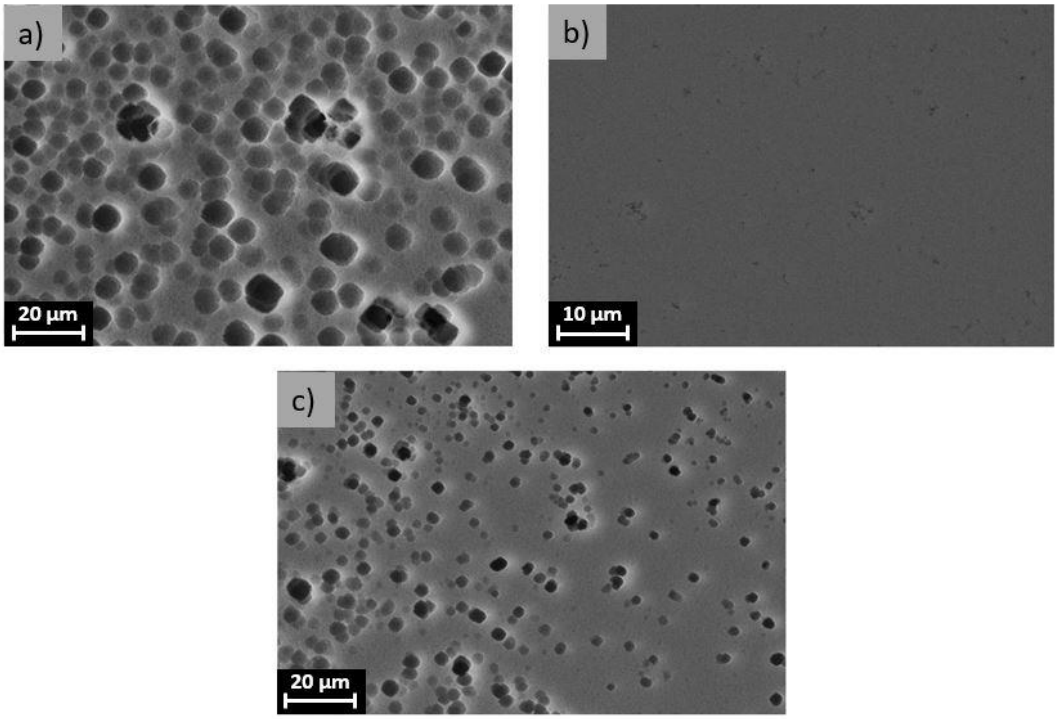

Figure 4.37. SEM images for different regions of laser-assisted etched Si sample under the illumination of 70% duty-cycle a) on-region b) off-region and, c) border between on and off regions.

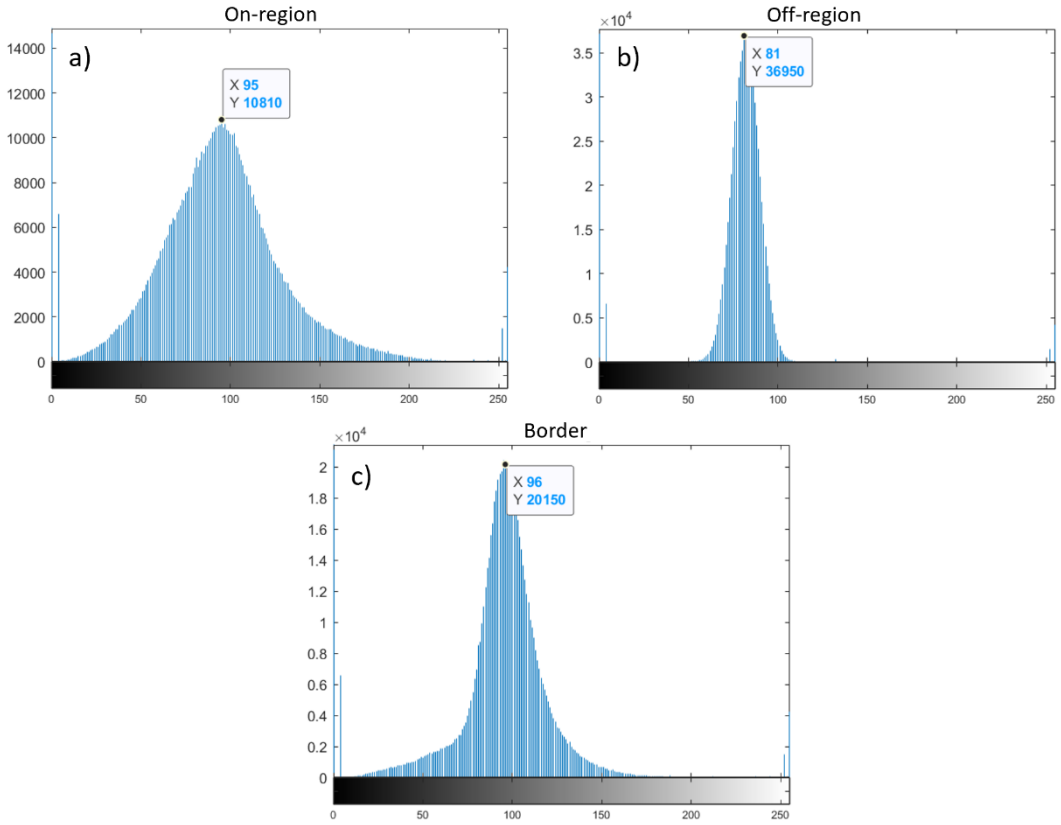

Figure 4.38. Greyscale histograms for different regions of the sample etched under the illumination of 70% duty-cycle a) on-region b) off-region and c) border between on and off-regions.

4.6.2.4 Centered Lattice-like Patterns

Since there was a 45 degrees tilt for squares in the checkerboard, a centered lattice-like pattern in circle form was introduced. To optimize the pattern, in the first step, the dimension of the circles was changed while the periodic dimension of the patterns was kept constant. A centered lattice-like pattern of circles with a circle dimension of 250 µm was designed. To achieve different surface percentages, the periodic pattern dimension between the circles which is shown as D in Figure 4.39 was changed to 1500 µm, 2000 µm, 2500 µm, and 3000 µm. The designed patterns are presented in Figure 4.39. The white circles refer to on-regions that are illuminated by light and the clack regions are off-regions that are not illuminated. The surface

coverage which means the surface ratio that is etched is calculated as 15%, 11%, 7%, and 6% and presented in Figure 4.39.

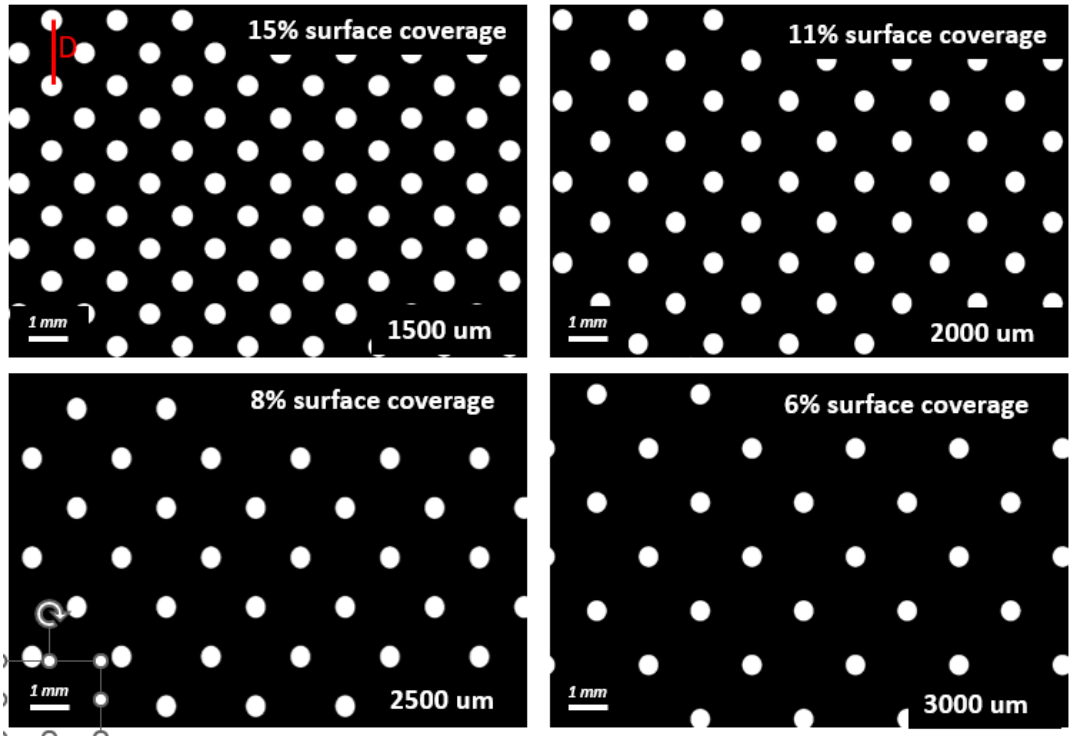

Figure 4.39. Centered lattice-like patterns with 250 µm circles and periodic patterns between the circles vary as 1500 µm, 2000 µm, 2500 µm, and 3000 µm.

The SEM images for silicon surfaces etched by applying each pattern are presented in Figure 4.40. As it is obvious from the SEM images, the off-regions are also etched the same as the previous checkerboard pattern but the on-regions are separated and are very close to the designed patterns. The nanoholes etched in the first pattern with D 1500 µm, were about 300-400 nm and the off region between the circles is etched with dense nanoholes smaller than 100 nm. As the D value increases the nanohole size in the on-region increases however the size of the nanoholes is constant. The size of the etched nanoholes increases to an average of 500 nm for a D value of 2000 µm, 700 nm for a D value of 2500 µm, and 1200 nm for a D value of 3000 µm. The size and density of the nanoholes decrease as the D value increases as it was expected. The SEM images of the on-region of each pattern are presented in Figure 4.41

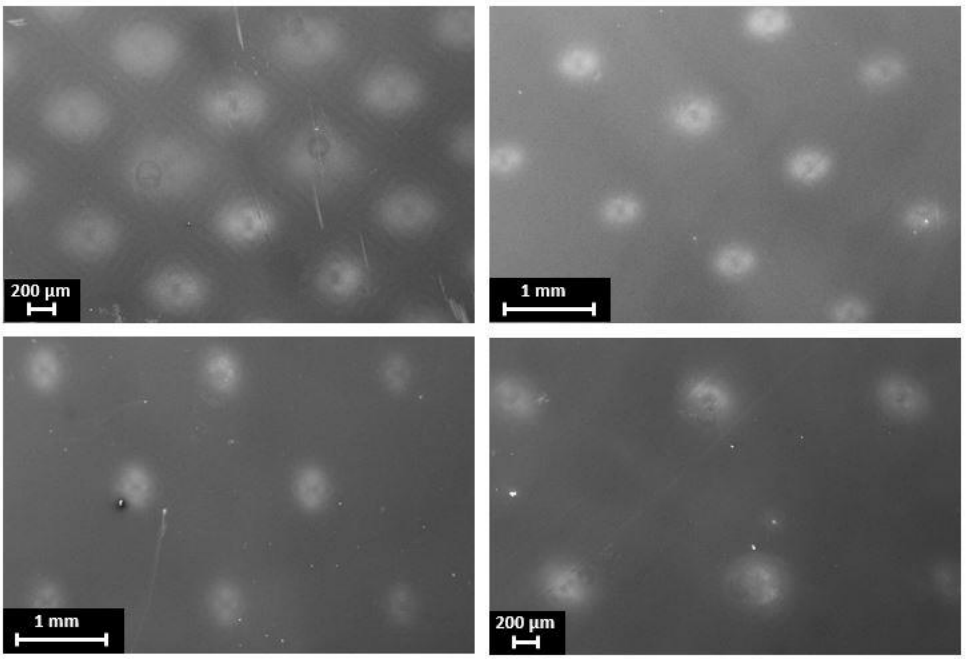

Figure 4.40. SEM images of silicon surface etched by centered lattice-like patterns with 500 µm circles and periodic patterns between the circles vary as a) 1500 µm, b) 2000 µm, c) 2500 µm, and d) 3000 µm.

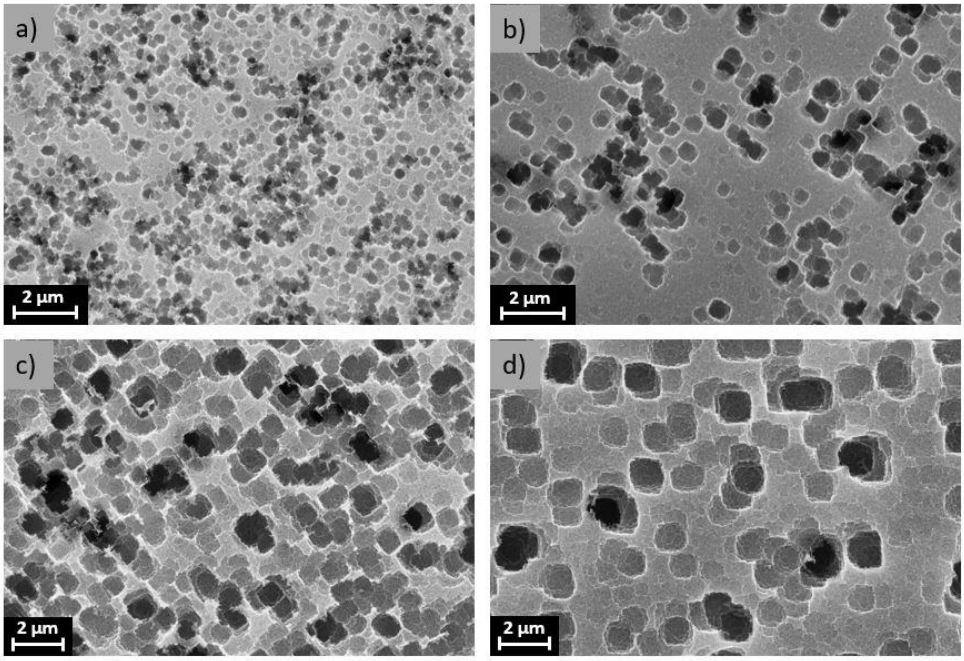

Figure 4.41. SEM images for on-regions with a radius of 250 µm related to a centered lattice-like pattern and D values of a) 1500 µm, b) 2000 µm, c) 2500 µm and d) 3000 µm.

The reflectance measurement for silicon surfaces etched by the PCE method with patterns presented in Figure 4.39 is presented in Figure 4.42. As it was expected as the D value increases, the reflectance decreases due to the decrease in the surface coverage percentage of nanoholes. Note that the porosity of the off-region decreases too as the D value increases, which also degrades the light trapping. The smallest reflection value is measured as 25-30 % for the visible range for a D value of 1500 µm. The reflectance value is high for photovoltaic applications.

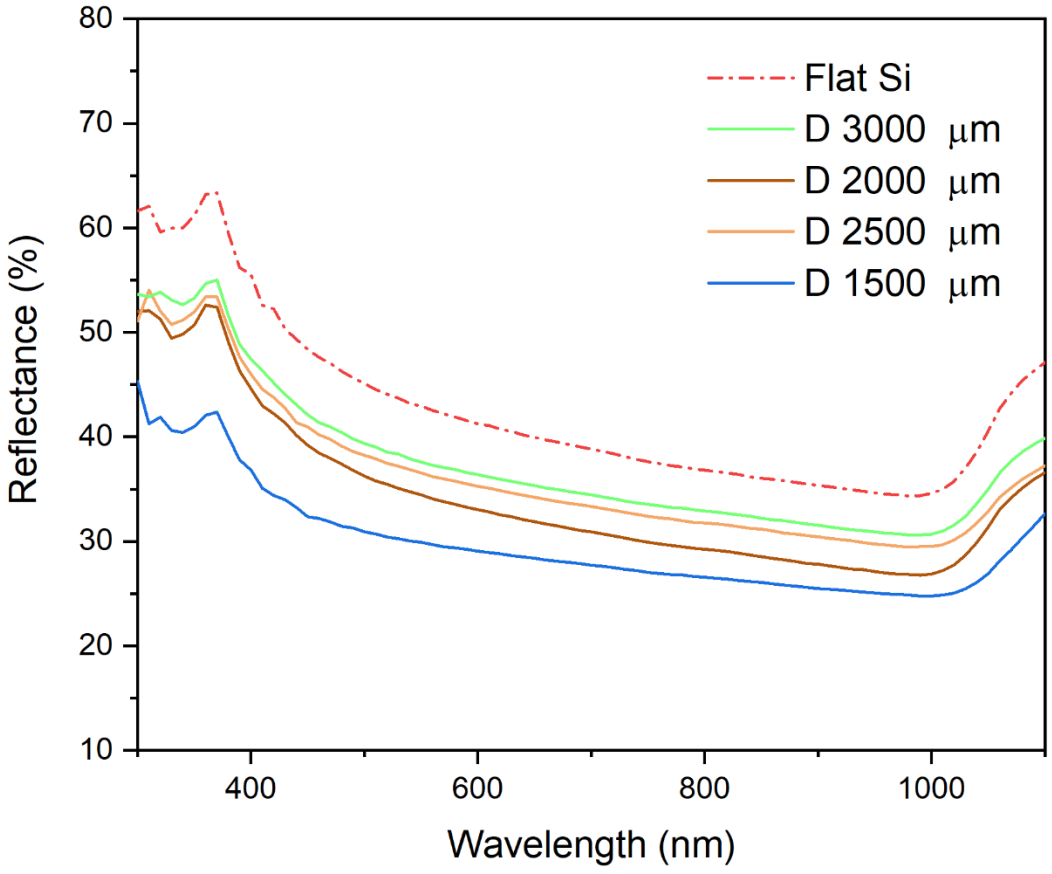

Figure 4.42. Reflectance measurement for silicon surfaces etched by entered lattice-lie patterns with a constant circle dimension of 500 µm and different D values of 1500 µm, 2000 µm, 2500 µm, and 3000 µm

The other important parameter for the centered lattice-like pattern is the size of the circles. For this purpose, the D value was kept constant at 1500 µm and the radius of the circles (r) was changed to values of 250 µm, 350 µm, and 500 µm. The designed

patterns and the surface coverage calculated for each pattern are presented in Figure 4.43.

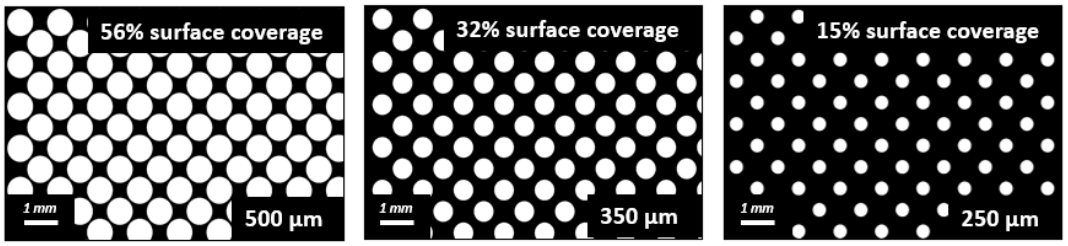

Figure 4.43. Centered lattice-lie patterns with a constant periodic dimension of 1500 µm and different circle radii of 250 µm, 350 µm, and 500 µm.

The SEM image for silicon surfaces fully etched for a square with an area of 16 mm^2 as a reference and silicon surfaces partially etched with a centered lattice-like pattern with constant D value and different on-region dimensions are presented in Figure 4.44. For this set of samples, as it is obvious from the SEM images, as the size of the on-region reduces, the produced nanoholes become denser. It is probably due to the decrease in the size of the beam which results in higher intensity. But on the other hand, the etching profile is not homogenous, the etching profile for the radius of 250 µm and 350 µm is in form of a ring rather than a circle. The center of the on-regions is etched less compared to the sides and then the etching density again decreases for the off-regions. the porosity of the silicon in the off-region decreases as the size of the on-region decreases as it was expected. The etching profile for the on-region radius of 250 µm is more homogenous.

Note that it is difficult to say an average nanohole dimension for the on-region radius of 250 µm and 350 µm since the etching profile and as a result, the dimension of the nanoholes are not constant and varies according to the location. But the etching profile and nanohole dimension produced in the pattern with a radius of 500 µm is very close to the fully etched reference.

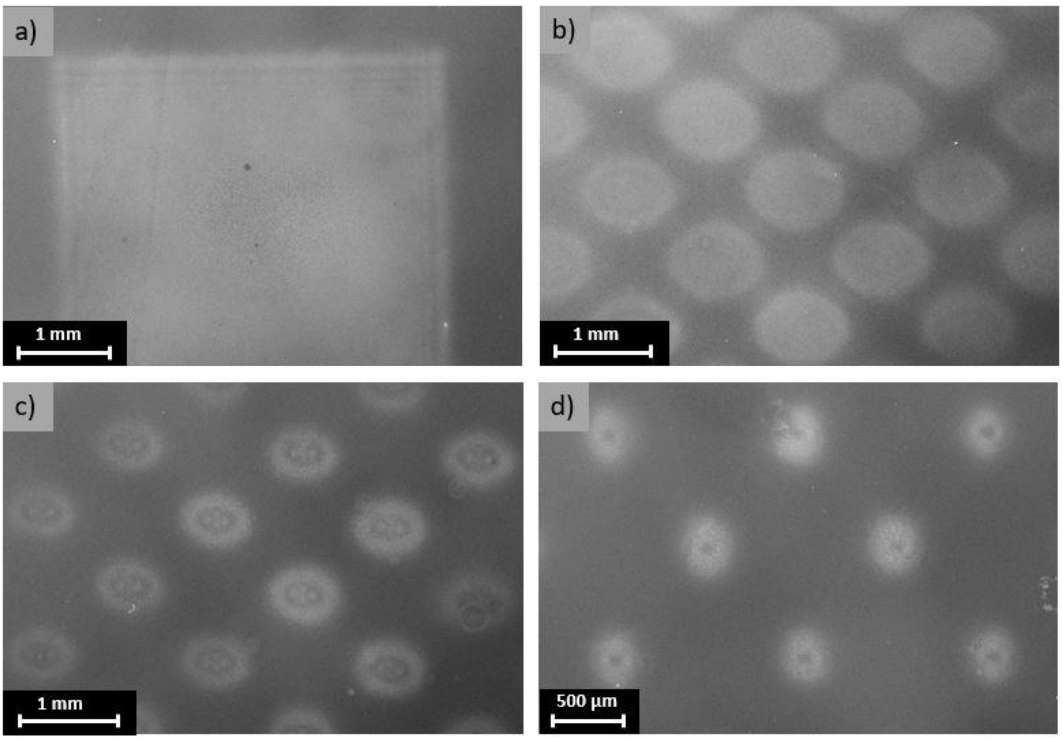

Figure 4.44. SEM images of silicon surfaces etched by PCE as a) a fully etched 16 mm^2 square and partially in centered lattice-like patterns with a constant periodic dimension of 1500 µm and different on-region dimensions of b) 1000 µm, c) 700 µm, and c) 500 µm.

The reflection measurements for the etched samples with constant D values and different radiuses are presented in Figure 4.45. According to the results, the reflectance decreases significantly as the radius of the on-region increases. The minimum reflectance was measured as 18-12% throughout the visible range for the centered lattice-like pattern with the on-region radius of 500 µm and D value of 1500 µm.

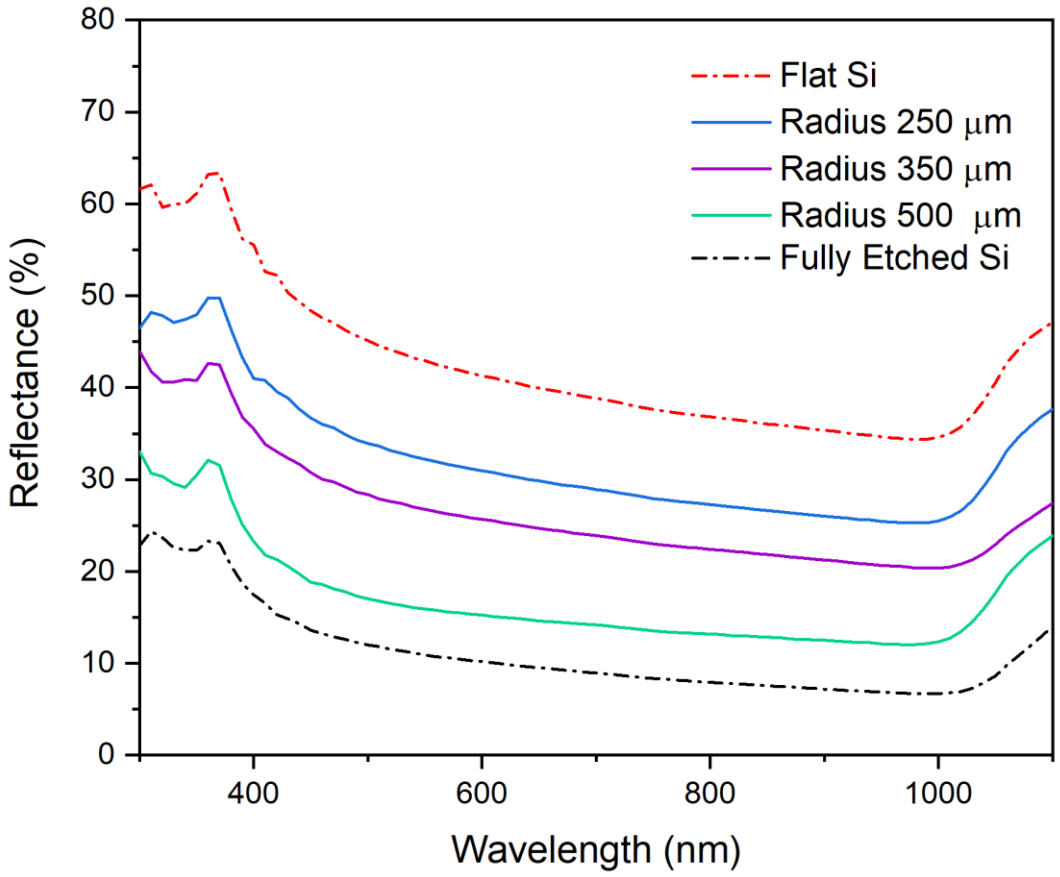

Figure 4.45. Reflectance measurement for silicon surfaces etched by entered lattice-lie patterns with a constant periodic dimension of 1500 μm and different on-region dimensions of 500 μm, 700 μm, and 1000 μm.

According to all the results and optimized parameters, the fully etched square and partially etched square with a centered lattice-like pattern with on-regions in the form of circles with a radius of 250 μm and D value of 1500 μm were chosen for the rest of the sturdy. They both have a more homogenous etching profile compared to the other patterns. the etching process was done with overall laser power of 650 mW in the case of full illumination of 16 mm^2 square. After applying the pattern, the overall power decreases to 350 mW due to the loss of the off-mirrors. The etching time and illumination duty cycle are fixed to 15 min and 70% as well. The nanoholes produced in the fully etched square have a dimension of 700-800 nm and the nanoholes produced in the partially etched sample have a dimension of 600-700 nm. The SEM

image of the side view of the samples is presented in Figure 4.47. For both fully and partially etched surfaces the depth of the nanoholes is measured up to values of ~500-700 nm. The reflectance for the fully etched silicon sample is measured as about 10 % whereas the reflectance measurement for the partially etched sample with a surface coverage of 56 % is measured as 15% for the visible range as presented in Figure 4.45.

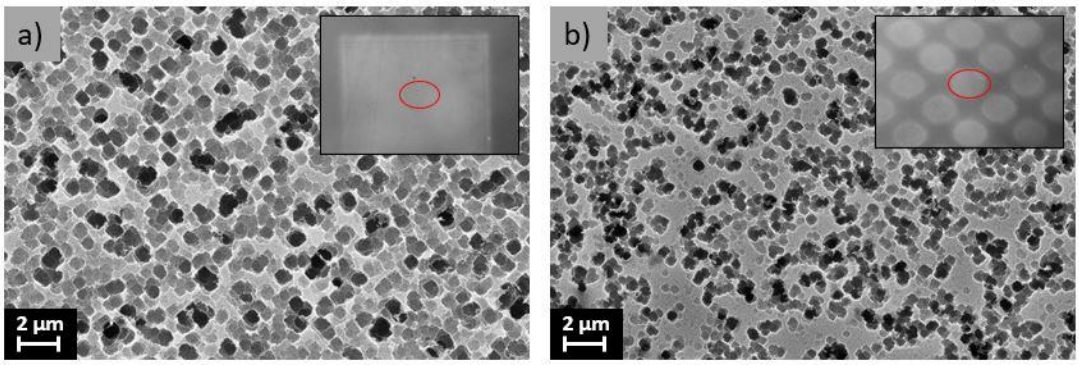

Figure 4.46. SEM image of the etched region for a) fully etched and b) partially etched (56 %) silicon surfaces.

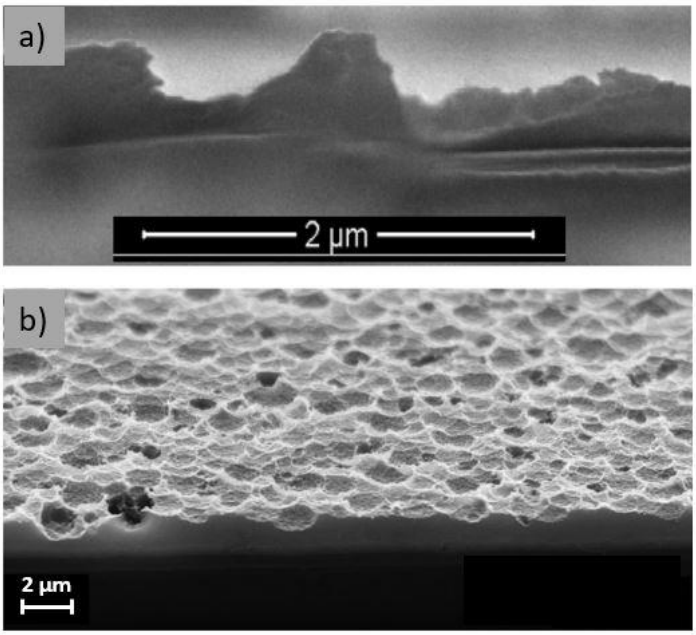

Figure 4.47. SEM image of a) magnified side view and b) overall side view for silicon surfaces etched by PCE method.

As a conclusion to this chapter, the reflectance measurements for silicon surfaces 100% etched by MACE, LIPSS, and PCE methods are provided in Figure 4.48. The lowest reflectance of about 5% is achieved for surfaces etched by MACE. The reflectance values for silicon surfaces textured by two laser-based etching methods of LIPSS and PCE are close to each other. They both have a higher value compared to MACE and it is about 10-15%. This is because of the dense and longer height of the nanostructures fabricated by MACE. The height of the nanowires synthesized by MACE is about 1 μm, the nanoholes etched by PCE have a depth of about 500 nm, and the nanostructure arrays etched by LIPSS have a height of about 200 nm. Note that the structures with larger height results in more light-trapping and less reflectance. Although the longer structures result in a higher aspect ratio and accordingly more carrier recombination. Comparing the two laser-based methods, the PCE method results in a reflectance value decreased to 10% whereas the reflectance measured for LIPSS is about 12-13%.

In conclusion, from the optical point of view, the MACE has the best performance where in decreases for PCE and LIPSS, respectively. Note that the reflectance of silicon surfaces etched by LIPSS and PCE are close to each other and there is not a significant difference. In the case of patterned samples, the trend is almost the same as the fully etched samples. The partially etched silicon surfaces by MACE have the smallest reflectance value and it increases to higher values for PCE and LIPSS. It is worth mentioning that comparing the silicon surfaces etched in 4-windows and 9-windows patterns, the 9-windows pattern with smaller dimensions of the etched and unetched regions shows a better performance in light-trapping.

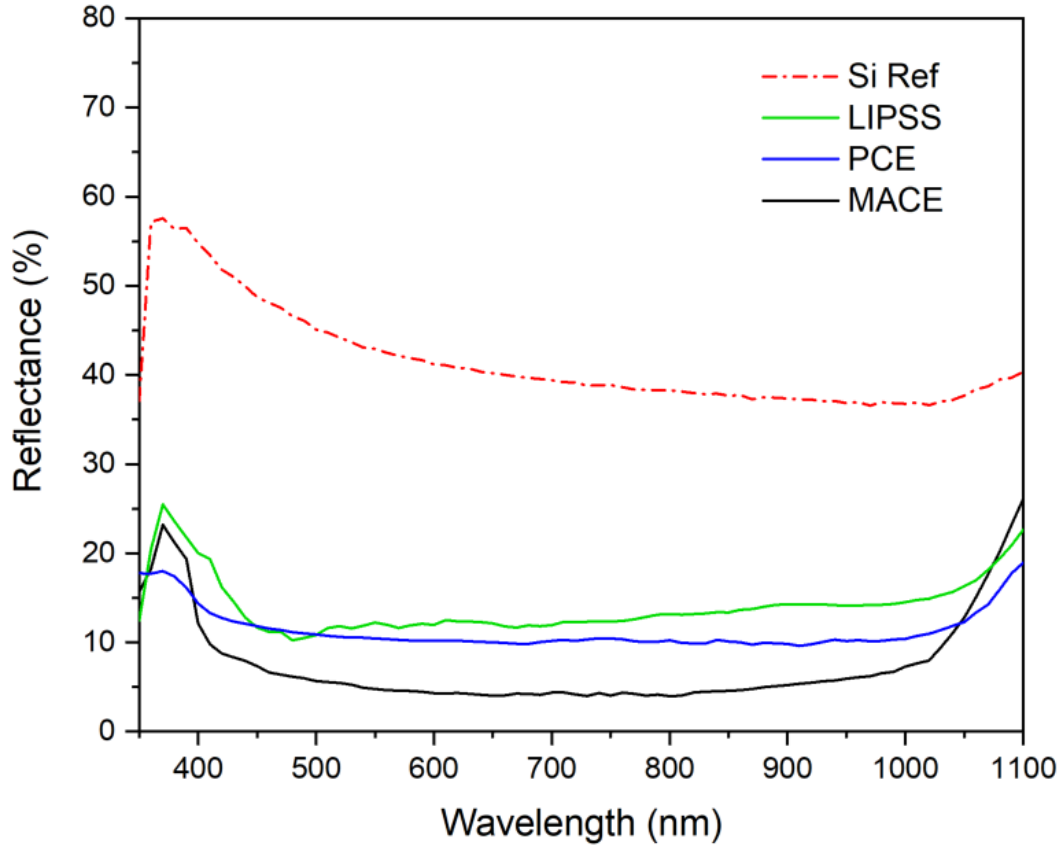

Figure 4.48. The reflectance measurement for fully etched silicon surfaces by MACE, LIPSS, and PCE methods.

CHAPTER 5

GRAPHENE/SILICON SCHOTTKY JUNCTION SOLAR CELL FABRICATION

The working principle and advantages of the graphene/silicon Schottky junction as a solar cell device were discussed in detail in Chapter 3. For this thesis, 3 different methods of MACE, LIPSS, and Photochemical etching are used to texture the silicon surface of the active area as it was reported in chapter 4. Devices with fully and partially etched surfaces with three methods are fabricated. In this chapter, In this chapter, surface texturing, device fabrication steps, graphene transferring, and doping are discussed and reported in detail.

5.1 Surface Texturing

The etching methods used for this thesis were discussed in detail in the previous chapter. The device fabrication steps, start which the surface texturing. For device fabrication, it is important to etch only the active area which absorbs the light. Keeping the rest of the area smooth improves the performance of the cells. Also, to compare the effect of partial etching of the surface in specific patterns, selective etching methods were suggested in Chapter 4. Since MACE and PCE are solution-based and LIPSS is a direct texturing method, process steps are different for each of them.

5.1.1 Metal-assisted Chemical Etching

In the case of b-Si fabrication by the MACE method, for selective etching, the Ag should be deposited in a specific pattern. For this purpose, shadow mask was used. The Ag was deposited on 4 mm^2 squares fully and also in 4-windows and 9-windows pattern forms. The samples were annealed to form AgNPs by dewetting. Finally,

samples are moved to an etchant solution to achieve fully and partially etched squares. The metal residuals are then removed and cleaned by HNO_3 dip and a two-step RCA2 cleaning process.

5.1.2 Laser-induced Periodic Surface Structuring

For the LIPSS method, it is possible to directly etch specific regions on the wafer by controlling the laser beam and the x-y stage. The step size is about 16 μm which is equal to the beam size. 4 mm^2 squares were fully etched and partially etched in two different 4-windows and 9-windows patterns and prepared for device fabrication.

5.1.3 Photochemical Etching

In the case of the PCE method, the etching process occurs inside a solution under illumination. Due to the light diffusion and also since a very slow etching process also happens in the unilluminated regions, keeping the unilluminated electrode region smooth needs an additional step. For this purpose, a photolithography step was applied. For the step, a positive quartz mask defining the active area is designed and prepared. The active area of devices was designed as 4 mm^2 squares in this study. A positive photoresist (PR) of S1805 is spin-coated on the surface of the substrate and a PR film with a thickness of 500 nm is formed. The photoresist is soft-baked on a hotplate at 115°C for 60 s after coating to remove the solvents in the photoresist and increase the adhesion. Then the designed mask is aligned on top of the substrate, and it is exposed to UV light in the mask aligner. The substrate with exposed photoresist on it is then transferred into a developer which removes the exposed area. The schematic of the photolithography step and the photograph of the samples are presented in Figure 5.1.

The silicon samples covered by the photoresist are then immersed in solution to etch the active area. The photoresist is resistant to acidic solution and accordingly the region beneath the photoresist is not attacked. The SEM image of the samples etched

by photochemical etching is presented in Figure 5.2. After the etching process, the photoresist will be removed by immersing the samples in Acetone.

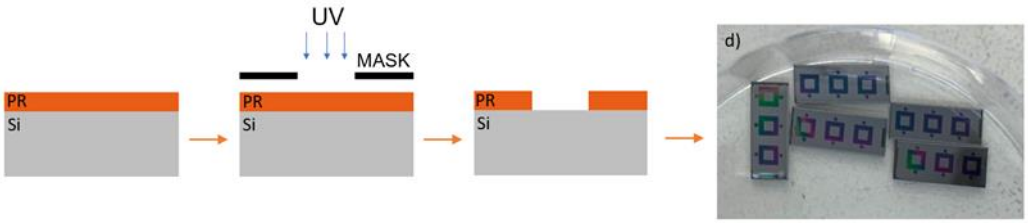

Figure 5.1. Schematic of the photolithography step for active area opening and photograph of the coated samples.

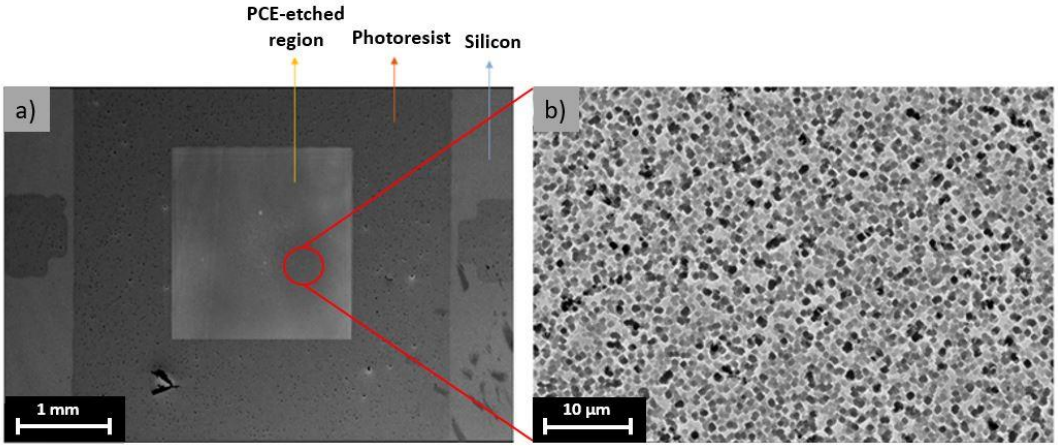

Figure 5.2. a) SEM image of 4 mm^2 area etched by PCE where the frame of the square is protected by photoresist b) The SEM image of the etched area.

5.2 Photolithography

During device fabrication for this study, a photolithography step was applied at different states. The Optical Associates INC (OAI) mask-aligner presented is used for all the photolithography steps in this study. The photograph of the device is presented in Figure 5.3. The device includes three main parts 1) a mask and sample holder, 2) a microscope, camera, and monitors for mask alignment, and 3) a UV lamp for exposure.

Generally, the photolithography step consists of three main steps. 1) Photoresist (PR) spinning, 2) exposure of the pattern, and 3) developing the photoresist. In the first step, a quartz mask is designed and prepared. Typically, copper is used to deposit in form of patterns on the quart mask. An example of a typical quartz mask with copper patterns on it is presented in Figure 5.3.a. For the photolithography step, a thin layer of photoresist is spin-coated on the silicon surface. Note that the rotation speed and time of the spin-coater control the thickness of the photoresist. Detailed information about the relation between the rotation speed and the film thickness is reported in the datasheet of each photoresist. The SPS Spin150i spin-coater with a spin speed of 1-12000 rpm presented in Figure 5.3.b is used for this study. The photoresists are also divided into positive and negative resists. In positive photoresist, the exposed areas become soluble in the developer and the unexposed area will be remained after developing. In negative photoresist, the exposed area becomes insoluble to the photoresist developer which means that the unexposed area of the photoresist will be dissolved in the developer. After spin-coating of the photoresist, the sample will be placed on a hotplate and annealed to remove the solvents in the photoresist and increase the adhesion. The required annealing temperature and duration also depend on the photoresist type and can be found in its datasheet. Then the silicon sample covered with a thin film of photoresist will be placed in the mask aligner. The designed quartz mask will be also placed in the mask-aligner, and it will be aligned to the silicon sample using the microscopic camera and monitors. The stage which holds the sample moves in three directions with steps of 1 um using a joystick. The mask and the silicon sample covered with photoresist will then be exposed to UV light. At this step, the exposed area becomes soluble in the case of a positive photoresist, and in the case of a negative photoresist, the unexposed area becomes soluble. Note that the required exposure time defers for different photoresists and their thicknesses accordingly the exposure time should be optimized. Finally, the exposed sample will be moved to a suitable remover which removes the soft photoresist resulting in specific patterns formed on the silicon sample. In order to improve the adhesion of the photoresist and finalize the patterns, another annealing

step, called hard-bake, is needed. The annealing temperature and time for the hard-bake step are also related to the type of photoresist.

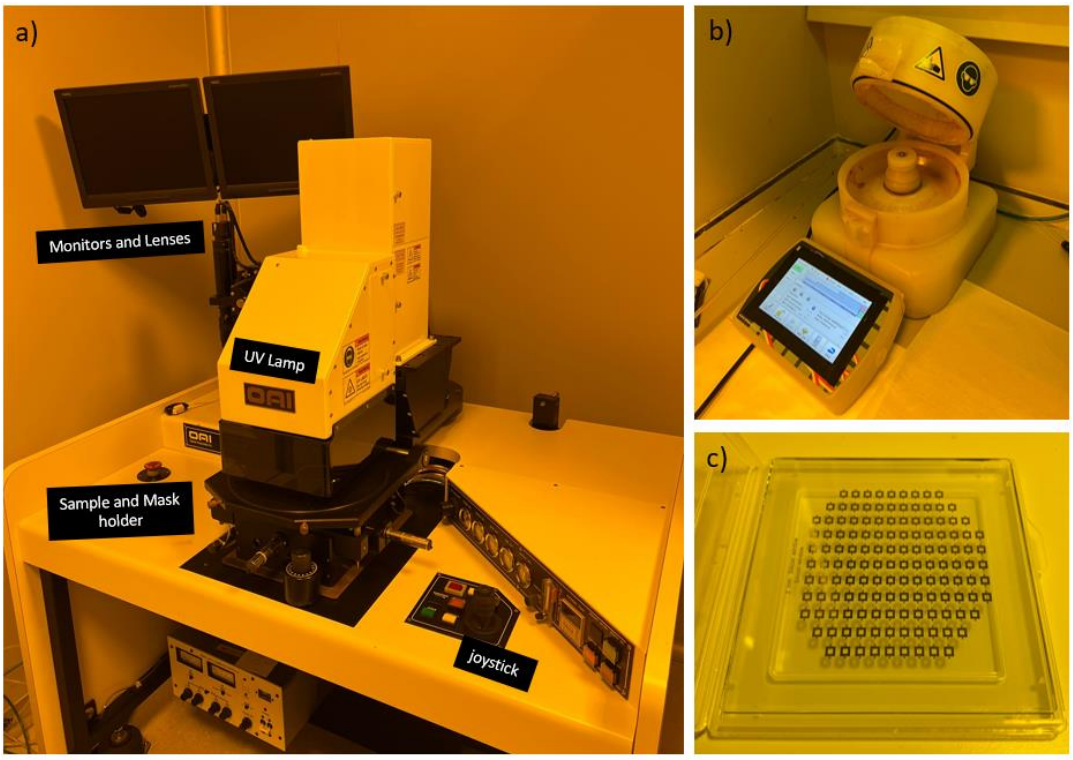

Figure 5.3. Photographs of a) Optical Associates INC (OAI) mask-aligner instrument b) a spin-coater device and c) a typical quartz mask.

5.3 Electrode Deposition

After etching the active area, the electrodes should be deposited. First, an insulator layer of SiO_2 should be formed to insulate the electrode from the silicon substrate. For this purpose, another photolithography step is applied. The same quartz mask prepared for window opening is used for this purpose too. But since at this step we want to cover the active area with a photoresist and open a frame around the active area, a negative photoresist of AZ5214 is used. AZ 5214 can be used as both a positive and negative photoresist. A PR film with 1 µm thickness is spin-coated on the silicon wafer. After spin-coating of the photoresist, the sample is annealed and soft-baked at 110° C for 50 seconds. Then the quartz mask is aligned on the sample

and it is exposed to UV light in the mask aligner setup. At this step, reversal steps of reversal bake and flood exposure are applied. The sample is baked again on a hotplate which is called the reversal bake step. And then fully exposed to UV which is called the flood exposure step. Finally, the sample will be immersed in the developer AZ351. As a final result, the photoresist will act as a negative resist and the unexposed frame area will be dissolved in the developer. The active area and the rest of the area will be covered by a photoresist. To clean any possible residuals of the photoresist, the sample goes through an oxygen plasma etching process. Otto Low-pressure plasma system from Diener Electronics. An oxygen plasma step at 0.3 mbar pressure and 20 sccm O_2 flow at 60W power for 1min helps to clean the photoresist residuals. Note that this step removes the photoresist too but since the photoresist is thick enough and it is hard-baked the removed enough is little enough to not affect the process.

After the photolithography step, 300nm SiO_2 is sputtered on the sample. For deposition Nanovak NVTH-350 Thermal Evaporation System device presented in Figure 5.4 is used. This setup has a vacuum chamber for a deposition where samples and targets are placed. There are both sputter gun for sputtering and boats for thermal evaporation. the samples with photoresist on them are placed inside the chamber for deposition. Accordingly, the SiO_2 layer will be deposited on the whole surface with and without photoresist. After SiO_2 deposition, the samples are immersed in hot acetone and as a result, the photoresist with SiO_2 on it will be removed in acetone and SiO_2 will be left on the frames around the active area. This process is called the "lift-off" process. The schematic of the reverse photolithography steps, SiO_2 deposition, and the lift-off process is presented in Figure 5.5.

Figure 5.4. Nanovak Thermal Evaporation System.

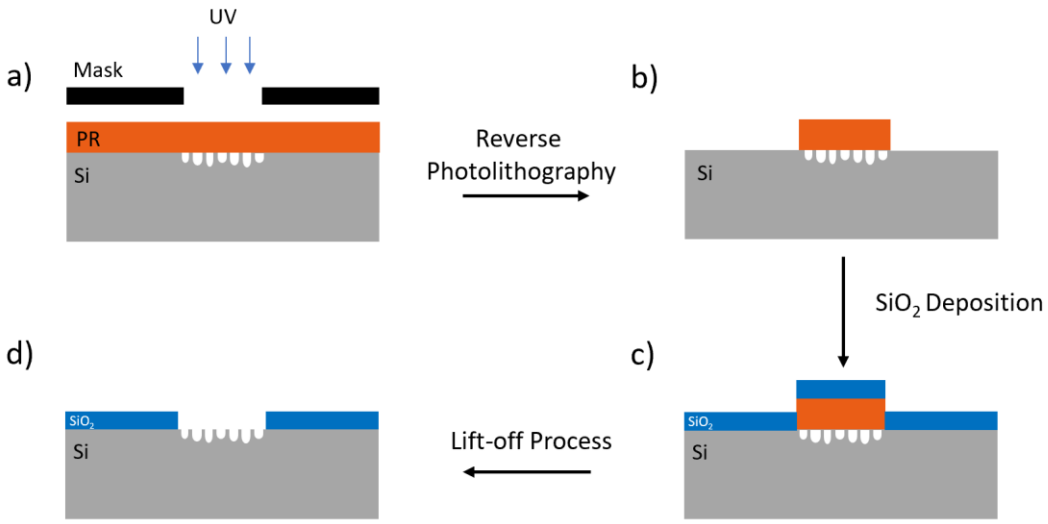

Figure 5.5. Schematic of fabrication steps of SiO_2 insulator layer. a and b) reverse lithography to open a region for SiO_2 deposition, c) 300 nm SiO_2 layer is deposited by sputtering, d) SiO_2 on photoresist is removed by a lift-off process.

It is worth mentioning that, a negative photoresist is more suitable for the lift-off process. As it is illustrated in Figure 5.6, it is possible to achieve a retrograde profile by adjusting the exposure and development time. The less exposure time results in more developer attacks which results in an undercut. It means that during the metal deposition by thermal evaporation the side walls of the photoresist are not covered, and acetone can attack the photoresist easily to remove it.

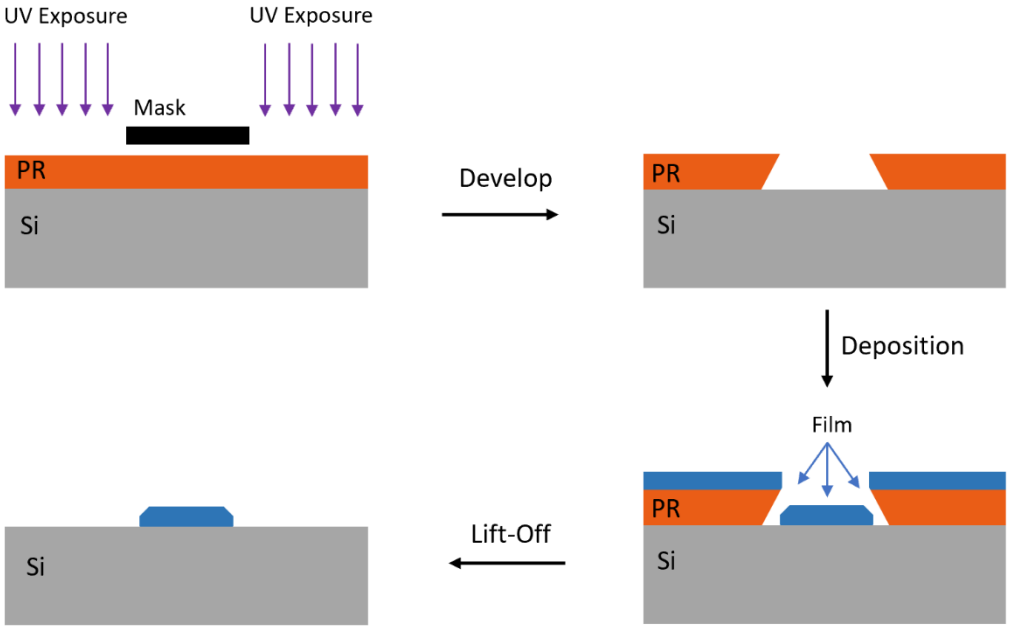

Figure 5.6. The lift-off process by utilizing a negative photoresist.

After the deposition of the SiO_2 insulator layer metal contacts should be deposited on top of it. The point is that to prevent any short circuit and leakage between the metal contact and the silicon substrate, the width of the metal contact should be less than the SiO_2. Accordingly, a quartz mask with frames with a thickness of 600 nm is designed and purchased. Another photolithography step is required to form patterns for metal contact deposition. The same photolithography step with positive photoresist of S1805 is used. 1 um thick photoresist is spin-coated, exposed, soft-baked, and developed in the developer solution. The point is that due to the nature of the positive photoresist it has a good vertical resist profile as illustrated in Figure 5.7. during the metal deposition with thermal evaporation, because of the angular distribution that almost all the methods have, the side walls of the photoresist will be covered by metal too. Accordingly, the lift-off process will be difficult in the case of using a positive photoresist. To overcome this issue, a Toluene Soek step is applied. After exposing the photoresist, before developing it, samples are soaked in Toluene for 5 minutes. It hardens the photoresist at the surface and then when the sample is transferred to the developer since the surface is more resistant to the developer, an

angular undercut etching profile will be achieved. Accordingly, after metal deposition, the side walls of the photoresist will not be covered and the lift-off process will be successful as presented in Figure 5.8.

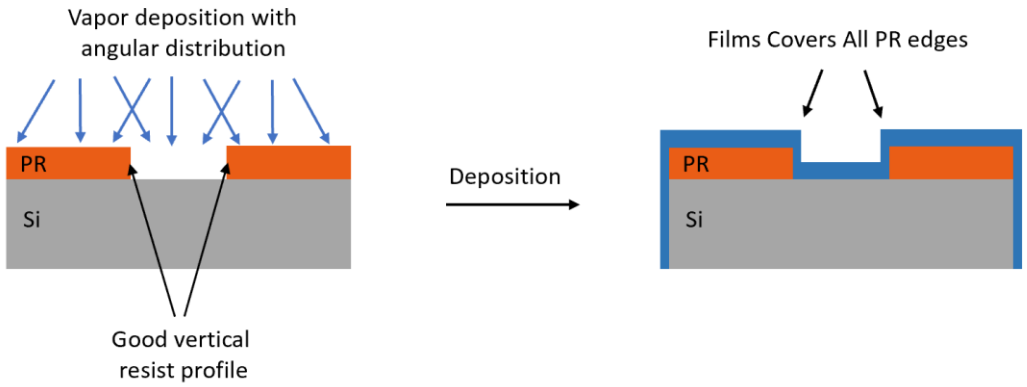

Figure 5.7. Deposition of thin film on positive photoresist with a good vertical profile.

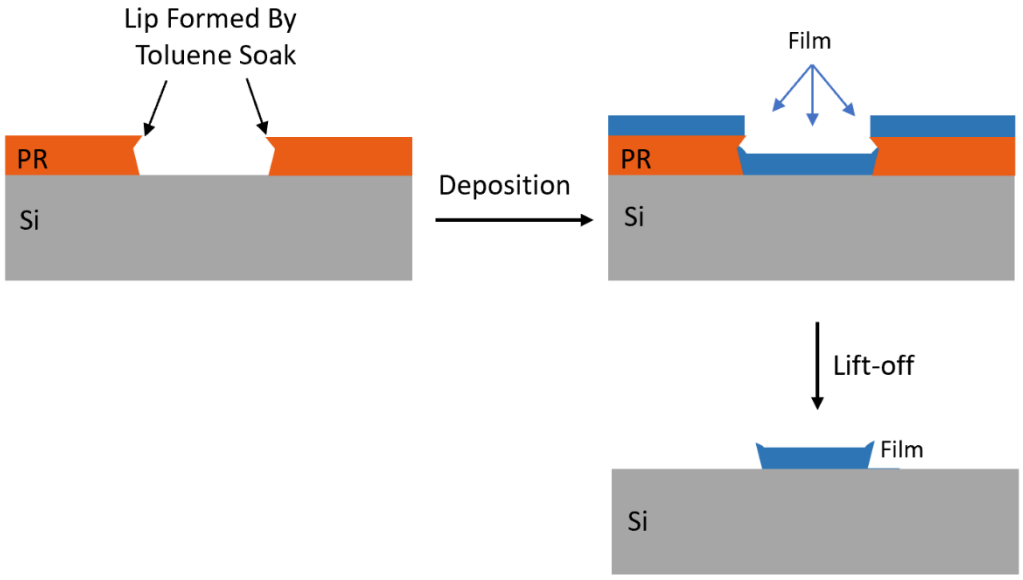

Figure 5.8. Toluene dip step used for improving the lift-off process using a positive photoresist with good vertical profiled.

After the photolithography step with the Toluene dip step, the prepared samples are transferred to the Nanovak thermal evaporation chamber for metal deposition. Gold

is used as the front electrode. To increase the adhesion of the gold to silicon, Cr is used. 5 nm of Cr is first deposited on SiO_2 and then 100 nm of Au is deposited by thermal evaporation to form Cr/Au top contact. Finally, the photoresist and the metal deposited on it are removed by lift-off process in a hot acetone bath. Finally, a 100 nm Cr/Au layer is deposited as the back contact on the backside of the samples. Note that in case of a lift-off step is applied where easy removal of photoresist is needed, the hard-bake step should not be applied. Although short, low-power oxygen plasma etching steps to remove the photoresist residuals help the lift-off process. The schematic of the electrode deposition steps is illustrated in Figure 5.9.

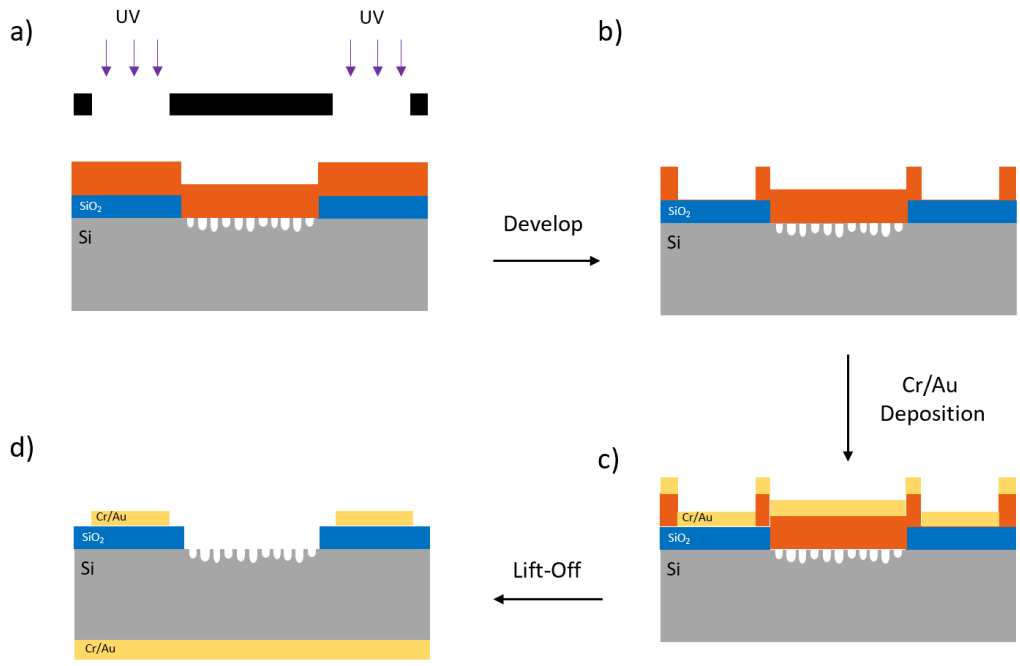

Figure 5.9. Schematic of the electrode deposition steps. a) photolithography step is applied to open the region needed for electrode deposition. b) exposed photoresist is developed after soaking in Toluene for 5 minutes c) Cr/Au thin film is deposited by thermal evaporation d) top electrodes form after the lift-off process and Cr/Au back-contact is deposited by thermal evaporation on the back-side

5.4 Wet Transfer of Graphene

A typical wet transfer process, involves the coating of CVD graphene on the copper foil with a supporting polymer film, etching away the copper, transfer of the polymer/graphene stack onto the target substrate, and cleaning off the polymer film. First, a piece of copper foil is to be prepared. A polymer such as liquid poly-methyl-methacrylate (PMMA) resist is spin-coated on one side of the copper foil. Copper foil is then baked on a hot plate to dehydrate the PMMA film and promote its adhesion to graphene. This process results in the deposition of a PMMA film on the graphene. Then, a smaller piece to be transferred is cut and left oating on an etchant aqueous solution. Copper foil is fully dissolved in the etchant solution, leaving PMMA/graphene stack oating on the surface of the etchant solution. Using a Si/SiO_2 substrate as a tool, PMMA/graphene stack is scooped and transferred into the de-ionized (DI) water bath for rinsing. The scooping process involves the unavoidable trapping of a small amount of respective etchant liquid between the membrane and substrate. This liquid serves as a buffer layer allowing the separation of the membrane from the substrate with minimal destruction when it is submerged in a DI water bath.

5.4.1 Single-layer Graphene

The wet graphene transfer process should be optimized for each step. For the first attempt, wet transfer of single-layer graphene (SLG) on a flat Si/SiO_2 wafer was applied. As mentioned in chapter 3, there is a contrast that can be detected easily by the naked eye for graphene transferred on SiO_2 and the highest contrast can be detected for SiO_2 wafers with a thickness of about 100nm and 300nm. Accordingly, commercially available Si/SiO_2 with thermally grown 300nm SiO_2 on Si from university wafers were used for optimizing the graphene transferring process. The CVD-grown graphene on Cu foil is also commercially available and purchased from ACS material. Graphene is grown by CVD on 35 μm thick copper foil. During the

growth, it is not possible to control the growth of the graphene on a single side, and accordingly, graphene is deposited on both sides of the graphene. The single-layer graphene has a sheet resistance of less than 600 Ω/sq, transparency of about 97%, and grain size of ~ 50 μm. In the first step, the unintentionally grown graphene on the backside of the copper foil should be removed. An oxygen plasma step is applied to remove the graphene on the backside. Since graphene is a single-atom-thick layer, low-power oxygen plasma will be enough to remove the layer properly. The removal process should be optimized and in this study 20 sccm O_2 flow, at 60 mW power removed the graphene properly. Then the graphene on the topside should be protected by a photoresist layer. PMMA which is a transparent photoresist is generally preferred for this process since it has minimum effect on the high transparency of the graphene. In this process, PMMA A9 with molecular weight 950k and dissolved in anisole (reduced to 4.5% solution) is used to protect the graphene. The thickness of the PMMA layer is very crucial for this process. It should be thick enough to protect the graphene. On the other hand, it is not possible to clean the thick PMMA layer properly after transferring the graphene. Accordingly, there is an optimum thickness and to find the optimized thickness the transferring process was repeated with different parameters. The optimum thickness value was founded as 300nm. To achieve this thickness PMMA was spin-coated with a spin speed of 2500 rpm for 1 min. To minimize the damage of centrifugal force on graphene, the rotation speed is increased step by step in a gradual manner from 500 rpm to 2500 rpm. Later, the sample is placed on the hotplate and annealed at 120℃ for 5 minutes to bake the PMMA. Now the hardened PMMA will act as the protection layer. Next, the sample is transferred to 97% $FeCl_3$ from Sigma Aldrich which is used as the copper etchant. The etching rate of the solution is about 0.2 μm/min. After about 3 hours the copper foil is completely etched. Next, the graphene/PMMA stack is scooped out of the solution by using a piece of thin silicon sample and transferred to DI water for 30 minutes to clean the etchant and copper residuals. To remove the etchant and residues properly, the DI water rising is repeated. Finally, the cleaned graphene/PMMA stack is scooped out by a piece of Si/SiO_2 wafer and left overnight

to completely evaporate the water that remained between the graphene layer and the substrate. Then the sample was placed on a hotplate to activate the bonds between the graphene and substrate. Next, PMMA is removed in a hot but not boiling acetone bath for 2 hours. Finally, samples are cleaned with isopropanol and DI water and dried out by nitrogen flow. The schematic of the transfer process steps is presented in Figure 5.10.

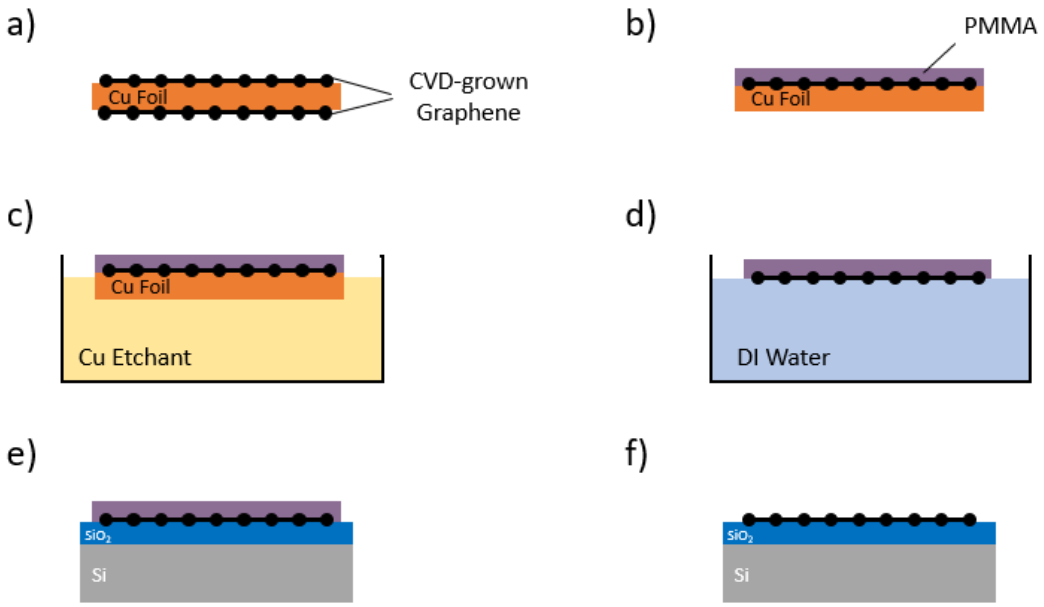

Figure 5.10. Schematic of the graphene wet transfer process. a) commercially available CVD-grown graphene on Cu foil, b) graphene on the backside of the foil is etched by oxygen plasma and graphene on the front is covered by PMMA, c) Cu foil is etched in the copper etchant, d) Cu and etchant residuals are cleaned in DI water, e) graphene/PMMA is transferred on a clean Si/SiO_2 wafer, and f) PMMA is removed in acetone.

5.4.1.1 Characterization of Single-layer Graphene Transferred on SiO_2

The microscopic image of the transferred single-layer graphene on a 300 nm SiO_2 wafer is presented in Figure 5.11. The contrast between the substrate and the

graphene is obvious from the photo. As is clear in Figure 5.11.b, there are some cracks on the graphene which are related to graphene growth on copper foil. These cracks are due to the role form of the copper foil and cannot be eliminated however, they reduce the device's performance significantly.

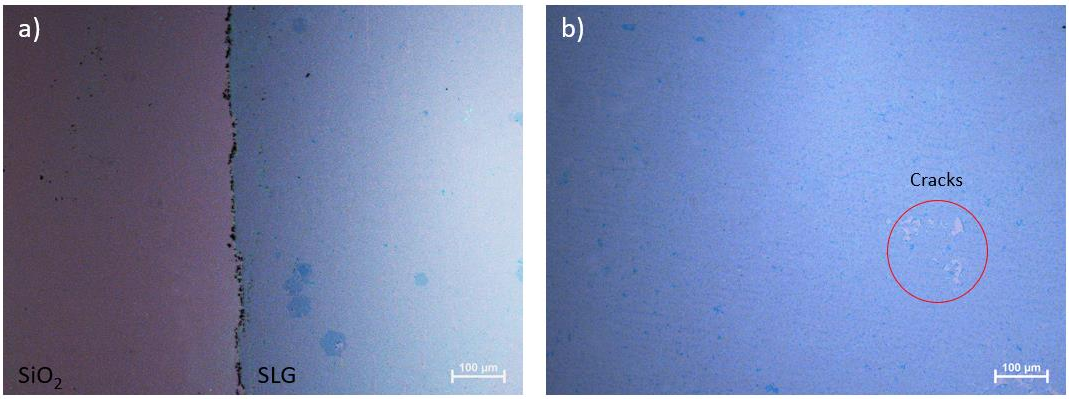

Figure 5.11. Microscopic image of the single-layer graphene transferred on Si/SiO_2 wafer by a wet transferring method illustrating the a) contrast between SiO_2 and MLG and b) overall image of the SLG and the unavoidable cracks.

The Raman spectra for single-layer graphene transferred on Si/SiO_2 wafer using the above-mentioned wet transfer process is presented in Figure 5.12. The 2D peak is located at 2678 cm^{-1} and the G peak of the graphene is located at about 1585 cm^{-1}. The Raman intensity for the 2D peak is 1.7 times higher than the Raman intensity of the G peak which indicates that the transferred graphene is a single-layer graphene. The D peak intensity is very small which indicates that the SLG is transferred with high quality.

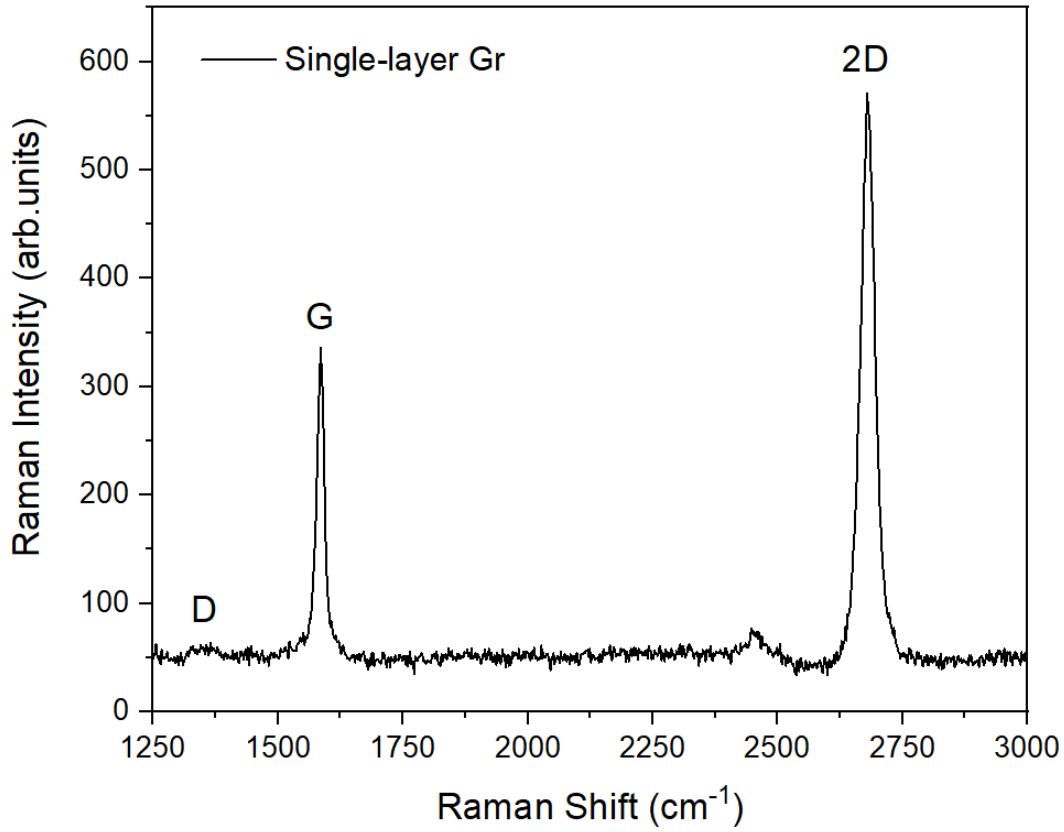

Figure 5.12. Raman spectra for single-layer graphene transferred on Si/SiO_2 wafer by a wet transferring method.

5.4.2 Multilayer Graphene

As mentioned in chapter 3, the layer number of the graphene is one of the important parameters that can change the properties of the graphene. The sheet resistance of the graphene decreases as the layer number increases to 4 layers. On the other hand, the absorption will increase for the higher number of layers which is not preferred. To achieve the 4-layer graphene, the transferring processes should be repeated four times and each time a single-layer graphene should be transferred. But this method has some disadvantages since during each transfer process there will be cracks and defects in graphene and also there will be some PMMA contamination and residues between the layers. All these together degrade the graphene quality significantly.

Accordingly for this study, commercially available 3-5 layer graphene grown on copper foil by CVD was purchased from ACS material. The same transferring process was applied to transfer the multilayer graphene (MLG) on Si/SiO_2 wafer. The microscopic image of the multilayer graphene transferred on the SiO_2 substrate is presented in Figure 5.13. Compared to single-layer graphene it has higher contrast since the absorption increase for MLG. Moreover, since graphene is deposited multiple times there are not any sharp cracks where graphene is not found at all. It means that the carrier conductivity increases and sheet resistance decreases.

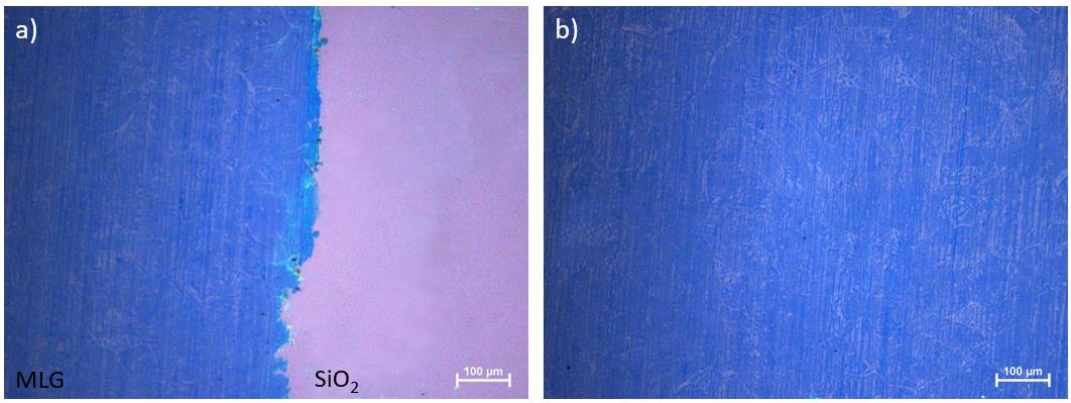

Figure 5.13. Microscopic image of the multilayer graphene transferred on SiO_2 substrate with the wet transferring process.

The Raman spectra measured for MLG are presented in Figure 5.14. In the case of MLG, a right shift for the G and 2D peaks is expected [151]. Also, the I_{2D}/I_G ratio decreases as the layer number increases [151], [152]. The G peak for MLG is shifted to 1586 cm^{-1} and the 2D peak is shifted to 2693 cm^{-1}. There is a significant shift of about 15 cm^{-1} for the 2D peak as expected. The intensity of the G peak is increased and the I_{2D}/I_G ratio is decreased to 0.73. The intensity of the D peak located at 1400 cm^{-1} which is related to the defects in graphene is increased since the defects and cracks increase in the case of MLG.

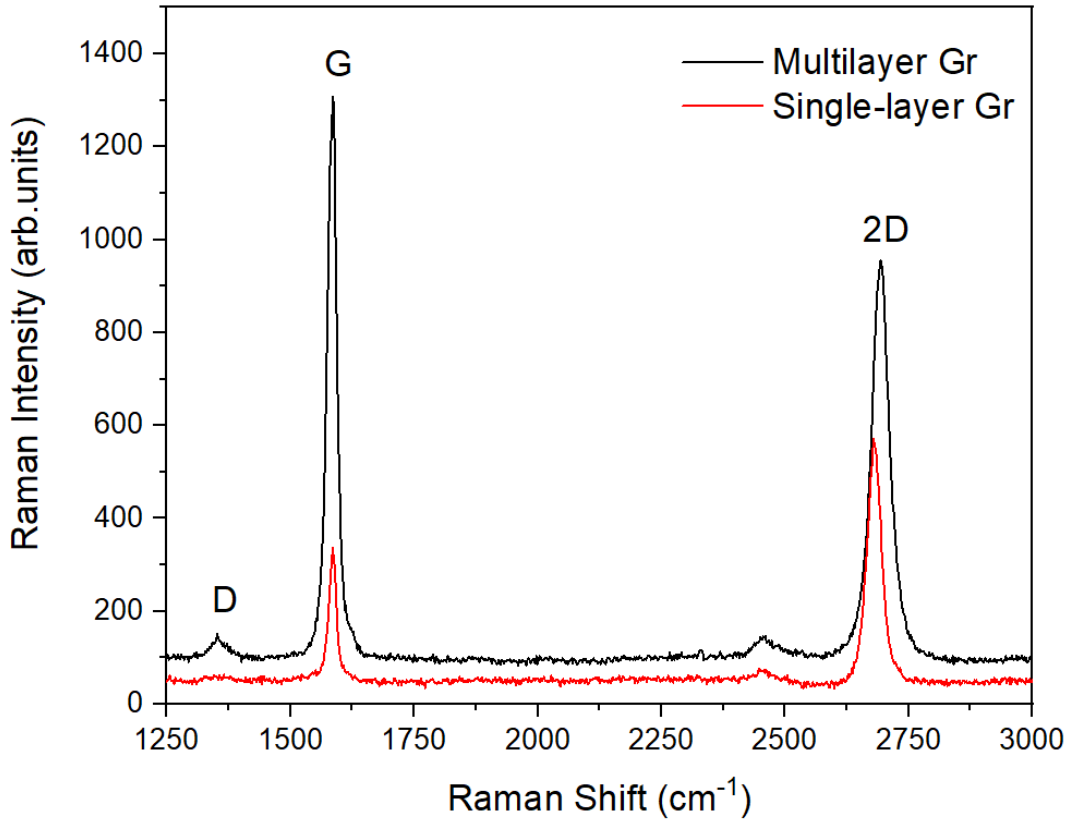

Figure 5.14. Raman spectra for multilayer graphene transferred on SiO_2 substrate with the wet transferring process.

5.5 Graphene Doping by HNO_3 Treatment

As mentioned in chapter 3, it is possible to tune the working function of the graphene by molecular doping which is called graphene doping. In 2010, Bae et al. [152] reported graphene doping by HNO_3 with reduced sheet resistance from 300 $\Omega.sq^{-1}$ to 125 $\Omega.sq^{-1}$. They reported low stability for this doping and there was a lack of information about surface chemistry after doping. Later in 2016, D'Arsie et al. [153], reported a detailed study in p-doping of graphene by low-concentrated, high-concentrated, and heated high-concentrated HNO_3 Acid. They reported that the G and 2D Raman peaks of graphene shift right after doping. The shift increases for increasing doping. Although they reported a decrease in I_{2D}/I_G value as the graphene is doped. Efficient graphene doping with different materials such as

bis(trifluoromethanesulfonyl)- amide (TFSA) [86] and $AuCl_3$ [154] were also reported for Schottky solar cell applications. In this study, HNO_3 has been used to p-dope the graphene for Schottky solar cell applications. The SLG is exposed to HNO_3 for 1 minute, 5 minutes, and 10 minutes. The Raman spectra presented in Figure 5.15 shows that the G and 2D peaks are right-shifted for longer doping time. The values for peak positions for undoped and doped SLG with different doping times are listed in Table 5-1. Also, the I_{2D}/I_G ratio is 1.7 for pristine graphene and it decreases to values of 1.06, 1.01, and 0.96 for 1 minute, 5 minutes, and 10 minutes of doping.

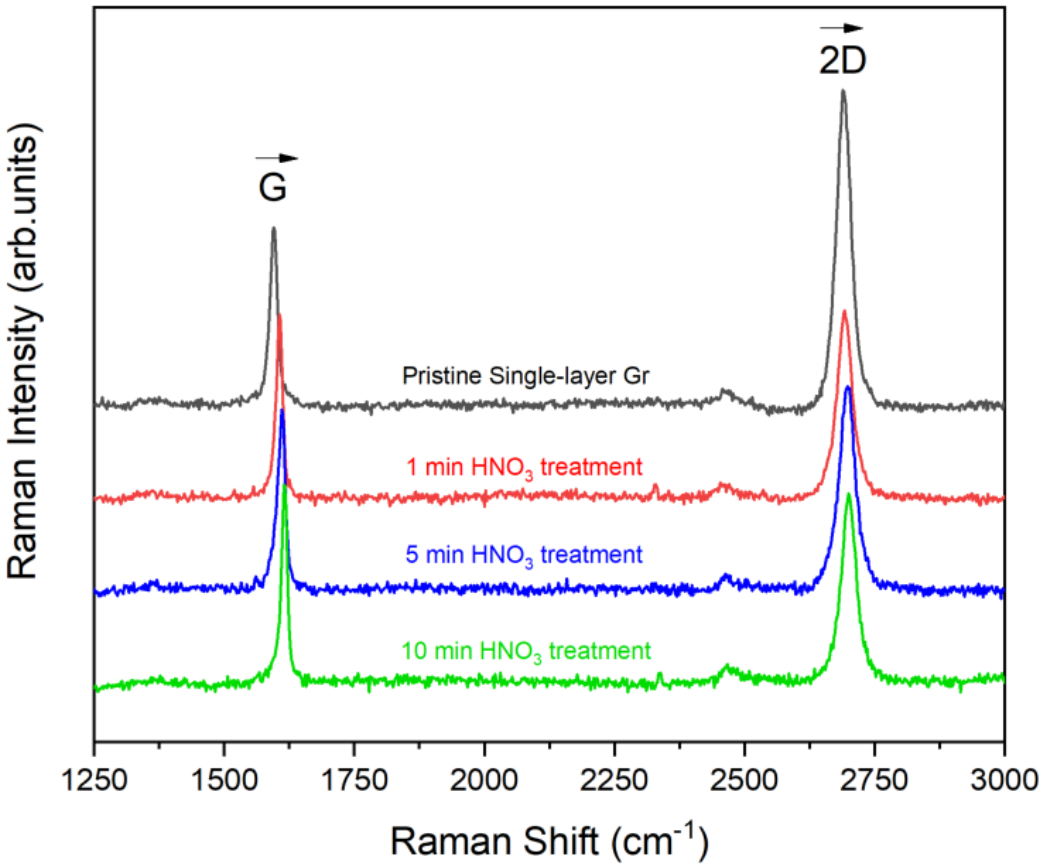

Figure 5.15. Raman spectra for p-doped SLG by HNO_3 for different durations.

The same doping process for different durations of 1 minute, 5 minutes, and 10 minutes is applied and the related Raman spectras are provided in Figure 5.16. The G peak and 2D peak positions are shifted to the right side as expected. The exact peak positions of the SLG and MLG doped with HNO_3 at different durations are listed in Table 5-1.

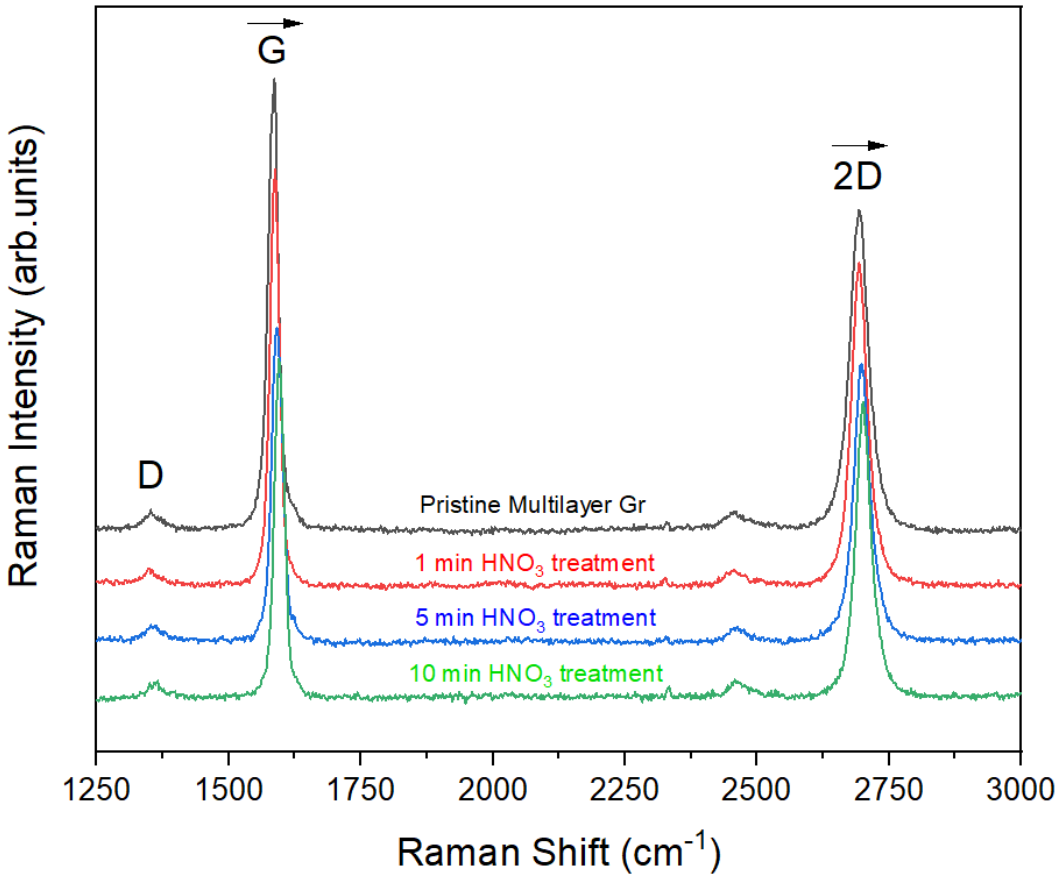

Figure 5.16. Raman Spectra for p-doped MLG by HNO_3 with different duration.

Table 5-1. G and 2D peak positions for SLG and MLG doped with HNO_3 at different durations.

	Pristine Gr	1 minute	5 minute	10 minute
Single-layer Graphene				
G peak (cm^{-1})	1585	1594	1600	1604
2D peak (cm^{-1})	2678	2682	2688	2690
Multilayer Graphene				
G peak (cm^{-1})	1586	1588	1590	1596
2D peak (cm^{-1})	2693	2694	2696	27

5.6 Graphene Transfer on Devices

Graphene transfer on textured silicon surfaces is much more difficult than transfer on a flat surface. Since graphene is a single-atom-thick layer it can crack and destroy easily. Accordingly, during the transfer on rough surfaces such as pyramids, it can be cracked easily. It becomes more important for MACE and fs direct laser texturing since they cause the formation of rough structures with sharp edges.

Photochemically etched silicon surfaces are advantageous in this case compared to the other two methods since it results in the formation of nanoholes instead of nanowires or nanopyramids. Accordingly, there are no sharp edges however the region which is not etched is not perfectly flat, but it is in form of porous silicon. Accordingly better graphene transferring results were achieved for surfaces etched by the photochemical etching method.

The other advantage of this process is that the graphene covers the surface and nanoholes. the graphene on the flat regions of the silicon forms the Gr/Si junction. On the other hand, the graphene which covers the cavities or nanoholes is called suspended graphene and has ultrahigh carrier mobility which is almost 2×10^5 cm^2/V_s and almost 20 times higher than the carrier mobility of the graphene which is bonded to the silicon. It means that this structure lets us combine the high mobility property of the suspended graphene and Si/graphene junction with the high light-trapping behavior of the nanoholes.

The single-layer and multilayer graphene can be transferred to the textured surfaces using the same recipe. The only difference is that, since the surface is rough, the silicon and graphene bonds are not as strong as the graphene bonds to flat silicon. Accordingly, after the final step of the hot acetone bath, the samples are cleaned by IPA as well. Then samples are again cleaned with hexane and let to dry at room temperature. It is because of the fact that to dry out the DI water a nitrogen flow should be used but since the bonds are not very strong the graphene layer can get apart from the silicon substrate. On the other hand, hexane evaporates easily at room temperature and there is no need for nitrogen flow.

Finally, graphene is transferred on photovoltaic devices with active area fully and partially etched by MACE, LIPSS, and PCE methods. The schematic and photograph of the final device are presented in Figure 5.17. Cell performance and I-V characteristics are measured by an AM1.5G calibrated class 3A flash solar simulator. The photograph of the measurement setup is presented in Figure 5.18. The measurement gives I-V curve, V_{oc}, I_{sc}, FF, and efficiency using the software which are presented and discussed in the next chapter.

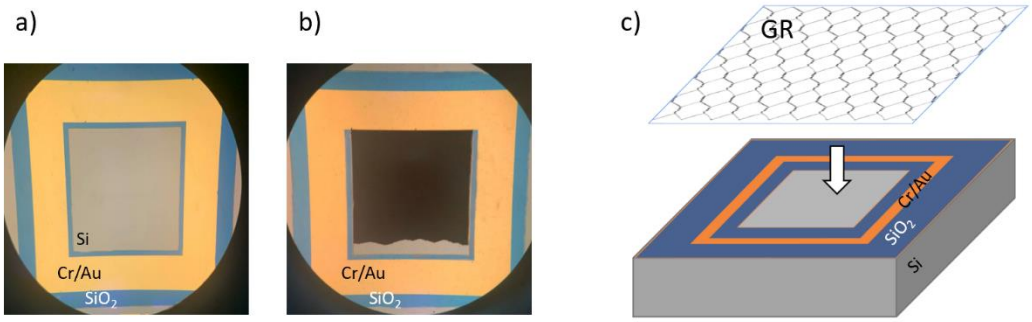

Figure 5.17. microscopic image of cells with a) flat and b) etched silicon surface. c) Schematic of Gr/Si Schottky junction.

Figure 5.18. Solar simulator measurement setup.

CHAPTER 6

RESULTS AND DISCUSSION

In this chapter, the performance of the Gr/Si Schottky solar cells with silicon surface etched by MACE, LIPSS, and PCE methods are presented and discussed. The effect of full and partial surface texturing with different etching methods on the performance of solar cells is studied and reported in detail.

6.1 J-V Measurement for Graphene/Silicon Schottky Solar Cells with a Flat Silicon Surface

The IV measurement results for devices with a flat active area without any etching, with single-layer and multilayer graphene transferred on it, are presented in Figure 6.1. There is not any current driven when there is not any graphene on the device which means that there is not any leakage in the device. After graphene is transferred and the Schottky junction is formed, the photovoltaic effect has been observed in the I-V curve. Both single-layer graphene and multilayer (3-5 layer) graphene are transferred to form Gr/Si Schottky solar cells. The V_{oc}, J_{sc}, FF, and η measured for samples with SLG are 0.360 V, 11.49 mA.cm^{-2}, 24.08%, and 1.00 % as well. For MLG, the values are all enhanced to 0.384 V, 15.86 mA.cm^{-2}, 25.67%, and efficiency is enhanced to 1.55%. The V_{oc} and J_{sc} are both increased as the layer number increases. The layer number can tune the work function of the graphene. In the case of Gr/n-Si the Schottky barrier increases which results in an enhancement in the V_{oc} value. Note that it decreases in the case of the Gr/p-Si junction. On the other hand, the series resistance decreases as the number of layers increases which increases J_{sc}. It means that the electron-hole carrier separation will be improved and as it is obvious from the J-V curves, the fill factor increases as well. The measured PCE values are listed in Table 6-1.

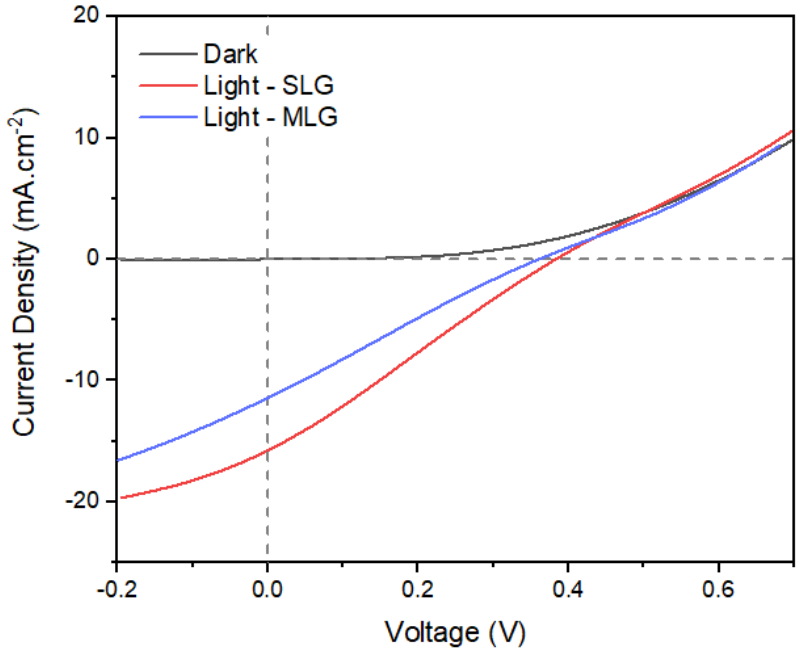

Figure 6.1. J-V measurement for Gr/Si Schottky solar cell with SLG and MLG on the untextured silicon surface.

Table 6-1. Corresponding PV characteristic parameters of the Gr/Si Schottky solar cells with the untextured surface.

	V_{oc} (V)	J_{sc} (mA.cm^{-2})	FF (%)	η (%)
SLG on flat Si surface	0.360	11.49	24.08	1.00
MLG on flat Si surface	0.384	15.86	25.67	1.55

6.2 J-V Measurement for Graphene/Silicon Schottky Solar Cells with a Textured Si Surface

As mentioned in chapter 4, there are various etching methods and various structures from micro to nano-scale which can be used for light trapping and absorption enhancement. Three different methods of MACE, LIPSS, and PCE were used for this study. Partially etched and fully etched surfaces were produced and devices were

fabricated. The patterns used for partial etching are provided in Figure 6.2. Pattern 4W and Pattern 9W are used for the partial etching process using the LIPSS and MACE methods. Both of the patterns result in the etching of 70% of the surface. Pattern 3 is used for the photochemical etching method. It results in ~56% surface coverage however the off-regions do not remain perfectly smooth in the case of the PCE method. Finally, single-layer and multilayer graphene were transferred to the cells to form Gr/Si Schottky junction solar cells. The prepared devices are named and coded as the chart presented in Figure 6.3.

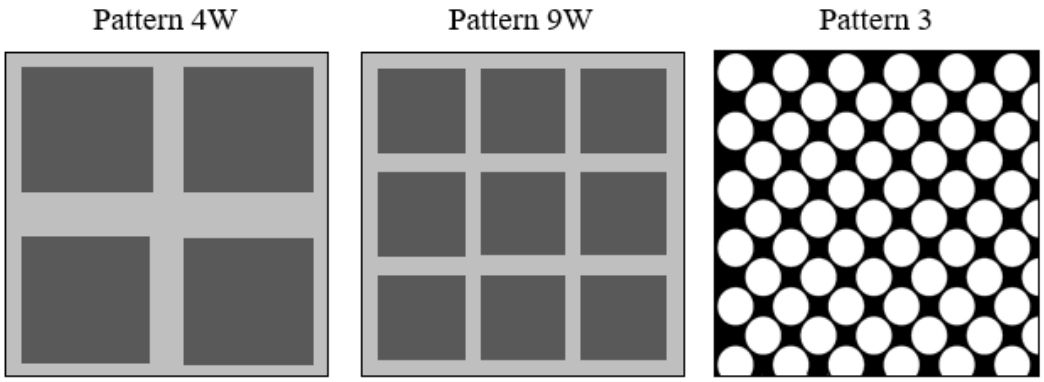

Figure 6.2. Patterns 4W and 9W were used for partial etching with MACE and LIPSS methods and pattern 3 is used for partial etching with the PCE method.

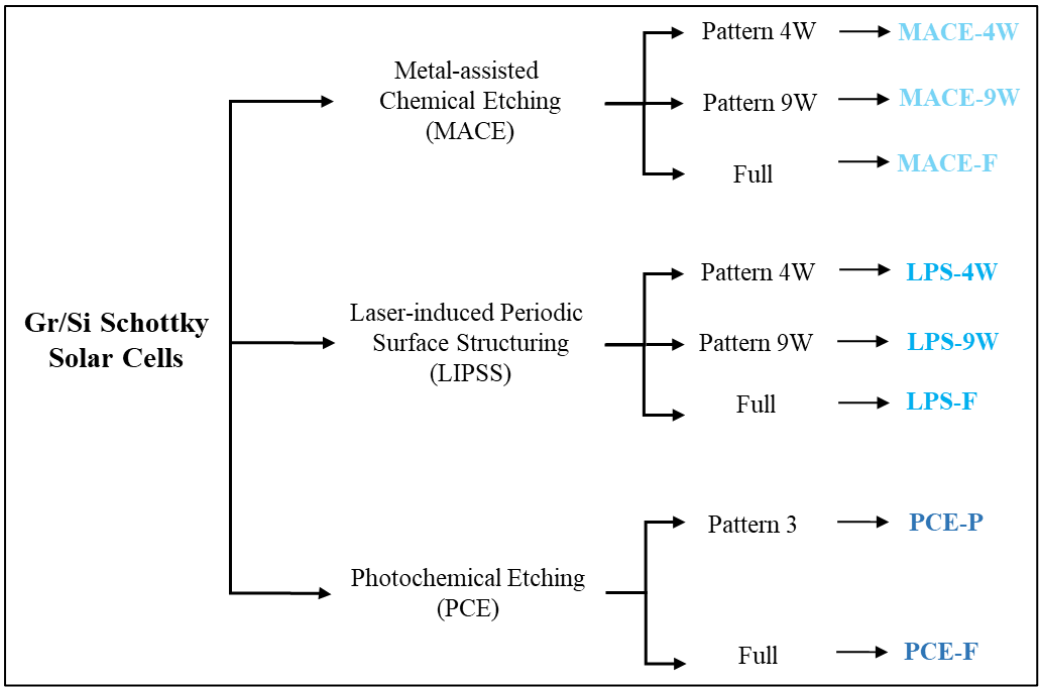

Figure 6.3. Coding chart for Prepared Gr/Si Schottky solar cells.

6.2.1 Silicon Surface Textured by LIPSS Method

Three different devices with silicon surfaces fully and partially etched by the LIPSS method were prepared and named LPS-4W, LPS-9W, and LPS-F as indicated in Figure 6.3. The optical photograph of the fabricated cells, the overall SEM images, and the magnified SEM images showing the side view and top view of the fabricated nanostructures on the silicon surface are presented in Figure 6.4. The single-layer and multilayer graphene is then transferred on the etched silicon surface.

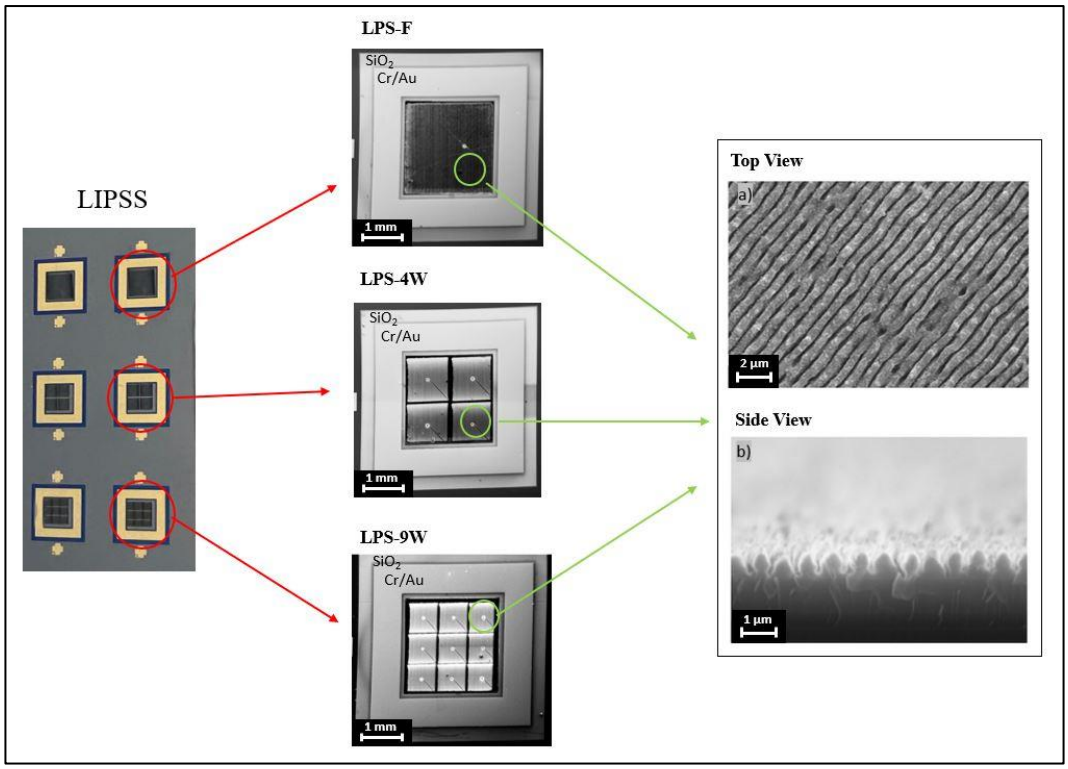

Figure 6.4. The optical photograph, SEM images, and magnified SEM images for LPS-4W, LPS-9W, and LPS-F Gr/Si Schottky solar cells.

6.2.1.1 Single-layer Graphene

The I-V measurements for samples named LPS-4W, LPS-9W, and LPS-F with single-layer graphene on it, are presented in Figure 6.5. The V_{oc}, J_{sc}, FF and η values for LPS-F are reported as 0.209 V, 5.15 mA.cm^{-2}, 27.78 %, and 0.30 %. For samples LPS-4W, LPS-9W with silicon surfaces partially etched by LIPSS, the cell performance is increased. According to the IV curve, the cell performance for the 9W pattern is higher compared to the 4W pattern. The V_{oc}, J_{sc}, FF, and η values are enhanced to 0.229 V, 6.76 mA.cm^{-2}, 28.04 %, and 0.42 % for LPS-4W and 0.254 V, 7.68 mA.cm^{-2}, 28.24 % and 0.55 % for LPS-9W, as well. According to the results, the performance of the devices is decreased compared to the untextured surfaces. It seems that it is because the silicon surface is seriously damaged by a high-power fs-laser. Accordingly, the junction quality degrades.

The better performance for 9W compared to 4W relates to the dimension of the etched area. The high aspect ratio and edges in the etched region cause higher defect density which results in electron recombination. In pattern 9W the electron produced in etched regions has to travel a shorter distance to reach the flat surface compared to Pattern 4W. It results in less electron recombination which improves the performance of the cell. The other factor which can affect the performance of the 9W pattern is the lower reflectance of the 9W pattern compared to the 4W pattern due to the light diffraction however, the difference in reflectance values of the two patterns is not significant. The corresponding PV characteristic parameters for each cell are listed in Table 6-2.

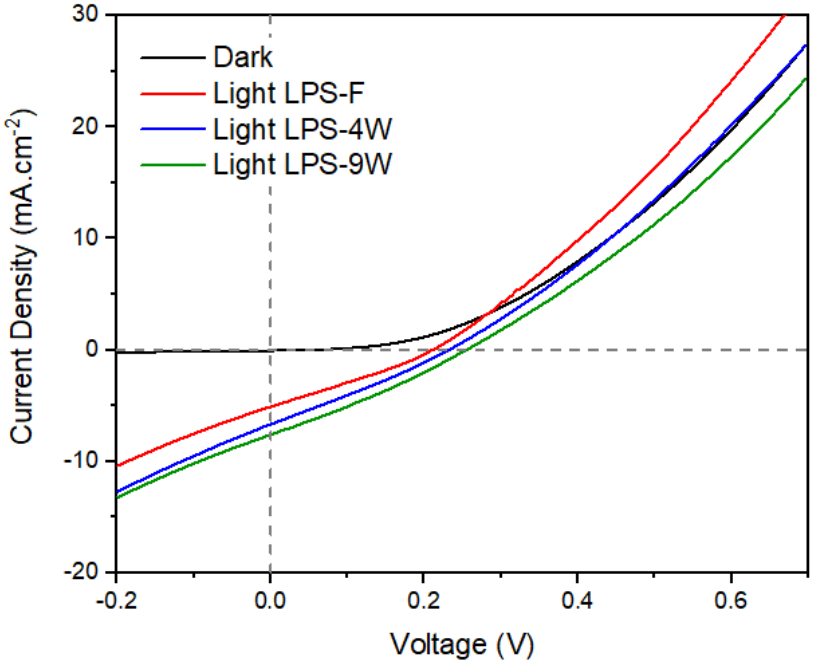

Figure 6.5. J-V measurement for Gr/Si Schottky solar cell with single-layer graphene and textured silicon surface by LIPSS method.

6.2.1.2 Multilayer Graphene

Multilayer graphene with 3-5 layers is then transferred on the same LPS-4W, LPS-9W, and LPS-F devices. The J-V measurements are presented in Figure 6.6. same performance enhancement as the samples with SLG on it is seen for multilayer

graphene too. The cell performance values of V_{oc} , J_{sc}, FF and η are reported as 0.224 V, 6.22 mA.cm^{-2}, 28.65 % and 0.40 % for LPS-F with multilayer graphene. All the values and the cell performance are enhanced compared to the cell with single-layer graphene on it as it was expected. This enhancement is due to the increase in the number of graphene layers. Same to the performance of the devices with single-layer graphene on them, the cell performance is enhanced for LPS-4W and LPS-9W with partially etched surfaces compared to LPS-F. The PV characteristic parameters are increased to 0. 249 V, 7.35 mA.cm^{-2}, 25.39 %, and 0.46 % for LPS-4W and later to 0.268 V, 7.92 mA.cm^{-2}, 26.93 %, and 0.57 % for LPS-9W. The highest performance is achieved for LPS-9W but even with multilayer graphene, the performance of the devices is still below the reference cell. The PV characteristic parameters measured for devices with multilayer graphene are presented in Table 6-2.

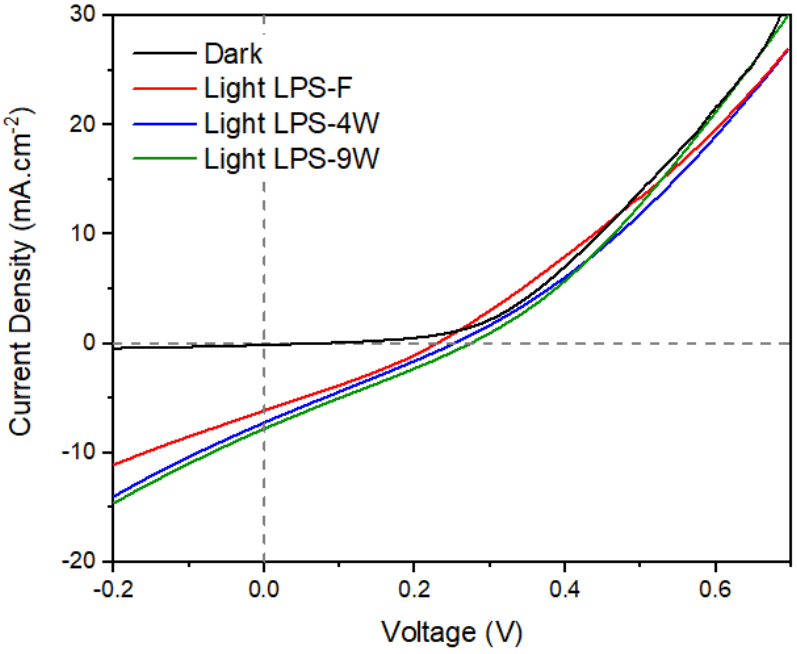

Figure 6.6. J-V measurement for Gr/Si Schottky solar cell with multilayer graphene and textured silicon surface by LIPSS method.

Table 6-2. Corresponding PV characteristic parameters of the Gr/Si Schottky solar cells with the silicon surface textured by LIPSS.

	V_{oc} (V)	J_{sc} (mA.cm^{-2})	FF (%)	η (%)
Single-layer Graphene				
LPS-F	0.209	5.15	27.78	0.30
LPS-4W	0.229	6.76	28.04	0.42
LPS-9W	0.254	7.68	28.24	0.55
Multilayer Graphene				
LPS-F	0.224	6.22	28.65	0.40
LPS-4W	0.249	7.35	25.39	0.46
LPS-9W	0.268	7.92	26.93	0.57

6.2.2 Silicon Surface Textured by MACE Method

Three samples with silicon surfaces partially and fully etched by the MACE method were prepared and named MACE-4W, MACE-9W, and MACE-F. 4W and 9W patterns were used to partially etch the silicon surface. The optical photograph, SEM images of the cells, and the magnified SEM images related to the fabricated silicon nanowires on the silicon surface of the Gr/Si Schottky solar cells are provided in Figure 6.7. SLG and MLG are transferred on the samples to form the Si/Gr Schottky junction.

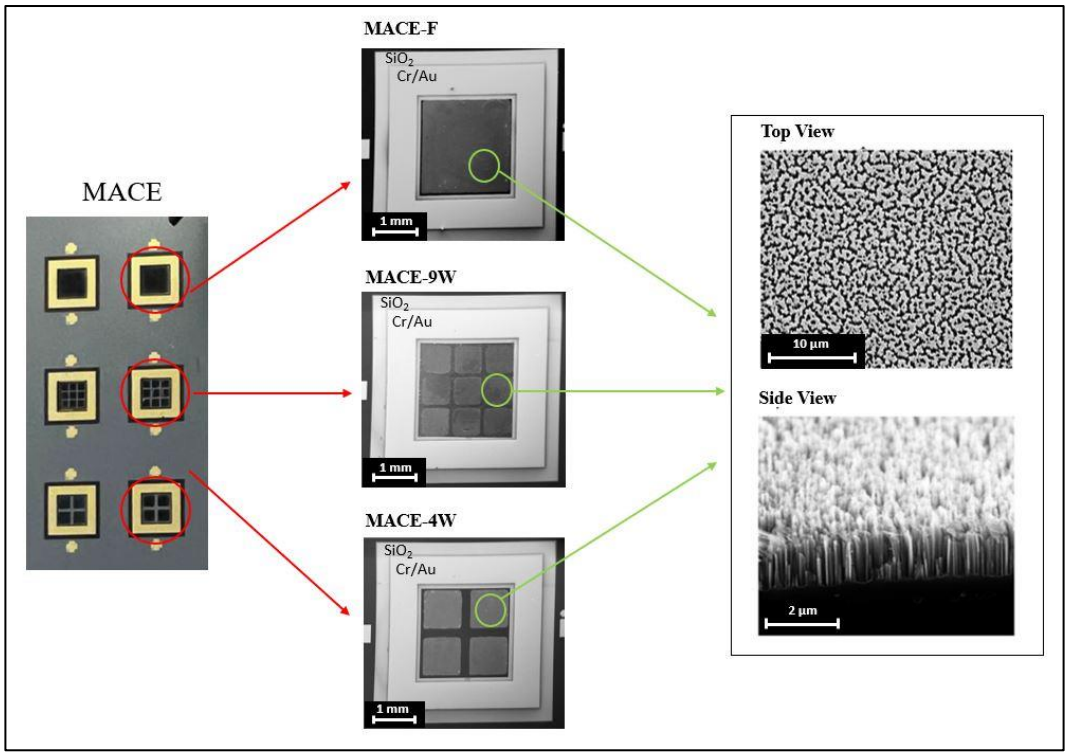

Figure 6.7. The optical photograph, SEM images, and magnified SEM images for MACE-4W, MACE-9W, and MACE-F Gr/Si Schottky Solar cells.

6.2.2.1 Single-layer Graphene

The J-V measurement results for samples MACE-F, MACE-4W, and MACE-9W with silicon surface etched by the MACE method and single-layer graphene on it are presented in Figure 6.9. The cell performance values of V_{oc} , J_{sc}, FF and η are reported as 0.328 V, 16.23 mA.cm^{-2}, 21.82 %, and 1.16 % for MACE-F. Same to the samples with silicon surfaces etched by LIPSS, the cell performance enhances for partially etched silicon surfaces. The PV characteristic parameters are reported as 0.339 V, 18.31 mA.cm^{-2}, 24.94 %, and 1.55 % for MACE-4W. The cell performance with pattern 9W is better compared to the cell etched with pattern 4W and reported as 0.354 V, 19.76 mA.cm^{-2}, 27.39 %, and 1.92 %. This enhancement is due to the decrease in the distance that the electron should travel to reach the flat surface and also the higher light absorption of MACE-9W same as samples textured by LIPSS.

Although, cell performance for devices with silicon surfaces etched by MACE is enhanced compared to samples with silicon surfaces etched by LIPSS which is because of the high damage of the fs-laser on silicon surfaces. The list of the PV characteristic parameters measured for MACE-F, MACE-4W, and MACE-9W with SLG on it is presented in Table 6-3.

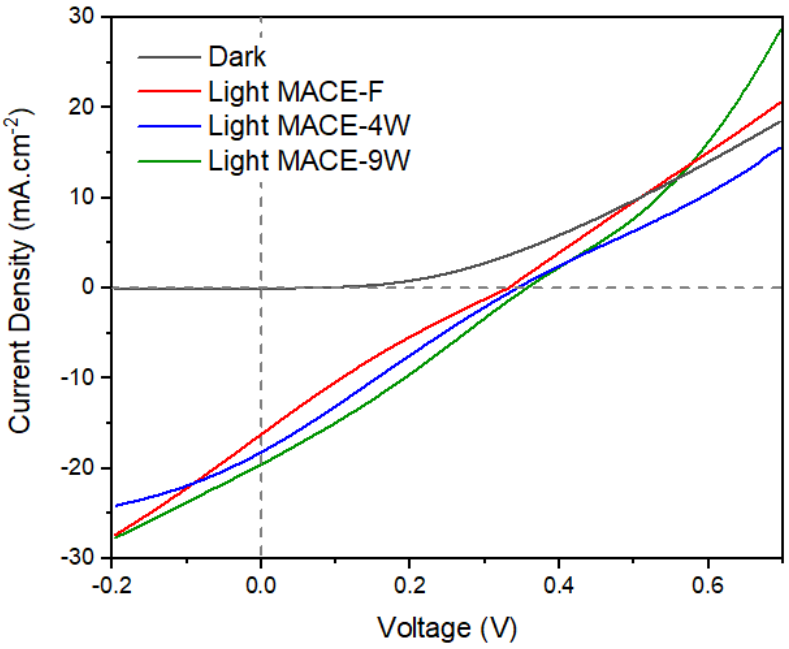

Figure 6.8. J-V measurement for Gr/Si Schottky solar cell with single-layer graphene and textured silicon surface by MACE method.

6.2.2.2 Multilayer Graphene

The J-V measurement results for multilayer graphene transferred on MACE-F, MACE-4W, and MACE-9W samples are presented in Figure 6.9. The cell performance for all three devices is enhanced compared to SLG as was expected. The PV characteristic parameters are listed in Table 6-3. The device performance values for MACE -F are increased to V_{oc} of 0.353 V, J_{sc} of 17.64 mA.cm^{-2}, FF 25.45% and η to 1.5 %. The performance of the cell is increased for MACE-4W and MACE-9W with partially etched surfaces. The highest performance was achieved

for MACE-9W with multilayer graphene on it with V_{oc} , J_{sc}, FF and η values reported as 0.374 V, 21.02 mA.cm^{-2}, 32.78 % and 2.58 %.

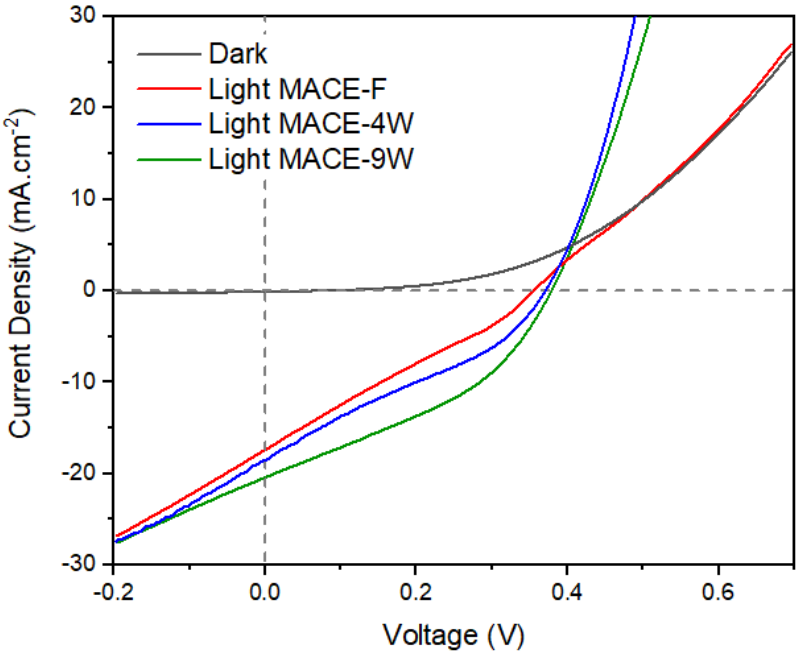

Figure 6.9. J-V measurement for Gr/Si Schottky solar cell with multilayer graphene and textured silicon surface by MACE method.

Table 6-3. Corresponding PV characteristic parameters of the Gr/Di Schottky solar cells with silicon surface textured by the MACE method.

	V_{oc} (V)	J_{sc} (mA.cm^{-2})	FF (%)	η (%)
Single-layer Graphene				
MACE-F	0.328	16.23	21.82	1.16
MACE -4W	0.339	18.31	24.94	1.55
MACE -9W	0.354	19.76	27.39	1.92
Multilayer Graphene				
MACE -F	0.353	17.64	25.45	1.59
MACE -4W	0.366	19.54	26.02	1.86
MACE -9W	0.374	21.02	32.78	2.58

6.2.3 Silicon Surface Textured by PCE Method

The pattern used for the photochemical etching method which was applied using a DMD was optimized in detail in chapter 3. The optimized pattern, named Pattern 3, and full etching were applied for cells with silicon surface textured by the photochemical etching method. Pattern 3 also results in the etching of almost 56 % of the surface. Single-layer and multilayer graphene is then transferred on top of them to form Si/Gr Schottky junction.

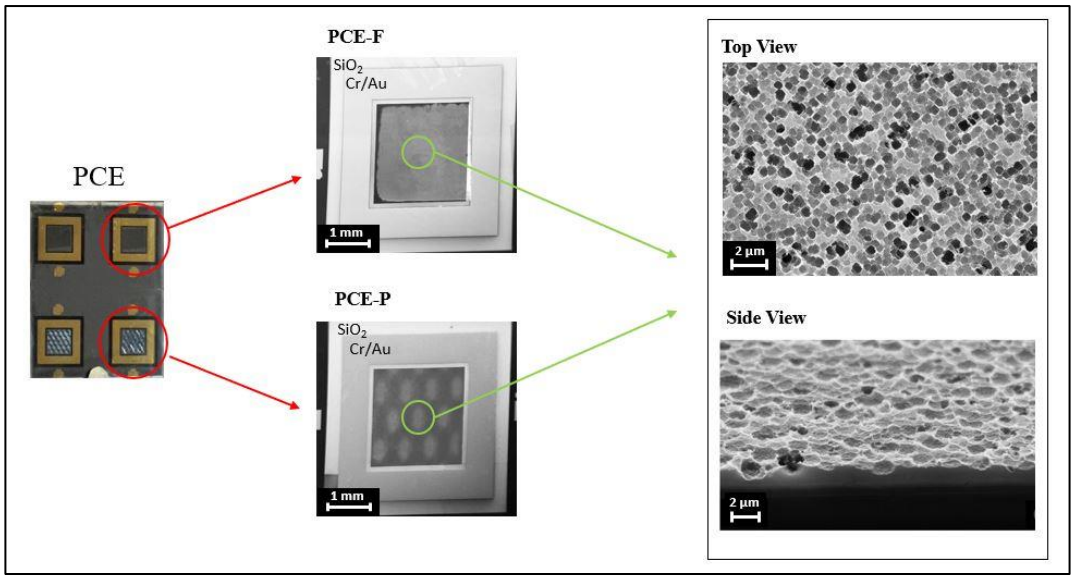

Figure 6.10. The optical photograph, SEM images, and magnified SEM images for PCE-F and PCE-P Gr/Si Schottky Solar cells.

6.2.3.1 Single-layer Graphene

The cells with silicon surface textured by the photochemical etching method are named PEC-F and PCE-P. The J-V curves achieved for cells with SLG transferred on the samples are presented in Figure 6.11. The V_{oc} and J_{sc} values for PEC-F are measured as 0.384 V and 22.31 $mA.cm^{-2}$, as well. The FF is calculated as 28.59 % and the efficiency is 1.79 %. The efficiency is increased compared to the flat active area due to the light trapping in nanoholes. The V_{oc} and J_{sc} values for PCE-P are measured as 0.365 V and 18.08 $mA.cm^{-2}$, as well. The FF and efficiency are calculated as 26.84 % and 1.79 %. Obviously, despite the cells textured with the other two methods reported in previous sections, the cell performance for the partially etched sample PCE-P is less than the fully etched sample PCE-F.

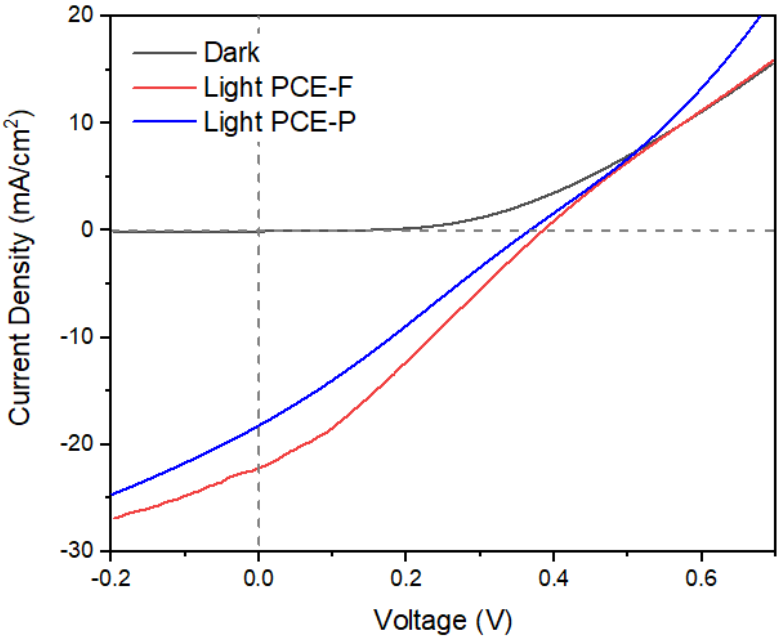

Figure 6.11. J-V measurement for Gr/Si Schottky solar cell with single-layer graphene and textured silicon surface by photochemical etching method.

6.2.3.2 Multilayer Graphene

The J-V curves for PCE-P and PCE-F with MLG are presented in Figure 6.12. Compared to the cell with SLG on it the V_{oc} and J_{sc} values for PCE-P with multilayer graphene on it are increased to 0.394 V and 26.24 mA.cm^{-2}. The FF is calculated as 34.21 % and the efficiency is 3.54%. Same to the devices with SLG, the performance of PCE-F with a fully etched silicon surface and MLG is better than the performance of the PCE-P. The V_{oc} is increased to 0.41 V and the J_{sc} value is enhanced to 28.90 mA.cm^{-2}. The FF and η are improved to 40.77% and 4.84%. The cell performance values for PCE-P and PCE-F with multilayer graphene are presented in Table 6-4. Accordingly the best results were achieved for PCE-P and PCE-F with MLG on it.

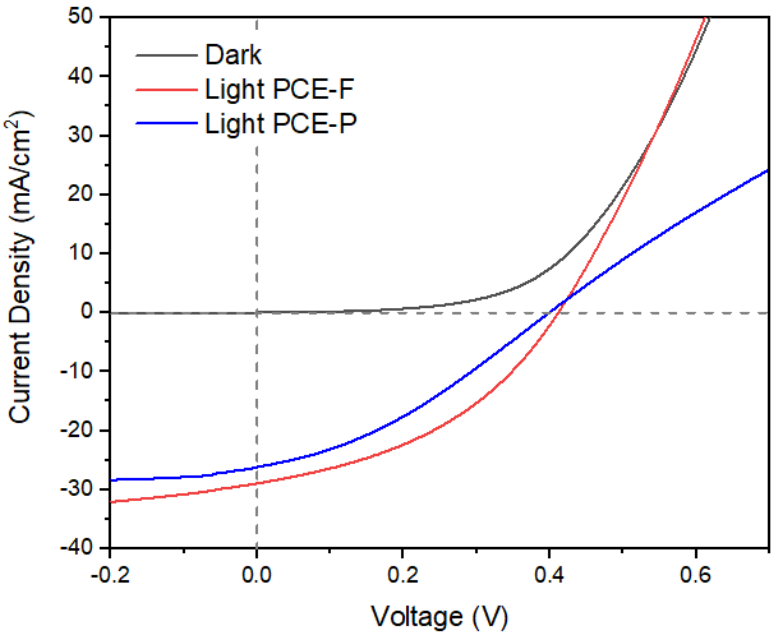

Figure 6.12. J-V measurement for Gr/Si Schottky solar cell with multilayer graphene and textured silicon surface by photochemical etching method.

Comparing the J-V results measured for cells with textured silicon surfaces by PCE, MACE and LIPSS, the PCE method results in better cell performance. Despite the samples etched by the MACE method, the device performance is enhanced for cells with fully etched silicon surfaces. It is due to the better material quality of silicon textured by PCE. It is concluded that in the case of PCE, the improvement in recombination doesn't overcome the optical loss for the partial etching case. The other reason for the enhanced performance of samples textured by PCE is the better quality of the graphene transferring. Since the topography of the nanostructures formed by PCE is in form of nanoholes the graphene transferred on these structures acts as suspended and bonded graphene which results in high electron mobility. Although the LIPSS and MACE methods result in the formation of rough and spiky nanostructures. The graphene transferred on such nanostructures with sharp edges cracks easily which results in the degradation of the graphene and junction quality.

Table 6-4. Corresponding PV characteristic parameters of the Gr/Si Schottky solar cells with silicon surface textured by photochemical etching method.

	V_{oc} (V)	J_{sc} (mA.cm^{-2})	FF (%)	η (%)
Single-layer Graphene				
PCE-F	0.384	22.31	28.59	2.45
PCE -P	0.365	18.08	26.84	1.79
Multilayer Graphene				
PCE -F	0.410	28.98	40.77	4.84
PCE -P	0.394	26.24	34.21	3.54

6.2.4 Graphene Doping

The PCE-F and PCE-P with multilayer graphene on it which have the highest performance were exposed to nitric acid fume for 5 mins at room temperature to p-dope the graphene. Figure 6.13 and Figure 6.14 refers to the J-V measurements for Gr/Si Schottky solar cells with partially and fully textured silicon surfaces by PCE method and doped MLG. The V_{oc} and J_{sc} are both increased for both PCE-P and PCE-F cells which is due to the enhancement in the working function of the graphene.

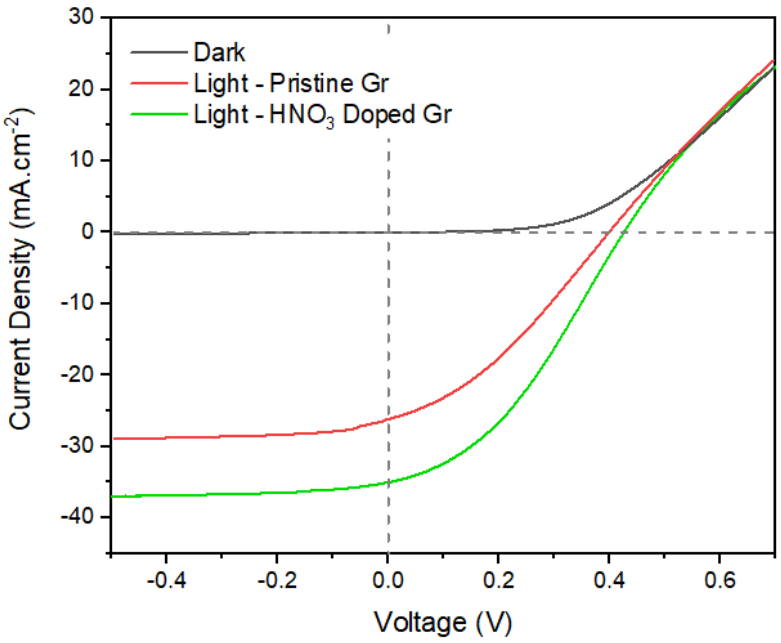

Figure 6.13. J-V measurement for PCE-P Gr/Si Schottky solar cell with multilayer graphene on it doped by HNO_3.

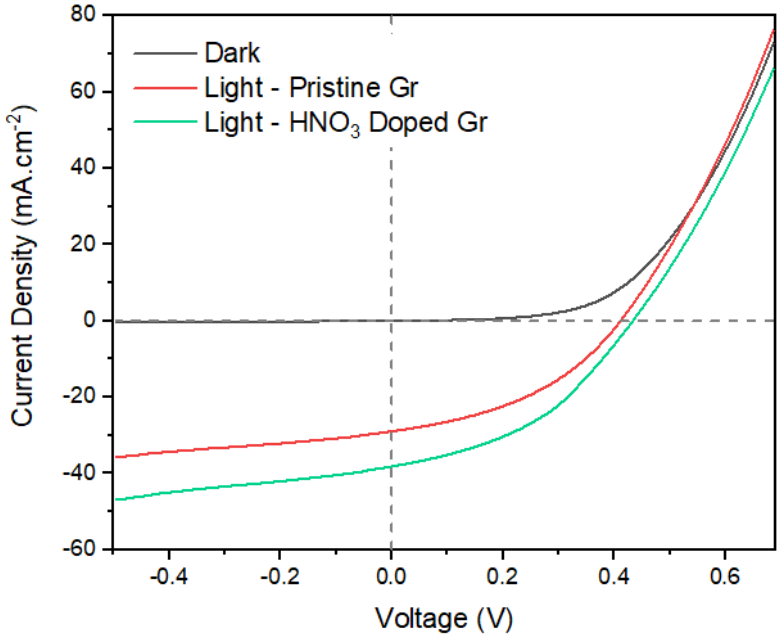

Figure 6.14. J-V measurement for PCE-F Gr/Si Schottky solar cell with multilayer graphene on it doped by HNO_3.

Table 6-5. Corresponding PV characteristic parameters of the Gr/Si Schottky solar cells with silicon surface textured by photochemical etching method and doped multilayer graphene with HNO_3.

	V_{oc} (V)	J_{sc} (mA.cm^{-2})	FF (%)	η (%)
Before Doping				
PCE-F	0.410	28.98	40.77	4.84
PCE -P	0.394	26.24	34.21	3.54
After Doping				
PCE -F	0.432	38.24	41.33	6.79
PCE -P	0.420	35.07	37.03	5.52

6.3 Conclusion

In this thesis, MACE, LIPSS, and PCE methods are compared in terms of efficacy in silicon surface texturing for graphene/silicon Schottky solar cell applications. The textured silicon surfaces facilitate improved light absorption by trapping. All these three techniques generate high aspect ratio structures leading to highly increased surface area which increases majority carrier recombination probability. To catch a trade-off between carrier mobility and light absorption the silicon surfaces were etched partially in specific patterns. Graphene was transferred on the silicon surface to form a Schottky junction. Gr/Si Schottky junction solar cells with an active area of 4 mm^2 were fabricated for comparing the effects of different texturing approaches and patterns.

The J-V measurements performed on different cells show that the cells with silicon surfaces textured by LIPSS have the lowest device performance. It is because LIPSS

damages the silicon surface which degrades the quality of the junction. Comparing the fully etched and partially etched (70% of surface coverage) silicon surfaces by the LIPSS method, the partially etched samples are found to have better performance. This supports the theory that the partial etching of the surface increases the carrier lifetime while it decreases the light absorption compared to the fully etched surfaces. For partial etching, two different patterns of 4-windows and 9-windows were used. Where the surface coverage for both of them was the same, the dimension of the etched region for the 9-windows is less than the etched region dimension for the 4-windows pattern. The better cell performance of the silicon surface partially etched with the 9-windows pattern is because of the decrease in carrier recombination since the carriers generated in etched regions have to travel a shorter distance to reach the flat surface. Although the 9-window pattern has higher absorption compared to the 4-windows pattern which results in higher J_{sc} too.

In the case of cells with silicon surfaces textured by the MACE method, the performance of the Gr/Si Schottky solar cell was found to be higher than that of the cells textured by LIPSS. I attribute this to the fact that the quality of silicon etched by MACE is better than the silicon etched by LIPSS. The performance of the cells etched partially is enhanced compared to the fully textured surfaces. Comparing the partially etched silicon surfaces, the silicon surface textured in the 9-windows pattern shows better performance same as the cells with silicon surface etched by LIPSS. It can be concluded that the overall performance of the MACE is better than the LIPSS. However, they show the same behavior for partially and fully textured cases.

The photochemical etching method was used as a third method in this thesis. An optical setup was constructed for this purpose in which a DMD was used to structure the light to texture the silicon surface in specific patterns. The idea of a partial etching by PCE method utilizing a DMD was introduced for the first time in this thesis. The J-V measurements of Gr/Si Schottky Junction solar cells with full and partial (56% surface coverage) structuring show an improved performance compared to the other two methods. But in contrast to the other two methods, the partial etching of the surface did not enhance the performance of the cell. My understanding is that this is

due to the lower carrier recombination rate for PCE compared to LIPSS and MACE. Partial etching decreases the light absorption and increases the carrier lifetime at the same time, however in the case of the photochemical etching method the increase in carrier lifetime does not overcome the decrease in light absorption.

In conclusion, according to the results, the photochemical etching method is found to overperform the LIPSS and MACE methods. Randomly and tightly located free-standing nanoholes can be fabricated by the PCE method, where LIPSS and MACE methods result in the formation of spiky nanostructures. From the Gr/Si Schottky junction point of view, the graphene transferred on harsh and spiky surfaces easily cracks and departs where the graphene that covers the nanoholes acts as suspended graphene with carrier mobility ten times higher than the graphene bonded on silicon. On the one hand, the silicon surface is highly damaged by LIPSS and MACE which degrade the quality of the remaining silicon compared to the PCE method. On the other hand, from the photon management point of view, the reflectance measurements show that the light trapping is highest with the MACE method, where it decreases further in PCE and LIPSS, in the given order. All these parameters together show that the photochemical method has the advantage of lower carrier recombination while its light management performance is in between the others two. Therefore, PCE is found to offer the highest overall performance by catching a trade-off between the optical and electrical properties of the textured silicon surface among the three structuring alternatives.

6.4 Future Prospects

The silicon surfaces textured by nanostructures with a high aspect ratio should be passivated to eliminate the dangling bonds that persist at the surfaces. The structures such as nanoholes, nanowires, and nanopyramids that are fabricated by PCE, MACE, and LIPSS methods in this thesis have a high aspect ratio at small dimensions which is a challenge to passivate. A conformal Al_2O_3 layer grown by ALD can be used as a passivation layer to enhance the performance of the Gr/Si Schottky solar cells

produced in this thesis. Note that such an Al_2O_3 layer is suggested also to act as an interlayer at the Gr/Si interface which alters the work function and improves the performance of the solar cell by helping the electron-hole separation [155].

Another issue with the PCE method presented in this thesis is that the laser beam can be expanded to a maximum dimension of 1 cm^2 which means the etch area is limited. To solve this problem an x-y translation stage can be integrated into the system to move the sample. Accordingly, it can be possible to texture larger areas by scanning the surface.

The partial texturing approach can, in principle, be fused with other light management ideas such as plasmonics. A stronger benefit from the synergy of the high aspect-ratio nanotexture and plasmonic nanostructures can be expected, subject to extensive optimization.

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CONFERENCES

- “Graphene/Silicon Schottky Solar Cells With Silicon Surface Textured By Photochemical Etching Method”, Poster presentation, 12th International Conference on Metamaterials, Photonic Crystals and Plasmonics, META 2022.
- “Graphene/Silicon Schottky Solar Cells With Silicon Surface Textured By Photochemical Etching Method”, Poster Presentation, 3rd International Conference on Photovoltaic Science and technologies, PVCON 2022.
- ”Silicon Surface Texturing By Photoelectrochemical Etching Method For Graphene/Silicon Schottky Diode Applications”, Poster Presentation, 22nd national workshop on optics, electro-optics, and photonics, Bilkent University 2021.
- “Single-Step Periodic Photoelectrochemical Texturing Of Silicon For Photovoltaics”, Poster Presentation, The 37th European Photovoltaic Solar Energy Conference and Exhibition, PVSEC 2020.
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PUBLICATIONS

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