A LOW-POWER SUCCESIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER INTEGRATED CIRCUIT FOR IMAGING SENSORS

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A LOW-POWER SUCCESIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER INTEGRATED CIRCUIT FOR IMAGING SENSORS

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ABSTRACT

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This thesis presents a low-power 14-bit successive approximation register analog-to-digital converter (ADC) designed in a CMOS process for the next-generation infrared imaging sensors and readout integrated circuits (ROIC). The ADC consists of 4 main components including input drivers, two digital-to-analog converter (DAC) integrated circuits, a comparator, and a SAR logic, all of which dissipate only 6.3 mW while operating at an 8 MS/s conversion rate.

The CMOS integrated circuit has novel architectures in all 4 main components to reduce the power consumption compared to the conventional architectures, while operating at a fast conversion rate for a typical 14-bit successive approximation register ADC. Firstly, the power consumption of the input buffers is decreased by using a charge sharing technique between the two DACs. The charge sharing technique reduces the output voltage swing and provides common-mode voltage at the output of the input buffers without any power consumption at the end of each conversion. As a result, the input buffers achieves 50% reduction in the power consumption. Secondly, each of the capacitive DACs has a split capacitor with 1

bridge capacitor architecture with a novel switching method, which not only decreases the power consumption by 25% compared to the state-of-art methods but also reduces the overall area by 75% compared to the conventional DACs with low common-mode voltage variation. In addition, two more optional novel switching method is proposed to decrease the power consumption further while achieving the same reduction in the overall area. Thirdly, there are two different comparator architecture in this thesis. The coarse comparator has a novel 2-level latch architecture including the pre-driver and strong-arm latch to reduce the power consumption of the strong-arm latch while achieving same noise level compared to the state-of-art comparators. The fine comparator has 2 pre-amplifier followed by a strong-arm latch with dynamic inverters to speed up the conversion cycle. Finally, a modified SAR logic provides less propagation time and minimizes the SAR conversion loop delay compared to the conventional design. A programmable digital controller and a bias generator provide flexible timing and biasing.

The proposed novel ADC architecture is designed and implemented in a standard 0.18 µm CMOS process, where it measures 0.5mmx1.3mm, operates from a 2.5V and 1.8 V supply voltage, and dissipates 6.3 mW at 8 MS/s conversion rate without the coarse comparator and 7.2 mW at 8 MS/s with the coarse comparator. The Walden figure of merit $(FoM)_W$ is 92.2 fJ/conv-step which is the lowest among all the ADCs with integrated input drivers for 14-bit resolution according to the best of our knowledge.

Keywords: Analog-To-Digital Converter Integrated Circuit, Digital-To-Analog Converter Integrated Circuit, Successive Approximation Register, Low-Power Comparator, Low-Power Input Driver

ÖZ

GÖRÜNTÜLEME SENSÖRLERİ İÇİN DÜŞÜK GÜÇLÜ ARDIŞIK YAKLAŞIKLAMA KAYDEDİCİLİ ANALOG-SAYISAL ÇEVİRİCİ TÜMLEŞİK DEVRESİ

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Bu tez, yeni nesil kızılötesi görüntüleme sensörleri ve tümleşik okuma devreleri için bir CMOS işleminde tasarlanmış düşük güçlü 14 bit ardışık yaklaşıklama kaydedicili (AYK) analog-sayısal çevirici (ASÇ) sunmaktadır. ASÇ, giriş sürücüleri, iki sayısal-analog çevirici (SAÇ) tümleşik devresi, bir karşılaştırıcı ve bir AYK mantığı dâhil olmak üzere 4 ana bileşenden oluşur ve bunların tümü 8 MS/s dönüştürme hızında çalışırken yalnızca 6,3 mW güç harcar. CMOS tümleşik devresi, geleneksel mimarilere kıyasla güç tüketimini azaltmak için 4 ana bileşenin tamamında yeni mimarilere sahiptir ve görüntüleme sensörleri için gerekli olan hızlı bir dönüşüm oranında çalışır. İlk olarak, sürücü devrelerinin güç tüketimini azaltmak için yeni bir yük paylaşım tekniği kullanılmıştır. Bu paylaşım tekniği giriş sürücülerinin çıkışlarının güç tüketimi olmaksızın orta voltaja çekilmesini sağlamaktadır. Böylece giriş sürücüleri raydan raya giriş voltajı sürmesine gerek kalmamıştır. İkinci olarak, kapasitif SAÇ'lerin her biri, yeni bir anahtarlama tekniğine sahip 1 zayıflatıcı kapasitör mimarisine sahip bir bölünmüş kapasitöre sahiptir; bu, son teknolojiye sahip yöntemlere kıyasla güç tüketimini yalnızca %25 oranında azaltmakla kalmaz, aynı zamanda toplam alanı da %75 oranında geleneksel mimarilere göre azaltır. Ek olarak, aynı toplam alanı elde ederken güç tüketimini daha da azaltmak için 2 yeni

anahtarlama tekniği daha önerilmiştir. Üçüncü olarak, karşılaştırıcı, sürücü devreleri ve güçlü kollu mandalın güç tüketimini azaltmak için güçlü kol mandalı dâhil olmak üzere yeni bir 2 seviyeli mandala sahiptir. Son olarak, değiştirilmiş bir AYK mantığı, daha az yayılma süresi sağlar ve geleneksel tasarımlara kıyasla AYK dönüşüm döngüsü gecikmesini en aza indirir. Programlanabilir bir sayısal devre ve bir kutuplama devresi, esnek zamanlama ve kutuplama sağlar. Önerilen yeni ASÇ mimarisi, standart 0.18 µm CMOS prosesinde tasarlanmış ve uygulanmış olup, burada 0.5mmx1.3mm ölçülerindedir, 2.5V, 1.8 V besleme voltajından çalışır ve 8 MS/s dönüşüm hızında hassas karşılaştırıcı yokken 6.3 mW harcar. Hassas karşılaştırıcı varken 7.2 mW güç harcar. Tasarlanan tümdevre 92.2 fJ/conv-step başarı performansı göstermektedir ve bizim bilgimize göre daha önce tasarlanmış olan 14 bit analog-sayısal çeviricilerin içinde en iyi değerdir.

Anahtar Kelimeler: Analog-Sayısal Çevirici, Sayısal-Analog Çevirici, Düşük Güçlü Karşılaştırıcı, Ardışık Yaklaşıklama Kaydedicili, Giriş Devresi

Dedication to my Parents

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ADC Analog-to-Digital Converter

DAC Digital-to-Analog Converter

SAR Successive Approximation Register

INL Integral Nonlinearity

DNL Differential Nonlinearity

FoM Figure of Merit

LSB Least Significant Bit

MSB Most Significant Bit

ENOB Effective Number of Bits

SNR Signal-to-Noise Ratio

THD Total Harmonic Distortion

SNDR Signal-to-Noise Distortion Ratio

SFDR Spurious Free Dynamic Range

CHAPTER 1

INTRODUCTION

Infrared imaging has been used in many applications such as health applications, defense industry, or space exploration researches. In 1963, the first image sensor was designed by Morrison [1]. Since 1963, the image sensors have rapidly growth and they can detect different electromagnetic spectrum ranging from UV to THz. As a result, today, the imaging sensors are used in daily life to find spots that cannot be easily observed, such as in automobiles, in cancer detection, in firefighting, or in building industry. As the semiconductor technology advances, the imaging sensors consist of millions of pixels with smaller pitch and operate at high frame rates. The image sensors are the main components of the infrared systems and each sensor consists of a detector converting the incoming radiation into electrical signals and a readout integrated circuit processing the electrical signals, which should be converted to the digital domain using an on-chip or off-chip analog-to-digital converter (ADC) to obtain images and videos. In the first infrared imaging systems, off-chip ADCs and the off-the-shelf components were used, resulting in high-cost bulky systems to perform imaging due to extra buffers, regulators, and their relative components which are not only increase the cost of the system and the area of the devices, but also degrade the overall performance of the system. As a result, in the past, the imaging systems were very expensive and only used in military systems or space systems. Today, the major research in the imaging area is to decrease the cost of the overall system by using on-chip analog-to-digital converter integrated circuits (ADC) and embedded processors while achieving same or better performance.

The on-chip ADCs can decrease the cost of the overall imaging system and improve the performance of the system. As the number of components increase, the imaging system becomes more complex and the performance is degraded by various peripheral components such as high speed logics and communication devices. Thus, in recent years, in order to improve the performance of the imaging systems researchers have been focused on imaging sensors with on-chip ADCs [2-3]. Each ADC used in the imaging systems has different architecture to optimize the performance of the system and it should be designed according to the system specifications such conversion rate, frame rate, noise linearity, power budget, and technology node. For instance, for low-speed and high resolution imaging systems that require beyond 14 bits, $\Delta\sum$ ADCs are used to perform imaging while, for high-speed imaging sensors, pipelined ADCs and Successive Approximation Register ADCs are employed. Unfortunately, these traditional ADC architectures do not meet multiple demands. For example, the pipelined ADC architectures are very fast, while their power consumption is very high. Custom and image sensor specific ADCs are required to achieve better performance compared to the conventional ADC architectures while demanding low-power consumption.

Low-power is one of the most important design specification in the imaging sensors, since they operate with battery-powered systems. As a result, the power consumption of the components such as ADCs in the image sensor should be as low as possible. For the imaging sensors, the ADCs can operate at tens of MS/s with 12 b to 14 b resolution, so that, the most commonly used architecture is pipeline ADC due to its power efficiency [4-6]. However, in recent years, the SAR ADC has become an alternative to the pipeline ADCs. The conventional pipeline ADCs use high-precision op-amps, complex switched capacitor circuits, and flash comparators which lead to large power consumption. Recent studies [7-10] has optimized the power consumption of the pipeline ADCs, but the figure of merit (FoM) is still in the range of hundreds of fj/conv-step, while today the state-of-the-art figure of merit reaches below 1 fj/conv-step. In addition, the pipeline ADCs cannot be easily scaled down to advanced technology nodes due to complex analog circuits. In contrast, the

SAR ADCs have simple analog circuits such as comparator and DAC. Thus, the SAR ADC can be easily scaled down to novel technology nodes, resulting a lower FoM. Today, the FoM is calculated for only the core circuit and does not include the significant components such as input drivers and reference drivers. Although, the FoM can be very low for the core ADC circuit, the input drivers and reference drivers can require large power consumptions to drive the internal circuits and DACs. In addition, recent studies [11-13] have only focused on decreasing the power consumption of the core circuit. As a result, when these state-of-art ADCs are combined with commercial input drivers, the power budget abruptly increases and they cannot be integrated into battery-powered systems. In addition to power consumption, external buffers and related passive components require large PCB area, which leads to bulky systems. In order to optimize the PCB area and power consumption, the input driver and core circuit should be designed together.

This thesis presents the design and implementation of a SAR ADC for 640x512 photon-based imaging systems. The proposed ADC is comprised of a DAC architecture with a novel switching scheme, a low-power fine comparator which consists of 2 pre-amplifier followed by a strong-arm latch with dynamic inverters, and a low-power input drive circuitry to reduce the overall power consumption. A modified SAR Logic decreases the conversion delay while a programmable digital controller and bias generator are used to provide required signals and bias currents.

Table 1.1 shows the preliminary design specifications of the SAR ADC. The power consumption of the SAR ADC should be as low as possible while operating at 8Ms/s, since image sensors work with battery-power systems. The DNL should be less than 1 LSB, to ensure that there is no missing codes. The noise of the ADC should be kept at low levels to differentiate very small temperature difference. The proposed SAR ADC has a fully differential architecture to achieve 14-bit resolution and suppress the common-mode variations. The core of the proposed SAR ADC consists of DACs array, a fine comparator, and a SAR logic for implementing the successive approximation algorithm. The prototype SAR ADC has a highly programmable digital controller, and bias generator. The programmable digital controller offers

flexibility for the required digital signals and it interfaces with an external processor by using a simple 4-wire SPI while the programmable bias generator is used to provide different bias currents and voltages to the main components of the SAR ADC. In the bias generator, a supply, and temperature independent bandgap circuit is employed in order to generate a reference voltage. In addition, an offset cancellation scheme is used in order to remove the offset voltage error of the fine comparator caused by the mismatches and environmental errors.

Table 1-1 Preliminary design specifications of the SAR ADC

Resolution	14-bit
Input Voltage Range	3.6V
Conversion Rate	8 Ms/s
INL	<±1 LSB
DNL	<±1 LSB
Power Consumption (mW)	<6.3mW at 2.5V/1.8V
Noise (LSB, where 1 LSB is 219 μV)	< 0.5LSB

This chapter introduces the basic information about the readout integrated circuits, analog-to digital conversion, and the motivation, as well as research objectives and organization of this study. First, Section 1.1 overviews of the imaging sensor readout integrated circuits, performs a comparison between an analog ROIC and digital ROIC, and discusses the detailed information about the systems requirements for the image sensors. Section 1.2, explains the principles of data conversion, and Section 1.3 analyzes the important performance parameters of the ADCs. Section 1.4 investigates different ADC architectures, while Section 1.5 defines the figure-of-merit for ADCs. Section 1.6 expresses the motivation and the goals of this thesis. Finally, Section 1.7 states the research objectives and thesis organization.

1.1 Overview of Imaging Sensor Readout Integrated Circuit

The readout integrated circuit is an integrated circuit that is used for processing the electrical signals coming from the detector which converts the incoming radiation into electrical signal. Depending on the type of the detector, there are different types of pixel circuits that interface with the detector. Each pixel circuit integrates the charges coming from the detector in a different way. After the integration, the input signal is amplified and multiplexed to sequentially read the pixel data.

Figure 1.1 shows the block diagram of a typical ROIC with an analog output. The ROIC consists of a pixel array, an analog column readout, column decoder, row decoder, bias generator, digital controller, and video buffers. The pixel array interfaces with the detector and integrates the electrical signals coming from the detector. The integrated pixel signals are then amplified, multiplexed, and buffered. The analog video outputs are sequentially sent to external electronics through several video channels. The bias generator generates the required voltages and currents, while the digital controller generates the required timing signals and interface with the external processors. Row and column decoder selects the specific row and column of the pixel array in a specific manner. The video buffers drive the analog output to be processed by the external electronics which includes ADC, regulators, and relative passive components.

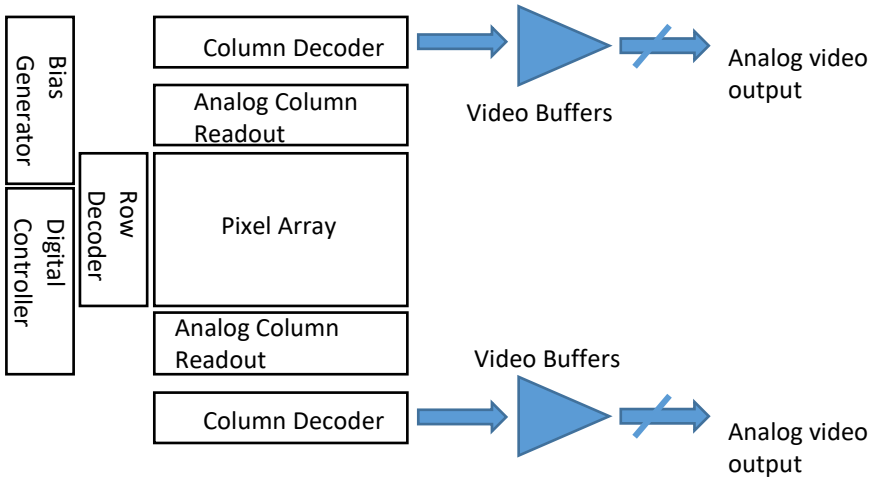


Figure 1-1: The block diagram of a typical ROIC with analog output.

Early infrared systems used off-the-shelf components such as ADCs, buffers, filters, or regulators. These components together with the passive components require large PCB area, increase the cost of the overall system, and raise temperature of the imaging sensor. The cost and size of the system can be reduced as more components such as buffers and ADCs are integrated into the ROICs. Integration of these external components into the single chip also eliminates the external components that increase the temperature. As a result, the digital ROICs have important advantages over analog ROICs and today, most of the sensor systems use digital ROICs in order to achieve state-of-the art performance.

1.1.1 General ADC Specifications for the Image Sensors

The general ADC specifications are determined according to the specific image sensor. Each image sensor has different readout topology and different array format with different operation rate. For instance, for the image sensors with high conversion rate, pipeline ADCs or SAR ADCs can be used to perform conversion. On the other hand, for the image sensors with low conversion rate and small array format, Δ-∑ ADCs and SAR ADCs can be employed. The general specifications for the ADCs can be listed as below;

1.1.1.1 Area

Area is an important specification especially for the ROICs with small array format. These types of ROICs require small silicon area. In order to achieve small silicon area, standalone ADCs cannot be used. Instead of using standalone ADCs, column ADCs such as single slope ADCs are used to perform conversion. Although, the single slope ADCs are a good choice for area limited sensors, the power consumption and linearity of each ADC can cause problems. Since each column has its own ADCs, the power consumption of each ADC should be very low to achieve a low overall power consumption. In addition, due to the process variations, each column ADC has different variations which can lead linearity problems between the columns. In order to tackle these problems, in recent years, SAR ADCs and their hybrid versions have been investigated to replace the single slope. The image sensors that do not has an area limitation can use a standalone ADC next to the image sensor. As a result, both analog, and digital outputs are available. In these image sensors, pipeline, SAR or, Δ-$\sum$ ADCs can be used to perform conversion.

1.1.1.2 Sampling Frequency

The speed of the image sensor is another specification for the ADCs. Some image sensors require fast conversion rates to obtain image or video. In order to achieve fast conversion rate, some topologies such as, Δ-$\sum$ ADCs or single-slope ADCs cannot be used. Instead of using these ADC architectures, SAR ADCs and pipeline ADCs are preferred.

1.1.1.3 Effective Number of Bits

The image sensors are low-noise sensors, which can detect small temperature differences between the object and they require high resolution ADCs to present the image or video in high quality. The effective number of bits is defined as the true resolution of an ADC after the measurements.

1.1.1.4 Integral Non-Linearity (INL)

The integral non-linearity is the deviation of the actual output from the ideal output for a certain code. The static non-linearity errors can be removed by using two-point non-uniformity corrections. In many imaging sensors, non-uniformity corrections are performed to increase the quality of the image and video.

1.1.1.5 Differential Non-Linearity (DNL)

The differential nonlinearity is defined as the deviation of the step size of the ADC from its ideal value. The step size depends on the analog input voltage range and the resolution of the ADC and it directly affects the image quality. Large deviations in the step size degrades the image quality and lead to loss of information. The loss of information can cause image artifacts which can be observed easily. In order to reduce image artifacts, the DNL should be kept below 1 LSB voltage.

1.1.1.6 Fixed Pattern Noise (FPN)

Due to the offsets coming from the detector and readout integrated circuits, a fixed pattern noise leads to image artifacts. The fixed pattern noise can be eliminated by using correction algorithms such as 1-point and 2–point corrections. Offset cancellation or double correlation sampling in the column can also be used to remove the fixed pattern noise.

1.2 Principles of Data Conversion

A signal is a function which carries an information such as voltage, current, or temperature in either analog domain, or digital domain. Analog signals are continuous signals, whereas the digital signals are discrete signals. Figure 1.2 plots an analog signal that has a 3.3V amplitude. The amplitude of the analog signal changes over time and the signal is continuous in time.

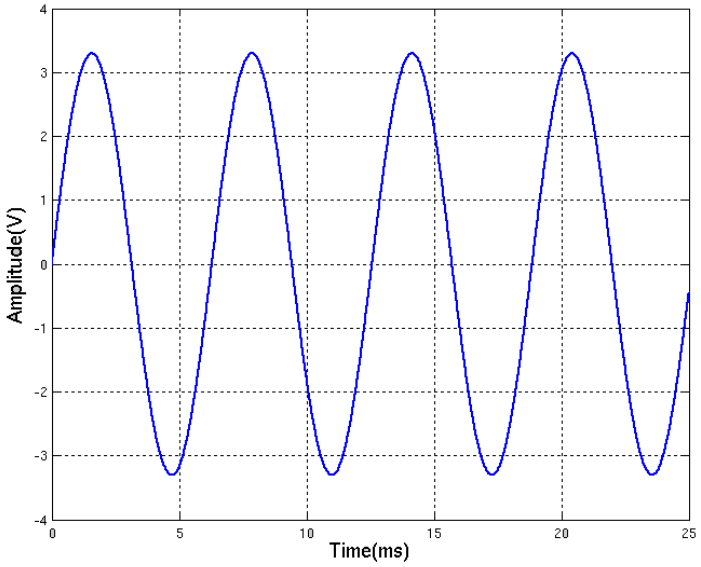


Figure 1-2. An analog signal that has a 3.3V amplitude.

Figure 1.3 illustrates a discrete digital signal that can be used in any systems. The digital signals are discrete signals and they can be represented in different forms. In general, the binary systems represent the digital signals.

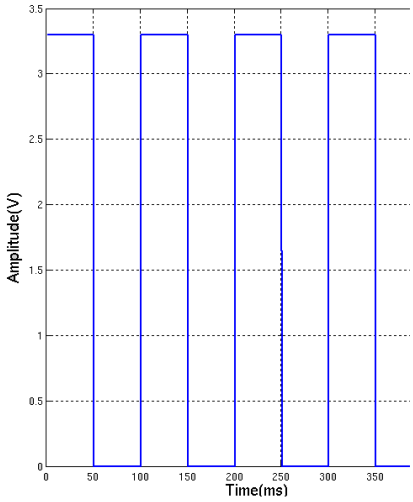


Figure 1-3. Discrete digital signal.

In order to use analog and digital signals in the desired domains, signal processing must be used. The type of the signal processing depends on the application area and it can be applied in either analog domain, or digital domain. In certain application areas, either an analog signal processing, or a digital signal processing is available. Thus, a data conversion between the analog domain and digital domain must be performed. The data conversion is performed by analog-to-digital converter integrated circuits and digital-to-analog converter integrated circuits. Figure 1.4 shows a block diagram of a simple ADC which is called as Nyquist ADC and it has a sampling frequency that is twice as the input signal bandwidth. In order to prevent aliasing from the high frequency components, the Nyquist ADC uses an anti-aliasing filters which can filter out the signals out of the frequency of interest bandwidth.

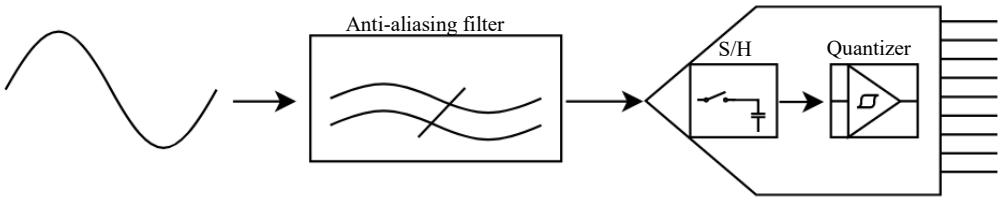


Figure 1-4. A block diagram of a simple ADC.

Following the filtering, the analog signal is sampled on a capacitor and the quantizer performs the comparison to generate the digital representation of the input voltage. On the other hand, the digital-to-analog converters (DACs) have a digital input and generate an output voltage according to the given digital input. Due to the fact that digital signals are discrete signals, the output of the DAC does not exactly correspond to its analog signal. As a result of this difference between the analog input and digital representation, an error called as quantization error occurs during the conversion. Figure 1.5 show an example of 3-bit DAC and its quantization error.

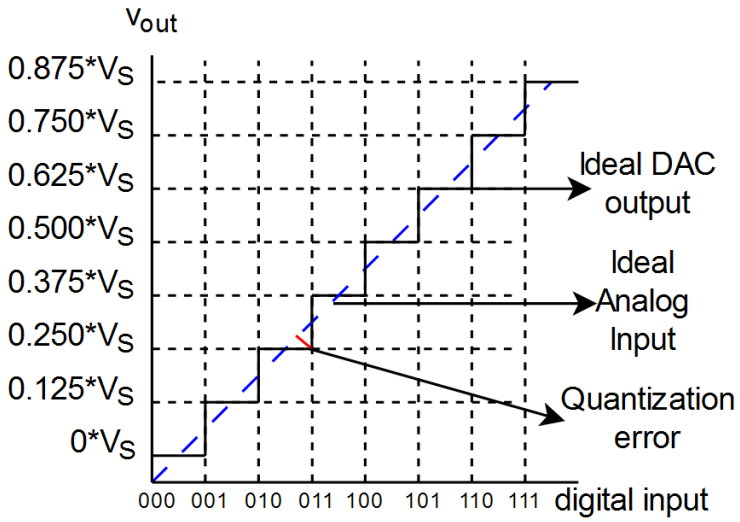


Figure 1-5. An example of 3-bit DAC and its quantization error.

The quantization error is the difference between the ideal analog signal and DAC output voltage. This error is a result of the conversion and it can become smoother by using a low-pass filter [14]. In ideal systems, the quantization error should be between ± 0.5 LSB voltages. In order to reduce the effect of the quantization error, the resolution can be increased.

1.2.1 Sampling

Sampling is a process that takes samples from the input signal in a given time interval. It can be performed in either analog domain or digital domain and it is very important for the ADCs. Figure 1.6 plots a simple sampling process with a sampling time interval Ts.

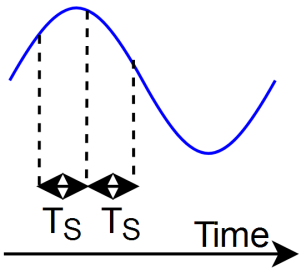


Figure 1-6. A simple sampling process with a sampling time interval Ts.

The sampling time is the required time interval between the two consecutive inputs. The inverse of this time interval is called as sampling frequency and it is abbreviated as f_s. If the upper limit of the input signal frequency is defined as f_B, in order to hinder the aliasing, the minimum sampling frequency should be written as

$$f_s \geq 2 \cdot f_B \tag{1.2.1}$$

Note that the sampling process is a repetitive process. It means that, the analog input signal in the frequency domain repeats periodically after sampling. Figure 1.7 illustrates an example of sampling of an arbitrary input signal [14].

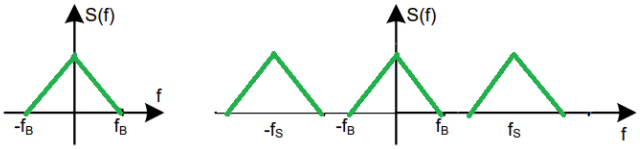


Figure 1-7. An example of sampling of an arbitrary input signal [15].

After the sampling, a number of copies of the input signal is reconstructed in the frequency domain. Under normal conditions, the fundamental signal component around the zero is the desired component that is used for further processing. In order to remove the other signals at the out of bands, a filter called as anti-aliasing can be used to filter out the high frequency components called as aliasing [16].

1.2.2 Quantization

Following the sampling process in ADCs, a quantization is performed to generate the digital representation of the analog input signal. The quantization can be performed with a number of levels that is specified according the applications. The number of levels determine the resolution of the ADC. Some applications such as infrared imaging require high resolution images, or videos. In order to achieve high resolution, the number of quantization levels must be increased.

1.2.2.1 ADC Resolution

The resolution of the ADC is defined by the number of quantization levels. It represents the distance between each consecutive quantization level. The quantization level is represented by Δ and the corresponding ADC resolution can be written as

$$\Delta = \frac{V_{FS}}{2^N - 1} \tag{1.2.2}$$

where V_{FS} represents the full scale analog input signal, and N defines the number of quantization levels.

1.3 ADC performance metrics

The ADC consists of static and dynamic performance metrics. Static parameters evaluate the signal at very low frequencies while the dynamic parameters analyses the signal at high frequencies.

1.3.1 Static Parameters

Static parameters include offset error, gain error, differential nonlinearity, and integral nonlinearity. Figure 1.8 plots the ADC transfer characteristics.

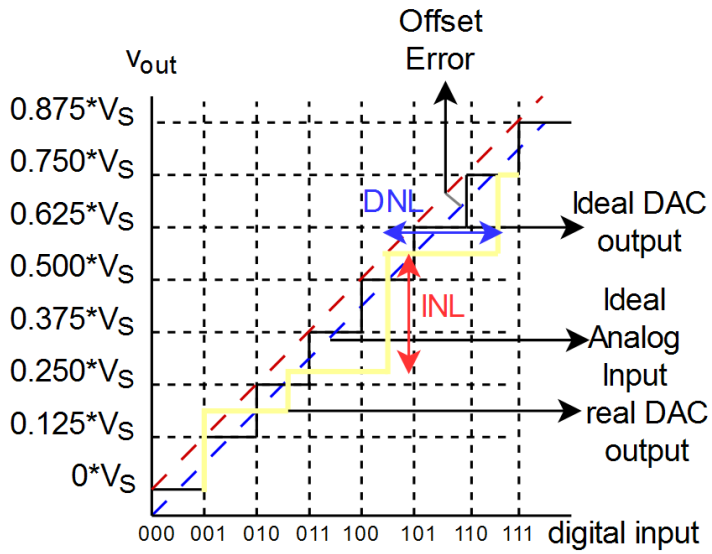


Figure 1-8. The ADC transfer characteristics.

- **Offset Error:** The offset error is the difference between the actual output and the ideal output. The environmental variations and process variations cause static offset errors. In order to cancel these offset errors, a reference conversion is performed. From the reference conversion, the offset error is extracted. For the remaining conversions, the extracted offset can be subtracted from the next outputs to cancel the variation.

- **Gain Error:** The gain error is defined as the difference between the slope of the actual output and the slope of the ideal output.
- **Differential Nonlinearity (DNL):** The differential nonlinearity is defined as the deviation of the step size of the ADC from its ideal value. The step size depends on the analog input voltage range and the resolution of the ADC. The DNL can be reduced by using calibrations.
- **Integral Nonlinearity (INL):** The integral nonlinearity is the deviation of the output from the line that connects the end points of the output curve [17]. The measurement is performed from the center of the step size. The INL can also be reduced by using calibrations that reduce the mismatch effects coming from the process variations.

1.3.2 Dynamic Parameters

Dynamic parameters are the parameters of the ADCs at the high frequencies while at low frequencies, the static errors are dominant and the effect of the dynamic errors can be negligible. Today, in many systems, the conversion rate is very high and the dynamic parameters should be carefully examined to analyze the performance of the ADCs. The most common dynamic parameters are signal to noise ratio (SNR), total harmonic distortion (THD), signal to noise, and distortion ratio (SNDR), and spurious free dynamic range (SFDR).

- **Signal to Noise Ratio (SNR):** The signal to noise ratio is the ratio of the power of the input signals to the power of the output noise.
- **Total Harmonic Distortion (THD):** The total harmonic distortion is the ratio of the sum of the powers of the harmonic frequency components to the power of the fundamental frequency.
- **Signal to Noise and Distortion Ratio (SNDR):** The signal to noise and distortion ratio is the ratio of the RMS value of the signal amplitude to the RMS value of all the spectral components.

- **Spurious Free Dynamic Range (SFDR):** It is the ratio of the power of the input signal to the power of the largest undesired signal [18].

1.4 ADC ARCHITECTURES

Today, there are different types of ADC architectures in the literature. Most common architectures are pipelined ADCs, ΔΣ ADCs, SAR ADCs, flash, and subranging ADCs. Figure 1.9 shows the common ADC architectures and their application areas with the resolution and sampling rate.

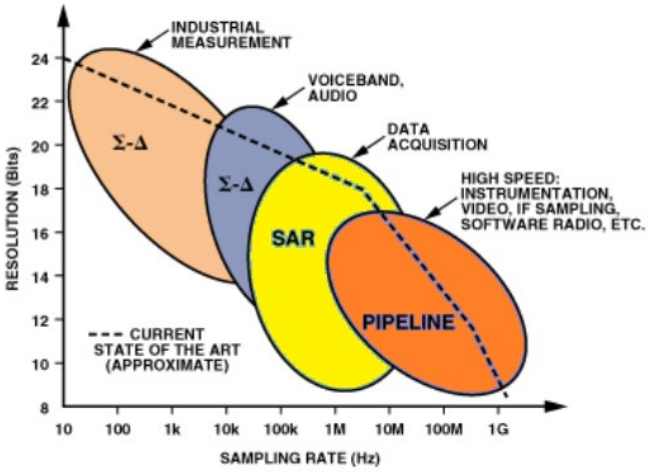


Figure 1-9. The common ADC architectures and their application areas with the resolution and sampling rate [19].

The ΔΣ ADCs are used for high resolution applications at low frequencies while SAR ADCs are preferred for medium resolution and medium speed applications. The pipeline ADCs are used for high speed applications which require low to high resolution. In general, The ADCs are mainly categorized into 2 main subgroup which are Nyquist rate ADCs and oversampled ADCs. The Nyquist ADCs operate at the frequencies which dictate that the sampling frequency should be 2 times larger than the input signal frequency in order to avoid aliasing. On the other hand, in the oversampled ADCs, the sampling frequency is much larger than the input signals, since the input is oversampled. For this reason, the maximum achievable bandwidth

is limited in oversampled ADCs compared to the Nyquist ADCs. This thesis focuses on Nyquist ADCs, so that in the next sections, the Nyquist ADCs will be investigated.

1.4.1 Flash ADC

Flash ADCs are used in radar signal processing, satellite communication, or high-speed data acquisition systems. It consists of parallel single channel ADCs. Each single channel ADC performs a single conversion at the same time, resulting in a high bandwidth. Figure 1.10 shows an example of flash ADC architecture. The flash ADC architecture includes multiple comparators followed by a thermometer decoder and binary encoder. It contains 4 single channel ADC in which an analog input signal is compared with a reference voltage that is generated from a resistive division.

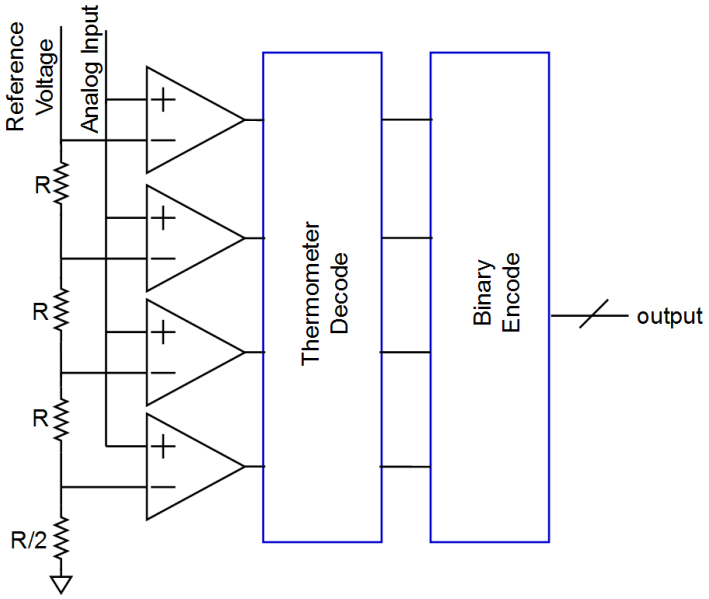


Figure 1-10. An example of flash ADC architecture [20].

While achieving high speed, flash ADCs suffer from high power consumption and large silicon area. Since for each bit, a comparator is required, for an N-bit flash ADC, 2^N-1 comparators and reference voltages are required to perform the conversion. Thus, the ADC occupies large silicon area and requires large power

consumption. As a result, the flash ADCs are used for low resolution applications which require up to 8-bits.

1.4.2 Subranging ADC

Subranging ADCs are an alternative to the flash ADCs. Since, the flash ADCs cannot be used for high resolution applications, a modified version of the flash ADCs called as subranging ADCs are used. Subranging ADCs are based on two-step conversion techniques to reduce the circuit complexity and power consumption of the overall circuit. Figure 1.11 shows a 2-step subranging ADC architecture.

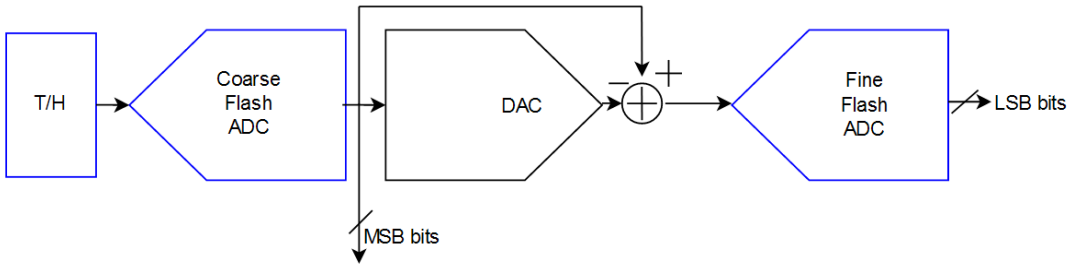


Figure 1-11. 2-step subranging ADC architecture [21]

The input voltage is tracked and hold by the sampling circuit and the first comparison is performed by a coarse flash ADC. From the first a few comparisons, the MSB bits are determined. Following the comparisons, these MSB bits are fed into a DAC to generate a voltage. This voltage is then subtracted from the input voltage to generate a residue voltage. The residue voltage is used by the fine flash ADC to perform LSB comparisons which determines the LSB bits. At the end of the conversion, a digital logic combines the LSB bits, and MSB bits and produces an output.

The subranging ADCs uses 2 different comparator per comparison. As a result, compared to the flash ADCs, the subranging ADCs require $2^{N/2}$-1 comparators, reduce the overall silicon area and power consumption of the ADC. On the other

hand, the subranging ADCs require extra time to obtain the same conversion rate compared to the flash ADCs, since the flash ADCs complete the conversion at one cycle, while the subranging ADCs need extra cycle to complete the conversion. In addition, subranging ADCs have low SNR values which limits the application area. In order to overcome this limitation, pipeline ADCs are preferred.

1.4.3 Pipeline ADC

The pipeline ADC achieves high resolution and it is commonly used for the sampling rates around 100MS/s. The pipeline ADC consists of multiple stage subranging ADCs which are called as odd stages and even stages. The odd stages operate at one cycle, while the even stages perform the conversion on the next cycle. Figure 1.12 shows an example of 12-bit pipeline ADC architecture.

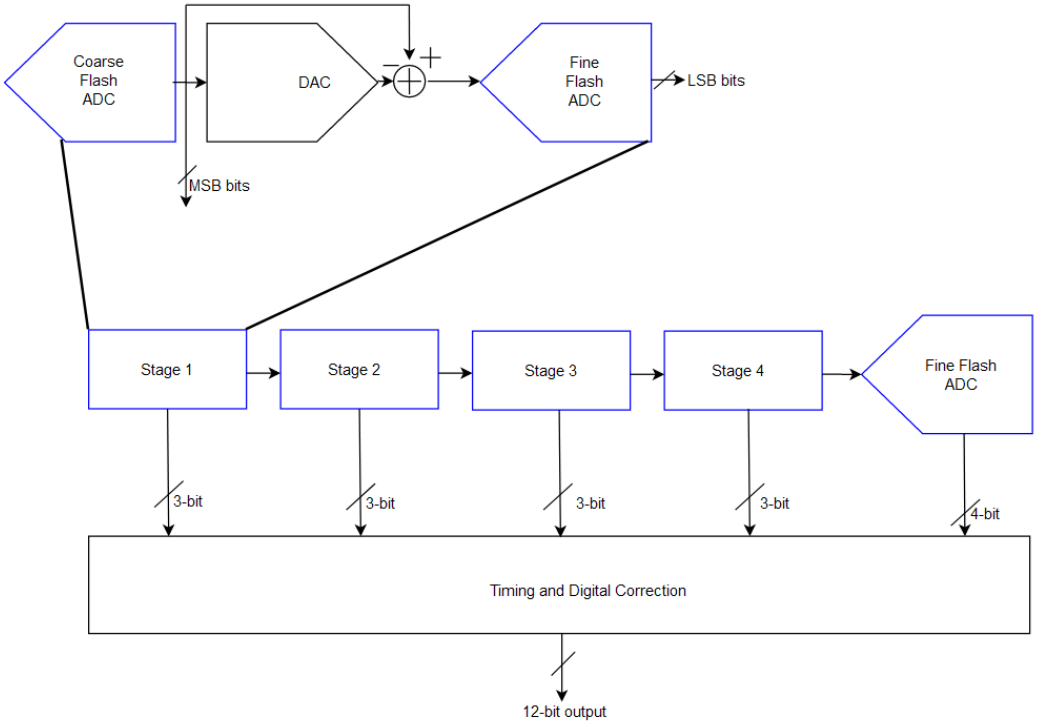


Figure 1-12. An example of 12-bit pipeline ADC architecture [22]

Each stage consists of a 1-stage subranging ADC. In the first stage, the subranging ADC determines the MSB bits which are used to generate a residue voltage. In order to achieve a high resolution, the residue voltage must be very precise which require precise DAC and amplifier to avoid static linearity problems. The second stage performs the comparison according to the generated residue voltage and the conversion continues until the last 4-bits. The last 4-bits are determined by a small flash ADC.

1.4.4 Successive Approximation Register (SAR) ADC

SAR ADCs are based on the binary search algorithm. Figure 1.13 shows a simple SAR ADC architecture. It consists of a sample and hold circuit, a DAC, a comparator, and a SAR Logic that implements the binary search algorithm. The SAR ADCs have less components compared to the previous architectures and they are suitable for applications that require medium resolution and medium speed. The main component of the SAR ADCs is the DAC array, which consists of a capacitor array, or a resistive array. It generates an output voltage, which is used for comparison with the input voltage. According to the result of this comparison, the DAC array is updated and another comparison is performed. For an N-bit ADC, N conversion step is required which is the drawback of this type of the ADCs, since the operation speed must be larger than the conversion rate of the ADC.

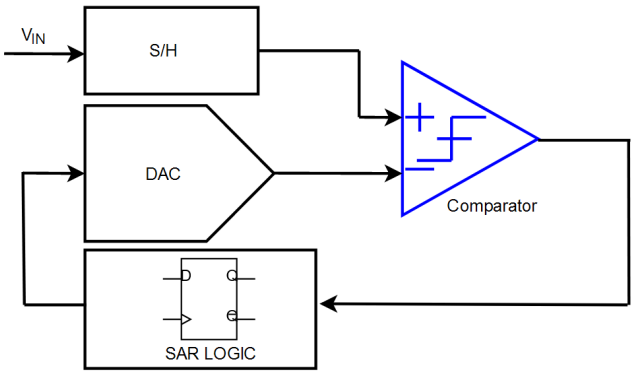


Figure 1-13. A simple SAR ADC architecture [23].

1.5 ADC Figure-of-Merit

In order to compare the performance of the various ADCs in terms of resolution, speed, power, consumption, and bandwidth, a standard figure-of-merit is used. There are 2 different types of figure-of-merit to make a fair comparison between different ADC architectures.

1.5.1 Walden Figure-of-Merit (FoMw)

The Walden figure-of-merit [24] ADCs is defined as

$$FoM_W = \frac{P_{ADC}}{\min(2 \cdot BW_{IN}, f_S) \cdot 2^{ENOB}} \quad (Joule\ per\ conv-step) \tag{1.5.1}$$

where P_{ADC} represents the power consumption of the ADC, ENOB is the effective number of bits of the ADC, BW_{IN} is the input signal bandwidth in which the ENOB is reduced by LSB/2 from its value at DC input [25], and f_S is the sampling frequency of the converter.

1.5.2 Schreier Figure-of-Merit (FoMs)

The Schreier Figure-of-Merit [25] is expressed as

$$FoM_s = SNR + 10\ log_{10}\left(\frac{BW_{IN}}{P_{ADC}}\right)\ (dB) \tag{1.5.2}$$

where P_{ADC} represents the power consumption of the ADC and SNR is the Signal-to-Noise ratio in dB. Due to the fact that Schreier Figure-of-Merit does not contain the distortion information, instead of using SNR, Signal-to-Noise and Distortion ratio is used. Equation (1.5.2) becomes

$$FoM_s = SNDR + 10\ log_{10}\left(\frac{BW_{IN}}{P_{ADC}}\right)\ (dB) \tag{1.5.3}$$

where BW_{IN} represents the input bandwidth where SNDR is reduced by 3 dB from its value at DC input [26].

In this thesis, Walden Figure-of-Merit is used to plot the SNR of the proposed ADC and calculate the ENOB from the SNR. Figure 1.14 shows the Walden FoM for the state-of-the-art ADCs up to 2022 [27]. For the Walden Figure-of-Merit, a low value is good in terms of energy efficiency and today the state-of-the-art FoM achieves under 1fjc/conv-step. The reduction in the FoM implies a great reduction in the power consumption.

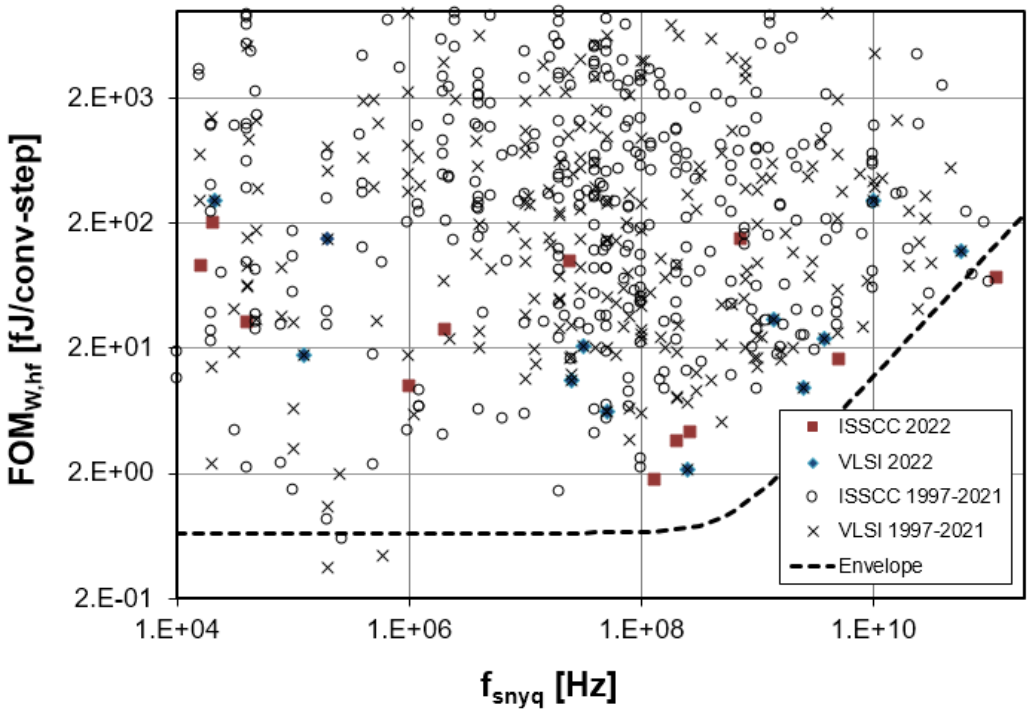


Figure 1-14. The Walden FoM for the state-of-the-art ADCs up to 2022[27].

The first great reduction in the FoM occurred in 2008 presented by Elzakker et al [28-29]. Later, energy efficient switching schemes for the DACs [30-31], low thermal noise dynamic comparators [32-33], and asynchronous SAR Logic are studied to reduce the power consumption of the overall ADC. As a result, over the past years, the $(FoM)_W$ is improved by 30-40 % and the overall energy consumption of the SAR ADCs is dramatically reduced [34-35]. However, these improvements do not include the input buffers. For this reason, it is important to address the low-power design techniques not only for the ADC core circuit but also for the input buffers to realize the overall system.

1.6 Motivation of the Thesis

The motivation of this thesis is to design and implement a low-power ADC that integrates the input drivers into the chip and it proposes novel solutions to decrease power consumption and reduce the size of the imaging system. Firstly, the standalone commercial ADCs require buffers, capacitors, resistors, or special regulators and they require large PCB area to implement the circuits. The large PCB area increases the overall cost of the system, since it contains different types of components. Secondly, these different components lead to additional noise, because the analog traces can overlap with other analog and digital signals. This additional noise can be a serious problem for the imaging sensors and the performance of the imaging systems can be seriously degraded by this additional noise. Thirdly, the imaging systems are based on the battery-powered systems and they consist of commercial components in which do not meet the power specifications. Input buffers are the main components that generally lead large power dissipation. Therefore, this thesis addresses to 3 main problems which are stated above.

In this thesis, a 14-bit ADC with integrated input buffers is designed to perform the data conversion. Novel low-power design techniques are proposed to decrease the overall power consumption of the ADC to the state-of-the art levels while achieving same performance. Compared to the existing 14-bit ADC architectures with the input buffers, the proposed ADC has the lowest FoM according to the best of our knowledge.

1.7 Research Objectives and Thesis Organization

The main goal of this thesis is to develop a low-power and high resolution ADC for a wide range of imaging sensors. The proposed ADC should occupy small silicon area and it has 14-bit resolution while operating at 8 MS/s conversion rate. Since, conventional SAR ADCs dissipate large power with conventional input buffers, this thesis focuses on an optimized ADC architecture with the input buffers. The detailed objectives, and novelties of this study is given below.

1. To design a DAC architecture with a modified switching scheme which requires less energy dissipation, reduces number of switches, and reduces required silicon area.
2. To design a novel low-power coarse comparator that includes 2-level charge re-cycle latch.
3. To implement a modified input sampling technique to reduce the power consumption of the input buffers.
4. To design a modified SAR Logic to minimize propagation delay.

Chapter 2 overviews the SAR ADC. Chapter 3 discusses the digital-to-analog-converter (DAC) and gives details about the DAC switching schemes. Chapter 4 concentrates on the design of the comparator. Chapter 5 focuses on the analog-front circuitry of the SAR ADCs. Chapter 6 presents the SAR Logic and peripheral circuits. Chapter 7 shows the top level integration of the proposed SAR ADC and Chapter 8 concludes the thesis and gives information about the future work.

CHAPTER 2

AN OVERVIEW OF SUCCESSIVE APPROXIMATION REGISTER ADC

The Successive Approximation Register (SAR) ADC is based on a Successive Approximation Register (SAR) algorithm which resembles to the solution of a Bachet's Weight mathematical Problem in the 1500s [36]. The Backet's Weight Problem sought the minimum number of weights for measuring an unknown weight. The solution was proposed by [37] which states that by using an integer number of weights such as 1, 2, 4, 8, 16, and 32 pounds and adding or removing these known weights while placing the unknown weight on the other side, the unknown weight can be measured. This solution is very similar to the binary search algorithm which is the fundamental of the SAR algorithm. The binary search algorithm basically aims to find a desired value in an array. The algorithm basically starts with the comparison of the desired value with the middle element in an array. According to the result of this comparison, the one half of the array is eliminated and the other half is used for further comparisons. The comparisons continue until finding the desired value. The desired value can be a number, a weight or a digital code in the ADCs. The Successive Approximation Register algorithm is based on finding the desired digital code which corresponds to certain analog quantity. The Bell Laboratories first introduced the Successive Approximation for the Pulse Code Modulation (PCM) system in order to describe a sequential coder [38]. Later on, the same concept was used in a 5-bit ADC which was implemented with the vacuum tubes [39]. The SAR ADC with a DAC was first presented in a patent [40] which was the fundamental architecture of the first commercial SAR ADC known as DATRAC [41]. The designed SAR ADC required a large power consumption in the order of hundred watts and the prices was $8000. After the first designs, the architecture of the SAR ADC has evolved and today, the architecture becomes the most commonly used ADC architecture used in the systems.

This chapter gives an overview of a SAR ADC. Section 2.1 explains the basic operation principle of a simple single ended N-bit SAR ADC. Section 2.2 analyzes the analog blocks such as the DAC array and comparator for discussing the effects of the non-idealities. Section 2.3 emphasis on the SAR logic and Section 2.4 explains the SAR loop delay that determines the conversion speed. Finally, Section 2.5 discusses the methods used in this study for achieving a high resolution SAR ADC. Section 2.6 summarizes the chapter.

2.1 Introduction

The core of the SAR ADC consists of a DAC array, a comparator, and a SAR logic. Figure 2.1 shows a simple single-ended N-bit SAR ADC architecture with its main components.

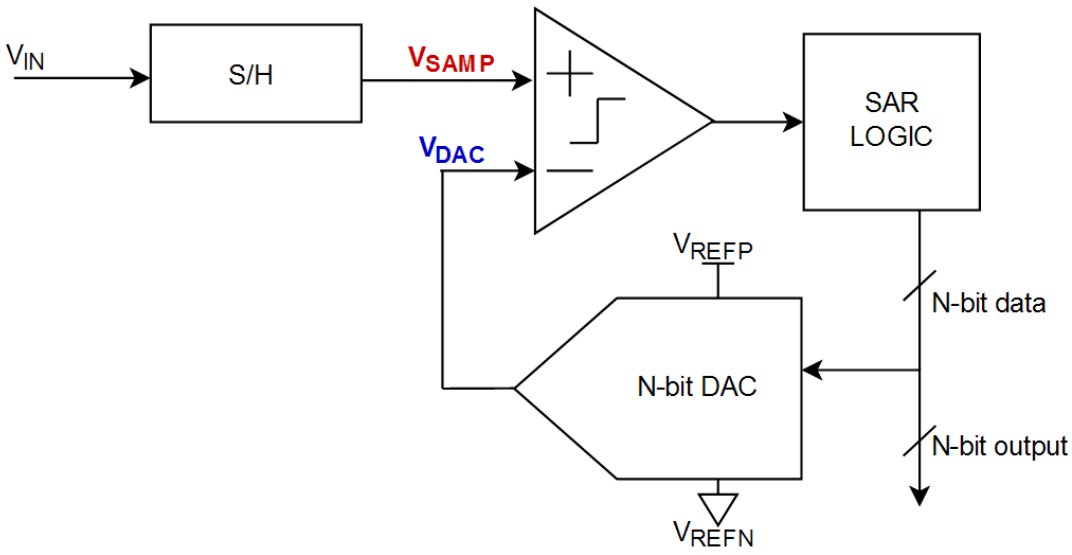


Figure 2-1. A simple single-ended N-bit SAR ADC architecture with its main components.

The conversion starts with the sampling mode. In the sampling mode, the input voltage is sampled and hold by a simple Sample/Hold (S/H) circuit during the sampling time interval. At the same time, the DAC array is reset to common-mode voltage to initiate the conversion. Following the sampling mode, the conversion starts and the sampled input voltage known as V_{SAMP} is compared with the output of N-bit DAC called as V_{DAC}. The output of the first conversion is labelled as most significant bit (MSB). According to the MSB, the SAR Logic generates the required digital signals and update the shift registers in order to update the DAC array. Then, the DAC array generates a new voltage and a second comparison is performed with the sampled input voltage. The output of the DAC, V_{DAC} increases or decreases according to the output of the previous decisions. The conversions continue until the end of the conversion. The N-bit SAR ADC requires N conversion cycles to perform the conversion. At the end of the conversion, the output of the SAR Logic is the output of the N-bit SAR ADC.

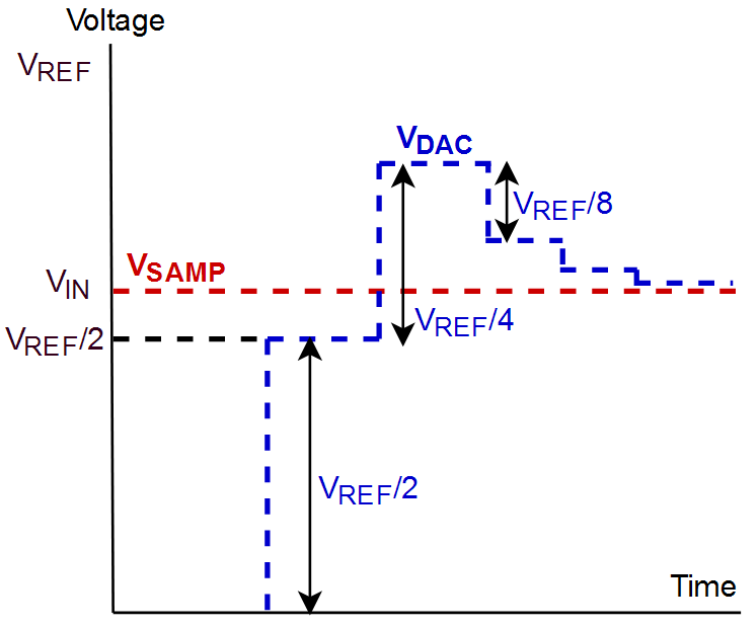


Figure 2-2 Waveform of the single-ended SAR ADC conversion.

Figure 2-2 shows the waveform of the single-ended SAR ADC conversion. After the sampling mode, the sampled input voltage is compared with the common-mode voltage, $V_{DAC} = V_{REF}/2$. For the given input voltage $V_{SAMP} > V_{DAC}$, the output of the comparison equals to 1. The SAR Logic updates its shift registers and generate a new analog voltage which is greater than the previous voltage by $V_{REF}/4$. In the second comparison, since $V_{SAMP} < V_{DAC}$, the output of the second comparison is 0 and the SAR logic is updated to decrease the output of the DAC array. The output of the DAC array approaches to sampled input voltage V_{SAMP}. At the end of the conversion, the output of DAC is reset to common-mode voltage to start a new conversion. The SAR ADC requires DAC array to generate an analog voltage for the comparison, and a comparator to perform the conversion.

Note that single-ended SAR ADC depends on the precision of the common-mode voltage which is very sensitive to environmental conditions. In order to eliminate the problems coming from the common-mode voltage, a differential architecture can be used. Figure 2-3 shows a simple differential SAR ADC.

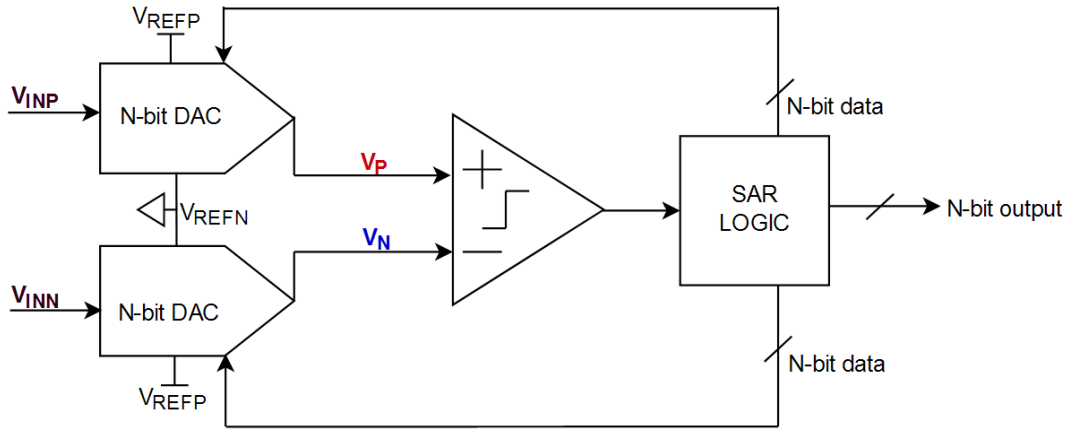


Figure 2-3.A simple differential SAR ADC.

In the differential SAR ADC, the input voltage is differential which has a positive voltage V_{INP} and a negative voltage V_{INN}. The differential input voltage is sampled on DAC_P and DAC_N respectively. An additional sample and hold circuit is not required for the input voltage sampling. After the sampling mode, the DAC_P and DAC_N generates analog voltages V_P and V_N respectively and first comparison is performed. According to the output of the first comparison, the SAR Logic updates the shift registers and DAC arrays generate new voltages. A second comparison is performed between these new voltages and according to the output of the second comparison, the SAR Logic updates the registers. The comparisons continue until the output voltage of the DAC arrays approach to common-mode voltages within 1 least significant bit (LSB) voltage. In this thesis, a differential SAR ADC is used in order to suppress the common-mode variations. In the following sections, the DAC array and comparator will be discussed further.

2.2 Analog Blocks

This section discusses the main analog components such as comparator, DAC array, and input buffer to introduce fundamental concepts.

2.2.1 Comparator

The comparator is main component responsible from performing the conversion. In the single-ended SAR ADC, the comparison is performed between the sampled input voltage and the output of the DAC array. In contrast, in the differential SAR ADC, the comparison is performed between the two outputs of the DAC array.

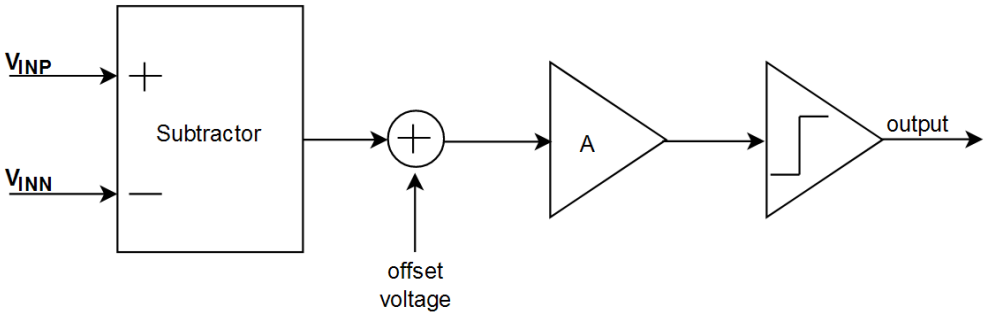


Figure 2-4. A simple comparator model to analyze the important concepts.

Figure 2-4 shows a simple comparator model to analyze the important concepts. The model initially performs subtraction in order to generate a differential input voltage. After the subtraction, an offset voltage due to process variations such as mismatches and environmental variations like temperature difference, is added to the output of the subtraction. The offset voltage may be tolerable for low and medium resolution ADCs. However, for high resolution ADCs, this offset voltage may change the comparison result. In the proposed model, after adding the offset voltage to the output of the subtraction, the voltage is multiplied by a constant A which represents the gain of the amplifier used in the comparator. Following the gain stage, a latch is used to saturate the output of the amplifier to either 1 or 0. The offset voltage can be eliminated by using offset calibration algorithms. Simple input or output offset cancellation schemes or advanced calibration algorithms can remove the offset voltage of the comparator. The model given in Figure 2-4 represents a simple comparator model which can be used for extracting fundamental properties.

In addition to this model, noise is another important concern in the comparators. In the proposed SAR ADC, the comparator noise consists of 2 major noise sources which are KT/C sampling noise and the thermal noise.

The proposed SAR ADC has a 14-bit resolution. The theoretical SNR can be defined as

$$SNR = 6.02 \cdot N + 1.76\ (dB) \tag{2.2.1}$$

where N is the resolution of the ADC. For a 14-bit ADC the theoretical SNR is 86.94 dB. The quantization noise power can written as

$$Quantization\ Noise\ Power = \frac{LSB^2}{12} = \frac{219\mu V^2}{12} = 3.99 \cdot 10^{-12}\ V^2 \tag{2.2.2}$$

The SNR can also be calculated in terms of the power of the signal, and the power of the noise of the converter.

$$SNR = \frac{P_{Signal}}{P_{Noise}} = \frac{(3.6/2\sqrt{2})^2}{P_{Noise}} \tag{2.2.3}$$

By using the equation (3.2.1), and equation (3.2.3) the power of the noise is calculated as $4.09 \cdot 10^{-9}$ V^2.Note that due to the fact that the ADC operates at 8 MS/s, and the core circuit operates much higher than the sampling frequency, the thermal noise of the comparator is dominant. As a result, the thermal noise of the comparator should be kept below 0.5 LSB voltage to differentiate the LSB voltage difference.

2.2.2 Digital-to-Analog Converter (DAC)

The Digital-to-analog converter (DAC) is used to generate analog voltage for conversion and it is a critical block that determines the performance of the overall SAR ADC. Although, the performance of the low and medium resolution SAR ADCs may not be affected by the DAC, the performance of the high resolution SAR ADCs depend on the performance of the DAC. In addition to the performance, the power dissipation and required input drivers for the DACs are the other important limitations for the SAR ADCs. These limitations depend on the DAC architecture which can be determined by the operation mode and the type of the output signal. According to the operation mode and the output signal, resistive, capacitive or hybrid DACs can be used in different SAR ADC architectures. In addition to DACs that

consists of passive components, current steering DACs can also be used in the ADCs to perform the generation of the analog signal.

1. Resistive String (R-2R ladder) network: The resistive string consists of a resistive ladder which provides a voltage division by adjusting the digital input code. In conventional architecture, the resistive string is connected to the two reference voltages V_{REF} and ground respectively. Depending to the digital input code, the resistors are either connected to V_{REF} or ground. The resistive string requires large power consumption, since the resistors are used and this type of network may not be suitable for low-power applications. Among the common resistive strings, R-2R ladder is the most common architecture used in the ADCs. Figure 2-5 shows a simple resistive DAC network.

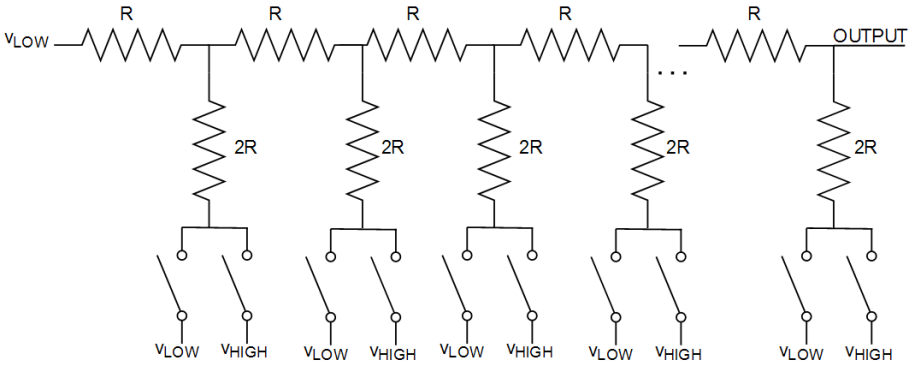


Figure 2-5. A simple resistive DAC array [15].

The digital input code controls the switches. Depending on the input code, each '2R' resistor is connected to either V_{HIGH} or V_{LOW} and an output voltage is generated.

2. Current-steering DAC network: This type of network uses binary weighted current sources instead of using resistors or capacitors. The currents of each branch is steered to one node and depending on the digital input code, the total current flowing through the output node is adjusted. The output is generally terminated with a resistor in order to generate an output voltage.

The current-steering DAC is suitable for high speed applications since, it does not require any output driver and simple switches are used to control the output current. Due to the fact that the current sources cannot be turned OFF during the conversion, it requires large power consumption compared to the other types of networks.

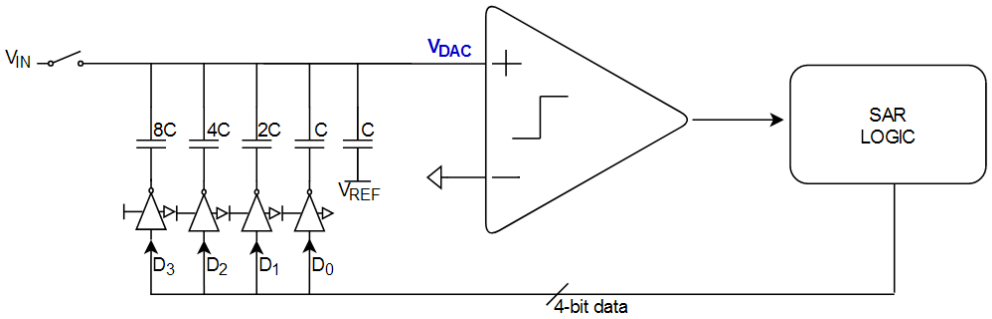
3. Capacitive DAC network: The capacitive DAC network uses capacitors and switches to perform the generation of an analog signal. Since the capacitive network is comprised of simple switches and capacitors, the implementation does not require special technology nodes and it can be easily transferred to advanced technology nodes for improving the performance of the SAR ADC. The capacitive DAC network is basically divided into two main groups which are charge-redistribution and charge-sharing DACs. The charge-sharing DAC is based on the principle of the charge sharing between the capacitors to generate an analog signal.
    a. Charge-sharing (CS) DACs: The charge-sharing DAC is based on charge sharing between capacitors. In this method, the input voltage is sampled on a sampling capacitor. Following the sampling, the sampling capacitor is disconnected from the input voltage and connected to an internal capacitor in parallel to provide charge sharing and generate the desired analog voltage for comparison. Since the working principle is based on the charge-sharing, the parasitic capacitance due to the layout can degrade the performance of the high resolution DAC. In contrast, the low and medium resolution DAC can tolerate the variations due to the parasitic capacitances and this method can be used to achieve a low-power operation.
    b. Charge-redistribution (CR) DACs: The operation of this type of DACs is based on the charge conservation and redistribution. The method requires simple switches and capacitors which makes easier to implement in any technology nodes. Since the DAC is comprised of switches and capacitors, sampling can also be performed in the

DAC which eliminates additional sampling circuits. In the conventional charge-redistribution DAC a binary weighted capacitors are used to generate analog voltage. At each conversion cycle, the bottom-plate of each capacitor is connected to a reference voltage which provides charge-redistribution on the top plate of the capacitors. The unit capacitor of the charge-redistribution DAC is determined by the kT/C noise if the mismatch limitation is not concerned. Choosing the unit capacitor at the kT/C noise limit can save switching energy during the conversion. This thesis focuses on the charge-redistribution DACs due to high immunity over parasitic capacitances, low-power and low-area properties.

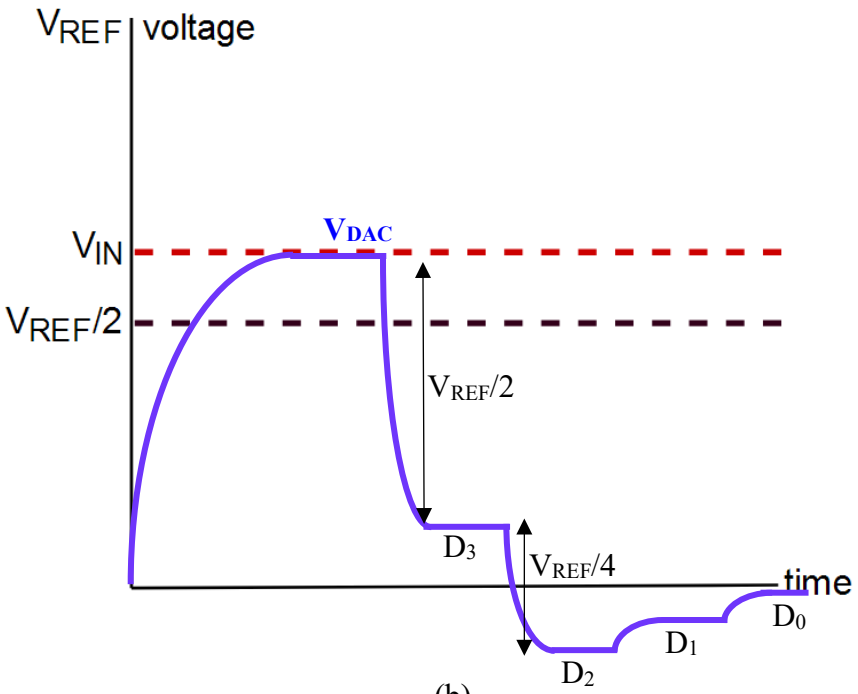
2.2.2.1 Charge-Redistribution DAC

Figure 2-6 (a) shows the SAR ADC which uses charge-redistribution DAC (CDAC) for a 4-bit implementation while (b) represents the waveform at the output of the DAC. The conversion starts with the sampling of the input voltage labelled as V_{IN}. During the sampling mode, the top plate of the capacitor array is connected to the input voltage while the bottom plate of each capacitor is connected to V_{REF}. Following the sampling mode, the sampling switch is OFF and the top-plate of the capacitor array becomes a floating node. In the next cycle, the conversion is initiated by connecting the bottom plate of the MSB capacitor to ground resulting a downward $V_{REF}/2$ shift on the top plate of the capacitor array. A comparison is performed for the given V_{IN}. In the given example the output is 1, since $V_{DAC} > 0$ and the MSB D3 is stored as 1 in the SAR Logic. In the next conversion cycle, the bottom plate of the MSB-1 capacitor is connected to ground resulting a downward $V_{REF}/4$ shift on the output of the DAC. A second comparison is performed and in this case the output of the comparison is 0 since, $V_{DAC} < 0$. The (MSB-1) D2 is stored as 0 in the SAR Logic while the bottom plate of the (MSB-1) capacitor is switched back to V_{REF}. In the next conversion cycle D1 is set to 1 and the bottom plate of the (MSB-2) capacitor is

connected to ground which results a net upward $V_{REF}/8$ shift when including the (MSB-1) capacitor effect. The conversion continues until the decision of the final bit called as LSB.



(a)



(b)

Figure 2-6 (a) SAR ADC which uses charge-redistribution DAC (CDAC) for a 4-bit implementation (b) Waveform at the output of the DAC.

The charge-redistribution DAC can also be designed with split capacitors and C-2C capacitor arrays. In the previous sections, the charge-redistribution DAC consists of binary weighted capacitors. Up to 10-bit the binary weighted capacitors can be used for the conversion. Beyond the 10-bit resolution, the power consumption and silicon area are the limiting factors. For these reasons, pure binary weighted capacitor arrays cannot be used for the high resolution SAR ADCs. Figure 2-7 shows a simple 5-bit SAR ADC with binary weighted capacitor DAC array.

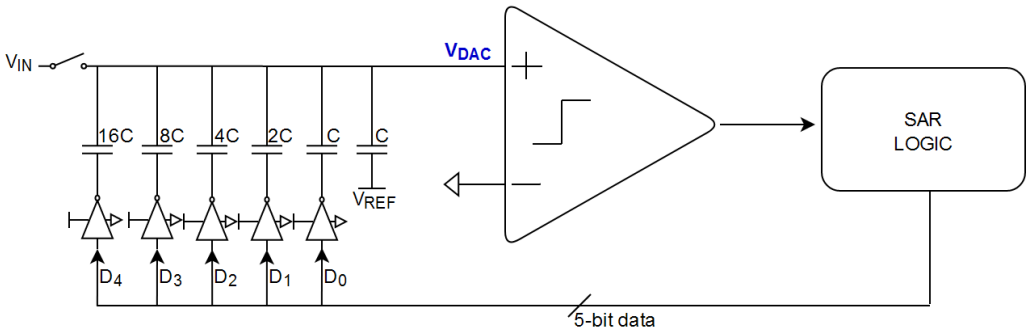
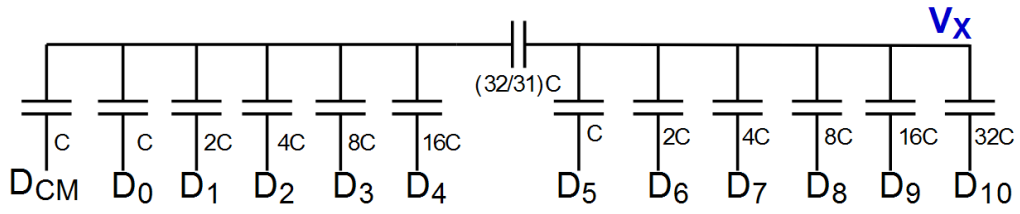


Figure 2-7. A simple 5-bit SAR ADC with binary weighted capacitor DAC array.

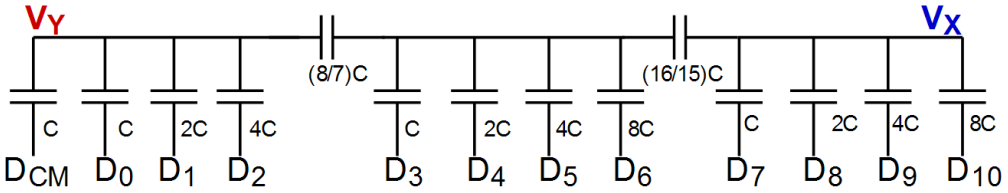
For an N-bit SAR ADC, 2^N unit capacitors are required to perform the conversion with single-ended DAC array. As it was mentioned above, the disadvantage of this DAC array is that it requires large silicon area for the resolutions beyond 10 bit. In contrast, the advantage of this binary weighted DAC array is that there is no parasitic capacitors coming from the bottom plates of the each capacitor in the DAC. As a result, the charge equation is not affected by the parasitic capacitors due to the bottom plates of each capacitor. However, in the layout due to the routings, there can be some parasitic capacitors which can degrade the performance of the binary weighted DAC array.

As the resolution increases, the number of unit capacitors exponentially increases which cannot be implemented in the silicon area, since the DAC arrays occupy large silicon area and require very strong and power hungry drivers to charge and

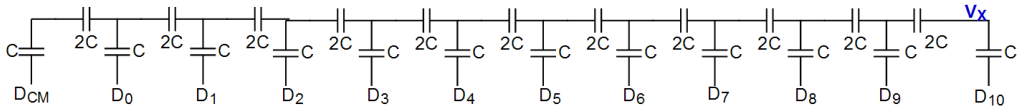
discharge each capacitor. Thus, simple binary-weighted capacitor array is not feasible for the high resolution SAR ADCs. In order to overcome this issue, a modified version of the capacitor array called as split capacitor array can be used. The split capacitor array divides the main capacitor array into 2 sub capacitor array by using a bridge capacitor resulting less number of unit capacitors compared to binary weighted capacitor array. As long as the capacitor ratios are preserved, the voltage change at the input of the comparator is same with change in the binary weighted array. There are different types of split capacitor DAC array. Figure 2-8 shows 3 different split capacitor DAC array architectures for an 11-bit ADC.



(a) 2bw1 C_{BRIDGE}



(b) 3bw2 C_{BRIDGE}



(c) C-2C array

Figure 2-8. 3 Different split capacitor DAC array architectures for an 11-bit ADC.

In each architecture, a bridge capacitor is used to divide the array into the sub array in order to provide a proper voltage division. The usage of the bridge capacitor decreases the number of unit capacitors and silicon area compared to the binary weighted capacitor array. Moreover, as the number of bridge capacitors increases, the number of unit capacitors decreases further. At first, decreasing the number of unit capacitors seems to be good. However, as the number of bridge capacitor increases, the bottom plate of each bridge capacitor leads to parasitic capacitances which can alter the charge equation, resulting wrong output voltages at the input of the comparator. In addition to this issue, the linearity becomes worse as the array shrinks down due to the non-fractional bridge capacitors, since there is a mismatch between the unit capacitor and these non-fractional bridge capacitors. In order to overcome this problem, [42-44] propose a solution which state that the unit capacitors can be re-sized according to the parasitic capacitance at the bottom plate of the bridge capacitor and the non-linearity can be eliminated. The non-linearity can be calculated as follows;

For a typical simple split capacitor array, the maximum error occurs when there is a transition from "0111…111" to "1000…000" which is MSB transition. For the architecture given in figure 2.7 (a), the output voltage of the DAC can be defined as

$$V_X = \frac{C_{10}}{\frac{(C_{CM}+\sum_{k=0}^{4} C_k)\cdot C_{BRIDGE}}{(C_{CM}+\sum_{k=0}^{4} C_k)+C_{BRIDGE}} + \sum_{k=5}^{9} C_k + C_{10}} \cdot vrefp \tag{2.3.4}$$

where the reference voltage *vrefp* represents the supply voltage. In this thesis, 1.8V supply voltage is used. For a given technology node, standard deviation of the mismatch of a capacitor is expressed as;

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{A_C}{\sqrt{WL}} \tag{2.3.5}$$

where A_C is the process dependent parameter, and it is 2.3 % µm in 0.18 µm CMOS technology. W, and L are the width, and length of the capacitor respectively. In order to calculate the voltage distribution, the unit capacitor is selected as 9 fF as a reference to select the best architecture. Figure 2.9 shows the Gaussian distribution, and histogram of the voltage V_X for a single bridge capacitor.

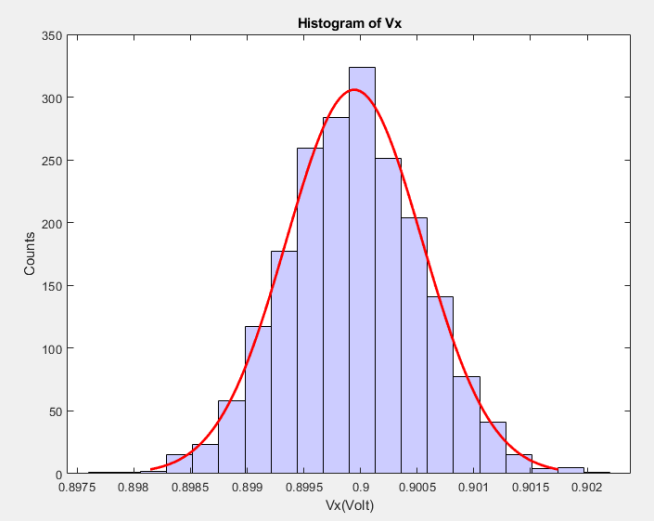


Figure 2-9. The Gaussian distribution, and histogram of the voltage V_X for a single bridge capacitor.

Figure 2.9 reveals that, the voltage change due to the mismatches are within the limits. Most of the samples are at 0.9V. Figure 2.10 shows the Gaussian distribution, and histogram of the output voltage for the 2 Bridge Capacitor.

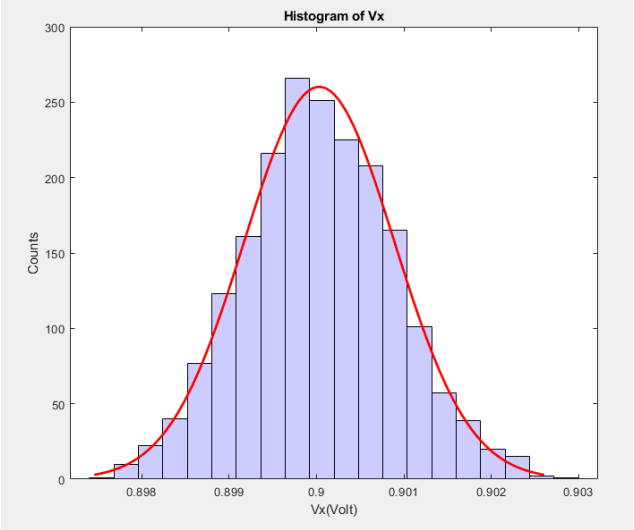


Figure 2-10. The Gaussian distribution, and histogram of the output voltage for 2 bridge Capacitor.

It is observed that when adding one more bridge capacitor, the variation in the voltage increases. Less samples are at 0.9V compared to the 1 bridge capacitor model. Figure 2.11 plots the Gaussian distribution, and histogram for the C-2C capacitor array.

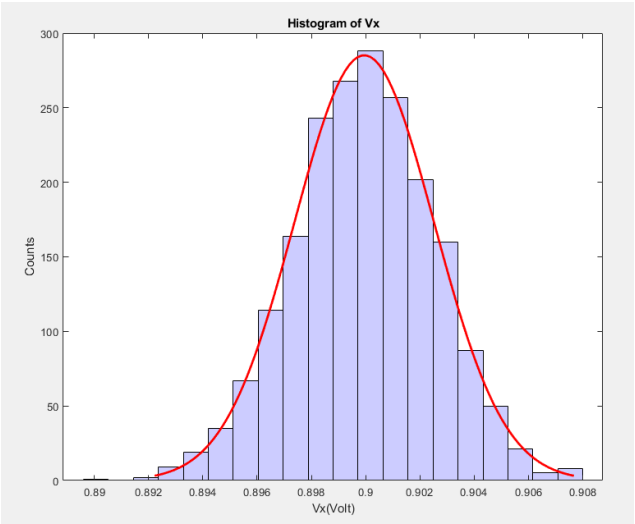


Figure 2-11. The Gaussian distribution, and histogram for the C-2C capacitor array.

When the number of bridge capacitors increases, the variations due to the mismatch increases, since the charge equation is altered compared to the original equation. For the best performance, in the proposed ADC, the split capacitor architecture with 1 bridge capacitor is used. Figure 2-12 shows the DNL estimation for a split capacitor array with 1 attenuator capacitor.

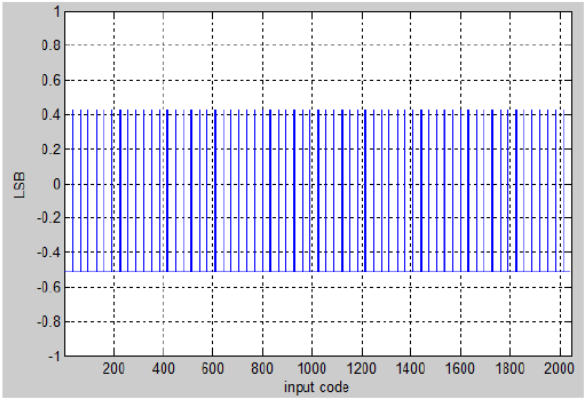


Figure 2-12. The DNL estimation for a split capacitor array with 1 attenuator capacitor [45].

The DNL of the array is within the limits and it guarantees that there is no missing code and non- monotonicity. Figure 2-13 shows the INL estimation of the split capacitor array with 1 attenuator capacitor.

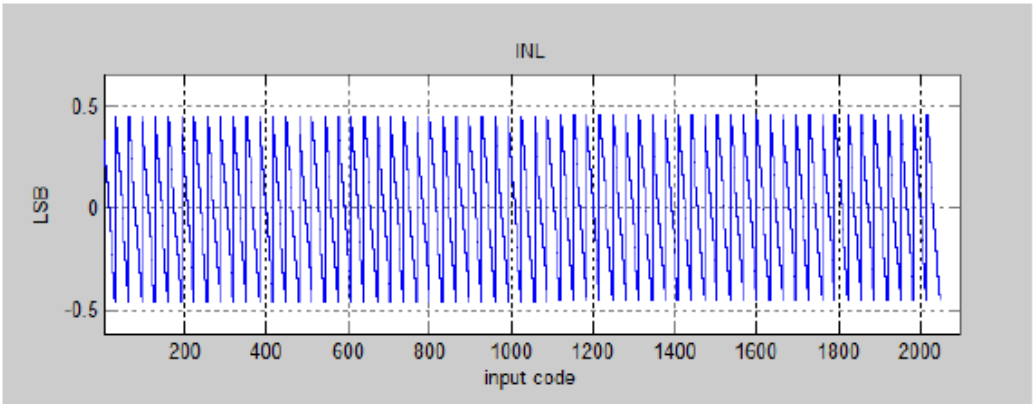


Figure 2-13. The INL estimation of the split capacitor array with 1 attenuator capacitor [45].

The INL is also within the limits which implies that the static error does not affect the performance of the ADC.

In addition to the linearity requirement, the sampling noise known as KT/C noise is another limit for the DAC array. The sampling noise should provide the required SNR. The required SNR is calculated by using the equations (3.2.1), (3.2.2), and (3.2.3). From the equations, the theoretical noise of the overall system is found as $4.069 \cdot 10^{-9}$ V^2. This noise is greater than the quantization noise as expected. Assume that the overall noise of the system is dominated by the KT/C noise. By the way, in many ADCs, the sampling noise is the dominant noise component. The noise equation can be written as;

$$\frac{KT}{C} = \ 4.069 \cdot 10^{-9} V^2 \tag{3.2.6}$$

where K represents the Boltzmann constant, and T is the ambient temperature. From equation (3.2.6) the minimum sampling capacitor is 1.07 pF. In addition to kT/C noise, the parasitic capacitances due to routings in the layout may also degrade the performance of the capacitor array. As a result, a large unit capacitor than the minimum size unit capacitor is generally preferred to suppress the parasitic effects.

2.3 Digital Blocks

The digital block of the core circuit is the SAR Logic which consists of a group of shift registers to store and generate the required digital signals. The SAR Logic updates the capacitive DAC array according to the result of the previous comparison. The conventional SAR Logic consists of 2 different group of shift registers. The first group of shift register fires the next bit to initiate a new comparison, while the second group of shift register serves as a memory to store the output data of the SAR ADC. At the end of the conversion, the output data in the memory are sent to the external processor or devices in parallel. The 14-bit output data can also be sent in serial by using a serializer which requires high speed to sustain an 8 MS/s conversion rate and high power consumption.

The SAR Logic can have synchronous or asynchronous timing for the conversion. Conventional early designs used synchronous timing which provides equal time interval for each comparison. In other words, the SAR logic allocates the same time interval for MSB and LSB comparison. The required time for the decision of the MSB comparison is shorter than the time required by the LSB comparison. As a result, for the conventional SAR Logic, the allocated time for the MSB comparisons is wasted. In order to overcome this issue, asynchronous timing can be used. In the asynchronous timing, the LSB comparisons require more time to perform comparison and the next comparison cycle is determined by itself using an on-chip delay lines [46-47]. Figure 2-14 shows an example of an asynchronous timing with the sampling clock.

Figure 2-14. An example of an asynchronous timing with the sampling clock [48].

Each comparison starts with the end of the reset interval. At the rising edge of the latch, the comparison is resolved and the output is determined. At the falling edge of the clock, the latch is reset to initiate the next comparison.

2.4 SAR Loop Delay Optimization

The speed of the SAR ADC is determined the sum of the delays of these blocks. Figure 2-15 shows the main components of the SAR ADC with the corresponding delays.

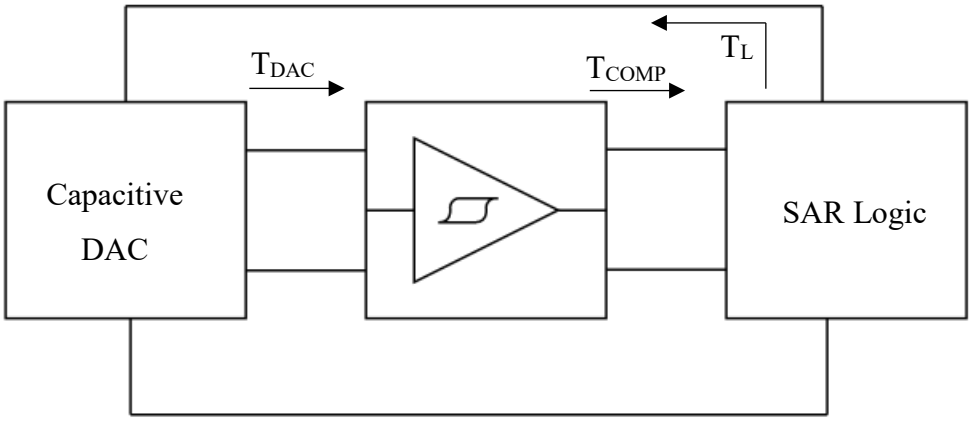


Figure 2-15. The main components of the SAR ADC with the corresponding delays.

The SAR loop delay consists of the settling time of the DAC array labelled as T_{DAC}, the comparator decision time T_{COMP}, and the SAR Logic delay T_L. In order to increase the speed of the converter, these 3 delays must be optimized.

a. The settling of the DAC array depends on the driving capability of the each capacitor in the array. The capacitors in the DAC array are driven by simple inverters during the conversion cycle. The size of the transistors in the inverters depend on the conversion rate, settling time, and the size of the unit capacitor. In order to speed up the conversion, larger inverters are required resulting large power consumption and larger required silicon area for the implementation.

b. The comparator delay is dictated by the minimum input differential voltage and the required power consumption. If the LSB voltage is very small, the comparator requires more time to make a decision. In addition, additional offset cancellation algorithms may be required for high resolution ADCs which allocates more time for the comparison.
c. The SAR Logic is generally limited by the propagation times of the shift registers. In the conventional architecture, there are 2 different group of shift registers resulting 2 times propagation delay for starting the next comparison.

In order to increase the conversion rate, all of the delays must be optimized while considering other limitations such as resolution and power consumption.

2.5 Achieving High Resolution Performance

Figure 2-16 illustrates the sampling frequency vs SNDR for SAR ADCs published at ISSCC, and the VLSI symposium [49]. It reveals that the high speed ADCs beyond 100 MS/s conversion rate have limited resolution, since adding more cycles results in more delay which leads to the reduction of the conversion rate. In addition, as the resolution of the ADC increases, the resolution of the DAC also increases and the number of unit capacitors increases. As the total size of the capacitor array increases, the ADC occupies larger silicon area and demands larger power consumption. In addition to area and power consumption limitation, driving the unit capacitors is another problem for the high-speed ADCs under certain limitations such as power consumption and sampling time.

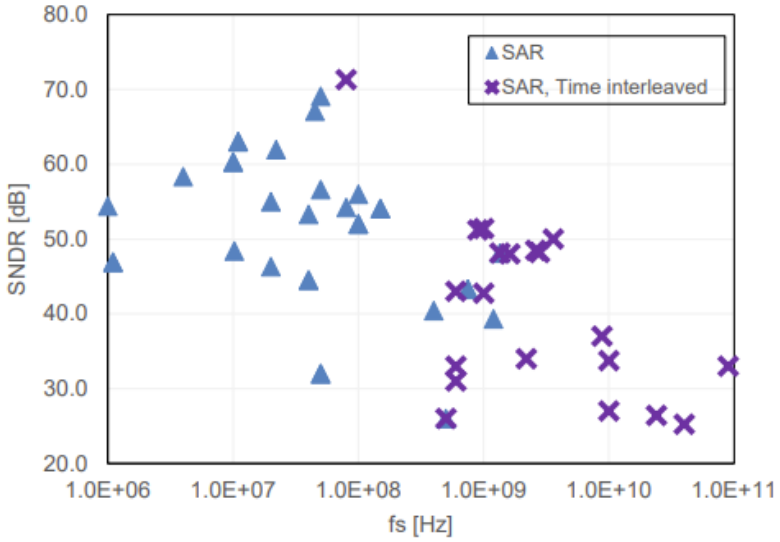


Figure 2-16. The sampling frequency vs SNDR for SAR ADCs [49].

In order to alleviate these problems, sub-ranging ADC architectures are used to perform conversion [50]. The sub-ranging SAR ADCs employ flash ADCs for the first MSB and uses DAC array for remaining bits. Another solution for high-speed ADCs is to use pipeline ADCs. Figure 2-17 shows a typical pipeline SAR ADCs [51-53].

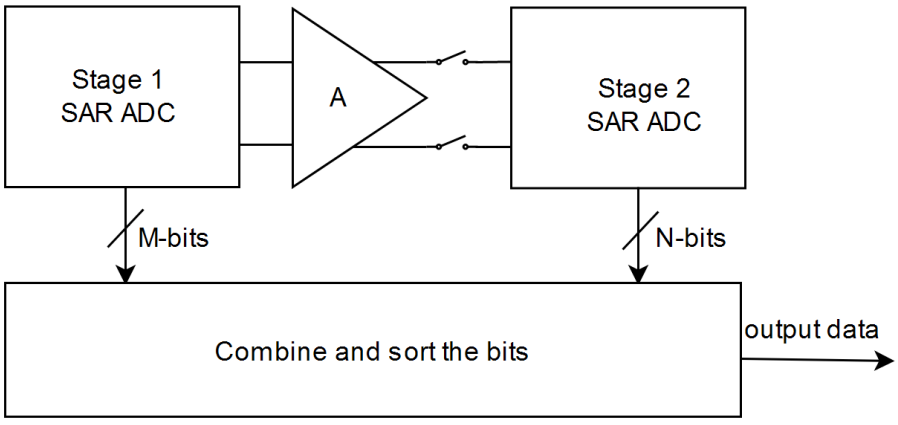


Figure 2-17. A typical pipeline SAR ADCs [32-34].

The 2-stage pipeline SAR ADCs have 2 moderate resolution (6-8 bits) standalone SAR ADCs to achieve a high resolution performance at high-speed and they use a residue amplifier as an inter-stage gain to separate and provide enough gain to second stage. In recent researches, the residue amplifier is replaced by dynamic amplifiers which provides good performance with low-power consumption [54]. However, dynamic amplifiers have some limitations to achieve high SNR values.

2.6 Conclusion

This chapter overviews of a basic SAR ADC and analyses its main components in order to evaluate based on the certain parameters such as linearity, power consumption and conversion rate. In order to analyze the main components, basic models are used implement the components.

a. The comparator is the main component responsible for performing the comparison. The offset voltage, noise and conversion rate are the limitation factors for the comparator.
b. The DAC array can be designed with either the passive components such as resistors and capacitors or current sources. The current sources demand large power consumption and they cannot be turned off when it is not used. The resistive DAC also requires large power consumption in addition to large silicon area. The capacitive DAC is more preferable since it requires less silicon area and demand less power consumption compared to the previous architectures. There are generally 2 different types of capacitive DAC array which are charge-sharing and charge-redistribution DAC array. In this thesis charge-redistribution DAC array is used to achieve a high resolution performance.
c. The SAR Logic can have either synchronous or asynchronous timing. Asynchronous timing allocates more time during LSB conversions and the

less time for the MSB conversions in order to achieve a good performance. In addition, by allocating less time in MSB conversions, the conversion speed of the SAR ADC is also increased which is very important for the high-speed applications.

d. The SAR loop delay determines the conversion rate. The loop delay consists of the settling time of the DAC array, comparator delay, and SAR logic delay. By using a synchronous SAR Logic and reduced number of shift registers, the propagation delay in the SAR Logic can be minimized. The settling time of the DAC array depends on the size of the unit capacitors and the size of the inverters. Larger inverters are required to drive the capacitors for the high-speed applications at the expense of large power consumptions. The comparison delay is dictated by the minimum input differential voltage, the conversion rate, noise and the power consumption requirement. By optimizing these delays, a high-speed SAR ADC with high resolution can be achieved.

CHAPTER 3

IMPLEMENTATION OF THE DIGITAL-TO-ANALOG CONVERTER

The previous chapters discussed the important parameters and design techniques for the implementation of the SAR ADCs. Chapter 1 analyzed the important transfer characteristics and performance metrics to understand the errors that can cause performance degradation. Chapter 2 investigated the important parameters of each component in the SAR ADC, analyzed the SAR loop delay, and sought novel methods for achieving high performance. This chapter presents the implementation of the digital-to-analog converter and compares with the state-of-the-art methods. Section 3.1 introduces the digital-to-analog converter architecture and DAC array. Section 3.2 explains the DAC switches and settling time. Section 3.3 discusses the existing state-of-the-art DAC switching schemes Section 3.4 analyzes the proposed switching schemes and compare them with the existing DAC switching schemes. Section 3.5 summarizes the chapter.

3.1 Digital-to-Analog Converter (DAC)

The digital-to-analog converter (DAC) is a very important component for the SAR ADCs. The overall performance of the SAR ADC depends on the architecture and the layout of the DAC. Especially, for high resolution applications, the mismatch and parasitic capacitance plays a critical role in the performance of the DAC. In order to overcome these problems and select the best DAC architecture, in the previous chapter, the DAC was analyzed and various architectures were investigated in terms of power and linearity. From these investigations, it can be deduced that the charge-redistribution DACs with 1 bridge capacitor is the most suitable DAC architecture for this thesis. The conventional charge-redistribution DAC with 1 bridge capacitor

requires a fractional bridge capacitor resulting mismatches and linearity problems which can degrade the performance of the SAR ADC. Figure 3-1 shows a typical 11-bit CR DAC with fractional bridge capacitor.

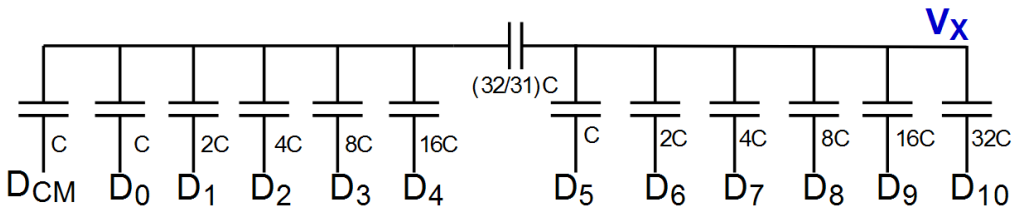


Figure 3-1. 11-bit CR DAC with fractional bridge capacitor.

In order to sustain the charge equation at the output node of the DAC called as V_X, this fractional capacitor is required. The resolutions up to 10-bit or even 12-bit, this architecture provides a good linearity performance. Beyond the 12-bit resolution, there may be serious linearity problems due to the process variations since, the bridge capacitor has a different size compared to the unit capacitor of the DAC array. In order to alleviate this issue, researches have focused on architectures that have integer bridge capacitor. The work in [55] shows that, that the DAC array with integer number bridge capacitor can be designed with minimum gain error. In this work, an 8-bit DAC was designed with different integer number of bridge capacitors. The result of this work reveals that, the effective number of bits known as ENOB is not seriously degraded. In order to use an integer number of bridge capacitor, a compensation capacitor is required to sustain the charge equation at the output node of the DAC array. This thesis adapts the 2C bridge capacitor where C is the unit capacitor for a 14-bit resolution DAC. Figure 3-2 shows the proposed architecture of the DAC array with 2C bridge capacitor.

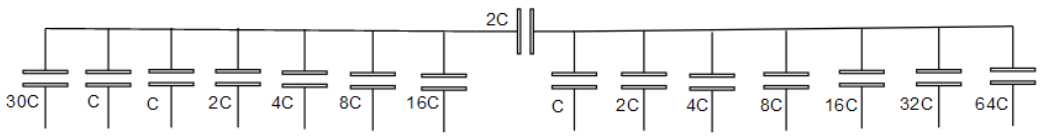


Figure 3-2. The proposed architecture of the DAC array with 2C bridge capacitor.

In conventional design, the proposed DAC architecture is used for a typical 12-bit conversion. In this thesis, same architecture is used for 14-bit conversion, decreasing the number of unit capacitors compared to the conventional architectures. The proposed DAC switching schemes which will be discussed in the following sections eliminate the MSB capacitors and uses the dummy capacitor for the LSB comparison. The proposed architecture has an additional 30C capacitor to sustain the charge equation at the output node of the DAC array. The bottom plate of this additional capacitor is always connected to the common-mode voltage and it does not connect to any other voltage in the DAC array during the conversion. The size of the unit capacitor of the proposed DAC array depends on the kT/C sampling noise. The KT/C noise is defined as:

$$V_{noise,RMS} = \sqrt{\frac{KT}{C}} \tag{3.1.1}$$

where K is the Boltzmann constant, T is the temperature, and C is the total sampling capacitor. The theoretical SNR of a 14 bit ADC is 86.04 dB. For such a SNR, the minimum value of the sampling capacitor is 1.017 pF. In other words, the minimum total capacitor value in the DAC array should 1.017 pF in order to achieve 14-bit performance. The proposed DAC array has 159 unit capacitors and the minimum value of the unit capacitor must be 6.39 fF to achieve a 14-bit resolution. In addition to KT/C noise limitation, linearity is another important factor for determining the size of the unit capacitor. The linearity requirement dictates that the minimum value of the unit capacitor should be approximately 25 fF in order to suppress the effects of the mismatches and provide 14-bit resolution. In this work, to eliminate the effects

of the parasitic capacitances due to the routings in the layout, 33fF capacitor is used as the unit capacitor. In order to obtain a good matching, the length and width of the capacitor are closed together which are 3.6 µm and 3.7 µm respectively. In order to minimize the size of the capacitor high density capacitors are used to implement the proposed DAC array. Figure 3.3 shows the layout of the proposed DAC architecture with the switches. The layout consists of 2 DAC array, and the layout measures 300 µmx290 µm.

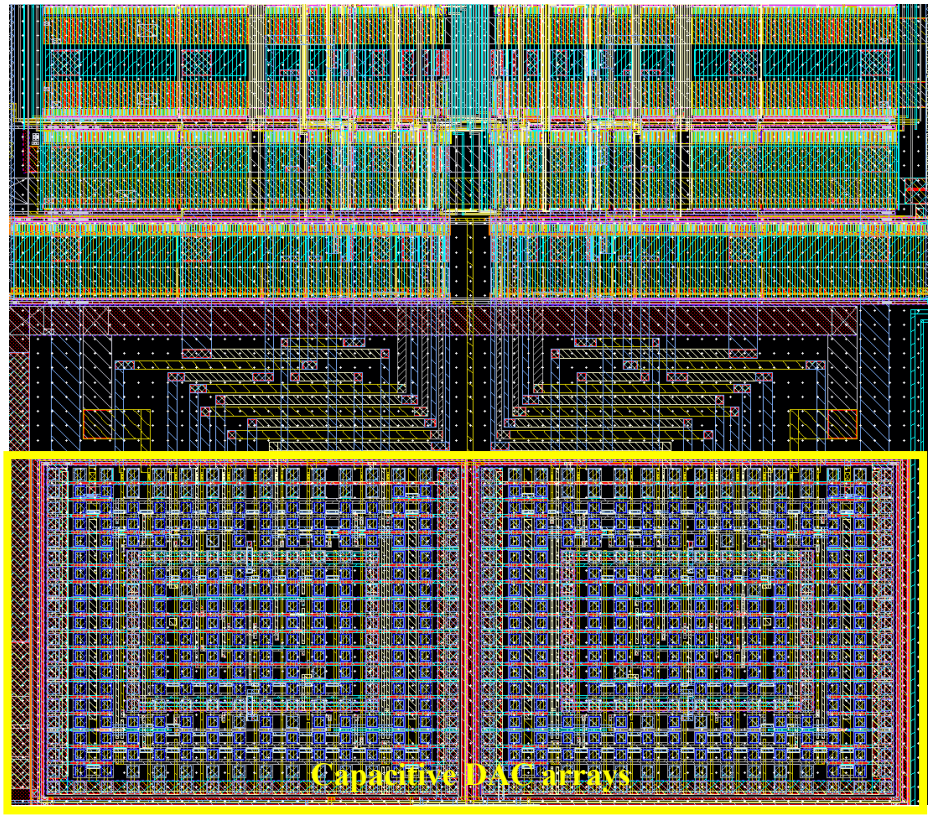


Figure 3-3. The layout of the proposed DAC architecture with switches.

In order to match the capacitors and minimizes the mismatches, a common centroid layout technique is applied for the layout of the capacitors. Figure 3-4 shows the floor plan of the layout of the proposed DAC array.

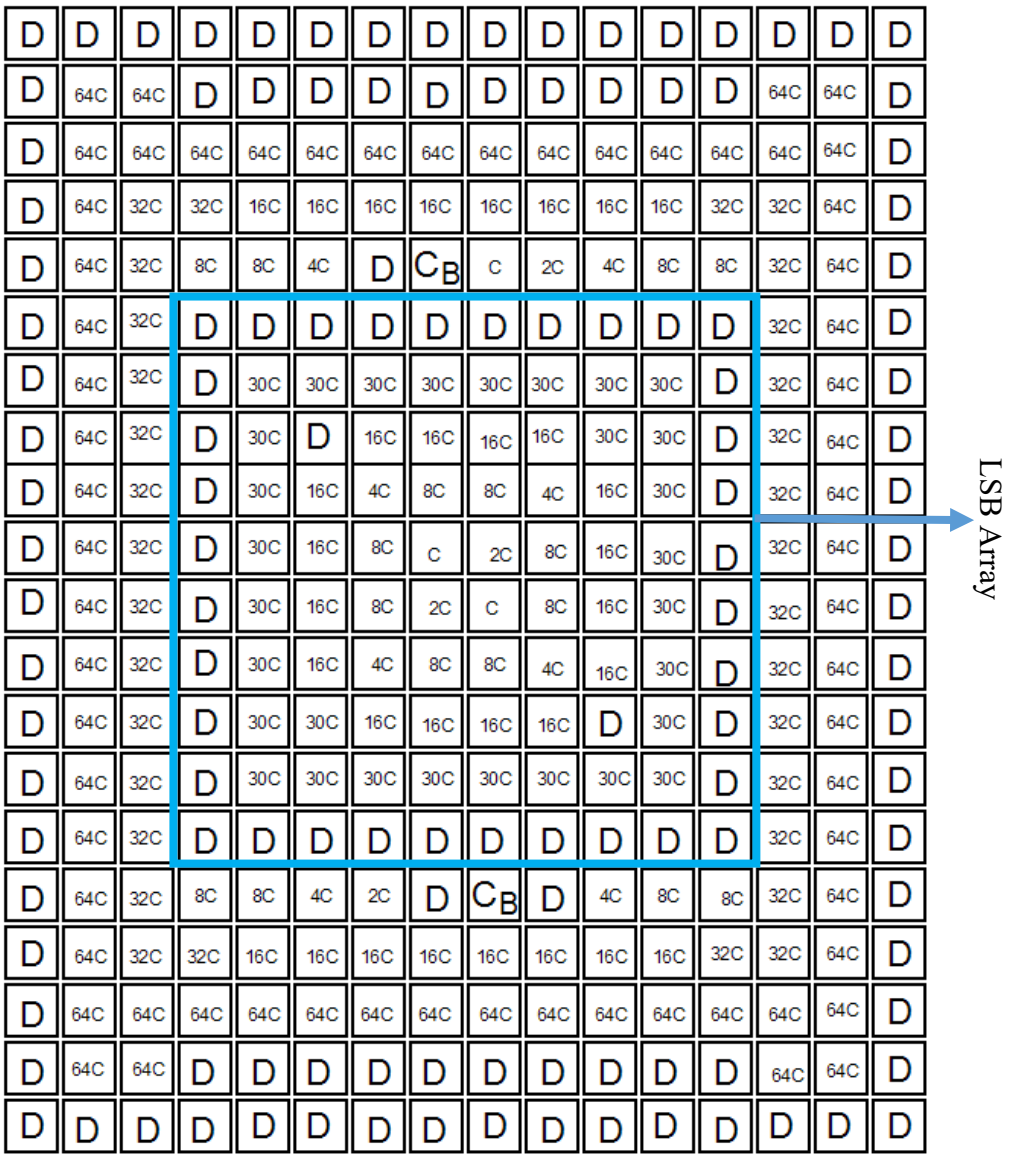


Figure 3-4. Floor plan of the layout of the proposed DAC array.

The floor plan includes dummy blocks labeled as D, bridge capacitor as C_B, and other unit capacitors forming the DAC array. During the analog extraction, it is observed that, when the dummy blocks are connected to ground, there are some capacitive couplings between the output node of the capacitor DAC array and ground. These couplings lead to wrong voltage divisions resulting wrong output data. For this

reason, the dummy blocks are not connected to the ground. In addition, for the dummy blocks simple metals are used, since the process that is used for the implementation of the ADC does not allow a float capacitor.

3.2 DAC Switches

The DAC switches play a critical role during the settling of the capacitors in the DAC array. They provide a connection between the bottom plate of the each capacitor and the reference voltages such as supply voltage and ground. The ON-switch resistance determines the settling time when the capacitor value is constant. In order to increase the conversion rate of the SAR ADC, the DAC switches should have low ON-switch resistance resulting large devices which may occupy large silicon area. There is a tradeoff between the settling time, and the required silicon area. In addition to large silicon area, the large switches may demand large power consumption. In the conventional architecture, the switches can be categorized into two different group which are mux-likes switches and shared-like switches. Figure 3-5 shows a typical mux-like topology for a typical DAC array. This method uses 3 different switches to connect the 4 different type of voltages to the bottom-plate of the capacitor. This type of switch is suitable for high speed operation, since this type of architecture requires less number of switches compared to the mux-like switch architecture.

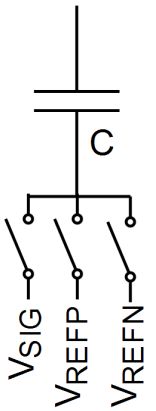


Figure 3-5. A mux-like topology for a typical DAC array.

The mux-like switch architecture requires more complex DAC control logic unit due to the fact that, at each conversion, the switch is ON while the rest of the switches are turned OFF. Figure 3-6 shows a shared-like topology for a typical DAC array.

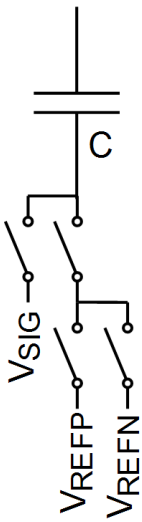


Figure 3-6. A shared-like topology for typical a DAC array.

In this topology, the first observation is that the number of switches increases compared to the previous topology resulting large silicon area. The second observation is that there is a series connection between the switches for providing the reference voltage. The series connection double the on-resistance of the switches in which the settling time is doubled, resulting incomplete settling time or reduction in the conversion rate of the ADC. On the other hand, this topology has simple DAC control logic unit, which relaxes the SAR digital controller. For low and medium speed SAR ADCs, this type of switch topology can be used while, for high speed ADCs, the mux-like topology should be used. In this thesis, the previous topology called as mux-like switch topology is used to achieve high speed and shorter settling time. The settling time of the capacitor determines the required time for each conversion cycle. In order to calculate the settling time, the ON-switch resistance

should be calculated. The switches in the DAC array are operated in the deep triode region. In this regime, the on- resistance of the switches can be expressed as:

$$R_{ON} = \frac{1}{\mu C_{OX}\frac{W}{L}(V_{GS}-V_{TH})} \tag{3.2.1}$$

where W and L are width and length of the transistor, C_{OX} and μ are process parameters, and V_{GS}-V_{TH} is the overdrive voltage of the transistor. For a typical DAC array, the maximum voltage shift occurs when there is a transition on the MSB capacitor. It means that RC time constant which corresponds to $R_{ON\text{-}EQ}C_{MSB}$ should satisfy the required time interval for each conversion. The time constant including the equivalent resistances capacitances can be written as

$$\tau = RC\ln(2^N) \tag{3.2.2}$$

where N represents the number of bits [56]. For N=14, the required time is 9.7 RC. The maximum allocated time for settling is 3.125 ns for each comparison. The unit capacitor is chosen to be 33 fF which was discussed in the previous section. As a result, the maximum total resistance should be 167 ohm for the settling within 3.125 ns. The settling should be finalized before the allocated time. For this reason, the switches should be designed in such a way that their resistance should be lower than the theoretical value.

3.3 Existing state-of-the-art DAC switching schemes

DAC switching scheme plays an important role in the ADC design. The reference driver provides the required switching energy and ensures the settling time by maintaining the instantaneous current for the DAC array. The settling time is also determined by the switch resistance and the capacitors in the DAC array. The DAC switching scheme adjusts the connections of the reference voltages to the capacitor array in order to generate analog voltage at the output of the DAC for comparison. The conventional DAC switching scheme provides V_{REF} and ground in a certain manner and requires simple DAC control logic to turn ON and OFF the DAC switches. However, the conventional DAC switching scheme wastes a considerable amount of energy during the conversion which is not suitable for low-power applications. Figure 3-7 shows the conventional DAC switching scheme with the SAR ADC architecture for a 3-bit typical implementation. In order to suppress the common-mode voltage variations and noise problems a differential architecture is used to illustrate the conventional DAC switching scheme. Figure 3-7 (a) illustrates the sampling phase. During the sampling phase, the bottom plates of the capacitors in the DAC arrays are connected to the input voltage, while the top plates of the capacitors in the DAC arrays are tied to V_{CM}. Following the sampling, the input sampling switches are turned OFF and the conversion starts. The bottom plate of the MSB capacitors in both DAC array are connected to V_{REF} and the bottom plate of rest of the capacitors in both DAC array are tied to ground and a comparison is performed. If $V_P > V_N$ the voltage at V_N shift upward by $V_{REF}/4$ while the voltage at V_P shifts downward by same amount which is illustrated in (c). In contrast, if $V_N > V_P$ V_N shifts upward by $V_{REF}/4$, and V_P shifts downward by the same amount which is shown is (d).

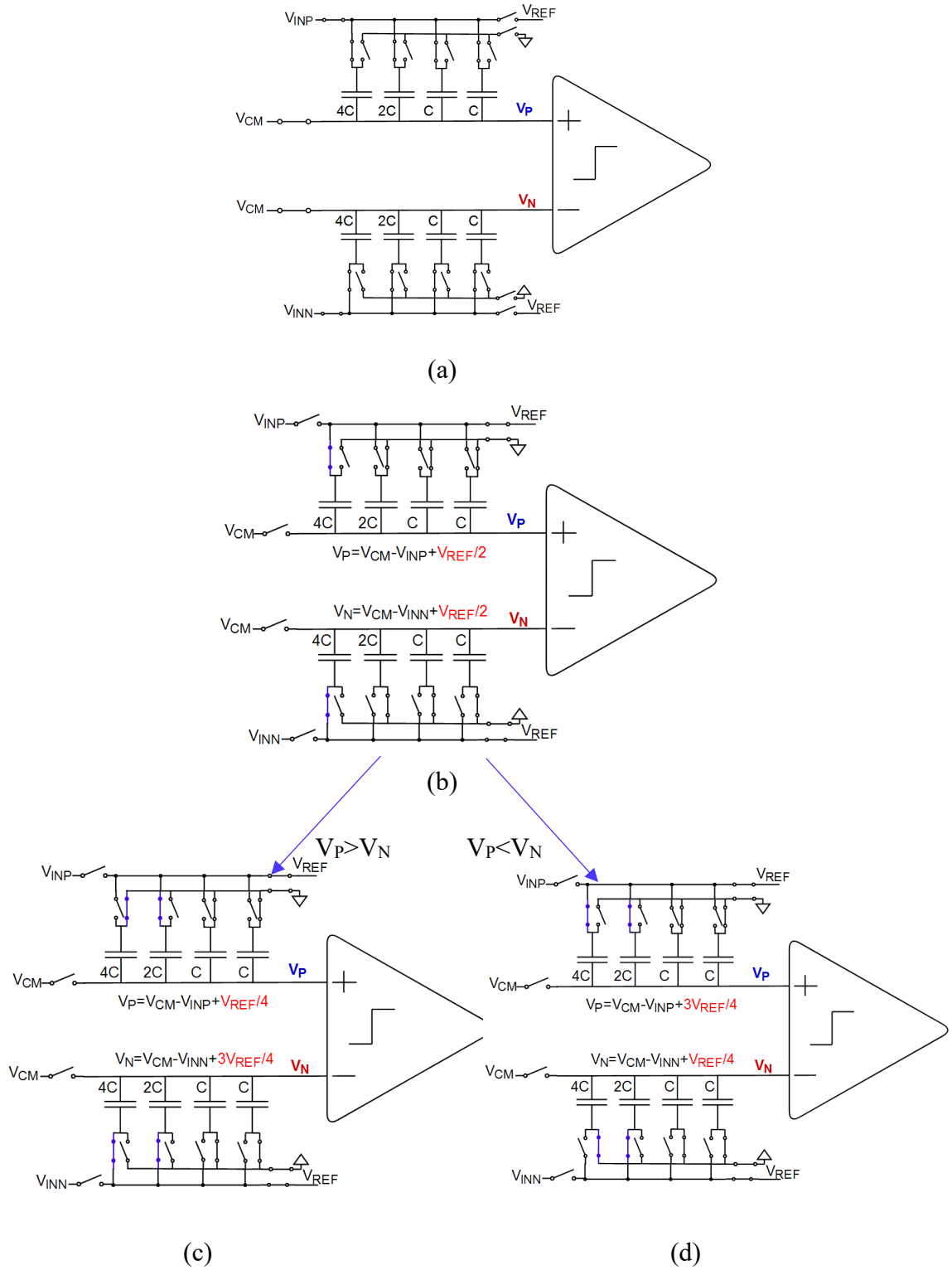


Figure 3-7. Conventional DAC switching scheme with the SAR ADC architecture for a 3-bit typical implementation (a) sampling phase (b) Conversion phase I (c) Conversion phase II if $V_P>V_N$ (d) Conversion phase II if $V_P<V_N$

The conventional DAC switching scheme has two reference voltages for the switching which is good for high resolution conversion. However, this switching algorithm wastes considerable amount of energy during reset phase. If comparison fails, the capacitors in the previous comparison have to switch back to old positions which requires some amount of energy. For MSB capacitors, this reset energy can be comparable to the switching energy which is an undesired situation. In order to decrease the reset energy, researches have focused on novel switching schemes which are not only used for decreasing the energy but also used to reduce the overall silicon area occupied by the capacitors. In addition to reduce the energy and silicon area, top-plate sampling is also used to eliminate the energy consumption demanded by the MSB capacitors, since the differential input voltages are directly sampled at the input nodes of the comparator. The top-plate sampling is a common way for the conversions required a resolution up to 10-bits. Beyond the 10-bit resolution, bottom plate sampling is required, since the input switches cause charge injection while turning OFF and the charge injection is signal dependent which is not static. In addition, since the input voltage is differential, the input nodes of the comparator encounter different charge injections which cannot be eliminated by the calibration algorithms. For this reason, in this thesis, the bottom-plate sampling technique is used to eliminate the charge injections. Note that, there are charge injections at the input node of the comparators due to the common-mode voltage switches in the conventional scheme. However, since the voltage is constant, the charge injections are almost same at the input nodes of the comparator which can be avoided during the differential operation. If the differential operation is not used, the charge injection leads to a static error which can be fixed by calibration algorithms.

In order to decrease the reset energy, Liu et al [57] proposed a monotonic switching technique which uses a top-plate sampling and the bottom plates are reset to V_{REFP}. This switching method requires switching activities in only one DAC array which is determined the output of the previous comparison. As a result, this technique reduces the energy consumption by 81.2% compared to the conventional DAC switching scheme. Due to the fact that, during the conversion, only one DAC array is switched

while in the other DAC array, there is no switching activities, the input common-mode voltage of the comparator is altered in each comparison. More specifically, the common-mode voltage is V_{CM} at the beginning of the conversion and gradually decreases to ground at the end of the conversion which can cause linearity problems for high resolution SAR ADCs [58]. This technique is very useful for low and medium resolution ADCs, since the comparator can handle the common-mode voltage variations at these resolutions. Beyond the 10-bit applications, in order to overcome this problem, the comparator requires a high common-mode voltage rejection which leads to additional power consumption and requires advanced analog circuitries.

To reduce the common-mode voltage variation issue, Sanyal and Sun [59] proposed a novel DAC switching scheme called as bi-directional single-side switching which uses both V_{REFN}, and V_{REFP} for switching. This switching scheme provides an 82.9% energy reduction compared to the conventional DAC switching scheme. Due to the fact that this switching scheme still requires one-side switching, a common-mode voltage variation cannot be totally eliminated and the performance of the SAR ADC is still limited by this variation.

In order to overcome the common-mode voltage variation, Zhu et al. [60] proposed a V_{CM}-based switching scheme. In this switching scheme, during the sampling phase, the top plates of the capacitors are connected to the V_{CM}, while the bottom plates of the capacitors are tied to input differential voltage in each DAC array. Following the sampling phase, the bottom plates of the capacitor in each DAC array are connected to the V_{CM} voltage instead of connecting them to either V_{REFP} or V_{REFN}. By connecting the bottom plates to V_{CM} the reset energy is totally eliminated, since this switching scheme does not switch back to capacitors to previous positions. In addition, the capacitors in each DAC array are symmetrically switched to ensure a constant common-mode voltage. This switching scheme reduces the overall power by 87.54 %, but at the cost of an additional reference driver for V_{CM} which can be a problem for high resolution SAR ADCs, since a precise third reference voltage is required during the entire switching steps. To avoid the additional reference driver,

Ginsgburg, and Chandrakasan [61] proposed a split capacitor switching scheme which divides the MSB capacitor into sub capacitor array. In this switching scheme, the MSB capacitor is formed with a group of binary-weighted capacitors which are either connected to V_{REFP} or V_{REFN} and when the comparison fails only the capacitors in the MSB capacitor array are switched back to previous positions and the rest of the capacitors do not need any switching to generate a voltage at the input nodes of the comparator. This switching scheme decreases the energy consumption by 68.8% while requiring reset energy, since for certain comparisons, the capacitors in the MSB capacitor array returns to previous positions which lead to reset energy. Compared to conventional scheme, this scheme does not require considerable amount of energy.

The switching schemes described above are the fundamental state-of-the art DAC switching schemes used for the SAR ADCs. Today, there are other DAC switching schemes which provides a great energy reduction and silicon area which are approximately 99.5% and 75% respectively. Table 3.1 summaries the current state-of-art DAC switching schemes.

Table 3-1 Current state-of-art DAC switching schemes according to their energy consumptions, occupied silicon area.

Switching method	**Average Switching energy (CV^2)**	**Energy saving (%)**	**Area reduction (%)**	**Extra reference voltage**	**V_{CM} variation**
Conventional	1363.3	0	0	No	0
Bi-directional [59]	234.2	82.9	75	Yes	$V_{REF}/4$
V_{cm}-based[60]	170.2	87.54	50	Yes	0
Monotonic[57]	255.5	81.2	50	No	$V_{REF}/2$
Split-cap [61]	425.7	68.8	0	No	0

In addition to these state-of-the-art switching schemes, there are other types of switching techniques such as detect-and-skip [54], however, it requires additional sub-capacitor arrays and circuits. In summary, V_{CM}-based switching scheme and split capacitor switching scheme are the most common methods that are used in state-of-art ADCs.

3.4 Proposed DAC Switching Schemes

In this thesis, 3 different DAC switching schemes are proposed to reduce the energy consumption of the DAC array and number of unit capacitors used for conversion.

3.4.1 First Proposed DAC Switching Scheme

The first proposed DAC switching scheme is a modified version of the V_{CM} –based DAC switching scheme. The conventional V_{CM}-based DAC switching scheme requires energy consumption in the second conversion cycle while the first conversion cycle do not consume energy. A considerable amount of switching energy during the conversion is consumed in the second conversion cycle. Figure 3-8 shows the sampling phase and first conversion cycle for a V_{CM}-based switching.

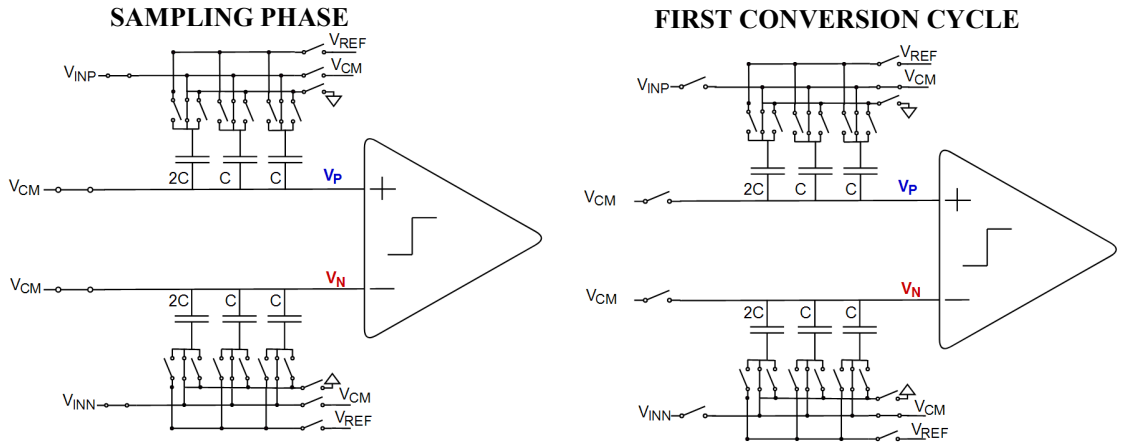


Figure 3-8 Sampling phase and first conversion cycle for a V_{CM}-based switching.

Following the sampling phase, the bottom-plates of the capacitors are connected to V_{CM} in both DAC array while the input nodes of the comparator are float resulting no energy consumption, since the voltage at the input nodes of the comparator is the summation of the sampled voltage and the voltage at the bottom-plate of the capacitor. In the second conversion cycle, the MSB capacitors in each DAC array are connected to either V_{REF} or ground depending on the result of the first conversion which requires considerable amount energy for the transition of the capacitors from V_{CM} to V_{REF}. In the first proposed scheme, in order to eliminate the energy consumption in the second conversion cycle, depending the first comparison result, in one side of the DAC array, the bottom-plates of the capacitors are connected V_{REF} while in the other DAC array, there is no switching. Figure 3-9 shows the proposed switching scheme for a 3-bit implementation. For the sake of simplicity, only the case where $V_{INP}>V_{INN}$ is analyzed.

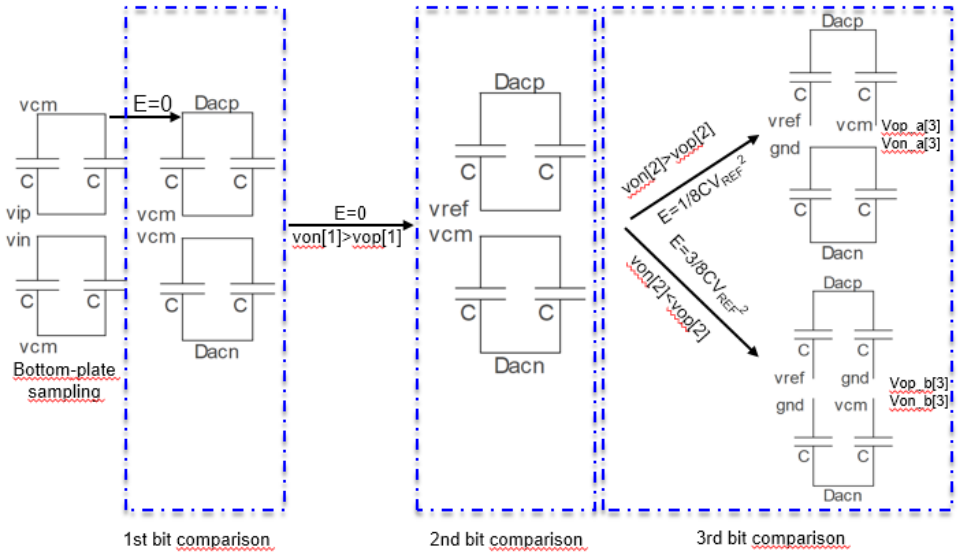


Figure 3-9. The proposed switching scheme for a 3-bit implementation.

Compared to the conventional V_{CM}-based switching scheme, the second conversion cycle and the last conversion cycle differs. In the second conversion cycle, depending on the result of the first conversion, the bottom-plates of the capacitors in one DAC array are connected to the V_{REF} while in the other DAC array, there is no switching activity. In the last conversion cycle, according to the previous conversion result, the bottom plate of the LSB capacitor which is used as dummy in the conventional switching scheme is either connected ground in one DAC array while in the other DAC array, no switching activities occur. This technique does not need any energy consumption, since the voltage at the input of the comparator is just a shifted version of the voltage at the bottom-plates. The energy consumption of a capacitor from the reference voltage can be expressed as

$$E_{0\to1} = \int_{0^+}^{Tp} iref(t)vref(t)dt = vref \int_{0^+}^{Tp} iref(t)dt \qquad (3.4.1)$$

where iref(t)=$dQ_C(t)/dt$, and charge continuity on a capacitor implies that $Q_C(0^+)= Q_C(0^-)$. As a result, the energy can be described as

$$E_{0\to1} = -vref \int_{0^+}^{Tp} \frac{dQ_C}{dt} dt = -vref \int_{Q_C(0^+)}^{Q_C(Tp)} dQ_C \qquad (3.4.2)$$

For the first MSB comparison, the energy consumption can be written as

$$E[0] = -vref \cdot C \cdot \left\{\left(V_{CM} + V_{inp} - V_{CM}\right) - \left(V_{CM} - \left(V_{inp} + V_{CM}\right)\right)\right\} \qquad (3.4.3)$$

which is simply zero. Same equation can be written for the second comparison and it can be seen that the net energy consumption in the second cycle is also zero.
In addition to energy consumption, the first proposed switching scheme uses LSB-down switching scheme which eliminates the (MSB-1) in the conventional V_{CM}-based switching resulting are reduction by 25% compared conventional V_{CM}-based

switching scheme. Although, this switching scheme save energy consumption compared to conventional V_{CM} –based switching scheme there is a common-mode voltage variation from V_{CM} to $1.5V_{CM}$ in the second cycle which may degrade the performance of the comparator. Since, the common-mode variation is constant, the comparator can designed for two different common-mode voltage to eliminate any non-idealities coming from this variation. However, this solution requires additional circuits for the comparator. As a result, the first proposed switching scheme can be safely used up to 10-bits. Beyond the 10-bits, a new DAC switching scheme is required.

3.4.2 Second Proposed DAC Switching Scheme

In the second proposed switching scheme, the common-mode voltage is nearly constant while reducing the energy and silicon area compared to the conventional and state-of-the art switching schemes. The second proposed switching technique modifies the first proposed DAC switching scheme in order to sustain the common-mode voltage of the DAC array nearly constant. As it was mentioned in the previous sub-section, in the first switching scheme, in the second comparison cycle, the common-mode voltage shifts from V_{CM} to 1.5 V_{CM} which can be problematic for the comparator. The second proposed switching scheme aims to solve this problem at the expense of energy consumption in the second conversion cycle. Compared to the first proposed DAC switching scheme, in the second cycle of the conversion, instead of connecting V_{REF} reference voltage to the bottom plates of the capacitor in one side of the DAC array, V_{REF} and ground are connected symmetrically to the bottom plates of the respective DAC arrays. Figure 3-10 shows the second proposed switching scheme for 4-bit implementation. DAC_P is the DAC array where V_{INP} is sampled and DAC_N is the DAC array where V_{INN} is sampled. The sampling phase and the first conversion cycle is same with the first proposed switching scheme which are illustrated in (a) and (b) respectively. In the second conversion cycle, if $V_N > V_P$ meaning that the differential voltage is positive and shown in (c), the bottom plate of

the MSB capacitor in the DAC_P is connected to V_{REF}, while the bottom plate of the MSB capacitor in the DAC_N is connected to ground. In the third conversion cycle, if $V_N > V_P$, the bottom plate of the (MSB-1) capacitor in DAC_P is connected to V_{REF} and the bottom plate of the (MSB-1) capacitor in DAC_N is tied to ground. In contrast, if $V_P > V_N$ in the second conversion cycle which is illustrated in (d), the bottom plates of the capacitors in both DAC arrays are connected to V_{CM} while the bottom plates of the (MSB-1) capacitors are connected to V_{REF} and ground respectively. Hence, the second, and a part of the third of the second proposed conversion cycle differ from the first proposed DAC switching scheme.

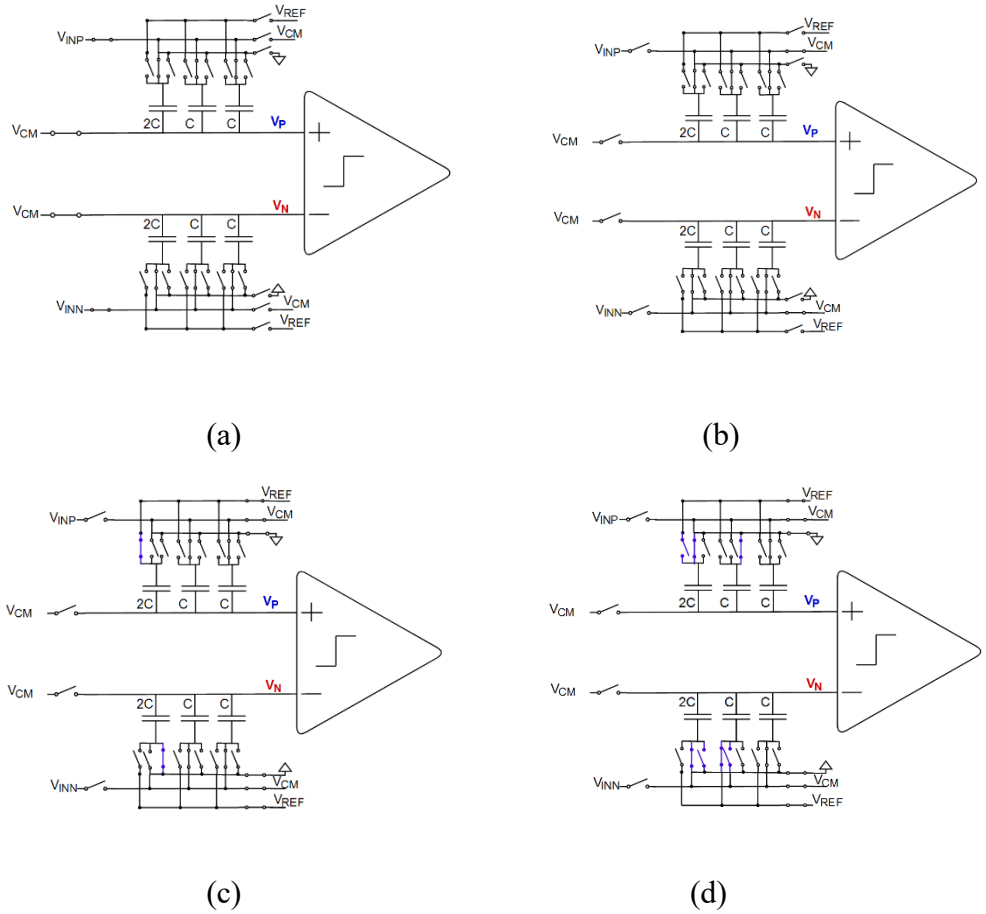


Figure 3-10. The second proposed switching scheme for 4-bit implementation (a) sampling phase, (b) first conversion cycle, (c) second conversion cycle when, $V_N > V_P$ in the first comparison, (d) third conversion cycle, when $V_P > V_N$ in the second comparison cycle.

Compared to the conventional V_{CM}–based switching scheme approach, 1 MSB capacitor is eliminated in the second proposed DAC switching scheme resulting a reduction by 75% compared to the conventional switching scheme and 25% compared to the conventional V_{CM} based switching scheme. Reducing the number of capacitors is very important for the high-speed ADCs, since the MSB capacitor determines the worst settling time of the DAC array. Note that, although the second proposed DAC switching scheme is not as power efficient as the first proposed DAC switching scheme, the common-mode voltage in the second scheme is nearly constant while in the first proposed scheme, the common-mode voltage is shifted from V_{CM} to $1.5V_{CM}$ which is not good for the comparator performance.

3.4.3 Third Proposed DAC Switching Scheme

In the previous two proposed DAC switching scheme, during the entire switching steps, there are 3 different reference voltages which are V_{REF}, ground and V_{CM} to perform the conversion. For high resolution SAR ADCs, the performance depends on the precision of these reference voltages. The noise and settling of the reference voltage are one of the most important limitations which affects the performance of the SAR ADC. In order to overcome these limitations, the DAC array should have minimum number of reference voltages. The third proposed switching scheme aims to reduce the number of reference voltage to achieve high resolution SAR ADC. Figure 3-11 shows the SAR ADC architecture for a typical 10-bit implementation. The SAR ADC architecture for the third proposed DAC switching scheme is different than the SAR architecture for the first two proposed switching schemes. In this SAR ADC architecture the MSB capacitors are formed by using binary weighted capacitors which are called as split capacitor array. In the third proposed DAC switching scheme, the first comparison is performed without using the DAC arrays. Before the sampling phase, the differential input voltage is directly connected to the main comparator. First comparison is performed without any sampling and switching activity and the output of the first comparison determines the connections of the

DAC arrays for the sampling phase. In the first comparison if $V_P > V_N$, the differential voltage is positive and V_{INP} is connected to DAC_P, while V_{INN} is tied to DAC_N.

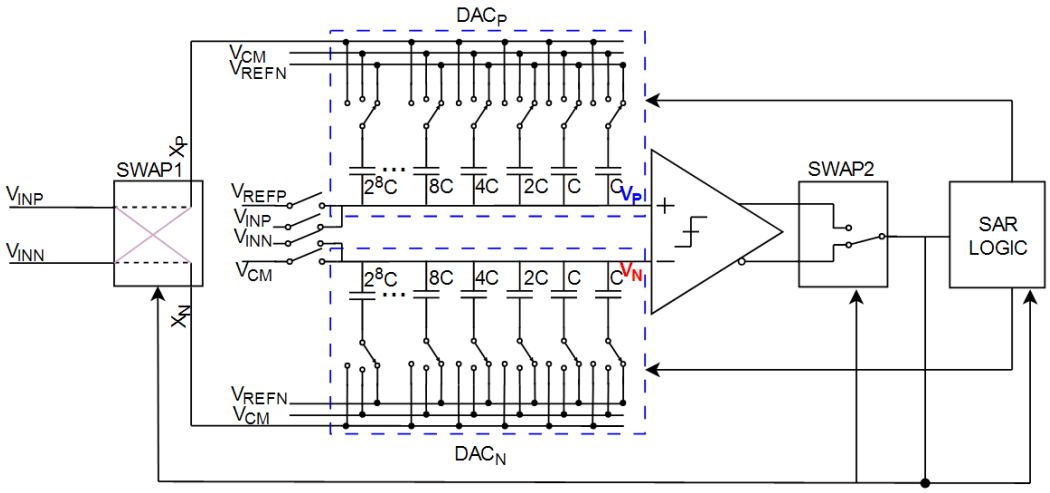


Figure 3-11. The SAR ADC architecture for a typical 10-bit implementation.

Therefore, the first comparison does not only determine the first bit, but also the connection of the differential input voltage to the DAC arrays. In addition to change the polarity, the output of the comparator is also altered according to the output of the first comparison to ensure the polarity of the conversion.

Consider the case where $V_{INP} > V_{INN}$ and thus $V_P > V_N$. The V_{INP} is connected to the DAC_P and V_{INN} is tied to DAC_N. In the sampling phase, apart from the previous state-of-the-art DAC switching schemes, the top plate of the DAC_P and DAC_N are connected to V_{REF} and V_{CM} respectively. At the end of the sampling phase, the voltages on the capacitors becomes V_{REF}-V_{INP} and $V_{CM} - V_{INN}$. In the second conversion cycle the bottom plate of the each capacitor in DAC_P and in DAC_N are connected to ground and V_{CM} respectively and the actual conversion starts. Figure 3-12 shows the proposed DAC switching scheme for 4-bit implementation.

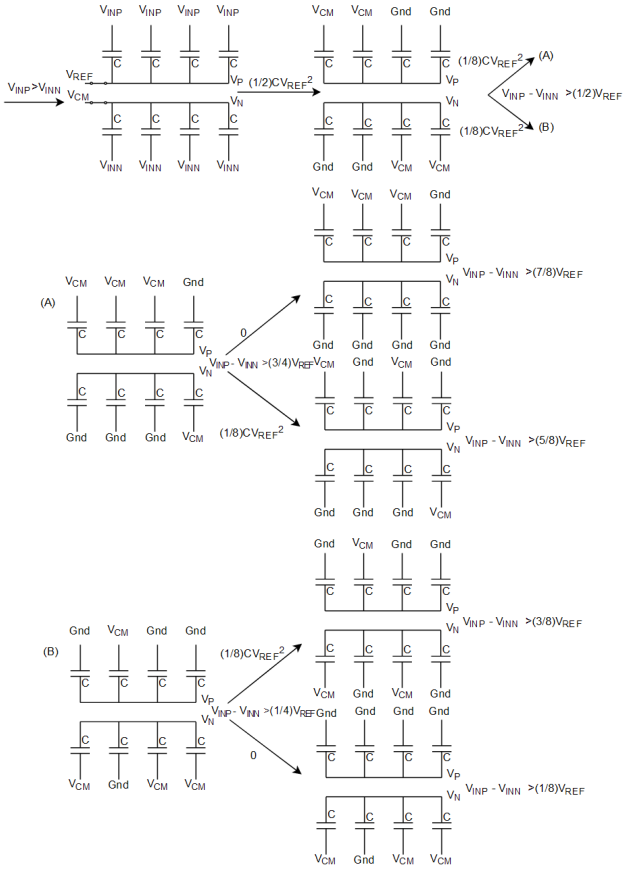


Figure 3-12. The proposed DAC switching scheme for 4-bit implementation.

In the second conversion, the bottom plate of the MSB capacitor in DAC_P is connected to V_{CM}, while the bottom plate of the rest of the capacitors in the same array are not altered. On the other hand, the bottom plate of the MSB capacitor in DAC_N is connected to ground and there is no switching activity for the other capacitors in the same array. The voltages at node V_P and V_N becomes;

$$V_P[1] = \frac{3}{2}V_{CM} - V_{INP} \tag{3.4.4}$$

$$V_N[1] = \frac{1}{2}V_{CM} - V_{INN} \tag{3.4.5}$$

A comparison is performed and depending on the output, there are different possibilities for the connection. If $V_N > V_P$, the (MSB-1) capacitor in the DAC_P is connected to V_{CM} and the (MSB-1) capacitor in the DAC_N is tied to ground. In

contrast if $V_P > V_N$ the largest capacitors in the MSB capacitors in both DAC_P and DAC_N switch back to previous positions. The conversion continues until the last conversion. In the last conversion, $V_N > V_P$ the one of the LSB capacitor is connected to ground while there is no switching activity in the other array. If the conversion fails the LSB capacitors in the MSB capacitors in both DAC_P and DAC_N returns to previous positions.

This switching technique eliminates the third reference voltage which is very important for high resolution SAR ADCs. In addition to the elimination of the third reference voltage, the proposed DAC switching scheme reduces the energy consumption and silicon area by 93.7% and 75% respectively. Besides that, the proposed switching scheme reduces the number of switches and relaxes the DAC control logic to provide faster operation and low power consumption. It shows that, the proposed switching algorithm is very suitable for high resolution such as 14-bit SAR ADCs.

Another concern in the DAC design is the linearity. The linearity of the DAC array was discussed in Chapter 2. However, all of the proposed switching schemes in this thesis relax the linearity requirements compared to the conventional architectures. One of the drawback of the SAR ADC is that the converter does not guarantee an intrinsic monotonicity resulting linearity problems. Process variations are the main reason of the linearity errors occurred in the DAC array. For conventional DAC architecture, the transition from 01111…11 to 1000…00 is the most important transition during the conversion. The random variation of the value of the unity capacitance with variance causes to a differential nonlinearity (DNL) at this critical transition. For the first proposed ADC, the first most significant bits are not affected by the mismatch, since there is no capacitor division while determining these bits. As a result, the worst case DNL occurs at 7/8 V_{FS}, and 1/8 V_{FS} respectively and the linearity equation is written as;

$$\sqrt{2}\varepsilon_C \cdot 2^{\frac{N-2}{2}} < 1/2 \tag{3.4.6}$$

which reduces the minimum value of the unit capacitor in the DAC array in terms of matching requirement. On the other hand, the second and third proposed switching scheme relaxes the first most significant bit conversion, since in the first conversion cycle, there is no capacitive division to perform the conversion resulting the worst case DNL at 1/4 V_{FS}, and 3/4 V_{FS} relaxing the required minimum value of an unit capacitor by $\sqrt{2}$ compared to the conventional architecture.

In addition to the energy consumptions of the DAC switching schemes, Figure 3-13 shows the power consumption of the common DAC switching schemes with respect to the overall power consumption of the SAR ADC. For the resolution below 12-bit, the power consumption of the DAC is approximately equal to the 1/4 of the overall power consumption. It means that, the power consumption is dominated by the other components. On the other hand, for the resolutions above 12-bit, the power

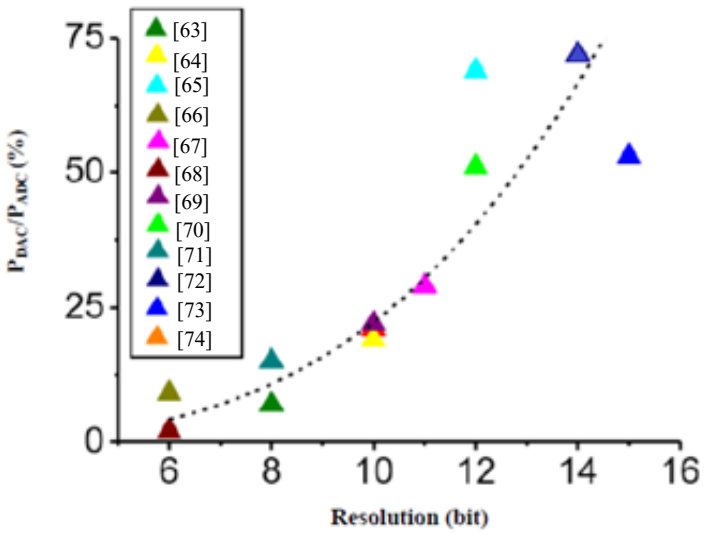


Figure 3-13. Power consumption of the common DAC switching schemes with respect to the overall power consumption of the SAR ADC [62].

consumption of the DAC dominates. As a result, it is critical to reduce the power consumption of the DAC for the proposed SAR ADC. In the proposed DAC ADC architecture, the power consumption of the SAR ADC is approximately 1.8 mW while the overall power consumption is 6.3mW including the input drivers and it

shows that the power consumption of the DAC does not dominate the overall power consumption.

3.5 Comparison with state-of-the-art DAC switching Schemes

Table 3.2 shows the comparison of the proposed switching schemes with published techniques for 10-bit implementation. The first proposed DAC switching scheme provides great energy reduction among the proposed switching schemes in this thesis while leading to a large common-mode voltage variation. This type of switching scheme is suitable for the resolutions up to 10-bits. Beyond the 10-bits, the other two proposed DAC switching scheme can be used to perform conversion. The second switching scheme reduces the switching energy and silicon area compared to V_{CM}-based and conventional schemes which are the most common techniques used in the literature. The second proposed scheme requires additional reset energy in the second conversion cycle for certain differential input voltages resulting larger switching energy compared to the first proposed switching scheme. The third proposed scheme eliminates the third reference voltage, reduces energy and silicon area, and decreases the number of switches used for switching activity while providing simple DAC control logic. Compared with the state-of-the art existing DAC switching schemes, the third proposed switching scheme can be a better candidate for the high resolution SAR ADCs, since it does not require the third reference voltage and sustains nearly constant common-mode voltage. On the other hand, the third proposed scheme requires more complex routings in the layout compared to the first and second DAC switching schemes, since more independent unit capacitors are used to implement the capacitive DAC array. As a result, this proposed switching scheme is suitable with architectures that does not have any area limitation and requires high resolution such as 14-bit. In this thesis, there is an area limitation and the routings are very important for achieving 14-bit performance. In contrast the second proposed scheme needs simple routings in the layout compared to the third proposed scheme, since, less independent capacitors are used to implement the DAC. For these reason

mentioned above, the second proposed DAC switching scheme is used in the proposed SAR ADC architecture.

Table 3-2 Comparison between the proposed DAC switching scheme, and the state-of-the-art switching scheme.

Switching method	**Average Switching energy (CV^2)**	**Energy saving (%)**	**Area reduction (%)**	**Extra reference voltage**	**V_{CM} variation**
Conventional	1363.3	0	0	No	0
Bi-directional [59]	234.2	82.9	75	Yes	$V_{REF}/4$
V_{cm}-based[60]	170.2	87.54	50	Yes	0
Monotonic[57]	255.5	81.2	50	No	$V_{REF}/2$
Split-cap [61]	425.7	68.8	0	No	0
First Proposed scheme	**70**	**95**	**75**	**Yes**	**$V_{REF}/4$**
Second Proposed scheme	**115**	**92**	**75**	**Yes**	**$V_{REF}/1024$**
Third Proposed scheme	**85.7**	**93.7**	**75**	**No**	**$V_{REF}/1024$**

3.6 Conclusion

In conclusion, this chapter illustrates the DAC architecture and explains the proposed DAC switching schemes. In this thesis, a split capacitor DAC array with 1 bridge capacitors which has an integer value is used to achieve a high resolution performance such as 14-bits. In order to use a bridge capacitor with an integer value, additional compensation capacitors are required which do not alter the charge equation. The gain error due to the modifications is very small which does not degrade the performance of the DAC array. In this thesis, three different DAC switching schemes are proposed and compared with the state-of-the-art techniques in the publications. The results shows that the second and third proposed switching scheme can be used for high resolution applications. The second switching algorithm sustains low common-mode voltage variation while providing a great energy and area reduction compared to the conventional architecture and requiring a third reference voltage and simple routing in the layout. The third proposed switching scheme eliminate the third reference voltage, decrease the number of switches used in the DAC, and reduces the energy consumption and area compared to the conventional architecture while sustaining a nearly constant common-mode voltage. The third proposed switching scheme requires more complex routings in the layout compared to the second proposed scheme which may result unwanted parasitic capacitance in the layout.

CHAPTER 4

COMPARATOR DESIGN

The comparators are the main components of the SAR ADCs performing the comparison. The performance of the comparators affect the result of the comparison which may increase or decrease the performance of the overall SAR ADC. In this chapter, the design of the comparator will be investigated. Section 4.1 gives an introduction to the comparators. Section 4.2 reviews the prior art. Section 4.3 discusses the proposed 2-level dynamic latch and Section 4.4 illustrates the coarse comparator by using the proposed 2-level latch. Section 4.5 compares the proposed coarse comparator with the state-of-the-art comparators in the publications. Section 4.6 analyzes the proposed fine comparator. Section 4.7 concludes the chapter.

4.1 Introduction

As mentioned above, the comparators are the heart of the SAR ADCs and it performs the comparison between the differential voltages at the output nodes of the DAC arrays. In general, the comparators can be divided into main groups which are static and dynamic comparators. Static comparators are the circuits that always demanding current even when there is no conversion. In other words, the static comparators consume power during the idle state. This type of comparator has a gain stage consisting of an amplifier followed by a latch to saturate the input to the one of the supply rails which are supply voltage and ground respectively. The static comparators are commonly used in the applications required high-resolution such as 14-bit. In the early comparators, even below the 10-bits, this kind of architecture was also used to perform the conversion. Today, dynamic comparators replace the static comparators for the applications require low or medium resolution, since these types

of comparators consume power during the conversion and it does require any power in the idle mode.

As the semiconductor technology is developing more and more, the researches have pushed the performance limits of the ADCs resulting low-power and high-performance ADCs with the advanced technology nodes and low supply voltage. Today, a Walden Figure of Merit below a 1fJ/conversion-step can be achieved for the SAR ADCs by using advanced technology node and extremely low supply voltage. In these state-of-the art SAR ADCs, the power consumption is dominated by the comparator, since the novel DAC switching schemes and simple SAR control logic significantly reduces the power consumption of the remaining circuits such as DAC and control logic [75-77]. In addition, the power consumption of the comparator affects the noise performance of a comparator which is a challenging issue especially under low supply voltages. The first type of dynamic comparators was the StrongArm latch which is the most commonly used architecture in current SAR ADCs. This type of comparator called as StrongArm latch does not require static power consumption and provides a fast decision cycle by using a positive feedback architecture [78-80]. Figure 4-1 shows a typical StrongArm Latch.

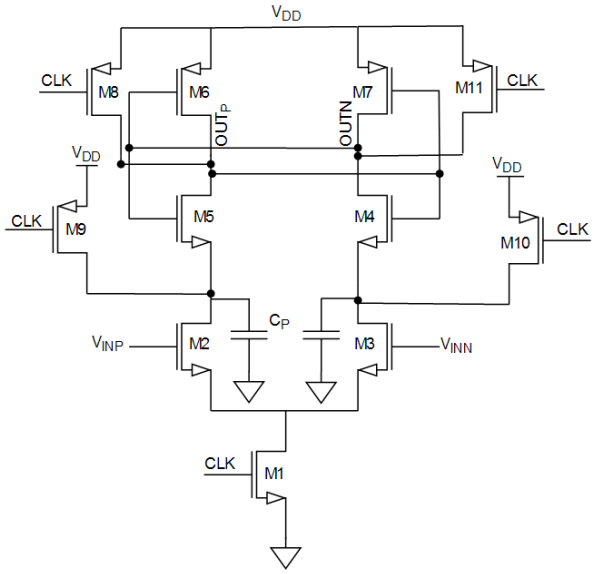


Figure 4-1. Typical StrongArm Latch [78-80].

The positive feedback circuit is cascaded on a differential amplifier which requires large voltage headroom discussed in [80] and [81]. In addition to voltage headroom limitation, due to the cascading architecture, this architecture suffers from a kick-back noise during enabling the positive feedback for fast decision. The kickback noise may degrade the performance of the comparator for small differential input voltages. In order to overcome this limitation, an architecture in [81] was proposed by separating the differential input stage from the latch. Figure 4-2 shows the proposed comparator in [81] called as Double-Tail Latch comparator. In this architecture, the pre-amplifier is separated from the latch to eliminate the kickback noise. The double-tail latch comparator has two independent tail transistors that are used for providing independent common-mode currents. Before starting the conversion, the output nodes of the pre-amplifier are reset to V_{DD}. When the conversion is initiated, the tail transistor becomes ON and the output nodes of the pre-amplifier completely discharge to ground at the end of the conversion. The energy consumption during the operation is equal to $2 \cdot C_P \cdot V_{DD}$ where C_P is the capacitance at the output of the pre-amplifier. The capacitance C_P also determines the output noise of the pre-amplifier and input referred noise [75]. Thus, the size of these capacitance should be properly optimized to achieve a low-noise while consuming low-power. The power consumption of the Double-Tail latch comparator is due to the discharging operation of the capacitors at the output nodes of the pre-amplifier. If there is a way to hinder the complete discharging, the power can be reduced. The following the section will discuss the state-of-the-art comparators published in the literature.

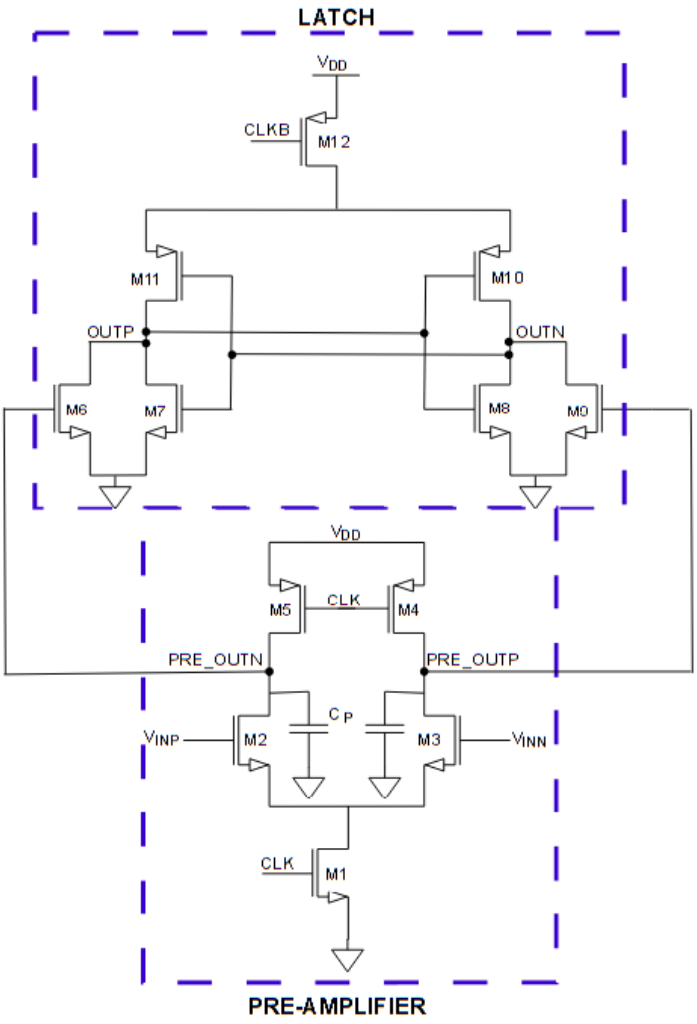


Figure 4-2. Double-Tail Latch type comparator [81].

4.2 Existing state-of-the-art Comparators

The first state-of-the-art comparator is the StrongArm Latch which is illustrated in Figure 4-1. The StrongArm latch operates as follows. During the reset phase, the transistors M8, M9, M10, and M11 reset the respective output nodes to V_{DD}. At the end of the reset phase, the conversion phase is initiated and the tail transistor turns ON. Depending on the differential input voltages, the output nodes discharges at a different rate which is sensed by the positive feedback loop to make a fast decision.

This first type of dynamic amplifier suffers from constant energy consumption and kickback noise. In order to alleviate these problems, double-tail latch type comparator was proposed shown in Figure 4-2. In this architecture, the pre-amplifier stage and the latch stage starts at the same time which is not an energy-efficient approach, since, at the beginning of the conversion, the differential voltage at the output of the pre-amplifier is zero and the latch cannot make a decision under this circumstance. For this reason, this architecture is not commonly used for the applications requiring low-power and medium to high-resolution such as 14-bit. In order to overcome this issue, Elzakker et al. in [75] designed a modified version of this comparator. Figure 4-3 shows the dynamic latch comparator proposed by Elzakker et al. In this architecture, there are two extra pmos transistors M12 and M13 to start the latch when the output nodes are below the certain voltage level, resulting energy saving compared to the conventional Double-Tail latch type comparator.

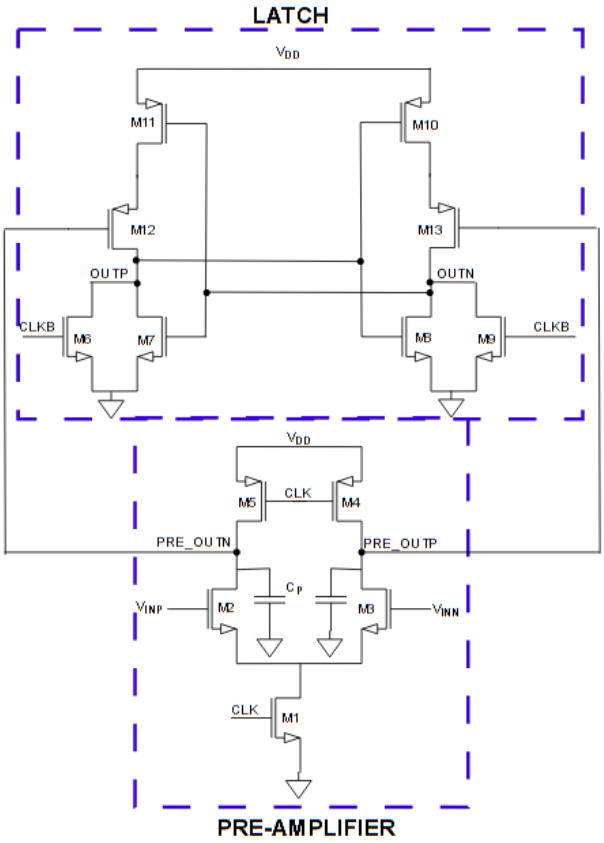


Figure 4-3. Dynamic latch comparator proposed by Elzakker et. al in [75].

More specifically, the conversion starts with discharging the output nodes of the pre-amplifier called as PRE_OUTN and PRE_OUTP respectively. When the voltage at the gate of the M12 and M13 is sufficiently low, these transistors turn ON and the second stage of the circuit operates to make a decision. This architecture eliminates the wasted energy at the beginning of the conversion which is very important for the low-power applications.

In order to save more energy during conversion, the comparator called as dynamically-biased integration comparator was proposed in [82], while achieving more gain. The proposed architecture has same latch circuit, but the novelty is in the pre-amplifier stage. Figure 4-4 shows the pre-amplifier stage of the proposed comparator in [82].

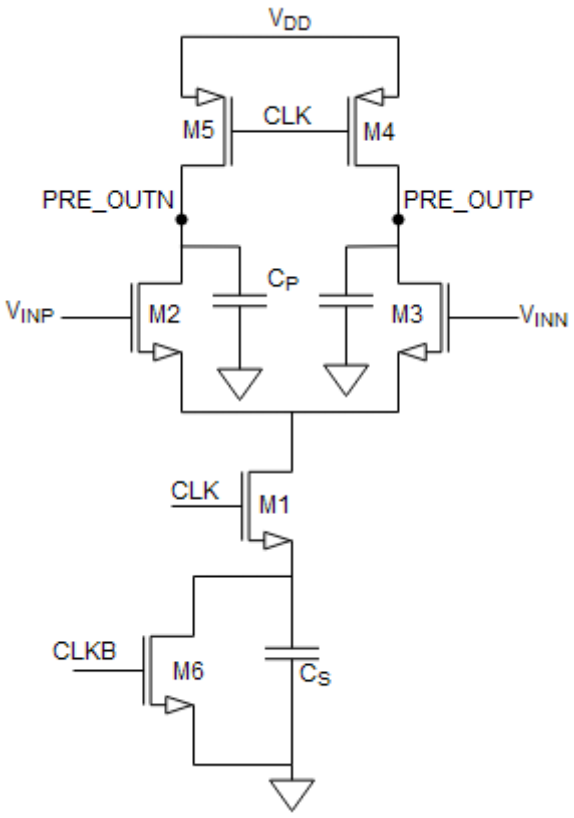


Figure 4-4. Pre-amplifier stage [82].

During the conversion phase, the output nodes of the pre-amplifier stage called as PRE_OUTN and PRE_OUTP respectively are discharged. As the current flows through the capacitor C_S the voltage at the source of MW and M3 starts to increase, since the capacitor C_S is charged. As the source voltage of a transistor is charged up, the overdrive voltages of these transistors starts to decrease, since the gate voltage is constant. This result brings two important benefits. The first benefit is that the output nodes of the pre-amplifier cannot completely discharge, since the transistors M2 and M3 turn OFF at the quenching point which is V_{GS}-V_{TH}. The second benefit is that during the conversion, while the overdrive voltage of the each input transistor decreases, the gain of the amplifier increases, since g_m/I_D increases during the conversion. As a result, this architecture provides good gain and noise performance while achieving 3 times improvement on the energy efficiency compared to the dynamic comparator.

In order to further the efficiency of the dynamic bias comparator, an inverter based floating amplifier was proposed in [83]. The dynamic inverter based floating amplifier uses the complementary part of the nmos differential stage and forms an inverter to implement the comparator. Figure 4-5 shows the dynamic floating inverter amplifier proposed in [83].

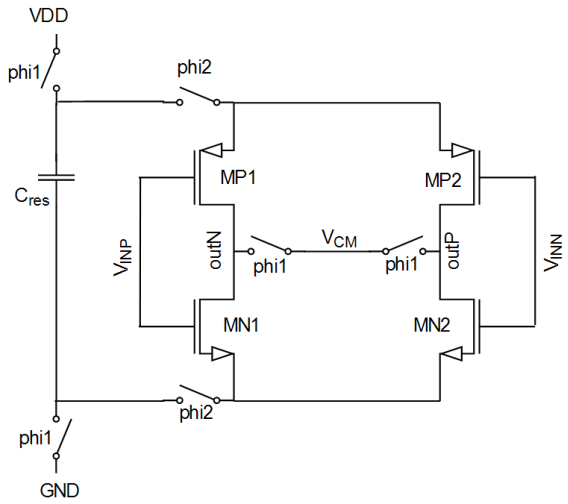


Figure 4-5. Dynamic floating inverter based amplifier proposed in [83].

The amplifier has two different phases which are the reset phase and the amplification phase. During reset phase, the reservoir capacitor is connected to the supply rails, and it is charged to V_{DD}. At the same time the outputs are reset to V_{CM} voltage to start a new conversion.

Following the reset phase, the amplification phase is initiated. During the amplification phase, the reservoir capacitor is connected to the circuit and the required bias voltage demanding by the circuit is supplied by the reservoir capacitor. The bias current flowing through the circuit is determined by the input common-mode voltage of the input transistors labelled as MN1, MN2, MP1 and MP2. The bias points of these transistors in the proposed design equal to 0.9V. As a result, the amplifier does not need any extra circuit to provide the bias voltages to the input transistors. During the amplification phase, the voltage at the sources of the nmos transistors increases, while the voltage at the sources of the pmos transistors decreases. As a result, the overdrive voltage of the nmos, and pmos transistors decreases. Let $G_m = g_{m,n} + g_{m,p}$ which is the overall transconductance of the circuit, and $g_{m,n}$, and $g_{m,p}$ are the transconductance of the nmos and pmos transistors respectively. At the beginning of the amplification phase, G_m / I_D of the amplifier is doubled compared to the conventional differential amplifier thanks to the current reusing approach. The same common-mode current is shared between pmos and nmos transistors. Due to the fact that, the overdrive voltages of the transistors decrease, G_m / I_D is increased and boosted by the amplifier, resulting a large improvement in the power efficiency.

The dynamic floating inverter based amplifier with reservoir capacitor brings some advantages. Firstly, only the differential charge is integrated on to the output capacitors at the output nodes outN and outP respectively, since the circuit is separated from the supply rails during the amplification phase. As a result, theoretically, the common-mode dc current flows through the circuit and ends at the negative side of the reservoir capacitor. Thus, the common mode voltage stays constant during the amplification phase and remove the common-mode drop limitation of the amplifier. In the conventional inverter based amplifier, small

mismatches in the bias transistors lead to different common mode currents. Thus, the common mode voltage at the output is severely affected and it requires advanced common-mode feedback circuits to stabilize the output common-mode voltage. The dynamic floating inverter based amplifier does not need any complex common-mode feedback circuit. A simple switches that reset the output nodes to common-mode voltage is sufficient for the proper operation. In addition, the reservoir capacitor does not only remove the process-voltage-temperature (PVT) variations but also provide a degeneration which reduces the power consumption of the amplifier and increase the gain of the amplifier during the amplification phase. In the next sub-section the pre-amplifier gain analysis will be investigated.

4.2.1 Theoretical Dynamic Floating Inverter Amplifier Gain Analysis

For small input differential voltages, nmos and pmos input transistors are biased in the vicinity of the weak inversion region at the beginning of the comparison. The transconductance of the transistor in weak inversion is expressed as:

$$g_m(t) \approx \frac{I_D(t)}{n \cdot U_T} = \frac{I_{amp}(t)}{2 \cdot n \cdot U_T} \tag{4.2.1}$$

where I_D (t) is the instantaneous current of the transistor, n is the weak inversion slope factor, and U_T is the thermal voltage which is equal to kT/q. If the output impedance of the input transistors is ignored, the differential amplifier output voltage can be approximated as:

$$\Delta V_{outn,DM}(t) = \frac{\int_0^t \Delta V_{I,DM} \cdot G_m(\tau) d\tau}{C_{outn}} \approx \frac{\Delta V_{I,DM} \int_0^t I_{amp}(\tau) d\tau}{n \cdot U_T \cdot C_{outn}} \tag{4.2.2}$$

The tail current I_{amp} (t) can be expressed as:

$$I_{amp}(t) = \frac{I_{amp}(0^+)}{1 + \frac{I_{amp}(0^+)}{n \cdot U_T \cdot C_{tail}} t} \tag{4.2.3}$$

The $I_{amp}(0^+)$ is the tail current at instant $t=0^+$ when the comparator starts. For a small differential input voltage $I_D(t) \approx (½)\ I_{amp}(t)$. The source voltage of the input transistors difference $\Delta V_s(t)$ can be written as;

$$\Delta V_S(t) = \frac{\int_0^t I_{amp}(\tau)d\tau}{C_{tail}} = n \cdot U_T \cdot \ln(1 + \frac{I_{amp}(0^+)}{n \cdot U_T \cdot C_{out}} t) \qquad (4.2.4)$$

where $C_{tail} = 2\ C_{reservoir}$ in the ac equivalent model, the integration gain is

$$A_v(T_{int}) = \frac{\int_0^{Tint} V_I \cdot G_m(\tau)d\tau}{V_I \cdot C_{out}} = \frac{2 \cdot C_{res} \cdot \Delta V_S(T_{int})}{n \cdot C_{out} \cdot U_T} \qquad (4.2.5)$$

where V_I is the differential input voltage, and T_{int} is the time period for the amplification phase.

4.2.2 Theoretical Dynamic Floating Inverter Amplifier Noise Analysis

In the floating inverter amplifier, the input differential pairs contribute $S_i(t) = 8qI_D(t)$. The mean square noise voltage generated at the output is expressed as

$$\sigma^2(t) = \frac{4q \cdot C_{reservoir}}{C_{out}^2} \Delta V_S(t) \qquad (4.2.6)$$

The input-referred noise at the end of the amplification phase can be written as,

$$\sigma^2(T_{int})\ \frac{2nkT}{C_{reservoir} \cdot \Delta V_S(T_{int})} \cdot \frac{I_D}{G_m} \qquad (4.2.7)$$

The input-referred noise is inversely proportional to G_m/I_D, and $C_{reservoir}$ and $\Delta V_S(Tint)$ provides larger gain.

4.2.3 Parasitic Capacitance Impact

In the simulation, the reservoir capacitance does not have any parasitic and it provides an isolated voltage domain for robust operation. However, in reality, with the parasitic capacitance to the supply, there is a common-mode transfer function. In

the proposed design, a symmetric MIM capacitor is used for implementation of the $C_{reservoir}$. The induced parasitic common-mode current due to the parasitic capacitors can be expressed as;

$$I_{P+}(t) - I_{P-}(t) = I_{CM}(t) \tag{4.2.8}$$

The induced current causes a change in the output common-mode voltage.

$$\Delta V_{out,CM}(t) = -(\Delta V_{S+}(t) + \Delta V_{S-}(t)) \cdot \frac{C_p}{C_{out}} \tag{4.2.9}$$

Due to the fact that, ΔV_{S+} / ΔV_{S-} is proportional to the input common-mode voltage, the output common mode voltage change can be expressed as:

$$\Delta V_{out,CM} \approx -2 \cdot \Delta V_{I,CM} \cdot \frac{C_P}{C_{out}} \tag{4.2.10}$$

4.3 Proposed 2-level Dynamic Latch

Following the pre-amplifier stages, a latch is used to determine the output of a comparison. The basic topology for a simple latch is called as Strong-arm latch topology which was mentioned in the previous section. This topology can be used as a sense amplifier or comparator. It was first introduced by Toshiba's Kobayashi et al. [78], and later used in Digital Equipment Corporation's StrongArm microprocessors [79-80]. In order to explain the proposed 2-level dynamic latch, the operation of this latch should be investigated in detail. Figure 4-1 shows the typical StrongArm latch comparator. The operation of the StrongArm latch is as follows;

There are three main phases in the comparator. These phases are reset phase, amplification phase, and regeneration phase respectively.

In the first phase, the clock CK is low, and all internal and output nodes are reset to supply voltage V_{DD} by charging the parasitic capacitors at these nodes.

In the second phase, the clock CK goes high, turning off the charging transistors M8, M9, M10 and M11. The differential pair M2 and M3 starts to draw current in

proportion to input differential voltage V_{INP}-$V_{INN.}$ In this phase M4, and M5 are initially OFF and the parasitic capacitors at the drain of M2 and M3 discharges. As these nodes fall from V_{DD}, a differential voltage proportional to V_{INP}-V_{INN} is generated during the amplification phase, which lasts the internal nodes reach to the quenching point which is V_{DD}-$V_{TH\,4,\,5}$. After this point, the amplification phase ends and the regeneration phase starts. During the amplification phase, the voltage gain is approximately given by

$$A_V = (2 \cdot g_{m2,3} \cdot V_{TH4,5})/I_{SS} \tag{4.3.1}$$

where ISS is the tail current flow through M1.

The third phase is the regeneration phase. At the end of the amplification phase, M4 and M5 turn on and the output nodes OUTP and OUTN starts to fall from V_{DD}. Initially, the transistors M6 and M7 are turned OFF. When the output nodes of the comparator reach to a quenching point VDD-$|V_{THP\,6,\,7}|$ M6 and M7 turn on and the two back-to-back inverter start to operate together in a positive feedback loop. While in the regeneration phase, the drain of the input transistors M2 and M3 are almost zero putting these transistors into the triode region. In this phase, the transistors M4, M5, M6, and M7 are turned ON and, one output is pulled back to VDD, while the other output drops to zero by M6 and M7 and the comparator makes a decision. The total power consumption of the comparator is approximated as:

$$P = 2 \cdot f_{CLK} \cdot C_P {V_{DD}}^2 + f_{CLK} \cdot C_x {V_{DD}}^2 \tag{4.3.2}$$

In addition to this power consumption, the clock path also draws a power of f_{CLK} C_{CLK} VDD^2. Before starting to design, there are some important observations from the StrongArm topology. Firstly, the precharging action occurs in the reset phase keeps the differential pair M2 and M3 in saturation during the amplification phase and allows the input transistors to provide a gain. Secondly, the precharging actions

reset the output nodes of the comparator and drain of the input transistors and equalize them to same voltage to suppress the dynamic offset. In the early design of the StrongArm latch, the drain of the input transistors M2 and M3 are not precharged to VDD. For this reason, the comparator can suffer from the dynamic offset in the next cycle. As a result, precharging is an important issue for this type of the comparator.

In this thesis, the comparator operates at 160MHz and it has 14-bit resolution for a 3.6V input range. In other words, the least significant bit (LSB) voltage should be 219 μV. The noise of the latch should be lower than 0.5 LSB voltage and the power consumption should be as low as possible. Normally, the StrongArm topology is a full comparator itself and it does not require any gain stage. However, for high resolution, low-power and low-noise applications, there are some issues about the StrongArm topology.

Firstly, the power consumption of the StrongArm latch is too much when achieving 14-bit resolution for 3.6V input range. More specifically, before starting to the proposed design architecture a StrongArm topology comparator was designed. In order to operate at 160MHz, the parasitic capacitances at the drain of the input transistors and output of the comparator are as much as small. To decrease these parasitic capacitances, the device width should be kept as much as small while concerning the limitations such as noise. Comparators in the ADCs, are typically limited by the thermal noise which is dominant over the flicker noise at high frequencies. In order to decrease the thermal noise in the StrongArm latch comparator, the input differential pair transistors should be wide and the power should be high to obtain 61 uV noise level (0.5LSB). For the noise analysis, the thermal noise contribution of the differential pair is dominant compared to the other transistors in the circuit. The power spectral density (PSD) of the thermal noise current for the differential pair (M2/M3) in strong inversion is [65].

$$\overline{V^2_{in,n}} = \frac{(V_{GS}-V_{THN})_{2,3}}{VTHN} * \left[\frac{4kT\gamma}{C_{outn,outp}} + \frac{(V_{GS}-V_{THN})_{2,3}}{VTHN}\frac{kT}{2C_{outn,outp}}\right] \qquad (4.3.3)$$

In order to decrease the input-referred noise of the latch, (gm/I_D) should be improved. The straight forward method is to increase the sizes of the input differential pair However, large devices are slow, and so there should be balance between the noise and the speed. The second method is to increase the gate-overdrive voltage. In order to increase the overdrive voltage while keeping the size constant, gm can be increased. The third method is to decrease the common mode current ID. In general, (gm/ID) improvement has a positive impact on the noise. In addition, to decrease the noise further, additional capacitors can be added to the drain of the input transistors M2 and M3. For a 50uV noise in the StrongArm latch, Table 4-1 shows the required width, and length of the transistors.

Table 4-1. Required width, and length of the transistors

$M_{2,3}$	W/L	36µm/180nm
M_1	W/L	8.8µm/180nm
$M_{4,5}$	W/L	4.4µm/180nm
$M_{6,7}$	W/L	8.8µm/180nm
$M_{9,10}$	W/L	4.4µm/180nm
$M_{8,11}$	W/L	2.2µm/180nm
$C_{internal}$		400fF

Figure 4-6 shows the transient response of the comparator for the given width, and length of the transistors. The rms current consumption of this comparator is 384 µA which is very high for a low-power application. In addition, this power consumption does not include the offset cancellation scheme.

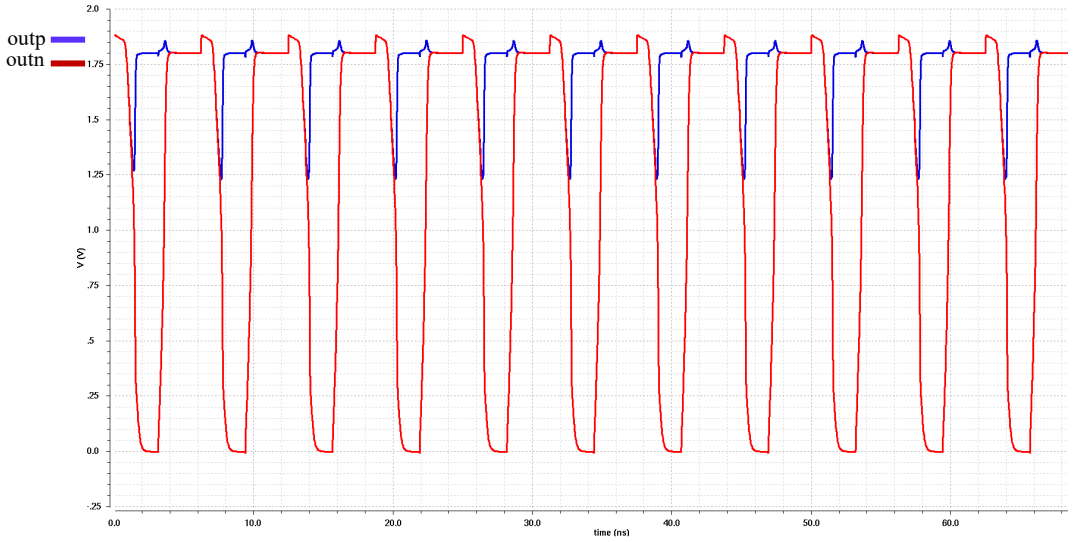


Figure 4-6. Transient response of the comparator for the given width, and length of the transistors.

The noise analysis of this type comparator in the simulations cannot be performed in the time domain, since the output is digital. For this reason, a reasonable simulation is the transient noise analysis. In the transient simulation analysis, the random noises are injected into the circuits randomly. The transient noise analysis is performed as follows:

a. Short the differential inputs and run a transient noise simulation for a long time such as 1000 clock cycle. Theoretically, for the shorted input, the comparator produces ones and zeros at the output with equal probabilities.
b. Apply a small differential input, and run the transient noise simulation. Since, the input differential skews the comparator decisions, the ones and zeros at the output are produced with unequal probabilities.
c. Look at the Gaussian distribution of the collected data. The input-referred noise voltage can be estimated as this differential input voltage. Figure 4-7 shows the transient noise simulation for the standard StrongArm latch comparator.

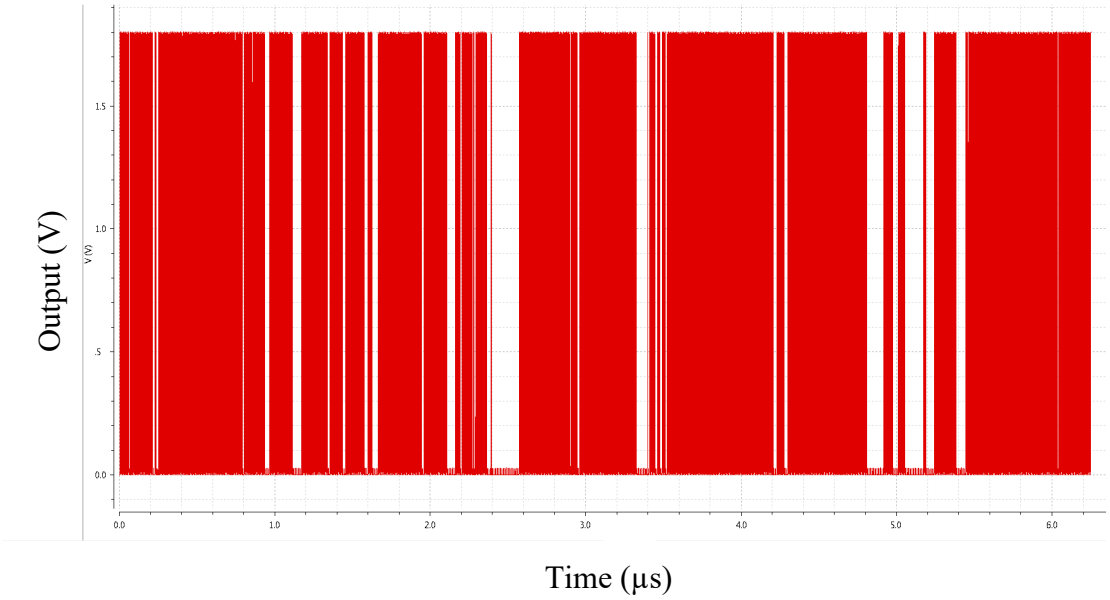


Figure 4-7. Transient Noise Simulation for the standard StrongArm latch comparator.

The noise of the comparator is approximately equal to 50uV while drawing a 716 µA from the supply voltage. The rms power consumption is 1.288 mW at 160 MHz. If a figure of merit is defined as the product of the power consumption with the power, the figure of merit for this comparator is 402.750 µV*µW/conv-step. The power consumption and the figure of merit show that the standard StrongArm latch is not suitable for low-power systems while achieving high-resolution. In addition, the StrongArm latch comparator has drawback which were mentioned in the previous section. In general the kickback noise and offset voltage are the fundamental limitations of the StrongArm latch topology for high resolution such as 14-bit.

Due to the reasons given above, in this thesis, the standalone StrongArm latch can only be used for latch. Thus, the size of the transistors can be decreased to reduce the power consumption of the latch. Besides no additional capacitors are required to decrease the noise, since there will be a gain stage before the latch stage. Table 4-2 shows the proposed latch has the following sizes.

Table 4-2 Proposed latch size

$M_{2,3}$	W/L	2µm/300nm
M_1	W/L	2µm/300nm
$M_{4,5}$	W/L	2µm/300nm
$M_{6,7}$	W/L	4µm/300nm
$M_{9,10}$	W/L	0.5µm/300nm
$M_{8,11}$	W/L	1µm/300nm

Table 4-2 shows that the sizes of the transistors which are very small compared to the conventional StrongArm latch topology. After designing the latch, a gain stage is required. Since the proposed StrongArm latch has nmos differential pair, the gain stage before the latch should have pmos differential pair. Figure 4-8 shows the dynamic differential amplifier with pmos input stage.

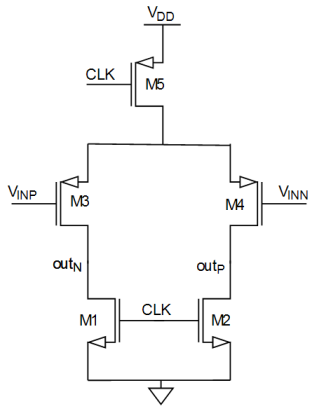


Figure 4-8. The dynamic differential amplifier with pmos input stage.

The circuit operates as follows:

When CLK is low, M5 turns on and provides the common-mode current to the transistors M3 and M4, while the transistors M1 and M2 are OFF. In this phase the output nodes are charged up by the input differential pair. The charging rate is in proportional to the size of the M3 and M4. This phase is called as amplification phase in which the parasitic capacitors at the output nodes rise to VDD and a differential voltage is generated between the output nodes. In amplification phase, one output reaches to VDD early depending on the input differential voltage. When the amplification phase ends, the nmos transistors turn on reset the output nodes to ground in order to eliminate the dynamic offset. This type of amplifier is commonly used in many SAR ADC architectures. In this architecture, all the charges at the output nodes are reset and wasted at the end of the comparison resulting considerable amount of power consumption during the conversion. In this thesis, instead of resetting the output nodes to ground at the end of the comparison, a charge re-suing approach is implemented in the proposed latch. In order to re-use the charges at the nodes, a novel modified dynamic differential amplifier is proposed in the thesis. Figure 4-9 shows the proposed novel 2-level latch architecture. In the proposed circuit, after the amplification phase, the charges at the output nodes are transferred into the latch to reset the nodes in the latches.

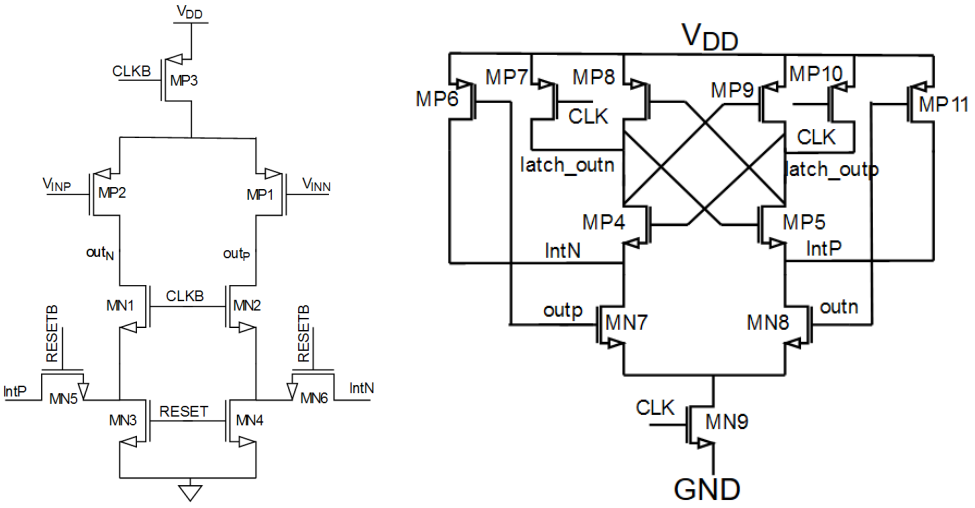


Figure 4-9. The proposed novel 2-level latch architecture.

The circuit works as follows:

When CLK is high, CLKB becomes low. MP3 turns on and provides the required bias current to turn on the input transistors MP1 and MP2 respectively. At the same time, the output nodes called as outn and outp are also charged up with the common-mode current. In addition to this common-mode current, the differential input pair also generates a small signal current depending on the input differential voltage which provides a difference between the output nodes. When the latch senses the differential voltage at the output of the first stage, it starts to work and make a decision. After the amplification phases end, the switches MN5 and MN6 turn on, and transfer the charges to the nodes INTP, and INTN respectively in order to charge these nodes without any bias transistor. After transferring the charge, the switches turn off, and MN3, and MN4 switches turn on. These switches reset the output nodes outn, and outp respectively in order to ensure that there is no dynamic offset in the next conversion cycle. The parasitic capacitors at the node INTP and INTN reach approximately 0.9V after charging. Following the passive charging, MP6 and MP11 turn on and charges the nodes in the StrongArm Latch to complete the charging phases. Thus, the power consumption while charging these capacitors is significantly

reduced. More specifically, the power is reduced by 50% compared to the conventional topology while achieving gain in the first stage. In addition, the rms current is approximately reduced by 10 % which becomes very important for battery-powered low-power systems. This architecture still has some drawbacks.

1. There is still a kickback noise due to the instantaneous current surges during the turning on, and off cases.

2. The pmos transistors are used in the differential input stage. Since pmos transistors are weaker than nmos transistors, in order to achieve the same result larger pmos devices are required, resulting larger silicon area and power consumption.

3. These types of comparator topologies depend on the input common mode voltage which can degrade the performance of the comparator for the different common mode voltages. In order to solve these problems, a preamplifier such as inverter based floating amplifier which was discussed before was proposed.

4.4 Coarse Comparator

The coarse comparator consists of a gain stage shown in Figure 4-5. The inverter based floating amplifier provides the required gain of the second gain stage. The second gain stage maintain the additional gain to suppress the noise and the offset of the differential pair in the StrongArm Latch. Figure 4-10 shows the complete architecture of the proposed coarse comparator. The coarse comparator consists of three stage which the first two stages are the gain stage.

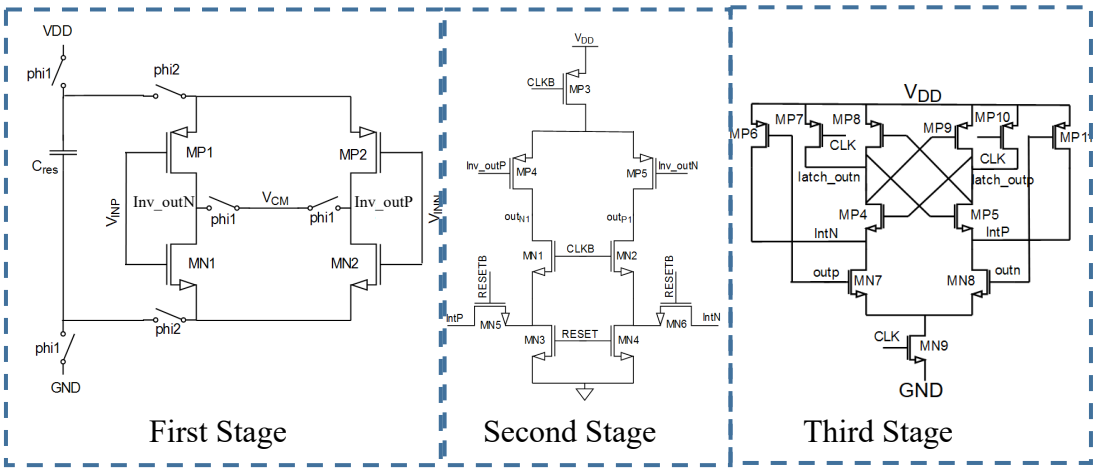


Figure 4-10. The complete architecture of the proposed coarse comparator.

Figure 4-11 shows the transient response of the coarse comparator when the input differential voltage is 10mV.

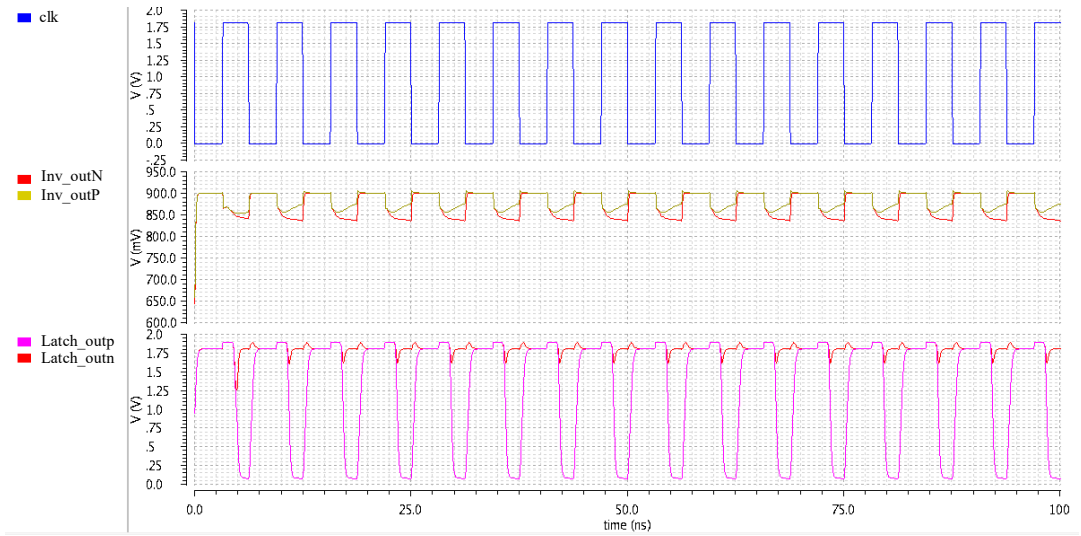


Figure 4-11. Transient response of the coarse comparator.

The transient response illustrates that the first gain stage provides the initial gain for the second stage. The output of the first stage is then amplified by the second stage. The third stage makes a decision depending on the input differential voltage.

4.5 Comparison with state-of-the-art comparators

Table 4-3 shows the comparison between the proposed architecture and the state-of-the-art comparators published in the literature.

Table 4-3. Comparison with the state-of-the-art comparators.

	This Work*	Solid-State Circuit Letter,2020 [84]**		VLSI 2019 [85]**		ESSCIRC 2017 [86]**	
Architecture	**Proposed Circuit**	Proposed Circuit	Double Tail	FIR SA	SA	Dynamic Bias	Double Tail
Process(nm)	**180nm**	65	65	180	180	65	65
Supply(V)	**1.8V**	1	1	1.2	1.2	1.2	1.2
Noise(μVrms) (without inv-preamps)	**43**	220	210	46	62	400	450
Energy(pJ) (without inv-preamps)	**0.95**	0.19	0.26	0.98	4.1	0.03	0.09
Clock(MHz)	**160**	25	25	No info	No info	25	25
Use of additional capacitors	**Yes**	No	No	Yes	No info	No info	No info
Use of extra signal	**Yes**	No	No	No	No	No	No info
Figure of merit without offset cancellation	**41.11**	42.24	54.6	45.08	254.2	13.6	39.6

Figure of merit : Noise(μV)·energy(pJ)

*Simulated work

**Measured work

Table 4-3 reveals that, the proposed coarse comparator has a good figure of merit compared to the state-of-the art comparators. The noise of the coarse comparator is very low compared to the state-of-the-art comparators while operating at 160 MHz. The operation rate of the comparator is also faster than the previous architectures which is another advantage of the proposed coarse comparator. One disadvantage is that it requires an additional reset signal which can be generated easily by the digital controller.

4.6 Fine Comparator

Figure 4-12 shows the proposed architecture of the fine comparator. The comparator consists of 3 stages. In the first 2 stages, an offset cancellation scheme is performed to reduce the effects of the offset voltage caused by the process variations.

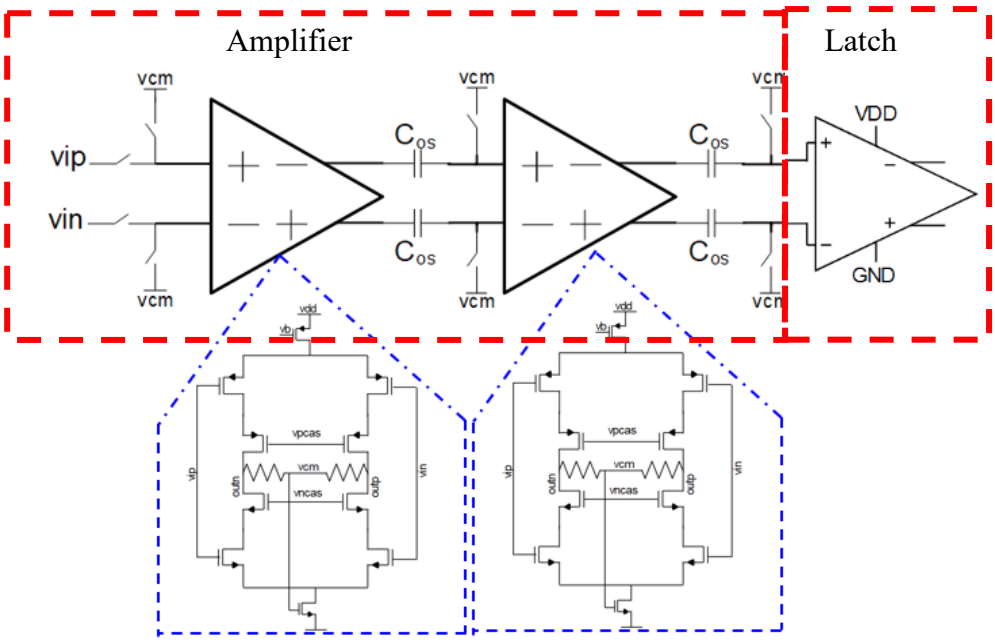


Figure 4-12. The proposed architecture of the fine comparator.

The gain of the first 2 stages are adjusted to balance the offset voltage coming from the latch. The first 2 stages consist of an inverter amplifier which provides more gain with the same bias current. These types of amplifiers are known as Current reuse amplifiers. Figure 4-13 shows the modified current reuse inverter amplifiers. The conventional inverter amplifiers do not have cascade transistors. In the proposed SAR ADC, the amplifier operates at 160 MS/s to support 8 MS/s conversion rate. Therefore, more gain is required at high frequencies. The amplifier has vncas and vpcas cascade voltages. The vncas voltage is 1.7V and the vpcas voltage is 200 mV respectively.

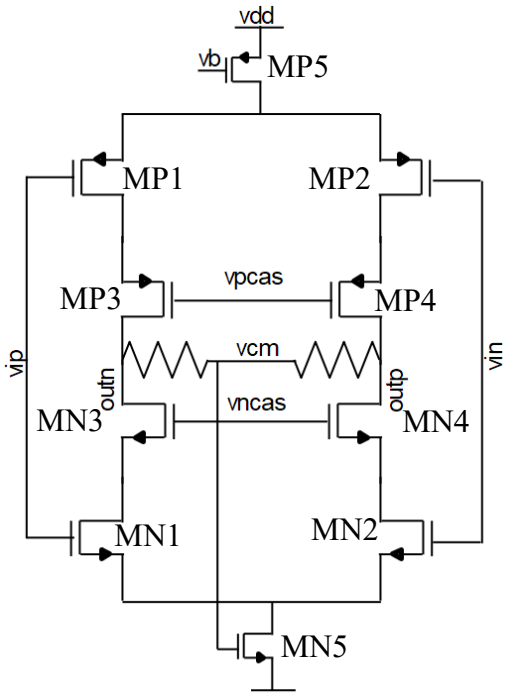


Figure 4-13. The modified current reuse inverter amplifiers.

A simple resistive common-mode feedback is used to ensure that the common-mode voltage of the amplifier is 0.9V. Since, the resistive feedback depends on the process parameters of the tail transistor, the output common-mode voltage of the amplifier changes between the process corners. More specifically, the common-mode voltage can shifts 50 mV from slow FS corner to SF corner. However, this voltage difference does not degrade the overall performance of the amplifier. The input of the second stage still has the same common-mode voltage thanks to the offset cancellation capacitors. Neglecting the resistors of the common-mode feedback, the gain of the amplifier can be written as

$$A_V \approx g_{mn1,2}\{(g_{mn3,4}r_{on3,4}r_{on1,2})||(g_{mp3,4}r_{op3,4}r_{op1,2})\} \qquad (3.4.1)$$

The cascade transistors boots the output impedance of the amplifier. Figure 4-14 shows the frequency response of the inverter amplifier. The gain of the first stage 18.5 dB at 160 MHz while dissipating approximately 200 mA including the 20 mA

bias current. In addition, since the amplifier operates in open-loop configuration, the amplifier does have any stability problems. The amplifier has a dominant pole at the output, the common-mode stability does not degrade.

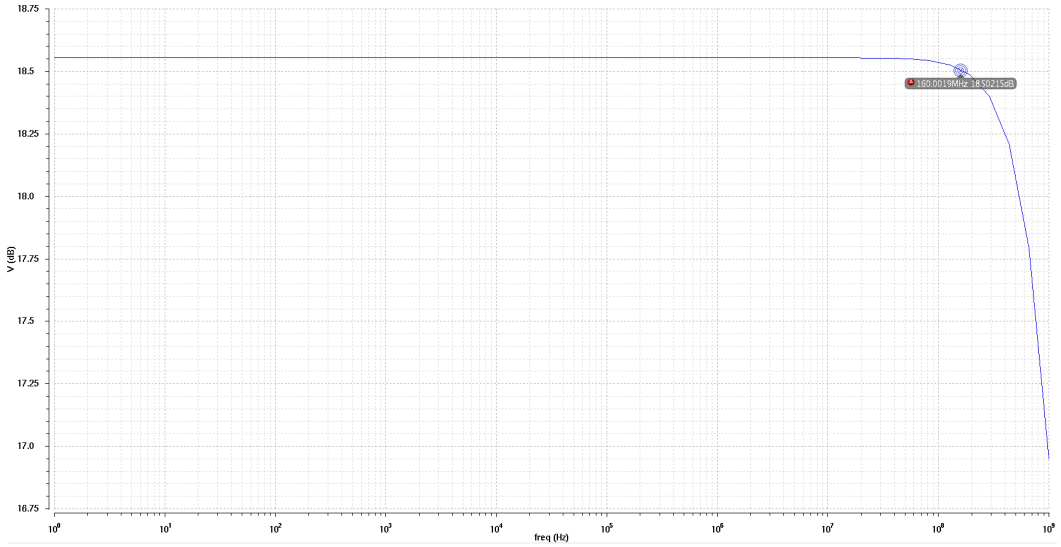


Figure 4-14. The frequency response of the inverter amplifier.

The gain of the amplifier should not exceed 20 dB, since the offset voltage of the amplifier can saturate and the offset cancellation scheme does not work. In addition to the gain of the amplifier, the input referred of comparator is important for high-resolution ADCs. The comparators discriminate small LSB voltages for high-resolution ADCs. Figure 4-15 shows the input referred noise voltage of the inverter amplifier. The input referred noise of the inverter amplifier is less than 0.5 LSB voltage which is suitable for the proposed. ADC. The noise of the amplifier is dominated by the input pairs. Since the amplifier operates at 160 MHz, the thermal noises of the input pairs dominate the overall performance of the amplifier.

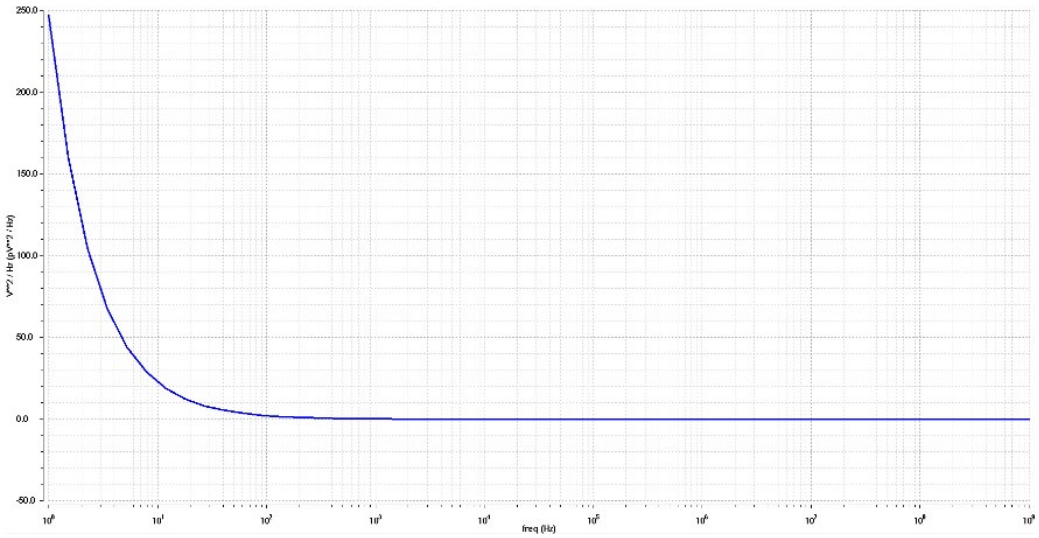


Figure 4-15. The input referred noise voltage of the inverter amplifier.

The second stage of the amplifier is similar to the first-stage amplifier except that the sizes are different. Since the amplifiers operates at 160 MHz, in order to improve the frequency response of the first–stage amplifier, the input transistors of the second stage are small to move the poles far away from the origin. For this reason, the second stage has a gain of 14.63 dB while dissipating 250 mA including the bias current. The first 2 stages of the comparator consists of static amplifiers. Static amplifiers do not have an input dependent offset, since the bias current does not depend on the inputs. On the other hand, the dynamic amplifiers are low-power amplifiers. However, their bias current depends on the differential input voltage which degrades the overall performance of the comparator. If the input common-mode voltage slightly changes, then this voltage change will return as an offset voltage. There are some numerous techniques to reduce the offset voltage, but static amplifiers are more reliable than the dynamic amplifiers in terms of the CMRR and offset variation. The total gain of the first 2 static amplifiers is approximately 32 dB. At the end of the second static amplifier, if the outputs exceed approximately 940 mV, the dynamic inverters triggers a valid signal, and the comparison is performed by the latch. As a result, the required time to make a decision is shortened, and the rest of the time is

reserved for the next conversion. Figure 4-16 shows the complete fine comparator architecture including the inverters to speed up the decision.

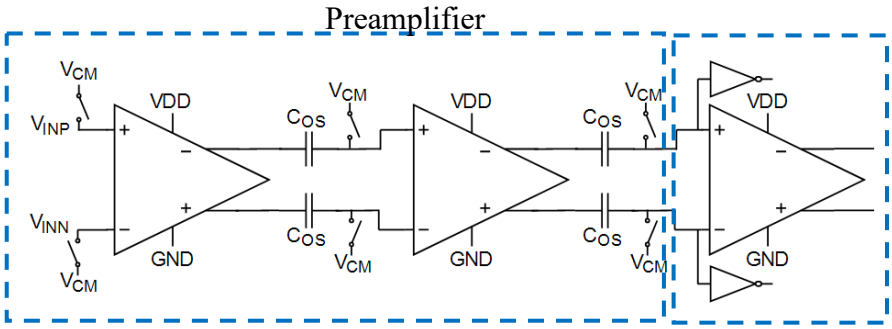


Figure 4-16. Complete fine comparator architecture.

In order to cancel the offset voltages, an output offset cancellation technique is implemented. There are different methods to minimize the offset voltages. Using large devices, and trimming is a method for reducing the effects of the process variations. However, the ADC operates at 160 MHz, large devices degrade the speed of the converter. Trimming is not suitable for this ADC, since it requires additional testing time for each die which cannot be a practical solution. The input offset cancellation does not totally cancel the offset voltage and it causes charge injection error due to the switches at the feedback loops. For these reasons, output offset cancellation is the best choice for the proposed ADC. At the beginning of the conversion, while the DAC array samples the input voltages, the comparators enter into offset cancellation mode. The inputs, and outputs of the inverter amplifiers are connected to the common-mode voltage. As a result, the offset voltages due to process variations are sampled on the C_{OS} capacitors. As a result, each comparison is not affected by the offset voltage.

The latch is a modified version of classic StrongArm Lath topology. The modified version includes two additional transistors in order to speed up the conversion. This topology is known as g_M-boosted StrongArm Latch. In this thesis, instead of using CLK at the gate of the tail transistor M1, a constant voltage which is 0.9V common-mode voltage is used to provide a constant common-mode current through the circuit which improves the CMRR of the circuit.

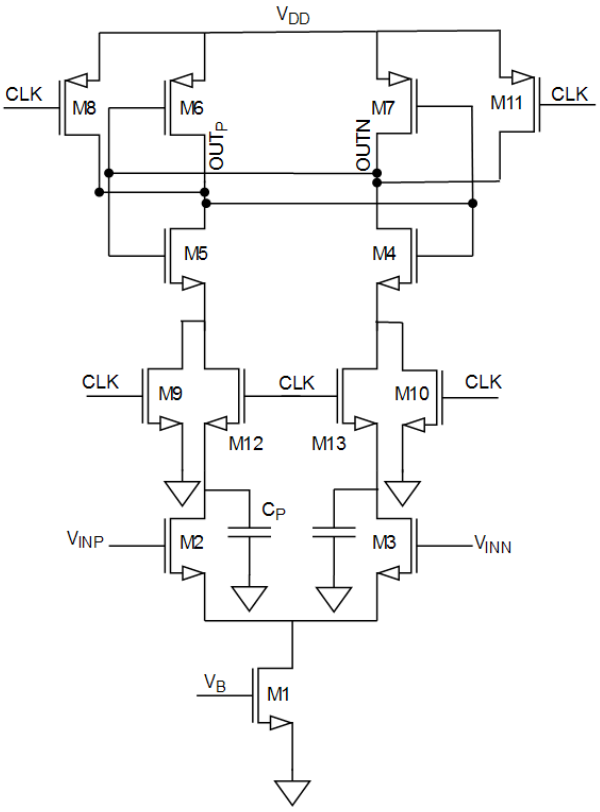


Figure 4-17. A modified version of StrongArm latch.

The modified version of the StrongArm latch has a dynamic offset, however, the gain of the first two stages balance this offset voltage which does not degrade the performance of the proposed fine comparator. Figure 4-17 shows the layout of the proposed fine comparator. The layout measures 350 µmx310 µm. In order to achieve a 14-bit performance common-centroid layout technique is applied to suppress the mismatches coming from the process variations.

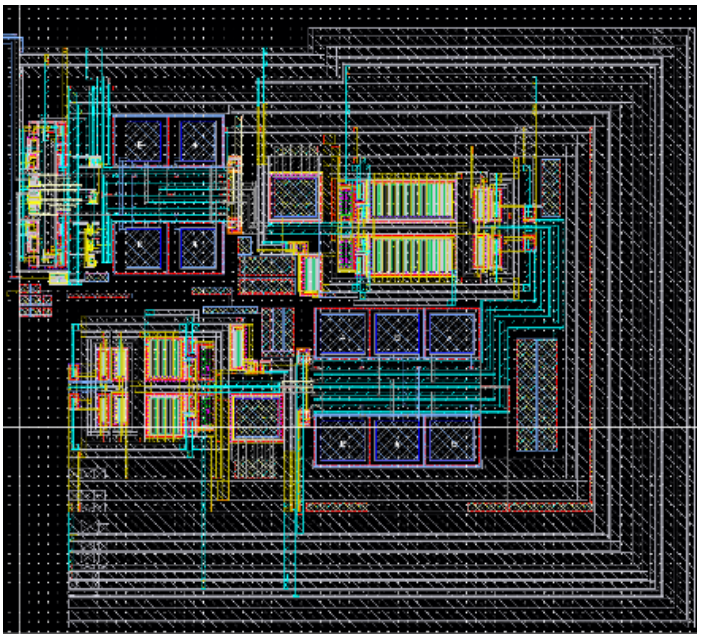


Figure 4-18. Layout of the proposed fine comparator. It measures 350µm x310 µm.

4.7 Conclusion

This chapter reviews the existing state-of-the-art comparator architectures and proposes a coarse and fine comparators. The prior art focuses on the dynamic amplifiers and different architectures are proposed to reduce the power consumption while achieving a good performance. The StrongArm Latch based comparator is the first type of comparator that eliminate the static consumption at the expanse of kickback noise. A double-tail latch based comparator divides the StrongArm Latch based comparator into two parts which are the pre-amplifier stage and latch stage. In this architecture, the latch start to operate at the same time with the pre-amplifier stage which is useless, since at the beginning of the comparison, there is no differential voltage. In order to overcome this problem, advanced architectures were proposed such as dynamic bias and inverter based floating amplifier. In this thesis, the previous architectures are not suitable. The inverter based floating amplifier requires an offset cancellation scheme. Classical offset cancellation schemes cannot be applied at the high frequencies. As a result, advanced calibration algorithms are

required for the inverter based floating dynamic amplifiers. The dynamic bias comparator also suffers from the same limitation.

In this thesis, the fine comparator consists of static amplifiers followed by a gm-boosted latch. The static amplifiers consists of inverter based amplifiers with simple resistive feedback circuits. In order to increase the gain of the amplifier, cascode stages are used. The first two stages provide require gain to suppress the offset coming from the input pair of the latch stage. There is no offset correction for the latch. In the latch, in order to speed up the comparison. These two additional transistors discharges the nodes at the same time with the input differential pair. Thus, the output of the latch discharges at a fast rate compared to the conventional architecture.

The coarse comparator consists of a inverter based dynamic floating amplifier followed by a novel 2-level latch in order to improve the power consumption while achieving a good performance compared to the conventional architectures. The inverter based dynamic amplifier provides the initial gain for the rest of the circuit. The novelty is in the second stage which is comprised of a charge-reused block. The second stage does not waste the charges at the end of the comparison. At the end of the comparison, the charges are shared with the StrongArm Latch topology to charge the required nodes in this latch. As a result, the second stage is not only used for amplifying the input differential voltage, but also for a charging storage for the latch. This architecture has almost same performance while the comparator operates at a faster conversion rate than the previous architectures. In conclusion, this chapter highlights the design of a comparator while overviewing the existing state-of-the-art architectures.

CHAPTER 5

LOW-POWER ANALOG FRONT-END CIRCUITRY FOR SAR ADCS

This chapter discusses the design of a low-power front-end circuit for SAR ADCs. In recent years, the researches have focused on the core architecture of the SAR ADC in order to reduce the power consumption while achieving a good performance. Today, the state-of-the-art SAR ADCs have a Walden Figure-of-Merit below 1 fJ/conv-step, resulting a great power reduction. However, these SAR ADC architectures do not include the input drivers which may degrade the figure of merit and abruptly increase the power consumption of the overall ADC. This thesis focuses on the integration of the input drivers into the SAR ADC by using novel circuit topologies. Section 5.1 introduces the fron-end circuits for SAR ADCs. Section 5.2 discusses the current state-of-the-art input circuit topologies. Section 5.3 explains the proposed input front-end circuit, while Section 5.4 compares the arcitecture with the state-of-the-art architecture. Section 5.5 discusses the input driver archtecture and Section 5.6 summaries the chapter.

5.1 Introduction

In recent years, SAR ADCs have been used for infrared imaginng systems. The current state-of-the-art techniques published in the literature focuses on the reduction in the Walden Figure of Merit which is now below the 1fJ per conversion-step [87,88]. The current Walden Figure of Merit can be achieved without the input drivers and the peripheral circuits of the SAR ADC. Especially, the input drivers requires considerable amount of power consumption to drive the SAR ADCs. The commercial input drivers even consumes more power than the state-of-the-art architectures found in the literature. For this reason, researches start to focus on

minimizing the input drive power consumption of a ADC. This thesis also seeks novel solution for the input drivers used in the low-power 14-bit SAR ADC.

The minimum required driving current for driving the sampling capacitor C_S of a SAR ADC can be defined as;

$$I_{DR,MIN} = N \cdot C_S \cdot \frac{\Delta V_{max}}{T_{Track}} \tag{5.1.1}$$

where Δ_{max} represents the maximum voltage change at the output of the input drivers and N is the integer number of time constants required for the settling within LSB/2 voltage precision at the end of the sampling period. In order to reduce the power consumption of the input drivers, the current must be minimized. The straightforward method to minimize the power consumption is the lowering the sampling capacitor. The sampling capacitor is limited by the kT/C noise and the linearity requirement which cannot be freely decreased. The period time and settling time also depends on the other factors such as conversion rate of the ADC. For these reasons, the only reasonable choice is to decreasing the maximum voltage change at the output of the input drivers. Figure 5-1 shows the waveform of the differential input for a typical SAR ADC. The differential input reaches its maximum value at $\pi/2$ and $3\pi/2$ which requires a peak to peak voltage swing in the conventional ADC architecture.

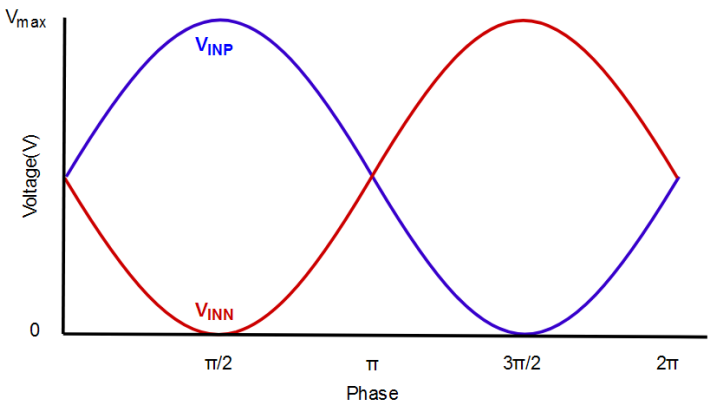


Figure 5-1. Waveform of the differential input for a typical SAR ADC.

In conventional SAR ADCs, the input buffers directly drive the DAC arrays in order to sample the differential input voltage. Figure 3-29 shows the conventional SAR ADC input circuitry architecture with differential input signal characteristics. Figure 5-1 shows the waveform of the differential input for a typical SAR ADC. The conventional SAR ADCs directly sample the different input on the DAC arrays. Assume that the positive differential input signal V_{INP} is defined as

$$V_{INP} = 0.5 \cdot V_{PK} + 0.5 \cdot V_{PK}\sin(2\pi f_{IN} t) \tag{5.1.2}$$

Then, the sampled voltage change on the capacitive DAC array for two consecutive samples at $t = \frac{n}{fs}$, and $t = \frac{n+1}{fs}$ can be expressed as

$$\Delta V_{DAC,conv} = 0.5 \cdot V_{PK} \sin\left(2\pi f_{IN} \frac{n+1}{f_s}\right) - 0.5 \cdot V_{PK}\sin(2\pi \frac{n}{f_s}) \tag{5.1.3}$$

$$\Delta V_{DAC,conv} = V_{PK} \cos\left((2n+1)\pi \frac{f_{IN}}{f_s}\right) \cdot \sin(\pi \frac{f_{IN}}{f_s}) \tag{5.1.4}$$

In the conventional SAR ADC, the maximum value of ΔV_{DAC} can be described as

$$\left|\Delta V_{DAC,conv,max}\right| = V_{PK} \cdot |\sin(\pi \frac{f_{IN}}{f_s})| \tag{5.1.5}$$

Equation (5.2.4) shows that the voltage change for two consecutive samples can reach the amplitude of the input signal if the input frequency is equal to the sampling frequency or multiples of sampling frequency. It means that, the input buffers must drive the peak voltage. The power consumption of the buffers equal to$2 \cdot V_{DD} \cdot I_{DR}$, since 2 buffers operates for differential input voltage according to the equation given in equation (5.1.1).

For the conventional input drivers, due to the fact, the input buffers drive peak voltage, the current consumption abruptly increases. In addition, the conventional SAR ADCs require rail-to-rail input buffers to drive the required differential input voltage. In the following chapters a simple technique using the charge-sharing method will be proposed to decrease the power consumption of the drivers.

5.2 Current State-of-the-art techniques

In this section current state-of-the art techniques are reviewed in order to determine the advantages and disadvantages of the current circuit topologies. In the literature, there are some researches on the front-end circuits to reduce the power consumption of the buffers. Bindra et. al in [86] introduced an input range dependent swapping technique. This technique is known as range pre-selection sampling (RPS) which determines the region of the current input signal, and sample the input signal corresponding DAC. Figure 5-2 illustrates the proposed RPS technique.

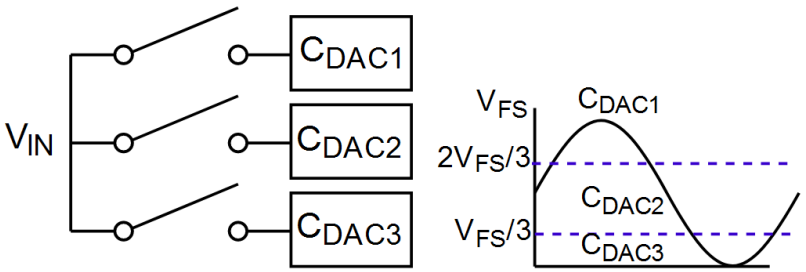


Figure 5-2. The proposed RPS Technique in [86].

The RPS technique uses 3 different CDACs and each CDAC covers the 1/3 of the input range, resulting a maximum voltage change of 1/3 of the input range. This techniques achieves 58.3 % reduction in the peak power compared to the conventional sampling method. However this technique requires 3 different CDACs which is not suitable for high-resolution ADCs and leads to a hardware overhead. A modified version of this work was reported in [89] was called as energy-reduced-sampling known as ERS. This technique swaps the output of the input driver

depending on the previous differential input voltage. In order to implement this technique a comparison is performed before the sampling phase and the inputs are connected to the corresponding DAC arrays. This technique achieves a reduction in 25% less than the previous research. Another work in [90] proposed a swap-to-reset technique which has zero reset power. In this technique, at the end of the conversion, the voltages at the inputs of the comparator approaches to common-mode voltage, since a top-plate sampling technique is used. As a result, the input buffers drive the half input swing which leads to 50% reduction in the power consumption.

The work proposed in [91] reduces the power consumption by 75% by using an input correlated input swapping technique which swaps the MSB, and MSB-1 capacitors between the capacitive DAC arrays and uses a flash ADC to determine the first 2 most significant bits. Depending on the comparison result of the first two comparison, the configuration of the MSB and MSB-1 capacitor is altered by changing the top plate connections of the respective capacitors. In this technique, the switches enabling the swapping are connected to the top plate of the DAC array. These switches can change the charge equations and degrade the linearity performance of the overall ADC. In order to solve these problems and reduce the power consumption of the input buffers, this thesis a novel technique is proposed.

5.3 Proposed Sampling Technique

In the previous sections, current state-of-the-art techniques were discussed. All of the techniques except [90] requires additional power consumption to reduce the maximum voltage change at the output of the input drivers. The work in [90] uses a DAC switching scheme that is based on top plate sampling which is not suitable for the high resolution ADCs, since the switches at the top plate causes nonlinear charge injection which cannot be recovered by the correction algorithms. In this thesis, a DAC switching scheme with bottom plate sampling technique is used to implement the SAR ADC. Figure 5-3 shows the proposed sampling technique in this thesis.

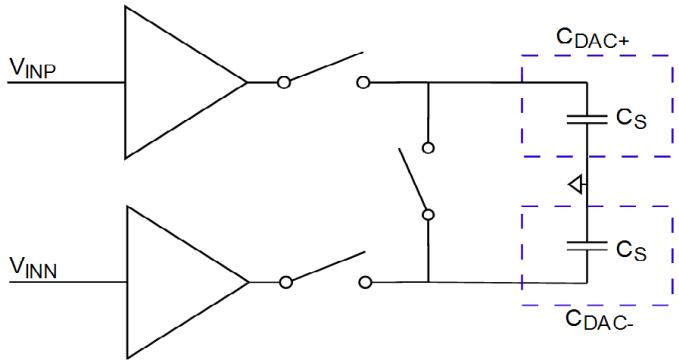


Figure 5-3. Proposed sampling technique in this thesis.

The proposed input sampling technique is used as follows;

1. At the end of each conversion, the output of the input drivers are disconnected from the DAC arrays, and the next conversion has not been started yet.

2. The top plate of the each DAC array is connected to V_{CM}, common-mode voltage. Normally, the top plate approaches to common-mode voltage at the end of the conversion, but in order to initiate the sampling this plate should be tied to common-mode voltage.

3. Following the connection of the top plate to the common-mode voltage, the bottom plates of DAC arrays are connected together.
4. After connecting the bottom plates of the DACs together, the voltage at the bottom plates of each DAC array approaches to common-mode voltage without any power consumption, since the previous voltages on the bottom plates are fully differential. This period is called as shorting phase.
5. When the shorting phase ends, the switches shorting the bottom plates of the DAC array turn OFF, and the output of the input drivers are connected to the corresponding DAC array. As a result, the input drivers do not require to drive the peak to peak voltage. The maximum voltage change at the output of each input driver is 0.9V which reduces the power consumption by 50%

compared to the conventional techniques without demanding any power consumption.

In the proposed technique For the worst case, C_{DAC+}, and C_{DAC-} deals with only either($\frac{V_{FS}}{2} - V_{FS}$), or ($\frac{V_{FS}}{2} + V_{FS}$) respectively. The voltage change across the sampling capacitors for two consecutive sampling instants can be expressed as:

$$\Delta V_{IN,swap} = 0.5 \cdot V_{PK} \sin\left(2\pi f_{IN} \frac{n+1}{f_s}\right) - 0.5 \cdot V_{PK} \tag{5.3.1}$$

$$\Delta V_{IN,swap} = 0.5 \cdot V_{PK} \sin\left(2(n+1)\pi \frac{f_{IN}}{f_s}\right) \tag{5.3.2}$$

The maximum value of $\Delta_{IN,SWAP}$ can be written as

$$|\Delta V_{IN,swap,max}| = 0.5 \cdot V_{PK} \sin\left(2\pi \frac{f_{IN}}{f_s}\right) \tag{5.3.3}$$

As a result, for the worst case, the voltage across the sampling DAC is reduced by half when Nyquist input frequencies are considered.

5.4 Comparison with Current State-of-the-Art Techniques

The proposed technique in this thesis does not require any power consumption while minimizing the voltage swing at the output of the each input driver. Although, the work in [89] also does not consume any power, it requires a DAC switching scheme with top plate sampling which can cause linearity problems for high resolution SAR ADCs. On the other hand, the proposed input sampling technique can be used with bottom plate sampling technique which can achieve 14-bit performance. Table 5-1 shows the comparison between the state-of-the art techniques, and proposed technique. In addition to power consumption and DAC sampling method, the proposed technique can be implemented in high resolution SAR ADCs, while the works in [86], [90] and [91] may not be implemented. The work in [91] uses extra

DAC array which can degrade the linearity performance of the ADC while occupying more silicon area. As it was mentioned before, the works in [86], [89] and [90] are based on the DAC switching scheme with top plate sampling. The work in [91] requires extra switches to implement to algorithm. Additional bits cause complex DAC array routings in the layout which can degrade the linearity performance of the ADC.

In conclusion, the proposed input sampling technique is suitable for high-resolution ADCs without any power consumption while using only simple charge-sharing technique.

Table 5-1.The comparison between the state-of-the art techniques, and proposed technique.

	ASSCC'17 [86]	**ESSCIRC'17 [89]**	**JSSC'17 [90]**	**ISCAS [91]**	**This Work**
Technology[nm]	65	65	65	28	**180**
Resolution[bits]	10	10	12	12	**14**
Sampling Rate[MS/s]	1	1	0.04	25	**8**
Supply Voltage [V]	1	1	0.8	0.9	**1.8**
DAC sampling method	Top	Top	Top	Bottom	**Bottom**
Additional power requirement due to extra circuits	Yes	Yes	No	Yes	**No**
Theoretical Reduction Factor	67%	33%	50%	75%	**50%**

5.5 Input Buffers

The proposed sampling technique reduces the driver current of the input driver by 50% compared to the conventional architectures. In addition, the proposed DAC switching scheme analyzed in the previous sections reduces the total number of capacitors. As a result, both of these novelties provide a great reduction in the power consumption of the input buffers compared to the conventional architectures. The input buffers drive a 3.840 pF load in 6 clock cycles. For low-to-medium resolution applications one n-type and p-type buffer can be used to reduce the power consumption. However, in the proposed ADC the errors coming from n-type and p-type buffer cannot satisfy the 14-bit resolution performance. For this reason, a low power class AB amplifiers are used for input drivers. The class AB amplifier has 2-stage. The first stage consists of a rail-to-rail input folded cascode opamp. Following the first stage, a second gain stage is used to design the amplifier. The stability of the class AB amplifier should analyzed carefully, since, the amplifier has two more than 2 poles which may not satisfy the stability condition over the given input voltage range. For this reason, the amplifier is simulated with the switches over the full input range. Figure 5-4 shows the layout of the buffers. It measures 108 µm x290 µm.

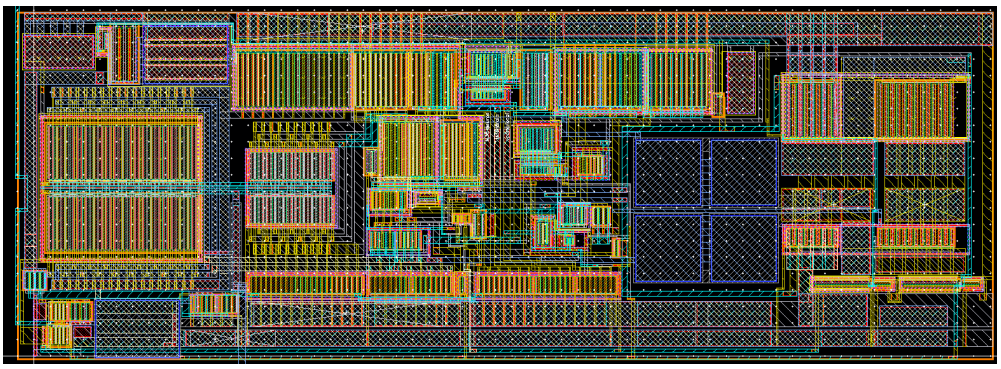


Figure 5-4. The layout of the buffers. It measures 108 µm x290 µm.

5.6 Conclusion

This chapter introduces the input sampling techniques and drivers to integrate the input buffers into the SAR ADC. The current state-of-the-art techniques published in the literature cannot satisfy the target specifications. A novel input sampling technique that does not require any active power consumption and large silicon area is proposed. The proposed input sampling technique reduces the power consumption by 50% compared to the conventional architecture and it can be easily implemented in the high-resolution SAR ADCs. The proposed input sampling technique uses a class AB amplifier to drive the SAR ADC. The class AB amplifier has a rail-to-rail input range while provides a good settling and linearity.

CHAPTER 6

SAR LOGIG AND PERIPHERAL CIRCUITS

This chapter introduces the SAR Logic and the peripheral circuits of the SAR ADC such as bias generator and digital controller. Section 6.1 explains the proposed SAR Logic circuit in order to speed up the conversion. Section 6.2 discusses the bias generator with the bandgap circuit. Section 6.3 overview the digital controller and Section 6.4 concludes this chapter.

6.1 SAR Logic

SAR Logic is the main block in the digital controller which is responsible for updating the DAC array. Figure 6-1 shows a conventional SAR Logic architecture.

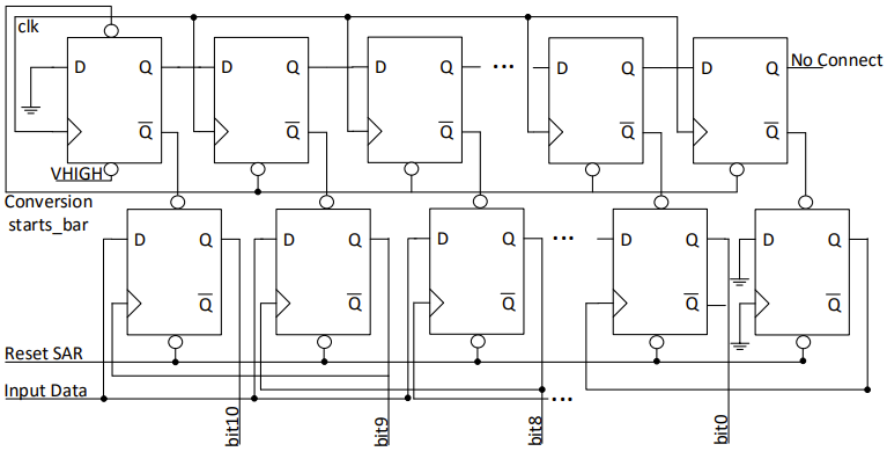


Figure 6-1. A conventional SAR Logic Architecture in [45].

The conventional SAR Logic has two row of shift registers and its operation is synchronous which allocates same conversion time for all of the conversion cycles.

The conventional SAR Logic operates as follows:

When the conversion starts, the output of the first Flip-Flop in the top shift register becomes 1 while the complementary output fires the first Flip-Flop in the bottom row shift register. The top row shift register is used for state machine, while the bottom row is used for memory in order to store the output data. When the first Flip-Flop in the second row shift register is fired, the first comparison is initiated and the comparator makes a decision. In the next clock cycle, the second Flip-Flop in the first row is fired and then the output of the second Flip-Flop in the second row becomes 1. At the same, the clk signal of the first Flip-Flop in the second row is fired to store the result of the first comparison. The operation continues until the last conversion. At the end of the conversion, the registers are completely reset to be ready for next conversion. This architecture is the fundamental architecture and it is suitable for low to medium speed ADCs, since the delay of the SAR Logic limits the speed of the overall ADC. The propagation delay of clock to output can be written as

$$T_{pd} = T_{pd1} + T_{pd2} \tag{6.1.1}$$

where T_{pd1}, and T_{pd2} are the propagation delays of the flip-flops. In addition, at the output of each Flip-Flop, buffers are used to drive the capacitive loads. As a result, the total propagation delay becomes:

$$T_{pd} = T_{pd1} + T_{pd2} + T_{buffer} \tag{6.1.2}$$

For the proposed ADC, single conversion cycle should be done within 3.125ns including the delay of the SAR Logic in order to allocate the required time for settling. For this reason, conventional architecture cannot be used in the proposed ADC. In order to allocate more time in the conversion cycle, the propagation delays should be minimized. In this thesis, a novel SAR Logic architecture is proposed in order to lower the propagation delays.

Figure 6-2 shows the proposed SAR Logic architecture. The proposed SAR Logic operates as follows:

When the comparison result is available, valid signal is triggered. First flip-flop in the top shift register is triggered, and the first MSB capacitor is charged to V_{DD}. After that, the first comparison is performed. When the valid signal is triggered, the unit

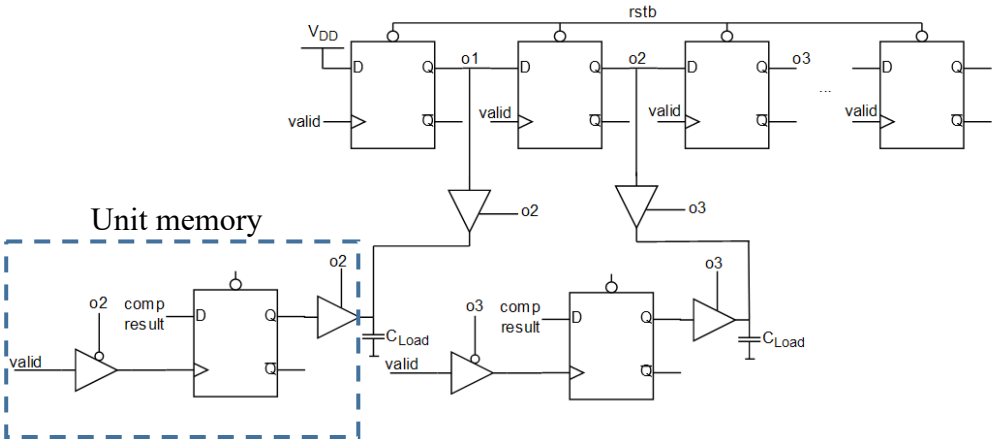


Figure 6-2. Proposed SAR Logic architecture.

memory is updated and the comparison result is stored in this memory unit. This operation continues until the end of the conversion. At the end of the conversion, the registers are reset to be ready for the next conversion. Compared to the conventional architecture, the proposed SAR Logic has only 1 propagation delay of the flip-flop. In other words, the propagation delay is reduced by 50% compared to the conventional architecture. Normally, standard cells do not meet the speed specification for high frequency applications. The proposed SAR ADC has approximately 400ps delay time which is sufficient for the capacitor settlings.

6.2 Peripheral Circuits

Bias generator and the digital controller are the main peripheral circuits to perform the conversion. In this section, the bias generator, and digital controller will be discussed.

6.2.1 Bias Generator

The bias generator is the first peripheral circuit that generates the bias currents and voltages. The bias currents the reference currents required for the each analog block while the bias voltages are the cascode voltages. These voltages should be generated in the chip, since there are considerable number of bias currents and voltages which cannot be provided outside of the chip. In addition, noise and settling are the other limitations when a bias current or voltage is generated outside of the chip. For these reasons, a programmable bias generator is used to generate required voltages and currents. The performance of the analog circuits may alter from one chip to another due to the process and environmental variations [78]. In order to eliminate these effects, a bandgap circuit with temperature and supply independent was used in this chip. The required bias voltages and currents are generated from this 1.2V bandgap voltage. Figure 6-3 shows the typical bandgap circuit used in the proposed ADC [45].

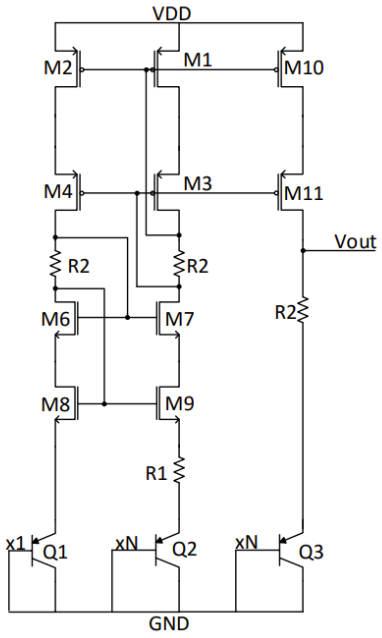


Figure 6-3. The typical bandgap circuit used in the proposed ADC [45].

The output voltage of the bandgap circuit can be written as:

$$V_{out} = V_{BE} + V_t lnN \frac{R2}{R1} \tag{6.2.1}$$

where N is a BJT multiplier. From the equation, it can be observed that the output voltage is a function of the ratio of the R2 and R1 with the BJT multiplier and base-emitter voltage of the BJT transistors. By selecting the proper ratio of the R2 and R1, an independent output voltage can be generated, due to the fact that the derivative of the output voltage with respect to the temperature is positive while the derivative of the output voltage with respect to the base-emitter voltage is negative. Following the generation of the bandgap voltage, a buffer is used drive the rest of the bias generator circuits. The buffer has a feedback circuit that is used for obtaining a 3V from 1.2V. In the bias generator, a reference current is generated from this golden voltage. This reference current is used in 7-bit current steering DACs to generate a current with 0.5 µA or 1 µA resolution while the 3V is used in the 12-bit resistive DACs which generate the cascode voltages required by the SAR ADC including the input drivers.

6.2.2 Digital Controller

The digital controller generates the required timing signals for the proper operation of the SAR ADC. In addition to digital controller, a low voltage differential signaling (LVDS) receiver is used to convert the LVDS signal into CMOS signal. The clock frequency is 160MHz for a 8 MS/s which cannot be provided from the FPGA with a CMOS signal due to the pad circuits and wire bonding effects. The digital controller communicate with external processor such as Field Programmable Gate Array (FPGA) and adjust the timing signals and digital memory for proper operation. Figure 6-4 shows the block diagram of the digital controller.

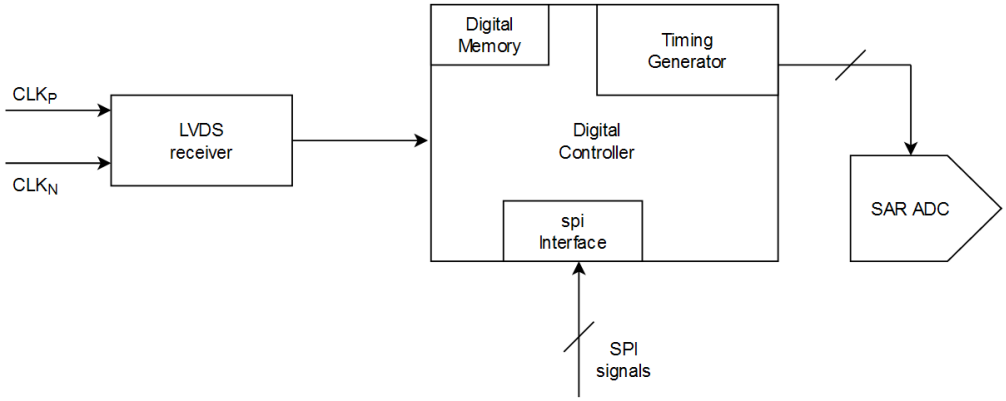


Figure 6-4. Block diagram of the digital controller.

The serial interface circuit is used for writing and reading operation and the digital controller generates the required signals. As it was mentioned above, the serial programming interface (SPI) is used for communication. A simple 4-wires communication including serial data input, serial clock, active low enable signal, and serial data output is used. The digital memory occupies most of the silicon are in the digital controller in order to provide flexibility. The digital memory stores the default values required for the operation of the SAR ADC, and they can be configured via 4-wire communication. In the digital memory, classic registers are used and the value of the static signals such as turn ON and turn OFF signals of an analog circuit are stored in these memories. All of the analog circuits are in reset phase when the chip

is powered up in order to ensure that, at the beginning of the power-up sequence, all the analog circuits are in safe. Otherwise, some current surges during the power-up sequence may cause problems. Figure 6-5 shows the layout of the digital controller. The width and length of the layout of the digital controller is 1120 µm and 633 µm respectively. The outputs of the SAR ADC are sent to external processor in parallel in order to reduce the complexity of the proposed SAR ADC.

Figure 6-5.Layout of the digital controller. It measure 1120 µmx 633 µm.

6.3 Conclusion

This chapter discusses the SAR Logic and peripheral circuits in detail. The SAR Logic is a critical circuit for the SAR ADC. The delays in the SAR logic lead to propagation delays in the SAR Loop which was mentioned in the previous chapter resulting lowering the conversion rate. The proposed SAR ADC operates at 8MS/s conversion rate while achieving 14-bit which is an unusual situation in the SAR ADC design. Due to the fact that the SAR ADC requires fast conversion, the SAR Logic has to be modified. The proposed SAR Logic minimize the propagation delay by 50 % by adding a unit element block that is fired when the output of the comparison is already determined. In the conventional SAR Logic, there are two different row shift registers. The first row shift registers fire the second row shift registers which are used for starting a new conversion, resulting a propagation delay two times larger than the proposed one.

Following the SAR Logic, this chapter investigates the bias generator and digital controller circuits used in the proposed SAR ADC. The bias generator is based on a supply and temperature independent bandgap circuit in which all of the bias voltage and currents are generated from the bandgap voltage. The proposed SAR ADC uses conventional bandgap circuit, while using different DAC architectures for the generation of the voltage and current generation.

The digital controller communicate with the external processor via 4 wire communication protocol and it generates required timing signals to control the proposed SAR ADC. The digital controller has memories which provide flexibility for programming.

The outputs are sent to external processor in parallel in order to minimize the complexity of the circuit. Normally a LVDS transmitter can be used to reduce the pad number but these extra circuits require additional power and silicon area.

CHAPTER 7

TOP-LEVEL INTEGRATION OF THE SAR ADC

This chapter presents the complete SAR ADC architecture proposed in this thesis and shows the top level simulation results. The proposed core SAR ADC operates from 1.8 supply voltage while the input drivers require 2.5V supply voltage. The proposed SAR ADC uses novel circuits proposed in this thesis in order to reduce the power consumption while achieving 14-bit performance. Section 7.1 gives an brief introduction. Section 7.2 discusses the proposed SAR ADC architecture and Section 7.3 shows the top layout of the SAR ADC. Section 7.4 shows the top level simulations results of the proposed SAR ADC while Section 7.5 compares the proposed SAR ADC with the current state-of-the-art SAR ADCs. Section 7.6 concludes the chapter.

7.1 Introduction

The SAR ADCs are widely used in the imaging applications where most the imaging sensors require input buffers in order to isolate the ADC from the ROIC and drive the large sampling capacitors of the ADC. In addition to driving capability and isolation, a voltage level conversion is required between the ROIC and ADC. Most of the ROICs operate from a 3.3V supply voltage for the analog circuits and the current ADCs operate from 1.8 supply voltage which is well below the analog supply voltage of the ROIC. In order to perform the conversion, a common-mode voltage shift is required between the two voltage domain. This common-mode voltage shift can be achieved with the input buffers.

Today, the current state-of-the-art SAR ADCs achieve a Walden Figure of Merit below 1 fJ per conversion-step which provides a great reduction in the power consumption. While the current SAR ADCs require very low energy consumption,

the input buffers require large power consumption usually greater than the required power by the SAR ADC. As a result, the overall Figure of Merit is much larger than the values obtained with only core circuit. Unfortunately, in many applications such as imaging and IoT applications, the input drivers are the compulsory circuits, since large sampling capacitors in the SAR ADCs cannot be driven by low-power sensor nodes and image sensors. The sensor nodes and image sensors are designed for battery-powered systems which dictates power reduction. In this thesis, in order to overcome this issue, a novel sampling technique is proposed which does require any power consumption for the implementation. In addition to the novel sampling technique, the proposed DAC switching schemes in this thesis provides extra reduction in the SAR ADC, while the SAR Logic speeds up the conversion by eliminating one of the propagation times in the SAR delay loop. The following chapter will discuss the proposed architecture in detail.

7.2 Architecture

Figure 7-1 shows the block diagram of the proposed SAR ADC with integrated input drivers. The differential inputs of the proposed SAR are labelled as V_{INP} and V_{INN} where the maximum and minimum voltages of the differential inputs are V_{PK} and ground respectively. In the proposed SAR ADC, the input voltage range is 3.6V where V_{PK} equals to 1.8V. Before starting the conversion, the output nodes of the input drivers are disconnected from the inputs of the SAR ADC core and the bottom plates of the capacitors in each of the DAC array are connected to each other, while the top plates of the capacitors are connected to common-mode voltage. By using this sampling technique which employs a simple charge-sharing, the voltage at the output of the input driver approaches to common-mode voltage without requiring any power consumption. This period can be defined as reset period. The input drivers used in this thesis are rail-to-rail input class AB amplifiers in order to achieve a 14-bit performance. Normally, for the resolutions such as 10-bit, instead of using a class AB amplifier, a p-type and n-type simple amplifiers can be used to drive the

sampling capacitor. However, using different input drivers in the high resolution ADCs may bring different nonlinearity due to the process and environmental variations to each of the input of the core SAR ADC which can degrade the performance of the ADC. As a result, to ensure the 14-bit performance, class AB amplifiers are preferred. Following the reset period, the input drivers are connected to the capacitive DAC arrays to start the conversion. Notice that, by using the novel sampling technique, while the differential inputs change from 0 to V_{PK}, the output nodes change from $V_{PK}/2$ to V_{PK} which reduces the output voltage swing. After the sampling phase, the conversion is initiated and 14-bit output data is determined.

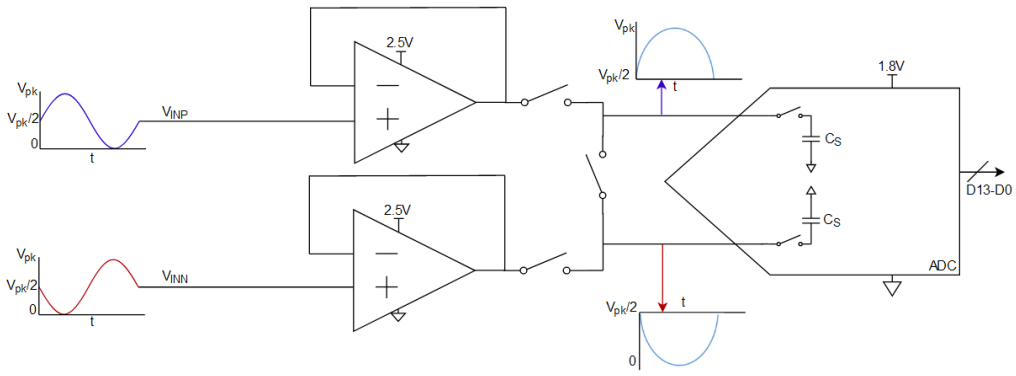


Figure 7-1.The block diagram of the proposed SAR ADC with integrated input drivers.

Figure 7-2 shows the detailed block diagram of the proposed SAR ADC with input buffers. The figure illustrates the comparator with the offset capacitors and additional inverters to speed up the conversion and the DAC array with the switches. Before starting to the conversion, the switches SW1 and SW2 are turned OFF and SW13 turns ON in order to ensure that the bottom plates of the capacitors in each DAC array are at common-mode voltage as a result of charge sharing. Following this reset period, SW13 turns OFF, and S1 and SW2 turns ON to start the sampling. At the same time, SW5 and SW6 are ON to provide a proper sampling. The sampling on the capacitor in the DAC array requires 5 clock cycles to complete the sampling considering the maximum input differential voltage.

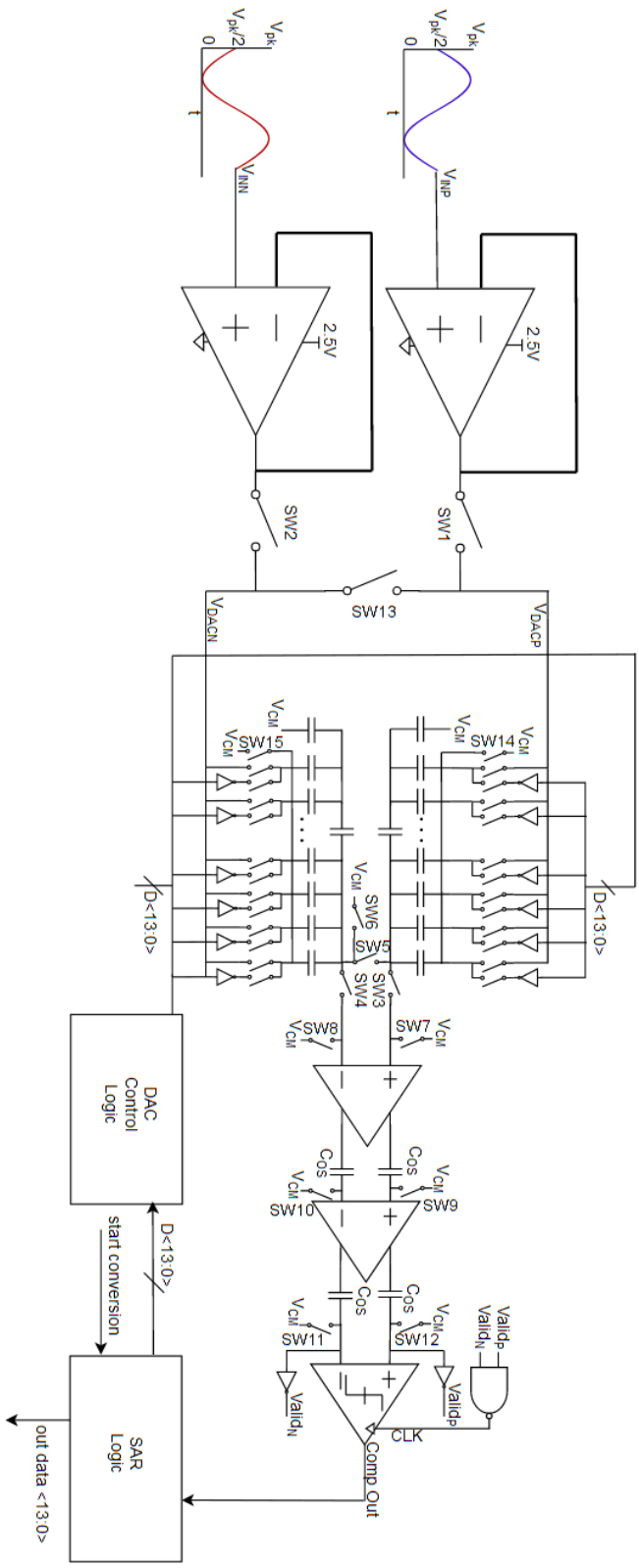


Figure 7-2. Detailed block diagram of the proposed SAR ADC with input buffers.

During the sampling period, SW7, SW8, SW9, SW10 and SW11 are ON to perform offset cancellation whereas SW3 and SW4 are OFF. The switches SW3 and SW4 are used for isolating the comparator from the core SAR ADC. More specifically, at the beginning of the sampling phase, there is an instantaneous voltage spike on the top plates of the DAC array. This instantaneous voltage spike can be defined as kickback voltage which affects the offset cancellation, this scheme has to be completed within 6 clock cycle. The kickback noise leads to unwanted voltage spikes that cannot be recovered easily. For this reason, SW3 and SW4 isolates the comparator and protects the offset cancellation scheme. After the 6 clock cycle including 1 clock cycle reset and 5 clock cycle sampling period and offset cancellation, the conversion is initiated. In the first conversion cycle, the bottom plate of each capacitor in the DAC arrays is connected to the common-mode voltage while SW5 and SW6 are OFF. In this first conversion, the sampled voltage on the capacitors is pushed to the top-plate without any energy consumption. Then the first comparison is performed and the latch in third stage of the comparator makes a decision. The clock signal of the latch is generated from the output of the second stage of the comparator. When the outputs of the second stage exceed a certain value which is adjusted for the worse cases, the clock signal is fired to start the operation of the latch. In the MSB comparisons, whenever this clock signal is fired, the latch makes a decision, which speeds up the conversion for the MSBs. By accelerating the comparison, more time for the settling of the MSB capacitors can be allocated. Therefore, the SAR ADC can operate at high frequencies such as 160 MS/s. The output of the comparator is stored in the SAR Logic which generates the required signal for the DAC arrays. Between the SAR Logic and DAC arrays an additional circuit called as DAC Control Logic is implemented to adjust timing for the switches connected to the bottom plates of the capacitors. Normally, by using shared-type switches, this block is not required. However, in order to minimize the number of switches, mux-like switch topology is implemented that requires a DAC control logic circuit. In the next clock cycle, the DAC arrays are updated depending on the previous comparison result. Until the last bit called as LSB, the conversion continues. At the end of 14 clock cycle, the

conversion is ended and the SAR Logic generates a flag signal to indicate the end of the conversion. When the flag is signal is fired, the output data is sent to an additional memory and the output data is sent outside of the chip in parallel.

Figure 7-3 shows a simple waveform of the outputs of the DAC array with sampling signal and clock signals. The signals labelled as bottom_plate_bR and bottom_plate_R are the output nodes for each of the DAC array while phi_latch is the clock signal generated from an external processor and clk_inv_in is the clock of the inverters at the output of the second stage. During the sampling period, the output of the DAC arrays are at the common-mode voltage. In the sampling phase, in order to eliminate any kickback voltage at the output of the first and second stage of the comparator, the clock signals are turned OFF. The inverters at the output of the second stage is a dynamic inverter which makes a decision faster than the conventional inverter architectures. In addition, the sampling period requires 5 clock cycles for proper sampling operation and the comparator needs 6 clock cycles for the offset cancellation.

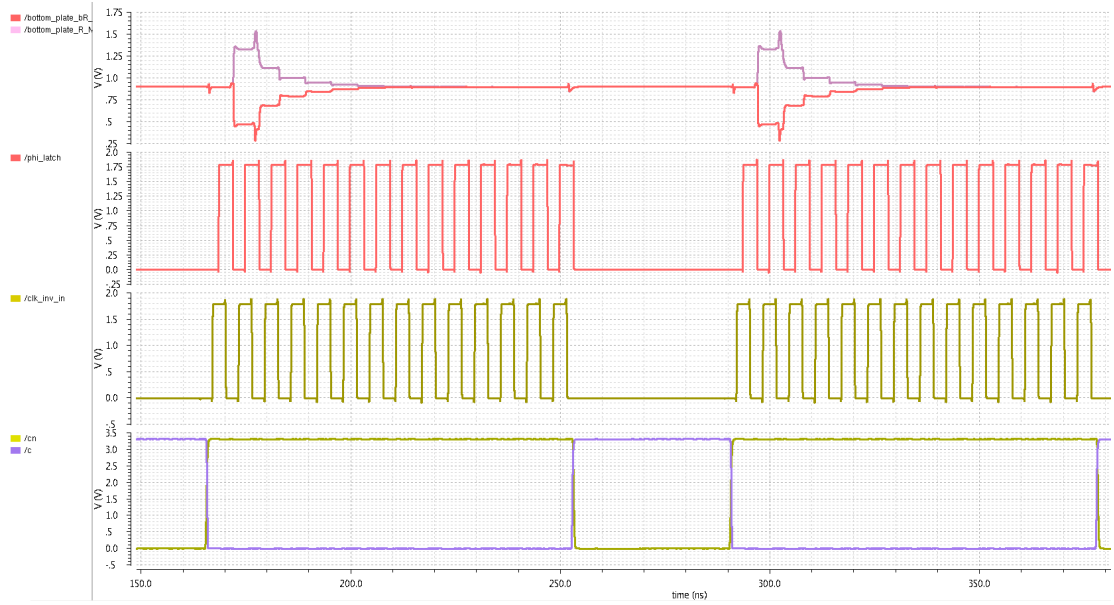


Figure 7-3. Waveform of the outputs of the DAC array with sampling signal and clock signals.

7.3 Top-Level Layout

Figure 7-4 shows the top layout of the core of the proposed ADC. It measures 1.2 mm x 0.7mm. The auxiliary blocks such as digital controller, and bias generator are not shown in here. The proposed ADC will share the digital controller, and bias generator in the ROICs, so that the common blocks are not included into the top layout. The proposed SAR ADC is placed at the right side of the ROIC. The size of the ROIC is constant, and there is no extra silicon area top and bottom of the pixel array. The proposed SAR ADC has a layout which extends through vertically in order to fit in the overall layout. The size of the comparator layout requires more silicon area when adding the power routings. Thick power lines are required to eliminate the resistances coming from the layout and avoid the voltage drop at the comparator. The layout of the DAC arrays occupy less silicon area compared to the conventional layouts, since the number of unit capacitors are minimized by using the novel DAC switching methods. On top of the layout of the DAC array, the switches are drawn. In order to minimize the routings between the DAC arrays and the switches, the DAC arrays and switches are placed next to each other. The resistances and capacitances coming from the layout may affect the settling performance of the capacitors. The DAC control logic is placed on the switches. The DAC control logic is used for generating the required signals to control the switches. As it was mentioned above, the mux-like switch topology is used in this thesis. For this reason, a more complex control logic is required to perform the conversion. Below the input drivers, the SAR Logic is placed. The SAR Logic and the DAC control unit should be placed as closed as possible, since the ADC operates at 8 MS/s, the clock frequency is 160 MHz. If the routings are too long, then the load may require extra settling time which may not be sufficient for the conversion. In addition to the layout of the each block, the high speed signals in the layout should have shields to avoid coupling and loading problems. The frequency of the clock signal is 160 MHz, and the length of the routing is too long due to the size and placement of the pad. For this reason, there are some repeater buffers between the digital controller and the core of

the ADC in order to ensure that there is no driving problem. Furthermore, for this signal, the shields are also clock signals. Normally, for shielding, ground is used to avoid any coupling between the clock and the other signals. However, ground leads to loading problem between the clock signal and itself. In order to overcome this problem, two additional clock signal are used to shield the main clock signal and the ground signals surround the clock shields. As a result, the main clock only sees itself which do not cause any loading problem. Figure 7-5 shows the top layout of the SAR ADCs with the ROIC. As it was mentioned before, the proposed SAR ADC is placed at the right side of the ROIC. There are totally 6 ADC channels which 2 of them are used for testing. The ROIC will operate with 4 channel operation. Although the layout of the single SAR ADC occupies small silicon area, the peripheral circuits such as bias generator, digital controller and buffer require more silicon area. However, the peripheral circuits are not in the scope of this thesis.

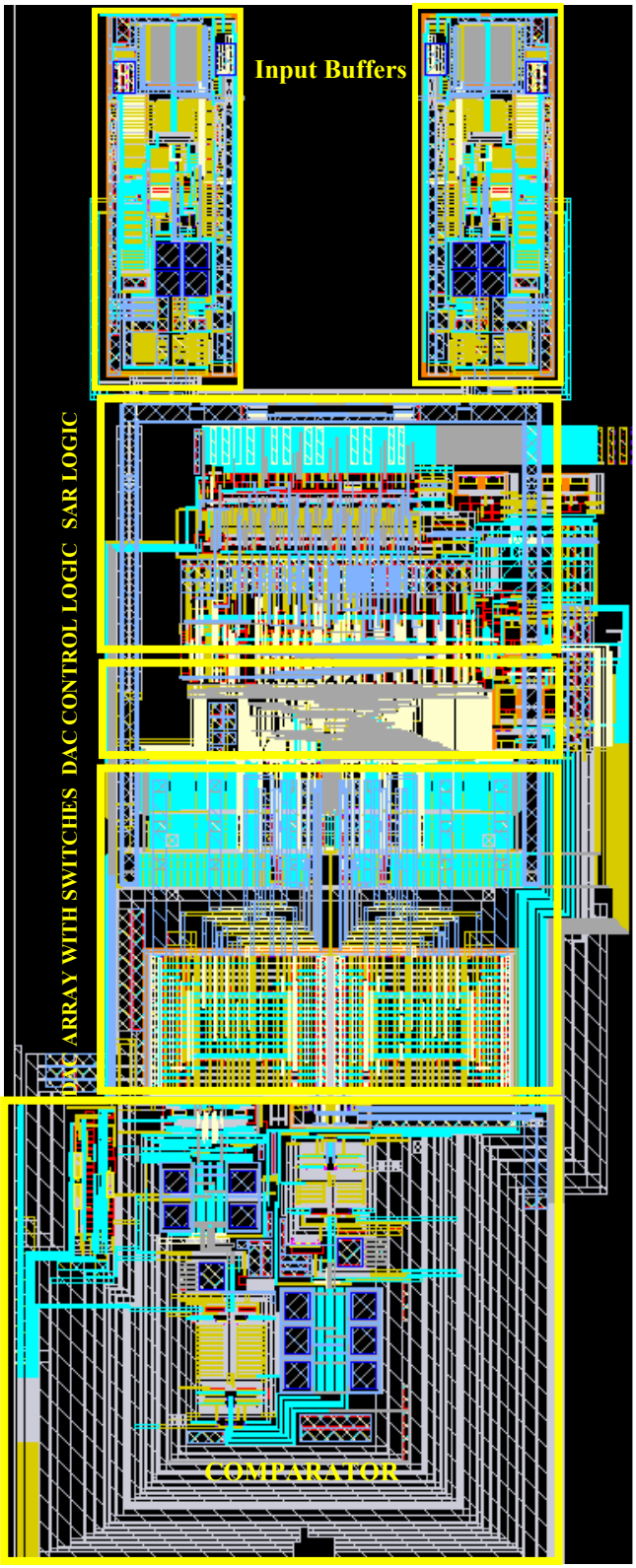


Figure 7-4. Top layout of the proposed SAR ADC including the input drivers and core circuit. It measures 1.2 mm x 0.7mm.

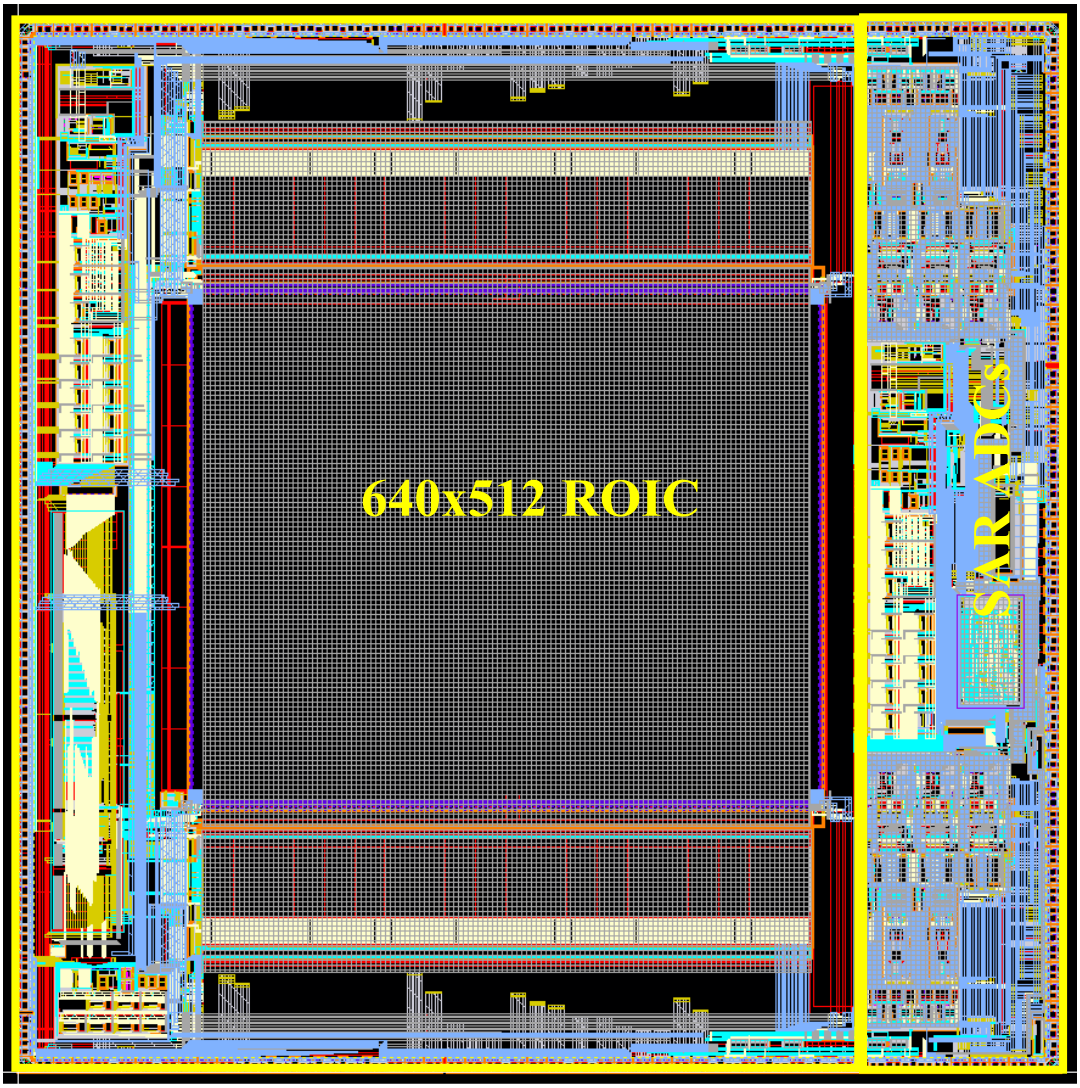


Figure 7-5. Top layout of the SAR ADCs with the ROIC.

7.4 Top-level Simulations

The top level simulations shows the results of the important nodes under worse speed (ws) and typical case which are the two important corners for the SAR ADC. There is another corner called as worse power (wp) in which the transistors have low threshold voltages, achieving better results compared to the ws case. For this reason, in this section ws and normal cases are investigated to observe the performance of the SAR ADC when the differential input voltage is 538µV which is 3 LSB voltage. Figure 7-6 shows the outputs of the differential DAC array under typical case. In sampling mode, the top plates of the capacitors in the DAC arrays are connected to the common-mode voltage. Following the sampling phase, the bottom plates are connected to the common-mode voltage, while the top plates become float and the voltage at the top plate equal to the summation of the sampled voltage on the capacitor array and the common-mode voltage. The first comparison is then performed and the SAR Logic updates the DAC arrays according to the result of the first comparison. The conversion continues until the last decision. The clock signal is fired to start the operation of the latch.

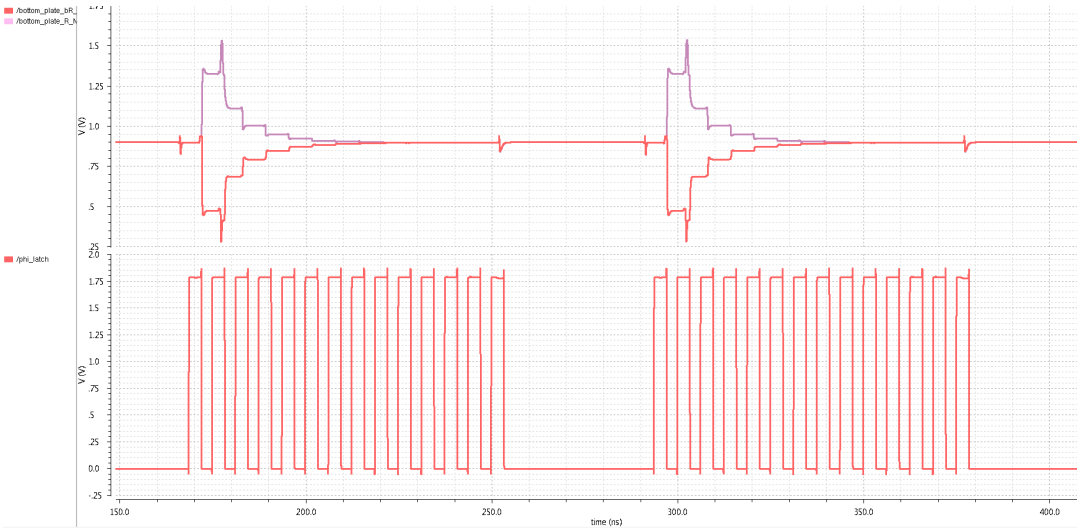


Figure 7-6. Outputs of the differential DAC array under typical case.

Figure 7-7 shows the outputs of the comparator. The comparator has 2 gain stages followed by a latch to make a decision. The signals labeled as outn1, outp1, outp2_int and outn2_int are the outputs of the first stage and second stage respectively. Due to the fact that, the second stage drives additional inverters, the settling of this stage requires more time compared to the settling of the first stage. This difference can be observed during the offset cancellation schemes. Note that at beginning of the simulation, the voltages at the output of the each stage are random which are determined by the simulation. As a result, in the first conversion, the offset cancellation can be completely performed. In the next conversions, this problem is recovered and the simulations shows the correct result. In order to isolate the comparator and avoid kickback voltages in the comparator during the offset cancellation, switches are used at the input of the first stage. The signals labeled as outn and outp at the top of the figure shows the results of the latch. The waveform of the outputs of the latch is similar to a typical StrongArm Latch. Then, from the outputs a comparator valid signal is generated to fire the SAR Logic in order to start the next conversion cycle.

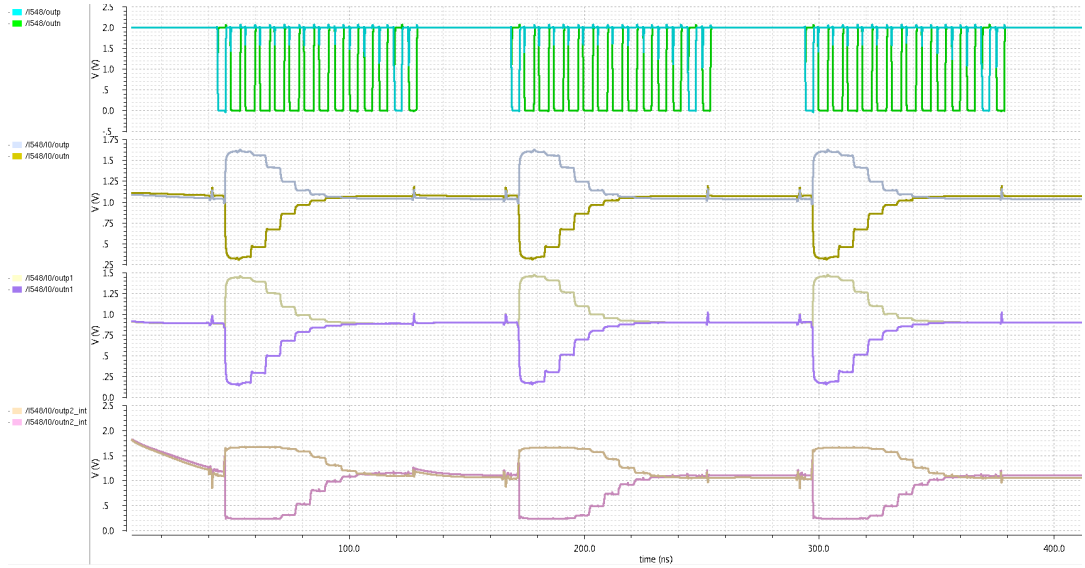


Figure 7-7. Outputs of the comparator.

Figure 7-8 shows the output data of the SAR ADC when the input is 538 µV. This differential voltage equals to 3 LSB voltage and the expected result is "10000000000010" which is similar the results obtained from the simulation. The outputs are sent to an additional memory circuit to store and sent them to outside of the chip in parallel. This simulation is performed under normal condition. However, the chips should be simulated at the corner cases. The next simulation is performed under worse speed (ws) case.

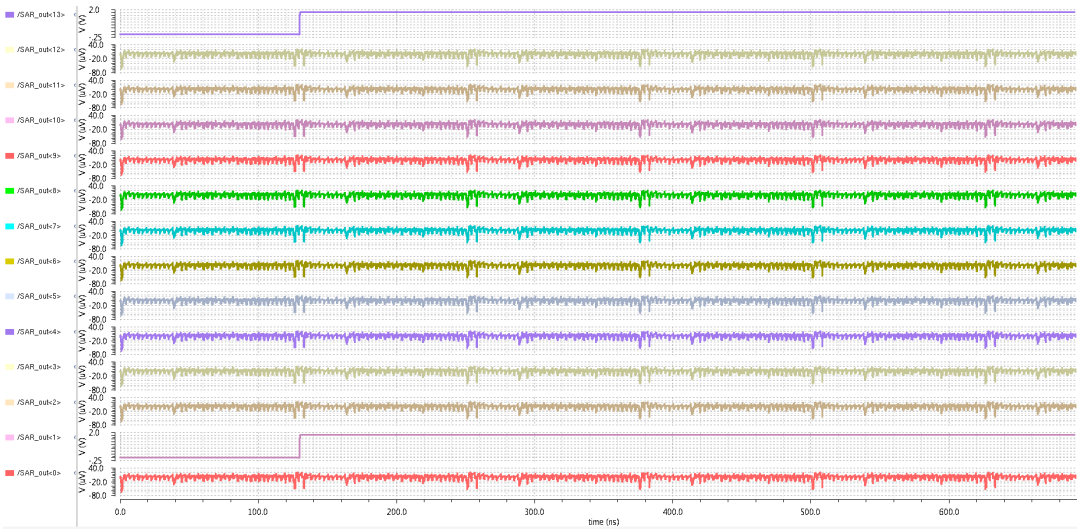


Figure 7-8. Output data of the SAR ADC.

Figure 7-9 shows the output of the differential DAC array under worse speed (ws) case. It is observed that under the worse speed case, the outputs of the DAC arrays do not change. In this corner, the transistors have larger threshold voltages and larger C_{OX} capacitances while the mobility of the transistors are lower. For this reason, it is very important to simulate the circuit in the corner.

Figure 7-9. Outputs of the differential DAC array under worse speed (ws) case.

Figure 7-10 shows the outputs of the comparator under worse speed case. In this case, the common-mode voltage of the comparator approaches to 1.1V. This voltage shift is due to the feedback circuit in each of the stage, since the feedback circuit depends on the process parameters of the tail transistor. For this reason, the common-mode voltages alter at the process corners, but it does degrade the performance of the circuits, since it is used for comparison. The gain of the each stage in the comparator slightly decreases, since the mirror operation and the bias current slightly changes, but the required gain is obtained at the process corners. Figure 7-11 shows the output of the SAR ADC. Since the comparator can suppress the process variations, the output of the comparator is same compared to the previous result.

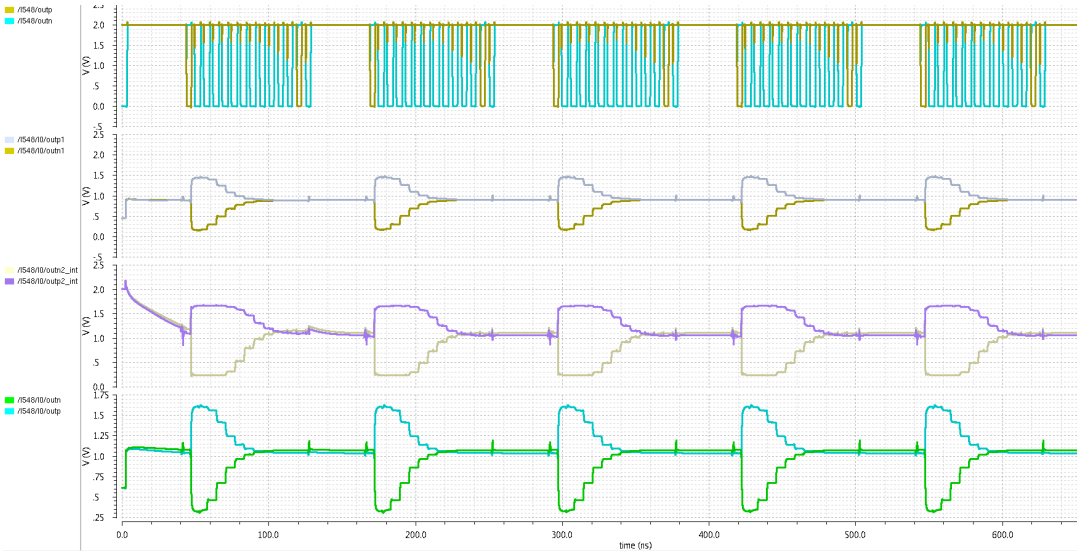


Figure 7-10. Outputs of the comparator under worse speed case.

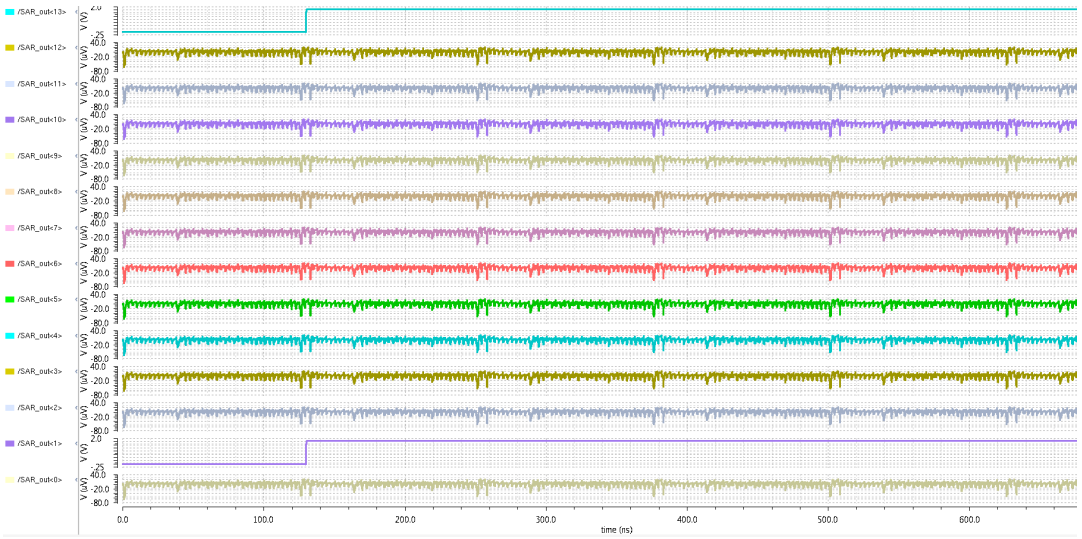


Figure 7-11. Output data of the SAR ADC under worse speed case.

The dynamic performance of the SAR ADC is another important factor. In order to evaluate the SAR ADC, a simple sine wave at 1MS/s is used in the full range. The sampling frequency of the SAR ADC is 8 MS/s. The results shows that the SNDR is 80.38 dB, while considering the settling of the capacitors in the DAC arrays. The result includes the capacitors mismatch which is 2.3 % in the given technology node. When the capacitor mismatch is included, the DNL changes between 0.4 LSB and -0.95 LSB while the INL alters between -1.85 LSB and 1.35 LSB. Under normal conditions, the expected INL and DNL are between -0.5 LSB and 0.5 LSB, since there is no mismatch. Adding the mismatch changes the charge equations at the top plate of the DAC arrays which lead to INL. The DNL obtained by using this SAR ADC is between -1 LSB and 1 LSB which ensures that there is no missing code. The INL may not be a problem for the imaging sensor. It only leads to static problem which can be recovered by using calibration algorithms. In this thesis, an off-chip calibration scheme will be implemented to correct the INL and DNL respectively.

7.5 Literature Comparison, and Summary

In summary, the proposed SAR ADC achieves the ADC specifications mentioned before. The results based on the simulations shows that the proposed ADC integrates the input buffers into the core circuit without excessively increasing the power consumption of the overall ADC. Table 7-1 shows the comparison between the state-of-the art ADC designs, and the proposed ADC. The proposed SAR ADC reaches a Walden FoM 92.2 fJ/conv-step which is comparable to the state-of-the-art SAR ADCs while achieving high-resolution.

Table 7-1 Comparison between the state-of-the-art ADC design, and the proposed ADC.

		Bindra [86]	**Kramer [92]**	**Tseng [93]**	**Kim [94]**	**This Work***
Technology		65nm	40nm	28nm	65nm	**180nm**
Supply Voltage [V]	ADC	1.2	1.2	1.1	0.9	**1.8**
	Buffer	1.2	2.5	2.5	1.2	**2.5**
Max. Sampling Rate [MS/s]		4	35	104	80	**8**
Nyquist Bandwidth [MHz]		2	17.5	52	1	**4**
$ENOB_{Nyq}$		8.73	12.1	7.2	12	**13.06**
Differential swing (pk to pk [V])		2 V_{PP}	1.8 V_{PP}	1.2 V_{PP}	1.8 V_{PP}	**3.6 V_{PP}**
Total Power Consumption		0.15 mW	54.5 mW	3.1mW	2.1mW	**6.3mW**
Walden FoM (fJ/conversion)		87	355	200	133	**92.2**

***** Simulation Results

The proposed SAR ADC operates with 1.8V and 2.5 supply voltage. The state-of-the-art ADCs use supply voltages below 1.8V for ADC core. As a result, they can reduce the power consumption of the overall ADC compared to the proposed ADC. In addition, the proposed SAR ADC is implemented using 0.18 µm CMOS process. For this reason, in order to achieve a fast conversion rate at this technology, the transistors require large gate-source voltage to turn on the transistor, since the threshold voltages are larger in this technology. Therefore, larger bias voltages are required to implement this thesis. The work proposed in [72] uses the same voltage for both the core circuit, and input buffers, but the input voltage range is limited compared to the proposed SAR ADC. In addition, the proposed ADC has a 14-bit resolution which is greater than the state-of-the-art designs. The effective number of bits (ENOB) in this thesis is 13.06 that provides an 80.3 dB SNDR. The linearity

results of the proposed SAR ADC shows that the DNL range is sufficient to ensure that there is no missing code, considering the mismatches in the unit capacitors. The INL exceeds 1 LSB which may not be a problem for the image sensors. The DNL is more important for the imaging applications, since it may bring blurring effects. The proposed SAR ADC has a large input voltage range compared to the previous SAR ADCs which can relax the specifications for the comparator at the cost of power consumption. If the input range is not rail-to-rail, then the input buffer can demand lower power compared to the proposed input driver in this thesis.

In conclusion, in this thesis, an optimized SAR ADC with an integrated input buffers is proposed to achieve a high-resolution which can be used in the imaging applications.

7.6 Conclusion

This chapter discusses the top level integration of the proposed SAR ADC. The chapter starts with the introduction of the proposed SAR ADC architecture. The architecture includes the input drivers and core circuits which uses the proposed novel techniques in order to reduce the power consumption of the SAR ADC, while achieving a 14-bit performance. The results shows that, the mismatches in the capacitive DAC array degrade INL performance of the proposed SAR ADC while the DNL is within the expected range. The INL may not be a problem for the imaging application and it can be corrected by using advanced calibration algorithms. The results of the simulations shows the expected values after fabrication, since the simulations include finite settling of the DAC array, sampling noise, comparator noise and capacitor mismatches in the DAC arrays.

CHAPTER 8

CONCLUSION AND FUTURE WORK

8.1 Conclusion

Analog-to-digital conversion is very important for sensing, acquisition, and data transmission. Over the years, researchers has focused on decreasing the energy consumption of the core ADC and Walden FoM approaches to under 1fJ-conv-step. However, the interaction between the core of the ADC and the peripheral circuitry such as input drivers has not been explored in detail. For this reason, ultra-low-power core ADCs have to be operated with power hungry input drivers and peripheral circuits. This thesis investigated the energy reduction methods not only for the core of the ADC but also for the input drivers and proposed design solutions that minimize the overall energy consumption of an ADC and input driver.

Chapter 1 gives an overview of image sensors and the basic information about the ADCs. This chapter introduces fundamental concepts about the ADCs such as dynamic parameters, static parameters, and Walden Figure-of-Merit. The chapter shows the main reason of selecting the SAR ADC architecture among the other data converter architectures for a low power image sensor application. Finally, the organization of the thesis is provided.

Chapter 2 focuses on the generic SAR ADCs before implementing at transistor level. The chapter introduces the basic SAR algorithm, investigates possible charge-redistribution DAC architectures, and studies on the nonlinearities due to the process variations. In addition to the DAC architecture, the basic parameters of the comparator is extracted and investigated.

Chapter 3 focuses on the implementation digital-to-analog converters (DAC). This chapter starts with the design of a DAC architecture. The DAC architecture has a split capacitor architecture with an integer number of bridge capacitor and dummy capacitors. In order to reduce the power consumption of the DAC architecture, this thesis proposes 3 different novel switching scheme. First switching scheme is the most power efficient scheme among the proposed schemes while the common-mode voltage shifts from V_{CM} to 1.5 V_{CM}. This common-mode voltage shift can be compensated by a comparator, but it requires additional circuits. In order to overcome this limitation, the second DAC switching scheme is proposed. In this scheme, the common-mode voltage does not change at the expense of consuming switching energy in the second cycle. The third proposed switching scheme reduces the switching energy further while eliminating the third reference voltage which can be used in the high resolution SAR ADCs. However, due to the fact the MSB capacitor is split into sub capacitors, this scheme requires more switches and control logics compared to the previous schemes. For this reason, for the proposed ADC, the second proposed DAC switching scheme is the perfect solution in terms of area, switching energy and the number of switches.

Chapter 4 discusses the design of a comparator. There are 2 different comparators in the proposed SAR ADC. The first comparator is the coarse comparator which is designed by the floating inverter amplifier followed by a second stage and strong-arm latch. A novel 2-level latch provides additional gain while reducing the power consumption of the latch. The noise and power consumption of the proposed coarse comparator is better compared to the previous solutions. Apart from the coarse comparator, the fine comparator has 2 pre-amplifier stages followed by a gm-boosted strong-arm latch with dynamic inverters to speed up the conversion. The fine comparator makes fast decisions for the MSB comparisons, and allocate more time to LSB conversions. The SAR logic in the proposed SAR ADC has novel logical blocks in order to accelerate the operation.

Chapter 5 reviews the current analog front-end circuitry for the SAR ADCs. This chapter investigates the possible input sampling techniques. The proposed input

sampling technique in this thesis reduce the output voltage swing at the input buffers by using simple charge sharing technique which does not require any active power consumption. This method can be implemented into high resolution ADCs without any requirement and does not depend on the technology node which can be used in advanced nodes.

Chapter 6 explains the architecture of the SAR Logic and peripheral circuit. The SAR Logic in the proposed SAR ADC speeds up the conversion by eliminating an extra propagation delay due to the shift register. The conventional SAR ADCs have 2 row shift registers in which one row shift register fires the second row shift register. For high speed application, the time for firing the second shift register should be very small to complete the conversion.

Chapter 7 discusses the top level integration of the SAR ADC. It includes the top level architecture of the proposed SAR ADC. The proposed SAR ADC uses the novel sampling techniques proposed in this thesis, while employing the new DAC switching scheme in order to reduce the energy consumption of the DAC arrays. The simulation results shows that a Walden FoM of 92.2 fJ/con-step which is the lowest among all the reported buffered SAR ADCs for 14-bit resolution to the best of my knowledge.

8.2 Original Contributions

- A floating inverter amplifier with novel second stage is demonstrated to reduce the power consumption while providing comparable noise.
- 3 different DAC switching schemes are proposed to reduce the switching energy of the proposed ADC. The proposed DAC switching schemes not only reduce the switching energy but also the number of switches and reference voltages compared to the existing methods.
- A novel input sampling method by using simple charge sharing method is proposed to reduce the voltage swing of the input buffer. The proposed

method does not consume power while providing 50% reduction in the voltage swing. The previous methods require additional circuits and power consumption to reduce the voltage swing at the output of the input buffers.

- A novel SAR Logic that speed up the operation which is very important for high speed applications.

8.3 Future Work

Firstly, this thesis investigates solutions for the reduction of the power consumption of the SAR ADC and concentrates on the integration of the input buffers into the core ADC. In addition to the input drivers, the reference driver should be on-chip in order to provide a clean reference voltage while demanding low-power. As a future work, the reference voltage should be generated within the chip. Furthermore, due to the wirebonds inductances, the reference voltage has some instantaneous peaks which can degrade the performance of the SAR ADC. These problems can be eliminated with on-chip reference voltage generators.

Secondly, the power of the fine comparator can be decreased by using dynamic amplifiers in the first stage. This thesis uses classic offset cancellation schemes for the offset cancellation which are suitable for the static amplifiers. The dynamic amplifiers require advanced calibration algorithms for removing the offset voltage. If a new calibration algorithm is used, dynamic amplifiers can be used for the pre-amplification phase. As a future work, advanced calibration algorithm and dynamic amplifiers can be used to reduce the power consumption of the SAR ADC.

Thirdly, the input drivers can be optimized to reduce the power consumption. In this thesis, class AB amplifiers are used for obtaining 14-bit performance. By reducing the output swing further, class A or class B amplifiers can be sufficient for the conversion. Therefore, new input drivers can increase the performance of the ADC.

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