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A 4096 channel event-based multielectrode array with asynchronous outputs compatible with neuromorphic processors

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Bio-signal sensing is pivotal in medical bioelectronics. Traditional methods focus on high sampling rates, leading to large amounts of irrelevant data and high energy consumption. We introduce a self-clocked microelectrode array (MEA) that digitizes bio-signals at the pixel level by encoding changes as asynchronous digital address-events only when they exceed a threshold, significantly reducing off-chip data transmission. This novel MEA comprises a 64 × 64 electrode array, an asynchronous 2D-arbiter, and an Address-Event Representation (AER) communication block. Each pixel operates autonomously, monitoring voltage fluctuations from cellular activity and producing digital pulses for significant changes. Positive and negative signal changes are encoded as "up" and "down" events and are routed off-chip via the asynchronous arbiter. We present results from chip characterization and experimental measurements using electrogenic cells. Additionally, we interface the MEA to a mixed-signal neuromorphic processor, demonstrating a prototype for end-to-end event-based bio-signal sensing and processing.

As we usher in an era of pervasive computing, we are witnessing an exponential proliferation of devices and systems designed to aid us in our daily lives. These systems are very diverse, ranging from localization devices to biomedical sensors. Still, they are all expected to operate continuously at minimal energy cost while facing the daunting task of ensuring the secure real-time interpretation of the generated data. This is especially true in the realm of biosensors that continuously monitor our bodily state through various signals. These include neural signals, manifested as action potentials and measured by electroencephalogram (EEG), cardiac signals manifested as extracellular field potential and recorded as electrocardiogram (ECG), as well as glucose and insulin signals. The current data inundation from these sensors necessitates the development of custom hardware that can process signals locally without the need for offline bulky backend computers or cloud servers. Biosensors, particularly those with many channels such as the ones employed in electrophysiological studies such as multielectrode arrays (MEAs), are experiencing a trend towards higher channel counts, for simultaneous recording from as many as 235k channels[1]. If encoded using a classical digital sampling approach, the bio-signal measured by a typical channel produces about 200 kbps, making scalability and off-chip transmission critical in terms of both bandwidth and power consumption[1–7]. Although innovations in recording systems, such as time-multiplexing techniques and sophisticated sampling schemes, have allowed for simultaneous recording from an increasingly large number of electrodes, the practical scalability of these systems remains difficult. Furthermore, most electrophysiology studies are primarily interested in the timing and shape of action potentials. Consequently, a considerable portion of the

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acquired data ends up being discarded only after costly post-processing techniques. This highlights the need for more efficient data acquisition and processing techniques that can better focus on the features of interest online, ultimately enabling more efficient online and closed-loop bio-signal processing systems[8].

In parallel, neuromorphic sensors[9–13] have emerged as a paradigm-shifting solution for low-latency and power-efficient signal processing. Unlike traditional sensing technologies that output a continuous, clocked stream of data, neuromorphic sensors are asynchronous and event-driven. Event-based sensors only respond to significant changes in the signal, thus drastically reducing data traffic and, subsequently, power consumption. Their clock-less, or self-clocked, operation bypasses the power-hungry high-frequency clock requirements, making them well suited for real-world edge, pervasive, and ubiquitous computing applications. Furthermore, when neuromorphic sensors are synergistically paired with neuromorphic processors[14–17], they unlock unprecedented potential, enabling sophisticated real-time signal processing[18] that can handle high temporal resolution requirements[19,20], rapid pattern recognition[21,22], and adaptive learning, challenges[23] that traditional systems often struggle with.

Within this context, in this paper, we present a fully event-based microelectrode array biosensor called GAIA (Global Asynchronous Intelligent Array). The GAIA system uses neuromorphic circuits to encode signals generated from bioelectric cells directly at the pixel level, generating and transmitting data only when relevant events, such as an action potential, occur.

Here, we first introduce the GAIA chip architecture, characterize the circuitry within each pixel, and characterize the signal encoding block (level-crossing ADC). We then demonstrate the ability of the sensor to detect bioelectric signals, and, finally, we validate GAIA with a beating cardiomyocyte culture. Going a step further, we interface GAIA to a mixed-signal event-based neuromorphic processor, demonstrating a proof-of-principle end-to-end neuromorphic sensing and processing pipeline. Figure 1 outlines the full event-based pipeline: time-continuous sensing, sparse asynchronous event generation, and, finally, spike-based processing. This novel combination represents an important step toward achieving an efficient, scalable, and adaptable sensing system that elegantly captures the spatio-temporal dynamics of biological systems while at the same time significantly reducing the amount of data transmitted off-chip.

Results

GAIA's distinct advantage lies in its adaptive data transmission approach: by outputting an asynchronous digital event only when detecting a local relative voltage change that surpasses a preset threshold, it favors the encoding of meaningful biological signals with large transients and discards noise and small fluctuations. Intuitively, our approach is based on the assumption that relevant biological signals exhibit voltage transients significantly higher than the noise floor. This unique data handling strategy makes the output data solely dependent on the detected activity of the signal, and since the activity of bioelectric cells is sparse in both space and time, it significantly reduces the overall output data[24].

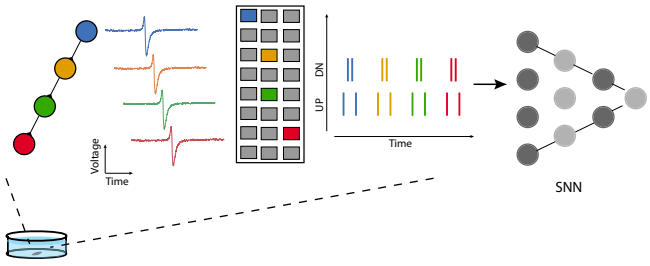

Fig. 1 | Schematic overview of GAIA's operating principle and benefits. Graphical representation of the working principle of the event-based 4096-channel GAIA sensor. The signal is sensed and compressed at the pixel level, enabling sparse and compressed data transmission off-chip. The new data topology is particularly well suited for on-line processing with Spiking Neural Networks (SNN).

The event-based microelectrode array

Figure 2a shows an overview of the 4096-channel GAIA MEA system. It consists of a central 64 × 64 pixel core, flanked by two X and Y address encoders, and an address event representation (AER)[25] communication block. Each electrode measures 15 × 15 μm^2, and the pitch between electrodes is 48 μm. Figure 2b shows a block diagram of the signal path within each pixel: it includes two adjustable gain stages (A1-A2), an event generation stage, and a reset stage. A large reference electrode, 10 μm in width, is positioned on the perimeter of the sensing array.

The A1-A2 amplifiers were designed to amplify signals in the 1 Hz–10 kHz range while rejecting the large DC component at the electrode-tissue interface. The amplitude of signals of interest can vary considerably and typically have amplitudes that range from 50 μV to 1 mV depending on the distance to the electrode and the cell type. The initial amplification stage (A1 - in red in Fig. 2b) is a single-ended common-source amplifier in which the gain is regulated by an adjustable current source. A tunable gate in the pseudo-resistor modifies the low cutoff frequency corner[26]. The pseudo-resistor in A1, working with the C_{in} capacitor, establishes a very low-frequency pole, stabilizing the original zero. The signal is subsequently AC-coupled to a variable gain amplifier (A2 - in green in Fig. 2b), where the C_c/C_f ratio determines the gain, offering eight configurable settings. Further details of the circuitry within each pixel are available in Supplementary Material 1.

The event generation block (in yellow in Fig. 2b) emits two digital types of events (UP and DN), depending on the direction of the signal variations[27]. These are linked to a four-phase asynchronous handshaking block, managing data transmission through asynchronous signals. Generated UP or DN pulses correspond to AER interface requests (REQ). The REQ signal will elicit an acknowledgment (ACK) signal from the downstream processing, resetting the comparator output.

Arbiter and AER interface

Each channel is integrated within an array. This array communicates asynchronously with peripheral circuits through a handshaking mechanism[25,28,29]. Upon event generation, the pixel raises a request signal (REQ) indicating its readiness for data transmission[30,31]. A 2D-arbiter system encodes this event's location using a unique (X,Y) address and event polarity (ON or OFF). This results in a 13-bit digital address: 6-bit each for X and Y addresses, complemented by an ON/OFF polarity bit. The structure of this 2D arbitrator can be seen in Fig. 2c.

To ensure a smooth handshaking process, the target receiver verifies all digital REQ events created on the chip. These signals employ a bundled data (BD) representation, where the 13-bit digital address is portrayed as a parallel word. This word is then accompanied by two supplementary REQ and ACK signals for handshaking control. The timing scheme of the asynchronous four-phase handshake, as well as the timing of the reset signals, is shown in Fig. 2e. In scenarios where multiple pixels simultaneously produce Address Events (AEs), the arbitration block comes into play to prevent signal interference. This block sequentially queues and transmits events over a shared bus, ensuring a collision-free environment. The peak throughput of the GAIA system is measured to be 20 mega events per second (Meps).

Figure 2d elucidates the method through which each pixel accesses this shared bus. To relay data, a pixel pulls the shared REQ line to ground, using a local pull-down transistor, signaling the need for event transmission. Recognizing this action, the downstream arbiter

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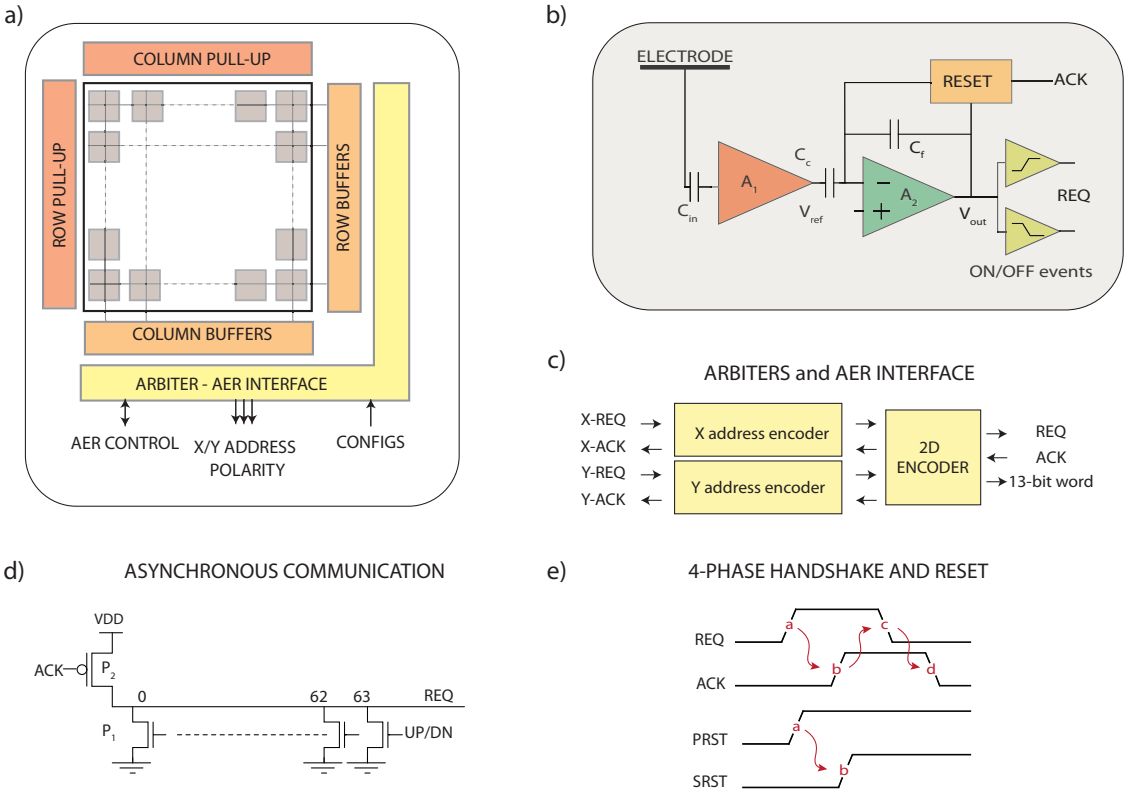

Fig. 2 | Detailed breakdown of the CMOS GAIA event-based microelectrode array. a High-level system architecture depiction. **b** Close-up view of the circuit elements within each pixel. **c** A schematic diagram illustrating the arbiter and address event representation hierarchy. **d** Core asynchronous communication components showing pull-up and pull-down transistors, responsible for generating and transmitting Request (REQ) and Acknowledgment (ACK) signals. **e** Temporal sequence of the 4-Phase handshake protocol fundamental to asynchronous communication on top. On the bottom, is the sequence of reset signals.

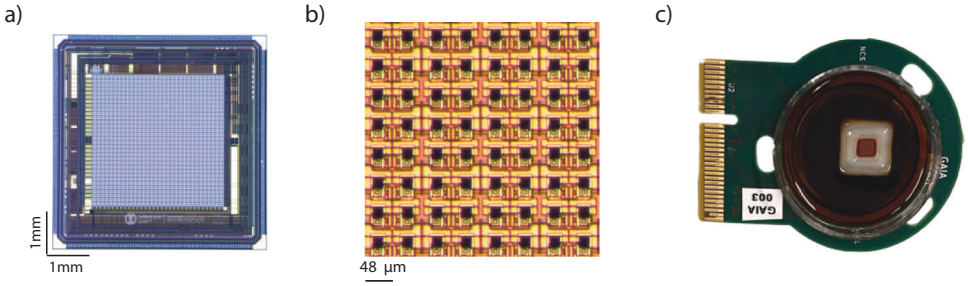

Fig. 3 | Micrograph and post-processing details of the GAIA chip. a Micrograph showcasing the GAIA chip with dimensions of a 5 × 5 mm^2 die and an active area of 3 × 3 mm^2. **b** Microscope image of the post-processed electrode array. The electrodes have a size of 15 × 15 µm^2 and are spaced squarely with a pitch of 48 µm. A small area of 4 × 6 electrodes is highlighted: the exposed top electrode is visible. **c** Image of the finalized, fully packaged chip. Following post-processing, the chip was affixed to a daughterboard PCB, encapsulated using a biocompatible epoxy resin, and subsequently coated with Pt-black to minimize electrode impedance.

returns an ACK signal to a global pull-up transistor within the common line, thereby resetting the REQ signal. This allows for subsequent event transmissions.

To enhance system fairness and efficiency, we adopted a 2D non-greedy arbiter[32,33]. Such arbiters strive to allocate equal access to the shared bus among competing nodes. The principle is simple: an arbiter will not acknowledge the same client consecutively, only proceeding after all other waiting clients have been attended to. This approach increases fairness, minimizes potential system congestion, and improves the overall performance of the system.

Characterization of amplifier gain, noise, power consumption, and latency

Figure 3 shows the micrograph of the GAIA chip, the electrodes, and the fully packaged chip. The electrical properties of GAIA were characterized by applying a 1 mVpp sinusoidal input and sweeping its frequency from 0.1 Hz to 10 kHz. Figure 4a illustrates the transfer functions that characterize the A1-A2 amplifier chain for various gain settings. The lowest and middle gain settings yield in-band amplifications of 37.4 dB and 48.1 dB, respectively. The gain can be programmed up to 57 dB. Additionally, by altering the bias of the A1 pseudo-resistor, the high-pass corner can be changed. We characterized the noise levels of the chip by sweeping the input frequency and amplitude using a spectrum analyzer. Figure 4b displays the signal-to-noise-distortion ratio (SNDR) as a function of the input amplitude. The dynamic range for the lowest gain setting is 37.9 dB, with a peak SNDR of 37.2 dB. Moreover, Fig. 4c demonstrates the power spectral density (PSD) of the input-referred noise across GAIA's operational bandwidth. The integrated input-referred noise in the 500 Hz–3 kHz band is 19.04 µV, while in the full 5 Hz–10 kHz bandwidth is 71.05 µV.

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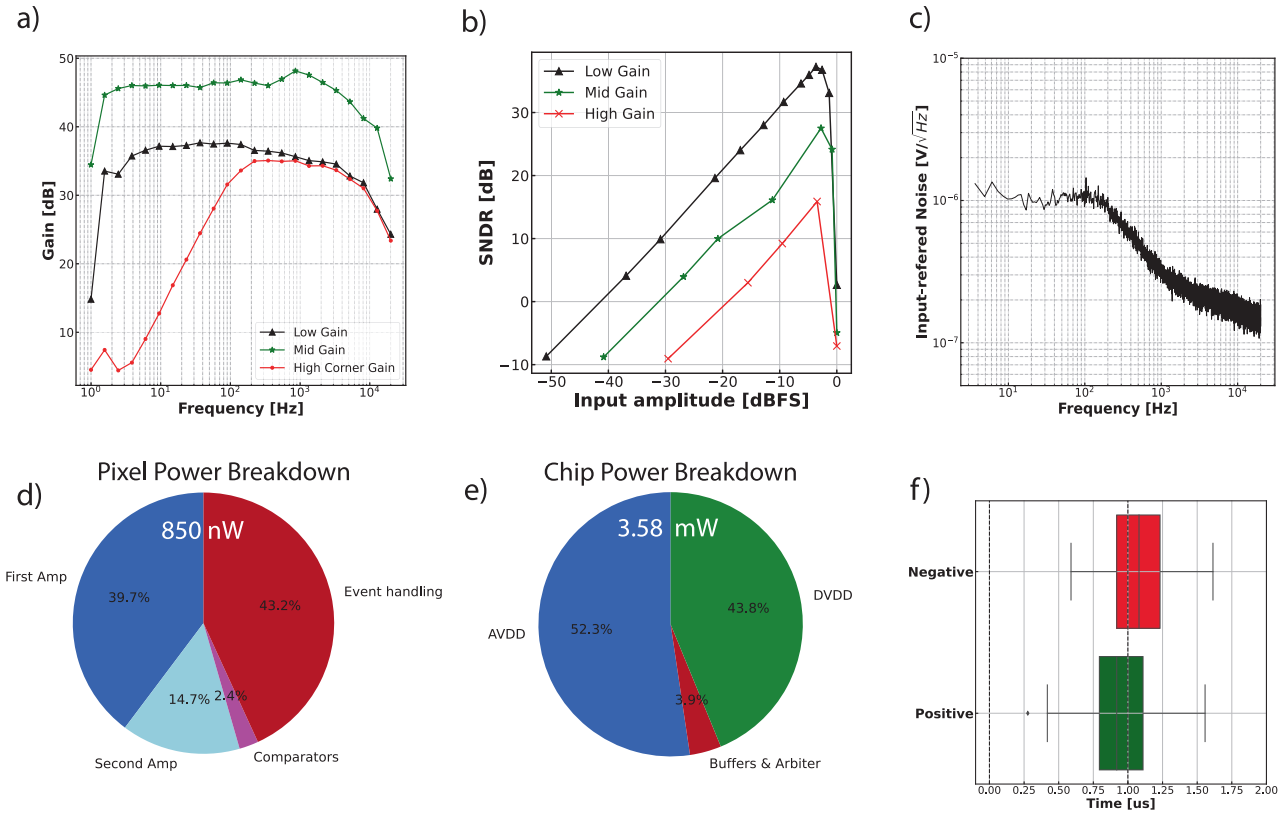

Fig. 4 | Electrical characterization of the GAIA microelectrode array. a Transfer functions of the A1-A2 amplifier chain across different gain settings. The amplifier offers eight programmable gain levels: the lowest (illustrated in black) is at 37.4 dB, the middle (shown in green) at 48.1 dB, and the high-pass filter corner can be adjusted (highlighted in red) via the A1 pseudo-resistor bias settings. **b** Signal-to-noise-distortion ratio (SNDR) plotted against input amplitude. At the lowest gain setting (depicted in black), the dynamic range is 37.9 dB with an SNDR of 37.2 dB. **c** Power spectral density representing the input-referred noise over the operational bandwidth of GAIA. Notably, the integrated input-referred noise within the 500 Hz–3 kHz range amounts to 19.04 μ*V*. **d** Detailed breakdown of power consumption for individual structures within a single pixel. Power sources for analog and digital components are depicted in blue and red, respectively. The total power consumption is 842.4 nW per pixel. **e** Comprehensive power consumption analysis for each power supply, resulting in an overall chip consumption made up of 3.58 mW. **f** Assessment of response latency for both positive and negative events, with an average latency measured at 0.9995 μs.

The power consumption of a single pixel is 842.4 nW. Figure 4d illustrates the contributions from various pixel structures. The analog and digital components within the pixel are supplied separately; the amplifiers are supplied with analog power (in blue), while the digital structures within the pixel receive digital power (in red). The total power consumption of the chip, including the pixel core and the 2D-arbiter, amounts to 3.58 mW. Figure 4e displays the breakdown for each power supply. Power calculations were performed using nominal biases, with a 2 kHz event rate response from each pixel.

The pixel response latency was assessed by measuring a single pixel's response to a low-frequency square wave. The sensor generates a positive event on every rising edge and a negative event on every falling edge. Figure 4f displays the latency for both positive and negative events. The average latency is 0.9995 μs, and the 1-sigma response jitter is 0.2798 μs. As expected, positive events exhibit lower latency than negative events due to design choices within the pixel. For layout symmetry purposes, the comparators are designed using transistors of the same size. Positive events are generated from an n-FET-based comparator (with electrons as majority carriers), while negative events are produced from a pFET-based comparator (with holes as majority carriers). The lower mobility of holes compared to electrons causes the pFET comparator to switch more slowly, resulting in higher latency for events with negative polarity. Characterizing latency using a single pixel is also valid for the larger array, as the pixel's response time is assumed to be orders of magnitude larger than the propagation time of digital events through the gates of the arbiter tree.

Increasing the number of channels in the GAIA system to 19,586, equivalent to the system described in ref. 3, would result in a proportional increase in power consumption due to the additional channels. Currently, each channel consumes ~850 nW; thus, scaling up to 19,586 channels would increase the total power to 16.6 mW. Furthermore, as the power associated with the AER system would rise at a sublinear rate due to the binary encoding of the address space, and as the activity is expected to be sparse, this part would not have a significant impact on the total power budget.

Event characterization

Following the initial electrical and functional characterization of GAIA, we characterized the event generation encoding at the core of the innovation of GAIA.

Figure 5a presents the asynchronous delta modulator (ADM) encoding of a 1 kHz sine wave. The original sine wave, single-channel events, amplified signal, and event-generating thresholds are all superimposed. A digital UP (DN) event is produced when the amplified signal exceeds (falls below) a configurable threshold, resetting the amplified signal to A2's positive output terminal. The placement of thresholds can be freely adjusted. Intuitively, the closer the thresholds, the more events will be generated, resulting in a denser or sparser encoding of the original signal. Figure 5b shows a 1 kHz sine wave encoded with different degrees of sparsity. Given known thresholds, the precise timing of the UP/DN events produced by the event-

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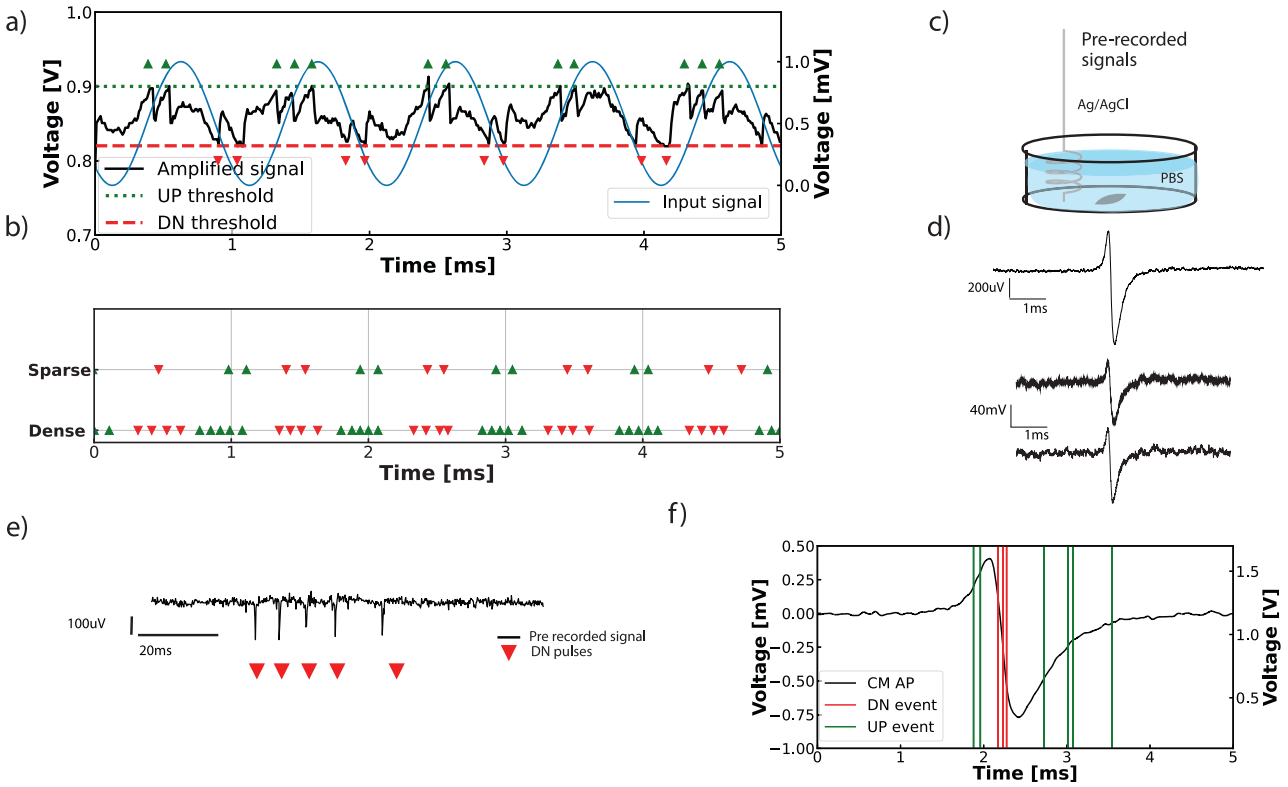

Fig. 5 | Event characterization of the GAIA microelectrode array. a Encoding of a 1 kHz sine wave. The original waveform (in blue) is amplified (in black) by the A1-A2 amplifier chain. When the amplified signal crosses the upper threshold (in green) or falls below the lower threshold (in red), positive or negative events are triggered, respectively. After crossing a threshold, the amplified signal is reset to a reference voltage, allowing the AC dynamics to persist. **b** The density of events can be influenced by the width of the thresholds, resulting in either denser (bottom) or sparser (top) event patterns. **c** Experimental setup employed to assess GAIA with bioelectric signals. A function generator is connected to an Ag/AgCl electrode submerged in PBS (phosphate buffer saline) solution. **d** Previously recorded cardiomyocyte extracellular field potential (top) and its corresponding sensed and amplified signal through the GAIA amplifier chain. **e** DN events (bottom in red) produced in response to a pre-recorded neural signal (top in black). **f** UP (in green), and DN events (in red) produced in response to a single pre-recorded cardiomyocyte extracellular field potential.

generating ADM circuitry contains all the information about the original input signal[34,35] (Signal reconstruction is available in the Supplementary Material section 5). To ensure our approach is effective, we aim to position the thresholds above the noise level to only capture large extracellular signals.

To fully characterize the on-chip amplification and event generation of GAIA, we tested the system using previously recorded signals. A function generator was connected to a silver-silver chloride electrode, which was submerged in phosphate-buffered saline (PBS) solution and positioned inside GAIA's recording chamber. Figure 5c illustrates the setup. The conductive PBS solution allows the signal from the function generator to be detected by all electrodes on the array. Using a previously recorded signal allowed us to test GAIA's response to a real extracellular potential through the electrode signal pathway and the entire encoding pipeline.

Figure 5d displays a previously recorded cardiomyocyte extracellular field potential (top) and the same signal amplified by GAIA's A1-A2 amplifiers (bottom). The top trace was previously recorded using another MEA[7] platform and used to evaluate the GAIA system. Figure 5f demonstrates the event encoding response for the same cardiac extracellular field potential signal. The extracellular field potential's stereotypical waveform is effectively encoded into an asynchronous stream of UP-DN-UP events on the chip. Figure 5e shows the response of GAIA to previously recorded neural signal. The neuronal signal (on top) and the corresponding response of the DN channel (on bottom) are displayed. The pixel accurately detects the input spike trains, demonstrating the capability of the system to encode and transmit biologically relevant signals.

Experimental results

To rigorously validate the GAIA platform, we recorded from a cardiomyocyte culture. Cardiomyocytes generate periodic signals[36–38] (at 1Hz), making them exemplary candidates for characterizing novel MEA systems.

Human-induced pluripotent stem cells (hiPSC) differentiated into cardiomyocytes were used for this validation process. Cardiomyocytes were seeded onto the GAIA sensor and kept in a humidity-controlled incubator. Recordings began on day seven after plating, providing sufficient time for the cells to aggregate and synchronize their beating patterns spontaneously. Throughout multiple days of observation, the cell culture remained stable, displaying a beating frequency that ranged from 50 to 90 beats per minute (bpm). The main outcomes of the cell culture experiment are described in Fig. 6. The histogram in Fig. 6a outlines the total number of events over a 20-second span. Each histogram peak corresponds to an extracellular field potential wave. The cells exhibit a beating frequency of 67 bpm. A deeper dive into two histogram peaks is presented in Fig. 6b. Specifically, it shows UP and DN events for each electrode generated by two distinct field potential waves. Each wave signal has a consistent origin and propagation pattern, resulting in similar footprints in the event space.

Figure 6c extracts the wave propagation velocity based on the spatial location of the electrode and the timing of the events generated. The extracted propagation velocity is 0.11 mm/ms. Finally, a confocal microscope was used to validate the viability of the tissue and ensure that the extracted beating frequency was correct. A snapshot from the microscope is shown in Fig. 6d, where the cell nuclei (in blue) and the cytoskeleton (in red) are highlighted.

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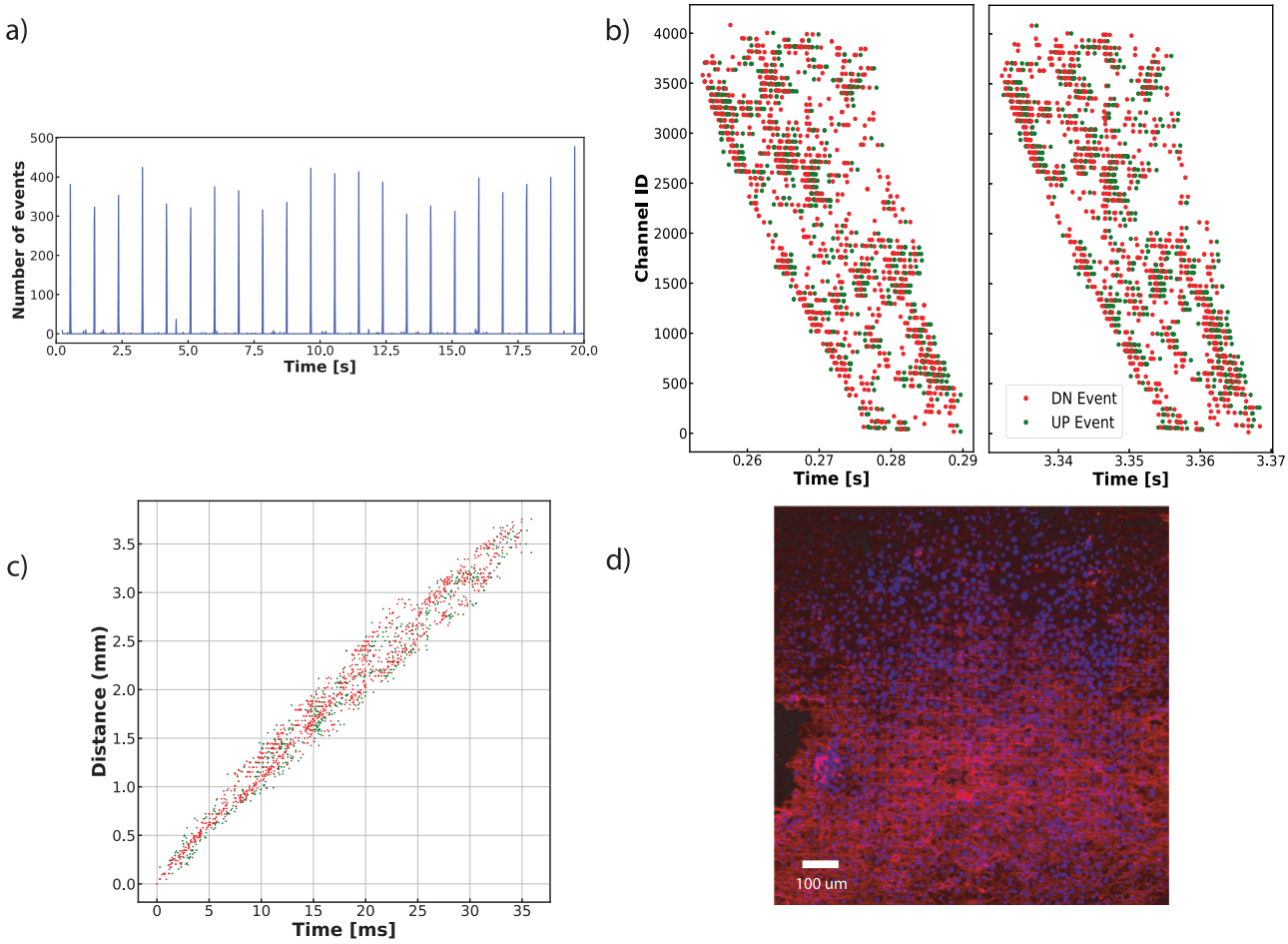

Fig. 6 | Analysis and visualization of cardiomyocyte activity on GAIA sensor. **a** Histogram showcasing the event distribution from GAIA over a 20s duration. Periodic peaks, resulting from the spontaneous beating of the CMs, reveal a frequency of 67 bpm. Each peak represents the extracellular field potential in response to a beat event. **b** Illustration of two distinct beating events. The *x* axis represents time, and the *y* axis indicates the Channel ID, emphasizing clear signal propagation. Uniformity in the recorded beating shapes indicates the signal's consistent origin and propagation pattern. **c** Estimation of the propagation speed of the extracellular field potentials, with an estimated velocity of 0.11 mm/ms. **d** Confocal imaging of cardiomyocyte cell culture on the GAIA sensor. Cytoskeletons in red are stained with SIR-Actin, while cell nuclei in blue are stained with NucBlue, Hoechst 33342. Imaging proves cell viability and optically validates the measured beating frequency.

Expanding upon these results, Fig. 7 provides a wealth of information that delves deeper into the propagation of electrical activity. It graphically presents a time series of the events sensed in response to an extracellular field potential wave as it travels across the entire array. Each detected wave follows a consistent trajectory, originating from the array's lower right and culminating at its upper left (also shown in Fig. 6b). Crucially, a wave of DN events is succeeded by a wave of UP events. This sequence mirrors the biphasic dynamics characteristic of EFPs. An additional graphical representation of the data and further analysis are available in the Supplementary Material sections 6 and 7.

In terms of data efficiency, the average unfiltered event rate output from the 4096 GAIA channels amounts to 10 kevs, signifying a dramatic reduction when compared to conventional sampling methods that can require up to 200 kbps per channel. This stands as a testament to GAIA's capability of compressing large amounts of data into manageable streams.

It is important to acknowledge that the hardware specifications of GAIA are not compatible with the signal levels and noise requirements to record from live neurons. We have, however, successfully shown that the overall approach works and is successful in recording from live cardiomyocytes and from pre-recorded signals as control inputs.

Spiking neural network interfacing

GAIA's production of a wholly novel type of data enables an array of exciting possibilities. Building on the results presented, we successfully interfaced GAIA's event-based outputs to an event-based mixed-signal neuromorphic processor. This integration aims to harness the benefits of both hardware components, laying the groundwork for their potential unification into a singular monolithic system. Here, pixel and neuron computations occur in the analog domain, while spike routing is managed digitally.

The union of GAIA's advantages with the real-time analysis capabilities of neuromorphic processors promises significant advancements in the realm of hardware-based neural computation. While several existing neuromorphic processors could serve as a proof-of-concept[15,16,39,40], we elected to employ the mixed-signal DYNAP-SE[14] processor (described in Supplementary Material section 8) to demonstrate a fully mixed-signal processing pipeline. The analog properties of silicon neurons and synapses have been extensively described[41–43]. Here we focus on two system-level network motifs. The first network is a spike detection motif that uses a single analog silicon neuron to detect spikes from a single GAIA channel. It relies on the integration of UP and DN events through different excitatory input synapses to create coincidence detection filters[44]. Digital UP events are

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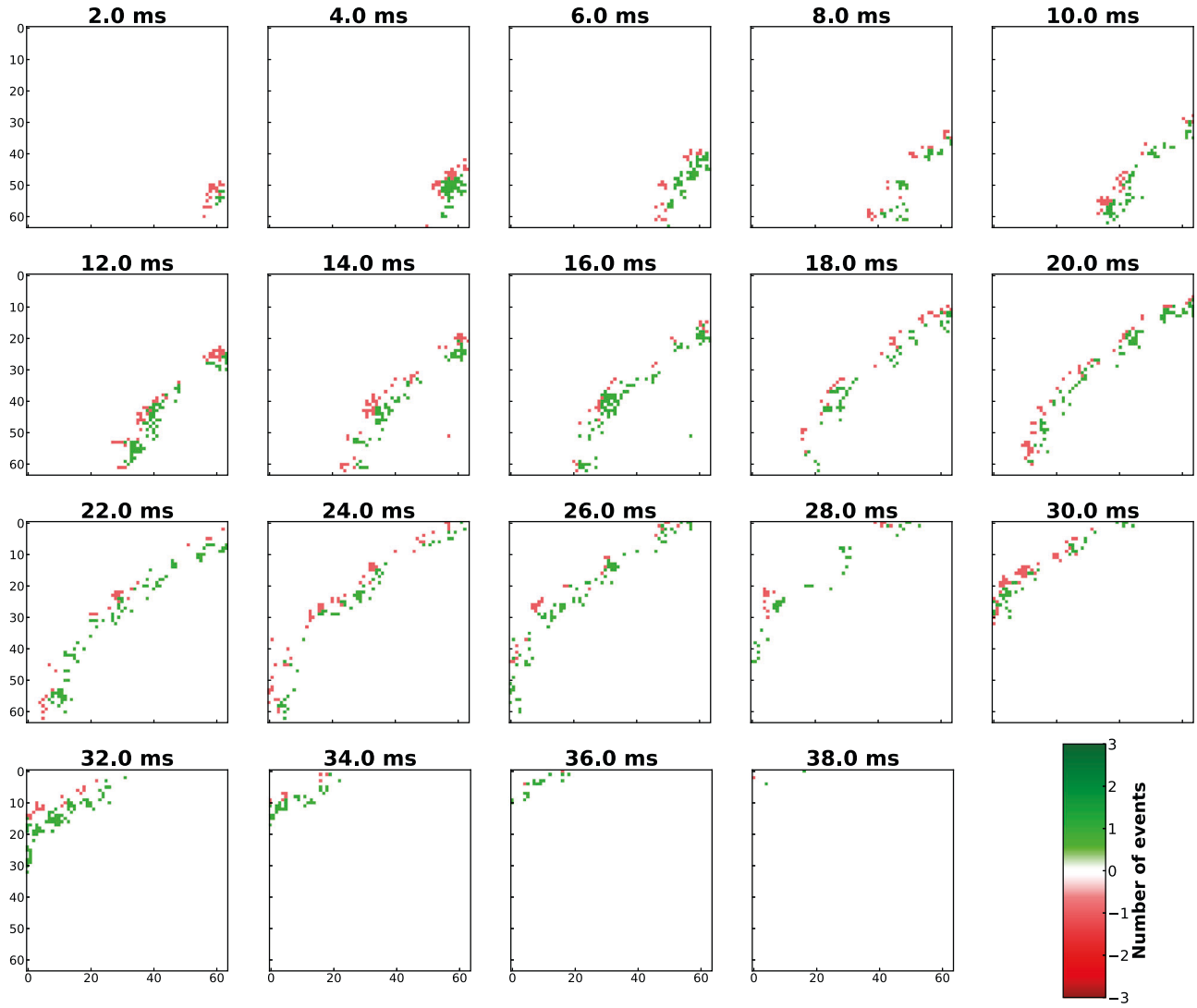

Fig. 7 | Propagation of extracellular field potential (EFP) wave. Time surface showing the propagation of electrical activity from a single EFP wave across the entirety of the GAIA chip. The activity is calculated over a 2 ms time window with an exponential decay parameterized by $\tau = 2$ ms. Negative and positive events (in red and green) are encoded from the biphasic shape. Notably, within the time frames presented, the total counts for UP and DN events are 1130 and 1111, respectively. Although it might seem that there are more UP events, this is because they represent the trailing edge of the wave, thus occurring closer to the snapshot time, making them appear more prevalent.

integrated via NMDA-like silicon synapses, while digital DN events are integrated via AMPA-like silicon synapses[45]. Both synapses are emulated via dedicated circuits on the DYNAP-SE processor. As in their biological counterpart[46], silicon NMDA synapses are voltage-gated circuit blocks wherein the output synaptic current is enhanced by the effect of a recent AMPA synaptic event boosting the neuron membrane potential. The resulting non-linear synaptic summation mechanism is leveraged in the spike detection network to trigger an output spike only when subsequent DN-UP events occur within a short time window. Figure 8a, b shows the described spike detection motif and the selectivity to spike time and polarity, respectively. Figure 8c shows, on the bottom, the raw, unfiltered data from a subset of GAIA channels and, on the top, the DYNAP-SE events generated in response to the data. The coincidence detection between different polarity events is a strong de-noising filter on the single output spikes. The on-chip spike detection network successfully responds only to close successions of DN-UP events while correctly silencing events due to noise. The second network uses the same principle to process the entire GAIA array within a single DYNAP-SE core. To map the full GAIA array into a single DYNAP-SE core, we coarse-grained the 4096 pixels into a 16×16 grid. Each grid element was connected to a single analog on-chip neuron. The coarse-graining approach allows the processing of the entire GAIA MEA within a single core. The synaptic biases and the time constants of the synapses and of the neuron have been tuned to ignore the background noise and limit false positives. Figure 8d shows the response over time of the DYNAP-SE core. The main panel shows periodic beating, while the bottom zoomed-in image focuses on detecting a single EFP wave event. Silicon neurons show a clear progression at the time of detection, consistent with the movement of the EFP wave. In conclusion, we have showcased a proof-of-concept of a fully mixed-signal processing pipeline. The sensing and processing inside GAIA and DYNAP-SE occur in the analog domain and the data transmission in the digital one.

Advantages and drawbacks of GAIA

As delineated in Table 1, the performance metrics of the GAIA system are compared to existing state-of-the-art MEA devices, providing a comparative perspective. GAIA stands out prominently due to its unique event-based asynchronous nature: the output data rate is solely determined by the sensed extracellular activity. The analog pixel

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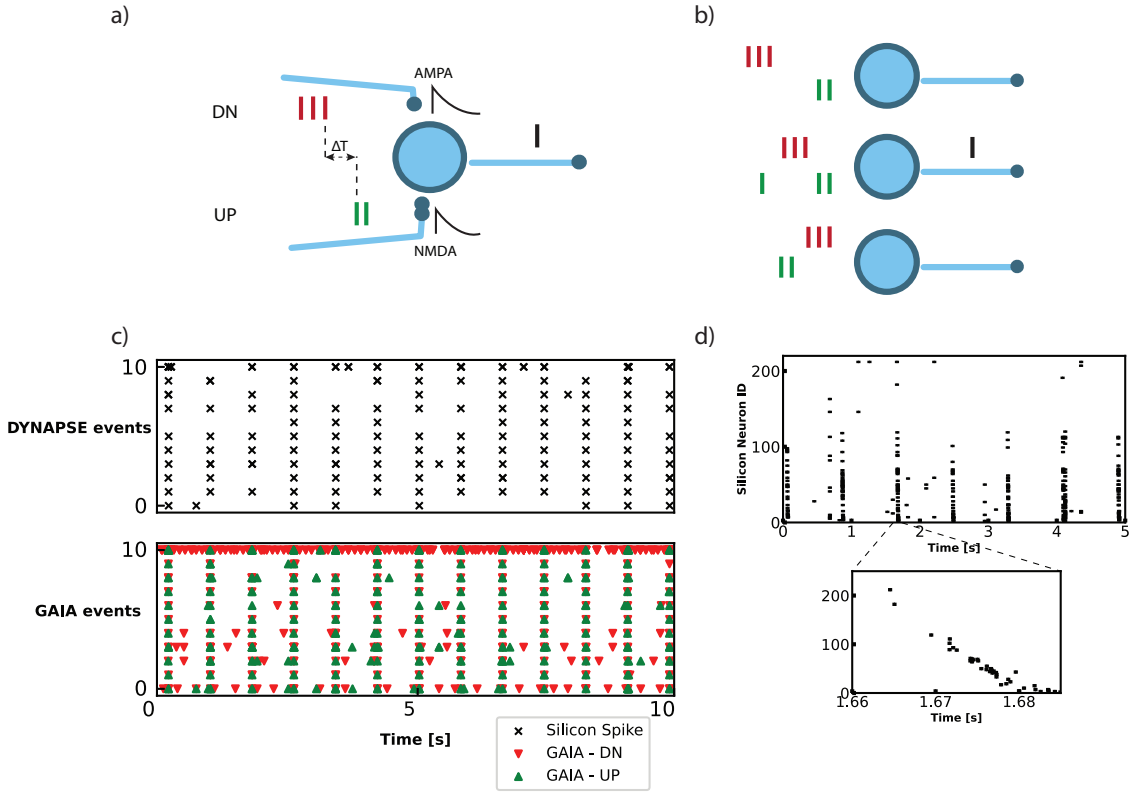

Fig. 8 | GAIA-DYNAP-SE interface. a Spike detection motif. UP and DN channels are connected to different synapses, filtering the incoming digital spikes with different time constants. **b** The network is tuned to respond only when a sequence with the correct polarity and the correct timing is presented (middle). If the timing (top) or the polarity is inverted (bottom), the silicon neuron is silenced. **c** Raw GAIA events (bottom) are processed by the DYNAP-SE processor (top). The silicon neurons on the DYNAP-SE spike only in response to a close succession of DN-UP GAIA events. **d** Neuron-IDs of a full DYNAP-SE core responding to raw, noisy input recorded by GAIA.

Table 1 | Comparison of state-of-the-art MEA systems

	This work	ref. 3	ref. 5	ref. 6	ref. 7	ref. 1
Technology [nm]	180	180	180	130	180	90/65
Die size [mm]	5 × 5	6 × 8.9	-	19.2 × 10	12 × 8.9	32.5 × 25.1
Pixel pitch [μm]	48	18	25	15	13.5	11.72
No electrodes	4096	19,586	65,536	16,384	59,760	2,36,880
No readout-channels	4096	19,586	65,536	1024	2048	2,36,880/33,840
Sampling rate	<1 μs latency	11.6 kHz	20 kHz	20 kHz	20 kHz	10/70 kHz
Input-referred noise	19.04	10.4	26	7.5	2.5	5.5
[μV_{RMS}]	(500–3 kHz)	(300–5 kHz)	(100–10 kHz)	(100–3 kHz)	(300–10 kHz)	(300–10 kHz)
Power/channel [μW]	0.8	5.9	-	19.8	42	130

electronics combined with asynchronous encoding collectively enable superior energy efficiency and reduced latency. However, the intrinsic nature of asynchronous event-based systems renders time-multiplexing unfeasible, and requires dedicated circuitry at each pixel. This poses a challenge in achieving an optimal balance between electronics size, which influences overall noise levels, and the physical spacing between electrodes, which dictates spatial resolution. Building upon the architecture of GAIA, its event-based design offers expansive opportunities for scalability. The inherent strength of signal compressing at the pixel level, of the arbiter design, combined with its efficient bandwidth, suggests that the present 64 × 64 configuration could seamlessly evolve into larger pixel arrays, echoing advances seen in vision sensors[47]. However, it is vital to acknowledge inherent challenges: with the pixel's active design, transmitting digital data over extended wire lengths within an analog computational environment introduces vulnerabilities to noise disturbances and potential coupling issues. In addressing the pixel pitch and input-referred noise challenges in the GAIA MEA system, it is essential to recognize the direct consequences of our novel encoding method on these parameters. The larger 48 μm pitch and elevated noise levels are the results of our commitment to an active pixel sensor design, integrating all amplification and event generation blocks within the pixel area. This approach, while increasing pixel size and noise, is a deliberate trade-off to leverage our unique event-based sensing capabilities. Looking forward, advancements such as hybrid architectures or lower technological nodes present promising avenues to mitigate these challenges, potentially reducing both pitch and noise without compromising the system's innovative encoding and spatial resolution capabilities. Moreover, the input-referred noise does not directly affect power consumption and robustness.

Discussion

As traditional multichannel biosensors follow a synchronous clocked data sampling scheme, they are limited in the number of channels they can record from simultaneously due to fundamental bandwidth and power constraints. The work we presented here bridges the gap between direct extracellular sensing and event-based technology, offering a new approach for real-time bioelectric sensing and monitoring. The GAIA sensor proposed evolves classical MEA designs by harnessing event-based encoding, offering benefits such as enhanced energy efficiency and improved scalability. Each pixel asynchronously converts the detected extracellular potential into a stream of digital events. GAIA significantly reduces redundant data at the pixel level, by initiating data generation and transmission only upon significant signal changes, such as single action potentials or large extracellular field potentials. This, in turn, eases the strain on data management and processing frameworks.

Another notable achievement of this paper is the demonstration of an integrated event-based MEA device with a mixed-signal neuromorphic processor. This combination demonstrates the practicality of combining event-based biosensing with neuromorphic processing, suggesting a roadmap for future edge biosensing applications.

The findings and developments presented in this paper set the stage for further exploration in the MEA and biosensor sector. Event-based technology in this context opens new avenues for research and optimization. Moreover, as showcased by direct sensing and processing integration, the potential for edge devices paves the way for more decentralized, efficient, and real-time solutions.

In summary, this work presents a novel technological approach and offers a practical blueprint for the next generation of bioelectronic interfaces, emphasizing real-world applicability and efficiency.

Methods

IC fabrication

The chip was fabricated using a standard 180 nm CMOS 6M1P process. Information on transistor sizing is available in the supplementary materials section 2. The dies were wire-bonded onto custom-made printed circuit boards (PCBs) for effective integration. PCBs were designed using the open-source Kicad software.

Post-processing, packaging, and Pt-Black deposition

For biocompatibility and usability, a three-phase post-fabrication protocol was employed. First, the chips were post-processed in a cleanroom to fabricate stable platinum electrodes and to isolate the electronics from the culturing media. The GAIA CMOS chip was post-processed at the die level. Platinum electrodes were manufactured on the electrode array using a shifted-electrode layout[48]. Three masks were used to deposit a SiO_2/Si_3N_4 passivation stack over the entire chip. Reactive-ion etching was used to create openings in the passivation to create the final $15 \times 15\,\mu m^2$ electrodes and for the wire bonding contacts.

Secondly, the chips were packaged with epoxy and a glass ring to ensure adequate insulation and to avoid leakage of the culturing media. Finally, Pt-black was deposited on the bright Pt electrode surface following a previously published protocol[49]. All electrodes were connected, and a static current of 500 µA was applied for 40 s. Figure 3 shows the micrograph of the GAIA chip, the electrodes, and the fully packaged chip.

Data pipeline

An XEM7310 FPGA (Opal Kelley, USA) board was used to interface the GAIA chip. Custom drivers were developed in System Verilog to digitize, timestamp, and pipeline incoming events. Custom C++ software was built to visualize and process incoming digital events. The same software controls the analog biases and digital latches on the GAIA chip. Additional information is available in the supplementary material section 4.

Data filtering

The recorded raw data was filtered to extract salient features by leveraging the analysis performed in Fig. 5f. The data was filtered using the event-based algorithms described in algorithm 1.

Algorithm 1. Event validation

- E: The list of events to be processed.
- `e.ts`: Timestamp of event e.
- `e.p`: Polarity of event e. Negative and positive polarity are denoted as -1 and 1, respectively.

for each e in E **do**
  if $\exists e' \in E$ such that $|e'.ts - e.ts| \leq 1$ ms and $p.e' = -p.e$ **then**
    $E_{valid} = E_{valid} \cup e, e'$.
  else
    Discard e from E.
  end if
end for
return E_{valid}

Characterization setup

The chip characterization was conducted using an array of specialized instruments. The transfer function of the A1-A2 amplification chain was assessed using an Agilent Analog Discovery 2. An SRS SR780 network signal analyzer was used to evaluate the noise and capture the power spectral density measurements. The necessary waveforms for testing were produced using the Agilent 33120A waveform generator, and their characteristics were monitored using the Agilent DSO6054A oscilloscope. The chip's analog and digital power needs were met using two separate Hewlett Packard E3610A power supplies. As for estimating the chip's total power consumption, initial computations were made using the post-layout extraction feature. These preliminary estimates were validated using real-time readings from the aforementioned power supplies.

Cell culture

Frozen vials of human-derived cardiomyocytes (iCell Cardiomyocytes Kit (Cat. R1057)) were purchased from Fujifilm Cellular Dynamics International (Wisconsin, USA). The cells were thawed and cultured following the manufacturer's guidelines. Before cell plating, the GAIA sensors were sterilized in 70% ethanol for 10 minutes and rinsed thrice with sterile deionized water. The electrode arrays were coated with human fibronectin (Cat. FC010, Signma-Aldrich) at a concentration of 50 mg/mL and incubated at 37 °C for 1 hour. The cells underwent a thawing procedure and had seeding density adjusted[38,50]. 30,000 cells were seeded onto the fibronectin-coated GAIA sensors, and 1.3 mL of iCell Plating Medium was added to each chamber. After 48 hours, iCell Plating Medium was fully replaced with 1.3 mL iCell Maintenance Medium. Half of the medium was exchanged using iCell Maintenance Medium every 2–3 days until the termination of the experiments.

GAIA-DYNAP-SE interface

The integration between GAIA and DYNAP-SE is facilitated through two primary components. Initially, GAIA's incoming data undergoes processing and timestamping via an FPGA, resulting in a catalog of pixel addresses paired with their corresponding event timestamps. Further details on this process can be found in the supplementary material section 4. Following this, the events captured by GAIA are transferred to the DYNAP-SE processor using a specialized API. The chronological integrity of the events is meticulously maintained, owing to the initial timestamping step.

Data availability

Data generated from GAIA supporting the findings of this study are available at: https://doi.org/10.5281/zenodo.11114022.

Code availability

Code that analyzes the data generated from GAIA is available at: https://doi.org/10.5281/zenodo.11114022.

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Author contributions

M.C., G.H., F.Ca., and G.I. conceived the project direction and experiments. M.C., S.N., F.Ca., and H.U. designed the GAIA sensor. M.C. designed the PCBs and the interfacing firmware. M.C. and N.R. developed the FPGA firmware. M.C., F.Ca., and H.U. were involved in the post-processing biocompatibility steps. M.C., C.-V.H.B., F.Ca., and H.U. conducted the cell culture experiments. M.C. analyzed the data. M.C., F.Co., and N.R. developed the on-chip SNN. G.I., A.H., and F.Ca. supervised the project in general. M.C. wrote the manuscript with inputs and revisions from all authors.

Competing interests

The authors declare no competing interests.

Additional information

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