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Gate leakage reduction in AIGaN/GaN HEMTs using *in situ* ion treatment

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#### Abstract

A new *in situ* treatment method is proposed to reduce the gate leakage in normally-on AlGaN/GaN HEMTs. It consists of  $O_2$ -Ar ion bombardment before the gate metalization. Ion treatment is found to improve the quality of gate metal and semiconductor interfaces. This process reduces the gate leakage current by around 25 times. The process is validated for wafer level uniformity and temperature dependency against the traditional NH<sub>4</sub>OH treatment. Ion treated HEMT devices are found to possess two orders of magnitude smaller standard deviations in gate leakage distribution across the wafer. The gate leakage is found to be less dependent on temperature comparatively. The trap energy level of the HEMTs treated using the proposed method is found to be higher than the traditional ones as extracted from Poole-Frenkel electron emission analysis. The new method results in a 0.13 dB improvement in the minimum noise figure of the HEMT on average from DC—16 GHz.

# 1. Introduction

The microwave community prefers designing transmitter, receiver, and transceiver circuits using Gallium Nitride (GaN) technology. GaN high electron mobility transistor (HEMT) emerged as a promising candidate for space, defense, and commercial applications [1–5]. Important attributes associated with GaN HEMTs are superior power density, high efficiency, promising thermal conductivity, enhanced saturated carrier velocity, and high electrical breakdown [6–8]. These benefits have led to rich research and literature on GaN-based power amplifiers. GaN HEMT technology offers low noise amplifiers that are faster, stronger, and more durable than their GaAs counterparts, negating the need for a limiter after the receiver antenna in the front-end assembly [9–12]. Silicon Carbide (SiC) is a preferred choice as a substrate for power performance due to its high thermal conductivity [13, 14].

One of the important factors to influence the device performance is the gate leakage current. Despite the advantages of AlGaN/GaN HEMTs and surpassing other III-V counterparts to achieve the required Johnson figure of merit [15], these devices are limited by gate leakage current [16–23]. The gate leakage also leads to the current collapse phenomenon related to surface state trapping in AlGaN/GaN HEMTs [24]. High gate leakage current results in the degradation of noise performance and breakdown voltage reduction [25].

Low leakage current is essential for applications that require low noise levels. Several methods are developed for leakage current reduction in GaN HEMTs. These methods are mainly related to *in situ/ex-situ* treatment before passivation layer [26], passivation layer schemes [27], treatment before gate metal deposition [28], gate metal stack variation [29], and adding an insulator to have MIS-HEMT structure [30]. The main motivation of these methods is to improve surface passivation at the access region, to improve metal/semiconductor interface



quality, or to put an additional barrier under the gate to minimize the injection of electrons from the gate to twodimensional electron gas (2DEG).

This paper demonstrates the effect of  $O_2$ -Ar ion process treatment before gate metal deposition. It effectively reduces the gate leakage current by 25 times with high wafer level uniformity without degrading the DC and RF performance of the device. The HEMT fabrication process, along with the details of novel treatment before gate metal deposition, is discussed in section II. Section III explains wafer level performance with and without the newly introduced ion treatment step and gate leakage current dynamics. DC and RF performance of the device is summarized in section IV, while a conclusion is provided in section V.

# 2. HEMT fabrication

SiC is the most suitable substrate for the GaN HEMT fabrication because of a better lattice match with GaN and higher thermal conductivity compared to that of Silicon (Si). A heterostructure is formed by an AlGaN layer on top of the channel GaN layer to create the mismatch to utilize piezoelectric polarization, which forms a 2DEG consisting of free electrons with high mobility. The devices investigated in this submission are fabricated using NANOTAM's 0.15  $\mu$ m GaN-on-SiC HEMT technology. An epi-layer containing 20 nm AlGaN and a 3 nm GaN cap layer is grown on a 3-inch GaN-on-SiC wafer with metal organic chemical vapor deposition. The purpose of





the thin GaN cap layer is to eliminate the oxidation of Al in the AlGaN layer, resulting in lower surface defects and higher reliability [31]. The measured 2DEG low field mobility and 2DEG concentration are 1960 cm<sup>2</sup>/Vs and  $1.20 \times 10^{13}$  cm<sup>-2</sup>, respectively. The process flow and simplified device geometry are shown in figure 1(a). The device has a 150 nm gate length (L<sub>g</sub>), a 3  $\mu$ m drain-source distance and a gate in the middle of drain-source contacts. For power amplifiers, gate is put near to source (away from drain) to increase breakdown voltage [32]. For LNAs, this asymmetric gate configuration is not required. The gate-source distance (L<sub>gs</sub>) is 1.425  $\mu$ m. The developed treatment method is compared with well-known NH<sub>4</sub>OH treatment regarding DC and RF performance.

The fabrication steps are ohmic contact formation, mesa isolation, deposition of the first passivation layer, T-gate formation, creation of the first metal layer, deposition of second passivation, and the second metal layer. Ohmic contacts are formed by rapid thermal annealing of Ti/Al/Ni/Au metal stack. The contact resistance and sheet resistance from transfer length method measurements is 0.4  $\Omega$ /mm and 280  $\Omega$ / $\Box$ , respectively. The first Silicon Nitride (SiN) passivation is deposited by plasma-enhanced chemical vapor deposition to passivate the dangling bonds at the semiconductor surface. To have a T-shaped gate contact, the first passivation layer is etched by F-based (CHF<sub>3</sub>, CF<sub>4</sub>, and SF<sub>6</sub>) reactive ion etching with a low power to avoid damage to the GaN surface. The T-shaped gate contact is formed with e-beam lithography (EBL) and e-beam evaporator systems. The first metal layer is created by lift-off technique with 1.1  $\mu$ m Ti/Au metal stack. The second passivation and the second metal layers are formed using the methods employed for their corresponding first layers. If the passivation processes can suppress surface leakage currents, metal-semiconductor junctions dominate gate leakage. Therefore, the treatment before gate metal deposition turns out to be crucial.

We introduce the  $O_2$ -Ar ion process before gate metal deposition as a novel crucial step shown in figure 1(a) with a filled circle. Initially,  $O_2$  ions are sent to the sample's surface to remove organic residues from EBL resist. After that, Ar ions are used to remove the oxidized layer from the surface physically. In that way, carbon contamination and poor quality thin oxidized surfaces are successfully removed. This *in situ* treatment effectively increases the Schottky junction quality. Figure 1(b) shows the SEM image of 4  $\times$  75  $\mu$ m HEMT after





successful fabrication. The band diagram in figure 2(a) is showing the 2DEG formation between AlGaN and GaN buffer. CV curve shown in figure 2(b) explains the existence of 2DEG and also depletion of 2DEG with negative gate bias. From CV characteristics, pinch-off voltage of the ion treated and NH<sub>4</sub>OH treated device are -4.2 V and -3.5 V, respectively. It is to be mentioned that the  $O_2$ -Ar ion treatment is commonly used to remove organic contamination coming from photoresist residue [33–36]. This is the first time, to the best of the authors' knowledge, that  $O_2$ -Ar ion treatment is introduced in the literature before gate metal deposition. It reduces gate leakage current without significant degradation in the device performance and increases the uniformity of the leakage current throughout the wafer.

#### 3. Wafer level performance and gate leakage dynamics

Generally, the leakage current of single HEMTs is studied in the literature, but the leakage current may vary depending on the chip's position within the wafer. Thus, assessing the leakage current distribution across the wafer helps to examine the method's suitability for wafer production. Figure 3 shows the gate leakage current of multiple devices through which the distribution of the leakage currents across the entire wafer is studied.

Table 1 indicates that the ion treatment suppresses the gate leakage current more than one order of magnitude, and it has two orders of magnitude smaller standard deviation. Figure 4 compares the absolute value of the gate leakage between an ion treated and  $NH_4OH$  treated device. In both treatment methods, the gate leakage current is larger than the drain leakage current at the drain voltages between 0 V and 40 V under -8 V gate bias. This shows that the leakage current between drain-source contacts due to high drain bias is much less than that of between reverse bias gate-source Schottky junction.



Table 1. Gate leakage current statistics of 4  $\times$  75  $\mu m$  HEMTs at 25° C.

Method	Vd = 10 V Maximum Minimum Standard			Vd = 25 V Maximum Minimum Standard			
	(A/mm)	(A/mm)	deviation	(A/mm)	(A/mm)	deviation	
NH <sub>4</sub> OH	85e-06	19e-06	22e-6	200e-06	48e-06	47e-6	
Ion	3.3e-06	1.9e-06	0.7e-06	5.3e-06	3.5e-06	0.7e-6	

It can be seen in figure 5 that there is a significant reduction in the gate leakage current above the threshold voltage ( $V_t$ ). The drain and source are grounded to eliminate drain bias dependency of leakage current. To clarify the gate leakage dynamics for these two treatment methods, gate leakage measurements are taken at several temperatures ranging from 25 °C to 150 °C. Figure 6 shows the temperature dependence of the gate leakage current of the NH<sub>4</sub>OH treated device initially increases for the gate bias above  $V_t$ . However, it is observed that elevating the temperature at gate voltage higher than the  $V_t$  results in a slight reduction in the leakage current. In the case of an ion treated device, the minimum leakage current occurs at a gate voltage above  $V_t$ , specifically when the temperature is around 75 °C. This behavior is related to deep acceptor trap initiated impact ionization [20]. The gate leakage current consistently increases with rising temperature for temperatures exceeding 75 °C and gate voltages below  $V_t$ . It is noticeable that leakage in ion treatment is less dependent on temperature as it has lower variation as a function of temperature.







The reverse bias gate current in GaN HEMTs is separated into four distinct elements: thermionic emission, trap-assisted tunneling, Poole-Frenkel (PF) emission, and Fowler-Nordheim tunneling [37]. Since the gate length of the device is as small as 150 nm, there will be a considerable uneven distribution of leakage current









Table 2. 4  $\times$  75  $\mu$ m HEMTs parameters from small signal and noise measurements.

Method	MAG	NF <sub>min</sub>	C <sub>in</sub>	C <sub>out</sub>	R <sub>ds</sub>	f <sub>t</sub>	f <sub>max</sub>
	(dB)	(dB)	(fF)	(fF)	(Ω)	(GHz)	(GHz)
NH <sub>4</sub> OH	13.4	0.66	386	198	496	54.9	63.3
Ion	12.8	0.52	376	198	244	51.8	64.2

density under the gate [38]. Therefore, only PF emission analysis will be provided, and the method used is similar to that in [39]. As a difference in [39], the electric field is obtained from simulations in Silvaco ATLAS TCAD. The relationship between leakage current density ( $J_{leak}$ ) and electric field (E) is given by [39]

$$J_{leak} \approx J_{PF} = CEexp\left[-\frac{q(\phi_t - \sqrt{(qE/\pi\epsilon_s))}}{kT}\right],\tag{1}$$

where C is a constant,  $\phi_t$  is the barrier height for electron emission from the trap state, and  $\epsilon_s$  is the permittivity of the semiconductor at high frequency. After rearranging equation (1)

$$ln(J_{leak}/E) = \frac{q}{kT} \sqrt{\frac{qE}{\pi\epsilon_s}} + c(T),$$
<sup>(2)</sup>

where

$$c(T) = -\frac{q\phi_t}{kT} + \ln(C)$$
(3)

Figure 7 shows the plot of equation (2), valid for gate voltage above the  $V_t$ . The barrier height for electron emission from the trap state is extracted as 0.27 eV and 0.46 eV for NH<sub>4</sub>OH treated and ion treated devices, respectively. Figure 8 shows that the ion treated device has a higher barrier for electron emission.

#### 4. DC and RF characterizations of HEMTs

HEMT periphery and topology both have significance in the design of a monolithic microwave integrated circuit (MMIC) amplifiers. Small periphery devices are suitable for low noise, high gain, and high frequency applications, while large periphery devices are favorable for high power and low frequency applications. Therefore, an optimum periphery is always chosen for particular amplifier design requirements. In this writing, DC and small signal performance of a  $4 \times 75 \ \mu m$  small periphery HEMT is analyzed focussing low noise amplifier design involving NH<sub>4</sub>OH and ion treatment fabrications.

DC measurements of  $4 \times 75 \ \mu m$  HEMT provides technology figures-of-merit. The maximum drain current (I<sub>Dmax</sub>) of 1.11 A/mm at Vgs = 1 V and maximum transconductance (g<sub>m,max</sub>) of 326 mS/mm are found for NH<sub>4</sub>OH process while for ion treatment, these values are 1.14 A/mm and 329 mS/mm. The breakdown voltage

at Ig =1 mA/mm is 40 V, the same for both fabrications. This shows that HEMTs have similar DC performance from both processes.

Small signal measurements of HEMTs from NH<sub>4</sub>OH and ion treatments are performed on Rohde & Schwarz ZVA PNA up to 40 GHz using external bias tees on-wafer. The measurements are performed under bias conditions of 10 V and 150 mA/mm. The 10 V is the external voltage, and 150 mA/mm is 13 % of I<sub>Dmax</sub>. Data for the 4 × 75  $\mu$ m HEMTs are recorded, and HEMT's performance parameters are extracted using PathWave Advanced Design System (ADS) from Keysight Technologies. These parameters include HEMT's input capacitance (C<sub>in</sub>), output capacitance (C<sub>out</sub>), and drain-source resistance (R<sub>ds</sub>). Input reflection coefficient (IRL) of HEMT provides C<sub>in</sub>, output reflection coefficient (ORL) gives C<sub>out</sub> and R<sub>ds</sub>. The other parameters include maximum available gain (MAG), maximum stable gain (MSG), cut-off frequency (f<sub>t</sub>), and maximum oscillation frequency (f<sub>max</sub>).

Figure 9 shows  $C_{in}$  and  $C_{out}$  of the HEMTs from NH<sub>4</sub>OH treatment and ion treatment. Input impedance has capacitive behavior up to 30 GHz and becomes inductive after that. The capacitance values are almost the same, up to 15 GHz for both processes and after that, ion treatment capacitance starts to increase. Figure 10 shows  $R_{ds}$  of the HEMTs from NH<sub>4</sub>OH treatment and ion treatment. NH<sub>4</sub>OH treatment has comparatively higher resistance than ion treatment. Lower  $R_{ds}$  results in the reduction of gain.

The technology figures-of-merit  $f_t$  and  $f_{max}$  of the 4 × 75  $\mu$ m HEMTs are characterized using small signal measurement data by extrapolating the current gain and MAG curves. It can be seen from linear fitting in figures 11 and 12 that  $f_t$  and  $f_{max}$  values for NH<sub>4</sub>OH treatment are 55 GHz and 63 GHz, respectively, while corresponding values for ion treatment are 52 GHz and 64 GHz. Although it appears from figures 11 and 12 that  $f_t$  and  $f_{max}$  values are slightly higher for ion treatment, it is justified to conclude that both treatment have almost same values of  $f_t$  and  $f_{max}$ .

Gate leakage current is in direct relevance with the noise performance of the HEMT [25]. Minimum noise figure (NF<sub>min</sub>) of both NH<sub>4</sub>OH treated and ion treated HEMTs is measured as shown in figure 13. Owing to the lower gate leakage current, the noise performance of the device fabricated using the novel ion treatment method is far better than NH<sub>4</sub>OH treatment. Therefore, it is justified to claim that the devices fabricated using the proposed method are promising for GaN-based low noise amplifiers.

Table 2 summarizes the small signal parameters of HEMTs fabricated using both NH<sub>4</sub>OH and ion treatment techniques. All parameter values are shown at 10 GHz except  $f_t$  and  $f_{max}$ . It is observed that ion treatment results in a decrease of MAG,  $C_{in}$ ,  $R_{ds}$  and  $f_t$ .  $f_{max}$  and NF min are improved.  $C_{out}$  is almost unchanged. The change in  $C_{in}$  value will only shift the optimum source impedance ( $\Gamma_{Sopt}$ ) without affecting HEMT's NF min value. Similarly, the change in  $C_{out}$  and  $R_{ds}$  values will result in the shift of optimum load impedance ( $\Gamma_{Lopt}$ ) without affecting its maximum output power.

#### 5. Conclusion

This paper discusses a novel approach to suppress gate leakage in AlGaN/GaN HEMTs. To the best of the authors' knowledge, ion treatment is applied before the gate metal deposition for the first time. DC and RF performance of the HEMTs with traditional NH<sub>4</sub>OH treatment and proposed  $O_2$ -Ar ion treatment is observed, and there is no significant degradation. There is a shift in input and output capacitances of the HEMT with the ion treatment method, which only shifts optimum source and load impedances without affecting optimum noise and output power performance. However, gate leakage is reduced significantly. The noise performance of GaN HEMT is highly dependent on the gate leakage. Therefore, the proposed approach benefits GaN HEMTs for low noise applications.

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#### Data availability statement

The data cannot be made publicly available upon publication because they are not available in a format that is sufficiently accessible or reusable by other researchers. The data that support the findings of this study are available upon reasonable request from the authors.

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