Magnet Free Inductive Wireless Power and Data Transmission System for Fully Implantable Cochlear Implants

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ABSTRACT

In this work, a wireless power and data transmission system (WPDT) for fully implantable cochlear implants that operates with a broad range of input power is implemented. In this inductive link, power conversion efficiency is maximized by switching the operation modes of the multi-mode rectifier according to the power sourcing capability under varying coupling conditions. These operation modes are named as half wave mode (HWM) and voltage mode (VM). While the input power of the transmitter is generated with a Class-E power amplifier, data transmission is conducted with differential binary phase shift keying. A large gain common gate amplifier is utilized to compensate variable input signal level. Data and carrier recovery is realized by an asymmetric charge-discharge structure with threshold detection. This novel WPDT circuit is implemented and fabricated in TSMC 180 nm BCD Technology with an active area of 1.2 mm^2. Average charging power values of the system for a 3.3 V load are measured as 42.96 mW, 38.90 mW, and 60.10 mW for only HWM, only VM, and mixed mode rectification for a transmitted power range of 10 – 140 mW. Meanwhile, BPSK demodulator consumes only 22.8 – 24.1 µW power and has a bit error rate (BER) range of 3.0×10^{-3} – 2.8×10^{-6} depending on receiver coil voltage level (50 – 300 mV).

CCS CONCEPTS

•Hardware~Very large scale integration design~Application-specific VLSI designs~Application specific integrated circuits •Hardware~Very large scale integration design~Analog and mixed-signal circuits~Analog and mixed-signal circuit optimization **•Hardware~Communication hardware, interfaces and storage~Wireless devices**

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KEYWORDS

Wireless power and data transmission, inductive coupling, multi-mode rectification, binary phase shift keying, non-coherent detection, medical implant, fully implantable cochlear implant

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1 Introduction

Cochlear implants (CIs), restoring hearing in patients with sensorineural hearing loss, are considered to be the most successful neural prosthesis, with more than one million devices implanted worldwide by 2022 [1]. Yet, there is still room for improvement considering the adoption rates of conventional CIs since there are more than 60 million individuals with severe to complete hearing loss [2]. Generally, reasons behind low CI adoption rate come down to the bulky structure of conventional CIs: environmental damage risks on external part, frequently replaced/recharged batteries, and last but not least aesthetics. Recently, to address these drawbacks, CIs with no external parts are being developed [3], [4].

Conventional CIs utilize wireless RF link to transfer externally attained and processed sound signal, in addition to power which is crucial for the electrical stimulation of the cochlea. For this mandatory and continuous RF transmission, spatial alignment of the coil pair is essential to maintain efficient transmission. Thus, a permanent magnet is placed between the inductive transmitter coil (TX) and receiver coil (RX) to satisfy proper alignment. Even though there are number of CIs currently compatible with MRI up to 3T, magnets potentially inflict harm to surrounding tissue [5], and cause some safety issues regarding magnetic resonance imaging (MRI) [6].

For a CI with no external parts, roles and design considerations of RF transmission change. In these systems, power required for stimulation is supplied through implanted batteries. These batteries are required to be recharged periodically. Therefore, efficient power transmission (WPT) plays a crucial role in the

implanted device. In addition, even though the implant operates autonomously, not being able to directly connect to a fully implanted CI's sound processor, stimulator, and control unit brings up the necessity of wireless data transmission (WDT). MRI safety concerns in such an implant implies a magnet free design as well. This approach calls for a design perspective which allows wireless power and data transmission (WPDT) in cases where inductive coupling between TX and RX coils varies. There are studies to cover a range of coupling coefficients [7], [8], but medical applications require the operation frequency to be 13.56 MHz according to Industrial Scientific and Medical (ISM) band regulations [9]. For a fully implantable CI implantation procedure, implantation area is also a concern and limits maximum coil size. Triple mode rectifier circuit [10], with an optimized coil size and 13.56 MHz carrier frequency, covers voltage coupling coefficient levels from 0.10 to >0.40 without a dead zone.

For data transmission on the other hand, there are three main methods being used to modulate data symbols. The first two methods, namely, amplitude shift keying (ASK) and frequency shift keying (FSK), manipulate the changes in the amplitude and frequency of a carrier signal, respectively, according to the data symbol. Requirement of a second carrier frequency in FSK means that available bandwidth must be larger. In ASK, complex demodulation circuits may be needed when the noise levels become comparable with the signal level and when signal levels change abruptly both of which are natural outcomes of varying coupling conditions. The third method which is used in this study utilizes phase shift keying (PSK) in which the amplitude and the frequency remains constant whilst the phase changes. The constant frequency provides better coupling of the coils [11] whereas the constant amplitude provides high efficiency during power transfer [12]. The PSK scheme also benefits from its low sensitivity to amplitude changes caused by noise and input power change. It also allows transmission rates at the carrier frequency when the transfer link can support it, meaning that the available bandwidth can be used more efficiently [13].

In this work, a WPDT system without an alignment magnet is presented. The power rectification method is selected autonomously by monitoring the output of a triple mode rectifier circuit. The encoded data is demodulated with a digital non-coherent design utilizing binary phase shift keying (BPSK). A compact design is achieved by multiplexing WPT and WDT on a single transmitter and receiver coil pair. The presented system enables additional opportunities not only for CIs but also for future fully implanted medical device studies.

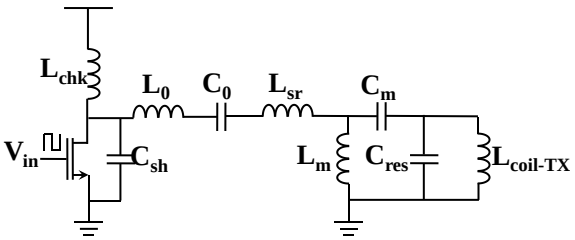


Figure 1: Class-E power amplifier structure with transmitter coil and matching network

2 Power Amplifier and Rectifier Type Selection

In wireless charging, transferred power must be least degraded at the receiver to be able to supply sufficient power to the rectifier and battery. As carrier frequency for power transmission is 13.56 MHz, receiver impedance should be matched to acquire maximum power at this frequency, suggesting an LC resonation [10]. In this study, a similar approach is adopted to transfer input power from the transmitter to receiver side. For the input power generation in the transmitter side, Class-D amplifiers are commonly used. However, Class-D amplifiers struggle with transistor mismatch [14], needing complex gate drivers and having significant harmonic power dissipation [15]. Hence, a single transistor Class-E power amplifier structure is preferred to minimize non-fundamental frequencies at the transmitter. For the Class-E amplifier circuit shown in Figure 1, inductance and capacitance values shown in Table 1 are selected. L0 and C0 are in resonance at the fundamental frequency. For an imaginary resistive load, aimed power and DC level is calculated. This DC value is then used to decide on Csh and Lsr values. Since load is not resistive for the inductive transmission case, a matching network is added to the output of the amplifier. Switching is performed with VN2010L NMOS transistor, as it has low input (35 pF) and output (9 pF) capacitances, allowing high frequency operations and low on-state resistance (10 Ω), minimizing losses due to switching.

Suggested WPT system employs a triple mode rectifier system, namely current mode (CM- Figure 2(a)), half-wave mode (HWM- Figure 2(b)), and voltage mode (VM- Figure 2(c)). CM is designed to cover low coupling ranges when rectifier output level (LOAD signal) is larger than rectifier input. VM on the other

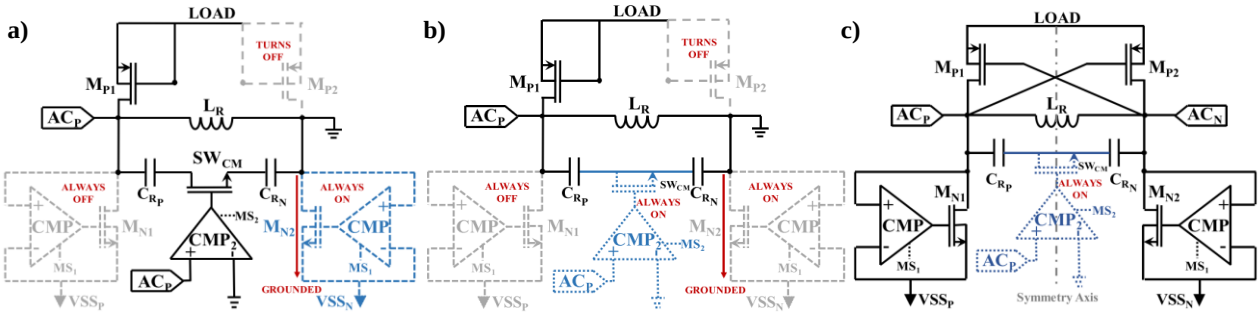


Figure 2: Multi-Mode Rectifier (a) Current Mode (b) Half-Wave Mode (c) Voltage Mode configurations

Table 1: Class-E power amplifier components, component values and descriptions

Component	Value	Description
L_{chk}	2.2 µH	Blocks AC leakage
C_{sh}	6.8 pF	Adjusts output DC level
L_0	4.7 µH	Resonance inductance
C_0	68 pF	Resonance capacitance
L_{sr}	1 µH	Adjusts output DC level
L_m	100 µH	Matching inductance
C_m	220 pF	Matching capacitance
C_{res}	153 pF	Coil matching capacitance
L_{coil}	1.1 µH	Transmitter coil

hand, operates in larger coupling ranges, where LOAD signal is lower than rectifier input, letting utilization of this voltage difference for current flow into battery. HWM, covering the intersection and dead zone of CM and VM, is designed to allow more efficient charging from the upper band of CM range and lower band of VM range. Switching between different modes is performed with a 2-bit control, allowing external control in addition to autonomous switching according to rectifier input level. Changing rectifier mode of operation according to input level, if transmitter power is fixed, corresponds to changing mode with respect to the coupling level between TX and RX. To cover an extended use case in which transmitted power also changes, an additional decision mechanism is designed.

When battery is connected to the rectifier, if proper mode is not selected (e.g., VM is not efficient when coupling is weak), rectifier draws current from the battery. This means that power induced on the RX coil is not sufficient to operate the rectifier with the selected mode (VM in the previous example). Therefore, to select the mode of operation in a case where transmitted power level is not well known, a search algorithm is implemented. Even though rectification efficiency of CM is less than HWM and VM under strong coupling conditions, starting the rectifier with CM operation is advantageous. Rectifier can source current to the battery for a large range of coupling conditions using this mode (>0.10). When coupling conditions are improved (coils are better aligned axially, or positioned with a smaller distance), at some point, it is more efficient to utilize HWM and eventually VM. Trigger points between the modes are decided by measuring LOAD voltage value and finding the points where rectifier switches can operate properly without the need of additional power from the battery. For 2-bit control signals, 4 transition points are decided. For the case where coupling conditions become better, a margin should be left so that at the lower parts of a mode range, no glitches are observed at control signals. On the other hand, when coupling conditions worsen, previously active mode should work as long as possible to improve average

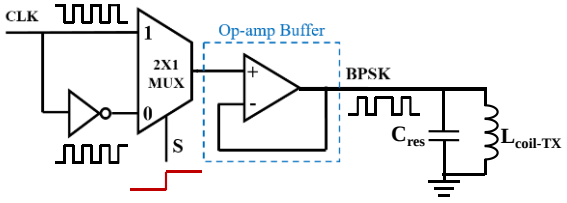


Figure 3: Multiplexing BPSK modulator

rectification efficiency. Following this, for the case where coupling conditions worsen, VM-HWM transition should be at 1.75V, and HWM-CM shift should be at 0.9V LOAD voltages. For improved coupling conditions, transitions should be with a margin around 0.2V from the reverse transition, corresponding to a load voltage of 1.1V for CM-HWM and 2V for HWM-VM transitions. These transitions are implemented with a digital hysteresis comparator. LOAD voltage is digitized with a 12-bit SAR-ADC and mode bits are selected according to LOAD voltage and direction of coupling change via hysteresis structure.

3 Data Transmission

Differential PSK (DPSK) encoded data signal consists of two phases with 180° difference, each phase corresponding to one of the symbols. In the suggested transmission system, symbols represent single bits meaning that symbols are the bit values themselves, 0 or 1. For data modulation, digital multiplexing is implemented (Figure 3). Carrier clock signal is switched with its inverse in accordance to the symbol value. Then, output is fed into a source follower to isolate digital output and load, namely TX coil. Digitally modulated waveform consists of harmonics of the carrier frequency, which is not an ideal case for transmission, as different harmonics are exposed to different amounts of time delay and attenuation. To limit this, TX coil is matched to resonate at the carrier frequency. This filters out the harmonics in the transmitted signal.

For demodulation, the main difference between coherent and non-coherent detection is the clock/carrier recovery approach. Coherent detection requires extraction of the original carrier waveform without phase delays, implying that delays due to circuitry and transmission should be compensated. Such a design requires locked loop logic, significantly increasing power consumption. On the other hand, as a special case of BPSK, DPSK allows non-coherent demodulation. In WDT system, digital and non-coherent detection is implemented. The received signal at RX coil has varying amplitudes for different coupling levels due to the magnet free design and the demodulator operates with digital signals to reduce power consumption. Considering these

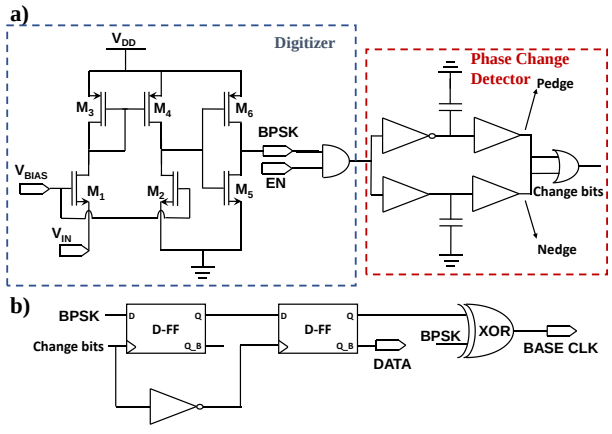
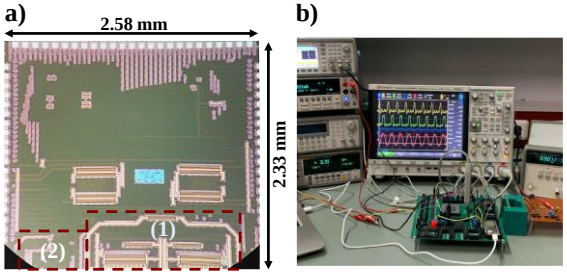


Figure 4: Demodulator schematics (a) Digitizer and Phase Change Detector (b) Data and Clock Recovery Unit

Table 2: Fundamental peak and 2nd—3rd harmonic suppression values

DC Supply Voltage (V)	Fundamental Peak (dBm)	Suppression (dB)	
		2nd Harmonic	3rd Harmonic
5	6.98	21.77	26.16
6	12.56	21.76	26.17
7	15.70	22.32	26.75
8	17.68	22.36	27.00
9	19.21	22.33	27.16
10	20.43	22.96	27.35
11	21.28	22.80	26.42
12	21.94	22.91	27.22
13	22.41	22.85	26.88
14	22.71	22.70	26.49
15	23.01	23.20	26.78
16	23.24	22.60	27.19

factors, received signal should be amplified to the same level for different input levels and be digitized. For amplification, a common gate (CG) amplifier is utilized to have an improved amplifier bandwidth to minimize errors due to amplification. Output DC voltage level of the amplifier is set to 0.9 V, half of the digital voltage supply (1.8 V) to be able to digitize the input linearly. Two cascaded CMOS inverters are added as output stage to digitize the amplifier output. Digitizer can be seen in Figure 4(a). Similar to CG stage, inverter thresholds are adjusted to be VDD/2. If data symbol duration is selected to be an integer multiple of the carrier period, symbol changing points correspond to 0.9 V amplitude points in the BPSK waveform. Therefore, in the digitized waveform, symbol change point voltage is either 1.8 V or 0 V for twice the half period of the carrier period. Symbol change detection exploits this outcome. Two unbalanced large CMOS inverters are fed by digitized buffered BPSK and its inverse. Discharge currents of the inverters are adjusted to be more than twice of the charging currents. Throughout a single symbol duration, outputs of the inverters swing between 0.9 V and 0V. When the symbol changes, for a duration of half of the carrier period, capacitance of the inverter charges up to a voltage value greater than 0.9 V. Discharge current being greater than two times of the charging current ensures this capacitance is discharged to 0 V before next charging-discharging cycle. Then, by threshold detection, symbol change point is detected. As this is done for the BPSK signal and its inverse, symbol transitions for both 0 to 1 and 1 to 0 are recovered. This symbol change information is used as a clock signal to read the BPSK signal with a master-slave configuration (Figure 4(b)). This master-slave configuration allows detection at either one of the edges, therefore compensates



1- Rectifier: 1.56 x 0.59 mm²
2- Demodulator: 0.69 x 0,46 mm²

Figure 5: (a) Chip micrograph and floorplan (b) test setup

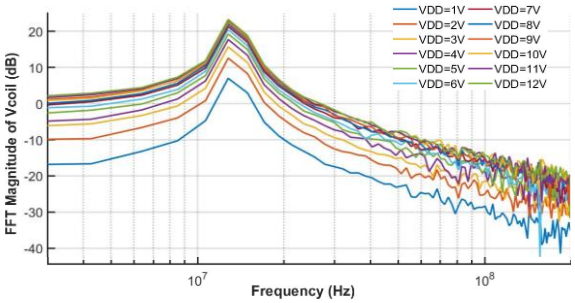


Figure 6: Power amplifier output with changing supply voltage

the delays caused by the circuitry after digitization of the incoming modulated waveform. To recover the clock, digitized BPSK signal has to be inverted each time the symbol changes and stay as such until next change, corresponding to 180° phase shift in digital domain. This is implemented by using an exclusive-OR (XOR) gate, the inputs of which are the digitized BPSK and recovered data signals.

4 Experimental Results

WPDT circuit is implemented in TSMC 180 nm BCD technology. Power amplifier and external modulator are implemented with discrete blocks. Chip micrograph and floor plan of the design alongside the test setup is shown in Figure 5. WPDT active area covers 1.2 mm^2. For transmission, a custom designed coil pair is used. External DC supply is used for amplifier biasing, supplying demodulator and ESD protection diodes. Digital control signals are powered with an external battery to reduce noise by isolating analog and digital supplies. A test PCB is designed and fabricated for convenient manipulation of control signals and for monitoring signals with minimal loading. To further reduce loading effects during tests, N2752A InfiniiMode Active Differential Probe is used while monitoring analog signals.

4.1 Rectifier Mode Selection

Changing coupling between the coil by physical means during tests is not feasible due its discontinuous nature. Therefore, an electrical setup that corresponds to physical coupling change is designed for the tests. Coupling change effectively resembles power delivered at RX coil. Same effect can be created with the change in transmitter power while keeping coil positions as the same. However, for this approach to correctly model coupling change, PA output signal composition. i.e., harmonic distribution should not depend on power level. To show this, power amplifier supply voltage is swept from 1 to 12 V and FFT of the output waveforms are plotted (Figure 6). FFT magnitudes at fundamental, second harmonic and third harmonic frequencies and suppressions are investigated by changing the DC supply voltage of the PA, and the results are listed in Table 2. On average, transmitted fundamental frequency power i.e., power consumed by TX coil (Z=80 Ω), is 71.04 mW. Second and third harmonics are suppressed with standard deviations of 0.43dB and 0.39dB, respectively. Therefore, the slope-wise similarity of the FFT characteristics can be underlined which means that changing

received power can be utilized for testing the system under changing coupling conditions.

For changing received power levels/coupling conditions, current that can be supplied to battery are investigated for HWM and VM separately. This done by creating a low resistance path to a 3.3 V node and measuring current flowing out of rectifier output. Maximum current for each mode and corresponding rectifier output voltages with respect to changing PA DC voltages are illustrated in Figure 7(a). After a point between 11 and 12 V, corresponding to 17.05 mA sourcing current, VM can supply more current to battery than HWM with same input power level. This point corresponds to 1.75 V LOAD voltage and is the optimal transition point from HWM to VM. Assuming a uniform probability for the input power level and single mode operation for this range, average source currents are calculated as 13.02 mA and 11.90 mA for HWM and VM respectively. With this transition point, and safety margin added hysteresis structure, the search algorithm is tested for cases where coupling conditions are improved and worsened. LOAD node voltages corresponding to same points are also shown in Figure 7(b). When multi-mode operation is applied, average source currents are calculated to be 18.25 mA and 18.18 mA for monotonously improved and worsened coupling conditions respectively (~ 60.10 mW – maximum power conversion efficiency (PCE) = 84.6 %). In addition to switching between HWM and VM, CM is used for starting up the system up until the point where HWM can operate.

4.2 Data Transmission

To test modulation and demodulation operations, besides the initial input stage amplification and digitization tests, repetitive 1001 data sequence is used. Clock frequency to interpret the data sequence is selected to be one sixteenth of the carrier frequency. This means that 16 period cycles of carrier signal correspond to one symbol (Figure 8(a)). Modulated carrier signal is generated with Cypress PSoC 4 CY8CKIT-042-BLE-A [16] and the same custom coils used in wireless power transmission tests are used for inductive link. For the initial input stage tests, carrier signal is modulated with a square pulse with 50% duty cycle and CG input voltage level i.e., coupling condition is swept with 6 linearly separated points having amplitudes in 50-300 mV range. Then, duty cycles of the digitizer are measured for each case. Duty cycles of the output waveforms ranges in between 47.20% and

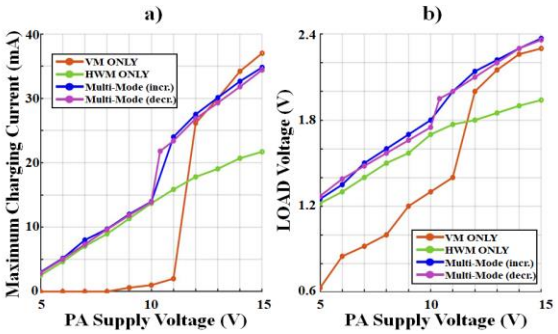


Figure 7: (a) Maximum charging currents (b) corresponding LOAD voltages for VM, CM and Mixed-Mode operations

Table 3: Comparison with the state-of-the-art circuits

Reference	[18]	[19]	[20]	[21]	This Work
Process	180nm BCD	350nm CMOS	350nm CMOS	65nm CMOS	180nm BCD
Coil Number	2	2	4	2	2
PCE	70%	N/A	>50%	75.4%	84.6%
Transmitter	Class-E	Class-E	Class-D	N/A	Class-E
Carrier (MHz)	13.56 MHz	256 kHz	13.56 MHz	13.56 MHz	13.56 MHz
Modulation	BPSK	PSK	PDM	ASK	BPSK
BER	$>10^{-6}$	N/A	4.3×10^{-7}	1×10^{-3}	2.8×10^{-6}
Rx Power (pJ/bit)	183	151	120	880	54.2

50.10% with 49.02% mean and 1.07% standard deviation. Below 40 mV, variation in duty cycle becomes greater than 6.67%, significantly increasing error rates for 16 cycle detection. Minimum mean-square phase jitter at the output is measured as 0.58° and maximum phase jitter is 1.11°. Input stage current consumption is measured to be varying between 4.7 µA and 3.4 µA, for 50-300 mV input voltage.

Output voltages of the large output capacitance CMOS inverters are demonstrated on Figure 8(b) and (c). As expected, it is observed that besides the region where symbol changes, inverter output voltages are less than 0.9V. When symbol changes and BPSK signal is high for a longer time, inverter outputs become larger than 0.9 V, threshold voltage of the next inverter stage, generating a spike. Combined spikes for 0 to 1 and 1 to 0 can be seen on Figure 8(d), as well. It is important to note that rising edges of these spikes correspond to where BPSK signal remains 0 V during 0 to 1 transition, and 1.8 V during 1 to 0 transition. As a result, these spikes can be used as clock signals for data recovery. Output of the D Flip-Flop (D-FF) that recover data by evaluating digitized BPSK signal at combined change spikes and recovered carrier at the XOR gate output are also illustrated in Figure 8(e) and (f), respectively. Overall, maximum power consumption of the demodulator is measured to be 24.1 µW. Considering 16 cycle symbol duration and 1.8 V supply voltage, Rx power is calculated to be 54.2 pJ/bit.

WDT system is tested for the duration of a typical application e.g., fitting duration with the same data sequence. Received data is recorded with a logic analyzer (Saleae Logic 8, 8 channels + 100 MS/s [17]. For changing coupling conditions (RX coil voltage levels), Bit Error Rates (BER) are calculated. Errors are caused by cases where phase jitters are added up in a way that symbol changes in the digitized waveforms do not generate a spike. For the RX coil voltage range of interest (50-300 mV i.e., 0.03-0.17 voltage coupling at 1.8 V TX), maximum BER is calculated to be 3.0×10^{-3}. BER is the lowest when RX coil voltage is 300 mV with 2.8×10^{-6}. Table 3 summarizes comparison of the presented WPDT and state of the art. Proposed system has the highest PCE and lowest Rx power consumption per bit while utilizing 2 coils.

5 Conclusion

In this paper, a magnet free wireless power and data transmission system for fully implantable cochlear implants is presented. Multi-mode rectifier is optimized to select the operation mode

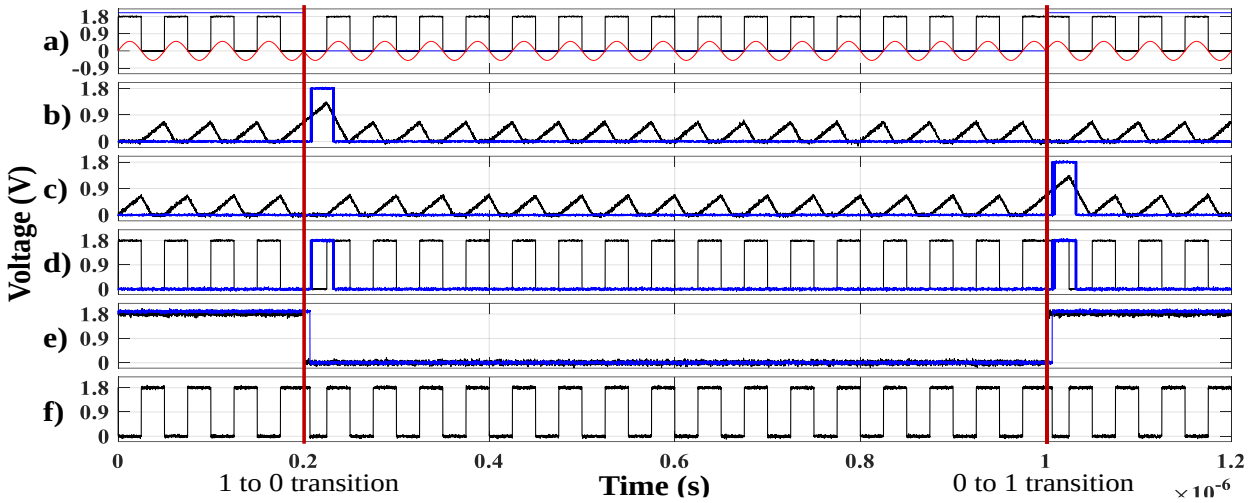


Figure 8: Demodulator node voltages during operation. (a) transmitted data sequence (blue), ideal analog BPSK waveform (red), digitized BPSK waveform (black). (b) phase change point detection (blue), detection inverter input voltage (black) for inverse digital BPSK. (c) phase change point detection (blue), detection inverter input voltage (black) for digital BPSK. (d) combined phase change points i.e., clock signal for data recovery (blue) and digital BPSK (black). (e) recovered data i.e., D-FF output (f) recovered clock i.e., XOR gate output.

supplying the maximum amount of power to the load at constant voltage, ensured with an external voltage supply. This inductive link power is generated with a Class-E power amplifier and transferred through inductive coil pair. For data transmission, digitally modulated differential BPSK is utilized. Designed demodulator circuit amplifies and shifts variable RX coil voltages to a DC level of 0.9 V and digitizes them for data and clock recovery. Phase change points are sensed by threshold detection on capacitors which are charged and discharged by digitized BPSK signal and its inverse. After the detection of phase change points, these points are exploited as clock signals for the D-FF which reads digitized BPSK signal at rising edges to recover transmitted data. Thereafter, recovered data and digitized BPSK signals are fed to an XOR gate. XOR gate inverted digitized BPSK when data changes. Consequently, carrier is recovered. Demodulator circuit consumes 24.1 µW power, corresponding to 54.2 pJ/bit, of which 8.5 µW is consumed by the digitizer. This novel WPDT circuit is tested under varying coupling conditions by changing transmitted power level. According to these tests, during power transmission 84.6 % for averaged maximum PCE is achieved with mixed-mode switching and a maximum BER of 3.0 $\times 10^{-3}$ is calculated under very weak coupling conditions.

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