DESIGN OF A FRONT-END ELECTRONICS AND USER INTERFACE BOARD FOR A COMPACT THERMAL IMAGER

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ABSTRACT

DESIGN OF A FRONT-END ELECTRONICS AND USER INTERFACE BOARD FOR A COMPACT THERMAL IMAGER

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Infrared imaging systems have found increasing usage in various military and industrial branches. The analog front-end unit of an imager plays a considerable role in determining the system performance. In this thesis, a 4-input, 20 MHz mixed-signal front-end electronics board has been designed, implemented and tested by taking all necessary design techniques into consideration to make a system limited by the detector performance. The board functions including the analog processing of the detector output, readout integrated circuit (ROIC) interfacing, analog to digital conversion and user interface are controlled by a field programmable gate array. The board is controllable by a PC through an RS232 port.

After the implementation and testing, the front end electronics board is integrated with a video processing board and a detector/dewar assembly to form a prototype thermal imager. The system is configured to support 128x128 focal plane arrays. The maximum frame rate is 550 Hz for 128x128 focal plane arrays. The

system supports focal plane arrays up to a maximum format of 320x256 at 25 Hz frame rate.

Under the worst conditions, the noise level of the board is less than 650 e^-, and is comparable with that of a typical read-out integrated circuit (550 e^-) being several times smaller than the noise level of a typical cooled longwavelength infrared detector, which is about 4000 e^-. Under typical operating conditions, the noise level of the front-end electronics board is less than 50 e^-, and the performance of the system is limited by the ROIC and detector noise.

Keywords: Infrared Imaging, Focal Plane Array, Front-End Electronics

ÖZ

KOMPAKT TERMAL GÖRÜNTÜLEME SİSTEMİ İÇİN DEDEKTÖR ÖN ELEKTRONİĞİ VE KULLANICI ARAYÜZ KARTI TASARIMI

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Termal görüntüleme sistemleri, çeşitli askeri ve endüstriyel dallarda giderek artan bir şekilde kullanım alanları bulmuştur. Bu sistemlerde kullanılan analog önarabirimler sistem performansını belirlemede önemli bir rol oynamaktadır. Bu tezde, dedektör performansıyla sınırlı bir sistem oluşturabilmek için gerekli tüm tasarım teknikleri dikkate alınarak 4 girişli 20 MHz'te çalışabilen karışık sinyalli bir ön elektronik kartı tasarımlanmış, üretilmiş ve test edilmiştir. Dedektör çıkışının analog işlenmesi, okuma devresi arayüzü, analog-sayısal çevirim ve kullanıcı arayüzünü içeren kart fonksiyonları alan programlanabilir kapı dizinleri entegre devresi tarafından gerçekleştirilmektedir. Kart, RS232 portu üzerinden PC tarafından kontrol edilebilmektedir.

Geliştirme ve test aşamalarından sonra, ön elektronik kartı video işleme ve dedektör/soğutucu birimi ile entegre edilerek prototip bir termal görüntüleme sistemi oluşturulmuştur. Sistem, 128x128 dizinli odak düzlem dedektörler ile uyumlu olacak şekilde yapılandırılmıştır. Maksimum resim hızı 128x128 dizinli odak düzlem

dedektörler için 550 Hz'dir. Sistem, 25 resim/saniye hızda 320x256 formatına kadar odak düzlem matrislerini desteklemektedir.

En kötü koşullarda, kartın gürültü seviyesi 650 e^-'dan küçüktür ve tipik bir okuma devresi çıkış gürültü seviyesi (550 e^-) ile karşılaştırılabilir düzeyde olup, 4000 e^- olan tipik soğutmalı uzundalga kızılötesi dedektör gürültü seviyesinden bir kaç kat düşük düzeydedir. Normal çalışma koşullarında, ön-elektronik sistemi gürültü seviyesi 50 e^-'dan küçüktür ve sistem performansı okuma devresi ve dedektör gürültüleri ile sınırlıdır.

Anahtar Kelimeler: Termal Görüntüleme, Odak Düzlem Dedektör Dizini, Dedektör Ön-Arabirim Elektroniği

To My Family

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INTRODUCTION

1.1 Overview

Infrared imaging provides the means to convert the infrared energy, which is emitted from the objects and invisible to human eye, to electrical signals that may be then processed to obtain thermal images. Different from the cameras used in visible light, it is possible to get high contrast and detailed images using infrared cameras in day, night and bad weather conditions due to the nature of infrared energy.

A basic infrared imaging system consists of many subsystems, each of which processes information differently. They may create artifacts or variations in the processed image that were not present in the original scene. Figure 1.1 illustrates five major subsystems: optics for focusing the radiation onto the detectors, IR detectors together with the readout integrated circuit (ROIC) for converting scene radiation into a measurable electrical signal, front-end electronics unit for digitizing detector output and producing necessary bias voltages with control signals for the detector, image processing unit for image enhancement, and the output stage for either displaying or storing.

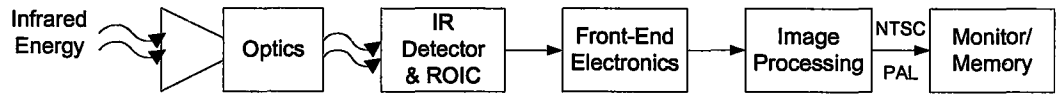


Figure 1.1: Block diagram of a basic infrared imaging system.

This thesis reports the development of a multi-functional front-end electronics system for staring focal plane arrays (FPAs). Main tasks of this system include detector bias voltage and control signal generation, analog processing and digitization of detector output, and nonuniformity correction coefficient calculation. The performance of the front-end electronics has significant effect on the overall system performance, and inadequate quality of this block results in poor thermal images. Careful design and component selection insures a system with focal plane array limited performance [1].

1.2 Aims

This thesis work focuses on the design and implementation of a front-end electronics system for a prototype thermal imaging system. The signals to the front-end electronics system come from a 128x128 InSb focal plane array coupled to an ROIC. The front-end electronics is designed to be compatible with the Indigo Systems' 980X series ROICs. The front-end electronics board is integrated with a video processing and system control board [2] for real time thermal imaging. This board generates timing signals for the detector, performs all image processing, and generates video signals for monitoring the real time thermal video. The video processing and system control board (VP_SC) has been implemented through another M. Sc. Thesis [2]. The VP_SC uses the nonuniformity correction coefficients calculated by the front-end electronics board to normalize the ROIC output. This board also converts the processed digital data to analog, and sends it to the monitor for display. A PC is used to control ROIC settings, to apply gain and offset for ROIC output, and monitor FPA temperature output.

Main functions of the front-end electronics board include low-noise detector bias, reference and control signal generation, buffering, offset and gain control, clamping, differential driving, 12-bit digitization, FPA digital temperature measurement, PC communication, and normalization coefficient calculation. Figure 1.2 illustrates the blocks of the front-end electronics board and interface of the board

with the other units. Figure 1.3 shows a picture of the front-end electronics system board designed and implemented in this work.

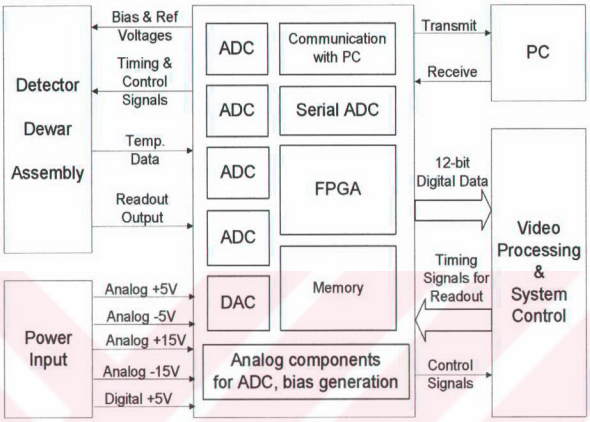


Figure 1.2: Blocks and interface of the front-end electronics board.

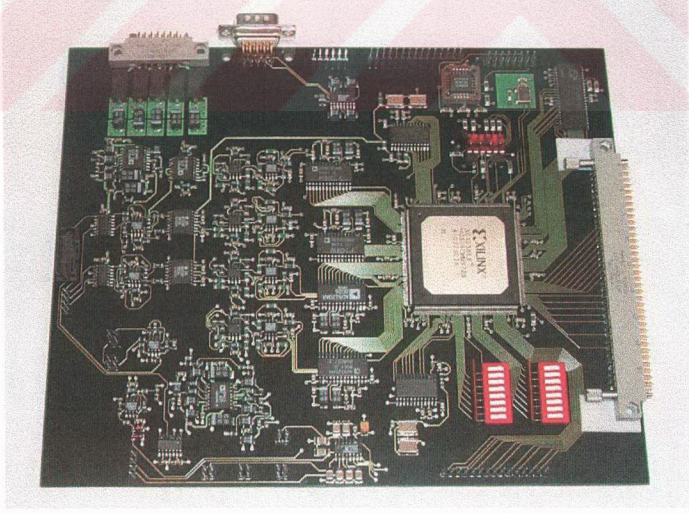


Figure1.3: Front-end electronics board.

The front-end electronics system was tested prior to integration with image processing board to ensure proper operation of board, and required flow of detector output through each integrated circuit on the board was checked. After the board was completely tested, it was integrated with the video processing and system control board to perform real time thermal imaging.

1.3 Organization of the Thesis

This thesis is composed of seven chapters. Chapter 2 provides an overview of the status of the infrared imaging technology.

Chapter 3 describes the readout integrated circuit (ROIC) by Indigo Systems which was used with the 128x128 FPA to test the prototype thermal imaging system.

Chapter 4 contains detailed information on the front-end electronics system, including the functions implemented and the hardware design. This chapter also describes the normalization coefficient calculation algorithms applied to correct non-uniformities of the FPA. Chapter 5 presents the simulation and testing of the board.

Chapter 6 focuses on the integration of the front-end electronics system with the video processing and system control board, and testing the system. Finally, Chapter 7 gives the conclusion and future work.

CHAPTER 2

INFRARED IMAGING SYSTEMS

2.1 Introduction

"Infra" is a prefix from the Latin meaning "below" or "beneath." Hence, infrared refers to the region beneath the red [3], lying between visible light and microwave portions of the electromagnetic spectrum. That region of the spectrum is also called as the heat region of the spectrum since objects radiate energy in the infrared region when they are heated. All objects, even the ones below 273K such as ice, radiate some energy in the infrared region.

Infrared radiation (IR) is a form of electromagnetic radiation, and it mainly differs from the other forms of electromagnetic radiation such as visible light, radio waves, and x-rays in its wavelength. Infrared region spans the 0.7 - 1000 μm region of the electromagnetic spectrum. Figure 2.1 shows a portion of the electromagnetic spectrum. Detection systems can not use the whole IR emission spectrum due to the absorption of the radiation by water or carbon dioxide in the atmosphere. However, a number of wavelength bands have good transmission, which are given below.

- The long wavelength IR (LWIR) band extends from 8 μm to 14 μm, and 100 % transmission can be realized on the 9 – 12 μm band. Most of the terrestrial objects have perfect visibility in the LWIR band.
- The medium wavelength IR (MWIR or MIR) band is in the 3.3 – 5.0 μm portion of the spectrum, and provides 100 % transmission. The ambient background

noise is lower than that of the LWIR.

- Visible and short wavelength IR (SWIR or near IR, NIR) in the 0.35 – 2.5 μm region has a high atmospheric transmission and peak solar transmission, so that the IR detectors provide better clarity and resolution than LWIR or MWIR. However, objects at 300K can not be visualized without ambient or artificially introduced illumination in SWIR.

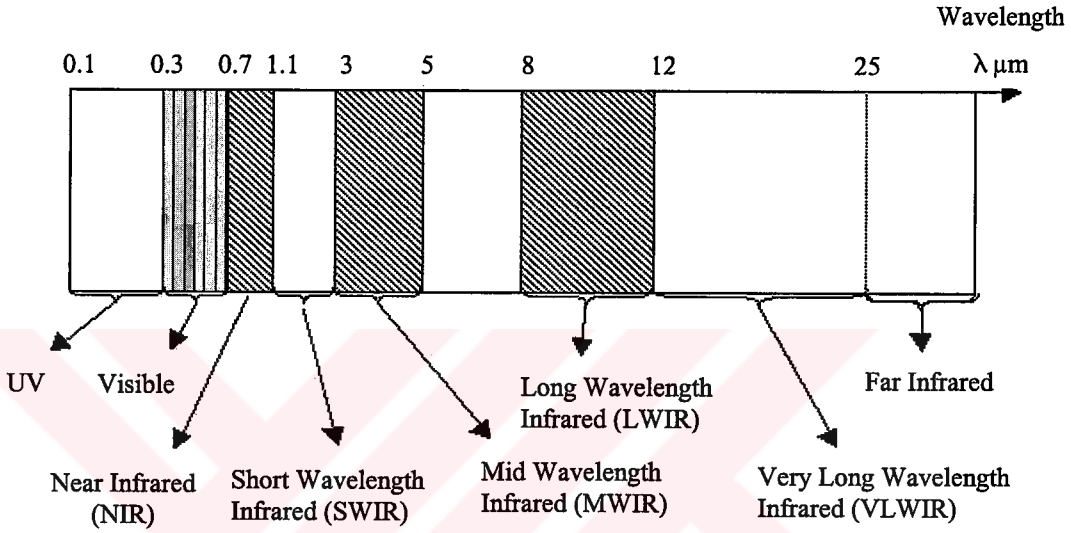


Figure 2.1 Electromagnetic Spectrum.

2.2 General Classification of IR Detectors

An infrared detector is used to convert the radiant energy in the infrared into a measurable form [3]. Infrared detectors have a wide range of applications in the military, scientific, industrial, medical, security, and automotive areas. They provide the ability of seeing the objects in the dark or in the obscured visibility by detecting the infrared energy emitted by objects different from the visible light imagers. Thermal images are formed from the detected energy based upon the energy differences between the objects so that an obscured object in visible light can be visualized.

Two fundamental methods are used for IR detection: thermal and photon

detection. Both types respond to absorbed photons, but they use different response mechanisms [4]. In thermal detection, the absorbed photons cause a temperature change, and then a temperature-dependent property of the detector material is measured. In photon detection, the absorbed photons directly generate free electrons or holes. Most of the advanced IR imaging systems makes use of photon detectors due to the ease in fabrication of large 2D focal plane arrays. However, they require cooling to cyrogenic temperatures. Thermal-detection based infrared imaging systems are uncooled and lower cost systems, but their performance is limited. Table 2.1 shows classification of infrared detectors and their subtypes based on their detection mechanisms.

Table 2.1 Infrared detector types.

Photon	**Thermal**
Photovoltaic	Bolometer
Photoconductive	Pyroelectric
Photoelectromagnetic	Thermocouple
Phototransistor	Pyromagnetic
Photon Drag	Golay Cells
Quantum Counter	Liquid Crystal

Infrared detectors are usually specified by the parameters of responsivity, cutoff wavelength, and detectivity. Responsivity is the ratio of electrical output to radiant input power. Cutoff wavelength is the longer of the two wavelengths at which the responsivity of the detector is half of its maximum. Detectivity is the figure of merit that takes responsivity, noise, and detector element size into account.

A number of formats are possible for the infrared detectors. Infrared detectors are available as single element detectors, long linear arrays, or 2D focal plane arrays [5]. Single element detectors can be in circular, rectangular, cruciform, and other geometries. Linear and 2D arrays are fabricated with different device architectures. Obtaining a thermal image from a single element detector or a long linear array requires the use of a scanning mechanism across the focused object.

The electronic circuits used to transmit detector array signals to relevant terminals in an appropriate form are called Read Out Integrated Circuits (ROICs) or analog multiplexers. Figure 2.2.a shows a detector array and the Readout IC, and Figure 2.2.b shows the integration of them with flip-chip bonding technique.

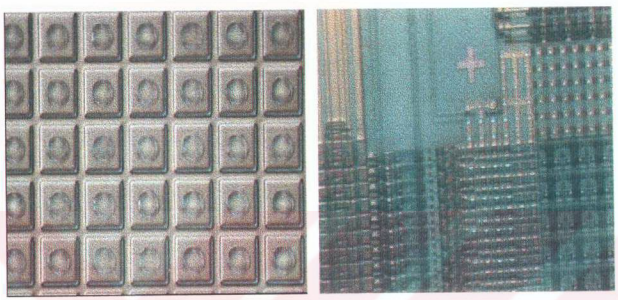


Figure 2.2.a: 128x128 detector array and Silicon ROIC.

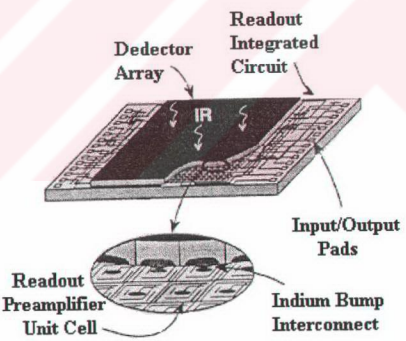


Figure 2.2.b: Schematics of flip-chip bonded detector and ROIC.

The readout element reads and transfers the signal from the image-sensing element to the output of the image sensor. Major functions of the ROICs can be summarized as,

- providing impedance buffer between detector and integration node,

- providing and maintaining detector bias,
- providing detector current,
- providing first level of signal processing,
- providing multiplexed signal output of the image sensor.

There are different readout techniques developed for IR focal plane arrays with different materials and structures. The two fundamental types of readout integrated circuits are charge-coupled-device (CCD) based and metal-oxide semiconductor (CMOS) based ones. The readout integrated circuit ISC9806 used in this thesis is CMOS based.

2.3 IR Imaging

Infrared imaging is the remote sensing and visual representation of the infrared energy emitted by all the objects. The variations in the visual representation are the result of the temperature variations across the scene. The detected radiation coming from the target and its background in the scene includes the self-emission, reflected emission, and atmospheric path radiance. Distinguishing a target from its background requires the detected radiation be different from its environment respectively.

There are a number of specifications to characterize an imaging system. Temperature resolution, the ability to measure small temperature differences, can be as fine as 0.01° C. Spatial resolution, the ability to measure temperatures on small areas, can be as fine as 15 microns. Temperature resolution is the smallest temperature difference in the scene that the system can resolve. Noise equivalent temperature difference (NETD) and minimum resolvable temperature difference (MRTD) are used to express the temperature resolution. NETD is the temperature difference for which the signal at the input equals the noise at the output. MRTD is the smallest temperature difference that can be recognized on the display. Angular resolution is the effective width of the detector element divided by the focal length of

the infrared optics. Angular resolution is also called instantaneous field of view (IFOV). System field of view, also referred as total field of view (TFOV), is the plane angel subtended by the scene imaged.

Infrared imaging technology has been developed for several applications. Hudson listed more than 100 different applications for thermal imaging systems in 1969 [6]. He categorized the list into four major divisions: military, industrial, medical, and scientific. Each division was then subdivided into (1) search, track and range, (2) radiometry, (3) spectroradiometry, (4) thermal imaging, (5) reflected flux, and (6) cooperative source.

Today, two broad categories are used: military and commercial. Table 2.2 indicates a few applications in each category. Military and commercial systems have similarities in their basic design; but each system is built for a specific purpose. As a result, different performance parameters should be used to describe military and commercial systems.

The recent tendency in infrared imaging systems is the integration of the infrared cameras with the personal computer (PC). The electronics are placed on a printed circuit board that can plug into a slot of the PC, and use the advantage of the high-resolution display, processing capability and mass storage. This integration prevents the cost overhead due to the separate displays, separate memory and enclosures.

New focal plane arrays based on thermal effects will result in high resolution cameras which can be fabricated in significantly smaller configurations and at much lower cost, however with lower performance. Focal plane arrays based on photon effects will also benefit from the reduced costs, and will be widely used in applications that need higher performance than that provided by the thermal detectors. These trends will further spur the growth in thermal imaging. The broad number of areas utilizing infrared imaging in new applications will be dramatic.

Table 2.2 Thermal Imaging Applications [7].

COMMUNITY	APPLICATIONS	
MILITARY	Reconnaissance Target acquisition Fire control Navigation	
COMMERCIAL	CIVIL	Law enforcement Fire fighting Border patrol
	ENVIRONMENTAL	Earth resources Pollution control Energy conservation
	INDUSTRIAL	Maintenance Manufacturing Non-destructive testing
	MEDICAL	Mammography Soft tissue injury Arterial constriction

2.4 IR Imaging System Electronics

An IR imaging system is composed of optics, detector, front-end electronics, digital image processing and output stages. A scanning mechanism may be required if the used detector is of a single element or long linear array format. Depending on the type of the detector, cooled or uncooled, a cooler may also be necessary. Figure 2.3 shows the electronics portion of an infrared imaging system including major sub-blocks. Buffering, gain and offset, and digitization parts compose the front-end electronics section of the system. Normalization, histogrammer, bad pixel replacement, timing generation, and video generation are included in the digital image processing section. The output of this block is sent to either a monitor for display, or to a storage equipment.

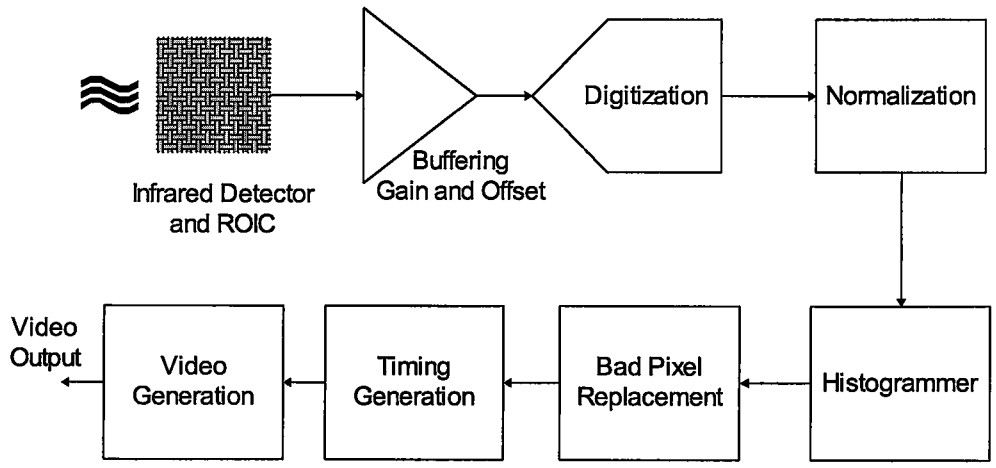


Figure 2.3: Block diagram of the IR imaging camera electronics.

Basic functions of the infrared camera electronics can be summarized as;

- Clock, syncronization and control signal generation for the detector
- Low noise bias and reference voltage generation for detector elements and ROIC
- Offset/Gain correction of detector output
- Analog-to-digital conversion of detector output
- Digital image processing section for non-uniformity corrections (NUC)
- Histogrammer block for compression coefficient calculation
- Compression for video output
- Timing generation for synchronization with required output format
- Video signal generation and image display

2.4.1 Front-End Electronics

Front-end electronics part of an infrared imaging system, following detector stage, plays an important role to designate the overall system performance. Detector interface requires careful design since bias generation must be low noise, frequently less than 100 μV. The most important role of the front-end electronics is to digitize the ROIC output with minimum distortion. Therefore, it is necessary to use high

speed, high gain/bandwidth product, and low noise components during the analog processing section of the detector output flow. Allowed noise level and required sensivity determine the number of bits of the output of ADC, which is 12 in our case.

2.4.2 Normalization for Infrared Imaging Systems

Images utilizing focal plane array detectors suffer from fixed pattern noise generated by non-uniformities in the response of the detector elements [8]. Fixed pattern noise is a result of variations in response from detector to detector in an IRFPA given a uniform input flux [9]. The presence of fixed pattern noise severely reduces the performance of the whole system, and its removal is essential.

The conventional approach to remove the nonuniformity, and hence increasing the accuracy of detector output data is to correct the detector data by calibrating, and periodically recalibrating, the detector array. While the signal processing system is off-line, a reference is introduced –such as a thermal reference source in the case of the exemplary thermal imaging systems – and the response of each detector in the detector array to the reference is recorded. Using these detector reference responses, a detector calibration error representative of deviation in detector reference response from the ideal can be computed for each detector of the detector array, and it can be used during on-line processing to correct detector output.

While the calibration correction for each detector will be different because of nonuniformities in detector-to-detector response to the reference, the reference output error for each detector can be characterized by a first order linear function ax + b, where a is a gain factor, and b is an offset level. That is, for each detector, detector response to a reference can be used to compute calibration gain (a) and offset (b) coefficients for correcting detector output. These calibration coefficients are then used to correct detector output errors during on-line operation.

2.5 Summary

This chapter makes an introduction to thermal imaging systems. It overviews the classification of IR detectors, IR detector formats, IR imaging, and applications. The front-end electronics system developed in this work receives its input from a 128x128 photon detector array coupled to a commercial readout circuit, performs analog processing, converts the signal to digital format, and sends it to the video processing and system control board. Another function of the system developed in this work is to generate bias voltages and control signals for the commercial ISC9806 readout circuit, developed by Indigo Systems Inc. (Santa Barbara, USA). In the next chapter, ISC9806 readout integrated circuit will be introduced.

CHAPTER 3

INDIGO's ISC9806 READOUT INTEGRATED CIRCUIT

Read-out integrated circuit used for the 128x128 detector array in this thesis is ISC9806 from Indigo Systems Inc (www.indigosystems.com). The ISC9806 is a high performance, 128 x 128 ROIC for p on n detectors. The ROIC supports a wide range of applications from portable infrared imagers to high-speed industrial imagers with its flexible and advanced operation modes.

A 0.6 micron single poly, double metal process benefiting from high speed CMOS transistors is used in the fabrication of the ISC9806. The ISC9806 has a 38 μm pixel pitch, and the input charge handling capacity of the unit cells are 6.2 x 10^6 electrons.

3.1 Input Circuit of ISC9806 ROIC

Figure 3.1 shows the simplified unit cell schematic for ISC9806 input circuit, using direct injection method. Detector current passing through the input gate transistor integrates on the integration capacitor. The anti-bloom gate prevents the input circuit from saturating. The integrated voltage is read out and multiplexed to the column amplifier. The control of the detector bias is realized by applying a bias to the Vdet_adj pad in default mode and by using the Serial Control Register of the ROIC in command mode.

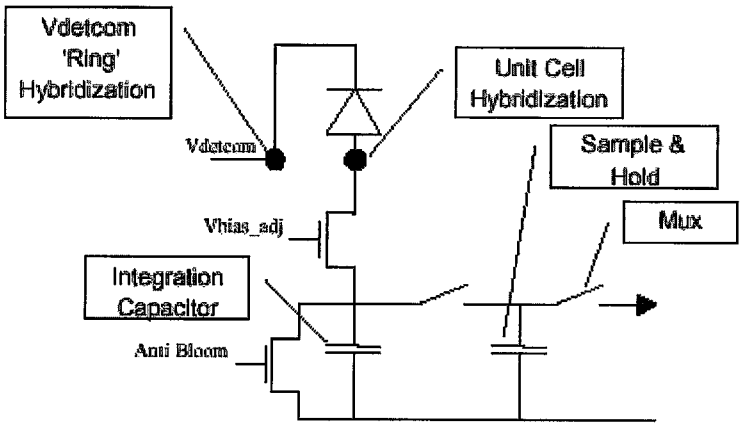


Figure 3.1: Simplified unit cell schematic for ISC9806 input circuit, where direct injection method is used [10].

3.2 Interface Connections

ISC9806 has a total of 38 interconnects and some of them are reserved for factory testing as shown in Figure 3.2. Table 3.1 gives the pinout descriptions of the ISC9806 ROIC.

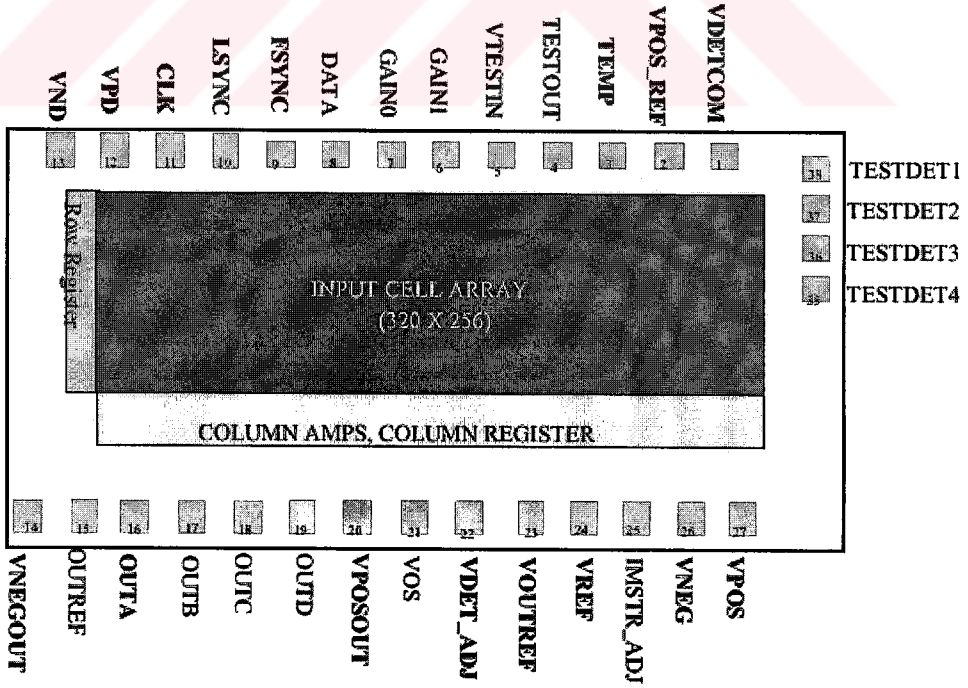


Figure 3.2: ISC9806 pinout schematic [10].

Table 3.1 Pinout descriptions of the ISC9806 ROIC [10].

Pin No	Signal Name	Description
6	Gain0	External Gain: These pins are used to control the gain of the chip when operating in Default Mode
7	Gain1	
8	Data	Serial Control Register Data
9	Fsync	Frame Sync
10	Lsync	Line Sync
11	Clk	Data Output and Command Data Stream Clock
16	OutA	Video Output A
17	OutB	Video Output B
18	OutC	Video Output C
19	OutD	Video Output D
15	Outref	Common Mode Reference Output
3	Temp	Buffered Temperature Diode
23	Voutref	Analog Output Reference Voltage
21	Vos	Skimming Voltage
24	Vref	Analog Reference Voltage
22	VdetAdj	Detector Bias Adjustment
25	ImstrAdj	Master Current Adjustment
1	Vdetcom	Detector Common
2	VposRef	Low Voltage Detector VDETCOM Supply
27	Vpos	Analog Supply
12	Vpd	Digital Supply
20	Vposout	Output Supply
13	Vnd	Digital Return
15	Vnegout	Output Ground
26	Vneg	Analog Ground

3.3 Operation Modes

The ISC9806 has two operation modes; a simplified Default Mode and a programmable Command Mode. In default mode, fewer external pad connections are required and only single output, full window, NTSC or PAL operation is supported. The Command Mode requires more external pad connections and enables the use of advanced features such as dynamic image transposition, dynamic windowing, high speed multiple output configurations and adjustable global offset.

3.3.1 Default Mode

This mode has a simple interface with reduced external electronics and power dissipation. This mode is suitable for applications where advanced ROIC features or high-speed performance are not required. Serial Control Register is not used in the default mode. Therefore, advanced features of the ROIC such as windowing, invert/revert and multiple data outputs are not available in the Default Mode. The maximum input clock frequency is 3.07 MHz providing an output rate of 6.14 MSPS maximum for default mode. At power-up, the device defaults to operation as a standard 128x128 format imager. Figure 3.3 shows the block diagram for default mode operation. Default Mode operation of ROIC requires a total of 19 interconnects.

In default mode, the bias applied on the Vdet_adj pad controls the detector bias. The detector bias is defined as the difference between the Vdetcom potential and the detector input bias potential as shown in Figure 3.4, which illustrates a typical direct injection ROIC circuit. Maximum forward detector bias is obtained by adjusting Vdet_adj to 5.5V, and maximum reverse bias condition is achieved by setting the bias applied to this pad to 0 V.

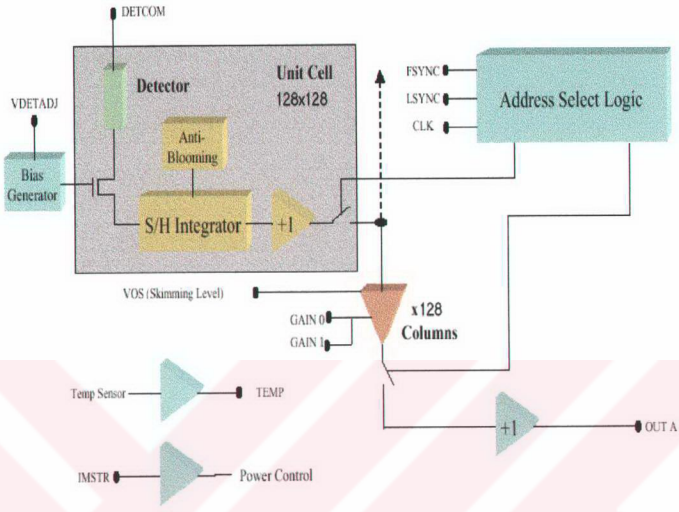


Figure 3.3: Block diagram for default mode operation in Indigo Systems' ROIC [10].

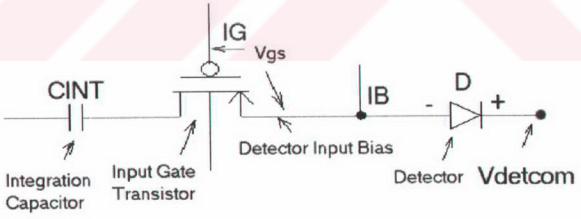


Figure 3.4: Typical direct injection circuit [10].

3.3.2 Command Mode

Command Mode operation makes use of the on chip Serial Control Register to control operation modes and advanced ROIC features. Figure 3.5 illustrates the

fields of the serial control register. The DATA pad is used to load control words into the serial control register to operate in this mode. The settings in this register determine the gain state, detector bias setting, power bias control, master current bias, skimming setting, output mode, window size, window position, image transposition and test mode. 16-20 interconnects are required, depending on the number of outputs and options invoked. There are 4 digital input signals:

- FSYNC : Controls frame start and integration time,
- LSYNC : Controls line readout timing,
- CLK : Master clock frequencies up to 5 MHz (10 MHz output rate) are supported when the ROIC is in the Command Mode.
- DATA : For command mode operation, IMSTR_ADJ, VDET_ADJ, GAIN0 and GAIN1 pads are controlled through command words shifted into the serial control register via the DATA input pad. The DATA pad is driven as a clock signal.

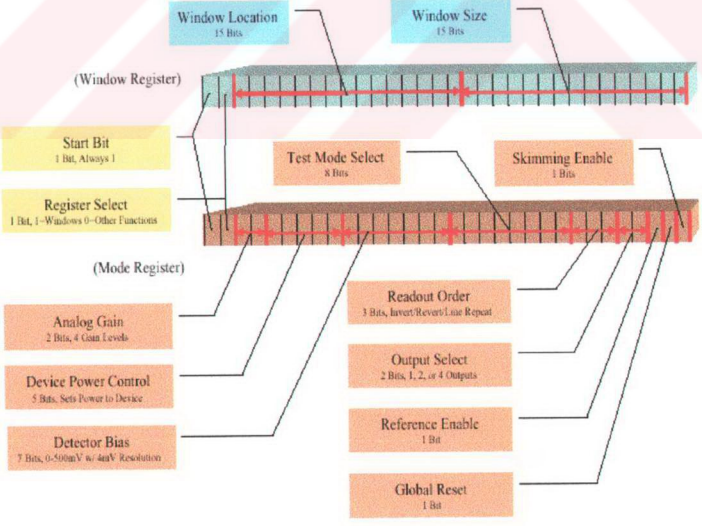


Figure 3.5: Serial control register [10].

The supply voltages are,

- VPOS : Positive supply for all analog circuits,
- VPD : Positive supply for all digital circuits,
- VNEG : Ground for all analog circuits,
- VNEGOUT : Ground for all analog circuits except output multiplexer and buffers,
- VND : Ground for all digital circuits,
- VREF, VOUTREF : Reference supply voltages

Other pads are as follows:

- VDETCOM : Detector substrate connection. Detector common bias is set by the voltage applied to this pad. The bias supplied to this pad may be in the range of 0 to 8.5 volts referenced to VNEG (at 0 volts). VDETCOM pad and VPOS_REF pads are connected together using a floating off chip pad for low reverse bias voltage detectors such as InSb photodiodes. VPOS_REF pad should not be applied any bias since VPOS_REF pad is a low impedance voltage output pad from the readout to the system.
- VOS : Skimming control voltage,
- TEMP : Temperature monitoring pad, an ADC is needed to display the temperature sensor output,
- OUTA-D : Output pads,
- OUTR : Reference output pad.

GAIN0 and GAIN1 pads are used to adjust the amplifier gain. The four possible gain states are given in Table 3.2:

Table 3.2: Gain States for internal amplifier of ROIC [10].

GAIN1(GC1)	GAINO(GC0)	Relative Signal Gain
0	0	1 (default)
0	1	1.33
1	0	2
1	1	3.8

In the command mode operation, the amplifier gain is adjusted through the Serial Control Register field GC(1:0), and GAIN pads should be driven low or left floating.

Detector bias adjustment is controlled through the Serial Control Register field DE(6:0) in command mode. When power is applied to the readout, the detector bias initializes to near the highest forward bias condition, also DE(6:0) is set to "0000000". Figure 3.6 shows that programming DE(6:0) to "1111111" will set the detector input bias to the maximum reverse bias condition. The detector bias can be read through the Vdet_adj pad in the command mode.

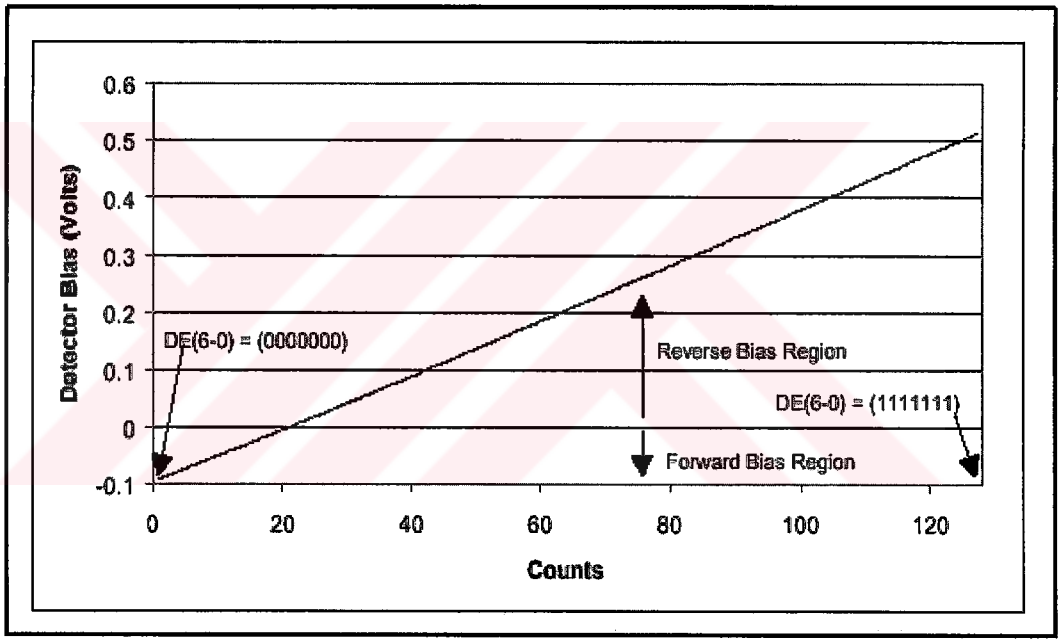


Figure 3.6: Command mode detector bias [10].

The chip is in the single output mode with the lowest power setting and disabled output reference in the default power up state. The power may need to be increased according to the mode of the operation required. This is achieved by using the Serial Control Register field PW(1:0) and I(2:0).

The I(2:0) field allows adjustment of the master current source to cover the requirements for process variations or changes in current requirements due to the

operating temperature of the device. When power is applied to the chip, I(2:0) defaults to "100", which corresponds to approximately 100 μA master current source. The master current can be increased by about 20% with a maximum setting of "111", and can be decreased by about 20% with the minimum setting of "000".

The PW(1:0) field is used to provide major current adjustments, that may be required for different clock rate applications. The two bits of the PW(1:0) field are sent to an on chip DAC which adjusts the transistor currents in the signal path. The default value at power up for PW(1:0) is "00", which corresponds to the minimum current condition. Adjusting the PW(1:0) field to "11" sets the bias to maximum current condition. The finest possible bias adjustment resolution with this method of current adjustment is equal to the minimum current with a maximum adjustment range of approximately 4 times the minimum current. Adjustments to the power settings have no effect on the power of the output driver circuitry. For a master clock frequency of 5 MHz, and 4 output mode, PWR(1:0) should be "11" and I(2:0) should be "000".

The skimming level adjustment is a global offset function utilized in the column amplifier circuit. Operating the skimming function requires the VOS pad be biased to a voltage greater than the voltage on the VREF pad. The VOS voltage is in the range of VREF to VPOS, which corresponds to offsetting from 0 to 100 % of full well. The skimming function is disabled by setting the OE bit in the Serial Control Register to 0. Setting the OE bit to 1 enables skimming. The setting of the skimming voltage is implemented through the VOS pad. Figure 3.7 describes the command mode operation.

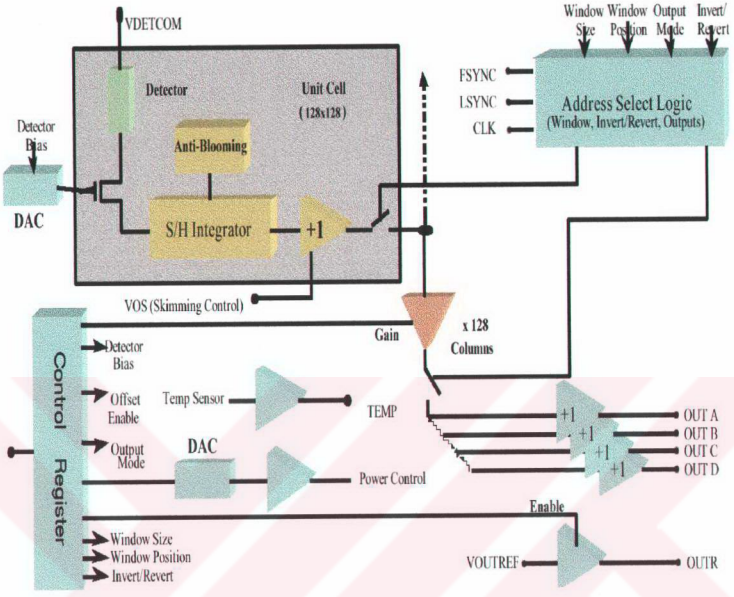


Figure 3.7: Block diagram for command mode operation [10].

The advanced features of the readout, including windowing, invert/revert readout order, output selection, reference enable, global reset, skimming enable, test mode selection, detector bias adjustment, master current adjustment, device power control and analog gain settings, are controlled by the 32-bit Serial Control Register. The Serial Control Register can contain two types of data words: a window or a mode word. A window word includes the row and column starting address along with the size of the window. A mode word contains operation mode parameters and adjustments to control the readout.

All register bits, fields and functions are described below starting with the Window Data Word.

Register Bit	Field	Function
D29	Start Bit	Defines start of control word, 1 for valid word
D28	Register Select	Determines window/mode word, window word = 1
D27-D24	Unused bits	Not used
D23-D18	WAX(5:0)	Window start address for column
D17-D12	WAY(5:0)	Window start address for row
D11-D6	WSX(5:0)	Readout window size, # of columns
D5-D0	WSY(5:0)	Readout window size, # of rows

For the Mode Data Word:

Register Bit	Field	Function
D29	Start Bit	Defines start of control word, always=1 for valid word
D28	Register Select	Determines window/mode word, mode word =0
D27-D26	GC(1:0)	Sets the amplifier gain state
D25-D24	PW(1:0)	Power control adjustment
D23-D21	I(2:0)	Master current adjustment
D20-D14	DE(6:0)	Setting for detector bias adjustment
D13-D8	TS(5:0)	Test functions for factory characterization testing only
D7-D5	RO(2:0)	Selects readout order

RO2	RO1	RO0	XDIR	YDIR	Line Repeat
0	0	0	normal	normal	no
0	0	1	normal	normal	yes
0	1	0	normal	invert	no
0	1	1	normal	invert	yes
1	0	0	revert	normal	no
1	0	1	revert	normal	yes
1	1	0	revert	invert	no
1	1	1	revert	invert	yes

D4-D3	OM(1:0)		Selects number of outputs
	OM1	**OM2**	**Number of Outputs**
	0	0	1
	0	1	2
	1	0	3
	1	1	4
D2	RE		Reference output, 0=disable, 1=enable
D1	RST		Reset to power up conditions
D0	OE		Skimming, 0=disable, 1=enable

The Serial Control Register is loaded through the DATA input pad. Figure 3.8 shows the timing of valid DATA relative to the FSYNC signal. DATA is sampled on the falling edge of CLK. During a frame time, a control word is loaded once, and 32 clock cycles are required to load a control word. After a control word has been loaded, it is held to be applied on the next rising edge of FSYNC. A new control word is only required if settings need to be changed. If a new control word is not loaded before the rising edge of FSYNC, the existing settings are applied. A detailed view in Figure 3.9 shows that a valid control word has the rising edge of the start bit either at least 32 clock cycles before the rising edge of FSYNC or at least 3 clock cycles after the rising edge of FSYNC.

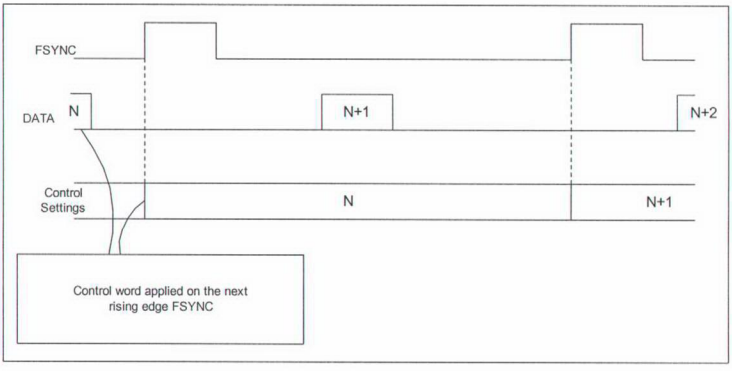


Figure 3.8: Serial Control Register Timing.

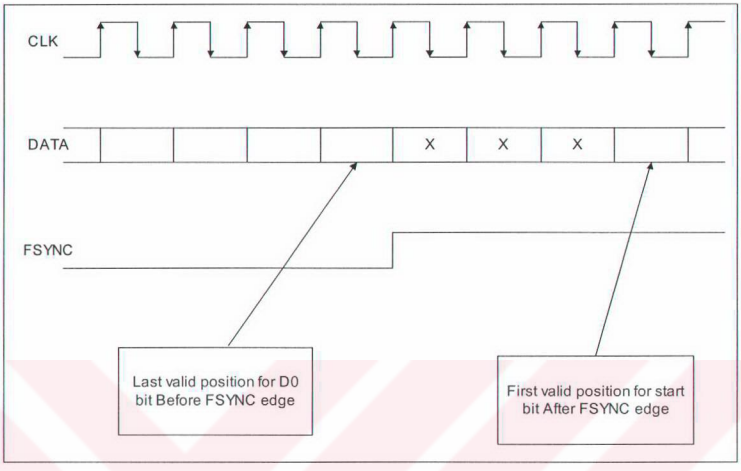


Figure 3.9: Detailed timing for Serial Control Register.

3.4 Output Modes

Readout can be adjusted to support one, two or four outputs with or without an output reference. The OM(1:0) bits of the Serial Control Register designate the number of outputs for the chip. In the single output configuration, all pixels are read out through OutA. In the multiple output configuration, pixels are allocated to a specific output channel, and will be read through only that channel, regardless of the image transposition (invert/revert), and windowing modes. When four-output mode is selected, the first pixel appears at OutA, the second pixel appears at OutB, the third pixel at OutC, and the forth at OutD. Alternating in four pixel increments, pixels appear at the A, B, C and D output channels, respectively. For four output mode, OM(1:0) should be "11".

3.5 Windowing

The readout full window size is 128 x 128, which is the default window size. The window size can be changed in the Command Mode. The Serial Control Register

data bits WAX(5:0) and WAY(5:0) determine the column and row start addresses, respectively. The data bits WSX(5:0) and WSY(5:0) define the window size by the number of columns and the number of rows, respectively.

3.6 Readout Timing

The readout time is dependent on pixel rate, number of outputs, window size, line repeat mode and line dead times. Setting the bit RO0 in the Serial Control Register controls the line repeat mode. The timing diagram in Figure 3.10 shows the readout timing.

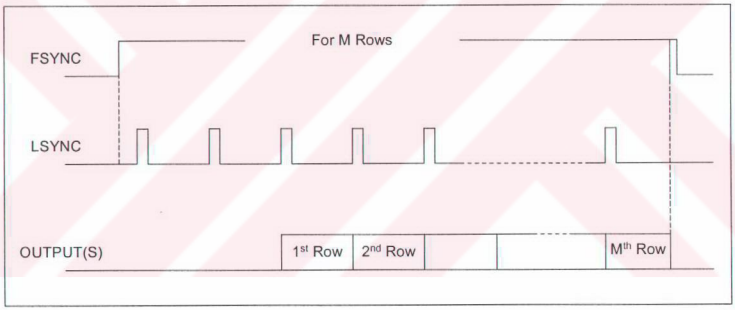


Figure 3.10: Readout timing.

As shown in a more detailed timing in Figure 3.11, a line time is composed of the analog setup time plus the active pixel time plus any line dead time. The analog setup time is minimum 16 clock cycles, and the active pixel time is also minimum 16 clock cycles, resulting in a line time of minimum 32 clock cycles in the four output mode.

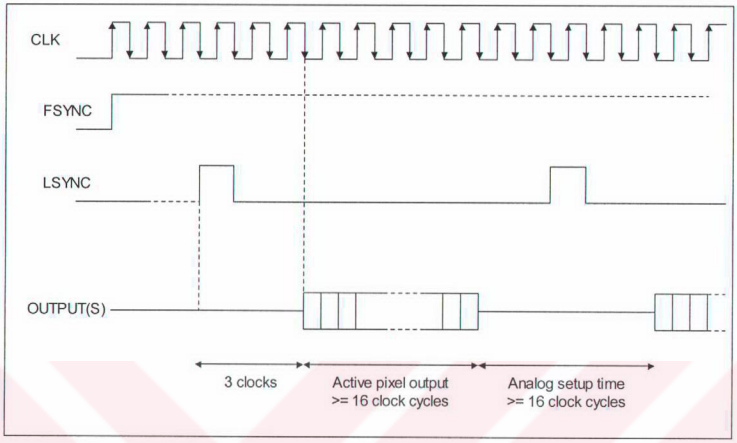


Figure 3.11: Detailed timing for readout.

3.7 Integration Modes

The ISC9806 ROIC samples all the pixels at the same time (snapshot integration) and the process is controlled by the FSYNC (Frame synchronization) clock of ROIC. There are two modes for this snapshot integration, Integrate-While-Read and Integrate-Then-Read modes.

A timing diagram related to the Integrate-While-Read mode is shown in Figure 3.12 next. Frame time starts with the rising edge of the FSYNC signal. Integration of the next frame starts after the falling edge of the FSYNC and occurs during current frame readout. Readout phase includes LSYNC (Line synchronization) pulses required for row and column synchronization. In this mode, frame time nearly equals the readout time.

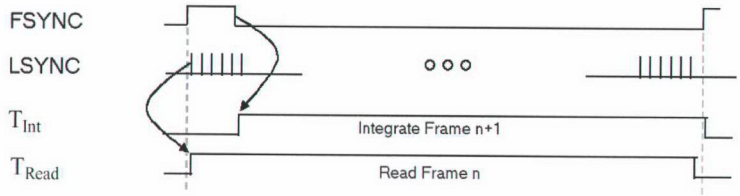


Figure 3.12: Integrate-While-Read timing diagram [10].

For the Integrate-Then-Read Mode, frame time starts with the rising edge of FSYNC. Figure 3.13 shows a timing diagram for the Integrate-Then-Read mode. In this mode, FSYNC clock remains high until the readout sequence has been completed. Since readout and integration parts are separated and follow each other, frame time is approximately equal to the readout time plus the integration time.

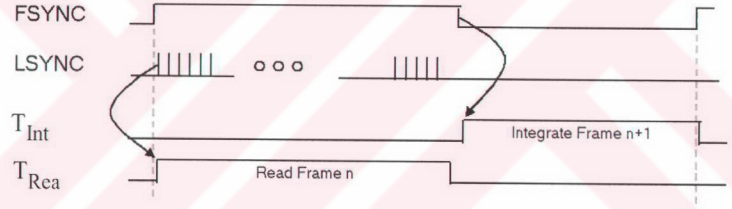
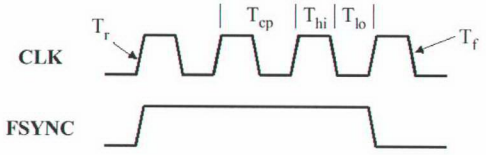


Figure 3.13: Integrate-Then-Read timing diagram [10].

3.8 Integration Time

For a predefined master clock frequency (MC) and frame time, variations on the ON and OFF time of the FSYNC clock pulse determines the integration time of the ROIC. The rising edge of the FSYNC clock starts the integration process and location of its falling edge controls the integration time. In order to provide synchronization between the FSYNC and the ROIC logic, FSYNC clock should be changed on the rising edge of the master clock. It is required that minimum OFF time of FSYNC clock must be at least one clock cycle per frame. Any change made on the FSYNC clock duty cycle will be applied to the logic circuitry on the next falling edge

of the master clock. Figure 3.14 shows the detailed timing of the rising and falling FSYNC edges with respect to the master clock.



Parameter	Min	Typ	Max	Comments
T_r	-	-	10ns	10-90% (All signals)
T_f	-	-	10ns	90-10% (All signals)
T_{sh}	5ns	-	-	Setup / Hold Time: All Signals to CLK Edge
T_{cp}	200ns	-	-	10MHz Pixel Rate
T_{hi}	-	$.5*T_{cp}$	-	Clock Duty Cycle = 50%
T_{lo}	-	$.5*T_{cp}$	-	Clock Duty Cycle = 50%

Figure 3.14: Detailed timings for digital control signals [10].

Approximate integration time for the Integrate-Then-Read Mode can be calculated approximately as

$$Tint \approx Tframe - (Tfsync - 25.5 \text{ MC cycles}) \quad (3.1)$$

where

Tint : Integration time, measured in MC cycles

Tframe: Frame time, measured in MC cycles

Tfsync : Width of fsync clock pulse, measured in MC cycles.

3.9 Summary

This chapter introduces the Indigo Systems' ISC9806 readout integrated circuit, presenting its circuit architecture, interface connections, operational modes and pad functions. Serial control register controlling readout circuitry is described with related timings. Detector signal output timings are also examined. The chapter concludes with integration modes and integration timings. The next chapter will present the design of the front-end electronics board implemented in this work.

CHAPTER 4

FRONT-END ELECTRONICS SYSTEM DESIGN

4.1 Introduction

Front-end electronics system plays an important role in determining the imaging system's performance. This chapter describes the design of the front-end electronics board implemented in this thesis including the hardware design rules followed and the user interface program written with HPVEE.

Front-end electronics is the interface electronics between detector readout and video processing board. Figure 4.1 shows the simplified interface diagram of the front-end electronics board with the other blocks in the system. The main function of the system is to convert analog outputs of the detector to 12-bit digital data, to generate command signals for the readout and to generate some control signals for the video processing and system control electronics.

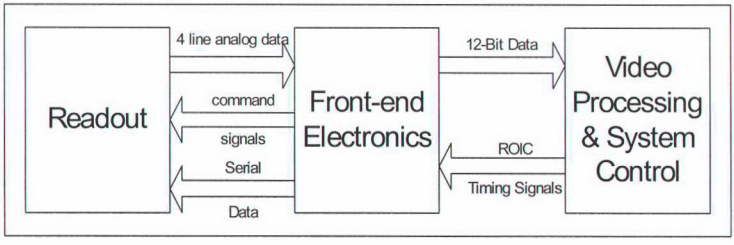


Figure 4.1: Simplified interface diagram of the front-end electronics board with the other blocks in the system.

The details of the functions of the front-end electronics board are given in the following sections. Section 4.2 describes the operation and interface. Section 4.3 explains the analog section of the board. Section 4.4 focuses on the digital section of the board. Section 4.5 overviews the printed circuit board (PCB) design rules followed. This chapter concludes with normalization algorithm given in Section 4.6.

4.2 Operation and Interface

Figure 4.2 shows the interface block diagram of the front-end electronics system with the other blocks in the thermal imaging system. Figure 4.3 illustrates the major blocks of the front-end electronics system.

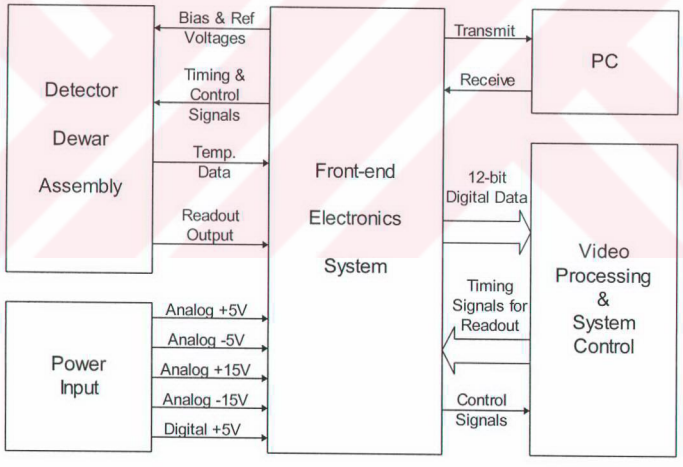


Figure 4.2: Interface block diagram of the front-end electronics system.

The system is composed of two parts: analog and digital. Functions of the analog section include low-noise readout bias and reference generation, detector signal unity gain buffering, DAC controlled global gain and offset level generation, clamping, differential ADC driving, 12-bit video digitization, DAC controlled gain

offset and readout temperature monitoring. Digital section provides sampling and multiplexing of digital data, PC communication with HPVEE user interface program, digital-to-analog converter control for global gain/offset levels and readout biases, serial ADC control for potentiometer-controlled settings and SRAM interface to store scene data for normalization coefficient calculation. The HPVEE user interface program controls the ROIC operation through the ROIC serial control register.

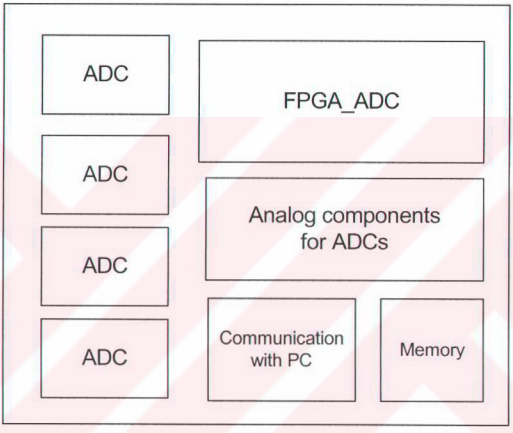


Figure 4.3: Major front-end electronics system blocks.

4.3 Analog Section

Analog section is the block where the analog processing of ROIC output, bias and reference generation for the ROIC and potentiometer controls are implemented. Figure 4.4 gives the block diagram for the analog section. The selection of the analog components used in this system is leaded by low-noise, sufficient bandwidth and fast settling time requirements. All of the components are industrial grade for better temperature dependance and surface-mount to reduce noise coupling and area related problems. The following sections describe the analog section of the front-end electronics board, including buffering, offset and gain amplifier and control, clamper,

differential driver, analog-to-digital conversion, bias and reference generation, and temperature data monitoring.

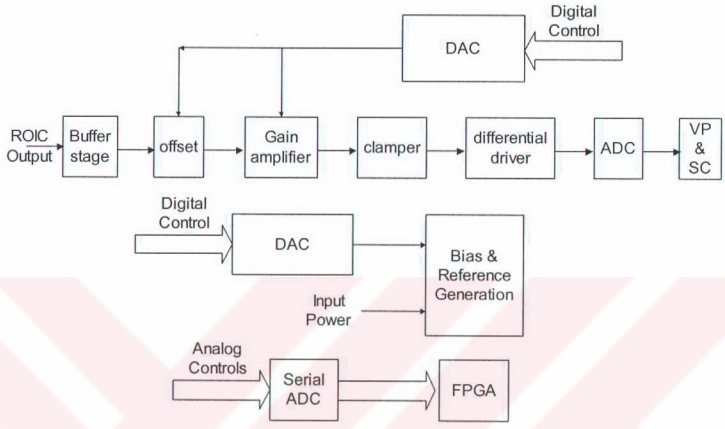


Figure 4.4: Block diagram for the analog section.

4.3.1 Buffering

The first component in the analog data processing chain is the CLC114 [11], quad low-power video buffer from National Semiconductor. The ROIC output requires a minimum resistance of 100KΩ and a maximum capacitance of 25 pF as the load for a proper transmission. However, AD812, used for offset level correction at the next stage, has an impedance of 65Ω at the negative input, so a buffer stage is needed at the ROIC outputs, otherwise connecting the source directly to the load would result in significant signal attenuation. Hence, 4 pixel outputs of the readout are buffered first. Assuming the system will work at 10 MHz sampling rate, and examining other specifications of the buffer which are given below, CLC114 is selected to be used as a buffer. Figure 4.5 gives the pinout for CLC114.

- Low supply current 16.5 mA
- Wide -3dB BW >135 MHz

- Fast slew rate 200 V/s
- Gain flatness ±0.8dB
- Equivalent Input Noise -155 dBm_{1Hz}

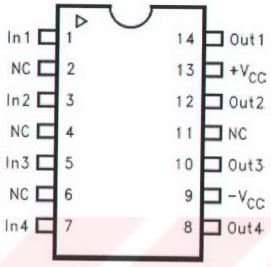


Figure 4.5: Pinout for CLC114 [11].

The output voltage range for CLC114 is 0 - 3.8V for a single +5V supply. Since ROIC output voltage is between 1.6V and 4.6V with 3V swing, use of 5V supply would clip the CLC114 output, so a higher supply is needed. For this purpose, a voltage divider circuit is used to obtain 7.5V from the 15V power input. The opamp used in this circuit is OP413 [12] from Analog Devices. The circuit used for this purpose is shown in Figure 4.6.

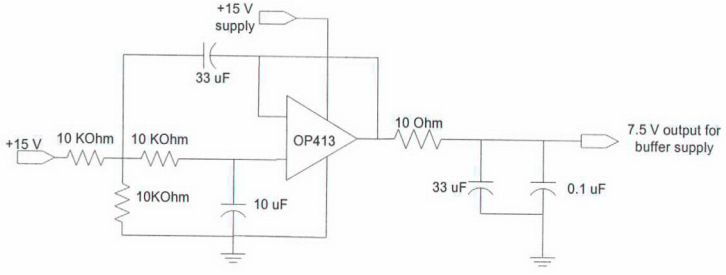


Figure 4.6: Divisor circuit for 7.5V supply generation.

4.3.2 Offset and Gain Amplifier and Control

Analog gain and offset control provide scene dynamic range management [13]. The input signal range presented to the analog-to-digital converter can be optimized to a particular scene content by adjusting the gain and offset resulting in maximum sensivity. In this work, offset and gain level generation is controlled by an FPGA (Field Programmable Gate Array), which writes to a Digital-to-Analog Converter (DAC) to generate the required voltages. To change the gain and offset levels, either Hewlett-Packard Visual Engineering Environment (HPVEE) user interface program or potentiometers on the board connected to a serial ADC are utilized. HPVEE is an iconic programming language optimized for instrument control by Hewlett-Packard.

User inputs through the PC are first converted to binary to be sent to the board in RS232 format. The incoming serial data through the RS232 port is converted to CMOS level by a transceiver IC, and sent to the FPGA. The serial data is then converted to parallel to form 12-bit digital data and written to the digital-to-analog converter which outputs the analog signals required for gain and offset control. Front-end electronics board output to the PC is first converted from parallel to serial and then sent to the transceiver by the FPGA. PC monitor showing user interfacing through the HPVEE program is presented in Appendix A.

Offset and gain levels can also be controlled through the potentiometers on the board. Manual control of gain and offset settings are realized by an 8-channel, 125 kSPS, 12-bit serial ADC, AD7888 [14] from Analog Devices. Figure 4.7 gives the pinout for AD7888. The offset and gain inputs of the ADC are sampled and the result is sent to FPGA in serial form. This serial data is converted to parallel by the FPGA and the data is written to a DAC. The digital timing and control signals for conversion by the DAC are formed by the FPGA. Figure 4.8 shows the DAC circuit producing vskim and gain signals.

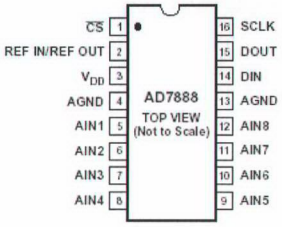


Figure 4.7: Pinout for AD7888 [14].

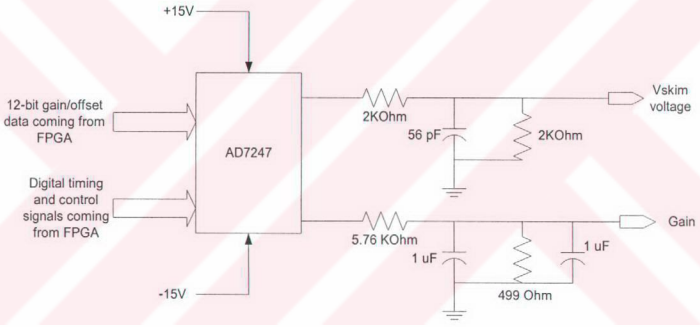


Figure 4.8: DAC circuit producing vskim and gain signals.

The output of the DAC generating the vskim and gain signals is between –5V and +5V, but a negative offset of 0 to –5V is needed to bring the ROIC output which is in the range of 1.6 - 4.6V to ±1.5V range, so that the ROIC output with the appropriate gain matches the ADCs' input range. Hence, the DAC output for vskim is divided by 2 and with the circuit shown in Figure 4.9, 2.5V is subtracted from the divided signal to obtain an offset voltage between 0 and –5V. The opamp used in this circuit is OP413.

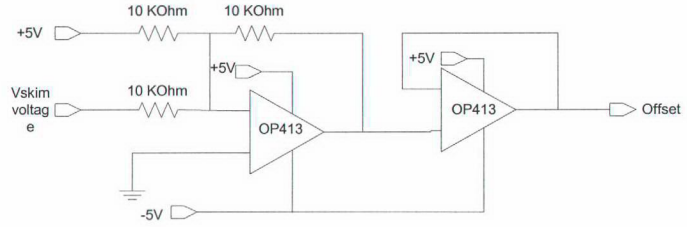


Figure 4.9: 2.5V subtraction circuit from the divided vskim signal to obtain offset signal.

The buffered ROIC data is sent to an opamp configured to add the above offset in order to fit the video signal to the A/D converter's input range. The ROIC data is between 1.6V and 4.6V. Thus, an offset of –3.1V will convert the output to be in the range of ±1.5V. If we apply a gain of 1.67, then the output will be in the range of ±2.5V. AD812 [15], dual low-power opamp, from Analog Devices is used for the offset setting stage. Figure 4.10 shows the pinout of AD812. Figure 4.11 presents the circuit used to add offset and a gain of 1.67 to the buffered ROIC data.

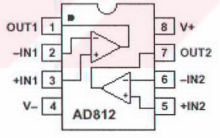


Figure 4.10: Pinout for AD812 opamp [15].

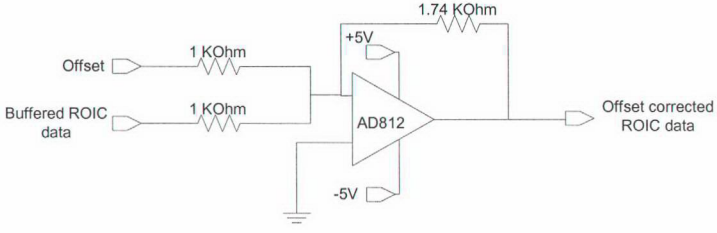


Figure 4.11: The circuit used to add offset to the buffered ROIC data.

Gain level generation, one of the most significant functions of front-end electronics system, is similar to the offset level generation. It may be either through the HPVEE user interface program or through the potentiometers. The output of the DAC is sent to AD602 [16], dual low-noise wideband variable gain amplifier from Analog Devices as shown in Figure 4.12. The gain of AD602 can be calculated using the following equation:

$$\text{Gain (dB)} = 32\ V_G + 10 \tag{4.1}$$

where V_G is the variable gain amplifier output coming from the DAC output. V_G is set to be in the range of ±0.398V to make amplification by a factor of 14 possible.

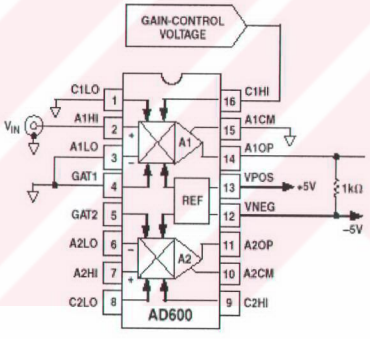


Figure 4.12: AD602 input and output [16].

The other important parameters of the AD602 are its input resistance (100 Ω), input capacitance (2pF), output impedance (2 Ω) and the nominal maximum input signal (VINP). Maximum input signal should be 1 V rms (1.4 V peak) when using the recommended ±5 V supplies. In order to prevent any malfunction, a 100 Ω series resistance is put at the input side of the amplifier as an amplitude divider. Figure 4.13 shows the circuit used for variable gain amplification of the two ROIC outputs. A similar configuration is used for the other two outputs of the ROIC.

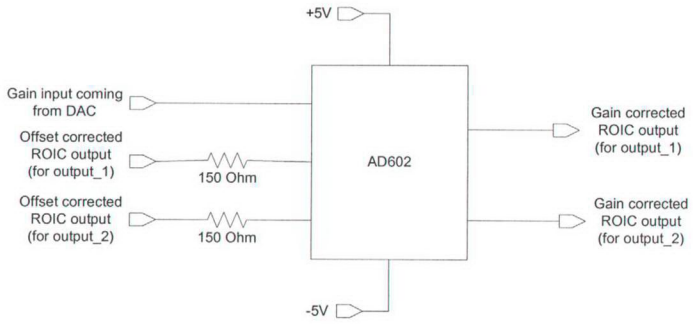


Figure 4.13: The circuit used for variable gain amplification.

4.3.3 Clamper

The amplified ROIC data is clamped to prevent the following stages of data flow from damage due to overvoltage. Clamping IC used here is CLC502 [17], which is an operational amplifier designed for low-gain applications, from National Semiconductor. This feature allows setting maximum positive and negative output voltage levels for the amplifier, thus allowing the CLC502 protect the following circuitry. The clamping voltages are selected to be ±2.5V. Figure 4.14 shows the pinout for CLC502.

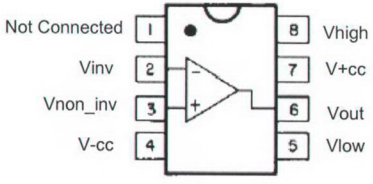


Figure 4.14: Pinout of CLC502 [17].

Offset-added ROIC data changes polarity due to the adder circuit designed. Another polarity reversing operation must be done to have the original polarity. This is done by connecting the ROIC data to the inverting input of the clamping amplifier.

4.3.4 Differential Driver

The next step is the AD8138 [18], low distortion differential ADC driver. A dramatic improvement in total harmonic distortion (THD) and spurious free dynamic range (SFDR) performance can be realized by operating the AD9220, the ADCs used on this board, in the differential mode. Therefore, to drive the ADCs differentially, AD8138 from Analog Devices is used. Figure 4.15 shows the pinout for AD8138.

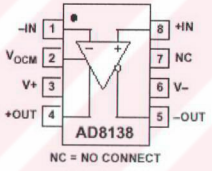


Figure 4.15: Pinout of AD8138 [18].

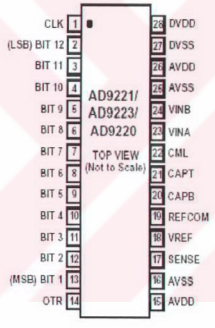
4.3.5 Analog-to-Digital Conversion

A/D converter's analog input range, number of conversion bits, sampling frequency, conversion time, power dissipation and number of supplies were among the important considerations during the selection of the ADC. The ADC satisfying all our requirements is AD9220 [19], complete 12-bit 10 MSPS Monolithic A/D converter. The key specifications of the ADC can be summarized as;

Digitization	12 bits
Input Range	5V peak-to-peak,
Conversion rate	10 MSPS
Input Capacitance	16 pF

Input Resistance	5 KΩ
Power Supply	Analog +5V and Digital +5V
Logic I/O	+3 V or +5 V
Digital Outputs	TTL/CMOS Outputs
Reference voltage	preferred 2.5V
Effective Input Noise	0.09 LSBs rms
Integral Nonlinearity	±1.25 LSB max
Differential Nonlinearity	±0.75 LSB max

Figure 4.16 shows the AD9220 pinout and pin descriptions.



Pin Number	Name	Description
1	CLK	Clock Input Pin
2	BIT 12	Least Significant Data Bit (LSB)
3–12	BIT N	Data Output Bit
13	BIT 1	Most Significant Data Bit (MSB)
14	OTR	Out of Range
15, 26	AVDD	+5 V Analog Supply
16, 25	AVSS	Analog Ground
17	SENSE	Reference Select
18	VREF	Reference I/O
19	REFCOM	Reference Common
20	CAPB	Noise Reduction Pin
21	CAPT	Noise Reduction Pin
22	CML	Common-Mode Level (Midsupply)
23	VINA	Analog Input Pin (+)
24	VINB	Analog Input Pin (–)
27	DVSS	Digital Ground
28	DVDD	+3 V to +5 V Digital Supply

Figure 4.16 Pinout and pin descriptions for AD9220 [19].

Selected ADC requires a single 5V supply. Therefore, before the ADC input, the signal should be DC shifted to the mid-rail of the ADC reference, creating a virtual ground to the ADC input. Differential-driven ROIC data is DC restored with 2.5V to the mid-rail of ADC reference to use full dynamic range of the ADC with CML output of the ADC connected to the V_{OCM} (common mode voltage) input of the differential driver. Figure 4.17 shows the analog-to-digital conversion circuit including the differential driver AD8138.

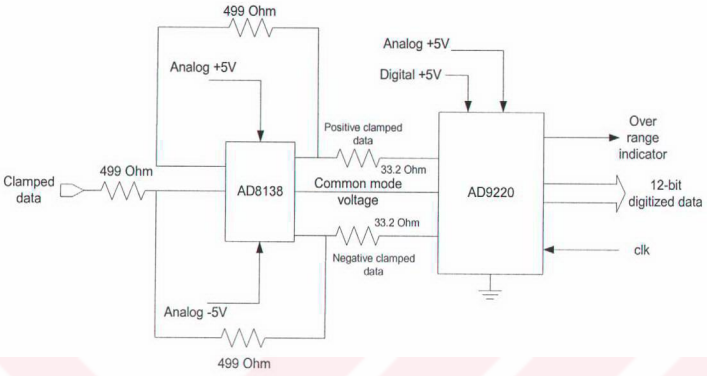


Figure 4.17: The analog-to-digital conversion circuit including the differential driver AD8138.

4.3.6 Bias and Reference Generation

Readout bias and reference voltages are generated in two ways. The fixed voltages are produced by a divider opamp circuit that uses an OP413. 5.5V voltage for the analog and digital supplies of the readout and 1.6V for ROIC reference voltage are produced by this circuit. Figures 4.18 and 4.19 show the circuits for generating 5.5V and 1.6V supplies, respectively.

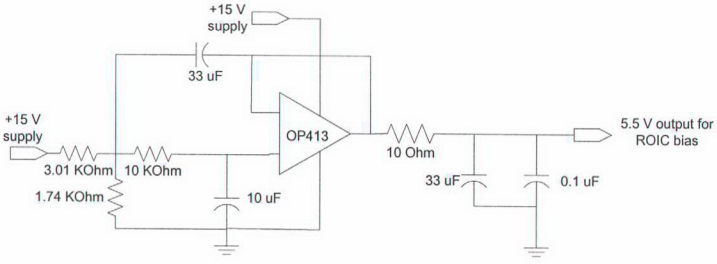


Figure 4.18: 5.5V generation circuit.

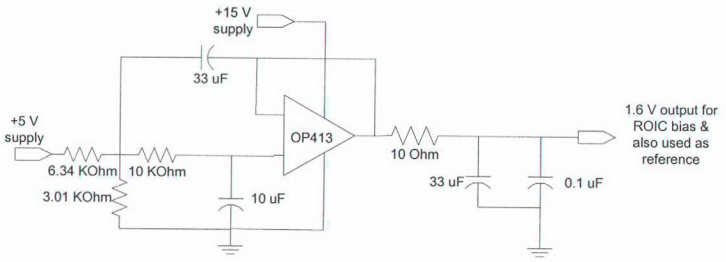


Figure 4.19: 1.6V generation circuit.

Vdet_com and Vos skimming inputs need varying voltages, therefore they are controlled by the FPGA. The controlling digital data can be written to FPGA either from HPVEE user interface program or by using the on-board potentiometers. The digital data for the control of these voltages are written to DAC. The DAC chip used is AD7247 [20], LC^{2}MOS Dual 12-bit DACPORTs. It has two DACs in the IC, and has digital controls to select the DAC of interest. Each of the outputs can be configured to be in 0 to +5V, 0 to +10V or –5V to +5V range.

One of the outputs of the DAC goes to an adder circuit utilizing AD812 and forms the skimming voltage, Vos, which changes between 1.6V and 5.5V. The other output is forwarded to a buffer circuit utilizing AD812, to produce Vdet_com, which varies between 1.6V and 8.5V. Figure 4.20 shows the generation of these voltages.

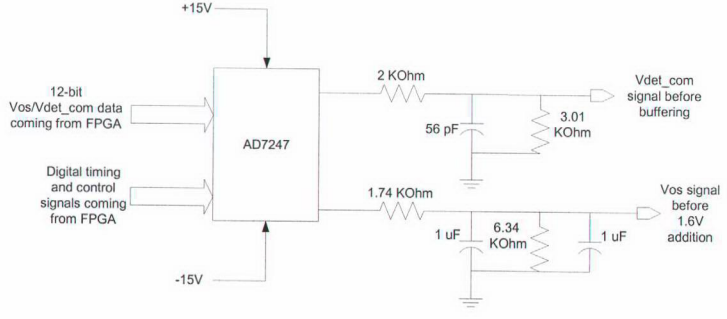


Figure 4.20: Generation of Vos and Vdet_com biases before processing.

The DAC producing Vos is fixed to give 0 to +5V. Vos is variable in a range of 1.6V to 5.5V. Hence, the DAC output, Vos signal before 1.6V addition, is adjusted to be in the 0 to 3.9V voltage range, and 1.6V is added to this output to form Vos. Figure 4.21 shows this adder circuit.

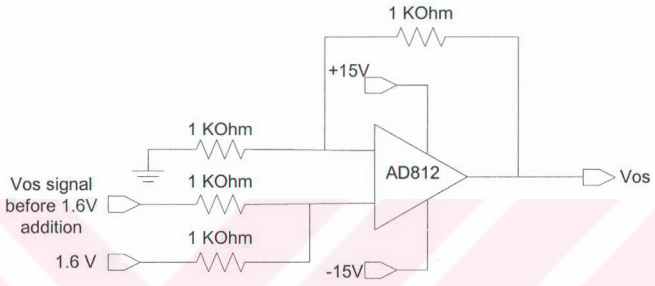


Figure 4.21 Adder circuit to form Vos.

Vdet_com is variable in the range of 1.6V to 8.5V, so the DAC producing Vdet_com signal before buffering is adjusted for 0 to 10V output range. The buffer circuit is used to clip the output, Vdet_com signal before buffering, to the required voltage levels. Figure 4.22 shows the buffer circuit.

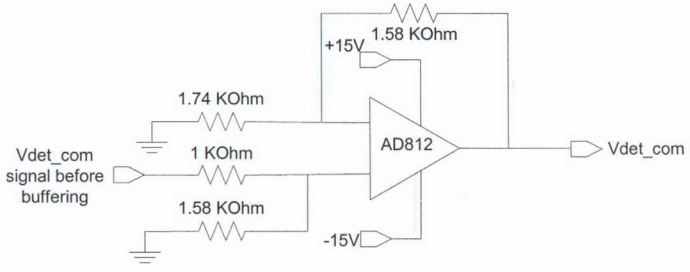


Figure 4.22 Buffer circuit to form Vdet_com.

4.3.7 Integration Time Control and Temperature Data Monitoring

The integration time of the ROIC can only be controlled through a potentiometer on the front-end electronics board in a manner similar to that for gain and offset control. The integration time can be varied from 100 μs to 6 ms which is a sufficiently large range for a typical cooled LWIR photon detector.

The temperature of the FPA in an infrared imaging system should be monitored. Since responsivity of the detectors may be affected by the temperature, predefined algorithms may be utilized using look-up tables to obtain better performances.

The temperature sensor on the ROIC outputs 0.7V at 300K and 1.1V at 77K. In order to monitor the FPA temperature, the related output of the ROIC is first buffered with CLC114. Then the buffered signal passes through an amplification circuit including AD812 to match to the input range of the serial ADC (AD7888), through which temperature signal is converted to a digital signal and monitored. The circuit used for this purpose is shown in Figure 4.23. Digitized temperature data is sent to PC through the RS232 port and displayed in the user interface program.

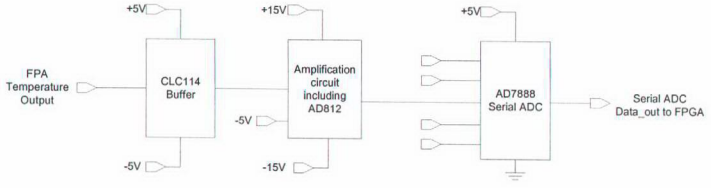


Figure 4.23: Temperature sensor output flow.

4.4 Digital Section

Digital section is the part where the digital control of the components, communication with PC, control of the ROIC, SRAM interface and transmitting of the digital ROIC data to VP_SC board takes place. Figure 4.24 shows the block diagram for digital section. The following sections describe the components and their functions, including FPGA, SRAM, FPGA configuration memory, RS232 transceiver, 4-digit seven segment display, and DIP switches.

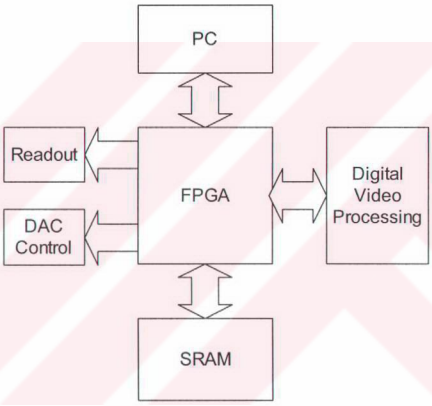


Figure 4.24: Block diagram for the digital section.

4.4.1 Field Programmable Gate Array (FPGA)

Main component of the digital part of the board is XC4036EX-HQ304 [21] FPGA from Xilinx. FPGA devices feature a gate-array-like architecture, with a matrix of logic cells surrounded by a periphery of I/O cells. Segments of metal interconnects can be linked in an arbitrary manner by programmable switches to form the desired signal nets between the cells.

Since many functions are implemented on the board and all should work at the same time (not sequentially), FPGA covers the requirement. Faster design and verification, ease of design change, in-system programmability, and high number of digital I /Os are among the other advantages of using an FPGA.

Different parts of the front-end electronics board require the FPGA design to follow a top-down approach; therefore FPGA has been divided into 4 functional blocks. Figure 4.25 shows these blocks.

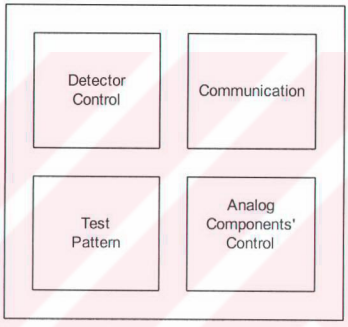


Figure 4.25: Blocks of FPGA.

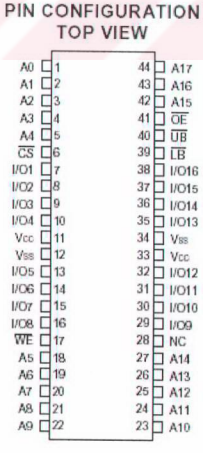
The FPGA has 4 functional blocks, which are detector control, communication, video control and test pattern blocks.

- Detector Control block produces the ROIC control word and directly passes other control signals coming from the VP_SC board,
- Communication block provides serial communication with PC. RS232 communication is accomplished in this block. Serial communication with the VP_SC board is also implemented in this block.
- Video Control block is the block where digital data coming from ADCs are multiplexed and sent to the VP_SC board,
- Test Pattern block produces test patterns that will be given to the monitor. Two of the test patterns are generated in the FPGA and one comes from the PC. Internally generated test data are increased at every LSYNC rising_edge to form

a black-to-white view from top to bottom, and at every ADC_CLK rising edge to from a black-to-white view from left to right of the monitor. If the test data comes from PC through a control software, it is concatenated with 4 leading '0's to form a 12-bit data since serial data coming is 8 bits and output to VP_SC board requires 12 bits. Test data and ROIC data are sent to a 4:1 multiplexer to form the data to be sent to the VP_SC board. Select of the multiplexer is also controlled in this block.

4.4.2 SRAM

In the calibration mode, the incoming ROIC data is written to an SRAM consecutively and then is sent to PC for normalization coefficient calculation. The SRAM used on the board is EDI816256CA [22], 256Kx16 monolithic SRAM from White Electronics Design. For a better calibration, consecutive frame data may need to be taken. Start of the write operation is controlled by one of the dip-switches. Figure 4.26 gives the pin diagram and pin functions of the SRAM.



PIN DESCRIPTION	
A_{0-17}	Address Inputs
LB(I/O_{1-8})	Lower-Byte Control (I/O_{1-8})
UB(I/O_{9-16})	Upper-Byte Control (I/O_{9-16})
I/O_{1-16}	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
Vcc	5V Power
Vss	Ground
NC	No Connection

Figure 4.26: Pin diagram and functions of EDI816256CA [22].

4.4.3 FPGA Configuration Memory

Configuration data for the FPGA is loaded from a nonvolatile memory (AT17C010 [23], from Atmel). It is an EE Programmable 524,288 x 1- and 1,048,576 x 1-bit Serial Memory designed to store configuration programs for FPGAs. It is compatible with the Xilinx XC3000, XC4000, XC5200, SPARTAN and Virtex FPGAs. The E^2PROM is produced with low-power CMOS process. Figure 4.27 shows the pinout of configuration memory.

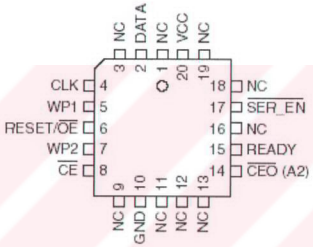
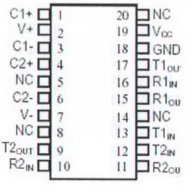


Figure 4.27 Pinout of configuration memory [23].

4.4.4 RS232 Transceiver

Communication of the board with PC is made possible through a RS232 transmitter/receiver, DS232A [24], a dual RS232 Transmitter/Receiver from Dallas Semiconductor. One channel of the chip is used for communication with PC. It operates from a single +5V supply, and has a high data rate of 250 kbits/sec. Figure 4.28 shows the pin assignment and description of DS232A.



V_{CC}	- +5-Volt Supply
GND	- Ground
V+	- Positive Supply Output
V-	- Negative Supply Output
$T1_{IN}$, $T2_{IN}$	- RS-232 Driver Inputs
$T1_{OUT}$, $T2_{OUT}$	- RS-232 Driver Outputs
$R1_{IN}$, $R2_{IN}$	- Receiver Inputs
$R1_{OUT}$, $R2_{OUT}$	- Receiver Outputs
C1+, C1-	- Capacitor 1 Connections
C2+, C2-	- Capacitor 2 Connections

Figure 4.28: Pin assignment and description of DS232A [24].

4.4.5 4-Digit Seven Segment Display

There is a 4-digit seven-segment display in the digital section of the board for FPA temperature monitoring. It can also be used for any system messages or warnings throughout the system operation.

4.4.6 DIP Switches

There are two 8-input dip-switches on the board for user control. Reset is one of the control signals that makes use of these switches. Test mode of the FPGA, freeze, normalization on/off, sending temperature/SRAM data to serial port, and start of the write operation to SRAM are also controlled through these switches.

4.5 PCB Design

As the printed circuit board of the system, a 12-layer board is designed following all the necessary design rules. The electronic circuit design entry process starts with schematic capture and continues with board layout and routing. Detailed layout is given in Appendix B.

Board power and signal layers are sequenced in an arrangement such that every signal layer is adjacent to a power or ground layer. The sequence is as signal1, ground, signal2, signal3, power1, ground, power2, signal4, ground, signal5, ground and signal6.

The seperation of analog and digital grounds is one of the most important points to take into consideration in mixed-signal boards. If analog and digital signals share the same ground path, one may face serious noise and crosstalk problems on the board. According to the suggested way of connecting analog and digital grounds given in the datasheet of ADC AD9220, the connection was made at one point just under the ADCs and DACs. Digital ground was placed under digital section of the

board and analog ground under the analog section. Power layers were composed by power fills.

Design rules given in the datasheets of the used components were also followed in detail. The decoupling capacitors are used on the power pins of each IC and located as close as possible to the active circuitry. Ceramic capacitors have a low inductance, so they can supply the pulses of current that the IC's require. Clock and control lines are kept as short as possible.

4.6 Normalization Algorithm

All IRFPAs, either scanning or staring, suffer from a fixed pattern noise due to the nonuniformities in the responsivity of the detector elements [25]. This fixed pattern noise significantly reduces the system performance and is important to be removed. The nonuniformity of the detector arrays can be partitioned into two parts, offset which is signal independent and gain which is signal dependent. The removal of these two terms provides enhanced images and improved performance of the system.

Mainly two non-uniformity correction algorithms are used on thermal imaging systems, one-point correction and two-point correction. In one-point offset correction, offset nonuniformities are removed whereas in one-point gain correction gain nonuniformities are eliminated. The detector response models for these one-point non-uniformity correction methods are

$$Y[i,j] = X[i,j] + b_{ij} \tag{4.2}$$

for one-point offset correction, and

$$Y[i,j] = X[i,j] \times a_{ij} \tag{4.3}$$

for one-point gain correction where

Y is the detector response,

X is the flux level,

a is the gain level and,

b is the offset level.

Another commonly used technique is the two-point correction method. The basis for this method is that all detector elements' responsivity should be the same to the equal amount of flux levels, and the detector response can be modeled as

$$Y[i,j] = a_{ij} \times X[i,j] + b_{ij} \tag{4.4}$$

The method requires the detectors to be exposed to two different flux levels. The responses of the detectors provide sufficient data to solve the above equation to calculate a and b. Successive frames of the scene may be taken to improve the accuracy of the calculated coefficients.

4.7 Summary

This chapter describes the design of the front-end electronics board. It explains the operation and interface with other blocks in the system. Then, the chapter focuses on the analog and digital sections of the board in detail, PCB design rules, and the normalization algorithm. The next chapter presents the simulation and testing of the front-end electronics board.

CHAPTER 5

SIMULATION AND TESTING OF THE FRONT-END ELECTRONICS BOARD

5.1 Introduction

This chapter describes the simulations and the tests done on the front-end electronics board. The simulations are held using Mentor Graphic's analog simulation tool, Accusim, and the tests are utilized with a mixed signal oscilloscope. Figure 5.1 shows the setup for the front-end electronics board testing.

Figure 5.1: The test-setup for the front-end electronics board.

5.2 Bias and Reference Generation

The results of the simulations on the voltage generation circuits demonstrated that the circuits work properly and provide constant voltages with required current levels. The test results are 5.49V for 5.5V, 1.59V for 1.6V, and 7.5V for 7.5V supply. Since the bias voltages for the ROIC have a margin of ±0.2 V, the slight differences do not cause any problem.

5.3 Analog Processing of ROIC Output

The processing of the ROIC output consists of buffering, offset correction, amplification, clipping, differential driving, and digitization.

5.3.1 Offset and Gain Setting

As explained in the previous chapter, the offset for the ROIC data is produced by a DAC, whose output is sent to an adder circuit to form the offset voltage that is used to make an offset corrected ROIC data. Offset voltage is required to change between 0 and –5V. The DAC is configured to give the output in the ±5V range, and the required voltage levels are obtained by voltage division. One output is voltage-divided to be in the range of ±2.5V to form the vskim signal, and -2.5V is added to the vskim voltage to make the offset voltage in the 0 to -5V range. Figure 5.2 shows the simulation graph for the offset voltage. The gain is applied directly from the output of the DAC and does not need any external circuitry.

The measurements indicate that the offset voltage changes in a range of 0.342V to –4.518V, which agrees with the simulation results. The ROIC data is in the 1.6 - 4.6V range. Therefore, if –3.1V offset is applied to the ROIC data with the offset correction circuit, the ROIC data varies between –1.5V and +1.5V. With the multiplicative factor of 1.67 in the offset addition circuit, the signal lies in the range of +2.5V and -2.5V to comply with the ADC's input range. Figure 5.3 shows the simulation for the offset corrected ROIC output. Table 5.1.a and Table 5.1.b give the

outputs of the offset correction circuit (calculated and measured values) for different offset voltages.

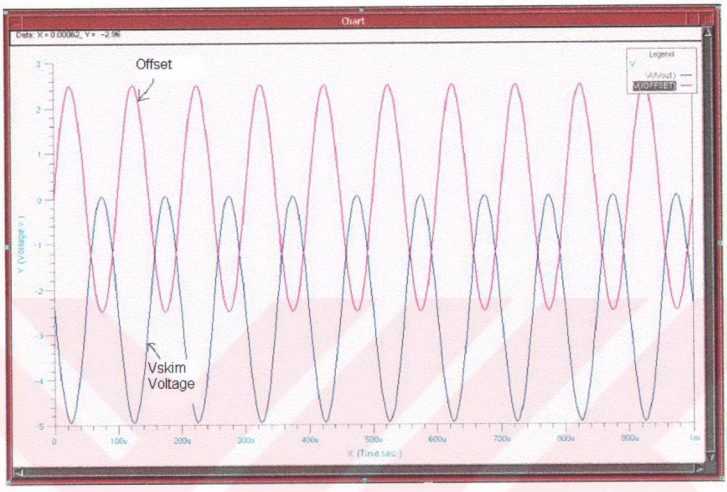


Figure 5.2: Simulation results for Offset vs. Vskim voltage.

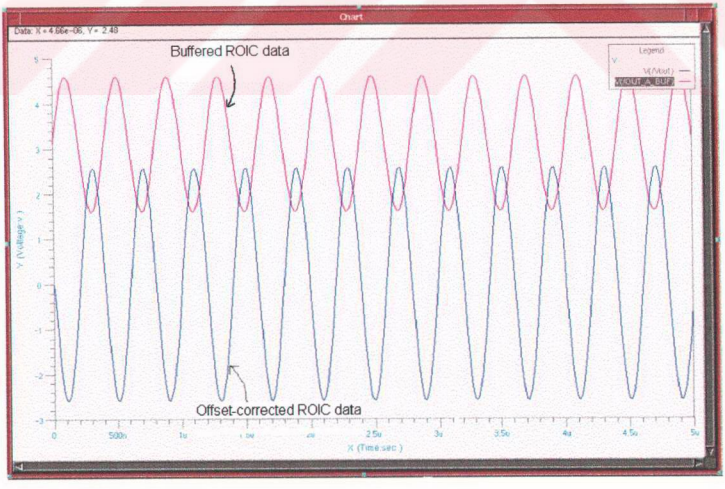


Figure 5.3: Simulation results for offset-corrected ROIC output.

Table 5.1.a: Offset correction circuit calculated and measured values for -3.8V offset.

Input	Offset	Calculated Signal	Measured Signal
1	-3,08	3,6192	3,58
1,6	-3,08	2,5752	2,5568
2	-3,08	1,8792	1,86
3	-3,08	0,1392	0,142
4	-3,08	-1,6008	-1,568
4,6	-3,08	-2,6448	-2,6

Table 5.1.b: Offset correction circuit calculated and measured values for -2.03V offset.

Input	Offset	Calculated Signal	Measured Signal
1	-2,03	1,7922	1,78
1,6	-2,03	0,7482	0,756
2	-2,03	0,0522	0,067
3	-2,03	-1,6878	-1,65
4	-2,03	-3,4278	-3,38
4,6	-2,03	-4,4718	-3,83

In Tables 5.2.a, 5.2.b, and 5.2.c, the measured and calculated values for different gain-corrected signals are given. Input, offset, and gain voltages are changed to check the correct operation of the offset and gain circuits.

Table 5.2.a: Gain applied ROIC data for -3.8V offset and -0.397V gain voltages.

Input	Offset	AD812 Calc.	AD812 Meas.	Gain Input	Gain Input Calculated	Gain Input Measured	Gain Output Calculated	Gain Output Measured
1	-3,08	3,6192	3,58	-0,397	1,44768	1,437	1,05970176	1,055
1,6	-3,08	2,5752	2,5568	-0,397	1,03008	1,025	0,75401856	0,755
2	-3,08	1,8792	1,86	-0,397	0,75168	0,747	0,55022976	0,552
3	-3,08	0,1392	0,142	-0,397	0,05568	0,057	0,04075776	0,04435
4	-3,08	-1,6008	-1,568	-0,397	-0,64032	-0,6285	-0,46871424	-0,461
4,6	-3,08	-2,6448	-2,6	-0,397	-1,05792	-1,04	-0,77439744	-0,765

Table 5.2.b: Gain applied ROIC data for -3.8V offset and -0.31V gain voltages.

Input	Offset	AD812 Calc.	AD812 Meas.	Gain Input	Gain Input Calculated	Gain Input Measured	Gain Output Calculated	Gain Output Measured
1	-3,08	3,6192	3,58	-0,31	1,44768	1,44	1,46070912	1,4458
1,6	-3,08	2,5752	2,56	-0,31	1,03008	1,036	1,03935072	1,035
2	-3,08	1,8792	1,876	-0,31	0,75168	0,751	0,75844512	0,759
3	-3,08	0,1392	0,151	-0,31	0,05568	0,06	0,05618112	0,062
4	-3,08	-1,6008	-1,57	-0,31	-0,64032	-0,63	-0,64608288	-0,6355
4,6	-3,08	-2,6448	-2,6	-0,31	-1,05792	-1,044	-1,06744128	-1,049

Table 5.2.c: Gain applied ROIC data for -2.03V offset and -0.31V gain voltages.

Input	Offset	AD812 Calc.	AD812 Meas.	Gain Input	Gain Input Calculated	Gain Input Measured	Gain Output Calculated	Gain Output Measured
1	-2,03	1,7922	1,78	-0,31	0,71688	0,716	0,72333192	0,723
1,6	-2,03	0,7482	0,756	-0,31	0,29928	0,303	0,30197352	0,307
2	-2,03	0,0522	0,067	-0,31	0,02088	0,027	0,02106792	0,028
3	-2,03	-1,6878	-1,65	-0,31	-0,67512	-0,664	-0,68119608	-0,669
4	-2,03	-3,4278	-3,38	-0,31	-1,37112	-1,35	-1,38346008	-1,36
4,6	-2,03	-4,4718	-3,83	-0,31	-1,78872	-1,53	-1,80481848	-1,54

5.3.2 Clamping

The amplified signal is then sent to clamping amplifier that is set to clip the input ROIC data to +2.5V if it is higher than +2.5V and to –2.5V if it is lower than –2.5V. However, the non-linearity of the chip causes some distortions and the input signal is changed slightly, as shown in Table 5.3. The polarity is reversed to obtain the original polarity since offset correction stage inverts the signal. Graphs of the output versus input clarify the non-linearity better. Figure 5.4 shows the slight non-linearity introduced by the chip.

Table 5.3: Clamping amplifier input and output data.

Clamping Input	Clamping output
1,4458	-1,4345
1,035	-1,027
0,755	-0,749
0,552	-0,547
0,307	-0,304
0,028	-0,027
-0,461	0,458
-0,6355	0,631
-1,049	1,043
-1,36	1,348
-1,54	1,53

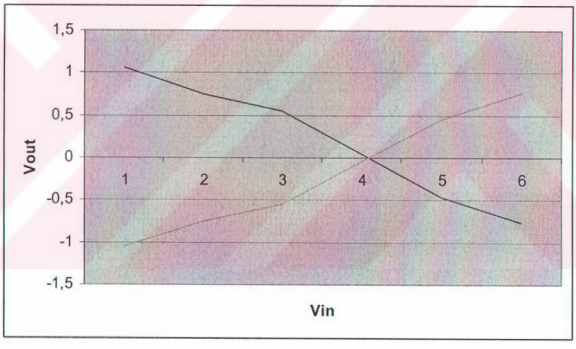


Figure 5.4: Graph indicating the slight non-linearity.

5.3.3 Digitization

The last stage in the analog processing of ROIC data is the digitization. The output of the clamping amplifier is sent to AD8138 to drive the ADC differentially. Table 5.4 shows calculated and measured ADC output data and the difference between them under various input data.

Table 5.4: ADC inputs, calculated and measured outputs and difference.

ADC Input	ADC Dig Out	Calculated	Difference
-1,4345	1101101011	1101101000	11
-1,027	10010110111	10010110110	1
-0,749	10110011011	10110011010	1
-0,547	11001000000	11000111111	1
-0,304	11100000110	11100000110	0
-0,027	11111101001	11111101001	0
0,458	100101110111	100101110111	0
0,631	101000000011	101000000100	1
1,043	101101010100	101101010110	10
1,348	110001001110	110001001111	1
1,53	110011100000	110011100100	100

5.4 Temperature Data Monitoring

The temperature sensor outputs 0.7V at 300K and 1.1V at 77K. Hence, the sensor output should be amplified to be in the range of 0 - 5V in order to comply with serial ADC's input range. The simulation of the amplification circuit shows that the amplified signal is between 0.8V and 4.85V.

The outputs are imitated with a power supply output between 0.7V and 1.1V. The serial ADC digitized outputs for these voltages are read and the serial data for PC to monitor temperature data is formed. In the setup, ROIC being connected to the board, the temperature shown on the user interface is between ~70K and ~290K, which is reasonable due to the considerable error margin of the ROIC temperature sensor output.

5.5 HPVEE Test Pattern Generation

Test pattern for ADC data is produced by another HPVEE program. A decimal input varying between 0 and 255 is sent to the front-end electronics board

where it is concatenated with 4 '0's to form 12 bit adc data and then sent to the VP_SC board for monitoring.

5.6 Summary

This chapter describes the simulation and testing of the front-end electronics board. Simulations and testing of the individual blocks have been implemented. Measurements have been taken to verify the correct functionality of the simulated blocks. Next chapter will present the integration of the front-end electronics board with the VP_SC board to form the prototype thermal imager and testing of the system.

CHAPTER 6

SYSTEM INTEGRATION AND TESTING

6.1 Introduction

This chapter describes the integration of the front-end electronics board with the video processing and system control board, and system testing. Figure 6.1 shows the imaging system test setup that includes a detector dewar assembly (DDA), front-end electronics and user interface board, VP_SC board, two power supplies, a PC, and an analog monitor.

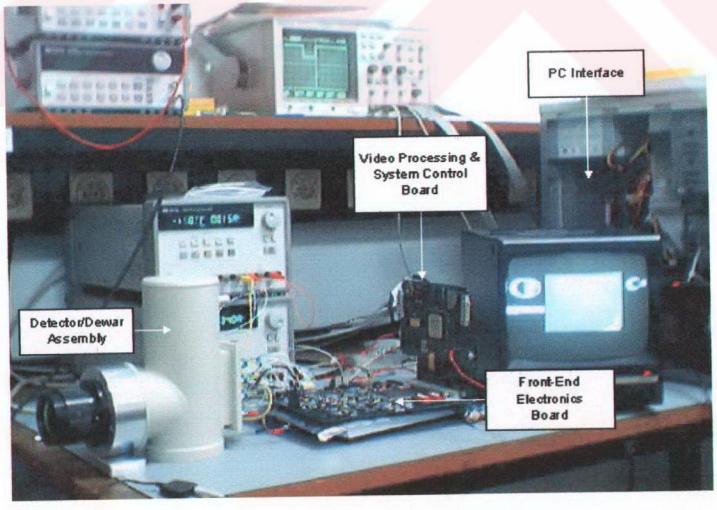


Figure 6.1: Imaging system test setup.

In this system, the PC (through the HPVEE user interface program) is used to produce the serial control word for detector readout, to input offset and gain settings for ROIC data, to monitor readout temperature, to program flash memory on the video processing and system control board for normalization and symbology insertion, and to get frame data to be used for normalization coefficient calculation. A MATLAB program is used to calculate and simulate the normalization coefficients. The monitor displays the processed infrared image.

6.2 Detector Dewar Assembly

The detector dewar assembly consists of a pour filled liquid nitrogen dewar, 50mm f2/3 3-5 μm germanium lens and sensor interface connections. Figure 6.2 shows a picture of the DDA. DDA is configured for ISC9806 ROIC packaged in an 84 pin LCC. DDA uses liquid nitrogen as cryogen. The IRFPA is placed on 84 pin LCC and clamped to the cold finger using indium foil in between the ceramic carrier and the cold finger.

Figure 6.2: Detector Dewar Assembly.

6.3 Video Processing and System Control Board

Video processing and system control board is the board where processing of digitized detector data and timing of the system operations are performed. After the

128x128 digital detector array data coming from the front-end electronics board is processed, analog video in CCIR format is generated to display on a standard monitor. Figure 6.3 shows the interfacing of the VP_SC board with the other blocks.

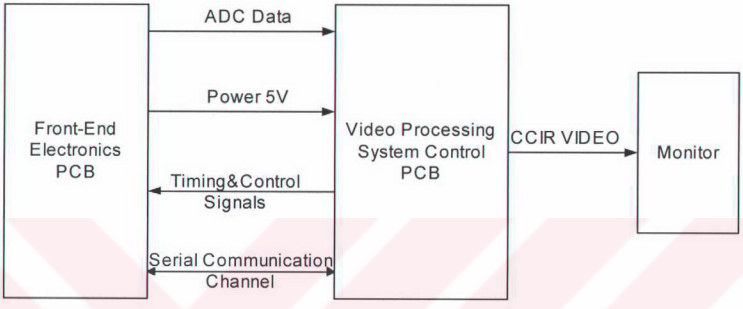


Figure 6.3: Interfacing of the VP_SC board with the other blocks.

Control of ROIC and the front-end electronics board requires some control signals generated. Frame and line synchronization signals, readout and analog to digital conversion clock signals are produced by the VP_SC board.

There is a serial communication channel between the front-end electronics and VP_SC board. Front-end electronics board provides the user to configure the system by means of either by HPVEE user interface program or potentiometers and switches on the board. Offset and gain corrections commands sent from the front-end electronics board are used to normalize the raw digital data.

Normalization coefficients calculated by the front-end electronics board are written to the on board nonvolatile flash memory. Real-time normalization can not be accomplished due to the long access times of flash memories. Therefore, the coefficients in the flash memory are written to SRAM, which has a shorter access time, at power-up. During system operation, the coefficients are read from the SRAM.

After normalization stage, the VP_SC board stores the video data in buffer memories in an interleaved manner, i.e. while the flowing video data is written to one of SRAMs, previous frame data is read to form the data to be sent to video digital-to-analog converter(VDAC). The previous frame data is sent to VDAC to produce analog video in CCIR format. The analog data is buffered to enable transmission to long distances with small distortions before it is sent out of the board through a 75 ohm BNC cable.

6.4 Monitoring Test and ROIC Data

Three types of test data are possible to monitor with the system, one set of test data increasing at every LSYNC rising edge, another set of test data increasing at every ADC_CLK rising edge, and one set of test data sent through the PC by the HPVEE test pattern generator program. The selection of the data to be monitored is done through the dip-switches on the front-end electronics board.

First type of the test data is increased at every line synchronization signal rising edge, and turns from black to white in the downward direction. Figure 6.4 shows a view of this type of test data.

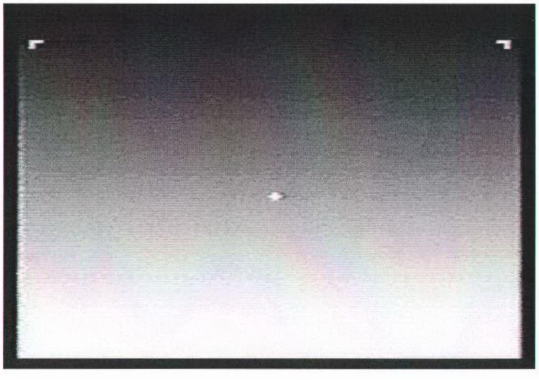


Figure 6.4: Test data increasing at every LSYNC rising edge.

Second type of test data is assigned zero at every LSYNC rising edge and increased at every ADC_CLK rising edge so that it turns from black to white from left to the right end of the monitor. Figure 6.5 shows a view for this type of test data.

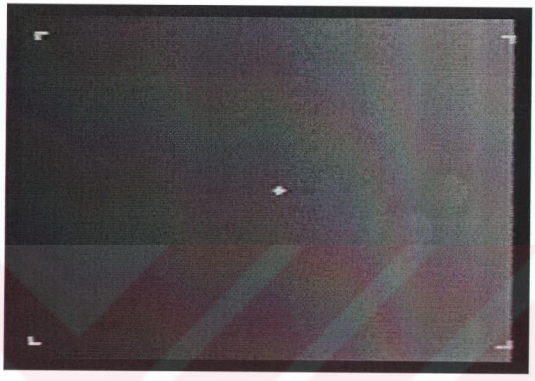


Figure 6.5: Test data increasing at every ADC_CLK rising edge.

The third type of test data is sent from PC by the HPVEE test pattern generator program. The value of the test data can be assigned any value between hexadecimal 00 and FF. The serial data coming from PC is 8 bits and the ADC data to be sent to VP_SC board is 12 bits, therefore "0000" is concatenated to the end of PC data before being sent. Figure 6.6 shows a view for this type of test data (hex 55).

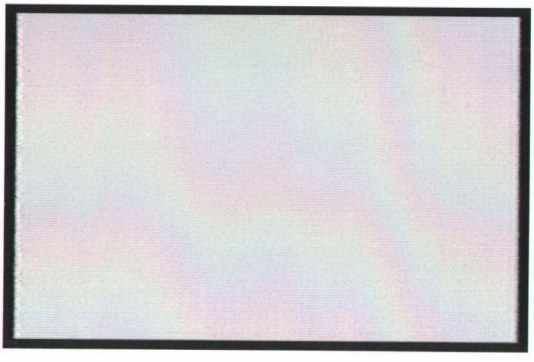


Figure 6.6: Test data sent from PC (hex 55)

After the three types of test data are formed and input to the system for testing purposes, the gain and offset settings of the system are tested and shown to work as required. Analog bias and reference generation, digital timing and control signals, and control of the ROIC through the serial control register are also checked.

After preliminary testing, the system is assembled with the DDA to obtain real time infrared images. The IRFPA used for the tests is a 128x128 InSb array on Si substrate integrated with Indigo Systems' ISC9806 ROIC. Due to the large lattice mismatch (19 %) between InSb and Si, the detectors yield high dark currents, which makes the thermal imaging of room temperature objects impossible. While the images captured with this IRFPA are not of high quality, hot objects such as candle light can be imaged to prove the system functionality. At first, raw images without non-uniformity correction were obtained. Figure 6.7 shows a snapshot of an infrared image taken from the IRFPA, while the array is looking at 300K background. As seen from this figure, the array is highly nonuniform.

Figure 6.7: Raw infrared image taken from IRFPA, while the array is looking at 300K background.

6.5 Normalization Coefficient Calculation

Acquired infrared images require nonuniformity correction for an enhanced view. Non-uniformity correction can be utilized as offset and gain correction as described in Chapter V. Offset and gain correction involves the calculation of the related coefficients.

SRAM on the front-end electronics board is used to acquire frame data for normalization. A dip-switch controls start of the write operation. At the start of the FSYNC signal, the coming scene data is written to the SRAM, and then sent to the PC. The serial data coming through the RS232 port is stored into a text file by the PC. The successive frame data is then used to calculate the offset and gain coefficients by a MATLAB program. The calculated coefficients are then written to another text file, which is sent to the VP_SC board through the front-end electronics board, and written to the flash memory on the VP_SC board. Figure 6.8 shows an uncorrected frame data of the InSb/Si array with the FPA looking at candle light, viewed by MATLAB to check the above communication. MATLAB codes written for the calculation of the offset and gain coefficients are given in Appendix C.

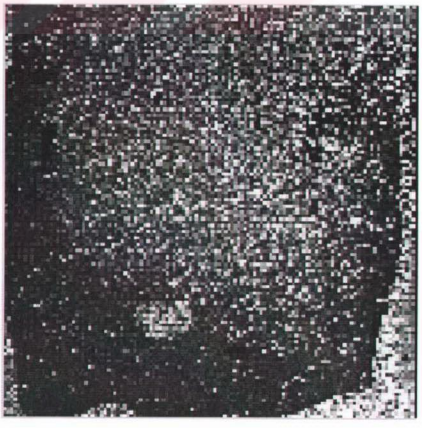


Figure 6.8: View of taken frame data in MATLAB with the FPA looking at candle light.

Nonuniformity correction can be implemented as one-point offset correction, one-point gain correction, or two-point offset and gain correction. One frame data is used for one-point nonuniformity correction calculation, whereas two frame data while the FPA is exposed to two different temperatures are required for two-point correction.

One-point offset correction assumes the detector response can be modeled as $y = x + b$. The offset coefficients are calculated with a reference target at 300K. The calculated offset coefficients are then subtracted from the frame data when the FPA is looking at candle light to form the offset-corrected frame data. Figure 6.9 illustrates the offset corrected frame data viewed in MATLAB with the FPA looking at candle light.

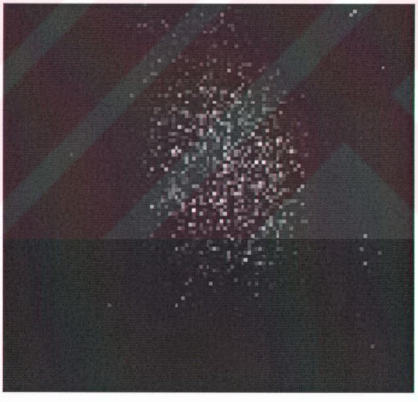


Figure 6.9: Offset-corrected frame data viewed in MATLAB with the FPA looking at candle light.

In one-point gain correction, the detector response is modeled as $y = a * x$. The gain coefficients are calculated by exposing all the pixels to the same flux level. A hot plate is used as a reference target for this purpose. The frame average is calculated using the image data taken with the reference target. Then, the gain

coefficient for each pixel is calculated by dividing the frame average to that pixel's response while it is exposed to the reference target. If the calculated gain coefficient for a pixel is larger than a selected threshold, then that pixel is assumed to be a bad pixel, and its gain coefficient is written with the 13^{th} bit being '1' to indicate that the pixel should be replaced by a neighboring working pixel. If the calculated gain coefficient is smaller than the above threshold and larger than a lower threshold, the largest possible gain is applied to that pixel. Otherwise, the calculated gain coefficient is used for gain correction. To obtain the corrected image, each pixel response is multiplied by the corresponding gain coefficient. Figure 6.10 shows the gain-corrected frame data viewed in MATLAB with the FPA looking at candle light.

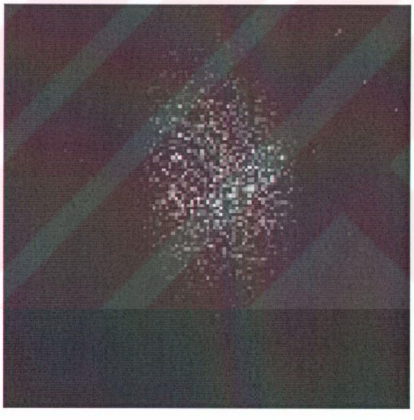


Figure 6.10: Gain-corrected frame data viewed in MATLAB with the FPA looking at candle light.

One-point gain correction provides a higher quality image when compared with the one-point offset correction, since the application of a multiplicative factor can produce larger changes in the response of a pixel than an additive factor. However, one-point correction may not achieve enough enhancement in the frame data, and the application of both offset and gain coefficients can be necessary.

Two-point correction includes both the offset and gain corrections, where the detector is modeled as $y = ax + b$. Frame data while the FPA is exposed to two different temperatures is required, since there are two unknowns, a, the gain coefficient, and b, the offset coefficient. One frame data is acquired while the pixels are looking at a reference target at 300K, and the offset coefficients are calculated. Then, another frame data is acquired with the FPA exposed to a high temperature reference target. The frame average is calculated using the image data at that temperature. The gain coefficient for each pixel is calculated using $y = ax + b$, where y is the frame average, b is the assigned offset coefficient, and x is that pixel's response. The calculated offset and gain corrections are then used to enhance the frame data. Figure 6.11 shows the offset and gain corrected frame data viewed in MATLAB with the FPA looking at candle light. Note that two-point correction provides better quality image when compared with the one-point offset or one-point gain correction.

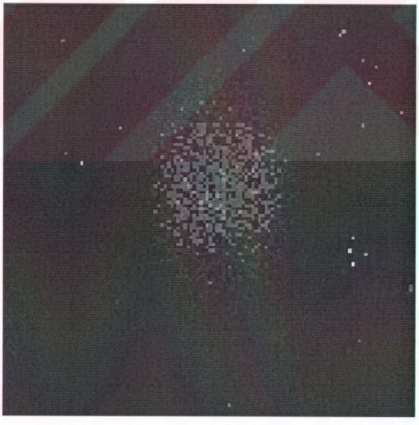


Figure 6.11: Offset and gain corrected frame data viewed in MATLAB with the FPA looking at candle light.

After the offset and gain coefficients are calculated and simulated with MATLAB, the coefficients are sent to the VP_SC board through the front-end

electronics board, and written to the flash memory. The coefficients are then used to correct real time thermal images. Figures 6.12 and 6.13 show two-point correction disabled and enabled thermal images with the FPA looking at candle light. A comparison of these images show substantial improvement in image quality and successful operation of the system.

Figure 6.12: Two-point correction disabled thermal image with the FPA looking at candle light.

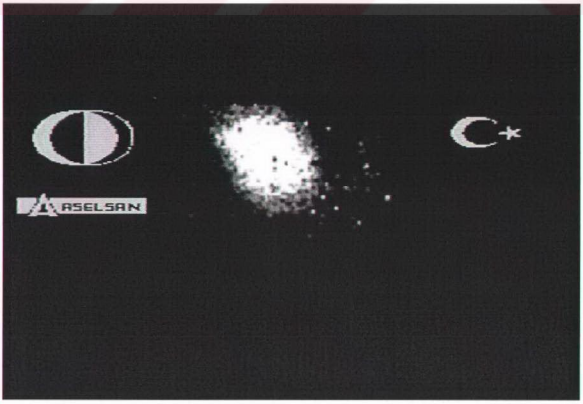


Figure 6.13: Two-point correction enabled thermal image with the FPA looking at candle light.

6.6 Summary

This chapter describes the integration and testing of the front-end electronics board with the other units in the system to obtain real time thermal imaging. Detector dewar assembly and video processing and system control board are introduced. Image capture with test data application and real time thermal imaging including nonuniformity correction are explained. Conclusions and future work will be presented in the next chapter

CHAPTER 7

CONCLUSION AND FUTURE WORK

The objective of this thesis work is to design and build a front-end electronics board which is integrated with a video processing and system control board to compose an infrared imaging system, which is the first prototype national thermal imaging system for staring FPAs. The study can be divided into four main subsections; i) design of the front-end electronics system, ii) implementation of the design iii) testing of the board iv) integration of the board with video processing and system control board to acquire infrared image and system testing.

The board has successfully been implemented and tested. The performance of the board was checked from the readout connector input to the digital outputs. Acquired frame data was used to calculate non-uniformity correction coefficients for a highly nonuniform InSb detector array on Si substrate and substantial improvement in the image quality was achieved.

The aim to design a system limited by detector performance was successfully realized. In the worst conditions, the noise level of the board (650 e^-) was comparable with the ROIC output noise (550 e^-) and several times smaller than the noise of a typical cooled LWIR detector (4000 e^-). In typical working conditions, the noise level of the system is dominated by the detector and ROIC, noise levels being orders of magnitude larger than the board (50 e^-).

The imaging system works at 25 Hz frame rate, and the maximum frame rate is 550 Hz in the 4 output mode of the ROIC for 128x128 FPA. The maximum supported FPA resolution is 320x256 with 25 Hz frame rate.

As a course of future study, the 10 MSPS 12-bit analog-to-digital converter can be replaced by a 14-bit ADC to improve the dynamic range. Selection of lower noise level and faster ICs will also add improvements in the front-end electronics board.

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APPENDIX A

HPVEE USER INTERFACE

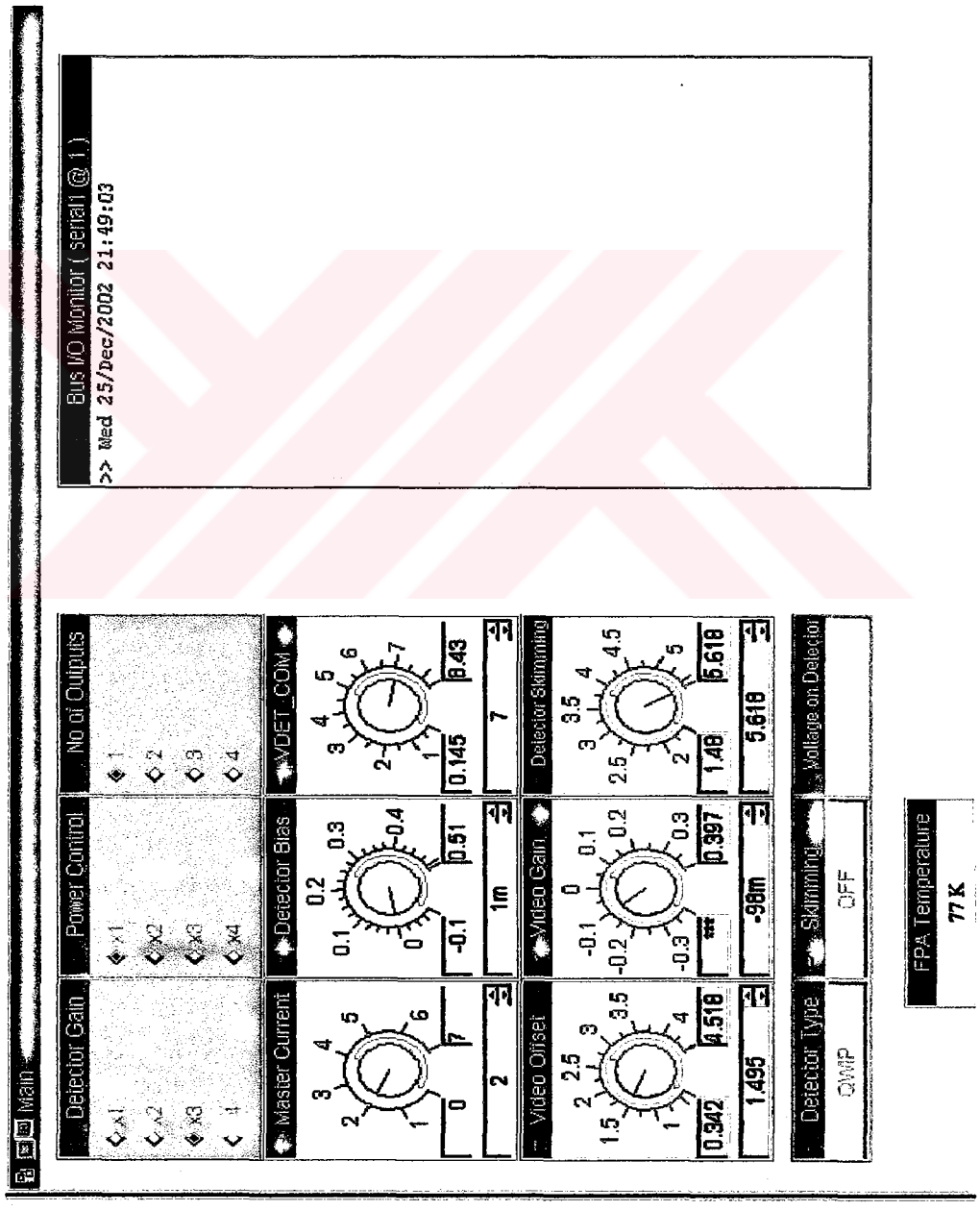

Figure A: HPVEE User Interface.

APPENDIX B

PCB LAYOUT OF FRONT-END ELECTRONICS

The 12-layer PCB is designed using Mentor Graphic's Layout tool. 6 layers are used for signal routing, 2 layers are used for power, and 4 layers are used for ground. The following sections show some of the layers of the PCB including component layer, solder layer, power layer, and ground layer.

B1. Component Layer

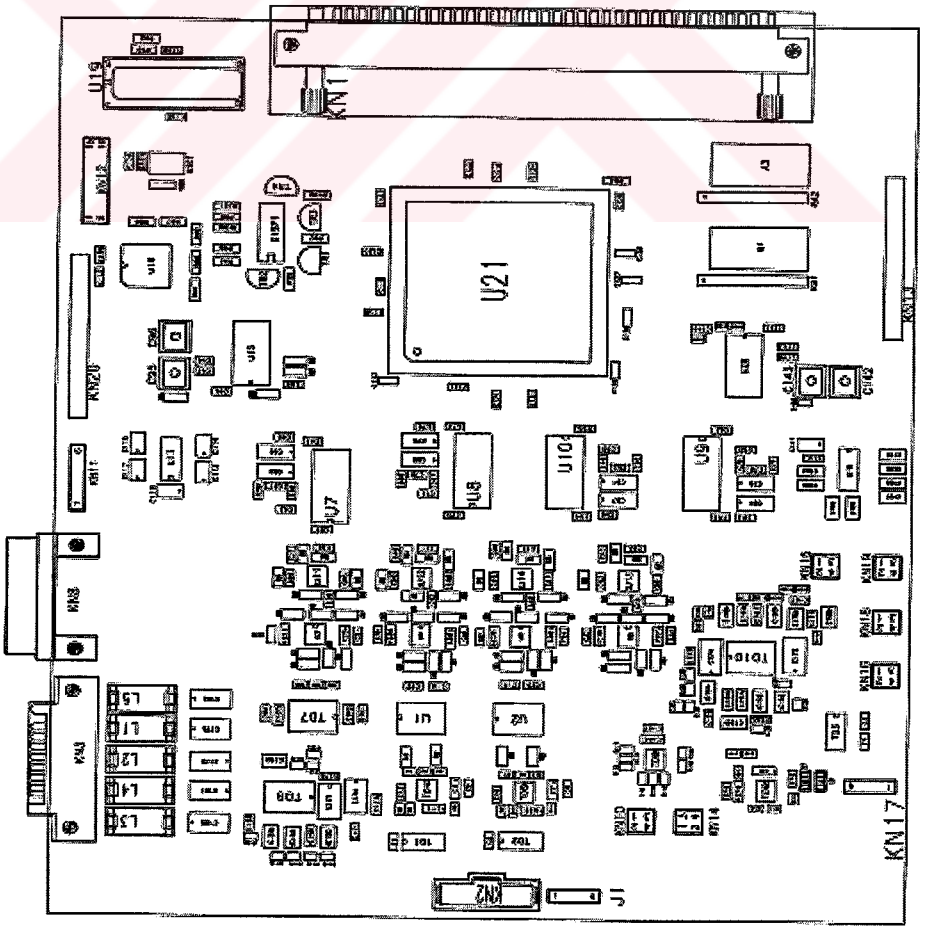

Figure B1: Component Layer.

B2. Solder Layer

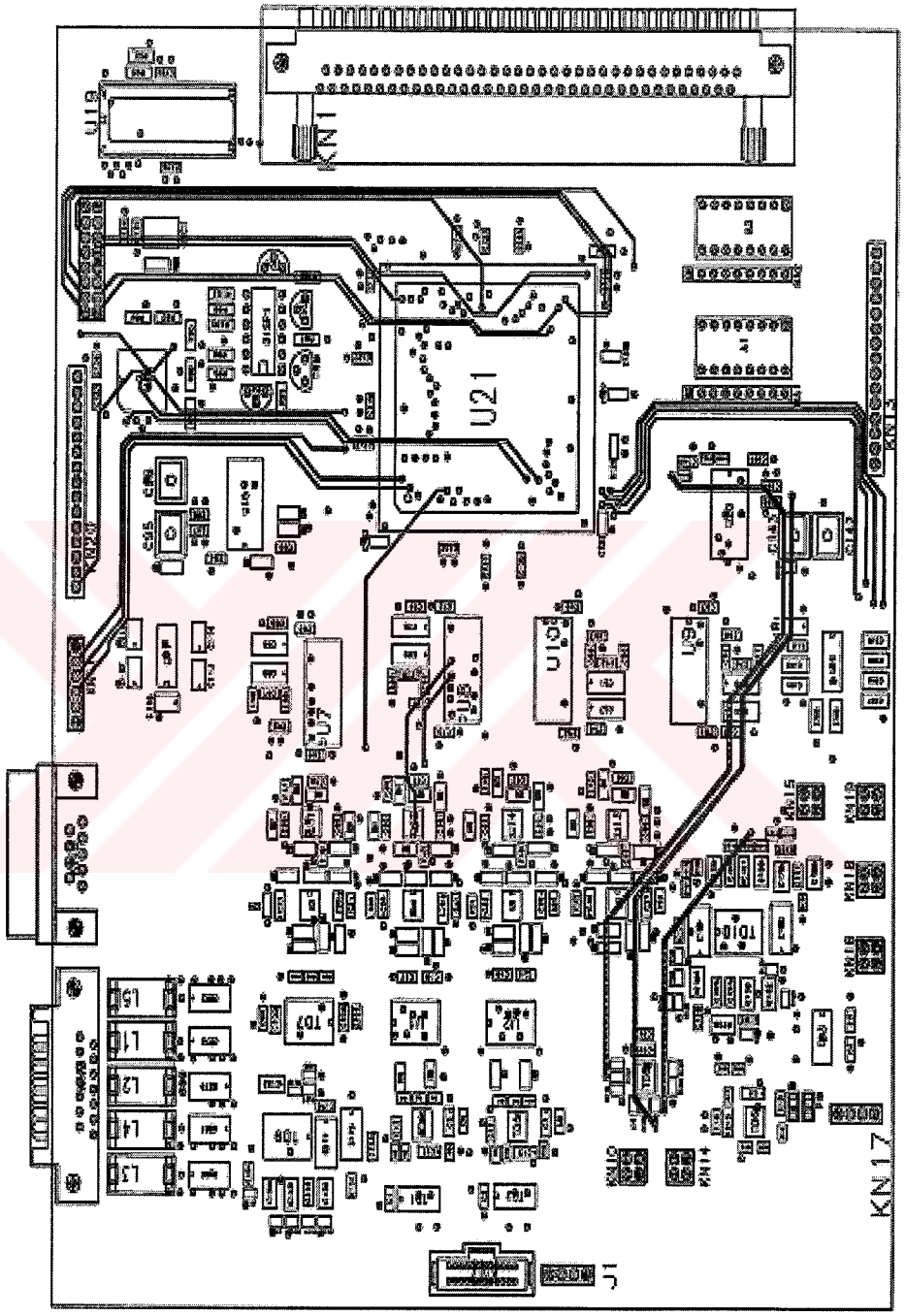

Figure B2: Solder Layer.

B3. Power Layer

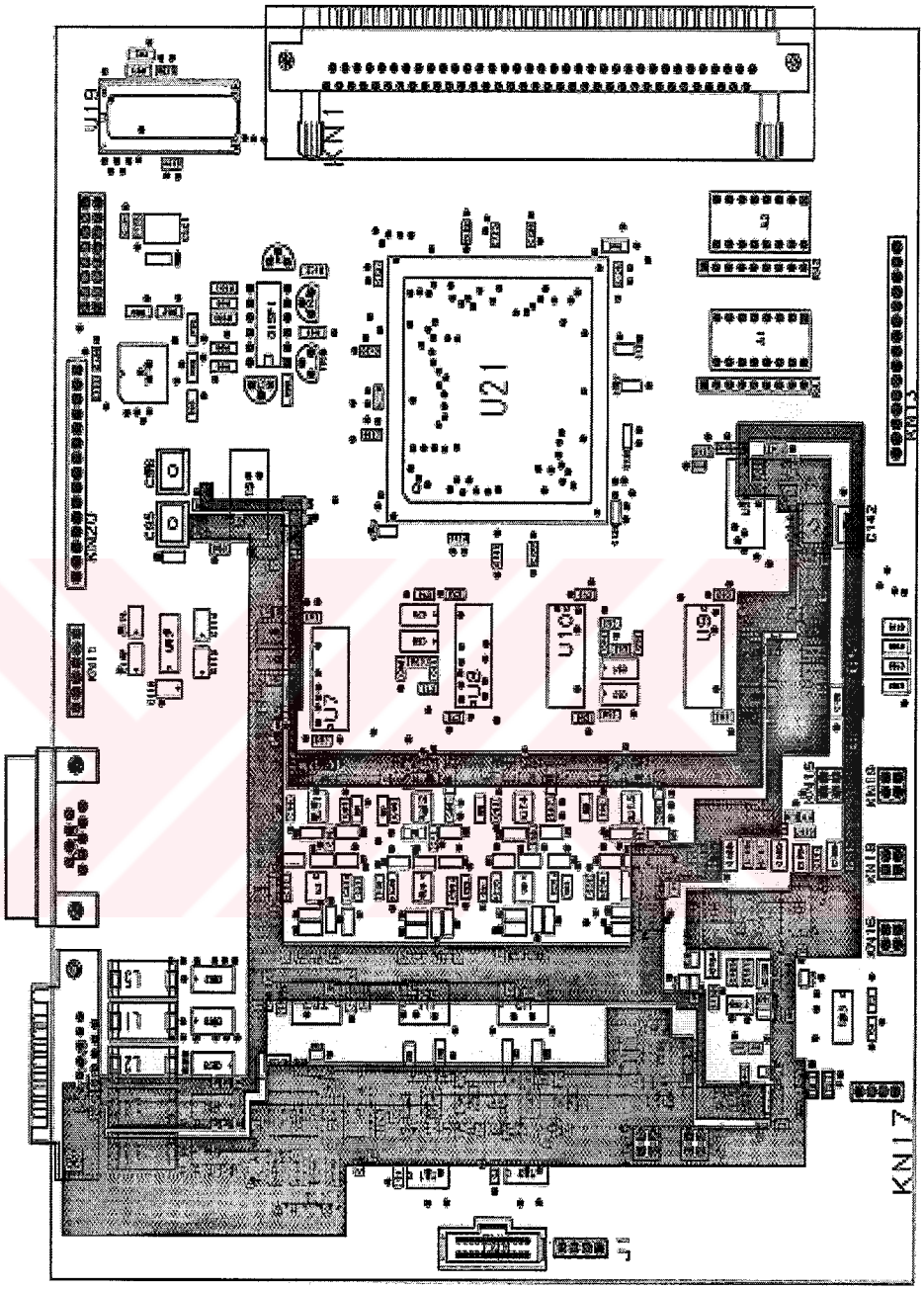

Figure B3: Power Layer.

B4. Ground Layer

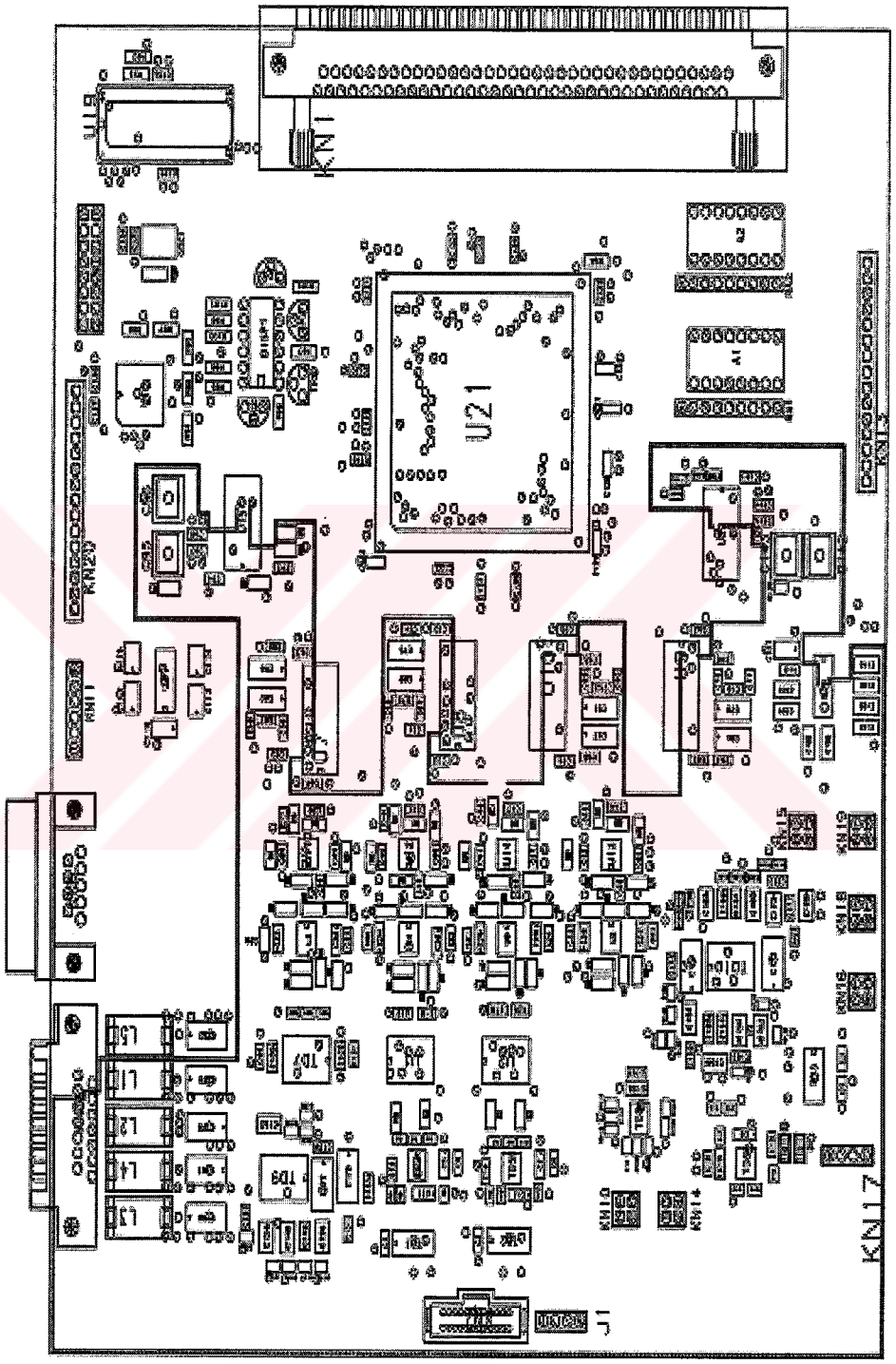

Figure B4: Ground Layer.

APPENDIX C

MATLAB CODES FOR NORMALIZATION COEFFICIENT CALCULATION

```
clear all;
close all;
number_frame=input('enter number of frames:');
pixelsperframe=input('enter number of pixels in each frame:');
frame1=load('frame1.txt');
[row1 coloum1]=size(frame1);
if (rem(row1,pixelsperframe)~=0)|(coloum1~=1)
   input('frame1.txt file does not match');
end

offset=load('frame2.txt');
[row2 coloum2]=size(offset);
if (rem(row2,pixelsperframe)~=0)|(coloum2~=1)
   input('frame2.txt file does not match');
end
if (row1~=row2)|(coloum1~=coloum2)
   input('files do not match');
end

% find the average of frame1 and write it a matrix of size (pixelsperframe X 1)

data1=zeros(pixelsperframe,1);
for i=1:row1
```

```
    if rem(i,pixelsperframe)==0
        data1(pixelsperframe)=data1(pixelsperframe)+frame1(i);
    else
        data1(rem(i,pixelsperframe))=data1(rem(i,pixelsperframe))+frame1(i);
    end
end
data1=data1/number_frame;
pure_gain=abs(data1-offset);
%pure gain image
a=1;
b=1;
clear pure_image;
for a=1:128
    for b=1:128
        pure_image(a,b)=pure_gain(((a-1)*128)+b);
    end
end
figure;
imshow(pure_image, [0 4096]);
title('pure image');

a=1;
b=1;
sum1=0;
count=0;
for a=1:128
  for b=1:128
      sum1=sum1 + pure_gain(((a-1)*128)+b);
      count=count+1;
  end
end
avg_data1=sum1/count;
```

```
difference=abs(data1-data2);
data1=data1+0.00000000010101;
difference=difference+0.00000000010101;

%calculate gain
pure_gain=pure_gain + 0.00000000010101;
gain=avg_data1./pure_gain;
display('gain calculated');

% calculate offset
offset=((avg_data2*data1-avg_data1*data2)./difference)./gain;
display('offset calculated');

for i=1:16384
  if gain(i)>4
    gain(i)=4;
  end;
end;

fid= fopen('frame2.txt');
y=fscanf(fid,'%f',[1,16384]);
cl=1;
rw=1;
cr=1;
clear const_image
clear b
clear c
for cl=1:128
  for rw=1:128
    const_image(cl,rw)=y(1,cr);
    cr=cr+1;
```

```
  end
end
 fid= fopen('datain.txt');
y=fscanf(fid,'%f',[1,16384]);
cl=1;
rw=1;
cr=1;
clear input_image
clear b
clear c
for cl=1:128
  for rw=1:128
    input_image(cl,rw)=y(1,cr);
    cr=cr+1;
  end
end

figure;
imshow(input_image, [0 4096]);
title('input image');

cl=1;
rw=1;
cr=1;
clear data1_out
clear b
clear c
for cl=1:128
  for rw=1:128
    data1_out(cl,rw)=data1((cl-1)*128+rw);
    cr=cr+1;
  end
```

```
end

figure;
imshow(data1_out, [0 4096]);
title('data1');

a=1;
b=1;
for a=1:128
  for b=1:128
    gain_corrimage(a,b)=gain(((a-1)*128)+b)  *  (((const_image(a,b)))  -  offset(((a-
1)*128)+b));
   end
end

a=1;
b=1;
for a=1:128
  for b=1:128
    if gain(((a-1)*128)+b)>6 & b~=1 & a~=1
      gain_corrimage3(a,b)=gain_corrimage3(a,b-1);
    elseif gain(((a-1)*128)+b)>4
      gain_corrimage3(a,b)=4 * (((input_image(a,b))) - offset(((a-1)*128)+b));
    else
     gain_corrimage3(a,b)=gain(((a-1)*128)+b)*(((input_image(a,b)))-offset(((a-
1)*128)+b));
     end
  end
end


figure;
```

```
imshow(gain_corrimage, [0 4096]);%, [0 256]);
title('corrected cons image');
figure;
imshow(gain_corrimage3, [0 4096]);%, [0 256]);
title('corrected image');


ab=1;
cd=1;
for ab=1:128
  for cd=1:128
    if (gain_corrimage(ab,cd)< 800)
      pix_sub_info(ab,cd)= 0;
    else
      pix_sub_info(ab,cd)= 255;
    end
  end
end

figure;
imshow(pix_sub_info, [0 255]);%, [0 256]);
title('pix_sub_info');

i=2;
j=2;
gain_corrimage_sub(1,:)=255;
gain_corrimage_sub(128,:)=255;
gain_corrimage_sub(:,1)=255;
gain_corrimage_sub(:,128)=255;
for i=2:127
  for j=2:127
```

```
    temp=gain_corrimage(i-1,j-1)+gain_corrimage(i-1,j)+gain_corrimage(i-
1,j+1)+gain_corrimage(i,j-
1)+gain_corrimage(i,j)+gain_corrimage(i,j+1)+gain_corrimage(i+1,j-
1)+gain_corrimage(i+1,j)+gain_corrimage(i+1,j+1);
    temp=temp/8;
    if (gain_corrimage(i,j)< temp - 300) | (gain_corrimage(i,j)> temp + 300)
      gain_corrimage_sub(i,j)=0;
    else
      %gain_corrimage_sub(i,j)=gain(((i-1)*128)+j) * (input_image(i,j) + offset(((i-
1)*128)+j));
      gain_corrimage_sub(i,j)=255;
    end
  end
end

offset=offset.*(-1);
offset_bin=dec2bin( mod( (offset), 2^16 ), 16 );
fid=fopen('noc.txt','w');
for i=1:16384
  for j=1:16
    fprintf(fid,'%c',offset_bin(i,j));
  end
  fprintf(fid,'\n');
end
fclose(fid);

figure;
imshow(gain_corrimage_sub, [0 255]);%, [0 256]);
title('subs image');

for i=1:pixelsperframe
   if gain(i)==4
```

```
      coefficient(i)=4095;
    else
      coefficient(i)=round(abs(gain(i))*1024)-1;
    end
 end

fid=fopen('ngc.txt','w');
for i=1:pixelsperframe
      fprintf(fid,'%s\n',dec2bin(round(gain(i)*1024)-1,16));
end
 fclose(fid);

for i=1:128
   for j=1:128
     if gain_corrimage_sub(i,j) == 0
        gain_correct(i,j)=4096;%for pixel replacement
     elseif (gain((i-1)*128+j)>4)
        gain_correct(i,j)=4095;
     else
        gain_correct(i,j)=(round(gain((i-1)*128+j)*1024));
     end
   end
end
temp=150;
for i=1:128
   for j=1:128
    if (pix_sub_info(i,j)==0) & (j~=1) & (i~=1) & (j~=128)
      gain_corrimage2(i,j)=gain_corrimage3(i,j-1);
      temp=333;
    else
      gain_corrimage2(i,j)=gain_corrimage3(i,j);
    end
```

```
end
end
figure;
imshow(gain_corrimage2, [0 4096]);%, [0 256]);
title('pix subs image');

figure;
imshow(gain_correct, [0 4096]);%, [0 256]);
title('gain correct image');
```