DESIGN OF A VIDEO PROCESSING AND SYSTEM CONTROL BOARD FOR A COMPACT THERMAL IMAGER

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
THE MIDDLE EAST TECHNICAL UNIVERSITY

BY

SERKAN DİNMEZ

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF
MASTER OF SCIENCE
IN
THE DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

DECEMBER 2002

Approval of the Graduate School of Natural and Applied Sciences.

Prof. Dr. Tayfur ÖZTÜRK
Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

Prof. Dr. Mübeccel DEMİREKLER
Head of Department

We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree Master of Science.

Assoc. Prof. Dr. Cengiz BEŞİKCİ
Supervisor

Examining Committee Members:

Assoc. Prof. Dr. Nevzat G. GENÇER

Assoc. Prof. Dr. Cengiz BEŞİKCİ

Assoc. Prof. Dr. Tayfun AKIN

Assoc. Prof. Dr. A. Aydın ALATAN

Assoc. Prof. Dr. Birsen SAKA

ABSTRACT

DESIGN OF A VIDEO PROCESSING AND SYSTEM CONTROL BOARD FOR A COMPACT THERMAL IMAGER

Dinmez, Serkan
M.S., Deparment of Electrical and Electronics Engineering
Supervisor: Assoc. Prof. Dr. Cengiz Beşikci

December 2002, 78 pages

This thesis reports the design and implementation of a high speed, system control and video processing board for a compact thermal imager. The board is integrated with a detector/dewar assembly, a front-end electronics board, and a video display unit to form a prototype infrared imaging system for 128x128 staring focal plane arrays. The functions of the video processing board include frame buffering, CCIR video generation, two point nonuniformity correction (NUC), image freeze, electronic zoom, and symbology insertion. Digital circuitry is implemented through the use of a Field Programmable Gate Array, which is programmed using the Very High Speed IC Description Language (VHDL).

After system integration, the prototype imaging system has thoroughly been tested and successful operation has been verified using a 128x128 InSb focal plane array. The imaging system can achieve a frame rate up to 550 Hz with 128x128 focal plane arrays coupled to Indigo 9806 read-out integrated circuits. The maximum supported standard focal plane array format is 320x256 at frame rates up to 100 Hz. Under typical operating conditions, the system performance is limited by the detector

and the read-out circuit where the noise level of the system is dominated by these components. Typical noise level of the front-end electronics board is 50 e^- which is considerably smaller than that of a typical cooled long wave infrared detector (4000 e^-).

Keywords: Infrared Imaging, Video Processing Electronics, Nonuniformity Correction

ÖZ

KOMPAKT TERMAL GÖRÜNTÜLEYİCİ İÇİN VİDEO İŞLEME VE SİSTEM KONTROL KARTI TASARIMI

Dinmez, Serkan
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Doç. Dr. Cengiz Beşikci

Aralık 2002, 78 sayfa

Bu tezde kompakt bir termal görüntüleme sistemi için yüksek hızlı, sistem kontrol ve video işleme kartı ve yazılımı tasarlanmıştır. Kart, 128 x 128 taramasız kızılötesi odak düzlem matrisli prototip termal görüntüleme sistemini oluşturmak için dedektör/ "dewar" takımı, dedektör ön elektronik kartı ve video monitörü ile entegre edilmiştir.Kart, görüntü kaydetme, CCIR video oluşturma, iki noktalı düzeltme, görüntü dondurma, elektronik büyütme ve semboloji ekleme fonksiyonlarını yerine getirebilmektedir. Sayısal tasarım, VHDL donanım tanımlama dili ile programlanan Alan Programlanabilir Kapı Dizileri (APKD) kullanılarak gerçekleştirilmiştir.

Entegrasyon sonrası, prototip görüntüleme sistemi, 128x128 InSb odak düzlem matrisi kullanılarak detaylıca test edilmiş ve başarı ile çalıştığı doğrulanmıştır. Görüntüleme sistemi, Indigo 9806 okuma entegresi ile kullanılan 128x128 odak düzlem matrisleriyle 550 resim/saniye hızda görüntüleme yapabilmektedir. Kartın desteklediği maksimum odak düzlem matris formatı 100 resim/saniye hıza kadar 320x256dır. Normal çalışma koşullarında, gürültü seviyesi dedektör ve okuma tümleşik devresi tarafından belirlenmekte ve sistem performansı bu birimler tarafından sınırlanmaktadır. Ön

elektronik kartının 50 e^- olan tipik gürültü seviyesi, tipik bir uzun dalga boyu kızılötesi detektörün gürültü seviyesine (4000 e^-) kıyasla oldukça düşüktür.

Anahtar Kelimeler: Kızılötesi Görüntüleme, Video İşleme Elektroniği, Farklılaşma Düzeltme

ACKNOWLEDGMENTS

I would like to express my sincere thanks to my advisor Assoc. Prof. Dr. Cengiz Beşikci for his encouragement, valuable comments and continued support throughout this study.

Special thanks to ASELSAN Inc. Microelectronics, Guidance and Electro-Optics division for providing technical support and laboratory environment in which we could develop our design.

I am also thankful to all my friends in ASELSAN and METU who have helped me throughout this thesis. Special thanks to teaching assistant Selçuk Özer (M.S) for his efforts to tackle the problems of the detector dewar assembly.

Finally, I would like to thank my family for their patience and support through out the thesis.

TABLE OF CONTENTS

APPENDICES

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

CHAPTER 1

INTRODUCTION

1.1 Overview

The thermal radiation emitted from the objects can not be sensed by human eye. Infrared imaging systems provide the opportunity of the conversion of infrared energy to the electrical signals by the detectors sensitive to this band of energy and the visualization of this information. In the generated image, the objects are seen in gray levels proportional to their IR radiation.

A basic infrared imaging system is shown in Figure 1.1. The system includes optics for collecting and focusing infrared radiation on the IR detector, an IR detector that can transduce infrared radiation to electrical signals, and signal processing electronics that form a visual representation of the IR scene from these electrical signals.

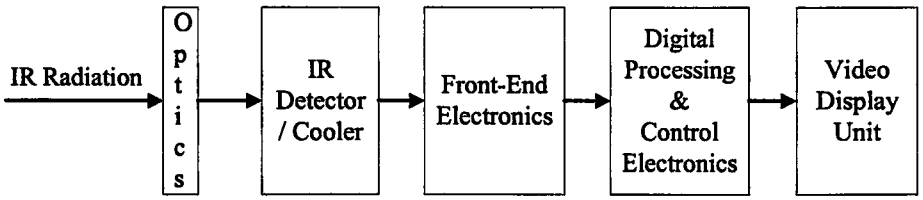

Figure 1.1 Block diagram of a basic infrared imaging system.

Signal processing chain of a staring array infrared camera is shown in Figure 1.2. Detector is the heart of an infrared camera because it converts infrared radiation

into measurable electrical signal and target spatial information into electronic temporal information. The quality of the detector directly effects the system performance.

The readout circuitry integrates the detector current on a capacitor, samples and holds the voltage on the capacitor, and multiplexes the voltage of all the detectors of the array to the output. The operation of the readout can be controlled through a digital interface.

The readout output voltages are buffered to maintain signal integrity. The analog output is adjusted by analog offset and gain circuitry to match the analog input level requirement of the analog to digital converter so that the dynamic range is used extenfully. Due to relative ease of of creating an image in digital domain and existance of many digital image enhancement algorithms, the analog detector voltage is digitized by an analog to digital converter [2].

The digitized data is stored in frame buffer memory for further digital processing. Digital processing algorithms can be used to enhance images, suppress noise, and put the image data into a format consistent with monitor requirements. The algorithms may also minimize the effects degrading the image caused by other parts of imaging system [3].

Every detector on an infrared array has a different gain (responsivity) and offset. These variations result in fixed pattern noise or spatial noise. If large deviations in responsivity exist, the image may be unrecognizable. As a result, systems employing more than one detector may require gain/level normalization [2] or nonuniformity correction (NUC) to produce an acceptable image. Although most literature [2] discusses NUC for staring systems, it also applies to scanning systems that have more than one detector in the cross scan direction [2]. For good imagery, the individual detector outputs are normalized (made equal) for several discrete input

intensities. These normalization intensities are also called calibration points or temperature references [5].

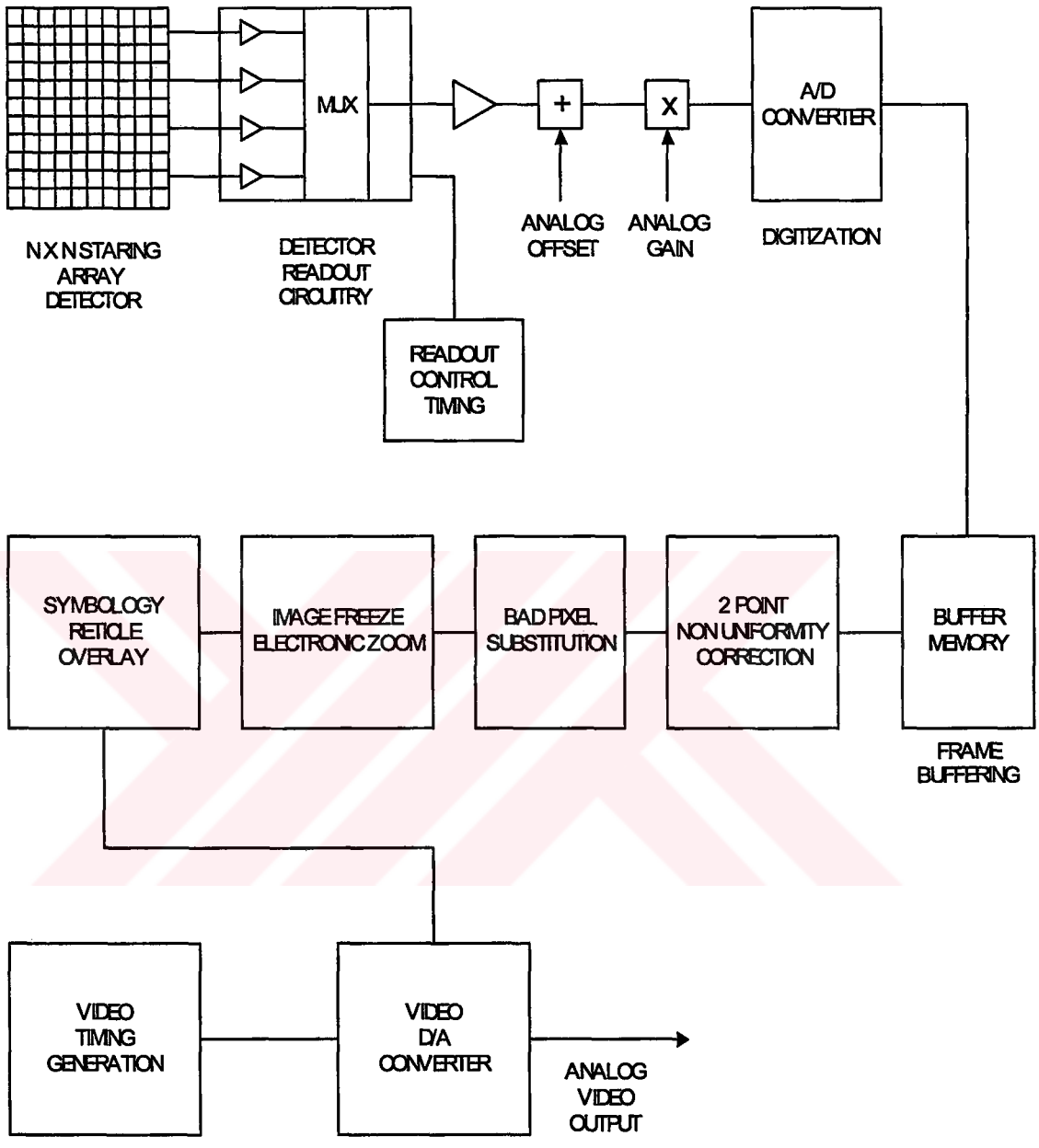

Figure 1.2 Signal processing chain of an infrared imager.

Figure 1.3 illustrates the responsivity of three different detectors before and after gain/level normalization. The outputs for input intensities I_1, I_2 and I_3 are shown

in Figure 1.3 (a). Figure 1.3 (b) illustrates the normalized output after correction at two points. If all the detectors had linear responsivities, then all the curves would coincide. As individual detectors deviate from linearity, the responsivity differences become more noticeable. It is this variation in responsivity that creates the fixed pattern noise (FPN) after gain/level correction [2].

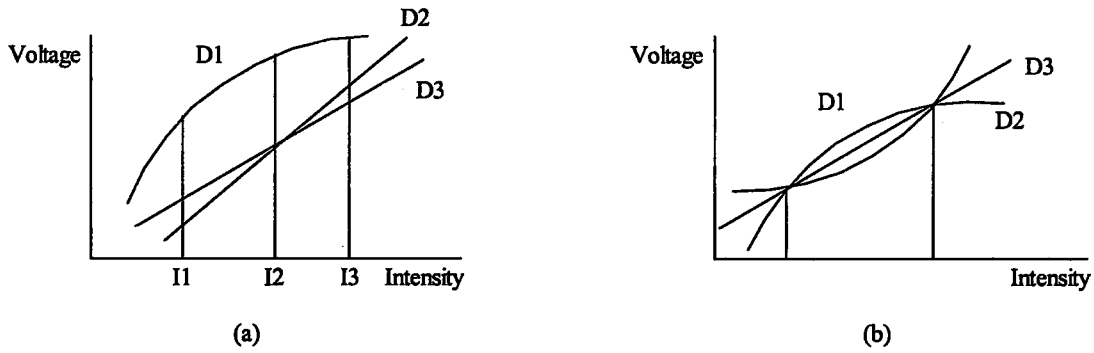

Figure 1.3 (a) Responsivity for three different detectors and (b) Responsivity curves after two-point correction.

With single point correction, the noise (fixed pattern plus random) will be a minimum at the reference intensity. With perfect correction, there will be no fixed pattern noise at the reference intensity. Truncation errors in the normalization algorithm and different spectral response of detectors produce residual FPN. As the background temperature deviates from the reference calibration temperatures, fixed pattern noise will increase. The amount depends upon how far the detector responsivity curves deviate from linearity. For two-point correction, the spatial noise will be minimum at two reference intensities. For any other intensity, the spatial noise increases. However, in the region between the two references, the spatial noise is less compared to the spatial noise outside the two references. As the reference temperatures are brought together, the fixed pattern noise between the reference inputs decreases and the fixed pattern noise outside the region increases. All input-to-output transformations affected by noise will be a function of the reference temperature and the background temperature [2].

Nonuniformity correction should be performed periodically. With scanning systems, the references can be placed at either end of the scan (Figure 1.4). During the inactive scan time, thermal reference scene is directed on to the detector by the use of a scanning mirror. The detector output due to the references is stored in memory and used in every frame for nonuniformity correction. One advantage of this method is that the thermal reference temperature can vary according to the scene dynamic range (called scene based correction). If the overall scene ΔT is small, then the differences in the reference temperatures are small. This dynamic correction ensures that nonuniformity is minimized for all scenes [2]. In some cases, it is not possible to include the blackbodies into the optical path for mechanical or optical reasons (notably staring arrays). With these systems, corrections are placed in firmware. Their success relies on detector stability; it assumes that the detector gain and offset does not change over time. This is true for many staring arrays.

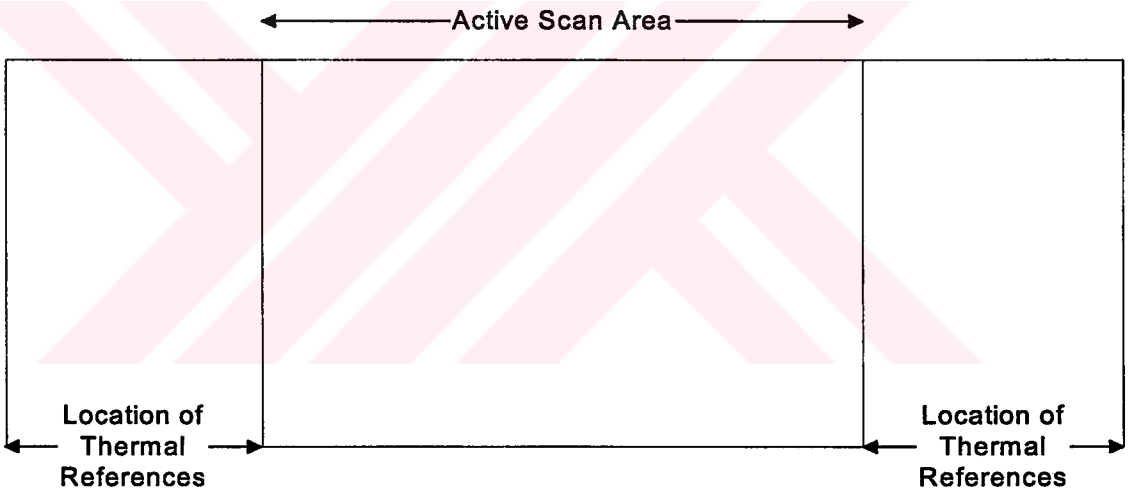

Figure 1.4 Location of thermal references in a scanning system.

Some of the detector pixels may not function well or may not function at all. During calibration process, these defective pixels are determined and their location in the array (defective pixel map) is stored in a nonvolatile memory [4]. This map is used for the nearest-neighbour defective pixel substitution.

Another function in an imaging system is the image freeze and electronic zoom capability, which enable the camera user to observe the scene in a more detailed manner. Image freezing is achieved by disabling the storage of new frame data to the buffer memory so that the last written image frame is read continuously. Electronic zooming is achieved by the interpolation of the pixels to have an enlarged image. Electronic zooming provides a larger display image of a narrower field, improving the probability of target detection and recognition, even though the actual field of view is not changed.

Symbology and reticle overlay on video is used to display messages or logos and is especially used in target tracking applications to choose the area of the image where the target is located.

There exist other image processing techniques applicable for infrared imaging systems that are not implemented through this thesis. Some systems use digital filters to implement image enhancement algorithms [16]. Dynamic range compression is another technique that is implemented in infrared systems to reduce the number of bits that carry the image information [16, 17]. The video processing and system control board is designed to support this kind of processing techniques as well. In the scope of this master thesis, FPGA designs of these techniques are not implemented.

After digital processing, the digital video should be converted to an analog representation that can be displayed on a monitor. The analog video generation is achieved by a video digital-to-analog converter, which accepts the digital video and monitor synchronization timing signals as input, and produces the composite analog video [5].

Digital processing and control electronics is an important element of an imaging system. The generation of control and timing signals required for system operation and the image processing techniques to improve image quality are implemented in this circuitry. The work presented in this thesis introduces a high

performance, flexible digital processing and control electronics design for a staring array detector based real time thermal imager.

1.2 The Goals and Organization of the Thesis

The main focus of this study has been placed on designing and constructing a digital processing and control electronics circuitry for a prototype real time infrared imager. The circuitry is interfaced to front-end electronics circuitry implemented through another MS. Thesis [1]. The readout and analog to digital converter control and timing signals are sent to the front-end electronics circuitry, and digitized detector data and user interface signals are received from the front-end electronics circuitry. The generated infrared video, complying CCIR standard, is displayed on the video display unit.

All digital design is implemented by using an FPGA. The sub-functions of FPGA logic are system control and timing signals generation, frame buffering, CCIR video generation, two-point nonuniformity correction, symbology insertion, electronic zoom, and image freeze.

A laboratory setup is organized to test the system. Laboratory test setup includes a blackbody as a thermal source for normalization process, a detector dewar assembly (DDA) to hold optics, cooler, detector and readout circuitry, the front-end electronics board, a logic analyzer and a digital oscilloscope to debug errors, and a PC with a HPVEE control software.

This thesis consists of six chapters. Chapter II explains the hardware architecture of the infrared imaging system designed. Chapter III presents the hardware design of the video processing and control electronics printed circuit board. Chapter IV focuses on the digital design of the video processing and system control electronics circuitry. Chapter V describes the setup used to test the infrared imaging

system and it presents the test results. Finally, Chapter VI comments on the conclusions and the future studies.

1.3 Summary

In this chapter, the infrared imaging systems are introduced. The basic components of the system are explained. Signal processing chain of the system is described. The goals and the organization of the thesis are defined. In the next chapter, the structure of the imaging system developed at METU and Aselsan Inc. will be described. Detector dewar assembly, the readout device, and the front-end electronics printed circuit board parts of the system will be explained.

CHAPTER 2

IR IMAGING SYSTEM DEVELOPMENT

2.1 Introduction

Figure 2.1 shows the block diagram of the IR imaging system developed at METU, which includes detector dewar assembly (DDA), front-end electronics PCB (FE), video processing and system control PCB (VP&SC) and CCIR standard display unit. The video processing and system control board of the imager has been designed and implemented in this thesis work.

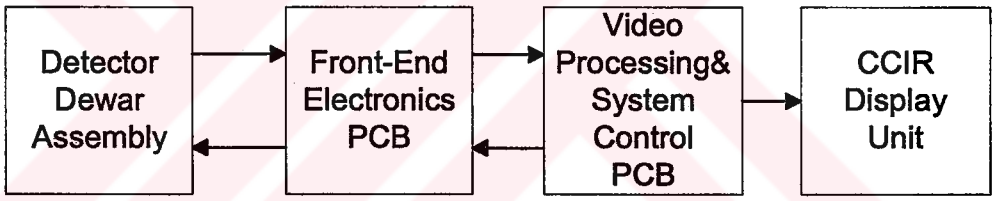

Figure 2.1 Block diagram of the IR imaging system.

2.2 Detector Dewar Assembly

Detector dewar assembly contains the optics, cooler, detector, and readout device. Various 128 x 128 staring array focal plane array detectors (QWIP, InSb) are currently used in the system but the hardware architecture is designed to support larger formats, such as 320x256.

2.2.1 Readout Device

The readout device used in the system is a commercial readout circuit provided by Indigo Systems [7]. The product with the part number ISC9806, is a high performance, 128 x 128 pixels, readout integrated circuit (ROIC) with snapshot mode integration. Both modes support integrate-while-read and integrate-then-read operations, variable gain, biasing techniques for high and low reverse bias detectors and signal skimming. Using four outputs, frame rates up to 480 frames per second can be achieved for full 128 x 128 frames [7]. The following sections summarize some of the features of this chip, including the pinout.

2.2.1.1 Pin out

The ISC9806 has 38 pins which are shown in Figure 2.2. The pin descriptions of the device are given in Table 2.1. The chip requires 5.5 V and 1.6 V bias voltages for correct operation. There are four video output channels. Gain and offset on these channels can be controlled through a digital interface. The readout timing can be also controlled through a digital interface.

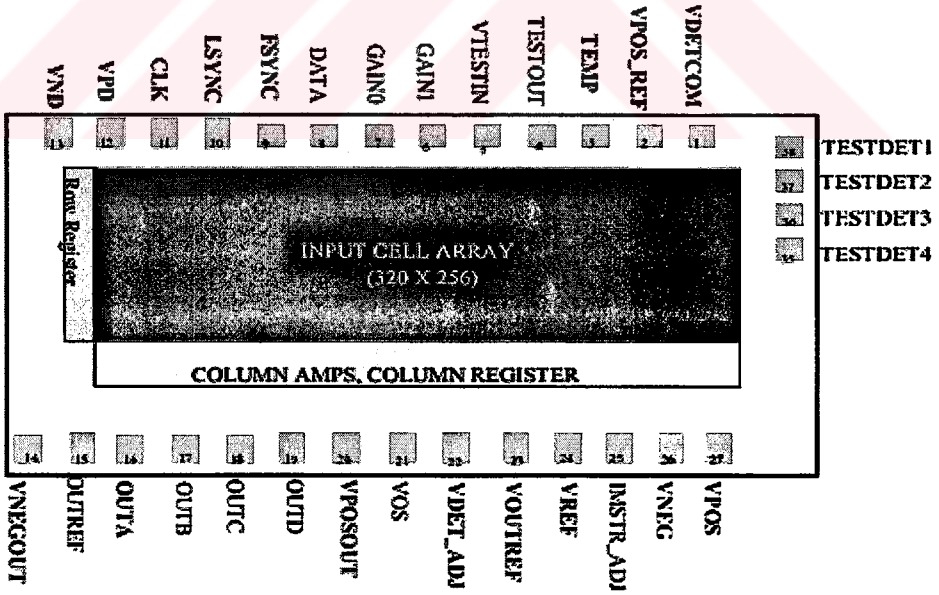

Figure 2.2 Readout device pinout [7].

Table 2.1 Pinout descriptions of the ISC9806 ROIC [7].

Pin No	Signal Name	Description
6	Gain0	External Gain: These pins are used to control the gain of the chip when operating in Default Mode
7	Gain1	
8	Data	Serial Control Register Data
9	Fsync	Frame Sync
10	Lsync	Line Sync
11	Clk	Data Output and Command Data Stream Clock
16	OutA	Video Output A
17	OutB	Video Output B
18	OutC	Video Output C
19	OutD	Video Output D
15	Outref	Common Mode Reference Output
3	Temp	Buffered Temperature Diode
23	Voutref	Analog Output Reference Voltage
21	Vos	Skimming Voltage
24	Vref	Analog Reference Voltage
22	VdetAdj	Detector Bias Adjustment
25	ImstrAdj	Master Current Adjustment
1	Vdetcom	Detector Common
2	VposRef	Low Voltage Detector VDETCOM Supply
27	Vpos	Analog Supply
12	Vpd	Digital Supply
20	Vposout	Output Supply
13	Vnd	Digital Return
15	Vnegout	Output Ground
26	Vneg	Analog Ground

2.2.1.2 Command Mode Operation

Command Mode operation utilizes the on chip serial control register to control device modes and advanced readout features. The fields of the serial control register are illustrated in figure 2.3. To operate in this mode, the data pad must be used to load control words into the serial control register. The settings in this register determine the gain state, detector bias setting, power bias control, master current bias, skimming setting, output mode, window size, window position, image transposition and test mode. Master clock frequencies up to 5 MHz are supported when operating in the command mode.

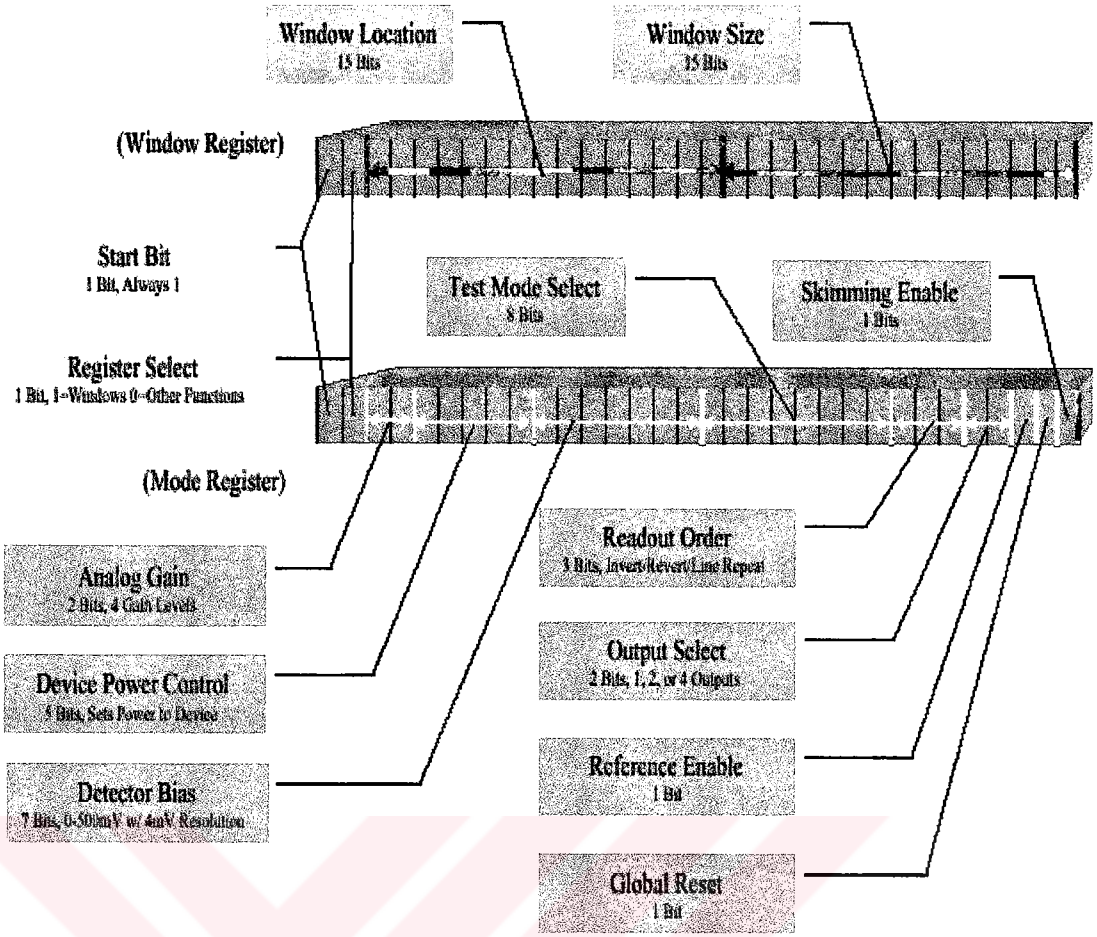

Figure 2.3 Serial control register fields [7].

2.2.1.3 Integration Modes

The readout device features snapshot mode integration, where all pixels integrate simultaneously. The integration process is controlled by the FSYNC clock, and allows both Integrate-While-Read and Integrate-Then-Read modes of operation. A timing pattern for the Integrated-While-Read operation is shown in the Figure 2.4. The rising edge of the FSYNC clock pulse marks the beginning of the frame time. This is followed by a series of LSYNC (LSYNC controls the synchronization of the readout of each individual line) pulses that produce the readout sequence. In this case, the frame time is approximately equal to the pixel readout time.

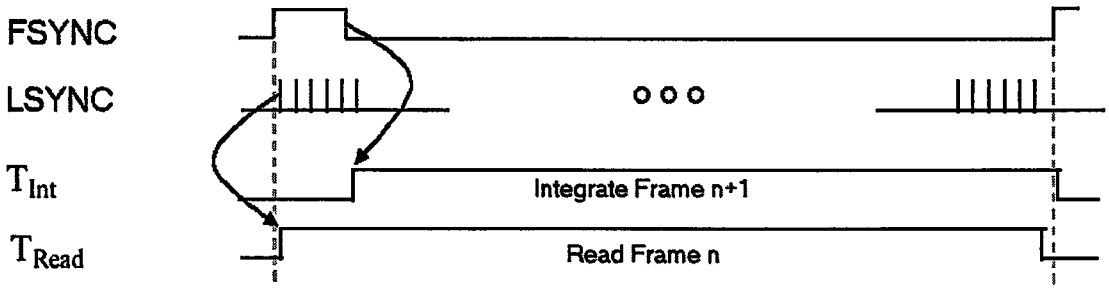

Figure 2.4 Integrate-While-Read mode [7].

Figure 2.5 shows a timing pattern for operation of the readout device in the Integrate-Then-Read mode. The rising edge of the FSYNC clock pulse marks the beginning of the frame time. This is followed immediately by a sequence of LSYNC pulses that produce a readout sequence. Note that in this case, the FSYNC clock remains high until the readout sequence has been completed. The integration time occurs after the readout time, resulting in a frame time that is approximately equal to the readout time plus the integration time. This results in a lower maximum frame rate and integration time duty cycle for a given window size.

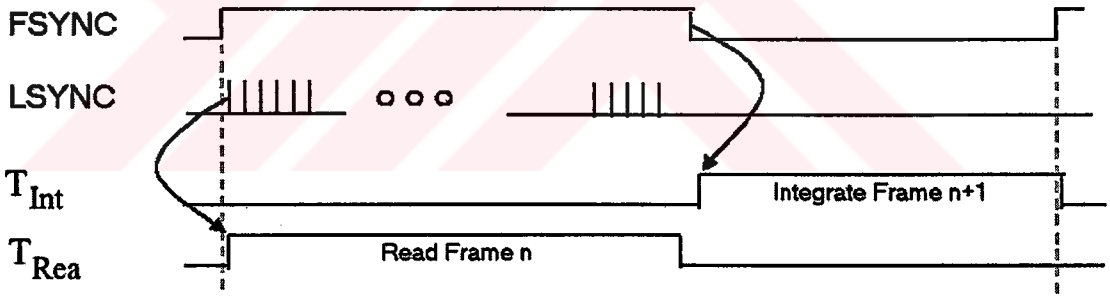

Figure 2.5 Integrate-Then-Read mode [7].

2.3 Front End Electronics PCB

Front-end electronics board is the interface electronics between detector readout circuitry and video processing board (Figure 4.6). The main functions of the

board are 12-bit digitization of the detector analog outputs, generation of the serial control word for the readout circuitry, communication with a PC via RS-232 interface, generation of power and reference voltage levels for the system, monitoring of focal plane array temperature, and control of the analog gain and offset on the detector output.

The user can control the readout parameters and image freeze operation through the interface supplied on the front-end electronics board. Switches and potentiometers enable the user to contol the settings. A serial ADC is used to digitize the information. FE FPGA adjusts the readout settings using this information. The control information required by the VP&SC board are transmitted via the serial communication channel between the boards. A HPVEE control software is also developed to control the paramaters via PC.

In the calibration mode, the digitized detector data are sent to a PC for two point nonuniformity correction coefficients calculation. The FE FPGA stores the consecutive frames of detector data to a SRAM and transfers this data to a PC via the RS-232 interface.

2.4 Summary

In this chapter, the structure of the imaging system developed at METU and Aselsan Inc. is described. Detector dewar assembly, the readout device, and the front-end electronics printed circuit board parts of the system are briefly explained. In the next chapter, the video processing and system control board PCB design will be introduced. Functional description and block diagram of the board will be presented. The components used in the design will be explained. High speed design considerations and techniques will be presented.

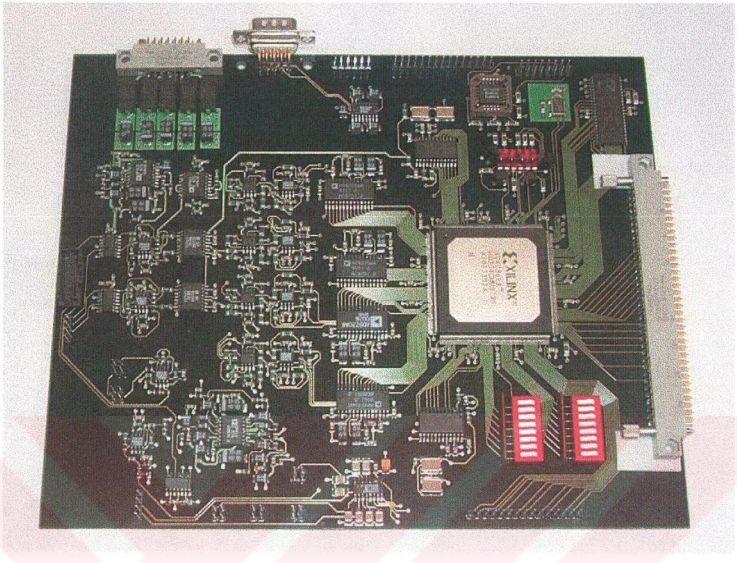

Figure 2.6 The front-end electronics printed circuit board, which is developed in the framework of another M.S. Thesis [1].

CHAPTER 3

VIDEO PROCESSING AND SYSTEM CONTROL PCB

3.1 Functional Description

In the framework of this thesis, a video processing and system control PCB (VP&SC) has been developed to be used in an IR imaging system. This PCB performs digital processing on digitized detector data and controls all system facilities. It acquires 128x128, 12 bit, detector array data from the front-end electronics PCB and after digital processing, it generates analog video in CCIR standard (25 frames/sec, 625 lines, 4:3 aspect ratio) which can be displayed on standard monochrome monitor (Figure 3.1).

To control the readout and front-end electronics circuitry some timing and control signals are required. Frame and line synchronization signals, readout and analog to digital conversion clock signals and scene state signals are generated by the video processing and system control board (Figure 3.2, Figure 3.3).

The communication with the front-end electronics PCB is handled through a serial transmission channel. The user can configure the system by the usage of potentiometers or switches on the front-end electronics PCB. Front-end electronics FPGA serialize this information and transmit it to the video processing and system control FPGA which intrepretes and serves the command. On the other way, the video processing and system control FPGA serializes the scene state information used to control analog gain and offset of the detector data and transmits it to the front-end electronics FPGA.

Nonuniform responsivity of the detectors causes fixed pattern noise on the image. To eliminate this noise, the detector data should be normalized. Normalization is achieved by addition of detector data with the normalization offset coefficient, and multiplication of the result with the normalization gain coefficient. The coefficients are calculated in the off-line mode. The detector data belonging to two different IR radiation levels are sent to a PC by the front-end electronics board. The PC normalization software calculates the coefficients for each detector. The coefficients are stored to the nonvolatile on board flash memory. Since flash memories have a long access time, real time normalization can not be acheived by using them. Because of this , with power on, the coefficients are transferred from the flash memory to the SRAMs which have a short access time. During system operation, the coefficients are read from these SRAMs.

The normalized detector data are stored in buffer memories.The buffer memories are used in an interleaved manner, such as, while one of them is storing current frame data, the other one is read to retrieve previous frame data. The retrieved frame data and CCIR video synchronization signals are sent to video digital to analog converter which forms the analog video in CCIR format. The analog video is buffered so that it can be transmited to long distances with negligible distortion. The buffered analog video is sent to the monitor through a 75 ohm BNC cable.

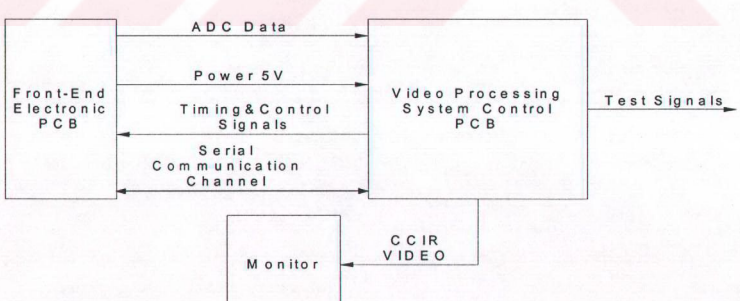

Figure 3.1 Interface diagram of the VP&SC PCB.

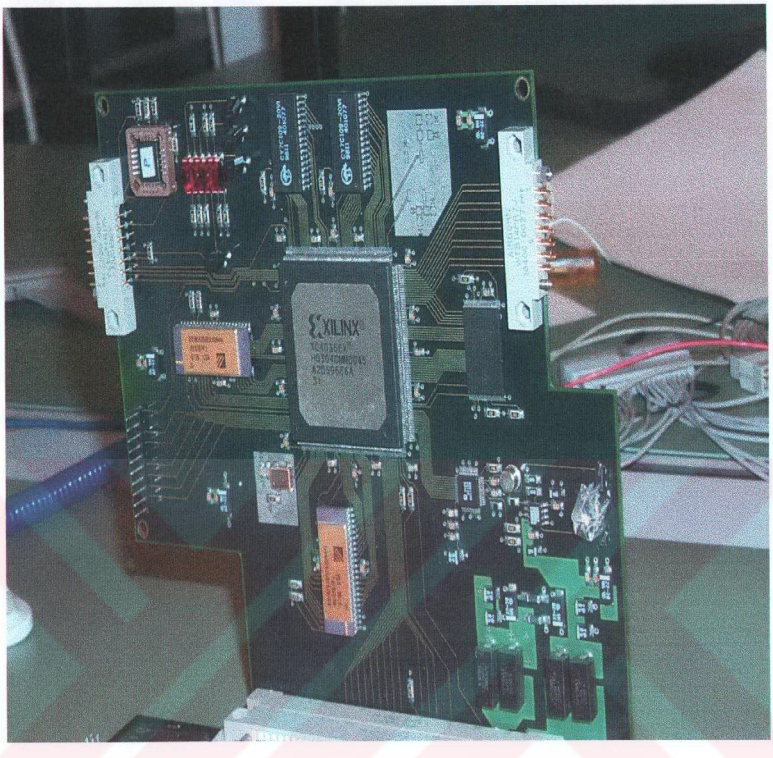

Figure 3.2 VP&SC printed circuit board.

Figure 3.3 Block diagram of VP&SC PCB.

3.2 Power

Video processing and system control PCB requires +5 V DC power supply for proper operation. Average power dissipation is about 1.5 W.

3.3 Critical Components

The critical components of the design are FPGA, FPGA configuration EEPROM, normalization coefficient SRAMs, buffer memory SRAMs, flash memory and video digital to analog converter.

3.3.1 Field Programmable Gate Array (FPGA)

FPGA is the most important component of the design. All the digital logic is embedded in this device. This device generates all the control and timing signals required for system operation. It contains the digital processing circuitry required to improve image quality.

FPGAs are extremely flexible logic devices. FPGA devices are implemented with a regular, flexible, programmable architecture of configurable logic blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable input output blocks (IOBs). They have routing resources to accommodate the complex interconnect patterns [9].

FPGAs are customized by loading configuration data into internal memory cells. The FPGA can either actively read its configuration data from an external serial or byte parallel PROM (master modes), or the configuration data can be written into the FPGA from an external device (slave and peripheral modes).

FPGA designs are supported by powerful and sophisticated software, covering every aspect of design from schematic or behavioral entry, floor planning, simulation, automatic block placement and routing of interconnects, to the creation and downloading, of the configuration bit stream. Because FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications.

Xilinx user-programmable gate arrays include two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs). CLBs provide the functional elements for constructing the application logic. IOBs provide the interface between the package pins and internal signal lines. Programmable interconnect resources provide routing paths to connect the inputs and outputs of these configurable elements to the appropriate networks. The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA [9].

The XC4036EX FPGA from Xilinx Company is chosen for our design. The parameters of this choice were the power dissipation, the speed, the logic density, the number of flip-flops and number of input output pins.

3.3.2 FPGA Configuration EEPROM

FPGA configuration data resides in an EEPROM, AT17C010 from Atmel Company (Figure 3.4). It is a 1,048,576 x 1-bit serial memory operating with a 5 V power supply [15].

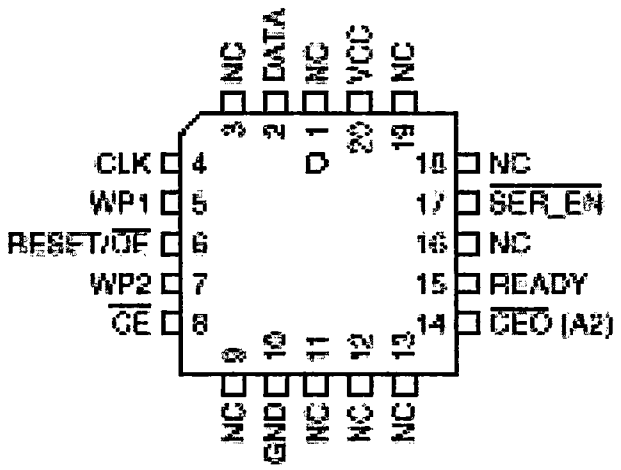

Figure 3.4 EEPROM pin diagram [15].

The M0, M1 and M2 pins of the FPGA select FPGA configuration mode. Applying logical low to these pins sets the configuration to master serial mode. In this mode, the CCLK output of the FPGA drives CLK input of the EEPROM. DIN input of the FPGA is connected to the DATA output of the EEPROM. The FPGA accepts the data on each rising edge of the CCLK. After loading of all the configuration data, DONE pin of the FPGA goes to logical high level indicating that configuration is successful. This pin is routed to the test connector for error debug purposes.

3.3.3 Nonuniformity Correction Coefficient SRAM

The nonuniformity correction coefficients reside in the SRAMs. The EDI816256CA from White EDC Company is chosen for this purpose (Figure 3.5, Table 3.1). It is a 256Kx16 bit CMOS static random access memory. It has an access time of 20 ns. It has TTL compatible inputs and outputs. It requires single +5V supply for operation. The operation truth table of the device is given in Table 3.2.

The parameters of choice are the capacity, the power dissipation and the access time. The memory capacity is selected to be more than required for a 128x128

detector array to support larger array of detectors. The 20 ns access time satisfies the system timing requirements. The coefficients reside in the 0 to 16383 addressed locations.

Table 3.1 EDI816256CA pin descriptions [10].

$A_{0\text{-}17}$	Address Inputs
$\overline{LB}$ ($I/O_{1\text{-}8}$)	Lower-Byte Control ($I/O_{1\text{-}8}$)
$\overline{UB}$ ($I/O_{9\text{-}16}$)	Upper-Byte Control ($I/O_{9\text{-}16}$)
$I/O_{1\text{-}16}$	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground
NC	No Connection

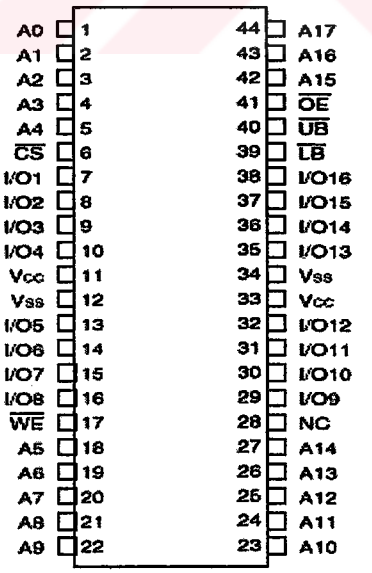

Figure 3.5 EDI816256CA pin diagram [10].

Table 3.2 EDI816256CA operation truth table [10].

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	Data I/O	
						I/O_{1-8}	I/O_{9-16}
H	X	X	X	X	Not Select	High Z	High Z
L	H	H	X	X	Output Disable		
L	X	X	H	H			
L	H	L	L	H	Read	Data Out	High Z
			H	L		High Z	Data Out
			L	L		Data Out	Data Out
L	L	X	L	H	Write	Data In	High Z
			H	L		High Z	Data In
			L	L		Data In	Data In

3.3.4 Buffer Memory SRAM

The digitally processed detector data are stored to and read from SRAMs. The CY7C109 from Cypress Company is chosen for this purpose (Figure 3.6, Table 3.3). It is a 128Kx8 bit CMOS static random access memory. It has an access time of 20 ns. It has TTL compatible inputs and outputs. It requires single +5V supply for operation. The operation truth table of the device is given in Table 3.4.

The parameters of choice are the capacity, the power dissipation and the access time. The memory capacity is selected to be more than required for a 128x128 detector array to support larger array of detectors. The 20 ns access time satisfies the system timing requirements. The detector data reside in the 0 to 16383 addressed locations.

Table 3.3 CY7C109 pin descriptions [13].

A_{0-16}	Address Inputs
I/O_{0-7}	Data Input/Output
CE1	Chip Enable-1
CE2	Chip Enable-2
V_{CC}	+5 V Power
GND	Ground
WE	Write Enable

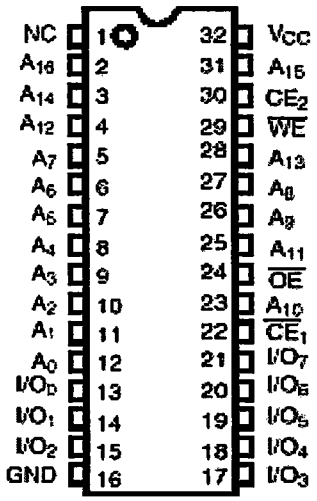

Figure 3.6 CY7C109 pin diagram [13].

Table 3.4 CY7C109 operation truth table [13].

$\overline{CE_1}$	CE_2	OE	WE	$I/O_0 - I/O_7$	Mode
H	X	X	X	High Z	Power-Down
X	L	X	X	High Z	Power-Down
L	H	L	H	Data Out	Read
L	H	X	L	Data In	Write
L	H	H	H	High Z	Selected, Outputs Disabled

3.3.5 Flash Memory

The nonuniformity gain and offset coefficients and symbology memory map reside in the nonvolatile flash memory. AM29F800B from AMD Company is chosen for this purpose (Figure 3.7, Table 3.5). It is an 8 Megabit (1 M x 8-Bit/512 K x 16-Bit) CMOS 5.0 Volt, Boot Sector Flash Memory with an access time of 120 ns [14].

The parameters of choice are the capacity, the power dissipation and the access time. The memory capacity is selected to be more than required for a 128x128 detector array to support larger array of detectors. The 120 ns access time satisfies the

system timing requirements. The offset coefficients reside in the 0 to 16383 addressed locations. The gain coefficients reside in the 16384 to 32767 addressed locations. The symbology memory map reside in the 32768 to 66047 addressed locations.

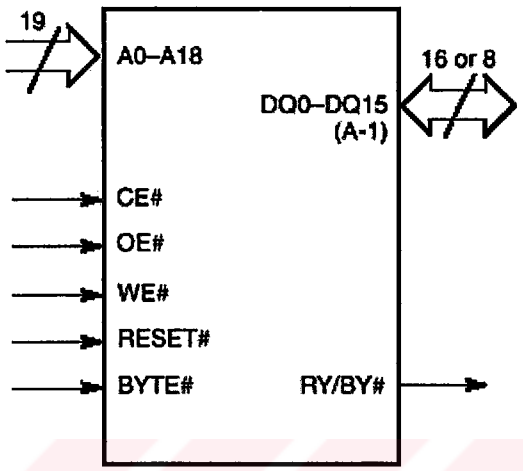

Figure 3.7 Flash memory pin diagram [14].

Table 3.5 Flash memory pin descriptions [14].

A_{0-18}	Address Inputs
DQ_{0-15}	Data Input/Output
CE	Chip Enable
RESET	Reset
V_{CC}	+5 V Power
GND	Ground
WE	Write Enable
OE	Output Enable
BYTE	8 bit or 16 bit Select

3.3.6 Video Digital to Analog Converter

The ADV7120 is a digital to analog video converter on a single monolithic chip. The part is specifically designed for high-resolution color graphics and video systems. It consists of three, high speed, 8-bit, video D/A converters (RGB); a standard TTL input interface and high impedance, analog output, current sources. Additional video input controls on the part include composite sync, blank and reference white.

3.3.6.1 VDAC Pin Descriptions

A single +5 V supply, an external 1.23 V reference and pixel clock input are required to make the part operational. The ADV7120 is capable of generating RGB video output signals, which are compatible with CCIR video standard [11].

Table 3.6 VDAC pin descriptions [11].

Pin Name	Pin Description
BLANK	Composite blank control input.The BLANK signal is latched on the rising edge of CLOCK.
SYNC	Composite sync control input.SYNC is latched on the rising edge of CLOCK.
CLOCK	Clock input. The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, SYNC, BLANK and REF WHITE pixel and control inputs.
REF WHITE	Reference white control input. REF WHITE is latched on the rising edge of clock.
R0–R7, G0–G7, B0–B7	Red, green and blue pixel data inputs. Pixel data is latched on the rising edge of CLOCK. R0, G0 and B0 are the least significant data bits.
IOR, IOG, IOB	Red, green, and blue current outputs.
ISYNC	Sync current output. This high impedance current source can be directly connected to the IOG output.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND, controls the magnitude of the full-scale video signal.
COMP	This is a compensation pin for the internal reference amplifier.

3.3.6.2 VDAC Design Considerations

An external 1.23 V voltage reference is required to drive the ADV7120. The AD589 from Analog Devices is chosen as reference. It is a two-terminal, temperature compensated bandgap voltage reference, which provides a fixed 1.23 V output voltage for input currents between 50 μA and 5 mA. Figure 3.8 shows the reference circuit connection diagram. The voltage reference gets its current drive from the ADV7120's analog power pin through an on-chip 1 kohm resistor to the V_{REF} pin. A 0.1 μF ceramic capacitor is required between the COMP pin and V_{AA} pin to provide compensation for the internal reference amplifier.

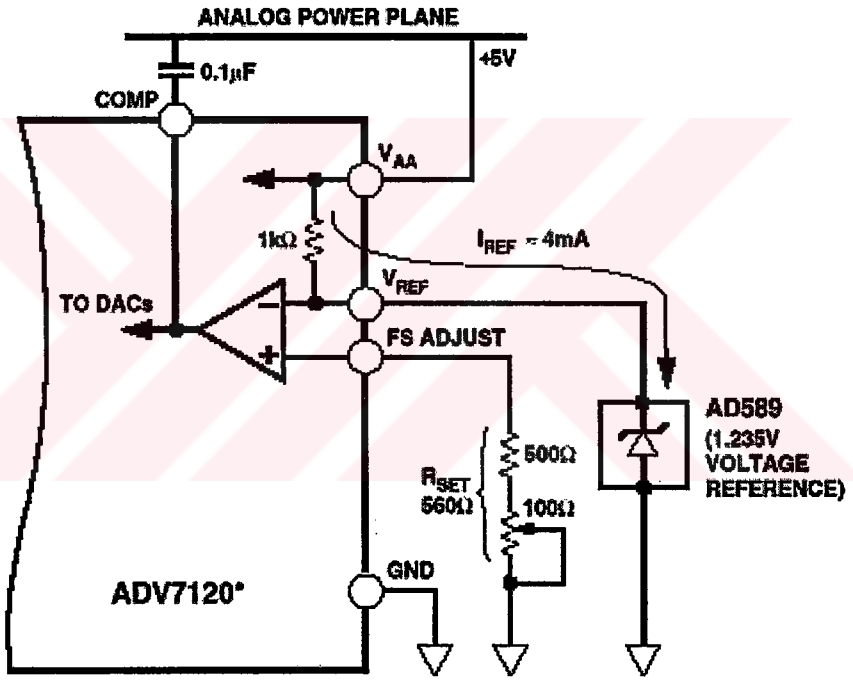

Figure 3.8 VDAC reference circuit.

A resistance RSET connected between FS ADJUST pin and GND pin determines the amplitude of the output video level according to the following equation:

$$IOG\ (mA) = 12{,}082 \times VREF\ (V)/RSET\ (ohm) \quad (3.1)$$

$$VOG\ (V) = IOG \times 37.5\ ohm \quad (3.2)$$

Selecting RSET as 560 ohm satisfies the required 1 V voltage level for CCIR standard.

In our design the ADV7120 is used for stand-alone, gray scale (mono-chrome) composite video application (i.e., only one channel used for video information). Since composite video synchronization insertion is available on only green channel, it is chosen for operation. The two unused video data channels are tied to logical zero.

The ADV7120 is specified to drive transmission line loads. However, in some applications it may be required to drive long transmission line cable lengths. Cable lengths greater than 10 meters can attenuate and distort high frequency analog output pulses. The inclusion of output buffers compensates for cable distortion. Buffers with large full power bandwidths and gains between 2 and 4 will be required. These buffers will also need to be able to supply sufficient current over the complete output voltage swing. The AD812 buffer from Analog Devices is chosen for our application [12]. Use of buffer amplifiers also allows implementation of other video standards besides CCIR. Altering the gain components of the buffer circuit results in any desired video level.

3.4 PCB Design Considerations

Designing a PCB containing high speed devices with fast slew rates requires special attention and design techniques to preserve the signal integrity and quality. A fast slew rate may contribute to noise generation, reflection, crosstalk and ground bounce. To a have a PCB properly work, the power must be filtered and evenly distributed to all devices to reduce noise, the signal lines should be matched and terminated properly to diminish reflections, the crosstalk between parallel traces should be minimized and effects of ground bounce should be reduced [6].

VP&SC board have three continuous ground planes and one continuous power plane which are adjacent to signal routing layers (Figure 3.9). This is required for three main reasons. First, it provides a low-impedance power system. Second, it makes the connection of low-impedance vias to device ground pins very convenient. Third, it provides a path for return currents. All of these are very important in keeping ground noise at a minimum, both on the board and in the devices [8].

The 5V DC power is filtered by a LC filter before distributed to the devices.To filter the high frequency noise due to switching outputs, bypass capacitors are placed as close as possible to the power pins of the devices. In bypass capacitor selection the frequency characteristics and current capability should be taken into account.

The ratio of signal rise/fall time to trace length can determine whether or not transmission-line effects will occur. In general, long traces with fast rise/fall times exhibit transmission-line effects. If the time it takes a signal to propagate down the length of the trace is more than 1/6 of the signal rise/fall time, transmission-line effects are likely, and the signal path must be simulated. The electrically long signals of this design have been simulated for this reason, and since ringing and reflection was acceptably low , no termination was required (Figure 3.10, Figure 3.11).

Clock signals require special attention for two reasons. First, it is critical that their timing not be marginalized by noise which can lead to false clocking of data. Second, clock signals often run at a higher frequency than data, and so can be more troublesome as noise sources. When doing component placement on the PCB all ICs are oriented and located to minimize the length of the clock runs. To mimize clock signal loops, they are routed very close to ground planes. Traces which run in parallel for long distances, may cause crosstalk problem mainly due to the mutual inductance. Separating the traces or decreasing their distance from the associated reference plane can decrease the crosstalk.

Signal Layer
Ground Layer
Signal Layer
Ground Layer
Power Layer
Signal Layer
Ground Layer
Signal Layer

Figure 3.9 VP&SC PCB layer stackup.

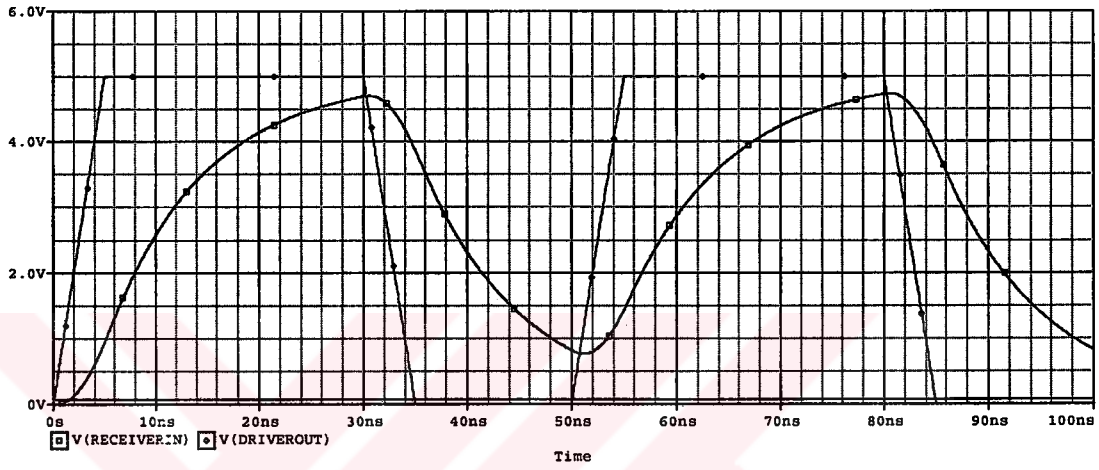

Figure 3.10 Simulation results for long traces of the PCB.

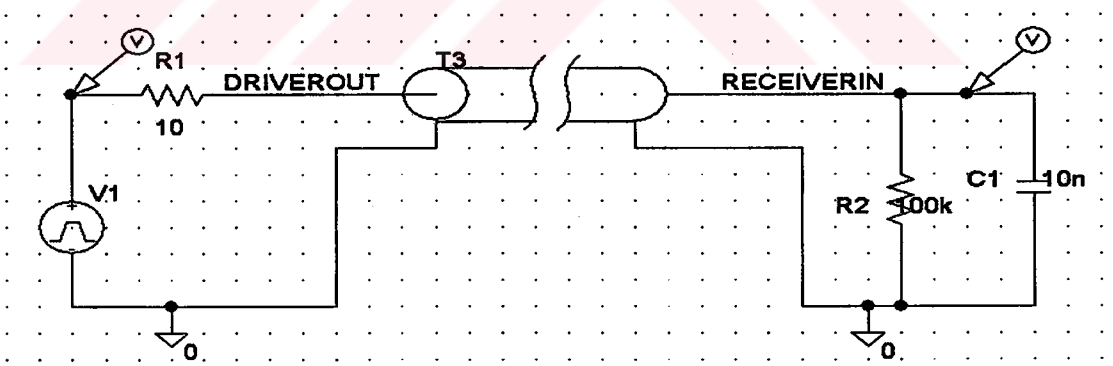

Figure 3.11 Simulation circuitry for long traces of the PCB.

3.5 Summary

In this chapter, the video processing and system board PCB design is introduced. Functional description and block diagram of the board is presented. The components used in the design are explained. High speed design considerations and techniques are presented. In the next chapter, the digital design embedded in the FPGA that implements the video processing and system functions of the board will be presented. The functional description and the block diagrams of the FPGA software will be given. The design details and the operation of the blocks will be explained.

CHAPTER 4

VIDEO PROCESSING AND SYSTEM CONTROL DIGITAL DESIGN

4.1 Introduction

All the digital functions required to make video processing and system control (VP&SC) PCB operational are designed and implemented using XC4036EX FPGA from Xilinx. Design flow starts with the analysis of the system requirements from which the subfunctions are defined. VHDL (Very High Speed IC Description Language) is used to describe the behaviour and structure of digital electronic hardware for subfunctions. The correct operation of VHDL design blocks are verified by functional simulations using test benches. After simulations, gate level netlist is achieved by synthesis of the VHDL design. In the next step, the gate level design is placed and routed in the FPGA. Finally post layout simulation is used to verify the design timings.

4.2 Functional Specification

VP&SC FPGA is composed of the two point nonuniformity correction block, the CCIR video timing block, the buffer memory write block, the buffer memory read block, the symbology inserter block, the readout timing block, the bad pixel substitution block, the image freeze and zoom block, the initialization block, the coefficient reader block and the serial communication block (Figure 4.1).

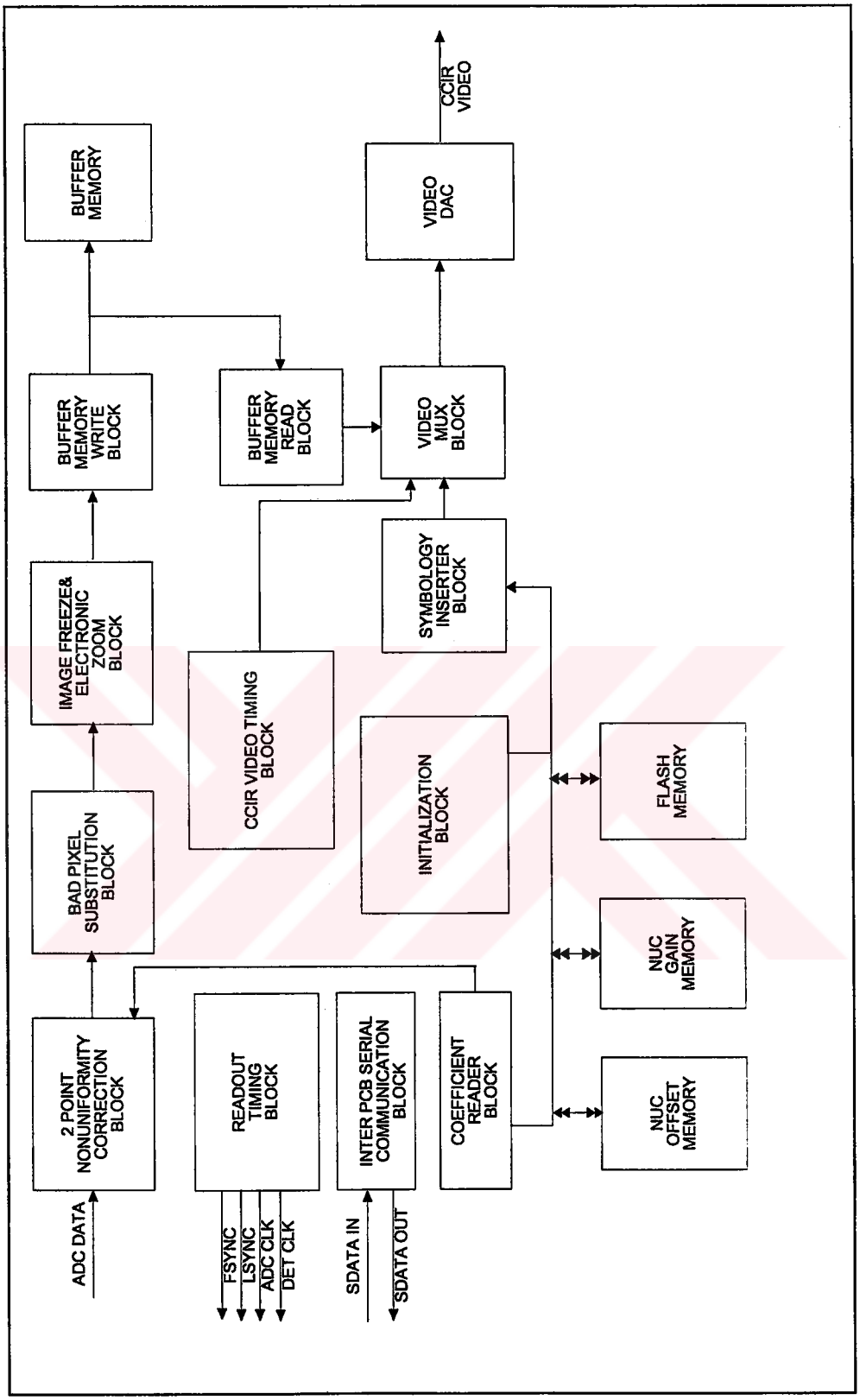

Figure 4.1 VP&SC FPGA block diagram.

4.2.1 Two Point NUC Block

In this section, two point NUC block of the FPGA logic is presented. The functional description, the pin descriptions (Table 4.1) and operation of the block are explained.

4.2.1.1 Two Point NUC Block Functional Description

Two point nonuniformity correction (NUC) block implements the correction algorithm on the incoming detector data. Firstly, it sums unsigned 12 bit video with 13 bit two's complement signed offset coefficient read from NUC offset memory. After summation it applies overflow/underflow check to the result and forms 12 bit unsigned result. Then this result is multiplied with 12 bit unsigned gain coefficient read from NUC gain memory. After clipping operation, the result is unsigned 8-bit two-point nonuniformity corrected video.

4.2.1.2 Two Point NUC Block I/O Description

The pinout of the two point NUC block is shown in Figure 4.2. This block has six input pins and two output pins. It has interface to buffer memory write block.

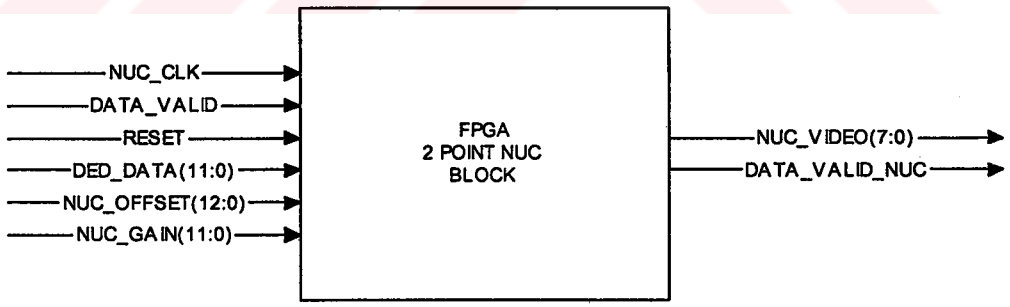

Figure 4.2 Pinout of the two point NUC block.

Table 4.1 Pin description of the two point NUC block.

RESET	Input	Global reset signal for all registers
NUC_CLK	Input	5 MHz operating clock
DED_DATA	Input	12 bit uncorrected detector data
DATA_VALID	Input	Signal indicating that the input detector data is valid
NUC_OFFSET	Input	13 bit 2's complement signed NUC offset coefficient
PIX_SUB	Input	Pixel substitution indicator
NUC_GAIN	Input	12 bit unsigned NUC gain coefficient
NUC_VIDEO	Output	8 bit corrected video
DATA_VALID_NUC	Output	Pipeline delayed DATA_VALID signal

4.2.1.3 Operation of Two Point NUC Block

To prevent overflow/underflow, sign extension is applied to DED_DATA and NUC_OFFSET signals. Sign extension on DED_DATA is achieved by "00" concatenation from the left and sign extension on NUC_OFFSET is achieved by most significant bit concatenation from the left. Sign extended signals are summed by the usage of a 14-bit adder. The adder output is checked by the overflow/ underflow control logic. Decision is based on the most significant 2 bits of the SUM, SUM (13,12). If SUM (13,12) equals "00", the least significant 12 bits of sum is latched to the 12 bit register on the rising edge of the NUC_CLK. If SUM (13,12) equals "01", this indicates an overflow condition and (3FF) Hex is latched to the register on the rising edge of the NUC_CLK. If SUM (13,12) equals "10" or "11" this indicates an underflow condition and (000) Hex is latched to the register on the rising edge of the NUC_CLK. The incoming video is unsigned so the summation should not turn it to a negative value (Figure 4.3). The operation of the adder circuitry is summarized by the equation 4.1, equation 4.2, and equation 4.3.

$$Op1=\text{"00"} \ \& \ DED\_DATA \tag{4.1}$$

$$Op2 = NUC\_OFFSET\ (12) \ \& \ NUC\_OFFSET \tag{4.2}$$

$$SUM = Op1 + Op2 \tag{4.3}$$

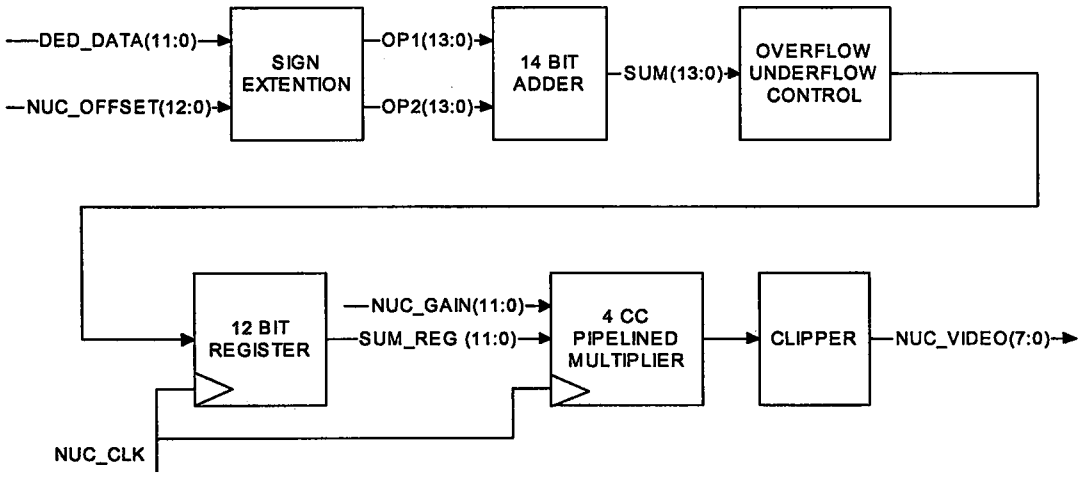

Figure 4.3 Two point NUC block diagram.

The examples given below, further illustrate the operation of the adder circuitry. The examples show the overflow, underflow and normal operation cases.

Examples:

a) Op1 = 00 1111 1111 1111 (4095 decimal) and

Op2 = 00 0000 0000 0001 (1 decimal)

SUM = 01 0000 0000 0000 SUM (13, 12) ="01" overflow so

SUM_REG = 1111 1111 1111

b) Op1 = 00 0000 0000 0000 (0 decimal)

Op2 = 11 1111 1111 1111 (-1 decimal)

SUM = 11 1111 1111 1111 Sum (13, 12) ="11" underflow so

SUM_REG =0000 0000 0000

c) Op1 = 00 0001 0010 0011 (291 decimal)

Op2 = 11 1111 0100 1010 (-182 decimal)

SUM = 00 0000 0110 1101 SUM (13, 12) ="00" no overflow/underflow so

SUM_REG = 0000 0110 1101

In the next step, gain correction is applied. The 12 bit offset corrected data is multiplied with 12 bit NUC gain coefficient. To achieve this in real time, a fast array parallel pipelined 12 bit times 12 bit unsigned fixed point multiplier is designed.

Figure 4.4 shows the structure of the multiplier, where Op1 denotes the multiplicand and Op2 denotes the multiplier. To calculate the product, twelve partial products should be added concerning their least significant bit positions. Addition of these twelve 12 bit partial products requires a huge combinational logic and long carry chains, which limit the operating clock frequency. Pipelining is applied to enable the multiplier work for higher clock frequencies, as shown in Figure 4.5. Instead of adding all partial products in one clock cycle, addition job is partitioned as in Figure 4.5 and ended in 4 clock cycles.

Another important issue is the alignment of the partial products before addition. The summation terms should be aligned by shifting according to the number of bits difference between their least significant bits.

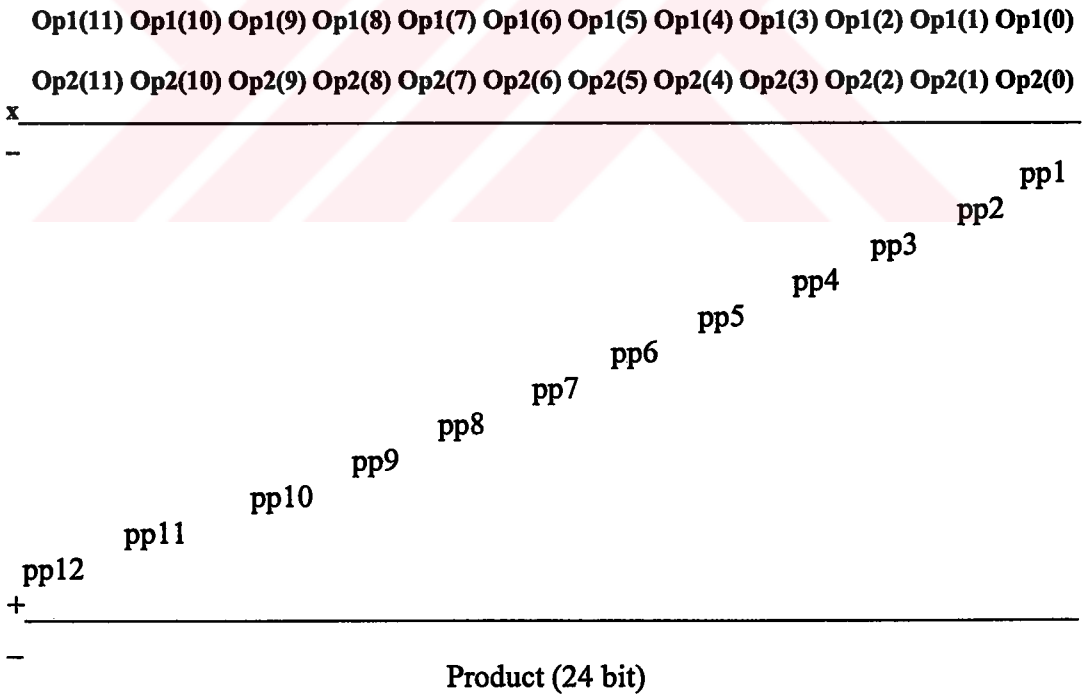

Figure 4.4 The multiplier structure.

After multiplication, 24 bit precision two point nonuniformity corrected video is achieved. The gain coefficient values stored in the memory are 2^{12} times of their actual values to achieve higher precision calculations. The clipping circuitry divides the product to 2^{12} by 12 bit right shifting and outputs the most significant 8 bits of the result to the NUC_VIDEO.

There exits five clock cycles latency between the valid DED_DATA and the valid NUC_VIDEO output. The DATA_VALID input signal is also five clock cycle delayed to form the DATA_VALID_NUC signal (Figure 4.6).

When the PIX_SUB signal is at logical high level, the current pixel is substituted with the previous one. This is achieved by a latch, which has previous and current pixel values multiplexed in its input.

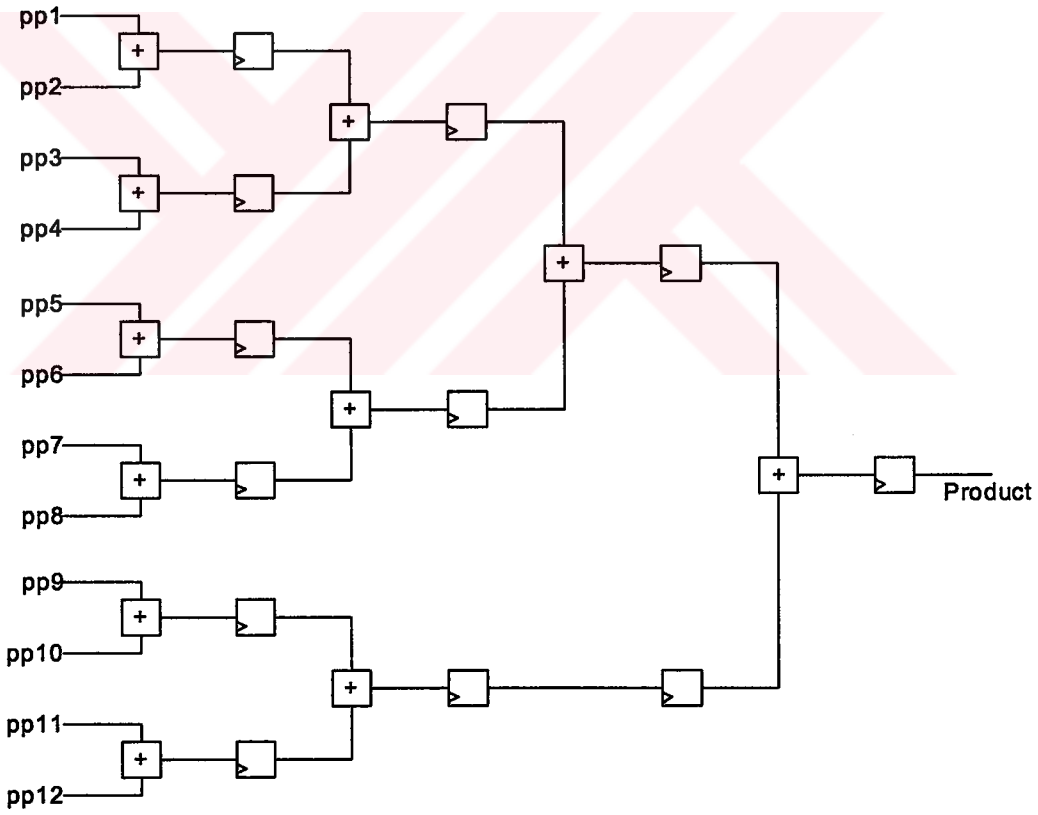

Figure 4.5 Pipelined summation.

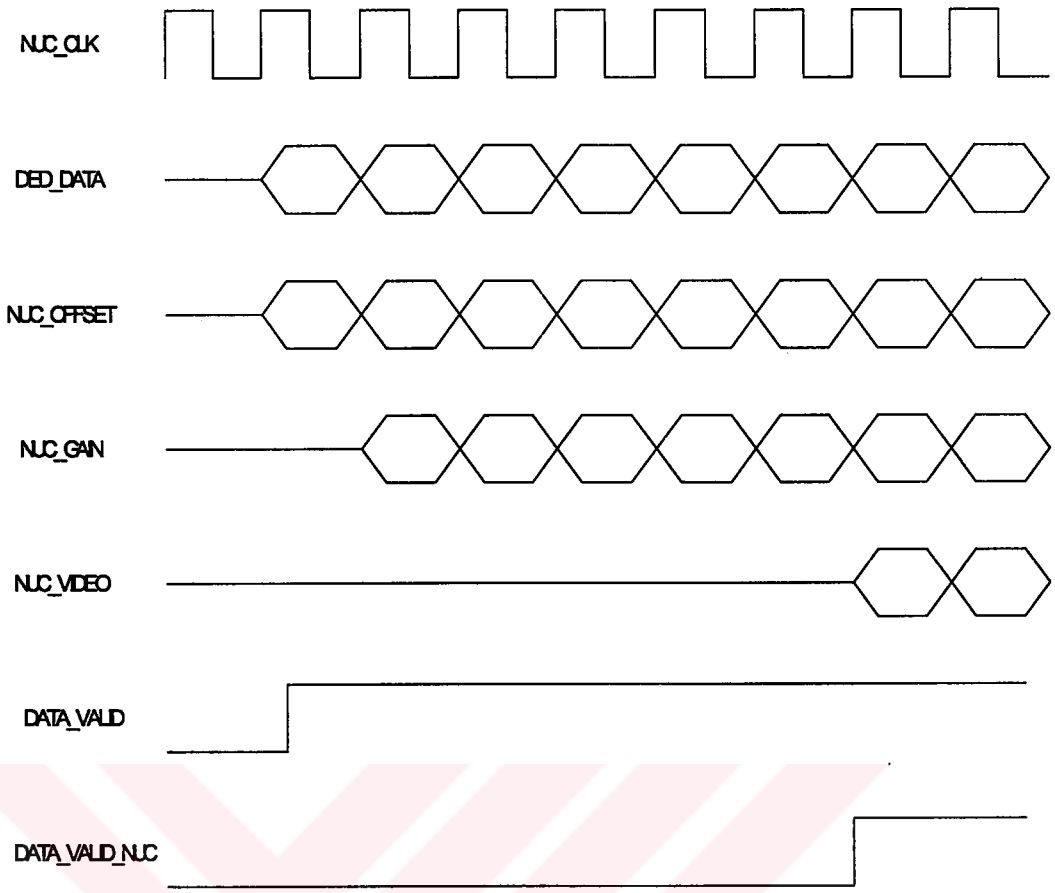

Figure 4.6 Two point NUC timing diagram.

4.2.2 Buffer Memory Write Block

In this section, buffer memory write block of the FPGA logic is presented. The functional description, the input output declaration, the pinout diagram, the pin descriptions (Table 4.2), and the operation of the block are explained. This block is responsible for the storing of the processed detector data to the buffer memory. The block applies the necessary address, data and control signals to the buffer memory.

4.2.2.1 Buffer Memory Write Block Functional Description

Buffer memory write block, stores one frame of processed 8 bit video to the buffer memory. This block generates the required buffer memory address and control signals.

4.2.2.2 Buffer Memory Write Block I/O Description

The pinout of the buffer memory write block is shown in Figure 4.7. This block has six input pins and four output pins. It has interface to the buffer memory.

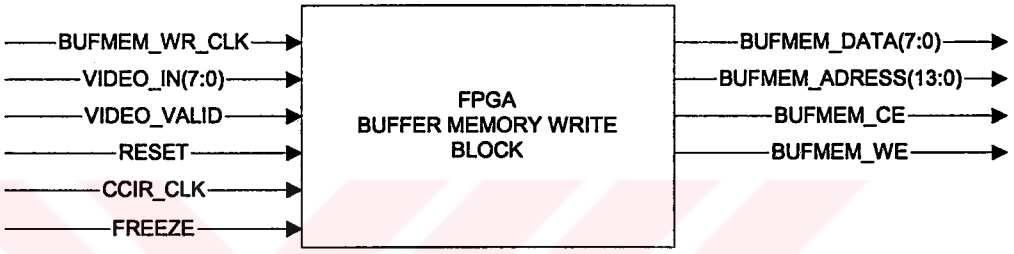

Figure 4.7 Pinout of the buffer memory write block.

Table 4.2 Pin description of the buffer memory write block.

RESET	Input	Global reset signal for registers
BUFMEM_WR_CLK	Input	5 MHz clock signal
VIDEO_VALID	Input	Indicates that the incoming video is valid
VIDEO_IN	Input	8 bit processed video
FREEZE	Input	Image freeze signal
CCIR_CLK	Input	10 MHz clock signal
BUFMEM_DATA	Output	Buffer Memory 8 bit data bus
BUFMEM_CE	Output	Buffer Memory active low chip enable pin
BUFMEM_WE	Output	Buffer Memory active low write enable pin
BUFMEM_ADRESS	Output	Buffer Memory 14 bit address bus

4.2.2.3 Operation of Buffer Memory Write Block

When the incoming data VIDEO_IN is valid, VIDEO_VALID signal is at logic high level. The logical not of this signal is used to produce the chip enable of the buffer memory.

In the addressing of the memory, a 14 bit counter is used. This counter increments at the rising edge of the clock as long as VIDEO_VALID signal is at logic high level. The VIDEO_VALID signal is at logic high level for 128 clock cycles for each line of video. Since there are 128 lines during a frame, there exists 128 VIDEO_VALID at logic high events. So the counter counts from 0 to 16384 during a frame. For one frame, with 128 by 128 resolution detector array, 16384 pixels are acquired. Hence this counter can address all the detector data.

To properly write to a memory, two points are critical; the address bus should be stable before the falling edge and till the rising edge of write enable pin .The data bus should be stable for setup time before rising edge and should be stable for hold time after rising edge. As shown in Figure 4.8, to fulfill this requirement, the CCIR_CLK signal is used. The CCIR_CLK signal frequency is 2 times of the BUFMEM_WR_CLK signal. By dividing the ccir_clk signal by 2, the write enable signal is produced which has 90 degrees phase difference with BUFMEM_WR_CLK signal (Figure 4.8). The image freeze operation is achieved by disabling the writing of new data to the buffer memories, hence last written frame data are read continuously. The FREEZE signal is controlled at the beginning of each frame, if it is at logical low level, the write enable pins are held at logical high level hence writing is disabled. The block diagram of the buffer memory write block is given in Figure 4.9.

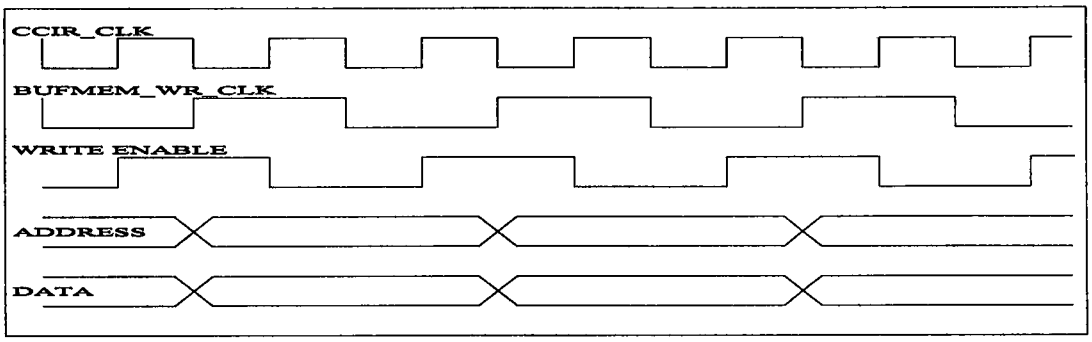

Fig 4.8 Memory write timing.

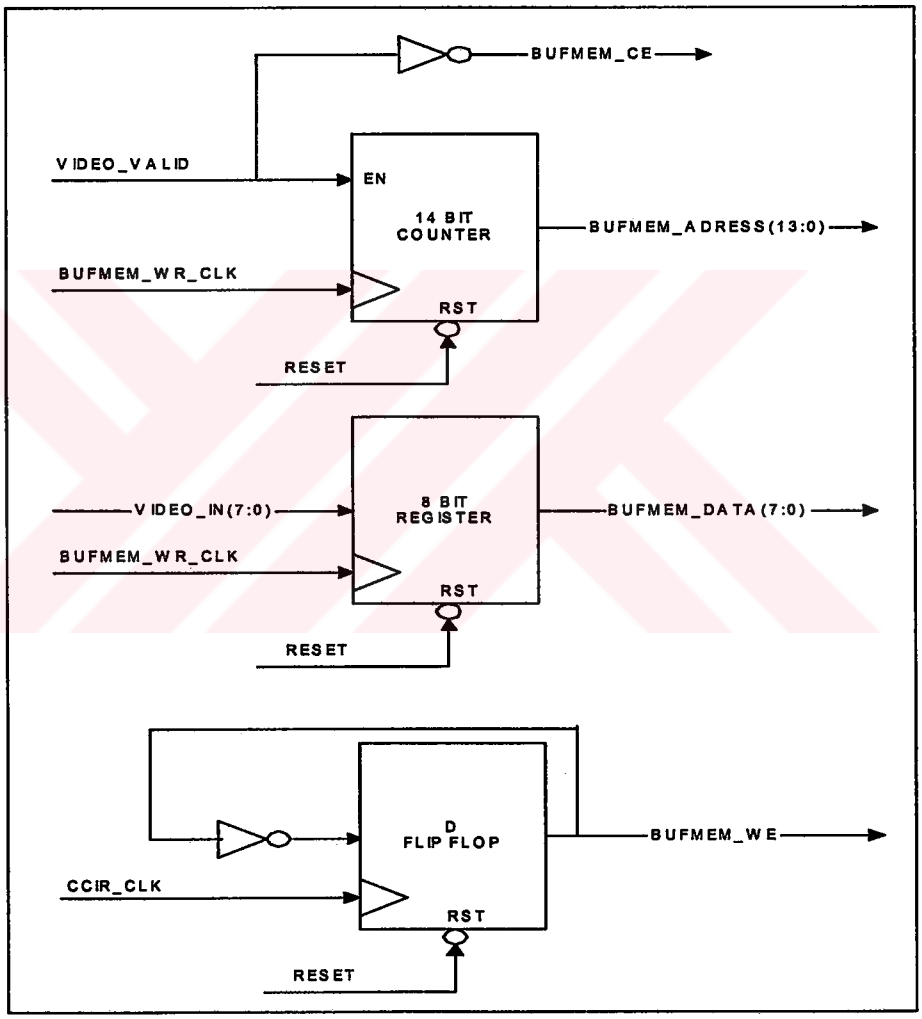

Figure 4.9 Buffer memory write block diagram.

4.2.3 Readout Timing Block

In this section, readout timing block of the FPGA logic is presented. The functional description, the pin descriptions (Table 4.3) and operation of the block are explained.

4.2.3.1 Readout Timing Block Functional Description

ROIC timing generation block generates the required timing signals to control the readout IC that reads detector array data. ROIC timing is controlled through a digital interface composed of FSYNC, LSYNC and CLK signals. This block also generates the ADC sampling clock of which frequency is twice of the ROIC_CLK. Another signal generated by this block is DATA_VALID_WRITE which informs the system that incoming detector data is valid.

4.2.3.2 Readout Timing Block I/O Description

The pinout of the readout timing block is shown in Figure 4.10. This block has two input pins and five output pins. It has interface to the front-end electronics board.

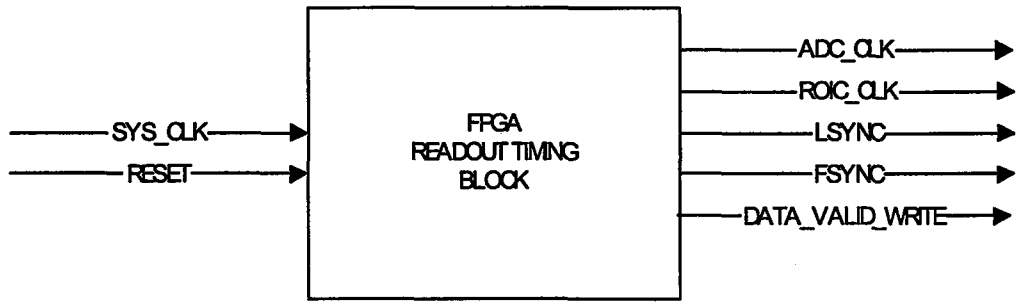

Figure 4.10 Pinout of the readout timing block.

Table 4.3 Pin description of the readout timing block.

RESET	Input	Global reset signal for registers
SYS_CLK	Input	40 MHz on board oscillator clock signal
DATA_VALID_WRITE	Output	Indicates that the detector data coming from FE PCB is valid
LSYNC	Output	ROIC line synchronization signal
FSYNC	Output	ROIC frame synchronization signal
ROIC_CLK	Output	2.5 MHz ROIC clock signal
ADC_CLK	Output	5 MHz ADC sampling clock signal

4.2.3.3 Operation of Readout Timing Block

The rising edge of the FSYNC signal marks the beginning of the frame time. LSYNC signal controls the synchronization of reading of each individual line on the detector array. The readout outputs detector array pixel values on the both edges of the ROIC_CLK signal. For proper operation of the ROIC, the FSYNC signal should change its state on the rising edge of the ROIC_CLK and LSYNC signal should change its state on the falling edge of the ROIC_CLK.

In this design, integrate-then-read mode of integration is used. The integration time can be adjusted by varying FSYNC signal pulse width. The integration time can be adjusted through a potentiometer on the FE PCB. FE FPGA sends this information to the VP&SC FPGA via the serial communication channel. The VP&SC FPGA uses this information to vary the FSYNC signal pulse width hence adjusting the integration time.

During one frame time 130 LSYNC pulses are sent to the ROIC. The first valid line data appears after the third LSYNC pulse and totally 128 lines are read. The first valid pixel of the line appears 3 clock cycles after the rising edge of LSYNC pulse and totally 128 pixels are read for each line. Each line read period is 131 clock

cycles composed of 3 clock cycles of latency, 64 clock cycles of data read and 64 clock cycles of analog setup time (Figure 4.11, Figure 4.12).

Since the detector data is read on both edges of the ROIC_CLK, ADC_CLK is twice of frequency of the ROIC_CLK. The ROIC_CLK and ADC_CLK signals are generated from the SYS_CLK signal by a clock divider circuitry.

For the generation of DATA_VALID_WRITE signal ROIC timing, FE PCB analog settling time and ADC timing are taken into account (Figure 4.13).

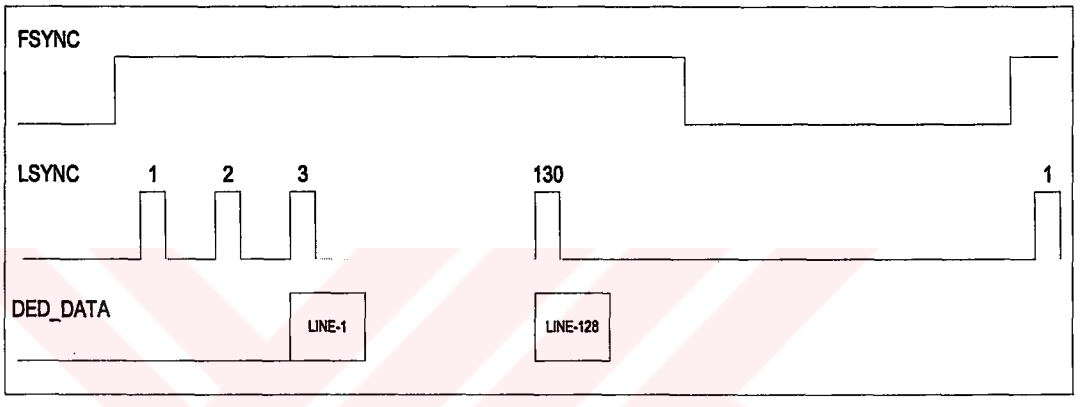

Figure 4.11 ROIC line read timing.

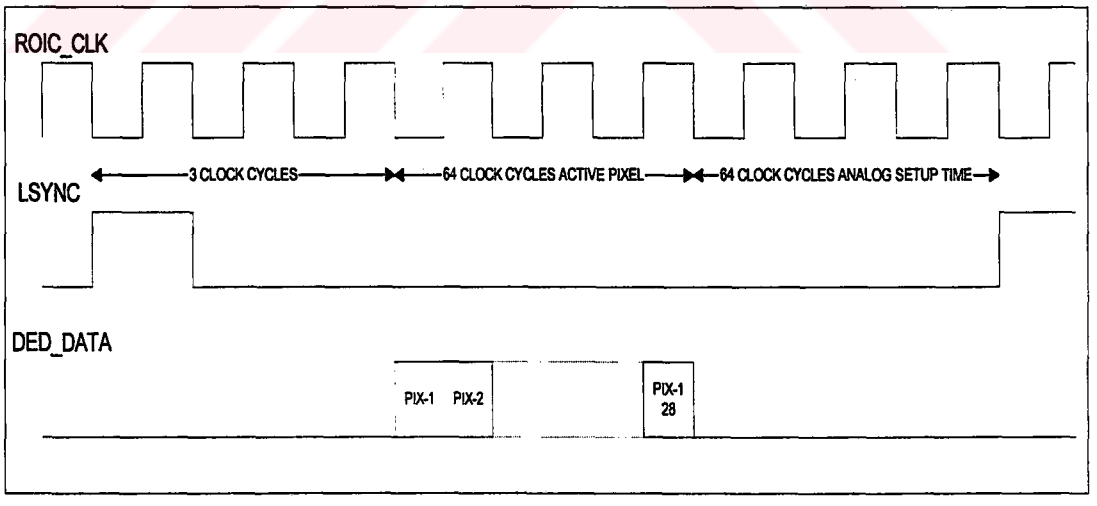

Figure 4.12 ROIC pixel read timing

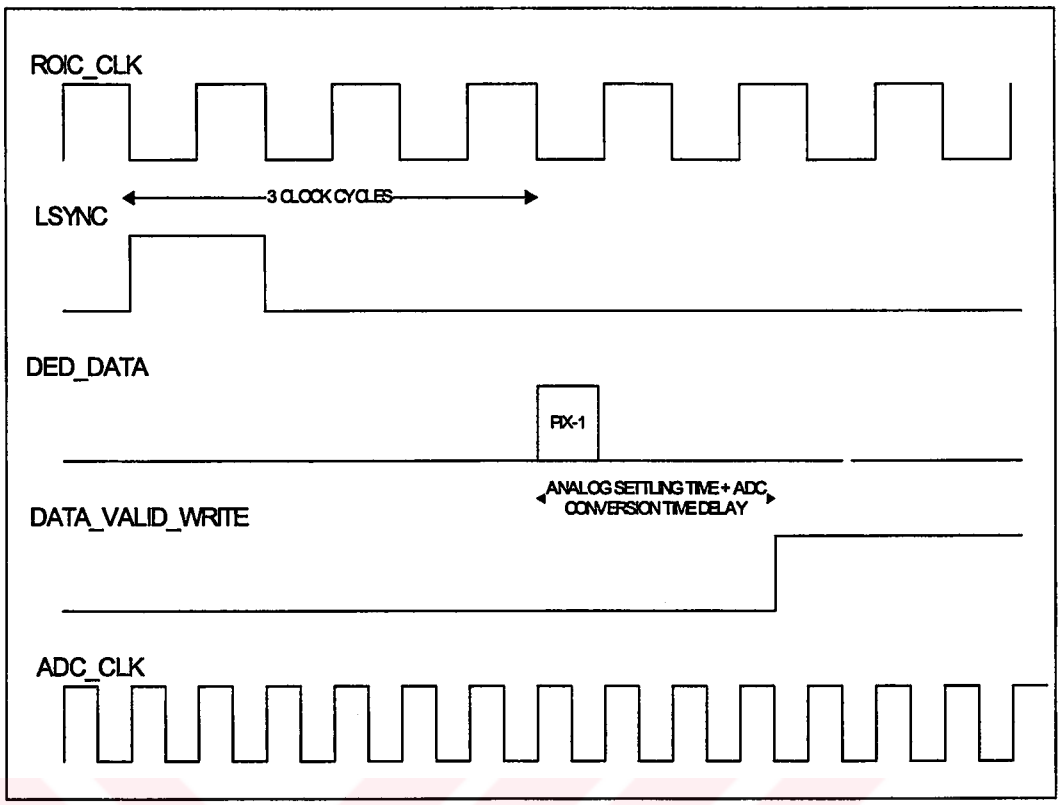

Figure 4.13 DATA_VALID_WRITE timing diagram.

4.2.4 Buffer Memory Read Block

In this section, buffer memory read block of the FPGA logic is presented. The functional description, the pin descriptions (Table 4.4) and operation of the block are explained.

4.2.4.1 Buffer Memory Read Block Functional Description

Buffer memory read block, reads the one frame of processed 8 bit video from the buffer memory. This block generates the required buffer memory address and control signals. During the video active time the pixels are read from the buffer memory and sent to the video digital-to-analog converter.

4.2.4.2 Buffer Memory Read Block I/O Description

The pinout of the buffer memory read block is shown in Figure 4.14. This block has four input pins and four output pins. It has an interface to the buffer memory.

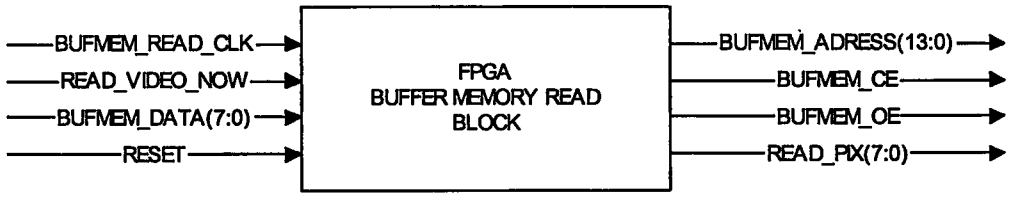

Figure 4.14 Pinout of the buffer memory read block.

Table 4.4 Pin description of the buffer memory read block.

RESET	Input	Global reset signal for registers
BUFMEM_READ_CLK	Input	5 MHz clock signal
READ_VIDEO_NOW	Input	Indicates the correct time to read video data from the memory
BUFMEM_DATA	Input	Buffer Memory 8 bit data bus
READ_PIX	Output	8 bit pixel data read from the memory
BUFMEM_CE	Output	Buffer Memory active low chip enable pin
BUFMEM_WE	Output	Buffer Memory active low output enable pin
BUFMEM_ADRESS	Output	Buffer Memory 14 bit address bus

4.2.4.3 Operation of Buffer Memory Read Block

The pixel data to be displayed on monitor is read from the buffer memory. The reading operation is synchronized to the CCIR video timings. The READ_VIDEO_NOW signal indicating the correct time of reading provides this synchronization.

When it is time to read pixel data from the buffer memory, READ_VIDEO_NOW signal is at logic high level. The logical not of this signal is used to produce the chip enable and output enable of the buffer memory.

In the addressing of the memory, a 14 bit counter is used. This counter increments at the rising edge of the clock as long as READ_VIDEO_NOW signal is at logic high level. The READ_VIDEO_NOW signal is at logic high level for 128 clock cycles for each line of video. Since there are 128 lines during a frame there exists 128 READ_VIDEO_NOW at logic high events. So the counter counts from 0 to 16384 during a frame. For one frame, with 128 by 128 resolution detector array, 16384 pixels are acquired. Hence this counter can address all the detector data.

While chip enable and output enable pins of the memory at logical low level, by the each address bus change, the memory outputs the 8 bit data residing in the specified address 20 ns after change event. This timing should be taken into account to latch the memory data bus correctly. The address is changed on the rising edge of the BUFMEM_READ_CLK signal, and data bus is latched on the next rising edge of the BUFMEM_READ_CLK signal (Figure 4.15). The block diagram of this block is given in Figure 4.16.

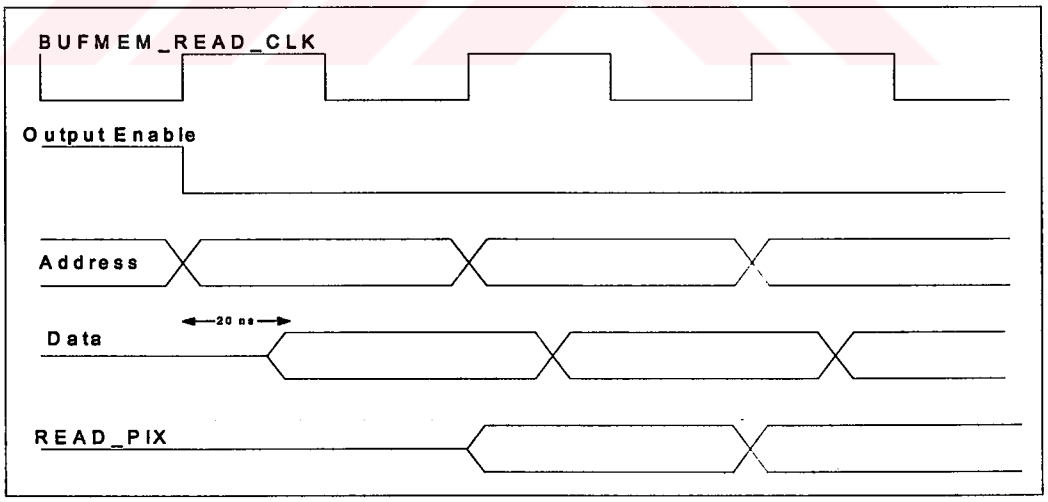

Figure 4.15 Memory read timing.

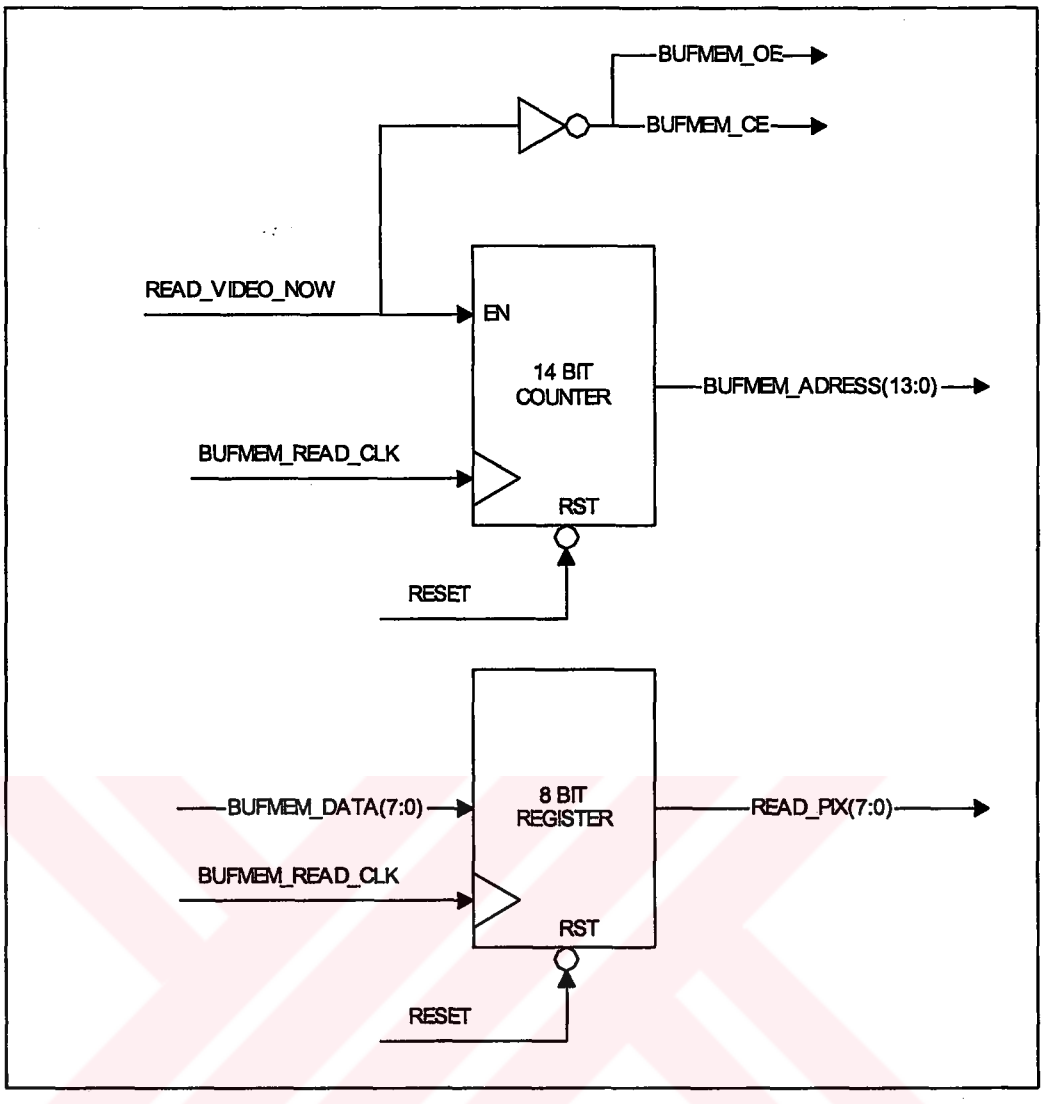

Figure 4.16 Buffer memory read block diagram.

4.2.5 CCIR Timing Block

In this section, CCIR timing block of the FPGA logic is presented. The functional description, input output pin declaration, the pin descriptions (Table 4.5) and the operation of the block are explained. This block is responsible for the generation of the timing signals that is used by video digital-to-analog converter to insert the monitor synchronization pulses.

4.2.5.1 CCIR Timing Block Functional Description

CCIR timing generation block generates the required timing signals to form the analog video complying CCIR standard. The monitor requires these timing signals to control scanning of the image on the display. Another signal generated by this block is DATA_VALID_READ, which determines the time to read detector data in the memory.

4.2.5.2 CCIR Timing Block I/O Description

The pinout of the CCIR timing block is shown in Figure 4.17. It has two input pins and four output pins. This block has interface to VDAC device.

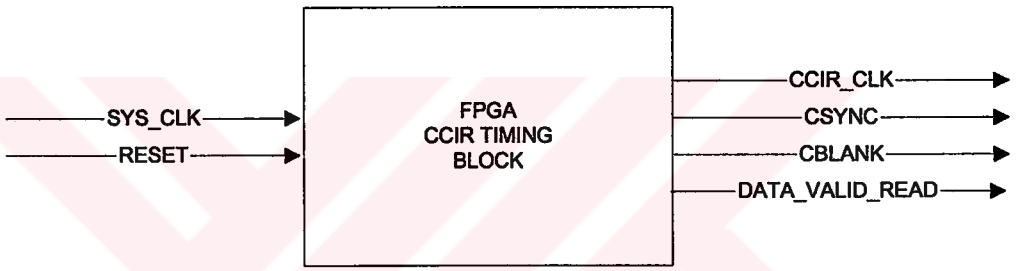

Figure 4.17 Pinout diagram of CCIR timing block.

Table 4.5 Pin description of CCIR timing block.

RESET	Input	Global reset signal for registers
SYS_CLK	Input	40 MHz on board oscillator clock signal
DATA_VALID_READ	Output	Indicates the correct time to read the detector data from the buffer memory
CSYNC	Output	Monitor synchronization signal
CBLANK	Output	Monitor blanking signal
CCIR_CLK	Output	10 MHz video timing clock signal

4.2.5.3 Operation of CCIR Timing Block

Analog video standard used in this design is CCIR (International Radio Consultative Committee). CCIR standard defines the video frequency characteristics for 625 line colour or monochrome display system.

Composite picture signal results from combining a blanked picture video signal with the blanking pulse and synchronizing signal. Blanking level is that level of a composite picture signal, which separates the range containing picture information from the range, containing synchronizing information. Synchronizing signal is employed for the synchronization of the interlaced scan process. Interlace is the positioning of the scan lines of alternate fields that form the frame so that even field lines are vertically spaced between the odd field lines.

VP&SC FPGA generates the CSYNC and CBLANK signals according to the specifications given in Table 4.6 and Figure 4.18 and sends it to the VDAC where composite analog video is formed.

Table 4.6 CCIR standard characteristics.

Characteristics	CCIR Standard
Number of lines per frame	625 (575 active)
Line frequency	15625 Hz
Field frequency	50 Hz
Frame frequency	25 Hz
Scan direction	Left to right Top to bottom
Interlace	2:1
Nominal duration of line	64 us
Line blanking period	12 us
Front porch	1.5 us
Line synchronizing pulse	4.7 us
Field blanking period	1612 us

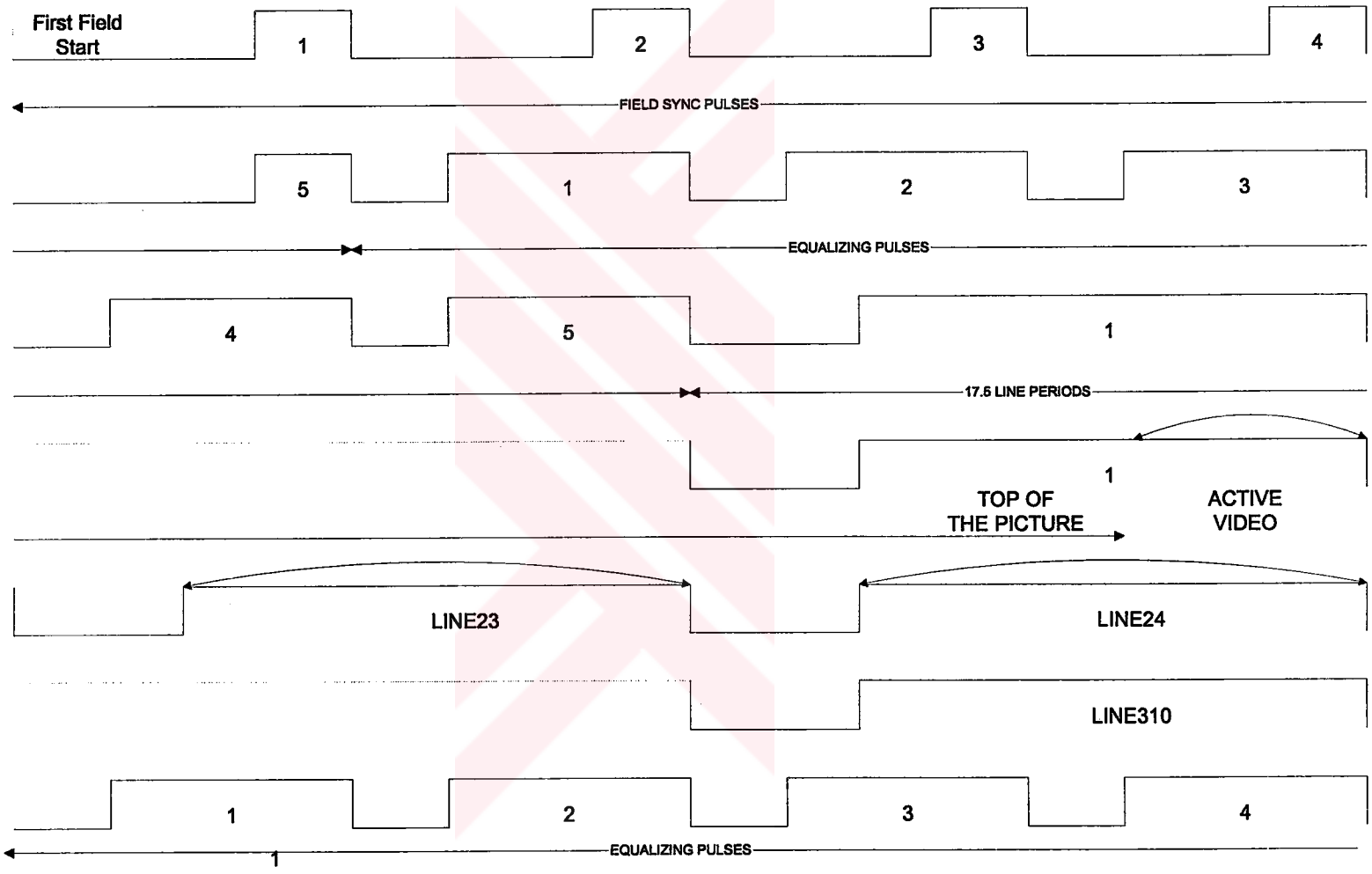

Figure 4.18 CCIR composite video first field.

Figure 4.19 CCIR composite video second field.

4.2.6 Initialization Block

In this section, initialization block of the FPGA logic is presented. The functional description, the pin descriptions (Table 4.7) and operation of the block are explained.

4.2.6.1 Initialization Block Functional Description

Initialization block is responsible for the transfer of the nonuniformity correction coefficients from the flash memory to the SRAMs where the coefficients are read during real-time processing. The operation starts with power on, and during initialization the access of other blocks to the memories are prevented by INITIALIZATION_FIN signal which informs the other blocks about the end of initialization. This block generates the required flash memory and SRAM address and control signals.

4.2.6.2 Initialization Block I/O Description

The pinout of the initialization block is shown in Figure 4.20. It has three input pins and twelve output pins. It has interface to the flash memory, offset correction memory, and gain correction memory.

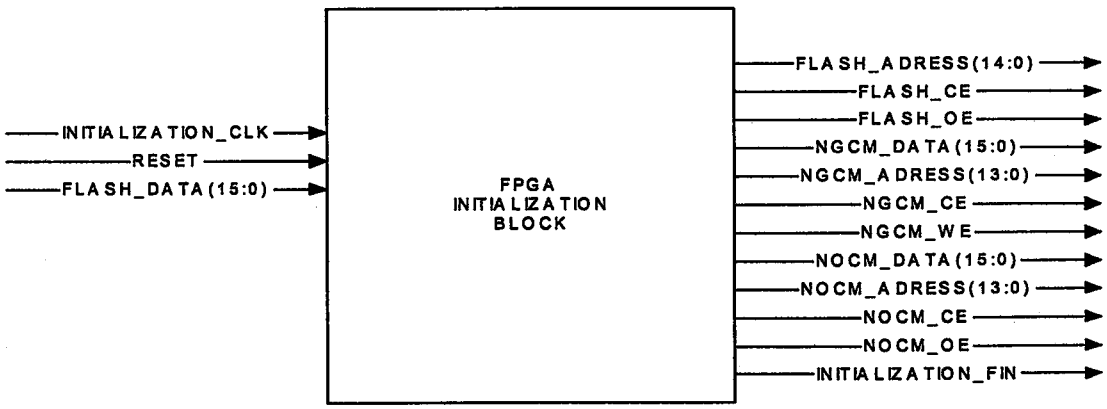

Fig.4.20 Pinout diagram of initialization block.

Table 4.7 Pin description of initialization block.

RESET	Input	Global reset signal for registers
INITIALIZATION_CLK	Input	5 MHz clock signal
FLASH_DATA	Input	16 bit flash memory data bus
FLASH_ADRESS	Output	15 bit flash memory address bus
FLASH_OE	Output	Flash memory output enable
NGCM_DATA	Output	16 bit NUC gain memory data bus
NGCM_ADRESS	Output	14 bit NUC gain memory address bus
NGCM_CE	Output	NUC gain memory chip enable
NGCM_WE	Output	NUC gain memory write enable
NOCM_DATA	Output	16 bit NUC offset memory data bus
NOCM_ADRESS	Output	14 bit NUC offset memory address bus
NOCM_CE	Output	NUC offset memory chip enable
NOCM_WE	Output	NUC offset memory write enable
INTIALIZATION_FIN	Output	Indicates the end of initialization

4.2.6.3 Operation of Initialization Block

The two point nonuniformity correction gain and offset coefficients are stored in the nonvolatile flash memory. Since flash memory is low speed to make the processing faster the coefficients are transferred to the high speed SRAMs.

The transfer is controlled by a state machine. There are 16384 offset coefficients in the flash memory and their address range is from 0000 (Hex) to 3FFF (Hex). The state machine firstly transfers the offset coefficients. The FPGA sequentially address the flash memory, reads and latches the coefficient from the data bus of the flash memory. The latched coefficient is then put on the SRAM data bus, the address and write enable pins are set accordingly hence the transfer is achieved. After 16384 offset coefficients are transferred, the state machine initiates the transfer of gain coefficients, which reside in the address range of 4000 (Hex) to 7FFF (Hex) of the flash memory. After the transfer of 16384 gain coefficients, initialization process finishes. The state machine informs other blocks of the FPGA about the end

of the initialization process by setting the INITIALIZATION_FIN signal to a high level (Figure 4.21).

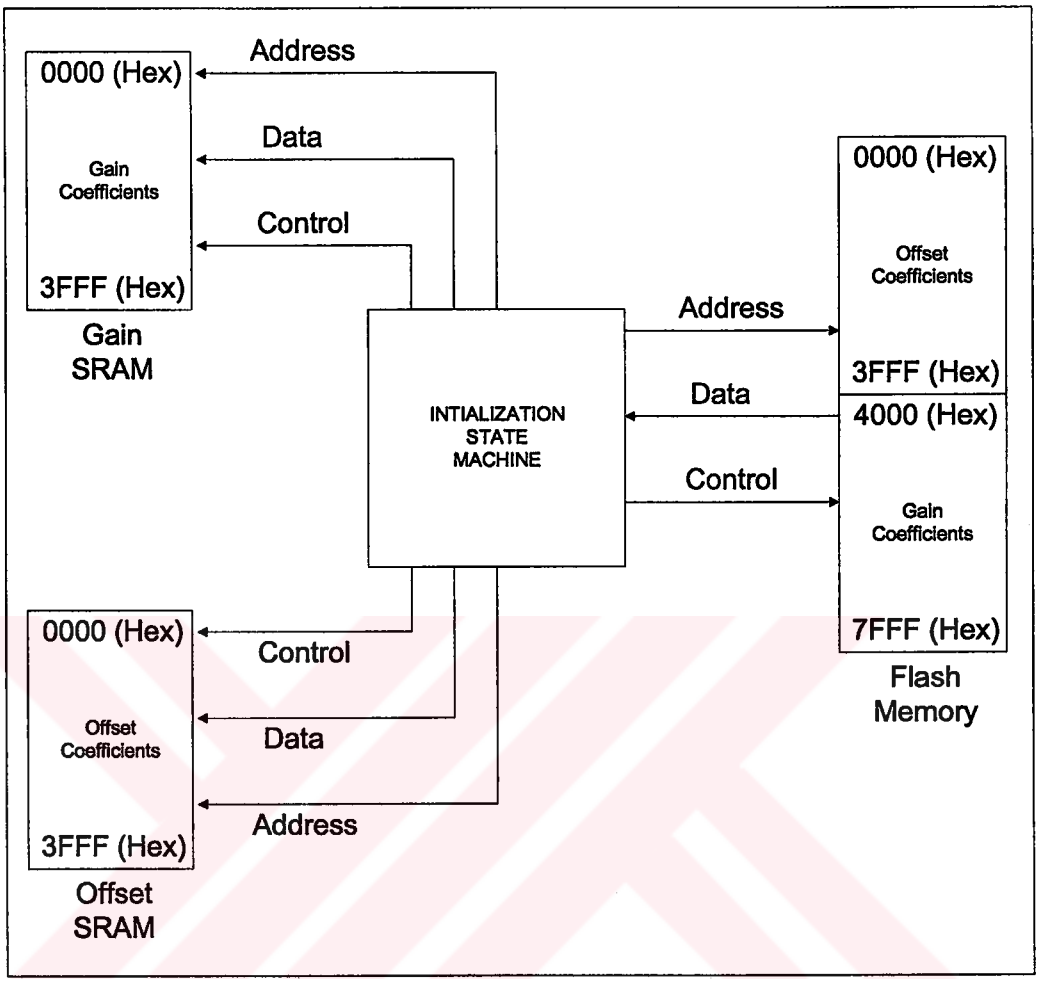

Figure 4.21 Block diagram of initialization.

4.2.7 Serial Communication Block

In this section, serial communication block of the FPGA logic is presented. The functional description, the pin descriptions (Table 4.8) and the operation of the block are explained. For the communication between the video processing and system control board and the front-end electronics board, a serial communication protocol operating at 9600 baud rate is developed.

4.2.7.1 Serial Communication Block Functional Description

Serial communication block establishes the serial communication between front-end electronics PCB and video processing and system control PCB. It is composed of asynchronous transmit and receive blocks. The transmission baud rate is 9600 bits/sec.

4.2.7.2 Serial Communication Block I/O Description

The pinout of the serial communication block is shown in Figure 4.22. It has four input pins and two output pins. The pins provide the communication channel between the boards.

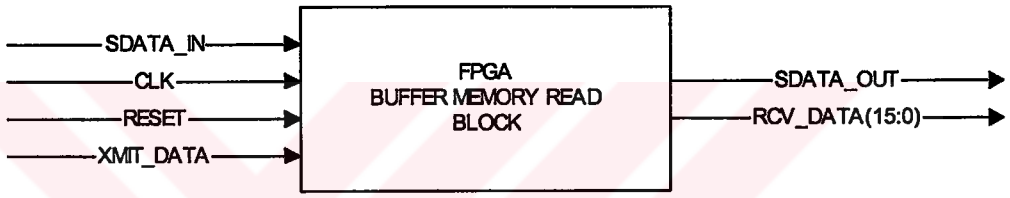

Fig.4.22 Pinout diagram of serial communication block.

Table 4.8 Pin description of serial communication block.

RESET	Input	Global reset signal for registers
CLK	Input	5 MHz clock signal
SDATA_IN	Input	Input serial data
XMIT_DATA	Input	16 bit data to be transmitted
SDATA_OUT	Output	Output serial data
RCV_DATA	Output	16 bit received data

4.2.7.3 Operation of Serial Communication Block

The serial data protocol is as shown in Figure 4.24. The transmission line is at logic high level when idle. The start bit, logic low level of one bit duration, indicates the start of the transfer. Then serialized 16 bit data is transmitted over the line. The

least significant bit of the 16 bit data is transmitted first. After 16 bit data, the stop bit, a logic high level of one bit duration, is asserted on the line.

A state machine is designed to control the operation of the transmitter. Transmitter state machine is in idle state till the rising edge of the frame synchronization signal. In the active states, a counter is used to control 9600 baud rate. Firstly, the start bit, a logical low pulse is sent to the line. The 16 bit parallel data is serialized through a shift right register working at the speed of the baud rate. After transfer of 16 bit data, the stop bit, a logical high pulse is sent to the line.

Receiver operation is controlled by another state machine. The state machine is in idle state till it senses a high to low transition in the line which signals the start of the transfer. In the next 16 clock cycles the serial input data is fed to the input of a shift right register, where serial to parallel conversion is achieved. After 16 bit data is achieved, the state machine goes to the idle state to wait for another transfer.

The user can select the readout integration time through a potentiometer on the FE PCB. The FE PCB digitizes and serializes this information before sending to VP&SC PCB. The serial communication block converts this information to parallel and sends it to the readout control block which generates the detector frame synchronization signal.

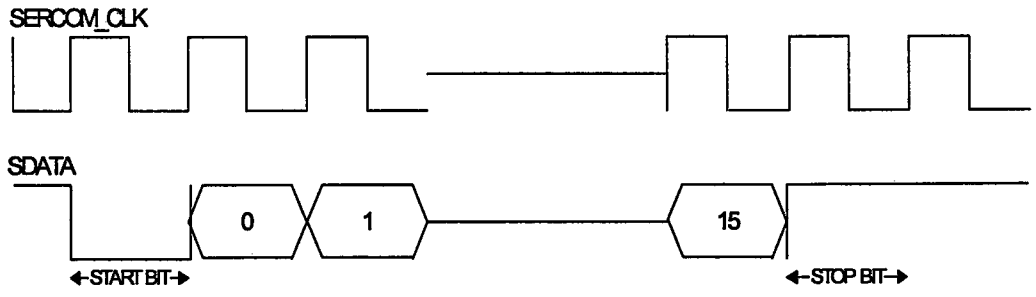

Figure 4.23 Serial transmission protocol.

4.2.8 Symbology Insertion Block

In this section, symbology insertion block of the FPGA logic is presented. The functional description, the pin descriptions (Table 4.9) and operation of the block are explained.

4.2.8.1 Symbology Insertion Block Functional Description

Symbology insertion block produces the necessary control and address signals to read the symbology information and using this information it generates the select signal for video multiplex operation.

4.2.8.2 Symbology Insertion Block I/O Description

The pinout of the symbology insertion block is shown in Figure 4.24.This block has four input pins and four output pins. Some of the out pins go to flash memory and some of them go to the video multiplexer block.

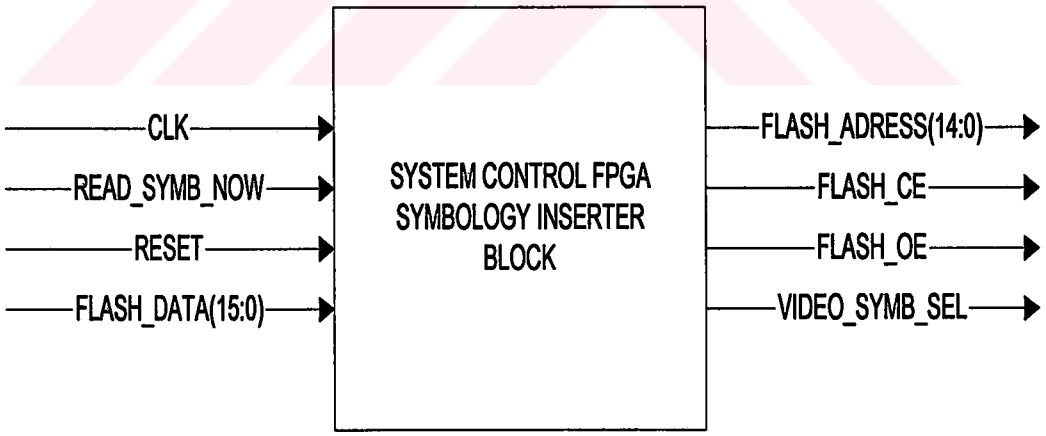

Fig.4.24 Pinout diagram of symbology insertion block.

Table 4.9 Pin description of symbology insertion block.

RESET	Input	Global reset signal for registers
CLK	Input	5 MHz clock signal
READ_SYMB_NOW	Input	Input serial data
FLASH_DATA	Input	16 bit Flash data
FLASH_ADRESS	Output	15 bit Flash address bus
FLASH_CE	Output	Flash chip enable
FLASH_OE	Output	Flash output enable
VIDEO_SYMB_SEL	Output	Video multiplex select

4.2.8.3 Operation of Symbology Insertion Block

The symbology memory map is kept in the flash memory. One word of the flash memory is 16 bits. Each bit of the flash data in the symbology region holds the video multiplex information of the corresponding pixel on the scene. A region of 256x128 pixels are in the symbology memory map so 2048 (256x128/16) places in the flash memory is reserved for symbology insertion.

Two state machines control the operation of this block. One state machine is responsible for reading the symbology information synchronized to the CCIR timings from the flash memory. The other state machine takes the data read and produces the video multiplex select signal. The synchronization between CCIR timings and read operation is achieved by the READ_SYMB_NOW signal. It goes to logical high level when it is time to read data. For each line there are 256 pixels, so for each line 16 flash words are read, for this duration of time READ_SYMB_NOW stays at high level. The state machine produces the flash memory address and control signals as long as READ_SYMB_NOW is at high level. The other state machine takes the 16 bit data, and by shifting it to the right synchronous with CCIR timings. The least significant bit of the shift register is used as the video multiplex select signal.

4.2.9 Coefficient Reader Block

In this section, readout timing block of the FPGA logic is presented. The functional description, the pin descriptions (Table 4.10) and operation of the block are explained. This block is responsible for the transfer of the nonuniformity coefficients from the flash memory to the SRAMs.

4.2.9.1 Coefficient Reader Block Functional Description

During two point nonuniformity correction, the correction coefficients are read from the SRAMs. Coefficient reader block generates the required SRAM address and control signals to read the coefficients in a way synchronized to the valid detector data flow. The thirteenth bit of the data read from NUC gain memory holds the pixel substitution information which is evaluated by the NUC block.

4.2.9.2 Coefficient Reader Block I/O Description

The pinout of the coefficient reader block is shown in Figure 4.25. This block has five input pins and nine output pins. Some of the out pins go to offset correction memory and some of them go to gain correction memory.

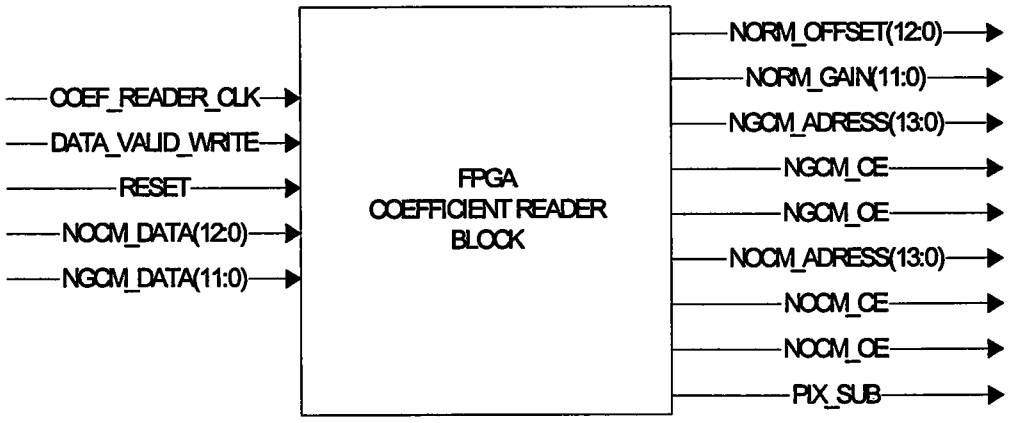

Fig.4.25 Pinout diagram of coefficient reader block.

Table 4.10 Pin description of coefficient reader block.

RESET	Input	Global reset signal for registers
COEF_READER_CLK	Input	5 MHz clock signal
NGCM_DATA	Input	12 bit NUC gain memory data bus
NOCM_DATA	Input	13 bit NUC offset memory data bus
DATA_VALID_WRITE	Input	Indicates the detector data is valid
NGCM_ADRESS	Output	14 bit NUC gain memory address bus
NGCM_CE	Output	NUC gain memory chip enable
NGCM_OE	Output	NUC gain memory output enable
NORM_OFFSET	Output	13 bit offset coefficient
NORM_GAIN	Output	12 bit gain coefficient
NOCM_CE	Output	NUC offset memory chip enable
NOCM_OE	Output	NUC offset memory output enable
NOCM_ADRESS	Output	14 bit NUC offset memory address bus
PIX_SUB	Output	Pixel substitution indicator

4.2.9.3 Operation of Coefficient Reader Block

The two point nonuniformity correction gain and offset coefficients are read from the SRAMs during system operation. The critical issue is to synchronize the reading of the coefficients to the detector data flow in the system. The coefficients read should belong to the correct detector pixel.

DATA_VALID_WRITE signal at logical high level shows that the detector data entering to the nonuniformity correction block is valid. The logical not of this signal is used to generate the output and chip enable signals of the offset coefficient SRAM. A 14 bit counter is used to address the SRAM. The counter increments as long as the DATA_VALID_WRITE signal at logical high level. Since there are 16384 detector data for a frame, the counter is reset when its value reaches to 16384. The SRAM outputs the data 20 ns after the address change. This data is latched on the rising edge of the clock and sent to the two point nonuniformity correction block as the offset data. The gain correction is done one clock cycle after the offset correction. Because of this, the gain coefficient SRAM control and address signals

are one clock cycle delayed versions of the offset coefficient SRAM. The data bus of this SRAM is latched at the rising edge of the clock and sent to the two point nonuniformity correction block as the gain data. The thirteenth bit of the data read from NUC gain memory, named PIX_SUB, holds the pixel substitution information .Pixel substitution information is used by NUC block to make the pixel substitution decision.

4.3 Summary

In this chapter, the digital design embedded in the FPGA that implements the video processing and system functions of the board are presented. The functional description and the block diagrams of the FPGA software are given. The design details and the operation of the blocks are explained. In the next chapter, the integration and test of the infrared imaging system developed at METU will be presented. System functions, real time imaging, nonuniformity correction, electronic zoom, and symbology insertion tests and their results will be presented.

CHAPTER 5

SYSTEM INTEGRATION AND TEST

5.1 Introduction

To test our thermal imaging system, the detector dewar assembly containing the focal plane array and readout circuitry, the front-end electronics board and the video processing and system control board are integrated (Figure 5.1). Before system integration, the operation of the boards is verified by use of the PC controlled test software. The test software stimulated the VP&SC board by controlling the FE board's FPGA, and operation of the board is verified by means of examining the on board signals thoroughly using an ossiloscope, a logic analyzer and an analog monitor. Different test patterns sent by the FE board FPGA are displayed on the monitor to verify the operation. Some synchronization and memory access mistakes are discovered by this method and cases are clarified by probing the FPGA signals by logic analyzer. The VDAC device is tested by sending 8 bit digital data covering the 0 to 255 input span and by observing the video signal going to the monitor by ossiloscope. The digital signals controlling the readout device and FE board are also checked by means of ossiloscope.

After verification of the boards, the system integration has been completed. To better see the improvements, a highly nonuniform focal plane array with relatively large number of bad pixels were chosen for integration. Due to the low responsivity and high dark current, the detector was sensitive to objects at temperatures higher than 300 K. High nonuniformity and low responsivity of the focal plane array was due to nonstandard nature of the array where InSb array on Si substrate was grown

under highly lattice mismatched conditions. Therefore, hot objects such as candle light and soldering iron have been used as targets. The analog video is recorded by a PAL recorder and transferred to a PC by a frame grabber. The test results are presented in the following section.

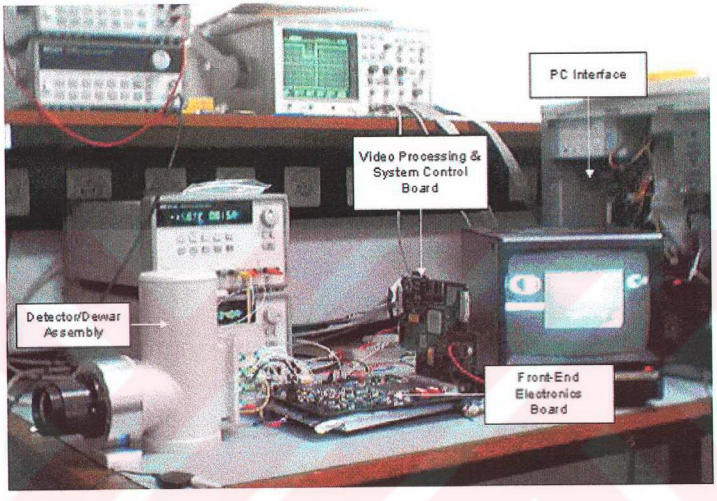

Figure 5.1 Setup for testing the infrared imaging system includes detector/dewar assembly, front-end electronics board, video processing and system control board, analog monitor, and a PC.

5.2 Test Results

VP&SC board has been tested first with test patterns seen below.The first pattern mimics the detector data as going from the dark level to light level in the direction top to bottom (Figure 5.2).The second test pattern mimics the detector data

as going from the dark level to light level in the direction of left to right and returns to dark at the end (Figure 5.3).

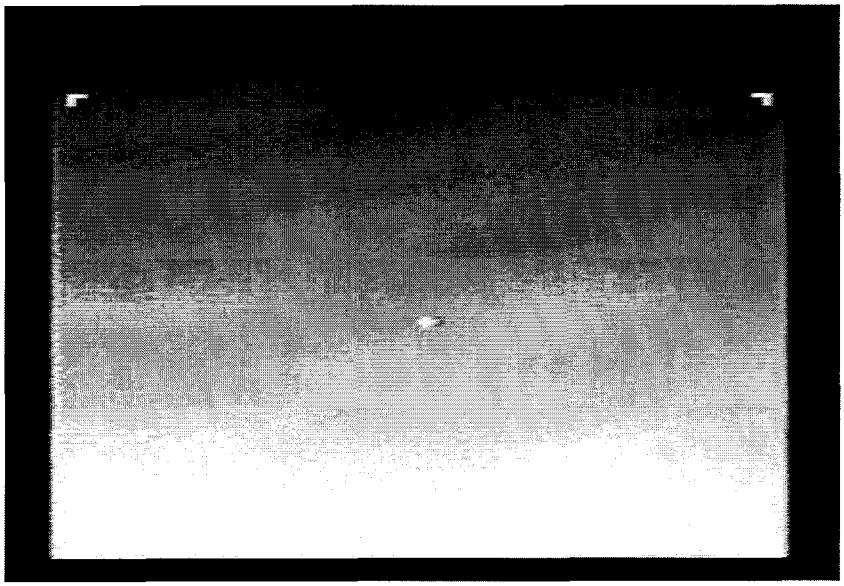

Figure 5.2 Test pattern 1.

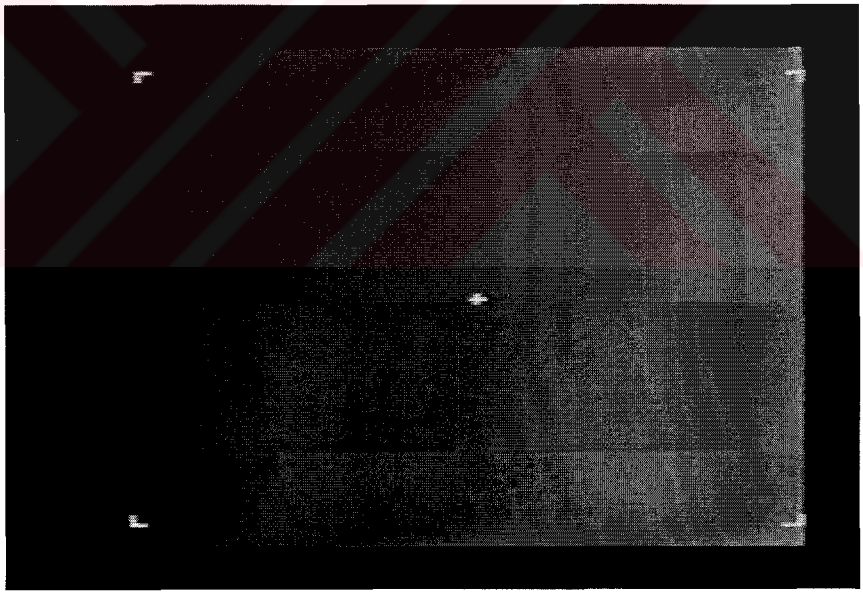

Figure 5.3 Test pattern 2.

The system has x2 electronic zoom capability. The zoom in horizantal direction is achieved by increasing the duration of the pixel change time by two

during reading video data from buffer memories. The zoom in vertical direction is achieved by reading the same detector frame data in both odd and and even fields of the video.

The system also has symbology insertion capability (Figure 5.4).The symbology memory map is held in the flash memory. While reading detector data, concurrently, the symbology information is retrieved from the flash memory. Depending on the symbology information, detector data and symbology data are multiplexed.

Figure 5.4 Symbology insertion on analog monitor.

The operation of the VDAC device is tested by applying 8 bit digital data and observing the analog video signal as seen in Figure 5.6.

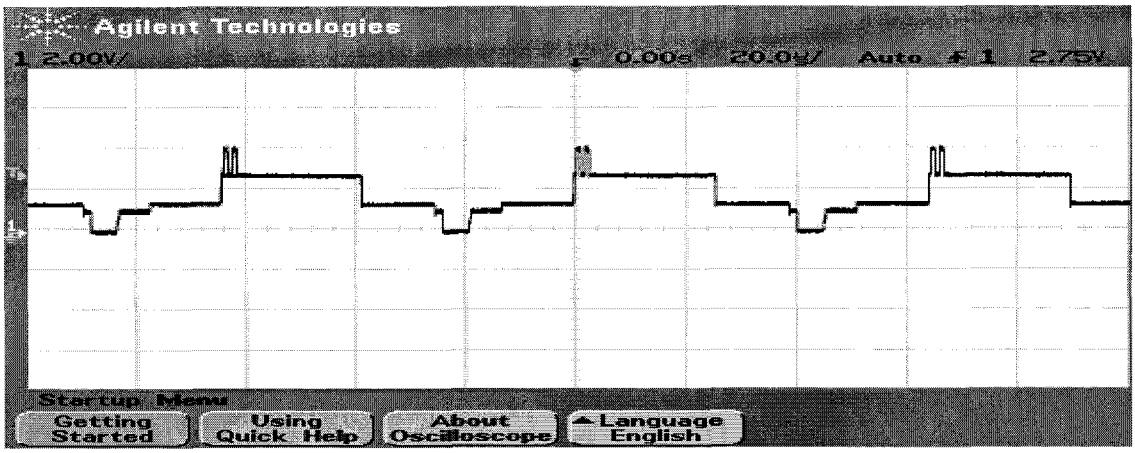

Figure 5.5 Analog video on oscilloscope.

To enhance the image quality, VP&SC board applies real-time nonuniformity correction and pixel substitution on the raw detector data. The coefficient calculations are made off line by a Matlab software. The software applies nonuniformity correction algorithms on calibration data, and writes the 16 bit coefficients to a text file in binary format. The detector pixels having coefficients too low or too high (i.e. less than 0.5 or greater than 2) are defined as bad pixels. The software sets the thirteenth bit of the gain coefficient to 1 for bad pixels. After the coefficients are calculated, the flash programmer software reads coefficients text file and sends this data to the VP&SC FPGA through serial port. The embedded flash programming logic in the FPGA converts serial data to parallel and takes care of the flash programming procedure. To be able to see the effects of processing, the processing operation can be bypassed by the user through an on board switch. In Figure 5.6, unprocessed thermal image taken with FPA looking at 300 K background is presented, showing that the FPA is highly uniform.

Figures 5.7 and 5.8 show the thermal image of a candle light with processing disabled and enabled, respectively. Application of two-point offset and gain correction substantially improves the image quality. Further improvements can be

achieved by incorporating dynamic range compression [16, 17] which can be implemented in the course of a future study.

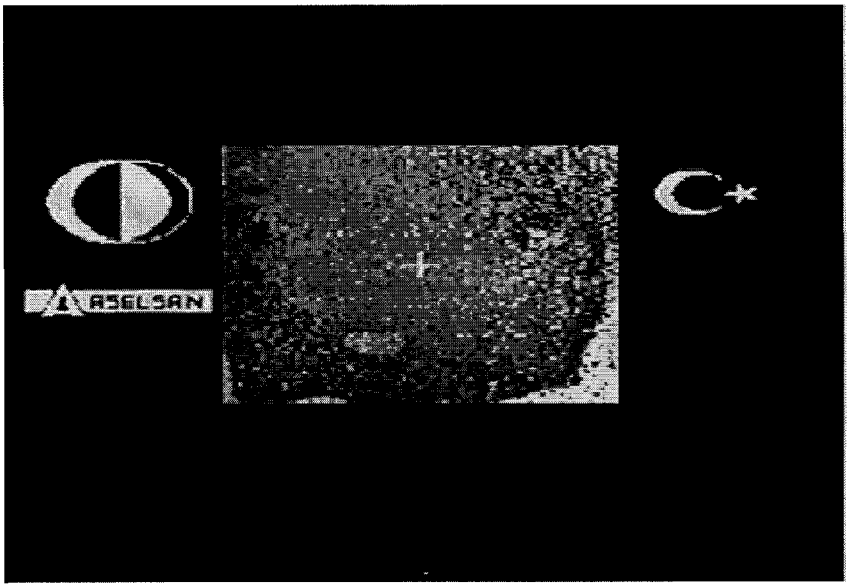

Figure 5.6 Unprocessed thermal image with FPA looking at 300 K background.

Figure 5.7 Unprocessed thermal image with FPA looking at candle light.

Figure 5.8 Processed thermal image with FPA looking at candle light.

5.3 Summary

In this chapter, the integration and test of the infrared imaging system developed at METU is presented. System functions, real time imaging, nonuniformity correction, electronic zoom, and symbology insertion are tested and the results are presented. In the next chapter, the conclusion of the study and future work will be presented.

CHAPTER 6

CONCLUSION AND FUTURE WORK

This study reports the design and implementation of a video processing and system control board to construct a compact real time thermal imager. The board is integrated with a detector/dewar assembly, a front-end electronics board, and a video display unit to form a prototype infrared imaging system for 128x128 staring focal plane arrays. This is the first national thermal imager designed and implemented for a staring focal plane array. The functions of the video processing board includes frame buffering, CCIR video generation, two point nonuniformity correction (NUC), image freeze, electronic zoom and symbology insertion. This study can be divided into four phases; i) conceptual development and system engineering of the thermal imager electronics, ii) design and implementation of printed circuit board, iii) design and development of the FPGA software, iv) system integration and testing.

The system test has been performed using a highly nonuniform 128x128 InSb focal plane array with a relatively large number of bad pixels and successful operation has been verified. The imaging system can achieve a frame rate up to 550 Hz with 128x128 focal plane arrays coupled to commercially available Indigo 9806 read-out integrated circuits. The maximum supported standard focal plane array format is 320x256 at frame rates up to 100 Hz. Under typical operating conditions, the system performance is limited by the detector and the read-out circuit where the noise level of the system is dominated by these components.

In the course of a future study, further improvement of the image quality by means of other image processing techniques such as 2-D filtering and video range compression can be targeted. By the use of these processing techniques, edge enhanced and sharper images can be acquired. With modifications in the FPGA software such as increasing the depth of the address counters, choosing a higher operating clock frequency, adjusting the readout timing parameters, systems supporting higher resolution detector formats can be developed.

REFERENCES

[1] Fatih IŞIK, *"Design of Front-end Electronics Board for a Compact Thermal Imager,"* MS. Thesis, Middle East Technical University, 2002.

[2] Gerald C. Holst, *"Testing and Evaluation of Infrared Imaging Systems,"* Co published by JCD Publishing and SPIE Press, 1998.

[3] Gerald C. Holst, *"CCD Arrays Cameras and Displays,"* p. 22, Co published by JCD Publishing and SPIE Press, 1998.

[4] T.S Villani, K.A. Loesser, S.N Perna, D.R. McCarthy and F.P. Pantuso, *"A compact high-performance MWIR camera with exposure control and 12-bit video processor,"* Proceedings SPIE, Vol.3379, pp 307-312, 1998.

[5] Henry W. (Bill) Neal, *"Advanced Uncooled Infrared System Electronics,"* Proceedings SPIE, Vol. 3379, pp 126-138, 1998.

[6] Lee W. Ritchey and James C. Blankenhorn, *"High Speed PCB Design,"* published by SMT Plus Inc, 1996.

[7] Indigo Systems, ISC9806 Standard 128 User's Guide, Version 1.3, 400-9806-10.

[8] Howard Johnson and Martin Graham, *"High Speed Digital Design,"* published by Prentice Hall Inc, 1993.

[9] Xilinx, The Programmable Logic Data Book, 1999.

[10] White EDC, EDI816C256CA Datasheet, 05055501.pdf, available at www.whiteedc.com, 2000.

[11] Analog Devices, ADV7120 Datasheet, adv7120.pdf, available at www.analog.com, 1999.

[12] Analog Devices, AD812 Datasheet, ad812_b.pdf, available at www.analog.com, 1998.

[13] Cypress, CY7C109 Datasheet, 30-05038.pdf, available at www.cypress.com, 2002.

[14] AMD, 29F800BB Datasheet, 21504.pdf, available at www.amd.com, 2002.

[15] Atmel, AT17C010 Datasheet, doc2321.pdf, available at www.atmel.com, 2002.

[16] Gabby Sarusi, Natan Ziv, O. Zioni, J. Gaber, M. Schechterman, I. Wiess, I. Friedland, M. Lerner, and A. Friedenberg, " "TADIR" El-Op's High Resolution Second Generation 480x4 TDI Thermal Imager," Proceedings SPIE, Vol. 3436, pp 199-201, 1998.

[17] Vigil E. Vickers, "Plateau equalization algorithm for real-time display of high quality infrared imagery," Opt. Eng. 35, 1996.

APPENDIX A

PCB LAYOUT OF VP&SC PCB

The video processing board has been designed using eight layers. Four of the layers have been used for signal routing, three of the layers have been used for ground distribution, and one layer has been used for power distribution. In the following sections, these layers are presented.

A.1 Component Layer

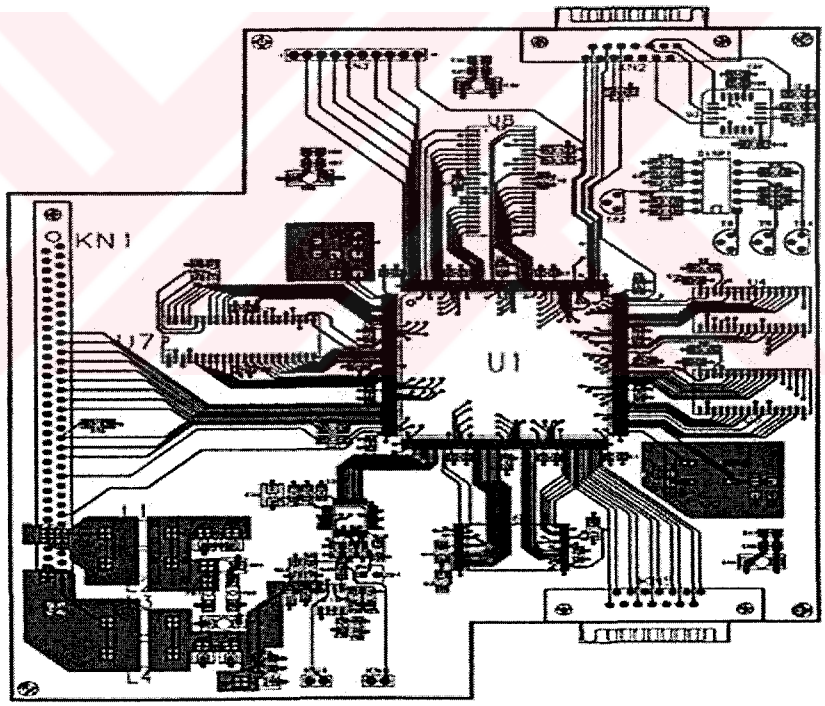

Figure A.1 Component layer of VP&SC PCB

A.2 Ground Layer

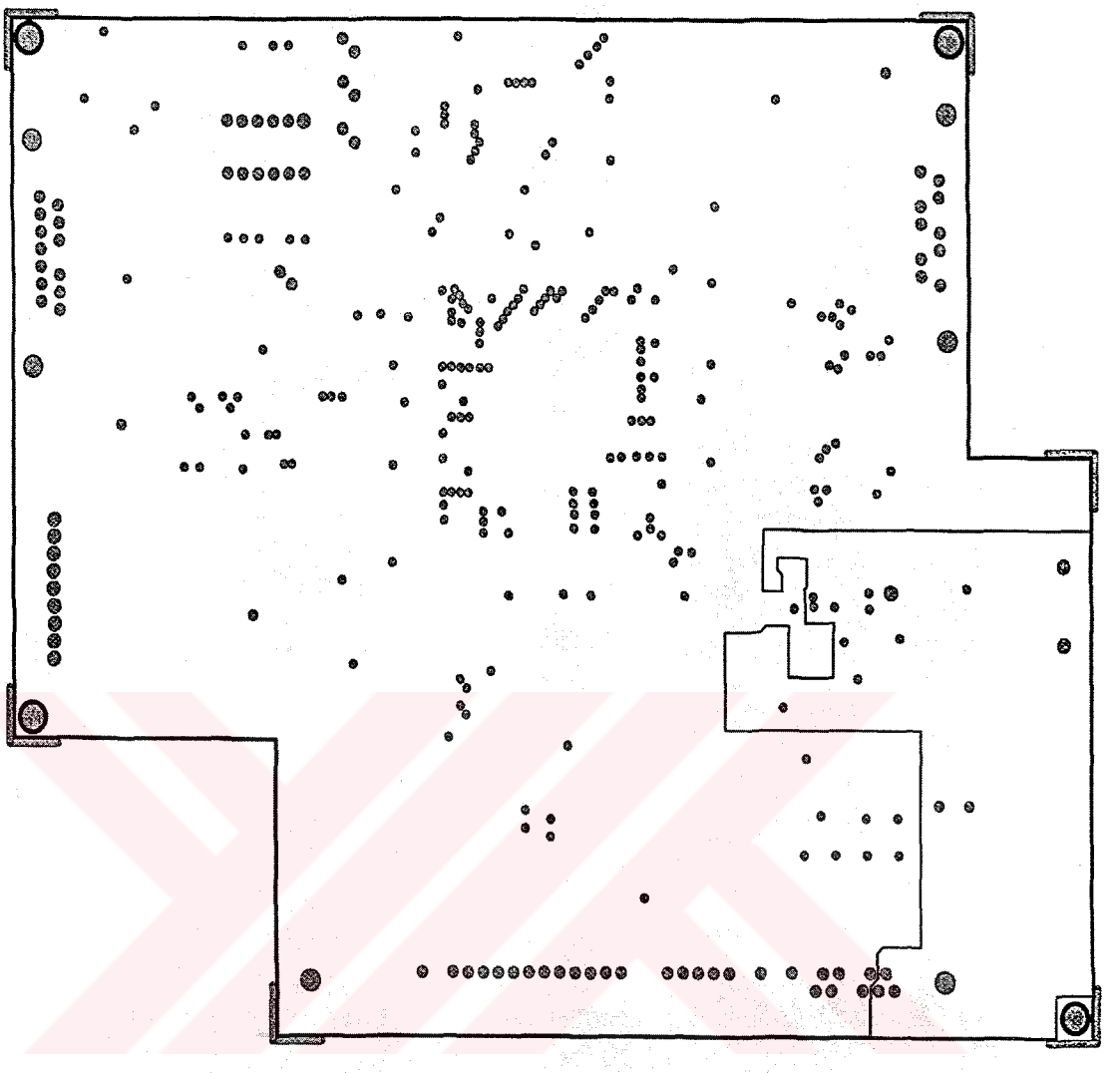

Figure A.2 Ground layer of VP&SC PCB

A.3 Power Layer

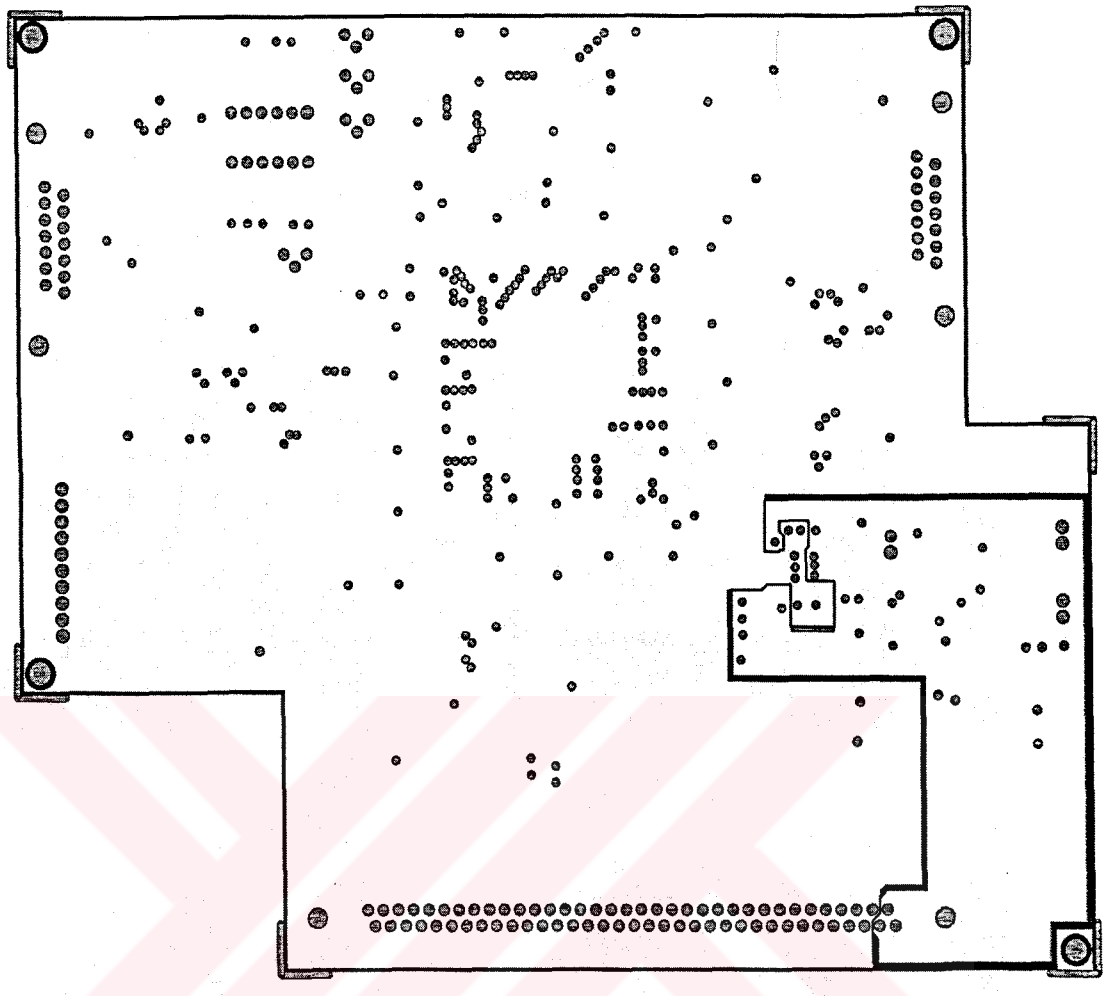

Figure A.3 Power layer of VP&SC PCB