THE ANALYSIS OF A DYNAMIC VOLTAGE RESTORER BASED ON LOAD SIDE CONNECTED SHUNT CONVERTER TOPOLOGY

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ÇAĞRI ACAR

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Prof. Dr. Tayfur Öztürk
Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

Prof. Dr. Mübeccel Demirekler
Head of Department

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

Prof. Dr. Muammer Ermiş
Supervisor

Examining Committee Members

Prof. Dr. Nevzat Özay

Assoc. Prof. Dr. Işık Çadırcı

Dr. Erbil Nalçacı

M.Sc. Faruk Bilgin

Prof. Dr. Muammer Ermiş

ABSTRACT

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ACAR, Çağrı
M.Sc., Department of Electrical and Electronics Engineering
Supervisor: Prof. Dr. Muammer Ermiş

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Complexity of the instruments used in the industry is increasing day by day due to the economic pressures to automate processes and improve efficiency, which results in the loads more sensitive to the voltage sags. Generally, voltage sags are caused by fault conditions on the system, therefore they may not be avoided completely. The Dynamic Voltage Restorer (DVR) is a series power electronics device which is designed to mitigate the voltage sags in the power systems. The primary advantage of the DVR is that, it is rated at a fraction of the total protected load, thereby yielding a very attractive cost versus benefit advantage.

The aim of this study is to describe the concept of the DVR and analyzing it with load side connected shunt converter topology which protects an 18MVA typical load. The successful operation of the DVR has been shown by simulations carried on PSCAD/EMTDC Software.

Keywords: Power Quality, Series Device, Dynamic Voltage Restorer, Voltage Sag

ÖZ

YÜK TARAFINDAN ŞÖNT BAĞLI ÇEVİRİCİ TOPOLOJİSİ TABANLI BİR DİNAMİK GERİLİM İYİLEŞTİRİCİSİ ANALİZİ

ACAR, Çağrı
Yüksek Lisans , Elektrik-Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Prof. Dr. Muammer Ermiş

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Gün ve gün ekonomik koşullar gereğince işlemlerin otomatize edilmesi ve verimliliğin arttırılması için endüstride gerilim düşümlerine daha duyarlı karmaşık cihazların kullanımı artmaktadır. Genellikle güç sistemlerinde meydana gelen arıza durumlarından kaynaklanan gerilim düşümlerinden tamamen kaçılması imkansızdır. Bu sebepten dolayı güç sistemlerindeki gerilim düşümlerini hafifletmek için, seri bağlantı yapılan bir güç elektroniği cihazı olan Dinamik Gerilim İyileştiricisi (DGİ) tasarlanmıştır. Cihazın temel avantajı, korunan toplam yükün bir kısmı değerinde olacağından dolayı getireceği eder ve kazanç avantajıdır.

Bu çalışmanın amacı, DGİ konusunu tanımlamak ve 18 MVA tipik bir yükü koruyan yük tarafından şönt bağlı çevirici topolojili GDİ'yi analiz etmektedir. Cihazın başarılı bir şekilde çalıştığı PSCAD/EMTDC yazılımında hazırlanan simulasyonlar ile gösterilmiştir.

Anahtar Kelimeler: Güç Kalitesi, Seri Cihaz, Dinamik Gerilim İyileştiricisi, Gerilim Düşümü

to my beloved wife, Feza

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LIST OF ABBREVIATIONS

DVR : Dynamic Voltage Restorer

IGCT : Integrated Gate Commutated Thyristor

PCC : Point of Common Coupling

PLC : Programmable Logic Controller

PLL : Phase Locked Loop

PWM : Pulse Width Modulation

rms : Root Mean Square

SLGF : Single phase line-to-ground fault

SCO : Short Circuit Operation

SRF : Synchronous Reference Frame

THD : Total Harmonic Distortion

VSI : Voltage Source Inverter

CHAPTER 1

INTRODUCTION

Introduction of sensitive loads to the power systems has changed the boundary conditions in the electrical supply industry towards the quality of the electrical supply. Users are deeply interested in the quality of the electrical supply while the utilities are concentrating on utilizing the existing transmission systems more efficiently.

Users need constant sine-wave shape, constant frequency and symmetrical voltage with a constant rms value to ensure the continuity of their production at their site. Among the disturbances that may be observed at a utility grid, the transient power supply interruptions and voltage sags are considered to be the most severe since many of the loads are susceptible and sensitive to temporary changes in the magnitude and phase of the power supply. Voltage depressions in the order of a few milliseconds may bring an entire production line to a standstill, and may cause a considerable amount of economic damage, furthermore the equipments may face the danger of breakdown.

A voltage sag can be loosely defined as a short-duration reduction in voltage magnitude generally caused by a fault somewhere in the system. Voltage sags can be characterized by magnitude and duration, and for many cases they are followed by an unbalance in the phase angle. Despite their short duration, with the increasing complexity of the instruments, voltage sags may effect various equipments seriously. The devices that are most sensitive to the sags are process-control equipment, computers and adjustable-speed drives [1].

The primary reason for the voltage sags is a short-duration increase in current generally contributed by motor starting, transformer energizing and faults (earth faults and short-circuit faults). In Figure 1.1, a typical voltage sag at the Point of Common Coupling (PCC) due to a fault in the parallel line is illustrated. The loads may be affected from the voltage sags even if the fault occurs kilometers away from the area of interest. In such cases, the magnitude of the remaining voltage at PCC will be a function of fault and source impedances (Z_s and Z_f) [2][3][4].

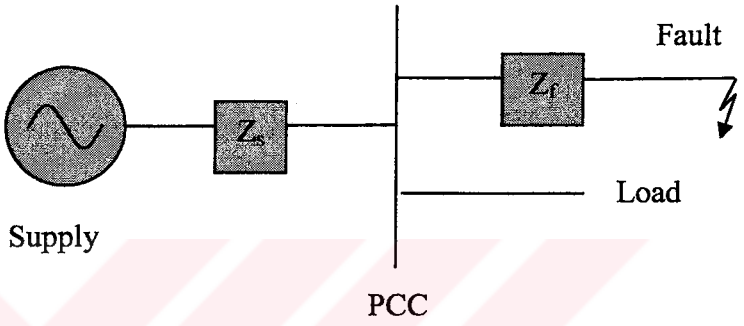

Figure 1.1 The origin of voltage sags

Even if the power system is designed for maximum reliability, disturbances, because of atmospheric influences and non-predictable component failures, may not be predicted and prevented. Therefore only additional measures taken in the power system or at the user's end can protect the critical loads from disturbances.

The most commonly used method is to install additional equipment at the system-load or system-customer interface which will guarantee a high-quality supply of electrical energy to the critical loads in cases of power system disturbances. UPS, the motor-generator set, the ferroresonance transformer and induction voltage regulator are conventional devices which solve the voltage sag problem. The static-transfer switch and Dynamic Voltage Restorer (DVR) are the latest examples of the equipments that may be installed to the system in order to increase the quality of the power system.

In order to protect industries from the voltage sags, a state-of-the-art device, the DVR which is introduced in the recent years constitutes a good solution for

compensating the missing voltage during a voltage sag event. The very basic idea of the DVR is to inject a dynamically controlled voltage generated by a forced-commutated converter in series to the bus by means of an injection transformer which is connected in the distribution level (Figure 1.2). Such an implementation will eliminate most of the voltage sags and minimize the risk of load tripping even if at very deep sags, therefore the plant where the device is connected will continue production process and the economic damage caused by voltage sags will be avoided.

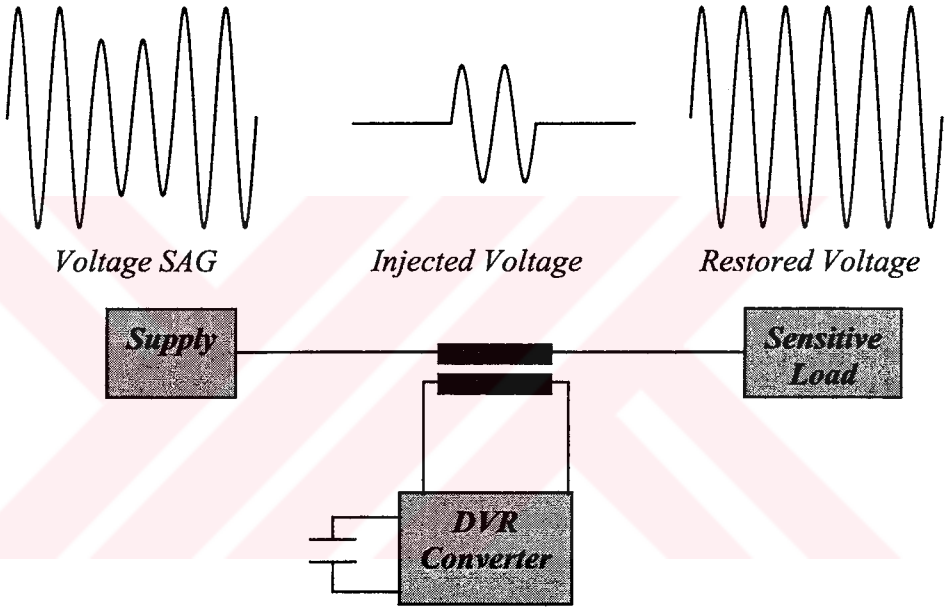

Figure 1.2 The operating principle of the DVR

For most of the time, the DVR will have "nothing to do" except monitoring the bus voltage. Therefore during the stand-by it should be ensured that the load is not disturbed by the DVR. The voltage drop caused by the injection transformer should be kept as low as possible and if this voltage drop degrades the load voltage requirement, the DVR may inject a small voltage in order to compensate the voltage drop it creates. The voltage drop on the DVR can be decreased by selecting an injection transformer with a relatively low leakage induction but the cost of the DVR will increase significantly.

When a disturbance is sensed in the bus voltage, the equivalent missing voltage will be generated by the inverter and injected to the line via the series injection transformer. Note that the DVR will not be designed to compensate total power supply interruptions, therefore it will be able to mitigate a certain amount of voltage sag and in case of deeper voltage sags or total power supply interruptions the DVR will not be treated.

The necessary energy for injection to the system by the DVR during the mitigation event may be supplied from either an energy storage device or directly from the grid that the DVR is connected. Operating with an energy storage device limits the performance of DVR for long duration sags and implementation costs will be rather high. Therefore topologies with shunt connected converter from the line itself or auxiliary supply have been proposed in the literature. Whereever the source of the energy of the DVR is fed, there exist strategies to decrease the energy absorbed in order to reduce the energy storage size. These strategies are called the "dynamic voltage restoration with minimum energy injection" which are based on advancing the phase of the injected voltage in order to utilize the source power more efficiently.

The DVR should sense the voltage magnitude and phase disturbance on the line quickly and generate the control signal for the pulse width modulated voltage sourced converters. In order to damp the harmonics generated by the PWM converter, a filtering scheme either to the line side or to the inverter side should be applied. The filtering scheme should ensure the remaining voltage at the supply side plus the injected voltage be within certain THD limits determined by the standards.

In this study, power quality problems will be discussed, necessary issues for DVR design will be covered and a DVR with the load side connected converter topology for a typical power system will be analyzed depending on the simulations carried on PSCAD/EMTDC software package.

The organization of the thesis is as follows:

- In Chapter 2, the most severe power quality problem, the voltage sag, is analyzed in depth. The voltage sags are characterized and the solutions are discussed.

- In Chapter 3, the operating principles of the DVR are introduced and the control issues are given.
- In Chapter 4, the topologies and components of the DVR are explained and analyzed in detail. The injection transformer, inverter and the filtering schemes are discussed.
- In Chapter 5, the system is described and the DVR design constraints are analyzed.
- In Chapter 6, the simulation results are given.
- In Chapter 7, the final conclusions on this study are made and the further work on this area is proposed.

CHAPTER 2

POWER QUALITY

Electric power quality can be defined as a measure of how well electric power service can be utilized by customers. From another point of view power quality is "having a bus voltage that closely resembles a sinusoidal waveform of required magnitude". IEC (1000-2-2/4) and CELENEC (EN 50160) define power quality as a physical characteristic of electrical supply provided under normal operating conditions which do not disturb or disrupt the customer's process.

Today, the expectations for power quality have increased. The companies do not want to suffer from poor quality power that feeds their plants. There are four major reasons for the growing requirements of power quality. First, the equipments are becoming more sensitive to power quality variations with the introduction of microprocessor-based controls and power electronics. Second, in order to reduce losses, adjustable-speed motor drives and shunt capacitors for power factor correction has been introduced for the overall system efficiency. Third, the end-users are more aware of power quality issues. Finally, since many things are interconnected via a network, the failure of any component has much more important consequences. All reasons listed above have just one aim, increased productivity for utility customers, such as more faster, productive and efficient machinery. The economics involved in solving the power quality problems is not always to eliminate the power quality variations but making a particular piece of sensitive equipment less sensitive to power quality variations.

Technically speaking, the following criteria quantify the power quality [6]:

- Constant sine-wave shape; the harmonics in the waveform should be kept in certain limits.
- Constant frequency; unchanged nominal value
- Symmetrical three-phase AC power system; the three phase voltages are with at phases shifted by 120^0.
- Constant rms value; the nominal power system voltage value unchanged over time.
- Fixed voltage; the power system voltage is unaffected by load variations.
- Reliability; the energy required is available at all times.

All of the listed above does have numerical upper and lower limits and during the operation, these values should be kept between limits determined by standards if the power quality level is considered to be high. Among these quantities "constant rms value" requirement is the most important and severe one. In case of rms value lower than the specific value a voltage sag event occurs vice versa a voltage swell event occurs. While the voltage swells can be prevented by surge diverters, the voltage sags require special attention. In this chapter the general information on the voltage sags which is required for deciding the DVR design parameters will be given.

2.1 VOLTAGE SAGS

A voltage sag is a momentary (i.e. 5-30 cycles) decrease in the rms voltage magnitude, usually caused by a remote fault somewhere else on the power system or within a customer facility. It is important to discriminate the interruptions and voltage sags. The former occurs when a protective device actually interrupts the circuit serving a particular customer when there is a fault on that circuit. But the latter occurs during the period of a fault on that circuit and there still remains a certain amount of voltage on the line. Faults on parallel feeders will cause voltage sags but will not result in interruptions.

IEC 1000-4-11 defines the voltage sags as "A sudden reduction of the voltage at a point in the electrical system, followed by voltage recovery after a short period of time, from half a cycle to a few seconds" while the interruptions are defined as

"The disappearance of the supply voltage for a period of time typically not exceeding one minute. Interruptions can be considered as voltage sags with 100% amplitude."

As the complexity of the electronics equipment used in the industrial plants increases, the equipments started to be more sensitive to the voltage sags. Today process controllers, Programmable Logic Controllers (PLC), adjustable speed drives, robotics, etc. are commonly used equipments which are very sensitive to voltage sags in the industrial plants. The frequency of the voltage sags is rather common than the interruptions which breeds the necessity of taking special measures to prevent unwanted voltage sag results.

2.1.1 Causes of Voltage Sags

Voltage sags are typically caused by fault conditions. Motor starting and transformer energizing can also result in under voltages, but these are typically longer in duration than 30 cycles and the associated voltage magnitudes are not as low.

Faults resulting in voltage sags can occur within the plant or on the utility system. The duration of the sags are determined by the fault-clearing time of the protective devices, typically a fuse or a plant feeder breaker for a plant and a branch fuse or a substation breaker for the utility system.

Utility system faults can occur on the distribution or transmission system. In Figure 2.1 a typical distribution system with a number of feeders supplied from a common bus is illustrated. A fault on feeder F1 will cause an interruption that will affect the customers on that feeder. However, the customer on the parallel feeders (F2 and F3) will experience a voltage sag while the fault is present on the system. Due to the reclosing breakers, the customers on the parallel feeders may experience more than one voltage sag lasting for durations ranging from a couple of cycles to more than ten cycles.

The consequences of the faults on the transmission system are more severe since such a fault can affect more customers fed from the system. Even the customers hundred kilometers away from the fault source still experience voltage sags.

The majority of the voltage sags are single phase line-to-ground (SLGF) faults that often result from weather conditions such as lightning, wind or ice.

Contamination of insulators, animal contacts and accidents during construction and transportation also cause faults. Three-phase faults are respectively are less common with respect to the single phase faults but the consequences will be more severe and harmful.

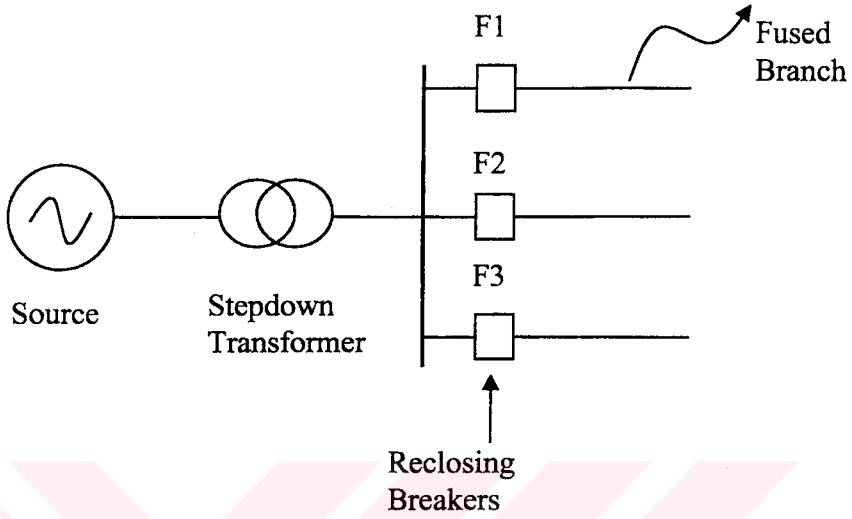

Figure 2.1 Typical distribution system with protection devices

Among the causes of the faults, lightning is the most common fault reason that effets the overhead transmission and distribution lines. Lightning can cause a fault by directly striking a phase conductor or by striking a ground object such as a shield wire or a tower. Although introduction of various protection measures and devices to the power system reduces the severity of the faults, there still happen events that will cause voltage sags.

In Figure 2.2, the rms values of the phase voltages during a large motor starting have been illustrated. The motor has started at 1 sec. This type of voltage sag can be described as a rather small voltage drop followed by gradual recovery. The large motors are all-three phase balanced loads which results in balanced voltage drops for all phases.

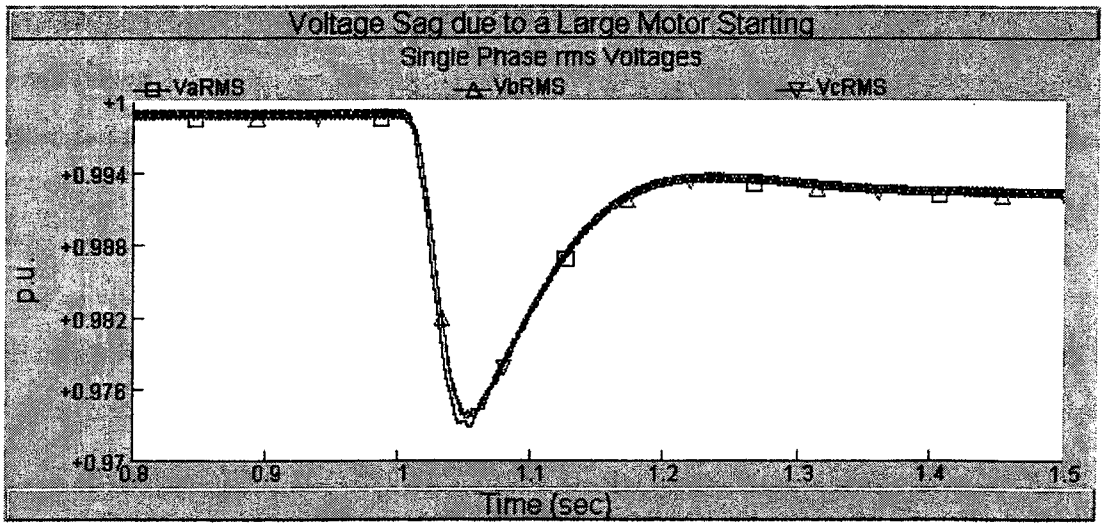

Figure 2.2 Typical voltage sag due to starting of a large load

A typical illustration of voltage sags due to energizing of transformers is shown in Figure 2.3. The transformer has been energized at 0.5 sec. The waveform characteristic is a sudden drop followed by a slow recovery. From the figure, the voltage sag level for all three phases is different. This event is due to the energizing of a large transformer where the inrush currents are different in three phases.

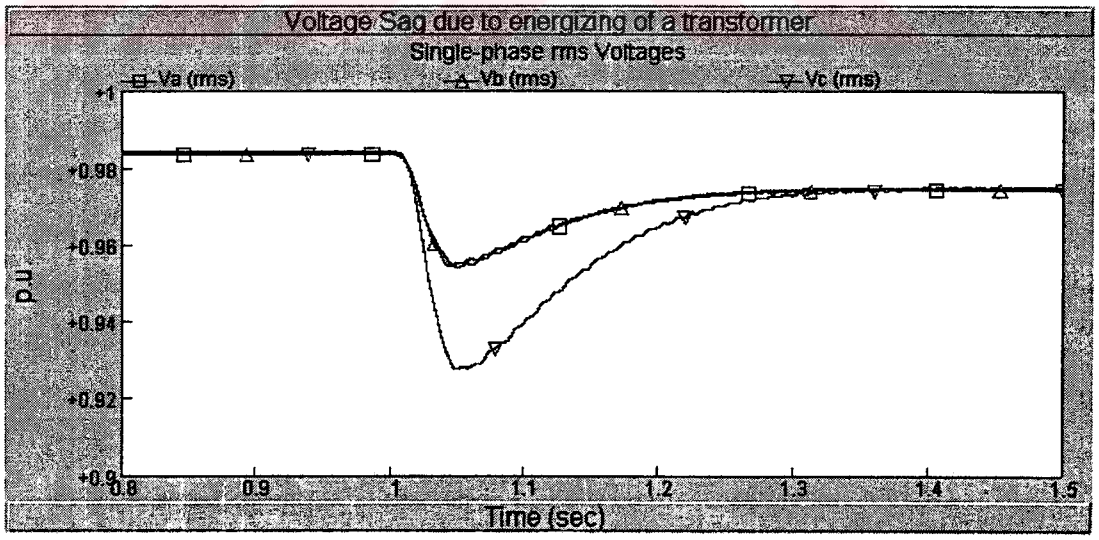

Figure 2.3 Typical voltage sag due to the energizing of a transformer

The majority of the voltage sags are caused by the fault conditions on the system. Figure 2.4 illustrates an unbalanced voltage sag caused by a fault in the parallel load.

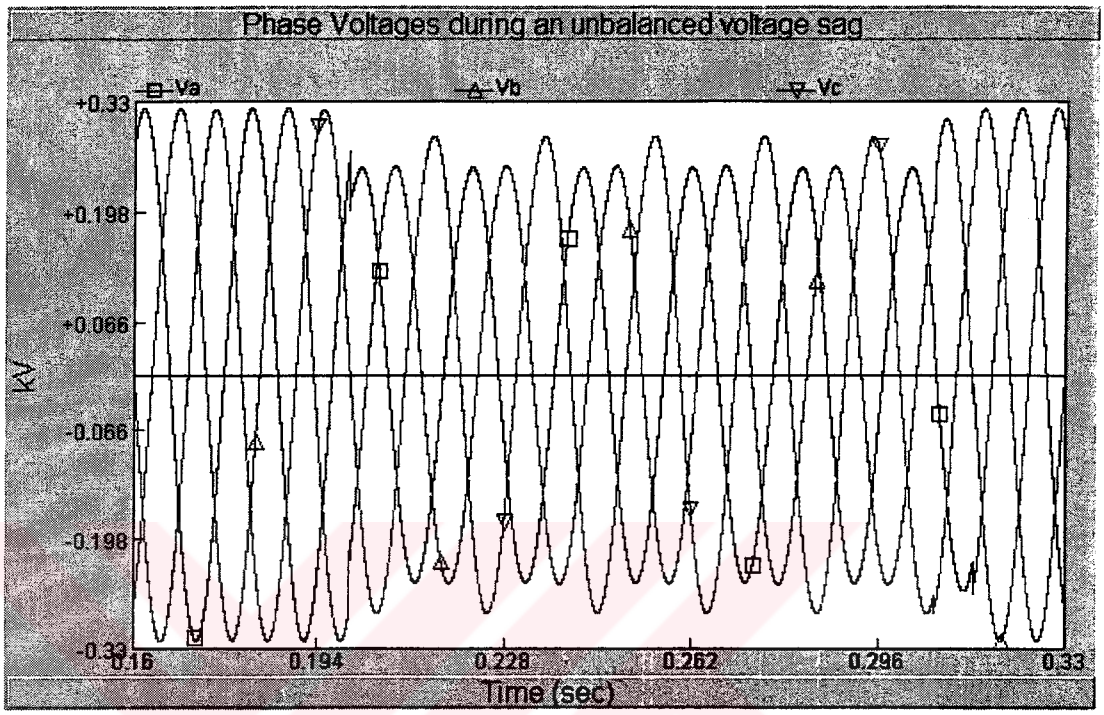

Figure 2.4 Typical voltage sag due an unbalanced fault

2.1.2 Characterization of Voltage Sags

The majority of the voltage sags due to faults are the single phase line-to-ground (SLGF) faults. Although SLGF can be prevented by proper isolation of the neutral, there still be faults that will cause voltage sags. The voltage on the faulted phase will go down to zero at the fault location. But the voltage level on the parallel feeders will depend on the distance of the fault which will be determined by the overall network impedances (Figure 1.1). The voltage sag level at the PCC can be calculated by:

$$\alpha = \frac{Z_f}{Z_f + Z_s} \tag{2.1}$$

where Z_f is the fault impedance and Z_s is the source equivalent impedance. α will vary between 0 and 1 and usually for the industrial power distribution, it will be very close to unity.

Another parameter that will determine the fault voltage level is the transformer connections as shown in Table 2.1 [3]. The voltage sag characteristics are modified by the connection type of the transformer. The delta connected transformers will decrease the severity of the voltage sag but the un-faulted phases will also experience partial voltage sags.

Table 2.1 Transformer Secondary Voltages with a SLGF on the Primary Side

Winding Connection	**Phase to Phase Voltages**			**Phase to Neutral Voltages**		
	AB	**BC**	**CA**	**A**	**B**	**C**
Yn/yn, Yn/y	58%	100%	58%	0%	100%	100%
Y/y, Y/yn	58%	100%	58%	33%	88%	88%
Dyn, Dy	33%	88%	88%	58%	58%	100%

Table 2.1 also shows that with respect to the type of transformer windings, some phases are not affected by the voltage sags (Yy connected) or all of the phases are partially affected (Delta/Delta). Note that the transformers with delta-connected windings act as a filter for the zero-sequence components by inducing symmetry and reducing the consequences of a fault. The phase voltage values of the non-faulted phases decrease slightly, so that the degree of asymmetry also decreases in comparison with the voltage system on the primary. For example in case of a voltage sag of 0.5 p.u. at phase A, filtering of the zero phase-sequence system on the secondary leads to a phase A voltage of approximately 66%. The voltages in phases not affected by the fault decrease in value about 8% and the phase displacement will about 8 degrees (Figure 2.7).

The duration of the voltage sags will be determined by the reclosing operation of the contactors and the reclosing breakers. This operation will require about 5 or 6 cycles (100 – 120 ms for 50Hz) to operate during which time a voltage sag occurs.

Figure 2.5, Figure 2.6 and Figure 2.7 illustrate voltage levels at the secondary of the transformer caused by a SLGF on the primary for different connection types.

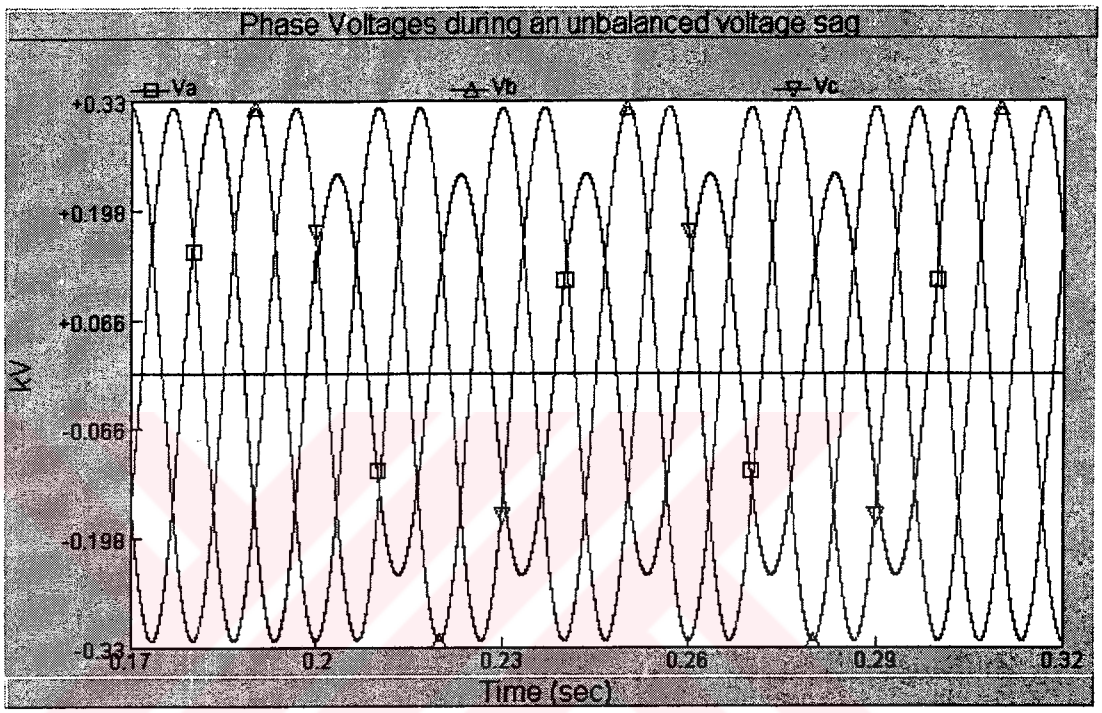

Figure 2.5 Voltage sag at the Wye/Wye connected transformer secondary

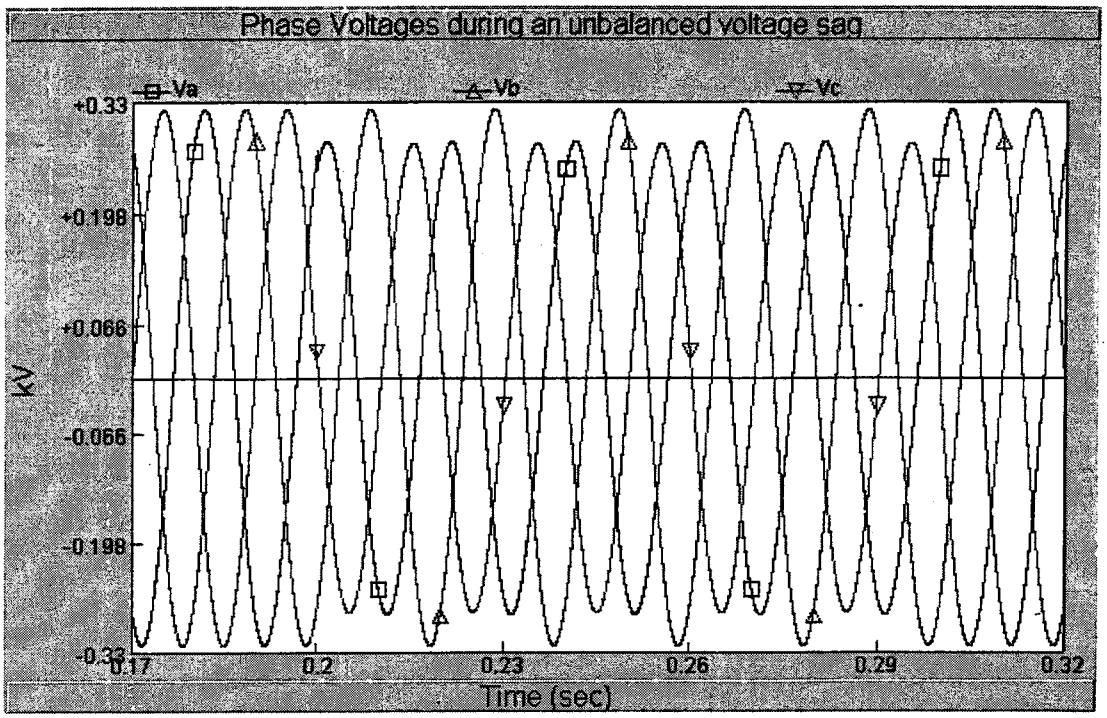

Figure 2.6 Voltage sag at the Delta/Wye connected transformer secondary

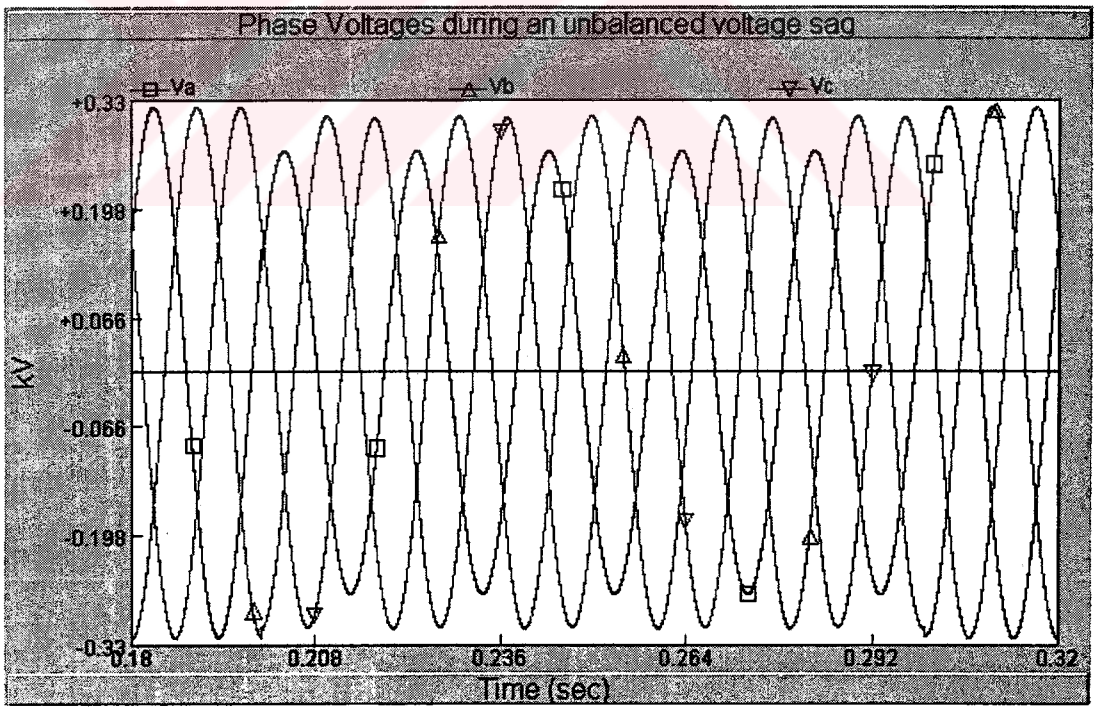

Figure 2.7 Voltage sag at the Delta/Delta connected transformer secondary

Even with a single-phase voltage reduction of 0.5 p.u., phase displacements about 10% may take place in the three-phase AC system which are not affected by the fault [8]. The voltage phase displacement in the non-faulted phases with respect to the single-phase fault level is shown in Figure 2.8 .

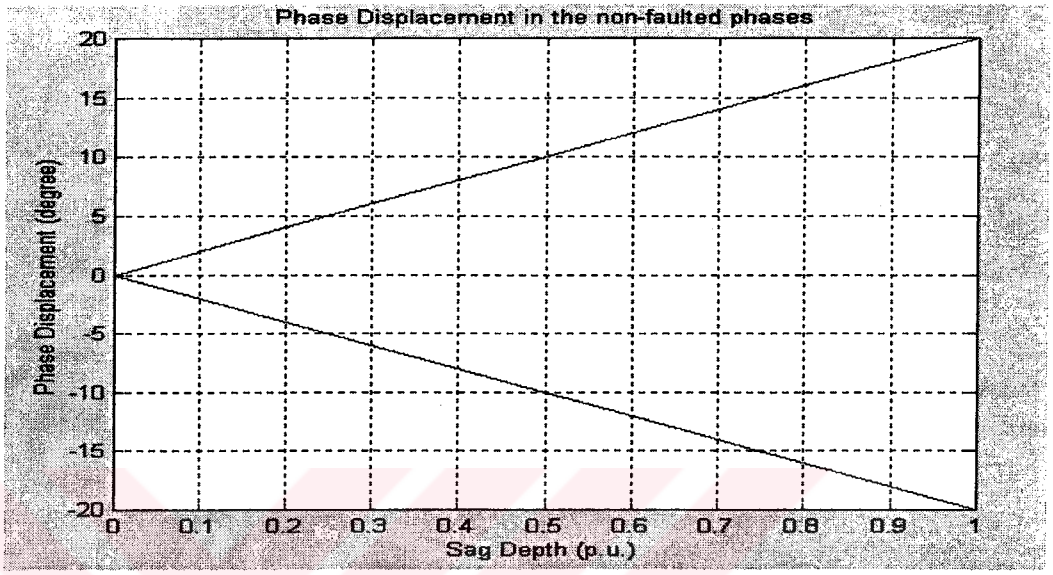

Figure 2.8 Change in the phase of the non-faulted wrt single-phase sag level

In Table 2.2, sample data taken from 222 distribution feeders in United States between 1993 and 1994 is given [25]. The table expresses the voltage sag occurrences for specific remaining voltage magnitude intervals versus the sag duration intervals (bin: between interval). For example there existed 6.8 sags per site per year with magnitudes between 70% and 80% and duration less than 200 ms. From the table it is clear that majority of the voltage sags (75% to 80%) are shorter than 200 msec and the sag magnitudes are below 50%.

Table 2.2 Sample voltage sag data [25]

Magnitude Bin	Time in Bin seconds (sec)				
	0.0 < 0.2	0.2 < 0.4	0.4 < 0.6	0.6 < 0.8	>=0.8
>80%-90%	53.1	4.8	1.9	0.7	2.9
>70%-80%	14.1	1.7	0.2	0.2	0.4
>60%-70%	6.8	0.9	0.1	0.1	0.2
>50%-60%	3.5	0.9	0.2	0.0	0.3
>40%-50%	1.4	0.4	0.2	0.0	0.3
>30%-40%	1.5	0.1	0.1	0.0	0.3
>20%-30%	1.2	0.3	0.2	0.2	0.4
>10%-20%	1.0	0.1	0.0	0.0	0.5
0%-10%	1.9	0.7	0.7	0.2	6.4

2.1.3 Standards Associated with Voltage Sags

During a voltage sag, the single phase devices may not be affected by the sag as shown in Table 2.1. But the three-phase devices and some of the single-phase devices will be affected. The sensitivity of the various equipments to the voltage sags is determined by the standards. But these equipments may be produced with different standards and may have significantly different sensitivity to voltage sags.

One of the most important equipment sensitive to voltage sags is the computers. The document associated with the voltage sags for the computers is the CBEMA curve [3] which was developed by the Computer Business Manufacturers Association. This applies primarily to data processing equipment.

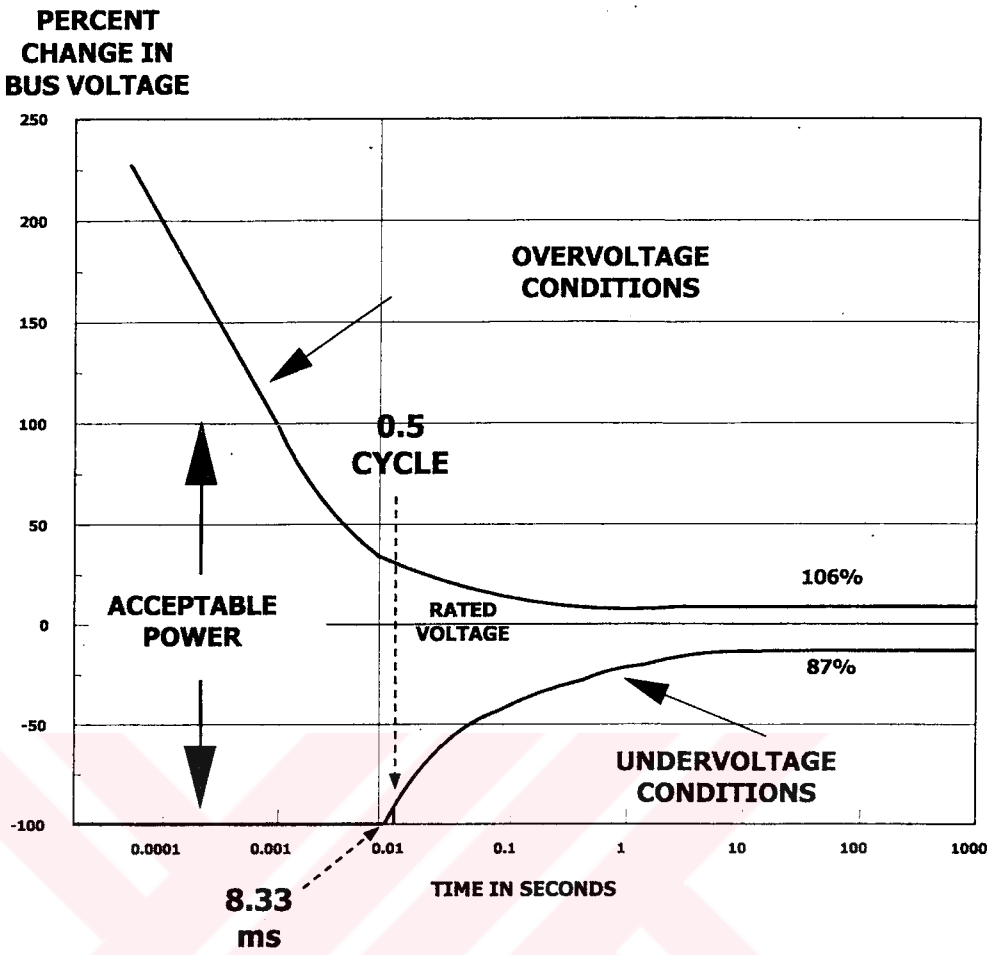

Figure 2.9 The CBEMA Curve

The CBEMA limits suggest a standard sensitivity to voltage sags for the data processing equipments but the equipment in a plant may have different characteristics to the voltage sags. For example the motor contactors and electromechanical relays, adjustable speed drives and programmable logic controllers' sensitivity level will be different.

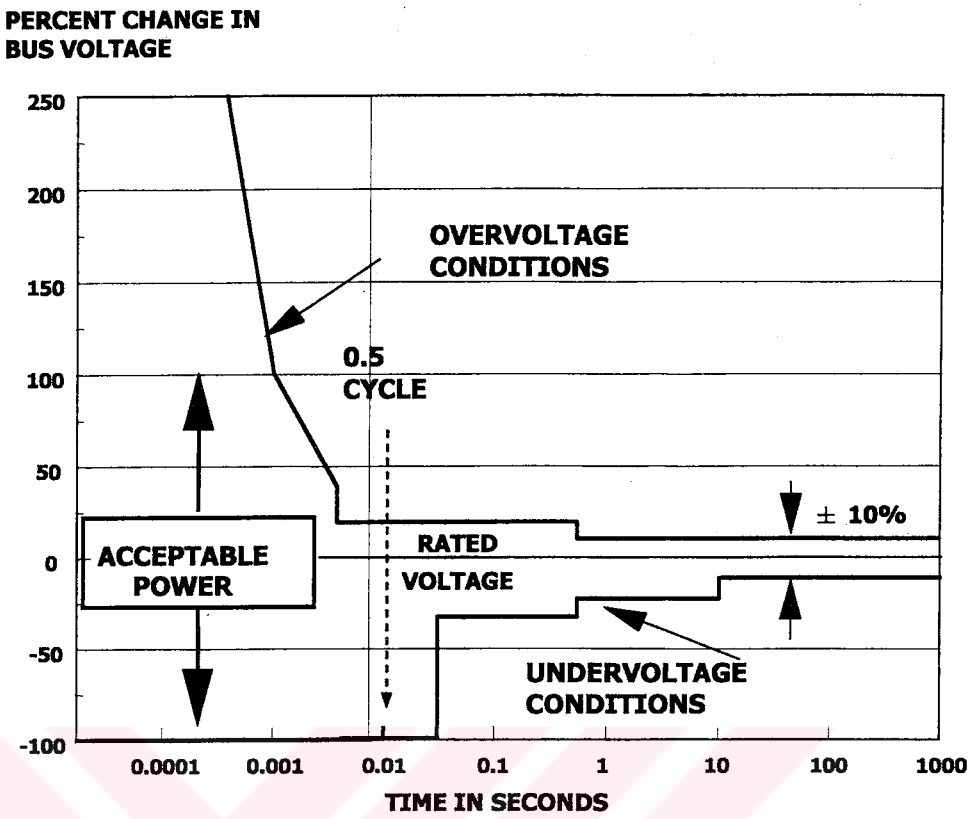

Figure 2.10 The ITIC Curve

Another standard is the Information Technology Industry Council (ITIC) curve (Figure 2.10). The main difference between the CBEMA curve and the ITIC curve is that the latter curve describes an acceptable operating region in steps rather than as a smooth curve. Instrumentation to check compliance with the ITIC curve is more easily designed.

Finally, Table 2.3 shows the standards associated with the voltage sags, the power acceptability curves.

Table 2.3 Power Acceptability Curves

Curve	Year	Application	Source
FIPS power acceptability curve	1978	Automatic data processing (ADP) equipment	U.S. federal government
CBEMA curve	1978	Computer business equipment	Computer Business Equipment Manufacturers
ITIC curve	1996	Information technology equipment	Information Technology Industry Council
Failure rate curves for industrial loads	1972	Industrial loads	IEEE Standard 493
AC line voltage tolerances	1974	Mainframe computers	IEEE Standard 446
IEEE Emerald Book	1992	Sensitive electronic equipment	IEEE Standard 1100

2.1.4 Mitigation Methods of Voltage Sags

Several measures may be taken by the utility, end user and equipment manufacturer to reduce the number and severity of voltage sags. We may reduce the number of events, improve our power system, mitigate the sag at the interface between system and load or finally improve our end-use equipment. Figure 2.11 illustrates the voltage sag solution alternatives and their relative costs [1][6].

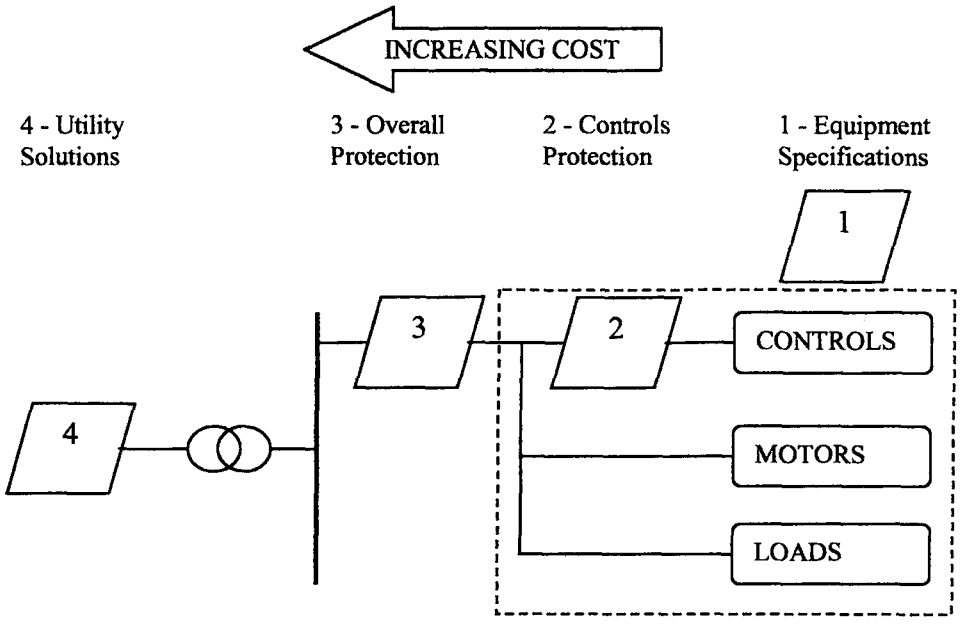

Figure 2.11 Mitigation Methods of Voltage Sags

Reducing the number of events is not an easy task and the cost can be very high since voltage sags at a location may be due to the faults kilometers away. Improving the power system does not reduce the number of events but makes them less severe. Again this may require large investments. Improving the end-use equipment seems to be the less costly but the manufacturers of the end-use equipments try to avoid this issue. Finally, the customers are left with one option: installing mitigation equipments.

Up to now, many methods have been proposed for the mitigation of voltage sags. UPS, motor-generator sets, ferroresonant transformers and induction voltage regulators are some commonly applied conventional methods that solve the problem partially. The state-of-the-art solution of the voltage sag problem is the application of the Dynamic Voltage Restorer (DVR) to compensate the missing voltages on the line.

CHAPTER 3

OPERATION PRINCIPLES OF DYNAMIC VOLTAGE RESTORER

3.1 INTRODUCTION

Since the voltage sags are considered to be one of the most severe disturbances among the power quality criteria, in order to mitigate the voltage sags in the power system, a series connected Custom Power device which consists of a voltage sourced inverter and a dc-link storage, the Dynamic Voltage Restorer, has been developed and integrated to the systems as a power quality device.

The primary function of the DVR is to eliminate or reduce voltage sags seen by sensitive large loads. Furthermore the device may be used in order to reduce phase unbalance seen by load and compensate voltage harmonics in the supply voltage. A DVR is schematically drawn in Figure 3.1 (Note that the energy storage of the DVR shown is optional and by application of different DVR topologies, the *Energy Storage* approach will vary).

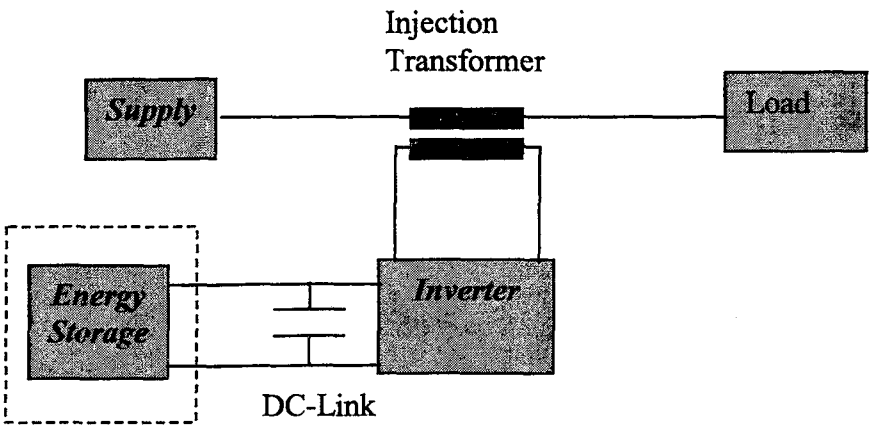

Figure 3.1 Schematic of a DVR

With the aid of the DVR, the industrial plants that come to a standstill during voltage sags will not suffer from the loss of money and time. Beyond the benefits of the DVR, the main drawbacks are the standby losses and equipment costs. Because of the large investments required for design and implementation of a DVR, a survey on the customers attitude show that customers suffering from voltage sag are tend to prefer a utility-provided solution with the cost included to their power bill as an alternative to the purchase, installation and operation of their own on-site equipment for the mitigation of power line disturbances. Therefore the DVR has been developed as part of a utility Custom Power device to provide a solution [30].

3.2 BASIC PRINCIPLE OPERATION OF DVR

The very basic idea of the DVR is to inject a dynamically controlled voltage generated by a forced-commutated converter in series to the bus by means of an injection transformer. Such an implementation will eliminate most of the sags and minimize the risk of load tripping at very deep sags.

From the practical point of view, for the DVR to perform proper operation, following criteria should be handled with care:

- During the normal utility system conditions, the DVR should not degrade the power system parameters.

- Voltage restoration for both short and long term voltage sags should be handled with proper design. During the restoration, the dc-link voltage should be maintained at certain level to ensure proper voltage injection. A trade-off between choosing a large capacitor bank or inserting a high rated rectifier circuit should be considered.
- The DVR must lock into the supply phase and must detect supply voltage distortions accurately.
- A PWM modulation scheme will be applied to synthesize the injected voltage, thus the switching frequency harmonics must be prevented from entering into the utility and customer system. For this purpose a filtering scheme should be introduced.

3.2.1 Steady State Operation of DVR

Under normal utility system steady-state conditions, the DVR may either inject only a small voltage to compensate for the voltage drop on the series reactance of the injection transformers and losses or go into a short circuit operation. If the load is not disturbed by the voltage drop on the DVR, the short circuit operation may be applied during the steady-state operation. Injection of a small voltage during steady-state may be necessary for weak utility distribution circuits without introducing and additional voltage drop for the voltage-drop-limited circuit.

3.2.1.1 Short Circuit Operation of DVR

If the voltage drop caused by the DVR does not affect the load requirements, the secondary of the injection transformer may be short circuited during steady-state operation in two ways [8]. One method is triggering the individual converter legs such as to establish a short-circuit path for the transformer low voltage leg. Note that no switching of semiconductors occurs in this type of operation. Therefore, only the comparatively low conduction losses of the semiconductors in this current loop contribute to losses. The switching of semiconductors may be seen in Figure 3.2 during short circuit operation (SCO).

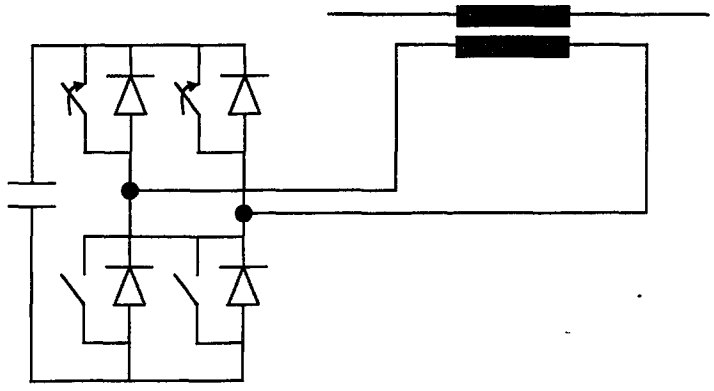

Figure 3.2 Short Circuit Operation of DVR with DVR Semiconductors

Another method to short circuit the transformer secondary is achieved by introducing a solid state bypass switch between the inverter and the transformer secondary. Furthermore since the Dynamic Voltage Restorer is connected in series, it will see the full load current as well as any currents due to downstream faults. In case of any temporary abnormal condition (i.e. load current overloads, etc.) the DVR will go into bypass until the load current returns normal conditions. Thyristors may be applied for the short-circuit device in order to protect the semiconductors to be thermally destroyed in case a downstream fault. Figure 3.3 illustrates the location of the short circuit device.

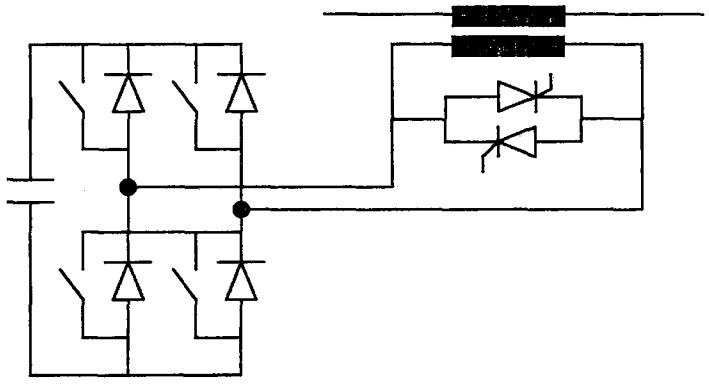

Figure 3.3 Short circuit operation with Thyristors

3.3 PROTECTION OF DVR

Another important point that should be considered during the implementation and production process of the DVR is the protection measures. The primary concern will be the increment in the current on the load side. The reason for this increment in the current magnitude may either be a downstream fault due to a short circuit on the load or drawing of large inrush currents such as connection of large AC loads and transformers. This may cause the DVR to go into a current limit to prevent damage to its power semiconductors. During the over current period, the control system of the DVR should remove itself from the line if the application of current limiting techniques such as output voltage reduction do not work. The DVR should have clever bypass schemes so as not to create additional disturbances onto the system which will affect the load. Solid-state bypass schemes as stated in (3.2.1.1) for the over current periods which exceed the DVR rating and/or electromechanical bypass systems for the long duration over current overloads, fault currents and for the isolation of DVR during maintenance may be applied. Note that the electromechanical bypass switches will be able to close typically at 4 to 6 cycles therefore a protection with thyristors should also be applied.

The transformer saturation is another problem during the recovery of a voltage sag. If the transformer saturates due to a lack of flux "headroom", the magnetizing currents will become very large such that they may damage the power semiconductors [9]. Again the control of the system should detect this situation and take the proper measures in order to avoid this problem. If the transformer is sized to handle two times the normal steady-state flux requirement at maximum rms injection voltage without saturation, this problem will be naturally solved but the cost of the injection transformer will surely increase.

3.4 VOLTAGE INJECTION STRATEGY

The aim of the DVR is not the restoration of full supply voltage but partial boosting of supply voltage during the mitigation of voltage sags. This results in a voltage injection limit on the DVR and the injection transformer. It is clear that

maximum single-phase voltage sag depth to be corrected will determine the primary-side voltage rating of the injection transformer.

Basically there exist two voltage injection strategies. First method is voltage injection in phase with the supply side voltage that is the mitigated voltage will be in-phase with the source side sag voltage. In this method the magnitude of the injected voltage will be minimized but the there will exist a phase-shift between the source side sag voltage and the pre-sag voltage in case of unbalanced voltage sags.

In this type of injection strategy, let the rated rms voltage of the primary feeder be V_p (per phase) and let the maximum voltage sag that our DVR will compensate is D p.u. Then a very rough estimation of required voltage injection magnitude can be calculated as:

$$V_i = DV_p \tag{3.1}$$

Where V_i is the required rms magnitude of injection voltage, D is the maximum per unit voltage to be injected and V_s is the rms phase voltage of the feeder.

As stated before, during the voltage sags, the amplitude and the phase-angle of the supply voltage varies according to the characteristics of the power system and the fault conditions. The voltage amplitude reduction can be accompanied by a significant phase-angle shift, such as illustrated in Figure 3.4. Thus another method which can be explained as compensating the difference between the sag and the pre-sag voltages may be applied. This strategy will be valid for both balanced and unbalanced voltage sags, and the restored voltage will be the same as the pre-sag voltage. Surely this method will require a voltage injection magnitude greater than the first method and normally a greater energy storage.

In Figure 3.4, the phase-shift on the source voltage (V_s) is denoted as α during a voltage sag. The load voltage (V_o) is restored to the pre-sag value by properly determined injected voltage (V_i)

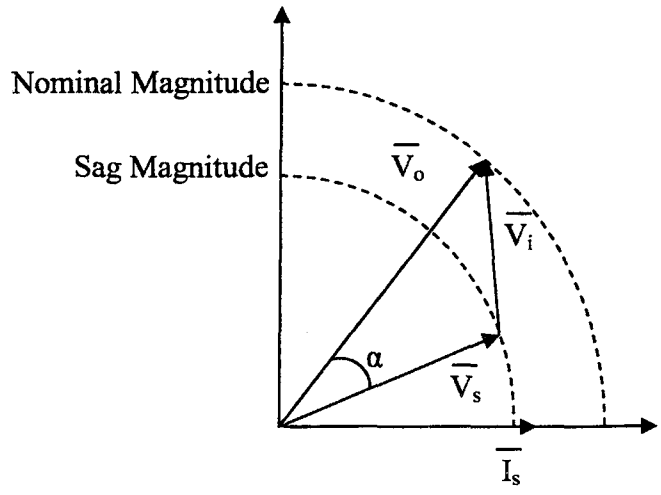

Figure 3.4 Voltage sag accompanied by phase displacement

In case of application of this voltage injection strategy, the steady-state voltage magnitude requirement will be:

$$V_i = \sqrt{V_o^2 + (1-D)^2 V_p^2 - 2V_o(1-D)V_p \cos\alpha} \qquad (3.2)$$

Where α is the largest possible phase-angle difference between restored voltage V_o and source-side voltage V_s.

Besides these two methods, recently another method for decreasing the energy storage capacity has been proposed called the dynamic voltage restoration with minimum energy injection.

3.4.1 Dynamic Voltage Restoration with Minimum Energy Injection

One of the recent topics studied on the DVR is on the energy storage optimization concept. The aim of the studies is optimizing the real power spent by the DVR thus minimizing the energy storage capacity. Mitigation of voltage sags by injection of appropriate series voltage component will surely require a certain amount of real and reactive power supplied by the DVR. However this amount of required power will be determined by the type of voltage disturbance and the voltage injection scheme.

The idea behind the dynamic voltage restoration with minimum energy injection concept is modifying the voltage injection scheme with respect to the conventional injection schemes so as to reduce the real power injected to the system by advancing the phase of the injected voltage [10][11]. In other words, with this method we decrease the power angle between the source voltage and the current thus forcing the power flow uphill from source to load. Since there is a phase difference between the input and output voltages, the magnitude of the injected voltage will surely be larger than the in-phase injection method. But the cost of this minimization will be in increased magnitude of injected voltage, phase-shift experienced in load voltage and the complexity of the control system. The phase-shift that will be experienced by the load voltage may result in voltage waveform discontinuity, inaccurate voltage zero-crossing and load power swing.

If our concern is only keeping the magnitude of the load voltage in some limits, minimum energy injection goal may be reached. To illustrate the idea, as shown in Figure 3.5, the locus of the load side voltage can lie anywhere on a circle with radius V_0. However the source voltage and the voltage injection limit of the DVR will determine the minimum energy injection operating point. The operating point in Figure 3.5 is denoted by D. The load voltage (V_o) is restored by a phase-advance angle of β with respect to source voltage (V_s) during a voltage sag by properly determined injected voltage (V_i). At this case the angle between the source voltage and the load voltage becomes φ.

If $Vs < V_0 cos\varphi$ and there is no injection limit, the operating point can lie anywhere on the arc AB. When $\theta = 0$, the injected real power $V_{ip2}I$ approaches minimum. If $V_s > V_0 cos\varphi$ then the operating point may be on the arc EF and operating point F is the zero power injection point. From Figure 3.5, in order to decrease θ, we should increase the magnitude of the injected voltage.

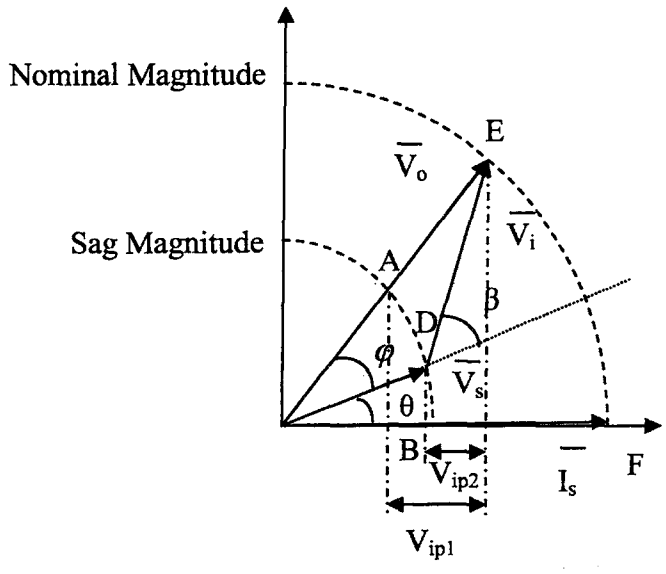

Figure 3.5 Phase-advance energy-saving voltage restoration

In this type of injection strategy, the magnitude of the injection voltage is the primary limiting factor for the economic considerations. Normally the higher the magnitude of the injected voltage the higher the rating of the DVR thus a trade-off between the rating of the DVR and minimum energy injection can be solved by a partial boosting strategy. The required magnitude of injected voltage can be calculated with:

$$V_i = \sqrt{V_o^2 + (1-D)^2 V_p^2 - 2V_o(1-D)V_p \cos\varphi} \qquad (3.3)$$

This equation is similar with (3.2). The phase-shift angle α is switched with the phase-advanced angle φ which is greater than α.

Another point to be paid attention occurs at the end of the voltage sag where the phase-advance method may result in a sudden phase difference as shown in Figure 3.6. In order to overcome this problem a progressive phase advance method should be implemented.

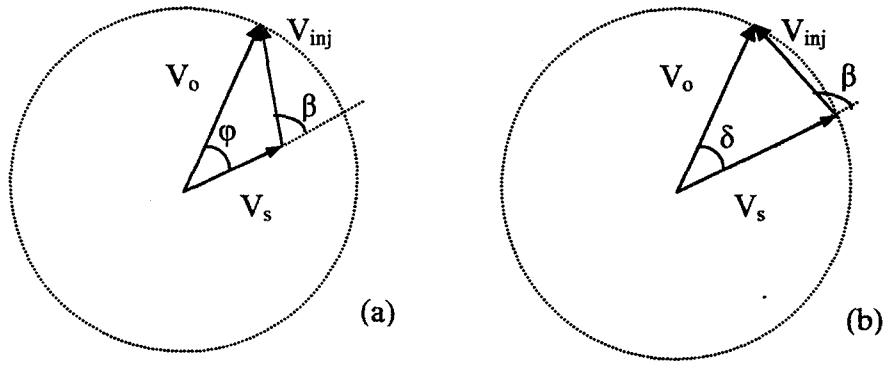

Figure 3.6 Phase difference event at the end of the sag

This method will start to work only after a time a voltage sag occurs since all of the methods for calculating the parameters of the supply voltage (magnitude and phase) requires a time delay. Fast Fourier Transformer (FFT) and Discrete Fourier Transform (DFT) algorithms have been applied to many important areas of waveform analysis of power systems but suffer from certain limitations such as number of samples per cycle to be an integer number and stationary input signal. These limitations can be overcome by Kalman filtering approach [11].

3.5 CONTROL OF DVR

The control strategy of the DVR should be designed to detect of the voltage sags in the supply voltage and apply the necessary missing voltage as soon as possible. In order to minimize the response time and maximize the dynamic performance, generally a direct feed-forward-type control architecture is applied.

Rms value calculation of the voltages can be considered for the first approach for the detection of the voltage sags. But the calculation of rms voltage will require at least one half period at the line frequency and this delay degrades the performance during the transients. Besides the transient operation of the DVR, the phase-shift associated with the voltage sags should also be considered while mitigating the voltage sags and this method is again very weak to this kind of problem.

Another important point is the presence of an inverter-side filtering scheme which will require special attention since this kind of filtering scheme will introduce a voltage drop and additional phase shift in the injected voltage.

3.5.1 Detection of Disturbances

In order to detect the voltage disturbance on the source side, three- to two-phase transformation is applied. This type of transformation will increase the fault detection time of the DVR and also will be valid for the unbalanced voltages. The two-phase values obtained will be separated into positive and negative sequence components and then will be compared with the proper reference values. For this type of operation the phase-angle information of the source voltages should be calculated.

Note that the zero sequence components can be ignored since the DVR will be located to the three wire distribution system and the zero sequence components will be filtered in the delta connected step-down transformers.

3.5.2 Phase Locked Loop

The detection of the phase-angle of the source voltage is critical for the DVR. The method should not be affected from the unbalanced voltages, flicker, harmonics and frequency variations. Considering these requirements, a Phase Locked Loop (PLL) algorithm for the detection of phase-angle should be implemented. The quality of the PLL operation will have an important impact on the control performance of the system.

The output of the PLL is as shown in Figure 3.7. The output of PLL is 0^0 when phase A is in the positive peak. The PLL tracks the phase of the source voltage and from the figure, reaches 360^0 when phase A reaches the second peak. The output of the PLL will be used while extracting the dq components of the three-phase source voltages. A method in [12] is proposed for the implementation of the PLL.

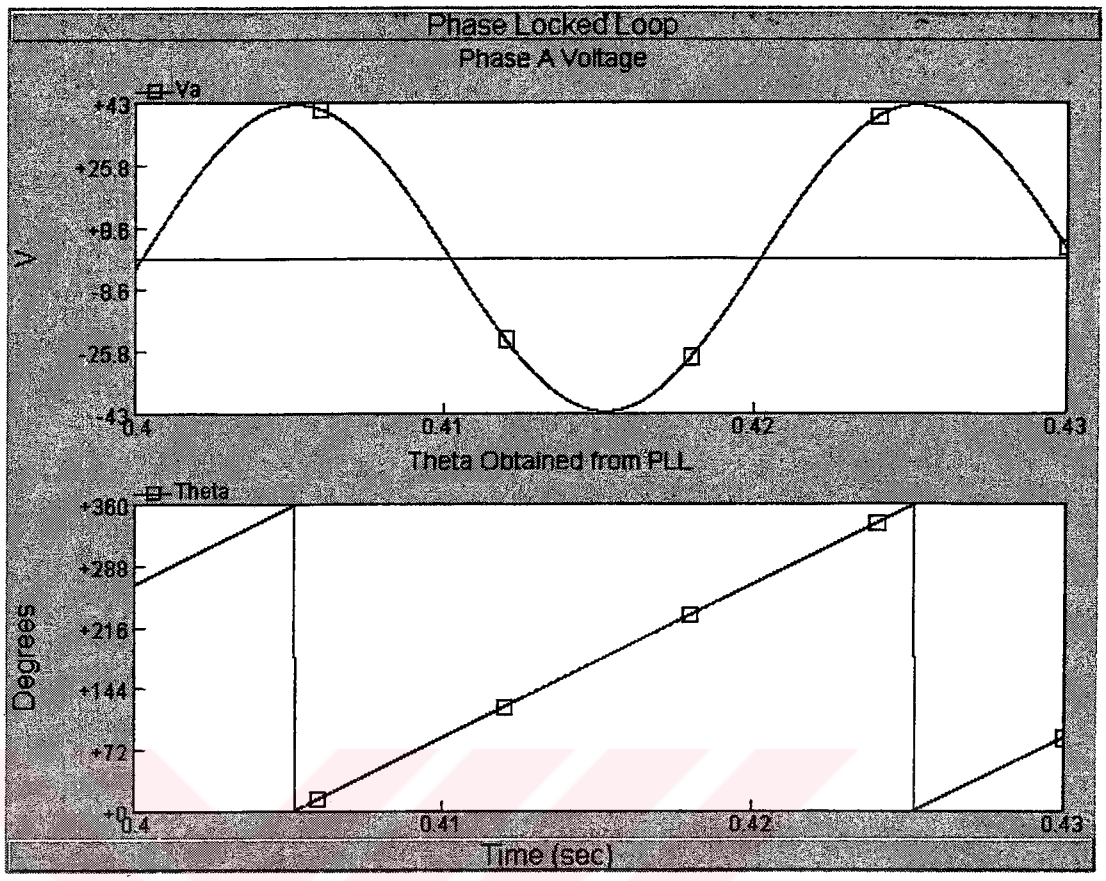

Figure 3.7 Phase Locked Loop output

3.5.3 Extraction of dq components

In the control of the DVR, the accurate phase voltages' magnitudes and phases should be obtained. One method to obtain this information is transforming the phase voltages to the synchronous rotating frames in order to obtain DC values for the required information. This method is called the instantaneous symmetrical components method.

In the first step, the three-phase source side voltages are transformed into two-phase $\alpha\beta$ voltages which are fixed with the source side voltage vector V_s as shown in Figure 3.8. With this transformation, the three-phase voltages are shown in two-axis coordinate system.

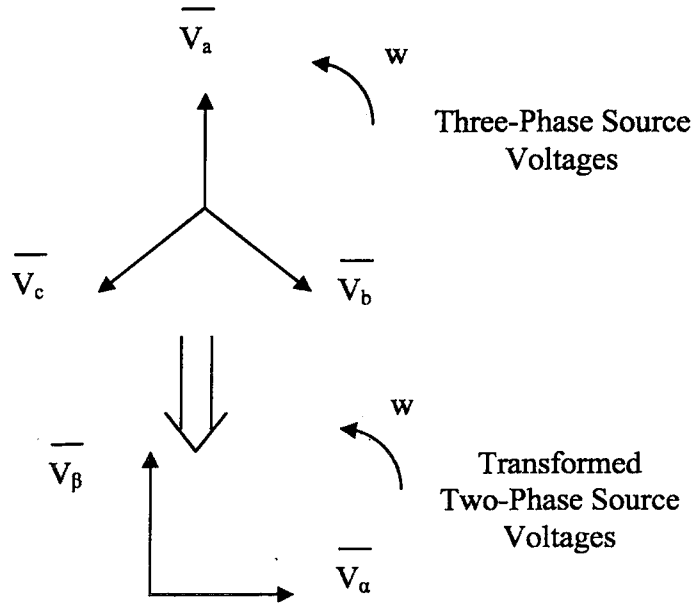

Figure 3.8 αβ transformation of voltages

If the define the source side voltage vector V_s with the instantaneous source side phase voltages V_{sA}, V_{sB} and V_{sC} as:

$$\overline{V_S} = V_{s\alpha} + jV_{s\beta} = \sqrt{\frac{2}{3}}(V_{sA} + \alpha V_{sB} + \alpha^2 V_{sC}) \tag{3.4}$$

Where $\alpha = e^{j2\pi/3}$, $\alpha^2 = e^{-j2\pi/3}$ then the three-phase to two-phase αβ transformation matrix can be written as:

$$\begin{bmatrix} V_{s0} \\ V_{s\alpha} \\ V_{s\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_{sA} \\ V_{sB} \\ V_{sC} \end{bmatrix} \tag{3.5}$$

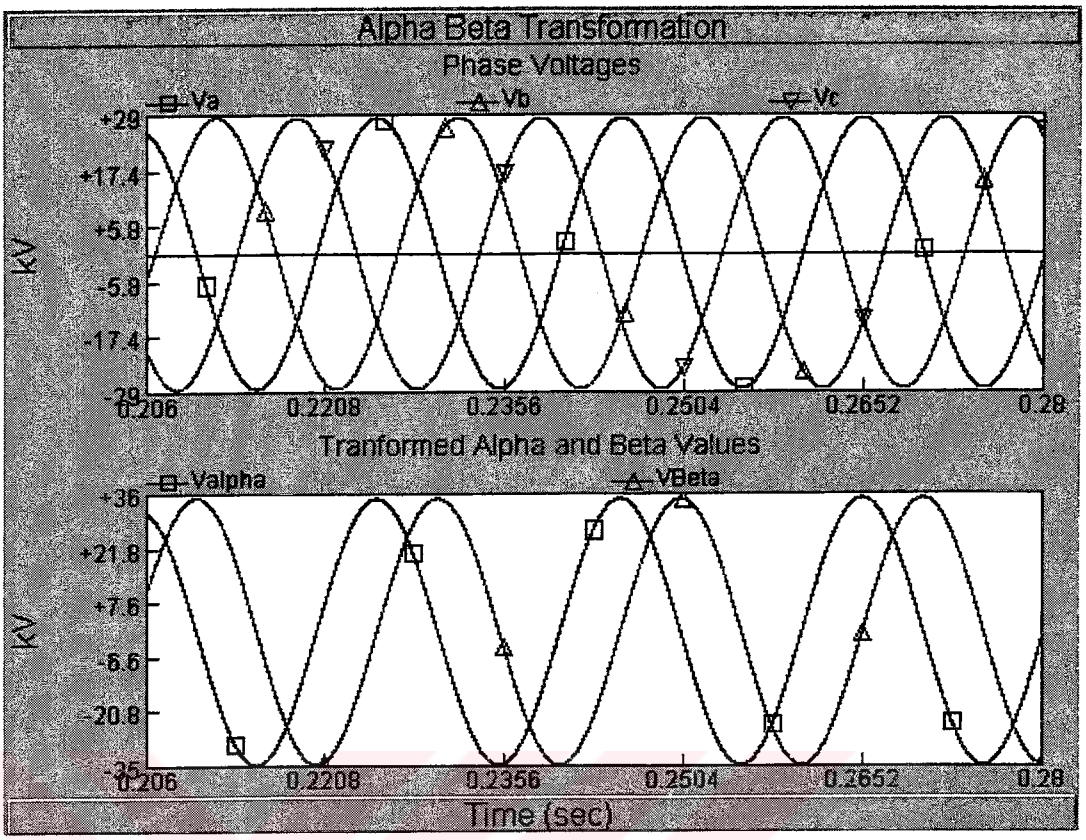

Figure 3.9 αβ transformed voltages

In the second step, the two phase values are transformed into rotating dq-coordinate system (Figure 3.10). With this transformation, it will be possible to obtain constant DC values of voltage components which is a great advantage in the control of the inverter.

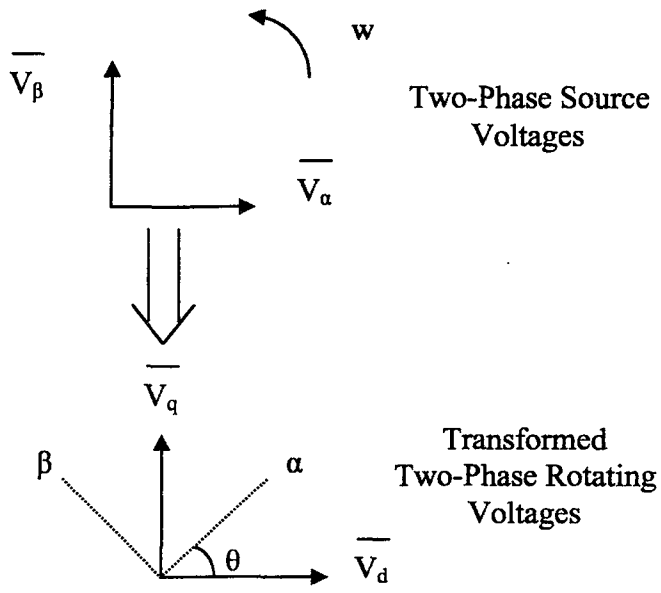

Figure 3.10 dq transformation of voltages

With the phase-angle information of θ obtained from the PLL, the stationary two-phase αβ vector can be converted into a rotating reference frame called as the dq transformation. The dq transformation equation and matrix are defined as:

$$V_{sd} + jV_{sq} = (V_{s\alpha} + jV_{s\beta})e^{-j\theta} \tag{3.6}$$

$$\begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_{s\alpha} \\ V_{s\beta} \end{bmatrix} \tag{3.7}$$

When the utility voltages are ideal and balanced, the dq components of the source voltage V_s appear as DC values (Figure 3.11) in the rotating reference frame.

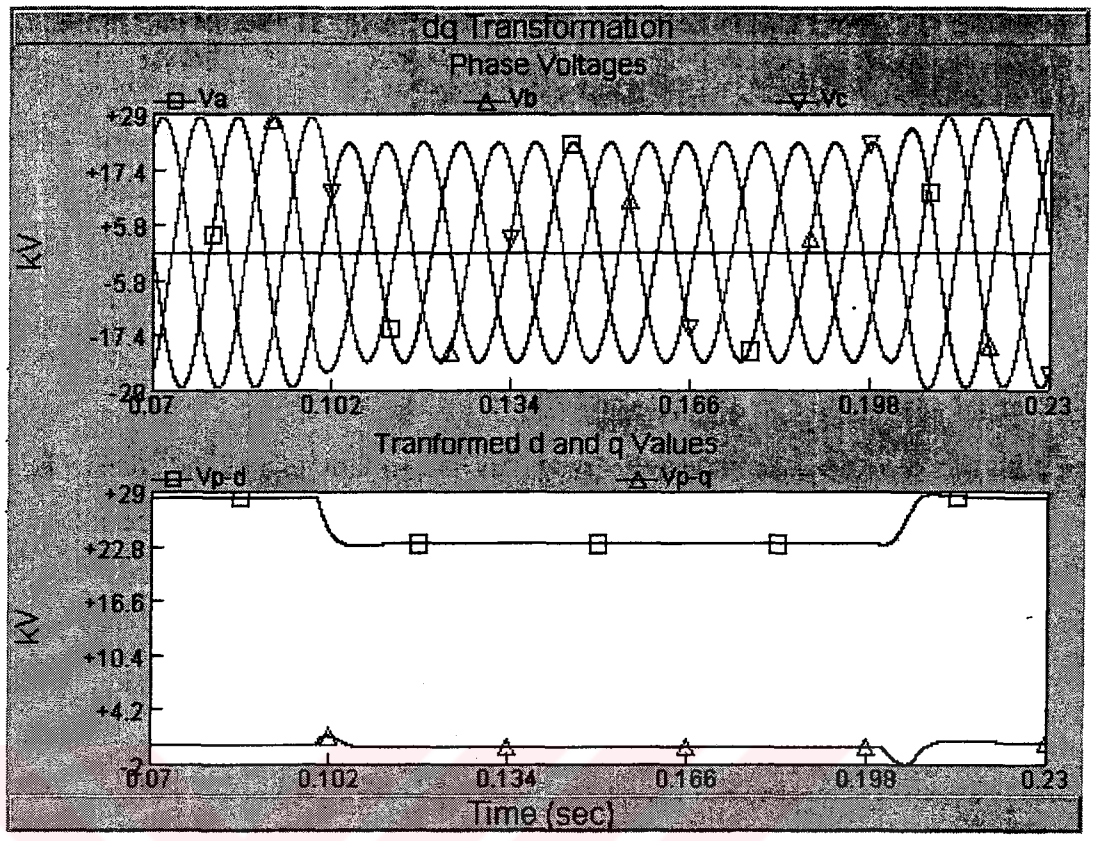

Figure 3.11 dq transformed voltages

3.5.4 Dq components of the unsymmetrical set of voltages

The unsymmetrical set of voltages (in case of source voltage unbalance), two rotating coordinate systems should be used for proper operation of the controller. The former will rotate counterclockwise direction, denoted as $V^{(p)}$ and called as the positive sequence synchronous reference frame (SRF), while the latter will rotate in the clockwise direction, denoted as $V^{(n)}$ and called as the negative sequence SRF, with the angular frequency of the system in the stationary reference frame (Figure 3.12).

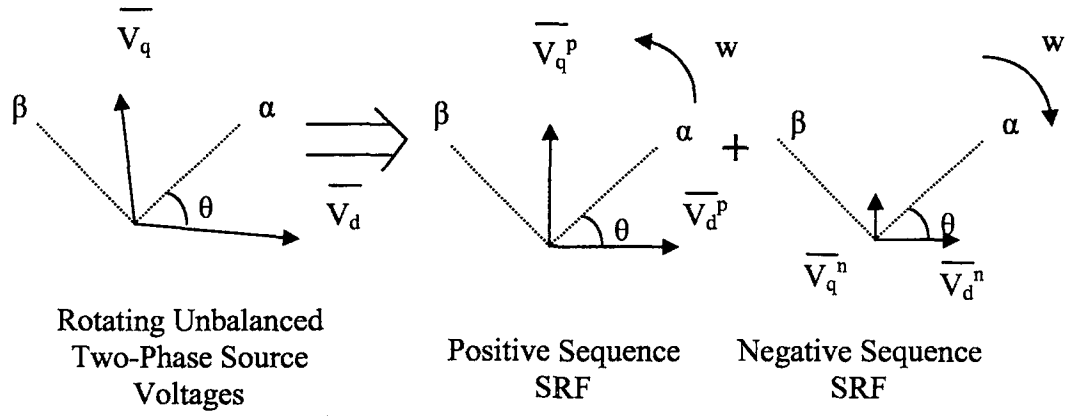

Figure 3.12 dq transformation of unbalanced voltages

The positive sequence SRF will be composed of positive sequence which is a DC component and negative sequence which is an AC component with the frequency twice of the angular frequency. The positive sequence SRF can be extracted when $\theta = wt$ in (3.6) (Figure 3.13).

Considering the negative sequence SRF, this time the negative sequence becomes DC component and the positive sequence becomes the AC component. The negative sequence SRF can be extracted when $\theta = -wt$ in (3.6) (Figure 3.13).

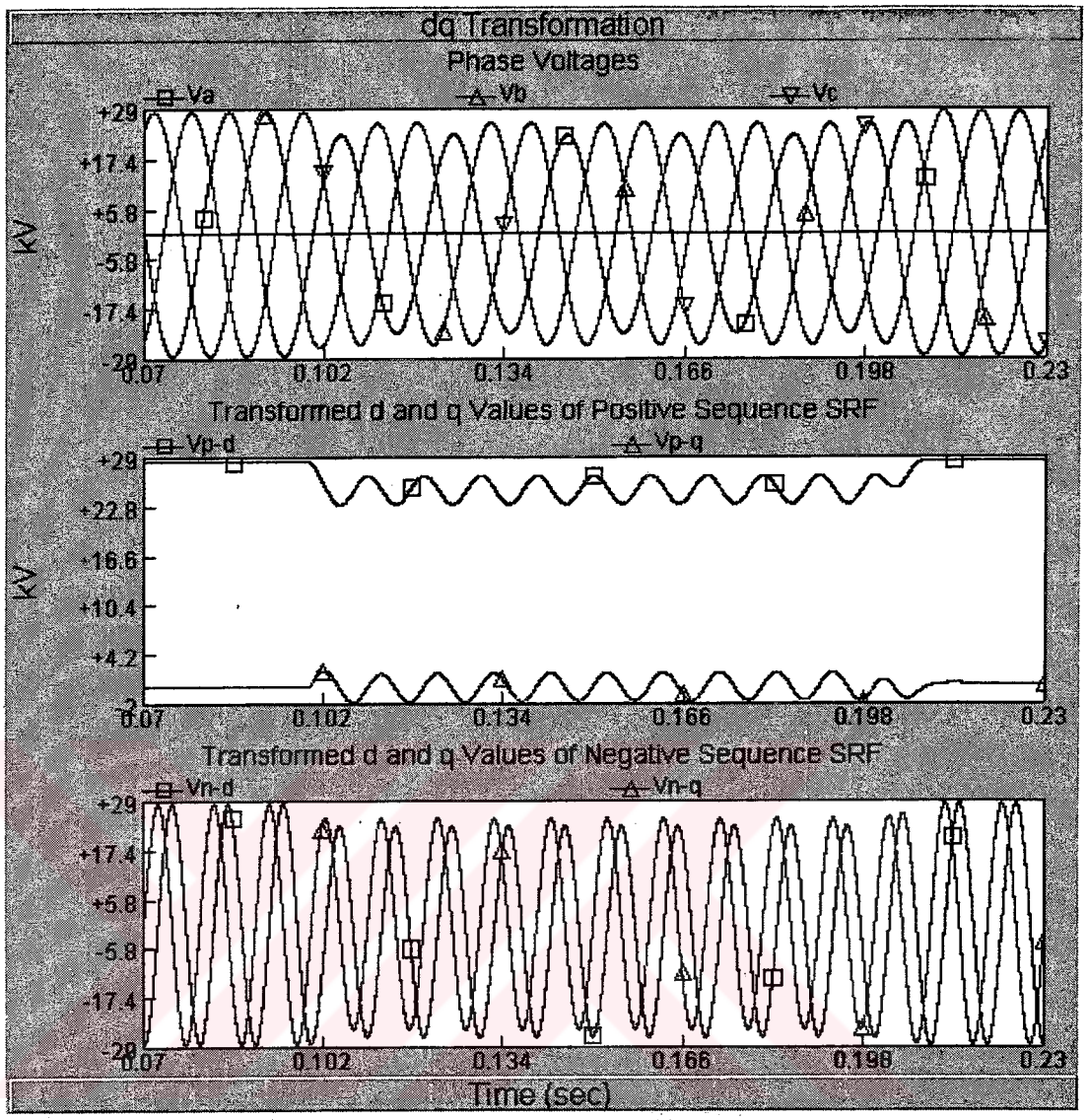

Figure 3.13 dq transformations in the negative and positive sequence SRF

For the effective control without phase shift in the steady state, the DC values of the positive and negative sequence SRF should be calculated accurately. Among the methods of this extraction, application of a low pass filter (LPF) may be considered. Application of a filter will introduce a delay in the control system. Furthermore the AC values in the negative sequence SRF is large with respect to the DC values thus a LPF will not be able to filter out the AC components. This problem may be solved by decreasing the cut-off frequency of the LPF but the controller response will be very slow.

In the literature, two methods for the extraction of the DC values are proposed. One proposes a differential controller method while the other proposes a mathematical solution which is based on extracting the signal with the *T/4* delayed signal thus obtaining the AC values. To illustrate, the DC components of the positive and negative sequence components are extracted via the FFT transformation. The DC components of the unbalanced voltages are as shown in Figure 3.14 [13][14].

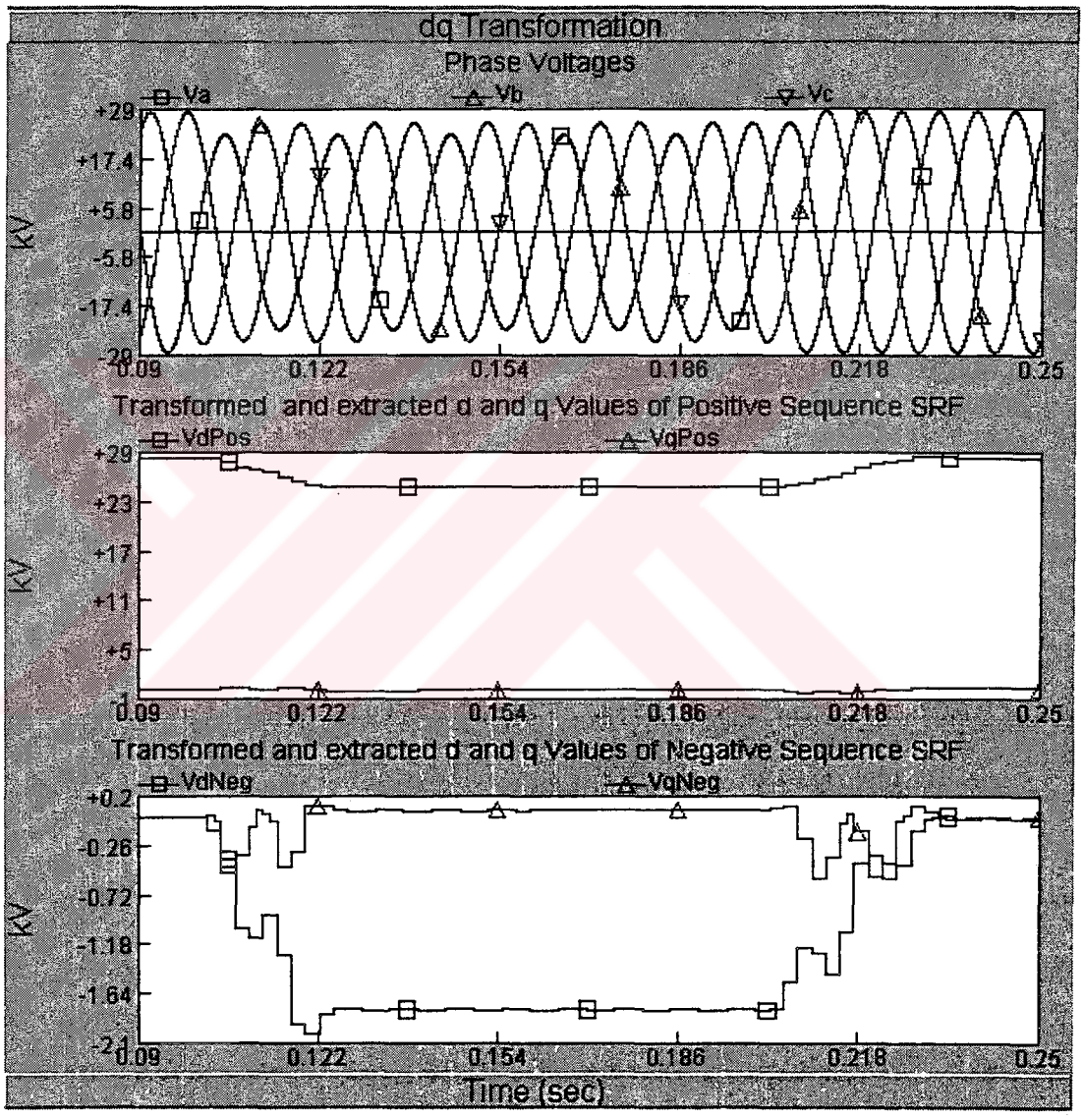

Figure 3.14 Extracted dq transformations in the negative and positive sequence SRF

3.5.5 Voltage Controller

The aim of the voltage controller is supply the load with a balanced set of voltages of desired amplitude resulting in the following components of the desired load voltage vector:

Positive sequence voltage in d-direction $V^{(p)}_d = 0$

Positive sequence voltage in q-direction $V^{(p)}_q = V_{l\text{-}r}$

Negative sequence voltage in d-direction $V^{(n)}_d = 0$

Negative sequence voltage in q-direction $V^{(n)}_q = 0$

Where $V_{l\text{-}r}$ is the rated phase-phase load voltage.

The components of the desired load voltage vector are compared with the above corresponding values in order to obtain positive and negative sequence components of the voltage to be injected. They are transformed back into the αβ-coordinate system and added and then transformed into the three-phase domain and the reference signal for the PWM inverter is obtained (Figure 3.15). For the symmetrical balanced faults, there is no need to extract the positive and negative sequence SRF components. Therefore the controller response to the balanced voltage sags will rather quick with respect to the unbalanced voltage sags. In order to reduce the error between the reference and the actual voltage values, PI controllers are inserted before the "dq to αβ" transformations.

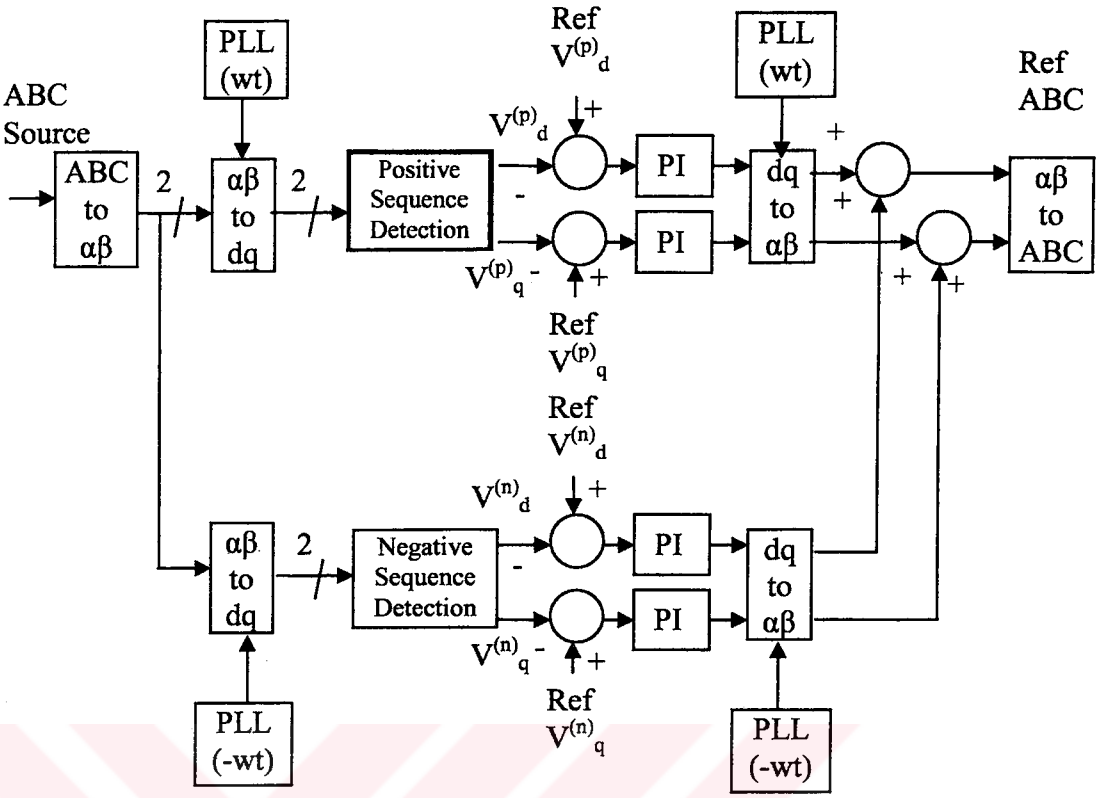

Figure 3.15 The Control Block Diagram

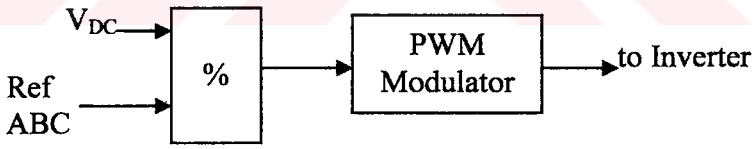

Figure 3.16 The generation of PWM signals

Another control issue that may be added to optimize the controller is the DC link voltage magnitude. During a voltage the energy on the DC-link will be transferred to the load, changing the magnitude of the DC-link voltage. Even if for the topologies that feed the DC-link during the compensation, there still be variations in the DC-link voltage related with the voltage sag depth. Therefore the controller

should ensure proper voltage injection magnitude considering the DC-link voltage (Figure 3.16).

Note that as introduced before the application of inverter side filter and the injection transformer will degrade the performance of the controller and thus will require special considerations

In this type of control strategy the DVR will inject voltage with the fundamental positive and the negative sequence. The advantage of this strategy is that the compensated voltage will be in phase with the pre-sag voltage. The disadvantage is the magnitude of the injected voltage should be greater than the in-phase injection strategy during an unbalanced voltage sag.

After obtaining the reference voltages, the PWM signals for triggering the each leg of the inverter should be calculated. Sinusoidal PWM method [24] is one of the simplest and effective methods which can be applied to the inverter of the DVR.

3.6 LOCATION OF DVR

The DVR will cope with voltage sags caused by faults in the transmission or distribution systems. In custom power applications, the DVR is connected in the utility primary distribution feeder via a series injection transformer. By this connection location, a voltage sag in the point of common coupling (Figure 3.17) caused by faults on the adjacent feeders or on the transmission system that would affect a certain group of customers will be mitigated.

Another advantage of this location is that the zero sequence components in case of an unbalanced voltage variation are filtered in the delta connected transformers therefore the DVR will not deal with the zero sequence components.

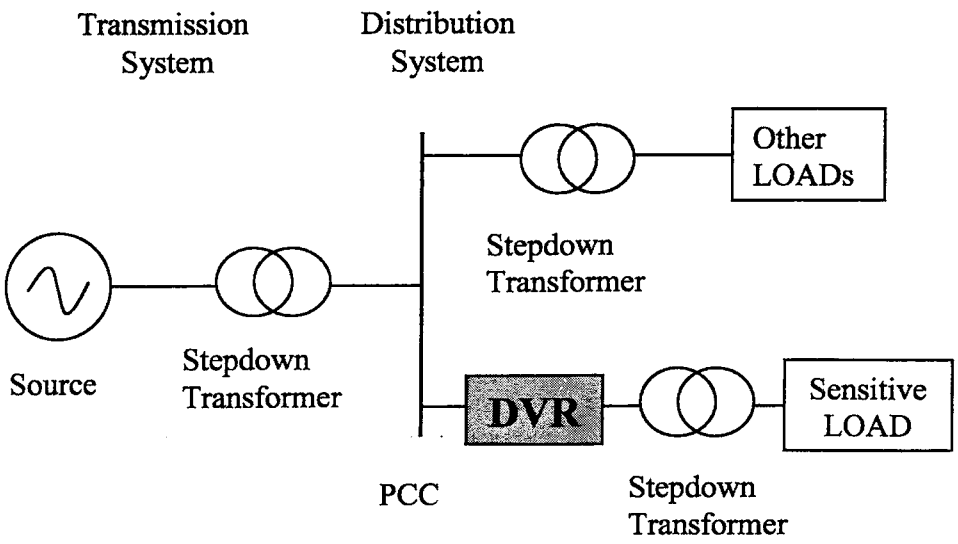

Figure 3.17 The Location of DVR

CHAPTER 4

DVR TOPOLOGIES AND COMPONENTS

The DVR is mainly composed of an inverter to generate the injection voltage, a filter to damp the harmonics generated by the inverter, an energy storage unit to supply the necessary active power during the mitigation of voltage sags and a series injection transformer to couple the generated voltage to the system. Different schemes and topologies exist for these components. In this chapter of the study, basic topologies of for charging energy storage unit, the parameters of the injection transformer, the inverter schemes that can applied and the filtering schemes will be introduced and analyzed.

4.1 TOPOLOGIES OF DVR

The most critical issue in designing a DVR is the source of energy to be supplied to the DVR. Compensating of voltages effectively in large voltage reductions requires active power which will be supplied from a storage system, the grid itself or from an auxiliary supply. The topologies proposed can be divided into two main groups following two sub-groups for each [15]:

- Topologies with no energy storage
    - Energy taken from the existing supply with a passive shunt converter connected to the supply side.
    - Energy taken from the existing supply with a passive shunt converter connected to the load side.

- Topologies with energy storage
  - Stored energy in the DC-link and a variable DC-link voltage
  - Arbitrary kind of energy storage with a controllable DC-link, which can be held constant.

4.1.1 DVR Topologies with No Energy Storage

During voltage sags, there still remains a significant part of the supply voltage. If the DVR is connected to a strong grid, the necessary power to the load can still be obtained from the source by increasing the supply current by a shunt converter.

A passive shunt converter is applied since only uni-directional power flow is assumed necessary.

4.1.1.1 Supply Side Connected Shunt Converter

The supply side connected converter is shown in Figure 4.1. The uncontrollable DC-Link voltage and the passive converter will charge the DC-Link capacitor to the actual state of the supply voltage.

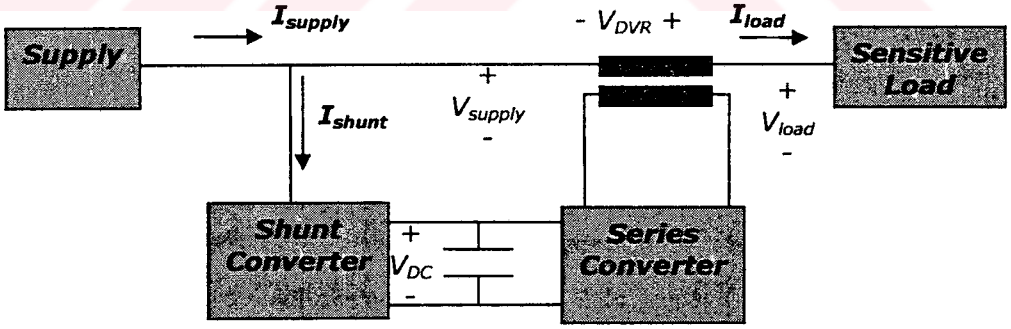

Figure 4.1 DVR with no energy storage and supply side connected converter

If no step-down transformer is introduced, the DC-Link voltage is approximately equal to the peak phase-phase value of the supply voltage. During a

voltage sag, the DC-Link voltage will drop with respect to the remaining sag voltage according to:

$$V_{DC} \cong \sqrt{6} * V_{Supply} \cong \sqrt{6} * V_{Sag} \tag{4.1}$$

where V_{DC} and V_{Supply} are the DC-Link Voltage and the rms supply voltage respectively. V_{Sag} is the phase voltage during a sag. The power and current handled by the converters can be approximated to:

$$P_{Shunt} = P_{Serie} \cong 3 * (1 - V_{Sag} / V_{Rated}) * P_{Load} \tag{4.2}$$

$$I_{Serie} = I_{Load} \tag{4.3}$$

$$I_{Shunt} \cong \frac{(1 - V_{Sag} / V_{Rated})}{V_{Sag} / V_{Rated}} * I_{Load} \tag{4.4}$$

P_{Shunt} and P_{Serie} are the three-phase powers handled by the shunt and series converter respectively. V_{Rated} is the rated supply voltage and I_{Load} is the rated load current.

In this topology the power handled by the shunt converter is proportional to the missing voltage and in case of severe sags the current drawn by the converter rises significantly. For example in case of a 50% voltage sag, the current through the shunt converter increases at a rate of 100%, that is $I_{Shunt} = I_{Load}$.

4.1.1.2 Load Side Connected Shunt Converter

In load side connected shunt converter topology (Figure 4.2), the DC-Link voltage is almost constant by injecting sufficient voltage (V_{DVR}).

$$V_{DC} \cong \sqrt{6} * V_{Load} \cong \sqrt{6} * (V_{Sag} + V_{DVR}) \tag{4.5}$$

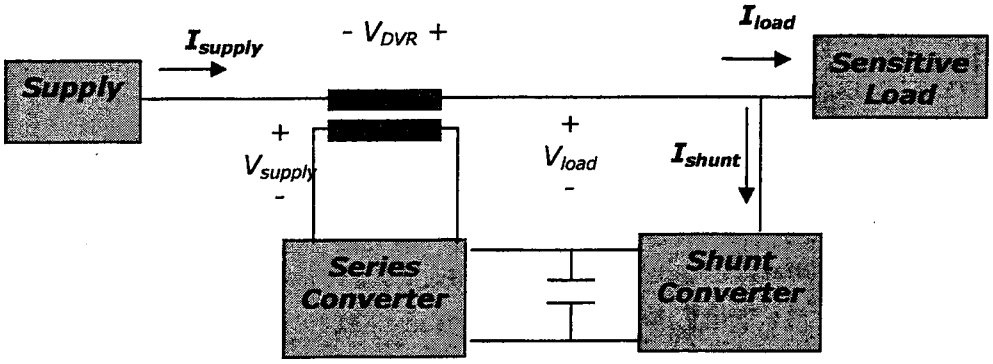

Figure 4.2 DVR with no energy storage and load side connected converter

The current relationships are approximately as:

$$P_{Shunt} = P_{Serie} \cong \frac{(1 - V_{Sag} / V_{Rated})}{V_{Sag} / V_{Rated}} * P_{Load} \tag{4.6}$$

$$I_{Serie} = I_{Supply} \cong \frac{P_{Load}}{3 * V_{Sag}} \tag{4.7}$$

$$I_{Shunt} \cong \frac{(1 - V_{Sag} / V_{Rated})}{V_{Sag} / V_{Rated}} * I_{Load} \tag{4.8}$$

The relationships show the main drawback of the topology, that is the high current through the series converter. For example in case of a 50% voltage sag the current through the series converter increases at a rate of 200% (required supply current doubles) and through the shunt converter, current equal to I_{Load} is drawn. This topology not only provides a clean an controlled voltage input to the rectifier, but also results in an overload rating for the inverter during non-sagged voltage conditions.

Another important drawback of the topology is the distorted current drawn by the passive shunt converter, which will significantly degrade the quality of the load voltage.

4.1.2 DVR Topologies with Energy Storage

Storage of energy requires a great cost, but the strain on the grid connection is lower. If the grid that the DVR is connected is weak, than topologies with energy storage should be applied in order to increase the performance of the DVR.

4.1.2.1 Variable DC-Link Voltage

Storage of energy in the DC-Link capacitors as shown in Figure 4.3 is a common solution for DVRs. The topology is simple and the DC-Link voltage is variable.

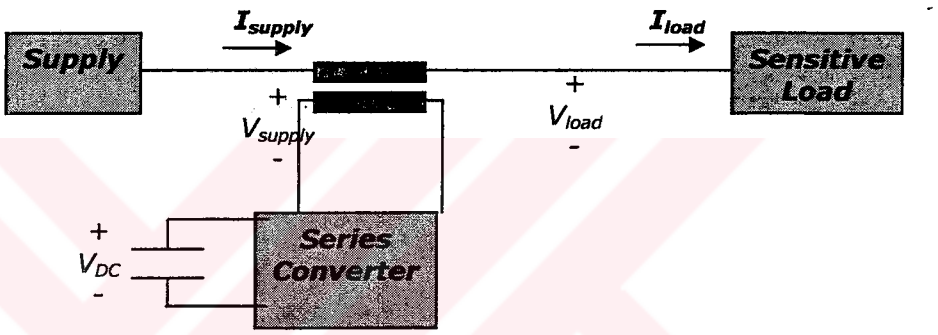

Figure 4.3 DVR with energy storage and variable DC-Link

The energy stored in the capacitor is calculated with the common equation:

$$E_{Storage} = \frac{1}{2} C_{DC} V_{DC}^2 \tag{4.9}$$

During a voltage sag, the voltage on the DC-Link capacitor decays exponentially such that in case of a long voltage sag the performance of the DVR decreases significantly.

$$P_{Serie} \cong (1 - V_{Sag} / V_{Rated}) * P_{Load} \tag{4.10}$$

This solution proposes a relatively simple power topology. The charging of the DC-Link may be supplied either from a low rated auxiliary charging converter or from the series converter. In this topology the efficiency of the energy storage is lower than the constant DC-Link voltage topology.

4.1.2.2 Constant DC-Link Voltage

In the constant DC-Link voltage topology (Figure 4.4), the DC-Link voltage is held constant by transferring necessary energy from a large storage to a small rated DC-Link. Super Magnetic Energy Storage (SMES), batteries or super capacitors with a highly rated energy conversion converter supplies the DC-Link with necessary energy.

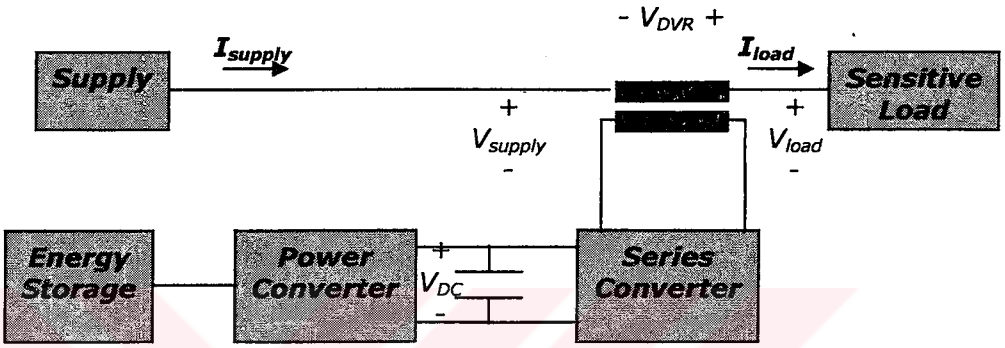

Figure 4.4 DVR with Constant DC-Link Voltage

The DC-Link voltage is almost held constant and the ratings of the converter can be calculated to:

$$V_{DC} = constant \tag{4.11}$$

$$P_{PowerConverter} = P_{Serie} \tag{4.12}$$

$$P_{Serie} \cong (1 - V_{Sag} / V_{Rated}) * P_{Load} \tag{4.13}$$

In performance is improved with respect to the variable DC-Link solution, but the equipment costs and the complexity of the power circuit increases.

4.1.3 The Comparison of Topologies of DVR

The topologies that may be applied to the DVRs have been covered and the advantages and disadvantages with respect to each other have been given. The analysis shows that the topology with load side connected shunt converter has been ranked as the best topology to be applied with low cost and complexity. But note that

negative grid effects and high rated series converter requirements may disqualify the solution for certain applications. For example a DVR with this kind of topology will not be suitable for weak grids.

The constant DC-Link voltage topology has been considered to be the second best of the topologies with performance. But the complexity, converter rating and overall costs are the drawbacks of this system.

In case of severe and long voltage sags, the performance of variable DC-Link voltage topology is found to be poor and ranked as the third. But the simple topology and converter rating is considered to be a plus.

Finally source side connected shunt converter topology is considered to be the worst of all topologies. Uncontrollable DC-Link voltage which will be surely proportional to the sag voltage and the non-symmetrical current which will be drawn in case non-symmetrical faults are the negatives of this system. Design of an active converter instead of passive shunt converter may clear some drawbacks of the system but this will increase the complexity of the system dramatically.

4.2 INJECTION TRANSFORMER OF DVR

In order to boost and couple the independent and arbitrary voltage waveforms to the line, three single-phase injection transformers are required. Injection transformer plays a crucial role in the design of the DVR. Its electrical parameters affect the performance of the restoration system dramatically. The following parameters of the transformer are to be determined [16]:

- The MVA Rating
- The primary winding voltage and current ratings
- The turn-ratio which, in turn, determines the secondary winding voltage and current ratings
- The short-circuit impedance

In order to determine these parameters the following system characteristics should be known:

- The MVA rating of the sensitive load to be protected
- The maximum allowable voltage drop across the transformer
- The characteristics of the expected voltage sags to be compensated for

- The design of the harmonic filter system
- The selection of the switching devices
- The energy storage capacity and the voltage restoration control strategy

4.2.1 Primary Voltage Rating

According to our voltage injection strategy, the primary voltage rating of the injection transformer is determined. It is clear that the in-phase voltage injection results in maximum voltage boost that is the magnitude of the injection voltage is minimized. (3.1) will be valid in case of in-phase voltage injection and the primary voltage rating of the injection transformer will be calculated with this equation..

In cases where phase-angle shift occurs and we inject a voltage to compensate for the difference between the sag and the pre-sag voltages then the rated primary voltage of the injection transformer should be calculated with (3.2).

As stated before, the minimum energy injection concept will increase the magnitude of the injected voltage and the primary voltage rating of the injection transformer should be calculated as given in (3.3).

Another important point while choosing the primary side voltage rating of the injection transformer is the filtering system applied to the DVR. With the application of the inverter-side filtering system, the primary voltage rating of the injection transformer can be calculated by one of the above equations since the inverter-side filter will block the harmonic currents entering the transformer thus the impact on the injection transformer current rating may be neglected.

The line-side filtering system as shown in Figure 4.10, the high-order harmonic currents will penetrate through the injection transformer and they will carry harmonic voltages. The equivalent circuit of the DVR and the system is given in Chapter 4.4.1 with details. At this point it is suffice to say that with the n^{th} harmonic voltage across the primary-side of the transformer is denoted as $V_{(n)}$, the primary-side voltage rating of the transformer should be:

$$V_{iR} = \sqrt{V_i^2 + \sum_{l}^{M} V_{(n)}^2} \tag{3.14}$$

Where V_i is calculated using (3.1) (3.2) or (3.3) whichever appropriate.

4.2.2 Primary Side Current Rating

The primary side current rating of the injection transformer is primarily determined by the load current characteristics since the DVR is a series connected device. However while sizing the current carrying capability, the effects of the high-order harmonics should be evaluated and included in the calculations. The penetration of the high-order harmonics are dominated by the inverter system applied.

As stated before the inverter-side filtering system will not allow the high-order harmonics to penetrate through the injection transformer thus the primary side current rating will be determined by the load current characteristics.

Line side filtering scheme requires more calculations since the high-order harmonics generated by the inverter will affect the current carrying capability of the injection transformer. The currents can be calculated based on the equivalent circuits shown in Figure 4.10. Suppose the n^{th}-order harmonic current is $I_{(n)}$, given the rated load current I_{rl} as the current rating of the primary side of the injection transformer can be calculated using:

$$I_{TR} = \sqrt{I_{rl(1)}^2 + \sum_{l}^{M} I_{(n)}^2} \tag{4.15}$$

Another point while choosing the primary current rating of the injection transformer, the topology that will be applied should be analyzed and the effects of topology to the current rating should be considered. Among the topologies investigated in Chapter 4.1, the load side connected shunt converter topology increases the supply current demand as calculated in (4.7) and thus in case of application of this topology, (4.8) should be multiplied with the calculation of (4.7) (The maximum sag voltage to be corrected should be known).

4.2.3 The MVA Rating

With the current and voltage rating obtained from equations (4.14) and (4.15), the capacity of the injection transformer may be obtained with:

$$S_i = K_{Si} * V_{ir} * I_{Tr} \tag{4.16}$$

where K_{si} is the safety margin.

4.2.4 Turns-Ratio Selection

The turns-ratio of the transformer is interrelated with the secondary voltage and current ratings. The secondary side parameters should be determined with the commercially available switching devices and DC-Link capacitors with optimum cost. In [16], a method for the selection of turns-ratio of the injection transformer is proposed. The main idea of the method is systematically adjusting the turns-ratio until there exist commercially available switching devices with proper current-carrying capability, blocking voltage and reasonable cost.

4.2.5 Short-Circuit Impedance Considerations

The short-circuit impedance will affect the fault current through the transformer in case of a downstream fault, the design of the filtering system and the voltage drop across the transformer under steady-state conditions.

If the inverter-side filtering system is applied, the equivalent circuit of the DVR is drawn in Figure 4.5. Here R_1, L_1, R_2 and L_2 are the leakage resistance and reactance of primary and secondary sides respectively and Z_m is the magnetizing impedance of the transformer. L_f and C_f are the inverter side filter elements. Finally R_v represents the total conduction voltage drop caused by the switches and the diodes. Since Z_m is larger compared to R_2 and L_2 and R_v is normally negligible, this circuit can be further simplified as Figure 4.6 where $L_k = L_1 + L_2$ and $R_k = R_1 + R_2$.

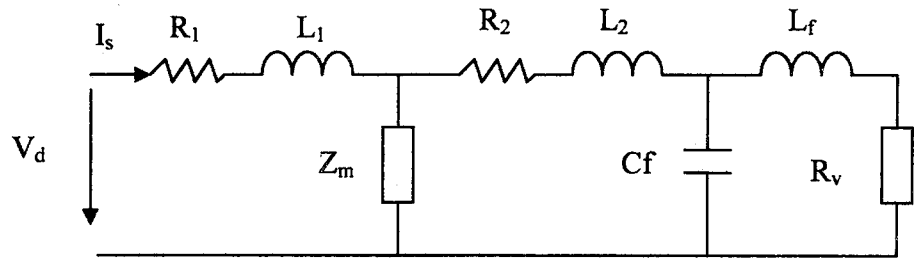

Figure 4.5 Equivalent circuit of DVR with inverter side filter

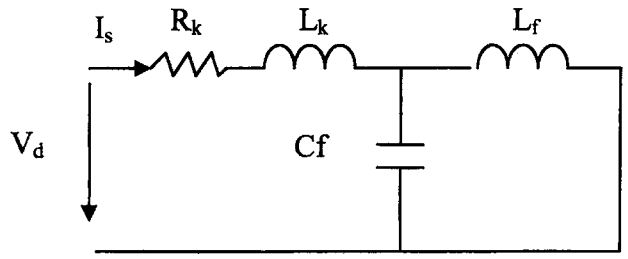

Figure 4.6 Further simplification of inverter side filter

Since during the steady state operation, we do not want our DVR to have a voltage drop, let's say V_d , below a specific limit, than the short-circuit impedance should satisfy:

$$\sqrt{R_k^2 + w^2(L_k + L_f/(1-w^2 L_f C_f))^2} < \frac{V_d}{I_s} \tag{4.17}$$

With the application of the line side filter, the equivalent circuit is as shown in Figure 4.7. The above simplifications are also valid for this circuit. Then in order to meet the voltage drop requirement, the short-circuit impedance should be as:

$$\sqrt{R_k^2 + w^2 L_k^{\,2}} < \frac{V_d}{I_s} \tag{4.18}$$

From the equation (4.18), in the line-side filtering scheme, the parameters of the injection transformer determines the voltage drop on the DVR. Therefore, choosing an injection transformer with lower leakage inductance seems to be preferable.

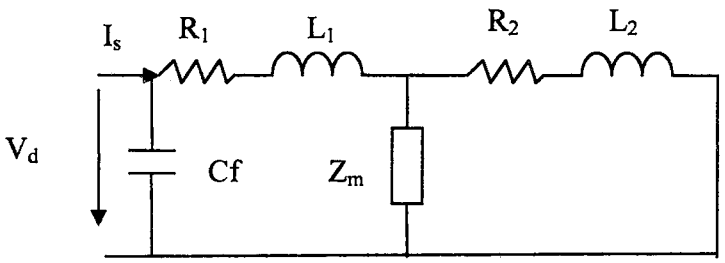

Figure 4.7 Equivalent circuit with line side filter

4.3 INVERTER OF THE DVR

The DVR will be connected at the distribution system of the load which will require high voltage injection magnitude. Therefore the injection transformer will step-up the voltage generated by the PWM Voltage Source Inverter (VSI). This event will require inverter rating to be low in voltage and high in current due to the application of step-up injection transformer.

The inverter will require an inductance to reduce the current ripple, but introduction of a large inductance (L_f in case of an inverter-side filter and L_k in case of a line side filter) will increase the DVR impedance thus resulting in an unwanted voltage drop on the DVR. Choosing a more complicated inverter topology will help to reduce the DVR impedance, current ripple and switching frequency but the cost and the complexity of the system will increase gradually.

The basic inverter topologies that may be applied to the DVR are the two-level half bridge, the three-level half bridge and the three-level full bridge inverter topologies (Figure 4.8). Several other multilevel topologies that may be applied are found but these will be in cost of increased the complexity of the system and the benefits will not be that much. Among these, two-level half bridge and the three-level full bridge inverter are the most common inverter types.

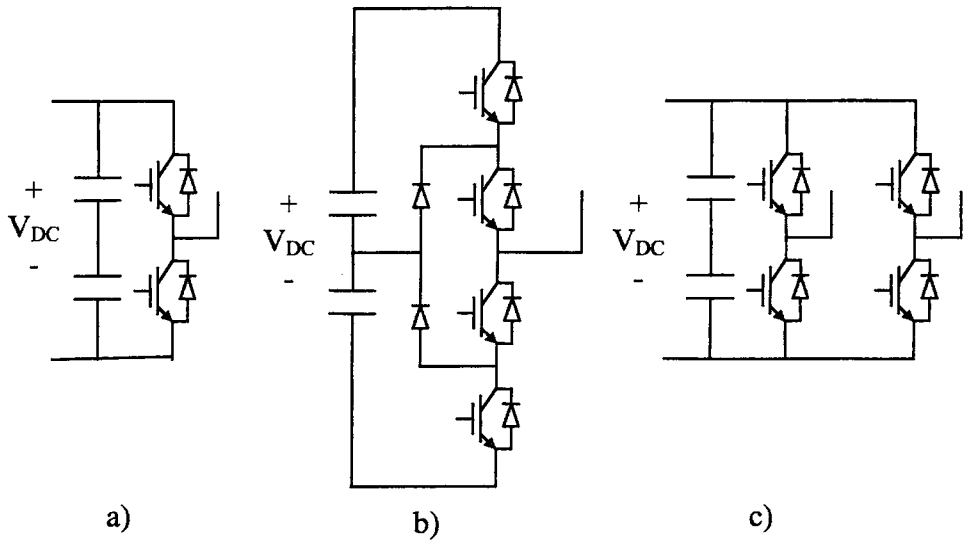

Figure 4.8 Basic inverter types for a DVR a) two-level half bridge

b) three-level half bridge c) three-level full bridge

For the semiconductor switches IGBTs are the commonly used ones which are suitable for series connection. But the new Integrated Gate-Commutated Thyristors (IGCT) technology offers proper semiconductors for series connection which have higher current ratings [8]. The primary drawback of the inverter is the high current rating of the semiconductors due to the step-up injection transformer. Therefore these semiconductors should handle the full load current during the normal steady state operation and an addition to this during the voltage sags, the injected power will flow through these semiconductors which will significantly increase the current rating of the semiconductors.

4.4 FILTERING SCHEMES IN THE DVR

One of the important problems of the DVR that should be solved is the attenuation of the high-order harmonics generated by the voltage source PWM inverter. Basically there are two types of filtering systems that may be applied to the DVR, inverter side filter filtering and line side filtering (Figure 4.9) [17][18]. The two types of filtering systems have advantages and disadvantages to each other.

Briefly the inverter side filtering scheme has the advantage of being closer to the harmonic source thus high-order harmonic currents are prevented to penetrate into the series injection transformer but has the disadvantage of causing voltage drop and phase-angle shift in the fundamental component of the inverter output. The advantages and the disadvantages of the inverter side filtering system are visa versa for the line side filtering system. In the line side filtering system harmonic currents penetrate into the series injection transformer but the voltage drop and phase-shift problem does not disturb the system.

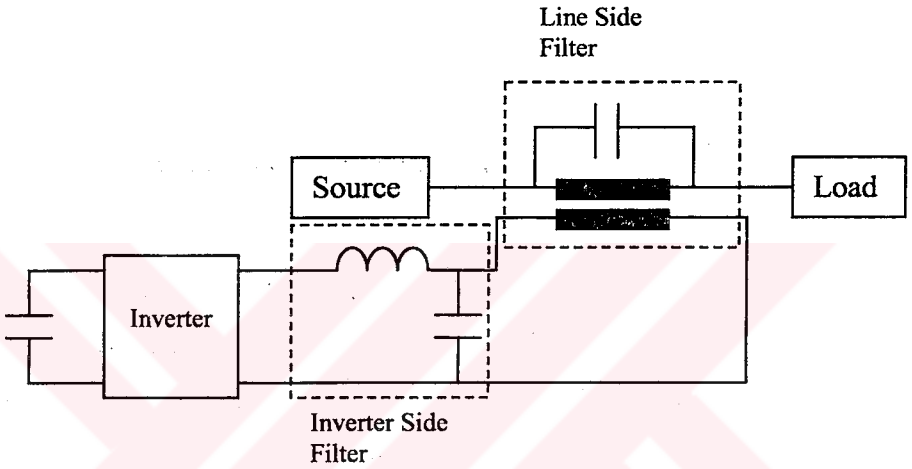

Figure 4.9 DVR Filtering Schemes

While choosing the filtering system, our primary concern is the attenuation of the harmonics. The mitigated load voltage THD value should be kept between the limits determined by the standards. Besides our primary concern, due to the filtering scheme, the amount of increase in the rating of the inverter, the size of the injection transformer should be evaluated and optimized according to our load characteristics.

4.4.1 Line Side DVR Filter

One of the filtering scheme that may be applied is the line side DVR filter. The equivalent circuit of the filter and the system is illustrated in Figure 4.10 where V_s represents the equivalent source of the power system with $(R_e + jwL_e)$ being the equivalent impedance of the system external to the DVR. V_{si} represents the voltage

on the inverter-side and considered as a harmonic source. R_{Ti} and L_{Ti} are the resistance and leakage inductance of the series injection transformer respectively. Our primary concern C_f is the filter capacitor that should be chosen in order to satisfy our requirements.

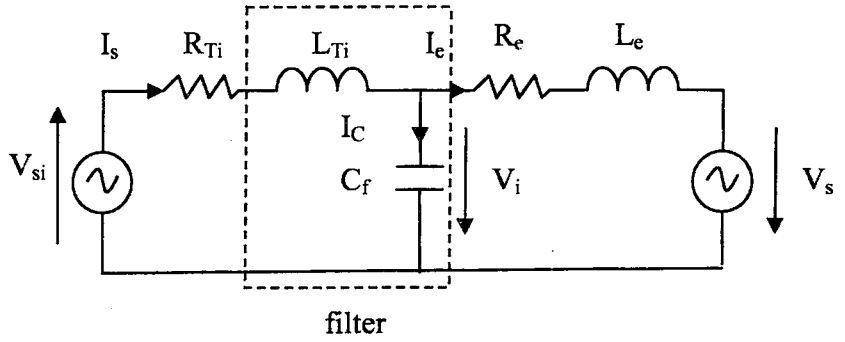

Figure 4.10 Equivalent circuit for line side filter

From Figure 4.10, the filtering operation may be observed, that is with the help of L_{Ti} , the leakage inductance of the series injection transformer, and C_f, the filter capacitor, the harmonic components are provided with a shunt path and attenuated with the proper selection of the filter capacitor.

In order that the high-order harmonics appearing at V_i is attenuated to a permissible level, the capacitor should chosen to satisfy:

$$\left|Z_{es(l)}\right| = K_f \left|Z_{e(l)}\right|, K_f >> 1 \tag{4.19}$$

Where $Z_{es(l)} = R_e + jlw_0L_e$ and $Z_{C(l)} = -j / lw_0C_f$ ($w_0 = 2\pi f_0$, f_o is the fundamental frequency, l is the order of the lowest harmonic to be attenuated. From Figure 4.10, if the n^{th} order harmonic generated by the inverter is represented by $V_{si(n)}$ and $V_{i(n)}$ represents the harmonic voltage across the filter capacitor where n = l, l+1, l+2, ..., M, then $V_{i(M)}$ is the highest harmonic order to be attenuated. The following relationship can be obtained with the consideration of (4.19):

$$\frac{V_{i(n)}}{V_{si(n)}} = \frac{1}{\sqrt{(1-(nw_o)^2 L_{Ti}C_L)^2 + (R_{Ti}nw_0C_L)^2}} \tag{4.20}$$

Our primary concern in choosing the filter capacitor is not to exceed the permissible THD level at the source voltage level which is denoted by K_{THD}. The

IEEE standards can be obtained from [18], and [19] Thus the permissible total harmonic voltage (V_T) across the capacitor can be calculated using:

$$V_T = K_{THD} V_p \tag{4.21}$$

To satisfy the THD requirements for the load side voltage of the DVR, from (4.20) C_f should be selected such that:

$$\sqrt{\sum_{n=l}^{M} V_{i(n)}^2} = \sqrt{\sum_{n=l}^{M} \frac{V_{si(n)}^2}{(1-(nw_o)^2 L_{Ti} C_L)^2 + (R_{Ti} n w_0 C_L)^2}} < V_T \tag{4.22}$$

Theoretically the solution of above equation will result with the value of C_f based on the permissible THD value. But the solution requires high order algebraic equation. The methods to manipulate and simplify (4.22) are given in [17]. The final equation obtained by the simplification of (4.22) results in:

$$C_f \geq \sqrt{\sum_{n=l}^{M} V_{si(n)}^2} /(K_{THD} V_p) /((Iw_0)^2 L_{Ti}) \tag{4.23}$$

Finally, in order to determine the filter capacitor value, we should specify the THD requirement at the load side of the DVR and the harmonic spectrum of the inverter output for specific injection transformer parameters.

Note that from (4.23) it is clear that the bigger the filter capacitor value, the better harmonic attenuation. But this is not true since the increasing value of C_f will overrate the inverter. Therefore while selecting the capacitor value, the effects on the inverter rating should be investigated in detail. Note that the assessment of C_f may be achieved by examining the relationship between the DVR current and the load current at the fundamental frequency. Reference [17] represents a complex analytical solution for this problem.

In order to calculate the high-order harmonic currents, the simplified circuit in Figure 4.11 may be applied. The equation for the high-order harmonic current and the current in the fundamental frequency through the capacitor is:

$$I_{C(n)} = n w_0 V_{si(n)} \sqrt{(n w_0 C_L R_{Ti})^2 + (n^2 w_0^2 L_{Ti} C_f - 1)^2} \tag{4.24}$$

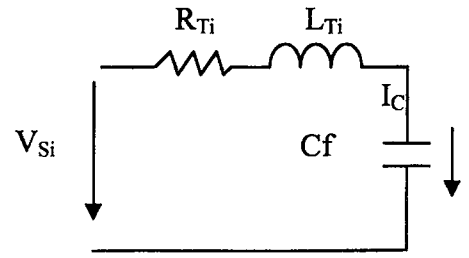

Figure 4.11 Simplified circuit for line-side filter current calculations

Consequently the rms capacitor current can be obtained as:

$$I_{Cr} = \sqrt{I_{C(1)}^2 + \sum_{l}^{M} I_{C(n)}^2} \tag{4.25}$$

The voltage across the capacitor will be the same as the injection transformer primary voltage rating. The same calculations will be valid as explained in Chapter 4.2.1 and for the V_{Cr} value, the primary voltage rating equation to be applied may be used. In case of a more detailed computation, (4.21) should be considered for the voltage rating, since the total harmonic voltage will be seen on the capacitor value.

Finally the rating of the capacitor can be calculated using where k_{sc} is a safety coefficient ranging from 1.0 to 1.15:

$$S_{Cr} = k_{Sc} * V_{Cr} * I_{Cr} \tag{4.26}$$

4.4.2 Inverter Side DVR Filter

The principles for the line-side filter design are also valid for the inverter side filter design. As shown in Figure 4.12, the (4.19) can be also used but with $Z_{es(l)} = (R_e + R_{Ti}) + jlw_0(L_e + L_{Ti})$ and $Z_e = -j / lw_0C_f$.

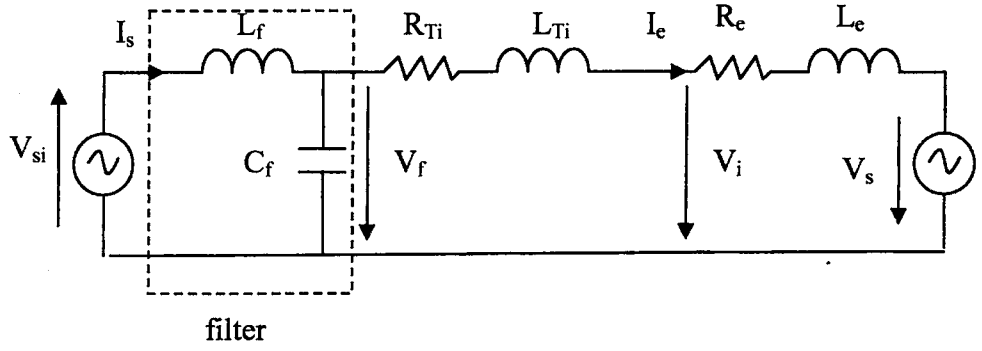

Figure 4.12 Inverter side filter circuit

In order to achieve the proper L_f and C_f values, this time the below equations should be satisfied (K_i is the turns ratio of the injection transformer):

$$V_T = \frac{K_{THD} V_p}{K_i} \tag{4.27}$$

$$\sqrt{\sum_{n=1}^{M} V_{i(n)}^2} = \sqrt{\sum_{n=1}^{M} \left(\frac{V_{si(n)}^2}{(nw_0)^2 LC - 1}\right)^2} < V_T \tag{4.28}$$

From the equations, the higher value of the capacitor seems to do better but again the inverter rating problem will arise in case of very high capacitor value. In literature, the inverter side filter concept is analyzed deeply therefore it will not be discussed further [17] [18].

4.5 Harmonic Voltage Drops on the DVR

From Figure 4.6 and Figure 4.7, it is clear that the DVR introduces a series capacitance and reactance to the line according to the filtering scheme applied. The harmonic currents of the load will generate harmonic voltage drops on the device degrading the load voltage. During the steady-state and the operation periods of the DVR these harmonic voltage drops can be an annoying problem. Furthermore application of a load side connected converter topology will generate harmonic currents due to the shunt rectifier. These harmonic currents may further disturb the DVR.

Figure 4.13 illustrates the line side filter circuit during the steady state. R_{Ti} and L_{Ti} are the leakage inductance and series resistance of the injection transformer referred to the primary side and C_f is the filter capacitance. In the figure, the short-circuiting semiconductor's conduction losses have been ignored. The corner frequency of the system can be calculated from:

$$f_c = \frac{1}{\sqrt{L_{Ti}C_f}} * \frac{1}{2\pi} \tag{4.29}$$

A typical response of this circuit is shown in Figure 4.14. The characteristics depend on the filter capacitance and the injection transformer parameters. The resonance frequency of the circuit is also the tune frequency of the filter and current harmonics at this frequency will be magnified and unwanted harmonic voltage drops on the DVR may occur. Due to the series resistance of the injection transformer (R_{Ti}), these harmonics will be damped (Figure 4.15). But the corner frequency will not vary with the varying series resistance. Special attention may be required, if the load current contains harmonics at the resonance frequency of the DVR. These harmonics may be magnified further by the DVR.

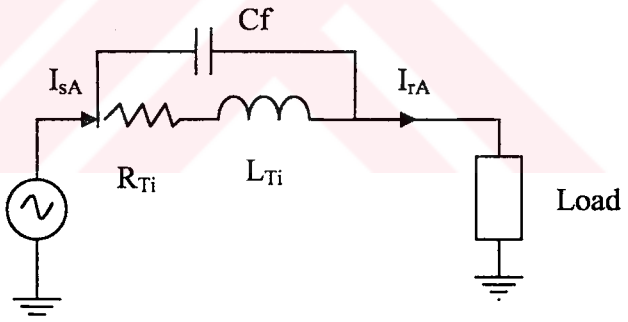

Figure 4.13 The illustration of DVR with line side connected filter circuit during steady-state

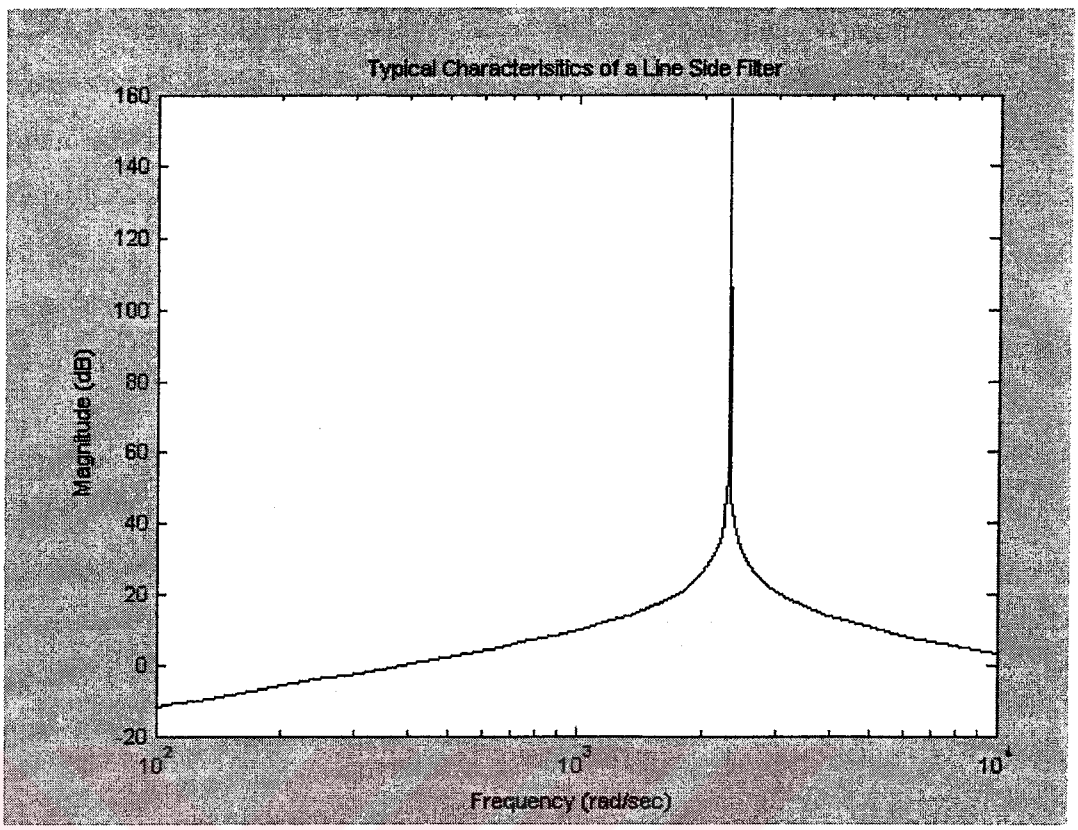

Figure 4.14 The frequency response of the DVR with line side connected filter with zero series resistance of injection transformer

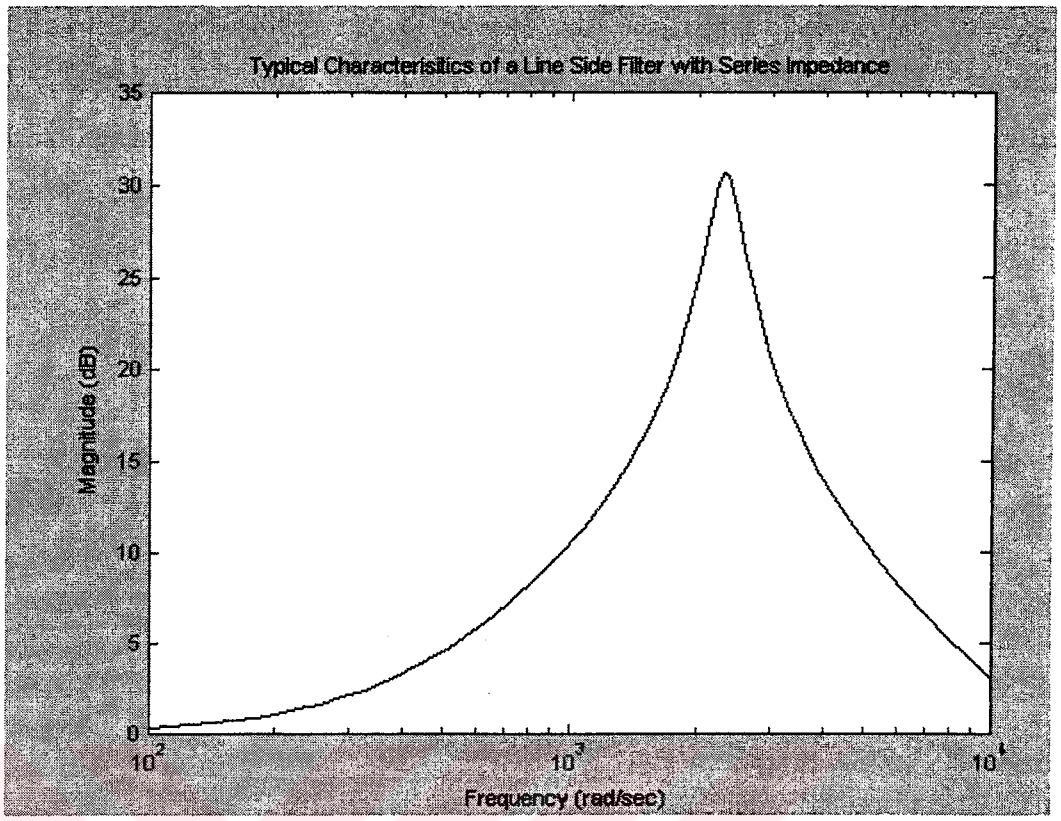

Figure 4.15 The frequency response of the DVR with line side connected filter with series resistance of injection transformer

CHAPTER 5

SYSTEM DESCRIPTION AND DESIGN

The history of the DVRs applied to the power systems does not go very past. They have been recently introduced therefore there does not exist too many examples. In this chapter the installed DVR applications will be introduced and the aim of the study the DVR with load side connected converter topology that is simulated will be given in detail with the design considerations and the power system that the DVR is connected will be given.

5.1 FIELD APPLICATIONS OF THE DVR

Up to now, there have been a few applications of the DVR throughout the world. The world's first DVR was installed on the Duke Power 12.47-kV (MV) distribution system in South Carolina, USA in August 1996 by Siemens [21]. It was assembled to protect a highly automated rug manufacturing plant from voltage sags, swells and phase imbalance.

Today DVR systems are protecting large loads up to 50 MVA in many sectors. If the typical injection capability of 50% is used, the rating of the DVR will be the half of the rating of the load. The installations of the DVR inverters are found to be feasible up to 2MVA therefore in order to achieve larger rating requirements, DVR modules are paralleled which consists of a master module with connected slave modules. In such arrangements the master module performs the voltage regulation function and the slaves will contribute current to the output. Here only one injection transformer with a common low voltage bus which is the point of current summing

junction for the filtered outputs of the inverters is used. The first Multi-Module DVR was installed in a paper mill plant in Scotland with a load of 47MW which is connected to the 11kV distribution line.

The energy source of the applied DVRs are generally fed from either from the auxillary supplies or from the line with the rectifiers connected to the load side.

5.2 THE APPLIED LOAD SIDE SHUNT CONNECTED CONVERTER TOPOLOGY

PSCAD / EMTDC V3.0.6 software tool has been used during the simulations. It is a powerful software package for the simulations of power systems combined with necessary control attributes. This software is powerful enough to handle the simulations of the DVR.

5.2.1 The Power Circuit

In order to analyze the response and the performance of the DVR, the power circuit shown in Figure 5.1 has been chosen. The power circuit resembles a typical large sized plant. Our aim is to have a corrected voltage at our load which is denoted as the "Sensitive LOAD" in the figure. For a complete power system, parallel loads have been inserted but no correction of voltage will be done on them therefore they will suffer from the voltage sag.

Our load which resembles a typical large plan fed from the 34.5kV distribution system is rated at 18MVA. The sensitive load assumed to be pure resistive and inductive therefore contains no harmonics.

The fault generation has been achieved by locating a fault generator near to the source with a variable resistance and to the low voltage side of the parallel loads. These will allow a precise control on the depth and type of the voltage sags generated. Note that the voltage sags caused by the faults on the parallel lines will show similar characteristics with the generated voltage sags.

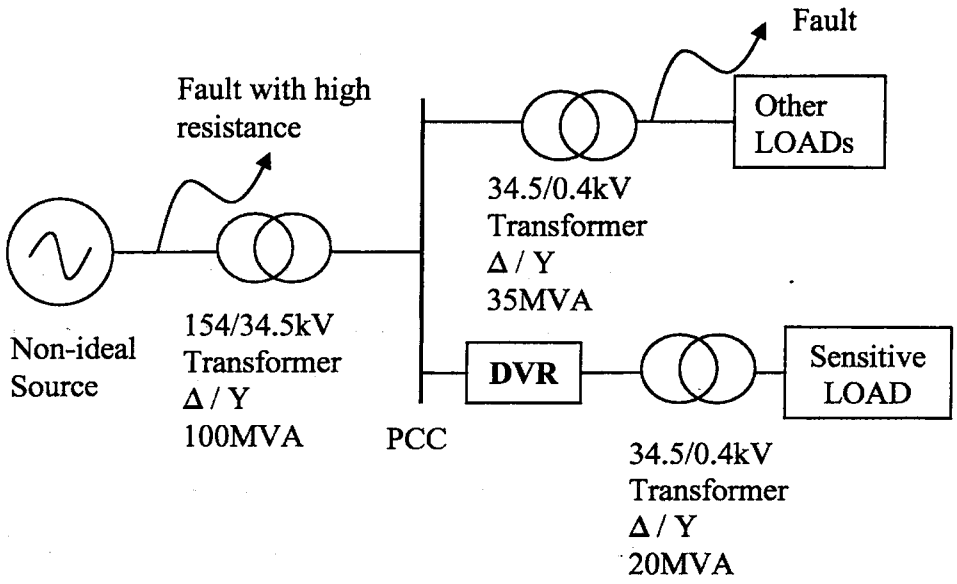

Figure 5.1 The Power Circuit Simulated

5.2.2 The DVR

The DVR have been inserted to the 34.5kV feeder before the stepdown transformer of our sensitive load. By this location, the whole sensitive load will be protected against the voltage sags. The primary aim of the device is to mitigate the single phase voltage sags up to 0.5 p.u. and three-phase voltage sags up to 0.4 p.u. with duration about 100-200ms. However with the topology applied, there will be no limit on the duration of the voltage sag to be corrected except the thermal limits that may be reached during the mitigation of the sags.

5.2.2.1 Topology

The utility grid is assumed to be strong, so that the DVR topology with no energy storage and the DC-link fed from the load side connected shunt converter (Figure 4.2) have been chosen. The primary reason for choosing this topology is the higher level of performance with respect to others followed by the low complexity and cost of the system.

Furthermore since no energy storage is required, this topology will be able to correct voltage sags with very long durations. Feeding the DC-link from the load side will also help in deep voltage sag cases with respect to the source side connected

converter topology and also increase the control on the DC-link voltage since the DC-link will be fed from the corrected load voltage. During deep voltage sags the DC-link voltage will stabilize at a relatively high voltage level therefore the complexity of the control of the DVR will be less because of the relatively stable DC-link voltage.

Besides the advantages of this topology, there exist important disadvantages that should be considered with respect to the application field. At the first glance the grid will be strongly affected by the shunt converter thus the grid that the DVR to be connected should be strong grid in order to reduce the effects of the system. For example in case of a three-phase 0.4 p.u. voltage sag, the line current requirement will approximately double. Secondly, the load side shunt connected topology will increase the series converter rating and the injection transformer because of the current magnitude increment as investigated in Chapter (4.1.1.2) thus in case of deep voltage sag correction requirement, the series converter rating will increase gradually. Another disappointing point for this topology is the high rating of the shunt converter. But except the variable DC-link storage topology, all other topologies surely require high rating shunt/charging converter.

5.2.2.2 Injection Transformer

With the increasing magnitude of the voltage sag, the current drawn from the supply will increase and the shunt converter should be sized considering the of the load rating and the maximum magnitude of the voltage sag to be mitigated in order to feed the DC-link during a long voltage sag. This current magnitude will also breed the necessity of the injection transformers to be sized larger than the other topologies. By chance, this overload rating of the injection transformer and the inverter will allow the DVR not to experience damage during over-current conditions on the load side.

The turns-ratio of the transformer has been set by considering the DC-link voltage and the magnitude of the maximum injection voltage. Therefore 11.20kV/1.60kV (2.2kV peak) primary and secondary voltage ratings have been found to be suitable for the applied DVR. Note that by this turns-ratio, the current of the semiconductors will be 7 times larger than the load current magnitude.

Another critical issue for the injection transformer is the voltage drop because of the leakage inductance. The transformers with low leakage inductance seem to be preferable but this property will increase the cost of the device. But for the line-side filtering scheme, the leakage inductance will help to attenuate the harmonics generated by the PWM inverter.

The single phase injection transformer's rating has been chosen to be 8MVA considering the criteria above. During the analysis of leakage inductance affects, the value has been varied between 0.04 p.u. and 0.08 p.u. .

5.2.2.3 DC-Link

Depending on the topology applied, no energy is stored at the DC-link, resulting in the lower size of the DC-link capacitors. The DC-link is fed via the step-down transformer connected to the load side and the uncontrolled rectifier. The step-down transformer decreases the line voltage to a proper level where there exist available large capacity DC-link capacitors in the market. But here there is a trade-off between the DC-link voltage and the semiconductor parameters. The greater the DC-link voltage, the lower the semiconductor currents due to the boosting injection transformer. Considering the DC-link capacitors on the market, 2200V for the DC-link has been chosen.

For the topology chosen, we do not need to store energy at the DC-link, in order words the capacitor magnitude will not be very large with respect to the topologies with energy storage. But the capacitor size will determine the voltage ripple on the DC-link and sizing it at lower values will result in large voltage ripples on the DC-link and degrade the performance of the DVR. It is clear that choosing larger DC-link capacitor will be better but the cost will gradually increase. Another effect of the topology applied, during the voltage sag mitigation operation of the DVR, the DC-link voltage will stabilize at a relatively high magnitude since the DC-link will be fed from the corrected load side. But the steady-state value will still be at a lower magnitude which will be determined by the sag magnitude because of the voltage drop on the shunt step-down transformer and the uncontrolled rectifier semiconductors due to high current drawn from the shunt branch of the DVR.

Since the DVR is supposed to mitigate voltage sags up to 0.5 p.u., roughly the DVR rating will be half of the load it protects. This will result in high current drawn from the DC-link in order to mitigate the voltage sag. And the current will be in pulses due to the PWM operation of the inverter. Therefore the DC-link should be sized to handle this large current and the capacitors should be able to supply these large current pulses.

The analysis on the DC-link capacitor consists of simulations with varying the capacitor value between 10mF and 80mF.

5.2.2.4 Attenuation of Harmonics

The attenuation of high order harmonics has been obtained by the line side filtering scheme. This scheme will lower the DVR impedance thus decrease the voltage drop on the DVR and ease the control strategy since no phase-shift will occur in the injected voltage. But the stress on the injection transformer will be much more with compared to the inverter-side filtering scheme therefore the rating of the injection transformer will be higher with respect to the inverter-side filtering scheme. The value of the filtering capacitor has been chosen to satisfy the equations in Chapter (4.4.1).

The parameters of the injection transformer is assumed to be fixed and with the alternating switching frequency the size of the filter capacitor has been changed in order to obtain a proper filtering operation. Note with increasing value of the filter capacitor, the current rating of the capacitor will be increased due to the decreasing impedance of the capacitor at the fundamental frequency and the harmonic frequencies. The voltage rating will be determined by the maximum injection limit of the DVR plus the allowable harmonic voltages that will satisfy the THD requirement of the load. The THD requirement for the applied DVR is 5% due to the voltage level of the power system (34.5kV) [20].

5.2.2.5 Inverter and the Switching of the Semiconductors

The three-level full bridge inverter topology with the IGBT semiconductors has been chosen for the inverter. By this topology the rating of the semiconductor

switches will be doubled and each of phases will be fed from the separated two legs of the inverter.

With the high turns-ratio of the injection transformer, the current magnitude of the semiconductors is very large. And during the stand-by operation the voltage drop on the semiconductors will degrade the steady-state performance of the DVR and increase the losses. Therefore semiconductors will low-voltage drop should be applied. The new Integrated Gate Commutated Thyristor (IGCT) technology offers high current, low loss semiconductors. But today these semiconductors require lower switching frequencies. The switching frequency will be determined by the load rating which will affect the inverter semiconductors current and voltage rating. Therefore in this study, the switching frequency of the inverter semiconductors has been varied and the resulting consequences of lower switching frequencies have been analyzed.

The reverse blocking voltage of the semiconductors is determined by the DC-link and they are 2200V for each power semiconductors.

5.2.2.6 Control Issues

The control method of the DVR is open loop control and the reference signals for the PWM inverter are generated as shown in Figure 3.15. The actual supply voltages (V_{sa}, V_{sb} and V_{sc}) is transformed in dq reference frames in positive sequence SRF and negative sequence SRF, the DC values are extracted and compared with the reference voltage DC values. Note that in case of unbalanced voltage sags, for the sake of complexity the DC values of the positive sequence SRF and negative sequence SRF have been extracted by applying FFT and obtaining the DC values which is gradually a slower method than the proposed methods in Chapter 3.5.4. The error signals are reduced by two low-pass filters for each SRF and transformed back into three-phase values and PWM modulated according to a uni-polar switching scheme. Another control parameter is the actual DC-link voltage (V_{DC}) value, which is taken into account for proper operation of the voltage controller. With this type of control, the mitigated load voltage will be in-phase with the pre-sag voltage.

The PLL output has been obtained from the PLL object of the PSCAD/EMTDC, therefore no implementation of PLL has been done. The

software's PLL object satisfies the requirement for obtaining the phase information of the source voltage.

In order to decrease the high dv/dt ratio on the injection transformer, PWM switching with zero states has been applied (Figure 5.2). The zero states are achieved by the SCO with the semiconductors described in Chapter 3.2.1.1.

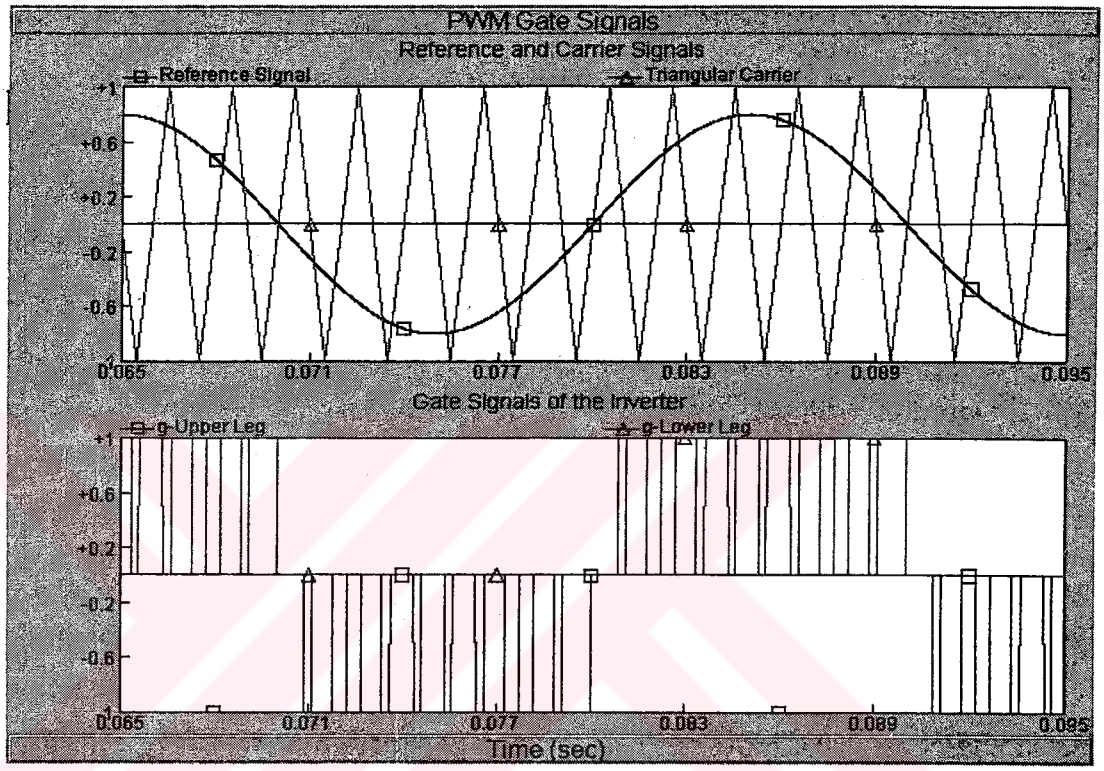

Figure 5.2 Triggering of Inverter

5.2.2.7 Simulated DVR

The simulated DVR is shown in Figure 5.3 for one phase of the system, where the shunt transformer, the rectifier and the DC-link will be common for all three phases.

Note that the protection issues have not been considered in the simulations. They will be important during the implementation of the DVR. Mechanical by-pass switches should be integrated to the system in order to isolate the DVR from the line it is connected during the maintenance and fault conditions. The short-circuit

operation of the DVR has been accomplished by switching the upper legs of the inverter as shown in Figure 3.2.

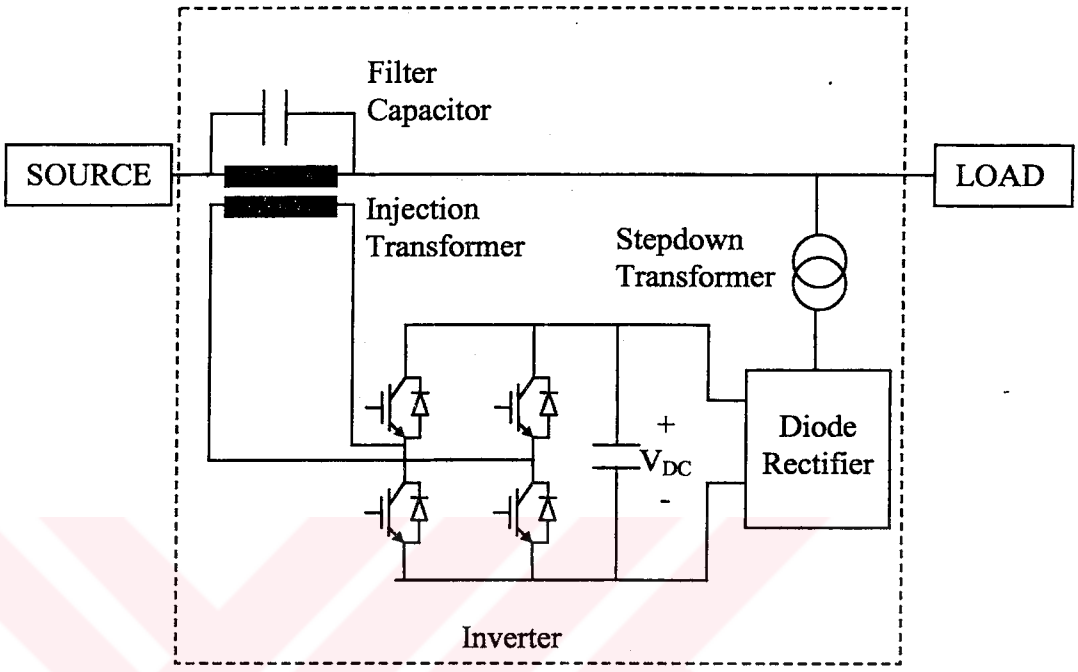

Figure 5.3 The Simulated DVR illustrated in one phase

5.2.2.8 Summary of Design Procedure

The critical points during the design process of a DVR have been given in this chapter. In order to gather all of the listed above, a systematic method for the design process has been illustrated in Figure 5.4 as a flowchart.

The selection of the turns-ratio of the injection transformer is interrelated with the the low voltage side voltage and current ratings which will determine the selection of the switching devices. Therefore the starting point has been chosen as the turns-ratio of the injection *transformer T(n).* Values should be adjusted such as *T(1)<T(2)<..T(n)*. In the figure, V_2 is the transformer low voltage side voltage rating while I_2 is the secondary current rating. Note that the DVR injection capability is not considered as a variable since this value will be determined by the site requirements.

The transformer's secondary ratings are calculated and it is checked whether there exists transformers with these ratings or such a design may be manufactured

with reasonable cost. The second step is the search for available semiconductors with these ratings. With these ratings, search whether there exist available DC-link capacitors on the market. After determining these parameters, the performance of the DVR should be verified by a simulation tool. After the verification of the performance, the cost of the device should be calculated. The temporary cost is stored at C_{temp} variable and if the calculated cost is smaller than the previously stored C_{temp} than this value is set as the temporary variable. Finally the whole process is repeated for the next turns-ratio value until there does not exist available components. The final results will be the parameters of the last C_{temp} which will give the optimum design parameters.

The major components that will determine the cost will be the semiconductors, the injection transformer and the DC-link capacitor. Note that the filter capacitance rating will be determined by the DVR voltage injection requirement therefore it can not be considered as a parameter. But it should be considered in the calculation of the total cost of the DVR.

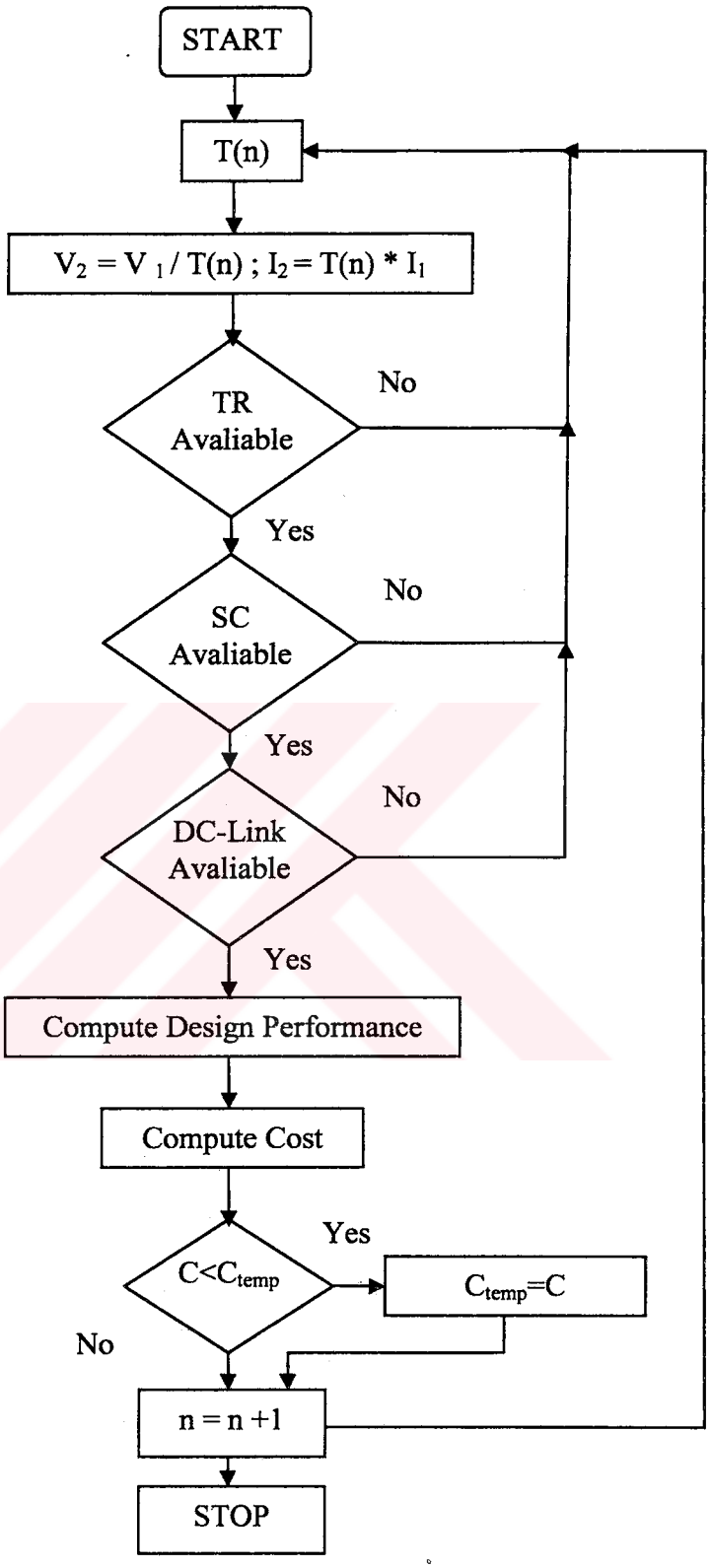

Figure 5.4 Flowchart of DVR design process

5.2.2.9 Simulation Parameters

Table 5.1 The Simulation Parameters

	Parameters Varied in the design work	Optimum values for DVR
LOAD		
Rating	18MVA	18MVA
Power Factor	0.95 lagging	0.95 lagging
Load Current THD	0%	0%
DVR		
Rated Capacity	9MVA	9MVA
Max. Injection Capability (Single Phase)	50%	50%
Max. Injection Capability (Three Phase)	40%	40%
Voltage Injection Duration	-	-
Injection Transformers		
Rated Capacity	8MVA	8MVA
Leakage Impedance	variable	0.05 p.u.
Primary Voltage Rating (rms)	11.20kV	11.20kV
Secondary Voltage Rating (rms)	1.60kV	1.60kV
No Load Losses	0.1 p.u.	0.1 p.u.
Magnetizing Current	0.4%	0.4%
Inverter		
Semiconductor Voltage	2200V DC	2200V DC
Semiconductor Current (peak)	variable	10kA
Switching Frequency	variable	1 kHz
DC-Link Capacitor		
Voltage	2200V DC	2200V DC
Current (rms)	variable	6 kA
Size	variable	80mF
Filter Capacitor		
Voltage (rms)	variable	11.20kV
Size	variable	75μF
Current (rms)	variable	400A
Shunt Transformer		
Rating	10MVA	10MVA
Primary Voltage	34.5kV	34.5kV
Secondary Voltage	1.65kV	1.65kV
Leakage Inductance	0.06 p.u.	0.06 p.u.
No load losses	0.1 p.u.	0.1 p.u.
Magnetizing Current	0.4%	0.4%
Rectifier Diodes		
Voltage (peak)	2.2kV	2.2kV
Current (peak)	10kA	10kA
Current (rms)	3.2kA	3.2kA

CHAPTER 6

SIMULATION RESULTS

PSCAD/EMTDC is an industry standard simulation tool for studying the transient behavior of electrical networks. The software has superior capabilities on power system modeling and user interface for all aspects of the simulation to be conducted to the users. Its comprehensive library of models supports most ac and dc of power plant components which makes the software perfect for the DVR simulations. Furthermore, useful tools and objects for construction of control algorithms are integrated within the software in order to establish fast and precise control blocks. For example, the PLL output has been obtained from the accurately designed "PLL Object" of the PSCAD/EMTDC. The simulation of the DVR has been constructed with modular sub-circuits which enables fast access to the bits of the whole circuitry. The power circuit and the modules constructed are given in APPENDIX A.1.

Additionally, for some mathematical calculations, data obtained from PSCAD/EMTDC has been processed on MATLAB. PSCAD/EMTDC can only show and compute up to 31^{th} harmonic, which results in very rough calculations for switching frequencies above 1 kHz. Therefore, the THD and harmonic magnitude spectrum calculations have been obtained from MATLAB with the programs given in APPENDIX A.2. The MATLAB outputs are shown in MS Excel graphics for clear view of the calculations.

First section of the simulation results chapter is composed of the effects of the parameters of the components on the DVR performance. The switching frequency,

the filter capacitor value, the leakage inductance of the injection transformer and the DC-link capacitor value has been modified and the consequences are analyzed with the help of the result tables given.

6.1 EFFECTS OF DVR PARAMETERS

6.1.1 The switching Frequency of the Inverter

In order to determine the switching frequency of the DVR, different simulations have been done and the effect of the switching frequency on the system has been analyzed. For the analysis to be consistent and reflect the worst case, the simulations are carried on the three-phase voltage sag with deepest sag magnitude (40%), on the same power circuit and the DVR branch connected to the same phase. Table 6.1 shows the parameters modified for observing the switching frequency effects. For consistency of the results with respect to each other, the leakage inductance of the injection transformer and the DC-link capacitance value has been set to 0.04 p.u. and 80mF respectively.

Table 6.1 Switching Frequency Simulations

Switching Frequency of Inverter	**0.5kHz**	**1kHz**	**1.5kHz**	**2Khz**	**3kHz**
Filter Capacitance Value	275μF	75 μF	25 μF	15 μF	10μF
	300 μF	100 μF	28 μF		15 μF
			35 μF		

For the same size of the filter capacitance, with the variation of the switching frequency, the results in Table 6.2 has been obtained. With lower switching frequency, the filtering performance of the line-side filter decreases significantly increasing the THD and the rms filter capacitance current increases because of the harmonics generated by the lower switching frequency of the PWM inverter. The fundamental component of the filter capacitor current does not change since this value only depends on the value of the filter capacitance for the same injected voltage magnitude.

Table 6.2 Effects of switching frequency with constant filter capacitor value

Switching Frequency	3kHz	2kHz
Filter Capacitance	15 μF	15 μF
THD	2.58%	4.70%
Filter Cap. Curr.	103A	169A
Filter Curr. (fund)	36A	35A
DC-Link Cap. Cur.	3.55kA	3.98A
Source Current (rms)	496A	495A

Since for a DVR at this large size, switching frequencies of 2kHz or 3Khz are only theoretical. For an applicable DVR as large as 10MVA, the switching frequency of the DVR should be decreased to proper levels. In order to keep the relationship between the filter capacitor and the switching frequency, all of the other parameters but the filter capacitor has been kept the same. In Table 6.3, with the decreasing switching frequency, in order to achieve the 5% THD limit on the load voltage, the value of the filter capacitor should be increased.

Table 6.3 Effects of switching frequency with variable filter capacitor value

Switching Frequency	3kHz	2kHz	1.5kHz	1kHz	0.5kHz
Filter Capacitance	10 μF	15 μF	28 μF	75 μF	275 μF
THD	3.22%	4.70%	4.22%	4.49%	4.95%
Filter Cap. Curr.	103A	169A	226A	380A	928A
Filter Curr. (fund)	24A	35A	70A	179A	658A
DC-Link Cap. Cur.	3.59kA	3.98A	4.31kA	5.63kA	9.68kA
Source Current (rms)	495A	495A	482A	510A	632A

Other switching frequency simulations and the effects can be observed from Table 6.4 and Table 6.5.

Table 6.4 Filter capacitor results at 1.5 kHz switching frequency

Switching Frequency	1.5kHz	1.5kHz	1.5kHz
Filter Capacitance	35 µF	28 µF	25 µF
THD	3.83%	4.22%	5.27%
Filter Cap. Curr.	226A	226A	243A
Filter Curr. (fund)	82A	70A	58A
DC-Link Cap. Cur.	4.38kA	4.31kA	4.36kA
Source Current (rms)	483A	482A	520A

Table 6.5 Filter capacitor results at 1 kHz switching frequency

Switching Frequency	1kHz	1kHz
Filter Capacitance	100 µF	75 µF
THD	3.78%	4.49%
Filter Cap. Curr.	408A	380A
Filter Curr. (fund)	240A	179A
DC-Link Cap. Cur.	5.60kA	5.63kA
Source Current (rms)	508A	510A

According to the results obtained from the filter capacitance value and switching frequency simulations, it is obvious that with the decreasing switching frequency, in order attenuate the harmonics generated by the PWM inverter, the size of the capacitor value increases. This will result in a filter design with overrated value. With the increasing capacitor value, the rms current of the filter capacitor increases significantly due the fundamental component (V_i / Z_C where $Z_C = -j / w_0 C_f$: Vi = injected voltage magnitude: $w_0 = 2\pi f_0$, f_o is the fundamental frequency) and the harmonic components of the PWM inverter. The injection transformer reflects the current of the filter capacitance to the inverter by the turns-ratio and this results in larger current drawn from the DC-link, consequently from the source.

6.1.2 Effect of Leakage Inductance of the Injection Transformer

For the 0.5 kHz switching frequency case, the filter fundamental and rms current is simulated to be enormous and it is obvious that this size is impossible to implement for a real system. At this point another parameter of the system, the

leakage inductance of the injection transformer may be varied to help the filtering of the harmonics.

From Table 6.6, if the leakage inductance of the injection transformer is changed from 0.04 p.u. to 0.08 p.u., the THD requirement can be satisfied with a lower valued filter capacitance. But increased value of the leakage inductance of the transformer will result in larger voltage drop on the DVR thus degrade the steady-state performance of the DVR. The voltage drops on the DVR can be calculated from Figure 4.7 and equation (4.18). The theoretical calculations according to (4.18) results in a voltage drop of 319V on the DVR which is 1.60% of the load voltage with 0.04 p.u. leakage inductance. From the simulations, 0.04 p.u. leakage inductance the voltage drop is calculated to be 1.78%. With the same calculations and simulations, for the 0.08 p.u. leakage inductance case the voltage drop is found to be 3.52%.

From the results, by increasing the leakage inductance of the injection transformer, the harmonic currents of the filter capacitance decreases but the fundamental component does not change.

Table 6.6 Effects of Leakage inductance of the injection transformer

Switching Frequency	**0.5kHz**	**0.5kHz**	**0.5kHz**	**0.5kHz**
Filter Capacitance	**300 µF**	**275 µF**	**275 µF**	**170 µF**
Tr. Leak. Ind.	**0.04 pu**	**0.04pu**	**0.08pu**	**0.08pu**
THD	4.37%	4.95%	2.25%	4.22%
Filter Cap. Curr.	960A	928A	754A	528A
Filter Curr. (fund)	724A	658A	689A	410A
DC-Link Cap. Cur.	9.67kA	9.68kA	6.56kA	6.07kA
Source Current (rms)	630A	632A	580A	524A

The similar simulations are carried on the 3 kHz switching frequency and the system has responded the same with respect to the 0.5 kHz case.

Table 6.7 Effects of leakage inductance of the injection transformer at 3 kHz switching frequency

Switching Frequency	3kHz	3kHz	3kHz
Filter Capacitance	6 µF	6 µF	10 µF
Tr. Leak. Ind.	0.04 pu	0.08pu	0.08pu
THD	5.09%	3.71%	3.26%
Filter Cap. Curr.	110A	53A	55A
Filter Curr. (fund)	14A	14A	23A
DC-Link Cap. Cur.	3.61kA	3.55kA	3.28kA
Source Current (rms)	498A	492A	488A

From the simulations on leakage inductance, effect of the injection transformer to the performance of the DVR is very important. This result is based on the line side filtering scheme applied. The series leakage inductance of the injection transformer is utilized for attenuation of harmonics therefore this value and the filter capacitor value determines the filtering characteristics. It is clear that application of an injection transformer with larger leakage inductance seems to be preferable at the design stage but the consequences will be larger voltage drop on the DVR and degrade the voltage level of the load at the full load conditions. This value can only be determined by the load voltage level requirement. Besides choosing an injection transformer with low leakage inductance, another solution for canceling the voltage drop on the DVR during the standby is injecting a small voltage to the line which will compensate the DVR voltage drop. This operation can be applied when the voltage drop on the DVR starts to disturb the load requirements.

6.1.3 DC-link Capacitor Value

In order to simulate the effect of the DC-link capacitor value to the performance of the DVR, simulations at 1.5kHz switching frequency has been chosen and the effect of the DC-link capacitance value on the performance of the DVR has been analyzed. As seen from Table 6.8, the increased value above a limit does not yield an increase in the performance of the device. This is an expected result since the load side connected converter topology is a non-energy storing topology. But below a specific limit the voltage ripple magnitude increases significantly thus decreasing the efficiency of the inverter resulting in large THD at the load voltage.

The simulations for the 1kHz switching frequency case for 40mF and 80mF DC-link capacitor value (Table 6.9) also does not have a significant variation in performance characteristics.

Table 6.8 The effect of DC-link capacitor value

Frequency	1.5kHz	1.5kHz	1.5kHz	1.5kHz
Filter Capacitance	35 µF	35 µF	35 µF	35 µF
DC-Link Cap.	10 mF	20 mF	40 mF	80 mF
Tr. Leak. Ind.	0.04 pu	0.04pu	0.04pu	0.04pu
THD	6.23%	3.78%	3.83%	3.74%
Filter Cap. Curr.	253A	227A	226A	226A
Filter Curr. (fund)	85A	83A	82A	82A
DC-Link Cap. Cur.	4.66kA	4.41kA	4.38kA	4.28kA
Source Current (rms)	522A	497A	483A	477A

Table 6.9 The effect of DC-link capacitor value at 1 kHz switching frequency

Frequency	1kHz	1kHz
Filter Capacitance	75 µF	75 µF
DC-Link Cap.	80 mF	40 mF
Tr. Leak. Ind.	0.04	0.04
THD	4.49%	4.56%
Filter Cap. Curr.	380A	380A
Filter Curr. (fund)	179A	180A
DC-Link Cap. Cur.	5.63kA	5.65kA
Source Current (rms)	510A	518A

The steady-state voltage magnitude of the DC-link is determined by the shunt connected transformer turns-ratio which is calculated and set by the design parameters. As stated before, during the voltage injection period, the voltage magnitude of the DC-link capacitor will decrease due to the voltage drop on the shunt transformer and the power diodes of the uncontrolled rectifier because of the high current which feeds the DC-link. In order to analyze this event, the depth of the sag is changed and the DC-link voltage has been observed. From

Table 6.10, it is clear that the DC-link voltage stabilizes at a relatively high magnitude during a voltage sag which is determined by the sag depth. One of the

advantage of the applied topology is this relatively high stabilized DC-link voltage magnitude which enhances the performance of the DVR

Table 6.10 The effect of sag depth on the DC-link voltage magnitude

Switching Frequency	3kHz	3kHz	3kHz	3kHz
DC-Link Cap.	80 mF	80 mF	80 mF	80 mF
Sag Depth	40%	30%	23%	18%
DC-Link Magnitude (high)	1.80kV	1.95kV	2.01kV	2.05kV
DC-Link Magnitude (low)	1.95kV	2.03kV	2.07kV	2.11kV

For the applied topology, the critical point in choosing the DC-link capacitor is not the capacitor value but the large rms current drawn in current pulses from the capacitor. The capacitor should be able to handle this large current. Therefore paralleling of lower valued capacitors with large current capability will be required for a DVR of this size.

6.1.4 Harmonic Voltage Drop on DVR

In order to analyze the harmonic voltages generated by the DVR, for the 3 kHz switching case, the tuning frequency of the DVR filter has been moved by changing the leakage impedance of the injection transformer. The filter capacitor has been chosen to be 6 μF and the leakage inductance of the injection transformer has been set to 0.04 p.u. and 0.08 p.u.

For the 0.04 p.u. leakage inductance case, the corner frequency of the DVR is found to be 1.3 kHz and for the 0.08 p.u. case 918 Hz with the equation given in (4.29).

These frequencies are around the 26^{th} and the 18^{th} harmonics respectively. Due to the applied topology, the shunt converter draws harmonic currents with harmonics at 6m±1 times of the fundamental component. Therefore we should see these harmonic voltages at the harmonic spectrum of the mitigated load voltages. Figure 6.1 is the harmonic magnitude spectrum of the load voltages normalized with respect to the fundamental component. The plot denoted by (x) is the first case with 0.04 p.u. and (○) is the 0.08 p.u. case. As expected, from the figure the harmonics

around the switching frequency better attenuated with the 0.08 p.u. value and the harmonics generated by the resonance frequency of the DVR is around the 26th harmonic. The harmonics of the 0.04 p.u. case is more clear around the 18th harmonic. Note that the 5th, 7th, 11th, 13th, ... harmonic voltages due to the uncontrolled rectifier current are clearly visible in both cases.

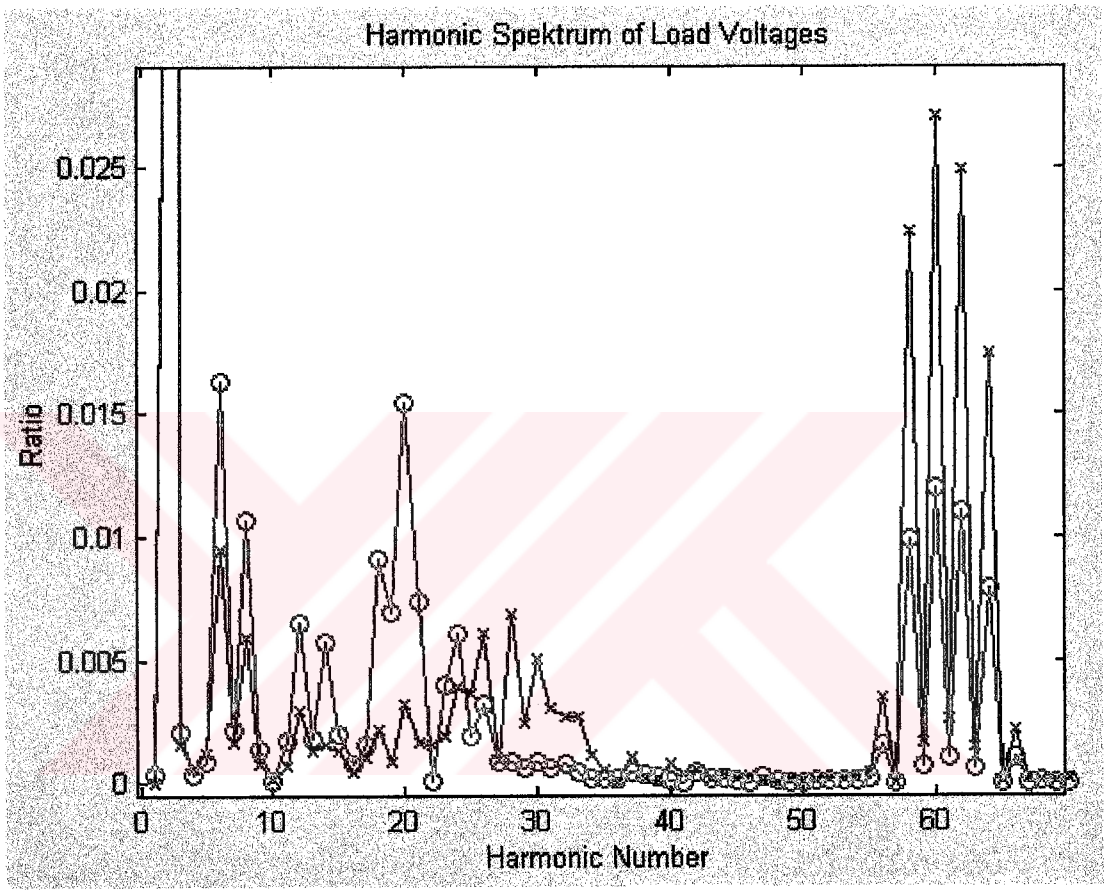

Figure 6.1 Harmonic Spectrum of Load Voltages with different tuned filters

6.2 DVR SIMULATIONS

From the results obtained, a DVR has been proposed and the necessary waveforms have been drawn. The power circuit is the one given in Chapter 5.2.1 while the DVR parameters are given in Table 5.1 in the "Proposed DVR" column.

In Figure 6.3, the source, injected and load voltages for the worst case of 40% voltage sag is illustrated. The load side voltage THD requirement is held below the level determined by the standards which guarantees the lesser magnitude mitigations

to be below the limits. The transient operation of the device is shown in Figure 6.5 which determines the dynamic response of the DVR. From the figure it is clear that the device starts to operate very quickly.

Figure 6.4 illustrates an unbalanced voltage sag (Figure 6.2) and the mitigation of the unbalanced voltages. The voltage sag of 40% occurred at phase A but due to the principles discussed in Chapter 2.1.2, the delta winding of the transformer caused a less severe voltage sag for phases A and C (28% voltage sag) with a phase shift of 8^0. The detailed view of the unbalanced voltage sag is given for phase A at Figure 6.6. From the figure, it is clear that a phase shift has occurred on the source voltage and the controller of the DVR restored the voltage sag to the pre-sag voltage which is denoted as the "Va-Reference" on the figure. The method for extracting the DC components of the positive and negative sequence SRF is not optimal and fastest which results in the very slow response of the DVR for the unbalanced voltage sags.

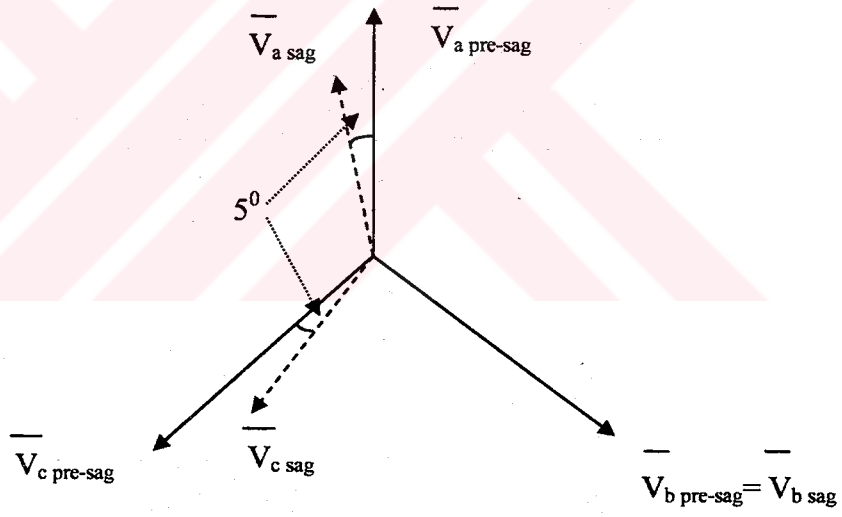

Figure 6.2 Unbalance voltage sag simulated

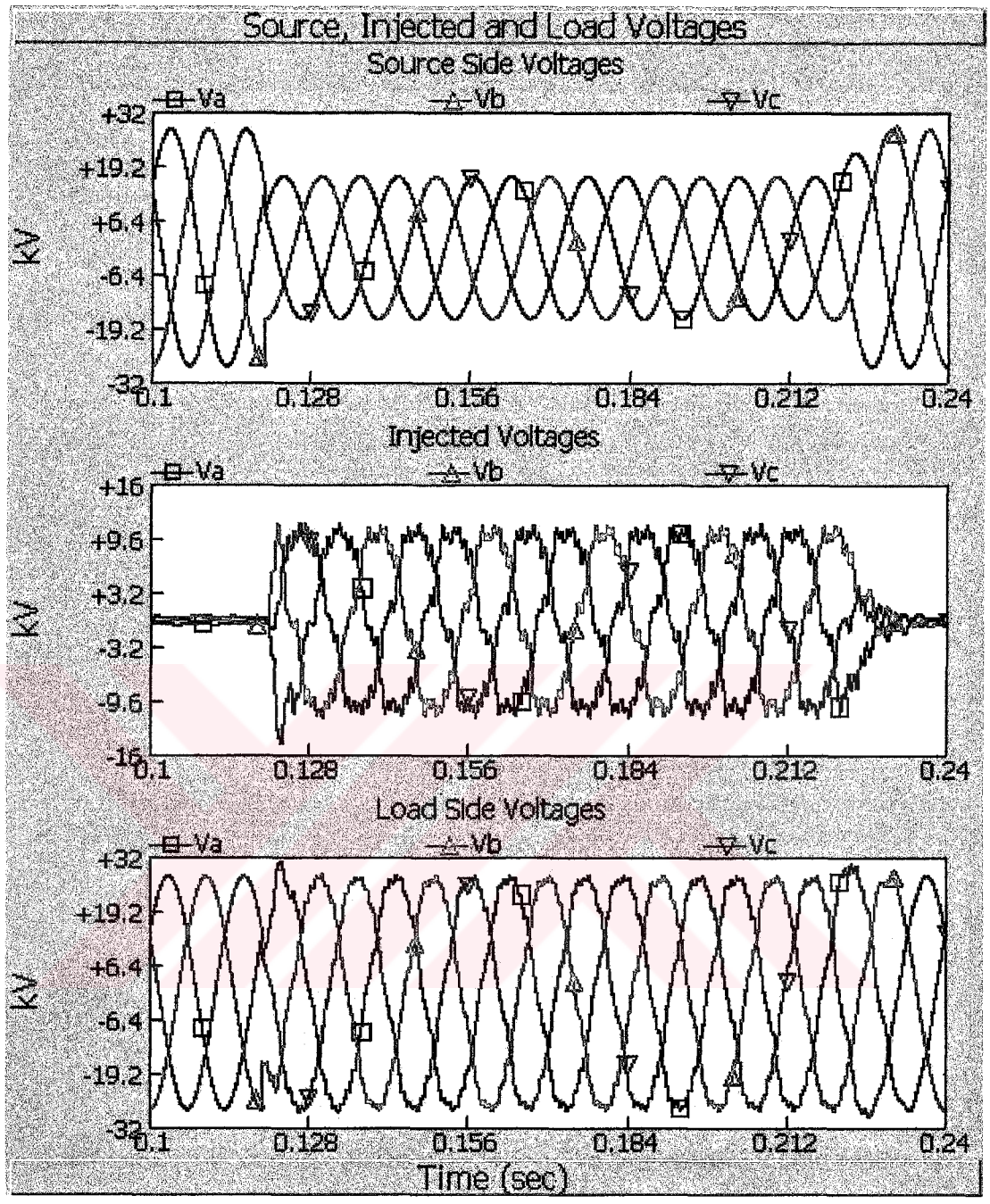

Figure 6.3 The Source, Injected and Restored Voltages (40% sag depth)

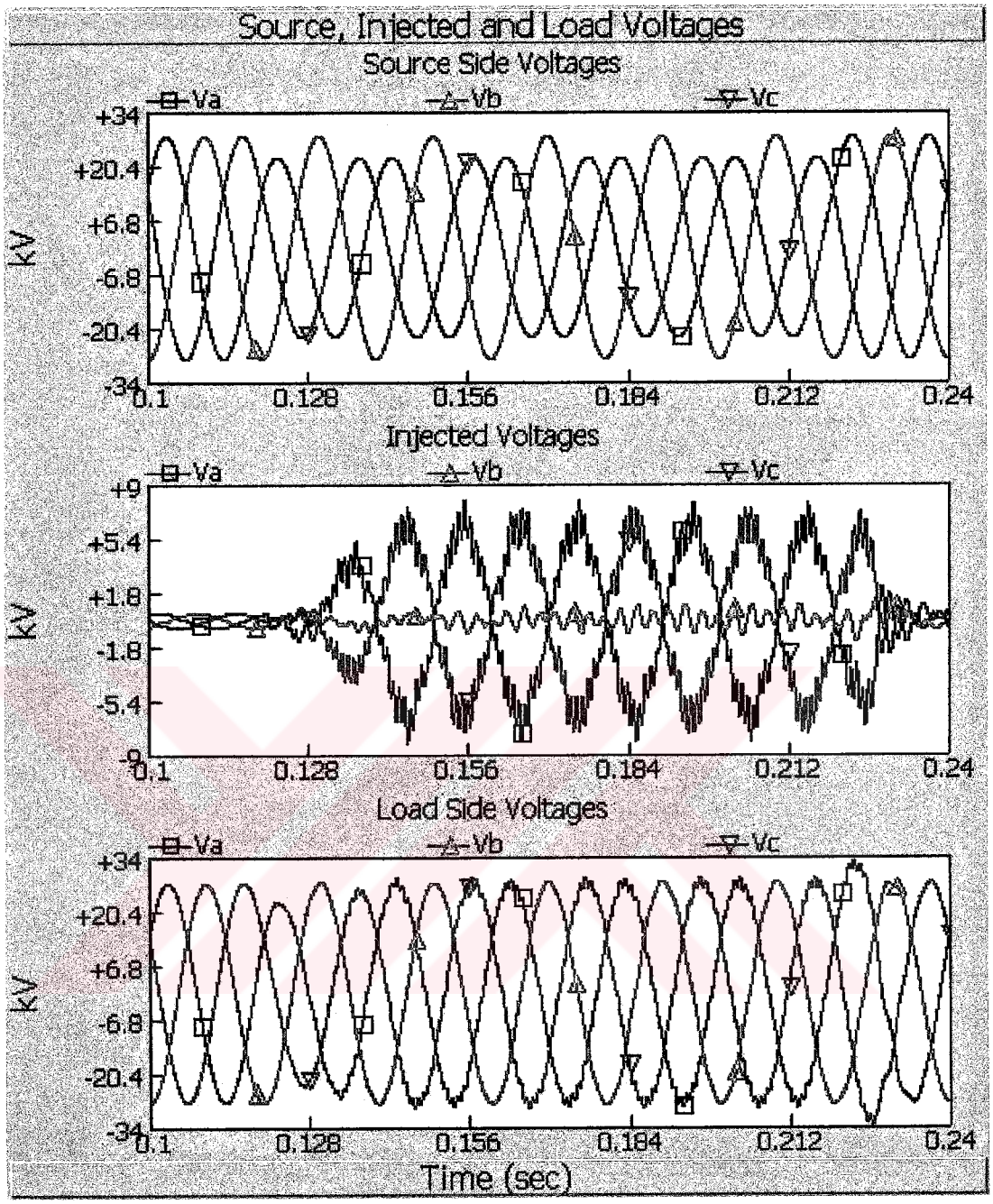

Figure 6.4 The Source, Injected and Restored Voltages for unbalanced voltage sag

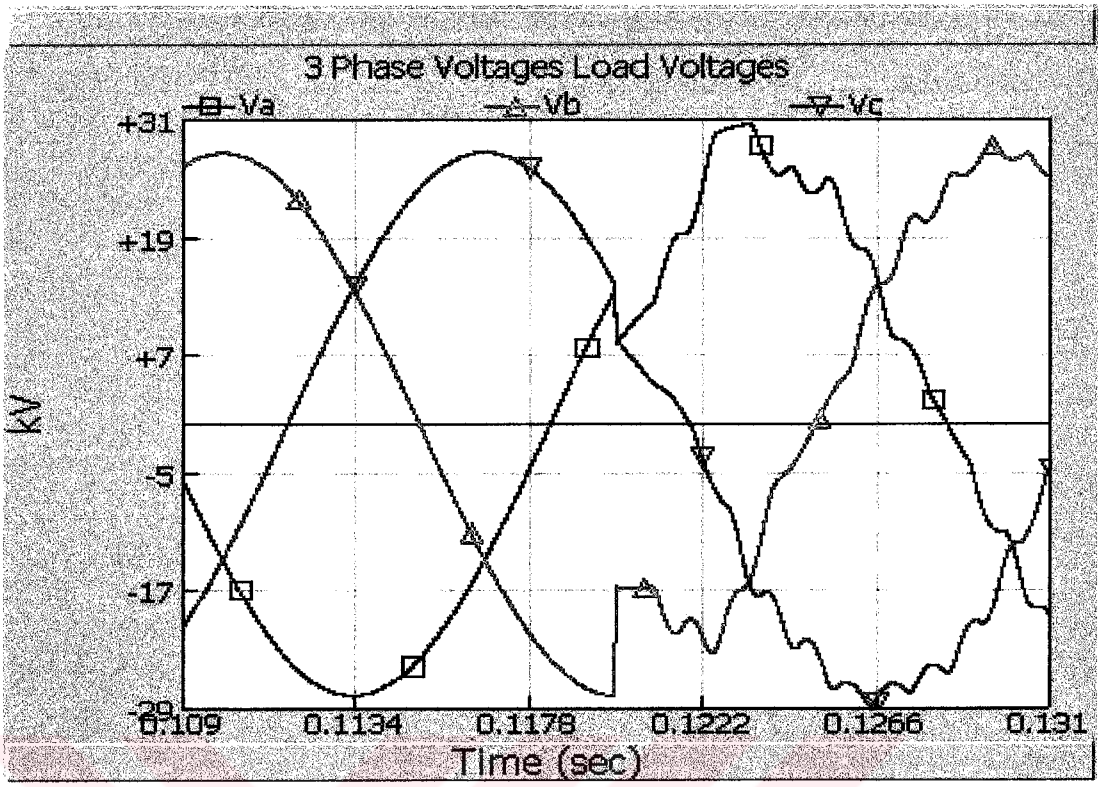

Figure 6.5 The dynamic response of the DVR

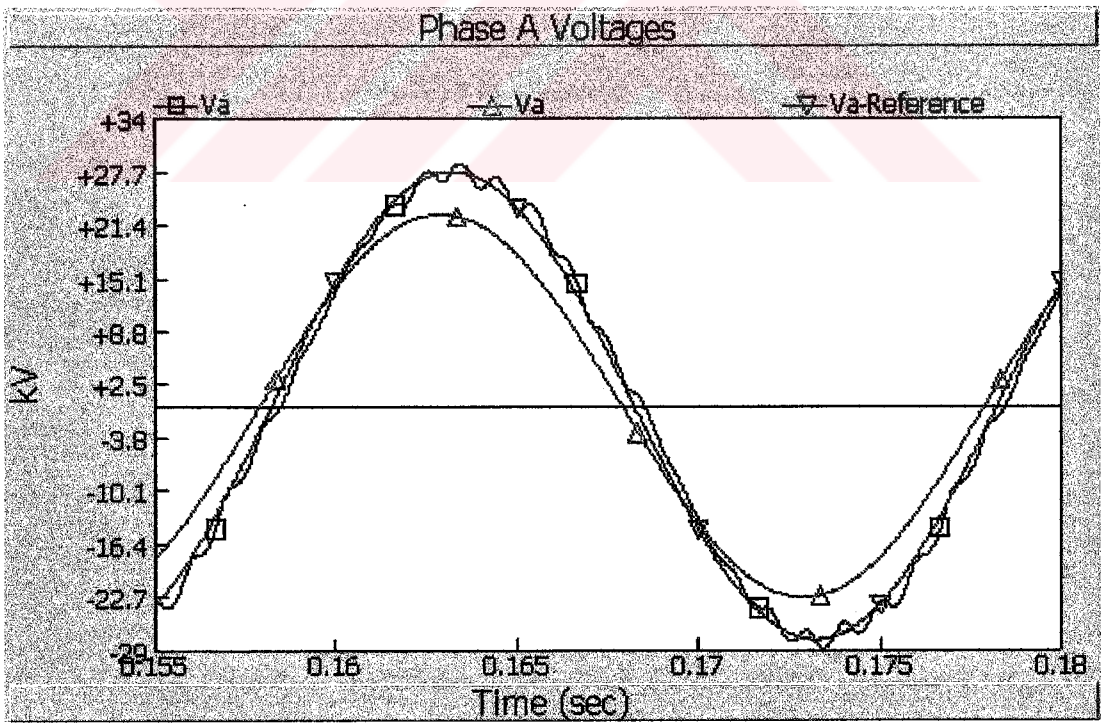

Figure 6.6 The Source, Injected and Restored Voltages of Phase A with phase-shift

The following simulations are carried on 30%, 3-phase balanced fault. For the waveforms to be clearly seen, the duration of the voltage sag limited to 100ms which happens between 120ms and 220ms. In the topology applied, the duration of the voltage sag does not limit the DVR performance except the thermal limits on the components.

In Figure 6.7, the source side, the injected and the restored load side voltages are shown. As soon as the voltage sag is detected, the DVR starts to inject voltages in order to mitigate the voltage sag on the source side. The distortions at the beginning of the mitigation process are due to the relatively lower switching frequency of the inverter. Figure 6.8 illustrates the source side voltage, the restored load side and the reference voltage of the phase A in detail. There exist ripples on the restored load side voltage but the THD of the load voltage is limited to 5% at the worst case by the design parameters. The THD calculations are shown in Figure 6.9 for each phase. From the figure, the THD of the load voltages are below the limits determined by the standards. The long and high THD levels during the transients are the result of the one cycle moving windowing operation of the THD calculator.

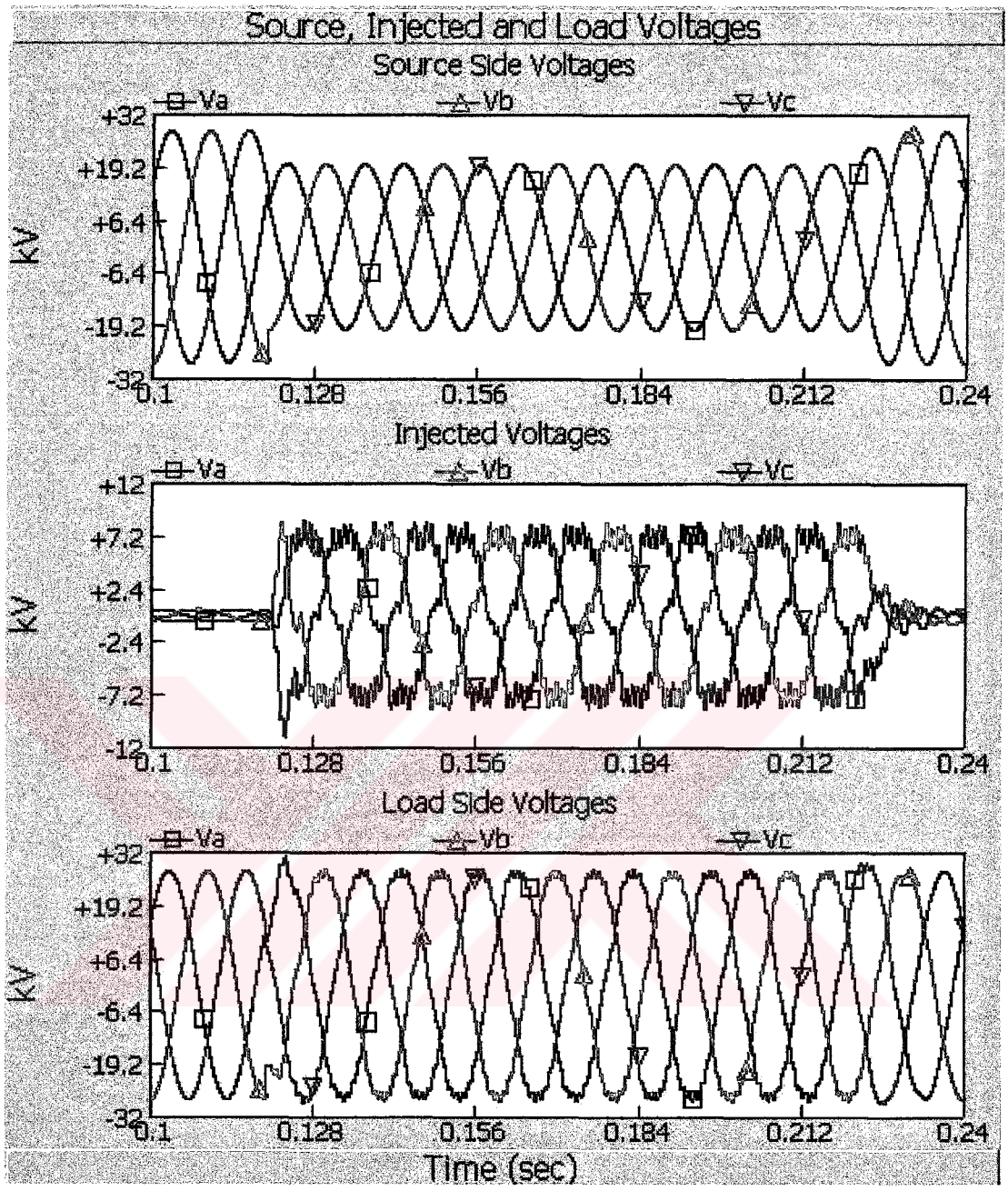

Figure 6.7 The Source, Injected and Restored Voltages (30% sag depth)

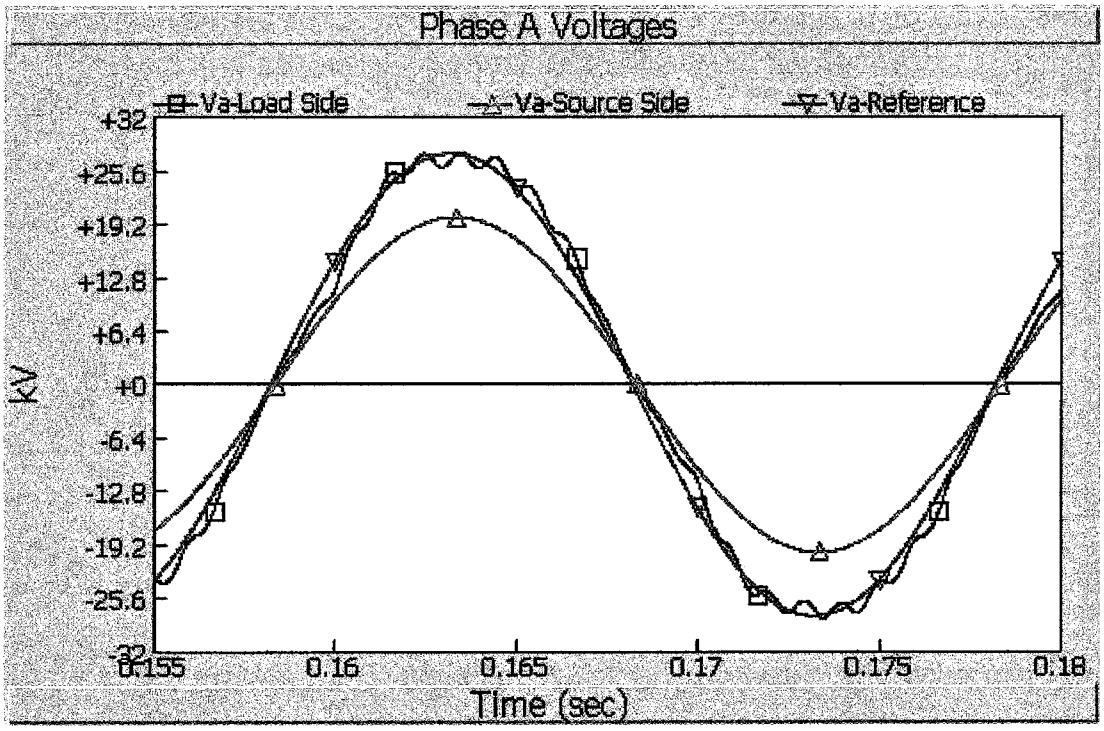

Figure 6.8 The Source, Injected and Restored Voltages of Phase A

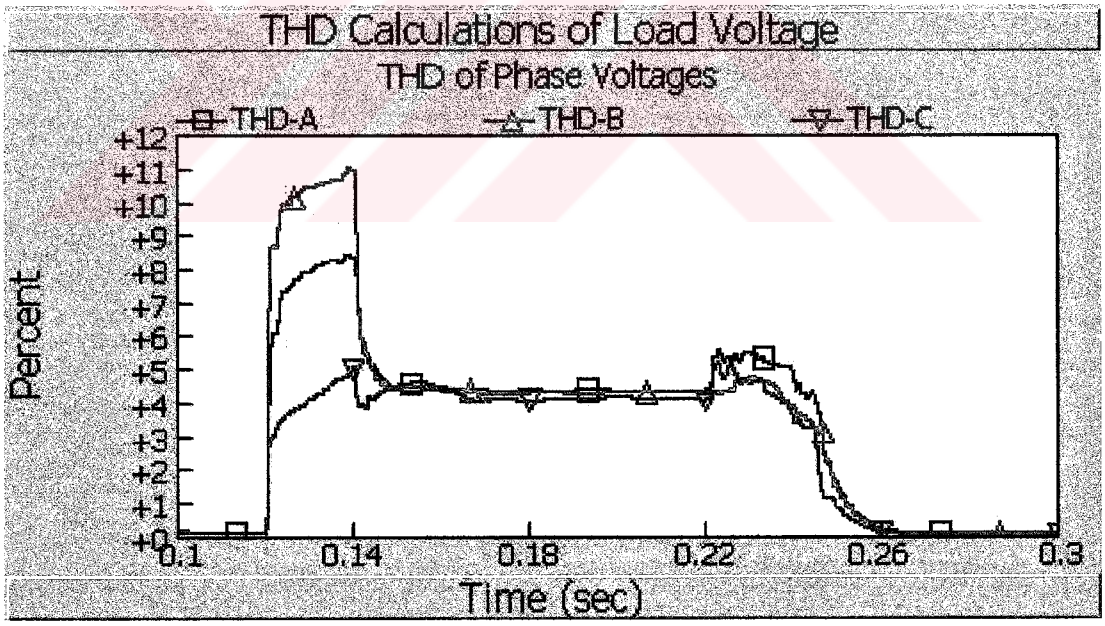

Figure 6.9 The THD of Load Voltages

The transformations of the source side voltages for the controller of the DVR are given in Figure 6.10. Since the fault is balanced and three phase, the dq components of the positive sequence SRF is ripple free. Additionally, the negative sequence components contain no DC values to be extracted. In Figure 6.11, the reference voltages for the PWM inverter generated by the controller are displayed.

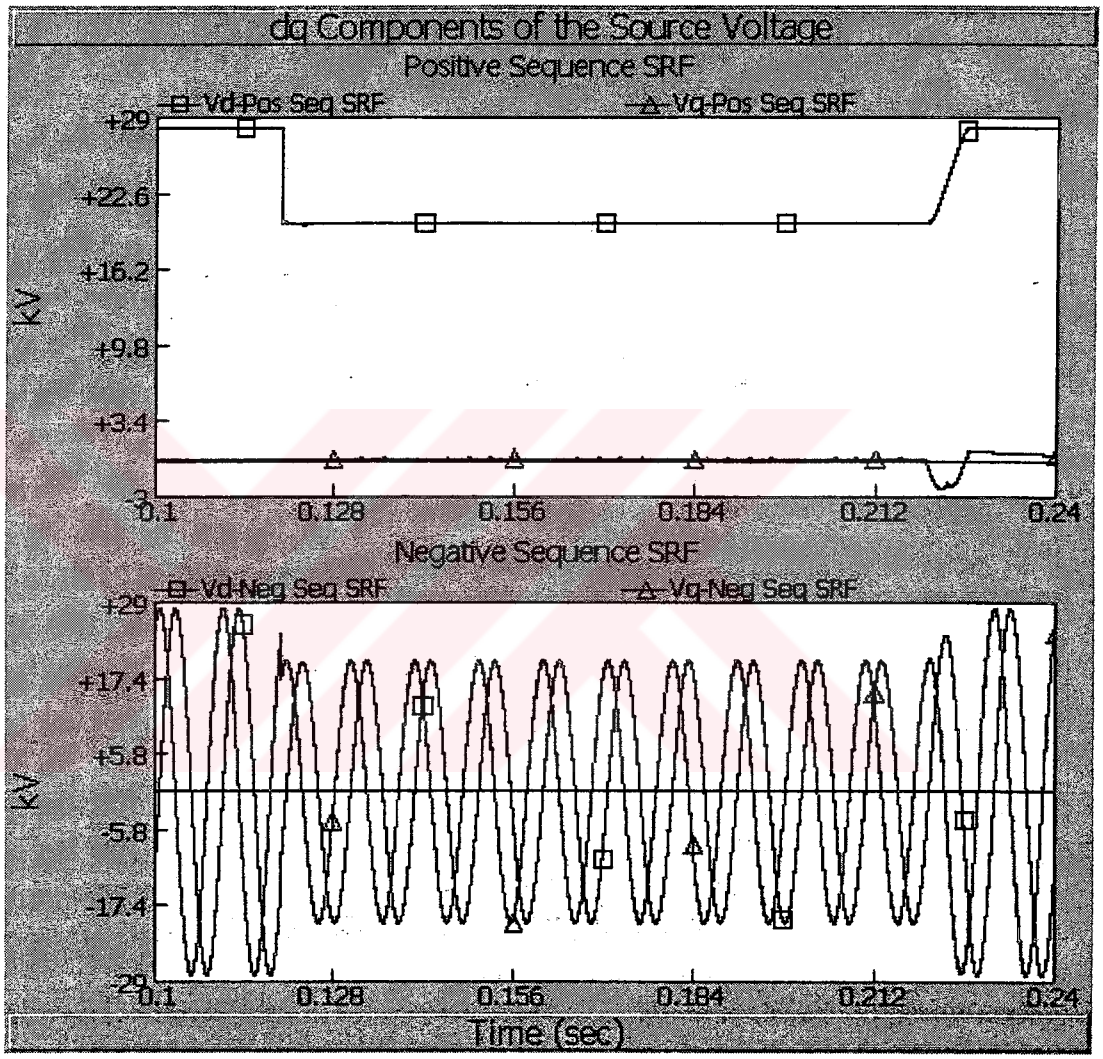

Figure 6.10 The transformed dq voltages of the source side

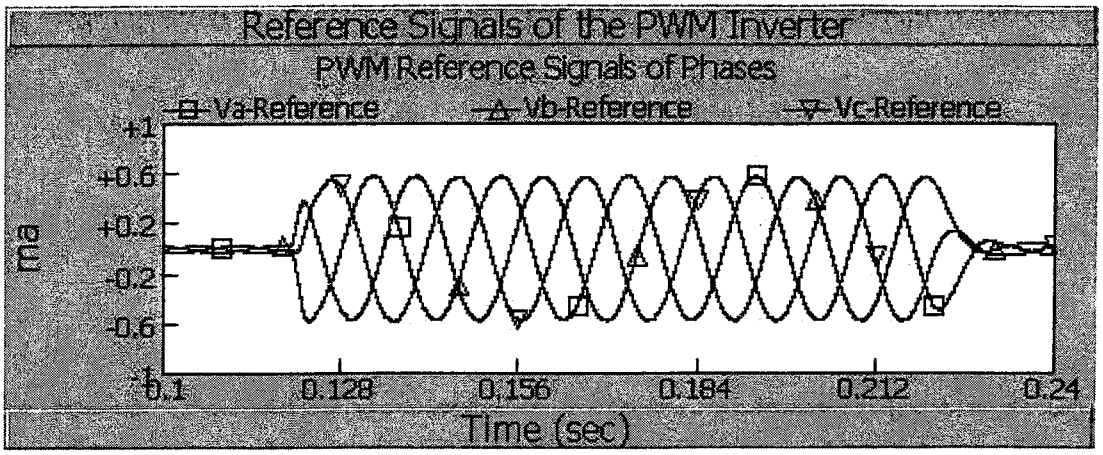

Figure 6.11 The reference signals calculated for the PWM Inverter

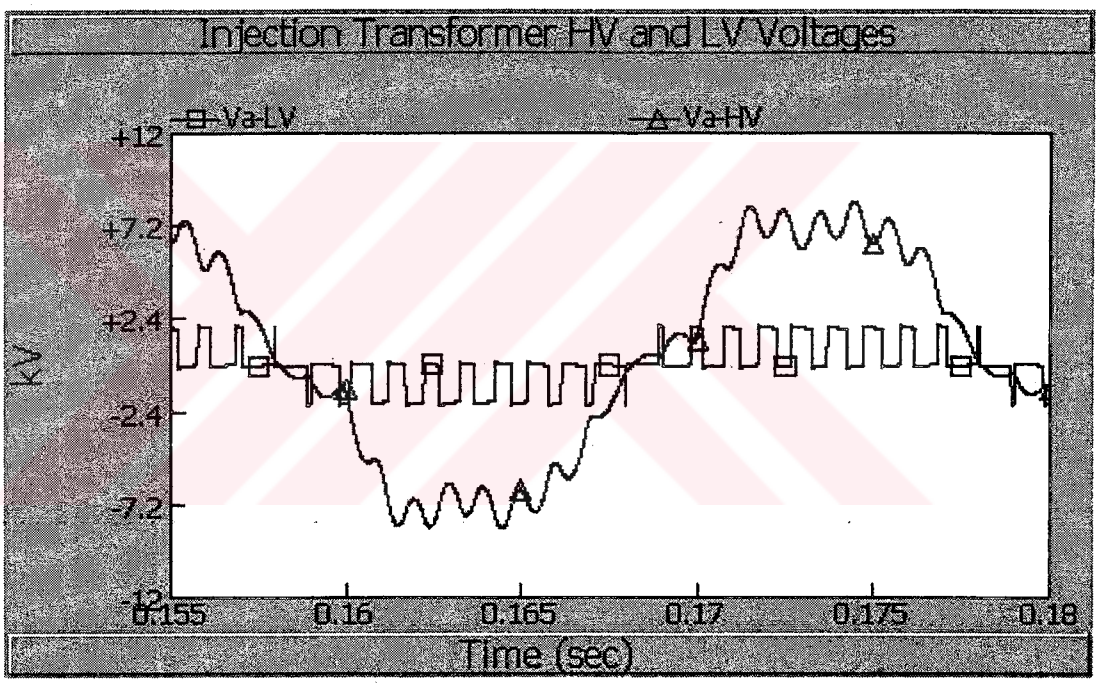

Figure 6.12 The low voltage and high voltage side of the injection transformer

Figure 6.12 illustrates the low voltage and high voltage side of the injection transformer. In the applied line side filtering scheme, the low voltage side of the injection transformer is in voltage pulses generated from the PWM inverter. This will surely increase the stress on the injection transformer. The series leakage inductance of the injection transformer and the shunt filter capacitor attenuates the harmonics of the PWM inverter and the voltage of high voltage side is added to the source side

voltage, resulting in restored load voltage. Note that the harmonics of the injected voltage is rather high, but with the addition of the source side voltage, the emphasis of the harmonics on the load side voltage decreases, allowing us to obtain a load voltage below 5% THD. The ripples on the pulses are due to the ripples on the DC-link.

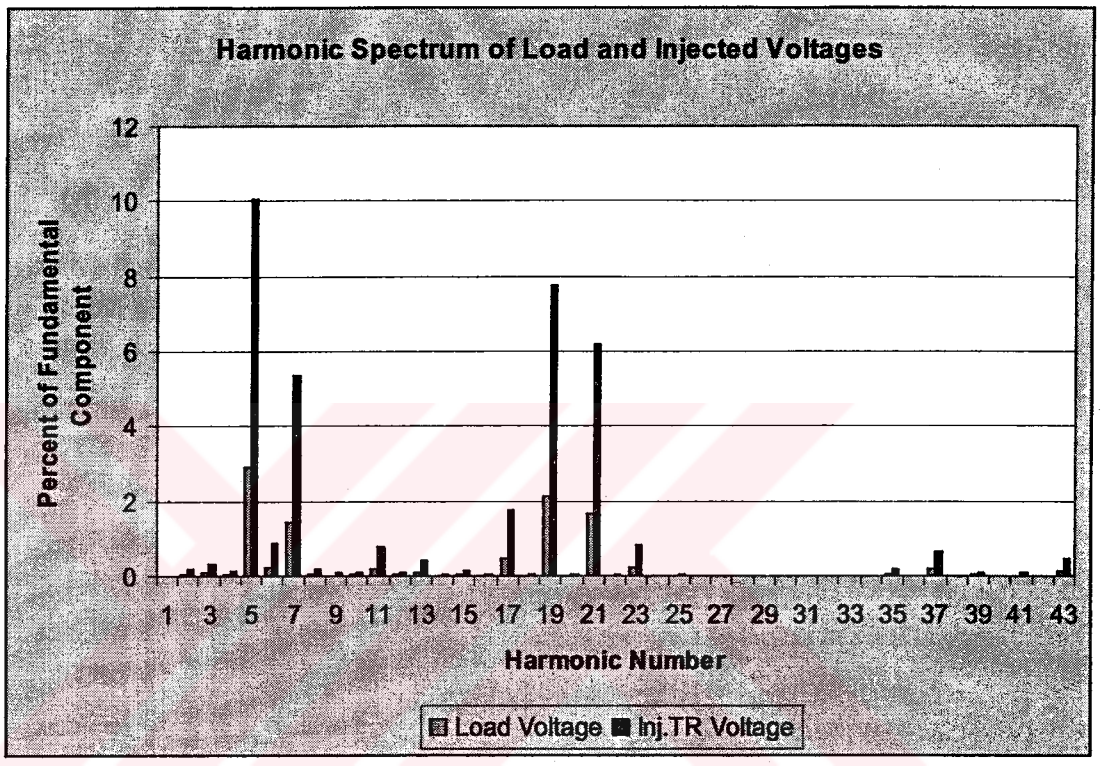

Figure 6.13 The harmonic spectrum of the injected and load voltages

The harmonic spectrum of the injected and the load voltages consists of the harmonics at the switching frequency and the multiples of the switching frequency plus the harmonic voltages due to the harmonic of the current passing through the injection transformer. As stated before, there exist harmonic voltage drops on the DVR due to the filtering scheme. In the Figure 6.13, the harmonic spectrum of the load voltage and the injected voltage with respect to their fundamental component is given. The injected voltage waveform is the larger one and the load voltage is the relatively smaller one. Since the load voltage is the addition of injected and source side voltages, the harmonic content of the load voltage decreases.

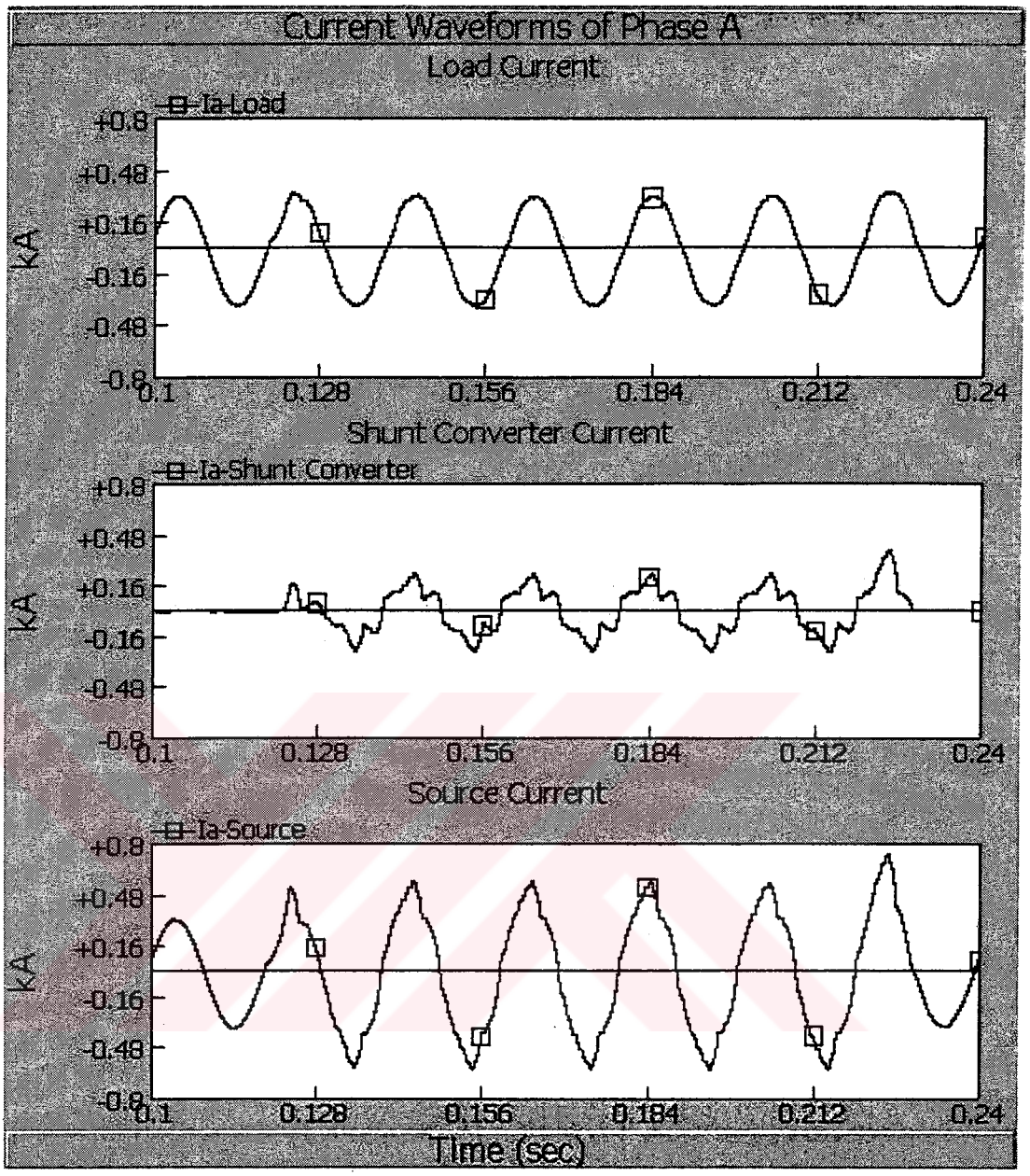

Figure 6.14 The Load, Source and Shunt Converter Currents

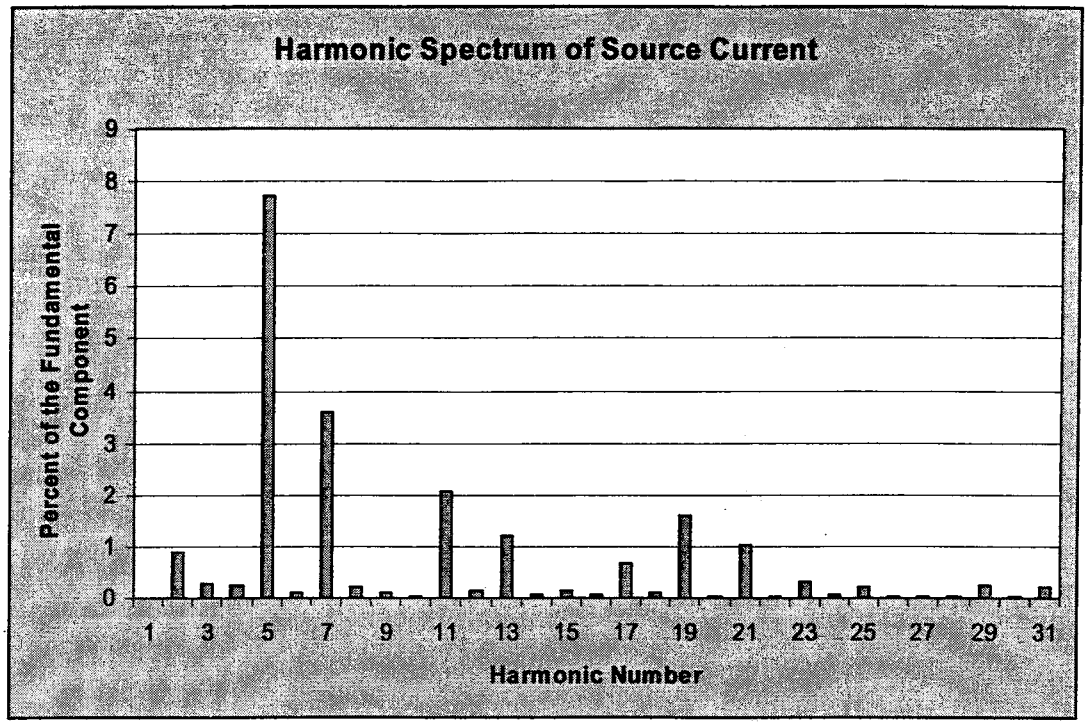

Figure 6.15 The harmonic spectrum of source current

Figure 6.14 illustrates the load, source and the shunt converter currents. The load current is harmonic free but the shunt diode rectifier draws harmonic current from the source causing harmonic currents flowing through the DVR. Note that since no energy is stored on the DC-link, the DC-link fed from the load side connected diode rectifier. For a 30% balanced voltage sag, according to (4.8) a current approximately 43% of the load current passes through the shunt converter which will significantly increase the current though the DVR. The reason for the over-rated value of the components is this high current passing though the DVR. But as stated before, one of the advantages of the over-rated components is the enhanced resistance of the DVR in case of a downstream fault at the load it protects.

In Figure 6.15 the harmonic content of the source current is given in percents. Note that the because of the diode rectifier, the harmonic content of the current are at the 6m±1 multiples of the fundamental frequency. According to (6.1), the resonance frequency of the DVR is calculated to be 367Hz which is around the 7^{th} harmonic. From Figure 6.13, the harmonics around this frequency are clearly visible. Since the load voltage THD can be kept below the limits, these harmonic contents may be

ignored. In cases where these harmonics severely affects the DVR performance, special attention to attenuate these harmonics should be taken.

Another disadvantage of the topology applied is the harmonic current drawn the source as shown from Figure 6.15. This highly distorted current may pass the limits allowed for the current waveform distortion for deep voltage sags which will surely require filters to damp these current harmonics.

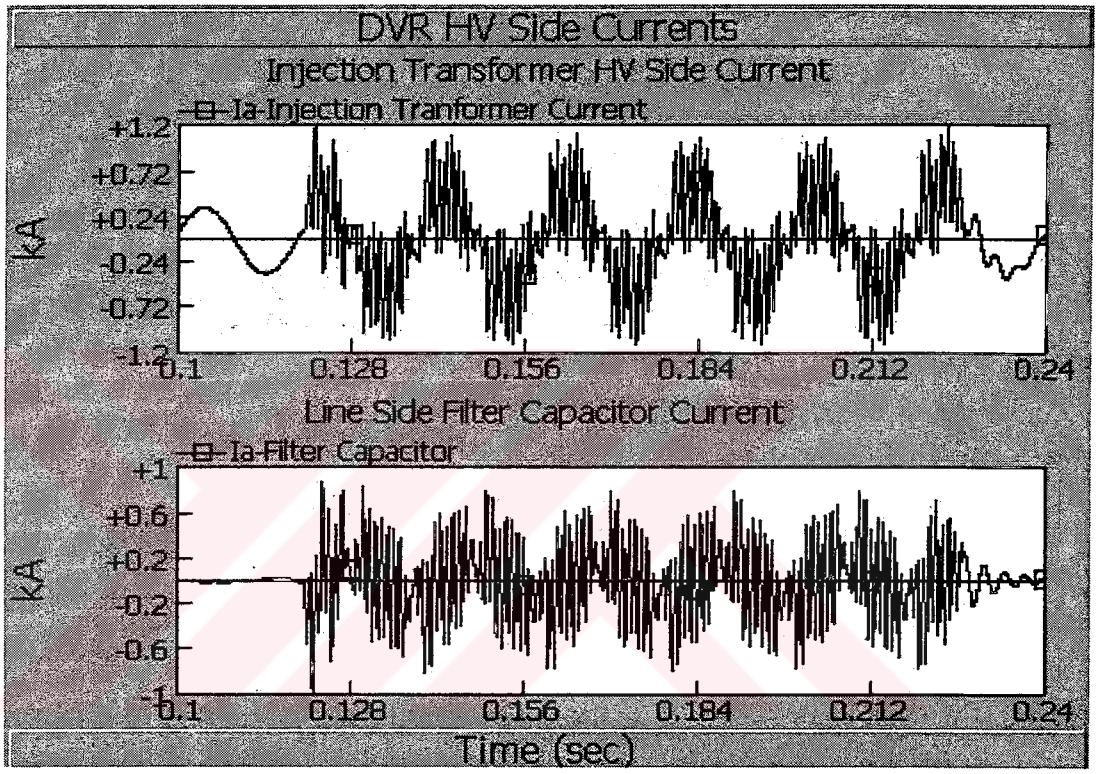

Figure 6.16 The Filter and Injection Transformer Primary Current

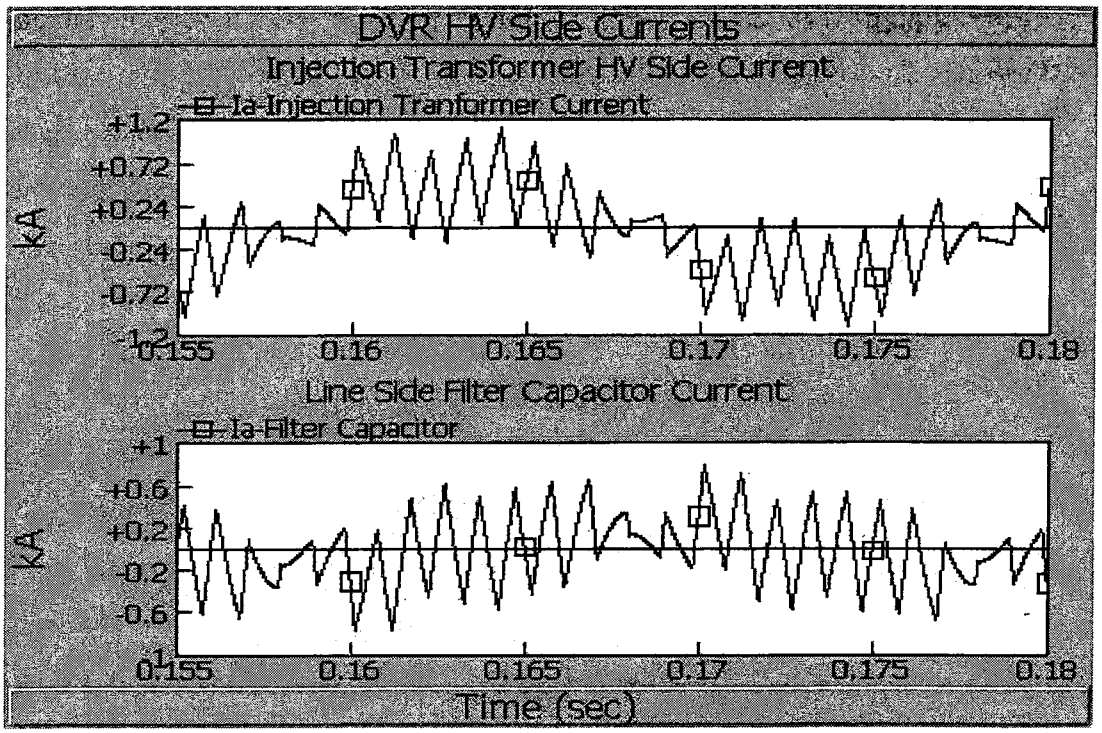

Figure 6.17 Detailed view of Figure 6.16

During the steady-state, the load current passes through the DVR and the injection transformer as shown in Figure 6.16 and the current on the filter capacitor is negligible. But as soon as the DVR starts to inject voltages to the line, the harmonic currents start to flow inside the DVR. But these harmonic currents circulate through the DVR not disturbing the source and load currents (Figure 6.14). The fundamental component of the filter capacitor current is determined by the injected voltage magnitude while the total rms current is determined by the switching frequency and the leakage inductance of the injection transformer helping the filtering of the harmonics. In Figure 6.18, the harmonic spectrum of the filter capacitor current is given. The voltage of the filter capacitor is the injected voltage. For a filter capacitor with these ratings, the MKK type capacitors for the DC-links may be applied considering the high current and voltage rating of the capacitors. For the high voltage rating of the capacitors, a series connection may be applied.

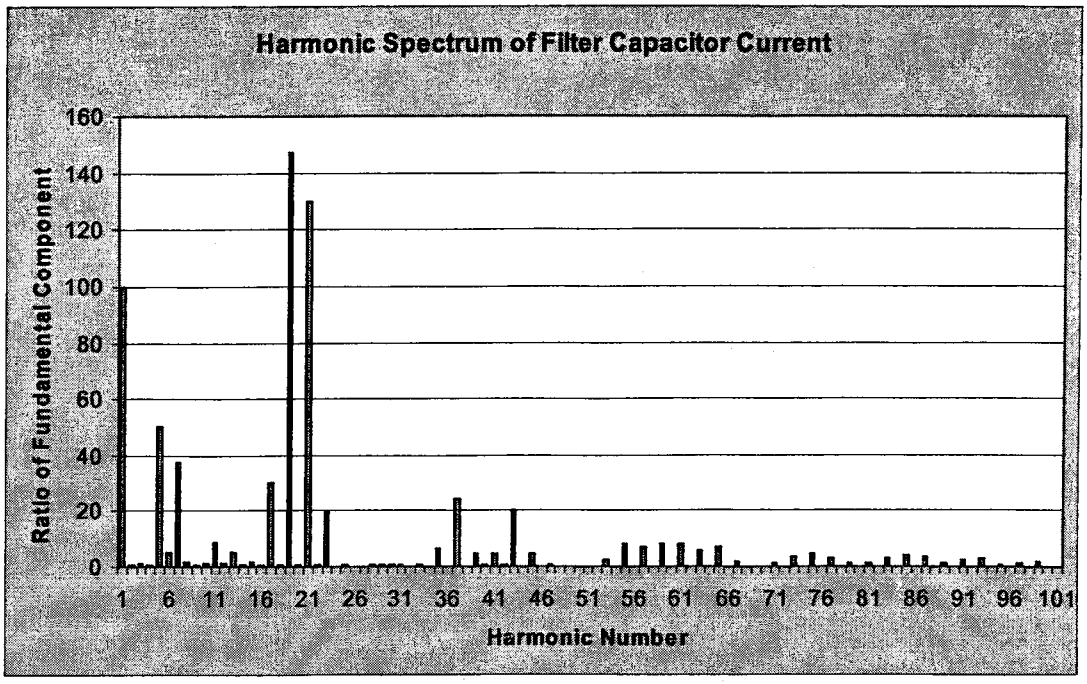

Figure 6.18 Harmonic spectrum of filter capacitor current

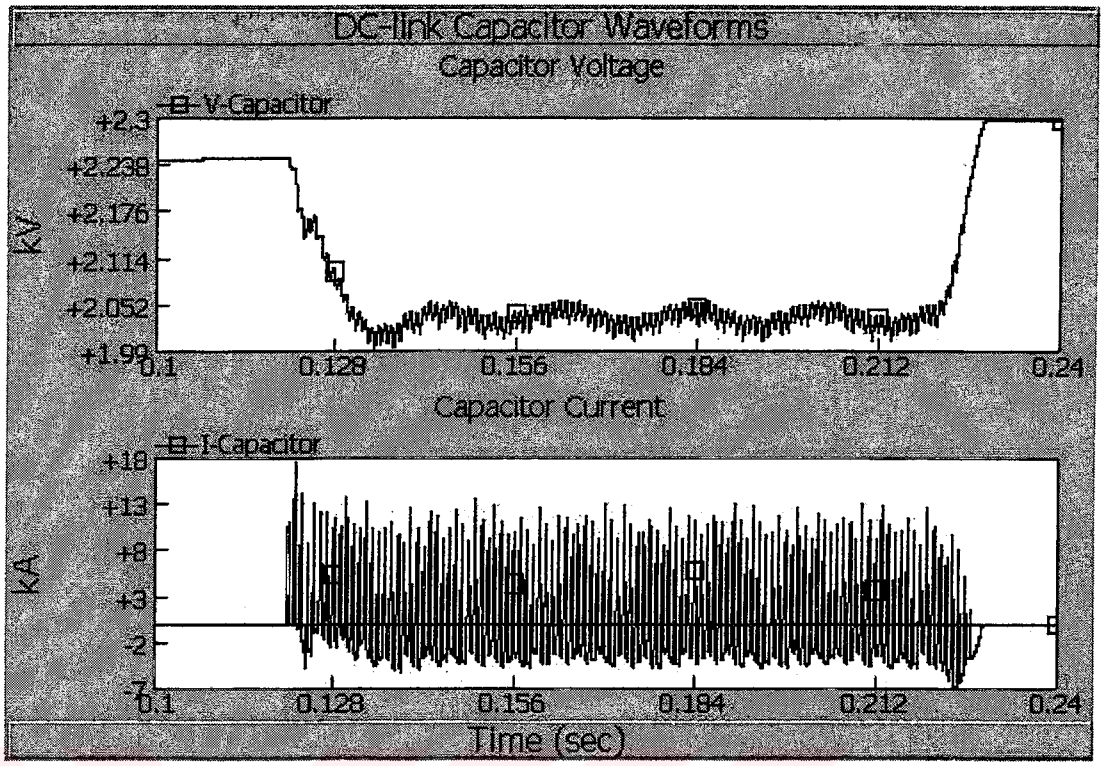

Figure 6.19 The DC-link capacitor waveforms

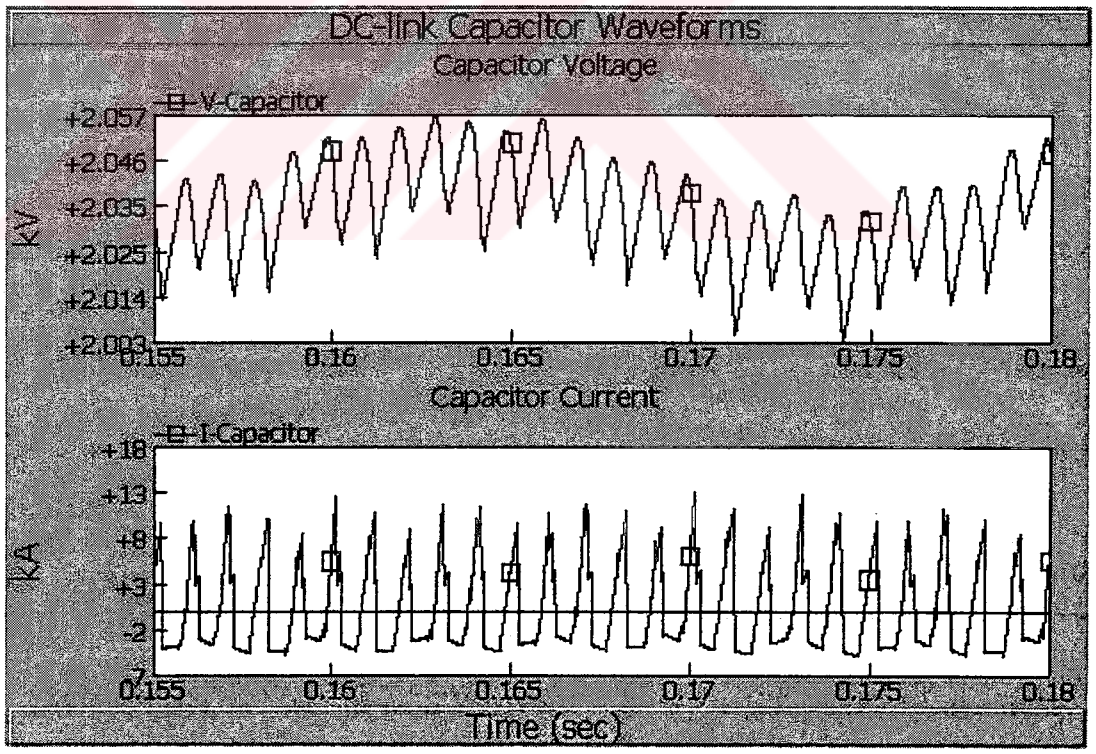

Figure 6.20 Detailed view of Figure 6.19

The DC-link which feeds the DVR during the voltage mitigation process is fed from the line side connected shunt uncontrolled rectifier. Since the load that the DVR connected is very large, in order to supply necessary power to the load, the DC-link current is very large. From the simulations in the former chapter, it has been shown that beyond the capacitor value, the current capability of the DC-link capacitor is more important in this topology. The DC-link should compose of capacitors paralleled each other in order to ensure to supply these large currents.

From Figure 6.19, the voltage magnitude of the DC-link decreases with respect to the steady-state value although the rectifier is fed from the corrected load side voltage. The reason for this is that the large currents passing through the shunt transformer and rectifier semiconductors causes a voltage drop on the components and therefore decreasing the voltage level of the DC-link during a voltage sag. As stated before the level of the DC-link voltage during the mitigation process is determined by the sag depth.

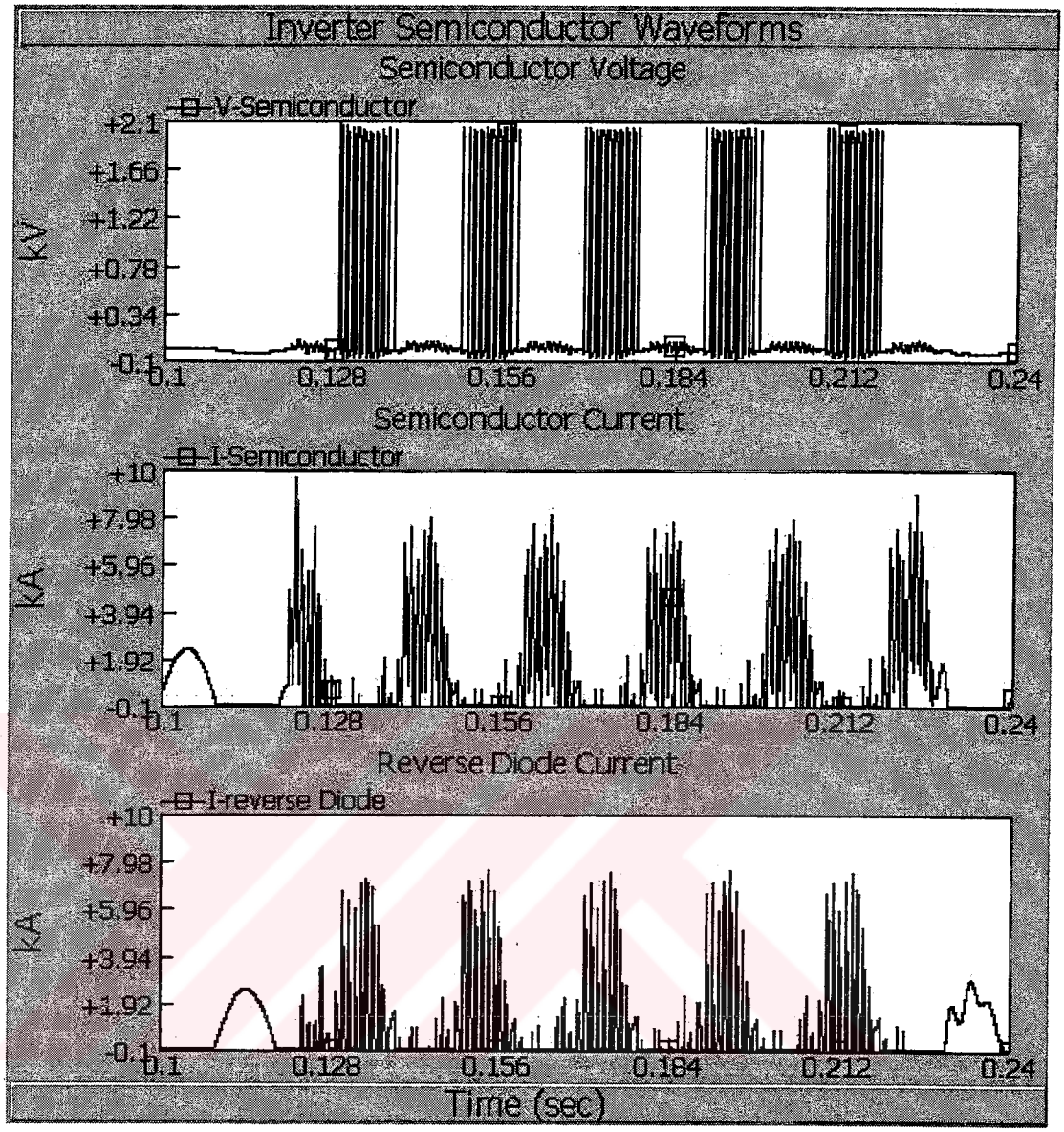

Figure 6.21 Semiconductor waveforms

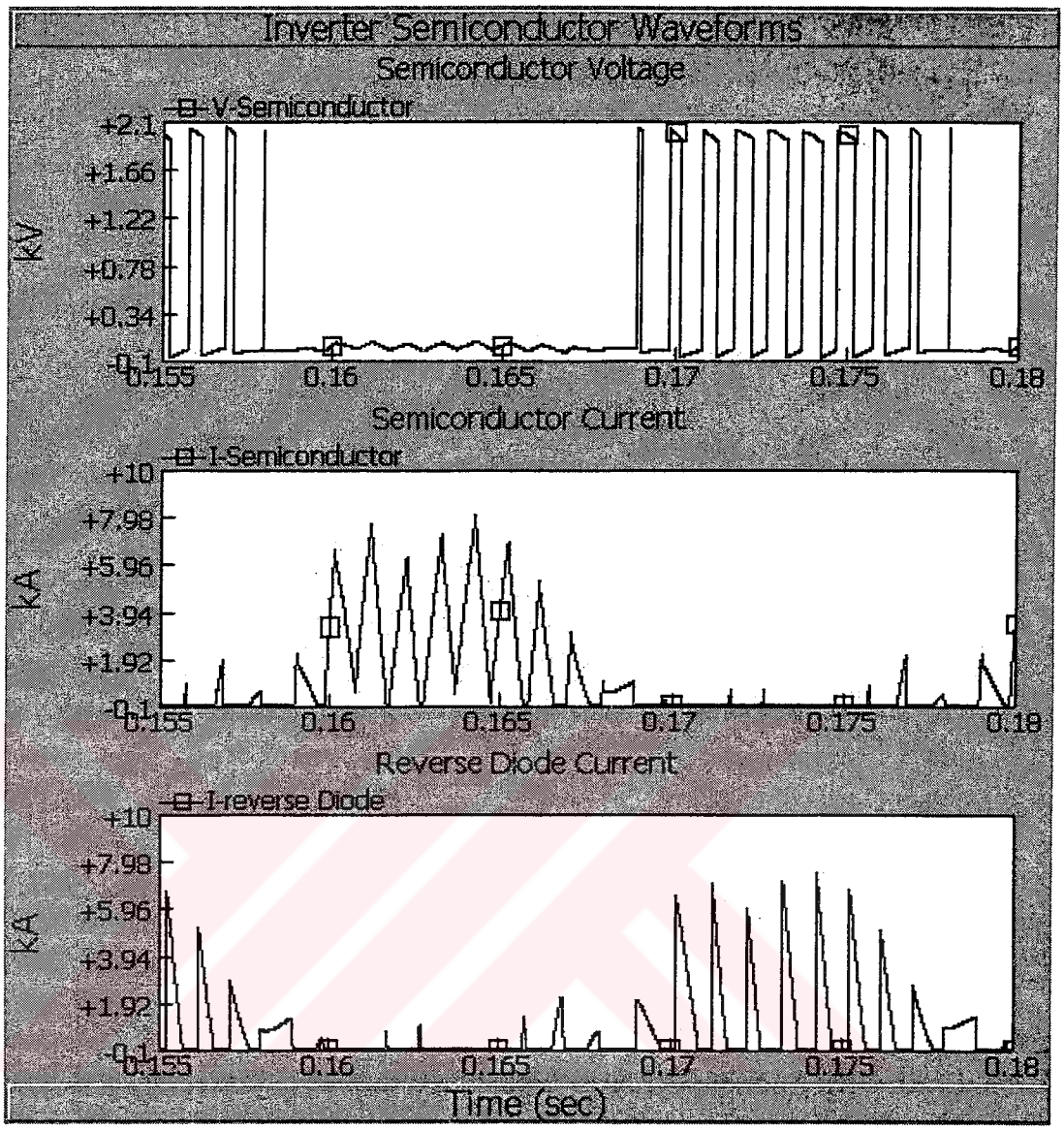

Figure 6.22 Detailed view of Figure 6.21

The critical point in large scaled DVRs is the semiconductors of the inverter. In case of the SCO of DVR with the semiconductors, the full load current passes through the semiconductors during the steady-state operation (Figure 6.21). During the mitigation process, even larger current flows since the load is partially fed from the DC-link according to the sag depth.

Up to now, there does not exist single semiconductor that may stand such currents. Even the new IGCT technology semiconductors are not rated at this level. The solution for this problem is paralleling of the semiconductors by creating

modules of lower rated inverters. In the field applications of the DVR, modules of 2MVA are paralleled for the larger load requirements [21]. It has been reported that the tie reactors connected to the output of each inverter module serve as an impedance to establish the output current therefore the low voltage side of the injection transformer becomes the current summing junction for the inverters.

Another method for large MVA inverters is the series connection of IGCT semiconductors. The state-of-the-art IGCT technology offers large MVA inverters for the medium voltage applications. With the series connection of IGCTs, the DC-link can be set for a larger value which will decrease the current through the semiconductors down to an applicable level [26][27][28][29].

In order to decrease the high power requirement of the load, one method is not fully compensating the voltage but compensating up to a level which will not disturb the sensitive load. For example, if the load is sensitive to the voltage sags below 0.1 p.u., then the compensation may restore the load voltage up to 0.9 p.u. which will decrease power required for the DVR. Special measures to increase the sensitivity of the equipments to the voltage sags can be taken in order to decrease the output power of the DVR.

CHAPTER 7

CONCLUSIONS

In this study, a state-of-the-art power quality device used for mitigating the voltage sags on the distribution system has been introduced. The Dynamic Voltage Restorer is a series power quality device which injects voltage to the line in case of a voltage sag event. With this recently introduced device the plants that suffer from voltage sags will not be disturbed and continue to work when a voltage sag is present on the line.

The device has been evaluated from top to bottom and the critical design issues have been given during the study. Furthermore, a DVR for an 18 MVA load has been designed, simulated and successfully operated in PSCAD/EMTDC software. It has been shown that at 1 kHz switching frequency of the semiconductors, the device has restored the load side voltage to the pre-sag voltage level as soon as the voltage sag has happened. Even if at 60% source voltage level of the nominal value, the device held the load voltage THD below 5% ensuring a proper protection.

The topology with the load side connected shunt converter is chosen for the implementation as it has been reported to be one of the most efficient topologies which may be applied for the DVRs. With this topology, the duration of the voltage sag will not be important since the DVR will not store a large energy and the required energy during voltage sags will be maintained from the line. This important feature will breed the disadvantage of harmonic current generation from the shunt uncontrolled rectifier and the over-rated DVR components. The harmonic currents will cause a harmonic voltage drop on the injection transformer but the DC-link voltage control will be superior to the source side connected converter topology and

the over-rated components will guarantee the toughness of the DVR due to the inrush currents or downstream faults.

The switching frequency and the attenuation of harmonics at different switching frequencies have been simulated and the results show that even if at lower switching frequencies the device will be able to work properly but the disadvantage will be the larger rating of the line-side filtering capacitor. The effect of the DC-link capacitor has been investigated and since no-energy storing topology is applied, the DC-link capacitor will be respectively at lower value although the current injection capability should be high due to the high rating of the load. With the introduction of newer semiconductors with high switching frequency and the high voltage and current ratings, the performance of the device will increase.

The simulations show that it is very difficult to protect a load of 18MVA with a basic inverter topology. This large rating can only be achieved either by implementing small scaled inverter modules and paralleling them with each other or with the series connection of semiconductors. The new IGCT technology enables series connection of the semiconductors with ease and safety.

The simulations have been carried for a typical large load which resembles a large factory. If the device has been connected to the plant, the voltage sags would not interrupt the production process and the money loss because of interruptions would be saved. But from the simulations, it is clear that implementation of such a device will be very expensive and the companies would not prefer to purchase such an expensive device. Therefore the DVR is a Custom Power device which can be considered as a utility-provided solution in order to protect the sensitive loads. It has been reported that the customers may prefer to pay for the cost of the device at their power bill.

The future work on this topic should be the implementation of a small scaled model at the laboratory. Depending on the results obtained experimentally, a large scaled model may be considered to be implemented for the industry. For large rating loads, the multi-module DVR concept should be studied and designed for proper operation. It has been reported that there are factories located in South-east Anatolia Region that suffer from low quality power in Turkey. After determination of the losses of customers from the voltage sags and necessary feasibility analysis, the

custom power device, the DVR, may be designed for the specific problem. I hope that this study may constitute a basis for future studies on this topic. I believe that there are regions in Turkey that will require a DVR installed to their power system.

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APPENDIX A

PSCAD SIMULATIONS AND MATLAB FILES

A.1 PSCAD SIMULATION

The simulation of the power circuit and the DVR has been carried out on the circuit shown in Figure A.1. The values and parameters of the components are modified according to the simulation to be carried.

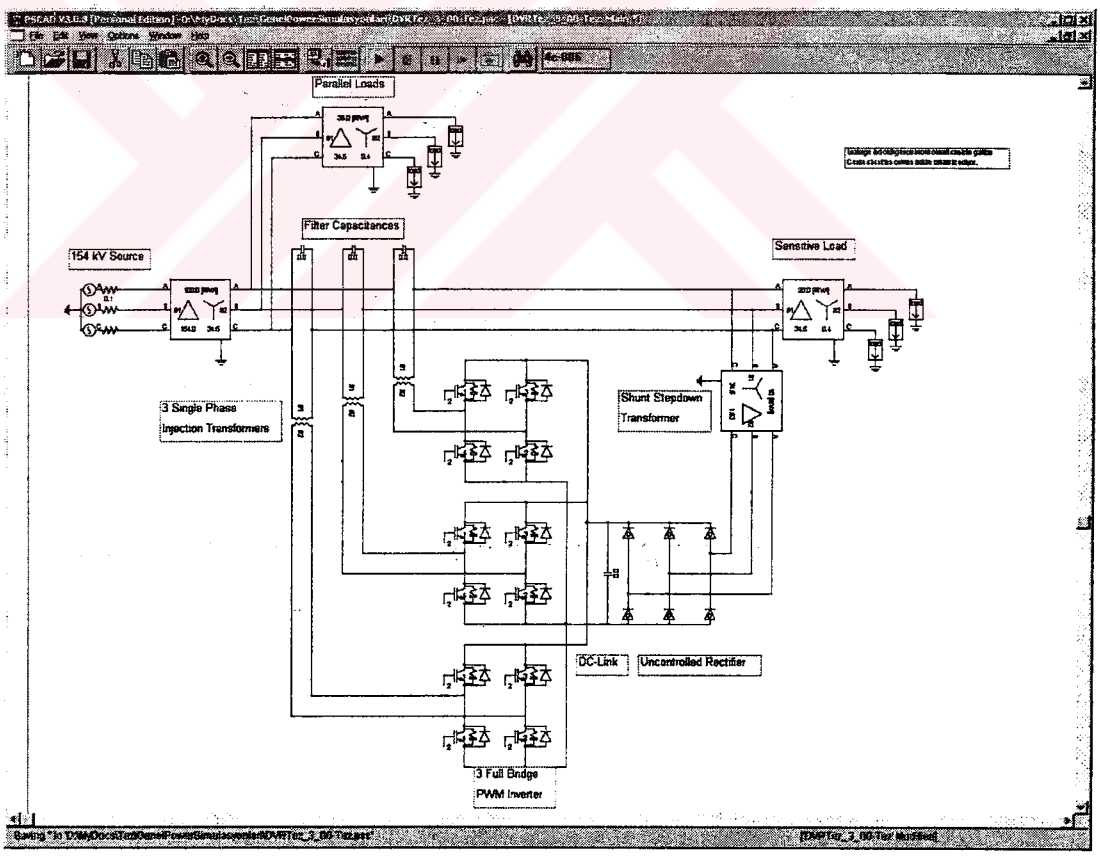

Figure A.1 PSCAD DVR simulation power circuit

The control of the DVR has been carried out with the diagram shown in Figure A.3. The phase angle information of the system voltages are extracted from the PLL object of the PSCAD/EMTDC. Note that the output of the PLL object is shifted by 90° (4.71 added and Modulo into 6.28 is taken). The output of the PSCAD/EMTDC PLL outputs the theta in radians/seconds and the Phase A zero crossing is calculated as 0 radians/seconds. But the control parameters are designed for 0 radians/seconds of PLL when the Phase A is in 90°.

The PWM reference signal are converted to the PWM gate signals of the inverter as shown in Figure A.3. The triangular carrier signal has been formed by the PSCAD "Variable frequency sawtooth generator" object. The frequency of the signal is entered to object and the required sawtooth signal is formed. The generated signal is compared with the reference signals in the "Interpolated Firing Pulses" object which constitutes the required gate signals of the semiconductors.

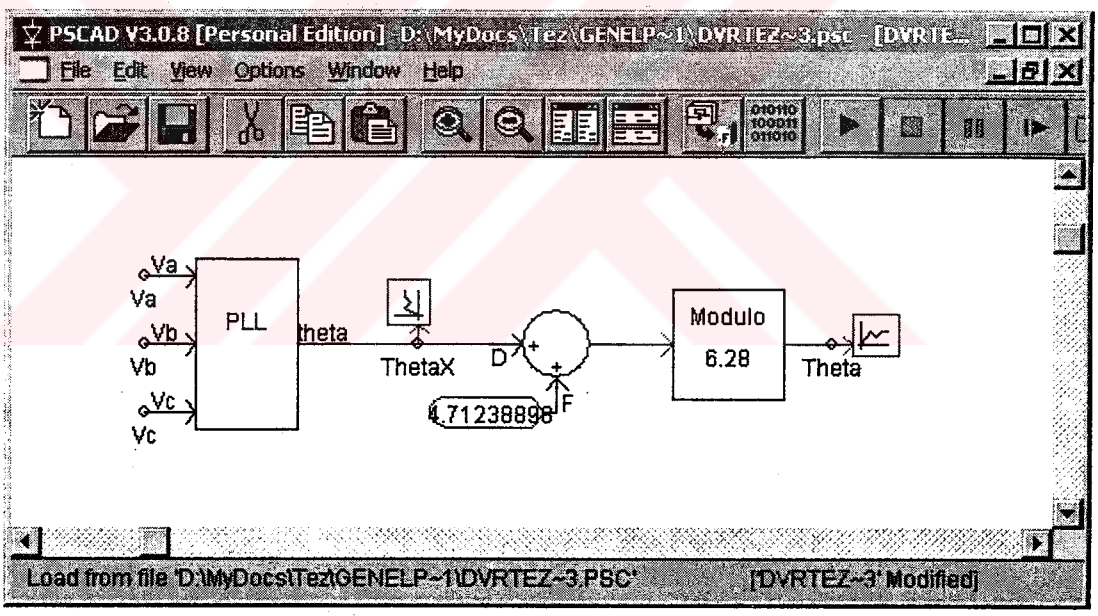

Figure A.2 PSCAD Simulation: Application of PLL Object

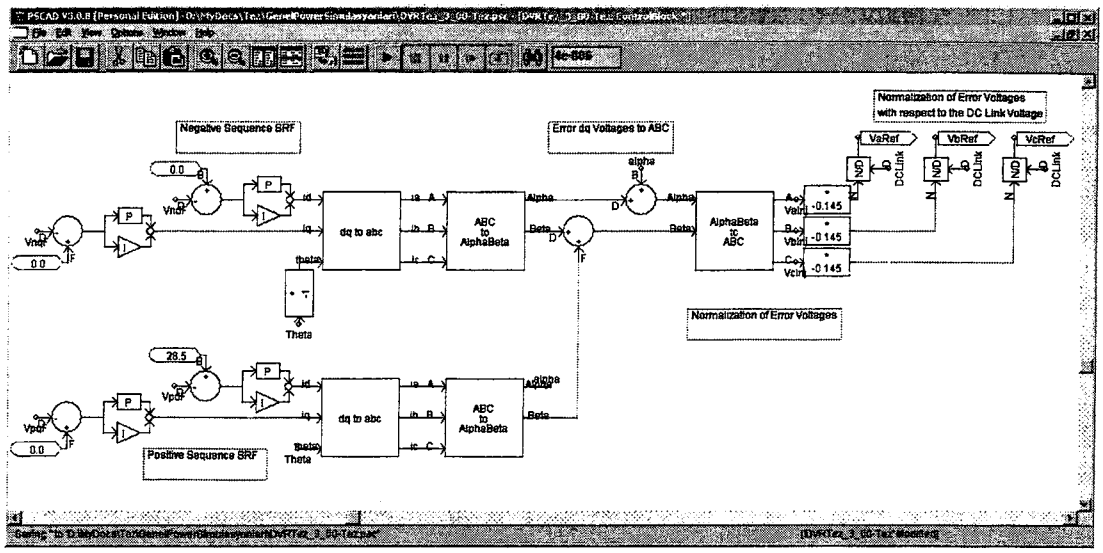

Figure A.3 PSCAD Simulation: Generation of Reference Signals

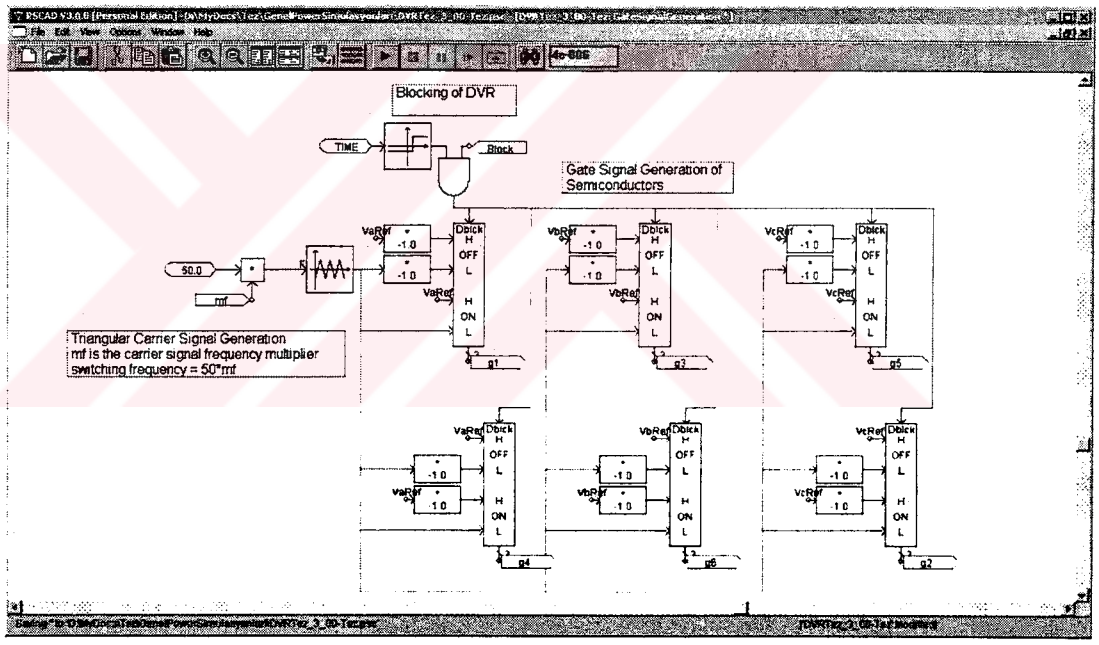

Figure A.4 PSCAD Simulation: Generation of PWM Gate Signals

The short circuit operation of the DVR and the zero-states during the PWM gating of the inverter is accomplished by the module shown in Figure A.5. The SCO operation has been achieved by triggering the upper leg of the each inverter to which constitutes a short circuit path for the DVR.

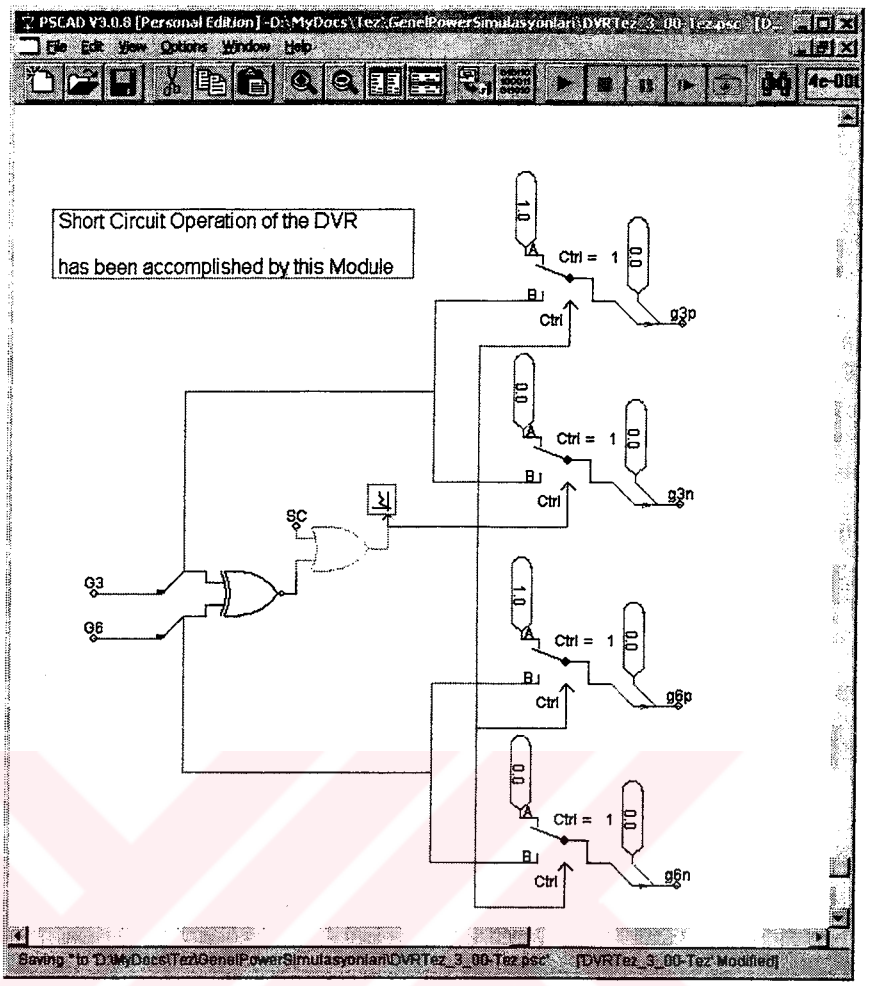

Figure A.5 PSCAD Simulation: SCO of DVR

A.2 MATLAB PROGRAMS

The harmonic frequency spectrum of the voltages and the currents, and the THD calculations are critical for determining the DVR parameters. These mathematical calculations have been done on the following MATLAB programs. The first program plots the frequency spectrum of the required array. The program parameters are the vector of voltage or current, the sampling time step of the vector and the repetitive frequency of the waveform. The program plots the frequency spectrum of the given vector.

The second program calculates the THD of the waveform which utilizes the first program in order to calculate the harmonics of the waveform.

A.2.1 MATLAB Program for Frequency Spectrum

```
function[spek,spek1]=freqspec(x,y,z)
% This function plots the harmonic spectrum of the waveform
% x is the waveform in the form of a vector
% y is the sampling time step
% z is the repetitive frequency of the waveform
h=inv(z)/y; %length of a vector in a period of repetitive waveform
time=zeros(length(x),1);
time=[0:y:y*length(x)];
time=time(1:h);
wav1=x((length(x)-h+1):length(x));% define a new vector which has
                                  %samples of the waveform in a
period
wav2=(2/h)*abs(fft(wav1));% fourier transform is taken and the peak
                          % amplitude of the harmonic components are
assigned
                          % to each entry of the vector, wav2
wav2(1)=wav2(1)/2; %avarage value is calculated

for n=0:100,
   wav5(z*n+1)=wav2(n+1);%wav5 contains harmonic compoents are
assigned according to the harmonic frequency up to 500z
   end;

for n= 1:4000,
```

```
   wav6(n)=wav5(n);%wav6 contains harmonic components up to 4000Hz.
end;
figure;
subplot(2,1,1),plot(time,wav1),grid,YLabel('magnitude'),XLabel('seco
nds');%plots one cycle of the period
subplot(2,1,2),plot(wav5),grid,YLabel('magnitude'),XLabel('frequency
');%plots the harmonic spectrum up to 500z Hertz
%subplot(3,1,3),plot(wav5),grid,YLabel('magnitude'),XLabel('frequenc
y');%plots the harmonic spectrum up to 400 Hertz
spek=wav5;
spek1=wav2;%wav2 and wav5 are the output vectors of this function
```

A.2.1 MATLAB Program for THD Calculation

```
function[spek]=Thd(x,y,z)
%This function calculates the total harmonic distortion of the
waveform
% x is the waveform in the form of a vector
% y is the sampling time step
% z is the repetitive frequency of the waveform

m=0;
h=inv(z)/y;
for k=(length(x)-h+1):length(x),
   m=m+(x(k)*x(k));
end;
I=(1/h)*m;
Irms=sqrt(I);%calculates the rms value of the waveform over a period

[wav5,wav2]=freqspec(x,y,z);%gets the harmonic components of the
waveform

I1=0;
for n=(z-5):(z+5),
I1=wav5(n)+I1;%finds the fundamental harmonic frequency component
end;

far=0;
for n=100:5000,
   far=far+wav5(n)*wav5(n)/2;
```

```
end;

I1rms=I1/sqrt(2);%calculates the rms value of the fundamental
                 %harmonic frequency component
Idis=sqrt((Irms*Irms)-(I1rms*I1rms));%total rms value of the
harmonic components
                                     %except the fundamental
harmonic
HF= I1rms/Irms
THDper= (far/I1rms)*100
THD=Idis/Irms*100
figure;plot(wav2);title('magnitude vs. harmonic number');
spek=wav5;
%fardis=sqrt(far-I1*I1);
%THDper1k=(fardis/Irms)*100
```