INSTABILITY STUDIES IN AMORPHOUS SILICON BASED ALLOYS

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ORHAN ÖZDEMİR

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Prof. Dr. Canan ÖZGEN
Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Doctor of Philosophy.

Prof. Dr. Sinan BİLİKMEN
Head of the Department

This is the certify that we read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Doctor of Philosophy.

Prof. Dr. Bayram KATIRCIOĞLU
Supervisor

Examining Committee Members

Prof.Dr. Bayram Katırcıoğlu _____

Assoc. Pr. Dr. İsmail Atılgan _____

Assoc Pf. .Dr. Cengiz Beşikçi _____

Prof.Dr Şenay Yurdakul _____

Prof.Dr. Demet Gülen _____

ABSTRACT

INSTABILITY STUDIES IN AMORPHOUS SILICON BASED ALLOYS

Özdemir, Orhan

Ph.D., Department of Physics

Supervisor: Prof. Dr. Bayram Katırcıoğlu

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The pixel element which is an integrated combination of a p-i-n diode with a thin film transistor (TFT) is used to produce image sensor arrays in scanning and displays technologies, necessitating the deposition of hydrogenated silicon based semiconducting and insulating thin films such as a-Si:H, a-SiNx:H over large area. The widely used techniques to achieve this goal is the plasma enhanced chemical vapor deposition (PECVD) due to its large area and low temperature (≤ 300 °C) abilities. In particular, PECVD has proved to be able to deposit both high quality insulator (a-SiNx:H) and active layer of p-i-n diode (intrinsic hydrogenated amorphous silicon carbide, a-SiCx:H) and by sequential deposition, it is possible to minimize the interface related problems, which play an important role in metal insulator semiconductor (MIS) and TFT structures.

PECVD deposited a-SiCx:H films over p-type crystal Si and metal substrates (MIS and MIM) were investigated by both admittance spectroscopy (Capacitance or conductance vs. voltage, temperature or frequency measurements) and Deep Level Transient spectroscopy (DLTS) to investigate the interface related problems. In this respect, instability phenomena (due to the creation of metastable states and charge injection into the gate electrode) were studied via the c-Si/a-SiCx:H (and/or a-SiNx:H) heterojunction. Specially, capacitance voltage kinetics were worked out and then the enrolled trap energies were identified with temperature mode DLTS.

The expertise gathered as a result of these studies were used in the fabrication and characterization of TFT's. In this respect, inverted gate staggered type Thin Film Transistor produced and characterized for the first time after Combo-251 Pattern Generator was implemented.

Keywords: İnstability, Percolation, Charge İnjection, MİS, TFT, Pattern Generator, Admittance Spectoscopy, DLTS, Large Area Electronics, İmage Sensor

ÖZ

AMORF SİLİSYUM TABANLI ALAŞIMLARDAKİ KARARSIZLIK ÇALIŞMALARI

Özdemir, Orhan

Doktora, Fizik Bölümü

Tez Yöneticisi: Prof. Dr. Bayram Katırcıoğlu

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P-i-n diyot ve ince film transistörün tümleşmesiyle oluşan gözenek, tarama ve görüntüleme teknolojisinde, görüntü sensor örgüsünün temel ögesidir. Bu yapının üretilmesinde kullanılan hidrojenlenmiş silisyum tabanlı yarıiletken ve yalıtkan ince filmlerin geniş yüzeyde biriktirilmesi gerekmektedir. Bu amaca ulaşmak için genellikle düşük sıcaklıklarda ve geniş yüzeylerde biriktirme yeteneğinden dolayı plazma destekli kimyasal buhar biriktirme tekniği (PECVD) kullanılmıştır. Özellikle, yüksek kaliteli yalıtkan (a-SiNx:H) ve p-i-n diyodun aktif bölgesinin (katkılanmamiş hidrojenlenmiş silisyum karbür, a-SiCx:H) PECVD tekniğiyle büyütülebileceği kanıtlanmiştır. Ayrıca, ardışık yapılan büyütmelerle ara yüzeyle ilgili problemlerin en aza indirilmesine çalışılmıştır. Bu arayüzeyler metal yalıtkan yarıiletken ve ince film transistör yapılarında önemli rol oynar.

p tipi kristal Silisyum ve metal taşıyıcılar üzerine PECVD ile büyütülmüş a-SiCx:H ve a-SiNx:H filmlerin, hem admittans spektroskopisi (sığa veya iletkenliğe karşı gerilim, sıcaklık veya frekans ölçümleriyle) hemde DLTS spektroskopisiyle ara yüzey durumları incelenmiştir. Bu yönden, kararsizlık olayları (yeni yerel durumların oluşması ve yüklerin ön elekroda doğru sızması) c-Si/a-SiCx:H (ve/veya a-SiNx:H) heterojen ekleminde yapılan ölçümlerle izlenmiştir. Özellikle, sığa gerilim kinetiği ve işin gerisinde olan tuzak enerji düzeyleri DLTS'in sıcaklık tarama moduyla belirlenmiştir.

Bu çalışmalar boyunca diyodlar üzerine ulaşılan birikim ve deneyim, ince film transistör (TFT) üretilmesinde ve özelliklerinin belirlenmesinde kullanılmıştır. Bu açıdan bakıldığında, alt geçit türü transistör, Combo-251 Biçim üreteci kullanılmak suretiyle, ilk defa üretildi ve karakterize edildi.

Anahtar Kelimeler: Kararsızlık, Sızma, Yük Enjeksiyonu, MİS, TFT, Biçim Üreteci, Admittans Spektroskopi, DLTS, Geniş Alanlı Elektronik

Dedicated to my wife, Özlem Evciler Özdemir

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CHAPTER 1

INTRODUCTION: LARGE AREA ELECTRONICS

1-1 Amorphous Silicon Based Alloys in Modern Electronics

Amorphous silicon and its alloys, apart from the fundamental importance in theoretical point of view, they are building stone of today's large area opto-electronics in the relevant market [1]. These large area devices have to stay large in dimensions as a necessity of man/machine interface such as image sensors, document scanners, electronic displays, printers etc… The crystalline silicon based conventional microelectronics could not satisfy the requirements of these large area opto-electronic devices due to both its poor optical properties and limited dimensions. The solutions developed on the semiconductors other than the crystalline silicon have created mismatching problems with the existing silicon based microelectronic structures.

Amorphous silicon whose huge amount of dangling bond states around midgap energy region (10^{20} $cm^{-1}eV^{-1}$) are reduced to minute amount (10^{15} $cm^{-1}eV^{-1}$) by the hydrogen compensation process, becomes able to be selectively doped both n and p types leading to a large number of practically useful devices such as p-n, p-i-n, Schottky diodes etc…[2]. As device feasibility of hydrogenated amorphous silicon (a-Si:H) has been achieved, the above mentioned two main drawbacks of crystalline silicon (c-Si), (namely poor optical properties and limited geometrical area or too high cost of material), are tried to be solved nowadays by this a-Si:H films. As for the optical weakness of c-Si the optical gap of a-Si:H is widened up to the visible region (≈1.75 eV) leading to the photoconductivity spectrum, shifted to shorter light wavelength compared with crystalline silicon. In other words, the a-Si:H spectrum coincides better with the sensitivity range of human eye (the alloying ability of a-Si:H with Ge, Sn, C, N and O creates a flexibility of adjusting the optical gap from IR to UV). Moreover, the optical absorption of a-Si:H is about 20 times larger than that of c-Si [3,4]. On the other hand, a-Si:H seems to be a solution to the large area problem of crystalline silicon because it can be deposited at low temperature (<300

°C) by the glow discharge method at reasonable cost as large area thin films on low cost substrate (such as glass and ordinary rude organic materials) [5].

Besides, the control of the electrical conductivity over 10 orders of magnitude [4] due to its dopability, the field effect allows the sheet conductance of a-Si:H layer to be switched over 6 orders of magnitude [6]. As a result, the development of thin film transistors for addressing circuits on large area electronics is facilitated by the fact that the gate dielectric layer (mostly a-SiNx:H film), the channel layer of a-Si:H film and the ohmic source and drain n^+ contact layers can all be deposited in the same plasma reactor (PECVD)[7].

This present work is a portion of much more extended “image sensors” project that has to be developed in the solid state electronic laboratory of METU Physics Department. Let us recapitulate the chorological development of image sensor based on both c-Si and a-Si:H semiconductors.

1-2 Comparison of imaging Array System on crystalline and amorphous Silicon

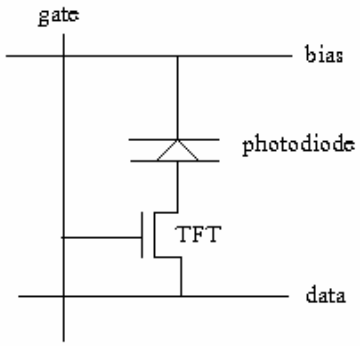


Fig.1.1 Pixel configurations constituted by transistor as a switch and a photo sensing diode.

One of the basis and most widely used pixel configurations is shown in fig.1.1. Each pixel is constituted by both a switching component (metal insulator silicon field effect transistor (MISFET) in c-Si case or thin film transistor (TFT) in a-Si:H case) and optical sensor. The pixel is connected to the matrix of gate and data lines as shown in fig.1.1. The configuration of a linear imaging array for photocopiers, fax machines and scanners is given in fig.1.2. In there, each block

has only one readout line but a high density of pixels. The source electrodes of all FETs in each block are connected to a single readout line. However, only one FET in each block is switched on at a time. The FET in one block is switched sequentially with the corresponding FETs in the other block. The output data of the blocks are scanned by multiplexing chip. By this way, no crossovers between signal lines occurs due to the sequential scanning, yielding a much better performance.

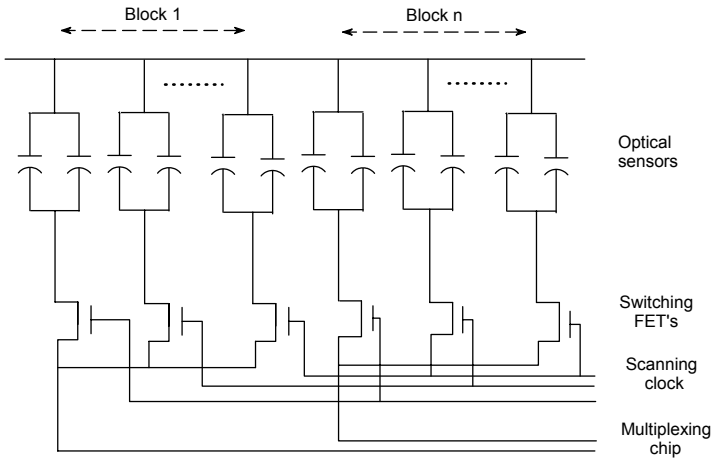


Fig. 1.2 Architecture of linear imaging array.

On the other hand, schematic representation in two dimensional imaging system (in optical/video cameras for optical imaging and imaging intensifier tubes for x-ray imaging) is given in fig.1.3 where the FET in each pixel behaves as a switch by means of source, drain and gate electrode connections. Drain (D) electrode is connected to the photodiode, source (S) is connected to a data line (being routed to an external charge sensitive amplifier) and the gate line is connected to the scanning clock generator so as to control the charge transfer from drain (D) to source (S). The gates for all the pixels in the same row are connected to a common scanning control line. All the pixels of the same column share a common data line and an amplifier. The readout of the entire detector can be performed in real-time, resulting the creation of 2-D images. The process of visualization of 2-D image is as follows; I) the scanning clock selects one row of FET switches and turns on all the switch in that row, ii) the charges on each photodiode are discharged from the photodiode to the input of (external) amplifier through the FET switch, iii) the clock trailing edge turns off the switch, iv) the signal at the amplifier input is

transferred to the output, v) the reset signal resets the amplifier input to zero, and vi) the above procedure is resumed until all rows are scanned.

a-Si:H has gained great promise in optical and x-ray imaging system where a-Si:H is used for both in photodiode as the image sensor and a-Si:H TFT as the switch.

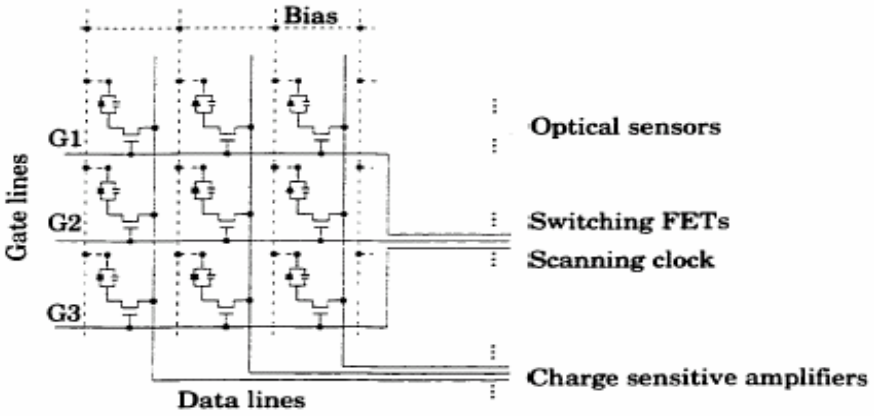
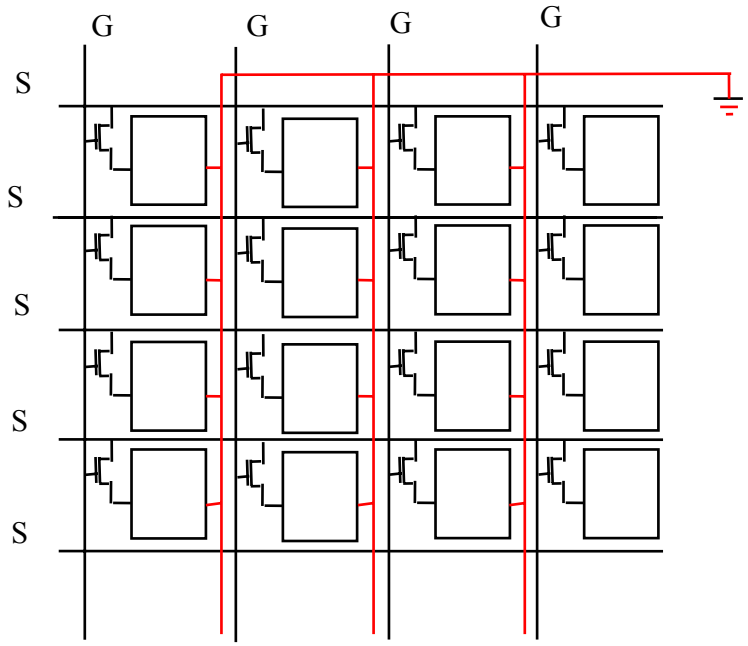


Figure 1.3: Architecture of 2-D imaging array.

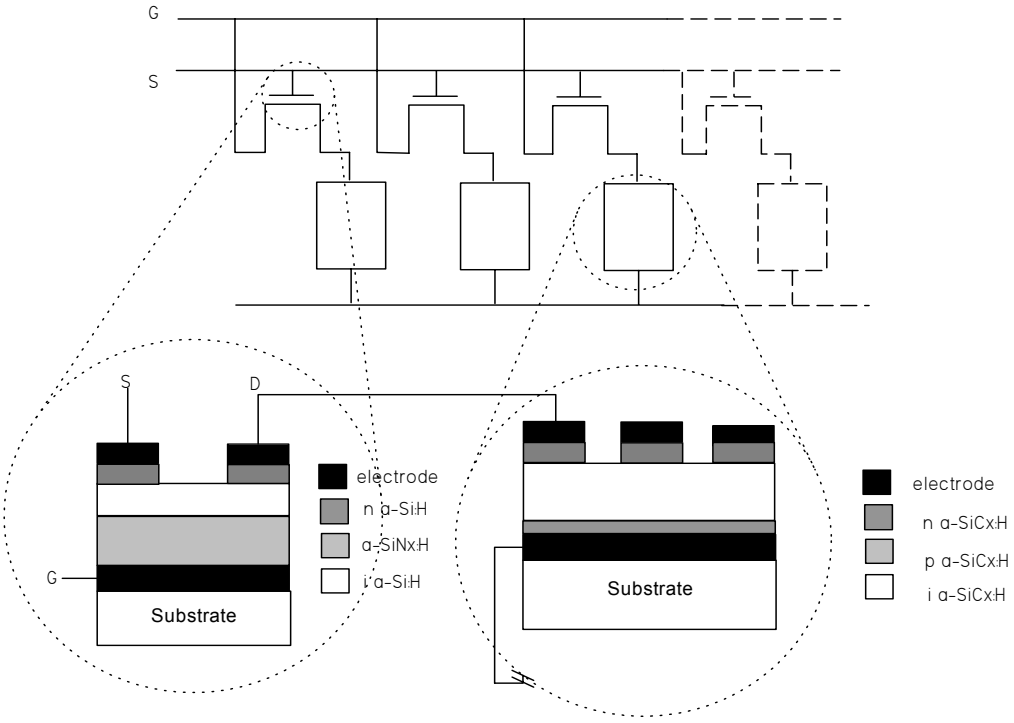
In addition, it is worth to note again that a-Si:H technology enables the easy manufacture of large area electronics at low temperatures in contrast to the single crystal (CCD or CMOS) technology which imposes restrictions in terms of either higher cost or limited detectable area.

As shown schematically in the figure 1.4, the pixel (= picture element) of the matrix array may be fabricated totally by various silicon based amorphous thin films deposited by using a single plasma reactor (PEVCD). The pixel is constituted by a pair of components: a “p-i-n” photo sensing diode and switching thin film transistor (TFT). The photo diode is connected to drain terminal of the transistor which in turn connected on one side to the drain (D) line by the source terminal, on the other side to the gate (G) line by the gate terminal (fig.1.4). The complete array is accessed by sequentially addressing all the gate line (G). A specially designed readout chip is used to sense the photo signals on each of the data lines (D). In other words, under illumination the photodiode accumulates the charges while TFT is turned off, turning on the TFT allows the accumulated charge to flow out of the data line (D) where it can be detected by external electronic circuit in succession. The fact that, in this

technology, both the array of image sensor and the scanning microelectronic circuit are silicon based leads to an increased reliability and lower cost.



(a)



(b)

Fig.1.4 (a) The matrix addressing of an image sensor array, (b) detailed view of image sensor with constituent pair of components; p-i-n (right) and TFT (left) structures, respectively.

1-3 Photo sensing Components of a pixel:

The ultimate goal of this work is to deal with the large area imaging system using a-Si:H technology. As discussed above, image sensor element might be either photoconductor, photodiode or photo TFT. The characteristic feature between them is given in table 1.1. As seen in the table, the leakage current of the diode structures is lower than those of the conductor and photo-TFT structures. In that sense, both Schottky type and p-i-n type diode is used in this work as an constituent part of image sensor but the leakage current of Schottky type is a bit higher than p-i-n structure, necessitating further work to reduce the leakage current (10^{-10} A/cm^2 leakage current is acceptable to be a candidate in an imaging system).

Table 1.1 Comparison of characteristic features of image sensor elements.

	Photoconductor	Schottky Diode	p-i-n	Photo-TFT
Photo Sensitivity	High	Low	Low	High
Response time (μsec)	Slow($\approx$ 500)	Fast ($\approx$50)	Fast (<5)	Slow($\approx$500)
Dark Current (Acm^{-2})	$\approx 10^{-6}$	10^{-7}-10^{-9}	10^{-10}-10^{-12}	10^{-7}-10^{-8}
Stability	Good	Good	Good	Acceptable
Large Area Compatibility	Yes	Yes	Yes	Yes

1.3.1 Schottky Type Diode

Optical sensors must have high photosensitivity, low leakage current, high photo response, stability and process simplicity. Schematic representation of Schottky type photodiode (ITO/I a-Si:H/n$^+$ a-Si:H/Cr) is given in fig. 1.5 where ITO is used as both a metal contact to form Schottky barrier and a light window which permit the light to go to the a-Si:H layer. Also, the intrinsic a-Si:H serves as an

active layer where electron-hole (e-h) pairs are generated upon illumination, n^+ a-Si:H acts as an ohmic contact between the a-Si:H and the bottom electrode.

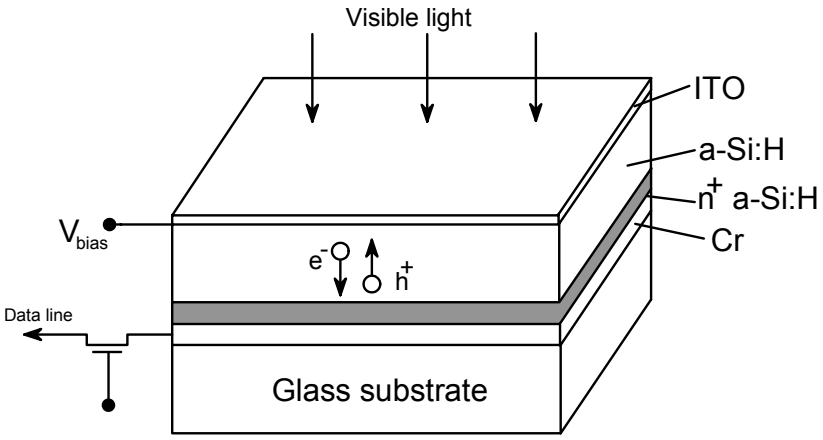


Fig.1.5 Illustration of Schottky diode.

Lastly, Chromium (Cr) metal is used for collecting the photo generated carrier (usually electrons due to higher mobility). Charge density is determined by the charges associated with localized states in the mobility gap oppose to crystalline case where charge density is determined by shallow donors or acceptors in depletion region.

The intrinsic a-Si:H has sufficient carrier lifetime to enable the separation of photo generated carrier pairs even without an external bias. At reverse bias, the intrinsic a-Si:H can sustain a fairly wide depletion region within either the Schottky barrier, or p-type region of a-Si:H based a p-n junction. In the former, the Schottky barrier serves as an electron blocking electrode so electron injection might be omitted. Also, photo generated carriers captured by traps, build up a space charge region, allowing high field that might reduce the applied field to low values in this region. For overcoming this drawback, a high enough applied field must be retained so that carriers can travel across the a-Si:H active layer.

1-3-1 p-i-n Type Diode

It should be noted that unlike the c-Si case, in a-Si:H both the p-n diode for the photodiode and the bipolar transistor structure for the switching elements are

ineffective due to the high density of defects. This high density of defects leads to very low diffusion length, as a result, the contribution of neutral parts (diffusion contributions) becomes negligible, depletion contribution (drift contribution) is dominant. In order to magnify this drift effect, an undoped intrinsic (i) layer is inserted between n and p regions (p-i-n). The p-i-n structure, which is important for light emitting diodes (LED) is schematically given in the fig. 1.6 and 1.7, for equilibrium and polarized states of low injection condition. Because of the difference between the optical energy gaps of p, i and n regions, at the p/i and i/n junctions built-in potentials (Band discontinuities) of ΔE_v and ΔE_c are formed.

Apart from a-Si:H, at present, hydrogenated amorphous silicon carbide (a-SiCx:H) thin film, grown on various substrate by the low temperature plasma enhanced chemical vapor deposition (PECVD) has become promising material for visible light emitting/sensing devices due to both its adjustable optical gap to any value within the visible region and its ability for large area flat panel displays [8-10]. A p-i-n diode of a-SiCx:H thin film as injecting device for LED application has been proposed [8]: electrons from n-side, holes from p-side are injected into the same intrinsic (i) intermediate region (shown in fig.1.7). In this respect, the carrier transport and recombination phenomena throughout the active intrinsic layer are primordial, requiring a detailed investigation of localized electronic state distribution within the energy gap (or pseudo gap).

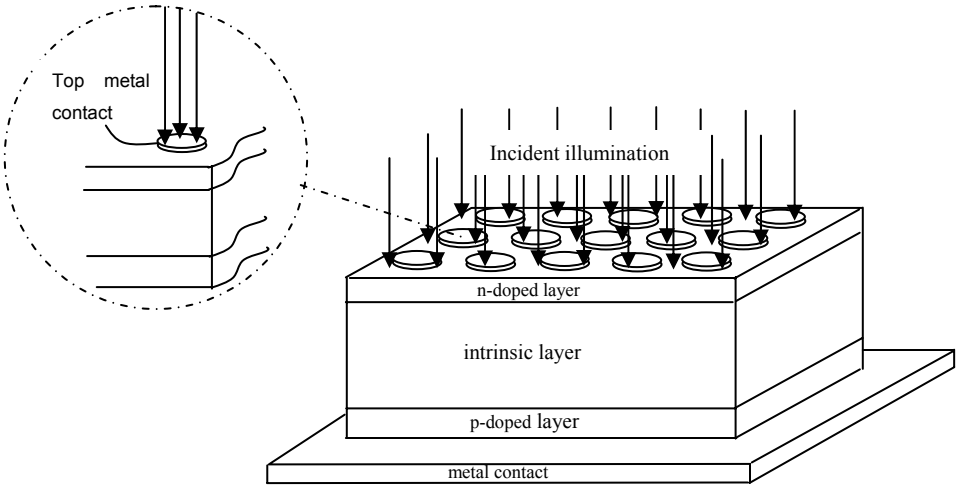


Figure 1.6 Structure of a-Si:H p-i-n photodiode.

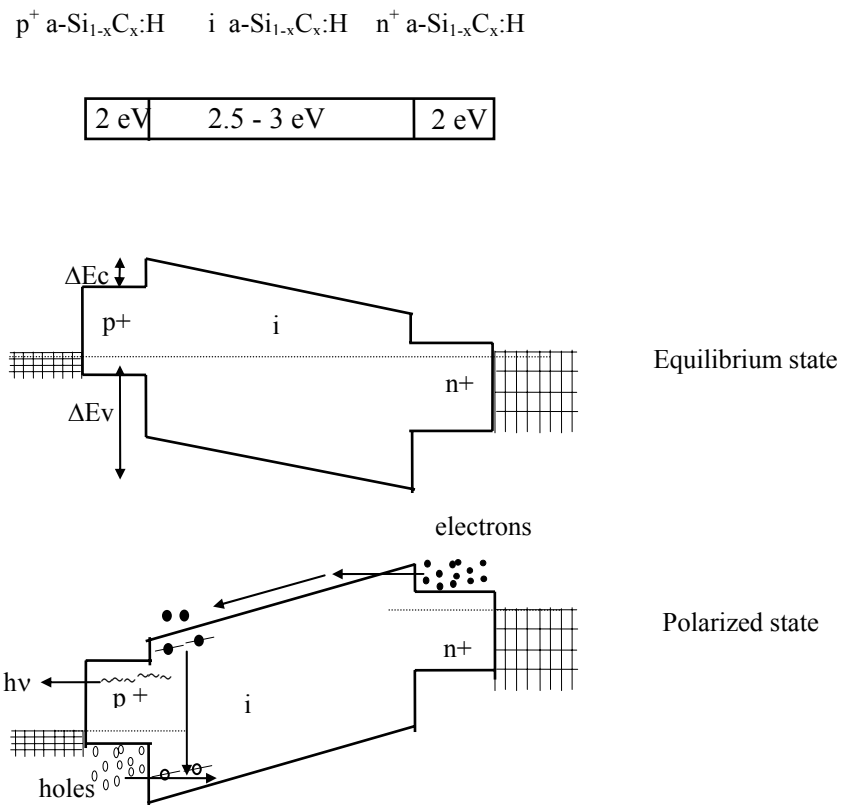


Figure 1.7 The equilibrium and polarized states of energy band gap structure of a-$Si_{1-x}C_x$:H p-i-n diode at low injection condition.

1-4 Switching Component of a Pixel: Thin Film Transistor (TFT)

1-4-1 Introduction

Due to the previously cited low diffusion length (which seriously limits the switching speed) in a-Si:H, the bipolar transistor structure is not suitable for switching element, instead, the field effect (FET) type thin film transistor (TFT) (fig. 1.8) is well suited to the a-Si:H case. In general for TFT, n-channel accumulation mode operation, using an undoped intrinsic a-Si:H channel is widely used. (The depletion mode is avoided, again due to the high defect density of doped a-Si:H film which makes difficult to deplete the channel).

After exploitation of dopability of hydrogenated amorphous silicon by W.E Spear and P. G. Lecomber, much technological and scientific investigations have

taken place and then the first device was made by D. Carlson and C. R. Wronski in 1976. Together with its photosensitive properties in photovoltaic, a-Si:H has been used as a switching device in large area electronics such as solid state imagers, printers, scanners and flat panel displays where a-Si:H is used as the semiconducting material in the thin film transistor (TFT) to provide the switching element. Recently, the demand for large area display applications such as portable computers has driven much of the research in a-Si:H technology. However, the basic transistor structure has not changed much and today's mainstream technology uses transistors that, apart from minor variations, are similar to the inverted staggered structure due to the lack of low-cost large area doping technique (see fig. 1.8).

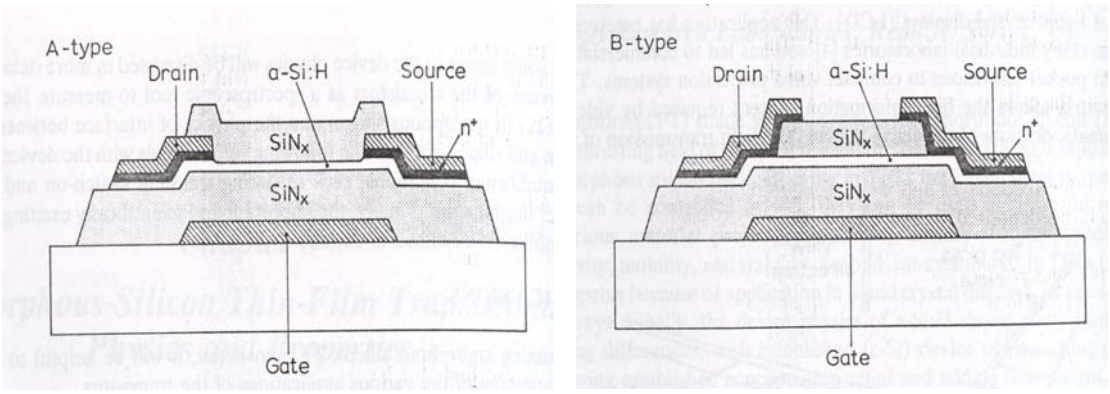


Fig.1.8 Widely used inverted staggered structure of transistor in A and B types. Note that in type A, the gate insulator, intrinsic and n^+ doped a-Si:H are deposited in single deposition, top passivation layer deposited in separate one, whereas for type B, gate insulator a-SiNx:H, a-Si:H and top passivation layer of a-SiNx:H are deposited in one run, but n^+ in a separate one. From: [9].

Fig 1.8 shows two types of inverted staggered transistors, for convenience, they are called type A and B (differ in the order of deposition of n^+ contacts and top passivation nitride). The transistors are fabricated on a rude/glass materials to reduce the cost using standard semiconducting processing technique such as photolithographic patterning and etching. The fabrication process of transistor is as follows: metal (typically Cr) coated glass are patterned (by means of photolithograph on the metal layer) and placed in the chamber of PECVD reactor where source gases, silane (SiH_4) and ammonia (NH_3) are introduced for the deposition of both

silicon nitride and amorphous silicon layers. In the fabrication of type A transistor, the gate insulator silicon nitride, the active layer intrinsic a-Si:H and the n^+ a-Si:H for the contacts are deposited consecutively. Then, a metal layer (Cr or Al or Mo) is evaporated on the semiconducting layers and then the transistor channel is defined by etching away the top metal and n^+ a-Si:H layer by photolithography.

1-4-2 Electronic Behavior of TFT's

Both of the mentioned structures operate in a similar fashion, that is, when a positive bias is applied to the gate, electrons are induced at insulator/film interface in an amount of $C_{ins}V_G/q$. For small gate voltages, until the threshold voltage, these electrons will be localized in the deep states of the amorphous silicon, beyond this threshold, a linearly increased amount of induced electrons as a function of gate voltage will be mobile, contributing to conductivity (i.e., the transistor switches on, and a current flows between source and drain). The n^+ layers serves to reduce the contact resistance between contact metal and intrinsic amorphous silicon.

For the application of negative gate bias, in spite of induced hole accumulation at the interface, the resulting current along the hole channel is not enough since n^+ contacts cannot supply enough holes to sustain a significant current on one side (the n^+ layer should have been replaced by p^+ one), on the other side these available holes have very low mobility (nearly two orders of magnitude less than that of the electrons). Nevertheless, this hole channel formation, despite its little practical significance, may be used to investigate eventual instability mechanisms in a-Si:H.

1-4-3 Current Voltage Relation

The reasons for choosing a-Si:H as the semiconducting material are as follows: (1) dopability of a-Si:H both n- and p-types leading to p-n junction based devices, (2) possibility of deposition over large areas at low temperature allowing low cost substrates such as ordinary glass, (3) good interface properties between a-Si:H and other thin film materials, (4) the off current of a-Si:H TFT is very low (order of pA) due to its high resistivity, and (5) non-toxicity feature yields the wide

acceptance of a-Si:H among many candidates to make TFT. Due to higher mobility of electrons, n-type a-Si:H is grown on amorphous silicon nitride (a-SiNx:H) thin film to form TFT structure. a-SiNx:H gate dielectric, the a-Si:H channel and a top nitride passivation layer are all deposited in one run of glow discharge technique (i.e., PECVD). Source and drain contact are grown later on protecting passivation layer. The derivations done for c-Si MOSFET are also valid in a-Si:H TFT except a-Si:H TFT operates in accumulation mode whereas MOSFET operates in inversion mode [11]. For formulating the I-V characteristic, the following conditions are assumed: (1) the carrier mobility is constant in the channel, (2) the gate capacitance is constant and independent of the gate voltage, (3) the source and drain electrodes are ohmic, (4) initially, n_0 charge density exist in the semiconductor and finally (5) the longitudinal electric field is greater than the transverse field in the channel.

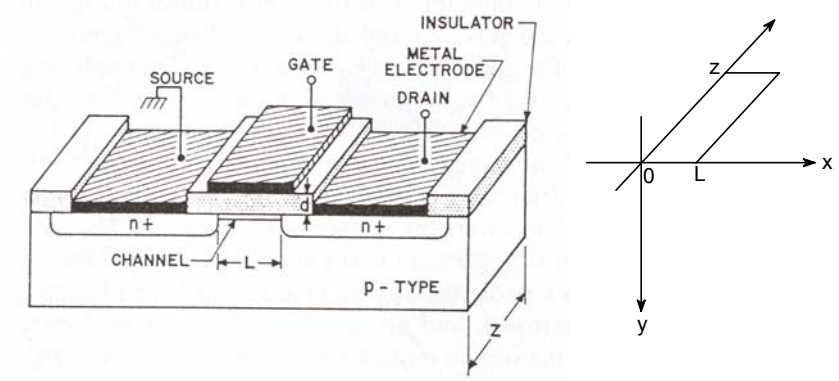


Fig.1.9 Schematic view of MISFET. Channel length (L), the channel width (Z), and the insulator thickness (d) are important parameters.

Application of a gate voltage V_G induces a density $\Delta n(x)$ of electron at the position x in the channel region and the following relation may be established:

$$e\Delta n(x) = \left(\frac{C_N}{x_{si}}\right)\left[V_G - V(x)\right] \qquad (1.1)$$

where x_{si} is the semiconductor thickness, C_N is the gate capacitance per unit area $\left(=\varepsilon_N / x_N\right)$ and $V(x)$ is the drain voltage at x from the source. If x_{si} is sufficiently small, the drain current I_d is given by

$$I_d = x_{si} Z[\sigma_0 + \Delta\sigma_0(x)]E_x \qquad (1.2\text{-a})$$

$$= x_{si} Ze\mu_n[n_0 + \Delta n_0(x)]E_x \qquad (1.2\text{-b})$$

where σ_0 and $\Delta\sigma(x)$ are the initial and the incremental conductivities due to n_0 and $\Delta n(x)$, respectively. Inserting eqn.1.1 into eqn.1.2-b leads to

$$I_d = Z\mu_n C_N[ex_{si}\, n_0/C_N + V_G - V(x)]\frac{dV(x)}{dx} \qquad (1.3)$$

Integrating both sides along the channel results

$$\int_0^L I_d dx = Z\mu_n C_N \int_0^{V_d} [ex_{si}\, n_0/C_N + V_G - V(x)]dV(x) \qquad (1.4\text{-a})$$

$$I_d = \mu_n C_N \left(\frac{Z}{L}\right)\left[(V_G - V_T)V_d - V_d^2/2\right] \qquad (1.4\text{-b})$$

where the threshold voltage $V_T \equiv -\frac{ex_{si} n_0}{C_N} \propto n_0$ (1.4-c)

For image sensors, TFT must satisfy the following criteria: The value of the "ON" resistance must be around $10^6\ \Omega$, while "OFF" resistance must be above $10^{14}\ \Omega$ and the parasitic capacitance must be low. Typical TFT drain current vs. gate voltage is shown in fig. 1.10. TFT uses the linear region of I_D vs. V_D during the operation of image sensor. In this regime, the "ON" resistance of TFT can be expressed as [12]

$$R_{on} = \frac{V_{SD}}{I_{SD}} = \left[C_N \mu (V_G - V_T) W/L\right]^{-1} \qquad (1.5)$$

where W and L are the width and length of the TFT, respectively. For x_N= 3000 Å and μ_n= 0.8 cm^2/Vs, R_{ON} becomes $R_{on} = 25\left[(V_G - V_T) W/L\right]^{-1}$ MΩ. Therefore a MΩ order is achieved by taking W/L ratio as 1-5 and V_G-V_T as ~10 V with V_T in the range of 0-2 V. In the sub-threshold region where V_G<V_T, a high off resistance is obtained (~$10^{15}\ \Omega$).

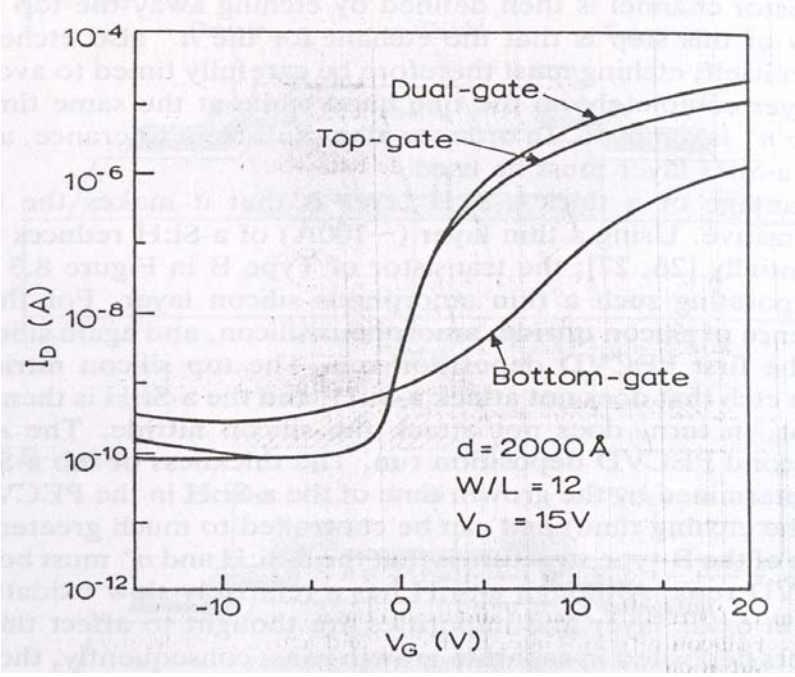


Fig.1.10 Typical drain current vs. voltage relation, for top, bottom and dual gate TFT structures. From [9].

1-4-4. Alternative Structures

In the inverted staggered structure, the channel is induced on one side only of the amorphous silicon. However, by means of putting an extra layer over the top passivating layer (see fig. 1.11), a second gate can be formed and a channel induced on the top side of the a-Si:H, yielding an increase of the transistor current (shown in fig 1.10). The increase of the current may be explained as follows; in dual gate mode, the field lines originating from the gates cannot penetrate as deeply into the a-Si:H as they can in single gate case due to the field from the opposite gate. In other words, charge is distributed closer to the interface causing increasing the fraction of the total charge situated in the extended states. In light of this information, it is expected that the threshold voltage of the transistor decreases, enhancing the current compared to single channel mode.

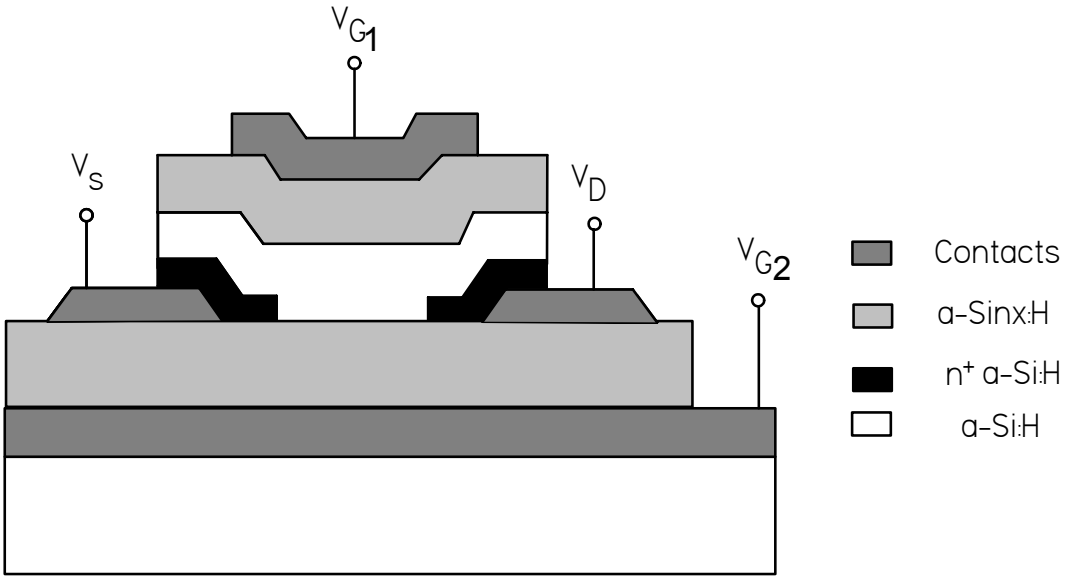


Fig. 1.11 Putting a second gate on top silicon nitride yields a dual gate TFT structure. Keep in mind that electron accumulation can be induced on both sides of a-Si:H, doubling current through device.

Another way to improve the current is by shortening the channel length of the device. With the special techniques, less than 1 μm channel length could be produced but large area technologies (especially in display and printers) requires the channel length below 10μm. To remove this contradiction, the device structure can be turned 90° (see fig1.12). However, since the large horizontal area of the source and drain contacts relative to the thickness of the spacing insulator, many field lines from the drain will terminate on the back of the a-Si:H, creating an electron channel that leads to a higher off currents, engineering features could be applicable to remove the effect but results a complicated structure and increase the cost.

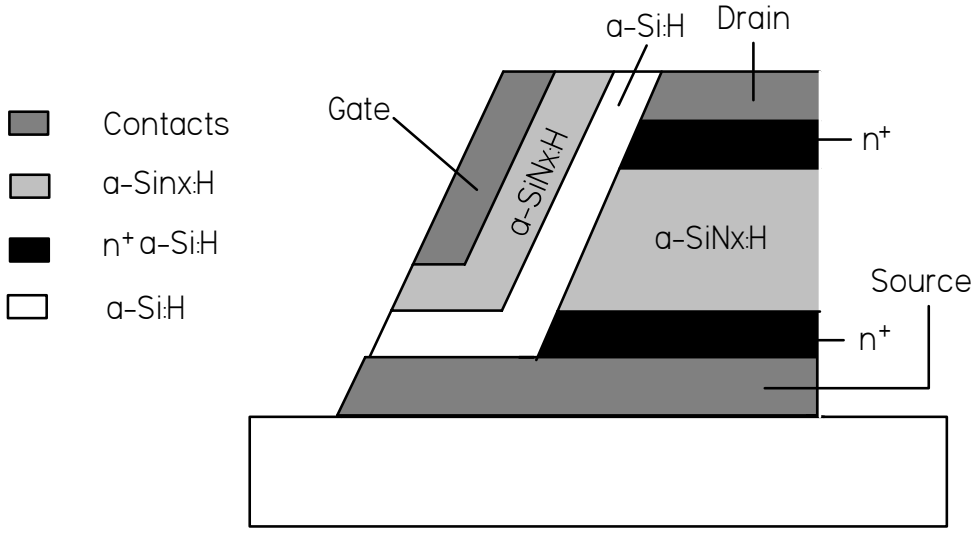


Fig. 1.12 Another alternative TFT structure, a vertical source and drain contacts are formed in horizontal layers, separated by spacer a-SiNx:H.

1-4-5 Effects of Contact metals and Candidate semiconducting/insulating films to improve TFT Performance

Even though two mask processes is able to achieve a displays, the trend for many today's prototypes is toward fewer masks, generally speaking, more complicated structure. Almost all of these transistors are classified as inverted staggered with a-SiNx:H/a-Si:H channel interface. In contrast to changing the transistor structure, other features (such as contact metal in one side and insulator film(semiconducting) on the other side) reduce the possibility of transistor failure. For example, instead of Cromium (Cr) and Aluminum (Al), a tantalum (To) alloy as gate line material helps to substantially reduce the line resistivity. Moreover, using double insulator layers (such as tantalum oxide over silicon nitride) avoids the problem of pinholes in the nitride while still using the good interface properties of the silicon nitride/amorphous silicon interface. Nowadays, the high dielectric constant materials (known as high-k materials, one of them is tantalum oxide) allows for a smaller gate voltage. In addition to that, instead of a-Si:H, μc Si may be used as a semiconductor due to its higher mobility.

In summary silicon based hydrogenated amorphous films [with their p and n type dopability, their field effect behavior, their ability to be deposited on large area at low temperature on low cost substrate within the same plasma reactor (PECVD), their compatibility with the existing crystalline silicon based microelectronic technologies, their improved optical properties (higher optical absorption) and their adjustable band gap from IR to UV by various alloying process] constitute a whole so called amorphous silicon technology for large area opto-electronics. However, the main drawback of this technology is metastability or degradation problems, originated from continuous evolution of the atomic configuration within the amorphous materials under the functioning circumstances. The following chapter is devoted to the defect chemistry behind these metastabilities.

CHAPTER 2

DEFECT CHEMISTRY- METASTABILITIES IN AMORPHOUS SILICON BASED ALLOYS:

2-1 Metastabilities in a-Si:H Thin Films-Defect Pool Model

The permanent defect creation and removal mediated by the hydrogen migration has been considered as the reason of these metastabilities. The local bonding environments of hydrogen atom within these hydrogenated amorphous materials and its eventual motion under external stresses (such as temperature, electric field, illumination etc…) are not well understood. Several attempts has been made, leading to famous defect pool model, first proposed by Smith and Wagner [13] and later developed by Powell et all [14]. Let us remind the main points of this model. First it has been carried out that the density of localized energy level E_{vt} of weak bonds (WBs) or tail states $g(E_{vt})$ is exponentially decaying as a function of E_{vt} from the edge of extended states E_v, deep inside the energy gap ($= N_{v0} \exp \frac{E_v - E_{vt}}{E_{v0}}$ with E_{v0} being disorder parameter, depending on the material and its growth conditions) as shown in figure 2.1 below.

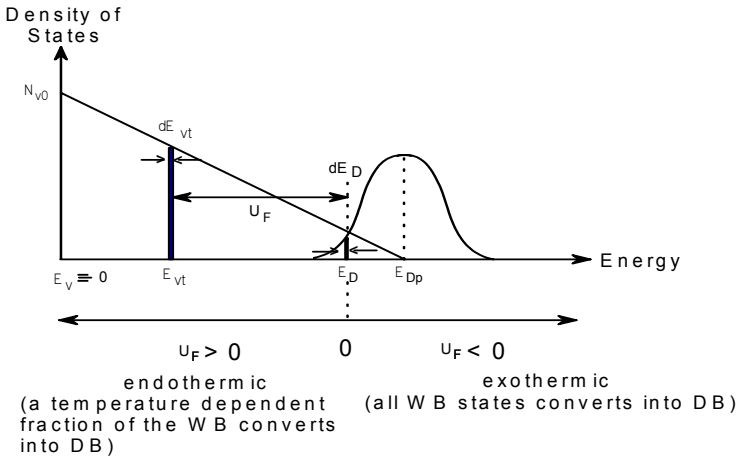


Fig.2.1 Illustration of the conversion of WB into DB leads to change of the electron (from a bonding state E_{vt} in the valance band to non-bonding state E_D in the gap).

There is a thermodynamical equilibrium between the existing WB density d(WB) of average energy E_{vt} (between E_{vt} and $E_{vt}+dE_{vt}$) and dangling bond (DB) density d(DB) of average energy E_D (between E_D and E_D+dE_D): $d(WB)_{eq} = d(DB)_{eq} \exp\frac{U_F}{kT}$ with U_F formation energy. The sum of d(WB) and d(DB) is equal to the potentially adequate WB density for conversion to the DB density of energy E_D:

$$d(WB)_{eq} + d(DB)_{eq} = g(E_{vt})P(E_D)dE_{vt} \qquad (2.1)$$

where $P(E_D) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left[-\frac{(E_D - E_{DM})^2}{2\sigma^2}\right] \equiv$ fraction of potentially available WBs (defect pool) for DB creation at the average energy E_D with E_{DP} = most probable DB energy, $\sigma =$ pool width (which is a characteristic measure of the actual disorder together with E_{v0} of the tail state distribution). Note that in the above relation (2.1), WBs corresponding to each infinitesimal interval dE_{vt}, have been considered as different chemical species; all the WBs from energy E_v to ∞ should be integrated [15-17].

2-1-1 Role of Hydrogen in defect creation

WB↔2DB (2.2)

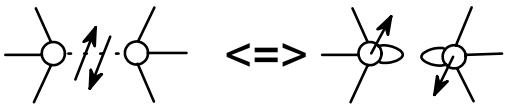


Fig 2.2. Schematic model for the weak bond-dangling bond conversion

The chemical equilibration process due to the interconversion of the WBs and DBs contains an inconsistency since a configuration where two DBs at the same site contradict the ESR experiment which points out an isolated neutral DB. As this pair could not move away from each other at relatively low temperature, an interstitially mobile species, the hydrogen atom, might intervene in the microscopic process [18,19] through schematic illustration of the chemical reactions below:

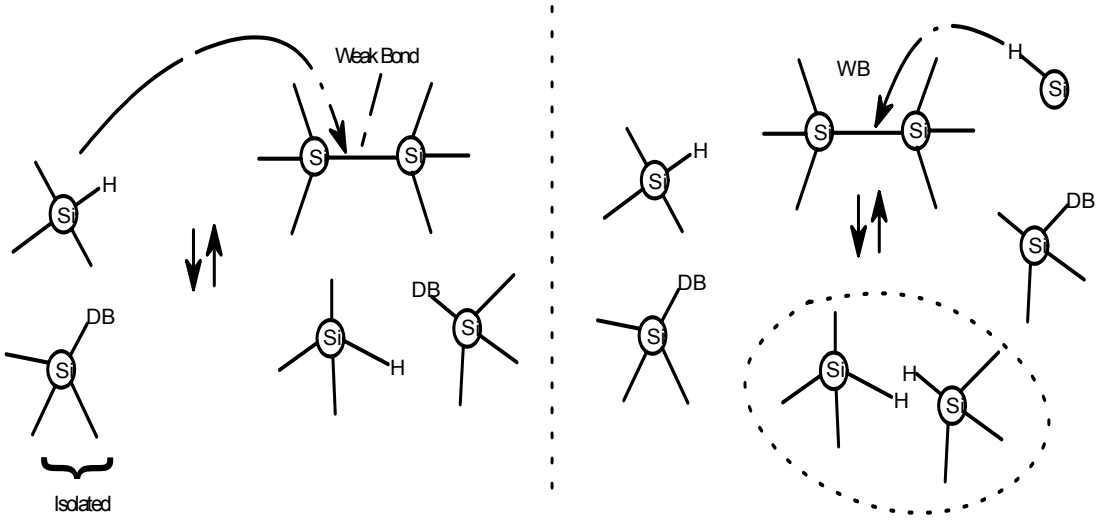


Fig 2.3. The eventual hydrogen involved (or mediated) equilibrium or equilibration. Note that in the first picture, two defects are formed, one originated from the isolated SiH bond, the second (SiHDSi) originated from the singly hydrogenated SiSi bond(i.e., $SiH + (SiSi)_{WB} \leftrightarrow DB + SiHDSi$). However, for the second case, SiSi bonds can have only zero or two H atoms which means that the correlation energy (the energy cost of putting a second electron in the bond) for H occupancy is negative ($2SiH + 2(SiSi)_{WB} \leftrightarrow 2(DB) + (SiHHSi)$).

$$SiH + (SiSi)_{WB} \leftrightarrow DB + SiHDSi \qquad (2.3\text{-a})$$

$$2SiH + 2(SiSi)_{WB} \leftrightarrow 2(DB) + (SiHHSi) \qquad (2.3\text{-b})$$

In the reactions above, the hydrogen atom is strongly bound to Si (binding energy of Si-H is about 3-4eV). This bound hydrogen might be released from this site to mobile (or interstitial) site through multiple excitation along “localized” states between SiH site and mobile site. As a result, interstitial hydrogen (H_I) and interstitial hydrogen site (I) should be introduced as species involving in the equilibrium or equilibration via the following chemical reaction:

$$SiH + (I - H_I) \leftrightarrow DB + H_I \qquad (2.4\text{-a})$$

$$(SiHDSi) + (I - H_I) \leftrightarrow SiSi + H_I \qquad (2.4\text{-b})$$

$$(SiHHSi) + (I - H_I) \leftrightarrow (SiHDSi) + H_I \qquad (2.4\text{-c})$$

According to reaction 2.4-a, which states that DB defect formed on the isolated SiH site should not be energetically favorable (due to the energy considerations since SiHDSi DB concentration, by far, exceeds that of the isolated DB concentration, so isolated DB's are omitted). Consequently, the eq. 2.4-b and c become the main reactions of equilibrium and equilibration: this microscopic model involves the release of a mobile interstitial hydrogen atom (H_I), from a SiHHSi complex in the valance band tail to create one DB (SiHDSi) (depicted in the fig 2.4.)

$$\left(SiHHSi \leftrightarrow SiHDSi + H_I\right) \qquad \left(SiSi + H_I \leftrightarrow SiHDSi\right)$$

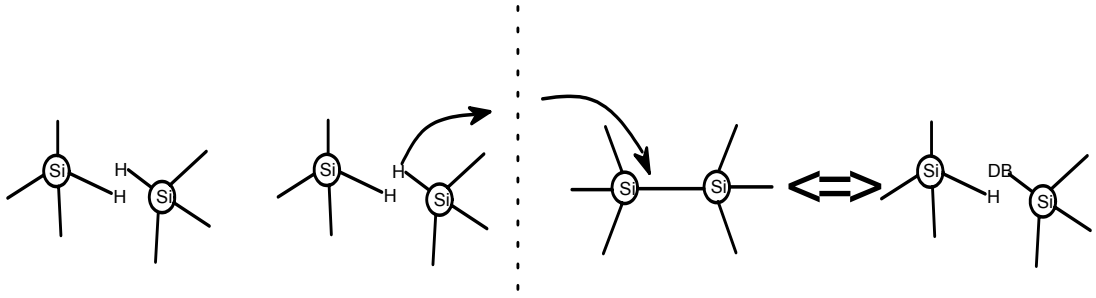


Fig 2.4 Schematic illustration of H diffusion through the network. Note that the mobile H inserts into a SiSi bond at remote site to give a second DB.

The addition of the above two successive reactions gives an overall reaction:

$$\left(SiHHSi\right) + \left(SiSi\right) \leftrightarrow 2\left(SiHDSi\right) \qquad (2.5)$$

As to correlation energy U_H of H atom, the last reaction can be expressed as follows: for the case of U_H <0, taking into account the energy distribution of both WBs and DBs, the above relation represent the superposition of very large number of reactions. In this respect, for most SiSi bonds, the hydrogen correlation energy is negative, and then the reaction (2.5) would be right to left side only. However, for the case of U_H>0, singly H occupied SiSi sites are favored leading to SiHDSi type DB defect sites, as a result the reaction (2.5) would be from left to right. In other words, as the isolated DBs, originated from isolated SiH sites are neglected, for the

evaluation of DB density, SiHDSi sites should be considered. After applying the law of mass action and little algebra, the following relation is obtained:

$$\frac{\delta[SiSi]_{eq}}{\delta[SiHD]} = \left(\frac{N}{H}\right)^{1/2} \exp\left[\frac{E_v + E_D{}' - 2E_{vt}}{kT}\right] \qquad (2.6)$$

where $\delta[SiSi]_{eq}$ represents the equilibrium concentration between E_{vt} and $E_{vt}+dE_{vt}$ with $\delta[SiSi]_{eq} = \delta[SiSi]_{total} - \delta[SiHDSi]$. While $\delta[SiSi]_{total}$ is the density of all the WB states between E_{vt} and $E_{vt}+dE_{vt}$ which would form (potentially) DB defects between E_D and E_D+dE_D and represented by eq.(2.1). In the light of this information, the changes in DB defect density can be expressed as;

$$dD(E_D, E_{vt}) = \frac{g(E_{vt})P(E_D)dE_{vt}}{1 + (N/H)^{1/2} \exp\left[\frac{E_v + E_D{}' - 2E_{vt}}{kT}\right]} \qquad (2.7)$$

$$dD = \frac{g(E_{vt})P(E_D)dE_{vt}}{1 + \exp\left[\frac{E_v + E_D{}' - 2E_{vt} + 1/2\ln[N/H]}{kT}\right]} \text{ with } E_D{}' = E_D + kT\ln\left[\frac{f^0(E_D)}{2}\right] \qquad (2.8)$$

Defining a new parameter $\left(2\xi \equiv E_v + E_D + kT\ln\left[f^0(E_D)/2\right] + kT\ln[N/H]\right)$ cause the integration splitting;

$$D(E_D) = \int_{E_v}^{\infty} dD(E_D, E_{vt}) = \int_{E_v}^{\infty} \frac{g(E_D)P(E_D)dE_{vt}}{1 + \exp[2(\xi - E_{vt})/kT]} = \underbrace{\int_{E_v}^{\xi}}_{\substack{\xi > E_{vt} \\ I_1}} + \underbrace{\int_{\xi}^{\infty}}_{\substack{\xi < kT \\ I_2}} = I_1 + I_2 \qquad (2.9\text{-a})$$

with $I_1 \approx \int_{E_v}^{\xi} N_{v0} \exp\left[\frac{E_v - E_{vt}}{E_{v0}}\right] \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left[-\frac{2(\xi - E_{vt})}{kT}\right] dE_{vt}$ (a Boltzmann fraction of WB are converted) (2.9-b)

and $I_2 \approx \int_{\xi}^{\infty} N_{v0} \exp\left[\frac{E_v - E_{vt}}{E_{v0}}\right] \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left[-\frac{(E_D - E_{DM})^2}{2\sigma^2}\right] dE_{vt}$ (all the WB are converted)

Performing integration and taking $E_v \equiv 0$ yields the famous defect pool model that relates equilibrium density of states (DOS) among WBs, DBs , electronic free carriers and the mobile interstitial hydrogens with each other,

$$D(E_D) = \left[\frac{2}{f^0(E_D)}\right]^{\frac{kT}{2E_{v0}}} P\left(E_D + \frac{\sigma^2}{2E_{v0}}\right)\gamma \qquad (2.10\text{-a})$$

with $\gamma \equiv \frac{2N_{v0}E_{v0}^2}{2E_{v0} - kT}\left[\frac{H}{N}\right]^{\frac{kT}{4E_{v0}}} \exp\left[-\frac{\left(E_{DM} - \frac{\sigma^2}{4E_{v0}}\right)}{2E_{v0}}\right]$ (2.10-b)

In the light of this information, the hydrogen contribution is two fold: (i), the hydrogen atom, mobile under various external stress (such as illumination, annealing, etc…) might be bound in a weak bond (WB) and then create an isolated DB defect; second, it decreases the defect chemical potential (actual defect formation energy) by providing extra entropy, S_H (= $S_H = -k\ln\left[\frac{D(E_D)}{[H]P(E_D)}\right]$), since there are several orders more hydrogen sites than DB defects (in other words, a DB defect at energy E_D gains an extra entropy from those hydrogen sites that would also form a DB defect at the same energy E_D).

As during the film growth at the temperature interval of 200-300 ˚C, the amphoteric nature of a neutral DB (i.e., it can release its electron or capture an extra one) leads to three different defect distributions [18,19] (see fig. 2.5) (negatively charged one, located below Fermi level E_F, neutral one around E_F, and positively charged one above E_F). Note that all effects affecting E_F might create instability of DB defects [20]. The effect of these various charge states is twofold also in the calculation of defect chemical potential: first the average energy $<E_D>$ of the electron on the DB defect should be considered. In other words, the mean energy $\langle E_D \rangle$ of the electrons in the DB states may be expresses as follows:

$$\langle E_D \rangle = E_F f^+(E_D) + E_D f^0(E_D) + (2E_D - E_F + U) f^-(E_D) \qquad (2.11)$$

with f^+, f^0 and f^- are the probabilities of the DB defect in each charge state[21];

$$\left(f^+\right)^{-1} = 1 + 2\exp\left[\left(E_F - E\right)/kT\right] + 2\exp\left[\left(2E_D - 2E + U\right)/kT\right] \qquad (2.12\text{-a})$$

$$f^0/f^+ = 2\exp\left[\left(E_F - E\right)/kT\right], \qquad (2.12\text{-b})$$

$$f^-/f^+ = \exp\left[\left(2E_D - 2E - U\right)/kT\right] \qquad (2.12\text{-c})$$

with $f^+ + f^- + f^0 = 1$.

Second, the extra entropy, S_e $\left(= -k\left[f^+ \ln f^+ + 2f^0/2 \ln f^0/2 + f^- \ln f^-\right]\right)$, gained by different possibilities of charge states should be taken into account [22]. Consequently, considering the effect of both the hydrogen and various charge states, the chemical potential of DB defect at E_D becomes [18]:

$$\mu_D\left(E_D\right) = \left\langle E_D \right\rangle - TS_e - TS_H \qquad (2.13)$$

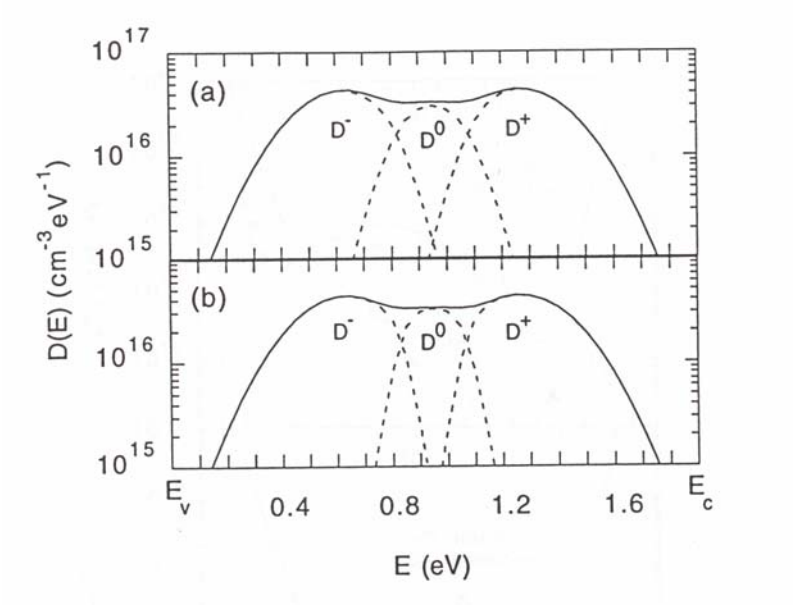


Fig.2.5 Density of each charge component within the gap at T=200 °C (a) and 40 °C (b), respectively. From: [12].

At the growth temperature, there is an immediate equilibrium among WBs, DBs, electronic free carriers and interstitial hydrogen with each other. At room temperature, the above situation is almost frozen-in with three different defect

distributions within the gap (see 2.5), the charge state of each one can be changed from positive to neutral, from neutral to negative by changing E_F or by making electronic transition from valance to these localized states in spectroscopic characterizing techniques (such as DLTS). Keeping in mind the shift in energy of negatively charged DB distribution due to the positive correlation energy of its pair of electrons; the above cited three different distributions (i.e., D_e, D_h and D_z) become six different distributions ($D_e^{+/0}, D_e^{0/-}, D_z^{+/0}, D_z^{0/-}, D_h^{+/0}, D_h^{0/-}$) covering the whole energy gap [18] as shown in fig.2.6. If the amount of DB density is above 10^{18} cm^{-3}, like a-SiCx:H films, the hopping electrical conductivity seems highly probable at any energy level of its energy gap.

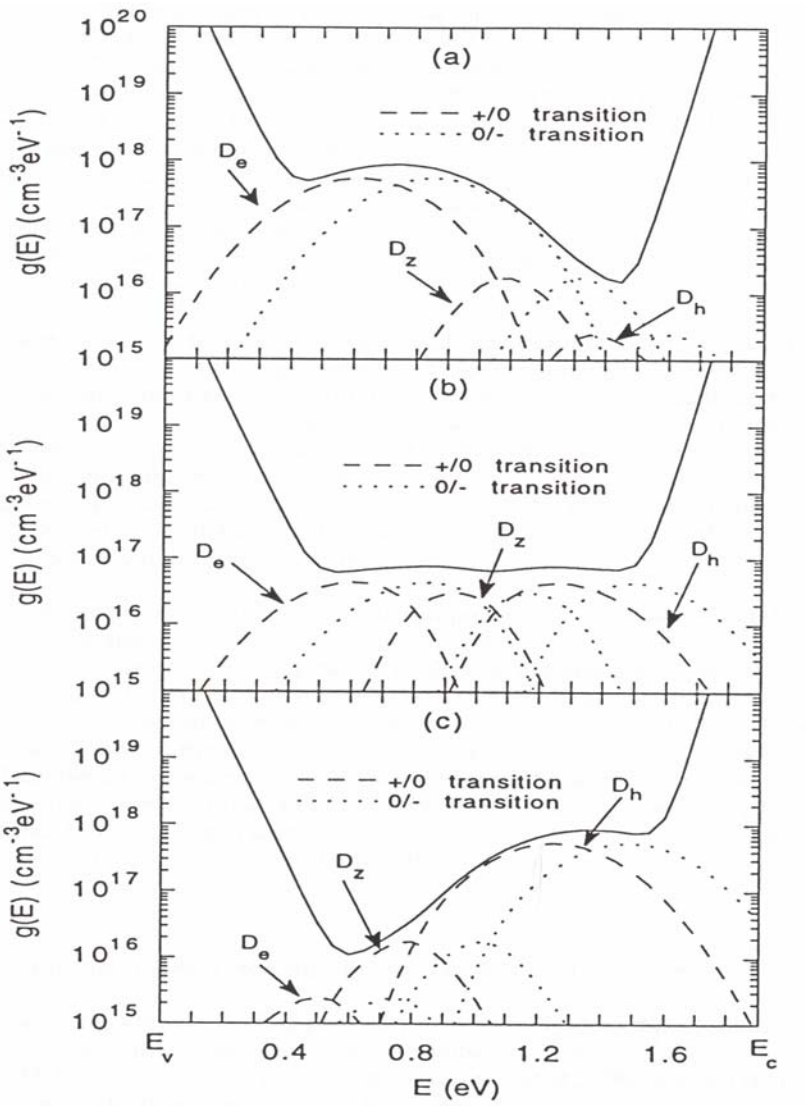


Fig.2.6 Density of states splits into +/0 and 0/- for (a) n type, (b) intrinsic and (c) p type a-Si:H. From: [12].

2-2 Electronically Active Defects in a-SiNx:H Thin Films

Apart from Si-H bond [23] and nitrogen dangling bonds [24], nowadays there is a consensus that silicon dangling bonds [25-26] (denoted by K^0) are responsible for charge trapping in a-SiNx:H film. In detail, K^0 center is comprised of an unpaired electron on a silicon atom bonded to three nitrogen atoms in stoichiometric and N-rich (x=1.6) a-SiNx:H alloys.

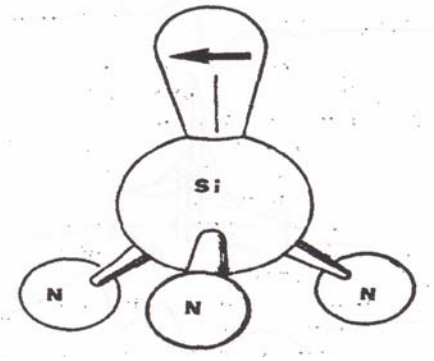


Fig. 2.7 Schematic view of the K center, an unpaired electron highly localized on a silicon atom bonded to three nitrogen. From [9].

These centers are amphoteric and paramagnetic when neutral and is detectable with the electron paramagnetic resonance (EPR). A change in spin and charge state leads to diamagnetic positively and negatively charged Si sites, denoted by K^+ and K^- centers, respectively. It is believed that a-SiNx:H film consist of positively and negatively charges Si sites.

Upon application of external agent such as UV-illumination and charge injection (discussed in chapter 6), these centers turns out to be K^0 centers and change the charge states from positive to negative and/or negative to positive, depending on the gate polarity of applied gate bias, with the following reaction, respectively:

$$K^+ + K^- + h\upsilon \rightarrow K^0$$

$$K^+ + 2e \rightarrow K^-$$

$$K^- + 2h \rightarrow K^+$$

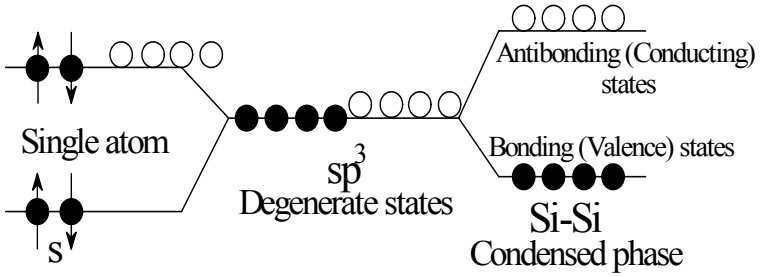
Indeed, the chemical reactions above are tested by Kanicki et all combining EPR, capacitance voltage and charge injection measurements on a-SiNx:H films and suggested that UV light simply cause an optical rearrangement of spin and charge states. In addition, they correlate the decrease in the paramagnetic K^0 center concentration with the increase in positive (negative) charge density in both UV-illuminated and virgin a-SiNx:H film. These discussion on a-SiNx:H is also the base of our charge carrier injection model discussed in chapter 6.

2-3 Recapitulation of localized defects in a-SiCx:H Thin Films

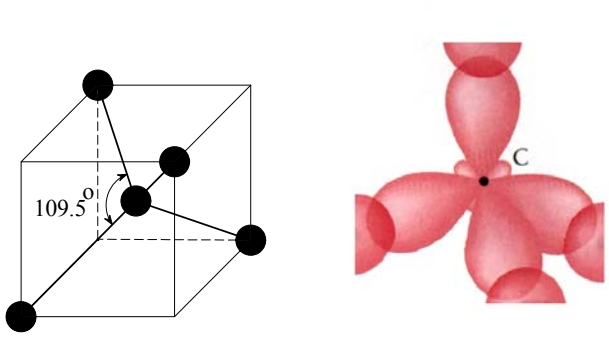
Let us outline and resume the eventual main points on the defect chemistry expected within a-SiCx:H thin film which may be considered also as Si, C and H alloy. In order to analyze the structure of a-SiCx:H alloy, both a–Si:H and a-C:H structures should be in mind. The properties of this alloy change more or less as a function of the values of x from x=0 (pure a-Si where tetrahedral sp^3 like hybrid covalent σ type bonding is dominant) to x=1 (pure a-C where all three types of covalent two center hybrid σ-like sp^3, sp^2, and sp^1 bonding coexist together with π-like relatively multicentered bonding [27].

In this respect, for $x < 0.5$, both Si-Si homonuclear bonds, and Si-C heteronuclear bonds, for $x \approx 0.5$ mainly Si-C heteronuclear bonds and for $x > 0.5$ both Si-C and the above cited different types homonuclear C-C bonds are expected.

Parallelly to these possible bonding changes on passing from Si-rich ($x<0.5$) to C-rich ($x> 0.5$) alloy, both the configuration and the amount of hydrogen and localized defects are different [27-32]. In other words, for silicon rich films, ideally the whole structure might be considered as a sp^3-like σ-bonded network (4 coordinated with only bond angle and bond length distribution). This ideal structure is too much strained, even hydrogenation could not decrease sufficiently the average coordination number for complete relaxation; the elastic strain is relieved by unavoidable generation of dangling bonds (DB) throughout the structure.



(a)



(b)

Figure 2.8. (a) Bonding orbital diagram of a-Si. Note that a-Si is tetrahedrally coordinated by four neighboring silicon atoms; the eight sp^3 hybridized orbitals are split into four bonding and antibonding orbitals, yielding the localized states, (b) tetrahedral structure of sp^3 hybridized silicon and carbon atoms

For a bit more clarity, let us revise the DB generation in a-Si:H: since each atom is free to move in 3 dimensions, fixed bond lengths and bond angles can be achieved only if $N_c(\bar{z}) \leq$ degree of freedom (3) with $N_c(\bar{z}) = (z/2 + z(z-1)/2)\bar{z}^2/2$ where the first term in parenthesis is the number of stretching and the second one is the number of bond bending, respectively. In this respect, a-Si with $z \approx 4$ is overconstrained (or over coordinated) network. The alloy of pure a-Si with hydrogen in an 10 % amount (since the best films have only 10 % of H) yields z $(= 4(1-x) + x = 4 - 3x)$=3.7 that states that a-Si:H still remains relatively overconstrained.

For carbon rich films, the eventual relaxation should be different from that of the above outlined one [27]. Let us outline the main points to be more understandable. It is known analogously to the organic molecules that the carbon element is able to build all sp^3 (tetrahedral or spatial), sp^2 (trigonal or planar) and to a lesser amount sp^1 (divalent or linear) hybridized σ-like C-C two center bondings in the formation of carbon based structures depending on the local atomic configuration and production conditions.

In the first stage of hybridization process, one of the two electrons at $2s^2$ is excited to the empty $2p_z$ state (sp^2 hydridization); in the second stage of linear combination of the $2s^1$ and $2p_x^1$, $2p_y^1$ $2pz^1$ orbitals form the hybrid orbital (sp^1 hybridization) (see fig.2.9). The driving force behind the planar and linear configurations of sp^2 and sp^1 like σ-bonding respectively is the coexistence of π-bonding. Omitting the less probable sp^1 case, the π-bonding, formed by sideway overlapping of unhybridized free atomic p_z orbitals perpendicularly on either side of C-C sp^2 orbitals together with the identical configuration of all 3 sp^2-like σ-bonds, favors the planar structure of sp^2-like trigonal bonding connected with 120° angle (depicted in fig.2.10-a).

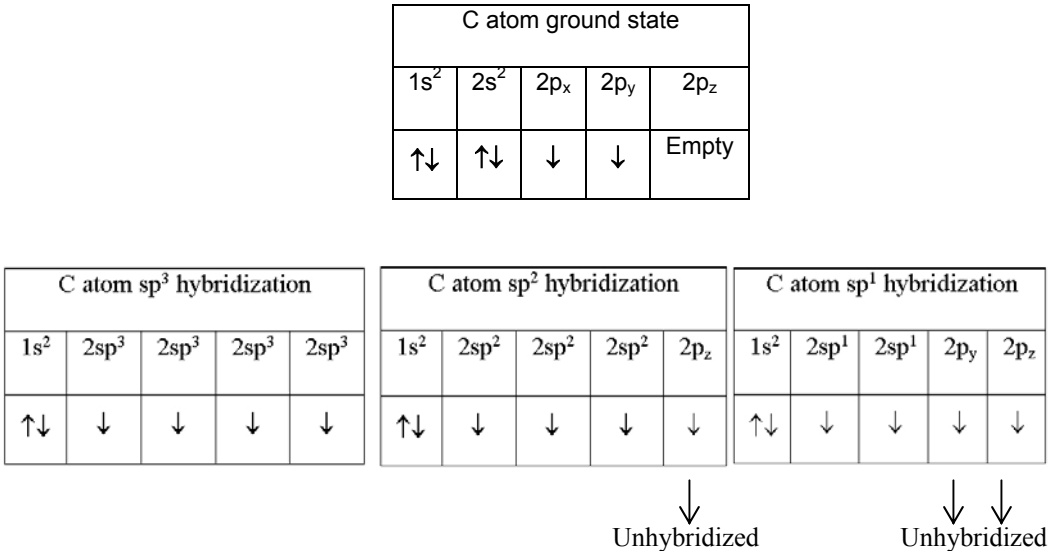


Fig. 2.9 Sp^3 (tetrahedral), sp^2 (trigonal/or planar) and sp^1 (linear) hybridization of the carbon atom.

This spatial correlation leads to planar clusters of hexagonal rings (graphitic structure, see fig.2.11-a). In there, electron probability distribution above and below the ring are continuous and these six electrons belong to the structure as a whole (i.e., not to any particular pair of atoms). The electrons in these extended π-orbitals are delocalized (or multicentered) within each such cluster and they are, by the way, weakly bound compared to σ electrons. The stability of the structure increases by increasing the number of rings taking place in the cluster [33]. On the other hand, for sp^1 case, the existence of two unhybridized p_y and p_z orbitals of a site should lead to linear structure along the interaction of the mutually perpendicular y and z planes along which p_y and p_z are lying respectively (see fig.2.10-b). Returning to the relaxation phenomenon within a carbon rich a-SiCx:H films, the interpretation of σ-bonded and π-bonded networks should be in mind. In other words, σ-bonded network (as in a-Si case) might have tendency to relieve strain by bond angle/bond length distortions with generation of randomly distributed dangling bonds while the π-bonding (through interaction between adjacent π-orbitals) places a strong constraint on the network of sp^2 sites to keep them as planar sheet of 6-folded rings. As a result of these two competing tendencies, the eventual strain is expected to be relieved by breaking π bonds beyond a certain size rather than σ-bonds since the π bond breaking requires less energy. The boundary regions of π bonded islands should be disordered tissue of sp^3 sites; in other words, the film might be considered as a two phase structure, a relatively more conductive first phase of sp^2 based π-bonded clusters embedded in a relatively more resistive second phase of sp^3-bonded disordered matrix. . Electrical conduction might be mainly limited by the matrix region with relatively larger energy gap which might constitute barrier against the motion of π-electrons confined within the graphitic clusters with relatively smaller gap $\left[energy\ gap \propto \left(\frac{1}{cluster\ size} \right)^{1/2} \right]$ [27,34-36]. In other words, the electrical conduction between more or less distant graphitic clusters might be by hopping through localized states or by tunneling respectively (will be discussed elusively in chapter 6).

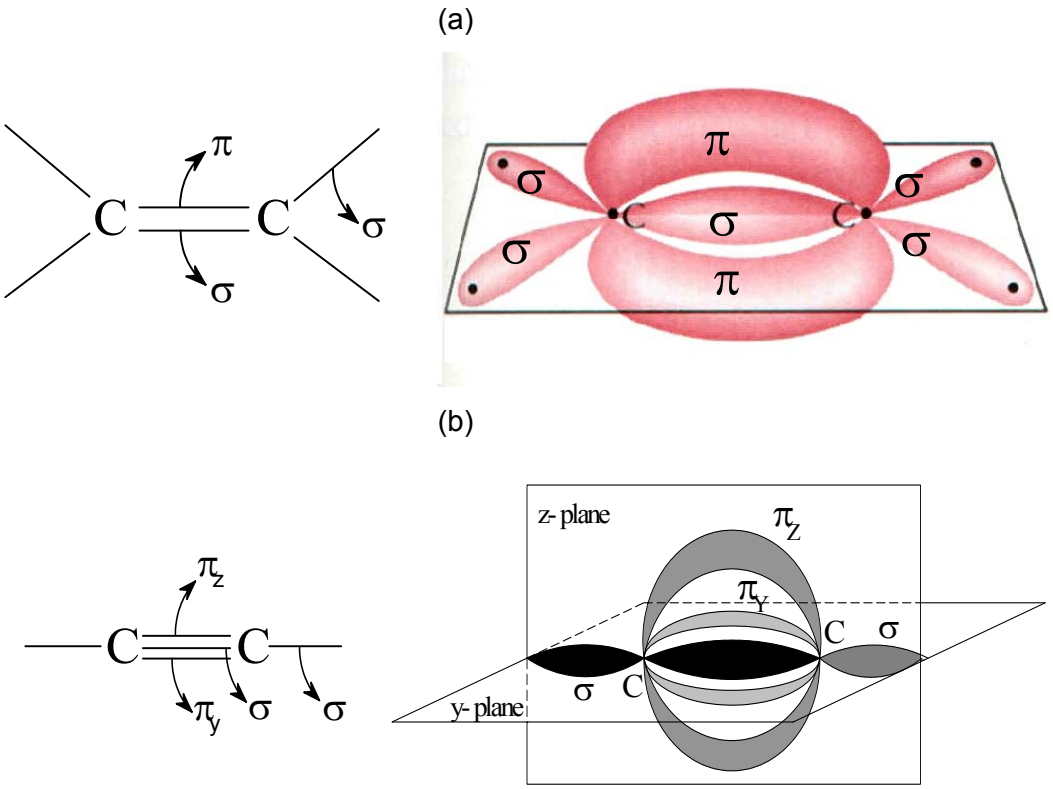


Fig 2.10.(a) The structure of sp^2 hybridized carbon atoms and σ and π bonds. Note that 3 planar sp^2 –like σ-bonds are formed together with an unhybridized free or delocalized p_z orbitals, perpendicular to the plane of the 3 sp^2 orbitals, available to form the subsidiary (produced by sideway overlapping of p_z orbital) π bond with other atoms. (b) Schematic representation of triple bonded (sp^1) hybridized carbon atoms

It is expected that hydrogenation encourages sp^3 bonding structure over sp^2 one by transforming the hydrogen unsaturated $H_2C{=}CH_2$ configuration into a hydrogen saturated $H_3C{-}CH_3$ one and then it dismantles the relatively larger graphitic clusters into smaller size one. Consequently, on the contrary of Si rich a-SiCx:H film, the hydrogenation of carbon rich film lowers the defect density, neither by saturating dangling bonds (DB) nor by more tightly binding the valence electrons (H–C on sp^3 site and H–C on sp^2 site have almost the same binding energy), but by reducing the graphitic cluster size by promoting sp^3 over sp^2 bonding and thereby increasing defect creation energy (due to the increased energy gap) and decreasing their thermodynamic probability [27].

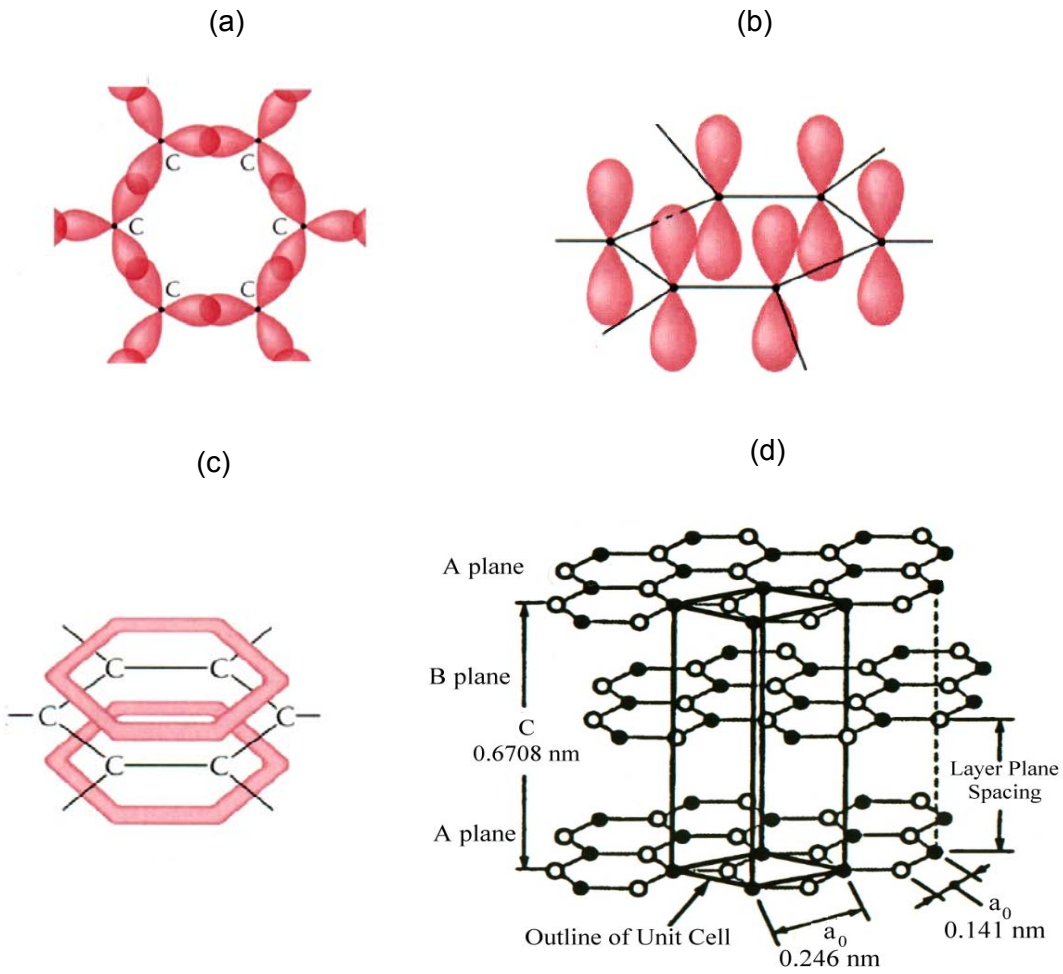


Figure 2.11. a) Hexagonal rings formed by the combination of three sp^2 hybridized carbons, b) and c) The formation of π bonds, d) The structure of graphite.

In carbon rich a-SiCx:H film, although the graphitic clusters (and their boundaries) containing σ and π bonding, have the possibilities of generating both σ and π coordination defects, the π defects are expected to be dominant due to their lower creation energy and they might take place around the Fermi level (or halfway between bonding π and antibonding π^* states) [27,36]. The coordination defect states within the tetrahedrally sp^3 bonded matrix, i.e., σ-like dangling bonds (DB) at both carbon site (C_3) and silicon site (Si_3) may be simultaneously present. As the electron is more tightly bound to the carbon site than silicon site such that their corresponding energy levels $E_{C_3} < E_{Si_3}$; charge transfer from neutral Si_3 site to neutral C_3 might be possible, the energy level of the resulting Si_3^+ and C_3^- centers should be located on either side of the Fermi level.

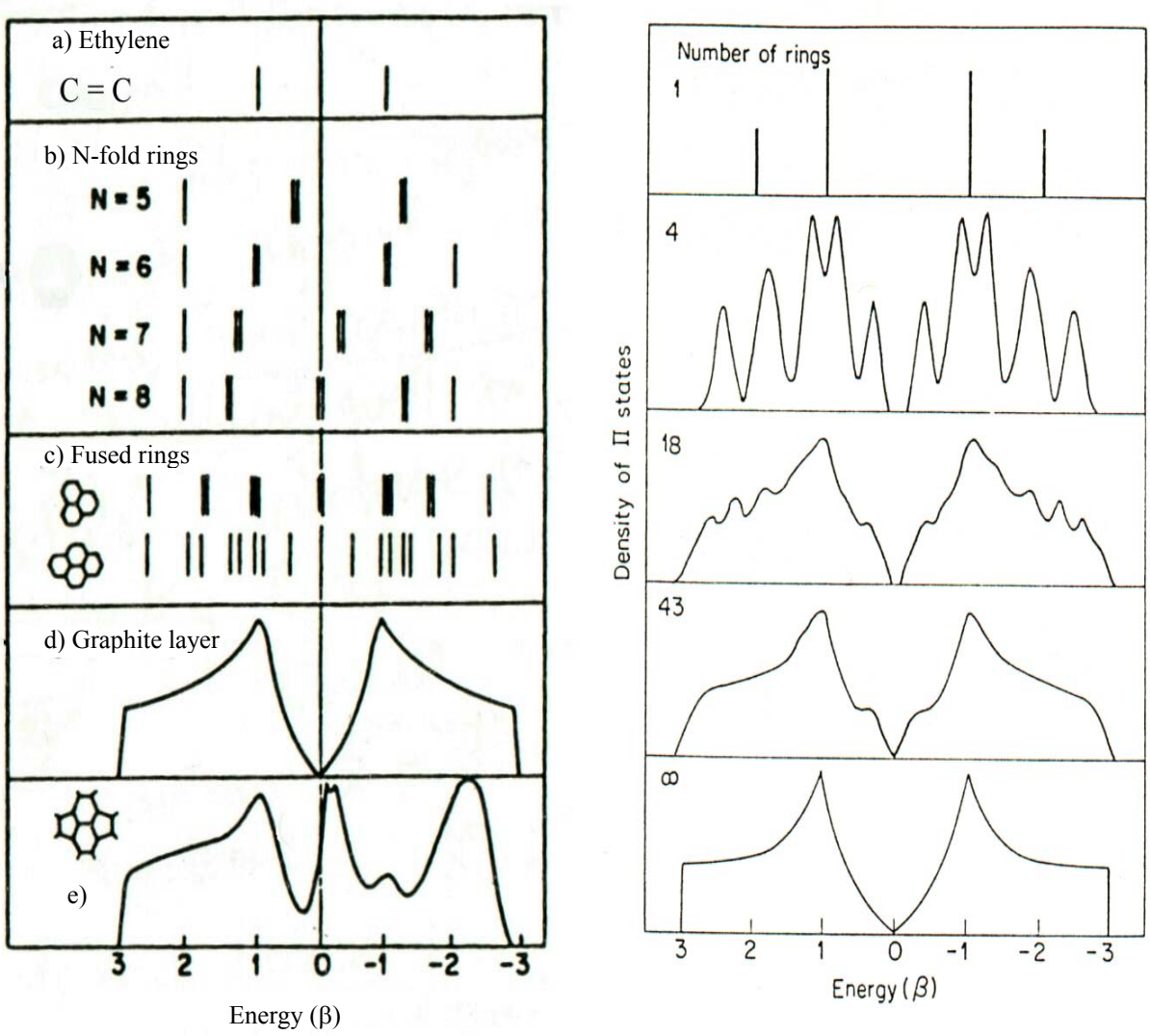


Figure 2.12 π state spectra of a) ethylene, b) planar rings with N=5-8, c) three fused rings, and four fused six-fold rings, d) single graphite layer, e) layer containing two five-fold and two seven-fold rings. II) π band density of states for compact clusters of fused 6-fold rings of increasing size [34-36].

The coordination defect states within the tetrahedrally sp^3 bonded matrix, i.e., σ-like dangling bonds (DB) at both carbon site (C_3) and silicon site (Si_3) may be simultaneously present. As the electron is more tightly bound to the carbon site than silicon site such that their corresponding energy levels $E_{C_3} < E_{Si_3}$; charge transfer from neutral Si_3 site to neutral C_3 might be possible, the energy level of the resulting Si_3^+ and C_3^- centers should be located on either side of the Fermi level.

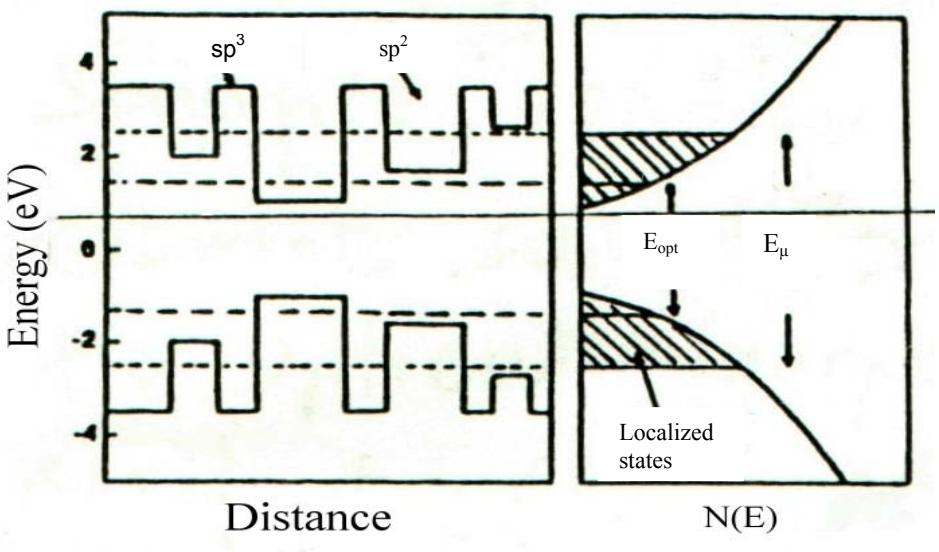
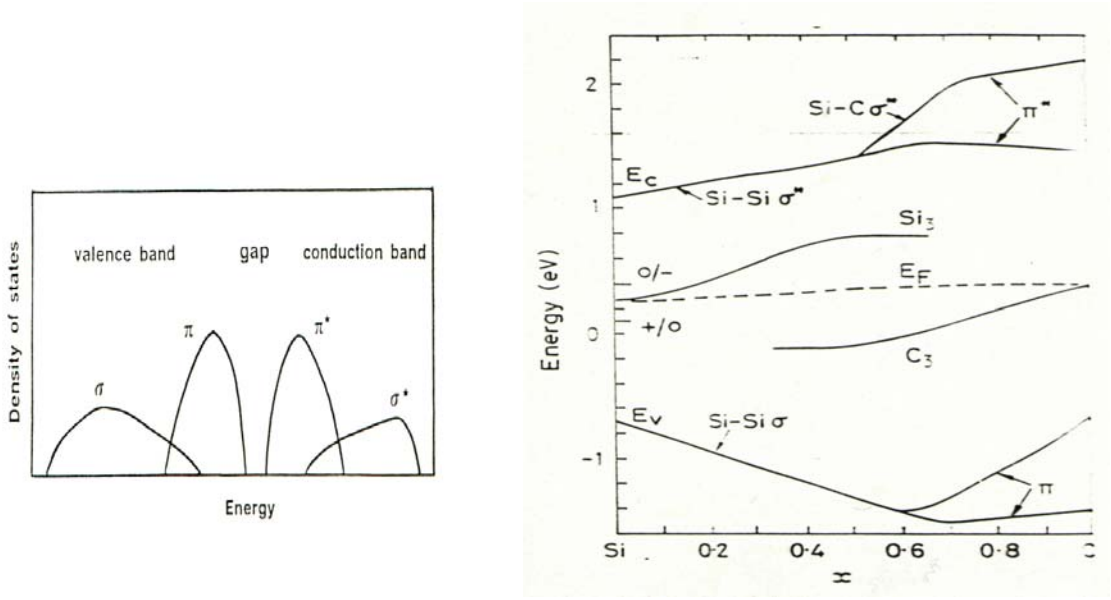


Fig.2.13 Schematic band diagram of carbon rich a-SiCx:H film [34,36].

This picture is too simple since DB energy is site dependent, instead of discrete single energy level, Gauss-like distributed density of states (DOS) within the gap is expected [15,16]. Moreover, the DB creation mechanism should be roughly revised in the light of the famous defect pool model [14,17,18].



(a) (b)

Fig 2.14. (a) Schematic electronic band structure of carbon rich a-SiCx:H, (b) The band tail variation of a-Si_{1-x} C_x and eventual defect levels. From []34-36].

CHAPTER 3

MASK MAKING AND PHOTOLITHOGRAPHICAL TECHNIQUES FOR VLSI

3.1 Introduction

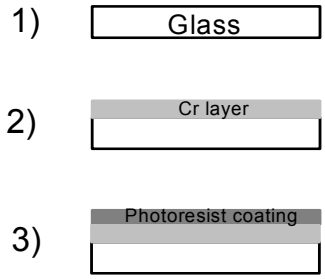
Many of the technologies that have enabled advances in miniaturazition were first developed for microelectronics and allow both lateral and thickness control in the creation of strucutures. The same processes that have allowed for decrease in size also allow parallel production of many devices. Thousands or millions of transistor or other devices can refashioned simultaneously on one chip the size of thumbnail, and many chips preprocessed at the same time on one wafer. The key steps in the process of creating these structures are; lithography and pattern transfer. Integrated circuit fabrication techniques all rely on lithography. The basic process involves covering and object with a thin layer of material that can be patterned but will resist subsequent processing and protect the material underneath. Photolithography is the most widely used form of lithography and is likely to continue to be so for the near future. To clarfiy the the point, the following discussion are made.

3.2 Mask Fabrication

It can be defined as the process of transferring geometric shapes (≡"patterns"≡ parts of a circuit) from a mask to the surface of Si wafer. In this process, there are two stages; (i) fabrication of masks, (ii) pattern transfer from the mask to Si wafer surface.

Photo-mask fabrication

UV-Visible light transparent glass plates are used for photomasks. Glass plates are coated with Cromium layer (hard mask) or emulsion (≡ light sensitive, becoming opaque after illumination). Let us discuss how a desired pattern (or reticle or die) can be obtained on a Cr coated glass:



There exist various sorts of photoresist (PR). The conventional PR is a three component materials, consisting of the ; (a) matrix material, (b) sensitizer and (c) solvent.

(a) matrix material (≡ resin): it forms the bulk of the PR, it is inert to the radiation but it provides the mechanical properties (thickness, flexibility, adhesion, etch resistance of the PR film).

(b) Sensitizer (≡ inhibitor): it is photoactive component. The molecules of this component under radiation (in the range 2000-4500 Á) are broken (≡photo scission). Therefore, this photochemical reaction changes the solubility of the PR film in an appropriate solution called developer. As a result, the regions of PR exposed to the radiation become soluble in the developer whereas the non-radiated regions remain intact (≡ resistant) in the developer. The sensitizer, being a “dissolution inhibitor” before illumination, becomes a dissolution enhancer after illumination.

(c) Solvent: it keeps the photo-resist in the liquid state until it is applied to substrate which has to be processed (it is volatile).

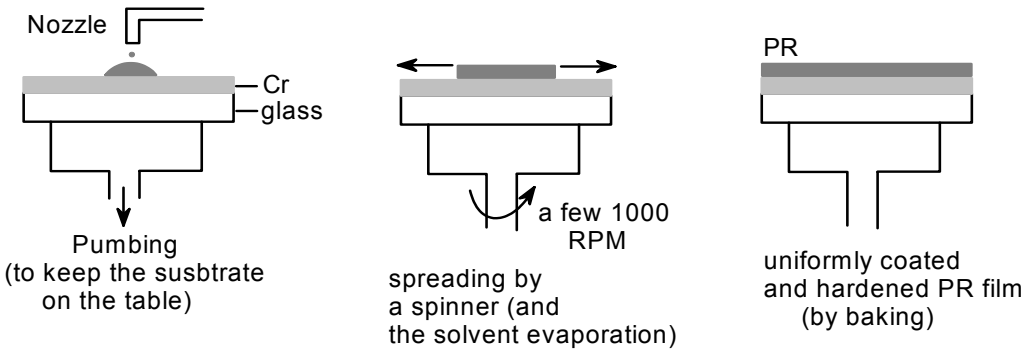


Fig.3.1 Coating of PR on susbstrate.

Note that PR may be either positive (+) or negative (-) and their effect was shown below;

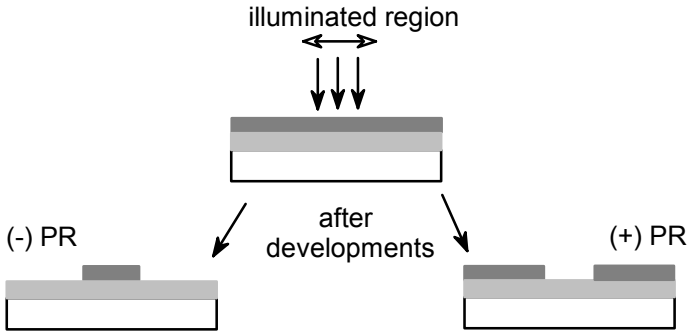


Fig.3.2 Effect of (+) and (-) PR

However, the higher resolution capabilities of (+) PR renders it the exclusive choice for very large scale integrated (VLSI) circuits.

4) pattern (or reticle or die) generation on the PR coated sample: pattern generation is to reduce any image to set of rectangles each specified by a height (H), and width (W), by X and Y center coordinates and by an angle θ relative to the coordinate axes. Combo Pattern generator at hand is used to produce a pattern on the PR coated sample to fabricate the mother mask and then using utility of image repeater (IR) of Pattern Generator, final mask pattern is obtained. It uses Hg arc lamp as UV-light source and its spectrum is given in fig.3.3.

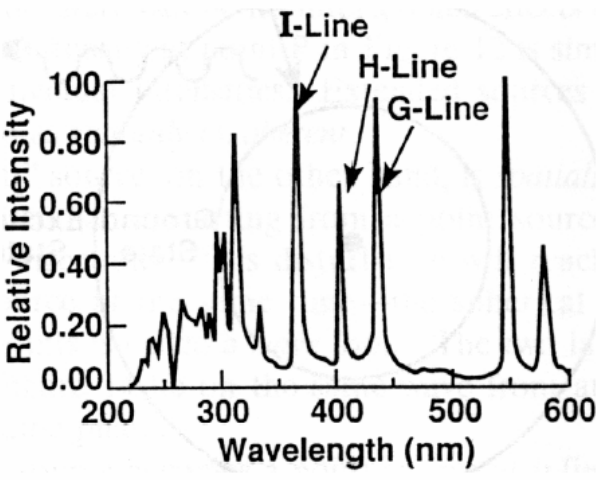


Fig.3.3 Hg arc lamp spectrum

Pattern generator uses H (405 nm) and G (436 nm) lines on Cr coated glass but E (546 nm) line is applied on emulsion type one. The pattern generator produces 10X reticles created by a photo-composition process utilizing a variable aperture assembly and sequentially exposing discrete rectangles on a sensitized plate (either Cr or emulsion type). The configuration of the image is determined by digital design information provided on 9 track magnetic tape. The reticles produced by the pattern generator are used in the manufacture of electronic integrated circuits.

The pattern generator camera is the basic electromechanical photographic component of a staging system. The pattern generator accepts the controller commands and produces a reticle image by progressively exposing a sensitized plate to a light source. The exposure is made through a rectangular aperture, the size and angular rotation of which are controllable. The sensitized plate is vacuum-clamped to the movable X-Y stage assembly, which is precisely positioned under the camera.

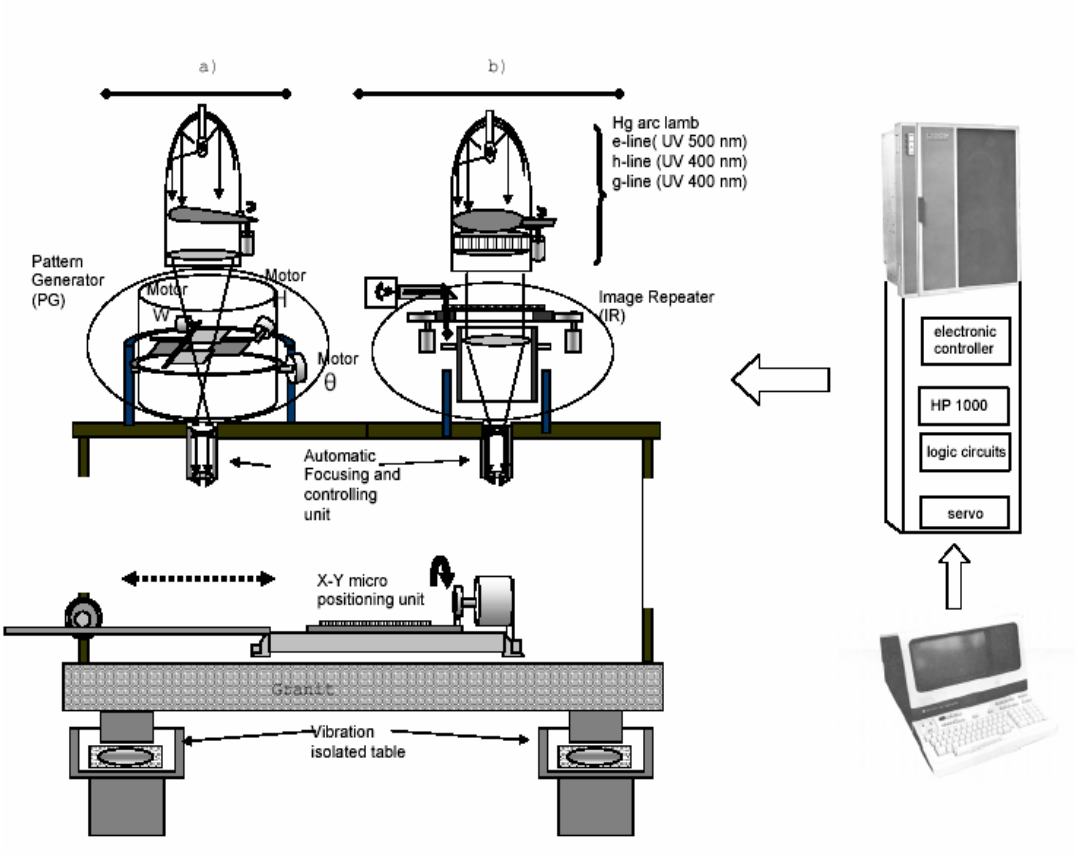


Fig.3.4 Schematic illustration of Pattern Generator.

The placement of each exposure on the plate is achieved by moving the stage underneath the aperture turret. The stage moves along the X-axis, parallel to the short side of the granite block. One side of the stage rides on the Y-segment of the stage or gantry, which moves along the Y-axis, parallel to the long side of the granite block. Both segments glide on frictionless air bearings.

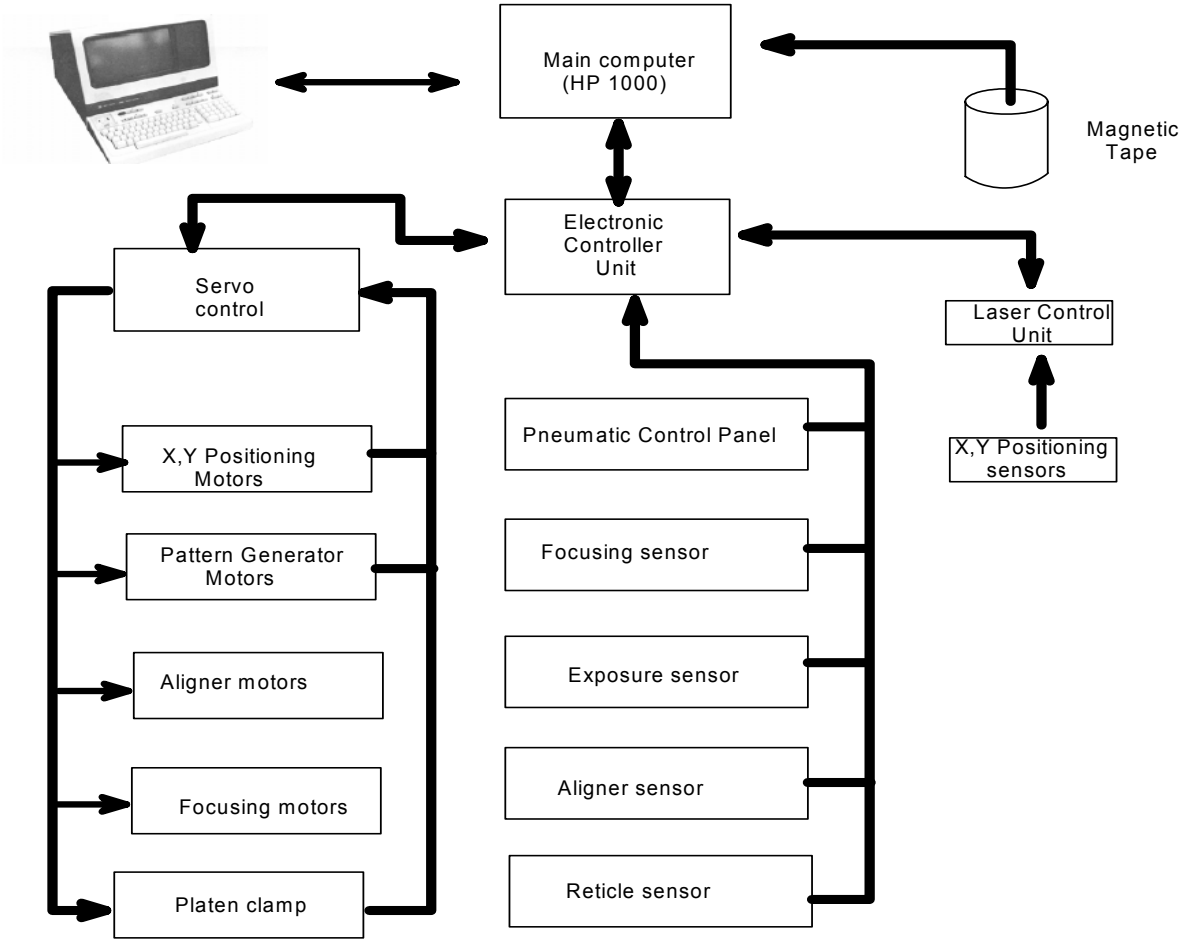


Fig.3.5 Schematic view of electro-mechanic control of Pattern Generator

The size of the aperture in terms of height (H or L or V) and width (W) of the opening is determined by the position of two sets of blades in the object plane of the pattern generator camera. Each set opens symmetrically about the optical axis to achieve the dimension commanded by the controller. One pair of blades establishes the length (distance along the Y-axis at 0 degree angle). The other pair similarly establishes the opening width. The aperture “image” is projected through 10X

reducing lens to the sensitized plate so that final size agrees with the commanded dimension.

The angle at which the rectangular image is placed on the plate is determined by rotation of the turret on which the aperture blades are mounted. The zero reference for rotation is the centerline between the width blades, parallel to the Y-axis. Rotation range is 0 to 90 degrees counter-clockwise as viewed above the turret; therefore, at the 0 degree position the width blades are parallel to the Y-axis, and at the 90 degree position the width blades are parallel to the Y-axis (shown in fig.3.6).

In addition to the two pairs of variable aperture blades and rotating turret, the camera assembly contains an automatic gauge focusing system and light source. The light source assembly contains the lamp, lamp box, light condenser and exposure control circuits.

FUNCTIONAL DESCRIPTION

The pattern generator is used to produce precision photo-masks for the semiconductor industry. The specific pattern to be constructed is described by a series of machine commands contained on magnetic tape. The final product is an image of the pattern ptohographically produced on glass.

The pattern is composed of rectangular elements; however, the very large number of elements which may be specified on the magnetic tape input allows a limitless range of complex patterns to be produced. The pattern generator automatically reads each sets of specifications for an elementary rectangular images, positions the glass with the precision of its twin laser interferometers, and adjusts its aperture to these values. When all of these conditions are met, a flash occurs which exposes the rectangular image on the photo-sensitive plate (see fig.3.6).

Because of the bearing suspension system, this precision operation is fast-speed of 50 flashes per second have been achieved. A pattern consisting of tens of thousands of flashes can typically be produced in less than an hour.

The glass blank accommodated by the machine can vary from 2 by 2 inches to 8 by 10 inches; the typical product is produced on a 3 by 3 inch or 4 by 4 inch square blank.

The size of the exposed area is established by dimensional length and width commands. The angular orientation of the rectangle is similarly controlled through 90 degrees of rotation. The placement of the rectangle on the sensitized plate is controlled by dimensioned commands of stage movement in the X and Y axes. Fig 3.6 shows how the component images are used to construct a simple pattern from several exposure rectangles.

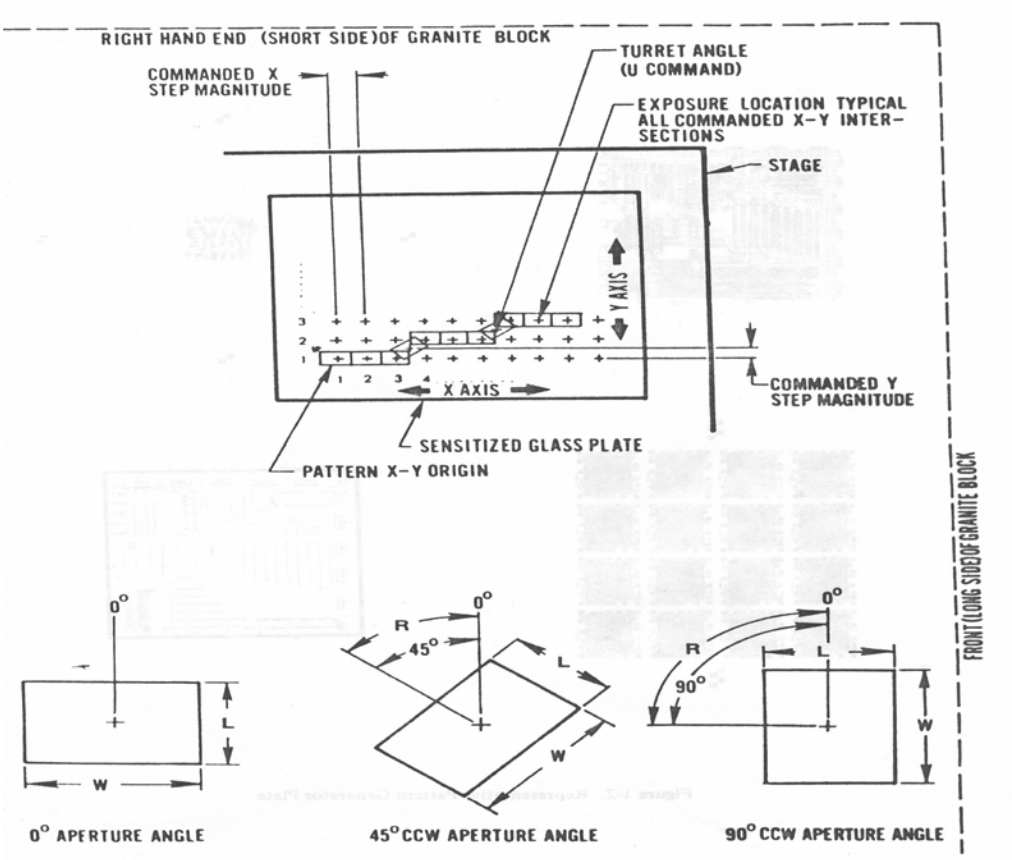
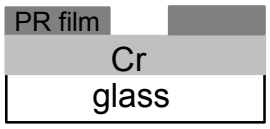
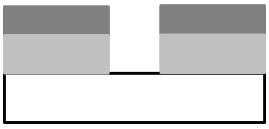


Fig.3.6 Image structure of pattern.

The pattern generator creates a circuit pattern in accordance with the tape recorded data that may be checked and verified before the process begins. Through the terminal, the operator can insert variable commands, dimensions, etc. The controller processes these commands and uses them to control the equipment.

5) 

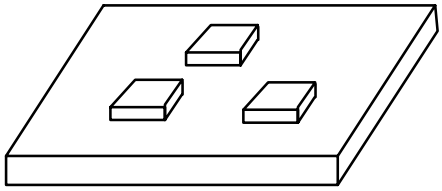
Development of PR.(The illuminated part is removed in a suitable developer(=solution)

6) 

Etching (or removal) of Cr within the PR "windows"

7) 

Removal of the remaining PR (PR stripping)



Top view: it is 10x or 5x times enlarged dimensions/final dimension.

8) Multiplication of the pattern (reticle); the previously fabricated reticle in step 7 should be regularly repeated on a new glass plate or directly on silicon wafer by image repeater (see fig.3.7) reducing the size of mother mask to 1x (by lens system).

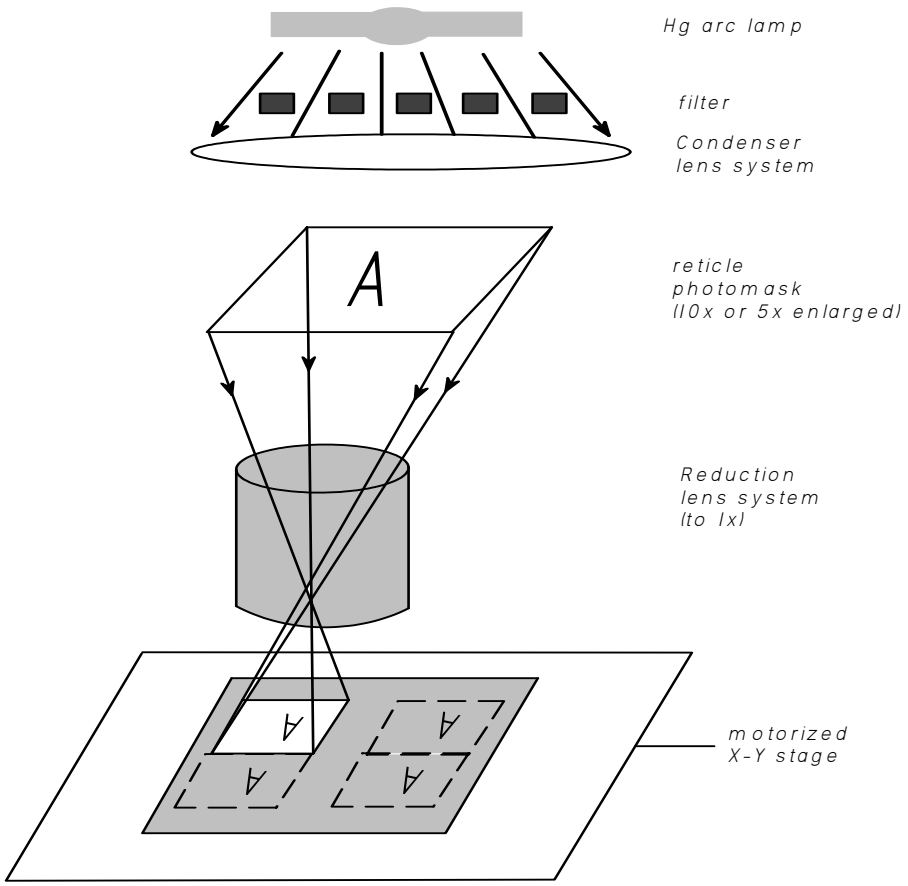


Fig.3.7 Schematic illustration of mask production via the image repeater utility of pattern generator

3.3 Resolution

The resolution of a lithographic process in a practical (industrial) sense is the ability to print (or resolve) minimum size images under conditions of manufacturing variation (≡ ability of distinguishing closely spaced objects). The resolution of a lithographic process can be limited by many aspects of process sequence; (a) hardware (optical limitations such as diffraction, lens aberrations (either geometric or chromatic)(chromatic aberration is eliminated in general by filters). Mechanical stability of the system. (b) properties of PR related chemical operations (baking, developing and etching).

The hardware resolution is imposed mainly by diffraction effects (not only by lens aberrations because here almost perfect optical elements are used in modern camera). Resolution due to the diffraction can be related via $R = 0.61\,\lambda/NA$ with NA= numerical aperture (NA=n sinθ). A larger angle of collection leads to better resolution. This benefit has a price because the depth of focus $\kappa = \pm\frac{\lambda}{2}\Big/\left(NA\right)^2$ is inversely proportional to $(NA)^2$. Therefore, one can be easily outside the focal plane due to the flatness variation of the substrate. Hence, there is a compromise between R and κ. To overcome the resolution limitation, e-beam lithography has been developed. In other words, another way to get beyond the diffraction limit of radiation based lithography is to use electrons or atoms to expose the resist. Diffraction does not limit the resolution of electron-beam lithograph because the quantum mechanical wavelengths of high energy electrons are exceedingly small. Electrons scatter quickly in solids, limiting practical resolution to dimensions greater than 10 nanometers-significantly greater than current demands of any practical technology. Electron-beam lithography has demonstrated resolution as small as 2 nanometers (0.02 microns) in a few materials. Electron beam technology, however, is limited in usefulness because an electron beam must be scanned across the entire wafer.

Photo-lithographical Processes:

The aim of (photo) lithographical processes is to be able to reproduce the pattern on mask within a film (SiO_2, a-SiNx:H) with fidelity.

The film should be removed (=etched) selectively within the resist window(s) by etching; etching could be either wet or dry:

1) wet etching: the resolution of etching process is measure of the fidelity of pattern transfer which can be qualified by two parameters; B=etch bias, A_f= degree of anisotropy=$1-\frac{v_l}{v_v}$ where v_l is lateral etch rate, v_v is vertical etch rate respectively. If v_l=0, perfect fidelity is achieved whereas for the case of $v_l \approx v_v$ bad fidelity occurs.

On the other hand, B($\equiv d_f - d_m$) represents the difference in lateral dimension between etched image and mask image. In other words, B describes the degree of undercutting (see fig.3.7). Examples of wet etchings of common materials in microelectronic fabrication environment: a) silicon, b) silicon dioxide, c) Al. a) etching solution is the mixture of HNO_3/HF in H_2O; first HNO_3 reacts with silicon to form a-SiNx:H then HF dissolves this oxide away and so on, b) for a-SiNx:H, etching solution is HF/H_2O mixture, here HF reacts with a-SiNx:H (dissolve it) but it does not attach Si itself. Etch rate would be 1000 Å/min, c) for the case of Al etching, the etching solution is H_3PO_4/HNO_3/H_2O. H_3PO_4 oxidizes the Al to form Al_2O_3 and the rest is as explained before. Unfortunately, the wet etching presents several critical problems for micron and submicron geometries although it has an excellent selectivity (= the ratio of etch rate between different materials, resist mask and underlying material (substrate)). The disadvantage of wet etching can be classified: (i) undercutting due to the isotropic etching, (ii) PR can lose adhesion in most solutions, (iii) as geometries decreases (< 1μm), the surface tension of etch solutions can cause the liquid to bridge the space between two resist stripes, etching of the underlying film is thereby precluded, iv) large volume of dangerous solution.

2) Dry (or plasma) etching exhibits viable solution to the problems encountered with wet (liquid) etching. It is almost anisotropic, has very little etch bias (undercutting). However, this dry etching has poor selectivity.

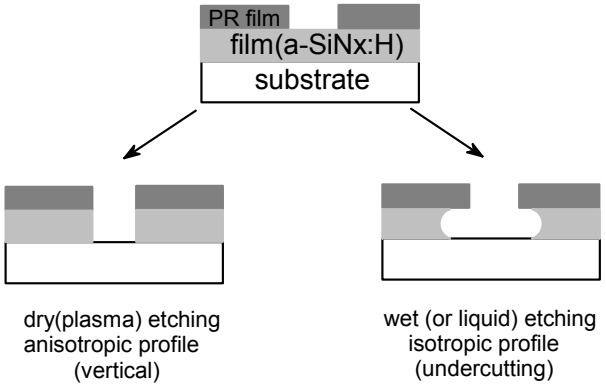


Fig.3.8 Comparison of dry (plasma) and wet(liquid) etching.

If samples are placed on grounded electrode, plasma etching or plasma deposition occurs. The chemical reaction taking place in plasma are often very complex which in general remain (“ill understood” or) unknown. However, the following reaction types may be cited: (a) excitation, (b) dissociative attachment, (c) dissociation (≡ fragmentation without ionization since ionization requires more energy), (d) ionization and (e) dissociative ionization. The role of plasma in etching (and deposition) processes is two fold (≡ a combination of chemical and physical processes): (1) creation of chemically reactive species (chemical), (2) supply of energetic radiation (≡ directional, leading to anisotropic processes). They are principally ions, electrons and photons. These radiation alter the surface chemistry. Events occurring both in the gas phase and at the substrate surface would be homogeneous type (I,ii, vi, see fig.3.9) and heterogeneous type reactions (iii, iv and v), respectively.

(i) generation of reactive species (radicals), (ii) diffusion of radicals towards the substrate surface, (iii) adsorption on the surface, (iv) reaction, (v) by product desorption (vi) diffusion of this b product from the surface into the bulk of gas phase. Note that if any of these individual processes do not occur, the overall deposition (or etching) cycle terminates.

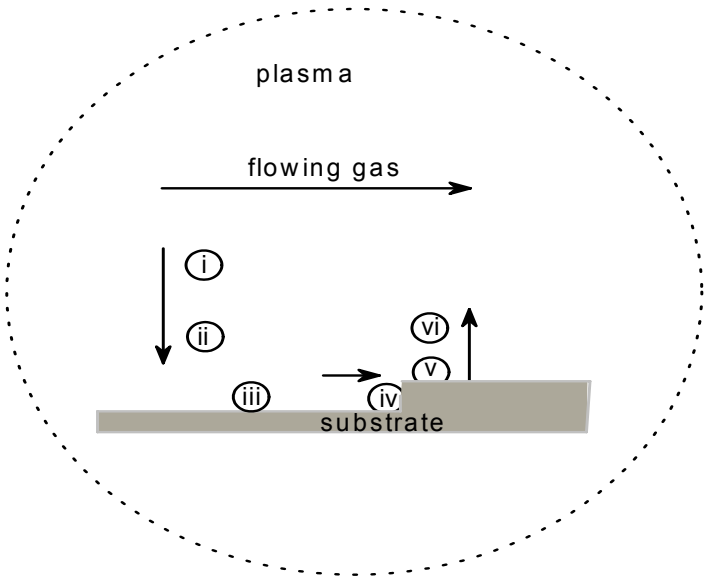


Fig.3.9 Illustration of events occurring in the plasma reactor.

3.4 PREPARATION OF PATTERN DATA ON MAGNETIC TAPE

Specification of magnetic tape:

Combo Pattern generator has a Hewlett Packard digital magnetic tape reader unit (HP 7970B). The tape unit is one of two basic types which are distinguished by the technique used to record data on magnetic tape. These recording techniques are referred to as " Non-Return-to-Zero-Inverted" (NRZI) and "Phase Encoded" (PE). There is a difference and the two techniques are not interchangeable. Hence, if a tape is written in NRZI, it must be read by NRZI tape units; likewise PE. HP 7970 is designed to write and/or read tapes using the NRZI techniques. Unfortunately, the tape unit at hand is not able to write data, only reads the NRZI coded magnetic tape. For that reason, in order to write data on a magnetic tape, another tape reader unit, HP 7974A, is used that has capable of writing/reading data recorded either NRZI or PE coded.

NRZI is written either seven or nine-track. NRZI data, for the purpose of recording on magnetic tape, is coded in one of two ways. One requires seven bits per character; the other, nine bits per character. Both of these codings include one bit for parity (a method of error detection). It is apparent that data coded in seven bit characters is written on a tape in a seven track format. Nine bits per character then requires a nine track format. Moreover, digital magnetic tapes are recorded at different densities, simply stated in terms of bytes per inch (BPI) of tape. HP NRZI tape unit support densities of 200, 556 and 800 bpi for seven track and 800 BPI for nine track. Phase encoded tapes are always recorded at 1600 BPI. Data with the mentioned density (either 800 or 1600 BPI) is written on a magnetic tape that has to have a write enable ring installed on the back of the reel. This ring, when in place, allows write operations. Moreover, as shown in fig.3.10, beginning of tape (BOT) and end-of-tape (EOT) has light reflecting tabs placed on by the tape supplier. The tape reader unit finds the beginning and end of the tape by detecting light reflected by these tabs.

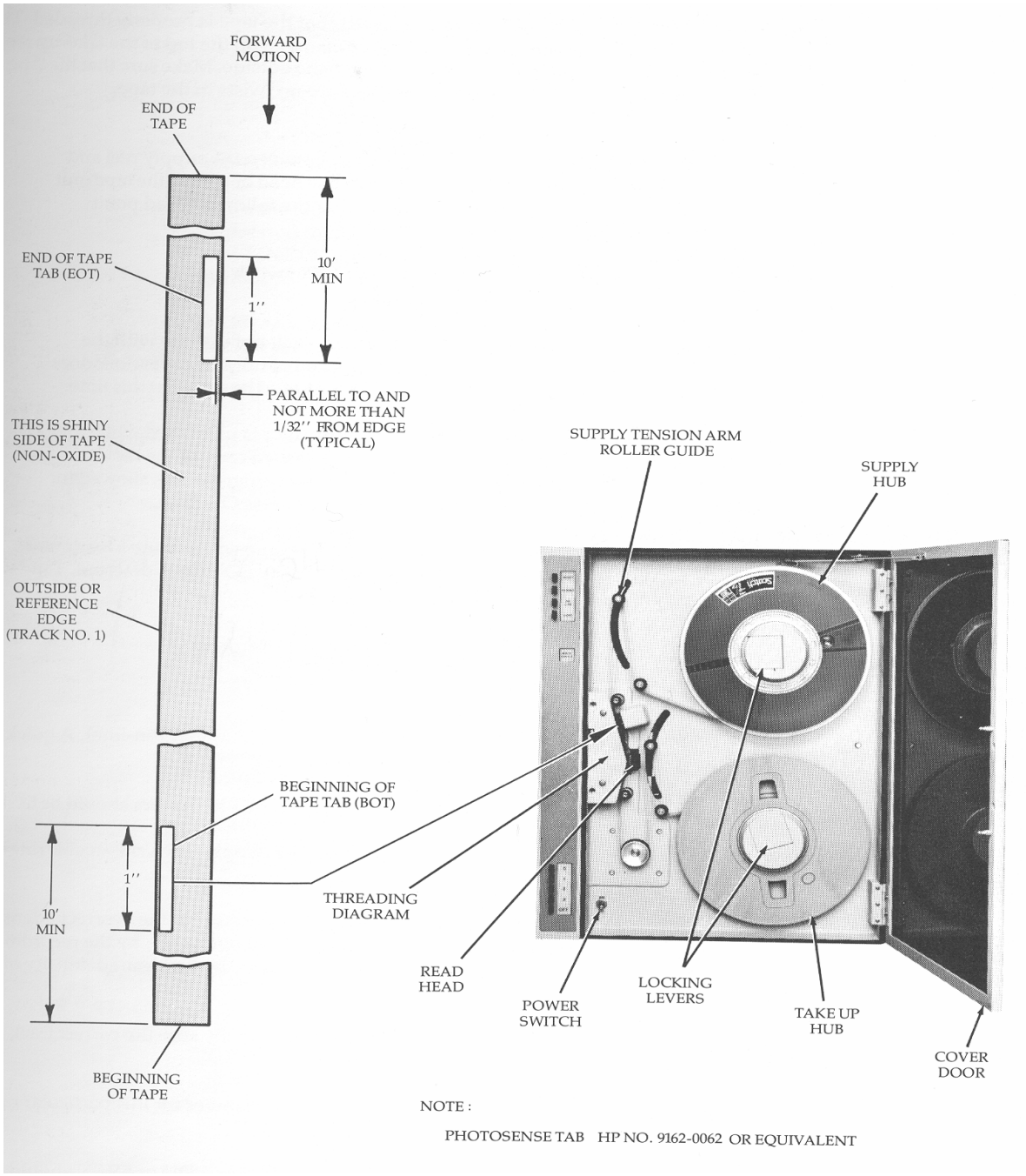


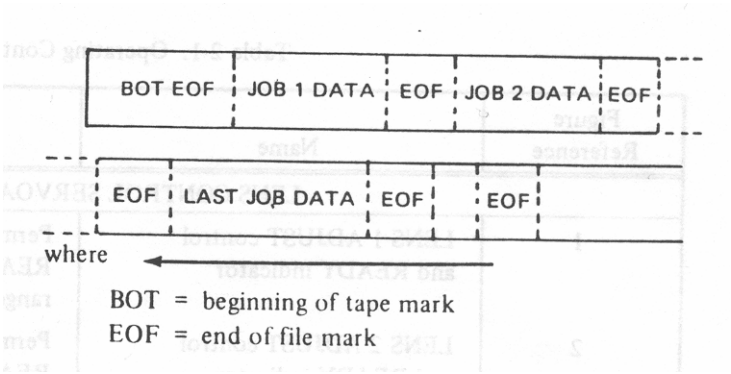
Fig.3.10 Tape threading.

PATTERN GENERATOR INPUT DATA:

The pattern produced by the pattern generator is made up of large number of individual rectangles as described above. Commands describing an individual rectangle can be entered through the keyboard or from magnetic tape. Because a

typical pattern requires thousands of such rectangles, its impractical to compose an entire pattern from the keyboard. In typical operations, nearly all rectangles are described in the magnetic tape input and the keyboard mode is used only for adding correction flashes.

A single magnetic tape will generally contain information describing several patterns. The pattern generator software can space down to a particular job, execute the pattern described and wait for the glass blank to be changed before executing another job. A magnetic tape would be organized as:



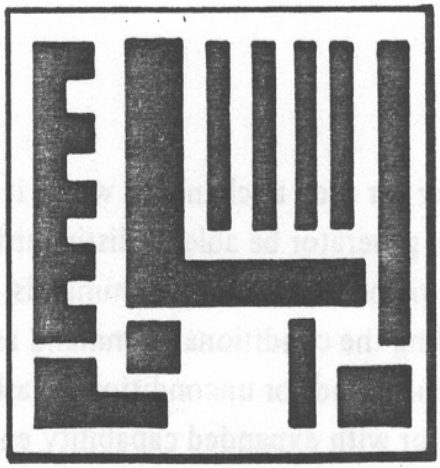
Job data are grouped into 800 character block (400 words with 2 characters per word). The fist character in the block must be start of record symbol, a cent sign (¢) when describing in EBCDIC (also known as old IBM format), or less than (<) when transcribing in ASCII format. The last valid character in a block must be end of record symbol. The standard Electromask format (see fig.3.10) requires 9-track, NRZI mode, EBCDIC tape character set. Also shown are the equivalents for recording ASCII characters on magnetic tape. Tapes must be recorded in characters that match both the hardware and software of a specific pattern generator, For compatibility with the largest number of machines, 9 track, NRZI mode, EBCDIC characters and odd parity are used. As seen in the fig.3.11, X (Y) is the X(Y) coordinate of rectangle position, W is the width of rectangle, V is the height of rectangle (vertical), U is the angular orientation of rectangle and Z(= end of job) and S(= flash command) are the control characters.

P/G Significance	Symbol	EBCDIC Image			Others (Octal)	
		Binary	Octal	Hxdec	ASCII	BCD
Start of Record*	¢ or <	01001010	112	4A	74	76
End of Record	.	01001011	113	4B	56	73
End of Job	Z	11100010	351	E9	132	31
Flash Command	S	11100010	342	E2	123	22
X-Position	X	11100111	347	E7	130	27
Y-Position	Y	11101000	350	E8	131	30
Rectangle Width	W	11100110	346	E6	127	26
Rectangle Height	V	11100101	345	E5	126	25
Rectangle Angle	U	11100100	344	E4	125	24
Numerical Values	0	11110000	360	F0	60	12
Numerical Values	1	11110001	361	F1	61	01
Numerical Values	2	11110010	362	F2	62	02
Numerical Values	3	11110011	363	F3	63	03
Numerical Values	4	11110100	364	F4	64	04
Numerical Values	5	11110101	365	F5	65	05
Numerical Values	6	11110110	366	F6	66	06
Numerical Values	7	11110111	367	F7	67	07
Numerical Values	8	11111000	370	FA	70	10
Numerical Values	9	11111001	371	FB	71	11
Start/End of Text	"	01111111	177	7F	42	37

*Start-of-record symbol is cent sign (¢) in EBCDIC, or less-than symbol (<) for other systems.

Fig.3.11 Tape character sets.

In the light of discussion above, pattern (produced by AutoCAD dxf file) are fracturated into rectangles through ASM 2600 software for Electromask Pattern generator. Fig. 3.12 shows a typical image (formed by AutoCAD drawing program) and its parts of equivalent data record for pattern generator job data in electromask format (ASCII format).



<X200270Y44500V3000U0SY47500SX203
700Y45570W860V5140SX201985Y48570
W2570V860U0SY46000V860SX205415Y4
8145W850V1710U0SX206270Y46430W86
0V1720SX208840Y48145W860V1710SX20
7985Y46430W850V1720SX207130Y44285
W860V2570SX210560Y44500W860V3000
SY47500SX212700Y43430W3420V860U0
SY48570SX211845Y46000W1710V860SX"
END JOB 220 FLASHES "Z.

Fig.3.12 Typical mask layout prepared by AutoCAD and its corresponding Electromask format output after the image is fracturated via ASM 2600 software.

There are four types communications way between instruments with computers; these are GPIB (equivalently HPIB), SCSI, RS 232 and TCP/IP. Since the tape reader unit (HP7974A) has an GPIB interface installed by HP, to communicate with the drive via computer, National Instrument GPIB card was installed and configured. To record the pattern data on a magnetic tape, a software (build in Borland C code) was developed as well as to read the prerecorded data on tape. The most important trick on the software is that the data should be sent in odd parity together with parallel poll should be enabled. Otherwise, GPIB error occurs. Also, in order to issue commands to the tape drive must first be addressed to listen (according to Read Data from tape or Write Record). After the listen addresses has been sent to the drive, the next message is expected is a secondary address commands. In fact, all tape commands like Read record, write gap, set density, rewind, move forward (backward) one file are sent via secondary addresses of the drive. To clarify the point, the GPIB message sequence should be

UNT/UNL (Untalk/unlisten)

MLA (my listen address)

MSA (tape command)

UNL/UNT (unlisten/untalk)

If the wrong sequence is selected, again GPIB error occurs. Before applying write record command (=5, tape command), tape density has to be set to 800 NRZI format (via tape command 18) and then with the mentioned GPIB sequence, write record command is sent to the drive unit. Similarly, other commands are issued. In addition to that, one must keep in mind that pattern data should be recorded in 800 bytes block (i.e., data should be divided into 800 bytes long files) in EBCDIC format onto 9 track magnetic tape with the sequence BOT/EOF/JOB data. Hence, finally, magnetic tape that contain pattern data are prepared and ready to use.

3.5 PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION-PECVD

3.5.1 Introduction

Low energy plasmas are partially ionized gases composed of ions, free electrons, atoms, molecules and free radicals. These plasmas are used in a wide variety of film processes, such as plasma enhanced chemical vapor deposition

(PECVD), plasma etching. Unlike other thin film techniques, such as molecular beam epitaxy and chemical vapor deposition (CVD), plasma processes are not at thermal equilibrium and the dynamics of these processes are not well described by equilibrium thermodynamics. Due to the complexities of plasma systems, many reaction mechanisms remain unknown, including those for material deposition.

Radicals have long been assumed to be the most important species in plasma depositions due to their relative reactivities and abundance in these systems. While traditional empirical methods of PECVD thin film analysis supply much needed information, the development of new plasma processes is severely limited by the lack of understanding of the chemistry occurring in these systems. Therefore, a solid understanding of the chemistry taking place at the plasma-surface interface during plasma processing is crucial for optimization of existing processes and to drive the development of new materials.

As mentioned above, unlike thermal plasmas (such as the sun), processing plasmas are not in thermodynamic equilibrium. In the bulk of plasma, the electron temperature is much higher than either the ion temperature or the neutral gas temperature. Although both electrons and ions gain energy from an external applied field, the elastic collisions with neutral molecules are numerous for both species. Because of the light masses of electrons compared to neutral molecules, little kinetic energy is transferred during collisions whereas similar masses between ions and neutrals yields a significant kinetic energy transferred between them. As known, in elastic collisions, kinetic energy and momentum are conserved physical quantities. Assuming the initial kinetic energy of neutral molecules is zero, the energy transformation within the head on collision approximation can be expressed as

$$E_{trans} = \frac{4 m_e m_n}{\left(m_e + m_n\right)^2} E_0 \qquad (3.1)$$

where m_e (m_n) is the mass of electron or ion (neutral molecule), E_{trans} is the energy transferred and E_0 is the initial kinetic energy of the ion or electron. This expression states that ions loose energy rapidly in collision with neutral molecules and they equilibrate to the same temperature. However, electrons (though they undergo

many elastic collisions) loose little kinetic energy (supplied by external applied field) due to the mass difference (see the expression 3.1). Thus, kinetic energy of electrons are much higher than ions or neutral molecules.

Because of the greater mobility of electrons over ions, electrons are lost preferentially to the surfaces of the plasma reactor which results in a positively charged sheath surrounding all surfaces in the reactor (see fig 3.12).

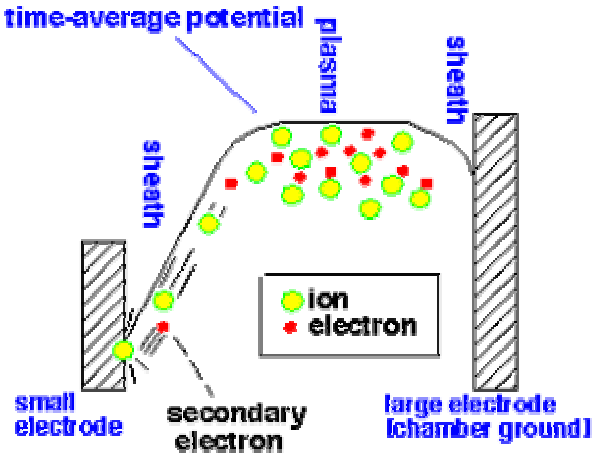


Fig.3.13 Potential distribution in the plasma reactor. Note also that plasma sheaths (dark area) occurs around surface in contact with the plasma.

Plasma sheaths are characterized by very low electron densities and appear as dark area adjacent to surfaces in contact with the plasma. Ions accelerated across this sheath are known as bombarding ions due to their high energy and plays an important role in reactive ion etching.

Another factors that makes plasma systems difficult to characterize is that they can exist in many different modes. All modes can be classified as either high density (such as inductively coupled rf discharges, microwave discharges and electron cyclotron discharges) or low density. The most common type of low density plasma is a parallel plate capacitively coupled discharge shown below:

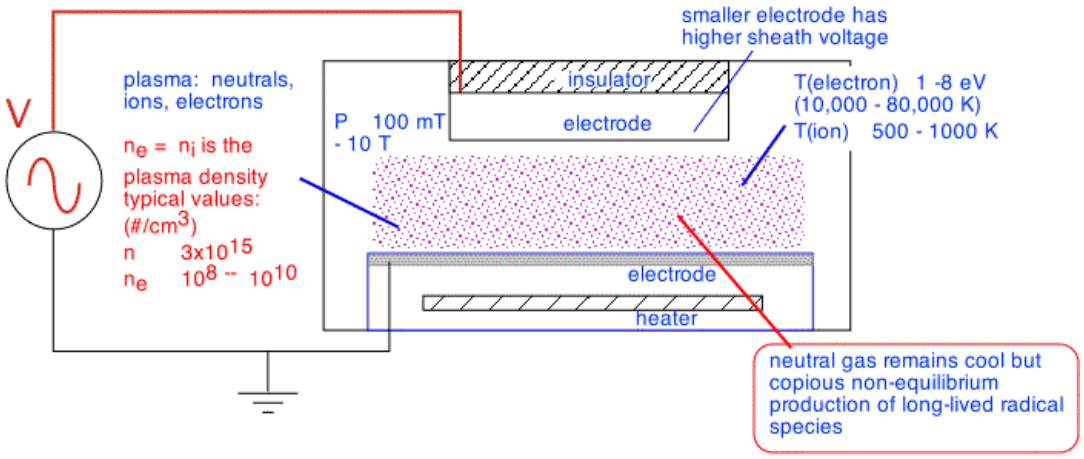


Fig 3.14. A simplified view of capacitive or Radio frequency (RF) diode plasma reactor. Also, typical numbers in plasma and its constituent pairs (electrons, ions) is given.

PECVD SYSTEM

Among various deposition technique, PECVD (glow discharge) is the most common method to deposit a-Si and its alloys (such as a-SiCx:H and a-SiNx:H); the former has found applications in solar cells, flat panel displays, photoreceptor and photo resist materials while the latter is used as gate dielectrics and barrier coatings in microelectronic devices, as capacitors in dynamic random access memory cells and in the micro fabrication of sensors and actuators. Here the various aspects of the chemistry of plasmas used for producing thin films of a-SiCx:H and a-SiNx:H will be investigated in the following subsections. Let us look at the main points of PECVD deposition system at hand (shown in fig.3.15 and 3.16).

For initiation of the plasma, the radio frequency (RF) power with a certain amplitude V_0 (large enough to cause the breakdown of process gas) is applied to the reactor. A typical reactor (see fig.3.15 and 3.16) consists of a source of power for the discharge (RF in our case), a gas inlet arrangement, a deposition chamber that holds the pair of electrodes and a substrate heating assembly, a pumping system.

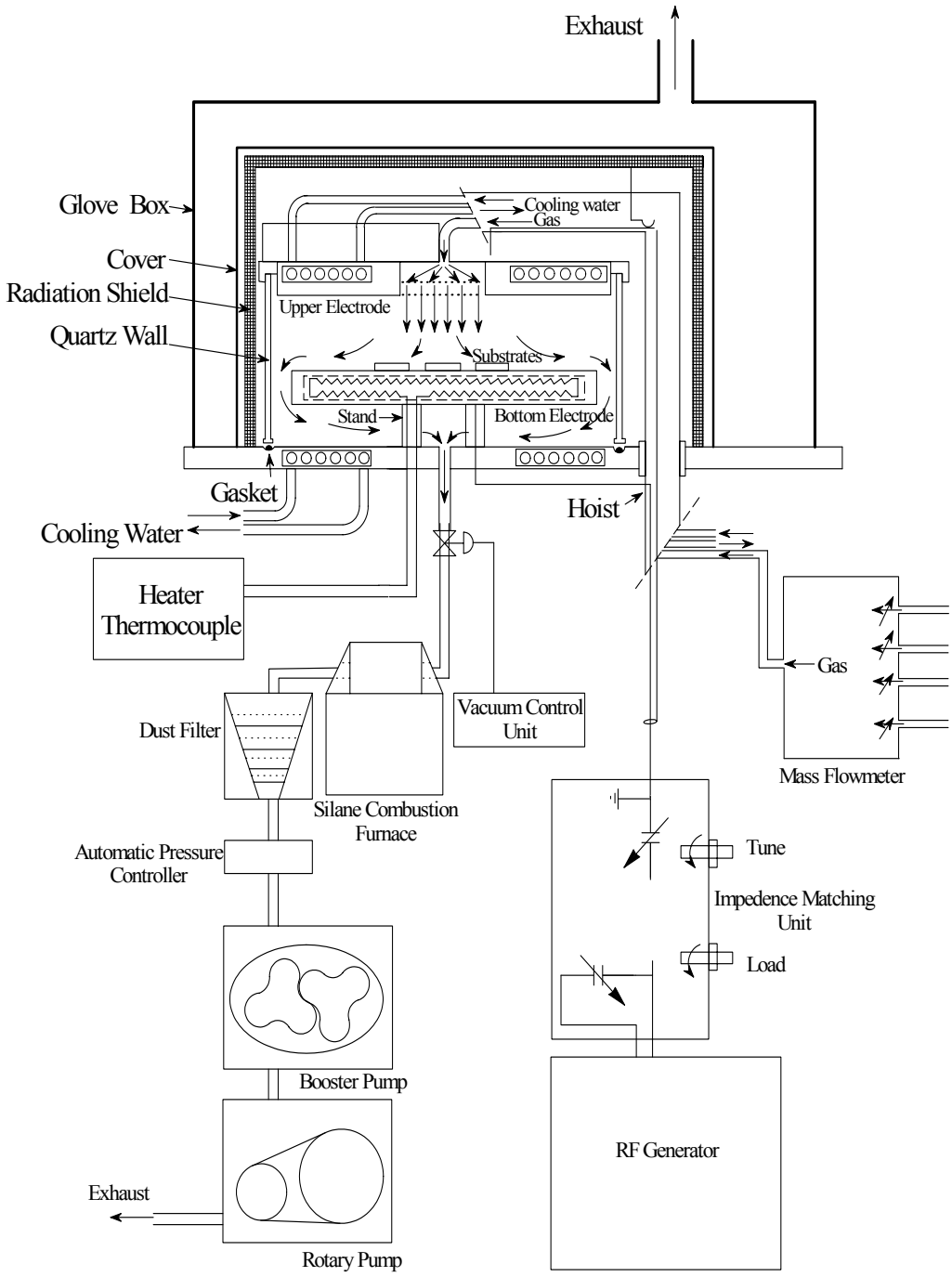


Fig 3.15. Schematic illustration of PECVD reactor at hand.

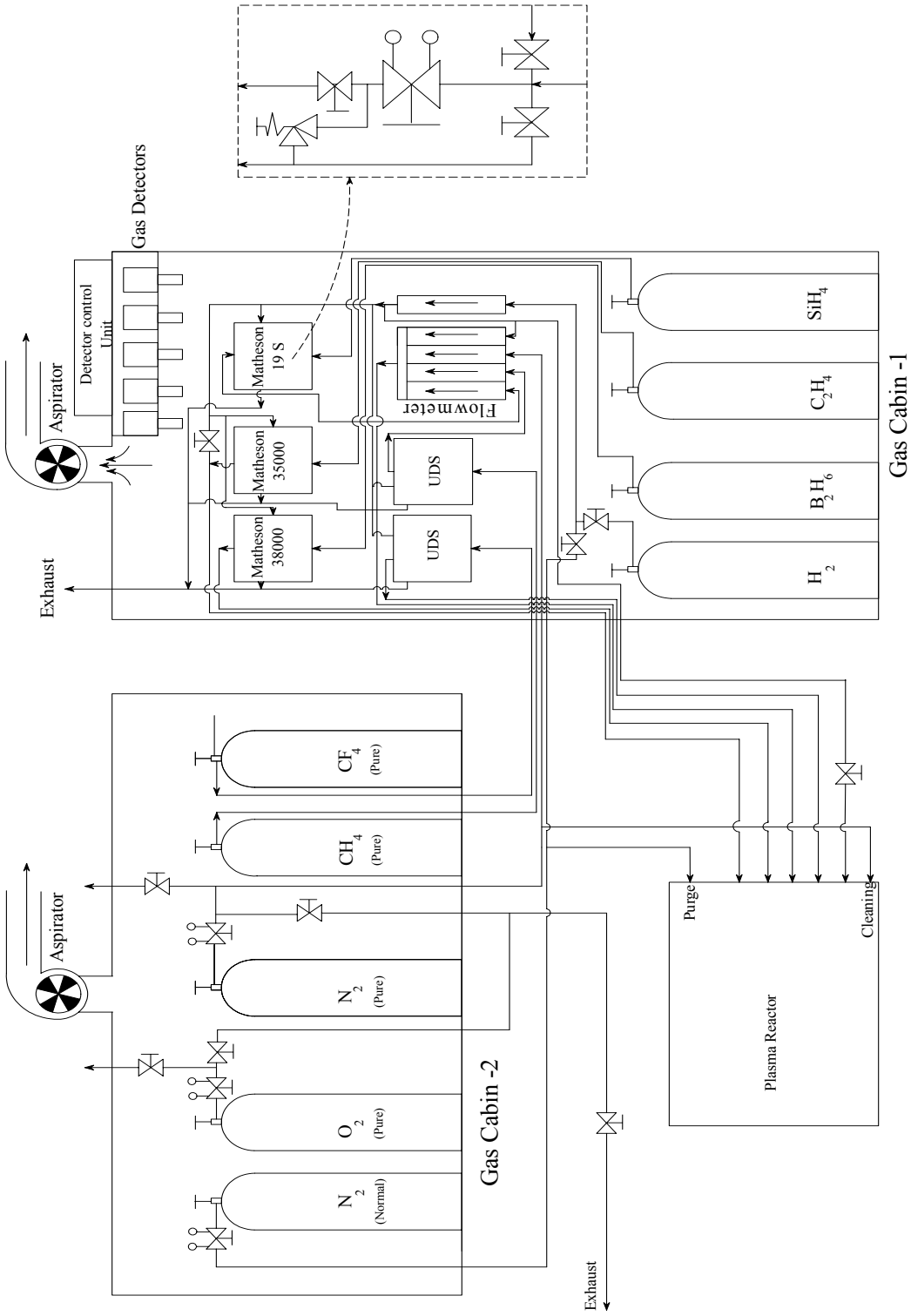


Fig 3.16. Gas cabinet system associated to PECVD system.

Radio Frequency (RF) Diode

One of the more popular configurations of processing reactors is the rf diode which consists of two electrodes that are capacitivley coupled, typically with one electrode powered by RF and the other grounded.

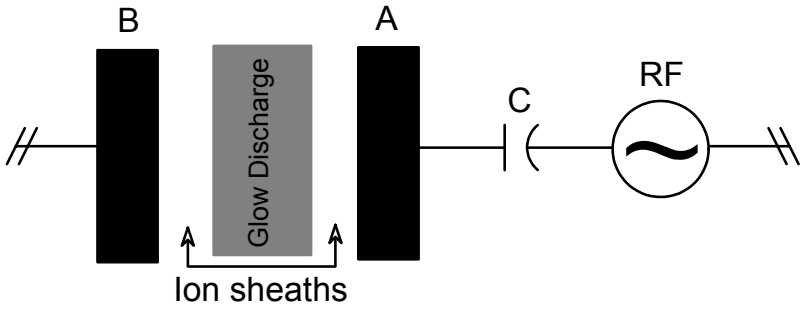


Fig.3.17 Schematic illustration of RF diode

The RF is usually 13.56 MHz, a frequency chosen to avoid interference with communication equipment. In the rf diode, the electrons respond to the instantaneous changes on the RF fields, while the heavier ions only respond to time averaged changes. The plasma provides high energy for the dissociation of the feed gas, while the thermal temperature remains relatively low. Processing plasmas typically have electron temperatures in the range of 1-8 eV, densities of 10^8-10^{13} cm^{-3}, and exist over a range of pressures roughly from 100 millitorr to 1 Torr.

Upon application of field with amplitude V_0 and frequency lower than the RF range, the ions created during the breakdown cannot fully extracted from the inter electrode gap in one half of the cycle while electrons are easily extracted due to their light masses. If the frequency is increased up to the RF range (25 kHz-25 MHZ), the electrons have insufficient time to drift to the electrode during the positive half cycle; thus these electrons oscillate in the inter electrode gap. Consequently, upon application of the RF power to the reactor, with a certain potential, discharging occurs in the inter electrode gap of the reactor. As a result, created electrons and positively charges ions constitute glow discharge with a potential V_p in the reactor (see fig.3.18)

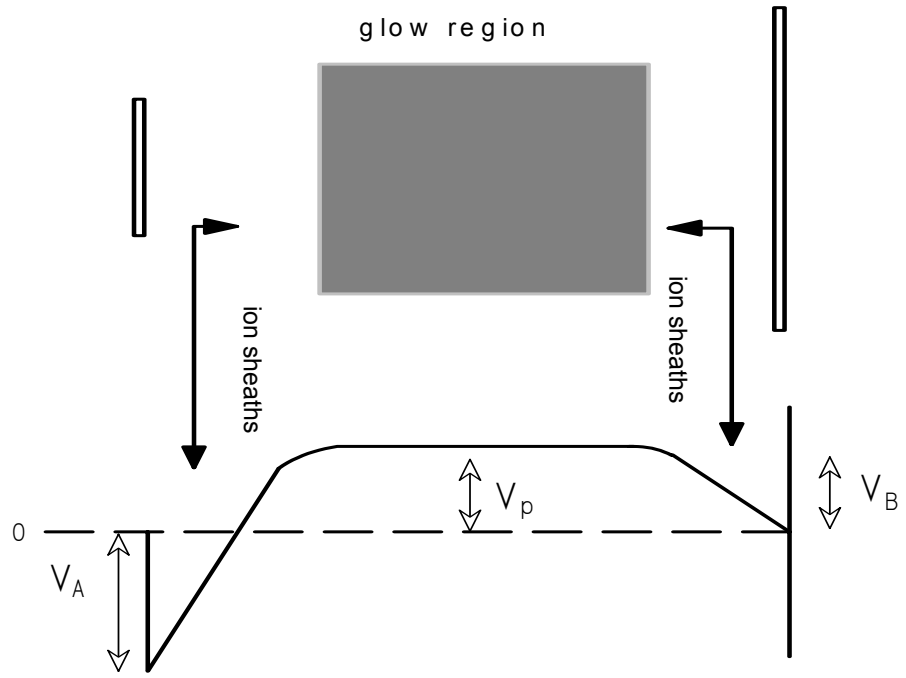


Fig 3.18. Potential distribution in PECVD reactor. Note that there are three main regions: V_B, grounded electrode, plasma potential, V_p and powered electrode, V_A.

One should keep in mind that the ground potential in the reactor is always negative with respect to plasma, as a consequence, the substrate surface on the grounded electrode should more or less suffer the positive ion bombardment. The potential on the powered electrode is also negative with respect to plasma potential; at the negative half cycle of the applied RF signal, positive ions from the discharge are accelerated towards the power electrode. These ions remove electrons from the electrode surface in order to be neutralized and leaving behind a positive charge on the electrode surface. On the other hand, as for the positive half cycle, the electrode collects electrons. Due to lighter mass of the electrons compared to ions, the electric field makes them accelerates more rapidly to the electrode. Thus during the two halves of first cycle, many more electrons than ions are collected, yielding the negative charge. For the subsequent cycles, the negative charge building increases up to the steady state where at negative cycles in coming electrons are repelled and incoming ions are attracted more strongly up to a certain value, in there, electron concentration is equal to ion concentration. Hence, this averaged negative charge

piles up at the electrode causes a negative dc offset voltage V_{dc} called self bias on the powered electrode shown in fig 3.18.

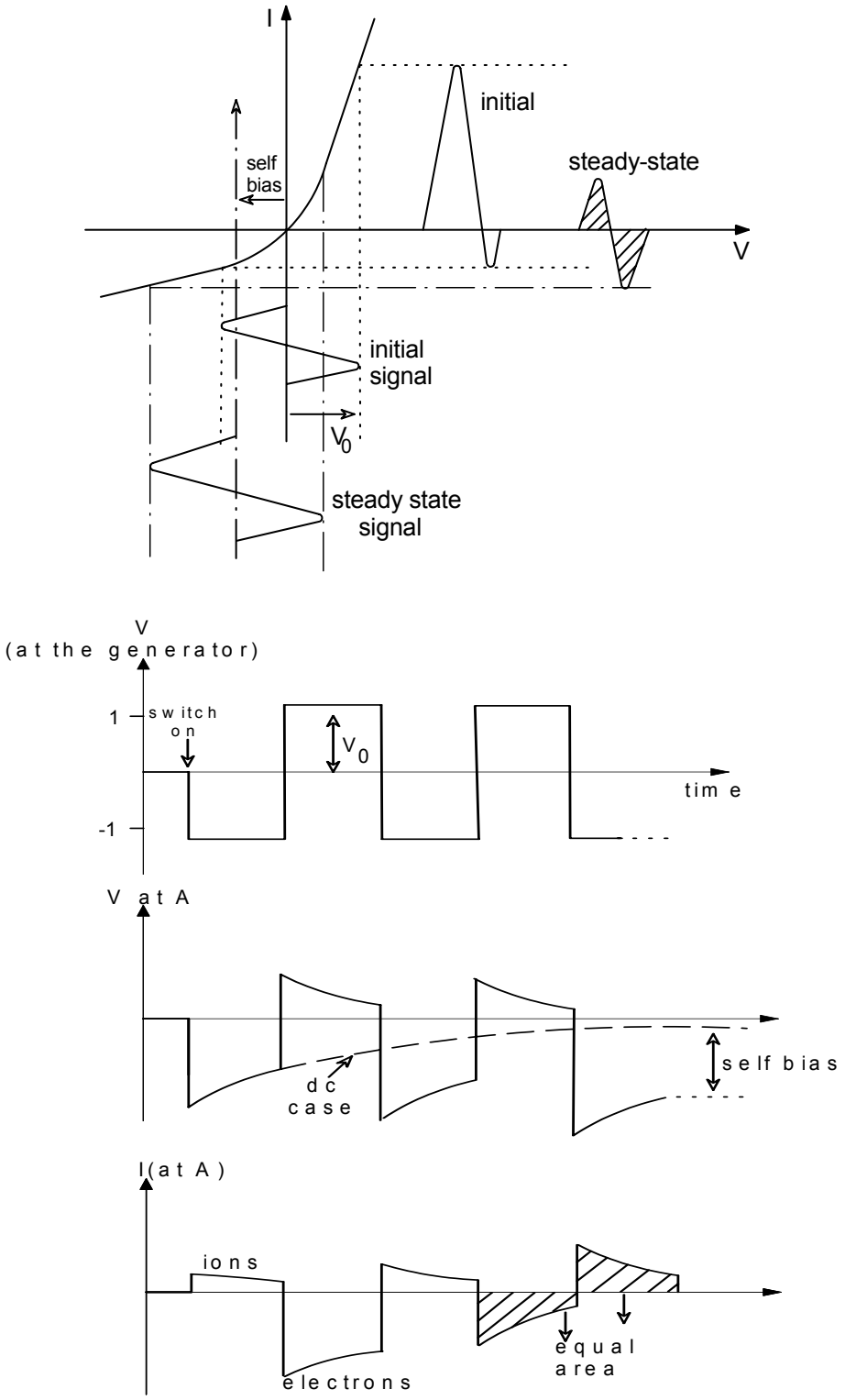


Fig. 3.19 I-V characteristic of the plasma

The I-V characteristic of the plasma (see fig.3.19) suggest that it is like a leaky diode, due to great difference in mobility between electrons and ions. During the half of the cycle, positive voltage is applied to the electrode, resulting a very large electron current flows in to the electrode. As for the negative half cycle, negative voltage is applied, a small ion current flows into the electrode. At steady state, the electrode is negatively self biased and zero net current is attained, since the blocking capacitor obstructs charges flowing out. Consequently, both electrodes are at negative potential with respect to the glow discharges. Besides in each electrode, dark regions (ion sheaths) constituted by positive ions without electrons are observed (see fig.3.18). Since the glow discharge region is at a fixed potential, the potential drop mainly occurs on these ion sheath regions.

Gas Inlet Arrangement

Control of process gas flow is crucial for PECVD system, so an elaborate gas control system (consists of gas cabinet, flow meters and gas pod) has to be owned. The process gases might be reactive and non-reactive. The latter used for purging the system where process gas are delivered. The former (such as silane) should be placed into a cabinet, donated with an exhaust to maintain air flow essential to eliminate any accumulation of process gases within the cabinet due to the fact that these gases are highly explosive and all poisonous. Therefore, most of the plumbing and connections from where gas leaks might probably occur under pressure are stainless steel and uniquely built into the gas cabinet. Additionaly, high quality stainless steel regulators, check valves and cross purge assembles have been utilized for safety reasons and cleanliness of the process. At final stage the master unit of the system has the gas pod where the flow of gases are automatically controlled by a programmable controller. The selection of flow lines are obtained by pneumatic valves since the process gas are flammable. Therefore, in that way, the probability of electrical arcs (might be dangerous in the case of gas leakage) is eliminated, as they operate under pressurized air over four bars. The flow-rate of process gases are controlled at the desired value by mass flow controllers using TYLAN source technique where the flow rate is sensed by a mass flow meter and controlled by an electromechanical servo value.

Pumping System

The pumping system consists of the turbo molecular pump and the roots blower type pump, used for producing and maintaining the low pressure during the operation of both reactors. The larger rotary value type mechanical pump is used as the backing pump of the roots blower and the other one is used for backing the turbo molecular pump. The turbo molecular pump is used to maintain high vacuum in the etching reactor to facilitate the removal of all residuals which may react with the plasma to deteriorate the etching process. Both of the roots blower and the turbo pumps are oil free, thus the impurity control of the process can be obtained as much as the purity of the process gases. The vacuum levels of the reactors are measured by the baratron gauge upto 3 mTorr. The pumping sequence of the reactors is controlled by a programmable timer with respect to pressures measured with gauges.

Deposition chamber

The reactors of this system are capacitive coupling type in cylindrical shape with diameter of 400 mm. The distance between the electrodes is 40 mm, RF power is applied to upper electrode, made of aluminum and cooled with water. The process gases are introduced into the plasma ambient from the middle of this electrode. Substrates are placed on the lower electrode, grounded and made of anodized aluminum. The temperature of the lower electrode can be controlled between room temperature and 400 ^{0}C. the table where the lower electrode is fitted with thermally resistive stand is cooled by water to protect the o-ring of the chamber wall, made of Pyrex glass. The upper electrode is mounted by the hoist assembly and hence sample change times are very short. Additionally, a glove box is supplied to load and unload the substrate or grown films in a clean environment under N_2 flow. This has a load lock to ensure that the atmosphere in the room can not be exposed into while placing the substrate in it.

3-6 Growth of Amorphous Silicon Based Thin Films

Before loading of the substrate into deposition chamber, the following procedure has to be followed up to clean the substrates (Silicon wafers for infrared and electrical characterization, sliced glass and quartz, for ellipsometry and UV-Visible Transmittance).

3-6-1 Cleaning of Substrates

Cleaning procedure for silicon wafers and others shows little difference; as for the former, after samples were boiled in trichlorethylene for 5 minutes, they were rinsed in deionized water (DW) H_2O and then agitated by ultrasound. The rinsing process was repeated after each step during the cleaning procedure. Later, samples were dipped in HCl/H_2O_2 mixture, with 1/1 mixing ratio, for 10 minutes. As a next step, samples were dipped in H_2SO_4/H_2O_2 mixture, with 2/1 mixing ratio, for 5 minutes. In the last stage, they were washed in running (DW) H_2O for 5 minutes. Finally, samples were dipped in HF/H_2O mixture, with 1/10 mixing ratio, about 30 seconds and then washed in running (DW) H_2O for 15-20 minutes.

On the other hand, as for sliced glasses and quartz substrates, they were dipped in KOH solution and agitated by ultrasound for at least 30 minutes. Subsequently, they were washed by (DW) H_2O. All the samples were finally dipped in diluted HF, with 1/100 ratio, and washed in (DW) H_2O. In order to prevent cleaned samples from pollution, the fabrication must start as soon as possible after cleaning.

3-6-2 Deposition of a-Si:H films

The growth of the film on the substrate takes place through the following stages: in the first one, electrons collide with silane to dissociate the silane molecules into a mixture of reactive species of ions and free radicals. The second stage is drifting or diffusion of these species to the surface of the substrate during which time there is a multiplicity of secondary reactions. In the third stage, the different species are adsorbed onto or react with the growing surface and finally,

these species or their reaction products are incorporated into the growing film or are reemitted from the surface into the gas phase.

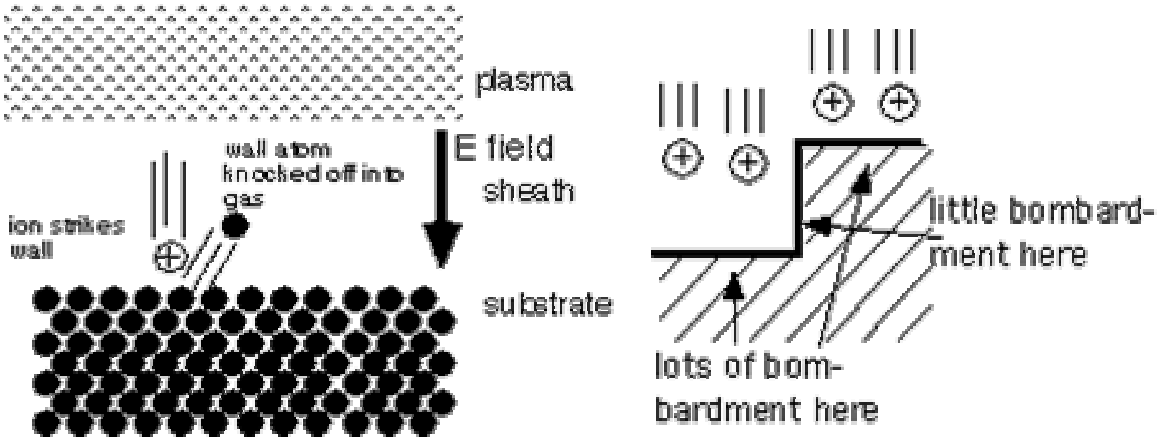


Fig.3.20. Schematic illustration of the formation on film in the PECVD reactor.

Some of the species generated by primary and secondary collisions.

Primary	Secondary
$e+ SiH_4 \rightarrow SiH_4+e$	$SiH_4+H \rightarrow SiH_3+H_2$
$\rightarrow SiH_2+H_2+e$	$SiH_4+SiH_2 \rightarrow Si_2H_6$
$\rightarrow SiH_3+H+e$	$SiH_3+SiH_4 \rightarrow SiH_4+SiH_3$
$\rightarrow SiH+H_2+H+e$	$SiH_4+Si_2H_6 \rightarrow Si_nH_m$
$\rightarrow SiH_2^{+}+H_2+e+e$	
$\rightarrow SiH_3^{-}+H+e+e$	
$\rightarrow SiH_3^{-}+H$	
$\rightarrow SiH_2^{-}+H2$	

Amongst the various species generated by the primary impact process, SiH_3 has the longest lifetime since SiH_2 react with the parent SiH_4 molecule to form SiH_4 and SiH_3 again. On the other hand, successive collisions of SiH_4 with SiH_2 can create higher silane related species that could continue to grow causing powder formation. The number density of the various species in the plasma that have been detected in a typical glow discharge reactor is shown in fig.3.21.

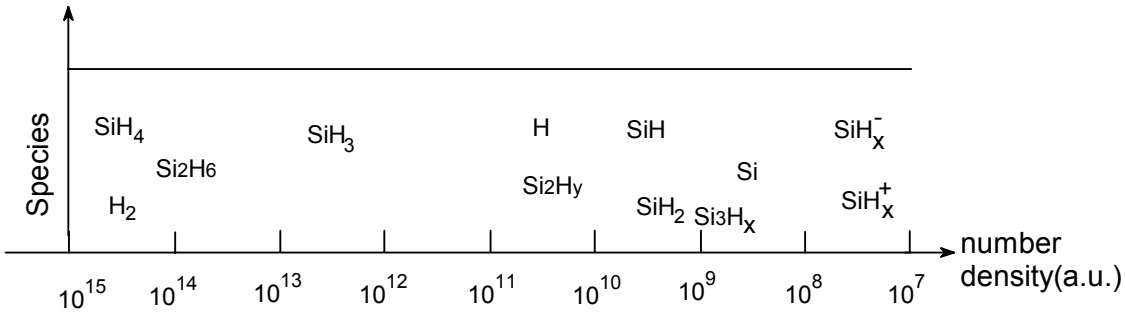


Fig 3.21. Number density cm^{-3} of species in a typical rf glow-discharge plasma. From [12].

All the species shown above, together with some higher silane related species, arrive at the substrate. Most of the growing surface is terminated with hydrogen and will not take up SiH_3 radicals, which is the most abundant species. Bonding of SiH_3 onto the surface needs dangling bonds, and removal of hydrogen from the surface is, therefore, a necessary step in the deposition of films from SiH_3. Hydrogen can be released from the surface by thermal excitation, or it can be stripped by SiH_3 reacting with SiH to form a dangling bond and SiH_4. Another SiH_3 molecule migrating alone the surface or arriving directly can then be incorporated in the film. The other radicals like SiH or SiH_2 can be incorporated directly on the hydrogen terminated surface and thus have high sticking coefficient. Under normal deposition conditions, these radicals do not contribute much to the film growth since their density is small. They have an adverse effect on film quality.

3-6-3 Deposition of a-SiCx:H films

Once introducing ethelenye over the silane in the reactor to produce a-SiCx:H, film, over the demonstrated silane reaction above, the cross reaction between the radicals of these mentioned two gases also occur [37-39].

$SiH_2+C_2H_4 \rightarrow C_2H_4SiH_2$ (silirane)

In the silane-ethylene mixture the reaction above becomes dominant and it generates silirane molecule. In the deposited films, Si-C bonds, Si-Si and C-C bonds are present (determined through IR analysis, given in Appendix B). Especially, in order to increase the forbidden energy gap of the films, the density of the carbon containing gases must be increased. Unfortunately, this also leads to the formation of aromatic islands of carbon rings, which negatively influences the band gap and electrical characteristics of the deposited film.

3-6-4 Deposition of a-SiNx:H films

PECVD deposited a-SiNx:Hy film is usually grown from a NH_3-SiH_4 gas mixture where x and y vary widely depending on the gas mixture and other deposition parameters, outlined in the section 3.4. Smith et all.[40] investigate the PECVD grown a-SiNx:H film with NH_3-SiH_4 gas mixture in order to minimize Si dangling bonds and Si-H bonds that being accused of trapping centers. Under low SiH_4 flow and sufficient power to activate the NH_3, the SiH_4 reacts completely to tetraaminosilane, $Si(NH_2)_4$ with the following chemical reaction:

$$SiH_4+NH_3 \rightarrow Si(NH_2)_4$$

The plasma chemistry is aminosaturated. $Si(NH_2)_4$ and the triaminosilane radical then become the precursors for the nitride deposition. Since Si is completely bonded to N in the precursors, films deposited under these conditions contain minute amount (or even no) (< 1%) Si-H bonding. Moreover, because of not all of the excess N is eliminated in the deposition process, the films are N-rich with substantial N-H and some NH_2 bonding. The N/Si ratio of investigated films in this work is 1.6 compared to stoichometric ratio of 1.33 for crystalline Si_3N_4. Fourier transform infrared (FTIR) absorption spectroscopy and UV-Visible transmission measurements were performed and results were given in Appendix B as optical probing of grown films.

3.7 Factors Influencing Film Quality

The deposition parameters/conditions that control the property of the material as follows:

i) Pressure and Electrode Seperation: The voltage necessary to sustain a plasma is defined as the Paschen curve which determine the sustaining voltage as a function of the pressure and the electrode separation.

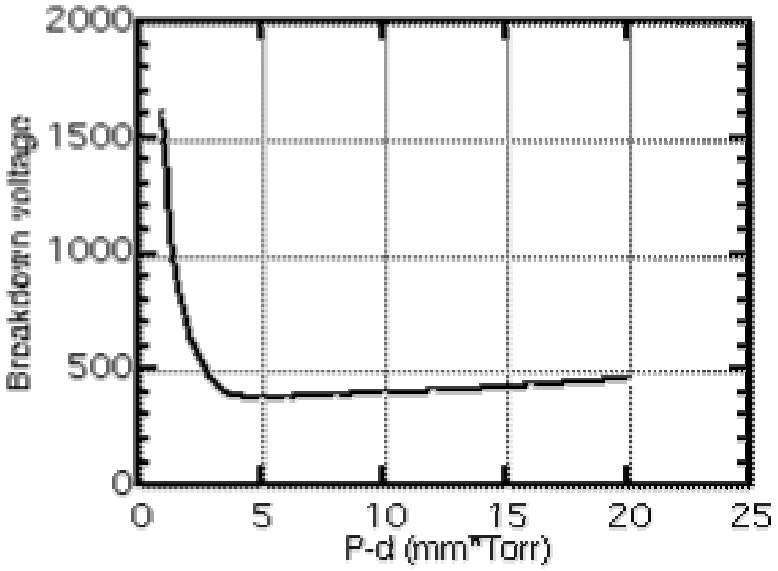


Fig.3.22. Breakdown voltage vs. P-d product for air, note that The voltage necessary to initiate a discharge is roughly a function of the product of the spacing between electrodes and the pressure. At higher pressures, the discharge voltage increases, making it difficult to start the plasma if the electrode spacing is large.

ii) In order to have a low sustaining voltage, the pressure is maintained between 0.1 to 1 Torr and the electrode separation between 4 to 6 cm. Higher pressure or larger electrode separation results in many secondary reactions which may cause formation of powder and higher silanes affecting material property.

iii) Temperature: The substrate temperature plays a key role in determining adatom mobility of the impinging species on the substrate, and a higher substrate temperature results in higher adatom mobility allowing more surface diffusion. This leads to the species to find an energetically

favorable site resulting in a denser material. Higher temperature, however, causes loss of hydrogen from the surface. The dangling bonds generated thereby increase the sticking coefficient and lower surface mobility. The optimum substrate temperature is between 200 to 300 ^{0}C for typical rf glow discharge deposition.

iv) Power density: With increasing power density, more polymeric radicals are formed in the plasma that may lead to powder formation. The heavier radicals also have low adatom mobility as they impinge on the surface of the growing film. This results in film grown with higher density of microvoids and leads to poor cell performance. The optimum power density is just above the value at which the plasma can be sustained and is typically 10 to 100 mWcm^{-2}.

v) Gas flow rate: As the gas flow rate decreases, the residence time increases, which may results in depletion of the active species. Matsuda [41] has shown that under these conditions, the calculation of the short-lifetime radicals (including heavy radicals) to the growth rate increases, yielding to poor material quality. An adequate flow rate results in a linear increase in the deposition rate as the power density increases, therefore, it is recommended.

vi) Hydrogen Dilution: Guha et all [42] has showed in 1981 that film grown with a gas mixture of silane diluted with hydrogen have improved quality. Hydrogen dilution is now used extensively with many different active gases. The vital role of hydrogen dilution is to improve surface coverage that results in increased surface diffusion.

CHAPTER 4

ADMITTANCE OF MIS STRUCTURE

4.1 MIS CAPACITOR

4-1-1 Introduction

The control of the insulator and insulator film interface (such as SiO_2/Si, a-SiNx:H/Si) properties are crucial for the performance and stability of the mentioned insulator/semiconductor material based devices. The charge states of the structural defects and impurities, either in the insulator or at the interface, can modify the energy band structure of the silicon in the vicinity of the interface and thus can lead to modifications in electrical characteristics of devices. These charges in the metal-insulator-semiconductor (MIS) system have gained special importance with the emergence of integrated circuits using MIS structure in thin film transistor as active elements. These circuits are sensitive to the presence of minute traces of charges ($\approx 10^{10}$ cm $^{-2}$). To simplify the study of the MIS system as prepared under realistic manufacturing conditions, the MIS capacitor is used extensively as a simple test structure. The resulting knowledge of the charges in the MIS capacitors may be used to improve the fabrication techniques and conditions.

The measurements of the admittance of MIS capacitors is a powerful tool for investigating the electronic properties of the different parts of this structure since it is extremely charge sensitive technique. This technique consists of the admittance measurements of MIS capacitors as a function of various parameters such as dc bias voltage, ac voltage modulation frequency, illumination, temperature, etc…In analyzing the experiments, equal importance is attributed to the imaginary (capacitive) and real (conductive) parts of the admittance. The capacitance C, (or conductance G) versus gate voltage V_G characteristics for various frequencies have been extensively used in the investigations for MIS structures.

4-1-2 CAPACITANCE-VOLTAGE CHARECTERISTICS

The term capacitance is used in this work to mean differential (or dynamical) capacitance: $C \equiv \delta Q_m / \delta V_G$ with Q_m designating the charge on the gate, V_G applied bias to the gate. On the other hand, keep in mind that the static capacitance $\left(C_{st} \equiv Q_m / V_G\right)$ different from differential capacitance since Q_m varies nonlinearly with V_G in some ranges.

The modulation V_G of the gate bias may be obtained by superimposing a relatively small amplitude a.c voltage $\left|\delta V_G = a \exp(j\omega t)\right|$ on the dc gate bias V_G. Consider an ideal MIS capacitor shown in fig. 4.1 (with no interface states, insulator charges or work function difference).

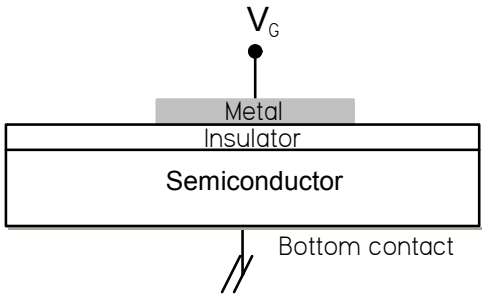


Fig. 4.1 Cross section of MIS capacitor

The small signal equivalent circuit of this ideal MIS system for p-type silicon substrate will be discussed; the results may be converted to an n-type silicon substrate system by adequate changes. There are mainly three regions of interest when plotting C-V_G: Accumulation, depletion and inversion.

i) Accumulation: for sufficiently large negative gate voltages, V_G, the majority carriers (holes) will be attracted to the surface of silicon (the gate voltage V_G will be wholly dropped across the insulator). As shown in fig.4.2-a, the measured capacitance will correspond to the insulator capacitance C_{ins} as a result of the parallel plate capacitor approximation:

$$C_{ins} = \delta Q_m / \delta V_G = \varepsilon_{ins} / x_{ins} \left(\text{F/unit area}\right) \qquad (4.1)$$

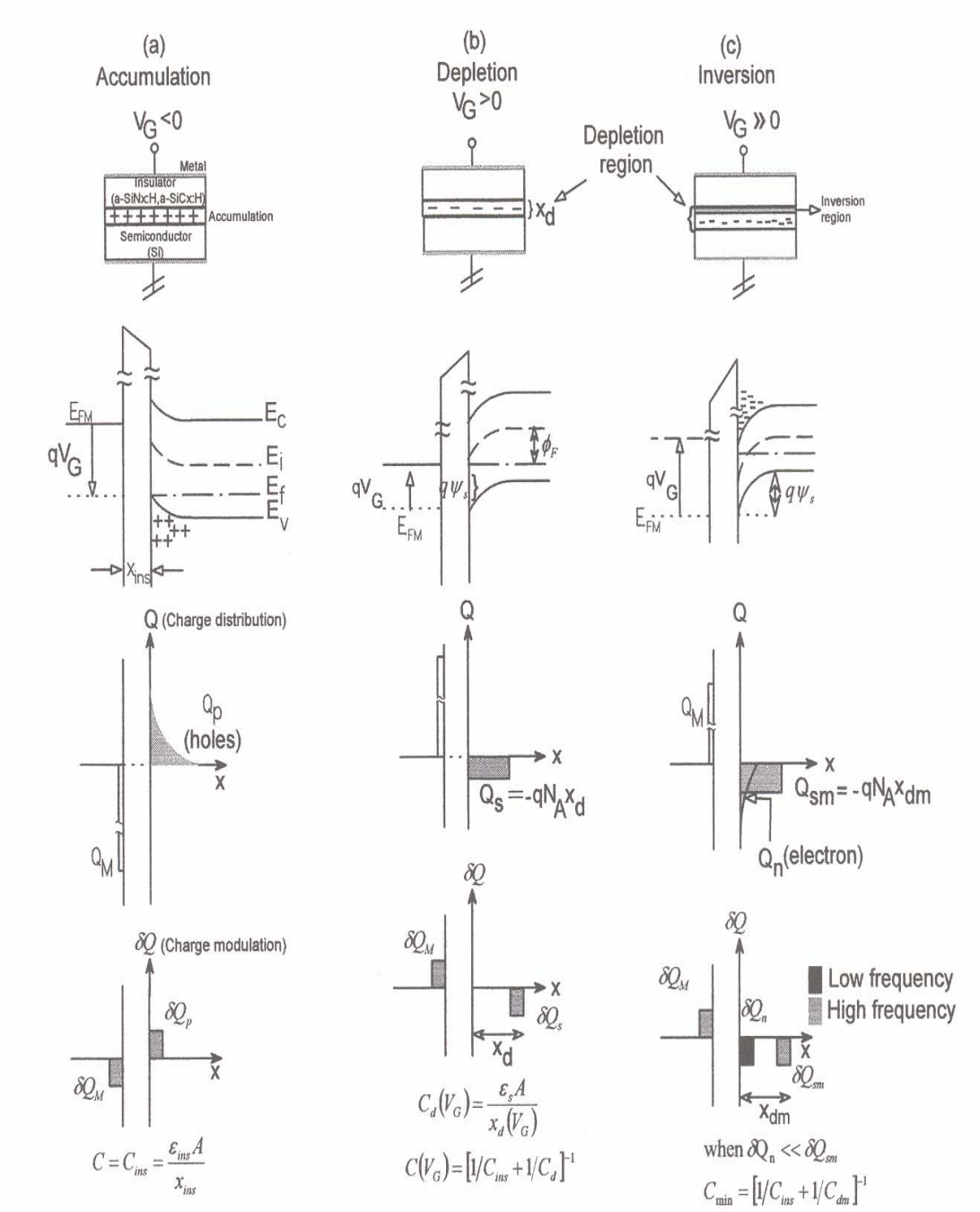


Fig. 4.2 Charge distribution (and capacitance) for different gate voltage values in the MIS structure.

ii) Depletion: when the gate voltage passes from negative to positive region, the free holes will be swept away from the surface region of silicon by the resulting electric field and a space charge or depletion region is formed (depicted in fig.4.2-b).

As the insulator is assumed to be nearly perfect, there is no dc current flow (thermodynamical equilibrium holds) and thus there is no need to solve transport equation; the Poisson equation alone governs the potential distribution $\psi(x)$, throughout the depletion region. As the product np of free carriers must remain constant at each point of the depletion region (due to thermodynamical equilibrium), to a decrease of free hole density $p_p(x)$ should corresponds to an increase of free electron density $n_p(x)$ towards the interface. As a result the space charge density $\rho(x)$ may be expressed as:

$$\rho(x) = q\left[p_p(x) - n_p(x) + N_D - N_A\right] \qquad (4.2)$$

The Poisson equation, in one dimension, may be written as:

$$\frac{d^2\psi(x)}{dx^2} = -\rho(x)/\varepsilon_s \qquad (4.3)$$

Where $\varepsilon_s = \varepsilon_0\varepsilon_r$ with ε_r semiconductor relative permittivity, N_A and N_D acceptor and donor ion concentration respectively. In the bulk of semiconductor, the equilibrium free carrier concentration p_{p0} and n_{p0} are equal to $p_{p0} - n_{p0} = N_A - N_D$ consequently $n_p(x)$ and $p_p(x)$ may be expressed as,

$$p_p = p_{p0}\exp\left[-q\psi(x)/kT\right]\ ;\ n_p = n_{p0}\exp\left[q\psi(x)/kT\right] \qquad (4.4)$$

The expression of the electric field $E(x)\left(\equiv -d\psi/dx\right)$ across the depletion region can be established by solving (4.3)

$$E(x) = \frac{2^{1/2}kT}{qL_D}\left[\exp\left(-q\psi/kT\right) + q\psi/kT - 1 + \left(n_{p0}/p_{p0}\right)\left(\exp\left(q\psi/kT\right) - q\psi/kT - 1\right)\right]^{1/2} \qquad (4.5)$$

Where the parameter L_D, called extrinsic Debye length is defined as the characteristic screening length of a small charge in an extrinsic semiconductor: $L_D = \sqrt{\frac{kT\varepsilon_s}{q^2 N_A}}$. The expression of the electric field at the semiconductor surface, ψ, is obtained by replacing $\psi = \psi_s$ and ψ_s is called surface potential. The space charge Q_s within the surface region of semiconductor, required to produce this field is obtained by using Gauss law:

$$Q_s = -\varepsilon_s E_s \qquad (4.6)$$

For most of practical uses, the depletion approximation may be assumed that is $p_p=n_p=0$ in the depletion layer and charge neutrality condition holds beyond the depletion layer edge (a step like boundary between neutral bulk and depletion region is assumed as shown in fig. 4.2-b). Within this approximation, the Poisson equation (4.3) yields the potential distribution:

$$\psi(x) = \psi_s(1 - x/x_d)^2 \text{ with } \psi_s = \frac{qN_A}{2\varepsilon_s} x_d^2 \text{ or } x_d = \left[2\varepsilon_s \psi_s / qN_A\right]^{1/2} \qquad (4.7)$$

Where x_d =depletion region width; $V_G = V_{ins} + \psi_s$ with V_{ins} =voltage drop across the insulator. A gate voltage modulation δV_G will induce a modulation $\delta\psi_s$ of ψ_s; $\delta V_G = \delta V_{ins} + \delta\psi_s$ and this modulation of surface potential, in turn, will induce a charge modulation δQ_s at the edge of depletion region as shown in the fig.4.2-b. According to the parallel plate capacitor model, the capacitance associated with the depletion region can be expressed as :

$$C_d(V_G) \equiv \delta Q_s \Big/ \delta\psi_s = \frac{\varepsilon_s A}{x_d(V_G)} \qquad (4.8)$$

This capacitance is in series with that of the insulator capacitance C_{ins} and the total capacitance C of the system is as

$$C(V_G) = \left[1/C_{ins} + 1/C_d\right]^{-1} \qquad (4.9)$$

At the boundary between the accumulation and depletion regions the flat band condition is reached where there is no band bending at the silicon surface, that is, $\psi_s = 0$. By expanding in a power series about $\psi_s = 0$, the exponential terms in relation (4.5) and (4.7), the depletion capacitance at the flat band condition $C_d(FB)$ may be derived:

$$C_d(FB) \equiv \left(\frac{\delta Q_s}{\delta \psi_s}\right)_{\psi_s=0} = \left(\frac{dQ_s}{d\psi_s}\right)_{\psi_s=0} = \varepsilon_s A / L_D \qquad (4.10)$$

The total capacitance of the MIS system at flat band condition, C_{FB}, can be expressed as:

$$C_{FB} = \left[1/C_{ins} + 1/C_d(FB)\right]^{-1} = C_{ins} C_d(FB) / \left(C_{ins} + C_d(FB)\right) \qquad (4.11)$$

iii) Inversion: In the depletion regime, the positive gate charge (Q_m) is balanced by negative acceptor ions in the silicon depletion layer (fig.4.2-b), however, free electrons as negative charges with increasing concentration towards the interface appear in the depletion region in order to keep the product $p_p n_p$ constant, when the positive gate bias continues to increase the surface potential ψ_s increases in the same direction; at $\psi_s = \phi_F$ the surface of silicon becomes intrinsic ($p_p = n_p$) with ϕ_F being the difference between intrinsic level E_i in the bulk and the Fermi level (fig.4.2-c). Beyond the value $\psi_s = \phi_F$, the surface region of silicon is inverted into n-type (a thin inversion layer if formed near the insulator/semiconductor interface, in a region of 20-300 Å depending on bias and doping density). The region from $\psi_s = \phi_F$ up to $\psi_s = 2\phi_F$ is called weak inversion. Beyond the limit $\psi_s = 2\phi_F$, the electron density at the surface will be exponentially increased and any further increases in positive charge will be balanced almost entirely by the addition of electrons to the inversion layer. The region beyond $\psi_s > 2\phi_F$ is called strong inversion (fig.4.2-c). During this regime, the depletion layer width, reaching its maximum value does not need to be changed:

$$x_{dm} = \sqrt{4\varepsilon_s \phi_F / qN_A} \qquad (4.12)$$

In accumulation and depletion bias regimes, the charge modulation in response to a gate voltage modulation, arises from majority carrier flow (here holes) in and out of the silicon depletion region. The majority carrier supply (or loss) may be considered instantaneous within the common frequency ranges (up to a few MHz); in other words the majority carrier charges will follow the ac gate voltage modulation as long as the period of the ac voltage is much longer than the dielectric relaxation time of silicon $\tau_D\left(10^{-12} < \tau_p < 10^{-6}\ \text{sec}\right)$. As a result no frequency dependence is expected in accumulation and depletion regime. But in inversion, the charge modulation, is carried out by the minority carrier flow in and out of the depletion region and the minority response time, τ_R, is relatively long (at room temperature, for silicon τ_R is typically 0.1-1 sec in strong inversion). The main mechanism for getting minority carriers to and from the inversion layer is the generation-recombination of minority carriers in the depletion layer through a bulk trap around the Fermi energy level. Because this response time is very long (compared to the period of ac gate voltage modulation), inversion layer capacitance will be frequency dependent except at very low and high frequencies:

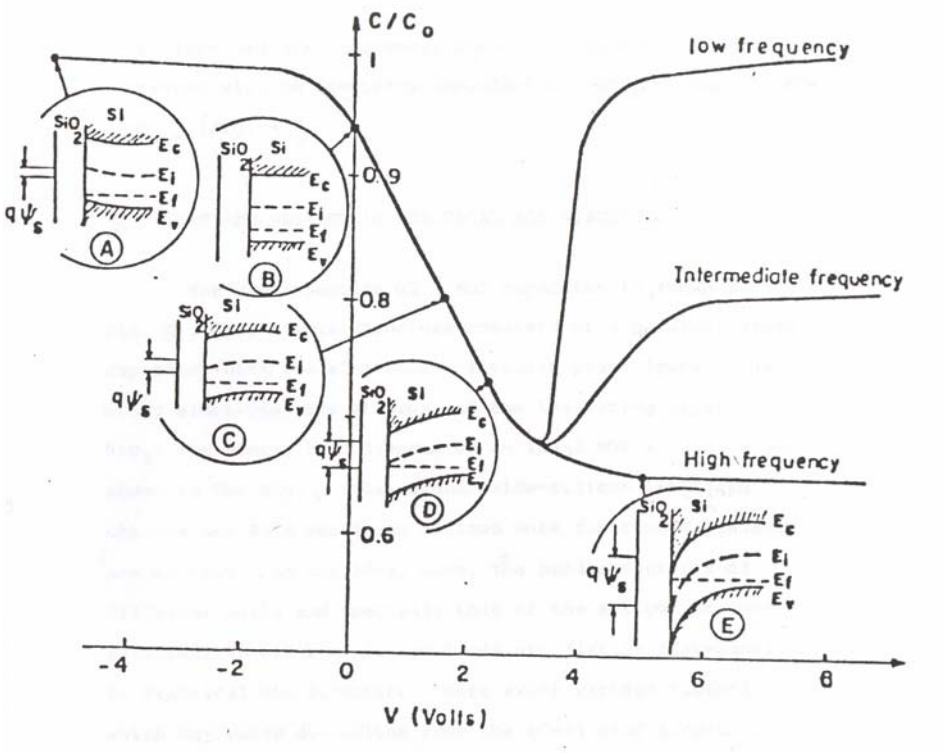


Fig.4.3 Capacitance-voltage characteristics of the ideal MIS structure with energy band structures corresponding to different gate voltage regions.

At low frequencies, the charge modulation in the depletion region is satisfied by the inversion layer, near the film/substrate interface and the resulting capacitance of the MIS system is equal to that of accumulation region, $C=C_{ins}$(fig.4.3)

At high frequencies, the minority carriers can not follow the ac gate voltage excitation, and the required charge modulation for total charge neutrality will be satisfied by the majority carriers flowing in and out of the boundary between the depletion layer and the bulk of silicon. As a result the capacitance of the MIS system, at high frequency, reaches its minimum value C_{min}, which is the depletion layer capacitance C_{dm}, in series with the insulator capacitance C_{ins} (fig.4.2-c and 4.3):

$$C_{\min} = \left[1/C_{ins} + 1/C_{dm}\right]^{-1} \qquad (4.13)$$

At intermediate frequencies, the capacitance of the MIS system will be frequency dependent situated between C_{ins} and C_{min} (fig.4.3).

4-1-3 Local charges obtained from the Flat Band Voltage

The energy band diagram of an ideal MIS structure is shown in fig. 4.4. Here insulator and insulator/semiconductor interface charges and gate metal and silicon work function differences are ignored.

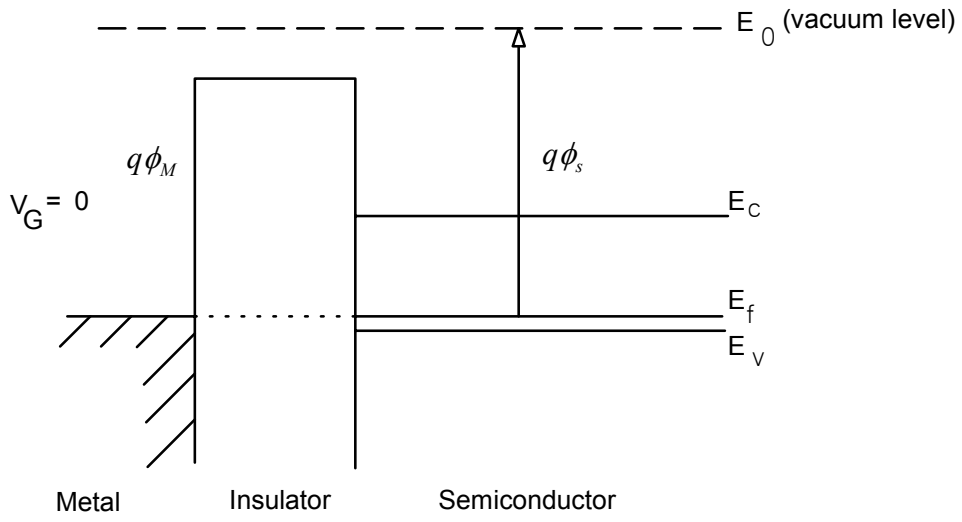


Fig. 4.4 Energy band diagram of an ideal MIS capacitor.

In the ideal case, the band structures of different parts and specially that of the silicon are not affected; in other words, the bands are flat (≡ flat-band). On the contrary, in practical MIS structure, there exist various factors which may cause deviations from the ideal band structure of a MIS structure. A rough classification of these factors may be presented as follows:

a) the work function ϕ_m of the gate metal is different from the work function of ϕ_s of silicon; this leads to a band bending at the surface region of silicon at the equilibrium as shown in fig.4.5-(a)

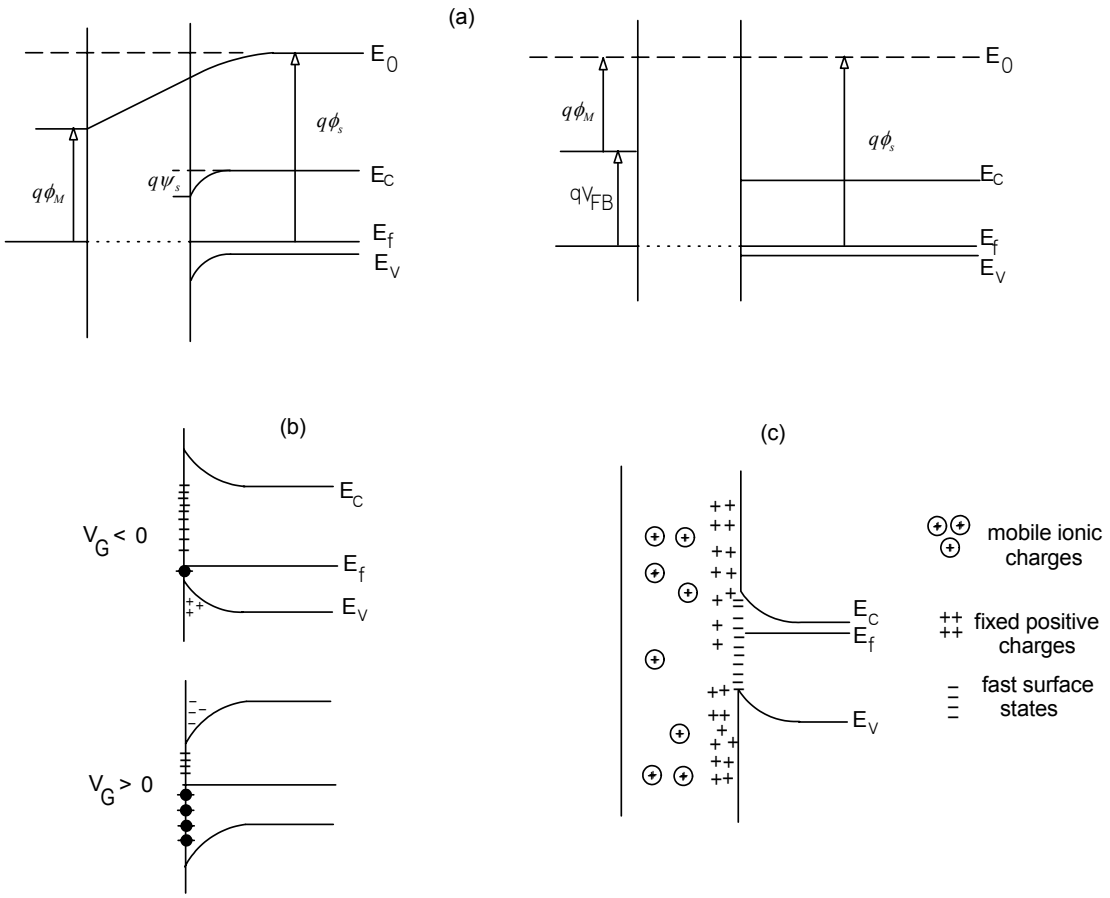


Fig.4.5 (a) Effect of the work function difference, (b) Effect(s) of V_G on the occupancy of fast surface states through relative shift of E_F at the interface, (c) Recapitulation of various local charges within a MIS structure.

(When the metal of MIS structure is shorted to the silicon, electrons will flow from metal to the semiconductor or vice versa until a potential will be built up between the two which counterbalance the difference in work functions; in other words the Fermi level will be aligned). To reach again the flat band condition of the ideal case, an amount of gate voltage V_{FB} should be applied (fig.4.5(a,b)):

$$V_{FB} = \phi_m - \phi_s = \phi_{ms} \tag{4.14}$$

(b) both fixed and mobile ionic charges located within the insulator (fig.4.6): a charge sheet of magnitude Q per unit area, located at a distance x from outer

surface of insulator layer, will induce opposite charges both at the silicon and metal interfaces.

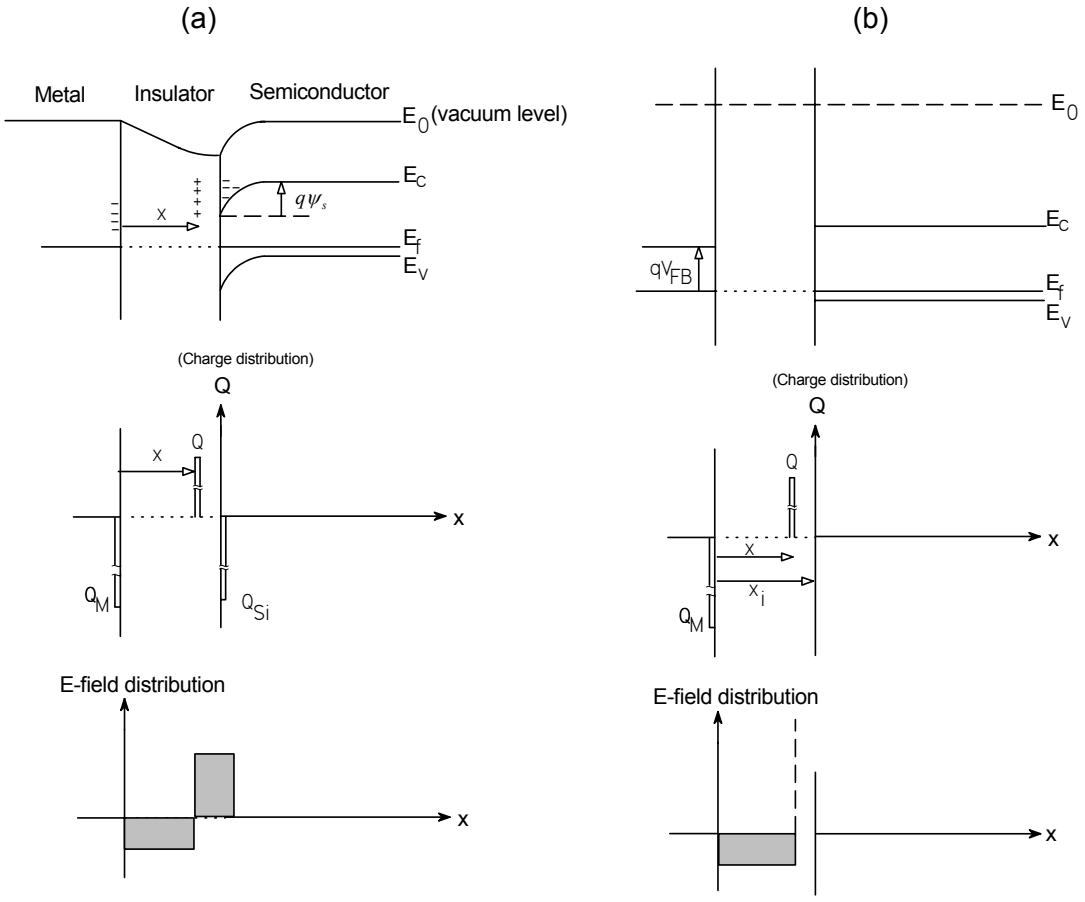


Fig. 4.6 Effect of changes within the insulator, (a) without applied gate bias (i.e., V_G=0), (b) V_G=V_{FB} ≠ 0

The induced charge distribution at the silicon surface region will lead to the development of potential distribution in this region according to the Gauss law; in other words, the energy bands are bent, with a maximum band bending $q\psi_s$ at the interface. For reestablishing charge neutrality or flat band condition at the silicon surface (Q_s), a certain voltage, called flat band voltage, V_{FB}, should be applied to the gate: $V_{FB} = -xQ/\varepsilon_{ins}$. As a result, V_{FB} depends both on the density and on the location of sheet charge Q within the insulator; when Q is next to gate metal V_{FB}=0, when Q is located next to the semiconductor, it will lead to a maximum flat band

voltage: $V_{FB} = -x_0\, Q/\varepsilon_{ins}$. If there is distribution of charges throughout the insulator layer of volume density $\rho(x)$, the corresponding flat band voltage may be obtained by taking the integral of the relation:

$$V_{FB} = -\frac{1}{\varepsilon_{ins}} \int_0^{x_0} x\rho(x)dx \tag{4.15}$$

(c) fixed positive surface state charge density which is located near insulator/semiconductor interface in the insulator (within ~ 30 Å) and whose energy levels lie outside of the forbidden badgap of silicon and thus they are permanently ionized independently from the applied gate voltage V_G. These charges are generally positive, their density depend on growth condition, annealing conditions and silicon orientation. The corresponding flat band voltage will be given by the relation (4.16)

$$V_{FB} = -x_0\, Q_{ss}/\varepsilon_{ins} \tag{4.16}$$

with Q_{ss} = charges per unit area. The total flat band voltage due to the work function difference ϕ_{ms} , ionic charge density $\rho(x)$ and fixed surface state charge density Q_{ss} can be written as follows:

$$V_{FB} = \phi_{ms} - x_0\, Q_{ss}/\varepsilon_{ins} - \frac{1}{\varepsilon_{ins}} \int_0^{x_0} x\rho(x)dx \tag{4.17}$$

The effect of ionic charge can be considered to be that of an “effective” interface charge density Q''_{ss} , in addition to the actual value of Q_{ss} so that:

$$Q''_{ss} = -\frac{1}{\varepsilon_{ins}} \int_0^{x_0} x\rho(x)dx\ ,\ Q'_{ss} = Q_{ss} + Q''_{ss}\ ,\ V_{FB} = \phi_{ms} - x_0\, Q'_{ss}/\varepsilon_{ins} \tag{4.18}$$

d) fast surface states which are located at the insulator/semiconductor interface due to the interruption of the periodic lattice structure at the surface of a crystal. The energy levels of these states fall within the silicon band gap, consequently the probability of occupancy of a level E will depend on the Fermi Dirac distribution:

$$f(E) = 1/(1 + \exp[E - E_F/kT]) \qquad (4.19)$$

As the difference E-E_F depends on the band bending magnitude, the occupancy of E will vary as a function of the gate voltage V_G (fig.4.5-b). These fast surface states will have more or less effect on the flat band voltage following their charge sensitivity varying as a function of the gate voltage (Various sort of insulator and interface charges are schematically shown in fig. fig.4.5-c).

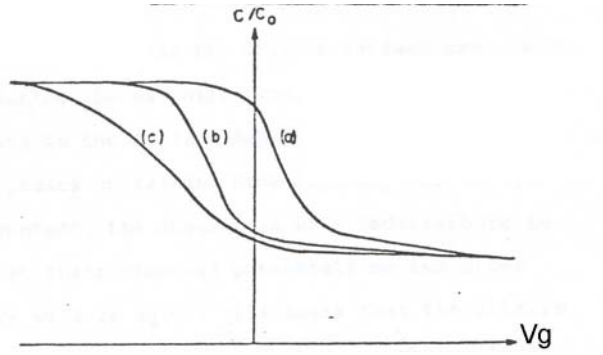


Fig. 4.7 Capacitance-voltage characteristics of the non-ideal MIS structure.

The capacitance-voltage characteristics of a practical MIS structure is deviated from the ideal capacitance-voltage characteristics shown in fig.4.7-a by various factors cited and roughly discussed before: work function difference, insulator charges and fixed positive surface states will shift parallely the ideal characteristics along the voltage axis (fig.4.7-b) but the effect of fast surface states will alter the shape of the C-V curve since the amount of charges in these states depends on the gate voltage as previously discussed (fig.4.7-c).

These fast surface states apart from their effect of the flat band voltage (dc effect) can be charged and discharged in response to a gate voltage modulation; as a result they represent a capacitance component C_{ss} parallel to the depletion capacitance but the relaxation time ($\tau = C_{ss}R_{ss}$) of these states is very long and they respond only at low frequency. The equivalent circuit of the MIS structure including fast surface state effect is represented in fig.4.8.

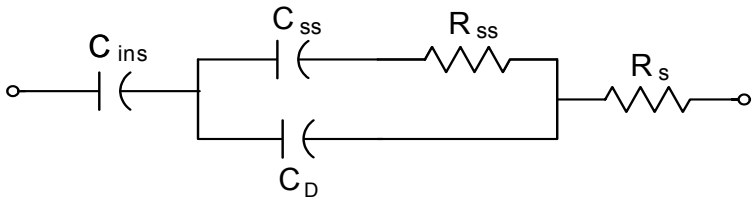


Fig.4.8 Equivalent circuits MIS structure having surface states.

It is remarkable that all C-V curves are shifted toward the negative gate voltages. From the magnitude of the flatband shift of the C-V curve, the effective density of interface charges can be determined as discussed in detail before.

4-1-4 Evaluation of Dopants by high frequency C-V Measurement

The ionized dopant impurity profile is obtained by the slope of a $(1/C_m^2)$ versus V_G curve, where C_m is the capacitance measured in depletion at gate bias V_G. When an incremental charge density dQ_G is added to the gate of MIS capacitor, the depletion layer edge x_d changes an amount of dx_d, then the ionized dopant impurity density at the depletion layer edge, an average distance x_d from the silicon surface, is $N(x_d)$ within dx_d at the depletion layer edge:

$$dQ_G = -qN(x_d)dx_d \qquad (4.20)$$

Average ionized dopant impurity density around the position x_d can be calculated from this equation if dQ_G and dx_d are known; dx_d can be obtained from the measured capacitance C_m and the gate bias change, dV_G that is

$$dQ_G = C_m dV_G \qquad (4.21\text{-a})$$

$$C_m^{-1} = C_{ins}^{-1} + C_d^{-1} \qquad (4.21\text{-b})$$

where C_{ins} is the insulator capacitance and C_d is the depletion capacitance (as given before). The determination dx_d can be done as: $dx_d = \varepsilon_s A d(1/C_{ins} + 1/C_d) = \varepsilon_s A d(1/C_m)$. By equating the relations (4.20) and

(4.21-a), $dQ_G = -qN(x_d)dx_d$ =$C_m dV_G$= $-qN(x_d)\varepsilon_s A d(1/C_m)$ and solving for N(x_d) yields

$$N(x_d) = 2\left[q\varepsilon_s A^2 \frac{d}{dV_G}\left(1/C_m^2\right)\right]^{-1} \tag{4.22}$$

with the corresponding value of x_d is found by rearranging (4.21-b) as

$$x_d = \varepsilon_s\left[C_m^{-1} - C_{ins}^{-1}\right] \tag{4.23}$$

The real distribution of impurities was determined experimentally by this method (shown below).

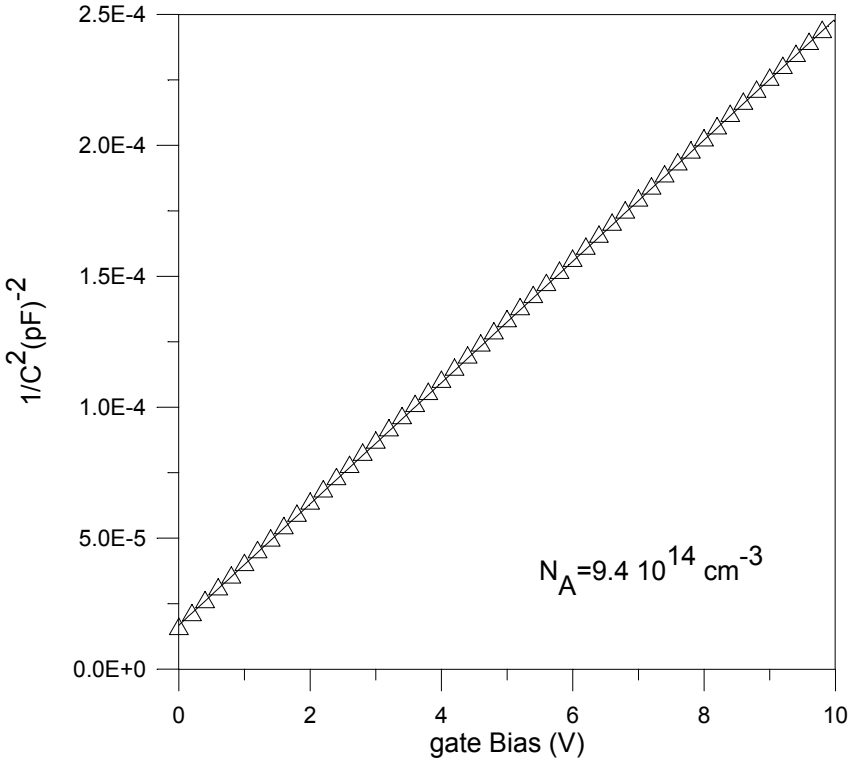


Fig. 4.9 Doping density of Al/p-Si Shottky diode.

CHAPTER 5

DENSITY OF STATES (DOS) AT INSULATOR/SEMICONDCUTOR INTERFACE OF MIS STRUCTURE

5-1 DOS by Steady State Capacitance (High-Low)

5-1-1 Introduction

Device based techniques such as ac admittance and DLTS measurements were carried out on MIS structure due to the fact that it is both the backbone of transistors and powerful tool to study the localized charge distribution at the interface which plays an important role in electronic applications. At the interface, inevitable local defects (≡ interface traps with capture cross section and density) discussed in chapter 4 exists that alters the properties of MIS capacitor. When the test signal with a high measuring frequency is applied on the metal side, the charge carrier exchange between interface traps and the relevant band cannot occur rapidly, so no contribution occurs to the measured capacitance. On the other hand, for low frequencies, interface traps has enough time to contribute to the measured capacitance. Based on the information above, interface trap density can be studied by comparing the measured capacitances at low and high frequencies, namely High-Low frequency C-V measurements that proposed first by Castagne and later used by Castagne and Vapaille [43]. It is a steady state technique and only interface trap distribution could be obtained via application of mentioned technique. Other dynamic parameter of interface trap (such as capture cross section) can be obtained via ac conductance and DLTS techniques (discussed in the next chapter).

5-1-2 Expression of DOS

C-V technique has been powerful tools in the study of MIS structures to study the electrical properties of interface states. After applying the test signal to MIS structure, the measured differential capacitance will be $C = dQ/dV_G$. As long

as the ac voltage can be considered a ‘ small signal’ (i.e., the current response is linear with the voltage), the measured capacitance C ;

$$C = \frac{dQ}{dV_G} = \frac{dQ}{d\psi_s}\frac{d\psi_s}{dV_G} \tag{5.1}$$

Applied gate voltage on the front contact of MIS structures should be counter balanced by the charges situated at the interface and in the silicon semiconductor. Qualitatively, $Q_m = -(Q_s + Q_{ss})$. For a small, infinitestimal change in gate bias, dV_G, turns the expression as: $\frac{dQ_m}{dV_G} = \frac{dQ_m}{d\psi_s}\frac{d\psi_s}{dV_G}$. Provided that the measuring frequency is low enough, both interface and semiconductor charges can contribute and hence $\frac{dQ_m}{dV_G} = \frac{d(Q_s + Q_{ss})}{d\psi_s}\frac{d\psi_s}{dV_G} = C_{LF} = (C_D + C_{ss})\frac{d\psi_s}{dV_G}$ with $C_D = dQ_s / d\psi_s$ (depletion capacitance) and $C_{ss} = dQ_{ss} / d\psi_s$ (interface state capacitance), respectively. To relate the surface band bending, both Gauss’s law and infinitestimal gate bias changes have to be considered:

$$\frac{d\psi_s}{dV_G} = \frac{C_{ins}}{C_{ins} + C_D + C_{ss}}. \tag{5.2}$$

Then the measured capacitance at low frequency will be

$$C_{LF} = \frac{(C_D + C_{ss})C_{ins}}{C_D + C_{ss} + C_{ins}} \tag{5.3}$$

On the other side, at high measuring frequency, no contribution comes from Q_{ss}, in other words, $Q_{ss} \rightarrow 0$, then the above expression turns out to be

$$C_{HF} = \frac{C_{ins}C_D}{C_D + C_{ins}} \tag{5.4}$$

Extracting the depletion capacitance from the measured high frequency capacitance from the relation (5.4) and inserting into eqn.(5.3) yields the interface state capacitance ($C_{ss}=qN_{ss}$) as;

$$C_{ss} = qN_{ss} = \left[1/C_{LF} - 1/C_{ins}\right]^{-1} - \left[1/C_{HF} - 1/C_{ins}\right]^{-1} \quad (5.5)$$

Surface band bending as a function of gate bias could also be determined to relate interface state distribution in the silicon band gap through low frequency C-V measurement. Integrating both side of relation (5.2) from flat band voltage towards to strong accumulation and inversion sides leads to variation of band bending as a function of gate bias;

$$\psi_s(V_G) = \int_{V_{FB}}^{V_G} \left(1 - \frac{C_{LF}}{C_{ins}}\right) dV_G \quad (5.6)$$

Then, interface state distribution in the silicon band gap will be

$$E_T - E_V = kT \ln\left(N_A/n_i\right) + q\psi_s \quad (5.7)$$

Moreover, the effective interface state density N_{ss} around the flatband capacitance C_{FB} can be adopted via the following relation [44]

$$N_{ss} = A^{-1}\left[\frac{C_{FB}\left(C_{ins} - C_{FB}\right)}{3qkT\left.\frac{dC}{dV_G}\right|_{FB}} - \frac{C_{ins}^2}{q^2\left(C_{ins} - C_{FB}\right)}\right] \quad (5.8)$$

5-2 DOS by ac Conductance

5-2-1 Introduction

Dispersion of the capacitance can be used to obtain information about the energy distribution and density of interface states in MIS capacitor. However, the capacitance technique has severe limitations; especially, the difficulty arises while extraction of interface state capacitance from the measured one which consists of insulator capacitance, depletion layer capacitance and interface state capacitance (see eqn. 5.3 in section 5.1). Fortunately, the above mentioned difficulties does not apply to the equivalent parallel conductance because conductance arises solely

from the steady state loss due to the capture and emission of carriers by interface states. Let us look at the loss phenomenon closely; applied small signal stimulus consists of positive and negative half cycle; in the first half cycle, valance bands moves towards the Fermi level, yielding the increase of the average energy of holes in the silicon. Holes at a higher average energy in the silicon will be captured by interface states at a lower average energy, resulting in energy loss. On the other half of the ac signal, conduction band moves towards the Fermi level. Holes in filled interface states now will be at a higher average energy than in silicon. As holes are emitted by the interface states into the silicon, they will lose energy again. Thus there will be an energy loss on both halves of the ac signal and seen as conductance peaks in the admittance measurement.

The admittance derivation of MIS capacitor is given in Appendix A. This derivation includes first an hypothetical single energy traps (single level model), then it is extended to the more realistic distributed energy traps (continuum model), finally it is completed by Gauss like space distributed traps (statistical model). The expression of the conductance $\langle G_p \rangle / \omega$ (hereafter it is denoted only $\frac{G_p}{\omega}$ for simplicity throughout the text) corresponding to the last case is resumed below as the most optimized approach:

$$\frac{G_p}{\omega} = \frac{qN_{ss}\left(2\pi\sigma_s^2\right)^{-1/2}}{2\xi} \int_{-\infty}^{+\infty} \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) \exp(-\eta) \ln\left(1+\xi^2 \exp(2\eta)\right) d\eta \quad (5.9)$$

where N_{ss} surface state density, $\eta = u_s - \overline{u}_s$ (with $u_s = e^{\frac{q\psi_s}{kT}}$), ψ_s = surface band bending, $\xi = \omega\tau_p = \omega\left(c_p N_A\right)^{-1} \exp\left(\overline{u}_s\right)$ (with c_p= majority carrier capture coefficient, N_A= majority doping density), σ_s is the variance of band bending in terms of kT/q.

5-2-2 Experimental Consideration

One should keep in mind that G_p/ω is not a measured quantity directly from the measured conductance G_m and capacitance C_m which contain also series resistance R_s (due to both the bulk of silicon and contacts) and insulator

capacitance C_{ins}, effect. To get rid of their effect and to extract the G_p/ω, the following equation has to be considered [45-47]:

$$\frac{G_p}{\omega}=\frac{\omega C_{ins}^2\left(G_m-\omega C_m^2 R_s-R_s G_m^2\right)}{\left(\omega^2 C_{isn} R_s C_m\right)^2+\omega^2\left(C_{ins}-C_m-C_{ins} R_s G_m\right)^2} \qquad (5.10)$$

where R_s and C_{ins} are determined from the measured capacitance and conductance in strong accumulation; $R_s=G_{ma}/\left(G_{ma}^2+\omega^2 C_{ma}^2\right)$ with G_{ma} and C_{ma} are the measured values of conductance and capacitance in the accumulation region.

Surface state parameters (density , capture cross section and position in the energy gap) could be extracted both from G_p/ω vs. $\ln\omega$ or G_p/ω vs. V_G curves, where the former will be discussed in Nicollian approach and the latter in Brews approach, respectively. Relation 5.9 gives the conductance as a function of the frequency with three parameters: N_{ss}, σ_s and τ which are implicit function of $\overline{u}_s$. Crucial step in conductance analysis is the determination of standard deviation σ_s of band bending (u_s) which is a measure of the width (difference of ω_p and 5 ω_p or 1/5 ω_p) of the G_p/ω vs. $\ln\omega$ curve at the peak position of frequency (ω_p) according to Nicollian's way [48]:

$$\frac{\left(G_p/\omega\right)_{n\omega_p}}{\left(G_p/\omega\right)_{\omega_p}}=n\frac{\int_{-\infty}^{+\infty}\exp\left(-\frac{\eta^2}{2\sigma_s^2}\right)\exp(-\eta)\ln\left(1+\xi_p^2\exp(2\eta)\right)d\eta}{\int_{-\infty}^{+\infty}\exp\left(-\frac{\eta^2}{2\sigma_s^2}\right)\exp(-\eta)\ln\left(1+\xi_p^2\exp(2\eta)\right)d\eta} \qquad (5.11)$$

with n=5 or 1/5 and ξ_p is the maximum value of ξ. The relation 5.11 is not able to be solved numerically unless ξ_p as a function of σ_s is known. Actually, this variation can be determined by taking the derivative of relation 5.9 as ξ a parameter at ω_p and equating to zero, equivalently, $\left(\frac{d\,G_p/\omega}{d\xi}\right)_{\omega_p}=0$, then ξ_p versus σ_s can be obtained by taking the numerical integration of the relation given below;

$$\int_{-\infty}^{+\infty} \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right)\exp(-\eta)\left[\frac{2\xi_p^2\exp(2\eta)}{1+\xi_p^2\exp(2\eta)} - \ln\left(1+\xi_p^2\exp(2\eta)\right)\right]d\eta = 0 \qquad (5.12)$$

The conductance expression given in 5.9 can also be expressed as

$$\frac{G_p}{\omega} = qN_{ss}f_D(\sigma_s) \qquad (5.13\text{-a})$$

with $f_D(\sigma_s) = \dfrac{\left(2\pi\sigma_s^2\right)^{-1/2}}{2\xi}\int_{-\infty}^{+\infty}\exp\left(-\dfrac{\eta^2}{2\sigma_s^2}\right)\exp(-\eta)\ln\left(1+\xi^2\exp(2\eta)\right)d\eta$ (5.13.b)

Reporting ξ_p as a function of σ_s leads a chance to compute $f_D(\sigma_s)$ by again numerical analysis. Moreover, the ratio (given in 5.11) can also be expressed in terms of $f_D(\sigma_s)$ and after a little algebra, the following relation is obtained. This relation is exclusively σ_s dependent and it bridges the variable with the experimentally measurable quantities after numerically solved:

$$\int_{-\infty}^{+\infty}\exp\left(-\frac{\eta^2}{2\sigma_s^2}\right)\exp(-\eta)\ln\left(1+\xi^2\exp(2\eta)\right)d\eta - 2\sqrt{2\pi}\left(n\sigma_s\xi_p f_D\right)\frac{\left(G_p/\omega\right)_{n\omega_p}}{\left(G_p/\omega\right)_{\omega_p}} = 0 \quad (5.14)$$

One should keep in mind that while determination of N_{ss}, τ_p and c_p, the procedure (given above) is in reversed order. In other words, first, σ_s has to be determined and then corresponding ξ_p and $f_D(\sigma_s)$ are obtained in Nicollian approach. Interface trap is calculated via the relation 5.13-a at ω_p of G_p/ω vs. $\ln\omega$ curve. Knowing ψ_s (from the relation 5.6 given in section 5.1) leads to τ_p and c_p easily.

The method (discussed above) involves locating conductance maxima accurately, which is inherently difficult for broad maxima and is a serious source of error. Brews pointed out this difficulty [49] and proposed an alternative method (known as Brews approach) where to find σ_s, the width of G_p/ω peak is estimated which is an arbitrary fraction of G_p/ω maximum:

$$G_p/\omega = \left(G_p/\omega\right)_{\omega_p} f_w \qquad (5.15)$$

where $\left(G_p/\omega\right)_{\omega_p}$ is the maximum value of G_p/ω and f_w is the chosen fraction of the width such as 0.3-0.9.

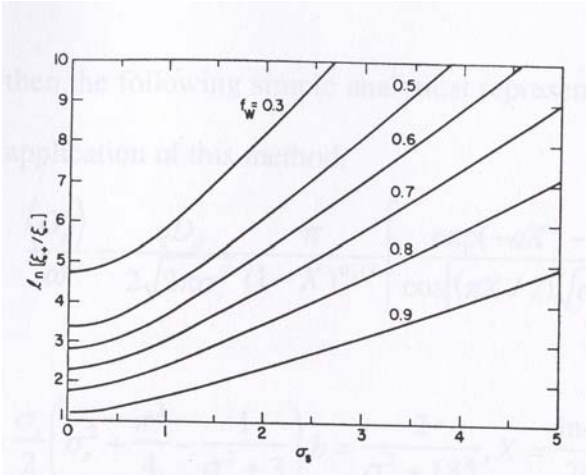


Fig.5.1 Experimental conductance curves width parameter as a function of broadening for various choices of the fractional value for the width, fw.

In the original work [49], σ_s is reported as a function of $\ln\left(\xi^+/\xi^-\right)$ (where ξ would be either frequency or band bending) with various f_w(see in fig.5.1). As a result in Brews approach after determining σ_s, the rest of the procedure is the same as the previously given Nicollian's one.

Though the conductance methods is believed to be the most complete method to probe the interface traps due to its high sensitivity and accuracy, it is extremely time consuming since G_p/ω vs. $\ln\omega$ or (V_G) family of curves is necessary. Fortunately, Yadava presented a new method in which G_p/ω vs. (V_G) measurements at just two frequencies is sufficient [50].In this way, conductance analysis for rapid characterization of the interface is a simple and straightforward affair, and the amount of data necessary is substantially reduced. Yadava opposed the following relation instead of eqn.5.9:

$$G_p\Big/\omega = \frac{qD_{it}}{2\left(2\pi\sigma_s^2\right)^{1/2}}\frac{\pi}{\left(1-X\right)^{\sigma_s/2}}\left\{\frac{\exp\left[-aX^2-b\right]}{Cos\left[\frac{\pi X}{2}\left(\frac{\sigma_s}{2}\right)^{1/2}\right]}\right\} \qquad (5.16)$$

where $|X|<1$ and $a=\frac{\sigma_s}{2}\left(\sigma_s^2+\frac{\pi^2}{4}-\frac{1}{\sigma_s^2+3}\right)$, $b=\frac{2}{\sigma_s^2+1.85}$, $X=\frac{\ln(\xi)}{2\sigma_s^2}=\frac{\ln(\omega^2)}{2\sigma_s^2}$

In the last method, G_p/ω values at two frequencies and the two values of band bending has to be determined. Band bending values, u_{s1} and u_{s2} (=$u_{s1}+\Delta u$) should be selected close enough so that σ_s should not vary significantly in between. Using G_p/ω vs. u_s (determined via relation 5.6 as a function of gate bias) curves at two frequencies ω_1 and ω_2, σ_s is obtained by solving the relation below:

$$\ln(R_1/R_2)=\frac{1}{\sigma_s}\left[\frac{1+0.7337(\sigma_s^2+1.637)}{\sigma_s^2(\sigma_s^2+3)}\right]\Delta u\ln\left(\frac{\omega_1}{\omega_2}\right) \qquad (5.17)$$

where $R_{1,2}=\frac{(G_p/\omega)_{\omega_1}}{(G_p/\omega)_{\omega_2}}$ for biases u_{s1} and u_{s2}, respectively. The analytical expression of R_1 at band bending u_{s1} is:

$$R_1=\frac{(1-X_{21})^{\sigma_s/2}Cos\left[\frac{\pi X_{21}}{2}\right]\left(\frac{\sigma_s}{2}\right)^{1/2}}{(1-X_{11})^{\sigma_s/2}Cos\left[\frac{\pi X_{11}}{2}\right]\left(\frac{\sigma_s}{2}\right)^{1/2}}\exp\left[-a\left(X_{11}^2-X_{21}^2\right)\right] \qquad (5.18)$$

with $X_{11}=\frac{\ln(\omega_1\tau_1)}{2\sigma_s^2}$, $X_{21}=\frac{\ln(\omega_2\tau_1)}{2\sigma_s^2}$

Solving the relations 5.17 and 5.18 numerically (by inserting experimental values of R_1, ω_1, ω_2 and σ_s), it is possible to report τ_p as a function of σ_s. As for interface state density, it is determined via numerical solution of the eqn. 5.16 once substituting both G_p/ω at ω_1 and calculated values of τ_{p1} and σ_s.

It has to be remembered that though it was an expedient form of Nicollian and Brews approach, the relation 5.16 is merely approximations to the exact behavior. In this sense, the results must be accepted as approximations to a full scale calculation compared to others.

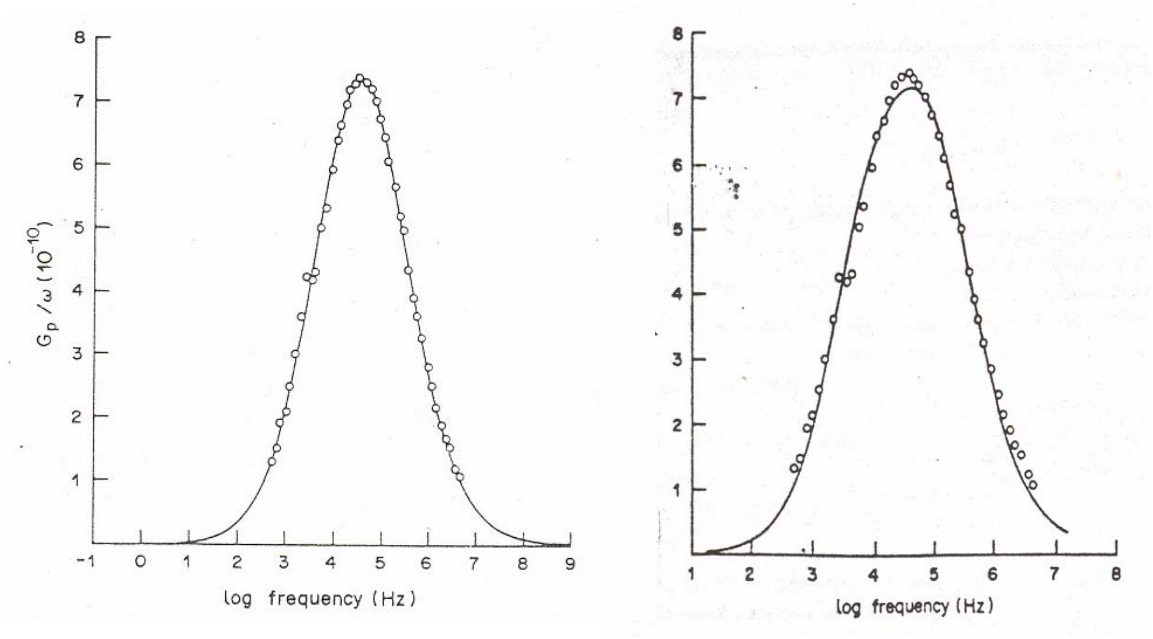
5-3 Alternative model

5-3-1 Introduction

An alternative explanation for the time constant dispersion was proposed by Preier, based on a model developed by Heimann and Warfield [51] where the interface states are supposed to be distributed in three dimensions, extending some way into the insulator itself, rather than the 2-D picture assumed by SRH statistics as in the case of statistical model (Appendix A). Thus electrons can tunnel from the semiconductor into insulator. Preier derived the parallel conductance for surface states as [52]:

$$\frac{G_p}{\omega} = qN_{ss}\int_0^d \frac{\ln\left[1+\left(\omega\tau\exp(2Kx)\right)^2\right]}{2\omega\tau\exp(2Kx)} \qquad (5.19)$$

where d is the effective tunneling distance for carriers, x is the distance in insulator measured as to interface, K is the wave vector of the carriers inside the insulator and τ is defined as the time constant of the states at the interface. The exchange of carriers between localized states around the interface (≡ interface states) and the relevant band of the semiconductor extended states has been interpreted mainly by both the statistical [48,53] (Appendix A) and tunneling [54] models Both models have successfully described the experimental broad time constant dispersion of the interface states (see in fig.5.2); the former introduces a statistical distribution of interface local charges leading to a fluctuation of semiconductor potential ψ_s which, in turn, is behind the time constant dispersion [48] through the fluctuation of interface free carrier density p_s (see Appendix A). The latter assumes the exchange of free carrier by tunneling between the semiconductor band and the localized states within the insulator more or less distant from the interface, leading to a spectrum of time constants due to the exponential decay of effective cross section as a function of tunneling distance x_t [51,54].



(a) (b)

Fig. 5.2 Measured Gp/w against frequency with best fit to the (a) statistical model (eqn.5.9), (b) tunneling model to the same data (eqn. 5.19) [52].

However, under accumulation bias regime, the admittance which is expected to remain independent of frequency apart from the effect of parasitic series resistance R_s [48], in agreement with the above mentioned two models, exhibits substantial frequency dispersion for some dielectrics [55,56]. For a bit more clarity, MIS structure under the accumulation bias regime may be considered equivalent to a metal-insulator-metal(≡ MIM) structure [57]

$$\delta I = \delta I_p + C_G \frac{d}{dt}(\delta V) - \frac{A}{W}\int_0^W \frac{\partial}{\partial_t}(\delta P)dx + A\int_0^W \left(1-\frac{x}{W}\right)\frac{\partial}{\partial_t}(\delta\rho)dx , \quad (5.20)$$

where the first term δI_p is the particle current (eventual dc leakage), the second term represents the displacement current (which would flow if there were no material present (C_G= geometrical capacitance= ε A/W with ε = dielectric constant, A= electrode area, W= insulator width); the third term accounts for the polarization phenomena which are the characteristic of the neutral insulator material itself (P= polarization which would be behind the frequency dependence of the dielectric constant) [57]; and the fourth term would arise from the space regions of charge density, ρ generally located near interfaces.

An eventual frequency dependence of the MIS admittance resulting from the dc leakage should vary as $\frac{1}{\omega^2}$ which would be easily tested. For the case of dielectric dispersion, it is observable either at high temperature or very low frequency measurements [56,58-60]. A possible factor behind the frequency dispersion of accumulation admittance would be due to the last term given in the relation (5.20). A serious attempt of model, based on the tunneling mechanism has been tried to account for the mentioned frequency dispersion [61]. Let us outline this model [45-47,62].

5-3-2 Theoretical Outline

The accumulation bias on the MIS structure will permit pile up of majority carriers at the interface in the semiconductor if the insulator is relatively resistant and free of pinholes, preventing the accumulated carriers from leaking off through the insulator. However, the exchange of carriers by tunneling between the accumulation region in the relevant band edge and the traps inside the insulator at the same energy is unavoidable. This depicted in Fig 5.3-a using the energy band diagram of the MIS capacitor biased in accumulation. This tunneling transition through a finite height energy barrier has been treated in detail [51]. The wave function $\varphi(\mathrm{x})$ of the penetrating carrier along the relevant band edge energy is expressed as $\varphi(\mathrm{x}) = \varphi_0 \mathrm{e}^{-\mathrm{K}_0 \mathrm{X}}$ where φ_0 = amplitude at the interface, and $\mathrm{K}_0^2 \approx \frac{2\mathrm{mU}}{\hbar^2}$ with U= amount of band discontinuity between the semiconductor and the insulator. On the other hand, τ_p^{-1}(=number of collisions that a free carrier might have with empty traps of density n_t in unit time) is expressed as $\tau_p^{-1} = \sigma_p \mathrm{v} n_t$ where v = carrier group velocity (which may be taken as thermal velocity), σ_p = capture cross sectional area. Moreover, the probability of a carrier impinging upon the insulator at the interface to be around the depth, x (between x and x+dx) is obtained by $\left[\varphi(\mathrm{x}) / \varphi_0\right]^2 = \mathrm{e}^{-2\mathrm{K}_0 \mathrm{X}}$.

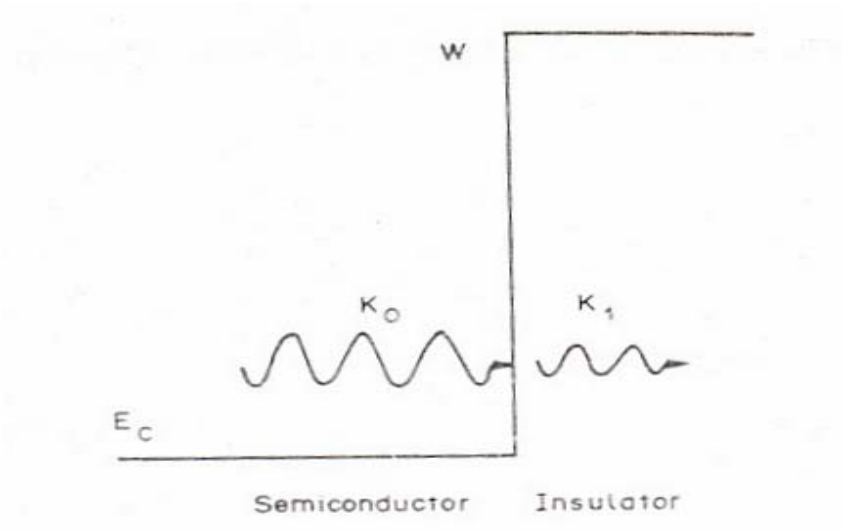


Fig.5.3 Representation of an electron in the bottom of the conduction band incident upon a potential barrier representing an insulator

In other words, a trap of capture cross section σ_p located in the insulator at a distance x from the interface may be viewed by a carrier at the interface as an effective interface trap with a "reduced" capture cross section σ_{px} by a factor $e^{-2K_0 X}$:

$$\sigma_{px} = \sigma_p \, e^{-2K_0 X}. \qquad (5.20)$$

Let us consider the incremental effective density of interface states dN_{ss}, "projected" from the insulator traps located around the both average position x from the interface and energy E_t between x/(x+dx) and $E_t/(E_t+dE_t)$ respectively. Assuming the exchange of carriers with the majority band only, the occupation rate of these effective interface states may be expressed as :

$$\frac{d}{dt}\left(dn_{ss}\right) = -\frac{dn_{ss}}{\tau_c} + \sigma_{px} v p_s dN_{ss} \; ; \; dn_{ss}(t) = (1-f) dN_{ss}\left(1 - e^{-\frac{t}{\tau_c}}\right), \qquad (5.21)$$

where f = Fermi-Dirac distribution for electrons = $\frac{p_1}{p_1 + p_s}$ with p_s = free carrier

concentration (here holes) at the interface, $p_1 \equiv N_v e^{-(E_t - E_f)/kT}$ and $\tau_c^{-1} = \dfrac{\tau_0^{-1} e^{-2K_0 x}}{1-f}$

with $\tau_0 = \left[\sigma_p v p_s\right]^{-1} =$ capture time for holes at the interface.

$$dn_{ss}(\infty) = (1-f)dN_{ss} \equiv N_t(x, E_t)\left[1 - f(E_t)\right]g(x, E_t)dx dE_t \approx N_t(1-f)dx dE_t, \quad (5.22)$$

where $N_t(x, E_t) \equiv$ space and energy distribution of insulator trap density; $g(x,E_t)$ gives the spatial deviation of trap occupancy from equilibrium value, depending on

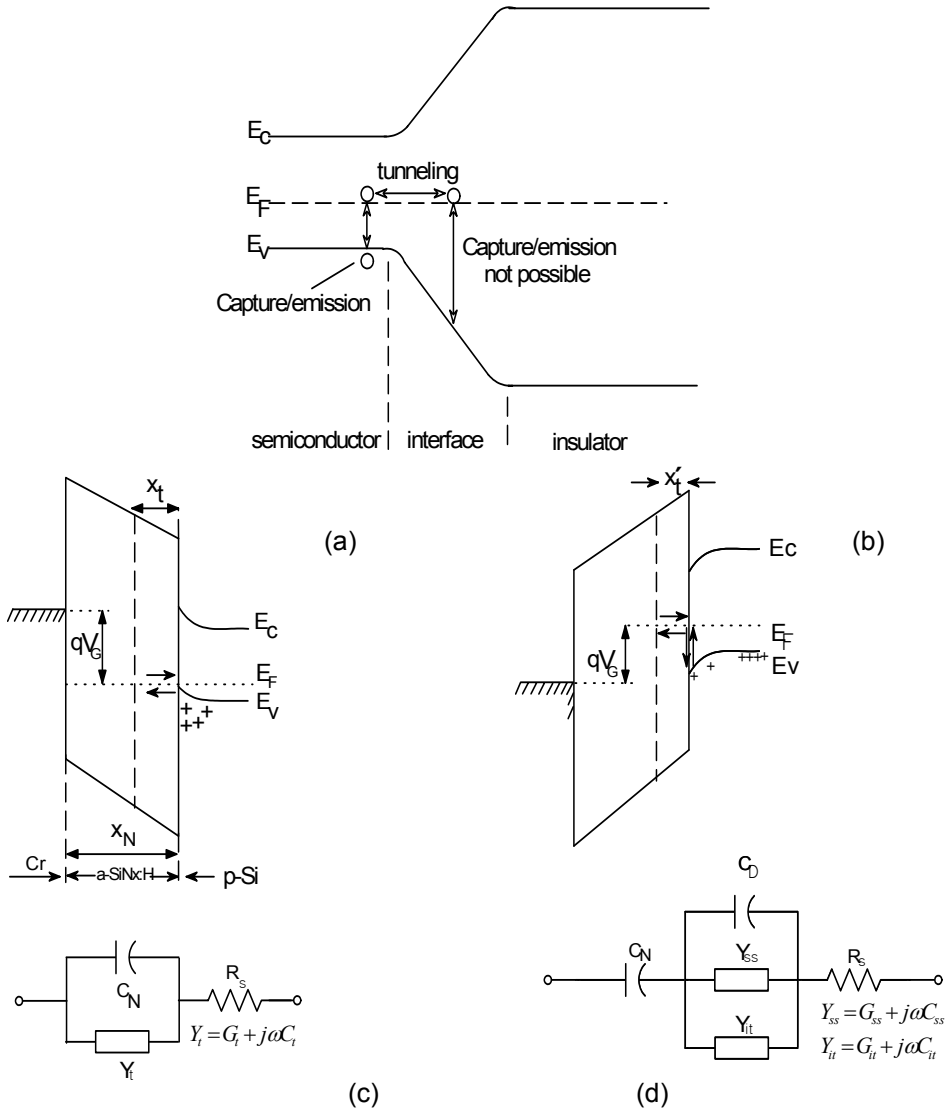


Fig.5.4 The schematic energy band diagram in accumulation bias regime (a) and in depletion bias regime (b) and their equivalent circuits (c) and (d), respectively.

the gate voltage application, all traps into a certain distance x_t may reach equilibrium [51]; in other words $g(x,E_t)$ abruptly changes from 1 to 0 at the position $x= x_t$.
As a result the total effective density of the interface states at a given gate bias V_G at thermal equilibrium may be approximated as follows:

$$n_{ss} = \int_0^{X_t} \int_{Ev}^{Ec} N_t(1 - f)\, dx dE_t \ , \qquad (5.23)$$

with E_c and E_v being conduction and valance band edges of the insulator respectively.

As the distribution of the electric field (by the way the gate voltage V_G) affects any energy level E_t lying across the insulator forbidden gap with respect to the semiconductor Fermi level E_F, the effective density of states N_{ss} is gate voltage dependent. When the gate voltage is incrementally changed from V_G to $V_G + \delta V_G$,by using the relations (5.21) and (5.22), the resulting first order incremental dynamical change of the effective density of states around the couple (x,E_t) may be expressed as :

$$\frac{d}{dt}\left\{\delta\left[dn_{ss}(t)\right]\right\} = - \frac{\delta(dn_{ss})}{\tau_c} + \frac{\delta N_{ss}}{\tau_0 e^{2K_0 X}} \ . \qquad (5.24)$$

If δV_G is a step like perturbation, the equilibrium modulation becomes :

$$\delta\left[dn_{ss}(\infty)\right] = - N_t \frac{\delta f}{\delta V_G} \delta V_G\, dE_t dx \, .$$

If $\delta V_G(t)$ $(\equiv a e^{j\omega t})$ is a small signal ac modulation type, $\frac{d}{dt}\left\{\delta\left[dn_{ss}(t)\right]\right\} = j\omega\delta\left[dn_{ss}(t)\right]$ leads to :

$$\delta\left[dn_{ss}\right] = d\left[\delta n_{ss}\right] = \frac{\delta f N_t dE_t dx}{1 + j\omega\tau_0(1-f)e^{2K_0 X}} \ , \qquad (5.25)$$

$$\frac{\delta n_{ss}}{\delta V_G} = \int_0^{x_t} \int_{Ev}^{Ec} \frac{\delta f}{\delta V_G} \frac{N_t\, dE_t\, dx}{1 + j\omega\, \tau_0 (1 - f)\, e^{2K_0 X}} \ . \qquad (5.26)$$

Assuming N_t independent of x, the above relation (5.23) takes the following form :

$$n_{ss} = x_t \int_{Ev}^{Ec} N_t (1 - f)\, dE_t = x_t n_{tb} \quad , \tag{5.27}$$

with $n_{tb} \equiv \int_{Ev}^{Ec} N_t(1 - f)\, dE_t$ gives the uniform trap density per unit volume. In light of this approximation, the potential distribution ψ (x) across the insulator between x= 0 (interface) x = x_t may be derived as follows:

$$\psi(x) = \frac{qn_{tb}}{2\varepsilon_N} x^2 + \frac{V_G - \psi_t - \psi_s}{x_N - x_t} x - \frac{qn_{tb}}{\varepsilon_N} x_t x + \psi_s \,, \tag{5.28}$$

$$\frac{d\psi(x)}{dV_G} = \frac{qx}{2\varepsilon_N}\left[\frac{x}{x_t} + \frac{x_t}{x_N} - 2\right]\frac{dn_{ss}}{dV_G} + \frac{x}{x_N} = -\frac{dE_t(x)}{qdV_G} \,, \tag{5.29}$$

where ε_N = insulator dielectric constant, x_N = insulator thickness, ψ_s = potential at x =0 (interface). For the potential ψ_t at $x = x_t$, it has the following expression:

$$\psi_t = -\frac{qn_{ss}}{2\varepsilon_N} x_t\left[1 - \frac{x_t}{x_N}\right] + \frac{x_t}{x_N}(V_G - \psi_s) \,, \tag{5.30}$$

$$\frac{\delta\psi_t}{\delta V_G} = -\frac{qx_t}{2\varepsilon_N}\left(1 - \frac{x_t}{x_N}\right)\frac{\delta n_{ss}}{\delta V_G} + \frac{x_t}{x_N}\left[1 - \frac{\delta\psi_s}{\delta V_G}\right] \tag{5.31}$$

The measured admittance Y_m of the MIS structure at hand is defined as follows:

$$Y_m = \frac{\left(\frac{\delta Q_G}{\delta t}\right)}{\delta V_G} = \frac{\left\{\frac{\delta Q_G}{\delta V_G}\frac{\delta V_G}{\delta t}\right\}}{\delta V_G} = j\omega\,\frac{\delta Q_G}{\delta V_G} \tag{5.32}$$

From Gauss law :

$$Q_G = -\left[Q_t + Q_s\right] = \varepsilon_N F_N = \varepsilon_N \frac{\left(V_G - \psi_t - \psi_s\right)}{x_N - x_t} \,, \tag{5.33}$$

where Q_t and Q_s are charge densities per unit area of the insulator and the semiconductor, respectively.

Using the relations (5.31) and (5.33), $\frac{dQ_G}{dV_G}$ may be expressed as follows :

$$\frac{\delta Q_G}{\delta V_G} = \frac{\varepsilon_N}{x_N}\left[1 + \frac{q x_t}{2\varepsilon_N}\frac{\delta n_{ss}}{\delta V_G} - \frac{\delta \psi_s}{\delta V_G}\right]. \qquad (5.34)$$

From now on, the accumulation and the depletion bias regimes should be analyzed separately in order to be able to consider simplifying assumptions.

5-3-3. Accumulation Bias Regime

Taking into account the slight variation of the interface potential ψ_s as a function the gate bias V_G in the accumulation regime [48], the relation (5.34) simplified by neglecting $\frac{\delta \psi_s}{\delta V_G}$:

$$\frac{\delta Q_G}{\delta V_G} \cong \frac{\varepsilon_N}{x_N}\left[1 + \frac{q x_t}{2\varepsilon_N}\frac{\delta n_{ss}}{\delta V_G}\right]. \qquad (5.35)$$

For further development of the above relation let us consider the relation (5.26) giving $\frac{\delta n_{ss}}{\delta V_G}$. In this relation δf is sharply peaked function within a range of around the interface energy defined by the Fermi level which in turn, is fixed by the dc gate bias V_G. Provided that N_t is nearly constant in this range of energy (otherwise it may be replaced by its average value), it may be taken out of the integral in the case of spatial uniformity as assumed previously and the relation (5.26) becomes

$$\frac{\delta n_{ss}}{\delta V_G} = N_t \int_0^{x_t} \frac{dE_t}{dV_G} I_1 \, dx - j N_t \int_0^{x_t} \frac{dE_t}{dV_G} I_2 \, dx \qquad (5.36\text{-a})$$

with $$I_1 = \int_1^0 \frac{df}{1 + \omega^2 \tau_0^2 (1-f)^2 e^{4K_0 X}} = -\frac{\tan^{-1}\left[\omega \tau_0 e^{2K_0 X}\right]}{\omega \tau_0 e^{2K_0 X}} \qquad (5.36\text{-b})$$

$$I_2 = \int_1^0 \frac{\omega \tau_0 (1-f) e^{2K_0 X} \, df}{1 + \omega^2 \tau_0^2 (1-f)^2 e^{4K_0 X}} = -\frac{\ln\left[1 + \omega^2 \tau_0^2 e^{4K_0 X}\right]}{2\omega \tau_0 e^{2K_0 X}} \qquad (5.36\text{-c})$$

Replacing $\frac{dE_t}{dV_G}$ in the relation (5.36-a) by its expression (5.29) in accumulation expression ($\frac{\delta \psi_s}{\delta V_G} \approx 0$), $\frac{\delta n_{ss}}{\delta V_G}$ becomes :

$$\frac{\delta n_{ss}}{\delta V_G} = \frac{-N_t \int_0^{x_t} q \frac{x}{x_N} \left[I_1 - jI_2 \right] dx}{1 + N_t \int_0^{x_t} \frac{q^2 x}{2\varepsilon_N} \left\{ \frac{x}{x_t} + \frac{x_t}{x_N} - 2 \right\} \left[I_1 - jI_2 \right] dx} . \qquad (5.37)$$

It can be practically carried out that the second term of the denominator in the above expression is negligible and then it is reduced to the following form: this approximation is equivalent [61] to take $\frac{dE_t}{dV_G} \approx -\frac{qx}{x_N}$ by omitting the first term in the relation (5.29):

$$\frac{\delta n_{ss}}{\delta V_G} \approx -\frac{qN_t}{x_N} \int_0^{x_t} x\, I_1\, dx - j \frac{qN_t}{x_N} \int_0^{x_t} x\, I_2\, dx . \qquad (5.38)$$

Reporting the expression (5.35) and (5.38) into (5.32), the admittance Y_m of the MIS structure under accumulation bias becomes Fig 5.3-.c

$$Y_m = j\omega (C_N + C_t) + G_t , \qquad (5.39\text{-a})$$

with $C_N = \frac{\varepsilon_N}{x_N}$, (5.39-b)

$$C_t = \frac{q^2 N_t x_t}{2 x_N^{\,2}} \int_0^{x_t} \frac{x \tan^{-1}\left[\omega \tau_0 e^{2K_0 X} \right] dx}{\omega \tau_0 e^{2K_0 X}} , \qquad (5.39\text{-c})$$

$$\frac{G_t}{\omega} = \frac{q^2 N_t x_t}{2 x_N^{\,2}} \int_0^{x_t} \frac{x \ln\left[1 + \omega^2 \tau_0^{\,2} e^{4K_0 X} \right]}{2\omega \tau_0 e^{2K_0 X}} dx . \qquad (5.39\text{-d})$$

The relations (5.39-c) and (5.39-d) have been further simplified in the reference [61] and their analytical forms have been obtained by taking for $\frac{dE_t}{dV_G} \left(\approx -\frac{qx}{x_N} \right)$ between x=0 and x= x_t, the average value $-\frac{qx_t}{2x_N}$ and then the following expressions may be obtained

$$C_t = \frac{q^2 N_t}{8K_0} \left(\frac{x_t}{x_N} \right)^2 \gamma , \qquad (5.40\text{ -a})$$

$$\frac{G_t}{\omega} = \frac{q^2 N_t}{8K_0}\left(\frac{x_t}{x_N}\right)^2 \beta, \qquad \text{(5.40 -b)}$$

$$\gamma \equiv \left[\frac{\tan^{-1}(\omega\tau_0)}{\omega\tau_0} - \frac{\tan^{-1}(u)}{u} + \frac{1}{2}\ln\left(\frac{1+\omega^2\tau_0^2}{\omega^2\tau_0^2}\right) - \frac{1}{2}\ln\left[\frac{1+u^2}{u^2}\right]\right], \qquad \text{(5.40 -c)}$$

$$\beta \equiv \left[\tan^{-1}(u) - \frac{\ln(1+u^2)}{2u} - \tan^{-1}(\omega\tau_0) + \frac{\ln(1+\omega^2\tau_0^2)}{2\omega\tau_0}\right], \qquad \text{(5.40 -d)}$$

with $u = \omega\tau_0 e^{2K_0 X_t}$.

5-3-4 Depletion Bias Regime

Under the depletion bias regime, the direct tunneling of carriers from interface into the insulator traps seems rather difficult [52,63,64] due to the absence of accumulated carriers at the interface. Instead of direct tunneling, a two step mechanism are expected [52] shown in Fig.5.4-b. In the first step, true interface traps (i.e., traps located at the interface plane without extension into the insulator) exchange carriers with the majority band by the well known Shockley - Read - Hall (SRH) statistics. As mentioned in the reference [52], any exchange of carriers between the insulator and the semiconductor without communication with the electrodes could not contribute to the measured admittance. In this respect, the admittance detects the tunneling process which is interconnected with the SRH process. In other words, a carrier exchanged by a true interface trap by SRH process can move towards the traps distributed inside the insulator by tunneling, leaving behind the previous true interface trap empty, ready for a new cycle by SRH process. Here the tunneling process contributes to the admittance by increasing the exchange rate of SRH process alone. This extra charging/discharging leads to a parallel admittance Y_{ss} to the one Y_{it} associated with the SRH process alone Fig.5.4.d. The corresponding time constants τ_{ss} and τ_{it} of these two independent parallel process should be close to each other for simultaneous contribution; moreover in order to the loss phenomenon behind the admittance occurs, the inequality $\tau_{ss}(=\tau_0 e^{2K_0 X_t})>\tau_{it}$ should be satisfied [52]. The well known expression of the admittance $Y_{it} = G_{it} + j\omega C_{it}$ resulting from the SRH process alone [48] is given as follows:

$$C_{it} = \frac{qD_{it,s}}{\omega\tau_{it}} \tan^{-1}\left[\omega\tau_{it}\right] \; ; \; \frac{G_{it}}{\omega} = \frac{qD_{it,s}}{2\omega\tau_{it}} \ln\left[1+(\omega\tau_{it})^2\right] \qquad (5.41)$$

For revising the evaluation of tunneling connected admittance, Y_{ss} [54,65], let us return back to the expression (5.34). In this relation, $\frac{\delta n_{tb}}{\delta\psi_G}\left(= x_t \frac{\delta n_{ss}}{\delta V_G}\right)$ which is substantially reduced in depletion due to the very low surface density p_s of available majority carriers, may be neglected in presence of the term containing $\frac{\delta\psi_s}{\delta V_G}$, this latter being around its maximum values under depletion regime. Then, the relation (5.34) becomes:

$$\frac{\delta Q_G}{\delta V_G} \approx \frac{\varepsilon_N}{x_N}\left(1 - \frac{\delta\psi_s}{\delta V_G}\right) \qquad (5.42)$$

On the other side, in relation (5.33), neglecting δQ_t, the gate charge modulation (δQ_G) is counter balanced by ($-\delta Q_s$) where both interface charges (δQ_{ss}) and depletion regime edge (δQ_D) contribute to the semiconductor charge modulation. In this case the relation (5.32) becomes :

$$Y_m = Y_s \frac{d\psi_s}{dV_G} \text{ with } Y_s = -j\omega C_D + Y_{ss} \text{ and } Y_{ss} = -j\omega \frac{\delta Q_{ss}}{\delta\psi_s} = -j\omega q \frac{\delta n_{ss}}{\delta\psi_s}. \qquad (5.43)$$

From the above expressions $\frac{\delta\psi_s}{\delta V_G}$ ratio may be easily obtained:

$$\frac{\delta\psi_s}{\delta V_G} = \frac{j\omega C_N}{j\omega C_N + j\omega C_D + Y_{ss}}$$

The MIS admittance, Y_m is the series combination of insulator capacitance with the semiconductor admittance Y_s Fig.5.4-d

$$Y_m^{-1} = \frac{1}{j\omega C_N} + \frac{1}{j\omega C_D + Y_{ss}}. \qquad (5.44)$$

Using relation (5.25), (5.26), (5.40-c) and (5.40-d) and considering that $\delta E_t = -q\delta\psi_s$, the expression of $\frac{\delta n_{ss}}{\delta\psi_s}$ may be obtained :

$$\frac{\delta n_{ss}}{\delta\psi_s} = -qN_t\int_0^{x_t} I_1 dx + jqN_t\int_0^{x_t} I_2 dx = \frac{qN_t}{2K_0}\gamma - j\frac{qN_t}{2K_0}\beta . \qquad (5.45)$$

Replacing (5.45) into (5.43), Y_{ss} becomes :

$$Y_{ss} = j\omega C_{ss} + G_{ss} \quad \text{with } C_{ss} = \frac{q^2 N_t}{2K_0}\gamma \text{ and } \frac{G_{ss}}{\omega} = \frac{q^2 N_t}{2K_0}\beta . \qquad (5.46)$$

5.4-Sample preparation and measuring equipment

Both a-SiCx:H and a-SiNx:H thin film studied in this work were deposited by the standard radio frequency (13.56 MHz) plasma enhanced chemical vapor deposition (PECVD) technique on two different substrates: Czochralski (CZ) grown, 100 oriented p-type silicon wafers of resistivity 12-18 Ωcm for both MIS structure and IR analysis, and transparent quartz substrate for UV-Visible transmission measurements. Prior to loading into deposition chamber, substrates were cleaned by RCA process (discussed in section 3.6.1). After the substrates were loaded, PECVD chamber was pumped down below 10^{-4} Torr, and then in situ cleaning process with 100 ccm hydrogen flow for 5 minutes was applied at 0.1 Torr. Subsequently, the deposition of a-SiCx:H and a-SiNx:H films were achieved with the parameters given in table2.5.1. The chamber pressure was kept at 0.5 (0.3) Torr for a-SiCx:H (a-SiNx:H) film; RF power density of 100 $mWcm^{-2}$ and 60 $mWcm^{-2}$ were used for cleaning and deposition process, respectively. The deposition rate was measured to be around 11 nm/min. For top electrode, aluminum metal (Al) was evaporated through a shadow mask on various substrate to obtain MIM (or MSM) and MIS structure (see fig.5.5 below). The same Al electrode was evaporated on bare silicon wafer for p-Si Schottky diode, used for the determination of dopant density in silicon substrate

5.4.1 Metalization

Metal electrodes on the deposited films are needed for the electric measurements as front and back contact. Hence, the deposited films must be

coated with metal (typically, aluminum (Al)) electrodes. Aluminum coating set up is schematically given in the figure 5.5 and principle of operation is given elsewhere [46].

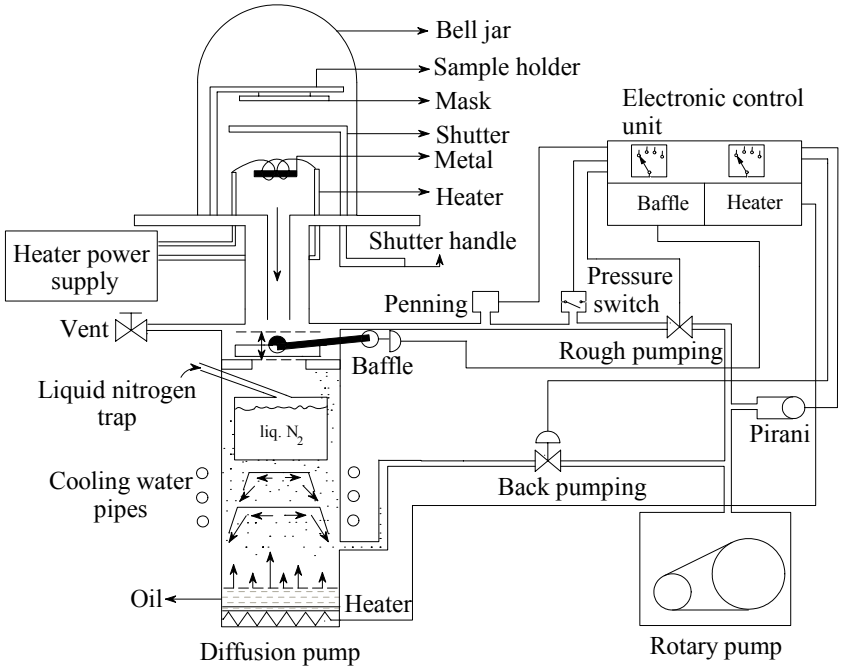


Fig. 5.5 Metal coating set up

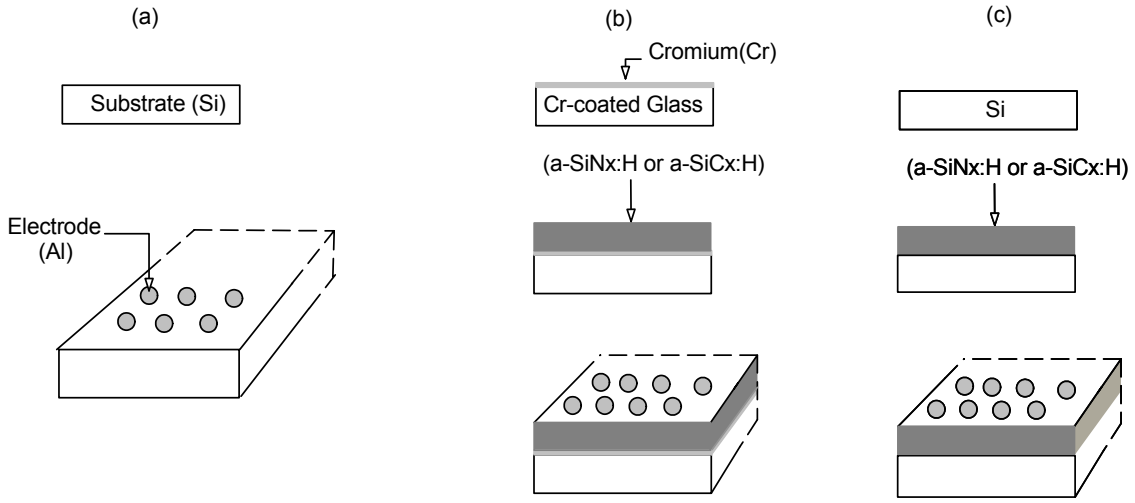


Fig.5.6 Formation of : Shottky diode (a), Metal-Insulator-Metal (MIM) (b) and Metal-Insulator-Semiconductor (MIS) structures (c), respectively.

In the light of discussion above, a-SiCx:H and a-SiNx:H films were grown on Si substrates; the deposition conditions reported in the table 5.1.

Table 5.1. Growth conditions for both a-SiCx:H and a-SiNx:H films.

	Press. (Torr)	Subs temp. (C)	SiH_4 flow (ccm)	C_2H_4 (NH_3) (ccm)	RF Power mW cm^{-2}	Deposition Rate (nm/min.)	Thick. (Å)
A (aSiCx:H)	0.5	250	30	30	60	11	1000-1200
B (a-SiCx:H)	0.5	300	6	54	60	11	4500
C (a-SiNx:H)	0.3	300	3	36	45	-	3000
D (a-SiNx:H)	0.3	300	3	36	45	-	5000

5-5 Results and Discussion

Examples of both the capacitance (C_m) and the ac conductance ($\frac{G_m}{\omega}$) as a function of gate bias V_G for various frequencies are given in the figure 5.7. The most remarkable behavior to be noticed on these curves is the frequency dependence along all the bias regimes (extended from the accumulation to the inversion) for frequencies that might be qualified as “high frequencies” apart from the expected exclusive frequency dependence of the conventional MIS structure in the inversion regime[48]. First, the shift of C_m vs. V_G curves along the voltage axis as a function of frequencies is reported in the figure 5.7-b as flatband voltage V_{FB} vs. logf. The perfect linearity (V_{FB} = -11.5-0.12logf) is consistent with the tunneling model where the time constant is exponentially penetration dependent as discussed in the Section 5.3.2.

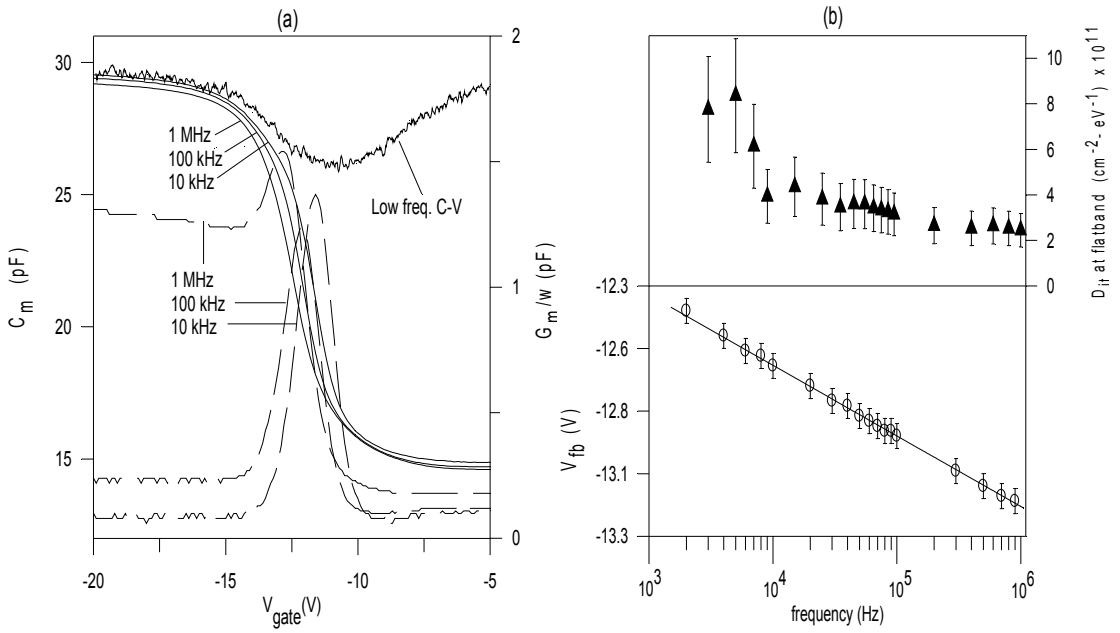


Fig.5.7 (a) Measured capacitance (solid line) and conductance (dashed line) vs. gate voltage at different frequencies of Cr/a-SiNx:H/p-Si MIS structure. (b) Flat band voltage shift (circle) (the line represent logarithmic fit) and interface trap density calculated at flat band (triangle) versus frequency.

In other words, at a given frequency, all traps possessing time constants smaller than the inverse of frequency follow the ac gate voltage modulation δV_G to maintain their charge state under the requirement of the equilibrium. This defines a corresponding flat band voltage. If the frequency is increased, part of previous traps with slower time constants could not follow the ac perturbation and then they will stay charged contributing in their turn to the increase of V_{FB}. However, the frequency modulation of the V_{FB} should remain limited since only those traps whose energy levels lie around the Fermi level and then whose charge state is able to be modified by the gate voltage modulation are involved. The main part of V_{FB} is due to charged traps remaining out of the voltage modulation scope. The relatively large value of V_{FB} (> -13 V) is a consequence of several hours aging under a voltage stress of -20 V: free holes accumulated at the semiconductor/insulator interface are possibly infected by tunneling into the traps in the insulator [66-68]. (These charges might be redistributed within the insulator, probably by hopping mechanism [69]). On the same figure 5.7-b, the effective interface state density D_{it} calculated around flatband capacitance C_{FB} by the relation (5.8) [44]:

Taking into account the extreme roughness of this D_{it} calculation at a single point, its overall variation as a function of frequency may be considered consistent with that of V_{FB}. This is in agreement with the fact that V_{FB} is the gate voltage applied to counterbalance the effect of the insulator fixed charges (Q_f) and the effective interface charges Q_{it} $\left(= q\int_0^{\psi_s} D_{it} d\psi_s\right)$ on the semiconductor potential distribution [48]:

$$V_{FB} \approx -\frac{\left(Q_f + Q_{it}\right)}{C_N}. \qquad (5.47)$$

Both V_{FB} and D_{it} variation as a function of frequency should be resulted from the second term of the above relation (5.47). This may be accepted as a “one more” confirmation of tunneling model.

The frequency dispersion of measured accumulation capacitance (C_{ms}) and measured series resistance (R_{ms}) along with the best fits (solid lines) using tunneling model outlined in section 5.3.2 is given in figure 5.8.a C_{ms} and R_{ms} are related to the fitting parameters (N_t, x_t) through (see figure 5.8)

$$C_{ms} = \left(C_N + C_t\right) + \frac{G_t{}^2}{\omega^2\left(C_N + C_t\right)}, \qquad (5.48\text{-a})$$

$$R_{ms} = R_s + \frac{G_t}{G_t{}^2 + \omega^2\left(C_N + C_t\right)^2} \qquad (5.48\text{-b})$$

In the fitting procedure, the minimization routine of Matlab [70] based on the algorithm of Nelder-Meade simplex search method has been used. In the calculations, K_0= 0.64 x 10^8 cm^{-1} [14] for Si_3N_4 and τ_0 = 10^{-11} sec (estimated from relaxation time constant for Si in accumulation [48]) was used.

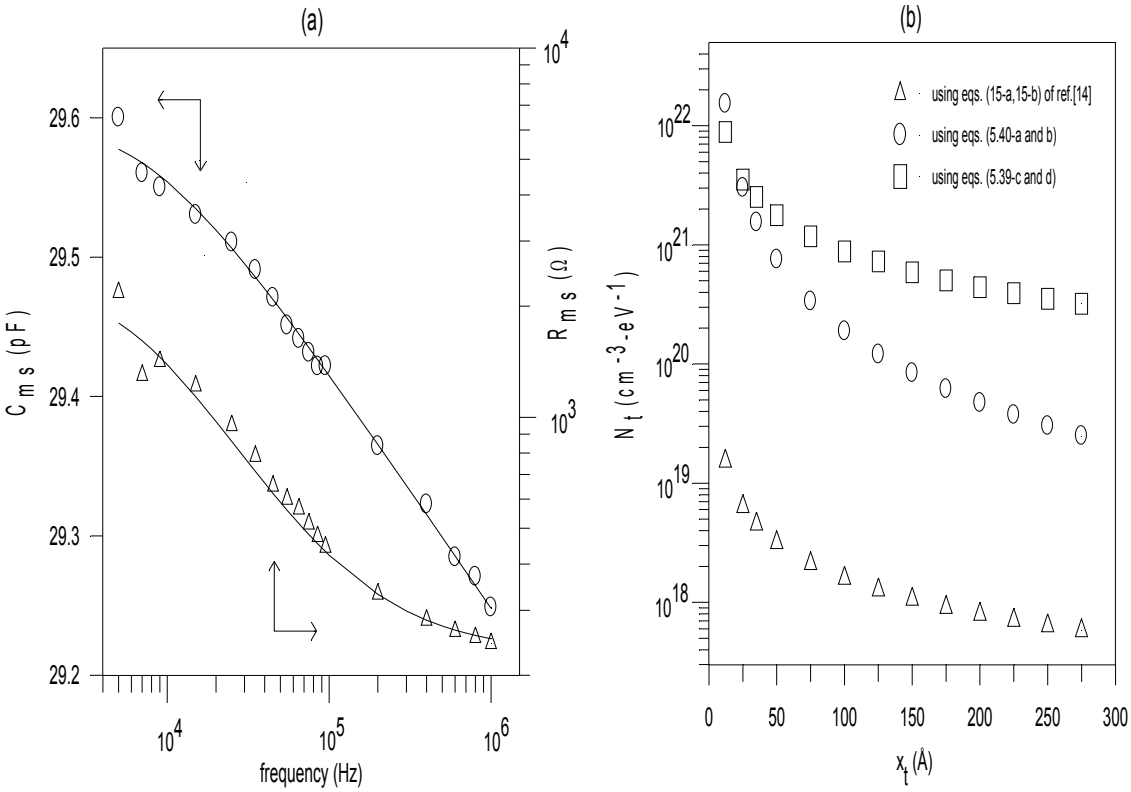


Fig.5.8 (a) Measured accumulation capacitance (circle) and equivalent series resistance (triangle) vs. frequency with the best fit (solid lines) obtained from tunneling model. Percentage erros in measured C_{ms} and R_{ms} are 0.5 % and 1 %, respectively.(b) (N_t, x_t) solution set giving same best fit to C_{ms} and R_{ms} with various equations.

The solution is not unique and the solution set (N_T, x_t) giving the best fit to the same experimental results of figure 5.8-a is reported in the figure 5.8-b by using the integral equations (5.39-c, 5.39-d), and analytical expressions (5.40-a, 5.40-b) for C_t and G_t. Apart from the unacceptably high value of N_t for lowest tunneling distance x_t, a decreasing N_t seems to be compensated by an increasing x_t in order to lead to the same admittance effect. Also, note that the result due to integral and analytical expressions diverges with increasing x_t. Furthermore, we should draw attention that when the factor $x_t/2x_N$ is omitted as in the work of some authors [61,63,71], N_t for a given x_t is about two orders of magnitude smaller. To clarify this point, figure 5.8 from reference [61] has been retrieved and the best fit to the measured C_{ms} and R_{ms} has been obtained with N_t : 1.46 x 10^{20}, 1.8 x 10^{20}, 3.09 x 10^{18}, 2.51 x 10^{18} $cm^{-3}eV^{-1}$ by using eq. (5.39-c, 5.39-d), eq .(5.40-a, 5.40-b), eq .(15-a, 15-b) of ref.[61] and eq (5,6) of ref.[63] respectively for given x_t = 12 Å and τ_0= 10^{-9} sec.

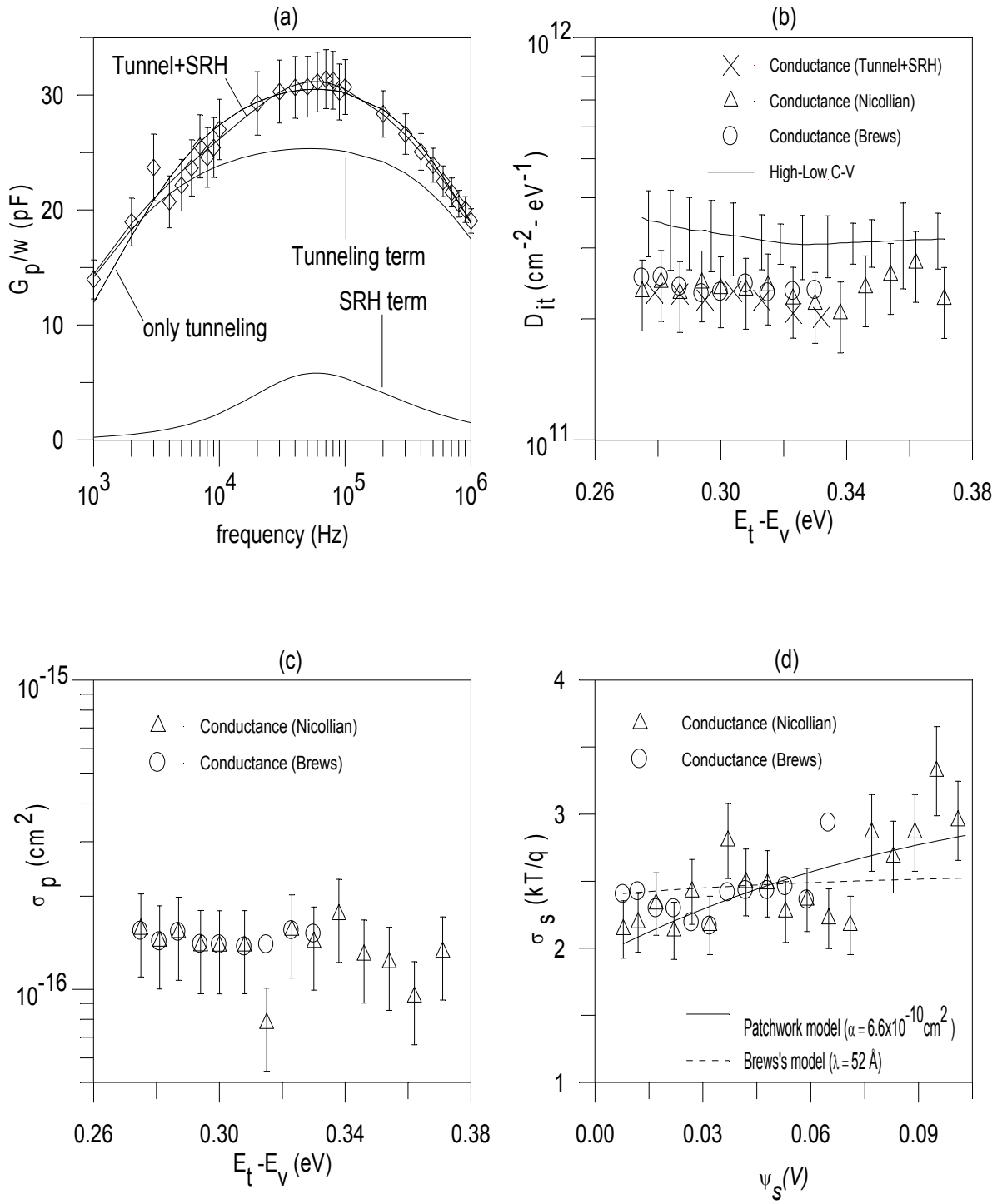


Fig. 5.9 a) Experimental G/w versus frequency in depletion at V_G=-12.8 V with the best fits obtained from tunneling model by neglecting (dotted line) and including (solid lines) SRH term. b) Energy distribution of interface trap density and c) capture cross section obtained by different models/techniques. d) standard deviation versus surface band bending from statistical approach of conductance technique in comparison with Brews's and patchwork models.

Figure 5.7 shows a measured a.c conductance vs. frequency ($\frac{G_p}{\omega}$ vs f) (after series resistance corrected and insulator capacitance compensated) in depletion at V_G= -12.8 V. A best fit (dotted curve) is performed using the relation (5.46) of the tunneling model alone with the fitting parameters N_t, x_t, and τ_{ss}. N_t = 4.37 x10^{18} cm^{-3}-eV^{-1}, x_t = 5.2 Å and τ_{ss} = 2.27 x 10^{-4} seconds have been obtained. The quality of fitting seems not excellent; since around the maximum and towards the low frequency side, the experimental point remain slightly above the tunneling curve. The combination of the SRH term (relation 5.41) with the tunneling one gives a more accurate result (solid lines), i.e.,

$$\frac{G_p}{\omega} = \frac{G_{it}}{\omega} + \frac{G_{ss}}{\omega}. \qquad (5.49)$$

Table 5.2 Fitting parameters of experimental (Gp/w - *f)* with the tunneling model with SRH recombination.

SRH Term				Tunneling term		
V_G(V)	E_t-E_v(eV)	$D_{it,s}$ 10^{10} (cm^{-2} eV^{-1})	τ_{it} 10^{-6} (sec.)	N_t 10^{18} (cm^{-3} eV^{-1})	X_t(Å)	τ_{ss} 10^{-4} (sec.)
-13.16	0.279	3.03	1.65	3.63	5.56	1.14
-13.0	0.286	2.78	2.88	3.57	5.69	1.71
-12.9	0.294	2.16	4.68	3.73	5.40	1.69
-12.8	0.303	2.35	5.40	3.52	5.99	4.44
-12.7	0.312	1.16	1.18	3.93	5.37	3.26
-12.6	0.322	3.44	1.20	4.09	4.28	1.20
-12.5	0.324	4.24	1.22	3.86	4.13	1.22

The fitting parameters at some gate voltages in depletion is given in table 5.2, by which the energy distribution of the interface trap density $D_{it} \approx D_{it} + N_t x_t$ has been given in figure 5.8.b in comparison with the statistical model and High-Low frequency C-V method. In the statistical model, the equivalent parallel conductance is given by[48];

$$\frac{G_{it}}{\omega} = \int_{-\infty}^{\infty} \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] P(v_s) dv_s, \qquad (5.50)$$

where $P(v_s)dv_s$ is a Gaussian probability function, and interface trap parameters are extracted either by using the ratio of the measured G_p/ω at 5xf_{peak} to that at f_{peak}

(Nicollians's approach) or by using the width of the measured G_p/ω at some fraction with respect to the peak position (Brews's approach) [49].

Although D_{it} from High-Low C-V method is a little bit higher, due perhaps to a systematical error resulting from the difference between high and low frequency capacitance (since high frequency capacitance might be slightly over corrected from the series resistance effect), the results seem to be consistent among each other. From the energy distribution of the capture cross section (σ_p) obtained from the statistical model, (figure 5.9.c), an average value of 10^{-16} cm^2 is thought to be acceptable and consistent with a neutral trap.

The experimentally determined standard deviation σ_s of the statistical model as a function of surface band bending ψ_S is given in the figure 5.9.d One of the following mathematical models which describe the dependence of σ_s on several device parameters was developed by Brews [72]:

$$\sigma_s^2 = \left[\frac{q}{kT(\varepsilon_{si}+\varepsilon_N)}\right]^2 \frac{q(Q_f+Q_{it})}{4\pi} \ln\left[1+\left(\frac{\varepsilon_{si}+\varepsilon_N}{C_N+C_D+q^2D_{it}}\right)^2 \lambda^{-2}\right], \quad (5.51)$$

where λ is the minimum wavelength of interface charge inhomogenities. This Brew's expression is fitted to the experimental values; the best fit gives λ as 52 Å which is the within the limit of the suggested interval [72].

Another analytical expression for σ_s was developed by Nicollian-Goetzberger [48,72]. This so called patchwork or quasi-uniform model provides an expression of σ_s as follows:

$$\sigma_s = \frac{q}{kT}\sigma_Q\left(C_N+C_D+q^2D_{it}\right)^{-1}, \quad (5.52)$$

where the overall MIS structure is approximated by an array of elementary capacitors with equal characteristic area α, and each capacitor possesses a uniform surface potential and a uniform effective interface charge density $Q_N = Q_f + Q_{it}$. Here Q_N presents a Gaussian distribution around the average value $\overline{Q}_N$ with the standard deviation $\sigma_Q = \left(\frac{q\overline{Q}_N}{\alpha}\right)^{\frac{1}{2}}$. This expression of σ_s is equally fitted to the experimental

values and the result (obtained for α= 6.6 x 10^{-10} cm^2) is reported on the same figure 5.9.d as comparison. Although both approaches correctly reflect the slight ψ_s dependence of σ_s , the patchwork model seems much more acceptable to cover the rather dispersed experimental values.

CHAPTER 6

HOPPING TRANSPORT ASSESSED BY ADMITTANCE

6.1 Introduction

Though (as mentioned before) amorphous silicon based thin film transistor technology has increasing number of appli cations in the market, this structure exhibits a serious instability problem when used in dc mode at prolonged gate voltage bias stress, interpreted by two basic mechanisms: progress of trapped charges across the gate insulator due to the charge injection [69,73-76] or alternatively a slow process of metastable state creation in the semiconductor side, consisting of weak Si-Si bond breaking [76-83] (discussed in chapter 2). For a-Si:H TFTs, the two mechanism, more or less, might contribute to the instability phenomena [11] and manifest themselves as a shift of both on/off voltage (i.e., threshold voltage) of TFTs and the flatband voltage of the MIS capacitors under stress.

The creation of metastable defects or states can be provoked by a variety of means including illumination [84], current [85,86], electric field [87], doping [88] and rapid thermal quenching [89]. However, throughout this work, defects created by constant bias stress (electric field) was studied. In other words, a bias is applied to the top contact of MIS capacitor at low temperatures (< 100 °C) for long periods of time (> 10^4 sec.). It is a unipolar stress as only electrons (positive bias stress) or holes (negative bias stress) are present. In H-diffusion model (outlined in Appendix C), the difference between reference voltage and applied gate bias can be related to the band tail carrier density through: $N_T=C_{ins}\ \Delta V$. Assuming no charge injection, the increasing number of dangling bonds is related to the shift in reference voltage (will be discussed in detail in section 6.2):

$$\Delta N_T(t) = N_T(t) - N_T(0) = C_{ins}\left(V(t) - V(0)\right) \qquad (6.1)$$

Inserting this relation into (C.4) yields the streched exponential relation;

$$\Delta V_{ref} = \Delta V(0)\exp\left[-(t/\tau)^{\beta}\right] \qquad (6.2)$$

with ΔV_{ref} is the experimentally observed reference voltage shift under the gate bias stress and $\Delta V(0)$ is the reference voltage value just at the turn on time of bias stress. The effect of negative bias stress on PECVD grown a-SiCx:H/c-Si structure was given as a function of time and temperature. There is a perfect agreement of this time evolution with the H-diffusion model (illustrated in Appendix C in fig.C.2).

Although H-diffusion model (proposed by Jackson and coworkers) [82,83] seems satisfactory, more recent investigations [89-92] have pointed out that the metastable defect creation mechanism can hardly accounts the observed time evolution or instabilities on a-SiNx:H/a-Si:H TFTs. In addition, Hickmott [93] has observed similar phenomenon in doped poly-crystalline silicon/thermal SiO_2/c-Si structures where hydrogen can not be present due to high temperature process (above 1000 ˚C). Therefore, a charge carrier injection model should be considered seriously; for this respect in order to avoid the ambiguity between two amorphous material (a-Si:H/a-SiNx:H or a-Si:H/a-SiCx:H), a single film a-SiNx:H or a-SiCx:H alone may be deposited on crystalline silicon to find out the role of carrier injection and related mechanism(s) behind the instability of MIS capacitor.From now on, a-SiCx:H and a-SiNx:H films will be designated by a-SiN(C)x:H and an eventual discussion is valid for both of them. Specifically a derivation/discussion on dc hopping mechanism will be carried out within nitrogen and carbon rich a-SiN(C)x:H films through MIS structure in section 6.2. Moreover, this proposed model for a-SiN (C)x:H based MIS structure will be extended to ac hopping for a slightly carbon rich a-SiCx:H thin film in section 6.4.

6.2 Charge Injection : dc hopping

6.2.1 The frame of the ac capacitance Measurements

The frequency dependence of the a-SiNx:H film based MIS structure was already investigated in Chapter 5 [62]. An hypothetical charge injection and eventual frequency dependence of the MIS (a-SiNx:H and a-SiCx:H as insulator) structure at

hand for both accumulation and inversion gate voltage regime are schematically illustrated together with the corresponding equivalent ac circuits in the fig.6.1. The bias and thermal stress induced shifts of the C-V as a function of time were carried out and given in the fig.6.3. The C-V curves illustrated in fig 6.2 clearly point out that in the horizontal shift of the C-V characteristic, 'd.c' and 'a.c' contributions coexist.In other words, a charge modulation δQ_G on the gate, produces equal amount of opposite charges $\delta Q_S = \delta Q_T + \delta Q_A$ ($+\delta Q_{ss}$) located at the distance $d_I - x_t$ (within a-SiN(C)x:H film, here x_t is assumed as the average distance from the Si interface along which the injected charges might be extended), d_I (a-SiN(C)x:H/p-Si interface), and $d_I + d_D$ (edge of the depletion region within p-Si substrate for a-SiCx:H films only), respectively. The modulation of Q_T (and Q_{ss} for a-SiCx:H film) is thought a slow phenomenon.

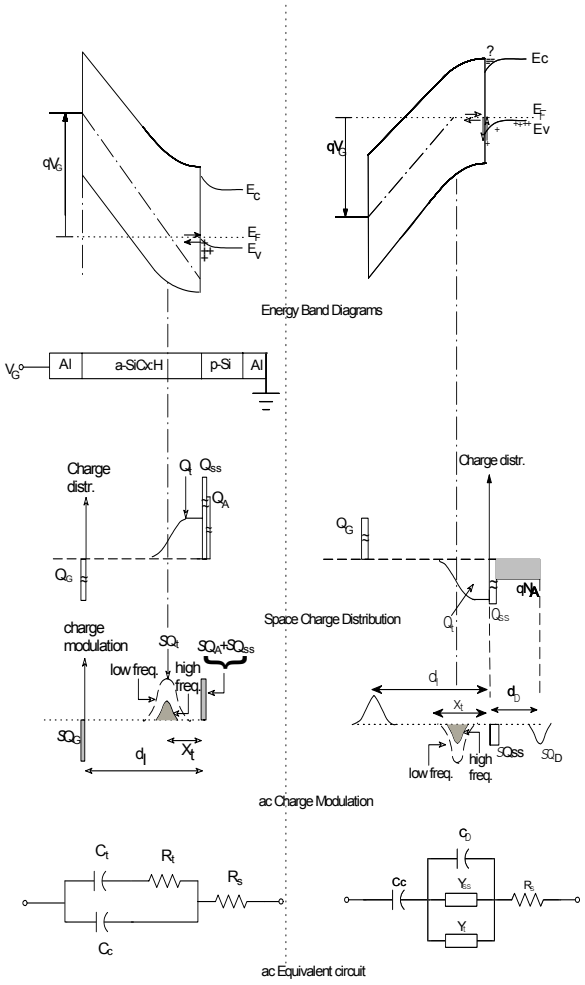


Fig.6.1 Schematic charge injection and resulting ac modulation

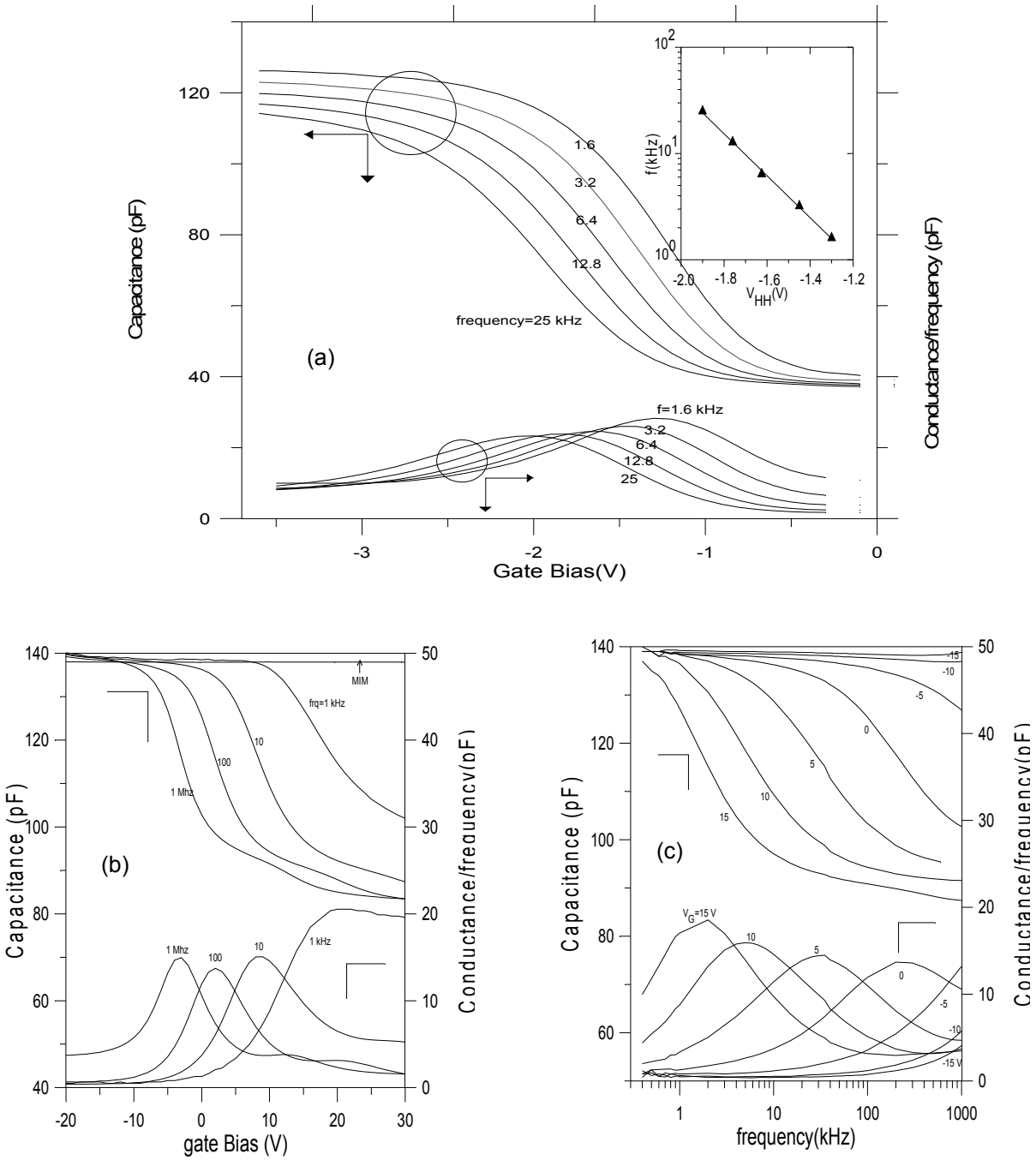


Fig.6.2 Typical example of C-V and G-V curves exhibiting the substantial frequency dependence of the Cr/a-SiNx:H/cryst. p-Si MIS structure. The inset shows the frequency dependence f(kHz) of half height V_{HH}(V) in MIS structure. Also, admittance vs. gate voltage curves of the carbon rich a-SiCx:H based MIS structure as a function of a.c gate voltage modulation frequency were given in (b,c). In addition, insulator capacitance is confirmed via C-V measurement on MIM (Cr/a-SiCx:H/Cr) structure, given in (b).

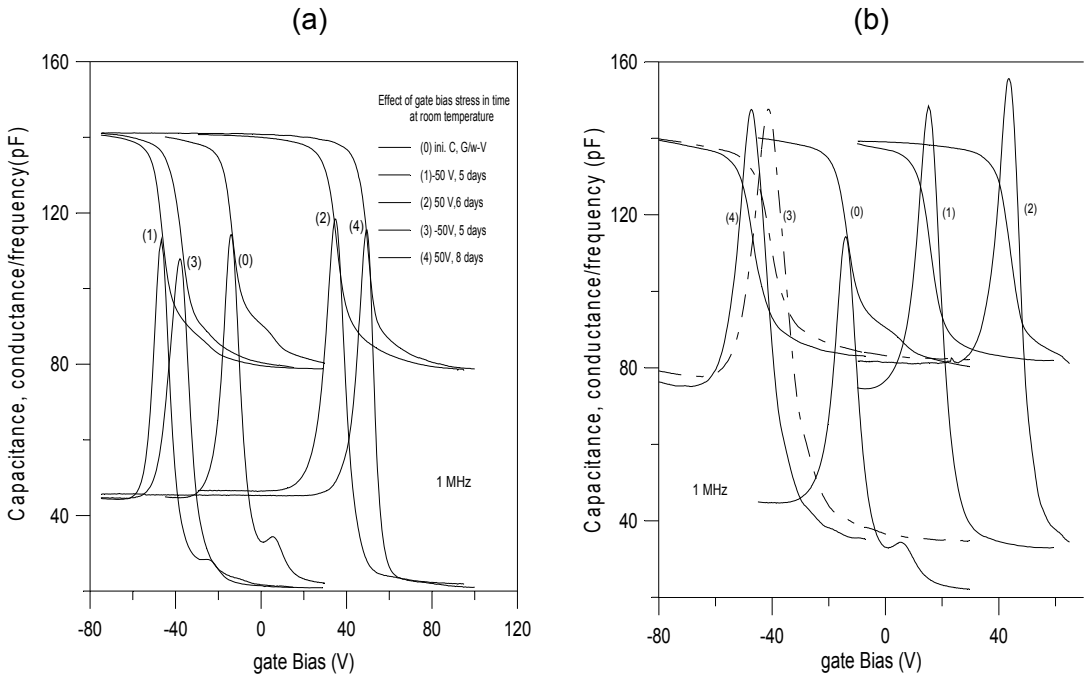


Fig.6.3 (a) Admittance vs gate voltage measurements under accumulating/inverting gate bias stress (-/+ 50 V) on Al/a-SiCx:H/p- Si MIS structure subjected to differing charge injection situation : (0) virgin, (1) holes, (2) electrons, (3) holes, (4) electrons, respectively. Note that the C,G vs V curves initially shift to the left, implying the trapping of holes, whereas for positive gate bias stress, the curves move to the right. Finally, the curves are returned roughly to its original state for -/+ 50 V bias stress again with no change in slope, indicating that no interface states in the lower part of the band gap are created. (b) enhanced effects of the temperature on the admittance vs gate voltage curves at -/+ 50 V bias stress for about 3 hours. Notice that 0,1 and 2 stands for +50V gate bias stress at temperatures 300,350 and 375 K, respectively whereas 3 and 4 represent -50 V gate bias stress for the temperatures 350 and 375 K.

Furthermore, as Q_t has a spatial dependence, both the amount of modulation and its space location are frequency dependent (see fig.6.1). In accumulation (and inversion), all components of $\delta Q_s \left[= \delta Q_t + \delta Q_A \left(+ \delta Q_{ss}\right)\right]$ are located near interface, except δQ_t which is lying more or less within the film at the average distance x_t, leading to more or less frequency dependence of accumulation (or inversion) capacitance respectively [62]. If $\frac{x_t}{d_I}$ <<1, this frequency dependence may remains

below the detectability limit as it is the case in a-SiCx:H film. However, it seems cautious to use the highest frequency available for evaluating the film thickness through capacitance measurement at accumulation.

For investigation of the injected charges into the dielectric film, the apparent C-V shift due to the a.c effect, should be avoided in the case of dc hopping case by selecting a measurement frequency high enough, avoiding the response from the position x_t, and leading to a conventional MIS capacitor behaviour. Consequently, the capacitances (C-V) of the sample was measured by a capacitance meter of 1 MHz measurement frequency at 350 mV/sec as gate voltage sweep rate. Typical C-V curves are given in fig. 6.4-a,b. They point out the extreme sensitivity of the structure both to an half an hour positive and negative bias stress application for various temperatures (uncertainty ≈ 2 K) and for either gate voltage sweep direction at 20 V and at –30 V corresponding respectively to free electron and free hole accumulation at the interface of the silicon substrate. A priori, the observed shift of the the C-V curve might be due to the injection of charge carriers from both gate electrode and the silicon sides. However, it is known that a given voltage shift ΔV of the C-V curve may be expressed as the first moment of the bulk trapped charges, i.e., the product of injected total charge amount Q_T through unit area by the moment arm (or centroid of trapped charges) $x_M(=d_I-x_t)$: $\Delta V = \frac{Q_T x_M}{\varepsilon_N}$ with $x_M = \frac{\int_0^{d_I} x\rho(x)dx}{Q_T}$, where $Q_T = \int_0^{d_I} \rho(x)dx$, d_I the insulator thickness and x_M are measured from the gate interface. In this respect, the gate side injection would lead to relatively negligible C-V shift since x_M remains smaller than d_I ($x_M << d_I$) within the previously mentioned time interval. Consequently, throughout this work an injection from the silicon substrate has been assumed. The evolution of charge trapping both in temperature and in time may be either interface limited (Fowler-Nordheim tunneling by the gradual change of interface electric field through an eventual build up of trapped space charge) or bulk limited due to the 'hard' mobility of trapped charges throughout the insulator.

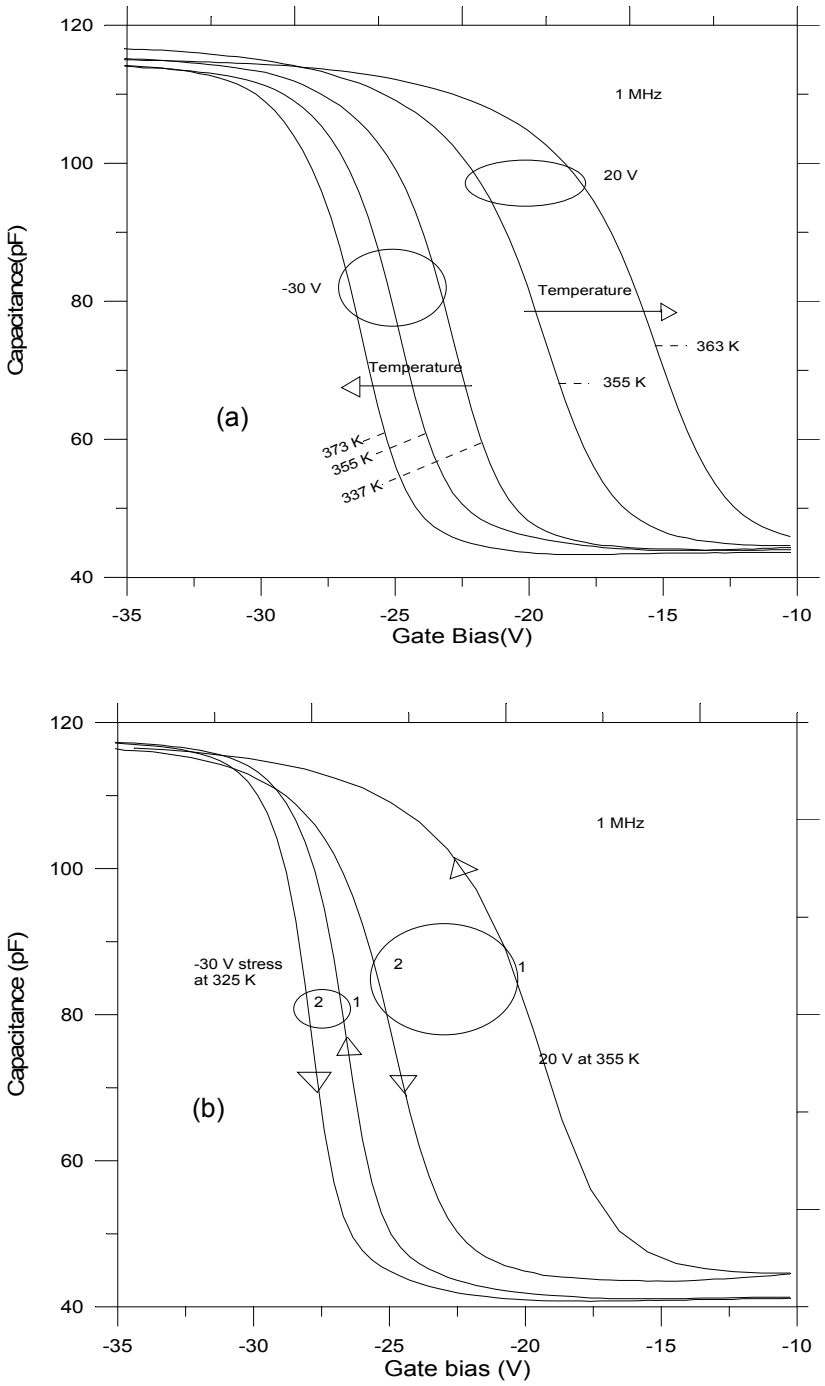


Fig 6.4. (a) Effects of the temperature on the C-V curves for both negative and positive stress gate voltages, (b) Effect of gate voltage sweep direction on the C-V curve: 1 and 2 represent (+) to (-) and reverse directions, respectively.

6.2.2 Kinetics of charge injection under thermal and bias stresses

For investigating charge behaviors under bias and temperature stresses, the following procedure was applied as given in the following flowchart diagram. First, initial C-V curve was taken and fitted to cubic spline, half height voltage value between accumulation and inversion capacitances was determined, denoted by V_{HH} in the text, due to practical reason instead of commonly used flatband voltage, V_{FB}. The corresponding capacitance value C_{HH} is used for determination of the whole C-V curve along the voltage axis, indicating the amount of fixed charges in the a-SiN(C)x:H. Then, sample is kept biased in accumulation for a given period at a temperature T. At time $t=t_i$, interrupting the stress, a capacitance was measured by applying previously determined V_{HH} and then the resulted C-V curve is fitted to cubic spline regression approach and the corresponding new $V_{HH}(t_i)$ is obtained within a predetermined uncertainty in less than 0.25 sec. and the process is continued till it is stopped by the experimenter.

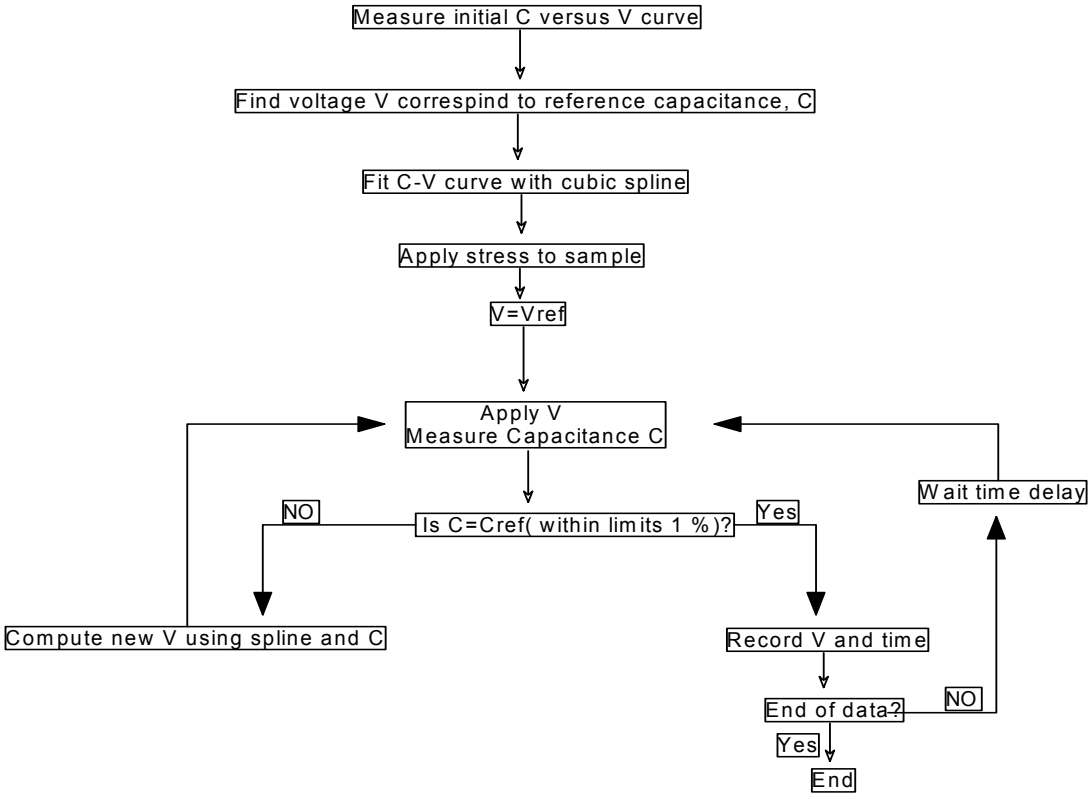


Fig. 6.5 Flowchart depicting the sequence of measurements for the rapid determination of C-V curve position along the voltage bias axis at a given date.

For achieving these tedious and time consuming experimental sequences, a LABVIEW program was developed to determine C-V voltage shifts vs. gate voltage stressing time $\left[\Delta V_{HH}\left(t_i\right)\right]$. After completing this task, final C-V is measured from accumulating to inverting gate voltages for carrying out the stress effects shown in fig.6.3 for each stress cycle. The mentioned time evolution cycle was similarly repeated for inverting gate bias stress, immediately after taking initial C-V curve by sweeping the voltage from accumulating to inverting side. The whole cycle was resumed for different temperatures

In addition to the above described capacitance kinetics, the d.c current versus time measurements (I(t)) were carried out on the same sample in order to guess the microscopic charge transport mechanism(s) or limitation(s). The measured I(t) curves under both accumulation (negative gate voltages) and inversion all exhibit a discernible time decay after the first few seconds and they tend to saturate for t beyond 10 hours (fig.6.6). The corrected current decays seem proportional to $t^{-(\alpha-1)}$ with $0<\alpha<1$. This dispersive transport is in agreement with the continous time random walk (CTRW) theory [94] suggesting hopping between localized states or multiple release from traps [95].

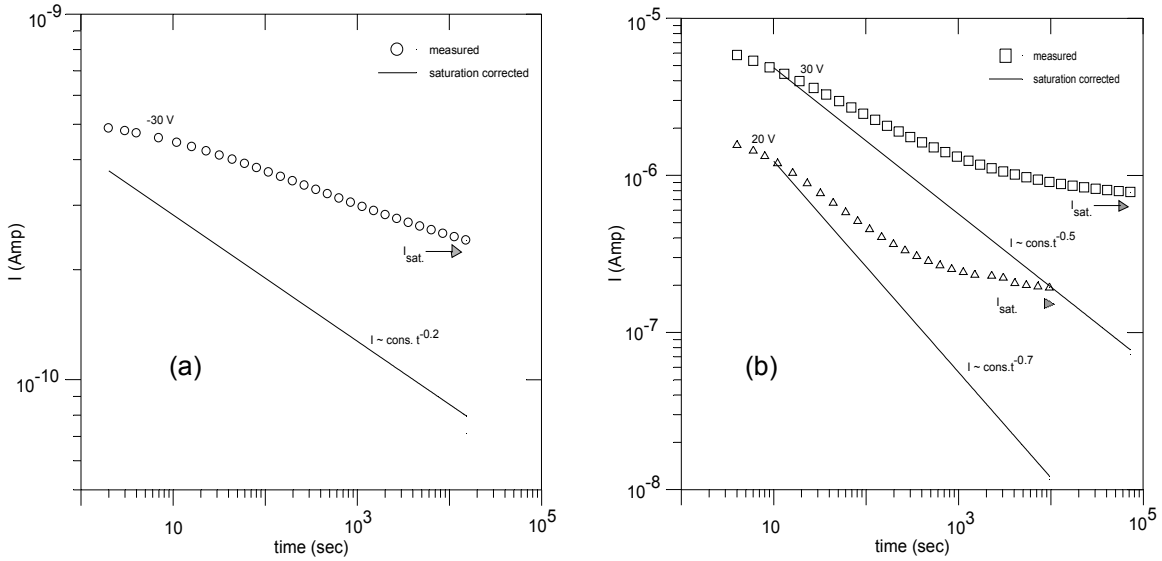


Fig. 6.6 Current time decays of the Cr/a-SiNx:H/p-cryst. Si MIS structure under various constant gate voltages at room temperature: (a) accumulation, (b) inversion. Note that experimental uncertainties are assessed by the size of relevant symbol.

6.2.3 Carrier percolation through the (semi) insulating a-SiCx:H film

In accumulation and inversion gate bias regime, the relevant carriers (holes in accumulation and electrons in inversion) may be injected into the film by direct tunneling; beyond a certain trap concentration it should become more favorable for carriers to hop farther by hopping (or multiple tunneling) rate *P* under local average electric field F which enhances the hopping towards the gate electrode direction (discussed in appendix D):

$P_{+,-} = \upsilon_{ph} \exp\left[-\frac{2R}{\lambda} - \frac{(W \pm qRF)}{kT}\right]$ leads to

$$P_{net} = P_{+} - P_{-} = \upsilon_{ph} \exp\left[-\frac{2R}{\lambda} - \frac{W}{kT}\right] \sinh\frac{qRF}{kT} \qquad (6.3)$$

where q= elementary charge, υ_{ph}= attempt to escape (phonon) frequency, $\exp\left(-\frac{W}{kT}\right)$= thermal activation factor with W= energy difference of the two involved traps, $\exp\left(-\frac{2R}{\lambda}\right)$= transfer integral of the relevant sites with R being the most optimal hopping distance and λ being the characteristic localization length of the wave function envelope around the trap site as $\exp\left(-\frac{x}{\lambda}\right)$. For $F < \frac{kT}{qR}$, $\sinh\left(\frac{qRF}{kT}\right) \approx \frac{qRF}{kT}$ and then P_{net} becomes proportional to the local electric field F:

$$p_{net} \approx \upsilon_{ph}\left(\frac{qRF}{kT}\right)\exp\left[-\frac{2R}{\lambda} - \frac{W}{kT}\right] \qquad (6.4)$$

On the other hand, at relatively low temperature, carriers will tend to hop to longer distances to find sites which would lie energetically closer than the nearest neighbors; this version of hopping mechanism is the so called variable range hopping [96]:

$$p_{net} \approx \upsilon_{ph}\left(\frac{qRF}{kT}\right)\exp\left[-\frac{A}{T^{1/4}}\right] \qquad (6.5)$$

where $A = 2\left[\frac{1}{\left(\lambda^3 kN(E)\right)}\right]^{1/4}$ with N(E)= trap density per unit vol. per unit energy interval.

For a disordered material, (on the contrary of the ordered structures where a constant transition rate p_0 exists between neighbors, corresponding to a hopping time distribution $\Gamma_0(t) = p_0 e^{-p_0 t}$ with $\int_0^\infty t\Gamma_0(t)dt = p_0^{-1} \equiv$ average hopping time constant), a continuous distribution of transition rate *p* results due to the variation of both the distances between the hopping sites and their energy depth [96]. The hopping time distribution [94] $\Gamma(t) = (const.)t^{-(1+\alpha)}$, with 0< α <1, leads to:

$$p^{-1} = \int_0^t t'\Gamma(t')dt' \approx t^{1-\alpha} \qquad (6.6)$$

Although the charge transport is a complex process in a-SiN(C)x films, under high field at steady state, field-induced detrapping (or Poole-Frenkel emission) process is generally admitted as dominant mechnasim [97]. But under lower field, charge trapping or injection leads to a current decaying with time [98]. In other words, the injected carriers from the crystal silicon are trapped in the a-SiN(C)x film and a space charge is built up affecting the value of the electric field F_s at the interface. This space charge which is continuosly supplied from the interface, is progressively extended into the dielectric film and then the current, I_E, measured in the external circuit [99]: $I_E = I_C + I_D$ with I_C=contact current and I_D= displacement current. The last one is expressed by the time variation of the interface electric fields F_s:

$I_D = \varepsilon \frac{\partial F_s}{\partial t}$ with ε dielectric constant. On the other side the interface electric field $F_s = -\left[\frac{V_G - V_{FB} - \Psi_s}{x_N} - \frac{Q_{ss}}{\varepsilon_N}\right]$ (where V_G=appied gate voltage, V_{FB}=flat band voltage, mainly due to the injected space charge Q_T, Q_{ss} interface state charge density) leads to $J_D = \frac{\varepsilon_N}{x_N}\frac{\partial V_{FB}}{\partial t}$ since the surface potential Ψ_s remains constant during accumulation and inversion gate voltage regimes. In other words, the shift of the C-V curve in time due to the change of V_{FB} and the time decay of the current are related to the same charge injection mechanism; the first one reflecting the stored charges, the last one being the charge flux.

As for the mobile carrier in this charge injection process dominantly one type carrier seems to be involved each case, i.e., electrons in the inversion and holes in the accumulation regimes. In this respect, at least two opposite type traps of equal efficiency (in the sense of concentration/cross section product), the one electron traps in inversion, the other hole trap in accumulation might be active inside the a-SiNx:H film. Moreover, their energy positions should be around midgap of a-SiNx:H film, at the proximity of silicon band gap. An adequate proposition might be the silicon dangling bond, the well known amphotheric K center [100] which is a negative correlation energy (U<0) defects: 2 K^0=K^++K^- is an exothermic reaction leading to stable intimate charged pairs (due to the charge transfer between singly occupied neutral K^0 centers. At equilibrium there are N/2 ionized K^+ (donor-like) center of energy level E_T and N/2 ionized K^- (acceptor-like) doubly occupied center of energy level E_T-U with the fermi energy pinned at about E_T-U/2. The unoccupied, singly and doubly occupied fraction of K centers at thermal equilibrium are expressed by f_0^+, f_0^0 and f_0^- respectively as follows [21]:

$f_0^+ = \frac{1}{Z}; f_0^0 = \frac{2\exp\left[\left(E_F - E_T\right)/kT\right]}{Z}$ and $f_0^0 = \frac{\exp\left[2\left(E_F - E_T + U/2\right)/kT\right]}{Z}$ with the partition function $Z = 1 + 2\exp\left[\frac{\left(E_F - E_T\right)}{kT}\right] + \exp\left[2\frac{\left(E_F - E_T - U/2\right)}{kT}\right]$. Within the frame of the above described defects type, the hopping transition occurs either between a K^0 center at one site to another K^0 center at the neighboring site or

between a K^- center and a K^+ center located in close proximity. The rate of charge density may be expressed as follows [101,102]

$$\frac{d}{dt}\left(N^+ - N^-\right) \approx P_{net} N^2 \left(\left(f^0\right)^2 - e^{-\frac{U}{kT}} f^+ f^- \right) \qquad (6.7)$$

where f^+, f^0, and f^- define the occupation probabilities of defetcs K^+,K^0 and K^- respectively which are reduced to the previously given thermodynamical distributions f_0^+, f_0^0 and f_0^-, N=total local concentration of the K centers.

The injection of cariers from both accumulation and inversion layers inside the a-SiN(C)x:H film might be seen as a ‘ thermalization’ of these stored charges, upto almost the position x_t inside the insulator (see fig.6.1) where a critical field is reached, limiting further trapping and enhancing the detrapping towards the relevant band by Poole-Frenkel barrier lowering [103]

6.2.4 Analytical outline of the capacitance voltage kinetics

The above summary in mind, now the analyses and discussion of the C-V curve time evolution under bias and temperature stresses may be interpreted by the following kinetic equation [104]:

$$\frac{dN_A(t)}{dt} = -N_A(t)\left[N_T - n_T(t)\right]S + Cn_T(t) \text{ with} \qquad (6.8\text{-a})$$

$$S = P_{eff}(t)\sigma_{eff}, \quad \sigma_{\text{eff}} = \sigma_p e^{-\frac{2x}{x_0}} \qquad (6.8\text{-b})$$

where σ_{eff} is effective capture cross section of trap located in the insulator at a distance x from the interface (because the capture probability of a carrier impinging upon the insulator is reduced by $e^{-\frac{2x}{x_0}}$ amount) [62], $N_A(t)$ is the number of charge through unit area in the semiconductor for an applied gate bias, N_T is the number of defects through unit area in SiN(C)x, and n_T is the number of filled ones,

respectively. The first and second terms of the right hand side of (6.8-a) represent the forward and reverse processes repectively. In the present condition, the reverse process may be ignored. The main assumption in the above equation is that the injected carriers do not reach the gate electrode. Taking into account the previously presented relations (6.3) and (6.6) the net hopping rate $P_{net}(t)$ and the time t becomes:

$$P_{net}(t) = \upsilon_{ph} \frac{qR}{kT} \frac{F_s(t)}{t^{(1-\alpha)}} \exp\left[-\frac{2R}{\lambda} - \frac{W}{kT}\right] \qquad (6.9)$$

with $F_s(t) = \dfrac{qN_A(t)}{\varepsilon_s}$.

Assuming both charge conservation, $q\left[N_A(t) + n_T(t)\right] = C_N\left[V_G - V_{FB}(t)\right]$ and the smallness of $n_T(t)$ in the presence of $N_T(t)$, the relation (6.8-a) becomes;

$$\frac{dN_A(t)}{dt} = -qN_A^2(t)Bt^{\alpha-1}$$

with $B = N_T\sigma_{eff}\left(\dfrac{qR}{kT\varepsilon_s}\upsilon_{ph}\right)\exp\left[-\dfrac{2R}{\lambda} - \dfrac{W}{kT}\right]$ (6.10)

The solution of the relation (6.10) with the boundary condition

$qN_A(0) = C_N\left[V_G - V_{FB}(0)\right]$

leads to:

$$\Delta V_{FB}(t) = \Delta V_{HH}(t) = \left[V_G - V_{FB}(0)\right]\left[1 - \frac{1}{1+\left(\dfrac{t}{\tau}\right)^{\alpha}}\right] \qquad (6.11)$$

with $\tau = \left\{\dfrac{\alpha}{BC_N\left[V_G - V_{FB}(0)\right]}\right\}^{1/\alpha}$.

6.3.5 Evaluation of the parameters involved in the flatband voltage shift.

Through computer controlled LABVIEW program, the $\Delta V_{HH}(t) \approx \Delta V_{FB}(t)$ curves were experimentally determined by Boonton 7200 capacitance meter as described in the section 6.2.4 at temperatures between 300-400 K under both strong accumulation and inversion gate voltage stresses. Examples of such measurements are given for both accumulation and inversion voltages in the fig. 6.7, respectively. It is worthwhile to note that the initial $V_{HH}(0)$ may be restored by applying the opposite stress voltage for a few minutes at the end of each temperature cycle. Qualitatively, the shapes of these two sets of curves seem to be similar although the variations for accumulation case is substantially more important. Using MATLAB minimization routine, the experimental sets of curves were fitted to the expression (6.11) and then the involved parameters $\Delta V_0 (=V_G - V_{FB}(0))$, τ and α were obtained for each temperature and given in table 6.1.Considering the relation (6.4), and (6.10), the quantity B may be put on the following form:

$$B = \frac{M_c}{T} \exp\left[-\frac{W}{kT} \right] \text{with } M_c = \frac{q \upsilon_{ph} R N_T \sigma_{eff}}{k \varepsilon_s} \exp\left[-\frac{2R}{\lambda} \right]. \qquad (6.12)$$

where the hopping range R is assumed independent of temperature; in other words the nearest neighbor hopping holds.

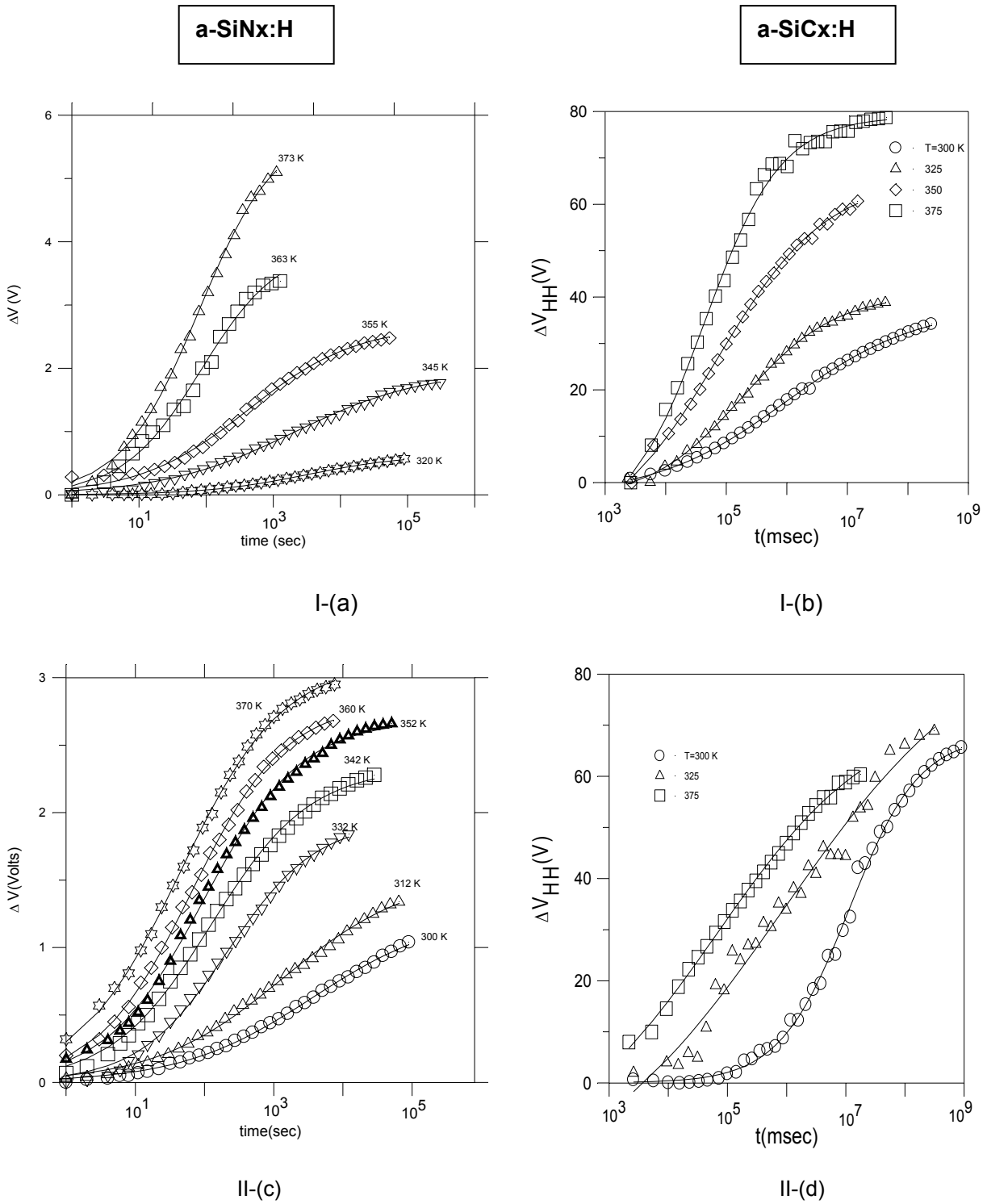


Fig.6.7 Time evolution of the capacitance vs. gate bias shift under; I-(a), (b) -30 and -50 V accumulating, II-(c), (d) +20 and +50 V inverting gate bias stresses at various temperatures for a-SiNx:H and a-SiCx:H films, respectively. Note that symbols are data, solid lines are obtained by fitting the relation (6.11) to the experimental points.

Table 6.1. Parameters ΔV_0, τ, α resulted from the fitting of eq. (6.11) to the experimental data of a-SiNx:H based MIS structure for each temperature/stress voltage pair.

V_G (V)	T (K)	ΔV_0 (V)	τ (s)
-30	310	1.203	15000
	320	0.6371	3204
	330	1.027	2705
	345	1.9727	2017
	355	2.6821	419.9
	363	3.9413	83.5
	373	5.8111	77.77
+20	300	1.2598	3672
	312	1.5466	1364
	320	2.0492	945.7
	332	1.9338	213.1
	342	2.3345	123.6
	352	2.6885	95.53
	360	2.7144	64.55
	370	4.512	28

The parameter B was evaluated by using the relation (6.11) and log(T B) vs 1/T has been plotted in the fig. 6.8 for accumulation and inversion stress voltages, respectively. From the slope of the graphs, activation energies of a-SiN(C)x:H film based MIS capacitor were obtained for accumulating and inverting gate biases, respectively and given in table 6.2. As discussed previously, in this process of charge redistributions, it is not impossible that carriers would try to hop to longer distances to find sites which would lie energetically closer than the nearest neighbors. Within the frame of this assumption R varies with temperature [96]:

$$R = \left(\frac{9q\lambda}{8\pi kN(E)}\right)^{1/4} \frac{1}{T^{1/4}}.$$

Using the relation (6.4) and (6.10), the expression of B becomes:

$$B = \frac{M_v}{T^{1/4}} \exp\left[-\frac{A}{T^{1/4}}\right] \text{with } M_v = \frac{N_T \sigma_{eff} q \upsilon_{ph}}{\varepsilon_s} \left(\frac{9q\lambda}{8\pi N(E)}\right)^{1/4}.$$

This assumption has been tested by plotting $\log\left(T^{1/4}B\right) \text{vs } T^{-1/4}$. The results, reported in the fig. 6.9, seem in agreement with the variable range hopping.

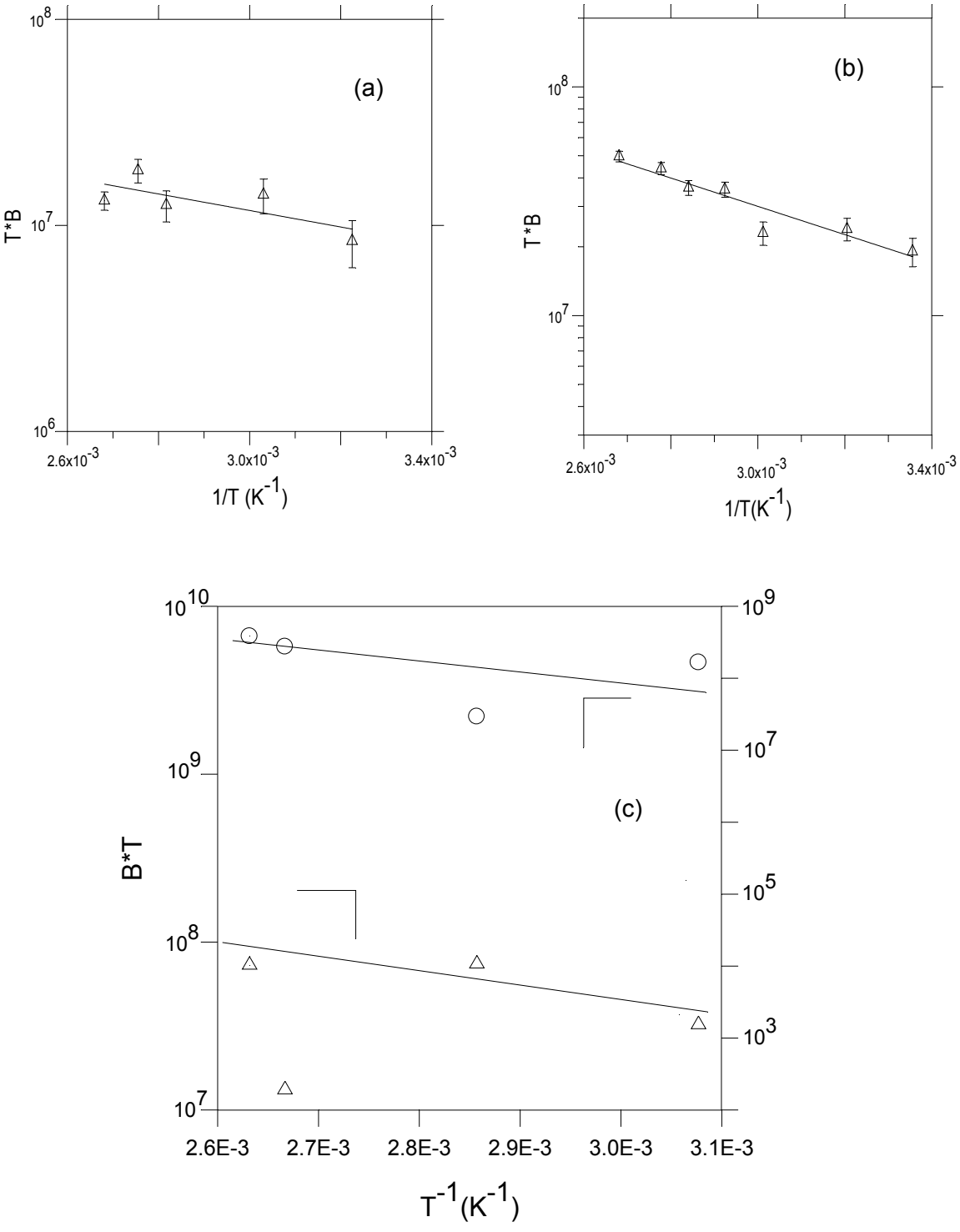


Fig.6.8Plotting of log (TxB) vs. 1/T for testing nearest neighbor hopping for both accumulating and inverting gate bias stresses on a-SiNx:H (a,b) and a-SiCx:H (c), respectively.

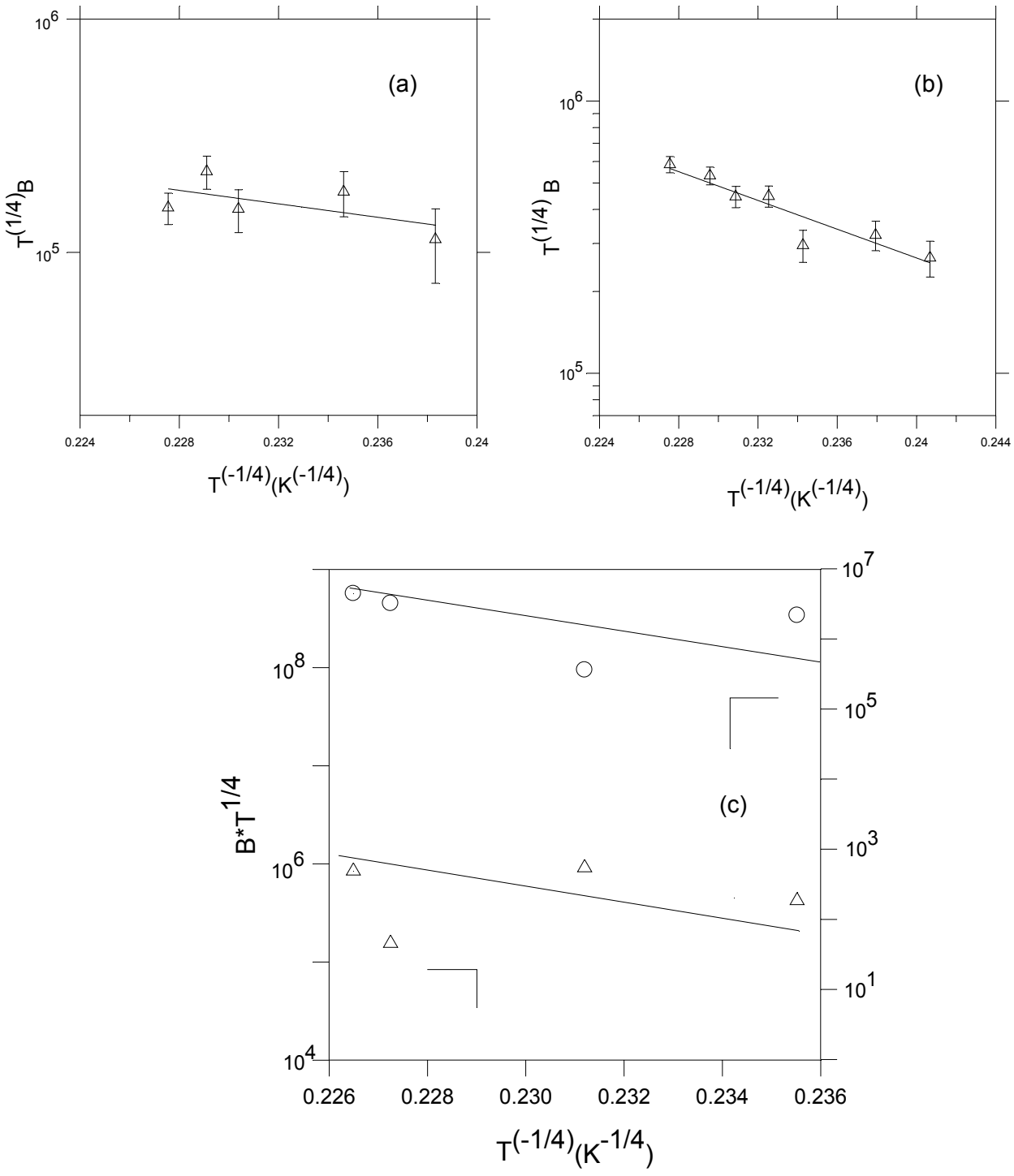


Fig.6.9 Plotting of log ($T^{1/4}$ xB) vs. $1/T^{1/4}$ for testing variable range hopping for both accumulating and inverting gate bias stresses on a-SiNx:H (a,b) and a-SiCx:H (c), respectively.

Table 6.2. R, W and N(E) are evaluated values of hopping range, activation energy and density of states are obtained from the nearest neighbor and variable range hopping graphs, respectively.

a-SiNx:H				
Nearest Neighbor hopping		*Variable Range Hopping*		
V_G (V)	W (eV)	λ (Å)	N(E) (x 10^{18} cm^3eV^{-1})	R(Å)
-30	0.11	12	12	61
20	0.12		8	68
a-SiCx:H				
-50	0.17	6	2.86	73
+50	0.17		2.93	73

The values of N(E) may be estimated as 9.6 10^{19} cm^{-3} eV^{-1} for accumulation and 6.3 10^{19} cm^{-3} eV^{-1} for inversion regimes from the slopes of the mentioned curves by taking [104] $\lambda \approx 6$ Å. However, these values for a-SiNx:H film seem towards the upper limit of acceptable range. This estimation of N(E) was repeated for a larger value of λ=12 Å (although slightly at the limit of an expected localization) and then more acceptable results given in table 2, were obtained. Moreover , for both reasonable penetration depth d_I-x_M [62] and attempt to hop frequency ranges [105], a speculation about N_T and σ_{eff} was attempted as given in the table 3.

Table 6.3.Speculation about N_T [100,106] and σ_{eff} values using both the values of $N_T\sigma_{eff}$ couple and the results given in table 2 for expected d_I-x_M and ν_{ph} values.

V_G (V)	N(E) ($cm^{-3}eV^{-1}$) x 10^{18}	R (Å)	$\delta=d_I-x_M$ (Å)	ν_{ph} (s^{-1})	$N_T\sigma_{eff}$ x10^{-6}	$N_T=N(E)\delta$ (cm^{-2}) x10^{12}	σ_{eff} (cm^2) x10^{-19}
-30	12	61	75-125	10^9-10^{11}	1.3-1.3x10^{-2}	9-15	0.8x10^{-2}-1.4
+20	8	68	75-125	10^9-10^{11}	2-2x10^{-2}	6-10	2x10^{-2}-3

The above analyses can be concluded as follows: although the investigation within the rather narrow temperature interval of 300-375 K could not allow to choose between nearest neighbor and variable range hopping, hopping in short as a dispersive rate limiting process seems consistent with the experimental results.

6.3 Depletion bias regime

Under the depletion bias regime (fig. 6.1), the direct tunneling of carriers from interface into the insulator traps seems to be less probable [52,61,63,64] due to the absence of accumulated carriers at the interface. Instead of direct tunneling, a two step mechanism is expected [52] (discussed in chapter 5). As given in fig.6.1, the corresponding characteristic time constants τ_t and τ_{ss} of these two independent parallel process might be assumed very different from each other (the probability of carrier exchange by the two step process is the product of individual probabilities corresponding to a longer characteristic time). Moreover, the rate limitation in this two step exchange might be imposed by the tunneling phenomenon [92], consequently $\tau_t \approx \tau_{ss} \exp\left[\frac{2x_t}{\lambda}\right]$. In other words, a trap of capture cross section σ_p located in the film at a distance x_t from the interface might be viewed by a

carrier at the interface as an effective trap with a capture cross section σ_{px} reduced by a factor $\exp\left[-\frac{2x_t}{\lambda}\right]$:

$$\sigma_{px} = \sigma_p \exp\left[-\frac{2x_t}{\lambda}\right] \tag{6.13}$$

6-3-1 Charge modulation effect on the admittance

The above described characteristic times τ_t and τ_{ss} are effective on the charge modulations of Q_t and Q_{ss} respectively (fig.6.1). It is well known that τ_t is related to both actual band bending ψ_s and trap capture cross section σ_p [48]:

$$\tau_{ss} = \left(\sigma_p v_{th} p_s\right)^{-1} = \left(\sigma_p v_{th} p_e\right)^{-1} \exp\left(\frac{q\psi_s}{kT}\right) \tag{6.14-a}$$

$$\tau_t = \left(\sigma_p v_{th} p_e \exp\left[-\frac{2x_t}{\lambda}\right]\right)^{-1} \exp\left(\frac{q\psi_s}{kT}\right) \tag{6.14-b}$$

where p_s and p_e (with $p_s = p_e \exp\left[-\frac{q\psi_s}{kT}\right]$) are free carrier concentration at the interface and in the silicon bulk, respectively. These two relations above might explain the two capacitance steps (corresponding conductance peaks) in the depletion bias regime (fig.6.2 and 6.3); the main step towards accumulation side might be due to the modulation of Q_t, and similarly, the smaller one (not always clearly distinguished) to that of Q_{ss}. The important difference in the preexponential factor of the above relations might be the reason of their appearance at distinct values of ψ_s, by the way, at different gate voltages V_G along the depletion region. The same effect may be assessed in the $C\left(\text{or}\,\frac{G}{\omega}\right)\text{vs.T}$ curves (see fig.6.10). The measured activation energies are almost the same ($\approx$0.4 eV), confirming the expression (6.14); one more confirmation of this expression may be seen in the temperature shift of these two steps from each other due to the difference of

effective time constants caused by the difference of effective capture cross sections discussed previously (eqn. 6.14).

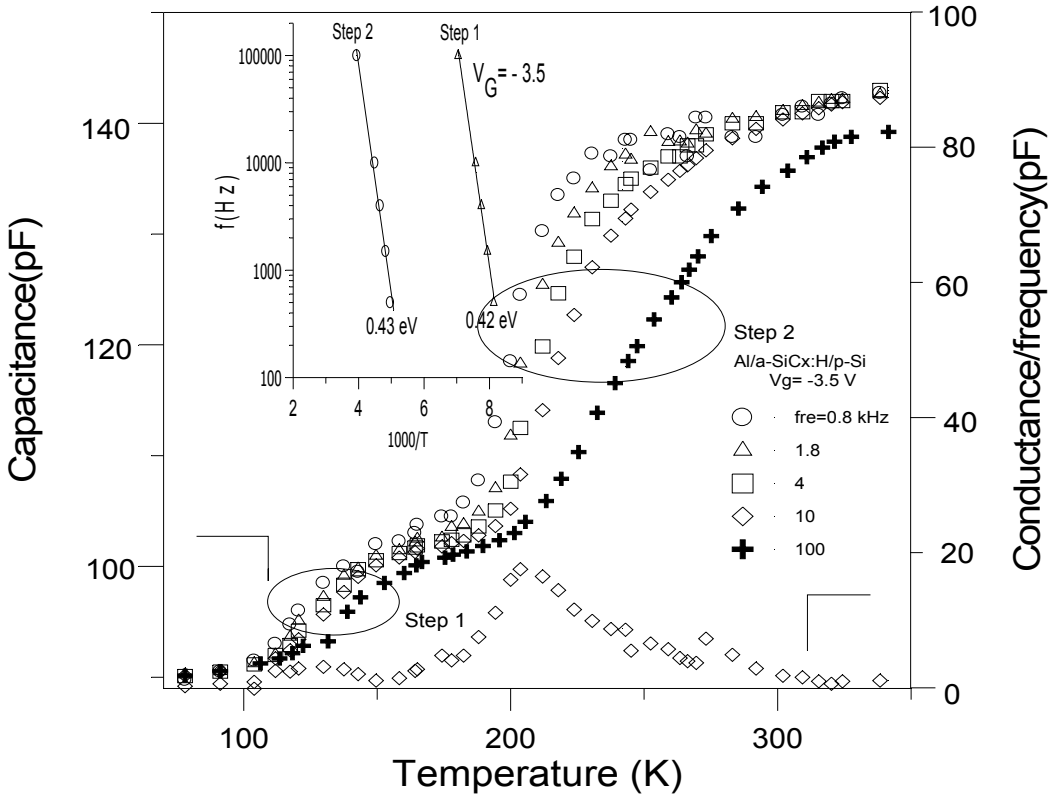


Fig.6.10 Admittance vs. temperature curves of the MIS structure (Al/a-SiCx:H/p-Si) as a function of a.c gate voltage modulation frequency.

In the case of accumulation bias regime (section 6.2), the relative frequency dependence of the space charges Q_t and Q_{ss} is considered (fig. 6.1). Let us discuss the behavior of Q_t: if a small amplitude a.c voltage of angular frequency ω is applied to the gate electrode, the modulation of localized states around both the Fermi level E_F, and the position d_I-x_t (measured from the gate side) is possible as long as both the free carrier supply and drain at the voltage modulation rate are satisfied. The energy depth $\Delta E_\omega \equiv E_\omega - E_F$ on either side of E_F (and parallelly Δx_ω on either side of d_I-x_t) is dependent on the modulation frequency ω. In other words, for a given couple of ω and temperature T, there exists an energy depth ΔE_ω (by the way, a spatial depth Δx_ω) such that the states within ΔE_ω are able to follow the

modulation, and the states beyond the depth ΔE_ω remain unchanged; for the boundary level (or position), the states can only partially respond to the modulation leading to the following condition:

$$\omega \tau_i = 1 \tag{6.15}$$

where τ_i = thermal emission (or release) time determined through the detailed balance calculation for the occupancy function f_t of localized states at E_F by the kinetics of carrier exchange [87] and $\tau_i = \upsilon_p^{-1} \exp\left[\frac{\Delta E_\omega}{kT}\right]$ with υ_p = attempt to escape frequency. The relation (6.15) becomes

$$\Delta E_\omega = kT \ln \frac{\upsilon_p}{\omega} \tag{6.16}$$

This expression points out roughly the extension of ΔE_ω, which is inversely frequency dependent. In chapter 2, the eventual distribution of localized states are discussed and a series of Gauss like distributed dangling bond (DB) states, shifted in energy from each other, is expected, leading to a more or less uniformly distributed density of localized states within the mobility gap apart from tail states. In light of this analysis and the relation (6.16), the modulation δQ_t of Q_t (fig. 6.1) might be considered as roughly proportional to ΔE_ω:

$$\delta Q_t = (const.) kT \ln \frac{\upsilon_p}{\omega} \tag{6.17}$$

The overall MIS capacitor may be considered as a parallel plate capacitor of capacitance C:

$$C = \frac{\varepsilon_{eff} A}{\bar{d}} \tag{6.18}$$

where the first plate is the gate electrode, the opposite second plate may be taken as a fictitious plate located at the position $\bar{d}$ from the gate; $\bar{d}$ is defined as a weighted average distance of all the charge modulations $\delta Q_s \left(= \delta Q_t + \delta Q_{ss} + \delta Q_A\right)$ to counter- balance the gate modulation δQ_G (see fig.6.1):

$$\bar{d} = \left[\frac{(d_I - x_t)\delta Q_t + d_I \delta Q_{ss} + (d_I + d_D)\delta Q_A}{\delta Q_s} \right] \qquad (6.19)$$

The relation (6.17) together with the expected frequency dependence of δQ_{ss}, C is strongly frequency dependent at depletion regime (see fig.6.2-b,c). The overall frequency dependence of the C-V_G curves may be carried out by plotting V_{FB} vs. log(ω) (fig 6.11). Moreover, on the same figure, the effective interface state density D_{it} were calculated around the flatband capacitance C_{FB} by the following relation [44]

$$D_{it} = A^{-1}\left[\frac{C_{FB}(C_I - C_{FB})}{3qkT[dC/dV]_{FB}} - \frac{C_I^2}{q^2(C_I - C_{FB})} \right] \qquad (6.20)$$

Similar variation of V_{FB} and D_{it} as a function of frequency seems consistent with the above discussion.

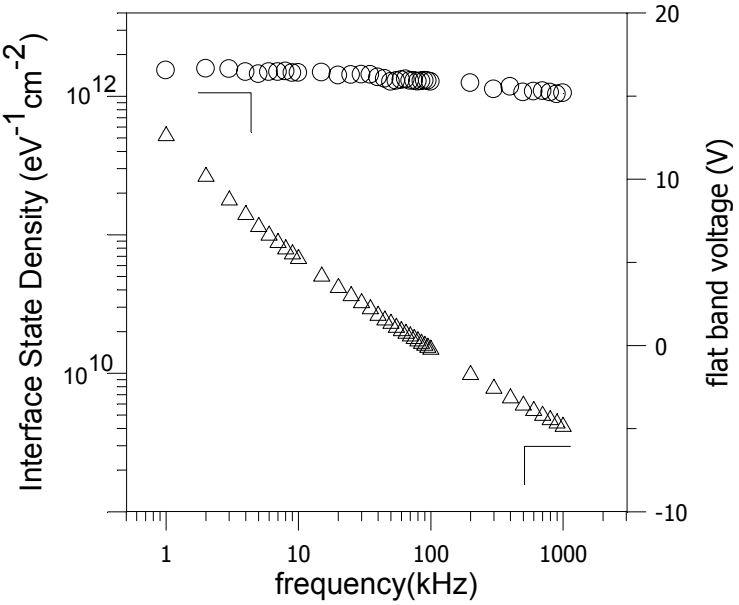


Fig.6.12 Flat band voltage and effective interface state density D_{it} at flat band configuration as a function of gate bias frequency.

6.3.2 DLTS Measurements

Deep level transient spectroscopy (DLTS) [107,108-119] as the conventional ac conductance technique [43] remains very attractive for determination of a great deal of information on the energy, concentration, and capture cross section of electrical interface traps.

The coexistence of traps of different origin or differing from a given trap by modification of the neighboring local environment inevitably leads to complex distributions of both trap energy and capture cross section throughout the band gap [48]. Consequently, the original large pulse DLTS signal requires complex data processing with rough approximations [117,119]. As a partial solution, a small signal (or energy resolved) version has been adapted to MIS samples, where a small injection pulse superimposed on a quiescent bias, V_G [112-117]. This quiescent bias, V_G, defining the position of the Fermi level at the surface of Si, may be used as a probe especially along one-half of the Si energy band gap by using depletion approximation. Interface traps of density D_{it} located in the lower half of the energy band gap of the p-type silicon substrate can be considered; the electron capture and emission process is neglected within the depletion approximation. The measurement involves the periodic application of small-voltage pulses δV_G of width t_p to drive a MIS capacitor from depletion towards accumulation to fill the interface traps in the region $E_F - \delta E$ around the Fermi level at surface E_F with majority carriers (holes). After returning to the quiescent gate bias V_G, emission of trapped carriers gives the capacitance transient $\delta C(t)$:

$$\delta C(t) = \frac{C_\infty^3}{\varepsilon_s N_A C_I} D_{it} \left[1 - \exp\left(-e_p t\right)\right] \delta E = \delta C(0) \left[1 - \exp\left(-\frac{t}{\tau_i}\right)\right] \qquad (6.21)$$

where C_∞=total MIS capacitance at the quiescent bias V_G, τ_i = characteristic thermal emission time discussed at the section 6.3.1.

Using linear correlation averaging [120], a comparison of the two different domains of the capacitance transient gives the DLTS signal as [112,114,121]:

$$S = \frac{1}{T_p}\int_0^{T_p} \delta C(t) F(t) dt \qquad (6.22)$$

where F(t)= weighting function, T_p = period of applied trap filling pulse. For our system, the equation can be reorganized by using its weighting function [122];

$$S = \delta C(0) \frac{1-\exp\left[-\frac{T_p}{2\tau_i}\right]}{T_p} \left\{ \tau_i \exp\left(-\frac{t_d}{\tau_i}\right) - (\tau_i - t_g)\exp\left(-\frac{T_p - 2t_p}{2\tau_i}\right)\right\} \qquad (6.23)$$

where t_p is the trap filling pulse width and $t_g=t_p+t_d$ with $t_d=\frac{T_p}{20}$ = the capacitance meter delay time [107,121-123].

By fitting the DLTS output S (eq.6.23), both the energy depth from the silicon valence band edge of probed energy interval δE and effective interface state density D_{it} may be evaluated from the positions in temperature (Arrheniuss plot) and height of the DLTS output extrema S_{ext} respectively [107,121-123]. Similar to $C\left(or\frac{G}{\omega}\right)$ vs. T curve, two series of peaks A and B were observed (see fig. 6.13-a,b). Both of them exhibit the same activation energy (~0.4 eV) illustrated in fig.6.13-c, confirming the analysis through the relation (6.14). The smaller peak (A) with shorter emission time, implying larger capture cross section, probably corresponding to the response of Q_{ss} (fig.6.1) leads to an effective density of state 4 x 10^{11} eV^{-1} cm^{-2}, the larger one (B) attributed to response of Q_t, gives a value of 10^{12} eV^{-1} cm^{-2} (fig. 6.13-b). As a result, the depletion regime of the MIS structure, may be unambiguously used for the determination of both the amount of injected charge carriers inside the film and density of states at film/silicon interface; these are extremely important for application point of view.

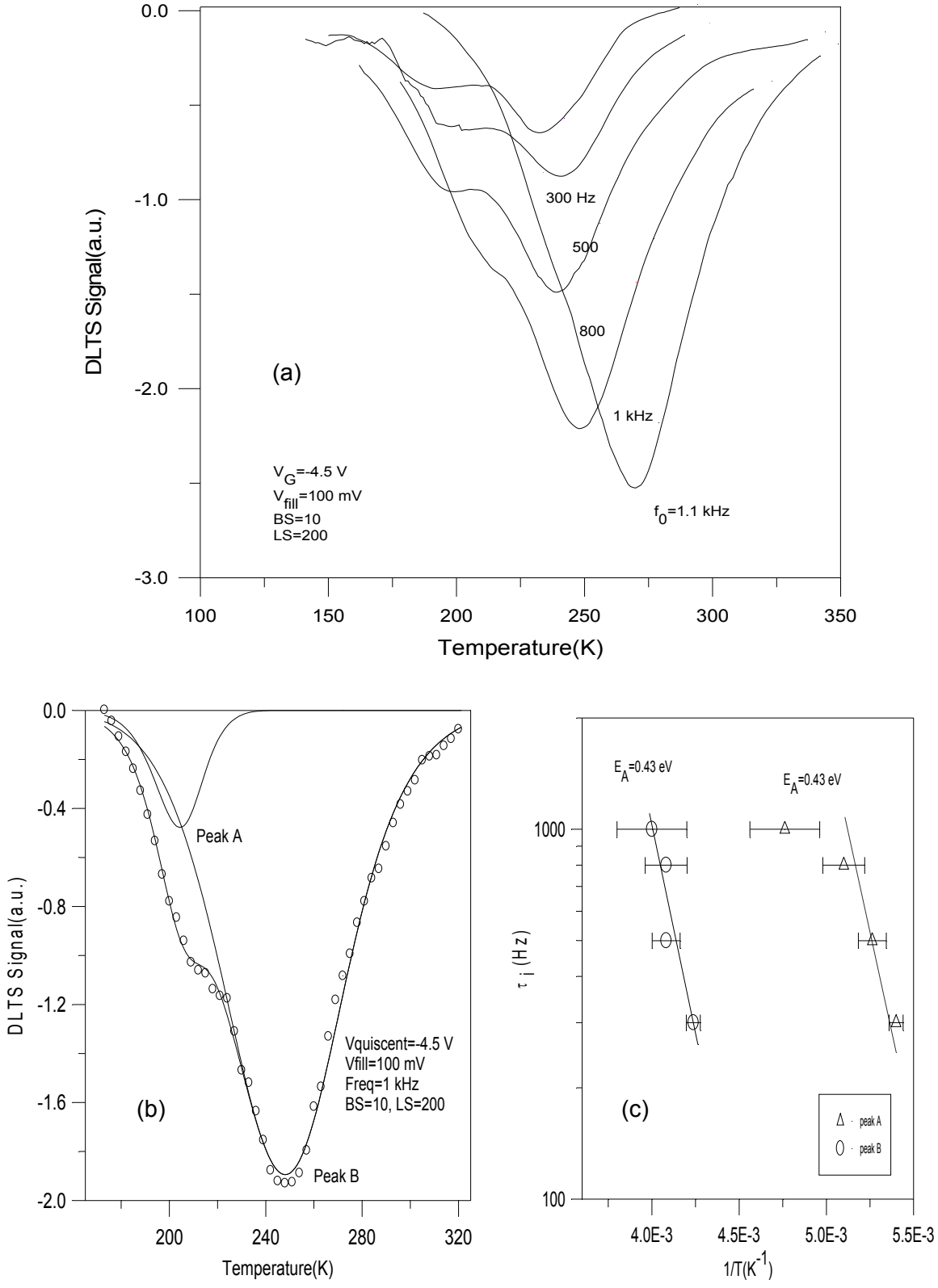


Fig. 6.13 (a) Small pulse DLTS spectra in temperature scan mode for MIS structure at constant gate bias for different frequencies. (b) Example of deconvolution procedure where symbol is data and solid lines are obtained by fitting to the S function of DLTS signal, (c) Arheniuss analysis of the emission rate for the two peaks in spectrum.

6.4 Ac Hopping conduction in intrinsic a-siCx:H film

In the case of dc hopping, the apparent C-V shifts due to ac effect was avoided by selecting the measurement frequency high enough. Now the analyses and discussion on slightly carbon rich intrinsic a-SiCx:H film in the form of MIS structure for both strong accumulation and inversion regimes will be interpreted by ac hopping conduction, assessed through admittance measurements (see fig. 6.14). In the figure, both conductance $\left(\frac{G}{\omega}\right)$ and capacitance (C) variations of the MIS structure as a function of dc gate bias voltage V_G for various ac modulation frequencies are given. Apart from almost expected voltage behavior, there is a remarkably strong frequency dependence. In reality, voltage and frequency dependences are interpenetrated. These curves exhibit two series of conductance peaks (and corresponding capacitance steps) for all frequencies except the low frequency range<20 Hz where only a single step is distinguished. Probably the silicon substrate at the interface might be slightly inverted (or injected) at zero dc gate bias voltage due to the huge density of localized states at the interface and within the film, depicted in fig. 6.14-c. The slight voltage dependence of the accumulation capacitance is due to the high density of localized states within the pseudo gap stretching the depletion towards the accumulation region[48,124,125]. For strong accumulation beyond V_G of about -15 volts, a saturated capacitance value was obtained. The qualitatively described phenomenon under accumulation in dc hopping case is also valid and may be simulated by the equivalent circuit given in fig 6.1. The measured accumulation capacitance C_{mp} (together with the measured parallel conductance G_{mp}) is related to the circuit elements:

$$C_{mp} = \frac{\left(C_t + C_c + \omega^2 C_c C_t^2 R_t^2\right)}{\left(1 - \omega^2 R_s R_t C_c C_t\right)^2 + \omega^2 \left(C_t R_t + R_s \left(C_c + C_t\right)\right)^2} \tag{6.24}$$

$$\frac{G_{mp}}{\omega} = \frac{\omega\left[C_t^2 R_t + R_s \left(C_c + C_t\right)^2 + \omega^2 R_s R_t^2 C_c^2 C_t^2\right]}{\left(1 - \omega^2 R_s R_t C_c C_t\right)^2 + \omega^2 \left(C_t R_t + R_s \left(C_c + C_t\right)\right)^2} \tag{6.25}$$

Similarly, the measured series accumulation capacitance (C_{ms}) and measured series resistance (R_{ms}) are related to the circuit elements:

$$C_{ms} = \frac{(C_c + C_t)^2 + \omega^2 C_c^2 C_t^2 R_t^2}{(C_c + C_t) + \omega^2 C_c C_t^2 R_t^2}, \; R_{ms} = \frac{C_t^2 R_t}{(C_c + C_t)^2 + \omega^2 C_c^2 C_t^2 R_t^2} + R_s \qquad (6.26)$$

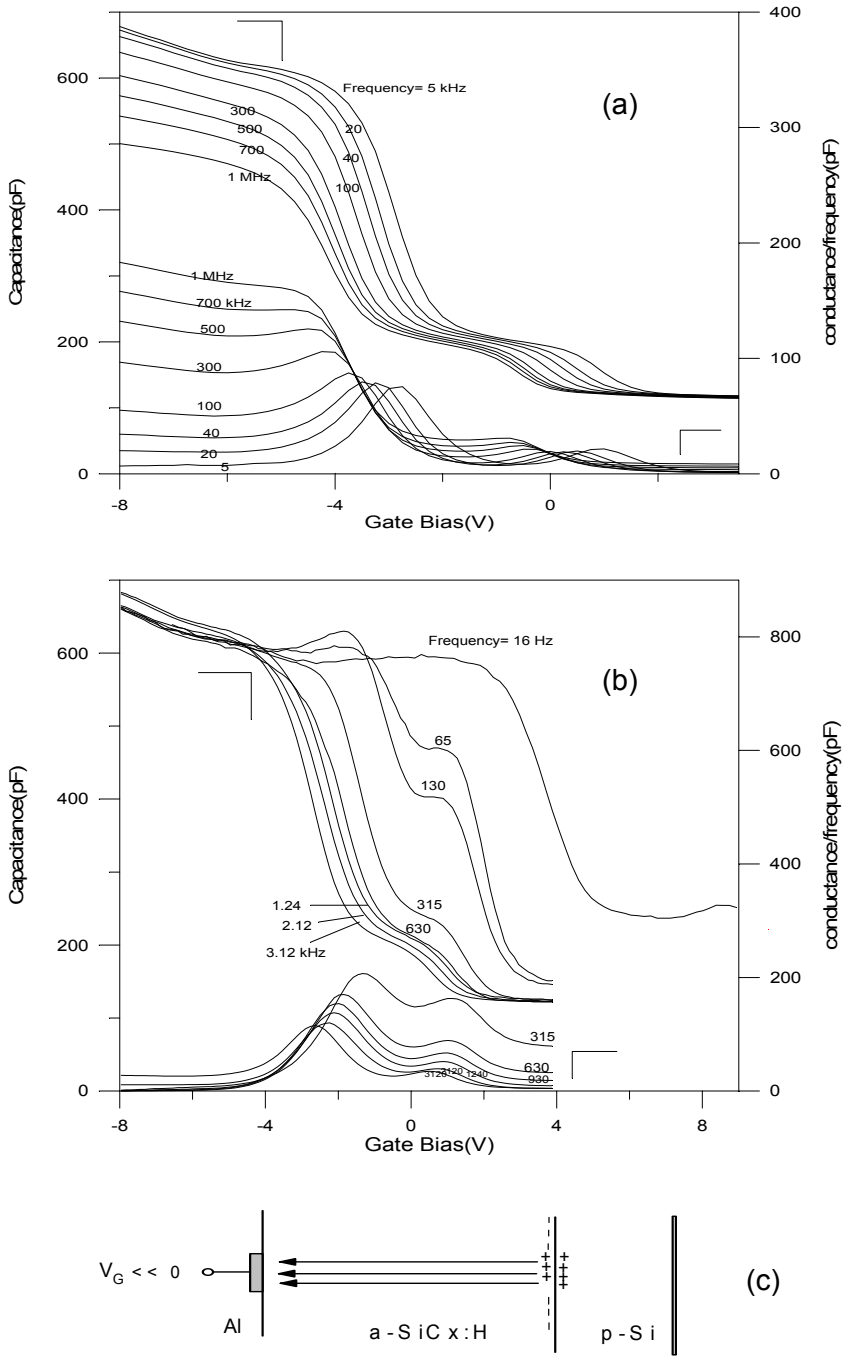


Fig.6.14 Admittance measurements of Al/a-SiCx:H/p-cryst. Si MIS structure as a function of gate bias: conductance and capacitance measured by both HP 4192A impedance analyzer for higher frequencies (a) and SR 830 Lock-in amplifier for lower frequencies (b). Schematic illustration of interface or injected charges around “interface” (c).

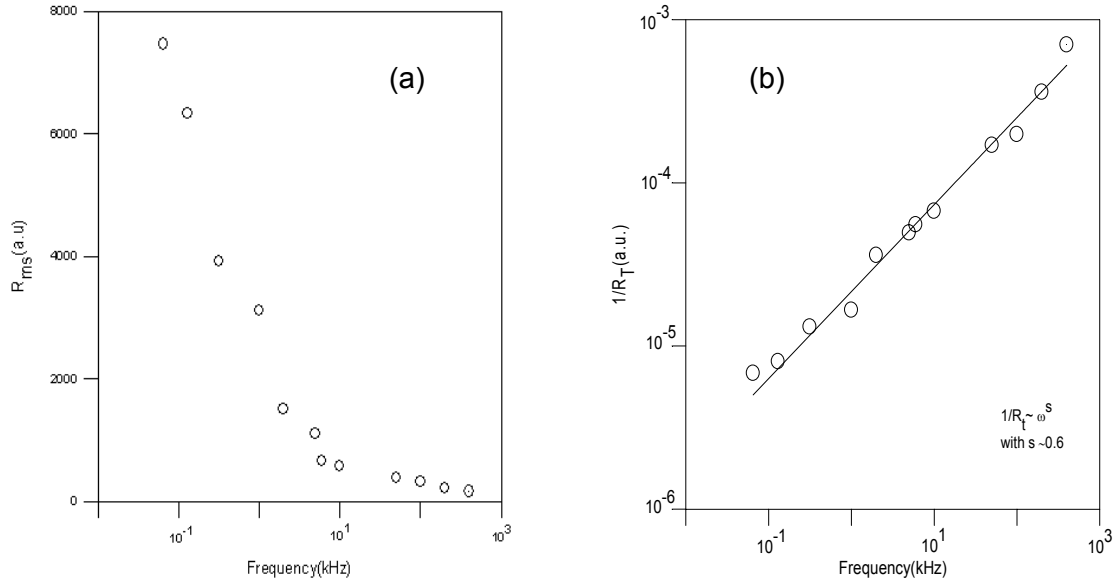


Fig. 6.15 (a) Evaluated R_{ms} as a function of frequency from the measured admittance, (b) extracted $1/R_T$ values (from the relation 6.27) as a function of ac modulation frequency to test the agreement with the prediction of ac hopping conductivity.

The frequency dependence of the admittance along the strong accumulation bias voltages (V_G<-4 Volts) may be originated from the more or less modulation of the injected charges Q_t (discussed elusively in previous section). In other words, increasing ac modulation frequency reduces δQ_t, a reduced δQ_t increases $\langle d \rangle$ which in turn decreases the accumulation capacitance C, in agreement with the capacitance values for V_G<-4 Volts as shown in fig.6.14-a. In the same figure, the measured parallel conduction $\frac{G}{\omega}$, on the contrary, increases substantially as a function of modulation frequency ω for each value of accumulation gate bias. An eventual series resistance R_s might produce qualitatively this type of admittance frequency dependence. Therefore, a Matlab program was used to evaluate series resistance R_{ms} as a function of frequency from the measured admittance, shown in fig.6.15. But the conventional series resistance correction [48] was not enough to remove the experimental frequency dispersion. The measured accumulation impedance (a capacitance C_{ms} in series with a resistance R_{ms}) has carried out that the series resistance is strongly frequency dependent (see fig. 6.15). The mentioned problem was solved by introducing a frequency dependent resistance, R_t, related to the path between the average position of δQ_t and interface as shown in fig.6.1 within the equivalent circuit diagram. Then, R_t was determined for each frequency

by using the relation (6.27) with the following parameters; C_c+C_t (≈670 pF) is lowest frequency capacitance value in the C-V curve where measured capacitance may be taken to be not affected by series resistance, C_c(≈ 520 pF) is the geometric capacitance of the film determined from the relation $C = \varepsilon A / d$ where ε and d were obtained through UV-Visible measurement and R_s (≈ 100 Ω) is the resistance of substrate, found by extrapolating the data in fig.6.15-a. The values of R_t^{-1} as a function of ac modulation frequency is reported on fig.6.15-b. The log-log plotting carries out a power dependence of R_t^{-1} on $\omega : R_t^{-1} \propto \omega^s$ with s≈0.6. This value of s is in agreement with the prediction of ac hopping conductivity [126]. The frequency dependence of the conductivity along the a-SiCx:H film is plausible within the model where the film is constituted by two phases, the first phase is more conductive π-bonded clusters dispersed randomly in a more resistive second phase of sp^3 bonded disordered matrix. Across such a structure, charges are stored at the boundaries between conducting and less conducting regions leading to time dependent polarization which in turn creates the frequency dependence of the conductivity[127]

Roughly, for the MIS structure at hand, during the dc gate bias voltage scanning from accumulation towards more positive values, the bias dependent capacitance range defines the depletion bias regime. A further change of dc gate bias towards more positive values, recreating the bias independent capacitance region, forms the inversion regime. In depletion, the direct percolation of carriers from interface into the insulator traps is not possible [52,61-64] due to the absence of stored carriers at the interface (the region under the gate electrode is depleted from the majority carriers, minority carriers are not yet generated enough and the inverted (or injected) layer at the interface beyond the gate, remains still disconnected from the region under the gate electrode, [128]). But indirect two step mechanism (tunneling + hopping) as described in previous section is plausible. This carrier percolation through the film contributes to the measured admittance by enhancing the exchange rate of SRH process compared to the exclusive interface process. This extra charging/discharging may be simulated by a parallel admittance Y_t to the one Y_{ss} associated with the interface SRH process alone as shown in the depletion equivalent circuit diagram given in fig.6.1. The characteristic capture time

of two step process related to the modulation of Q_t is substantially larger than that of single step process, related to the modulation of Q_{ss}. This difference in characteristic capture times, might explain the two series of conductance peaks (or capacitance steps) occurring at distinct gate bias voltages along the depletion region (the peak series towards accumulation side might be due to the modulation of Q_t [129]. Capture time τ is proportional to $e^{\frac{q\psi_s}{kT}}$ where ψ_s is the band bending at silicon surface; in turn, ψ_s increases with V_G and hence capacitance decreases for high frequencies shown in fig. 6.14-a and b. But, at lower frequencies than about 1 kHz, majority percolation still dominates the measured capacitance because of the fact that charges deep inside the film may respond ac modulation. As a result, first step moves toward strong inversion gate bias voltages at which already trapped holes are injected back to Si, and dc field is terminated by inversion and depletion charges. On the other hand, second step superimposed on the first one, (see fig.6.14-a and b), becomes visible with a slight increase in its height as frequency decreases below 1 kHz. This scenario is also confirmed by conductance peaks where smaller peak is superimposed on the larger one (i.e., first peak) again, clearly visible at low frequencies in fig.6.14-a,b.

Another feature seen in fig.6.14 is that C-V measurements do not exhibit the conventional MOS low frequency characteristics even at strong inversion regime; inversion charges may respond only dc voltage without being affected by ac modulation. In other words, the carriers would be trapped by surface states or traps inside the film where their exchange with silicon conduction band might be very slow process. The mechanism seems plausible since the band offset between crystalline Si and a-SiCx:H might greatly be located at the valence band side [130,131]. Therefore, minority carriers (inversion charges) might easily jump over or tunnel through a small barrier and get trapped inside the film in order to counterbalance the applied dc gate bias. Beyond a certain dc gate bias, depending on the frequency, both the capacitance and conductance are saturated to constant values C_s and G_s respectively, independent of bias. In turn, C_s and G_s are also frequency dependent (the lower the frequency, the higher C_s and G_s, see fig.6.14). This saturated admittance has been interpreted here by taking into account the lateral ac conduction at film/Si interface beyond the gate along more or less inverted (or

injected) layer [128]. The situation is depicted in fig.6.16 and a relevant equivalent circuit is added: C_c is the a-SiCx:H film capacitance, R_f (R_c) is the field dependent (independent) resistor, C_D is the depletion capacitance under the field plate and C'_D is the depletion capacitance beyond the field plate [128].

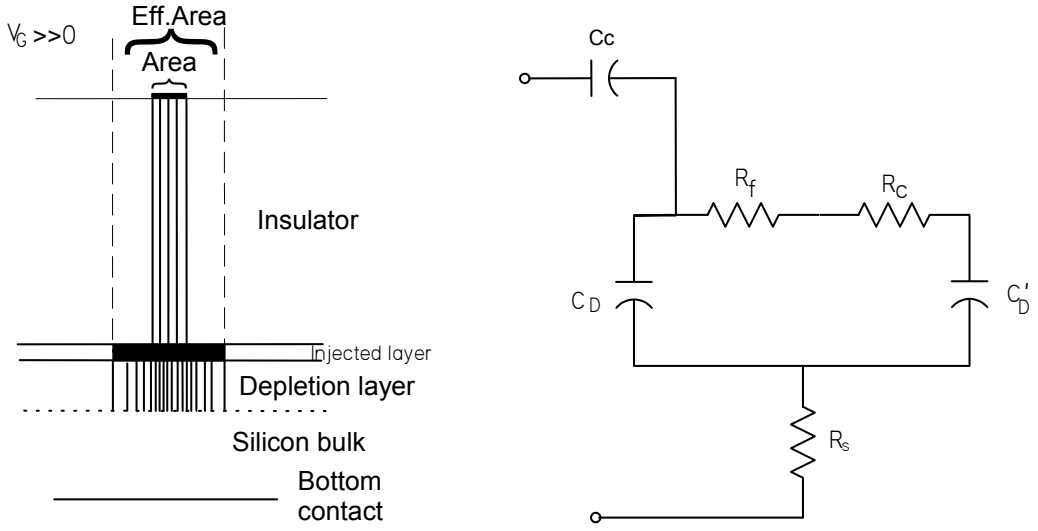


Fig.6.17 Schematic illustration of lateral ac conduction at film/semiconductor interface and is equivalent circuits.

For weak inversion and before, R_f^{-1} beneath the gate is low even zero; this voltage dependent R_f^{-1} increases with V_G connecting the inverted (or injected) layer beyond the gate. In other words, the ac current spreads laterally, enlarging the effective gate area, from the geometric value A to A_{eff}. A_{eff} increases inversely proportional to the modulation frequency, leading to $C'_D >> C_D$. This voltage independent C'_D increases the measured capacitance by decreasing the frequency and explains the bias independence of measured admittance. The admittance corresponding to the equivalent circuit in fig.6.16 may be expressed as a function of circuit elements as follows[48,128]:

$$\frac{G_s}{\omega} = \frac{\left(\omega g_{Tot} C_c^2 C_D'^2\right)}{\left(\omega^2 C_D'^2 \left(C_D + C_c\right)^2 + g_{Tot}^2 C_T^2\right)} \qquad (5.5.5)$$

$$C_s = \frac{C_c\left(g_{Tot}^2 C_T\left(C_D + C_D'\right) + \omega^2 C_D'^2 C_D\left(C_D + C_c\right)\right)}{\left(\omega^2 C_D'^2\left(C_D + C_c\right)^2 + g_{Tot}^2 C_T^2\right)} \qquad (5.5.6)$$

where $C_T = C_D' + C_D + C_c$, $g_{Tot} = R_{Tot}^{-1} = \frac{g_c g_f}{g_c + g_f}$ with $g_f = R_f^{-1}, g_c = R_c^{-1}$, and C_D is the depletion capacitance in the strong inversion regime As in the case of accumulation part, those equations were solved for g_{Tot} by iteration, after C_D was determined from the minimum of the capacitance ,C_{min} $\left(= \frac{C_c C_D}{C_c + C_D}\right)$,measured at high frequency limit. The iteration cycle was resumed for other measurement frequencies and the extracted g_{Tot} and C_D' were reported in the fig.6.18 where fairly good match is obtained between theory and experiment. As can be seen in these figures, g_{Tot} (C_D') get larger for higher (lower) measurement frequencies. The frequency dependence of g_{Tot} $\left(g_{Tot} \propto \omega^s \text{ with } s \approx 0.6\right)$ might carry out a lateral hopping conductivity inside a-SiCx:H around the interface.

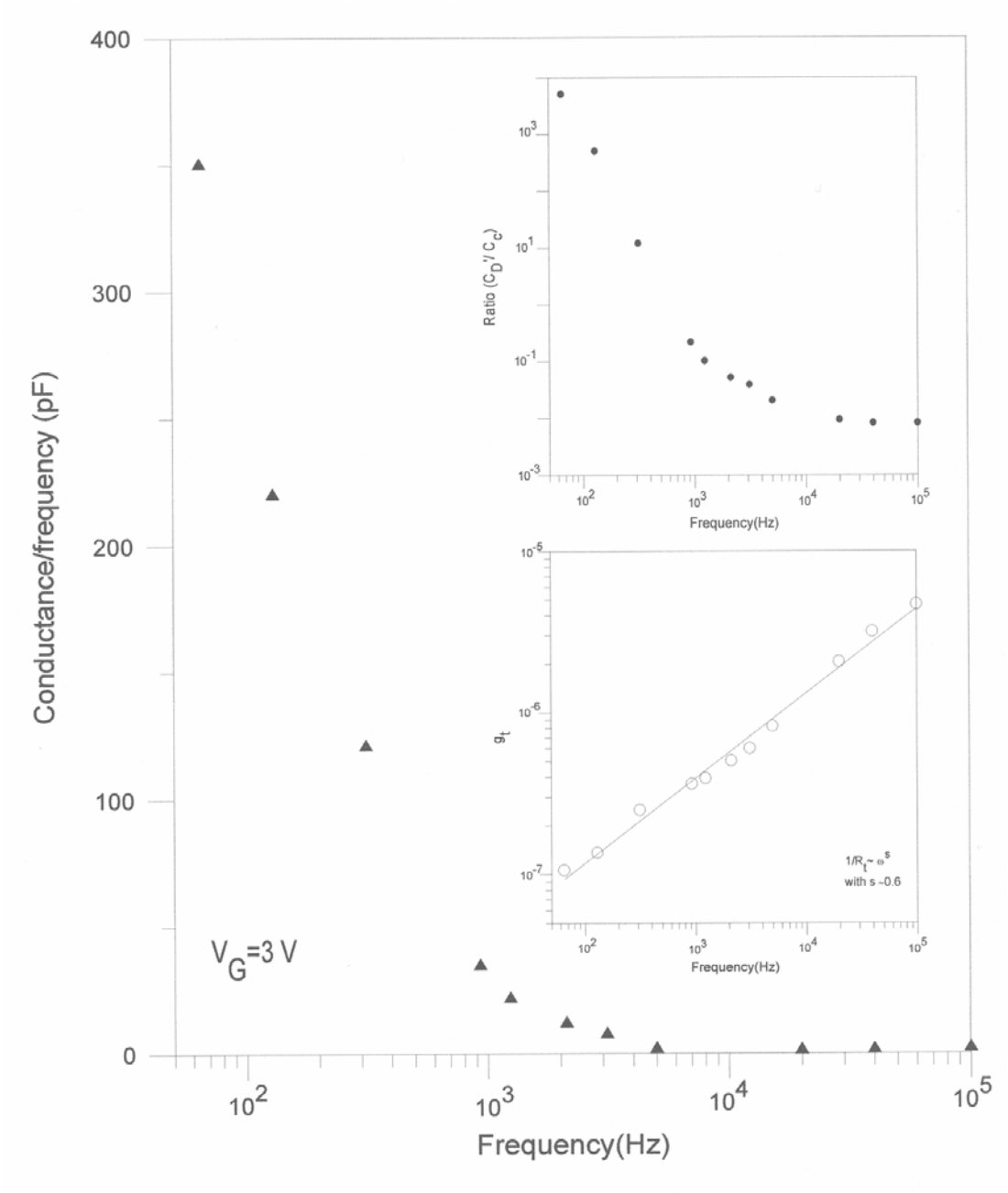


Fig. 6.18 Measured conductance vs. measuring frequency at constant gate bias (3 V) for Al/a-SiCx:H/p-Si MIS structure. Evaluated g_{Tot} and $C_D^{'}$ were also given as a function of frequency. Notice that log (g_{Tot}) vs. log(f) is a straight line with s≈ 0.6, consistent with percolation theory.

CHAPTER 7

CONCLUSIONS AND FUTURE WORKS

Besides microprocessors, large area electronics such as liquid crystals displays, optical scanners with 20-25 cm device dimensions are the other developing part of integrated circuit technology. In recent years, special attention has been devoted to the use of plasma enhanced chemical vapor deposition (PECVD) grown amorphous silicon alloys thin film in display and input/output technologies. The pixel, constituted by a pair of p-i-n photo sensing diode and switching thin film transistor (TFT) may be fabricated totally by various silicon based amorphous thin films. In that sense, in one side a-SiCx:H thin film for light sensing/emitting diode (p-i-n or Schottky), on the other side a-SiNx:H film as an insulator both for MIS and TFT structures were intensively investigated.

In this work, a-SiNx:H and a-SiCx:H thin films have been produced by PECVD technique on c-Si semiconductor in the form of MIS structure and both the quality of the production processes and films have been monitored with the determination of electrical characteristic of mentioned films with the c-Si interface via admittance measurements (Capacitance, conductance vs. gate bias, its ac modulation frequencies, and temperature measurements together with DLTS). Also, optical characterization of the mentioned films were investigated through FTIR and UV-Visible Transmission measurements as optical probing.

The main drawback of this a-Si:H technology for large area opto-electronics is metastability or degradation problems originated from continous evolution of the atomic configuration within the amorphous materials under the functioning circumstances. In that sense, instability phenomena (due to the creation of metastable states and charge injection/percolation into the gate electrode) were studied in both c-Si/a-SiCx:H and c-Si/a-SiNx:H heterojuctions. Specially, the time evolutions of both d.c current and flatband voltage of these heterojunctions, based on MIS structure, were worked by subjecting to bias/temperature stressing kinetics.

Then the enrolled trap energies leading to instability phenomenon were identified with temperature mode of DLTS and freezing out measurements.

According to experimental observations, the following points are remarkable; the accumulated charges (electrons or holes as to gate polarity) at the interface are percolated by tunneling and hopping throughout the insulator towards the gate electrode. This dispersive transport of carriers might occur through amphotheric type localized centers, active for both electrons and holes. These localized states might be attributed to the silicon dangling bonds in the a-SiNx:H, namely the famous K centers of negative correlated energy. The energy level of the positively charged centers would be distributed in energy around the silicon conduction band edge, that of the negatively charged centers would near the silicon valance band edge. This situation would allow the injection of accumulated electrons at strong inversion for the former case, the accumulated holes at strong accumulation for the latter case. The injection from the semiconductor to the insulator might be by direct tunneling or through the eventual interface trap mediated tunneling. However the rate limiting process seems to be dispersive hopping mechanism across the a-SiNx:H film.

It seems us that the discussion above for a-SiNx:H film is also valid for intrinsic carbon rich a-SiCx:H film once taking into account the structures of both a-Si:H and a-C:H films. The eventual localized state types and their distribution in a-SiCx:H have been qualitatively and descriptively outlined. Both the FTIR and UV-Visible transmittance tests indicate the presence of π-bonded graphitic clusters dispersed randomly in the “sea” of σ-sp^3 like tetrahedral disordered matrix.

As the main contribution of this work, MIS structure has been shown as a simple test device to study the ac hopping conductivity across intrinsic a-SiCx:H and a-SiNx:H films. The dependence of the ac conductivity on the frequency power $\left(\sigma \propto \omega^s \text{ with } s \approx 0.6\right)$ has been admitted as due to the eventual hopping mechanism.

At last, Combo Pattern Generator was implemented and then inverted staggered type thin film transistor was succesfully produced.

As a future works, the expertise gathered as a result of these works on c-Si (and/or a-Si:H)/a-SiNx:H (and/or a-SiCx:H) interface will be used in the characterization of TFT's and it seems that more intensive works to fabricate device quality insulator for TFT should be done once considering the image sensor arrays, which is much more complicated structure than TFT's.

APPENDIX A

REVIEW OF CONDUCTANCE ANALYSIS

Let us derive expressions for the admittance of the MIS capacitor as a function of bias and frequency to obtain the corresponding equivalent circuits (given in fig.4.8) which fit to experimental observations. Experimental evidence indicates that only capture and emission of majority carriers are important when measuring in the depletion region. Application of an ac signal results in a time varying Fermi function.

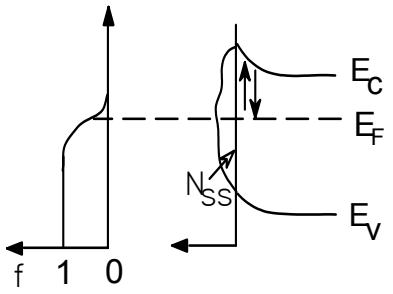


Fig A-1. Schematic diagram of band bending in depletion of silicon surface in n-type MIS capacitor.

Single Level Model:

From Schockley-Read-Hall statistics, the capture rate of electrons (or holes for p-type Si) by a single level interface state is (see fig.A-1)

$$R_n(t) = N_{ss} c_n [1 - f(t)] n_s(t) \qquad \text{(A-1)}$$

and the emission rate is

$$G_n(t) = N_{ss} e_n f(t) \qquad \text{(A-2)}$$

where N_{ss} is the density of states (cm^{-2}), c_n electron capture probability (cm^2/sec), e_n electron emission constant (sec^{-1}), f(t) is the Fermi function at

time t, and $n_s(t)$ electron density at the silicon surface at time t(cm^{-3}). Therefore, the net current density will be,

$$i_{ss}(t) = qN_{ss}c_n(1 - f(t))n_s(t) - qN_{ss}e_n f(t) \qquad \text{(A-3)}$$

Reporting both the Fermi function and the amount of charge density at the silicon surface as the sum of dc and ac part;

$$f(t) = f_0 + \delta f \qquad \text{(A-4-a)}$$

$$n_s(t) = n_{s0} + \delta n_s \qquad \text{(A-4-b)}$$

with f_0 is the Fermi function, corresponding to dc gate bias, V_G, and δf is the change caused by ac signal, n_{s0} is the charge density at the silicon surface when the Fermi level is at the trap level and δn_s is the change caused by ac signal. Expressing the emission rate (e_n) in terms of capture one (c_n) from the balance equation $\left(= e_n = c_n(1 - f_0)n_{s0}/f_0\right)$ and substituting the above relations into the net current density relation (eq.A.3) leads to ;

$$i_{ss}(t) = qN_{ss}c_n\left[(1 - f_0)\delta n_s - n_0\frac{\delta f}{f_0}\right] \qquad \text{(A-5)}$$

On the other hand, redefining the net current density as $\left(i_{ss}(t) = qN_{ss}\, df/dt\right)$, and equating the relation (A-3) and solving for df/dt yields;

$$\frac{df}{dt} = c_n(1 - f_0)\delta n_s - c_n n_{s0}\frac{\delta f}{f_0} \qquad \text{(A-6)}$$

The small signal variation of the Fermi function is defined as $\delta f = f_m e^{j\omega t}$, hence time variation will be equal to the relation given below;

$$\frac{df}{dt} = j\omega\delta f \qquad \text{(A-7)}$$

Rearranging the relation (A-6) and (A-7) and extracting δf causes to:

$$\delta f = \frac{f_0(1 - f_0)\delta n_s}{n_{s0}\left[1 + j\omega f_0/c_n n_{s0}\right]} \qquad \text{(A-8)}$$

Substituting the eq.(A-8) into (A-5) yields the net current density as;

$$i_{ss}(t) = \frac{j\omega q N_{ss} f_0(1 - f_0)\delta n_s}{(1 + j\omega f_0/c_n n_{s0})n_{s0}} \qquad \text{(A-9)}$$

with $\delta n_s / n_{s0}$ term is equal to the ac surface potential $\left(\equiv \delta u_s = \frac{q\psi_s}{kT} \right)$ where ψ_s is the silicon band bending in terms of kT/q. Finally, the equation (A-9) turns out to be

$$i_{ss}(t) = Y \delta \psi_s \quad \text{(A-10-a) with } Y = j\omega \frac{q^2}{kT} \frac{N_{ss} f_0 (1 - f_0)}{(1 + j\omega f_0 / c_n n_{s0})} \quad \text{(A-10-b)}$$

The relation (A-10-b) is the admittance of a series RC network with capacitance $C_{ss}\left(= \left(q^2 N_{ss} f_0 (1 - f_0)\right) / kT\right)$ and time constant $\tau_{ss}\left(= f_0 / c_n n_{s0}\right)$, respectively. Separating real and imaginary parts (due to the fact that impedance analyzer was implemented to measure admittance in parallel mode though it has ability to measure in series mode as well), the equivalent conductance and capacitance are obtained as follows:

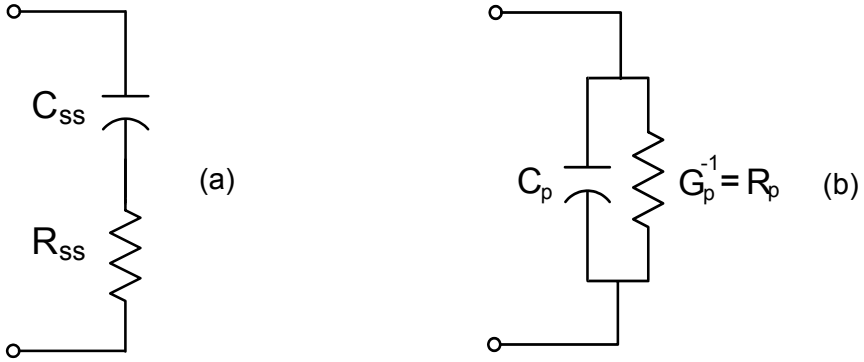


Fig. A.2 (a) Interface trap admittance of RC branch and (b) derived relevant quantities.

$$G_p = \frac{C_{ss} \omega^2 \tau_{ss}}{1 + \omega^2 \tau_{ss}^2} \quad \text{(A.11-a) ,}$$

$$C_p = \frac{C_{ss}}{1 + \omega^2 \tau_{ss}^2} \quad \text{(A.11-b)}$$

On the contrary, for an MIS capacitor, the total charge density at a given bias will be

$$Q_T=Q_s+Q_{ss}+Q_f \qquad \text{(A.12)}$$

where Q_s is the silicon space charge density, Q_{ss} is the surface state charge density and Q_f is the fixed charge density in the insulator. The ac current density, $i_T(t)$ $\left(\equiv dQ_T/dt\right)$ would be;

$$i_T(t)=i_s(t)+ i_{ss}(t) \qquad \text{(A.13)}$$

where $i_s(t)$ and $i_{ss}(t)$ are the ac current densities changing the silicon space charge layer and interface states, respectively. To obtain the former one, $i_s(t)$, variation of current with respect to band bending has to be considered: $i_s(t)=\frac{dQ_{sc}}{d\psi_s}\frac{d\psi_s}{dt}$ with $\psi_s(t)=\psi_{s0}+\delta\psi_s$ is the silicon band bending in volts at a time t, ψ_{s0} is the silicon band bending corresponding to the applied gate bias and $\delta\psi_s=a\exp(j\omega t)$. Therefore, time variation would be $d\psi_s/dt=j\omega\delta\psi_s$. As for the latter one, $dQ_s/d\psi_s=C_D$ is the depletion layer capacitance. Consequently, $i_s(t)=j\omega C_D\delta\psi_s$ and $i_{ss}(t)=Y_{ss}\delta\psi_s$. Substituting the result to the relation (A.13) yields

$$i_T(t)=(j\omega C_D+Y_{ss})\delta\psi_s \qquad \text{(A.14)}$$

The results suggest that C_D appears in parallel with the series RC network of the surface states for a single energy level. Rearranging Y in terms of real and imaginary parts yield

$$C_p=C_D+\frac{C_{ss}}{1+(\omega\tau_{ss})^2} \qquad \text{(A.15-a)}$$

$$\frac{G_p}{\omega}=\frac{C_{ss}\omega\tau_{ss}}{1+(\omega\tau_{ss})^2} \qquad \text{(A.15-b)}$$

Equation A.15-b depends only on the surface state and goes through a maximum when $\omega\tau_{ss} = 1$, and equal in magnitude to $C_{ss}/2$ there. Thus, equivalent parallel conductance corrected for insulator capacitance gives C_{ss} and τ_{ss} directly from the measured conductance. Keep in mind that the discussion above is just for having the reader to be familiar to the admittance concept, and exhibiting the way as the physical quantities can be represented by equivalent circuit using circuit theory. Single energy level was assumed just for pedagogical purposes though it was far away for the representation of actual MIS structure via admittance analysis.

Distribution of Levels, Continuum Model:

One possible modification over the discussion above might be including the surface states that observed to be comprised of many levels so closely spaced in energy that they can not be distinguished as separate levels. Equivalent depletion circuit diagram for continuum model is given in fig A.3.

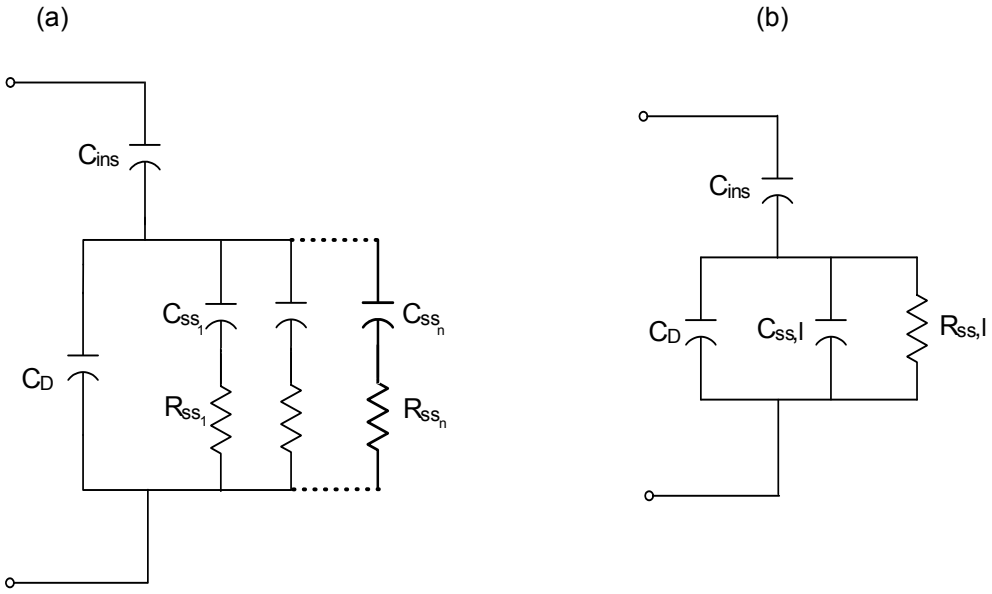


Fig. A.3 (a) Equivalent depletion region circuit of MIS capacitor as to continuum model, (b) Lumped parallel equivalent of circuit, $C_{ss,I}$ and $R_{ss,I}$ given in (a). Note also that, C_{ins} is added to the circuit.

For a continuum of states, capture and emission of majority carriers can occur by states located within a few kT/q on either side of the Fermi level. The admittance of the continuum is obtained by integrating eq.(A.10-b) over the band gap

$$Y = j\omega \frac{q^2}{kT} \int \frac{N_{ss} f_0 (1 - f_0) d\psi}{(1 + j\omega f_0 / c_n n_{s0})} \qquad (A.16)$$

The integrand of eq. A.16 is sharply peaked about the Fermi level with a width of kT/q. Making the substitution $f_0(1 - f_0) = kT/q\,(df_0/d\psi)$ turns an integral over f_0 where f_0 changes from 0 to unity. After performing the integration, the admittance will be

$$Y = \frac{qN_{ss}}{2\tau_m} \ln(1 + \omega^2 \tau_m^2) + jq \frac{N_{ss}}{\tau_m} \arctan(\omega \tau_m) \qquad (A.17)$$

with $\tau_m = 1/c_n n_{s0}$.

Real part of eq. (A.17) gives the conductance as

$$\frac{G_p}{\omega} = \frac{qN_{ss}}{2\tau_m} \ln(1 + \omega^2 \tau_m^2) \qquad (A.18)$$

The technique is called hereafter as *continuum model*. Once the conductance curves for continuum model are compared with that of single level model, it seems that the width of the peak at half maximum is greater, the conductance peak has been shifted from $\omega\tau = 1$ to $\omega\tau = 1.98$ and the peak magnitude (G_p/ω) has decreased from 0.5 to 0.403 C_{ss}. Though continuum model gives better results compared with single level, it is not adequate to explain the experimental results where conductance peaks remain much wider and of lower amplitude, necessitating further improvement.

Statistical Model:

To remove this contradictory broadening, Nicollian and Goetzberger proposed a statistical model, based on the non-uniform distribution of surface band bending over the interfacial plane, yielding time constant dispersion. As time constant, τ , has an exponential dependence on band bending $\left(\tau_p^{-1} = c_p N_A \exp\left[-q\psi_s / kT\right]\right)$, small variations on ψ_s will produce large variations on τ . In the mentioned model, the entire gate area is divided into many small patches where band bending and depletion layer width (W) are nearly uniform for each patch but varies from patch to patch. In the light of this information, the modified equivalent circuit diagram of the MIS capacitor (given in fig A.4) is composed of parallel array of elementary capacitors, each corresponding to a different patch.

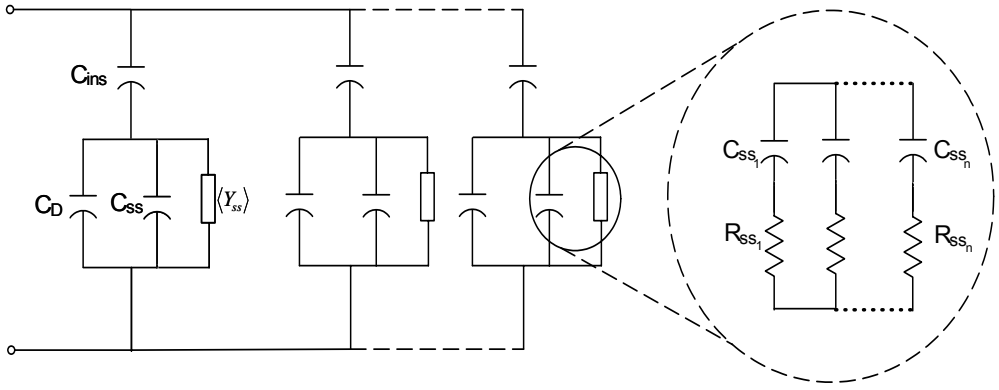


Fig.A.4 Revised form of circuit diagram for statistical model. Note that C_D is different as given in continuum model; it varies from branch to branch as discussed in the text.

Therefore, surface state admittance, Y_{ss}, represent only a single patch. To express the surface state admittance for the whole patches, band bending fluctuations in Gaussian form (due to the fact that interface charge density is assumed to have an Gaussian distribution) has to be considered. As a result, the surface state admittance would be

$$\left\langle Y_{ss} \right\rangle = q \int_{-\infty}^{+\infty} \overline{Y}_{ss}(u_s) P(u_s) du_s \text{ with } P(u_s) = \left(2\pi\sigma_s^2\right)^{-1/2} \exp\left[-\frac{\left(u_s - \overline{u}_s^2\right)}{2\sigma_s^2} \right] \quad \text{(A.19)}$$

where $\overline{Y}_{ss}(u_s) \equiv Y_{ss}$ is the surface state admittance over the silicon band gap and averaged over the surface state level distribution for any given band bending u_s (with $u_s = \psi_s / kT$) and $\langle Y_{ss} \rangle$ represent the surface state admittance after further averaging over band bending variations, σ_s is the variance of band bending in terms of kT/q and $\overline{u}_s$ is mean value of band bending. In the light of this information, derived conductance expression for continuum model turns out to be

$$\langle G_p \rangle \Big/ \omega = \frac{q}{2} \int_{-\infty}^{+\infty} \frac{N_{ss}}{\omega\tau} \ln\left(1 + \omega^2 \tau^2\right) P(u_s) du_s \qquad \text{(A.20)}$$

Assuming the surface state level density N_{ss} and majority carrier capture probability c_p as constant, they can be taken outside of the integrand. After inserting the relation for time constant and Gaussian probability into the above relation, the conductance expression would be

$$\frac{\langle G_p \rangle}{\omega} = qN_{ss}\left(2\pi\sigma_s^2\right)^{-1/2} \left(\frac{c_p N_A}{\omega}\right) \int_{-\infty}^{+\infty} \exp\left[-\frac{\left(u_s - \overline{u}_s^2\right)}{2\sigma_s^2}\right] \exp(-u_s) \tan^{-1}\left(\frac{\omega}{c_p N_A} \exp(u_s)\right) du_s \qquad \text{(A.21)}$$

Defining a new variable to eliminate $(c_p N_A)$ term from the emission rate via $\xi = \omega\tau_p = \omega(c_p N_A)^{-1} \exp(\overline{u}_s)$, conductance expression turns out to final form as

$$\frac{\langle G_p \rangle}{\omega} = \frac{qN_{ss}\left(2\pi\sigma_s^2\right)^{-1/2}}{2\xi} \int_{-\infty}^{+\infty} \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) \exp(-\eta) \ln\left(1 + \xi^2 \exp(2\eta)\right) d\eta \qquad \text{(A.22)}$$

with $\eta = u_s - \overline{u}_s$. Derived expression for conductance in the light of statistical model is satisfactory in fitting results compared with other models, hence interpretation of experimental conductance data is made through the last model.

APPENDIX B

MEASURING TOOLS AND TECHNIQUES

Due to stringent requirements imposed by modern technology, improvement of interface properties and minimization of interface trap density is absolutely necessary for both MIS and TFT structures. On one side, film properties (intrinsic, doped semiconductor and insulator film) alone was investigated via both fourier transform infrared spectroscopy (FTIR) and UV-Visible transmission measurements as optical probing and on the other side, film/semiconductor interface properties and quality of produced film was studied by means of MIS and TFT structures through current-voltage (I-V), admittance (capacitance and conductance measurements) and deep level transient spectroscopy (DLTS) as electrical probing. Let us give an detail information about the mentioned techniques and observations of produced films via application of mentioned techniques.

B-1 Electrical Measuring Equipments

B-1-1 Current Voltage

The current voltage characteristic (shown in fig.4.10) was obtained via Keitley 6517 electrometer and then resistivity of the produced film was calculated around 10^{15} Ω cm by finding the ohmic region up to 5 x 10^4 V cm^{-1} in the J-E curve. The error in the resistivity is estimated to be around 2 x 10^4 Ω cm due to fluctuation of the measured currents.

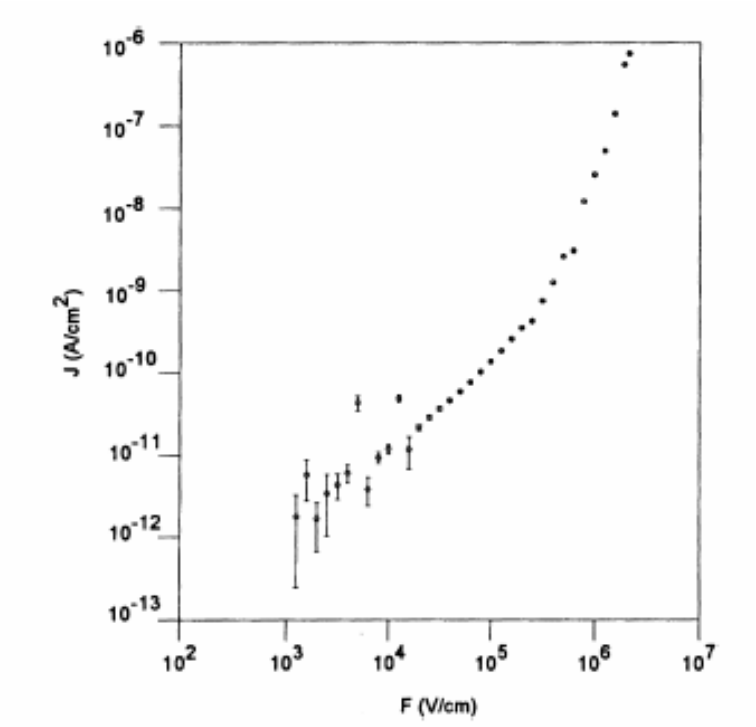


Fig.4.10. Current density (J) vs. electric field (E) of Cr/a-SiNx:H/p-Si structure.

The J-F characteristics shows the quality of film as ohmic region dominates up to F=5 x 10^4 V cm^{-1} region where tunneling or space charge current starts to dominate the current mechanism. The resistivity of the film, around 10^{15} Ω cm is also within the range of resistivities of the a-SiNx:H films used in the TFT strucuttures [132,133].

B-1-2 Measuring System at low and high frequency C-V measurements

C-V measurements were achieved through a computer controlled program for slow, intermediate and high measuring frequencies. Let us present roughly the relevant equipments and their principal of measurements.

(a) **Quasistatic C-V measurements**

The quasi-static C-V meter (Keitley 595) gives the lowest frequency capacitance of the sample. The circuit diagram of the system is given below where a small voltage step is applied to the test sample after C_F is discharged (by closing the

switch S) and a charge $\left(\Delta Q = C_x \Delta V\right)$ transferred into the integrator is measured (by determining the amount of charges before and after voltage step).

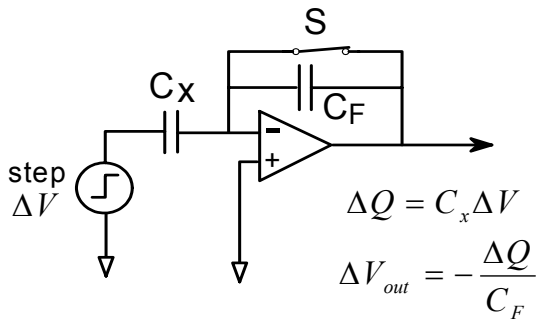


Fig.B.1 Circuit diagram of Quasistatic C-V meter

Hence, the unknown capacitance can be calculated through the following relation;

$$C_x = \frac{\Delta Q}{\Delta V} = -C_F \frac{\Delta V_{out}}{\Delta V} \qquad \text{B-1}$$

However, the actual situation for MIS structure is a bit different than discussed above due to the presence of (more or less) leakage currents that quasistatic C-V meter is able to measure and correct the amount of leakage current (below 10^{-11} A) from the measured capacitance. For a bit more clarity, the procedure is as follows: three measurements of voltage output (V_{out}) are made as shown in fig.B-2, since each measurement corresponds to the charge integrated up to a given time. The measurements mentioned above are labeled Q_1 (= baseline charge immediately preceding the voltage), Q_3 (=final charge transferred through the test sample after a specific time) and Q_2 (= charge measured before Q_3).

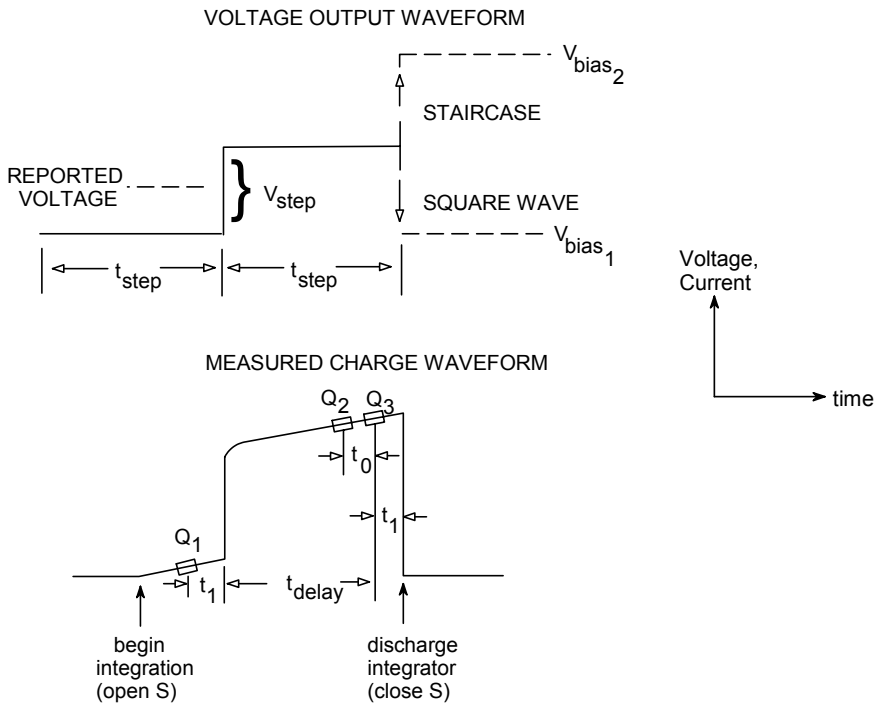


Fig.B-2 Schematic representation of determination of leakage current while quasistatic C-V measurements.

By means of these three charges, both corrected capacitance and leakage current can be determined. In the absence of dc current, the device is thought to be in equilibrium and the correct value of the measured capacitance can be obtained through determination of Q_1 and Q_3 charges solely. Hence, the capacitance would be;

$C_{LF} = \dfrac{Q_3 - Q_1}{V_{step}}$. Otherwise, in the presence of dc leakage current $\left(Q/t = \left(Q_3 - Q_2\right)/t_0\right)$, this current should be determined and substracted from the measured capacitance (with Q/t designating the amount of leakage current, t_0 is the delay time). In light above information, the corrected low-frequency capacitance is obtained as:

$$C_{LF(corrected)} = C_{LF} - \frac{Q}{t}\frac{\left(t_{delay} + t_1\right)}{V_{step}} \qquad \text{B-2}$$

where t_{delay} is the delay time necessary to obtain equilibrium measurement. The equilibrium could be recognized either C or Q/t vs. Delay time: in the former,

quasistatic capacitance value in inversion region rises from the depletion value to approach insulator capacitance, C_{ins}, in the latter, Q/t is at the dc leakage of the system (shown in fig.B-3).

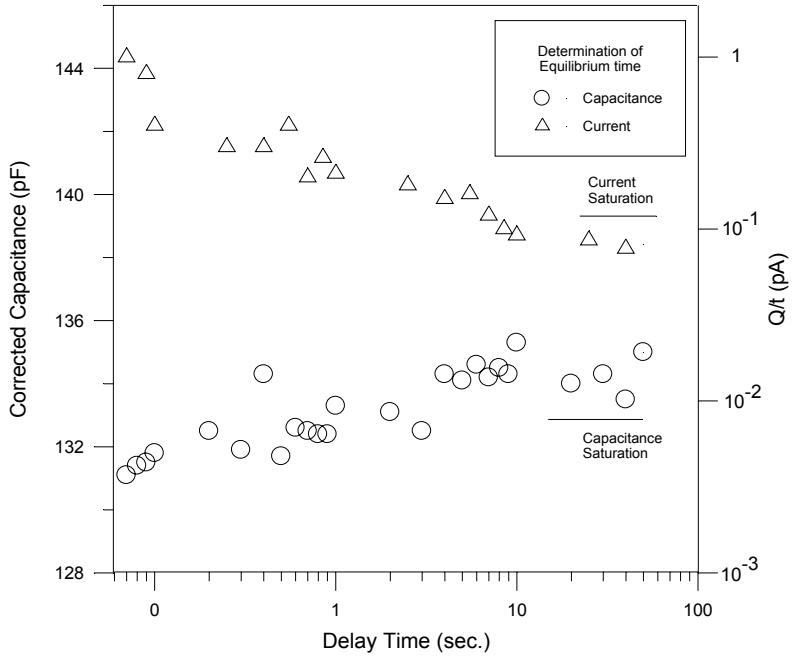


Fig. B-3. Recognizing Equilibrium using C and Q/t vs. Determination of delay (equilibrium) time on Cr/a-SiNx:H/p-Si MIS structure under inverting gate bias.

(b) High frequency C-V measurements

High frequency capacitance measurements have been obtained in a straight-forward manner, by use of either a 1 MHz capacitance meter (such as Boonton 7200 capacitance meter) or impedance analyzer (HP4192A) within 5 Hz-13 MHz of frequency interval. Though a frequency range 5 Hz-13 MHz has been declared for the impedance analyzer, a more reduced range (400Hz < f < 1 MHz) is applicable due to limitations of low excitation signal level and impedance matching problems.

(c) Intermediate frequency C-V Measurements

SR 830 lock-in amplifier has been used in the intermediate (1Hz-1kHz) frequency range for admittance analysis. In order to calibrate the amplifier output for

capacitance and conductance measurements, one needs standard high quality capacitors and conductors whose values should be around the values to be calibrated. In this work 100 and 600 pF Boonton standard capacitors were used for calibration of admittance versus gate bias via fully computer controlled LABVIEW program under different frequencies (in the range of Hz to kHz) for sample A-C and B, respectively.

As a final warning about admittance measurement as a function of both bias gate d.c voltage and its modulation frequency, one should keep in mind during the data analysis that a frequency scan was achieved by the impedance analyzer for frequencies > 5kHz under each constant dc gate voltage whereas a dc gate scan (50 mV/sec) was applied by the lock-in amplifier at each frequency < 5kHz.

B-2 Optical Probing

B-2-1 Infrared (IR) Analysis

The vibrational spectra of hydrogenated amorphous silicon alloys (a-SiCx:H and a-SiNx:H) by infrared (IR) spectroscopy has been undertaken. Moreover, the Fourier Transform version of this spectroscopy (Nicolet-FTIR), due to its rapidity and high sensitivity, is a powerful tool for investigating and testing of the plasma deposited silicon based amorphous materials. In that aim, a-SiCx:H film in p-i-n diode as active element for image sensor in one side, and a-SiNx:H for insulator and top passivating layer in MIS and TFT structures on the other side were investigated through FTIR analysis and results are given in fig.B.4

The spectrum of bonding structure of the a-SiNx:H film has been given in the figure B-4-a. Since, there is large amount of literature dealing with the concentrations and the frequencies of the various Si-H, N-H, and Si-N vibrations, the type of the films whether Si or N rich can easily be appreciated [40,132-138]. The dominant peak centered at 890 cm^{-1} in the spectrum shown in fig.B.4-a is due to the convolution of symmetric (920 cm^{-1}) and asymmetric (840 cm^{-1}) stretching vibrations of the Si-N. This peak is found in the literature at 860 cm^{-1} for the films

with low H content, and changes slightly to higher frequencies as H content increases [139]. The second peak at 1190 cm^{-1} is due to the bending vibrations of the N-H bonds which has the peak position at 1200 cm^{-1}, slightly shifted by the much stronger N-H peak. The type of hydrogen incorporation into the structure is generally obtained by comparing N-H and Si-H stretching peaks at 3350 cm^{-1} and 2150 cm^{-1}, respectively. Since these peaks are not in the mixed state, the peak height can be taken as proportional to the relevant bond density, and in this respect it is found that the N-H bond density is 9 times higher than that of the Si-H bond. Moreover, the frequency shift of the Si-H bonds from 2000 to 2150 cm^{-1} can be taken as a second argument for the N-rich film since the neighboring Si atoms are replaced with the more electronegative N atoms [136,137]. The N/Si ratio may be evaluated as around 1.4-1.5 in light of the relevant literature [138]. Furthermore, a very small NH_2 bending vibration peak at 1550 cm^{-1} also indicates that the H content of the films at hand is relatively high.

On the other hand, the IR spectrum of a-SiCx:H film at hand is given in fig (B-4-b). The striking feature of the spectrum may be outlined as follows: absorption bands of SiH_n (n=1 to 3) and CH_n (n=1 to 3) are easily distinguished [130]. The relative difference in the height of the peaks around 2100 cm^{-1} and 2900 cm^{-1}, attributed to the stretching modes of SiH_n and CH_n, respectively, shows that most of the H in the structure are bonded to C atoms [140-142]. This feature is also seen in the absorption band of 600-1300 cm^{-1} where the dominant peak position moves away from wagging mode of SiH vibrations (630 cm^{-1}) to higher frequencies at about 780 cm^{-1} which is attributed to wagging and stretching modes of $Si{-}CH_3$ structure [140,141]. Additionally, the absorption peak of wagging and rocking modes of CH_n (n=1 to 3) bonds around 1050 cm^{-1} is seen comparable to that of $Si{-}CH_3$ [141]. Thus, the deposited film seems carbon rich one, because the vibrational characteristic of the films are mainly dominated by CH_n bonds. On the other hand, the small shoulder seen around 3000 cm^{-1}, attributed to stretching modes of CH and

CH_2 σ-bonds of type sp^2, reveals the existence of a certain amount of sp^2 type σ-bonding together with the dominant sp^3 type [143-145]. As a result, IR spectrum supplies rapidly the hydrogen bonding configurations and especially confirms the presence of sp^2 planar graphitic islands throughout the film (discussed in chapter 2).

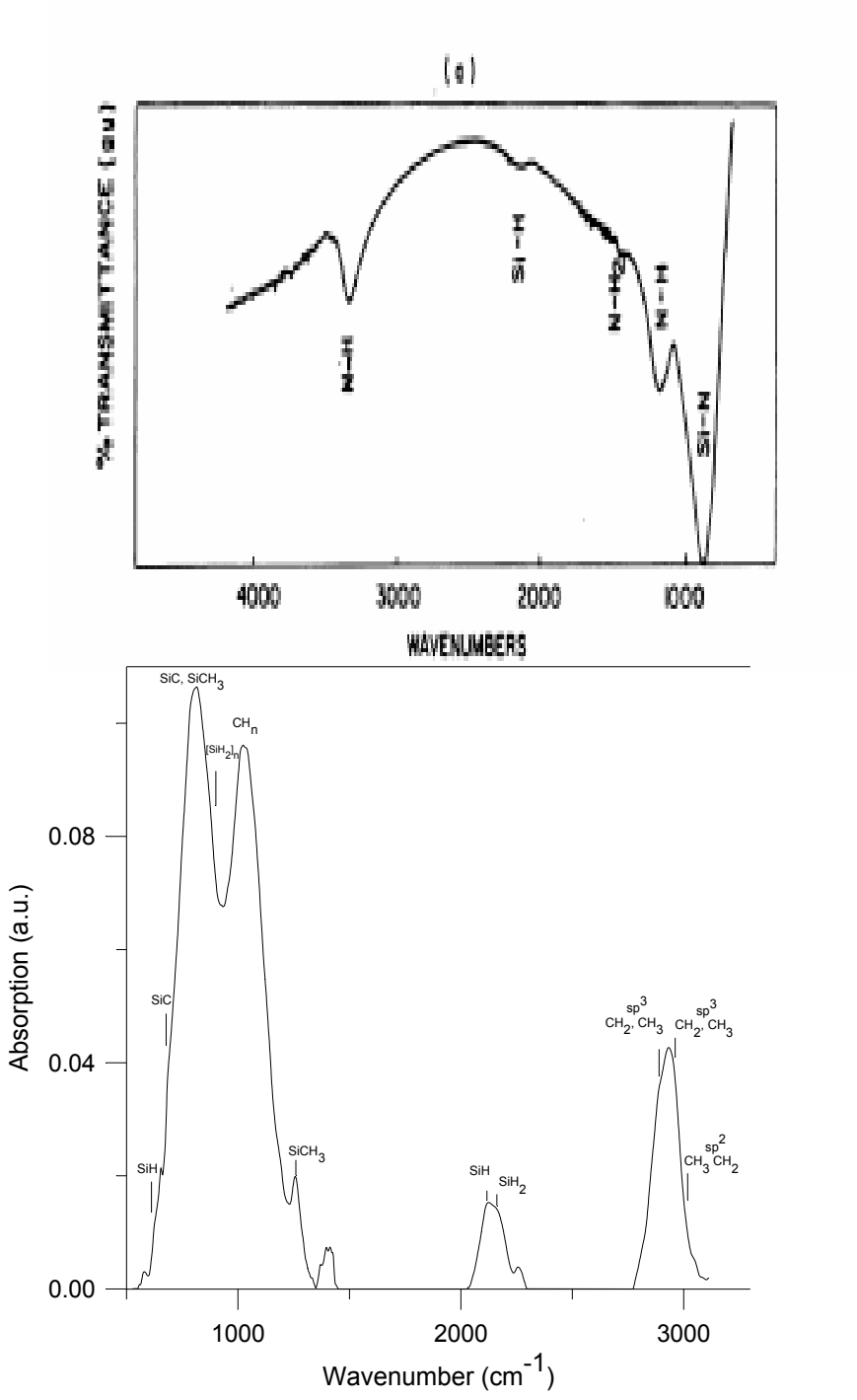
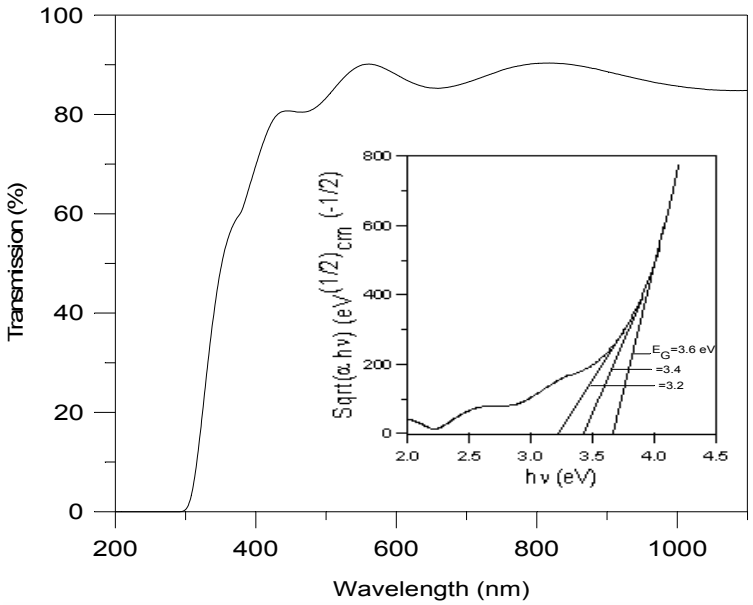


Fig. B.4 (a) FTIR spectrum of a-SiNx:H (a-SiCx:H) film grown on c-Si substrate (b).

B-2-2 UV-Visible Analysis

Optical properties of the films have been investigated within the wavelength range of 200-1100 nm by UV-Visible Spectrometer (Perkin Elmer λ2) with 2 nm slit width. The UV-Visible transmission of a-SiCx:H film is supplied in fig (B.5-a).

(a)



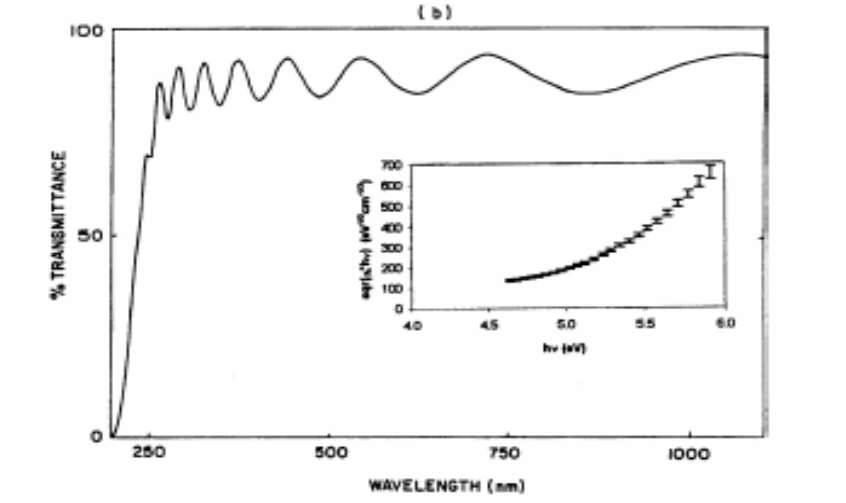


Fig.B-5 (a) UV- Visible transmission spectrum of a-SiCx:H (a-SiNx:H) film deposited on quartz substrate (b), the inset shows the Tauc's plot, without a clear linear region for a-SiCx:H.

The thickness, d_l and the refractive index, n_l, of the film were extracted from the transparent region of the transmission spectrum [146,147]; the results are checked by ellipsometry at 632.8 nm [148] (see table B.1).

Table B1. Evaluated optical constants of a-SiNx:H and a-SiCx:H (here x is estimated from E_{04} vs. x curve) [143-149,150]

Samples	E_G(Tauc) (eV)	E_{04} (eV)	d_l (nm)	n_l	X
A	3.2-3.6	3.45	450	1.78	0.7-0.8
B	2.50	-	120±10	2±0.1	≈0.5
C	5.03	-	600	1.88	1.4-1.5

The optical absorption coefficient α was derived from the strong absorption region of the transmission spectrum [146-148]; the optical gap, E_G (Tauc) was determined by using so called Tauc plot [151]. As depicted in the inset of fig (B.5-a), E_G (Tauc) could not be defined irrefutably, the Tauc plot remains slightly curved. This behavior might be interpreted as follows: In amorphous semiconductors, there are mainly 3 types of optical transitions: a) localized electronic state to localized state (LL), b) extended state to localized state (EL) or localized state to extended state (LE), c) extended state to extended state (EE, transitions over the mobility edges, i.e., conventional valence to conduction bands). The optical matrix elements for EE and EL (or LE) transitions are similar; but the LL transitions depend on whether or not the initial and final states are confined within the same regions (≡ large overlapping of their wave functions) or at distant regions (≡ zero or small overlapping). In a-Si films, the final and initial states are, in general, in different parts of the sample, leading to a very small LL matrix elements so LL transitions may be omitted and the optical absorption has EE and EL/LE character. However, in carbon rich a-SiCx:H films, the LL transitions are expected to be strongly probable since most of the initial and final states are lying on the same graphitic clusters (as described in chapter 2) and consequently an optical absorption up to about 10^4 cm^{-1} may be due to LL transitions alone [152,153] (the photon energy E_{04} corresponding to the absorption value of 10^4 cm^{-1} is often used to appreciate the optical gap for comparison of different a-SiCx:H films). As the analysis, given in chapter 2, assumes a distribution of cluster sizes, the observed spectral variation of the optical absorption coefficient,

α, might be a convolution of individual cluster absorption spectra of different gaps, depending on their sizes. Tauc plotting may be misleading within the frame of this analysis and then E_{04} value may be used as "symbolic" optical gap, allowing comparisons in literature. Consequently, UV-Visible analysis, apart from the thickness determination, has been successfully used for evaluating the carbon content of the film at hand through gap and refractive index values in comparison with these in the relevant literature. These information have been used in both the interpretation of the sample capacitance and the suggestion of irrefutable presence of π-like localized states in carbon rich a-SiCx:H film.

On the other side, a typical spectrum for a-SiNx:H film is shown in the figure B.5-b. The dependence of n on the wavelength, $\lambda_{h\nu}$ has also been investigated by a polynomial fitting of the form $n = 1.88 + \frac{1.1x10^4}{\lambda_{h\nu}^2}$, and then the values of n($\lambda_{h\nu}$) in the strong, and medium absorption region were obtained by extrapolation. Thus, absorption coefficients, α_o were calculated and then the mobility gap, E_g (5.03 eV) of the films were determined by using the Tauc plot, depicted in the inset of the figure B.5-b. This rather high value of E_g is another confirmation of N-rich feature of the a-SiNx:H films[135-137].

APPENDIX C

METASTABILITY PHENOMENA

H-Diffusion model

Nowadays, there is a consensus that the density of Si DB states is determined by a chemical equilibrium process due to the intercoversion of WBs and DBs:

$$SiSi \leftrightarrow 2DB \qquad (C.1)$$

To be consistent with ESR experiment (spin active or isolated neutral DBs are necessary), this pair of DB defects should be able to move away from each other. However, the eventual motion (or diffusion) of these DB defects at relatively low temperature seems non-probable. Consequently, the experimentally observed equilibration microscopic process requires a mobile species [strecthed exponential $e^{-(t/\tau)^{\beta}}$ type equilibration kinetics require a species, possessing a dispersive diffusion across the material at relatively low temperature. Diffusion of the species is executed as a continuous time random walk (CTRW) composed of alternating steps and pauses as in analogy with the dispersive transport of charge carriers across tail states; the release time from deeper traps is longer, equilibration becomes slower at longer times (see fig.C.1).

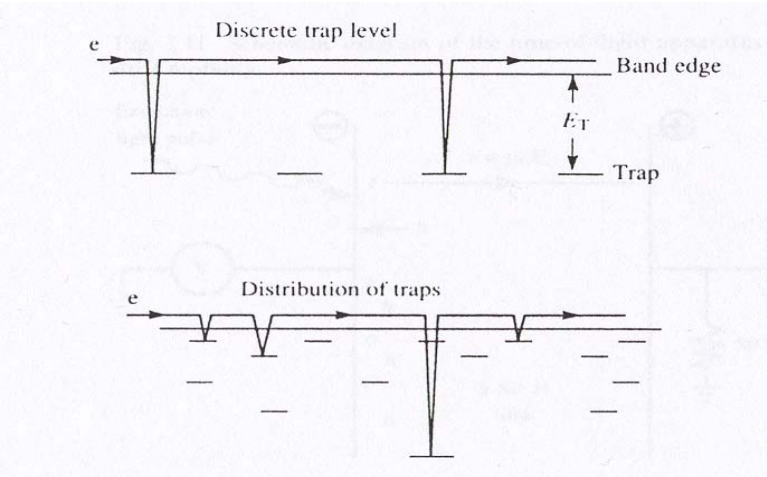


Fig.C.1 Illustration of trap-limited transport of carriers for a discrete or distributed trap levels.

In other words, the pausing time has a power law time dependence. In this respect, the hydrogen atom (which is dispersively mobile in a-Si:H) might be the required mobile species. Since hydrogen provides a mechanism for the creation and annealing of defects in a-Si:H, the removal rate of these defects can be assumed to be governed by H-diffusion. As to the extended Glarum model [154], the rate of defect formation is proportional to the rate of hydrogen diffusion towards the defect formation sites. Consequently, it can be inferred that the rate of defect removal is linked by the same mechanism. Therefore, the change of defect density from equilibrium N_T can be expressed as

$$\frac{d}{dt}\left(N_T\right) = -AD(t)N_T \qquad \text{(C.2)}$$

where A is constant and D(t) is the time dependent dispersive hydrogen diffusion coefficient. The theory of multiple trapping and trap limited transport in traps of exponentially distributed distribution of trap energies ($e^{\frac{E}{kT_0}}$ with the characteristic temperature T_0, determined by the degree of disorder) predicts a dispersive diffusion coefficient, given by [12]

$$D(t) = D_{00}(\upsilon t)^{-\gamma} \qquad \text{(C.3)}$$

where D_{00} is the diffusion constant and υ is the hydrogen attempt to escape frequency, γ is the temperature dependent dispersion parameter: $\gamma = 1-\beta = 1-\frac{T}{T_0}$. Substituting the relation (C.3) into (C.2) and integrating yields

$$\Delta N_T = \Delta N_{T0}\exp\left[-(t/\tau)^{\beta}\right] \qquad \text{(C.4)}$$

with $\tau = \upsilon^{-1}\exp\left(\frac{E_T}{kT}\right)$, $E_T = kT_0\ln\left(\frac{\beta\upsilon}{AD_{00}}\right)$

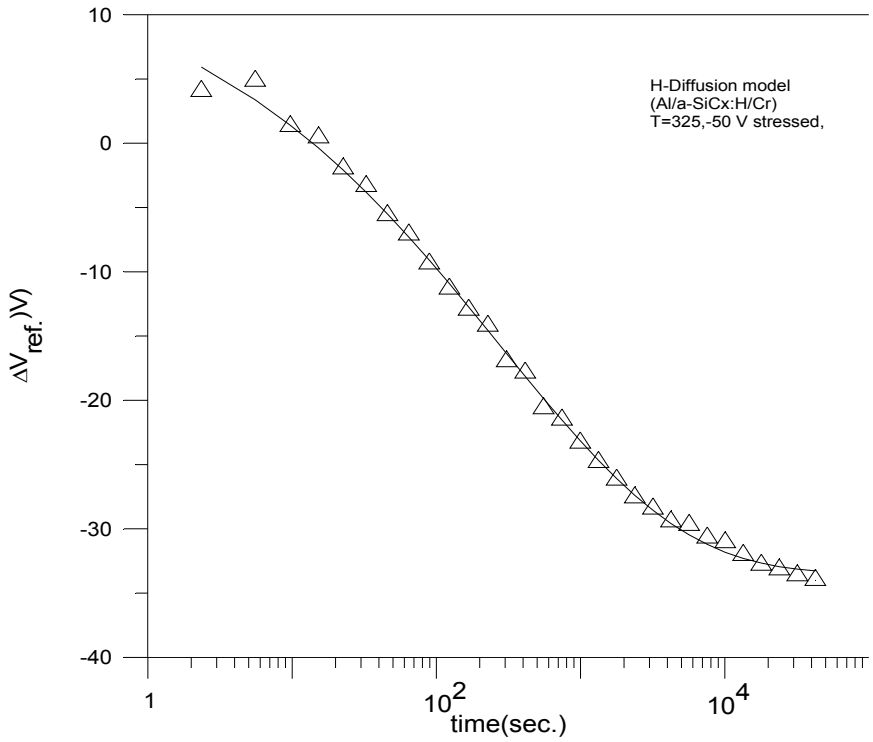


Fig.C.2 Reference voltage shift versus time at T=325 K. Data are represented by Δ symbol, solid line is fit result to the H-diffusion model, given in the relation (6.2).

APPENDIX D

TRANSPORT ANALYSIS IN AMORPHOUS SEMICONDUCTOR

In the following section, in a-Si:H, the most important transport mechanisim (namely extended states conduction) and the hopping conduction will be discussed and by the analogy, the discussion will be extended into a-SiCx:H and a-SiNx:H films, and the resultes were given in the body of text.

D-1 Electrical Transport :

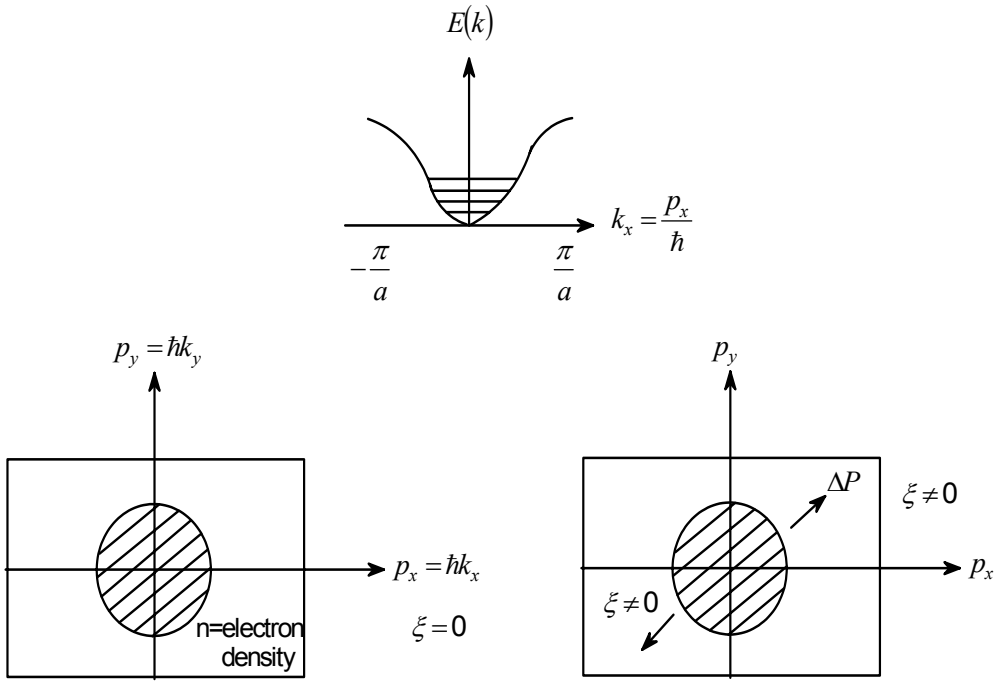


Fig.D-1. Schematic illustration of number of states in Brillion zone. Note that around brillion zone, E(k) is parabolic whereas for 2 dimension, it is circle. Application of external field leads to displace all states by equal amount ΔP.

In the absence of an external electric field, he electron “gas” in a semiconductor is in a of equilibrium and obeys the Fermi-Dirac equilibrium

distribution function: $f(E)=\dfrac{1}{1+\exp\left[\left(\dfrac{E-E_F}{kT}\right)\right]}$ with $E=\dfrac{\hbar^2k_x^2}{2m^*}=\dfrac{p_x^2}{2m^*}=\dfrac{m^*V_x^2}{2}$.

Hence, $f(E)=\dfrac{1}{1+\exp\left[\left(\dfrac{m^*V_x^2}{2kT}\right)\right]\exp\left(\dfrac{-E_F}{kT}\right)}$. Fermi distribution (f) is symmetrical with respect to the sign of velocity: $f(-V_x)=f(V_x)$. Therefore, the average velocity o an electron in any direction is zero (i.e., current is zero). Under external electric field, total quasi momentum P_Σ:

$$P_\Sigma=\sum_{i=1}^{n}P_i(t)=\sum_{i=1}^{n}P_i(0)+nq\xi\tau \qquad \text{(D-1)}$$

Electron velocity corresponding to the state P_i is as:

$v_i=\dfrac{dE}{dp_i}=\dfrac{p_i}{m^*}$ (= the equilibrium distribution changes). For an homogeneous crystal and in the absence of a temperature gradient, the external electric field ξ leads to the variation of f: $\dfrac{\partial f}{\partial t}=\left(\dfrac{\partial f}{\partial t}\right)_\xi+\left(\dfrac{\partial f}{\partial t}\right)_{collision}$ where the last term expresses the change in the distribution f of the carriers due to the collisions by impurities and lattice vibrations(≡ phonons). Note that when electric field, after application, is removed (ξ =0) leads to $\left(\dfrac{\partial f}{\partial t}\right)_\xi=0$ and $\dfrac{\partial f}{\partial t}=\left(\dfrac{\partial f}{\partial t}\right)_{collision}$. This means that carriers (electrons) will return to the equilibrium (where f=f_0 due to scattering with phonons and impurities (this process is called *relaxation*). The simplest process may be as follows: $\dfrac{\partial f}{\partial t}\propto f-f_0$ with constant of proportionality $1/\tau$. Hence, $\dfrac{\partial f}{\partial t}=-\dfrac{f-f_0}{\tau}$, $f-f_0=(\Delta f)_0\exp(-t/\tau)$. At steady state (or stationary state) under electric fields (ξ ≠0) leads to $\dfrac{\partial f}{\partial t}=0$. Therefore,

$$\left(\frac{\partial f}{\partial t}\right)_\xi=-\left(\frac{\partial f}{\partial t}\right)_{collision} \qquad \text{(D-2)}$$

with $\left(\frac{\partial f}{\partial t}\right)_\xi = \frac{\partial f_0}{\partial P_x}\frac{\partial P_x}{\partial t}$ where $\frac{\partial P_x}{\partial t} = F_x = -e\xi$ and $\frac{\partial f_0}{\partial P_x} = \frac{\partial f_0}{\partial E}\frac{\partial E}{\partial P_x}$ with $\frac{\partial E}{\partial P_x} = v_x = \frac{p_x}{m^*}$ as $E = \frac{p_x^2}{2m^*} = \frac{\hbar^2 k^2}{2m^*}$. As a result, $\left(\frac{\partial f}{\partial t}\right)_\xi = -q\xi v_x \frac{\partial f}{\partial E}$. Rearranging relation (D-2) yields

$$f = f_0 - q\tau\xi v_x \frac{df_0}{dE} \quad \text{(= Boltzman's kinetic equation)} \quad \text{(D-3)}$$

In a crystal of unit volume, in the elementary quasi momentum volume $d\Gamma_k$, the density dn of charge carriers is as: $dn = f\frac{d\Gamma_k}{4\pi^3}$. Hence, the elementary current density dJ_x along the field direction x around the state k is as:

$dJ_x = qv_x dn = qv_x f\frac{d\Gamma_k}{8\pi^3}$. So, $J_x = \frac{q}{8\pi^3}\int\limits_{(\text{all k values})} v_x\left(f_0 - qv_x\tau\xi\frac{df_0}{dE}\right)d\Gamma_k$,

$= \underbrace{\frac{q}{8\pi^3}\int\limits_{(\text{all k values})} v_x f_0 d\Gamma_k}_{\text{equilibrium case} = 0} - \frac{q^2\xi}{8\pi^3}\int\limits_{(\text{all k values})} v_x^2\frac{\partial f}{\partial E}\tau(k)d\Gamma_k$. Instead, transitions occur only between overlapping sites in real space. In the light of discussion above, the disorder reduces the carrier mobility due to the frequent scatterings ($\mu \approx 1000$ $cm^2/V.sec.$ in crystal Si whereas for a-Si, this is around 2-5 $cm^2/V.sec.$).

D-2 Electronic Transport :

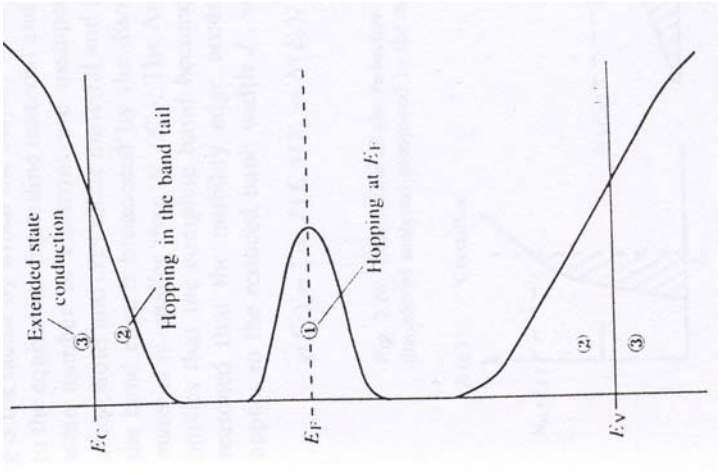


Fig. D-2. Representation of the three main conduction paths in amorphous semiconductors.

In light of previous analyses, at least two different electrical conduction mechanism exist in amorphous structure:

A) Extended state conduction $(\mu \neq 0)$

B) Localized state conduction $(\mu = 0)$

Among localized states, the band tail (B_1) and deep dangling bond defect states (B_2) might behave differently following the position of Fermi level E_F. Moreover, the conduction (or mobility) around E_c (= mobility edge) might be much more complex than a simple abrupt mobility edge passage.

A) **Extended state conduction**

Consider the current density relation: $\vec{J}_x = -q^2 \vec{\xi} \int_{(v_k)} v_x^2 \frac{\partial f_0}{\partial E} \tau(k) \frac{d\Gamma_k}{8\pi^3} \equiv \sigma \vec{\xi}$ with $\sigma = -q^2 \int_{(v_k)} v_x^2 \frac{\partial f_0}{\partial E} \tau(k) \frac{d\Gamma_k}{8\pi^3}$ where $v_x = \sqrt{kT/m}$, $\frac{\partial f_0}{\partial E} = -f_0(1-f_0)/kT \approx \frac{-f_0}{kT}$ and $\frac{d\Gamma_k}{8\pi^3} = N(E)dE$. Substituting the relations, conductivity expression turns out to be $\sigma \approx q \int N(E)\mu(E) f_0 dE$ with $\mu(E) = q\tau(E)/m$ and $f_0 \approx e^{-\frac{(E-E_F)}{kT}}$. Rearranging the relation leads to $\sigma = \frac{1}{kT} \int \sigma(E) e^{-\frac{(E-E_F)}{kT}} dE$ with $\sigma(E) = qN(E)\mu(E)kT$ .3 factors determine the dominant conduction path along the E-axis. Two cases may be considered as:

$\sigma(E)$ increases monotonically with E

$\sigma(E)$ increases abruptly at E=E_c.

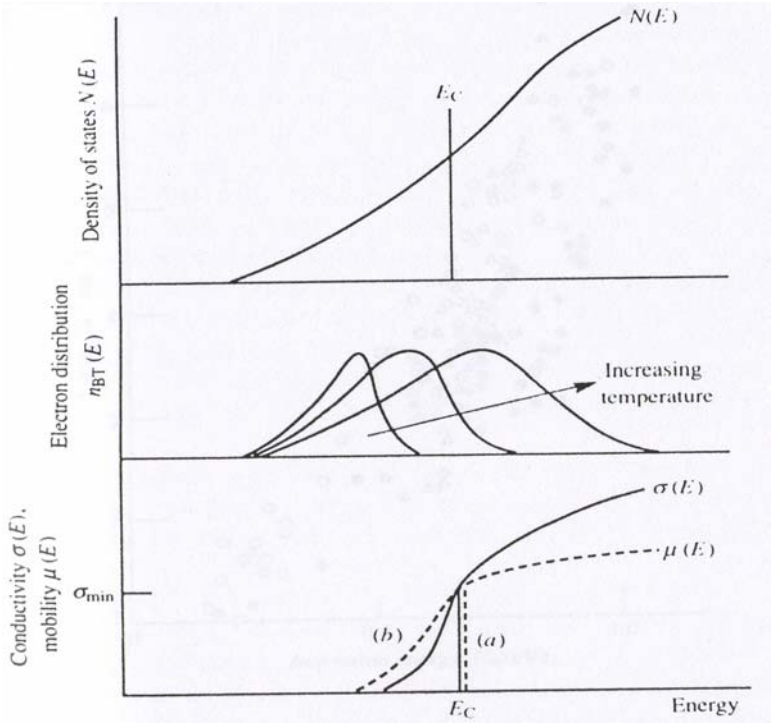


Fig.D-3. Illustration of the density of states at the band edge, together with the electron distribution $n_{BT}(E)$, the conductivity σ(E) and mobility μ(E): σ(E) and μ(E) may change abruptly (a), or gradually (b) at the mobility edge E_c.

This last case leads to

$$\sigma = \frac{1}{kT}\int_{E_c}^{\infty}\sigma(E)\exp\left[-\frac{E-E_F}{kT}\right]dE = \sigma_{\min}\exp\left[-\frac{E_c-E_F}{kT}\right] \quad \text{with} \quad \sigma_{\min} = N(E_c)q\mu_0 kT$$

where μ_0 is the mobility at $E=E_c$. Nowadays, there is a considerable doubt about the sharpness or even the existence of a mobility edge. Nevertheless in the conductivity result analyses, $\sigma = \sigma_{\min}\exp\left[-\frac{E_c-E_F}{kT}\right]$ is used even if $\sigma(E)$ does not change abruptly at E_c (but it might increase rapidly within a limited energy range around E_c). Keep in mind that, as always σ is an average of $\sigma(E)$ over an energy range of at least kT, the sharpness can be observed at very low T; but in practice E_F in a-Si:H can not be brought closer than about 0.1 eV to E_c such that σ can hardly be measured below 100 K. Consequently, there exist limited information about the sharpness f the mobility edge (on the contrary of metals).

In practice, there are 4 techniques for experimentally measuring dc electronic transport: a) dc conductivity, b) drift mobility, c) thermo-power, d) Hall effect. Here let us consider dc conductivity.

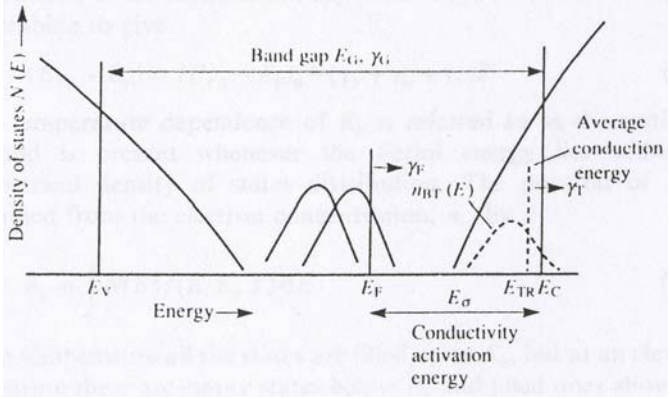


Fig.D-4. Schematic illustration of the density of states distribution as a function of conductivity activation energy, E_a, the average conduction energy, E_{TR}, with respect to the mobility edges, and the Fermi energy. Also, in the figure, temperature dependent parameters (γ_F, γ_G and γ_T) are indicated.

Dc Conductivity:

Dc conductivity is thermally activated (at least over a given temperature range): $\sigma(T) = \sigma_0 e^{-\frac{E_\sigma}{kT}}$ where σ_0 is prefactor, $E_\sigma (= E_{TR} - E_F)$ is activation energy.

For a conductivity throughout the extended states, E_{TR} coincides with E_c, further(?) mechanism (such as band tail hopping) are possible where $E_{TR} \neq E_c$. Note that $Log\sigma$ vs. 1/T could not give σ_0 and E_σ directly, since σ_0 has found different for different samples, arising a discussion on σ_0. E_σ is temperature dependent due to the temperature dependence of: i) E_F (statistical shift due to the asymmetric DOS distribution), ii) E_G (gap states move with respect to each other when T changes, iii) E_{TR} (=average conduction energy) obviously T affects E_{TR}

If linear temperature variation of slope γ_F, γ_G and γ_T are assumed respectively, then $E_\sigma \equiv (E_{TR} - E_F)_T = \underbrace{(E_{TR} - E_F)_0}_{E_{\sigma 0}} - (\gamma_F + \gamma_G + \gamma_T)T$. Conductivity expression appear as $\sigma(T) = \sigma_0 e^{\frac{\gamma}{k}} \exp\left[-\frac{E_{\sigma 0}}{kT}\right]$

B Localized State Transport

Although there is no macroscopic conduction throughout localized states at T=0 K, at higher temperature, quantum mechanical tunneling transitions between localized states, might lead to conduction.

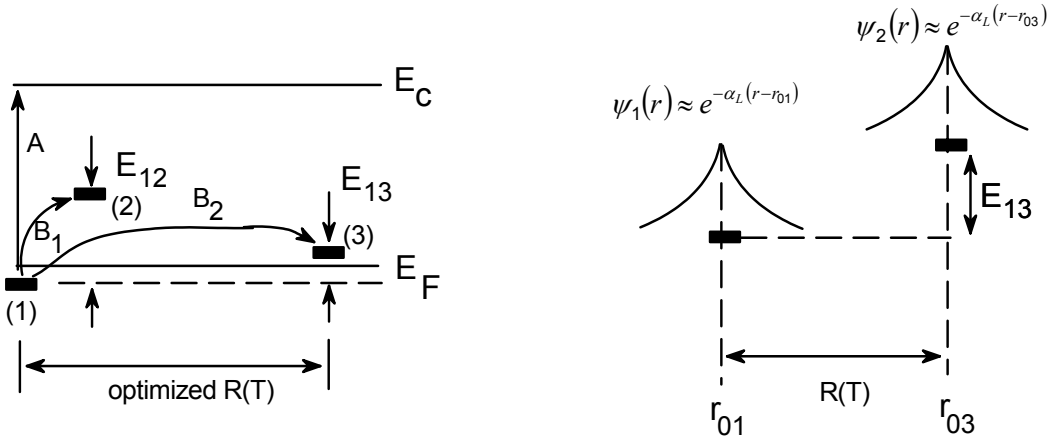


Fig.D.5 Illustration of tunneling transitions between localized states.

The probability P_{ij} that an electron will jump from the state (i) to the state (j) is determined by the following 3 factors:

1 the probability of finding a phonon with excitation equal to E_{ij}, given by Boltzmann factor $\exp\left(-\frac{E_{ij}}{kT}\right)$

2 the attempt to escape frequency ω_0 which cannot be greater than the maximum phonon frequency (in the range 10^{12}-10^{13} sec^{-1}.)

3 the probability of electron transfer from one state (i) to another (j). This factor depends on the overlapping of the wavefunctions and should be given by $e^{-2\alpha_L R}$:

$$P_{ij} = \omega_0 \exp\left[-2\alpha_L R - \frac{E_{ij}}{kT}\right]$$ with α_L^{-1} = localization length= $\left[\frac{\hbar^2}{2m(E-E_c)}\right]^{1/2}$

Analogy with the motion of particles in a gas, diffusion coefficient D in crystals may be expressed by the formula of the kinetic theory of gases: $D = \frac{1}{3}\bar{\nu}\bar{\lambda} = \frac{1}{3}\frac{\bar{\lambda}^2}{\tau}$ where $\bar{\lambda}$ is the mean free path in the gas phase, τ is time interval between collisions, $\bar{\nu}\left(=\bar{\lambda}/\tau\right)$ is average velocity. Instead of mean value of $\bar{\lambda}$, mean square values should be calculated: $e^{-\frac{x}{\lambda}}$ = probability of particle traversing the distance x without suffering any collisions is given $\left\langle x^2 \right\rangle = \frac{\int_0^\infty x^2 e^{-\frac{x}{\lambda}} dx}{\int_0^\infty e^{-\frac{x}{\lambda}} dx} = 2\lambda^2$. Hence, $D = \frac{\lambda^2}{3\tau} = \frac{\left\langle x^2 \right\rangle}{6\tau} = \frac{R^2}{6} P_{ij}$. Einstein relation $\mu = \frac{eD}{kT} = \frac{eR^2 P_{ij}}{6kT}$. Note that for transition probability from (i) to (j), the state (i) should be occupied (f_i) and the state (j) should be empty ($1-f_j$). For maximum transfer, the product f_i ($1-f_i$) should be maximum. Therefore, hopping should occur around Fermi level.

$$\sigma = qN\left(E_F\right)\mu = \frac{q^2R^2N\left(E_F\right)}{6kT}P_{ij} = \frac{q^2R^2N\left(E_F\right)}{6kT}\omega_0 \exp\left[-2\alpha_L - \frac{E_{ij}}{kT}\right]$$

As temperature decreases, the number and the energy of phonons decreases and then the more energetic phonon-assisted hopping will progressively become less favorable. As a result, carriers will tend to hop to larger distances in order to find sites which lie energetically closer than the nearest neighbor; this mechanism us the so-called variable range hopping. In order to find the most favorable hopping distance the exponent of $\exp\left[-2\alpha_L - \frac{E_{ij}}{kT}\right]$ should be minimized. For this purpose, let us express E_{ij} within a distance R from a particular site is given by: $\frac{4\pi R^3}{3}N\left(E_F\right)E_{ij}$. The electron can leave its site only if the number of accessible sites is at least one. Taking this into account, one gets for the average energy spacing between states near E_F level: $E_{ij} = \frac{3}{4\pi N\left(E_F\right)R^3}$. Inserting into transition rate equation: $P_{ij} = \omega_0 \exp\left[-2\alpha_L R - \frac{3}{4\pi N\left(E_F\right)kTR^3}\right]$.

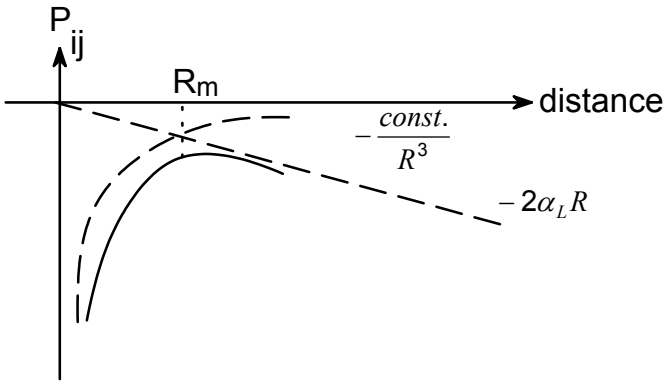


Fig.D.6 Illustration of the probability P_{ij} (that an electron will jump from state (i) to (j)) as a function of distance.

Minimizing the exponent term with respect to R, the maximum hopping distance can be evaluated: $R_m = \left[\frac{9}{8\pi\alpha_L N(E_F)kT}\right]^{1/4}$. Then, the transition rate would be: $P_{ij} = \omega_0 \exp\left[-\frac{A}{T^{1/4}}\right]$ with $A = 2\left[\frac{32\alpha_L^3}{9\pi k N(E_F)}\right]$. Finally, conduction expression turns into : $\sigma = \frac{q^2 R_m^2 \omega_0 N(E_F)}{6kT}\exp\left[-\frac{A}{T^{1/4}}\right] = \sigma_0(T)\exp\left[-\frac{A}{T^{1/4}}\right]$

APPENDIX E

FABRICATION AND CHARACTERIZATION OF TFT

E-1 Introduction

Thin film transistor, deposited on hydrogenated amorphous silicon (a-Si:H), has widespread application in technology as well as research tool. Because in TFT's the Fermi level in the amorphous silicon can be controlled at will, they can be used as powerful tool to investigate various material properties, including density of states distribution, photoconductivity, mobility and stability. Moreover, interest in a-Si:H TFTs receives commercial impetus due to the application in liquid crystal displays, image sensors and printer arrays. In addition, due to the similarity and striking differecenses of c-Si device physics in some extent, a-Si:H based devices might yield fruitfull contiribution.

Typical inverted staggered TFT structure is given in fig.E-1, where source and drain contacts are deposited onto a-Si:H film, and bottom gate electrode is the beneath of PECVD grown a-SiNx:H film.

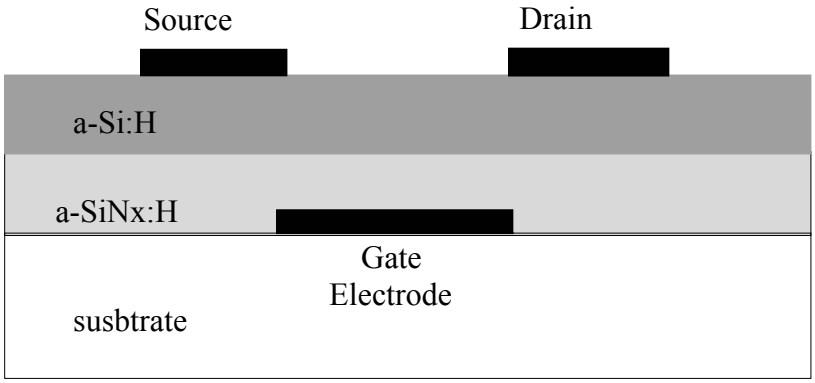


Fig.E-1. Inverted staggered TFT structure.

E-2 Production of TFT:

In this work, as stated above, inverted staggered type TFT is produced. Before depositing a-SiNx:H and a-Si:H fims, substrates were cleaned via RCA cleaning procedure and then Cr metal was evaporated on the glass substrate. This metal layer was patterned by defining a photoresit pattern on the metal layer and etching away the metal outside the photoresit regions. The samples were then introduced into the PECVD reactor and then the gate insulator silicon nitride, the active layer a-si:H were deposited consecutively in the PECVD reactor under continuous vacuum conditions. The samples were then taken out of the reactor and metal layers was evaporated onto a-Si:H film and patterned by means of photolithograpy (as Source and Drain electrodes). Production stages was given in the flowchart (see fig. E-2)

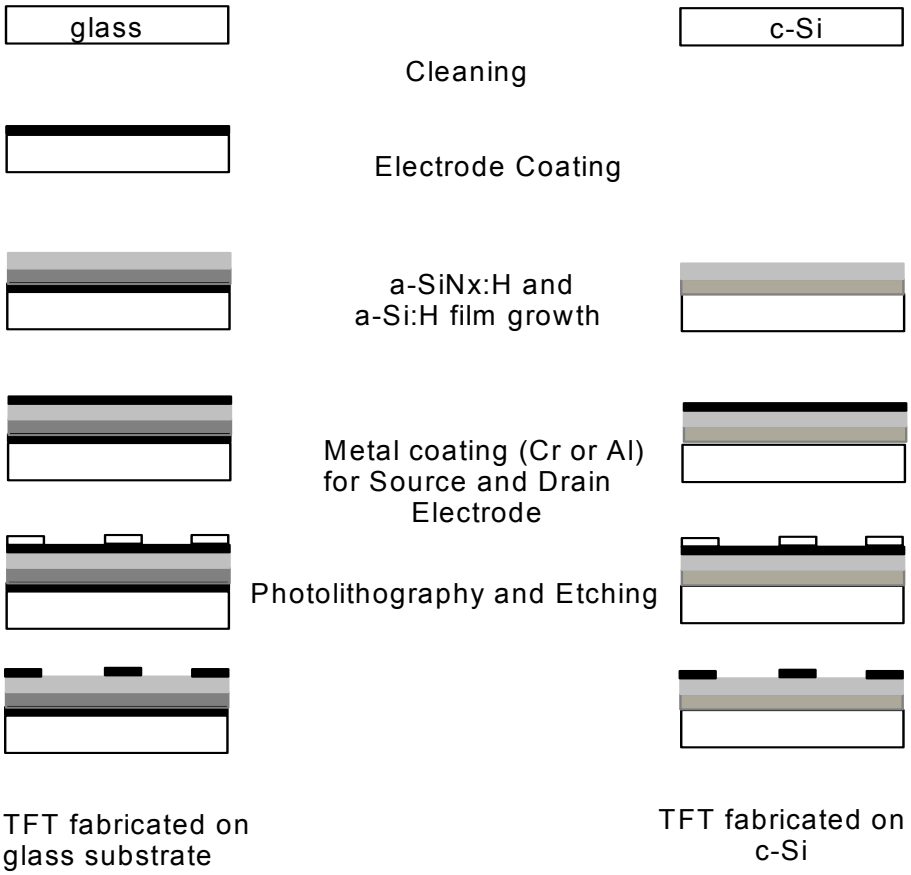


Fig.E-2 Production stages of TFT

One should keep in mind that while patterning Source and Drain electrodes of TFT via photolithograpy, first metal coated substrates were coated with PR by spreading around 3500 RPM, then baked at 65°C at 25 min to enhance the photo-sensitivity, later patterned via Pattern Generator, finally the illuminated part was removed in a suitable developer (=etched).

E-3 :Characterization of TFT

Typical current voltage relations of the produced TFT was given in Fig.E-3. The ON/OFF ratio (10^4) of the TFT was given in Fig.E-3-a and channel conductivity as a function of gate bias was given in fig.E-3 c. Due to the lack of saturated current regions, mobility of charge carriers was determined via the slope of current voltage relation and found as 0.4 cmVsec.$^{-2}$. It seems that it was low than demanded but suitable value once compared with the literature.

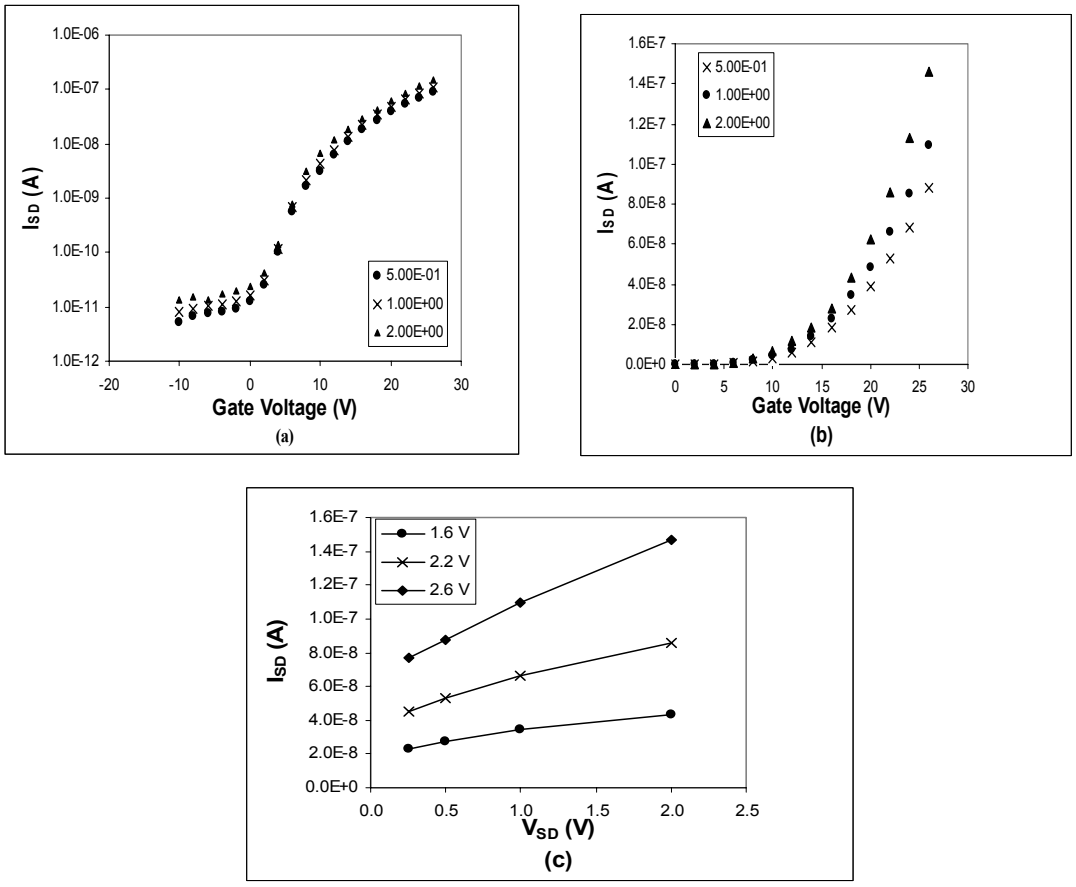


Fig.E-3 Current-Voltage relation of TFT.

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VITA

The author of this work was born in Ordu at 1973. He has received his B.Sc. and M. Sc. Degrees in physics at 1996 and 1998, both at Middle East Technical University (METU), Ankara. Since 1996, he has been employed as a research assistant by the Department of Physics at METU.

The author has interest in a number of areas including silicon technology (both crystalline and amorphous cases), thin films. His publication include:

- Orhan Özdemir, İsmail Atılgan and Bayram Katırcıoğlu," Admittance Analysis of an MIS structure made with PECVD deposited a-SiNx:H thin films", J. Non-Cryst. Solids, 249, pp. 131-144, 1999.
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