INVESTIGATION OF InSe THIN FILM BASED DEVICES

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ABSTRACT

INVESTIGATION OF InSe THIN FILM BASED DEVICES

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In this study, InSe and CdS thin films were deposited by thermal evaporation method onto glass substrates. Schottky and heterojunction devices were fabricated by deposition of InSe and CdS thin films onto SnO_2 coated glass substrates with various top metal contacts such as Ag, Au, In, Al and C. The structural, electrical and optical properties of the films were investigated prior to characterization of the fabricated devices.

The structural properties of the deposited InSe and CdS thin films were examined through SEM and EDXA analysis. XRD and electrical measurements have indicated that undoped InSe thin films deposited on cold substrates were amorphous with p-type conductivity lying in the range of 10^{-4}-10^{-5} $(\Omega.cm)^{-1}$ at room temperature. Cd doping and post-depositional annealing effect on the samples were investigated and it was observed that annealing at 100 ^{o}C did not show any significant effect on the film properties, whereas the conductivity of the samples increased as the Cd content increases. Temperature dependent I-V and Hall effect measurements have shown that conductivity and carrier concentration increases with increasing absolute

temperature while mobility is almost temperature independent in the studied temperature range of 100-430 K.

The structural and electrical analysis on the as-grown CdS thin films have shown that the films were polycrystalline with n-type conductivity. Temperature dependent conductivity and Hall effect measurements have indicated that conductivity, mobility and carrier concentrations increases with increasing temperature. Transmission measurements on the as-grown InSe and CdS films revealed optical band gaps around 1.74 and 2.36 eV, respectively.

Schottky diode structures in the form of TO/p-InSe/Metal were fabricated with a contact area of around $8x10^{-3}$ cm^2 and characterized. The best rectifying devices obtained with Ag contacts while diodes with Au contacts have shown slight rectification. The ideality factor and barrier height of the best rectifying structure were determined to be 2.0 and 0.7 eV, respectively. Illuminated I-V measurements revealed open-circuit voltages around 300 mV with short circuit current $3.2x10^{-7}$ A. High series resistance effect was observed for the structure which was found to be around 588 Ω. Validity of SCLC mechanism for Schottky structures was also investigated and it was found that the mechanism was related with the bulk of InSe itself.

Heterostructures were obtained in the form of TO/n-CdS/p-InSe/Metal and the devices with Au and C contacts have shown the best photovoltaic response with open circuit voltage around 400 mV and short circuit current $4.9x10^{-8}$ A. The ideality factor of the cells was found to be around 2.5. High series resistance effect was also observed for the heterojunction devices and the fill factors were determined to be around 0.4 which explains low efficiencies observed for the devices.

Keywords: InSe, CdS, Thermal Evaporation, Thin Film, Schottky Diode, Heterojunction.

ÖZ

InSe INCE FILM TABANLI AYGITLARIN INCELENMESI

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Bu çalismada, InSe ve CdS ince filmler isisal buharlastirma yöntemi ile cam tabanlar üzerine büyütülmüstür. Schottky ve çoklueklem aygitlari, InSe ve CdS filmlerin kalay-oksit kaplanmis cam üzerine büyütülmesi ve çesitli metallerin (altin, gümüs, indiyum, aliminyum ve karbon) üst kontak olarak kullanilmasiyla üretildi. Ince filmlerin yapisal, elektriksel ve optik özelliklerinin incelenmesinden sonra Schottky ve çoklueklem aygitlar karakterize edildi.

Üretilmis filmlerin yapisal özellikleri taramali elektron mikroskopisi ve enerji dagilimli X-isinlari analizi yöntemleri ile incelendi. X-isinlari kirinimi analizi ve elektriksel ölçümler soguk taban üzerine büyütülmüs InSe filmlerin p-tipi ve amorf (düzensiz) yapida olduklarini gösterdi. Oda sicakliginda p-tipi filmlerin iletkenliklerinin 10^{-4}-10^{-5} $(\Omega.cm)^{-1}$ civarinda oldugu gözlendi.

Kadmiyum katki ve üretim sonrasi tavlama etkileri arastirildi ve 100 ^{o}C de tavlanmis filmlerin yapilarinda ve elektriksel parametrelerinde önemli degisiklikler gözlenmedi. Diger yandan, kadmiyum katkisi arttikça filmlerin iletkenliklerinin arttigi bulundu.

Sicaklik bagimli akim-voltaj ve Hall etkisi ölçümleri 100-430 K sicaklik bölgesinde yapildi ve tasiyici yogunlugu ile iletkenligin sicaklikla arttigi tespit edildi. Buna ragmen, mobilite ayni sicaklik araliginda hemen hemen sicakliktan bagimsiz bir davranis gösterdi.

CdS ince filmlerin yapisal ve elektriksel incelemeleri sonucu, filmlerin çoklu-kristal yapida ve n-tipi olduklari tespit edildi. Sicaklik bagimli iletkenlik ve Hall etkisi ölçümlerinden iletkenlik, tasiyici yogunlugu ve mobilitenin sicaklikla arttigi bulundu. Optik geçirgenlik ölçümlerinden, InSe ve CdS ince filmlerin optik band araliklari, sirasiyla 1.74 ve 2.36 eV civarinda bulundu.

TO/p-InSe/Metal formundaki Schottky yapilari çesitli üst metal kontaklarla, kontak alani yaklasik olarak $8x10^{-3}$ cm^2 olacak sekilde üretildi ve karakterize edildi. Incelenen yapilar içinde en iyi dogrultucu yapi gümüs kontakla elde edilirken, altin kontakli diyot da çok az dogrultma gösterdi. Diyotlarin idealite faktörü ve bariyer yükseklikleri sirasiyla 2 ve 0.7 eV civarinda bulundu. Örneklerin isik altinda ki ölçümleri 300 mV civarinda açik devre voltaji ve $3.2x10^{-7}$ A kisa devre akimi verdi. Schottky aygitlarinda 588 Ω'luk yüksek seri direnç etkisi gözlendi. Sinirli bosluk yükü akim mekanizmasinin Schottky yapilardaki geçerliligi arastirildi ve bu mekanizmanin, dogrudan InSe (bulk)'a bagli oldugu tespit edildi.

Çoklueklem günes pili yapilari TO/n-CdS/p-InSe/Metal formunda elde edildi. En iyi foto-voltaj tepkisinin altin ve karbon metal kontaklarla elde edildigi anlasildi. Açik devre voltaji ve kisa devre akimlari sirasiyla 400 mV ve $4.9x10^{-8}$ A civarinda bulundu. Çoklueklem aygitlarin idealite faktorleri 2.5 yakinlarinda gözlendi. Yüksek seri direnç etkisi çoklueklem aygitlar için de gözlendi ve FF (doluluk faktörü) 0.4 civarinda hesaplandi ki, bu da düsük verimliligin bir nedeniydi.

Anahtar Kelimeler: InSe, CdS, Isisal Buharlastirma, Ince Film, Schottky Diyot, Çoklueklem.

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In Memory of My Grandparents …

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CHAPTER 1

INTRODUCTION

Growing energy needs of today's world force the researchers to look for alternative energy sources other than traditional energy forms. Furthermore, energy sources like natural gas, petroleum and nuclear reactors concern the scientists as regards the high level of pollution to the environment. Therefore, especially in the last decade, researchers have focused on the development of renewable sources of energy forms by which the pollution of the environment is minimized. Among the alternative energy forms, solar energy seems to be a promising one because it is cheap, clean and unlimited in comparison with the energy needs of the world. The solar energy may be converted to other forms through several methods, such as photothermal, photochemical, photoelectrochemical, photobiochemical and photovoltaic. Among these methods, the cleanest and most efficient way of solar energy conversion to electrical power is the photovoltaic (PV) or solar cell devices. A solar cell consists of a potential barrier within a semiconductor material which is capable of separating the electrons and holes that are generated by the absorption of light within the semiconductor. Photovoltaic cells for conversion of solar energy into electrical power can be found in two main forms: large area and thin film solar cells. Thin film forms of photovoltaic devices have advantageous over large area cells by using small amounts of material and economical processing. Two dimensional materials created by the process of condensation of atoms, molecules or ions are called thin films. The most common deposition techniques utilized for thin film solar cell fabrication are thermal evaporation, sputtering, chemical deposition, chemical vapor deposition, electro-deposition, glow discharge and spray pyrolysis. Today, thin films play an important role in almost all electronic and optical devices.

The study of layered compounds in photovoltaics has experienced great developments in the last decade. In recent years, InSe layered semiconductors of the

III-VI family have been a subject of interest both in thin film and single-crystalline form because of certain properties that make it attractive for device applications. Each layer is formed in packets of two In and two Se sublayers and the interlayer (Se-Se) bonding is of the van der Waals type, while inside the layers the bonding is largely covalent. Due to this bonding scheme, no dangling bonds exist at the surface which is an ideal condition for fabricating metal-semiconductor or p-n heterojunctions. Thus, the interfaces between such layered materials are unstrained even for the relatively high lattice mismatches [1]. The possibility of obtaining p- and n-type conduction with doping makes InSe is a promising material for p-n heterojunction device structures with a low density of interface states [2-4]. Moreover, with a room temperature band gap about 1.3 eV which is close to the solar optimum [5], InSe is an appropriate material for photovoltaic conversion [6-8]. The structural and electrical properties of the InSe thin films, which strongly affect the device performance, depend on the deposition techniques and conditions [9-11]. The understanding of the electrical parameters of the material, considerably influenced by the presence of energy levels in the forbidden gap, is essential for device studies. In the literature, different measurement techniques were used to identify the trap level parameters in InSe single crystals and polycrystalline films such as the dark conductivity [12-14], photoconductivity [15,16], thermally stimulated current [15,17,18] and space-charge-limited current (SCLC) measurements [12,19,20]. The structural and electrical properties of undoped p-InSe thin films, which could be used as a potential absorber layer for heterojunction devices, obtained by thermal evaporation technique were investigated [21] and the results indicated that as-grown films have amorphous structure and heat treatment results in a transformation into polycrystalline state and also increases the conductivity. The electronic properties of the InSe thin films are more favorable than other layered semiconductors such as GaSe and GaTe. Mobilities of majority carriers along the layers can be as high as 10^2-10^3 cm^2/V.s. The indirect gap, some 50 meV below the energy of the direct gap is weak enough not to be observable in optical absorption. Its presence is the reason for the high life times and diffusion lengths of photoexcited carriers, even in comparatively low purity material [1]. The conduction type of InSe thin films plays an important role in device applications and the largest solar cell collection have

been observed with ITO/p-InSe solar cells [1,3]. Wide gap III-VI semiconductor compounds such as GaS, GaSe and InSe are promising materials for visible and infrared detectors. For the near infrared photodetectors n-InSe/p-InSe junctions have been fabricated and investigated [6]. As a Schottky diode, InSe thin films show high rectifications which results in efficient applications of fast rectifiers [22-24]. Conditions for efficiency improvement for ITO/p-InSe/Au single crystal cells are investigated by Pastor et.al [3] and it was found that efficiencies up to 10 % can be obtained by annealing and doping with various metals such as Cd, Zn and As. Photovoltaic effect on TO/ In_xSe_{1-x} amorphous thin film system with different metal contacts (Sb, Au, Al, Ag and Cu) were also investigated by Nang et.al [25] and the results indicated that the best photovoltaic performance obtained with the Sb electrode. A. Segura et.al [1] has also investigated Bi/p-InSe, Pt/n-InSe and ITO/p-InSe device structures and it was reported that among the devices examined Pt/n-InSe structure shown the highest efficiency up to 6% whereas others have shown nearly ohmic behaviors. Au/InSe Schottky barriers were investigated by Di Giulio [26] through dark I-V, C-V and spectral dependence of photoemission current characteristics with a barrier height of about 0.65 eV. It can be seen from the literature that the results concerning the structure and physical properties of InSe and the devices associated with it, are often contradictory [27]. This disparity results from the difficulty of growing single crystals. The complex band structure of this semiconductor results in good rectifying barriers with low work function materials like ITO, as well as with high work function materials like Au and Pt [3].

Studies presented by a number of researchers in literature have proved that InSe may be used for a variety of possible devices for solar energy conversion. The optical and phototransport properties are now sufficiently investigated so that the photovoltaic response can be quantitatively interpreted over all the useful part of the solar spectrum. Barriers can be as high as 1 eV which is close enough to the band gap. However, detailed explanations of the electrical properties of the rectifying structures remain an open question mainly because of poor knowledge of impurity levels in the bulk of material. Despite the fact that InSe films and associated devices has been studied by a large number of workers, most of the work done considered the single crystal forms or n-type polycrystalline films and a very little information is

known about the photovoltaic effect in amorphous semiconductors. Thus, structural, electrical and optical properties of amorphous p-type InSe thin films and related device characteristics are yet to be studied. Therefore, the main purpose of this work is to study the structural and physical properties of amorphous p-type Inse thin film based devices, namely, Schottky barriers in the form of metal/p-InSe junctions and n-CdS/p-InSe heterojunctions. Furthermore, investigation of doping and annealing effects on the devices fabricated is also a subject of this work.

Cadmium-Sulfide which is a compound of the II-VI family, is used in this work as a wide band gap (2.42 eV) window layer for the heterojunction structures. Window layer must be a wide gap material because almost all the absorption should occur within the depletion layer of the narrow gap material. In this sense, CdS is an appropriate material as a window layer for the n-p heterojunction structure over the useful part of solar spectrum since it passes a large fraction of the solar radiation incident on its surface. Furthermore, its resistivity can easily be reduced by intentional doping which results in decreasing the sheet and the contact resistances of the cell so that the depletion layer width in the absorber semiconductor is extended. CdS is one of the most extensively investigated semiconductors in thin film form and a large variety of deposition techniques have been used to obtain solar cells using CdS layers. These deposition techniques include thermal evaporation [28], spray pyrolysis [29], sputtering [30], MBE [31], VPE [32], CVD and chemical deposition [33]. The structural and electrical properties of the CdS thin films strongly depend on the deposition techniques and the substrates temperatures [35]. Evaporated CdS thin films prepared for the solar cell applications usually have resistivities in the range of 1-10^3 (Ωcm) and carrier concentrations in the range of 10^{16} to 10^{18} cm^{-3} [28]. The films are always n-type with a polycrystalline form and the conductivity is dominated by the deviation from stoichiometry which results from the S vacancies or Cd excess. Mobilities are in the range of 0.1-10 ($cm^2V^{-1}s^{-1}$) [36]. It has been observed that CdS films grown at higher rates indicate higher carrier concentration and the carrier concentration is found to increase with an increase in film thickness which results in a corresponding decrease in resistivity [34]. The Cu_2S/CdS heterojunction solar cells was first to receive significant attention when Reynolds et.al [37] in 1954 studied this system and reported a 6% efficiency. Later, Cusano

[38] and Boer [39] produced thin film Cu_2S/CdS solar cells by using thermal evaporation technique. Bogus and Mattes [40] proposed that the performance of Cu_2S/CdS solar cells could be considerably improved by depositing a very thin film of copper layer onto Cu_2S with subsequent heat treatment. Photovoltaic properties of n-CdS/p-Si heterojunction cells were first studied by Okimura et.al [41] in 1967. Later he studied the same system with vacuum evaporated CdS films at various substrate temperatures and reported a 5.5% efficiency. The electrical and photovoltaic properties of CdS solar cells have been studied extensively over the last decade and Scafe published his work on CdS:In/p-Si solar cells with an efficiency of 11%. The CdS/CdTe heterojunction solar cells fabricated by depositing a thin layer of n-CdS onto p-CdTe single crystal wafer have been reported by various workers [42]. The first CdS/CdTe thin film heterojunction solar cell was fabricated by Adirovich et.al [43] with a low efficiency (1%). This work stimulated further research on this system and efficiencies up to 10% have been reported by different groups by the early of 1980's [44]. The practically achievable efficiency of polycrystalline CdS/CdTe cell is estimated to be 22% [45]. To the best of our knowledge, there has been no report published concerning the electrical and photovoltaic properties of n-CdS/p-InSe solar cells so far. In this study, it is proposed that wide band gap n-CdS as a window layer and narrow band gap p-InSe as an absorber layer provides a promising hetero structure as a solar cell with their suitable structural, electrical and optical properties.

In this study, InSe thin films with and without Cd doping and CdS films were deposited by thermal evaporation technique under vacuum. The electrical properties of the films were investigated by means of temperature dependent conductivity, and Hall effect measurements in the temperature range of 100-430 K. The structural parameters and the composition of the films were also studied through X-ray Diffraction (XRD) and Energy Dispersive X-ray Analysis (EDXA), respectively. The surface properties of the films were investigated using scanning electron microscopy (SEM). Post depositional annealing was done following the deposition as a function of time and temperature. Device behaviors of the samples were studied by vacuum evaporation of metallic contacts on the InSe thin films using In, Ag, Au, Al and by C painting. The dark and illuminated current-voltage (I-V), capacitance-voltage (C-V)

as a function of frequency and photocurrent as a function of wavelength were measured on the TO/p-InSe/Metal sandwich structures. Finally, the heterostructures were fabricated by thermal evaporation technique in the form of TO/n-CdS/p-InSe/Metal and the photovoltaic behaviors of these solar cells were studied by carrying out I-V, C-V and photoresponse measurements.

In the second chapter of this thesis, basic theoretical fundamentals about the properties of thin films, metal-semiconductor junctions and n-p heterojunction solar cells are given. In the third chapter, the experimental procedures on the growth of InSe and CdS thin films for the fabrication of associated devices are explained and the details of the measurement techniques are summarized. In chapter four, the structural, electrical and optical properties of the grown thin films and the characterization of the fabricated devices are discussed over the results presented. Finally, general conclusions and the interpretations of the results are made in the last chapter.

CHAPTER 2

THEORETICAL CONSIDERATIONS

2.1 Material Properties

2.1.1 Structural Properties of Indium-Selenide

Indium-Selenide is a layered semiconductor of the III-VI family with a quasi-direct band gap of 1.3 eV at room temperature whereas the indirect gap is 50 meV below the direct gap which is weak enough not to be observable in optical absorption. InSe crystals are easily cleaved along the layer planes and high quality surfaces are obtainable without mechanical grinding or chemical etching [7]. The molecular unit bonded by first-order covalent or ionic forces extends in two dimensions, instead of being three-dimensionally bonded as in group II-VI, IV or III-V semiconductors. The elemental sheet formed by pairs of graphite-like hexagonal lattices with two kinds of atoms as indicated in Fig.2.1. Two of these are bonded by metal-metal bridges which distort the hexagons [1]. Each layer is formed in packets of two In and two Se sub-layers such that the metal atoms are sandwiched between two planes of chalcogen atoms. The layers are themselves bound by van der Waals forces so that layer terminated surfaces posses no dangling bonds. Therefore, interfaces between such layered semiconductors are free of surface states which is a desirable condition for heterojunction applications [46].

The structural and physical properties of InSe differ widely in literature [27]. The contradictory results arise from the difficulty of growing InSe single crystals. Different crystal structures such as hexagonal, rhombohedral and monoclinic forms have been reported by various workers [47]. The first study on the structural properties of indium-monoselenide was reported by Schubert et.al [48].

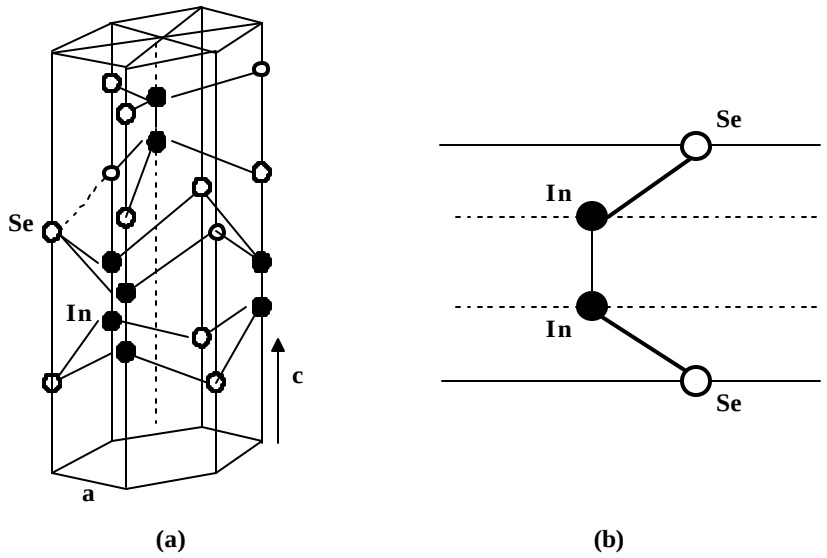


Fig.2.1: (a) The Crystal structure of InSe (b) Representation of a single layer.

In this work the unit cell crystal form was found to be rhombohedral. Later, Celutska and Popovic [49] have determined a hexagonal structure and the melting point was estimated as 636 ^{0}C. Some of these structures can also coexist in the same crystal giving rise to high stacking disorder which strongly affects the transport properties along the c-axis that is normal to the layers. The stacking disorder and weakness of the bonds between adjacent layers result in large densities of extended defects such as dislocations and stacking faults which will act as deep traps of carriers [7,50]. The crystallographic structure of a single layer is the same but due to the weakness of the interlayer bonds, several polytypes have been observed corresponding to different stacking sequences of layers. Most frequently observed polytypes in the family of III-VI compounds are $\beta, \varepsilon, \gamma,$ and δ. The β and ε polytypes are consist of eight atoms in the unit cell and extend over two layers. Whereas γ contains two cations and two anions distributed on four adjacent layers. InSe crystals have been usually observed in the ε and γ polytypes [51-53]. Optical properties of InSe are well known in the ordinary configuration that is perpendicular to c-axis and partially known for parallel to the c-axis where c-axis is defined as perpendicular to the layers. The valence and conduction band levels originate from a single layer which is the split by interlayer interaction. Carrier orbitals for those levels thus

extend along the c-axis and have little two-dimensional character. Therefore, the effective masses do not have large anisotropies. The anisotropies found in transport properties are due to the interlayer defects [26].

2.1.2 Structural Properties of Cadmium-Sulfide

Cadmium-Sulfide is a member of II-VI family and generally crystallizes in the hexagonal wurtzite form which can be considered as two interpenetrating hexagonal close-packed lattices as shown in Fig.2.2. However, it has been reported that CdS films prepared at substrate temperatures up to 150^0C crystallizes as a cubic zincblende structure whereas above 170^0C the structure was found to be hexagonal wurtzite form. Combination of these two structures has been observed for the samples grown between these substrate temperatures [54].

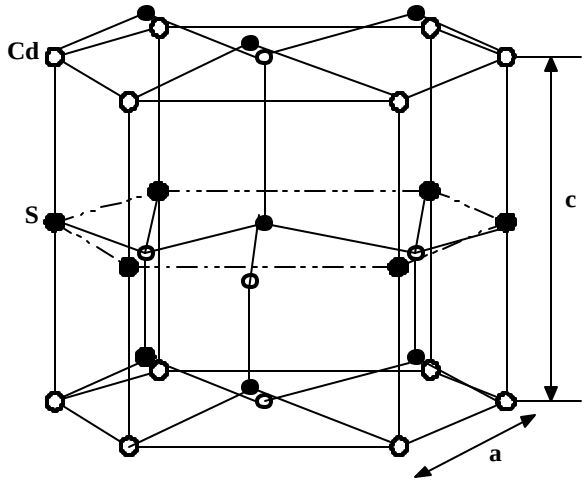


Fig.2.2: Hexagonal wurtzite lattice structure of a CdS crystal.

The grain sizes of these films are usually around 0.3-0.5 μm and as the thickness of the film decreases, the grain sizes tend to decrease with random orientation. After the growth is completed, the grain sizes can be increased by annealing which also improves the crystallinity. CdS has a direct band gap of 2.42 eV at room temperature which corresponds to a wavelength of 0.52 μm, thus a large

fraction of solar spectrum is transmitted through the bulk. Therefore, CdS is a suitable material as a window layer in heterojunction solar cell applications [55-57]. Besides, the optical absorption coefficient is very high for the incident photons which have energies greater than the band gap. CdS begins to sublime at around 700 ^{0}C and melts at about 1750 ^{0}C under several atmospheric pressure. It is possible to grow CdS either from the vapor phase or from the high pressure liquid phase. CdS can only be made n-type and attempts to grow p-type CdS were unsuccessful because of the tendency towards self-compensation in CdS is very strong such that introduced acceptor impurities results in creation of vacancies to maintain the charge neutrality. Anderson and Mitchel [58] and Chernov [59] tried to obtain p-type CdS by ion implantation but Tell and Gibson [60] showed that p-type conductivity was resulted from radiation damage rather than introduced chemical impurities. Pure CdS crystals have a high resistivity of about 10^{12} (Ω-cm) which can be easily reduced by intentional doping with In, Sn, Al, Cl or Br, all of which form shallow donors. Also, sulphur vacancies, resulted from the presence of excess cadmium during film or crystal growth, act as donors and resistivities below 0.1 (Ω-cm) can be achieved with no additional impurity doping. The native donors can also be compensated by the deep acceptor states introducing Cu, Ag or Au impurities into the structure [61]. CdS thin film form used in heterojunction applications grows with a preferred orientation of crystallites in a direction along the c-axis which is perpendicular to the substrate so that no grain boundaries exist parallel to the junction which would limit the flow of the excess carriers to the collector electrode. The degree of orientation decreases as the temperature at which the film deposition rate increases, whereas at low deposition rates higher degree of preferred orientation was observed. Crystallite size also varies with the film thickness. As the film thickness is increased, fewer but larger crystallites are formed in the film. Heat treatment of the CdS thin films changes the film stoichiometry and annealing at higher temperatures results in an increase in crystallite size, reduction in defect density and also re-crystallization of the films [62].

2.2 Transport Mechanisms in Thin Films

2.2.1 Transport Properties of Amorphous Semiconductors

Amorphous semiconductors lack long-range ordering of their constituent atoms which means no unique directionality or axis exists on a macroscopic plane. The short-range order is directly responsible for the observable semiconductor properties such as activated electrical conductivities. Amorphous semiconductors do not consists of close-packed atoms, but rather they contain covalently bonded atoms arranged in an open network with correlations in ordering up to the third or fourth nearest neighbors. Bonding anisotropies associated with the polymorphism of elemental solids and atom size differences for alloy and compounds results in amorphous state in semiconductors. Amorphous semiconductors only differ from crystalline semiconductors in that they contain a number of localized trap-like states within the mobility gap. Disorder of the material tends to restrict motion and thus facilitating self-trapping. The band structure of the amorphous semiconductors indicate narrow tails of localized states at the edges of the valance and conduction bands and further a band of localized levels near the middle of the band gap. Several models were proposed for the band structure of the amorphous semiconductors all of which uses the concept of localized states in the band tails. Based on the Mott's and Anderson's model [65], the configurational disorder in amorphous materials results from the spatial fluctuation in the potential which will lead to the formation of localized states. Therefore, tails above and below the normal band are formed for the amorphous semiconductors. Mott and Davis model indicates that the tails of localized states are narrow and should extent a few tenths of an electron volt into the forbidden gap. They also proposed that the existence of the localized levels near the middle of the band gap originates from defects in the random network such as dangling bonds and vacancies. The density of states distribution with respect to energy is shown in the Fig.2.3, where E_c and E_v represent the energies which separate the states that are localized and extended. Localized gap states which associated with defect centers are located at well defined energies in the gap. Mott suggested that at

the transition from extended to localized states the mobility drops by several orders of magnitude which defines the mobility edge [63,64].

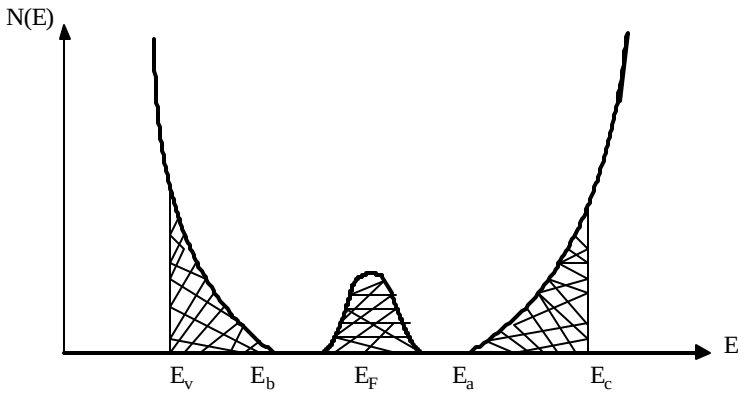


Fig.2.3: Density of states distribution of Davis-Mott model.

The interval between the energies E_c and E_v acts as a pseudo-gap and is called the mobility gap. This gap determines the energy necessary to excite the carrier across the mobility gap. In order to determine whether particular electronic states are localized or extended, one may use the carrier's intrinsic drift mobility in an electric field. If mobility is high ($\mu >> 1\ cm^2/V.s$) and decreases with increasing temperature, the scattering picture in which zeroth-order states are extended may be considered. On the other hand, for low mobility values ($\mu << 1\ cm^2/V.s$) which increases with increasing temperatures, transport is usually interpreted within a hopping picture in which zeroth order states are localized.

According to the Davis and Mott model [65], conduction in amorphous semiconductors occurs in three different processes in different temperature ranges. At very low temperatures, thermally assisted tunneling between states at the Fermi level is responsible for conduction. At higher temperatures, conduction takes place by excitation of charge carriers into the localized states of the band tails by hopping mechanism. At very high temperatures, carriers are excited across the mobility gap into the extended states in which mobility is higher than that of localized states. Below, brief information about these transport mechanisms is given but conduction in localized states will be discussed in section (2.2.2) in detail, thus will not be given here.

a) *Extended State Conduction*. This mechanism is predominant at very high temperatures. Transport occurs due to electrons excited beyond the mobility edge into the extended states under the assumption of constant density of states and constant mobility. The conductivity for the electrons is given by [63],

$$s = eN(E_c)kTm \exp\left[-\frac{(E_c - E_F)}{kT}\right] \tag{2.2.1}$$

where m is the average mobility. Therefore dc conductivity for amorphous semiconductors can be written in the general form of,

$$s = s_0 \exp\left[-\frac{\Delta E}{kT}\right] \tag{2.2.2}$$

where ΔE is the activation energy and σ_0 is the pre-exponential factor.

b) *Conduction in Band tails*. If the wave functions are localized, conduction occurs by thermally activated hopping in the tails of localized states at the band edges. Carriers move from one state to the other due to energy exchange with phonons. Thus, the mobility has temperature dependence in the form of,

$$m = m_0 \exp\left[-\frac{W}{kT}\right] \tag{2.2.3}$$

where m_0 is the pre-exponential factor and depends on the phonon frequency and the average distance covered in one hop. W is the energy necessary for a carrier to hop from one state to the other. The conductivity which depends on the energy distribution of the density of localized states is expressed as the following,

$$s \propto \exp\left[-\frac{(E_a - E_F + W)}{kT}\right] \tag{2.2.4}$$

where E_a is the energy of the band tail of the conduction band.

2.2.2 Transport Properties of Polycrystalline Materials

As compared with amorphous materials, crystallization in polycrystalline state is the long-range ordering of atoms in a periodic solid-phase lattice near equilibrium. Polycrystalline semiconductors are composed of grains with each grain containing array of atoms surrounded by a layer of boundary atoms called grain boundary. The grains or crystallites have random size, shape and orientation of

packing. The grains are formed by independent nucleation and growth process and the grain size is controlled by the number of nucleating sites, which can be increased by rapid cooling or with highly abraded substrate surfaces. The crystallite growth ceases when surrounding grains restrict further growth. Re-crystallization is then possible by annealing which reduces the grain boundary surface area by diffusion. The shape of the crystallite is determined by the surface orientations favorable for additional atom attachment from the vapor phase.

Several models have been proposed by various workers to explain the transport properties of polycrystalline semiconductors [64]. Most of these models are based upon the consideration that the grain boundaries have an inherent space charge region due to interface which results in band bending and potential barriers between the grains as seen in the Fig. 2.4. In the figure, L_b and L_g represent the width of grain boundary and grain size, respectively. The potential barrier height due to grain boundary is $q\phi_b$.

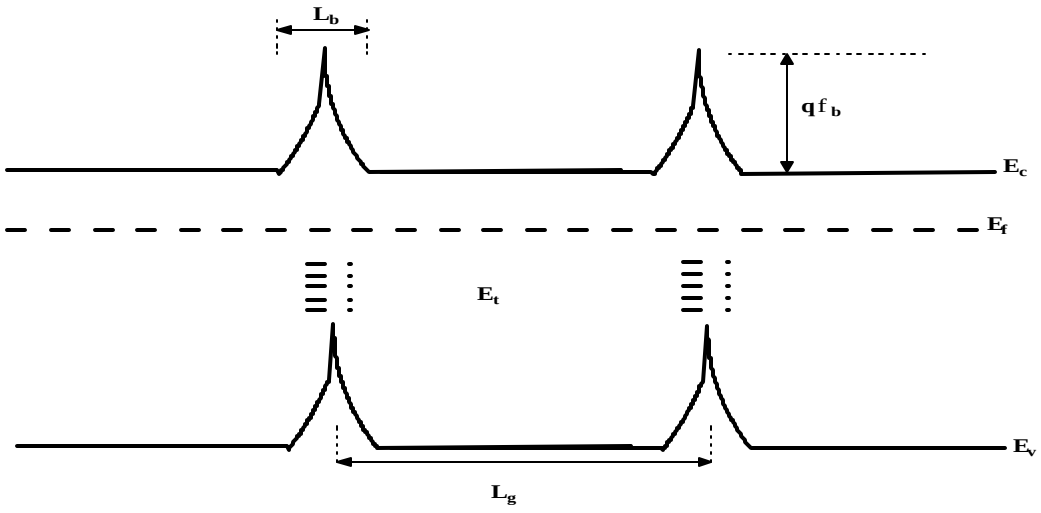


Fig. 2.4: Energy band diagram of an n type polycrystalline semiconductor, representing the grain boundary barrier.

The first model on the transport of polycrystalline materials was proposed by Volger [66]. According to this model, polycrystalline materials have inhomogeneous domains of high conductivity and very low conductivity in which no space charge region exits. The width of the low conductivity regions which are the grain

boundaries is negligible in comparison with the width of the grains. Therefore, this model simulates a situation in which ohmic transport of the carriers dominates. This analysis was followed by Petritz's [67] model in which the thermionic emission was assumed to be the dominant transport mechanism. In his model, he dealt with parameters as averages of many grains. Later, Seto [68] proposed a more detailed model called grain boundary trapping model in which the grain size were taken into account. The model introduces a large number of active trapping sites at the grain boundary which captures free carriers. In this model, thermionic emission and diffusion of charge carriers through the grain boundary barrier were considered as the conduction mechanisms.

In general, three transport mechanisms are favorable for polycrystalline semiconductors in different temperature regions. These mechanisms are hopping between the localized states, tunneling through the grain boundary barrier and thermionic emission of the carriers. Below, the three mechanisms are briefly discussed and more detailed information can be found in literature.

A) *Thermionic Emission.* This type of conduction mechanism is dominant in the high temperatures due to the carriers which have enough energy to cross over the barrier formed at the grain boundary region. As mentioned, the grains in a real polycrystalline material exist in different size and shapes. Grains or crystallites joined together by the grain boundaries which consist of a few atomic layers of disordered atoms. The presence of the large number of defects due to incomplete atomic bonding resulted from the disordered atoms at the boundary. The carriers are trapped due to the defect states and therefore, the number of free carriers available for conduction is reduced. To simplify this model, the grains with different size and shapes are assumed to have the identical size (L_g) and the shape. Another assumption is that all the impurity atoms are ionized and of one type. Furthermore, the distribution of these impurities is assumed to be uniform. The grain boundaries consist of number of traps which are initially neutral and become charged after trapping free carriers. All the mobile carriers in a region very close to the grain boundary are trapped, resulting in a space charge region. Conduction occurs in this model by tunneling and thermionic emission of carriers. However, for highly doped materials, the barrier height decreases very sharply so that the tunneling currents can

be neglected. The conductivity can now be determined using a thermionic emission current only [64],

$$J = qn_{av}\left(\frac{kT}{2pm^*}\right)^{\frac{1}{2}} \exp\left(-\frac{qf_b}{kT}\right)\left[\exp\left(\frac{qV_a}{kT}\right)-1\right] \qquad (2.2.5)$$

where n_{av} is the average carrier concentration and V_a is the applied voltage across the grain boundary. For small values of applied voltage, $(qV_a << kT)$, the current-voltage expression fits a linear relationship which indicates that the ohmic transport of carriers are dominant. Then, the conductivity can be expressed as,

$$s = q^2 L_g n_{av}\left(\frac{1}{2}pkTm^*\right)^{1/2} \exp\left(-\frac{qf_b}{kT}\right) \qquad (2.2.6)$$

for a polycrystalline semiconductor with a grain size L_g. Using the general expression for conductivity,

$$s = qn_{av}m \qquad (2.2.7)$$

effective mobility of the carriers is obtained as the following relation,

$$m = qL_g\left(\frac{1}{2pkTm^*}\right)^{\frac{1}{2}} \exp\left(-\frac{f_b}{kT}\right) = m_0 \exp\left(-\frac{f_b}{kT}\right) \qquad (2.2.8)$$

Details of the derivations and the results for the cases in which $L_gN>N_t$ and $L_gN<N_t$, where N is the concentration of impurities and N_t being the number of traps, can be found in literature [68]. As the grain boundary barrier height increases with doping, the mobility decreases.

B) *Tunneling*. If the barrier at the grain boundary is high but narrow, the carriers do not have enough energy to surmount the barrier at low temperatures. Instead of thermionic emission, conduction occurs by quantum mechanical tunneling of the carriers through the barrier. The tunneling currents have been studied by various workers such as Seager and Pike [69], Garcia [70]. Seto [68] assumed that the bottom of the conduction band inside the crystallite is taken to be at zero energy and the number of trap states at the boundary is temperature independent. Then, the transport of carriers is mainly due to the thermionic emission and tunneling currents. The tunneling current density calculated by WKB (Wentzel-Kramers-Brillouin) approximation is given by Simmons [71],

$$J = J_0\left(\frac{FT}{\sin(FT)}\right) \tag{2.2.9}$$

where J_o is the tunneling current at 0 K and F is given by,

$$F = \frac{2kp^2(2m^*)^{\frac{1}{2}}L_{bf}}{h\langle f\rangle^{\frac{1}{2}}} \tag{2.2.10}$$

where $\langle\phi\tilde{n}$ is the average barrier height of the grain boundary potential and L_{bf} is the barrier width at the Fermi level. The conductivity can be found from $s = L_g J/V$ as,

$$s = s_0\frac{FT}{\sin(FT)} \tag{2.2.11}$$

with s_0 is the conductivity at 0 K. If FT is small enough, the conduction for tunneling mechanism is expressed as

$$s = s_0\left[1+\left(\frac{F^2}{6}\right)T^2\right] \tag{2.2.12}$$

C) *Hopping*. Hopping conduction is the dominating transport mechanism in the low temperature region. When the impurity states are sufficiently low, they do not contribute to conduction within the impurity band. Therefore, the current conduction occurs for the carriers having low activation energy due to hopping between the localized states. According to Mott's hopping mechanism [63], electrons in states near the Fermi energy hop from a state below the Fermi energy to one above by exchanging energy with a phonon. At low temperatures, hopping conduction by electrons in states near Fermi level dominates the thermionic emission conduction which is due to the thermal excitation of electrons to the conduction band. There are two possible processes that hopping can take place in the conduction of carriers. One of them is the constant range hopping which occurs by the hopping of carriers to the nearest states. The other one is the variable range hopping in which the carriers hop to empty states away from the nearest neighbor. For the polycrystalline materials, charge carriers which do not have enough energy to surmount the barrier at the grain boundary hops into a neutral trap state from a charged trap state. The hopping process in that case depends on the grain size L_g, doping concentration N and the dielectric constant of the sample e. The definition of the Debye length is given by [73],

$$L_D = \left(\frac{ekT}{q^2 N} \right)^{\frac{1}{2}} \tag{2.2.13}$$

If the grain size is much smaller than the Debye length, the variable range hoping conduction will be dominant over a wide range of temperature. Otherwise, the variable range hopping will be effective only at the lowest temperature.

According to Mott's analysis, the average energy difference between states near the Fermi level is determined by the assumption that the probability of an electron jumping to another site is at least one. Thus the energy W can be expressed as [63],

$$W = \frac{3}{4pR^3 N(E_F)} \tag{2.2.14}$$

The most probable jump distance (R), defined as the distance that electrons jump from one state to another, and is given by,

$$R = \left[\frac{9}{8p\,aN(E_F)kT} \right]^{\frac{1}{4}} \tag{2.2.15}$$

where α is the decay constant that indicates the rate of fall-off the wave function of an electron at a site. Thus, the jump probability for the most probable jumping distance is given by,

$$P = n_{ph} \exp\left(\frac{-A}{T^{1/4}} \right) \tag{2.2.16}$$

where

$$A = 2.1\left[\frac{a^3}{kN(E_F)} \right]^{1/4} \tag{2.2.17}$$

Therefore, according to the Mott's analysis the temperature dependence of the variable range hopping conduction is given as,

$$s = s_0(T) \exp\left(-\frac{A}{T^{1/4}} \right) \tag{2.2.18}$$

There are several derivations proposed for the conductivity of variable range hopping expression. In general, temperature dependence remains the same but the numerical factor *A* differs. The most general form of the conductivity for the disordered materials at low temperatures is given as the following,

$$s = \frac{s_0}{\sqrt{T}} \exp\left[-\left(\frac{T_0}{T}\right)^{1/4}\right] \qquad (2.2.19)$$

where σ_0 is the pre-exponential factor and T_0 is the measure of disorder and given by the expression,

$$T_0 = \frac{l a^3}{kN(E_F)} \qquad (2.2.20)$$

where l is a dimensionless constant at a value around 18. The variable range hopping is always to be expected when $W > kT$ and $aR>1$.

2.3 Electrical Characterization

2.3.1 Hall Effect

The Hall effect was discovered by E.H. Hall in 1879 during an investigation on the force acting on a current carrying conductor in a magnetic field. The Hall effect measurements provide information on the carrier type, the carrier concentration and the mobility of the carriers at a given temperature.

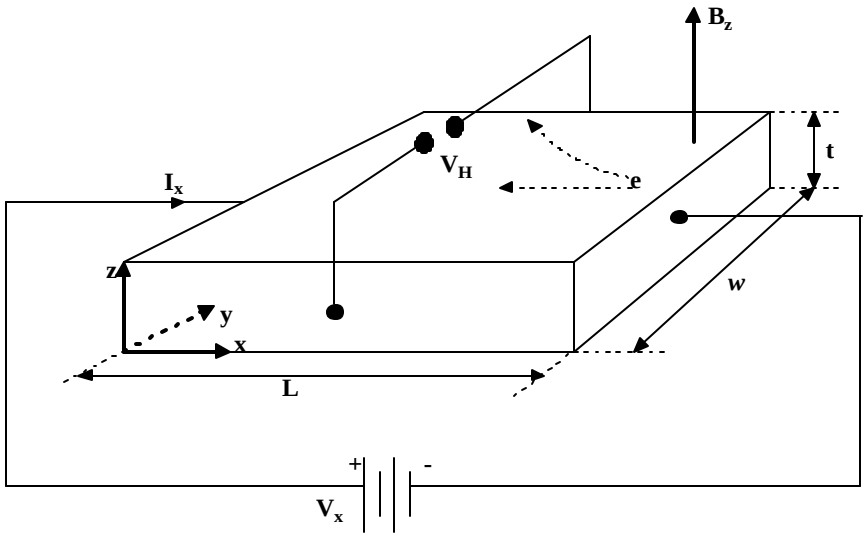


Fig.2.5: Configuration for measuring the Hall effect.

When a magnetic field is applied perpendicular to the direction of current flow in the z-direction as shown in Fig.2.5, the carriers will be deflected due to the Lorentz force and an electric field is built up along the y-direction resulting from the accumulated carriers at *y=0* surface of the semiconductor. The electric field produced by the deflected carriers is called the Hall field. The direction of this field depends on the type of carriers responsible for the current flow. Since there is no net current along the y-direction in the steady state, the magnetic field force will be exactly balanced by the induced electric field force which can be expressed as [75],

$$\vec{F} = q\left(\vec{E} + \vec{v} \times \vec{B}\right) = 0 \qquad (2.3.1)$$

The current density in terms of the drift velocity is defined as,

$$\vec{J} = nq\vec{v} \qquad (2.3.2)$$

Thus, from Eq2.3.1 and Eq.2.3.2 the Hall field can be obtained for the configuration considered, as the following

$$E_y = \frac{J_x B_z}{nq} \qquad (2.3.3)$$

Hall field is proportional to the product of current density and magnetic field. The proportionality constant is defined as the Hall coefficient and in general given by,

$$R_H = \frac{E_y}{J_x B_z} = -\frac{r}{nq}, \frac{r}{pq} \qquad (2.3.4)$$

where r is the Hall factor which depends on the scattering mechanism in the semiconductor. In the high magnetic field limit, r is of the order of unity. The positive sign is for the case when the free carriers are holes and negative sign for the case when free carriers are electrons. Therefore, Hall coefficient leads to a determination of the carrier type as well as the carrier concentration.

If Ohm's law obeyed, the conductivity must be independent of the applied electric field. Thus the conductivity is defined as $s = nqm$ where m is the electron drift velocity per unit electric field (or equal to the Hall mobility for free electrons). Then, the Hall mobility is given by the following expression,

$$m_H = |R_H| s \qquad (2.3.5)$$

and measured quantity Hall voltage ($V_H = E_y w$) can be derived from Eq.2.3.3 as,

$$V_H = \frac{R_H BI}{t} \tag{2.3.6}$$

where I is the current passing through the sample and t is the thickness along the direction of the magnetic field.

2.3.2 Space Charge Limited Currents

The space charge limited current (SCLC) measurements provide a reliable method for obtaining information about the position of trapping states and the density of these states in the forbidden gap of wide band gap semiconductors. If the electrodes made on the semiconductor film are ohmic, the conduction process is space charge limited. Ohmic contacts will not add significant impedance to the resistance of the bulk of the semiconductor and thus the equilibrium carrier densities in the bulk is not affected by the electrodes. For low applied voltages, the conduction is controlled by the resistance of the bulk of the semiconductor and a linear current-voltage curve is obtained by Ohm's law. Because the traps are initially empty at lower injection levels and injected carriers will be captured and immobilized. Thus, this results in a reduced current at lower applied voltages. However for higher voltages, carriers injected from the contact dominate the current flow in the film. When the injected carrier density is greater than the free carrier density, the current becomes space charge limited since the traps will be saturated and injected carriers will directly contribute to the conduction process and increases the current flow. Thus, the current-voltage characteristic shows a linear behavior at low applied voltages whereas when the traps are saturated at higher voltages the ohmic region is followed by a super linear region in which current is proportional to V^l, l is equal to 2.

The general form of the current density with the presence of the single set of trap levels is given by Mathur and Dahiya [79] and Rose [80],

$$J = \left(\frac{2l+1}{l+1}\right)^{l+1}\left(\frac{l}{l+1}\right)^{l}\left(\frac{e_s}{N_t}\right)q^{(1-l)}mN_v \exp\left(-\frac{E_t}{kT}\right)\frac{V_a^{(l+1)}}{L^{(2l+1)}} \tag{2.3.7}$$

where V_a is the applied voltage, e_s is the dielectric constant of the material, L is the distance between electrodes, m is the mobility of the carriers, $l = T_c/T$ and T_c is defined as the characteristic temperature of the trap distribution. When the material contains

traps, most of the injected space charge condenses into the traps so that only a fraction of the charge contributes to the conduction. Thus for this model, when a single set of discrete shallow trap levels are present, in the super linear region where *l=2*, the space charge current takes the form as the following relation,

$$J = \frac{9\varepsilon_s \mu q V_a^{\,2}}{8L^3} \tag{2.3.8}$$

where q is the ratio of free charge to trapped charge density and given by,

$$q = \left(\frac{N_v}{N_t}\right)\exp\left(-\frac{E_t}{kT}\right) \tag{2.3.9}$$

where N_t is the trap density and E_t is the position of the trap above the top of the valance band. As the voltage increases further to the trap filled limit, the semiconductor acts as a trap free material and current-voltage characteristic shows a steep increase again by an amount of θ^{-1} [81].

The SCLC mechanism discussed so far has regarded the energy level of any kind of traps with density N_t located at E_t. In the case of amorphous semiconductor films evaporated thin layers of poorly defined crystallinity, this approach does not explain the current injection mechanism due to the large amount of structural disorder. In this case, the SCLC mechanism is explained by the presence of an exponential distribution of trap levels. At high voltages, the voltage exponents were found to be greater than 2 which indicate the energy distribution of traps instead of discrete levels. The distribution of the trap states in energy can be represented by a Gaussian distribution and is given by the following relation [82],

$$N_t(E) = N_0 \exp\left(\frac{E_v - E}{kT_c}\right) = N_n \exp\left(\frac{E_{fo} - E}{kT_c}\right) \tag{2.3.10}$$

where N_n is defined in terms of the thermal equilibrium trap density N_0,

$$N_n = N_0 \exp\left(\frac{E_v - E_{fo}}{kT_c}\right) \tag{2.3.11}$$

The current density can be defined as $J = \rho n_d$, where the drift velocity is proportional to the applied voltage as $n_d = \mu(V_a/L)$ and the charge density as $\rho \approx qN_v(\varepsilon_s V_a / qL^2 N_0 kT_c)^l$. Therefore, the current density in the presence of distribution of traps in the band gap of the amorphous films is given by the following expression

under the assumption that the shift of the Fermi level from the equilibrium value is less than kT_c,

$$J \cong qmN_v \left(\frac{e_s}{qN_0 kT_c} \right)^l \frac{V_a^{(l+1)}}{L^{(2l+1)}} \tag{2.3.12}$$

In the case that T_c<T, the empty traps at the bottom of the distribution near the valence band always dominates the ones near the quasi-Fermi level, and the process turns into the case when the discrete traps present. In deriving Eq.2.3.12, it has been assumed that $kT_c > E_f - E_{f0}$ so that the traps can be considered as uniformly distributed in energy such that $N_t(E) \sim N_n$. In this approximation, the current density relation can be written as,

$$J \cong qp_o m \left(\frac{V_a}{L} \right) \exp\left(\frac{e_s V_a}{qN_n kTL^2} \right) \tag{2.3.13}$$

where p_o is the free hole density and given by,

$$p_o = N_v \exp\left(\frac{E_v - E_{f0}}{kT} \right) \tag{2.3.14}$$

The current density which increases more sharply with voltage than that of discrete traps obtained in Eq.2.3.13 is typical that can be expected in an amorphous solid [74,76].

2.4 Metal-Semiconductor Junctions

2.4.1 Barrier Formation

When two substances are brought into contact, a redistribution of charge occurs; finally a new equilibrium condition is reached in which the Fermi levels of the two substances are at equal heights. The effect of the surface states is ignored here and will be discussed briefly in section (2.4.3). The band diagram of a p-type semiconductor-metal junction before contact is formed represented in Fig.2.6, for the case in which the work function of the semiconductor is greater than the work function of the metal. E_{mf} and E_{sf} represent the Fermi energy levels of metal and the semiconductor, respectively. E_{vac} is the vacuum energy level for both before contact

is made. Work function is defined as the energy required removing an electron from the top of the Fermi level to the vacuum level.

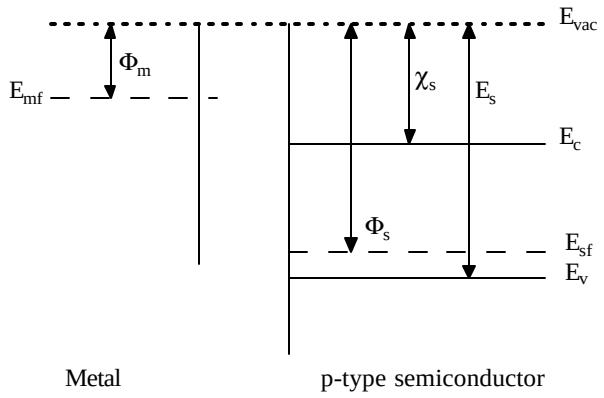


Fig.2.6: Energy-band diagram of metal-p-type semiconductor before contact when $\Phi_s > \Phi_m$.

In the figure, work function of the metal and the p-type semiconductor is denoted by Φ_m and Φ_s, respectively. Work function of the semiconductor depends on the doping and impurity because the position of the Fermi level of the semiconductor can be altered by the variations of these parameters. Electron affinity (χ_s) of the semiconductor is the energy required to remove an electron from the bottom of the conduction band to the vacuum level. Before contact, the Fermi level of the semiconductor is below the Fermi level of the metal by an amount ($\Phi_s - \Phi_m$). As the gap between the metal and the p-type semiconductor decreases, electrons flow from the metal into the semiconductor until the Fermi levels of both sides are leveled. A negative space charge region of thickness *d* which is depleted of holes in the semiconductor will be created due to ionized acceptors. Accordingly, a surface density of positive charge formed at the metal surface as seen in Fig.2.7.

Due to this new charge configuration at the metal-semiconductor junction, an electric field *e* which is located almost entirely in the depletion region of the semiconductor is produced. This electric field results in a gradient of electrostatic potential across the depletion layer which also means that the energy levels in the bulk of semiconductor have been raised by an amount ($\Phi_s - \Phi_m$). Therefore, the built-

in potential barrier between the semiconductor and the metal for a hole going from the semiconductor to the metal is given by $qV_{bi} = (\Phi_s - \Phi_m)$. However, the potential barrier for holes on the metal side of the contact is $(E_s - \Phi_m)$, where E_s is defined as the depth of the top of the filled band of the semiconductor below the vacuum level and given by $(\chi_s + E_g)$.

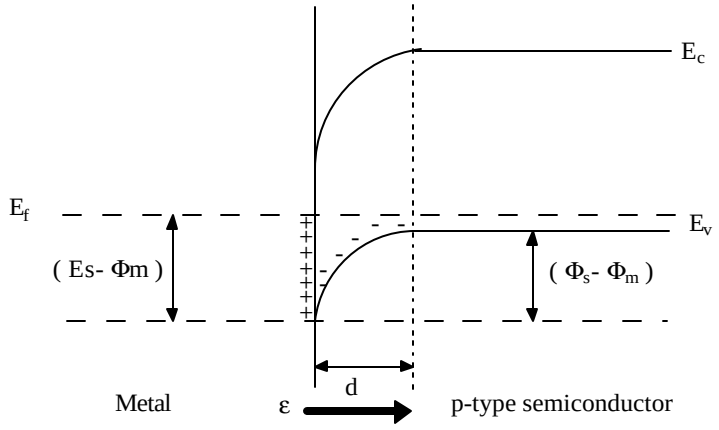


Fig.2.7: Energy band diagram after contact is made.

The above discussion explained the barrier formation at the metal-semiconductor junction for the case that the work function of the semiconductor is greater than the work function of the metal. The opposite case for which Φ_m is greater than Φ_s can be analyzed by analogy, as the following. The Fermi level in the semiconductor is above the Fermi level in the metal by an amount $(\Phi_m - \Phi_s)$. As the gap between metal and semiconductor vanishes, electrons flow out of the semiconductor leaving a positive surface charge due to holes on the semiconductor side and a negative surface charge on the metal side. Therefore, the Fermi level in the semiconductor is lowered by an amount of $(\Phi_m - \Phi_s)$ and leveled with the Fermi level of the metal. Holes that move into the metal from the semiconductor are neutralized instantly due to the high electron concentration in the metal side. As seen in Fig.2.8, no barrier formed for the holes in the semiconductor. Such a metal-p-type semiconductor junction shows an ohmic behavior, since the forward and the reverse currents are almost equal [72,77].

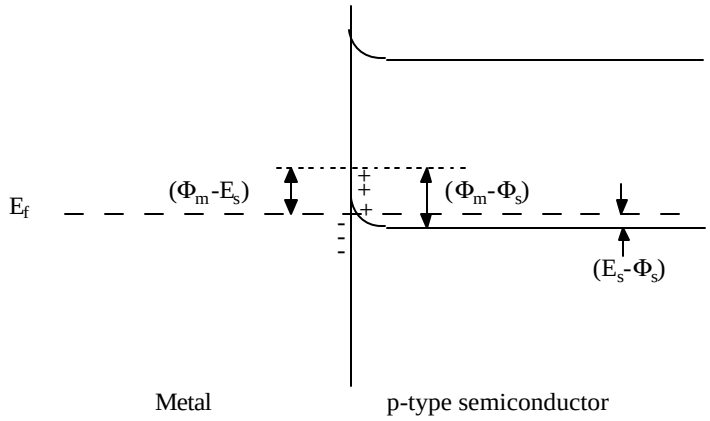


Fig. 2.8: Energy band diagram after contact when $\Phi_s < \Phi_m$.

2.4.2 Effect of an Applied Potential on a Metal-Semiconductor Junction

For a p-type semiconductor-metal junction, forward bias is a positive potential applied to the semiconductor side. The barrier to hole flow is lowered by qV_a under the application of forward voltage V_a. Thus the barrier to the flow of holes becomes $qV_i = (\Phi_s - \Phi_m - qV_a)$. However, barrier height for the reverse bias increases as the applied voltage increases. Therefore, the hole flow to the metal is decreased. Under the reverse bias of the junction by which the semiconductor is made negative with respect to the metal, the barrier becomes $(\Phi_s - \Phi_m + qV_a)$ for the holes. In the case of $\Phi_m > \Phi_s$, there is no barrier formed to current flow for holes, and applied bias voltage does not affect the net current flow across the junction. However, for $\Phi_s > \Phi_m$ case, the net current at equilibrium is zero through the junction meaning that two equal and opposite currents J_0 are crossing the barrier. If a forward voltage is applied to the junction, the hole current flowing from the semiconductor to metal is changed by a factor $\exp(qV_a/kT)$ since all the energy levels in the semiconductor is lowered by an amount of qV_a, whereas the current from metal to semiconductor remains the same. Then, by choosing the direction from semiconductor to metal as positive, there is net flow of current through the junction with $J = J_0(\exp(qV_a/nkT) - 1)$ dependence.

Therefore J-V characteristic of this junction fits to an asymmetric behavior and is rectifying.

All the above discussions can be summarized as the following. For a p-type semiconductor-metal junction, if the semiconductor work function is greater than the metal work function, it is expected that the contact to be rectifying. Otherwise the contact is expected to be ohmic. It can be shown that this rule is reversed for metal contacts to an n-type semiconductor for which the contact is rectifying if $\Phi_s < \Phi_m$. However, this rule may not be consistent with the experimental results. One reason is that the neglect of the effect of the surface states at the semiconductor surface. Furthermore, the determinations of the work functions of metals are widely spread in value which makes difficult to use this rule [72].

2.4.3 Effect of the Surface States to Metal-Semiconductor Junctions

The surface properties of the semiconductors depend on the density and energy distribution of the surface states. The presence of the surface states may be associated with incomplete covalent bonds. Thus, each surface atom has one broken covalent bond known as dangling bonds. Due to these surface states a surface potential barrier must be included in the band diagram if the semiconductor surface has large number of dangling bonds. This results in energy levels in the forbidden gap of the semiconductor. Further, chemical defects such as a thin oxide layer on the surface may be causing the existence of these surface states. There is generally one such surface state per surface atom. The wave function for such a state is localized in space near surface. If the number of surface states is high, the wave functions associated with them may overlap to form the bands. The surface band structure of a p-type semiconductor can be analyzed with donor surface states. Assuming that the number of surface donors is not high and all of them are ionized such that having given up their electrons to acceptors in the bulk at equilibrium. This in turn means that a positive surface charge and a negative space charge region in the bulk of the semiconductor. Due to this space charge, the electrostatic potential is lower in the bulk than at the surface by Φ, the surface potential. This also means that the hole energy in the bulk is higher by an amount of $q\Phi$, than it is at the surface. The net

result is that the energy bands are bent downward at the surface, relative to the bulk. In this case the surface donor energy is above the Fermi level because all of the donors are empty. In the case considered above the Fermi level position of the surface is determined by the Fermi level position in the bulk, since it is assumed that all of the surface states are ionized.

Considering a semiconductor for which the number of surface states is very high such that not all of them are ionized. Then, the electrons flow from the surface donors into the p-type semiconductor bulk until the Fermi level at the surface coincides with the surface donor energy. This in turn means that some surface donors will remain un-ionized, occupied by electrons. Therefore, the position of the Fermi level at the surface is fixed, and is independent of the doping in the bulk of the semiconductor which is called Fermi level pinning at the surface donor energy.

2.4.4 Current Transport Theory in Schottky Barriers

The current transport in Schottky barriers is primarily due to majority carriers in contrast to p-n junctions where minority carriers are responsible. The phenomena affecting majority carrier current flow in Schottky barriers can be listed as thermionic emission, diffusion, tunneling, space charge effects and image force lowering of the barrier. There are two main theories on the current transport mechanisms in metal-semiconductor junctions. Thermionic emission theory is first proposed by Bethe [83] and the diffusion theory has been introduced by Schottky [84]. The more general theory which combines the two into a single theory is later developed by Crowell and Sze [85].

The thermionic emission characteristics are derived using the assumptions that the barrier height is much larger than kT. The electron collisions within the depletion region and the effect of image force are neglected so that the current flow only depends on the barrier height. When the junction is forward biased, the barrier is lowered to $q(V_{bi}-V_a)$ and holes with energies greater than the barrier flow to the metal. However, the current flow from the metal into the semiconductor is unaffected by the applied voltage on the contact. Thus, the current flowing out of the metal is

the same as its equilibrium value. The current density J_{sm} from semiconductor to the metal is given for the thermionic emission theory [78] as,

$$J_{sm} = qp\left(\frac{kT}{2pm*}\right)^{1/2} \exp\left(-\frac{m*u^2}{2kT}\right) \tag{2.4.1}$$

where p is the hole concentration, $m*$ is the effective mass for a free hole and the u is the minimum velocity required to surmount the barrier. The following relation should be satisfied in order for a hole to flow over the barrier.

$$\frac{1}{2}mu^2 = q(V_{bi} - V_a) \tag{2.4.2}$$

The hole concentration of the semiconductor is defined as the following,

$$p = p_0 \exp\left(-q\frac{(V_{bi} - V_a)}{kT}\right) \tag{2.4.3}$$

Where p_0 is the hole concentration in the neutral region of the semiconductor and is defined in terms of the effective density of states as,

$$p_0 = N_v \exp\left(-\frac{(E_f - E_v)}{kT}\right) \tag{2.4.4}$$

Thus, the hole concentration in terms of the barrier height f_B is given by,

$$p = N_v \exp\left(-q\frac{(f_B - V_a)}{kT}\right) \tag{2.4.5}$$

Eq.2.4.2 and Eq.2.4.5 into Eq.2.4.1 result in the final relation for the current flowing from the semiconductor to metal,

$$J_{sm} = A*T^2 \exp\left(-\frac{qf_B}{kT}\right)\exp\left(\frac{qV_a}{kT}\right) \tag{2.4.6}$$

where $A*=(4\pi qm*k^2/h^3)$ is the Richardson constant for holes emitted into metal.

Since the barrier height for the current flow from the metal into the semiconductor is not affected by the applied voltage, it has to be equal to its equilibrium value when V_a=0. Thus, this current is defined by analogy,

$$J_{ms} = -A*T^2 \exp\left(-\frac{qf_B}{kT}\right) \tag{2.4.7}$$

The total current density J is the addition of these two current densities and found as,

$$J_{ms} = A*T^2 \exp\left(-\frac{qf_B}{kT}\right)\left[\exp\left(\frac{qV_a}{kT}\right) - 1\right] \tag{2.4.8}$$

Defining the terms outside the parenthesis as the saturation current J_0 density, the relation for the hole current transport in metal-semiconductor junction according to the thermionic emission theory is obtained as the following,

$$J = J_0\left[\exp\left(\frac{qV}{kT}\right)-1\right] \qquad (2.4.9)$$

A hole has to pass through the depletion region before emitted into the metal. The effect of collisions within the depletion region is included in the diffusion theory. The theory assumes that the barrier height is much larger than kT, the carrier concentrations are unaffected by the current flow and the impurity concentration of the semiconductor is nondegenerate. According to this theory, the current is limited by diffusion and drift of the carriers in the depletion region. An electric field applied to the device will produce a force on electrons and holes so that they will experience a net acceleration and net movement, provided that there are available energy states in the conduction and valence bands. This net movement of charge due to an electric field is called drift. Thus, the drift current is the result of this applied field. In addition to drift, diffusion is the process whereby charge flows from a region of high concentration toward a region of low concentration. The net flow of charge would result in a diffusion current.

There are two other important carrier transport mechanisms which occur in the Schottky barrier that should be discussed separately is tunneling through the barrier and carrier recombination (or generation) in the depletion and neutral regions. Tunneling through the barrier and the recombination in the depletion region are the main reasons of departure from the ideal diode behavior.

The tunneling phenomenon is a majority carrier effect. The tunneling time of carriers through the potential energy barrier is determined by the quantum transition probability per unit time. The space charge width in rectifying metal-semiconductor contact is inversely proportional to the square root of the semiconductor doping. The width of the semiconductor depletion region decreases as the doping concentration in the semiconductor increases. Thus, the probability of tunneling through the barrier increases. The tunneling current increases exponentially with semiconductor doping. The tunnel current can also vary with temperature because of the temperature

dependence of the barrier height. Tunneling occurs either as field emission or thermionic field emission.

For lightly doped semiconductors ($N_D<10^{17}\ cm^{-3}$) the current flows as a result of thermionic emission with holes thermally excited over the barrier. In the intermediate doping range ($10^{17}<N_D<10^{19}\ cm^{-3}$) thermionic field emission dominates in which carriers are thermally excited to an energy where the barrier is narrow enough for tunneling. However, at low temperatures for highly doped semiconductors ($N_D>10^{19} cm^{-3}$) the process is known as field emission in which the holes can tunnel directly through the barrier, since the barrier is so narrow at the valence band for the holes to pass through the metal side. Thus, for a metal-semiconductor junction with a high impurity doping concentration the tunneling process will be dominant transport mechanism [65,74].

Carrier generation or recombination in the junction depletion region is also an important factor that explains the deviations from ideality of the diode (n>1). The generation or recombination current has to be added to the thermionic emission current in order to obtain more precise results. The electron-hole pair generation is balanced by the recombination rate in the depletion region of the barrier at thermal equilibrium (no applied bias). When there is an applied bias on the junction, a net generation or recombination of carriers exists depending on the polarity of the applied bias. If a reverse voltage is applied to the junction made on the n-type semiconductor, number of electron-hole pairs in excess of their equilibrium value will be generated in the depletion region. Thus a reverse current is formed due to these pairs which were forced to move by the electric field of the barrier. However, if the junction is forward biased then the electrons will move into the depletion region from the neutral bulk semiconductor and holes will be injected from the metal. Therefore, these excess electron-hole pairs will recombine in the depletion region to give a forward recombination current. The carrier generation and recombination current in the depletion region is given by [86],

$$J_{RG} = J_0\left[\exp\left(\frac{qV_a}{2kT}\right)-1\right] \qquad (2.4.10)$$

with $J_0 = (qdp_i / 2\tau_0)$ where d is the width of the depletion region and τ_0 is the minority carrier lifetime in the depletion region. The current is a generation current

when the junction is reverse biased and is a recombination current when the junction is forward biased. According to the Eq.2.4.10 the recombination current is important only at low values of the forward bias. Further, a generation-recombination current in depletion region has to be taken into account when the barrier height is large at low temperatures and the semiconductor is lightly doped. A recombination center is most effective when its energy level lies at the center of the band gap, namely at $E_g/2$ which means the semiconductor is lightly doped or intrinsic.

2.4.5 Metal-Semiconductor Junction Capacitance

The electric field and potential distribution in the depletion region of a metal-semiconductor junction depends on the applied voltage, the barrier height and the impurity concentration. Assuming that the semiconductor is non-degenerate and uniformly doped, the width of the depletion region can be obtained from the solution of the Poisson equation with the abrupt junction approximation. If the charge density in the depletion region is due to uniformly distributed ionized acceptors only, the depletion region width is given by the following relation [87],

$$w = \left(\frac{2e_s}{qN_A} \left| V_{bi} - V_a \right| \right)^{\frac{1}{2}} \tag{2.4.11}$$

where V_{bi} is the built-in potential at zero bias. The width of the depletion region can be altered by a change in the voltage across the Schottky barrier junction. The depletion region width decreases below its equilibrium value with the increasing forward bias and increases with reverse bias. The movement of the charge carriers into the space charge layer or out of this region is the cause of this change in the depletion region width.

The barrier height of the junction and the acceptor concentration of the semiconductor can be determined through the capacitance-voltage characteristics. In this technique, the diode capacitance per unit area is measured as a function of applied reverse bias. When a small ac voltage is superimposed upon a reverse dc bias, charges of one sign are induced on the metal surface and charges of opposite

sign in the semiconductor. The depletion region charge per unit area is then expressed as,

$$Q_d = \left[2qe_s N_A \left(V_{bi} - \frac{kT}{q} \right) \right]^{\frac{1}{2}} \tag{2.4.12}$$

and thus the depletion region capacitance excluding the image force barrier lowering is given by,

$$C = A \left[\frac{qe_s N_A}{2\left(V_{bi} + V_R - \frac{kT}{q} \right)} \right]^{\frac{1}{2}} \tag{2.4.13}$$

where A is the diode cross-sectional area, e_s is the permittivity of the semiconductor, V_R is the applied reverse voltage. In the derivation of this relation, it was assumed that p-type semiconductor has uniform acceptor concentration and no interfacial oxide layer exits at the junction. It is clear that a plot of C^{-2} *vs* V_R results in a straight line with a slope $\frac{2}{A^2 e_s q N_A}$ which leads the determination of acceptor concentration. The intercept on the voltage axis yields,

$$V_0 = \left(V_{bi} - \frac{kT}{q} \right) \tag{2.4.14}$$

and the barrier height can be calculated from Eq. 2.4.14 as,

$$f_B = \left(qV_0 + kT + f_n \right) \tag{2.4.15}$$

where f_n is the penetration of the Fermi level in the band gap of the semiconductor. The kT factor comes from the contribution of majority carriers to the space charge. A comprehensive discussion of determination of barrier height from C-V measurements has been given by Goodman [88] who also dealt with the limitations of the method.

2.4.6 The Spectral Response of Metal-Semiconductor Junctions.

Illumination of a metal-semiconductor junction by a monochromatic light produces a photocurrent across the device. The measurement of the wavelength dependence of photocurrent is an effective tool as a characterization technique. Any change in the material properties or in the electronic structure of the junction result in a change in the photocurrent which shows up in the spectral response curve and analysis of the data can provide considerable information on the nature of the change. The spectral response measurement is the most direct and precise method of determining the barrier height of a metal-semiconductor junction. A basic set up for the method and the photo excitation mechanism are shown in Fig.2.9.

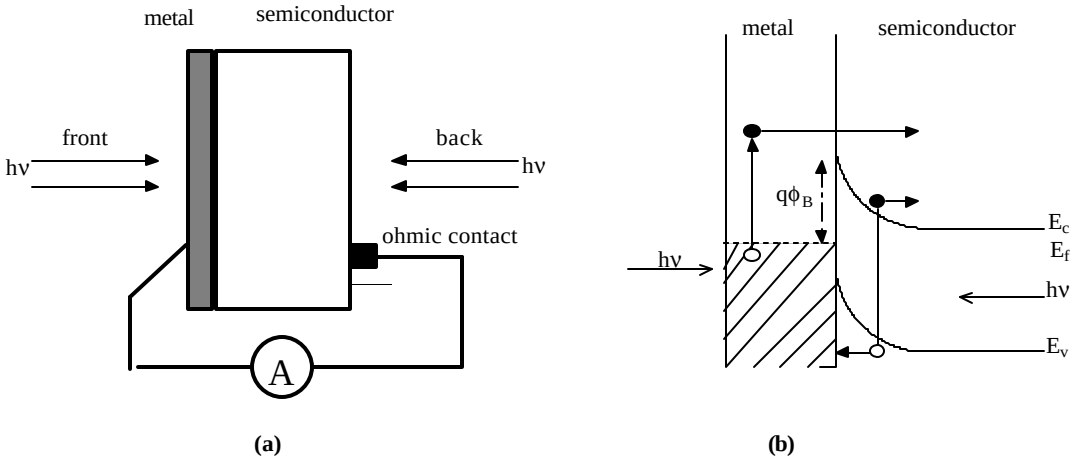


Fig.2.9: (a) Basic set up for photoelectric measurements (b) Shematic representation of photo excitation processes.

For the back illumination, photoelectrons can be generated if $h\nu > q\phi_B$, but when $h\nu > E_g$; the photo excited electron-hole pairs have very small probability of reaching the junction due to the absorption of the incident photons in the semiconductor. However, If the photon energy is larger than the barrier height (i.e $h\nu > q\phi_B$) for the front illumination, light can generate excited electrons in the metal and also can generate electron-hole pairs in the semiconductor if the metal film is thin enough and $h\nu > E_g$. Thus, the photo excited carriers will be swept out by the

built-in electric field and cause a photocurrent. The resulting photocurrent per absorbed photon for ($h\nu - q\phi_B$)>>3kT, as a function of the photon energy, is given by the Fowler theory [87],

$$I_{ph} = B(hn - qf_B)^2 \qquad (2.4.16)$$

where B is a constant of proportionality. When $(I_{ph})^{1/2}$ is plotted as a function of photon energy, a straight line should be obtained whose intercept on the energy axis gives the barrier height. It has been observed that the barrier heights found from the C-V method are generally larger than those obtained by the I-V and the spectral response measurements. This contradiction is associated with the fact that the C-V method gives the flat band barrier height while the other two methods give the zero bias barrier height. The zero bias barrier height is lower than the flat band barrier height value because of the image force barrier lowering. However, this discrepancy cannot be explained only through the image force lowering. It was observed that if the barrier heights obtained from the I-V measurements is multiplied by the diode ideality factor, the results can be found in agreement with those obtained from the C-V measurements. Therefore, the differences in the results can probably be due to the presence of a relatively thick interfacial layer.

2.5 p-n Heterojunctions

2.5.1 Physics of Heterojunctions

In general, a heterojunction is defined as the interface between two different materials with different band gaps. They can be classified as abrupt or graded heterojunctions depending on the distances in which the transition from one material to the other is completed at the interface. If the transition occurs within a few atomic distances the junction is called abrupt, otherwise, is graded. Another classification of the heterojunctions was made in literature by the types of conductivity present on either side of the junction. If the junction is formed with two different materials of the same conductivity type, then the junction is called isotype heterojunction, otherwise is classified as anisotype heterojunction. Various models have been

proposed for current flow in heterojunctions. Gubanov was first to study both isotype and anisotype heterojunctions. Later, Kroemer has suggested that anisotype heterojunctions shown better results of injection efficiencies in comparison to isotype heterojunctions. However, the basic model was introduced by Anderson in 1960. He was also the first to fabricate both types of heterojunctions. His model is a fundamental one that provides a base for the ideal situation in the heterojunctions [89].

In practice current flow in a heterojunction is usually a sum of injection, tunneling and recombination at the interface states. The following discussion indicates the basic diffusion model proposed by Anderson which considers a p-n heterojunction neglecting the effects of dipoles and interface states. This model makes a good approximation to the observed behavior of an ideal p-n heterojunction.

A typical band diagram of two semiconductors with different band gaps and conductivity types when they are not in contact is shown in Fig.2.10. Both semiconductors are at equilibrium and vacuum level is common for both of them.

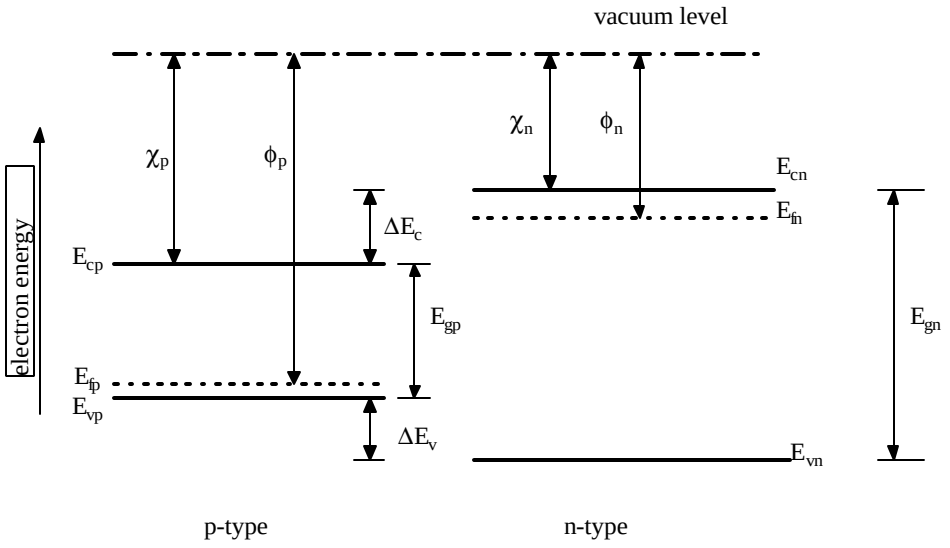


Fig.2.10: Energy band diagrams of p and n-type semiconductors before contact.

As seen in Fig.2.10, the semiconductor with n-type conductivity indicates larger band gap than the one with p-type conductivity. Also, these two type of

semiconductors assumed to have different work functions, electron affinities and dielectric constants. The p-n heterojunction considered in the above figure indicates that electron affinity of the p-type material is greater than that of n-type side. Before contact, the Fermi levels of the p and n sides are at different heights. The Fermi level in the p region is close to the top of the filled band whereas the Fermi level in the n region is close to the bottom of the conduction band. The difference in the conduction band edges is equal to the difference in electron affinities of the two semiconductors and denoted by DE_c. When the two semiconductors brought into contact, the Fermi levels of both sides leveled due to the flow of charge carriers from one to the other as shown in Fig.2.11. At equilibrium, a depletion region is formed on either side of the junction with equal and opposite space charges in magnitude. The total built-in voltage $V_D = (\phi_p - \phi_n)$, is equal to the sum of relative conduction band bendings on both p and n sides which are denoted by V_{Dp} and V_{Dn}, respectively. The solution of the Poisson's equation gives the transition widths extending in p and n regions as the following relations [89],

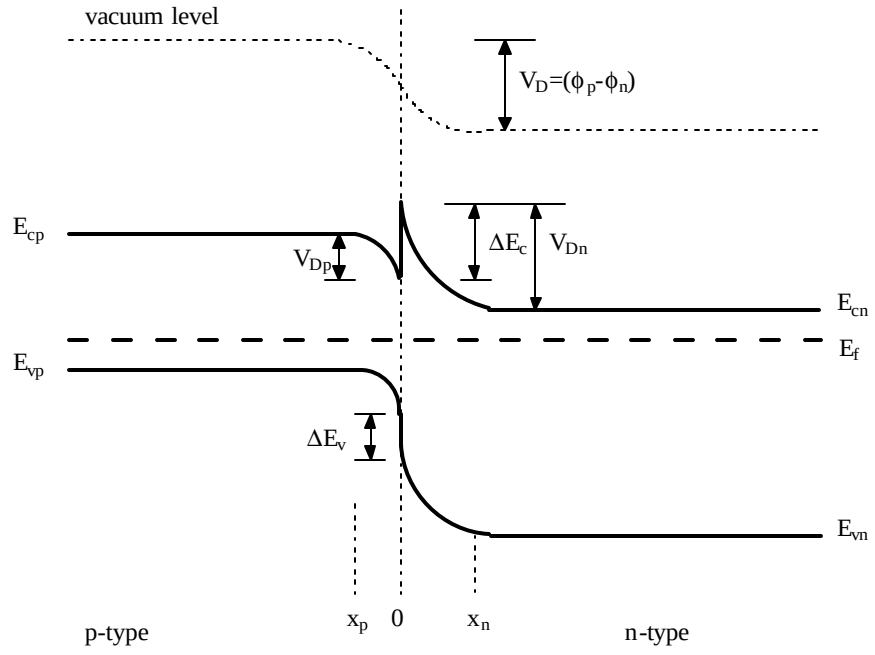


Fig.2.11: Energy band diagram of an abrupt p-n junction at equilibrium.

$$x_p = \left[\frac{2N_a e_p e_n V_D}{qN_d \left(e_p N_a + e_n N_d \right)} \right]^{\frac{1}{2}} \tag{2.5.1}$$

$$x_n = \left[\frac{2N_d e_p e_n V_D}{qN_a \left(e_p N_a + e_n N_d \right)} \right]^{\frac{1}{2}} \tag{2.5.2}$$

where e_p and e_n is the dielectric constants of p and n-type semiconductors, N_a and N_d are the concentrations of acceptors and donors in p and n-type semiconductors, respectively. Since the space charges in these regions are equal and opposite in magnitude, the relation between two relative voltages effective in both semiconductors are given by,

$$\frac{V_{Dp}}{V_{Dn}} = \frac{N_d e_n}{N_a e_p} \tag{2.5.3}$$

which means that most of the potential difference placed in the most lightly doped region providing that the dielectric constants of both sides are equal.

According to the model discussed above, the dominant current carriers are electrons because the barrier for electrons is much smaller than the barrier for holes. When there is no voltage applied to the junction, the barrier for electron flow from the n side to the p side is qV_{Dn}, whereas the barrier for the electron flow from the p side to the n side is given by $(DE_c - qV_{Dp})$, as seen in Fig.2.11. At equilibrium, two oppositely directed electron flows are equal resulting in a zero net current at the junction. Thus, the relation represents the net currents is given by,

$$A_p \exp\left[-\left(\frac{\Delta E_c - qV_{Dp}}{kT} \right) \right] = A_n \exp\left(-\frac{qV_{Dn}}{kT} \right) \tag{2.5.4}$$

where A_p and A_n are constants that depend on the carrier effective masses and doping of the materials.

When an external forward (p side is made positive) voltage V_a is applied on the junction, total built-in potential becomes $(V_D - V_a)$, but V_a is composed of two components as V_p and V_n which are effective in p and n sides of the junction, respectively. Therefore, the band bending in the p side becomes $(V_{Dp} - V_p)$ and in the n side $(V_{Dn} - V_n)$. The Fig.2.12 represents the change in the energy band diagram when the junction is forward biased.

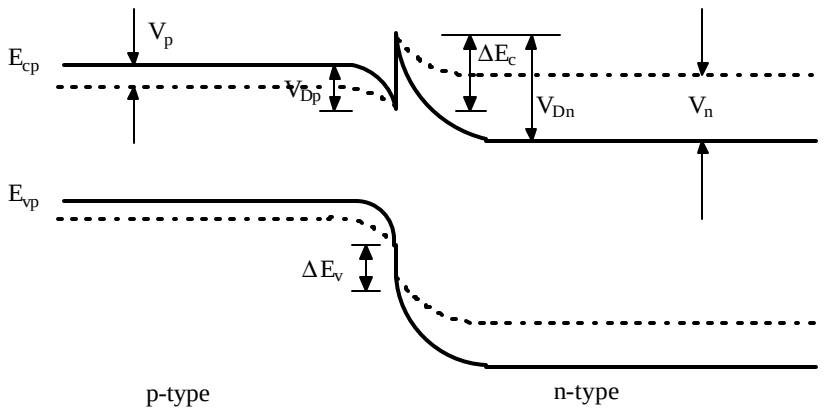


Fig. 2.12: Dashed lines represent the band diagram under forward bias of the junction.

The net flow of electrons can be expressed in terms of the barrier heights changed by the applied voltage,

$$A_p \exp\left[-\left(\frac{\Delta E_c - (qV_{Dp} - Vp)}{kT}\right)\right] = A_n \exp\left(-\frac{q(V_{Dn} - V_n)}{kT}\right) \qquad (2.5.5)$$

Eq. 2.5.4 and Eq.2.5.5 results in the current-voltage expression, for the p-n heterojunctions according to the simplified model which neglects the effects of tunneling and generation-recombination currents at the interface, as the following;

$$J = A\exp\left(-\frac{qV_{Dn}}{kT}\right)\left[\exp\left(\frac{qV_n}{kT}\right) - \exp\left(-\frac{qV_p}{KT}\right)\right] \qquad (2.5.6)$$

and pre-exponential factor A is defined as,

$$A = \mathrm{T}qN_d\left(\frac{D}{t}\right)^{\frac{1}{2}} \qquad (2.5.7)$$

where T is the transmission coefficient for electrons that have enough energy to surmount the barrier, D and t are the diffusion constant and life-time for electrons in p-type semiconductor, respectively. The first exponential term in Eq. 2.5.6 is dominant for the forward bias, and the second term in bracket for the reverse. The current varies exponentially for all bias conditions.

The above current-voltage expression proposed by Anderson [89] has shown deviations from the experimental values found by various workers. The experimental

values are much smaller than the results found from the Anderson's model. The reason for this discrepancy would be the reflection of the incident charge carriers at the junction.

There are other current transport mechanisms that affect the total current flow in p-n heterojunctions which are tunneling and recombination at the interface. These two mechanisms will be discussed briefly here. Detailed discussions about these mechanisms can be found in [78,89,90].

Diffusion-emission models cannot explain the temperature independence of the experimental slopes of current-voltage curves for many heterojunctions. Rediker, Stopek and Ward [91] were proposed the tunneling model in order to explain this behavior. They considered that the electrons have to tunnel through the potential barrier in the n-type wide band gap semiconductor in order to flow from n side to p side or vice versa. According to their model, the tunneling current is obtained as the product of the tunneling probability and the incident electron flux. When the tunneling through the barrier dominates the thermal emission over the barrier, the current-voltage characteristic under forward bias is given by,

$$J = J_s(T)\exp\left(\frac{V_a}{V_0}\right) \tag{2.5.8}$$

where $J_s(T)$ is a weakly increasing function of temperature which is later defined empirically by Newman [92] as proportional to $exp(T/T_0)$. Therefore, the form of the current-voltage expression for tunneling through the barrier becomes,

$$J = J_0 \exp\left(\frac{T}{T_0}\right)\exp\left(\frac{V_a}{V_0}\right) \tag{2.5.9}$$

where J_0, T_0, V_0 are constants. In this model, it is clearly seen that the voltage and temperature is separable variables and temperature dependence is exponential. If the tunneling is predominant at higher energies, then the tunneling current depends on the temperature. However, if the tunneling takes place at the base of the potential barrier, the current is independent of the temperature.

The emission-recombination model was first proposed by Dolega [90]. The model based on fast recombination of holes and electrons at the interface providing that there exists a thin layer at the junction of two materials. This process takes place via thermal emission of electrons and holes over their respective barriers. A very fast

recombination results in no rectification unless the space charge region is wider than this thin layer. The current-voltage relation according to this model can be written in the simplified form given by Van Opdorp is as the following [89],

$$J = J_s\left[\exp\left(\frac{qV_a}{nkT}\right)-1\right] \tag{2.5.10}$$

where

$$J_s = A\exp\left(-\frac{qV_D}{nkT}\right) \tag{2.5.11}$$

where V_D is the diffusion voltage and A represents a function that is weakly temperature dependent and also depends on the effective recombination velocity at the interface. The factor n depends on the ratio of impurities in the semiconductors which forms the heterojunction and ranges in between 1 and 2.

2.5.2 The Effect of Illumination for an Ideal p-n Heterojunction

The photovoltaic converters which convert optical radiation into electrical energy requires no external voltage source since the junction itself turns into a voltage source when it is exposed to radiation of particular spectral distribution. For an ideal p-n junction at equilibrium, the net current flowing through the junction is zero since the hole flow from p to n side is equally balanced with the flow from n to p side. When the junction is reversed biased, the number of majority carriers that are crossing the junction greatly reduced due to the increase in the respective barriers. However, the minority carrier flux remains the same. Thus, the total current saturates at a negative value known as the reverse saturation current and is limited by the rate of thermal generation of electron-hole pairs in the both sides of the junction. On the other hand, when the junction is forward biased, the flux of majority carriers crossing the junction is exponentially increased and dominates the flux of minority carriers by a factor of exp(qV_a/kT). Therefore the current-voltage expression for an ideal p-n heterojunction is given by the following relation,

$$J = J_0\left[\exp\left(\frac{qV_a}{kT}\right)-1\right] \tag{2.5.12}$$

where V_a is the applied voltage and J_0 is the reverse saturation current given by [78],

$$J_0 = qn_i^2\left(\frac{1}{N_D}\left(\frac{D_h}{t_h}\right)^{\frac{1}{2}} + \frac{1}{N_A}\left(\frac{D_e}{t_e}\right)^{\frac{1}{2}}\right) \tag{2.5.13}$$

where n_i is the intrinsic carrier density, N_D and N_A are donor and acceptor concentrations in the two regions. D_h, D_e and τ_h ,τ_e are diffusion constants and life times for holes and electrons, respectively. Reverse saturation current could also be written in terms of diffusion lengths of electrons and holes, L_e and L_h;

$$J_0 = q\left(\frac{e_p L_e}{t_e} + \frac{h_n L_h}{t_h}\right) \tag{2.5.14}$$

where e_p and h_n are the minority carrier concentrations in p and n regions respectively.

When the p-n heterojunction is illuminated, the photons of energies greater than the band gap is absorbed and electrons are excited from the valence band to the conduction band. Therefore illumination results in an increase in the density of electrons in the conduction band and an equal increase in the density of holes in the valence band. The carrier concentrations of electrons and holes both increased beyond their thermal equilibrium values. The excess carriers will tend to recombine unless separated by an internal field which exists in a p-n heterojunction solar cell. The increase in the majority carriers is negligible whereas the increase in the minority carriers increases the reverse saturation current density. Thus the reverse saturation current under illumination is given by,

$$J_0 + J_{ph} = q\left(\frac{(e_p + \Delta_e)L_e}{t_e} + \frac{(h_n + \Delta_h)L_h}{t_h}\right) \tag{2.5.15}$$

where J_{ph} is the photocurrent density and Δ_e and Δ_h are the excess carrier densities due to absorption of photons. In equilibrium the rate of generation of electron-hole pairs is equal to the recombination rate of electrons and holes. Thus, the excess carrier density is given by the following expression,

$$\Delta e = \Delta h = \frac{j\,aQt_e}{hn} = \frac{j\,aQt_h}{hn} \tag{2.5.16}$$

where Q is the quantum efficiency which is defined as the number of electron-hole pairs produced per number of photons absorbed. j is the incident photon radiation

per unit area and a is the absorption coefficient. Thus the photocurrent generated by the illumination is,

$$J_{ph} = \frac{j\, aQq}{hn}\left(L_e + L_h\right) \tag{2.5.17}$$

When the p-n heterojunction is illuminated with no bias applied to the cell, minority carriers from both regions flow to the other side of the junction due to the built-in voltage of the junction. The flow of minority carriers produce a field that reduces the internal barrier formed already at the junction which means an additional forward current of equal magnitude to light generated reverse current is produced. The effect of illumination on the solar cell can be described as if the p-n junction is forward biased. A photovoltaic junction, therefore, exhibits an open circuit voltage V_{oc} and a short circuit current I_{sc} upon illumination. The complete current-voltage relation for an ideal solar cell is given by the following relation [93],

$$-J_{tot} = J_0\left(\exp\frac{qV_a}{kT} - 1\right) - J_{ph} \tag{2.5.18}$$

The equivalent circuit diagram of an ideal p-n junction (i.e solar cell) is shown in Fig.2.13. In this diagram the reverse photocurrent generated in the solar cell is produced by a constant current generator and the ideal diode gives a forward current density due to the forward voltage across the diode.

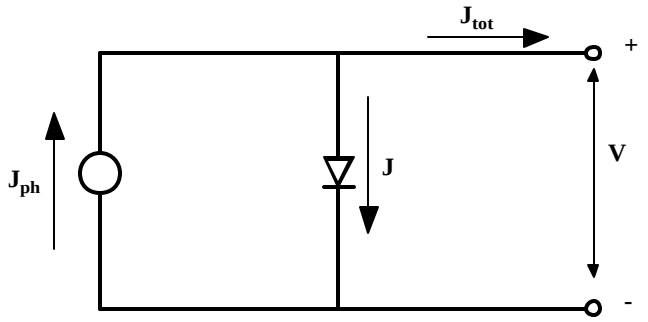


Fig. 2.13: Equivalent circuit diagram for an ideal solar cell.

2.5.3 Photovoltaic Effect and Solar Cells

Basically, photovoltaic conversion occurs through the absorption of light to create electron-hole pairs within the semiconductor. Thus, the photovoltaic effect is the generation of an electric potential by means of photon irradiation. These generated electrons and holes will recombine unless separated by an internal electric field. This internal field can be formed by a junction between two semiconductors with different types of conductivities in the form of homojunctions or heterojunctions or a junction between a metal and a semiconductor in the form of Schottky devices. The absorption of a photon with energy greater or equal to the band gap of the material generates electron-hole pairs at or near the junction. The charge carriers formed in the depletion region are immediately separated by the built-in potential. The holes are swept toward the p-side and the electrons toward the n-side leading to a potential difference across the junction. The internal electric field can therefore be considered as a means to separate carriers, as long as photons or even any other source generates them. It is important that carriers are generated at or near the junction meaning that the product αL_D should be as large as possible, where α is the absorption coefficient and L_D is the diffusion length of the minority carriers.

The most important example of photovoltaic converters is the solar cells. The power obtained from the cell depends on the properties of the material, the incident light, the design and the fabrication techniques. The performance of a solar cell can be examined through the current-voltage characteristics. A typical current-voltage characteristic of an ideal cell is given in Fig.2.14. As seen from the figure that the dark J-V curve is shifted by the amount of photocurrent density. There are five important photovoltaic parameters of a solar cell which are briefly explained as follows [65,94].

A) *Short-circuit current* is defined as the current that flows through the junction under illumination without an external bias is applied. As defined in previous section, short-circuit current is equal to the light generated current in the ideal case, $J_{sc}=-J_{ph}$. It increases with increase in the minority carrier lifetimes and the diffusion lengths. As Eq.2.5.17 indicates, J_{sc} is also directly proportional to the

intensity of the illumination and the material parameters that control the collection distance.

B) *The open-circuit voltage* is defined as the voltage developed across the cell when there is no external current through the device in which case the separated electrons and holes remain in the solar cell until they recombine. The open-circuit voltage is found from Eq.2.5.18 when the net current through the device is set to zero for an ideal cell.

$$V_{oc} = \frac{kT}{q} \ln\left(1 + \frac{J_{sc}}{J_0}\right) \tag{2.5.19}$$

Open-circuit voltage of a solar cell increases with i) a decrease in the temperature of the cell ii) an increase in photocurrent or the short-circuit current iii) an increase in the band gap of the material iv) a decrease in the resistivity of the material v) an increase in the minority carrier life time or diffusion lengths $(L = (Dt)^{1/2})$ in the material. As indicated in the Fig.2.14, at both I_{sc} and V_{oc} values, the solar cell delivers no power to the load.

C) *Power Output* is obtained from the cell at any point between J_{sc} and V_{oc} (at which no power obtained from the cell) is given by [95],

$$P = J_{tot}V = \left[J_0 \left[\exp\left(\frac{qV}{kT} - 1\right)\right] - J_{sc} \right] V \tag{2.5.20}$$

The maximum power that can be obtained from the cell can be found by the condition $\frac{\partial P}{\partial V} = 0$. Thus, at the maximum power point (M.P.P.), the current density can be found as the following expression,

$$J_m = \frac{\left(\frac{qV_m}{kT}\right)(J_{sc} + J_0)}{\left(1 + \frac{qV_m}{kT}\right)} \tag{2.5.21}$$

the voltage V_m at the M.P.P can also be calculated, by using Eq.2.5.19, from the following relation;

$$\exp\left(\frac{qV_{oc}}{kT}\right) = \exp\left(\frac{qV_m}{kT}\right)\left(1 + \frac{qV_m}{kT}\right) \tag{2.5.22}$$

Therefore, the maximum power output $P_m=V_mJ_m$ of an ideal solar cell is found as discussed above.

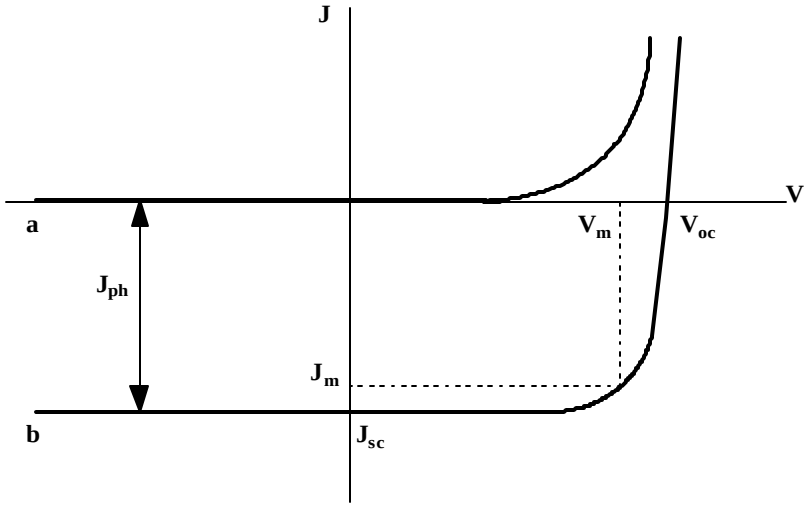


Fig. 2.14: Current-voltage curve for an ideal solar cell a) dark and b) illuminated.

D) *Fill Factor* is a parameter that relates the maximum power a cell produce to the product of $V_{oc}J_{sc}$ which measures the squareness of the *J-V* curve. The fill factor, FF, is thus defined as [95];

$$FF = \frac{J_m V_m}{J_{sc} V_{oc}} = \frac{V_m}{V_{oc}} \left[1 - \frac{\exp\left(\frac{qV_m}{kT}\right) - 1}{\exp\left(\frac{qV_{oc}}{kT}\right) - 1} \right] \tag{2.5.23}$$

The FF increases with increasing values of open-circuit voltage and with decreasing values of temperature. Higher band gap materials results in a higher FF because of their higher open-circuit voltages.

E) *Efficiency* is the ratio of maximum power produced by the solar cell to the power incident due the solar irradiation. The efficiency (h) of a solar cell in converting the energy of light into electrical energy is given by,

$$h = \frac{P_m}{P_{in}} = \frac{V_{oc} J_{sc} (FF)}{P_{in}} \tag{2.5.24}$$

where P_{in} is the power incident on the device. The power conversion efficiency of a solar cell depends on the magnitude of the photo-generated current and the ratio J_{ph}/J_o. In order to obtain maximum efficiency both of these values should be as large as possible. Notice that all the parameters of a solar cell can be determined by reverse saturation and photo-generated current densities.

All the parameters that define a solar cell are given above assuming the cell is an ideal one. The basic solar cell equation derived for the ideal cell was given in Eq.2.5.20. However, this equation does not represent the actual solar cell *J-V* characteristics with sufficient accuracy because the effects of series and shunt resistances were not taken into consideration for the ideal cell. The more realistic model that also considers series and shunt resistance effects is given by the following relation [93],

$$-J_{tot} = J_o\left[\exp\left(\frac{q(V+JR_s)}{kT}\right)-1\right]+\frac{V}{R_{sh}}-J_{ph} \qquad (2.5.25)$$

where R_s is the series and R_{sh} is the shunt resistance. The equivalent circuit of the

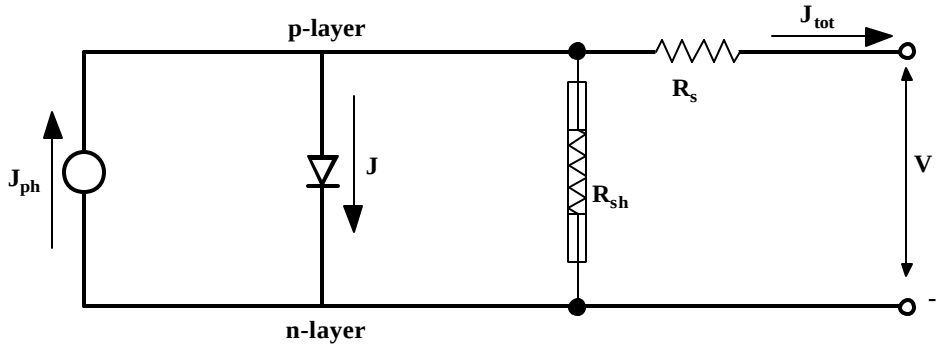


Fig.2.15: Equivalent circuit diagram of a more realistic solar cell.

realistic solar cell is shown in Fig.2.15. The fill factor of a solar cell can be degraded by high series resistance and low shunt resistance. In an ideal solar cell series resistance is zero and shunt resistance is infinity. However, this is not achieved in practical solar cells for which the efficiencies are much smaller than the theoretical values. The shunt resistance arises due to various leakage paths such as crystal defects or surface leakage along the edges of the cell. Series resistance is related with the resistance of the top and the base materials and the resistance of top and the

bottom contacts. The effect of the series resistance is more dominant at high level of illumination whereas poor shunt resistance is more pronounced at low illumination of the cell. An increase in R_s limits the J_{sc} but does not affect V_{oc} . As the shunt resistance decreases, the V_{oc} is reduced. Reflection loss from the top layer is also a factor that lowers the efficiency of a cell. These losses can be minimized by proper design of the cell and by suitable choice of the materials and contacts.

2.5.4 Junction Capacitance for p-n Heterojunctions

The capacitance-voltage relation for p-n heterojunctions will be given in this section with abrupt junction approximation. When the impurity concentration in a device changes abruptly from acceptor impurities to donor impurities one obtains an abrupt junction. In equilibrium, the electric field in the neutral regions of the semiconductors must be zero, that is the total negative charge per unit area in the p side must be exactly equal to the total positive charge per unit area in the n side as indicated in the following relation,

$$N_D x_n = N_A x_p \tag{2.5.26}$$

Thus when the equilibrium is attained, space charge regions on either side are formed. The capacitance-voltage relation for n-p junctions can be derived by assuming that the heterojunction is a combination of two series Schottky diodes. Applying the Poisson equation with the assumption that the junction is abrupt and that the doping is uniform in both materials the capacitance per unit area as a function of voltage neglecting the interface states is given by [96],

$$C = \left[\frac{q e_p e_n N_A N_D}{2(e_n N_D + e_p N_A)(V_{bi} - V_a)} \right]^{\frac{1}{2}} \tag{2.5.27}$$

where N_D and N_A are the donor and acceptor concentrations, e_n and e_p are the dielectric constants of n and p-type semiconductors, respectively. It can be seen from this relation that a plot of C^{-2} *vs* V_a is linear and its extrapolated intercept on the voltage axis gives the built-in junction potential. If the doping concentration of one side is known, than the doping concentration of the other side can be deduced from the slope of the C^{-2} *vs* V_a plot. Thus the measurement of the junction capacitance as

a function of applied voltage is a reliable tool for the analysis of the depletion region potential and the charge distribution in a heterojunction.

The deviation from the ideal C-V behavior expressed in Eq.2.5. 27 is explained through the existence of interface states and the trap levels in the band gap. The capacitance of a heterojunction diode is often observed to decrease as the measurement frequency is increased. This effect in homojunctions is caused by the inability of deep impurity centers in the depletion region to follow the increasing frequency. However, for the heterojunctions the frequency dependence of capacitance was explained through the relaxation time constants of the interface states.

2.5.5 The Spectral Response of p-n Heterojunctions

Optoelectronic properties of heterojunctions can be divided into two groups, one which deals with generation of photocurrents due to absorption of photons in an incident light whereas the other deals with emission of photons resulting from electronic excitation in heterojunctions. The absorption of photons in a semiconductor can occur via different ways depending on the wavelengths of the incident photons. Two important absorption processes which strongly influence the photoelectric properties of heterojunctions are; i) the creation of free electrons or holes due to photoexcitation of an impurity (or interface state) and ii) The creation of free electron-hole pairs due to band-to-band excitations. The photocurrent in heterojunctions results from the created free carriers by these processes at or within a diffusion length from the interface which is formed by two semiconductors with different type of conductivities. The spectral response of a solar cell can be defined as the short circuit current as a function of the incident light. More precisely, the photocurrent collected at each wavelength relative to the number of photons incident on the surface at that wavelength determines the photoelectric response of the device.

The expression defining the spectral response of a heterojunction can be obtained by considering the one-dimensional geometry shown in Fig.2.16. In the figure, d is the junction depth, and L_e and L_h are the minority carrier diffusion lengths in the p and n side of the junction respectively.

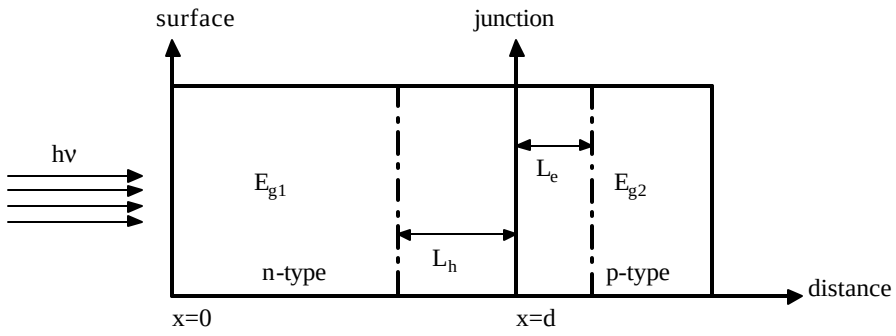


Fig. 2.16: A schematic representation of a p-n heterojunction under illumination ($E_{g1}>E_{g2}$).

For the photons whose energies are greater than the band gap, the density of photons in the semiconductor changes as the following relation [65],

$$\Phi_{ph} = \Phi_0 \exp(-ax) \tag{2.5.28}$$

where Φ_{ph} is the number of photons per sec-cm^2 and a is the absorption coefficient which is a function of the wavelength. The electron-hole generation rate due to the incoming photons is then given by,

$$G(x) = \Phi_0 a \exp(-ax) \tag{2.5.29}$$

Due to the creation of electron-hole pairs in both sides, the total number of carriers crossing the p-n junction is given by,

$$N_T \approx \frac{\Phi_0 a}{\left(a - \frac{1}{L_h}\right)}\left[\exp\left(-\frac{d}{L_h}\right) - \exp(-ad)\right] + \frac{\Phi_0 a \exp(-ad)}{\left(a + \frac{1}{L_e}\right)} \tag{2.5.30}$$

It is assumed that the electric field in the depletion region is sufficient such that the photogenerated carriers are moving out of the region before recombination occurs. The current passing through the junction is constant at equilibrium, thus the total number of carriers crossing the junction is directly proportional to the photocurrent. The energy of an individual photon depends on its frequency which leads to the fact that the photon density is proportional to the wavelength of the incident light. Thus, the short-circuit current per unit wavelength is given by,

$$\frac{dI_{sc}(l)}{dl} \approx a\,l\left[\frac{L_h}{1-aL_h}\left(\exp(-ad)-\exp(-d/L_h)\right)+\frac{L_e\exp(-ad)}{1+aL_e}\right] \qquad (2.5.31)$$

with the assumptions of aL_e and $aL_h<<1$, and $d/L_h>>1$, this equation is simplified to the following relation,

$$\frac{dI_{sc}(l)}{dl} \approx a\,l\left[(L_e+L_h)\exp(-ad)\right] \qquad (2.5.32)$$

High surface recombination velocity results in a reduction of the lifetime of carriers near the surface which also reduces the response of the cell to short wavelengths of incident light. In order to increase the short wavelength response the junction should be placed closer to the surface, since $1/a$ is small for short wavelengths. By analogy, as the depth of the junction increases, response to long wavelengths also increases.

CHAPTER 3

EXPERIMENTAL TECHNIQUES

3.1 The Preparation of InSe and CdS Thin Films

In order to study the film and device properties, InSe and CdS thin films were deposited by thermal evaporation technique onto soda lime and tin-oxide coated glass substrates using the prepared copper masks shown in Fig.3.1a-b. Two different mask shapes were prepared to investigate the structural, optical and electrical properties of the films. Fig.3.1b shows the mask shape for the structural studies of the films and the Fig.3.1a shows the six-arm bridge (Hall bar shape) geometry mask suitable for the electrical and optical measurements of the films. The masks used for the metallic contact deposition for the hall-bar and point contact geometries are shown in Fig.3.2a-b. Prior to deposition, substrates should be cleaned in order to avoid dirtiness between the film and the substrate so that evaporated atoms stick well on the substrate surface. The procedure of substrate cleaning is briefly explained as follows.

(a) **(b)**

Fig.3.1: a) Six arm-bridge (Hall bar), and b) Mask geometry for structural measurements of film studies.

(a) **(b)**

Fig.3.2: Metal contact geometries for a) Hall bar shape, and b) Point contacts with radius of 0.5 mm for device fabrication.

The glass substrates (20x23 mm^2) were first cleaned thoroughly with a detergent solution to get rid of the gross dirt exist on the surface. Then this process was repeated at 70°C in a separate cup. In order to clean the detergent solution, the glass slide was rinsed in a distilled water filled cup by using an ultrasonic cleaner. To clean out the organic materials which may still exist on the surface, a boiling solution of diluted H_2O_2 30% was used so that the organic dirt's were converted to water soluble compounds. As a final step of the substrate cleaning procedure, the substrate was rinsed in a separate cup filled with hot water in the ultrasonic cleaner. The cleaned substrates were kept in methanol, and prior to deposition they were dried by blowing nitrogen gas.

To check the cleanliness of the substrates, "wettability test" was applied such that when the substrate were hold in a vertical position, formation of film of water on the surface was observed which indicates that the surface was free of any dirty spots.

3.1.1 The Evaporation Cycle of InSe Thin Films

a) The evaporation system: The deposition of InSe thin films using thermal evaporation method carried out in a Leybold Univex 300 vacuum system. The lowest pressure attainable with this system was around 10^{-6} Torr which was obtained through a complete turbo-molecular pumping system equipped with pirani and penning gauges. The system composed of a bell-jar vacuum chamber which was placed on a base plate with feedthroughs and power control units of the source and substrate as shown in Fig.3.3.

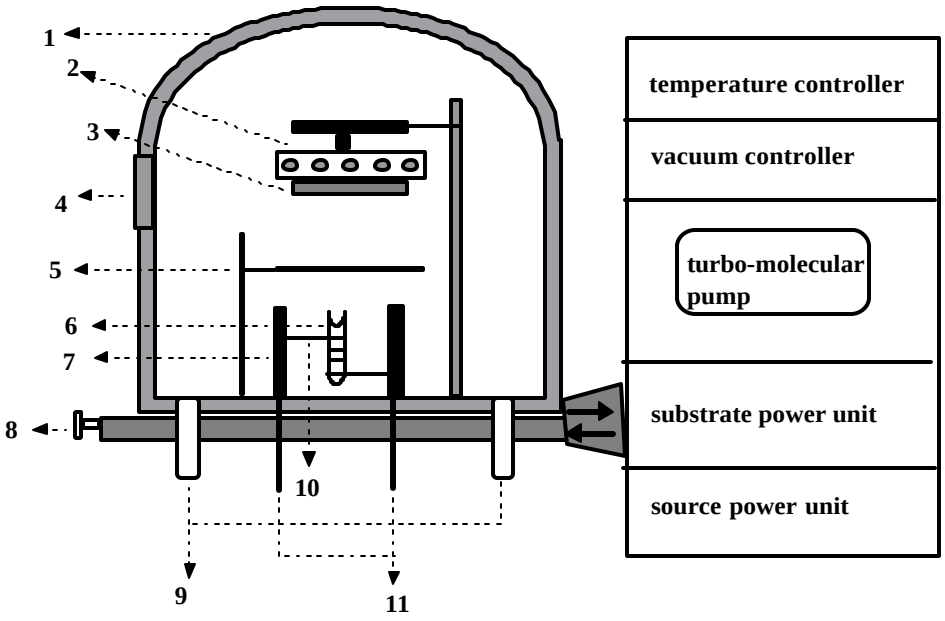


Fig.3.3: The vacuum evaporation system for InSe thin film deposition. 1. Bell-jar, 2. Substrate heater, 3. Substrate holder, 4. Window, 5. Shutter, 6. Source boat, 7. Feedthrough, 8. Air valve, 9. Pirani and Penning gauges, 10. Source heater, 11. Filament current wires.

Source unit is a quartz ampoule in which the source material was heated, wound with molybdenum wire all of which was placed into a ceramic shielder in order to localize the source temperature. The source was heated by adjusting the current passing through the molybdenum wire with the source power unit of the system. The source temperature during the growth process was measured with a Pt/Pt-13%Rh thermocouple placed within the quartz ampoule, and controlled by an Elimko-4000 temperature controller.

The substrate heater was made of an aluminum block with chrome-nickel heating wires insulated by quartz tubes. The substrates and the masks were placed in the copper substrate holder which was mounted about 12 cm above the source. The substrate temperature was measured with a copper-constantan thermocouple which is in contact with the aluminum block. Elimko-4000 temperature controller was used to control the temperature of the substrates, and a shutter that was placed just above the source controls the start and the stop of the deposition process.

b) The evaporation process: 1gr of 99.99% pure In_2Se_3 single crystal powder was used as the source material. After the substrates and the masks were placed in the holder, the system was turned on to evacuate. When the vacuum of about 10^{-6} Torr was reached, the source was started to heat up around 700-800 ^oC at which point the source starts melting. For the hot substrate deposition, substrate temperature was kept at around 100 ^oC. For the cold substrate depositions, substrate was not heated intentionally but with the effect of the source temperature, the substrate temperature reached at about 30 ^oC. The deposition time which was controlled by the shutter was in between 8-16 minutes to obtain films with different thicknesses. The deposition rates for different cycles were observed to be in the range of 0.1-0.3 μm/min.

Cd-doped Inse thin films were obtained by the same procedure explained above. In this process, however, cadmium was placed in a second quartz crucible which was mounted at 2 cm away from the InSe source. For the doped films, 0.1 gr. of cadmium was used and heated up to around 320 ^oC simultaneously with the InSe source. The shutter then opened at the same time for both sources and deposition stopped simultaneously as well.

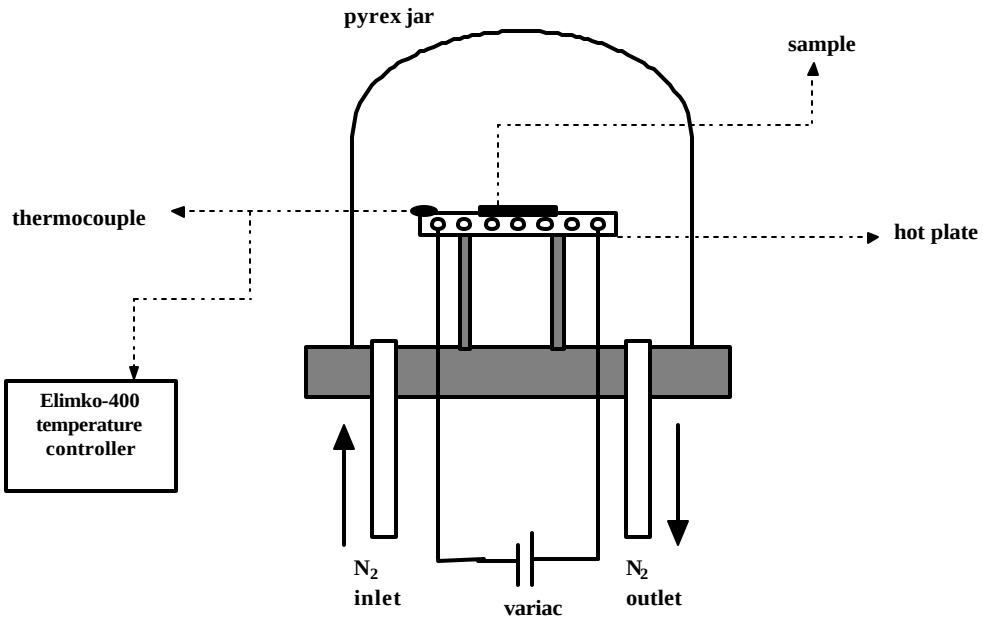


Fig.3.4: The hot plate fixture for annealing process.

As a post-deposition treatment some of the films were annealed at temperatures ranging in 100-150 ^{o}C for various times under nitrogen flow using the hot plate shown in Fig.3.4. The hot plate is composed of chrome-nickel heating wires placed in insulating ceramic tubes sandwiched between two ceramic plates. The temperature of the plate was measured with a chromel-alumel thermocouple and monitored by Elimko-4000 temperature controller. During the annealing process, continuous flow of N_2 was supplied in the covering pyrex glass jar.

3.1.2. The Evaporation Cycle of CdS Thin Films

a) The evaporation system: The CdS thin films were deposited by thermal evaporation technique in a Varian NCR 836 oil diffusion vacuum system. The bell jar assembly is shown in Fig.3.5. The lowest pressure obtainable with the system is around 10^{-7} Torr. A quartz crucible wound with molybdenum wire was used to evaporate the source. The tube was shielded with a molybdenum cylinder to localize the heat in the source. Pt/Pt-13%Rh thermocouple were placed in contact with the powder to measure the temperature of the source and controlled by Elimko-4000 temperature controller. The substrate heater was made of an aluminum block containing chrome-nickel heating wires insulated by pyrex glass tubes inside the block. The substrate temperature was measured by a copper-constantan thermocouple and controlled by Elimko-4000 temperature controller. A stainless steel shutter was placed between the source and the substrates to control the start and the stop of the deposition.

b) The evaporation process: The CdS powder which was 99.99% pure and had a particle size around 0.3 mm was placed in the quartz crucible. Some quartz wool was also placed on top of the powder in order to reduce the splattering of the source material and thermocouple was made sure to be in contact with the source. Then, the system was started to evacuate first by the mechanical pump then by the oil diffusion pump. When the vacuum of around 10^{-6} Torr was obtained, the source and the substrates were started to heat up gradually to the required temperature values. The temperature of the substrate was kept around 200 ^{o}C until the source heated up to the melting temperature of the CdS which was around 700 ^{o}C. The deposition time

was about 15-20 minutes. The approximate deposition rates for different deposition cycles were in the range of 0.01-0.1 μm/min.

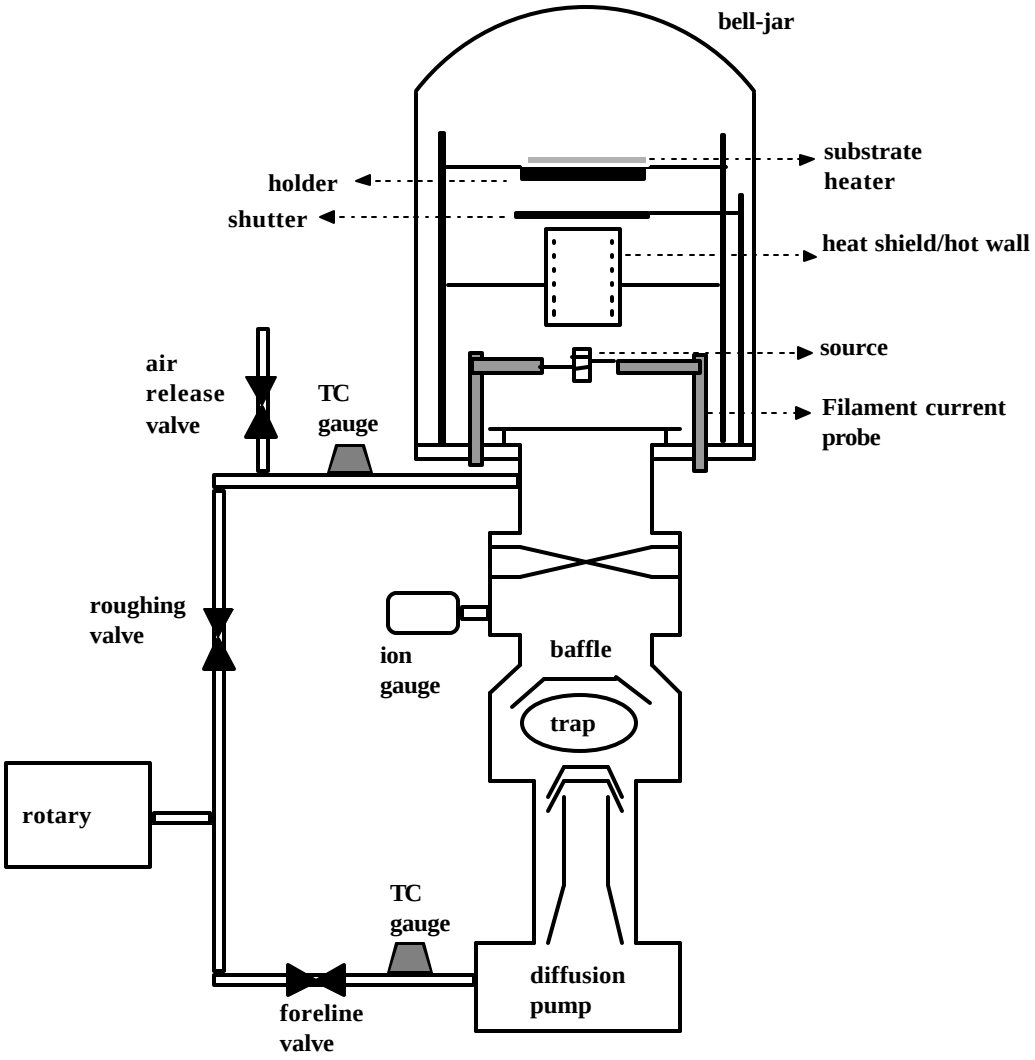


Fig.3.5: Schematic diagram of the evaporation system of CdS thin films.

3.1.3 The Metallic Evaporation System

Metallic evaporation was required to achieve electrical contacts to both thin films and devices produced in this work. Indium ohmic contacts were evaporated on to InSe and CdS Hall bar shaped thin films to carry out the electrical and optical

measurements. For the Schottky diodes and solar cells, various metals such as Ag, Au, In, Al and C contacts were achieved onto TO/InSe and TO/CdS/InSe structures, in order to investigate the device properties of these junctions.

The metallic evaporations were carried out by using a Nanotech evaporator system, the bell-jar assembly of which is shown in Fig.3.6. The lowest attainable pressure with this system is 10^{-6} Torr through a diffusion pump. For the evaporation, the source metal was placed in a molybdenum boat which was heated by a manually controlled variac. The substrates and the appropriate masks were placed in a copper holder that was mounted around 10 cm above the source boat.

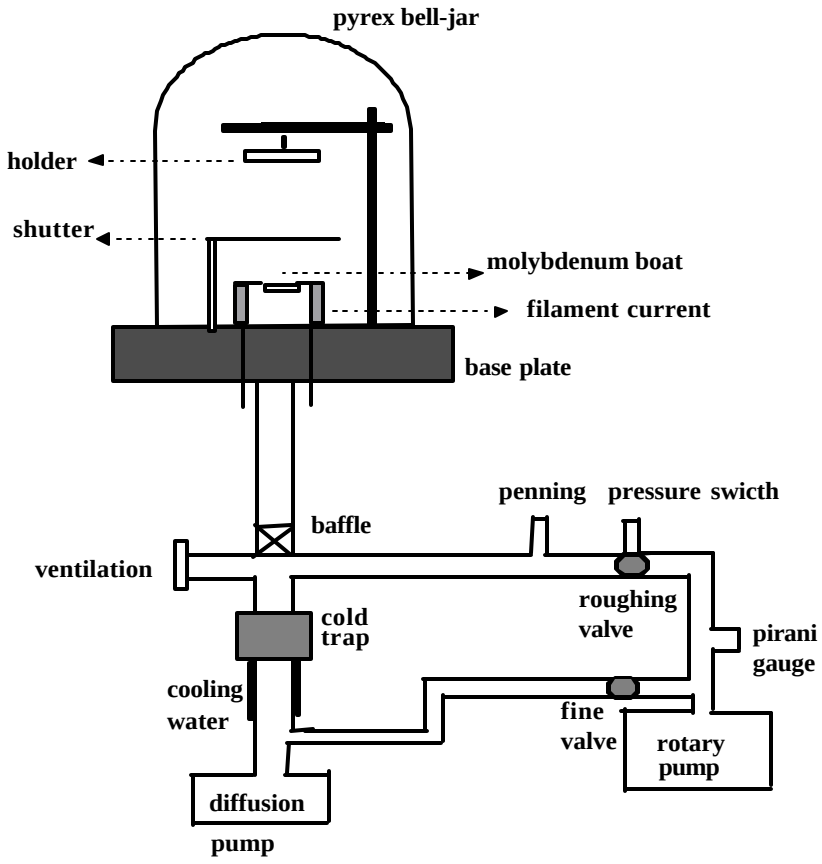


Fig.3.6: The schematic view of metallic evaporation system.

3.2 Electrical Measurements

3.2.1 Resistivity Measurements

The room temperature dark resistivity of the InSe and CdS thin films were measured with a standard dc technique on the hall-bar shaped films. The reliability of these measurements strongly depends on the ohmic behavior of the metal contacts such that the contacts should not add any parasitic impedance to the structure and do not change the equilibrium carrier densities within the film. The ohmicity of the metal contacts was checked by the linear variations of the I-V characteristics which were independent of the reversal of the applied bias in working current range. In Fig.3.7, the circuit diagram of the experimental set up for the resistivity measurements of the hall-bar (six-arm bridge) type samples is given. A constant current was applied between the contacts 1-5 by using a Keithley 220 programmable constant current source which can supply currents in the range between 0.1 nA to 10 mA with a compliance voltage of up to 100V. The working current range was adjusted for different samples in accordance with the total resistances of each sample. The voltage drops across the side contacts 2-4 and 6-8 were measured by using a Keithley 614 and 619 electrometers. The electrical resistivity of the films can be expressed by the following relation

$$r = \frac{V}{I}\frac{wt}{L} \tag{3.2.1}$$

where t is the thickness, w is the width and L is the spacing between the contacts across which the voltage is measured. For determining the total resistivity, the average value of the two voltage drops V_{24} ad V_{68} was used to plot the I-V characteristic from which the inverse of the slope of the linear line yields the V/I value.

The electrode spacing and the dimensions of the film was measured by using a traveling microscope. The total length, width and spacing between the adjacent probes were found to be 1.15±0.01 cm, 0.22±0.01 cm and 0.48±0.01 cm, respectively. The thicknesses of the films were measured for InSe and CdS films with a Dektak 3030ST profilometer whose properties will be given in section (3.4).

The thicknesses for InSe films were found to be in the range of 0.22-3.45 μm, while for the CdS films it was found to be in the range of 0.34-2.64 μm. The alignment of the contacts and possibility of damaged contacts were checked by comparing voltage drops across different contact pairs during the measurement.

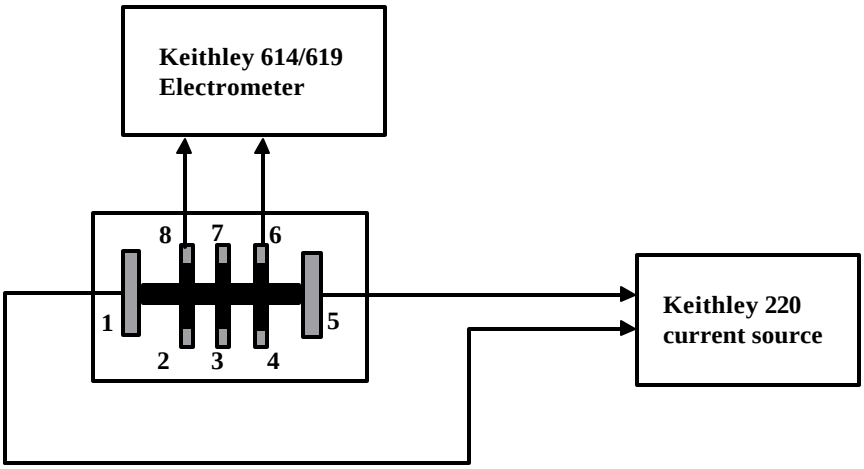


Fig.3.7: The electrical measurement circuit for hall-bar shaped thin films.

3.2.2 Temperature Dependent Conductivity and Hall Effect Measurements

The investigations of the electrical properties of deposited InSe and CdS thin films were also studied through temperature dependent conductivity and Hall effect measurements in the temperature range of 100-430 K by means of a Janis Liquid Nitrogen VPF Series Cryostat. After mounting the sample onto the cold head, the system was pumped down to 10^{-3} Torr by using an Ulvac Rotary pump. Cooling of the cryostat was achieved by adding liquid nitrogen to the system and the temperature was measured with a GaAlAs diode sensor and controlled by a LakeShore-331 temperature controller. When the desired temperature and pressure conditions were met, conductivity measurement was carried out as the temperature gradually increased by 10 K increments with a Keithley 220 programmable constant current source and a Keithley 619 electrometer. At each temperature point, the

system was allowed to stabilize around that temperature in order for the sample to reach a thermal equilibrium.

The Hall effect measurements were carried out by the same system described above except a constant magnetic field of 0.97 T applied parallel to the c-axis (perpendicular to the film surface) of the films using Walker Magnion model FFC-4D magnet. The schematic representation of the Hall effect measurements is given in Fig.3.8. The applicability of the dc method is limited for samples for which the resistance across the sample is in the order of 10^3-10^9 Ω. AC method is usually used for the lower-resistive samples. Constant current was applied to the sample with a Keithley 220 constant current source through the contacts 1-5 and the hall voltage produced by the magnetic field was measured between the side contacts 3 and 7 with a Keithley 619 electrometer, for the Hall-bar film represented in Fig.3.7. The Hall voltage was measured by series of readings which includes four different combinations of current and the magnetic field directions to reduce the error in the Hall voltage value that was produced due to several effects which can be briefly defined as follows;

- The thermoelectric voltage V_T that was generated due to the thermal gradient between the contacts.

- A transverse temperature dependence called Ettingshausen effect which generates another erroneous potential V_E .

- An additional potential drop V_{RL} between the contacts due to Righ-Leduc effect which also results from the temperature differences across the sample.

- Nernst potential difference V_N caused by the difference between the contact and the sample material.

- The potential drop V_M caused by the imperfect alignment of the contacts in the absence of the applied magnetic field.

Thus, making a series of readings for the Hall voltage with four different combinations of current and magnetic field directions reduces these errors in the Hall voltage down to a reasonable value. These combinations of readings for the directions of magnetic field and current were as the following,

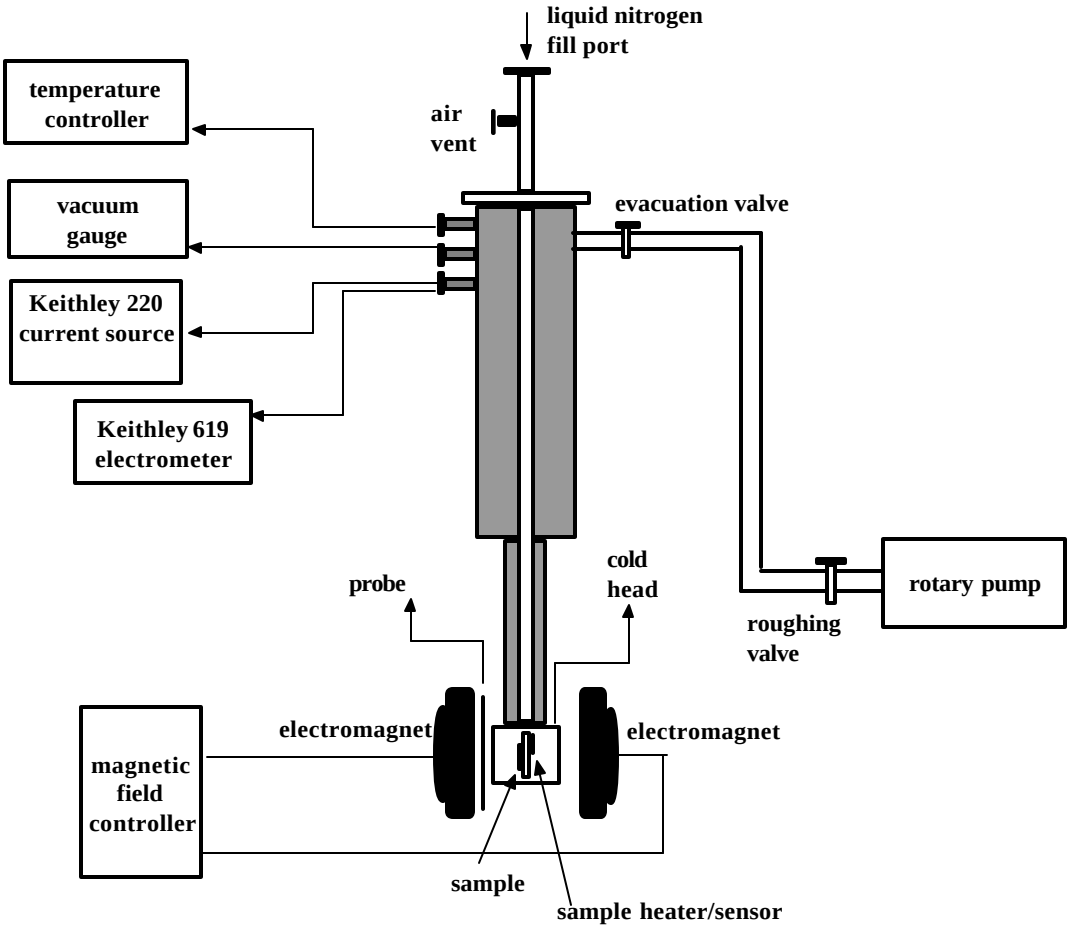


Fig.3.8: The schematic diagram of the Hall effect measurement set up.

(+B,+I) $V_1=V_H+V_E+V_N+V_{RL}+V_M+V_T$

(-B, +I) $V_2= -V_H-V_E-V_N-V_{RL}+V_M+V_T$

(+B, -I) $V_3= -V_H-V_E+V_N+V_{RL}-V_M+V_T$

(-B, -I) $V_4=V_H+V_E-V_N-V_{RL}-V_M+V_T$

The Hall voltage V_H can be determined as taking all of these separate measurements into consideration and given by,

$$V_H+V_E = (V_1+V_4-V_2-V_3)/4 \qquad (3.2.2)$$

where V_E is the Ettingshausen voltage effect which is too small so that it can be ignored. The theoretical value of the Hall voltage as discussed in section (2.3.1) given by the Eq.(2.3.6). As seen from the equation, the plot of IB versus V_H curve

yields the slope of t/R_H from which the Hall coefficient can be calculated. Therefore, Hall effect measurements give information about the hole concentration and carrier mobility values for the thin films under investigation.

3.2.3 Current-Voltage Measurements of the Devices

Schottky structures were fabricated by depositing InSe thin films with thermal evaporation technique explained in section (3.1.1) onto TO coated glass substrates where TO used as the back contact in the structure. The metal point contacts, with area of 7.85×10^{-3} cm^{-2}, such as Ag, Au, Al and In were achieved as described in section (3.1.3) for the characterization of Schottky barriers formed between the metals and the InSe thin film. The n-CdS/p-InSe heterojunction structures were fabricated with a successive evaporation of n-CdS films onto TO coated glass substrates as explained in section (3.1.2) and p-InSe films onto TO/n-CdS structures. Subsequently, the upper metal contacts Au, Ag, In and Al were then evaporated onto the p-InSe films to study the electrical properties of the solar cell structures. Carbon cold contacts were also applied to both structures by painting liquid colloidal graphite onto the p-InSe films. The Fig.3.9a-b represents the Schottky diode and n-CdS/p-InSe hetero structures fabricated in this work.

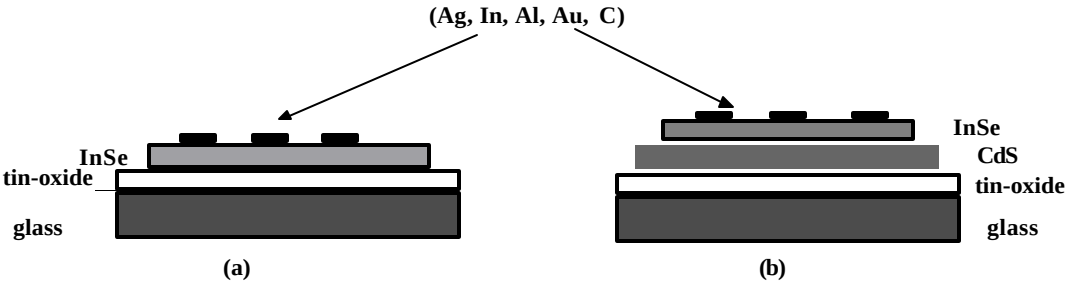


Fig.3.9: (a) Schottky diode and (b) Solar cell structures.

In order to investigate the rectifying behaviors of the devices dark current-voltage characteristics were measured at room temperature. A constant current was applied between the back and the upper contacts of the devices with a Keithley 220 current

source and the voltage drop across the device was measured with a Keithley 619 electrometer. The forward bias for the Schottky diodes were obtained by connecting the positive probe to the tin-oxide so that the InSe thin film was made positive with respect to the upper metal contacts. The current-voltage characteristics of the n-p heterojunction was studied by the same method at room temperature, however, forward bias for this structure was achieved by connecting the positive probe of the current source to the upper ohmic contacts in order to make the p-InSe thin film positive with respect to the n-CdS thin film.

The temperature dependent dark current-voltage characteristics of the devices were investigated with the cryostat system shown in Fig.3.8 given in section (3.2.2). Through the temperature dependent I-V measurements, the current transport mechanisms were studied in the temperature range of 100-430 K. All electrical connections were made via an electrical feedthrough mounted on the sample holder. The temperature of the sample which was placed in the cold head was measured with a GaAlAs diode sensor and controlled by a LakeShore-331 temperature controller.

The Space-Charge-Limited Currents (SCLC) measurement were also carried out in the temperature range of 200-320 K to investigate whether SCLC mechanism was dominating the current transport at higher voltage biases of the Schottky diode structure. Furthermore, the measurement yielded information on the trap levels and the trap densities of InSe thin films. A Schottky structure, which was sandwiched between to ohmic contacts, was used for the SCLC measurements. A voltage in the range of 0.1-60 V was applied between the contacts of the diode, shown in Fig.3.9a, by means of a Hickok Model 5056 power supply and a Keithley 619 electrometer was used to measure the current passing across the diode perpendicular to the layers.

I-V characteristics of the Schottky and heterojunction structures under illumination were measured by using a solar simulator built-in our laboratory shown in Fig.3.10. The light source was a 100 W halogen lamp with a parabolic reflector housing made of aluminum plate and the height of the lamp was adjustable. The intensity of the light can be controlled either by a manually operated variac or by changing the height of the light source. The illumination intensity of the lamp on the surface of the sample measured by using a 180^{o} pyronometer which was placed at the same height with the sample. A leveled metal frame placed between the light source

and the sample that contained a 2 cm deep tray of water that prevents the sample from being heated. Also, the light was filtered through the water like air filtering in the real sun spectrum. Underneath the tray, an adjustable sample holder was mounted which allows back or front illumination of the devices.

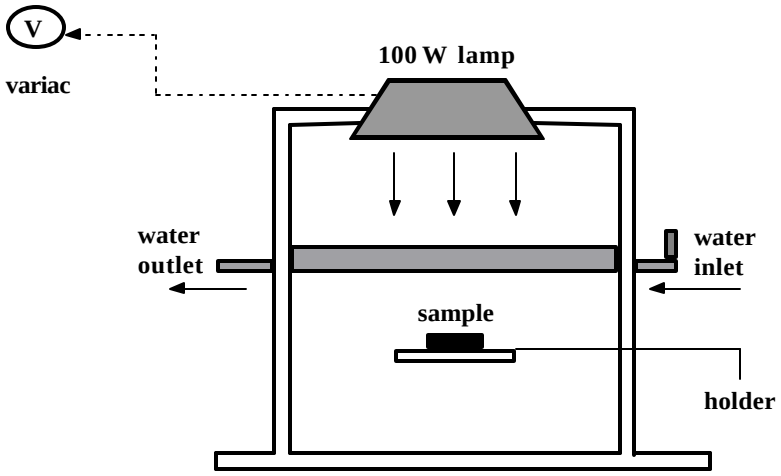


Fig. 3.10: The schematic diagram of the solar simulator for front and back illumination.

The illuminated current-voltage characteristics of the devices were approximately obtained under simulated AM1 condition which was defined as surface illumination intensity of 100 mW/cm^2.

3.2.4 Capacitance-Voltage Measurements

The capacitance-voltage measurements have been used as a useful tool to study the junction region structure and the effects due to the interface states and deep levels. The C-V characteristics of a metal-semiconductor or a heterojunction device yields information on the barrier height of the junction and impurity concentrations of the materials. The measurements were carried out by using a HP 4192A LF Impedance Analyzer which was controlled by a personal computer with the necessary software to measure capacitance and conductance. The instrument uses a linear voltage ramp to sweep the voltage over the bias range from accumulation to

inversion or vice versa at a specified bias ramp rate. A small ac voltage is superimposed on the ramp voltage to measure the differential capacitance change in the depletion region. The sweep capability of the built-in frequency synthesizer and dc bias source allows quick and accurate measurements. The built-in frequency synthesizer can be set to measuring frequency within the range from 5Hz-13 MHz with maximum resolution of 1 MHz. Oscillation level of the ac voltage can be altered from 5 mV to 1.1 Vrms and it can be swept in 1mV increments. The internal dc bias voltage source can provide ± 35 V in 10 mV increments. The measuring frequency or dc bias voltage can be automatically or manually swept in either direction. The measurements on the p-InSe based Schottky and n-CdS/p-InSe heterojunction devices were carried out within the frequency range of 1 kHz-2 MHz. The amplitude of the dc ramp was varied from -1 to 1.5 V with 0.05 V increments. The oscillation level of the ac voltage was set to 0.05 V. Prior to measurement, a standard capacitance of known value was used to calibrate the system and the sample devices were placed in a shielded box. The diagram of the experimental set up for C-V measurements is shown in Fig.3.11.

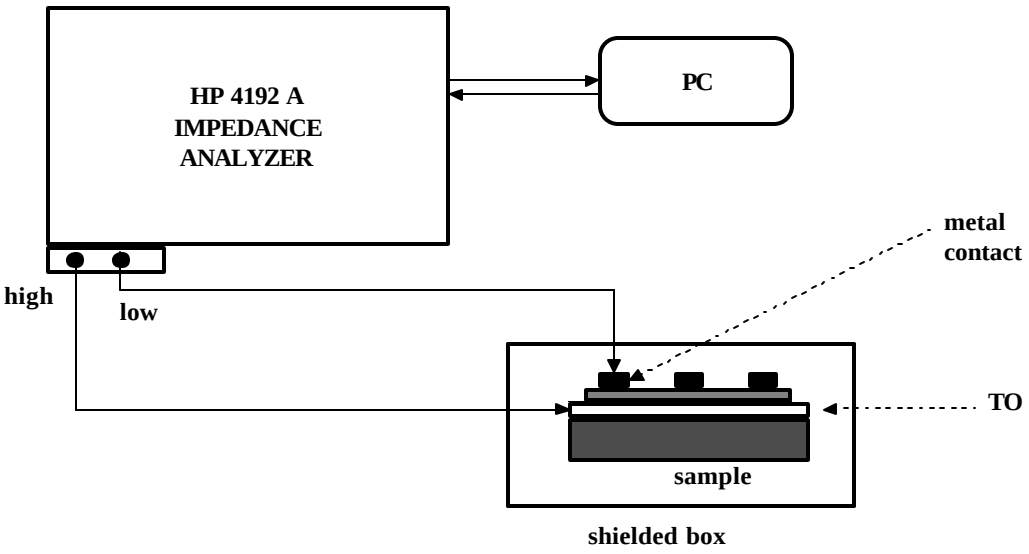


Fig.3.11: The experimental set up of the capacitance measurement system.

3.3 Spectral Response Measurements

The spectral response measurements were carried out for both the six-arm bridge shaped films and the devices produced in this work. The technique is based on measuring the photocurrent as a function of the wavelength of incoming monochromatic light. The spectral distribution of a semiconductor film reveals the band gap of the material whereas for the devices, it is the most direct method for determining the barrier height. The schematic diagram of the spectral response measurement system is shown in Fig.3.12.

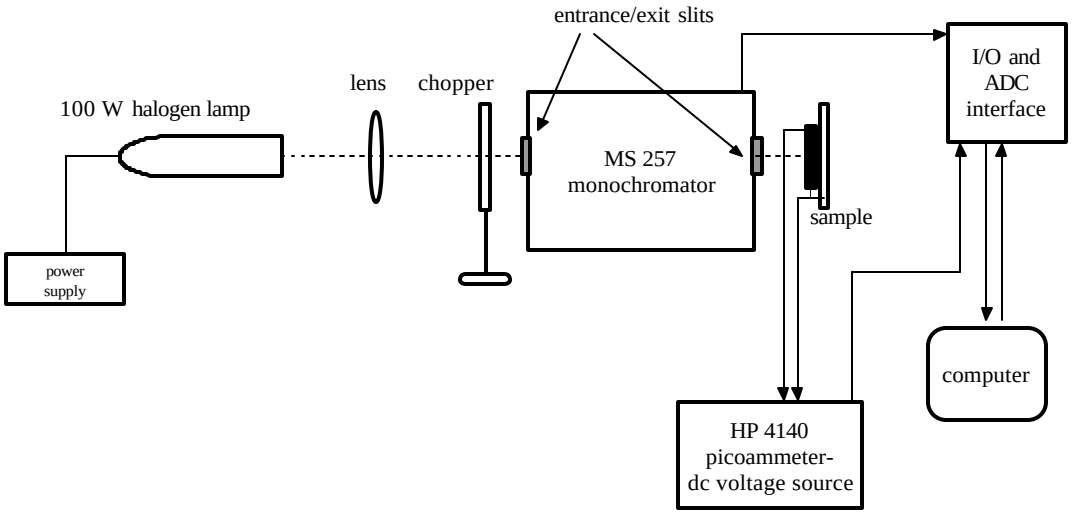


Fig.3.12: The schematic diagram of the spectral response measurement system.

The measurements were performed by using an Oriel MS 257 monochromator and the produced photocurrent was measured in the wavelength of 450-900 nm with 5nm increments by using HP 4140 picoammeter/dc voltage source. The light source was a 100 W halogen projector lamp which is aligned with the entrance slit of the monochromator. In order to focus the light on the slit a lens was set in front of the light source. A variable frequency chopper which was placed between the lens and the slit enables to measure the currents in dark and under illumination. The samples were mounted right in front of the exit slit such that the

monochromatic light which comes out of the slit illuminates perpendicular to the surface of the films and the devices, except, the measurements of the n-CdS/p-InSe solar cells were carried out by illumination from the back wall where the light first passes through the CdS window layer. The net photocurrent was obtained by subtracting dark current from the measured photocurrent in the presence of illumination. The photoresponse spectra obtained was then corrected for the spectral distribution of the light source used for the illumination.

3.4 Thickness Measurement

The thicknesses of the InSe and CdS thin films were measured by DEKTAK 3030ST profilometer which can measure surface texture below 10's of nm and film thickness up to 131 microns with a 10 to 20 Angstrom resolution. The system consists of a 12.5 micron diameter stylus and a camera for locating the stylus on the region at which the thickness were to be measured. The stylus can be moved electromechanically on the surface of the film and the force of the stylus can be set to a value in the range of 1-50 mg, in order to optimize the load for the surface of the film. The thin films were deposited onto glass substrates, thus the thicknesses were measured by scanning the stylus over the glass surface up to the edge of the film surface. Measurements were carried out for different regions of the films and it was observed that the thickness over the whole surface was almost unchanged.

3.5 Structural Characterization

3.5.1 Scanning Electron Microscopy (SEM) and Energy Dispersive X-rays Analysis (EDXA)

The uniformity of the surface and the composition of the material is an important factor in thin film applications. Scanning electron microscopy (SEM) provides valuable information on the surface of the material and composition of the region near the surface region with a lateral resolution of about 20 Å. The

determination of the grain size and c-axis orientation of thin films can also be determined through the SEM analysis. The basic physical principle that scanning electron microscopy based on can be summarized as follows. When an electron beam is scanned across the surface of the material, different interactions occur between the electron beam and the sample. The incoming electron beam on the surface of the material causes the emission of secondary electrons which are collected to form a high-magnification image of the surface that is the secondary emission mode of the SEM. The microanalization mode of SEM is based on inner shell ionization of atoms induced by the beam of electrons. An energetic electron inelastically scatters and ionizes an inner shell atom by removing an atomic electron that requires a specific minimum amount of energy known as the critical ionization energy. The characteristic X-rays emitted by this process is used to determine the elemental composition of the material. This technique is called energy dispersive analysis of X-rays (EDXA) and can be used to investigate elements which has atomic number greater than eleven.

The surface analysis and the elemental compositions of the deposited films were carried out by using a JSM-6400 scanning electron microscope equipped with energy dispersive X-ray facility in Department of Metallurgical Engineering at METU.

3.5.2 X-ray Diffraction Analysis (XRD)

The crystallinity and the phases of the InSe and CdS thin films were determined by the X-ray diffraction analysis. The X-ray region normally considered to be the part of the electromagnetic spectrum lying in between 0.1-100 Å. The interatomic distances are usually of the order of a few angstrom, thus standard optical microscope measurements do not provide enough information on the crystal structure. However, X-rays with a few angstroms wavelengths can be used to investigate the microstructures of the materials. When a beam of monochromatic X-ray falls onto a material, it is necessary that the waves emitted by individual atoms be in phase with each other in the direction of observation. The maximum conditions for

a beam diffracted by atomic planes are given by the following expression which is known as the Bragg equation.

$$n\,l = 2d\sin q \qquad (3.5.1)$$

where n represents the order of reflection maximum and is an integer. The other physical parameters are defined as follows: wavelength of the incoming X-rays is l, the interplanar spacing between successive atomic planes is d and the angle of incidence, q, which is equal to the angle of reflection.

The XRD analysis were carried out by using a Rigaku Miniflex system equipped with Cu-K_α radiation of average wavelength 1.54059 Å in the scan range of $2q = 5^o$-80^o with 2^o/min. scan speed. The XRD patterns were analyzed with a computer software and ICDD database which includes the diffraction patterns of well known structures of InSe and CdS. The peak matching process was carried out based on the observed peak positions at specific $2q$ values and relative intensities of the peaks. The schematic diagram of the XRD system is shown in Fig.3.13.

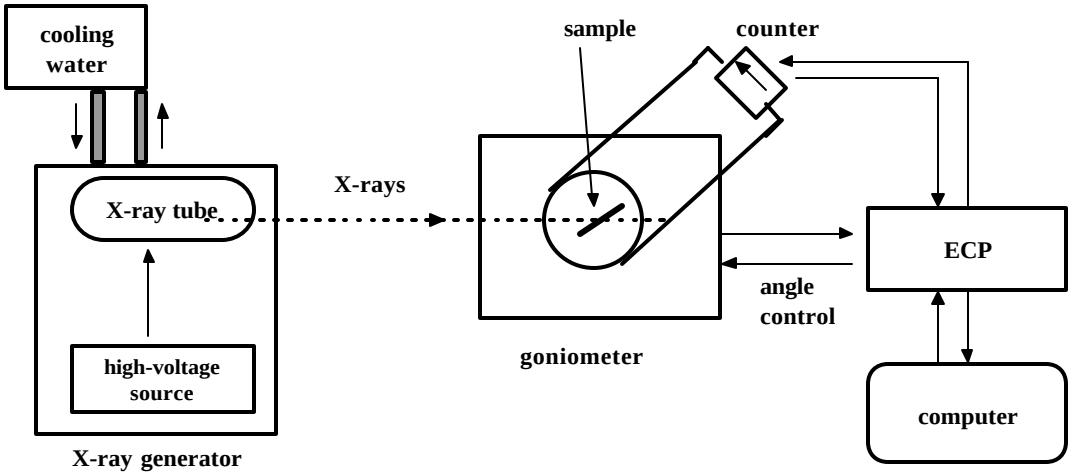


Fig.3.13: The schematic diagram of the XRD system.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Structural Characterization

4.1.1 Structural Analysis of InSe and CdS Thin Films

InSe thin films. Undoped and Cd-doped InSe thin films have been deposited onto hot and cold soda-lime glasses by thermal evaporation technique. The structural properties and the composition of the films are strongly dependent on the deposition parameters and the source material. The starting material is a 99.99% pure single crystal powder of In_2Se_3. The XRD pattern of the powder as seen in Fig. 4.1 confirmed that the powder is In_2Se_3 single crystal with a preferred crystalline orientation in the plane of (015). The crystal structure of the powder is hexagonal with lattice parameters of a=4.05, b=4.05 and c=29.41 Å.

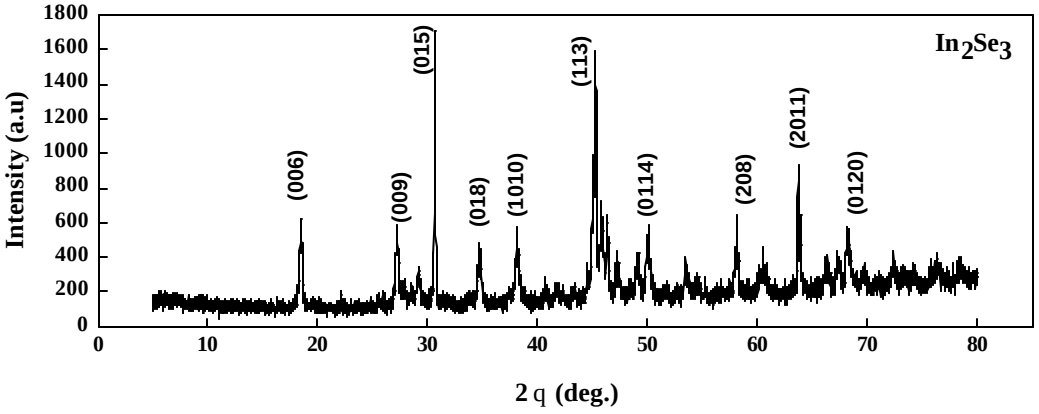


Fig.4.1: XRD pattern of the evaporation source.

SEM analysis have indicated that as-grown films were composed of about 49% In and 51% Se and no other impurity atoms found in the structure. XRD measurements of the cold substrate as-grown InSe films indicated that the films were amorphous in nature which was consistent with the previous works done by Chaiken et.al [97] and Quasrawi [98]. Two broaden peaks were clearly distinguishable in the XRD pattern. However, the intensities of these peaks were very low which indicates that long-range crystallinity is not formed in the structure of the films with a preferred directionality. Annealing at 100 ^{o}C of the cold substrate un-doped InSe films for various annealing time periods does not change the structure as seen in the Fig.4.2. Transformation into crystalline state starts with annealing at 150 ^{o}C for 60 minutes.

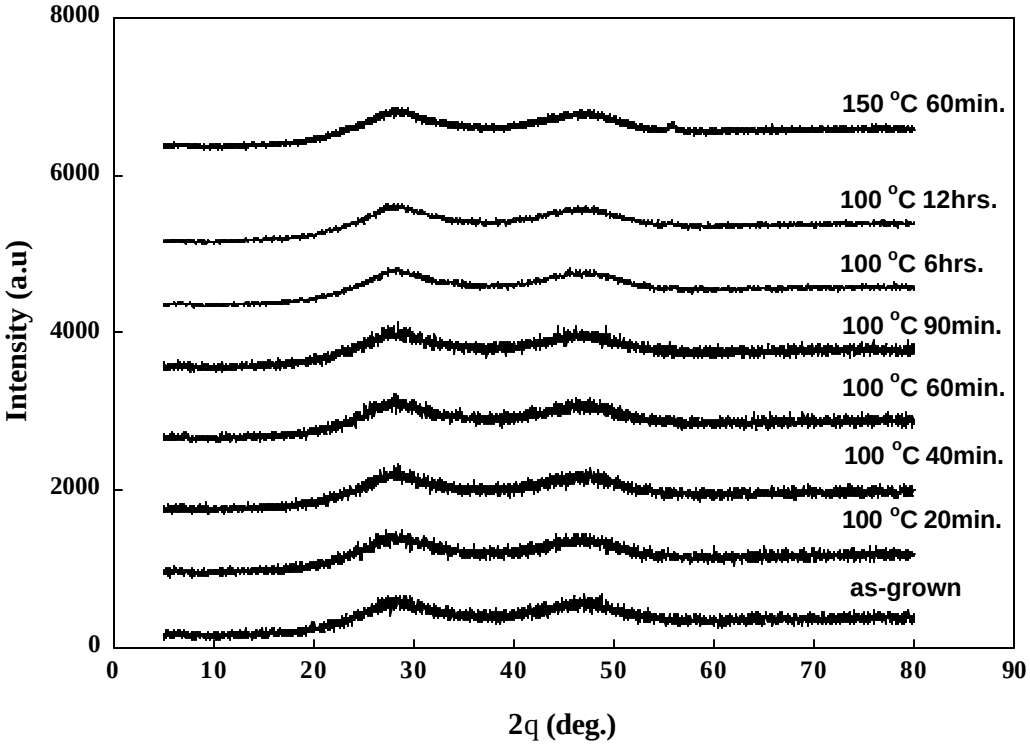


Fig.4.2: XRD pattern of undoped InSe films annealed at 100 ^{o}C and 150 ^{o}C for different annealing times.

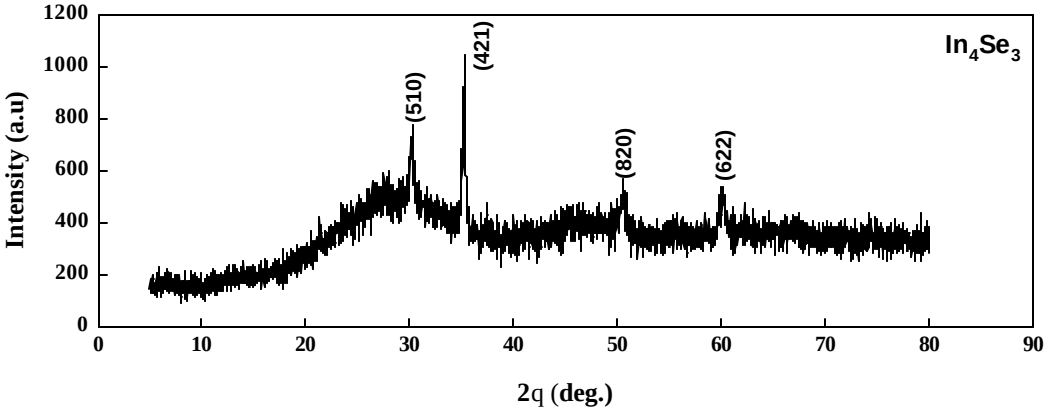


Fig. 4.3: XRD pattern of T_s >100 °C undoped InSe films.

However, the conductivity type also converted into n-type at this temperature which is not a desired condition for this work because the main purpose of this work is to study p-type InSe based devices. When the films are deposited on hot substrate above 100 °C, XRD results show polycrystalline behavior as seen in Fig.4.3. The deposited films in this case exhibit In_4Se_3 phase with a preferred crystalline direction along the (421) plane. The crystal structure was found to be orthorhombic with lattice parameters a=15.3, b=12.18 and c=4.05 Å.

Later, the effects of Cd doping were also investigated on the InSe films. XRD patterns of the lightly Cd doped films with less than 0.17 Cd/InSe ratio indicated that the cold substrate Cd-doped films were exactly the same as the ones without doping. Annealing at 100 °C of these films also shows no change in the structure.

However, further annealing above 100 °C indicates the start of transition into polycrystalline state as illustrated in Fig.4.4. On the other hand, heavily doped cold substrate film with Cd/InSe ratio of 0.24 has shown In_6Se_7 polycrystalline phase with three peaks in the planes of (112), (113) and ($\bar{2}$14). Contribution of Cd atoms into the InSe structure results in forcing the In and Se atoms to form an ordered polycrystalline structure. The crystal structure was found to be monoclinic with lattice parameters a=9.43, b=17.66 and c=4.06 Å as shown in Fig.4.5. However, the samples grown with Cd doping on hot substrates are unexpectedly in amorphous

phase. This could be due to the segregation of Cd atoms producing disorder in the structure.

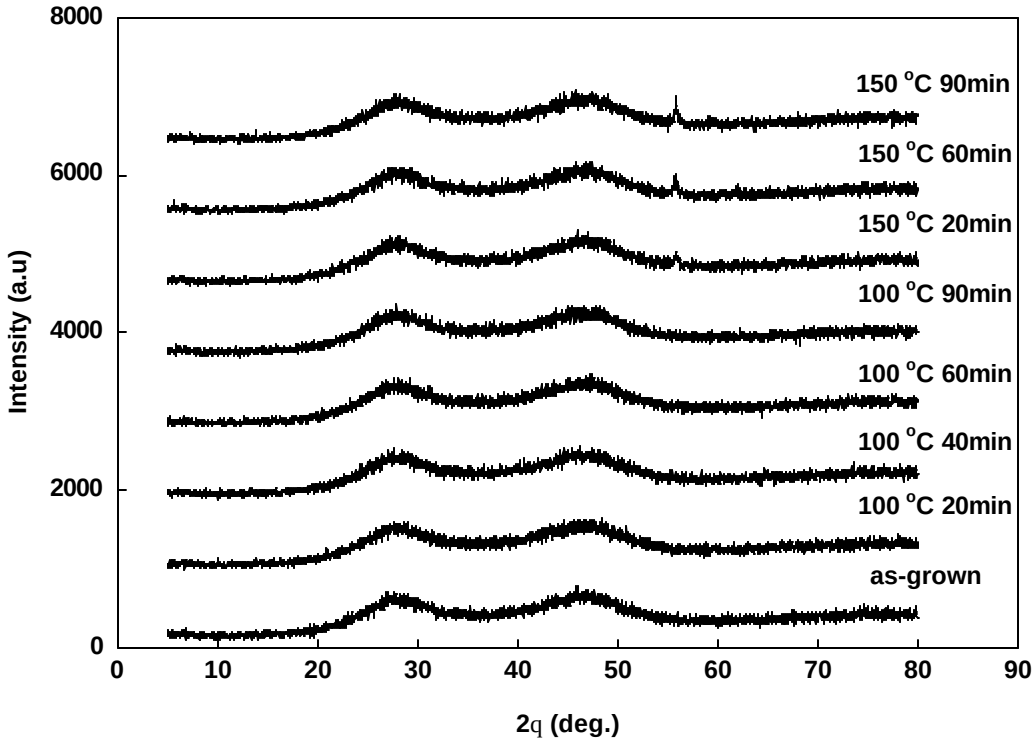


Fig.4.4: XRD pattern of the lightly doped cold substrate InSe films annealed at 100 °C and 150 °C for various annealing time periods.

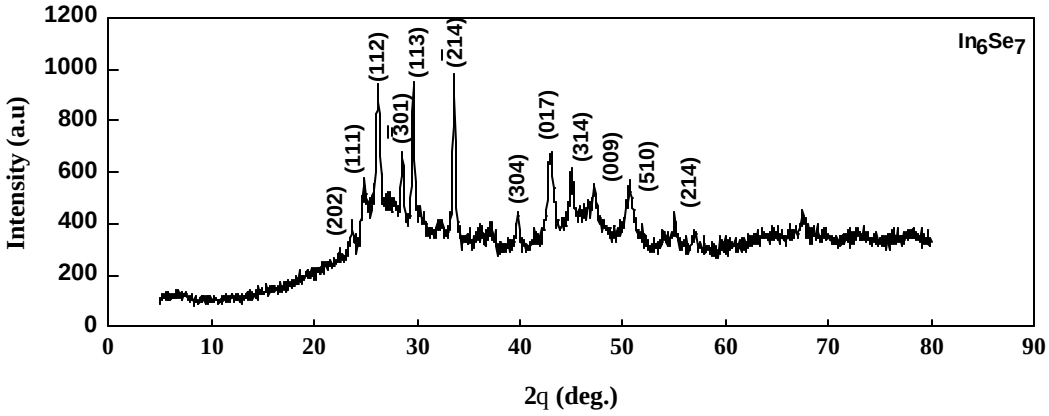


Fig.4.5: XRD pattern of heavily doped cold substrate InSe film.

The structural properties obtained from SEM and XRD analysis of the un-doped (A) and Cd-doped (B) as-grown InSe thin films were summarized in Table 4.1.

Table 4.1: The structural parameters of the undoped and doped as-grown InSe thin films.

Sample	T source (°C)		T substrate (°C)	In %	Se %	Cd %	Cd/InSe %	In/Se %	phase
	InSe	Cd							
A1	673	-	-	48.9	51.1	-	-	1.0	amorphous
A2	723	-	>100	-	-	-	-	-	In_4Se_3
B1	700	320	-	55.6	36.3	8.1	0.1	1.5	amorphous
B2	700	320	-	46.3	34.6	19.1	0.2	1.3	In_6Se_7

CdS thin films have been deposited onto hot soda lime glass by using CdS powder by thermal evaporation technique. The XRD spectra as shown in Fig.4.6 exhibits a sharp peak at 2θ equal to 26.44° which corresponds to (002) plane of hexagonal CdS. This result indicates that the film is in a polycrystalline state with a preferred direction of crystallization in (002) plane which is consistent with previous works done by Parlak [99] and Mamikoglu [61]. A broader and much less weaker peak is also observed in the plane of (004) plane at 2θ equal to 54.52°.

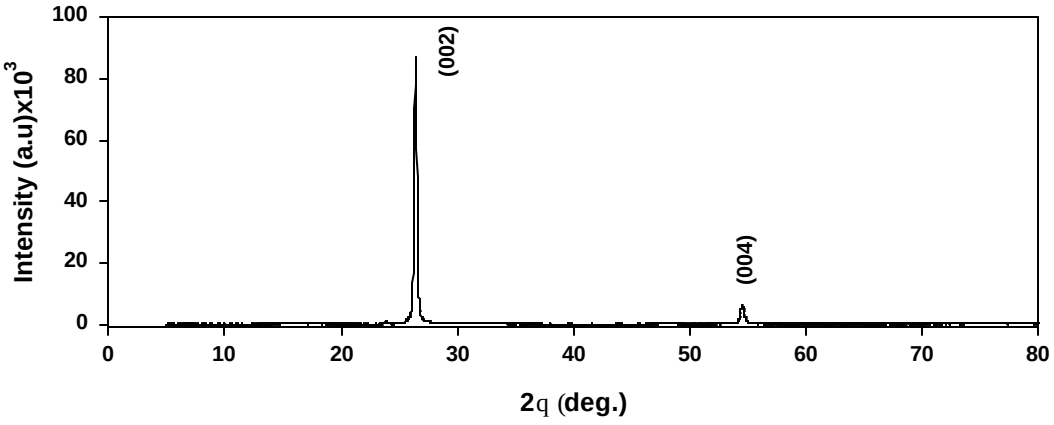


Fig. 4.6: XRD pattern of CdS thin film.

4.2 Electrical Properties of InSe Thin Films

4.2.1 Conductivity Measurements

In this section, the results of electrical conductivity of the films deposited with and without Cd-doping on cold and hot substrates are presented together with the effect of post depositional annealing. The observed conductivity in vacuum deposited thin films is often due to extrinsic properties rather than intrinsic properties. The source of the extrinsic conductivity is often associates with the defect nature of the evaporated films. Stoichiometric films of compound semiconductors are difficult to obtain by thermal evaporation technique. It is because, one of the starting materials of the compound may evaporate more rapidly and as a result the film contains trap centers. Furthermore, vacuum deposited films contain large stresses which result in more trapping centers due to the structural disorder.

In order to carry out electrical measurements, indium ohmic contacts were evaporated onto Hall bar shaped (six-arm bridge) Cd doped and un-doped InSe thin films. Thus, indium contacts will not add any parasitic impedance to the semiconductor thin films beyond the equilibrium values. The ohmicity of the films was checked during the dark current-voltage measurements at different temperatures. The I-V measurements at different temperatures indicated that the variations were linear and independent of reversal of the applied bias. All the films deposited onto cold substrates were exhibited p-type conduction while the films grown at substrate temperatures above 100 ^{o}C shown n-type conductivity. The room temperature conductivity values of as-grown films grown on cold substrates, with thicknesses in the range of 1.1-3.5 μm, have conductivities in the range of $8.7x10^{-5}$-$1.1x10^{-4}$ $(\Omega\text{-cm})^{-1}$. Deposition of hot substrate films at substrate temperatures between 100-150 ^{o}C has not shown a pronounced effect on the conductivity values which were found to be in the order of 10^{-4} $(\Omega\text{-cm})^{-1}$. However, Cd-doping of the films effectively increases the conductivity of the films depending on the doping concentration. Heavily doped films with Cd/InSe ratio 0.24 has conductivity 4 order of magnitude higher than the undoped ones. Whereas, lightly doped films with Cd/InSe ratio up to 0.17 have almost the same conductivity with the undoped films.

Thus, the conductivity of the InSe thin films increases with increasing doping concentration. Some electrical parameters of undoped, lightly doped and heavily doped InSe films are listed in Table 4.2.

Table 4.2: The room temperature electrical parameters of undoped (A) and Cd-doped (B) InSe thin films.

Sample	Cd/InSe %	T_a (^oC)	t (min.)	σ $(\Omega.cm)^{-1}$	μ ($cm^2/V.s$)	p (cm^{-3})
A1	-	-	-	$8.7x10^{-5}$	54	$1.0x10^{13}$
A11	-	100	20	$5.5x10^{-5}$	46	$7.4x10^{12}$
B1	0.09	-	-	$4.1x10^{-5}$	21	$1.2x10^{13}$
B11	0.09	100	20	$4.8x10^{-5}$	44	$6.9x10^{12}$
B12	0.09	100	90	$4.1x10^{-5}$	56	$1.4x10^{12}$
B13	0.13	-	-	$3.0x10^{-3}$	-	-
B2	0.24	-	-	$2.3x10^{-1}$	0.1	$1.5x10^{19}$

The variation of conductivity with temperature was studied in the range of 100-430 K in order to determine the conduction mechanisms in different temperature regions for doped and un-doped thin films. Here, only the results of cold substrate films are given because of type conversion for hot substrate films. It was found that for doped and un-doped films the conductivity increased exponentially with increasing temperature. The Fig.4.7 indicates the variation of conductivity with respect to temperature for a typical un-doped cold substrate , as-grown film. As seen from the plot, the conductivity increases sharply with increasing temperature above 200 K. Below 200 K, the temperature dependence is weak.

The temperature dependence of the conductivity indicates that different conduction mechanisms are dominating in different temperature regions. In order to determine these conduction mechanisms, the conductivity data was first analyzed by the general conductivity expression given below,

$$s\sqrt{T} = s_0 \exp\left(-\frac{E_a}{kT}\right) \qquad (4.2.1)$$

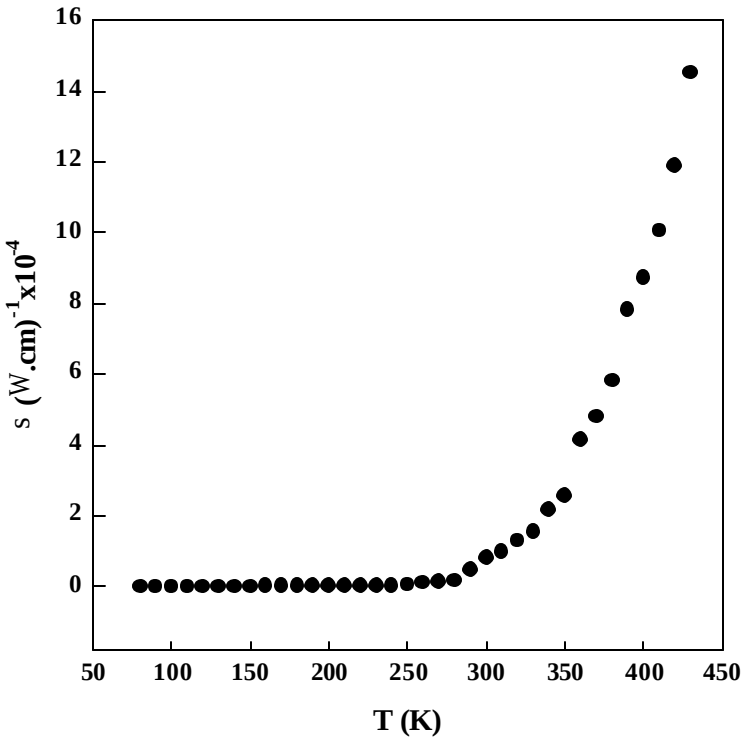


Fig.4.7: A typical variation of conductivity-temperature dependence for undoped as-grown InSe thin film in the temperature range 80-430 K.

where E_a is the activation energy and σ_0 is the pre-exponential factor. The plot of $\ln(\sigma T^{1/2})$ versus inverse temperature shows a linear behavior above 200 K as shown in Fig.4.8 which indicates that the conductivity obeys the relation given in Eq. 4.2.1. The slope of the linear region gives the activation energy E_a=288 meV. Thus, it can be concluded that above 200 K the dominant transport mechanism is thermal excitation of the carriers. As seen in Fig 4.8, the variation is also linear in between 80-190 K. However, the weak temperature dependence of the conductivity with small activation energy of about 11meV in this region, gives the indication of possibility of Mott's hopping conduction instead of thermal excitation mechanism.

At low temperatures the hopping conduction according to the Mott's theory is given by the following expression [78],

$$s\sqrt{T} = s_0 \exp\left(-\frac{T_0}{T}\right)^{\frac{1}{4}} \qquad (4.2.2)$$

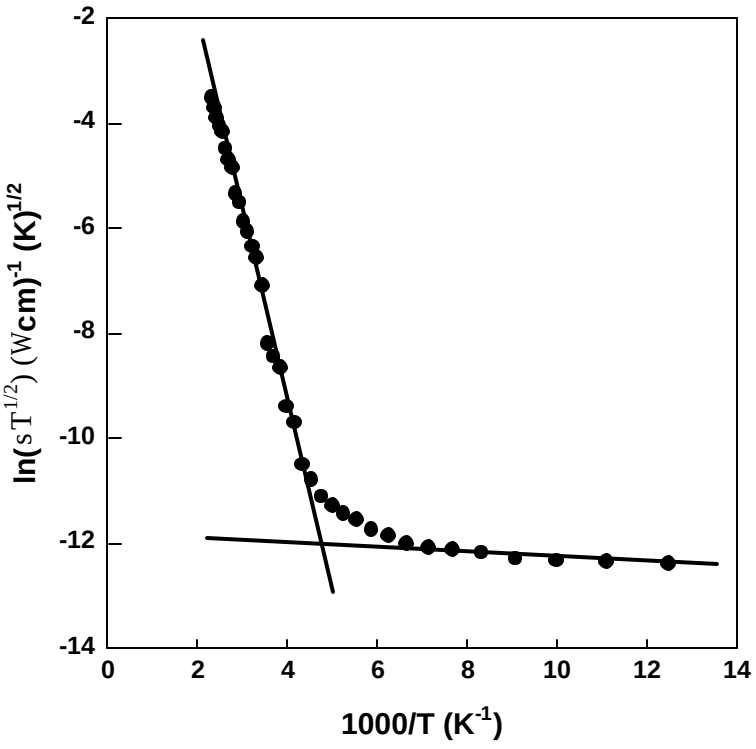


Fig. 4.8: The variation of conductivity with inverse temperature.

where T_0 is the degree of disorder and σ_0 is the pre-exponential constant. Both of these values can be obtained experimentally from the $\ln(\sigma T^{1/2})$ versus $T^{-1/4}$ plot as in Fig.4.9. These values were used to evaluate Mott's parameters that were previously discussed in detail in section (2.2.2). The Mott's parameters determined through the temperature dependent conductivity measurements were tabulated in Table 4.3, for typical undoped and lightly doped as-grown InSe thin films in the temperature range of 100-190 K. Here, $N(E_F)$ is the density of localized states at Fermi level, R is the hopping distance between the closest sites, W is the average hopping energy and α is the decay constant. As seen in Table 4.3, the requirements for the validity of Mott's variable range hopping were satisfied as $W > kT$ and $\alpha R > 1$ with the degree of disorder $T_o > 10^3$ which indicates that variable-range hopping is the dominant conduction mechanism below 200 K for lightly doped and un doped InSe thin films.

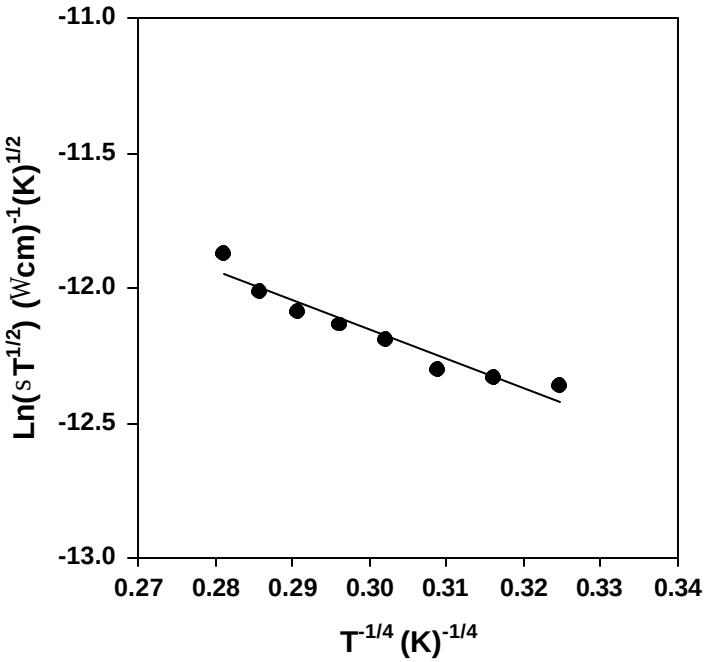


Fig.4.9: Ln($\sigma T^{1/2}$) vs $T^{-1/4}$ plot.

Table 4. 3: The Mott's parameters determined at an average temperature of 145 K for a typical un-doped (A) and lightly Cd-doped (B) as-grown InSe thin films.

Sample	T_o (K)	α (cm^{-1})	$N(E_F)$ ($cm^{-3}eV^{-1}$)	R (cm)	W (meV)	αR	kT (meV)
A	$2.8x10^6$	$1.6x10^5$	$2.6x10^{14}$	$2.9x10^{-5}$	39	4.6	13
B	$3.7x10^6$	$9.9x10^5$	$4.6x10^{16}$	$5.0x10^{-6}$	42	5.0	13

The product αR is the degree of localization and kT is the thermal energy of the carriers at a specific temperature. In this mechanism, conduction occurs by hopping of the carriers to larger distances in order to find energetically closer sites. The disordered atoms create trapping states which are located in the band-gap. The empty states can only capture carriers from the filled states below the Fermi level at low temperatures since there are no free carriers to capture from the valence band.

In order to determine the effect of post depositional annealing on the samples, they were annealed at different temperatures and time periods. However, in this

section only the results for annealing at 100 ^{o}C are given due to the type conversion at higher temperatures. As seen from Fig.4.10, annealing of the samples did not show any effect on the variation and the conductivity values, however, the activation energies in both high and low temperature regions increased from 220 to 263 meV and from 14 to 34 meV, respectively. This increase of the conductivity activation energy implies that the annealing clears out some traps exist in the band gap region.

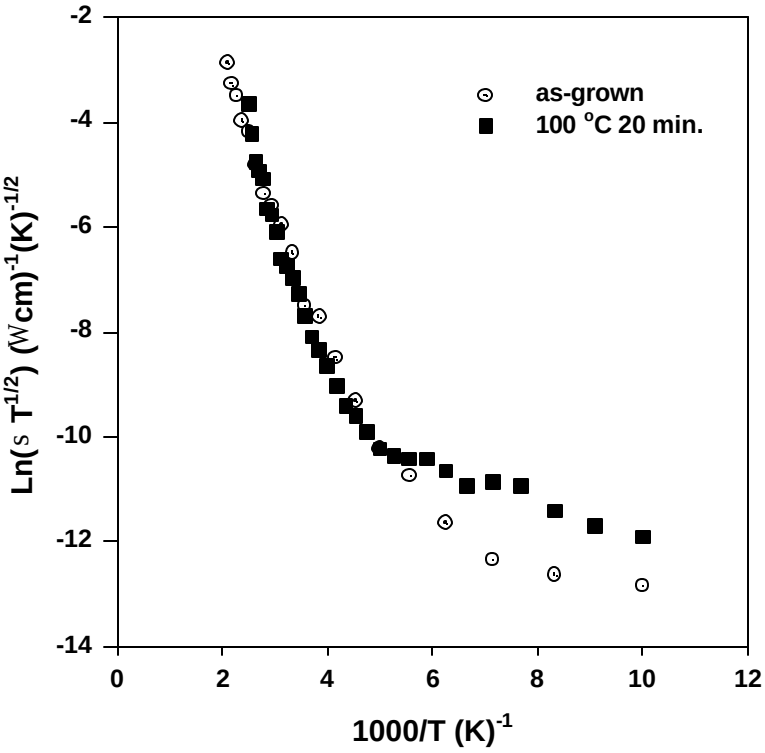


Fig.4.10: The conductivity variation of (a) un-annealed (b) annealed at 100 ^{o}C for 20 minutes, undoped cold substrate InSe films.

In the low temperature region, conductivity values increased slightly whereas in the high temperature region conductivity is unchanged. The overall variation of the both annealed and un-annealed films are the same which indicates that thermal excitation is the dominant conduction mechanism above 200 K and variable range hopping is dominant below 200 K for annealed film also.

Doping effect of the films was investigated through dark temperature dependent I-V measurements. As mentioned in the beginning of this section,

conductivity values were reasonably increased for the samples with Cd/InSe ratio 0.24, whereas for the samples with Cd/InSe ratios up to 0.17 were almost the same as the undoped samples. Figure 4.11 represents the conductivity variation with inverse temperature in comparison of undoped, highly and lightly doped samples.

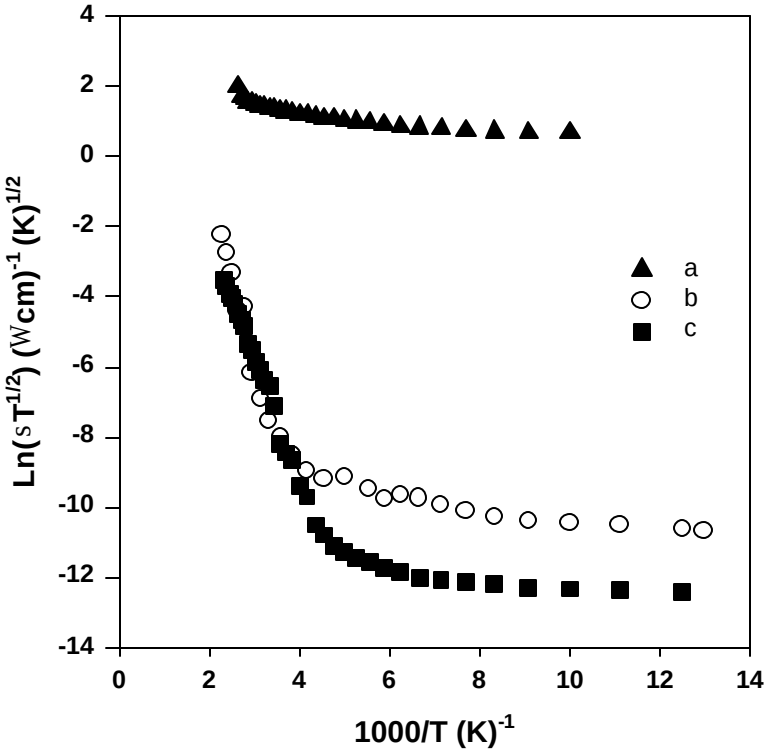


Fig. 4.11: The conductivity variation of (a) heavily doped (b) lighty doped (c) undoped InSe films.

As seen from the Fig. 4.11, undoped and lightly doped samples have the same conductivity variation and lightly doped sample have slightly higher conductivity values in the low temperature region. The activation energies for lightly doped sample were found to be 325 meV and 15 meV for high and low temperature regions respectively. In comparison with the undoped sample, activation energies were slightly increased with light doping of the films. However, heavily doped sample have shown 4 orders of magnitude higher conductivity values and the temperature dependence of the conductivity were weak in the range of 100-380 K. Activation energies in between 100-230 K and 230-380 K were found to be 29 meV and 7 meV,

respectively. This variation of conductivity for highly doped samples with low activation energy can be interpreted as a metallic behavior. This behavior may be attributed to defective degenerate structure caused by the high concentration of Cd atoms. Annealing effect was also studied for lightly doped films and it was concluded that annealing at 100 ^{o}C of the film did not show a pronounced effect on the sample as seen in Fig. 4.12.

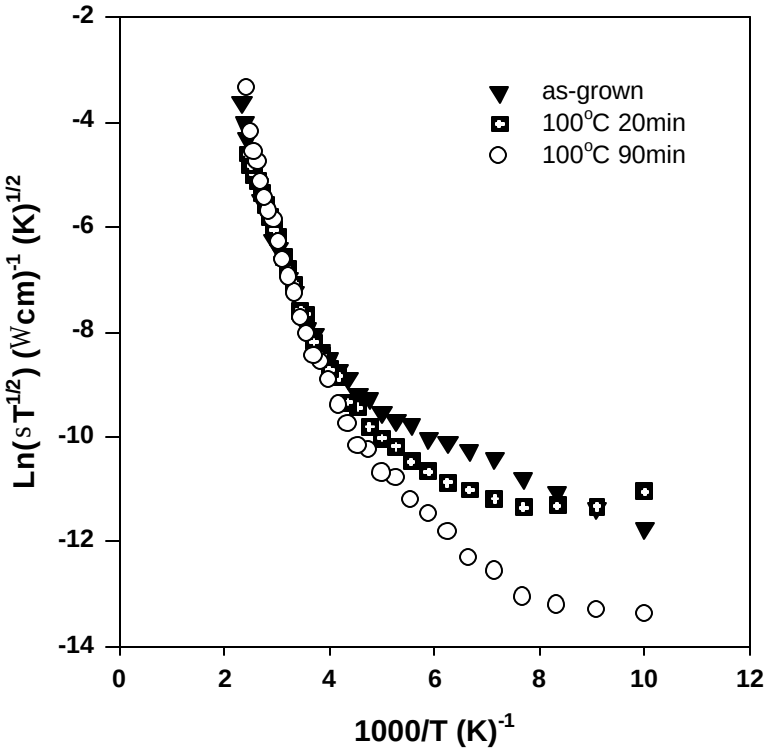


Fig. 4.12: The conductivity variation of lightly doped un-annealed and annealed film at 100 ^{o}C for different annealing times.

As seen from Fig. 4.12, annealing at 100 ^{o}C up to 90 minutes did not show a significant effect neither on the variation nor on the conductivity values. Two different conduction mechanisms are dominant above and below 200 K which are thermal excitation and variable range hopping respectively, as in the case of un-doped films.

The overall conclusion on the temperature dependent conductivity measurements for the doped and un-doped InSe films can be stated as follows. The

conductivity variations and the values are the same for lightly doped and un-doped samples. Annealing at 100 °C of these samples did not improve the conductivity independent of the time of annealing. Also, XRD measurements indicated that annealing at 100 °C for 12 hours did not show any significant change in the structure of the films. Heavily doped samples, however, have shown four order of magnitude higher conductivity values yet they became metallic. Further annealing of the samples was not considered because as the hot probe technique revealed that annealing above 100 °C converts the conductivity type from p- to n-type.

4.2.2 Carrier Concentration and Hall Mobility

In order to determine the carrier concentration and Hall mobility of the doped and undoped films, temperature dependent Hall effect measurements were carried out in the temperature range of 100-430 K. The magnetic field strength was kept at a constant value of 0.97 T in the specified temperature range for all measurements. The Hall coefficient R_H were determined experimentally by measuring the Hall voltage V_H using the expression $R_H=tV_H/IB$ as explained in section (2.3.1). The value of the Hall coefficient then revealed the carrier concentration at each temperature by the expression $R_H=r/pq$ where r was chosen to be of the order of unity. Room temperature carrier concentrations for the undoped cold substrate films were found to be in the range of $2.6x10^{12}$-$3.5x10^{13}$ cm^{-3}. Lightly doped films have shown the concentration values between $1.4x10^{12}$-$1.2x10^{13}$ cm^{-3} comparable to that of undoped ones. However, heavily doped sample have considerably higher carrier concentration in the order of 10^{19} cm^{-3} due to high amount of Cd atoms found in the structure by SEM analysis. These results were consistent with the conductivity measurements such that conductivities of the un-doped and lightly doped samples were comparable whereas the heavily doped samples had four orders of magnitudes higher conductivities in comparison to that of un-doped and lightly doped ones. For a typical undoped cold substrate InSe thin film, variation of concentration with inverse temperature is shown in Fig. 4.13 in the temperature range of 100-430 K. As seen in the figure, the carrier concentration increases with increasing temperature in accordance with $p=p_0\exp(-\Delta E/kT)$. The temperature dependence is strong above

200 K in which region carrier concentration sharply increases with increasing temperature. The activation energy was found to be 204 meV in this temperature region. Below 200 K temperature dependence is weak but the activation energy could not be calculated due to fluctuation of the data.

Annealing effect were investigated for the undoped cold substrate films in the same temperature range and it was found that annealing at 100 ^{o}C for 20 minutes did not show a significant effect on the carrier concentration as seen in Fig.4.13, in comparison with the un-annealed one. The activation energy in high temperature region for the annealed sample was found to be slightly increased to 238 meV. Further annealing above 100 ^{o}C was avoided since in that case conductivity type converts from p- to n-type.

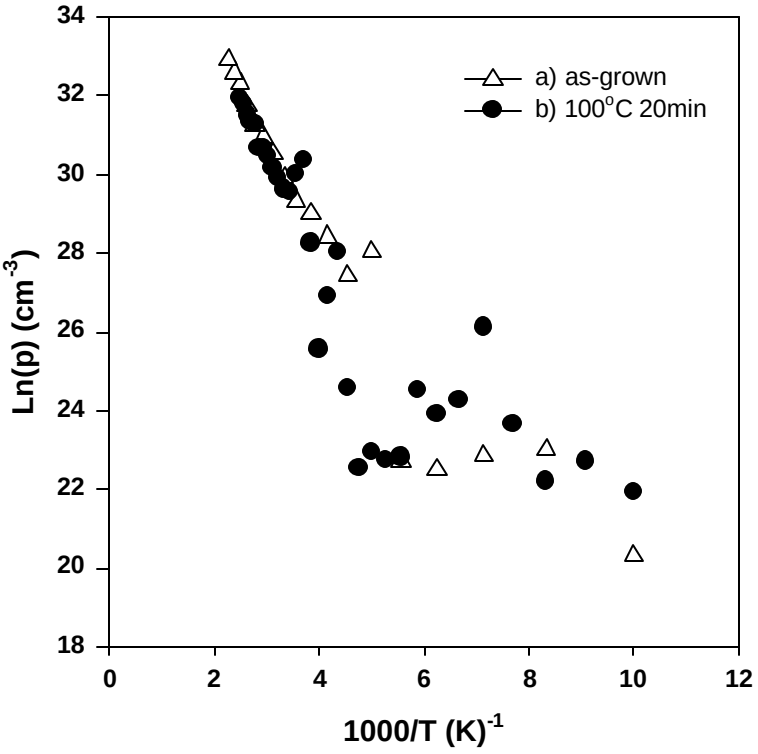


Fig. 4.13: The variation of carrier concentration (a) un-annealed (b) annealed at 100 ^{o}C for 20 minutes for undoped cold substrate films.

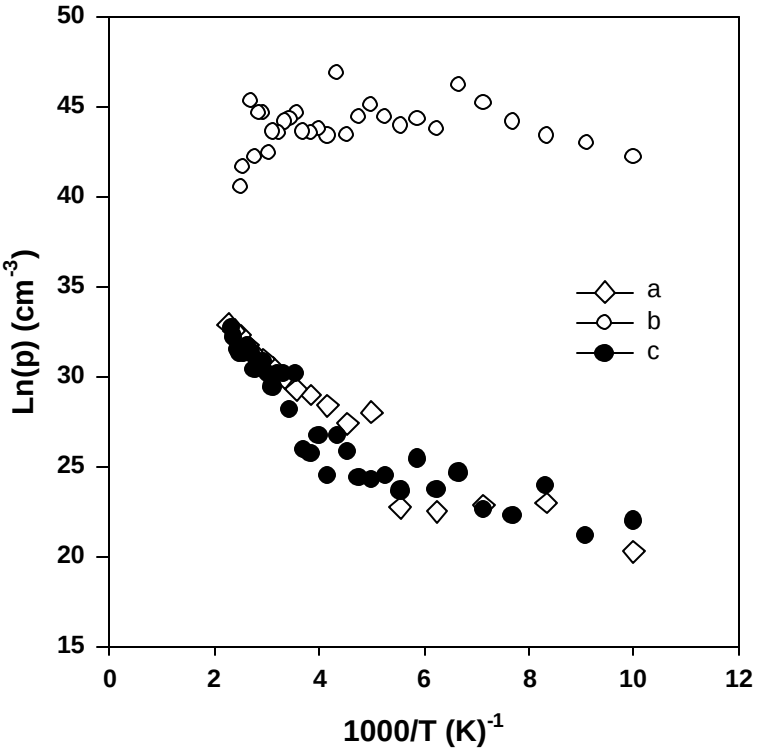


Fig.4.14: The variation of carrier concentration with inverse temperature for (a) undoped, (b) heavily doped, (c) lightly doped films.

In order to get information about the carrier concentration and mobility by the effect of doping, temperature dependent Hall effect measurements were also carried out for highly and lightly doped samples in the temperature range of 100-430 K. Fig.4.14 represents the variation of carrier concentration with respect to inverse temperature for doped and undoped samples. The carrier concentration values for lightly doped sample were found to be similar to that of undoped one, however, the heavily doped samples with Cd/InSe ratio around 0.24 were almost insensitive to the change of sample temperature and had concentration values seven order of magnitude higher than that of lightly doped and undoped ones.

The weak temperature dependence of carrier concentration for heavily doped sample indicates metallic or degenerate structure of this sample which is consistent with the results of the conductivity measurements.

Annealing effect was also investigated for the lightly doped sample in the same temperature range. It was observed that annealing at 100 ^{o}C up to 90 minutes results in no significant change in the concentration values and variations over the studied temperature range.

The room temperature mobility values of the doped and un-doped samples calculated using the relation $\mu=\sigma/pq$ and it was found that the room temperature mobility values for the un-doped samples vary in the range of 2.7-82 $cm^2/V.s$ depending on the growth conditions. Whereas, mobility values for the heavily doped and lightly doped samples were calculated in between 0.1-21.2 $cm^2/V.s$ depending on the Cd doping concentration as seen in Table 4.2. The mobility values obtained here are comparable to those reported in previous work done by Quasrawi [98].

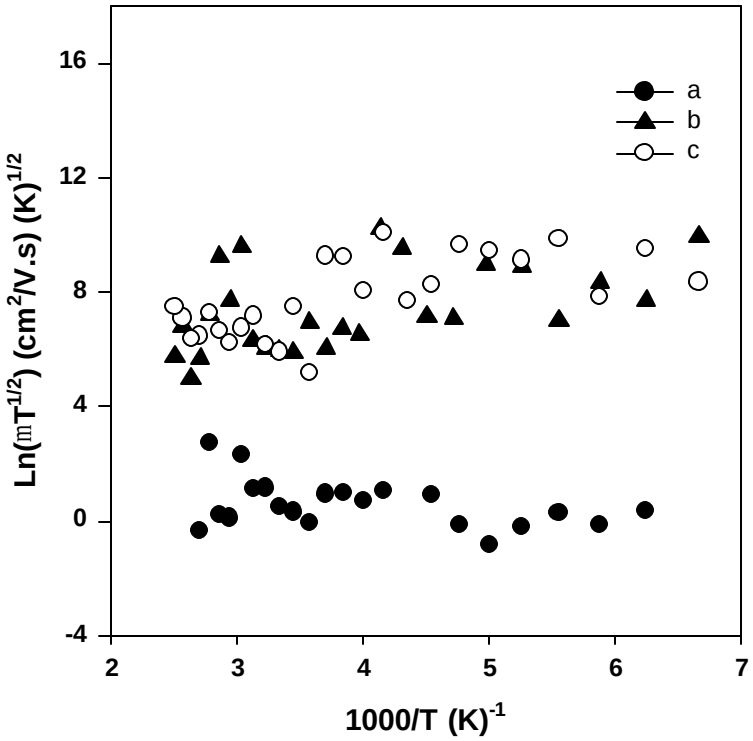


Fig.4.15: The variation of mobility for typical (a) heavily doped (b) undoped (c) lightly doped amorphous InSe thin films in the temperature range of 150-400 K.

As seen from Fig.4.15, undoped and lightly doped samples have mobility values in the same order, however, heavily doped sample have one order of magnitude lower mobility value than that of undoped and lightly doped ones. For these samples, variations of mobility with temperature are observed to be weak over the whole studied temperature range which indicates that the dominant scattering is neutral impurity scattering.

It was also found that post annealing did not yield any considerable changes in the mobility of the undoped and doped samples.

4.3 Electrical properties of CdS Thin Films

4.3.1 Conductivity Measurements

The temperature dependent electrical conductivity and the Hall effect measurements were carried out for undoped CdS thin films in the range of 100-430 K. The measurements were done by evaporation of In ohmic contacts onto the six-arm bridge CdS films with thicknesses in between 2.1-2.6 μm. The room temperature conductivities for these films were found to be around 1 $(\Omega cm)^{-1}$. All the deposited CdS films exhibit n-type conductivity which was determined by the sign of Hall coefficient and the hot probe technique. Temperature dependent conductivity measurements indicated that the conductivity of the CdS films increases exponentially with increasing temperature as illustrated in Fig. 4.16.

The conductivity data for the CdS thin films was analyzed by the grain boundary model proposed by Seto [64] as explained in section (2.2.2). In order to determine the dominant conduction mechanism, the conductivity-temperature dependence is plotted as $Ln(\sigma T^{1/2})$ -1000/T.

As seen from the Fig.4.17, two linear regions with activation energies of 77 meV and 11 meV were found corresponding to high and low temperature regions, respectively. The analysis of conductivity data indicates that the dominant conduction mechanism above 200 K is the thermionic emission of the carriers over the grain boundary. The activation energy in this region is larger than kT.

However, the low activation energy in the 100-200 K temperature range rules out the possibility of thermionic emission over the grain boundary.

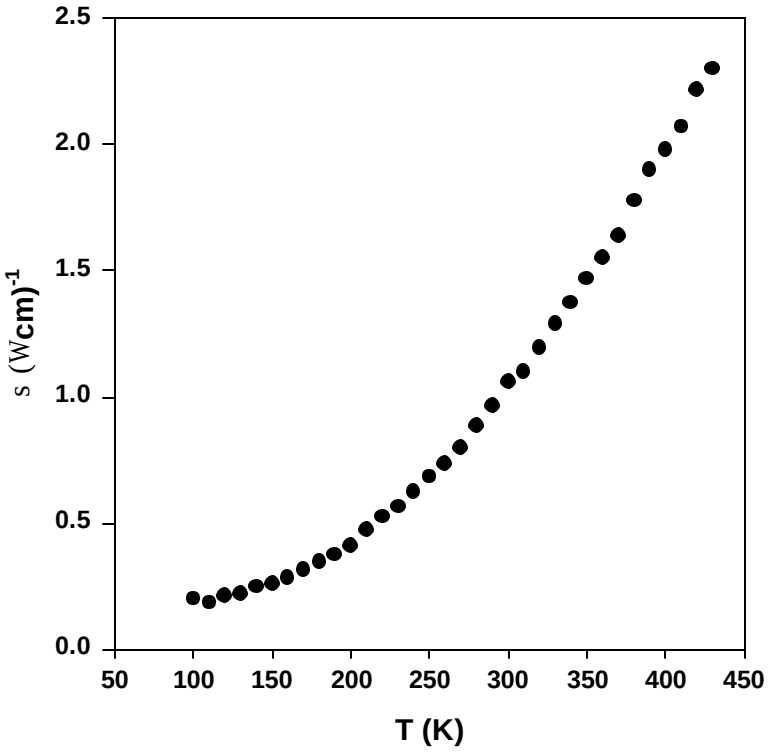


Fig. 4.16: The variation of conductivity with temperature for a typical CdS thin film.

Thus, Mott's hopping conduction mechanism, expressed as Eq.4.2.2, may be the dominant conduction mechanism in this region since the carriers do not have enough energy to surmount the grain boundary potential. The Mott's parameters are calculated by using the slope and the intercept values of Fig.4.18 as explained in section (2.2.2) and it was found that in between 100 and 200 K conduction is dominated by the variable range hopping (VRH) since the requirement for VRH is satisfied as $\alpha R>1$ and $W>kT$. Therefore, the conduction in this low temperature region occurs by hopping of the charge carriers from the filled trap states to the empty trap states.

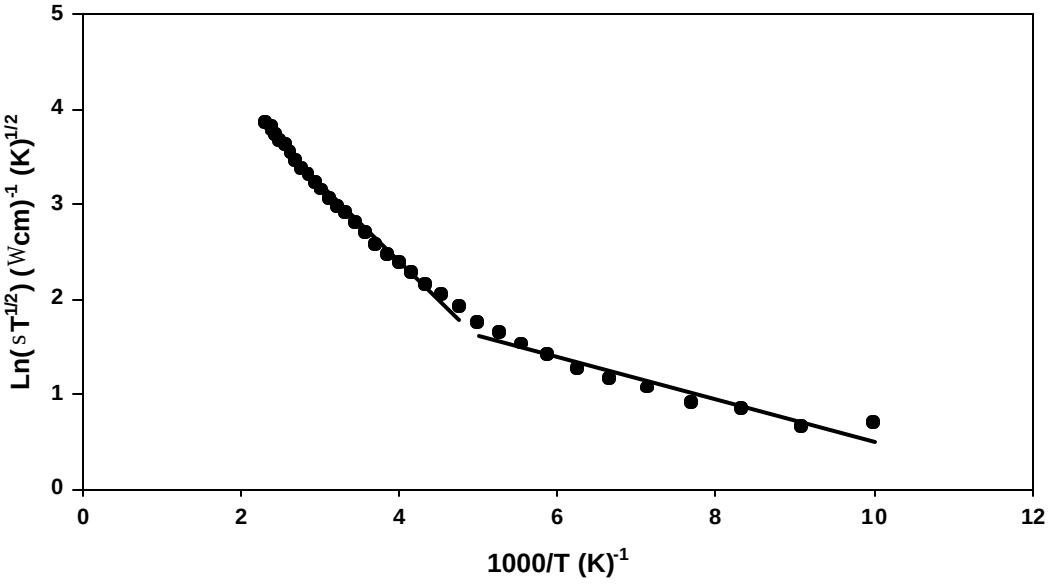


Fig. 4.17: The variation of the conductivity with inverse temperature in the range of 100-430 K.

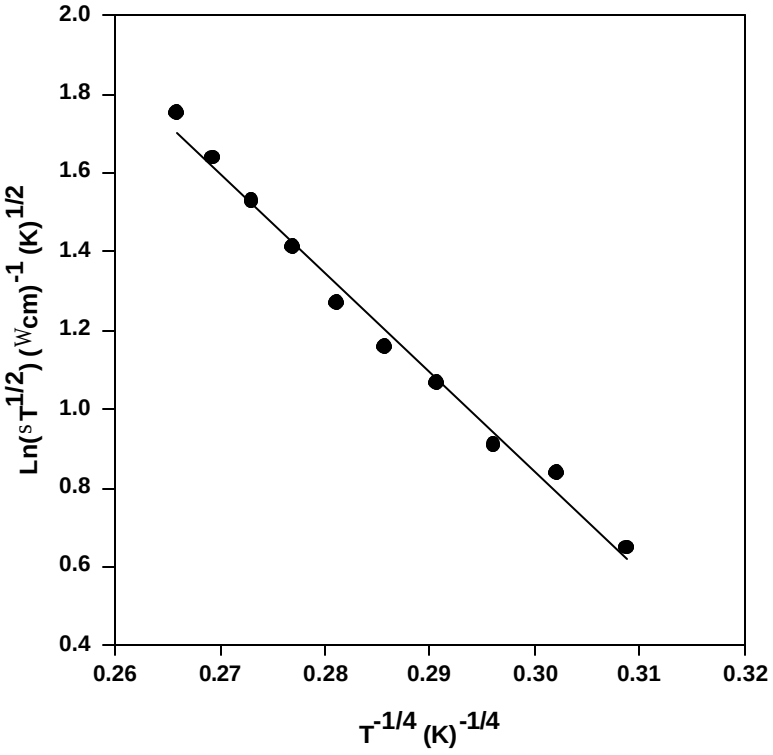


Fig. 4.18: The $Ln(\sigma T^{1/2})$-$T^{-1/4}$ variation in the temperature range of 100-200 K.

Annealing effect was also investigated for the sample annealed at 100 ^{o}C for 20 minutes through temperature dependent conductivity and Hall effect measurements but no significant change were observed for the room temperature electrical conductivity of the annealed CdS thin film with activation energies of 78 meV and 9 meV in the high and low temperature regions, respectively. The Mott's parameters found in the temperature range of 100-200 K for two as-grown CdS thin films grown with different deposition parameters were given in Table 4.4 at an average temperature of 145 K.

Table 4.4: Mott's parameters of two as-grown CdS films.

T_{source} (^{o}C)	T_{subs}(^{o}C)	T_o (K)	α (cm^{-1})	$N(E_F)$ ($cm^{-3}eV^{-1}$)	R (cm)	W (meV)	αR	kT (meV)
725	213	$2.2x10^{5}$	$5.2x10^{7}$	$1.1x10^{23}$	$4.7x10^{-8}$	21	2.5	13
700	232	$7.1x10^{6}$	$1.5x10^{9}$	$7.9x10^{25}$	$4.0x10^{-9}$	49	5.8	13

4.3.2 Carrier Concentration and Hall Mobility.

The carrier concentration and Hall mobility of the CdS thin films were investigated by the Hall effect measurements with the same technique explained for the InSe thin films in section 4.2.2. Room temperature electron concentrations of the films were found to be in the range of $1.4x10^{16}$-$3.4x10^{18}$ cm^{-3} depending on the substrate temperatures. The variation of electron concentration with inverse temperature in the temperature range of 150-420 K for a typical CdS film is illustrated in Fig.4.19, which shows that the carrier concentration increases exponentially with the absolute temperature in the high temperature region where thermionic emission is the dominant conduction mechanism. However, in the low temperature region in between 100-200 K, temperature dependence of the carrier concentration is weak.

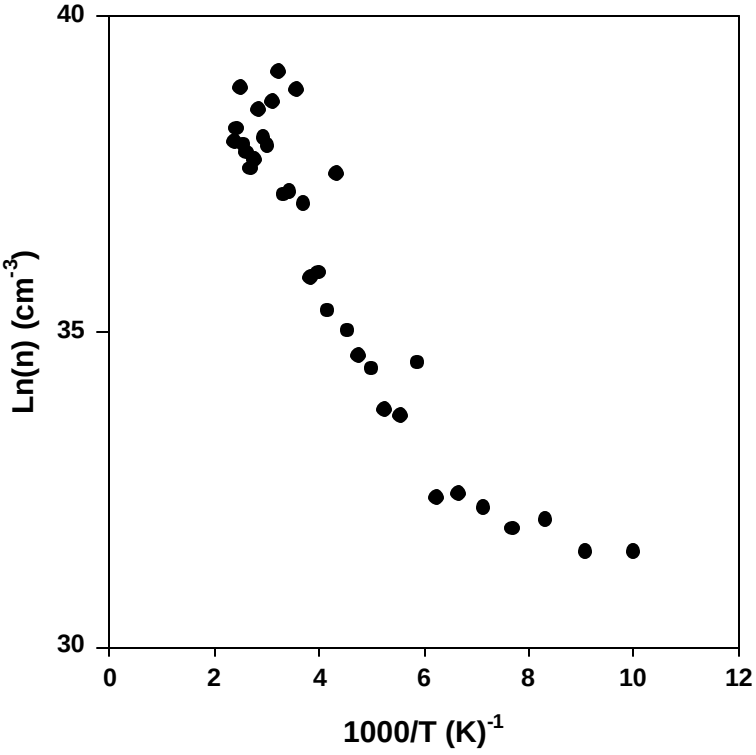


Fig. 4.19: The variation of electron concentration of a typical CdS thin film.

The room temperature Hall mobility of the films were found in between 3.1-3.5 $cm^2/V.s$. The temperature dependence of the mobility data was analyzed according to the thermionic emission model proposed by Seto [64]. In this model the effective mobility can be expressed as;

$$m = m_0 T^{-1/2} \exp\left(-\frac{q f_b}{kT}\right) \qquad (4.3.1)$$

where ϕ_b is the barrier height at the grain boundary. The $Ln(\mu T^{1/2})$-1000/T variation of a typical sample is given in Fig. 4.20. It indicates that the mobility increases as the absolute temperature increases. The grain boundary height (f_b) was found to be 98 meV and 14 meV above and below 200 K, respectively. The barrier height in the high temperature region is larger than kT which verifies that thermionic emission is the dominant conduction mechanism in this region.

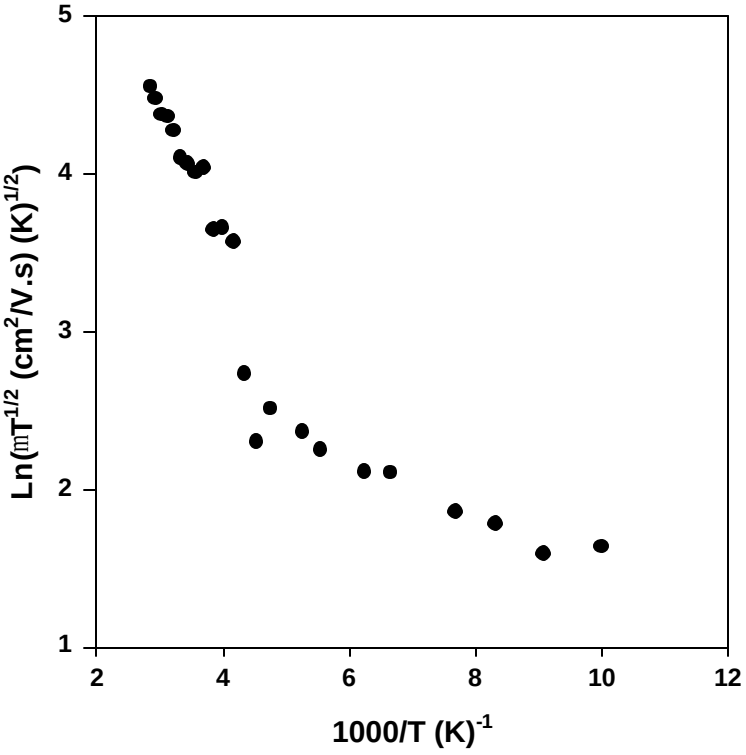


Fig. 4.20: The variation of mobility with inverse temperature.

In order to determine the existent scattering mechanisms, Log(μ)-Log(T) variation was considered as the increase in mobility with temperature satisfies the relation $m \alpha T^n$. The value of the exponent n determines the dominant scattering mechanism at each temperature range.

Fig.4.21 shows that in the low temperature region the mobility variation is almost temperature independent. The anomalous variation of mobility in this region indicates that the neutral impurity scattering is dominant. However, in the high temperature region above 220 K the linear variation fits to $m \alpha T^{5/2}$ relation which indicates that ionized impurity scattering is the dominant scattering mechanism. Thus, it can be concluded that scattering of carriers by impurities takes place over the whole temperature range studied and ionization of impurities increases with increasing absolute temperature.

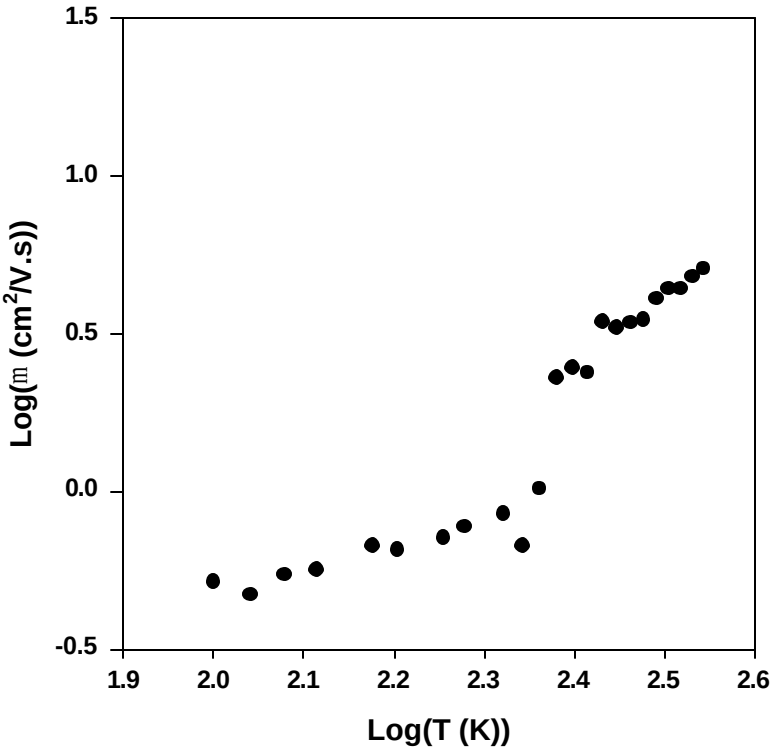


Fig. 4.21: Log(μ)-Log(T) variation for a typical CdS thin film.

Mobility variation with temperature did not change for the annealed sample at 100 ^{o}C for 20 minutes. However, room temperature mobility value decreased from 3.5 to 1.8 $cm^2/V.s$ with annealing whereas the carrier concentration slightly increased from $1.9x10^{18}$ to $3.4x10^{18}$ cm^{-3}. Therefore, at high temperatures the contribution of the intergrain ionized impurity scattering to the effective mobility increases with absolute temperature.

4.4 Optical Absorption of InSe Thin Films

The optical transmission or absorption spectrum is commonly used to investigate the optical properties of the materials. These measurements reveal information on the absorption coefficient, band structure and impurity levels of a semiconductor. The transmission measurements were carried out with a computerized double beam Perkin-Elmer UV/VIS Lambda 2S spectrometer by

directing light with energy in the range of 1.1-1.9 eV onto the semiconductor film and measured the transmitted light as a function of wavelength. Then, the transmission data were corrected according to the background absorption of the glass substrate on which the film was deposited. The optical absorption coefficient can be determined from the measured transmission data using the following relation,

$$a = \frac{1}{d}\ln\left(\frac{1}{T}\right) = \frac{1}{d}\ln\left(\frac{I_0}{I}\right) \tag{4.4.1}$$

where d is the thickness of the film and T is the transmission. The relation between the absorption coefficient and the incident photon energy is given by,

$$(ahn) = A(hn - E_g)^n \tag{4.4.2}$$

where A is a constant depending on the transition probability, E_g is the band gap of the semiconductor and n is an index having values ½ and 2 for direct and indirect allowed transitions respectively. The direct band gap of a semiconductor is therefore determined from the plot of $(ahu)^2$ versus incident photon energy.

The Fig. 4.22 represents the variation of the absorption coefficient with respect to incident photon energy for a typical undoped, cold substrate, as-grown InSe thin film. As seen from the plot, the absorption coefficient α decreases exponentially with decreasing photon energy. The absorption coefficient at room temperature was found to be in the range of $5.3\text{x}10^2$-$2.6\text{x}10^4$ cm^{-1} for the incident photon energies of 1.1-1.9 eV. The variation of the optical absorption near the fundamental absorption edge revealed the direct band gap around 1.74 eV for the film with thickness of 3 μm. This result is consistent with the band gap of amorphous InSe thin films given in the literature [97]. The high band gap may be the result of high structural disorder and defects in the structure of the film.

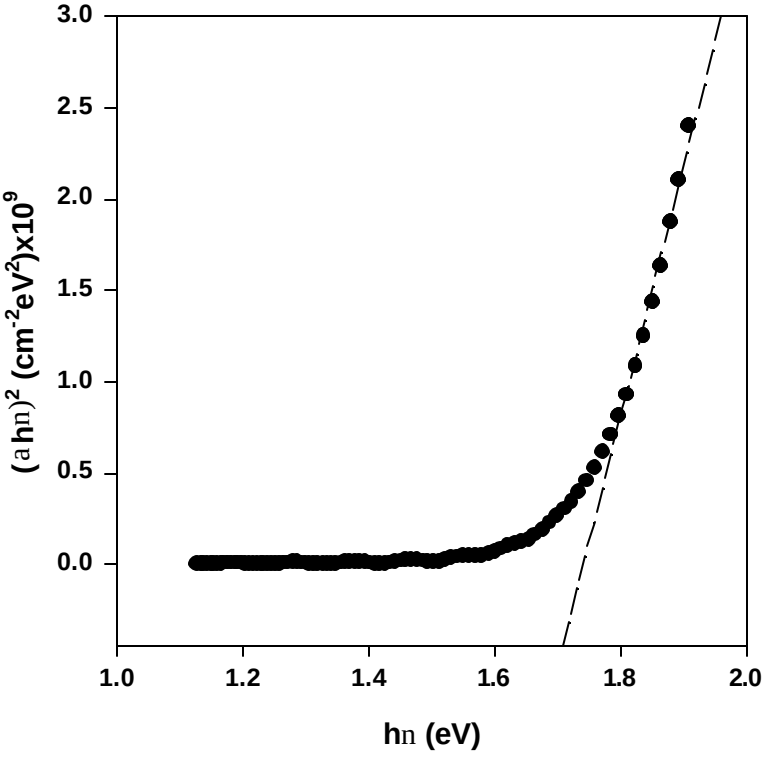


Fig.4.22: The variation of absorption coefficient for a typical InSe thin film.

4.5 Optical Absorption of CdS Thin Films.

The transmission spectrum of a typical CdS thin film measured in the spectral range of 1.1-2.9 eV with the same procedure used for InSe film explained in section (4.4.1). Using the transmission data, absorption coefficients at room temperature were calculated by Eq.4.4.1 in the specified energy range. The absorption coefficients at room temperature were found to be $1.4x10^3$-$3.8x10^4$ cm^{-1} for the minimum and maximum photon energies, respectively. The Fig. 4.23 represents the variation of absorption coefficient with respect to incident photon energy.

As seen from the figure, the film is almost transparent up to 2.31 eV of photon energy and from that point absorption of the photons increases sharply with photon energy in which region the absorption takes place through direct interband transition and extrapolation of the linear variation gives the optical band gap of about

2.36 eV for a typical polycrystalline CdS film with thickness of 2.64 μm. This result is in well agreement with the previous works done in literature [61,65].

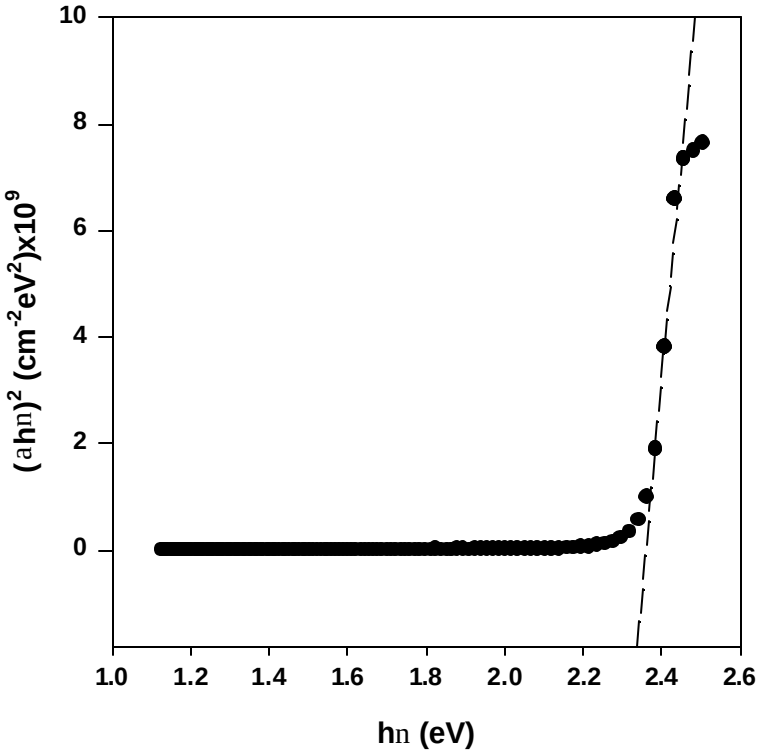


Fig. 4.23: The variation of absorption coefficient with photon energy for a typical CdS thin film.

4.6 Characterization of p -InSe Schottky Diodes

4.6.1 Current-Voltage Characteristics

In this section, the characterization results for the devices obtained with undoped, as-grown, cold substrate InSe thin films, are presented. InSe thin films have been deposited by thermal evaporation of 99.99% pure In_2Se_3 kept at around 800 ^oC onto tin oxide (TO) coated and soda lime glass substrates. Following the deposition, various metal contacts such as Ag, Au, In, Al and C with area of

$7.5x10^{-3}$ cm^2 were applied as explained in section (3.1.4) to achieve sandwich structures onto a-InSe/TO films which have thicknesses around 1 μm. As discussed in section (2.4.3), p-type semiconductors usually make rectifying junctions with metals whose work functions are less than that of the semiconductor. However, due to the complex band structure of p-InSe thin films this is not always the case experimentally. This is due to the self-compensating nature of p-InSe by which deep donors are created. Thus, p-InSe films can have rectifying structures with both low and high work function metals. For the case of low work function metals the diode is a typical Schottky barrier with a negative space charge region, whereas for the high work function metals the barrier is created by ionized deep donors [3]. The dark current-voltage measurements in this study have shown that amorphous p-type InSe thin films make the best rectifying contact with Ag. The junctions with In, Al and C and most of the Au contacts have shown ohmic behavior. However, Au contacts have shown some rectification for some of the samples which will be discussed later. Below, the current-voltage characteristics of different Schottky diode structures made with different metal contacts are presented.

i) *TO/a-InSe/In* structure: This structure has shown ohmic dark current-voltage characteristics even though the work function of indium is much smaller than the electron affinity of a-InSe in which case indium is expected to make rectifying contact. The linear current-voltage characteristic of a typical TO/a-InSe/In structure is represented in Fig.4.24, which indicates that the current in reverse and forward directions increase linearly with increasing voltage.

In order to decide whether there is a rectifying contact between TO/ a-Inse or a-InSe/In or not, the current-voltage characteristic of In/a-InSe/In was checked and it was found that the structure also indicates an ohmic behavior as shown in Fig.4.25. Thus, it can be concluded that indium makes an excellent ohmic contact to amorphous p-InSe thin films.

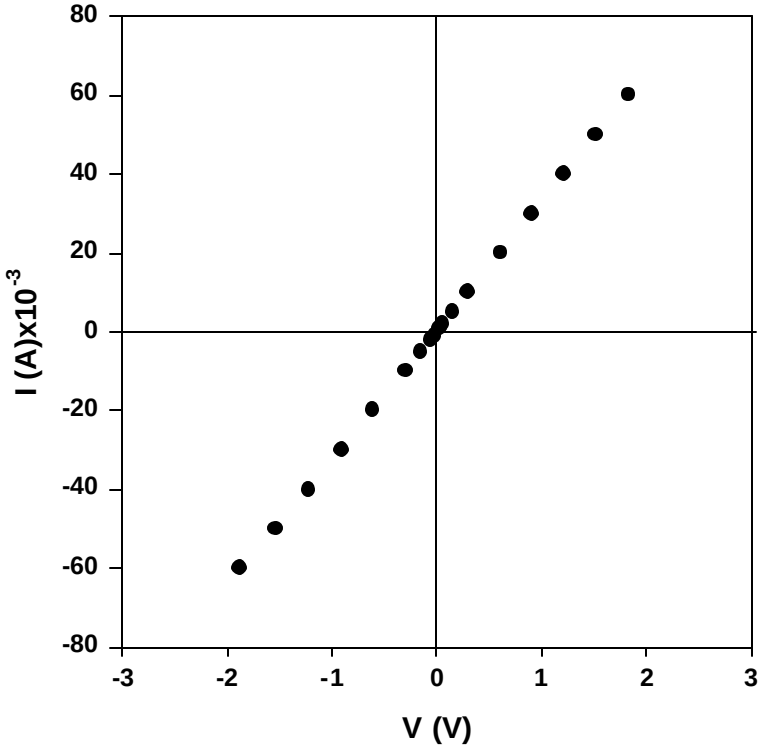


Fig.4.24: The current-voltage characteristic of a TO/a-InSe/In structure.

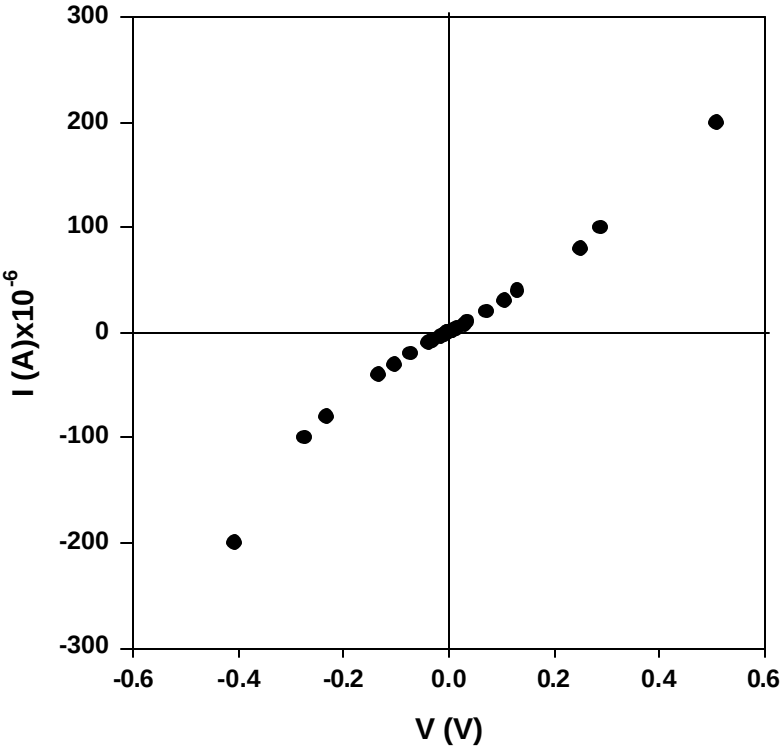


Fig.4.25: The current-voltage characteristic of In/a-InSe/In structure.

ii) *TO/a-InSe/Al* structure: This structure has also shown ohmic current-voltage characteristics contrary to Ag contacts. The work function of Al and Ag is almost comparable or less than the electron affinity of InSe, thus it was expected that these contacts were to be rectifying. However, only Ag contacts have shown considerable rectification whereas Al contacts are ohmic. The reason for this may be explained as Al makes block contact to the films and not diffuse into the film as in the case of Ag contacts. A typical current-voltage characteristic of TO/a-InSe/Al structure is shown in Fig. 4.26. The structure under reverse and forward biases behaves the same indicating that the current increases linearly as the voltage increases.

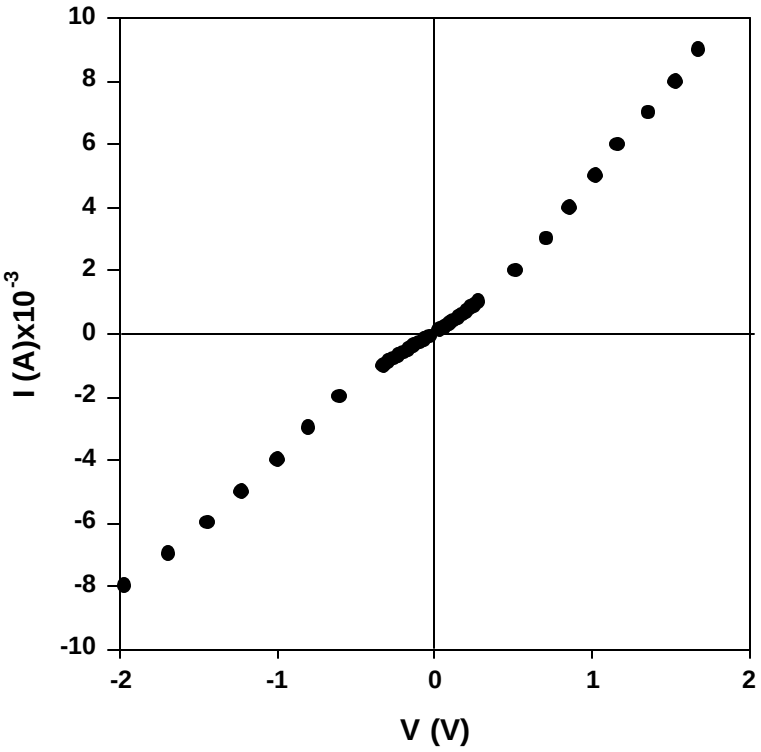


Fig.4.26: The current-voltage characteristic of TO/a-InSe/Al structure.

In order to strengthen this conclusion In/a-InSe/Al structure were also investigated and it was observed that both In and Al makes ohmic contacts to the typical amorphous p-InSe thin films deposited in this work. Fig.4.27 represents the dark current-voltage characteristic of In/InSe/Al structure.

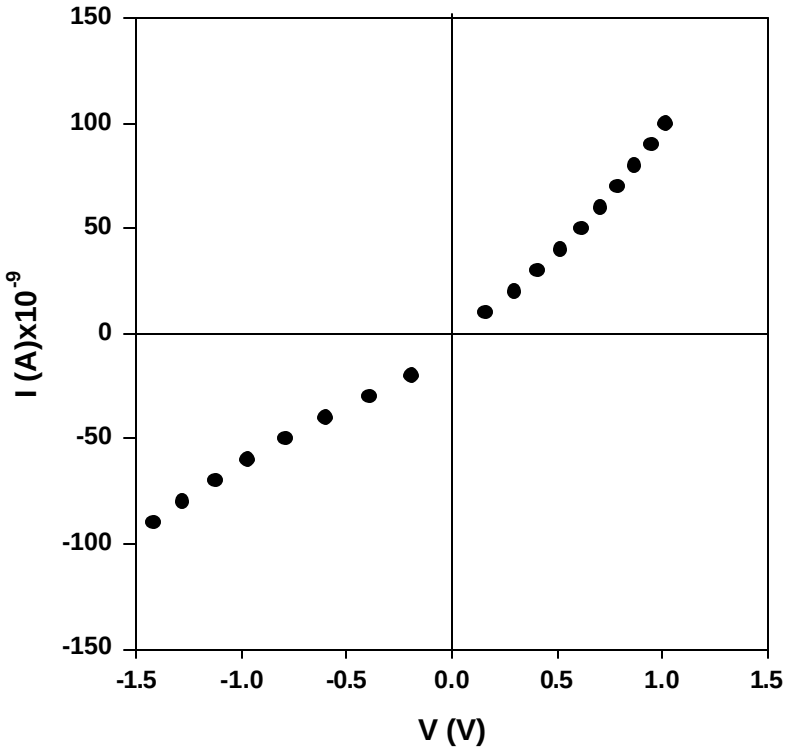


Fig.4.27: The current-voltage characteristic of In/InSe/Al structure.

iii) *TO/a-InSe/C* structure: Liquid colloidal graphite used to achieve cold contact onto a-InSe thin films without thermal evaporation. Carbon has a work function greater than that of InSe, thus carbon was expected to be ohmic with p-InSe thin film. The current-voltage characteristics also agreed with this theoretical expectation indicating an ohmic behavior as seen in Fig.4.28. This result is also supported by the current-voltage characteristic of In/InSe/C structure which also showed almost ohmic behavior as indicated in Fig.4.29.

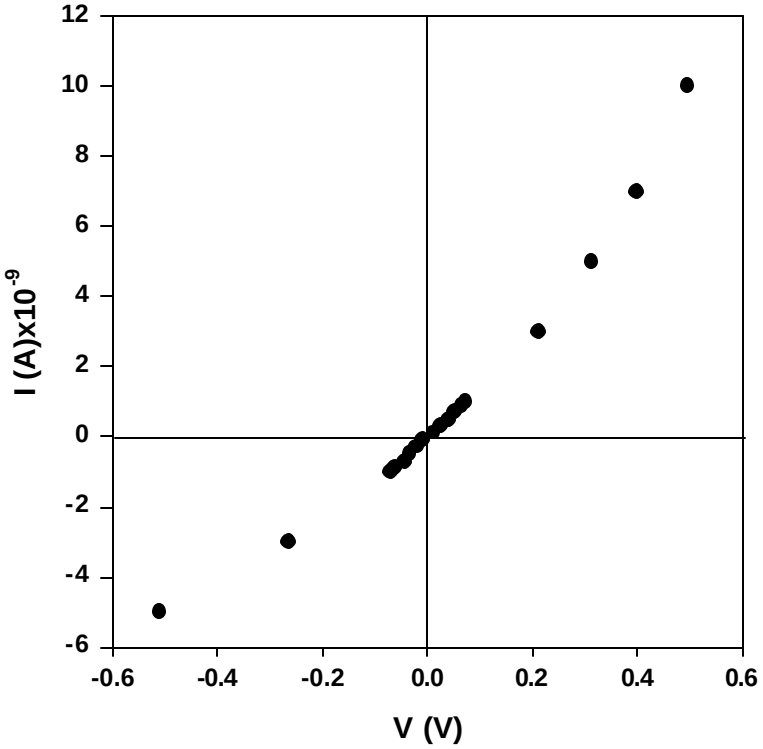


Fig.4.28: The current-voltage characteristic of TO/a-InSe/C structure.

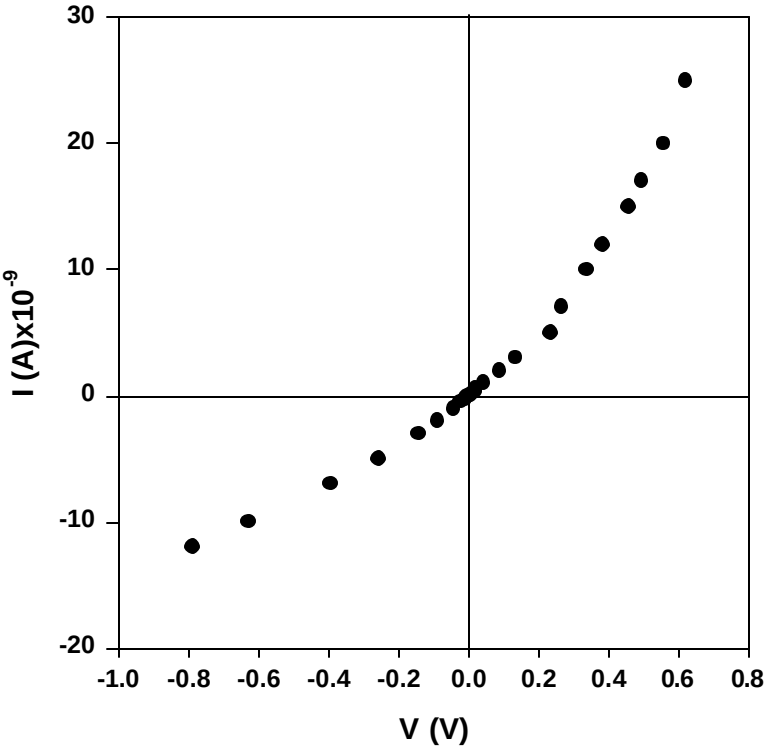


Fig.4. 29: The current-voltage characteristic of In/InSe/C structure.

iv) *TO/a-InSe/Au* structure: The current-voltage characteristic of this structure is also expected to be ohmic since Au has a work function greater than that of InSe electron affinity. Unexpectedly, it was experimentally observed that Au contact showed slight rectification with p-InSe thin film as shown in Fig.4.30. This result was also confirmed by the I-V characteristic of Au/a-InSe/Au structure as represented in Fig.4.31. Both figures indicated that there exists a small barrier between Au and p-InSe thin film at low voltage regions. Further proof can be interpreted from the I-V characteristic of In/a-InSe/Au structure since it was known experimentally that In makes ohmic contact with p-InSe film as seen in Fig.4.32.

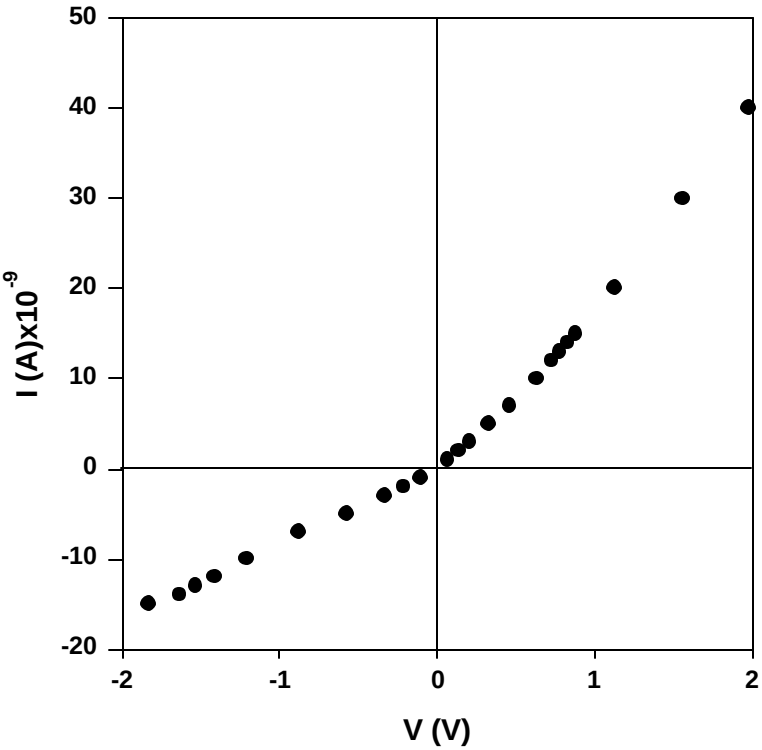


Fig.4.30: The I-V characteristic of TO/a-InSe/Au structure.

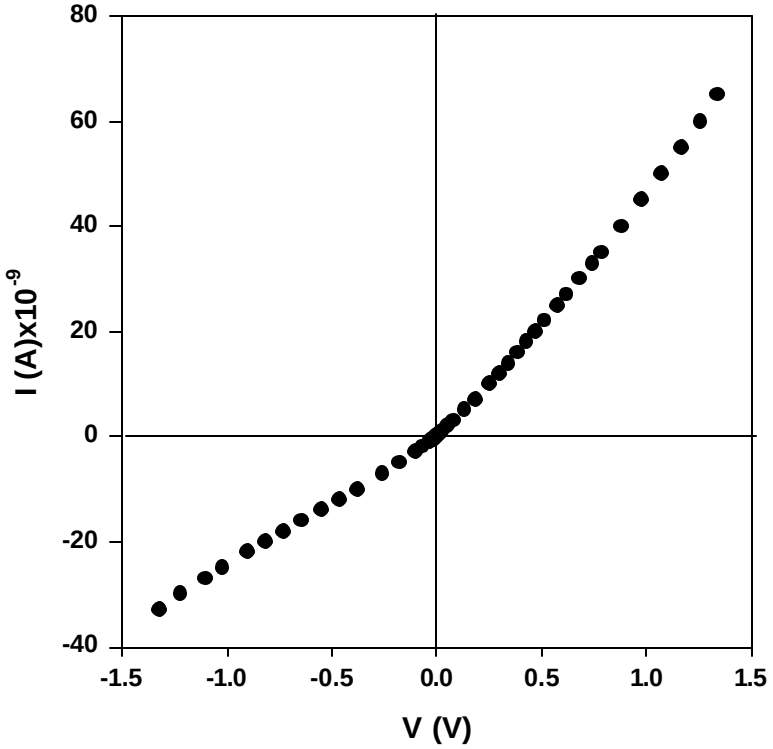


Fig.4.31: The I-V characteristic of Au/a-InSe/Au structure.

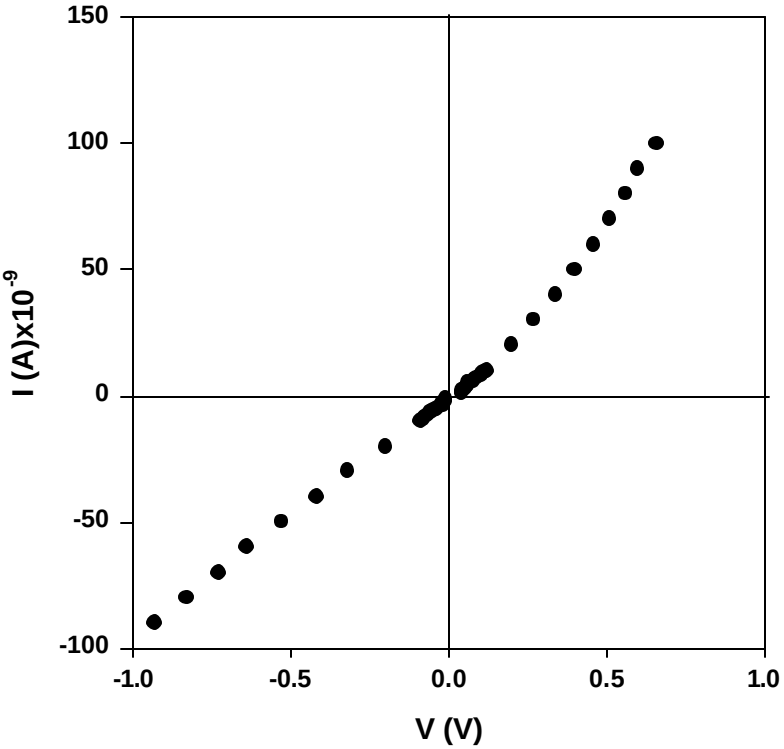


Fig.4.32: The I-V characteristic of In/a-InSe/Au structure.

This unexpected behavior of Au contact can be explained by the complex band structure of the InSe thin films such that p-InSe contains not only acceptor impurities but also deep donor levels. Therefore the ionized impurities coming from a deep donor level causes an increase of the electron concentration in the sample and the electrons from this level are transferred to the gold. Thus, it means that p-InSe acts in this device as if it was n-type [3].

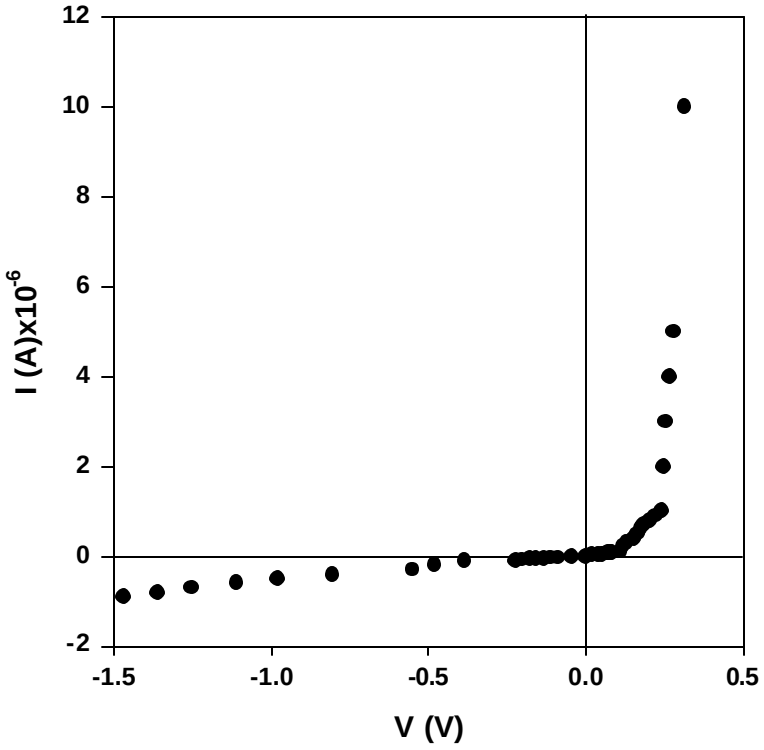


Fig.4.33: The linear I-V characteristic of a rectifying TO/a-InSe/Ag structure.

v) *TO/a-InSe/Ag* structure: This structure exhibited the best rectifying behavior among all the Schottky structures investigated in this work. The device is forward biased when the TO side is made positive with respect to Ag electrode. The forward current increases exponentially with increasing voltage whereas reverse current increases slowly up to the breakdown voltage after which irreversible breakdown occurs. A typical linear current-voltage characteristic of TO/a-InSe/Ag structure is shown in Fig.4.33, and this result is reproducible over the whole surface of the film.

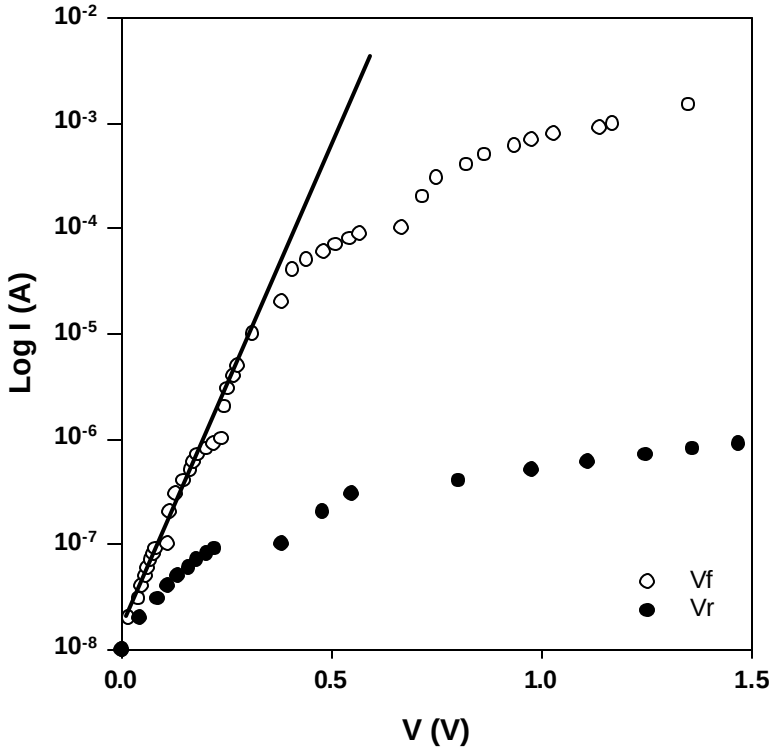


Fig.4.34: The semi-logarithmic plot of I-V for TO/a-InSe/Ag structure.

As seen from Fig.4.34, the forward current indicates a linear region up to around 0.5 V where the forward current increases linearly with increasing voltage, followed by a region in which deviation from linearity occurs due to the series resistance of the device which was found to be around 588 Ω. The forward current is related to the applied voltage for the Schottky barrier diodes is given by the following relation which was discussed in detail in section (2.4.4),

$$I = I_s\left(\exp\left(\frac{qV_a}{nkT}\right)-1\right) \tag{4.6.1}$$

where n is a dimensionless factor representing the diode ideality factor, V_a is the applied voltage and I_s is the saturation current given by the expression,

$$I_s = A^{**}AT^2\exp\left(-\frac{qf_b}{kT}\right) \tag{4.6.2}$$

where A is the area of the diode, A^{**} is the Richardson constant and f_b is the barrier height. The ideality factor and the barrier height were calculated by using Eq.(4.6.1)

and Eq.(4.6.2) from the semi-logarithmic plot of current-voltage characteristic of the diode. The ideality factor and the Schottky barrier height at room temperature were found to be around 2.0 and 0.7 eV, respectively. The deviation from ideality could be related with many reasons such as highly disordered nature of the amorphous film which results in defect states or the current transport mechanisms such as generation-recombination in the depletion region and tunneling through the barrier.

The ideality factor at room temperature is greater than unity ($n \gg 2$) which would reveal that thermal excitation over the barrier is not the transport mechanism. The tunneling through the barrier is possible only in highly doped materials at lower temperatures. Thus, tunneling mechanism is thought to be out of possibility. Recombination in the depletion region seems to be the dominant transport mechanism in the Schottky regime and the recombination occurs through the localized states when the bulk traps are present in the depletion region. At higher voltages following the Schottky regime, the Schottky contact becomes ohmic so that highly resistive InSe thin film is in between two ohmic contacts. Detailed analysis of the current-voltage characteristics will be given according to the SCLC model in the next section.

In order to verify that Ag is a rectifying contact with amorphous p-InSe thin film, In/a-InSe/Ag structure were investigated and the dark current voltage characteristic confirmed that Ag is a rectifying contact with p-InSe thin film as indicated in Fig. 4.35. Since indium is known to be ohmic contact with p-InSe film, Ag is definitely the rectifying contact for this structure.

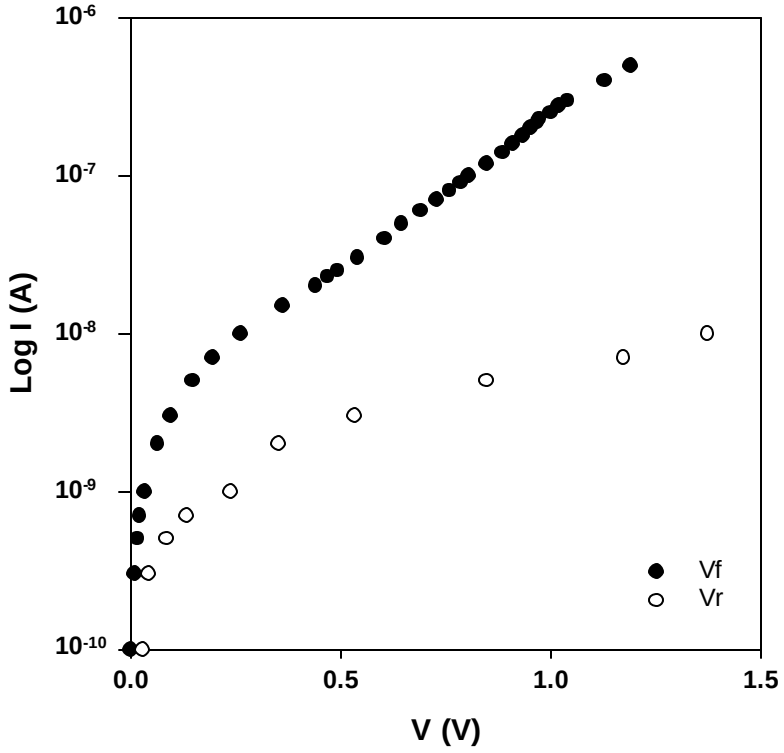


Fig.4.35: The current-voltage characteristic of In/InSe/Ag structure.

4.6.2 Current-Voltage Characteristics Under Illumination

From the dark current-voltage (I-V) measurements of Schottky structures, it was observed that the structure with Ag contacts have shown the best rectifying behavior whereas the gold contacts seems to be slightly rectifying. Dark I-V characteristics of typical Schottky structures TO/InSe/Ag and TO/InSe/Au were given in Fig.4.36 and Fig.4.37, respectively.

The photovoltaic behavior of these Schottky diodes were measured as explained in section (3.2.3) under simulated AM1 conditions. Illuminated I-V characteristics of both structures were given in Fig.4.38 for comparison. As expected from the dark I-V behavior, the TO/InSe/Ag structure has shown better photovoltaic response with open circuit voltage (V_{oc}) around 300 mV and short circuit current (I_{sc}) of 3.2×10^{-7} A.

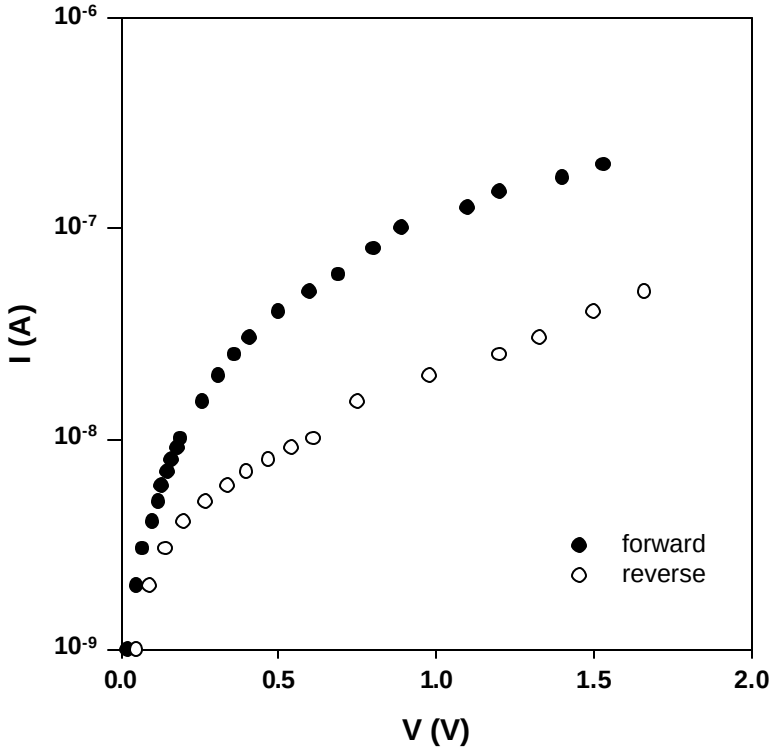


Fig.4.36: Semilogarithmic dark I-V characteristic of a typical TO/InSe/Ag structure.

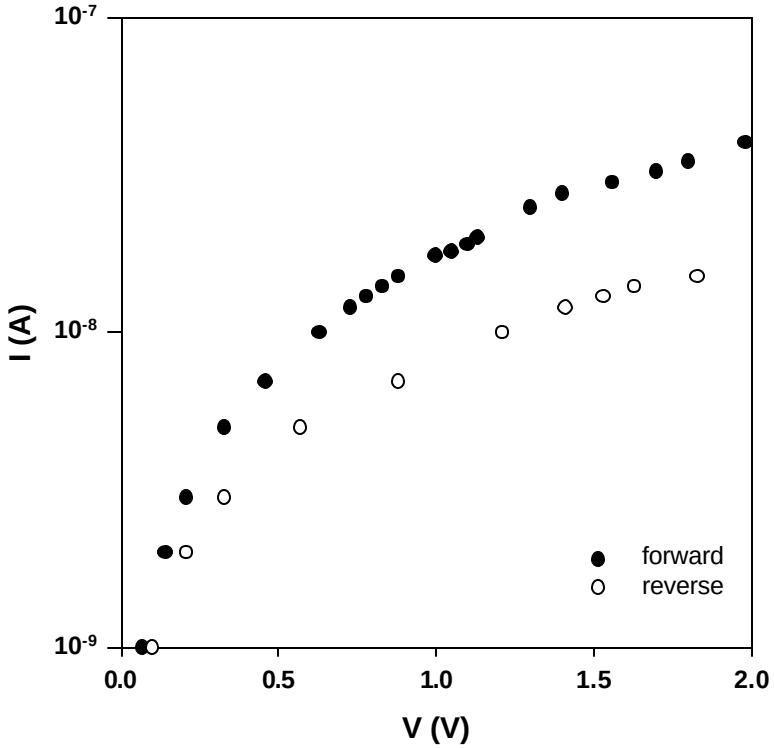


Fig.4.37: Semilogarithmic dark I-V characteristic of a typical TO/InSe/Au structure.

However, unexpectedly, the TO/InSe/Au structure has also shown considerable photovoltaic response with V_{oc} around 230 mV and I_{sc} of $2x10^{-8}$ A. This anomalous behavior may be interpreted as under illumination, donor impurities are ionized which provides increasing donor concentration in the InSe film, thus, the minority carriers become dominant in the structure and form a dominating barrier with Au contact because the electrons from ionized deep donors are transferred to the gold. This result is consistent with the previous work done by Pastor et al. [3].

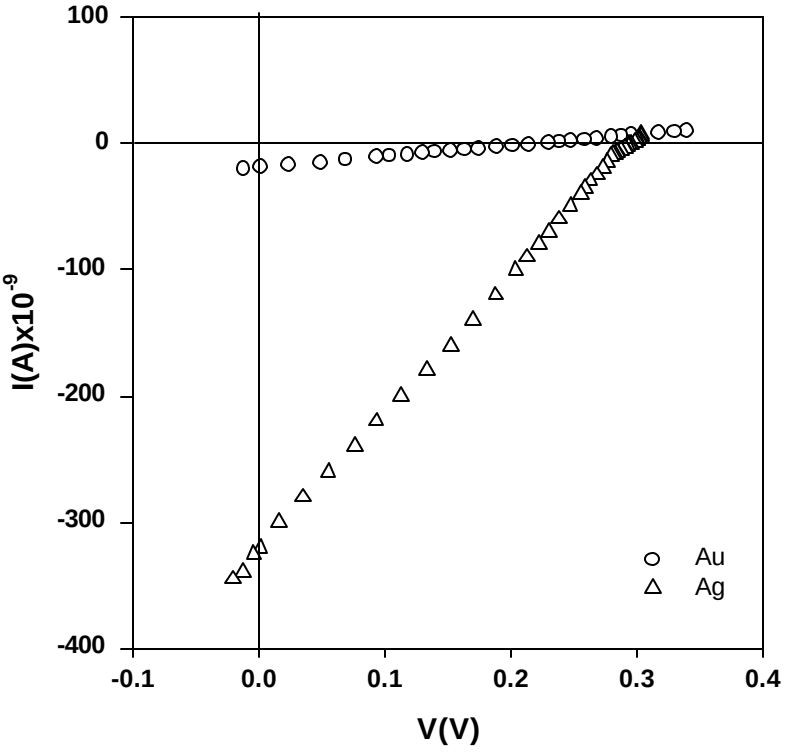


Fig.4.38: I-V characteristic under illumination for Schottky structures with Ag and Au contacts.

Illuminated I-V characteristics for both structures are straight lines due to the high series resistances of the devices which can arise from the resistance of the bulk material and the contacts.

4.6.3 Space Charge Limited Currents

The study of space-charge limited currents (SCLC) in amorphous p-InSe thin films is presented in this section. The temperature dependent current-voltage measurements were carried out for TO/a-InSe/Au sandwich structures in the range of 200-320 K. Following the deposition of the films, Au contacts with area of 7.5×10^{-3} cm^2 were evaporated to achieve the sandwich structures onto the a-Inse/TO film. The measurements were carried out for two samples with thicknesses 1.2 and 1.0 μm. The current-voltage characteristic of a typical sample at room temperature is given in Fig.4.39 in a logarithmic scale.

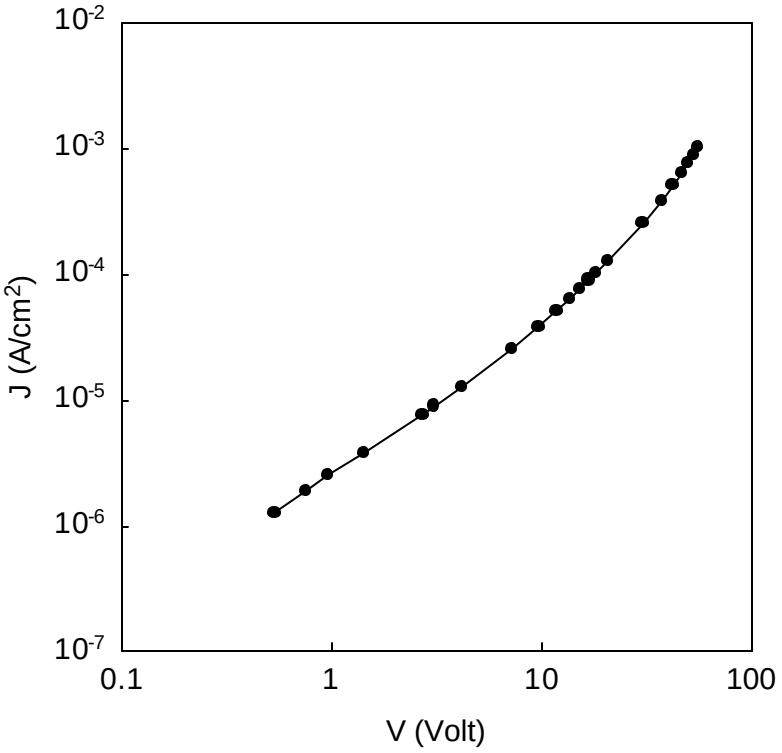


Fig.4.39: Logarithmic plot of current-voltage characteristic for a typical sample at room temperature.

The J-V behavior shows an ohmic region up to 10 V where current is proportional to voltage, followed by a SCLC region, where current is proportional to

V^l with $l=2$. The current-voltage characteristics of the same sample at different temperatures in between 200 and 320 K are illustrated in Fig. 4.40.

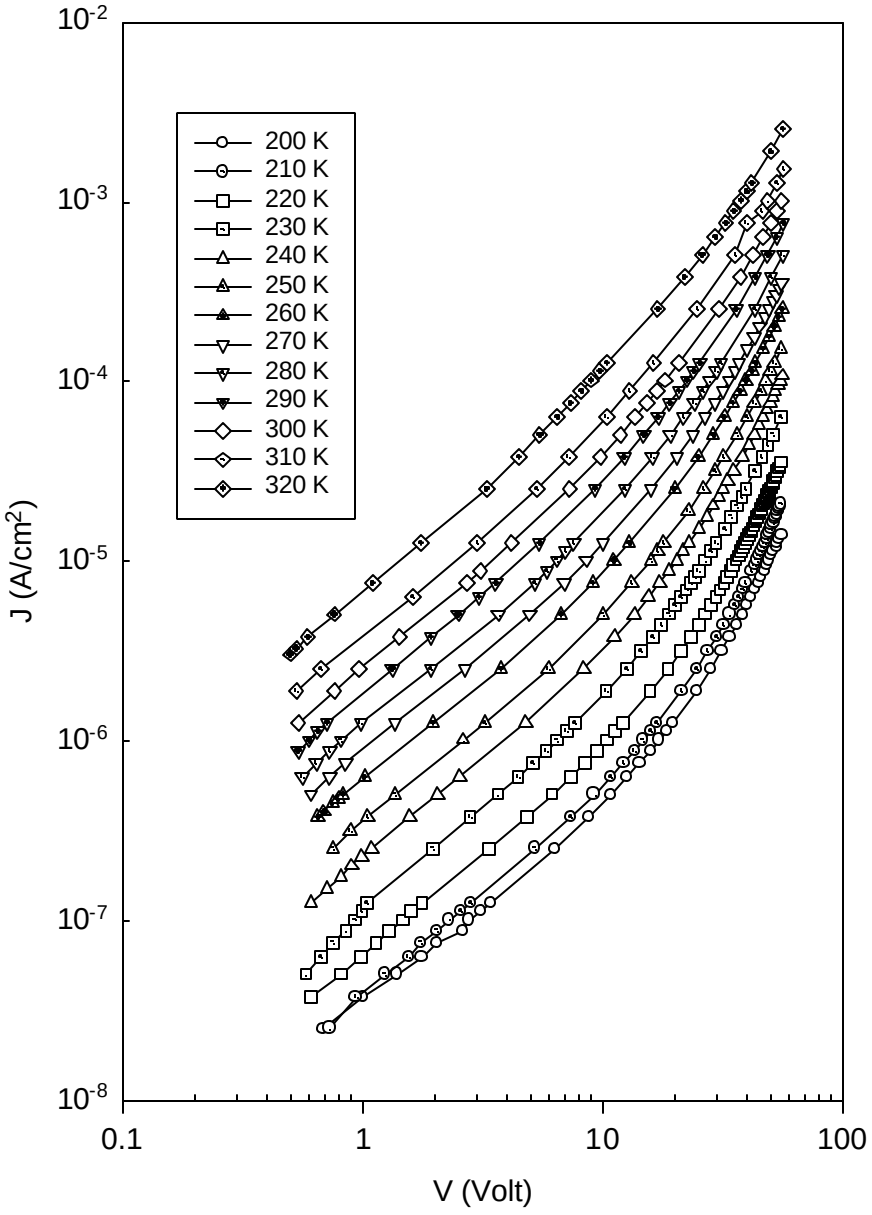


Fig.4.40: Log(J) versus Log(V) plots for a typical sample at different temperatures.

Current increases at each constant voltage with absolute temperature and all J-V characteristics yield the two conduction regions depending on the measurement temperature. For the studied samples, the proportionality constant l in the SCLC region changes between 2 and 2.9 with temperature.

For the amorphous semiconductors, when the density of states is high, the current at high electric fields might be affected by the Poole-Frenkel effect [100], which is the enhancement of thermal emission of carriers from deep traps due to the lowering of the potential barrier through an external electric field. Then, the determination of the density of states from the SCLC studies is not reliable. The net lowering of the emission barrier is $(qe/\pi\varepsilon_s)^{1/2}$, and the current increases as the following relation,

$$I = I_{\Omega} \exp\left(\frac{\sqrt{qe/pe_s}}{kT} \right) \tag{4.6.3}$$

where I_{Ω} is the current in the ohmic region, e is the electric field, and e_s is the dielectric permittivity of the semiconductor. In order to check whether the Poole-Frenkel effect is favorable or not , I-V characteristics were replotted in the high voltage region as Ln(I/V) versus $(V)^{1/2}$ for two different samples with different thicknesses and are illustrated in Fig. 4.41. The non-linearity of these plots verifies that the Poole-Frenkel effect is absent and the SCLC is the transport mechanism operating in the amorphous InSe films under study. At high voltages, in the SCLC regions, the voltage exponents were found to be greater than 2, which indicates energy distributions of traps instead of discrete levels. For the determination of trap distribution in energy, the analytical method proposed by Pfister [101], which leads directly to the trap distribution from the I-V characteristics, was used. This method which was later developed by Manfredotti et al. [102] and Stockman [103], refined by Weisfield [104], uses the following assumptions: *(a)* the distance *L* between the two metal contacts is constant, *(b)* the DOS and the mobility μ are assumed to be uniform and field independent, *(c)* the trap occupancy is determined by the position of the equilibrium Fermi level E_{f0}, *(d)* the gap state density *N(E)* varies slowly and continuously over energies of the order of kT, *(e)* the current density is uniform.

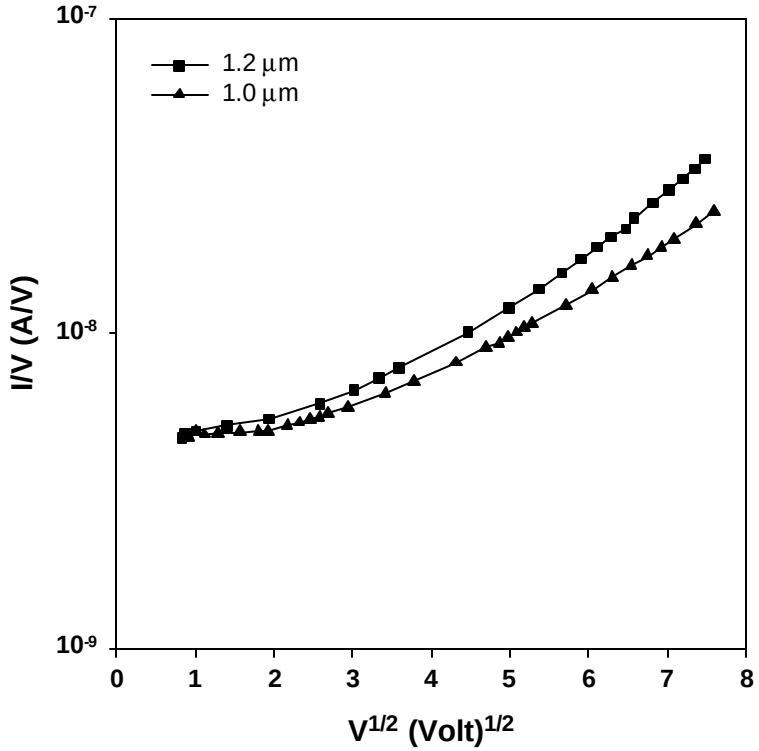


Fig.4.41: The plot of Ln(I/V) vs. $(V)^{1/2}$ for the Poole-Frenkel effect.

By using these assumptions and the Poisson's equation, the expression for the free carrier concentration and total charge density at the anode are obtained. Simultaneous solution of the obtained expressions and differentiation of the charge density, gives the information about the energy distribution of the traps. Thus, the gap state density is given by [104],

$$N\left(E_{f0}+\Delta E_f\right)=\frac{Ve_s}{qkTL^2}\left[a\left(2-a\right)+\frac{g-b\left(3-2a\right)}{1-a+b/\left(2-a\right)}\right] \qquad (4.6.4)$$

where $e_s=k_s e_0$ is the dielectric permittivity of InSe, k_s is the dielectric constant, e_0 is the permittivity of vacuum, L is the thickness of the film, k is the Boltzmann constant, T is the absolute temperature and a, b and g are defined by the following expressions,

$$a=\frac{d\left(LogV\right)}{d\left(LogJ\right)} \qquad b=\frac{d^2\left(LogV\right)}{d\left(LogJ\right)^2} \qquad g=\frac{d^3\left(LogV\right)}{d\left(LogJ\right)^3}$$

DE_f is the position of the quasi-Fermi level which is calculated by the following relation,

$$E_f - E_{f0} = kT\left[Log\left[\frac{V(2-a)}{J}\right] - Log\left(\frac{V_\Omega}{J_\Omega}\right)\right] \qquad (4.6.5)$$

Here, J_Ω is the current density of the critical voltage (V_Ω) that is located at the region where the ohmic behavior ends, $I_\Omega = qp_0\mu(V_\Omega/L)$ and p_0 is the thermal equilibrium density of free holes. To obtain the position of thermal equilibrium Fermi level E_{f0} with respect to the valence band edge E_v, the temperature dependence of conductivity above 200 K was obtained from the ohmic current values at different temperatures. The variation of conductivity with temperature for the typical a-InSe film is shown as Ln(σ) versus 1000/T in Fig. 4.42.

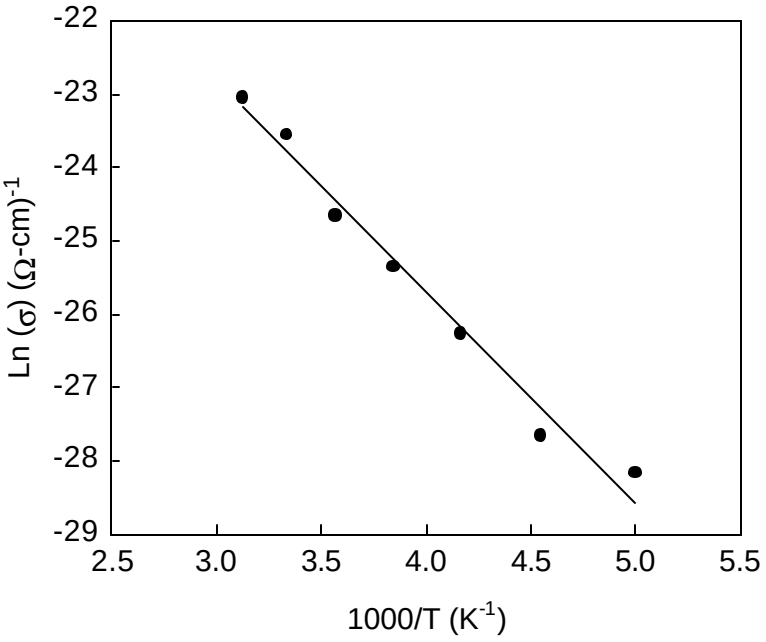


Fig.4.42: Variation of conductivity with inverse temperature.

The conductivity variation with respect to inverse temperature was analyzed by the following expression where E_s denotes the conductivity activation energy.

$$s = s_0 \exp\left(-\frac{E_s}{kT}\right) \qquad (4.6.6)$$

As seen from Fig.4.42, the plot showed activated behavior with an activation energy E_s =250 meV, which is in agreement with the value obtained for the coplanar configuration in a previous study [21].

To calculate *N(E)* and E_f from Eq.(4.6.4) and Eq.(4.6.5), experimental I-V data at 300 K was replotted as J-V to get a cubic polynomial, as shown in Fig.4.43.

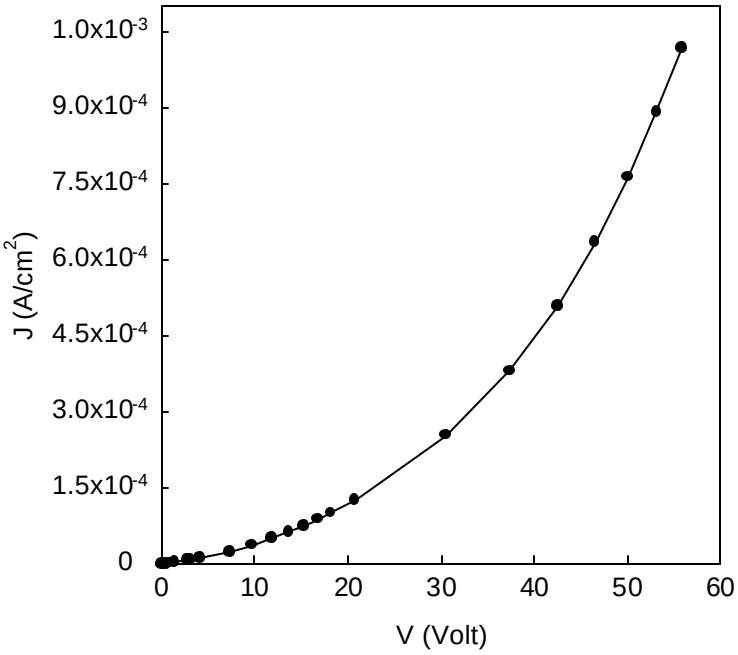


Fig.4.43: Current-Voltage dependence at 300 K.

The function has sufficient curvature to calculate the necessary derivatives. The curve-fitting processes were applied together with the smoothing parameters such that the calculated derivative is the same as the slope of the experimental plot. The calculated DOS values were plotted in the energy range of 190-250 meV in Fig.4.44. The position of E_{f0} is taken as 0.25 eV above the valence band E_v. As observed from the figure, the density of states changes with energy in the range of 3.82 x10^{17}-1.73 x 10^{18} $eV^{-1}cm^{-3}$ and the variation of the energy distribution of DOS at each temperature is the same, and almost uniform over the energy range given. The temperature dependence of DOS is given in Fig.4.45 as Ln(*N(E)*) versus *1/kT* from which *N(E)* is observed to be almost temperature independent.

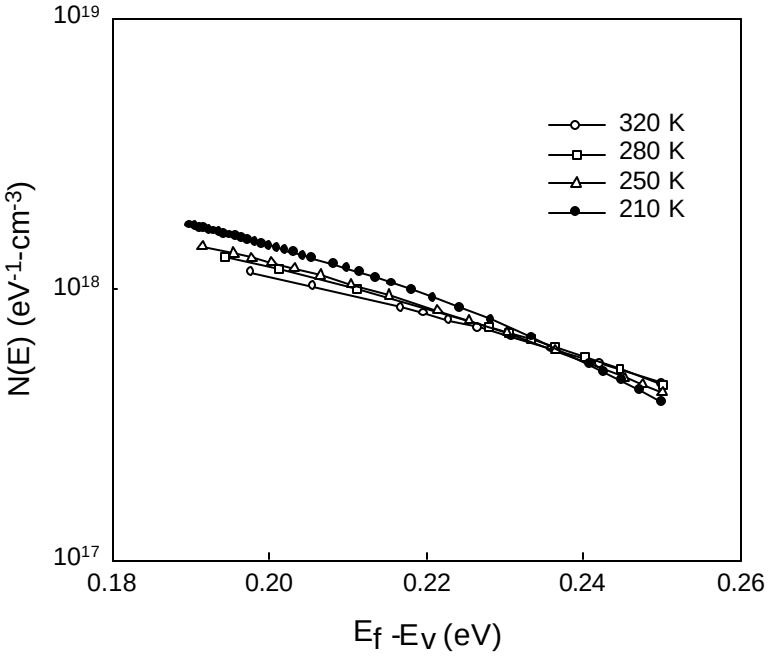


Fig.4.44: Ln(N(E)) versus (E_f-E_v) at different temperatures.

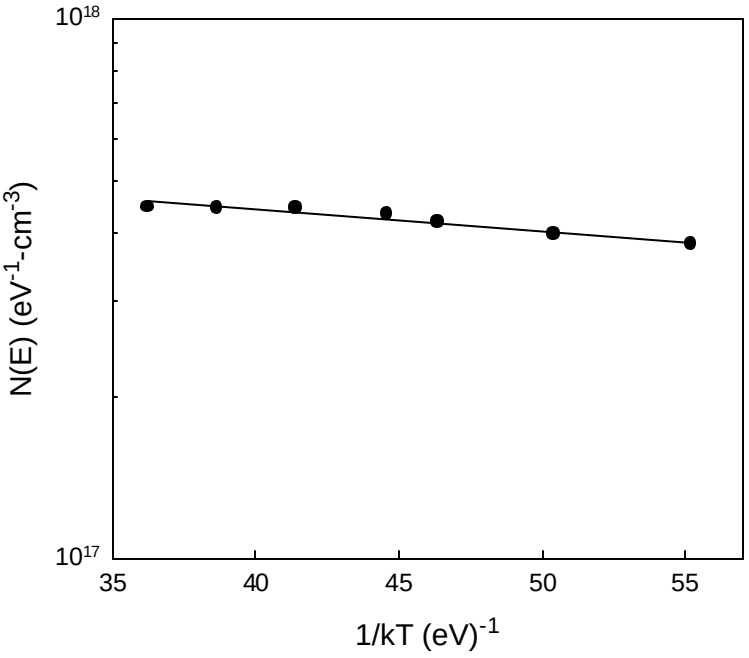


Fig.4.45: Variation of density of states with 1/kT

These results implied that SCLC in amorphous InSe thin film is related with the bulk and not with the contact and/or the formation of a surface layer and also verifies the assumptions used to obtain the analytical expression for the gap state density *N(E)*.

For further verification of the SCLC regime after critical voltage, the thickness scaling law was checked. Lampert and Mark [82] have shown that if the SCLC mechanism is valid, the I-V characteristics must satisfy the expression given by $I/L=f(V/L^2)$ for the samples with different thicknesses but identical electrical properties. This law is somewhat difficult to test exactly due to experimental difficulties in producing the films with identical electrical properties with different thicknesses. In this study, the deposition of a-Inse films in different thicknesses was carried out in a single run by using a double shutter assuming that the films grown at the same rate onto all substrates. To test the thickness scaling law , Log(I/L) versus $\log(V/L^2)$ were plotted as in Fig.4.46, for films having thicknesses 1.2 and 1.0 μm.

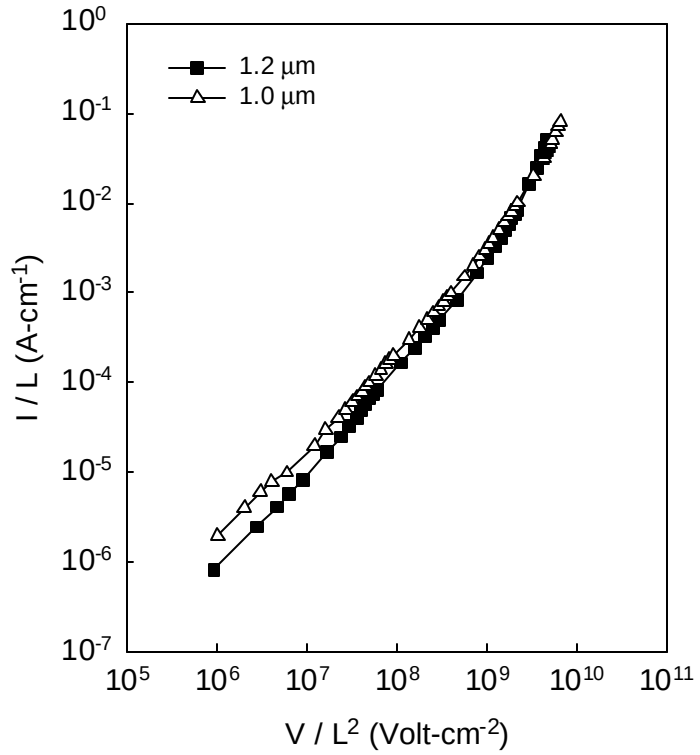


Fig.4.46: Log(I/L) versus $\text{Log}(V/L^2)$ for thickness scaling test.

As seen from the plot, the variation coincides exactly which means that the samples have SCLC characteristics that scale reasonably well with thickness. As a result of this study, the calculated $N(E)$ values are found to be temperature independent, indicating that the SCLC in the deposited amorphous InSe films is related to the bulk, not the surface layer between the contact and the film [105].

4.6.4 Capacitance-Voltage Characteristics

As discussed in section (2.4.6), the capacitance-voltage characteristic of a metal-semiconductor junction yields information on the barrier height of the junction and the acceptor concentration of the semiconductor. In this technique, the diode capacitance is measured as a function of applied reverse bias. Measurement of the depletion region capacitance under forward bias is difficult since the diode is highly conducting due to the lowering of the barrier and the capacitance is shunted by a large conductance in this case. When a small ac voltage is applied to a reverse bias diode the depletion region capacitance C can be found by the Eq.(2.4.15) with the assumptions that there is no interfacial layer (i.e. oxide layer) between the semiconductor and metal. Also, it was assumed that the p-type semiconductor has a uniform acceptor concentration. With these assumptions, the width of the depletion region can be obtained from the solution of the Poisson's equation and given by Eq.(2.4.13) by using the abrupt junction approximation. A change in the voltage across the junction causes a change in the width of the depletion region which also results in the movement of charge carriers into or out of the space charge layer. The change of amount of charge in the depletion region gives rise to a capacitance.

It can be seen from Eq.(2.4.15), the plot of C^{-2} versus V_R gives a straight line with a slope of $(2/A^2 e_s q N_A)$ which leads the determination of acceptor concentration. The intercept at the voltage axis yields $V_0=(V_{bi}-kT/q)$ where V_{bi} is the built-in potential. The barrier height can then be calculated as (qV_0+kT-f_n) where f_n is the penetration of the Fermi level in the band gap of the semiconductor. In the case where N_A is not uniform in the depletion region, C^{-2} versus V plot does not give a straight line but still the slope at any point of the characteristic will be given by $(2/A^2 e_s q N_A(w))$ where $N_A(w)$ represents the dopant concentration which varies with

the distance into the semiconductor. Thus by measuring the slope at a given depth from the surface will yield the impurity concentration at that point.

The room temperature C^{-2} versus V variation of a typical TO/a-InSe/Ag Schottky diode is shown in Fig.4.47 at 10 kHz frequency.

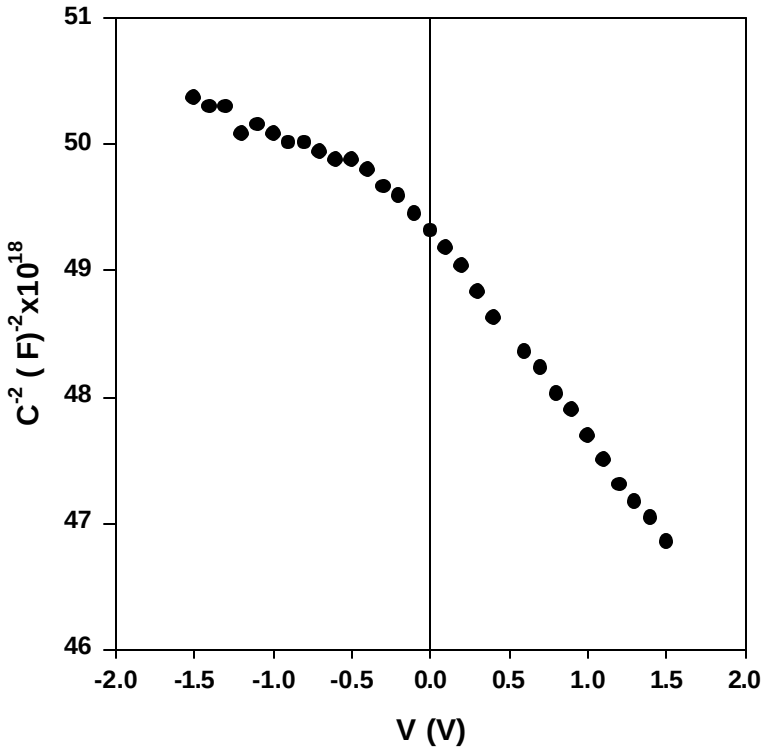


Fig.4.47: The plot of C^{-2}-V at 10 kHz under reverse bias of the Schottky diode.

As seen from the plot, the junction capacitance is almost independent of the applied reverse bias indicating that almost whole thickness of the semiconductor may be depleted because of high resistivity of the InSe. Since the capacitance variation was found to be independent of the applied reverse bias the built-in voltage, barrier height and the acceptor concentration values could not be derived from the Fig.4.47.

Capacitance-voltage measurements as a function of frequency have been carried out in the range of 1-1200 kHz at room temperature and it is observed that the C-V variations at different frequencies are weak but capacitance changes with

frequency at each voltage value. As illustrated in Fig.4.48, the dependence of capacitance on frequency at zero bias is relatively strong at low frequencies indicating the presence of high interface states responding to the ac signal thus generating higher capacitance. The number of interface states (N_{IS}) can be roughly estimated by using the following expression [61],

$$N_{IS} = \frac{(C_L - C_H)}{q} \tag{4.6.7}$$

where C_L and C_H denotes the low and high frequency capacitance values, respectively. The capacitance values at low frequencies are usually due to the total number of states of the depletion and interface regions whereas the high frequency capacitance values are only due to the number of states in the depletion region. Thus, this expression roughly gives the number of total interface states. At zero bias and room temperature, the number of interface states was calculated from the high and low capacitance values to be 1.9×10^8 $cm^{-2}V^{-1}$.

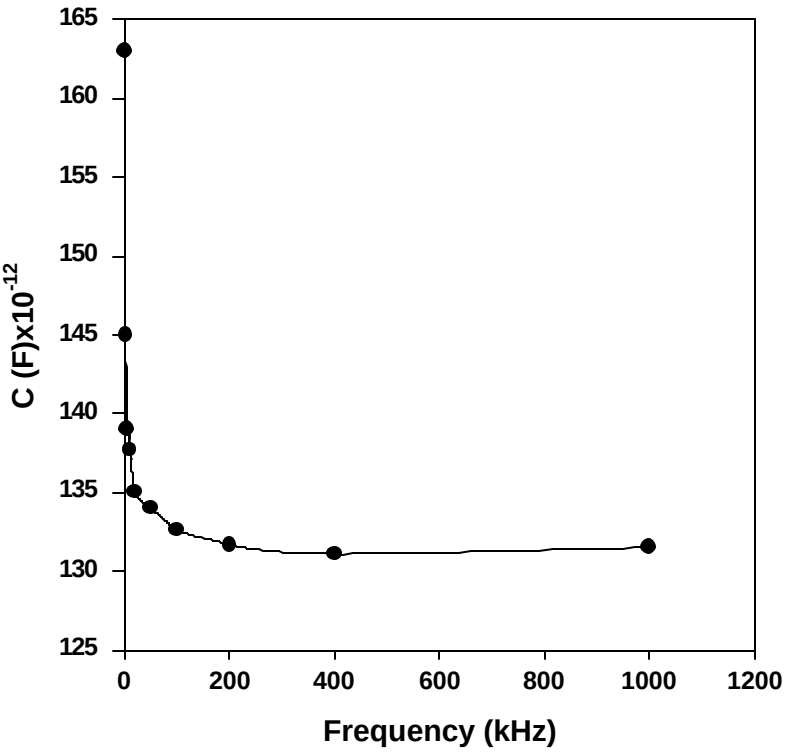


Fig.4.48: The variation of capacitance as a function of frequency at zero bias.

4.6.5 Spectral Response

The photo-response of TO/p-InSe/Ag structure was measured in the wavelength region of 450-900 nm as explained in section (3.3). The photo-response spectra obtained was corrected for the spectral distribution of the light source used for illumination. The typical spectral distribution for this structure as a function of photon energy is shown in Fig. 4.49.

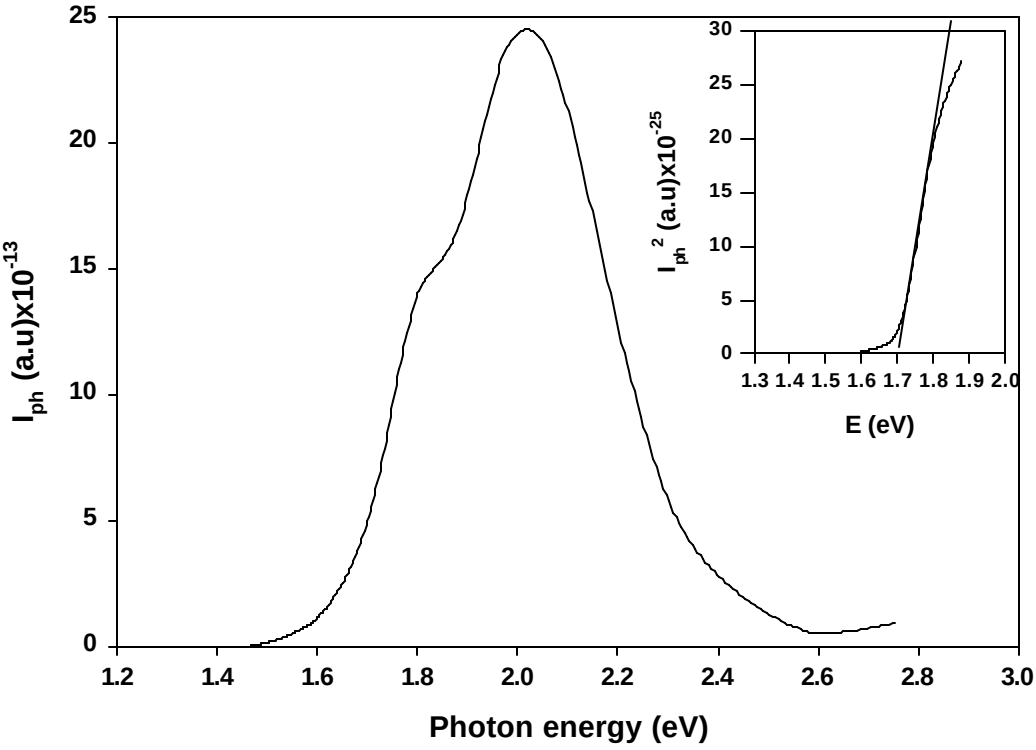


Fig. 4.49: Spectral response of a typical p-InSe/Ag Schottky diode.

I_{ph}-hν dependence shows a broad distribution between the photon energies of 1.5-2.5 eV. The short circuit photocurrent increases gradua lly with increasing incoming photon energy after the long wavelength threshold followed by a sharp increase corresponding to the transition between the band tails. The curve goes through a small shoulder around 1.8 eV which may be related with interface states. The photocurrent starts to decrease after 2 eV with increasing energy of the incoming

photons because the photons at these energies are absorbed at or near the surface where recombination velocities are higher than that of the bulk of the semiconductor.

The photocurrent created by the photons with energies larger than band gap of the semiconductor per absorbed photon as a function of the photon energy is described by Fowler [87]. According to this theory, the photocurrent is directly proportional to absorption coefficient. Therefore, created photocurrent for photon energies $h\nu > E_g$ can be related to the band gap of the semiconductor as the following relations,

$$I_{ph}^{2} \propto \left(h\nu - E_g\right) \tag{4.6.8}$$

for direct gap optical excitation and,

$$I_{ph}^{1/2} \propto \left(h\nu - E_g\right) \tag{4.6.9}$$

for indirect gap optical excitation. The plot of I_{ph}^{2}-$h\nu$ in the vicinity of the band tail region reveals the optical band gap of a typical InSe film as indicated in the inset of Fig.4.49. Optical band gap value obtained as 1.7 eV is consistent with the one calculated from the transmission measurements.

4.7 Characterization of TO/CdS/InSe/Metal n-p Heterojunction Solar Cells.

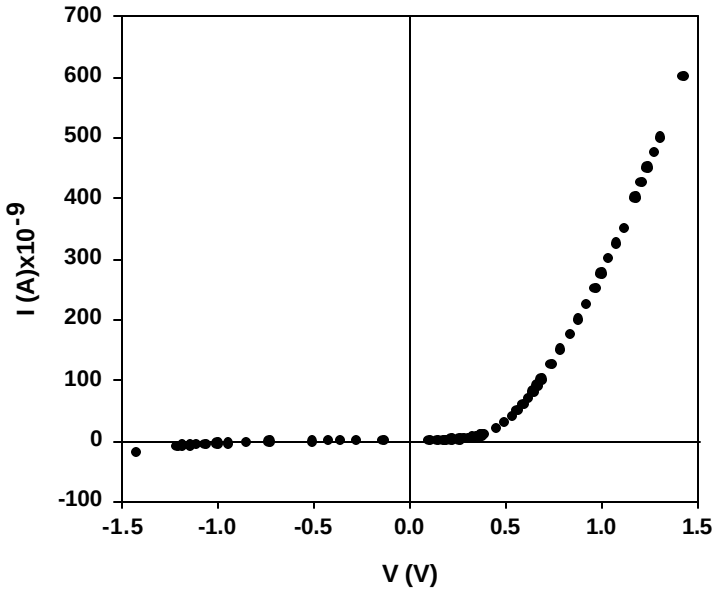
In this section, results of the experimental studies on TO/CdS/InSe/Metal n-p heterojunction devices are presented. Dark and Illuminated I-V, C-V and spectral response measurements were carried out to determine the device parameters. In order to fabricate the n-CdS/p-InSe heterojunction, first of all, CdS thin films were deposited onto TO coated glass substrates which were kept at 200 ^{0}C. Following the deposition of CdS thin films, InSe thin films were deposited onto TO/CdS films where CdS thin films used as the window layer and InSe thin films used as the absorber layer. For the top ohmic contacts, various metals such as Au, C, In, Al and Ag were thermally deposited onto TO/CdS/InSe structure as to form the n-p heterojunction solar cells. Schottky diode structures with the same metals have shown previously that C, In and Al make well ohmic contacts to the p-type InSe films grown in this work, whereas Au makes almost ohmic contact. The only well

rectifying diode structure obtained with Ag top contacts. Among all the metals deposited as top ohmic contact, heterojunctions with Au and C contacts have shown the best photovoltaic behavior. Therefore, in this section TO/CdS/InSe/Au and TO/CdS/InSe/C heterojunction solar cells were studied in detail through the electrical and optical measurements.

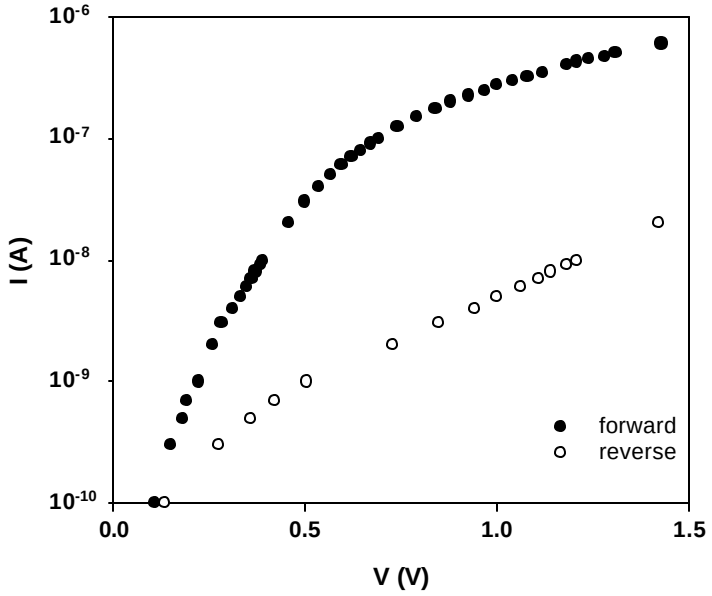
4.7.1 Dark and Illuminated I-V Characteristics.

The dark and illuminated I-V characteristics of both TO/CdS/InSe/Au and TO/CdS/InSe/C structures were investigated to determine the diode and the solar cell parameters of the devices. Both samples have shown diode characteristics which can be fitted to the standard diode equation given by Eq.2.4.1.

a) *TO/CdS/InSe/Au solar cells*: The I-V variations in the linear and semilogarithmic plots are given in Fig.4.50(a) and Fig. 4.50(b), respectively. The forward current of the TO/CdS/InSe/Au solar cell increases exponentially with the increasing applied voltage by at least two orders of magnitude of current. The diode ideality factor of this structure was found to be n= 2.4 with a reverse saturation current of the order of $3x10^{-11}$A.



(a)



(b)

Fig.4.50: Dark current-voltage behavior for a typical TO/CdS/InSe/Au structure as (a) linear, and (b) semilogarithmic plot.

The dark I-V characteristics have shown that the ideality factor remains unchanged with annealing at 100 ^{o}C, however, due to the slight decrease in the resistivities of the films linear region of the current became more observable in which region the curve fits to the diode equation. Further annealing above 100 ^{o}C was avoided, because it was found in section (4.2.1) from the conductivity measurements of the InSe films that above this temperature the conductivity of the films convert from p-type to n-type.

The current-voltage characteristics of the TO/CdS/InSe/Au structures under illumination that correspond to simulated AM1 condition which is about 100 mW/cm^2, given in Fig. 4.51.

The open circuit voltage V_{oc} is around 400 mV whereas the short circuit current I_{sc} is 4.9x10^{-8} A. The efficiency of this solar cell is quite low due to the small short circuit current. The value of the fill factor for the same device was calculated by Eq.2.5.26 and found to be 0.44.

Doping effect on the device performance was also investigated but it was found that solar cells produced with the Cd doped InSe films have shown the poorest photovoltaic behavior.

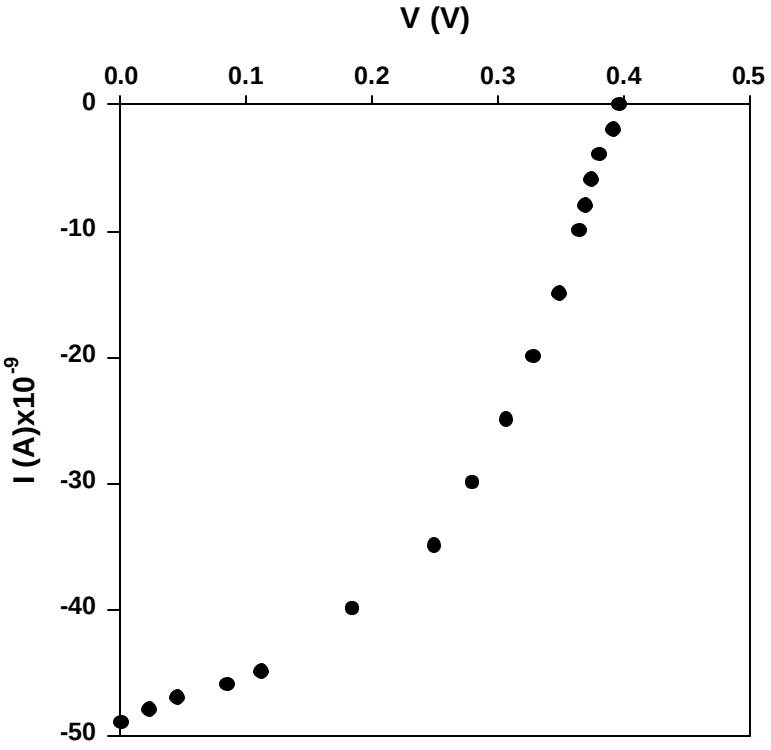


Fig.4.51: The linear I-V characteristics of TO/CdS/InSe/Au solar cell under illumination.

b) *TO/CdS/InSe/C solar cells*: The dark and illuminated I-V measurements of this structure have shown similar photovoltaic behavior to TO/CdS/InSe/Au structure as seen in Fig.4.52 and Fig.4.53.

The diode ideality factor was calculated to be n= 2.95 with a reverse saturation current around $2x10^{-11}$A at room temperature. The illuminated I-V behavior is almost linear which indicates the presence of high series resistance effect on the device.

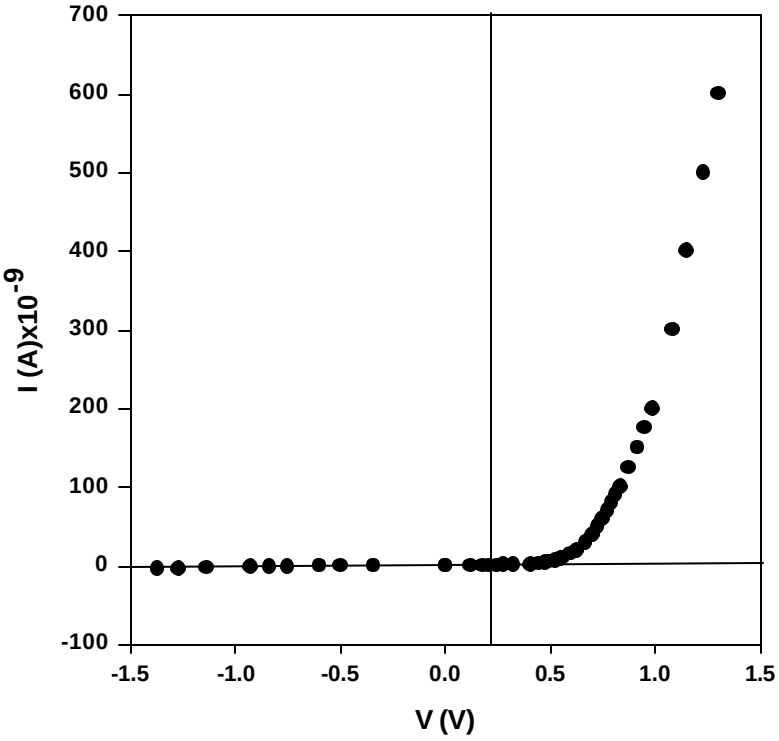


Fig.4.52: The dark I-V characteristic of TO/CdS/InSe/C solar cell.

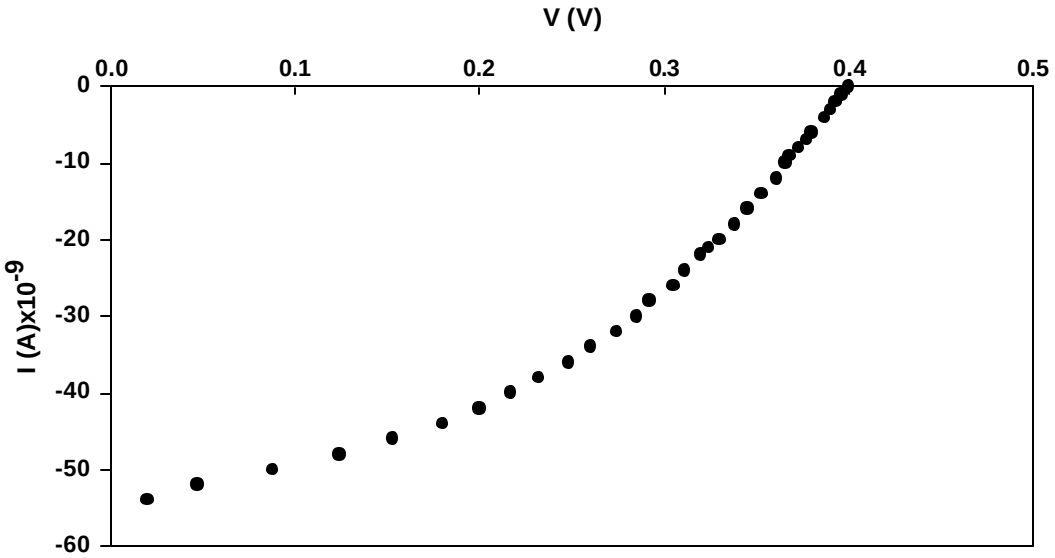


Fig.4.53: The illuminated I-V characteristics of TO/CdS/InSe/C solar cells under simulated AM1 conditions.

The open circuit voltage V_{oc} and short circuit current I_{sc} were found to be around 400mV and $5.4x10^{-8}$A which resulted in low efficiency. The filling factor (*FF)* of the device was determined to be 0.41.

4.7.2 Capacitance-Voltage Characteristics.

As discussed in section (2.5.5), the capacitance-voltage studies have been widely used to understand the junction region structure and the effects related to interface states and deep levels. For an abrupt heterojunction for which the impurity concentration changes abruptly from donor impurities to acceptor impurities, the electric field in the neutral regions of the semiconductors at equilibrium must be zero such that the total negative charge per unit area in the p-layer must be exactly equal to the total positive charge per unit area in the n-layer, thus space charge regions on either side are formed. Capacitance-voltage characteristic of such a junction is expressed by the Eq.(2.5.27). It is clearly seen from this equation that the intercept of the plot of C^{-2} versus applied voltage on the voltage axis yields the built-in potential of the junction. If the doping concentration of one side is known, the doping concentration of the other side can be determined from the slope of C^{-2}-V plot. Therefore, the analysis of the C-V characteristics of a heterojunction as a function of applied bias gives information on the depletion region potential and the charge distribution. As discussed in section (4.6.4), the measurement of the depletion region capacitance is difficult under forward bias since the capacitance is shunted by a large conductance. Therefore, the capacitance is measured as a function of applied reverse bias.

Room temperature dark C-V measurements were carried out for the TO/CdS/InSe/Au and TO/CdS/InSe/C structures at various frequencies and similar behaviors were observed for both. The typical capacitance-voltage characteristic of a TO/CdS/InSe/Au solar cell is shown in Fig.4.54 in the frequency range of 1kHz-2 MHz. The capacitance at low frequencies decreases with decreasing voltage for the forward bias, but in the reverse bias region remains almost constant due to high resistance of InSe film. C-V dependence is weak at high frequencies.

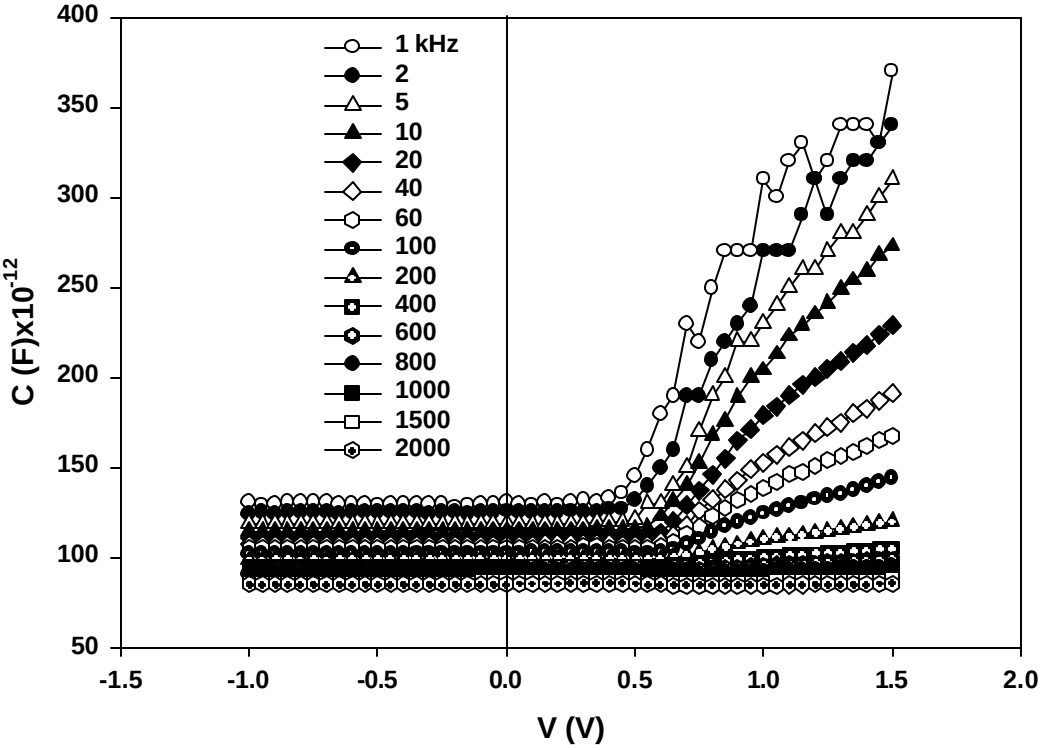


Fig.4.54: The C-V variation of a TO/CdS/InSe/Au solar cell at various frequencies.

The C^{-2} versus voltage variation is plotted in order to find the built-in potential of the junction as seen in Fig.4.55. We observed that capacitance-voltage dependence shows slow variation up to 0.4 V, and after this point there is pronounce increasing of the capacitance with voltage at forward bias. This implies that both sides of the heterostructure are depleted, however, because of the high resistivity of InSe as compared to the CdS, we are only observing the decreasing depletion layer on the CdS side.

The plot also indicates that the slopes of the linear variations increase with increasing frequency. The built-in potential values were found to vary in the range of 0.85-1.10 V as the measurement frequency increases from 1 to 20 kHz which is explained through the effect of the interface states. These built-in potential values are higher than theoretically expected value of 0.7 V (E_{gCdS} - $E_{gInSe} \cong$ 2.4-1.7 eV). This difference can be explained by the presence of a relatively thick interfacial layer.

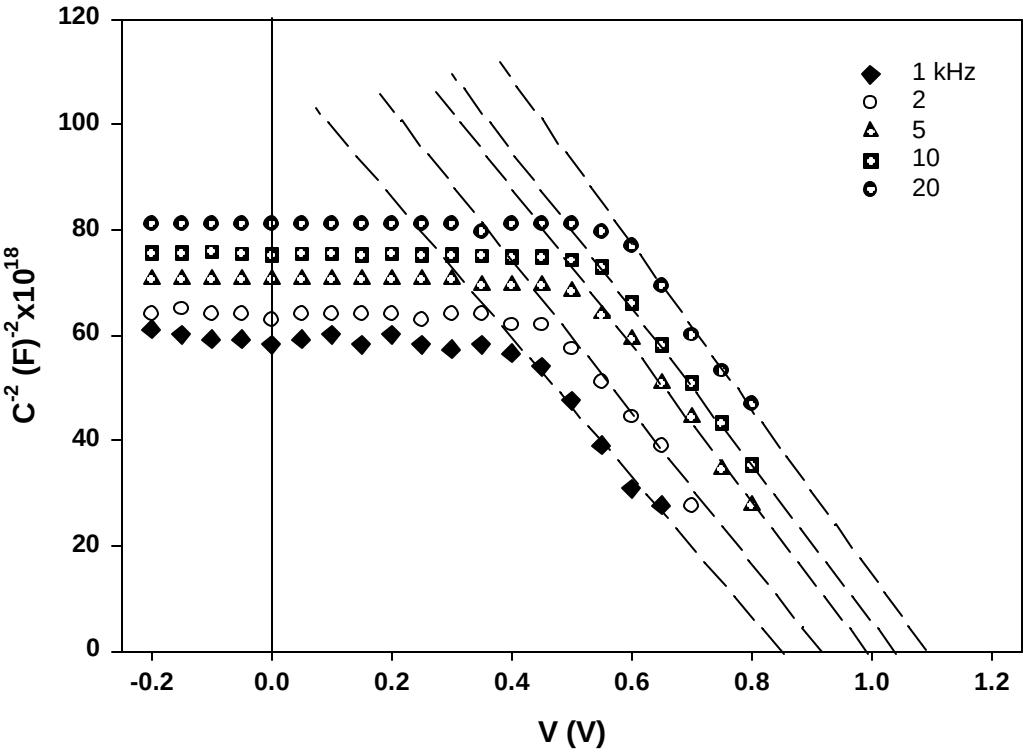


Fig.4. 55: The C^{-2}-V variation at different frequencies.

Further verification of the presence of high interface states is shown in Fig.4.56 as capacitance-frequency variation at zero bias. The plot shows that the frequency dependence of the capacitance is strong at low frequencies than that of the high frequencies which is clearly due to the high concentration of interface states. The capacitance variations at high frequencies are small because the ac signal at these frequencies can no longer be followed by the interface states. The number of interface states can be estimated roughly by the Eq.(4.6.7) by using the values of low and high frequency capacitance values at zero bias and it was found to be of the order of 2.86×10^{8} $cm^{-2}V^{-1}$. Actual number of interface states may be higher than the obtained value since the minimum measurement frequency was not low enough to determine the saturated capacitance value for the device.

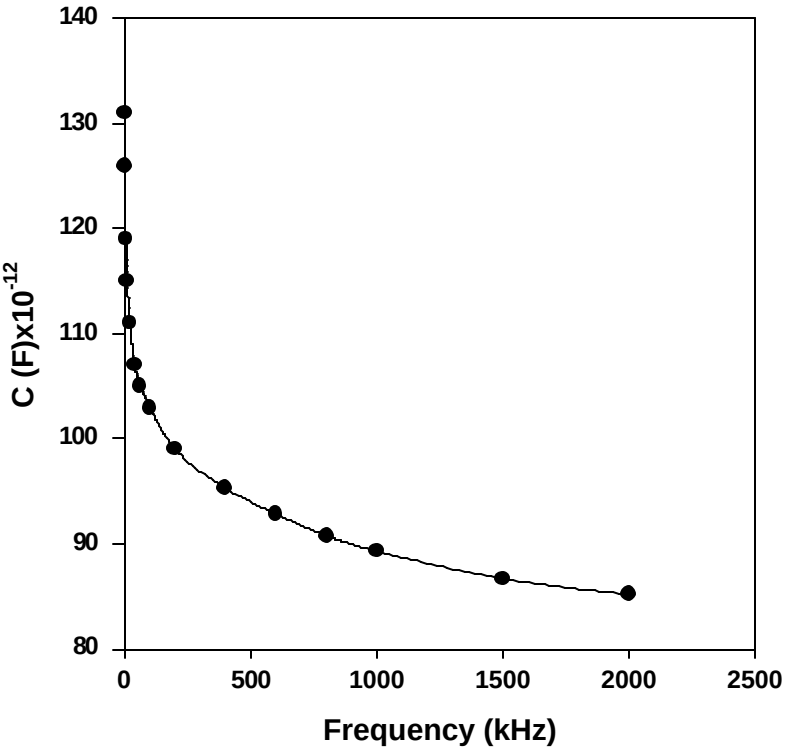


Fig.4. 56: The Capacitance-Frequency variation in the range of 1 kHz-2 MHz at zero bias.

The C-V results presented here have shown that proper n-p heterojunction was not formed due to high resistivity of the InSe and high concentration of interface states at the junction. Thus, further analysis of the capacitance data could not be done for the sample.

4.7.3 Spectral Response

The photo-response of TO/CdS/InSe/Au solar cell was measured in the wavelength region of 450-900 nm under the illumination from the window layer side which is CdS. The obtained spectral distribution was corrected for the spectral distribution of the light source used for the illumination. The typical spectral distribution for this structure as a function of photon energy is shown in Fig.4. 57.

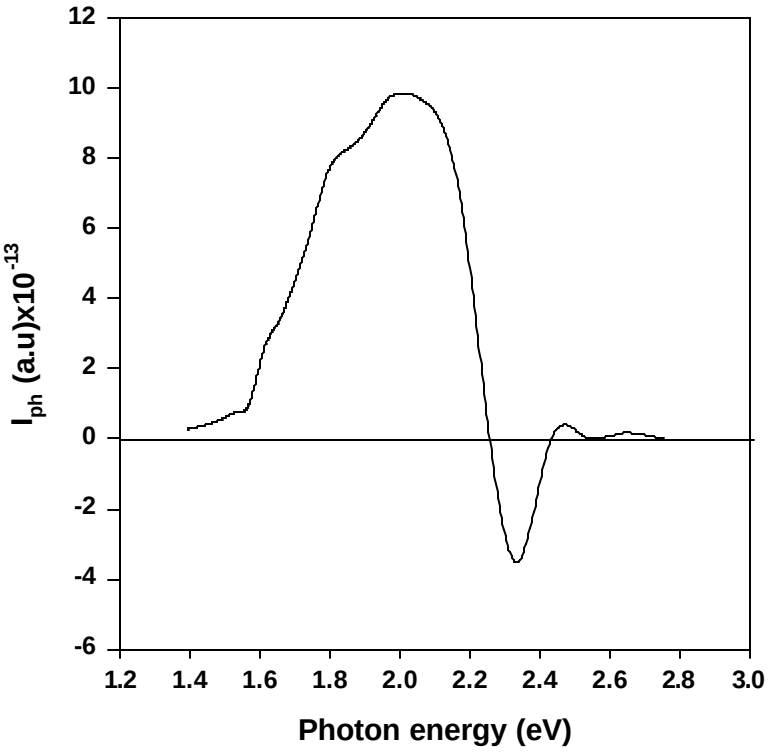


Fig.4. 57: The spectral distribution of n-CdS/p-InSe solar cell at zero bias.

As seen from the plot, the low energy threshold of the cell obtained around 1.5 eV and the photocurrent gradually increases as the energy of the incoming photons increase sharply up to a shoulder located at around 1.8 eV. This small shoulder may be associated with the interface states at or near the junction region. After this point, the photocurrent peaks at around 1.9 eV due to the band-to band excitation in InSe. Then, a sharp cut-off with the increasing photon energy was observed which may be associated with the high recombination rates of the interface states. After the sharp cut-off photocurrent changes sign and starts increasing up to 2.34 eV at which point direct band-to-band transition in CdS takes place. When the photon energies exceeds the band gap value of the CdS the photocurrent gradually decreases because photons with these energies are absorbed at or near the surface of the CdS where recombination velocities are higher than that of the bulk of the CdS. The change of the sign in photocurrent indicates that the dark current at some point becomes comparable or greater than the current obtained under illumination. After

around 2 eV, while dark current increases the current under illumination decreases and, these two currents become equal at around 2.2 eV. This can be interpreted as the effect of majority carriers because due to the interface states the minority photo-carriers may be assumed to recombine at the interface. At wavelengths of sufficient energy to excite carriers in CdS but not in InSe, the photo-excited carriers in CdS produces a photocurrent, therefore, the photoresponse is negative. The negative photoconductivity may also be explained in terms of donor like traps in the structure which increase the recombination process. Thus, the number of holes is decreased substantially by reducing the total concentration of mobile charge carriers, and hence creates a negative photoconductivity. This tentative explanation is valid only for the high energy region in which photon energy is sufficient to create pairs of charge carriers. The relative magnitudes of the InSe and CdS peaks depend on the resistivity ratio of the two layers.

The low energy threshold of the photocurrent is a measure of the barrier height at the junction which can be calculated by the Fowler plot, $I_{ph}^{1/2}$ versus energy in the vicinity of the threshold as seen in Fig. 4. 58.

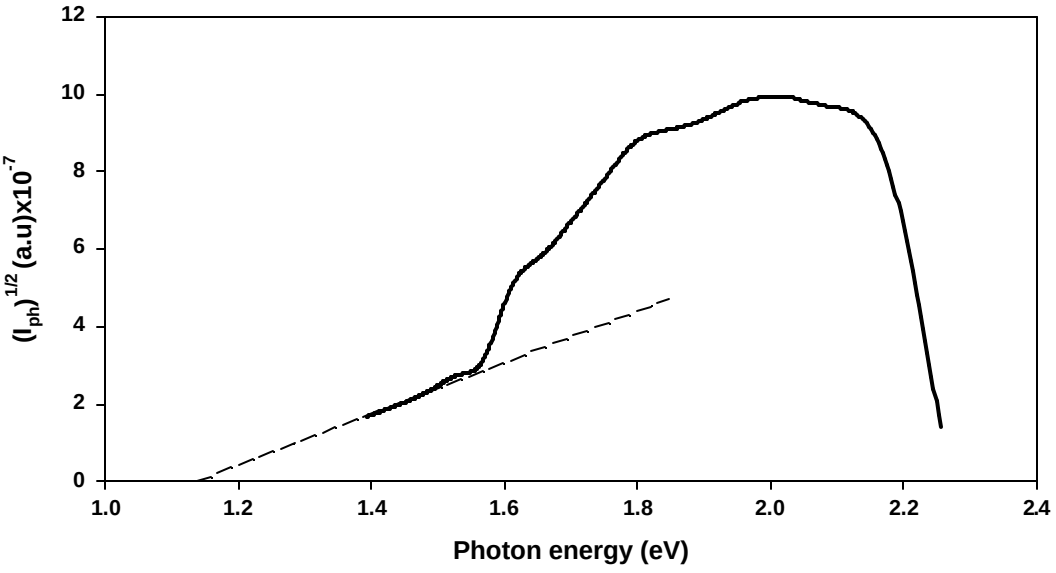


Fig.4.58: The Fowler plot of the solar cell at the threshold energy of the spectrum.

The intercept on the energy axis gives the barrier height of the n-p junction which was found to be around 1.1 eV. This value of the barrier height is comparable to the value obtained from the C-V studies given in section (4.7. 2). Determination of the band gap values from the spectral distribution is also possible since the photo-response of the solar cell can directly be related to the absorption coefficients of the semiconductors used to form the n-p heterojunction. As discussed in section (4.6.5), the direct band gap of a semiconductor can be found by the Eq.(4.6.8) from the spectral distribution. Therefore, the direct band gaps of InSe and CdS can be obtained from the insets of the two peaks which were located around 1.9 and 2.4 eV, respectively, as shown in Fig.4. 59. The intercepts of the linear lines on the energy axis yields the band gaps of InSe and CdS around 1.7 and 2.3 eV respectively. These results were in well agreement with the values found from absorption and photo-response measurements of the InSe and CdS thin films, given previously in this work.

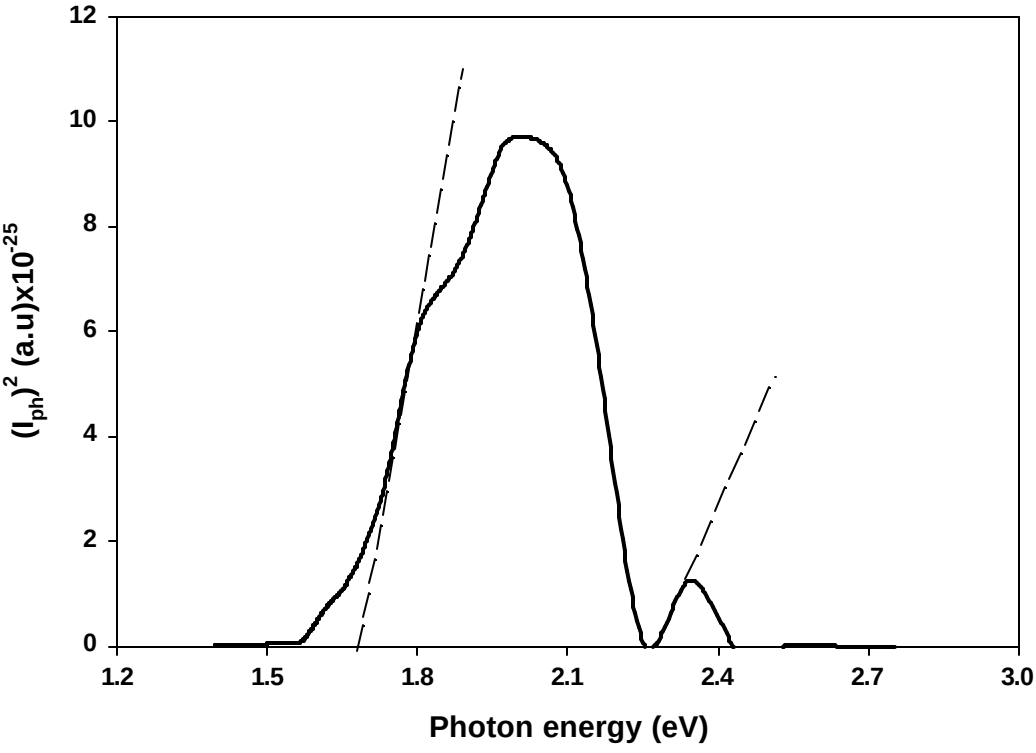


Fig.4. 59: Determination of the band gaps by the I_{ph}^2-hν variation of the solar cell.

CHAPTER 5

CONCLUSION

The main purpose of this work was to investigate and characterize device behavior of n-CdS/p-InSe heterostructures and p-InSe based Schottky diodes by evaporating various metal contacts such as Ag, Au, In, Al and C. Before producing such devices; electrical, optical and structural properties of the films were investigated. The structural properties of InSe and CdS thin films were examined by means of SEM, EDXA and XRD analysis.

The XRD pattern of the source powder was confirmed that the source material was In_2Se_3 single crystal with a preferred crystalline orientation in the plane of (015) in the hexagonal form.

XRD measurements of the cold substrate, as-grown films shown that the films were amorphous with p-type conduction which was determined by the hot probe technique and the sign of the Hall coefficient. Post-depositional annealing of these films at 100 ^{o}C did not produce any changes in the structure as a function of annealing time. Transition into crystalline state starts with annealing at around 150 ^{o}C, but at this annealing temperature conductivity type of the films turned to n-type.

In order to obtain polycrystalline films with p-type conductivity, we have tried to deposit films on hot glass substrates at temperatures above 100 ^{o}C. Cadmium doping agents were used with the same amount of Cd in different deposition cycles and films with Cd/InSe ratio in between 0.01-0.24 were deposited. XRD patterns of lightly doped films with less than 0.17 Cd/InSe ratio indicated that the films were amorphous as the ones without doping. Annealing at 100 ^{o}C of these films did not change the structure, similar to the undoped ones, further annealing at 150 ^{o}C starts the transition into polycrystalline state but with n-type conductivity. Heavily doped cold substrate films with Cd/InSe ratio around 0.24 on the other hand, were found to

be in In_6Se_7 phase with three preferred crystalline orientation in the planes of (112), (113) and ($\bar{2}$14). This may be due to the presence of large amount of Cd atoms in the structure which force the In and Se atoms to form an ordered structure. However, these films were not used in the device fabrication either since the conductivity measurements revealed that they show metallic behavior rather than a semiconductor. Interestingly, the hot substrate heavily doped films were found to be amorphous which may be attributed to the segregation of Cd atoms during the deposition that produces disorder in the structure. Furthermore, it was found that undoped or lightly doped InSe films deposited on cold substrates were amorphous with p-type conductivity.

Structural properties of CdS thin films deposited by thermal evaporation technique were also analyzed for the purpose of p-n heterojunction device investigations. XRD pattern of all deposited CdS films revealed that the films were polycrystalline with a preferred direction of crystallinity in (002) plane. The observed reflection peaks can be attributed to the typical (00*l*) lines of the hexagonal structure of CdS.

Electrical conductivity measurements of the InSe films deposited with and without Cd-doping on cold and hot substrates were carried out together with the effect of post depositional annealing. The room temperature conductivity values of as-grown films grown on cold substrates were found to be in between $8.7x10^{-5}$-$1.1x10^{-4}$ $(\Omega\text{-cm})^{-1}$. Deposition of hot substrate films above 100 ^{o}C did not significantly effect the conductivity values which were found to be in the order of 10^{-4} $(\Omega\text{-cm})^{-1}$. However, Cd doping of the films has shown a pronounced effect with the Cd/InSe ratio increases above 0.17, due to the increase of the free carrier concentration in the films. Heavily doped films with Cd/InSe ratio around 0.24, had conductivity values 4 orders of magnitude higher than that of undoped ones. Whereas lightly doped films with Cd/InSe ratio up to 0.17 had conductivities almost the same order of magnitude with the undoped ones. These results are consistent with the Hall effect measurements from which it was found that the carrier concentrations of undoped and lightly doped samples were in the order of 10^{12}-10^{13} cm^{-3} whereas heavily doped samples were in the order of 10^{19} cm^{-3}.

For the cold substrate undoped and lightly doped InSe thin films temperature dependent conductivity measurements (100-430 K) indicated that different conduction mechanisms dominate in two temperature regions below and above 200 K. The conduction mechanism was determined to be thermal excitation above 200 K in which region conductivity increases sharply with temperature whereas below 200 K, the temperature dependence was weak and conduction dominated by variable-range hopping. The activation energies were found to be 288 meV and 11 meV in high and low temperature regions, respectively. However, activation energies in both high and low temperature regions increased slightly from 220 to 263 meV and from 14 to 34 meV with annealing. This may be explained that annealing clears out some of the traps exist in the band gap region. The Conductivity measurements were consistent with XRD analysis from which we have found that undoped and lightly doped samples had similarly amorphous structure while heavily doped sample was in polycrystalline phase. The activation energies for the heavily doped sample were found to be 29 and 7 meV in the temperature regions 100-230 K and 230-380 K, respectively. This can be interpreted as a metallic behavior and may be attributed to defective degenerate structure caused by the high concentration of Cd atoms.

Temperature dependent Hall effect measurements have indicated that room temperature mobility values were comparable for the undoped and lightly doped samples in the range of 2.7-82 $cm^2/V.s$ whereas heavily doped samples had one order of magnitude lower mobility around 0.1 $cm^2/V.s$. For all samples, variations of mobility observed to be weak over the whole studied temperature range (150-400 K) that reveals the dominant scattering mechanism as neutral impurity scattering.

The temperature dependent electrical conductivity and Hall effect measurements were also carried out for CdS thin films in the range of 100-430 K. All the deposited films exhibited n-type conductivity and room temperature conductivity values were around 1 $(\Omega\text{-cm})^{-1}$. The variations of conductivity of CdS thin films were found to be increasing exponentially with increasing temperature. In the high and low temperature regions below and above 200 K, two different activations energies were found as 77 and 11 meV that indicates different conduction mechanisms were dominating in these regions. Above 200 K, thermionic emission

was determined to be the dominant conduction mechanism while below 200 K, it was found to be variable-range hopping due to the low activation energy. Post-depositional annealing at 100 ^{o}C did not show a pronounced effect on the conductivity values and variations.

Room temperature electron concentrations and Hall mobility of the CdS thin films were found to vary in the range of 10^{16}-10^{18} cm^{-3} and 3.1-3.5 cm^2/V.s, depending on the substrate temperatures. It was seen that the mobility increases as the absolute temperature increases. The grain boundary height was calculated to be 98 meV and 14 meV in the high and low temperature regions, respectively. The dominant scattering mechanism in the low temperature region was found to be neutral impurity scattering as in this temperature region mobility variation was independent of absolute temperature. In the high temperature region, the variation fits to ionized impurity scattering that may be attributed to the increase of ionization of impurities with increasing temperature thus scattering of carriers by impurities occurs in this region. Mobility variation for the annealed CdS thin films were not significantly changed by annealing at 100 ^{o}C for 20 minutes, however, room temperature mobility values decreased from 3.5 to 1.8 cm^2/V.s while the carrier concentration slightly increased from $1.9x10^{18}$ to $3.4x10^{19}$ cm^{-3} which indicates that at high temperatures, the contribution of intergrain ionized impurity scattering to the effective mobility increases with absolute temperature.

The optical band gaps of the as-grown undoped InSe and CdS thin films were determined through absorption measurements. For the InSe thin films, the absorption coefficient decreases exponentially with decreasing photon energy and room temperature values for absorption were found to be in the range of $5.3x10^{2}$-$2.6x10^{4}$ cm^{-1} for the incident photon energies between 1.1-1.9 eV. The optical band gap of the amorphous p-InSe thin film was determined to be around 1.74 eV which is consistent with the literature. The absorption measurements of the CdS thin films indicated that room temperature values were in between $1.4x10^{3}$-$3.8x10^{4}$ cm^{-1} for the photon energies ranging in 1.1-2.9 eV. The absorption spectra revealed the direct band gap of CdS thin film around 2.36 eV which is in well agreement with previously found values in literature.

After the characterization of InSe and CdS thin films, we have fabricated Schottky and p-n heterojunction structures on tin-oxide coated glass substrates with various top metal contacts such as Ag, Au, In, Al and C.

As discussed in section (2.4.1), it was theoretically expected that p-type semiconductors make rectifying junctions with metals whose work functions are less than that of the semiconductor. However, experimental results have shown that this is not always true for p-InSe/Metal junctions due to the complex band structure of p-InSe. This complex band structure arises from the impurity states and self-compensating nature of the p-InSe films in which deep donors are created. This results in rectifying structures with both low and high work function metals. The barrier with the low work function metals are created such that the junction is a typical Schottky structure with negative space charge region, however, for the case of high work function metals the barrier is created by deep donor levels. Among all the TO/a-InSe/Metal Schottky structures studied in this work, the best rectifying behavior was observed for the Ag contact. Some of the diodes with Au top contacts have shown slight rectification but most of them were ohmic. In, Al and C contacts results in ohmic behavior for all the samples. Below the results on the characterization of all studied diode structures with different metal top contacts were summarized briefly.

Indium contacts: Indium has a work function lower than the electron affinity of p-InSe, thus, it was expected that In contacts should be rectifying on p-InSe thin films. However, current-voltage characteristics have clearly indicated that TO/p-InSe/In structure was ohmic. This might be due to the presence of two barriers with almost equal heights between the TO/p-InSe and p-InSe/In junction. In order to check this possibility out, In/p-InSe/In Schottky structure was also investigated and it was observed that this structure also shows ohmic behavior. Thus, it can be concluded that In makes an excellent ohmic contact with p-InSe. Furthermore, this result was expected from film characterization results because all films with In contacts was ohmic so that current-voltage measurements could be carried out.

Aluminum contacts: TO/p-InSe/Al and In/p-InSe/Al Schottky structures have indicated ohmic behavior for all samples and the results were reproducible. Since it was known that In makes ohmic contacts to the p-InSe films, Al was definitely

ohmic in the structure. One contradiction with this result is that, Al has a work function comparable to that of Ag. Therefore, it was expected that Al should also make a rectifying contact with p-InSe film. However, Al is known from the literature that it makes block contact with the films such that it does not diffuse into the film as in the case of Ag contacts.

Carbon contacts: Liquid colloidal graphite was painted onto p-InSe thin films in order to achieve a diode structure in the form of TO/p-InSe/C. The current-voltage characteristics agreed with the theoretical expectations that C makes an ohmic contact with p-InSe film since C has a greater work function than the electron affinity of p-InSe. In/p-InSe/C Schottky structure were also investigated by means of dark and illuminated I-V characteristics and it was found that this structure was ohmic as well.

Gold contacts: The Schottky structures with Au top contacts were another one which contradicts with the theoretical expectations. Au has a greater work function than that of p-InSe, however, experimental results for some of the samples have shown that a slight rectification was observed with the Schottky structures fabricated with Au top contact. This may be due to the band structure of InSe thin films such that p-InSe contains not only acceptor impurities but also deep donor levels. The ionized impurities coming from deep donor levels increases the electron concentration in the film such that the film acts as if it was n-type in the structure. Further proof of this was observed with the current-voltage characteristic under illumination of the TO/p-InSe/Au structure which results in open circuit voltage around 230 meV that was significantly high for a sample with slight rectification. Therefore, we have concluded that under illumination donor impurities are ionized such that the minority carriers become dominant in the film and form a dominating barrier with Au contact because the electrons from ionized deep donors are transferred to the gold contact.

Silver contacts: TO/p-InSe/Ag Schottky structure has shown the best rectifying behavior among all the structures investigated. The ideality factor and the barrier height at room temperature were found to be around 2 and 0.7 eV, respectively. The deviation from ideality is attributed to the highly defective structure of the amorphous InSe film. The conduction mechanism is thought to be

recombination in the depletion region through the localized states. The open circuit voltages and short circuit currents under illumination were found to be 300 mV and $3.2x10^{-7}$ A, respectively. The current-voltage characteristics under illumination shows a straight line which indicates the effect of high series resistance found to be around 588 Ω in comparison with the sheet resistance of the film.

At higher voltages for the rectifying structures, the Schottky contacts become ohmic so that highly resistive InSe film is in between two ohmic contacts, thus the current-voltage characteristics were analyzed by SCLC model which gives information on the density of states in the band gap. The analysis was carried out in the temperature range of 200-320 K for TO/p-InSe/Au structure and it was found that, the density of states was continuously distributed in the range of 0.19-0.25 eV in between $3.82x10^{17}$-$1.73x10^{18}$ $eV^{-1}cm^{-3}$. The calculated values of density of states indicated that the SCLC mechanism in the structure is related with the bulk not with the surface layer between the contacts and the film.

In order to get more information on the rectifying Schottky structures, capacitance voltage (C-V) and spectral response measurements were carried out. C-V measurements indicated that the junction capacitance is almost independent of the applied reverse bias. This may be attributed to the high resistivity of the InSe film of which the whole thickness may be depleted. However, frequency dependent C-V measurements have been performed in the frequency range of 1-1200 kHz and it was found that capacitance changes with frequency at each voltage value. The dependence of capacitance on low frequencies at zero bias is stronger than higher frequencies that is the indication of high number of interface states at the junction.

From the spectral response distribution, the operation range of the Schottky devices was found to be in between 1.5-2.5 eV. The band gap of the InSe thin films were obtained from the Fowler plot which reveals a value around 1.7 eV that was in well agreement with the value calculated from the absorption spectrum of the film.

To improve the device parameters, annealed and Cd doped InSe films were also investigated. Annealed devices at 100 ^{o}C did not show pronounced improvement in the device properties. This was an expected result, because from the film characterization we have seen that annealing at this temperature changed neither the structure nor the electrical parameters of undoped or doped InSe thin films. Further

annealing above 100 ^{o}C results in type conversion which would not meet with our purpose for this study. The structures with Cd doped InSe films have shown ohmic behavior and the poorest photovoltaic response.

At the final stage of our study, p-n heterojunction solar cells, in the form of TO/n-CdS/p-InSe/Metal structure were investigated. The metal contacts tried for the Schottky structures were also investigated on top of heterostructures and among all of them, the best photovoltaic behaviors observed for the Au and C contacts. The ideality factor for the structure with Au contact was found to be around 2.4 and a reverse saturation current of $3x10^{-11}$ A. The I-V characteristics of this structure under illumination at AM1 condition indicated an open circuit voltage around 400 mV and short circuit current of $4.9x10^{-8}$ A. The efficiency of the solar cell was quite low with a fill factor of 0.44 which is due to the small short circuit current that is limited by the high resistivity of the InSe layer. The typical TO/n-CdS/p-InSe/C structure had quite similar characteristics with the one with Au top contact. The ideality factor for this structure was found to be 2.9 and the reverse saturation current was of the order of $2x10^{-11}$ A. The open circuit voltage and the short circuit currents for this structure was determined form the illuminated I-V characteristic around 400 mV and $5.4x10^{-8}$ A, respectively. The filling factor of 0.41 was also comparable with the heterostructure with Au contact and may be attributed to the high resistance of the InSe layer.

As in the case of Schottky structures, annealing at 100 ºC of the devices and Cd doping of the InSe thin films did not improve the photovoltaic properties.

In order to understand junction region capacitance and the effects of surface states, capacitance-voltage and capacitance-frequency measurements have been carried out in the range of 1-2000 kHz and it was found that both structures have shown similar behaviors. The capacitance in the reverse bias region varied slightly whereas in the forward region decreases with decreasing voltage. This is attributed to the high resistance of InSe film and the change of capacitance in the forward bias region is due to the change of the depletion region in CdS side. C-V dependence was weak at high frequencies. The built-in potential in the frequency range of 1-20 kHz was found to be in between 0.85-1.10 V. This variation of the built-in potential with frequency was explained through the effect of interface states at the junction. The

values of the built-in potentials were not in agreement with the theoretically calculated value of 0.7 V which indicates the presence of relatively thick interfacial layer. Furthermore, capacitance-frequency dependence also reveals the existence of high interface states. Frequency dependence of the capacitance is stronger for the low frequencies than for higher frequencies which can be interpreted as at high frequencies ac signal could not be followed by the interface states. Overall from the capacitance measurements, it was understood that a proper p-n junction was not formed due to the high resistivity of InSe layer and high concentration of interface states. Thus, further information on the junction region such as barrier height and acceptor concentration could not be obtained from the C-V analysis.

The photocurrent measurements of a typical p-n heterostructure in the wavelength range of 450-900 nm showed two peaks, one at around 1.9 eV and other one at around 2.4 eV, which are attributed to band-to-band transition in InSe and CdS thin films, respectively. A small shoulder around 1.8 eV is thought to be related with the interface states at or near the junction. The negative peak which is due to the CdS film is explained through the effect of majority carriers because the minority carriers may be recombined at interface states. Another reason for negative photoconductivity could be attributed to donor like traps in the structure which results in an increase in the recombination process. This occurs with the decrease in the hole concentration hence create a negative photoconductivity. However, this is only valid in high energy region in which photon energy is sufficient to create electron-hole pairs. The negative photoconductivity in the TO/CdS/InSe/Au heterostructure can also be the indication of some part of depletion layer extends through the CdS side. Since in the high photon energy region, generation of electron-hole pairs in CdS changes the polarity of devices with respect to the low photon energy region. The Fowler plot reveals the barrier height at around 1.1 eV which is comparable with the value found from the C-V analysis. The spectral distribution also yields the direct optical band gaps of InSe and CdS thin films at around 1.7 and 2.4 eV, which are consistent with the absorption and previous photoelectric measurement of Schottky de vices.

The n-CdS/p-InSe heterojunction solar cell structure investigations revealed that the cells with Au and C top contacts have the best photovoltaic behavior.

However, proper junctions could not be obtained due to the high series resistance of InSe film. Cadmium doping of InSe thin films did not provide any controllable changes in the resistivity of the films because it could not be managed by the thermal evaporation technique. That can be overcome by using pre-sintering of evaporation source powder with Cd. This is going to be the future work for this study.

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