CHARACTERIZATION OF CdS THIN FILMS AND SCHOTTKY BARRIER DIODES

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SİBEL KORKMAZ

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Prof. Dr.Canan Özgen
Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

Prof. Dr. Sinan Bilikmen
Head of Department

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

Prof. Dr. Çiğdem Erçelebi
Supervisor

Examining Committee Members

Prof. Dr.Bahtiyar Salamov (Gazi Unv., PHYS)

Prof. Dr. Çiğdem Erçelebi (METU, PHYS)

Prof. Dr. Bülent G. Akınoğlu (METU, PHYS)

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Name, Lastname : SİBEL KORKMAZ

Signature :

ABSTRACT

CHARACTERIZATION OF CdS THIN FILMS AND SCHOTTKY BARRIER DIODES

KORKMAZ, SİBEL

M.Sc., Department of Physics

Supervisor: Prof. Dr. Çiğdem Erçelebi

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CdS thin films were deposited by thermal evaporation method onto glass substrates without any doping. As a result of the structural and electrical investigation it was found that CdS thin films were of the polycrystalline structure and n-type; and of the transmission analysis optical band gap was found to be around 2.4 eV. Temperature dependent conductivity measurements were carried out in the range of 180 K-400 K. The dominant conduction mechanism is identified as tunnelling between 180 K-230 K and thermionic emission between 270 K and 400 K. To produce Schottky devices, CdS thin films were deposited onto the tin-oxide and indium-tin-oxide coated glasses, by the same method. Gold, platinum, carbon and gold paste were used as metal front contact in these devices. The area of these contacts were about $8\,\mathrm{x}10^{-3}$ cm^2. Temperature dependent current-voltage measurements between 200 K and 350 K, room temperature current-voltage measurements, capacitance-voltage measurement in the frequency range 1 kHz - 1 MHz and photoresponse measurements were carried out for the characterization of these diodes. Ideality factor of the produced Schottky devices were found

to be at least 1.5, at room temperature. Dominant current transport mechanism in the diodes with gold contacts was determined to be tunnelling from the temperature dependent current voltage analysis. Donor concentration was calculated to be about 10^{24} m^{-3} from the voltage dependent capacitance measurement.

Keywords: Schottky, CdS, thin film

ÖZ

CdS İNCE FİLMLERİN VE SCHOTTKY BARİYER DİYOTLARIN KARAKTERİZASYONU

KORKMAZ, SİBEL
Yüksek Lisans, Fizik Bölümü
Tez Yöneticisi: Prof. Dr. Çiğdem Erçelebi

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CdS ince filmleri, termal buharlaştırma yöntemiyle hiç bir katkılama yapılmadan cam tabanlar üzerine büyütülmüştür. Yapısal ve elektriksel incelemelerin sonucunda CdS ince filmlerin çoklu kristal yapıda ve n tipi olduğu; optik geçirgenlik analizinden de optik band aralığının 2.4 eV civarında olduğu bulunmuştur. Sıcaklık bağımlı iletkenlik ölcümleri 180 K - 400 K aralığında yapılmıştır. Bu ölçümlerden baskın iletim mekanizmasının 180 K ile 230 K arasında tünelleme, 270 K ile 400 K arasında termal emisyon olduğu tespit edilmiştir. Schottky aygıtı üretmek amacıyla CdS ince filmleri kalay-oksit ve indiyum-kalay-oksit kaplı cam tabanlar üzerine büyütülmüştür. Bu aygıtlarda önkontak olarak altın, platin, karbon ve altın pasta kullanılmıştır. Bu kontakların alanı yaklaşık $8\,\text{x}10^{-3}$ cm^2 olarak belirlenmiştir. Bu diyotların karakterizasyonu için 200 K ile 350 K arasında sıcaklık bağımlı akım-voltaj ölçümleri, oda sıcaklığında akım-voltaj ölçümleri, 1 kHz - 1 MHz frekans aralığında sığa-voltaj ölçümleri ve foto tepki ölçümleri yapılmıştır. Elde edilen Schottky aygıtlarının idealite faktörlerinin oda sıcaklığında en az 1.5 olduğu bulunmuştur. Sıcaklık bağımlı akım voltaj analizinden altınla yapılan diyotlarda baskın akım mekanizmasının tünelleme olduğu belirlenmiştir. Voltaj bağımlı

sığa ölçümlerinden donor konsantrasyonunun 10^{24} m^{-3} civarında olduğu hesaplanmıştır.

Anahtar Kelimeler: Schottky, CdS, ince film

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CHAPTER 1

INTRODUCTION

Smaller and faster is the technological imperative of our times and so there is a need for suitable materials and processing techniques. Thin films play an important role in fulfilling this need. Besides, they have been used for device purposes over the past 45 years. Thin film is a two dimensional structure, i.e. it has a very large ratio of surface to volume, and created by the process of condensation of atoms, molecules or ions. They do the same function with the corresponding bulk material and their material costs are smaller. Most of the electronic devices require reliable ohmic contacts for electrical signals to flow into and out of the device, and highly stable metal-semiconductor rectifying contacts as the active region. In both cases one must know how to fabricate reliable and efficient metal contacts which have high yield and stability. Thus, it is clear that knowledge of these devices can be used for the development of future technology.

CdS has numerous applications as photoconductive material, because of its wide band gap, such as an n-type window layer within the heterojunction photovoltaic cells which converts the optical radiation into electrical energy [1, 2],

thin film FET transistors, X-ray detectors [3, 4], photodiodes for solar-meters and recently photoelectrolytical and photocatalytical solar energy stocking [5].

CdS thin films can be prepared by several different deposition techniques such as, spray pyrolysis [5, 6, 7], thermal evaporation [8], close space sublimation [9], sputtering [10], electrolysis [11], molecular beam epitaxy (MBE) [12], screen printing, chemical deposition, etc. The chemical deposition is among the least expensive methods in terms of energy [13]. Thermally evaporated and annealed CdS film is the most similar one to the single-crystal CdS from the view point of spectral transmission characteristics among thermal evaporation, chemical deposition by solution growth and spray pyrolysis techniques [14]. Deposition techniques and substrate temperature has a strong effect on the electrical and structural properties of CdS thin films [15].

Polycrystalline CdS thin film's room temperature dark resistivity can be decreased to about 10^{-3} Ω-cm by doping with In, Sn, Al, Br etc. Its mobilities change from 0.1 $cm^2V^{-1}s^{-1}$ to 10 $cm^2V^{-1}s^{-1}$ [16]. The current transport behavior of metal-CdS rectifying contacts were initially studied in 1960's [17, 18, 19, 20, 21]. A reason of found non-ideal behaviors was explained with existence of interface states [17, 22, 23].

Studies on the transport properties of Schottky barrier diodes with CdS show that there is no linear correlation between barrier height and metal work function [24]. In general it is believed that differences are caused by interface defect

formation [25]. Previous studies showed that there are significant changes in the degree of reactivity between CdS and different metals [26, 27, 28, 29]. To investigate chemical composition of and bonding at the metal CdS interfaces, X-ray photoelectron spectroscopy (XPS) analysis were performed on clean and oxidized CdS. Investigations in these studies show that Al, Co and Pd react with CdS surface to form a metal sulfide together with metallic Cd and that Sn on CdS has two forms, namely Sn-Sn and Sn-S, in which case there is no metallic Cd observed. Authors also found that Ag and Sb on CdS does not react with CdS and that Au appeared to disrupt surface causing out-diffusion of S [30, 31].

Although it has generally been considered that the formation of p-type CdS is very difficult because of the strong self-compensation and the depth of the acceptor level in CdS ($\sim$1 eV), there are some recent articles on Cu doped CdS having p-type conduction [32, 33, 34]. In the X-ray diffraction (XRD) analysis of these p-type CdS films [32], only hexagonal CdS were observed and in the XPS analysis [33], there was a decrease in the concentration of Cd with Cu doping but sum of the concentrations of Cd and Cu was 50%. In both analysis and in high-resolution transmission electron microscopy energy dispersive X-ray (HRTEM-EDX) analysis, Cu-S compounds weren't found. Therefore, authors of these articles thought that the p-type characteristics of these films were resulting from Cu acceptor in which some of the Cd^{+2} were substituted by Cu^{+} in the unit cells of CdS, not to the formation of p-type Cu-S [33]. From blue-green to red

colors of light was observed to be emitted from the ITO/p-CdS(Cu)/n-CdS/Al thin film diodes [34].

In this study, undoped, polycrystalline CdS thin films were produced by thermal evaporation technique. The structural parameters of the films were obtained by XRD analysis. Optical properties of the films were studied by transmission analysis. The variation of conductivity with temperature in the range $180\ \mathrm{K} - 400\ \mathrm{K}$ was investigated and current transport mechanisms were determined in two different temperature range. Schottky devices were fabricated in the TO/CdS/metal form by thermal evaporation of Au and Pt and by painting C and gold paste. Electrical properties of these devices were studied at room temperature. Temperature dependent current voltage measurements were performed for Pt and Au Schottky diodes in the range $200\ \mathrm{K} - 350\ \mathrm{K}$ and dominant current transport mechanisms were determined. Optical properties of TO/CdS/C structures were studied.

In the following chapter, properties of CdS, theory of transport mechanism in polycrystalline thin films, formation and current transport mechanism of metal-semiconductor junctions are given. In the third chapter, details of the films' and contacts' deposition technique and measurement methods are presented. In the fourth chapter, structural, electrical and optical characterization of the films and electrical and optical properties of Schottky devices are discussed and results of the measurements are given.

CHAPTER 2

THEORETICAL CONSIDERATIONS

2.1 Properties of CdS Thin Film

Cadmium sulfide is a II-VI compound semiconductor. Bonding in these compounds is a mixture of covalent and ionic types. Group VI atoms are considerably more electronegative than group II atoms and this introduces ionicity. This character has the effect of binding the valence electrons rather tightly to the lattice atoms. Thus, each of these compounds has a higher melting point and larger band gaps than those of the covalent semiconductors of comparable atomic weights [35]. Two types of crystal structures, cubic zincblend and hexagonal wurtzite, are observed in these compounds. Structure type of the deposited crystals depends on the substrate temperature; at low substrate temperature it becomes zincblend whereas at a high temperature one hexagonal wurtzite type is seen [36].

CdS has 2.42 eV direct band gap at room temperature. It is a relatively wide band gap energy so that CdS can be used as a window layer for many heterojunction thin-film solar cells such as CdTe/CdS and CdS/CuInSe [37, 38, 39]. Because CdTe's near optimal band gap energy, high optical absorption, low cost and easy

fabrication, it becomes a mostly used solar cell [40]. Practically used efficiencies for this cell is around 16% [41] and calculated theoretical maximum yield values is nearly 28% [42]. Besides, Cu_xS/CdS is also a promising solar energy conversion device with conversion energy more than 9.1% [43].

CdS becomes sublime at about 700 ^oC and melts at about 1750 ^oC under several atmospheric pressures. It can be deposited either from vapor phase or from high pressure liquid phase. Electron hall mobility of CdS single crystals was found by Kröger, Vink and Volger to increase from about μ_e=210 $cm^2V^{-1}s^{-1}$ at room temperature to a maximum value of μ_e=3000 $cm^2V^{-1}s^{-1}$ at 40 K; but below this temperature it again decreases, presumably due to impurity scattering [44]. Its effective permittivity (dielectric constant) is 11.6 and density is approximately 4.84 g/cm^3. CdS does not show intrinsic behavior at room temperature, i.e. deposited CdS thin films doesn't need doping to become n-type. Formation of p-type CdS is very difficult, because of the strong self-compensation effect caused by sulfur vacancies [45, 46].

Pure CdS crystals have a high resistivity about 10^{12} Ω-cm. Polycrystalline CdS thin film's resistivity can be reduced by In, Sn, Al, Cr or Br doping or by some growth techniques. For example, 10^{-3} Ω-cm resistivity was reported for the films grown by close-space vapor transport [47]. The grain sizes of CdS films are usually around 0.3-0.5 μm. As the film thickness is increased, larger crystallites are formed in the film. Annealing at high temperatures enhance the

grain size and recrystallization of CdS [14]. $CdCl_2$ treatment increase the effect of annealing [48].

2.2 Transport Mechanism of Polycrystaline Semiconductors

The polycrystalline material is composed of random sized, shaped and oriented crystallites or grains separated by grain boundaries. Inside each crystallite the atoms have nearly perfect periodicity and so it is considered as if a single crystal. The grain boundary consists of a few atomic layers of disordered atoms which cause the large number of defects. This results in formation of trapping states [49].

Several models have been proposed to explain the polycrystalline semiconductor transport properties and the grain boundaries between grains play an important role in determining these properties [50]. In general, there are three types of conduction mechanisms depending on temperature region, for polycrystalline thin films. They are thermionic emission, tunnelling and hopping and are explained in the following sections.

2.2.1 Thermionic Emission

The most dominant conduction mechanism in the high temperature region is the thermionic emission. Majority carriers which have enough energy to pass over the potential barrier at the grain boundary cause this kind of conduction.

To simplify his model Seto [51] made some assumptions. The first one is that

all crystallites are identical and have the same grain size of L(cm). He also assumes that impurity atoms are ionized, uniformly distributed with concentration $N(\text{cm}^{-3})$ and they are of the same type. His further assumption is that grain boundary thickness is negligible compared to L. Grain boundary contains initially neutral $Q_t(\text{cm}^{-2})$ number of traps with energy E_t with respect to the intrinsic Fermi level. In his model both tunnelling and thermionic emission contributes to the current across the grain boundary. In a highly doped polycrystalline, barrier height and width decreases swiftly so tunnelling will be smaller with respect to thermionic emission and can be neglected.

Thermionic emission current density across the grain boundary is [51],

$$J_{th} = qn_a \left(\frac{kT}{2m^*\pi}\right)^{1/2} exp\left(-\frac{qV_B}{kT}\right)\left[exp\,(\frac{qV_a}{kT}) - 1\right] \tag{2.1}$$

where m^* is the effective mass of the carrier, V_a is the applied voltage, qV_B is the barrier height and n_a is the average carrier concentration. For $qV_a \ll kT$ eqn.(2.1) becomes

$$J_{th} = q^2 n_a \left(\frac{kT}{2m^*\pi}\right)^{1/2} exp\left(-\frac{qV_B}{kT}\right) V_a \tag{2.2}$$

which shows a linear relationship between V_a and J_{th}. Thus the conductivity of a polycrystalline film with a grain size (L) can be expressed as,

$$\sigma = Lq^2 n_a \left(\frac{kT}{2m^*\pi}\right)^{1/2} exp\left(-\frac{qV_B}{kT}\right) \tag{2.3}$$

By inserting the average carrier concentration, n_a, for $NL < N_t$ and $NL > N_t$

conductivity relationships are found as

$$\sigma \quad \alpha \quad exp\,[-(\frac{1}{2}qV_B - E_F)/kT\,] \qquad NL < N_t \tag{2.4}$$

$$\sigma \quad \alpha \quad T^{-1/2}\,exp\,(-qV_B/kT\,) \qquad NL > N_t \tag{2.5}$$

where N_t is the number of traps located at energy E_t with respect to the Fermi level. This interpretation will fail when $qV_B \ll kT$ like highly doped materials. The expression $\sigma = qn_a\mu$ shows the relation between mobility and conductivity.

2.2.2 Tunnelling

When the potential barrier at the grain boundary is high but narrow and the carriers do not have enough energy to surmount the barrier, quantum mechanical tunnelling of carriers through the barrier become dominant. This situation may be attainable at low temperatures.

Following Seto's model, energy barrier was determined by the one-dimensional solution of Poisson equation. Then tunnelling current density can be calculated in terms of WKB (Wentzel-Kramers-Brillouin) approximation as [52]:

$$J_{tu} = J_0\,\left(\frac{FT}{\sin FT}\right) \tag{2.6}$$

where J_0 is the tunnelling current density at 0 K and

$$F = \frac{2\pi^2(2m^*)^{1/2}k\triangle s}{h\,\overline{\phi}^{1/2}} \tag{2.7}$$

where $\overline{\phi}$ is the mean barrier height at the grain boundary and $\triangle s$ is the barrier width at the Fermi level. Conductivity corresponding to tunnelling current can be calculated from $\sigma_{tu} = LJ_{tu}/V$

$$\sigma_{tu} = \sigma_0 \frac{FT}{\sin FT} \tag{2.8}$$

where $\sigma_0 = LJ_0/V_0$ is the limit of the film conductivity at 0 K given by

$$\sigma_0 = \frac{Lq^2(2m^*)^{1/2}\overline{\phi}^{1/2}}{2h^2 s} \exp\left(\frac{-8\pi(2m^*)^{1/2} s\,\overline{\phi}^{1/2}}{h}\right) \tag{2.9}$$

If FT is small enough, then σ_{tu} is expressed as:

$$\sigma_{tu} = \sigma_0\Big[\,1 + (\,\frac{F^2}{6}\,)T^2\,\Big]. \tag{2.10}$$

2.2.3 Hopping

In the low temperature range, hopping may become the dominant conduction mechanism. When the impurity states are sufficiently low, ordinary conduction mechanism cannot take place within the impurity region. Therefore, hopping conduction becomes dominant conduction mechanism. In this type of conduction the carriers with low activation energy hop between the localized states. There are two types of hopping mechanisms according to the range of localized states. Hopping of carriers to the nearest empty one is called constant range hopping whereas to the empty states remote from the nearest one is called variable range hopping.

Conductivity expression of Mott's hopping mechanism [53] is given by

$$\sigma\sqrt{T} = \sigma_0\, exp\,(\,-\,\frac{T_0}{T}\,)^{1/4} \tag{2.11}$$

where σ_0 and T_0 are constants.

In polycrystalline materials, the variable range hopping exists in the grain boundaries from charged trap states to neutral trap states when the carriers don't have enough energy to surmount the barrier by thermionic emission at the grain boundary. In that case dominant conduction process depends on the relative grain size L_g with respect to Debye length L_D which is given as,

$$L_D = \left[\,-\,\frac{\varepsilon\varepsilon_o kT}{q^2 N_d}\,\right]^{1/2} \tag{2.12}$$

where N_d is doping concentration and ε is the dielectric constant of material. If grain size is too smaller than L_D, variable range hopping process is dominant over a wide range of temperature. And in the opposite case thermionic emission predominates over the variable range hopping even at very low temperatures [54].

2.3 Schottky Barrier Diodes

Rectification nature of metal-semiconductor interfaces has been known since 1874 when F. Braun issued his report about the nature of metallic contacts on copper, iron and lead sulfide crystals.

Point contact diodes which were produced by pressing a sharpened metallic wire onto a clean semiconductor surface were the metal-semiconductor diodes in

early 1900's. In 1906 Pickard patents the silicon diodes which were used as radio wave detectors in these days and then as frequency converter and as low level microwave detectors diode during the Second World War. However, they were not reliable and reproducible and were replaced by thin metallic films deposited onto thin semiconductor films.

A rectifying metal-semiconductor contact was known as a Schottky Barrier after W. Schottky who realized the potential barrier at the interface of metal-semiconductor contact. Subsequently, Schottky and Mott proposed models to describe the barrier formation.

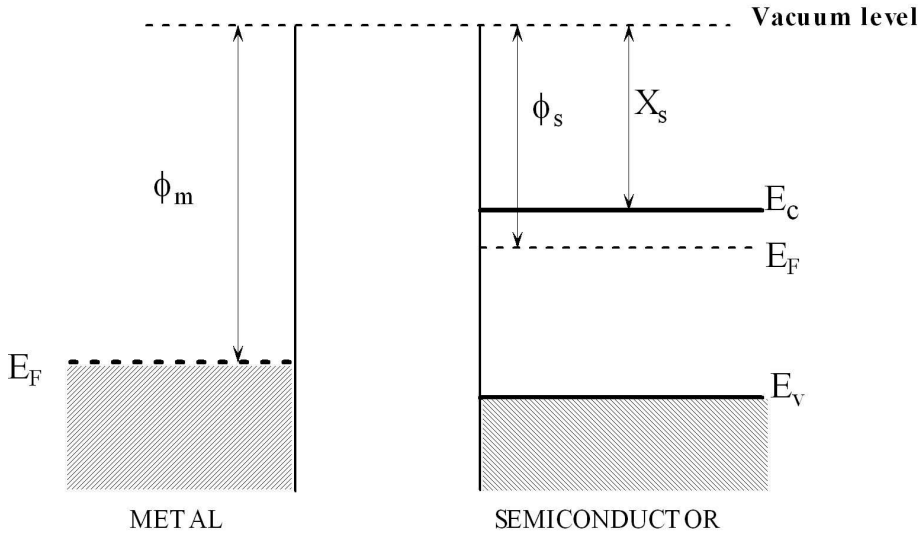

Figure 2.1: Energy band diagram of n-type semiconductor and metal separated from each other

2.3.1 Energy Band Diagram of Schottky Contacts

According to Schottky and Mott model, the difference in the work functions of metal and semiconductor causes the barrier. To describe this model, consider first the energy band diagrams of n-type semiconductor and metal isolated from each other (see Figure 2.1). In the figure E_F is the Fermi level, ϕ_m is the work function of metal which is the minimum energy required to liberate an electron from the metal. The Fermi level of metal is assumed to be lower than the Fermi level of n-type semiconductor ($\phi_m > \phi_s$), which means that electrons in the semiconductor have higher energy than electrons in the metal.

a) Thermal Equilibrium

When an intimate contact is made between metal and semiconductor, the electrons in the conduction band of the semiconductor move into the metal till the Fermi level of two sides are coincident. This creates a depletion region at the semiconductor interface. Decreases in the electron concentration of semiconductor boundary region cause bending up at the conduction band boundary as shown in Figure 2.2.

At thermal equilibrium; the quantity of electrons transferring in both ways are the same; and so, there is no net current flow. Since there is a few mobile carriers in the depletion region, its resistance is very high in comparison to the metal and neutral semiconductor. Thus, applied voltage appears at this

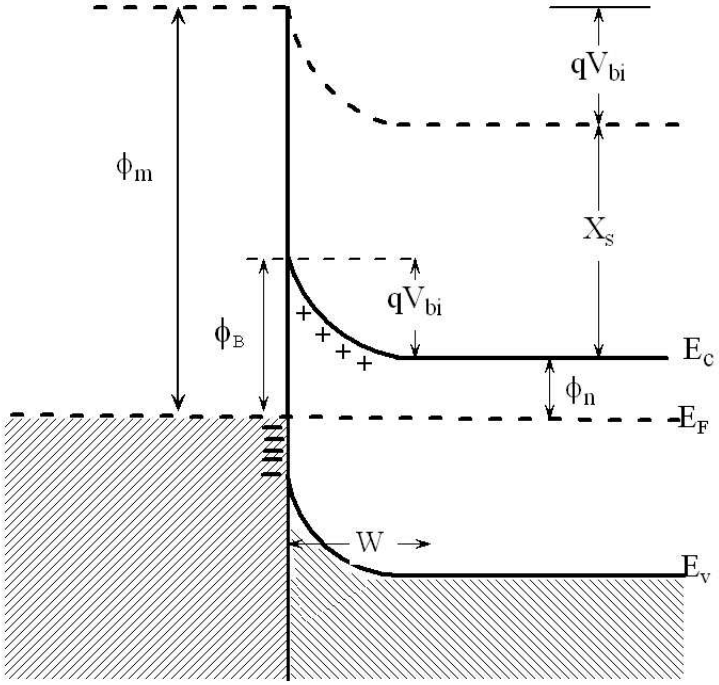

Figure 2.2: Energy band diagram of n-type semiconductor and metal at thermal equilibrium

region.

b) Forward Bias

Applied forward voltage reduces the depletion region width, W, and voltage across this region from V_i to $V_i - V_F$. Therefore, electrons on the semiconductor sides come across a lower barrier. However, on the metal sides barrier doesn't change. As a result, the flow from semiconductor to metal increases but the one from metal to semiconductor doesn't change. Consequently, there is a net current flow from metal to semiconductor and this current increases by increasing V_F.

c) Reverse Bias

Applied reverse voltage increases the width of the depletion region and voltage across this region increases from V_i to $V_i + V_R$. Thus the electrons on the semiconductor side meet with an increased barrier. However, the barrier on the metal side is again the same. Therefore, a net current flow from metal to semiconductor occurs and it increases by increasing V_R. When compared to forward current this is a smaller current.

2.3.2 Ohmic Contacts

For the n-type semiconductors when the Fermi level of semiconductor is lower than the Fermi level of the metal ($\phi_s > \phi_m$) an ohmic contact is formed. In

this type of contact there is no restriction to the flow of charge carriers. After an intimate contact is made between metal and semiconductor, electrons on the metal flow to the semiconductor's conduction band. These electrons accumulate near the boundary region as a surface charge and they leave behind positive charges at the boundary of metal. These positive charges are also surface charges and form a thin level with a distance about 0.5 A from the metal-semiconductor interface.

At thermal equilibrium, it is clear that no depletion region is formed in the semiconductor and there is no barrier to the electron flow at both sides. Besides, there is no net electron flow and so no net current flow.

Because of the increasing electrons near the interface, all applied voltage, practically, appears across the bulk region. Therefore, the current is determined by the bulk region resistance and it is independent of the applied bias voltage direction.

2.4 Current Transport Mechanisms in Schottky Barriers

The current flow in Schottky barriers is mainly due to the majority carriers. There are four different mechanisms by which carrier transport can occur:

a) thermionic emission-diffusion over the barrier

b) tunnelling through the barrier

c) carrier recombination (or generation) in the depletion region

d) carrier recombination in the neutral region

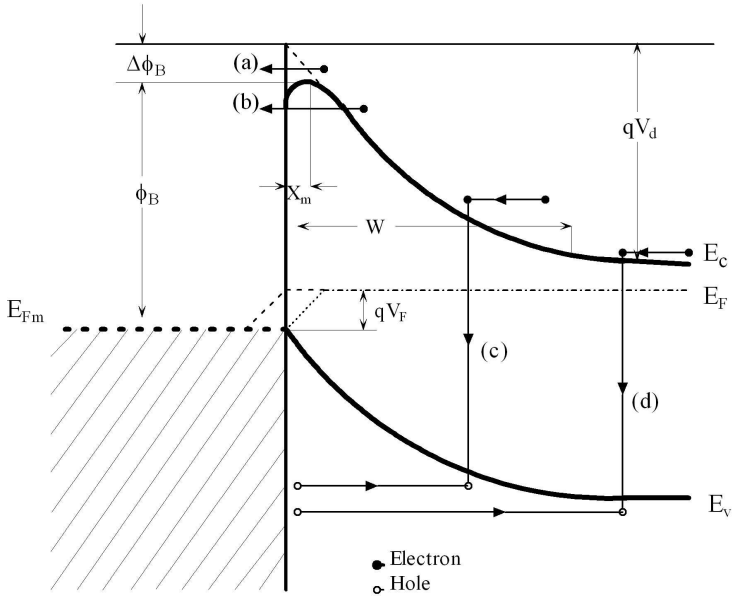

Figure 2.3: Energy band diagram of n-type semiconductor and metal under forward bias

2.4.1 Diffusion and Thermionic Emission

As seen in Figure 2.3 electrons emitted over the barrier from semiconductor into the metal must move through the high field depletion region. Two processes, namely the emission over the barrier and the drift and diffusion in the depletion region, limit the diode current. These processes are effectively in series and the one which offers the higher resistance determines the current. Drift and diffusion theory were treated by Wanger [55], Schottky and Spenke [56] and thermionic

emission theory was proposed by Bethe [57]. The difference between these mechanisms is that in the diffusion theory electrons are in thermal equilibrium with the lattice so that their quasi-Fermi level coincides with metal Fermi level at the interface (as shown in Figure 2.3 by dotted curve) but in the thermionic emission theory, electrons entering the metals have higher energy than the metal electrons and their quasi-Fermi level is almost horizontal through the depletion region (as shown in the Figure 2.3 by dashed curve). Thermionic theory assumes that drift and diffusion in the depletion region is negligible, the barrier height is much larger than kT and the effect of the image force is negligible. The current density J_{sm} is given by:

$$J_{sm} = qn \left(\frac{kT}{2\pi m^*} \right)^{1/2} \exp \left(-\frac{m^* v_x^2}{2kT} \right) \tag{2.13}$$

where n is the electron concentration, m^* is the effective mass for free electron, v_x is the minimum velocity required to surmount the barrier and is given by the relation:

$$\frac{1}{2} m^* v_x^2 = q(V_{bi} - V_a) \tag{2.14}$$

where V_{bi} is the built-in potential and V_a is the applied voltage. The electron concentration of the semiconductor is given by

$$n = n_0 \exp \left(-q \frac{V_{bi} - V_a}{kT} \right) \tag{2.15}$$

$$n_0 = N_c \exp \left(-\frac{E_c - E_F}{kT} \right) \tag{2.16}$$

where n_0 is the electron concentration in the neutral region of the semiconductor. By inserting eqn.(2.16) in eqn.(2.15) electron concentration is found as:

$$n = N_c \exp\left(-\frac{\phi_B - qV_a}{kT}\right) \tag{2.17}$$

Then, J_{sm} can be expressed as,

$$J_{sm} = A^* T^2 \exp\left(\frac{-\phi_B}{kT}\right) \exp\left(\frac{qV_a}{kT}\right) \tag{2.18}$$

where $A^* = \frac{4\pi q m^* k^2}{h^3}$ is the Richardson constant.

When applied voltage, V_a, is zero, under the thermal equilibrium, no net current can flow. Consequently, the current given by eqn.(2.18) is balanced by the current flow, J_{ms}, from metal into the semiconductor must be equal to

$$J_{ms} = -A^* T^2 \exp\left(\frac{-\phi_B}{kT}\right) \tag{2.19}$$

The total current density is given by the sum of J_{sm} and J_{ms},

$$J = J_s(\exp\left(\frac{qV_a}{kT}\right) - 1) \tag{2.20}$$

where

$$J_s = A^* T^2 \exp\left(\frac{-\phi_B}{kT}\right). \tag{2.21}$$

Crowell and Sze combine these two theory and they take into account the effect of image force barrier lowering and optical phonon scattering in the metal and quantum mechanical reflection from the barrier [58].

2.4.2 Tunnelling

Tunnelling can occur either as field emission or thermionic field emission with respect to the doping rate and temperature. When doping concentration is high, depletion region becomes very thin and the Fermi level may lie above the bottom of the conduction band. Electrons are close to the Fermi level at low temperature and in the forward bias these electrons may flow from the Fermi level of the semiconductor to the metal; this is known as field emission (FE). At higher temperature some electrons are able to rise above the Fermi level where they see a thinner and lower barrier and can tunnel into the metal before reaching the top of the barrier; this process is known as thermionic field emission (TFE). TFE can be observed only in the intermediate doped semiconductors and it becomes maximum at an energy level, E_m. E_m is measured from the bottom of the conduction band at the edge of the depletion region and equals to,

$$E_m = \frac{qV_{bi}}{[cosh(E_{00}/kT)]^2} \tag{2.22}$$

where V_{bi} is the voltage corresponding to the total band bending and E_{00} is the characteristic energy that determines the relative importance of tunnelling and thermionic emission diffusion as a current mechanism. It is expressed as

$$E_{00} = \frac{h}{4\pi}\left(\frac{N_d}{m_e^*\varepsilon_s}\right)^{1/2} \tag{2.23}$$

where m_e^* is the effective mass of electrons, ε_s is the permittivity of the semiconductor, N_d is the donor concentration in m^{-3}. FE is the dominant mechanism

when $E_{00} \gg kT$. It is the case that is mostly observed only at low temperatures. At higher temperatures $E_{00} \sim kT$ and contribution of TFE to the diode current becomes dominant. If the temperature continues to rise gradually, a limit is reached at which all the electrons are able to reach to the top of the barrier and $E_{00} \ll kT$. This is the case for thermionic emission-diffusion. I-V relationship for tunnelling mechanism is given by

$$I_t = I_{t0} \exp\left(\frac{qV_a}{E_0}\right) \tag{2.24}$$

where

$$E_0 = E_{00} coth\left(\frac{E_{00}}{kT}\right). \tag{2.25}$$

The pre exponential factor I_{t0} in eqn.(2.24) is a complicated function of barrier height, parameters of semiconductors and temperature. For FE the slope of Ln I vs V doesn't change with temperature and it is equal to q/nkT for the TFE regime.

In the above analysis of Padovoni and Stratton [59] and Crowell and Rideout [60], image force barrier lowering and quantum mechanical reflections of the electrons from the top of the barrier are neglected and Boltzmann statistics is used. Chang and Sze [61] in their studies took into account both of above effects and used degenerate Fermi statistics. For the TFE regime their studies' results are similar to those of Padovoni and Stratton and Crowell and Rideout. Although there is differences in the FE regime, Padovoni and Stratton and Crowell

and Rideout's analysis described above is sufficient to explain the experimental data [62].

For the reverse bias, increase in the electric field in the junction increase the probability of an electron to tunnel from the metal into the semiconductor. Therefore, under reverse bias tunnelling can also be observed as the dominant current transport mechanism at lower doping concentration. [59].

2.4.3 Carrier Generation Recombination in the Depletion Region

This current is a generation current for the reversed biased junction and recombination current for the forward biased one. It is added to the thermionic emission current and in some cases may be responsible for the value of $n > 1$. It becomes dominant only for large barrier height, low temperature, and lightly doped semiconductor of low carrier lifetime.

At zero bias there is no net current flow because electron-hole pair generation rate is balanced by electron-hole recombination rate at the depletion region of Schottky barrier. When a reverse bias is applied to a Schottky barrier junction on n-type semiconductor, electron-hole pairs excess their thermal equilibrium value in the depletion region. Electric field of the barrier sweep out these pairs and that causes a reverse current. However, when the applied voltage is forward bias electrons are injected into the depletion region from neutral bulk semiconductor and holes are injected from the metal. These excess electron-hole pairs recombine

in the depletion region thereby causing a forward recombination current. The carrier generation-recombination current in the depletion region is given by [63]

$$J_{rg} = \frac{qn_iW}{2\tau_0}\,[\,exp\,(\frac{qV_a}{2kT}) - 1\,] \tag{2.26}$$

where τ_0 is the minority carrier lifetime in the depletion region, W is the width of depletion region and n_i is the intrinsic electron concentration. This equation shows that this current becomes important only at low values of forward bias.

2.5 Capacitance-Voltage Characteristics

The electric field and potential distribution in the depletion region of the Schottky barrier junction depend upon the barrier height, the applied voltage and impurity concentrations. When it is assumed that the semiconductor is nondegenerate and uniformly doped, one-dimensional Poisson equation can be written as,

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\epsilon_s}[N_d + p(x) - n(x)] \tag{2.27}$$

where ϵ_s is the semiconductor permittivity, $n(x)$ and $p(x)$ are the electron and hole concentrations at any point x in the semiconductor, respectively. A closed form solution of this equation is not possible. By using depletion approximation, eqn.(2.27) can be written in a simplified form;

$$\frac{d^2\phi}{dx^2} = 0 \qquad\qquad x > W \tag{2.28}$$

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\epsilon_s}N_d \qquad 0 < x < W \tag{2.29}$$

where W represents the width of the depletion region. Depletion region electric field ε, potential energy ϕ and width W can be found from this equation by using boundary conditions $\varepsilon(0) = \varepsilon_m$ (ε_m is the maximum electric field), $d\phi(W)/dx = 0$ and $\phi(W) = 0$. Width can be expressed as,

$$W = (\frac{2\epsilon_s}{qN_d} |V_i - V|)^{1/2} \tag{2.30}$$

where V is the applied voltage and V_i is the built in voltage. Change in the applied voltage across the Schottky barrier junction causes a change in the width of the depletion region and because of this change, charge carriers move into or out of the space charge layer. The space charge layer capacitance per unit area is defined by the relation,

$$C = \frac{dQ_d}{qV_d} = -\frac{d(Q_m + Q_h)}{qV_d} \tag{2.31}$$

where V_d is the voltage drop across the junction, Q_d is the charge in the depletion region which results from the movement of electrons out of the semiconductor into the metal, Q_m is the charge on the metal surface caused by the electrons that have crossed from the semiconductor into the metal and Q_h is the holes charge placed in the semiconductor region just adjacent to the metal contact. Q_d is the opposite charge required to balance $Q_m + Q_h$. If we neglect the effect of the minority carriers, take $Q_h = 0$ and assume that band bending is so small, i.e. $p(x)$ is negligible everywhere then we obtain eqn.(2.27) as

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\epsilon_s} N_d - n_0 \, exp \left[\frac{q\phi(x)}{kT} \right] \tag{2.32}$$

where $\phi(0) = -V_d$, $\phi(W) = 0$ are the boundary conditions and assuming $N_d = n_0$. By using these boundary conditions and $\epsilon_s \varepsilon_m = Q_d$ which is found by applying Gauss law at the metal semiconductor boundary we obtain,

$$C = A \frac{dQ_d}{qV_d} = A \left[\frac{q\epsilon_s N_d}{2(V_i - (kT/q) - V)} \right]^{1/2} \tag{2.33}$$

where A represents the area of the Schottky barrier contact and the term kT/q is the contribution of the majority carriers to the space charge. When this term is omitted C becomes

$$C = \frac{A\epsilon_s}{W}. \tag{2.34}$$

Schottky barrier acts as a parallel plate capacitor [64, 65]. The plot of the C^{-2} against the applied voltage is a straight line with a slope $2/A^2 q\epsilon_s N_d$. From intercept with the voltage axis of this plots we may determine the barrier height. If the doping concentration varies with the distance in the semiconductor, this plot is not a straight line, the slope at any point is given by $2/A^2 q\epsilon_s N_d(W)$ [66].

In some Schottky diodes the capacitance under forward bias is larger than the space charge (depletion region) capacitance. The difference between the measured and the space charge capacitance is called excess capacitance and is attributed to interface states which are created by crystal lattice discontinuities (dangling bonds), interdiffusion of atoms or a large density of crystal lattice defects close to metal semiconductor interface [64]. As long as the interaction between the real interface states and electrons in the semiconductor and metal is approximated

by the Shockley-Read-Hall (SRH) model, there is an upper reverse bias voltage (barrier height is larger than $E_g/2$) beyond which the net charge in the interface states is kept constant and does not contribute to I-V characteristic. On the other hand, in the forward bias, majority carriers increase and force the occupancy of interface states to follow the Fermi level, and this causes a non-ideal behavior in C^{-2}-V plots [67, 68, 69]. Thus the capacitance frequency analysis is practically done in low forward voltages. In general, the interface states in equilibrium with the semiconductor do not contribute to the measured capacitance at sufficiently high frequencies because the charge at the interface states cannot follow the ac signal. In this case, measured Schottky diode capacitance is only the space-charge capacitance C_{sc}. At low frequencies, measured capacitance value is the summation of the space charge capacitance and the interface states capacitance C_{ss}.

$$C = C_{sc} + C_{ss} \quad (at\ low\ frequency),$$

$$C \cong C_{sc} \qquad (at\ high\ frequency).$$

Therefore, from the C-f plot C_{ss} can be found. Interface states capacitance can be described as [68, 70]

$$C_{ss} = qAN_{ss}\frac{arctan(w\tau)}{w\tau} \tag{2.35}$$

where A is the diode area and τ is the interface states relaxation time. For the small values of $w\tau$, the interface states density can be calculated from the

relation [71]

$$N_{ss} = \frac{C_{ss}}{qA} \tag{2.36}$$

The effects of the trapping in the depletion region, the edge effect and the effect of the roughness of the surface to which the contact is made, the possible effects of an interfacial layer between metal and semiconductor with fixed surface charge density at the boundary surface between the semiconductor and interfacial layer and the effect of the reverse layer was examined for CdS by Goodman [72].

2.6 Optical Considerations

In this study, transmission and photoresponse were made for calculation of optical properties. Polycrystalline semiconductors are composed of undesirable and uncontrolled impurities, stoichiometry deviations, point defects, etc in addition to the grain boundaries. Optical measurements are not as sensitive as electrical ones to these effects [73].

2.6.1 Transmission

The fundamental absorption refers to the band to band transition, i.e. the excitation of an electron from the valence band to the conduction band. Electromagnetic waves interact with electrons in the valence band and they excite them into the conduction band. There are two types of optical transition, direct and indirect. In the indirect transition, there is an simultaneous interaction with

lattice vibration.

Photon absorption coefficient $\alpha(h\nu)$ for a given photon energy can be expressed as [74],

$$\alpha(h\nu) = A\,\Sigma P_{if}\,n_i\,n_f \tag{2.37}$$

where P_{if} is the is the probability of transition from initial state to final state and n_i and n_f is the density of electrons in initial and final states, respectively. During transition measurements light is sent on the sample and the transmitted light is measured as a function of wavelength. The optical absorption coefficient was calculated from the transmission data by using the relation,

$$\alpha = \frac{1}{d}\,ln(\frac{I_0}{I}) \tag{2.38}$$

where d is the thickness of the sample and I is the intensity of the transmitted light, I_0 is the intensity of the incident light [75]. According to the interband absorption theory, the optical absorption coefficient for the direct allowed transition is given as,

$$\alpha(h\nu) = A\,(h\nu - E_g)^{1/2} \tag{2.39}$$

where A is a constant and E_g is the optical energy band gap situated between the localized states [76].

2.6.2 Spectral Response

The photoelectric method is one of the direct method to determine barrier height and band gap. When a monochromatic light is incident on a metal-semiconductor junction, photocurrent may be generated. This photocurrent can be the result of either photoelectrons or electron hole pairs depending on the energy of photons. For the back illumination (light is incident on the semiconductor side), if the photon's energy is between barrier height and semiconductor band gap, photoelectrons are generated and so photocurrent is observed and if its energy is higher than the band gap energy electron hole pairs are obtained. However, the photocurrent may not be observed because these pairs are generated at the back side of the semiconductor and they are recombined before reaching the metal side.

Under the front illumination (light is incident on the metal side of the junction), metal's electrons are excited by absorbing incident light and emitted from metal into the semiconductor when the photon energy is higher than the barrier height and lower than the band gap. As it is for the back illumination, electron hole pairs are generated when photon's energy is higher than the band gap and metal is sufficiently thin. Unlike back illumination, these pairs can produce photocurrent. Besides these, electron hole pairs can also be generated by photons which have much greater energy than the band gap, but because penetration depth of the light decreases with increasing its energy these pairs are created

near the surface. Hence, they recombine with majority carriers before diffusing into the depletion layer. This event does not contribute to the current flow and is not detectable.

According to Fowler analysis, photocurrent, I_{ph}, is given as a function of photon energy $h\nu$ by the relation [64]

$$\sqrt{I_{ph}}\,\alpha\,(h\nu - h\nu_0). \tag{2.40}$$

The intercept of a plot of $\sqrt{I_{ph}}$ vs $h\nu$ graph, called Fowler plot, yields the threshold photon energy $h\nu_0$ which is equal to the barrier height of the junction. In Fowler analysis photocurrent is directly associated with absorption coefficient, so for the photon energy higher than band gap, E_g, square of the photocurrent is related with the band gap as:

$$I_{ph}^2\,\alpha\,(h\nu - E_g) \tag{2.41}$$

for direct band gap and,

$$I_{ph}^{1/2}\,\alpha\,(h\nu - E_g) \tag{2.42}$$

for indirect band gap. Therefore, intercept of the photon energy axis of the plot of I_{ph}^2 vs hν gives the direct optical band gap of CdS.

CHAPTER 3

EXPERIMENTAL TECHNIQUES

3.1 Introduction

In this chapter, the details of CdS thin film growth and Schottky diodes preparation processes are summarized. Besides these, electrical measurement methods, thin films' structural characterization techniques and analysis of experimental data are introduced. The CdS thin films were deposited by thermal evaporation technique onto the flat tin oxide and indium tin oxide coated glass substrates. Hall-Bar shaped thin films were used for the conductivity measurement. Hall-bar mask was used onto the glass substrates when the films were deposited to obtain Hall-bar shaped films. Hall effect measurement between 120 K and 400 K is carried out to do electrical characterization of films. For the structural characterization of the films X-ray diffraction was carried out. Additionally current-voltage, capacitance-voltage and temperature dependent current-voltage measurements were done to investigate the electrical characteristics of the Schottky diodes. Transmission and photo response measurements were performed to determine the optical properties of the films and Schottky barriers, respectively.

3.2 PREPARATION OF CdS THIN FILMS

3.2.1 Substrate Preparation

As substrates, soda lime glass slides, tin oxide coated and indium tin oxide coated glasses were used in the deposition of CdS thin films. The glass slides were cleaned to eliminate any possible sticking particles and impurities from them. They were cleaned by the following procedure

- The slides were cleaned in a diluted solution of detergent at 70 ^{o}C for ten minutes.

- Secondly, the container was put into the ultrasonic cleaner for 5 minutes to remove the protein, and other sticking particles on the surface of the slides.

- Thirdly, ultrasonic cleaner procedure is repeated with pure water in another container for 5 minutes. Some of the detergent and sticking particles are removed at this step.

- After that, slides are boiled with 30% H_2O_2, 70% pure water solution to remove the detergent residue.

- Finally, slides were put into another container filled with clean hot pure water and then this container was put in the ultrasonic cleaner for 10 minutes.

3.2.2 Vacuum Deposition Cycle

Varian NCR 836 oil diffusion vacuum system was used to deposition of CdS thin film by thermal evaporation. This system is shown in Figure (3.1).The details of the system is given in the literature [8].

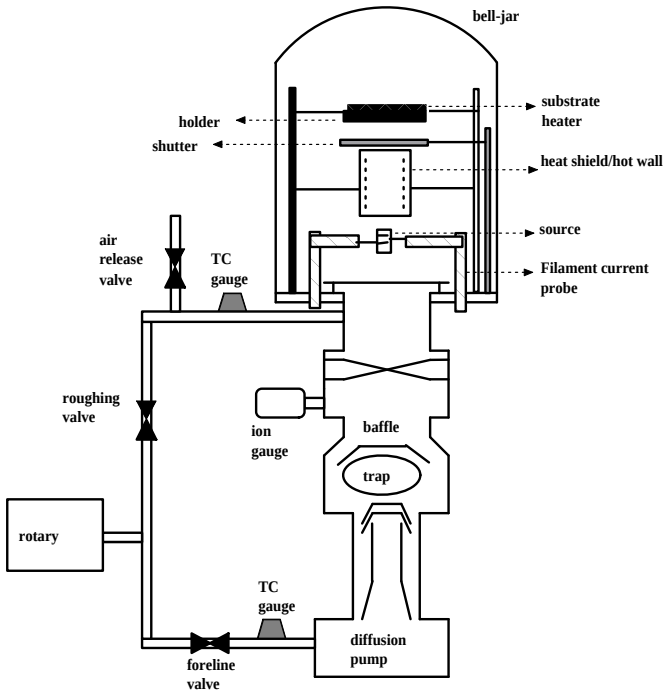

Figure 3.1: Vacuum evaporation system

During a few growths, hot wall was used between the substrate and the source. This hot wall was a quartz cylinder heated by a variac and its temperature was measured by a chromel/alumel thermocouple which made contact with the inner surface of chimney. A stainless steel shutter was placed between the hot wall and the substrate.

Quartz crucible was filled with pure CdS powder which was better than 99.9998% with a particle diameter less than 0.3 mm. To prevent the splattering of the source, some quartz wool were placed on the top of the crucible. Cleaned substrates put on to the masks inserted into the substrate holder. Source, substrate holder, hot wall and their thermocouples were placed as described in the evaporation systems.

System was evacuated firstly by rotary pump and then the diffusion pump. After reaching a vacuum level about 10^{-6} torr substrate, source and the hot wall were started to heat up. The required temperatures which were kept fixed until the source temperature achieved melting point of CdS (700 ^{o}C), of the substrate and hot wall were 200 ^{o}C and around 350 ^{o}C, respectively. After the evaporation started, shutter was opened to start deposition. Deposition took about 15-20 minutes.

3.3 Metallic Evaporation Systems

Metallic evaporation system was used to make electrical contacts on the films to produce Schottky devices. Indium contacts were taken on the Hall-bar shaped thin films to make conductivity measurement by these ohmic contacts. In order to investigate Schottky diodes' electrical properties, Au, Pt were evaporated on to the TO/CdS and ITO/CdS films. Evaporations were carried out by resistive

evaporation using the Nanotech evaporator system and by electron beam evaporation. Films and masks were placed on the copper substrate holder in a sandwich structure. In resistive evaporation, metal was placed in the molybdenum boat heated by manually controlled variac.

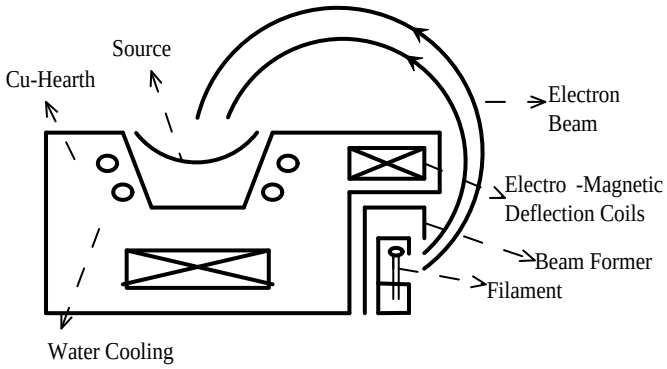

Figure 3.2: The major components of e-beam evaporator

In electron beam evaporation, high-energy beam of electrons are used to locally heat the material. To achieve desired vacuum level, turbo-molecular pump is used and pressure inside the chamber is measured by an ion gauge. A schematic diagram of a typical e-beam source is shown in Figure 3.2. Concentrated electrons can heat the evaporant to temperatures as high as 2500 ^{o}C. Thermionic electron gun with a tungsten filament as cathode part, is used to produce electrons. Major problem of this gun is that higher pressures cause scattering of the electron beam and shorten the cathode life because of the erosion by ion bombardment. Filament is located out of the direct line of sight of the evaporant and using magnetic

field, it is maintained that electron beams scan the surface of the evaporant by appropriate variation on the x and y components of the magnetic field. Scanning of the electron beam makes a uniform heating of the evaporant, so local hot spots are not formed. Evaporant is contained in the water-cooled crucible so only its surface gets to a high temperature and its metallurgical reaction with crucible is prevented.

3.4 Electrical Measurement

For the investigation of the electrical properties of the deposited CdS thin films, resistivity measurement (at room temperature) and Hall effect measurements were performed. Resistivity measurement was done with ordinary dc-measurement technique applied on the Hall-bar samples. Additionally, to find the electrical properties of the Schottky diodes, current-voltage and capacitance-voltage measurements were carried out at room temperature. The temperature dependent current-voltage behavior of Schottky devices was studied in the range of 200 K to 350 K by using Janis Liquid Nitrogen VPF Series Cryostat which is shown in Figure 3.4. Rotary pump is used to maintain desired vacuum inside the cryostat and the GaAlAs diode sensor is used to measure the sample temperature which is controlled by the LakeShore-331 temperature controller.

3.4.1 Resistivity Measurement

Resistivity of the CdS thin film was measured by the standard dc method at room temperature using Hall-bar type samples shown in Figure 3.3. A constant temperature was applied on the contacts 1 and 5 and the voltage drop across them were measured. These contacts were ohmic contacts so they didn't change the density of the carriers in the CdS film. Keithley 220 programmable constant current source and Keithley 619 electrometer were used in the above measurement.

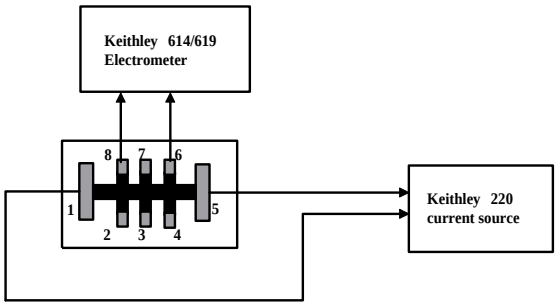

Figure 3.3: Resistivity measurement set up

Electrical resistivity can be calculated by the following expression:

$$\rho = \frac{wt}{L}\frac{V}{I}$$

where w is the width of the Hall-bar, L is the spacing of the contacts across which voltage is measured, t is the thickness of the film, I is the applied constant current and V is the measured voltage at this current value.

Travelling electron microscope having ± 10 μm error was used to measure the dimensions of the samples. Their measured total length and width were 1.15 cm and 0.22 cm, respectively.

3.4.2 Hall Effect Measurement

The Hall effect measurements were performed by dc-method in the temperature range 120 K $-$ 400 K. It is the simplest and the most often used system in the industry. Generally, this method is used when the sample resistance is in the range of $10^3 - 10^9$ ohms. The circuit design used in the Hall effect measurement

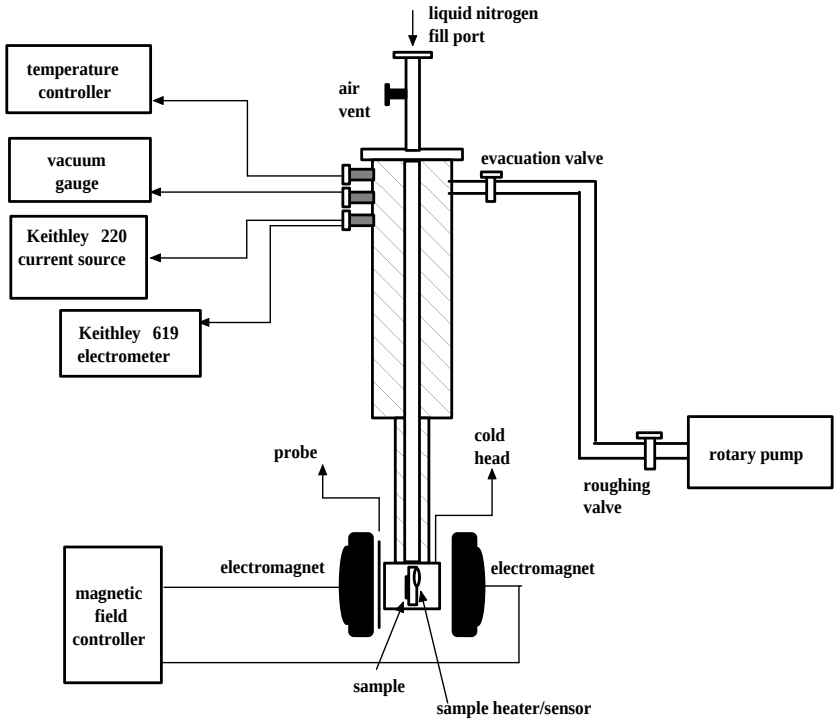

Figure 3.4: Experimental set up of the Hall measurement

for Hall-bar samples was the same as the one for resistivity measurement. The experimental set up of the Hall measurement is shown in Figure 3.4 where Walker Magnion Model FFC-4D electromagnet was used for producing the uniform 0.9 T magnetic field which was perpendicular to the current and the sample surface. Janis Liquid Nitrogen VPF Series Cryostat was used as it was used for the temperature dependent current-voltage measurement of Schottky diodes. Constant current is applied between the contacts 1 and 5 with Keithley 220 Current Source, and the Hall-voltage drop was measured between 3rd and 7th contacts by using Keithley 619 electrometer which is with a very high input impedance in forward and reverse directions for both the current and the magnetic field. These four different combinations of the current and the magnetic field were measured to eliminate unwanted voltages developed between the Hall-probes. These voltages are Nerst voltage (Ettinghausen voltage), thermoelectric voltage, contact voltage and Righ-Leduc effect resulting voltage. Measured four voltages are:

$$\begin{aligned} +B, +I &\Rightarrow V_1 \\ -B, +I &\Rightarrow V_2 \\ +B, -I &\Rightarrow V_3 \\ -B, -I &\Rightarrow V_4 \end{aligned}$$

By using them, the Hall-voltage can be calculated from the relation

$$V_H = \frac{V_1 + V_2 + V_3 + V_4}{4}$$

Actually, from this relation sum of the Hall voltage and the Ettinghausen voltage is found; but the Ettinghausen voltage is usually so small that it can be ignored.

3.4.3 Current-Voltage Measurement of Schottky Diodes

CdS thin films was deposited onto the soda lime glass substrates coated with tin oxide which was used as back contact. Then Au and Pt were evaporated to form the Schottky diodes. C and gold paste cold contacts were also applied onto the n-type films for the same reason. In order to investigate the rectifying behaviors of the contacts at room temperature current-voltage characteristics were obtained by connecting positive probes of Keithley 220 Current Source and Keithley 619 Electrometer to the metal contact and negative probes to the back contact. Then the voltage drop across the sample for different constant currents were measured.

The temperature dependent dark current-voltage measurements were done in the range $200\ \mathrm{K} - 350\ \mathrm{K}$ by using Janis Liquid Nitrogen VPF Series Cryostat at each successive 10 K increments in the temperature.

3.4.4 Capacitance-Voltage Measurement

Schottky barrier height, doping concentration and surface states density can be determined by measuring capacitance as a function of the bias voltage or

frequency. Metal-semiconductor junctions act as parallel plate capacitor with thin charged layer on metal side and a thick charged layer (depletion region) on the semiconductor side, as explained in sec.(2.5).

By superimposing a small ac signal on the dc bias voltage, diode's capacitance can be measured. These measurements were carried out by using HP 4192A LF Impedance Analyzer and data were taken by a software program written with Lab-view. These measurements were done in the frequency range of 500 Hz-1 MHz. The ac voltage oscillation level was set to 0.05 V for the frequencies below 200 kHz and 0.1 V for others. The dc bias voltage amplitude was varied from -1.5 V to 1.5 V with 0.05 V increments. This voltage was swept automatically at each setting of the frequency in the stated range.

3.5 Optical Characterization

3.5.1 Transmission Measurement

The optical properties of the vacuum evaporated CdS thin films have been studied by transmission measurements. Equinox 55 Fourier Transform Infrared Spectroscopy (FTIR) was used in these measurements. The basic optical component of FTIR is the Michelson interferometer shown in simplified form in Figure 3.5 [77, 78]. Incoherent light from the Si/Ge near infrared source is incident on a quartz beam splitter which creates two separate optical coherent light paths by reflecting half of the incident light and transmitting the remaining. One of

these two paths reflects from a fixed mirror and turns back to the beam splitter which partially reflects this light to the source and partially transmits to the detector. The other path reflects from a movable mirror and then it also turns back to the beam splitter where it is partially transmitted back to the source and partially reflected to the detector. Path difference of these two beams reaching

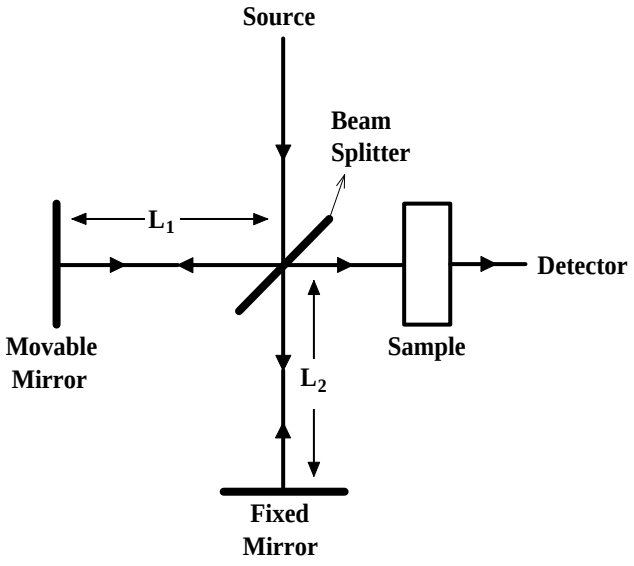

Figure 3.5: Schematic diagram of FTIR spectrometer

the detector is zero when L_1=L_2. By moving movable mirror, path difference can be changed and so the detector output, the interferogram, consists of series of maxima and minima. This measured quantity includes the spectral information of the source and the transmittance characteristics of the sample. Transmission data as a function of wavelength of incident photons are obtained by using a computer which makes a Fourier transform to give these desired information.

3.5.2 Photoresponse Measurement

The optical properties of Schottky diodes were obtained by photoresponse measurement. In this measurement a focused monochromatic light beam is incident on the metal side of the sample. 100 W halogen projector lamp was used as the light source and light was aligned with the entrance slit of Oriel MS 257 monochromator. The sample was placed in front of the exit slit as shown

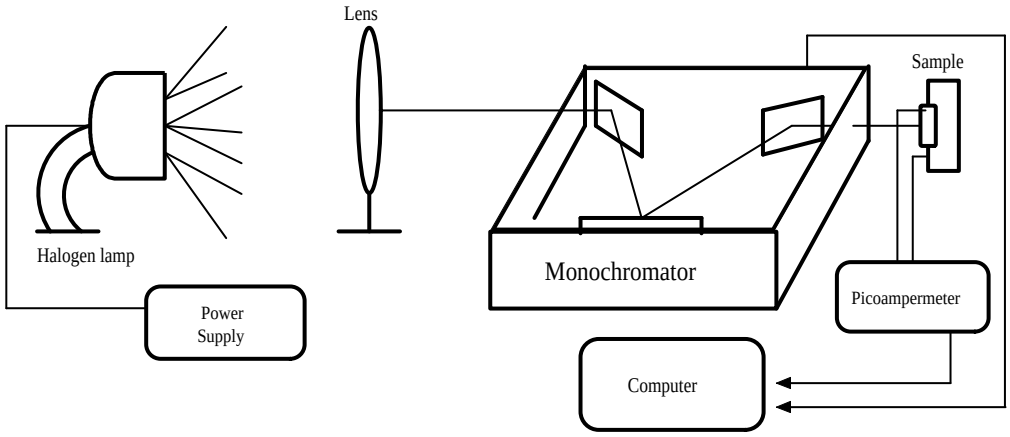

Figure 3.6: Photoresponse measurement system

in Figure 3.6. The short circuit photocurrent was measured in the wavelength range 450 A − 755 A by using HP 4140 picoampermeter/dc voltage source. By subtracting the current measured in dark from the measured photocurrent under illumination, net current was determined. This net current is corrected by dividing it to the spectral distribution of the light source.

3.6 Structural Characterization

X-ray diffraction technique is used to find the structural parameters of the deposited CdS thin films. X-ray diffraction measurements were carried out with using Rigaku Miniflex system equipped with Cu-K_α radiation of average wavelength 1.54059 A. Scan scale is set for the 2θ angle from 5^o to 80^o with scan speed of 2 ^{o}/min. Diffraction pattern was analyzed by using a computer software and ICDD database where specifically ICDD database was used to match the measured peak with one of the known structures.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Structural Properties of CdS Thin Films

CdS thin films deposited onto the soda lime glass slides were examined by X-ray diffraction (XRD) technique to find the structural characterization of the films. Figure 4.1 shows the typical XRD pattern of the samples. Diffraction

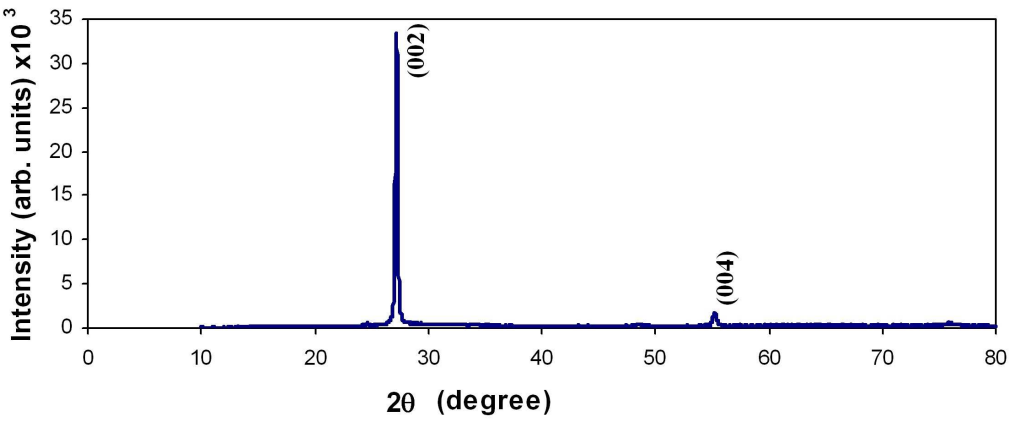

Figure 4.1: XRD pattern of CdS thin film

angles are shown in the figure. The strong XRD peaks at $2\theta \approx 27.22^o$ corresponds to the diffraction angles of the (002) plane of hexagonal CdS. The weaker peak at

$2\theta \approx 55.26^o$ also corresponds to hexagonal CdS with (004) plane. Therefore, the CdS films deposited on a glass substrate by vacuum deposition were of hexagonal structure and the c-axis of crystallites was mostly oriented perpendicular to the substrate. This results indicates that the grown films are polycrystalline.

4.2 Electrical Properties of CdS Thin Films

In this section, temperature dependence of the conductivity was studied in the temperature range of 180 K − 400 K to investigate the dominant current transport mechanism in CdS thin film. Typical temperature dependence of the polycrystalline CdS thin film's conductivity is seen in Figure 4.2. In this figure, conductivity increases with increasing temperature but this temperature dependence of the conductivity shows different nature in different temperature regions.

Transport mechanism, explained in chapter 2, can be investigated by the nature of the temperature dependence of conductivity. According to the possible conduction mechanisms, conductivity is given by:

- For thermionic emission [51]

$$\sigma\sqrt{T} = \sigma_0\, exp\left(\frac{E_a}{kT}\right)$$

- For thermally assisted tunnelling [50]

$$\sigma = \sigma_0\,[1 + \frac{F^2}{6}T^2]$$

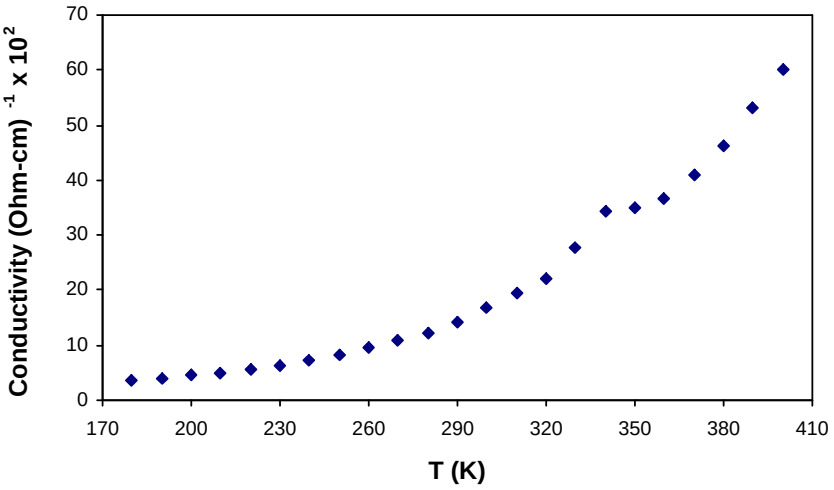

Figure 4.2: Variation of conductivity of CdS thin film as a function of temperature

where σ_0 and F are constants.

- For Mott's hopping mechanism [76]

$$\sigma\sqrt{T} = \sigma_0 exp\,(-\frac{T_0}{T})^{1/4}$$

where σ_0 and T_0 are constants.

To investigate the validity of thermionic emission type of transport mechanism σ-T data were replotted according to eqn.(4.2) as $\sigma T^{1/2}$ vs T^{-1} and illustrated in Figure 4.3. There are two linear regions with different slopes from which activation energies were calculated as 138 meV and 45 meV. This behavior indicates that different transport mechanisms dominate above 270 K and below 230 K with a transition region in temperature. The linearity of Ln($\sigma T^{1/2}$)-T^{-1}

plot above 270 K sufficiently high activation energy of 138 meV indicate that the thermionic emission is the dominant conduction mechanism above 270 K.

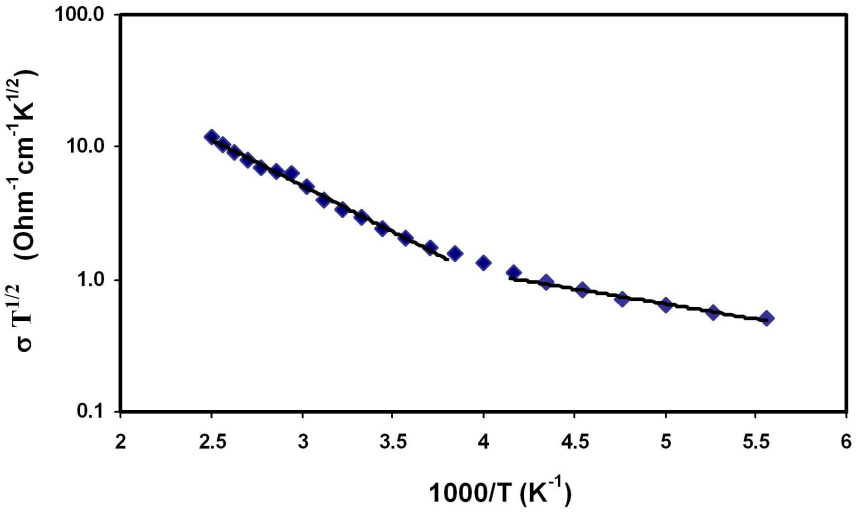

Figure 4.3: Ln(σT$^{1/2}$)-1000/T graph in the range of 180 K-400 K

Below 230 K even tough Ln(σT$^{1/2}$)-T^{-1} plot is linear, the activation energy value of 45 meV is slightly higher than kT which indicates that not the thermionic emission but a different transport mechanism dominates the conduction. Both the temperature range and the activation energy are high to observe hopping as a dominant transport mechanism so tunnelling was investigated in this temperature region. Thus σ-T data were replotted as σ vs T^2 according to eqn.(2.10) in the temperature range of 180 K $-$ 230 K. The linearity of this plot indicates that tunnelling mechanism dominates the conduction in this temperature interval.

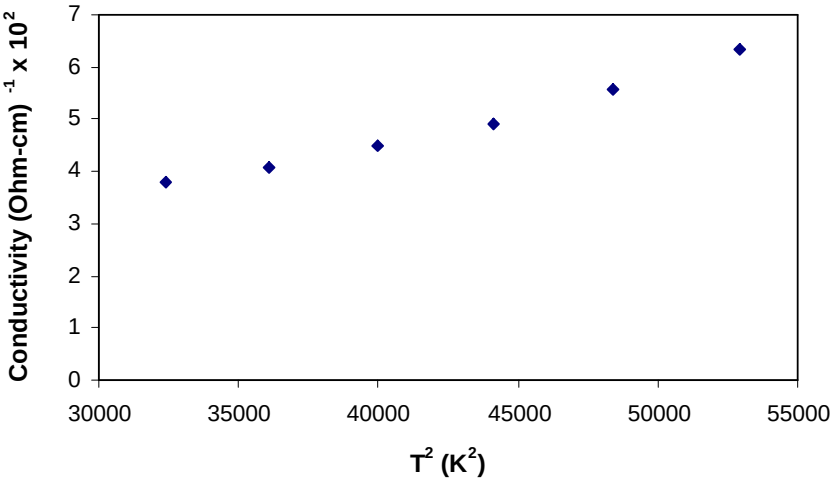

Figure 4.4: σ-T^2 graph in the range of 180 K-230 K

4.3 Optical Properties of CdS Thin Films

To investigate the optical properties of CdS thin film, optical absorption coefficient was calculated from the room temperature transmission data, measured in the photon energy range of 0.99 eV-2.72 eV (see Figure 4.5).

Absorption coefficient as a function of photon energy is calculated by using eqn.(2.38),

$$\alpha = \frac{1}{d} ln(\frac{I_0}{I})$$

where, d, film thickness values of the investigated films are around 1 μm. As explained in sec.(2.6.1), the relation between incident photon energy and absorption

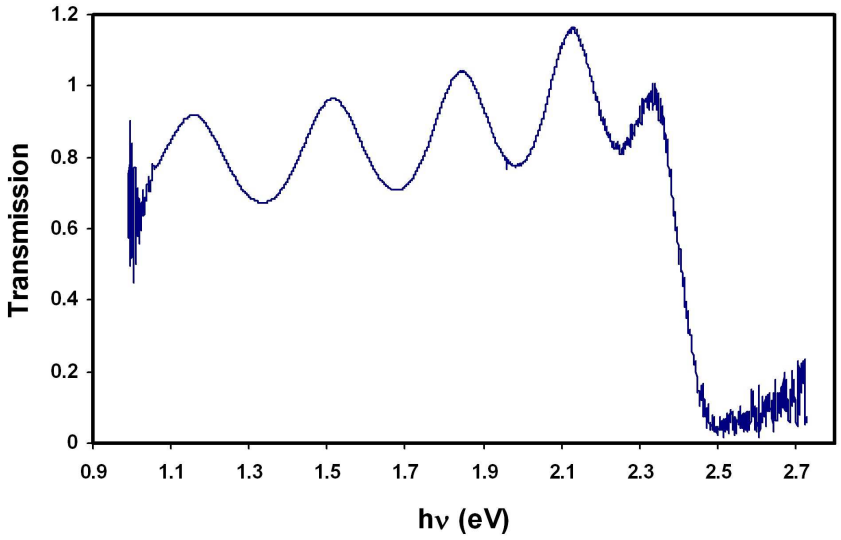

Figure 4.5: The transmittance of CdS thin film

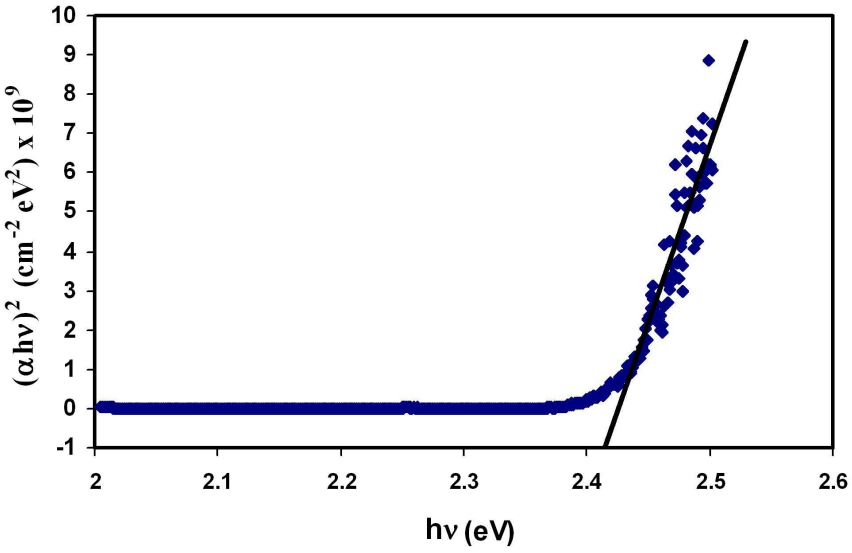

Figure 4.6: The variation of $(\alpha h\nu)^2$ as a function of incident photon energy

coefficient is given by eqn.(2.39)

$$\alpha(h\nu) = A(h\nu - E_g)^{1/2}$$

The plot of $(\alpha h\nu)^2$ vs incident photon energy, $h\nu$, shown in Figure 4.6 has a linear region above 2.4 eV indicating the allowed direct band transition. The direct band gap of CdS thin film found from the $h\nu$ axis intercept is around 2.42 eV which is perfectly consistent with the literature [65].

4.4 Characterization of Schottky Diodes

To produce and characterize Schottky diodes, CdS thin films were evaporated onto tin oxide and indium tin oxide coated glass substrates. Then Au and Pt were deposited onto these films by evaporation as it is described in sec.(3.3). Besides, gold paste and liquid colloidal graphite were used to fabricate cold gold and C contacts, respectively. These metals' work functions are given in table (4.1).

Typical linear dark I-V characteristic of the TO/CdS/Metal structures are given in Figure(4.7). These structures illustrate the exponential current voltage variations. However, for ITO/CdS/Metal structures, ohmic behavior was observed. To find the reason behind this, indium contacts were evaporated onto the ITO/CdS structures and from the current voltage characteristics obtained, it was noticed that there was a rectification. It is known that CdS makes an ohmic contact with indium; so, ITO must have made a rectification with CdS. In fact,

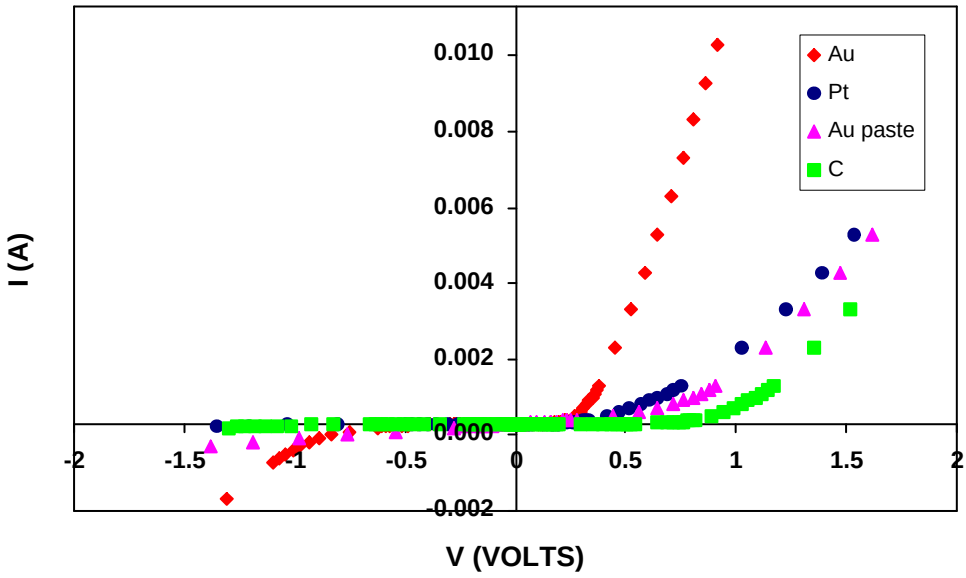

Figure 4.7: Current-Voltage characteristics of the Schottky barrier diodes with Au, Pt, C and gold paste onto the TO/CdS structures

in previous studies it is reported that the work function of ITO can raise above that of CdS with oxidation [79] and so ITO/CdS junction would be rectifying rather than ohmic [80].

Room temperature Log I-V variations are given in Figure 4.8 and Figure 4.9. Current-voltage characteristics of all of these Schottky diodes deviate from the exponential behavior due to series resistance at high voltages.

When series resistance, R_s, contributes to device behavior the diode voltage becomes $V_d = V_a - IR_s$. Thus, eqn.(2.20) becomes

$$J = J_s(\exp\left(\frac{qV_a - IR_s}{kT}\right) - 1) \tag{4.1}$$

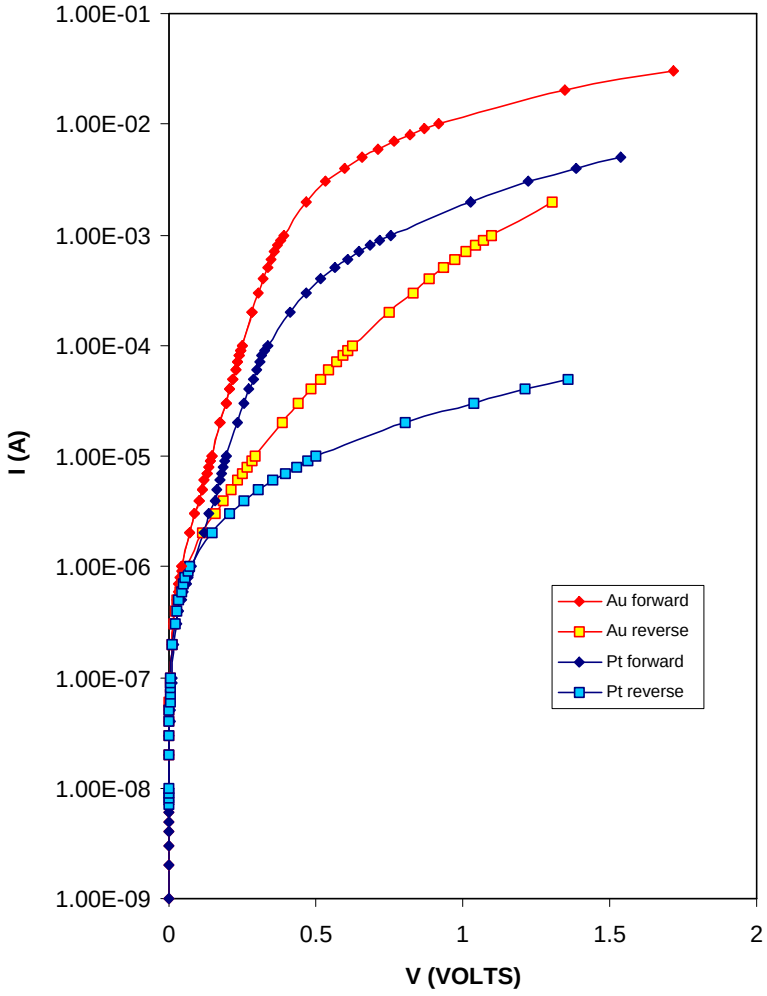

Figure 4.8: The room temperature Log I-V of the Schottky barrier diodes with Au, Pt on to the TO/CdS structures

Therefore, it can be determined from Figure 4.7 that gold contacts have the lowest series resistance. Gold and platinum diodes have the longest linear region in the Log I-V variation. Gold pastes' rectification, changes from half to three orders of magnitude for different samples. Pastes cannot be made identical, so they have

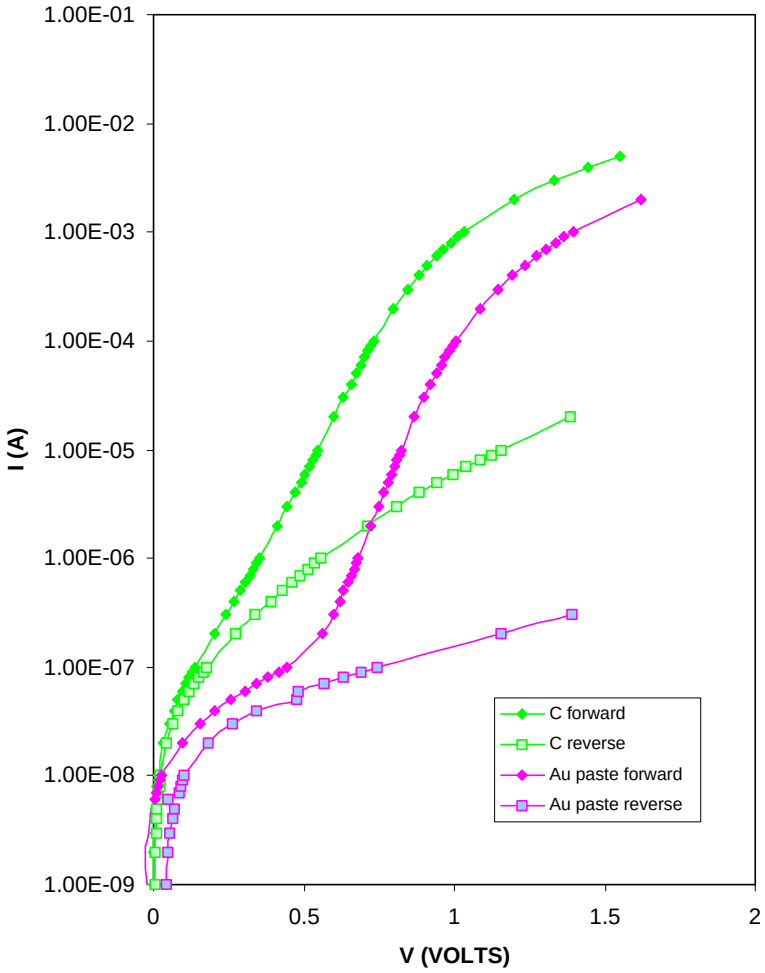

Figure 4.9: The room temperature Log I-V of the Schottky barrier diodes with C and gold paste on to the TO/CdS structures

very different shapes for each contact and also there may be a leakage into the film. The diode ideality factor values obtained from the linear parts of LnI-V variations are given in table 4.1.

The stable and reproducible structures are obtained with Au and Pt contacts. Therefore, the detailed characterization of the structures are given in the following

Table 4.1: The room temperature values of TO/CdS/Metal structures

Metals	Work Function (eV)	Ideality Factor
Au	5.1	1.8
Pt	5.65	2
C	4.6	3.2
Gold paste	5.1	2.6

sections for Au and Pt contacts.

4.4.1 Temperature Dependent Characterization

In order to analyze current transport mechanism of Schottky diodes with Au and Pt, the current voltage measurements were performed in the temperature range of 200 K − 350 K.The I-V variation of TO/CdS/Pt structures at different temperatures is illustrated in Figure(4.10). Diode ideality factors are found from the slopes of the Ln I vs V curves' linear parts. The ideality factor values decrease from 3.41 to 1.39 with increasing temperature. This variation of the ideality factor with temperature is shown in Figure 4.11. The ideality factor declines sharply up to 300 K and above this temperature it decreases slowly with increasing temperature. Saturation currents can be found from the interception of the extrapolated straight line of (linear part) Ln I vs V curves at V=0. The temperature dependence of zero bias barrier height evaluated from the saturation current which was explained in thermionic emission theory sec.(2.4.1) is shown

in Figure 4.12.

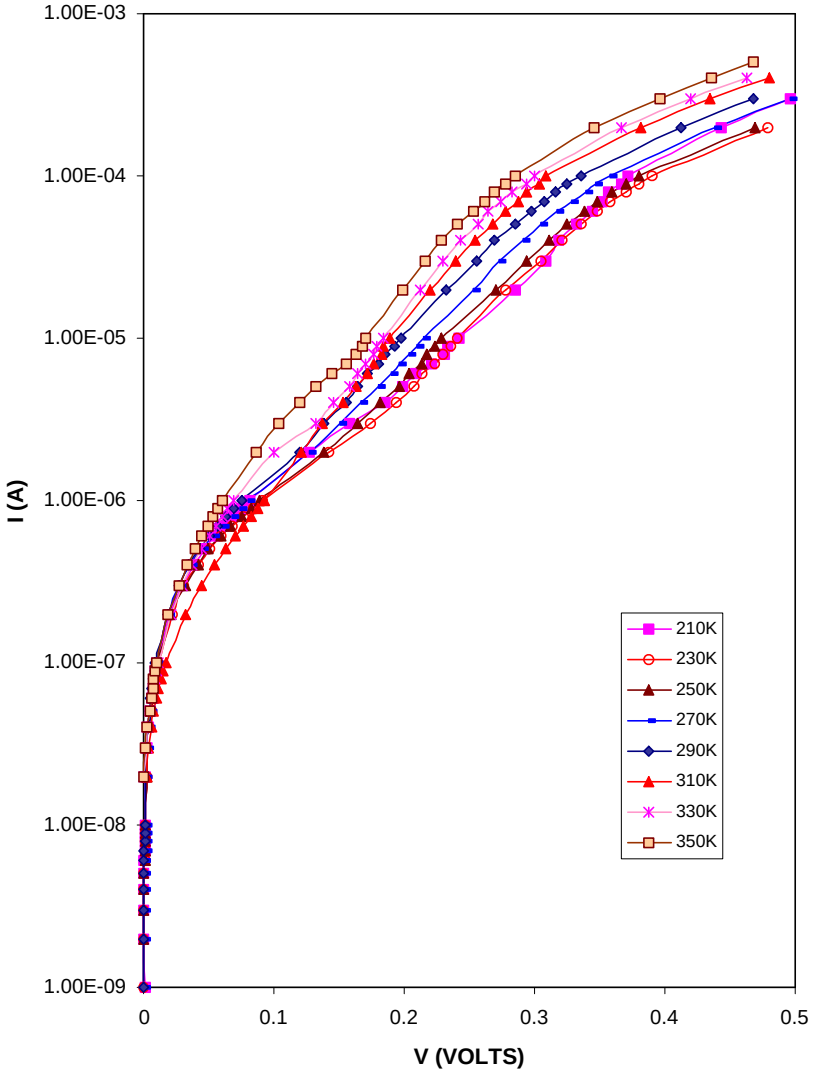

Figure 4.10: Forward LnI-V characteristics of the TO/CdS/Pt at different temperatures

It increases from 0.42 eV to 0.77 eV with the rise in the temperature as dependence of the barrier height can be evaluated by $\phi_{bo}(T) = \phi_{bo}(0) + \alpha T$

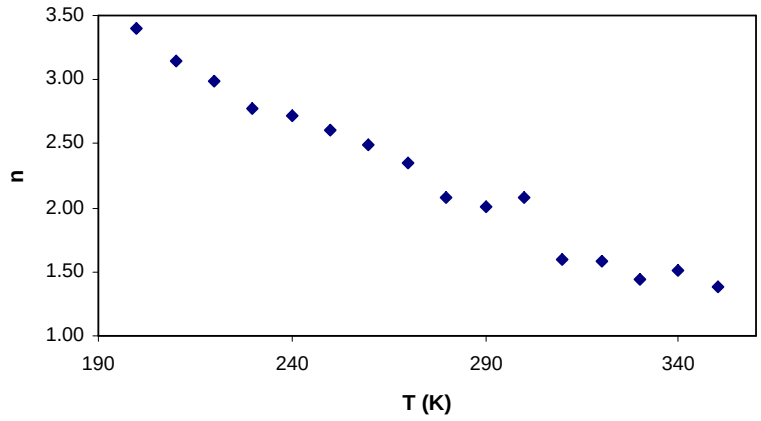

Figure 4.11: Variation of the ideality factor of TO/CdS/Pt with temperature

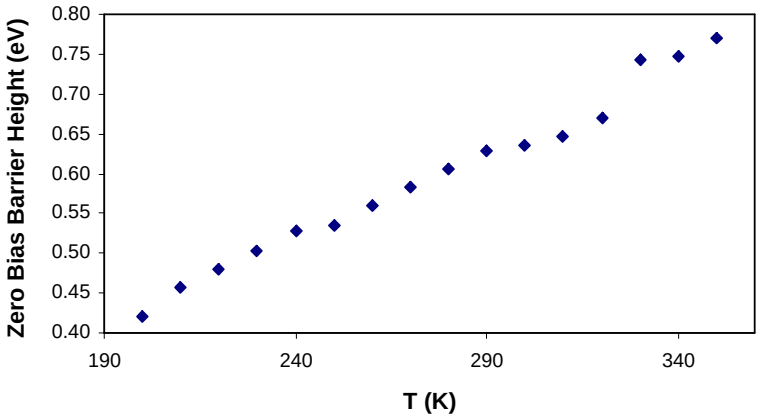

Figure 4.12: Variation of the zero-bias barrier height of TO/CdS/Pt with temperature

where α is the temperature coefficient of the barrier height [81]. By fitting of the experimental data, α=0.0022 eVK^{-1} and $\phi_{bo}(0)$=0.0107 eV are found.

Both the decrease in ideality factor and increase in barrier heights with rise in temperature and the high ideality factor values are indicative of the deviation from the thermionic emission-diffusion theory. On the other hand, above 300 K ideality factor becomes nearly constant and smaller so the thermionic emission-diffusion theory may become dominant in this temperature region.

The forward I-V characteristics of Au Schottky barrier diode on TO/CdS at different temperatures is shown in Figure 4.13. The variations are linear over two to three orders of current. The slopes of these linear regions are around 22 V^{-1} for all temperatures. The zero bias barrier height and ideality factor values were plotted as a function of temperature with the same method used for Pt in Figure 4.14 and Figure 4.15. This zero bias barrier height increases from 0.41 eV to 0.72 eV and the ideality factor decreases from 2.67 to 1.50 with increasing temperature.

From the experimental data, α =0.0021 eVK^{-1} and $\phi_{bo}(0) = 0.0015$ eV were found. Saturation current density, J_s (eqn.(2.21)), of the thermionic emission-diffusion theory can be used to calculate the Richardson constant A^*. The ordinate intercept of $Ln(I_s/T^2)$ vs 1/T plot shown in Figure 4.16, gives $Ln(A^*A_d)$, where A_d is the diode area. However, this cannot give a reasonable value because the variation of the barrier height with temperature wasn't taken into account. When the correction is made, the intercept of $Ln(I_s/T^2)$ vs 1/T yields $Ln(A^*A_d) - \alpha q/k$ [81]. From this relation A^* was found to be 127 A $cm^{-2}K^{-2}$,

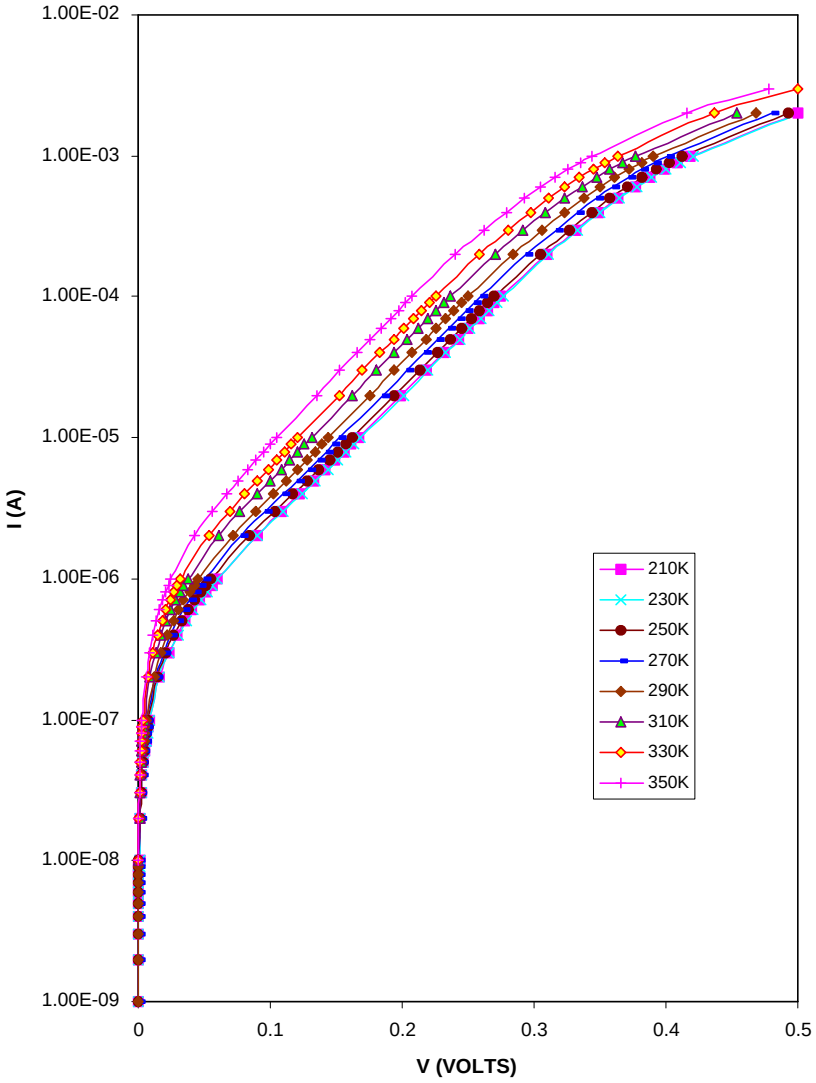

Figure 4.13: Forward LnI-V characteristics of the TO/CdS/Au at different temperatures

which is much higher than the known value. Increase in ideality factor, decrease in barrier height with decrease in temperature and too high value of the Richardson constant which is calculated from experimental data are at first sight indicative

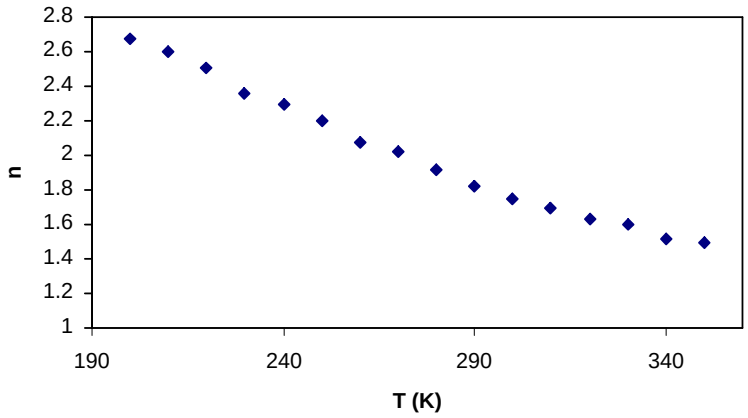

Figure 4.14: Variation of the ideality factor of TO/CdS/Au with temperature

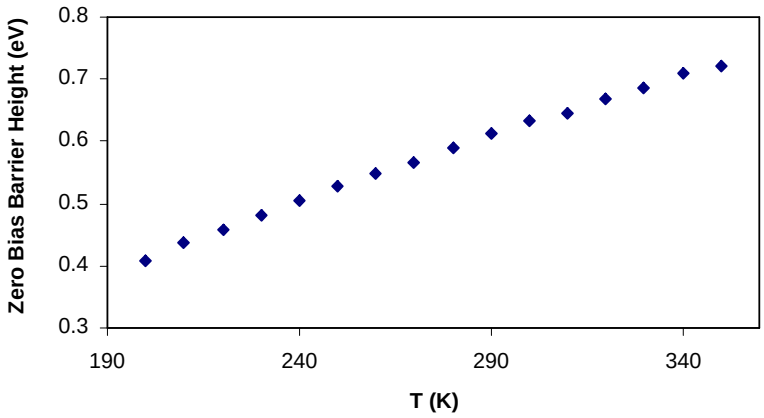

Figure 4.15: Variation of the zero-bias barrier height of TO/CdS/Au structure with temperature

of the deviation from pure thermionic emission-diffusion theory. This occurs perhaps due to the current resulting from other processes, namely tunnelling through the barrier and recombination in the depletion region.

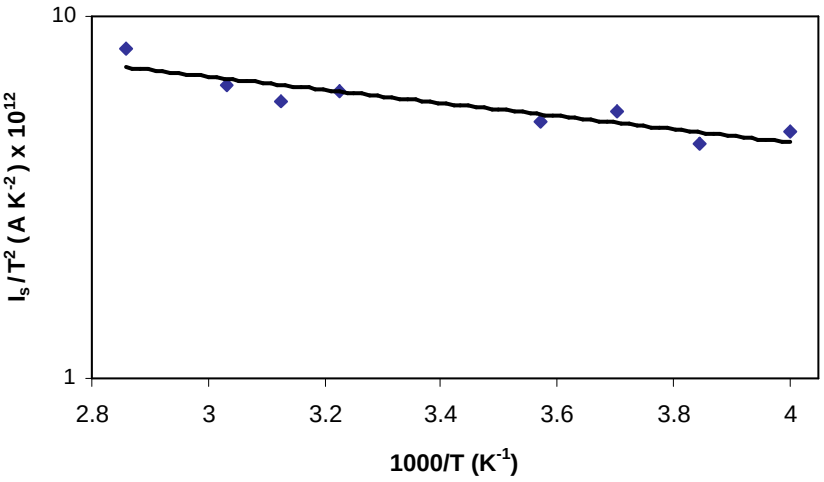

Figure 4.16: $\mathrm{Ln}(I_s/T^2)$ versus 1000/T plot of TO/CdS/Au

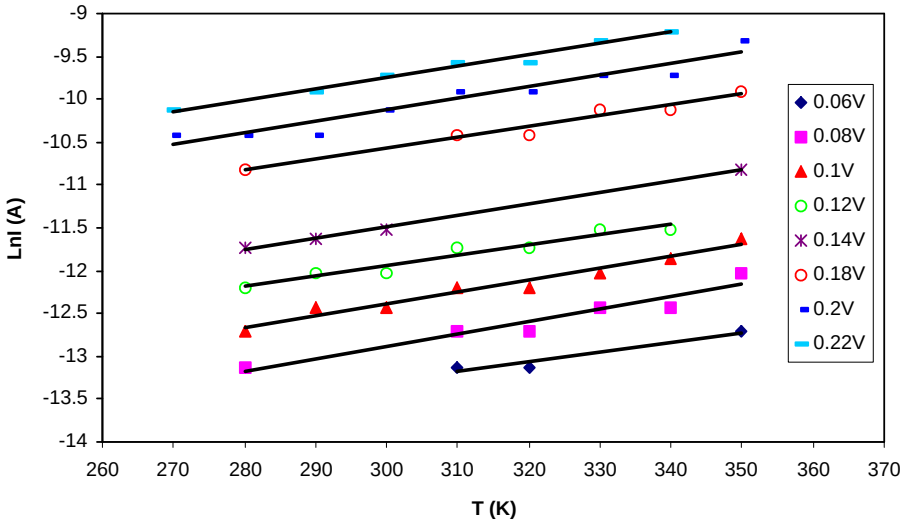

Figure 4.17: Variation of the current with temperature for TO/CdS/Au

It can be seen in Figure 4.13 that the slopes of the Ln I vs V variation are nearly constant at different temperatures; this is an indication of the tunnelling behavior. Ln I was replotted as a function of T to capture the effect of the tunnelling mechanism on the current transport. Ln I vs T plots at several voltages were found to be linear as shown in Figure 4.17. Below 270 K, current does not change with temperature. Tunnelling can be suggested as the current transport mechanism in the light of all above behaviors. The parameter that determines the relative importance of tunnelling (thermionic-field emission or field emission) and thermionic emission-diffusion is given by [59, 60]

$$E_{00} = \frac{h}{4\pi}\left(\frac{N_d}{m_e^* \varepsilon_s}\right)^{1/2}.$$

Corresponding E_{00} value is 20 meV with $m_e^* = 0.235\, m_0$ and $\varepsilon_s = 11.6\, \varepsilon_0$. Moreover, the donor concentration found from C-V measurement was used for the calculation of E_{00}. This makes E_{00}/kT to be equal to 1 at 230 K. For the Pt contacts at same temperature, it is equal to 0.08, which is a very low value. According to the theory, field emission (FE) becomes important when $E_{00} \gg kT$, whereas thermionic field emission (TFE) dominates when $E_{00} \sim kT$, and thermionic emission-diffusion dominates if $E_{00} \ll kT$ [82, 64]. Obviously, for TO/CdS/Au diodes thermionic-field emission is the dominant current transport mechanism. The current-voltage relationship in the case of tunnelling through the barrier is

of the form [59, 60]

$$I_t = I_{t0} exp\left(\frac{qV}{E_0}\right)$$

where

$$E_0 = E_{00} coth\left(\frac{E_{00}}{kT}\right).$$

From the slope of the Ln I vs V plot (see Figure 4.13) E_0 was found to be in the range 44 meV-47 meV. When these E_0 values are fitted in to eqn.(2.25), E_{00} value was found to be 46 meV which is two times of the value estimated from eqn.(2.23). Tunnelling can be enhanced by an increase in the electric field at the junction's interface [83, 84]. Such a field enhancement can occur at the edge of the sample, or it can be related to the local charge defects at the interface. Tunnelling can also be enhanced by the interface states which act as assisting centers in the tunnelling process [85]. It is known that tunnelling is observed only in highly doped semiconductors. Although samples used in this work were not doped, they are n-type because of the sulfur vacancy whereas generally it is not enough to observe tunnelling as a current transport mechanism. Investigations in previous studies, which were made by using XPS showed that Au appeared to disrupt the CdS surface and cause some out-diffusion of S, i.e. surface becomes Cd rich [31]. Therefore, its surface becomes highly n-type and so, observing tunnelling as the current transport mechanism is an expected result. In this work such a disruption may have occurred and made samples highly n-type.

The recombination current as described in Chapter 2 is given by eqn.(2.26)

$$J_{rg} = \frac{qn_iW}{2\tau_0}\,[\,exp(\frac{qV}{2kT}) - 1\,]$$

with $n_i = (N_cN_v)^{1/2}exp(-E_g/2kT)$. Here E_g is the band gap and N_c and N_v are the effective conduction and valence band density of states, respectively. Other parameters were described in Chapter 2. Because, there is $(N_cN_v)^{1/2} \sim T^{3/2}$ relation, the energy band gap can be determined from the slope of the $\mathrm{Ln(J}_{rg}\mathrm{/T}^{3/2})$ versus 1/T plot. From this plot E_g, was found to be 0.09 eV, which is a quite low value. Besides, the depletion region recombination generation current is expected to become important only for Schottky diodes at low temperatures with large barrier height and lightly doped semiconductors with low carrier lifetime. Therefore, recombination current is insignificant.

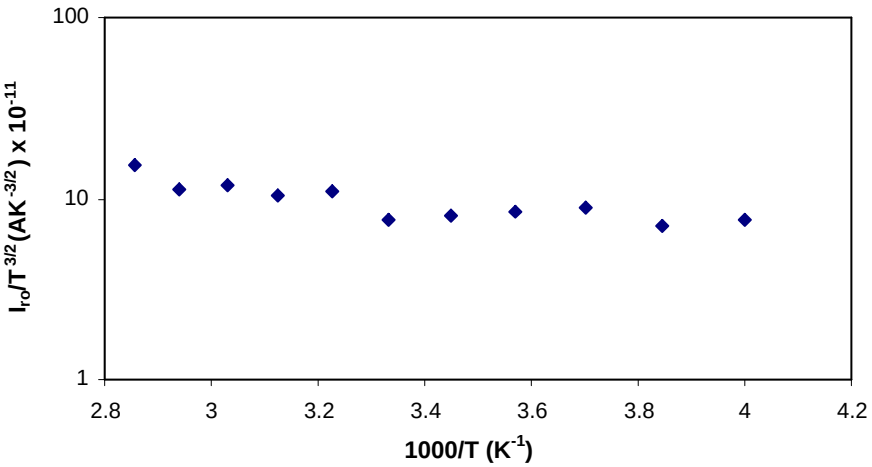

Figure 4.18: $\mathrm{Ln(I}_{r0}\mathrm{/T}^{3/2})$ versus 1000/T plot of TO/CdS/Au

According to thermionic emission-diffusion theory, Schottky barrier diode's reverse saturation current density is given by the following expression

$$J_{R0} = A^* T^2 exp\left(\frac{-\phi_{b0}}{kT}\right). \tag{4.2}$$

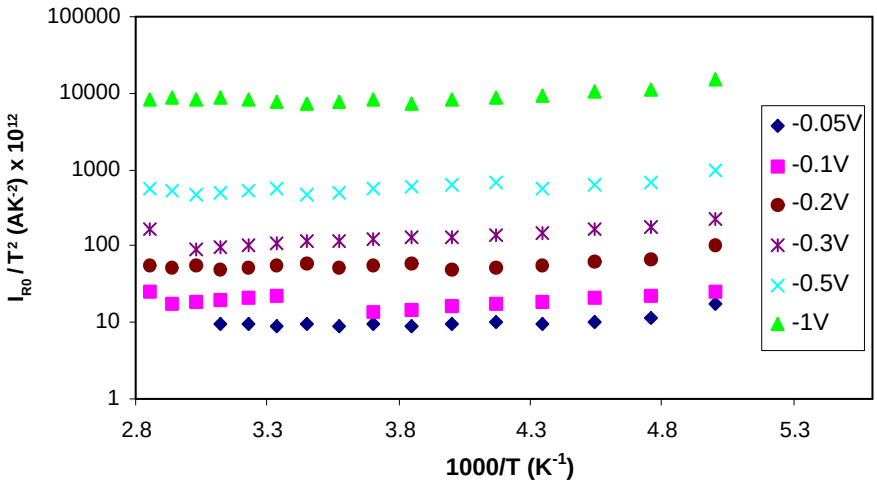

Figure 4.19: Ln(I_{R0}/T^2) versus 1000/T plot of TO/CdS/Au under various reverse bias

This saturation current has not been observed in practical devices due to the electric field dependence of barrier height, tunnelling and generation of electron hole pairs in the depletion region. The Ln(I_{R0}/T^2) vs 1000/T plots show a soft characteristic as seen in Figure 4.19. Therefore, thermionic emission cannot be dominant reverse current mechanism [81].

Electric field increase with reverse bias, make the reverse current increase as exp($\Delta\phi_B$/kT), where $\Delta\phi_B$ is the barrier lowering at reverse bias. Image force

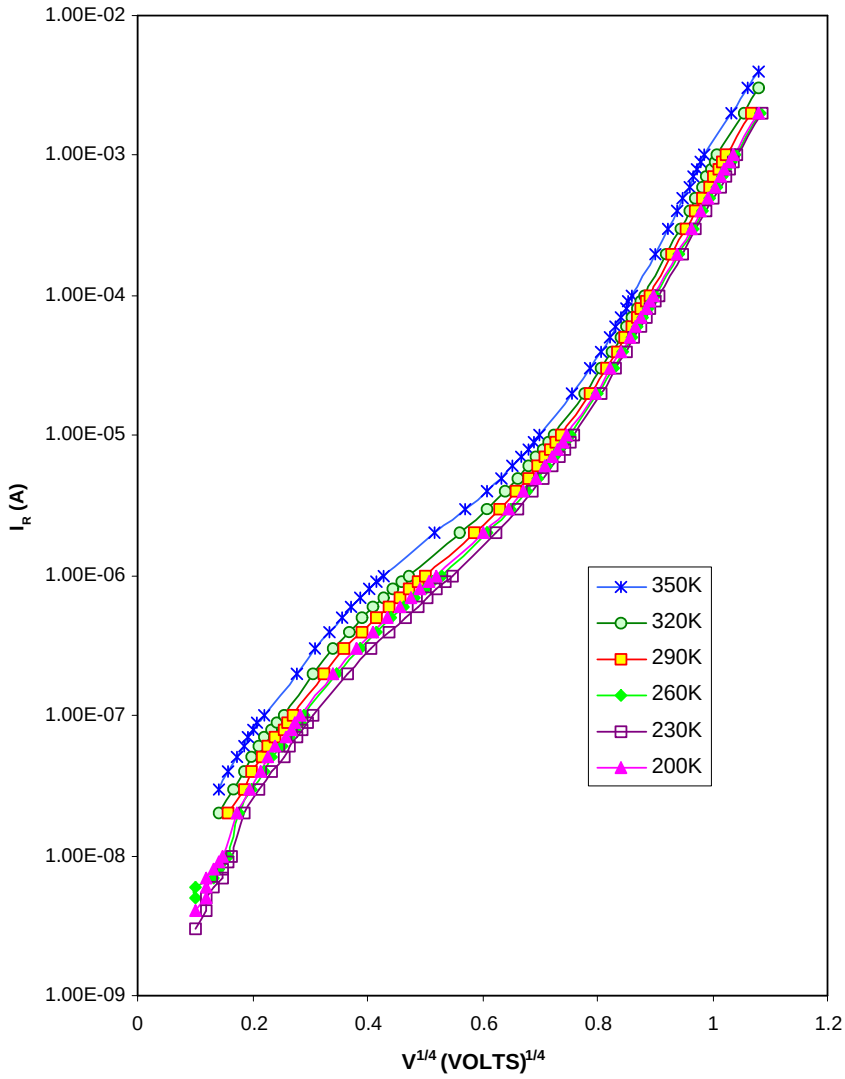

Figure 4.20: Ln(I_R) versus reverse bias $V^{1/4}$ plot of TO/CdS/Au

barrier lowering is an unavoidable effect that makes the barrier height depend upon the electric field in the depletion region. This barrier lowering is given by [65],

$$\Delta\phi_B = \left(\frac{q^3 N_d}{8\pi^2 \epsilon_d^2 \epsilon_s}(V_{bi} + V_R)\right)^{1/4} \tag{4.3}$$

where ϵ_d is image force permittivity, V_R is reverse current, V_{bi} is the built-in potential and others have meanings given in chapter 2. The plot of Ln I_R against $V_R^{1/4}$ above about reverse 0.4 V, is a straight line; so, image force barrier lowering must be dominant above this voltage.

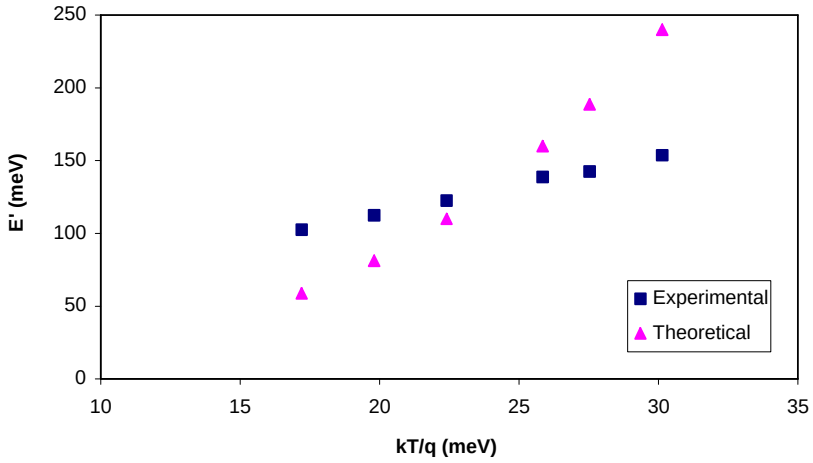

Figure 4.21: Theoretical and experimental values of E′ as a function of temperature of TO/CdS/Au

Since thermionic field emission is the dominant forward conduction mechanism, tunnelling (FE or TFE) can also be the dominant mechanism for the reverse characteristic. In the range where TFE becomes dominant mechanism,

the reverse current can be written as [59]

$$J_R = I_{RO} exp\left(\frac{qV_R}{E'}\right) \tag{4.4}$$

where

$$E' = E_{00}[(E_{00}/kT) - tanh(E_{00}/kT)]^{-1}.$$

From the slope of Ln J_R vs V_R, the energy E' was found at various temperatures. The E_{00} value found for forward characteristic was used to calculate E' theoretically. However, values found from this graph do not show a good agreement with the theory demonstrated in Figure 4.21. FE tunnelling may occur instead of TFE.

4.5 Capacitance-Voltage Characteristics

Capacitance-voltage measurements were done to find the barrier height, donor concentration and the surface states density. Generally, barrier heights deduced from this method are larger than those obtained from current-voltage or photoresponse measurements. This situation can result from several reasons. One of them is the image force barrier lowering. By using C-V method, the flat band barrier height is measured while by using the other two methods, the zero bias barrier height is obtained. Tunnelling of the electrons from metal into the semiconductor forbidden gap can be an another reason. Because of this tunnelling, metal has positive and semiconductor has negative net charge, so the barrier's parabolic

shape is distorted. I-V and photoresponse measurements, give the maximum barrier height of this distorted shape whereas C-V method gives the undistorted barrier height as if the barrier shape remains parabolic.

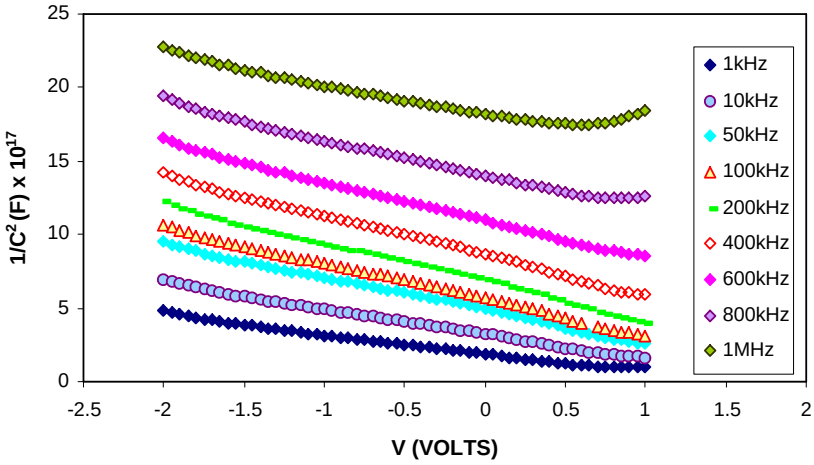

Figure 4.22: The plots of C^{-2}-V of TO/CdS/Pt at various frequency

In Figure 4.22, typical C^{-2} vs V variation of TO/CdS/Pt Schottky diode in the frequency range 1 kHz-1 MHz is shown. The slopes of these plots are equal to $2/A^2 q\epsilon_s N_d$ as explained in sec.(2.5). The donor concentration was determined from this slope; it is about 10^{24} m^{-3} for this sample. Barrier height found from the voltage axis intercept was unacceptably high. Image force barrier lowering alone cannot explain this value. This may have occurred because of the followings: a) low variation of the capacitance with reverse bias, b) effect of tunnelling as explained above c) thin oxide layer between the film and Au contact. In the forward direction, the capacitance curve shows a peak around 0.75 V at 1 MHz

frequency. This peak is seen in C^{-2}-V plot as a turning point. This peak is also observed at higher forward voltage for lower frequency. This decrease of capacitance results from imperfect back-contacts [86] or from the effect of series resistance [87].

The variation of capacitance with the frequency at zero bias is illustrated in Figure 4.23. The excess capacitance can be observed at low frequencies. This difference in capacitance between low and high frequency is attributed to interface states. The interface states capacitance depends on the forward bias and frequency [67].

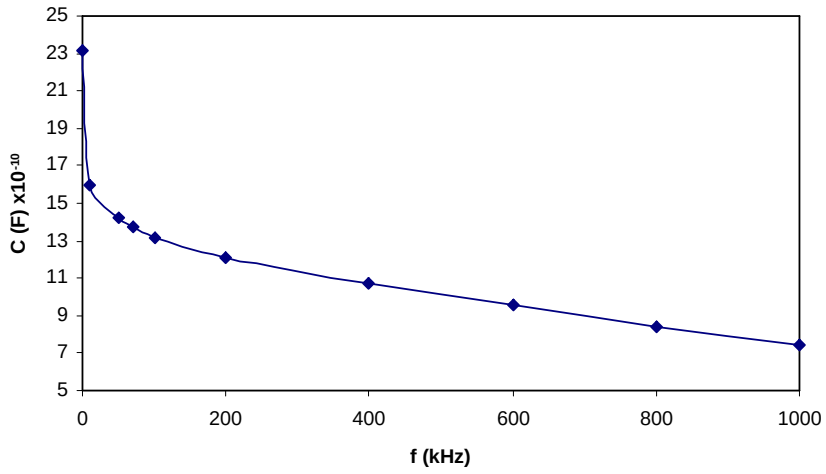

Figure 4.23: Variation of capacitance as a function of frequency of TO/CdS/Pt structures at zero bias

At sufficiently high frequency, interface states do not contribute to capacitance because the charge at interface states cannot follow the a.c. signal. As explained

in Chapter 2, at low frequency measured capacitance value approximately equals to the sum of the space charge capacitance and the interface states capacitance whereas at high frequency it equals only space charge capacitance. Interface states capacitance, C_{ss}, as a function of frequency is determined by subtracting space charge capacitance from the measured capacitance value.

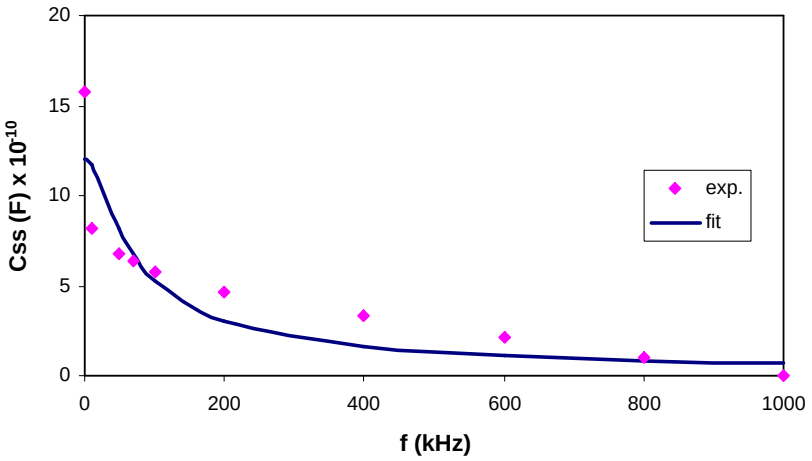

Figure 4.24: Variation of interface states capacitance as a function of frequency of TO/CdS/Pt structures at zero bias

The interface state density, N_{ss}, for small values of frequency is given by eqn.(2.36),

$$N_{ss} = \frac{C_{ss}}{qA}$$

The value of C_{ss} used for the determination of N_{ss} is taken as the vertical axis intercept value. Interface states density, N_{ss}, found from eqn.(2.36) is around $1.3\,\mathrm{x}10^{12}$ $\mathrm{cm}^{-2}\mathrm{eV}^{-1}$. Besides, fitted values of N_{ss} and relaxation time τ can also

be determined by fitting the C_{ss} values into eqn.(2.35),

$$C_{ss} = qAN_{ss}\frac{arctan(w\tau)}{w\tau}$$

From this fitting procedure (see Figure 4.24), the N_{ss} and τ values are found to be 9.6 x10^{11} cm^{-2}eV^{-1} and 0.03 s, respectively.

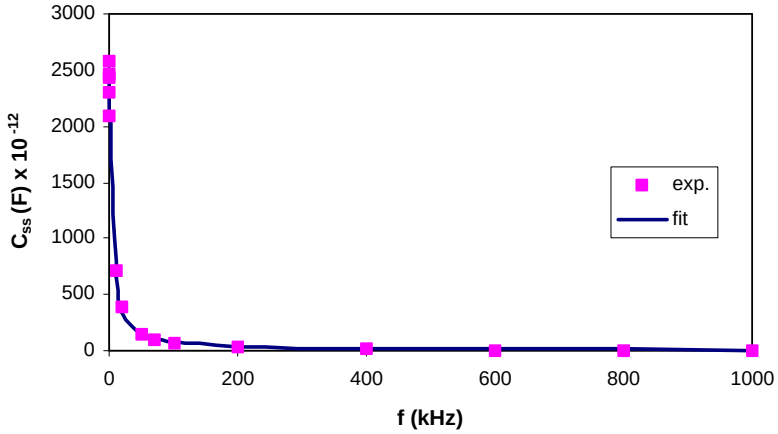

Figure 4.25: Variation of interface states capacitance as a function of frequency of Pt contact at zero bias

For the Pt and Au contacts interface states densities are found to be about 2.1 x10^{12} cm^{-2}eV^{-1} and 4.4 x10^{11} cm^{-2}eV^{-1} from eqn.(2.36) for a different sample, respectively. The difference in the N_{ss} values of Au and Pt contacts may have resulted from the difference in the oxide layer width which is formed when the contacts were produced on the film. As seen in Figure 4.25 the fitted curve represented by dashed lines has a nearly perfect consistence with the experimental data of the Pt contact for this sample. The fitted N_{ss} values are 1.9 x10^{12} cm^{-2}eV^{-1} for

Pt contact and 4.3 x10^{11} $cm^{-2}eV^{-1}$ for Au contact, respectively. The relaxation time value of Pt contact which is also found from the fitting procedure is equal to 0.5 s and of Au contact is equal to 0.02 s.

4.6 Spectral Response Characteristics

The spectral distribution of photocurrent of TO/CdS/C thin film diode was measured using front wall illumination in the wavelength range 450 A- 755 A. The typical corrected result of photocurrent as a function of photon energy is shown in Figure 4.26.

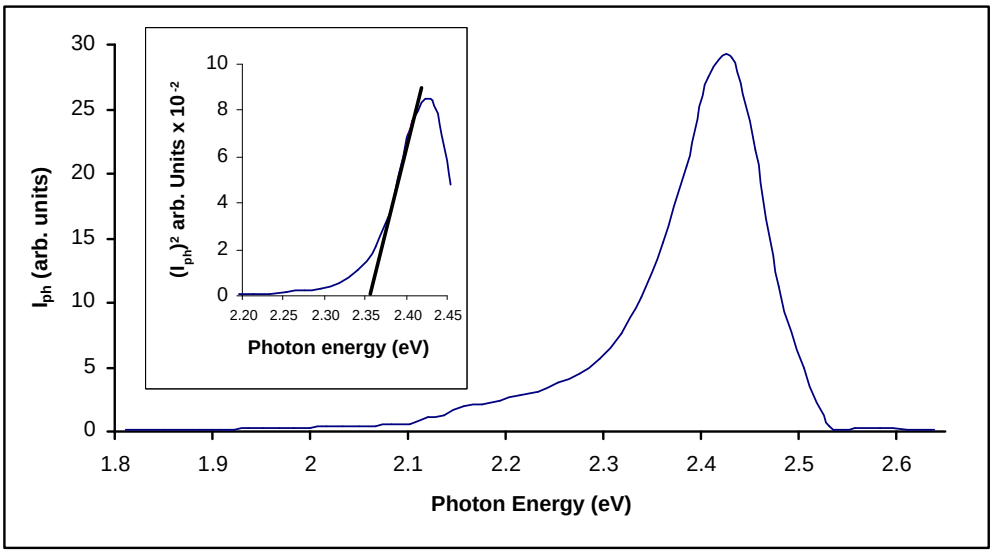

Figure 4.26: The photocurrent as a function of photon energy for TO/CdS/C structure and insert shows square of the photocurrent as a function of photon energy

The photoelectric threshold at low photon energies resulted from photoelectric

emission from carbon into the CdS. After the threshold value at low photon energy, short circuit photocurrent increases gradually with increasing photon energy and reached a maximum value at photon energy of 2.43 eV. This sharp increase was associated with band to band electron-hole pairs creation in the depletion region of the CdS layer. According to Fowler theory, for photon energies, $h\nu > E_g$, the direct band gap and the photocurrent relation is given by,

$$I_{ph}^2 \alpha \left(h\nu - E_g\right) \tag{4.5}$$

Therefore, from the plot of the square of the photocurrent against the photon energy, direct band gap of CdS can be obtained as 2.35 eV as shown in inset of Figure 4.26. After the maximum value, photocurrent decreases gradually with increasing photon energy because absorption takes place at the surface. Photons' penetration depth decreases with increasing their energy; so, electron-hole pairs are produced at the surface and before they diffuse into the depletion region they are recombined by majority carriers.

CHAPTER 5

CONCLUSION

Electrical characterization of the metal-CdS contacts is the main objective of this thesis. In this respect doping concentrations,ideality factor of Schottky diodes and finally current transport mechanisms were found. Besides, structural, optical and electrical characterization were made on thin CdS films to check the film parameters' eligibility to device production.

The produced films were polycrystalline and n-type and their band gaps were about 2.4 eV. All of these properties were consistent with the vacuum deposited CdS thin films in literature. However, not surprisingly the films were highly resistive, 700 Ω-cm, because of a high degree of compensation. Two different dominant current transport mechanisms were found in the films. One of them is thermionic emission in the temperature range 270 K-400 K with activation energy 138 meV. The other one is tunnelling in the range 180 K-230 K with activation energy 45 meV.

Schottky diodes were fabricated with Au, Pt, C and Au-paste. All contacts had a non-ideal behavior, i.e. their ideality factor were higher than 1. Some of

Au-paste contacts gave the best rectifying behavior but they were not stable. The second best rectifying was by Pt contacts but their resistivities were the highest. Au contacts had the lowest series resistance and tunnelling was determined as a current transport mechanism for these contacts. Above reverse 0.4 V, image force barrier lowering was observed. Reverse dominant current transport mechanism was again tunnelling. Doping concentration found from C-V measurement was about 10^{24} m^{-3} and interface states density was nearly 10^{12} $cm^{-2}eV^{-1}$. Capacitance frequency behavior of Au was nearly fit the theory. However, Pt contacts' capacitance frequency behavior had a perfect consistence with theory. From the optical characteristic of TO/CdS/C contact, band gap was found to be around 2.4 eV.

It was determined by using I-V characteristic that there was a barrier between indium-tin-oxide and CdS. To conclude as such, In contacts were deposited onto the ITO/CdS structure and then rectifying behavior was observed at their I-V characteristics. It is known that ITO/CdS structure can show such a behavior for some oxide level of the ITO.

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