A NOVEL TWO-PARAMETER MODULATION AND NEUTRAL POINT POTENTIAL CONTROL METHOD FOR THE THREE-LEVEL NEUTRAL POINT CLAMPED INVERTER

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Approval of the Graduate School of Natural and Applied Sciences

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ABSTRACT

A NOVEL TWO-PARAMETER MODULATION AND NEUTRAL POINT POTENTIAL CONTROL METHOD FOR THE THREE-LEVEL NEUTRAL POINT CLAMPED INVERTER

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In this thesis, the neutral point potential drift/fluctuation of the three-level neutral point clamped inverter is analyzed and a novel control algorithm, the two-parameter PWM method is proposed to confine the neutral point potential variation to a very small range. The two-parameter PWM method provides superior neutral point potential control performance even with small DC bus capacitors. The method is based on PWM pulse pattern modification and requires no additional hardware. Detailed analytical models of the neutral point current and potential as a function of the modulation parameters are established and the neutral point potential behavior is thoroughly investigated. Based on the study, the deficiency of the known methods is illustrated and the two-parameter PWM method is developed and its superior performance demonstrated. The performance of the two-parameter PWM method is verified by means of computer simulations utilizing both the per-PWM-cycle average model and the detailed model of the inverter. The results are supported by laboratory experiments involving both an R-L load and an induction motor drive.

Keywords: Three-level inverter, NPC, neutral point potential, PWM, space vector

ÖZ

ÜÇ DÜZEYLİ NÖTR NOKTASI BAĞLANTILI EVİRİCİ İÇİN İKİ PARAMETRELİ MODÜLASYON VE NÖTR NOKTASI DENETİM YÖNTEMİ

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Bu tezde, üç düzeyli nötr noktası bağlantılı eviricinin nötr noktası gerilim kayması/dalgalanması analiz edilmiş ve nötr noktası geriliminin değişimini çok küçük bir aralığa sınırlayan özgün bir denetim yöntemi önerilmiştir. Küçük doğru gerilim bara kondansatörleriyle bile üstün başarımı olan iki değişkenli darbe genişlik modülasyonu algoritması önerilmiştir. İki değişkenli darbe genişlik modulasyonu yöntemi darbe şablonunun değiştirilmesine dayanmaktadır ve ek donanım gerektirmemektedir. Nötr noktası akımı ve geriliminin ayrıntılı analitik modeli modulasyon değişkenlerinin fonksiyonu olarak ifade edilmiş ve nötr noktası gerilimi davranışı ayrıntılı olarak incelenmiştir. Yapılan analizlere dayanılarak, bilinen denetim yöntemlerinin yetersizlikleri gösterilmiştir ve iki değişkenli darbe genişlik modülasyonu yöntemi geliştirilmiştir. İki değişkenli darbe genişlik modülasyonu yönteminin başarımı bir darbe genişlik modülasyonu ortalama değer modeli ve ayrıntılı model bilgisayar benzetimleri ile doğrulanmıştır. Elde edilen sonuçlar R-L tipi yük ve asenkron motor sürücü laboratuvar deneyleri ile desteklenmiştir.

Anahtar Kelimeler: Üç düzeyli evirici, nötr noktası bağlantılı (NPC), nötr noktası gerilimi, darbe genişlik modülasyonu (PWM), uzay vektörü

To My Family,
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for their patience and support
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CHAPTER 1

INTRODUCTION

1.1 Electrical Motor Drives

Electric energy is important part of modern life and it is widely utilized in every aspect of it in order to provide service to the mankind. Electrical heaters are utilized for heating processes, electric lamps are utilized for illumination, and electrical machinery are utilized to provide motion. Electric motors are widely employed in domestic and industrial applications in order to provide torque so that the acceleration, speed, and/or position of motion involving processes are controlled and work is done. Home appliances such as washing machines, refrigerators, mixer, etc. all employ electric motors. Industrial applications of electric motors involve a wider range of variety; fans, pumps, extruders, lifts, hoists, cranes, robot manipulators, rolling mills, etc. all employ specific type of electric motors to meet the efficiency, accuracy, reliability criteria set forth for the application. Thus, electric motors are the prime movers of the industry.

Electric motors consume nearly 65% of the electrical energy utilized by the industry [1]. In the past, direct current (DC) motors were used to obtain torque and control motion in most industrial processes. The speed of a DC machine can be easily controlled by means of controlling its armature voltage. This method was invented by Ward Leonard and depending on the technological progress it has been implemented by manual voltage control methods in the early stages and via power electronics in modern times. However, DC motors need maintenance because of commutators/brushes and this characteristic makes the DC motors problematic in many applications. As a result the utilization of DC motors has experienced a limited

growth in the recent decades while Alternating Current (AC) motors have experienced substantial growth.

Presently, industrial applications use AC motors much more often than DC motors. Especially three phase induction motors are used widely. The wound rotor induction motor was invented by Nicola Tesla more than one century ago, followed by the invention of the squirrel cage induction motor by Dolivo Dobrowolsky. The squirrel cage induction motor is comutator-less and it has low maintenance requirements. It also has higher overload capability than the DC motor. Therefore it is more robust than the DC motor. In addition the induction motor is more economical.

Every industrial application has a specific motion quality requirement. While for most fan and pump applications crude speed regulation is sufficient, in robot manipulators high quality position control is mandatory. Therefore, the torque/speed/position/acceleration requirement of each application is unique. If a squirrel cage induction motor is fed from a fixed frequency, fixed magnitude voltage utility grid (such as 50Hz, 380V), the motor provides a specific fixed torque-speed characteristic. It is impossible to effectively control the motor speed/torque/position without external means. To obtain controllable speed and torque from same induction motor, it has to be driven from a variable voltage variable frequency supply. Adjustable Speed Drives (ASDs) provide this function. ASDs increase the energy efficiency of the motion control processes and improve their motion quality.

Early ASDs employed the constant volts-per-hertz (V/f or flux) operation principle as it was a simple means of speed regulation method (the best achievable at that time). The performance was sufficient for fan and pump type applications requiring only crude speed regulation. The new generation ASDs utilize a wide range of modern control techniques, including the Field Orientation Control (FOC) principle to obtain adjustable speed and torque and provide high motion quality. Modern ASD systems employ modern digital signal processors and/or microprocessors to meet the torque and speed regulation requirements over a wide operating range with high accuracy. In order to provide controllable voltage at controllable frequency, modern

ASD systems utilize power electronic converters involving modern power semiconductor devices such as Insulated Gate Bipolar Transistors (IGBTs).

1.2 Voltage Source Inverters

A modern power electronic converter utilized in ASDs involves two stages. The first stage is the AC to DC conversion stage that obtains DC voltage from the AC utility grid. This stage is called a rectifier and is usually formed by diodes connected in bridge form (thus called full bridge diode rectifier). The second stage involves DC to AC conversion and such a device is called an inverter. In an ASD, this converter is utilized to obtain variable voltage and frequency at the output of the ASD so that the motor speed, torque, etc. can be controlled with high performance. The basic block diagram of a modern ASD system is shown in Figure 1.1.

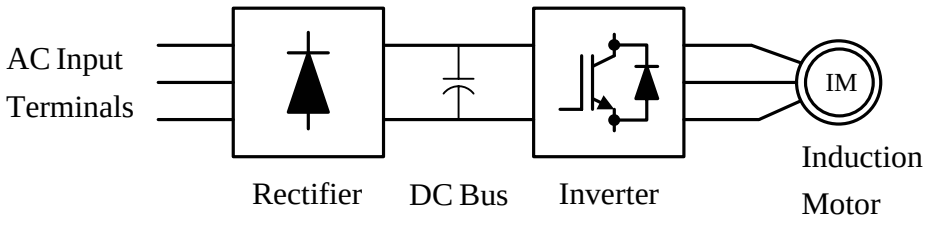


Figure 1.1 Basic block diagram of a modern ASD system.

In Figure 1.1, the rectifier block represents a three-phase, full-bridge diode rectifier. The three-phase, full-bridge diode rectifier is a line commutated converter, which converts AC voltage to DC voltage. Diodes are switched naturally at the utility grid fundamental frequency. The DC output voltage of rectifier should be as ripple free as possible. A large capacitor or capacitor banks are connected to output of the rectifier to obtain ripple free DC voltage.

Modern ASDs utilize the Voltage Source Inverter (VSI) power converter topologies for converting the DC voltage to variable voltage and frequency AC voltage output. Of the VSI topologies, shown in Figure 1.2, the three-phase two-level VSI is the

most widely employed inverter topology. It is utilized in ASDs as DC/AC converter with variable voltage variable frequency output. It is employed in regenerative applications as AC/DC converter (opposite of inverter mode implying regeneration) with variable voltage fixed frequency. In Uninterruptible Power Supply (UPS) applications it is utilized in both the AC/DC and DC/AC conversion stages.

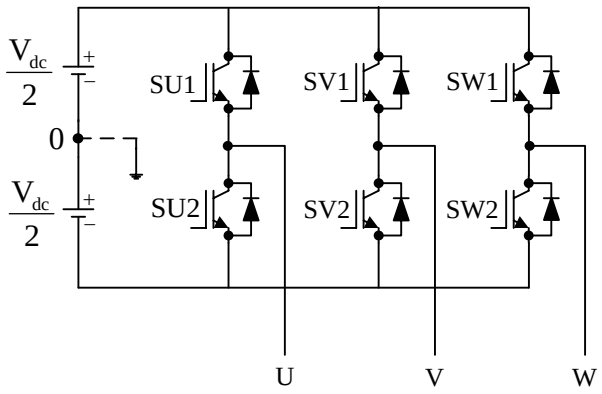


Figure 1.2 The three-phase, two-level voltage source inverter circuit topology.

As the simplest topology for converting DC voltage to three phase AC voltage, the two-level inverter topology consists of six controllable semiconductor switching devices and their freewheeling diodes. The phase output voltage waveform of the inverter takes the values of $-V_{dc}/2$ or $+V_{dc}/2$ with respect to midpoint of the voltage source (0), that is "the inverter has two levels of output voltage." Hence, "two-level inverter." The line to line output voltage waveform in this case, consists of three voltage levels. These are $-V_{dc}$, 0, and $+V_{dc}$ respectively. The modulation and control methods of this inverter topology are simple and the implementation is economical. As a result, the two-level inverter is the most commonly used topology. However, at high voltage levels (400 V line-to-line or higher), the two level inverter topology has a major disadvantage; the output voltage of this inverter has a high dv/dt ratio during the switching transients. The IGBT switches are turned on and off with a high rise and fall rate (turn-on and turn-off time) in order to reduce the switching losses. When the voltage level change is significant the combination of steep voltage change and a large step due to the inverter structure, a very high rate dv/dt results (in 400 V line input applications, 500 V DC bus, two-level inverter, and 100 ns rise/fall time for

IGBTs result in 5 kV/μs). This high ratio creates problems especially in long cable drive applications. These problems are stator winding insulation breakdown due to voltage reflection, corrosion on motor bearings because of discharge currents, EMI emitted to the environment (can cause nuisance trip of the same drive, or interfere with communication equipment or other type electronic devices) [2]. As a result, the two-level inverter topology becomes unsatisfactory in high power and high voltage drive applications.

1.3 The Three-Level Neutral Point Clamped Inverter

Variations and alternatives of the two-level VSI topology have been under development for more than a quarter of a century. One general approach that has been under investigation is the multi-levelling approach that increases the number of output voltage levels and decreases the step voltage magnitude change in order to obtain lower dv/dt rating output voltages. The first practical multi-level inverter topology, the Neutral Point Clamped (NPC) voltage source inverter was invented by Nabae, et al, in 1980 [3]. In Figure 1.3 three-phase three-level NPC-VSI circuit topology is shown.

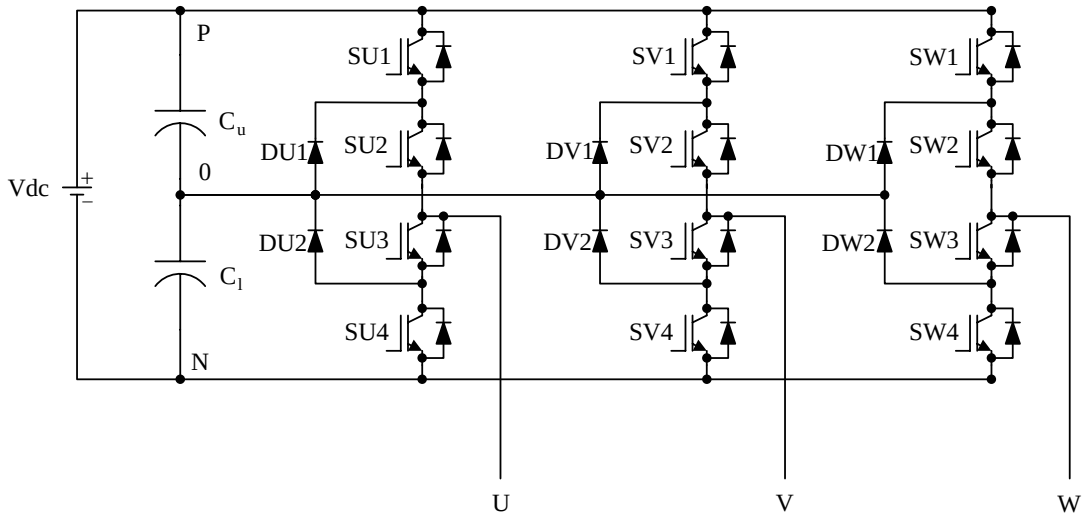


Figure 1.3 The three-phase three-level NPC-VSI circuit topology.

The NPC inverter topology consists of twelve semiconductor switching devices with their freewheeling diodes and six neutral point clamping diodes. The neutral point of this circuit topology is marked as “0” in Figure 1.3. The line to neutral point output voltage waveform of this inverter may have one of the three different voltage levels $-V_{dc}/2$, 0 , and $+V_{dc}/2$ respectively. The line to line output voltage waveform of NPC inverter consists of five voltage levels, $-V_{dc}$, $-V_{dc}/2$, 0, $+V_{dc}/2$, and + V_{dc}. The Pulse Width Modulation (PWM) and control of this topology is complex compared to the two-level inverter topology.

The three-level NPC inverter has several important advantages over the two-level inverter. The blocking voltage across the semiconductor switches is half of the DC bus voltage. This implies that for the same semiconductor voltage ratings, it is possible to reach twice an inverter power rating as the two-level inverter. In PWM mode operation, the voltage harmonics start at about twice the switching frequency and their magnitude is about half of that in the two-level inverter so that the PWM ripple current and acoustic noise is significantly reduced compared to the two-level inverter. Most importantly, dv/dt is half of that in the two-level inverter. This low dv/dt results in superior performance in the long cable ASD applications, reducing the filtering, protection, maintenance requirements, and extending the life of the drive system.

However, the NPC inverter topology has several disadvantages that limit its applications to a narrower range than the two-level VSI. One disadvantage involves the number of switches it has. In low cost applications where component count sensitivity is significant, the additional six transistors and six fast recovery clamp diodes (with high blocking voltage ratings) make the method economically impractical. The modulation and control of the NPC-VSI topology is more complex than the two-level inverter topology and requires more sophisticated digital hardware. Of all, the most important problem is the neutral point potential variation. As the neutral point of the DC bus capacitors is accessed by the inverter, depending on the switching states and the currents in the phases, charge is drawn from or injected to the neutral point leading to neutral point potential variation. The neutral

point potential variation may be a continuous drift or a fluctuation. Depending on the magnitude of deviation from zero voltage level, significant problems such as semiconductor device (IGBT or diode) overvoltage failure, output voltage distortion, DC bus capacitor failure due to thermal overloading can result. Therefore, the neutral point potential must be closely monitored and controlled such that the failure is avoided and this adds to the ASD cost. As a result, the NPC inverter has only found applications in very high power (megawatts and above) and high voltage rating (400 V and above) applications. However, at power ratings below a megawatt, the topology is mostly prohibitive in terms of cost and complexity.

1.4. Scope of The Thesis

In this thesis, the neutral point potential variation of the three-level NPC inverter is analyzed and a novel control algorithm is proposed to confine the neutral point potential variation to a very small band. A two-parameter modulation algorithm is proposed that provides superior neutral point potential control performance even with a small DC link capacitance value.

Although the literature in the area of NPC inverter modulation and neutral point potential control is rich [4]-[8], the published methods do not provide neutral point potential error minimization in one algorithm over the complete modulation region. This work provides a complete solution to the neutral point potential variation problem over the full modulation range (the full inverter hexagon in the voltage vector space). The two-parameter modulation method and neutral point potential control technique based approach is a generalized form of the classical Nearest Triangle Vector PWM (NTV-PWM) method employed in the commercial NPC inverters. However, with the additional control parameter, the proposed method can provide better performance, in particular in the high modulation region. As a result smaller filter capacitors can be utilized. Smaller capacitors imply lower cost and smaller size. Thus, this approach leads to further integration and miniaturization in power electronics.

The organization of this thesis is as follows. In the second chapter, multi-level inverter topologies are reviewed and as the specific case of multilevel inverters and the main topic of this thesis, the three-level NPC inverter topology is discussed in detail.

In the third chapter, the popular modulation techniques utilized in the three-level NPC inverter are reviewed and the influence of these modulation techniques on the neutral point potential is investigated. A new modulation technique, the two-parameter modulation method is proposed to control the neutral point potential. Its behavior is analyzed via analytical methods and its superior performance is shown.

The fourth chapter shows the detailed three-phase R-L load and motor drive simulation results of the three-level NPC inverter drive. A constant volts-per-hertz (constant V/f) fed R-L load and again constant volts-per-hertz controlled motor drive system that feeds a fan load are simulated. The simulations compare the neutral point potential performance of the standard NTV-PWM method and the proposed modulation technique.

In the fifth chapter, the experimental system is described and experimental results are reported. Comparison between computer simulations and experimental results is provided in this chapter.

The sixth chapter summarizes research results and recommends further investigations on subjects related to this thesis.

CHAPTER 2

MULTILEVEL INVERTERS

2.1 Introduction

Multilevel inverters have been developed over the last three decades for the purpose of meeting the drive high voltage rating and low dv/dt value requirements that could not be met by the classical two-level inverter. Until recently, power transistors were slow, and their long turn-on and off times resulted in excessive switching losses that constrained the switching frequency to several kHz values. Also the voltage blocking capability of power transistors was below a kilovolt that implied such switches could not be utilized in two-level inverters at high voltage levels and could not be operated at switching frequencies in the tens of kilohertz range. In the early 1980's utilizing darlington power transistors and Gate Turn Off Thyristors (GTOs), the three-level NPC inverter could provide effectively quadrupled switching frequency and could provide high inverter voltage ratings (twice that of the two-level inverter). As a result, power and voltage levels above that of two-level inverter could be reached and the three-level NPC inverter has found immediate application in traction drives and industrial drives.

In the 1990's, the IGBT was introduced as a fast turn-on fast turn-off device that provided significant switching loss reduction and also the secondary breakdown of the Bipolar Junction Transistor (BJT) was absent. As a result, IGBTs with higher switching frequencies and blocking voltages have extended the two-level inverter ratings to the kilovolt level and some of the three-level NPC inverter applications could be replaced with the two-level inverter. However, in particular in the 400 V and above voltage levels, the two-level inverter turned out to be problematic in terms of the dv/dt stresses during the fast switching of IGBTs. As a

result, the NPC inverter has been favored again due to its reduced dv/dt rating compared to the two-level inverter. As a result at 400 V and above, when fast IGBTs are utilized it is presently favorable to utilize the three-level NPC inverter.

At the present time, as the power converter rating increases above a megawatt, which also implies a voltage rating above 400 V, the practical power converter topology is a multilevel inverter topology. In the lower megawatt range the three-level NPC inverter and at the higher range the cascaded H-bridge topology have been in use in industry for longer than a decade. Utility power electronics applications such as Static Compensator (STATCOM), Unified Power Flow Controller (UPFC), and Flexible AC Transmission System (FACTS) applications involve higher level inverters such as four, five or higher level NPC inverters and recently the flying capacitor topology has also been considered. In the utility power electronics applications, multilevel inverters are required because the voltage levels involved are very high (kV range) and the required level can only be reached by either series connection of large number of power semiconductor or by means of multilevel inverter topologies involving large number of levels. At the 400 V distribution system level, generally the three-level inverter topology suffices.

In general, multilevel inverter topologies synthesize variable frequency variable voltage that is nearly sinusoidal output waveform with low dv/dt, reduced common mode voltage, and low harmonics yielding a motor friendly performance. Although the topology types are various, in all multilevel inverter topologies the basic idea is to utilize low voltage rating power transistors in series connection along with multistage DC capacitor voltage levels such that higher output voltage levels with small incremental steps could be obtained. With high voltage waveform quality, the multilevel inverters result in negligible bearing current and decrease the effect of winding insulation breakdown in motor drives. Due to the reduced stresses and EMI, they provide better interface between DC voltage sources/loads and the AC utility grid when operated as PWM rectifiers and power conditioners.

In multilevel inverters, to increase the number of output voltage levels, the number of semiconductor devices and capacitor voltage sources should be increased. As a result, the power and control circuit of the multilevel inverter becomes more complex, large and costly. In addition, significant voltage imbalance problems arise. Therefore, with the three-level inverter being the most common, mainly up to five-level inverters have been reported. The topology option is more constrained than the number of levels. As illustrated in Figure 2.1, multilevel inverter technology involves three different topological structures.

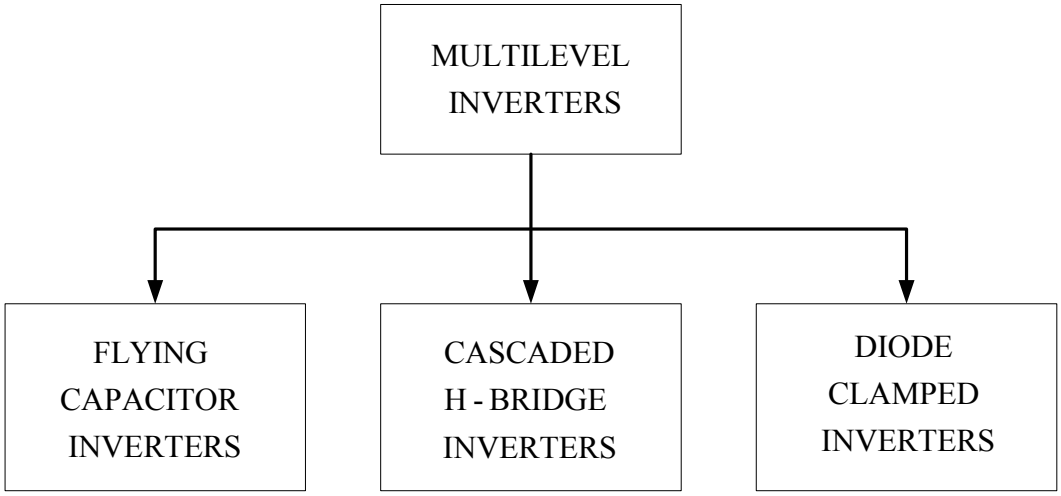
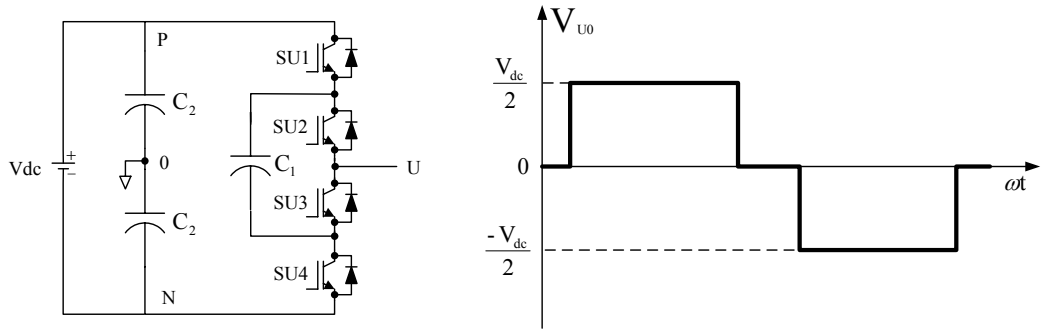


Figure 2.1 Multilevel inverter topologies.

2.2 Flying Capacitor Multilevel Inverter Topology

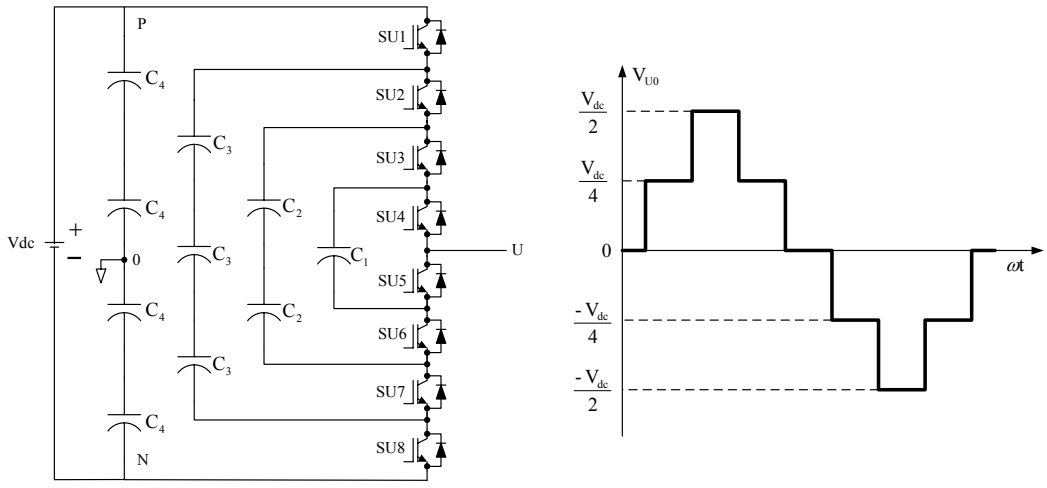
The flying capacitor multilevel inverter topology was proposed in 1992 [9]. The flying capacitor topology is also called as "capacitor clamped multilevel inverter." Figure 2.2.a shows one phase leg of the three-level version of this topology and Figure 2.2.b shows corresponding output voltage waveform when switching at the fundamental frequency. The five-level flying capacitor inverter circuit topology and its output voltage waveform are shown in Figure 2.3.a and Figure 2.3.b, respectively. With all capacitor voltages being equal, in the three-level flying capacitor inverter, the output voltage V_{U0} has three different voltage levels $-V_{dc}/2$, 0, and $+V_{dc}/2$. For the voltage level $+V_{dc}/2$ the semiconductor switches SU1 and

SU2 have to be turned ON. For the 0 level, semiconductor switches SU1 and SU3 or SU2 and SU4 need to be turned ON. For $-V_{dc}/2$, semiconductor switches SU3 and SU4 need to be turned ON. For the five-level case the same strategy can be used to obtain five-level output voltage waveform.



(a) (b)

Figure 2.2 Three-level flying capacitor inverter phase leg structure (a) and output voltage waveform (b).



(a) (b)

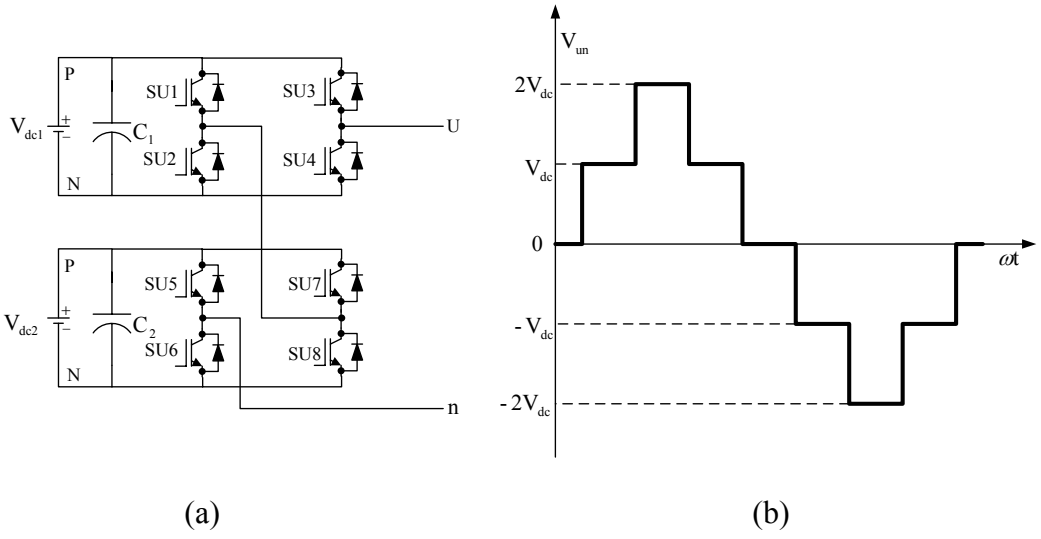
Figure 2.3 Five-level flying capacitor inverter phase leg structure (a) and output voltage waveform (b).

The capacitor charge control method of the flying capacitor inverter topology is complex and the required control algorithm to maintain capacitor voltages within

a specified range is involved. The flying capacitor topology requires larger capacitors (the flying capacitors) than the diode-clamped multilevel inverter DC bus capacitors. Therefore, the flying capacitor topology is not feasible for ASD systems and has mainly been considered for utility power electronics applications.

2.3 Cascaded H-Bridge Multilevel Inverter Topology

In the cascaded H-bridge inverter topology, single phase H-bridge inverters with isolated (separate) DC sources are connected in series. Each such unit is called a cell. Figure 2.4.a shows one phase of the five-level cascaded H-bridge inverter topology and Figure 2.4.b shows the output voltage waveform. This topology has been utilized in industry for medium voltage motor drive applications [10]. Each single-phase H-bridge inverter generates three voltage levels at the output: $-V_{dc}$, 0, and $+V_{dc}$. This is made possible by connecting the capacitors sequentially to the AC side via semiconductor switches. In the five-level cascaded inverter, two cells per-phase are connected in series as shown in Figure 2.4.a. Of the two cells of a phase, in each cell, the DC bus voltage can be different provided that in each phase the same level cell has the same voltage. Then various voltage step waveforms could be obtained. In the case that the voltage levels of all cells are the same, the analysis and synthesis becomes simple. In this case, depending on the output voltage of each cell, the phase output voltage can be one of the following discrete levels; $-2V_{dc}$, $-V_{dc}$, 0, $+V_{dc}$, $+2V_{dc}$. Hence, five-level inverter.



(a) (b)

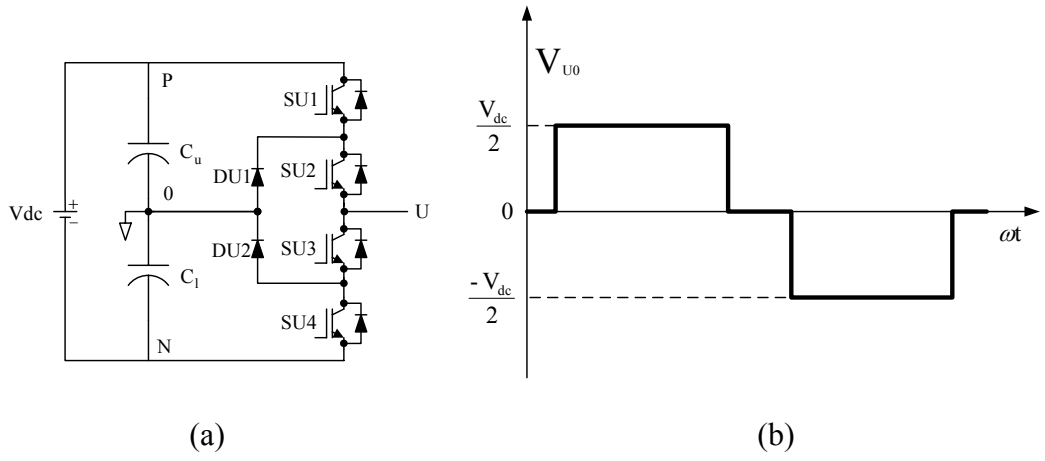
Figure 2.4 The structure of one phase leg of the five-level cascaded multilevel inverter (a) and its output voltage waveform (b).

The cascaded H- bridge multilevel inverter topology has low harmonic content at the motor terminal voltages and low dv/dt rating. By selecting various DC bus voltage levels for various cells and also by selecting a sufficiently large cell count, it is possible to obtain high output voltage waveform quality even at very high voltage and power levels. The cascaded H-bridge inverter topology is fault tolerant. A fault in a single-phase inverter does not necessitate complete shut-down of the ASD system. This structure has modularity, and for this reason maintenance is easy. Isolated DC voltages could be provided via multiwinding transformers and with appropriate rectifier and transformer design the drive AC input current waveform could be made of high quality yielding a utility line friendly performance. However, the cascaded H-bridge inverter topology involves a relatively large number of isolated H-bridge modules, a fairly large and complex input transformer [11], and moreover complex control circuitry. As a result, the topology is utilized in megawatt power rating motor drives. At power ratings below megawatt, the topology is prohibitive in terms of cost and complexity.

2.4 Diode Clamped Multilevel Inverters

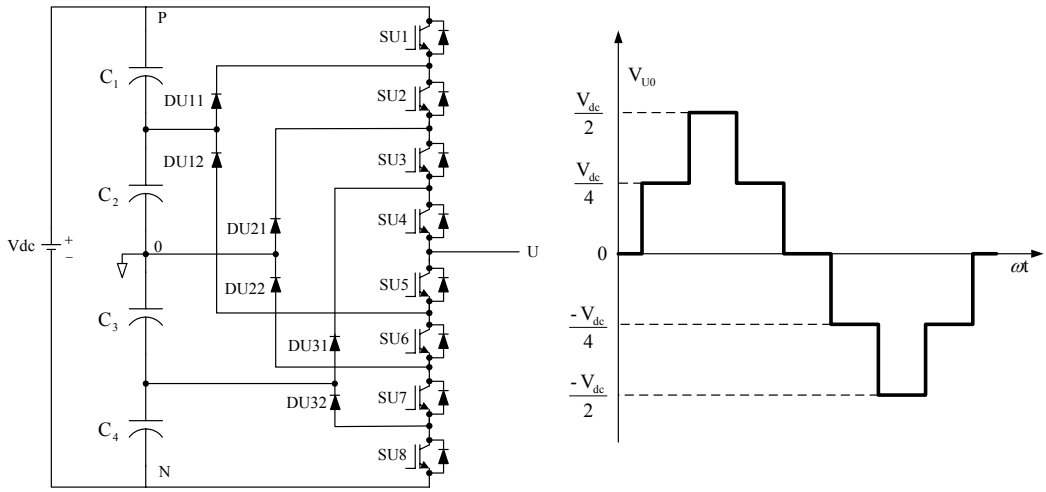
As the first practical multilevel inverter topology, the three-level neutral point clamped (NPC) voltage source inverter was invented by Nabae, et al, in 1980 [3]. Figure 2.5.a shows one phase leg of this topology and Figure 2.5.b shows its output voltage waveform. The NPC inverter is also called as the "Three-Level Diode Clamped" NPC inverter. In the topology, the DC bus voltage must be split in two via series connected capacitor banks. In the three-level inverter, the output voltage V_{U0} has three levels; $-V_{dc}/2$, 0, and $+V_{dc}/2$. For $+V_{dc}/2$ semiconductor switches SU1 and SU2 are turned ON. For 0 output voltage, semiconductor switches SU2 and SU3 are turned ON. And for $-V_{dc}/2$ semiconductor switches SU3 and SU4 are turned ON. The semiconductor switches (SU1, SU3) and (SU2, SU4) are turned ON and OFF in complementary logic. The clamping diodes DU1 and DU2 clamp the semiconductor switch voltage to half of the DC bus voltage.

Figure 2.6.a shows the five-level diode clamped inverter structure and Figure 2.6.b shows its output voltage waveform in Figure 2.6.b. There are four DC bus capacitors that split the DC bus voltage and the voltage across the each capacitor is $V_{dc}/4$. Six clamping diodes are used in this circuit topology. In Figure 2.6.a clamping diodes DU11 and DU32 need to block $V_{dc}/4$, DU12 and DU31 need to block $3V_{dc}/4$, DU21 and DU22 need to block $V_{dc}/2$. The output voltage V_{U0} has five levels $-V_{dc}/2$, $-V_{dc}/4$, 0, $+V_{dc}/4$ and $+V_{dc}/2$. For the voltage level $-V_{dc}/2$, the semiconductor switches SU5 through SU8 are turned ON; for level $-V_{dc}/4$ semiconductor switches SU4-7 are turned ON; for 0 level semiconductor switches SU3-6 are turned ON. For voltage level $+V_{dc}/4$ semiconductor switches SU2-5 are turned ON. For voltage level $+V_{dc}/2$ semiconductor switches SU1-4 are turned ON.



(a) (b)

Figure 2.5 The three-level diode clamped inverter phase leg structure (a) and output voltage waveform (b).



(a) (b)

Figure 2.6 The five-level diode clamped inverter phase leg structure (a) and output voltage waveform (b).

When used as three-phase inverter, the NPC inverter phase output voltage levels and the line-to-line output voltage levels are related with the 2n-1 relation. The number of voltage levels of the line to line output voltage waveform is 2n-1, where n is the number of the phase voltage output levels. Therefore, for the three-

level NPC inverter case line-to-line output voltage consists of five different voltage levels.

The three-level NPC inverter structure was originally developed for the purpose of increasing the power ratings of power converters (to megawatt levels) without paralleling or in series connecting converter modules or semiconductor devices. Since its invention the NPC inverter has found place in significant number of applications involving high voltage and/or power ratings. Although the early applications involved niche areas such as railway drives, presently the utilization has spread to the general purpose ASD area.

The three-level diode clamped inverter (NPC) inverter has been utilized in 400 V and above voltage ratings in the power range from a few kilowatts to megawatt. This wide range places the three-level NPC inverter in a special place among all the multilevel inverter topologies. Similar to the flying capacitor topology, the three-level NPC inverter topology also has the drawback of capacitor voltage variation. In the three-level NPC inverter the neutral point (connection point of the two DC bus capacitors) potential may drift or vary and countermeasures must be taken when employing this topology.

2.5 Multilevel Inverter Modulation Methods

Multilevel inverter modulation methods can be classified according to switching frequency as shown in Figure 2.7. Fundamental frequency switching methods perform one or two commutations of the semiconductor switches during one cycle of output voltages [12]. Twelve-step mode modulation method and selective harmonic elimination method are low frequency modulation methods.

PWM frequency switching methods are widely employed in multilevel inverters. Based on the implementation technique, two main PWM methods are utilized in multilevel inverters. The first method is the “Scalar PWM” method and the second method is the “Space Vector PWM” method.

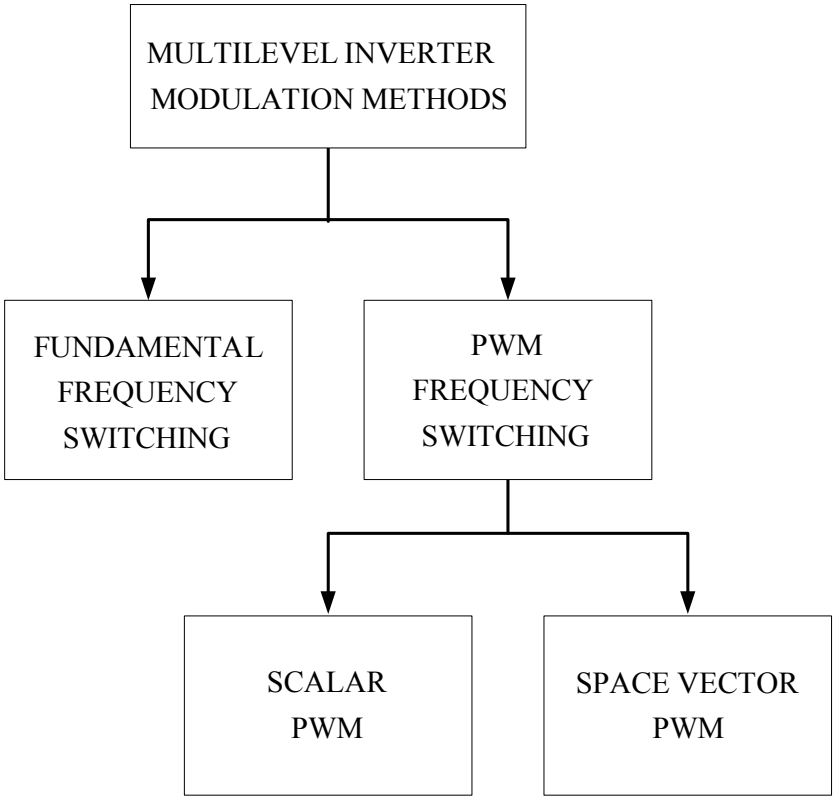


Figure 2.7 Classification of multilevel inverter modulation methods.

2.5.1 The Scalar PWM Method

In multilevel inverters when utilizing the scalar method, multiple carrier waves and multiple modulation (reference) signals are involved. Intersections of the carrier and modulation waves define the switching instants of the associated switches. According to the desired number of levels on the output voltage waveform, the number of carrier waves and modulation signals change. As an example; for a three-level inverter two carrier waves and one modulation signal, or two modulation signals and one carrier wave is utilized. For a five-level inverter, four carrier waves and one modulation signal are used.

In the multicarrier wave case, the carrier waves may have equal magnitude, but they are placed with phase shift. Alternatively, they may have the same phase but

they may have different offset values leading to a vertical arrangement of the carrier waves.

In either case, the modulation waves are compared with the triangular carrier waves and at the intersection points the switching decisions are made for the associated switches.

In an n-level cascaded H-bridge inverter topology, when the carrier wave phase shifting method is utilizied, the carrier waves are phase shifted by the angle of $360^{\circ}/n$ with respect to each other and the effective switching frequency is equal to n times the carrier frequency. For the five-level cascaded H-bridge inverter, the carrier waves are phase shifted by $360^{\circ}/5=72^{\circ}$. Minimum distortion is observed on the output voltage waveform by using 72° phase shift. This modulation technique is illustrated in Figure 2.8. In the vertically placed carrier wave approach, five carrier waves are placed on top of each other as shown in Figure 2.9. Intersections of the carrier waves with the modulation wave define the switching instants of the associated switches.

In all the discussed scalar modulation methods, in order to increase the output voltage, a third harmonic voltage (or its multiples) may be added to the each modulation wave. In this manner, the modulation waves are flattened and saturation of the modulation waves is delayed to a higher modulation index. Since triplen harmonic voltages do not result in a current in three-wire three-phase system, extending the voltage linearity by this approach comes at no cost [13].

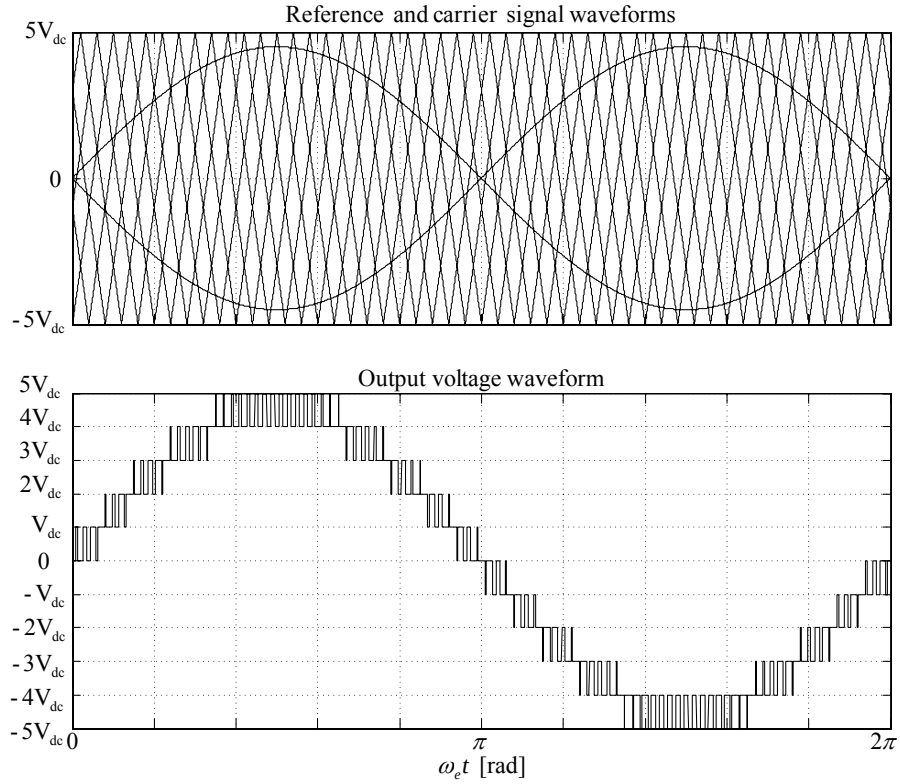


Figure 2.8 Illustration of shifted multicarrier scalar PWM method.

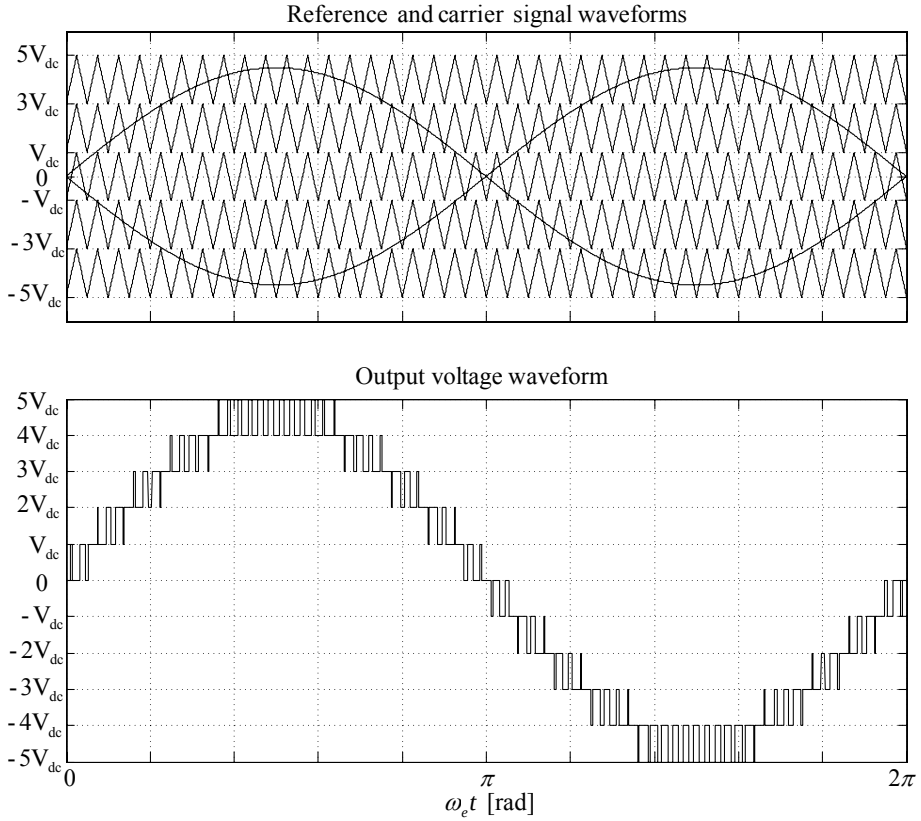


Figure 2.9 Illustration of added multicarrier scalar PWM method.

2.5.2 The Space Vector PWM Method

The space vector modulation technique which transforms the three-phase inverter output voltages to complex variables in the complex plane and allows for advanced modulation and control methods to be implemented has been widely utilized in two-level inverters. The approach has been extended to multilevel inverters and widely applied. The space vector representations of the classical two-level and three-level NPC inverter output voltages are shown in Figure 2.10.a and Figure 2.10.b, respectively.

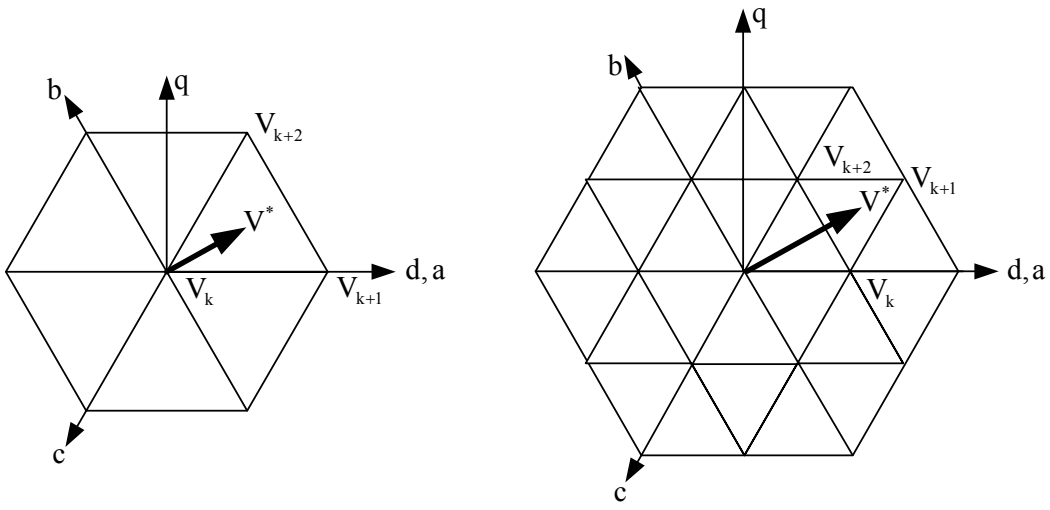


Figure 2.10 Space vector representation of the two-level inverter output voltages (a) and the three-level NPC inverter output voltages (b).

The space vector representation of three-level inverter is valid for the three-phase diode-clamped, flying capacitor, and cascaded H-bridge inverters. In the space vector modulation theory, the reference voltage vector is synthesized by three adjacent voltage vectors. The duty cycles of adjacent voltage vectors are calculated by using the following complex variable volt-second balance equation.

$$V^*T_s = T_kV_k + T_{k+1}V_{k+1} + T_{k+2}V_{k+2} \quad (2.1)$$

Where V^* is the reference voltage vector, T_s is the switching period, V_j , V_{j+1} , and V_{j+2} are the three voltage vectors adjacent to the reference voltage vector tip point, and T_j , T_{j+1} , and T_{j+2} are time lengths of the three adjacent voltage vectors, respectively. For higher number of inverter levels the space vector diagram of the inverter output voltage becomes more complex and selection of the switching states may be a laborious task.

Generally, space vector PWM methods utilize the DC bus voltage of the inverter better than scalar PWM methods. Also the output voltage waveform of space vector PWM methods is superior to scalar PWM methods such as sinusoidal PWM. Space vector PWM methods can be implemented by using digital signal processors and/or additional digital hardware. Further details on the space vector PWM approach will be provided in the next chapter.

2.6 Applications of Multilevel Inverters

Ever since its conception, the flying capacitor topology has been considered for utility power electronic applications such as STATCOM and FACTS where reactive power control is the main issue. In this case all the flying capacitors are charged or discharged by power exchange through the AC output terminals of the inverter. Unlike the conventional inverters, there is no DC bus and therefore there is no associated rectifier circuitry. To the knowledge of the author, there has been no commercial use or practical application of the flying capacitor multilevel inverter until the present time.

The cascaded H-bridge inverter topology has been employed in medium voltage high power motor drive applications. In this application scalar modulation methods such as sinusoidal PWM have been in use. In Figure 2.11, a seven-level cascaded H-bridge inverter drive system is shown. The eleven-level version of this inverter topology output voltage waveform has low Total Harmonic Distortion (THD) value that is less than 10% and with the motor load being inductive, the output current waveform becomes nearly sinusoidal. In such high

power drives, the drive input power quality is also of significant concern. With phase multiplying transformer structures that involve several rectifiers and a transformer with several windings, the AC line input current waveform can be made nearly sinusoidal. In commercial products input current THD less than 1% has been reported [9]. In the inverter drive, selection of the level number is determined by the output voltage value. For a 2.3 kV output voltage, three cascaded H-bridge inverters and for 3.3 kV output voltage, four cascaded H-bridge inverters have been utilized [14].

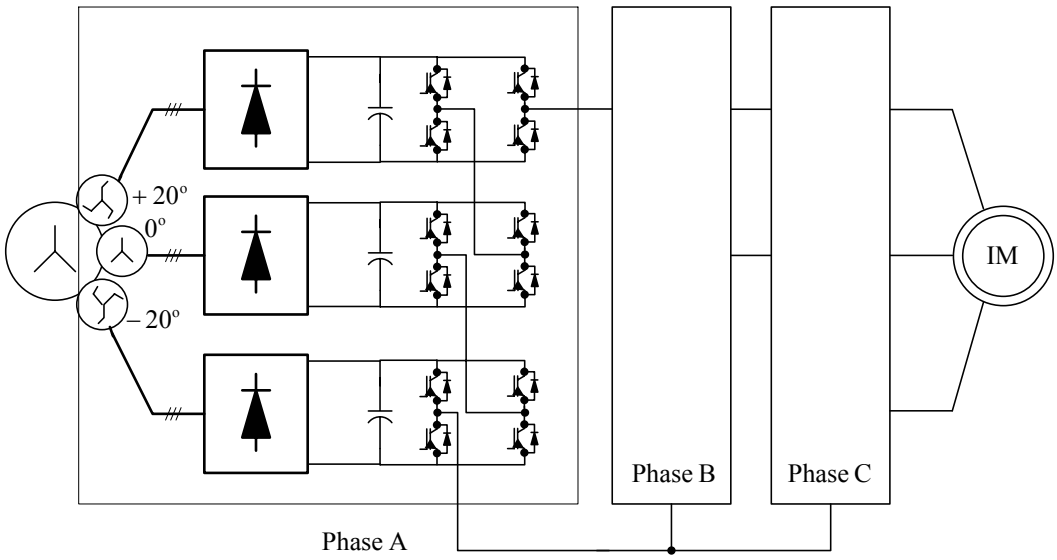


Figure 2.11 The seven-level cascaded H-bridge inverter drive system.

Although the cascaded H-bridge multilevel inverters have found use over the last decade, the utilization typically has been constrained to multi-megawatt power levels. On the other hand, NPC inverters have found broader use in industry. In particular the three-level NPC inverter has been utilized in a wide power and voltage range. Figure 2.12 shows the circuit diagram of a commercial three-level NPC inverter drive. Such drives have been in use in voltage levels above 400 V (2.3 kV up to 6 kV) and the power rating is typically in the megawatts range. Fans, pumps, blowers, compressors, and conveyors have been typical application fields of such drives. In these drives the application mostly involves non-

regenerative operating modes and therefore at the input diode rectifiers suffice. However, due to the input power quality requirements, instead of six-pulse diode rectifiers, phase multiplication techniques are utilized. As shown in the figure, in one such configuration a 12-pulse input rectifier is utilized and the input current waveform quality significantly improves. As the power rating increases and the power quality requirements become more stringent, higher pulse number rectifiers with phase multiplying transformers (such as 18-pulse, 24-pulse etc. structures) become inevitable. At the 400 V distribution voltage level the three-level NPC inverter topology has also been finding increasing number of applications. Recently, 400 V rating general purpose drives that are based on the three-level NPC topology have been commercialized. The circuit diagram of such a drive is drawn in Figure 2.13. In this case, the front end is a six-pulse diode rectifier (perhaps additional passive filters will be utilized at the front end). As a result, it can be stated that the three-level NPC inverter has been widely accepted in 400 V and above applications in a wide power range and its applications have been tremendously increasing over the last decade. However, the NPC inverter technology is not fully matured and several technical problems with the three-level NPC inverter topology need to be cured.

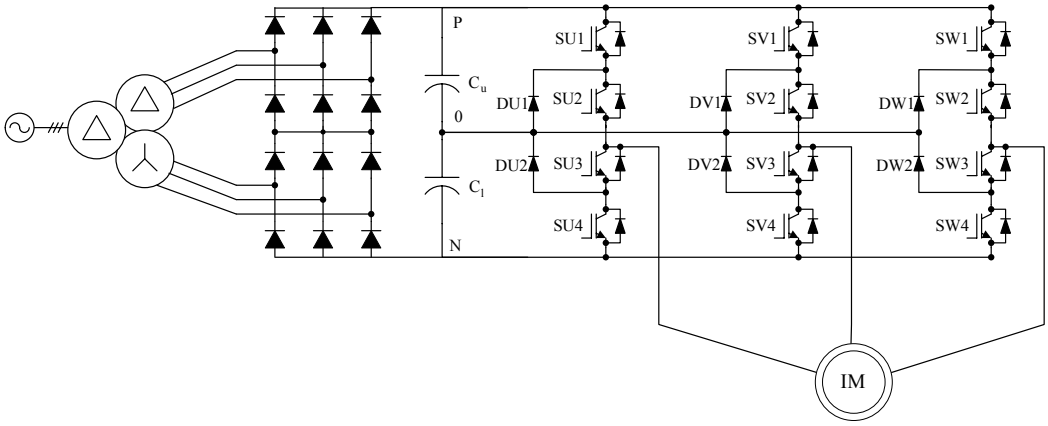


Figure 2.12 A three-level NPC inverter drive with 12-pulse input rectifier.

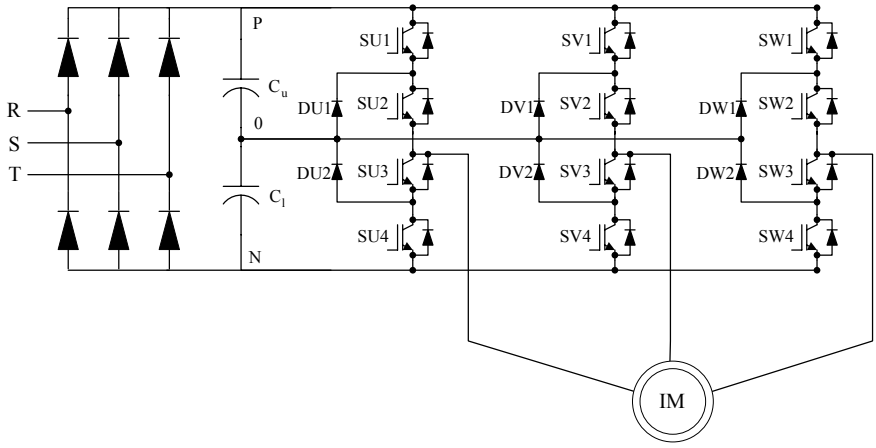


Figure 2.13 A commercial three-level NPC inverter drive with three-phase full-bridge diode rectifier.

2.7. Performance Issues of The Three-Level NPC Inverter

In the three-level NPC inverter the number of power semiconductor devices and the associated gate drive circuitry is twice that of the classical two-level inverter. Thus, cost reduction, protection, converter efficiency issues must be addressed. In the 400 V distribution voltage and sub-megawatt power range, these difficulties have been overcome with the integrated power module approach where the power electronics of the converter could be shrunk into a small package yielding economical and compact solution. However, the main drawback of the three-level NPC inverter is the variation and/or drift of the neutral point potential. To maintain the neutral point potential within acceptable boundaries, the inverter must be intelligently controlled. The neutral point potential control problem has attracted the attention of many researchers ever since the conception of the inverter topology and various methods have been reported [6], [8], [15], [16]. However, most methods reported have constrained performance range and also involve complex control algorithms. In the following chapter a generalized and compact control algorithm for the neutral point potential control of the three-level NPC inverter will be proposed and its performance illustrated. With the main focus of the thesis being the three-level NPC inverter, and specifically its neutral point potential control, the next chapter will be devoted to the three-level NPC inverter analysis and neutral point potential control.

CHAPTER 3

MODULATION AND NEUTRAL POINT POTENTIAL CONTROL OF THE THREE-LEVEL NPC INVERTER

3.1 Introduction

The three-level NPC inverter circuit topology is complex due to the high number of switches involved. Therefore, its behavior is more complex than the two-level inverter and studying its performance involves more effort. Different from the two-level inverter, the three-level NPC inverter has a neutral point terminal connection (via the clamping diodes) and the neutral point draws current and its potential may drift leading to overvoltage stress and eventually failure of the switches. As a result control of the neutral point potential is mandatory. Controlling the neutral point potential can only be achieved by manipulating the inverter switches. Therefore, in the three-level inverter, neutral point potential control and output voltage programming algorithm must be considered together. As a result, determining the PWM pulse pattern is a difficult task.

This chapter will elaborate on the three-level NPC inverter topology, its PWM methods, develop background on the neutral point potential problem, and provide a modulation technique that overcomes the neutral point potential variation problem. The classical three-level NPC inverter PWM methods will be discussed. The analysis and formulation of the neutral point current is followed by the investigation of the effect of the neutral point current on the neutral point potential. Then the two-parameter PWM method that provides superior performance in terms of neutral point potential control will be introduced and its performance will be investigated.

3.2 The Three-level NPC Inverter Circuit Topology

The three-level NPC inverter consists of twelve gate controlled (turn-on and turn-off controlled) semiconductor switching devices such as IGBTs with their freewheeling diodes and six clamping diodes to provide a connection to the neutral point. Figure 3.1 shows the three-level NPC inverter topology. The neutral point is the mid-point of the DC bus capacitors connected in series. In Figure 3.1, the neutral point is marked as "0". The positive DC bus terminal is presented as "P" and the negative DC bus terminal is presented as "N" in Figure 3.1. The DC bus is represented with a constant voltage source V_{dc} which could be a battery or the diode rectifier output voltage (that actually pulsates at $6\omega_e$ radial frequency and its multiples, where ω_e is the electrical radial frequency of the utility grid voltage). The total DC bus voltage (V_{dc}) variation does not have any effect on the neutral point potential, but may affect the output voltage. If the DC bus voltage variation is accounted for by means of the DC bus voltage disturbance rejection compensation technique [17], the effect of the DC bus voltage variation on the output voltage of the inverter can also be neglected. Therefore, throughout the discussions, the DC bus voltage will be assumed constant for the sake of simplicity.

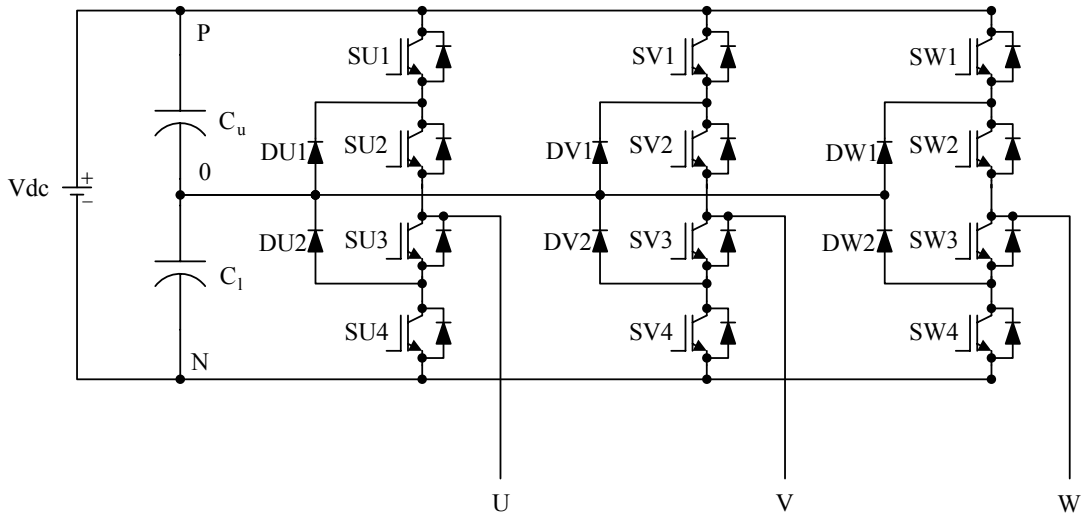
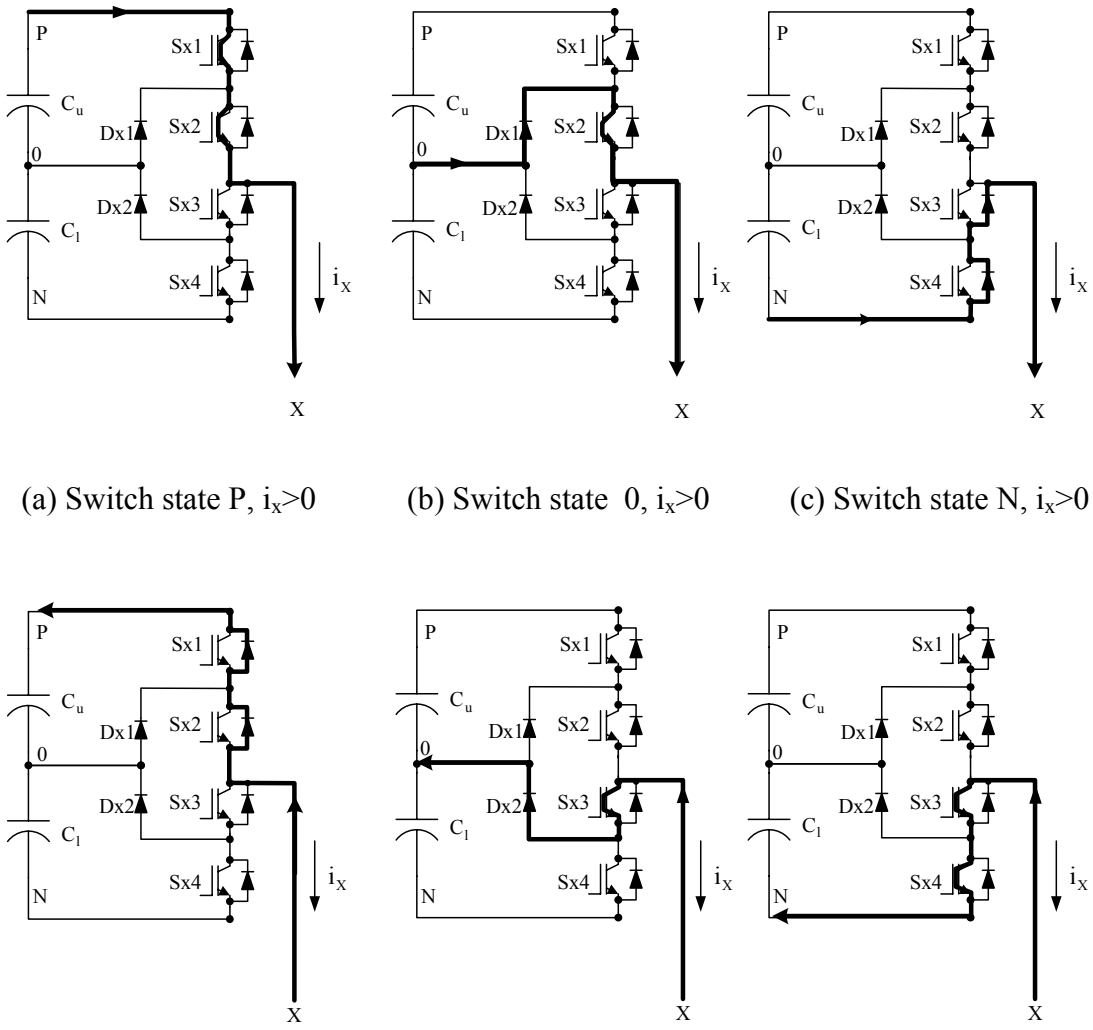


Figure 3.1 The three-level NPC inverter circuit topology.

The connection of a phase output terminal to the positive DC bus terminal is provided by turning the semiconductor switches Sx1 and Sx2 of the associated inverter leg (x: U, V, W) ON. The neutral point connections are made either via Dx1 and Sx2 pair or Dx2 and Sx3 pair according to the phase current polarity. The negative DC bus terminal connection is accomplished by turning the associated semiconductor switches Sx3 and Sx4 ON. Figure 3.2 shows the current paths of the three-level NPC inverter for one phase leg of the inverter. In Figure 3.2.a the phase current is positive (flows to load) and the semiconductor switches Sx1 and Sx2 are turned ON. In that case the load current flows through the semiconductor switches Sx1 and Sx2, and the load terminal is connected to the positive DC bus terminal "P." Figure 3.2.b shows the connection to the neutral point "0" when the phase current is positive. The semiconductor switches Sx2 and Sx3 are turned ON. However, the phase current flows through Sx2 and Dx1. In Figure 3.2.c, the connection to the negative DC bus terminal "N" is shown. In that case the phase current is positive and the semiconductor switches Sx3 and Sx4 are turned ON. The phase current flows through the freewheeling diodes of the semiconductor switches Sx3 and Sx4. The connection to the positive DC bus terminal "P" when the phase current is negative (flowing from the load to the inverter) is shown in Figure 3.2.d. In that case, the semiconductor switches Sx1 and Sx2 are turned ON. However, the phase current flows through their freewheeling diodes. Figure 3.2.e shows connection to the neutral point "0" when the phase current is negative. The semiconductor switches Sx2 and Sx3 are turned ON and current flows on Sx3 and Dx2. In Figure 3.2.f, the connection to the negative DC bus terminal is shown when the phase current is negative. Table 3.1 shows the switching combinations of one inverter leg and the corresponding value of the phase voltage (V_{x0}).



(a) Switch state P, $i_x>0$ (b) Switch state 0, $i_x>0$ (c) Switch state N, $i_x>0$

(d) Switch state P, $i_x<0$ (e) Switch state 0, $i_x<0$ (f) Switch state N, $i_x<0$

Figure 3.2 Current paths of the three-level NPC inverter (x: U,V,W).

Table 3.1 Switching combinations of the three-level NPC inverter

("1" means ON and "0" means OFF)

Switch states	Phase voltage (V_{X0})
Sx1=1 & Sx2=1 (Sx3=0 & Sx4=0)	$+V_{dc}/2$
Sx2=1 & Sx3=1 (Sx1=0 & Sx4=0)	0
Sx3=1 &and Sx4=1 (Sx1=0 and Sx2=0)	$-V_{dc}/2$

In the three-level NPC inverter, semiconductor switches Sx1 and Sx4 are called as the outer switches, and semiconductor switches Sx2 and Sx3 are called the inner switches. The switching rule for the three-level NPC inverter is that; the semiconductor switches Sx1 and Sx3 are turned ON and OFF with complementary logic. The semiconductor switches Sx2 and Sx4 are also turned ON and OFF complementarily.

In the standard approach, the transition from one switch state to another is carefully done to maintain low dv/dt during switching. In the topology, the output voltage is not swung from positive to negative (or from N to P) bus terminals in one step. Instead, the intermediate level of mid-point potential is benefited from. Thus, the switching strategy of the three-level NPC inverter is that; the outer semiconductor switch can only be turned ON, when the associated inner semiconductor switch is conducting. As an example, Sx1 can only be turned ON when the semiconductor switch Sx2 is conducting. The other rule of switching strategy is that; the inner switch can only be turned OFF, when the associated outer switch is turned OFF. As an example, Sx2 can be turned OFF only after the semiconductor switch Sx1 is already in OFF state. If these switching rules are not obeyed, the semiconductor switch can be over stressed by the full DC bus voltage.

The created line to neutral point output voltage waveform of the three-level NPC inverter is shown in Figure 3.3. As seen from Figure 3.3 the line to neutral output voltage waveform of the NPC inverter consists of three different voltage levels. It contains $-V_{dc}/2$, 0V and $+V_{dc}/2$ levels. The output voltage can not change from positive to negative directly. It has to have a zero voltage level between positive and negative voltage levels.

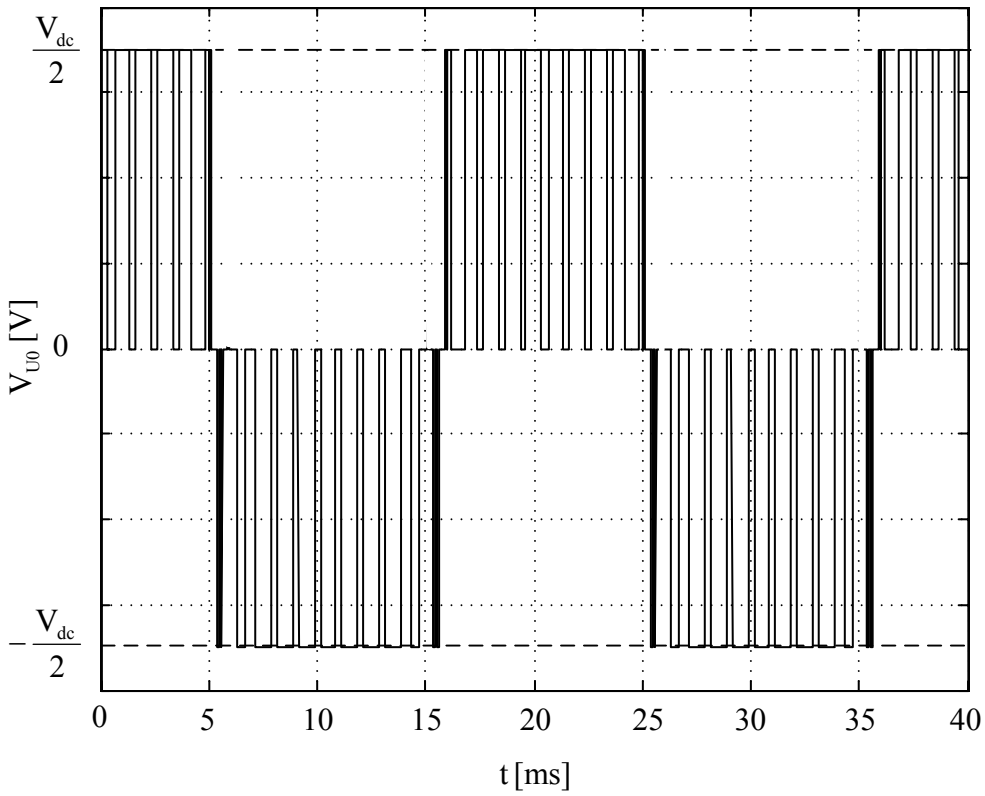


Figure 3.3 Line to neutral point output voltage of the three-level NPC inverter.

The line-to-line output voltage waveform of the three-phase three-level NPC inverter is shown in Figure 3.4. The line-to-line output voltage waveform contains five different voltage levels. These levels are $-V_{dc}$, $-V_{dc}/2$, 0, $+V_{dc}/2$ and $+V_{dc}$. For level $-V_{dc}$ and $+V_{dc}$ one of the phases need to be connected to negative terminal of the DC bus and the other one needs to be connected to the positive terminal of the DC bus. For levels $-V_{dc}/2$ and $+V_{dc}/2$ one phase needs to be connected to the neutral point of the DC bus and the other phase needs to be connected to the negative or the positive terminal of the DC bus. For 0 voltage level, all the phases need to be connected to the same terminal of the DC bus. The obtained waveform consists of five different voltage levels. Therefore, the output voltage waveform and the associated phase current of the load has significantly reduced amount harmonic content compared to the two-level inverter case.

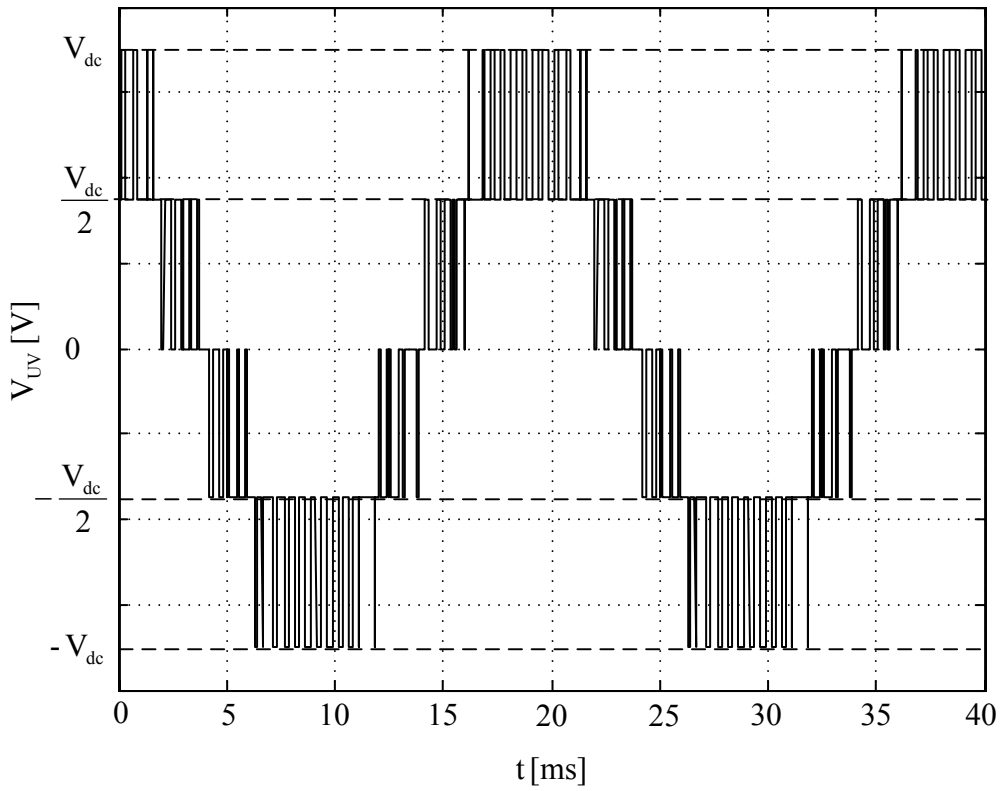


Figure 3.4 Line–to-line output voltage of the three-level NPC inverter.

3.3 Neutral Point Current Analysis of The Three-Level NPC Inverter

In the case of two-level inverter, the DC bus voltage can be formed from the combination of capacitors connected in series or in parallel. In case of series connection, the intermediate levels of the DC bus are never connected to the inverter. Thus, no current is drawn from the intermediate connection points of capacitors. The small unbalance between the series connected capacitors is compensated for via the parallel connected bleeding resistors and with the correct choice of the bleeding resistors in the application there is no midpoint potential drift. In the three-level NPC inverter case, there are two capacitor banks which are connected in series to create the DC bus. The midpoint of the capacitor banks is connected to the inverter over through clamping diodes to create a neutral point connection from the DC bus to the inverter output terminals (to the phases). This point is marked as “0” in Figure 3.1 and named as “the neutral point potential” indicating a zero level potential (ideally). According to the switch states and the phase current polarity, the load

current is drawn from or injected to the capacitors from this point. These cases are shown in Figure 3.2.b and Figure 3.2.e. The phase currents injected to the neutral point via these switch paths can create potential variation (fluctuation) or drift (deviation from zero level). Reasons for the neutral point potential drift can be; dynamic loading conditions, unbalances between the semiconductor switches (due to structural differences or operational differences) and/or unbalanced load. When becoming excessive, the potential drift may cause several problems. The voltage stress on the semiconductor switches may increase and there may be semiconductor switch failure (insulation breakdown). Excessive output voltage waveform distortion may be created and the output performance of the three-level NPC inverter decreases. To avoid neutral point fluctuation or drift, an appropriate control algorithm should be used with the modulation technique employed. The potential drift or fluctuation should typically be kept within 2-3% of the DC bus voltage.

Whether the phase currents inject current to or draw current from the neutral point depends on the phase current polarities and the inverter switch states and their on-duration. In the three-level NPC inverter, there are 27 switch states. Some of the switch states of the three-level NPC inverter load the neutral point (inject to or draw charge from it). Twelve of the switch states, called as “Class-I switch states”, are shown in Figure 3.5.a to Figure 3.5.l. These states charge or discharge the neutral point according to the phase current polarities. As an example, as shown in Figure 3.5.a, in the switch state “P00,” the upper DC bus capacitor is used as voltage source and for the shown current polarities, the load current discharges the upper capacitor and charges the lower capacitor. As a result the neutral point potential drifts up. Switch state “0NN,” as shown in Figure 3.5.b, has the opposite effect on the neutral point potential. It charges the upper capacitor and discharges the lower capacitor. As a result the neutral point potential drifts down. If the current polarities are as shown in Figure 3.5.a-l, the switch states “P00,” “00N,” “0P0,” “N00,” “00P,” and "0N0” discharge the upper capacitor and charge the lower capacitor. The neutral point potential drifts up. Switch states “0NN,” “PP0,” “N0N," “0PP,” “NN0,” and “P0P” discharge the lower capacitor and charge the upper capacitor. Therefore, the neutral point potential drifts down. Switch states “P00” and “0NN” create the same line-to-

line voltages at the motor terminals. In the switch state pairs “00N” and “PP0,” “0P0,” and “N0N,” “N00” and “0PP,” “00P” and “NN0,” “0N0” and “P0P,” each member of the associated pair creates same line-to-line voltages. Therefore, the members of the switch state pairs are redundant in terms of output voltage property (For example 00N and PP0 are redundant and they both create the same output voltage). However, as described above these switch states have opposite effects on the neutral point potential. Therefore, they can be used in an appropriate sequence to keep the neutral point potential at the desired level.

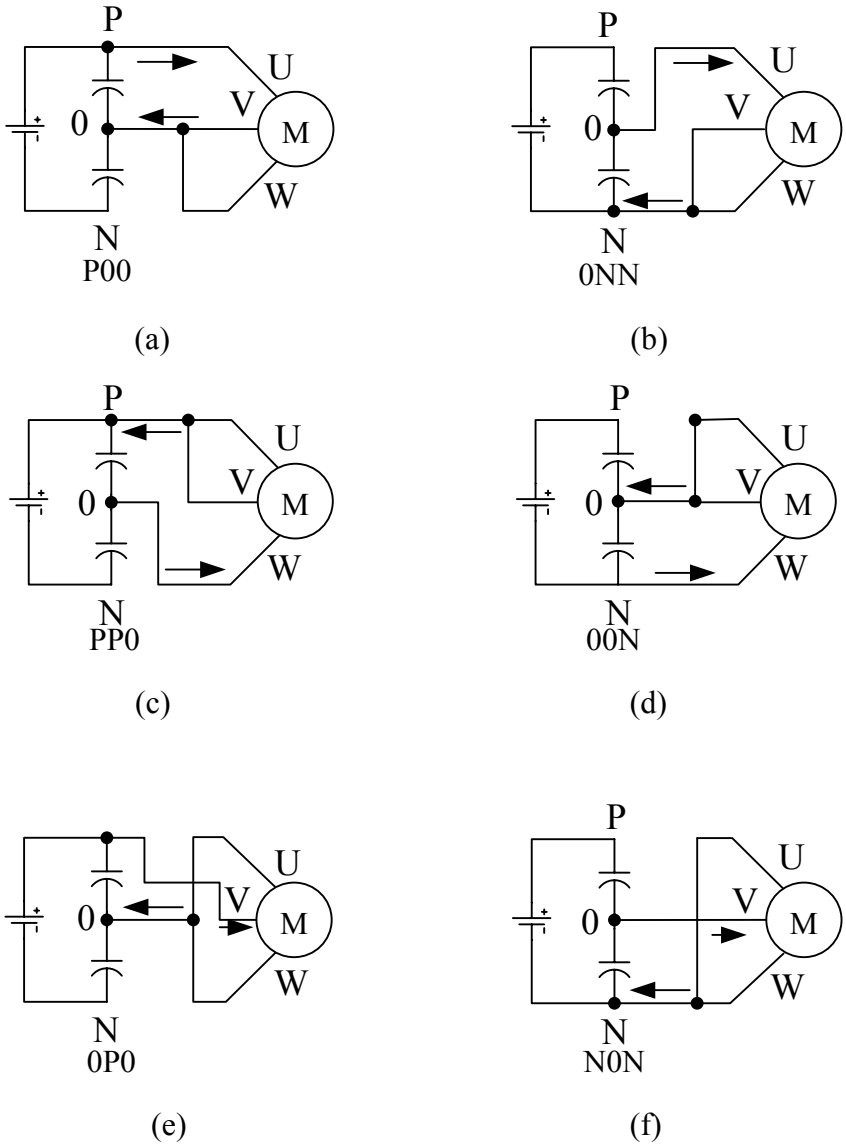


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Figure 3.5 The effect of Class-I switch states on the neutral point potential.

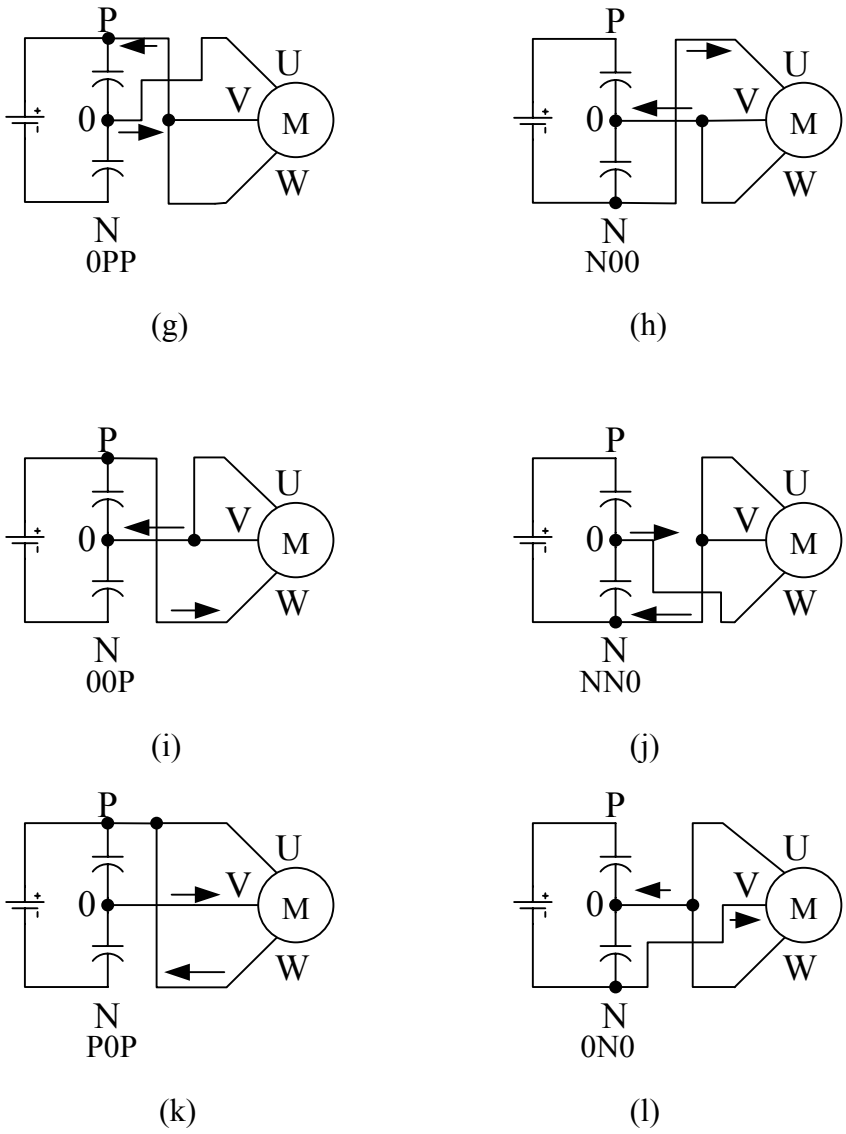

Figure 3.5 The effect of Class-I switch states on the neutral point potential.

Of the remaining 15 switch states, only six states load the neutral point. These states are shown in Figure 3.6.a to Figure 3.6.f and they are called "Class-II switch states." These are "P0N," "0PN," "NP0," "N0P," "0NP," and "PN0". These switch states connect each of the three output terminals of the three-level NPC inverter to three different DC bus terminals. Generally, at steady-state operation with conventional modulators, the phase connected to the neutral point changes every 60˚ (of the 360˚ period) and therefore in each 60^{o} segment different phase current is injected to the neutral point. Thus, a triplen harmonic neutral point current waveform is created. As a result, these switch states inject a triplen harmonic current to the neutral point and

this current creates potential fluctuation on the neutral point at the triple of the output voltage fundamental frequency. The triplen harmonic current and therefore the triplen harmonic voltage on the neutral point potential depends on the load current magnitude, on the power factor of the load and on the modulation index. For lower power factor and higher modulation index values, the magnitude of the triplen harmonic component on the neutral point potential becomes larger.

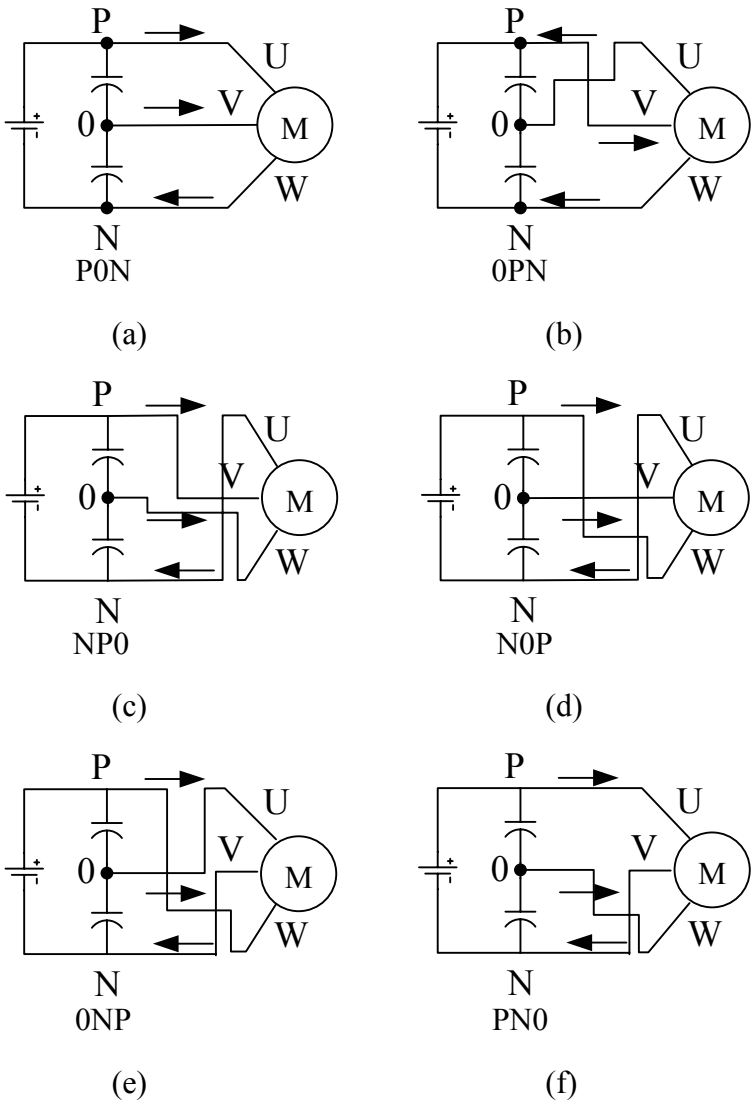

Figure 3.6 The effect of Class-II switch states on the neutral point potential.

As can be seen from Figure 3.7, the remaining switch states do not load the neutral point of the three-level NPC inverter. These switch states are called “Class-III switch

states". Class-III switch states "PNN," "PPN," "NPN," NPP," "NNP," "PNP," "PPP," and "NNN" do not connect any phase to the neutral point terminal of the three-level NPC inverter. Therefore these switch states do not have any effect on the neutral point potential. Switch state "000" connects all phases to the neutral point. However, it does not load the neutral point.

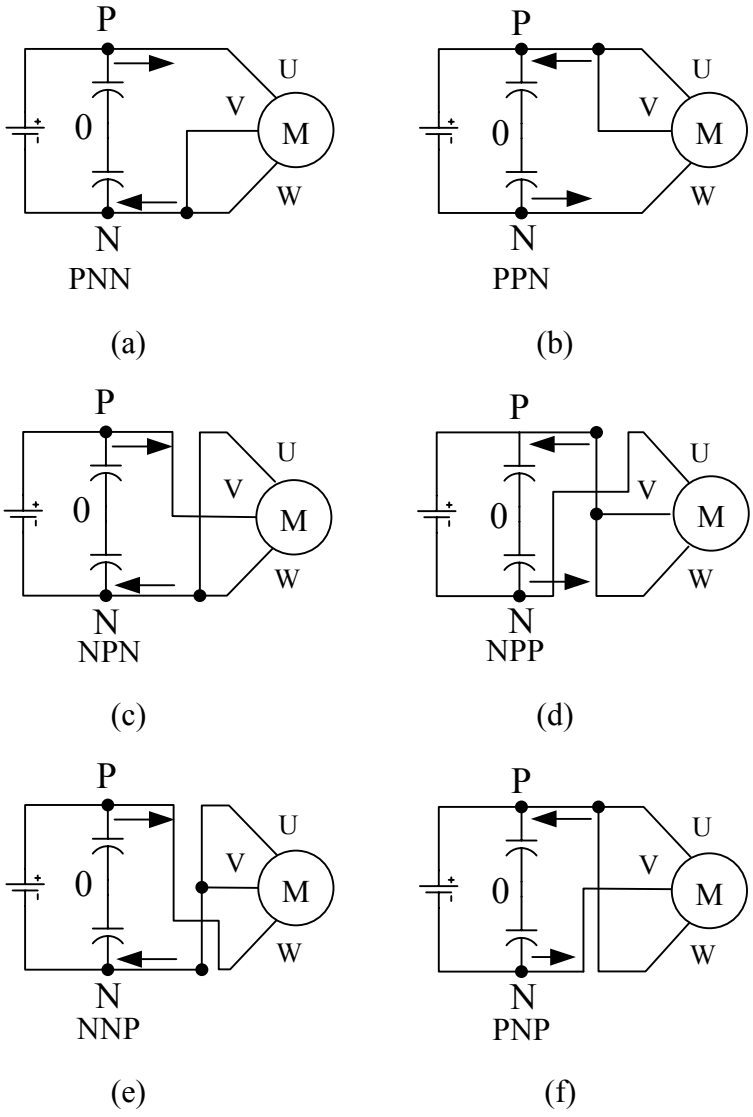

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Figure 3.7 The effect of Class-III switch states on the neutral point potential.

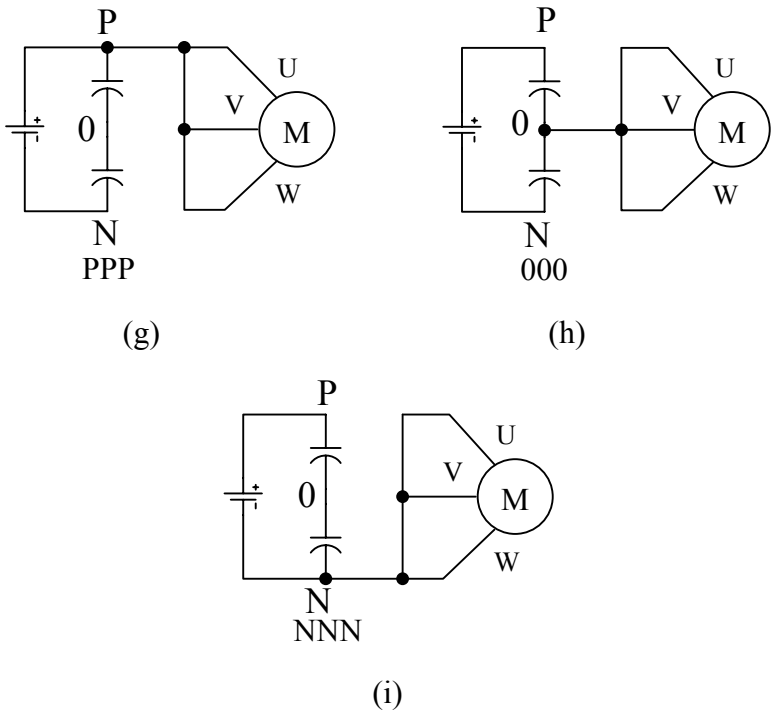


Figure 3.7 The effect of Class-III switch states on the neutral point potential.

As described above, Class-I and Class-II switch states have strong influence on the neutral point potential. This result implies that the neutral point potential of the three-level NPC inverter is directly dependent on the modulation method involved. Therefore, the neutral point current and potential should be analyzed along with modulation methods. In the following, modulation methods of the three-level NPC inverter will be studied and analysis of the neutral point current and potential according to the modulation method will follow.

3.4 Three-Level NPC Inverter Modulation Methods

The modulation methods employed in the three-level NPC inverter can be divided into two groups; scalar PWM and space vector PWM. The scalar PWM method is the simplest modulation method employed in the three-level NPC inverter. In the scalar PWM method, modulation and triangular carrier waves are compared and the intersection points give the switching instants for the inverter switches. In the space vector PWM method, the switch on-state durations are calculated from the complex

number volt-seconds balance equation for the inverter voltage and the switch pulse pattern is programmed via digital PWM hardware/software.

3.4.1 The Scalar PWM Method

In the scalar PWM methods there can be two carrier waves and one modulation signal, or one carrier wave and two modulation signals. These define the two types of scalar PWM method. The first method is the unipolar PWM method and the second method is the bipolar PWM method.

In the unipolar PWM method, there are two carrier waves and one modulation signal. The unipolar PWM method is illustrated in Figure 3.8. One of the carrier waves is between 0 and $V_{dc}/2$, and it is called the "upper carrier wave." This carrier wave is associated with semiconductor switches Sx1 and Sx3. The other carrier wave is between 0 and $-V_{dc}/2$, and it is called the "lower carrier wave." This carrier wave is associated with semiconductor switches Sx2 and Sx4. When the modulation signal is positive, i.e. the modulation signal is larger than the lower carrier wave, the semiconductor switch Sx2 is kept ON and Sx4 is kept OFF. If the modulation signal is larger than the upper carrier wave, semiconductor switch Sx1 is turned ON and Sx3 is turned OFF. Then, the load terminal is connected to the positive DC bus terminal (switch state "P"). When the modulation signal is smaller than the upper carrier wave, the semiconductor switch Sx1 is turned OFF and Sx3 is turned ON. The load terminal is connected to the neutral point of the three-level NPC inverter (switch state "0"). When the modulation signal is negative, i.e. the modulation signal is smaller than the upper carrier wave, the semiconductor switch Sx3 is kept ON and Sx1 is kept OFF. If the modulation signal is smaller than the lower carrier wave the semiconductor switch Sx4 is turned ON and Sx2 is turned OFF. Then the load terminal is connected to the negative DC bus terminal (switch state "N"). When the modulation signal is bigger than the lower carrier wave, the semiconductor switch Sx2 is turned ON and Sx4 is turned OFF. Then the load terminal is connected to the neutral point (switch state "0"). As shown in Figure 3.8, in the unipolar PWM

method, the output voltage and the reference voltage polarity match (the output voltage is unipolar). Hence, "unipolar PWM."

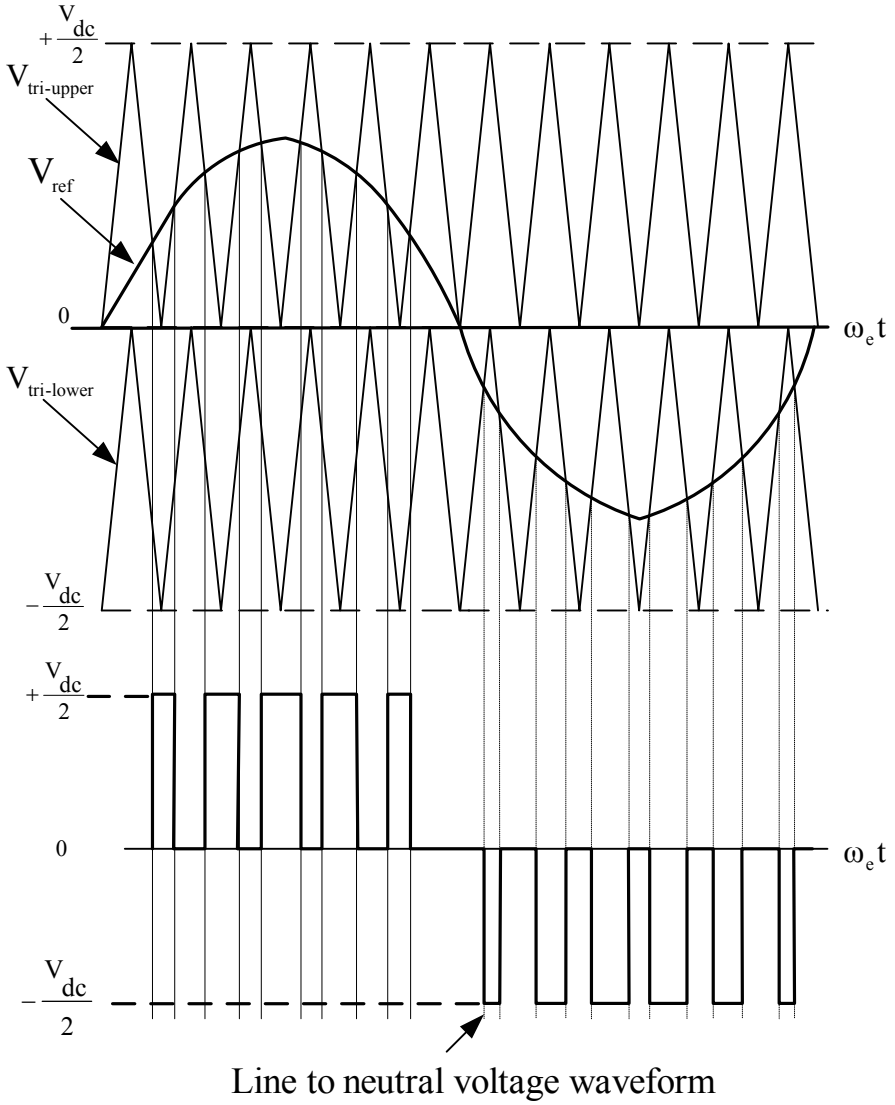


Figure 3.8 Illustration of the unipolar PWM method for the three-level NPC inverter.

In the case of bipolar PWM, there is one carrier wave and there are two modulation waves. In Figure 3.9, the bipolar PWM method for the three-level NPC inverter is illustrated. The carrier wave is between $-V_{dc}/2$ and $+V_{dc}/2$. The horizontal axis of the first modulation signal is at $+V_{dc}/4$ and this modulation signal is called as "upper modulation signal." The other modulation signal has a horizontal axis at - $V_{dc}/4$ and it is called as "lower modulation signal."

When the lower modulation wave is larger than the triangle, Sx1 is kept ON and Sx3 is OFF. In this case, the load terminal is connected to the positive DC bus terminal (switch state "P"). For the upper modulation wave, when the modulation wave is smaller than the triangle, Sx2 is OFF and Sx4 is ON. In this case, the load terminal is connected to the negative DC bus terminal (switch state "N"). When the lower modulation wave is smaller than the triangle or when the upper modulation wave is larger than the triangle the switches Sx1 and Sx4 are kept OFF and Sx2 and Sx3 are kept ON. In this case, the load terminal is connected to the neutral point of the DC bus (switch state "0").

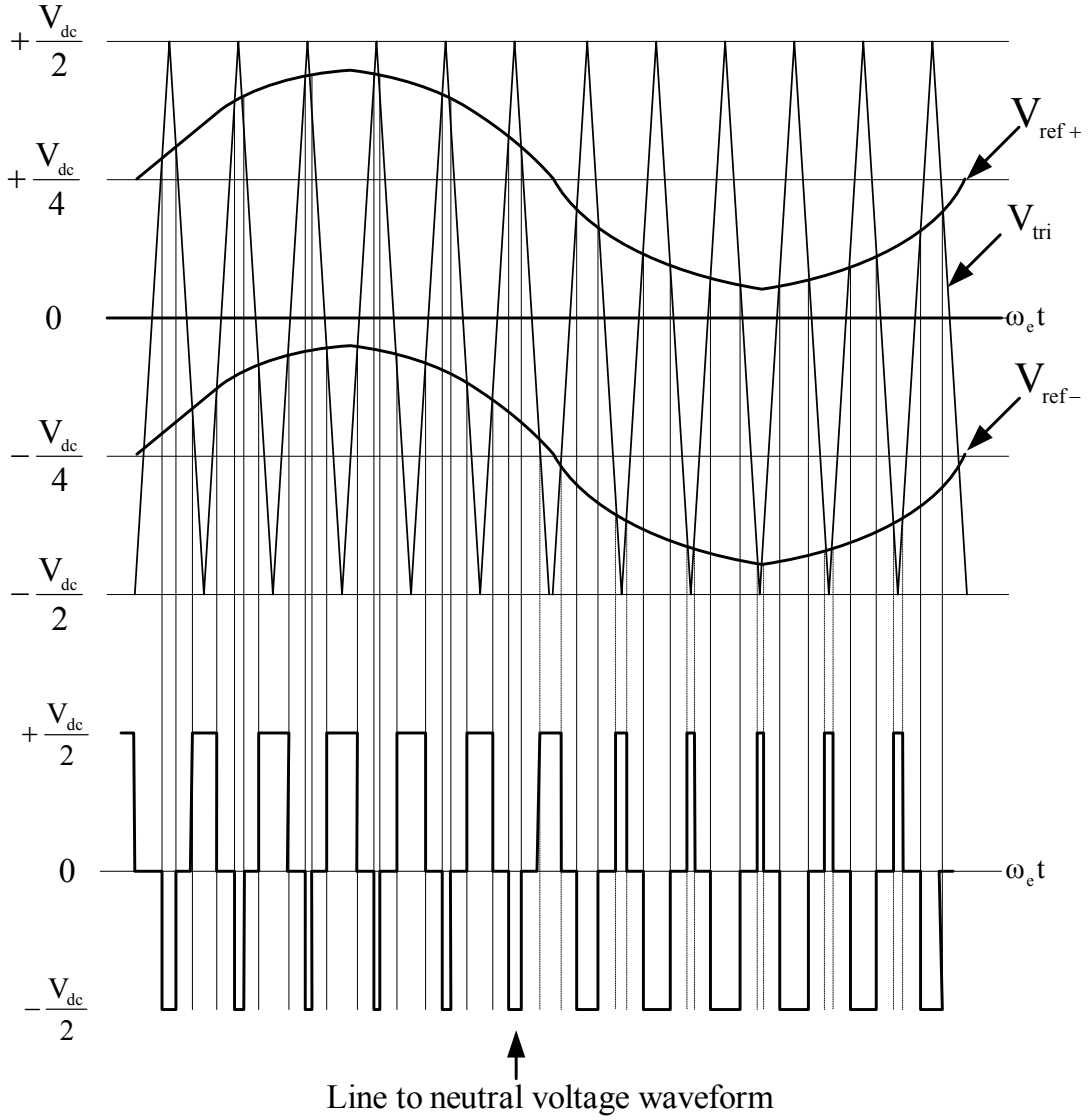


Figure 3.9 Illustration of the bipolar PWM method for the three-level NPC inverter.

In both the unipolar and bipolar modulation methods, the neutral point potential can be controlled by adding a zero sequence modulation signal to each modulation signal. Various zero sequence signal injection based neutral point potential control methods have been reported [18], [19], [20]. In general, scalar PWM methods are easier to implement than the space vector PWM approach. However, scalar modulation methods are less intuitive in terms of neutral point potential performance of the NPC inverter. Further, the controllability of the neutral point potential in these methods is more constrained than the space vector PWM approach. For this reason, neutral point potential control by using scalar PWM is not within scope of this thesis.

3.4.2 The Space Vector PWM Method

In the space vector approach, the three-phase inverter and load variables (voltages or currents) are transformed to complex variables via the following formula.

$$X = \frac{2}{3}\left(X_U + aX_V + a^2 X_W\right) \tag{3.1}$$

$$X = X_q - jX_d = |X|e^{-j\psi} \tag{3.2}$$

$$a = e^{j120} = -\frac{1}{2} + j\frac{\sqrt{3}}{2} \tag{3.3}$$

$$a^2 = e^{j240} = -\frac{1}{2} - j\frac{\sqrt{3}}{2} \tag{3.4}$$

At this stage let's define a set of three-phase sinusoidal voltage references in the following.

$$\left.\begin{aligned} V_U^* &= V_m \cos(w_e t) \\ V_V^* &= V_m \cos(w_e t - 2\pi/3) \\ V_W^* &= V_m \cos(w_e t - 4\pi/3) \end{aligned}\right\} \tag{3.5}$$

V_m: magnitude of the sinusoidal reference voltage

w_e : radial electrical frequency of the reference voltage

With the given vector transformation, the above given three-phase sinusoidal voltage references are transformed to a reference voltage vector that has a magnitude of $|V_{ref}|$ and rotates with the angular speed of w_e. The reference voltage vector has complex form, as shown in (3.7).

$$V_{ref} = \frac{2}{3}\left(V_U^* + aV_V^* + a^2 V_W^*\right) \tag{3.6}$$

$$V_{ref} = V_q - jV_d = V_m e^{-jw_e t} \tag{3.7}$$

In the three-level NPC inverter, the 27 different switch combinations give 27 different phase output voltage values. Transforming these voltages to the vector coordinates with the space vector transformation, the space vector representation of the three-level NPC inverter can be obtained. In Figure 3.10 space vector representation of the three-level NPC inverter output voltages is shown. In Figure 3.10 in some locations there are multiple circles on the same points. This means that the corresponding output voltage vector can be created from two or three different switch states (redundant states). The space vector representation of the three-level NPC inverter contains 27 different switch states corresponding to 27 voltage vectors. Nineteen different and eight redundant voltage vectors are available in the space vector representation. In Figure 3.10, voltage vectors “ap,” “an,” “bp,” and “bn” are called as “small voltage vectors,” the vectors “oo,” “op,” and “on” are called as “zero voltage vectors,” the vectors “a” and “b” are called as “full voltage vectors,” and the vector “c” is called as “medium voltage vector.” Class-I switch states correspond to

small voltage vectors, Class-II switch states correspond to medium voltage vectors, and switch states "PNN," "PPN," "NPN," "NPP," "NNP," and "PNP" (Class-III switch states) correspond to full voltage vectors. Switch states "PPP," "000," and "NNN" (Class-III switch states) correspond to zero voltage vectors. Therefore, the small voltage vectors load the neutral point and charge or discharge the neutral point potential. The medium voltage vectors inject triplen harmonic current to the neutral point and the neutral point potential fluctuates at the third harmonic frequency of the output currents. By using space vector PWM, the control of the neutral point potential can be performed effectively.

In the space vector approach, over one PWM cycle a specific number of voltage vectors are selected and used in a specific time length and sequence. Typically, three voltage vectors are selected. In this case, associated with the three voltage vectors V_k, V_{k+1}, V_{k+2}, three time lengths T_k, T_{k+1}, T_{k+2} should be determined. To calculate the time lengths, the complex variable volt-second balance rule is applied.

$$V_{ref}T = V_kT_k + V_{k+1}T_{k+1} + V_{k+2}T_{k+2} \tag{3.8}$$

When expressed in terms of the d-q coordinate components, the above equation is expanded as follows.

$$(V_q - jV_d)T = (V_{kq} - jV_{kd})T_k + (V_{(k+1)q} - jV_{(k+1)d})T_{k+1} + (V_{(k+2)q} - jV_{(k+2)d})T_{k+2} \tag{3.9}$$

In (3.9) the real parts of the both sides should be equal to each other. This rule is also valid for the imaginary parts. Then, (3.10) and (3.11) are obtained.

$$V_qT = V_{kq}T_k + V_{(k+1)q}T_{k+1} + V_{(k+2)q}T_{k+2} \tag{3.10}$$

$$V_dT = V_{kd}T_k + V_{(k+1)d}T_{k+1} + V_{(k+2)d}T_{k+2} \tag{3.11}$$

The total time lengths of voltage vectors in a PWM period should be equal to the PWM period.

$$T = T_k + T_{k+1} + T_{k+2} \tag{3.12}$$

Once the inverter output voltage vectors are selected, the above three equations can be solved to obtain the three unknown time lengths.

The standard Nearest Triangle Vector (NTV) space vector PWM method is the first and most widely utilized space vector PWM method in the three-level NPC inverter. In the following, the NTV-PWM method will be described and the analysis of the neutral point current and potential will be studied.

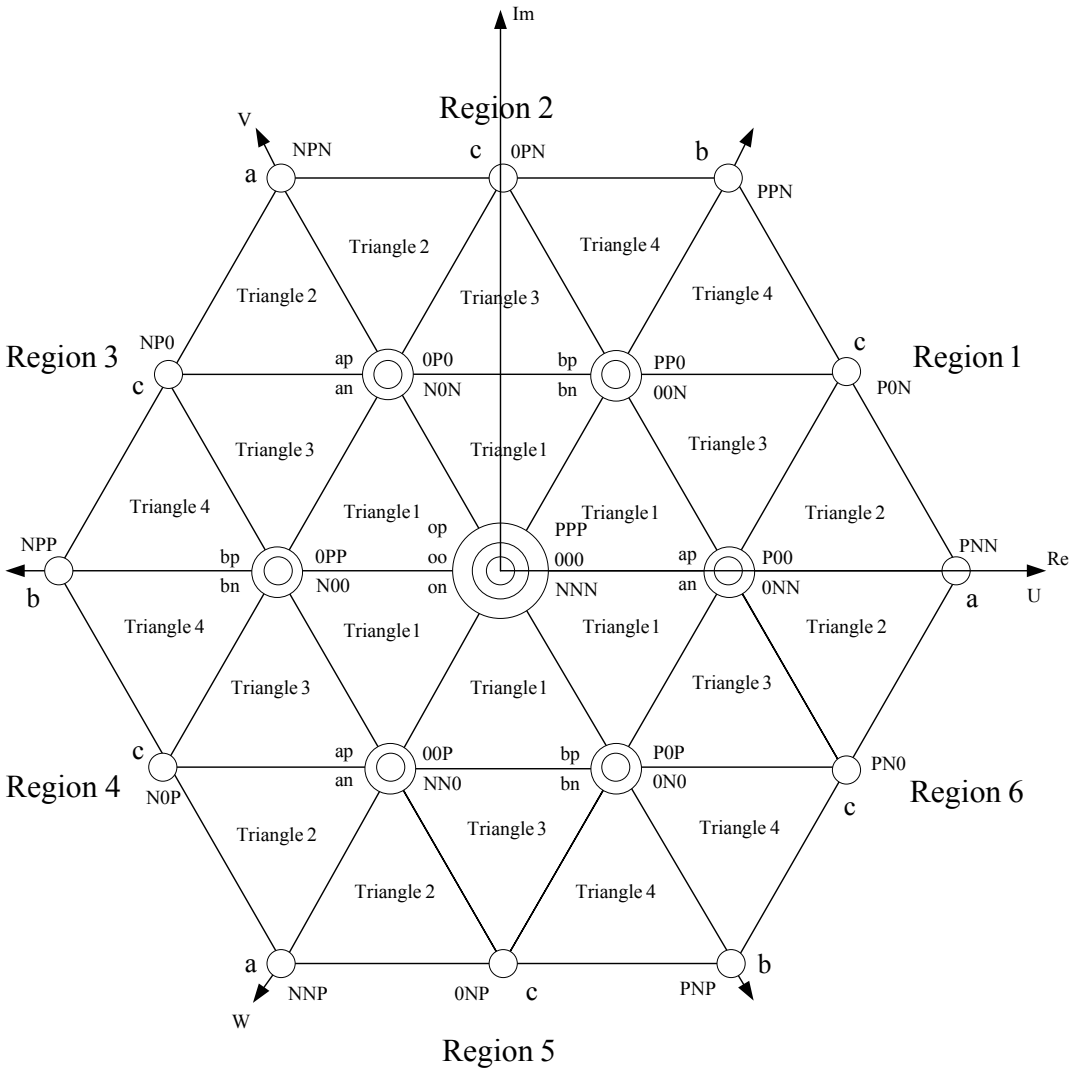


Figure 3.10 Space vector representation of the three-level NPC inverter output voltages.

3.4.2.1 Nearest Triangle Vector (NTV) Space Vector PWM

In this modulation method, as shown in Figure 3.10, there are six main regions and each region has four sub-regions. They are shown in Figure 3.10. In the NTV-PWM approach, the reference voltage vector is laid out in the inverter voltage vector space. After finding the main region (R=1,2,3,4,5 or 6), that the reference voltage vector belongs, the next step is to find the triangle region where the tip point of the reference voltage vector belongs. Provided that the reference vector is within the inverter hexagon, the tip point of the reference voltage vector will be in one of the four triangular sub-regions. The first sixty-degrees of the vector space is illustrated in detail in Figure 3.11 for the purpose of discussion. In the figure, the reference voltage vector is in "Region 1" and the tip point of the reference voltage vector is in "Triangle 3". The reference voltage vector is synthesized by the voltage vectors whose tip points are the edges of "Triangle 3." These vectors are the small voltage vectors named "ap," "an," "bp," and "bn," the medium voltage vector "c." This modulation method is called as "Nearest Triangle Vector (NTV)" modulation method because the voltage vectors nearest to the reference voltage vector are utilized. In this method, the time length of the output voltage vectors in a PWM period is given in Table 3.2.

Table 3.2 Nearest triangle vector time length calculation

Region	NTV	Time length of NTV
Triangle 1	op,oo,on	$t_0=T\{1-2M_i\sin(\theta+\pi/3)\}$
	ap,an	$t_1=2M_iT\sin(\pi/3-\theta)$
	bp,bn	$t_2=2M_iT\sin(\theta)$
Triangle 2	ap,an	$t_1=2T\{1-M_i\sin(\theta+\pi/3)\}$
	c	$t_3=2M_iT\sin(\theta)$
	a	$t_4=T\{2M_i\sin(\pi/3-\theta)-1\}$
Triangle 3	ap,an	$t_1=T\{1-2M_i\sin(\theta)\}$
	bp,bn	$t_2=T\{1-2M_i\sin(\pi/3-\theta)\}$
	c	$t_3=T\{2M_i\sin(\theta+\pi/3)-1\}$
Triangle 4	bp,bn	$t_2=2T\{1-M_i\sin(\theta+\pi/3)\}$
	c	$t_3=2M_iT\sin(\pi/3-\theta)$
	b	$t_5=T\{2M_i\sin(\theta)-1\}$

T: PWM Period

M_i: modulation index

$$M_i = \frac{V_m}{(V_{dc}/\sqrt{3})}$$

V_m: magnitude of the reference voltage vector

V_{dc}: DC bus voltage

θ: angle from the nearest full voltage vector "a" to the reference vector

t_0: total time length of the zero voltage vectors "op," "oo," and "on"

t_1: total time length of the small voltage vectors "ap" and "an"

t_2: total time length of the small voltage vectors "bp" and "bn"

t_3: time length of the medium voltage vector "c"

t_4: time length of the full voltage vector "a"

t_5: time length of the full voltage vector "b"

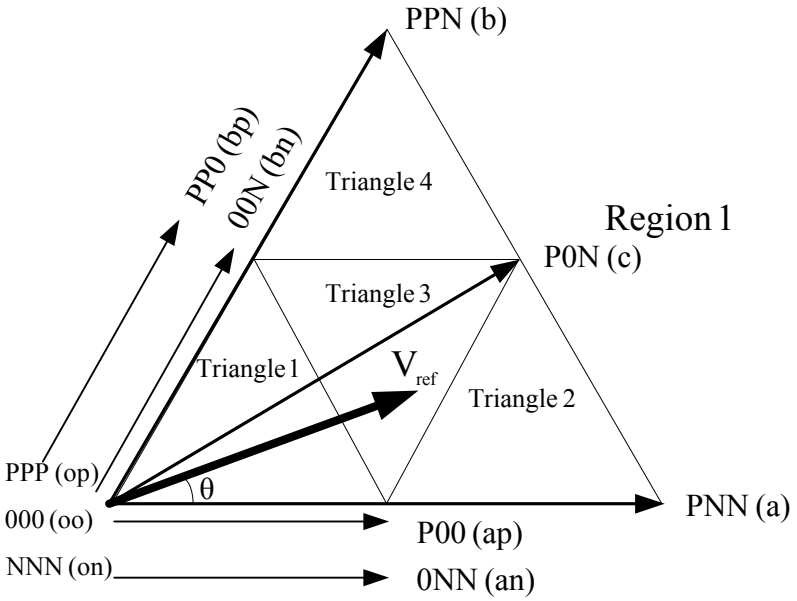


Figure 3.11 Illustration of the three-level NPC inverter space vectors in Region 1.

After calculating the time lengths of the voltage vectors, these voltage vectors can be applied in any sequence. Also these vector time-lengths can be split into subintervals and applied. Once the sequence and time partitioning details are decided, the pulse

pattern of the semiconductor switches of the inverter gets determined. The choice of the sequence and partitioning (thus the pulse pattern) influences the inverter performance substantially. The standard pulse pattern of the NTV-PWM technique is shown in Figure 3.12 [4]. The pulse pattern is determined with a high waveform quality and a minimum number of switching criteria. In this pattern, the inner triangles (triangle 1) involve bipolar line to neutral output voltage waveform and four switchings per-phase exist. This results in twelve switchings per PWM cycle. In triangles 2 and 4, the output voltage has unipolar waveform and there are two switchings per phase. Hence six switchings per PWM cycle. In triangle 3, one phase has bipolar and two phases have unipolar voltage waveforms and the total number of switching is eight.

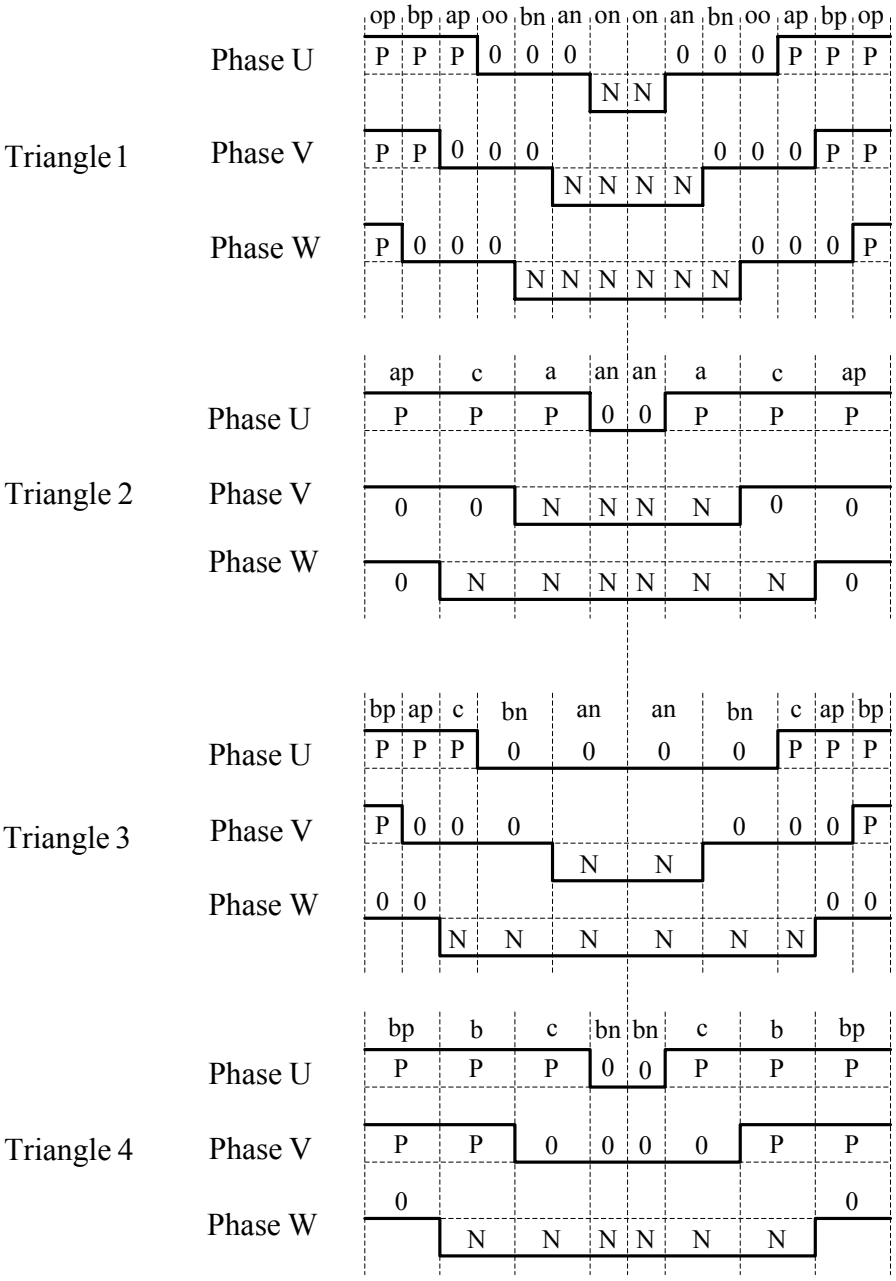


Figure 3.12 The pulse pattern of NTV-PWM in Region 1 Triangles 1-4.

Given the vector duty cycles, the switch duty cycles can be calculated and programmed such that the desired pulse pattern is generated. The resulting duty cycle functions resemble the scalar modulation method waveforms. For example, at steady-state sinusoidal operation, the duty cycles of the semiconductor switches of one inverter leg are shown in Figure 3.13 for a high modulation index value (M_i= 0.8). For high modulation index, as shown in Figure 3.10, the tip point of the reference voltage vector rotates and passes through triangles 2, 3, and 4 in "Region

1" and through triangles 4, 3, and 2 in "Region 2," and so on. This can be followed from Figure 3.10. For example, for "Region 1" and "Region 6," in triangles 2, 3, and 4, the phase "U" has unipolar voltage waveform as it is shown in Figure 3.12. Phase "U" output voltage has only zero and positive values. To obtain such a waveform the semiconductor switch SU2 should be kept ON and duty cycle of SU2 is equal to one. In "Region 2" and "Region 5" phase "U" pulse pattern is the same as phase "V" pulse pattern in "Region 1." In that case, in triangle 4 the "U" phase waveform is unipolar and it has only zero and positive values as, it can be seen from Figure 3.12. The duty cycle of the SU2 is equal to one. In other triangles and regions, the duty cycle of semiconductor switch SU2 is not equal to one. For "Region 1" and "Region 5" for all the triangles, phase "U" voltage waveform has all values (positive, zero and negative). As a result, the duty cycle of semiconductor switch SU1 is not equal to zero. In "Region 2" and "Region 5" and in triangle 2 the phase "U" voltage waveform has only zero and negative value, in that case the duty cycle of semiconductor switch SU1 is equal to zero. For other triangles the duty cycle of SU1 is not equal to zero. In "Region 3" and "Region 4," phase "U" pulse pattern is the same with phase "W" pulse pattern of "Region 1." For "Region 3" and "Region 4," and triangle 2, 3, and 4, the waveform of phase "U" is unipolar and has only zero and negative values as, it can be seen from Figure 3.12. Therefore, the semiconductor switch SU1 duty cycle is equal to zero. Duty cycle waveforms obtained are the same as the scalar PWM method known as SVPWM (involving injection of a zero sequence signal that is created from half of the smallest magnitude signals of the sinusoidal reference modulation waves) with half third harmonic injected modulation signals.

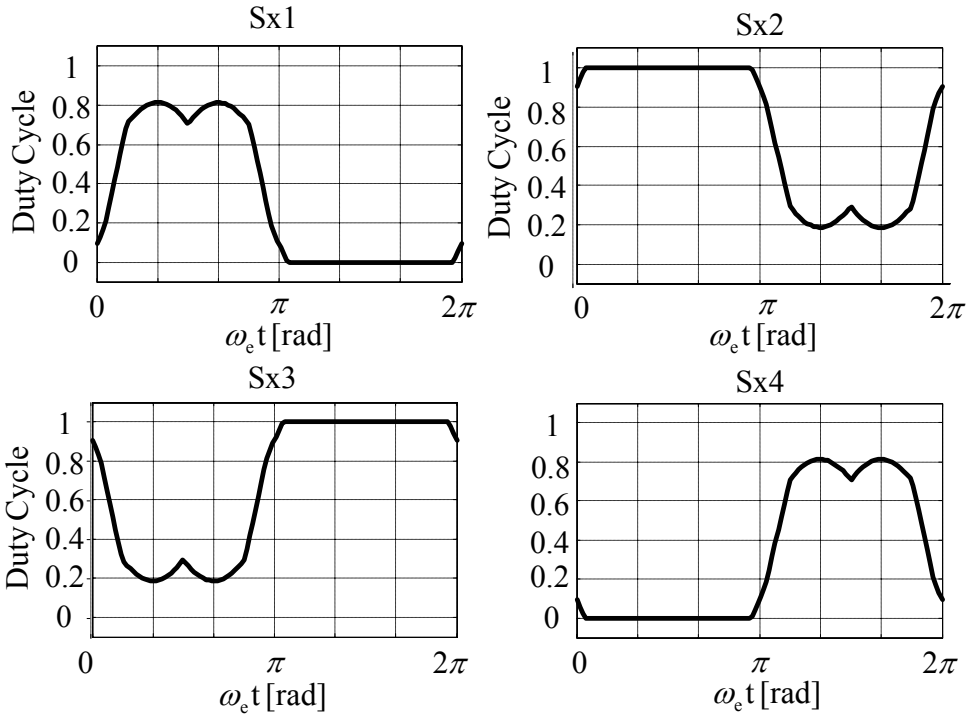


Figure 3.13 Duty cycles of the semiconductor switches of one inverter leg for NTV-PWM (M_i=0.8).

3.4.2.2 Neutral Point Potential Analysis of The NTV-PWM

In the NTV-PWM technique, in order to control the neutral point potential the duty cycles of the redundant small voltage vectors are employed. As seen from Figure 3.10 the small voltage vectors can be produced by two different switch states (redundant states). These two small voltage vectors have opposite influence on the neutral point potential. One of them charges the neutral point and drifts its potential up, the other one discharges neutral point and drifts its potential down depending on the polarity of the associated current. By using this property the neutral point potential can be kept within specified tolerance boundaries. To control the neutral point potential by using small voltage vectors two parameters should be defined. These parameters are shown in following equations.

$$\alpha_1 = \frac{t_{ap}}{t_1} \qquad t_{ap} + t_{an} = t_1 \qquad 0 \le \alpha_1 \le 1 \tag{3.13}$$

$$\alpha_2 = \frac{t_{bp}}{t_2} \qquad t_{bp} + t_{bn} = t_2 \qquad 0 \le \alpha_2 \le 1 \tag{3.14}$$

t_1 : total time length of the small voltage vectors “ap” and “an” (In Table 3.2)

t_2 : total time length of the small voltage vectors “bn” and “bp” (In Table 3.2)

t_{ap} : time length of the small voltage vector “ap”

t_{an} : time length of the small voltage vector “an”

t_{bp} : time length of the small voltage vector “bp”

t_{bn} : time length of the small voltage vector “bn”

Assuming that the three-phase AC load currents are constant over a PWM period, the average neutral point current over a PWM period “i_n” can be calculated by using (3.15) [4].

$$i_n = \frac{i_x(R)\cdot(t_{an} - t_{ap}) + i_y(R)\cdot(t_{bp} - t_{bn}) + i_z(R)\cdot t_3}{T} \tag{3.15}$$

In (3.15), $i_x(R)$, $i_y(R)$, and $i_z(R)$ are the phase current functions. They depend on the region defined in Figure 3.10. Table 3.3 shows the region dependency of the variables $i_x(R)$, $i_y(R)$, and $i_z(R)$.

Table 3.3 Region dependent phase current functions

Region	1	2	3	4	5	6
$i_x(R)$	i_u	i_v	i_v	i_w	i_w	i_u
$i_y(R)$	i_w	i_w	i_u	i_u	i_v	i_v
$i_z(R)$	i_v	i_u	i_w	i_v	i_u	i_w

By substituting (3.13) and (3.14) in (3.15), the following equation is obtained.

$$i_n = \frac{i_x(R)\cdot(1-2\alpha_1)\cdot t_1 - i_y(R)\cdot(1-2\alpha_2)\cdot t_2 + i_z(R)\cdot t_3}{T} \tag{3.16}$$

For the purpose of neutral point potential variation analysis, an equivalent circuit can be derived. To obtain the equivalent circuit, the DC bus voltage source is replaced with two ideal DC voltage sources with constant (and equal) magnitude and the neutral point charging currents are modeled as a current source (i_n) as shown in Figure 3.14. As shown in the following equation, the average change of the neutral point potential over a PWM period (ΔV_n) is the integral of (3.16).

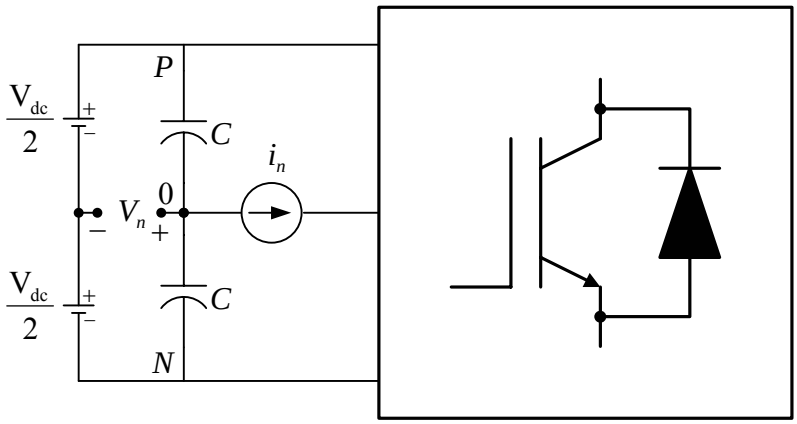


Figure 3.14 Neutral point potential charging current source equivalent circuit of the inverter drive.

$$\Delta V_n = \frac{1}{2C}\int_{kT}^{(k+1)T} i_n(t)dt \tag{3.17}$$

Substituting (3.16) in the above equation, the explicit form of the neutral point potential increase over a PWM period can be written in terms of the phase currents and the redundancy functions in the following.

$$\Delta V_n = \frac{1}{2C}\{i_x(R)\cdot(1-2\alpha_1)\cdot t_1 - i_y(R)\cdot(1-2\alpha_2)\cdot t_2\} + \frac{1}{2C}\cdot i_z(R)\cdot t_3 \quad (3.18)$$

$$V_{n-new} = \Delta V_n + V_{n-old} \quad (3.19)$$

$$V_{n-new} = \frac{1}{2C}\{i_x(R)\cdot(1-2\alpha_1)\cdot t_1 - i_y(R)\cdot(1-2\alpha_2)\cdot t_2\} + \frac{1}{2C}\cdot i_z(R)\cdot t_3 + V_{n-old} \quad (3.20)$$

C : the capacitance value of one of the series connected DC bus capacitors

T : PWM period

V_{n-old} : the neutral point potential value at the beginning of the current PWM period

V_{n-new} : the neutral point potential value at the end of the current PWM period

If $V_{n\text{-}new}$ has positive value, this means that the voltage of the lower DC bus capacitor is larger than the upper DC bus capacitor. If $V_{n\text{-}new}$ is negative, the upper DC bus capacitor voltage is larger than the lower DC bus capacitor voltage.

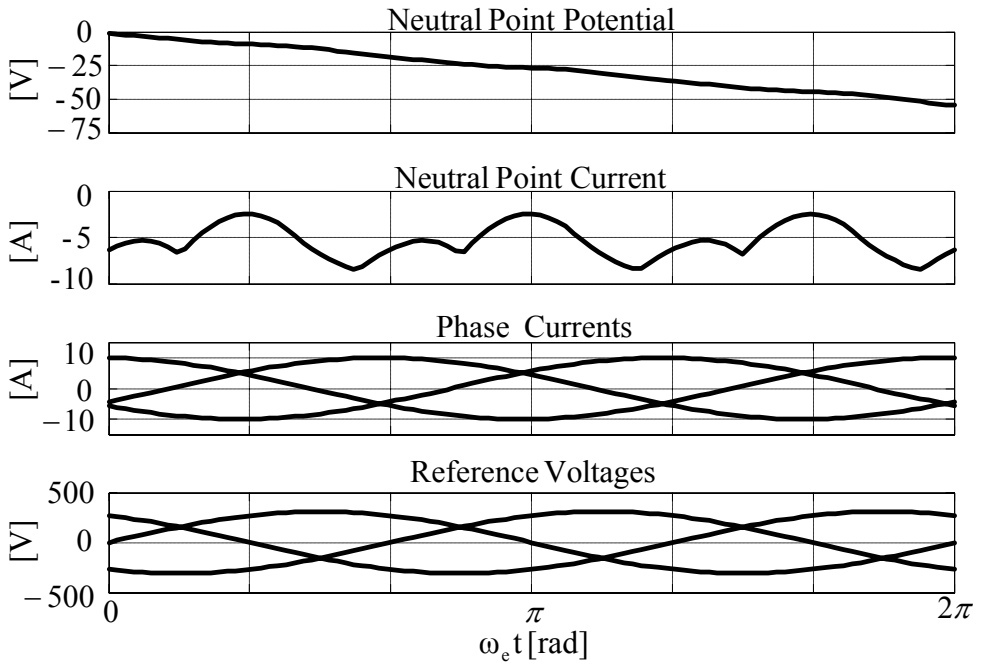
In triangles 1 and 3 there are two redundant voltage vectors (small voltage vectors "ap," "an," "bp," and "bn") and in triangles 2 and 4 there is only one redundant voltage vector. If α is equal to 0.5 and $\alpha=\alpha_1=\alpha_2$, the effects of $i_x(R)$ and $i_y(R)$ on the neutral point potential disappear. This is valid if the computed and applied time lengths of the voltage vectors are exactly equal. In practice this condition may not be exactly matched due to inverter turn-on delay times, pulse programming resolution constraints, and semiconductor switch dynamic characteristics (turn-on and turn-off times of the IGBT). Therefore, in practice due to non-ideality of the PWM generator and switches there may be a neutral point potential fluctuation or drift due to the small vector even if $\alpha=\alpha_1=\alpha_2=0.5$ value is retained. In practical applications, dynamic loading conditions also may cause non-zero result on the first term of (3.18) for $\alpha=\alpha_1=\alpha_2=0.5$ and neutral point potential variation results. For example, when only the inner hexagon is utilized (corresponding to low modulation index) during dynamic loading, neutral point potential drift can be significant. Inside the inner hexagon, the small redundant vectors are utilized along with the zero voltage vectors and no medium vectors are utilized. In this case the t_3 involving term of (3.18) is zero. With $\alpha=\alpha_1=\alpha_2=0.5$, according to (3.18), it is expected that the average neutral

point potential variation to be zero. However, this may not be the case during a dynamic condition. This behavior can be illustrated via system simulation or experimental evaluation. Therefore, feedback control involving the redundancy functions is necessary. When utilizing the outer triangles (implying high modulation and utilization of the full inverter hexagon), the medium voltage vector is also utilized and according to (3.16) it creates additional term on the neutral point current and results in neutral point potential fluctuation. Therefore, the parameter α should be changed (controlled) dynamically instead of being held constant.

In the following the influence of the redundancy function on the neutral point potential will be illustrated via computer simulation of the average model shown in Figure 3.14. In this simulation the neutral point potential initial value is zero. As the redundancy functions α_1 and α_2 are changed, it is observed that the neutral point potential varies in a specific manner. The simulation utilizes equation (3.20) for the neutral point potential calculation. In the simulation a balanced three-phase current sink type load with 50 Hz frequency and 7.1 A rms (10 A peak) value is considered. The inverter three-phase reference voltages involve only fundamental component and their magnitude corresponds to 0.72 modulation index (implying operation along triangles 2-3-4). The phase angle between a phase reference voltage and its associated phase current sink is 25^o corresponding to 0.9 lagging power factor.

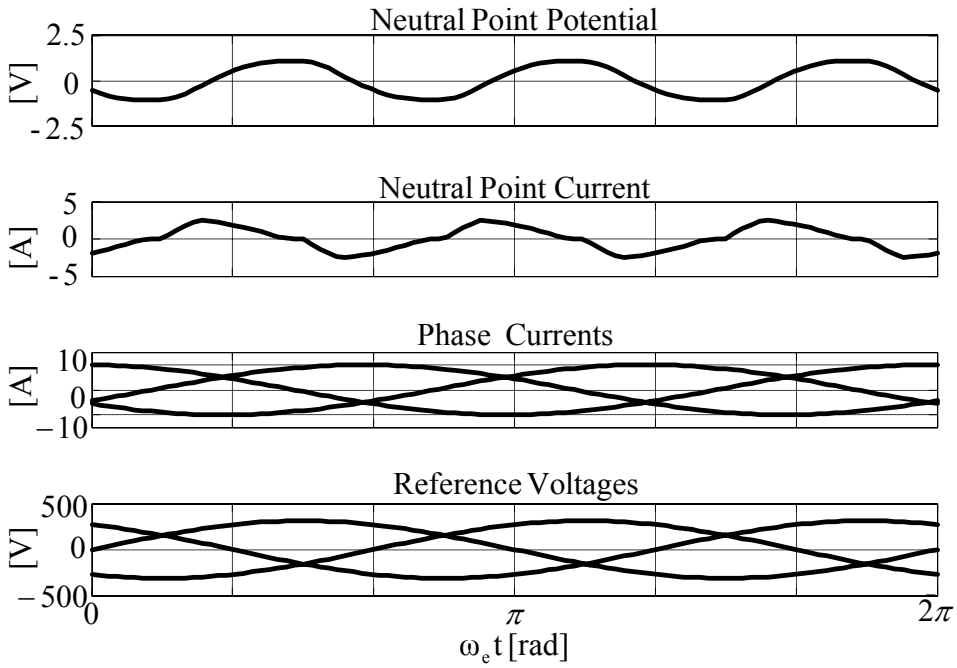
Figure 3.15 shows the neutral point current and potential variation at steady-state sinusoidal operation for various $\alpha = \alpha_1 = \alpha_2$ values. As shown in Figure 3.15.a, for $\alpha=\alpha_1=\alpha_2=0$, the average value of the neutral point current is not equal to zero. It has a positive DC component that charges and drifts up the neutral point potential. In Figure 3.15.b, $\alpha=\alpha_1=\alpha_2=0.5$ corresponds zero DC component on the neutral point current and the neutral point potential fluctuates around zero potential. There is no drift on the neutral point potential. As shown in Figure 3.15.c, for $\alpha=\alpha_1=\alpha_2=1$, the neutral point current has a negative DC component and the neutral point potential drifts down. This discussion illustrates that the neutral point current and thus the neutral point potential can be controlled by varying α_1 and α_2.

In the inner hexagon (low modulation index), the medium voltage vector is not utilized and t_3 is equal to zero. For a high modulation index value, the medium voltage vector is utilized and the time length t_3 is not equal to zero. The $i_z(R) \cdot t_3$ term exists in (3.16). Therefore, the neutral point potential problem is variant in space and specifically depends on whether the inner or outer triangles are utilized.

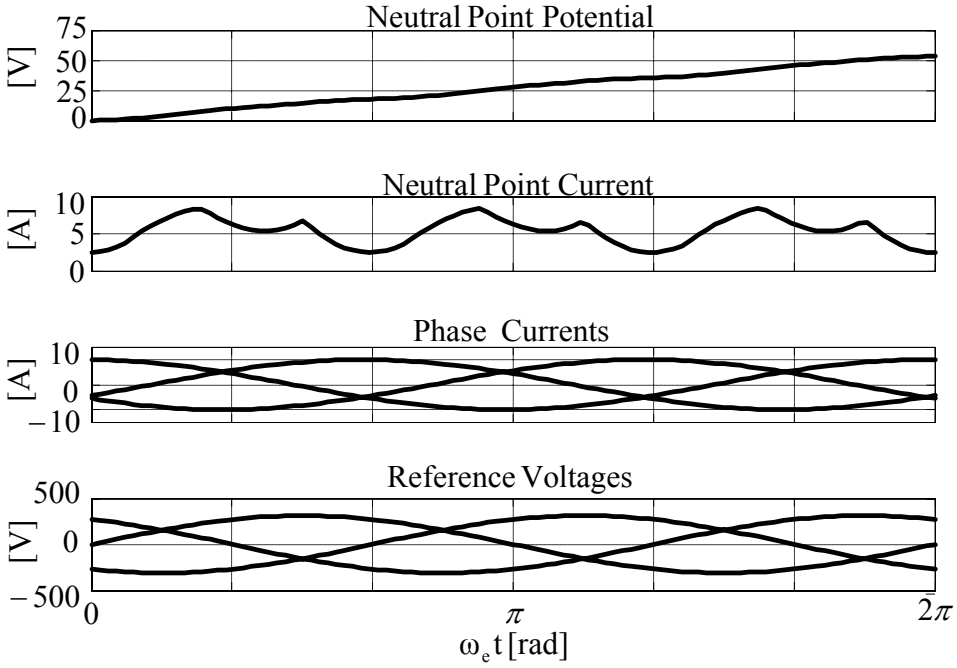


(a) α=0

Figure 3.15 Neutral point potential variation as a function of α; (a): α=0, (b): α=0.5, (c): α=1 (I=7.1A, PF=0.9 and M_i=0.72).



(b) α=0.5



(c) α=1

Figure 3.15 Neutral point potential variation as a function of α; (a): α=0, (b): α=0.5, (c): α=1 (I=7.1A, PF=0.9 and M_i=0.72).

3.5 Control of The Neutral Point Potential

The previous section illustrated that the neutral point potential variation of the three-level NPC inverter has to be controlled. There are two approaches to the neutral point potential control problem of the three-level NPC inverter. The first approach involves additional balancing hardware which could be active or passive circuits. The second approach is totally software based and the PWM pulse pattern is modified for the purpose of neutral point potential balancing. These control methods will be described in detail in the following.

3.5.1 Hardware Configuration Based Neutral Point Potential Balancing Methods

The neutral point potential problem of the three-level NPC inverter can be solved by employing additional circuitry. The additional circuitry may be passive or active circuits. In the passive balancing approach, balancing resistors are connected in parallel with the DC bus capacitors as shown in Figure 3.16.

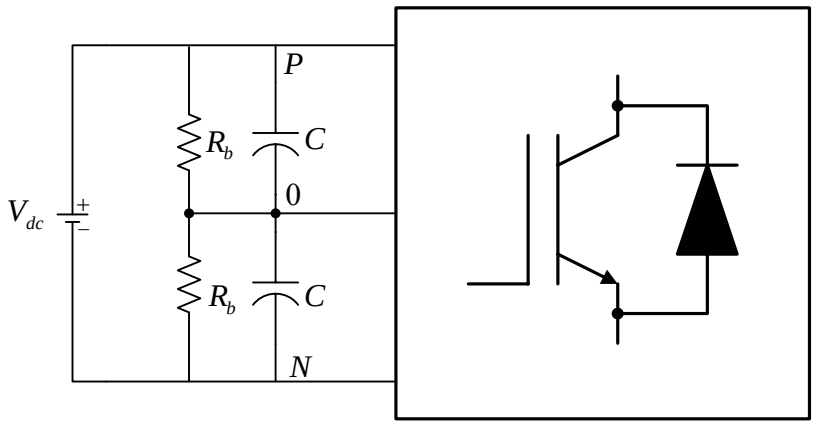


Figure 3.16 Balancing resistor circuit.

The resistance value is calculated by using the equivalent circuit as shown in Figure 3.17. If there is an imbalance between the capacitor voltages, a current flows from the resistors to the neutral point to charge the neutral point in a direction to decrease the imbalance. When the imbalance decreases to zero, the balancing current

disappears. The current may become zero in very short time depending on the time constant of the RC circuit. The time constant of the circuit is equal to $R_b \cdot C$. To obtain quick response the time constant of the circuit should be selected small. For example, in the case of C=1000 μF in order to cancel the neutral point potential in 20 ms the balancing resistance should be 20 Ω. For 500 V DC bus voltage the total power dissipation on the resistors is equal to 6.25 kW. The 6.25 kW loss is quite significant even for high power drives involving megawatt ratings. Thus, the passive resistive balancing approach is not feasible for balancing the neutral point potential. The passive resistor based balancing approach is only feasible for inverter drives involving series connected capacitors with no neutral point potential connection (such as two-level inverters at high voltage ratings). In those cases, the series capacitors may have small differences in terms of leakage currents and capacitance values that result in small voltage imbalances. Such small voltage imbalances could be eliminated with fairly large balancing resistors and typically these resistors measure in at least several kilo-ohms in value. However, in the NPC inverter, the neutral point current can be significantly larger than the leakage currents in orders of magnitude and balancing resistors are not satisfactory to balance the capacitor voltages in acceptable time durations (in several milliseconds or less).

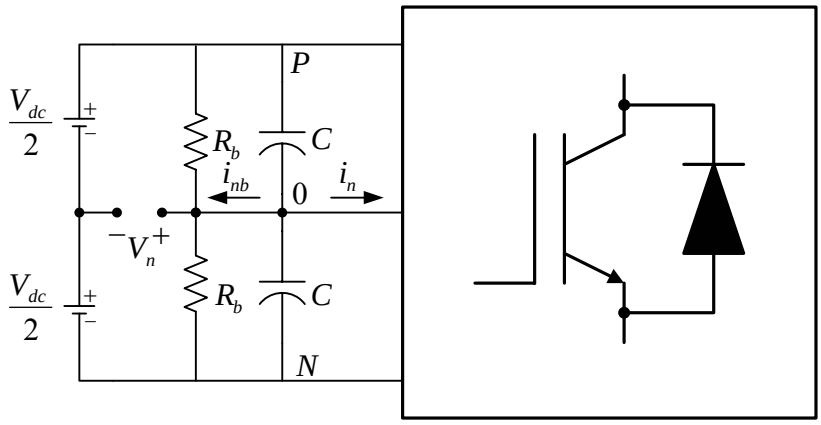


Figure 3.17 DC bus equivalent circuit illustrating the passive resistance based neutral point potential balancing technique.

Active circuits may also be used to compensate for the neutral point potential error. One such approach involves two DC-DC converters connected together as shown in Figure 3.18 [21]. The balancing circuit consists of one buck DC-DC converter and one boost DC-DC converter. S_1, L_1, D_1, and C_2 are the components of the buck converter. The boost converter consists of S_2, L_2, D_2, and C_1. In the balancing mode, the buck and boost converters work in complementary periods. When the voltage of the capacitor C_1 (V_{C1}) is greater than the voltage of the capacitor C_2 (V_{C2}), the buck DC-DC converter is activated and charges up C_2 (discharges C_1) by operating S_1 in PWM mode until the imbalance is eliminated. If V_{C2} is greater than V_{C1}, the boost DC-DC converter operates. In this case, the boost converter discharges capacitor C_2 and charges capacitor C_1 via PWM operation of S_2 until the imbalance disappears.

The above described hardware fixes to the neutral point potential problem are practically prohibitive in most general purpose inverter drive applications. While the first method is highly problematic in terms of energy efficiency, the DC-DC converter based solution involves high auxillary converter cost. The voltage ratings of the power transistors (IGBTs) and diodes are higher than the NPC inverter IGBTs. Although the current ratings of the devices are small compared to the nominal load current, the high voltage ratings imply cost prohibitive solution. Therefore, except in some niche applications, the most practical neutral point potential balancing methods involve inverter pulse pattern modifications as they involve little or no additional cost.

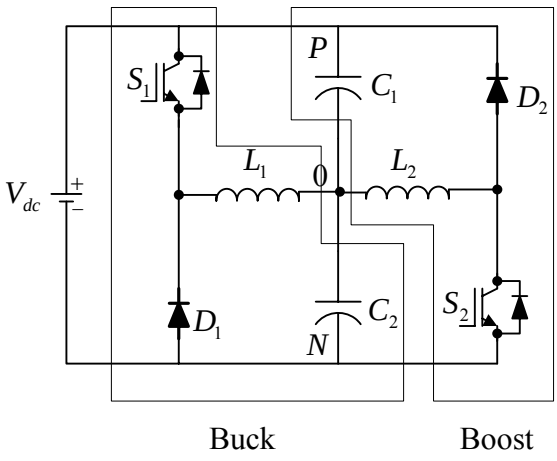


Figure 3.18 An active neutral point potential balancing circuit [21].

3.5.2 Pulse Pattern Modification Based Neutral Point Potential Balancing Methods

As seen from Figure 3.15.a to Figure 3.15.c, the neutral point potential can be controlled by changing (incrementing/decrementing) the α_1 and α_2 parameters. To change α_1 and α_2, the neutral point potential is observed by means of a feedback signal. According to the feedback signal α_1 and α_2 may be increased/decreased by an appropriate amount. The correction can be provided in incremental steps, by means of a linear controller such as a Proportional and Integral (PI) type controller, or more intelligently the neutral point potential error can be manipulated precisely by evaluating (3.20).

With the control variables of the standard NTV-PWM method being the redundancy functions α_1 and α_2 these parameters can be coordinated in two forms. In the first form, the two parameters α_1 and α_2 are equal. This method is called as the "uniform α" method. In the second method, α_1 and α_2 are coordinated in a manner to provide maximum capacity of charge so that the neutral point potential control capability of NTV-PWM will be maximized. Hence, "optimal α" method. In the NTV-PWM method, these two are the only choice. However, controlling the neutral point potential with a better performance without an additional degree of freedom is impossible. A third method which involves the introduction of a third variable, γ is introduced in this thesis. In this method the pulse pattern of NTV-PWM is also modified. In the so called "two-parameter method" the α parameters are optimized as in the "optimal α" method and the additional parameter γ is the other control parameter. Hence, the "two parameter method." Therefore, three unique pulse pattern modification based neutral point potential balancing methods will be considered in this thesis. In all these methods, the modulation parameters are utilized along with a controller that makes decision regarding the parameter values for neutral point potential balancing. In the following, the three methods will be described in detail.

3.5.2.1 The Uniform α Control Method

Of all the space vectors, only the small voltage vectors and the medium voltage vectors load the neutral point. Therefore, controlling the redundancy of the small voltage vectors, the neutral point potential can be controlled. In the uniform α control method, the redundancy functions of the small voltage vectors are selected equal as $\alpha=\alpha_1=\alpha_2$. In this case, the neutral point current equation of (3.16) can be re-written in the following.

$$i_{n\alpha u} = \frac{(1-2\alpha)\cdot\left[\, i_x(R)\cdot t_1 - i_y(R)\cdot t_2 \,\right] + i_z(R)\cdot t_3}{T} \tag{3.21}$$

Evaluating the neutral point potential equation of (3.20) as a function of neutral point current by employing (3.21), the dependency of the neutral point potential on the uniform α parameter can be analytically written in closed form. The selection of the α parameter for balancing the neutral point potential can be based on incremental approach or optimization technique can be utilized. If an optimization procedure is followed, the neutral point potential error can be minimized in finite PWM cycles. If $V_{n\text{-}old}$ is initially zero, there is no compensation requirement and α is 0.5. However, if the neutral point potential error is not zero, then the uniform α compensator decreases the neutral point potential error from $V_{n\text{-}old}$ to zero. Thus, $\Delta V_n = -V_{n\text{-}old}$. For example, if the charge available is sufficient the error can be reduced to zero rapidly. In order to decrease the neutral point potential error from $V_{n\text{-}old}$ to zero in one PWM cycle (step) the optimal uniform α can be found as follows.

$$\alpha_{uo} = \frac{1}{2} - \frac{-2C\cdot V_{n-old} - i_z(R)\cdot t_3}{2\cdot\{i_x(R)\cdot t_1 - i_y(R)\cdot t_2\}} \tag{3.22}$$

The effectiveness of the uniform α control method is illustrated in a simplified inverter model based simulation in Figure 3.19 for various modulation index values. The average model simulation described in section 3.4.2.2 is utilized for the uniform α control method simulation. For the average value simulations, each DC bus

capacitor capacitance is 1000 μF, PF=0.0 (worst case), and the three-phase 50 Hz load current rms value is equal to 7.1 A. The DC bus voltage is 540 V, and the initial value of the neutral point potential is set equal to 30 V. This large initial value is selected so that the capability of the control method to bring the neutral point potential to zero is tested. In Figure 3.19, for low modulation index values 0.2 and 0.4 the controller response is extremely slow, because the available charge for neutral point potential error compensation is not large enough to compensate for the neutral point potential error. In the low modulation index range, the small voltage vectors are utilized and each small voltage vector has an amount of neutral point potential charging capability associated with it. The individual available charge of the small voltage vectors may be sufficient to compensate for the neutral point potential error. However, when the redundancy functions of the small voltage vectors are selected equal to each other, i.e. the uniform α control method, for PF=0 the total charge from the small voltage vectors are not significant (nearly zero) because the individual charges of the small voltage vectors cancel each other. As a result, for PF=0 and low modulation index values, the uniform α control method has poor performance. The time interval required to eliminate the neutral point potential error is very long (several minutes). For the modulation index range of 0.4-0.8, the response of the uniform α method yields satisfactory result. However, as the modulation index further increases, the medium voltage vector begins to dominate and a large triplen harmonic inevitably appears on the neutral point potential. Here, for the reason that the small voltage vector time length is small, the charge capability of the method is limited and the time involved in compensating for the neutral point potential error becomes large again. Specifically, as M_i approaches unity, the response time reaches several hundred milliseconds. Therefore, for zero power factor the effectiveness region of the uniform α controller is confined to a specific M_i range that is in the range of 0.4-0.8.

For the unity power factor operating condition again simulations were conducted and the performance investigated. The uniform α method gives satisfactory performance throughout the modulation index range. As Figure 3.20 illustrates, in all the cases the neutral point potential error rapidly decays to zero. However, at the higher

modulation index range, the triplen harmonic can not be totally eliminated due to the dominance of the medium voltage vector. Hence, a small triplen harmonic frequency ripple remains on the neutral point potential.

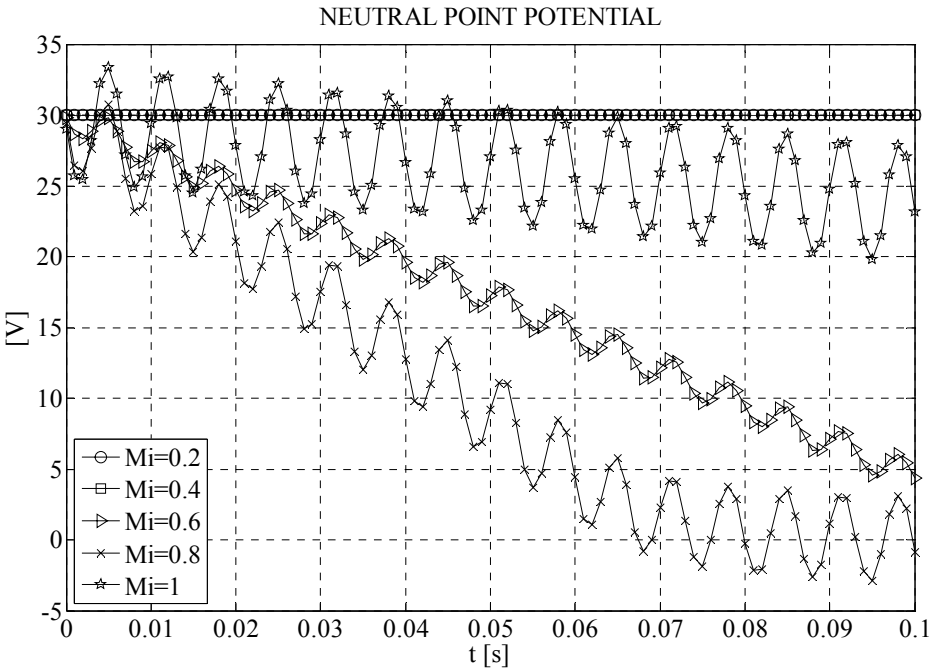


Figure 3.19 Neutral point potential control performance of the uniform α control method for various modulation index values and PF=0.0.

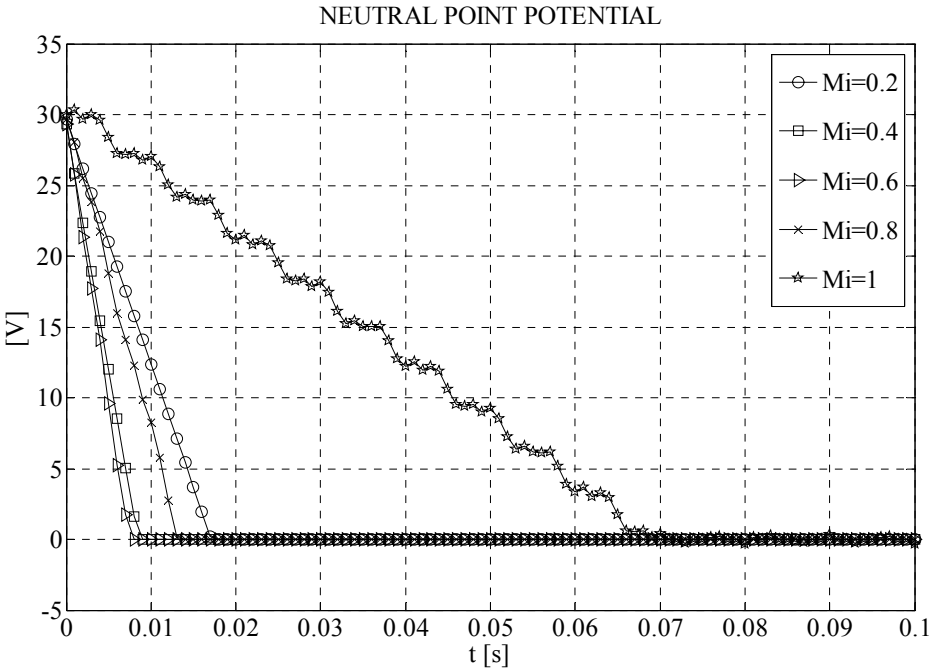


Figure 3.20 Neutral point potential control performance of the uniform α control method for various modulation index values and PF=1.0.

3.5.2.2 The Optimal α Control Method

The uniform α method does not consider the polarities of $i_x(R)$ and $i_y(R)$. Therefore, under certain circumstances, the error may not be totally eliminated. In a method that considers the phase current polarities and coordinates α_1 and α_2 such that the maximum neutral point potential controlling capability of the small vectors is utilized, the performance is superior [4]. In the outer hexagon of the voltage space vector (high modulation index) the small and medium voltage vectors load the neutral point. To control the neutral point potential, the formula given by (3.22) gives less than optimal results. The suggested neutral point potential control technique in [4] uses the polarity information of the currents $i_x(R)$ and $i_y(R)$. The parameters α_1 and α_2 are determined according to Table 3.4, and the maximum charge for neutral point potential control becomes available. For example, in "Region 1" and for PF=1, $i_x(R)$ is positive and $i_y(R)$ is negative. For PF=0 (lagging) $i_x(R)$ and $i_y(R)$ are positive. For PF=-1, $i_x(R)$ is negative and $i_y(R)$ is positive.

$$i_n = \begin{Bmatrix} (1-2\alpha).(i_x \cdot t_1 - i_y \cdot t_2) \pm i_z \cdot t_3, & \text{PF} = 1 \\ (1-2\alpha).(i_x \cdot t_1 + i_y \cdot t_2) \pm i_z \cdot t_3, & \text{PF} = 0 \\ (1-2\alpha).(-i_x \cdot t_1 + i_y \cdot t_2) \pm i_z \cdot t_3, & \text{PF} = \text{-}1 \end{Bmatrix} \quad (3.23)$$

Table 3.4 Current polarity dependency of the parameters α_1 and α_2.

$i_x(R) \geq 0$	$\alpha_1 = \alpha$
$i_x(R) < 0$	$\alpha_1 = 1\text{-}\alpha$
$i_y(R) \geq 0$	$\alpha_2 = 1\text{-}\alpha$
$i_y(R) < 0$	$\alpha_2 = \alpha$

For the above conditions and by selecting α_1 and α_2 as shown in Table 3.4, the neutral point current formula becomes as in (3.24).

$$i_{n\alpha o} = \frac{(1-2\alpha)\cdot\{\ |i_x(R)|\cdot t_1 + |i_y(R)|\cdot t_2\ \} + i_z(R)\cdot t_3}{T} \quad (3.24)$$

By using the (3.17) and (3.24) the average change of the neutral point potential over a PWM period (ΔV_n) can be calculated in the following.

$$\Delta V_n = \frac{1}{2C}(1-2\alpha)\cdot\{\ |i_x(R)|\cdot t_1 + |i_y(R)|\cdot t_2\ \} + \frac{1}{2C}\cdot i_z(R)\cdot t_3 \quad (3.25)$$

$$V_{n-new} = V_{n-old} + \Delta V_n \quad (3.26)$$

In order to decrease the $V_{n\text{-}old}$ error to zero in one PWM cycle (step) the optimal redundancy function α can be calculated by employing (3.27).

$$\alpha_{oo} = \frac{1}{2} - \frac{-2C\cdot V_{n-old} - i_z(R)\cdot t_3}{2\cdot\{|i_x(R)|\cdot t_1 + |i_y(R)|\cdot t_2\}} \quad (3.27)$$

The neutral point potential performance of the optimal α control method is illustrated in Figure 3.21 for various modulation index values and zero power factor. For average model simulations, the DC bus capacitor capacitance is 1000 μF, the load current is at 50 Hz and its rms value is equal to 7.1 A, and the initial value of the neutral point potential is equal to 30 V. In the figure for low modulation index values 0.2 and 0.4 the controller response is fast, because the available charge for neutral point potential error compensation is high enough to compensate the neutral point potential error in a short time period. In other words, coordinating α_1 and α_2 yields superior performance to the uniform α method. As seen from the figure, for $M_i > 0.8$, the controller response is slow for the same reason as in uniform α. The difference between the two methods is marginal. The optimal α controller response is slightly faster than the uniform α controller response as shown in Figure 3.21. The controller can not compensate triplen harmonic component on the neutral point potential in the high modulation index values, as shown in the Figure 3.21. The unity power factor operating performance of the optimal α method is better than the zero power factor operating performance as shown in Figure 3.22.

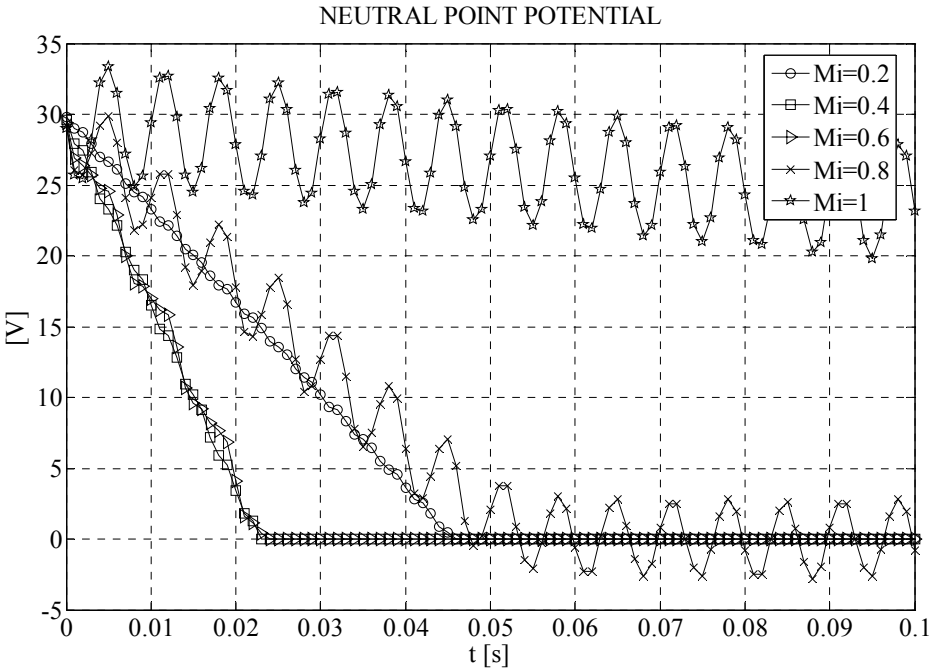


Figure 3.21 Neutral point potential control performance of the optimal α control method for various modulation index values and PF=0.0.

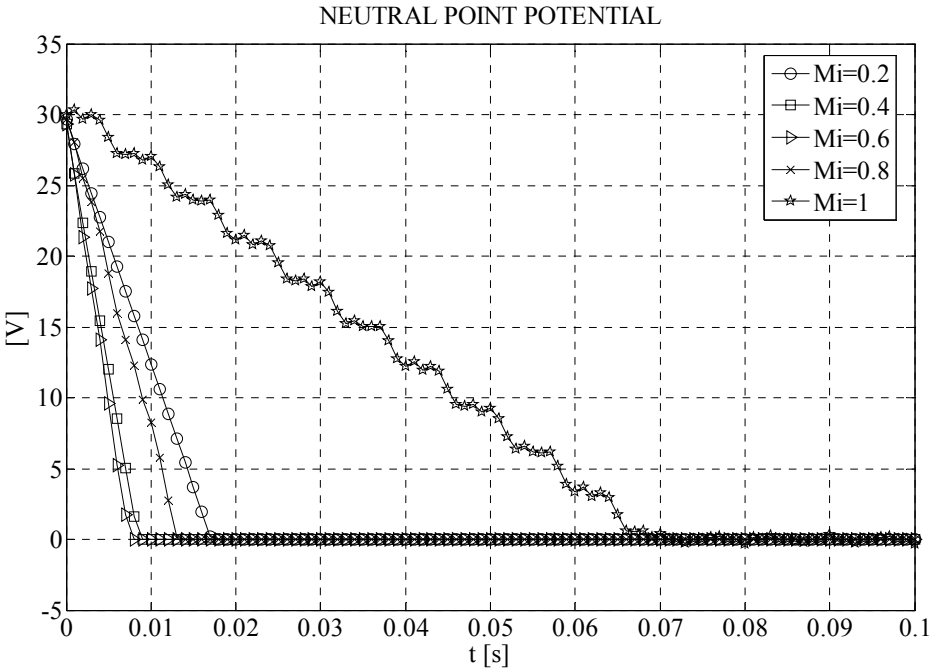


Figure 3.22 Neutral point potential control performance of the optimal α control method for various modulation index values and PF=1.0.

As this section and section 3.5.2.1 illustrated, the proposed two methods do not provide a complete cure to the high modulation index range operation neutral point potential performance problems. As was shown in a previous section in Figure 3.15.a, b, and c; the neutral point current has a dominant AC component. The frequency of this AC component is triple of the load current fundamental frequency. Under certain operating conditions, even with the utilization of the optimal redundancy function and the one step optimal formula of (3.27) the NTV-PWM technique can not completely eliminate the effect of the triplen harmonic current due to the medium voltage vector "c." As illustrated in detail in the above simulations, at high modulation index, the time length of the medium voltage vector "c" is larger than the smaller vectors and its effect on the neutral point potential is dominant over the effect of the small voltage vectors. All the charge available by the small voltage vectors may not compensate for the effect of the medium voltage vector. Thus, a requirement for techniques to overcome the neutral point potential drift or fluctuation under such conditions is necessary. In the following, a high performance method will be developed.

3.5.2.3 The Two-Parameter Space Vector PWM Method

In the NTV-PWM pulse pattern based approach with the control methods discussed in the previous sections, the only control variable is α and by means of appropriate partitioning of the small voltage vectors the neutral point potential is controlled. However, at high modulation index and under strong dynamics or imbalances, the correction capacity of the small redundant voltage vectors is quite limited. Especially near unity modulation index, the duty cycle of the small vectors and therefore their effect diminishes. Under such conditions the effect of the medium voltage vector becomes dominant in determining the neutral point potential. Therefore, removing the effect of the medium voltage vector must involve reduction or elimination of the duty cycle of the medium voltage vector.

In the literature, modulation methods that avoid the medium voltage vector "c" have been reported [6], [7]. However, total avoidance of the medium voltage vector is unnecessary both from the switching stress perspective and output voltage harmonic distortion perspective. Therefore, the amount (duty cycle) of the medium vector should be controlled in continuous manner rather than discrete (implying full or no use of the medium vector).

In this work, a method that adjusts duty cycle of the medium voltage vector "c" such that the neutral point potential is controlled and high output performance is maintained has been developed. The so called "two-parameter method" involves two control parameters. The first parameter is α and this parameter is same parameter as in the NTV-PWM method. The second parameter, γ is the effective duty ratio of the medium voltage vector "c." The effective duty ratio is the ratio of the utilized time to NTV-PWM computed time value of the medium voltage vector. The parameter γ is given by (3.28).

$$\gamma = \frac{t_c}{t_3} \tag{3.28}$$

$0 \le \gamma \le 1$

t_c : the actual (applied) time length of the medium voltage vector "c."

t_3 : the NTV-PWM computed time length of the medium voltage vector "c."

The difference between the NTV-PWM computed time length and the actual time length of the medium voltage vector (t_3-t_c) is the time that the medium vector will not be utilized. The required complex number volt-seconds in this case must be compensated by the two large (full) adjacent voltage vectors. Thus, during the remaining time, time length of the medium voltage vector "c" is distributed to the full voltage vectors "a" and "b" equally. This distribution is illustrated in Figure 3.23. Depending on the requirement for neutral point potential control, the effective duty ratio of the medium voltage vector γ can be adjusted from 0 to 1 corresponding to zero contribution and full contribution to the neutral point potential variation respectively. The distribution of the medium voltage vector "c" changes the time length formulas of the voltage vectors and it results in different formulas from the NTV-PWM. In Table 3.5 time lengths of the voltage vectors in a PWM period are given for the two-parameter space vector PWM method.

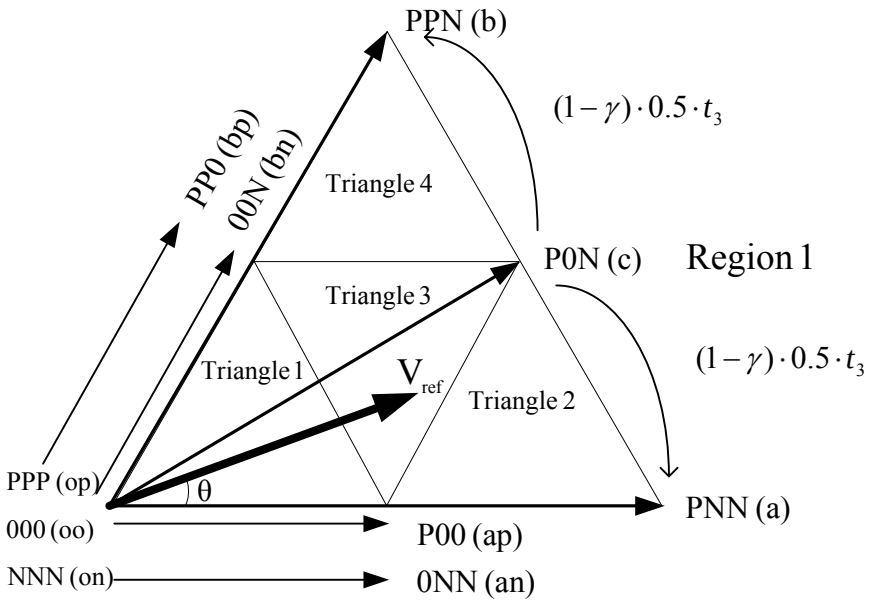


Figure 3.23 Illustration of the distribution of the remaining time of the medium voltage vector "c" to the full voltage vectors "a" and "b."

Table 3.5 The two-parameter space vector PWM method time length calculations

Region	Voltage vectors	Time length of NTV
Triangle 1	op, oo, on	$t_0=T\{1-2M_i\sin(\theta+\pi/3)\}$
	ap, an	$t_1=2M_iT\sin(\pi/3-\theta)$
	bp, bn	$t_2=2M_iT\sin(\theta)$
Triangle 2	ap, an	$t_1=2T\{1-M_i\sin(\theta+\pi/3)\}$
	c	$t_3=2M_iT\sin(\theta)$ $t_c=\gamma t_3$
	a	$t_4=T\{2M_i\sin(\pi/3-\theta)-1\}+0.5(1-\gamma)t_3$
	b	$t_5=0.5(1-\gamma)t_3$
Triangle 3	ap, an	$t_1=T\{1-2M_i\sin(\theta)\}$
	bp, bn	$t_2=T\{1-2M_i\sin(\pi/3-\theta)\}$
	c	$t_3=T\{2M_i\sin(\theta+\pi/3)-1\}$ $t_c=\gamma t_3$
	a	$t_4=0.5(1-\gamma)t_3$
	b	$t_5=0.5(1-\gamma)t_3$
Triangle 4	bp, bn	$t_2=2T\{1-M_i\sin(\theta+\pi/3)\}$
	c	$t_3=2M_iT\sin(\pi/3-\theta)$ $t_c=\gamma t_3$
	a	$t_4=0.5(1-\gamma)t_3$
	b	$t_5=T\{2M_i\sin(\theta)-1\}+0.5(1-\gamma)t_3$

In Figure 3.23, in triangle 1 (inner hexagon), the medium voltage vector “c” is not utilized, thus it has no effect on the neutral point potential and the γ parameter is not involved. In the remaining triangles γ appears as a control variable and is utilized to control the neutral point potential.

Since in the two-parameter PWM method in the outer triangles the additional full voltage vectors replace a portion of the medium voltage vector, the pulse pattern becomes different from the NTV-PWM pulse pattern. The pulse pattern of the NTV-PWM is not suitable for this modulation technique. For this modulation technique a new pulse pattern should be defined and this pulse pattern should allow the distribution of the medium voltage vector. The defined new pulse pattern is shown in Figure 3.24. This pulse pattern is more complex and the implementation needs more complex digital hardware than the NTV-PWM pulse pattern. In triangle 1 the pulse pattern is same as the NTV-PWM case. The pulse pattern is changed for other triangles. The minimum number of switching criteria and high quality waveform criteria are taken care into consideration when developing the new pulse pattern.

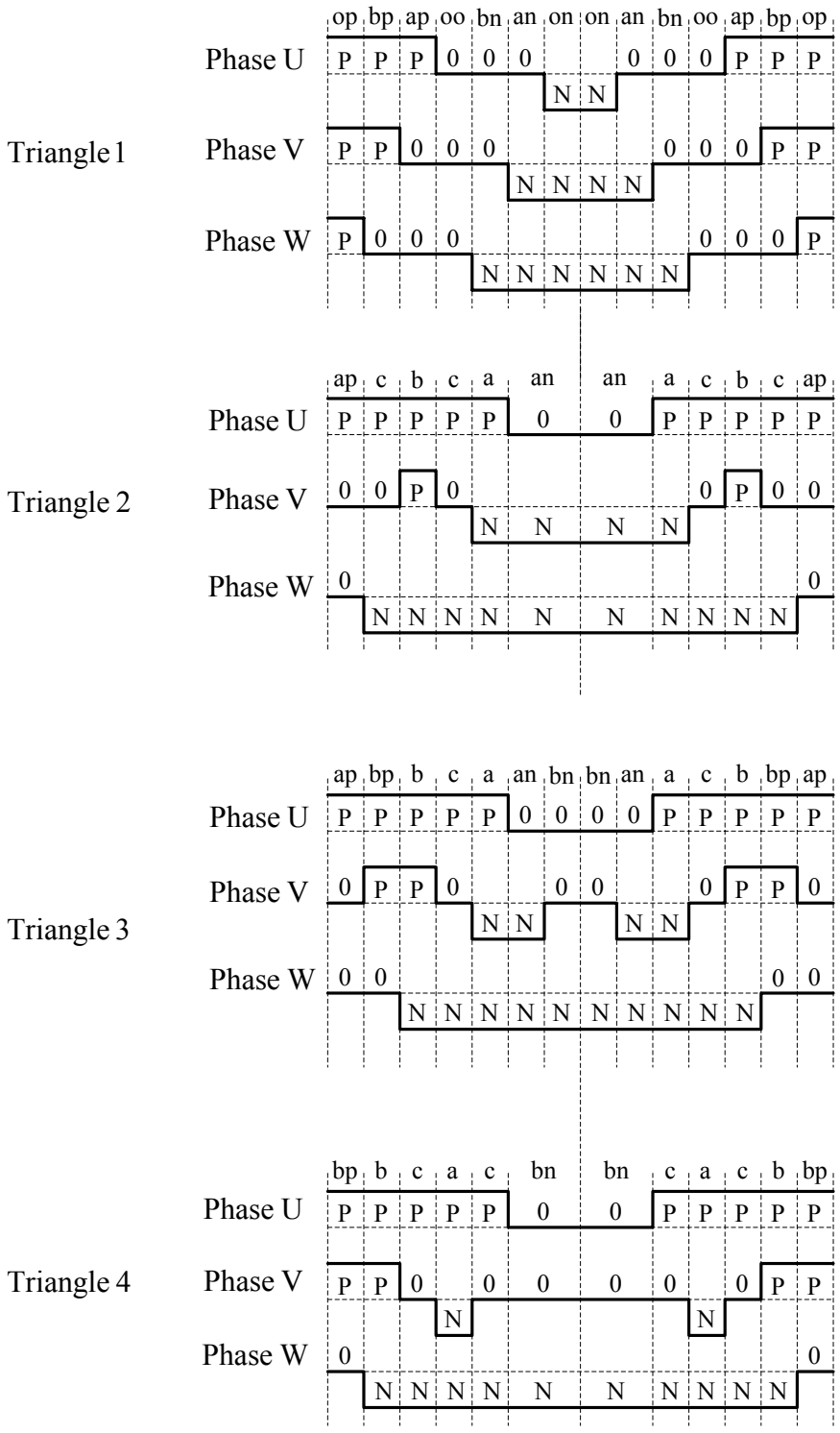


Figure 3.24 The pulse pattern of the two-parameter PWM method.

As an example, if the reference voltage vector is in triangle 3, the reference voltage vector is synthesized by the small voltage vectors “ap,” “an,” “bp,” “bn,” the medium voltage vector “c,” and the full voltage vectors “a” and “b.” If the parameter γ is

equal to zero (γ=0), the medium voltage vector "c" is not utilized to synthesize the reference voltage vector. If the parameter γ is equal to one (γ =1), the full voltage vectors "a" and "b" are not used to synthesize to the reference voltage vector and it is same as the NTV-PWM. The duty cycles of the semiconductor switches of one inverter leg for various γ values are shown in Figure 3.25.

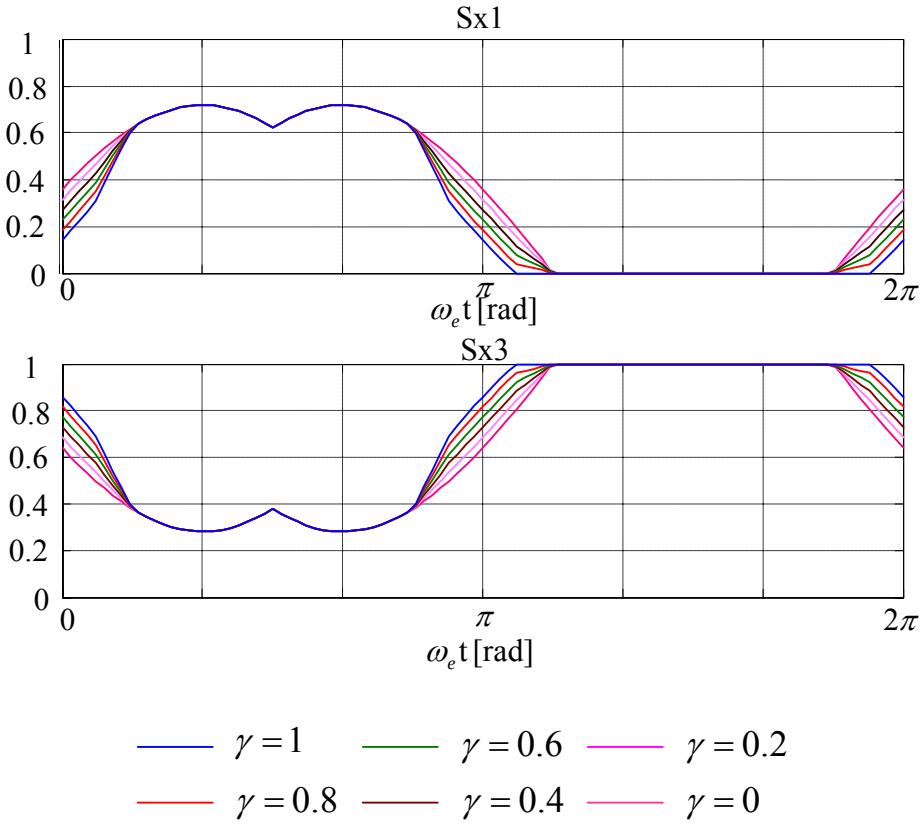


Figure 3.25 Duty cycles of the semiconductor switches of one inverter leg as a function of γ (M_i=0.8).

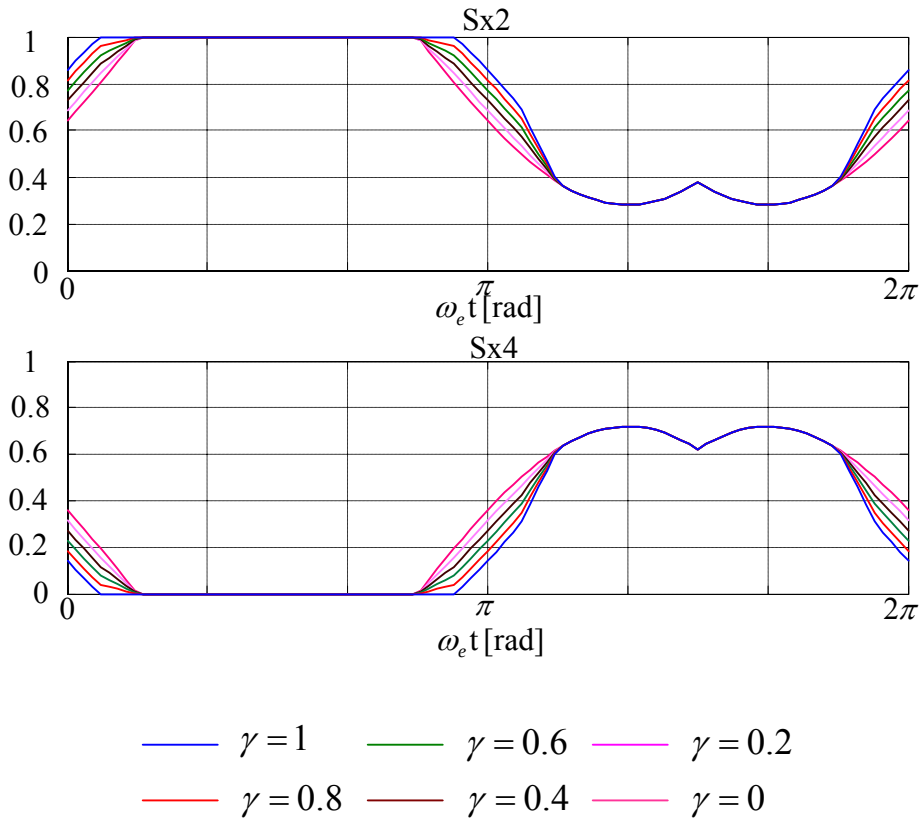


Figure 3.25 Duty cycles of the switches of one inverter leg as a function of γ (M_i=0.8).

As seen in the Figure 3.25, when the reference voltage of the associated phase is the most positive or the most negative, the duty cycles of the semiconductor switches are the same (not affected) for all values of γ. However, when the reference voltage of the related phase is between the most positive phase and the most negative phase, the parameter γ has influence on the duty cycles of the semiconductor switches of the associated phase.

3.5.2.3.1 Neutral Point Potential Analysis of The Two-Parameter PWM Method

In the two-parameter PWM method, the duty cycles of the small voltage vectors are controlled by using the same strategy as in the NTV-PWM. The difference in this modulation technique is that the duty cycle of the medium voltage vector "c" is controlled according to the neutral point potential value. Depending on the charge requirements for neutral point potential control, the medium voltage vector duty

cycle may be reduced and the adjacent state full voltage vectors are utilized additionally. The full vectors are utilized with appropriate duty cycle and sequence to compensate for the missing volt-seconds (due to reduction of medium voltage vector duty cycle). For this modulation technique, $\gamma \cdot t_3$ is written instead of t_3 in (3.15) to obtain the average neutral point current over a PWM period in the following.

$$i_n = \frac{i_x(R)\cdot(t_{an}-t_{ap}) + i_y(R)\cdot(t_{bp}-t_{bn}) + \gamma\cdot i_z(R)\cdot t_3}{T} \tag{3.29}$$

By employing the optimal α control method, the average neutral point current over a PWM period is given by

$$i_n = \frac{(1-2\alpha)\cdot\{\ |i_x(R)|\cdot t_1 + |i_y(R)|\cdot t_2\ \} + i_z(R)\cdot\gamma\cdot t_3}{T} \tag{3.30}$$

Where $i_x(R)$, $i_y(R)$, and $i_z(R)$ are the phase current functions given in Table 3.3, α_1 and α_2 are the same parameters as the NTV-PWM. t_1 and t_2 are the time lengths of the small voltage vectors, and t_3 is the NTV-PWM computed time length of the medium voltage vector.

As shown in the following, the average neutral point potential change over a PWM period (ΔV_n) equation is changed compared to the second term of (3.25).

$$\Delta V_n = \frac{1}{2C}(1-2\alpha)\cdot\{\ |i_x(R)|\cdot t_1 + |i_y(R)|\cdot t_2\ \} + \frac{1}{2C}\cdot i_z(R)\cdot\gamma\cdot t_3 \tag{3.31}$$

To illustrate the effect of γ on the neutral point potential lets consider the following example. In (3.30), if α=0.5, and γ=0, the average neutral point current over a PWM period is zero. Both the α terms and the γ terms are individually zero. Keeping the α same (0.5) and increasing the γ term, the average neutral point current becomes non-zero. In the following, the effect of the γ parameter is illustrated by means of an example. Equation (3.30) and (3.31) are calculated and plotted for various γ values. In this example, the conditions are PF=0.9, M_i=0.72, α=0.5, the load current is

sinusoidal (50 Hz) and has an rms value of 7.1 A. The variation of the neutral point potential and current is shown for various γ in Figure 3.26. The largest fluctuation of the neutral point potential is observed for γ=1. In this case, the medium voltage vector is used throughout the NTV-PWM computed time and it is not partitioned with the full voltage vectors. The magnitudes of the triplen harmonic neutral point voltage and current components decrease when the value of γ decreases as shown in Figure 3.26. When the γ parameter is equal to zero, the average neutral point current and therefore the neutral point potential change is zero.

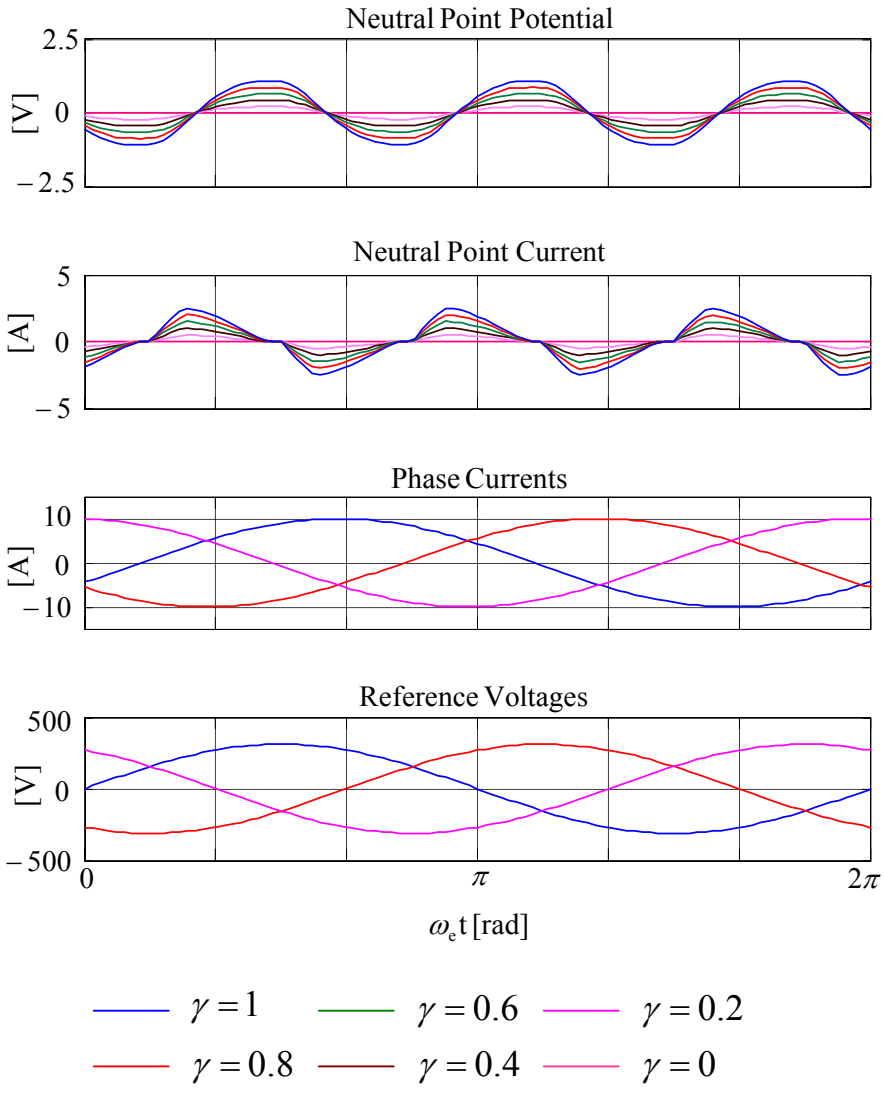


Figure 3.26 The neutral point current and potential waveforms at steady-state (I=7.1A, PF=0.9, M_i=0.72 and α=0.5).

The per-PWM-cycle average neutral point current and neutral point potential change depend on the load current magnitude, the load power factor and modulation index. When the modulation index increases, the time length of the medium voltage vector "c" also increases. The load is connected to the neutral point for longer time duration and the magnitude of neutral point current increases. The modulation index dependency of the neutral point potential is shown in Figure 3.27 for α=0.5. In Figure 3.27 the peak value of the neutral point potential is zero until the modulation index is equal to 0.5 because the medium voltage vector is not utilized in triangle 1. The maximum variation is observed when M_i=1.0. Because for M_i=1.0, the time length of t_3 dominates and large amount of charge is injected to/from the neutral point.

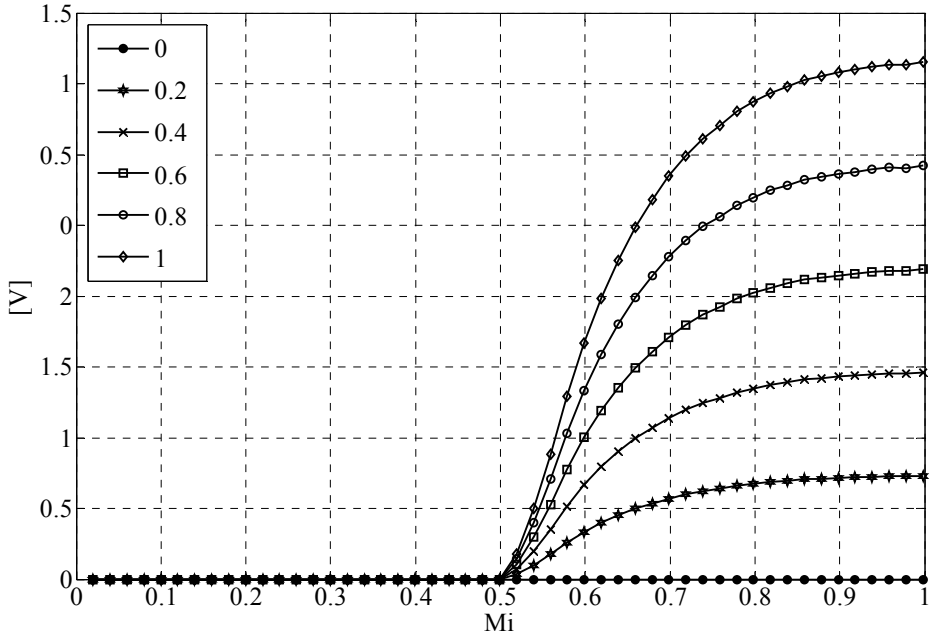


Figure 3.27 The neutral point potential peak value as a function of M_i for γ as parameter (I=7.1A, PF=0.9 and α=0.5).

The load power factor has strong influence on the neutral point current and potential. If the load has a low power factor, the magnitude of the neutral point current becomes large. Figure 3.28 shows the variation of the maximum value of the neutral point potential fluctuation as a function of power factor. The neutral point potential

fluctuation is zero for γ=0. The maximum value of the neutral point potential fluctuation is observed for PF=0 and γ=1.

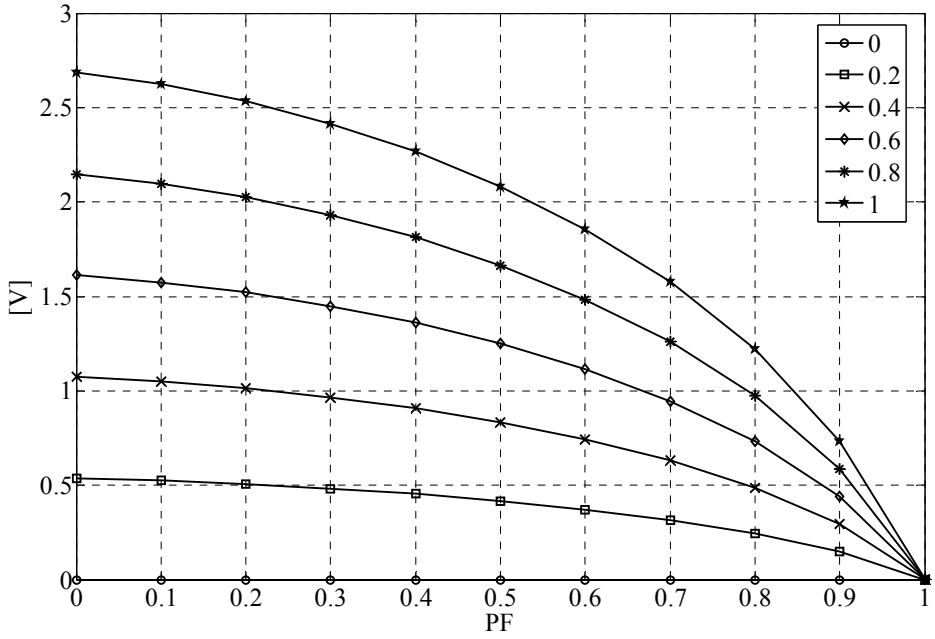
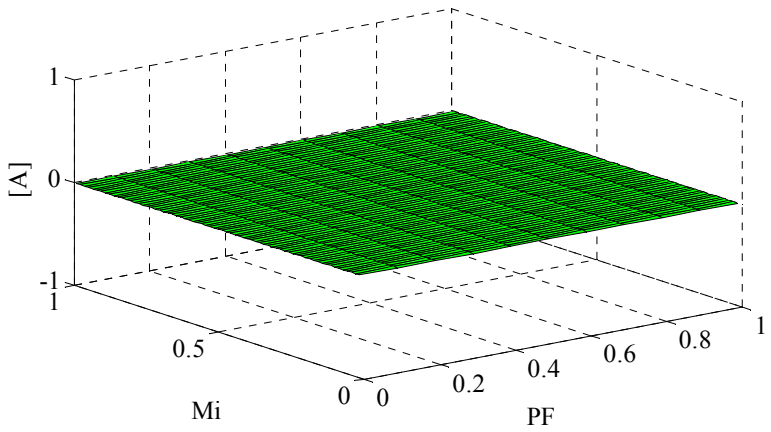
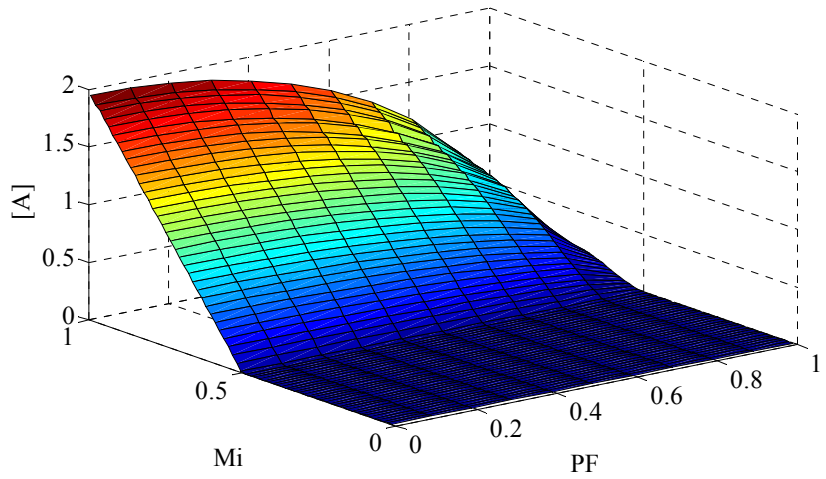


Figure 3.28 The neutral point potential peak value as a function of the power factor for γ as parameter (I=7.1A, M_i=0.72 and α=0.5).

Figure 3.29 shows the variation of $i_{n\text{-}peak}$=f(M_i, PF) characteristics in three dimensional plots for α=0.5 and various γ values. The load current is sinusoidal and has an rms value of 7.1 A. The neutral point current has a waveform that consists of the triplen harmonics of the load fundamental component. Its peak value determines the neutral point potential. Therefore the neutral point current peak value is of interest. For γ =0, the neutral point current peak value is equal to zero for all PF and M_i values. This means that the neutral point current is independent from the power factor and modulation index for γ=0. This is shown in Figure 3.29.a. The largest neutral point current peak value is observed in Figure 3.29.f when PF=0 and M_i=1.0 for γ=1. In Figure 3.29.a to Figure 3.29.f, it can be seen that the neutral point current peak value decreases with the power factor and increases with the modulation index and γ.



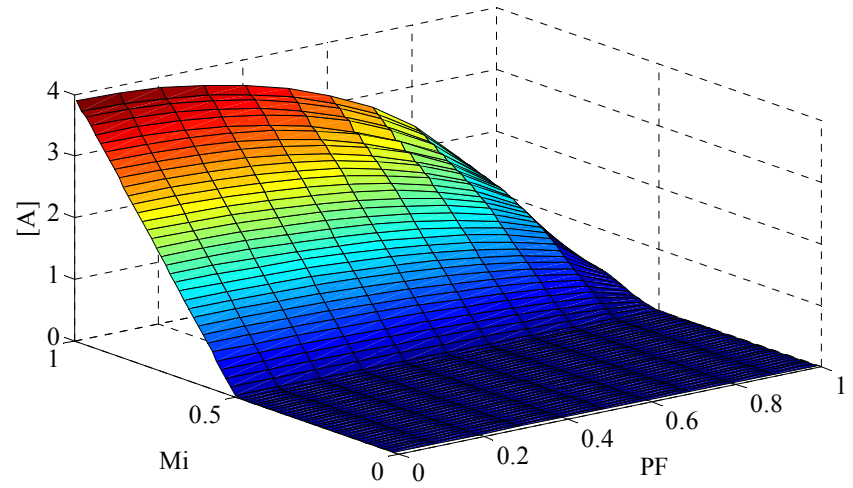
(a) γ=0



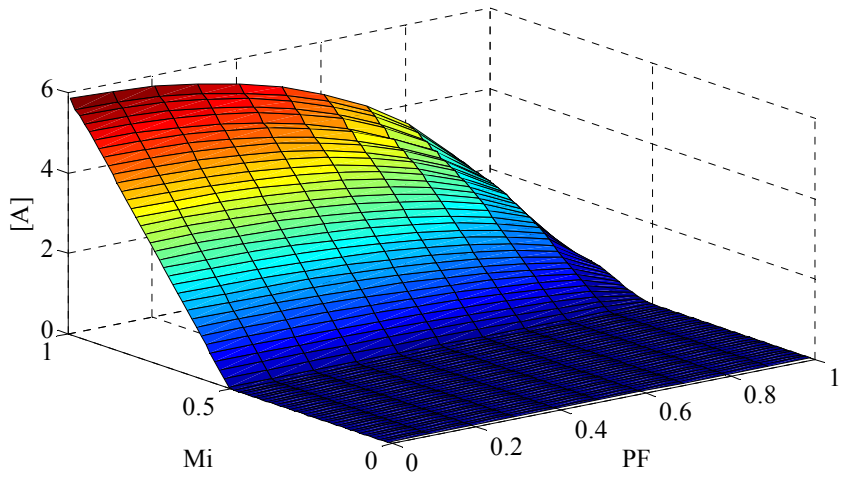
(b) γ =0.2

➔

Figure 3.29 The neutral point current peak value as a function of M_i and PF (I=7.1 A and α=0.5).



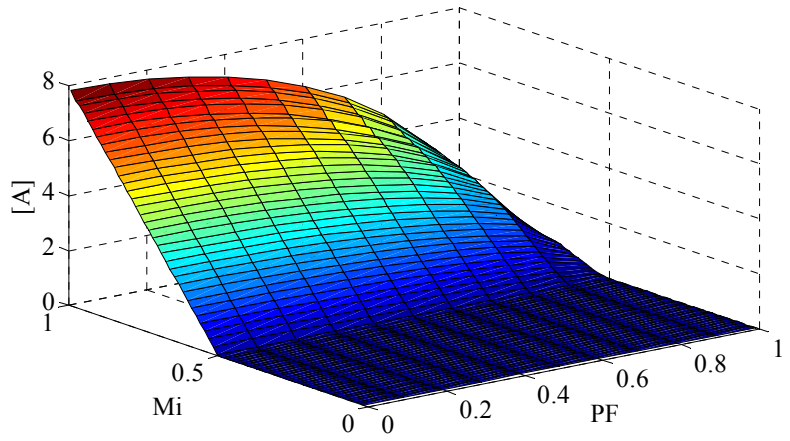
(c) γ =0.4



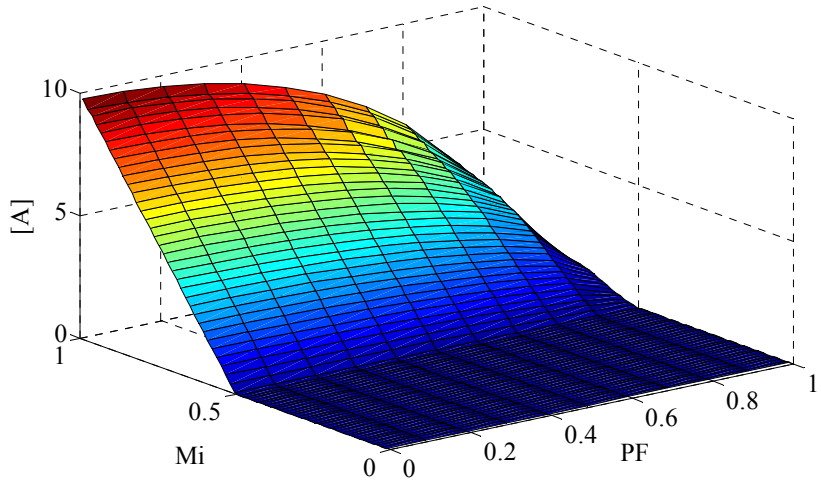
(d) γ =0.6

➔

Figure 3.29 The neutral point current peak value as a function of M_i and PF (I=7.1 A and α=0.5).



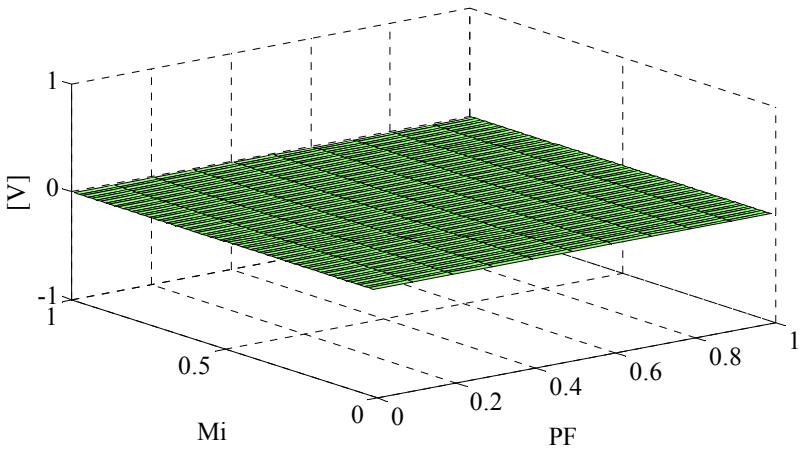
(e) γ =0.8



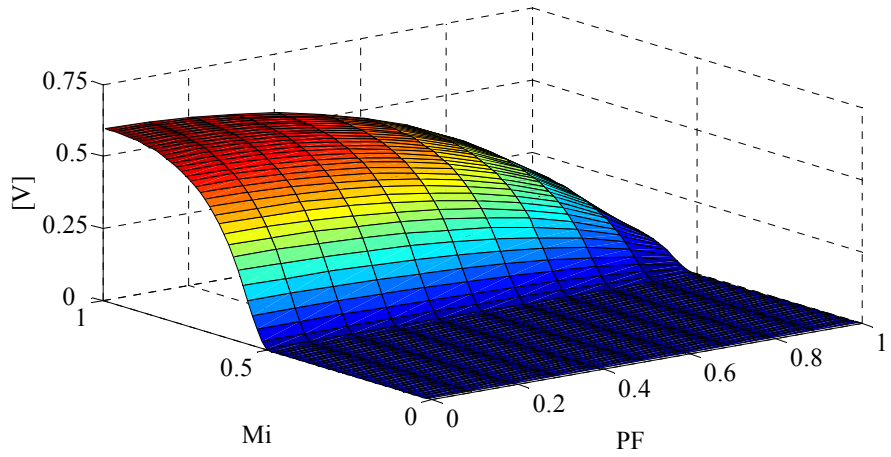
(f) γ =1.0

Figure 3.29 The neutral point current peak value as a function of M_i and PF (I=7.1 A and α=0.5).

Figure 3.30 shows the neutral point potential peak value as a function of the power factor and modulation index for various γ values. Since the neutral point current consists of the load current triplen harmonics, the neutral point potential (which is proportional to the integral of the neutral point current) also has the same waveform type. Therefore, the peak value of the neutral point potential is the key performance parameter and it will be discussed accordingly. The fluctuation of the neutral point potential is zero for $\gamma = 0$ for all M_i and PF values. It is same as the associated neutral point current situation. When the neutral point current is zero, the neutral point potential change must be zero. The largest magnitude of the neutral point potential is observed in Figure 3.30.f for PF=0, M_i=1.0, $\gamma = 1$. In Figure 3.30.a to Figure 3.30.f it can be seen that the magnitude of the neutral point potential fluctuation decreases with the power factor and increases with the modulation index and γ.



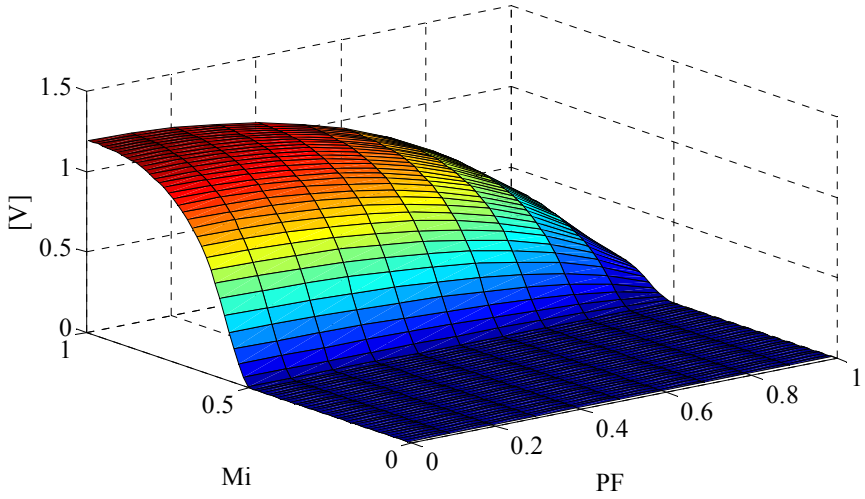
(a) γ =0



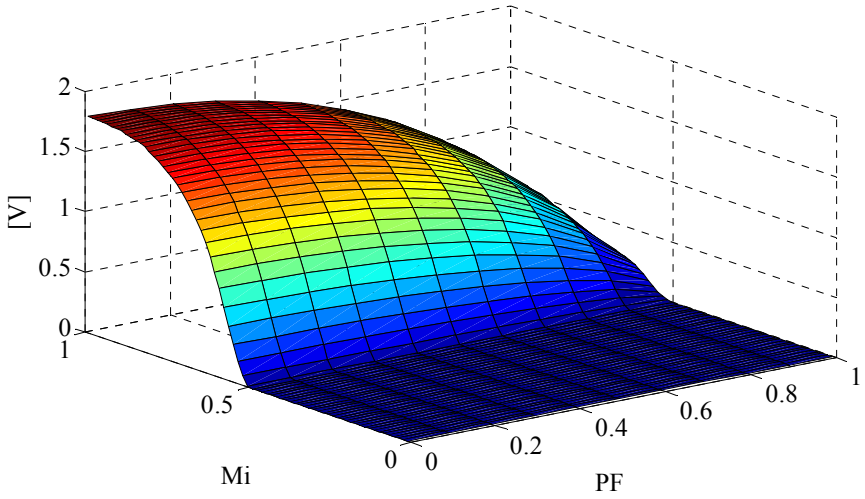
(b) γ =0.2

➔

Figure 3.30 The neutral point potential peak value as a function of M_i and PF (I=7.1 A and α=0.5).



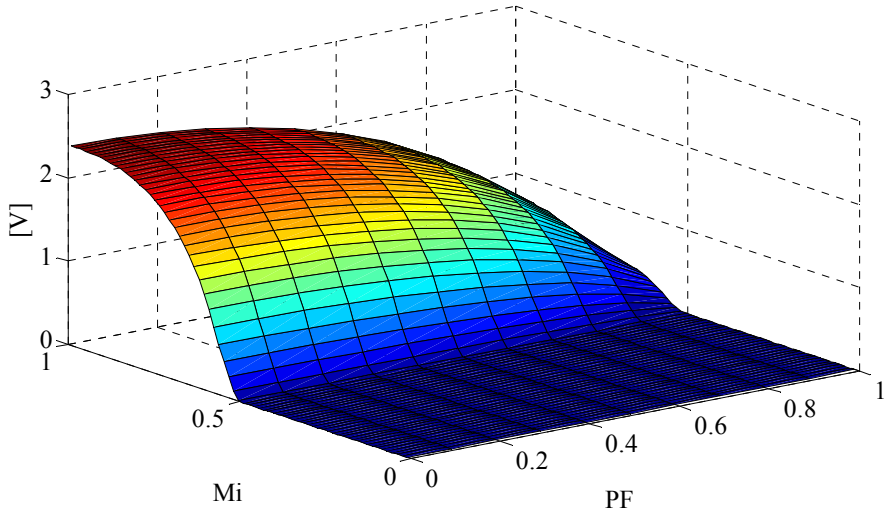
(c) γ =0.4



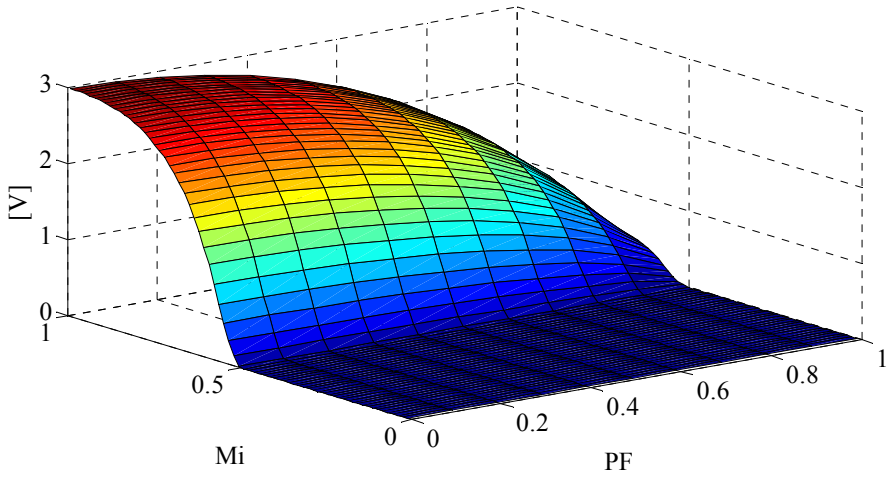
(d) γ =0.6

➔

Figure 3.30 The neutral point potential peak value as a function of M_i and PF (I=7.1 A and α=0.5).



(e) γ =0.8



(f) γ =1.0

Figure 3.30 The neutral point potential peak value as a function of M_i and PF (I=7.1 A and α=0.5).

3.5.2.3.2 Neutral Point Potential Control of The Two-Parameter PWM Method

As shown in the analytical results of the previous section, the neutral point potential is a function of α and γ and it becomes obvious that by selecting proper α and γ, the neutral point potential can be controlled as desired. The α parameter may be used in the same manner as in the NTV-PWM method. The optimal charge range control method defined by (3.27) can be utilized at no cost (in terms of switching count, switching stress and harmonic performance). However, the method must be used with modifications. If the medium voltage vector current i_z(R) is in the direction that forces the neutral point potential error to decrease, the i_z(R) current component is useful and may be retained. However, the medium voltage vector may charge the neutral point potential in opposite direction (more than enough charge may be injected by the medium voltage vector to the neutral point). If the polarities of V_{no} and i_z(R) are the same, the medium voltage vector influences the neutral in the unwanted direction (forces the neutral point potential to deviate from zero). In both cases, the α parameter can be utilized as a corrective measure but may or may not be sufficient to eliminate the neutral point potential error. First, it can be assumed that the medium voltage vector duty cycle is unchanged (γ=1) and the optimal α parameter is calculated according to the following equation.

$$\alpha_{oo} = \frac{1}{2} - \frac{-2C \cdot V_{n-old} - i_z(R) \cdot \gamma \cdot t_3}{2 \cdot \{|i_x(R)| \cdot t_1 + |i_y(R)| \cdot t_2\}} \Bigg| \gamma = 1 \tag{3.32}$$

In (3.32), if the result is a feasible α ($0 \leq \alpha \leq 1$), the result indicates that the neutral point potential error can be reduced to zero at the end of the PWM cycle. This implies that γ=1 can be retained and no further computation is required. The pulses can be programmed as NTV-PWM. However, if α is outside the feasible limits (α<0 or α >1), the neutral error potential can not be reduced to zero in one cycle. This result implies that γ should be less than one. In this case, α is held at the boundary value (for α<0, the new parameter should be α=0, and for α >1, the new parameter should be α=1). As a result the maximum available charge from the small vectors is fully utilized. However, this is not sufficient to compensate for the neutral point

potential error to become zero. As a result, the duty cycle of the medium voltage vector should be decreased. The γ parameter is calculated from (3.31) by employing (3.33).

$$\gamma_o = \frac{-2C \cdot V_{n-old} - (1-2\alpha) \cdot \{\ |i_x(R)| \cdot t_1 + |i_y(R)| \cdot t_2\ \}}{i_z(R) \cdot t_3} \Bigg|_{\alpha_o=0 \ \ or \ \ \alpha_o=1} \tag{3.33}$$

$$0 \le \gamma_o \le 1 \tag{3.34}$$

As seen from above equations if the small voltage vectors are able to compensate for all the neutral point potential error, γ is equal to one and the medium voltage vector is utilized for full computed time. At high modulation index and low power factor cases (large fluctuation on the neutral point potential), both α and γ are employed to control the neutral point potential. In this case, α may have zero or one value, and γ is between zero and one value.

The neutral point potential performance of the two-parameter PWM method with optimal α-γ control is illustrated in Figure 3.31 for various modulation index values and PF=0. For average model simulations, the DC bus capacitor capacitance is 1000 μF, PF=0, the load current rms value is equal to 7.1 A, and the initial value of the neutral point potential is equal to 30 V. In the figure for low modulation index values 0.2 and 0.4 the controller response is same as the optimal α controller response, because for lower modulation index values the medium voltage vector is not utilized and the redundancy functions of the small voltage vectors are selected by employing the optimal α control method. As seen from the figure, even for $M_i > 0.8$, the controller response is faster than the uniform and optimal α controller response. As seen from Figure 3.31 the controller eliminates triplen harmonic component on the neutral point potential in the high modulation index values. As a result the two-parameter PWM method with optimal α-γ control has superior performance over the full modulation range. The unity power factor operating performance of the two-parameter PWM method with optimal α-γ control is better than the zero power factor operating performance as shown in Figure 3.32.

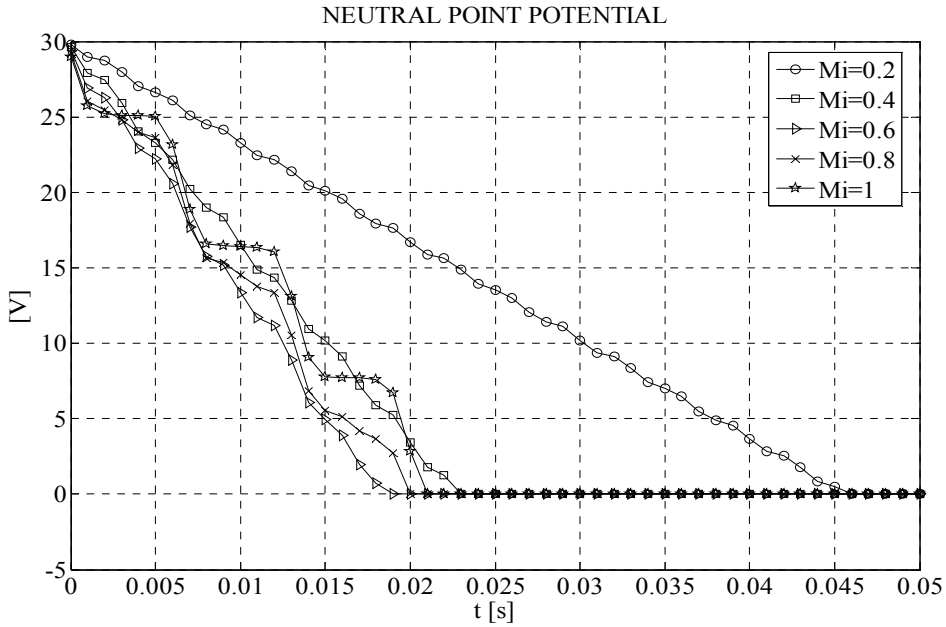


Figure 3.31 Neutral point potential control performance of two-parameter PWM method with the optimal α-γ control method for various M_i and PF=0.0.

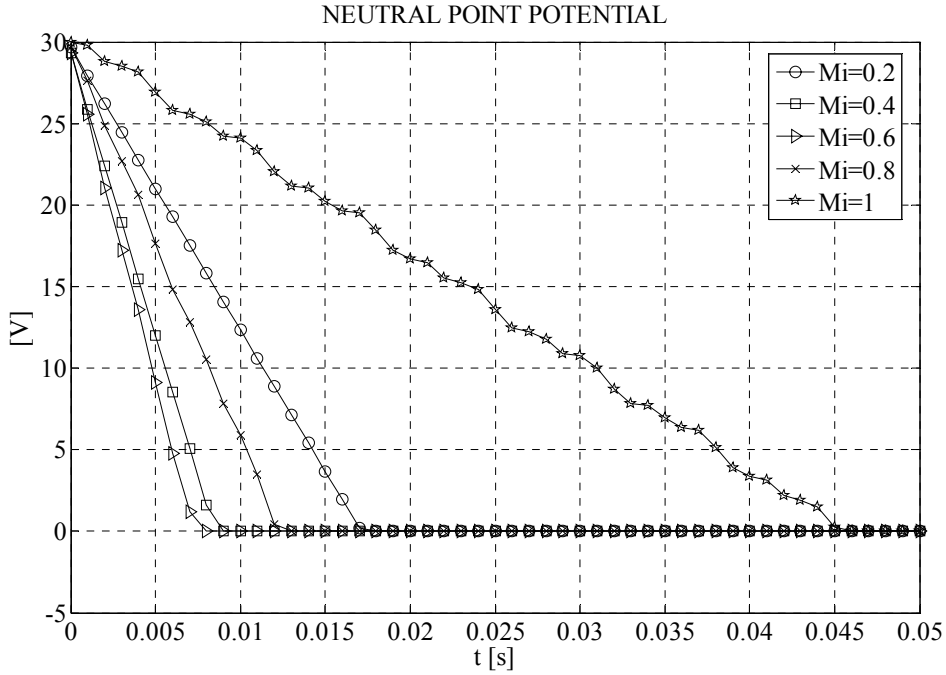


Figure 3.32 Neutral point potential control performance of the two-parameter PWM method with the optimal α-γ control method for various M_i and PF=1.0.

3.6 Performance Comparison of Pulse Pattern Modification Based Neutral Point Potential Balancing Methods

The pulse pattern modification based neutral point potential control techniques are comparatively evaluated in this section. The steady-state and dynamic performance of the three methods are compared qualitatively in Table 3.6. The table illustrates the superiority of the two-parameter PWM with optimal α-γ control method. The dynamic response of the optimal α method is thrice faster than the uniform α control method in the low modulation index range (internal hexagon). The two-parameter control method utilizes the control method of the optimal α control method inside the internal hexagon. Therefore, it performs equally. In the high modulation index range (outside the internal hexagon) the dynamic response of the two-parameter PWM with optimal α-γ control method is twice faster than that of the optimal α control method.

The steady-state performance of the uniform α control method results in large neutral point voltage ripple at high modulation index values associated with the external triangles. The optimal α control method performs better than the uniform α control method until the modulation index reaches the linearity limit of one. Then the effect of the medium voltage vector dominates and the ripple becomes large. The two-parameter PWM with optimal α-γ control method provides superior steady-state performance overall the operating range. The effect of the medium voltage vector can be reduced or totally eliminated depending on the limit value of the γ parameter.

The above analysis and simplified computer simulation results of the last section shows that the proposed two-parameter PWM with optimal α-γ control method has better neutral point potential performance than the other methods. The following chapter provides detailed system simulations that verify the overall performance of the two-parameter PWM with optimal α-γ control method.

Table 3.6 Performance comparison of the neutral point potential balancing methods for PF=0 as the worst case operating point

Method	Transient Response		Steady-state Response	
	$M_i < 0.5$	$M_i > 0.5$	$M_i < 0.5$	$M_i > 0.5$
Uniform α	Average	Poor	Average	Poor
Optimal α	Optimal	Poor	Optimal	Poor
Optimal α - γ	Optimal	Optimal	Optimal	Optimal

CHAPTER 4

THREE-LEVEL NPC INVERTER NEUTRAL POINT POTENTIAL CONTROL PERFORMANCE STUDY BY MEANS OF COMPUTER SIMULATIONS

4.1 Introduction

In this chapter, the three-level NPC inverter neutral point potential drift/fluctuation is investigated, and the performance of the neutral point potential control methods discussed in the previous chapter is verified by means of detailed computer simulations.

First, a three-phase current sink type load is simulated for various power factor and modulation index values. As in the previous chapter, the fall time of an initial neutral point potential error is investigated and the dynamic performance of the controller is illustrated. This study is conducted in order to verify the accuracy of the average model and the performance of the neutral point potential control theory developed in the previous chapter.

Second, detailed simulations for a three-phase R-L type load are conducted. The neutral point potential drift/fluctuation of the three-level NPC inverter driven a three-phase R-L load is studied for various operating conditions (modulation indices). Following the illustration of the neutral point potential drift/fluctuation problem by means of simulations, the established and the newly proposed neutral point potential control methods are considered. The neutral point potential control methods are simulated and their performance is evaluated and a comparison is provided.

Third, the neutral point potential drift/fluctuation of the three-level NPC inverter driven induction motor feeding a fan load is studied for various operating conditions. The neutral point potential drift/fluctuation is illustrated via the simulation waveforms. An induction motor drive that feeds a fan load is simulated at various load and speed levels. For the motor drive, the neutral point potential behavior is also investigated under dynamic loading conditions. Following the illustration of the neutral point potential drift/fluctuation problem, the established and the newly proposed neutral point potential control methods are considered. The neutral point potential control methods are simulated and their performance is evaluated and a comparison is provided.

Finally, the chapter concludes with the comparative evaluation of various control methods and leads to the experimental studies of the following chapter.

4.2 Inverter Drive Modeling

For the purpose of modeling, a computer simulation package program, Ansoft-Simplorer has been utilized [22]. The program is a graphic window based (pick and place) power electronic circuit simulator. The program involves a circuit schematic diagram, a graphic view window, and the Day-postprocessor window. In the schematic window, the circuit is drawn via pick and place, the control blocks are created, and simulation parameters are assigned. The graphic window has the properties of an oscilloscope which displays the simulation results (voltage, current, etc. waveforms).

In the computer simulation, the trapezoidal integration method is utilized. Figure 4.1 shows the window that illustrates the selected integration method, minimum step size, and maximum step size in the simulation. The maximum and minimum step sizes are selected to minimize the computational errors and obtain high accuracy in the simulations without excessive data storage and computational burden. Since the PWM frequency is 5 kHz (200 μs), in order to account for the narrow voltage pulses, the minimum integration size is selected as 200 ns (1/1000 of the PWM cycle).

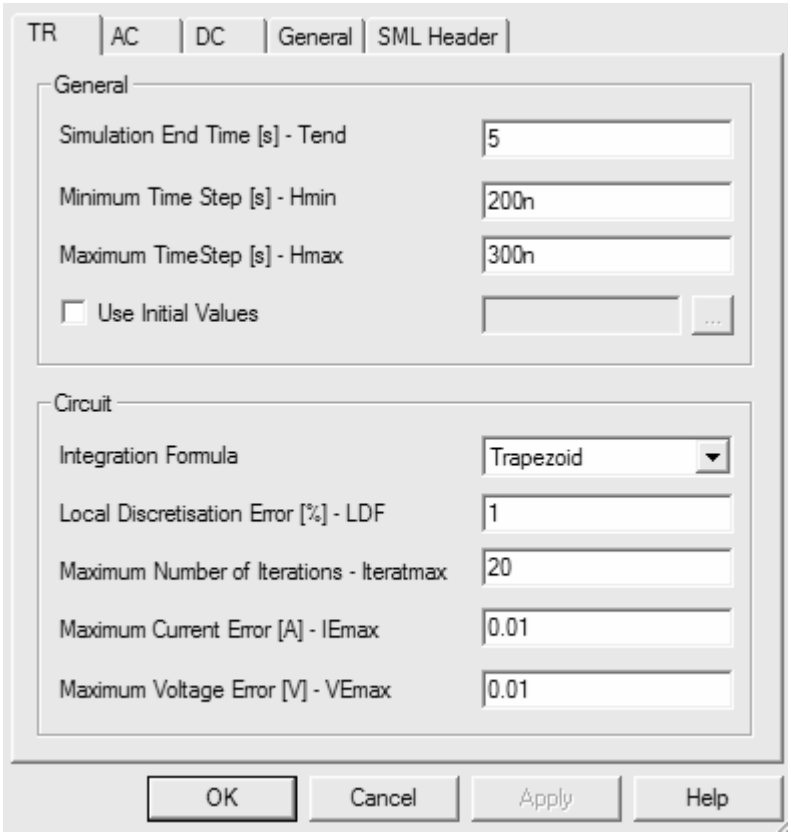


Figure 4.1 Simulator parameters and integration method.

The circuit simulator is based on a modified nodal approach. The trapezoidal algorithm is applied for the solution of the differential equation system. The solution of nonlinear equations is obtained by using the Newton-Raphson method. The calculation of the equation systems, linearization in the operating point, takes place by means of LU factorization after applying the Gauss method [22].

In all the simulations used in this chapter, the utility grid is modeled as a three-phase Y-connected AC voltage source with an internal impedance. The 50 Hz source line-to-line voltage rms value is 380 V. The equivalent internal resistance is 20 mΩ and the equivalent internal inductance is 100 μH per-phase. The inverter drive is of the three-phase full-bridge diode rectifier front-end type. Thus, it draws nonsinusoidal currents from the AC grid. An additional 3 mH three-phase AC line reactor is inserted in series with the AC line such that the power quality is improved. The computer simulation model is shown in Figure 4.2. This model is built in Ansoft-

Simplorer Schematic window as an "ssh" file. The series inductance shown in the simulation diagram represents the total line reactance and the filter reactance. The DC bus of the three-level NPC inverter system consists of two series connected capacitors. Each capacitor has 1000 μF capacitance value and capacitors are assumed ideal.

In both the diode-rectifier and the three-level NPC inverter, in the simulation "system level devices" are utilized in establishing the simulation model. In the system level model, the switch model involves a simple switch with a pair of series and parallel resistors. Thus, the semiconductor device switching dynamics are not modeled. The parameters of the system level switching device models are given in Table 4.1. Throughout the simulations, the switching frequency (f_{PWM}) is selected as 5 kHz corresponding to 200 μs PWM period.

Table 4.1 System level semiconductor device model parameters

Device	Forward voltage (V)	Bulk resistance (Ω)	Blocking resistance (Ω)
Diode	0.7	0.000001	1000000
IGBT	1.5	0.001	100000

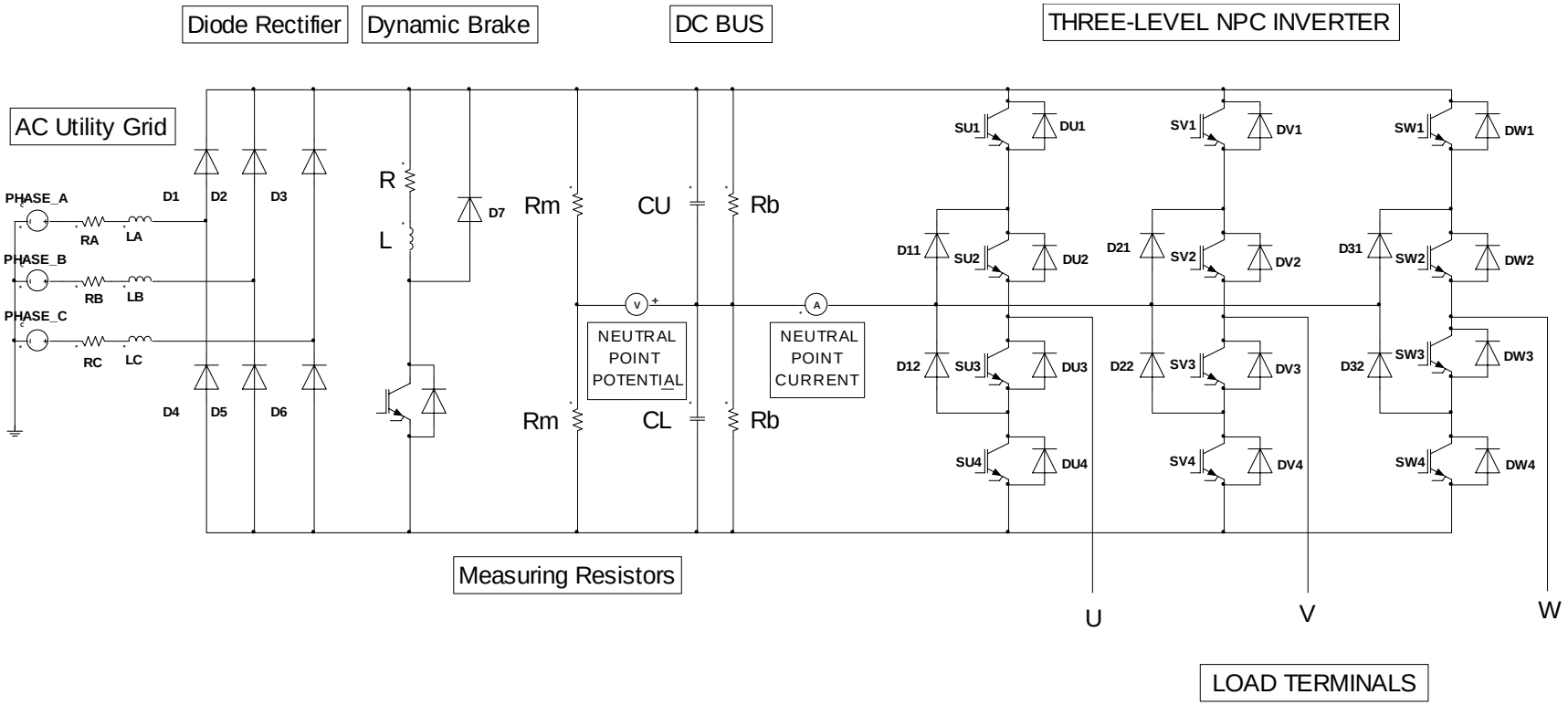


Figure 4.2 Three-level NPC inverter drive system simulation model circuit diagram (Simplorer V7.0 Schematic ssh file).

4.3 Current Sink Type Load Simulations

In this section, a three-phase Y-connected current sink type load is simulated for various power factor and modulation index values. This study is conducted in order to verify the accuracy of the average model and performance of the neutral point potential control theory developed in the previous chapter. The fundamental frequency of the current sink is 50 Hz and the rms values of the phase currents are 7.1 A. As in the previous chapter, the fall time of an initial neutral point potential error of 30 V is investigated and the dynamic performance of the controller is illustrated. The circuit parameters and the operating conditions are exactly same as those in the previous chapter.

First, the NTV-PWM method with uniform α control results are provided. Second, the NTV-PWM with optimal α control results are illustrated. Third, the two-parameter PWM with α-γ control method results are presented. Finally, the three methods are compared and also correlation with the average model simulations of the previous chapter is provided.

4.3.1 NTV-PWM with The Uniform α Control Method

This section presents the simulation results of the NTV-PWM with uniform α control method ($\alpha=\alpha_1=\alpha_2$ and $\gamma=1$) for various operating conditions. In Figure 4.3, the neutral point potential control performance of the uniform α control method is illustrated for various M_i and PF=0.0. The time from 30 V neutral point potential error to zero is investigated. As seen from Figure 4.3, for M_i values of 0.2 and 0.4, the controller response is slow. However, the controller response is faster than the average model simulation case (Figure 3.19). The reason is that in the average model simulation, the inverter is modeled as a loss-less block. In the detailed computer simulation case, the inverter model includes losses due to semiconductor switch forward voltage drop, internal resistance, i.e. The inverter losses create a damping effect on the neutral point potential which is similar to that of the balancing resistors. For $M_i=0.6$ and $M_i=0.8$, the controller response is faster than the lower M_i cases. At $M_i=1.0$, the

controller response is also slow, because the medium voltage vector is dominant over the small voltage vectors. The triplen harmonic voltage appears on the neutral point potential at high modulation index values ($M_i > 0.5$).

For the unity power factor operating condition, as illustrated in Figure 4.4, the performance of the uniform α control method is satisfactory and the results obtained are approximately the same as those in Figure 3.20.

In the system simulations, the numerical results obtained by the full system simulation via the Ansoft-Simplorer software package were stored in a data file and the numerical data was transferred to MATLAB. The graphic tools of MATLAB were utilized to overlay and plot the neutral point potential waveforms of both Figure 4.3 and Figure 4.4. This approach is followed in all the current sink model based simulations of Section 4.3 due to the limited graphic tool capability of Ansoft-Simplorer software package. The graphic window of Ansoft-Simplorer can not overlay different simulation results.

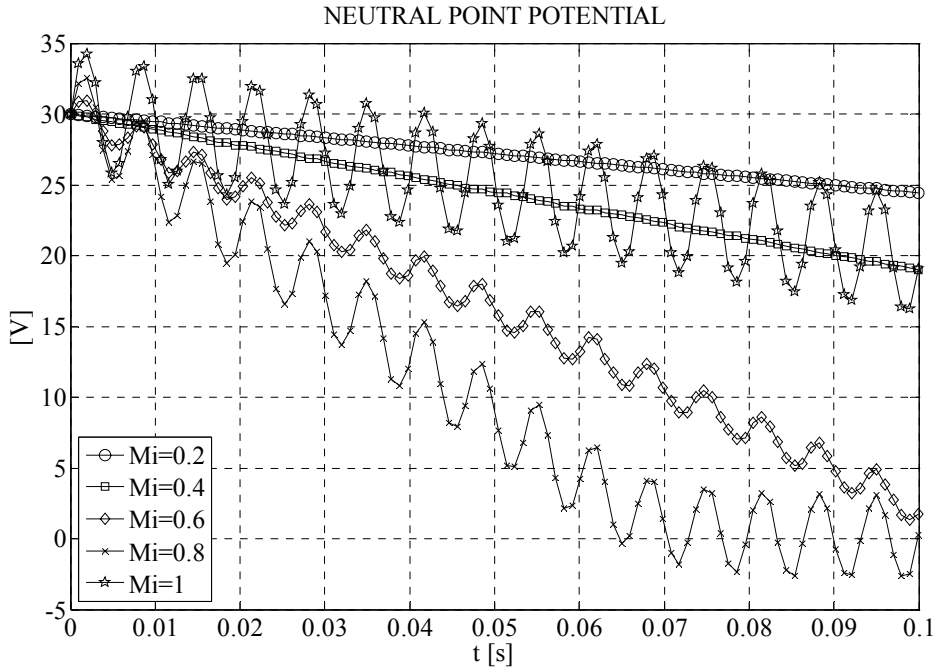


Figure 4.3 Neutral point potential control performance of the uniform α control method for various modulation indices and PF=0.0.

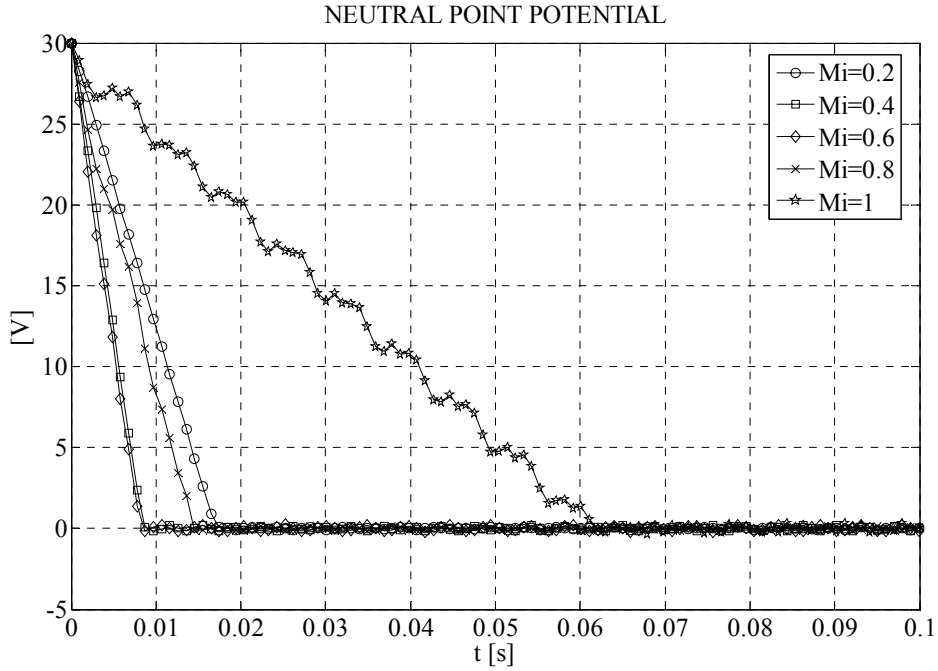


Figure 4.4 Neutral point potential control performance of the uniform α control method for various modulation indices and PF=1.0.

For the above simulation cases, the additional voltage/current waveforms (such as the phase currents, voltages, etc.) will not be shown for all the operating conditions studied due to the limited space. However, as a representative example, the simulation waveforms for M_i=0.8 and PF=0.0 will be shown in the following. Figure 4.5 shows the three-phase balanced current sink waveforms which are sinusiodal with 7.1 A rms (10 A peak value). Figure 4.6 shows the uniform α variable. As the figure illustrates, the uniform α controller mostly operates at the maximum values (0 or 1) in order to minimize the neutral point potential error. Figure 4.7 illustrates the corresponding neutral point current. Due to the PWM operation, the neutral point current consists of nearly rectangular current pulse waveforms. The resulting neutral point potential is illustrated in Figure 4.8. The neutral point potential has a strong third harmonic component that is due to the medium voltage vector. Due to this large triplen harmonic voltage, the uniform α controller is forced to operate at the α boundaries of 0 or 1. However, the error can not be totally manipulated. Due to the extreme α values, the line-to-neutral output voltage of the inverter legs involves a

distorted waveform. As Figure 4.9 illustrates the line-to-neutral voltage waveform is partially saturated and does not have a quarter-wave symmetry. The saturation of the uniform α controller at the boundaries of 0 or 1 results in elimination of one of the small voltage vectors and the symmetry is lost. Hence, an asymmetric (or a-periodic) phase voltage waveform. On the other hand, this asymmetry and distortion does not reflect to the load performance because the line–to-line voltage is not distorted. As Figure 4.10 shows, the line-to-line voltage exhibits a regular pattern of NTV-PWM.

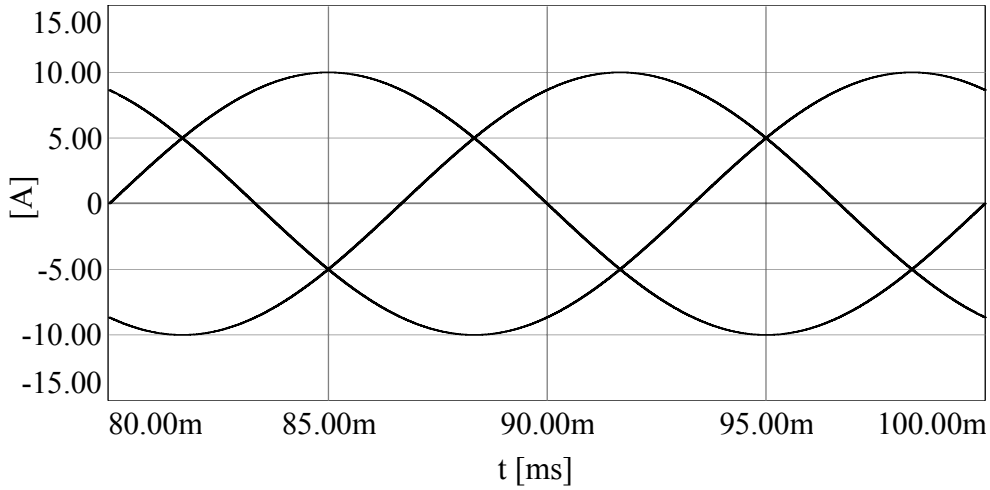


Figure 4.5 Current sink type load three-phase current waveforms for M_i=0.8 and PF=0.0.

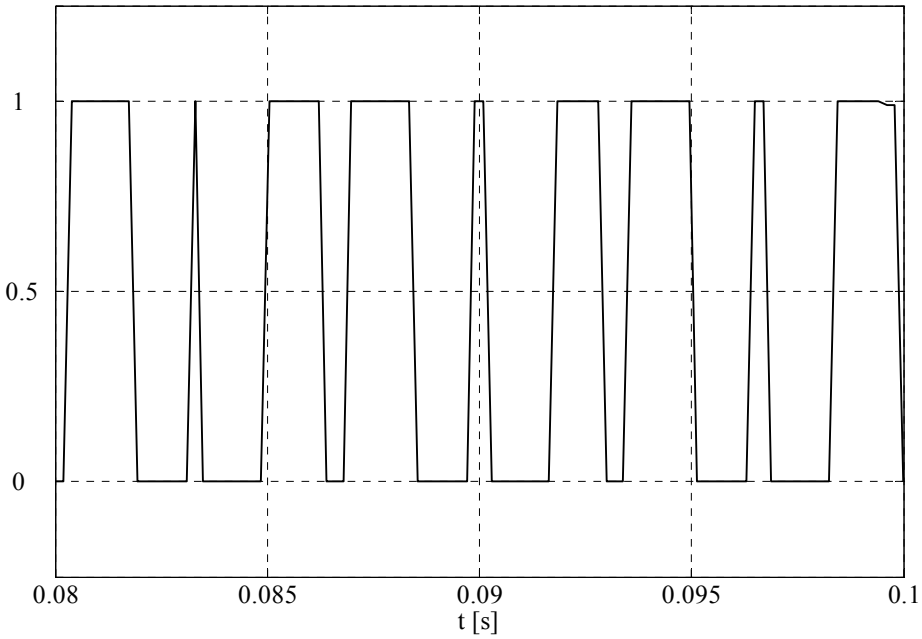


Figure 4.6 The redundancy function α for the uniform α method (M_i=0.8 and PF=0.0).

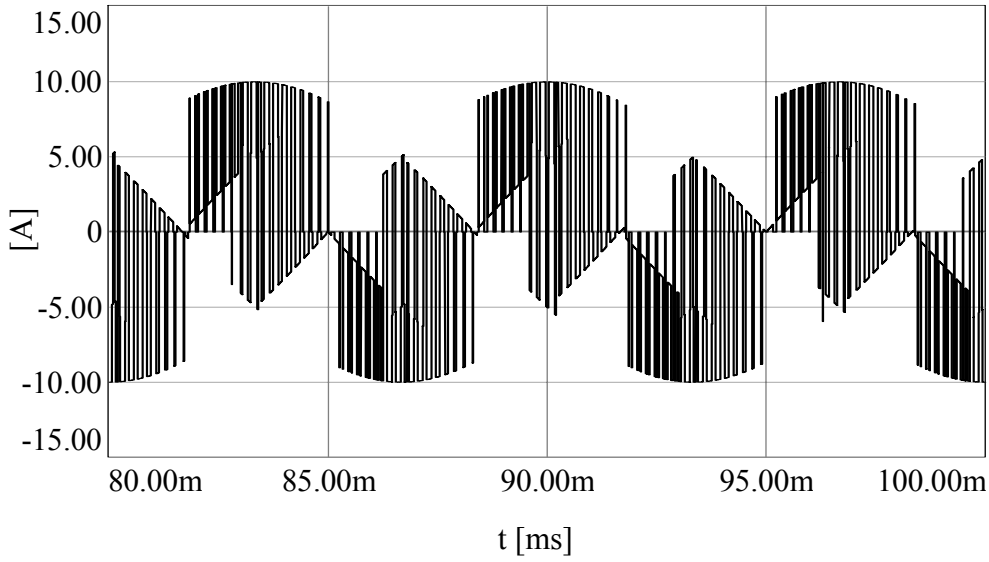


Figure 4.7 Neutral point current waveform at steady-state for M_i=0.8 and PF=0.0.

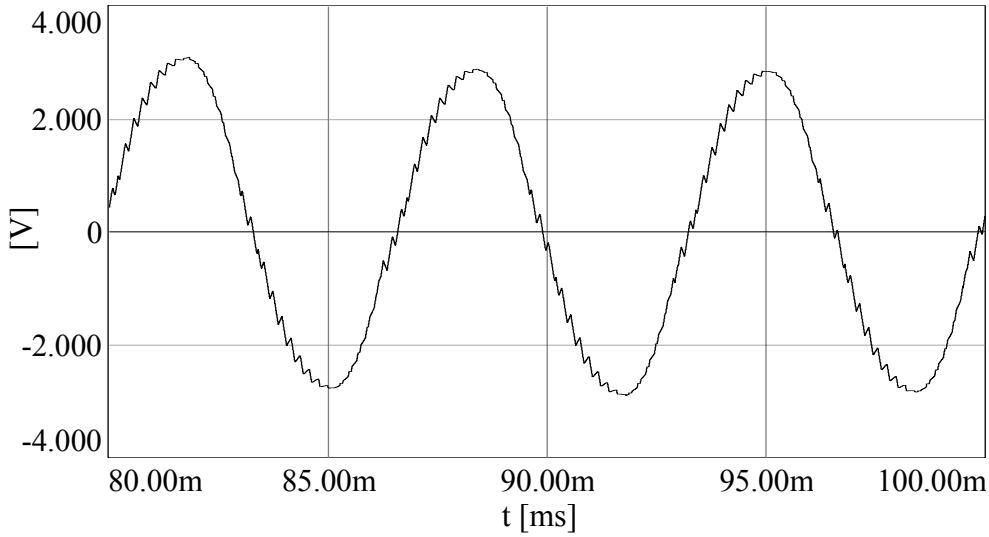


Figure 4.8 Neutral point potential waveform at steady-state for M_i=0.8 and PF=0.0.

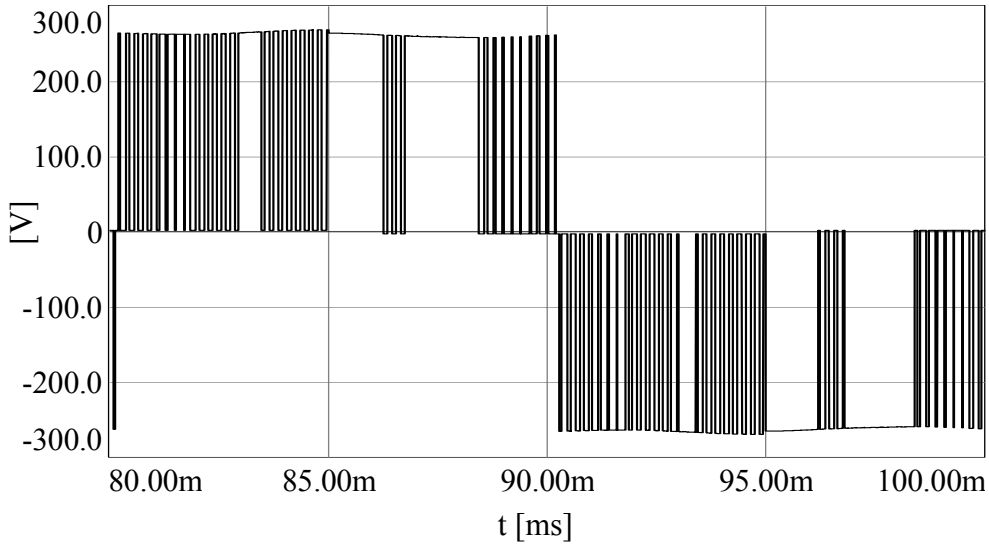


Figure 4.9 The line-to-neutral output voltage waveform at steady-state for M_i=0.8 and PF=0.0.

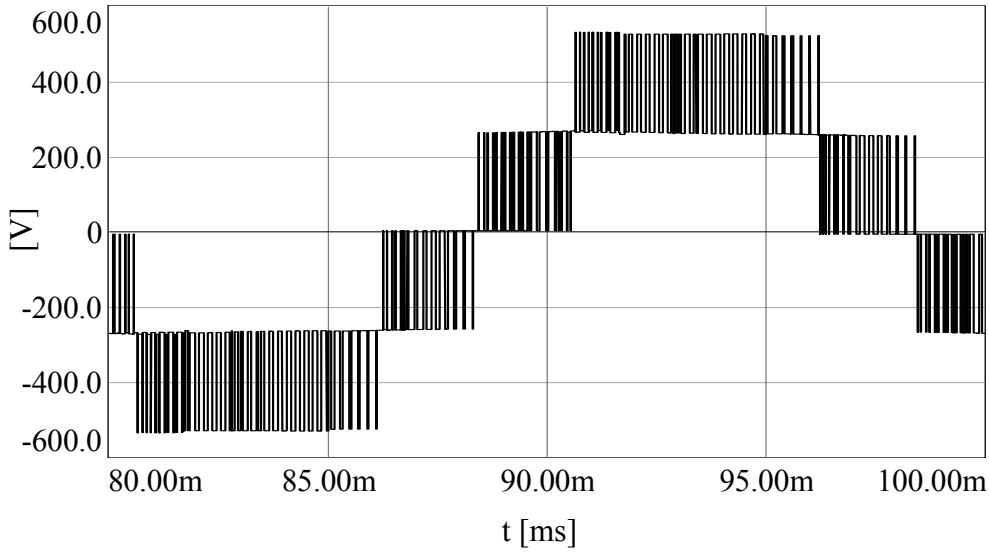


Figure 4.10 The line-to-line output voltage waveform at steady-state for M_i=0.8 and PF=0.0.

4.3.2 NTV-PWM with The Optimal α Control Method

In this section, the neutral point potential behavior of the NTV-PWM with optimal α control method is presented. In Figure 4.11, the neutral point potential control performance of the optimal α control is illustrated for various M_i values and PF=0.0. The time from 30 V neutral point potential error to zero is investigated. As seen from Figure 4.11, the performance of the controller is satisfactory except for the M_i=1 operating condition. For low modulation index values 0.2 and 0.4, the controller response is faster than the uniform α control method case. The response of the control method is nearly same as the average model simulation response (Figure 3.21). The triplen harmonic voltage on the neutral point potential can not be totally eliminated for the modulation index range of 0.6-1.

At PF=1.0, the optimal α control method is satisfactory in all modulation range as shown in Figure 4.12. The response is nearly same as the average model simulation case (Figure 3.22).

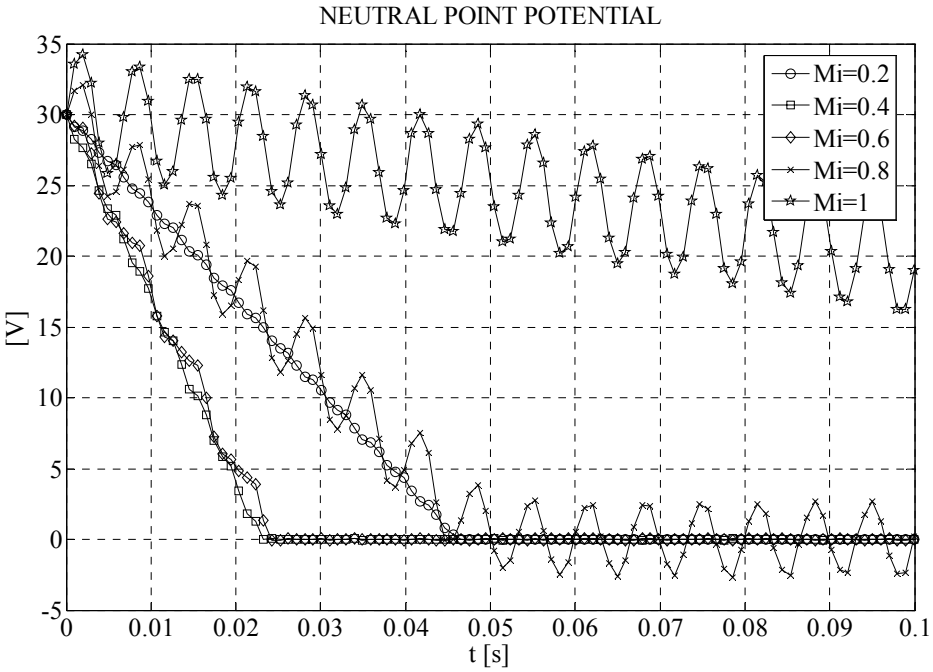


Figure 4.11 Neutral point potential control performance of the optimal α control method for various modulation indices and PF=0.0.

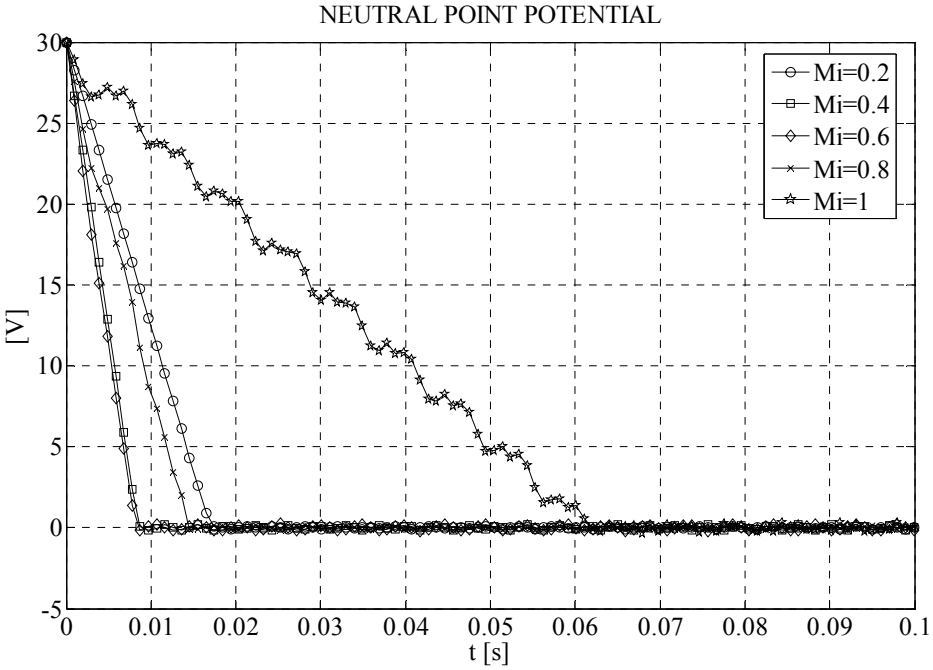


Figure 4.12 Neutral point potential control performance of the optimal α control method for various modulation indices and PF=1.0.

As a representative example, the detailed simulation waveforms for M_i=0.8 and PF=0.0 will be shown in the following. The load current waveform is the same as in Figure 4.5. Figure 4.13 shows the optimal α redundancy functions. As the graphic illustrates, as the optimal α controller attempts to reduce the error to zero at the optimal rate, the redundancy functions saturate in a coordinated manner. For the illustrated zero power factor case, they saturate in opposite directions, yielding the maximum possible charge for neutral point potential error compensation. Figure 4.14 illustrates the corresponding neutral point current. Due to the PWM operation, the neutral point current consists of nearly rectangular current pulse waveforms. The resulting neutral point potential is illustrated in Figure 4.15. The neutral point potential has a strong third harmonic component that is due to the medium voltage vector. Due to this large triplen harmonic voltage, the optimal α controller is forced to operate at the α boundaries of 0 or 1. However, the error can not be totally manipulated. Due to the extreme α values, the line-to-neutral output voltage of the inverter legs involves a distorted waveform. As Figure 4.16 illustrates the line-to-neutral output voltage waveform is partially saturated and does not have a quarter-wave symmetry. The saturation of the optimal α controller at the boundaries of 0 or 1 results in elimination of one of the small voltage vectors and the symmetry is lost. Hence, an asymmetric (or a-periodic) phase voltage waveform. On the other hand, this asymmetry and distortion does not reflect to the load performance because the line to line voltage is not distorted. As Figure 4.17 shows, the line-to-line voltage exhibits a regular pattern of NTV-PWM. Performance comparison to the uniform α method can be made via the comparison of Figure 4.8 and 4.15. There is a small difference between the results for the two methods considered. The peak neutral point potential is larger than 2.5 V for the uniform α method while it is slightly less for the optimal α method. In both cases the charge of the small voltage vectors is insufficient to compensate for the effect of the medium voltage vector.

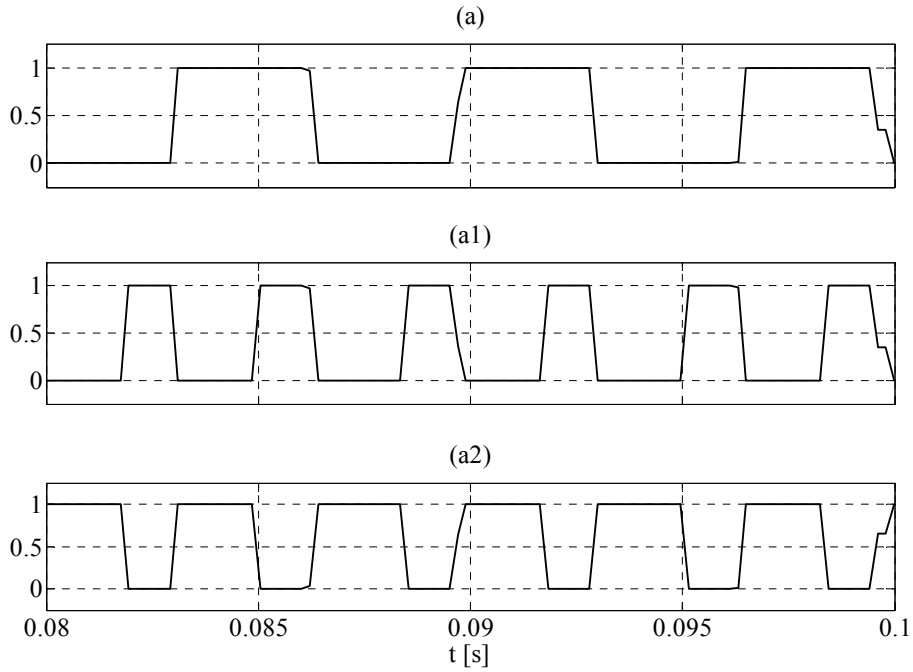


Figure 4.13 The redundancy function α, α_1, and α_2 for the optimal α control method at steady-state for M_i=0.8 and PF=0.0 (a:α, a1:α_1, and a2:α_2).

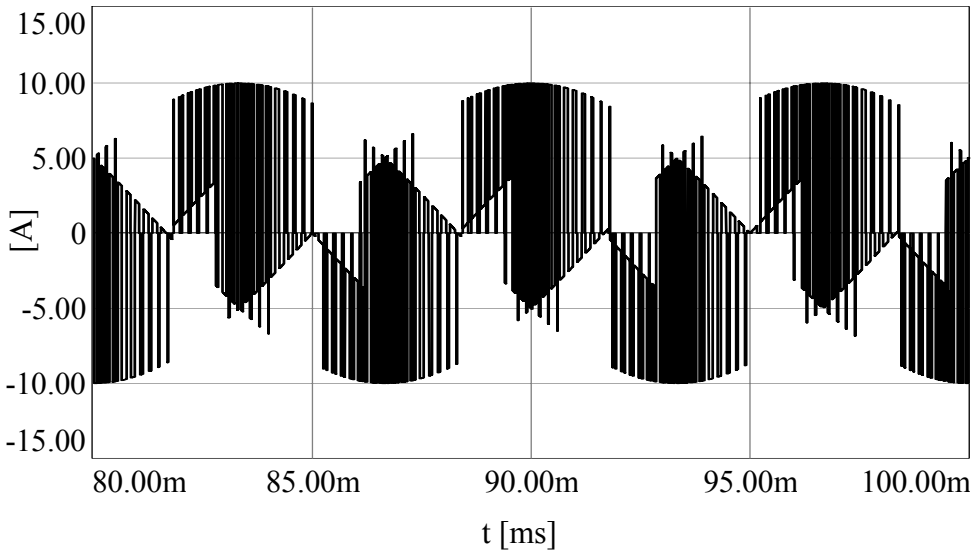


Figure 4.14 Neutral point current waveform at steady-state for M_i=0.8 and PF=0.0.

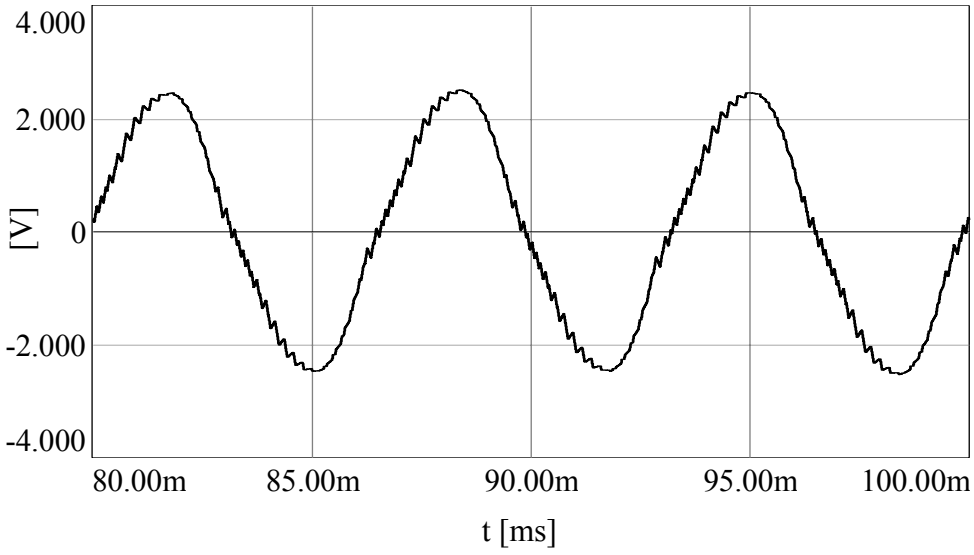


Figure 4.15 Neutral point potential waveform at steady-state for M_i=0.8 and PF=0.0.

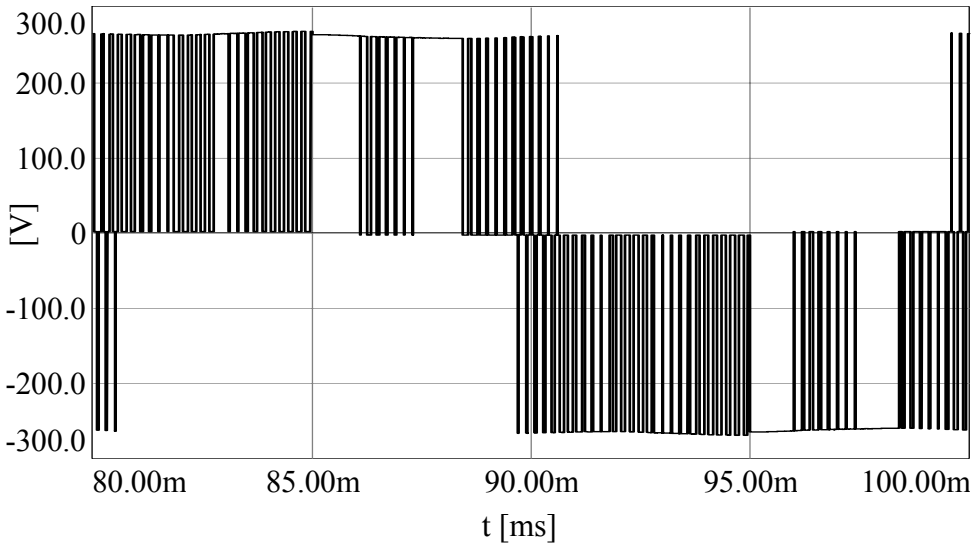


Figure 4.16 The line-to-neutral output voltage waveform at steady-state for M_i=0.8 and PF=0.0.

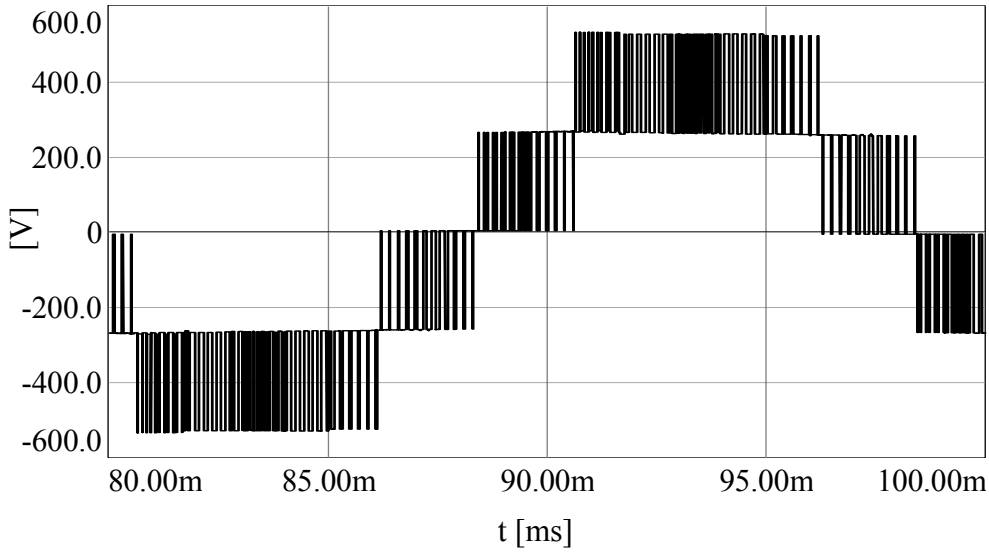


Figure 4.17 The line-to-line output voltage waveform at steady-state for M_i=0.8 and PF=0.0.

4.3.3 Two-Parameter PWM with The Optimal α-γ Control Method

This section illustrates the neutral point potential control performance of the two-parameter PWM with α–γ control method for various modulation index and power factor values. In this case, the optimal α–γ method proposed in 3.5.2.3.2 is utilized. In Figure 4.18, the neutral point potential performance of the optimal α–γ control method is presented for PF=0.0 and various M_i values. As seen from the figure, the performance of the optimal α–γ control method is superior to other methods over the full modulation range. There is no significant triplen harmonic on the neutral point potential throughout the linear modulation range. The low modulation index (M_i<0.5) range performance of the optimal α–γ control method is same as the optimal α control method performance. At high modulation index values, the optimal α–γ method performance is superior to other methods**.** The results are in strong agreements with those of section 3.5.2.3.2 of the previous chapter where the average model is utilized. At unity power factor operating condition, the neutral point potential performance of the optimal α–γ control method is illustrated in Figure 4.19. The simulation results are in agreement with those of the average model simulation (Figure 3.32) of the previous chapter.

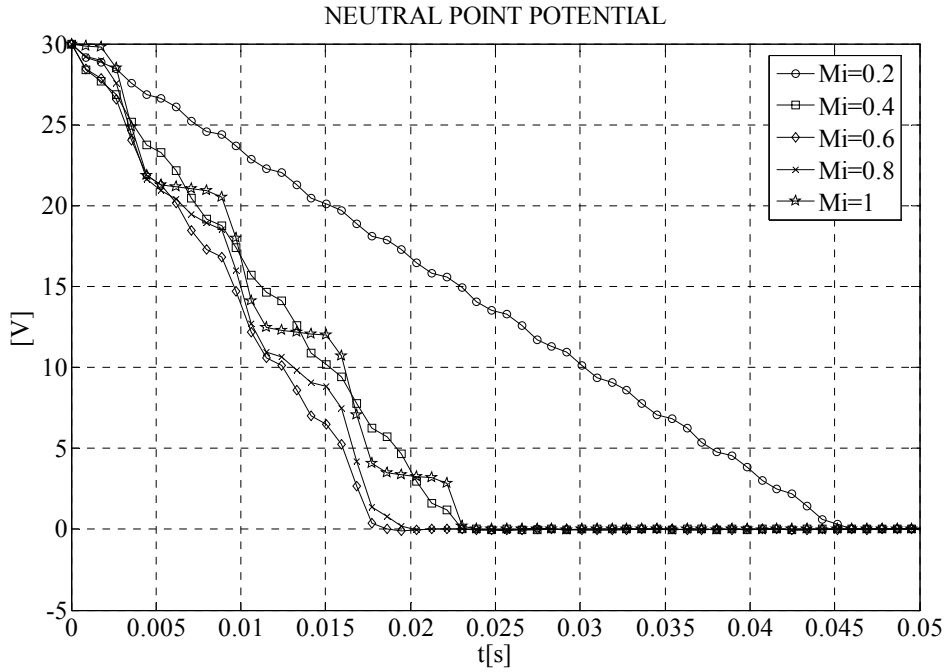


Figure 4.18 Neutral point potential control performance of the two-parameter PWM method with optimal α-γ control for various modulation indices and PF=0.0.

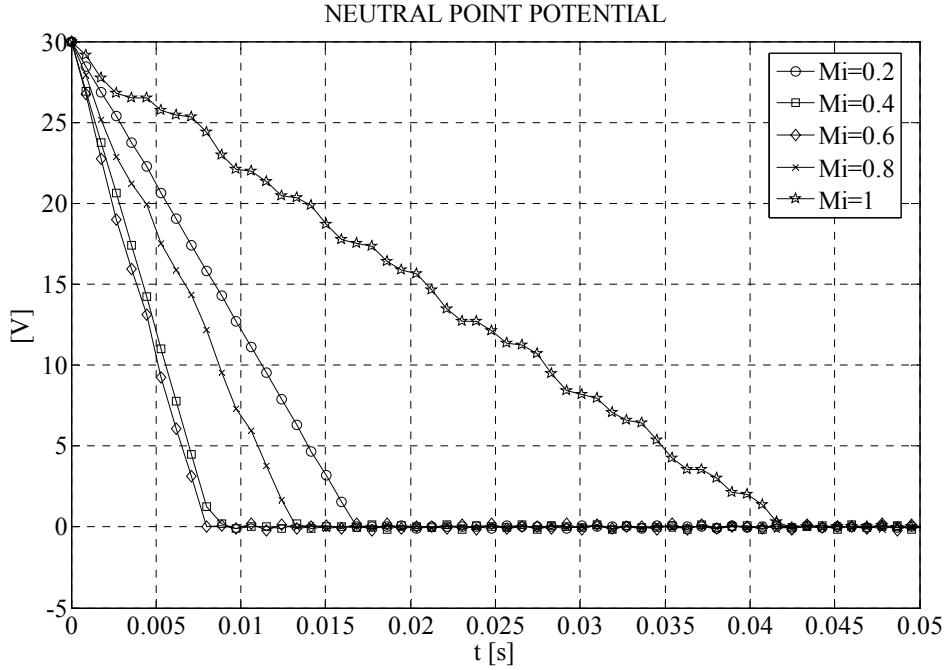


Figure 4.19 Neutral point potential control performance of the two-parameter PWM method with optimal α-γ control for various modulation indices and PF=1.0.

As a representative example, the detailed simulation waveforms for M_i=0.8 and PF=0.0 will be shown in the following. The load current waveform is the same as in Figure 4.5. Figure 4.20 shows the optimal α–γ redundancy functions. As the graphic illustrates, as the optimal α–γ controller attempts to reduce the error to zero at the optimal rate, the redundancy functions saturate in a coordinated manner. For the illustrated zero power factor case, first the α controller tries to reduce the error to zero, and coordinates α_1 and α_2 in a manner to maximize the charge capability. When the neutral point potential error is large, the optimal α variables saturate in opposite directions, yielding the maximum possible charge for neutral point potential error compensation. If the compensating charge is insufficient, the γ variable is also decreased such that the effect of the medium voltage vector is reduced. As seen from Figure 4.20 at steady-state, the γ parameter is rarely unity and this implies the γ controller is active and strongly reducing the effect of the triplen harmonic neutral point current. Figure 4.21 illustrates the corresponding neutral point current. Due to the PWM operation, the neutral point current consists of nearly rectangular current pulse waveforms. The resulting neutral point potential is illustrated in Figure 4.22.

The neutral point potential has no visible triplen or any other harmonic component because the medium voltage vector is effectively eliminated. The results are in strong agreement with the average model simulations of the previous chapter. Figure 4.23 illustrates the line-to-neutral output voltage waveform. In this case the waveform has a quarter-wave symmetry. As Figure 4.24 shows, the line-to-line voltage exhibits a different pulse pattern from the regular pattern of NTV-PWM and full DC bus voltage switchings occur (the line to line voltage has pulses of V_{dc} magnitude).

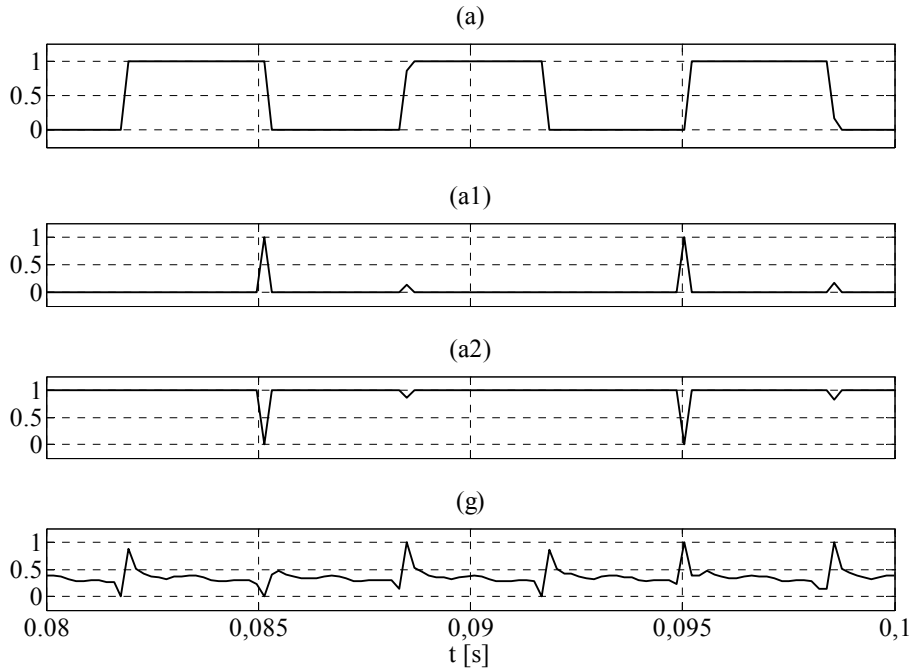


Figure 4.20 The redundancy function α, α_1, α_2 and distribution factor γ for the α-γ method for M_i=0.8 and PF=0.0 (a:α, a1:α_1, a2:α_2, and g:γ).

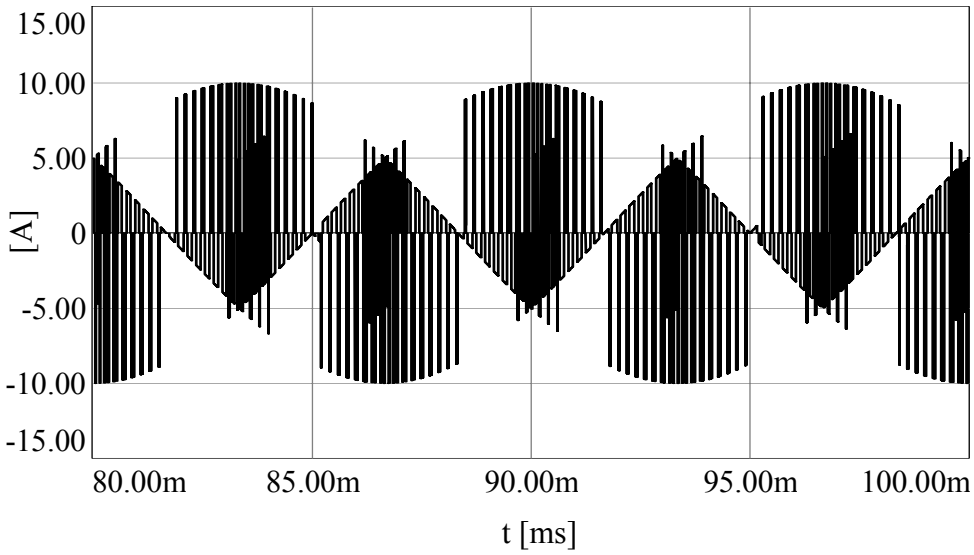


Figure 4.21 Neutral point current waveform at steady-state for M_i=0.8 and PF=0.0.

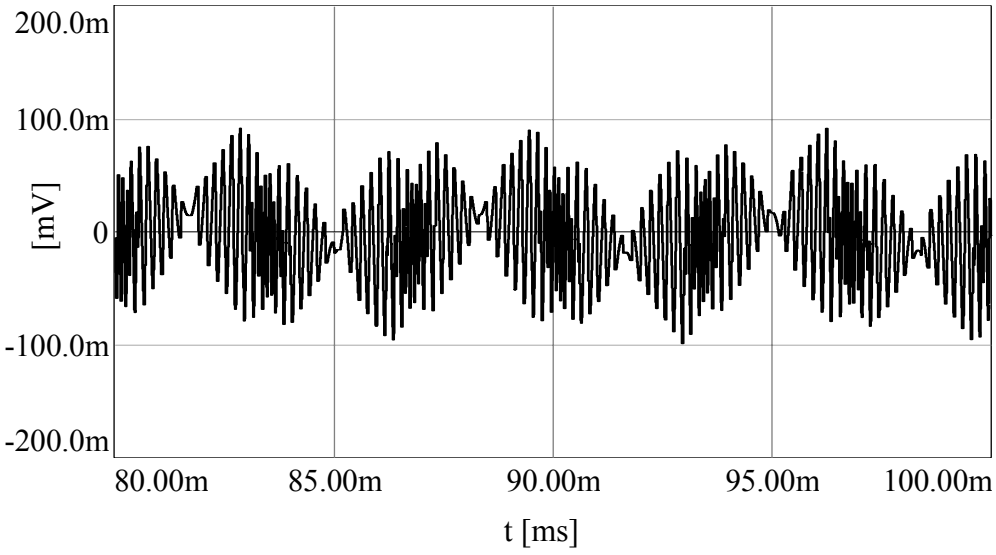


Figure 4.22 Neutral point potential waveform at steady-state for M_i=0.8 and PF=0.0.

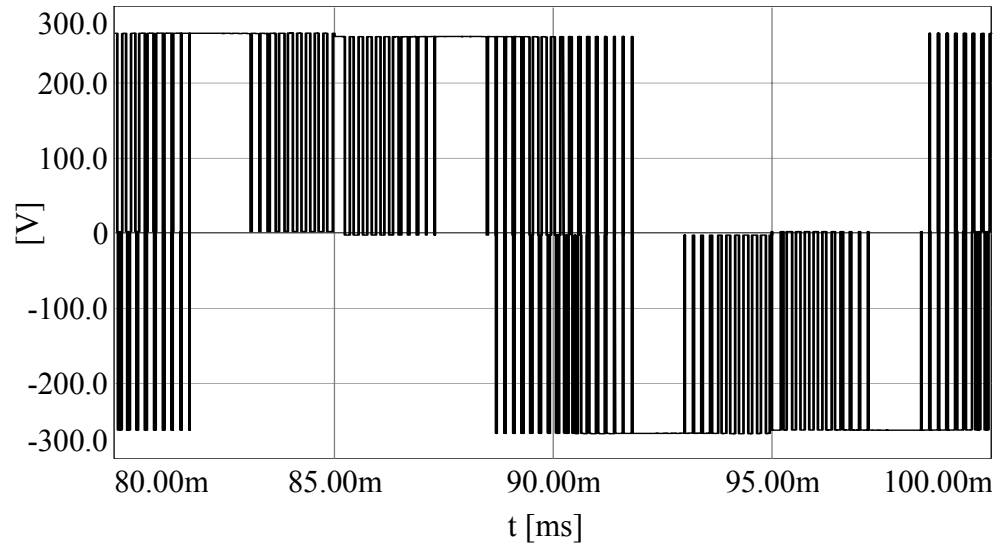


Figure 4.23 The line-to-neutral output voltage waveform at steady-state for M_i=0.8 and PF=0.0.

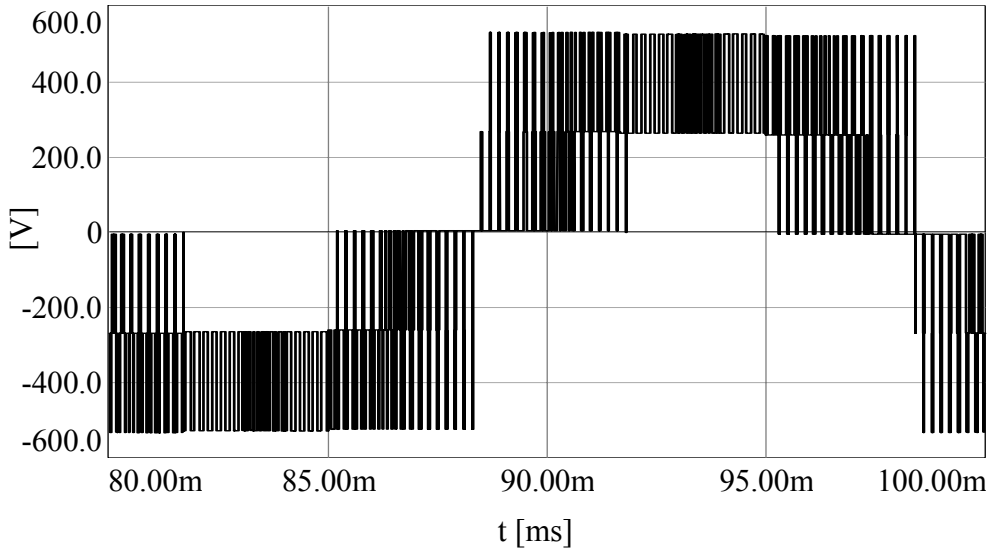


Figure 4.24 The line-to-line output voltage waveform at steady-state for M_i=0.8 and PF=0.0.

4.3.4 Performance Comparisons of The Neutral Point Potential Control Methods and Accuracy Comparison of The Average and Detailed Simulation Models

Table 4.2 and Table 4.3 summarize the neutral point potential performance of the three control methods simulated in section 4.3.1 to 4.3.3 of this section. The time interval from 30 V neutral point potential error to zero neutral point potential error Δt and the steady-state peak to peak neutral point potential value ΔV_{pp} are shown in the tables. The tables compare the detailed model simulation results to those obtained by the average model simulation of chapter 3. As the tables indicate, for both unity and zero power factor conditions the average model and detailed model simulations yield highly correlated results. Thus, the accuracy of the average model has been proven. At low modulation index and zero power factor, the average model gives incorrect results due to the fact that the inverter losses are not represented. At all other operating points, the average and detailed models are practically equal.

The tables illustrate the neutral point potential performance superiority of the optimal α-γ control method to the other methods. Specifically at high modulation index

values, the time to zero neutral point potential error is the smallest with the optimal α-γ control method and it is several times smaller than the optimal or uniform α control method. For example, at unity modulation index, the ratio is about twenty times. Moreover, the most striking difference appears in the peak to peak voltage ripple. While the optimal α-γ control method gives practically zero value, the other methods have approximately 5 V ripple. Therefore, both the steady-state and dynamic performance of the optimal α-γ control method are superior to those of the other two methods.

Although the detailed inverter drive model with a current sink provides a good behavioral model of the drive system for the purpose of the neutral point potential analysis, it is insufficient in terms of completely illustrating the drive dynamics, the inverter output current ripple, and other effects. For that reason, in the following a more detailed load model involving a three-phase R-L circuit is investigated.

Table 4.2 Performance comparison of various neutral point potential control methods (PF=0)

Control Method	Model	Average Model Simulation					Detailed Model Simulation				
	M_i	0.2	0.4	0.6	0.8	1.0	0.2	0.4	0.6	0.8	1.0
Uniform α_u	ΔV_{pp} (V)	0	0	2	6	8	0	0	3.2	5.6	8
	Δt (ms)	120000	60000	120	80	500	600	270	110	75	300
Optimal α_o	ΔV_{pp} (V)	0	0	0.01	5	8	0	0	0	5	7
	Δt (ms)	46	23	24	60	500	45	22	22	55	400
Optimal α_o-γ_o	ΔV_{pp} (V)	0	0	0	0	0	0	0	0	0	0
	Δt (ms)	46	23	19	20	21	45	23	18	20	23

Table 4.3 Performance comparison of the various neutral point potential control methods (PF=1.0)

Control Method	Model	Average Model Simulation					Detailed Model Simulation				
	M_i	0.2	0.4	0.6	0.8	1.0	0.2	0.4	0.6	0.8	1.0
Uniform α_u	ΔV_{pp} (V)	0	0	0	0	0.63	0	0	0	0	0.4
	Δt (ms)	18	9	8	14	71	17	8	8	14	62
Optimal α_o	ΔV_{pp} (V)	0	0	0	0	0.63	0	0	0	0	0.4
	Δt (ms)	18	9	8	14	71	17	8	8	14	62
Optimal α_o-γ_o	ΔV_{pp} (V)	0	0	0	0	0	0	0	0	0	0
	Δt (ms)	18	9	8	13	46	17	8	8	13	42

4.4 Simulation of a Three-Level NPC Inverter Driving an R-L Load

In this section, the neutral point potential behavior of the three-level NPC inverter for an R-L load is investigated by means of computer simulations. In the university laboratory there is no flexible motor drive test bench. An alternative means is the passive three-phase R-L type load. The R-L load provides an effective and practical means for verifying the neutral point potential performance of the proposed control methods in the university laboratory. Thus, the performance of the developed neutral point potential control methods can be verified by means of experimental results of an R-L load and experimental results can be correlated with computer simulations and analysis. For this reason, in this section three-level NPC inverter driven R-L load simulations will be provided in detail.

The per-phase R-L load parameters of the simulated system are as given in Table 4.4. The three-phase R-L load is fed by the same three-level NPC inverter as discussed throughout this chapter. In the simulations the R-L load is driven from the inverter by using the constant V/f method. The V/f ratio of the inverter is selected as 220 V / 50 Hz=4.4 T. The AC line supply voltages feeding the three-phase rectifier in this case are assumed as 233 V (rms) as this value corresponds to the typical AC line voltages measured at the university laboratory. Note that in the previous simulations the AC line voltage values were taken as 220 V rms nominal value. The deviation from the nominal value is for the purpose of creating simulation conditions similar to what will be tested in the laboratory and reported in the following chapter.

Table 4.4 Three-phase R-L load parameters

Load Phase	R (Ω)	L (mH)
U	8.2	55.45
V	8.2	55.45
W	8.0	55.45

In the simulations, two different frequency values are used that correspond to two different modulation indices. For low modulation index (M_i=0.29), the reference

frequency value is 15 Hz and for high modulation index (M_i=0.93), the reference frequency value is 45 Hz. First, NTV-PWM without neutral point potential control (α=0.5) will be employed and simulation results will be shown both for 15 Hz and 45 Hz. Second, the uniform α control method simulation results will be shown at low and high modulation index. Third, the optimal α control method results will be presented. Finally, the two-parameter PWM with optimal α–γ control method simulation results will be shown and briefly the simulation results of this section will be compared.

4.4.1 NTV-PWM without Neutral Point Potential Control

This section presents the simulation results of the NTV-PWM method without neutral point potential control for the unbalanced R-L load. In Figure 4.25, the neutral point potential waveform is shown at low modulation index (M_i=0.29). As seen from the figure, the neutral point potential drifts by a small amount. The small voltage vectors are employed at low modulation index (inner hexagon) and the small voltage vectors inject current to or draw current from the neutral point. The drift is slow, but visible from the waveform. The minimal drift is due to the simulation model symmetry. In the simulations all inverter switches are identical and all phases are symmetric. Therefore, it is expected that in the experimental test the drift will be faster than the simulation case. The zoomed view of the simulated neutral point potential is shown in Figure 4.26. The PWM frequency ripple is the only visible ripple. In Figure 4.27, the phase current and the neutral point potential are shown. The phase current is nearly sinusoidal. This is due to the superior waveform quality characteristics of the three-level NPC inverter. The effective switching frequency is twice as the two-level inverter with the same carrier frequency. Since in this case 5 kHz carrier frequency is utilized, effectively the results are as good as those of a 10 kHz two-level inverter. Thus, invisible ripple on the phase current waveforms. The line-to-line output voltage waveform is given in Figure 4.28 and shows the attributes of a two-level inverter with half-DC-bus voltage value, that is typical of the three-level NPC inverter.

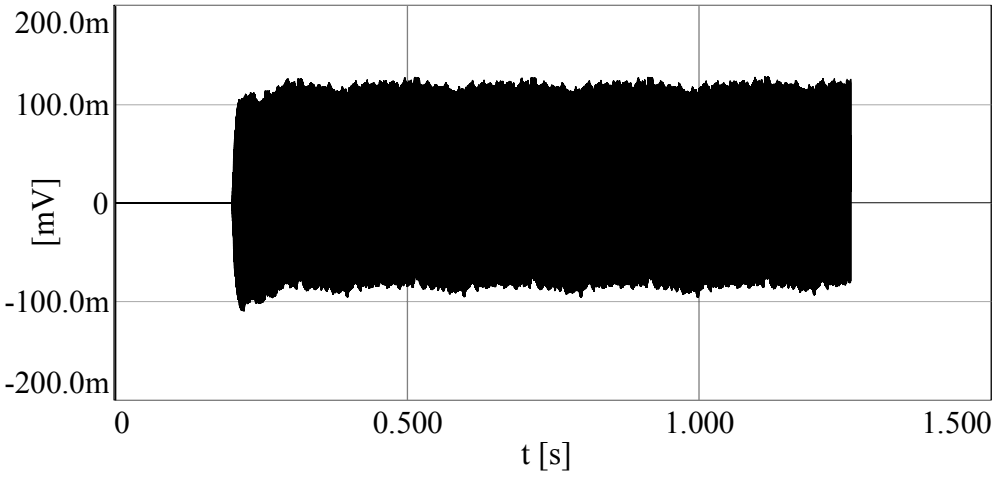


Figure 4.25 The neutral point potential waveform at low modulation index (M_i=0.29) for NTV-PWM without neutral point potential control (α=0.5).

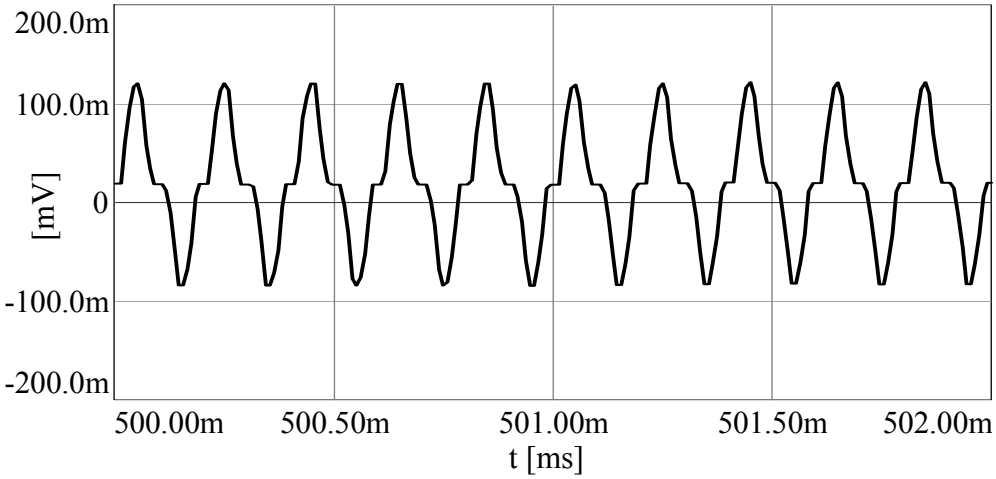


Figure 4.26 The zoom-in view of the neutral point potential at low modulation index (M_i=0.29) for NTV-PWM without neutral point potential control (α=0.5).

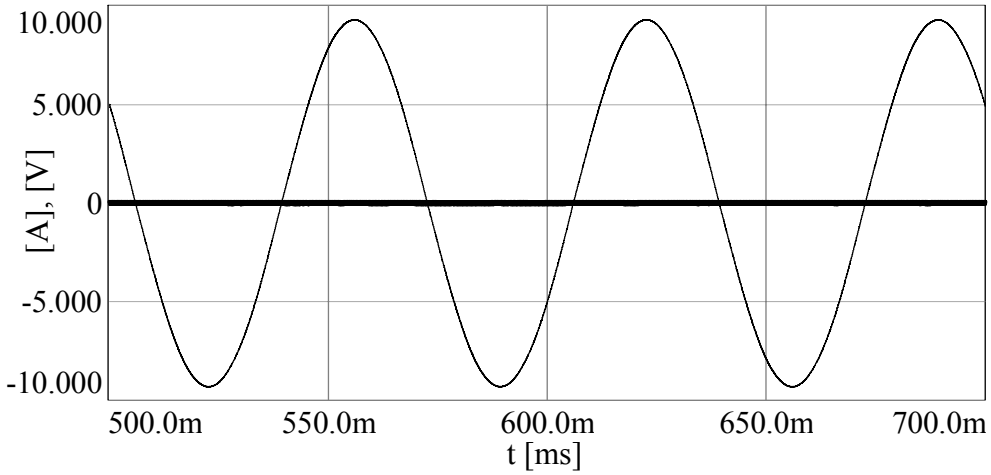


Figure 4.27 The neutral point potential (bold) and the phase current at low modulation index (M_i=0.29) for NTV-PWM without neutral point potential control (α=0.5).

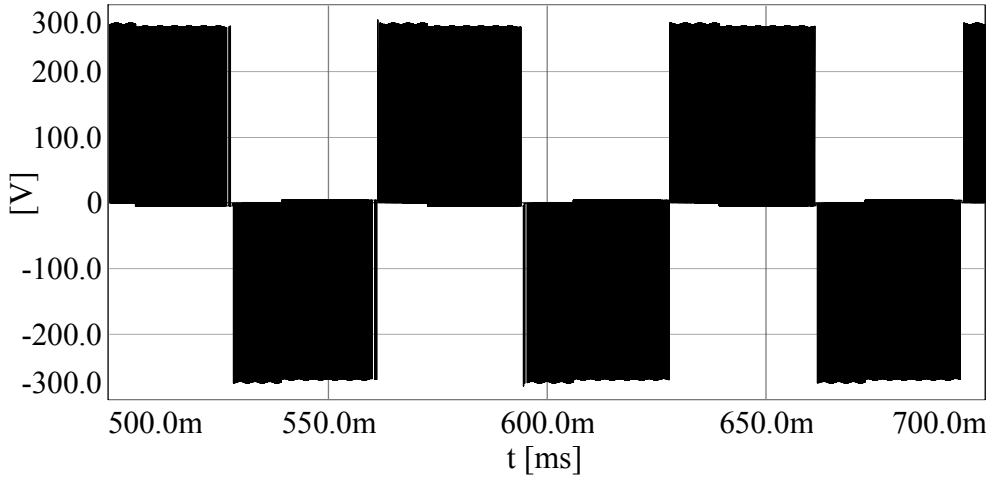


Figure 4.28 The line-to-line output voltage waveform of the three-level NPC inverter for NTV-PWM without neutral point potential control (α=0.5) at low modulation index (M_i=0.29).

The neutral point potential behavior of the NTV-PWM without neutral point potential control at high modulation index (M_i=0.93) is shown in Figure 4.29. The neutral point potential has a small drift and has a dominant triplen harmonic component as shown in Figure 4.30. The small drift is created by the small voltage

vectors and triplen harmonic content is created by the medium voltage vector. In Figure 4.30, the phase current and the neutral point potential are shown in the same window to illustrate the triplen harmonic content. The phase current has a sinusoidal waveform. The line-to-line output voltage waveform has five levels as shown in Figure 4.31.

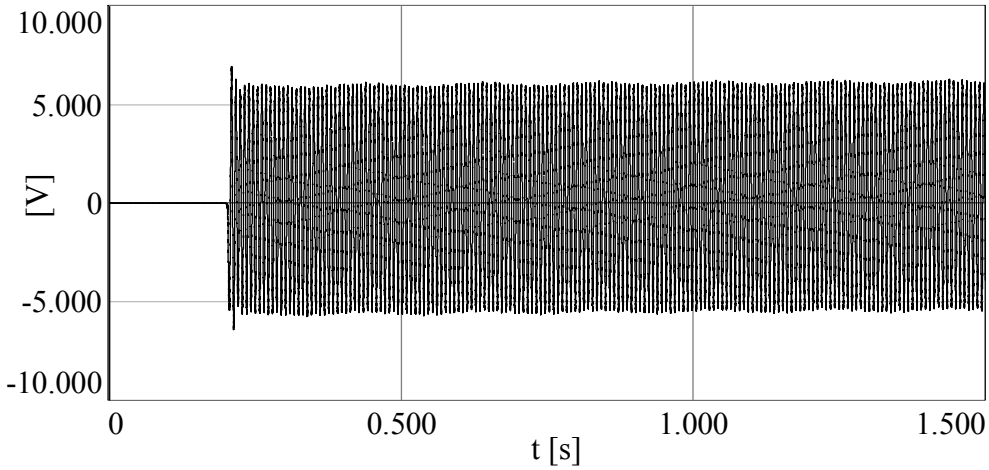


Figure 4.29 The neutral point potential waveform at high modulation index (M_i=0.93) for NTV-PWM without neutral point potential control (α=0.5).

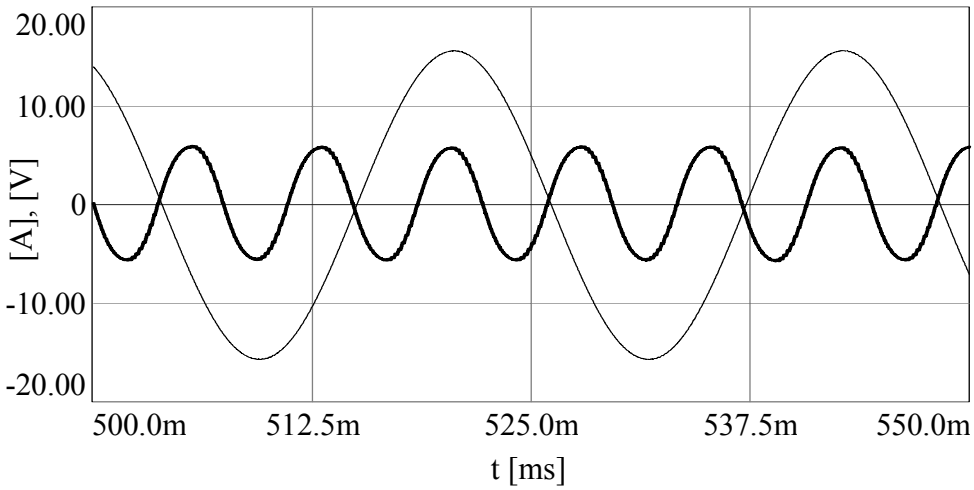


Figure 4.30 The neutral point potential (bold) and the phase current at steady-state and high modulation index (M_i=0.93) for NTV-PWM without neutral point potential control (α=0.5).

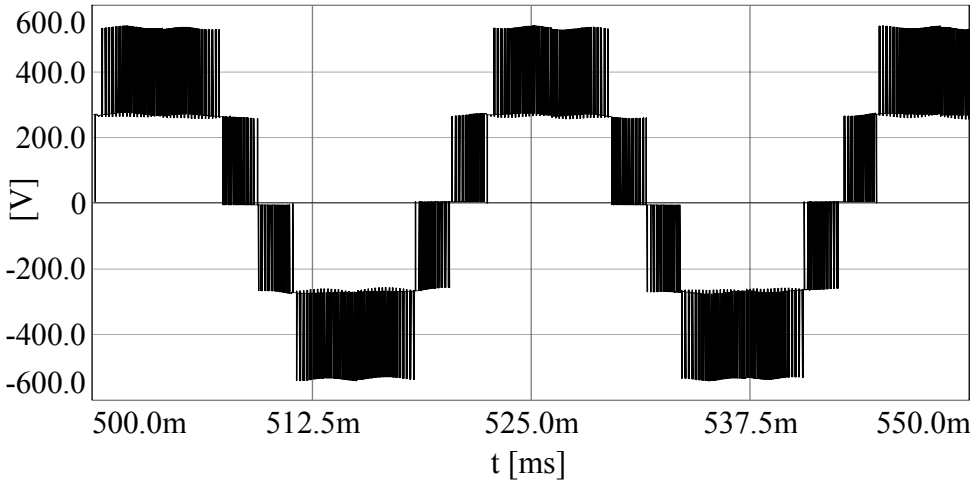


Figure 4.31 The line-to-line output voltage waveform of the three-level NPC inverter for NTV-PWM without neutral point potential control (α=0.5) at steady-state and high modulation index (M_i=0.93).

4.4.2 NTV-PWM with The Uniform α Control Method

In this section, NTV-PWM with the uniform α control method simulation results are illustrated. Initially, the neutral point potential error is set as 40 V. This value is different from what has been used in the current sink type load system simulations (30V). This change in the initial value is based on the findings of this research during the advanced stages. As will be illustrated in the following chapter, during the laboratory test of the same R-L load of Table 4.4, about 40 V neutral point potential drift was measured without any neutral point potential control loop. Thus, in this section the 40 V initial neutral point potential error will be assumed. In Figure 4.32 the neutral point potential waveform is shown for low M_i (M_i=0.29). As seen from the figure, the neutral point potential error is eliminated in about 22 ms and at steady-state the neutral point potential has only PWM frequency ripple with a small magnitude as shown in Figure 4.33. The phase current and the neutral point potential waveform are illustrated in Figure 4.34. There is no dominant triplen harmonic on the neutral point potential and the phase current is nearly sinusoidal. The line-to-line output voltage waveform of the three-level NPC inverter is shown in Figure 4.35.

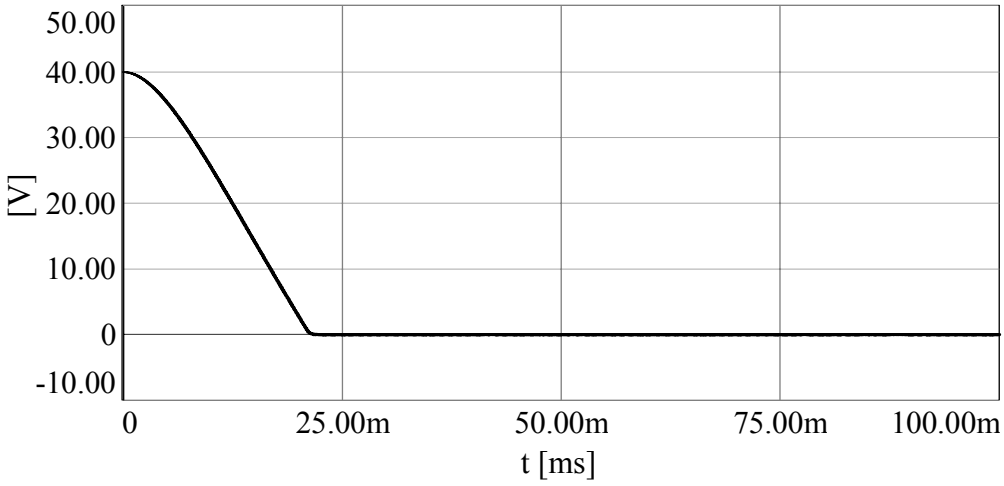


Figure 4.32 The neutral point potential waveform at low modulation index (M_i=0.29) for the NTV-PWM with the uniform α control method.

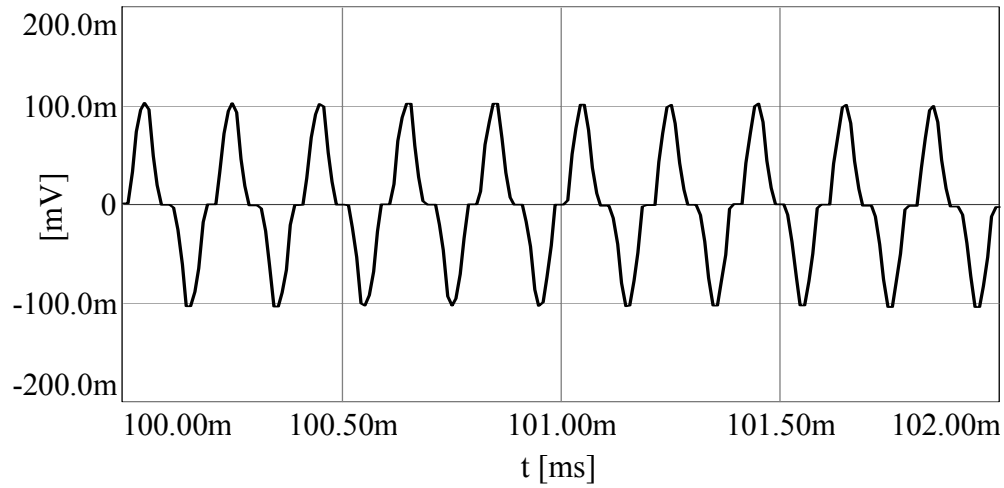


Figure 4.33 The zoom-in view of the neutral point potential at steady-state (M_i=0.29) for NTV-PWM with the uniform α control method.

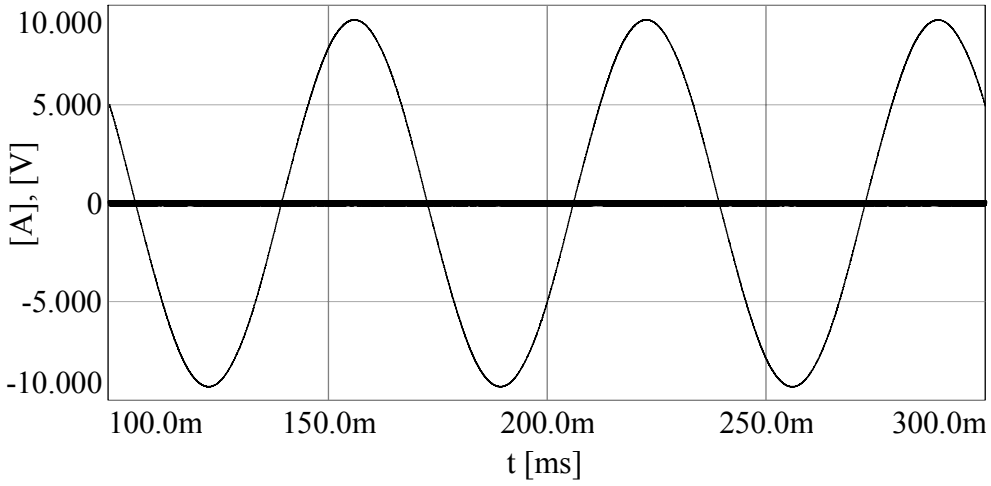


Figure 4.34 The neutral point potential (bold) and the phase current at steady-state (M_i=0.29) for NTV-PWM with the uniform α control method.

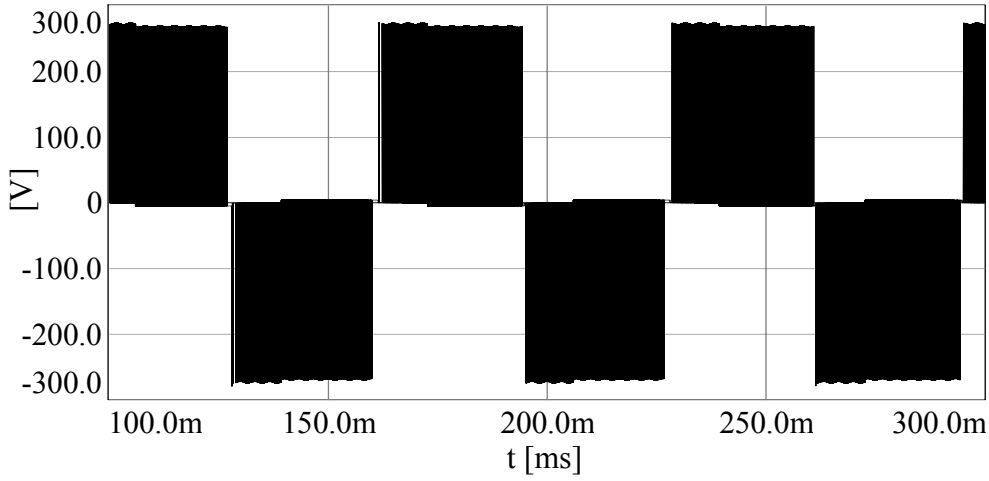


Figure 4.35 The line-to-line output voltage waveform of the three-level NPC inverter for the NTV-PWM with the uniform α control method at steady-state (M_i=0.29).

The neutral point potential performance of the uniform α control method for high modulation index value (M_i=0.93) is shown in Figure 4.36. The neutral point potential error is set equal to 45 V initially. Similar to the low modulation index case, the initial neutral point potential error is different from the current sink type load case of the previous section for the same reason. As seen from Figure 4.36, the

neutral point potential error is eliminated in about 50 ms. However, the triplen harmonic content of the neutral point potential can not be eliminated totally by the uniform α control method. In Figure 4.37, the steady-state operation neutral point potential and the phase current waveforms are illustrated. As seen from the figure the triplen harmonic content is dominant on the neutral point potential and the phase current has nearly pure sinusoidal waveform. The line-to-line output voltage waveform is shown in Figure 4.38. In the figure, the 300 Hz (six times the line frequency of 50 Hz) ripple on the line-to-line voltage magnitude is due to the six-pulse diode rectifier bridge with limited DC bus capacitive filtering.

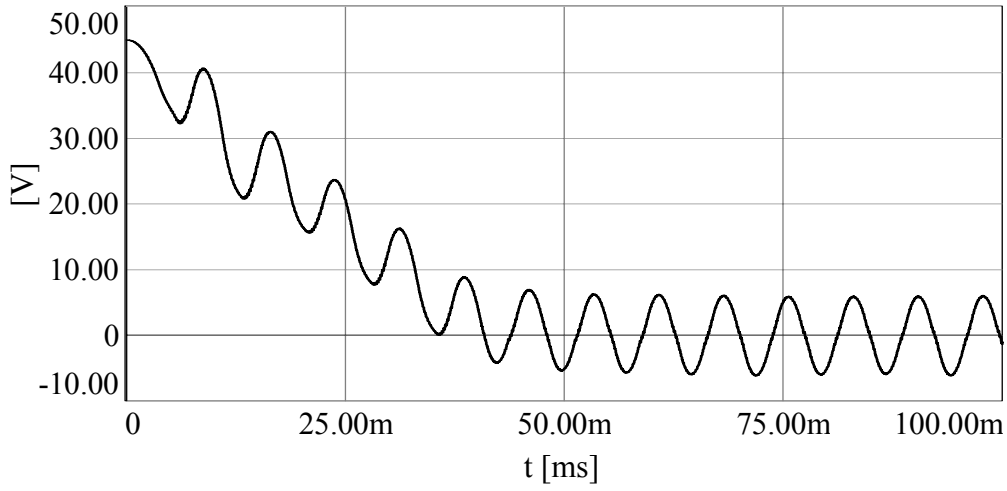


Figure 4.36 The neutral point potential waveform at high modulation index (M_i=0.93) for the NTV-PWM with uniform α control method.

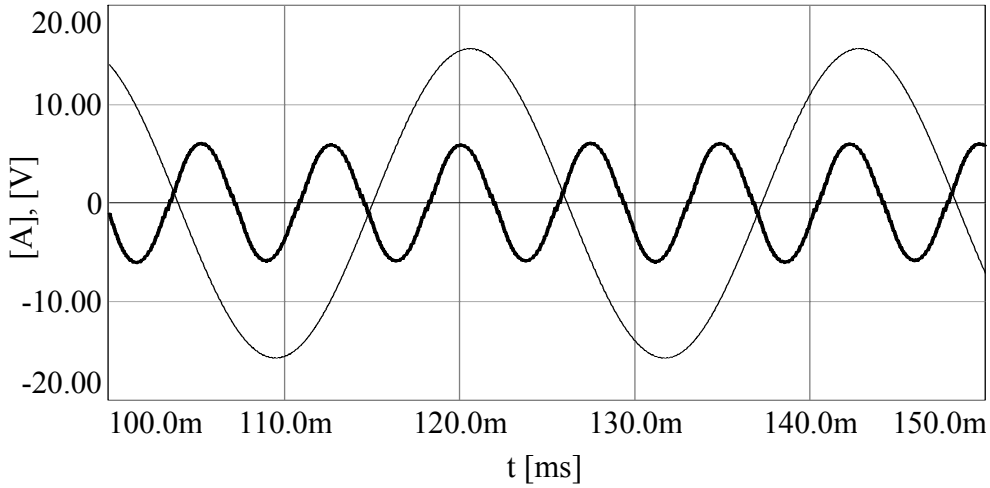


Figure 4.37 The neutral point potential (bold) and the phase current at steady-state (M_i=0.93) for the NTV-PWM without uniform α control method.

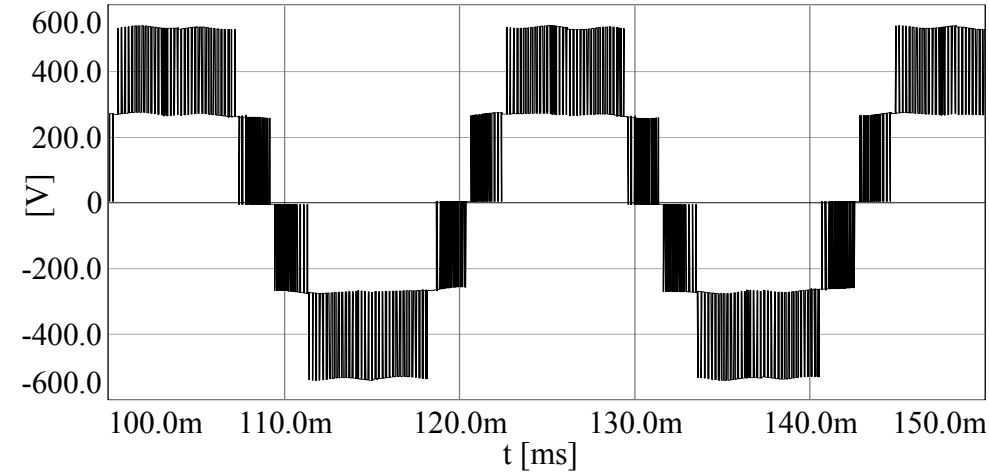


Figure 4.38 The line-to-line output voltage waveform of the three-level NPC inverter for the NTV-PWM with uniform α control method at steady-state (M_i=0.93).

4.4.3 NTV-PWM with The Optimal α Control Method

This section presents NTV-PWM with the optimal α control method simulation results. Initially, the neutral point potential error is set as 40 V. In Figure 4.39 the neutral point potential waveform is shown. As seen from the figure, the neutral point

potential error is eliminated in about 21 ms and the neutral point potential has only PWM frequency ripple with a small magnitude at steady-state as shown in Figure 4.40. The phase current and the neutral point potential waveform are illustrated in Figure 4.41. There is no dominant triplen harmonic on the neutral point potential and the phase current is nearly sinusoidal. The line-to-line output voltage waveform of the three-level NPC inverter is shown in Figure 4.42 and it is the same as the uniform α control method case.

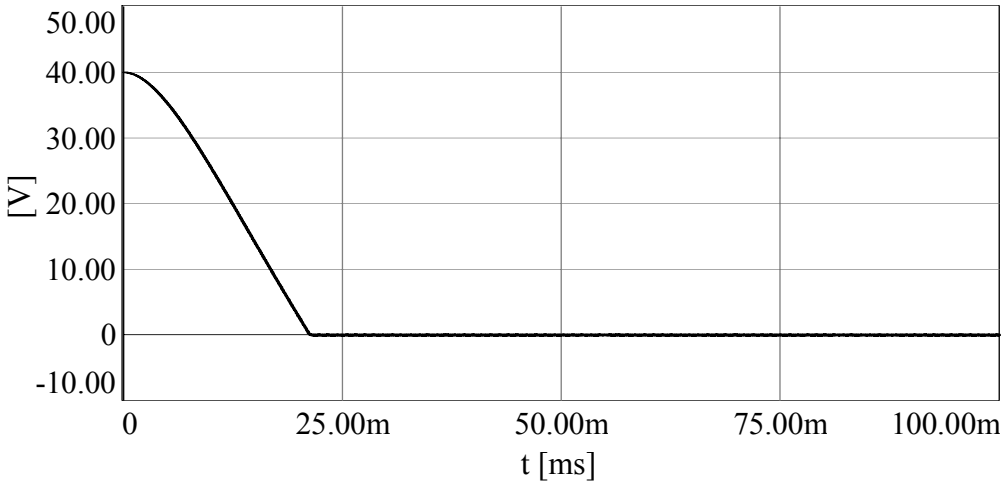


Figure 4.39 The neutral point potential waveform at low modulation index (M_i=0.29) for NTV-PWM with the optimal α control method.

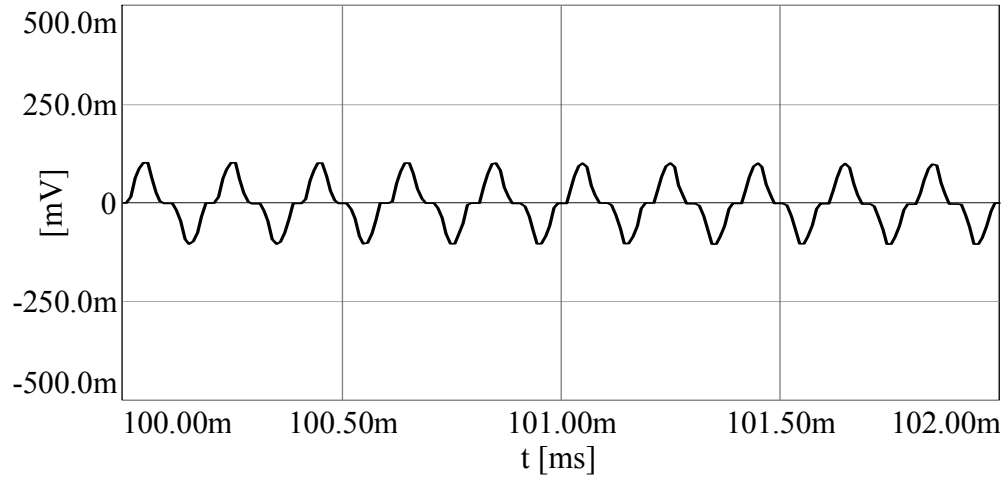


Figure 4.40 The zoom-in view of the neutral point potential at steady-state (M_i=0.29) for NTV-PWM with the optimal α control method.

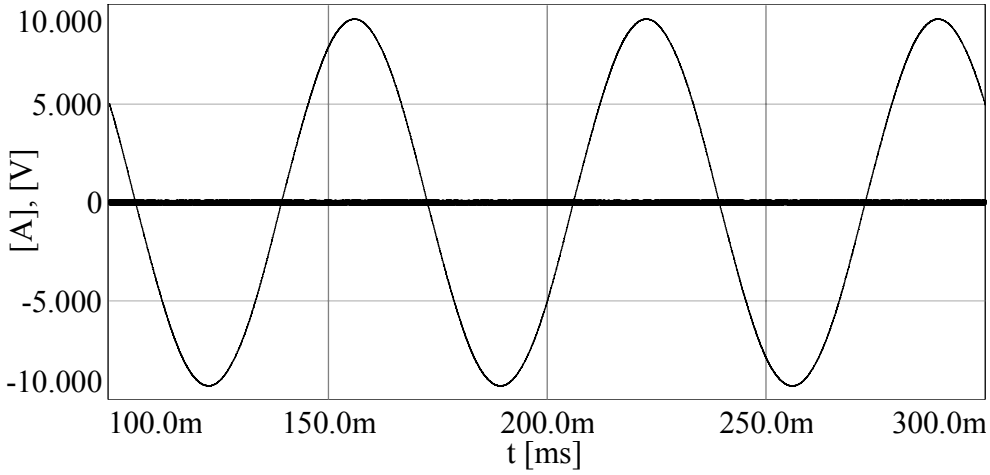


Figure 4.41 The neutral point potential (bold) and the phase current at steady-state (M_i=0.29) for NTV-PWM with the optimal α control method.

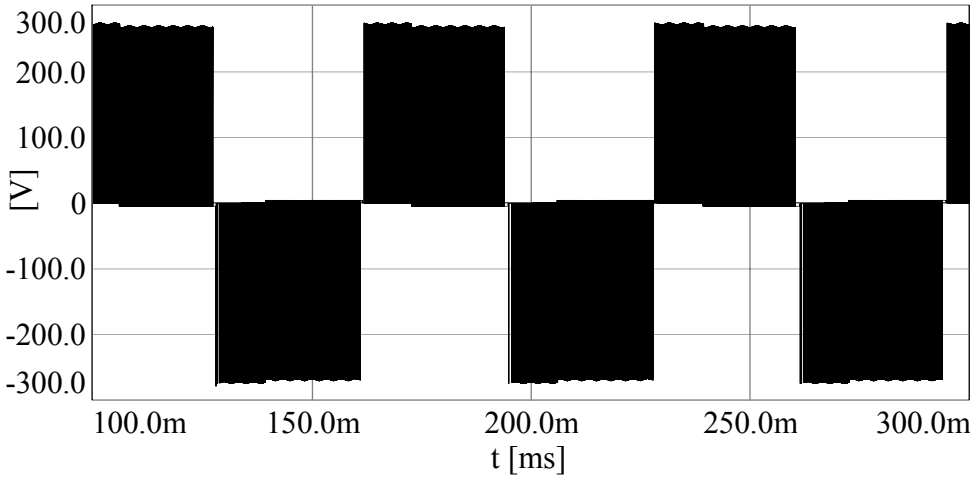


Figure 4.42 The line-to-line output voltage waveform of the three-level NPC inverter for the NTV-PWM with optimal α control method at steady-state (M_i=0.29).

The neutral point potential performance of the optimal α control method for high modulation index value (M_i=0.93) is shown in Figure 4.43. The neutral point potential error is set as 45 V initially. As seen from Figure 4.43, the neutral point potential error is eliminated in about 50 ms. It has the same performance as the

uniform α control method. At high modulation index values, the triplen harmonic content of the neutral point potential can not be eliminated totally by the optimal α control method. In Figure 4.44, the neutral point potential and the phase current waveforms are illustrated. As seen from the figure the triplen harmonic content is dominant on the neutral point potential and the phase current is sinusoidal. The line-to-line output voltage waveform is shown in Figure 4.45 and it is same as the uniform α control method case.

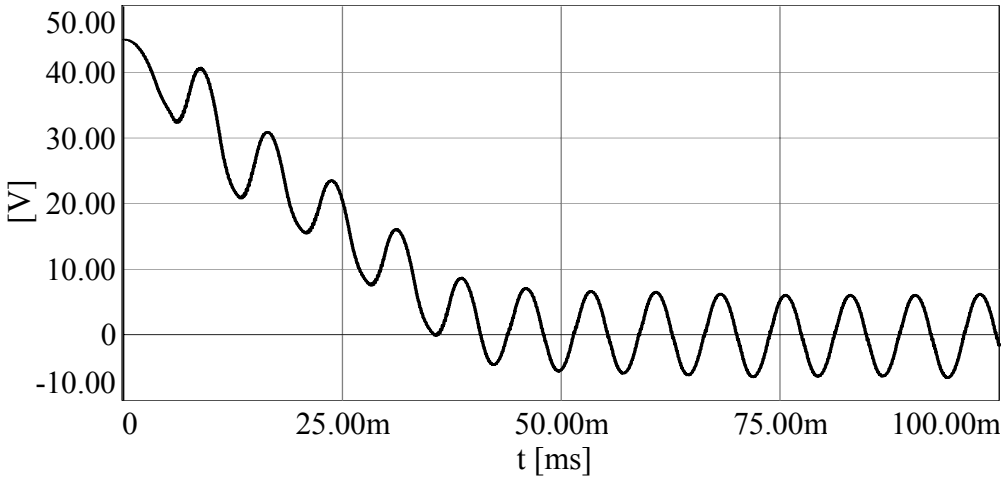


Figure 4.43 The neutral point potential waveform at high modulation index (M_i=0.93) for NTV-PWM with the optimal α control method.

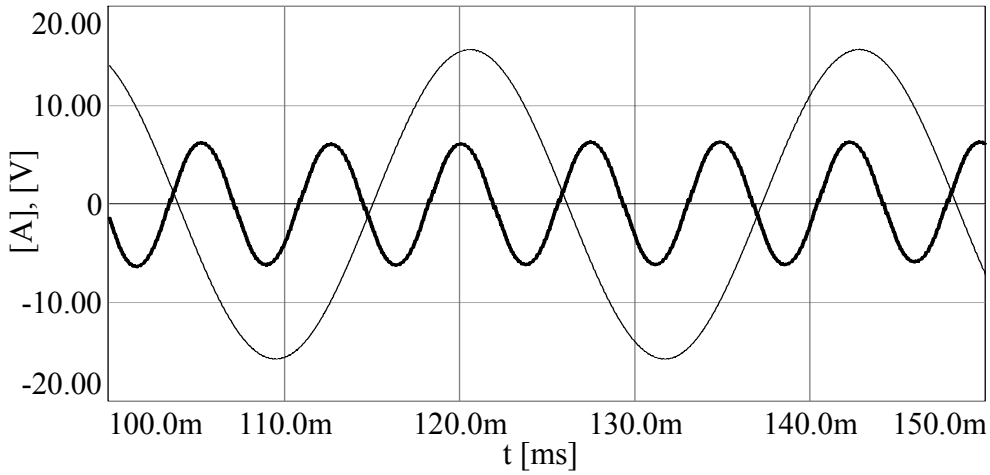


Figure 4.44 The neutral point potential (bold) and the phase current at steady-state (M_i=0.93) for NTV-PWM with the optimal α control method.

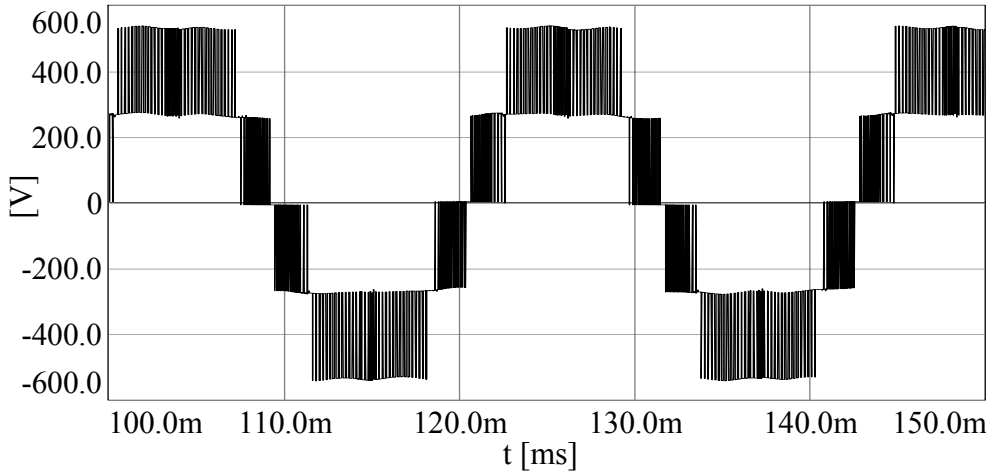


Figure 4.45 Line-to-line output voltage waveform of the three-level NPC inverter for NTV-PWM with the optimal α control method at steady-state (M_i=0.93).

4.4.4 Two-parameter PWM with The Optimal α-γ Control Method

In this section, the neutral point behavior of the two-parameter PWM with optimal α-γ control method is investigated for a three-phase R-L load at high modulation index. The low modulation index performance of the two-parameter PWM with the optimal α-γ control method is exactly same as the optimal α control method case because of the identical controller structure. Therefore, the low modulation index performance is neither shown nor discussed. In Figure 4.46, the neutral point potential waveform is shown for high modulation index value (M_i=0.93). The initial neutral point potential error is 45 V. As seen from figure, the neutral point potential error is eliminated in about 20 ms and it has no ripple at steady-state. The zoom-in view of the neutral point potential is shown in Figure 4.47 and the neutral point potential has only small ripple at the PWM frequency as shown from the figure. There is no dominant triplen harmonic content on the neutral point potential. The phase current waveform is shown in Figure 4.48 with the neutral point potential waveform. The line-to-line output voltage waveform at high modulation index is shown in Figure 4.49. It is different from the previous control method cases. In some cases, the line-to-line output voltage waveform is same as the two-level inverter line-to-line output voltage waveform. This pulse pattern results in increased PWM ripple voltage, however with

the R-L load time constant being long (6.76 ms) the ripple current becomes small and not visible on the current waveform.

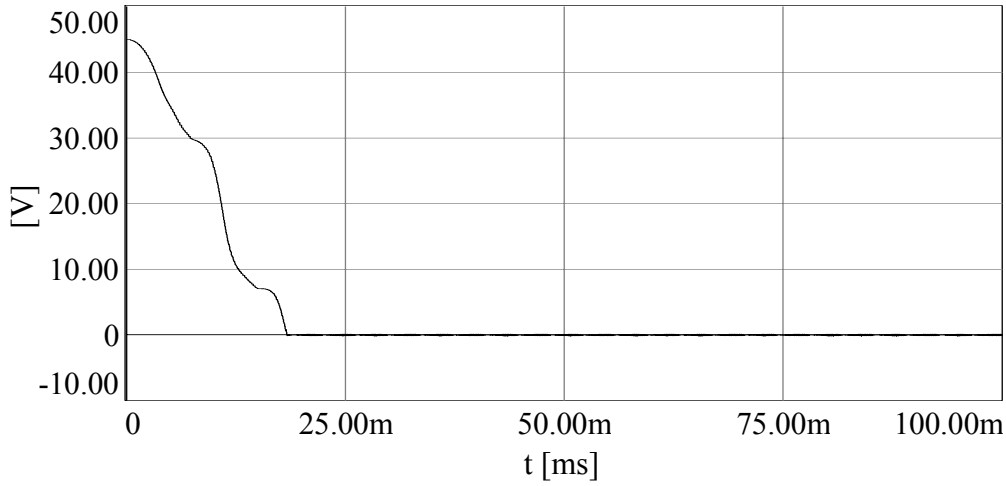


Figure 4.46 The neutral point potential waveform at high modulation index (M_i=0.93) for two-parameter PWM with the optimal α-γ control method.

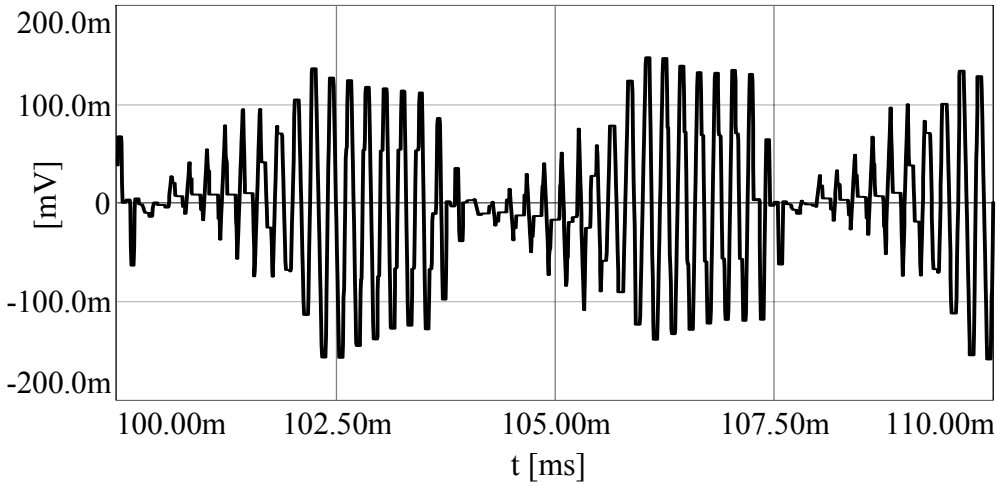


Figure 4.47 The zoom-in view of the neutral point potential at steady-state (M_i=0.93) for two-parameter PWM with the optimal α-γ control method.

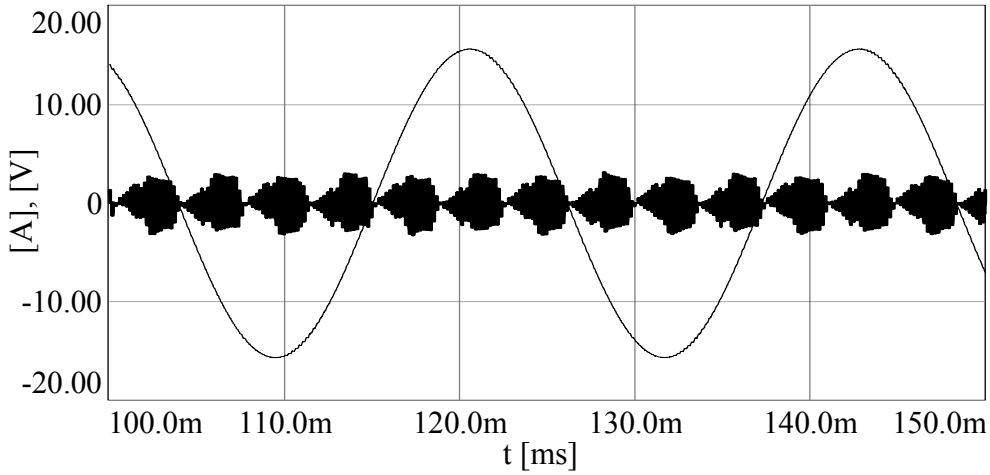


Figure 4.48 The neutral point potential (bold, scale: 20x) and the phase current at steady-state (M_i=0.93) for two-parameter PWM with the optimal α-γ control method.

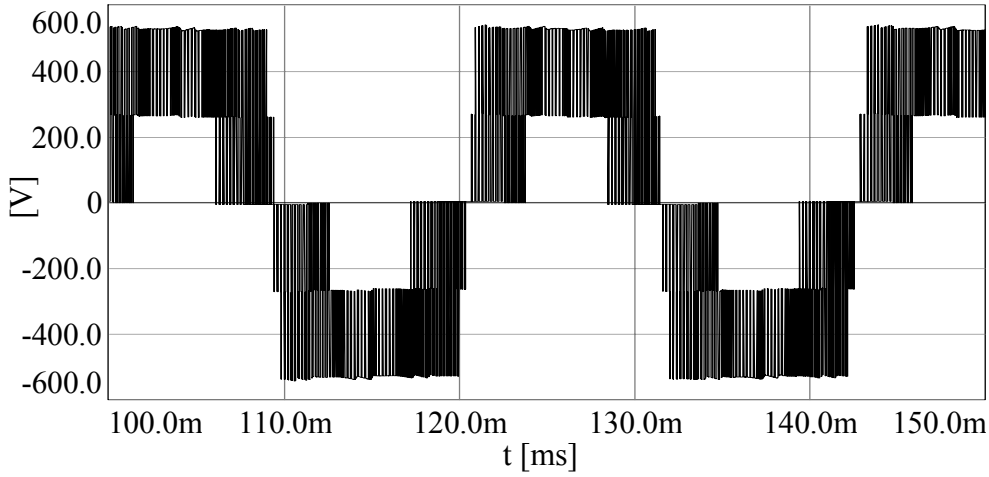


Figure 4.49 Line-to-line output voltage waveform of the three-level NPC inverter for two-parameter PWM with the optimal α-γ control method at steady-state (M_i=0.93).

4.4.5 Performance Comparisons of The Control Methods For The Constant V/f Driven R-L Load

Table 4.5 and Table 4.6 summarize the neutral point potential performance of the uncontrolled neutral point potential case R-L load along with the three control methods simulated in section 4.4.1 to 4.4.4 of this section. The time interval from a specific value of neutral point potential error to zero neutral point potential error Δt and the steady-state peak-to-peak neutral point potential value ΔV_{pp} are shown in the tables.

The tables illustrate the neutral point potential performance superiority of the optimal α-γ control method to the other methods. Specifically at high modulation index, the time to zero neutral point potential error is the smallest with the optimal α-γ control method and it is about 2.5 times smaller than the optimal or uniform α control method. Moreover, the most striking difference appears in the peak-to-peak voltage ripple. While the optimal α-γ control method gives practically zero value, the other methods have approximately 12 V ripple. Therefore, both the steady-state and dynamic performance of the optimal α-γ control method are superior to those of the other two methods. These results are in correlation with those obtained in the current sink type load simulations in section 4.3.4.

Although the detailed inverter drive model with an R-L load provides a good behavioral model of the drive system for the purpose of the neutral point potential analysis, it is insufficient in terms of completely illustrating the drive dynamics, the inverter output current ripple, and other effects. For that reason, in the following a more detailed load model involving an induction motor fed fan load is investigated by means of simulation.

Table 4.5 Neutral point potential performance comparison of various control methods at low modulation index (M_i=0.29, f_o=15Hz)
(f_{PWM}: PWM frequency)

Control Method	Neutral Point Potential Drift	Steady-state Peak Voltage ΔV_{pp} (mV)	Error Elimination Time Δt (ms)	Neutral Point Potential Ripple Frequency
NTV-PWM (α =0.5)	18 mV	200	None	f_{PWM}
Uniform α	None	200	21.5	f_{PWM}
Optimal α	None	200	21	f_{PWM}
Optimal α-γ	None	200	21	f_{PWM}

Table 4.6 Neutral point potential performance comparison of various control methods at high modulation index (M_i=0.93, f_o=45Hz)
(f_{PWM}: PWM frequency and f_o: output voltage fundamental frequency)

Control Method	Neutral Point Potential Drift	Steady-state Peak Voltage ΔV_{pp} (V)	Error Elimination Time Δt (ms)	Neutral Point Potential Ripple Frequency
NTV-PWM (α =0.5)	200 mV	9.6	None	$3f_o$
Uniform α	None	12.4	48	$3f_o$
Optimal α	None	12.4	48	$3f_o$
Optimal α-γ	None	0.32	19	f_{PWM}

4.5 Induction Motor Drive System Simulations

In this section the neutral point potential behavior of a three-level NPC inverter driving an induction motor is investigated by means of computer simulations. For motion control, constant V/f ratio method is employed. The induction motor parameters are given in Table 4.7.

Table 4.7 Three-phase induction motor parameters

Rated power	5 Hp
Rated frequency	50 Hz
Line to line rated voltage	380 V
Number of poles (P)	4
Stator resistance (r_{stator})	1.969 Ω
Referred rotor resistance (r'_{rotor})	1.730 Ω
Stator leakage inductance (L_{stator})	11.20 mH
Referred rotor leakage inductance (L'_{rotor})	11.20 mH
Magnetizing inductance (L_m)	275.63 mH
Inertia (J)	0.05 kg m^2/s

The V/f ratio of the inverter is selected as 220 V/50 Hz=4.4 T. In the simulations, the motor drives a fan load. The fan load is assumed to have a quadratic relation to the load torque ($T_L=K\cdot\omega_m^2$). For the fan load the torque coefficient is selected as K=0.00127 such that the motor nominal torque and speed corresponds to the nominal operation of the fan load. The drive will be tested under various operating conditions such as acceleration and constant speed operations. The neutral point potential performance of the various neutral point potential control methods will be tested. First, the low speed performance of the neutral point potential control methods will be evaluated. The motor will be accelerated from zero speed to 400 rpm. Here at steady-state the inverter output voltage electrical frequency becomes 13.3 Hz. Second, the high speed performance of the neutral point potential control methods will be investigated. The motor will be accelerated from zero speed to 1311 rpm. In

this case, at steady-state the inverter output voltage electrical frequency becomes 46.7 Hz.

In the following, the above described motor drive operating conditions will be simulated with emphasis on the neutral point potential behavior under various speed (modulation index) values and neutral point potential control methods. The following techniques will be considered in the appearing sequence:

i) NTV-PWM without neutral point potential control ($\alpha=\alpha_1=\alpha_2=0.5$ and $\gamma=1$)
ii) NTV-PWM with the uniform α control method ($\alpha=\alpha_1=\alpha_2$)
iii) NTV-PWM with the optimal α control method ($\alpha=\alpha_o$)
iv) Two-parameter PWM with the optimal α-γ control method

4.5.1 NTV-PWM without Neutral Point Potential Control

In this section, the simulation results for NTV-PWM without neutral point potential control are presented. The redundant small voltage vectors are utilized in equal time length. This means that the redundancy function of the small voltage vectors α is equal to 0.5. The constant V/f ratio controlled motor drive reference motion profile and actual motor speed waveforms are shown in Figure 4.50 for low modulation index (corresponding to low speed). The motor speed has oscillations during acceleration and the oscillations disappear at steady-state. The actual motor speed approaches but can not reach the reference speed profile (the difference is the slip frequency). In the simulations, there is no speed feedback signal provided for speed error compensation (open-loop operation). For the fan load, the corresponding induction motor torque is shown in Figure 4.51. The motor torque has oscillations, because the motor is operated in open-loop speed control mode. In Figure 4.52, one of the motor phase currents is illustrated. As seen from the figure, the motor phase current has small amount of low frequency harmonics during the acceleration (due to open-loop operation). At steady-state, the low frequency harmonics disappear from the phase current waveform.

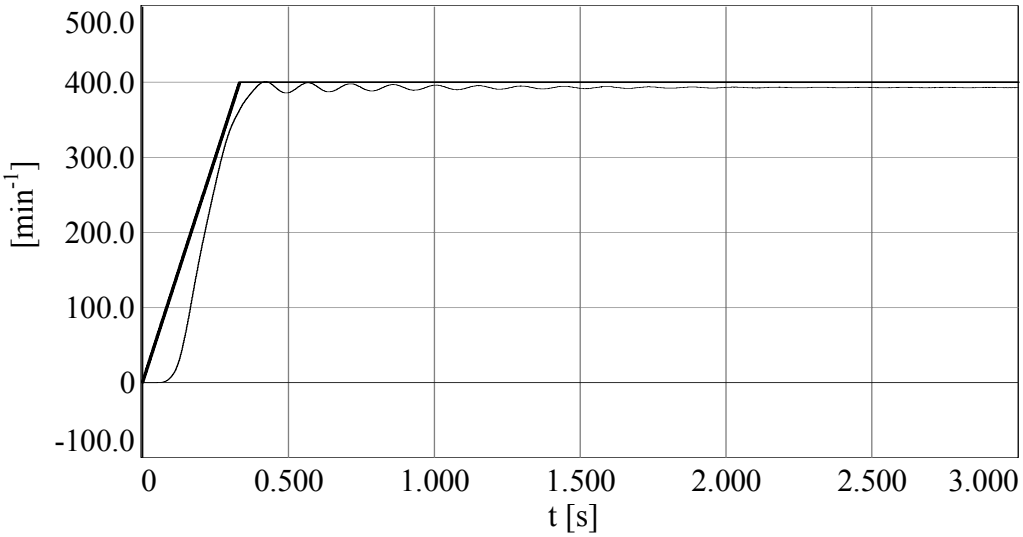


Figure 4.50 Reference speed (bold) and actual motor speed for low M_i (400 min^{-1} and M_i=0.27).

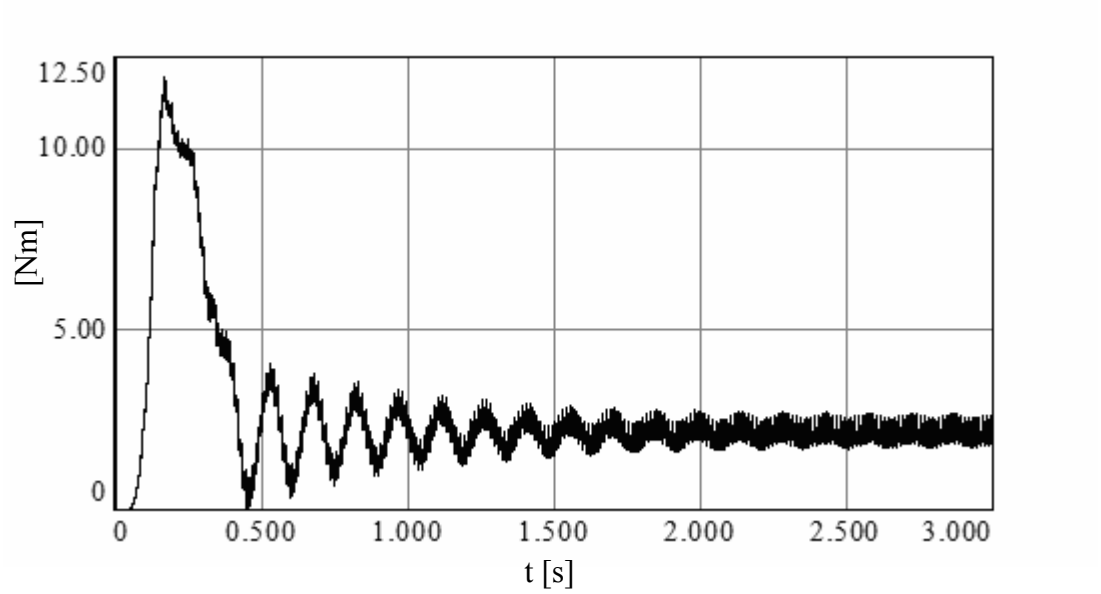


Figure 4.51 Induction motor developed torque for low M_i (400 min^{-1} and M_i=0.27).

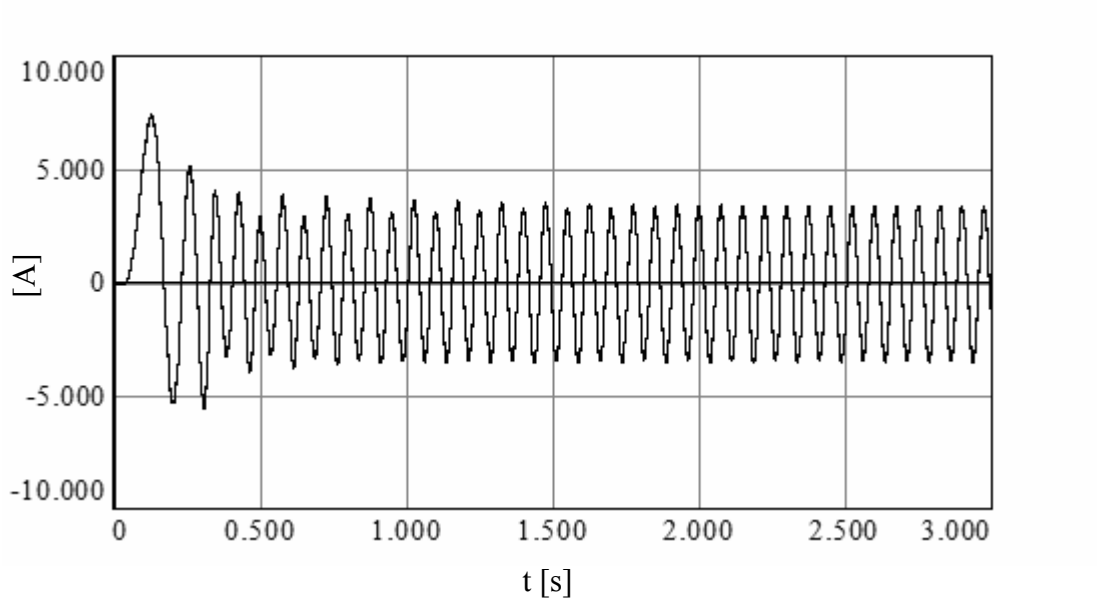


Figure 4.52 Induction motor phase current for low M_i (400 min^{-1} and M_i=0.27).

At 400 min^{-1} (which is a low operating speed that involves the inner hexagon), the drive neutral point potential behavior is illustrated in Figure 4.53 and Figure 4.54. As seen from Figure 4.53, the neutral point current consists of pulses created by the PWM switching of the inverter. The resulting current waveform appears to be AC and with no DC-offset. However, the neutral point potential which involves the integral value of the neutral point current contains a small amount of DC-offset. As seen from Figure 4.54, the neutral point potential drift over several seconds is not significant. However, this simulation illustrates over a long time period and with larger motor currents, the drift may increase to prohibitive levels. Longer duration system behavior could not be investigated by means of computer simulations due to the computational speed and computer memory allocation constraints. Therefore, the long duration neutral point potential drift could not be proven by means of simulations. However, the study conducted is sufficient to demonstrate that the neutral point potential does not remain fixed and is prone to drift. In this low modulation index operating range where only the inner triangles (triangle 1 in Figure 3.10) are utilized, the drift is due to the small voltage vectors since in this range the medium voltage vector is not utilized. Therefore, the neutral point potential does not contain dominant triplen harmonic components. In Figure 4.55, the neutral point potential is shown in a zoomed window. As expected, there is a small ripple on the

neutral point potential and its frequency is equal to the PWM frequency. Thus, the drift is slow and not visible in a few PWM cycles. In Figure 4.56, the fundamental frequency range behavior of the neutral point potential is illustrated. As shown in the figure, the phase current is nearly free of ripple. The nearly sinusoidal current is due to the small voltage vectors that create an output voltage with low harmonic content. The line-to-line output voltage waveform of the three-level NPC inverter has three voltage levels at low modulation indices (M_i<0.5), as shown in Figure 4.57. The three-level NPC inverter acts like a two-level inverter with half of the DC bus of the three-level total DC bus voltage. Thus, the line-to-line output voltage has half the magnitude of the full DC bus. In Figure 4.57, the line-to-line output voltage waveform appears to have a slight distortion that implies that the capacitor voltage is varying by a few per-cent. However, it has been found that this distortion is based on a graphic window illustration failure of Ansoft-Simplorer and the real numerical data does not have any noticeable distortion. Thus, the capacitor voltages do not have any noticeable voltage ripple and the inverter output line-to-line voltage has low distortion leading to nearly sinusoidal motor phase currents.

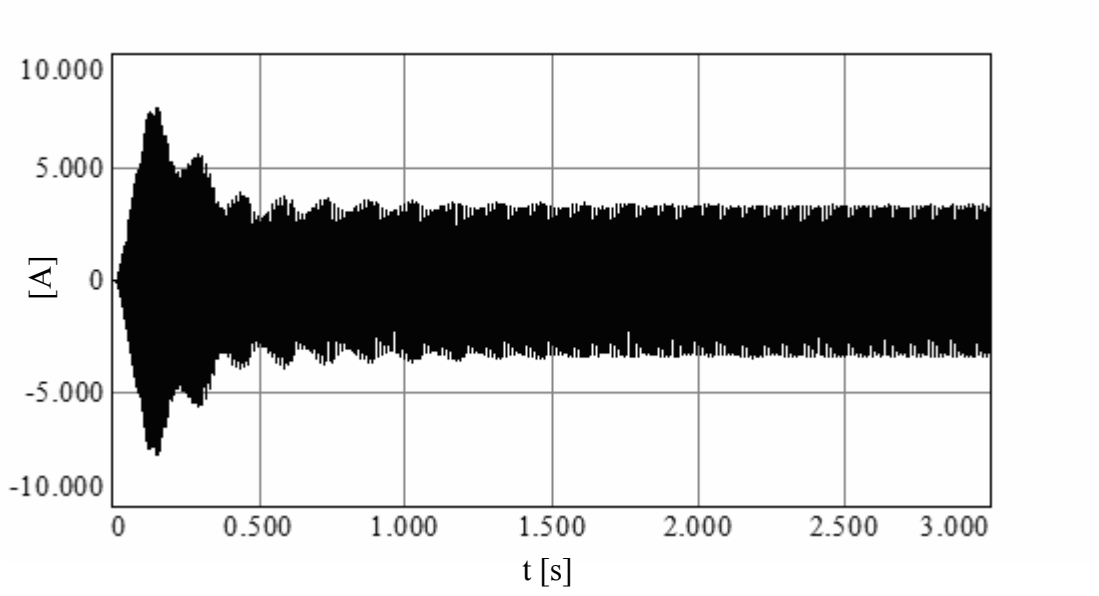


Figure 4.53 The neutral point current waveform at high M_i (400 min^{-1} and M_i=0.27) for NTV-PWM without neutral point potential control (α=0.5).

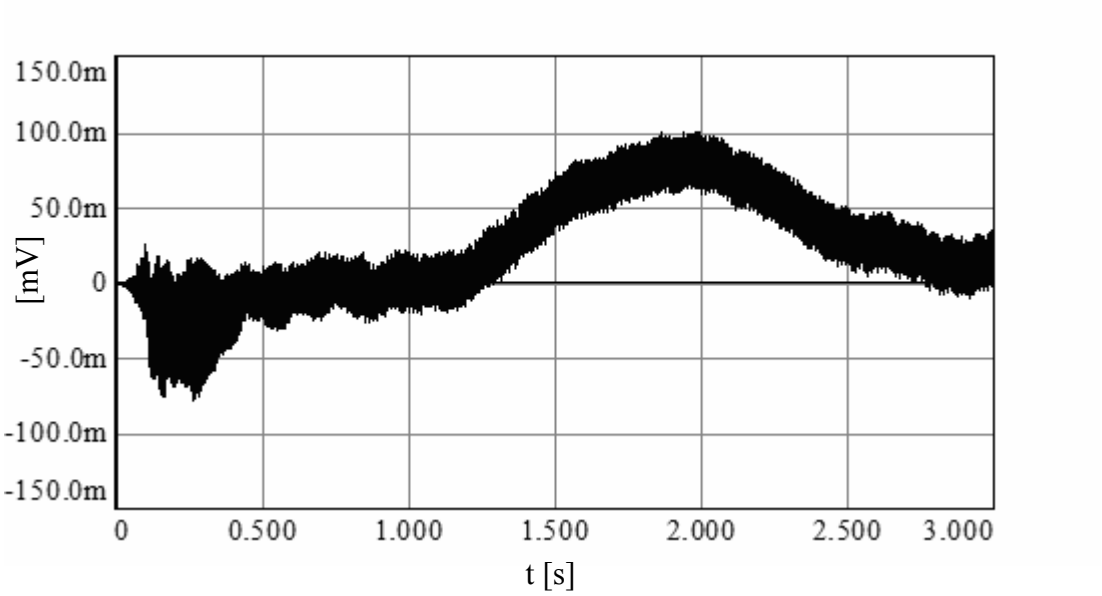


Figure 4.54 The neutral point potential waveform at low M_i (M_i=0.27) for NTV-PWM without neutral point potential control (α=0.5).

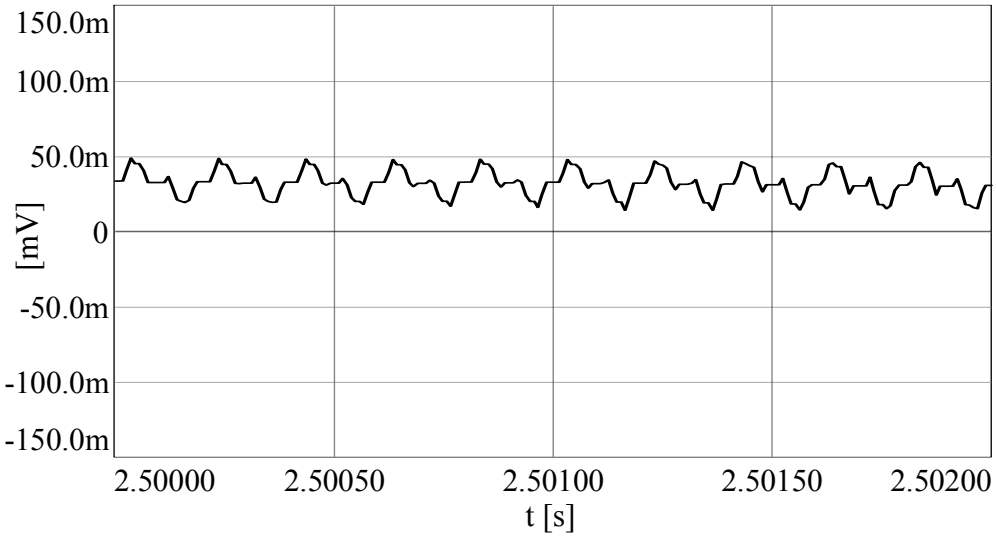


Figure 4.55 The zoom-in view of the neutral point potential waveform at steady-state and low M_i (M_i=0.27) for NTV-PWM without neutral point potential control (α=0.5).

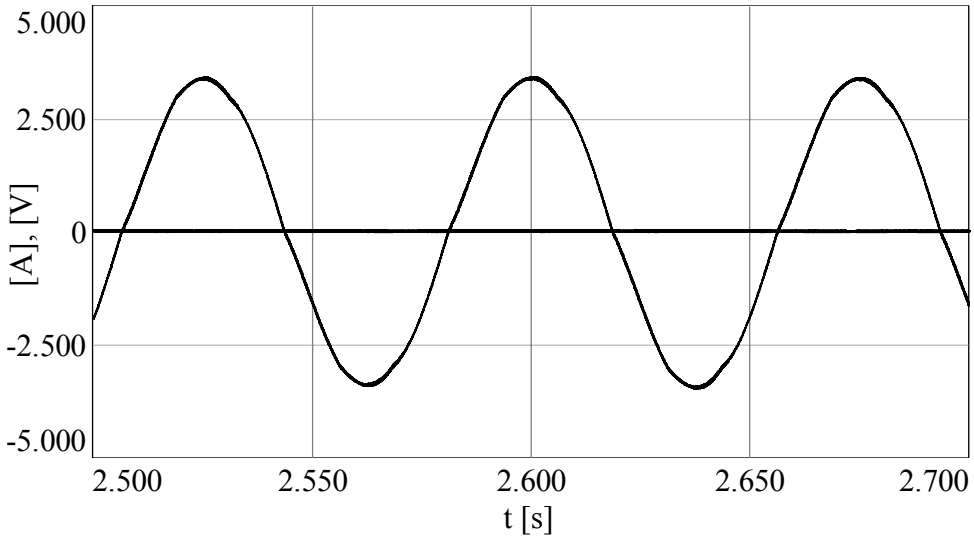


Figure 4.56 The neutral point potential (bold) and the phase current at steady-state and low M_i (M_i=0.27) for NTV-PWM without neutral point potential control (α=0.5).

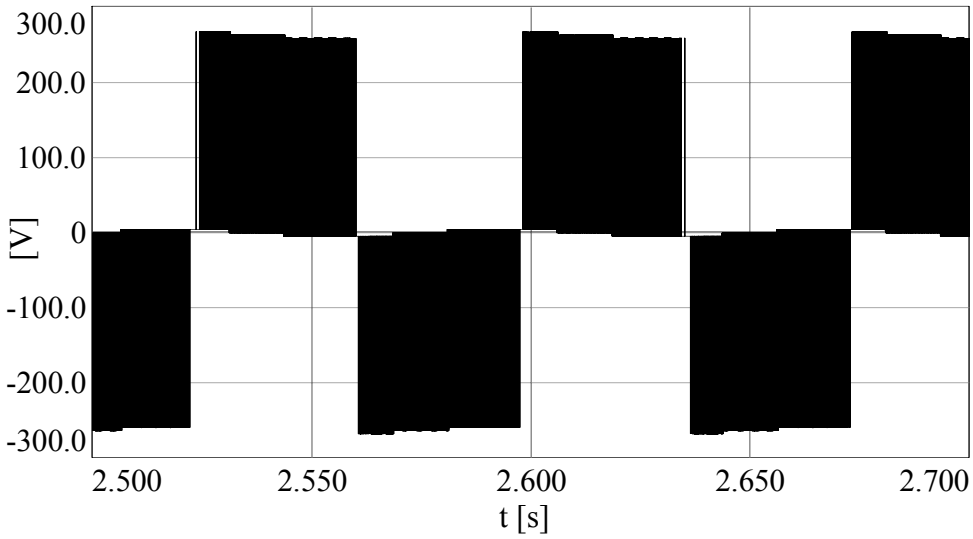


Figure 4.57 The line-to-line output voltage waveform of the three-level NPC inverter at steady-state and low M_i (M_i=0.27)for NTV-PWM without neutral point potential control (α=0.5).

At high modulation index, the inverter drive and the neutral point potential behave differently from the low modulation index range. To illustrate the behavior the motor

drive is simulated with 1400 min^{-1} final value speed reference. The reference and actual speed profiles are shown in Figure 4.58. The motor speed is less than the reference due to the slip frequency. The motor drives the fan load. The developed torque is illustrated in Figure 4.59. Corresponding to the motor torque, one of the motor phase currents waveform is illustrated in Figure 4.60. The resulting neutral point current waveform is illustrated in Figure 4.61 and being proportional to the integral of the neutral point current, the neutral point potential waveform is shown in Figure 4.62. As seen from Figure 4.62, the neutral point potential does not have any significant drift. The reason is that the small voltage vectors are utilized less than the low modulation index case. However, the neutral point potential has a dominant triplen harmonic component for the high modulation index case. Figure 4.63 shows the load current and the neutral point potential in the same window to illustrate the triplen harmonic content of the neutral point potential. The triplen harmonic content is injected by the medium voltage vector. In NTV-PWM, the triplen harmonic component can not be compensated for and the magnitude of the triplen harmonic depends on the load current magnitude, load power factor, and modulation index. The magnitude of triplen harmonic has the largest value at full-load case. In Figure 4.64, line-to-line output voltage waveform of the three-level NPC inverter is shown and it has five levels. As a result of the five-level line-to-line voltage waveform the corresponding load current is nearly a pure sinusoid, as shown in Figure 4.63.

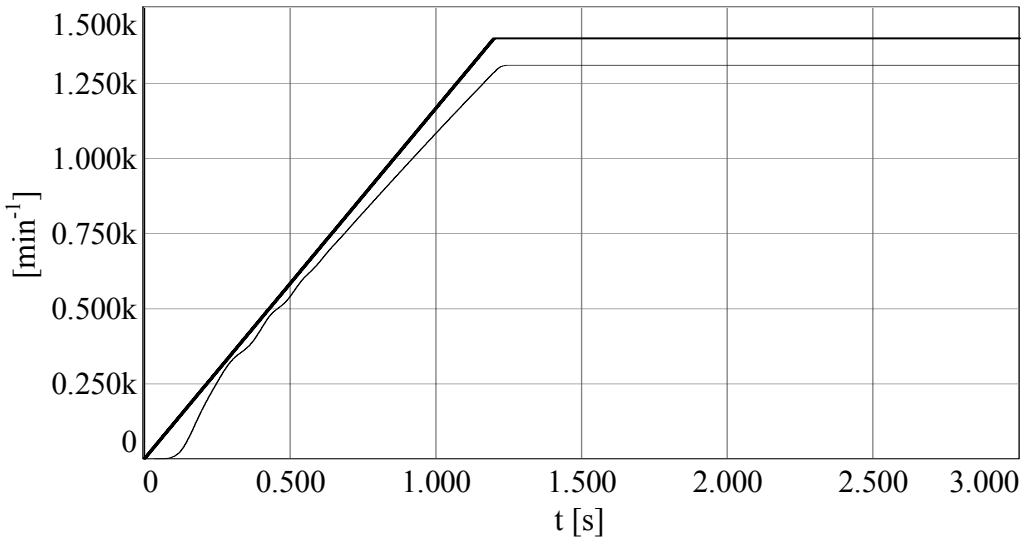


Figure 4.58 Reference speed profile (bold) and actual motor speed for high M_i (1311 min^{-1} and M_i=1.0).

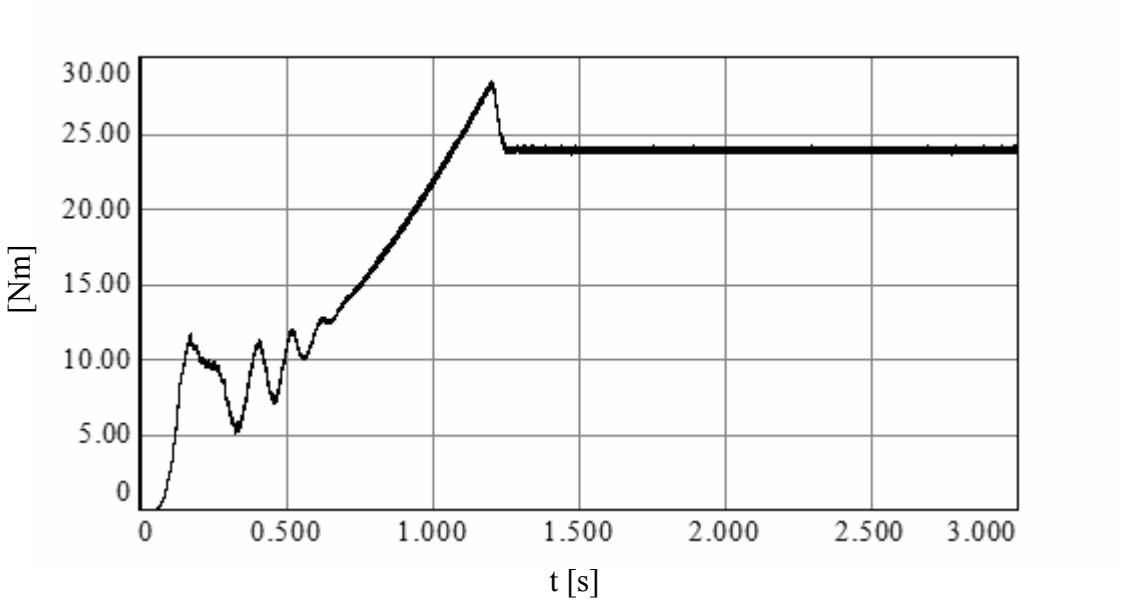


Figure 4.59 Induction motor produced torque for high M_i (1311 min^{-1} and M_i=1.0).

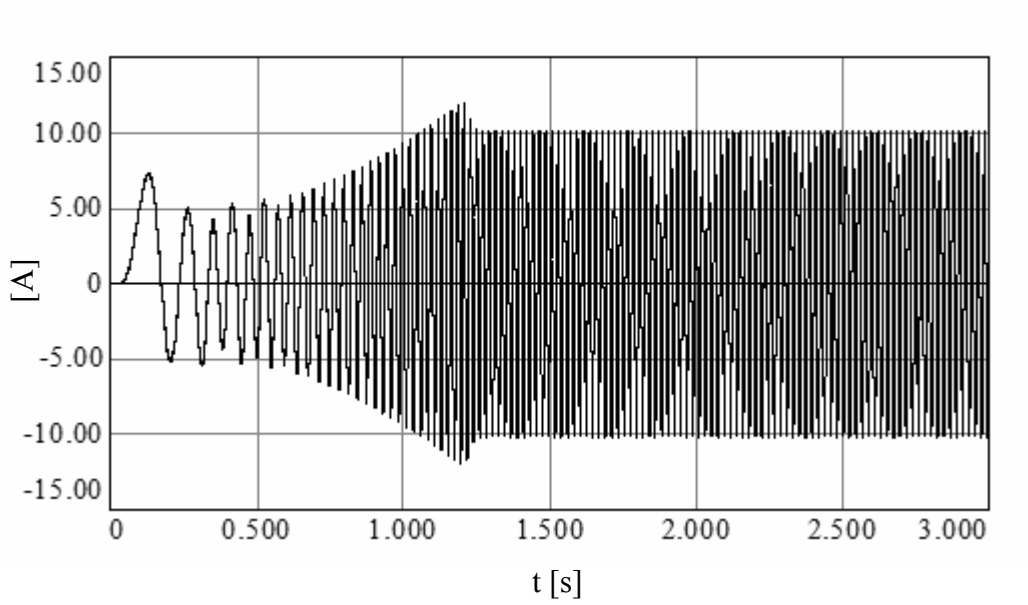


Figure 4.60 Induction motor phase current for high M_i (1311 min^{-1} and M_i=1.0).

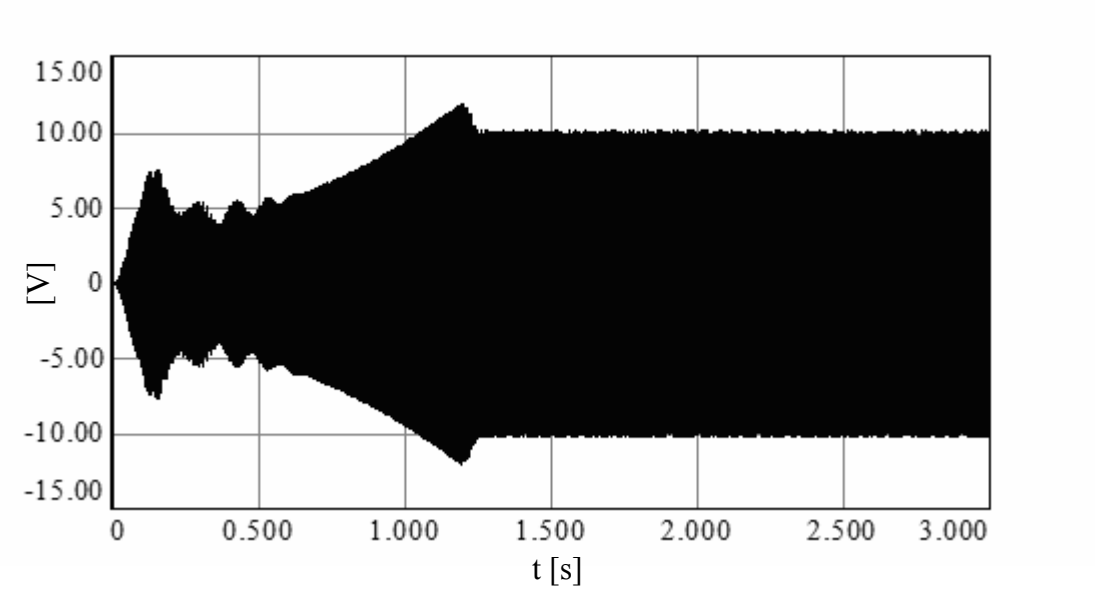


Figure 4.61 The neutral point current waveform at high M_i (1311 min^{-1} and M_i=1.0) for NTV-PWM without neutral point potential control (α=0.5).

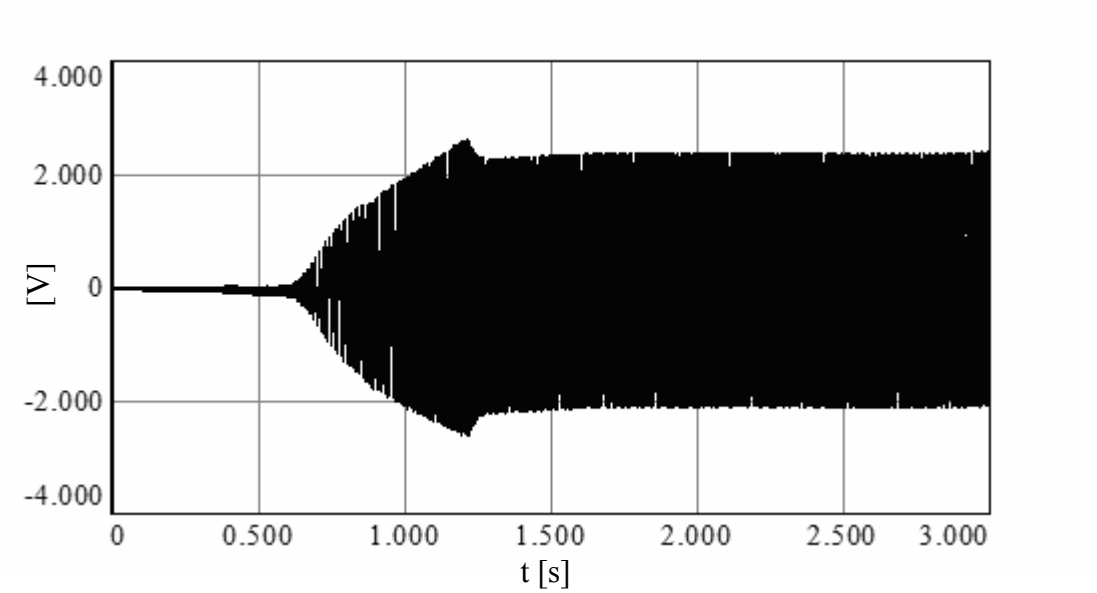


Figure 4.62 The neutral point potential waveform at high M_i (M_i=1.0) for NTV-PWM without neutral point potential control (α=0.5).

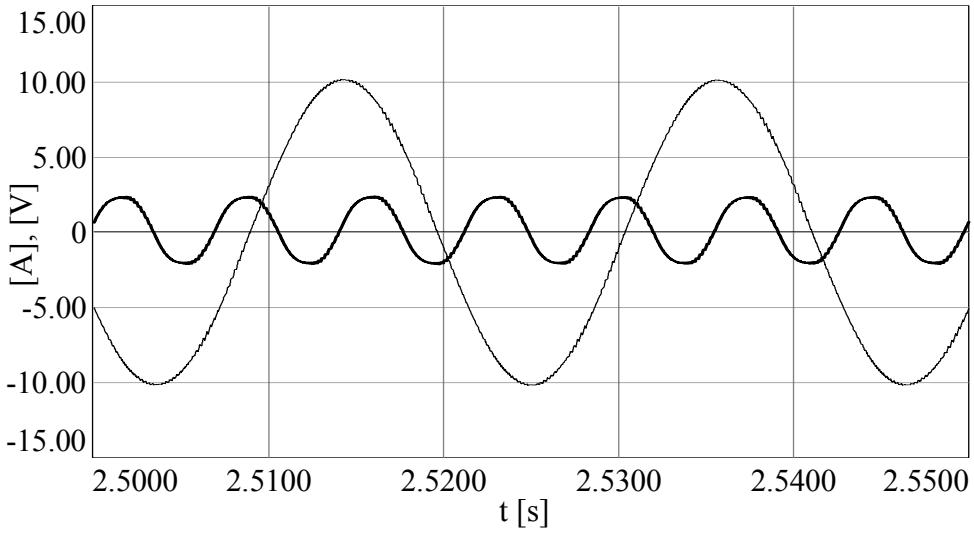


Figure 4.63 The neutral point potential (bold) and the phase current at steady-state and high M_i (M_i=1.0) for NTV-PWM without neutral point potential control (α=0.5).

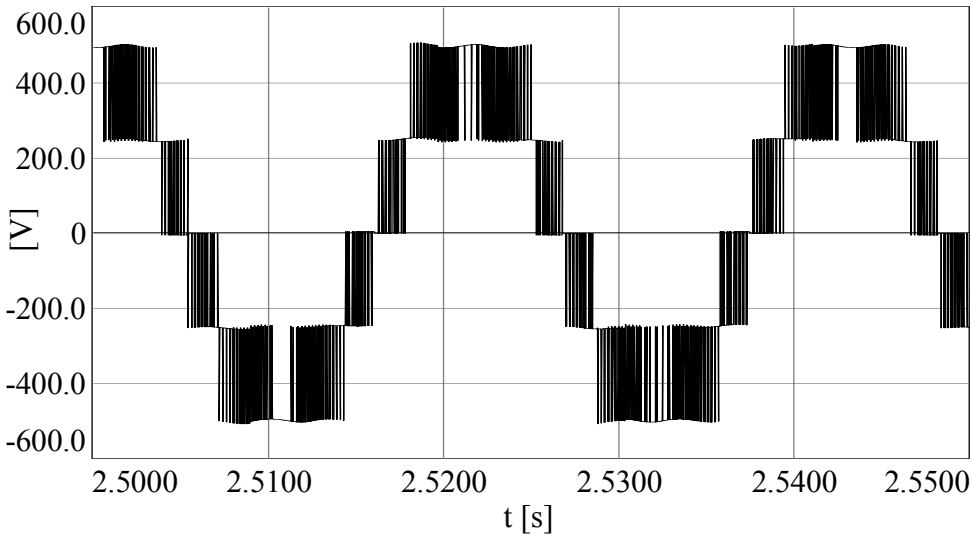


Figure 4.64 The line-to-line output voltage waveform of the three-level NPC inverter at steady-state and high M_i (M_i=1) for NTV-PWM without neutral point potential control (α=0.5).

4.5.2 NTV-PWM with The Uniform α Control Method

This section presents the induction motor drive simulation results of the NTV-PWM with uniform α control method ($\alpha=\alpha_1=\alpha_2$ and $\gamma=1$) for low modulation ($M_i=0.27$ corresponding to ω_r^*=400 min^{-1}) and high modulation ($M_i=1.0$ corresponding to ω_r^*=1400 min^{-1}) operating conditions. In terms of motor speed, torque, and phase current characteristics, the results are practically the same as in the uncontrolled neutral point potential case of 4.5.1. The differences between the waveforms are insignificant and indistinguishable to the human eye. Therefore, the motor speed, torque, current, etc. related behavior will not be discussed and waveforms will not be shown for the sake of brevity. Thus, focus will be placed on the neutral point current and potential waveforms.

First, the drive behavior at 400 min^{-1} is investigated. In Figure 4.65, the neutral point current waveform is illustrated. As seen from the figure, the neutral point current has no DC component and it consists of rectangular current pulses due to PWM operation. Figure 4.66 shows the neutral point potential. As seen from the figure, the neutral point potential fluctuates around zero and unlike the NTV-PWM method without neutral point potential control ($\alpha=0.5$) there is no potential drift. In this case, the small voltage vectors are utilized a manner to keep the neutral point potential around the zero voltage level. Also at steady-state there is no dominant triplen harmonic content on the neutral point potential as shown in Figure 4.67. Because the medium voltage vector is not employed in the inner hexagon of the three-level output voltage space vector. The neutral point potential oscillation is kept within a small range by the uniform α controller dynamically, and the ripple frequency is the PWM frequency. In Figure 4.68, the redundancy function α is illustrated at steady-state. As seen from the figure, the redundancy function α has values around 0.5. In Figure 4.69, the phase current and the neutral point potential are shown in the same graph. The phase current is nearly sinusoidal. The line-to-line output voltage waveform is same as the NTV-PWM without neutral point potential control case, as shown in Figure 4.70.

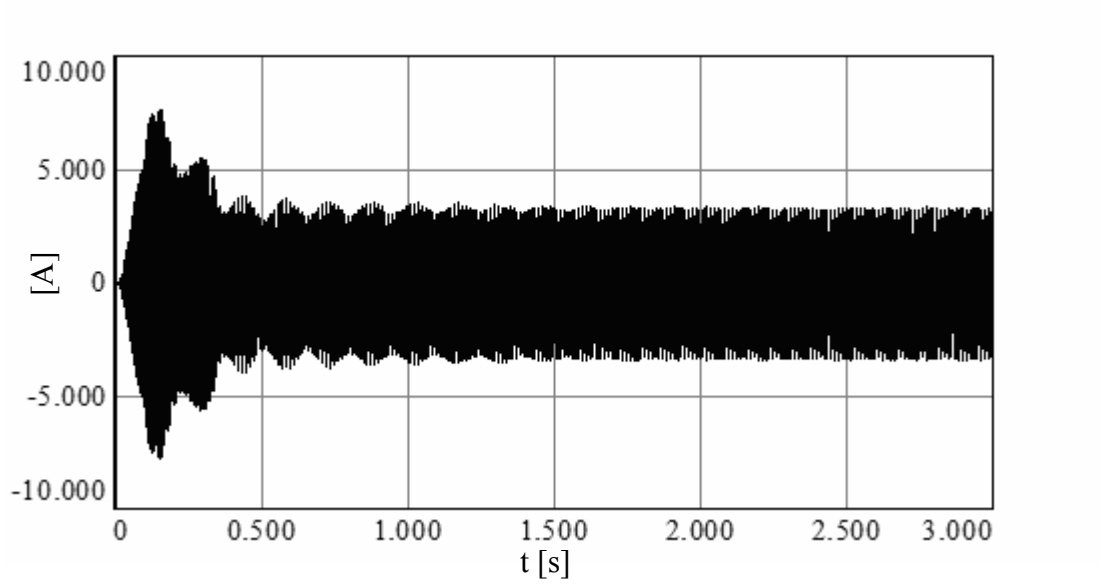


Figure 4.65 The neutral point current waveform at low M_i (M_i=0.27) for NTV-PWM with the uniform α control method.

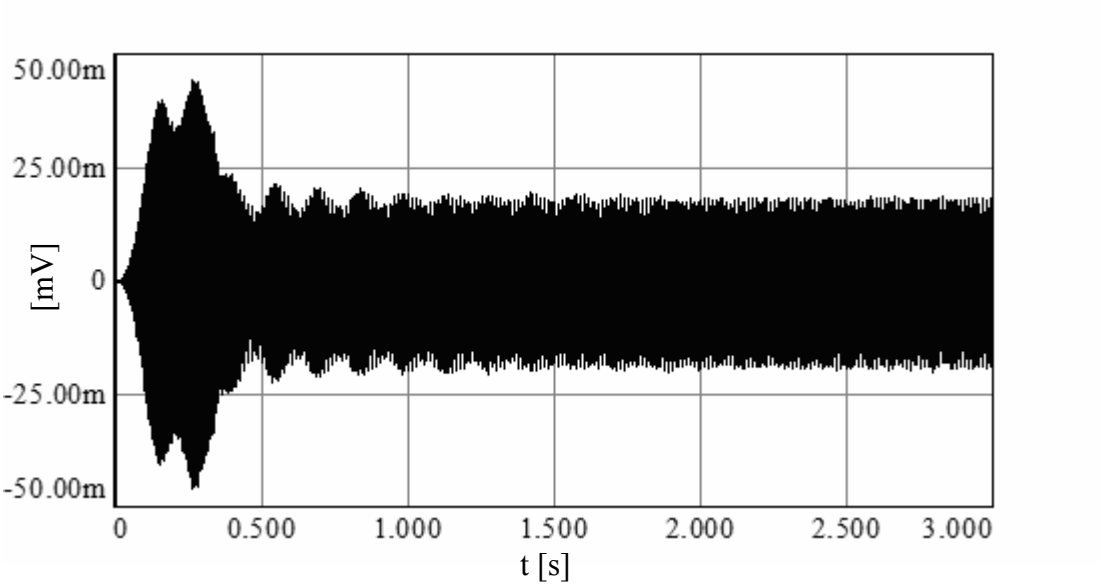


Figure 4.66 The neutral point potential waveform at low M_i (M_i=0.27) for NTV-PWM with the uniform α control method.

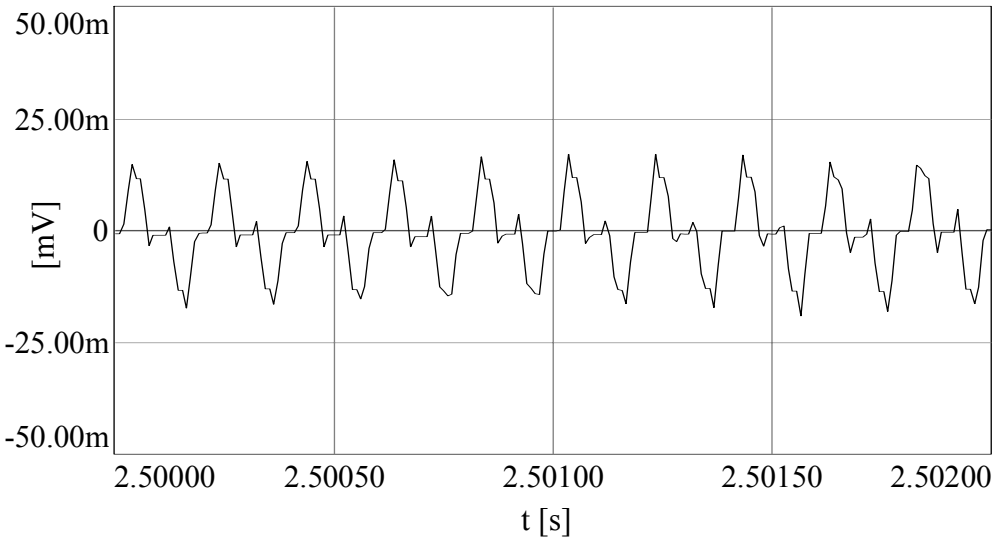


Figure 4.67 The zoom-in view of the neutral point potential waveform at steady-state and low M_i (M_i=0.27) for NTV-PWM with the uniform α control method.

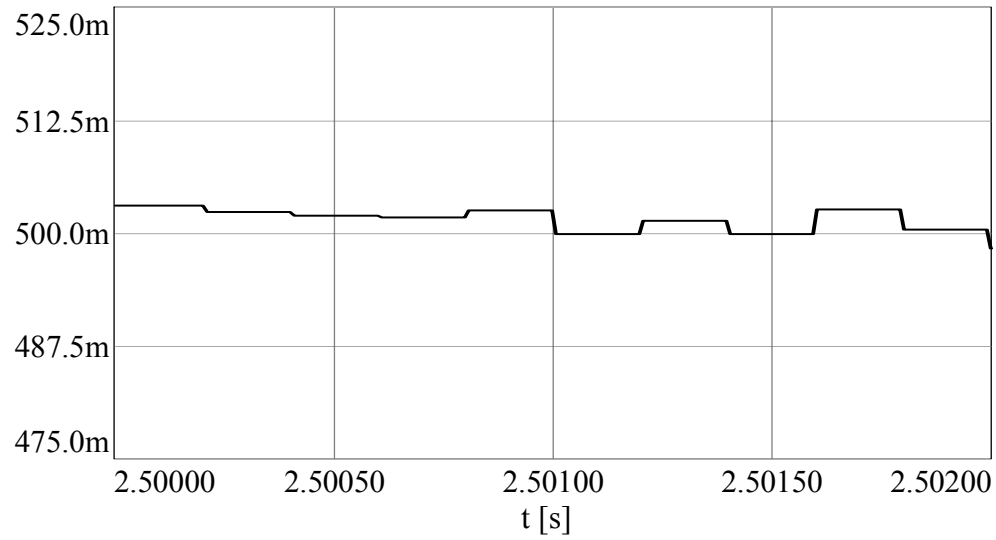


Figure 4.68 The redundancy function α of the uniform α control method at steady-state (M_i=0.27).

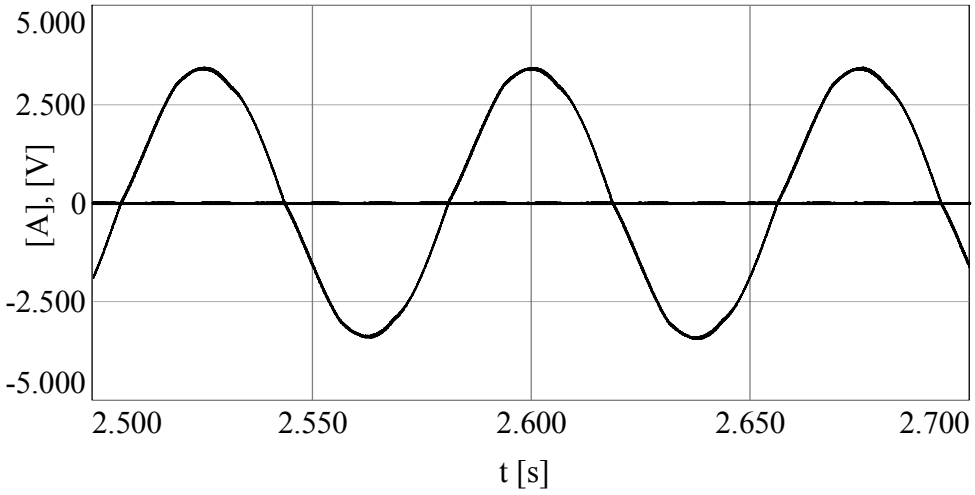


Figure 4.69 The neutral point potential (bold) and the motor current at steady-state and low M_i (M_i=0.27) for NTV-PWM with the uniform α control method.

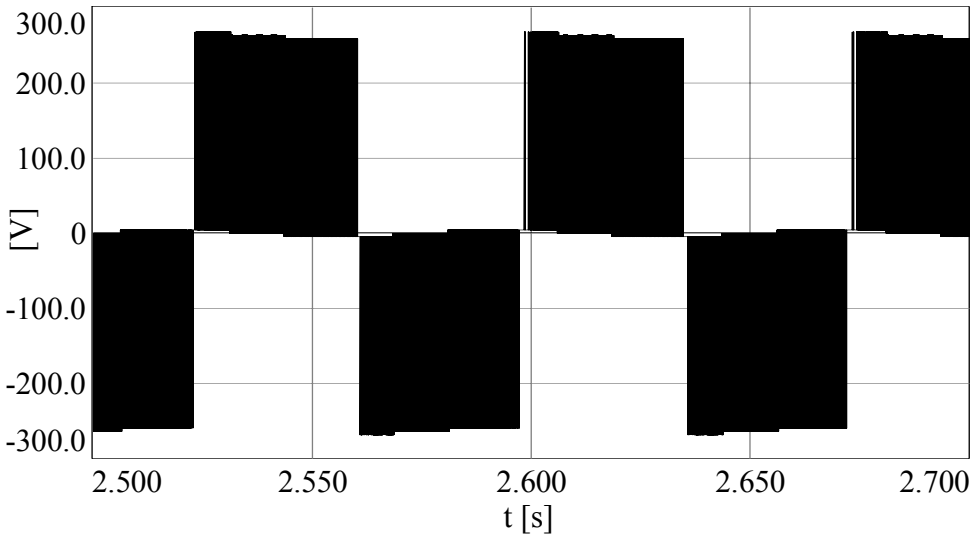


Figure 4.70 Line-to-line output voltage waveform of the three-level NPC inverter at steady-state and low M_i (M_i=0.27) for the uniform α control method.

Second, the drive behavior at 1400 min^{-1} is investigated. In Figure 4.71, the neutral point current waveform is illustrated. As seen from the figure, the neutral point current has no DC component and it consists of rectangular current pulses due to

PWM operation. Figure 4.72 shows the neutral point potential. Figure 4.73 shows the zoom-in view of the neutral point potential along with the phase current waveform at steady-state. As seen from Figure 4.72, the neutral point potential has no drift. The small voltage vectors are employed less and the medium voltage vector is dominant. Therefore, the triplen harmonic content is dominant, as shown in Figure 4.73. As a result the redundancy function α reaches the limit values of 1 or 0 in an attempt to eliminate the neutral point potential error, as shown in Figure 4.74. Even for limit values of the redundancy function α, the uniform α neutral point potential control method is not capable of fully compensating for the triplen harmonic component. As seen from Figure 4.73, the phase current is nearly sinusoidal and as seen from Figure 4.75, the line-to-line output voltage is the same as NTV-PWM without neutral point potential control (Figure 4.64).

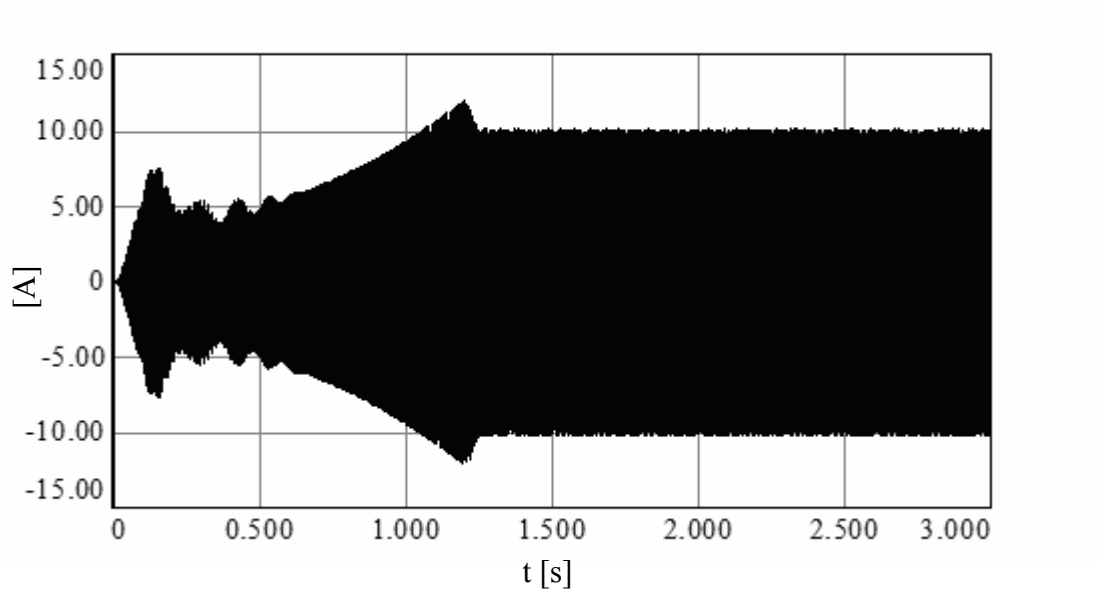


Figure 4.71 The neutral point current waveform at high M_i (M_i=1.0) for NTV-PWM with the uniform α control method.

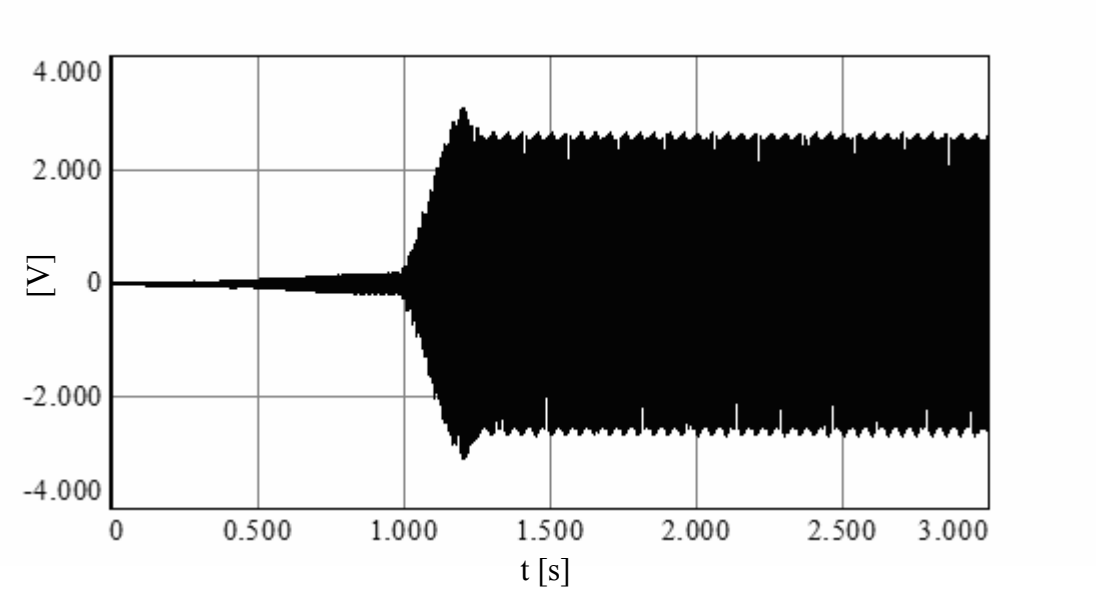


Figure 4.72 The neutral point potential waveform at high M_i (M_i=1.0) for NTV-PWM with the uniform α control method.

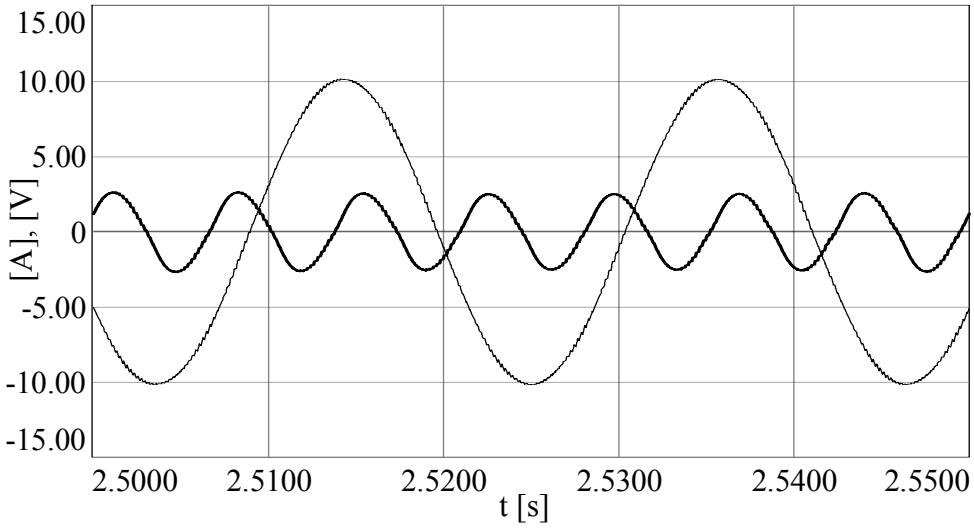


Figure 4.73 The neutral point potential (bold) and the motor current waveform at steady-state and high M_i (M_i=1.0) for NTV-PWM with the uniform α control method.

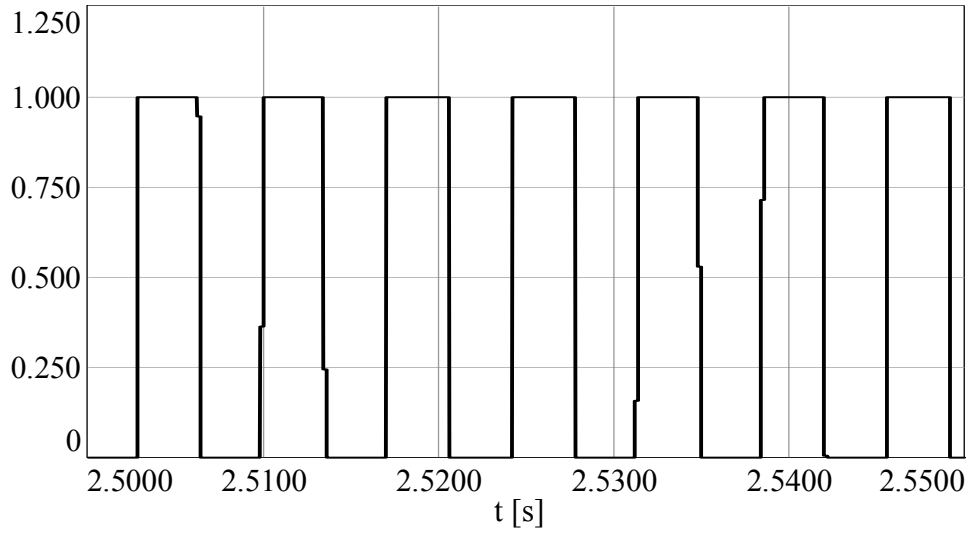


Figure 4.74 The redundancy function α of the uniform α control method at steady-state (M_i=1.0).

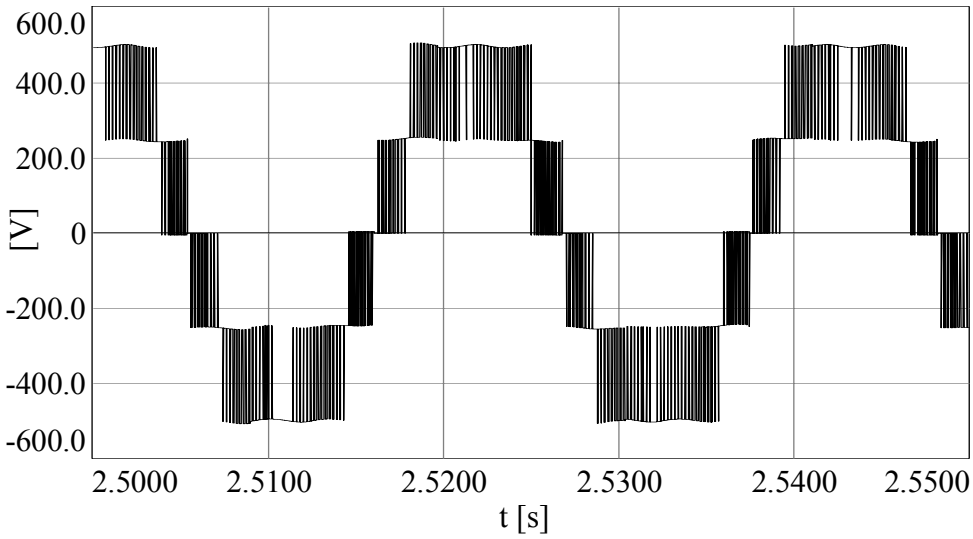


Figure 4.75 The line-to-line output voltage waveform of the three-level NPC inverter at steady state and high M_i (M_i=1.0) for the uniform α control method.

4.5.3 NTV-PWM with The Optimal α Control Method

This section presents the induction motor drive simulation results of NTV-PWM with the optimal α control method for low modulation (M_i=0.27 corresponding to ω_r^*=400 min^{-1}) and high modulation (M_i=1.0 corresponding to ω_r^*=1400 min^{-1}) index operating conditions. The motor speed and torque waveforms are not shown as they are the same as those in section 4.5.1 The differences between the waveforms are insignificant and indistinguishable to the human eye. Therefore, the motor speed, torque, current, etc. related behavior will not be discussed and waveforms will not be shown for the sake of brevity. Thus, focus will be placed on the neutral point current and potential waveforms.

First, the drive behavior at 400 min^{-1} is investigated. In Figure 4.76, the neutral point current waveform is illustrated. As seen from the figure, the neutral point current has no DC component and it consists of rectangular current pulses due to PWM operation. Figure 4.77 shows the neutral point potential. As seen from the figure, the neutral point potential fluctuates around zero and there is no potential drift. In this case, the small voltage vectors are utilized a manner to obtain maximum charge from the small voltage vectors to keep the neutral point potential around the zero voltage level. In this control method the charge obtained from the small voltage vectors is maximized by coordinating redundancy functions of the small voltage vectors according to the associated phase current polarity. Also at steady-state there is no dominant triplen harmonic content on the neutral point potential as shown in Figure 4.78. The medium voltage vector is not employed in the inner hexagon of the three-level NPC inverter output voltage space vector. The neutral point potential oscillation is kept within a small range by the optimal α controller dynamically, and the ripple frequency is the PWM frequency. In Figure 4.79, the redundancy function α, α_1, and α_2 are illustrated at steady-state. As seen from the figure, the redundancy function α has values around 0.5. The redundancy function α_1 has values (1-α) and α_2 has the same values as the redundancy function α as seen from Figure 4.79.b and Figure 4.79.c, respectively. In Figure 4.80, the phase current and the neutral point potential are shown in the same graph. The phase current is nearly sinusoidal. As

shown in Figure 4.81, the line-to-line output voltage waveform is same as the NTV-PWM without neutral point potential control case.

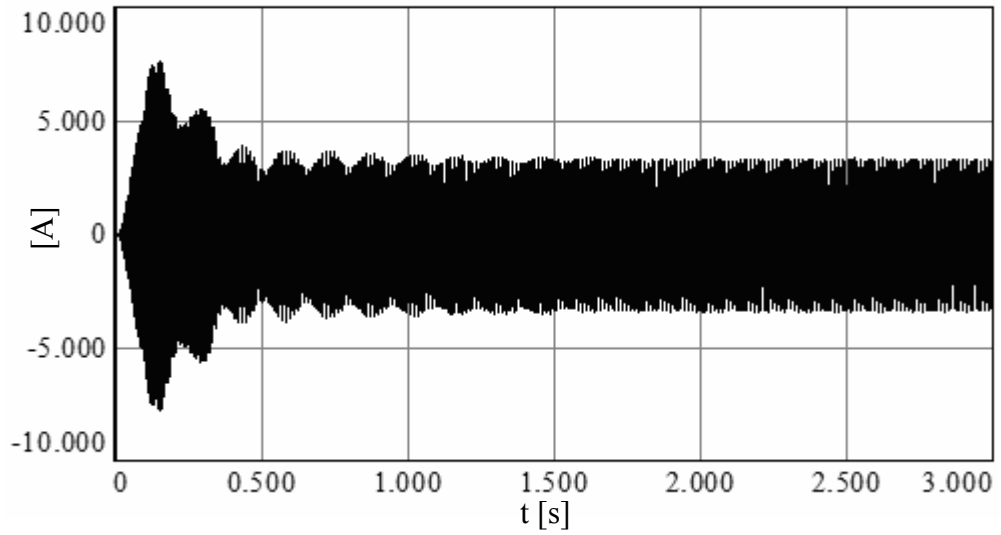


Figure 4.76 The neutral point current waveform at low M_i (M_i=0.27) for the NTV-PWM with the optimal α control method.

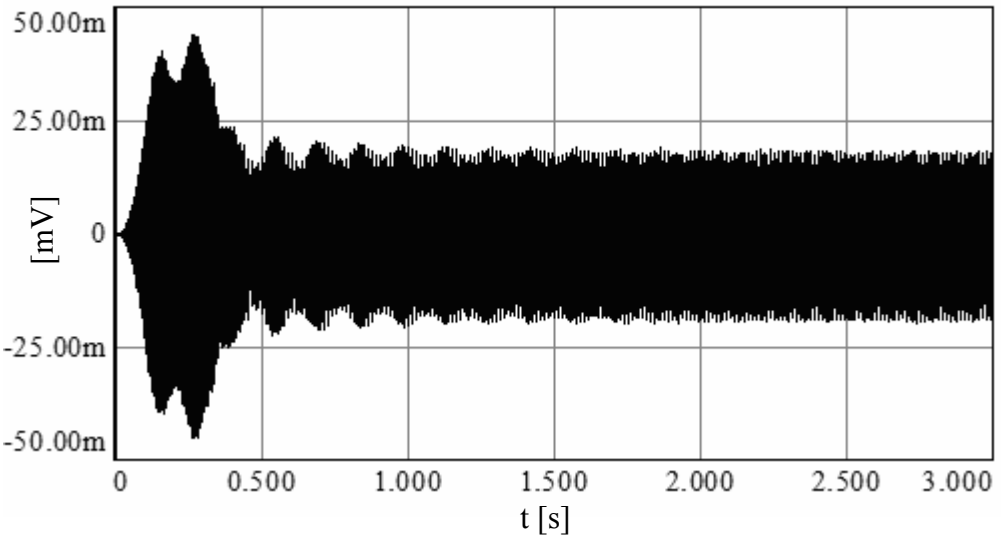


Figure 4.77 The neutral point potential waveform at low M_i (M_i=0.27) for NTV-PWM with the optimal α control method.

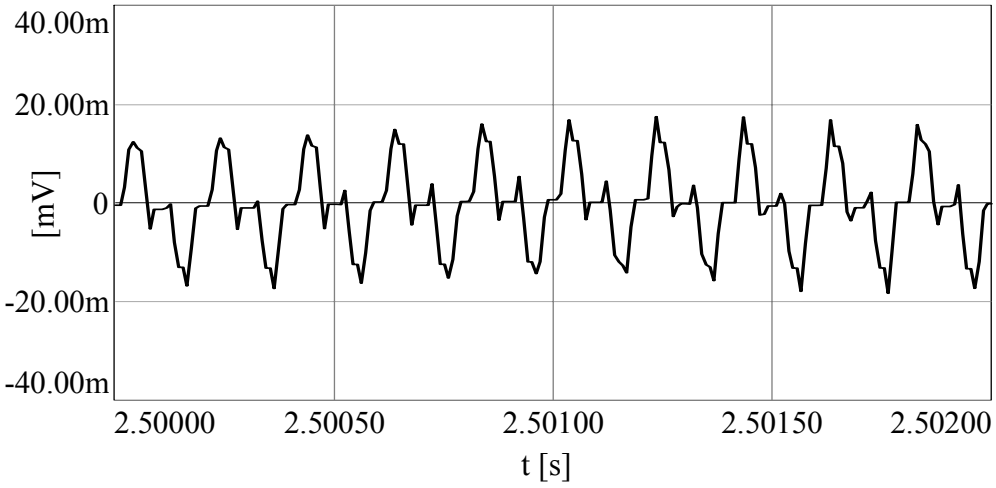
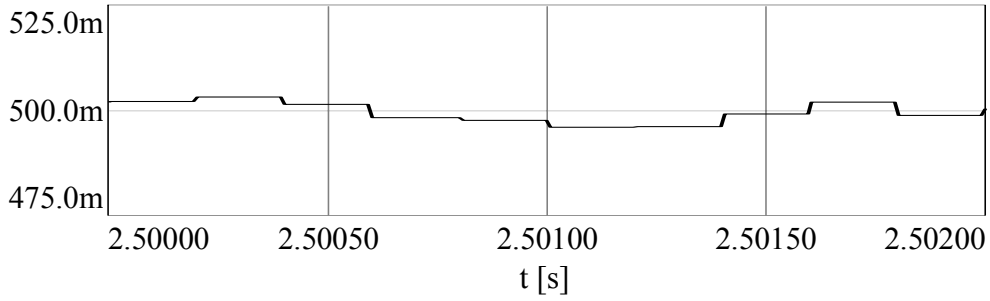
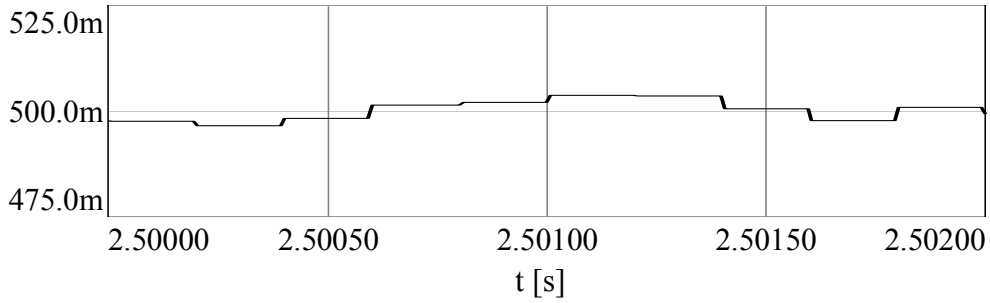


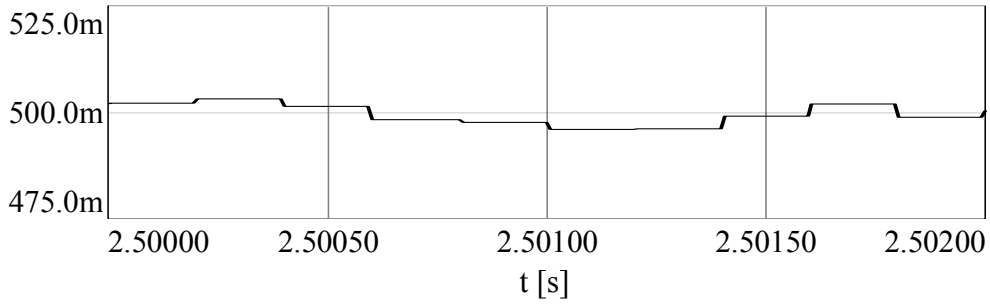
Figure 4.78 The zoom-in view of the neutral point potential waveform at steady-state and low M_i (M_i=0.27) for NTV-PWM with the optimal α control method.



(a) α



(b) α_1



(c) α_2

Figure 4.79 The redundancy function α of the optimal α control method at steady-state (M_i=0.27).

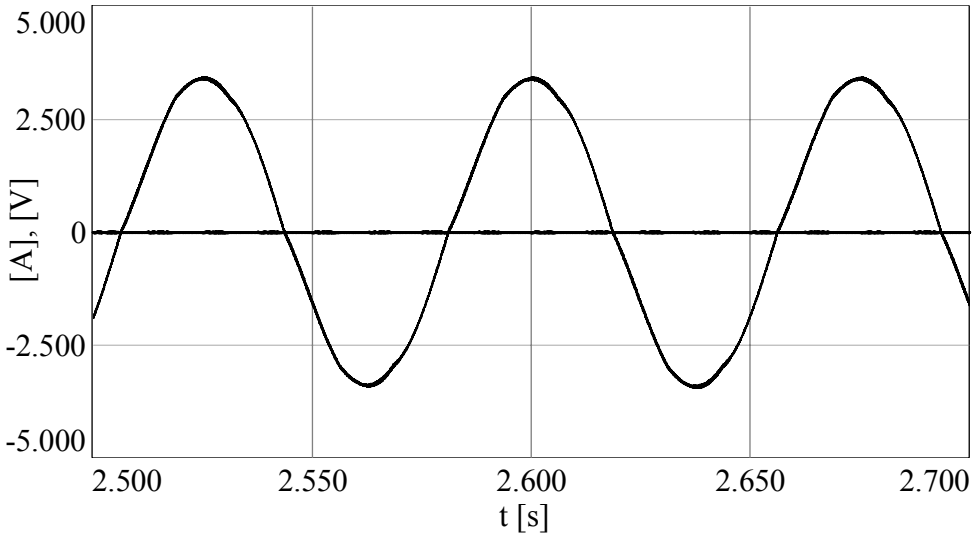


Figure 4.80 The neutral point potential (bold) and the motor current at steady-state and low M_i (M_i=0.27) for NTV-PWM with the optimal α control method.

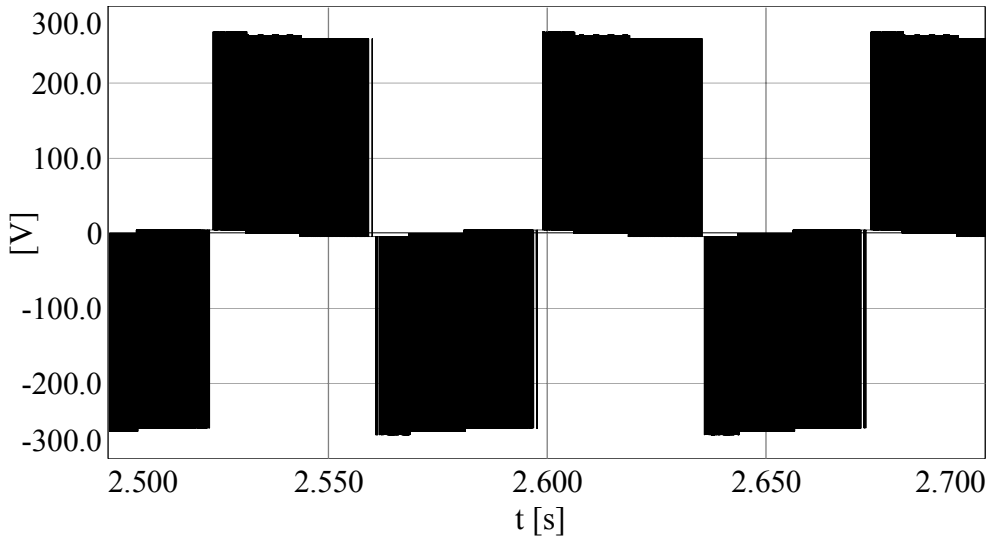


Figure 4.81 The line-to-line output voltage waveform of the three-level NPC inverter at steady-state and low M_i (M_i=0.27) for NTV-PWM with the optimal α control method.

Second, the drive behavior at 1400 min^{-1} is investigated. In Figure 4.82, the neutral point current waveform is illustrated. Figure 4.83 shows the neutral point potential.

Figure 4.84 shows the zoom-in view of the neutral point potential along with the phase current waveform at steady-state. As seen from Figure 4.83, the neutral point potential has no drift. The small voltage vectors are employed less and the medium voltage vector is dominant. Therefore, the triplen harmonic content is dominant, as shown in Figure 4.84. As a result the redundancy function α reaches the limit values of 1 or 0 in an effort to eliminate the neutral point potential error, as shown in Figure 4.85. Even for the limit values of the redundancy function α, the maximum charge available from the small voltage vectors is not sufficient to fully compensate for the triplen harmonic component charge. As seen from Figure 4.84, the phase current is nearly sinusoidal and as seen from Figure 4.86, the line-to-line output voltage is the same as the NTV-PWM without neutral point potential control case (Figure 4.64). In the figure, the 300 Hz (six times the line frequency of 50 Hz) ripple on the line-to-line voltage magnitude is due to the six-pulse diode rectifier bridge with limited DC bus capacitive filtering. In Figure 4.85 there are rare glitches in the α waveforms that correspond to the phase current polarity change (zero current crossing). These glitches have no effect on the controller performance as the associated current is near zero and has practically negligible effect on the neutral point potential.

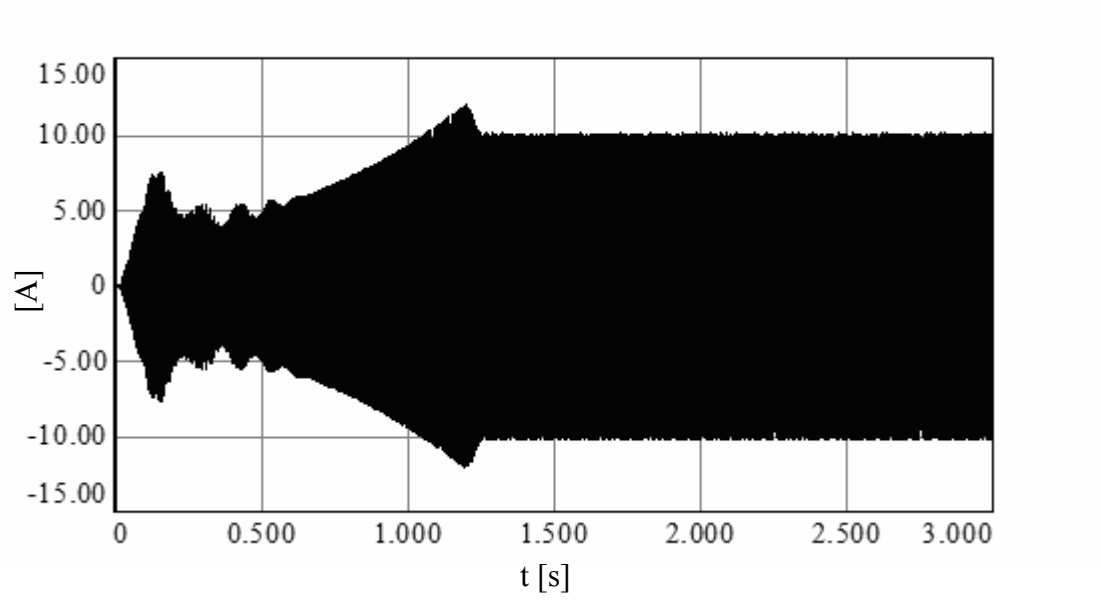


Figure 4.82 The neutral point current waveform at high M_i (M_i=1.0) for the NTV-PWM with optimal α control method.

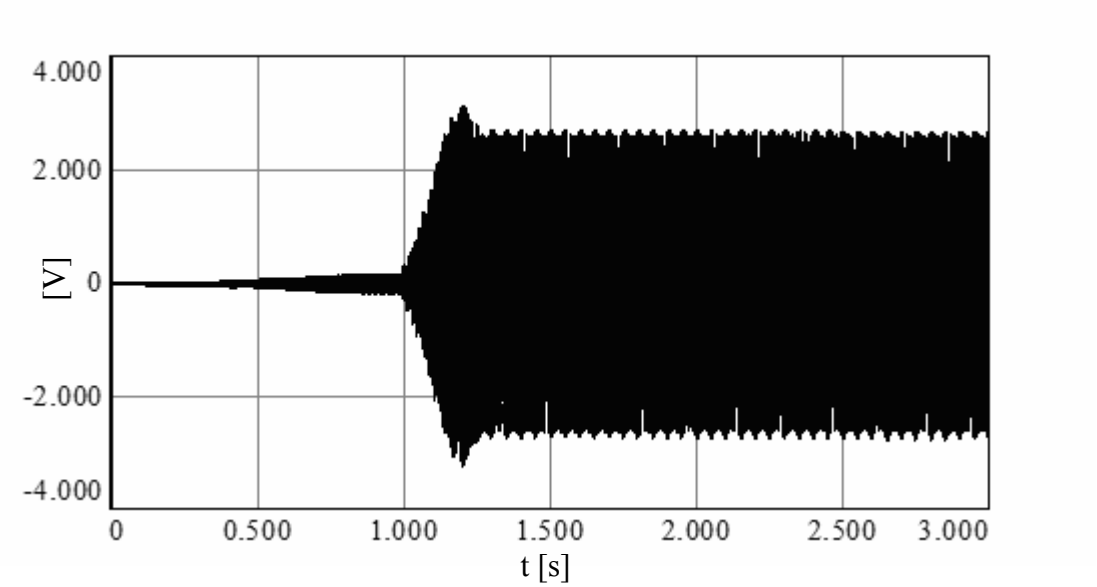


Figure 4.83 The neutral point potential waveforms at high M_i (M_i=1) for NTV-PWM with the optimal α control method.

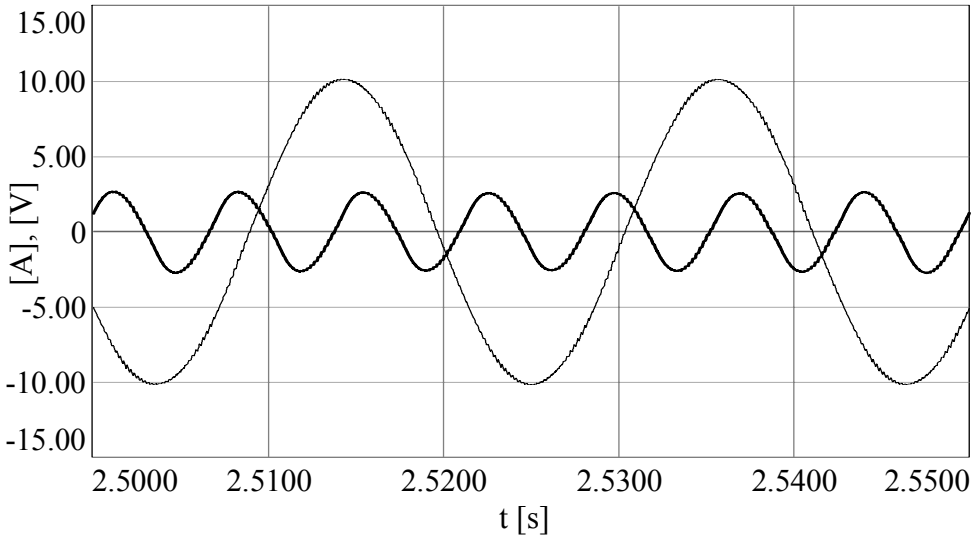
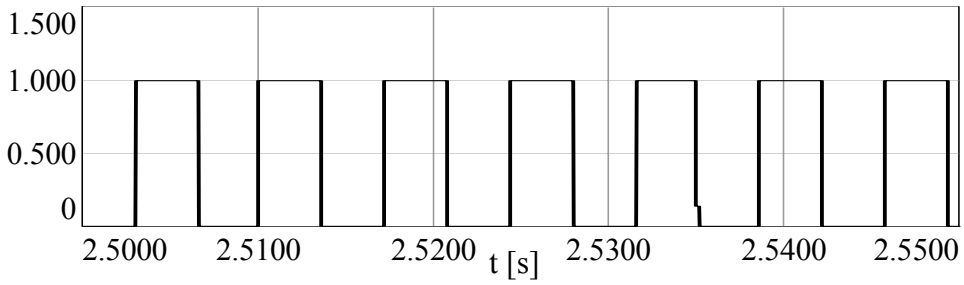
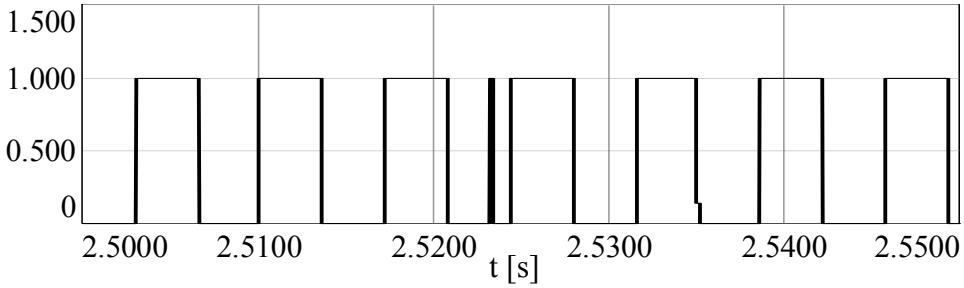


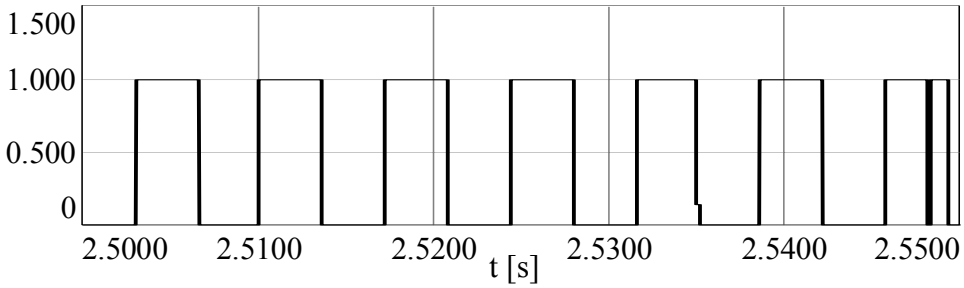
Figure 4.84 The neutral point potential (bold) and the motor current at steady-state and high M_i (M_i=1) for NTV-PWM with the optimal α control method.



(a) α_o



(b) α_1



(c) α_2

Figure 4.85 The redundancy function α of the optimal α control method at steady-state (M_i=1.0).

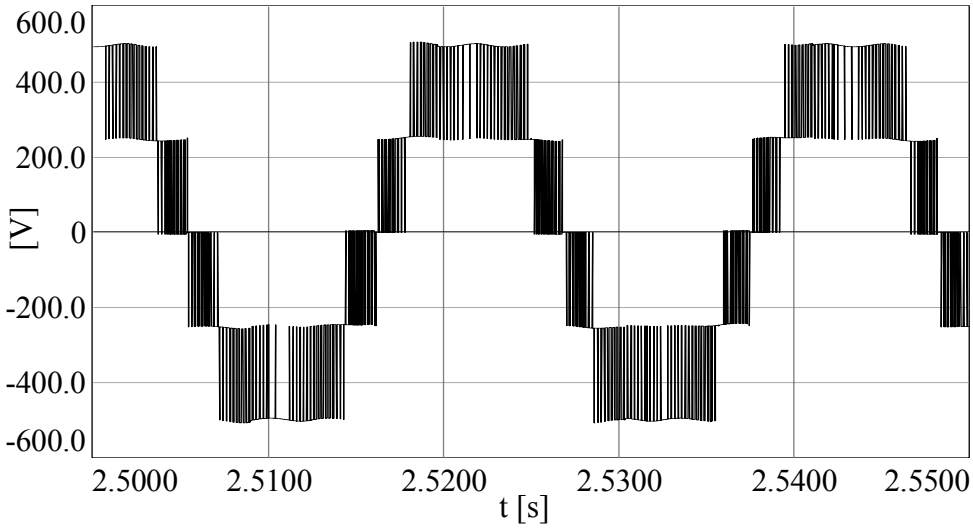


Figure 4.86 The line-to-line output voltage waveform of the three-level NPC inverter at steady-state and high M_i (M_i=1.0) for NTV-PWM with the optimal α control method.

4.5.4 Two-Parameter PWM with The Optimal α-γ Control Method

This section presents the induction motor drive simulation results of two-parameter PWM with the optimal α-γ control method for high modulation (M_i=1.0 corresponding to ω_r^*=1400 min^{-1}) index operating conditions. For the 400 min^{-1} operating range, the behavior is the same as in the optimal α control method. Because, at low speed which corresponds to low modulation index, only the inner hexagon is utilized and in the inner hexagon the optimal α and optimal α-γ methods perform identically. Therefore, focus is placed on the 1400 min^{-1} operating condition which corresponds to high modulation index where the medium voltage vector related neutral point potential problems dominate.

In Figure 4.87, the neutral point current waveform is illustrated. The neutral point current consists of phase current segments. Figure 4.88 shows the neutral point potential corresponding to the neutral point current pulses. As seen from Figure 4.88, the neutral point potential has no drift. Figure 4.89 shows the zoom-in view of the neutral point current waveform at steady-state for a sixty-degreee segment of the output cycle. The neutral point current consists of small width pulses at the PWM

frequency. The corresponding neutral point potential is shown in Figure 4.90. The neutral point potential is proportional to the integral of the neutral point current as shown in Figure 4.90. There is no dominant triplen harmonic content on the neutral point potential, as shown in Figure 4.90. Corresponding to the waveform in Figure 4.90, as shown in Figure 4.91, the redundancy function α frequently reaches the limit values of 1 or 0 in order to eliminate the neutral point potential error. The maximum charge available from the small voltage vectors is employed. At the limit values of the redundancy function α (0 or 1), when the charge of the small voltage vectors is not enough to compensate the neutral point potential, the γ parameter is utilized and the its value becomes less than one as shown in Figure 4.92. By employing the γ parameter as the additional control variable, the neutral point potential error is eliminated.

For the same operating condition as above, in Figure 4.93, the redundancy function α of the optimal α - γ control method is shown for one output voltage fundamental cycle (46.7 Hz). As seen from the figure, the redundancy function α is periodical and its frequency is three times of the output voltage fundamental frequency. In Figure 4.94, the γ parameter of the optimal α - γ control method is shown for one output voltage fundamental cycle. As seen from the figure, γ is periodical and its frequency is six times the output voltage fundamental frequency. As seen from Figure 4.95, the phase current is nearly sinusoidal. However, its ripple magnitude is larger than the previous control method cases. As seen from Figure 4.96, the line-to-line output voltage is not the same as the NTV-PWM case. The distorted line-to-line output voltage increases the load current ripple magnitude.

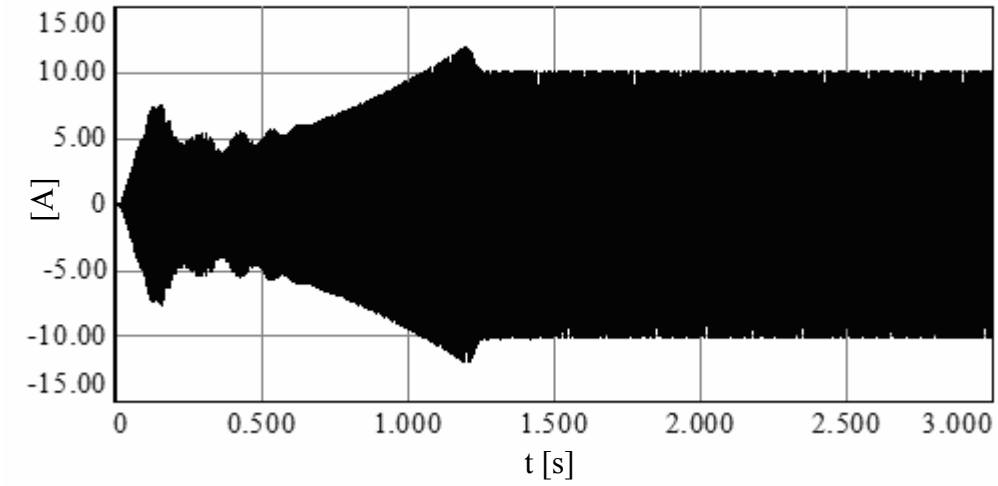


Figure 4.87 The neutral point current waveform at high M_i (M_i=1.0) for two-parameter PWM with the optimal α-γ control method.

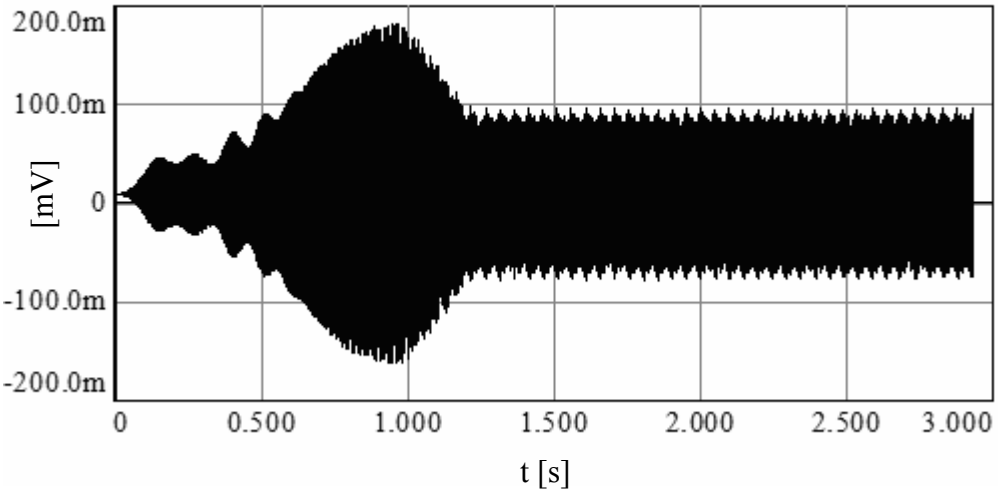


Figure 4.88 The neutral point potential waveforms at high M_i (M_i=1.0) for two-parameter PWM with the optimal α-γ control method.

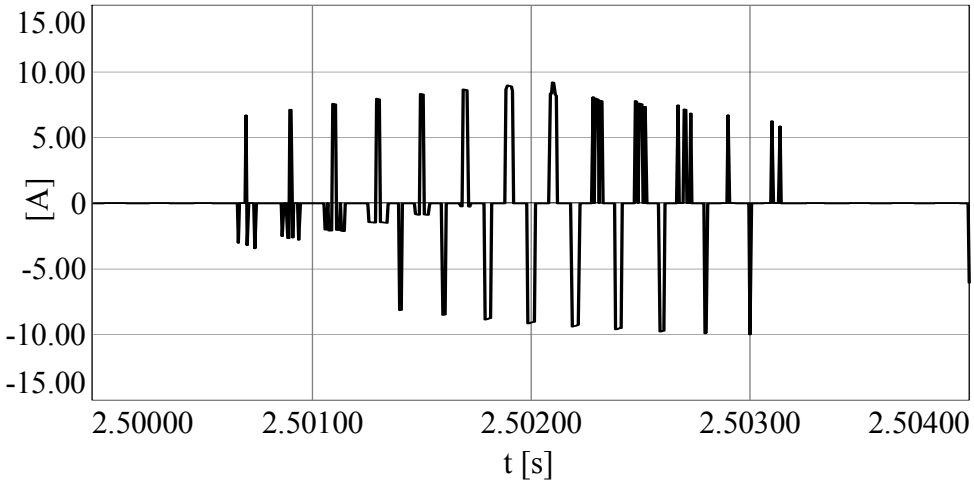


Figure 4.89 The zoom-in view of the neutral point current waveform at steady-state and high M_i (M_i=1.0) for two-parameter PWM with the optimal α-γ control method.

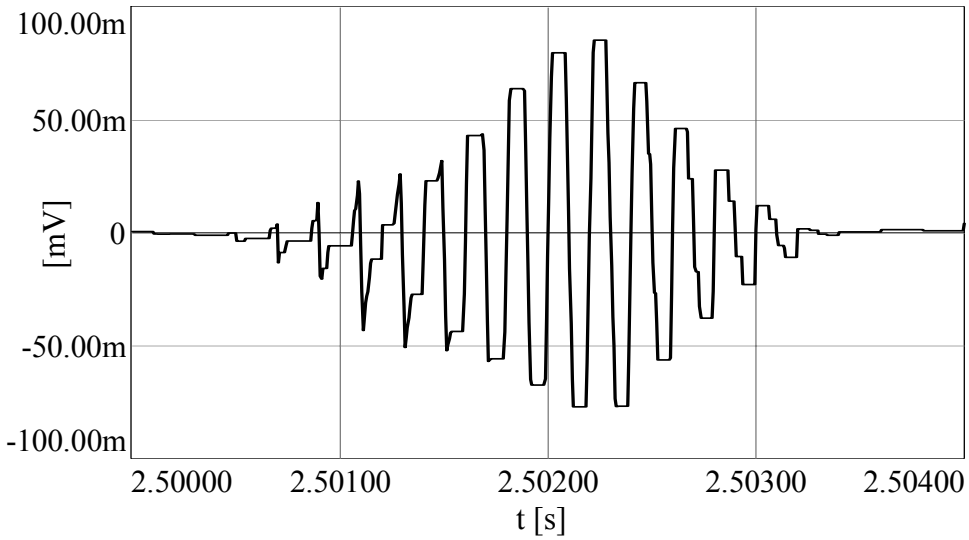
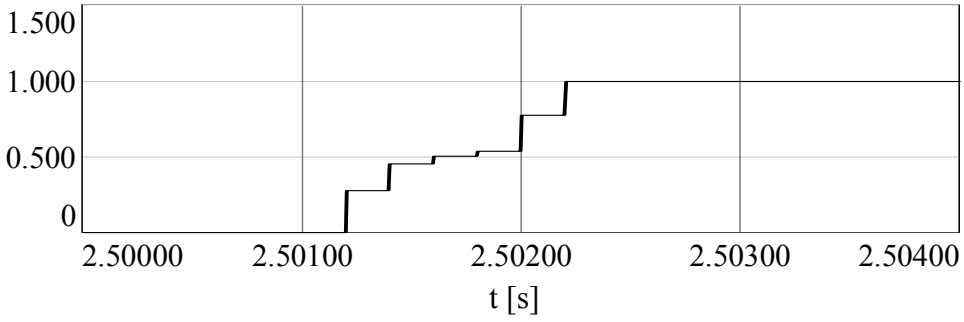
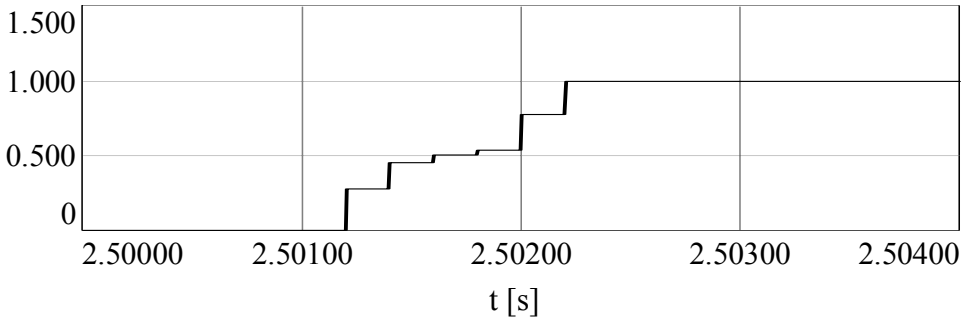


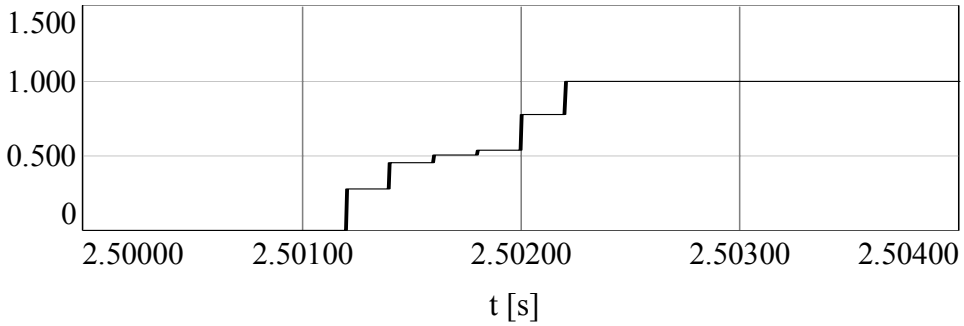
Figure 4.90 The zoom-in view of the neutral point potential waveform at steady-state and high M_i (M_i=1.0) for two-parameter PWM with the optimal α-γ control method.



(a) α



(b) α_1



(c) α_2

Figure 4.91 The redundancy function α of the optimal α-γ control method at steady-state (M_i=1.0).

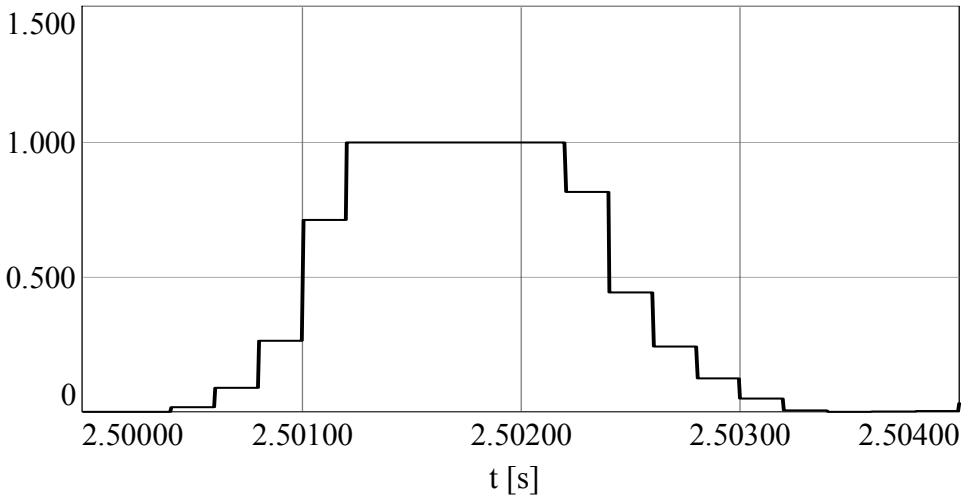


Figure 4.92 The γ parameter of the optimal α-γ control method (M_i=1.0).

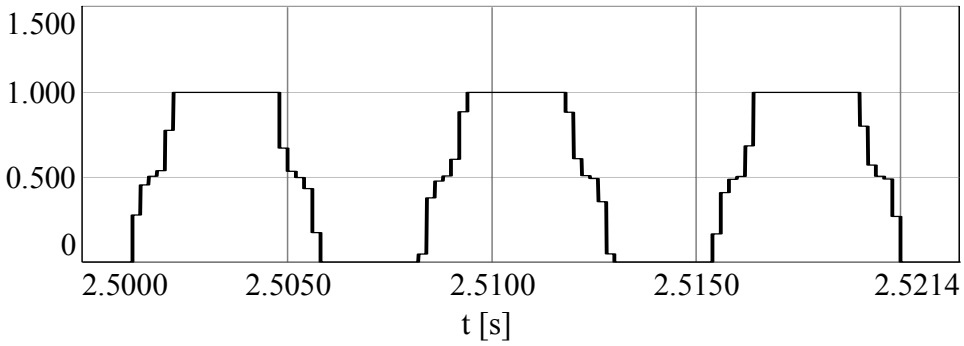


Figure 4.93 Variation of α in the optimal α-γ control method (M_i=1.0) within one output voltage fundamental period at steady-state.

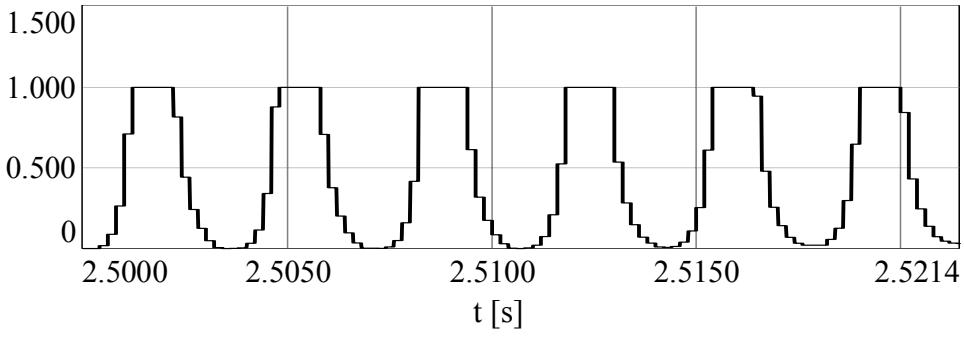


Figure 4.94 Variation of γ in the optimal α-γ control method (M_i=1.0) within one output voltage fundamental period at steady-state.

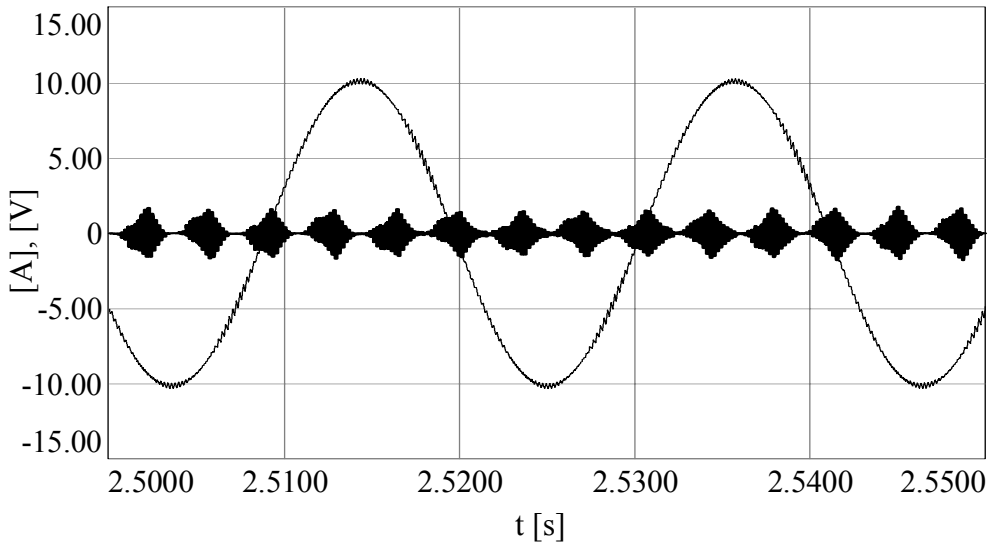


Figure 4.95 The neutral point potential (bold, scale: 20x) and the phase current at steady-state and high M_i (M_i=1.0) for two-parameter PWM with the optimal α-γ control method.

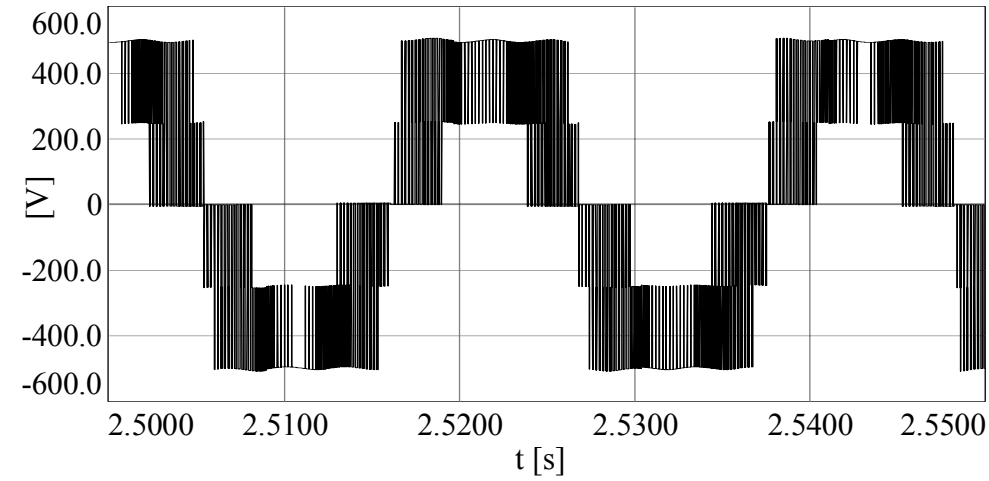


Figure 4.96 Line-to-line output voltage waveform of the three-level NPC inverter at steady-state and high M_i (M_i=1.0) for two-parameter PWM with the optimal α-γ control method.

4.5.5 Performance Comparisons of The Control Methods For The Constant V/f Controlled Induction Motor Drive

Table 4.8 and Table 4.9 summarize the neutral point potential performance of the uncontrolled neutral point potential case along with the three control methods simulated in section 4.5.2 to 4.5.4 of this section. The steady-state peak-to-peak neutral point potential value ΔV_{pp} and the dynamic peak neutral point potential value are shown in the tables.

The tables illustrate the neutral point potential performance superiority of the optimal α-γ control method to the other methods. Specifically at high modulation index values, the neutral point potential is the smallest with the optimal α-γ control method and it is several times smaller than the optimal or uniform α control method. While the optimal α-γ control method gives practically zero value, the other methods have approximately 2.6 V ripple. Therefore, both the steady-state and dynamic performance of the optimal α-γ control method are superior to the other two methods.

Another important point regarding the optimal α-γ control method is that the γ parameter range defines the effectiveness of the optimal α-γ controller. If the γ parameter is freely varied, the neutral point potential error can be totally eliminated at high modulation index. However, confining the range between $0.5 \leq \gamma \leq 1$, the neutral point potential error can not be completely eliminated and a triplen harmonic appears at the neutral point potential. Therefore, the range of the γ parameter is the major determining factor as far as elimination of the neutral point potential error is concerned. However, the trade-off involves a more distorted output voltage waveform. In Table 4.9, the influence of constrained γ is summarized. If γ is constrained between 1 and 0.5 the neutral point potential performance rapidly degrades. When selecting γ=0, the inverter frequently operates as two-level inverter and the neutral point potential problem disappears (at the expense of increased output voltage waveform distortion and switching losses).

Table 4.8 Neutral point potential performance comparison of various control methods at low M_i (M_i=0.27, 400 min^{-1})

(f_{PWM}: PWM frequency)

Control Method	Dynamic Peak Voltage (mV)	Neutral Point Potential Drift	Steady-state Peak Voltage (mV)	Neutral Point Potential Ripple Frequency
NTV-PWM (α =0.5)	100	40 mV	40	f_{PWM}
Uniform α	44	None	18	f_{PWM}
Optimal α	44	None	18	f_{PWM}
Optimal α-γ	44	None	18	f_{PWM}

Table 4.9 Neutral point potential performance comparison of various control methods at high M_i (M_i=1, 1311 min^{-1})

(f_{PWM}: PWM frequency and f_o: output voltage fundamental frequency)

Control Method	Dynamic Peak Voltage (V)	Neutral Point Potential Drift	Steady-state Peak Voltage (V)	Neutral Point Potential Ripple Frequency
NTV-PWM (α =0.5)	2.60	0.2 V	2.400	$3f_o$
Uniform α	3.00	None	2.600	$3f_o$
Optimal α	3.10	None	2.700	$3f_o$
Optimal α-γ	0.18	None	0.085	f_{PWM}
Optimal α-γ (1>γ>0.5)	1.80	None	1.550	$3f_o$
Optimal α-γ (γ=0)	0.55	None	0.500	f_{PWM}

In the following chapter, the theoretical results of the previous chapter and the computer simulation based results of the present chapter will be verified via detailed laboratory experiments.

CHAPTER 5

EXPERIMENTAL RESULTS AND PERFORMANCE EVALUATION OF THE THREE-LEVEL NPC INVERTER NEUTRAL POINT POTENTIAL CONTROL METHODS

5.1 Introduction

The previous chapter presented the computer simulations that investigate the neutral point potential performance of a three-level NPC inverter with various control methods. In this chapter, experimental results of the neutral point potential control methods will be shown. In the experimental study, the steady-state and dynamic performance of the neutral point potential control methods will be investigated. A three-phase R-L type load and a three-phase induction motor feeding a fan load will be tested both.

5.2 Drive System Hardware Description

For the purpose of experimental evaluation, a 5 kVA prototype three-level NPC inverter was designed and built at METU Electrical and Electronics Engineering Department, in the Electrical Machines and Power Electronics Laboratory. The block diagram of the experimental set-up is shown in Figure 5.1. The electrical power circuitry of the system is shown in Figure 5.2. In the experimental set-up, to convert the three-phase 380 V, 50 Hz AC utility grid voltage to DC voltage, a 1600-V, 100-A three-phase full-bridge diode rectifier module is employed. A three-phase 20-A automatic fuse is employed at the utility grid connection point for the protection purpose. To get a low-distortion input current waveform, a three-phase AC line reactor (L_o=2.3 mH per-phase with 20 A rms current rating) is inserted between the AC line and the three-phase full-bridge diode rectifier. Also a DC link

reactor (L_{dc}=1.46 mH with 20 A rms current rating) is inserted between the rectifier output and the DC bus of the inverter in order to further improve the input current waveform and reduce the rms current stress on the DC bus capacitors. The DC bus of the system consists of two capacitors connected in series. Manufactured by Mallory Inc., each capacitor has 1000 μF capacitance, 450-V_{dc} voltage rating, and 5.5-A rms current rating. To balance the voltages of the DC bus capacitors and discharge the inverter during shut-down, bleeding resistors are connected in parallel with the DC bus capacitors and each bleeding resistor has 30 kΩ resistance value (R_b=30 kΩ) and 10-W power rating. A pre-charge resistor ($R_{pre\text{-}charge}$) is utilized to limit the inrush current during the start-up of the system and the pre-charge resistor is short-circuited (by-passed) by means of a manual by-pass switch after the DC bus capacitor is charged to its steady-state value. The pre-charge resistance value is equal to 47 Ω and it has a 50 W power rating. For the purpose of protection, 20-A fast fuses are employed on the DC bus. One fast fuse provides connection between the positive terminal of the rectifier and the positive terminal of the capacitor bank. The remaining fast fuses are utilized between the DC bus and the three-level NPC inverter. For the purpose of measuring the neutral point potential, two measuring resistors (R_m) are employed with the ratings of 30 kΩ and 10 W. The neutral point potential is measured as the difference between the midpoint of the series connected DC bus capacitors and the midpoint of the measuring resistors. The neutral point potential is marked as "V_n" in Figure 5.2.

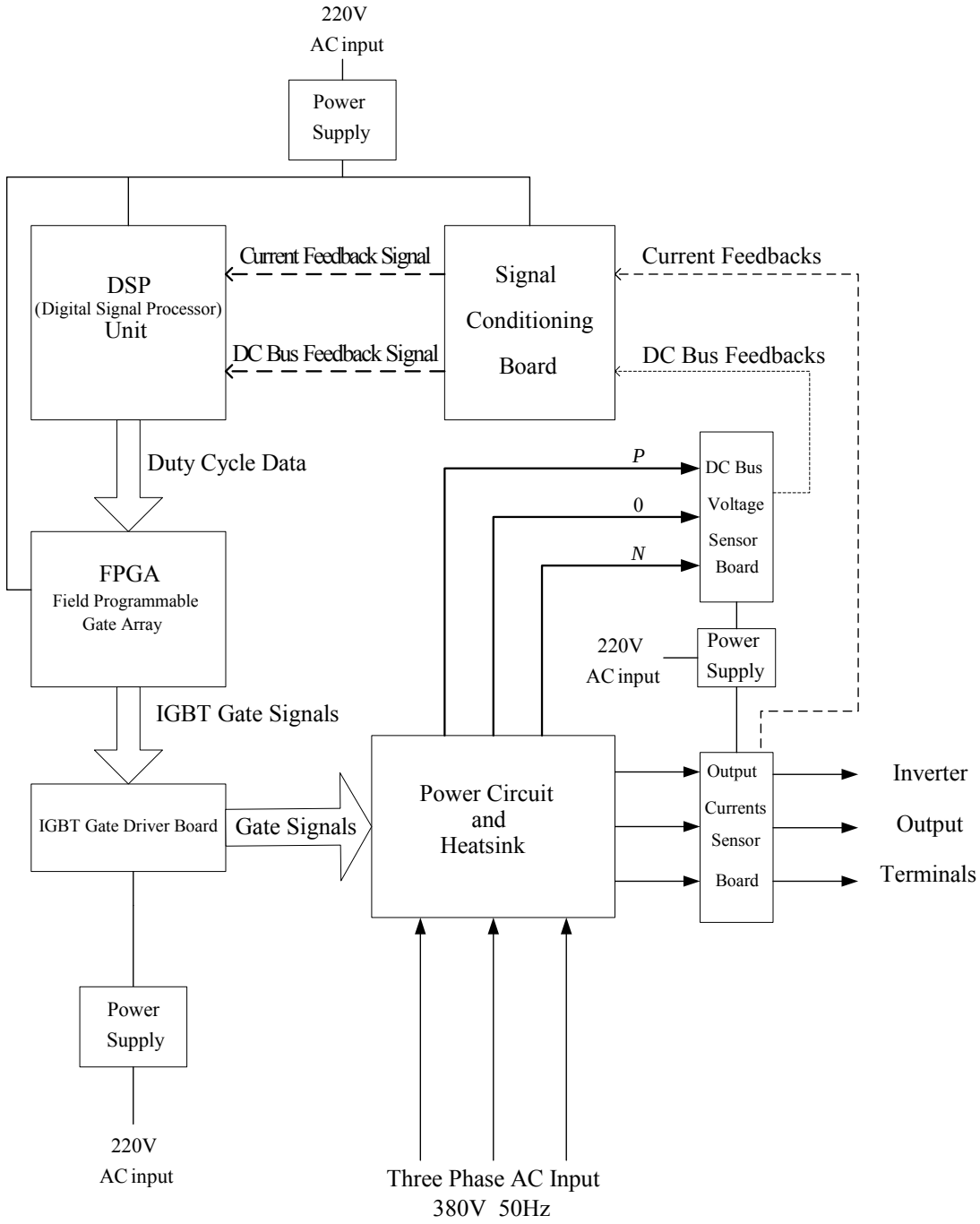


Figure 5.1 System block diagram of the experimental set-up.

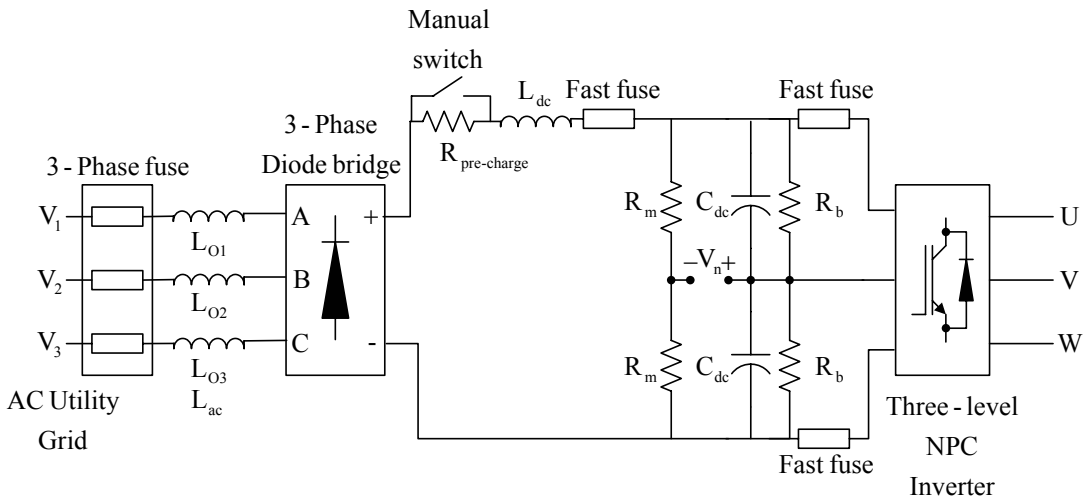


Figure 5.2 Experimental set-up electrical power circuit diagram.

The three-level NPC inverter is built by using six dual-pack IGBT modules and three dual-pack fast diode modules. Each phase of the three-level NPC inverter consist of two IGBT modules and one diode module, as shown in Figure 5.3. Semikron brand IGBT modules, SKM 50 GB 123 D and diode modules SKKD 40F10 are utilized. The IGBT modules are driven by the Semikron SKHI 22A gate driver modules. The basic specifications of the power semiconductors and gate drive circuit utilized in the designed inverter are summarized in Table 5.1. The gate driver modules have built-in analog dead time generation facility. The dead-time can be set as 3.3 μs or 4.3 μs by changing the externally connected passive components. However, during the experiments it has been seen that the dead-time generation facility of the gate driver modules is not precise. The dead-time in some of these gate drive modules was measured as large as 6-7 μs. The differences between the dead-time values of different modules create distortion on the output voltage waveform and cause neutral point potential drift in the three-level NPC inverter as will be discussed later in this chapter in detail.

Table 5.1 Specifications of the power semiconductor modules and gate driver modules utilized in the experimental three-level NPC inverter drive

SKM 50 GB 123 D (IGBT of the dual pack)		
V_{CES}	Collector-emitter blocking voltage rating	1200 V
I_C	Continuous collector current rating (rms)	50 A
V_{CEsat}	Collector-emitter saturation voltage at 50 A	2.7 V
$t_{d(on)}$	Turn-on delay time	70 ns
t_r	Rise time	60 ns
$t_{d(off)}$	Turn-off delay time	400 ns
t_f	Fall time	45 ns
SKM 50 GB 123 D (Diode of the dual pack)		
V_F	Forward voltage drop at I_F=50 A	2 V
I_{RRM}	Peak reverse recovery current	23 A
Q_{rr}	Recovered charge at I_F=40 A	2.3 µC
SKKD 40F10 (Diode module)		
V_{RRM}	Repetitive peak reverse voltage	1000 V
I_{FRMS}	RMS forward current	100 A
V_F	Forward voltage I_F=150 A	2 V
I_{RRM}	Peak reverse recovery current	10 A
Q_{rr}	Recovered charge at I_F=100 A	3 µC
t_{rr}	Reverse recovery time	600 ns
SKHI 22A Gate Driver Module		
V_S	Supply voltage primary side	15 V
I_{SO}	Supply current primary side at no-load/max.	80 / 290 mA
$V_{İ}$	Input signal voltage ON/OFF	15 / 0 V
$V_{İT+}$	Input threshold voltage (High)	11.7 V
$V_{İT-}$	Input threshold voltage (Low)	5.5 V
R_{in}	Input resistance	10 kΩ
$V_{G(ON)}$	Turn-on gate voltage output	+15 V
$V_{G(OFF)}$	Turn-off gate voltage output	-7 V
t_{TD}	Top-Bottom interlock dead-time min. / max.	3.3 / 4.3 µs

The three-level NPC inverter DC bus is designed with the planar bus technique. In this case, three aluminum planes are utilized one for each rail of the DC bus. The DC bus layers are sandwiched with paper type insulation material with 10 kV insulation level. Thus, in the design a low inductance DC bus structure could be obtained. To reduce the switching stress on the IGBT and diode modules, snubber capacitors are connected between the positive and negative DC bus terminals of each inverter phase, as shown in Figure 5.3. The snubbers are placed right on the top of the planar DC bus and semiconductor device terminals. Each snubber capacitor has a 680 nF capacitance value and 630 V voltage rating.

To sense the output phase currents LTS 25 NP hall-effect current sensors manufactured by LEM Company are employed and the output signals of the current sensors are conditioned by using basic operational amplifier circuits and passive noise filters. The DC bus capacitor voltages were measured by using isolated voltage sensors LV25-P manufactured by LEM Company and a basic operational amplifier circuit is employed along with passive noise filters to condition the output signal of the voltage sensors.

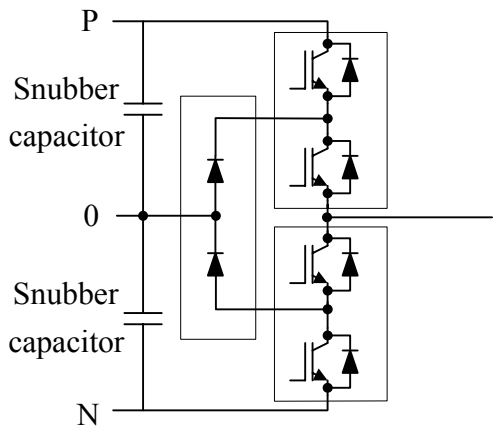


Figure 5.3 One phase leg of the three-level NPC inverter with C-type snubbers.

The pulse pattern programming and control functions of the three-level NPC inverter are accomplished by a system consisting of a Digital Signal Processor (DSP) and a Field Programmable Gate Array (FPGA). Computational functions such as analog to

digital (A/D) conversion and duty cycle calculation are accomplished by the DSP. The pulse pattern programming function is accomplished by the FPGA.

In the experimental set-up, for a DSP, the eZdsp F2812 board manufactured by Spectrum Digital is employed to accomplish the control functions. The features of the eZdsp F2812 board are given in Table 5.2 [23]. The board contains the TMS320F2812 DSP manufactured by Texas Instruments and the features of TMS320F2812 are given in Table 5.3.

The main control program is implemented in the DSP. One of DSP's two event managers named "EVA Timer1" is employed to generate an interrupt for the required calculations periodically. This interrupt is called as the "main interrupt." The main interrupt takes place once every 200 μs which corresponds to 5 kHz. When a main interrupt occurs, the DSP goes to the "main interrupt service routine" function to calculate duty cycle information of the semiconductor switches. The flow chart of the main interrupt service routine is shown in Figure 5.4. As seen from the figure, the main interrupt service routine starts with the A/D conversion of the three output phase currents and two DC bus capacitor voltages. According to the values and the polarities of the phase currents, the values of the DC capacitor voltages, and value of the reference voltage vector; the duty cycles of the semiconductor switches are calculated from Table 3.5. The calculated duty cycle values are transferred to the FPGA in order to generate the gate drive signals. The connection between the DSP and the FPGA is illustrated in Figure 5.5.

Table 5.2 Main features of the eZdsp F2812 board

Digital Signal Processor	TMS320F2812
External Clock Frequency	30 MHz
External Memory	64K words SRAM
Expansion Connectors	• Analog • Digital I/O • External Interface
Interface	• IEEE 1149.1 JTAG* Controller • IEEE 1149.1 JTAG Emulation Connector

*: Joint Test Action Group

Table 5.3 Main features of TMS320F2812 DSP

Operating Frequency	150 MHz
Clock and System Clock	• On-Chip Oscillator • Watchdog Timer
Central Processing Unit (CPU)	32-bit high performance CPU
On-Chip Memory	• 128K×16 Flash Memory • 18K×16 RAM** • 1K×16 OTP ROM***
Timers	Three 32-Bit CPU Timers
Motor Control Peripherals	Two Event Manager (EVA, EVB)
Analog-Digital Converter (ADC)	• 12-Bit ADC • 16 Channels • Fast Conversion Rate: 80ns/12.5 MSPS
General Purpose Input/Output	Up to 56 Pins
External Interface	• Up to 1M Total Memory • Three Individual Chip Selects
Serial Port Peripherals	• Serial Peripheral Interface • Two Serial Communications Interfaces • Enhanced Controller Area Network • Multi-channel Buffered Serial Port

**: Random Access Memory

***: One-Time Programmable Read Only Memory

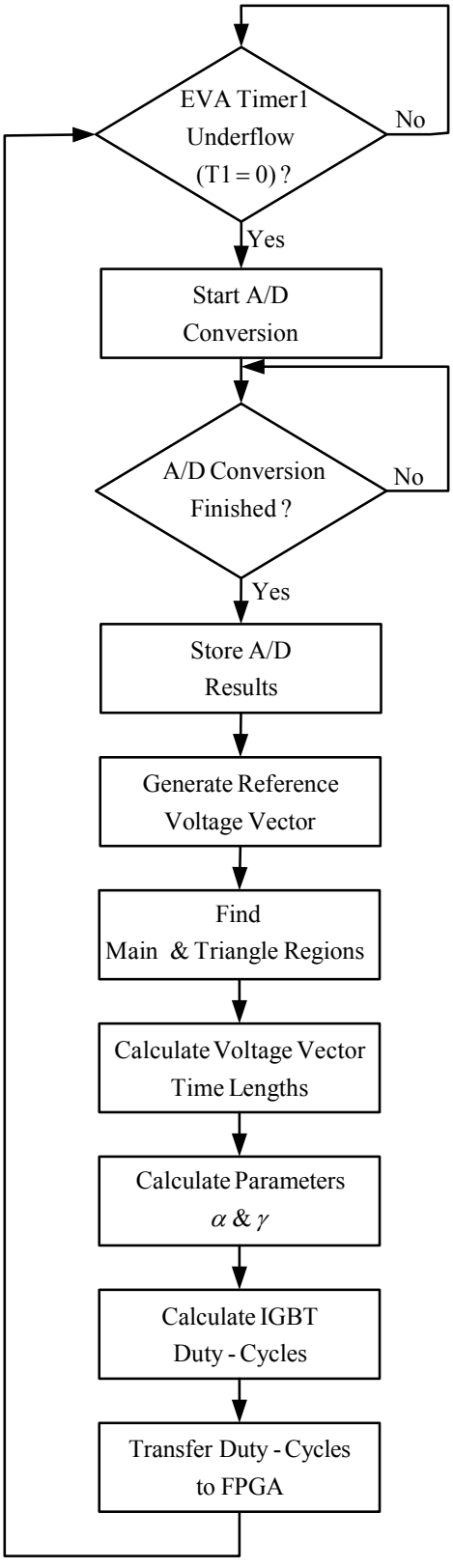


Figure 5.4 The flow chart of the main interrupt service routine.

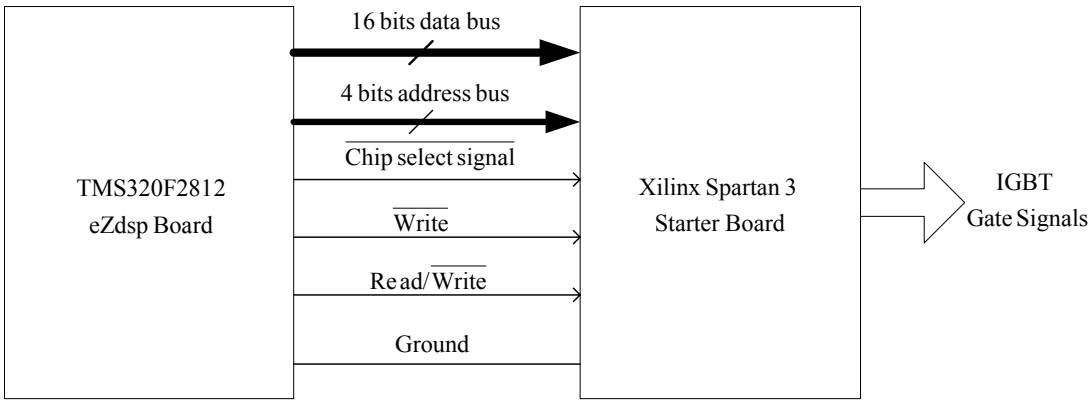


Figure 5.5 Illustration of the connection between the DSP and the FPGA.

In the experimental set-up the Xilinx Spartan3 FPGA Starter Board is utilized for the purpose of pulse pattern generation. The features of the FPGA board are given in Table 5.3 [24] and the features of Xilinx Spartan-3 XC3S200 FPGA are given in Table 5.4 [25]. In the FPGA, utilizing digital hardware components, the pulse pattern is generated.

In the pulse pattern generator, first, a continuous up-down counter is built as shown in Figure 5.6. The continuous up-down counter clock frequency is set as 100 MHz to obtain high resolution. The continuous up-down counter is controlled by a counter state machine that is shown in Figure 5.7. At the second stage, twelve buffer registers are created to store the DSP-calculated duty cycle values of the associated phase semiconductor switches in the FPGA. The twelve duty cycle data are input from the DSP to the FPGA and the word length of each data is 16-bit. Each inverter phase leg has four registers in the FPGA, as shown in Figure 5.8.

The twelve duty-cycle values are calculated by the DSP. This twelve-duty-cycle-information is only for six semiconductor switches. When the switch pulse pattern is created for these six switches, the pulse pattern of the remaining six is created by simply taking their complementaries. For transferring data from the DSP to the FPGA, the external interface module of the DSP [26] is employed. A 4-bit address bus, 16-bit data bus, one chip select signal, write signal, and read/write signal are employed to transfer data from the DSP to the FPGA as shown in Figure 5.5. First, the chip select signal is activated and the address is placed on the address bus.

Second, the write signal and read/write signal is activated and data is placed on the data bus. Except for the data bus, the signals are used for the purpose of decoding the each semiconductor switch data register. The data transfer procedure is repeated once every 200 μs. Therefore, the duty cycle information is refreshed once every 200 μs by DSP. And the duty cycle values are compared with the up-down counter and IGBT gate signals are generated.

Table 5.3 Features of Xilinx Spartan-3 FPGA Starter Board

FPGA Chip	Xilinx Spartan-3 XC3S200 FPGA
Platform Flash	2 Mbit Xilinx XCF02S
Memory	1 MB SRAM
External Clock	50 MHz
Others	• 3-bit, 8-color VGA display port • 9-pin RS232 Serial Port • PS/2-style mouse/keyboard port • Four-character, seven-segment LED display • Eight slide switches • Eight individual LED outputs • Four push button switches

Table 5.4 Features of the Xilinx Spartan-3 XC3S200 FPGA

• 4320 logic cell equivalent
• Twelve 12K-bit block RAMs
• Twelve 18×18 hardware multipliers
• Four Digital Clock Managers (DCMs)
• Up to 173 user-defined Input/Output signals

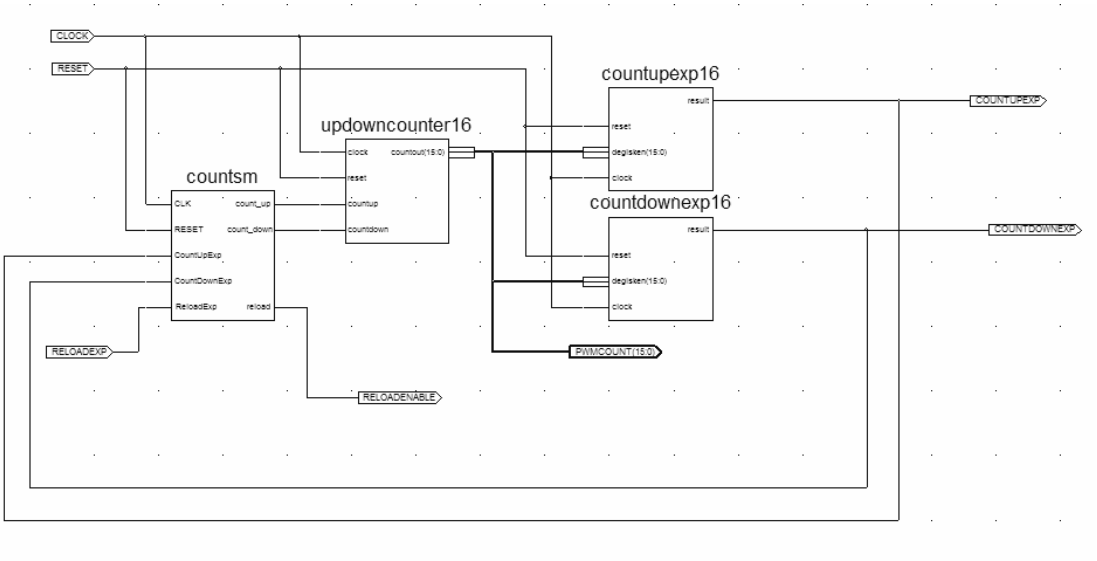


Figure 5.6 Block diagram of the up-down counter in the FPGA.

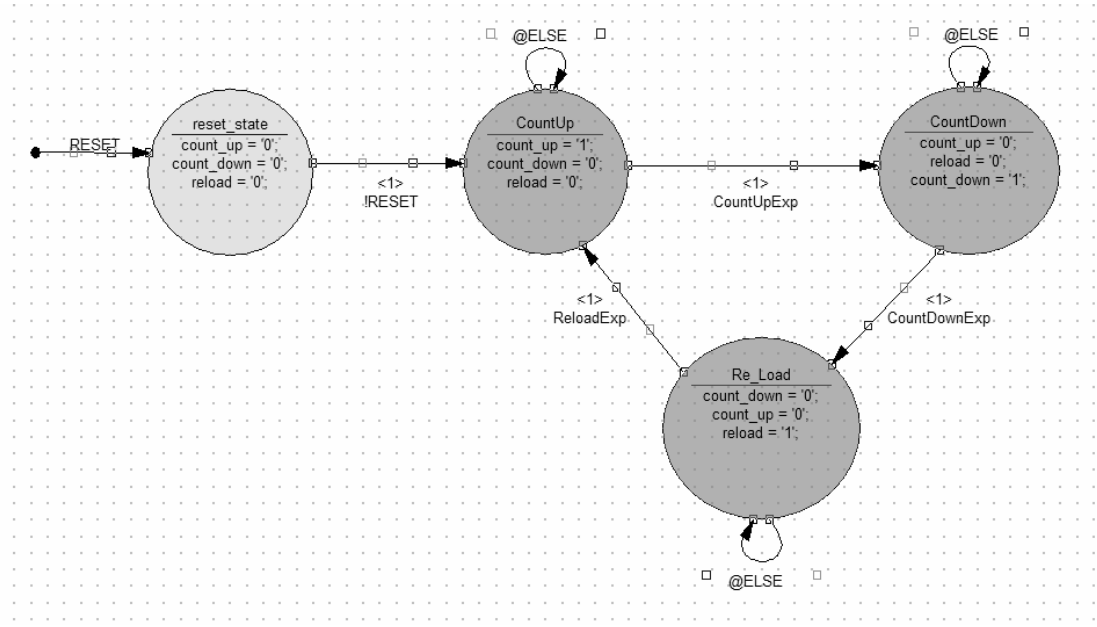


Figure 5.7 The continuous up-down counter state machine.

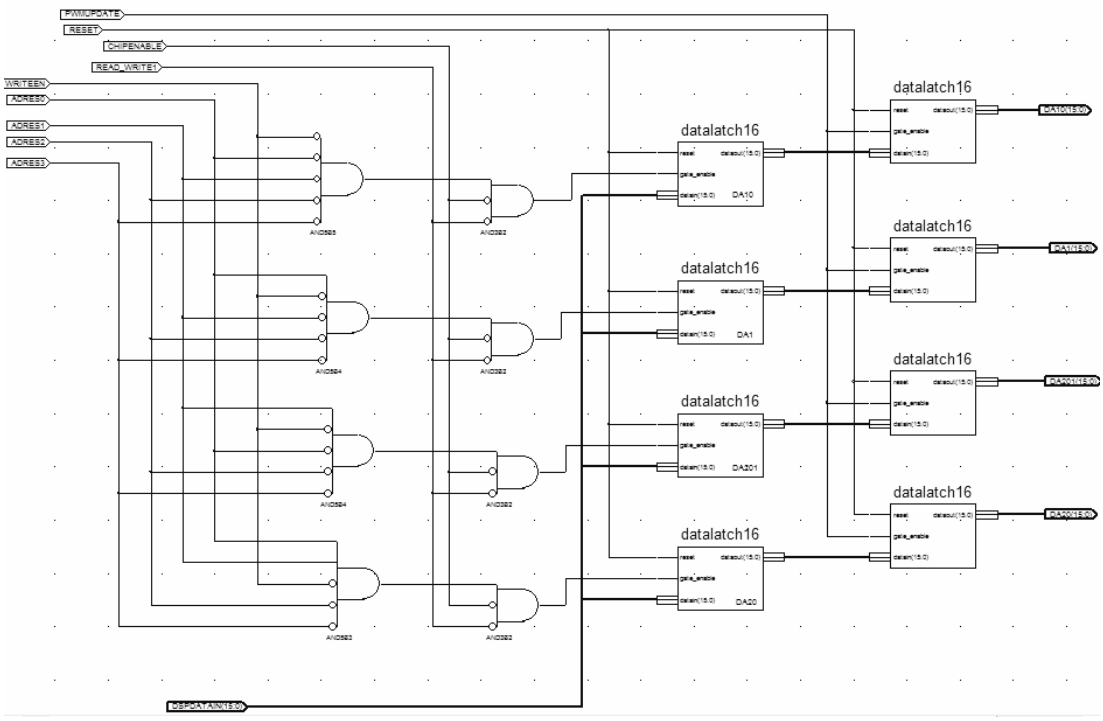


Figure 5.8 Registers of one inverter phase leg in the FPGA.

In Figure 5.9 the photograph of the laboratory prototype three-level NPC inverter is shown. In Figure 5.10 the digital control platform of the inverter drive that includes the DSP evaluation board and the FPGA starter kit is shown. In figure 5.11 the whole set-up is photographed.

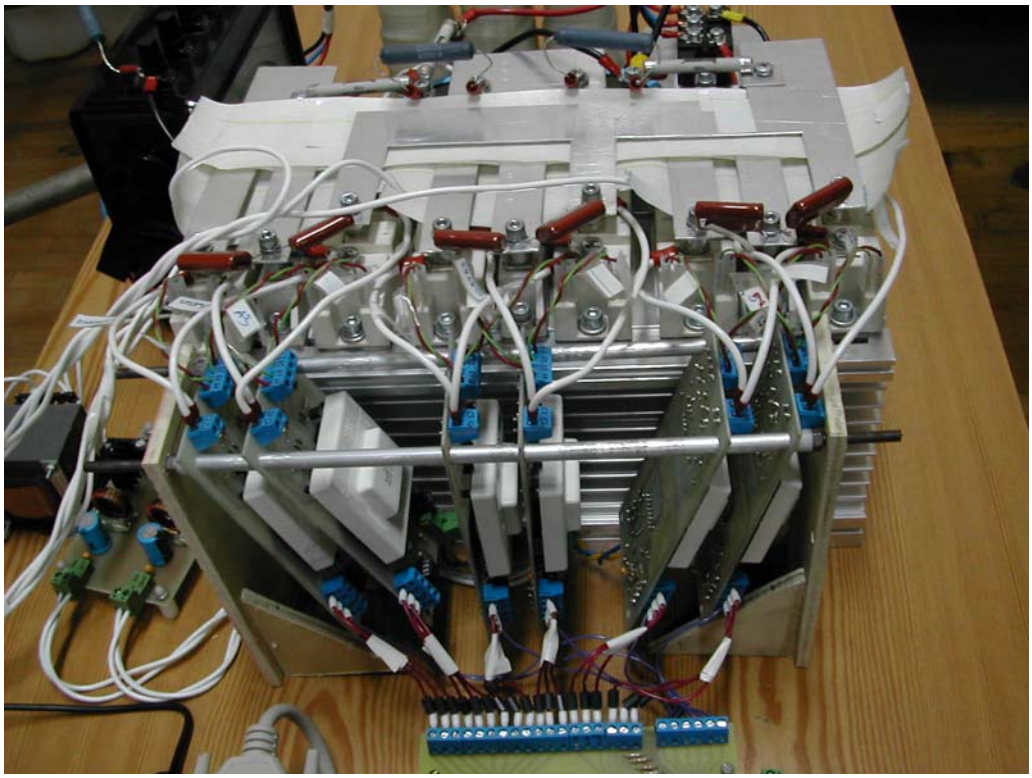


Figure 5.9 Laboratory prototype three-level NPC inverter.

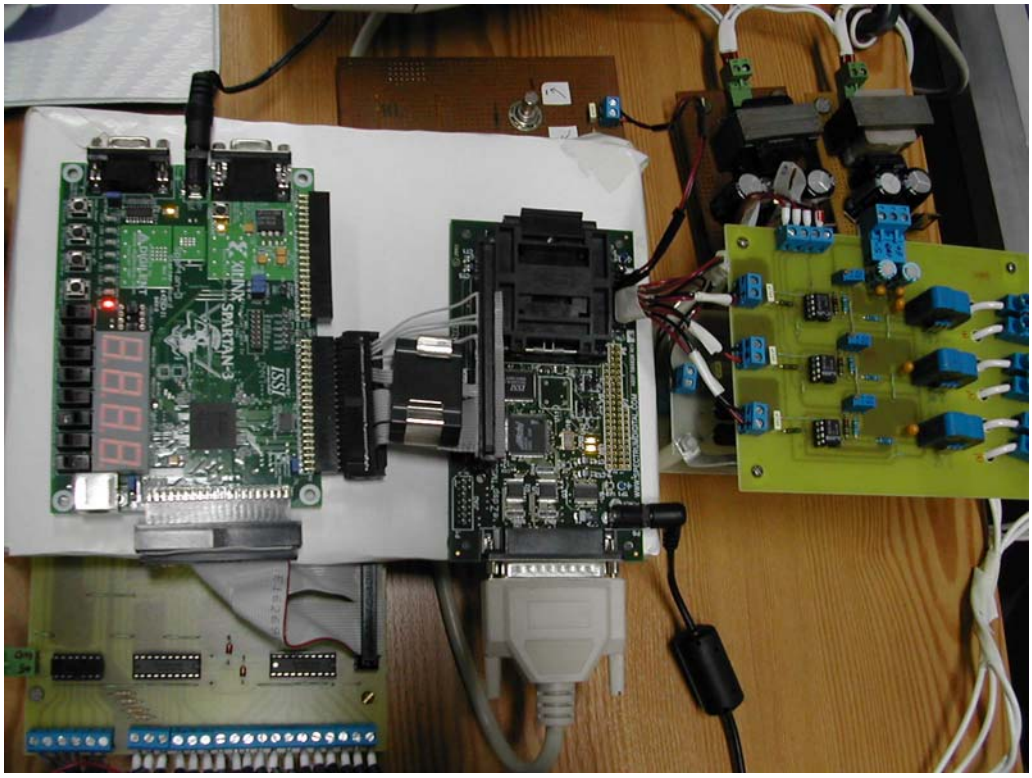


Figure 5.10 Digital control platform of the laboratory prototype three-level NPC inverter.

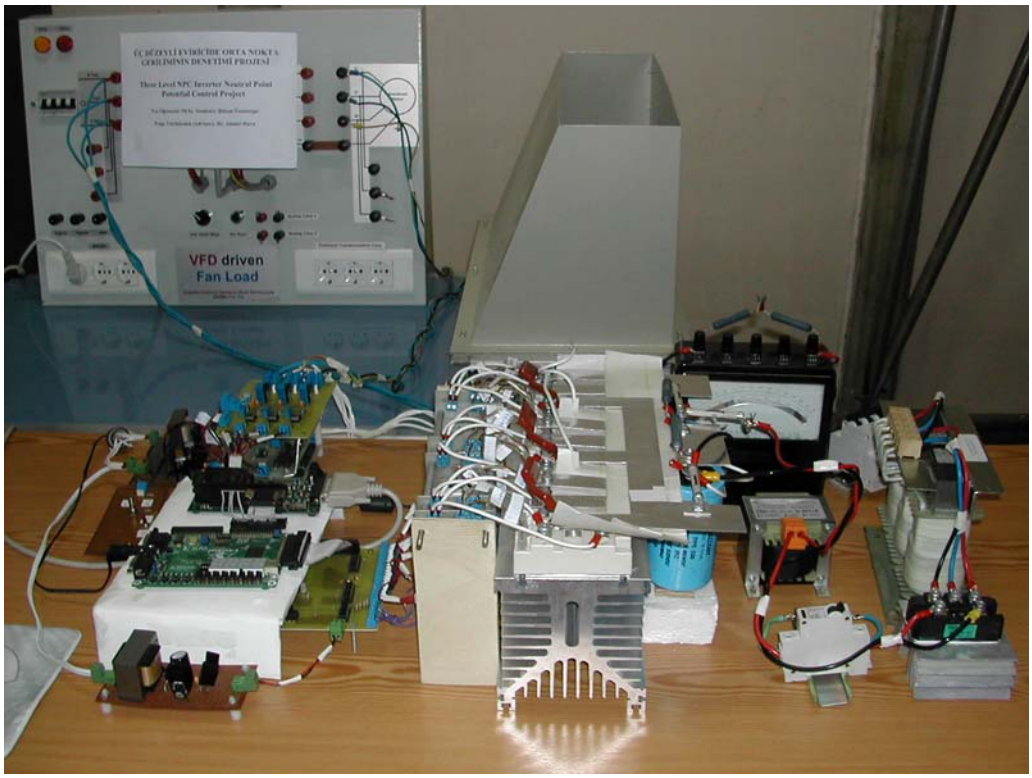


Figure 5.11 Laboratory prototype three-level NPC inverter drive system set-up.

5.3 Experimental Results

In this section the experimental results of the three-level NPC inverter drive will be presented first for a three-phase passive R-L type load and second for an induction motor feeding a fan load. In both cases, the experimental results will be compared with the computer simulations of the associated section of chapter 4 and comments will be made. In both experiments the same inverter hardware configuration will be utilized.

5.3.1 R-L Load Experimental Results

In this section, in order to verify the three-phase R-L load simulation results, a three-phase Y-connected R-L load is connected to the three-level NPC inverter and tested at various operating conditions. The load parameters are given in Table 5.5. As seen

from the table, the load parameters are the same as those in section 4.4 of chapter 4 (Table 4.4). The three-phase load is driven at fixed frequency and magnitude inverter output voltage. This implies that the three-phase reference voltage vectors have a fixed magnitude (fixed modulation index) and a fixed frequency value. First, NTV-PWM without neutral point potential control case experimental results are presented for f_o=15 Hz corresponding to low M_i (M_i=0.3) and f_o=45Hz corresponding to high M_i (M_i=0.92). Second, NTV-PWM with the uniform α control method results are shown for the same operating conditions. Third, NTV-PWM with the optimal α control method results and last, two-parameter PWM with optimal α–γ control method results are presented.

Table 5.5 Experimental three-phase Y-connected R-L load parameters

Load Phase	R (Ω)	L (mH)
U	8.2	55.45
V	8.2	55.45
W	8.0	55.45

5.3.1.1 NTV-PWM without Neutral Point Potential Control Method

This section presents the experimental results of NTV-PWM without neutral point potential control. In this case, the redundancy function of the small voltage vectors is set as 0.5 (α=0.5).

First for f_o=15 Hz and M_i=0.3 the results are presented. Loading transients and steady-state operating conditions are tested both. Initially the inverter is in the off-state and when the inverter is enabled the inverter excites start-up transients on the R-L load. In the experiment both the start-up and steady-state waveforms are recorded. In Figure 5.12, the DC bus voltage, the load current, and the neutral point potential waveforms are shown. As seen from the figure, the three-level NPC inverter is loaded suddenly. After loading the DC bus voltage slightly decreases and the neutral point potential starts to drift as shown in Figure 5.12. The neutral point

potential drift takes about 15 seconds and its final value is about 40 V when all the signals settle to their steady-state values. At steady-state, the load current and the neutral point potential waveforms are as shown in Figure 5.13. The load current is nearly sinusoidal and the neutral point potential has no triplen harmonic content. The line-to-neutral output voltage of the three-level NPC inverter is illustrated in Figure 5.14. As seen from the figure, the line-to-neutral output voltage waveform has approximately 40 V DC offset due to the neutral point potential drift. The line-to-line output voltage waveform of the three-level NPC inverter is shown in Figure 5.15. The line-to-line output voltage waveform is generated from two DC bus voltage levels that are no more equal. This appears on the waveform in the figure as an additional intermediate voltage level. The neutral point potential drift causes distortion on the line-to-line output voltage waveform. In Figure 5.16, the DC bus voltage ripple is shown. As seen from Figure 5.16, the frequency of the ripple is six times of the AC supply fundamental frequency. This is due to the diode rectifier and has no effect on the neutral point potential.

The neutral point potential drift is significantly larger than that of the computer simulation under the same conditions (Figure 4.25). There are several reasons for the difference in the amount and duration of the drift. The computer simulation could not be run for sufficiently long time due to the computational speed and memory allocation constraints of the computer available at the university. Second, the simulation model assumed an ideal inverter with identical switches while in the practical implementation this condition is not satisfied. In the experimental set-up, the switches are different from each other within the manufacturing tolerance limits. Moreover, the IGBT gate driver circuits have significant amount of dead-time with strong imbalance between the dead-time values of different phase legs. Thus, the pulse pattern deviates from the ideal and creates conditions favoring the neutral point potential drift when constant α with the 0.5 value is utilized.

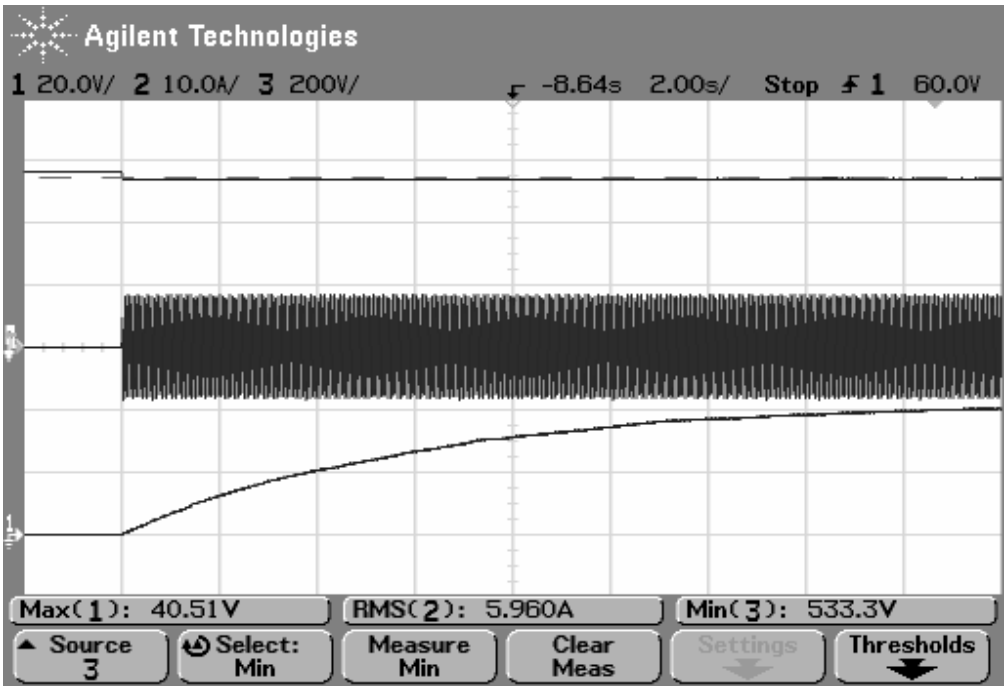


Figure 5.12 The DC bus voltage, the load current, and the neutral point potential waveforms (from top to bottom) at f_o=15 Hz and M_i=0.3 (scales: 200 V/div, 10 A/div, 20 V/div, 2 s/div).

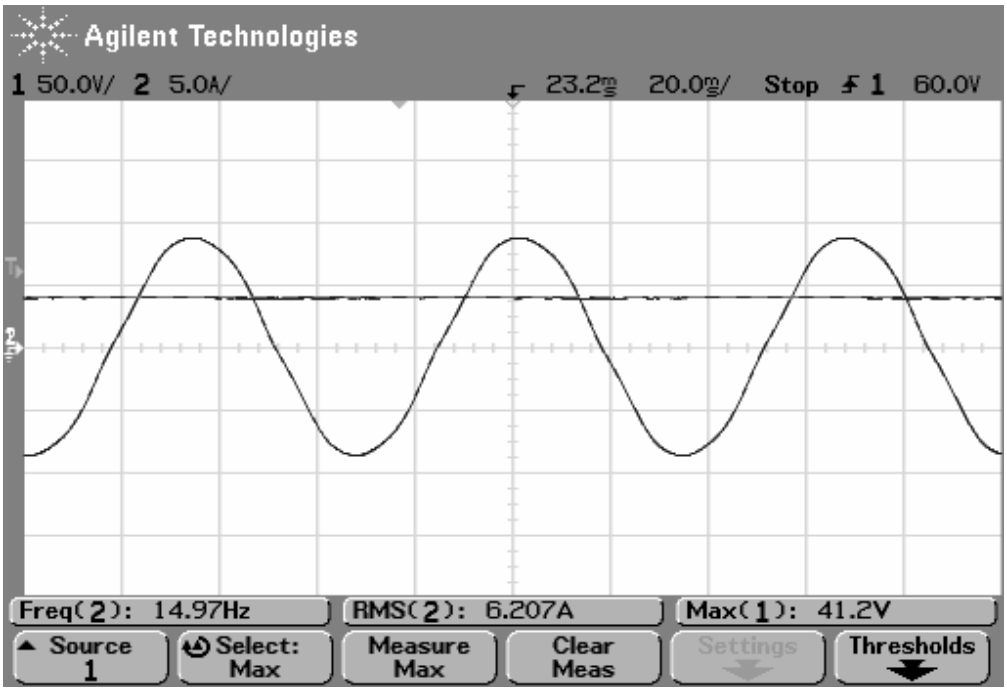


Figure 5.13 Load current and the neutral point potential waveforms at steady-state for f_o=15 Hz and M_i=0.3 (scales: 50 V/div, 5 A/div, 20 ms/div).

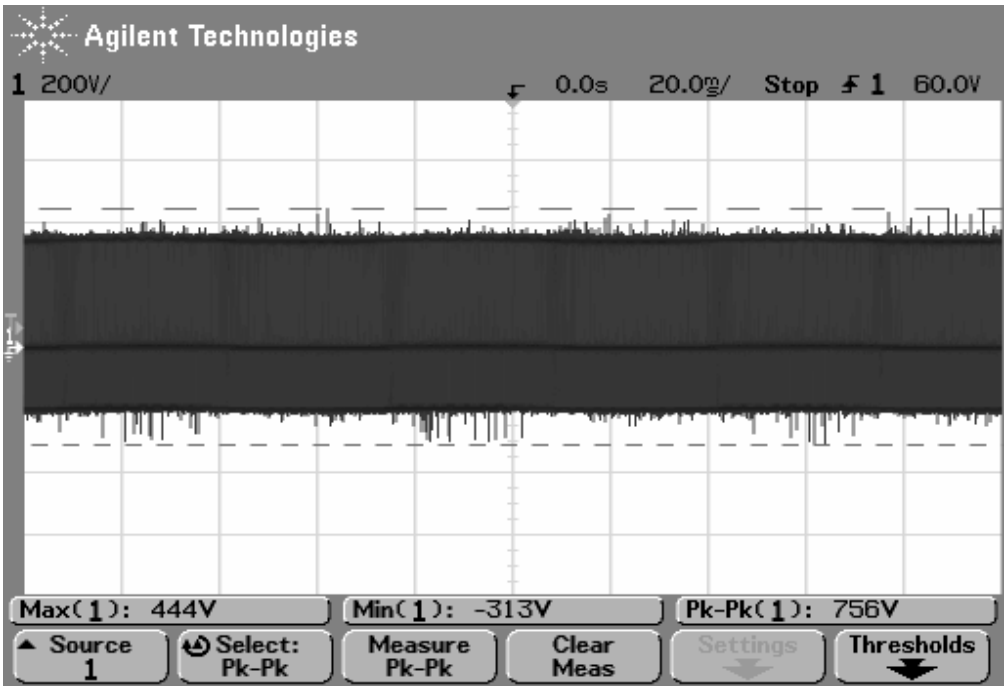


Figure 5.14 The line-to-neutral output voltage waveform at steady-state for f_o=15 Hz and M_i=0.3(scales: 200 V/div, 20 ms/div).

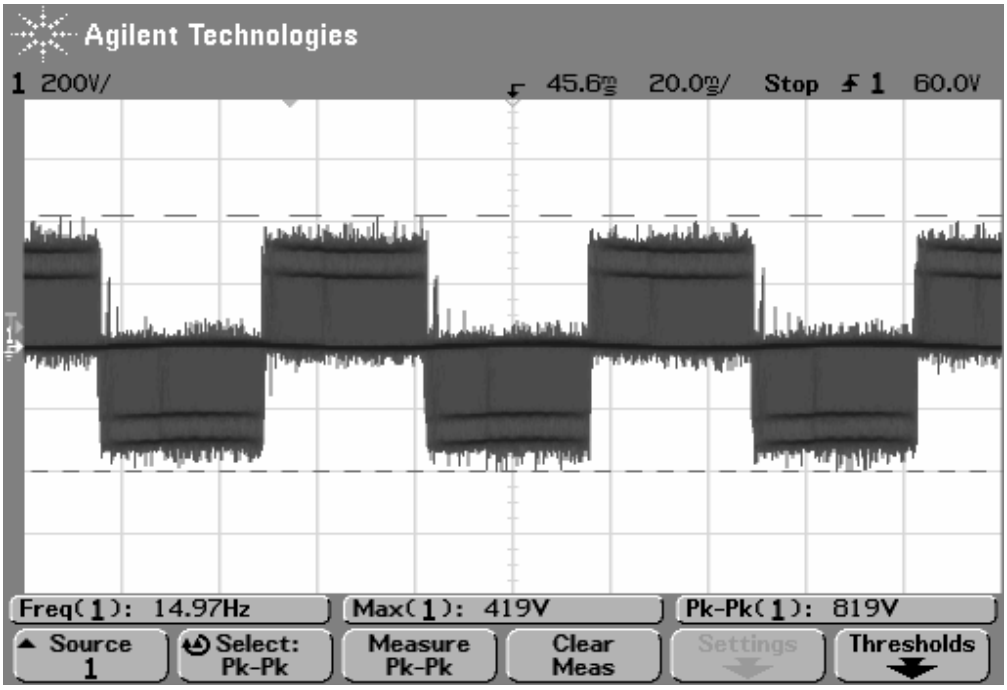


Figure 5.15 The line-to-line output voltage waveform at steady-state for f_o=15 Hz and M_i=0.3 (scales: 200 V/div, 20 ms/div).

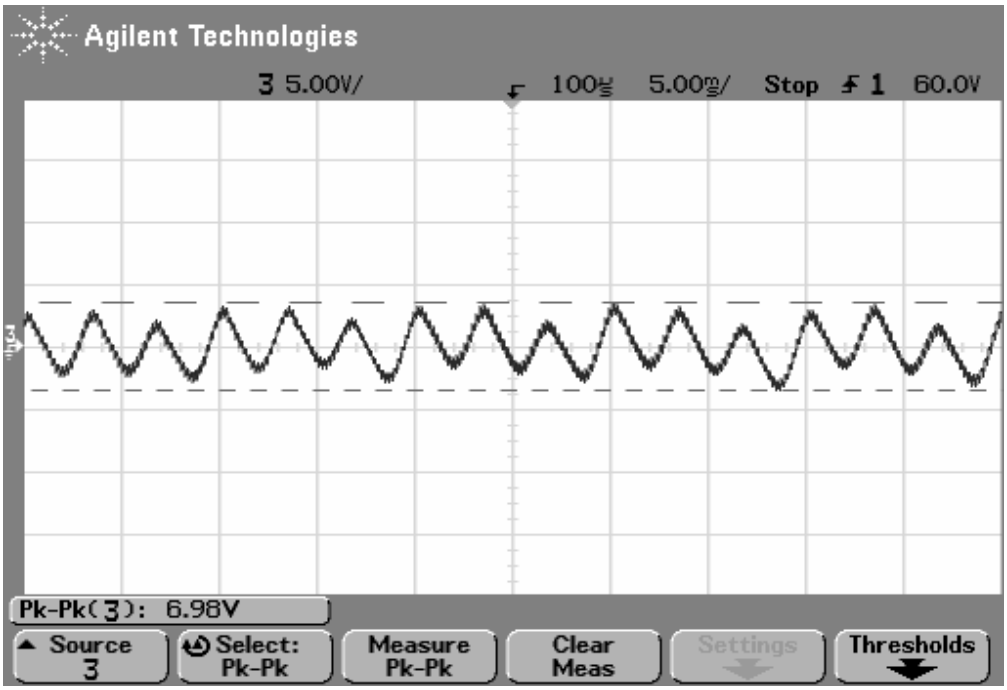


Figure 5.16 DC bus voltage ripple at steady-state for f_o=15 Hz and M_i=0.3 (scales: 5 V/div, 5 ms/div).

The neutral point potential behavior of NTV-PWM without neutral point potential control for f_o=45 Hz and M_i=0.92 is also investigated in the same manner as for the low modulation index. The DC bus voltage, load current, and the neutral point potential waveforms involving the loading transients and steady-state are shown in Figure 5.17. After loading, the DC bus voltage slightly decreases and the neutral point potential starts to drift as shown in Figure 5.17. The neutral point potential drift takes about 5 seconds and its final value is about 32 V when all the signals settle to their steady-state values. At steady-state, the load current and the neutral point potential waveforms are as shown in Figure 5.18. The load current is nearly sinusoidal and the neutral point potential has a dominant triplen harmonic content with 12 V peak-to-peak value. The line-to-line output voltage waveform of the three-level NPC inverter is shown in Figure 5.19. The line-to-line output voltage waveform is distorted and has no waveform symmetry due to the neutral point potential fluctuation and drift. Although the inverter output line-to-line voltage is highly distorted the load current shown in Figure 5.18 appears to be sinusoidal. This is due to the high inductance of the R-L load.

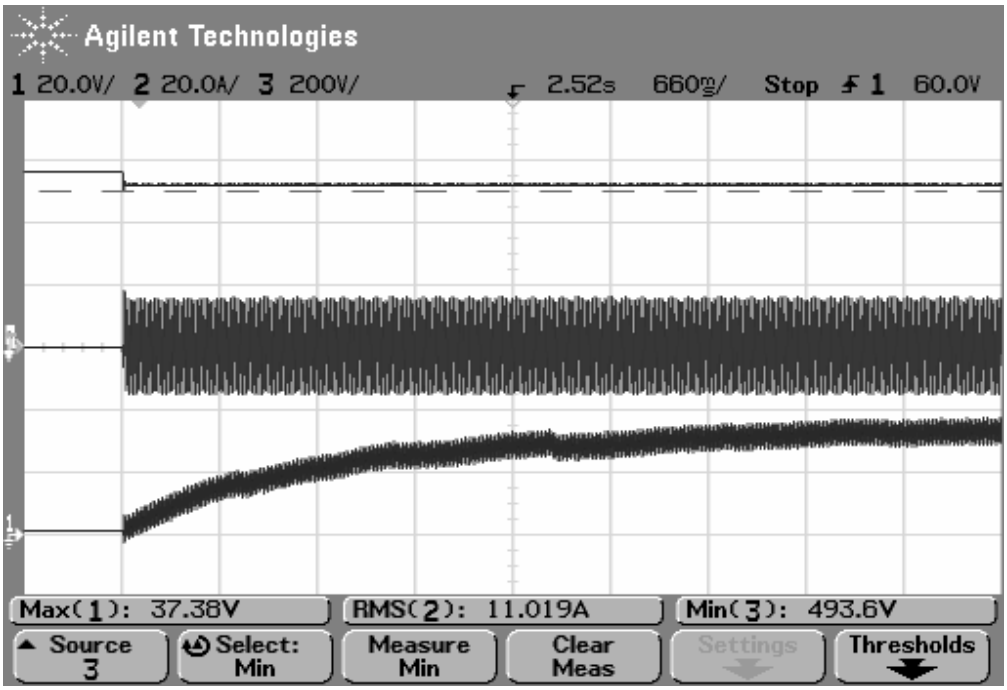


Figure 5.17 The DC bus voltage, the load current, and the neutral point potential waveforms (from top to bottom) at f_o=45 Hz and M_i=0.92 (scales: 200 V/div, 20 A/div, 20 V/div, 660 ms/div).

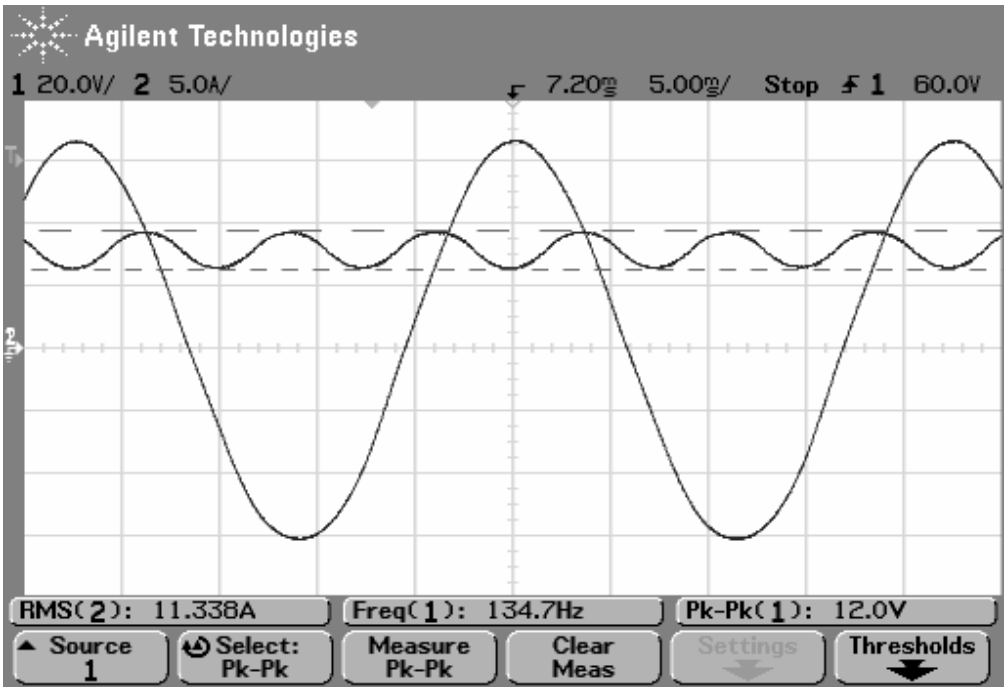


Figure 5.18 Load current and the neutral point potential waveforms at steady-state for f_o=45 Hz and M_i=0.92 (scales: 20 V/div, 5 A/div, 5 ms/div).

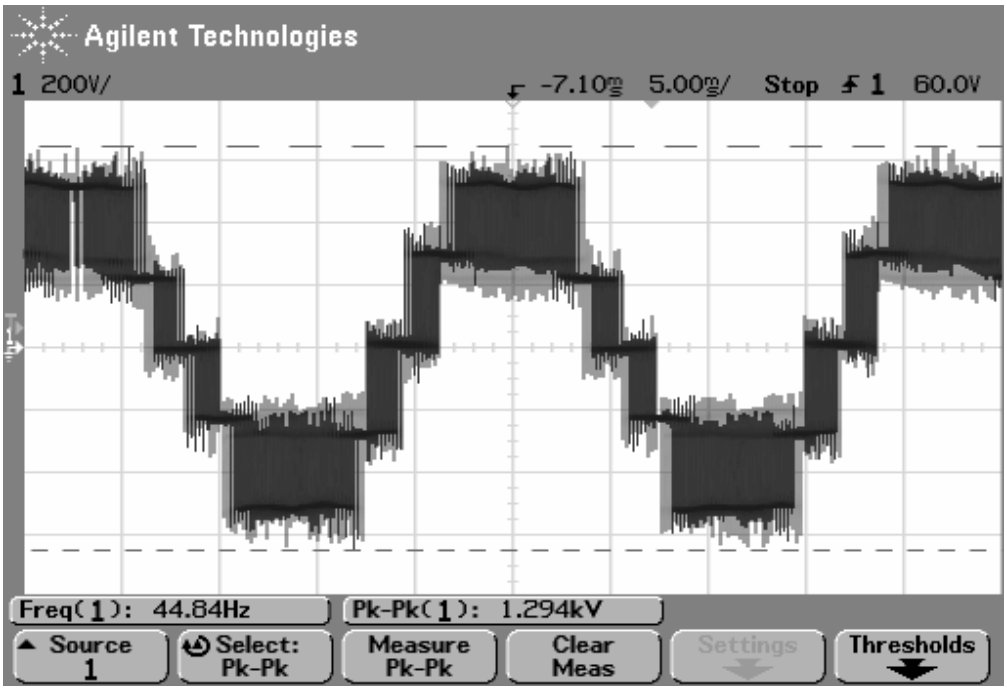


Figure 5.19 The line-to-line output voltage waveform at f_o=45 Hz and M_i=0.92 (scales: 200 V/div, 5 ms/div).

5.3.1.2 NTV-PWM with The Uniform α Control Method

This section presents the experimental R-L load results of NTV-PWM with the uniform α control method. In this case, the redundancy function of the small voltage vectors is uniform ($\alpha_u=\alpha_1=\alpha_2$). The neutral point potential error elimination capability of the method is first tested for low M_i (M_i=0.3) and then for high M_i (M_i=0.92). In these experiments, the start-up of the load is done with the neutral point potential controller being disabled. Thus, at start-up, the neutral point potential drifts and settles to a steady-state value (the values obtained in the experiments of section 5.3.1.1). Then, the controller is activated and the neutral point potential is decreased to zero by the controller. The time from the maximum neutral point potential drift to zero is observed and compared to those obtained in the computer simulations of chapter 4.

First for f_o=15 Hz and M_i=0.3 the results are presented. In Figure 5.20, the DC bus voltage, load current, and the neutral point potential waveforms are shown. As seen

from the figure, the uniform α controller is enabled after the neutral point potential error stabilizes at about 40 V. The uniform α controller decreases the neutral point potential error to zero in about 20 ms. The 20 ms time to zero error is significantly short compared to the error settling time which is 15 seconds. Therefore, the uniform α controller acts rapidly and effectively on the error. The DC bus voltage is not effected by the uniform α controller, as shown in Figure 5.20. The load current and the neutral point potential waveforms are shown in Figure 5.21. The load current is nearly sinusoidal and the neutral point potential has no potential drift and no triplen harmonic content. The line-to-neutral output voltage of the inverter is illustrated in Figure 5.22. As seen from the figure, the line-to-neutral output voltage waveform has no DC offset. The line-to-line output voltage waveform of the inverter is shown in Figure 5.23. The line-to-line output voltage waveform has noticeable distortion as seen from the figure. The line-to-line output voltage has frequent polarity reversals which would not occur when the neutral point potential controller was not enabled (see Figure 5.15). In Figure 5.23, the distortion appears as narrow notches arising due to the inverter dead-time. The SKHI 22A gate driver modules have built-in analog dead-time circuits. In each gate driver, the dead-time is adjusted via a circuit consisting of a resistor, a capacitor and a diode. The values of these components in each gate driver module are different due to manufacturing tolerances. Thus, the analog dead-time circuit of each module creates a different dead-time from the dead-time of other modules. When the uniform α controller is activated and operates with the optimal value to maximize the charge for the neutral point potential error to become zero at the shortest available time, the α variable frequently expires (reaches the boundaries of zero or one). Under such circumstances, one of the small redundant voltage vectors theoretically disappears. However, due to the unequal dead-time values, an unexpected narrow pulse appears at the line-to-line voltage. Therefore, line-to-line output voltage waveform gets distorted. The uniform α parameter is an internal variable inside the DSP and its value can not be exported to the oscilloscope screen. However, its time variation could be obtained from the TI-DSP Code Composer Studio (CCS) graphic window which is the DSP development kit accessory [27]. The uniform α parameter obtained from this graphic window is illustrated in Figure 5.24. As can be seen from the waveform, the uniform α

parameter frequently reaches the boundaries of zero or one in order to eliminate the neutral point potential error.

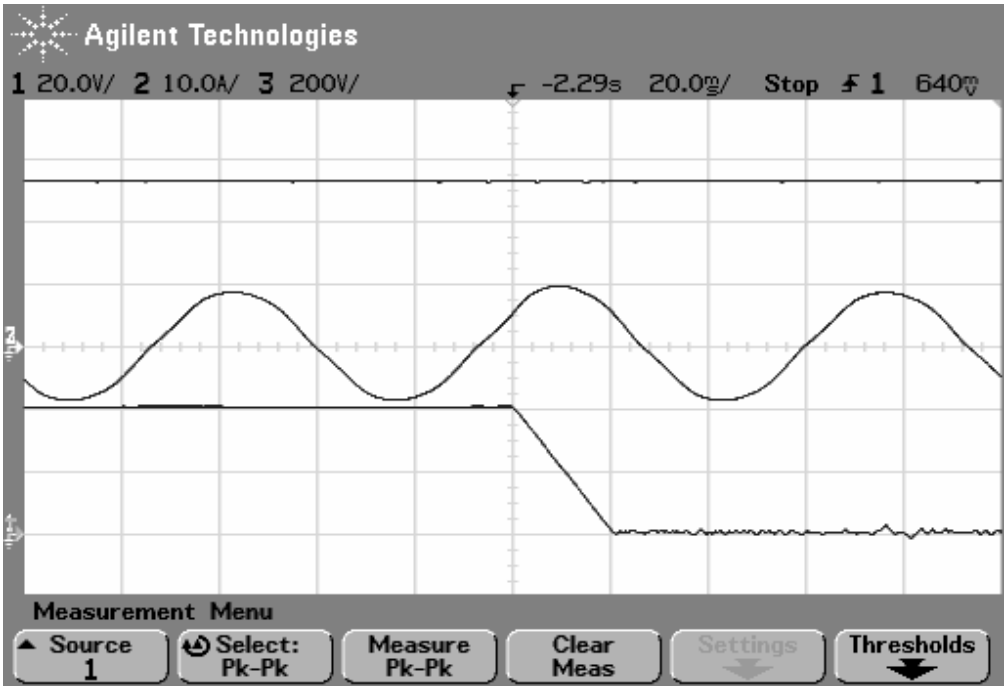


Figure 5.20 The DC bus voltage, the load current, and the neutral point potential waveforms (from top to bottom) at f_o=15 Hz and M_i=0.3 (scales: 200 V/div, 10 A/div, 20 V/div, 20 ms/div).

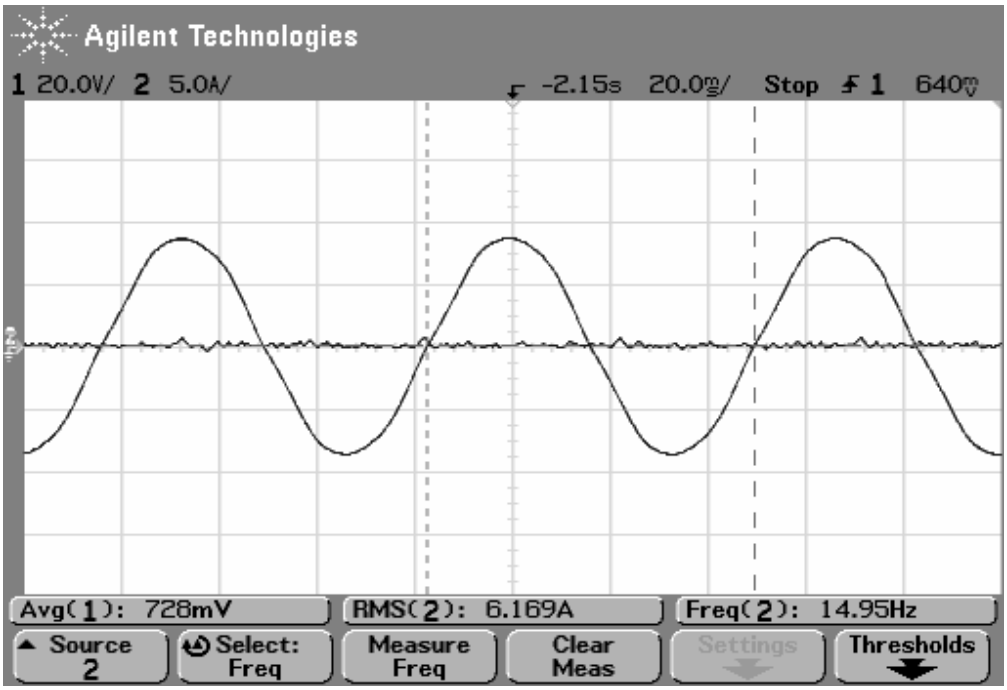


Figure 5.21 Load current and the neutral point potential waveforms at steady-state for f_o=15 Hz and M_i=0.3 (scales: 20V/div, 5A/div, 20ms/div).

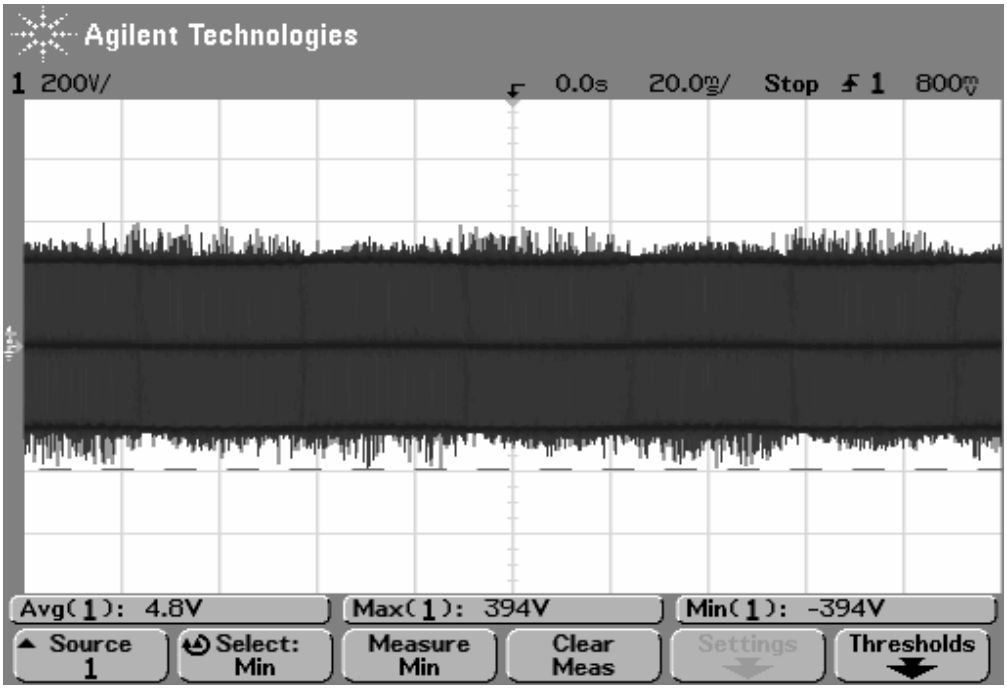


Figure 5.22 The line-to-neutral output voltage waveform at steady-state for f_o=15 Hz and M_i=0.3 (scales: 200 V/div, 20 ms/div).

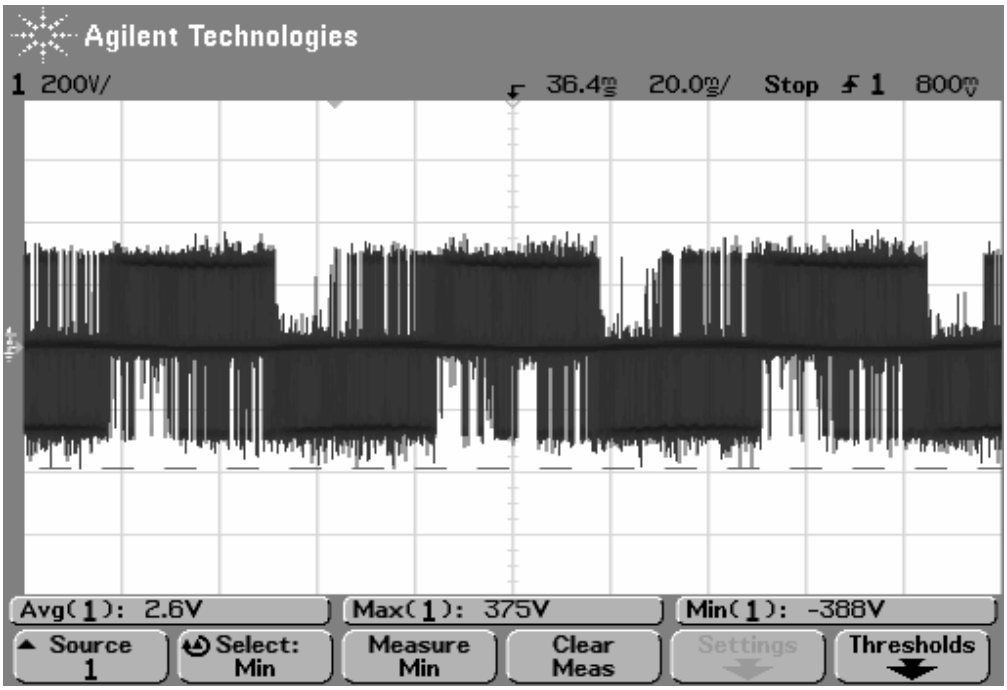


Figure 5.23 The line-to-line output voltage waveform at steady-state for f_o=15 Hz and M_i=0.3 (scales: 200 V/div, 20 ms/div).

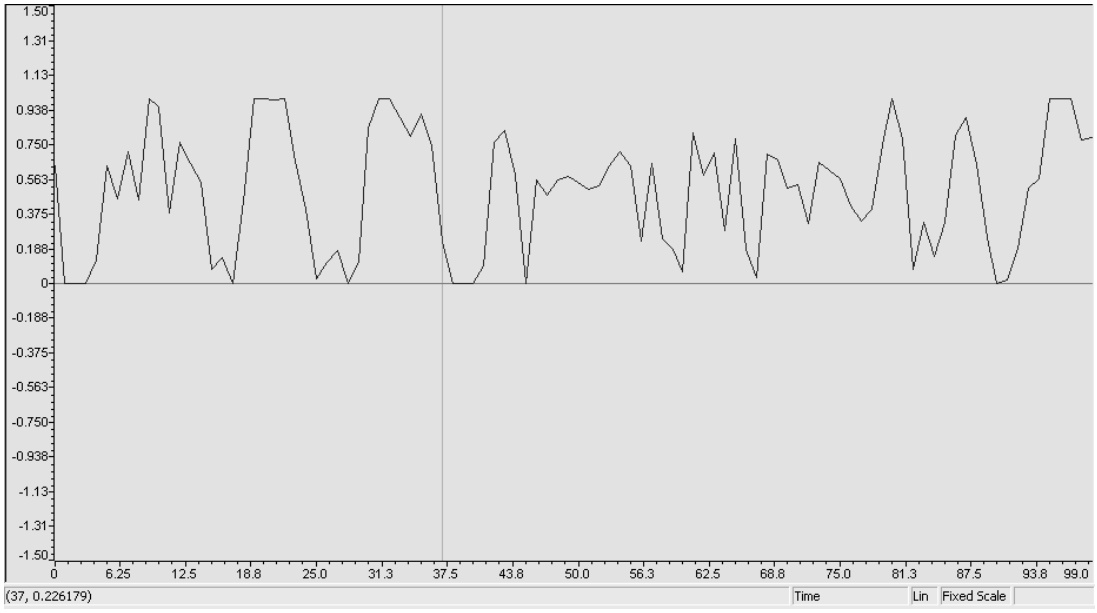


Figure 5.24 The uniform α parameter at steady-state for f_o=15 Hz and M_i=0.3.

Second, for f_o=45 Hz and M_i=0.92 the results are presented. In Figure 5.25, the DC bus voltage, load current, and the neutral point potential waveforms are shown. As seen from the figure, the uniform α controller is enabled after the neutral point potential error reached to about 30 V. The uniform α controller decreases the neutral point potential average value error to zero in about 60 ms. Although the average value of the neutral point potential error (the drift) is eliminated, the ripple is still present. The triplen harmonic content is dominant on the neutral point potential as shown in Figure 5.26. The load current is nearly ripple free and has nearly sinusoidal waveform. The line-to-line output voltage waveform is shown in Figure 5.27. It has five different voltage levels. The waveform has better waveform quality than the NTV-PWM without neutral point potential control. The uniform α parameter is illustrated in Figure 5.28. As seen from the figure, the uniform α parameter frequently reaches boundaries.

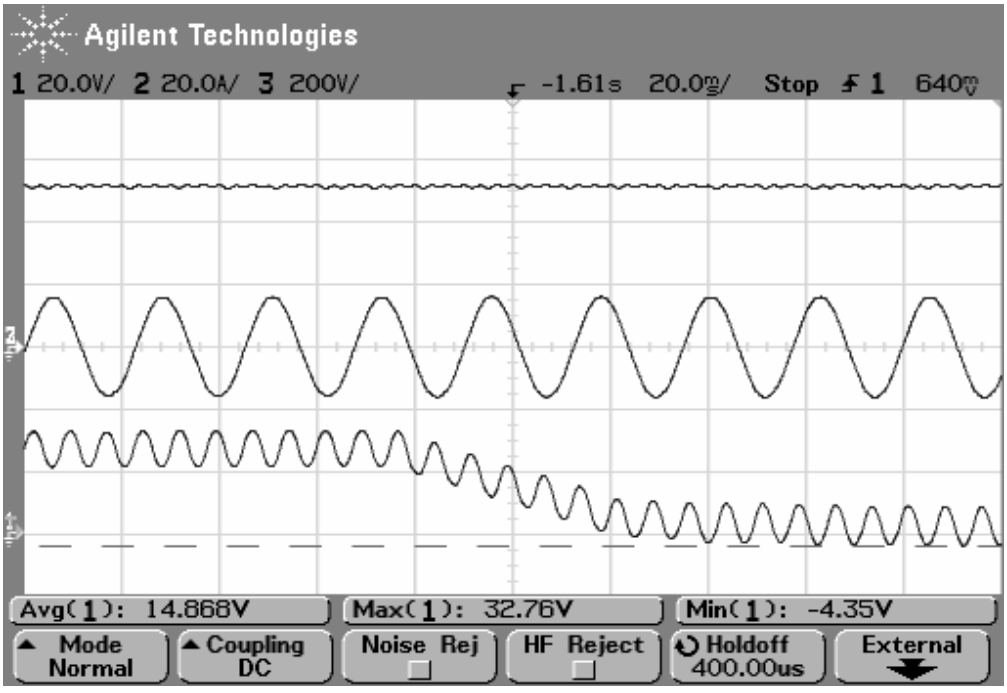


Figure 5.25 The DC bus voltage, the load current, and the neutral point potential waveforms (from top to bottom) at f_o=45 Hz and M_i=0.92 (scales: 200 V/div, 20 A/div, 20 V/div, 20 ms/div).

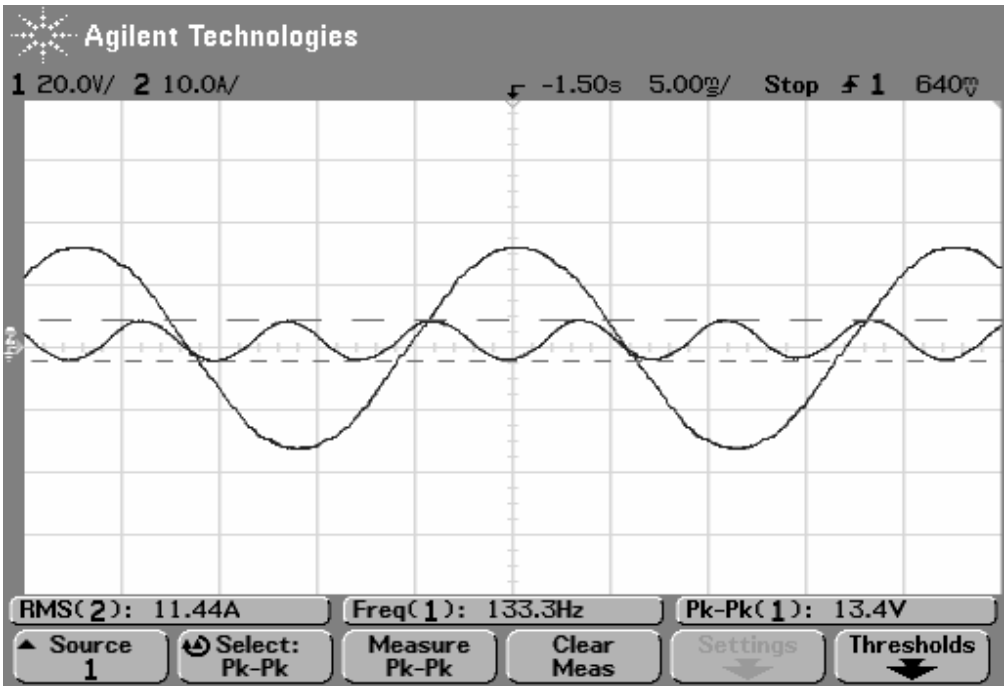


Figure 5.26 Load current and the neutral point potential waveforms at steady-state for f_o=45 Hz and M_i=0.92 (scales: 20 V/div, 10 A/div, 5 ms/div).

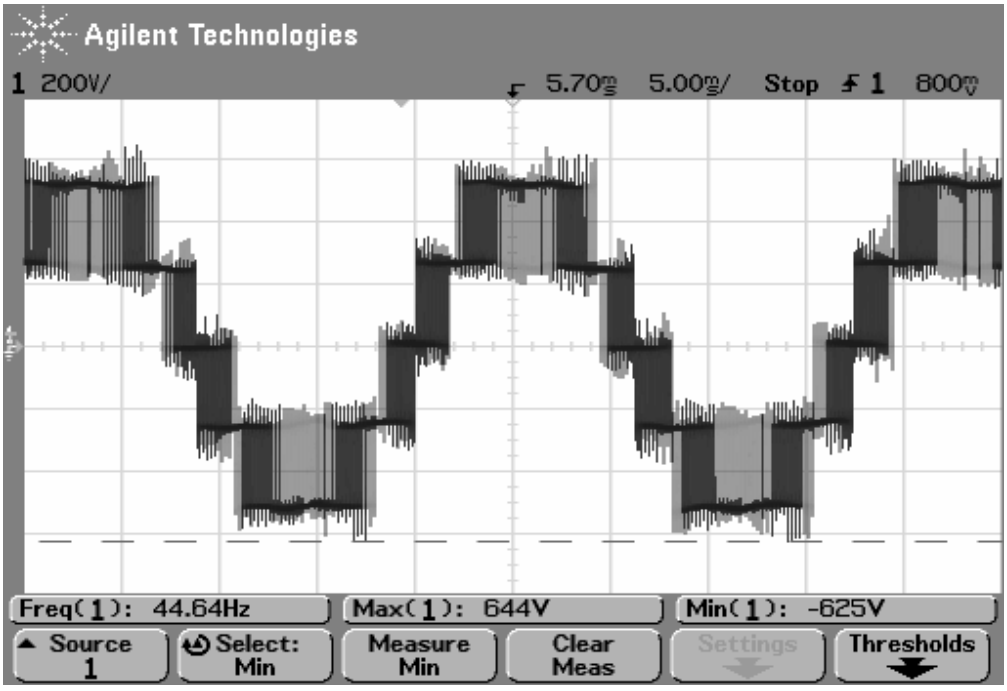


Figure 5.27 The line-to-line output voltage waveform at steady-state for f_o=45 Hz and M_i=0.92 (scales: 200 V/div, 5 ms/div).

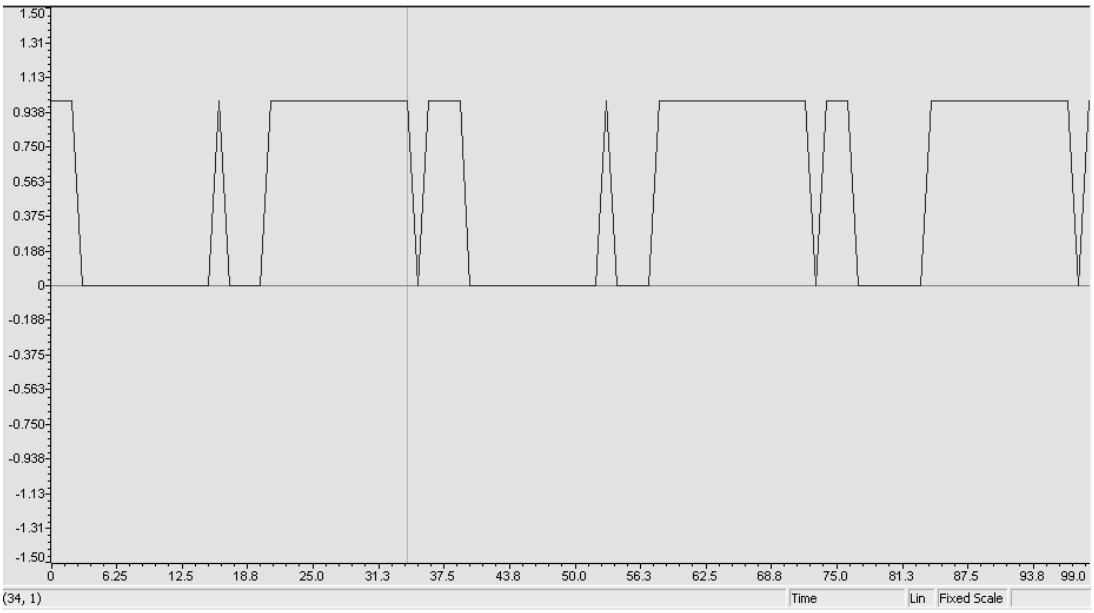


Figure 5.28 The uniform α parameter at steady-state for f_o=45 Hz and M_i=0.92.

5.3.1.3 NTV-PWM with The Optimal α Control Method

This section presents the experimental R-L load results of NTV-PWM with the optimal α control method. In this case, the redundancy functions of the small voltage vectors are coordinated in order to obtain maximum charge from the small voltage vectors. The neutral point potential error elimination capability of the method is first tested for low M_i (M_i=0.3) and then for high M_i (M_i=0.92). In these experiments, the same procedure is followed as the uniform α control method section. The time from the maximum neutral point potential drift to zero is observed and compared to those obtained in the computer simulations of chapter 4.

First for f_o=15 and M_i=0.3 the results are presented. In Figure 5.29, the DC bus voltage, the load current, and the neutral point potential waveforms are shown. As seen from the figure, the optimal α controller is enabled after the neutral point potential error reaches to about 40 V. The optimal α controller eliminates the neutral point potential error to zero in about 20 ms. Therefore, the optimal α controller decreases the error effectively. The DC bus voltage is not effected by the optimal α controller, as shown in Figure 5.29. The load current and the neutral point potential

waveforms are shown in Figure 5.30. The load current is nearly sinusoidal and the neutral point potential has no potential drift and no triplen harmonic content, which is the same as the uniform α control method. The line-to-line output voltage waveform of the three-level NPC inverter is shown in Figure 5.31. The line-to-line output voltage waveform has noticeable distortion as seen from the figure. The line-to-line output voltage has frequent polarity reversals which would not occur when the neutral point potential controller was not enabled (see Figure 5.15). The reason for the polarity reversals is the gate driver modules unbalanced dead-times, as mentioned previous section. The optimal α parameter obtained from the CCS graphic window is illustrated in Figure 5.32. As can be seen from the waveform, the optimal α parameter frequently reaches the boundaries of zero or one in order to eliminate the neutral point potential error.

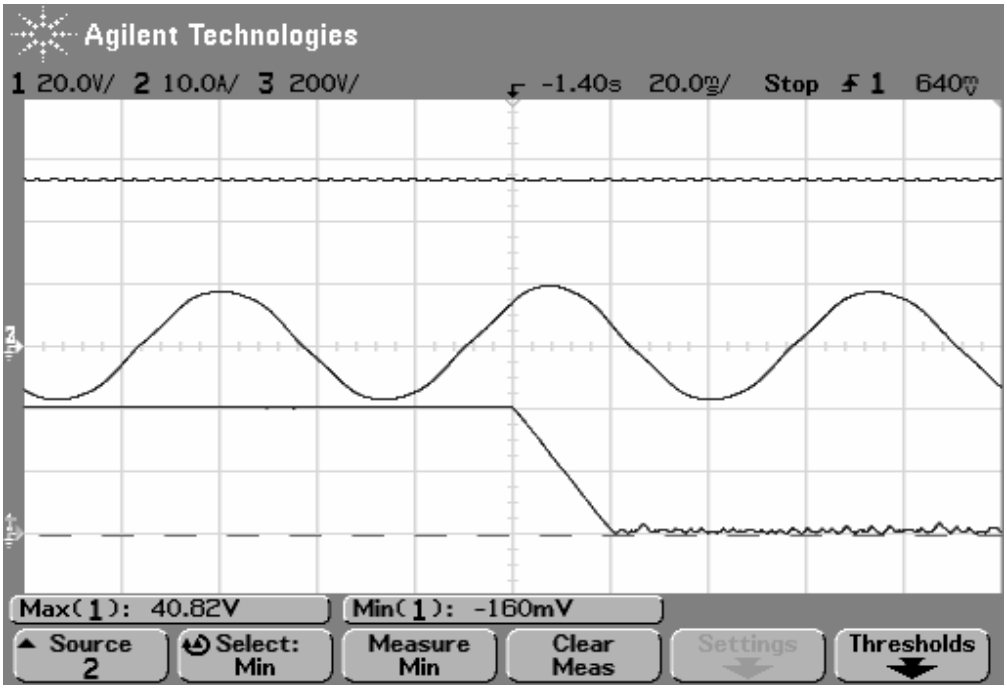


Figure 5.29 The DC bus voltage, the load current, and the neutral point potential waveforms (from top to bottom) at f_o=15 Hz and M_i=0.3 (scales: 200 V/div, 10 A/div, 20 V/div, 20 ms/div).

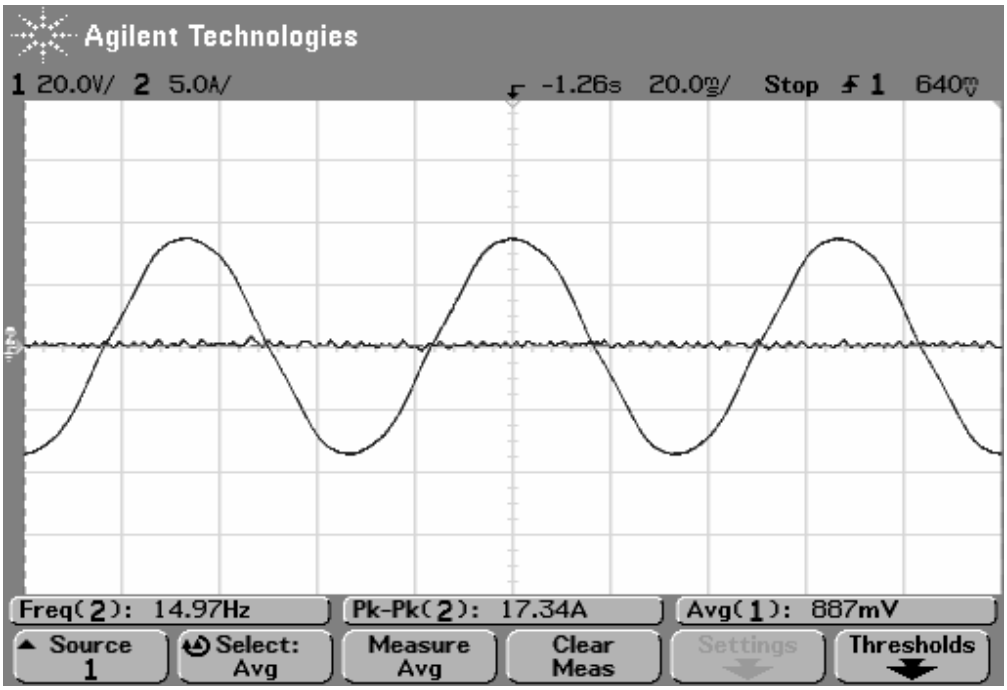


Figure 5.30 Load current and the neutral point potential waveforms at steady-state for f_o=15 Hz and M_i=0.3 (scales: 20 V/div, 5 A/div, 20 ms/div).

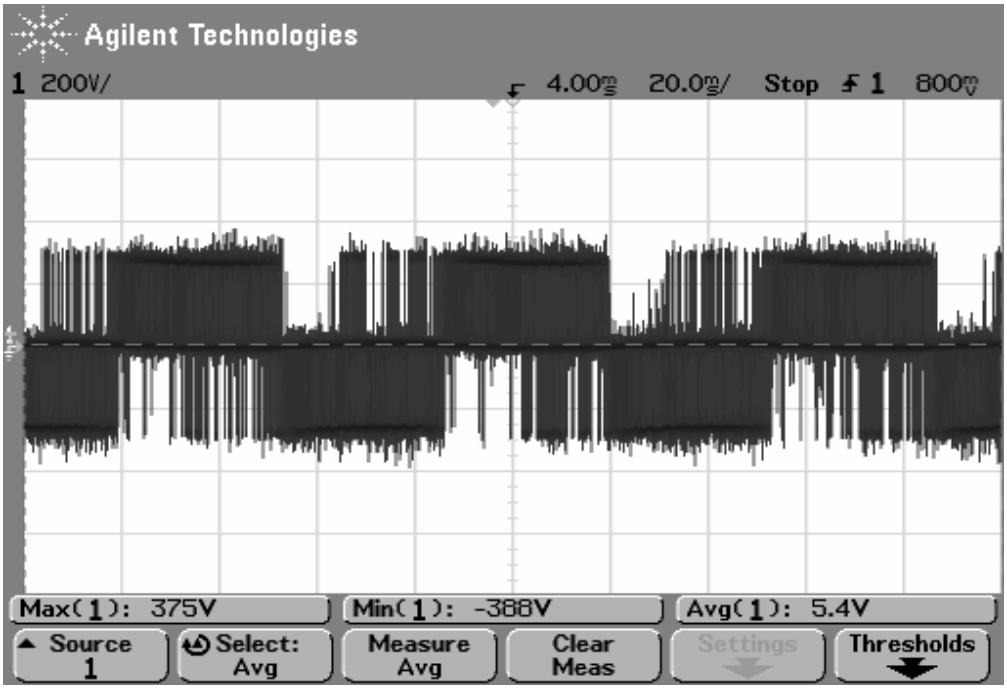


Figure 5.31 The line-to-line output voltage waveform at steady-state for f_o=15 Hz and M_i=0.3 (scales: 200 V/div, 20 ms/div).

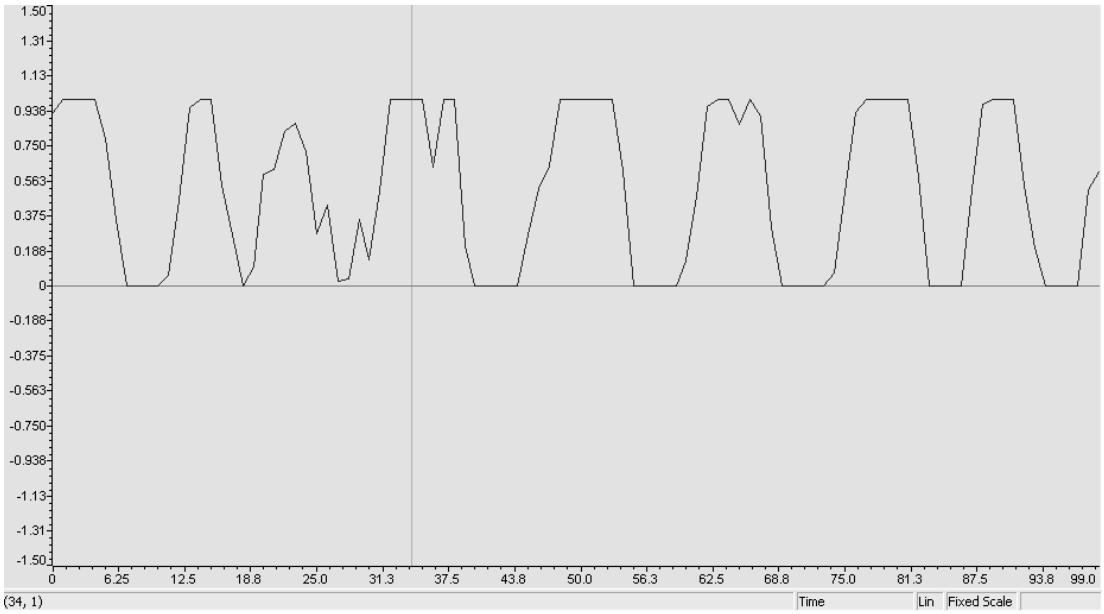


Figure 5.32 The optimal α parameter at steady-state for f_o=15 Hz and M_i=0.3.

Second for f_o=45 Hz and M_i=0.92 the results are presented. In Figure 5.33, the DC bus voltage, load current, and the neutral point potential waveforms are shown. As seen from the figure, the optimal α controller is enabled after the neutral point potential error reached to about 40 V. The optimal α controller decreases the neutral point potential average value error to zero in about 60 ms. Although the average value of the neutral point potential error (the drift) is eliminated, the ripple is still present. The triplen harmonic content is dominant on the neutral point potential as shown in Figure 5.34. The load current is nearly ripple free and has nearly sinusoidal waveform. The line-to-line output voltage waveform is shown in Figure 5.35. The line-to-line output voltage waveform is the same as the uniform α control method. The waveform quality is better than the NTV-PWM without neutral point potential control. The optimal α parameter is illustrated in Figure 5.36. As can be seen from the waveform, the optimal α parameter frequently reaches the boundaries of zero or one in an attempt to eliminate the neutral point potential error.

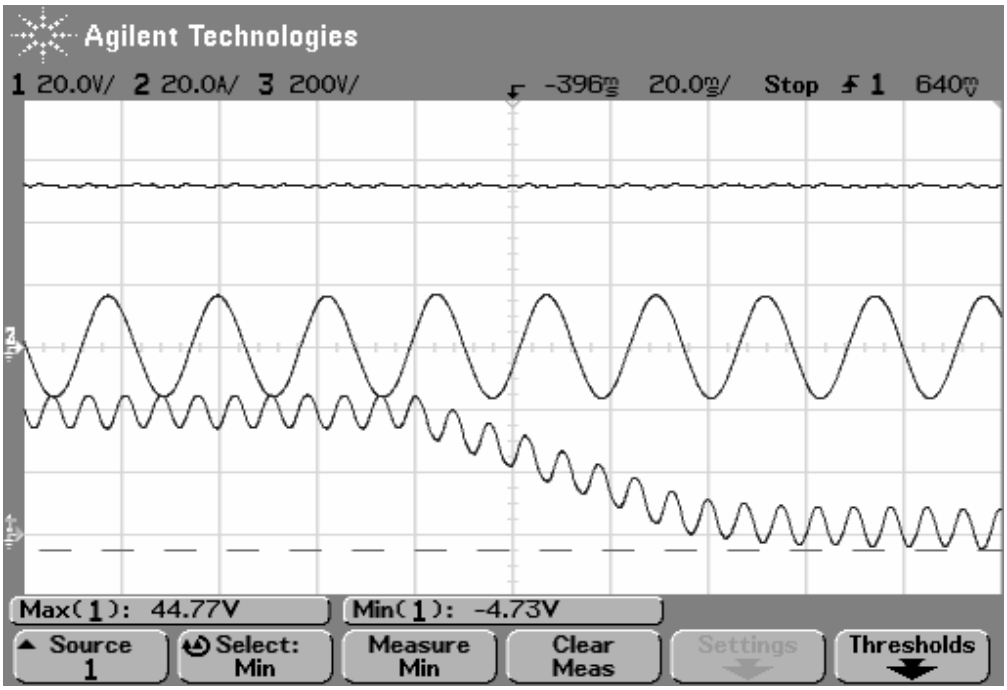


Figure 5.33 The DC bus voltage, the load current, and the neutral point potential waveforms (from top to bottom) at f_o=45 Hz and M_i=0.92 (scales: 200 V/div, 20 A/div, 20 V/div, 20 ms/div).

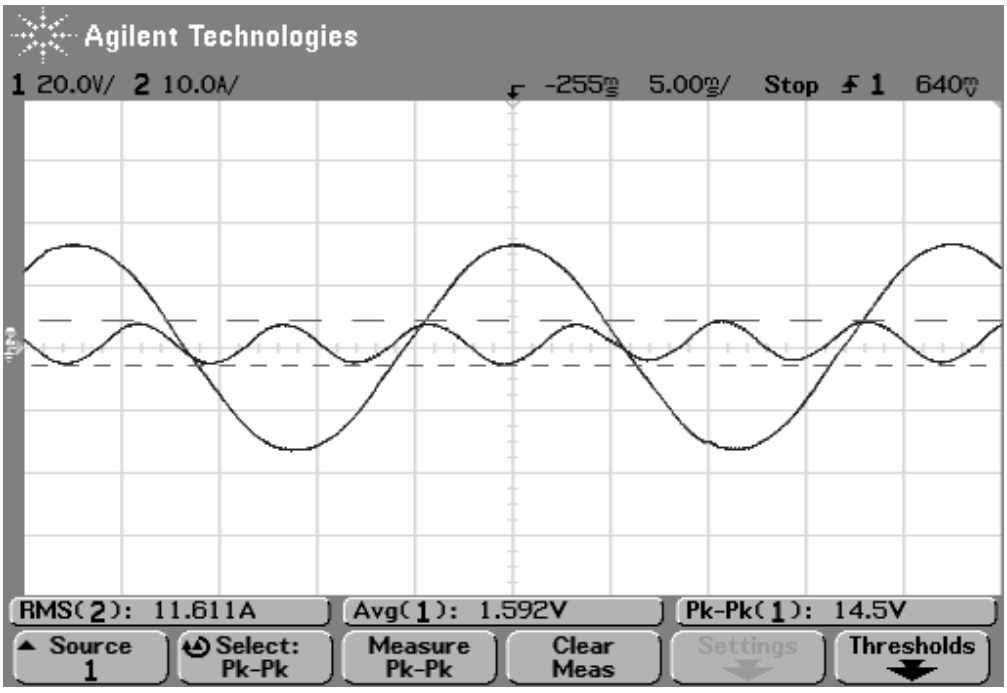


Figure 5.34 Load current and the neutral point potential waveforms at steady-state for f_o=45 Hz and M_i=0.92 (scales: 20 V/div, 10 A/div, 5 ms/div).

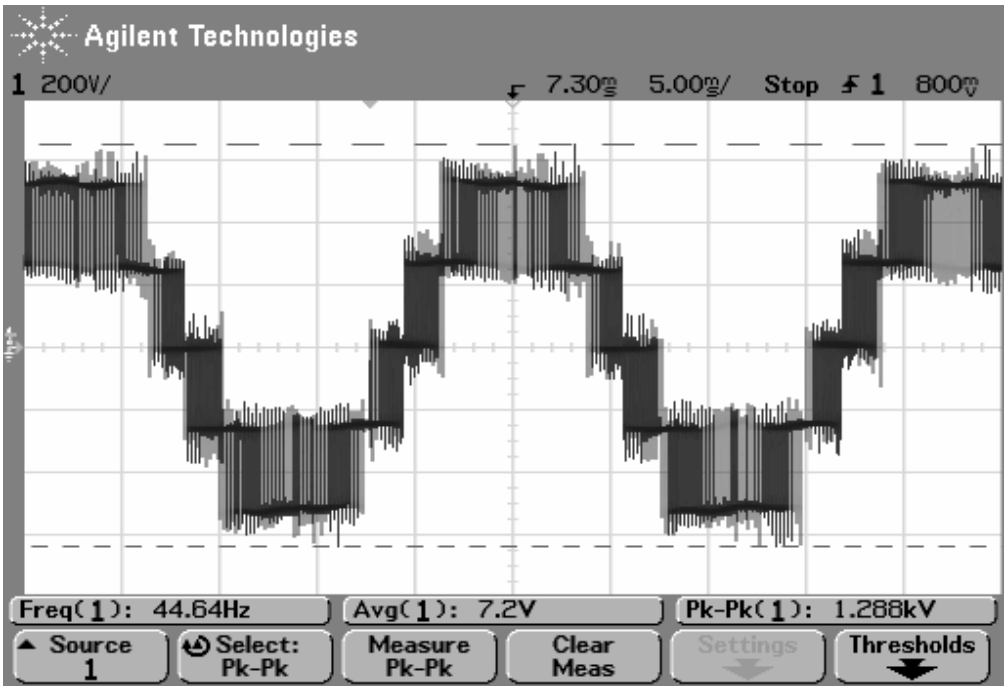


Figure 5.35 The line-to-line output voltage waveform at steady-state for f_o=45 Hz and M_i=0.92 (scales: 200 V/div, 5 ms/div).

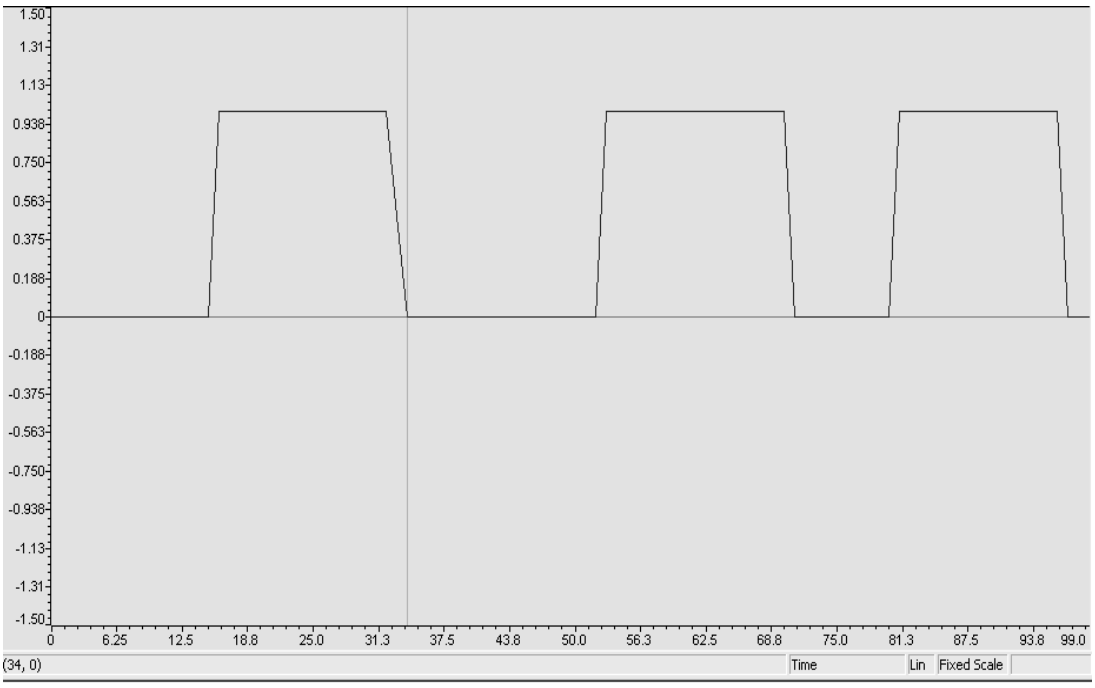


Figure 5.36 The optimal α parameter at steady-state for f_o=45 Hz and M_i=0.92.

5.3.1.4 Two-Parameter PWM with The Optimal α-γ Control Method

This section presents the experimental R-L load results of two-parameter PWM with the optimal α- γ control method. The low modulation index performance of two-parameter PWM with the optimal α-γ control method is exactly same as the optimal α control method case because of the identical controller structure. Therefore, the low modulation index performance is not shown. The neutral point potential error elimination capability of the method is tested only for high M_i (M_i=0.92). In this experiment, the same procedure is followed as the uniform α control method section. The time from the maximum neutral point potential drift to zero is observed and compared to those obtained in the computer simulations of chapter 4.

For f_o=45 Hz and M_i=0.92 the results are presented. In Figure 5.37, the DC bus voltage, load current, and the neutral point potential waveforms are shown. As seen from the figure, two-parameter PWM with the optimal α-γ control method is enabled after the neutral point potential error reached to about 44 V. The optimal α-γ controller decreases the neutral point potential average value error to zero in about 25 ms. The optimal α-γ controller is about 2 times faster than the uniform α and the optimal α control methods for high modulation index range. The average value of the neutral point potential error (the drift) is eliminated and the triplen harmonic content is minimized significantly. The triplen harmonic content is not dominant on the neutral point potential as shown in Figure 5.38. The load current has nearly sinusoidal waveform. The line-to-neutral output voltage waveform is illustrated in Figure 3.39 and the zoom-in view of the line-to-neutral output voltage waveform is shown in Figure 3.40. As seen from Figure 3.40, the line-to-neutral output voltage waveform has direct transitions from the positive DC bus to the negative DC bus. When γ is equal to zero these transitions occur. These direct transitions cause distortion on the output voltage waveforms of the three-level NPC inverter and increase the ripple of the load current. The line-to-line output voltage waveform is as shown in Figure 3.41. The line-to-line output voltage waveform quality is lower than the uniform α control method and the optimal α control method. The zoom-in view of the line-to-line output voltage waveform is illustrated in Figure 3.42. As seen from the figure, when the γ parameter is equal to zero, it has direct transitions from full

DC bus voltage level to zero voltage level. Therefore, the line-to-line output voltage waveform of the three-level NPC inverter is the same as the line-to-line output voltage waveform of the two-level inverter for $\gamma=0$. The α and γ parameters are shown in Figure 3.43. Both α and γ parameters frequently reach the boundary values of zero or one in an attempt to keep the neutral point potential at zero level.

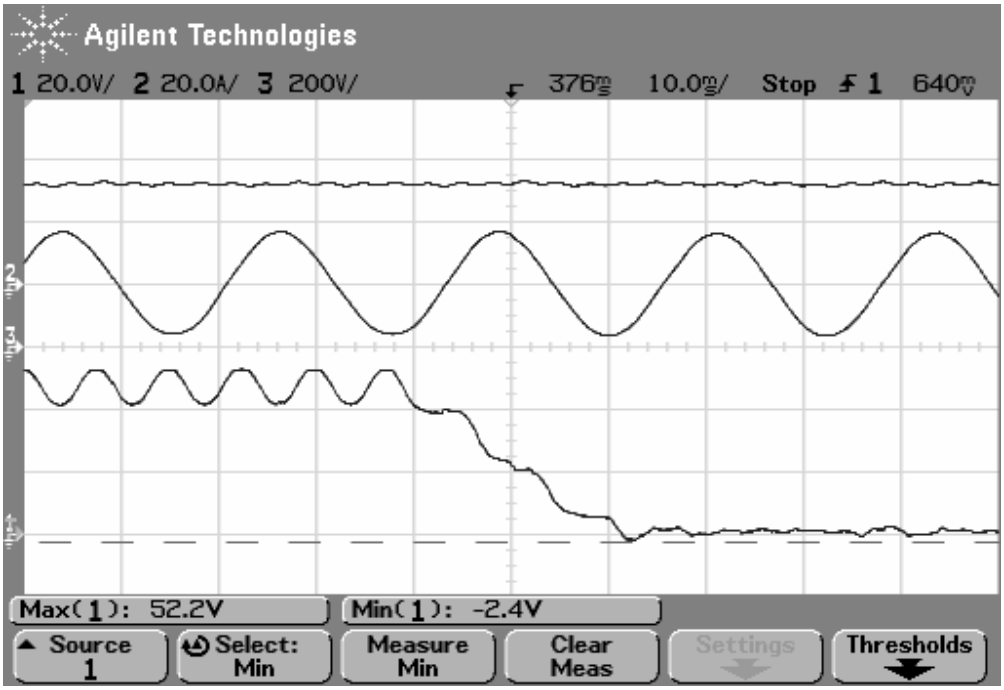


Figure 5.37 The DC bus voltage, the load current, and the neutral point potential waveforms (from top to bottom) at f_o=45 Hz and M_i=0.92 (scales: 200 V/div, 20 A/div, 20 V/div, 10 ms/div).

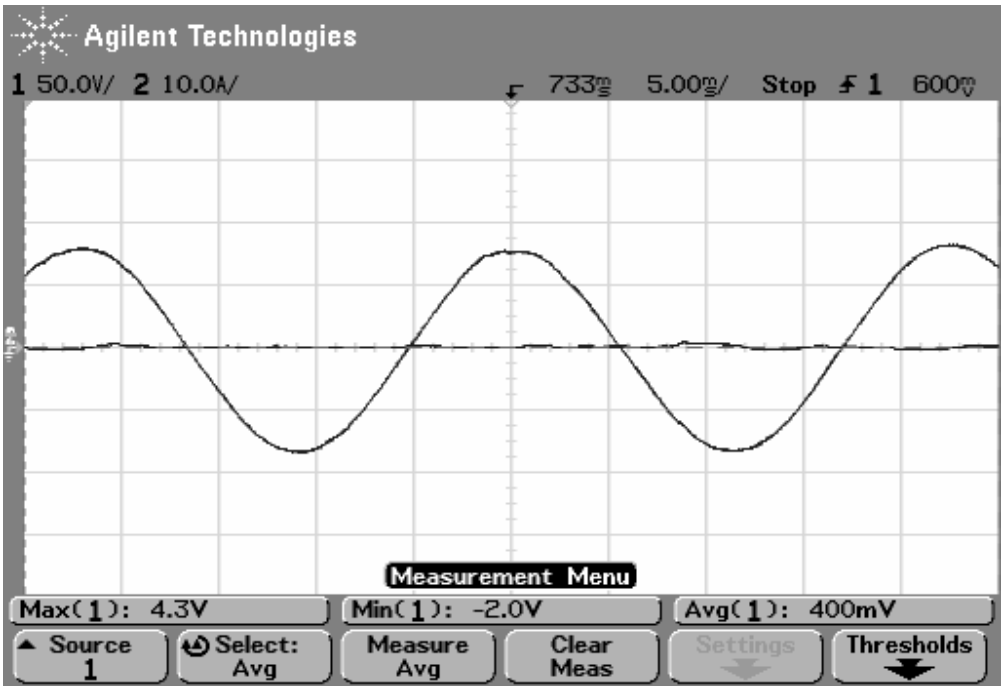


Figure 5.38 Load current and the neutral point potential waveform at steady-state for f_o=45 Hz and M_i=0.92 (scales: 50 V/div, 10 A/div, 5 ms/div).

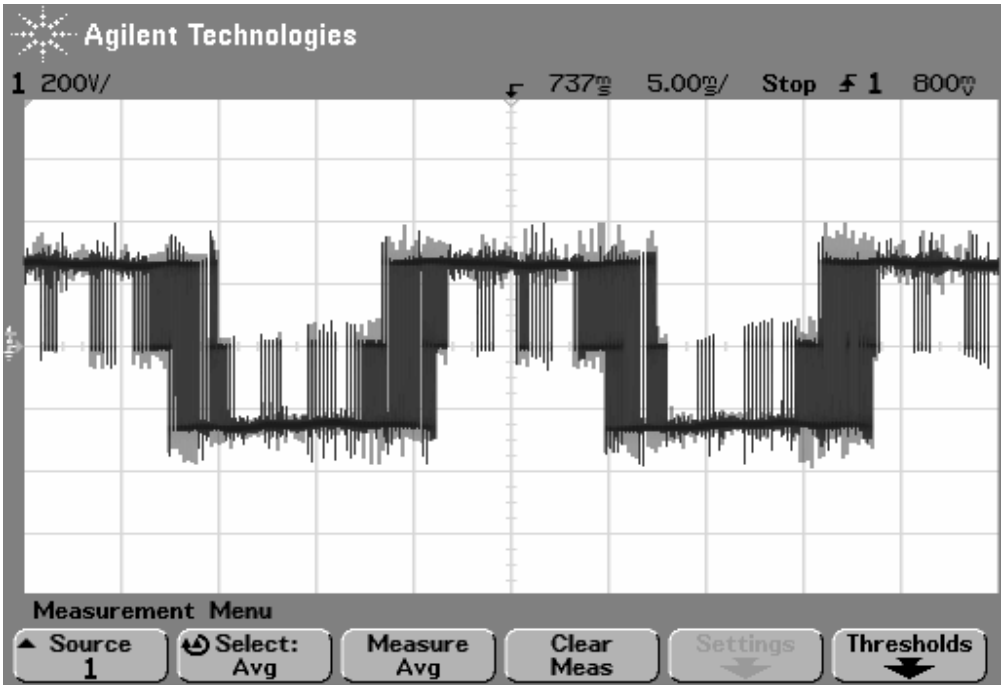


Figure 5.39 The line-to-neutral output voltage waveform at steady-state for f_o=45 Hz and M_i=0.92 (scales: 200 V/div, 20 ms/div).

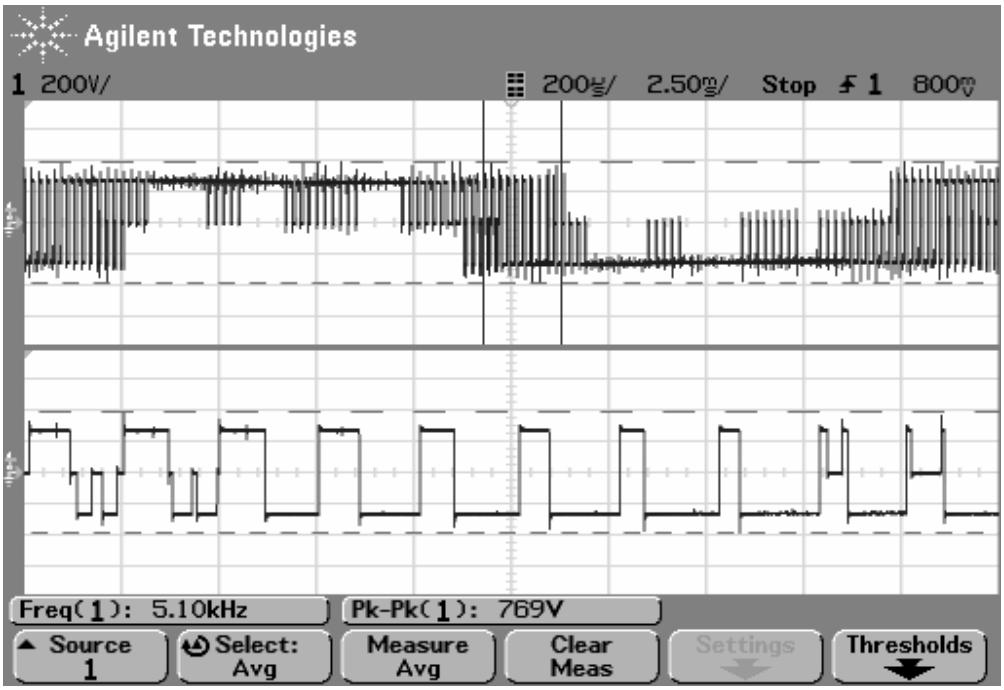


Figure 5.40 The line-to-neutral output voltage and the zoom-in line-to-neutral output voltage waveforms (from top to bottom) at steady-state for f_o=45 Hz and M_i=0.92 (scales: 200 V/div, 200 V/div, 2.5 ms/div, 200 µs/div).

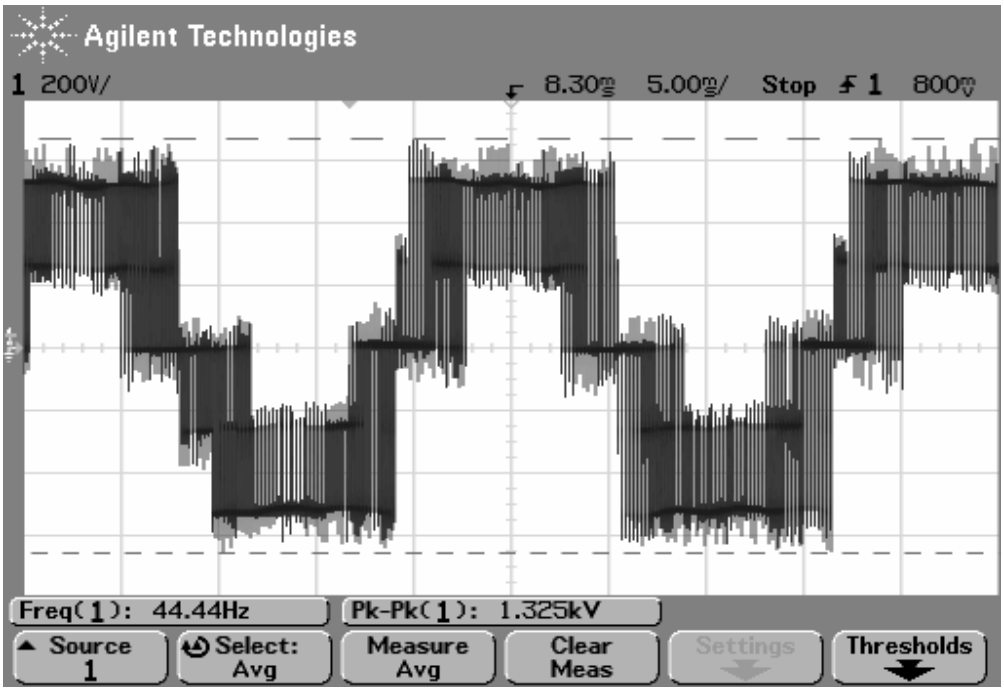


Figure 5.41 The line-to-line output voltage waveform at steady-state for f_o=45 Hz and M_i=0.92 (scales: 200 V/div, 5 ms/div).

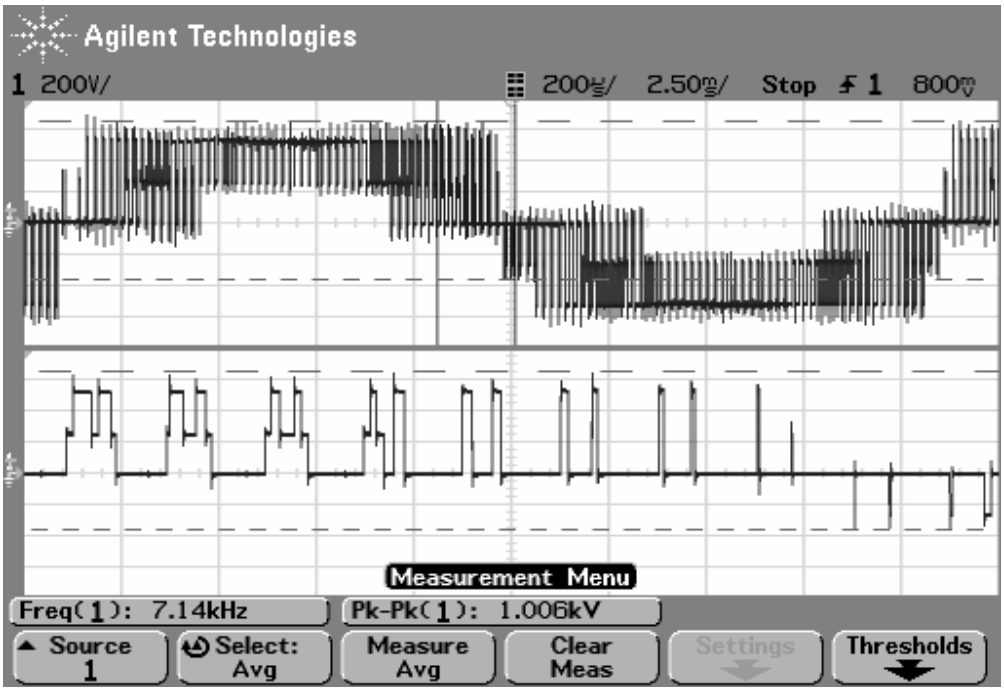


Figure 5.42 The line-to-line output voltage and the zoom-in view of line-to-line output voltage waveforms (from top to bottom) at steady-state for f_o=45 Hz and M_i=0.92 (scales: 200 V/div, 200 V/div, 2.5 ms/div, 200 µs/div).

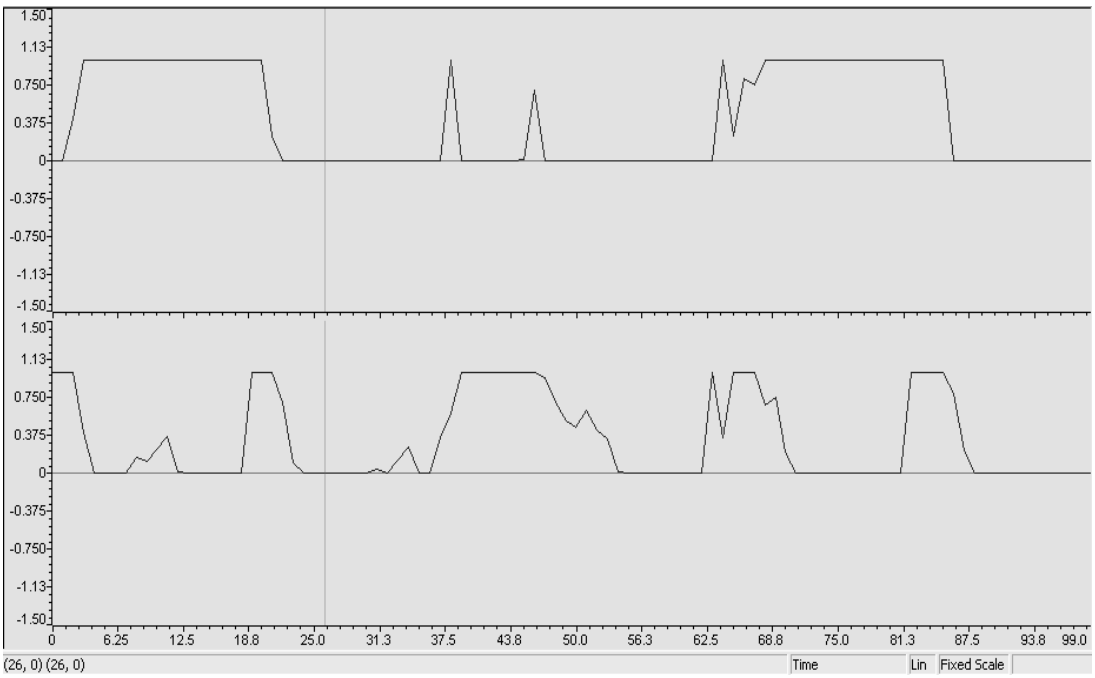


Figure 5.43 The α (top) and γ (bottom) variables at steady-state for M_i=0.92.

5.3.1.5 Performance Comparisons of The Control Methods For R-L Load

Table 5.6 and Table 5.7 summarize the neutral point potential performance of the uncontrolled neutral point potential case along with the three neutral point potential control methods tested for the three phase R-L load in section 5.3.1.1 to 5.3.1.4. The neutral point potential error elimination rate (V/ms) of the three control methods are shown in the tables. Since the neutral point potential drift values could not be obtained equal in all the cases, for a fair comparison it is better to utilize the error elimination rate rather than the time to zero error (of the computer simulations). In Table 5.7, the steady-state peak-to-peak neutral point potential value ΔV_{pp} is also shown.

Table 5.6 illustrates the three control methods have the same performance in the low modulation index range. The uniform α, optimal α, and the optimal α-γ control methods eliminate the 40 V neutral point potential error in 20 ms. Therefore, all neutral point potential control methods have an error elimination rate of 2 V/ms. In the three-phase R-L load computer simulations, the uniform α control method error elimination rate is observed as 1.86 V/ms. There is a correlation between the computer simulations and the experiments. The optimal α and the optimal α-γ control methods have the identical control structure in the low modulation index range as mentioned before. Therefore, in the three-phase R-L load computer simulations both methods have an error elimination rate 1.9 V/ms and the error elimination rate is close to 2 V/ms obtained in experiments. At steady-state the neutral point potential has only PWM frequency ripple with negligibly small magnitude.

The high modulation index performance of the neutral point potential control methods is compared in Table 5.7. The table illustrates the neutral point potential performance superiority of the optimal α-γ control method to the other methods. The optimal α-γ control method eliminates 45 V neutral point potential error in about 20 ms. Therefore, the error elimination rate of the optimal α-γ control method is 2.25 V/ms. This value is about 5 times larger than the error elimination rates of the other control methods. In the three-phase R-L load computer simulation case, the optimal

α-γ control method eliminates the 45 V neutral point potential error in about 19 ms. The error elimination rate is 2.36 V/ms in the computer simulations. The difference between the computer simulation results and the experimental results is in acceptable limits. The uniform α control method has an error elimination rate of 0.5 V/ms as shown in Table 5.7. In the three-phase R-L load computer simulations, the uniform α control method error elimination rate is 0.94 V/ms. The optimal α control method error elimination rate is 0.67 V/ms in the experiments and 0.94 in the computer simulations.

Table 5.6 Performance comparison of various neutral point potential control methods at low modulation index (M_i=0.3, f_o=15Hz)

(f_{PWM}: PWM frequency)

Control Method	Neutral Point Potential Drift	Error Elimination Rate (V/ms)	Neutral Point Potential Ripple Frequency
NTV-PWM (α =0.5)	40 V	Not Applicable	f_{PWM}
Uniform α	None	2	f_{PWM}
Optimal α	None	2	f_{PWM}
Optimal α-γ	None	2	f_{PWM}

Table 5.7 Performance comparison of various neutral point potential control methods at high modulation index (M_i=0.92, f_o=4 5Hz)
(f_{PWM}: PWM frequency and f_o: output voltage fundamental frequency)

Control Method	Neutral Point Potential Drift	Steady-state Peak Voltage ΔV_{pp} (V)	Error Elimination Rate (V/ms)	Neutral Point Potential Ripple Frequency
NTV-PWM (α =0.5)	30 V	12	None	$3f_o$
Uniform α	None	13.4	0.50	$3f_o$
Optimal α	None	14.5	0.67	$3f_o$
Optimal α-γ	None	3	2.25	f_{PWM}

5.3.2 Induction Motor Drive Experimental Results

In this section, the laboratory tests of the three-level inverter feeding an induction motor are conducted. For the induction motor drive experiments, the fan load experimental set-up available in METU Electrical and Electronics Engineering Department, in the Electrical Machines and Power Electronics Laboratory has been used. The motor is a three-phase Y-connected, 3-kW, 400-V, 50-Hz and 2-pole induction motor.

Experimental results are presented for f_o=15 Hz (corresponding to 900 min^{-1} shaft speed command) corresponding to low M_i (M_i=0.29) and f_o=45 Hz (corresponding to 2700 min^{-1} shaft speed command) corresponding to high M_i (M_i=0.87). The induction motor is driven with the constant V/f ratio of 220 V / 50 Hz. The induction motor is accelerated from zero speed to the commanded speed in 1.5 seconds for f_o=15 Hz and is accelerated from zero speed to the commanded speed in 2.6 seconds

for f_o=45 Hz. For the f_o=15 Hz command case, the shaft speed settles at 893 min^{-1} due to the motor slip frequency. For the f_o=45 Hz case shaft speed settles at 2652 min^{-1} at steady state.

First, NTV-PWM without neutral point potential control case experimental results are presented. Second, NTV-PWM with the uniform α control method results are shown for the same operating conditions. Third, NTV-PWM with the optimal α control method results and last, two-parameter PWM with optimal α–γ control method results are presented.

5.3.2.1 NTV-PWM without Neutral Point Potential Control Method

This section presents the experimental results of the NTV-PWM without neutral point potential control. In this case, the redundancy function of the small voltage vectors is set as 0.5 (α=0.5).

First, the low modulation index and low frequency operating condition is tested (M_i=0.29 and f_o=15 Hz). Acceleration transients and steady-state operating conditions are tested both. In the experiment both the start-up and steady-state waveforms are recorded. In Figure 5.44, the DC bus voltage, the motor phase current, and the neutral point potential waveforms are shown. As seen from the figure, as the drive is accelerated from zero speed to the commanded speed, the motor phase current increases and the DC bus voltage experiences a temporary dip. As the motor accelerates and the current decreases, the DC bus voltage recovers. As the figure illustrates, during acceleration the neutral point potential drifts and as the motor currents settle (implying that the motor speed is stabilized) the neutral point potential error settles at a steady-state value. The neutral point potential drift takes about 11 seconds and its final value is about 18 V when all the signals settle to their steady-state values. At steady-state, one of the motor phase currents and the neutral point potential waveforms are as shown in Figure 5.45. The motor current has distorted sinusoidal waveform (low frequency distortion, relating to the inverter dead-time and other nonlinearities at low modulation) and the neutral point potential

has no triplen harmonic content. The line-to-neutral output voltage of the inverter is illustrated in Figure 5.46. As seen from the figure, the line-to-neutral output voltage waveform has approximately 18 V DC offset due to the neutral point potential drift. The line-to-line output voltage waveform of the three-level NPC inverter is shown in Figure 5.47. The line-to-line output voltage waveform is generated from two DC bus voltage levels that are no more equal. This appears on the waveform in the figure as an additional intermediate voltage level. The neutral point potential drift causes distortion on the line-to-line output voltage waveform. In Figure 5.48, the DC bus voltage ripple is shown. As seen from Figure 5.49, the frequency of the ripple is 300 Hz which is six times of the AC supply fundamental frequency of 50 Hz. This is due to the six-pulse diode rectifier characteristics and has no effect on the neutral point potential.

The neutral point potential drift is significantly larger than that of the computer simulation under the same conditions (Figure 4.25). There are several reasons for the difference in the amount and duration of the drift. The computer simulation could not be run for sufficiently long time due to the computational speed and memory allocation constraints of the computer available at the university. Second, the simulation model assumed an ideal inverter with identical switches while in the practical implementation this condition is not satisfied. As previously explained in 5.3.1.1, the switching devices and the gate driver dead-time circuits all contribute to imbalances resulting in a strong neutral point potential drift in the experiments. Thus, the pulse pattern deviates from the ideal and creates conditions favoring the neutral point potential drift when constant α with the value of 0.5 is utilized.

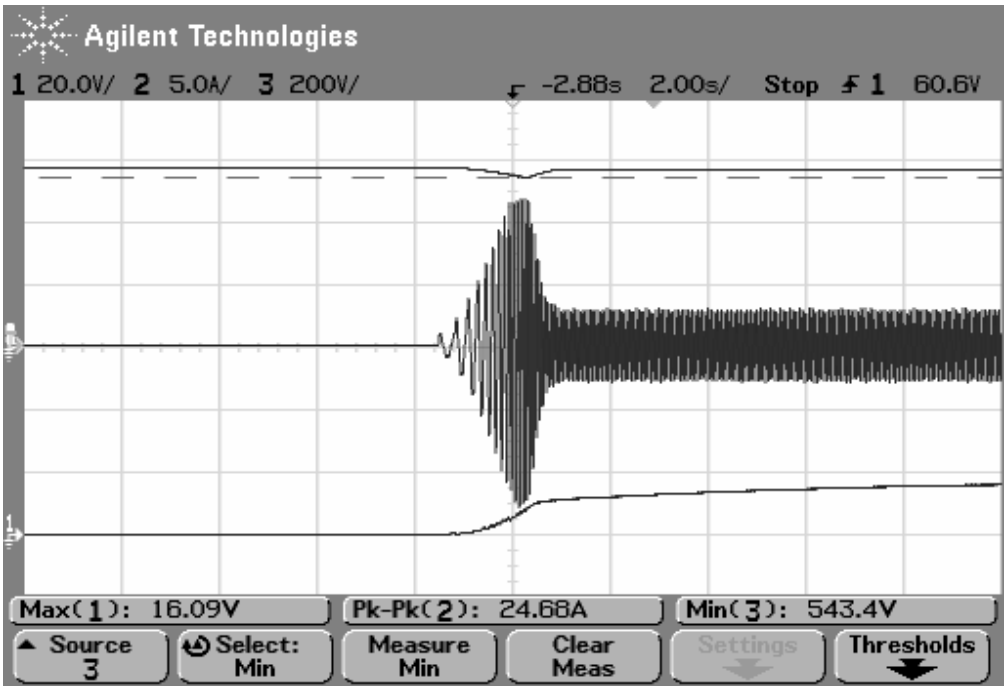


Figure 5.44 The DC bus voltage, the motor phase current, and the neutral point potential waveforms (from top to bottom) at f_o=15 Hz and M_i=0.29 (scales: 200 V/div, 5 A/div, 20 V/div, 10 ms/div).

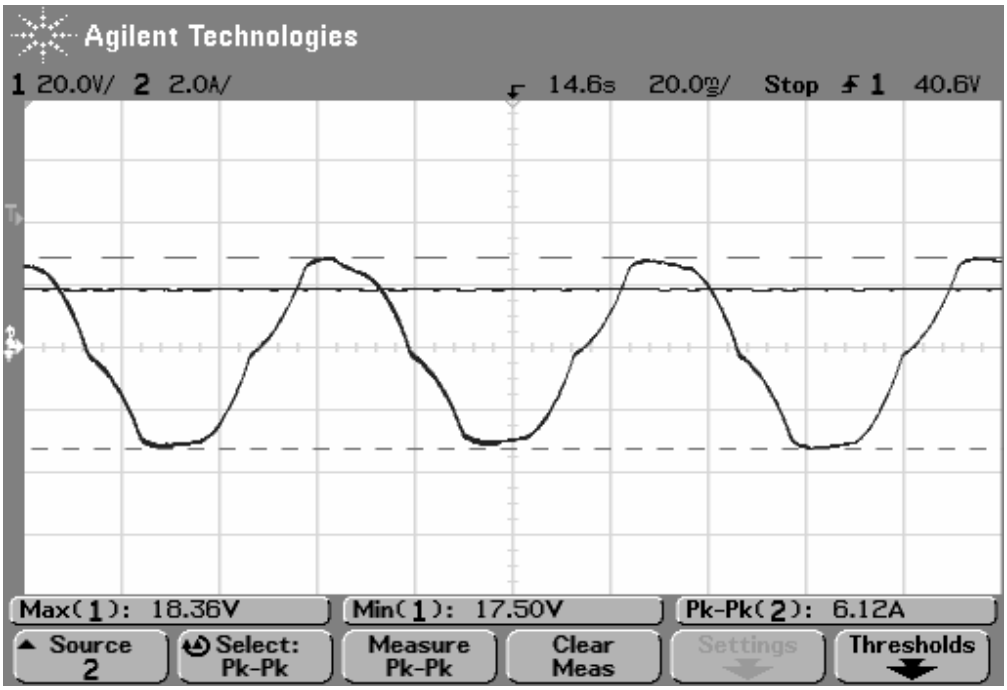


Figure 5.45 Motor phase current and the neutral point potential waveforms at steady-state for f_o=15 Hz and M_i=0.29 (scales: 20 V/div, 2A /div, 20 ms/div).

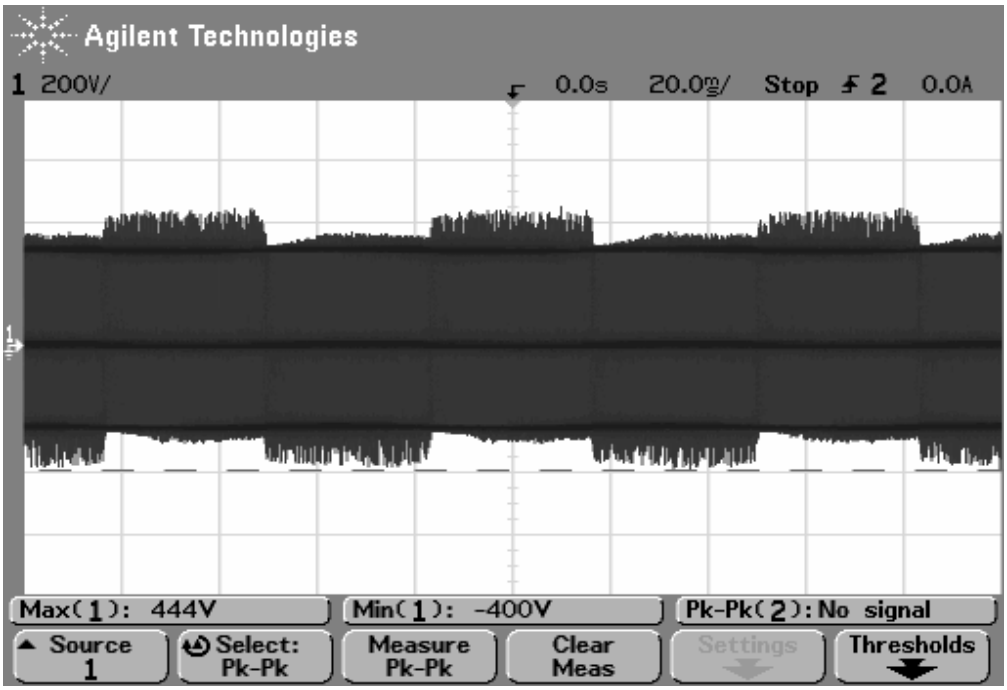


Figure 5.46 The line-to-neutral output voltage waveform at steady-state for f_o=15 Hz and M_i=0.29 (scales: 200 V/div, 20 ms/div).

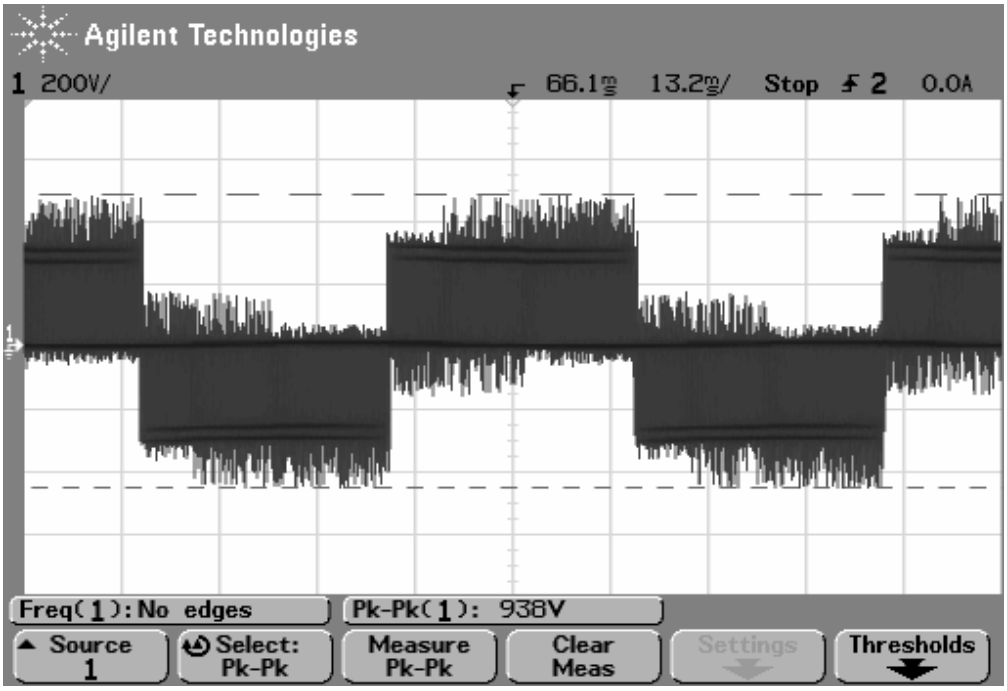


Figure 5.47 The line-to-line output voltage waveform at steady-state for f_o=15 Hz and M_i=0.29 (scales: 200 V/div, 13.2 ms/div).

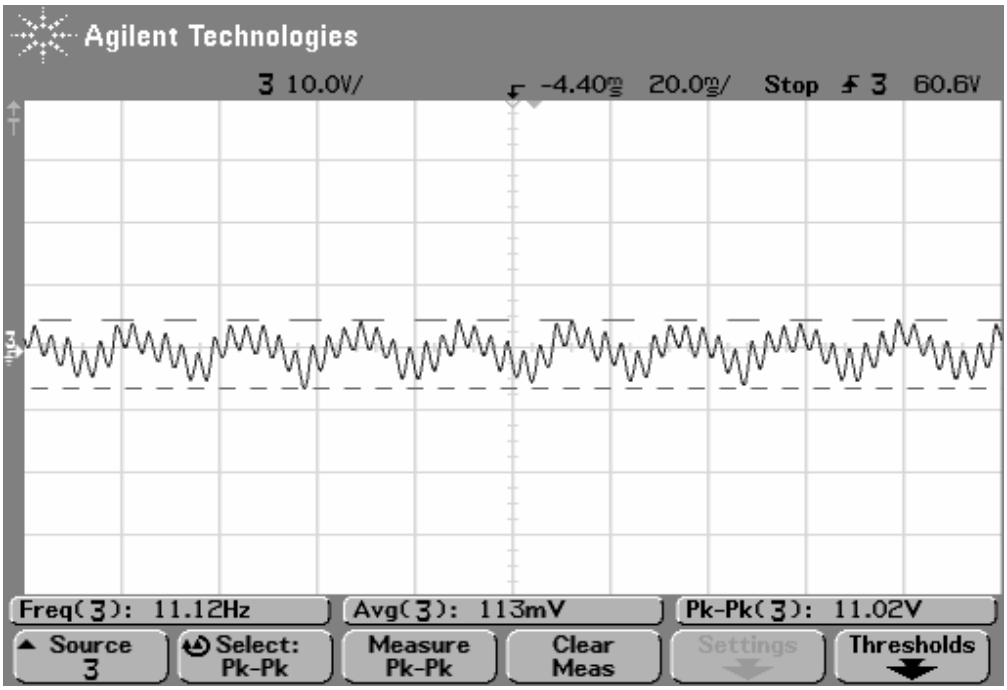


Figure 5.48 The DC bus voltage ripple at steady-state for f_o=15 Hz and M_i=0.29 (scales: 10 V/div, 20 ms/div).

In the second experiment of this section, the high modulation index and frequency operating condition is tested (M_i=0.87 and f_o=45 Hz). Acceleration transients and steady-state operating conditions are tested both. In the experiment both the start-up and steady-state waveforms are recorded. In Figure 5.49, the DC bus voltage, motor phase current, and the neutral point potential waveforms involving the loading transients and steady-state are shown. As seen from the figure, as the drive is accelerated from zero speed to the commanded speed, the motor phase current increases and the DC bus voltage has a temporary dip. As the motor accelerates and the current decreases, the DC bus voltage recovers. As seen from Figure 5.49, during acceleration, the neutral point potential starts to drift. The neutral point potential drift occurs only during acceleration. At steady-state, the neutral point potential drift is nearly zero. In this case, the neutral point potential drift is eliminated naturally by the three-level NPC inverter. At steady-state, the motor current and the neutral point potential waveforms are as shown in Figure 5.50. The motor current is nearly sinusoidal and the neutral point potential has a dominant triplen harmonic content with 2.9 V peak-to-peak value. The line-to-neutral output voltage waveform of the

inverter is shown in Figure 5.51. As seen from the figure, there is no distortion on the waveform, because the neutral point potential has no significant drift to create distortion. The line-to-line output voltage waveform of the inverter is as shown in Figure 5.52. The line-to-line output voltage waveform is distorted slightly.

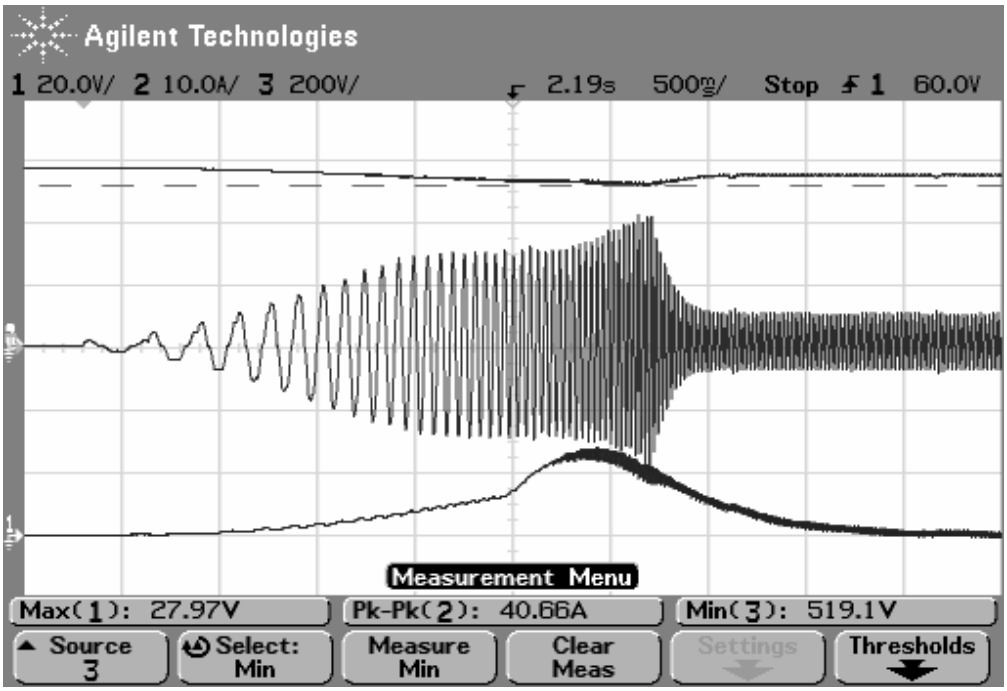


Figure 5.49 The DC bus voltage, the motor phase current, and the neutral point potential waveforms (from top to bottom) at f_o=45 Hz and M_i=0.87 (scales: 200 V/div, 10 A/div, 20 V/div, 500 ms/div).

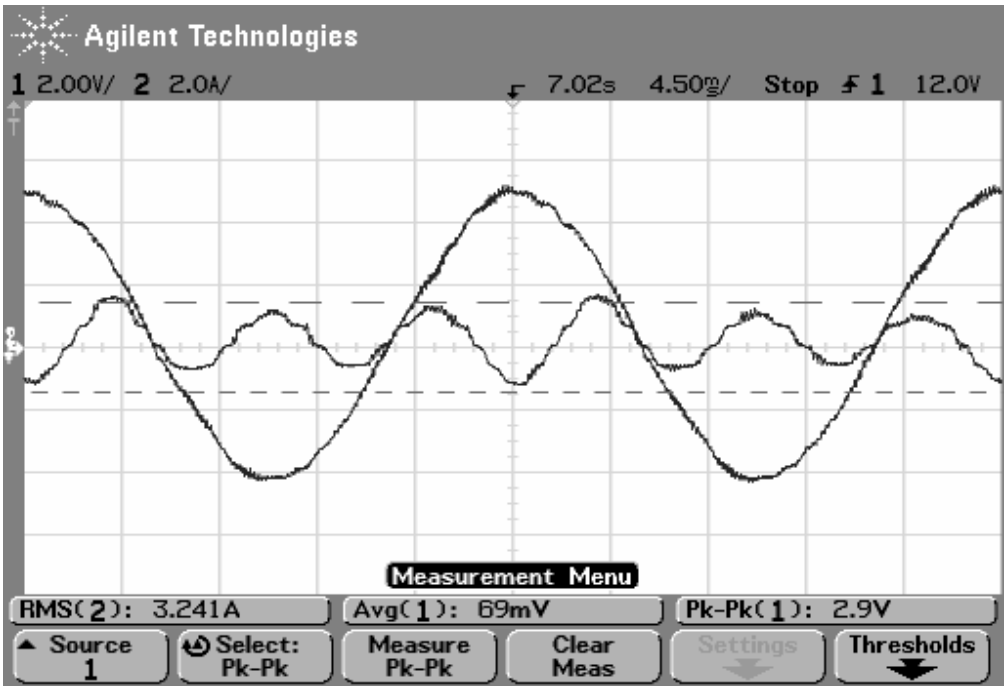


Figure 5.50 Motor phase current and the neutral point potential waveform at steady-state for f_o=45 Hz and M_i=0.87 (scales: 2 V/div, 2 A/div, 4.5 ms/div).

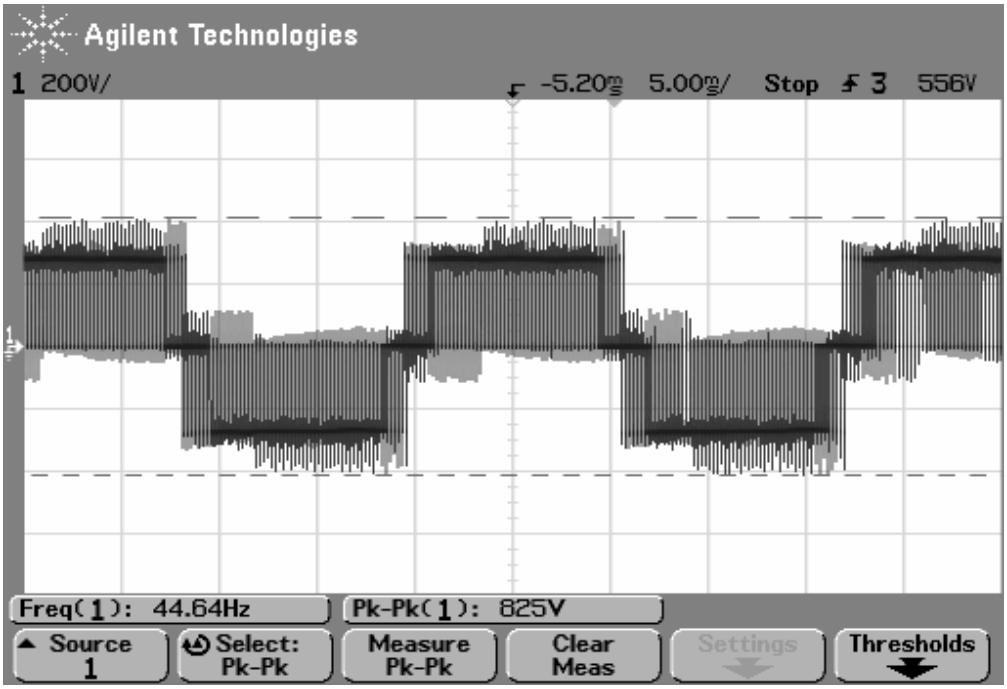


Figure 5.51 The line-to-neutral output voltage waveform at steady-state for f_o=45 Hz and M_i=0.87 (scales: 200 V/div, 5 ms/div).

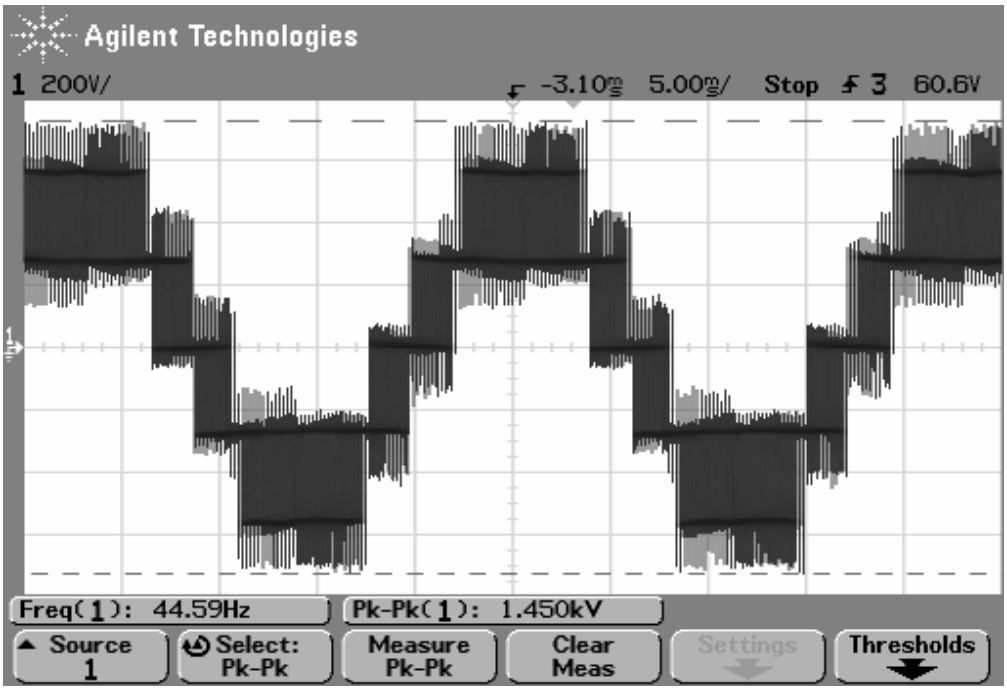


Figure 5.52 The line-to-line output voltage waveform at steady-state for f_o=45 Hz and M_i=0.87 (scales: 200 V/div, 5 ms/div).

5.3.2.2 NTV-PWM with The Uniform α Control Method

This section presents the experimental results of NTV-PWM with the uniform α control method for the induction motor drive. In this case, the redundancy function of the small voltage vectors is uniform ($\alpha=\alpha_1=\alpha_2$). The neutral point potential error elimination capability of the method is first tested for low M_i (M_i=0.29) and then for high M_i (M_i=0.87). In these experiments, the acceleration of the induction motor is done with the neutral point potential controller being disabled. Thus, at acceleration, the neutral point drifts and settles to a steady-state value (that obtained in section 5.3.2.1). Then, the controller is activated and the neutral point potential is decreased to zero by the controller (if possible). The time from the maximum neutral point potential drift to zero and the neutral point potential ripple are observed.

In Figure 5.53, the DC bus voltage, the motor phase current, and the neutral point potential waveforms are shown for f_o=15 Hz and M_i=0.29. As seen from the figure, the uniform α controller is enabled after the neutral point potential error reached to about 18 V. The uniform α controller decreases the neutral point potential error to

zero in about 50 ms. The 50 ms time to zero error is significantly short compared to the error settling time which is 11 seconds. Therefore, the uniform α controller acts rapidly and effectively on the error. The DC bus voltage is not effected by the uniform α controller, as shown in Figure 5.53. The motor phase current and the neutral point potential waveforms are shown in Figure 5.54. The motor current is not pure sinusoidal and the neutral point potential has no potential drift and no triplen harmonic content. The line-to-line output voltage waveform of the three-level NPC inverter is shown in Figure 5.55. The line-to-line output voltage waveform has noticeable distortion as seen from the figure. The line-to-line output voltage has frequent polarity reversals which would not occur when the neutral point potential controller was not enabled (see Figure 5.47). The distortion appears as narrow notches arising due to the inverter dead-time. The reason for the distortion is the same as the three-phase R-L load section.

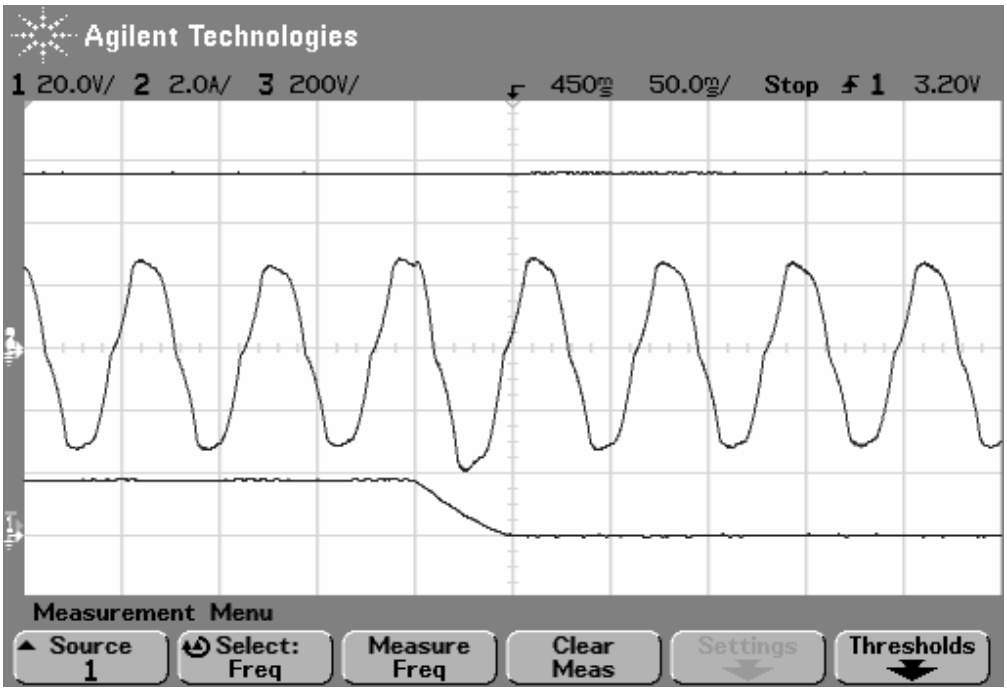


Figure 5.53 The DC bus voltage, the motor phase current, and the neutral point potential waveforms (from top to bottom) at f_o=15 Hz and M_i=0.29 (scales: 200 V/div, 2 A/div, 20 V/div, 50 ms/div).

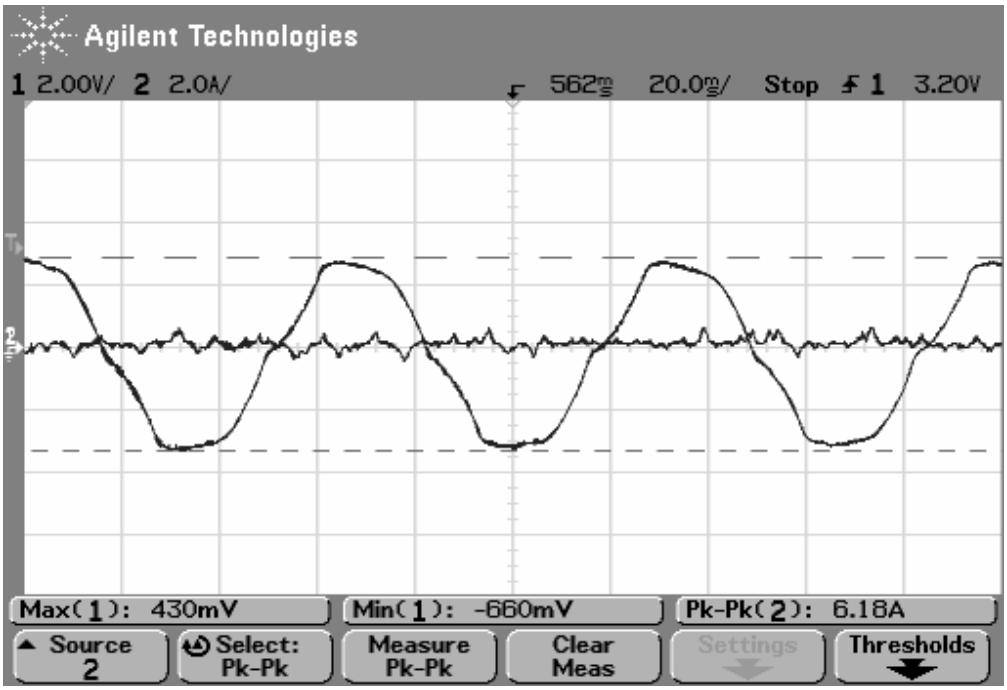


Figure 5.54 Motor phase current and the neutral point potential waveforms at steady-state for f_o=15 Hz and M_i=0.29 (scales: 2 V/div, 2 A/div, 20 ms/div).

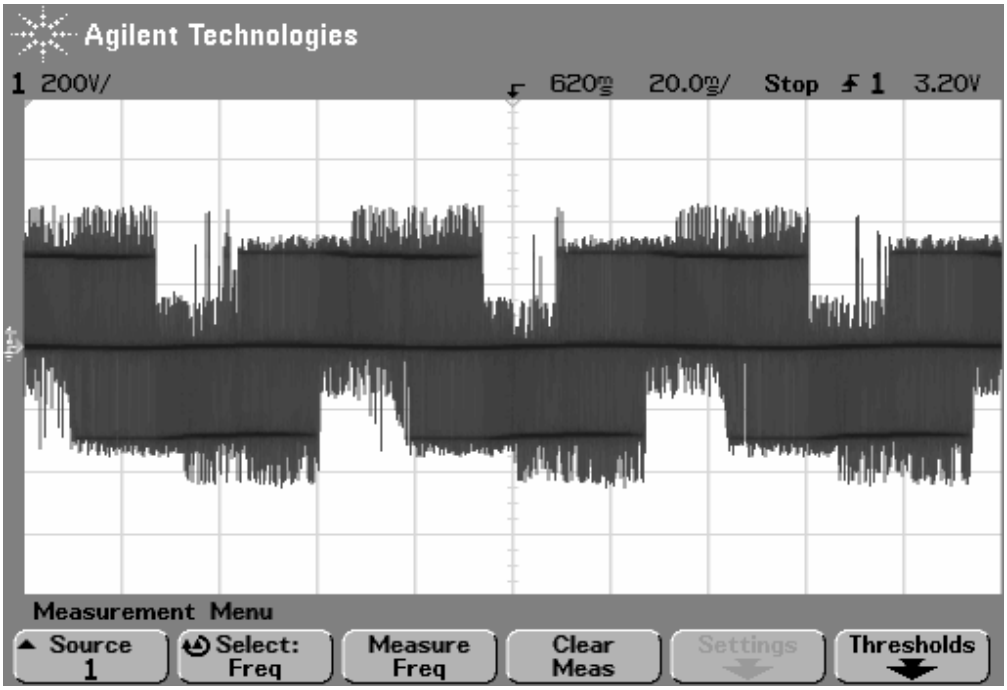


Figure 5.55 The line-to-line output voltage waveform at steady-state for f_o=15 Hz and M_i=0.29 (scales: 200 V/div, 20 ms/div).

In Figure 5.56, the DC bus voltage, the motor phase current, and the neutral point potential waveforms are shown for f_o=45 Hz and M_i=0.87. As seen from the figure, there is no drift on the neutral point potential. Therefore, the error elimination time can not be tested and illustrated in Figure 5.56. On the other hand, the triplen harmonic content is dominant on the neutral point potential as shown in Figure 5.57. The motor phase current contains some visible amount of ripple. The line-to-line output voltage waveform is shown in Figure 5.58. It has five different voltage levels and it is the same as the NTV-PWM without neutral point potential control case.

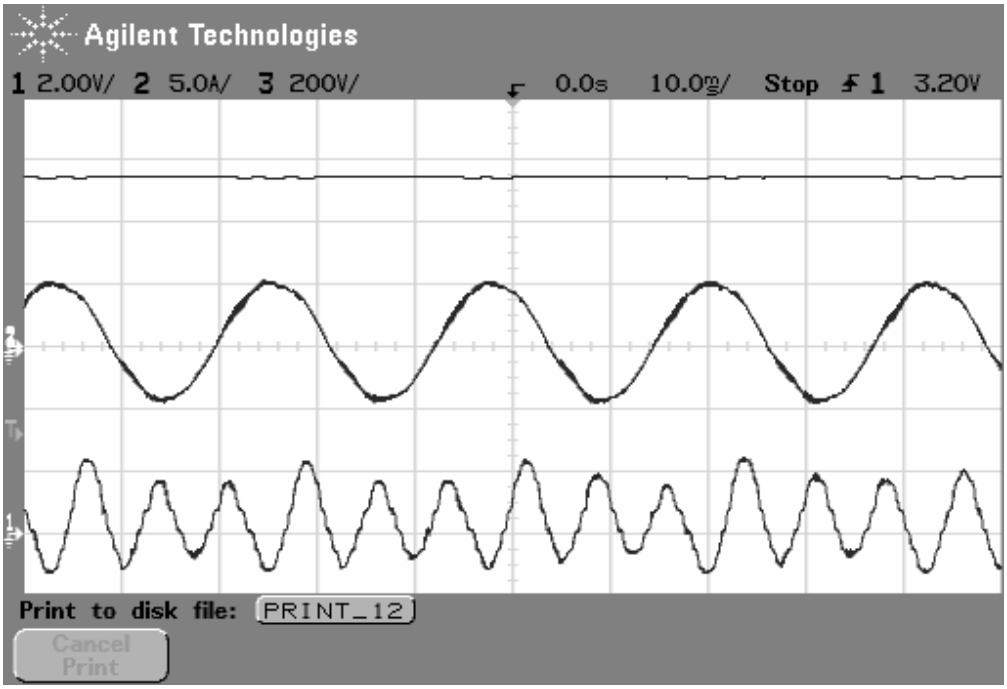


Figure 5.56 The DC bus voltage, the motor phase current, and the neutral point potential waveforms (from top to bottom) at f_o=45 Hz and M_i=0.87 (scales: 200 V/div, 5 A/div, 2 V/div, 10 ms/div).

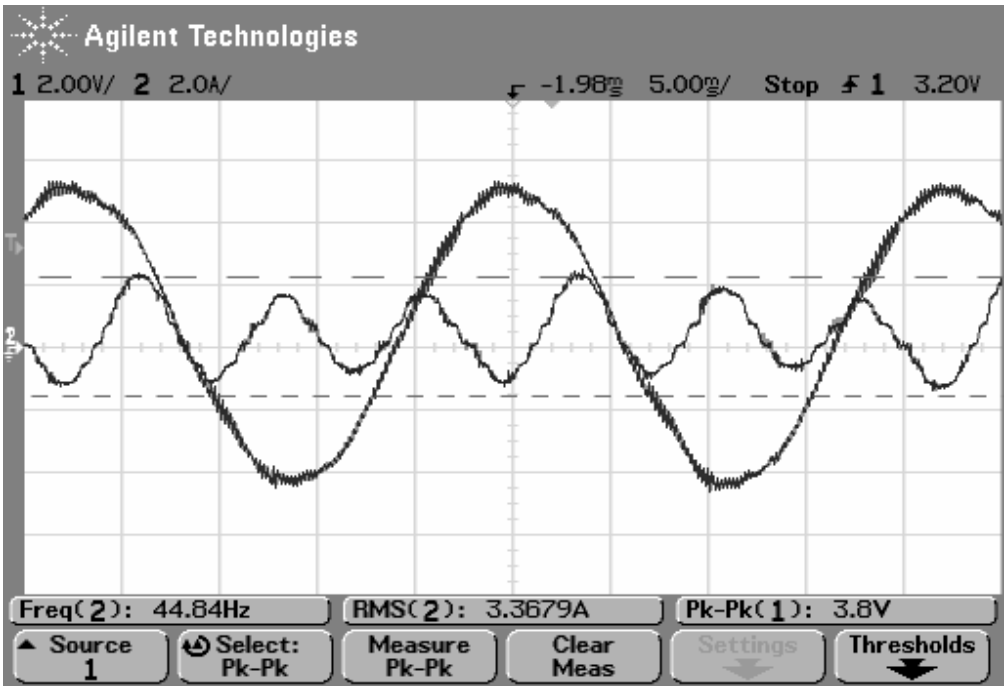


Figure 5.57 Motor phase current and the neutral point potential waveforms at steady-state for f_o=45 Hz and M_i=0.87 (scales: 2 V/div, 2 A/div, 20 ms/div).

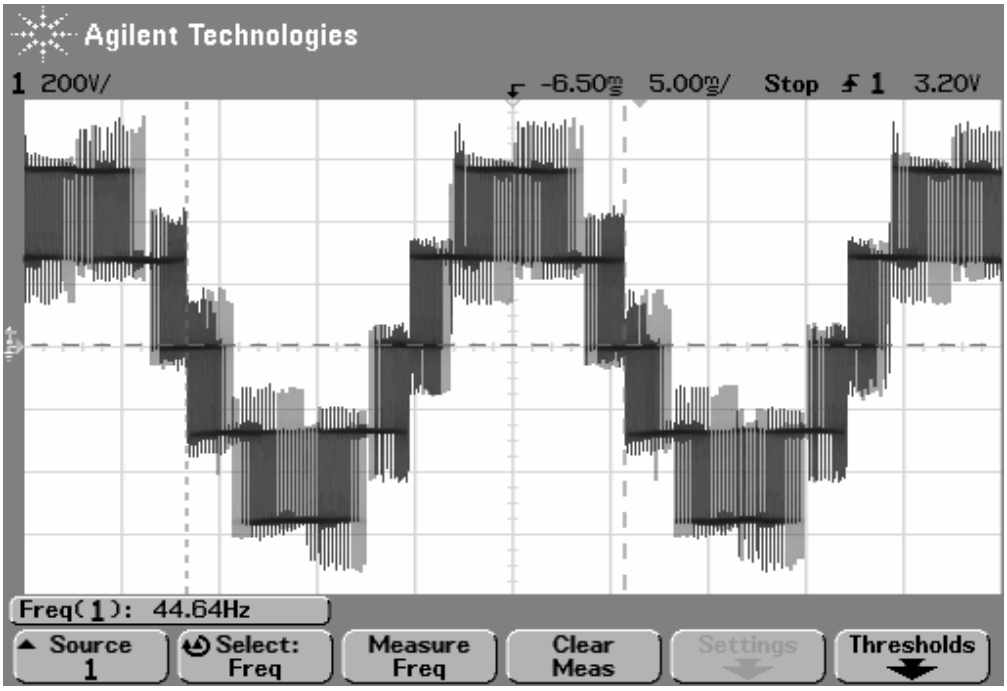


Figure 5.58 The line-to-line output voltage waveform at steady-state for f_o=45 Hz and M_i=0.87 (scales: 200 V/div, 20 ms/div).

5.3.2.3 NTV-PWM with The Optimal α Control Method

This section presents the induction motor drive test results of NTV-PWM with the optimal α control method. In this case, the redundancy functions of the small voltage vectors are coordinated in order to obtain maximum charge from the small voltage vectors. The neutral point potential error elimination capability of the method is first tested for M_i=0.3 and f_o=15 Hz and then for M_i=0.92 and f_o=45 Hz. In these experiments, the same procedure is followed as the uniform α control method section. The time from the maximum neutral point potential drift to zero is observed.

In Figure 5.59, the DC bus voltage, the motor phase current, and the neutral point potential waveforms are shown for f_o=15 Hz and M_i=0.29. As seen from the figure, the optimal α controller is enabled after the neutral point potential error reaches to about 18 V. The optimal α controller eliminates the neutral point potential error to zero in about 45 ms. Therefore, the optimal α controller decreases the error effectively. The DC bus voltage is not effected by the optimal α controller, as shown in Figure 5.59. The motor phase current and the neutral point potential waveforms are shown in Figure 5.60. The load current has distortion and the neutral point potential has no potential drift and no triplen harmonic content, which is the same as the uniform α control method. The line-to-line output voltage waveform of the three-level NPC inverter is shown in Figure 5.61. The line-to-line output voltage waveform has distortion as seen from the figure. The reason for the distorted output voltage waveform is the imbalanced dead-times of the gate driver modules.

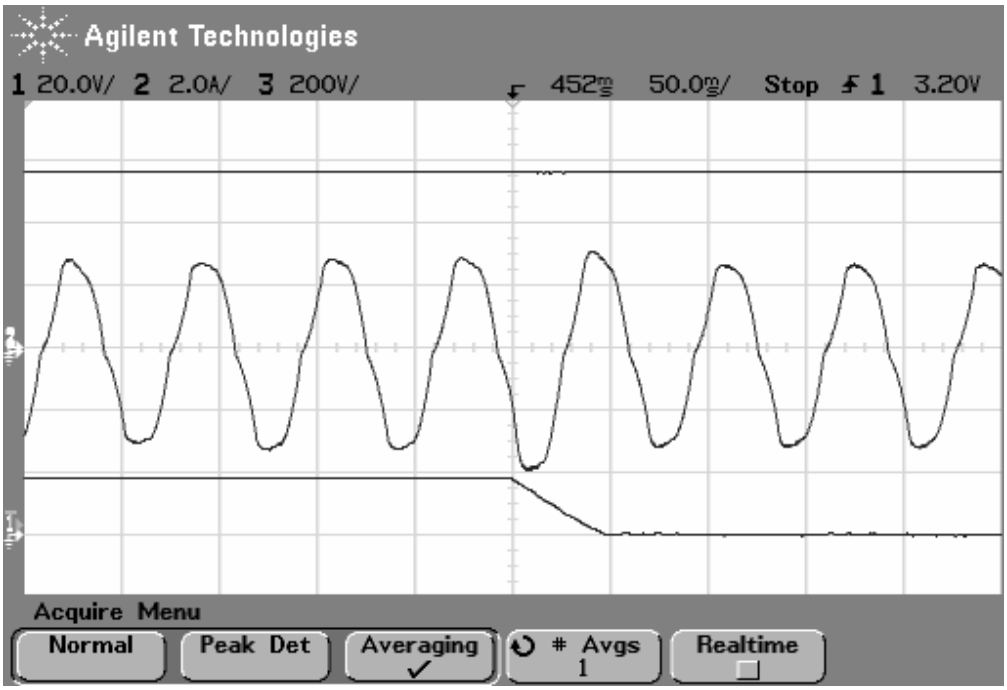


Figure 5.59 The DC bus voltage, the motor phase current, and the neutral point potential waveforms (from top to bottom) at f_o=15 Hz and M_i=0.29 (scales: 200 V/div, 2 A/div, 20 V/div, 50 ms/div).

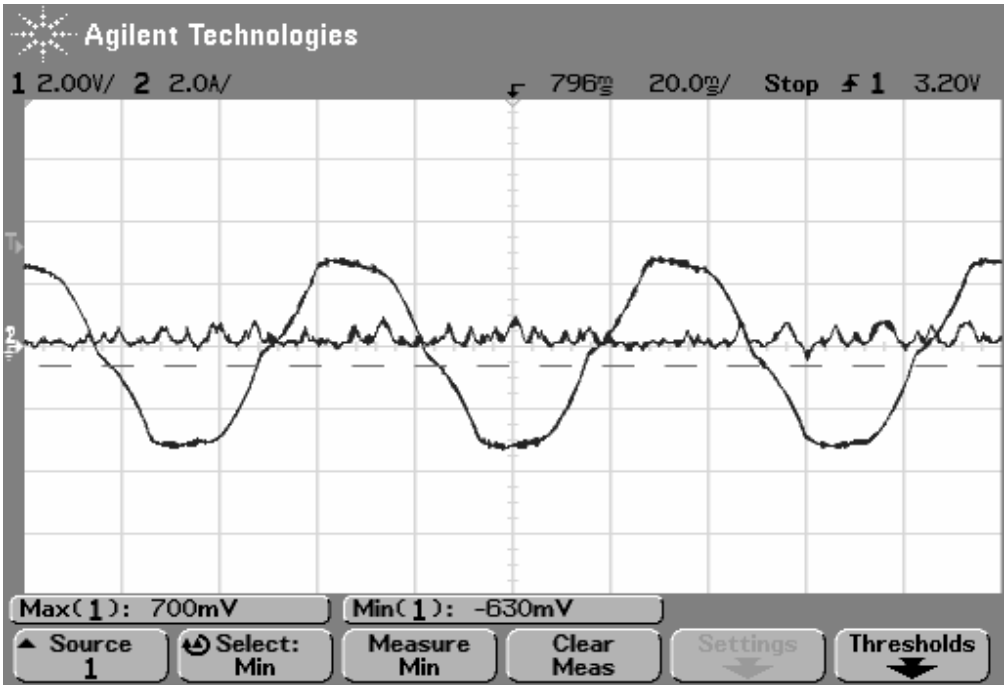


Figure 5.60 Motor phase current and the neutral point potential waveforms at steady-state for f_o=15 Hz and M_i=0.29 (scales: 2 V/div, 2 A/div, 20 ms/div).

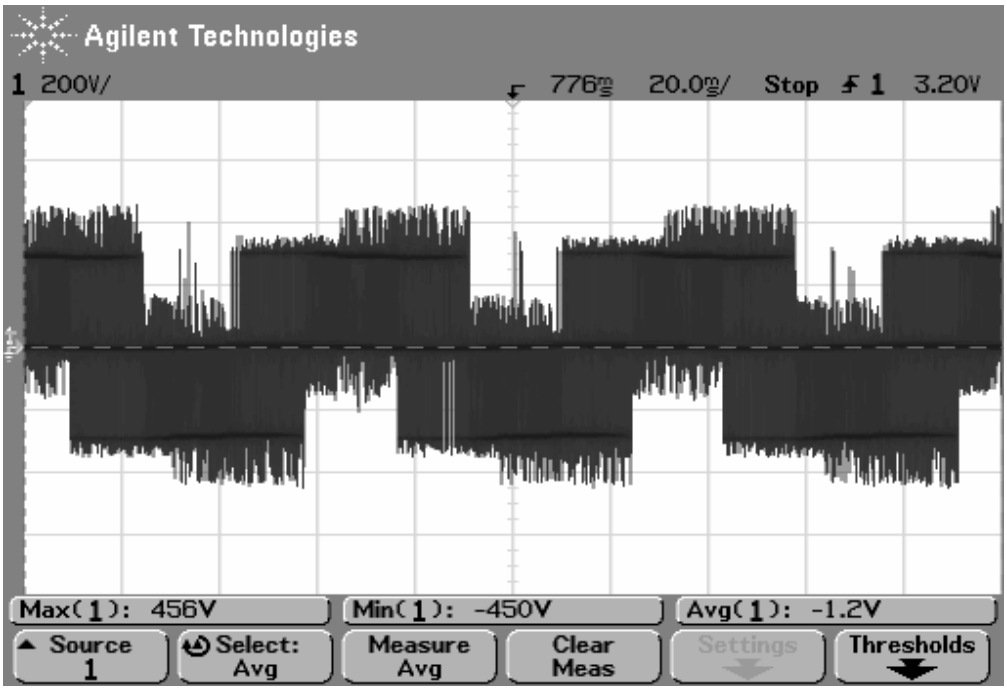


Figure 5.61 The line-to-line output voltage waveform at steady-state for f_o=15 Hz and M_i=0.29 (scales: 200 V/div, 20 ms/div).

In Figure 5.62, the DC bus voltage, the motor phase current, and the neutral point potential waveforms are shown for f_o=45 Hz and M_i=0.87. As seen from the figure, the average value of the neutral point potential error (the drift) is nearly zero, the ripple is still present. Therefore the error elimination time can not be tested and illustrated. The triplen harmonic content is dominant on the neutral point potential as shown in Figure 5.63. The motor phase current has noticeable ripple and the ripple frequency is equal to two times of the PWM frequency (zoom in view not shown in the figure). The line-to-line output voltage waveform is shown in Figure 5.64. The line-to-line output voltage waveform is the same as the uniform α control method. The waveform quality is slightly better than the NTV-PWM without neutral point potential control.

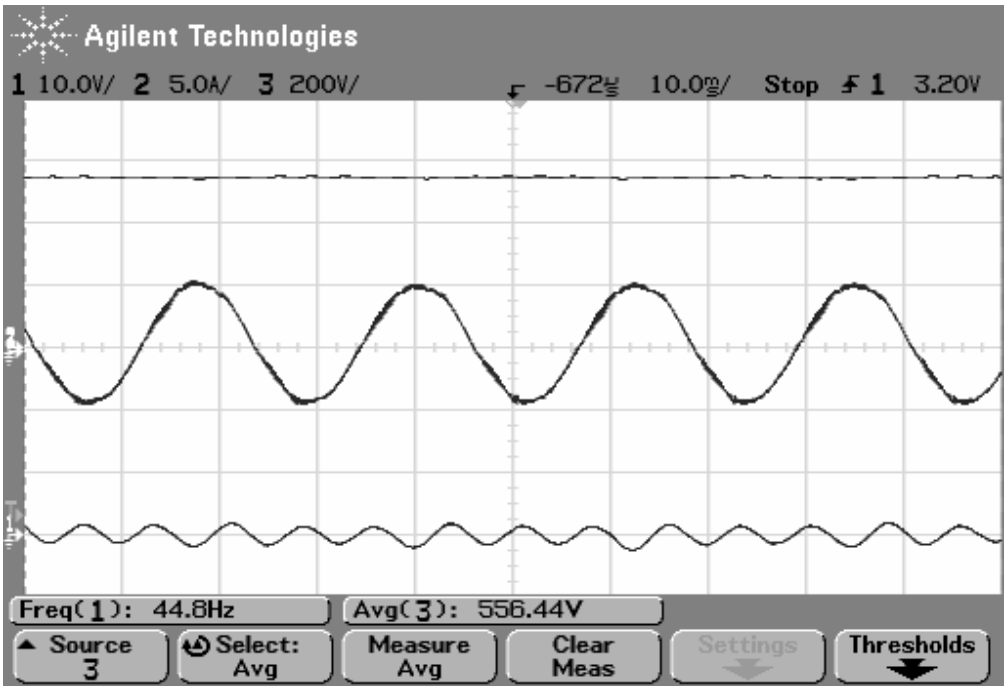


Figure 5.62 The DC bus voltage, motor phase current, and neutral point potential waveforms at M_i=0.87 (scales: 10V/div, 5A/div, 200V/div, 10ms/div).

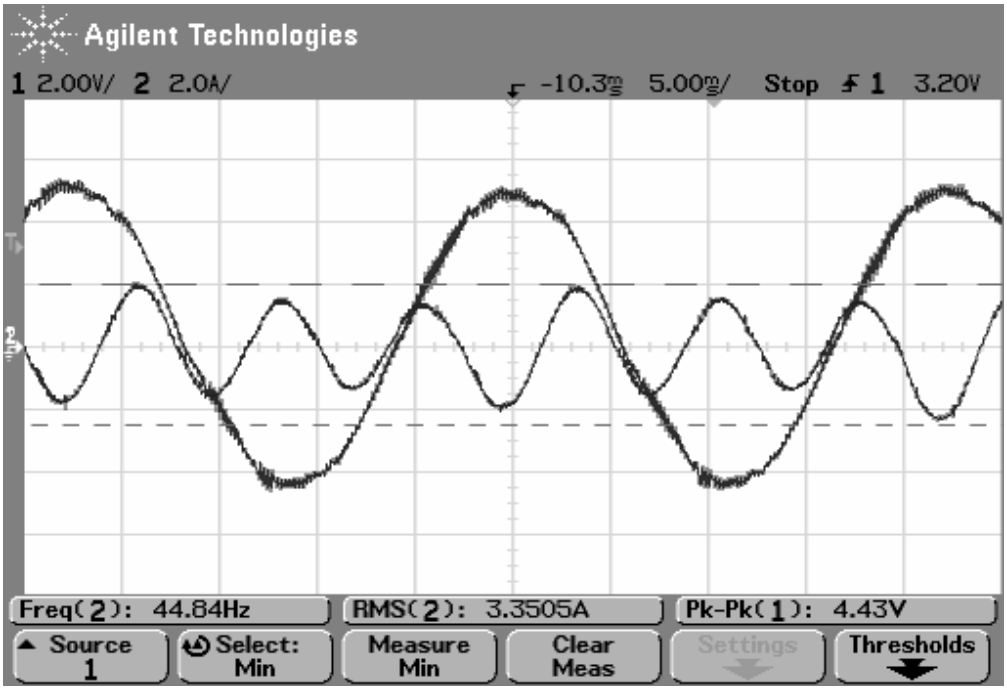


Figure 5.63 Motor phase current and the neutral point potential waveforms at steady-state for M_i=0.87 (scales: 2V/div, 2A/div, 5ms/div).

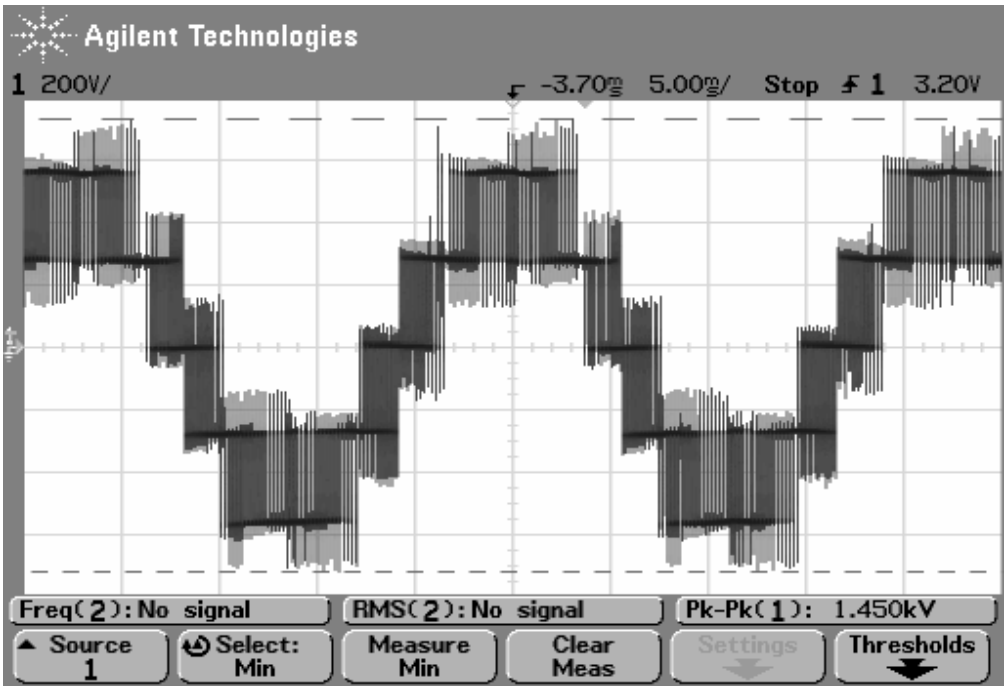


Figure 5.64 The line-to-line output voltage waveform at steady-state for M_i=0.87 (scales: 200V/div, 5ms/div).

5.3.2.4 Two-Parameter PWM with The Optimal α-γ Control Method

This section presents the experimental results of two-parameter PWM with the optimal α-γ control method for the induction motor drive. The low modulation index performance of two-parameter PWM with the optimal α-γ control method is exactly the same as the optimal α control method case because of identical controller structure. Therefore, the low modulation index performance is not shown. The neutral point potential error elimination capability of the method is tested only for high M_i (M_i=0.87). In this experiment, the same procedure is followed as the uniform α control method section. The neutral point potential ripple is observed.

In Figure 5.65, the DC bus voltage, the motor phase current, and the neutral point potential waveforms are shown for f_o=45 Hz and M_i=0.87. As seen from the figure, two-parameter PWM with the optimal α-γ control is enabled after the transient disappeared. The average value of the neutral point potential error (the drift) is eliminated and the triplen harmonic content is reduced significantly. The triplen harmonic content is not dominant on the neutral point potential as shown in Figure

5.66. The motor phase current has noticeable ripple. The motor phase current has more ripple than the uniform α and optimal α control method cases. The line-to-neutral output voltage waveform is illustrated in Figure 5.67 and the zoom-in view of the line-to-neutral output voltage waveform is shown in Figure 5.68. As seen from Figure 5.68, the line-to-neutral output voltage waveform has direct transitions from the positive DC bus to the negative DC bus. When γ is zero, these transitions occur. These direct transitions cause distortion on the output voltage waveforms of the three-level NPC inverter and increase the ripple of the motor phase current. The line-to-line output voltage waveform is as shown in Figure 5.69. The line-to-line output voltage waveform quality is poorer than the uniform α control method and the optimal α control method. The zoom-in view of the line-to-line output voltage waveform is illustrated in Figure 5.70. As seen from the figure, when γ is equal to zero, it has full DC bus voltage switchings. Therefore, for γ=0 the line-to-line output voltage waveform of the three-level NPC inverter is the same as the line-to-line output voltage waveform of the two-level inverter.

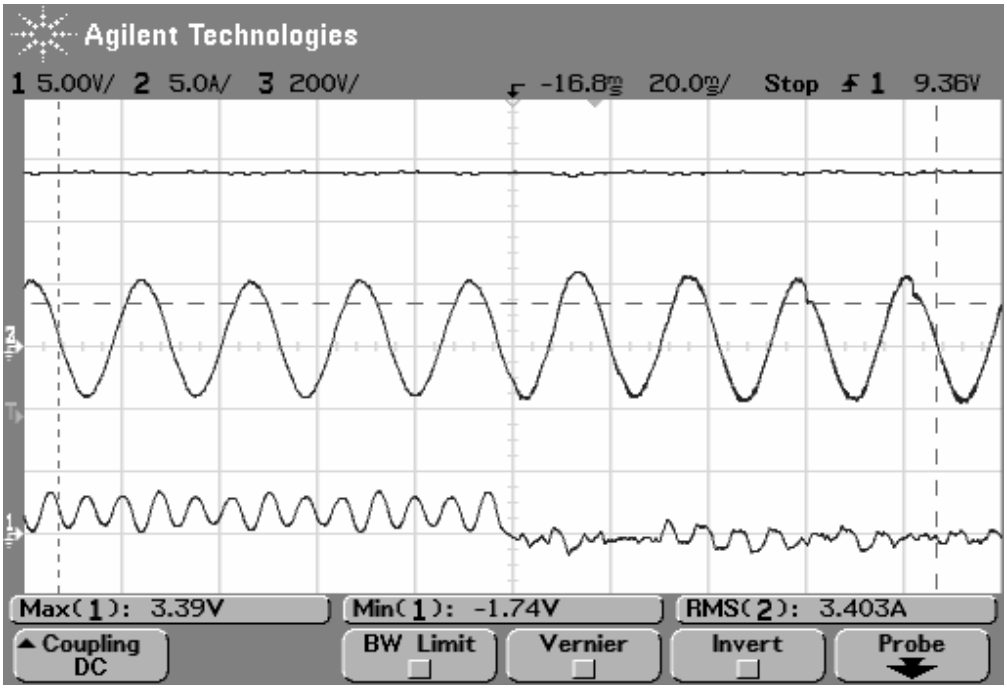


Figure 5.65 The DC bus voltage, the motor phase current, and neutral point potential waveforms at M_i=0.87 (scales: 5V/div, 5A/div, 200V/div, 20ms/div).

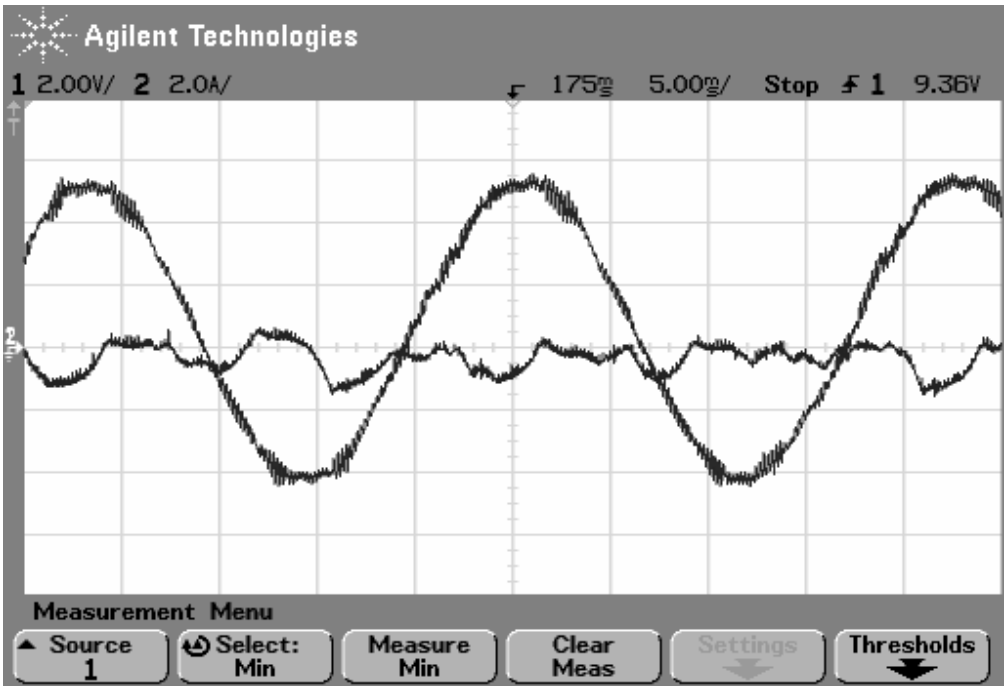


Figure 5.66 Motor phase current and the neutral point potential waveforms at steady-state for M_i=0.87 (scales: 2V/div, 2A/div, 5ms/div).

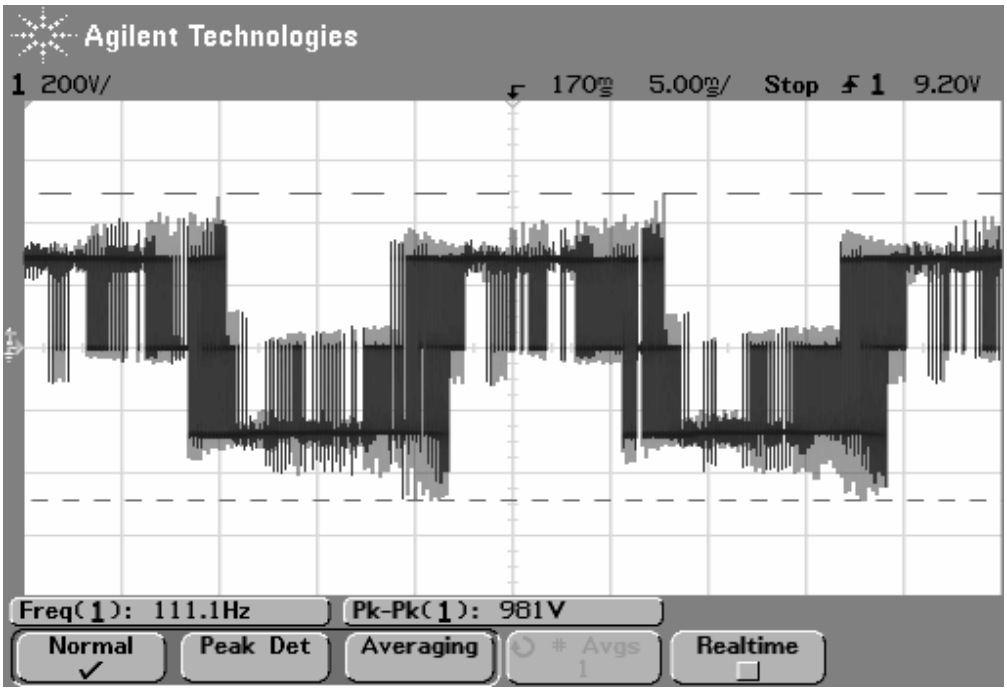


Figure 5.67 The line-to-neutral output voltage waveform at steady-state for M_i=0.87 (scales: 200V/div, 5ms/div).

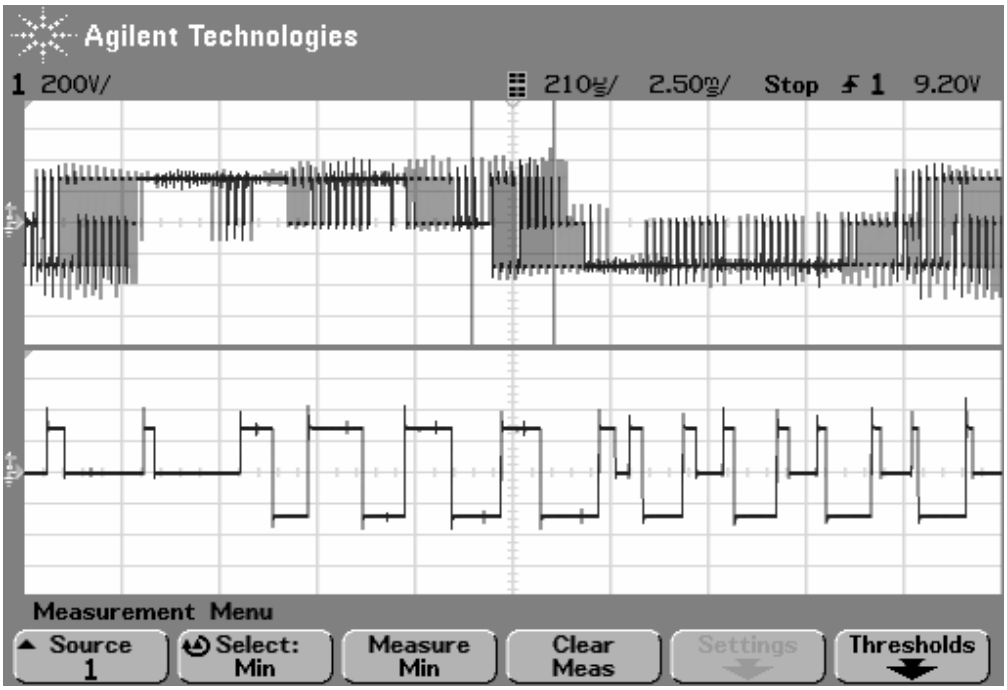


Figure 5.68 The line-to-neutral output voltage and the zoom-in line-to-neutral output voltage waveforms (from top to bottom) at steady-state for f_o=45 Hz and M_i=0.87 (scales: 200 V/div, 200 V/div, 2.5 ms/div, 210 µs/div).

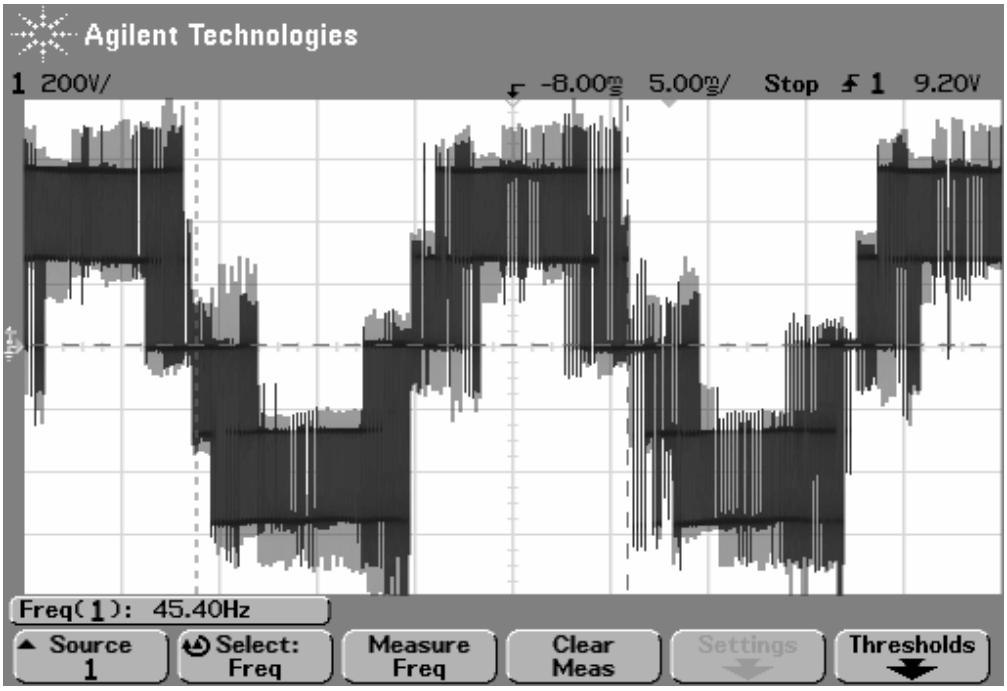


Figure 5.69 The line-to-line output voltage waveform at steady-state for M_i=0.87 (scales: 200V/div, 5ms/div).

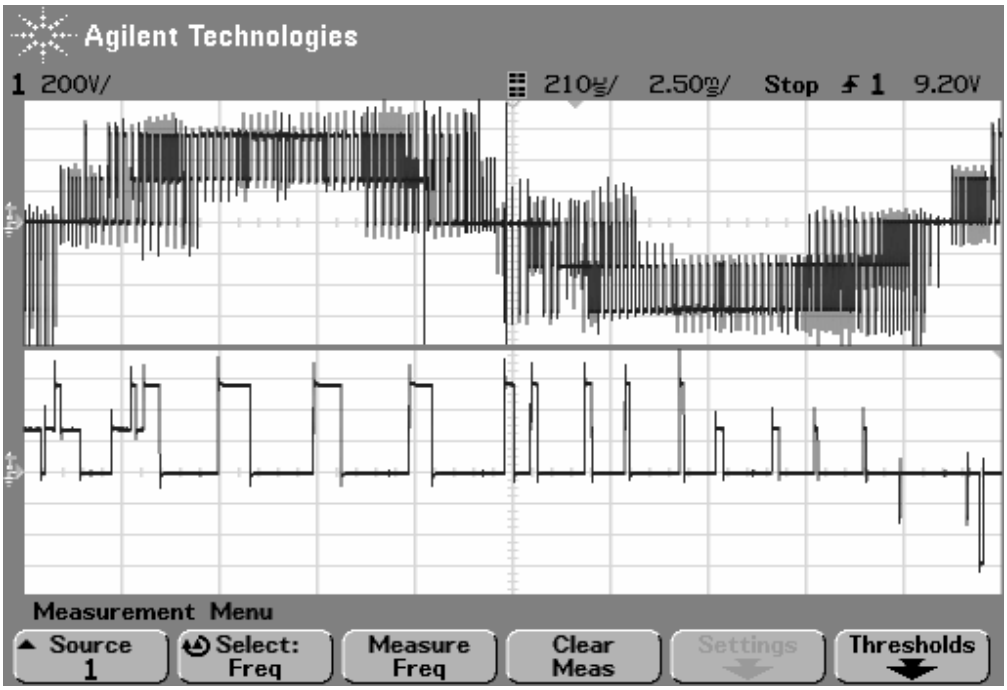


Figure 5.70 The line-to-line output voltage and the zoom-in line-to-line output voltage waveforms (from top to bottom) at steady-state for f_o=45 Hz and M_i=0.87 (scales: 200 V/div, 200 V/div, 2.5 ms/div, 210 µs/div).

5.3.2.5 Performance Comparison of The Control Methods For Induction Motor Drive

This section provides a comparison between the three neutral point potential control methods for an induction motor drive feeding a fan load.

First, the induction motor is driven at M_i=0.29 and f_o=15 Hz by employing constant V/f ratio method. For M_i=0.29 and NTV-PWM without neutral point potential control, the neutral point potential has drifted about 18 V. The uniform α control method eliminates 18 V neutral point potential error in about 50 ms. Therefore, the error elimination rate is 0.36 V/ms. The same neutral point potential error is eliminated in about 45 ms by the optimal α control method. The error elimination rate of the optimal α controller is 0.4 V/ms. The optimal α-γ control method has the same performance as the optimal α control method in the low modulation index

range. At steady-state, the neutral point potential has high frequency ripple with small magnitude.

Second, the induction motor is driven at Mi=0.87 and f_o=45 Hz. The neutral point potential drift could not be observed for M_i=0.87. Therefore, only the neutral point potential ripple is observed at steady-state for NTV-PWM without neutral point potential control and three control methods. The neutral point potential ripple peak-to-peak value is about 3 V and the ripple frequency is three times of the output voltage fundamental frequency ($3f_o$). For the uniform α and the optimal α control methods the neutral point potential ripple has 3.8 V peak-to-peak value with the frequency of $3f_o$. The optimal α-γ control method minimizes the neutral point potential ripple. The neutral point potential ripple peak-to-peak value is decreased to 1 V. As above results indicate, especially at high modulation index range the optimal α-γ control method has superior performance over the other control methods.

In summary, for both R-L and induction motor loads the neutral point potential drift and fluctuation problems could be illustrated experimentally and the results could be correlated to the computer simulations and analysis of the previous chapters. However, differences between the simulations and experimental results were noticed and these differences could be mainly attributed to the un-modeled behavior of the power semiconductor switches of the inverter.

The neutral point potential drift and fluctuation problems could be manipulated by the two parameter PWM method more effectively than the alternative methods. However, the inverter output voltage ripple and therefore the motor phase current ripple increases noticeably when employing the pulse pattern of this method. The waveform distortion of the motor phase current was more pronounced than the R-L load phase current due to the fact that the R-L load has large phase inductance while the motor leakage reactance is small and responds to the PWM voltage ripple of the inverter.

CHAPTER 6

CONCLUSIONS

In this thesis, the neutral point potential drift and fluctuation of the three-level NPC inverter was analyzed and a novel control algorithm was proposed to confine the neutral point potential variation to a very small band. A two-parameter PWM algorithm was proposed that provides superior neutral point potential control performance even with small DC bus capacitors.

In the first chapter of the thesis, a review of the two-level and three-level voltage source inverter topologies was provided. Advantages and disadvantages of the two voltage source inverter topologies were reviewed and compared. The neutral point potential drift and fluctuation problems of the three-level NPC inverter were briefly described.

In the second chapter, general background on the multilevel inverter topologies was provided. Topologies and modulation methods were reviewed. The advantages of the multilevel inverters were discussed. Several applications were illustrated. A detailed introduction to the three-level NPC inverter was provided and its neutral point potential performance issues were discussed.

The third chapter of the thesis was dedicated to a thorough analysis of the neutral point potential behavior of the three-level NPC inverter. First the standard PWM methods were reviewed in detail with emphasis on space vector PWM. Then the relation between the PWM pulse pattern and the neutral point current was analytically formulated. Employing the per-PWM-cycle average model approach, the neutral point current was formulated as a function of the modulation method redundancy functions and inverter output currents. Based on the neutral point current

formula, the neutral point potential behavior could be analytically formulated and its behavior investigated.

With the neutral point potential being formulated as a function of the modulation method parameter (the redundancy function, α), the pulse pattern modification based neutral point potential control methods were considered and the two known methods were taken into consideration. The performance limitations of these two methods were illustrated and the two-parameter PWM method which overcomes the deficiencies of these methods was introduced.

The two-parameter PWM method is a PWM method that involves only two control parameters (α and γ) that shape the pulse pattern and provide complete controllability of the neutral point potential throughout the voltage vector space of the inverter. Thus, it is possible to continuously and smoothly vary the control parameters and obtain a pulse pattern such that both high waveform quality output voltage and zero neutral point potential values could be obtained at the same time. Controlling both attributes in one such algorithm unifies the structure of the modulator and neutral point potential controller in one and yields a compact hardware/software structure for the inverter.

The performance of the proposed two-parameter PWM method is superior to its alternatives. Specifically, the method provides a very flexible control capability over the medium voltage vector while operating at high modulation indices. The neutral point potential error can be reduced or totally eliminated based on the selected range of the γ parameter. Thus, the method allows limitation or complete elimination of the neutral point potential drift or fluctuation by means of pulse pattern modification and even with very small DC bus capacitors. The performance superiority of the two-parameter PWM method with optimal α-γ parameters over the other two methods was demonstrated by means of average model simulations and a thorough comparison was provided at the end of chapter 3.

The fourth chapter of the thesis involved detailed computer simulations that evaluate the performance of the various neutral point potential control methods. The analytical results obtained in the third chapter were verified by means of detailed computer simulations of a three-phase current sink type load, a three-phase R-L load, and an induction motor drive system feeding a fan load. The study illustrated that the detailed computer simulation results were in strong agreement with the analytical results and with the average model computer simulation results provided in chapter 3. The detailed computer simulation results illustrated the neutral point potential performance superiority of the two-parameter PWM method with optimal α-γ control compared to the other neutral point potential control methods. It was shown that specifically at high modulation index values, the neutral point potential control performance of the optimal α-γ control method is superior during both dynamic and steady-state operating conditions. At steady-state the optimal α-γ control method gives practically zero neutral point potential value, while the other methods have noticeable voltage ripple magnitude.

In the fifth chapter, experimental results of the laboratory prototype three-level NPC inverter drive were reported. A 5 kVA prototype three-level NPC inverter was built and tested at the university laboratory to verify the results of the analysis and the detailed computer simulations. The digital control platform of the three-level NPC inverter was established by the combination of a DSP and an DSP. Both a three-phase R-L load and a three-phase induction motor feeding a fan load were tested.

In the experimental study, the steady-state and dynamic performance of the neutral point potential control methods were investigated. Experimental results were obtained for various operating conditions. The experimental results obtained have supported the analytical results of chapter 3 and the computer simulation results of chapter 4. The experiments mostly illustrated the superior performance of the two-parameter PWM method. However, in the experimental set-up, the line-to-line output voltage waveform was more distorted than what was obtained in the computer simulations and as a result, the output current waveform was also noticeably distorted. However, the neutral point potential control capability of the proposed

method was proven and its superiority to other methods was clearly demonstrated. Based on the theoretical and experimental results, Table 6.1 summarizes the properties of the considered neutral point potential control methods.

The theoretical and experimental studies conducted in this thesis have proven that the proposed two-parameter PWM method solves the neutral point potential fluctuation and drift problem effectively. It only involves PWM pulse pattern modification and requires no additional hardware. Moreover, with the control over the neutral point potential being established, the DC bus capacitors of the inverter drive could be reduced and as a result the total inverter cost and size could be considerably reduced. It has been shown that the only two disadvantages of the two-parameter PWM with optimal α-γ control method are the partially distorted output voltage waveform and increased dv/dt rating. However, the dv/dt rating could be restored with a switching state-machine and the dv/dt problem could be eliminated. The waveform quality degradation is an issue involving the load type and may not be considered as a major drawback for high inductance load applications.

Table 6.1 Performance and waveform quality comparison of the neutral point potential control methods

Method	Transient Response		Steady-state Response		Inverter Output Voltage and Current Waveform Quality (Steady-state)		Additional Information
	$M_i < 0.5$	$M_i > 0.5$	$M_i < 0.5$	$M_i > 0.5$	$M_i < 0.5$	$M_i > 0.5$	
Uniform α	Average	Poor	Average	Poor	Good*	Good	* Problems occur due to dead-time Easy to implement
Optimal α	Optimal	Poor	Optimal	Poor	Good^{x}	Good	x Problems occur due to dead-time Easy to implement
Optimal α – γ	Optimal	Optimal	Optimal	Optimal	Good†	Poor**	† Problems occur due to dead-time ** Complex pulse pattern

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