FULLY DIGITAL PARALLEL OPERATED SWITCH-MODE POWER SUPPLY MODULES FOR TELECOMMUNICATIONS

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ABSTRACT

FULLY DIGITAL PARALLEL OPERATED SWITCH-MODE POWER SUPPLY MODULES FOR TELECOMMUNICATIONS

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Digitally-controlled, high power universal telecommunication power supply modules have been developed. In this work, the converter control strategy, and its design and implementation first, by means of parallel-operated, dual, 8-bit microcontrollers, and then by using a high processing power digital signal processor (DSP) have been emphasized. The proposed dual-processor based digital controller provides an extended operating output voltage range of the power supplies, user programmable current limit setting, serial communication based active load current sharing with automatic master-slave selection among parallel-operated modules, user selectable number of back-up battery cells, programmable temperature compensation curves, and automatic derating without extra hardware requirement. Overload and output short-circuit protection features are also controlled by software.

One of the processors in the digital controller is employed for user interface purposes such as long term records, display, and alarm facilities, and remote control, which are inherently slow processes. The fast processing speed required by output voltage setting, current limit, and load current sharing however is to be fulfilled by a second processor dedicated to the adjustment of output voltages of modules. Tight dynamic load regulation requirement of a telecommunication power supply has been fulfilled by a 150 MIPS DSP, in place of a low cost, 8-bit microcontroller.

The implemented digitally-controlled, 1.8 kW, 0-70V telecommunication power supplies have been tested successfully in several locations in the field.

Keywords: Switch mode power supplies, digital control, dc-dc power converters

ÖZ

HABERLEŞME UYGULAMALARI İÇİN TAMAMEN SAYISAL PARALEL ÇALIŞAN ANAHTARLAMALI GÜÇ KAYNAĞI MODÜLLERİ

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Sayısal kontrollü, yüksek güçlü evrensel telekomünikasyon güç kaynakları geliştirilmiştir. Bu çalışmada çevirgeç kontrol stratejisinin önce paralel çalışan, çift, 8-bit mikrodenetleyiciler ve daha sonra yüksek işlem güçlü sayısal sinyal işleyici (DSP) kullanılarak tasarım ve geliştirimi vurgulanmıştır. Önerilen çift işlemci tabanlı sayısal kontrol ünitesi geniş çıkış çalışma gerilim aralığı, kullanıcı tarafından ayarlanabilen akım sınırı, paralel çalışan modüller arasından otomatik efendi-köle seçim özellikli seri haberleşmeye dayalı aktif yük paylaşımı, kullanıcı tarafından ayarlanabilen akü hücre sayısı, programlanabilen sıcaklık kompanzasyon eğrileri ve otomatik güç sınırlaması özelliklerini ek bir donanım ihtiyacı olmadan sağlamaktadır. Ayrıca, aşırı yüklenme ve çıkış kısa devrelerine karşı koruma da sayısal olarak kontrol edilmektedir.

Sayısal kontrol ünitesinde kullanılan mikrodenetleyicilerden birisi kullanıcı arayüzü, uzun süreli kayıtlar, alarm ve uzaktan kontrol gibi doğası gereği yavaş işlevleri yerine getirmek için kullanılmaktadır. Çıkış gerilimi ayarlama, akım sınırlama ve aktif yük paylaşımı gibi hızlı kontrol gerektiren işlevler modüllerin çıkış gerilimini ayarlamaya ayrılmış ikinci bir işlemci tarafından karşılanmaktadır. Telekomünikasyon güç kaynaklarının sıkı dinamik yük regülasyon ihtiyacı ucuz 8-bit mikrodenetleyicinin yerine 150 MIPS bir DSP kullanılarak karşılanmıştır.

Gerçekleştirilen sayısal kontrollü, 1.8kW, 0-70V telekomünikasyon güç kaynakları sahada birçok yerde başarı ile test edilmiştir.

Anahtar kelimeler: Anahtarlamalı güç kaynakları, sayısal kontrol, da-da güç çevirgeçleri

To My Wife and Daughter

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TABLE OF CONTENTS

PLAGIARISM…… iii

ABSTRACT……... iv

ÖZ…….. vi

DEDICATION…….. viii

ACKNOWLEDGMENTS…… ix

TABLE OF CONTENTS……. x

LIST OF FIGURES……. xiii

CHAPTER

1. INTRODUCTION……... 1

1.1. General…….. 1

1.2. Development of Switch-Mode Techniques…….. 2

1.2.1. Linear Regulator versus Switch Mode Technology... 2

1.2.2. Review on Switch-Mode Power Supply Topologies.. 6

1.2.3. Control Techniques…… 8

1.2.3.1.Voltage Mode Control……. 9

1.2.3.2.Peak Current Mode Control…… 10

1.2.3.3.Average Current Mode Control…….. 12

1.3. Telecommunication Power Supplies……... 13

1.3.1. Recent Trends in Telecommunication Power Supplies……. 13

1.3.2. Application of Switch-Mode Techniques to Telecommunication Power Supplies…… 17

1.4. Digital Control of SMPS…… 21

1.5. Scope of the Thesis…… 27

2. SYSTEM DESCRIPTION……... 31

2.1. AC/DC Preregulator Stage…… 37
2.2. DC/DC Converter Stage…….. 38
2.2.1. Phase-Shifted Zero Voltage Switching……. 39
2.2.2. System Controller……. 43
3. PHASE I: DESIGN AND IMPLEMENTATION WITH DUAL MICROCONTROLLERS……... 46
3.1. System Description…….. 47
3.2. Digital Controller Design…… 50
3.2.1. Current Sharing Loop……... 53
3.2.2. Current Limit Loop…….. 55
3.2.3. Derating Loop…….. 56
3.2.4. Voltage Regulation Loop……. 58
3.3. Controller Implementation……. 58
3.4. Remote Control…….. 63
3.5. Results…… 66
3.6. Operation in the Field…… 76
4. PHASE II: DESIGN AND IMPLEMENTATION OF DSP CONTROLLED ZVS PHASE-SHIFTED FULL-BRIDGE CONVERTER……... 77
4.1. Theory…… 79
4.1.1. Phase Shifted Zero Voltage Transition (ZVT) Power Converter……. 79
4.1.2. Two-Pole-Two-Zero Compensation……... 80
4.1.3. The Z-Transform……. 82
4.1.3.1.Dealing with Poles and Zeros in Z-domain…... 83
4.1.3.2.Determining the Corresponding Poles and Zeros of s-domain in z-domain……... 84
4.2. Modelling and Simulation…….. 87
4.2.1. Output Stage…… 88
4.2.2. Verification of the model…… 91

4.2.3. Design of the Control Stage…… 92
4.2.4. Simulation of the Overall System……. 94
4.3. Design and Implementation……. 97
4.3.1. Hardware……... 97
4.3.1.1.PWM Generation…… 97
4.3.1.2.MOSFET Drivers…… 101
4.3.1.3.Analog Interface…….. 102
4.3.2. Software……... 104
4.3.2.1.General..... 104
4.3.2.2.Coefficient Calculations..... 106
4.3.2.3.Software Implementation..... 109
4.4. Results…….. 111
5. CONCLUSIONS…… 116
REFERENCES……. 119
APPENDICES
A. THE FAMILY OF SWITCHING REGULATORS……... 130
B. PHASE SHIFTED ZERO VOLTAGE TRANSITION……. 135
C. APPLICATIONS OF THE IMPLEMENTED SYSTEM IN THE FIELD…….. 150
D. NEC uPD78F0058 DATASHEET……..... 152
E. TEXAS INSTRUMENTS TMS320F2812 DATASHEET…... 162
CURRICULUM VITAE……... 169

LIST OF FIGURES

FIGURES

1.1.Practical Linear Series Regulator Circuit…… 4
1.2.Practical Circuit of a Switch-Mode Regulator…… 4
1.3.Voltage Mode Control…… 9
1.4.Peak Current Mode Control……... 10
1.5.Average Current Mode Control……. 13
1.6.A Typical Telecom Power System…… 14
1.7.Ferro-Resonant Power Supply…….. 18
1.8.Double Switch Forward Converter…….. 19
1.9.Zero Voltage Switching with Additional Capacitors (ZVSWAC) Type DC/DC Converter……... 20
2.1.Block Diagram of the System…….. 35
2.2.Circuit Diagram of the System…… 36
2.3.Full Bridge Topology…….. 39
2.4.Conventional Full Bridge PWM Waveforms……. 40
2.5.Phase Shifted PWM Control Waveforms…….. 41
2.6.The Circuit Schematic for Phase Shift Operation…….. 42
2.7.Block Diagram of the System Controller……... 44
3.1.General Hardware Block Diagram of the Dual-processor Based Digital Control System…… 47
3.2.Hardware Block Diagram of Each Digitally Controlled Module……. 48
3.3.System of Parallel-connected Modules with Digitally-controlled Load Current Sharing…… 49
3.4.Block Diagram of the Digital Controller…….. 51

3.5.Controller Block Diagram for Current Sharing Loop…….. 53
3.6.Block Diagram of Current Limit Loop……..…. 56
3.7.Block Diagram of Derating Loop…….. 57
3.8.Derating Curve Against Input Voltage…….. 57
3.9.Voltage Regulation Loop……... 58
3.10.Flowchart of the Digital Controller……. 61
3.11.The Implemented Control Stage PCB……. 62
3.12.Systems with Remote Control Unit……. 64
3.13.Screenshots from Central Office Software…….. 66
3.14.The Implemented Power Supply Module…… 67
3.15.Inside View of the Implemented System……. 67
3.16.Six Digitally-controlled, Universal Telecommunication Power Supplies in Parallel……... 68
3.17.Digitally Controlled Load Current Sharing Between Parallel Operated Modules…….. 70
3.18.Output Voltage and Output Current of Modules Under Overload……... 71
3.19.Output Short-circuit Current……... 73
3.20.Derating Versus Input Voltage……..... 74
3.21.International PCIM/HFPC Conference and Exhibition Booth, and the “1999 Technology Achievement Award”… 75
3.22.Systems in the Field…… 77
4.1.Hardware Block Diagram of the DSP Based Control System of the ZVS phase-shifted full-bridge converter…… 79
4.2.The Bode Plots for Two-Pole Two-Zero Compensation….. 81
4.3.Relationship Between s-plane and z-plane……... 83
4.4.Second Order System…… 84
4.5.A zero/pole in s-domain…… 85
4.6.Corresponding zero/pole in z-domain…….. 85
4.7.Zero/pole on the Real Axis…….. 87

4.8.Output Stage of the Rectifier…… 88
4.9.The z-domain Poles of the Output Stage……... 90
4.10.The Model of the Output Stage of SMPS in MATLAB….. 91
4.11.Simulation Results of the Output Stage……... 92
4.12.The Pole and Zero Locations pf the Control Stage…….. 94
4.13.Bode Plots of the Converter……. 95
4.14.MATLAB Simulation Results……. 97
4.15.Experimental Setup of the Implemented DSP Controlled ZVS Phase-shifted Full-bridge…… 98
4.16.PWM Control Signals Generated……..... 100
4.17.MOSFET Driver Circuit Diagram…….. 102
4.18.Block Diagram of a DSP System…… 103
4.19.Timing Sequence of the Digital Controller Tasks…….. 110
4.20.The I/O Relationship Between Tasks of Digital Controller…… 110
4.21.Flowchart of the Controller…… 111
4.22.Full-bridge Inverter Output Voltage at Different Duty Cycles…… 112
4.23.Measured Output Voltage Step Response……. 113
4.24.Measured Dynamic Response,$V_{o(ac)}$, for a Transient Variation of I_o Between 5A and 25A……. 114
A.1.The Single Switch Non-Isolated Switching Regulator Family…… 131
A.2.The Single Transistor Isolated Topology Family……... 133
A.3.The Multiple Switch Topology Family……. 134
B.1.The Circuit Schematic for Phase Shift Operation……. 135
B.2.Initial Condition…… 136
B.3.Right Leg Transition……. 137
B.4.Clamped Freewheeling Interval…… 138
B.5.Left Leg Transition…… 139

B.6.Power Transfer Interval…… 141
B.7.V_{DS} and V_{GS} Voltage Waveforms for High Side Switch…. 148
B.8.V_{DS} and V_{GS} Voltage Waveforms for Low Side Switch…. 149

CHAPTER I

INTRODUCTION

1.1.GENERAL

Increasing demand for high power converters in telecommunication, and computer power supplies drives the need for higher flexibility in control, increased level of system integration, and more reliability, besides achieving high levels of performance. The trend in power supply design is towards the implementation of digital control systems providing several benefits over traditional analog control methods. The digitally controlled power converter has the advantages of high reliability, high controllability, and high flexibility. Noise immunity, resistance to environmental effects, the possibility of changing the control scheme without modifying the hardware, and implementing intelligent control algorithms, are the attractive features of digital controllers. Recent developments in the digital signal processors and the demand for the digital controller features give impetus to the implementation of digital controllers in the area of switch mode power supplies.

The power range of the SMPS market starts from a few watts to some kilowatts. In the kilowatt range, the telecommunication power supplies form the major part of the SMPS market.

In any business, network availability is of crucial importance and depends on the quality and proper operation of the hardware and software elements. The functioning of the hardware and software elements in turn depends on the quality of power. For a telecom power system for example, due to minimized

downtimes, which is only a few minutes in its lifetime of approximately 20 years, the associated power system is required to be of high quality and high reliability. In addition to system redundancy, essentially high quality is required for each subsystem. Power converters are always at the top of the failed component list that has a very big impact on a telecom power system. If the AC/DC rectifier stage fails, a large subset of a telecom system will not function. The voice or data transmission capacity will be reduced significantly, although the battery will provide some back-up time at this condition. However, at a telecom load, if the DC/DC power supply fails, the board will not function and, sometimes, the expensive digital integrated circuits on the circuit board may be damaged. This causes local service disruption [1].

The power demand and efficiency requirements of modern telecommunication systems are growing with each generation of equipment. As a result, the need for sophisticated power management design strategies are becoming more acute as system loads increase.

Power electronics is a central part of these infrastructures and is required to meet the design requirements. A telecom power system is an important part that needs to provide reliable and cost effective power solution to modern telecommunication power systems.

1.2. DEVELOPMENT OF SWITCH-MODE TECHNIQUES

1.2.1. Linear Regulator versus Switch Mode Technology

With the introduction of the transistor in the early 1950's, and especially with the development of integrated circuits from the early 1960's onwards, designers of electronic equipment, computers and instrumentation have increasingly demanded smaller, more efficient power sources to supply their equipment. To

meet this demand, the power supply itself has become more and more sophisticated. In fact the developments in power supply technology can be directly related to the introduction of various power semiconductor devices, even though the theory, in many cases, was already well known.

The regulated power supply technology can be divided into two distinct classes; firstly, the linear or series regulator and, secondly, the switch-mode conversion technique. Switch-mode technology is multi-facetted with a wide variety of topologies achieving the end result of providing a regulated DC voltage.

The main differences between the linear and switch-mode regulator are in the size, weight and efficiency. The linear regulator utilizes simple techniques of controlled energy dissipation to achieve a regulated output voltage independent of line and load variations. It is therefore, inherently inefficient, especially when a wide input voltage range has to be catered for. When linear techniques are applied to regulating a low voltage from the mains 110V or 240V AC source, then the disadvantages of the technique become apparent.

A typical linear power supply is shown in Fig.1.1. The step-down, low frequency mains transformer is very bulky, large heat-sinking is required to dissipate the heat generated by the regulating element and very large filter capacitors are required to store enough energy to maintain the output voltage for a reasonable length of time when the mains source is removed. Switch-mode techniques, on the other hand, offer the possibility of theoretically loss-less power conversion. The switch-mode regulator, employs duty cycle control of a switching element to control the flow of energy and thus achieves regulation. When applied to off-line applications, it has the added advantage of giving significant size reduction in the voltage transformer and energy storage elements.

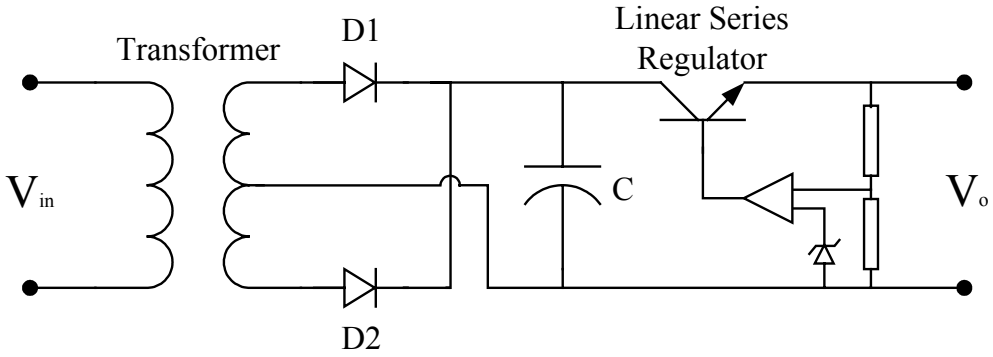


Fig.1.1.Practical Linear Series Regulator Circuit

Since a switch-mode converter can operate at significantly high frequencies, smaller transformer using ferrite cores can be used. Also, since the rectified mains voltage is chopped, energy storage for hold-up can be accomplished on the primary side of the step-down transformer, and so much smaller capacitors than the linear counterpart can be used, as shown in Fig.1.2 below.

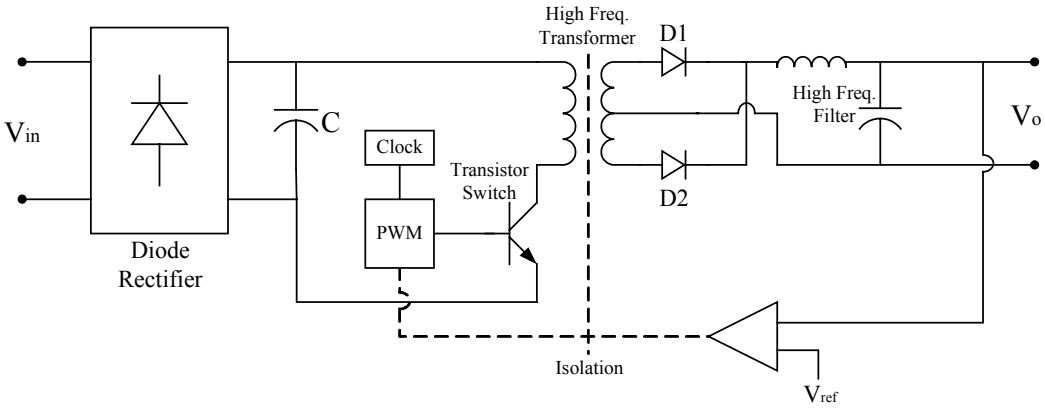


Fig.1.2. Practical Circuit of a Switch-Mode Regulator

Although the benefits of switch-mode techniques are great, there is a penalty paid in the increased noise present at both input and output of the supply due to the power switching techniques. Also the associated control circuitry is much more complicated than its linear counterpart.

Historically, the linear regulators were very common during the late 1950's and early 1960's when power supplies using switching techniques were very rare. The ascendency of switch-mode power supplies is directly linked to the development of fast high voltage switching power transistors in 1967 and, to a lesser extent, on developments in ceramic ferrite materials and capacitor technology [2]. Even so, linear regulators and power supplies still have their areas of application today, such as at low power below 50W, where the costs of the different technologies is comparable, and also in stabilised bench power supplies. The linear regulators are also preferred where a virtually noiseless supply is required.

The origins of switch-mode converters are linked with the developments in inverter circuitry. The earliest described inverters were developed before the first transistors appeared and, therefore, employed valves as switching elements, such as a push-pull inverter described by Wagner [3]. After the first bipolar junction transistor was produced in 1948 [4], there was a proliferation in inverter circuit designs. In 1952 a low power high voltage DC supply was described by Bryan for applications such as Geiger counters [5]. This utilised a transistor in an oscillator with power delivered to the output in a flyback mode via a transformer.

From 1952 onwards, Germanium power transistors increasingly became available [6] so giving impetus to inverter developments. The various forms of transistor switching circuits developed during the 1950's were categorised into three main groups by the end of the decade, [7] namely Ringing Choke [8], Self-Oscillating Push-Pull [9] and Drive Push-Pull Converters.

The 1960's heralded the development of the modern forms of switching regulators and switch-mode power supplies. During the early 1960's three forms of non-dissipative switching regulators were developed for low voltage DC to DC applications. They are the buck, boost and buck-boost regulators (Appendix

A). The buck regulator steps down the input voltage to a lower regulated output voltage. The boost regulator steps-up the input voltage to a higher regulated level. The buck-boost regulator, also referred to as a flyback regulator, is used to regulate a negative voltage at a level higher or lower than the positive input voltage. The method of regulator control in all cases is achieved by varying the duty ratio of the electronic switch, most commonly by pulse width modulation (PWM).

Power supplies working from the mains for the commercial market were still largely linear forms, with isolation, a necessary requirement for safety, being achieved by using a bulky mains frequency transformer. The major breakthrough for the commercial power supply section occurred at the end of the 1960s with the introduction of high voltage silicon switching transistors [6].

Power supply design engineers were then able to implement switching regulator and inverter technology into stabilized power supplies operating from the mains. In the USA, with the advantage of a lower magnitude (110V rms) mains supply than Europe, manufacturers of power supplies were the first to introduce switch-mode converters. In Europe also, switch-mode power supply developments took place using the new high voltage switching transistors.

1.2.2. Review on Switch-Mode Power Supply Topologies

While the commercial switch-mode power supply manufacturing industry was beginning to grow during the 1970s, the theory and technology of switch-mode conversion was being relationalised as part of the academic discipline of Power Electronics. By far the greatest contribution made within the discipline has been the work done by R.D. Middlebrook and his colleagues in the Power Electronics Group of Caltech in California, USA. The initial work of the Caltech Group, started in 1970, was aimed at developing models for the three basic dc-to-dc

switching regulator topologies already developed in the 1960s, namely the buck, boost and buck-boost converters [10-11]. From this work stemmed the modelling and analysis method called state-space averaging which allowed the theoretical prediction of a converters frequency response, and therefore a better understanding of a switch-mode regulator's feedback loop and stability criteria [12-14].

Further work at Caltech, especially by Cùk in his PhD Thesis, produced a fourth member of the basic dc-to-dc switching regulators which has been described as an optimum topology because of its symmetrical structure and non-pulsating input and output currents [15]. The new optimum topology DC/DC switching regulator is now commonly known as the Cùk converter after its inventor and completes the family of single-switch non-isolated switching regulators. The circuit diagram of the family are given in Fig.A.1 in Appendix A together with the steady-state current waveforms and input-output transfer functions.

In many applications, such as operating off the AC mains, isolation is a necessary requirement within the converter between input and output. By inserting an isolation transformer into the four basic switching regulator topologies, then the four single-ended isolated switching converters have been derived (Fig. A.2 in Appendix A).

The isolated buck and isolated buck-boost topologies are more commonly referred to as the forward and flyback converters respectively, and are the most popularly used topologies in commercial switch-mode power supplies .

The main disadvantage of the single switch topologies is the need for the high voltage blocking capability of the transistor switch (twice the DC input voltage), especially when operating from a rectified AC mains supply. Also, the single switch topology is not an ideal solution for higher power converters, where the

current rating of the transistor switch needs to be much greater. Therefore, another group of isolated converters utilizing more than one switch can be identified. Fig.A.3 in Appendix A illustrates the three multiple switch topologies, namely the half-bridge, full-bridge and push-pull converters. All three converters are buck derived due to the nature of switching involving pulsating input current and non-pulsating output current and also having an identical ideal voltage gain as the forward converter.

These topologies also have an added advantage over the single-ended forward and flyback converters in that full flux swing of the transformer core occurs instead of only a half swing of flux capability. This makes these multiple switch topologies more suited to higher power operation.

The topologies reviewed previously in this section all have their more favoured applications. In general switching regulators are commonly used as secondary regulators on multiple-output units, isolated single-ended configurations are used in low power single or multiple output ac to dc converters, and multiple switch topologies are used for higher output power applications [79].

1.2.3. Control Techniques

The major control techniques adopted traditionally in switch-mode power supplies are as follows:

- Voltage Mode Control
- Peak Current Mode Control
- Average Current Mode Control

1.2.3.1.Voltage Mode Control

This is the traditional method where there is a single voltage feedback path, with pulsewidth modulation performed by comparing the voltage error signal with a constant ramp waveform [16]. Current limiting must be done separately (Fig. 1.3).

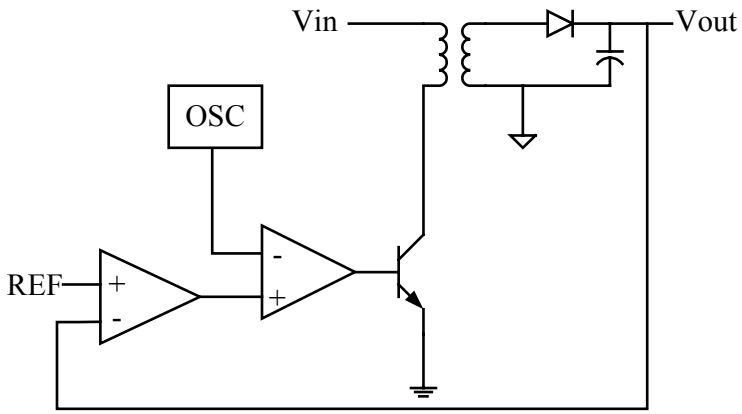


Fig.1.3. Voltage Mode Control

The advantages of voltage-mode control are:

1. A single feedback loop is easier to design and analyse.
2. A large-amplitude ramp waveform provides good noise margin for a stable modulation process.
3. A low-impedance power output provides better cross-regulation for multiple output supplies.

Voltage-mode's disadvantages can be listed as:

1. Any change in line or load must first be sensed as an output change and then corrected by the feedback loop. This usually means slow response.

2. The output filter adds two poles to the control loop requiring either a dominant-pole low frequency roll-off at the error amplifier or an added zero in the compensation.
3. Compensation is further complicated by the fact that the loop gain varies with input voltage.

1.2.3.2. Peak Current Mode Control

Peak current mode control adds a second control loop to the voltage feedback loop. In place of the ramp from the oscillator, as in voltage mode control, the current ramp derived from output inductor current is used for the error voltage-to-PWM process. The oscillator now only serves to fix the frequency of operation. The level of error voltage dictates the maximum level of peak current allowed [16] (Fig. 1.4).

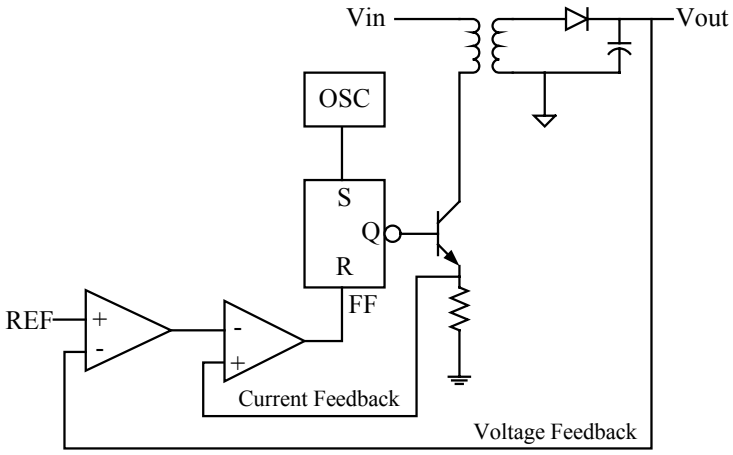


Fig.1.4. Peak Current Mode Control

The advantages which this control technique offers include the following:

1. This mode of control will respond immediately to line voltage changes, eliminating both the delayed response and gain variation with changes in input voltage.

2. Since the Error Amplifier is now used to command an output current rather than voltage, the effect of the output inductor is minimized and the filter now offers only a single pole to the feedback loop (at least in the normal region of interest). This allows both simpler compensation and a higher gain bandwidth over a comparable voltage-mode circuit.
3. Additional benefits with current-mode circuits include inherent pulse-by-pulse current limiting by merely clamping the command from the Error Amplifier, and the ease of providing load sharing when multiple power units are paralleled.

While the improvements offered by peak current-mode are impressive, this technology also comes with its own unique set of problems which must be solved in the design process [16]. A listing of some of these is outlined below:

1. There are now two feedback loops, making circuit analysis more difficult.
2. The control loop becomes unstable at duty cycles above 50% unless slope compensation is added.
3. Since the control modulation is based on a signal derived from output current, resonances in the power stage can insert noise into the control loop.
4. A particularly troublesome noise source is the leading edge current spike typically caused by transformer winding capacitance and output rectifier recovery current.
5. With the control loop forcing a current drive, load regulation is worse and coupled inductors are required to get acceptable cross-regulation with multiple outputs.
6. Average current is what should be controlled, but peak is controlled instead. The peak to average error is quite large, especially at light loads,

and the voltage loop must correct for this, which increases response time [17].

1.2.3.3. Average Current Mode Control

Peak current mode control operates by directly comparing the actual inductor current waveform to the current program level (set by the outer loop) at the two inputs of the PWM comparator. This current loop has low gain. Referring to Fig. 1.5, the technique of average current mode control overcomes these problems by introducing a high gain integrating the current error amplifier (CA) into the current loop. The desired current program level is compared with the voltage across current sense resistor R_s, which represents actual inductor current. The difference, or current error, is amplified and compared to a large amplitude sawtooth (oscillator ramp) at the PWM comparator inputs. The gain-bandwidth characteristic of the current loop can be tailored for optimum performance by the compensation network around the CA. Compared with peak current mode control, the current loop gain crossover frequency can be made approximately the same, but the gain will be much greater at lower frequencies [17].

The result is:

1. Average current tracks the current program with a high degree of accuracy.
2. Slope compensation is not required, but there is a limit to loop gain at the switching frequency in order to achieve stability.
3. Noise immunity is excellent.
4. The average current mode method can be used to sense and control the current in any circuit branch. Thus it can control input current accurately with buck and flyback topologies, and can control output current with boost and flyback topologies.

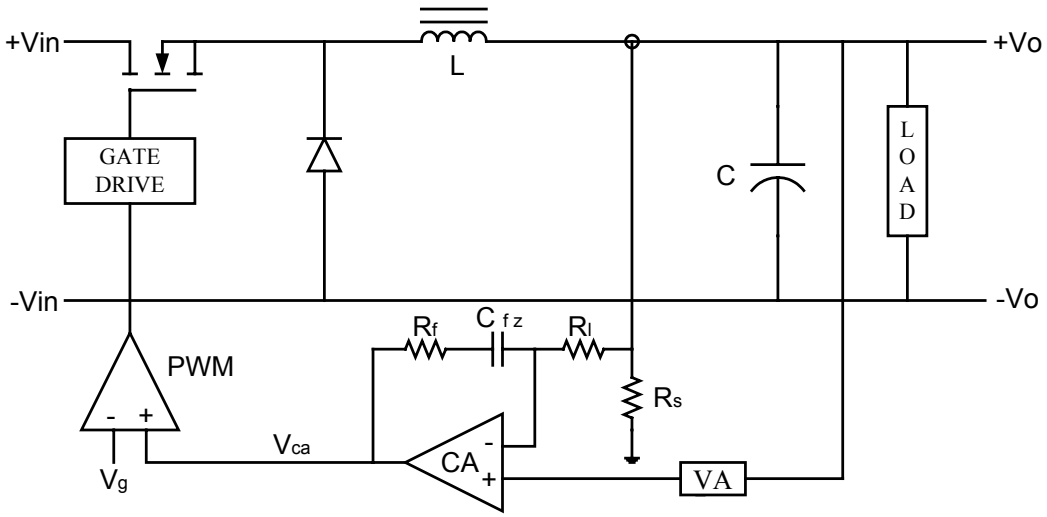


Fig 1.5. Average Current Mode Control

1.3. TELECOMMUNICATION POWER SUPPLIES

1.3.1. Recent Trends in Telecommunication Power Supplies

The supply voltage of most telecommunication switching equipment is 48V. This voltage value is a universal standard for telecommunications equipment, and is well defined both by the European Telecommunications Standards Institute (ETSI) and the American National Standards Institute (ANSI). One of the motives behind the universal 48V DC standard is that it allows to work on a live conductor with minimum risk for personal injury and without special safety measures. This is a practical advantage when crafts persons work at a distance from the voltage source, and therefore can not disconnect it [18].

A 48V DC power supply system consists of a number of paralleled rectifiers that connected to one or more battery strings also connected in parallel. Generally, the power levels of the rectifier modules involved in telecommunication applications are 750W or 1500W. In the event of a mains outage or rectifier failure, the load continues to operate from the batteries without switching or

interruption. The distribution of power to the loads originates at the point where the battery strings are paralleled, with only fuses or circuit breakers interposed (Fig.1.6) [18].

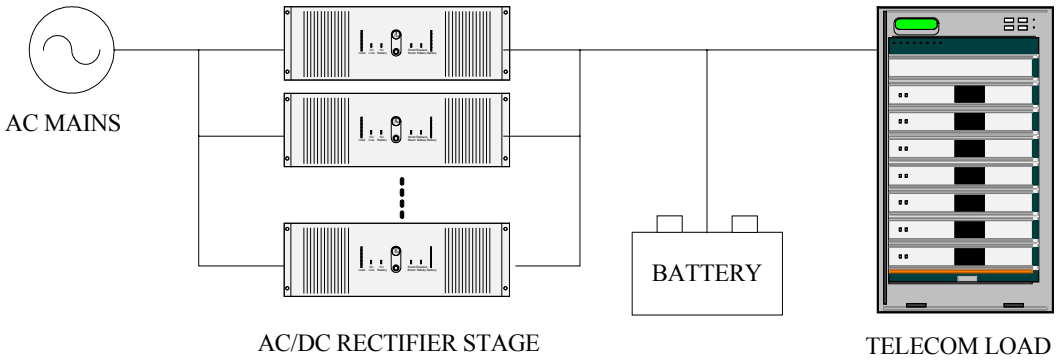


Fig.1.6. A typical telecom power system

During operation, the parallel rectifiers provide the current consumed by the load, the float current for the batteries and the additional current for recharging the batteries after a mains outage. Redundant rectifiers meet two needs: battery recharging after mains outage and continued operation if one rectifier fails [18].

Nowadays, digital telephone exchanges need to be fed from a power supply which guarantees a high reliability degree and accurate electrical requirements. The recent features required by the telecommunication equipment can be summarized as follows :

Remote Controlled : The power equipment must be 'intelligent', and suitable to be connected to a remote supervision system. This will decrease the maintenance cost [19].

In telecom power supply systems most functions are supervised. The traditional solution is to use a centralised control unit. This requires a lot of cabling and is not very flexible. The emergence of small, powerful and inexpensive

microcontrollers has made a new distributed control system possible, a system where collection of data is done close to the actual component [20].

The power supply system is part of a bigger telecommunication system. In many cases it is vital to know that every part of the system is working as intended. When an alarm occurs this information will be relayed to the main controller. Locally this will produce an alarm. An alarm relay is activated and can be used in other local supervision systems. This has traditionally been the extent of power supply supervision systems. Now more customers tend to demand a higher level supervision. A big telecommunication system spread over a large area has a power supply at each site [20].

Some means of communication between the main controller at the site and the central office is necessary. A computer network, dial-up connection, leased lines or a multi-drop serial bus will suffice. At the central office a network server will handle all communication with the power supply systems. The end user is able to get all necessary information from the sites [20].

Reduced dimensions and weight : This feature is an important requirement for telecommunication equipments in order to be installed in reduced floor space of normal civil building or collocated in the same room of the telephone exchange [19].

Modularity (System Extendibility) : The initially installed rectifier system should be suitable for the installation of additional rectifier modules [21].

Modular systems are imperative for simple and inexpensive maintenance of installations by people with limited training on power systems, a need shared by telecom operators with other companies and organisations [18].

Operation reliability : Traditional telephony enjoys a service availability in the vicinity of about 99.999% (“five nines”) to 99.9999% (“six nines”). The reliability of the electricity grid is of the order of only 99.9% (“three nines”). Because of the backup power systems, the availability of telephone services is not limited to “three nines“ by the electricity supply [22].

Redundancy (n+1) : In determining the number of the modules it should be taken into account that for the reason of safety at least two rectifier modules must be installed ($n \geq 2$). It is an additional requirement that the power supply system must meet the requirement of the telecommunications load even in the case of a module fault [1].

Better electrical performances : The output voltage transient must be kept at minimum level at the different working conditions [19]. The main requirements are low EMI, and high power factor or low harmonic distortion [1]. For the purposes of telecommunication powering, the actual quality of the AC supply is not particularly relevant. With DC backup infrastructure, the telecom equipment are always galvanically isolated from the mains. The large system battery also works as a filter against possible transients or harmonics passing through the rectifier. However, this is not the case when considering the general consumption of electricity. Modern electrical appliances and devices have only limited immunity to poor power quality, and are increasingly affected by the power quality aspects of the supply, more than in the past [18,22].

The noise and EMI requirements are very strict for the telecommunication power supplies. All telecom power equipment placed on European market has to comply with the requirements of EN 300 386-2 standard latest on October 1, 2001. EN 300 386-2 that covers both emission and immunity requirements will become a common EMC requirement basis for most of telecom power manufacturers worldwide [23].

High efficiency : The power demands and as a result the efficiency requirements of modern telecommunication systems are growing with each generation of equipment. High efficiency power conversion is an essential element in cutting the running costs of a telecommunications system [80]. End users save cost over the product lifetime due to:

- Lower utility costs.
- Higher MTBF.
- Cheaper input filtering options.
- Less front-end power.

1.3.2. Application of Switch-Mode Techniques to Telecommunication Power Supplies

During the 70's and 80's the development pace of new DC systems were, in today's terms, quite low. The technical improvements were fewer and a typical system could have a life cycle of ten to fifteen years before replaced by a new product. The rectifiers were mainly Ferro-Resonant or Thyristor-based, and the system was placed in the basement and was feeding a telecom switch one or several floors above. The power equipment was of the same brand as the switch, like Nortel, Ericsson, Siemens and Lucent, and was in most cases owned by the governmental controlled PTT (Post, Telephone and Telegraph) or BOC (Bell Operating Company) [24].

In 1986, the rectifiers used in Turkish Telecom were thyristor-controlled full bridge converters. These rectifiers have an efficiency in the order of %83, and an input power factor of 0.8. These rectifiers are also very heavy and bulky.

In the second half of 1980's, Ferro-Resonant technology is started to be used in telecom rectifiers [25]. A Ferro-Resonant power supply is very similar to an

unregulated power supply except for the characteristics of the ferro-resonant transformer (Fig.1.7).

The Ferro-Resonant transformer supplies a constant output voltage over a wide variation of the transformer input voltage. Regulation takes place within step-down transformer by core saturation means. The problems with using a Ferro-Resonant power supply include that it is very sensitive to slight changes in line frequency and would not be switchable from 50 Hz to 60 Hz, and that the transformers dissipate more heat than conventional transformers. These power supplies are heavier and will have high audible noise from the transformer resonance.

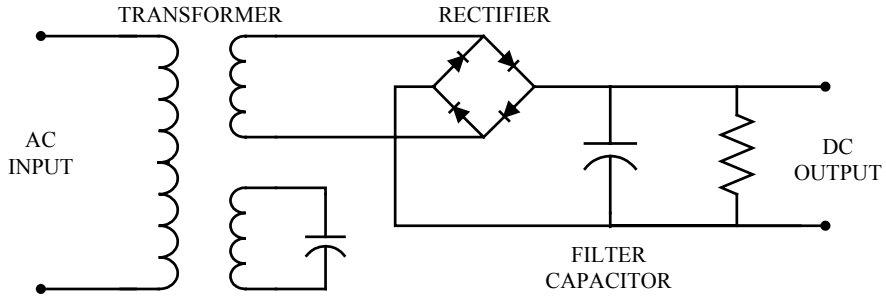


Fig.1.7. Ferro-Resonant Power Supply

In the first half of the 1990's, the switch mode power supply technology was started to be used in the telecommunication power supplies. First, the double switch forward converters have been used. In the "double switch forward converter", also called asymmetrical half bridge forward converter, the magnetizing energy stored in the primary inductance of the transformer is automatically returned to the bulk capacitor by the two demagnetization diodes. The two power switches and demagnetisation diodes have to withstand half of the voltage compared to single switch forward converter. The double switch forward converter needs a floating gate drive for the high side switch (Fig 1.8) [26-28].

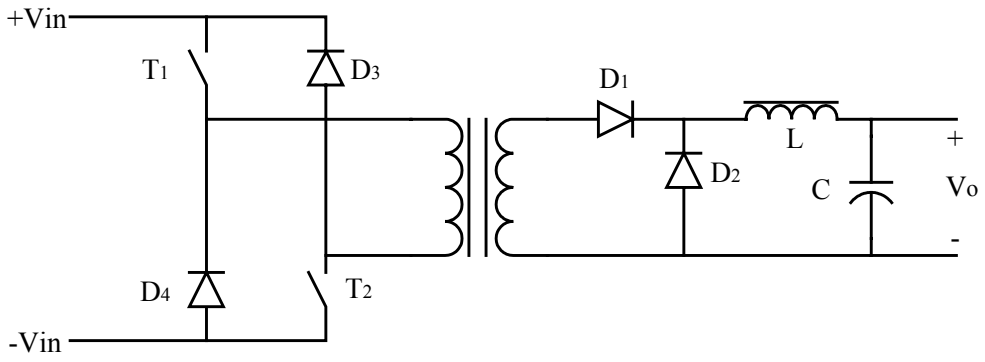


Fig.1.8. Double Switch Forward Converter

In [29], a 10kW, 100kHz zero voltage switching with additional capacitors (ZVSWAC) type DC/DC converter for telecommunication power system has been introduced. (Fig.1.9) The unit consisted of two types of high frequency converters – Buck converter and DC-DC converter. The ZVS type Buck configured by an energy recovery snubber produces 250V DC. Its switch – IGBT is switching at 20kHz. The modified phase shifted full bridge type dc/dc converter consisted of two 5kW modules which produces 50V DC from 250V DC. Its switches – MOSFETs are switching at 100kHz. It has over 0.9 input power factor, and 88% efficiency. The AC input circuit for this circuit consisted of a Buck converter after a diode bridge rectifier. The Buck converter uses IGBT by switching device, and ZVS characteristics is got by an energy recovery snubber at 20kHz.

Today, the requirements of the telecommunication power systems are very strict. The power supplies used in telecommunication applications should have unity input power factor, high efficiency, and very short transient response time. Therefore, two-stage AC/DC rectifier is used in the telecommunication rectifiers nowadays. One stage is the AC/DC converter that converts the AC line voltage into an intermediate DC voltage (usually 400V). Power factor correction is achieved in this stage. In late 1990's, diode bridge was used in this stage.

Nowadays, the power factor preregulator boost converter is commonly used, because of its easy control for input current wave shaping and it is suitability for high DC output voltages [1].

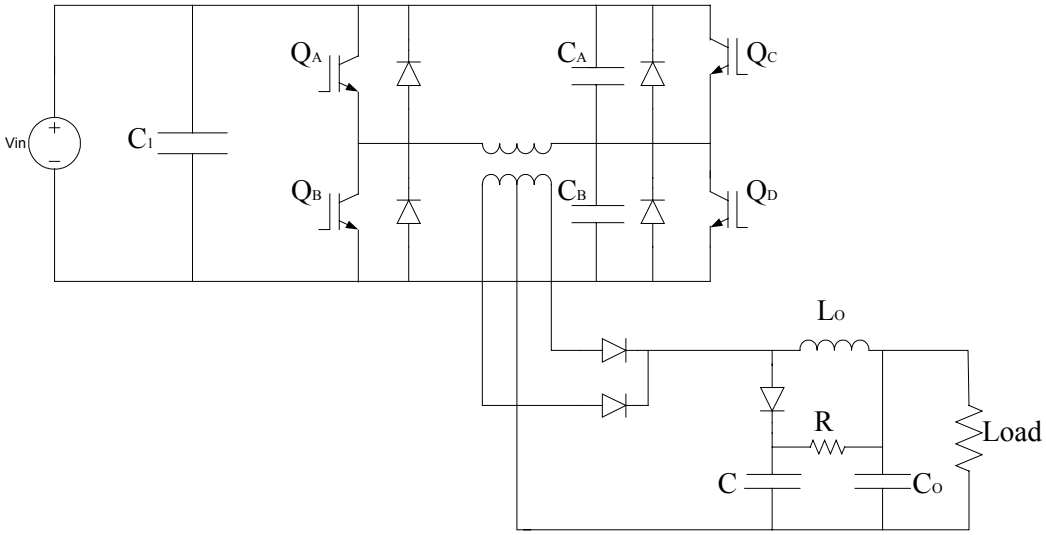


Fig.1.9. Zero voltage switching with additional capacitors (ZVSWAC) type DC/DC converter

The second stage is the DC/DC converter, that converts the preregulated 400V DC to nominal output voltage (usually 48V DC). Electrical isolation is provided at this stage. A phase-shifted bridge converter is preferred for high power applications [1]. (Fig1.10) The benefits of soft-switching converters, and in particular zero-voltage switching (ZVS) circuits, are well-known. High-frequency converters powered from a high source voltage show significant improvements when operated with soft switching [30-36]. These improvements are:

1. reduced switching losses, which allow high switching frequency and size reduction of reactive components,
2. reduced EMI/RFI noise,
3. no need for complex and expensive snubbers,

4. exploitation of the parasitic circuit elements to help the resonant transition.

Because of these characteristics, ZVS topologies are now widely used in power electronics, and especially in telecom power systems [37]. The switching loss can greatly be reduced by using ZVS. However, the ZVS condition is usually too narrow and the conduction loss high. On the one hand, the lagging leg transition is slow, and possible under almost all conditions, on the other hand the leading leg transition is abrupt and the ZVS operation is highly dependent on the load condition. The freewheeling periods inserted into the primary side of the transformer cause conduction loss in the switching devices. To solve these two problems zero-voltage and zero-current switching has been proposed [38-39].

Nowadays, manufacturers focus on producing higher quality, reduced cost, and more compact products by integration. Integration is a keyword meaning to use the ASIC (Application Specific Integrated Circuit) technology both in power components and controlling/monitoring. Integration means less discrete components and results in less manufacturing cost as well as improved product reliability and quality. ASIC technology normally implies the use of mixed signal processes including DSP necessitating the adoption of a computer-controlled system [40].

1.4. DIGITAL CONTROL OF SMPS

In recent years, increasing demand for high power converters in telecommunication, and computer power supplies drives the need for higher flexibility in control, increased level of system integration, and more reliability, besides achieving high levels of performance. Digital controllers provide the flexibility to implement sophisticated control algorithms by easy programming

without modifying the hardware, and the ability to implement communication for remote monitoring/control functions, in addition to features such as noise immunity, less susceptibility to environmental conditions, component tolerances, and aging etc.

Digital control provides the flexibility to implement sophisticated and nonlinear control algorithms [41-42]. From a performance reasoning, some researchers believe that deriving a control action from linguistic rules might be a general design approach that avoids some complexities associated with nonlinear mathematical modeling. Fuzzy logic is aimed at providing solution for controlling non-linear processes and to handle ambiguous uncertainty linguistic variables. Some work on implementing fuzzy controllers to dc/dc converters has been reported in the literature [43-45].

Noise immunity, resistance to environmental effects and component tolerances are the attractive features of digital controllers. In a DC power supply with galvanic isolation and analog controller implementation, the analog signal at the output of the error amplifier is transmitted to the primary side through an opto-coupler that operates in linear mode as a gain stage. A drawback of this approach is that the opto-coupler gain can vary significantly from component to component and due to over temperature. In a digital controller implementation, the output can be converted to digital by an A/D converter placed at the output side and digital error signal can be calculated and transmitted as serial data through an opto-coupler that operates as a logic gate. In the digital implementation, the loop performance is not affected by variations in opto-coupler or error amplifier parameters, which allows a less conservative design of the feedback loop. An implementation of a digital controller chip set consisting of two ASICs, one for the primary side and one for secondary side, for DC-DC converters with transformer isolation has been reported in [46]. The secondary-side controller includes an A/D converter that outputs a digital error signal,

which is then transmitted as serial data through an opto-coupler that operates as a logic gate. The primary-side controller includes a serial data receiver that restores the digital error signal, a programmable digital regulator that implements a discrete-time control law, and a high- resolution (10-bit) digital pulse-width modulator (DPWM) with programmable switching frequency (up to 700 KHz).

Digital controllers also provide the ability to implement communication for remote monitoring/control functions. A microcontroller unit processing the input signals and controlling the rectifier state (by varying the voltage and current references, and by turning on or off the rectifier in case of alarms), displaying the measurements, the alarms and the state and allowing connection through a serial bus to a centralized control unit is implemented for a switch-mode three-phase 200A/48V rectifier with input unity power factor [47].

To benefit from the advantages of the digital controllers, a few research has been carried out in the area of the switch mode power supplies [43-65].

Most of the research on digital controllers have been carried out on power factor corrector (PFC) side of converters as it is not needed to have too fast response time for this kind of converters [48-51]. One of the major drawbacks of the digital controllers is that they are slower than analog controllers. They are well suited for PFC application as they can provide the needed response time, and provide the advantages like flexibility, low sensitivity to environmental conditions, and additional processing options like monitoring and controlling from remote site.

The digital controller implementation with PFC converters also provides performance improvements because of the digital control techniques involved in the design. A simple and efficient method for implementation of a digital

controller for a power factor corrector based on a boost converter operating at the switching frequency of 200kHz, that exhibits very low harmonic distortion of the input current, and extended bandwith of the outer voltage loop was introduced in [49]. Another adopted control technique improving the system dynamics is given in [51].

A control scheme is proposed for controlling multiple single-phase power-factor-correction (PFC) modules with a single low-cost digital signal processor (DSP) [50]. The proposed scheme allows for multiple PFC modules of different current ratings to be operated in parallel and controlled via a single DSP. DSP-based control provides simple current sharing, provides size reduction and lower cost.

It is necessary to sample the analog voltage and current to realize the proper feedback control in power factor correction applications. The sampling speed is greatly limited by the A/D conversion speed of DSP chips. For a digitally controlled PFC, single sampling in one period (SSOP) makes the controller more sensitive to the noise. A high peak often appears at the switching point due to switching noise coupled to the current sensor. Such noise creates difficulties in keeping system proper operation. A novel sampling algorithm is proposed in [52], that can improve the switching noise immunity greatly.

The advantages of digital controllers force power supply designers to include such controllers not only in PFC, but also in other type of converter designs. Results from an investigation into the modelling, and simulation of DC/DC converters controlled by an 8-bit microcontroller have been discussed in [53]. [54] presents the design oriented analysis of digitally controlled dc-dc power converter with very high switching frequency.

In 1993, the idea (no experimental result is reported) of a microcontroller based dc power supply working at a frequency 40kHz was reported [55]. In this design

the microcontroller is used to produce a reference voltage for the single phase inverter, and since it should run at very high frequency, a hardware circuit is added for feedback and compensation purposes.

A digital PID controller for the PWM and/or PFM controlled switching dc-dc converters is presented in the literature in 1998. This digital controller can be used for the dc-dc converters whose switching frequency can be varied from 20kHz to 500kHz. It is composed of discrete digital components like counters, latches, etc. to fulfill the high speed requirements, as the microcontrollers, and DSP technology at that time could not satisfy this requirement [56].

Another digital PID controller for a buck converter operating at 1MHz was reported in 2003. The proposed digital PID controller circuit consists of TTL and memory IC's. The memory IC's are used to improve the calculating time for I-D control process [57].

One of the major disadvantages of digital control has been the limited control loop bandwidth due to the time delay introduced by the zero order hold effect, and the computational time delays.

A technique that compensates for the phase lag introduced by the zero-order-hold was presented in 1999. The proposed compensator adds a pole/zero pair to the existing controller. This method has the advantage of being relatively simple to implement. However, the proposed compensator only compensates for a part of the control loop overall delay [58].

To answer more precisely the problem of computational time delay in switch mode power supplies, some predictive techniques were proposed. The proposed control schemes are simple to design and implement. However, although they

improve the controller dynamic response, they do not reach the level of performance obtained with traditional analog controllers [59].
A design procedure based on the dead-beat concept for a DC/DC converter working in the continuous mode was proposed. This method relies on prediction of the output current and voltage to overcome the zero-order-hold effect [60].

Another problem with digitally controlled high-frequency PWM converters is the resolution limitation caused by the minimum timing cycle of hardware timer used to generate the PWM waveform. Some PWM techniques have been proposed to overcome this limitation [61-63].

Double PWM technique adopts the idea of high frequency switching and low frequency modulating. This technique adds a lower-frequency PWM (called the second order PWM) into conventional PWM (called fundamental PWM). But in this technique, one can adjust the output in the modulating frequency (the second order PWM) which causes the system response time to increase [61].

The design of a digital controller for a low-power high-frequency buck converter has been reported. In [62], an external DPWM chip is used as the built-in PWM units on the DSP used could not supply the needed resolution. Another implementation of DPWM by using and FPGA chip is given in [63]

Digital controllers are more expensive than analog counterparts for low power applications. To overcome this issue, a multi-output converter system that controls, simultaneously and independently, the separate Buck converter and Boost converter with the different specifications by one DSP digital controller has been presented [64]. The Buck converter is designed to operate with the switching frequency 10kHz, the output voltage 5V, the input voltage 15V, and the output current 1A. Boost converter has the switching frequency 10kHz, the output voltage 24V, the input voltage 15V, and the output current 1A.

In summary, relatively few digital controllers have been built for dc-dc converters used in high frequency switch-mode power supplies [43-64]. Recent advances in DSP technology, however, make now possible the direct implementation of digital control in high frequency switch-mode power supplies, without the need for sophisticated control algorithms for compensation of the time delays. Therefore, digital control applications are now feasible not only in the area of ac drives and three-phase converters, where they are extremely popular, but also in the field of DC/DC converters used in SMPS.

1.5. SCOPE OF THE THESIS

In reviewing previous work in the area of digital controllers, it is evident that the majority of the work has been carried out in the control of medium or high power variable speed drives, and UPS systems. However, limited research has been reported in the area of high power switch-mode power supplies, and most of the research on digital controllers in this area has been carried out on power factor corrector (PFC) side of converters, as it is not needed to have too fast response time for this kind of converters used as pre-regulators. Some implementations have been done to control the DC/DC converters. In these papers, the authors have been mainly concerned with proving that certain digital control schemes can work for power converters, and to a lesser extent, with practical circuit design issues, such as power consumption and achieving high frequencies. In fact, the switching frequencies for the applications considered in these efforts have been in the order of 10-20 kHz, or lower as the digital signal processor technology at that time could not satisfy the processing power and speed requirement of such applications.

In this research work, design and implementation of a digital controller for universal telecommunication power supply modules, based on parallel-operated, dual processors have been presented. The contributions made to the related subject can be summarized as follows [67,68,78]:

- The Digitally-Controlled Universal Telecommunication Power Supply Concept has not been reported in the literature yet. The digitally controlled universal telecommunication power supply modules have the following additional software-controlled features over analog systems:
    - Extended operating output voltage range (0 – 70V DC adjustable output voltage via remote control or keypad) of the SMPS at universal input voltage range (80 – 275V AC).
    - Serial communication based active digital load current sharing between modules with automatic master/slave selection among parallel operated modules
    - Digital paralleling of modules up to 16 units to reach higher powers
    - User programmable current limit setting (adjustable between zero and maximum value)
    - User programmable temperature compensation curves
    - Automatic derating at low input voltages without extra hardware requirement
    - Program loadable in the field according to user requirements
    - Minimized component count, which is expected to yield increased Mean Time Between Failure (MTBF).

- Fully digital feedback control of the telecom power supply has been implemented:
    - The high processing power requirement of the implementation of the digital feedback to achieve tight transient response specifications of a high frequency Telecom power supply is

fulfilled by the first member of a new fixed-point DSP family : TMS320F2810.

- Additional features implemented by software are given as follows:
    - Output voltage and current limit setting of the modules can be adjusted from a remote site.
    - The alarms and events can be recorded on the power supply modules for maintenance purposes
    - Provides implementation of four stage battery charging algorithms by user selectable number of battery cells connected to the output as a back-up.

The contributions made in the thesis are only related to the digital controller side of the power supply, the power stage is an existing analog design, which is out the scope of this thesis.

The outline of the thesis is given below:

The second chapter describes the building blocks, and technical/functional specifications of the designed telecommunication power supply. General information about the operation of each block is presented in this chapter.

Chapter 3 is devoted to the first phase of this thesis, which is concerned with the design and implementation of the digitally-controlled universal telecommunication power supplies, using two low cost 8-bit microcontrollers. In this chapter, the tasks of the digital controller and the interaction among these tasks have been presented in detail. The software implementation of these tasks have been reported. The experimental results obtained from the implemented power supply modules, the corresponding applications to industry, and field tests are given.

Chapter 4 covers the second phase of the thesis. The design and implementation stages of the DSP controlled ZVS phase-shifted full-bridge converter have been presented in detail. In the first sections of the chapter, theoretical design procedure is explained. The simulation results are given. At the end of the chapter, the corresponding experimental results are presented.

The last chapter is devoted to the conclusions and gives insight on further work that can be carried out based on this thesis.

CHAPTER II

SYSTEM DESCRIPTION

In this thesis, digitally controlled, universal telecommunication power supply modules have been designed and implemented. The modules consist of two converter stages. First stage is the AC/DC converter that converts the AC line voltage into an intermediate DC voltage of 400V. Power factor correction is achieved in this stage. The average current mode controlled power factor preregulator boost converter is used for this stage, because of its easy control for input current wave shaping and it is suitability for high DC output voltages. The second stage is the DC/DC converter, that converts the preregulated 400V DC to nominal output voltage, which is adjustable between 0-70V with 100mV resolution. Electrical isolation is provided at this stage. A voltage mode controlled zero voltage switching phase-shifted full bridge converter is used at this stage. The designed system also includes a two stage π - type EMI filter at the input of the power supply, and a single stage EMI filter at the output stage to meet the strict requirements of the CISPR-22A standards.

The electrical characteristics and functional specifications of the implemented digitally controlled power supply module are as given below.

Technical Specifications:

Input Characteristics:

AC Input voltage range:	Single-phase, 220 Vrms nominal
	80 – 275 V rms

Supply frequency:	45 – 66 Hz
Power factor :	≥ 99% (from half-load to full-load)
Input current THD:	< 10% (from half-load to full-load)
Inrush current:	< 8 A

Output Characteristics:

DC Output voltage setting:	0 – 70V with 100mV resolution manual/remote control Default setting: 53.5 V
Temperature compensation:	Adjustable
Output current:	33 A nominal
Current limit:	0 – 40A user adjustable
Efficiency:	≥ 93% (at full-load)
Static regulation:	≤ 50 mV (5 %- %100 load change) ≤ 50 mV (0 -55°C temperature change) ≤ 10 mV (±20% AC input voltage change)
Dynamic regulation:	1 V (from 10% to 100% load in 2 ms rise and fall time)
AC voltage ripple:	≤ 100 mV rms (at full-load) ≤ 10 mV (9 x 30 A parallel modules)
Soft Start:	No overshoot in output voltage and current ramp-up
Noise in 3.4-150 kHz frequency band:	≤ 5 mV
Psophometric noise:	2 mV, CCITT-A filter (9 x 30 A parallel modules)

General

Operating temperature:	0 - 55°C
Storage temperature:	-10°C - 70°C
Cooling:	Natural convection

Protections:

Output current limit:	Constant current down to zero volt
Output short-circuit:	Nominal current under short-circuit
Output over-voltage:	Over-voltage protection setting adjustable
Input under/over-voltage:	Rectifier is turned-off automatically by software
Excessive temperature:	For heatsink temperatures beyond 80°C, rectifier is turned-off
EMC	According to CISPR-22A

Functional Specifications:

- Rectifiers are operated with n+1 redundancy, and active digital load current sharing between parallel-operated modules.
- At the input of rectifiers, an ac contactor is present as an ON/OFF switch.
- Rectifiers have an adjustable over-voltage protection between 54-59V. In equalizing charge, over-voltage protection is inhibited.
- From the LCD present on the front panel of rectifiers, output current, output voltage, input voltage, faults, and alarms can be monitored.
- Rectifiers incorporate ‘flash-memory’ type parallel operating processors, with program loadable in the field according to the specific needs of the user.

- At the input of each rectifier, a 2000V (1.2 μs/50μs) protection exists according to IEEE Std. 587B and IEEE C62.41, against surge voltages such as lightning.
- Rectifier current limit setting can be adjusted by the user.
- For very low input voltages, rectifier current limit setting is automatically adjusted to a safe level not exceeding the maximum allowable input current limit.
- Rectifier outputs are short-circuit proof. Under short-circuit, the modules continue to supply the adjusted current limit value.
- Output voltage settings are adjusted manually via keypad, or from remote control via serial communication port.
- The number of battery cells to be charged can be set by the user via keypad from 1 to 30 cells, depending upon the requirements of the application.
- Temperature compensation curves used in charging the batteries can be programmed directly by the user via keypad.
- Temperature can be measured digitally from 4 different points (heatsink, ambient inside the module, PCB, and batteries).
- Rectifier modules are capable of storing statistical records of several events. In the records, module identification number, output current values, output and input voltage values outside the normal limits, and faults are stored.

The block diagram, and circuit diagram of the system are given in Fig.2.1 and Fig.2.2, respectively.

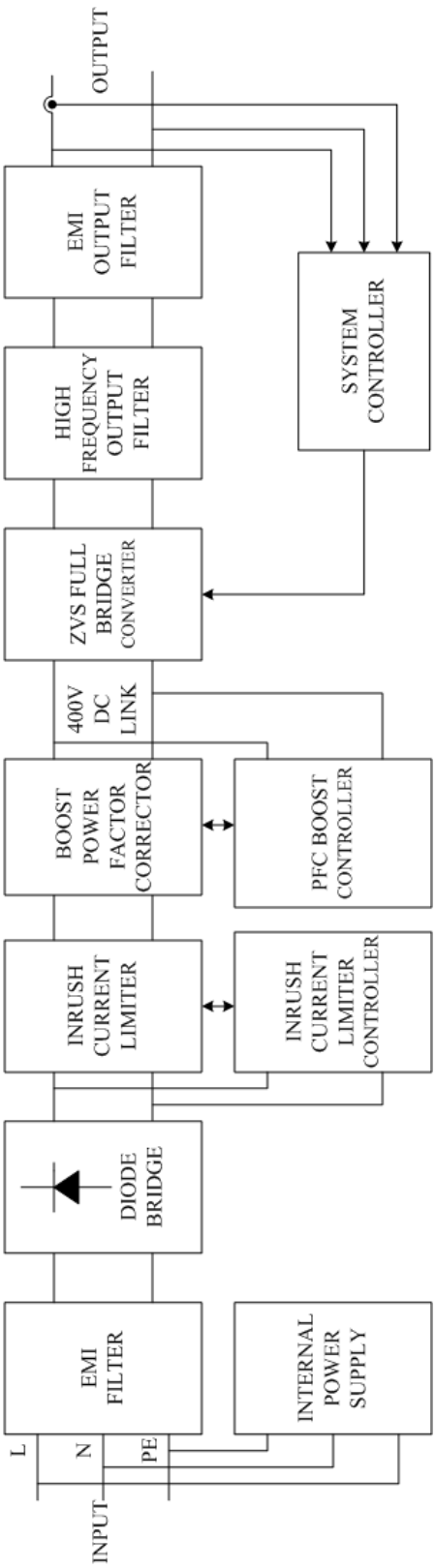


Fig.2.1. Block Diagram of the System

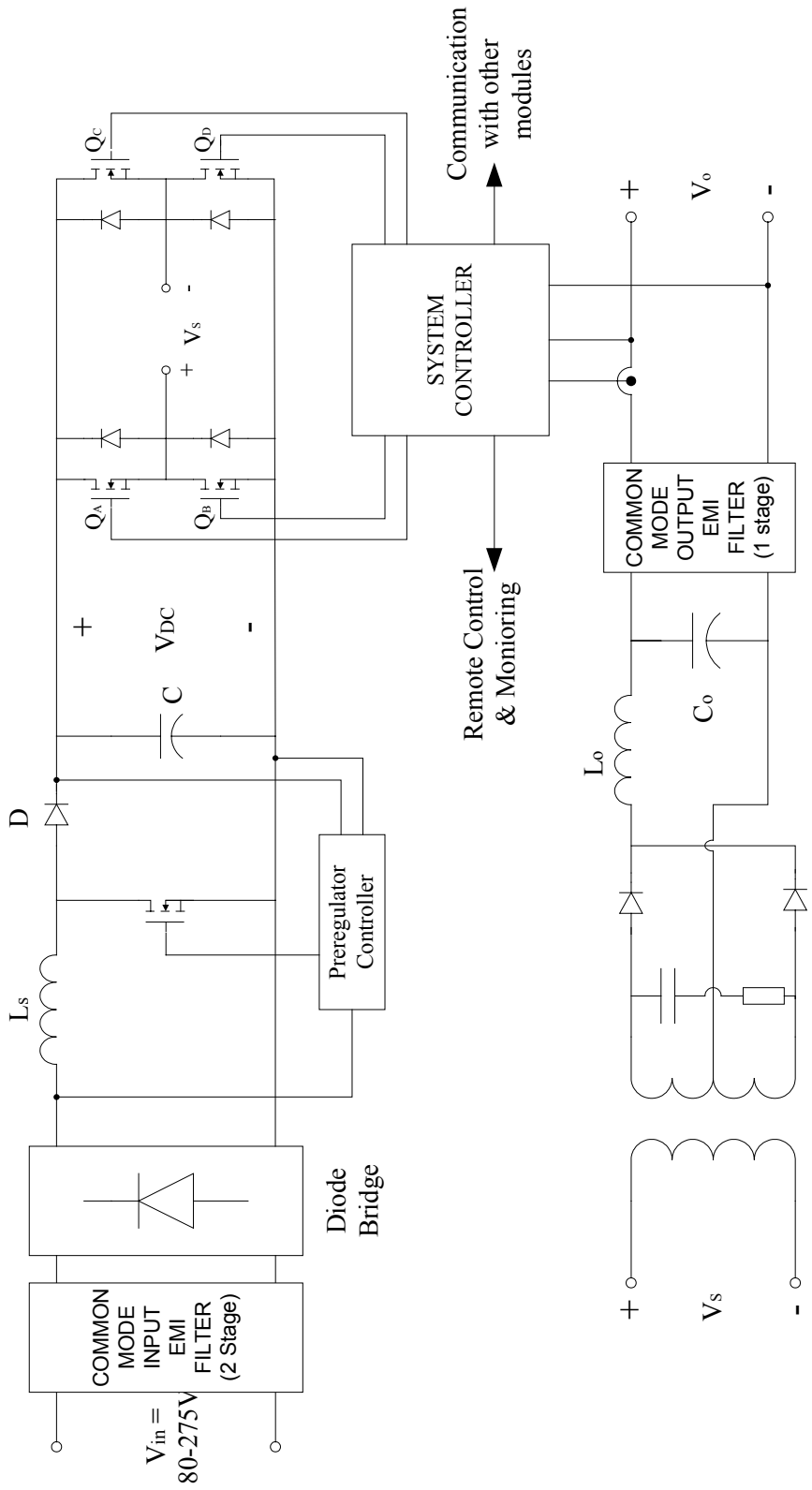


Fig.2.2. Circuit Diagram of the System

2.1.AC/DC PREREGULATOR STAGE

The AC/DC preregulator stage is the first stage of the designed converter that converts the AC line voltage into an intermediate DC voltage of 400V. Power factor correction is achieved in this stage. A boost type power factor corrector is used for this stage, because it is easy to implement input current wave shaping, and it is suitable for high DC output voltages.

Off-line switching power supplies usually employ a rectifier bridge or doubler with a simple capacitor input filter to draw power from the ac line. The bulk filter capacitor charges to nearly the peak ac line voltage, supporting an unregulated dc bus powering the downstream switching converters. This bulk capacitor must be large. It alone supplies total power during most of each half-cycle while instantaneous line voltage is below the dc bus. Unfortunately, with a capacitor input filter, the line current waveform is non-sinusoidal. Input power factor is only 0.5 – 0.65, and the high harmonic content causes line noise. High power factor is a requirement for many power supply applications, especially for the telecommunication power supplies.

Therefore, the high power factor switching preregulator is interposed between the input rectifier bridge and the bulk filter capacitor. Switching at frequency much higher than the line, the preregulator is programmed to draw a half-sinusoid input current, in phase with the line voltage. The current is controlled by the deviation of the dc bus voltage from the desired value. The result is :

- Improved power factor : 0.999 at rated load
- Reduced harmonics : ≤ 3% at rated load
- Tapless / switchless operation over the full 80V-275V line voltage range
- Smaller bulk capacitor size and cost.

- Crudely regulated bulk capacitor voltage. The resulting narrow dc bus voltage range permits the downstream converters to be designed for lower cost, and greater reliability and efficiency.
- Reduced rms charging current resulting in improved capacitor reliability [65].

In the designed system, a preregulator converter with a switching frequency of 80kHz using UC3854 controller is used. The design procedure of the preregulator stage is out of the scope of this thesis.

2.2. DC/DC CONVERTER STAGE

The second stage consists of a zero-voltage-switching full-bridge DC/DC converter operating at 75kHz to convert the pre-regulated voltage of 400Vdc to a regulated dc output voltage.

The attempts to reduce pulse-width modulated power supply size by increasing the switching frequency quickly ran into unacceptable switching losses in the power devices, and that while resonant techniques made switching more efficient, these approaches added new losses caused by the higher peak currents of the sinusoidal waveshape. An additional troublesome characteristic of resonant mode topologies is the fact that control is accomplished by varying the switching frequency, a situation which complicates the design of the input and output filters and causes the system designer concern over noise sensitivity.

A resonant-switch, phase-shifted PWM control algorithm addresses all these issues. First, pulse-width modulation infers square waveshapes for both current and voltage which transfers more power for a given current level than sine waves, and keeps the I^2R losses low. Secondly, resonant switching means that the high square-wave switching losses at each transition are alleviated by using

resonant techniques to switch the current at zero voltage. Finally, by controlling the phase relationship between two square-waves, a full range of control may be achieved with constant switching frequency. This technique is most easily implemented with a full bridge topology [66].

2.2.1. Phase-Shifted Zero Voltage Switching

In the phase-shifted Zero Voltage Switching technique, effects of the parasitic circuit elements are used advantageously to facilitate the resonant transitions as opposed to being dissipatively snubbed. This resonant tank functions to position zero voltage across the switching device prior to turn-on, eliminating any power loss due to the simultaneous overlap of switch current and voltage at each transition. High frequency converters operating from high voltage input sources stand to gain significant improvements in efficiency with this technique.

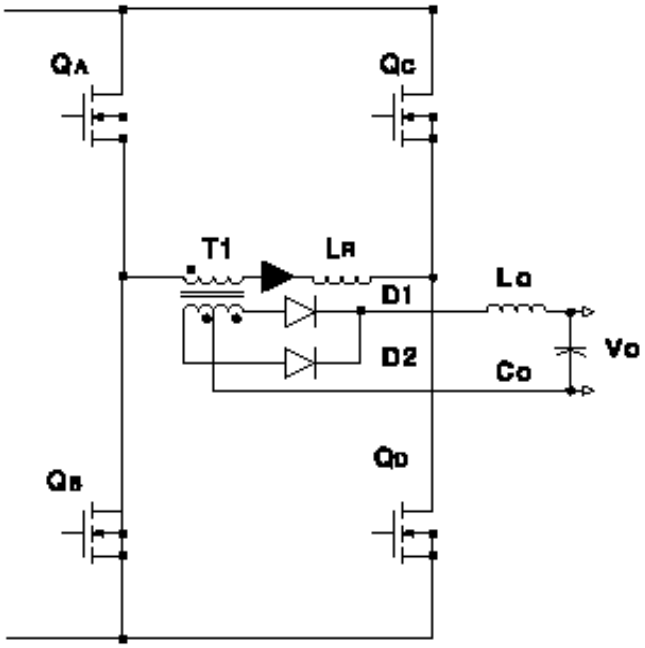


Fig.2.3. Full Bridge Topology

The diagonal bridge switches are driven together in a conventional full bridge converter (Fig.2.3), which alternately places the transformer primary across the input supply, Vin, for some period of time, t(on) as shown in Fig.2.4. Power is only transferred to the output section during the ON times of the switches, which corresponds to a specific duty cycle when operated at fixed frequency. Additionally, the complete range of required duty cycles is unique to the application, and can be estimated from the power supply input and output voltage specifications.

Rather than driving both of the diagonal full bridge switches together, a deliberate delay will be introduced between their turn-on commands with the Phase Shifted approach. This delay will be adjusted by the voltage loop of the control circuitry, and essentially results as a phase shift between the two drive signals. The effective duty cycle is controlled by varying the phase shift between the switch drive commands as shown in Fig.2.5.

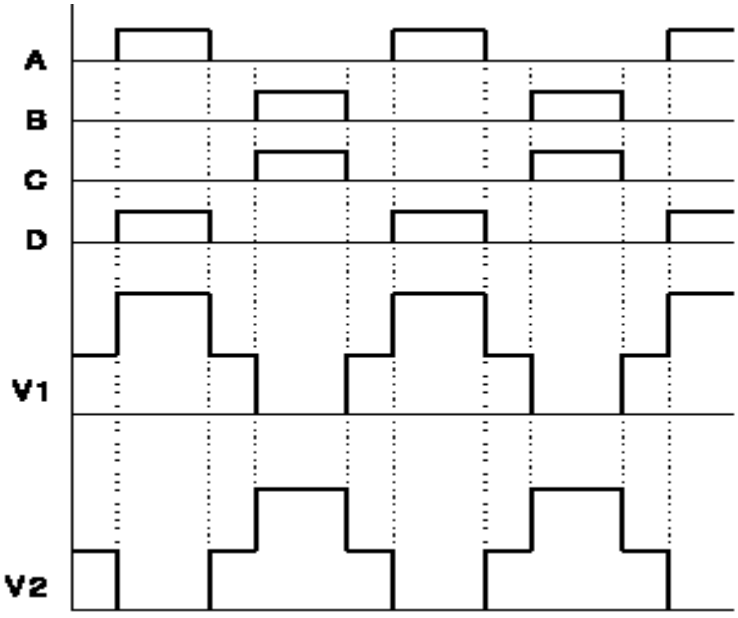


Fig.2.4. Conventional Full Bridge PWM Waveforms

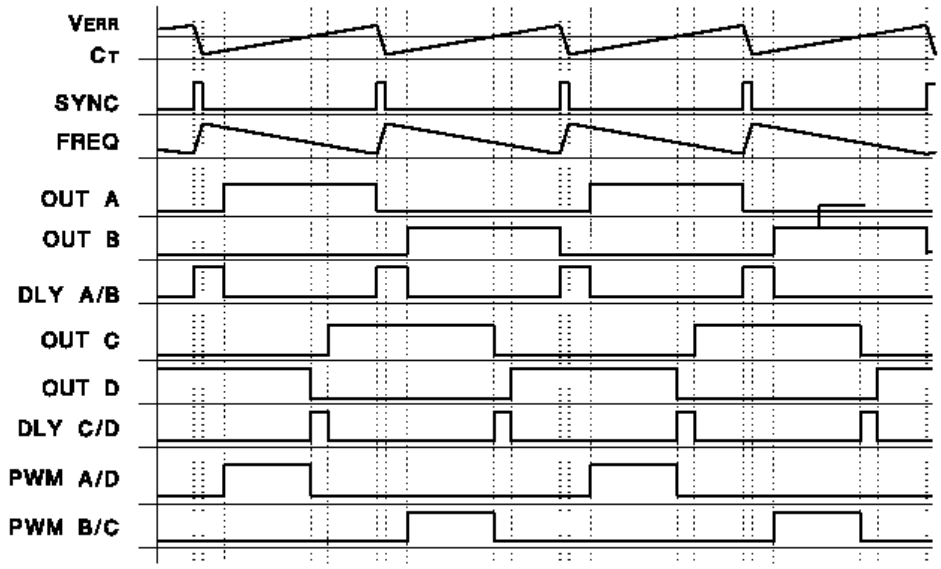


Fig.2.5. Phase Shifted PWM Control Waveforms

Unique to this phase shifted technique, two of the switches in series with the transformer can be ON, yet the applied voltage to the transformer is zero. These are not diagonal switches of the full bridge converter, but either the two upper or two lower switches. In this mode the transformer primary is essentially short circuited and clamped to the respective input rail. Primary current is maintained at its previous state since there is no voltage available for reset to take place. This deadband fills the void between the resonant transitions and power transfer portion of the conversion cycle. Switches can be held in this state for a certain period of time which corresponds to the required off time for that particular switching cycle. When the correct one of these switches is later turned off, the primary current flows into the switch output capacitance causing the switch drain voltage to resonate to the opposite input rail. This aligns the opposite switch of the particular bridge "leg" with zero voltage across it enabling zero voltage switching upon its turn ON [66].

Switches within the phase-shifted full bridge converter will be utilized differently than those of its non-resonant counterpart. Instrumental to this

technique is the use of the parasitic elements of the MOSFET switch's construction. The internal body diode and output capacitance (C_{oss}) of each device (in conjunction with the primary current) become the principal components used to accomplish the resonant transitions.

The circuit schematic of this technique is shown in Fig.2.6 including voltage and current designations. The basic circuit is comprised of four switches labelled Q_A through Q_D and is divided up into two "legs", the right and left hand legs. Each switch is shown shunted by its body diode (D_A through D_D) and parasitic output capacitance, (C_A through C_D). These have been identified separately to clarify the exact elements and current paths during the conversion interval.

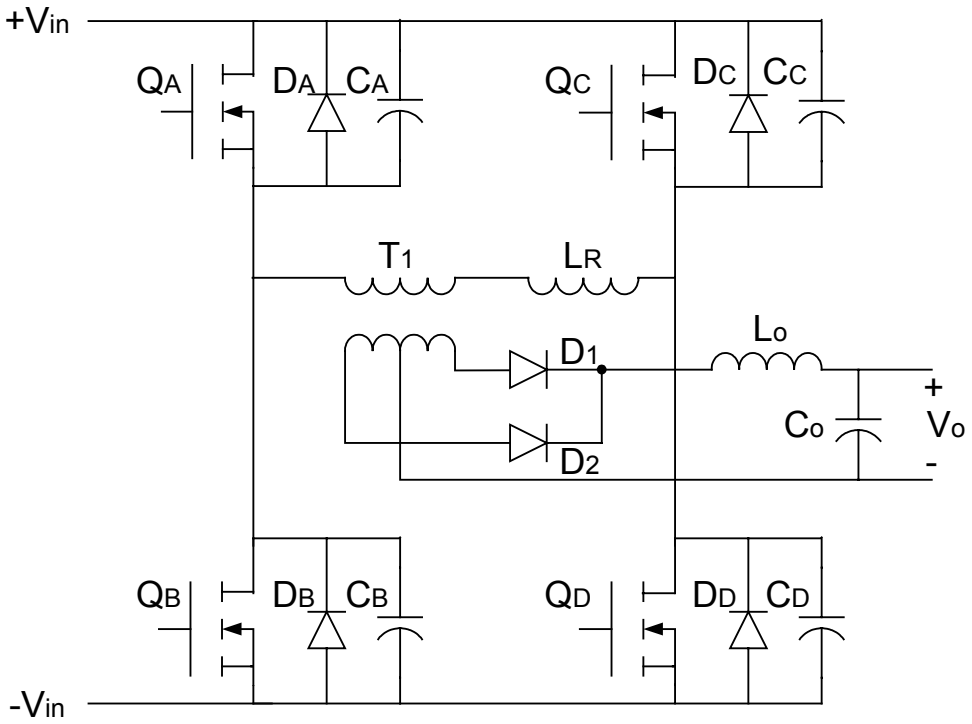


Fig.2.6. The circuit schematic for phase shift operation

The operation of the phase shifted ZVS full bridge converter is presented in Appendix B in detail.

2.2.2. System Controller

Today, the power equipment used in the telecommunication applications should be intelligent, and suitable to be connected to a remote supervision system. In this way, the maintenance costs decrease by a considerable amount. Therefore, in the designed and implemented system, the system controller is responsible not only for the control of DC/DC converter, but also for user interface, maintenance, and remote control and monitoring processes.

The system controller consists of six main modules (Fig. 2.7):

- **Analog Interface :** The Analog Interface module is responsible for converting the output voltage, output current and input voltage signal, which are inherently analog, to their digital counterpart. These signals are then processed by the System Controller for calculating the necessary duty cycle for the PWM Generator module. Moreover, these signals are also used by other modules for recording, and user interface purposes.

- **PWM Generator :** The PWM Generator module generates the necessary gate signals for the MOSFETs used in the full-bridge converter according to the duty cycle calculated by the system controller using the signals from the analog interface module.

- **Internal Communication :** The Internal Communication module provides communication with other converters. The output current and voltage information is exchanged between the converters through Internal Communication module for equal sharing of the load current among the parallel-connected converters, and for exchanging the settings.

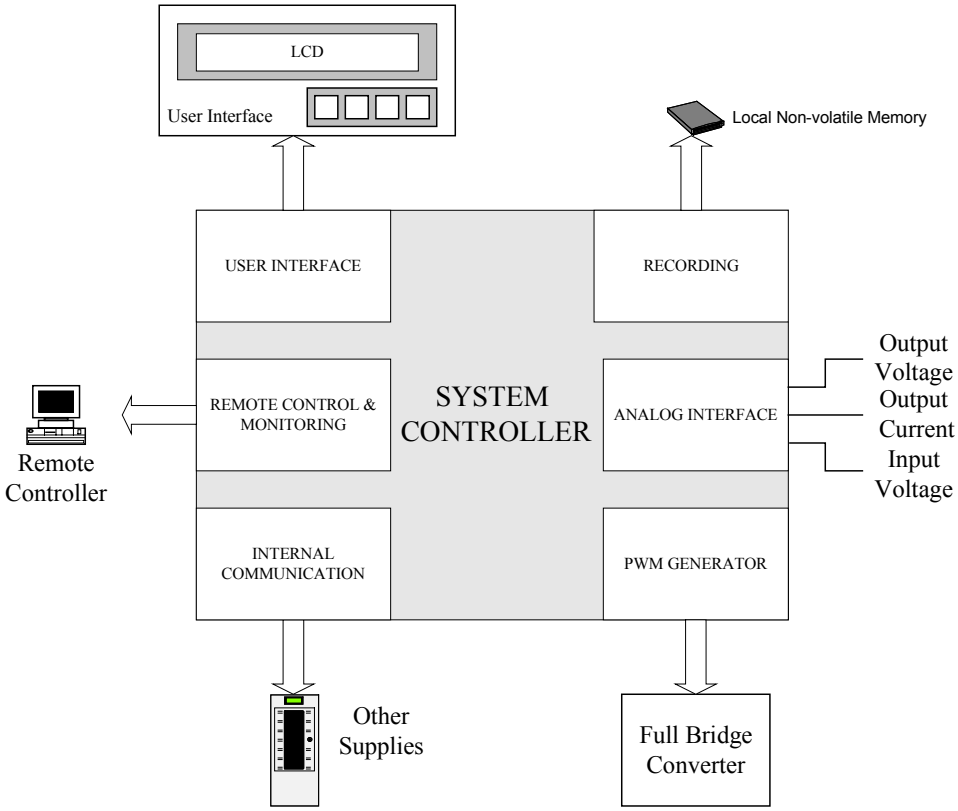


Fig.2.7. Block Diagram of the System Controller

- **User Interface :** The User Interface module provides the user to access the information about the converter condition and to enter settings through the LCD and buttons existing on the front panel of the converter.

- **Remote Control and Monitoring :** The converter can be controlled and monitored from a remote site by using Remote Control and Monitoring module.

- **Recording :** The Recording Module is responsible from logging of some parameters like the output current, voltage, etc., and occurred alarms for maintenance purposes.

In this work, the implementation of the System Controller is carried out in two phases: The System Controller is first implemented by using two 8-bit low cost microcontrollers, and an external PWM generator IC, and then by using a high speed DSP, as explained in detail in Chapters III and IV.

CHAPTER III

PHASE I : DESIGN AND IMPLEMENTATION WITH DUAL MICROCONTROLLERS

In this section, the design and implementation of a digital controller for universal telecommunication power supplies, based on parallel-operated, dual, low-cost, 8-bit microcontrollers, are presented (Fig.3.1). One of the microcontrollers is employed for user interface purposes, such as long term records, display and alarm facilities, which are inherently slow processes. The fast processing speed required by output voltage setting, current limit, and load current sharing however, is fulfilled by the second microcontroller, which adjusts the output voltages of modules.

The proposed dual-processor based digital controller provides extended operating output voltage range (0-70V) at universal input voltage range, user programmable current limit setting (adjustable between 0–40A), serial-communication based, active load current sharing between modules with automatic master/slave selection property, and de-rating at low input voltages without extra hardware requirement. The overload and output short-circuit protection features are also software-controlled.

The proposed controller is successfully tested in the field on six parallel operating, 1.8 kW, 0-70V telecommunication power supplies, each incorporating a phase-shifted, full-bridge DC/DC converter operated from a preregulated bus. Experimental results on digitally-controlled load current sharing, current limiting, derating, and output short-circuit protection are presented [67,68].

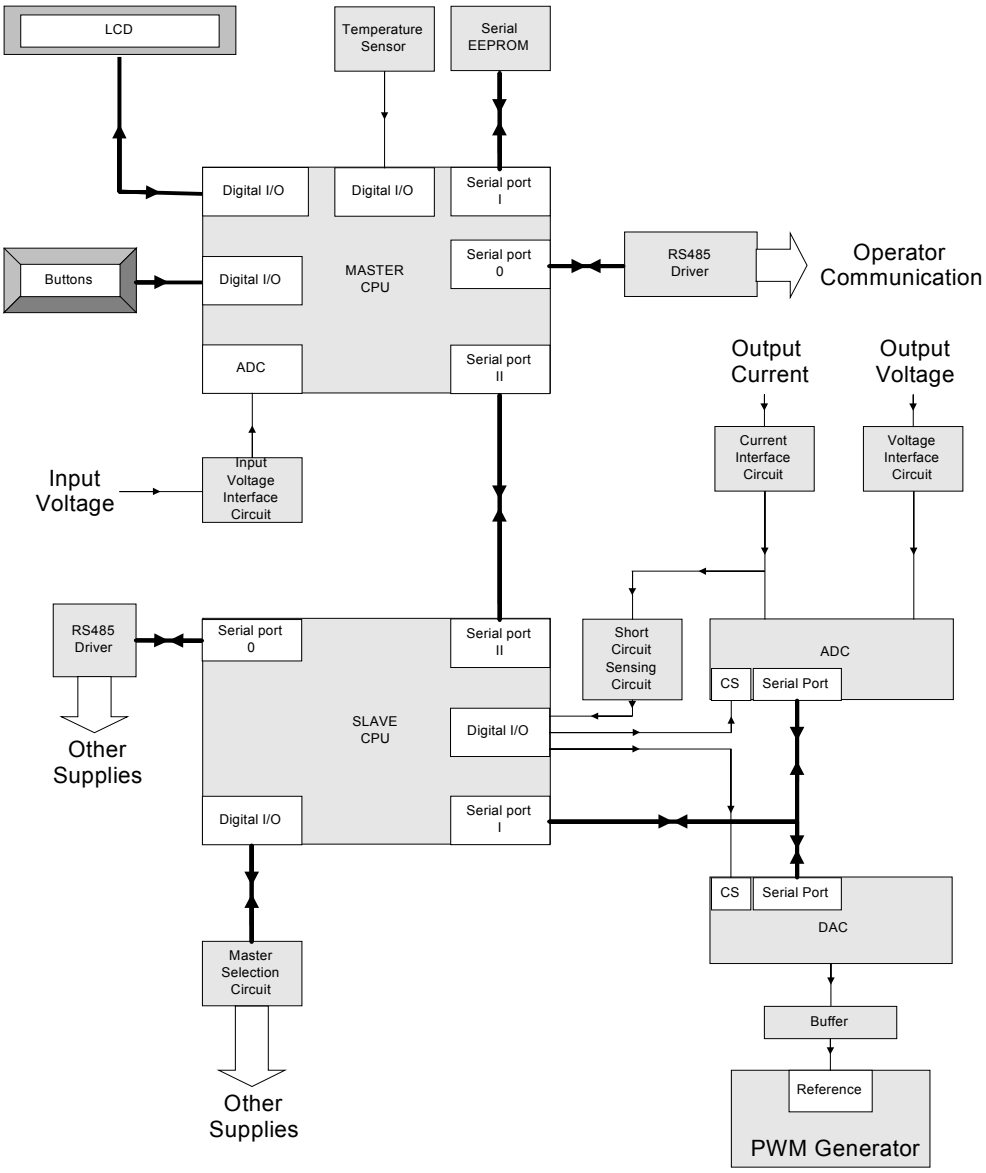


Fig.3.1. General hardware block diagram of the dual-processor based digital control system

3.1. SYSTEM DESCRIPTION

The general hardware block diagram of the parallel operated, dual-processor based digital control system of the power supply modules is given in Fig.3.2. The universal telecommunication power supply control is based on two 8-bit microcontrollers, NEC uPD78F0058YGC, with 64 kB of internal flash memory,

1 kB of internal random access memory, 8 channel, 8-bit analog-to-digital (A/D) converter, 3 serial communication ports (one of which is 3-wire/UART mode selectable), one 16-bit timer, two 8-bit timers, and 69 I/O ports [69].

One of the microcontrollers (MCU1) is employed for user interface purposes such as long term records, display, and alarm facilities, which are inherently slow processes. It also includes the functions for remote control. The fast processing speed required by output voltage setting, current limit, and load current sharing however is fulfilled by the second microcontroller (MCU2), which adjusts the output voltage reference of the PWM generator in the DC/DC converter, according to the set voltage information coming from MCU1 through the serial interface. The output voltage of the module is user adjustable between 0-70V with 0.1V resolution.

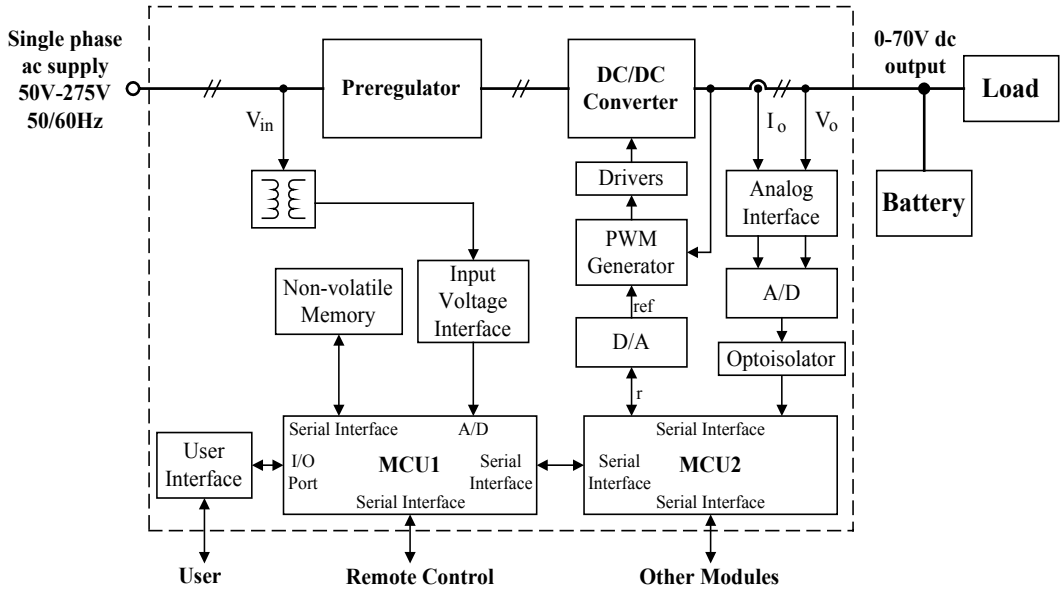


Fig.3.2. Hardware block diagram of each digitally controlled module

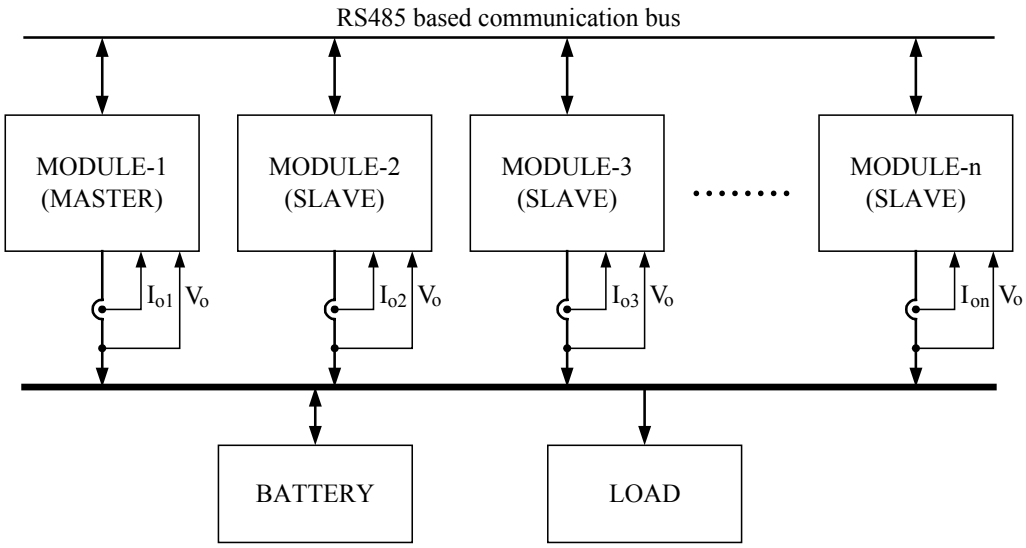


Fig.3.3. System of parallel-connected modules with digitally-controlled load current sharing

The digital controller employed manages the current limit, current sharing, derating, and the steady-state voltage regulation. Transient response of the DC/DC converter operating at a switching frequency of 100 kHz is controlled by a simple, analog voltage feedback circuit employing UC3875 integrated circuit. Among the functions of the digital controller, only derating is accomplished by MCU1. To implement this function, MCU1 reads the input voltage through the built-in A/D converter. On the other hand, an external 12-bit A/D converter is used in the output current, and output voltage measurements, for sufficient accuracy in performing current limit, and current sharing functions. Furthermore, to control the reference input of UC3875, a 16-bit external digital-to-analog (D/A) converter is employed in the control system. The digitally-controlled power supply modules are operated in parallel via a serial data bus (RS485) used for communication between the modules (Fig.3.3). The current sharing process is based on master/slave operation of the modules. The master module is selected among the active modules when the system is switched-on. In case of failure of the master module, the other modules select a new master among themselves, and ignore the defective module, for redundant operation.

3.2. DIGITAL CONTROLLER DESIGN

The control system consists of four loops:

- Derating Loop : The derating loop is responsible for calculating applicable current limit. According to the input voltage level and the power limit of the preregulator, it calculates the maximum output current that the module can supply. The lowest of the calculated output current limit and the set current limit is selected as the applicable current limit.
- Current Limit Loop : The current limit loop is responsible for preventing the output current level to exceed the determined current limit level. In case the output current level exceed the set current limit, it decreases the output voltage of the module by using a PI controller.
- Current Sharing Loop : Current sharing is responsible for equal sharing of the total load current among the parallel operated modules. One of the modules is selected as master among the active modules and this modules collects the output current information from the remaining modules. With this information, it calculates the arithmetic mean of the output current levels and broadcast the calculated mean current to other modules. Each module tries to keep the output current level at the mean current level by adjusting their output voltage with a PI controller.
- Voltage Regulation Loop : Voltage regulation loop is responsible to prevent output voltage drifts due to environmental condition.

The input/output scheme of the control loops, and the interaction among them are given in Fig.3.4. Derating loop's inputs are the current limit set value ($I_{lim\ set}$), output voltage setting (V_{set}), and input voltage (V_{in}). This loop calculates the applicable current limit (I_{lim}), according to the power limit of the pre-regulator, and outputs this information to the current limit loop. The output current (I_o), I_{lim} from derating loop, and calculated reference value r_3 from current sharing loop

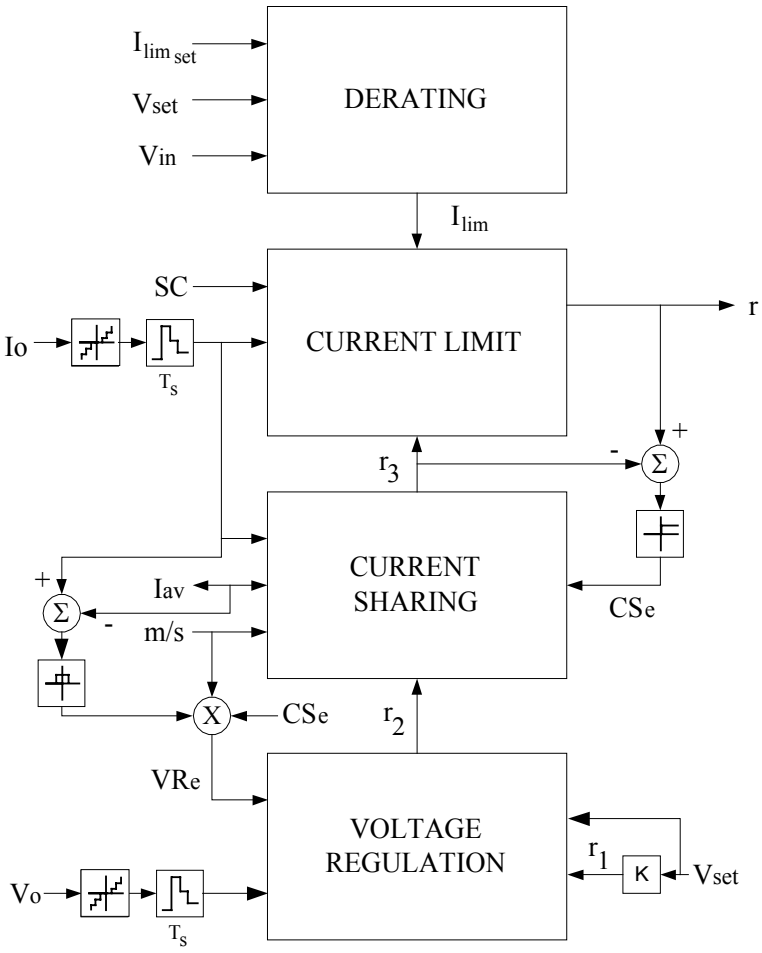


Fig.3.4. Block diagram of the digital controller

constitute the inputs of the current limit loop. The current limit loop produces the reference r, that will be applied to D/A converter, in order to prevent the output current of the module from exceeding I_{lim}. The inputs of the current sharing loop are I_o, master/slave selection signal (m/s), current sharing enable (CS_e) signal, and calculated reference from voltage regulation loop (r_2). The average current of modules (I_{av}) is an input for a slave module, whereas it is an output for a master module. The function of current sharing loop, for a slave module, is to produce the reference voltage (r_3) for the current limit loop such that all modules share the output current equally, and for a master module, to calculate the average current for slave modules. Voltage regulation loop keeps the output voltage fixed at the set value, against drifts due to temperature variations, ageing

etc, by using V_{set}, the output voltage (V_o), voltage regulation enable signal (VR_e), and the reference r_1. r_1 is obtained by multiplying V_{set} with a constant K in order to convert the set voltage to the corresponding D/A setting.

The current limit loop, current sharing loop, and the voltage regulation loop are mutually exclusive loops, i.e. only one of them can be active at any time. In the selection of the active loop, priority scheduling is used. Among the control loops, the current limit has the highest priority. When output current exceeds the applicable limit, current limit loop is activated. In this case, r will be smaller than r_3. It is clear from Fig.3 that, the difference $r - r_3$ will be negative. The sign operator therefore produces a 0 as CS_e signal, which prevents the current sharing loop's action.

When CS_e signal is 0, current sharing loop keeps r_3 unchanged. Similarly, the result of the multiplication operation, which produces VR_e will also be 0, as CS_e is 0. Therefore, voltage regulation loop also keeps r_2 unchanged.

For slave modules, current sharing loop has the lowest priority, and voltage regulation loop is inactivated. The m/s signal is 1 if the module is master, and 0 otherwise. The VR_e signal will be 0 for a slave module, due to the m/s signal being 0. When current limit is not active, r will be equal to r_3 and CS_e will be 1, thus allowing the current sharing loop to be active. For master module, voltage regulation loop has the lowest priority, and current sharing loop only calculates I_{av}.

In this case, the current sharing loop communicates with other modules, via RS485 serial data bus, in order to get their output current values. Calculating I_{av}, it sends this information to slave modules. The voltage regulation loop acts when the master module is not in current limit (CS_e=1), and the output current lies within the range $I_{av} \pm \Delta I$.

3.2.1. Current Sharing Loop

The current sharing loop provides equal sharing of total load current among modules. The function of the loop differs according to the module status. If the module is master, the function of the loop is to calculate the average current, keeping its output voltage constant. On the other hand, if the module is a slave one, it adjusts its output voltage so as to supply the average current determined by the master module. By this way, the master module determines the voltage level of the whole system, and the slave ones provide the current sharing. The block diagram of the current sharing loop is given in Fig.3.5. The current sharing loop is enabled when the current limit loop is disabled, with CS_e signal equal to 1. The current sharing loop consists of two mutually exclusive inner loops: the master_loop, and the slave_loop. The m/s signal determines the active loop.

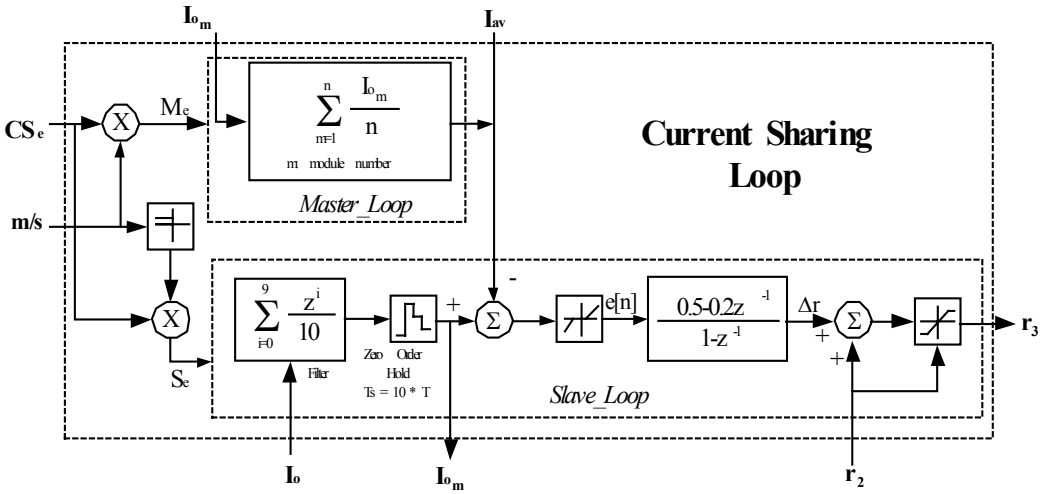


Fig.3.5. Controller block diagram for current sharing loop

When the system is master, m/s signal is 1, which results in master enable (Me) signal to be 1 (CSe=1), and slave enable (Se) signal to be 0. As a result, the master_loop is activated. In this loop, the module gets the slave modules' current values (Io_m) through the RS485 based serial link, takes their average, and

broadcasts the average current (I_{av}) to the slave modules. In the slave module, m/s signal will be 0, causing the slave loop to be activated, and the master loop to be inactivated. In the slave loop, the output current is read from A/D converter with 0.1A resolution, and at a 10 kHz sampling rate.

A simple digital filter taking the average of the last 10 samples is used to filter out the output current signal. This value is also sent to the master module for I_{av} calculation. Error is calculated from the difference between filtered output current, and I_{av}.

In the system, the error is permitted to lie in the range I_{av}±0.5A. When the error is out of this range, PI type of control in discrete time domain acts, with K_p = 0.5, and K_i = 0.3, as expressed in Eq. 3.1.

$$\Delta r[n] = \Delta r[n-1] + 0.5e[n] - 0.2e[n-1] \tag{3.1}$$

The corresponding z-domain transfer function is:

$$G(z) = \frac{\Delta r(z)}{e(z)} = \frac{0.5 - 0.2z^{-1}}{1 - z^{-1}} \tag{3.2}$$

The output of the current sharing loop, which constitutes the reference that will be applied to current limit loop is then calculated from Eq.3.3.

$$r_3[n] = r_2[n] + \Delta r[n] \qquad \begin{cases} r_3[n] & r_2 - 2V < r_3 < r_2 + 2V \\ r_2 + 2V & r_3 > r_2 + 2V \\ r_2 - 2V & r_3 < r_2 - 2V \end{cases} \tag{3.3}$$

As mentioned in Section 3.2, output voltage of the system is determined by the master module, but in case of failure of the master module, output voltage can

rise or drop. To prevent the slave modules from following the voltage of a defective master module, r_3 is permitted to vary in the range $r_2 \pm \Delta x$, where Δx is the reference which corresponds to 2V deviation at the module output. The calculated r_3 signal is then applied to the current limit loop.

3.2.2. Current Limit Loop

The block diagram of the current limit loop is given in Fig.3.6. The function of current limit loop is to keep the output current of the module below a predefined adjustable value. The current limit loop is enabled (CL_{en}) when the output current is above the current limit value, or the reference (r) is smaller than the reference determined by the paralleling loop (r_3), which corresponds to the case of recovery from an overload. Being active, the current limit loop reads the output current from A/D converter with 0.1A resolution, and at 10 kHz sampling rate. The current limit value is subtracted from filtered output current to calculate the error, which is then compared with a dead-band. If the error is out of this dead-band, it is applied to the transfer function given in Eq.3.2. This is the same PI controller in discrete time as the one used in the current sharing loop. Sum of Δr and r_3 is then applied to the reference of PWM generator (UC3875), after being converted to an analog signal through the D/A converter. The current limit loop is kept relatively slow to prevent the oscillations in multi-module operation, or in case of battery back-up. Hence, this loop is not sufficient to protect the system against short circuits, and heavy overloads. Therefore, in the control system, a hardware interrupt (SC) is generated when the output current exceeds the maximum value of ≈ 45 A, in order to protect the system against such heavy overloads, and short-circuits at the output. In that case, the flip flop (FF) in Fig.3.6 will be cleared causing the reference to be zero, thus reducing the output voltage of the module to zero. The current limit loop will then increase the output voltage so as to rise the output current to current limit value. When the output voltage reaches the set value, and the output current falls below current

limit value, FF will be set, and reference from current sharing loop (r_3) is transferred to the reference (r).

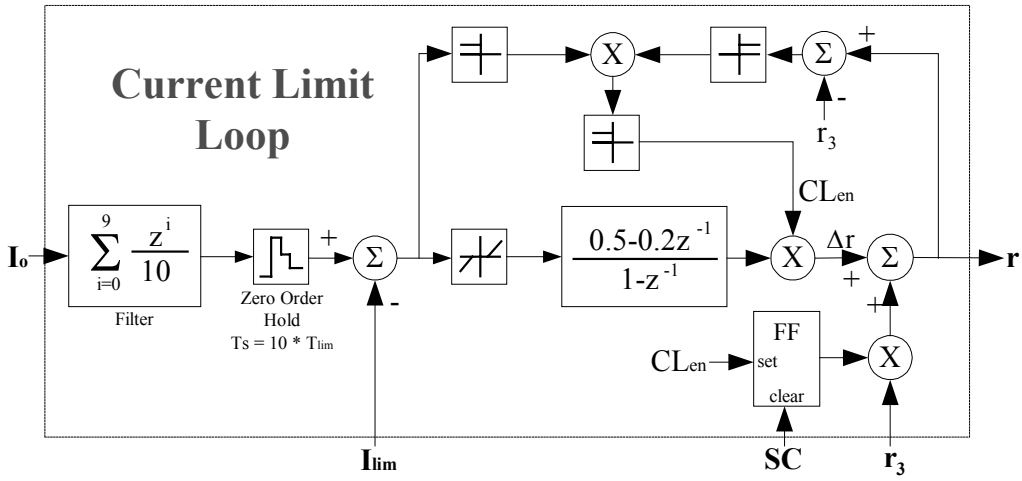


Fig.3.6. Block diagram of current limit loop

3.2.3. Derating Loop

Derating loop is the control loop by which the module self protects against input voltage drops. This is achieved by output power limitation (derating). The block diagram of this loop is given in Fig.3.7. In derating loop, the power limit of the pre-regulator obtained experimentally is used as a basis. The corresponding power limit vs input voltage characteristic is given in Fig.3.8, by the dotted line. The non-linear power limit curve is then piecewise linearized as shown in Fig.3.8 by a solid line, below the preregulator characteristic. The power limit (P_{lim}) equation used is given in Eq.3.4. The maximum current limit that can be applied at a given input voltage is then calculated by dividing P_{lim} to the output set voltage (V_{set}).

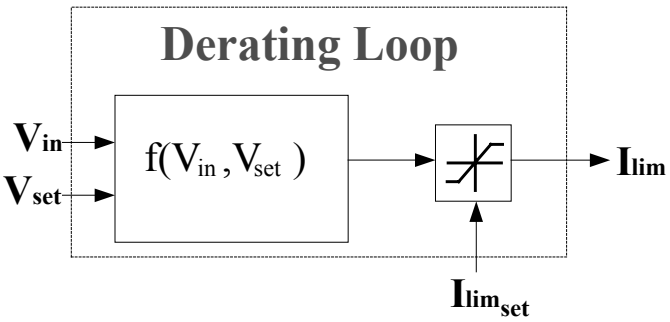


Fig.3.7. Block diagram of derating loop

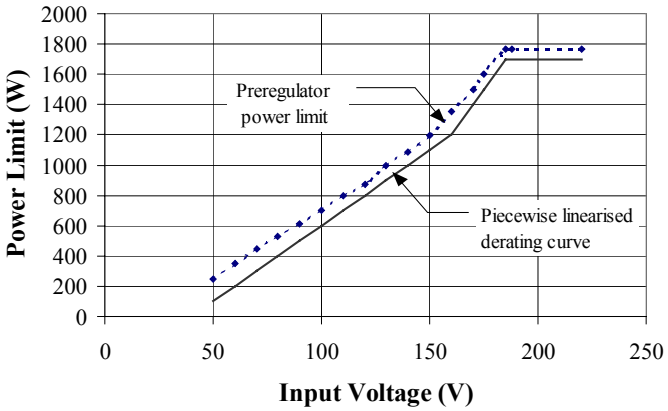


Fig.3.8. Derating curve against input voltage

$$P_{lim} = \begin{cases} 1700W & V_{in} \geq 185V \\ 20.(V_{in} - 100) & V_{in} \geq 160V \quad \text{and} \quad V_{in} < 185V \\ 10.(V_{in} - 40) & V_{in} \geq 50V \quad \text{and} \quad V_{in} < 160V \\ 0 & V_{in} < 50V \end{cases} \tag{3.4}$$

The maximum current limit value calculated by the function given in Eq.3.5 constitutes the threshold for the saturation block shown in the block diagram in Fig.3.7.

$$I_{lim_{max}} = f(V_{in}, V_{set}) = \frac{P_{lim}}{V_{set}} \tag{3.5}$$

3.2.4. Voltage Regulation Loop

Ageing, and environmental conditions, such as temperature, humidity, etc. affect the analog feedback of the system, which causes the output voltage of the module to drift. To minimise this drift, voltage regulation loop, whose block diagram is given in Fig.3.9 is included in the control system of the module. The A/D converter of the system has very low temperature drift. Therefore, the reading of the A/D can be taken as the reference for the voltage regulation loop. The output voltage read from the A/D is subtracted from the set voltage. A small difference, which is ±99 mV, is permitted. In case the difference is out of this range, the voltage regulation loop decreases or increases the reference in steps to keep the output voltage at the set value, and sends this reference to the current sharing loop.

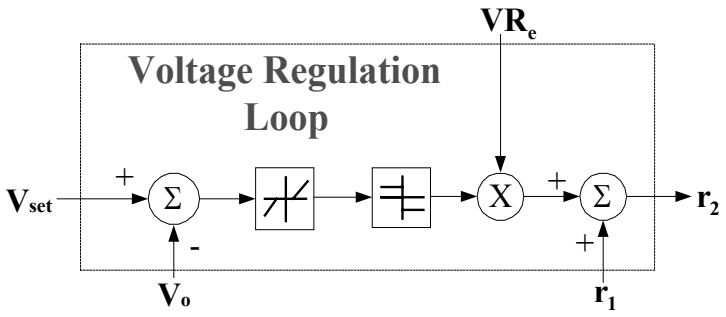


Fig.3.9. Voltage regulation loop

3.3. CONTROLLER IMPLEMENTATION

The digital controller described in Section 3.2 is implemented by software. The functions except de-rating are managed by the software of MCU2. The flowcharts of the softwares of both MCU1 and MCU2, and the communication between them are given in Fig.3.10. MCU1 is mainly responsible for user interface, remote control, alarm, and recording functions. MCU1 also determines

the applicable current limit value for MCU2. It reads the input voltage, and by using the predefined power limit curve, voltage setting of the module, and the current limit set by the user, it calculates the current limit of the module, and sends it to MCU2. Moreover, MCU1 sends the voltage set information supplied by the user to MCU2, while getting the output voltage and current values from MCU2 for display, alarm, and recording purposes.

The software running on MCU2 implements the main functions of the digital controller. When the module is turned-on, MCU2 initialises its register and memory. Then, it communicates with other modules' MCU2 to select the master module. Determining the master module it sets the m/s flag accordingly. Before enabling the DC/DC converter, it first checks the output voltage to decide on the starting method, direct-on or soft-starting. If the output voltage is less then 2V, which indicates that there is no battery back-up, or another parallel-operating power supply in the system, it directly applies the reference voltage level corresponding to the set voltage coming from MCU1. Otherwise, it applies the soft-start algorithm, in which the output voltage is adjusted 0.5V below the measured output voltage, and then increased using the current limit algorithm until the set voltage is reached, or the supplied current has reached the current limit value.

Enabling the DC/DC converter, MCU2 enters its main control loop. It takes the output voltage and current samples. Then, it checks Current Limit Flag (CL), which indicates that the module is limiting the output current, if set. If CL is set, MCU2 directly jumps to the subroutine that implements the current limit function as stated in the digital controller design section for the current sample of output current. On the other hand, if CL is cleared, it checks whether the output current is above the limit value or not. In case the output current is higher than the current limit set value, it sets CL flag, and implements the current limit loop.

After processing the current sample in current limit loop, it compares the reference with the reference corresponding to the set voltage to terminate the current limit loop. If the reference is above the set value, which indicates the termination of the current limit, MCU2 clears CL, and passes the control to the main loop to manage the next function, which is current sharing. In case of short circuit, a hardware interrupt is activated in MCU2. In the interrupt handling subroutine, MCU2 clears the reference to 0, and passes the control to current limit loop. Upon determining that the module is not in current limit condition, MCU2 checks m/s flag to decide upon the function that it will implement in current sharing loop. If the module is master, it gathers the output current values of the other modules, and calculates and broadcasts the average current. On the other hand, for a slave module, MCU2 processes the current sample through the current sharing loop to equalise the output current to the average current, as explained in Section 3.2. The slave module then takes another sample, and accomplishes the same functions, continuously. After calculating the average current, the master module's MCU2 compares its own output current with the average current. In case they are equal, which reveals that the modules share the total load current equally, it enables the voltage regulation loop, in which the output voltage drifts caused by environmental effects are compensated. The master module then takes another sample, and implements the main control loop. The implemented control stage PCB is given in Fig. 3.11.

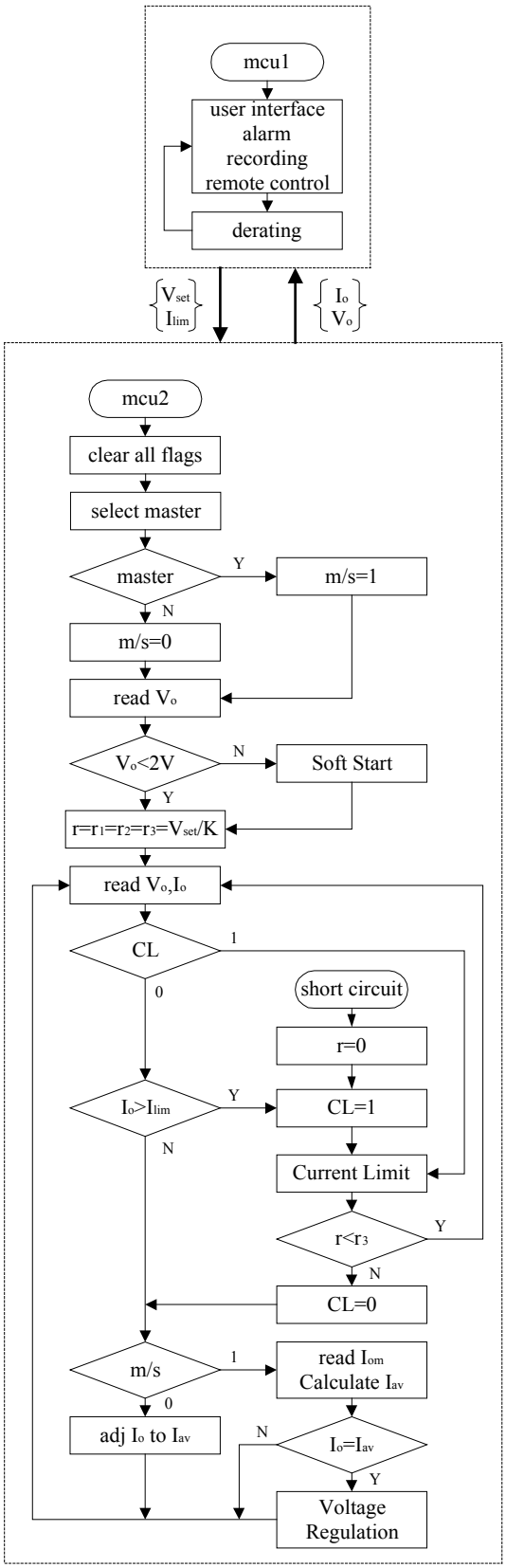
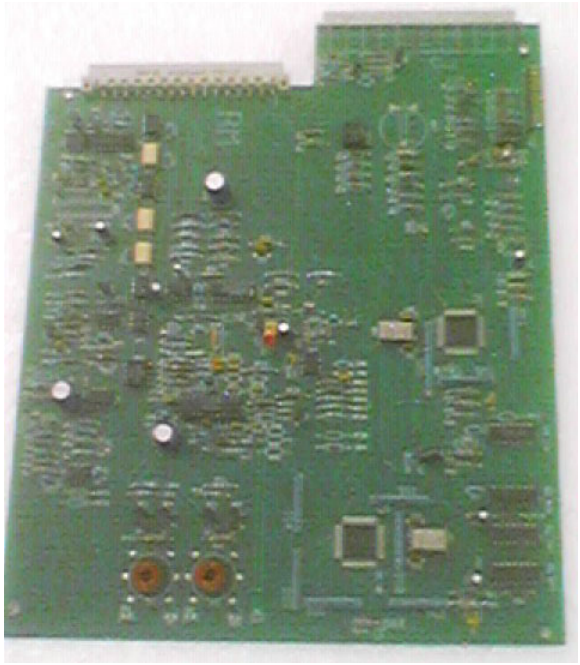
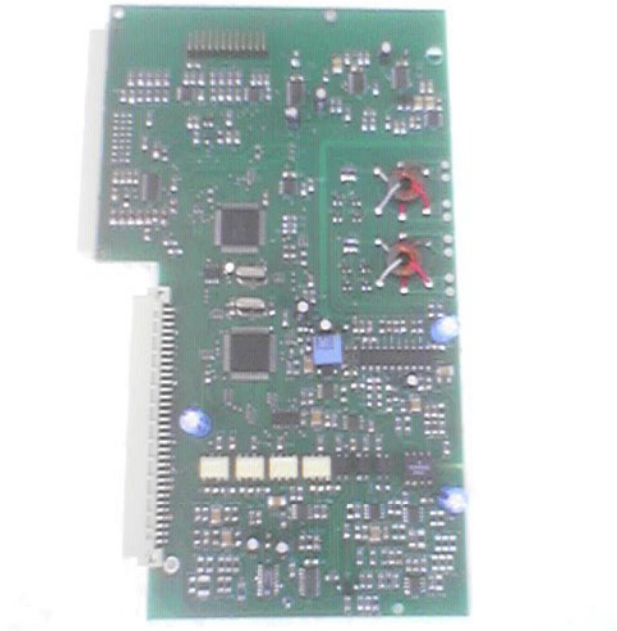

mcu1
user interface
alarm
recording
remote control
derating
Vset
Ilim
Io
Vo
mcu2
clear all flags
select master
master
Y
m/s=1
N
m/s=0
read Vo
Vo<2V
N
Soft Start
Y
r=r1=r2=r3=Vset/K
read Vo,Io
CL
1
0
short circuit
r=0
Io>Ilim
Y
CL=1
N
Current Limit
r<r3
Y
N
CL=0
m/s
1
read Iom
Calculate Iav
0
adj Io to Iav
N
Io=Iav
Y
Voltage
Regulation

Fig.3.10. Flowchart of the digital controller



(a) First generation of the implemented control stage PCB



(b) Second generation of the implemented control stage PCB using SMD technology

Fig.3.11. The implemented control stage PCB

3.4. REMOTE CONTROL

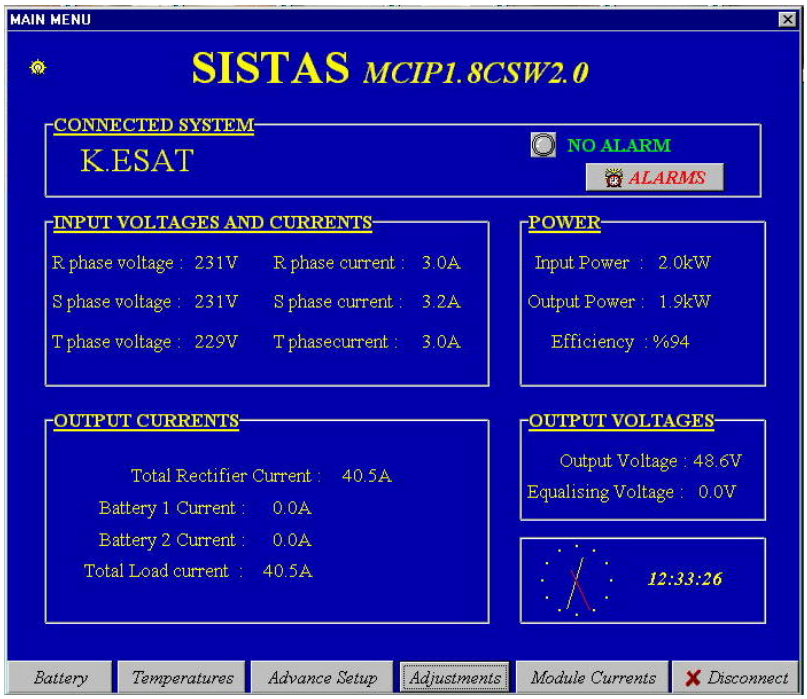
The telecommunication system spreads over a very large area to provide communication services to individual users. As a result, the telecommunication equipment, and the systems powering this equipment are distributed in a large geographical area. On the other hand, communication is a service that should be delivered continuously, which implies that the downtime for the telecom equipment and the telecom power systems should be minimised. These two facts creates the need for remote monitoring and control of not only the telecommunication equipment but also the telecom power systems, which are always at the top of the failed component list. Today the feature of remote controllability is one of the major property expected from the telecommunication power supplies. This feature provides the monitoring of the telecom power systems from a central office and getting information about the failures in a short time, which decreases the downtime of the general system. Moreover, this feature also decreases the maintenance costs.

The designed system can be monitored and controlled remotely. Each power supply system is communicating with the remote control unit via a serial bus based on RS485 standard. The power supplies inform the remote control unit about the state of the system and the alarms activated, and get settings from it. The remote control unit is connected to the central office with a dial up modem. This connection is an on demand type connection. The connection can be setup by the user or by the system. The user connects to the system whenever he wants to check the system state. On the other hand, the system sets up the connection whenever there is an active alarm, and records the alarm to the database located on the central office.

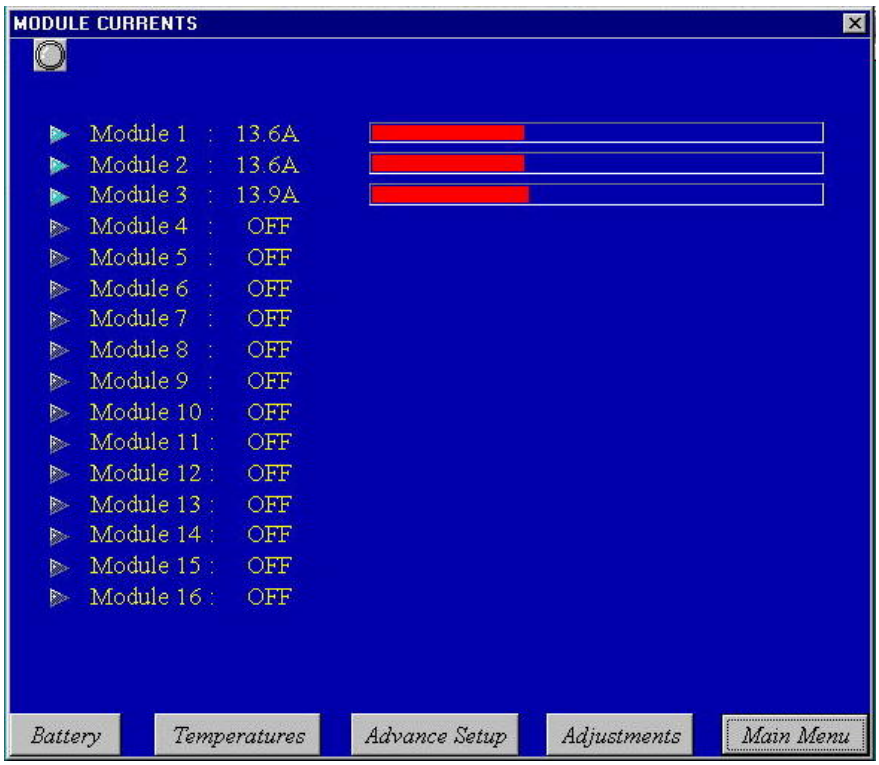
Implemented systems with remote control unit are shown in Fig.3.12.

Fig 3.12. Systems with Remote Control Unit

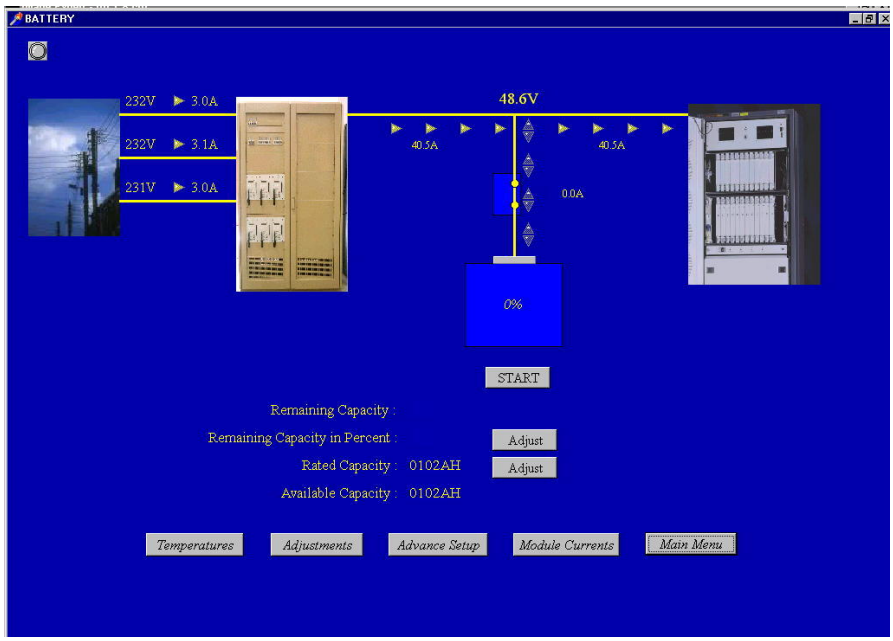
Some screenshots from the software located in the central office can be found in Fig.3.13.



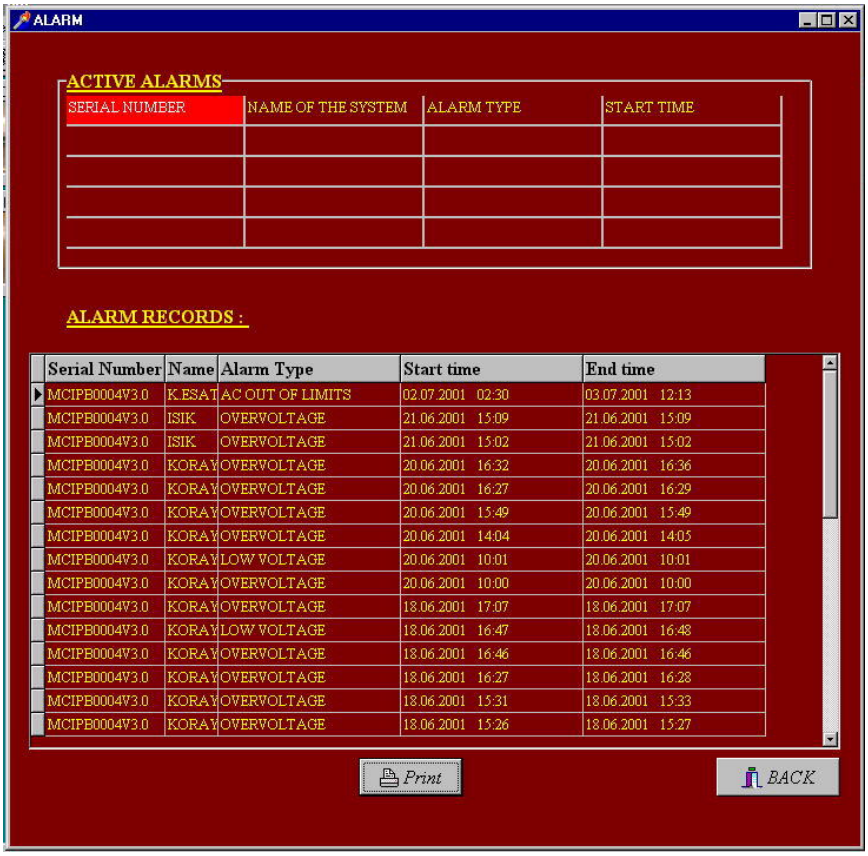
(a) Main Menu



(b)Module Currents



(c) System Menu



(d) Alarm Menu

Fig.3.13. Screenshots from Central Office Software

3.5. RESULTS

The implemented power supply system is given in Fig. 3.14 and Fig 3.15. The proposed digital controller has been implemented on six universal, telecommunication power supply modules operating in parallel, as shown in Fig.3.16. Experimental results of software-controlled load current sharing among modules, current limiting, output short-circuit protection feature, and derating are given (Figs.3.17-3.20).

Fig.3.14. The implemented power supply module

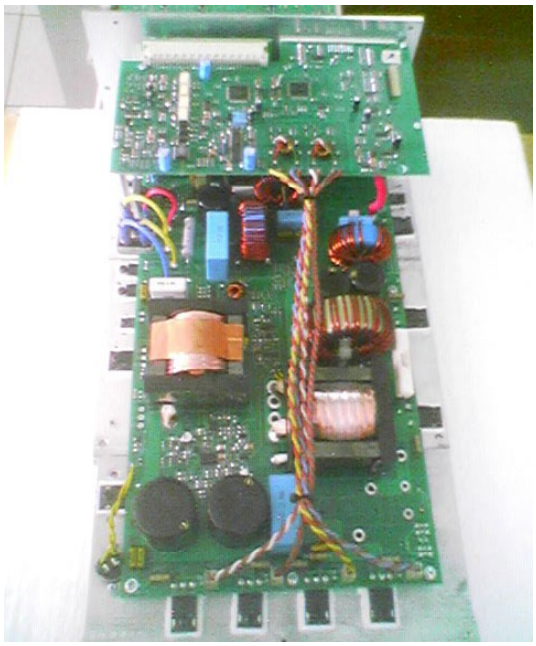
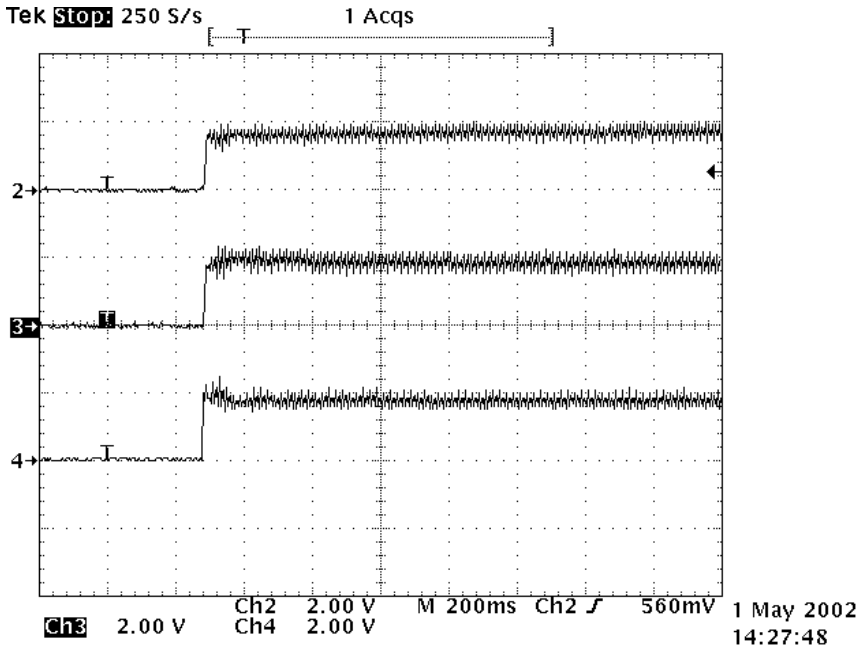


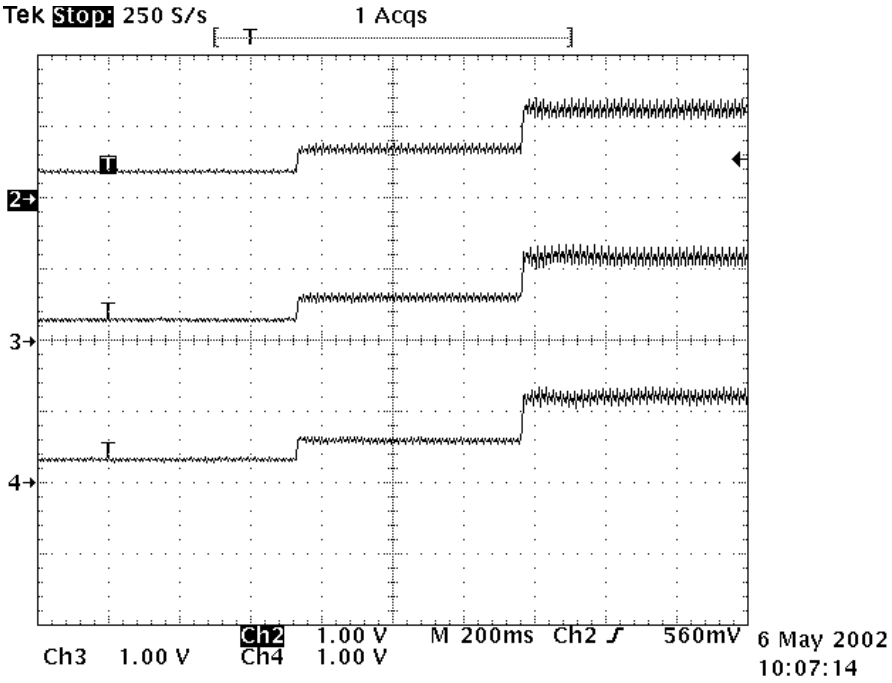
Fig.3.15. Inside view of the implemented system

Serial-communication based, active load current sharing in multi-module operation is illustrated in Fig.3.17, for three parallel operating modules. Current sharing loop activity at start-up of modules is shown in Fig.3.17.a. To observe the current sharing loop response under varying load conditions, the three modules' currents are monitored while the load current is increased in steps from 9A to 18A, and then to 36A. It is seen from Fig.3.17.b that, the total load current is equally shared between modules, and the transient response of module currents is quite satisfactory.

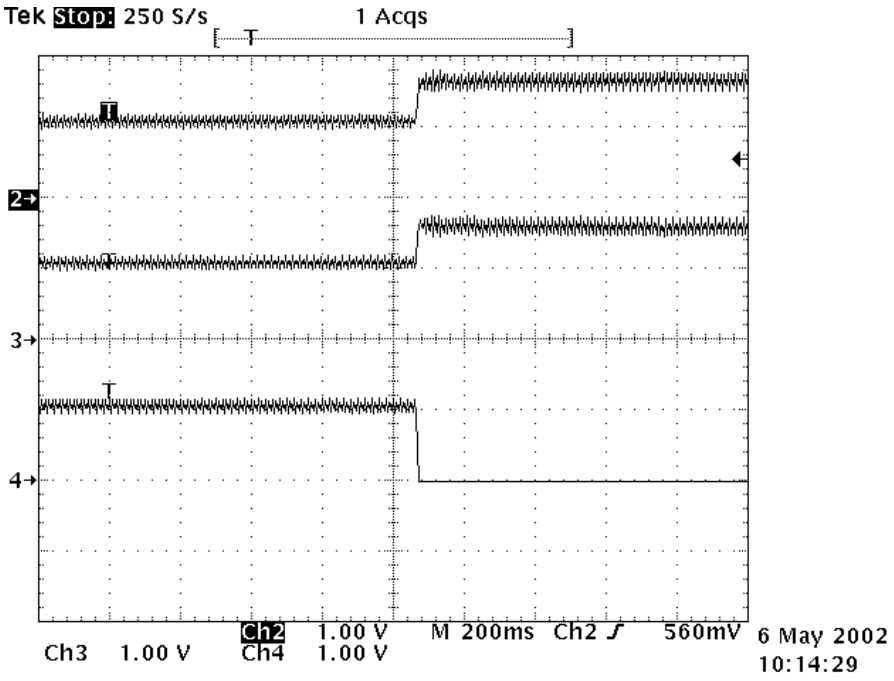
Fig.3.16. Six digitally-controlled, universal telecommunication power supplies in parallel



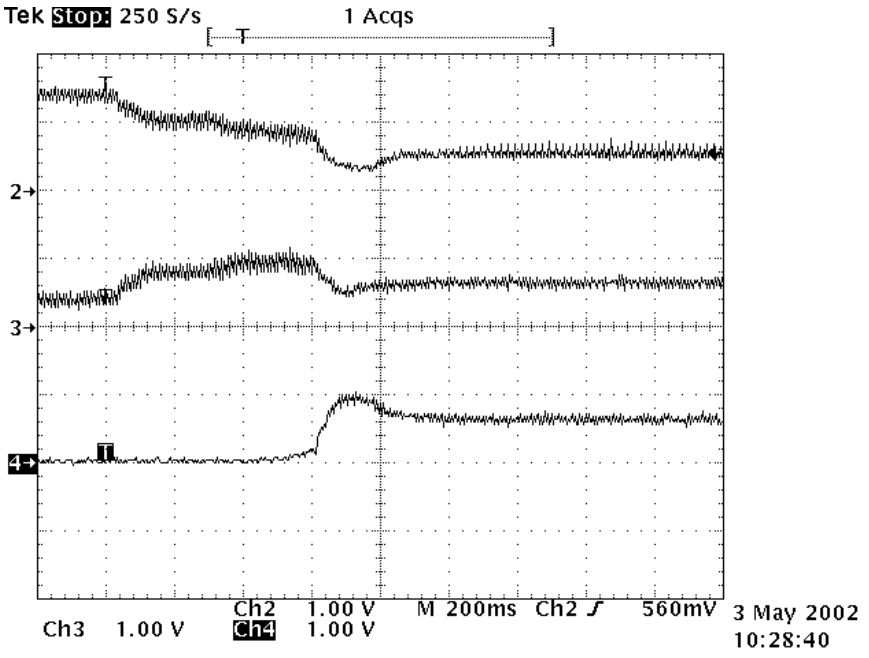
(a) Current sharing of modules at start-up



(b)Current sharing under varying load conditions



(c) Redundant operation of modules



(d) Master / slave operation of modules

Fig.3.17. Digitally controlled load current sharing between parallel operated modules (Ch.2, Ch.3, Ch.4: module currents, 10 A/div)

Redundant operation of modules is shown in Fig.3.17.c, where one of the three parallel operating modules is shut-down while they were carrying 30A of load current. Note that, the remaining two modules continue to share the load current equally. Finally, to illustrate the digitally-controlled master/slave operation, the response of output currents of modules for initially disconnected, and then connected communication bus connectors are monitored as given in Fig.3.17.d. Initially, output currents of modules are not equally distributed due to non identical cabling and components, and small differences in output voltages of low output impedance modules. At t=200 ms, the current share bus connectors are plugged-in manually. Due to slight differences between contact instants of connectors, two of the modules are connected to the communication bus first, and then the third module is connected with a time delay of ≈ 600ms. With RS485 communication bus being active, the load current is shared equally between modules, with less than a few percent accuracy.

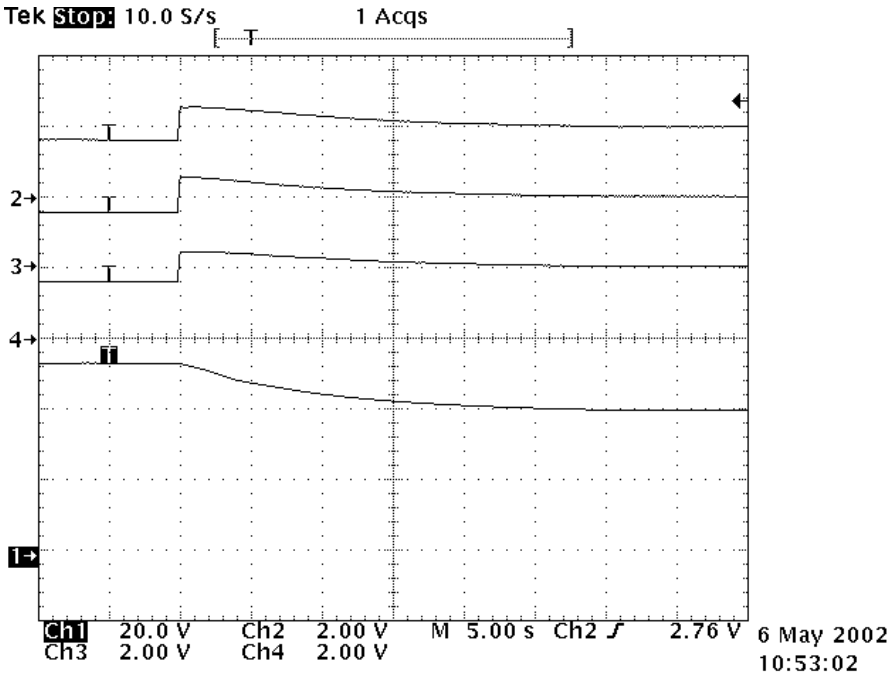
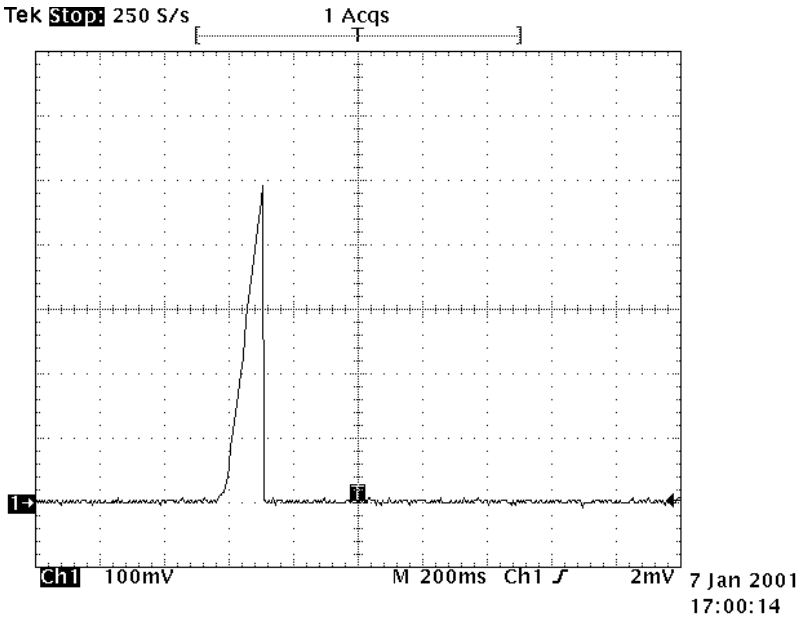


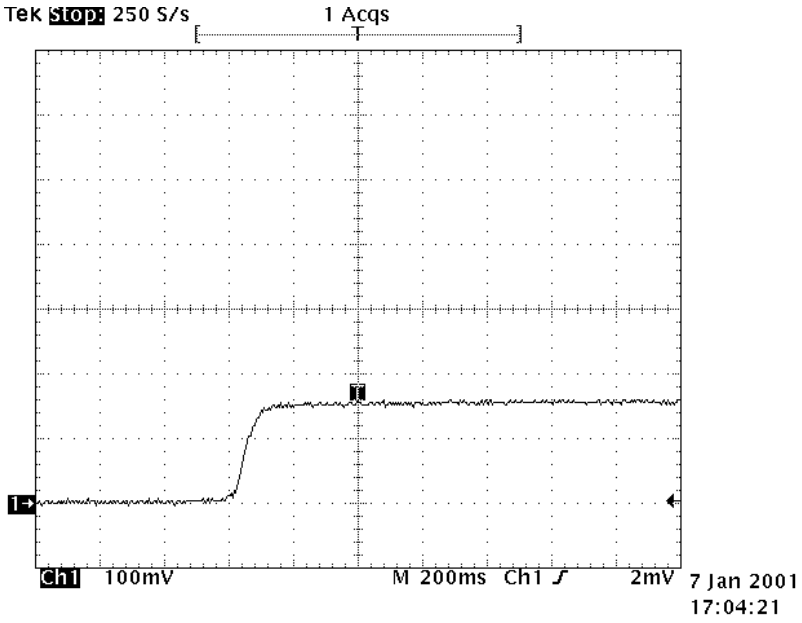
Fig.3.18. Output voltage and output current of modules under overload
(Ch.1: output voltage, 20V/div; Ch.2, Ch.3, Ch.4: module currents, 20A/div)

The current limit loop activity under overload case is shown in Fig.3.18, for multi-module operation. The current limit of the three modules used is set to 20A, each. When an overload occurs, MCU2 decreases the voltage step by step, according to current control algorithm. The current control loop is kept relatively slow, so that three modules are capable of limiting 3x45A without entering short-circuit hardware interrupt. In Fig. 3.19.a, the response of the system to an output short-circuit case is given. In this case, the output voltage is set to 0 by MCU2, using the hardware interrupt. The response is therefore very fast. Recovery from the short-circuit case to current limit operation is shown in Fig.3.19.b.

MCU2 increases the voltage in very small steps to supply the maximum permissible current.



(a) At the short-circuit instant



(b) At recovery

Fig.3.19. Output short-circuit current (10 A/div)

The derating loop's performance is illustrated in Fig.3.20, in which I_{lim} from derating loop is monitored against input voltage variations from nearly 250V to 50Vrms. The current limit value calculated by the derating loop is monitored from built-in D/A converter of MCU1. The input line voltage however is measured from secondary side of a measuring transformer. The current limit set value is input to the module as 25A, and output voltage is adjusted to nominal value of 53.5 V.

As shown from Fig.3.20, the current limit remains equal to the set value until the input voltage is reduced to nearly 167Vrms. Below this value, derating loop is activated, and the current limit value is decreased. The effect of piecewise linearisation of derating curve is observed as a decrease in the slope of current limit characteristic below V_{in}=160 V.

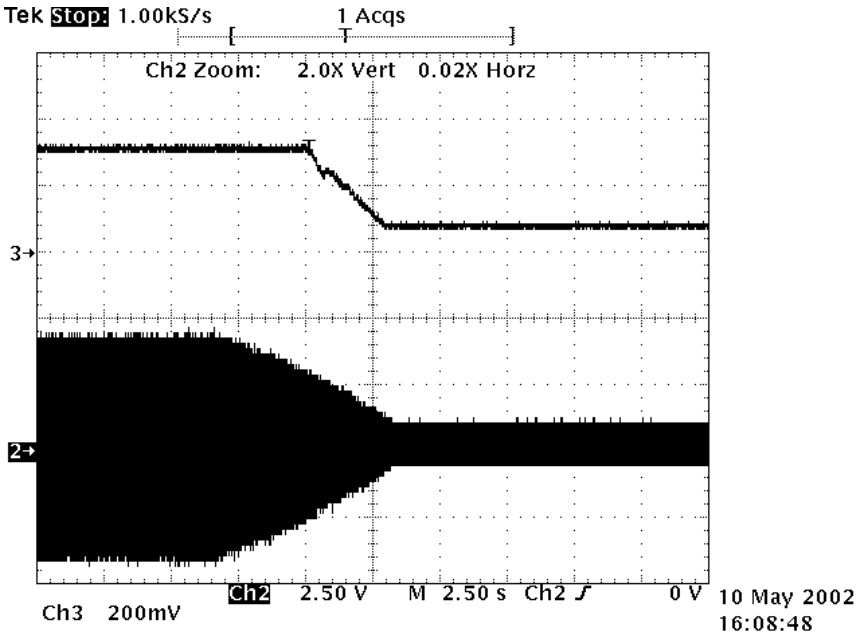


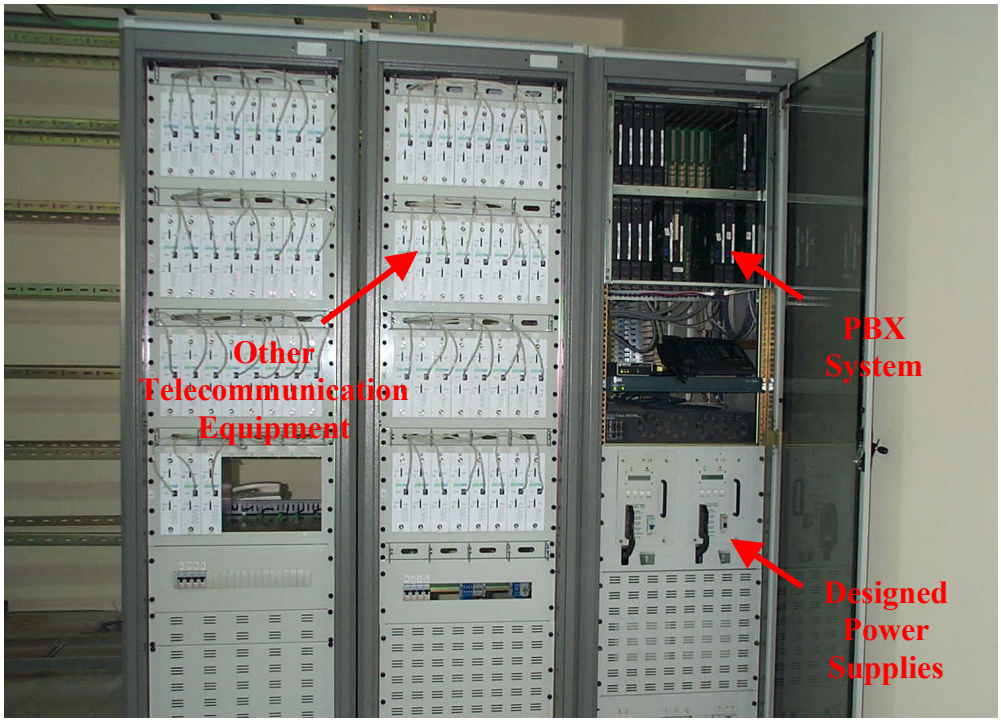
Fig.3.20. Derating versus input voltage (Ch 2: input voltage, 193 V/div; Ch.3: current limit value, 15.5 A/div)

This project won the "Technology Achievement Award" from TUBITAK, TTGV, and TUSIAD in 1999. The power supply modules are also exhibited in the 42th International PCIM/HFPC Conference and Exhibition held in Boston-USA, in year 2000 (Fig.3.21).

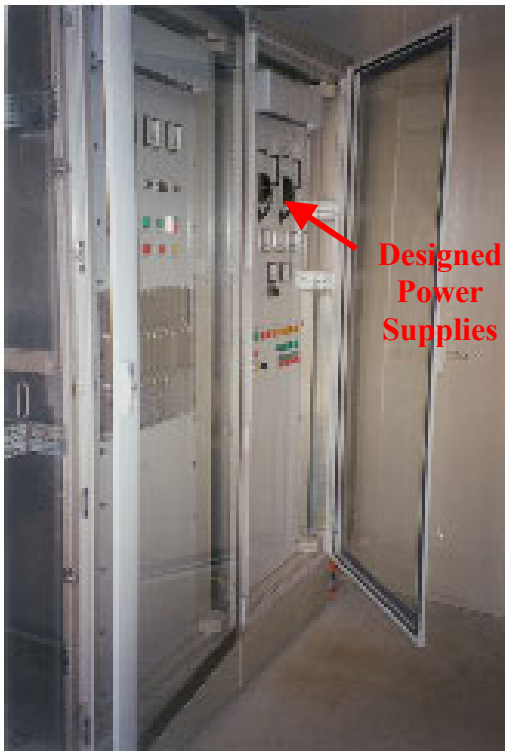
Fig.3.21. International PCIM/HFPC Conference and Exhibition Booth, and the "1999 Technology Achievement Award"

3.6. OPERATION IN THE FIELD

The implemented power supply modules have been installed in hundreds of locations, and are operating successfully, even under very harsh operating conditions (Appendix C). In Fig.3.22, some of the installations in the field are shown.



(a) A telecommunication system installed in TSM company in Istanbul



(a) TKI/ELI Reactive Power Compensation System

Fig.3.22. Systems in the Field

CHAPTER IV

PHASE II : DESIGN AND IMPLEMENTATION OF DSP CONTROLLED ZVS PHASE-SHIFTED FULL-BRIDGE CONVERTER

In the first phase of this thesis, the digital control of the telecommunication power supply, by the use of two low-cost 8-bit microcontrollers has been realized as described in Chapter 3. The two microcontrollers accomplish all the tasks related with the control of the power supply modules, except the transient response of the ZVS phase-shifted full-bridge converter.

Among the functions of the digitally controlled switch-mode power supply, implementation of the digital feedback necessitates high processing power and speed, due to the need for updating the switching patterns of power transistors by the control loop once every switching cycle, i.e. every 13.3μs. The processing speed and power needed is fulfilled by the first member of a new 32-bit, fixed-point DSP family: TMS320F2810 made commercially available in 2002, with a processing speed of 150MIPS (6.67 ns cycle time), and a built-in 12-bit A/D converter with a single conversion time of 200ns, and a pipeline conversion time of 60ns [70].

In this section, the design and implementation of the DSP controlled ZVS phase-shifted full-bridge converter will be presented. The general hardware block diagram of the proposed system is given in Fig.4.1. The output voltage of modules can be made user adjustable over a wide range (0-60Vdc in 100mV steps) by using a DSP – based digital controller, thus resulting in a universal output telecommunication rectifier.

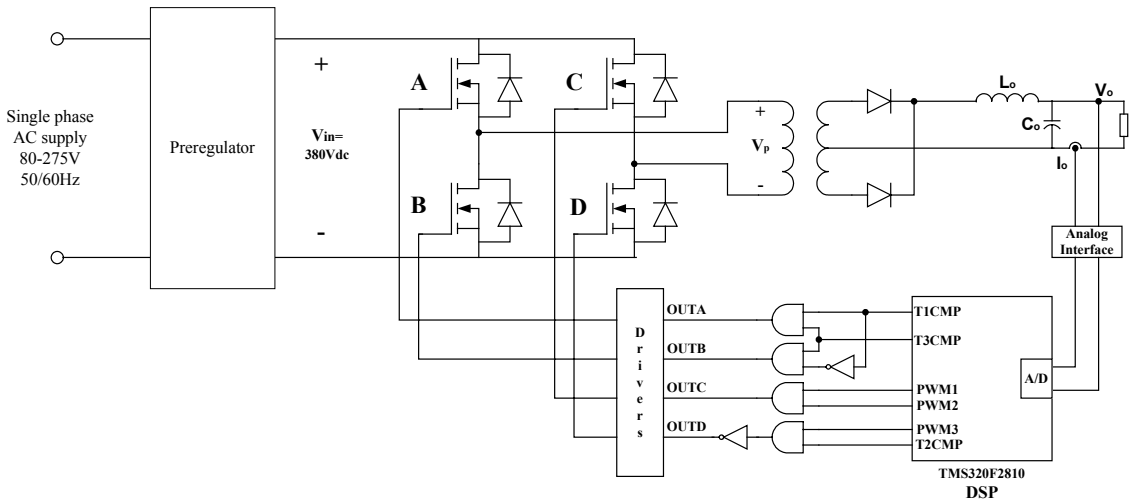


Fig.4.1. Hardware block diagram of the DSP based control system of the ZVS phase-shifted full-bridge converter

There are in general three approaches to design a digital feedback control system: The first is to design an analog controller and then discretize it, the second is to discretize the plant, and then do a discrete-time design, and the third is the so-called direct sampled-data approach, which amounts to designing a digital controller directly in the continuous-time domain. Since the second approach has the disadvantage of ignoring intersample behaviour and the third is still under development [71], the first approach is the one most often used one in industry, and is also used in this thesis [72].

4.1.THEORY

4.1.1. Phase Shifted Zero Voltage Transition (ZVT) Power Converter

The benefits of lossless Zero Voltage Transition (ZVT) switching techniques are well known throughout the power supply industry. The parasitic circuit elements are used advantageously to facilitate resonant transitions rather than snubbing

dissipatively. The resonant tank functions to put zero voltage across the switching devices prior to turn-on, eliminating power loss due to the simultaneous overlap of switch current and voltage at each transition. High frequency converters operating from high voltage input sources gain significant improvements in efficiency with this technique. The details of the operation of Phase Shifted ZVT power converter is described in Section 2.2.1.

4.1.2. Two-Pole-Two-Zero Compensation

This method of compensation is intended for power supply converters that exhibit a –40 dB/decade roll off above the poles of the output filter and a -180° phase lag. These are the forward-mode converters such as the buck, push-pull, half-bridge, and full-bridge topologies using voltage-mode control. The two-pole, two-zero method introduces zeros into the error amplifier compensation to reduce the steep gain slope above the double pole caused by the L-C filter, and its associated -180° phase shift.

The Bode response for two-pole, two-zero compensation is given in Fig.4.2. As seen from this figure, the amplifier has a +20 dB/decade slope between the zero and pole pairs. It also has a "phase bump" that peaks at the geometric mean frequency between the highest pole and the lowest zero frequency. The phase bump also has a maximum possible phase lead of +180° (or a net amplifier phase lag of -90°). The actual peak value of the phase bump is determined by the frequency separation between the zeros and the poles. So the greater the difference, the higher the phase peak. The purpose of the phase peak is to counteract the -180° phase lag of the L-C filter. The +20 dB/decade slope over this range also brings the overall gain slope to the –20 dB/decade slope. The lower of the high-frequency poles within the amplifier counteracts the zero caused by the ESR of the filter capacitor. The last pole is placed to increase the gain margin of the closed-loop system. So this pole is placed at a frequency higher than the gain crossover frequency [73].

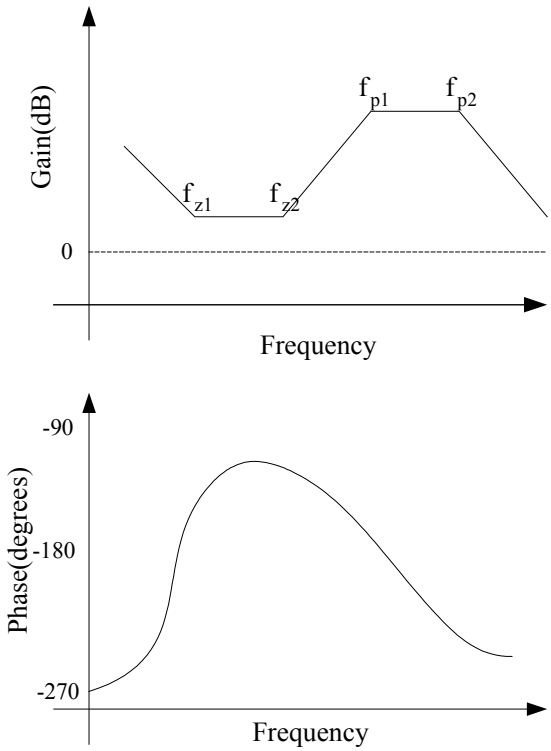


Fig.4.2. The bode plots for two-pole two-zero compensation

In the two-pole two-zero compensation method applied, following points are considered in the placement of the controller zeros and poles, and in the determination of the controller gain [73].

- The crossover frequency f_{x0} is chosen close to $f_s/5$ where, f_s is the converter switching frequency.
- The controller gain is chosen to bring the overall system transfer function to 0dB at the desired crossover frequency.
- The lower zero is placed at a frequency of $f_{P(LC)} / 5$.
- The second zero is placed just above the output LC filter poles.
- The first pole is placed at the lowest expected zero caused by ESR of the output filter capacitor.
- The second pole is placed above the overall crossover frequency.

4.1.3. The Z-Transform

The Laplace transform is defined by the relationship between time domain and s-domain signals. The z-transform is the discrete-time counterpart of the Laplace transform. Just as analog systems are analyzed using Laplace transform, digital systems are analyzed with a parallel technique called the z-transform.

The standard form of the z-transform:

$$X(z) = \sum x[n]\, z^{-n} \qquad (4.1)$$

where $z=re^{jw}$.

The relationship between the s-plane and z-plane can be seen in Fig.4.3.

The s-plane is a rectangular coordinate system with σ expressing the distance along the real axis, and ω the distance along the imaginary axis. In comparison, the z-plane is in polar form, with r being the distance to the origin, and ω the angle measured to the positive horizontal axis. Vertical lines in the s-plane, such as illustrated by the example of poles and zeros in Fig.4.3, correspond to the circles in the z-plane.

The left and right sides of the s-plane correspond to the interior and the exterior of the unit circle, respectively. For instance, a continuous system is unstable when poles occupy the right half of the s plane. In the same way, a discrete system is unstable when poles are outside the unit circle in the z-plane.

A continuous sinusoid can have any frequency between DC and ∞. This means that s-plane must allow ω to run from $-\infty$ to $+\infty$. In comparison, a discrete sinusoid can only have a frequency between DC and half of the sampling rate.

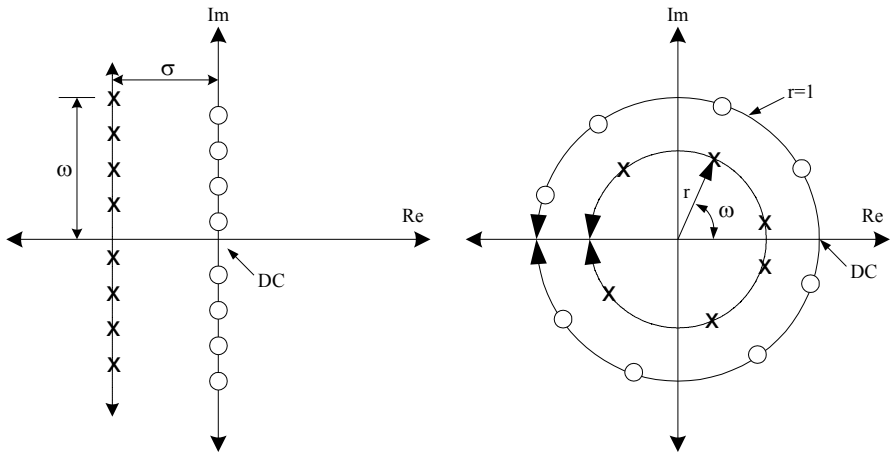


Fig.4.3. Relationship between s-plane and z-plane

In the s-plane, the values that lie along the vertical axis are equal to the frequency response of the system. In an analogous manner, the frequency response in the z-domain is found along the unit circle.

4.1.3.1.Dealing with poles and zeros in z-domain

Consider a simple second order system (Fig.4.4).

$$H(z) = \frac{(z - Z_1)(z - Z_2)}{(z - P_1)(z - P_2)} \tag{4.2}$$

For this system, the magnitude of the transfer function H(z) at frequency ω is

$$|H(z)| = U_1U_2 / V_1V_2 \tag{4.3}$$

and the phase of H(z) is

$$\angle H(z) = \theta_1 + \theta_2 - (\phi_1 + \phi_2) \tag{4.4}$$

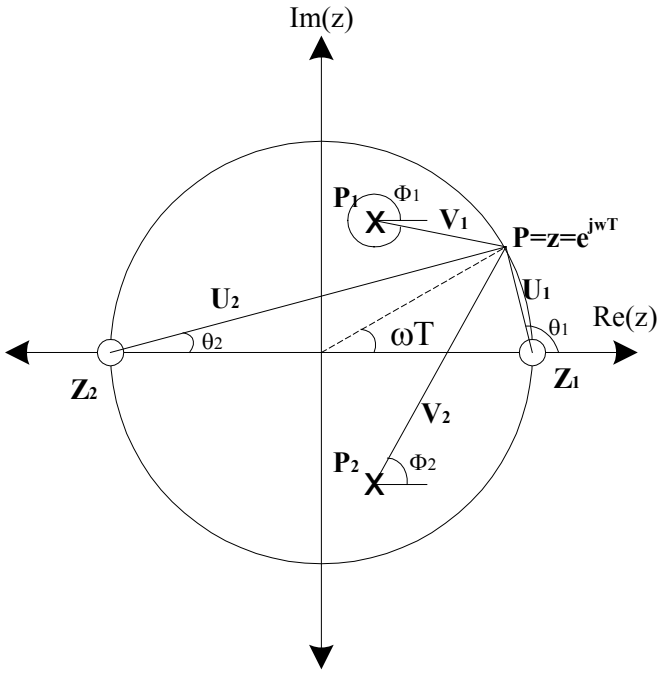


Fig.4.4. Second order system

4.1.3.2.Determining the corresponding poles and zeros of s-domain in z-domain

i- If the pole or zero is complex conjugate

Consider a zero/pole in s-domain as shown in Fig.4.5. In Fig.4.5, G_{dc} designates the DC gain, G_w is the minimum gain and the G_s is the gain at the half of the sampling frequency of the discrete signal that will be modeled in z-domain.

Fig.4.6 corresponds the corresponding zero/pole in z-domain.

To determine the exact location of zero/pole in z-domain, we must solve the angle θ and r values.

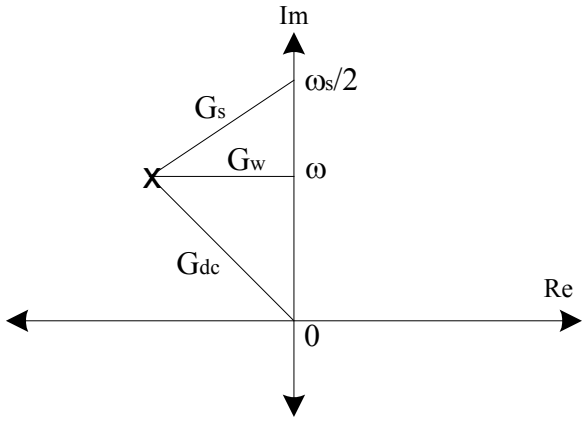


Fig.4.5. A zero/pole in s-domain.

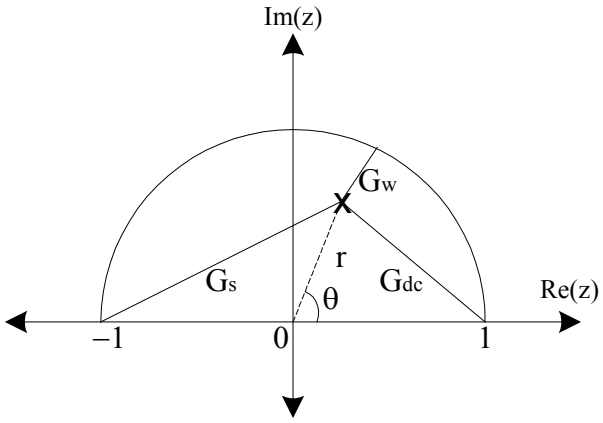


Fig.4.6.Corresponding zero/pole in z-domain.

The angle θ can be find by Eq.4.5.

$$\theta = w \times 180 / \pi \times \text{Switching frequency} \qquad (4.5)$$

In this equation switching frequency is in Hertz and θ will be in degrees.

To find r, define $a = G_{dc} / G_{min}$. By using some trigonometric equations we will obtain Eq.4.6.

$$r^2 - 2\frac{\text{Cos}\theta - a^2}{1 - a^2} r + 1 = 0 \qquad (4.6)$$

The root of Eq.4.6, which is $0 < r < 1$, will be the corresponding r of the zero/pole. As a result the corresponding zero/pole M will be

$$\begin{aligned} M &= r\, e^{j\theta} \\ &= r\,\text{Cos}\theta + j\, r\,\text{Sin}\theta \\ &= k + j\, n \end{aligned} \qquad (4.7)$$

Therefore the transfer function for zero will be

$$\begin{aligned} H(z) &= [z - (k+jn)]\,[z - (k-jn)] \\ &= z^2 - 2za + r^2 \end{aligned} \qquad (4.8)$$

For a pole,

$$H(z) = 1 / (z^2 - 2za + r^2) \qquad (4.9)$$

ii- If the pole or zero is on the real axis

If the zero/pole is on the real axis, the s-domain zero/pole and the corresponding z-domain zero/pole is shown in Fig.4.7.

To determine the z-domain zero/pole in z domain we have to determine only the G_{dcz} because in this case the angle θ will be 0.

We can define G_{sz} in terms of G_{dcz} as given in Eq.4.10.

$$G_{sz} = 2 - G_{dcz} \qquad (4.10)$$

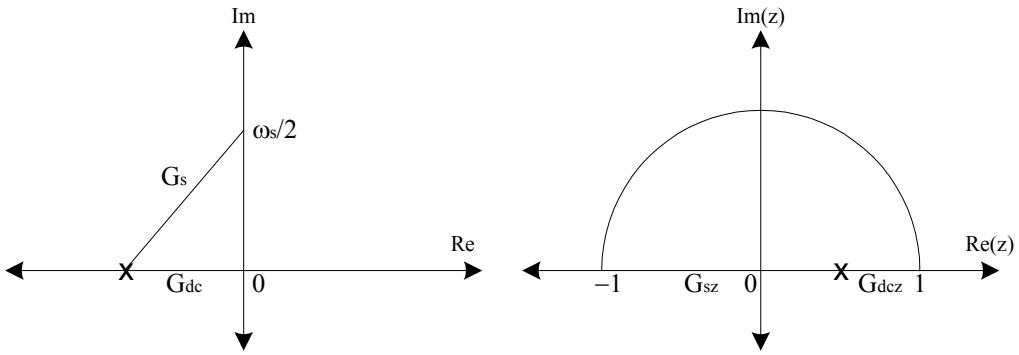


Fig.4.7. Zero/pole on the real axis

So to find G_{dcz}, we should solve Eq.4.11.

$$G_{dc} / G_s = G_{dcz} / (2 - G_{dcz}) \tag{4.11}$$

As a result, r of the z-domain zero/pole will be,

$$r = 1 - G_{dcz} \tag{4.12}$$

The transfer function of the zero in z-domain will be

$$H(z) = z - r \tag{4.13}$$

The transfer function of the pole in z-domain will be:

$$H(z) = 1 / (z - r) \tag{4.14}$$

4.2.MODELLING AND SIMULATION

In this section, determination of the digital control loop parameters will be explained. It is well known that for power supply converters that exhibit a –40

dB/decade roll-off above the poles of the output filter, and -180° phase lag, as it is the case for a voltage-mode full-bridge converter, application of a two-pole, two-zero compensation method (Fig.4.2) is suitable. Therefore, parameters of the digital controller are calculated based on the frequency response of the converter's output stage. In the design of the digital controller, z-domain techniques have been employed.

4.2.1. Output Stage

The output stage of the converter is an LC filter, which can be modelled as an RLC combination, by taking into account the equivalent series resistance of the filter inductor, as given in Fig.4.8.

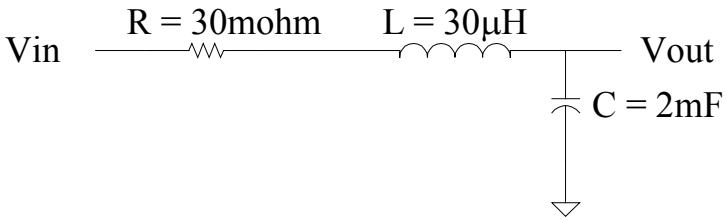


Fig.4.8. Output stage of the rectifier

The transfer function of the output stage in s-domain is given in Eq.4.15

$$\frac{V_{out}}{V_{in}} = \frac{1/LC}{s^2 + (R/L\,s) + (1/LC)} \tag{4.15}$$

This system has two complex conjugate poles. These pole locations can be determined by evaluating the roots of the denominator as given below.

$$P_1 = -500 - j\,4082.45$$
$$P_2 = -500 + j\,4082.45 \tag{4.16}$$

In the implemented converter, the switching frequency is chosen as 75 kHz, which also corresponds to the sampling frequency. The corresponding pole locations in the z-domain can be found as explained in detail in Section 4.1.3.

By using equations 4.5, and 4.6,

$$\theta = 3.120344° \tag{4.17}$$

$$r = 0.9933529784 \tag{4.18}$$

Therefore, the corresponding poles in z-domain can be expressed as :

$$P_1 = 0.9933529784\ e^{j3.120344}$$

$$P_2 = 0.9933529784\ e^{-j3.120344} \tag{4.19}$$

As a result, by using Eq.4.9, the transfer function of the output stage in z-domain is found as given in Eq. 4.20:

$$H(z) = 1 / (z^2 - 1.9837604778\ z + 0.9867501397) \tag{4.20}$$

The z-domain poles of the output stage are located on z-plane, as shown in Fig.4.9.

To determine the DC gain of the z-domain representation, one should calculate first V_1 and V_2 (Fig.4.9).

$$V_1 = \sqrt{(1 - r\mathrm{Cos}\theta)^2 + (r\mathrm{Sin}\theta)^2} \tag{4.21}$$

$$V_1 = 0.0546778013 \tag{4.22}$$

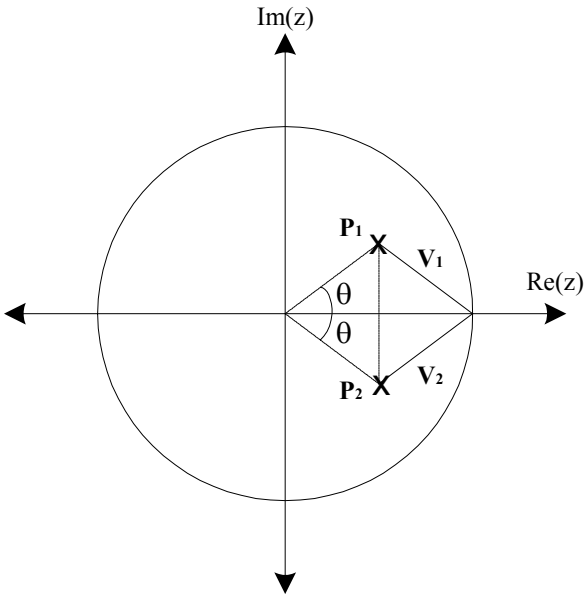


Fig.4.9.The z-domain poles of the output stage

The DC gain of the z-domain representation will be,

$$G_{dcz} = 1 / V_1 V_2 \tag{4.23}$$

From Fig.4.11, it is clear that $V_1 = V_2$. Therefore,

$$G_{dcz} = 334.485976 \tag{4.24}$$

The DC gain of the output stage of the rectifier should be 1. Therefore, one should divide the transfer function by 334.485976. As a result, the transfer function of the output stage, H(z), can be written as :

$$H(z) = \frac{(1/334.4859761)}{z^2 - 1.9837604778z + 0.9867501397} \tag{4.25}$$

4.2.2. Verification of the model

The calculated transfer function is verified by a model in MATLAB. The model is given in Fig.4.10.

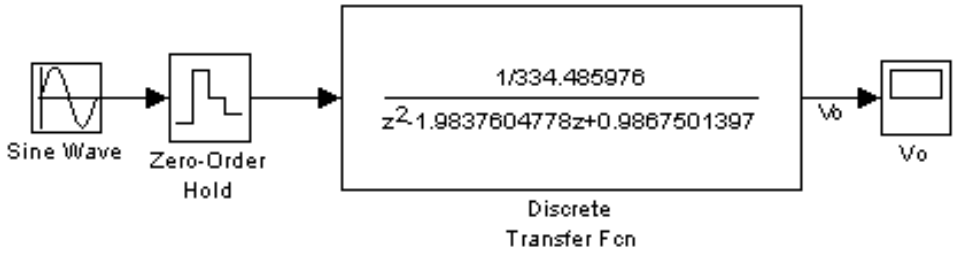


Fig.4.10. The model of the output stage of SMPS in MATLAB

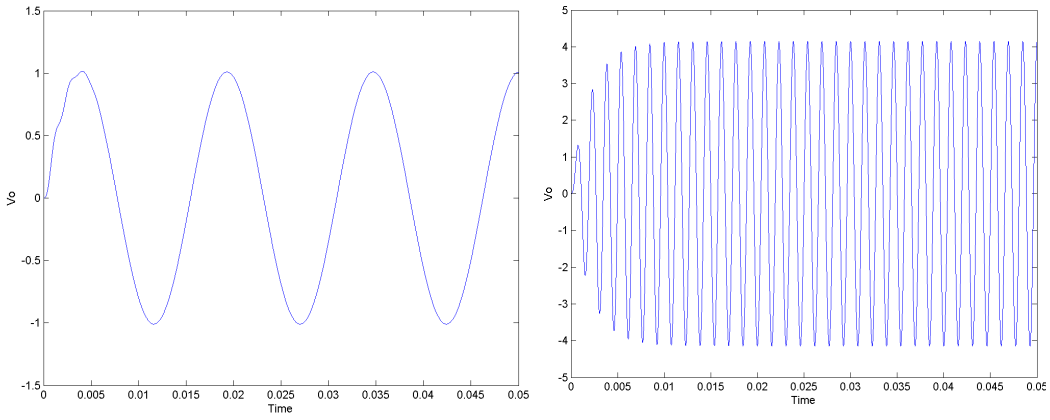
A sine wave with amplitude 1 and at variable frequency is applied to the system.

The corner frequency of the output stage is 650Hz. First a sine wave with a frequency of 65 Hz is applied. The output is a sine whose amplitude is 1 as expected, because the gain of the filter is 1 at 65Hz.

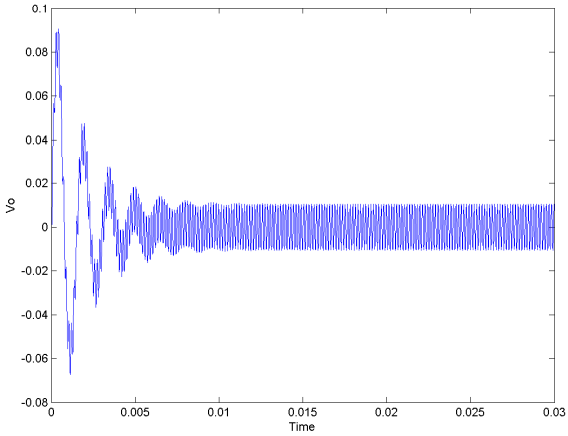
The second sine wave is at 650Hz which is the corner frequency. The output signal has an amplitude of 4 as expected.

The last input signal is at 6500Hz which is 10 times the corner frequency. As this filter has 40dB/decade attenuation, it is expected to have an output with 0.01. The result matches the expected output.

The output for these three input signals is given in Fig.4.1.



a. f = 65Hz b. f= 650Hz



c. f = 6500Hz

Fig.4.11. Simulation results of the output stage

4.2.3. Design of the control stage

In the design, the gain contributions coming from the power stage, and feedback circuitry are all included in the transfer function of the control stage. In the two-pole two-zero compensation method applied, the points mentioned in Section 4.1.2 are taken into account.

Some fine tuning can be made to the calculated gain, poles, and zeros as a result of the simulations carried out. As sampling is done at a frequency of 75 kHz, an anti-aliasing filter will be implemented at 37.5 kHz, which results in an inherent pole at 37.5 kHz. On the other hand, one should have a pole at DC, which inherently exists in the two-pole, two-zero compensation method, as shown in Fig.4.2. As a result, the poles and zeros of the control system that will be implemented are determined as given in Eq.4.26.

$$\begin{aligned} &Z1 = 707.6\text{Hz} \\ &Z2 = 1.4167\text{KHz} \\ &P1 = 0 \\ &P2 = 13.16\text{KHz} \end{aligned} \tag{4.26}$$

To find the corresponding poles and zeros in z-domain, they are first located in s-domain (Fig.4.12). The relationships between s-domain, and z-domain representations have been explained in detail in Section 4.1.3. By using equations 4.10, 4.11, and 4.12, the corresponding r values are found as given in Eq.4.27.

$$\begin{aligned} &r_{z1} = 0.96294788592 \\ &r_{z2} = 0.9272438225 \\ &r_{p1} = 1 \\ &r_{p2} = 0.50247795922 \end{aligned} \tag{4.27}$$

The control stage gain is determined as 25 by using the two-pole, two-zero compensation theory, and the simulation results carried out, to satisfy the specifications. As a result, the transfer function, H_c, of the control stage is:

$$H_c(z) = \frac{25(z - 0.96294788592)(z - 9272438225)}{(z-1)(z - 0.50247795922)} \tag{4.28}$$

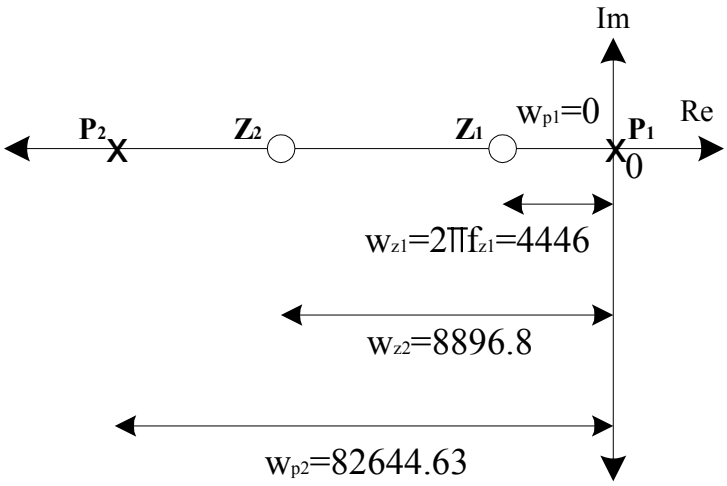
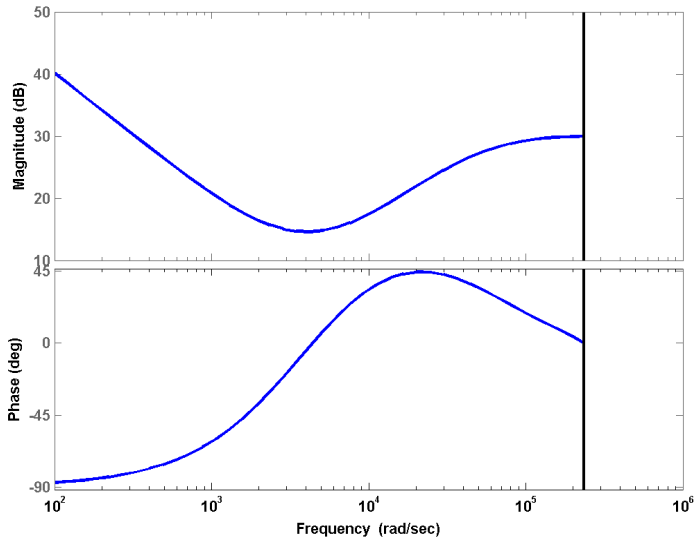


Fig.4.12.The pole and zero locations of the control stage

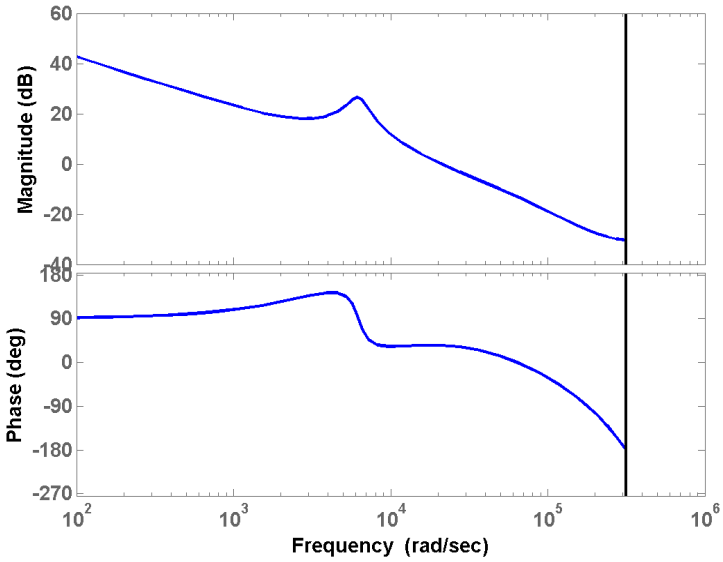
Corresponding frequency responses of the controller, and the overall system are given in Fig.4.13, using the z-domain transfer functions of the system.

4.2.4. Simulation of the overall system

The complete system, including the output, and control stages, is modeled in z-domain in MATLAB, as shown in Fig.4.14.a. In order to assess the transient load response, a resistive voltage divider is placed at the output of the model. The lower part of the resistive divider represents the output impedance of the rectifier, while the upper part represents the load. The simulation results related to the transient response of the converter against variations in load current, and step changes in the output voltage set value are given in Fig.4.14.b, and c, respectively.

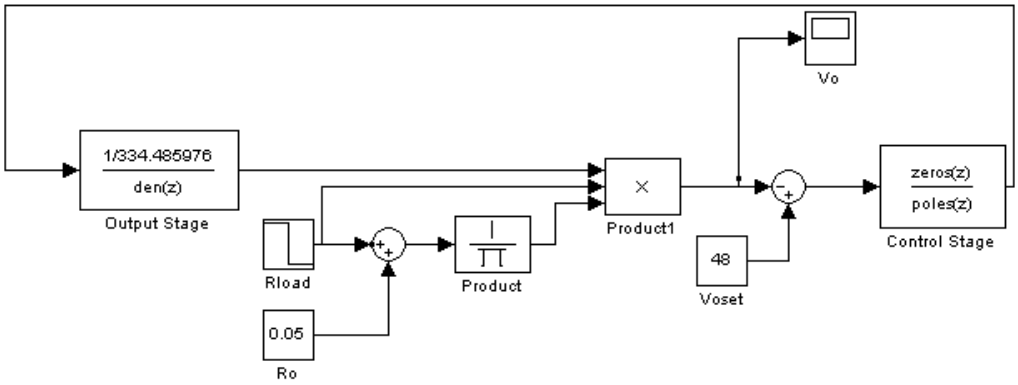


(a) The Bode plots of the control system

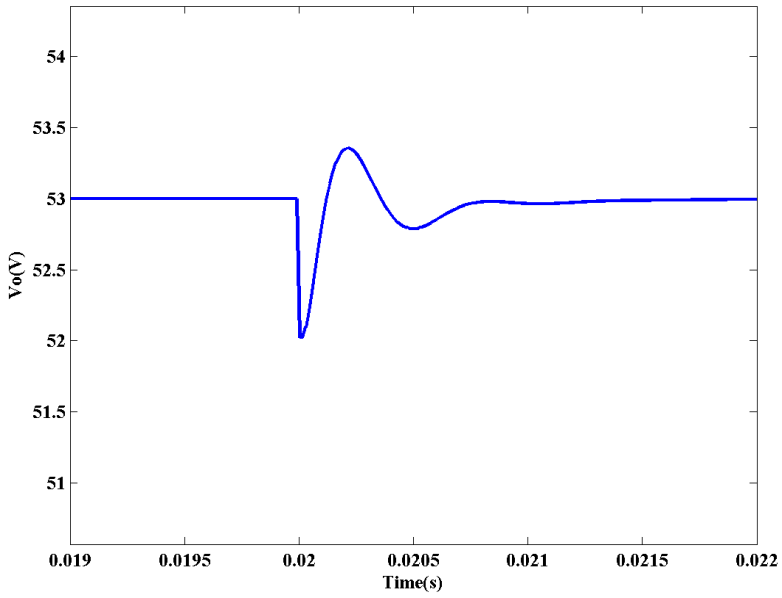


(b) The Bode plots of the overall system

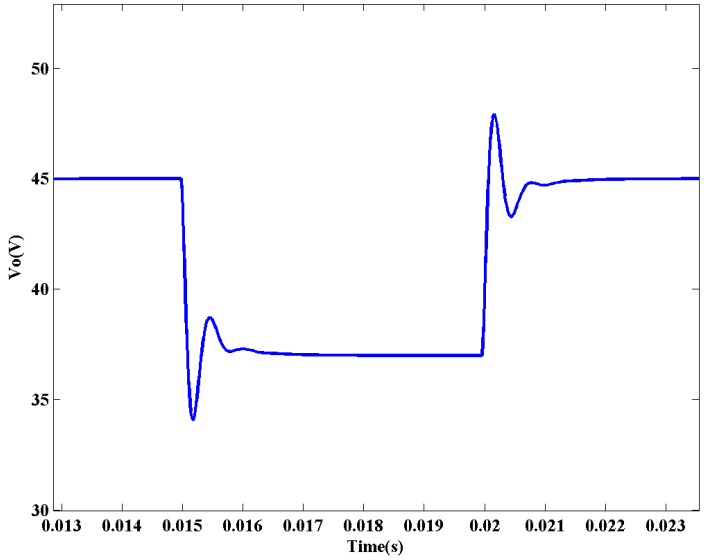
Fig.4.13. Bode plots of the converter



(a) The z-domain model of the converter in MATLAB



(b) Dynamic load regulation for an output current variation from 5A to 25A



(c) Transient response against a change in output voltage setting from 45Vdc to 37Vdc and vice versa

Fig.4.14. MATLAB simulation results.

4.3.DESIGN AND IMPLEMENTATION

4.3.1. Hardware

The DSP controlled ZVS phase-shifted full-bridge converter has been implemented by the use Starter Kit of TMS320F2810 DSP, and an interface board (Fig. 4.15).

4.3.1.1. PWM Generation

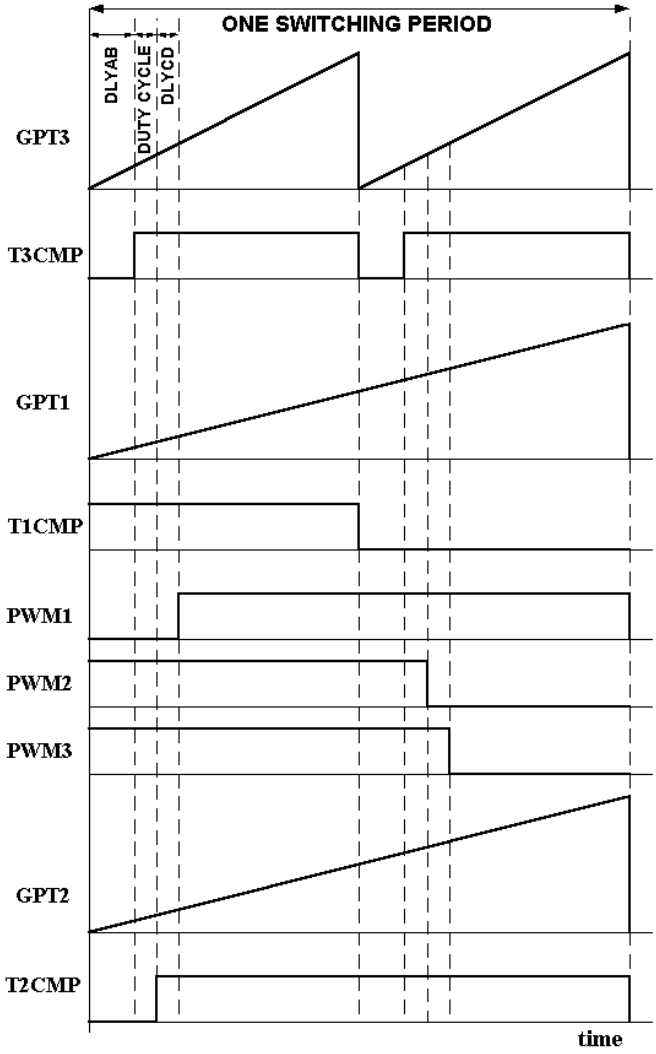
In the phase-shifted ZVS full-bridge converter control, rather than driving both of the diagonal full bridge switches together, a deliberate delay is introduced between their turn-on commands.

Fig.4.15. Experimental setup of the implemented DSP controlled ZVS phase-shifted full-bridge

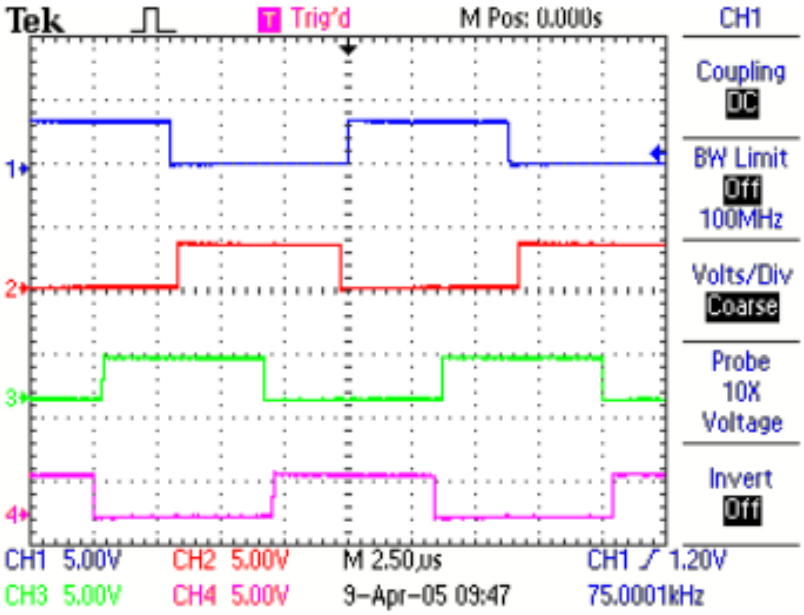
This delay is adjusted by the control circuitry, and essentially results as a phase shift between the two drive signals. The effective duty cycle is controlled by varying the phase shift between the switch drive commands. The PWM generation circuits, i.e. the event managers, on the DSP, however, are designed for generation of PWM signals with adjustable duty cycles. Therefore, to generate the phase-shifted PWM patterns, a special PWM generation technique is needed. The event manager (EV) modules in the DSP include general-purpose (GP) timers, and full-compare/PWM units.

The two EV modules, EVA and EVB, on the TMS320F2810, consist of two general purpose timers. In generation of the phase shifted firing patterns, the two general purpose timers of the first event manager (GPT1, GPT2), one of the

general purpose timers of the second event manager (GPT3), and the compare units for these timers are used. By using these peripherals, the six signals labeled as T1CMP, T2CMP, T3CMP, PWM1, PWM2 and PWM3 are produced at the pins of the DSP as shown in Fig.4.16. In this configuration, T1CMP and T3CMP are used to obtain the PWM signals for left leg switches of the full bridge converter (OUTA and OUTB), and constitute the reference.



a. PWM control signals produced by the DSP



b. PWM control signals generated experimentally at the driver inputs (Ch.1: OUTA, Ch.2: OUTB, Ch.3: OUTC, Ch.4: OUTD)

Fig.4.16. PWM control signals generated

OUT A : T1CMP AND T3CMP ;

OUT B : $\overline{\text{T1CMP}}$ AND T3CMP (4.29)

The remaining four signals, T2CMP, PWM1, PWM2, and PWM3 are adjusted according to the duty cycle calculated by the control loop, and are used for generation of the shifted PWM waveforms for right leg switches (OUTC and OUTD).

OUT C : PWM1 AND PWM2 ;

OUT D : $\overline{\text{T2CMP AND PWM3}}$ (4.30)

The signals at the PWM output pins of the DSP are then converted to the phase shifted PWM waveforms by using the hardware shown in Fig.4.1.

The minimum resolution of the PWM depends on steady-state operating conditions in the circuit and A/D resolution. The required PWM resolution is given by Eq.4.31 [74].

$$n_{pwm} \geq \text{int}\left[n_{a/d} + \log_2\left(\frac{V_{ref}}{V_{\max_{a/d}} \times D} \right) \right] \tag{4.31}$$

where n_{pwm} is the PWM resolution,

$n_{a/d}$ is the A/D converter resolution,

V_{ref} is the reference voltage of A/D converter

$V_{max\ a/d}$ is the full-range voltage of the A/D converter, assuming unipolar conversion in the rangefrom 0 to $V_{max\ a/d}$, and

D is the gain of the converter.

In our case,

$$n_{pwm} \geq \text{int}\left[12 + \log_2\left(\frac{3.3}{3.3 \times 0.13} \right) \right] \tag{4.32}$$

$$n_{pwm} \geq 15 \tag{4.33}$$

The DSP we use in our design has 16-bit resolution PWM facility, which satisfies the above condition.

4.3.1.2. MOSFET Drivers

The voltage and the current ratings of the CMOS circuits used in generating the PWM signals are not sufficient to drive the MOSFETs used in the full bridge converter. Therefore, a totem pole output driver circuit has been designed. In this design, MOSFETs are used as the switching elements because of being voltage

driven switching devices. Moreover, to provide galvanic isolation and to drive the high side MOSFETs, pulse transformers are used. The driver circuit designed is shown in Fig.4.17.

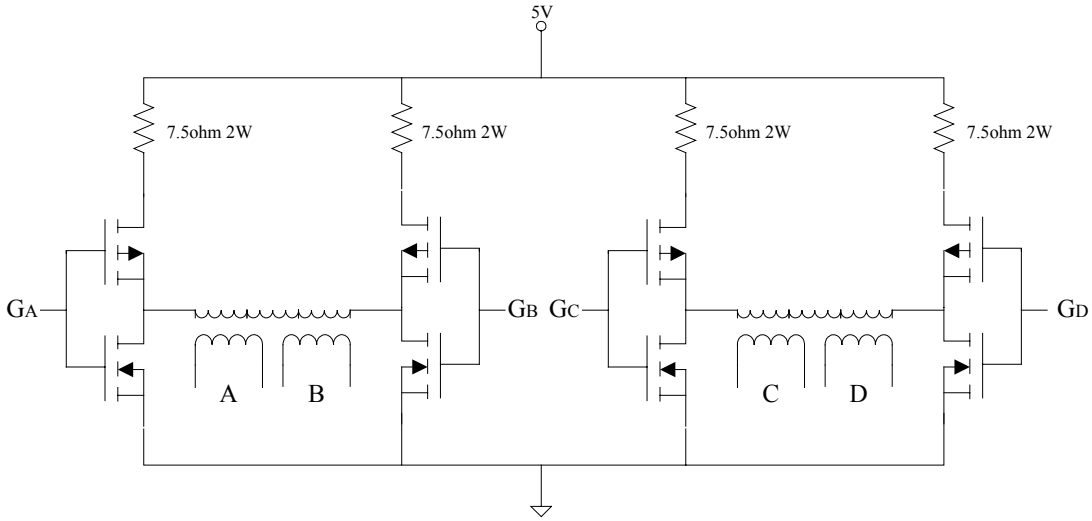


Fig.4.17. MOSFET driver circuit diagram.

4.3.1.3.Analog Interface

The sampling theorem, frequently called the Shannon sampling theorem, or the Nyquist sampling theorem, indicates that a continuous signal can be properly sampled, only if it does not contain frequency components above one-half of the sampling rate. For instance, a sampling rate of 2,000 samples/second requires the analog signal to be composed of frequencies below 1000 cycles/second. If frequencies above this limit are present in the signal, they will be aliased to frequencies between 0 and 1000 cycles/second, combining with whatever information that was legitimately there.

The key point to remember is that a digital signal cannot contain frequencies above one-half the sampling rate (i.e., the Nyquist frequency/rate). When the frequency of the continuous wave is below the Nyquist rate, the frequency of the

sampled data is a match. However, when the continuous signal's frequency is above the Nyquist rate, aliasing changes the frequency into something that can be represented in the sampled data. Every continuous frequency above the Nyquist rate has a corresponding digital frequency between zero, and one-half of the sampling rate. If there happens to be a sinusoid already at this lower frequency, the aliased signal will add to it, resulting in a loss of information.

Fig.4.18 shows a block diagram of a DSP system, as the sampling theorem dictates it should be. Before encountering the analog-to-digital converter, the input signal is processed with an electronic low-pass filter to remove all frequencies above the Nyquist frequency (one-half the sampling rate). This is done to prevent aliasing during sampling, and is correspondingly called an antialias filter.

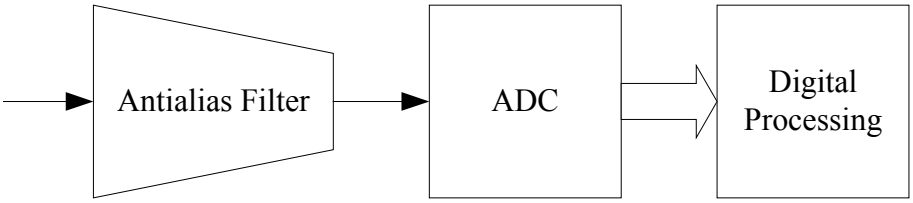


Fig.4.18. Block diagram of a DSP system

The relationship among the number of bits of A/D converter and the output frequency from the oscillator of the dc-dc converter is clarified in [74].

$$f_{ck} \cong \frac{2^{Q}-1}{T_s} \tag{4.34}$$

where, f_{ck} is the frequency of the oscillator

Q is the number of bits of the A/D converter

T_s is the switching period.

When we apply Eq.4.34 to our design,

$$2^{Q} - 1 \cong 150MHz \times 13.3\mu s \cong 1995 \quad (4.35)$$

From Eq.4.35, the resolution of the A/D converter should be minimum 11 bits. In our design, we use the built-in A/D converter with a resolution of 12-bits.

4.3.2. Software

A power supply requires efficient negative feedback control to have good line and load regulation, and good dynamic response to system disturbances. Deficiencies in gain and phase margins must be compensated for using an appropriate pole-zero compensation network. This leads to a minimised steady-state error in the output, fast transient response to sudden load changes, and unconditional stability of the system.

As mentioned earlier, there are two basic approaches for digital controller design based on the conventional control theory: digital redesign and direct digital design. The digital redesign approach is used in this work. Digital redesign enables to use some of the well-known controller design methods previously developed for continuous-time analog implementations [75].

4.3.2.1.General

In discrete domain, a system can be described as given by Eq.4.36.

$$y[n]=(a_0 * x[n] + a_1 * x[n-1] + a_2 * x[n-2] +...)–(b_1 * y[n-1] + b_2 * y[n-2] +...) \quad (4.36)$$

where x[ ] and y[ ] are the input and output signals, respectively, and the "*a*" and "*b*" terms are the coefficients**.** An obvious use of this equation is to describe how

a programmer would implement the system. An equally important aspect is that it represents a mathematical relationship between the input and output that must be continuously satisfied. Just as continuous systems are controlled by differential equations, discrete systems operate in accordance with this difference equation.

To see what this controlling relationship looks like in the z-domain, we take the z-transform of both sides of Eq.4.36. With a fair amount of algebra, we can separate the relation into: $Y[z] / X[z]$, that is, the z-domain representation of the output signal divided by the z-domain representation of the input signal. Just as with the Laplace transform, this is called the system's transfer function, and designated by H[z] as given in (4.37).

$$H[z] = (a_0 + a_1 z^{-1} + a_2 z^{-2} + ...) / (1 + b_1 z^{-1} + b_2 z^{-2} + ...) \quad (4.37)$$

This is one of two ways that the transfer function can be written. This form is important because it directly contains the coefficients.

Equation 4.37 expresses the transfer function using negative powers of z. After an actual set of coefficients have been plugged in, we can convert the transfer function into a more conventional form that uses positive powers by multiplying both the numerator and denominator with the highest power of z:

$$H[z] = (a_0 z^n + a_1 z^{n-1} + a_2 z^{n-2} + ... + a_n) / (z^n + b_1 z^{n-1} + b_2 z^{n-2} + ... + b_n) \quad (4.38)$$

Just as with the s-domain, an important feature of the z-domain is that the transfer function can be expressed as poles and zeros. This provides the second general form of the z-domain:

$$H[z] = [(z-z_1) (z - z_2) ...] / [(z-p_1) (z - p_2) ...] \quad (4.39)$$

Each of the poles and zeros is a complex number. To move from Eq.4.39 to Eq.4.38, multiply out the expressions, and collect like terms. While this can involve a tremendous amount of algebra, it is straightforward in principle, and can easily be written into a computer routine.

4.3.2.2. Coefficient Calculations

As it is given in Section 4.2.3, the transfer function of the control stage is calculated to be:

$$H_c(z) = \frac{25(z - 0.96294788592)(z - 9272438225)}{(z - 1)(z - 0.50247795922)} \tag{4.40}$$

This representation is the second general form of the z-domain as shown in Eq.4.39. We need to convert it to form given in Eq.4.36, which gives us the coefficients that will be used in the implementation.

To start with, we should convert Eq.4.40 to form given in Eq.4.38. To do this, we multiply out the expressions and collect like terms.

$$H[z] = \frac{25z^2 - 47.2547927105z + 22.322186965}{z^2 - 1.50247795922z + 0.50247795922} \tag{4.41}$$

Following this process, we should convert Eq.4.41 to form given in Eq.4.37 by dividing both the numerator and the denumarator by z^2.

$$H[z] = \frac{25 - 47.2547927105z^{-1} + 22.322186965z^{-2}}{1 - 1.50247795922z^{-1} + 0.50247795922z^{-2}} \tag{4.42}$$

The last stage is to convert the Eq.4.42 to the form given in Eq.4.36. This is very easy because the coefficients are directly given in Eq.4.42, where

$a_0 = 25$
$a_1 = -47.2547927105$
$a_2 = 22.322186965$
$b_1 = -1.50247795922$
$b_2 = 0.50247795922$ (4.43)

As we will make the implementation with a DSP, we make some rounding in the coefficients and obtain the coefficients given in Eq.4.44.

$a_0 = 25$
$a_1 = -47.2$
$a_2 = 22.3$
$b_1 = -1.5$
$b_2 = 0.5$ (4.44)

As a result, our control stage can be described by Eq.4.45.

$$y[n] = 25\,x[n] - 47.2\,x[n-1] + 22.3\,x[n-2] + 1.5\,y[n-1] - 0.5\,y[n-2] \quad (4.45)$$

We use 12 bit ADC to digitize the output voltage. We adjust the gain of the analog interface such that 1 step corresponds to 16mV.

$$x[n] = 0.016 * x[n]' \quad (4.46)$$

where x[n]' is the value read from ADC.

Furthermore, the transfer function given in Eq.4.45 produces the applied voltage to the LC filter. However, the duty cycle that must be applied to the switches in

the bridge configuration should be calculated. There is a linear relation between the output voltage and the corresponding duty cycle. In our case, when we apply 100% duty cycle, the voltage applied to the LC filter will be 85V. As a result, to convert the calculated output voltage to the desired duty cycle, the calculated y[n] should be multiplied with 100/85.

$$y[n]'=y[n] * 100/85 \tag{4.47}$$

where y[n]' is the duty cycle that must be applied to the switched in the bridge configuration.

As a result we can modify the transfer function given in Eq.4.45 to the one that we will use in the implementation as given below.

$$y[n]'=y[n] * 100/85 \tag{4.48}$$

Replace y[n] with the expression given in Eq.4.45:

$$\begin{aligned} y[n]' = (&25\, x[n] - 47.2\, x[n-1] + 22.3\, x[n-2] \\ &+ 1.5 * 85/100\, y[n-1]' - 0.5 * 85/100\ y[n-2])*100/85 \end{aligned} \tag{4.49}$$

Replace x[n] with the expression given in Eq.4.46:

$$\begin{aligned} y[n]' = (&25 * 0.016\, x[n]' - 47.2* 0.016\, x[n-1]' + 22.3* 0.016\, x[n-2]' \\ &+ 1.5\ * 85/100\, y[n-1]' - 0.5 * 85/100\ y[n-2]) * 100/85 \end{aligned} \tag{4.50}$$

Moreover, as we use a fixed point DSP, we have to use integer constants. If the second part of the Eq.4.45 is multiplied with, and divided by1024, then the calculated output, y[n], will not differ. Here, we use 1024, because it is easier and faster in DSP to divide the numbers to 2's exponents (by right shifting).

$$y[n]' = (25 * 0.016\, x[n]' - 47.2 * 0.016\, x[n-1]' + 22.3 * 0.016\, x[n-2]' + 1.5 * 85/100\, y[n-1]' - 0.5 * 85/100\, y[n-2]) * 100/85 * 1024 /1024 \quad \ldots (4.51)$$

When we simplify Eq.4.51,

$$y[n]'=(482\, x[n]' - 910\, x[n-1]' + 429\, x[n-2]' + 1536\, y[n-1]' - 512\, y[n-2]')/1024 \quad \ldots (4.52)$$

where,

y[n]': calculated duty cycle,

x[n]': value read from ADC.

Equation 4.52 is used in the implementation.

4.3.2.3.Software Implementation

In the designed digitally-controlled universal telecommunication rectifier, the DSP has three main tasks to carry out in one switching period. They are related to the control of the full bridge converter. The timing diagram of these three tasks, and their input/output relationship are given in Figs.4.19 and 4.20, respectively. The first task is the sampling of voltage from the output of the power supply. The built-in A/D converter is used for this process. The A/D converter starts conversion on receiving the compare interrupt generated by GPT1.

This interrupt occurs at the middle of the switching period. After completing this task, DSP starts the second task which is the control process. The control process applies the control algorithm to the output voltage, and calculates the duty cycle to be applied to the full bridge converter in the next cycle. The control algorithm is determined from the theoretical results found in Section 4.3.2. The third task is

the PWM generation, which starts with the compare interrupt generated by GPT1, and runs in parallel with the sampling process. In this task, the DSP produces the necessary signals for generation of the phase- shifted PWM signals, by adjusting the compare registers for the three general purpose timers (GPT1,GPT2,GPT3), and the PWM registers of GPT1. The flowchart of the DSP-based controller is shown in Fig.4.21.

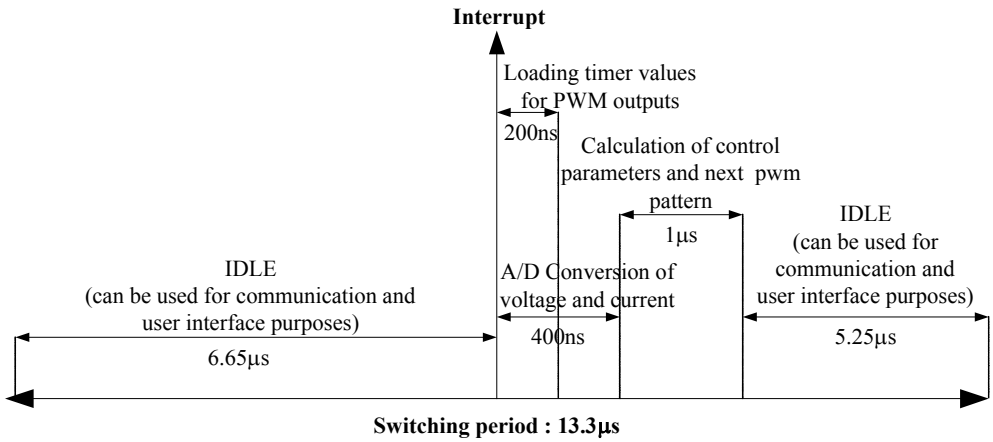


Fig.4.19. Timing sequence of the digital controller tasks

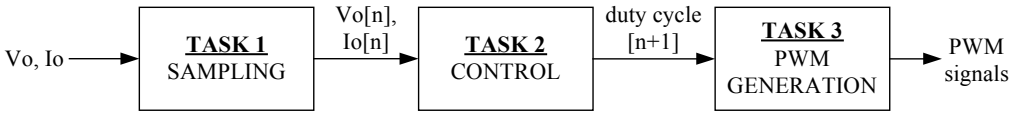


Fig.4.20. The I/O relationship between tasks of digital controller

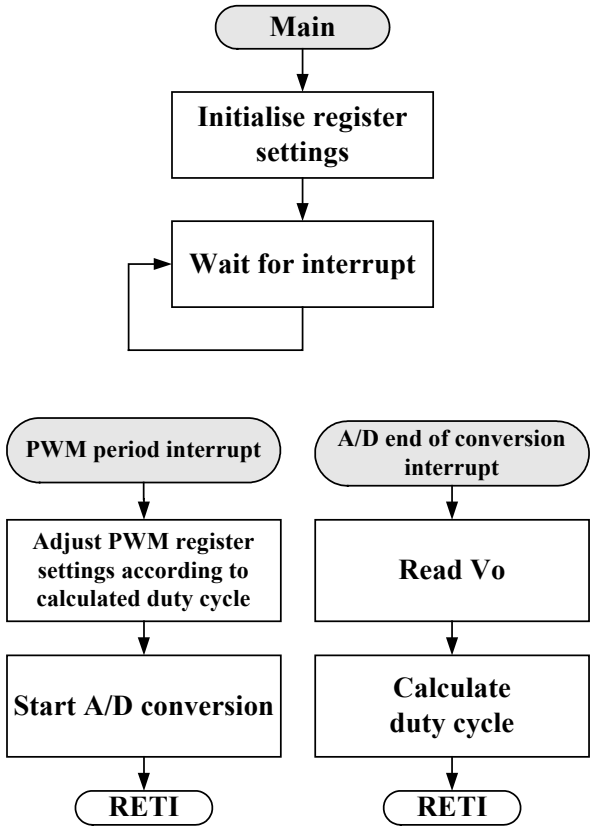
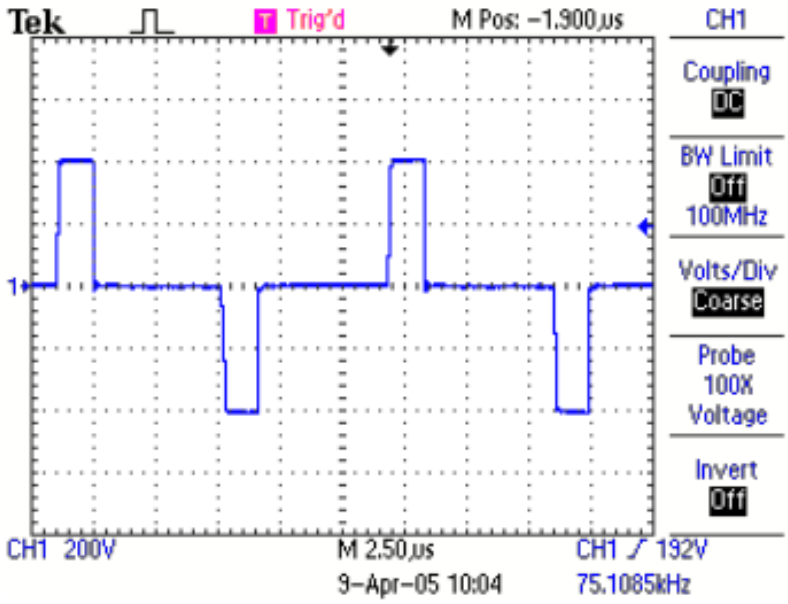


Fig.4.21. Flowchart of the controller

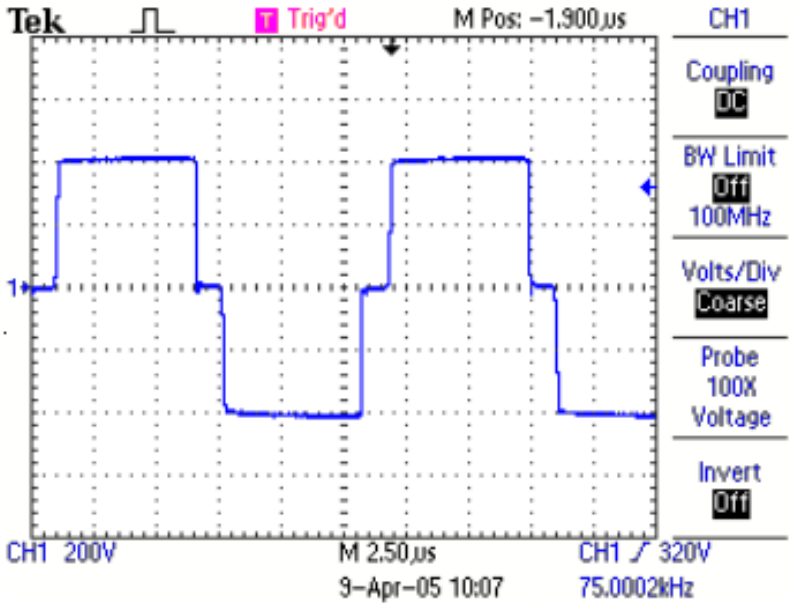
4.4. RESULTS

Experimental results obtained on the prototype telecom rectifier are presented in this section. The transformer primary voltage waveform at the full bridge inverter output is given in Fig.4.22, under both light and heavy load conditions corresponding to two different duty cycles, D.

The system performance was assessed by considering the response of the converter's output voltage to step changes in the output voltage set value, and to load current variations. The output voltage response to a step change in the reference voltage setting of the converter module from 45V to 37V, and vice versa is given in Fig.4.23. The system presented a satisfactory response to step changes in the reference setting, over the entire operating range.



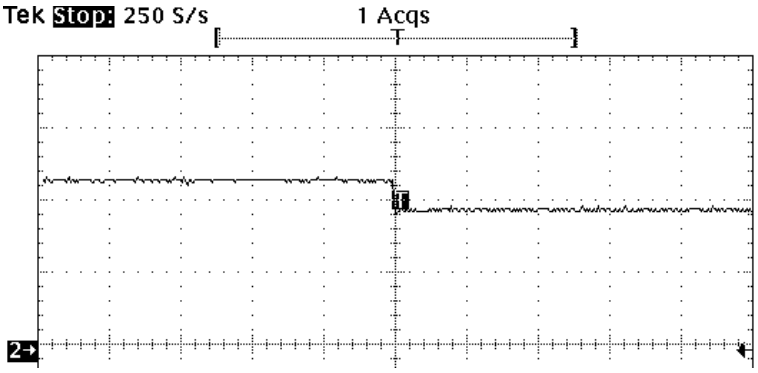
a. D=20%



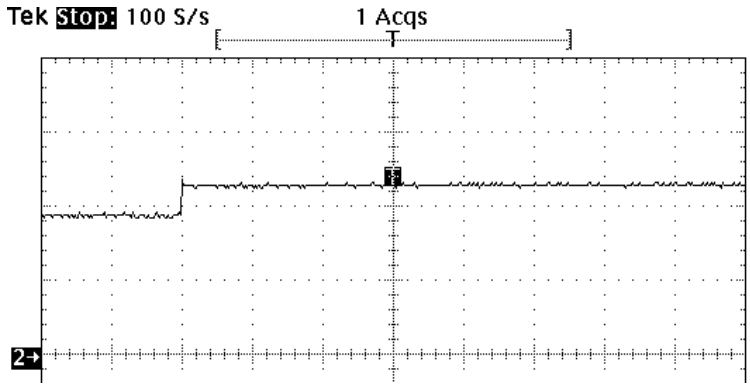
b. D=80%

Fig.4.22. Full-bridge inverter output voltage at different duty cycles

Fig.4.24 shows the output voltage dynamic load regulation against a step change in the load current from 5A to 25A, and vice versa, obtained by means of an electronic load (HP6050A), while the converter was operating at the nominal output voltage of V_o=48V_{dc}. The system has been tested using both the digitally implemented controller, and its analog counterpart.

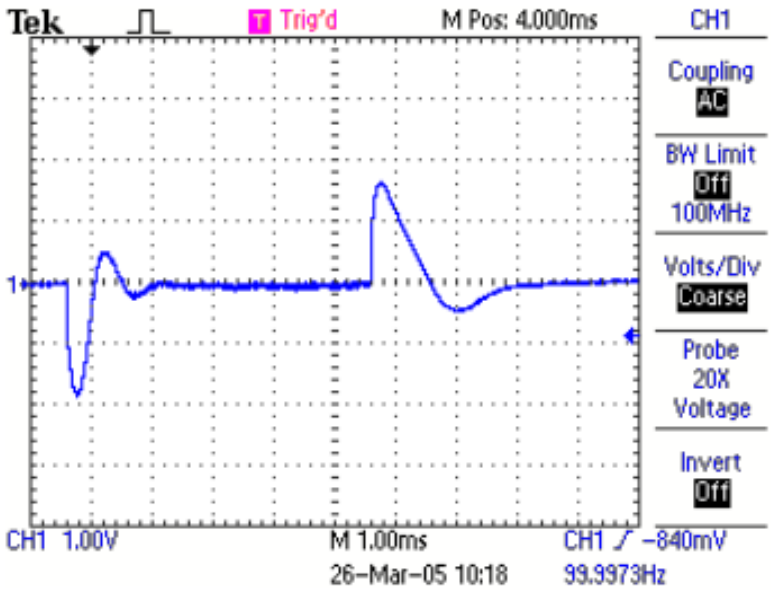


(a) V_{set}: from 45V to 37V

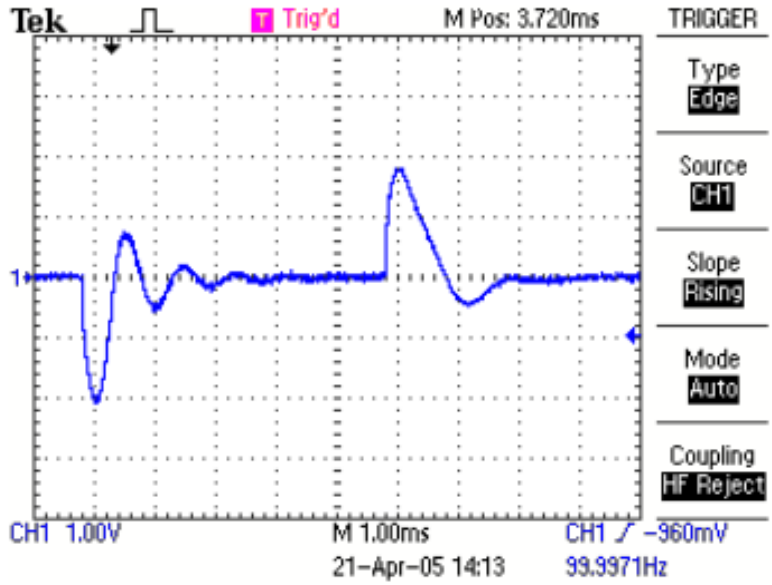


(b) V_{set}: from 37V to 45V

Fig.4.23. Measured output voltage step response (20V/div, 200 ms/div)



(a) Fully digital control



(b) Analog control

Fig.4.24. Measured dynamic response, $V_{o(ac)}$, for a transient variation of I_o between 5A and 25A (1V/div, 1ms/div)

As it is observed from the ac component of output voltage, even more satisfactory results have been obtained for the dynamic load regulation of the digitally controlled converter as compared to its analog counterpart. This is due to the fact that, component tolerances, ageing etc do not affect the digital controller parameters, which can be precisely adjusted by software.

CHAPTER V

CONCLUSIONS

In this research work, digitally controlled, universal-input, universal-output, telecommunication power supply modules have been designed, implemented, and tested successfully in the field. The proposed digital control system provides a cost-effective, viable alternative solution to the analog counterparts with increased controllability, flexibility, and reliability. The design and implementation of the digital controller for 1.8 kW telecommunication power supply modules have been carried out in two phases.

In the first phase, design guides of a parallel-operated, low-cost, dual-microcontroller based digital controller have been presented. In the implemented power supply modules, the processors share the tasks according to their speed requirements. One of the microcontrollers is employed for user interface purposes, such as long term records, display, and alarm facilities which are inherently slow processes. It also includes the functions for remote control, and derating under extremely low input ac supply voltages.

The fast processing speed required by output voltage setting, current limit, and load current sharing among parallel operated power supply modules is fulfilled by the second microcontroller, which adjusts the output voltage setting of the PWM generator in the phase-shifted full-bridge converter according to the information coming from the first microcontroller through the serial interface. By this way, the output voltage of modules can be adjusted between 0 – 70 Vdc with 0.1V resolution via keypad or remote control. Transient response of the full-bridge converter operating at a switching frequency of ≈ 100 kHz, however,

is controlled by the use of an external integrated circuit (UC3875) to meet the tight dynamic load regulation requirements of a telecommunication power supply.

The user programmable current limit setting (between 0 – 40 A), serial-communication based, active load current sharing with automatic master/slave selection property between parallel-operated modules, extended operating output voltage range, and overload and output short-circuit protection features have been successfully implemented as the digitally-controlled features of the universal telecommunication power supplies.

The implemented power supply modules have been installed in hundreds of locations, and have been operating continuously even under harsh operating conditions in the field, since year 2000. The corresponding research and development project received the "Technology Achievement Award" from TUBITAK, TTGV, and TUSIAD in the 'Third Technology Congress'. The developed digitally-controlled power supply modules [68,78] have also been exhibited in the 42th International PCIM/HFPC Conference and Exhibition held in Boston-USA, in October 2000.

In the second phase, a fully digital feedback control of a 75 kHz, 1.8 kW ZVS phase-shifted full-bridge converter has been designed and implemented using a high processing power DSP with PWM generation capability, to alternatively replace the second microcontroller and the external PWM IC. The digital feedback for controlling the transient response of the DC/DC converter operating at a high switching frequency can only be achieved properly using a high processing power DSP, with an instruction capacity of 100 MIPS or higher. With the advents in high processing power DSP technology, the duty cycle of the converter can now be updated every switching cycle. In the digitally-controlled power supply module, the phase-shifted PWM signals have been generated from

the built-in PWM outputs of a 150 MIPS DSP by using a special PWM generation technique, the time delay between the switching in the two legs of the full-bridge converter being adjustable in 6.7 ns steps.

The dynamic performance of the resulting DC-DC converter at 75 kHz is found to be comparable to those of the same class of power converters based on traditional analog controllers, without the need for some complicated control schemes to compensate for the time delays, and to increase the controller bandwidth. Even more satisfactory results have been obtained for the dynamic load regulation of the digitally controlled converter as compared to its analog counterpart, due to the fact that component tolerances, ageing etc do not affect the digital control parameters, which can be precisely adjusted by software. Further flexibility in control can be achieved as a feature of the digital controller, such as extending the control range of the output voltage over a wide range by easy programming of the converter, without extra hardware requirement. The relatively slow response of the current limit loop against overload obtained in the first phase of this work can also be improved by implementing the pulse-by-pulse current limiting technique on the DSP.

As a further work on this subject, both the input boost type power factor preregulator, and the phase-shifted full-bridge converter can be controlled using the same DSP, thus minimizing the component count with the use of a single digital controller for the overall module, resulting in a more compact design.

The trend in control and monitoring of electronic equipment nowadays is more and more carried out via Internet. Therefore, a further research work in this area would be on the IP (Internet Protocol) - based control of the power supply modules via the Internet.

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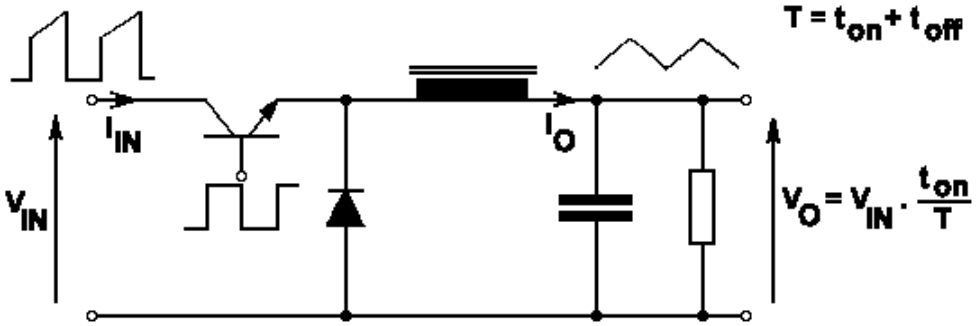
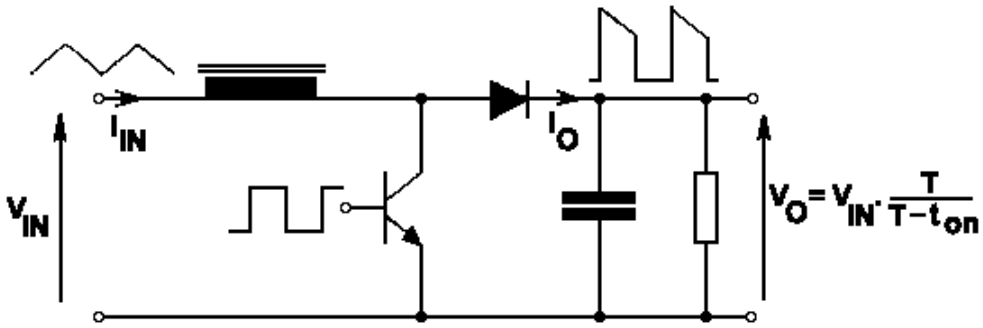
APPENDIX A

THE FAMILY OF SWITCHING REGULATORS

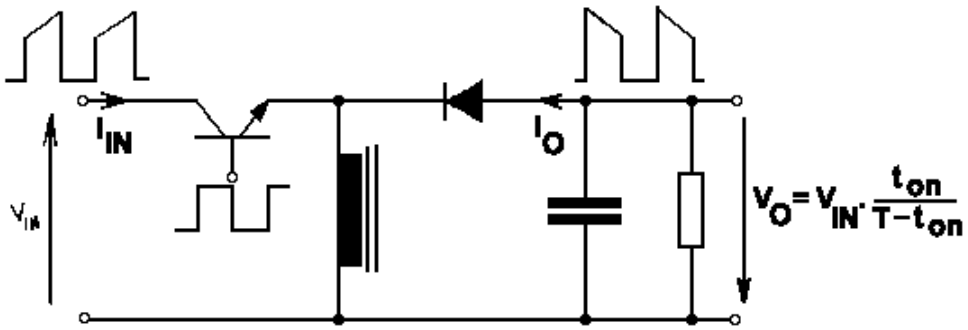
A.1. SINGLE SWITCH NON-ISOLATED SWITCHING REGULATORS



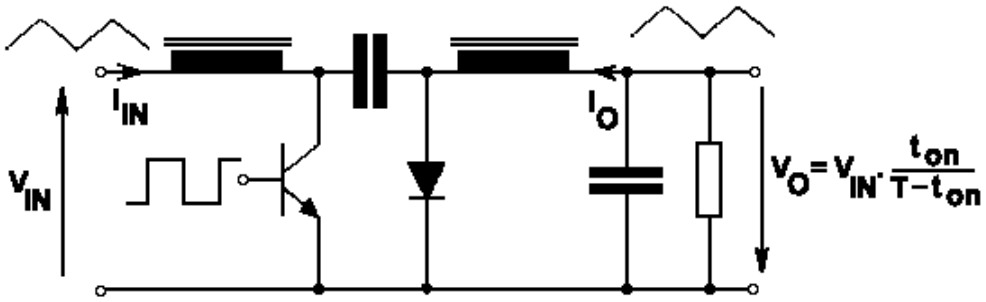
a. Buck Regulator



b. Boost Regulator



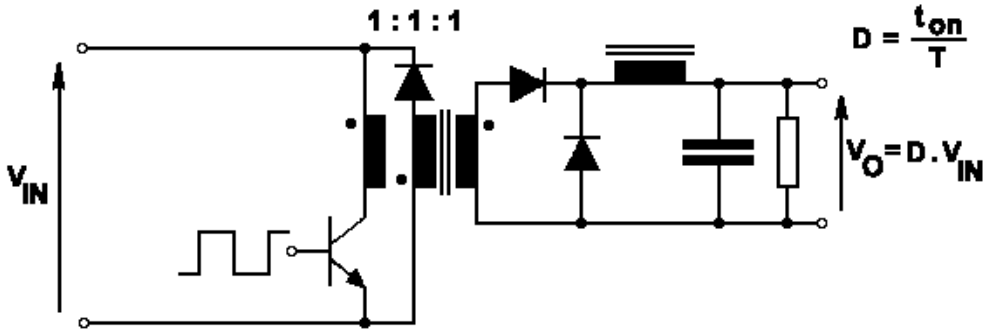
c. Buck-Boost Regulator



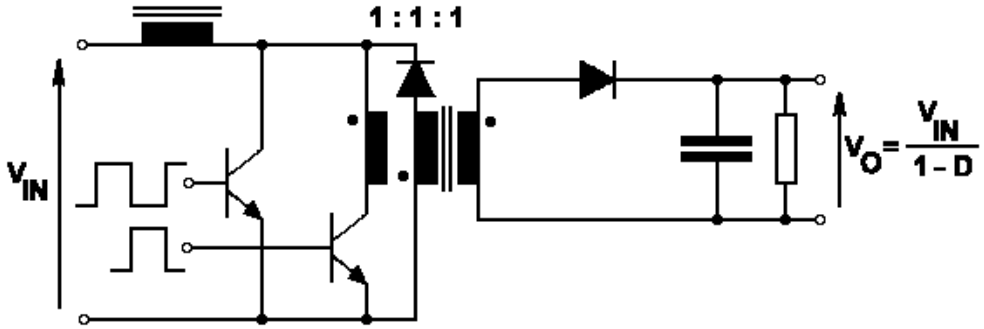
d. Cuk Regulator

Fig.A.1. The Single Switch Non-Isolated Switching Regulator Family

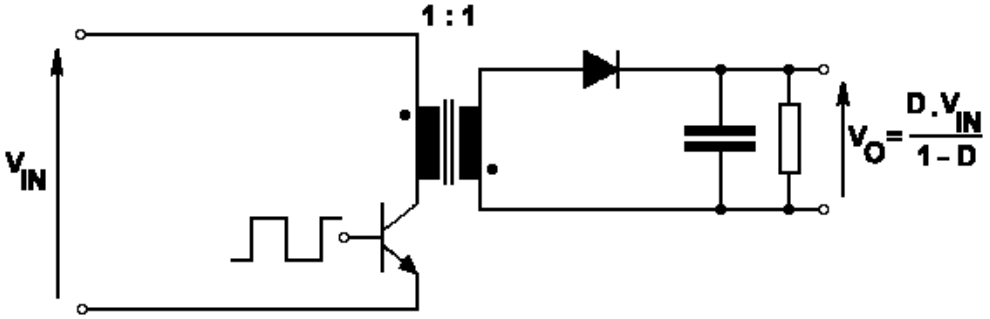
A.2. SINGLE SWITCH ISOLATED SWITCHING REGULATORS



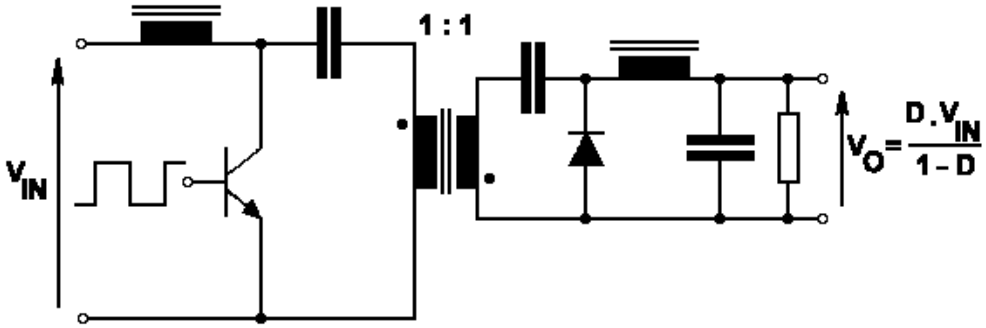
a. Forward Converter



b. Isolated Boost Converter



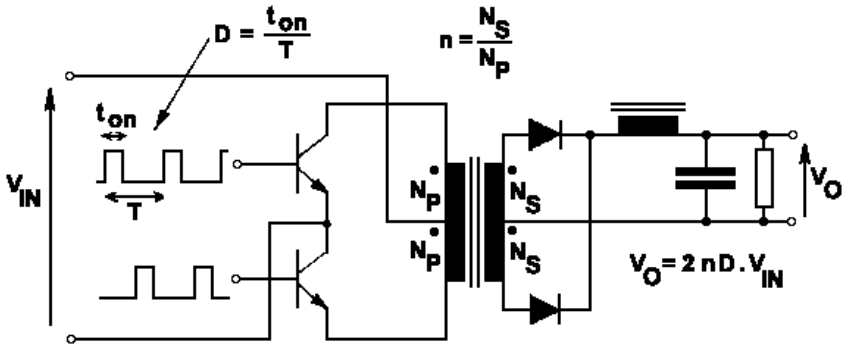
c. Flyback Converter



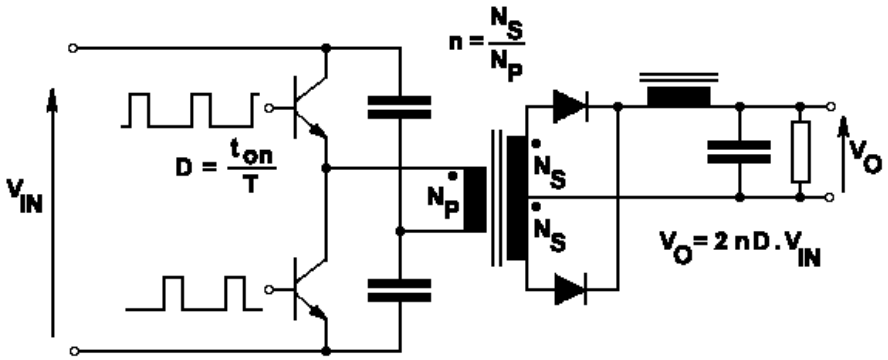
d. Isolated Cuk Converter

Fig.A.2. The Single Transistor Isolated Topology Family

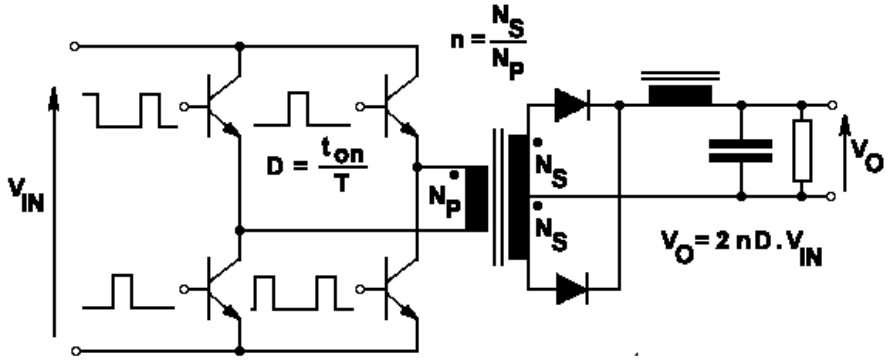
A.3. MULTIPLE SWITCH REGULATORS



a. Push-Pull Converter



b. Half-Bridge Converter



c. Full-Bridge Converter

Fig.A.3. The Multiple Switch Topology Family

APPENDIX B

PHASE SHIFTED ZERO VOLTAGE TRANSITION

B.1. CIRCUIT SCHEMATICS AND DESCRIPTION

The circuit schematic of this technique is shown in Fig.B.1 including voltage and current designations. The basic circuit is comprised of four switches labelled QA through QD and is divided up into two "legs", the right and left hand legs. Each switch is shown shunted by its body diode (DA through DD) and parasitic output capacitance, (CA through CD). These have been identified separately to clarify the exact elements and current paths during the conversion interval [76].

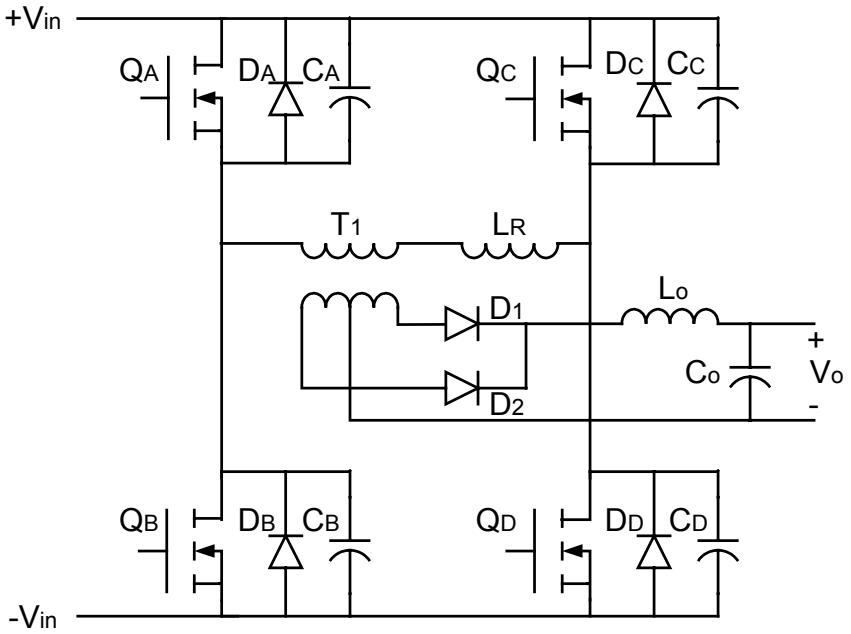


Fig.B.1. The circuit schematic for Phase Shift Operation

B.1.1. Right Leg Resonant Transition Interval (t(0) < t < t(1))

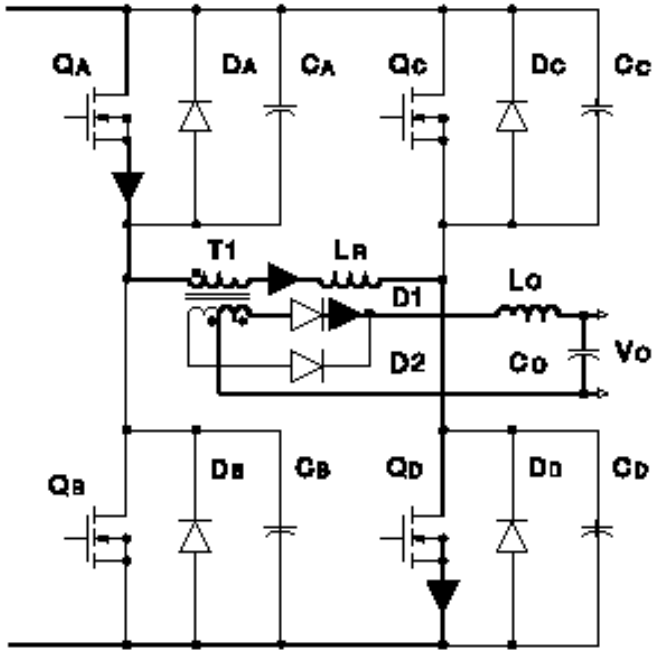


Fig.B.2. Initial Condition (t < t(0)), Q_A = ON , Q_D = ON

The primary current flowing at time t(0) is equal to Ip(t(0)) and was being conducted through the diagonal set of transistors QA in the upper left hand corner of the bridge and transistor QD in the lower right (Fig.B.2). Instantly, at time t(0) switch QD is turned off by the control circuitry which begins the resonant transition of the right hand leg of the converter. The primary current flowing is maintained nearly constant at Ip(t(0)) by the resonant inductance (Lp(res)) of the primary circuit, often referred to as the transformers leakage inductance. Since an external series inductance can be added to alter the effective leakage inductance value, the lumped sum of these inductors will be referred as the resonant inductance, Lr. In a practical application it may be difficult to accurately control the transformers leakage inductance within an acceptable ZVS range, necessitating an external “shim” inductor to control the accuracy. It’s also possible that the transformer leakage inductance can be too

low to provide the desired transition times for the application so an external inductor can be introduced to modify the resonant inductance. With switch QD turned off, the primary current continues to flow using the switch output capacitance, C_{oss} to provide the path. This charges the switch capacitance of QD from essentially zero volts to the upper voltage rail, V_{in} +. Simultaneously, the transformer capacitance (C_{xfmr}) and the output capacitance of switch QC is discharged as its source voltage rises from the lower to the upper rail voltage. This resonant transition positions switch QC with no drain to source voltage prior to turn-on and facilitates lossless, zero voltage switching [76]. (Fig.B.3)

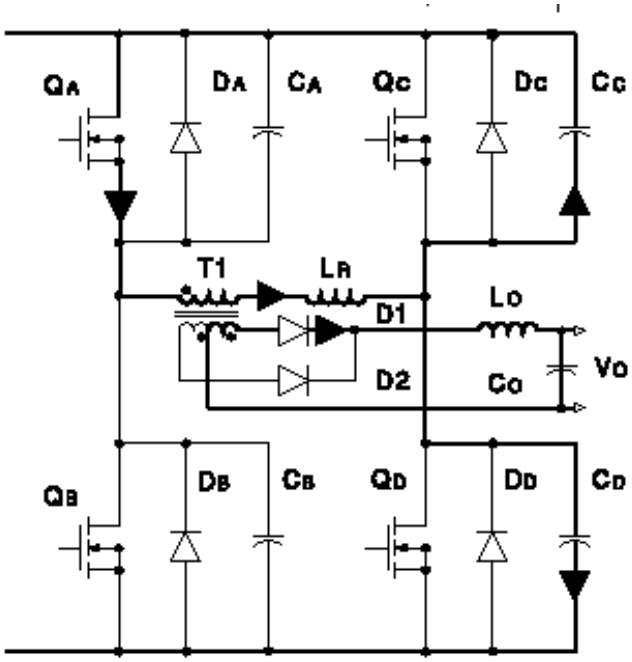


Fig.B.3.Right Leg Transition (t(0) < t < t(1)), Q_A = ON

The primary current causing this right leg transition can be approximated by the full load primary current of IP(t(0)). The small change due to the barely resonant circuit contribution is assumed to be negligible in comparison to the magnitude of the full load current. During this right leg transition the voltage across the transformers primary has decreased from V_{in} to zero. At some point in the transition the primary voltage drops below the reflected secondary voltage,

V_{out}*N. When this occurs the primary is no longer supplying full power to the secondary and the output inductor voltage changes polarity. Simultaneously, energy stored in the output choke begins supplementing the decaying primary power until the primary contribution finally reaches zero. Once the right leg transition has been completed there is no voltage across the transformer primary. Likewise, there is no voltage across the transformers secondary winding and no power transferred, assuming ideal conditions. Note that the resonant transition not only defines the rate of change in primary and secondary voltages dV/dt, but also the rate of change in current in the output filter network, dI/dt [76].

B.1.2.Clamped Freewheeling Interval (t(1) < t < t(2))

Once the right leg transition is complete the primary current free wheels through transistor QA and the body diode of switch QC. The current would remain constant until the next transition occurs assuming that the components were ideal. Switch QC can be turned on at this time which shunts the body diode with the FET Rds(on) switch impedance thus lowering conduction losses. Although current is flowing opposite to the normal convention (source to drain) the channel of QC will conduct and divide the current between the switch and body diode [76]. (Fig.B.4)

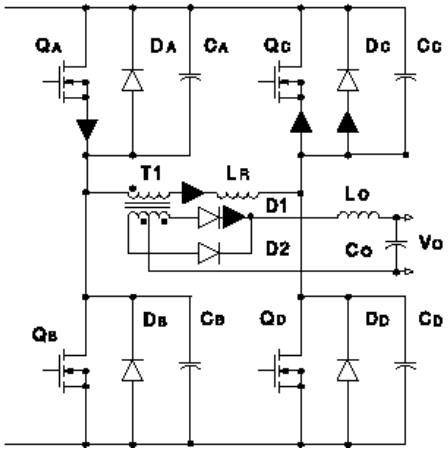


Fig.B.4.Clamped Freewheeling Interval (t(1) < t < t(2))

Q_A = ON, Q_C = ON, D_C = ON

B.1.3.Left Leg Transition (t(2) < t < t(3))

At time t(2) a residual current was flowing in the primary of the transformer which is slightly less than IP(t(0)) due to losses. Switch QC has been previously turned ON and switch QA will now be turned OFF. The primary current will continue to flow but the path has changed to the output capacitance (C_{oss}) of switch QA instead of its channel. The direction of current flowing causes the drain to source voltage of switch QA to increase and lowers its source from the upper to lower rail voltage. Just the opposite conditions have occurred to switch QB which previously had the full input across its terminals. The resonant transition now aligns switch QB with zero voltage across it, enabling lossless switching to occur. Primary current continues to flow and is clamped by the body diode of switch QB, which is still OFF. This clamping into a short circuit is a necessary condition for fixed frequency, zero voltage switching. Once switch QB is turned ON, the transformer primary is placed across the input supply rails since switch QC is already ON and will begin to transfer power. Although zero voltage switching has already been established, turning ON switch QB the instant it reaches zero voltage will cause variable frequency operation [76]. (Fig.B.5)

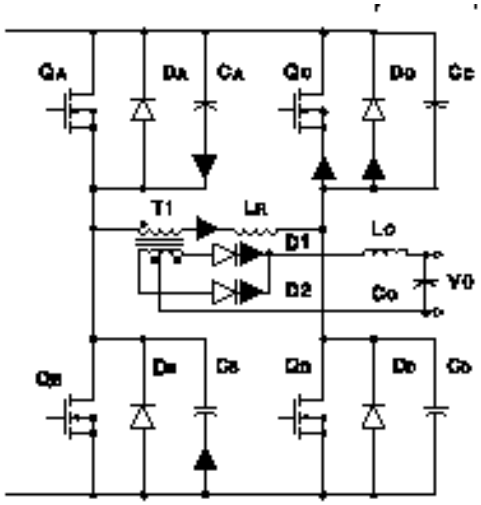


Fig.B.5.Left Leg Transition (t(2) < t < t(3))

$$Q_A = OFF, Q_C = ON, D_C = ON$$

Note that this left leg transition will require more time to complete than the right leg transition. Conduction losses in the primary switches, transformer winding and interconnections result in a net DC voltage drop due to the flowing primary current. Energy stored in the series resonant inductor and magnetizing inductance is no longer ideally clamped to zero voltage. This loss, in addition to the losses incurred during the previous transition, reduce the primary current below its initial (IP(t(0)) value, thus causing a longer left leg transition time than the right leg. Unlike conventional power conversion, one transistor in the diagonal pair of the phase shifted full bridge converter is ON just before power is transferred which simplifies the gate drive. An additional benefit is realized by designating these commutating switches as the high side switches of the converter, usually far more difficult to drive than their lower side counterparts [76].

B.1.4.Power Transfer Interval (t(3) < t < t(4))

Two diagonal switches are ON which applies the full input voltage across the transformer primary. Current rises at a rate determined by V_{in} and the series primary inductance, however starts at a negative value as opposed to zero. The current will increase to a DC level equal to the output current divided by the turns ratio, I_{out}/N. The two time variant contributors to primary current are the magnetizing current (I_{mag}) and the output inductor magnetizing contribution reflected to the primary, L_{out}/N^2 [76]. (Fig.B.6)

B.1.5.Switch Turn Off (t(4))

One switching cycle is concluded at time t(4) when QC the upper right hand corner switch is turned OFF. Current stops flowing in QC's semiconductor channel but continues through the parasitic output capacitance, C_{oss}. This

increases the drain-to- source voltage from essentially zero to the full input supply voltage, Vin. The output capacitance of the lower switch in the left hand leg (QD) is simultaneously discharged via the primary current. Transistor QD is then optimally positioned for zero voltage switching with no drain-to-source voltage. The current during this interval is assumed to be constant, simplifying the analysis. In actuality, it is slightly resonant as mentioned in the right leg transition, but the amplitude is negligible in comparison to the full load current [76].

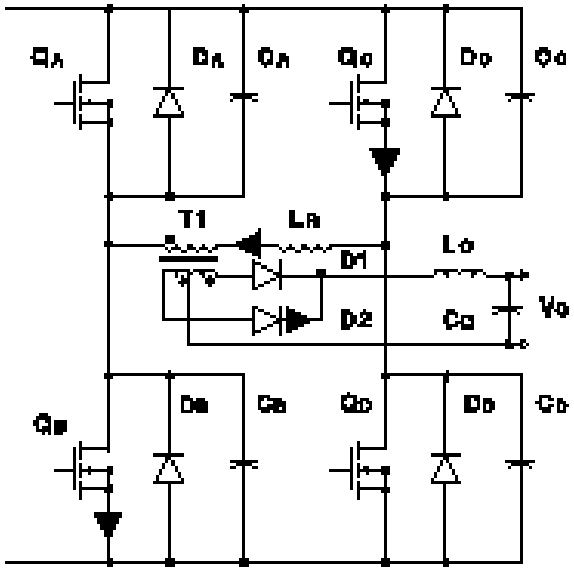


Fig.B.6.Power Transfer Interval (t(3) < t < t(4))

Q_B = ON, Q_C = ON

B.2. RESONANT CIRCUIT PARAMETERS

Two conditions must be met by the resonant circuit at light load, and both relate to the energy stored in the resonant inductor.

1. There must be enough inductive energy stored to drive the resonant capacitors to the opposite supply rail.

2. This transition must be accomplished within the allocated transition time.

Lossy, non-zero voltage switching will result if either, or both are violated. The first condition will always be met when the latter is used as the resonant circuit limitation.

The stored inductive energy requirement and specified maximum transition time have also defined the resonant frequency (W_r) of the tank circuit. Elements of this tank are the resonant inductor (L_r) and capacitor (C_r), formed by the two switch output capacitors, also in parallel with the transformer primary capacitance C_{xfmr}. The maximum transition time cannot exceed one-fourth of the self resonant period, (four times the self resonant frequency) to satisfy the zero voltage switching condition [76].

The resonant tank frequency, W_r :

$$W_r = \frac{1}{\sqrt{L_r \times C_r}} \tag{B.1}$$

$$t(max)transition = \frac{\pi}{2 \times W_r} \tag{B.2}$$

C_{oss}, the specified MOSFET switch output capacitance will be multiplied by a 4/3 factor to accommodate the increase caused by high voltage operation. During each transition, two switch capacitances are driven in parallel, doubling the total capacitance to 8/3 x C_{oss}. Transformer capacitance (C_{xfmr}) must also be added as it is not negligible in many high frequency applications.

The resonant capacitance, C_r :

$$C_r = \left[\left(\frac{8}{3}C_{oss}\right) + C_{xfmr}\right] \tag{B.3}$$

The capacitive energy required to complete the transition , $W(C_r)$ is:

$$W(C_r) = \frac{1}{2} \times C_r \times V_{pri}^2 \tag{B.4}$$

This energy can also be expressed as:

$$W(C_r) = \frac{1}{2} \times \left[\left(\frac{8}{3}C_{oss}\right) + C_{xfmr}\right] \times V_{pri}^2 \tag{B.5}$$

The energy stored in the resonant inductance must be greater than the energy required to charge and discharge the FET output and transformer capacitances of the leg in transition within the maximum transition time. Inside the transformer, all of the energy is stored in the leakage inductance since the secondary current has clamped the transformers primary voltage to essentially zero. This causes high circulating primary current in the physical winding but has no effect on the stored energy used to perform the ZVS transition.

The energy stored in the resonant inductor, L_r:

$$W(L_r) = \frac{1}{2} \times L_r \times I_{pri}^2 \tag{B.6}$$

The resonant tank frequency must be at least four times higher than the transition time to fully resonate within the maximum transition time t(max) at light load.

$$T_{res} = 4 \times t(max) \tag{B.7}$$

$$W_r = 2 \times \pi \times F_{res} = \frac{2 \times \pi}{T_{res}} \tag{B.8}$$

Reorganizing and combining these relationships;

$$W_r = \frac{\pi}{2 \times t(max)} \tag{B.9}$$

The resonant radian frequency (W_r) is related to the resonant components by the equation:

$$W_r = \frac{1}{\sqrt{L_r \times C_r}} \tag{B.10}$$

Both sides of this can be squared to simplify the calculations and reorganized to solve for the exact resonant inductor value.

$$L_r = \frac{1}{W_r^2 \times C_r} \tag{B.11}$$

Previously outlined relationships for W_r and C_r can be introduced to result in the following specific equation.

$$L_r = \frac{1}{\left[\frac{\pi}{2 \times t(max)}\right]^2 \times \left[\left(\frac{8}{3} \times C_{oss}\right) + C_{xfmr}\right]} \tag{B.12}$$

The energy stored in the resonant inductor must be greater than the capacitive energy required for the transition to occur within the allocated transition time. The governing equations are summarized below.

$$\frac{1}{2}\times L_r \times I_{pri}^2(\min) > \frac{1}{2}\times C_r \times V_{in}^2(\max) \tag{B.13}$$

The minimum primary current required for the phase shifted application can now be determined by reorganizing Eq.2.13.

$$I_{pri}(\min) = \sqrt{\frac{C_r \times V_{in}^2}{L_r}} \tag{B.14}$$

B.3. ZVS IN THE IMPLEMENTED SYSTEM

In the implemented system, IRFP460 MOSFETs are used as the switching element in the full bridge. The output capacitance for the IRFP460 is 470pF(C_{oss}) [77]. The turns ratio for the transformer is 3.5. The leakage inductance of the transformer is 22μH and the capacitance is 50pF. Therefore :

C_{oss} : 470 pF
C_{xfmr} : 50 pF
N : 3.5
L_r : 22μH (B.15)

The resonant capacitor can be calculated by Eq.B.3.

$$C_r = \left[\left(\frac{8}{3}C_{oss}\right) + C_{xfmr}\right] = \left[\left(\frac{8}{3}\times 470\times 10^{-12}\right) + 50^{-12}\right] = 1303\text{pF} \tag{B.16}$$

The minimum primary current required for the phase shifted application can be determined by applying Eq.B.14 to the values given in Eq.B.15 and B.16.

$$I_{pri}(\min) = \sqrt{\frac{C_r \times V_{in}^2}{L_r}} = \sqrt{\frac{1303\times 10^{-12}\times 400^2}{22\times 10^{-6}}} = 3\text{A} \tag{B.17}$$

The 3A primary corresponds to 10.5A load current. This means the zero voltage switching will occur for the load currents greater then 10A. This is a satisfactory result. In this way, ZVS operation down to about 1/3 of full load is achieved. Even though the total losses increases below this point, the total losses are much less than at full load.

The resonant frequency can be calculated by Eq.B.11.

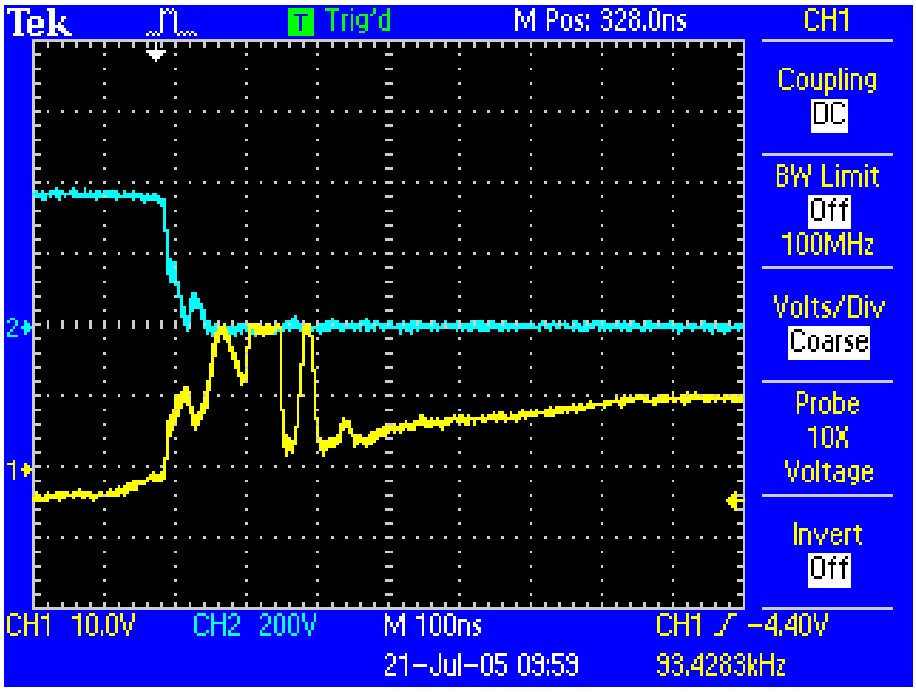
$$W_r = \frac{1}{\sqrt{L_r \times C_r}} = \frac{1}{\sqrt{22 \times 10^{-6} \times 1303 \times 10^{-12}}} = 5.9\text{MHz} \qquad \text{(B.18)}$$

By reorganizing Eq.B.9, the max time required for ZVS can be calculated as follows:

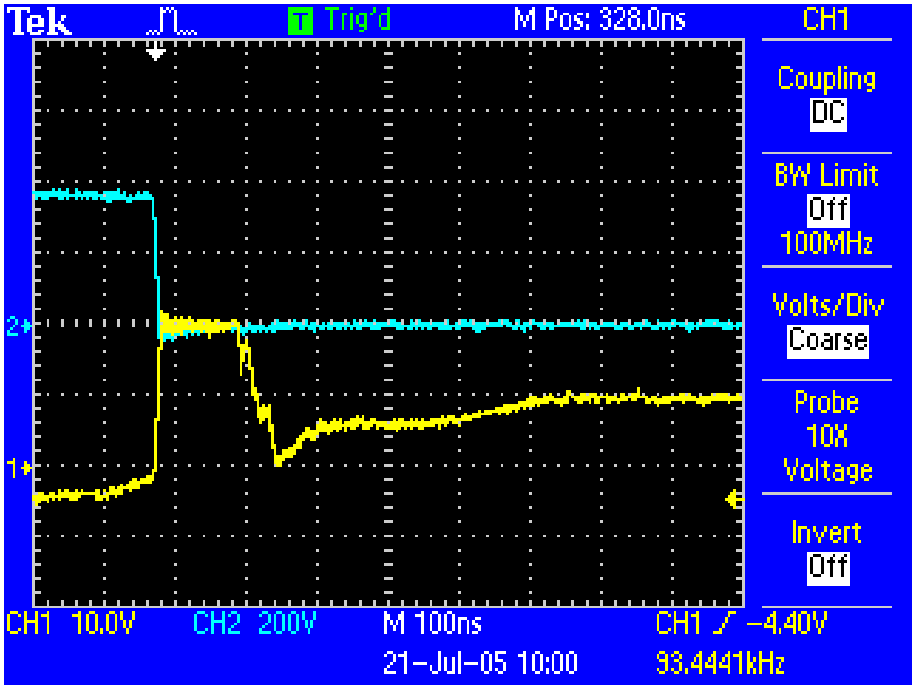
$$t(\max) = \frac{\pi}{2 \times W_r} = 0.266\mu\,\text{sec}. \qquad \text{(B.19)}$$

This duration corresponds to 2% duty cycle for 75kHz switching frequency (0.266μsec/13.3μsec). In the application, 0.665μsec (=5% duty cycle) is reserved for ZVS to occur which is satisfactory result.

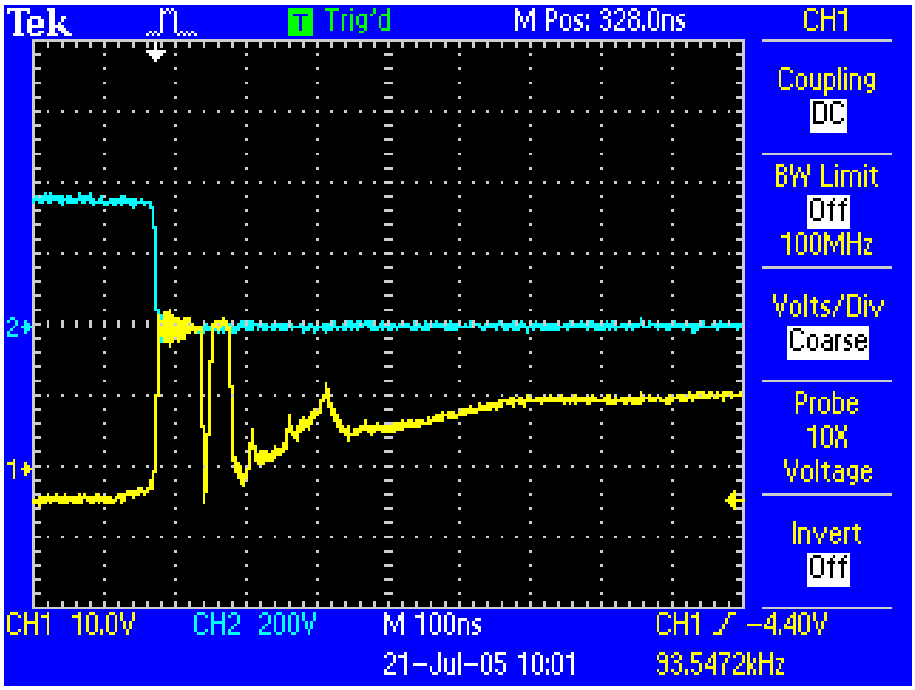
In Fig.B.7 and Fig.B.8, the Drain-Source (V_{DS}) and Gate-Source (C_{GS}) voltage waveforms are given for different load currents for Q_C and Q_D (Fig. B.1), respectively. It is clearly seen from the waveforms that above 10A the ZVS operation is successfully achieved.



(a) at 5A load current

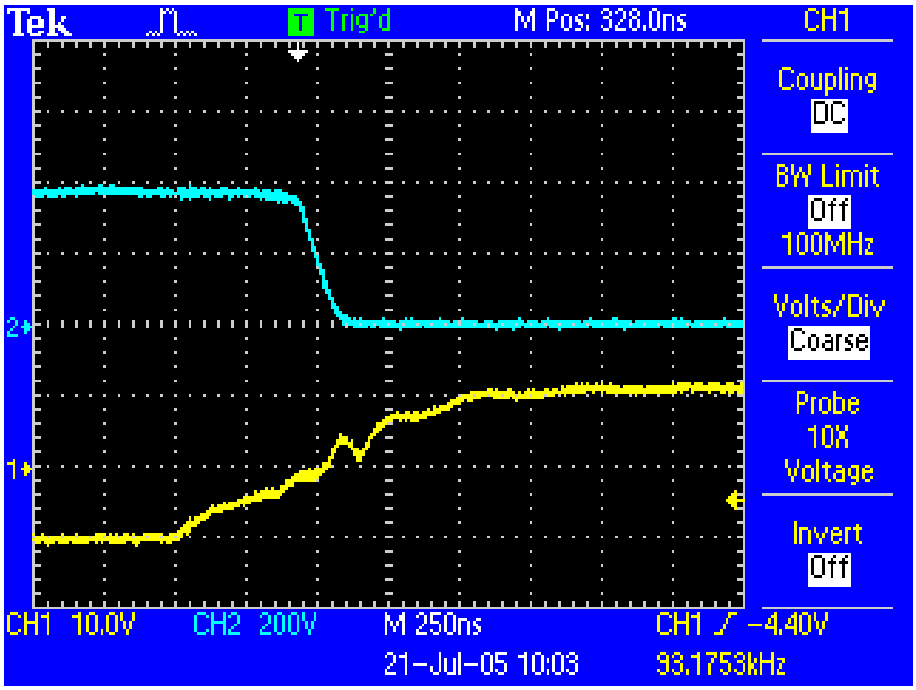


(b) at 10A load current

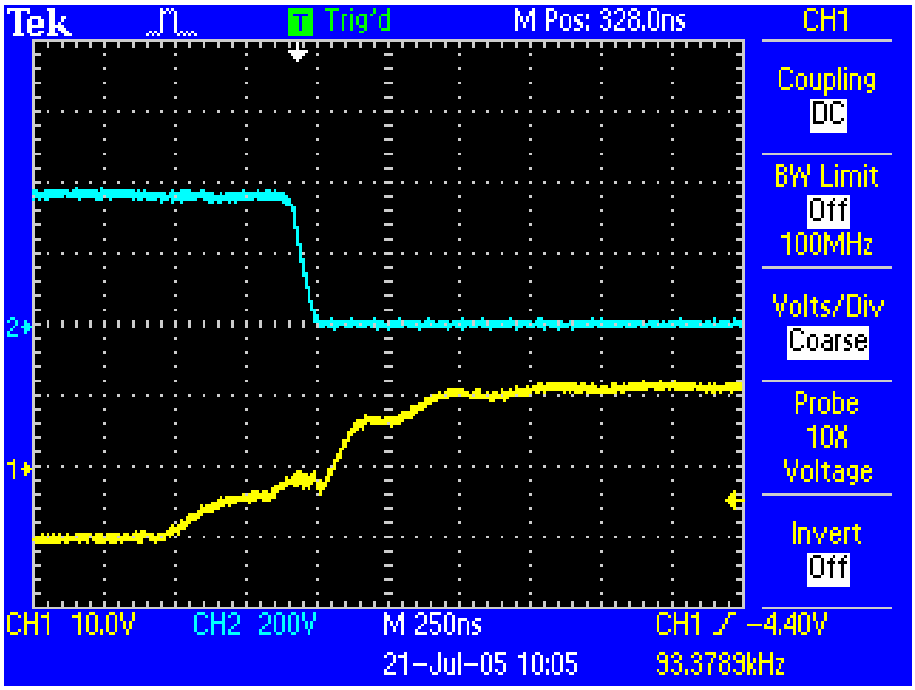


(c) at 25A load current

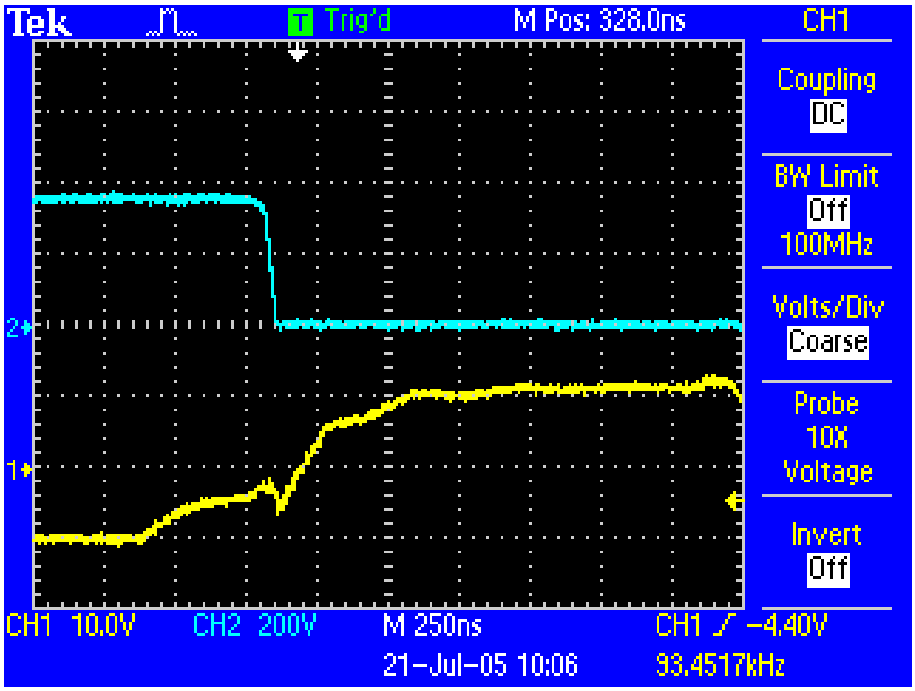
Fig.B.7. V_{DS} and V_{GS} voltage waveforms for high side switch (Q_C)



(a) at 5A load current



(b) at 10A load current



(c) at 25A load current

Fig.B.8. V_{DS} and V_{GS} voltage waveforms for low side switch (Q_D)

APPENDIX C

APPLICATIONS OF THE IMPLEMENTED SYSTEM IN THE FIELD

- Show TV
- Headquarter of Vakıflar Bank
- Kurtköy Airport
- Headquarter of Ceylan Holding
- Doğan Holding-Hürriyet
- General Directorate of Forests in Turkey
- UPS
- Çelebi IC Antalya Airport 2. International Terminal
- Antalya Sun Gate Port Royal Resort Hotel
- Ihlas Armutlu Resort Hotel
- Istanbul Metropolitan Municipality
- ATV
- Dalaman Airport
- State Planning Organization (DPT)
- Ege University
- Ege University Medicine Faculty
- Mersin University
- İstanbul Hyatt Regiency Hotel
- Konya Meram Medicine Faculty
- Mavi Jeans
- Oyak Bank Söğütözü
- Sanko

- TTK (6 different enterprise)
- TürkSAT
- Yapı Kredi İzmir Regional Office
- Besler
- İstanbul İsviçre Hospital
- TUBITAK-UME
- Kosifler Oto
- Akkanat Holding
- Sirene Golf Hotel
- TKI

APPENDIX D

NEC uPD78F0058 DATASHEET

DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78F0058,78F0058Y

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD78F0058 is a product of the μPD780058 Subseries in the 78K/0 Series and equivalent to the μPD780058 with a flash memory in place of internal ROM. This device is incorporated with a flash memory which can be programmed without being removed from the substrate.

The μPD78F0058Y is a products based on the μPD78F0058, with an I²C bus interface supporting multimaster.

Functions are described in detail in the following user's manuals, which should be read when carrying out design work.

μPD780058, 780058Y Subseries User's Manual :U12013E
78K/0 Series User's Manual Instruction :U12326E

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Flash memory : 60 Kbytes[Note 1]
- Internal high-speed RAM : 1024 bytes
- Internal expansion RAM : 1024 bytes[Note 2]
- Buffer RAM : 32 bytes
- Power supply voltage : V_{DD} = 2.7 to 5.5 V

Notes 1. The flash memory capacity can be changed with the memory size switching register (IMS).

2. The internal expansion RAM capacity can be changed with the internal expansion RAM size switching register (IXS).

Remark For the differences between the flash memory versions and the mask ROM versions, refer to **1. DIFFERENCES BETWEEN μPD78F0058, 78F0058Y, AND MASK ROM VERSION.**

APPLICATION FIELDS

Car audio systems, cellular phones, pagers, printers, AV equipment, cameras, PPCs, vending machines, etc.

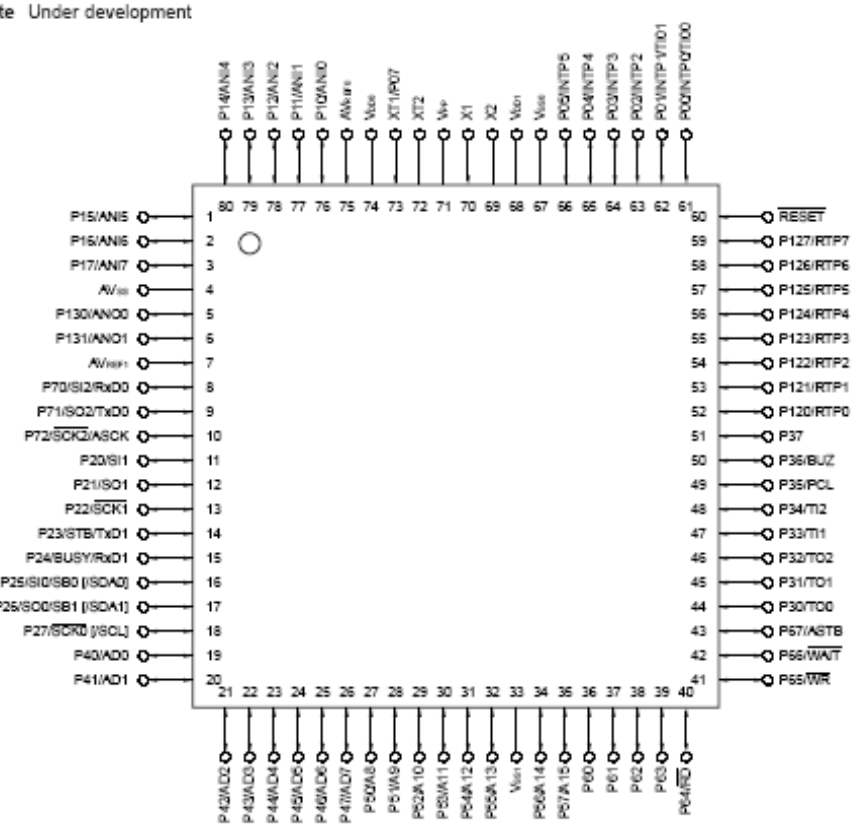
OVERVIEW OF FUNCTIONS

Item \ Product Name		μPD78F0058	μPD78F0058Y
Internal memory	Flash memory	60 Kbytes	
	High-speed RAM	1,024 bytes	
	Buffer RAM	32 bytes	
	Expanded RAM	1,024 bytes	
Memory space		64 Kbytes	
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@5.0 MHz operation)	
	When subsystem clock is selected	122 μs (@32.768 kHz operation)	
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.	
I/O ports		Total: 68 • CMOS input: 2 • CMOS I/O: 62 • N-ch open-drain I/O: 4	
A/D converter		• 8-bit resolution × 8 channels (V_{DD} = 2.7 to 5.5 V)	
D/A converter		• 8-bit resolution × 2 channels (V_{DD} = 2.7 to 5.5 V)	
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selectable: 1 channel	• 3-wire serial I/O/2-wire serial I/O/I^2C mode selectable: 1 channel
		• 3-wire serial I/O mode (automatic data transmit/receive function for up to 32 bytes provided on chip): 1 channel • 3-wire/serial I/O/UART mode (time division transfer function provided on chip) selectable: 1 channel	
Timers		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel	
Timer outputs		3 (14-bit PWM output × 1)	
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (@5.0 MHz operation with main system clock) 32.768 kHz (@32.768 kHz operation with subsystem clock)	
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (@5.0 MHz operation with main system clock)	
Vectored interrupt sources	Maskable	Internal: 13, External: 6	
	Non-maskable	Internal: 1	
	Software	1	
Test inputs		Internal: 1, External: 1	
Supply voltage		V_{DD} = 2.7 to 5.5 V	
Operating ambient temperature		T_A = −40 to +85°C	
Package		• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.0 mm)	

1. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (14 × 14 mm)**
  μPD78F0058GC-8BT, 78F0058YGC-8BT
- **80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm)**
  μPD78F0058GK-BE9, 78F0058YGK-BE9
- ★ **80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.0 mm)**
  μPD78F0058GK-9EU[Note], 78F0058YGK-9EU[Note]

Note Under development



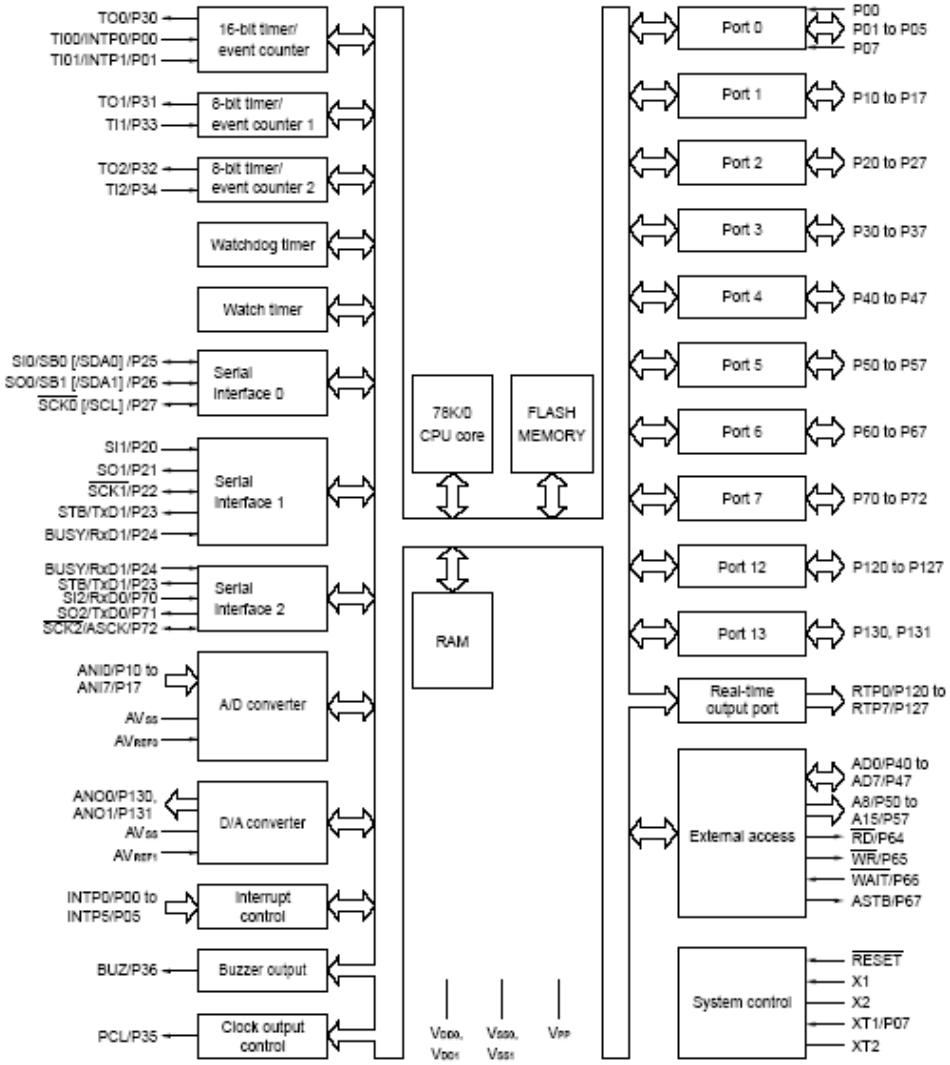
Cautions 1. Connect the V_{PP} pin directly to V_{SS0} or V_{SS1} in normal operation mode.

2. Connect the AV_{SS} pin to V_{SS0}.

PIN IDENTIFICATION

A8 to A15	: Address Bus	$\overline{RD}$	: Read Strobe
AD0 to AD7	: Address/Data Bus	$\overline{RESET}$	: Reset
ANI0 to ANI7	: Analog Input	RTP0 to RTP7	: Real-Time Output Port
ANO0, ANO1	: Analog Output	RxD0, RxD1	: Receive Data
ASCK	: Asychronous Serial Clock	SB0, SB1	: Serial Bus
ASTB	: Address Strobe	$\overline{SCK0}$ to $\overline{SCK2}$	: Serial Clock
AV_{REF0}, AV_{REF1}	: Analog Reference Voltage	SCL	: Serial Clock
AV_{SS}	: Analog Ground	SDA0, SDA1	: Serial Data
BUSY	: Busy	SI0 to SI2	: Serial Input
BUZ	: Buzzer Clock	SO0 to SO2	: Serial Output
INTP0 to INTP5	: Interrupt from Peripherals	STB	: Strobe
P00 to P05, P07	: Port 0	TI00, TI01	: Timer Input
P10 to P17	: Port 1	TI1, TI2	: Timer Input
P20 to P27	: Port 2	TO0 to TO2	: Timer Output
P30 to P37	: Port 3	TxD0, TxD1	: Transmit Data
P40 to P47	: Port 4	V_{DD0}, V_{DD1}	: Power Supply
P50 to P57	: Port 5	V_{PP}	: Programming Power Supply
P60 to P67	: Port 6	V_{SS0}, V_{SS1}	: Ground
P70 to P72	: Port 7	$\overline{WAIT}$	: Wait
P120 to P127	: Port 12	$\overline{WR}$	: Write Strobe
P130, P131	: Port 13	X1, X2	: Crystal (Main System Clock)
PCL	: Programmable Clock	XT1, XT2	: Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



4.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0 7-bit input/output port	Input only	Input	INTP0/TI00
P01	I/O		Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P07[Note 1]	Input		Input only	Input	XT1
P10 to P17	I/O	Port 1 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software[Note 2].		Input	ANI0 to ANI7
P20	I/O	Port 2 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB/TxD1
P24					BUSY/RxD1
P25					SI0/SB0 [/SDA0]
P26					SO0/SB1 [/SDA1]
P27					$\overline{SCK0}$ [/SCL]
P30	I/O	Port 3 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					–
P40 to P47	I/O	Port 4 8-bit input/output port Input/output can be specified in 8-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. The test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

4.1 Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P50 to P57	I/O	Port 5 8-bit input/output port LEDs can be driven directly. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	A8 to A15
P60	I/O	Port 6 8-bit input/outport port Input/output can be specified in 1-bit units.	N-ch open-drain input/output port LEDs can be driven directly.	Input	–
P61					
P62					
P63					
P64			When used as an input port, an on-chip pull-up resistor can be specified by means of software.		$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	I/O	Port 7 3-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	SI2/RxD0
P71					SO2/TxD0
P72					$\overline{SCK2}$/ASCK
P120 to P127	I/O	Port 12 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistor can be specified by means of software.		Input	RTP0 to RTP7
P130, P131	I/O	Port 13 2-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	ANO0, ANO1

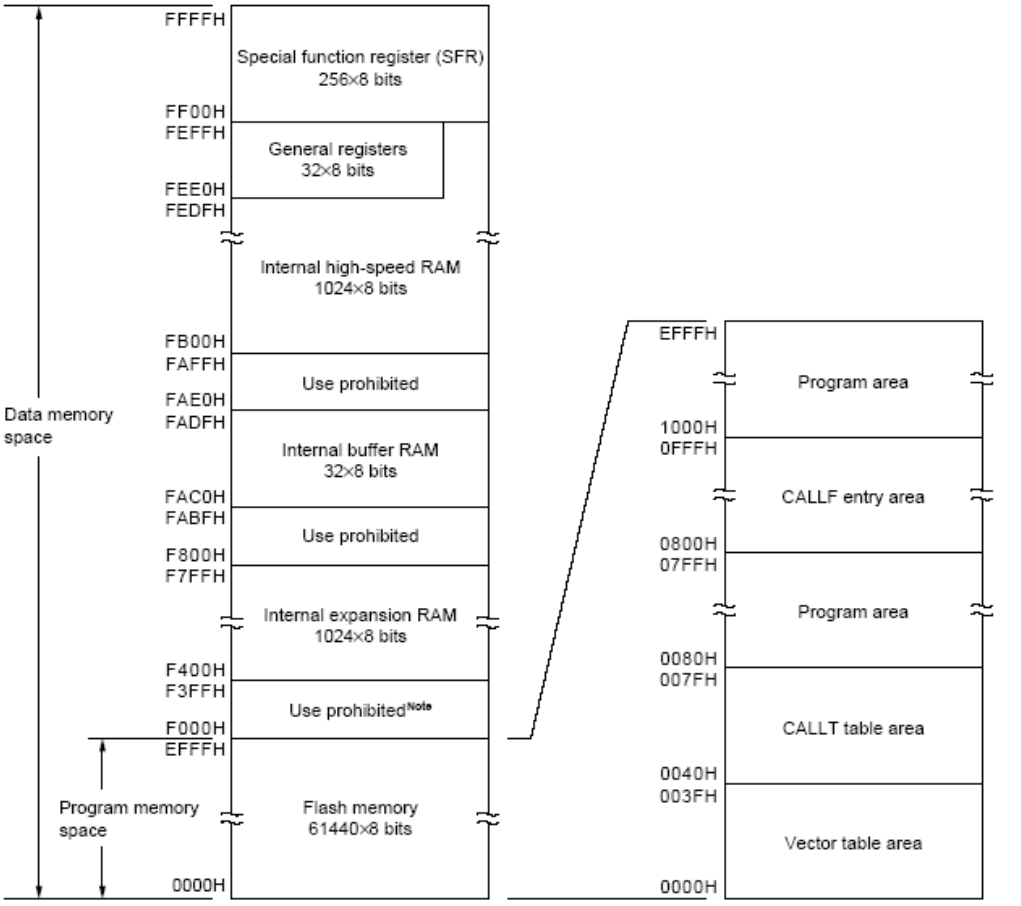
4.2 Non-Port Pins (1/2)

	Pin Name	I/O	Function	After Reset	Alternate Function
	INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising edge and falling edges) can be specified.	Input	P00/TI00
	INTP1				P01/TI01
	INTP2				P02
	INTP3				P03
	INTP4				P04
	INTP5				P05
	SI0	Input	Serial interface serial data input	Input	P25/SB0 [/SDA0]
	SI1				P20
	SI2				P70/RxD
	SO0	Output	Serial interface serial data output	Input	P26/SB1 [/SDA1]
	SO1				P21
	SO2				P71/TxD
	SB0	I/O	Serial interface serial data input/output	Input	P25/SI0 [/SDA0]
	SB1				P26/SO0 [/SDA1]
★	SDA0		μPD78F0058Y only		P25/SI0/SB0
★	SDA1				P26/SO0/SB1
	$\overline{SCK0}$	I/O	Serial interface serial clock input/output	Input	P27 [/SCL]
	$\overline{SCK1}$				P22
	$\overline{SCK2}$				P72/ASCK
★	SCL		μPD78F0058Y only		P27/$\overline{SCK0}$
	STB	Output	Serial interface automatic transmit/receive strobe output	Input	P23/TxD1
	BUSY	Input	Serial interface automatic transmit/receive busy input	Input	P24/RxD1
	RxD0	Input	Asynchronous serial interface serial data input	Input	P70/SI2
	RxD1				P24/BUSY
	TxD0	Output	Asynchronous serial interface serial data output	Input	P71/SO2
	TxD1				P23/STB
	ASCK	Input	Asynchronous serial interface serial clock input	Input	P72/$\overline{SCK2}$
	TI00	Input	External count clock input to the 16-bit timer (TM0)	Input	P00/INTP0
	TI01		Capture trigger signal input to the capture register (CR00)		P01/INTP1
	TI1		External count clock input to the 8-bit timer (TM1)		P33
	TI2		External count clock input to the 8-bit timer (TM2)		P34
	TO0	Output	16-bit timer (TM0) output (also used for 14-bit PWM output)	Input	P30
	TO1		8-bit timer (TM1) output		P31
	TO2		8-bit timer (TM2) output		P32
	PCL	Output	Clock output (for trimming of main system clock and subsystem clock)	Input	P35
	BUZ	Output	Buzzer output	Input	P36
	RTP0 to RTP7	Output	Real-time output port from which data is output in synchronization with a trigger	Input	P120 to P127
	AD0 to AD7	I/O	Lower address/data bus for expanding memory externally	Input	P40 to P47

4.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
A8 to A15	Output	Higher address bus for expanding memory externally	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for reading from external memory	Input	P64
$\overline{WR}$		Strobe signal output for writing to external memory		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input (also used for analog power supply)	–	–
AV_{REF1}	Input	D/A converter reference voltage input	–	–
AV_{SS}	–	A/D converter and D/A converter ground potential Use at the same potential as V_{SS0}.	–	–
$\overline{RESET}$	Input	System reset input	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	Input	P07
XT2	–		–	–
V_{DD0}	–	Port block positive power supply	–	–
V_{SS0}	–	Port block ground potential	–	–
V_{DD1}	–	Positive power supply (except for port and analog blocks)	–	–
V_{SS1}	–	Ground potential (except for port and analog blocks)	–	–
V_{PP}	–	Setting flash memory programming mode. Applying high voltage for program write/verify. Connect directly to V_{SS0} or V_{SS1} in normal operation mode.	–	–

Figure 5-1. Memory Map



APPENDIX E

TEXAS INSTRUMENTS TMS320F2812 DATASHEET

3.2 Brief Descriptions

3.2.1 C28x CPU

The C28x™ DSP generation is the newest member of the TMS320C2000™ DSP platform. The C28x is source code compatible to the 24x/240x DSP devices, hence existing 240x users can leverage their significant software investment. Additionally, the C28x is a very efficient C/C++ engine, hence enabling users to develop not only their system control software in a high-level language, but also enables math algorithms to be developed using C/C++. The C28x is as efficient in DSP math tasks as it is in system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC capabilities of the C28x and its 64-bit processing capabilities, enable the C28x to efficiently handle higher numerical resolution problems that would otherwise demand a more expensive floating-point processor solution. Add to this the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The C28x has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables the C28x to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

C28x and TMS320C2000 are trademarks of Texas Instruments.

1 Features

- High-Performance Static CMOS Technology
  - 150 MHz (6.67-ns Cycle Time)
  - Low-Power (1.8-V Core, 3.3-V I/O) Design
  - 3.3-V Flash Programming Voltage
- JTAG Boundary Scan Support†
- High-Performance 32-Bit CPU (TMS320C28x)
  - 16 x 16 and 32 x 32 MAC Operations
  - 16 x 16 Dual MAC
  - Harvard Bus Architecture
  - Atomic Operations
  - Fast Interrupt Response and Processing
  - Unified Memory Programming Model
  - 4M Linear Program Address Reach
  - 4M Linear Data Address Reach
  - Code-Efficient (in C/C++ and Assembly)
  - TMS320F24x/LF240x Processor Source Code Compatible
- On-Chip Memory
  - Up to 128K x 16 Flash (Four 8K x 16 and Six 16K x 16 Sectors)
  - 1K x 16 OTP ROM
  - L0 and L1: 2 Blocks of 4K x 16 Each Single-Access RAM (SARAM)
  - H0: 1 Block of 8K x 16 SARAM
  - M0 and M1: 2 Blocks of 1K x 16 Each SARAM
- Boot ROM (4K x 16)
  - With Software Boot Modes
  - Standard Math Tables
- External Interface (F2812)
  - Up to 1M Total Memory
  - Programmable Wait States
  - Programmable Read/Write Strobe Timing
  - Three Individual Chip Selects
- Clock and System Control
  - Dynamic PLL Ratio Changes Supported
  - On-Chip Oscillator
  - Watchdog Timer Module
- Three External Interrupts
- Peripheral Interrupt Expansion (PIE) Block That Supports 45 Peripheral Interrupts
- 128-Bit Security Key/Lock
  - Protects Flash/OTP and L0/L1 SARAM
  - Prevents Firmware Reverse Engineering
- Three 32-Bit CPU-Timers
- Motor Control Peripherals
  - Two Event Managers (EVA, EVB)
  - Compatible to 240xA Devices
- Serial Port Peripherals
  - Serial Peripheral Interface (SPI)
  - Two Serial Communications Interfaces (SCIs), Standard UART
  - Enhanced Controller Area Network (eCAN)
  - Multichannel Buffered Serial Port (McBSP) With SPI Mode
- 12-Bit ADC, 16 Channels
  - 2 x 8 Channel Input Multiplexer
  - Two Sample-and-Hold
  - Single/Simultaneous Conversions
  - Fast Conversion Rate: 80 ns/12.5 MSPS
- Up to 56 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins
- Advanced Emulation Features
  - Analysis and Breakpoint Functions
  - Real-Time Debug via Hardware
- Development Tools Include
  - ANSI C/C++ Compiler/Assembler/Linker
  - Supports TMS320C24x™/240x Instructions
  - Code Composer Studio™ IDE
  - DSP/BIOS™
  - JTAG Scan Controllers† [Texas Instruments (TI) or Third-Party]
  - Evaluation Modules
  - Broad Third-Party Digital Motor Control Support
- Low-Power Modes and Power Savings
  - IDLE, STANDBY, HALT Modes Supported
  - Disable Individual Peripheral Clocks
- Package Options
  - 179-Ball MicroStar BGA™ With External Memory Interface (GHH) (F2812)
  - 176-Pin Low-Profile Quad Flatpack (LQFP) With External Memory Interface (PGF) (F2812)
  - 128-Pin LQFP Without External Memory Interface (PBK) (F2810)
- Temperature Options:
  - A: –40°C to 85°C (GHH, PGF, PBK)
  - S: –40°C to 125°C (GHH, PGF, PBK)

TMS320C24x, Code Composer Studio, DSP/BIOS, and MicroStar BGA are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.
† IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port

ADVANCE INFORMATION

2.2 Device Summary

Table 2–1 provides a summary of each device's features.

Table 2–1. Hardware Features†

FEATURE		F2810	F2812
Instruction Cycle (at 150 MHz)		6.67 ns	6.67 ns
Single-Access RAM (SARAM) (16-bit word)		18K	18K
3.3-V On-Chip Flash (16-bit word)		64K	128K
Code Security for On-Chip Flash/SARAM		Yes	Yes
Boot ROM		Yes	Yes
OTP ROM		Yes	Yes
External Memory Interface		—	Yes
Event Managers A and B (EVA and EVB)		EVA, EVB	EVA, EVB
+ General-Purpose (GP) Timers		4	4
+ Compare (CMP)/PWM		16	16
+ Capture (CAP)/QEP Channels		6/2	6/2
Watchdog Timer		Yes	Yes
12-Bit ADC		Yes	Yes
+ Channels		16	16
32-Bit CPU Timers		3	3
SPI		Yes	Yes
SCIA, SCIB		SCIA, SCIB	SCIA, SCIB
CAN		Yes	Yes
McBSP		Yes	Yes
Digital I/O Pins (Shared)		56	56
External Interrupts		3	3
Supply Voltage		1.8-V Core, 3.3-V I/O	1.8-V Core, 3.3-V I/O
Packaging		128-pin PBK	179-ball GHH 176-pin PGF
Temperature Options‡	A: –40°C to 85°C	PBK	PGF and GHH
	S: –40°C to 125°C	Available at TMS only	Available at TMS only
Product Status§ Product Preview (PP) Advance Information (AI) Production Data (PD)		AI (TMP¶)	AI (TMP¶)

† The errata for this silicon, *TMS320F2810 and TMS320F2812 Digital Signal Processors Silicon Errata* (literature number SPRZ193), has been posted on the Texas Instruments (TI) website. It will be updated as needed.

‡ "S" temperature option (–40°C to 125°C) characterization data will be available at TMS.

§ PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.
ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

¶ TMP: Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

ADVANCE INFORMATION

2.3.2 Pin Assignments for the PGF Package

The TMS320F2812 176-pin PGF low-profile quad flatpack (LQFP) pin assignments are shown in Figure 2–2. See Table 2–2 for a description of each pin's function(s).

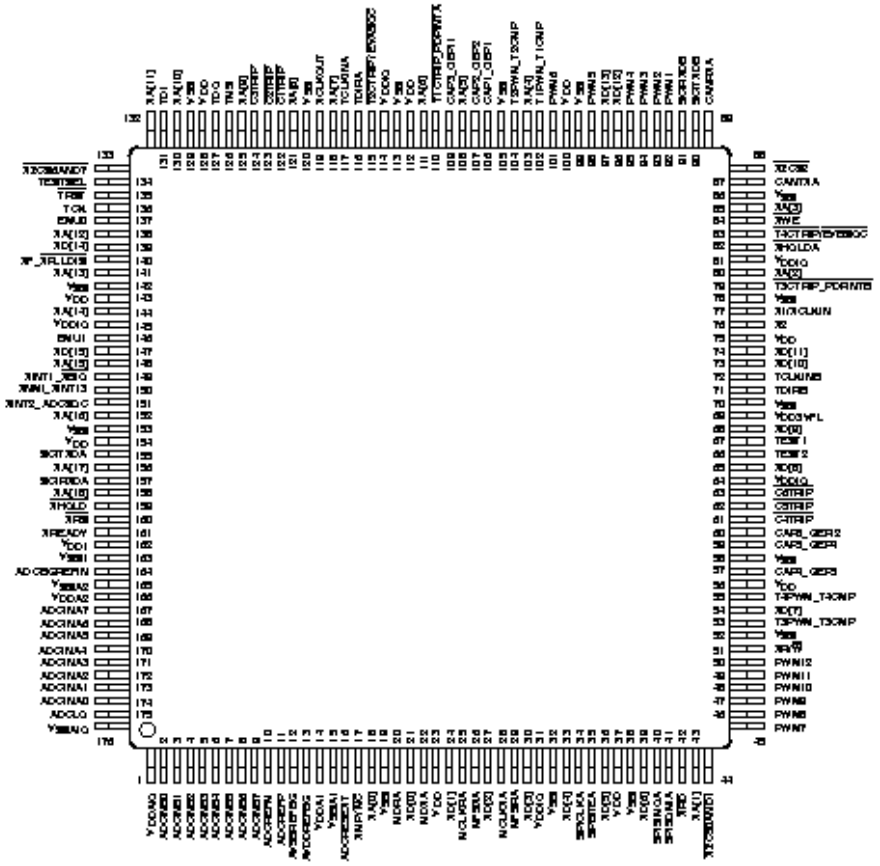


Figure 2–2. TMS320F2812 176-Pin PGF LQFP (Top View)

3 Functional Overview

ADVANCE INFORMATION

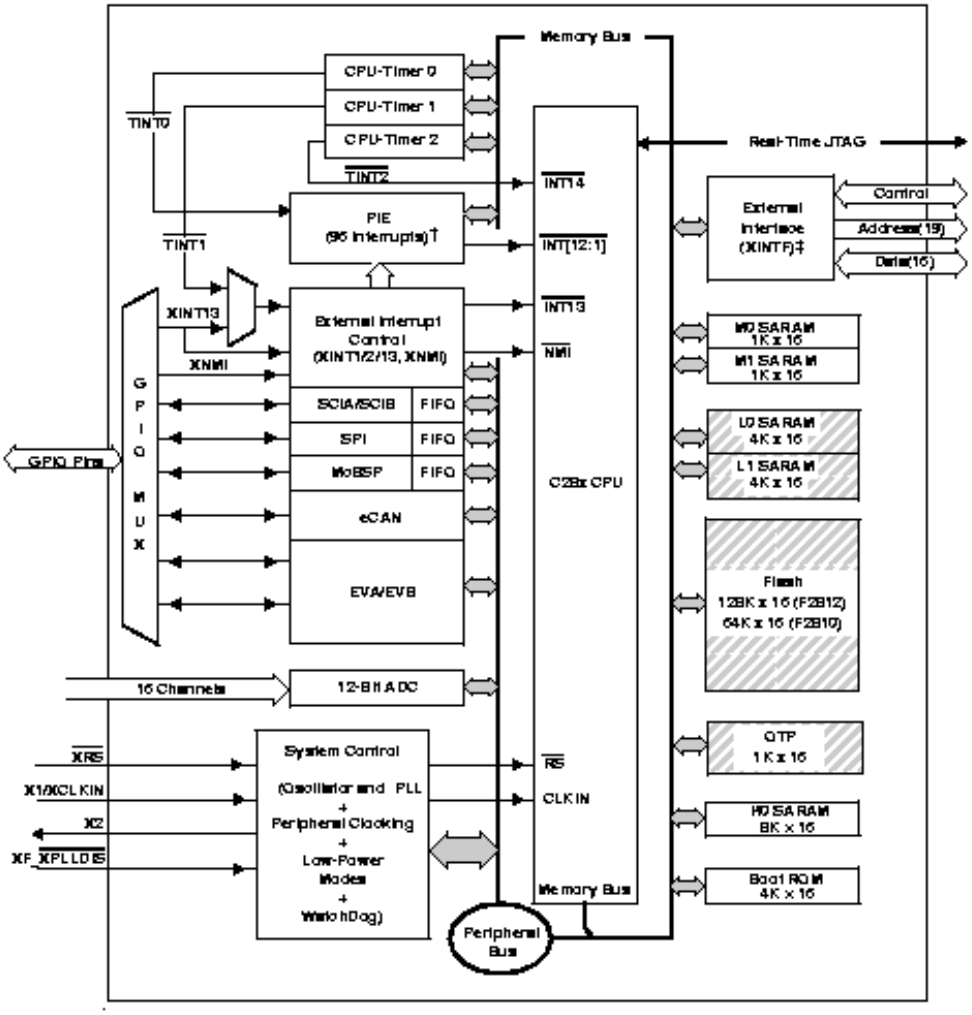


Figure 3–1. Functional Block Diagram

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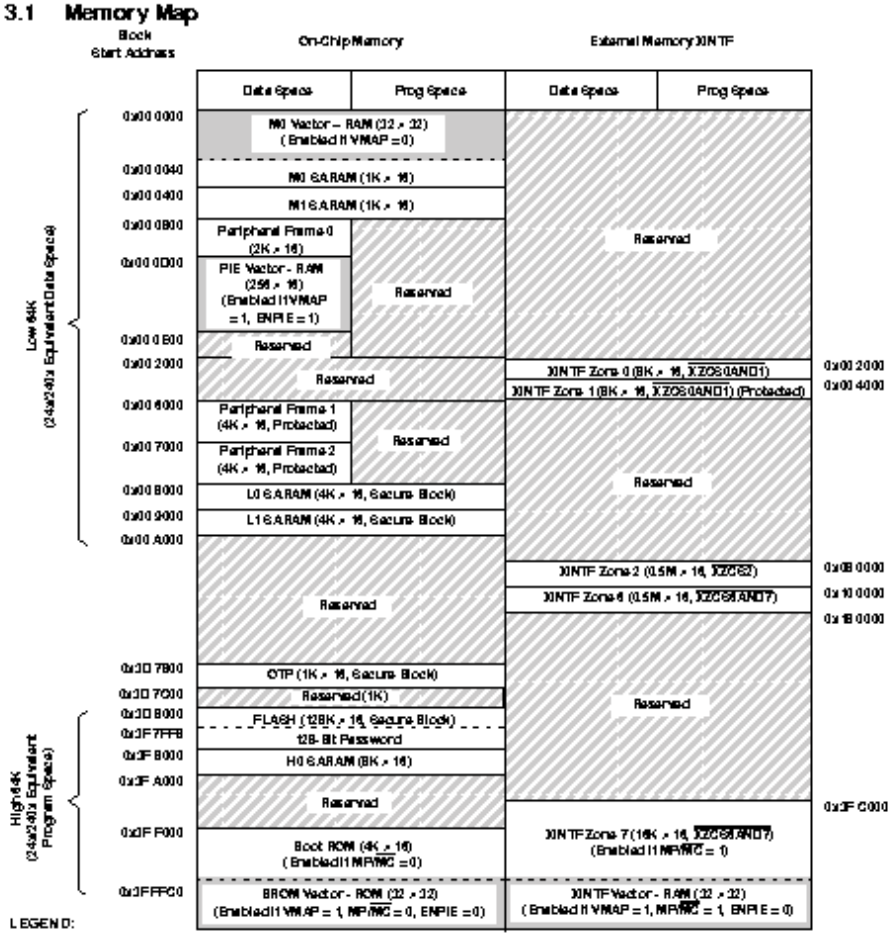
3.1 Memory Map

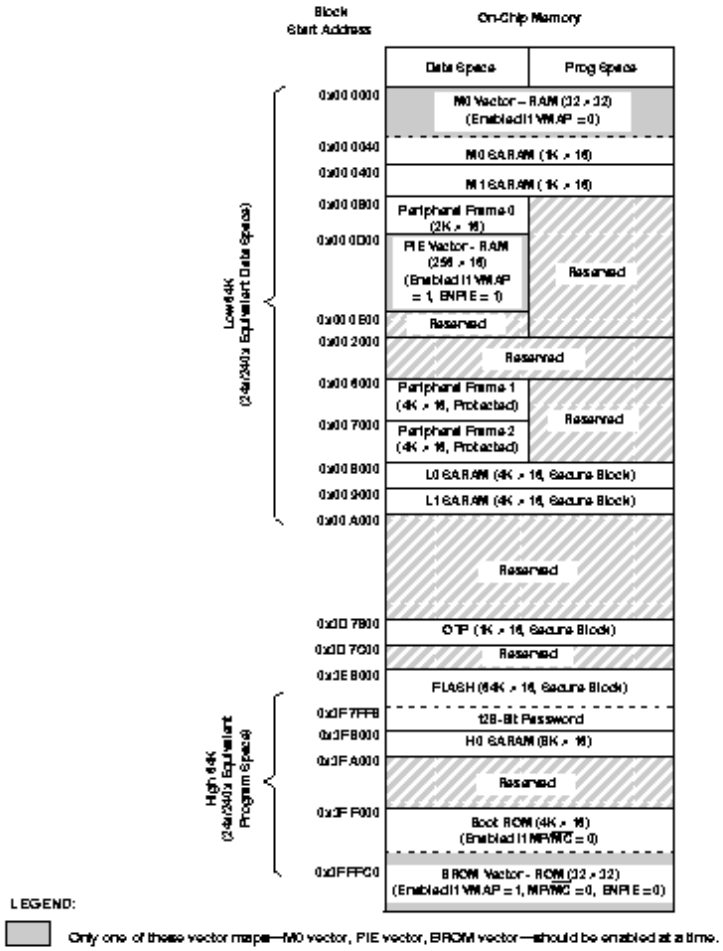


NOTES: A. Memory blocks are not to scale.
B. Reserved locations are reserved for future expansion. Application should not access these areas.
C. Boot ROM and Zone 7 memory maps are active either in on-chip or XINTF zone depending on MP/$\overline{MC}$, not in both.
D. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.
E. "Protected" means the order of Write followed by Read operations is preserved rather than the pipeline order.
F. Certain memory ranges are EALLOW protected for spurious writes after configuration.
G. Zones 0 and 1 and Zones 6 and 7 share the same chip select; hence, these memory blocks have mirrored locations.

Figure 3–2. F2812 Memory Map

ADVANCE INFORMATION

ADVANCE INFORMATION



NOTES: A. Memory blocks are not to scale.
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C. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.
D. "Protected" means the order of Write followed by Read operations is preserved rather than the pipeline order.
E. Certain memory ranges are EALLOW protected for spurious writes after configuration.

Figure 3–3. F2810 Memory Map

CURRICULUM VITAE

PERSONAL INFORMATION

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Date and Place of Birth: 12 April 1973 , Mersin
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EDUCATION

Degree	Institution	Year of Graduation
MS	METU Electrical-Electronic Engineering	1999
BS	METU Electrical-Electronic Engineering	1995
High School	Içel Anadolu High School, Mersin	1991

WORK EXPERIENCE

Year	Place	Enrollment
2002- Present	SISTAS A.S.	R&D Engineer
1995-2002	TUBITAK-BILTEN Power Electronics Gr.	R&D Engineer

FOREIGN LANGUAGES

Advanced English.

PUBLICATIONS

1. K. Kutluay, I. Çadırcı, A. Yafavi, and Y. Çadırcı, “Digital Control of Universal Telecommunication Power Supplies Using Dual 8-Bit Microcontrollers”, IEEE Industry Applications Magazine, Jan/Feb 2006.

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