DESIGN AND IMPLEMENTATION OF MICROWAVE LUMPED COMPONENTS AND SYSTEM INTEGRATION USING MEMS TECHNOLOGY

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I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

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This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

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ABSTRACT

DESIGN AND IMPLEMENTATION OF MICROWAVE LUMPED COMPONENTS AND SYSTEM INTEGRATION USING MEMS TECHNOLOGY

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This thesis presents the design and fabrication of coplanar waveguide to microstrip transitions and planar spiral inductors, and the design of metal-insulator-metal capacitors, a planar band-pass, and a low-pass filter structures as an application for the inductors and capacitors using the RF MEMS technology. This thesis also includes a packaging method for RF MEMS devices with the use of "benzocyclobutene" as bonding material.

The transition structures are formed by four different methods between coplanar waveguide end and microstrip end, and they are analyzed in 1-20 GHz. Very low loss transitions are obtained by maintaining constant characteristic impedance which is the same as the port impedance through the transition structures.

The planar inductors are formed by square microstrip spirals on a glass substrate. Using the self-inductance propery of a conductive strip and the mutual inductance between two conductor strips in a proper arrangement, the inductance value of each structure is defined. Inductors from 0.7 nH up to 20 nH have been designed and fabricated.

The metal-insulator-metal capacitors are formed by two coplanar waveguide structures. In the intersection, one end of a coplanar waveguide is placed on top of the end of the other coplanar waveguide with a dielectric layer in between. Using the theory of parallel plate capacitors, the capacitance of each structure is adjusted by the dimensions of the coplanar waveguides, which obviously adjust the area of intersection. Capacitors from 0.3 pF up to 9.8 pF have been designed.

A low-pass filter and a band-pass filter are designed using the capacitors and inductors developed in this thesis. In addition to lumped elements, the interconnecting transmission lines, junctions and input-output lines are added to filter topologies.

The RF MEMS packaging is realized on a coplanar waveguide structure which stands on a silicon wafer and encapsulated by a silicon wafer. The capping chip stands on the BCB outer ring which promotes adhesion and provides semi hermeticity.

Keywords: Transition between transmission lines, planar spiral inductor, metal-insulator-metal capacitor, RF MEMS packaging, surface micromachining.

ÖZ

MİKRODALGA TOPLU DEVRE ELEMANLARININ VE SİSTEM ENTEGRASYONUNUN MEMS TEKNOLOJİSİ İLE TASARIMI VE YAPIMI

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Eylül 2006, 154 sayfa

Bu tezde eşdüzlemsel dalga kılavuzundan mikroşeride geçişlerin, düzlemsel spiral indüktörlerin tasarımları ve üretimleri, metal-yalıtkan-metal kapasitörlerin, alçak geçiren ve bant geçiren filtrelerin tasarımları sunulmaktadır. Bunların yanı sıra, tezde, "benzocyclebutene" ile gerçekleştirilen RF MEMS paketleme çalışmaları da yer almaktadır.

Geçiş yapıları, mikroşerit hattın ucu ile eşdüzlemsel dalga kılavuzu ucu arasında olacak şekilde dört farklı tipte oluşturulmakta, 1-20 GHz frekans bant aralığında analiz edilmektedir. Geçiş yapılarının içindeki karakteristik empedans, giriş-çıkış empedansına eşit tutulmakta, ve bu yolla çok az kayıplı geçişler elde edilmektedir.

Düzlemsel indüktörler, kare şeklindeki mikroşerit spirallerin cam taban üzerine yerleştirilmesiyle oluşturulmaktadır. İletken şeridin sahip olduğu öz-indüktans özelliği ve uygun konumlandırma ile sağlanan iki iletken arasında meydala gelen eş-indüktans ile her bir indüktör istenilen indüktansa sahip olacak şekilde tasarlanmıştır. 0.7 nH ile 20 nH arasında indüktanslara sahip indüktörler tasarlanmış ve üretilmiştir.

Metal-yalıtkan-metal kapasitörler iki eşdüzlemsel dalga kılavuzu ile oluşturulmaktadır. İki hattın kesişim noktasında, iki hattın uç bölgeleri üst üste olacak şekilde konumlandırılmakta ve araya iletken tabaka yerleştirilmektedir. Paralel plaka kapisitör teorisi kullanılarak, toplam kapasitans hatların boyutları ile, diğer bir deyişle kesişim noktasındaki plaka alanı ile ayarlanmaktadır. 0.3 pF ile 9.8 pF arası kapasitanslara sahip kapasitörler tasarlanmıştır.

Tez kapsamında tasarlanan indüktör ve kapasitörler ile alçak geçiren ve bant geçiren filtre yapıları tasarlanmıştır. Ayrıca filtre yapısı içindeki her devre elemanı arasındaki iletim hatların, birleşim noktaları ve giriş-çıkış hatları filtre yapısına eklenmiştir.

RF MEMS paketleme, silikon taban üzerine üretilen eşdüzlemsel dalga kılavuzunun silikon kapak ile kapatılmasıyla gerçekleştirilmektedir. Silikon kapak, eşdüzlemsel dalga kılavuzunu içine alan yapışkan bir BCB çemberi üzerine yerleştirilmektedir.

Anahtar kelimeler: İletim hatları arasındaki geçiş, düzlemsel spiral indüktör, metal-yalıtkan-metal kapasitör, RF MEMS paketleme, yüzey mikroişleme.

To My Family

and

Friends

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CHAPTER I

INTRODUCTION

In modern communication world, the need for high power transmission arouses the need for higher frequency of operation. In order to operate single devices or systems at considerably high frequencies, the dimensions must be shrinked to a certain limit where the wavelength of the operation is comparable with the device dimensions. As the millimeter-wave technology has advanced tremendously in the last few decades, the size of the devices operating at these frequencies tends to be in the order of micrometers. The size is not the only property that matters when it comes to realization of the required microwave components, as equally important other parameters are low cost, high performance, compatibility with common production techniques, low loss, and wide band of operation.

The fabrication of extremely small size devices can be done with micromachining technology in terms of thin layer metallization or dielectric deposition. Using this technology, single or multi layered structures can be constructed and suspended bridge-type elements can be formed.

This thesis proposes three different topics which includes the design and fabrication of planar microwave structures using radio frequency micro-electo-mechanical systems (RF MEMS) technology. The first topic included in the thesis is coplanar waveguide (CPW) to microstrip transitions, where low loss and wide band transition of these two different kinds of transmission lines is achieved. The idea in transition rises from the impedance matching theory. The reflections in the transition section are minimized in order to obtain the transition with minimum loss. Four types of

transition structures, i.e., direct type, linear type, staircase type, polynomial type, are analyzed with various parameter changes. In the direct and linear type transitions, effects of multiple reflections in the unmatched sections are observed. With staircase and polynomial type transition very succesfull transitions are observed using the characteristic impedance matching idea. The structures are fabricated monolithically using the MEMS technology. The relation to transition structures with RF MEMS can be noticed in many aspects. The first application is appearent when RF MEMS devices are measured on wafer with the probe station. The probes are CPW ended and in order to measure a microstrip end RF MEMS structure, the microstrip ends must transformed to CPW ends with the use of transition structures. Another application is using the transition within a RF structure which has both CPW and microstrip sections. The transition structure smoothly transfers the wave from one mode to another with minimum loss.

The second topic included in the thesis includes the design, fabrication and measurement of lumped inductors and capacitors fabricated with MEMS technology. As an application to the lumped elements, a low-pass filter and a band-pass filter are designed. A library of square planar spiral inductors and a library of metal-inductor-metal (MIM) capacitors are created. The aim of creating these libraries is to supply on chip circuit components in system-size applications. Also the filter structures built by these components are subject to be modified and made tunable using RF MEMS technology. It is easier to modify filter structures built with lumped components to be tunable rather than coupled filter structures, one of which is explained in the previous studies section of filter structures.

The third topic of the thesis is about packaging of RF MEMS devices with wafer-to-wafer bonding with Benzocyclobutene (BCB) as sealing and bonding material. A fabrication experiment on the adhesion quality and bonding parameters are performed. From the simulations it is observed that for cap cavities more than 50 μm, the RF performance of a CPW structure is not affected.

This chapter briefly summarizes the work of this thesis. The previous works and more detailed explanation of developed structures on each topic are included in the introduction sections of the related chapters. Section 1.1 gives a genereal view on the RF MEMS technology, and Section 1.2 gives the research objectives and organization of the thesis.

1.1. General View on RF MEMS

During the research of microelectromechanical systems, the application of the RF branch is diversed into many sub-branches. The technology enables the production of single ciruit elements like switches with different topologies and actuation methods [1]-[3], inductors [4]-[5], tunable capacitors and varactors [6]-[7], transmission lines [8]-[9], high quality mechanical filters [10]-[11], and thin film bulk acoustic resonators [12]. Besides, integration of these circuit elements makes it possible to design adjustable system-level devices with higher complexity. MEMS phase shifter [13]-[14], is a capacitively loaded transmission line where a change in the loading capacitance changes the phase velocity of the traveling wave in the structure. Tunable antennas [15]-[16], tunable filters [17]-[18], tunable resonators [19], and tunable frequency selective surfaces [19], are all examples of complex structures with intergrated MEMS elements.

There are several advantages of MEMS technology that can be summarized as follows:

- *Near zero power consumption*: Since most MEMS devices need electromechanical actuation, there consume power only in the switching period and the power dissipation is less than 0.1 mW [19].
- *Adjustablity:* The mechanical propery of the MEMS devices allows adjustable characteristics with movable structural parts such as filters, matching network and capacitively loaded any other RF structures.

- *High Linearity:* Since no semiconductors or other nonlinear components are used in RF MEMS devices, a very high linearity and very low intermodulation is observed.
- *Low loss:* RF devices with very low loss can be realized with MEMS technology. In 1-100 GHz band, MEMS switches have loss less than 0.2 dB [19].
- *Very High Isolation for MEMS switches:* MEMS switches provide very high isolation up to 100 GHz. It is reported that it is possible to design switch structures at Ka, V and W bands with isolation better than -20 dB [19].

However MEMS technologhy has few drawbacks that can be summarized as follows:

- *Low Speed:* The switching time of MEMS switches is reported as 1-300μs [19]. The low resonant frequencies of the mechanical structure of the RF MEMS structure are the limiting factor on switching time.
- *High actuation voltage:* The MEMS switches require actuation voltages up to 90V [19]. In order to supply voltages of this level, a seperate power regulator circuit may be required.
- *Power handling:* It is reported that MEMS switches can handle only moderate power levels up to 300mW [19].
- *Reliability:* There are switch structures with switching cycles more than 60 billion available in the literature [19]. However a switching time is heavily dependent on the duty cycle of operation where the down state period determines the quality of the switching cycle and device rhobustness. Unfortunatly today's wireless communication systems requires switching cycles in the order of hundred billion cycles.
- *Packaging:* The environmental conditions critically determine the life time and performance of RF MEMS devices. A good packaging is necessary to isolate the movable sections of the device from the outside environment. However packaging increases the device cost, complicates the fabrication process and negates the device performance.

Considering the wide range of applications, device performances and a huge variation of devices, the RF MEMS technology is declared to play a major role in future's communication systems.

1.2. Research Objectives and Organization of the Thesis

The main goal of this thesis is to design and fabricate low loss CPW-microstrip transitions, planar spiral inductors, MIM capacitors, a low-pass filter, a band-pass filter and to experiment on RF MEMS packaging with BCB. The specific objectives can be summarized as follows:

- Design and fabrication of various transition structures between coplanar waveguides and microstrip lines. The transitions shall be designed to have a very low insertion loss and high isolation to achieve successful characteristics within a small physical length.
- Design and fabrication of a planar spiral inductor library with MEMS technology. The inductor structures shall have compact size where maximum outside diameter is at most 500µm. A various inductor values must be covered in the library from sub nH to more than 10 nH.
- Design and fabrication of a MIM capacitor library with MEMS technology. The structures must be realized with available MEMS technology in METUMET. The devices shall have capacitance from sub pF to 10 pF.
- Design and fabrication of a low-pass and a band-pass filter shall as applications to integration of spiral inductors and MIM capacitors. The low-pass filter shall have a critical frequency of 2 GHz where the band-pass filter shall have criticial frequencies of 2 and 4.6 GHz respectively. The pass band of the filter is limited by the SRF of spiral inductors.
- Initialization and optimization of RF MEMS packaging using BCB as adhesive and seal layer at microelectronics facilities of METU.

The thesis is composed of five chapters. After this introduction chapter, Chapter 2 explains the coplanar waveguide to microstrip line transition theory and proposed transition structures with design and fabrication results including the process steps.

Chapter 3 explains the design, measurements and detailed fabrication steps of inductor and capacitor structures together with their filter applications. The comparison of circuit model of capacitors and inductors with the EM simulations is done.

Chapter 4 presents the studies on RF MEMS packaging with adhesive BCB layer. A parametric analysis on capping chip design is explained. In addition to some proposed process steps explained in the chapter, an experimental wafer bonding is performed in METUMET and the quality of the bonding is observed.

Chapter 5 summarizes the results of this study and suggests the areas for future research.

CHAPTER II

COPLANAR WAVEGUIDE TO MICROSTRIP TRANSITIONS

In this chapter studies on coplanar waveguide to mictostrip transitions are explained. Section 2.1 gives an introduction about the topic and Section 2.2 gives the previous research of the transition structures. Section 2.3 and 2.4 give useful information on microstrip and coplanar structures respectively. Section 2.5 explains the reflection in a transmission line, and Section 2.6 explains the effects of a step discontinuity. Section 2.7 gives the basic idea of transition, and Sections 2.8-2.11 explains the proposed transition models. Section 2.12 and 2.13 give the fabrication steps and measurements respectively. Finally, an insightful discussion is presented in Section 2.14.

2.1. Introduction

Since the demand for high density and high performance microwave and millimeter wave circuits is continually increasing, an utter need for smaller and more highly integrated RF devices is growing. These compact devices are mostly fabricated with different types of components which require different types of transmission lines. Microstrip line is one of the most commonly used transmission lines in RF circuit designs due to its relatively compact size, uncomplicated structure thus ease of fabrication and low cost. The coplanar waveguide (CPW) is another commonly used type of transmission line which has a great use especially in Radio Frequency

Micro-Electromechanical-Systems (RF MEMS) while constructing movable switch structures and variable capacitors in terms of loaded transmission lines. Particularly in RF MEMS studies, most of the integrated devices include both types of transmission lines. To achieve the highest possible integration, while maintaining each circuit's effective performance, transitions are needed to reduce the mismatch and coupling between different circuit elements. Transitions have another vital role in the measurement stage of microstrip ended RF circuits. On wafer measurements of such devices require microstrip-CPW transitions in order to establish a proper connection the CPW probes of the probe stations in order to be fully analyzed with Network Stations.

This chapter presents a parametric study on various compact, wideband transitions from a CPW to a microstrip line where both transmission lines have characteristic impedances (Z_0) of 50 Ω. The transition structures are designed and fabricated on Pyrex 7740 glass substrate with a center frequency of 10 GHz. The Finite Element Method (FEM) is used to both verify the experimental results and optimize the design.

2.2. Previous Work on CPW-Microstrip Transitions

There are numerous studies on transitions between different kinds of transmission lines in the literature however not many examples on CPW-microstrip transitions are available. The first transition example is applied to a dual polarized slot-dipole antenna in [20]. The structure is reazlied as proximity coupled overlay transition between microstrip and coplanar waveguide. In this case the electromagnetic coupling occurs in the overlap region between the coplanar waveguide and microstrip.

The second example is a via-less transition structure which demonstrates a maximum insertion loss of 0.1 dB over the frequency range from 10 GHz to 40 GHz with a value of 0.4 dB at 20 GHz [21]. In the transition section, the width of the CPW signal strip is gradually increased to match the width of the microstrip. At the same time, the gap between the ground planes and signal line is widened to retain a 50 Ω characteristic impedance in order to match that of the microstrip line.

The third example [22] is the source of the staircase type transition explained in this thesis. In the HFSS simulation results, it is reported that a bandwidth of 13 GHZ with less than -25 dB return loss can be achieved. Back- to-back conductor backed CPW to microstrip transitions are fabricated on InP susbtrate and the measurements point that S_{11} is measured better than -12 dB up to 14 GHz. For Alumia substrate the S_{11} is measured as less than -15 dB up to 25 GHz.

The fourth example [23] covers different types of vertical connections between microstrip lines on parallel planes and a CPW is used as a vertical connection between the planes. A number of transitions between the horizontal and vertical parts of the connection as well as the influence of the solder are numerically investigated.

Another example is a development of a broadband via-less CPW to microstrip transition [25]. The transition uses sections of conductor backed CPW with a gradually increased slot width and a tapered bottom ground plane to provide a smooth transformation of the electromagnetic fields and impedance matching, and presents a good performance over a broad bandwidth. Also the modelling of the transitions is investigated in [24] and [26].

2.3. Microstrip Transmission Line

Microstrip transmission lines consist of a conductive strip of width "w" and thickness "t" and a wider ground plane, separated by a dielectric layer of thickness "h" as shown in Figure 2.1. This is one of the most popular microwave transmission lines, especially for microwave integrated circuits and MMICs due to its simplicity in design and fabrication.

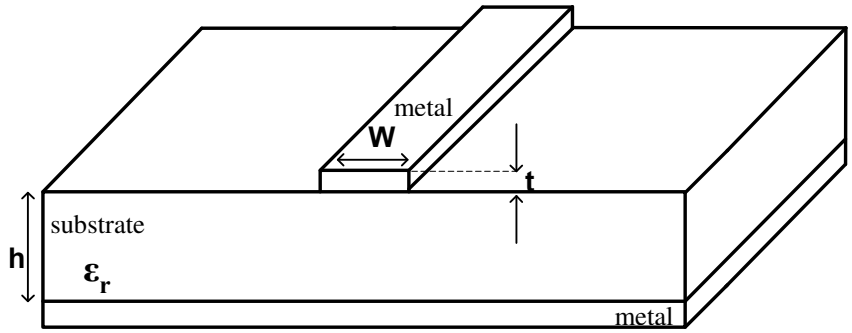


Figure 2.1: Microstrip line structure, where a metal line is placed on a glass substrate.

In a microstrip transmission line the dielectric does not enclose the signal line completely which complicates the wave behaviour. Some of the field lines are in the dielectric region concentrated between the strip conductor and the ground plane, and some fraction in the air region above the substrate. Therefore the propagation is not a pure TEM since the phase velocity in air and the phase velocity in dielectric region are different.

An effective dielectric constant is taken into consideration while analyzing the wave characteristics. While calculating the characteristic port impedance of the microstrip line, the effective dielectric constant is calculated differently depending on the ratio

of width and height. For different width and height ratios, the effective permittivity and characteristic impedance are calculated as follows [27]:

For $\left(\frac{w}{h}\right) \leq 1$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + 12\left(\frac{h}{w}\right)\right)^{-1/2} + 0.04\left(1 - \left(\frac{w}{h}\right)\right)^2\right] \quad \textbf{(2.1)}$$

$$Z_0(ohms) = \frac{60}{\sqrt{\varepsilon_{eff}}} \ln\left(8\frac{h}{w} + 0.25\frac{w}{h}\right) \quad \textbf{(2.2)}$$

For $\left(\frac{w}{h}\right) \geq 1$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + 12\left(\frac{h}{w}\right)\right)^{-1/2}\right] \quad \textbf{(2.3)}$$

$$Z_0(ohms) = \frac{120\pi}{\sqrt{\varepsilon_{eff} \times \left[\frac{w}{h} + 1.393 + \frac{2}{3}\ln\left(\frac{w}{h} + 1.444\right)\right]}} \quad \textbf{(2.4)}$$

2.4. Coplanar Waveguides

A coplanar waveguide (CPW) consists of a conductor that is separated from a pair of ground planes which are on the same plane. The structure stands on a dielectric medium, which is thick enough so that EM fields die out before they get out of the substrate.

The major advantage of a coplanar waveguide is the ability to connect active and passive circuit components in shunt from the center conductor to the ground plane on the same side of the substrate. Since both grounds are located coplanar with the signal line, the need for vias in the substrate is avoided which is a troublesome issue especially with glass type of substrates.

The characteristic impedance of the CPW is determined only by the dimension ratios, meaning that the structure dimensions can be minimized until a practical limit, where the losses become effective due to the shrinked area of the fields, is reached.

2.4.1. Conductor Backed Coplanar Waveguides

Conductor backed coplanar waveguide (CBCPW), shown in Figure 2.2, is a variant of the standard CPW. The difference is the metal layer on the backside of the substrate. With this addition to conventional CPW, the rigidity and power carrying capability of the waveguide are improved. In order to satisfy a successful CPW – microstrip transition, it is crucial that a common ground is present in the system. When constructing a transition, using CBCPW enables us to join the backside metallizations of both transmission line types and nullifies the effect of floating grounds.

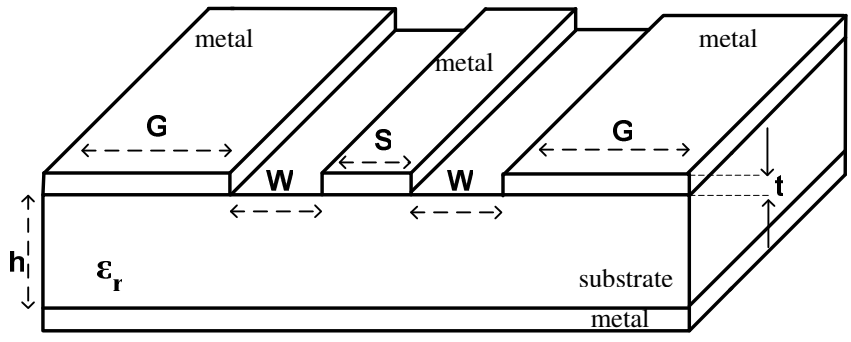


Figure 2.2: Conductor backed coplanar waveguide structure.

The analysis of the CPW is performed using the quasi-static approach using mapping techniques [28]-[30] which gives the analytical expressions for a fast and precise design. Since the dielectric does not enclose the signal line completely the effective dielectric constant for CPW is composed of free space and substrate components. As "G" goes to infinity, the effective permittivity and characteristic impedances are calculated as follows:

$$\varepsilon_{eff} = 1 + q(\varepsilon_r - 1) \tag{2.5}$$

$$Z_0 = \frac{60\pi}{\sqrt{\varepsilon_{eff}}} \frac{1}{K(k_1)/K'(k_1) + K(k_2)/K'(k_2)} \tag{2.6}$$

$K(k)/K'(k)$ is the ratio of the elliptic integrals of first kind given in [REF] as:

For $0 \le k \le 0.707$

$$\frac{K(k)}{K'(k)} = \frac{\pi}{\ln\left[2(1+\sqrt{k'})/(1-\sqrt{k'})\right]} \tag{2.7}$$

For $0.707 \le k \le 1$

$$\frac{K(k)}{K'(k)} = \frac{1}{\pi}\ln\left[2(1+\sqrt{k})/(1-\sqrt{k})\right] \tag{2.8}$$

$$k' = \sqrt{1-k^2} \tag{2.9}$$

The explicit k parameters in the expressions are:

$$k_1 = \frac{S}{S+W} \tag{2.10}$$

$$k_2 = \frac{\tanh(\pi S / h)}{\tanh(\pi(S + 2W) / h)} \tag{2.11}$$

$$q = \frac{K(k_2) / K'(k_2)}{K(k_1) / K'(k_1) + K(k_2) / K'(k_2)} \tag{2.12}$$

2.5. Reflection Coefficient Calculation

Figure 2.3 shows a lossless transmission line model [31] which is terminated by a load impedance Z_L.

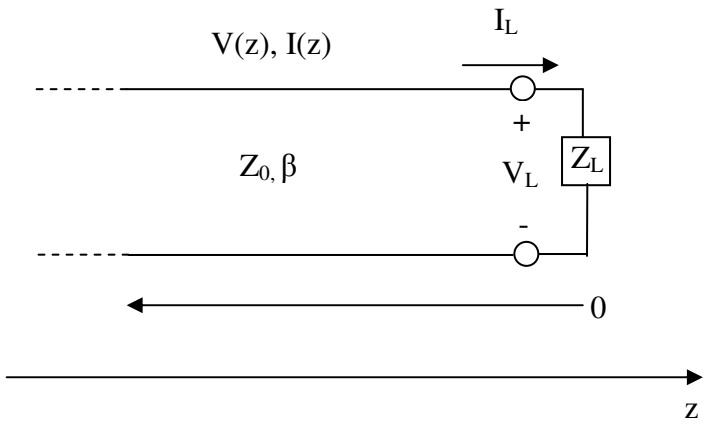


Figure 2.3: Lossless transmission line terminated by Z_L.

The total voltage anywhere on the line can be written as the summation of the incident wave and the reflected wave as following:

$$V(z) = V_0^{+} e^{-j\beta z} + V_0^{-} e^{+j\beta z} \tag{2.13}$$

The total current on the line is derived as:

$$I(z) = \frac{V_0^+}{Z_0} e^{-j\beta z} - \frac{V_0^-}{Z_0} e^{+j\beta z} \tag{2.14}$$

At the load end, i.e z = 0, the characteristic impedance is equal to the load impedance as:

$$Z_L = \frac{V(0)}{Z(0)} = \frac{V_0^+ + V_0^-}{V_0^+ - V_0^-} Z_0 \tag{2.15}$$

Solving for V_0^- yields:

$$V_0^- = \frac{Z_L - Z_0}{Z_L + Z_0} V_0^+ \tag{2.16}$$

The ratio of reflected voltage to incident voltage gives the reflection coefficient as:

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.17}$$

When the load is not matched, i.e $Z_L \neq Z_0$, the available power from the generator is not delivered to the load completely and this causes a loss in the system, defined as the return loss.

$$RL(dB) = -20\log|\Gamma| \tag{2.18}$$

From the equation (2.17), reflection is zero when "$Z_L = Z_0$". In a conventional uniform CPW or microstrip line, the port impedances are equal to characteristic impedances. If we assume to have ideal lossless transmission lines on the both ends

of the transition section, the only loss parameters are stemming from the transition geometry due to impedance mismatch, i.e. return loss and other parasitics.

2.6. Effects of a Step Discontinuity

A step change in width of the center strip conductor of a CPW is shown in Figure 2.4 [32]. The step discontinuity perturbs the normal CPW electric and magnetic fields and gives rise to additional reactances. These additional reactances are assumed to be lumped and located at the plane of the strip discontinuity. The step discontinuity is modeled as a T-network consisting of two series inductances L_{s1} and L_{s2} and a shunt capacitance C_s

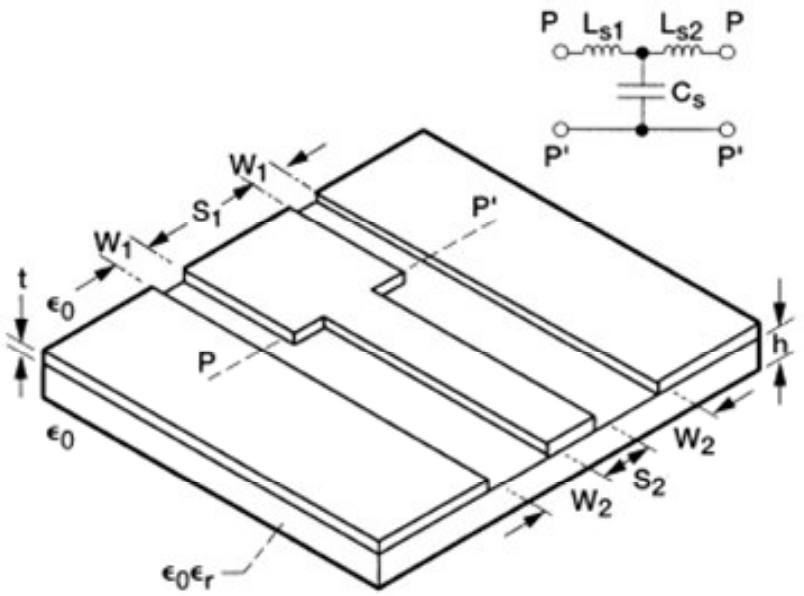


Figure 2.4: Step change in the center conductor of a CPW [32].

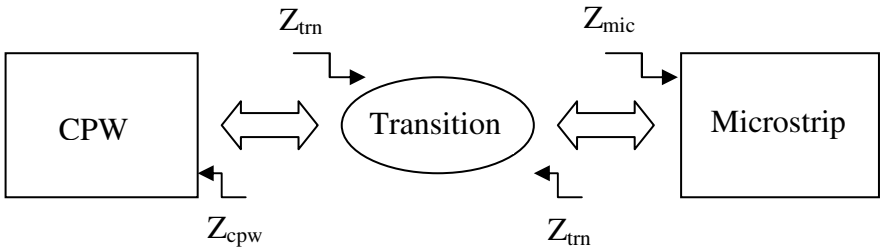
This behaviour obviously changes the characteristic impedance of tapered structures with respect to a homogenous transmission line and this effect is meant to be minimized in the transition structures explained in this chapter. In chapter III, the series inductance contribution of the discontinuity is considered before the design of the filter circuit so that the EM simulated structures meet the filter requirements.

2.7. Basic Concepts of Transition Design

The transition structure can be any planar geometry if it provides low reflection and low insertion loss. In order to satisy these needs, as explained in the previous topic, the port impedances of the transition structre shall match that of the transmission lines on both ends. Figure 2.5 shows a diagram of impedance matching idea where all impedances are set to the same impedance. The easiest way of realizing this is to have the same dimensions and geometry of the load elements on the input and output ports of the transition structure. In other words, one port of the transition shall have a microstrip end and other port shall have a coplanar end.

The port impedances of each structure are determined with port simulations. During port simulations, only the field distribution at the ports is analyzed and characteristic impedances are determined accordingly. Iterations have been made to reach the desired 50 Ω impedance.

Another issue to be considered is the reflections throughout the transition structure. At low frequencies this effect can be neglected since the guided wavelength, λ_g is large enough not to be disturbed by the discontinuity unless the discontinuous dimension is comparable with λ_g. In addition to this effect, the characteristic impedance through the transition region section shall match that of the entire system



$$Z_{cpw} = Z_{trn} = Z_{mic}$$

Figure 2.5: Diagram of a matched impedance condition.

in order to get rid of the multiple reflections from each unmatched sections. In the following designs, especially the direct and linear transition models, these parasitic effects are present but in the latter designs, methods to remove these effects are presented.

The designs are performed under the guidance of the scattering parameters (S-parameters) which give direct information on the reflected and the transmitted voltage waves at the ports. Equation (2.19) gives the generalized S-parameters which is the ratio of the incident and the reflected port voltages when the characteristic impedances are the same [31].

$$S_{ij} = \frac{V_i^- / \sqrt{Z_{0j}}}{V_j^+ / \sqrt{Z_{0i}}} \qquad \textbf{(2.19)}$$

In the design procedure, S-parameter analysis is performed between the input port of the microstrip which is set to port 1, and the output port of the CPW section which is set to port 2. Therefore S-parameter analysis of the complete structure is performed. S_{11} and S_{21} parameters of the designed structure give information on reflection and

insertion loss, respectively. The optimizations on the designs are done in order to minimize S_{11} and maximize S_{21}.

Figure 2.6 shows the cascaded CBCPW and microstrip structures, whose dimensions are chosen to give 50 Ω characteristic impedances, and the s-parameter simulation results. The simulation is done with ADS Momentum which uses the MOM analysis technique. The maximum reflection (S_{11}) is observed to be around -35 dB and the maximum insertion loss (S_{21}) is 0.3 dB in the 1 – 20 GHz frequency band. This result reflects the ideal case since the transition effects are omitted in the simulation.

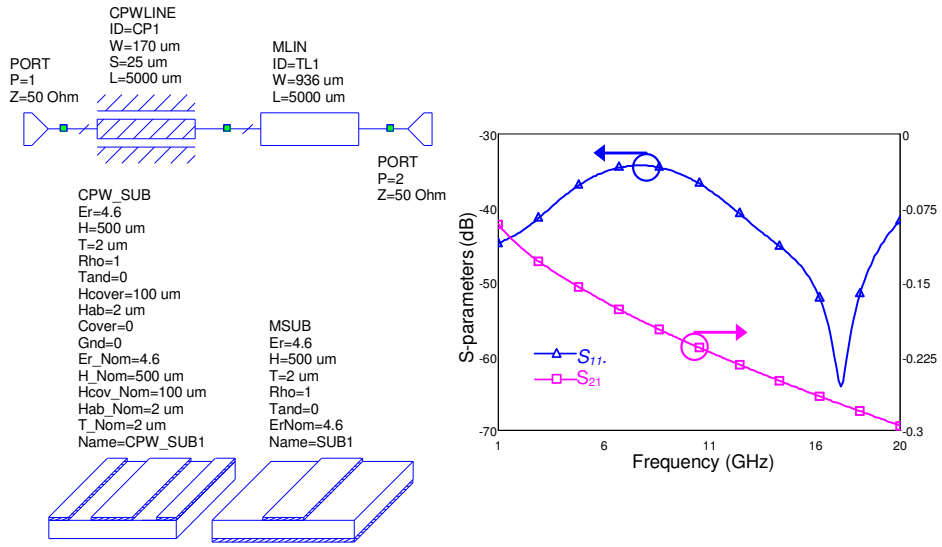


Figure 2.6: Schematics and EM simulation results of an ideal transition.

2.8. Direct Transition Model

Figure 2.7 shows the perspective view of a direct transition model. In this type of transition, a short section of a narrow microstrip between CPW and MS is employed

for direct connection. The main idea in using this transition geometry is to accomplish the transition in shortest distance where minimum area design is desired. Also this acts as a base for the rest of the superior transition geometries which are compared to this approach.

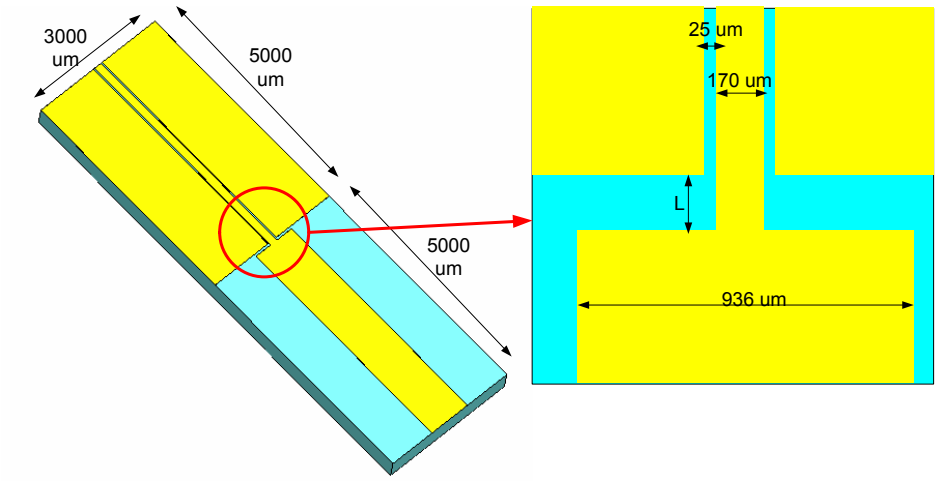
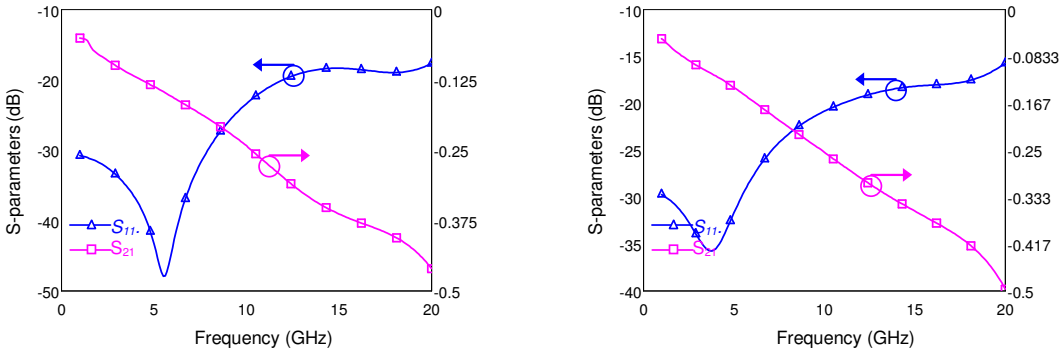


Figure 2.7: General view of a direct transition model with dimensions.

The structure consists of a CBCPW with 170-25 µm signal gap dimensions and a microstrip line whose width is 936 µm. Both of the transmission lines have lengths of 5 mm and are placed on 500 µm Pyrex 7740 glass substrate ($\varepsilon_r = 4.6$, $\tan\delta$ = 0.005) with a metallization thickness of 1.5 µm. The characteristic impedances of both lines are set to 50 Ω using EM port simulation techniques in order to achieve minimum reflection with the given specifications. The varying parameter is the center signal line length, L, of the CBCPW section which extends from 25 µm to 500 µm in the designed structures. The center signal line is directly connected to the microstrip end in the transition region.

2.8.1. Simulation Results

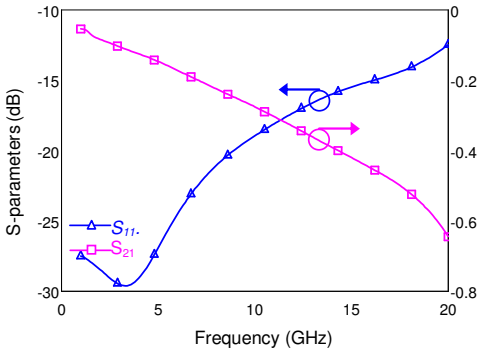
The EM simulations are performed using ANSOFT HFSS v9.2™ in the 1-20 GHz frequency band. S-parameter analysis clearly points that at frequencies lower than 10 GHz, the reflection (S_{11}) is less than -20 dB in all structures. The transition region distances are taken as L = 25, 50, 100, 200, 300, 400, 500 µm. Figure 2.8 and Figure 2.9 show the magnitudes of simulated S-parameters. As the wavelength of the traveling wave decreases with increasing frequency, the transition region where the characteristic impedance is not 50 Ω, causes reflections in the wave, thus the matching becomes distorted. This effect is also obvious in longer transition regions at low frequencies, where S_{11} values are poor at both low and high frequencies.



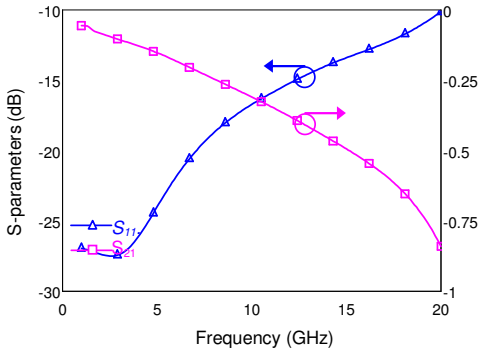
(a) 25 µm direct transition

(b) 50 µm direct transition

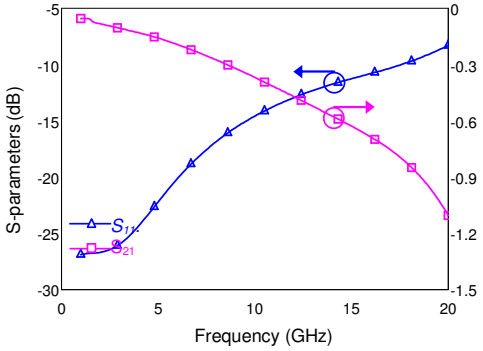
Figure 2.8 (a) – (b): Simulated S-parameter magnitudes of 25 µm and 50 µm direct transition structures.



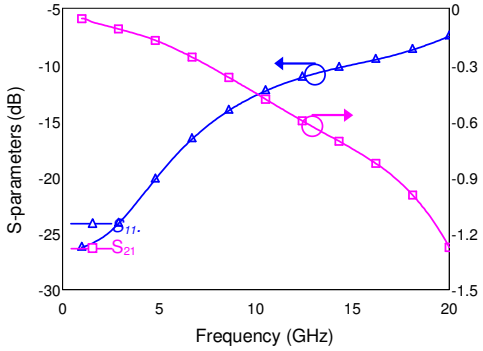
(a) 100 µm direct transition



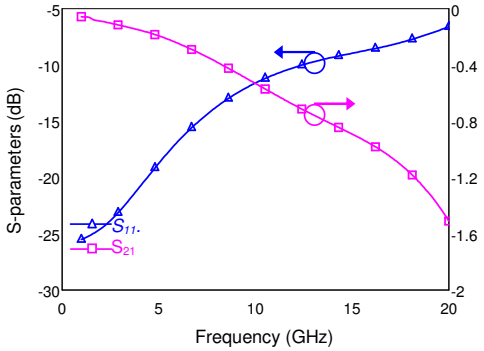
(b) 200 µm direct transition



(c) 300 µm direct transition



(d) 400 µm direct transition



(e) 500 µm direct transition

Figure 2.9 (a) – (e): Simulated S-parameter magnitudes of 100 µm to 500 µm direct transition structures.

The simulation results show that for frequencies less than 10 GHz, direct type transitions are very efficient in terms of reflection and occupied area. The transition provides the lowest reflection, below -20 dB up to 10 GHz and below -18 dB in the rest of the band when the strip length is selected to be 25 µm. The worst case is the 500 µm long design where the reflection is below -20 dB only for frequencies up to 5 GHz and goes up to -7 dB at 20 GHz. The S_{21} plots are in agreement with the reflection coefficients. For 25 µm transition, insertion loss is less than 0.45 dB in the entire frequency band and it is less than 1.5 dB for the 500 µm case.

2.9. Linear Transition Model

Figure 2.10 shows the general view of the linear type transition model. The transition is realized between the center conductor of CBCPW section and microstrip line where the center conductor end joins to microstrip end with a linear extension and the ground planes of the CPW is terminated, again linearly, at the structure edges. The varying parameter in this geometry is again the transition length, L, which is the same for both the signal and ground parts of the CPW section

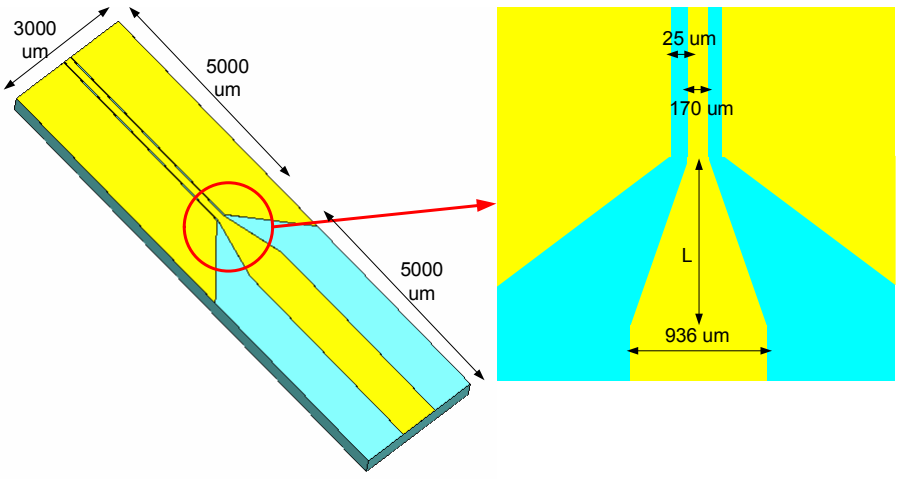
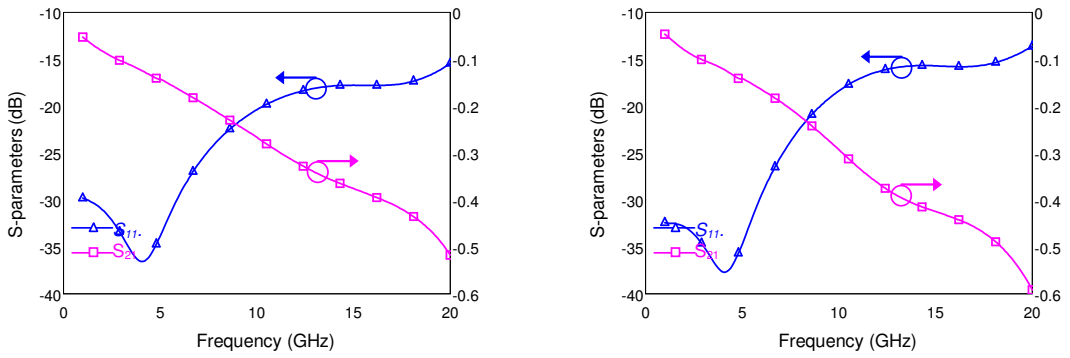


Figure 2.10: General view of a linear transition model with dimensions.

The dimension of all materials are the same as the previous model where transition lengths are taken as L = 250, 500, 750, 1000, 1250, 1500, 1750, 2000 µm. The aim of this design is to try to eliminate the effect of discontinuities of the prior design at the expense of a larger transition length.

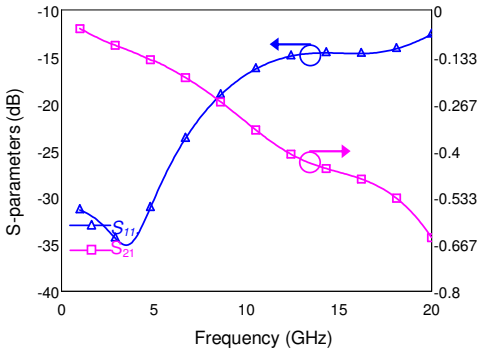
2.9.1. Simulation Results

ANSOFT HFSS v9.2^{TM} simulation results for the 1 – 20 GHz frequency band in Figure 2.11 and Figure 2.12 shows that in 1 – 10 GHz band and with respectively longer transition region lengths, similar reflection values that of the direct type transition model are obtained. Same wavelength effects are also present in this model since the transition section is not matched to 50 Ω and the length of the transition section distorts the wave at high frequencies.

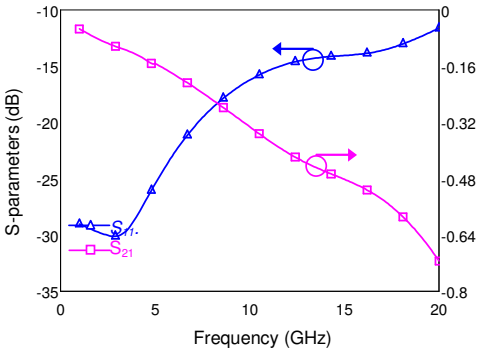


(a) 250 µm linear transition **(b)** 500 µm linear transition

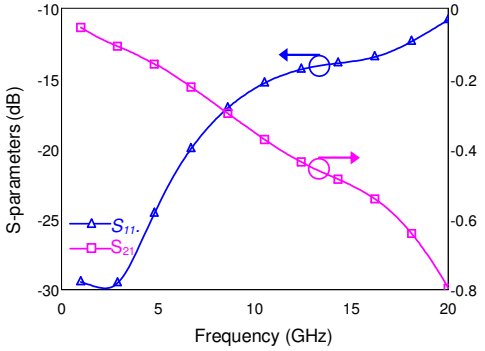
Figure 2.11 (a) – (b): Simulated S-parameter magnitudes of 250 µm and 500 µm linear transition structures.



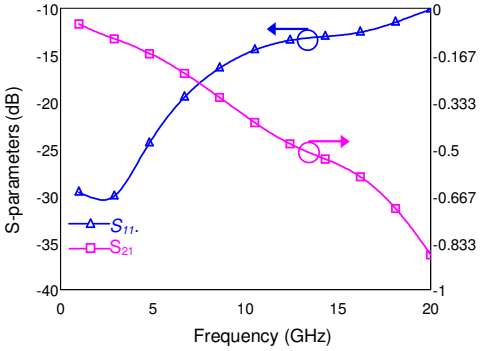
(a) 750 µm linear transition



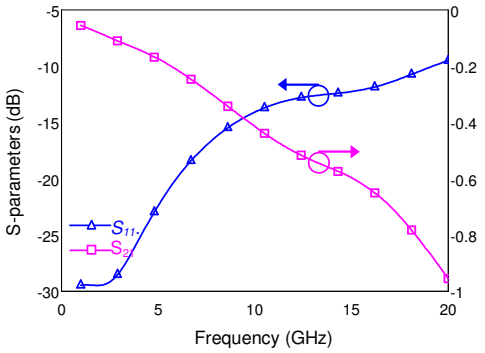
(b) 1000 µm linear transition



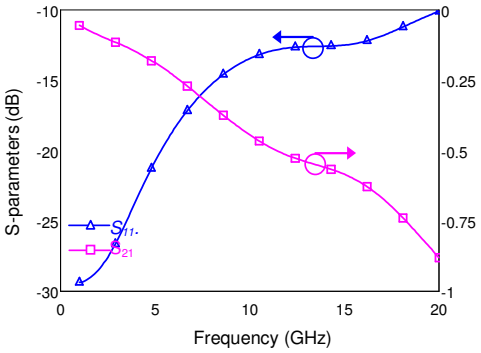
(c) 1250 µm linear transition



(d) 1500 µm linear transition



(e) 1750 µm linear transition



(f) 2000 µm linear transition

Figure 2.12 (a) – (f): Simulated S-parameter magnitudes of 750 µm to 2000 µm linear transition structures.

Best transition is observed at L=250 µm below 10 GHz where the S_{11} is less than -20 dB up to 10 GHz and less than -12 dB in the rest of the band. For L=2000 µm, reflections are kept below -20 dB up to 5 GHz and they get higher than -10 dB at 20 GHz. In the complete frequency band, the S_{21} parameters are below 0.53 dB for 250 µm and below 1 dB for 2000 µm transition lengths. This design and the previous one highlight the necessity of continuously matched transition geometries when a wideband, i.e. 1-20 GHz transitions are desired. The following two models are designed using this concept.

2.10. Staircase Transition Model

Figure 2.13 shows the general view of a staircase type transition model. The transition section of the structure has CPW subsections whose dimensions are adjusted to satisfy 50 Ω characteristic impedances individually.

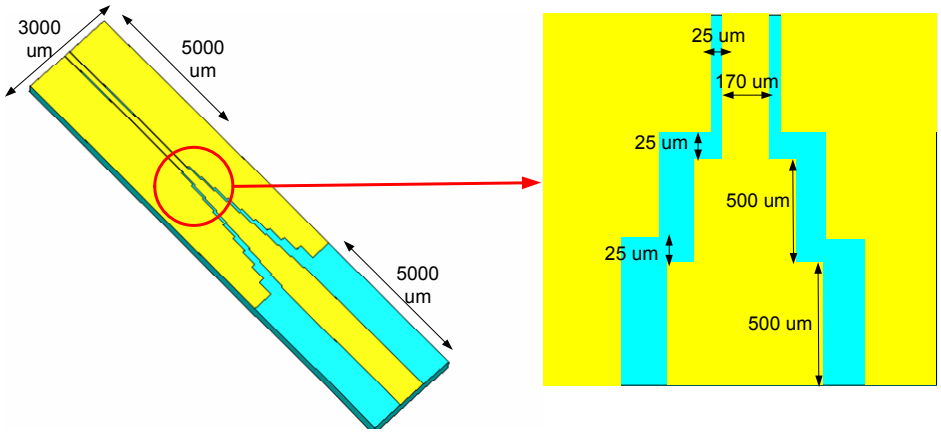


Figure 2.13: General view of a staircase transition model with dimensions.

The varying parameter is the number of CPW subsections, in other words the number of steps of the staircase, N=4, 5, 6, 7, 8, 9. Each step is 500 µm long and the

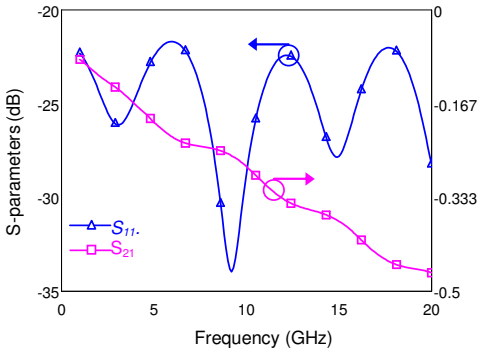
CPW and microstrip lines are 5000 µm long. In this geometry, required characteristic impedance is satisfied in the entire region at the expense of discontinuities at each step edge. Table 2.1 gives the dimensions of each CPW subsections.

Table 2.1: Signal-Gap dimensions for staircase transitions with different number of steps.

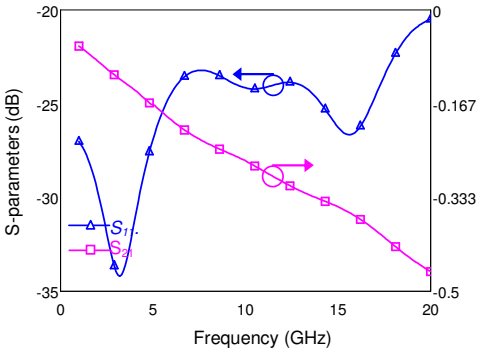
#of Steps	Signal – Gap dimensions (µm)
4	320-50, 470-85, 620-150, 770-275
5	297-45, 424-81, 551-114, 678-180, 805-330
6	279-41, 388-64, 497-94, 606-140, 715-210, 824-360
7	265-39, 360-57, 445-80, 550-114, 645-160, 740-240, 835-388
8	255-37, 340-53, 425-72, 510-98, 595-132, 680-195, 765-262, 850-430
9	245-35, 320-50, 395-65, 470-85, 545-105, 620-150, 695-200,770-275, 845-420

2.10.1. Simulation Results

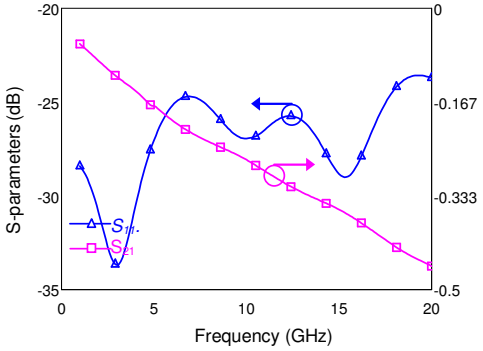
EM Simulation results in Figure 2.14 for the 1-20 GHz prove that in the entire frequency range, very low loss transitions have been observed. S_{11} parameters in all variations are less than -20 dB in the complete frequency band, and it becomes even less for higher step numbers starting from N=6, less than -25 dB. Since the characteristic impedance in the transition is maintained at 50 Ω, the transition is effectively performed even at high end of the frequency band.



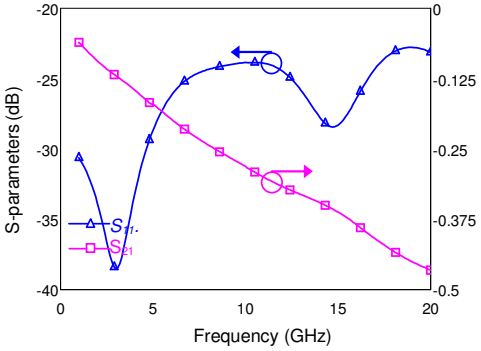
(a) 4 step transition



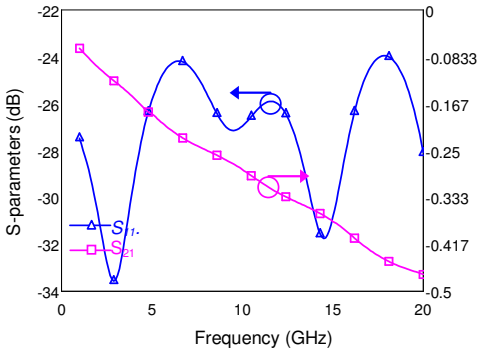
(b) 5step transition



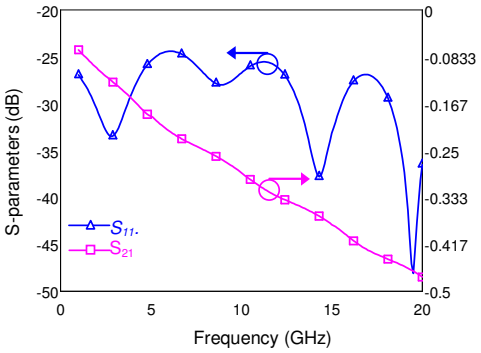
(c) 6 step transition



(d) 7 step transition



(e) 8 step transition



(f) 9 step transition

Figure 2.14 (a) – (f): Simulated S-parameter magnitudes of staircase transition structures.

As the number of steps increase, the discontinuity between each step increment becomes less. Therefore the extra inductive contribution from the edges becomes more negligible even though the number of discontinuity increases. The insertion loss is observed to be less than 0.5 dB in all structures. The next step using this concept is to eliminate the discontinuities completely by designing a transition geometry which connects the CPW and microstrip ends smoothly. The next transition model uses this approach.

2.11. Polynomial Transition Model

Figure 2.15 shows a perspective view of the CPW – microstrip transition structure. The transition section is composed of a linearly extending signal line from CPW center conductor to microstrip, and ground planes of the CPW which are terminated at the point where the transition signal line reaches to 936 μm. The ground planes are designed to obtain a characteristic impedance of 50 Ω at 30 distinct, equally spaced points through the transition section and these 30 points are attached linearly one by one, forming the optimum ground curve. Two different structures are designed with the same number of points in the transition but with different transition lengths, 1500 and 3000 μm respectively. The CPW and microstrip lines are 5000 μm each and the port dimensions are the same as previous designs.

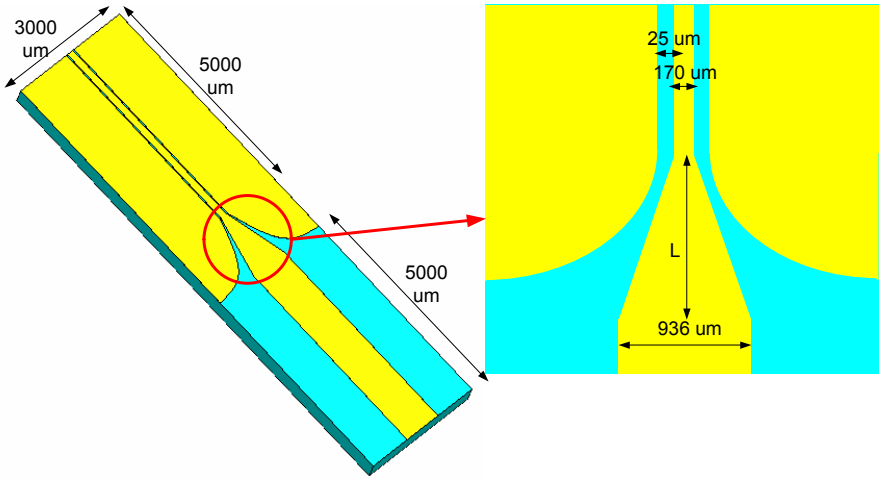
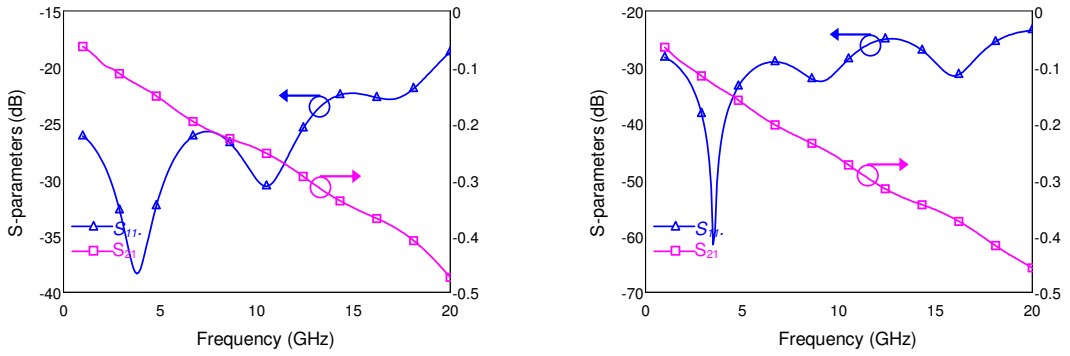


Figure 2.15: General view of a polynomial transition model with dimensions

2.11.1. Simulation Results

ANSOFT HFSS v9.2^{TM} simulation results clearly verifiy that in the complete 1-20 GHz region, S_{11} parameters of the 1500 µm long model are below -20 dB, where S_{11} parameters of the 3000 µm long model are below -25dB. The S_{21} parameters of both structures are below 0.5 dB which is pretty similar to the staircase model. Figure 2.16 shows the simulated S-parameters of the structures.



(a) 1500 µm polynomial transition **(b)** 3000 µm polynomial transition

Figure 2.16 (a) – (b): Simulated S-parameter magnitudes of polynomial transition structures.

The discontinuity effects are minimized in this geometry but the simulation results does not differ much from the staircase model. The reason for this is that the reflections converge for the structures with 50 Ω transition section where the discontinuities are getting negligible, i.e. starting from N=6 of the staircase model, including the polynomial case.

2.12. Fabrication Process

The devices are fabricated in METU-MET Cleanroom Facilities. Surface micromachining techniques were applied in terms of first metallization, lithography and backside metallization on 500 μm thick Pyrex 7740 4" glass wafer. The process steps include wafer cleaning, two sided metal sputtering, lithography and metal etching. Lithography consists of photo-resist spinning, allignment, exposure, and development stages.

2.12.1. Mask Preperation Stage

Before the fabrication process, a mask layout is prepared and sent for fabrication. The mask is necessary in the lithography stage to define the structural layers of the designed device. For multilayered MEMS processes, the required mask number is at least same as the layers in the device. So an optimization of the number of masks to be used in a device is necessary in terms of cost efficiency. In this transition study only a single mask is adequate since there is only one layer which is gold. Since the backside is completely gold without any patterns, no extra mask is necessary for backside processing.

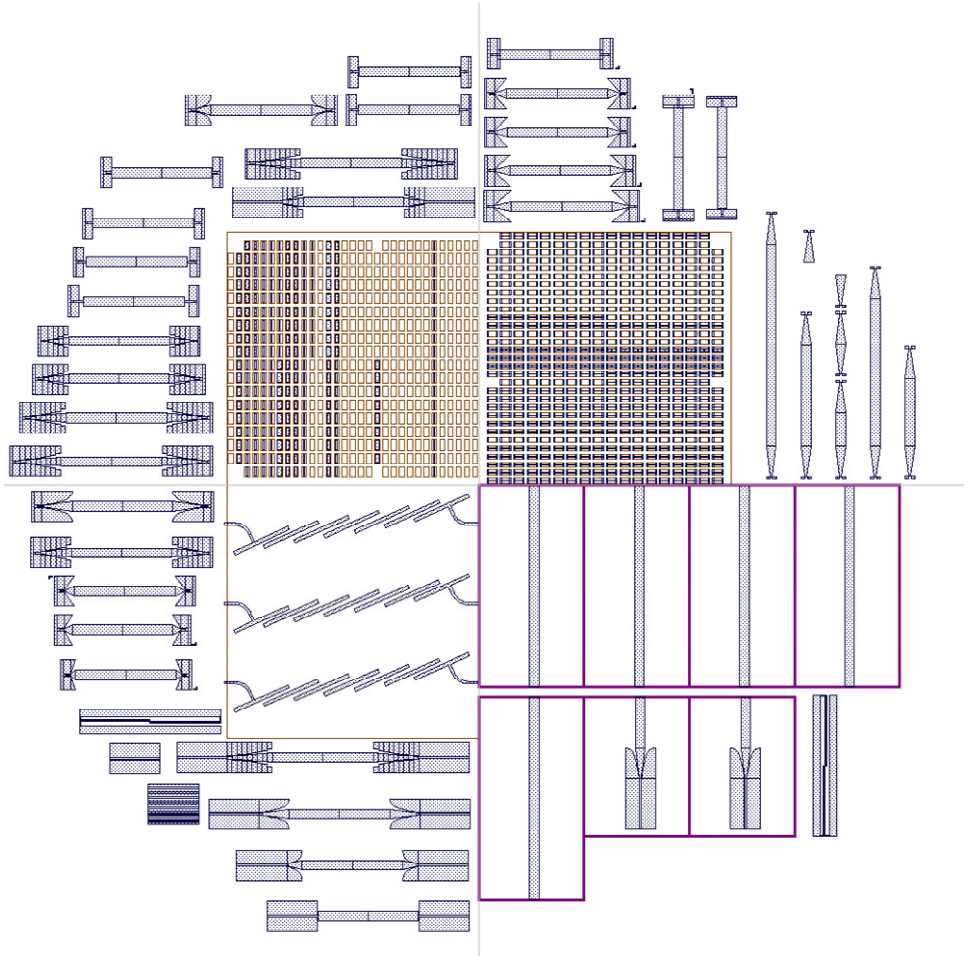


Figure 2.17: Transition mask layout.

The transition mask shown in Figure 2.17 is prepared with CADENCE Software with minimum feature size of 2 µm. The mask is a clear field mask, which means the shaded regions on the mask defines the areas where the metal layers remain on the wafer.

2.12.2. Pre-Process Stage

Wafer cleaning is the first pre-process step where the new wafers are cleansed from organic residues from the outside world environment. Wafers are placed in a wafer cassette and the cassette is left in piranha solution (H_2SO_4 +H_2O_2) for 30 minutes. When this step is completed, the wafers are washed with de-ionized water (DIW) so that the chemical is thoroughly removed from the wafer surface.

The next step after the wafer cleaning is the buffered HF (BHF) stage. BHF is a chemical which interacts with the glass molecules and etches the glass surface in order to improve the surface roughness so that the gold sticks more firmly to the surface of the wafer. The wafers are placed in to BHF (NH_4F:HF 7:1) solution for 30 seconds and the cassette holding the wafers is gently swung in the solution. DIW washing is applied to the wafers in order to remove the chemical off the wafers.

2.12.3. First Metallization Deposition Stage

The transition structures are single metal layered structures so this step defined the structures completely. The word "first" is used in the name of the stage since this stage is the same for any multi-layered structures. Before beginning the metal diposition, the wafers are initially baked in the oven at 120 °C for 30 minutes. This step is called the dehydration step which ensures the wafers to be completely dry so that the metal diposition is accomplished properly.

The base metallization is gold. The conductivity and the thickness of the metal play an important role on RF performance especially at high frequencies. Gold has a high conductiviy ($4.1x10^7$ S/m) and the thickness of the metal is aimed to be 2 µm

which is thick enough to decrease the loss of the structures which are electrically very long.

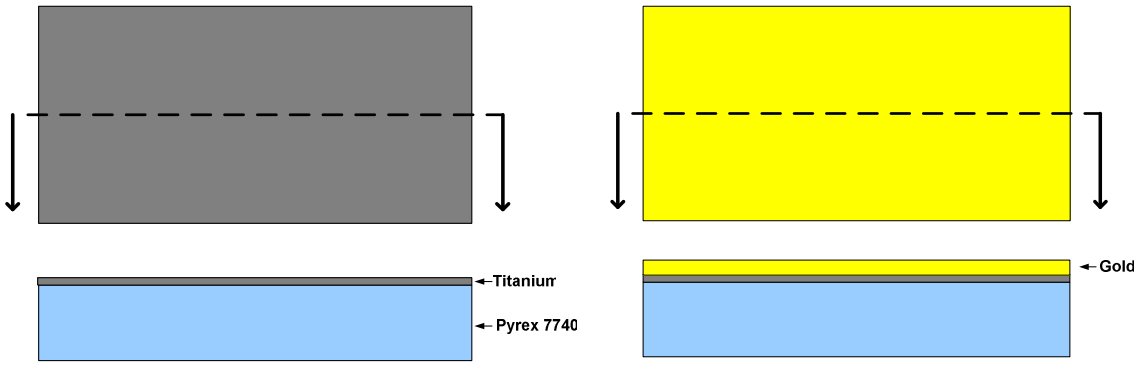
The gold does not stick to glass surface perfectly. A seed metal is required which sticks well to both glass and gold surfaces. Titanium is a metal which satisfies this condition and it is deposited as a very thin layer before the gold. When titanium diposition is completed, gold is dipositied on titanium layer. The diposition is realized the sputtering system. Sputter is a device which creates an electric field in its chamber. During the sputtering, the chamber consists of wafer, active gold and titanium targets and argon ions. The argon ions are accelerated with the electric field and collide with the metal target and scatter ions from the target. Then these metallic ions are directed to the wafer surface and under a certain pressure and flow conditions the ions are bonded on the glass surface. Adjusting the time of this process adjusts the thickness of the metal. Table 2.2 and Table 2.3 show the process recipe of sputtering of titanium and gold respectively. Figure 2.18 shows the schematics of the wafer after titanium and gold diposition.

Table 2.2: Process recipe for titanium deposition.

Sputtering for First Metallization – Ti	
Power – Current	300 W
DC bias	383 V
Temperature	120°C
Pressure	2.3e-3 mBar
Flow	2.4e-3 mBar
Endpoint	110A
Rate	1.2 Å /sec
Time 1 – Time 2	120 s - ~80 s

Table 2.3: Process recipe for gold deposition.

Sputtering for First Metallization – Au	
Power – Current	300 W
DC bias	440 V
Temperature	120°C
Pressure	13e-3 mBar
Flow	17.4e-3 mBar
Endpoint	2500A
Rate	4.9 Å /sec
Time 1 – Time 2	120 s - ~520 s



(a) Ti deposition **(b)** Au deposition

Figure 2.18 (a) – (b): Ti/Au deposition as the base metallization.

2.12.4. First Metallization Lithography Stage

When the sputtering step is completed, the titanium/gold (Ti/Au) layer must be patterned. To do this, the wafer is coated with a photoresist. Photoresist is a chemical whose chemical property changes when exposed to UV rays. The Shipley S1828 photoresist is spun on the the wafer using spinner.

Spinner is a device which has a rotating plate in a large semi-spherical cavity. The wafer is placed on this rotating plate and photoresist is spilled onto the wafer. With

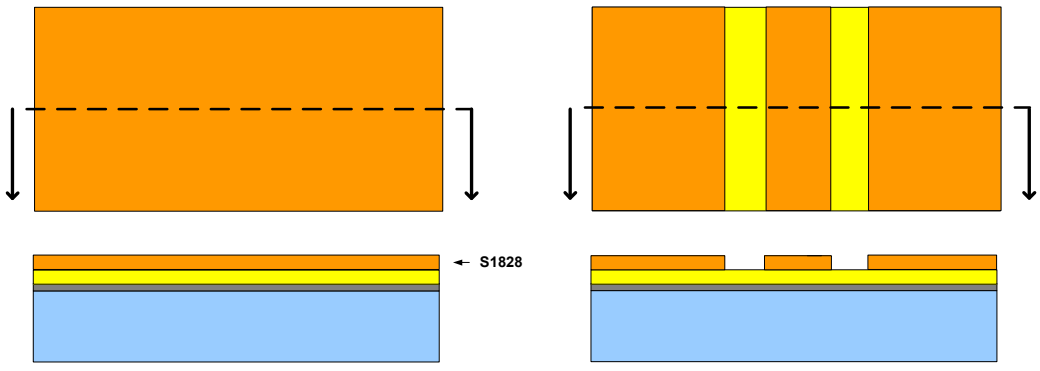
the speed of rotation, the centrifugial force spreads the photoresist uniformly in all directions. As a result, the speed of the rotation controls the thickness of the photoresist. The photoresist thickness is adjusted to be around 2 µm with the given recipe in Table 2.4. The wafer is soft-baked on a hot plate so that the photoresist gets more solid and does not stick to mask in the mask alignment and exposure steps.

When the wafer is coated with photoresist, it is ready to be patterned using the UV sensitivity of the photoresist. The wafer is aligned with the mask using the mask aligner. When the alignment is complete, UV light is applied to the aligned mask and wafer. The UV rays first go through the mask and then fall on the wafer surface. The areas shaded by the wafer are not exposed to UV rays so the chemical property of the photoresist remains unchanged.

The final step in the lithograpy is the development step, where the wafers are swung in a developer with the help of wafer holders. The developer is a chemical solvent which interacts with the photoresist and depending on the polarity of the photoresist, exposed or shaded areas of the photoresist dissolve in the solvent. If a photoresist is positive, when exposed to UV, the shaded areas remain on the wafer after the development and if it is negative, the exposed areas remain on the wafer. In this lithograpy, since positive photoresist is used since dark patterns on the mask correnspond to the metal layers of the structure. Table 2.4 gives the detailed recipe of the lithography and Figure 2.19 shows the schematic views of the wafer through the lithography steps.

Table 2.4: Process recipe for S1828 Lithography

Lithography using S1828	
Dehydration	120 C° 10 min in oven
Primer HDMS	@ 500 rpm dispense (5 secs acceleration from 0 rpm-7 secs duration- 3 secs acceleration to 3000 rpm) @2000 rpm spin (30 secs duration-3secs deceleration to 500 rpm) @ 500 rpm final speed (10 secs duration-3 secs deceleration to 0 rpm)
Spin **S 1828**	@ 500 rpm dispense (5 secs acceleration from 0 rpm-10 secs duration- 5 secs acceleration to 3750 rpm) @3750 rpm spin (30 secs duration-3 secs deceleration to 500 rpm) @ 500 rpm final speed (10 secs duration-3 secs deceleration to 0 rpm)
Softbake	115 C° on hotplate for 3:30 min (+30 secs hold the wafer close to the plate)
Exposure	16 secs @ 18 mW/cm^2
Development	1:45 min development in MF26 A solution
O_2 plasma	2 min duration Plasma power: 300 W Plasma pressure: 0.25-0.3 Torr
Hardbake	120°C 20 min in oven



(a) S1828 Coating **(b)** S1828 Patterning

Figure 2.19: Lithography with S1828.

2.12.5. First Metallization Etching Stage

The purpose of this step is to pattern the Ti/Au layer with the help of patterned photoresist and gold etchant. Photoresists are resistant to metal etchants. This feature enables the removal of the bare gold areas which are not covered with the photoresist. It is crucial to finish the etching right after the bare gold areas are etched so that no undercut occurs. Undercut happens when the wafer is left in the etchant for a long time that etchant begins to leak through the photoresist and interacts with the preserved gold areas. This effect shall be extremely hindered when the minimum resolution of the devices are in the order of a few micrometers.

The wafer is first swung in the gold etchant and then the titanium with durations given in Table 2.5 and Table 2.6 respectively. The etching times are very sensitive to environmental conditions like temperature and wafer swinging speed.

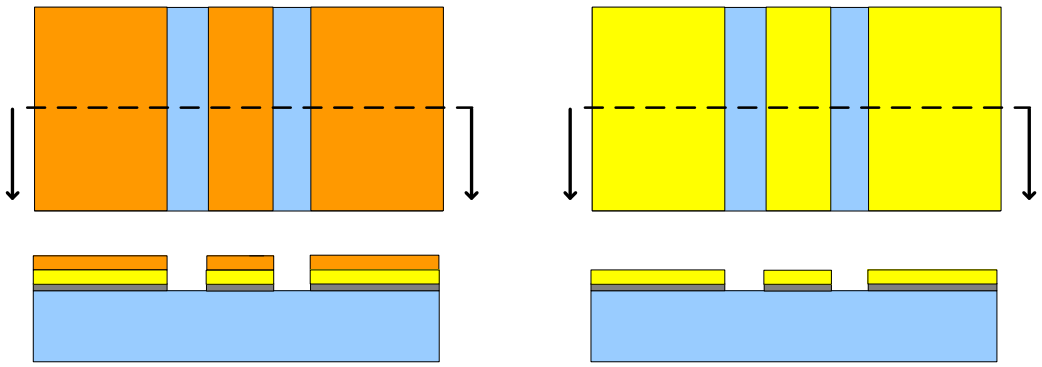
After the etching is completed, the photoresist on the remaining metal areas are to be removed. Acetone is a great chemical to rapidly wash off the photoresist. However it remains stains on the wafer surface. In order to remove these stains, Isopropyl alcohol (IPA) is applied right after acetone. The wafer is washed with DIW and placed into oxygen plasma. Oxygen plasma is used to get rid of any organic residues on wafer surface. The first metallization stage of the wafer is completed at this point. Figure 2.20 shows the schematics of etching and photoresist removal.

Table 2.5: Process recipe for Ti/Au etch.

Ti/Au Etch for First Metallization	
Au etch	Transene Au etchant 1:50 min
Ti etch	$HF:H_2O_2:DI$ (1:1:640) 2 min

Table 2.6: Process recipe for S1828 Strip.

Photoresist Strip	
Resist Strip	Acetone + IPA + DI rinse + IPA
O_2 plasma	5:00 min duration Plasma power: 300 W Plasma pressure: 0.7 Torr



(a) Ti/Au etch **(b)** Photoresist strip

Figure 2.20: Ti/Au etching and photoresist removal of the base metallization.

2.12.6. Backside Metallization Stage

When the front patterning of the wafer is completed, the backside of the wafer is coated with Ti/Au/Ti respectively in order to realize the conductor back of the CPW sections and ground of the microstrip sections. The procedure of this stage is the same as first metal sputtering. First titanium layer is deposited to create a seed layer for gold. Gold is sputtered on top of titanium to form the background metallization. These two steps are adequate for single metal layered structures. However if we had a structure with a second metallization, this backside metallization stage would be performed before the second metal sputtering. So an extra protective layer of titanium would be sputtered to protect the backside gold during the etching of the

second gold layer on the front side. This is the case in the filter structures which will be explained in the next chapter. The sputtering recipes for the three metal layers are given in Table 2.7.

Table 2.7: Process recipe for backside metallization.

Sputtering for Back Metallization – Ti	
Power - Current	300 W
DC bias	383 V
Temperature	Room Temp
Pressure	2.3e-3 mBar
Endpoint	110A
Rate	1.2 Å /sec
Time 1 - Time 2	120 s - ~80 s
Sputtering for Back Metallization – Au	
Power - Current	300 W
DC bias	440 V
Temperature	Room Temp
Pressure	5e-3 mBar
Endpoint	2500A
Rate	4.5 Å /sec
Time 1 - Time 2	60 s - ~550 s
Sputtering for Back Metallization – Ti	
Endpoint	200A

Figure 2.21 and Figure 2.22 show the Veeco Surface Profiler screenshots and measured metal thickness of the staircase and polynomial type transitions. The first metallization thickness is pretty uniform on the wafer which is around 1.3 µm. In each structure unnegligible metal uniformities below 0.1 µm are observed.

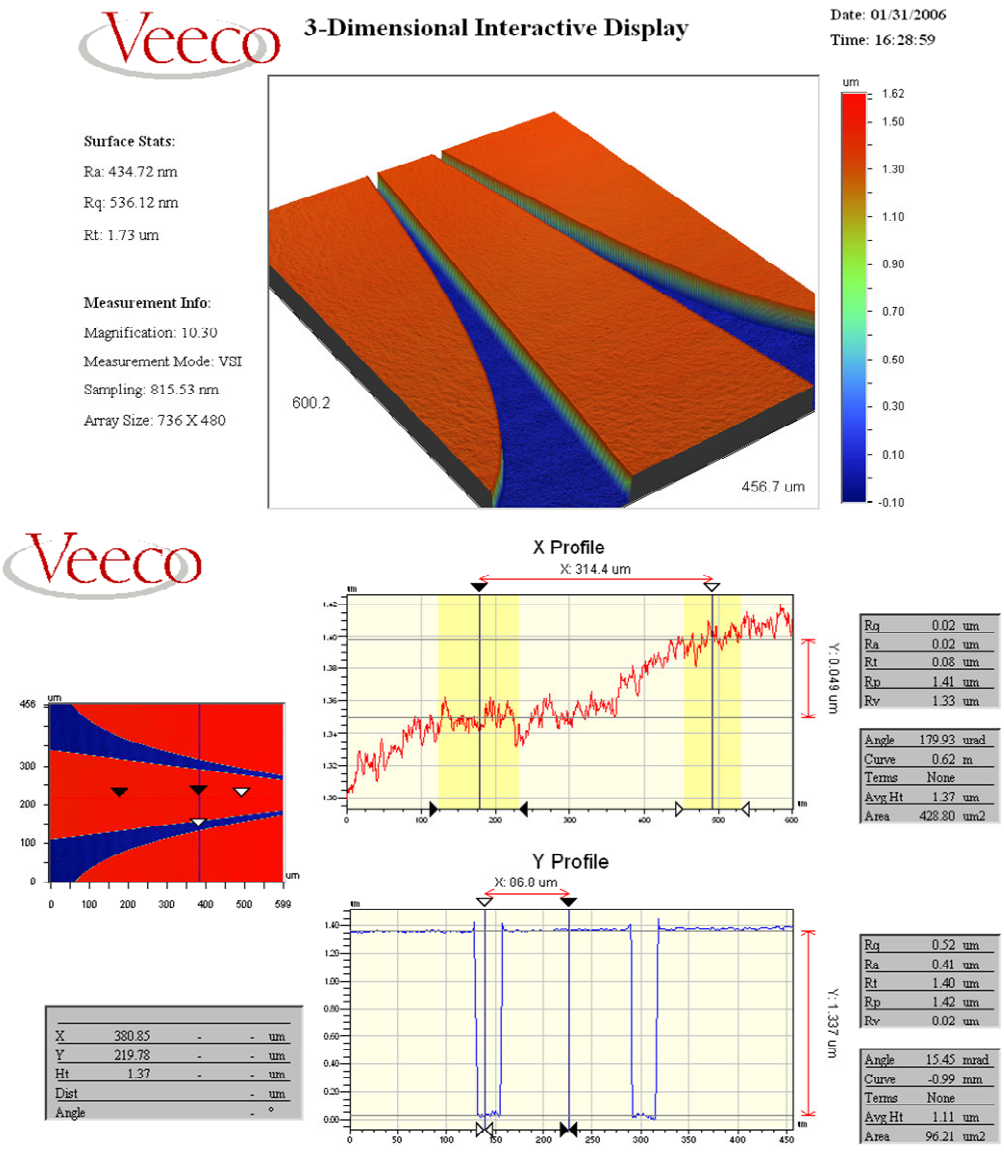


Figure 2.21: Surface profiler measurements a polynomial type transition.

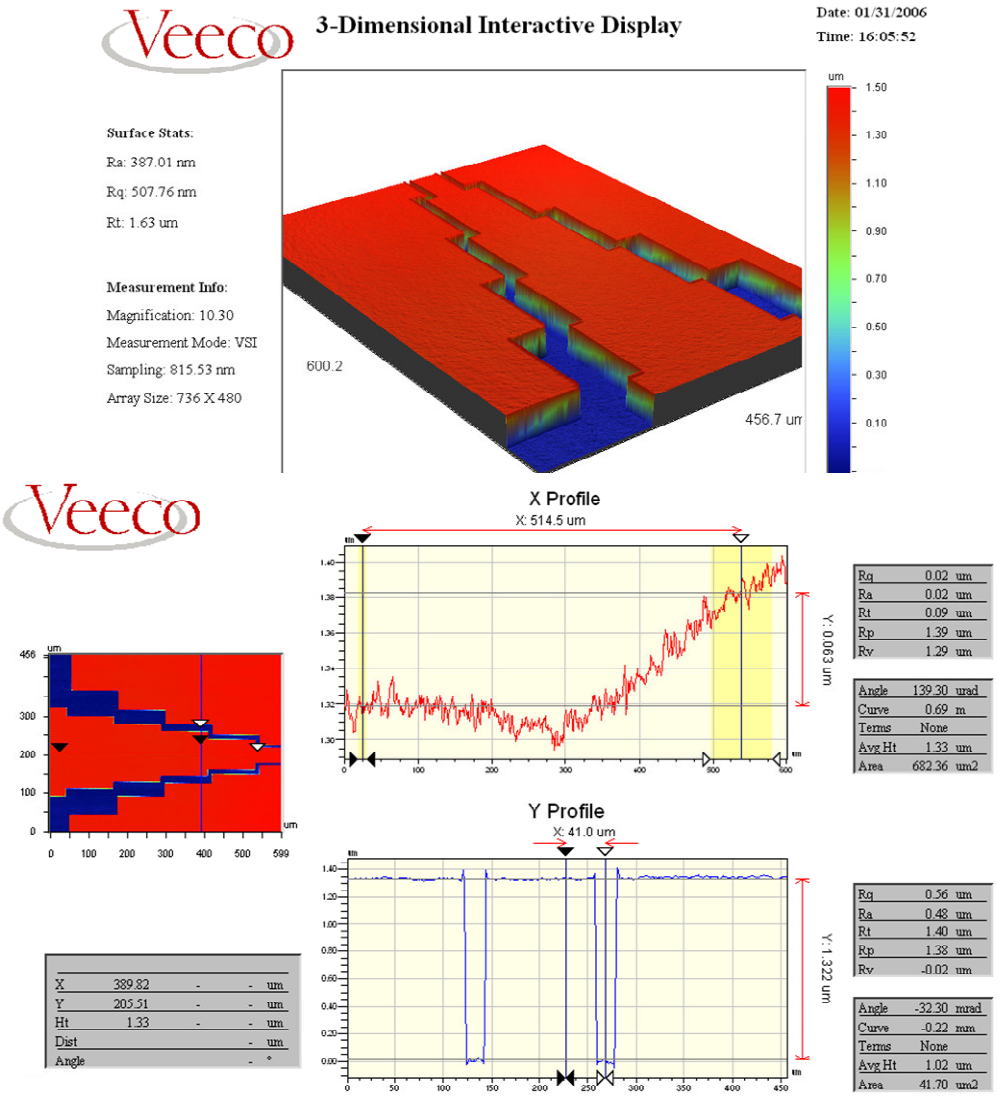
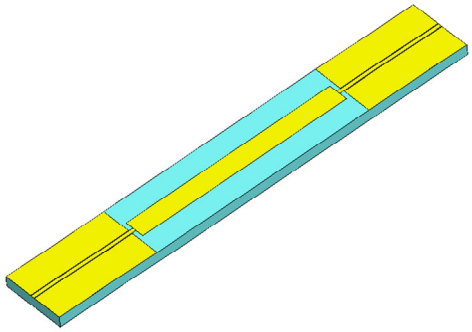


Figure 2.22: Surface profiler measurements a staircase type transition.

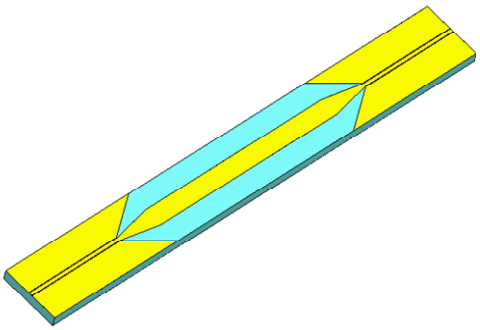
2.13. Measurement Results

The S-parameter measurements of the fabricated transition structures are done with network analyzer where the connections to the structures are realized with the air coplanar probes of the probe station. Since the probe dimensions are compatible with the CPW dimensions, Short-Open-Load-Through (SOLT) calibration is performed so that the reference plane is carried to the input ports of the transition

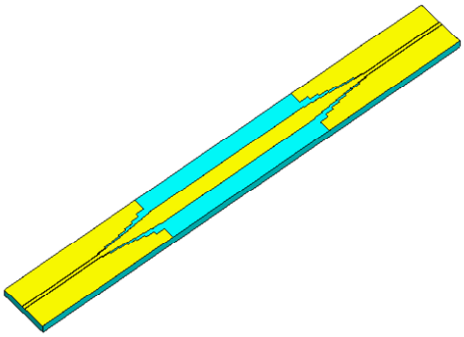
structures. The measurement frequency range is set to 1 – 20 GHz and the number of samples in this band is set to be 801. Since the measurements setup probes are coplanar ended, the transition structures are fabricated as back-to-back versions of the simulated designs as shown in Figure 2.23. In other words, the structures are fabricated with a mirror image of itself at the microstrip end so that both input and output ports are CPW.



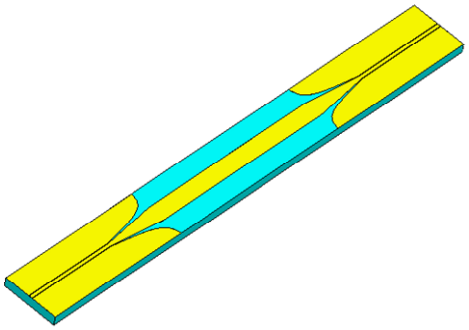
(a) Direct back-to-back transition



(b) Linear back-to-back transition



(c) Staircase back-to-back transition



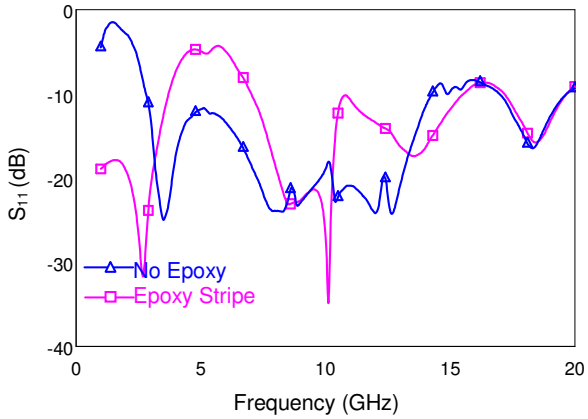
(d) Polynomial back-to-back transition

Figure 2.23 (a) – (d): Back-to-back transition geometries.

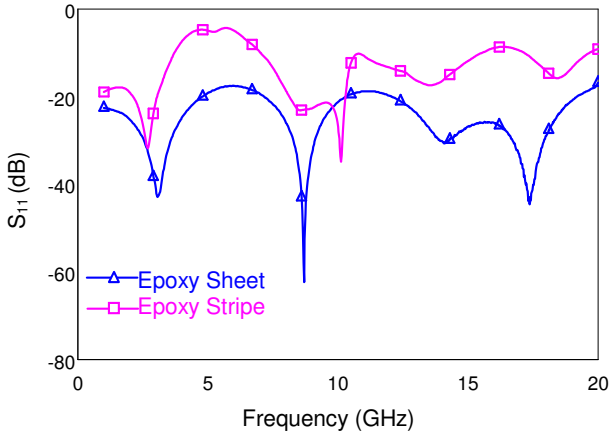
In order to analyze the transition characteristics accurately, the back-to-back structures are simulated with ANSOFT HFSS v9.2^{TM} and the measurement results are compared to the simulations.

The characteristics of the transitions are measured in two stages. The first stage is the on wafer measurement stage. In this stage wafer is not diced and all the samples are measured in their on wafer positions. The second stage is the measurement after dicing. When the samples are diced, they are separated from each other, so individual modifications to each sample can be done. Applying these two stages is compulsory due to the fact that each design has five separate grounds, two grounds on each two CBCPW sections and a ground as the backside metallization required for the microstrip and CBCPW sections. The measurement results given in Figure 2.24 clearly highlight the importance of proper grounding especially at low frequencies where the capacitane between the top metallization and backside metallization is effective when these metal layers are not electrically shorted.

The electrical connection between each of the five grounds is accomplished with silver epoxy which is applied from each side of the CPW grounds to a bottom metal plate on which the sample is firmly placed, providing a proper DC connection. Figure 2.25 and Figure 2.26 show the pictures of the fabricated structures with and without epoxy connections. Here, another issue becomes important. The conductive silver epoxy has a certain resistance and this resistance shall be set to minimum in order to have a better shorting between the parallel plates. The epoxy is first applied as a thin stripe between CPW grounds and base metal plate. The capacitance effect is greatly diminished at low frequencies but reflections are measured to be too high especially in the X-band. The reason for not having a fine transition in the entire 1 – 20 GHz is that the thin stripe of silver epoxy has an unnegligible resistance since the area of the current flow is low. Also due to inhomogenous structure of the epoxy stripe and its junction with the base plate, the S_{11} parameters of the transitions is greatly distorted in the frequency band except low and high frequency ends. In order to suppress this effect, the silver expoxy is applied as a conductive sheet between the CPW grounds and the bottom metal plate. In this way the resistivity of the epoxy is greatly diminished since the area of the resistor is increased and the simulated and measured S – parameters almost match each other.



(a) Measured S_{11} magnitude comparison of Epoxy Stripe vs. No Epoxy



(b) Measured S_{11} magnitude comparison of Epoxy Stripe vs. Epoxy Sheet

Figure 2.24 (a) – (b): Epoxy applications in stripe and sheet forms.

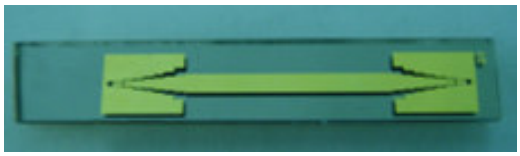


Figure 2.25: Picture of a diced single 6 step staircase transition without epoxy connections.

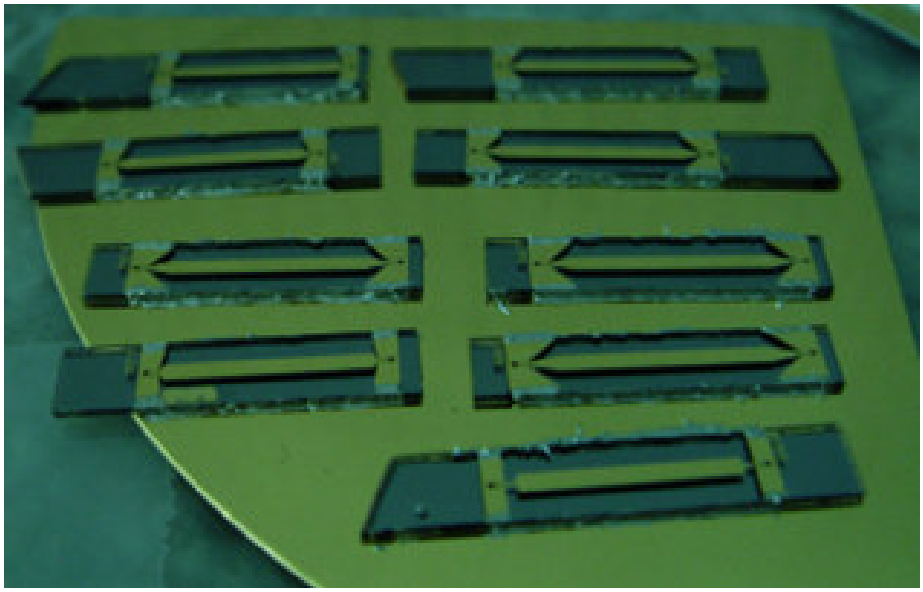


Figure 2.26: Picture of some direct and linear transition structures with epoxy connections to a common base metal plate.

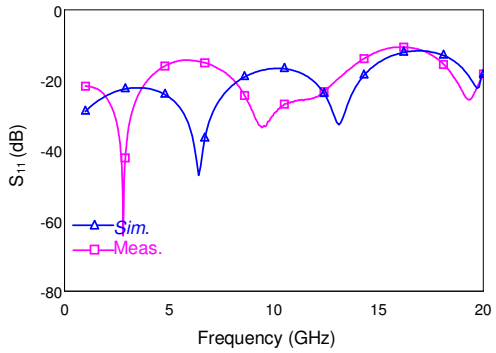
The general characteristics of the S-parameter simulations of back-to-back and single type of all kind of transition models alter due to the doubled length of the device which introduces an increase in the number of dips and an increased conduction loss. The reflection measurements mostly agree with the EM simulations. The differences between the measurements and the simulations may stem from the small dimension changes due to process conditions and epoxy application.

The insertion loss characteristics of simulations and measurements are observed to be different from each other. The measured S_{21} parameters are lower than simulated parameters. The main reason for such a deviation may be the improper loss calculation of the EM simulator with respect to the measurements. The metal loss modeling of the metal loss in EM simulator may be too ideal to match with real conduction losses within the wafer metallization. Also, this deviation may be

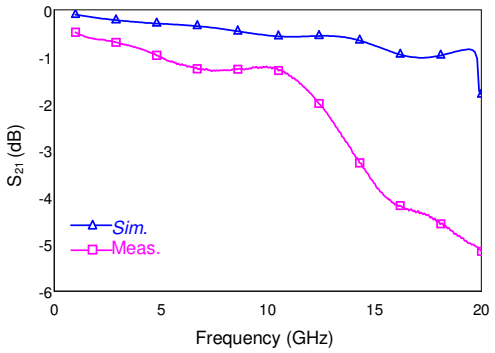
present due to inefficient measurement environment which introduce extra loss to the response of the overall setup or the radiation loss. Another important reason for the mismatch may be changes occurred on the device due to the process conditions and epoxy application which introduce extra loss to the structures.

2.13.1. Measurement Results of Direct Type Transition

Direct transition with transition lengths of 25, 100, 200, 300 and 500 µm are fabricated. S_{11} parameters around -20 dB up to 5 GHz have been obtained with transition lengths of 25 and 100 µm as shown in Figure 2.27, Figure 2.28, and Figure 2.29. The reflections are getting higher at high frequencies as the transition length increases which is an expected behaviour from the EM simulations. However the reflection parameter S_{11} is kept below -20 dB up to 6 GHz for 25, 100 and 200 µm structures. When the transition section length increases more than 300 µm, the reflection characteristics become worse and a low loss transition is not achieved.

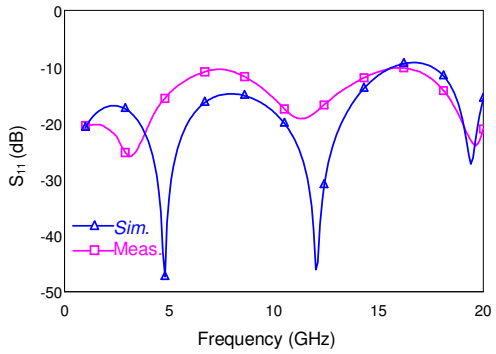


(a) S_{11} of 25 µm direct transition

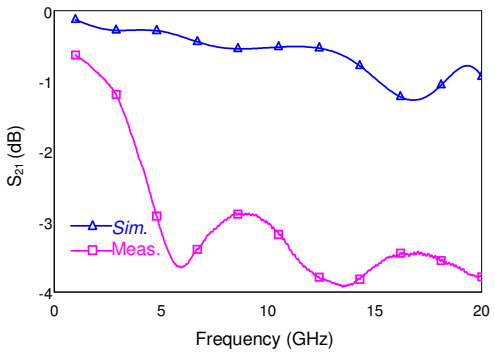


(b) S_{21} of 25 µm direct transition

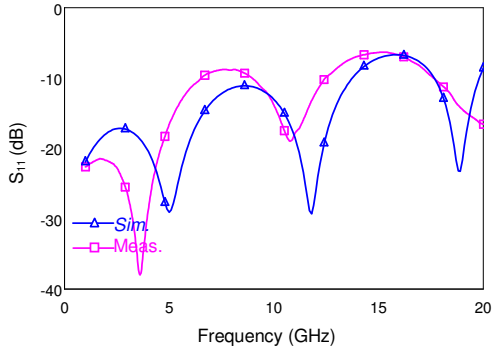
Figure 2.27 (a) – (b): Measurement results of back-to-back 25 µm direct transition structures in comparison with simulations



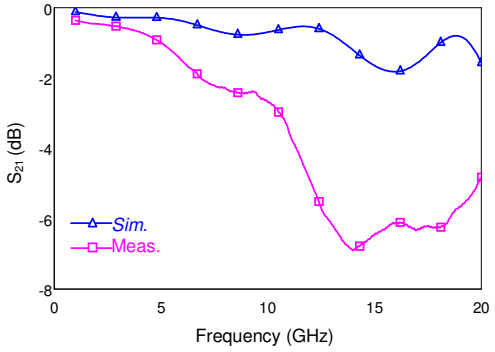
(a) S_{11} of 100 µm direct transition



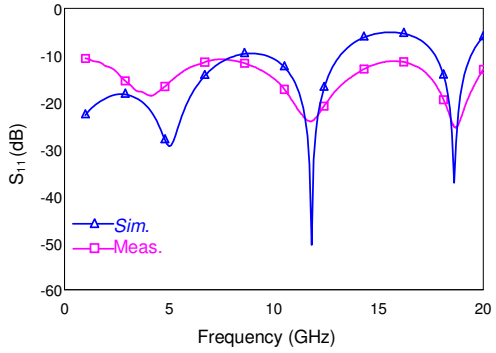
(b) S_{21} of 100 µm direct transition



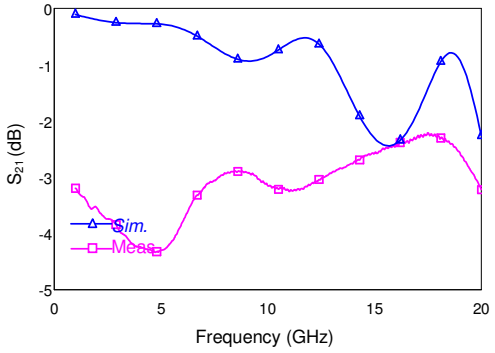
(c) S_{11} of 200 µm direct transition



(d) S_{21} of 200 µm direct transition

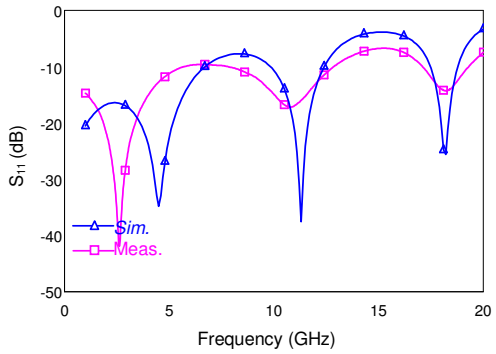


(e) S_{11} of 300 µm direct transition

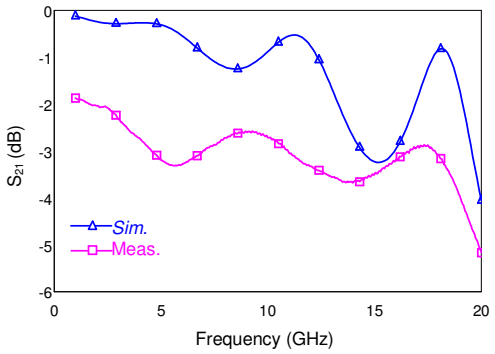


(f) S_{21} of 300 µm direct transition

Figure 2.28 (a) – (f): Measurement results of back-to-back 100 µm to 300 µm direct transition structures in comparison with simulations.



(a) S_{11} of 500 µm direct transition

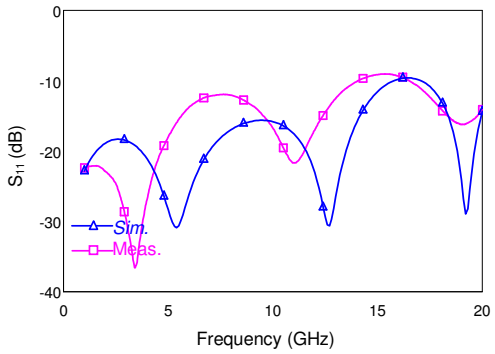


(b) S_{21} of 500 µm direct transition

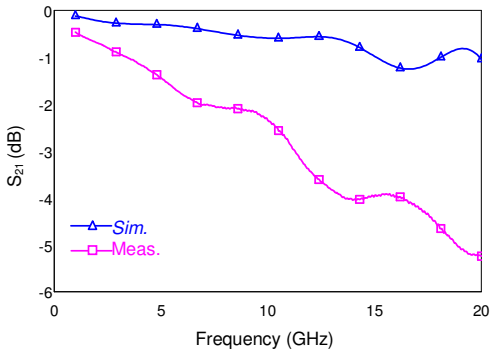
Figure 2.29 (a) – (b): Measurement results of back-to-back 500 µm direct transition structures in comparison with simulations.

2.13.2. Measurement Results of Linear Type Transition

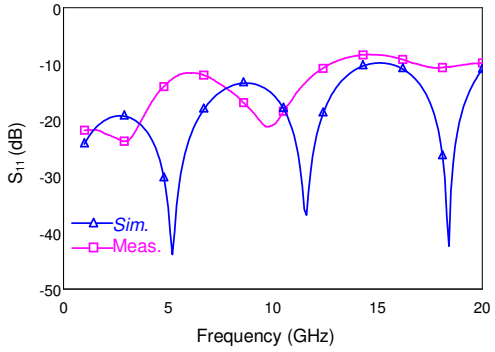
Linear type transitions with transition lengths 250, 500, 750, 1000, 1250, 1500 and 1750 µm have been fabricated and the measurements results are compared with back-to-back simulations as shown in Figure 2.30, Figure 2.31, and Figure 2.32. The reflection parameter of this type of transition is observed to be less than -15 dB up to 5 GHz and below -7.5 dB in the complete frequency band for all variants. Insertion loss characteristics of the measured and simulated results are in better agreement where the transition is not very low loss at longer transition sections. The reason for this agreement may be the fact that the dominant effect of the insertion loss becomes the characteristic impedance mismatch rather than purely metallic loss



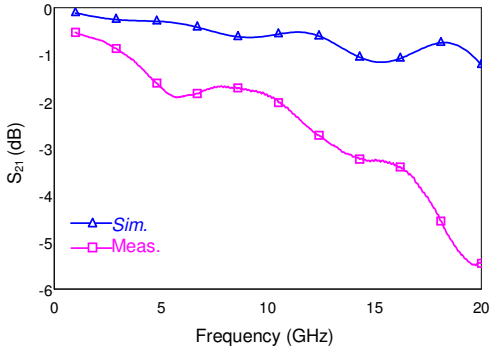
(a) S_{11} of 250 µm linear transition



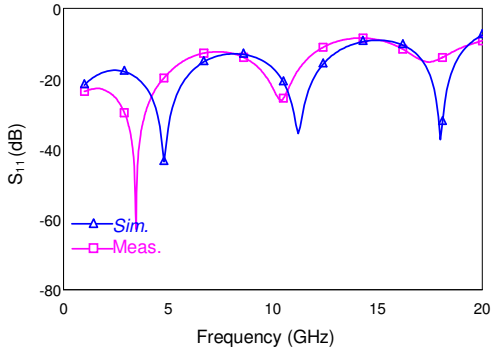
(b) S_{21} of 250 µm linear transition



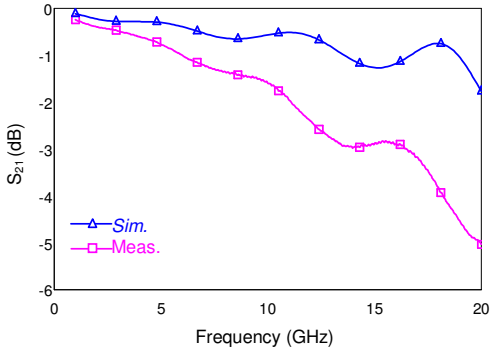
(c) S_{11} of 500 µm linear transition



(d) S_{21} of 500 µm linear transition

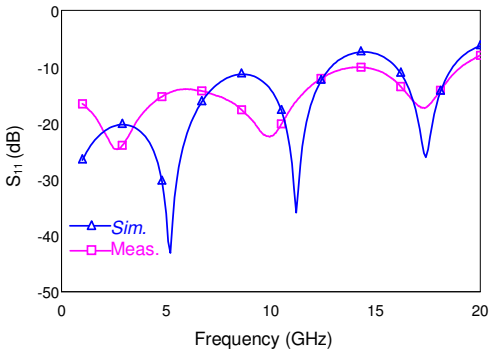


(e) S_{11} of 750 µm linear transition

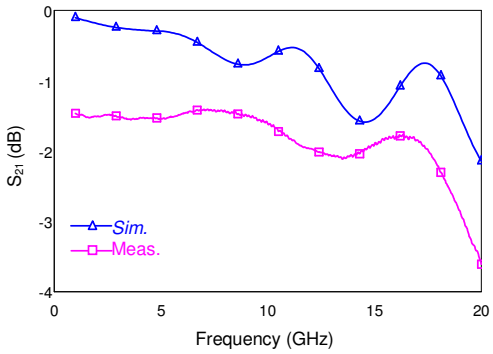


(f) S_{21} of 750 µm linear transition

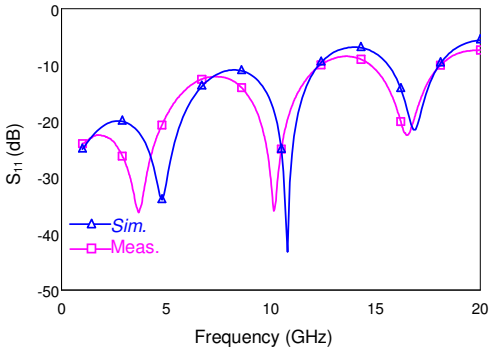
Figure 2.30 (a) – (f): Measurement results of back-to-back 250 µm to 750 µm linear transition structures in comparison with simulations.



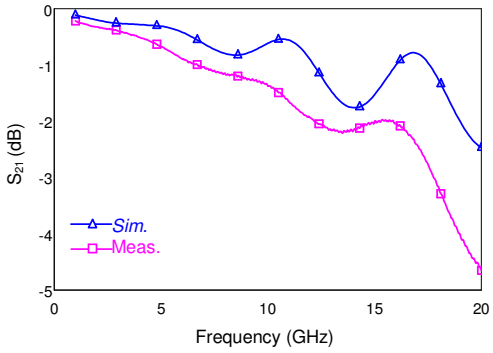
(a) S_{11} of 1000 µm linear transition



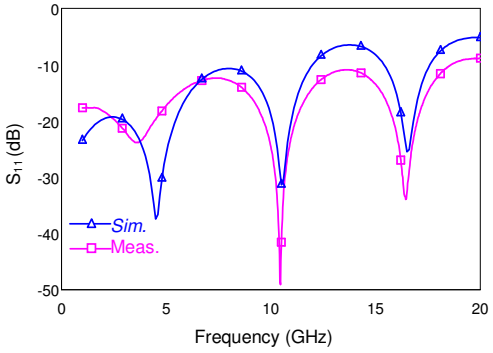
(b) S_{21} of 1000 µm linear transition



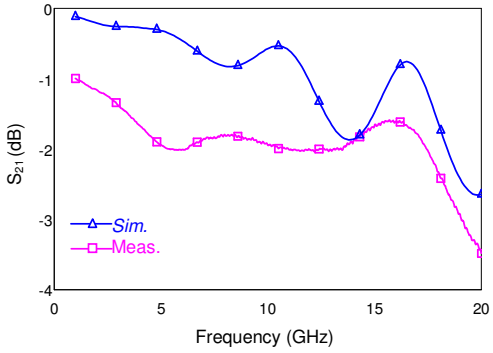
(c) S_{11} of 1250 µm linear transition



(d) S_{21} of 1250 µm linear transition

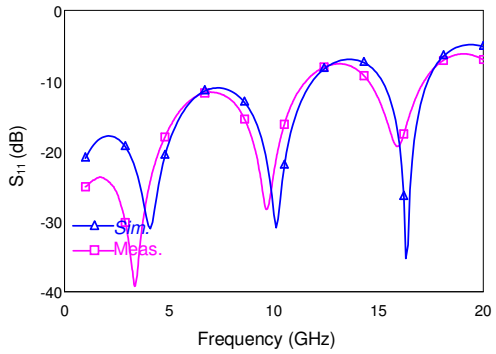


(e) S_{11} of 1500 µm linear transition

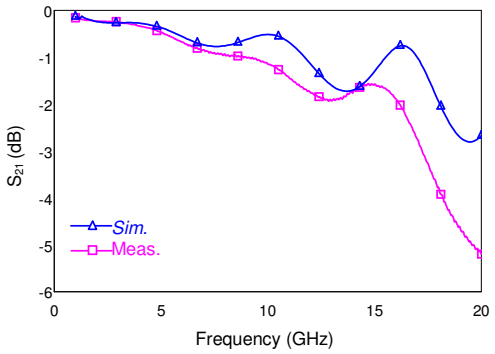


(f) S_{21} of 1500 µm linear transition

Figure 2.31 (a) – (f): Measurement results of back-to-back 1000 µm to 1500 µm linear transition structures in comparison with simulations.



(a) S_{11} of 1750 µm linear transition

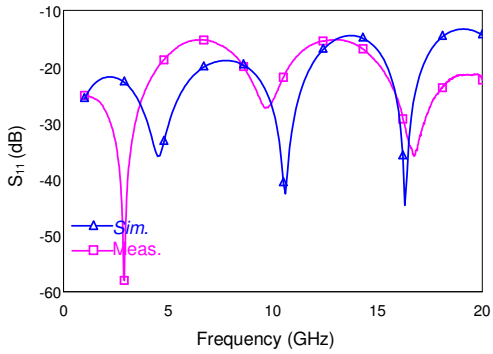


(b) S_{21} of 1750 µm linear transition

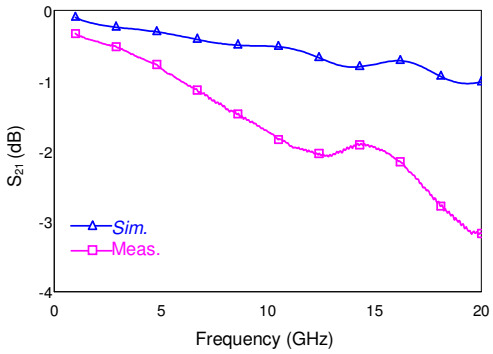
Figure 2.32 (a) – (b): Measurement results of back-to-back 1750 µm linear transition structures in comparison with simulations.

2.13.3. Measurement Results of Staircase Type Transition

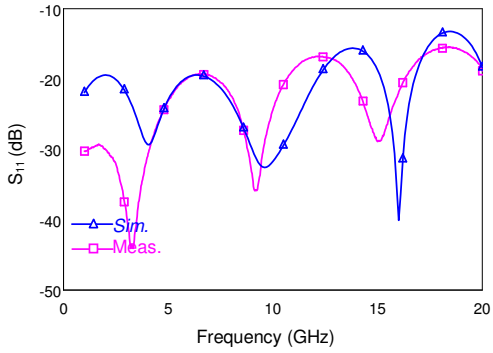
Staircase type transitions with step numbers of 4, 5, 7, 8, and 9 are fabricated and measurements are compared to the simulations as shown in Figure 2.33 and Figure 2.34. S_{11} parameters of the 4 step transition are observed to be below -20 dB in 1 – 5 GHz and 15 – 20 GHz bands, and below -15 dB elsewhere. The 5 step transition provides a lower reflection, less than -19.37 dB for frequencies below 10 GHz and below -15.5 dB in the rest of the band. Reflection is measured to be the lowest, where S_{11} is below -17.53 dB in the entire frequency band with the 7-step transition. The dips of the transition line characteristics of the measurements agree well with the simulations. The S_{11} response goes over -20 dB barrier within 7 – 8 GHz and 18 – 20 GHz band for the 8 step transition and 3 – 5 GHz band for the 9 step transition. In the rest of the frequency band the reflection is measured to be below –20 dB for both of the designs.



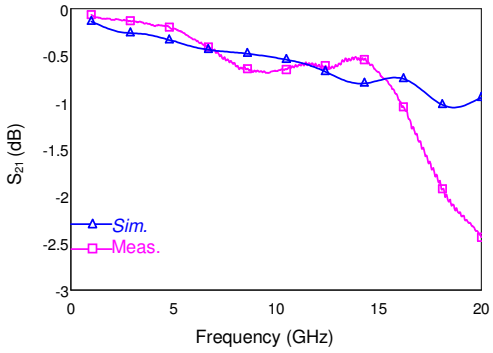
(a) S_{11} of 4 step transition



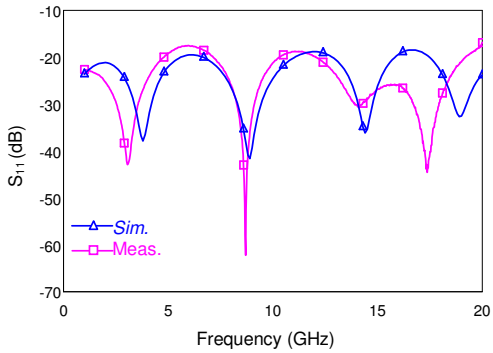
(b) S_{21} of 4 step transition



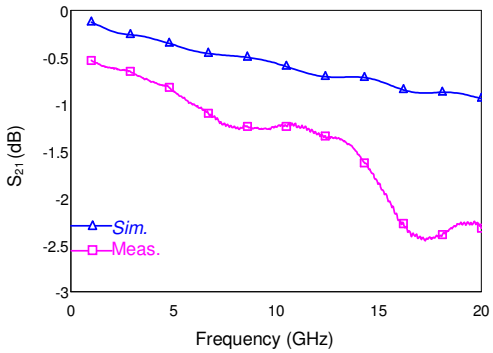
(c) S_{11} of 5 step transition



(d) S_{21} of 5 step transition

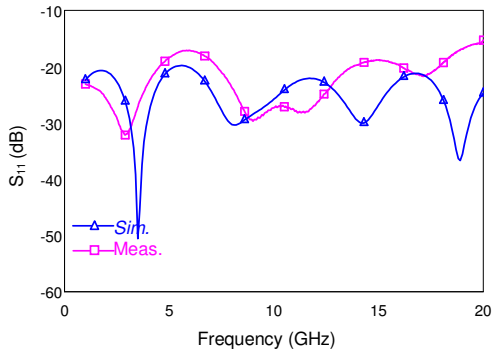


(e) S_{11} of 7 step transition

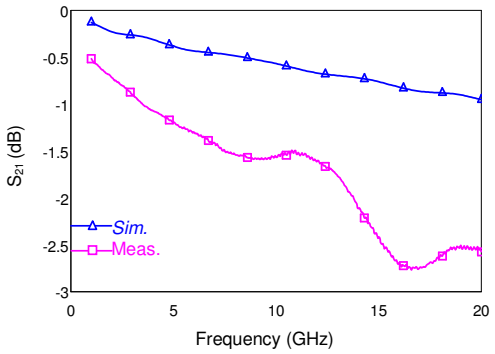


(f) S_{21} of 7 step transition

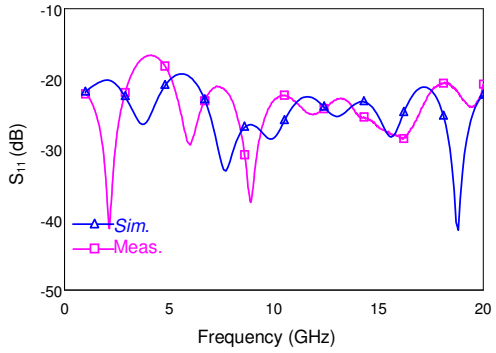
Figure 2.33 (a) – (f): Measurement results of back-to-back 4 to 7 step staircase transition structures in comparison with simulations.



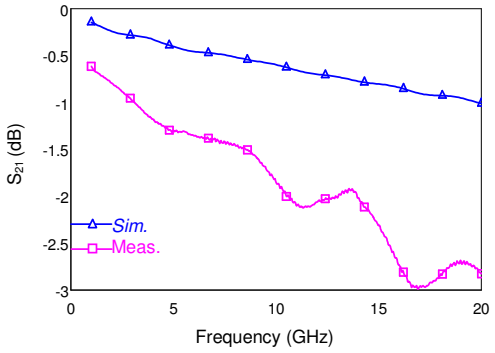
(a) S_{11} of 8 step transition



(b) S_{21} of 8 step transition



(c) S_{11} of 9 step transition



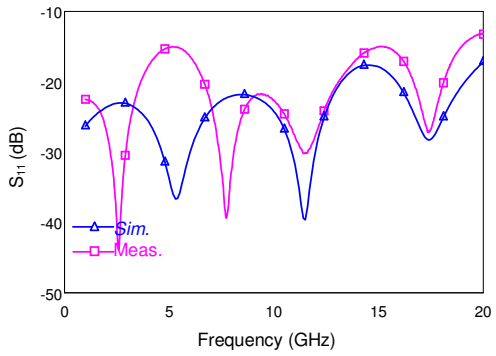
(d) S_{21} of 9 step transition

Figure 2.34 (a) – (d): Measurement results of back-to-back 8 and 9 step staircase transition structures in comparison with simulations.

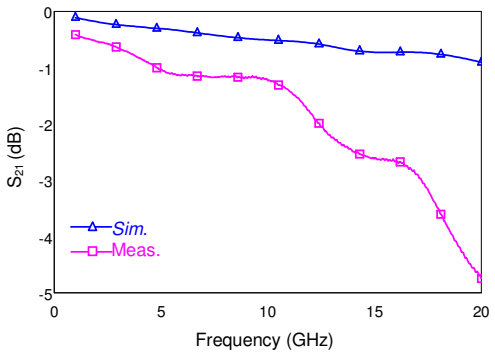
2.13.4. Measurement Results of Polynomial Type Transition

Two variants of polynomial type transitions have been fabricated and measured. The S_{11} results of the 1500 µm long transition structure is not as satisfactory as expected especially in the 3-6 GHz and 15-20 GHz frequency bands where the reflection goes over -15 dB. The reason may be the improper epoxy implementation or the undercuts in the metal layer which occur in the etching stage of the base metallization. For 3000 µm long transition, the reflection is below -20 dB for

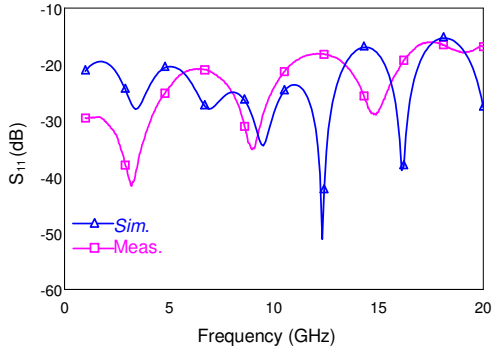
frequencies up to 11 GHz and below -16.23 dB between 18 and 20 GHz. Figure 2.35 shows the simulated and measured s-parameters of the structures.



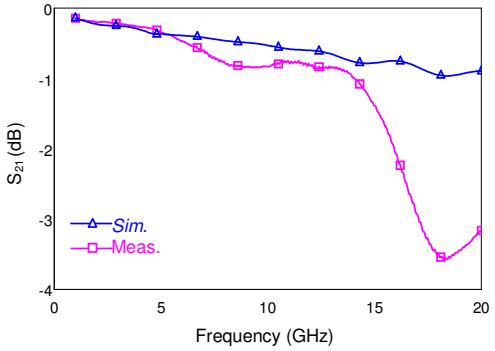
(a) S_{11} of 1500 µm polynomial transition



(b) S_{21} of 1500 µm polynomial transition



(c) S_{11} of 3000 µm polynomial transition



(d) S_{21} of 3000 µm polynomial transition

Figure 2.35 (a) – (d): Measurement results of back-to-back polynomial transition structures in comparison with simulations.

2.14. Discussions

When we compare the single transition simulation results with the ideal transition simulation results, the best transition has 10 dB more reflection than the ideal case where the maximum S_{11} is obtained around -35 dB. The main reason is that the ideal case simulation is done with Microwave Office (MWO) using MOM and the

transition simulations are performed with ANSOFT HFSS 9.2 using FEM. It is observed that for certain CPW geometry, HFSS calculates the port impedance 1-2 Ω more than what MWO calculates. Also during the simulation phase the losses and field distributions are not perfectly same for both simulators. Surely the dominant reason for this difference is the effect of transition discontinuities and introduced extra transition length. But when we compare the simulated back-to-back results and the measurement results, it is clearly seen that the characteristics of the plots are in well agreement.

The transition is desired to be low loss however the compactness may play a more important role in structures which have certain dimension constraints. So there may be a compromise between transition length and transition quality in most cases.

Table 2.8 gives the measured maximum reflection coefficients by giving the maximum S_{11} (dB) values for certain frequency bands.

Table 2.8: Maximum S_{11} (dB) values for 1-8, 8-12, and 10-18 GHz frequency bands

Transition Type	Transition Length (um)	max S11 (dB) 1-8 GHz	max S11 (dB) 10-18 GHz	max S11 (dB) 8-12 GHz
Direct 25	25	-14,25	-10,56	-19,6
Direct 100	100	-10,46	-10,2	-11
Direct 200	200	-8,76	-6,31	-9
Direct 300	300	-10,66	-11,26	-11,2
Direct 500	500	-9,57	-6,71	-10,16
Linear 250	250	-12,13	-8,6	-12,13
Linear 500	500	-11,57	-8,34	-11,76
Linear 750	750	-12,32	-8,38	-12,75
Linear 1000	1000	-14	-10,1	-13,28
Linear 1250	1250	-12,03	-8,43	-12,57
Linear 1500	1500	-12,4	-10,9	-12,84
Linear 1750	1750	-11,64	-7,5	-8,8
Step 4	2000	-15,2	-15,17	-16,11
Step 5	2500	-19,37	-15,5	-16,89
Step 7	3500	-17,53	-18,74	-18,8
Step 8	4000	-17,15	-18,79	-24
Step 9	4500	-16,62	-20,8	-23,55
Poly 1500	1500	-15,03	-15	-22,42
Poly 3000	3000	-20,89	-16,23	-19

For 1-8 GHz band, the direct 25 model gives a very efficient transition, max S_{11} below -14.25 dB, in an extremely small transition length of 25 µm. The staircase transitions have higher quality transition characteristics, where step 5 has maximum S_{11} of -19.37 dB for 2500 µm long transition section. Lowest reflection is obtained with poly 3000 model with maximum S_{11} -20.89 dB however the transition length is increased to 3000 µm. Comparing the direct 25 and poly 3000 models, the S_{11} is improved by -6.64 dB in poly 3000 but the transition length is 120 times the transition length of direct 25. Figure 2.36 shows the complete set of structures with their maximum S_{11} values and transition lengths.

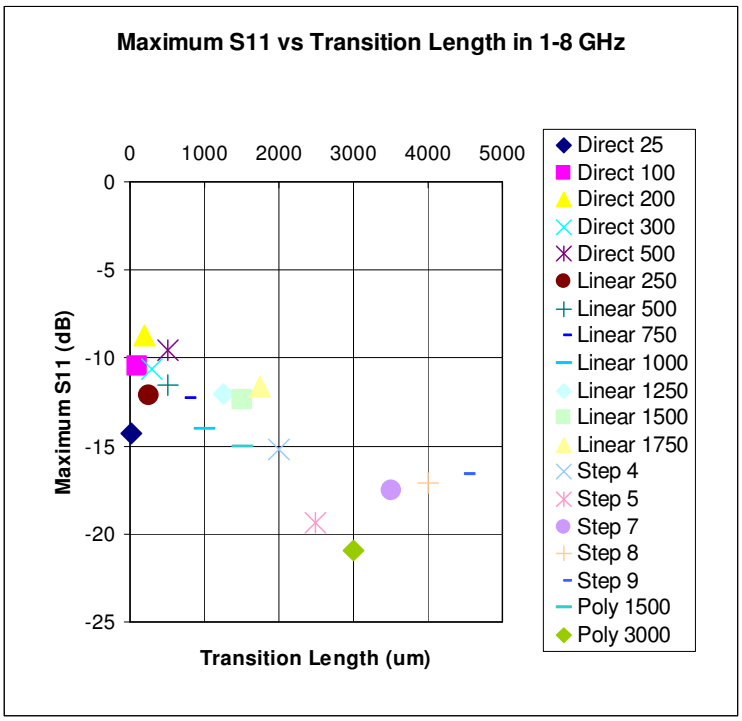


Figure 2.36: Maximum S_{11} vs. Transition Length Plot in 1-8 GHz.

As seen in Figure 2.37 for X – band frequencies, i.e. 8-12 GHz, the reflections of direct 25 transition structure are still very low, S_{11} is below -19,6 dB in the entire band. Linear 1000 model has the best transition characteristic in its class where

maximum S_{11} is below -13.28 dB. Step 8, step 9 and polynomial transition structures show a high reflection quality and poly 1500 model has a very low maximum S_{11} which is only -27.42 dB with a transition length of 1500 µm.

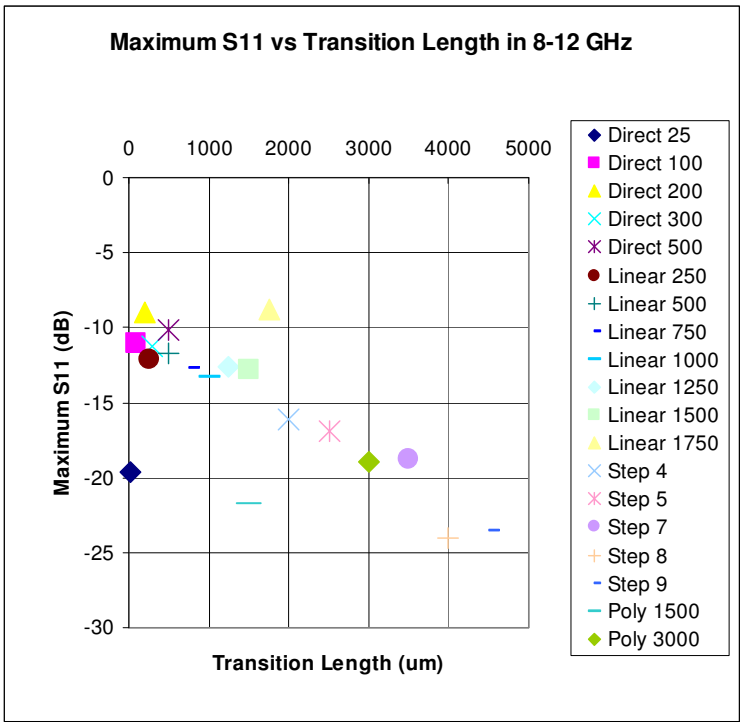


Figure 2.37: Maximum S_{11} vs. Transition Length Plot in 8-12 GHz.

For 10-18 GHz frequency band, the reflections of direct transition structures are getting worse with respect to lower frequency reflection results. Also the linear transition structures show poor reflection quality. However for staircase and polynomial transitions, the maximum S_{11} value is below -15 dB for all cases. For step 9, the lowest reflection is observed where S_{11} is below -20.8 dB. For high frequencies, it is compulsory to have a large transition area to maintain a satisfactory transition. The related graph can be observed in Figure 2.38.

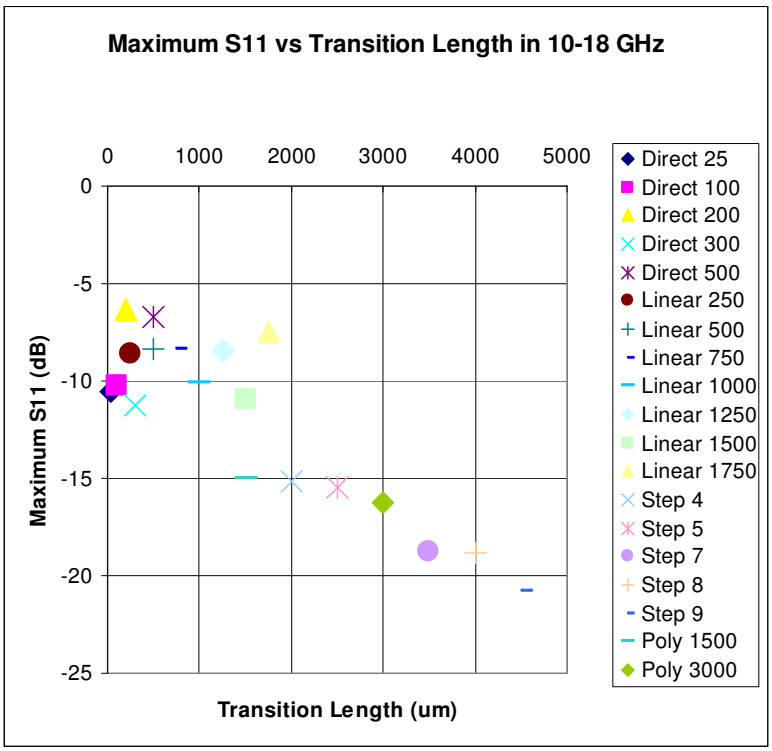


Figure 2.38: Maximum S_{11} vs. Transition Length Plot in 10-18 GHz.

Due to its low-loss transition characteristics in broad-band, the polynomial type transition is used in the integration of phase shifters and antennas in a phased array antenna system. Figure 2.39 gives the pictures of a fabricated phased array system which uses polynomial transitions as interconnecting elements between CPW and microstrip structures.

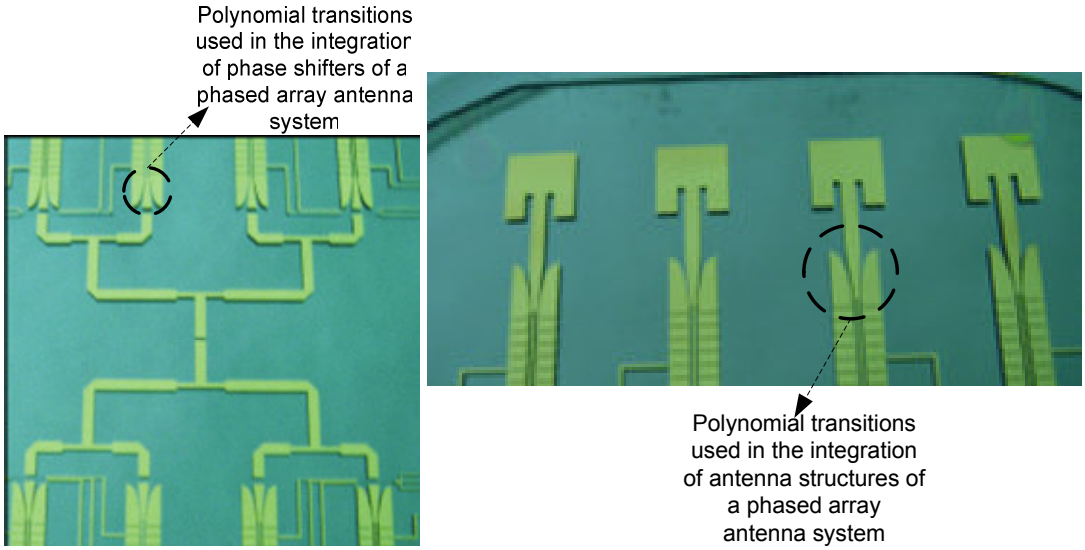
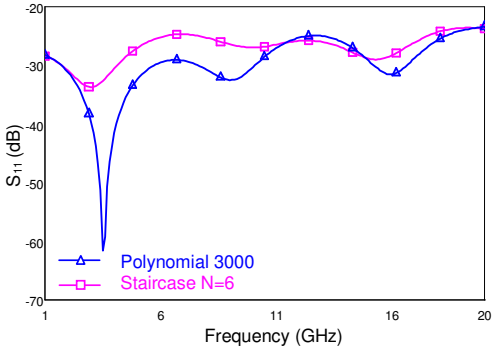
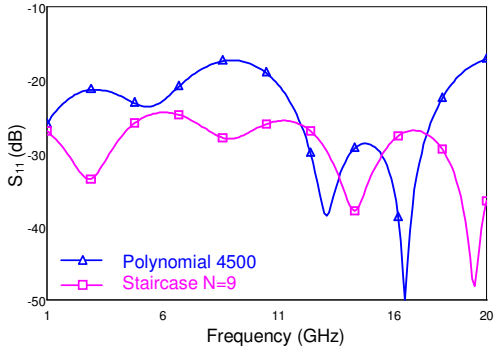


Figure 2.39: Pictures of polynomial transitions used in a phased array antenna system.

It is also sensible to compare the transition characteristics of the staircase and polynomial models with the same transition length. Figure 2.40 shows the simulation results of simple CPW-microstrip transitions realized in 3000 and 4500 µm. It is noticed that for 3000 µm, the polynomial transition has lower reflections up to 11 GHz; however for 4500 µm, the staircase model has lower reflections in the entire band. It is important to note once more that the polynomial model is composed of 30 horizontal sections where the dimensions are adjusted for a "50 Ω" characteristic impedance, and these sections are connected linearly in between. When the transition length gets very large, these unmatched line segments begin to disturb the low-loss characteristics of the structure. It may be concluded that for transition lengths, say up to 3000 µm 30 point structure is satisfactory but if the transition length is desired to be made longer, then the number of points shall be increased to maintain the low-reflection characteristics. The staircase model does not suffer such a problem since it has only step discontinuities which remain the same regardless what the total length is.



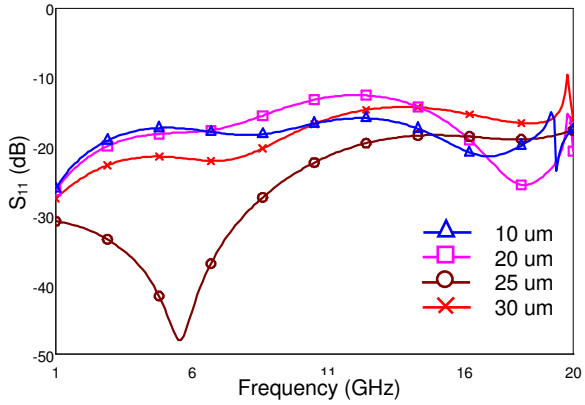
(a) S_{11} comparison for 3000 µm long transitions.



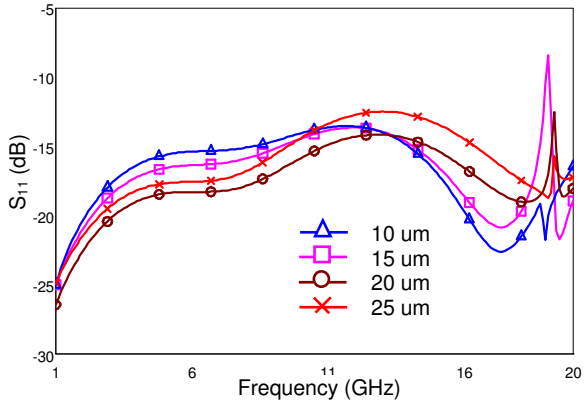
(b) S_{11} comparison for 4500 µm long transitions.

Figure 2.40 (a) – (b): Comparison of staircase and polynomial models within a same transition length.

In the direct transition, an interesting conclusion is observed while investigating the relation between the signal-ground gap of the CPW section and the transition length. When the transition length is equal to CPW signal-ground gap length, the reflection is lower with respect to other transition gap lengths. To support this idea, simulations for two different CPW structures, 150 µm-20 µm and 170 µm-25 µm with various transition gaps are performed. The simulated reflection characteristics are shown in Figure 2.41. During the definition of the design parameters of a direct model transition, it is advisable to choose these two dimensions as equal to improve the performance of the system. For 150-20 µm CPW structure, lowest reflection is observed with 20 µm transition length with S_{11} below -15 dB in 1-20 GHz band. For 170-25 µm CPW structure, maximum S_{11} is observed below -18 dB in the complete frequency band. It is also noticeable that for wider CPW signal line, the maximum S_{11} is lower. As the signal line gets wider, the dimension difference between the microstrip line and CPW signal line becomes smaller and the transition is realized in a smoother region. This may explain the reason for the improvement of reflection for wider CPW signal lines.



(a) Reflection analysis for 170-25 µm CPW with different transition lengths



(b) Reflection analysis for 150-20 µm CPW with different transition lengths

Figure 2.41 (a) – (b): Comparison of reflections for various transition lengths for two different CPW structures.

This property can also be used in the staircase transition model. In the studied structures the gap between each step edge and the ground plane is 25 um (Figure 2.13) and this value can be arranged at each step so that this distance is equal to the previous step CPW's signal-ground gap dimension, which may further improve the transition performance.

CHAPTER III

SURFACE MICROMACHINED FILTERS USING SQUARE PLANAR SPIRAL INDUCTORS AND METAL-INSULATOR-METAL CAPACITORS

This chapter explaines the studies on surface micromachined lumped components. Section 3.1 gives an introduction about the topic and Section 3.2 gives the previous research studies on the components. Section 3.3 and Section 3.4 explain the design and fabrication steps of inductors and capacitors respectively. Section 3.5 and Section 3.6 give the low-pass filter and the band-pass filter designed with the lumped circuit components respectively.

3.1. Introduction

In the recent communication era, there are great demands for RF filter structures with smaller size, lighter weight and higher performance for advanced mobile communication systems, especially in receiver-transmitter units. However in highly integrated systems the design of the filters is generally subject to serious size constraints where surface micromachining technology finds itself a great use in minimizing the filter elements.

This study aims to create a micromachined "square spiral inductor library" and a "Metal – Insulator – Metal (MIM) capacitor library" which may be used to supply on chip inductive and capacitive components with various characteristics. Then these designed elements are used as building blocks to construct micromachined band-pass and low-pass filter structures. In order to achieve this goal, square spiral inductors with various dimensions are designed and fabricated with inductances from sub nH to 20 nH. Also MIM capacitors from sub pF to 10 pF are designed and fabricated. Using chosen elements from these libraries, a low-pass filter with cut-off frequency of 2 GHz and a band-pass filter with 2 – 4.6 GHz bass-band are designed and fabricated. EM Simulations are performed with ANSOFT HFSS v9.2^{TM} using FEM techniques and lumped model parameters are obtained by matching the S-parameters of the EM simulation with the S-parameters of the circuit models. The inductance values gathered from the circuit model are then compared with the inductance values calculated using the "modified wheeler" formulations in order to check the validity. The capacitors are initially derived from conventional capacitance formulation and then the simulations are compared with the microwave circuit model of the capacitors in order to extract the capacitance. Finally the fabrication process is performed and the measured data are compared with the simulations.

3.2. Previous Studies on Lumped Components

The spiral inductors are being studied for a long time in the literature, as a result many types of structures are available; however the spiral section remains the same in most works where different approaches for quality factor improvement make each study unique. The first example about simple planar inductors with accurate expressions is presented by [33]. Several new simple and accurate expressions for the DC inductance of square, hexagonal, octangonal and circular spiral inductors are given. The calculated inductances are also compared by the fabrication results. The

inductors are fabricated directly on the substrate without any consideration on quality factor. This, in fact, is the same methodology covered within this thesis. The second example is an air-gap inductor structure using microbump bonding [34]. It is pointed that spiral inductor using air-gap structures have the advantages of low losses, and low parasitic capacitance compared to conventional inductors on doped silicon semiconductor structure. Another approach is present in [35] where a fully-embedded LTCC spiral inductor is proposed by incorporating an air cavity between the spiral and ground plane for high quality factor and high self-resonant frequency. With this application a maximum Q of 51 and SRF of 9.1 GHz are obtained in the measurements. The fourth example is a suspended spiral inductor structure which is sustained with the T shaped pillars [36]. Great improvements in Q-factor are achieved because of the separation between the substrate and the inductor. The last example in this topic is a self-assembling variable inductor which uses warping members to assemble itself away from the substrate to improve the quality factor [37]. It is based on a three dimensional self-assembling structure that uses interlayer stress to bend itself out of the plane on which it is fabricated. The structure separates from the circuit substrate to minimize parasitic losses, and uses thermally controlled inter-member positioning to alter the overall inductance. Q values greater than 13 are demonstrated as well as continuous inductance variations greater than 18%.

For the MIM structures, the analog characteristics and DC RF characteristics of dielectric silicon nitride layer which is also used in this thesis, are investigated in [42] and [43] respectively. The break down field strength of MIM capacitos with 200-Å-thick Si_3N_4 is larger than 3.5 MV/cm and the main capacitance per unit area is extracted as 2900 pF/mm^2 in [43]. Also MIM capacitors include many different dielectric materials as TaTiO [44], High-K Al_2O_3 and $AlTiO_x$ [45]. The next step in MIM capacitors is the tunability contribution. Nickel electroplated widely tunable micromachined capacitor [46] is the first example tunable capacitors which changes the air gap of between the top and bottom metal layers with DC actuation. Another example is presented by [47]. Different from two-parallel-plate tunable capacitors,

this structure consists of one suspended top plate and two fixed bottom plates. One of the two fixed platers and the top plate form a variable capacitor, where as the other fixed plate and top plate are used to provide electrostatic actuation for capacitance tuning. For the fabricated prototype tunable capacitors, it is reportes that a maximum controllable tuning range of 69.8% is achieved. The last example in this topic is investigated in [48]. The structure consists of two parallel electrodes, i.e., fixed and micoing electrodes and six bi-directional electrostatic actuators, which are able to produce both attractive and repulsive force to drive the moving electrode. As a result the capacitor is able to move in both directions, up and down, away from its static position and therefore achieve a large tuning ratio of 3:1 at a driving voltage of 16 volts.

For the micromachined filter structures, the first examples in the literature are the membrane supported low-pass and bandpass filters presented by [49]. The designs are realized in CPW form using short and open end series stubs with integrated MIM capacitors, and are compact in lateral and longitudinal dimensions. S-parameters of a low-pass filter with a cutoff frequency at 17 GHz and a second bandpass at 115 GHz are presented. The same approach is also used in the design of band-pass filters which exhibit 1.5-2 dB insertion loss and bandwidths around 10%. Another example is a cross coupled filter presented by [50]. The cross coupling is realized quarter-wave resonators where the coupling mechanism is realized magnetically from the short ends of the resonator. There are also a lot of studies on tunable micromachined filters, one of which is investigated in [51] in terms of tunable components for reconfigurable filters. In the study, shunt capacitors, series inductors and shunt inductive stubs are the main tunable circuit elements utilized in this work. In [52], miniature and tunable filters using MEMS capacitors are presented. Using CPWs on a quartz substrate, a miniature three-pole wilter is developed with 8.6% bandwidth. The midband insertion loss is observed as 2.9 dB at 21.1 GHz. The pass band of the same type of filter is tuned with MEMS bridges which are used as varactors. Such a tunable filter is formed on a glass substrate.

Over a tuning range from 14% from 18.6 to 21.4 GHz., the miniature tunable filter has a fractional bandwidth of 7.5 and a midband insertion loss of 3.85 to 4.15 dB.

3.3. Spiral Planar Inductors

3.3.1. Basics

The inductor is a dynamic circuit element with a time variation of the magnetic field produced by a current. Any conductor carrying a certain current has a magnetic flux that surrounds itself. The ratio of the total magnetic flux over the current flowing on the conductor at any time is defined as the self inductance L of the conductor [38].

$$L = \frac{\lambda(t)}{i(t)} \tag{3.1}$$

The voltage on the conductor is a function of the inductance and current as

$$V(t) = L\frac{di(t)}{dt} \tag{3.2}$$

When a second conductor is brought close to the first conductor, the flux from the first conductor is coupled to the second conductor. If the current in the first conductor is time dependent, then this flux linkage will induce a voltage on the second conductor. The mutual inductance M is the outcome of this coupling when changing current on one conductor results a change in voltage on the other conductor.

$$v_1(t) = L_1 \frac{di_1(t)}{dt} \pm M \frac{di_2(t)}{dt} \tag{3.3}$$

$$v_2(t) = L_2 \frac{di_2(t)}{dt} \pm M \frac{di_1(t)}{dt} \quad \textbf{(3.4)}$$

The basics of inductor design roots from the natural inductive behaviour of transmission lines. A transmission line itself has a self inductance per unit length since it is excited by varying current at very high frequencies. The idea in spiral inductor theory is to design a structure with transmission lines such that the self inductance and the total positive mutual inductance between the windings of the structure are maximized and the negative mutual inductances between the lines are minimized. To assemble such a geometry, (1) the current flow in the mutually coupled lines shall have the same direction for positive mutual inductance, (2) the transmission lines which have negative direction of current shall be placed as far as possible to diminish the negative inductance, (3) the total line length shall be increased to achieve a sufficient self inductance. These three points are the main parameters to design an inductor with the desired inductance.

Figure 3.1 shows the schematic of a square spiral inductor. It is a microstrip line which is oriented in a spiral fashion on a substrate. The spiral geometry not only increases the total length of the line in a given area to provide higher self inductance, but also enables the same current to flow in the neighboring lines to increase positive mutual inductance and increases the distance between the lines, which have negative current direction with respect to each other, so that the negative mutual inductance is less effective [39].

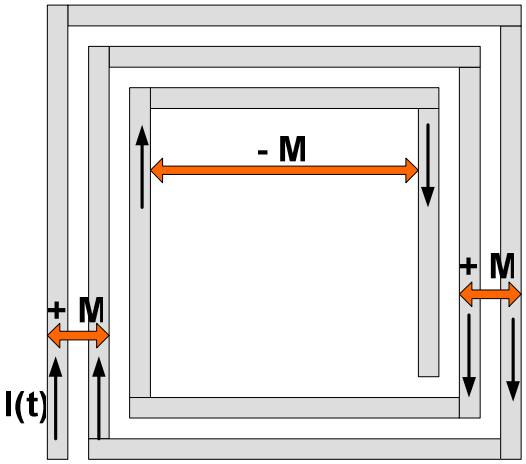


Figure 3.1: Schematic of a spiral inductor and mutual inductances between adjacent conductors.

3.3.2. Modified Wheeler Formultion

For a given geometry, as shown in Figure 3.2, an inductor is completely specified by the number of turns “n” , the turn width “W” , the turn spacing “G” , and any one of the following: the outer diameter “D_{out}” , the inner diameter “D_{in}” , the average diameter “$D_{avg} = 0.5 (D_{out} + D_{in})$”, or the fill ratio, defined as “$\rho = (D_{out} - D_{in}) / (D_{out} + D_{in})$”. The thickness of the inductor has only a very small effect on inductance but it is strictly related with the series resistor that models the ohmic loss thus it dramatically effects the quality factor. The modified wheeler formulation [33] is the simplified version of Wheeler Formulation [40] and it calculates the inductance of a spiral structure using the fill ratio, avarage diameter and number of turns. The coefficients K_1 and K_2 in (2.1) are 2.34 and 2.75 respectively for square spiral inductors. This formulation is also valid for different geometries which have different K_1 and K_2 values.

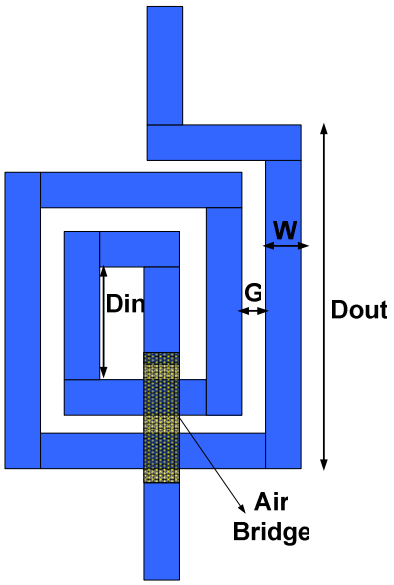


Figure 3.2: A 2-turn square spiral inductor including the air bridge and design parameters.

$$L_{mw} = K_1 \mu_0 \frac{n^2 D_{avg}}{1 + K_2 \rho} \tag{3.5}$$

3.3.3. Lumped and Simplified Lumped Model

Figure 3.3 shows a detailed model that is often used to represent the behaviour of the spiral [33]. Even though the spiral inductor is not symmetrical with respect to the two ports, the equivalent model is assumed to be symmetrical for simplicity. All the components in the model have physical meanings. Ls and Rs represent the series inductance and the resistance of the microstrip inductor. Cs, the parallel capacitor models the capacitive coupling between the windings of the spiral inductor. Cox is the oxidation layer capacitance in the cases where an oxidation layer is used in order

to minimize the substrate losses. The substrate effects are taken into consideration with capacitance and resistance to the substrate as Csub and Rsub.

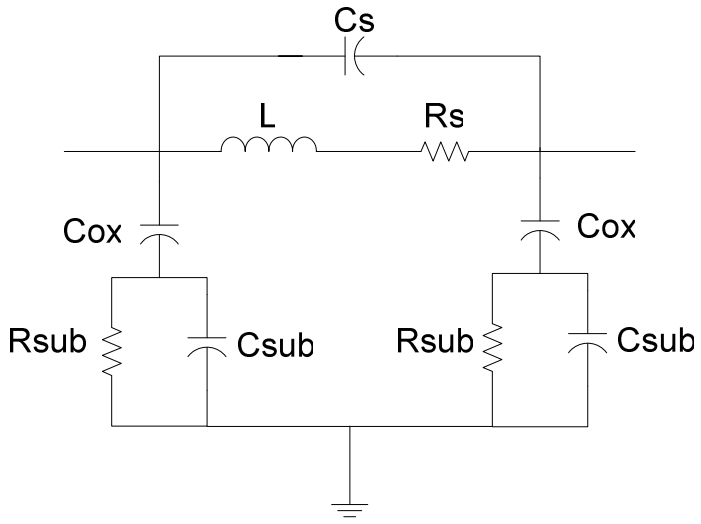


Figure 3.3: Circuit model of a spiral inductor.

The series resistance of the inductor increases with frequency due to skin effect . A first-order model for Rs can be expressed by the following equation [41]:

$$R_s = \frac{\rho l}{w\delta(1-e^{-t/\delta})} \tag{3.6}$$

where δ and ρ denote the skin depth and resistivity of the interconnect material, respectively. Proximity effect between the traces of the spiral can also cause R to increase because of mutually induced eddy current.

In this study, circuit model analysis showed that each shunt branch that models the substrate effects can be simplified to a single capacitor. The resistance of the substrate has a negligible role in the overall scattering matrix of the spirals. The

remaining cascaded capacitors are uniformed into one capacitor to obtain the simplified circuit model of the spiral inductor as shown in Figure 3.4. To obtain the element values, s-parameters from the EM simulations are optimally fit to s-parameters of the simplified lumped model.

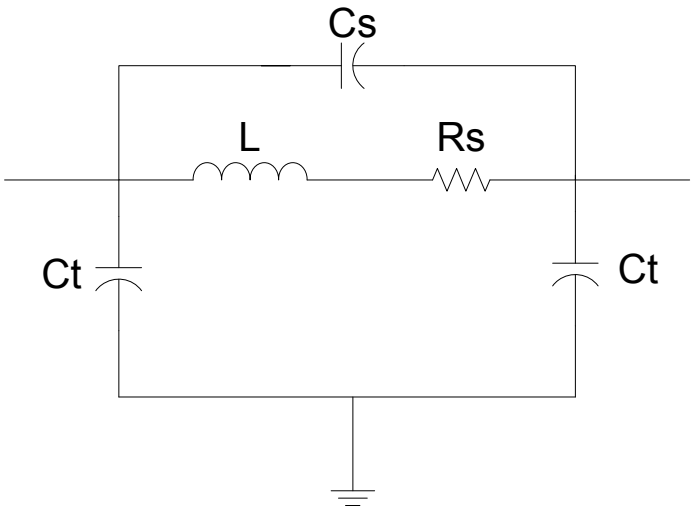


Figure 3.4: Simplified circuit model of a spiral inductor

3.3.4. Design Procedure

The design strategy for spiral inductors has several steps. Initally modified wheeler formulation is used to calculate the number of turns and average diameter of the spiral for a desired inductance value. When data on these two parameters are gathered, width, gap and the outer dimension of the spiral are calculated. There are infinite solutions to this problem and the dimensions that are consistent with process capabilities are chosen. When the spiral dimensions are decided, EM simulations of the spiral are done and s-parameter characteristics are obtained. After this step s-parameters of the simplified lumped model are matched with the s-parameters of the

simulated structure with optimization tools. Next step is to acquire the lumped element values including the inductance of the spiral structure. Finally, the extracted inductance is compared to the initially desired inductance value to check the validity of the design procedure.

3.3.5. EM Simulation Results

The simulations of the designed structures are done using ANSOFT HFSS v9.2™ which uses the conventional Finite Element Method (FEM). The dimensions and materials of the substrate and metal thickness are chosen in order to match with the process conventions. The substrate is 4" thick Pyrex 7740 (ε_r = 4.6) and the base metal including the air bridge is gold (conductivity = 41000000 S/m). The input and output ports of the device are microstrip lines whose width dimensions are the same as that of the width of the spiral section. The simulations are performed with the actual port impedances of the microstrip ends but the results are extracted with standard 50 Ω characteristic port impedance. However the fabricated devices have coplanar waveguide (CPW) ports in order to be measured with network analyzer. The dimensions of the CPW are chosen as 15 µm-150 µm -15 µm (ground-signal-ground) having a 50 Ω characteristic impedance. To avoid port impedance mismatch, the port impedances of the circuit model are also set to 50 Ω.

The width of the microstrip turns (W), the gap between the turns (G), the outermost dimension (Dout), and the number of turns in the spiral (N) are the sufficient parameters to define a unique square spiral inductor as seen in Figure 3.2. The signal at the end of the final turn of the spiral is conducted with an air bridge in order to be able to get the signal out of the the spiral loop. The air bridge height is set to 2 µm and the effect of the inductance of this segment is present in the simulation as it was neglected in the modified wheeler formulation.

Table 3.1 gives the list of inductors that have been designed to create the inductor library. The minimum feature size is determined to be 5 µm so that all the features of the structures are fabricated successfully. Maximum Dout is chosen to be 500 µm to assure a compact size for the inductors.

The inductor has extra inductive components which are the input-output microstrip lines and the air bridge section where the contribution from the latter can be ignored. The input and output microstrip lengths are chosen to be equal to Dout.

Table 3.1: Design parameters of the inductor library

Inductor Name	N	W (µm)	G (µm)	D out (µm)
i1	4	20	5	300
i2	4	10	5	300
i3	4	5	5	300
i4	4	30	5	400
i5	4	10	10	400
i6	4	10	5	200
i7	4	5	10	200
i8	4	20	20	500
i9	4	5	5	500
i10	4	20	30	500
i11	3	20	5	300
i12	3	10	5	300
i13	3	5	5	300
i14	3	30	5	400
i15	3	10	10	400
i16	3	10	5	200
i17	3	5	10	200
i18	3	20	20	500
i19	3	5	5	500
i20	3	20	30	500
i21	2	20	5	300

Table 3.1 cont'd.

Inductor Name	N	W (µm)	G (µm)	D out (µm)
i22	2	10	5	300
i23	2	5	5	300
i24	2	30	5	400
i25	2	10	10	400
i26	2	10	5	200
i27	2	5	10	200
i28	2	20	20	500
i29	2	5	5	500
i30	2	20	30	500
i31	1	20	5	300
i32	1	10	5	300
i33	1	5	5	300
i34	1	30	5	400
i35	1	10	10	400
i36	1	10	5	200
i37	1	5	10	200
i38	1	20	20	500
i39	1	5	5	500
i40	1	20	30	500
i41	1	80	10	500
i42	1	50	5	300
i43	1	55	20	400

The simulations are performed in 1 - 20 GHz frequency range for inductances more than 3 nH and 1 - 30 GHz range for inductances below 3 nH in order to see the dips in S_{21} plots which is important while matching the circuit response with the simulation. The reason for the dips in the S_{21} plots is the LC shunt branch of the lumped model. At low frequencies, the input impedance of the inductive branch is low and the overall characteristic is inductive. However after a certain frequency,

the capacitive branch starts to have a lower input impedance and the overall circuit behaviour becomes capacitive. The critical frequency where the dip occurs is the self resonant frequency (SRF). An inductor behaves ideally when its working frequency is well below the self resonant frequency. As its working frequency increases, the effects of the parasitic capacitance become more pronounced until its self-resonant frequency, when the effective inductance is zero since it is canceled by its counterpart. Therefore it is safer to assume the spiral structure as an inductor only at low frequencies far away from the frequency where the dip is located.

As explained in the "Design Procedure" section, the s-parameters of the simulated spiral structures are fit with the lumped equivalent model and the each lumped element is extracted. Table 3.2 contains the element values of the simplified circuit model including the calculated and the simulated inductance values.

Table 3.2: Element values of the simplified circuit model of the inductors.

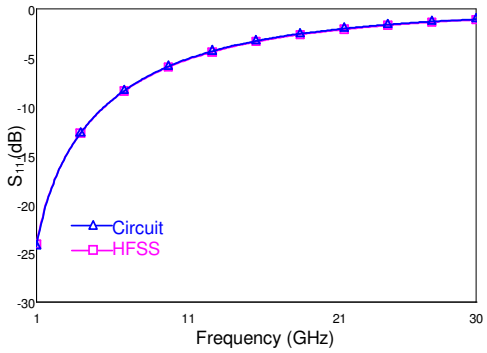
Inductor name	Ct (pF)	Cs (pF)	L (nH)	Rs (Ω)	L (nH) Wheeler
i1	0.0235	0.0186	4.279	3.409	4.0093
i2	0.0218	0.0164	7.415	3.527	6.9059
i3	0.0134	0.0176	9.301	2.533	8.8666
i4	0.0277	0.0315	5.279	2.67	5.0604
i5	0.0277	0.0171	10.16	4.44	9.3541
i6	Fit error	Fit error	Fit error	Fit error	3.1779
i7	Fit error	Fit error	Fit error	Fit error	3.3390
i8	0.0281	0.01746	9.06	5.97	7.5584
i9	0.0277	0.03046	20.9	20.68	17.7921
i10	0.0277	0.01283	6.6	2.34	5.6671
i11	0.0289	0.01926	3.78	3.2	3.2086
i12	0.0277	0.01746	5.3	4.4	4.6871
i13	0.0253	0.01706	6.37	3.3	5.6449
i14	0.0265	0.03046	4.76	4.48	4.0427
i15	0.0337	0.01713	7.71	3.48	6.3474

Table 3.2 cont'd.

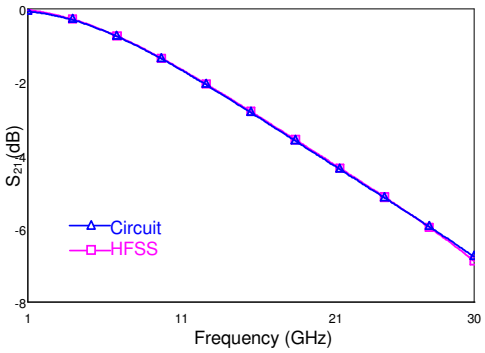
Inductor name	Ct (pF)	Cs (pF)	L (nH)	Rs (Ω)	L (nH) Wheeler
i16	Fit error	Fit error	Fit error	Fit error	2.3926
i17	Fit error	Fit error	Fit error	Fit error	2.5092
i18	0.0257	0.01833	6.61	3.98	5.8125
i19	0.01185	0.03273	12.92	6.68	10.7790
i20	0.0377	0.01316	6	3.23	4.7887
i21	Fit error	Fit error	Fit error	Fit error	1.9573
i22	Fit error	Fit error	Fit error	Fit error	2.5088
i23	0.01535	0.0151	3.53	2.9	2.8391
i24	0.01695	0.0305	3.01	2.1	2.5097
i25	0.01555	0.0161	4.19	2.130	3.3972
i26	Fit error	Fit error	Fit error	Fit error	1.4105
i27	Fit error	Fit error	Fit error	Fit error	1.4778
i28	0.01655	0.0155	4.45	1.16	3.4936
i29	0.01715	0.0299	7.29	4.82	5.1604
i30	Fit error	Fit error	Fit error	Fit error	3.1224
i31	0.01715	0.0043	1.38	0.44	0.6672
i32	0.01175	0.00102	1.6	1.08	0.7551
i33	Fit error	Fit error	Fit error	Fit error	0.8034
i34	0.02665	0.000528	1.64	0.7675	0.8692
i35	0.02235	0.00028	2.04	1.245	1.0225
i36	0.01298	0.000262	1.12	1.035	0.4659
i37	0.01048	0.000325	1.25	1.345	0.4880
i38	0.00748	0.000281	1.23	1.625	1.1756
i39	0.02606	0.000309	2.35	0.96	1.3900
i40	0.03506	0.0008775	2.31	0.52	1.1328
i41	0.03583	0.03942	1.09	0.194	0.7806
i42	0.02263	0.01551	0.7	0.1	0.4596
i43	0.03013	0.01611	0.98	0.1	0.6423

EM simulation results and circuit simulation results of some of the elements in the table cannot fit most probably due to a simulator error and they are marked as "Fit error". Also there is a slight difference between simulated and calculated values.

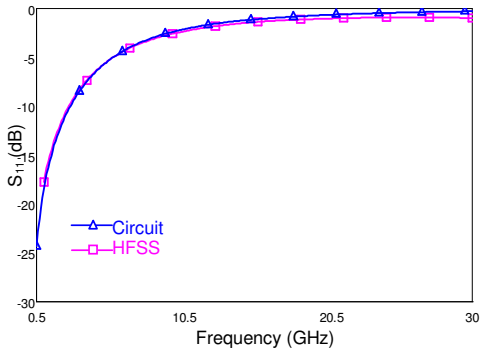
The simulated inductances are higher than the calculated ones. The reasons for this may be the following: (1) The modified wheeler formulation is not 100% accurate. (2) The lumped model and the modified Wheeler formulation takes only the spiral section into account. However the complete inductor structure consists of input and output microstrip lines and air bridge in addition to the spiral section. All these extra features increases the overall inductance of the structure. As observed in Table 3.2, the percentage error in inductances are smaller in cases where inductance is high since the extra inductance addition ratio to the spiral section becomes smaller. Figure 3.5, Figure 3.6, and Figure 3.7 shows the S_{11} and S_{21} characteristics of various simulated square spirals.



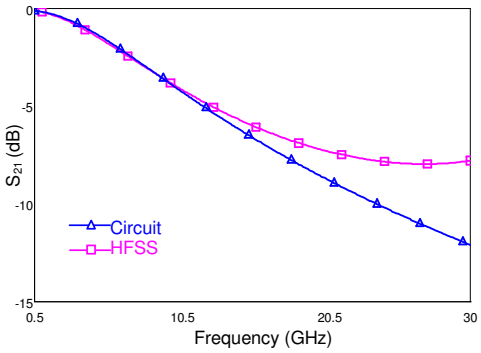
(a) S_{11} comparison for L = 0.7 nH



(b) S_{21} comparison for L = 0.7 nH

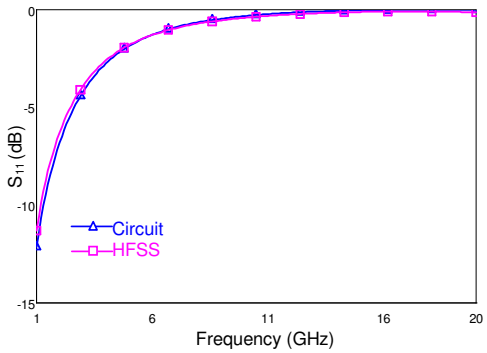


(c) S_{11} comparison for L = 2.04 nH

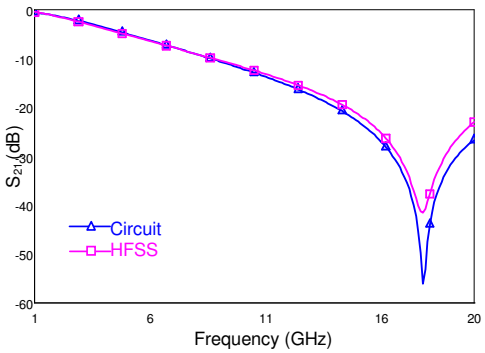


(d) S_{21} comparison for L = 2.04 nH

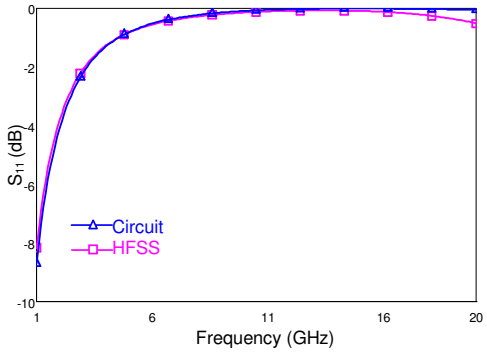
Figure 3.5 (a) – (d): Comparison of S-parameters extracted from EM simulations and circuit responses of 0.7 nH and 2.04 nH spiral inductors from the library.



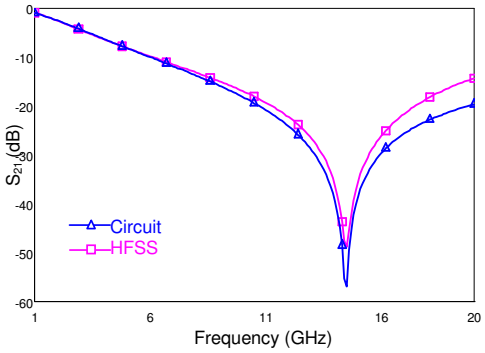
(a) S_{11} comparison for L = 4.27 nH



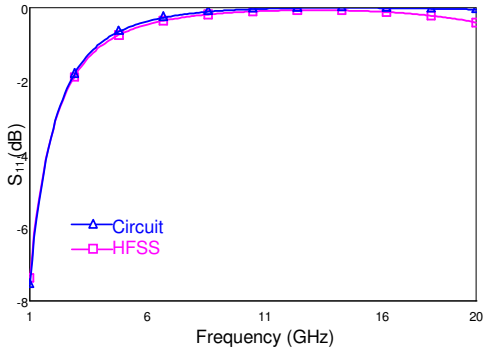
(b) S_{21} comparison for L = 4.27 nH



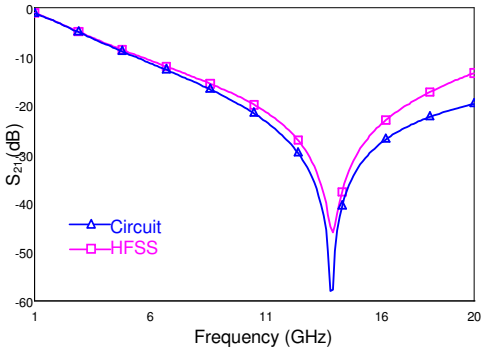
(c) S_{11} comparison for L = 6.61 nH



(d) S_{21} comparison for L = 6.61 nH

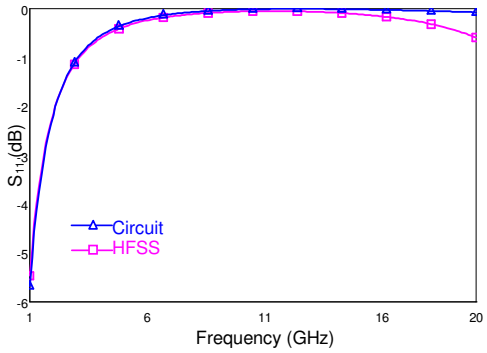


(e) S_{11} comparison for L = 7.71 nH

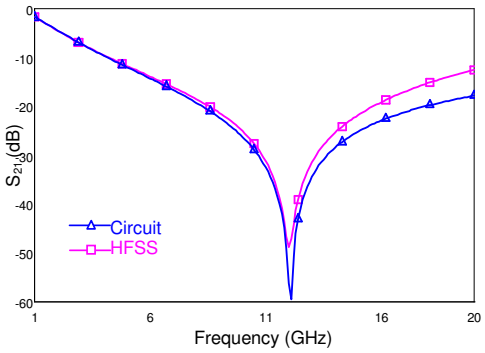


(f) S_{21} comparison for L = 7.71 nH

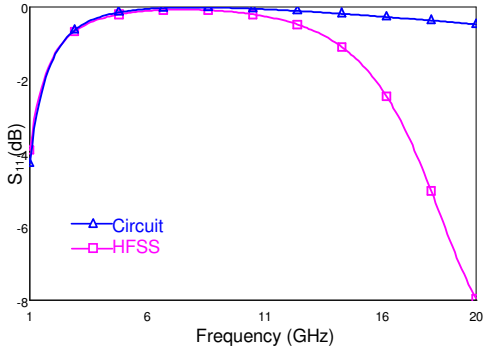
Figure 3.6 (a) – (f): Comparison of S-parameters extracted from EM simulations and circuit responses of 4.27 nH, 6.61 nH, and 7.71 nH spiral inductors from the library.



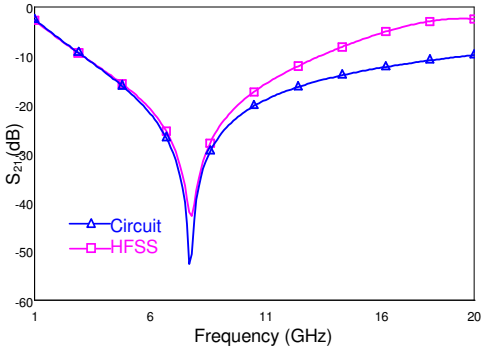
(a) S_{11} comparison for L = 10.16 nH



(b) S_{21} comparison for L = 10.16 nH



(c) S_{11} comparison for L = 12.92 nH



(d) S_{21} comparison for L = 12.92 nH

Figure 3.7 (a) – (d): Comparison of S-parameters extracted from EM simulations and circuit responses of 10.16 nH and 12.92 nH spiral inductors from the library.

The dips in S_{21} plots move to lower frequencies when the inductance is increased. This shows that the maximum frequency when a spiral acts as an inductor decreases as the inductance increases. In other words SRF is lower when the inductance is increased. In addition to this general trend, it is observed that for inductors with similar inductances, the SRF is also dependent on the geometry of the spiral. Figure 3.8 shows the insertion loss for similar inductances.

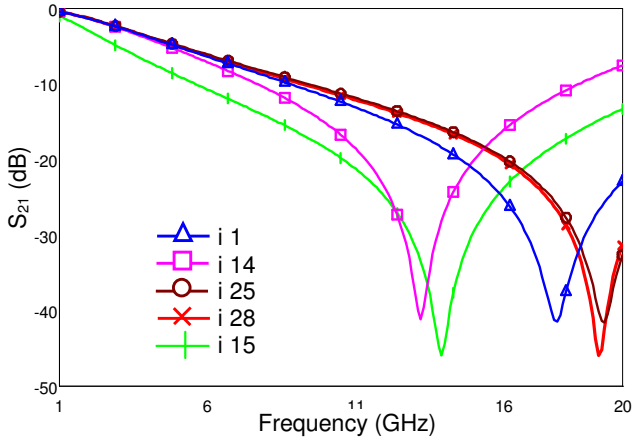


Figure 3.8: SRF investigation for inductors with similar inductances.

The SRF of i14 (L=4.76 nH) is way lower than i1 (L = 4.28 nH), i25 (L = 4.19 nH), i28 (L = 4.45 nH), and even i15 (L = 7.71 nH). The main difference between these structures is the W/G ratio. For W/G= 1, i.e. for i14, i28, the SRF is obtained as maximum, however for increasing W/G ratio, the SRF becomes smaller as the ratio is 4 for ind1 and 6 for ind14.

3.3.6. Fabrication Process

A new set of mask have been designed and produced for the fabrication process. The mask includes inductor, capacitor and filter blocks which are explained in this study. The mask preparation procedure is previously explained in transition mask layout, however in this case four different masks are required to define the structures completely. The first mask to be used is the first metallization mask to define the base metal regions of the structures. The second mask is the “Silicon Nitride” mask which defines the dielectric layers used in Metal-Insulator-Metal capacitors. The third mask is the polyimide sacrificial layer anchor etch mask which defines the air bridge anchors of the inductors and the top plate regions over the dielectric layer of the MIM capacitors. The fourth and the final mask is the second metallization mask

which patterns the air bridges of the inductors and top metal plates of the capacitors. Filter structures are composed of capacitors and inductors so these four masks automatically define the filter layers.

The mask set is drawn using CADENCE and minimum feature size is 2 µm in all masks.

Figure 3.9 shows the mask layout and zoomed areas where inductors, capacitors and filters are located.

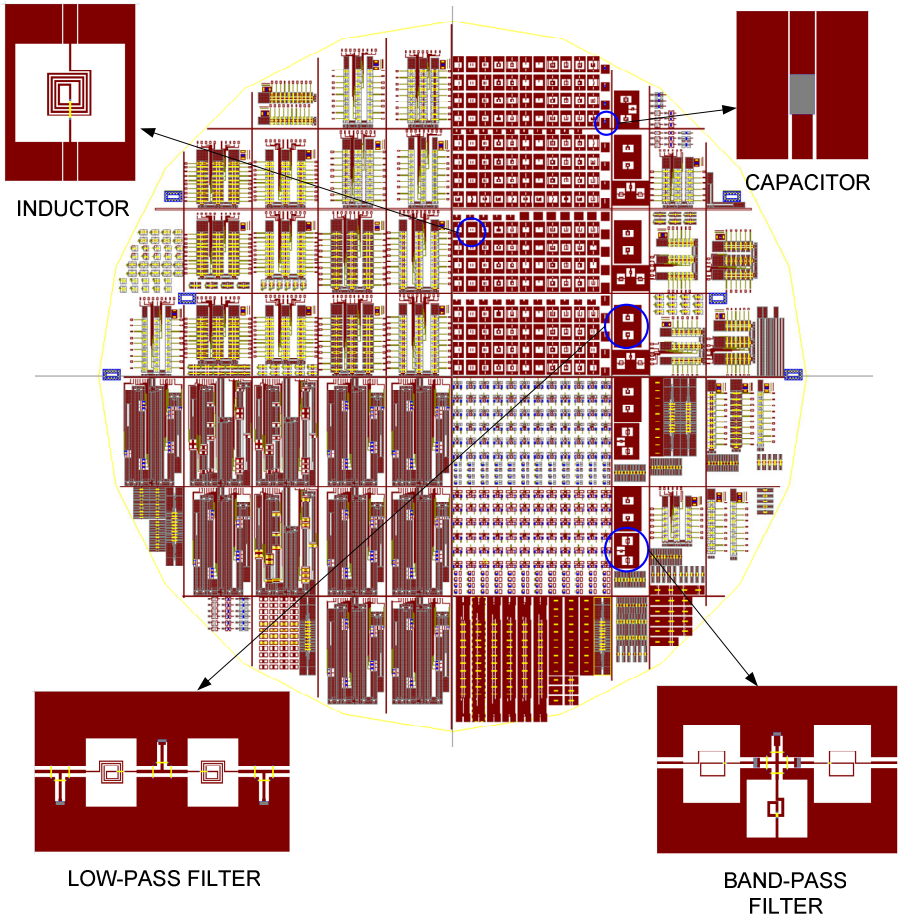


Figure 3.9: Mask layout that consists the inductor, capacitor libraries and low-pass and band-pass structures included in this study.

3.3.6.1. Sacrificial Layer Deposition Stage

In the fabrication process, the first metallization and backside metallization stages are exactly the same as the fabrication of previously explained CPW-microstrip transitions. So these stages are omitted in this part and the process flow begins with the sacrificial layer diposition stage. It is also important to notice that the dielectric deposition stage, which is before the sacrificial layer diposition stage, is skipped in this part since inductor structures do not contain insulators however in capacitor fabrication process this stage will be explained. Figure 3.10 shows an inductor structure which only has the first metallization layers.

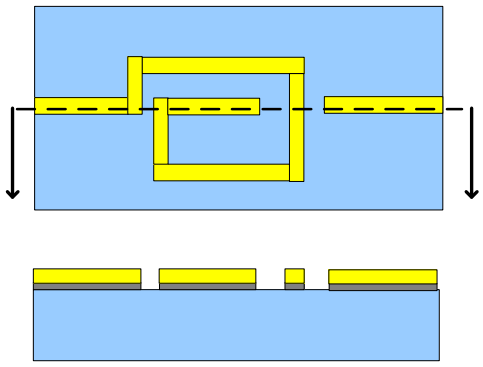


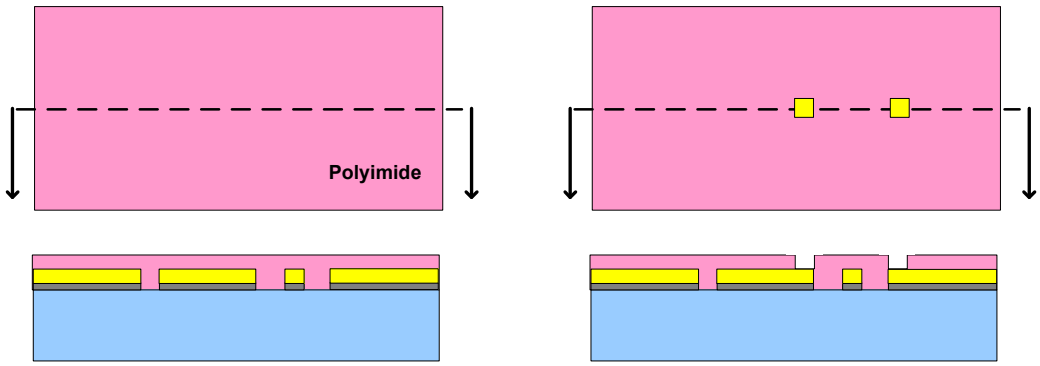
Figure 3.10: The first metallization of the spiral.

Sacrificial layer is a temporary layer that is sacrificed at the end of the process stages in order to obtain suspended bridges. The second metal is built on the sacrificial layer and it is connected to first metal via anchor areas which are defined using anchor etch mask. The sacrificial layer is polyimide (PI2737). This is a chemical which is resistant to both gold and titanium etchants and photosensitive which means that no extra photoresist is necessary in lithography stage. The PI is spinned on the wafer with spinner and exposed to UV rays in the mask aligner. The thickness of the sacrifical layer is optimized to 2 µm using the lithography recipe given in

Table 3.3. Figure 3.11 shows the schematics of polyimide coated and patterned structures.

Table 3.3: Process recipe for Polyimide coating and development

Lithography for Sacrificial Layer using Polyimide (PI2737)	
Dehydration	120 C° 20 min in oven
Spin **PI 2737**	@ 500 rpm dispense (5 secs acceleration from 0 rpm-15 secs duration- 20 secs acceleration to 3000 rpm) @3000 rpm spin (30 secs duration-10 secs deceleration to 500 rpm) @ 500 rpm final speed (5 secs duration-1 secs deceleration to 0 rpm)
Softbake	75 C° on hotplate for 8 min (+30 secs hold the wafer close to the plate)
Exposure	18 secs @ 18 mW/cm^2
Development	2:45 min development 30 secs rinse (DE9040 developer – PA 401R rinser)
O_2 plasma	2 min duration Plasma power: 300 W Plasma pressure: 0.25-0.3 Torr
Hardbake	55°C to 150°C ramp with 4°/min + 30 min @ 200°C



(a) Polyimide coating **(b)** Polyimide patterning

Figure 3.11 (a) – (b): Polyimide lithography for anchor etching.

3.3.6.2. Structural (Second) Metallization Stage

The next step after defining the anchor areas in the sacrificial layer is to construct the structural gold on top of the sacrificial layer with sputter. When the gold is deposited, it is patterned with S1828 photoresist to determine the structural metallization of the air bridges. The areas shaded under the photoresist patterns are protected and rest of the structural gold is removed in the gold etching process. At this step, the polyimide layer protects the base gold during the etching of the structural gold. Table 3.4, Table 3.5, and Table 3.6 shows the sputtering, lithography and etching recipes respectively and Figure 3.12 step-by-step explains the process steps.

Table 3.4: Process recipe for Au structural metal deposition

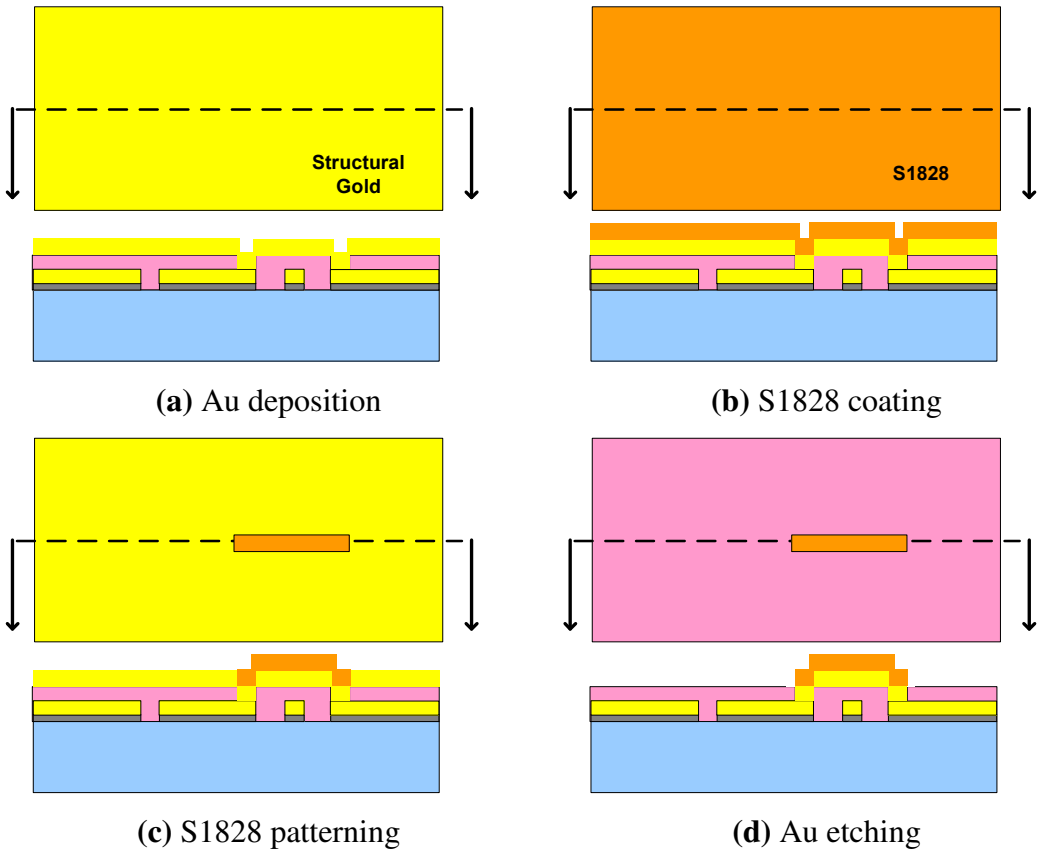
Sputtering for structural layer – Au	
Power – Current	214 W
Current	0.5 A
Temperature	Room temp
Pressure	10e-3 mBar
Flow	mBar
Endpoint	4000A
Rate	4.9 Å /sec

Table 3.5: Process recipe for S1828 structural metal lithography

Lithography using S1828	
Dehydration	120 C° 10 min in oven
Primer HDMS	@ 500 rpm dispense (5 secs acceleration from 0 rpm-7 secs duration- 3 secs acceleration to 3000 rpm) @2000 rpm spin (30 secs duration-3secs deceleration to 500 rpm) @ 500 rpm final speed (10 secs duration-3 secs deceleration to 0 rpm)
Spin **S 1828**	@ 500 rpm dispense (5 secs acceleration from 0 rpm-10 secs duration- 5 secs acceleration to 3750 rpm) @3750 rpm spin (30 secs duration-3 secs deceleration to 500 rpm) @ 500 rpm final speed (10 secs duration-3 secs deceleration to 0 rpm)
Softbake	115 C° on hotplate for 3:30 min (+30 secs hold the wafer close to the plate)
Exposure	16 secs @ 18 mW/cm^2
Development	1:45 min development in MF26 A solution
O_2 plasma	2 min duration Plasma power: 300 W Plasma pressure: 0.25-0.3 Torr
Hardbake	120°C 20 min in oven

Table 3.6: Process recipe for Au structural metal deposition

Au Etch for First Metallization	
Au etch	Transene Au etchant 1:50 min



(a) Au deposition **(b)** S1828 coating

(c) S1828 patterning **(d)** Au etching

Figure 3.12: Second metallization steps including Au deposition, lithography and etching.

3.3.6.3. Release Stage

This is the final stage of the full wafer process where the sacrifical layer and the photoresist are removed from the surface of the wafer. The wafer is left in SVC solution at 80°C for at least 12 hours so that no residues are left under the suspended structures. The wafer is rinsed with DIW after release and put into alcohol to prepare for the criticial point dryer (CPD). CPD is a device which uses the immediate vaporization property of liquid CO_2 at a certain pressure and temperature which is namely the critical point. This step assures that the bridges remain suspended as the liquid CO_2 vaporizes instantly over and under the suspended bridges. Figure 3.13 shows the view of a released inductor.

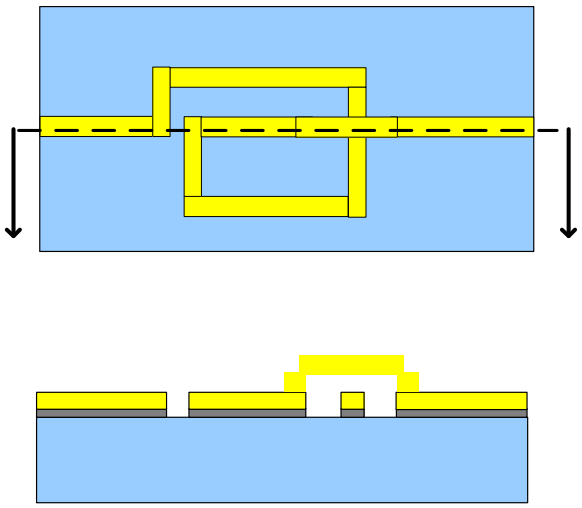


Figure 3.13: Released spiral inductor with air-bridge.

3.3.7. Measurement Results

Using the proposed fabrication steps, the inductive spirals are fabricated in METU-MET Facilities with 0.3 µm first metal thickness. Table 3.7 gives the element values gathered from the measured characteristics. Since the metallization thickness is much smaller than the simulated thickness, the capacitive coupling between each winding is diminished and the ohmic conductor loss is increased. Also the spiral structures are fabricated as CPW ended in order to realize on wafer measurements with air coplanar probes. In the evaluation phase these additional lines are de-embedded from the measurement results. The "measured" values in Table 3.7 refer to the de-embedded results; i.e., the tabulated values are for the naked inductor. However, the effects of CPW-microstrip transition are not compensated which might partially be the cause of the discrepancies. Also, it is observed that the measured inductance values fit better to the simulated ones especially for the cases where number of turns are large, i.e. more than 2, and the spiral width is comparably

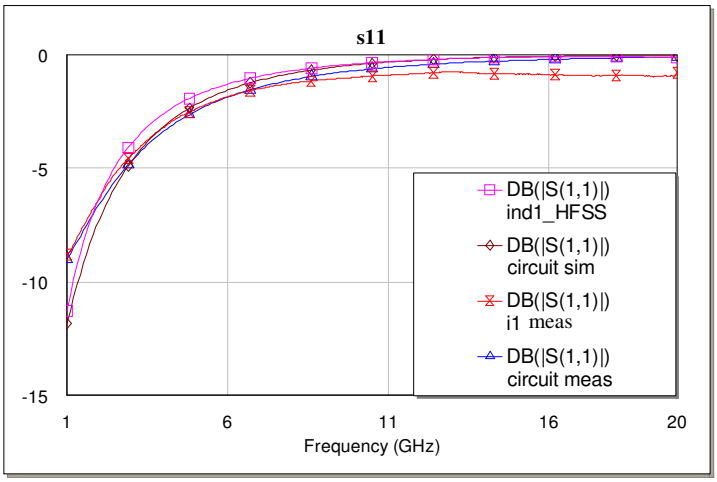
narrow, i.e. less than 30 µm. The deviation becomes more for structures where the number of turns get smaller and the spiral width gets larger.

Table 3.7: Element values extracted from the measurement characteristics.

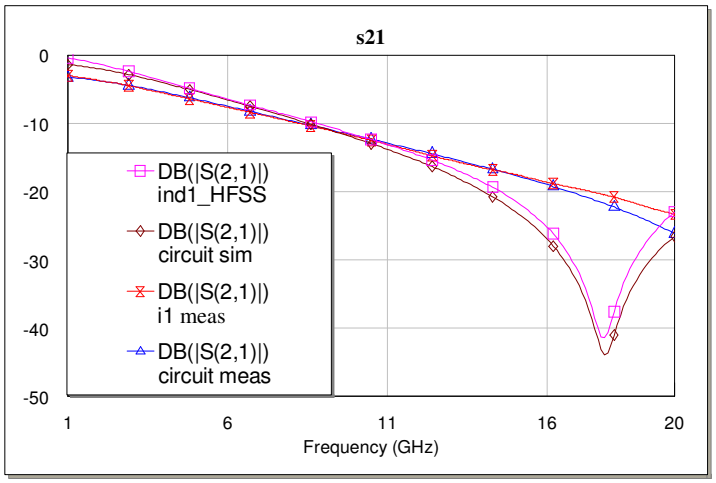
Inductor	Ct (pF) meas.	Cs (pF) meas.	Rs (Ω) meas.	L (nH) meas.	L (nH) sim.	L (nH) calc.
i1	0.0235	0.0093	42.81	4.339	4.279	4.0093
i4	0.0277	0.0191	52.51	5.839	5.279	5.0604
i8	0.0281	0.0087	71.11	8.799	9.060	7.5584
i10	0.0277	0.0057	51.81	6.799	6.600	5.6671
i11	0.0289	0.0087	40.05	3.699	3.780	3.2086
i14	0.0265	0.0152	31.05	4.909	4.760	4.0427
i18	0.0257	0.0076	58.25	6.799	6.610	5.8125
i20	0.0377	0.008	51.05	5.999	6.000	4.7887
i24	0.01695	0.00989	28.65	3.359	3.010	2.5097
i28	0.01655	0.00767	50.65	4.709	4.450	3.4936
i31	0.01715	0.00467	22.175	1.290	1.380	0.6672
i34	0.02665	0.00376	20.08	1.790	1.640	0.8692
i38	0.00748	0.00316	31.78	2.034	1.230	1.1756
i40	0.03506	0.00488	31.18	2.544	2.310	1.1328
i41	0.03583	0.00558	16.09	1.434	1.090	0.7806
i42	0.02263	0.00494	10.89	1.119	0.700	0.4596
i43	0.03013	0.00298	13.59	1.334	0.980	0.6423

The SRF of each structre moves to higher frequencies as winding capacitance is smaller so the inductive behaviour is spread in a wider frequency band. However this also brings a higher ohmic loss and lower quality factor for each inductive

spiral. Figure 3.14 shows the measurement results for i1 and Figure 3.15 shows the pictures of one of the fabricated spirals.

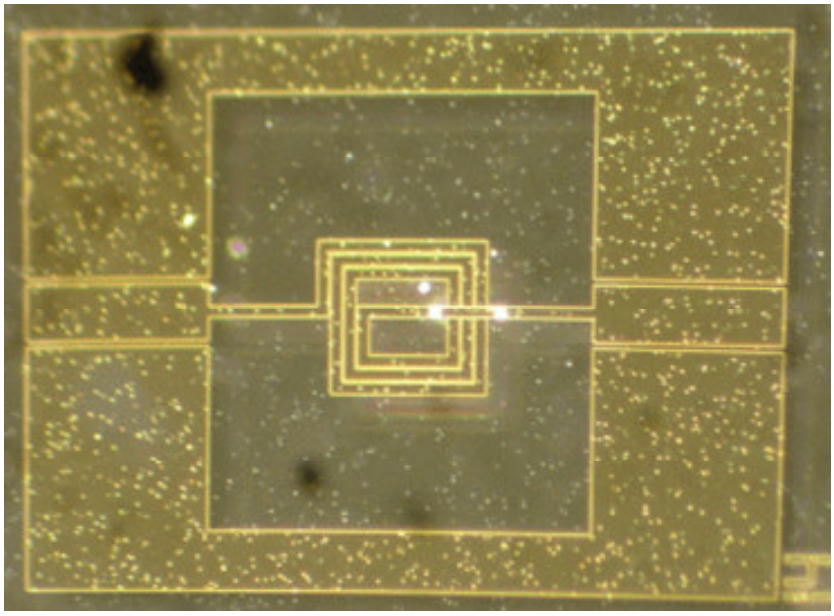


(a) Measured and simulated S_{11} characteristics.

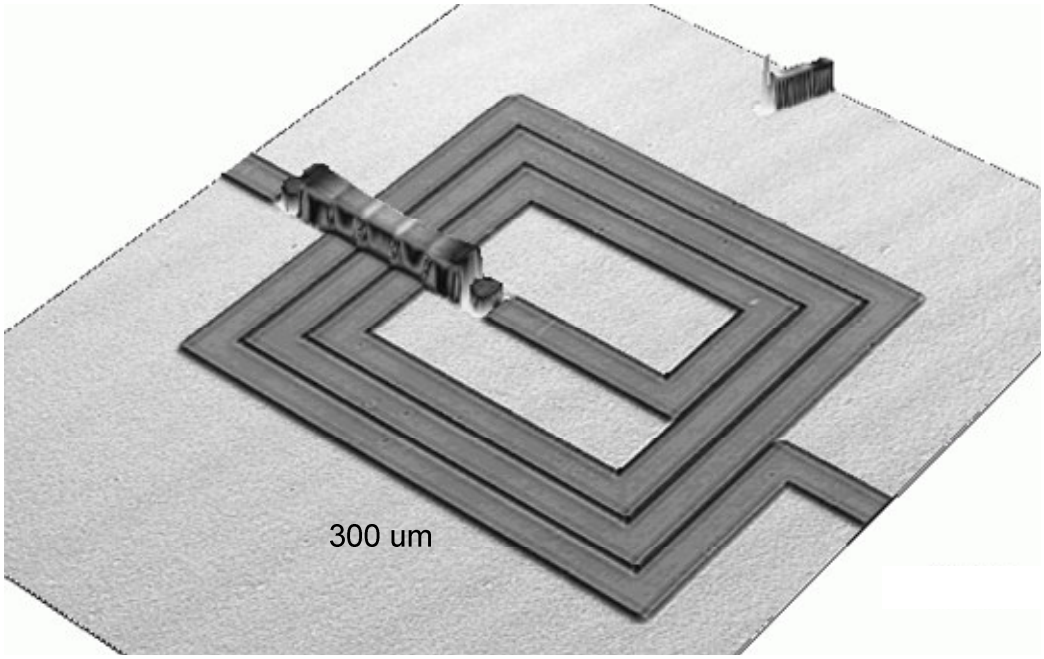


(b) Measured and simulated S_{21} characteristics.

Figure 3.14 (a) – (b): Measurement results for i1.



(a) Microscope shot of a spiral inductor.



(b) Surface profiler view of a spiral inductor.

Figure 3.15 (a) – (b): Pictures of a fabricated spiral inductor.

3.4. Metal-Insulator-Metal Capacitors

3.4.1. Capacitance and Capacitor

Two conductors that can store equal charges ($\pm$Q) without being affected by the other conductors in the system form a capacitor [53]. One of the conductors of a capacitor is shielded by the other conductor, meaning that the potential contributed to each of the conductors by the external forces must be the same. Figure 3.16 shows a system where conductors 1 and 2 form a device of this type.

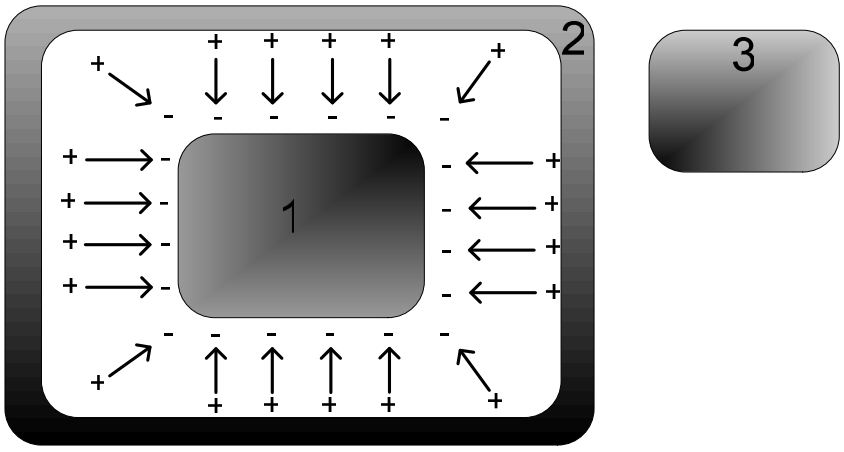


Figure 3.16: Capacitor structure constructed by conductors 1 and 2.

The potentials on each individual can be expressed as

$$V_1 = p_{11}Q + p_{12}(-Q) + V_x \quad \textbf{(3.7)}$$

$$V_2 = p_{12}Q + p_{22}(-Q) + V_x \quad \textbf{(3.8)}$$

where $\pm Q$ are the stored charges, V_x is the common potential contributed by other external charges, i.e. conductor 3, and p_{ij} is the potential of the *i*th conductor due to a unit charge on conductor *j* as

$$V_i = \sum_{j=1}^{N} p_{ij} Q_j \,. \tag{3.9}$$

When we subtract (3.8) from (3.7), we get

$$\Delta V = V_1 - V_2 = (p_{11} + p_{11} - 2p_{12})Q \,. \tag{3.10}$$

It is clear that the difference in potential between the conductors of a capacitor is proportional to the charge stored. It is important to remember that the total charged stored is zero but the absolute value of the charge on one of the conductors is called the charge on the capacitor. (3.10) can be written as

$$Q = C\Delta V \tag{3.11}$$

"$C = (p_{11} + p_{11} - 2p_{12})^{-1}$" is called the capacitance of the capacitor. C is the charge stored per unit of potential difference and is measured in farads, coulombs/volt.

If the geometrical arrangement of the two conductors is simple, the capacitance can be calculated analytically. In this study parallel plate capacitors are designed and fabricated so the derivation of this kind of capacitors is given.

Figure 3.17 is the schematic of a parallel plate capacitor with electric field lines. Neglecting the fringing field at the edge of the parallel plates, the rest of the electric field is uniform between the conductor plates. This is realizable when the separation "d" between the plates is very small compared to the dimensions of the plate which minimizes the fringing field.

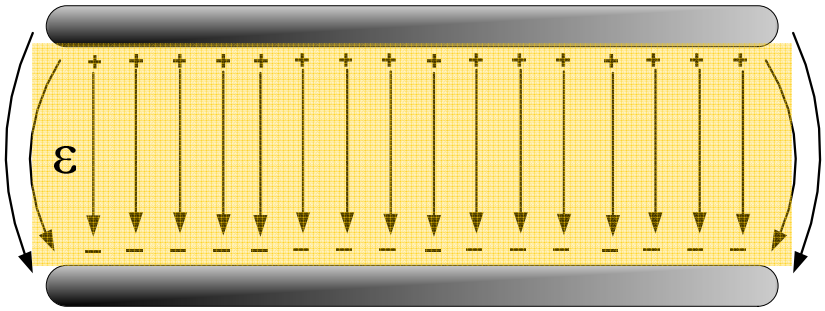


Figure 3.17: Parallel plate capacitor.

If the region between the plates is filled with a dielectric of permittivity ε, then the electric field in the region is

$$E = \frac{1}{\varepsilon}\sigma = \frac{Q}{\varepsilon A} \tag{3.12}$$

Here, A is the area of one plate. The potential difference becomes

$$\Delta V = Ed = \frac{Qd}{\varepsilon A}. \tag{3.13}$$

Using (3.13), the capacitance of the structure is calculated as

$$C = \frac{Q}{\Delta V} = \frac{\varepsilon A}{d} \tag{3.14}$$

3.4.2. Capacitor Lumped Model

Figure 3.18 shows the circuit model of a capacitor operationg at microwave frequencies [27]. Each element has a physical meaning and the L1 and L2 lines are added to the core model in order to obtain more exact capacitance values for the topology which is discussed in the "EM Simulations" section. C represents the

capacitance that is purely due to paralel plate effect without the fringing fields. Cp represents the parasitics due to fringing fields that occur at the both ends of the plates. Ls is total the self inductances of the both plates and Rs represents the ohmic conductor loss. Rp accounts for the dielectric loss in the capacitive region.

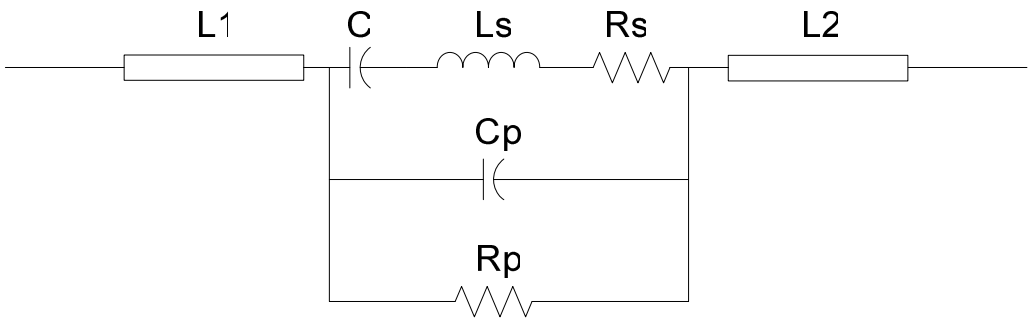


Figure 3.18: Capacitor circuit model.

3.4.3. Design Procedure

A Metal-Inductor-Metal capacitor library is created which is used a constructing tool for the filter structures. Initially the desired capacitance values for a certain capacitor topology are calculated using the paralel plate capacitance formulation (3.14). Then the EM simulations of the capacitors are performed and the s-parameter characteristics of the EM simulations are matched with the s-parameters of the circuit models by optimization. At this point, all the element values of the circuit model are extracted and the capacitance values are compared to the initially desired capacitances to check the validity of the design method.

3.4.4. EM Simulation Results

The simulations of the designed structures were done using ANSOFT HFSS v9.2™ . The dimensions and materials of the substrate and metal layers are same as the inductor since the devices are fabricated on the same wafer, consequently both inductors and capacitors have the same metallization conditions. The devices are CPW ended on both ports with "$g + s + g = 220\mu m$" in order to be measured with air coplanar probes of the same "$g + s + g$" value.

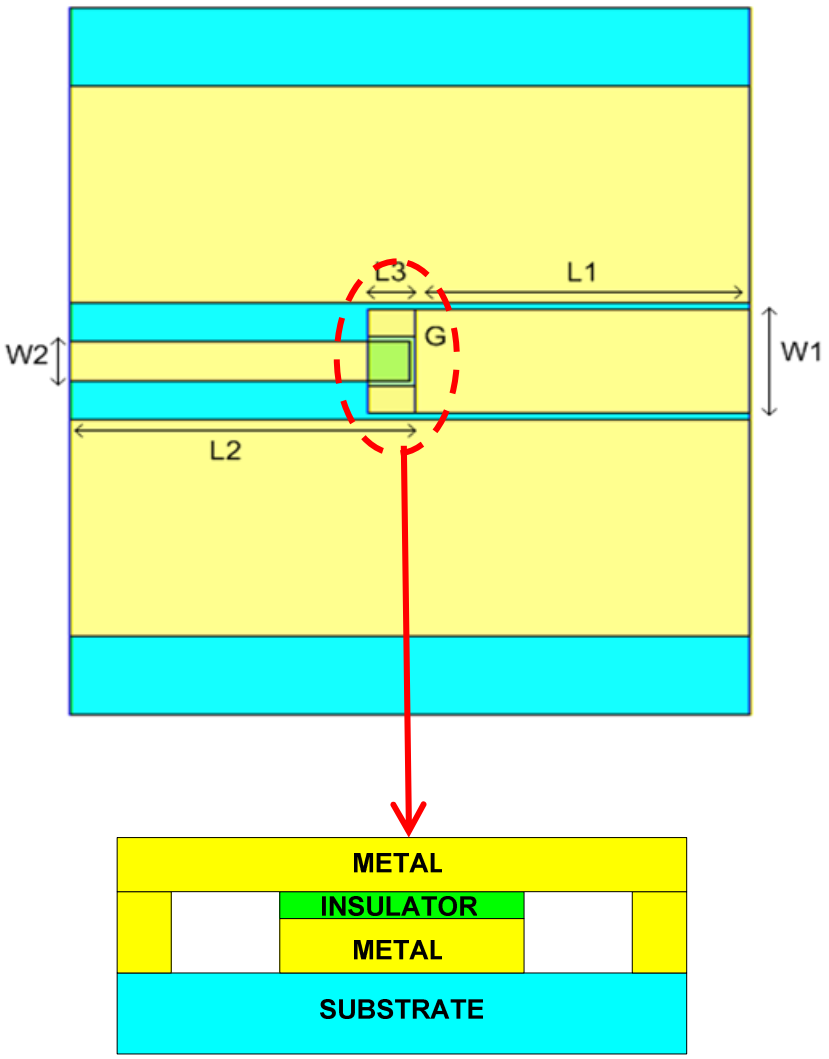


Figure 3.19: Schematic view of a MIM capacitor.

Figure 3.19 shows a top-view of a capacitor model including the input-output CPW sctions and the close-view of the paralel plate region. The ground-signal-ground dimensions of the CPW sections are defined such that the capacitive region has a desired area for the desired capacitance. "W1" dimension is taken as large as possible so that only the capacitance defining parameters are "W2" and "L3", i.e. the area of the plates. The distance parameter in the parallel plate capacitance formulation is set to be constant at 0.3 μm and the dielectric medium between the plates is silicon nitride with $\varepsilon_r = 7$ as this is an optimized and conventional recipe used in METUMET cleanroom facilities. "G" is taken around 10 μm so that the top metal plate is placed as horizontal as possible on the dielectric layer condsidering the sputtering process during the fabrication. "G" is not taken smaller in order not to increase the effect of fringing fields. The line lengths "L1" and "L2" have no effect on the capacitance since they are added to circuit model and their effects are subtracted from the overall device characteristics.

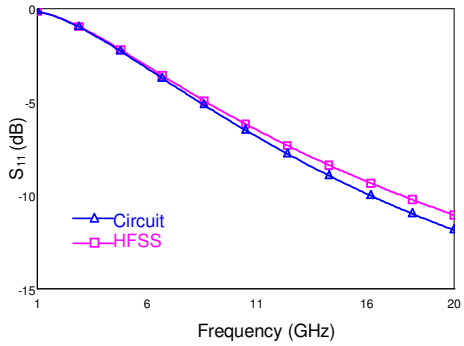
Table 3.8 gives the simulated capacitors together with the initially calculated capacitances and their dimensions; Table 3.9 gives the extracted lumped elements of the circuit model. The simulation results are given in Figure 3.20, Figure 3.21, Figure 3.22, and Figure 3.23.

Table 3.8: MIM capacitor library and design parameters.

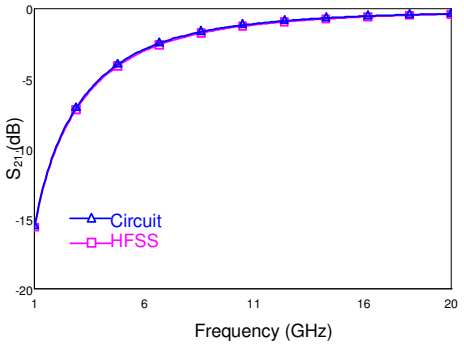
Name	Calculated Capacitance (pF)	Circuit Model Capacitance (pF)	W1 (um)	W2 (um)	L1 (um)	L2 (um)	L3 (um)	G (um)
C1	0.25pF	0.274291	194	60	317	221	21	7
C2	0.3pF	0.3287	194	60	317	221	28	7
C3	0.5pF	0.4768	194	72	595	535	55	11
C4	0.86pF	0.871291	194	60	317	221	74	7
C5	1pF	0.990523	194	72	560	570	80	11
C6	1.7pF	1.76846	194	120	317	221	55	7
C7	2pF	2.11664	194	72	490	640	150	7
C8	3.5pF	3.62752	194	160	490	640	110	7
C9	5pF	5.16361	194	160	490	640	165	7
C10	10pF	9.87769	194	160	490	640	310	7

Table 3.9: Circuit model element values of the capacitors in the library.

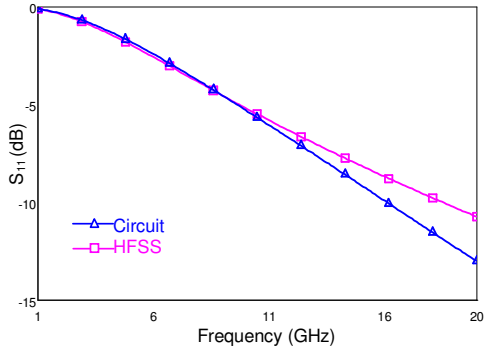
Name	C (pF)	Rs (Ω)	Ls (nH)	Cp (pF)	Rp (Ω)	L1 (um)	L2 (um)
C1	0.274	0.0532	0.0032	0.0141	221261	159.423	602.022
C2	0.328	0.0643	0.0045	0.0193	79878	159.946	594.487
C3	0.476	0.0719	0.0030	0.0168	182951	644.409	685.492
C4	0.871	0.1315	0.0051	0.0278	75319.5	257.794	465.149
C5	0.990	0.1363	0.0042	0.0164	∞	706.093	595.238
C6	1.768	0.0944	0.0070	0.0272	58044.7	368.902	285.669
C7	2.116	0.1406	0.0058	0.0253	∞	545.646	671.72
C8	3.627	0.1397	0.0063	0.0172	∞	495.389	721.709
C9	5.163	0.1830	0.0048	0.0172	∞	608.332	624.438
C10	9.877	0.1384	0.0068	0.0220	∞	580.678	688.577



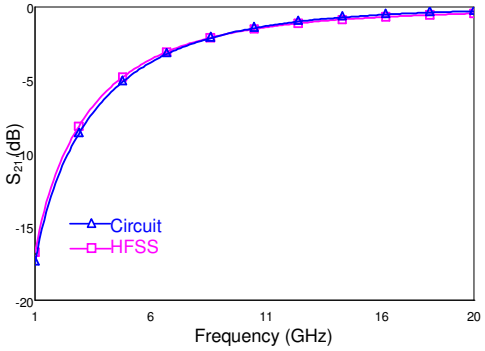
(a) S_{11} comparison for C = 0.27 pF



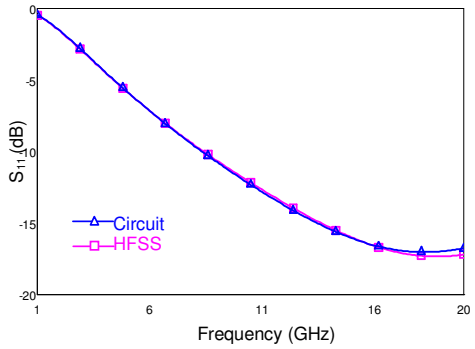
(b) S_{21} comparison for C = 0.27 pF



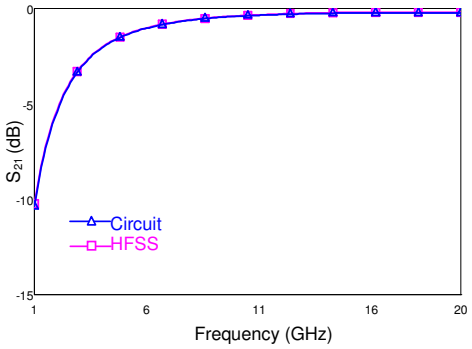
(c) S_{11} comparison for C = 0.33 pF



(d) S_{21} comparison for C = 0.33 pF

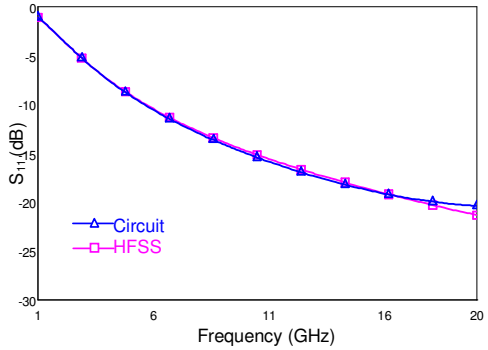


(e) S_{11} comparison for C = 0.48 pF

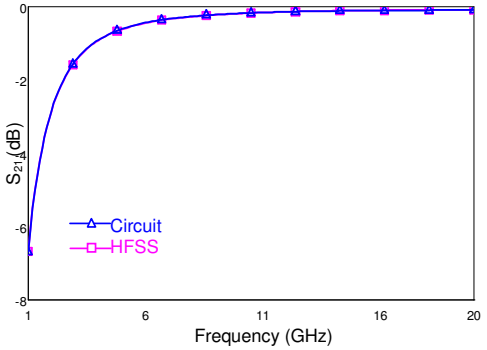


(f) S_{21} comparison for C = 0.48 pF

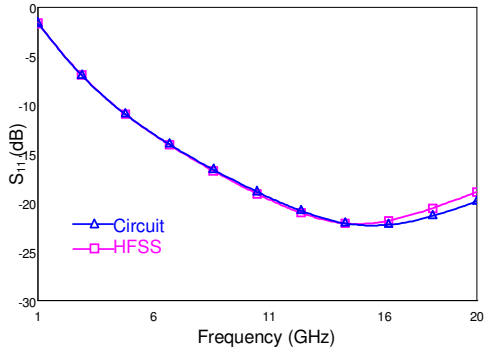
Figure 3.20 (a) – (f): Comparison of S-parameters extracted from EM simulations and circuit responses of C1, C2, and C3.



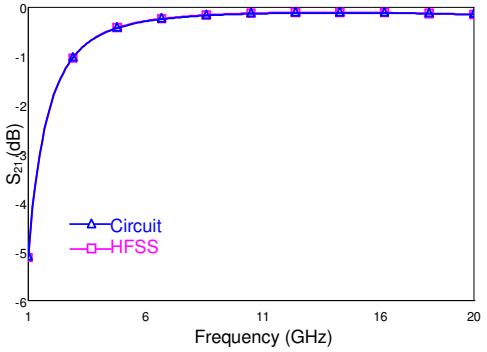
(a) S_{11} comparison for C = 0.87 pF



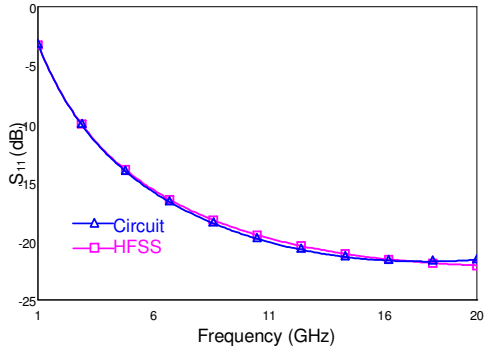
(b) S_{21} comparison for C = 0.87 pF



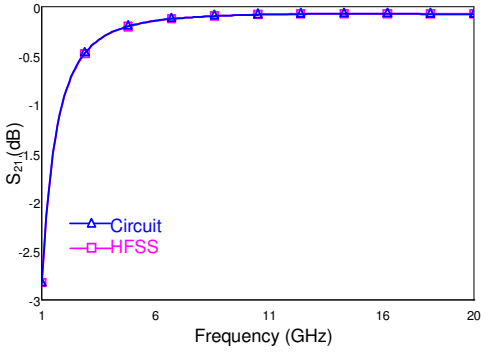
(c) S_{11} comparison for C = 0.99 pF



(d) S_{21} comparison for C = 0.99 pF

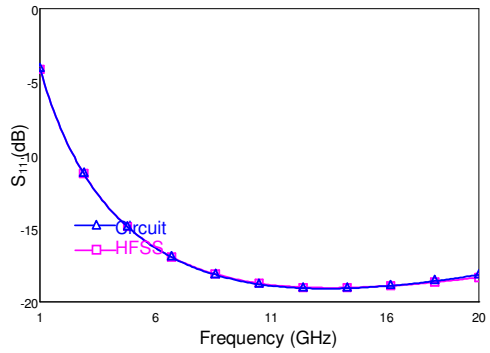


(e) S_{11} comparison for C = 1.77 pF

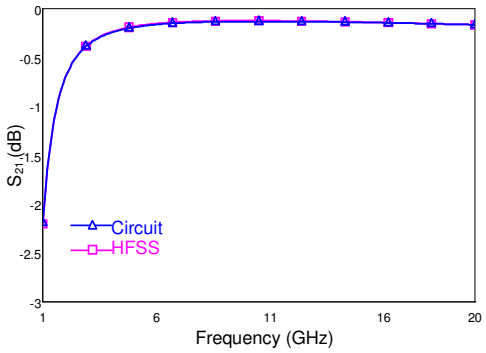


(f) S_{21} comparison for C = 1.77 pF

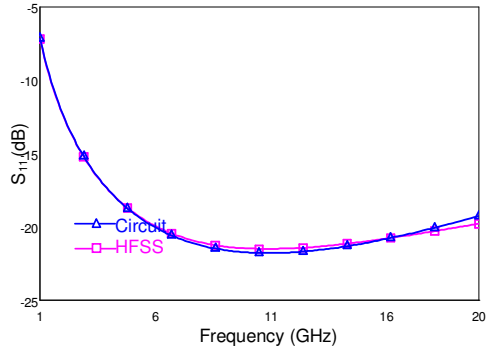
Figure 3.21 (a) – (f): Comparison of S-parameters extracted from EM simulations and circuit responses of C4, C5, and C6.



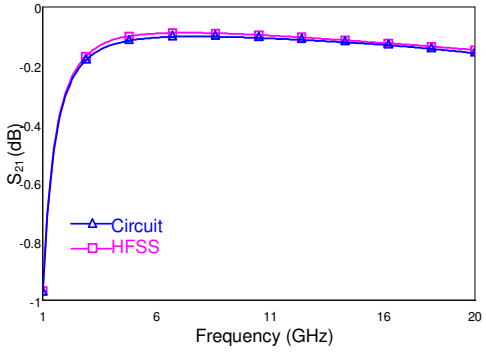
(a) S_{11} comparison for C = 2.12 pF



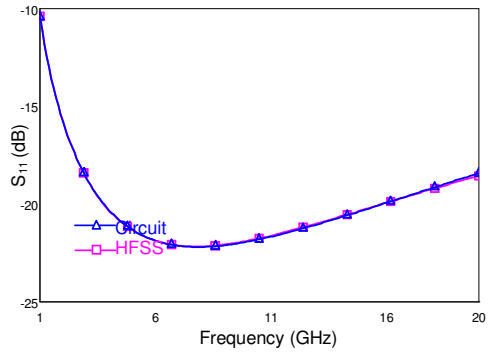
(b) S_{21} comparison for C = 2.12 pF



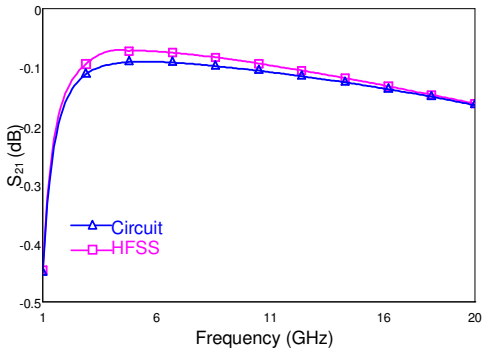
(c) S_{11} comparison for C = 3.63 pF



(d) S_{21} comparison for C = 3.63 pF

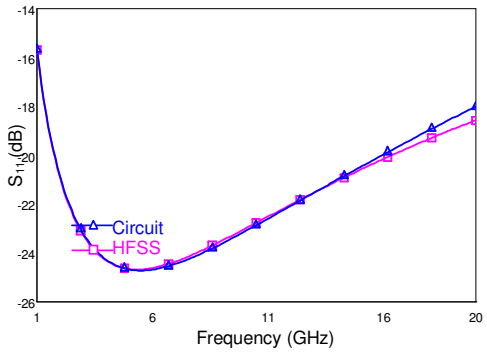


(e) S_{11} comparison for C = 5.16 pF

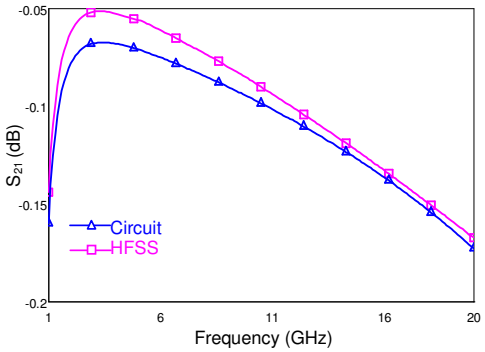


(f) S_{21} comparison for C = 5.16 pF

Figure 3.22 (a) – (f): Comparison of S-parameters extracted from EM simulations and circuit responses of C7, C8, and C9.



(a) S_{11} comparison for C = 9.88 pF



(b) S_{21} comparison for C = 9.88 pF

Figure 3.23 (a) – (t): Comparison of S-parameters extracted from EM simulations and circuit responses of C10.

During the optimization of the circuit model and the EM simulation results, the circuit element values, it is observed that each element has different effect on the overall characteristic of the capacitor. The parallel resistance Rp has a minimal effect on the S-parameters since its branch can almost be modeled as open circuit as shown in the tabulated list. The series inductance "Ls" and the parallel capacitance "Cp" are very close to zero; however each increment of these elements drastically changes the circuit response. The input and output CPW lengths; i.e. "L1" and "L2" are slightly different than the simulated structures due to the difference in simulation techniques of HFSS and MWO. For capacitance values more than 10 pF, the model begins to get distorted. As the total area increases in order to achieve higher capacitance values, the "L3" dimension also increases as the lateral dimension is limited by 220µm. However "L3" is obviously a part of the signal line and it is loaded by the dielectric layer and the top metal plate. As the capacitively loaded signal line section increases, it becomes less possible to have a matced response between the circuit model and the EM simulations.

3.4.5. Fabrication Process

The first metallization and backside metallization of the structures are same as any other structures explained in this work so they are skipped in this part. Also the sacrificial layer and second metallization stages are the same as the process flow of the inductors. What is new in this structure is the introduction of dielectric layer, namely the Silicon Nitride. The process flow of dielectric coating will be given in detail, however rest of the steps will be explained with figures since the process flow is exactly the same as the previous structures. Figure 3.24 shows the capacitor structure with only the first metallization.

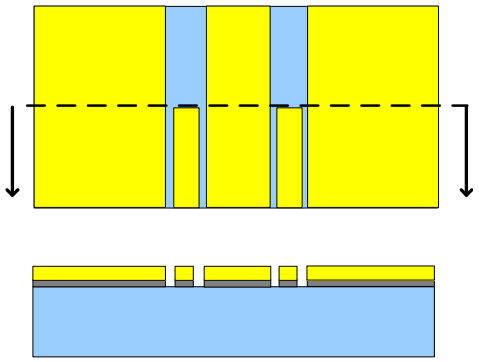


Figure 3.24: First metallization of the MIM capacitor.

The choice of dielectric layer in the capacitor fabrication is determined by the other RF MEMS structures on the wafer. Dielectric layers of RF MEMS switches shall withstand high actuation voltages and Silicon Nitride is a well known material with a breakdown voltage up to 90 Volts. Since this material is used for the switched structures, it is also used as the dielectric layer in the capacitors for process simplicity.

The silicon nitride is deposited on the wafer using plasma enhanced chemical vapour deposition (PECVD) techniques. Coated wafer goes into a lithography process

where S1828 is spun on the wafer and patterned in order to protect the selected areas in the etching stage. The etching of the silicon nitride is realized with reactive ion etching (RIE). When the dielectric layer is successfully etched, the protective photoresist layer is stripped with Acetone and rinsed with IPA. Table 3.10, Table 3.11, Table 3.12, Table 3.13 shows the process recipes and Figure 3.25, Figure 3.26, and Figure 3.27 show the schematics of the complete process steps including the release.

Table 3.10: Process recipe of SiN coating

PECVD SiN coating	
Pressure	900 mTorr
Temperature (Platten)	300°C
Temperature (Shower head)	250°C
Flow	N_2 : 1960 sccm SiH_4 : 40 sccm NH_3 : 40 sccm
Power	20 W 6 sec HF 20 W 2 sec LF
Deposition rate	130 Å/min
Time	23:00 min
Duration	0.3 um targeted
Log no	80-2

Table 3.11: Process recipe of the lithography for SiN RIE

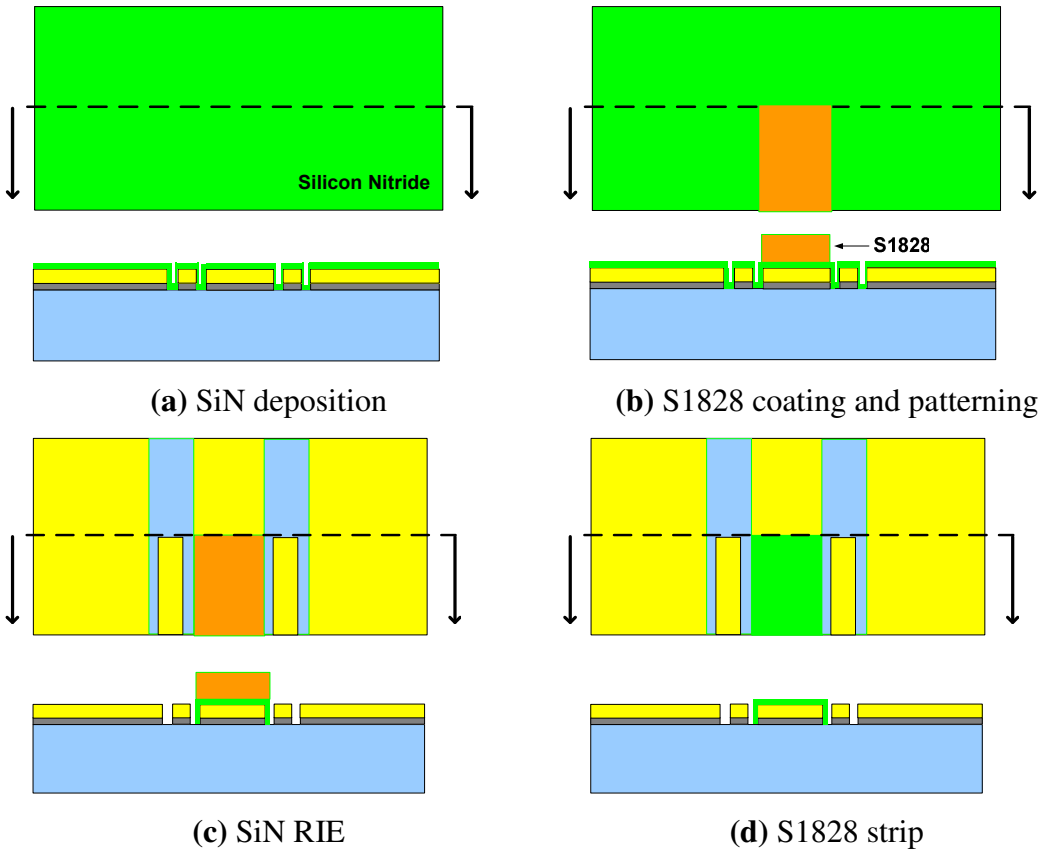
Lithography using S1828	
Dehydration	120 C° 10 min in oven
Primer HDMS	@ 500 rpm dispense (5 secs acceleration from 0 rpm-7 secs duration- 3 secs acceleration to 3000 rpm) @2000 rpm spin (30 secs duration-3secs deceleration to 500 rpm) @ 500 rpm final speed (10 secs duration-3 secs deceleration to 0 rpm)
Spin **S 1828**	@ 500 rpm dispense (5 secs acceleration from 0 rpm-10 secs duration- 5 secs acceleration to 3750 rpm) @3750 rpm spin (30 secs duration-3 secs deceleration to 500 rpm) @ 500 rpm final speed (10 secs duration-3 secs deceleration to 0 rpm)
Softbake	115 C° on hotplate for 3:30 min (+30 secs hold the wafer close to the plate)
Exposure	16 secs @ 18 mW/cm^2
Development	1:45 min development in MF26 A solution
O_2 plasma	2 min duration Plasma power: 300 W Plasma pressure: 0.25-0.3 Torr
Hardbake	120°C 20 min in oven

Table 3.12: Process recipe for SiN RIE

SiN RIE	
Pressure	70 mTorr
Flow	CF_4 : 60 sccm CHF_3 : 22 sccm O_2: 10 sccm
Power	250 W
Duration	739-1 40 + 5 + 5 + 5 + 6 sec 741-2 5 sec 746-2 10 + 10 sec 747-1 5 + 5 + 5 + 5 + 5 sec

Table 3.13: Process recipe for PR strip

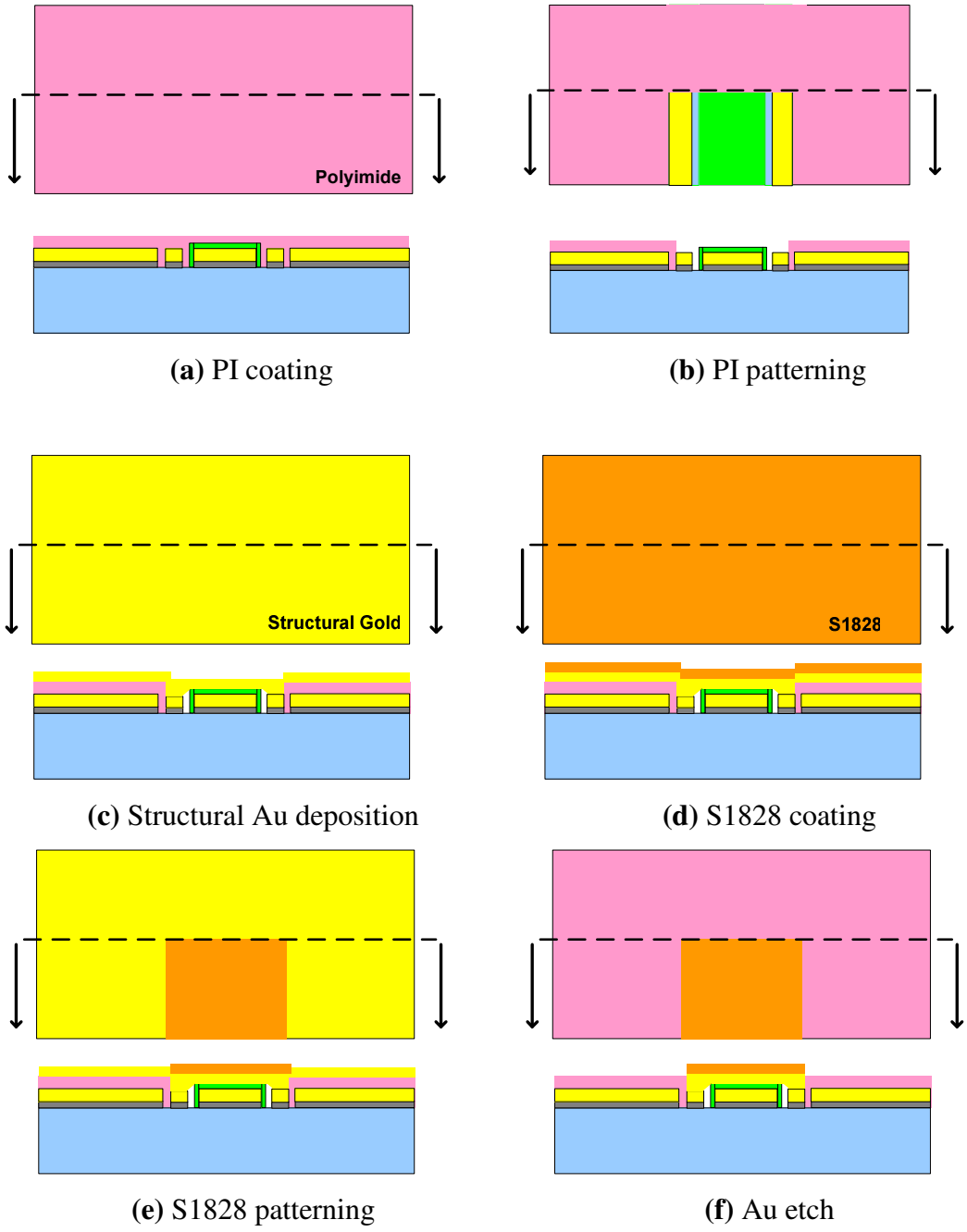
Photoresist Strip	
Resist Strip	Acetone + IPA + DI rinse + IPA
Resist Strip	80 C° SVC-175 5:00 min
O_2 plasma	10:00 min duration Plasma power: 300 W Plasma pressure: 0.25-0.3 Torr



(a) SiN deposition **(b)** S1828 coating and patterning

(c) SiN RIE **(d)** S1828 strip

Figure 3.25 (a) – (d): Lithography steps up to silicon nitride patterning.



(a) PI coating

(b) PI patterning

(c) Structural Au deposition

(d) S1828 coating

(e) S1828 patterning

(f) Au etch

Figure 3.26 (a) – (f): Lithography steps up to etching of the structural gold.

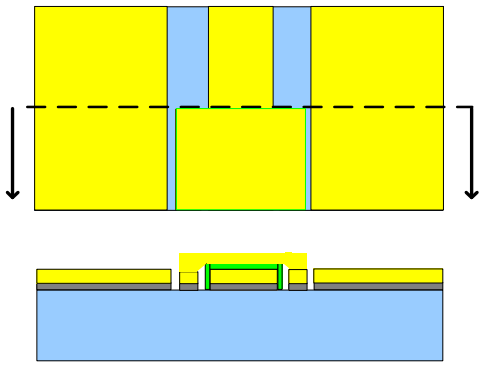


Figure 3.27: Polyimide and phorotesist strip.

3.5. Low-Pass Filter Design

The first filter type constructed using the elements of the capacitor and the inductor library is a low pass filter with a cut off frequency of 2 GHz. The circuit model of the filter is designed with FilPro Student Version. The capacitors and inductors that are not included in the libraries are designed with ANSOFT HFSS v9.2^{TM} and these new elements are added to the library. The S-parameters of the filter topology using EM simulation results and the circuit model are compared to verify the design methodology. It is important to notice that the complete EM simulation of the full filter structure cannot be done due to the complexity as the inital meshing during the FEM is not completed successfully. So in order to understand the behaviour of the filter structure, the EM simulation results of individual elements are used as building blocks to create a box design which has the same topology as the circuit model.

Figure 3.28 shows the circuit model of the low pass filter. The initial circuit model is constructed using the LC prototype and the response is chosen as Chebychev with a pass band ripple of 0.1 dB. However the extracted element values exceed the limits of realizability, consequently an optimization is compulsory to create a filter

topology with available components. The element values are tuned and a topology with minimum number of inductors is acquired. A satisfactory filter response is obtained with a compromision between element values and circuit response. Figure 3.29 shows the circuit response in dB.

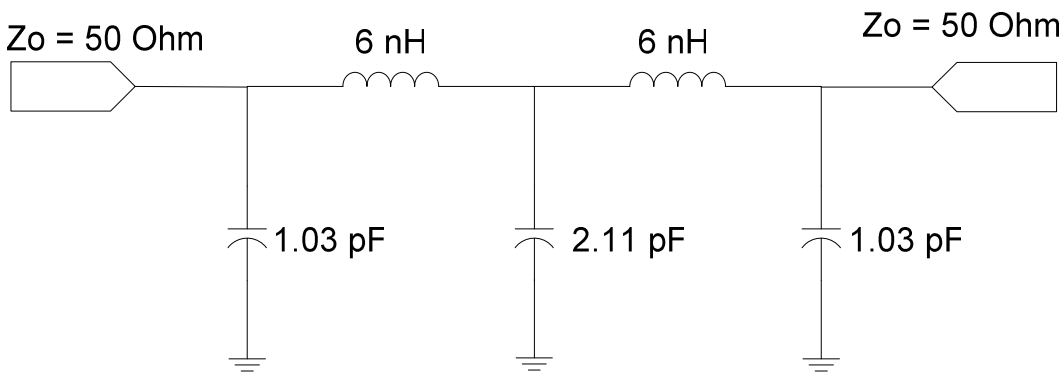


Figure 3.28: Circuit model of the low-pass filter.

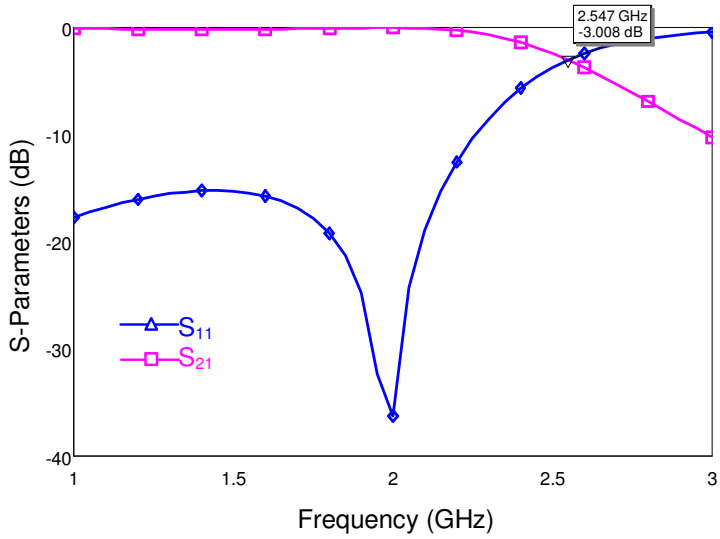


Figure 3.29: Circuit model S-parameters of the low-pass filter

As seen in the S-parameter response of the circuit, the 3 dB frequency is obtained at 2.547 GHz which has to be 2 GHz in the final design. However, the realization of the filter requires interconnecting transmission lines between each element and junctions for the shunt components and also input and output transmission lines. As these junctions and interconnecting transmission lines are added to the system, these elements increases the overall system inductance and the critical frequency shifts to a lower level which is set to 2 GHz by carefully choosing the transmission line dimensions. As seen in the S-parameter response, the reflections are kept below -15 dB in the pass band region where S_{21} is less than -0.1 dB in the pass band.

The EM simulations are cascaded using ADS Momentum to construct the same topology of the circuit model with the EM simulation results. Figure 3.30 gives the basic layout of the EM box simulation and Figure 3.31 shows the related system response compared with the circuit model. The EM system in this case is not the final design since it lacks the junctions and the interconnecting transmission lines.

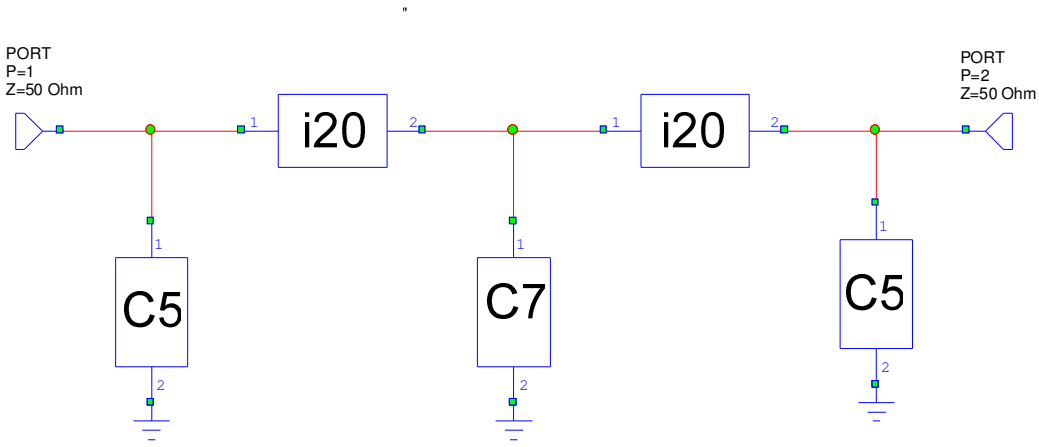


Figure 3.30: Layout of the low-pass filter with EM simulated lumped element blocks.

The capacitances and the inductors of the EM box system almost match with the circuit elements. The verificiation is also repeated by observing the S-parameters of a single circuit element and EM simulation result of an element in the library. As explained earlier, at high frequencies, especially for the inductors, the inductive behaviour vanishes as the SRF becomes smaller. So this limits the filter characteristics to a certain frequency region. This becomes more important in the band pass filter design where the region of operation is at higher frequency and it is ignored for this low pass structure.

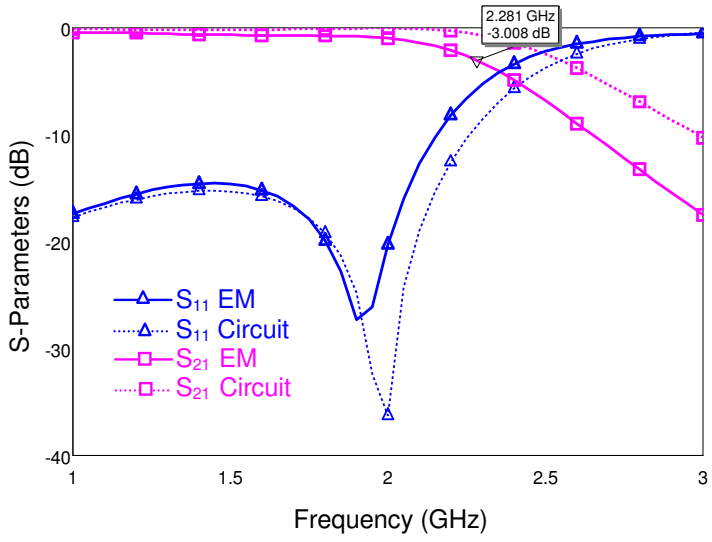


Figure 3.31: S-parameter comparison between EM box simulation and circuit simulation.

From the comparison of the EM results and the circuit results, the new cut off frequency is 2.281 GHz which is an improvement of 266 KHz with respect to the circuit model at the expense of 10 dB more reflection around 2GHz. However the maximum reflection up to 2 GHz is slightly better. Since the elements are not ideal as the circuit model, a significant insertion loss is introduced where S_{21} decreases by -0.4 to -1dB in the 1-2 GHz band.

The next step in the design is to introduce interconnecting transmission lines and tee junctions to the EM simulation block diagram so that the filter structure is realizable. Figure 3.32 shows a junction point consisting of a tee junction and three equal transmission lines. This structure is replaced with the connection lines in Figure 3.30 so that all parasitic effects are taken into consideration. The transmission line is a CPW with signal width 60 µm and ground-signal gap 80 µm with a total length of 500 µm. The tee junction is also a CPW structure with same signal and ground dimensions as the transmission lines to minimize discontinuity effects. To minimize the parasitics, the grounds around the tee junction are connected with three distinct 30 µm wide air bridges to ensure a common ground in the system. The dimensions of the lines and tee junction is determined in order to optimize the the filter behaviour so that it provides minimum reflection and insertion loss with a critical frequency of 2 GHz. Figure 3.33 shows the final topology of the low-pass filter including the interconnections and input-output CPW ports.

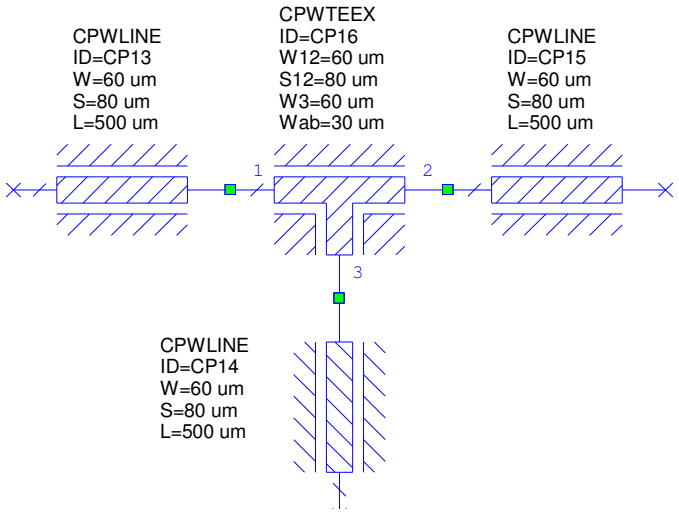


Figure 3.32: Schematic of the Tee junction and the interconnecting CPW sections with dimensions.

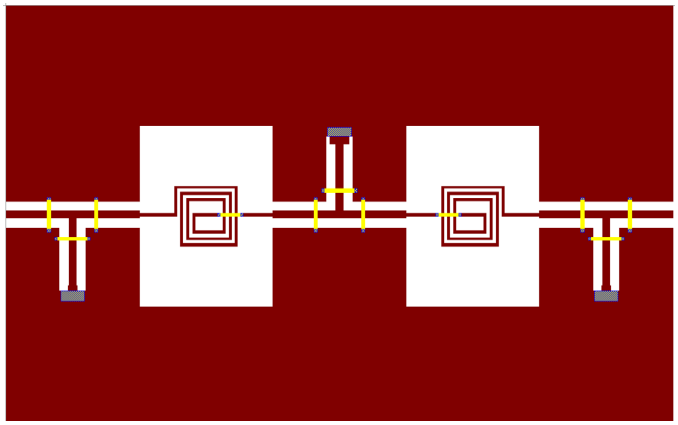


Figure 3.33: Final topology of the low-pass filter.

Figure 3.34 shows the response of the final filter structure. The 3 dB frequency is obtained at 2.009 GHz and the maximum S_{11} magnitude in the pass band is kept below -15 dB up to 1.8 GHz. The insertion loss is moderate as S_{21} magnitude is -0.5 dB at 1 GHz and -1.2 dB at 1.8 GHz. When we compare this result with the initial circuit model, we see a 547 KHz improvement in cut off frequency.

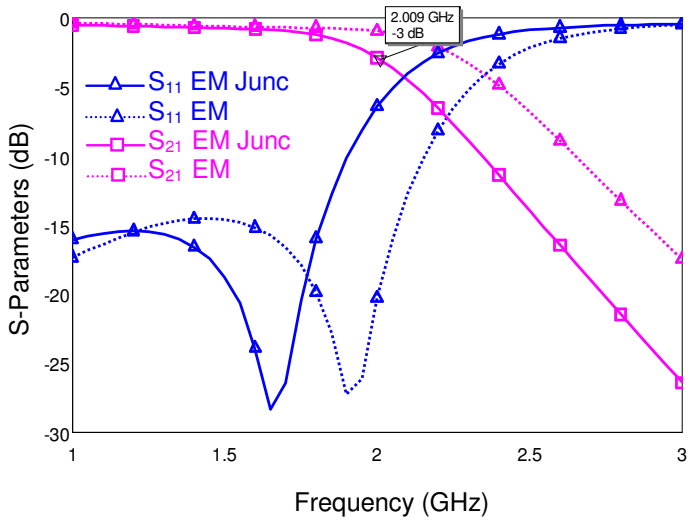


Figure 3.34: S-parameter comparison of the EM box models with and without interconnecting elements.

3.6. Band - Pass Filter Design

The second type of filter constructed using the capacitor and inductor library is a band pass filter with a 2 - 4.6 GHz pass band. The design procedure is more or less the same as the low pass filter where the circuit model of the filter is defined by FilPro Student Version and elements of the EM simulated filter structure are chosen to be the elements of the capacitor and inductor libraries. Finally once more the S-parameters of the filter topology using EM simulation results and the circuit model are compared to verify the design methodology. The meshing problem in the full EM analysis using ANSOFT HFSS v9.2^{TM} is observed in this filter type just as the case of the low pass type. So each inidividually simulated elements are cascaded in the full filter system and same topology of the circuit model is constructed.

Figure 3.35 shows the circuit model of the band pass filter structure and Figure 3.36 shows the filter characteristics. The initial circuit model is constructed using the LC prototype and the response is chosen as Chebychev with a pass band ripple of 1 dB which reduces the the order of the filter so that the tunability of the elements increases. The elements are tuned to be the same of the elements in the libraries. As seen in the S-parameter plots of the inductors, the SRF limits the inductive behaviour of the inductors which automatically limits the filter characteristics up to a certain frequency. To be more explicit, for high inductance values the usable frequency is more limited since SRF is lower, where for the low inductances it is just the opposite.

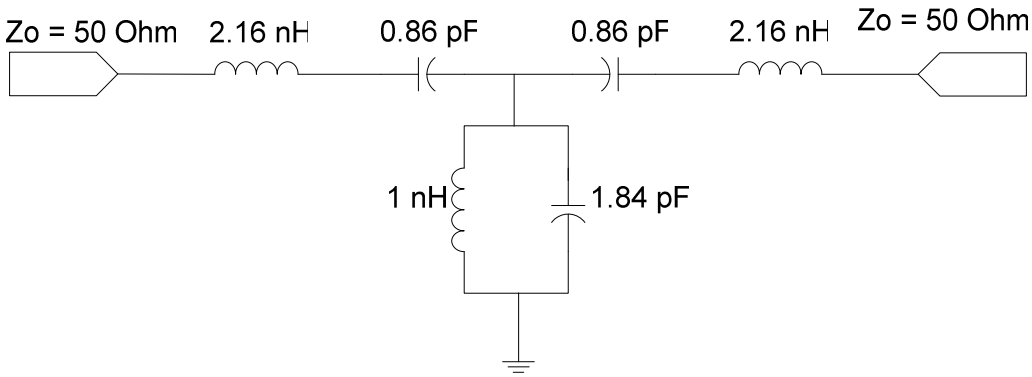


Figure 3.35: Circuit model of the band-pass filter.

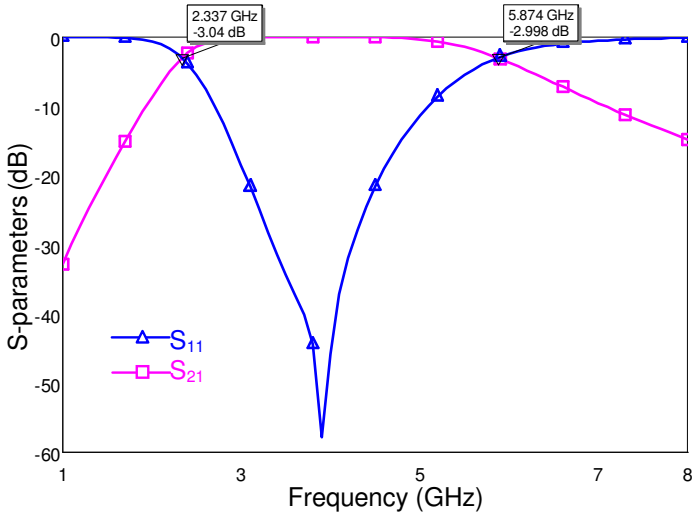


Figure 3.36: Circuit model S-parameters of the band-pass filter.

The 3-dB critical frequencies of the initial circuit model are 2.337 and 5.874 GHz. A very low reflection is realized where S_{11} is obtained as -57.84 dB at 3.9 GHz in the pass band and it is above -0.5 dB at frequencies lower than 2 GHz and higher than 7 GHz. The insertion loss parameter S_{21} is below 0.1 dB in the 2.93-4.7 GHz band.

While constructing the full system with EM simulated sub-blocks, the inductance contribution of the discontinuities in CPW and CPW to microstrip direct transitions in the inductor input ports are taken into consideration. Consequently, the inductors used in the EM simulated topology have lower inductances than the circuit model to compromise this effect. Figure 3.37 shows the full schematic of the filter structure including junctions and transmission lines and Figure 3.38 gives its s-parameters in comparison with the circuit response. The width of the CPWs in the tee junction and in the interconnecting lines is 60 µm and the ground gap is 80 µm, where the air bridge width in the tee junction is 25 µm. The total length of the interconnecting lines is 200 µm which is defined during the filter character optimizations. The final topology of the band-pass filter including the interconnections and input-output CPW ports can be seen in Figure 3.39.

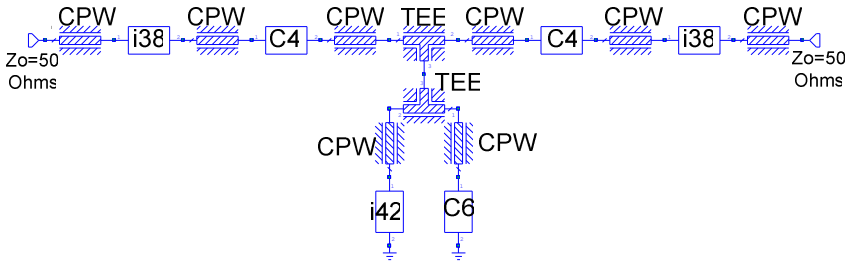


Figure 3.37: Layout of the band-pass filter including the interconnecting elements.

The comparison between circuit model and the EM simulated structure clearly shows that the pass band of the filter has become narrower and moved to lower frequencies with respect to the circuit model. The percentage bandwidth of the filter is 89%. The new 3 dB frequencies are obtained at 1.96 and 4.629 GHz and the minimum S_{11} of -22.26 dB is obtained at 2.6 GHz. In the frequency band 2.38-3.85 GHz S_{21} is observed to be less than 1 dB.

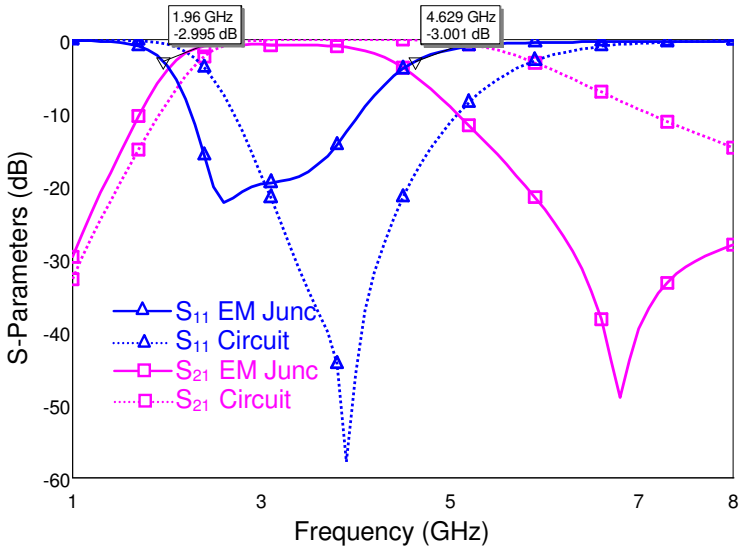


Figure 3.38: S-parameter comparison of the interconnected EM box model and circuit model.

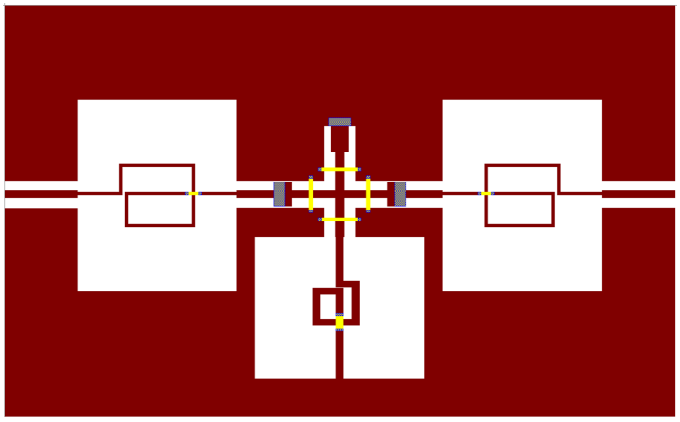


Figure 3.39: Final topology of the band-pass filter

CHAPTER IV

RF MEMS PACKAGING USING BENZOCYCLOBUTENE (BCB) AS SEALING AND BONDING MATERIAL

In this chapter studies on RF MEMS packaging with BCB is explained. Section 4.1 gives an introduction about the topic and Section 4.2 gives the previous research studies on packaging. Section 4.3 explains the patterned polymer adhesives including BCB and Section 4.4 gives a parametric analyis of a capping chip. Section 4.5 explains the necessary feed-through modification for packaging and Section 4.6 gives the proposed fabrication steps. Finally Section 4.7 explains an experimental packaging process.

4.1. Introduction

RF MEMS devices like switches, resonators and tunable coupled elements contain movable and fragile parts which shall be encapsulated for two main reasons. First, to ensure protection during wafer handling, wafer dicing or system integration. Second, to ensure reliable and stable device performance characteristics by providing dedicated medium of operation. The encapsulation can be realized after the wafer is diced; however the individual packaging of each component will bring a high cost and too many technological complexities. Consequently it is desirable that the packaging is carried out before the dicing stage. The packaging that is implemented on the whole wafer is called wafer level or 0-level packaging. This

type of packaging has an on-wafer device scale package that covers the MEMS device by means of a sealed cavity. When this first protective structure is introduced, the MEMS device can be diced without damage.

The individual packaged device can be obtained by three different assembly methods which are wafer-to-wafer, chip-to-wafer or chip-to-chip packaging. Each method has its own advantages depending on many factors like device type, number of devices to be packaged on wafer, device size, ease of processing, available equipment and cost. If the number of MEMS devices to be packaged on a wafer is small, chip-to-wafer bonding, which is carried out in a pick-and-place operation, can be preferred. This type of bonding is also beneficial since it enables different cap materials to be used for the same device wafer. Wafer-to-wafer bonding is less costly and simple to fabricate when a large number of cavities are to be fabricated per wafer.

In this work, wafer-to-wafer bonding is studied since each RF MEMS wafer contains a lot of switches which are too difficult to handle separately using chip-to-wafer bonding method.

The wafer-to-wafer bonding method also has its subcategories in terms of bonding techniques. Specific bonding method is guided by the required strength, level of hermeticity and ambient pressure inside the package, and further, by the impact the package has on the electrical performance of the device, by the process compatibility and finally the allowable cost. Bonding techniques that can be used for this purpose include metal bonding (solder, gold-gold thermo-compression, etc), fusion, anodic, glass frit bonding or polymer adhesives.

4.2. Previous Studies on RF MEMS Packaging

The first example for MEMS packaging for coplanar MMIC structures are presented in [54]. A common resistivity silicon (1-30 Ω-cm) carrier is proposed in order to reducre coplanar parasitic problems of leakage, coupling, and resonance. The proposed carrier scheme is verified by fabricating and measuring the GaAs CPWs on three types of Si-carriers (Gold-plated carrier, 15 Ω-cm Si-carrier, HRS carrier) in the frequency from 0.5 to 40 GHz.

The second example demonstrates a technique to premold and transfer lead-free solder balls for MEMS packaging applications [55]. A bulk micromachined silicon wafer is used to mold a solder paste and remove excess flux prior to transfer to a host wafer that may contain released MEMS. It is reported that the packages survive over 600 hours in an autoclave (130°C, 85% RH, 2 atm) and more than 1300 temperature cycles (55 °C to 125 °C).

The third example is a flip chip hermetic RF MEMS packaging presented in [56], where a typical solid-state RF switch might be a discrete device integrated onto an RF microcircuit using a flip-chip process. This integration process allows the device to come into very close contact with the transmission line, reducing signal degradation. However it is claimed that for a high performance system, vacuum encapsulation is required which potentially leads to large device costs and poor long-term performance due to vacuum degradation.

The last example is a packaging method using LTCC capping substrate and BCB adhesive bonding presented in [57]. The LTCC substrate is used as a capping substrate and silver via holes are implanted in LTCC substrates are used as RF feedthroughs, a vertical interconnection. BCB layers play a role in bonding of MEMS device and LTCC capping substrate. The measured value of the only CPW line without a packaging has the insertion loss of 0.047 dB at 2GHz, and 0.092 dB at

20 GHz respectively. After packaging, the insertion loss of the packaged CPW is 0.091 dB at 2GHz and 0.312 dB at 20 GHz, respectively.

4.3. Wafer-Level Packaging with Patterned Polymer Adhesive

Adhesive full-wafer bonding is a technique which uses a polymer as an intermediate layer between two wafers to be bonded [58]. The polymer is applied, usually by spin coating and usually to the cap wafer, and the bonding is carried out involving pressure and a temperature high enough to fully cross-link the polymer in order to achieve a strong adhesion between the wafers and polymer, and to get a strong bulk of the polymer itself.

The main advantages of adhesive bonding are as follows:

- Integrated circuit compatibility due to low process temperature and no applied voltage during process.
- Insensitivity to particles and surface nonuniformities.
- Adjustable polymer thickness range.
- Simple and robust processing.
- Good polymer adhesion to most materials used in microsystems and microelectronics production.
- Substrate material independence and ability to bond different substrates.
- Polymers do not contain ions that diffuse into silicon and change its electrical properties.
- The adhesive can be patterned prior to bonding to create defined cavities in the bonding layer
- The polymer bonding layers act as a stress buffer between the bonded structures due to their elastic properties.

The bonding material shall be chosen concerning the required process compatibility, thermal stability, mechanical stability, creep strength, chemical resistance, handling, etc.

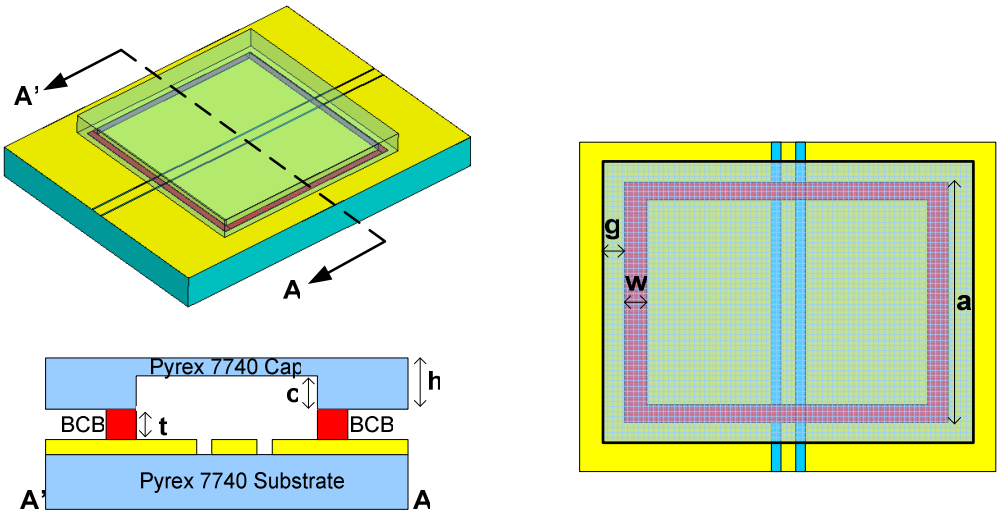
Benzocyclobutene (BCB) [59] from the Dow Chemical Company is found to be the most suitable for adhesive bonding since no outgasing occurs during curing process and it is possible to pattern the material in a soft cured state. The patterning can be done either by dry etching or by using a photosensitive version of the material. Dry-etch BCB is available for a single layer thickness from 1 to 26 µm and photosensitive version is available for a single layer thickness up to 40 µm.

Using BCB for the sealing and bonding material defines a relatively simple and low-temperature process which is less than 250^{o}C. In particular, the liquid-like behavior of BCB observed during curing makes the sealing of cavities with protruding signal feedthroughs rather straightforward, compared to the more complex buried feedthroughs implemented for metal, anodic or silicon direct bonding. Moreover, BCB bonding, like every polymer bonding, is not susceptible to particles compared to anodic or fusion bonding which requires very clean and flat surfaces and does not need extra electrical field as required for anodic bonding (about 1 kV is usually required, which might be a problem for dielectric breakdown). Furthermore, its high resistivity (10^{19} Ωcm), low loss tangent (0.0008–0.002 in the range 1 MHz–10 GHz) and low permittivity (2.65) make BCB a very good candidate for high-frequency (RF-MEMS) applications. One drawback of polymer bonding, including BCB, is that this method does not provide with hermeticity in terms of gas-tightness [60].

4.4. Parametric Analysis of a BCB Package using EM Simulations

In order to examine the effects of a BCB packaging structure on a particular RF MEMS device, EM simulations of a packaged CPW line with different package dimensions are performed and their effects on the RF characteristics are observed.

Figure 4.1 shows a schematic view of a packaged CPW with a BCB ring. A Pyrex 7740 capping chip placed on the BCB ring with a cavity depth of "c" and cap thickness of "h". The side length of the square BCB ring is "a" and the thickness of the BCB layer is "t". The capping chip extends from the sides of the BCB ring and the length of this extension is "g". CPW is patterned on a Pyrex 7740 substrate which is 500 µm thick and gold is used as the metallization layer whose thickness is 2 µm. The signal and signal-to-ground dimensions of the CPW are taken as 170 and 20 µm respectively in order to satisfy 50 Ω characteristic impedance at the CPW ends and the total length of CPW is 5000 µm.



(a) Perspective and cross-section **(b)** Top view

Figure 4.1 (a) – (b): Different views of a packaged CPW structure.

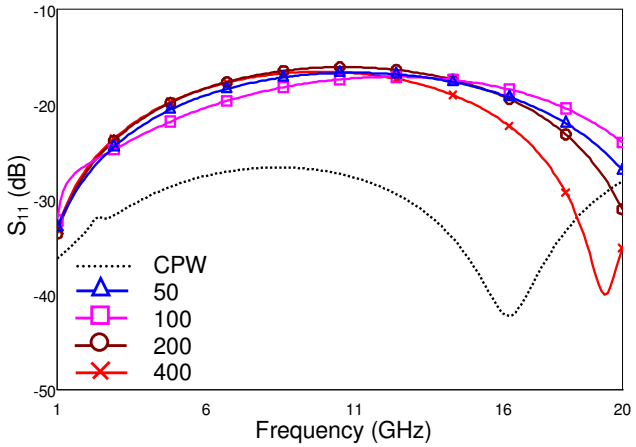
The EM Simulations are performed with ANSOFT HFSS v9.2^{TM} in 1-20 GHz frequency band. Several values are used for the given parameters and s-parameters of each design are observed. Table 4.1 gives the parameter values used in the simulations.

BCB thickness is chosen in the range which can be achieved with process conditions and the width of the BCB ring is chosen in the range such that the capping chip is mechanically well supported and the RF signal is not distorted much.

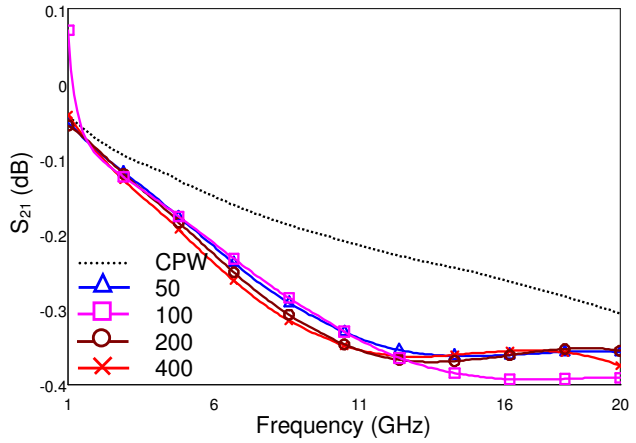
Table 4.1: Design parameters of the simulated packaged CPW structure

Parameter	Value in micrometers
g	50,100,200,400
h	100,300,400,500
t	5,7,10,15,30
w	100,200,400,800
c	10,20,30,40,50,100
a	3000

The effect of each parameter change is observed by varying the desired parameter in the given range and keeping all the other parameters fixed. Figure 4.2 shows the s-parameters with varying "g". The rest of the parameters are kept fixed as "t = 5 µm", "w = 100 µm", "a = 3000 µm", "h = 300 µm", and "c = 0 µm". The simulation result of an unpackaged CPW is also added to the plots in order to fully observe the effect of the glass cap. The cap section introduces an external loading to the CPW and the overall electrical length of the structure decreases as the dielectric constant of the medium is partially increased. However the amplitude alteration is negligible as seen in the plots and the amplitude is mostly dependent on the other parameters. Maximum S_{11} is obtained below -17 dB in all structures and minimum S_{21} is above -0.4 dB in the 1-20 GHz frequency band.



(a) S_{11} characteristics of packaged CPW with varying "g"

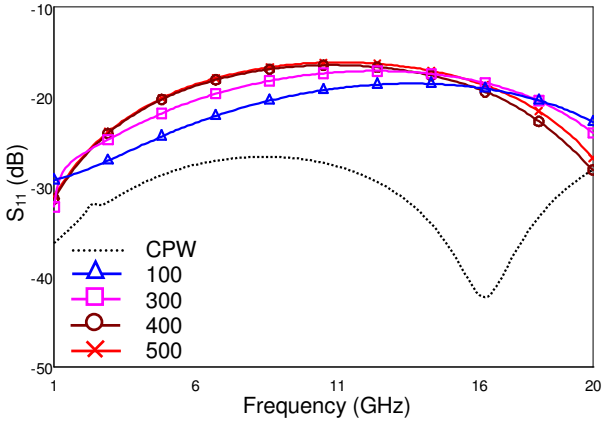


(b) S_{21} characteristics of packaged CPW with varying "g"

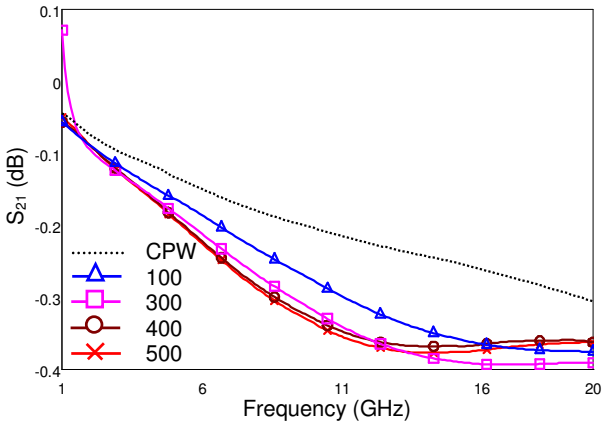
Figure 4.2: S-parameters of packaged CPW structures with varying "g" parameter.

Figure 4.3 shows the parametric analysis of "h" in terms of s-parameters where the other parameters are kept constant as "t = 5 µm", "w = 100 µm", "a = 3000 µm", "g = 100 µm", and "c = 0 µm". The cover thickness determines the amount of capacitive loading over the CPW. Since the dielectric constant of the medium increases with the introduction of the cap, the overall characteristic impedance begins to deviate from 50 Ω which increases reflections in the CPW. For the

thinnest cap, S_{11} is observed below -20 dB in the entire frequency band however for the thickest case, it is below -17 dB. S_{21} values for all "h" values are obtained above -0.4 dB.



(a) S_{11} characteristics of packaged CPW with varying "h"

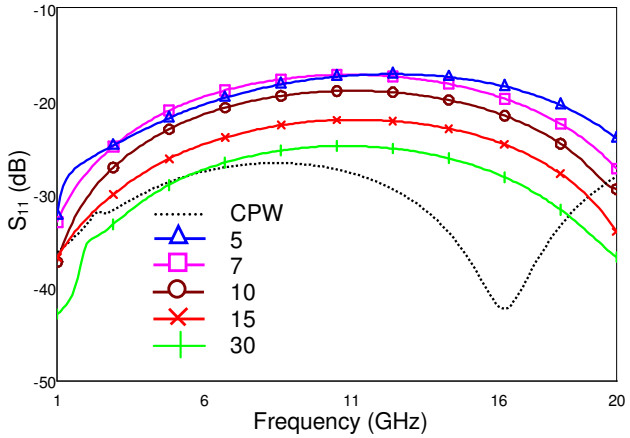


(b) S_{21} characteristics of packaged CPW with varying "h"

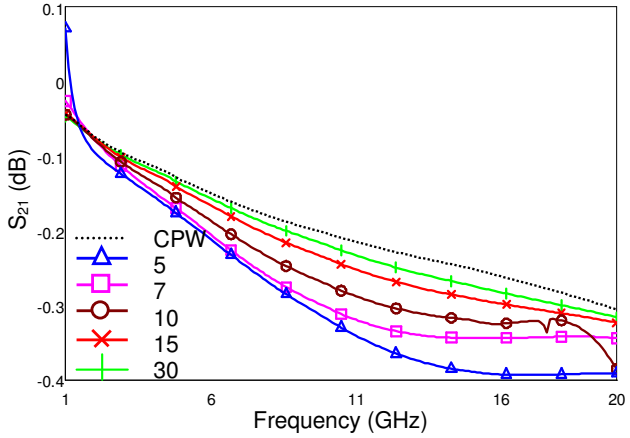
Figure 4.3: S-parameters of packaged CPW structures with varying "h" parameter.

The BCB thickness "t" is one of the dominant parameters which affect the CPW characteristics. The thickness both determines the capacitive loading of the BCB

ring and the glass cap which stands on top of the ring. Figure 4.4 shows the simulated s-parameters for varying "t" as the other parameters, i.e. "g = 100 µm", "w = 100 µm", "a = 3000 µm", "h = 300 µm", and "c = 0 µm" are fixed. S_{11} values for "t = 5 µm" are obtained below -18 dB, where for "t = 30 µm" they are below -27 dB which is a great improvement from the prior case. S_{21} values of all variants are kept above -0.4 dB up to 20 GHz.



(a) S_{11} characteristics of packaged CPW with varying "t"

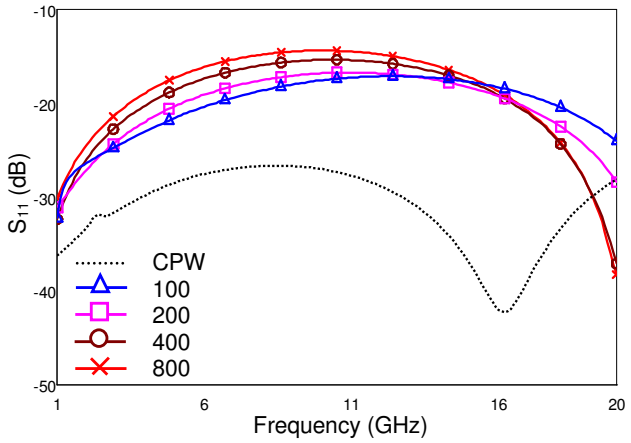


(b) S_{21} characteristics of packaged CPW with varying "t"

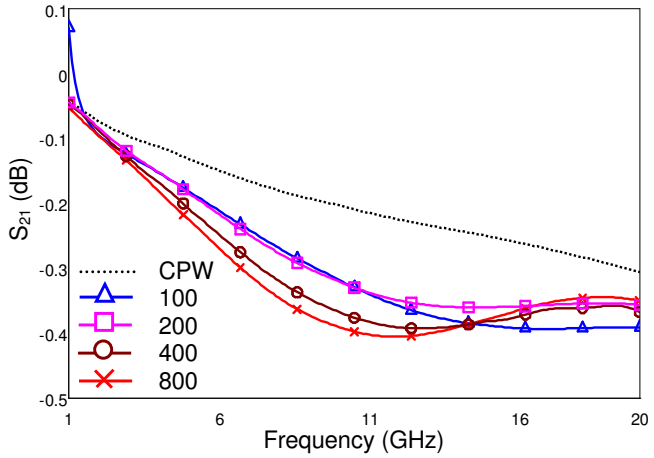
Figure 4.4: S-parameters of packaged CPW structures with varying "t" parameter.

The width of the BCB ring "w" is crucial in the feedthrough sections of the CPW since the width corresponds to the length of the unmatched line due to BCB filled

gaps in the CPW ports. Figure 4.5 shows that for "w = 800 µm" maximum S_{11} is observed to be below -14 dB, however for "w = 100 µm" it is obtained below -19 dB. Minimum S_{21} is observed to be below -0.4 dB in the entire band.



(a) S_{11} characteristics of packaged CPW with varying "w"

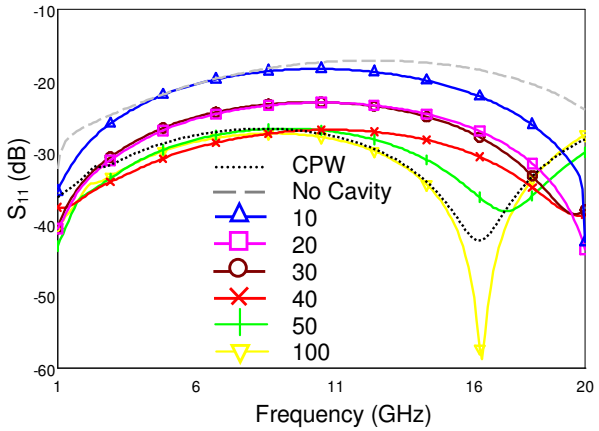


(b) S_{21} characteristics of packaged CPW with varying "w"

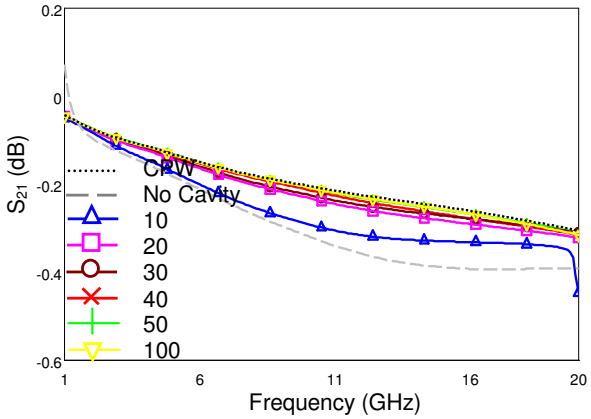
Figure 4.5: S-parameters of packaged CPW structures with varying "w" parameter.

Figure 4.6 shows the simulated s-parameters for different cavities. At first glance, it is noticed that for "c = 100 µm", the characteristics of a cap free CPW and capped CPW are almost the same where the maximum S_{11} is below -28 dB and minimum S_{21} is above -0.23 dB in 1-20 GHz. As the cavity gets shallower, reflections begin to

occur and also the electrical length begins to decrease since the overall dielectric constant begins to increase. For cavity depth of 10 µm, the reflection is kept below -20 dB and the insertion loss is above -0.4 dB for all frequencies.



(a) S_{11} characteristics of packaged CPW with varying "c"



(c) S_{21} characteristics of packaged CPW with varying "c"

Figure 4.6: S-parameters of packaged CPW structures with varying "c" parameter.

4.5. Feed-Through Modification

The characteristic impedance of the packaged CPW is altered in the feed-through and capped sections due to the capacitive loading of the cap material and BCB ring. In order to remove the negative effects of this loading, which distort the matching through the CPW, a feed-through modification is necessary to minimize the unwanted reflections. The modification is realized in terms of adjusting the CPW dimensions in the feed-through and capped sections such that the 50 Ω characteristic impedance is sustained in the whole structure. Figure 4.7 shows the schematics of the feed-through and applied modifications in terms of CPW dimensions.

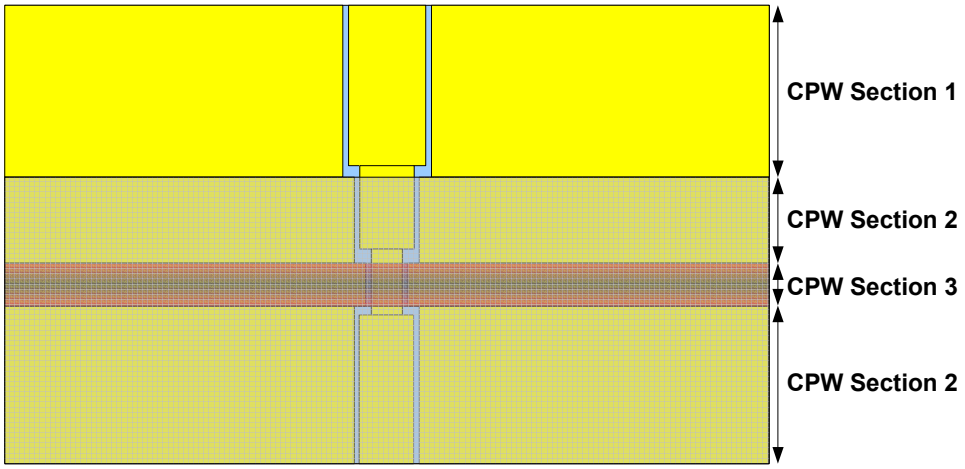


Figure 4.7: Feed-through geometry of the packaged CPW.

The CPW feed-through is divided into three sections. The first section is the bare CPW which is the input or output ports that remains outside the packaged area. The second section is shaded by the glass cap but does not contain the BCB ring. The third section contains both the BCB ring and the top cover.

While calculating the required CPW dimensions, it is assumed that there is no cavity in the cap. If there were a cavity, which is more than 50 µm, the feed-through modification would not be necessary since the loading effect becomes negligible as observed from Figure 4.6. Table 4.2 shows the CPW dimensions and the characteristic impedance of the modified and unmodified CPW sections.

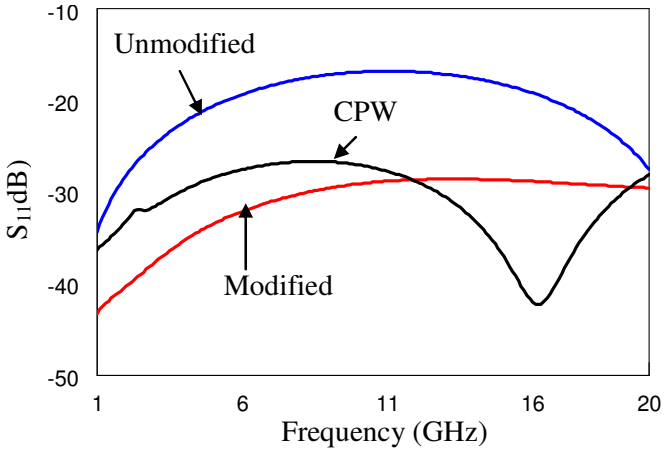
Table 4.2: CPW dimensions and corresponding Z_0 values in feed-through sections for modified and unmodified cases.

CPW Section	Unmodified G-S-G (µm)	Unmodified Z_0 (Ω)	Modified GSG (µm)	Modified Z_0 (Ω)
Section 1	20-170-20	49.83	20-170-20	49.83
Section 2	20-170-20	44.57	20-120-20	50.17
Section 3	20-170-20	41.83	20-80-20	50.05

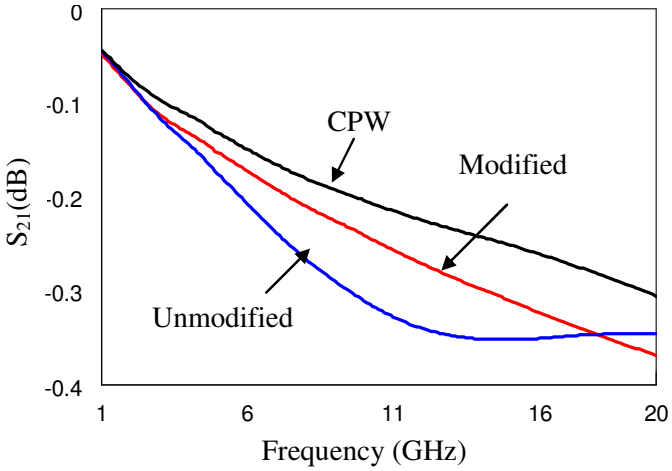
In order to see the improvement in the packaged CPW, EM simulations have been performed and the s-parameters for bare, unmodified and modified cases are compared. The simulations are performed on a structure with "t = 7 µm", "w = 100µm", "a = 3000 µm", "g= 100 µm", "h = 500 µm", "c = 0 µm". Figure 4.8 shows the ANSOFT HFSS v9.2™ simulation results in 1 – 20 GHz band.

The maximum S_{11} value for the packaged structure with the unmodified feed-through is obtained as -15 dB in the entire frequency band. However with the feed-through modified, this value goes down to -29 dB which is a tremendous improvement. The amplitude of S_{11} plot of the unmodified case nearly matches with the bare CPW characteristic and even better in some regions because the bare CPW does not have a characteristic impedance of exact 50 Ω and as seen in Table 4.2, some sections have impedance values much closer to 50 Ω. The difference in the minimum S_{21} value of modified and unmodified structures is maximum around 11

GHz which is -0.07 dB. The modified structure has lower insertion loss and its S_{21} characteristic is similar to that of a bare CPW. Minimum S_{21} value for both structures is above -0.38 dB in the complete frequency range.



(a) S_{11} comparison



(b) S_{21} comparison

Figure 4.8: S-parameter comparision of packaged CPW structures with unmodified and modified feed-throughs with respect to an unpackaged CPW structure.

4.6. Proposed Fabrication Process Steps

The fabrication process of wafer bonding with a BCB as adhesive layer depends on many parameters. The process is completely different if the BCB ring is to be applied on the process wafer or on the capping wafer, a cavity is required or not. In this section two main methods to achieve a successful bonding are explained for two cases: (1) BCB ring on process wafer without a cavity, (2) BCB ring on capping chip with cavities. Also an alternative approach for the latter case is explained.

4.6.1. BCB Ring on Process Wafer without Cavities

RF MEMS devices contain suspended, movable and fragile structures. These suspended structures will be destructed if the BCB is applied after releasing since BCB is in a liquid form before curing. In order to accomplish the BCB ring on the process wafer, the BCB ring can be constructed on the base metal and left as a bulk until the final wafer bonding stage. Since there is no cavity in the cap, it is better to have a thick BCB layer so that RF signal is not distorted by the cap. This can be achieved by using a single layer XU 3575.00 which has a thickness range 15-25 µm or a multi layer CYCLOTENE 4024-40 which has a single layer thickness range of 3-8 µm. Both of the chemicals are photo-definable and act as a negative photo-resist.

The BCB is coated on the wafer with spinner and adhesion promoter AP3000 is applied before spinning to ensure a possible bond strength improvement. After the spinning, the BCB is soft cured at around 200°C so that it keeps its bulk form during the other process steps. The BCB loses its viscousity after the soft cure and rest of the process steps so in order to accomplish a successful bonding to the cap; contact printing method can be applied after the MEMS device is released. Contact printing is a method where an auxiliary wafer with a BCB ink is used. A very thin BCB, in

the order of a few micrometers is coated on the auxiliary wafer and left uncured and not even put onto a hotplate so that it is as vicous as possible. The top surface of the BCB pattern on the substrate is then inked by pressing the auxiliary wafer to the substrate wafer with the wafer bonder. Afterwards, the wafer can be separated using a razor blade. Since the ink BCB is not cured, the wafers can be easily removed, leaving a thin BCB ink on top of the bulk BCB pattern. Figure 4.9 shows the schematics of the contact printing method.

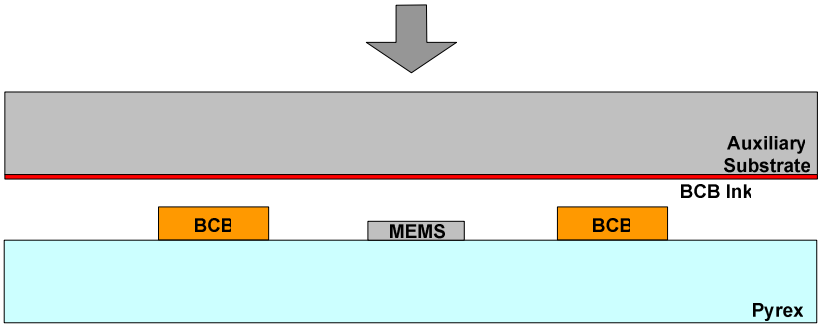
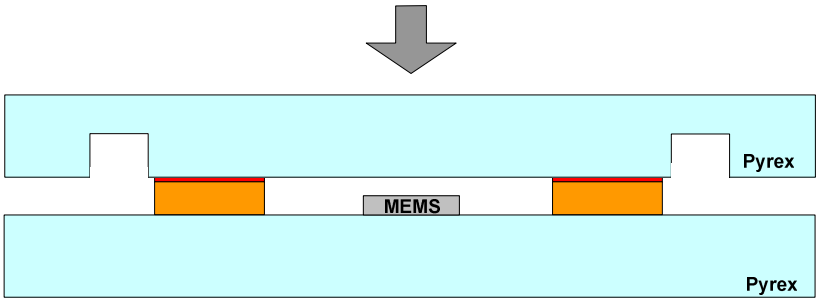


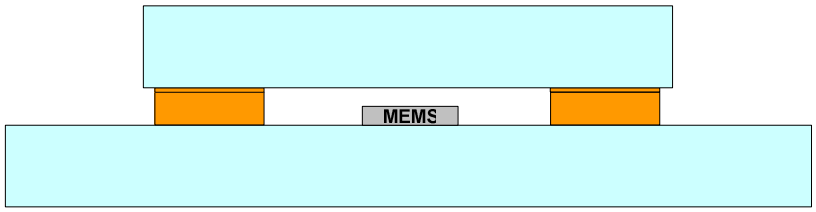
Figure 4.9: Contanct printing of the BCB ink on the bulk BCB ring.

Now that the process wafer is ready to be bonded with the capping wafer, the bonding can be accomplished by using the wafer bonder at a certain pressure and temperature. However the capping wafer shall be physically modified concerning the dicing of the wafer. The outlines of the final glass-lids can be routed on the front side of the wafer. This allows a lower vertical accuracy of the die saw when dicing the wafer after the bonding in order to separate each component. But since a thick BCB layer is used in the process, this step may well be skipped as the thickness of the layer may be larger than the vertical accuracy of the die saw. Bonding is done for about 1 hour at 250°C in an EVG wafer bonder. After the bonding, first the top wafer is diced along the outlined of the glass lid and then the bottom wafer is diced

to separate each device from the rest of the wafer. Figure 4.10 shows the schematics of the bonded and diced structures.



(a) Bonding of the cap wafer and the process wafer



(b) Dicing of the cap wafer

Figure 4.10: Process steps including bonding and dicing.

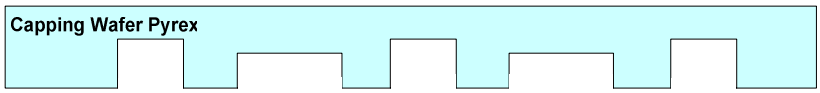
4.6.2. BCB Ring on Capping Wafer with Cavities

Having the bulk BCB in the process wafer has viscousity problems as explained in the previous case, so in order to get rid of these problems, the BCB ring can be patterned on the capping wafer. The process steps are outlined in Figure 4.11. The bonding process is done with two wafers; one is the fully processed MEMS substrate including the release and the other is the cap wafer including the required cavities and gaps. The cavities in the glass wafer can be formed by etching in the buffered

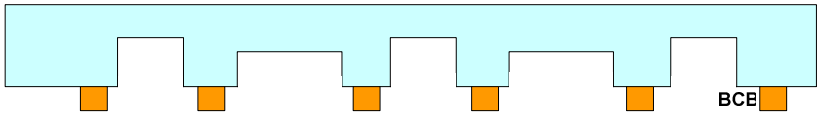
HF (50%) solution. The unetched sections of the glass can be protected with a double layer of titanium-gold stack. Extra gaps can be optionally etched in order to form openings for the input and output ports of the RF MEMS devices. The glass etching requires a two-step lithography and etching, in which the cavities are etched first, followed by the etching of the gaps sections. The gap depth can be in the order of a few 100 μm and the cavity depth can be around 50 μm so that the RF signal remains unchanged.

After etching the cavities and the gaps, BCB layer is spin coated of the cap wafer and using the lithography steps, it is patterned. It is important to notice that in this method there may remain some residual BCB in the cavities and gaps in order not to observe undercuts in the BCB ring sections but they will not affect the device performances much since they will be located around 50 μm above the device.

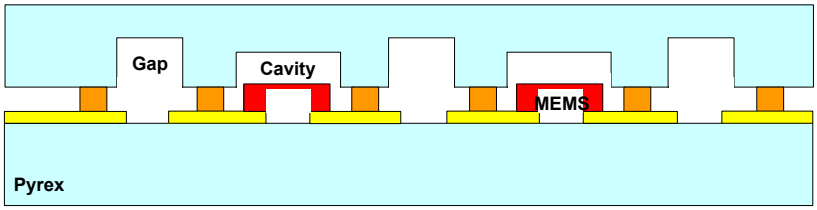
After this step, capping wafer is aligned and bonded to the process wafer using EVG wafer bonder at a certain pressure and temperature which are to be optimized. Then the cap wafer is grinded, in other words thinned, until it reaches to the gap level. Since METUMET facility does not have a grinder, this process may be done in another facility. The last step is the dicing of the process wafer through the gap openings.



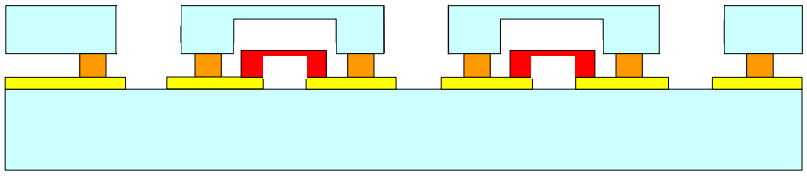
(a) Etching of the cap wafer to create cavities and gaps



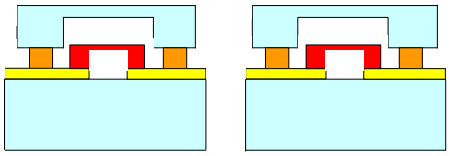
(b) Patterning the BCB rings



(c) Bonding of the cap wafer and process wafer



(d) Dicing of the cap wafer



(e) Dicing of the process wafer

Figure 4.11: Process flow of the BCB on the cap wafer.

4.6.3. Alternative Process for BCB Ring on Capping Wafer with Cavities

In the previous process flow, there is a problem with removing the BCB layer off the cavities. In order to solve this problem, BCB can be coated before the glass etching. The first layer to be coated and patterned on the glass cap wafer is polysilicon. This layer protects the base of the BCB ring during the glass etching. BCB is then coated on polysilicon and patterned with lithography steps including a soft cure at 180°C. Then AZ 1512 is deposited on BCB and patterned as a protective layer during glass etching. Then the bare glass regions on the wafer are etched with BHF (50%) solution until a desired depth is reached. However this process allows only cavities to be etched, excluding the gap sections but the routing method used in the first process can be applied for this case. When the glass is etched, AZ 1512 is removed from the wafer and the wafer-to-wafer bonding can be realized. Then the wafer is diced from the routed boundary and capped structures are obtained.

4.7. Trial Process

The process optimization for wafer-to-wafer bonding using BCB 4024 adhesive layer is initiated in METUMET Clean Room Facilites. During the optimization period, tests on many parameters like BCB coating conditions, exposure time and intensity, bonding temperature and pressure have begun. The experimental process is realized on 500 μm silicon wafers that serve both as the capping and base wafers. The reason why silicon is preferred rather than glass is that a silicon wafer costs less than a glass wafer. Also the BCB adhesion is more or less the same for both glass and silicon.

4.7.1. Process Flow

The process begins with the removal of any organic resiudes from the surface of the silicon wafers with O_2 plasma etching. This ensures non-contaminated surface for the BCB to be coated uniformly. After this step, the wafers are dehydrated in the oven at 120 °C for 30 minutes in order to remove the moisture on the wafers, consequently establishing a cleaner surface during BCB spinning. The next step is the BCB spin coating on the cap wafer. Before the BCB coating AP 3000 adhesion promoter is applied on the wafer to improve the adhesion of the silicon surface. Right after the AP coating, BCB is spin coated with a thickness defined by the angular speed of the spinning tray. When the wafer is completely coated with BCB, edge bead removal is done on the edges of the wafer. Also the BCB drops on the backside of the wafer that splash during the spinning are removed using a Q-Tip soaked with T 1100 chemical. These steps are done in order to prevent contamination in the wafer bonder. Table 4.3 gives the process recipe during the BCB coating.

The process up to this point is carried on with two cap wafers. Wafer 1 has a single layer BCB and Wafer 2 has a double layer BCB. The aim of processing the double layer BCB wafer is to see the thickness limit that can be acquired in multi-layer process. Also the sticktion of the second layer BCB on the first layer BCB is examined.

Table 4.3: Process recipe for BCB coating.

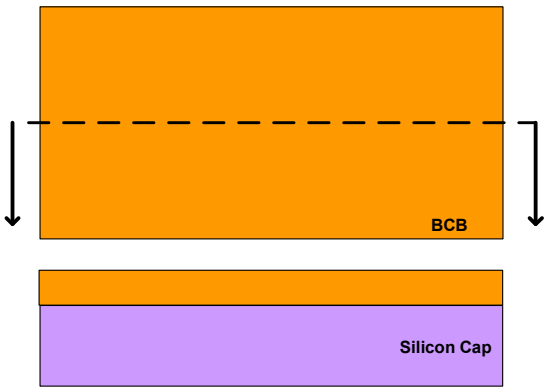
Process	**Wafer1**	**Wafer2**
AP 3000 Coating	2000rpm for 30 secs	2000rpm for 30 secs
Softbake on Hotplate	80°C for 90 secs	80°C for 90 secs
BCB 4024 Coating	1500rpm for 30 secs	1500rpm for 30 secs **X2**
Softbake on Hotplate	80°C for 90 secs	80°C for 90 secs **X2**
Edge Bead Removal	1000 rpm for 30 secs	1000 rpm for 30 secs

A previously prepared mask for a different MEMS application is used in the BCB patterning of the trial wafers since it contains necessary square ring patterns. The side length of the squares is 5000 µm and the width of the ring sections is 100 µm. The alignment and exposure is done using EVG Aligner. The exposure is applied for 15 seconds at 18 mW/cm^2 UV intensity. Exposed wafers are developed with DS 3000 developer. The double coated BCB is disintegrated in the developer. The reason for this defect may be the improper adhesion of the second layer BCB on the base BCB. However the BCB thickness is measured from the remaining BCB masses on the wafer. The achieved thicknesses for both wafers and development conditions are given in Table 4.4.

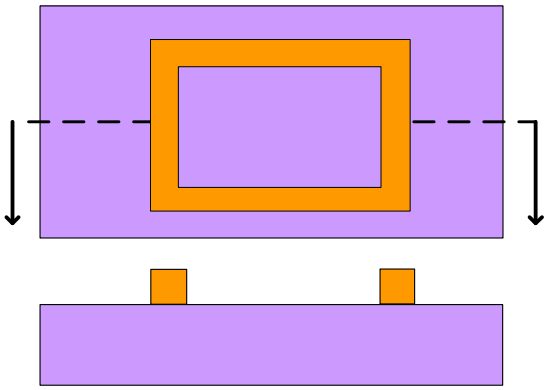
Table 4.4: Process recipe for BCB development stage.

Process	**Wafer 1**	**Wafer 2**
DS 3000 Develop	2 min 30 sec at 33°C	6 min at 33°C
DS 3000 Develop	2 min at room temp.	Defect
IPA Rinse	3 min	Defect
Measured Thickness	11.3 µm	19 µm

Now that the BCB patterning is complete, the single BCB layered wafer and a blank silicon wafer is bonded in the EVG Wafer Bonder at 2500 mBar and 250°C for 70 minutes. During the curing a strong bond is established between the silicon and BCB. Figure 4.12 and Figure 4.13 show the basic steps of the complete process. The results of the BCB adhesion are investigated in the next section.



(a) BCB coating



(b) BCB patterning

Figure 4.12 (a) – (b): Process steps up to BCB patterning.

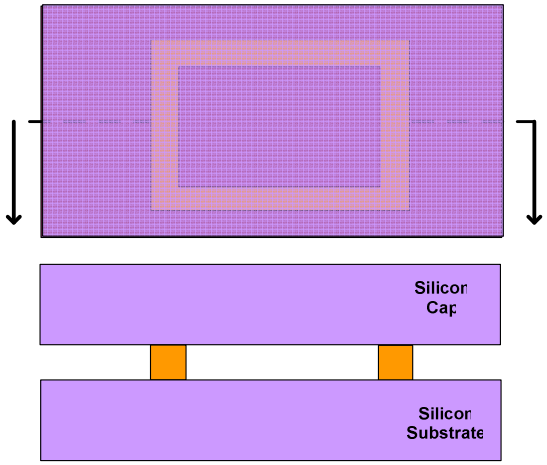


Figure 4.13: Wafer bonding of the capping chip.

4.7.2. Bond Interface Investigation

Right after the cooling period of the bonded wafers, in macro sense, it is observed that a satisfactory bonding between the two substrates is achieved. However when the packaged wafer is investigated under the microscope, adhesions of various qualities are examined.

Figure 4.14 is a microscope shot of a successfully bonded BCB ring. On the bonding interface, no sign of cracking or unsticktion is present. However in concave corners, the BCB slightly flows out of the shapes of the BCB stamp into the cavity, resulting in rounded ring corners. However this effect can be pre-considered and since the BCB ring, practically, will be placed far enough from the suspended structures, this corner rounding will not probably distort the characteristics of the MEMS structure. After the bonding, the dimensions of the BCB extend from the ring width and shrink from the ring thickness as the BCB is still viscous in the beginning of the bonding phase. This effect shall be pre-considered again at the design stage of the packaged structures

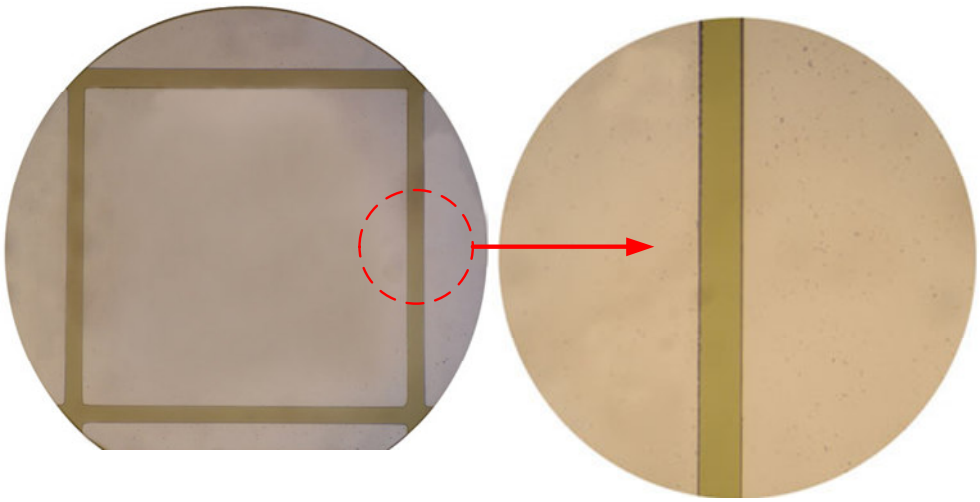


Figure 4.14: Microscope shot of a successfully bonded BCB ring

Figure 4.15 is a microscope shot of a partially bonded BCB ring where the patterns in the zoomed view correspond to the unbonded regions. The reason for this improper bonding may the insufficient contact force or contact time during the bonding. In Figure 4.16, the bonding is merely accomplished. The light colored inner central ring is the unbonded region which is surrounded by a darker ring where the bonding is achieved.

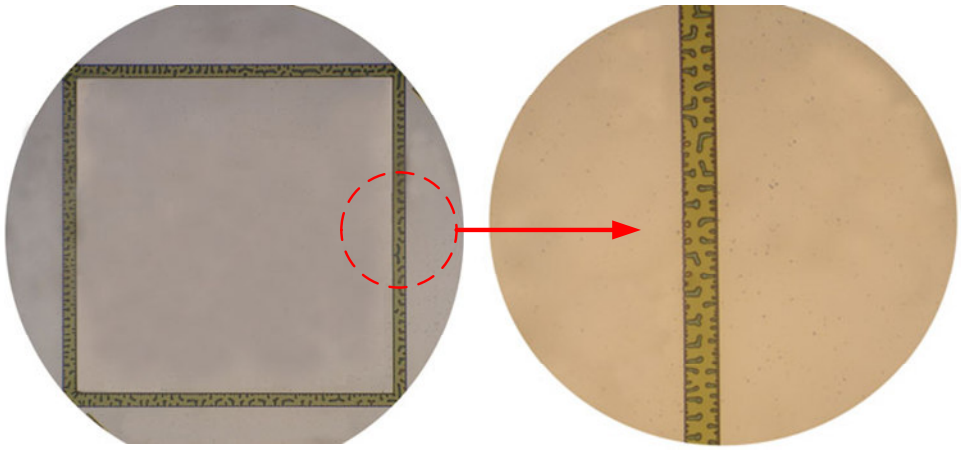


Figure 4.15: Microscope shot of a partially bonded BCB ring.

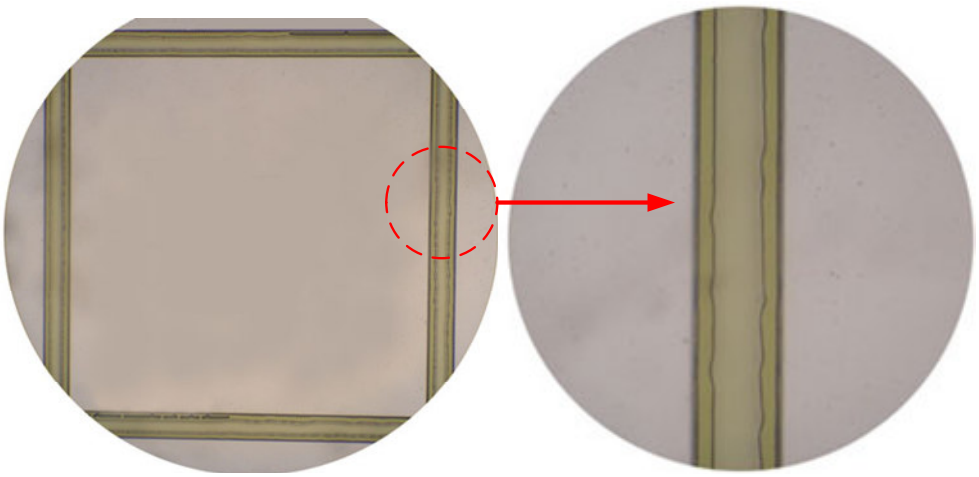


Figure 4.16: Microscope shot of a poorly bonded BCB ring.

CHAPTER V

CONCLUSION AND FUTURE WORK

The study presented in this thesis includes literature search, design, production, and measurement of different topics, including, CPW-microstrip transitions, planar spiral inductors, metal-insulator-metal capacitors, a band-pass filter, a low pass filter, as well as RF MEMS packaging using BCB as adhesive layer. CPW-to microstrip transitions are realized by minimizing the reflection coefficient in terms of characteristic impedance matching. Lumped circuit components, i.e. capacitors and inductors, are constructed using the circuit models and equations obtained through the literature search. A band-pass filter and a low-pass filter are designed as an application using the lumped circuit components. BCB packaging studies in METU-MET cleanroom facility are initiated. All devices of are fabricated monolithically using the surface micromachining technology. The measurements are performed with Network Station in METU Millimeter-wave Laboratory.

The up to date achievements in the research topics can be summarized as follows:

1. A parametric analysis of direct type CPW-microstrip transition is performed. The structures are analyzed with electromagnetic simulators. At low frequencies, a very satisfactory transition with a compact transition size is achieved. The structures with different transition dimensions are fabricated and measured.

2. A parametric analysis of linear type CPW-microstrip transition is performed. The effect of transition length and angle is observed. Structures with different transition dimensions are designed, fabricated and measured. A parametric analysis of staircase type CPW-microstrip transition is performed. Very low loss transitions are obtained in a wide frequency band. Structures with various steps are designed, fabricated and measured.
3. A parametric analysis of polynomial type CPW-microstrip transition is performed. Very low loss transitions are observed in a wide frequency band. Two different types of the same model are designed, measured and fabricated.
4. A library of surface micromachined planar square spiral inductors with various inductance values is created. The inductor designs are initiated with parameter extraction using Modified Wheeler formulations. The S-parameter characteristics of the simulated structures are fitted to S-parameter characteristics of the spiral inductor circuit model. The inductance values are obtained from the circuit model and they are compared with the values obtained from the formulations. The structures are fabricated and measured.
5. A library of surface micromachined metal-insulator-metal capacitors with various capacitance values is created. The circuit model and parallel plate capacitance formulation are used in the design of the structures. The extracted capacitance values from the circuit model and formulation are compared.
6. A low-pass filter structure structure is designed using the lumped inductors and capacitors of the previously created element libraries. The effects of discontinuities in the junctions between each element are observed. The structure is simulated element-wise and the final topology is defined with the introduction of interconnecting transmission lines and Tee junctions including air bridges.
7. A band-pass filter is designed using the lumped inductors and capacitors of the previously created element libraries. The structure is initially simulated

element-wise and the final simulation is performed with the introduction of discontinuities from the junctions and interconnecting transmission lines.

8. The adhesive behaviour of BCB for packaging was investigated. The design parameters of the packaging structure were defined and the effect of each dimension change in the capping chip was observed with parametric EM simulations. A bonded sample was fabricated and the bonding quality of the sample was observed.

Each of the mentioned topics can be improved in many ways:

1. In the transition structures, the connection between the backside metallization and CPW grounds was supplied via silver epoxy. This step can be omitted when a coupling between the top ground planes and bottom ground plane is formed. New designs including coupled grounds shall be investigated.
2. The quality factor of the spiral inductors can be improved by avoiding the substrate loss. This can be achieved by using silicon thin film as the base for the inductors or designing suspended inductors on glass wafer.
3. Both or one of the elements (capacitor, inductor, or both) used in the filter structures can be made tunable so that the filter structures become tunable themselves. The MIM capacitors can be substituted with RF MEMS shunt switches. The inductors can be made tunable by changing the total line length or separation of the windings.

4. The BCB process is subject to optimization and improvement. The cap material can be substituted with high resistivity silicon if the losses introduced by the cap are found too high during the future measurements of packaged RF MEMS devices.

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