HIGH PERFORMANCE READOUT ELECTRONICS FOR UNCOOLED INFRARED DETECTOR ARRAYS

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Ömer Özgür Yıldırım

ABSTRACT

HIGH PERFORMANCE READOUT ELECTRONICS FOR UNCOOLED INFRARED DETECTOR ARRAYS

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This thesis reports the development of high performance readout electronics for resistive microbolometer detector arrays that are used for uncooled infrared imaging. Three different readout chips are designed and fabricated by using a standard 0.6 µm CMOS process. Fabricated chips include a conventional capacitive transimpedance amplifier (CTIA) type readout circuit, a novel readout circuit with dynamic resistance nonuniformity compensation capability, and a new improved version of the CTIA circuit.

The fabricated CTIA type readout circuit uses two digital-to-analog converters (DACs) with multiple analog buses which compensate the resistance nonuniformity by adjusting the bias currents of detector and reference resistors. Compensated detector current is integrated by a switched capacitor integrator with offset cancellation capability followed by a sample-and-hold circuit. The measured

detector referred current noise is 47.2 pA in an electrical bandwidth of 2.6 KHz, corresponding to an expected SNR of 530.

The dynamic nonuniformity compensation circuit uses a feedback structure that dynamically changes the bias currents of the reference and detector resistors. A special feature of the circuit is that it provides continuous compensation for the detector and reference resistances due to temperature changes over time. Test results of the fabricated circuit show that the circuit reduces the offset current due to resistance nonuniformity 42.5 times. However, the calculated detector referred current noise is 360 pA, which limits the circuit SNR to 70.

The improved CTIA type readout circuit introduces a new detector biasing method by using an additional auxiliary biasing transistor for better current controllability. The improved readout circuit alleviates the need for high resolution compensation DACs, which drastically decreases the circuit area. The circuit occupies an area of one seventh of the first design. According to test results, the current compensation ratio is 170, and the detector referred current noise is 48.6 pA in a 2.6 KHz bandwidth.

Keywords: Uncooled infrared readout electronics, readout circuits for resistive microbolometers, nonuniformity compensation.

ÖZ

SOĞUTMASIZ KIZIL ÖTESİ DETEKTÖR DİZİNLERİ İÇİN YÜKSEK PERFORMANSLI OKUMA ELEKTRONİĞİ

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Bu tezde soğutmalı kızıl ötesi görüntülemede kullanılan direnç tipi mikrobolometre detektör dizinleri için yüksek performanslı okuma elektroniğinin geliştirilmesi anlatılmaktadır. Üç farklı okuma yongası tasarlanmış ve bu yongalar standart 0.6 µm CMOS üretim sürecinde ürettirilmiştir. Üretilen yongalar kapasitif transempedans yükseltici (KTEY) türü okuma devresini, direnç eşdeğersizliğini telafi etme özelliğine sahip yeni bir okuma devresini ve KTEY türü devrenin geliştirilmiş yeni bir modelini içermektedir.

Üretilen KTEY türü okuma devresi, iki adet detektör ve referans dirençlerinin eğimleme akımlarını ayarlayarak direnç eşdeğersizliğini telafi eden çoklu analog çıkışı olan sayısal-analog çevirici (SAÇ) devresi kullanmaktadır. Telafi edilmiş detektör akımı ise bir örnekle-ve-tut devresinin izlediği anahtarlamalı kapasitör entegratörü tarafından integre edilmektedir. Ölçülen dedektör akımı gürültüsü

2.6 KHz elektriksel band aralığında 47.2 pA olup beklenen işaret gürültü oranı (İGO) 530'dur.

Dinamik eşdeğersizlik telafi etme devresi, detektör ve referans dirençlerinin eğimleme akımlarını dinamik olarak değiştiren bir geri besleme devresi kullanır. Devrenin özel bir tarafı ise detektör ve referans dirençlerinin sıcaklık değişikliği yüzünden zamanla değişebilen direnç değerlerini devamlı olarak telafi edebilmesidir. Üretilen yonganın test sonuçları, devrenin direnç eşdeğersizliği yüzünden oluşan ofset akımını 42.5'te birine düşürdüğünü gösterir. Fakat hesaplanan detektör akımı gürültüsü 360 pA olup bu gürültü devrenin İGO'sunu 70 ile sınırlandırır.

Geliştirilmiş KTEY türü okuma devresi, akımı daha iyi kontrol edebilmek için fazladan yardımcı eğimleme transistörü kullanan yeni bir detektör eğimleme yöntemi sunmaktadır. Geliştirilmiş okuma devresi, yüksek çözünürlükteki SAÇ'lere olan gereksinimi azaltarak devrenin alanını önemli ölçüde azaltmaktadır. Bu devre ilk tasarımın yedide biri bir alanı kaplar. Test sonuçlarına göre akım telafi etme oranı 170 olup dedektör akımı gürültüsü 2.6 KHz band aralığında 48.6 pA'dır.

Anahtar sözcükler: Soğutmasız kızılötesi okuma elektroniği, direnç tipi mikrobolometreler için okuma devreleri, eşdeğersizlik telafi etme.

To The Greatest Person in the World

My Mother Mürüvvet Yıldırım

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INTRODUCTION

The light human eye sees is really a very small portion of the electromagnetic spectrum. In addition to visible light, the electromagnetic spectrum contains gamma rays, X-rays, ultraviolet rays, infrared rays, microwaves, and radio waves. While gamma rays have the shortest wavelength (less than a few picometers) and the highest energy, radio waves have the largest wavelength (up to hundreds of kilometers) and the lowest energy.

Infrared radiation has wavelengths between approximately 0.7 μm and 1000 μm, i.e., longer than those of visible light, but shorter than those of radio waves. Any material above the absolute zero (0 Kelvin) radiates in the infrared range of the electromagnetic spectrum. Therefore, any object can be seen by sensing the infrared radiation. Infrared imaging systems having infrared detectors are used in order to sense the infrared radiation.

Infrared imaging systems have the ability to provide image under zero illumination conditions and can see through most smoke and obscurants [1]. Infrared imaging is being developed for a wide range of applications including military [2-4] and civilian applications such as industrial control [5, 6], aerospace applications [7, 8], and medical imaging [9, 10].

Infrared detectors are generally designed to a specific wavelength range in the infrared spectrum, that consists of four regions, namely short-wave infrared (SWIR),

mid-wave infrared (MWIR), long-wave infrared (LWIR), and far infrared (FIR) which have wavelengths of 1-3 μm, 3-6 μm, 6-16 μm, and more than 16 μm, respectively [11]. MWIR and LWIR are the most common regions for infrared detection because of the high atmospheric transmittance rate in these regions [12].

Detection mechanisms of infrared radiation fall into three categories, photon detection, wave interaction detection, and thermal detection. Table 1.1 gives the classes of infrared detectors [13].

Table 1.1: Classes of infrared detectors [13].

Photon	Wave Interaction	Thermal
Photoconductivity	Optical heterodyne	Bolometer
Photovoltaic	Photon-assisted tunneling	Thermocouple/thermopile
Photoelectromagnetic	Optical parametric	Pyroelectric
Phototransistor	Schottky barrier mixer	Golay cell microphone
Photon drag	Metal-oxide-metal	Absorption edge
Photoemissive		Pyromegnetic
Quantum counter		Liquid crystal
		Thermomechanical

The most common infrared detection mechanisms are photon and thermal detection, which depend on the intensity of the incident electromagnetic radiation. On the other hand, wave interaction effects depend on the magnitude of the incident electric field vector, and none of efforts made to apply this technology to the detection of infrared radiation has proven to be of any practical value [13].

In photon detectors, absorbed infrared photons generate free hole-electron pairs. These free charges are collected by applying an electric field, thus they form an infrared induced current. Since, at room temperature, the number of thermally

generated hole-electron pairs are much more than that of infrared induced hole-electron pairs, photon detectors must be cooled down to cryogenic temperatures such as 77 K or below in order to reduce the number of thermally generated hole-electron pairs. Therefore, photon detectors are also called cooled detectors. Photon detectors have better performance than thermal detectors; however, in order to operate in cryogenic temperatures, they need special coolers which are big, heavy, and expensive and dissipate high power, limiting the application areas of photon detectors. These detectors find application areas where performance is the primary issue, such as in expensive military devices and in special medical instruments. The most known fabricated cooled infrared detectors are Indium Antimonide (InSb) [14, 15], Mercury Cadmium Telluride (HgCdTe) [16-18], and Quantum Well Infrared Photodetectors (QWIPs) [19-22].

In thermal detectors, absorbed infrared radiation increases the detector temperature causing a change in one of the measurable electrical parameters. Different from photon detectors, thermal detectors can operate at room temperature and do not need to be cooled down to cryogenic temperatures. For this reason, they are also called uncooled infrared detectors. In spite of their lower performance, uncooled infrared detectors have a wide application area due to their advantages such as low cost, low power dissipation, and small size, making them suitable for large volume commercial applications.

The most common thermal detectors are bolometers, thermoelectric detectors, and pyroelectric detectors. Thermoelectric detectors, which are also called thermopiles, are implemented using series connected thermocouples. Temperature difference between the hot and cold points of thermocouples generates a voltage depending on the Seebeck coefficient of the materials used [23]. Main advantages of thermopiles are their monolithic fabrication and their operation without choppers and temperature stabilizers [24]. Nonetheless, their low responsibility and large pixel size limit their application areas. Pyroelectric detectors which use the pyroelectric effect, i.e., rapid temperature change in some materials displays transient electric polarization [13]. However, in order to measure the infrared radiation, a chopper must be used for

modulating the infrared radiation. Moreover, pyroelectric detectors are operated just below their Curie temperatures which are generally very high temperatures; to illustrate, Curie temperatures of iron and nickel are 1043 Kelvin and 627 Kelvin, respectively. The need for chopper and temperature stabilizers is the main disadvantage of pyroelectric detectors. There are large format pyroelectric imagers reported with 320 x 240 array size and an NETD value of 60 mK [25].

Bolometers overcome most of drawbacks of other thermal infrared imaging systems such as the need for thermocoolers or thermoheaters and large size detectors. Therefore, it is possible to fabricate low power, large array infrared detectors with this technology. Worldwide effort is still continuing to implement very large format, high performance, and low cost microbolometers. Microbolometers together with their integrated readout circuitry fabricated by using MEMS and standard CMOS technologies are very low cost and proper to be improved by designing special readout circuitries. This thesis reports the development of such high performance readout electronics for resistive uncooled microbolometer detector arrays.

The rest of the chapter is organized as follows: Section 1.1 explains operating principles of microbolometers and their development history. Section 1.2 describes readout electronics of microbolometers, and Section 1.3 examines the performance of resistive readout electronics. Finally, Section 1.4 gives the research objectives and thesis organization.

1.1. Microbolometers

Microbolometers measure the change in an electrical parameter which depends on the detector temperature related with the amount of incident infrared power. The most important types of microbolometers are diode and resistive types. Also capacitive [26] and transistor [27] type microbolometers have been tried. In diode type microbolometers, the electrical parameter is the forward diode voltage, and the

temperature rise due to absorbed infrared power decreases the diode forward voltage. In resistive type microbolometers, the electrical parameter is the resistance, and the temperature rise due to absorbed infrared power causes a change in the resistance depending on the temperature coefficient of resistance (TCR) of the resistive material.

Figure 1.1 shows a simplified perspective view of a microbolometer pixel structure [28]. Temperature of the suspended bridge rises due to the absorbed infrared power. The reflector directs infrared radiation on the suspended bridge which is thermally isolated from the substrate. The rise in the detector temperature causes a change in an electrical parameter of the detector, which is sensed by a the electronic circuitry.

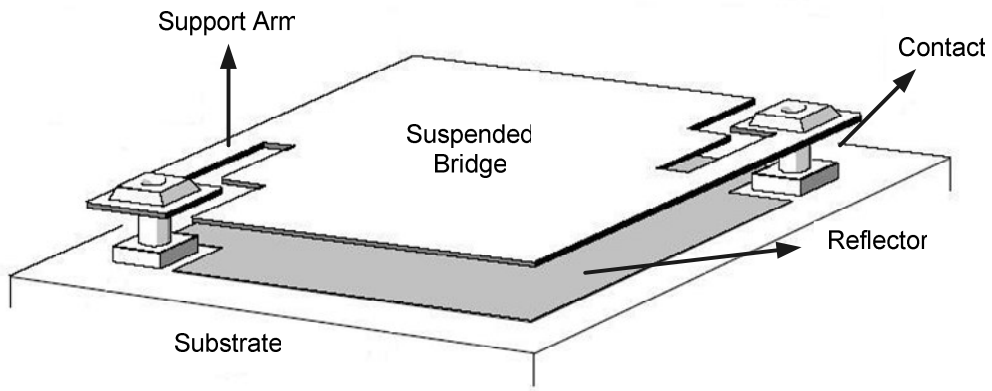
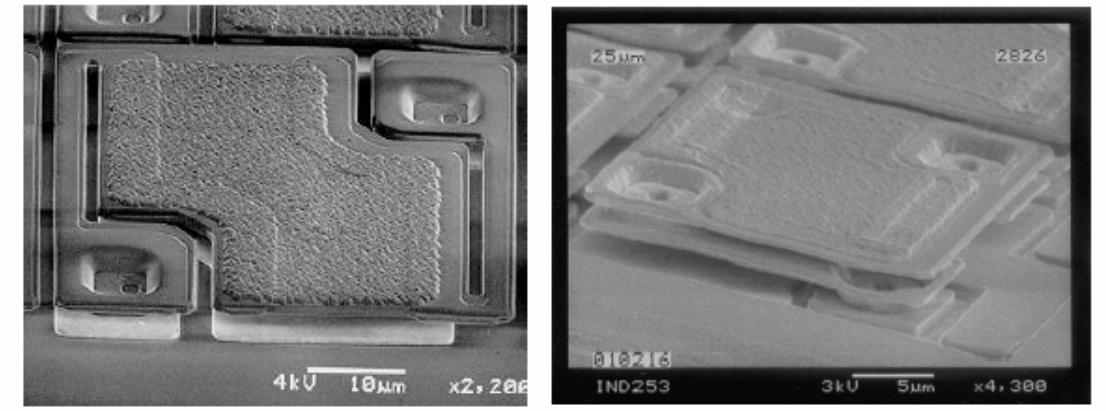


Figure 1.1: Simplified perspective view of a microbolometer pixel structure [28].

Microbolometer bridges can be implemented on CMOS processed wafers using temperature sensitive layers with very small thickness, very small mass, and very good thermal isolation by using surface micromachining. This method allows readout circuitry to be realized under the bridges resulting in high fill factor. Figure 1.2 (a) shows SEM picture of a surface micromachined microbolometer pixel with 50 µm pixel pitch; and Figure 1.2 (b) shows a high fill factor, 25 µm surface micromachined microbolometer pixel with supporting legs below the platform [29].



(a) (b)

Figure 1.2: SEM pictures of the VO_2 surface micromachined microbolometer detectors with (a) 50 µm pixels and (b) high fill factor, 25 µm pixels [29].

There are many different materials used in surface micro-machined microbolometers such as amorphous silicon (a-Si) [30, 31], vanadium oxide (VO_x) [32, 33], polycrystalline silicon–germanium (poly SiGe) [34], and Yttrium Barium Copper Oxide (YBaCuO) [35-37]. Bulk micromachining is another approach to fabricate uncooled infrared microbolometers in which the silicon substrate is removed by etching to have suspended bridges [38-40].

Although the fabrication of the first thermal infrared detector was in 1880 [41], the main developments have occurred after 1980's as the microfabrication techniques advanced. In those years, a group of researchers under the direction of R. Andrew Wood at the Honeywell Technology Center developed an uncooled microbolometer with 336 × 240 array format and 50 µm x 50 µm pixel size by using vanadium oxide (VO_x) resistors as the active material [42].

The research on uncooled infrared detectors was conducted under classified projects until 1992 [13]. In 1992, information on uncooled thermal imaging has been made available to the public; hence, companies such as Raytheon, DRS, BAE Systems, Mitsubishi, INO, ULIS, Indigo, NEC, and LETI LIR started fabricating uncooled

infrared imaging systems. Moreover, there are also many research institutions working on uncooled microbolometers such as IMEC in Belgium, ETH in Switzerland, The University of Texas at Arlington and The University of Michigan in the U.S., KAIST in Korea, and METU in Turkey.

1.2. Readout Electronics of Microbolometers

Absorbed infrared power changes one of the electrical parameters of the microbolometer, which is measured by the readout integrated circuit (ROIC) that is integrated in the silicon substrate [43, 44]. The readout circuit includes an amplification circuit for the detector signal before any signal processing step as well as a pixel addressing circuitry [45]. Pixel addressing circuitries are generally similar for each type of microbolometers; however, amplification structures vary for different type detectors.

As mentioned in Section 1.1, there are two common types of microbolometers namely diode and resistive types. Diode type microbolometer readout electronics have been previously implemented in the frame work of three theses at METU [45-47]. This thesis focuses on readout electronics of resistive microbolometers, especially the amplification part of the readout electronics. Microbolometer preamplifiers in the literature will be explained in next sections.

1.2.1. Readout Electronics for Diode Type Microbolometers

Diode type microbolometers measure the change in the diode voltage or in the diode current due to temperature rise resulted from infrared radiation, depending on the detector bias type. Figure 1.3 shows simple readout circuits of diode type microbolometers (a) for current bias, and (b) for voltage bias cases. In the current

bias case, diode forward voltage changes with temperature. In the same manner, diode forward current changes with temperature under constant voltage bias.

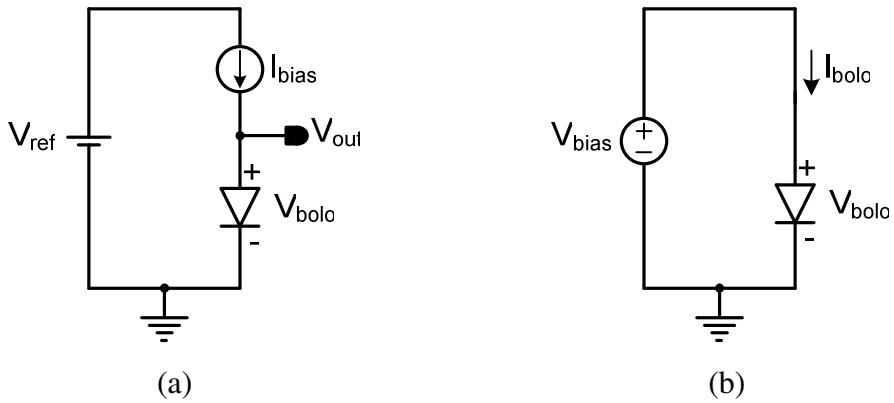


Figure 1.3: Simple readout circuits for diode type microbolometers: (a) with constant current bias and (b) with constant voltage bias.

In the interested temperature range, these changes in diode electrical parameters are almost linear. To illustrate, the diode forward voltage under a constant current bias is given as

$$V_D = V_{D0} + \alpha_D \Delta T \tag{1.1}$$

where, V_{D0} is the diode forward voltage at a reference temperature, α_D is the temperature coefficient of the diode forward voltage, and ΔT is the temperature change due to the absorbed infrared power. Hence, by measuring the diode forward voltage, the amount of infrared radiation is sensed.

In the literature, there are also more advanced readout circuits for diode type microbolometers. Figure 1.4 shows such a circuit used in previous designs at METU [45, 47]. In this circuit, in addition to the detector diode, a reference diode is used in order to cancel process variations and temperature effects. A low noise

transconductance amplifier converts the voltage output into current, which is going to be integrated by the switched capacitor integrator circuit. A current source removes the undesired offset current of the transconductance output current. The switched capacitor integrator limits the electrical bandwidth of the circuit for low noise operations, which is explained in detail in Chapter II.

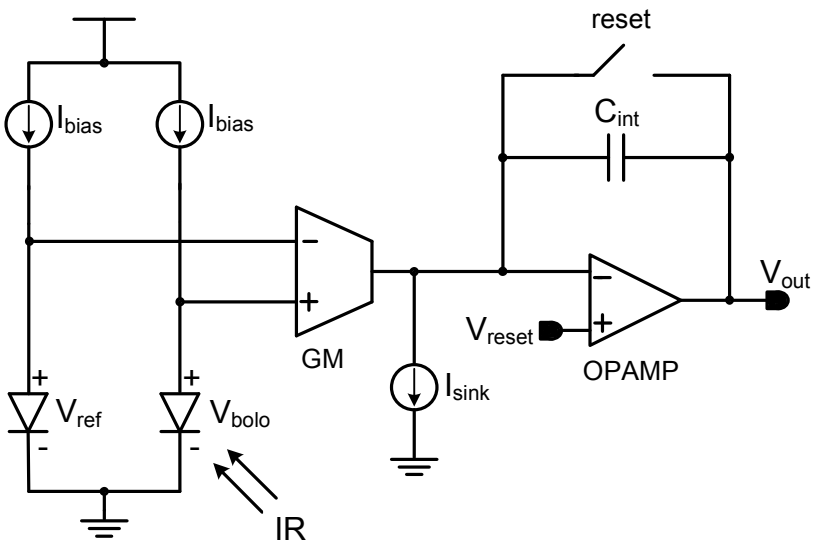


Figure 1.4: Simplified schematic of a preamplifier circuit for diode type microbolometers [45].

It is also possible to use multiple diodes in order to obtain better infrared responses. There are successful implementations of microbolometers with multiple series diodes in the literature [48, 49]. In the next section, readout electronics for resistive microbolometers will be explained.

1.2.2. Readout Electronics for Resistive Microbolometers

Temperature of a microbolometer rises due to absorbed infrared power, causing a change in the microbolometer resistance. The change in the microbolometer resistance value depends on the temperature coefficient of resistance (TCR) of the resistive material that is used on the microbolometer. Microbolometer resistance is given as

$$R = R_0 + R_0 \alpha_R \Delta T \tag{1.2}$$

where, R_0 is the resistance value at a reference temperature, α_R is the temperature coefficient of resistance, and ΔT is the temperature change due to absorbed infrared power. The microbolometer resistance is measured by the readout circuit. Figure **1.5** shows simple readout circuits for resistive microbolometers (a) for current bias where voltage output is read, and (b) for voltage bias where current output read cases.

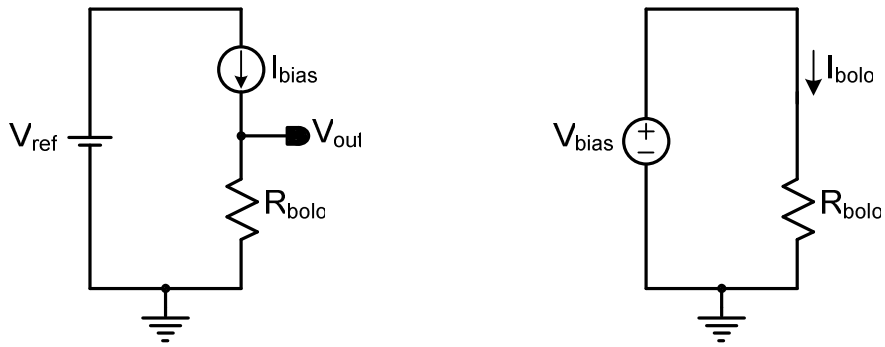


Figure 1.5: Simple readout circuits for resistive microbolometers: (a) with constant current bias and (b) with constant voltage bias.

There are a number of preamplifiers for resistive microbolometers. The most important preamplifiers are the Wheatstone bridge differential amplifier [50], the bolometer current direct injection amplifier [51], and the capacitive transimpedance amplifier [44, 52]. In the former amplifier, the detector voltage is converted to current by a transconductance stage, and then the current is integrated; however, in other amplifiers, the detector output current is directly integrated through the preamplifier.

1.2.2.1. Wheatstone Bridge Differential Amplifier

Figure 1.6 gives the schematic of the Wheatstone bridge differential amplifier. This amplifier has a Wheatstone bridge bias circuitry which is connected to a trans-conductance difference amplifier followed by a switched capacitor integrator. Reference resistors are used in order to cancel process variations and temperature effects like self heating.

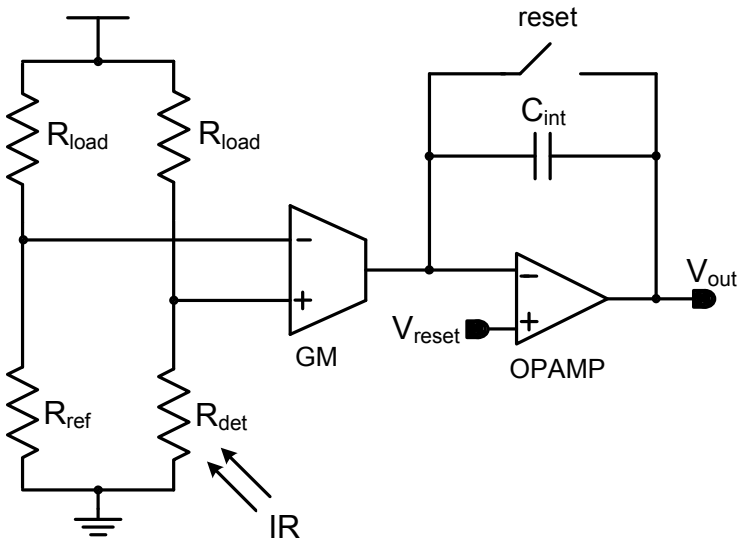


Figure 1.6: Schematic of the Wheatstone bridge differential amplifier [50].

The noise of the biasing circuit and transconductance amplifier are very critical in Wheatstone bridge differential amplifier. In order to decrease the voltage noise of the biasing circuit small resistors should be selected; however, small resistors cause high power dissipation and excessive self heating of suspended structures. Moreover, since input referred noise of the transconductance amplifier is directly seen on the detector, the amplifier's noise should be very low and preferable much smaller than noise of the biasing circuit. Nonetheless, low noise transconductance amplifiers are limited to the maximum possible area of the differential input stage transistors. Furthermore, there would be an offset current at the output of the transconductance amplifier due to the mismatched resistors of the biasing circuit and due to the mismatched input stage transistors of the differential transconductance amplifier. This undesired offset current decreases the dynamic range of the switched capacitor integrator, but it can be removed by adding a controllable current sink at the output of the transconductance amplifier.

1.2.2.2. Bolometer Current Direct Injection Amplifier

Figure 1.7 shows the schematic of the bolometer current direct injection amplifier [51]. Detector and reference resistors are under constant voltage bias, and the detector current is integrated with a switched capacitor circuit. Bipolar technology provides almost constant voltage bias on resistors with a low current noise. The reference resistor not only cancels process variations and temperature effects like self heating, but also removes the DC part in the detector current to be integrated. Although this circuit is very simple and allows very low noise current integration, i.e., the total noise is almost due to the detector and reference resistors [51], nonzero impedance of the integration capacitor seen from the collectors of the bipolar transistors creates problems. At the beginning of the signal integration, the capacitor behaves like zero impedance node and starts charging linearly. However, as it charges increasing capacitor voltage prevents the linear integration of the detector current because the impedance of the capacitor becomes comparable to the output resistance at the collectors of the bipolar transistors. To overcome this problem,

large integration capacitors can be used or integration time can be decreased but both degrade the gain and sensitivity of the amplifier as well as large capacitors occupy a large area in ROIC. Another method is to increase the output impedance of the bias circuitry which is proportional to the bolometer resistance and the forward gain of bipolar transistors. However, increasing bolometer resistance also degrades the gain and sensitivity while the forward gain of bipolar transistors highly depends on the process parameters, and it is almost not possible to use high forward gain bipolar transistors in a standard CMOS technology.

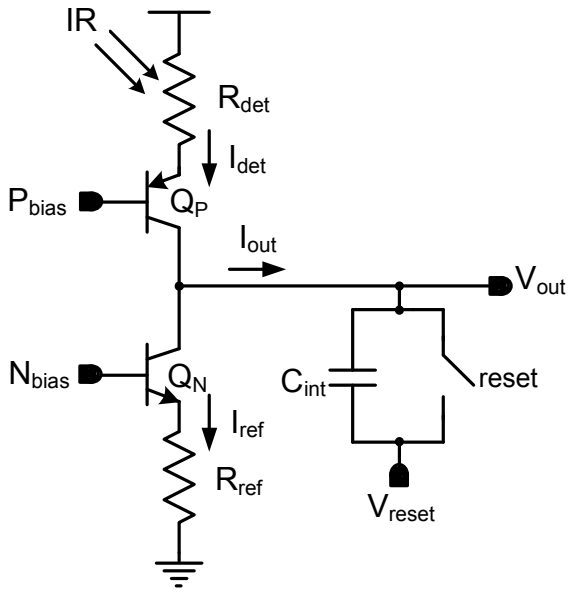


Figure 1.7: Schematic of the bolometer current direct injection amplifier [51].

1.2.2.3. Capacitive Transimpedance Amplifier

The most common readout circuit for resistive microbolometers is the capacitive transimpedance amplifier (CTIA) [28, 29, 44, 52]. Figure 1.8 shows the schematic of the CTIA. The detector and reference resistors are biased by a constant voltage, and the switched capacitor integrator integrates the detector current. Like the

bolometer current direct injection amplifier, the CTIA is also uses a reference resistor in order to cancel DC part of the detector current as well as self heating current and the current due to process and operating temperature variations.

The CTIA overcomes the nonlinear current integration problem of the bolometer current direct injection amplifier. The switched capacitor integrator connected to the drain terminals of the MOS injection transistors provide almost zero impedance charging path by establishing constant voltage at the drain of the injection transistors. Thus, the net output current, which is the difference of the detector and reference currents, is linearly integrated through the switched capacitor integrator.

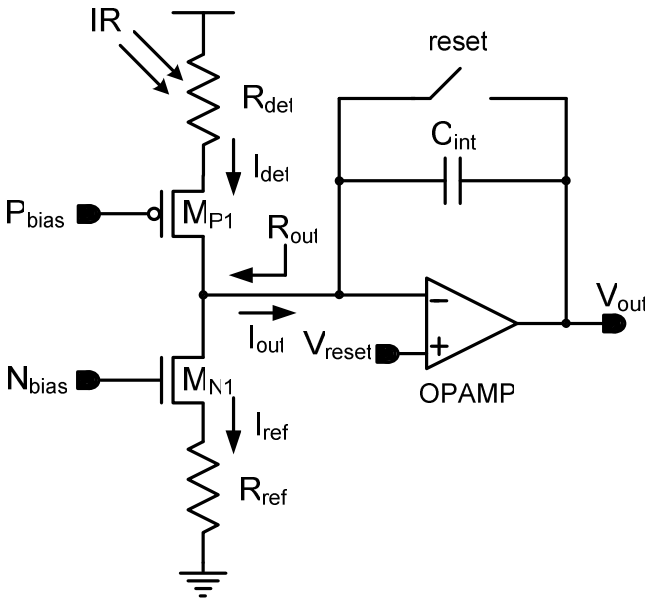


Figure 1.8: Schematic of the capacitive transimpedance amplifier (CTIA) [44].

Bias voltages of the detector and reference resistors are controlled by the bias voltages of the PMOS and NMOS injection transistor (M_{P1} and M_{N1}), respectively. Generally, digital-to-analog converters (DACs) controlled by external electronics are connected to the gate of the injection transistors in order to adjust the detector and

reference currents. By equalizing these currents, offset integration current becomes as low as possible which allows high signal integration time without saturation of the integration capacitor.

The CTIA is a low noise preamplifier. By proper choosing of the dimensions of injection transistors, the total noise is almost equal to noise of the detector and reference resistors provided that the operational amplifier's input referred noise is suppressed by the high output resistance seen by the inverting input of the operational amplifier. In fact, injection transistors which are in common gate connection increase the output resistance at that point. Therefore, the total noise is generally determined by the detector and reference resistors.

Since the CTIA is the most common preamplifier for resistive microbolometers, performance of the CTIA is examined in the next section in order to give a general idea about the performance of current readout electronics in the literature. The CTIA will also be explained in detail in Chapter II.

1.3. Performance of Resistive Microbolometer Readout Electronics

The main performance parameters of a readout circuit are responsivity, noise, signal-to-noise ratio (SNR), and noise equivalent temperature difference (NETD). Moreover, the other circuit specifications which determine the circuit performance are the circuit area, power dissipation, and resistance to temperature drift.

Responsivity is defined as the ratio of the detector current to the infrared power incident on the active detector area. Responsivity of the CTIA can be expressed as

$$\Re = \frac{g_m \times R_{\det}}{1 + g_m \times R_{\det i}} \times \frac{I_0 \alpha \eta}{G_{th}} \tag{1.3}$$

where, g_m is the transconductance of the injection transistor, R_{det} is the detector resistance, I_0 is the nominal current on the detector resistor, α is the TCR of the detector resistor, η is the absorption coefficient, and G_{th} is the thermal conductance of the detector. The first factor in the above responsivity equation is due to negative feedback structure of the CTIA amplifier. Generally, the g_m x R_{det} product is much larger than unity, so the only parameter in the responsivity equation which is related to the readout structure is the nominal current on the detector bias. Thus, the detector resistance should be selected as small as possible to increase responsivity. However, self heating of the detector increases with decreasing resistance, limiting the nominal bias current.

SNR is the ratio of the maximum detector current change due to infrared radiation to the root-mean-square (rms) current noise of the amplifier, ignoring the noise of the operational amplifier which is generally suppressed by the circuit. While the maximum detector current change is directly proportional to the nominal bias current of the detector, the total rms current noise is directly proportional to the square root of the bias current, assuming the detector and reference resistors are the only noise sources and ignoring Flicker noise of the resistors. Therefore, SNR becomes directly proportional to the square root of the bias current. Nevertheless, self heating of the detector is again the limiting case to use very high bias currents in the readout circuitry.

NETD is the difference in temperature between two side-by-side blackbodies of large lateral extent which gives rise to a difference in signal-to-noise ratio of unity in the electrical outputs of the two halves of the array viewing the two blackbodies when viewed by a thermal imaging system [13]. NETD of a resistive microbolometer can be given as [13]

$$NETD = \frac{4F^2 I_n}{\tau_0 A_D \Re (\Delta P / \Delta T)_{\lambda_1 - \lambda_2}} \tag{1.4}$$

where, I_n is the total electrical rms current noise, and $\Re$ is the responsivity in A/W, τ_0 is the transmittance of the optics, A_D is the active area of the detector in cm^2, F is a coefficient related with optics, and $(\Delta P/\Delta T)_{\lambda 1-\lambda 2}$ is a constant whose definition is the change in power per unit area radiated by a blackbody at temperature T, with respect to T, measured within the spectral band from λ_1 to λ_2.

NETD should be minimized for a better performance. Responsivity and noise are the only parameters in the above equation which can be controlled by the readout circuitry. In order to achieve small NETD, the nominal detector current should be high as in the high responsivity and high SNR cases.

The other circuit specifications which determine the circuit performance are the circuit area, power dissipation, and resistance to temperature drift. Low power dissipation is generally achieved by using low power, moderate slew-rate operational amplifiers which is enough to drive and reset integration capacitor.

Microbolometers generally work with temperature stabilizers in order to prevent the saturation of the integration capacitor due to temperature drift. Although there are microbolometer readout circuits which do not need a temperature stabilizer [53, 54], most of the circuits in the literature use temperature stabilizers. There is a worldwide trend for implementing microbolometer readout electronics resistant to temperature drift in order to obtain low cost and low power infrared imaging systems.

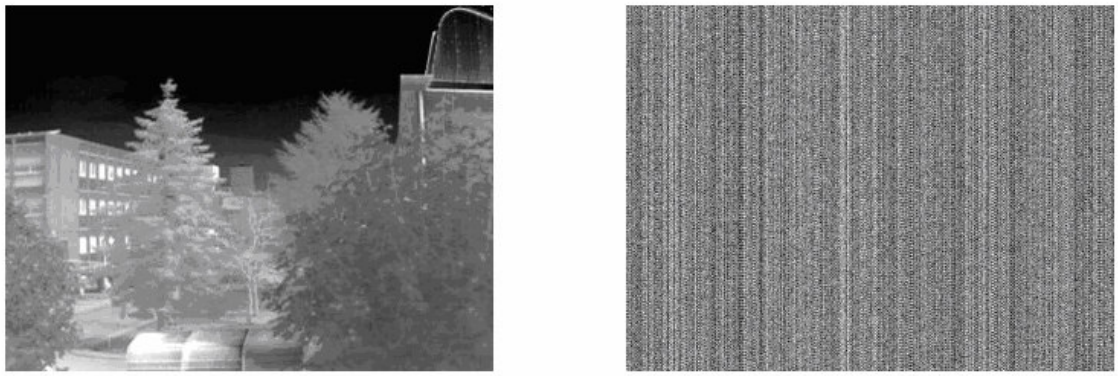
The circuit area is the final specification which determines the readout electronics performance. The main area occupying elements in the layout of a ROIC are integration capacitor and DACs. The integration capacitor should be high enough to not saturate with the integration current, which consists of the infrared induced current, self heating current, and offset current due to nonuniformities. Shortening the integration period is another method for preventing the saturation of the integration capacitor; nonetheless, shorter the integration time higher the rms noise and NETD. Offset current due to nonuniformities in detector parameters such as resistance and temperature coefficient of resistance (TCR) [55] should also be

considered by the readout circuit. Offset currents can be minimized effectively by using high resolution DACs, which usually occupy a large area, dissipate high power, and require complicated external circuitry with high frequency data transfer to the microbolometer chip. Therefore, there is a trade-off between the area of the integration capacitor and the resolution of compensation DACs.

The effects of nonuniformities can be shown by MATLAB simulations. In simulations, a 320x240 resistive microbolometer array is considered, where 320 parallel CTIAs are used with two reference resistors for each amplifier. These reference resistors are biased consecutively, preventing excessive self heating of the reference. Detector and reference parameters are as follows: 80 KΩ detector and reference resistances, $1.3x10^{-7}$ W/K thermal conductance, $2.2x10^{-9}$ J/K detector thermal capacity, $2.2x10^{-7}$ J/K reference thermal conductance [35], and 0.5 absorption coefficient. Timing parameters are selected as 30 frames per second (fps) image format, 140 μs detector selection time, 110 μs integration time. Finally, the maximum infrared power incident on a detector is taken as 10 nW.

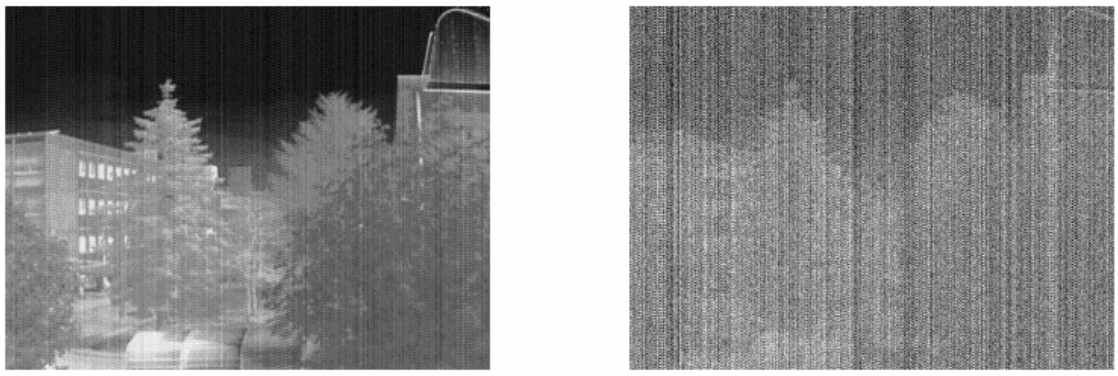
Figure 1.9 (a) shows the simulation output when the input image [52] is readout by a uniform resistive microbolometer array, while Figure 1.9 (b) shows the simulation output when the microbolometer array has nonuniformities such as ±5% resistance nonuniformity and ±1% thermal conductance, thermal capacitance, and absorption coefficient nonuniformities. In the latter case, most of the pixels in the detector array saturate, causing lost of the infrared data.

Figure 1.10 (a) shows the simulation output when thermal conductance, thermal capacitance, and absorption coefficient nonuniformities are ±0.1%, while Figure **1.10** (b) shows the simulation output when only resistance nonuniformity is ±0.1%. Therefore, resistance nonuniformity has the highest effect on distortion of the output image. The offset current due to resistance nonuniformity compensated by the use of DACs, which are connected to the injection transistors of the CTIA and programmed to allow a predefined current through microbolometer resistors [44].



(a) (b)

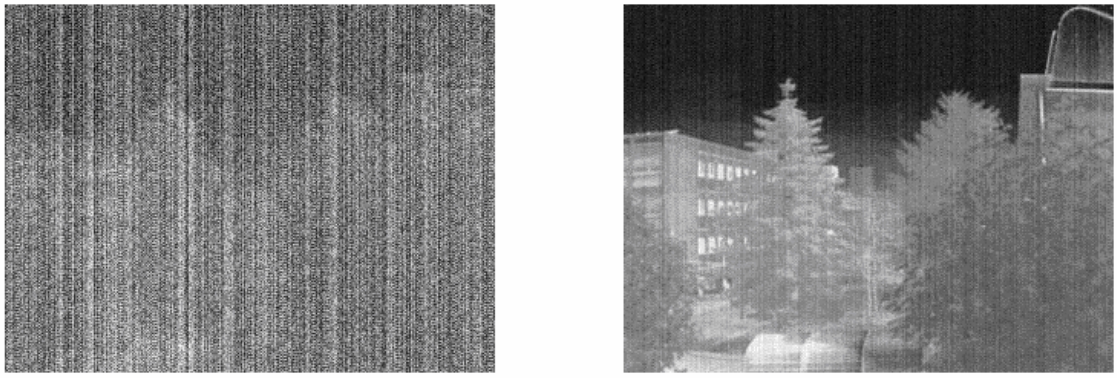
Figure 1.9: Output image of two systems: (a) an ideal system, i.e., all parameters are uniform and (b) an actual system when resistance nonuniformity is ±5% and thermal conductance, thermal capacitance, and absorption coefficient nonuniformities are ±1%. In this case most of the pixels saturate and infrared data are almost lost.



(a) (b)

Figure 1.10: Output images of the system (a) when thermal conductance, thermal capacitance, and absorption coefficient nonuniformities are ±0.1% and (b) when only resistance nonuniformity is ±0.1%. Resistance nonuniformity causes the most distortion.

The resolution of compensation DACs determines the amount of the maximum offset current. Higher the DAC resolution lower the maximum offset current. Figure 1.11 (a) and (b) show simulation outputs of an actual system which uses 10-bit DACs and 14-bit DACs, respectively. Although these images are not clear especially the first one, most of the infrared data can be extracted after removing the spatial nonuniformity, because DACs prevent the saturation of the integration capacitor and lost of infrared information.

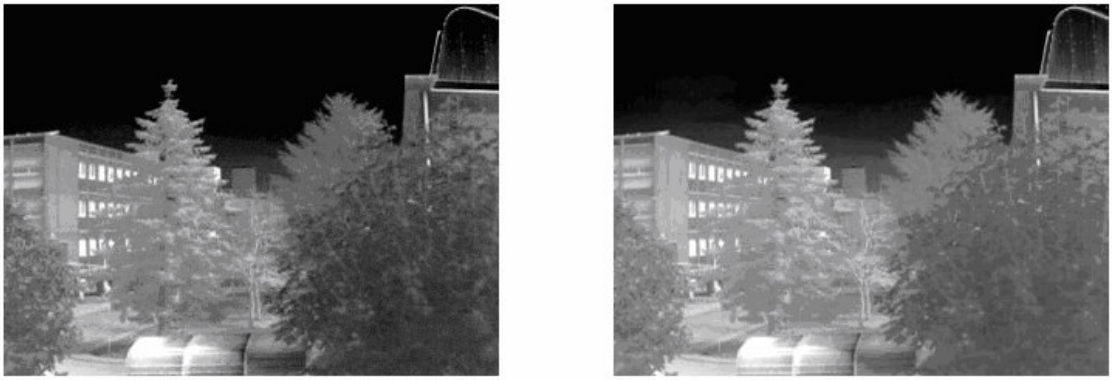


(a) (b)

Figure 1.11: Output images of an actual system with resistive nonuniformity compensation when saturation of the integration capacitor is prevented by using: (a) 10-bit DACs and (b) 14-bit DACs. Resistance nonuniformity is ±5% and thermal conductance, thermal capacitance, and absorption coefficient nonuniformities are ±1%.

Nonuniformity correction (NUC) algorithms effectively remove the spatial nonuniformity. In the literature, there are a number of algorithms such as two-point [56, 57], multi-point [58, 59], and other correction methods [60, 61]. Higher the number of correction points, better the nonuniformity correction, because each detector in the microbolometer array has a different nonlinear response curve. Increasing the number of correction points provides better fit to the detector response

curve, i.e., a multi-point algorithm can correct a nonlinear response curve over a wide temperature range [58]. Figure 1.12 shows the simulation output extracted from the image in Figure 1.11 (a) by using one-point NUC and two-point NUC. The second image has lower spatial noise due to nonuniformities of the microbolometer detector array.



(a) (b)

Figure 1.12: Output images extracted from the image in Figure 1.11 (a) by using (a) one-point NUC (b) and two-point NUC. The second image has lower spatial noise.

In summary, an ideal readout circuit for resistive microbolometers should (1) be capable of low noise amplification with high SNR, (2) compensate the resistance nonuniformity to prevent the saturation of the readout, (3) occupy a small area, and (4) dissipate low power.

So far at METU, the uncooled infrared research is mainly conducted on diode type microbolometer detector arrays and their readout electronics [45-47]. Although it is possible to fabricate very low cost diode type readout imaging systems, their performance is limited by their readout circuit that has much higher noise than its detector [46]. Therefore, resistive microbolometer detector arrays with their high

performance readout electronics have started to be developed in order to fabricate higher performance uncooled infrared imaging systems.

The work presented in this thesis reports the development of high performance readout electronics for resistive microbolometer detector arrays. Three different preamplifiers are designed, fabricated, and tested with novel circuit parts with unique properties in the literature. Research objectives and thesis organization are explained in the next section.

1.4. Research Objectives and Thesis Organization

The goal of this research is to develop high performance readout electronics for resistive microbolometer detector arrays. The specific objectives can be listed as follows:

1. Development of readout circuits for resistive microbolometers capable of low noise amplification with high SNR and compensating the resistance nonuniformity to prevent the saturation of readout electronics. The circuit should occupy a small area and dissipate low power in order to be used in large array microbolometer applications.

2. Development of novel compensation structures for resistive microbolometers which simplify the operation without compromising the performance. As well as small circuit area and low power dissipation specifications, the circuit should be resistant to temperature drift in time in order to reduce the dependence of the circuit on temperature stabilizers.

3. Preparation of required test setups of the fabricated chips. In addition to monitoring the transient operation, performance parameters including noise and SNR should be measured. Printed circuit boards should be designed in order to

monitor detector and reference current waveforms, where digital signals are provided by an FPGA. Furthermore, a discrete low-noise preamplifier should be designed for readout noise measurements. Finally, a high resolution analog-to-digital converter (ADC) card should be prepared for measuring overall noise of the system.

Thesis organization and contents of the following chapters are summarized as follows:

Chapter II gives detailed information about a CTIA type resistive microbolometer readout circuit including its compensation DACs. It also gives the architecture of the chip, design steps of the readout circuit, simulation and test results in detail.

Chapter III introduces a new dynamic nonuniformity compensation circuit including its preamplifier for resistive microbolometer applications. The chapter also presents the design of the chip, the operation principle of the proposed circuit, simulation and test results.

Chapter IV presents an improved readout circuit for resistive microbolometers which has two operation modes: static and dynamic. The static readout circuit improves the conventional CTIA type readout circuit, whereas the dynamic circuit overcomes main problems of the dynamic nonuniformity compensation circuit which is presented in Chapter III. This chapter gives the operational principle, the circuit design, and simulation and test results of the improved circuit.

Finally, Chapter V summarizes the research performed, presents the conclusions of this research, and gives possible future work related to this study.

CHAPTER II

A CAPACITIVE TRANSIMPEDANCE AMPLIFIER TYPE READOUT CIRCUIT

This chapter presents design details, implementation, and simulation and test results of a high performance readout circuit for resistive uncooled microbolometer detector arrays. The design includes a capacitive transimpedance amplifier (CTIA), a sample-and-hold circuit, two compensation digital-to-analog converters (DACs), and detector and reference resistors arrays where low power and low noise DACs with high output resolution property adjust bias currents of detector and reference resistors for different resistance values. The circuit is fabricated by a standard 0.6 μm CMOS process. As well as verification of circuit operation, the chapter gives performance parameters like noise and compensation ratio measurement results.

This chapter is organized as follows: Section 2.1 presents the operating principle of the chip. Section 2.2 gives detailed information about the circuit blocks. The structure of each block and their operation principle are explained, and Cadence simulation results and layout snapshots are given with each block. Section 2.3 presents the overall schematic, overall layout, and floor plan of the designed chip. Section 2.4 gives the test results of the fabricated chip. Finally, Section 2.5 concludes the chapter by summarizing the features of the readout electronics.

2.1. Operating Principle of the Readout Circuit

In a focal plane array (FPA), which consists of two dimensional arrays of microbolometer detectors, a readout integrated circuit (ROIC) is supposed to readout a number of detectors, depending on the size of the array and the number of parallel readout channels in the FPA chip.

For a given size of an array, when the number of readout channels is increased, the integration time for a detector will increase, resulting in a decrease in the electrical bandwidth according to the following equation [62]:

$$BW = \frac{1}{2T_{\text{int}}} \tag{2.1}$$

where, BW is the electrical bandwidth of the integrator output and T_{int} is the integration period for a detector. The detector is selected by analog switches in order to be readout by the ROIC.

Figure 2.1 shows a ROIC for resistive microbolometers, including a CTIA, a sample-and-hold (S&H) circuit, and two compensation DACs. CTIA is a low noise preamplifier that integrates the detector current. DACs are connected to the injection transistors (M_{N1} and M_{P1}) of CTIA and programmed to allow a predefined current through the injection transistors. If DACs are not used, the integration capacitor mostly saturates before the end of the integration period, because the offset currents due to resistance nonuniformity is much higher than the maximum infrared induced current [54]. After the signal integration, the S&H circuit samples the voltage at the output of the CTIA and holds it until the next sample of the next pixel.

The circuit noise depends on the electrical bandwidth and thus on the number of readout channels in the FPA chip. The number of readout channels should increase in order to improve the performance, which is possible by using small area readout circuits in each readout channel. DACs are generally the most area occupying

elements in a readout circuit. Therefore, area-performance optimization of DACs is imperative for improving the performance of the circuit. A special DAC architecture is used in the design, which is given in detail in the following sections along with the other structures, such as the CTIA and the S&H circuit.

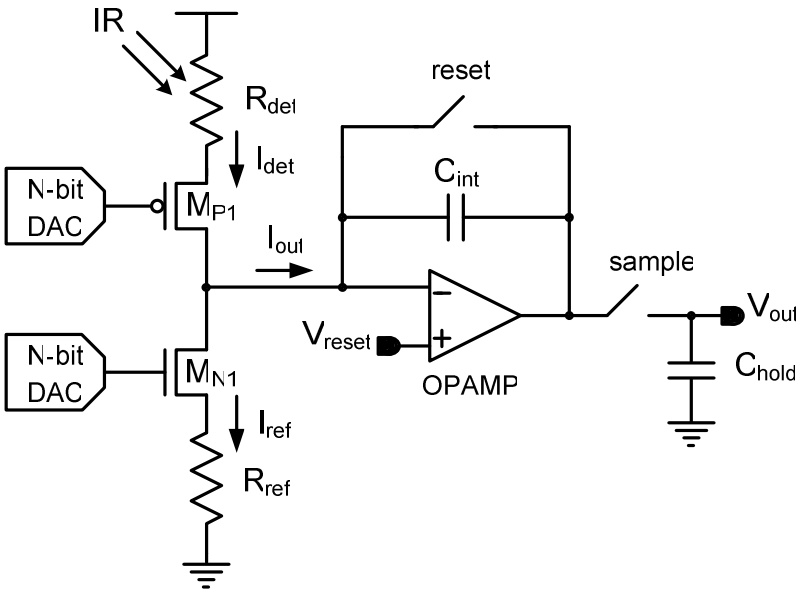


Figure 2.1: Simplified schematic of a CTIA type ROIC for resistive micro-bolometers, which includes a CTIA, a sample-and-hold circuit, and two compensation DACs.

2.2. Design of the Readout Circuit

This section explains detector and reference resistors selection circuits, detector and reference resistors bias circuit, the DAC, the switched capacitor integrator (SCI) of the CTIA, and S&H circuit in detail along with their Cadence simulation results.

2.2.1. Detector and Reference Resistor Selection Circuits

In order to verify the operation of the circuit, various reference and detector resistors are implemented with the high resistance poly layer of the CMOS process. The nominal resistance value is selected as 80 KΩ, while resistance nonuniformity of ±5% is achieved by implementing 16 reference and detector resistors in the range of 76 KΩ to 84 KΩ.

2.2.1.1. Detector Resistor Selection Circuit

The detector resistor is selected by four inputs connected to a 4-to-16 decoder. Figure 2.2 shows the block diagram of the detector resistor selection circuit.

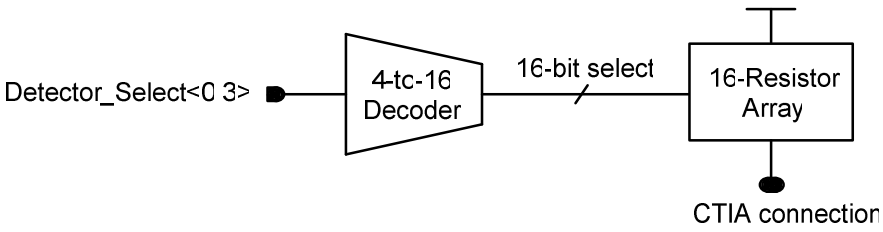


Figure 2.2: Block diagram of the detector resistor selection circuit.

Figure 2.3 shows the circuit schematic of the 16 detector resistor array. The outputs of the 4-to-16 decoder are connected to the gates of PMOS selection transistors in the resistor array. The aspect ratio of PMOS selection transistors is 60 µm/2 µm. The on-resistance of selected transistors is around 650 Ω, which is negligibly small with respect to the nominal detector resistance of 80 KΩ. Only one of the PMOS transistors turn on depending upon the select input, providing a low resistance, around 650 Ω, connection to the PMOS injection transistor of the CTIA.

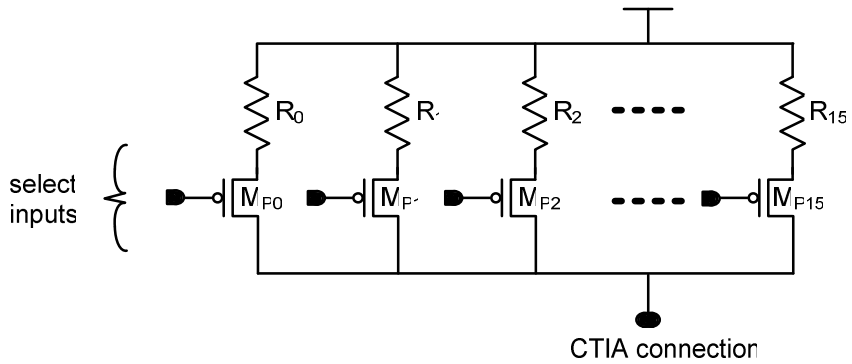


Figure 2.3: Schematic of the 16-resistor array for the detector resistance.

2.2.1.2. Reference Resistor Selection Circuit

The selection mechanism of the reference resistor is the same as that of the detector resistor. Figure 2.4 gives the block diagram of the reference resistor selection circuit.

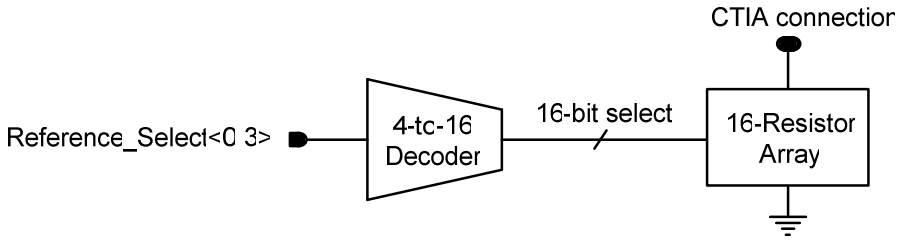


Figure 2.4: Block diagram of the reference resistor selection circuit.

Figure 2.5 shows the circuit schematic of the 16-resistor array used for reference resistor. In this case, the aspect ratio of NMOS selection transistors is 19.5 µm/2 µm. The on-resistance of select transistors is around 650 Ω, which is approximately same as that of PMOS selection transistors. These switches connect reference resistors to the NMOS injection transistor of the CTIA.

The 4-to-16 decoders are constructed by using sixteen 4-input OR gates for detector selection and by using sixteen 4-input AND gates for reference selection. Table 2.1 shows the selected detector and reference resistors with respect to the decoder inputs.

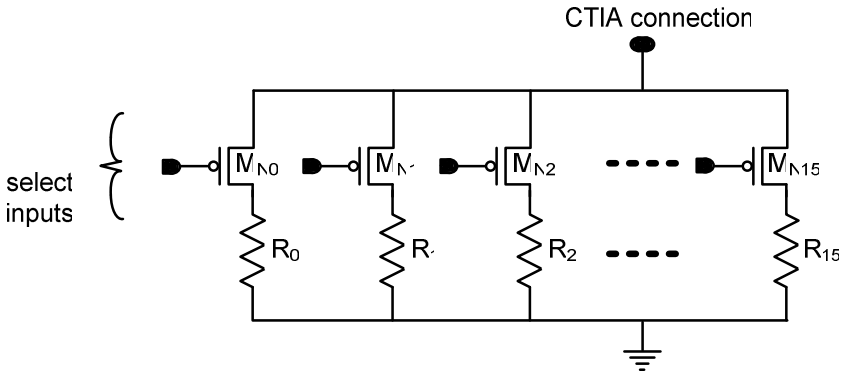


Figure 2.5: Schematic of the 16-resistor array for the reference resistance.

Table 2.1: Select inputs of decoders for the detector and reference resistor selection.

Detector or Reference Select Signal <3:0>	Reference or Detector Resistance (Ω)
0000	84000
0001	83500
0010	83000
0011	82000
0100	81500
0101	81000
0110	80500
0111	80000
1000	79920
1001	79500
1010	79000
1011	78500
1100	78000
1101	77000
1110	76500
1111	76000

Figure 2.6 shows the layout of detector and reference resistor selection circuits. It measures 725 µm x 270 µm in a 0.6 µm CMOS process. Resistors are implemented with the high resistance poly layer of the CMOS process.

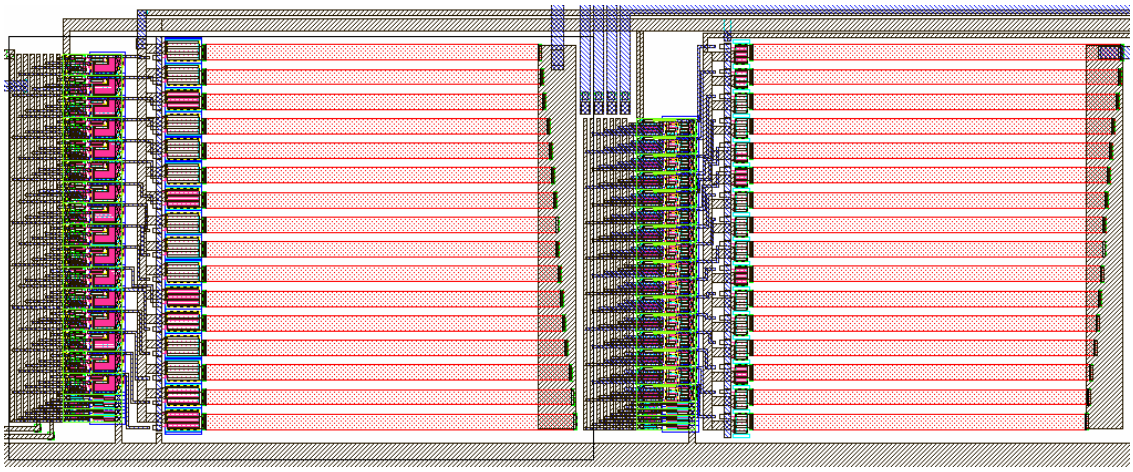


Figure 2.6: Layout of the detector (the left side) and reference (the right side) resistor arrays with selection switches. The layout measures 725 µm x 270 µm in a 0.6 µm CMOS process.

2.2.2. Detector and Reference Resistors Bias Circuit

Figure 2.7 shows the biasing circuit of the detector and reference resistors. The currents through the detector and reference resistors (I_{det} and I_{ref}) are controlled by voltages applied to the gates of the injection transistors (M_{P1} and M_{N1}) of the CTIA. There is a negative feedback between the bias voltage on a resistor and the current passing through that resistor as explained below for the reference resistor biasing:

$$N_{bias} = V_{GS} + I_{REF} \times R_{REF} \tag{2.2}$$

where, N_{bias} is the gate voltage of M_{N1}, V_{GS} is the gate-to-source voltage of M_{N1}, and I_{REF} is the current passing through the reference resistor, R_{REF}. Assuming the proper

mode of operation, i.e., the transistor is in the saturation state, the formula becomes as follows ignoring the body effect and channel length modulation of the transistor:

$$N_{bias} = V_{GS} + \frac{K_N}{2}(V_{GS} - V_{TN})^2 \times R_{REF} \tag{2.3}$$

where, K_N and V_{TN} are the transconductance and the threshold voltage of the transistor, respectively. By solving the quadratic equation

$$V_{REF} = I_{REF} \times R_{REF} = N_{bias} - V_{TN} - \frac{\sqrt{1 + 2K_N R_{REF}(N_{bias} - V_{TN})} - 1}{K_N R_{REF}} \tag{2.4}$$

bias voltage on the reference resistor, V_{REF}, is found out that it increases slightly with increasing resistance. Therefore, the current change due to the resistance change slightly decreases, and hence responsivity of the circuit slightly decreases. In order to reduce this undesired feedback effect, the $K_N R_{REF}$ product must be high.

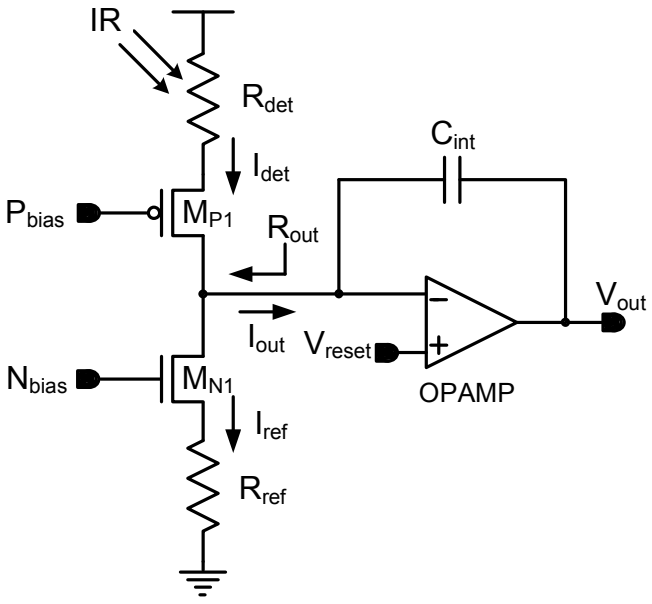
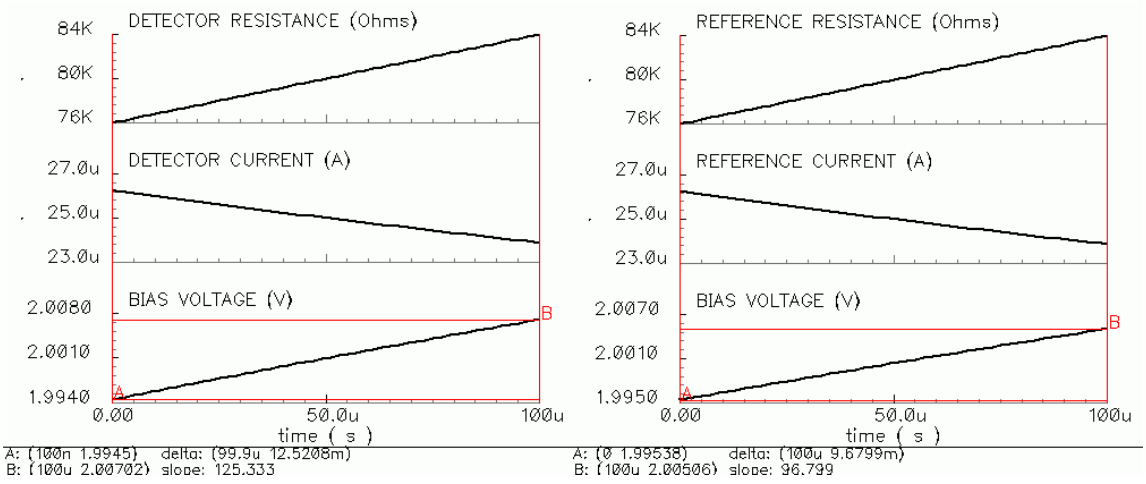


Figure 2.7: Schematic of the biasing circuit of the detector and reference resistors.

Figure 2.8 gives simulation results showing the almost constant voltage bias on the detector and reference resistors. Both of the resistors are swept from 76 KΩ to 84 KΩ, i.e., in the ±5% resistance nonuniformity range. While the currents through resistors change approximately 10%, the bias voltages on the resistors change only 0.5%.



(a) (b)

Figure 2.8: Bias voltage and bias current values of (a) detector and (b) reference resistors with respect to their resistance. The currents through resistors change approximately 10%, and the bias voltages on the resistors change only 0.5% when both of the resistors are swept from 76 KΩ to 84 KΩ. These results support the almost constant voltage bias of the biasing circuit.

Figure 2.9 shows the schematic of (a) the biasing circuit and (b) the biasing circuit with noise sources. M_{P2} and M_{N2} are switches in order to select the detector and reference resistor respectively. The total noise power spectral density of the biasing circuit output current (I_{out}) is equal to the sum of the noise power spectral densities of each current noise source and noise current power spectral density generated by the input referred noise of the operational amplifier.

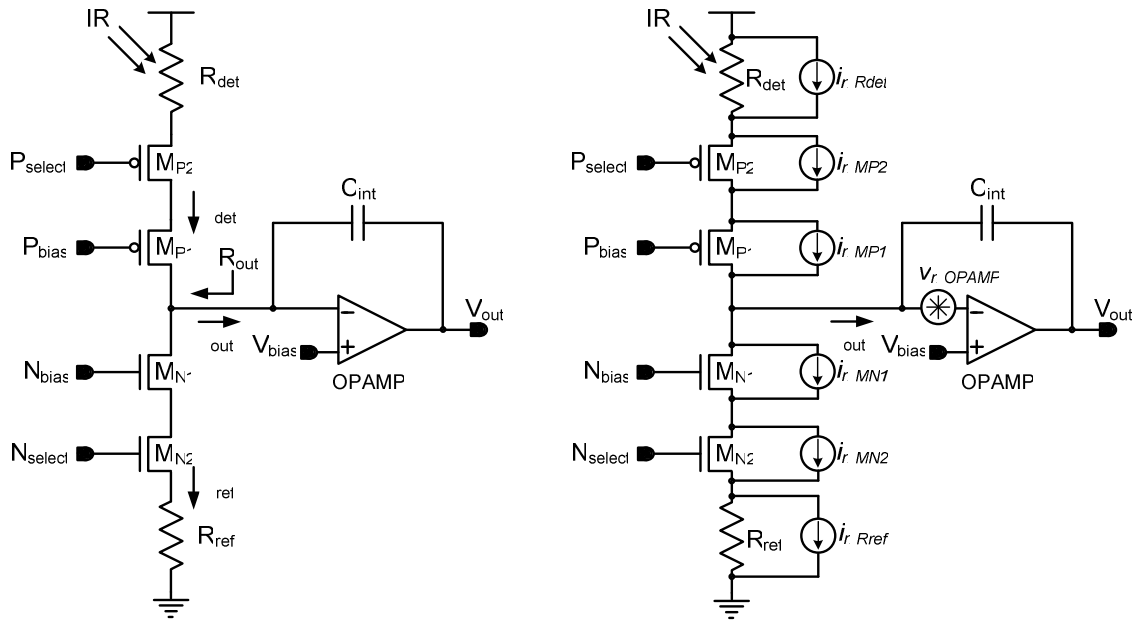


Figure 2.9: Schematic of (a) the biasing circuit and (b) the biasing circuit with noise sources.

The current noise power spectral densities of a transistor and a resistor can be expressed as:

$$i^2_{n,R\det} = \frac{4kT}{R_{\det}} + \frac{I^2_{\det} K_{1/f}}{f} \tag{2.5}$$

$$i^2_{n,MP1} = \frac{8kT}{3g_{m,MP1}R_{\det}^{\ 2}} + \frac{K_p}{C_{ox}(WL)_{P1} f R_{\det}^{\ 2}} \tag{2.6}$$

where, R_{det} is the detector resistance, I_{det} is the bias current of the detector resistor, $g_{m,MP1}$ is the transconductance of M_{P1}, C_{ox} is the unite area gate oxide capacitance of a transistor, W and L are the width and length of M_{P1}, f is the frequency, T is the absolute temperature, k is the Boltzman constant, and $K_{1/f}$ and K_P are the Flicker noise constants for a PMOS transistor and a resistor, respectively. The Boltzman constant is equal to $1.38\text{x}10^{-23}$ J/K, while Flicker noise constants are very process

dependent [63]. Assuming that the $g_{m,MP1}R_{det}$ product is much higher than unity which is also the case for almost constant voltage biasing property of the circuit, the total noise power spectral density of the output current can be expressed as:

$$i^2_n = i^2_{n,R\det} + i^2_{n,MP2} + i^2_{n,MP1} + i^2_{n,Rref} + i^2_{n,MN2} + i^2_{n,MN1} + \frac{V^2_{n,OPAMP}}{R^2_{out}} \qquad (2.7)$$

where, $V^2_{n,OPAMP}$ is the input referred noise power spectral density of the operational amplifier and R_{out} is the output resistance of the biasing circuit. Generally, the dominant noise source is the noise of the detector and reference resistors. Noise of the transistors is suppressed by the high transconductance of the injection transistors, and input referred voltage noise of the operational amplifier is suppressed by the high resistance seen from the inverting input of the operational amplifier.

For a 5 V CMOS technology, the CTIA allows up to 30 μA bias current for 80 KΩ detector and reference resistors; however, the output resistance of the biasing circuit decreases with increasing bias current. Since the input referred noise of the operational amplifier is seen by the output resistance of the biasing circuit, a low biasing circuit output resistance causes a high current noise on the output current. Figure 2.10 shows dependence of output resistance and noise current upon the bias current of the CTIA. On the other hand, the performance of the microbolometer improves with increasing bias current as follows:

$$SNR = I_{IR,\max} / \bar{i}_n \qquad (2.8)$$

where, SNR is the signal-to-noise ratio of the CTIA output, $I_{IR,\ max}$ is the maximum detector current change due to infrared radiation, and i_n is the root mean square (rms) output noise current. $I_{IR,\ max}$ can be written:

$$I_{IR,\max} = I_{BIAS} \times \alpha \times \Delta T_{IR,\max} \qquad (2.9)$$

where, I_{BIAS} is the detector bias current, α is the temperature coefficient of resistance (TCR) of the detector resistor, and $\Delta T_{IR,\ max}$ is the maximum temperature of the detector microbolometer due to the absorbed infrared power. Assuming the dominant noise source is the thermal noise of the detector and reference resistors, the rms output noise current is equal to:

$$\bar{i}_n \cong \sqrt{8kT\Delta f / R} \tag{2.10}$$

where, k is the Boltzman constant, T is the absolute temperature, Δf is the electrical bandwidth of the output current in Hz, and R is the resistance of the detector and reference microbolometers. Therefore, SNR can be expressed as:

$$SNR = \frac{\sqrt{I_{DET}}\sqrt{V_{DET}} \times \alpha \times \Delta T_{IR,\max}}{\sqrt{8kT\Delta f}} \tag{2.11}$$

where, V_{DET} is the bias voltage on the detector and reference microbolometers. I_{DET} and V_{DET} are the readout circuit parameters in the above equation. V_{DET} is constant for a CMOS process, i.e., it is around 2 V in a 5 V CMOS process. Therefore, I_{DET} is the only readout circuit parameter which affects the SNR.

Figure 2.10 gives the dependence of biasing circuit output resistance and rms output current noise on the CTIA bias current. Since SNR is proportional to the square root of the bias current, the bias current should be high. However, the output resistance should also be high in order to suppress the input referred noise voltage of the operational amplifier, as stated in the Equation 2.7. Considering the need for high SNR and high CTIA output resistance, the bias current of the CTIA is chosen as 25 μA.

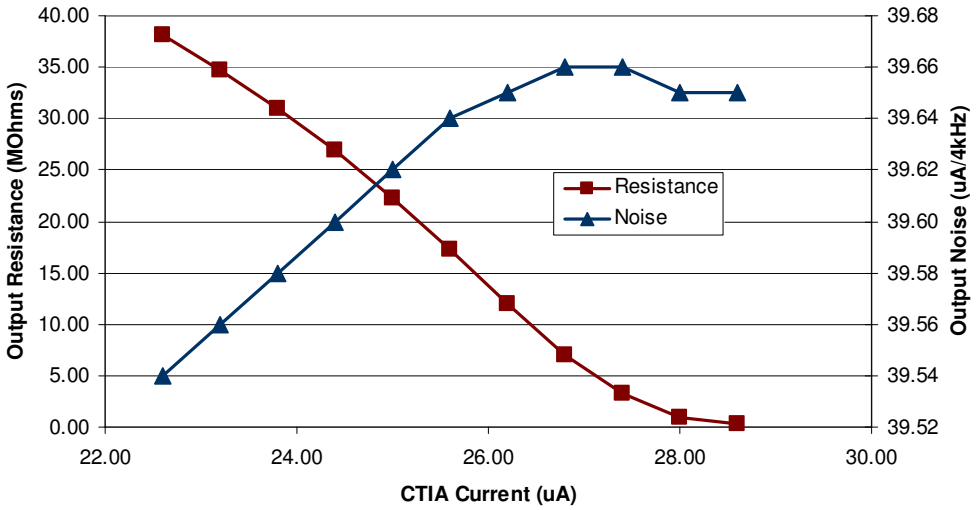


Figure 2.10: Output resistance and output noise of the CTIA with respect to bias current. While output noise stays almost constant, output resistance drastically decreases with increasing bias current, which increases the effect of input referred noise of the operational amplifier.

Aspect ratios of the PMOS and NMOS injection transistors (M_{P1} and M_{N1}) of CTIA are set considering the output resistance, the output current noise, and circuit responsivity. While the same transistor length is used for both of injection transistors, the width of the PMOS transistor is drawn two times of that of the NMOS transistor, considering the electron and hole mobility of the fabrication process and body effect of the NMOS transistor. In the final design aspect ratio of NMOS and PMOS injection transistors are selected as 120 µm/10 µm and 240 µm/10 µm, respectively. The output resistance of the CTIA is 22.3 MΩ and rms output current noise of the CTIA is 39.6 pA in a 4 KHz electrical bandwidth. This amount of output resistance is high enough to suppress the input referred noise of the operational amplifier. The aspect ratio of the detector and reference selection switches are chosen considering their on-resistances, as explained in Section 2.1.1. Table 2.2 gives the aspect ratios and the number of gates of the transistors in the biasing circuit of the CTIA shown in Figure 2.9 (a).

Table 2.2: Aspect ratios and number of gates of the transistors in the biasing circuit.

Transistor	Aspect Ratio (µm/µm)	Number of Gates
M_{P1}	240/10	4
M_{N1}	120/10	4
M_{P2}	60/2	3
M_{N2}	19.5/2	3

Currents through detector and reference resistors are controlled by the bias voltages of the injection transistors. Figure 2.11 and Figure 2.12 demonstrate the change in the bias voltages of the NMOS and PMOS injection transistors to obtain 25 µA reference and detector currents for resistance values of 76 KΩ, 80 KΩ, and 84 KΩ.

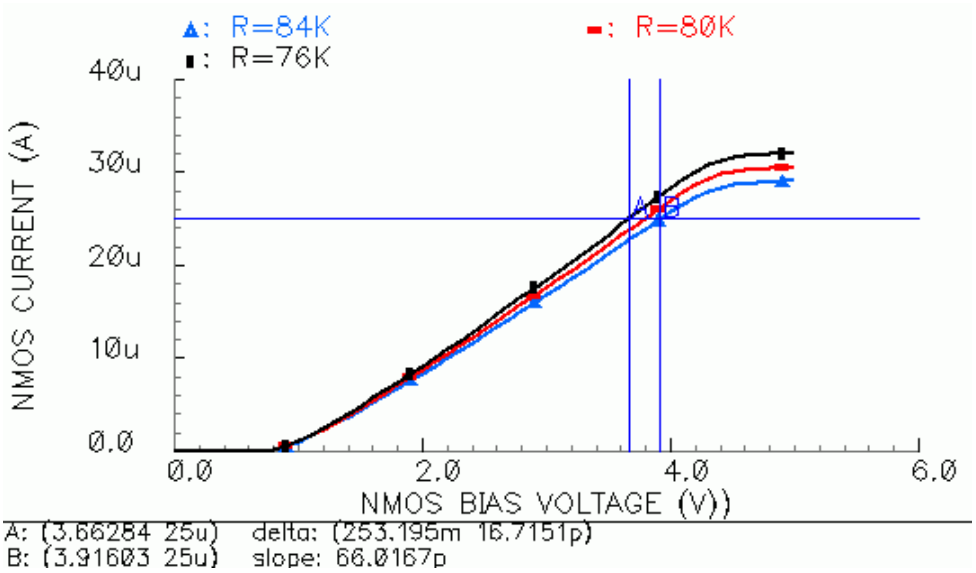


Figure 2.11: Simulation results of the reference current versus NMOS injection transistor bias voltage for different values of the reference resistor. Bias voltage should increase for larger resistors in order to provide constant current for the reference resistance values in the resistance nonuniformity range.

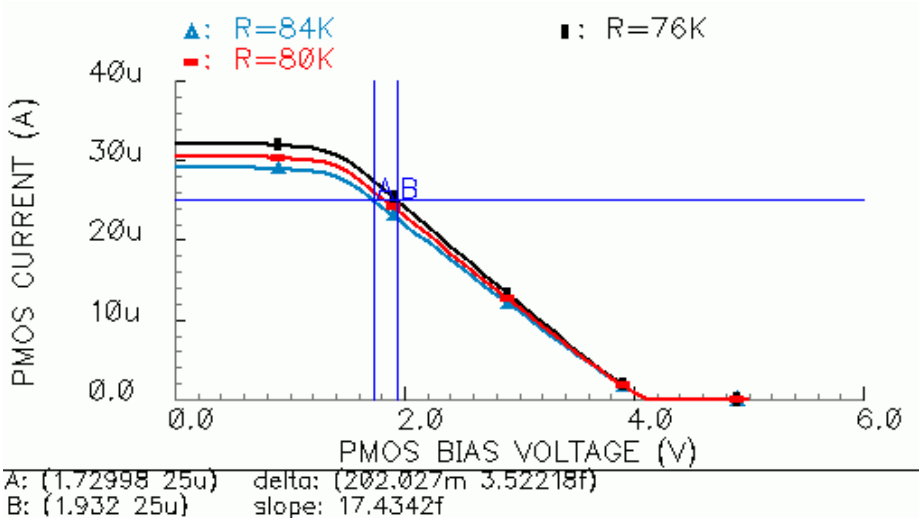


Figure 2.12: Simulation results of the detector current versus PMOS injection transistor bias voltage for different values of the detector resistor. Bias voltage should decrease for larger resistors in order to provide constant current for the detector resistance values.

The magnitude of the bias current determines the responsivity of the circuit, as explained in Section 1.3. The amount of the current change is proportional to the magnitude of the bias current. For a 25 µA bias current and a 80 KΩ microbolometer resistor, the current change due to a 1 Ω resistance change is around 0.3 nA. Figure **2.13** and Figure 2.14 show the transient simulation of the biasing circuit of the CTIA. While the output current changes 29.28 nA when the detector resistance changes 100 Ω, the output current changes 29.77 nA when the reference resistance changes 100 Ω. In the same manner, the detector resistance change due to the absorbed infrared power changes the output current.

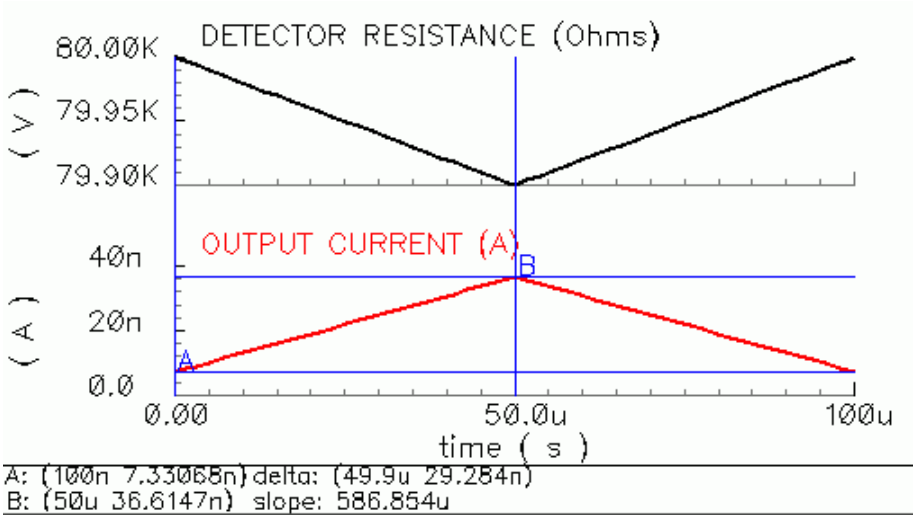


Figure 2.13: Transient simulation of the biasing circuit of the CTIA. The output current changes 29.28 nA when the detector resistance changes 100 Ω.

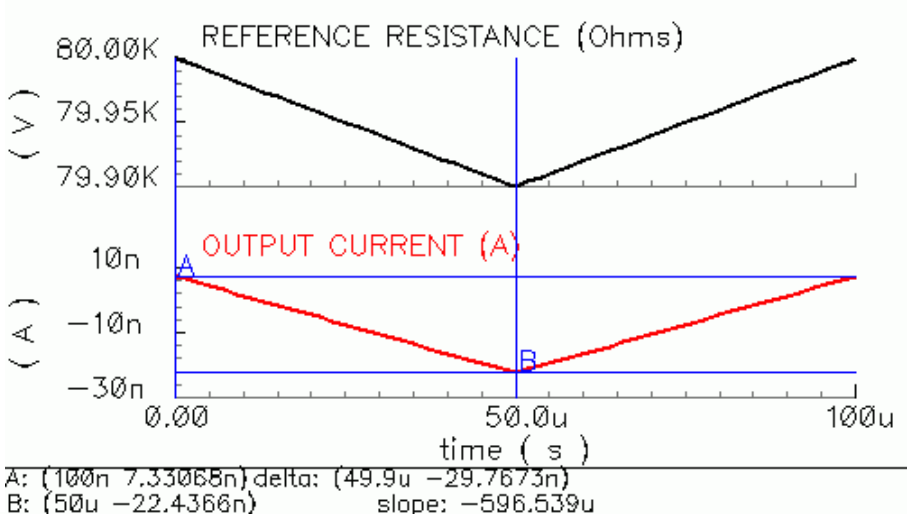
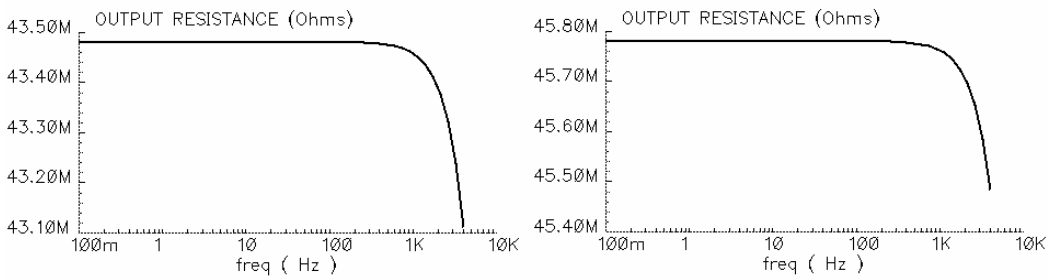


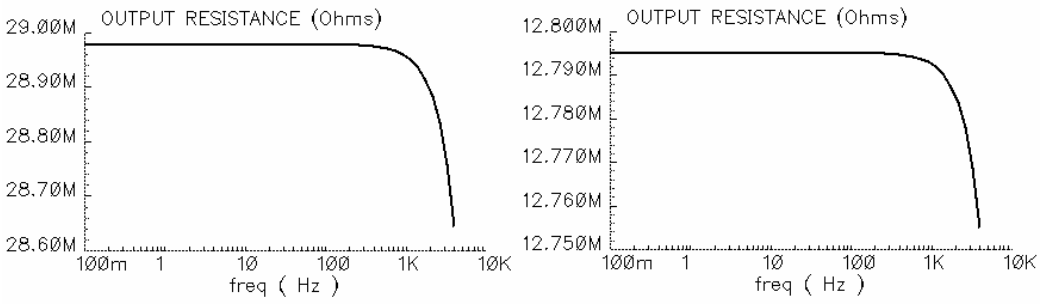
Figure 2.14: The output current changes 29.77 nA when the reference resistance changes 100 Ω. However, the change in the output current is in the reverse direction of the detector case.

The output resistance of the biasing circuit should be high for suppressing the input referred noise of the operational amplifier in order to achieve low noise signal integration. In fact, the injection transistors of the biasing circuit are in common gate connection, which increases the output resistance. Figure 2.15 shows the simulated output resistance versus frequency of the reference side and of the detector side of the biasing circuit for 80 KΩ reference and detector resistors. Output resistances of two sides are approximately equal, proving the proper choice of selecting the aspect ratio of the NMOS and PMOS injection transistors. The output resistance strongly depends on the bias level at the gate of the injection transistor. Since bias voltages are subject to change to adjust the microbolometer current for different resistance values, output resistances are also subject to change. For the reference side of the biasing circuit, the maximum output resistance is 69.5 MΩ and occurs when the reference resistor is minimum, 76 KΩ; the minimum output resistance is 19.5 MΩ and occurs when the reference resistor is maximum, 84 KΩ. For the detector side of the biasing circuit, the maximum and minimum output resistances are 49.7 MΩ and 37.2 MΩ, respectively. Figure 2.16 gives the maximum and minimum cases of the output resistance versus frequency graphics of the whole biasing circuit, where the DC output resistance values are 29 MΩ and 12.8 MΩ, respectively.



(a) (b)

Figure 2.15: Output resistance versus frequency (a) of the reference side and (b) of the detector side of the biasing circuit for 80 KΩ reference and detector resistors.



(a) (b)

Figure 2.16: Output resistances versus frequency of the biasing circuit (a) for the maximum resistance case and (b) for the minimum resistance case. Output resistance stands higher than 12 MΩ in the worst case, which is still high enough to suppress the input referred voltage noise of the operational amplifier.

Therefore, the input referred noise power spectral density of the operational amplifier in Equation 2.7 can be neglected. The total noise power spectral density of the output current becomes as follows:

$$i^2_n = i^2_{n,R\,\det} + i^2_{n,MP2} + i^2_{n,MP1} + i^2_{n,Rref} + i^2_{n,MN2} + i^2_{n,MN1} \tag{2.12}$$

where, the total current noise spectrum is equal to the sum of the individual current noise spectrum of each noise source, namely the detector and reference resistors, the PMOS and NMOS injection and selection transistors.

Figure 2.17 shows the simulated output current noise of the CTIA biasing circuit. The rms current noise is 39.62 pA in an electrical bandwidth of 4 KHz. Noise also depends on the microbolometer resistor values, which can take any value in the nonuniformity range. For the minimum case, the reference and detector resistances are 84 KΩ, and the rms current noise is 38.7 pA in an electrical bandwidth of 4 KHz; and for the maximum case, the reference and detector resistances are 76 KΩ, and the rms current noise is 40.61 pA in an electrical bandwidth of 4 KHz.

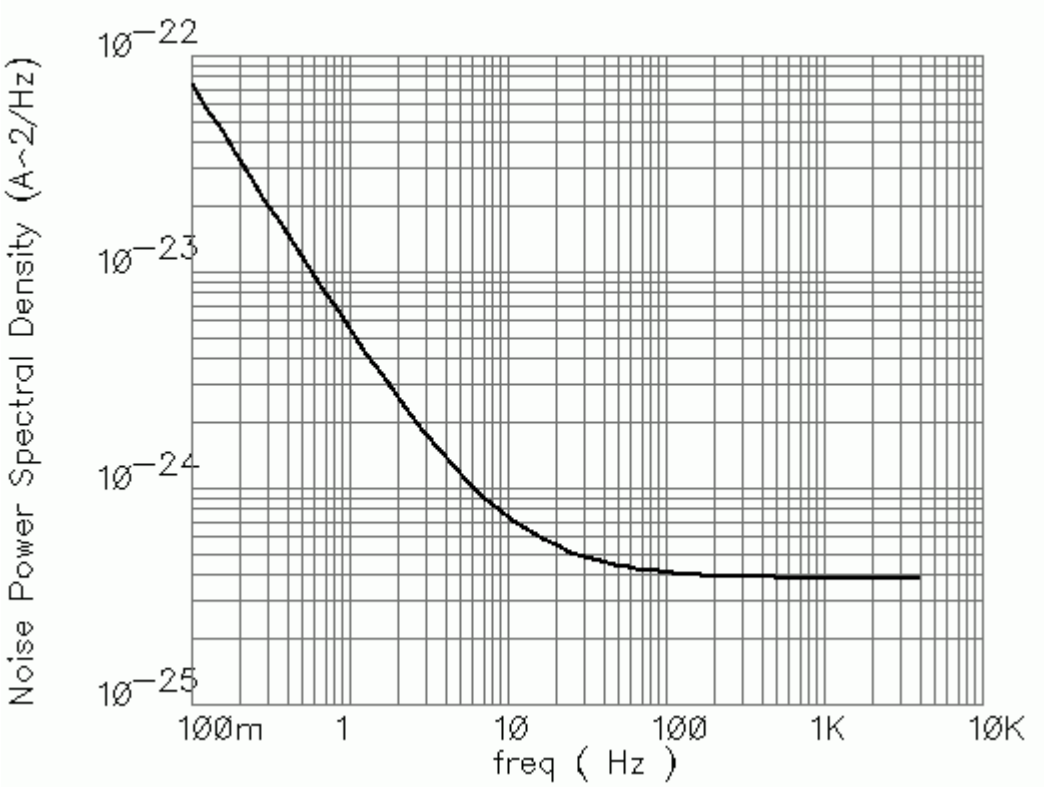


Figure 2.17: Simulated noise power spectral density of the biasing circuit of the CTIA for 80 KΩ reference and detector resistors. The rms current noise is 39.62 pA in an electrical bandwidth of 4 KHz.

2.2.3. Digital-to-Analog Converter (DAC)

The offset current at the output of the biasing circuit, which is generally much higher than the current due to infrared radiation, occupies most of the dynamic range of the switched capacitor integration circuit, reducing the responsivity of the readout circuit. Therefore, this offset current, which is mainly because of the resistance nonuniformity, must be removed by a compensation circuit before the detector current integration.

One method to cancel the offset current is to adjust the bolometer resistance by switching series resistors; however, since the series resistors have no responsivity,

the performance of the microbolometer decreases [64]. Another method is to use high resolution DACs that are connected to gates of the injection transistors. A compensation system including the use of DACs adjusts the bias voltage of the detector and reference resistors, and hence the bias currents of the detector and reference resistors according to the bias information stored in the external digital memory.

DACs supply the desired voltage value to the gate of the bias transistor. As demonstrated in Figure 2.11 and Figure 2.12, only a small portion of the DAC output range is used for biasing. While the PMOS injection transistor uses 200 mV portion of the 5 V output range, the NMOS injection transistor uses 250 mV portion of that range. Other analog outputs of a conventional DAC are not used by the circuit.

A nonuniformity compensation architecture using multiple analog buses is used in this design [65]. Figure 2.18 shows the DAC architecture for M readout channels. Two multi-level voltage generators are constructed by using a basic resistor array. The multi-level voltage generators have 64 analog voltage outputs. Two 64-level analog buses are extended along all readout channels. One analog voltage is selected from the analog bus through the transmission gate network which is controlled by digital gates. This selected analog voltage biases the injection transistor in order to set the bias current of the resistor.

The main advantage of this system is that the DAC output spans only the bias range, i.e., all the DAC input combination corresponds to a useful output voltage. This design, which has 64-level analog voltage output, is equivalent to a 6-bit DAC system that has a better output resolution than a conventional system that uses 10-bit DACs in the resistive microbolometer application.

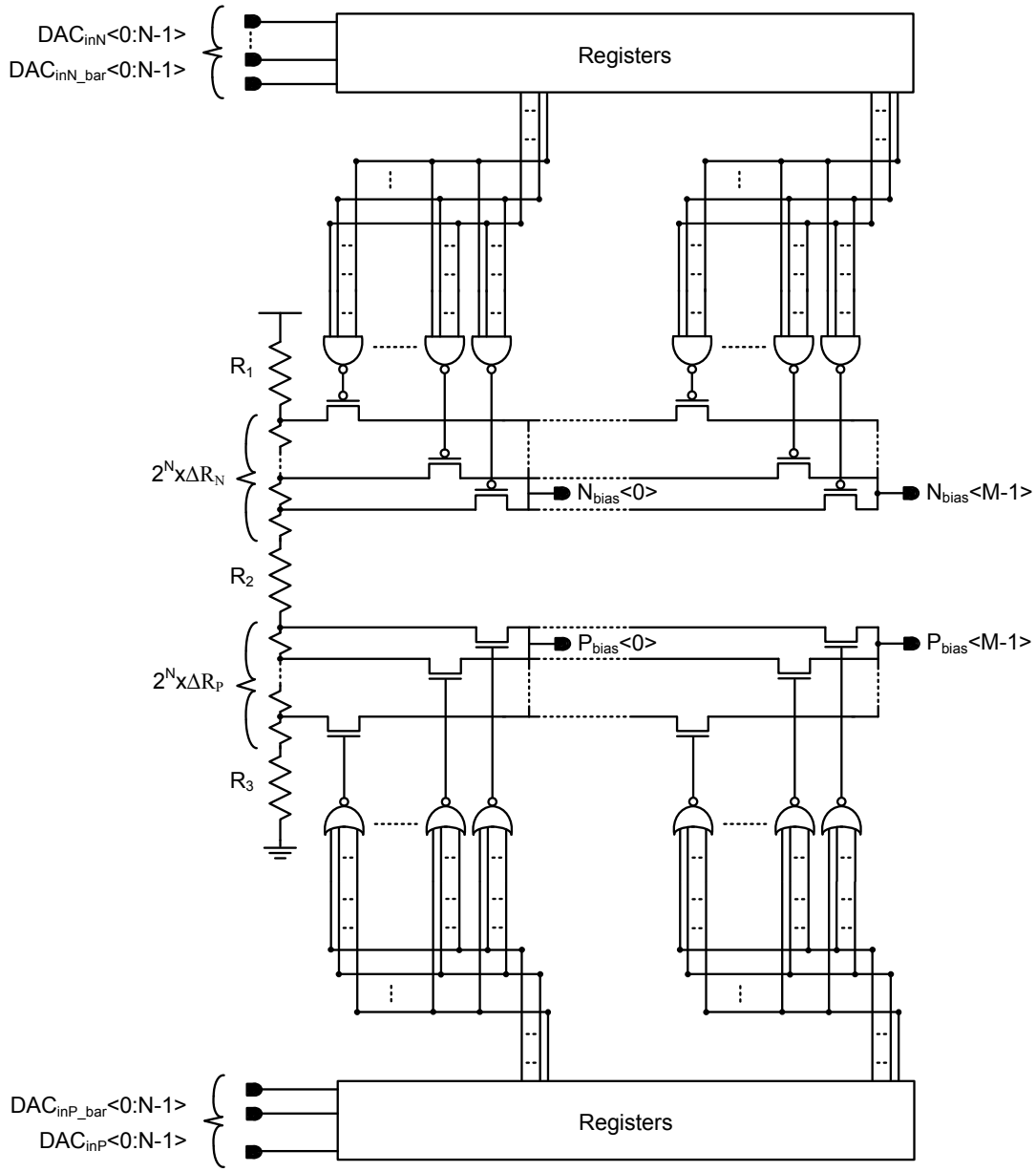


Figure 2.18: Simplified DAC architecture of the microbolometer readout circuit which has M readout channels. In the design, two 64-level analog buses are extended along all readout channels where one analog voltage is selected from the analog bus through the transmission gate network to bias each injection transistor of the CTIA.

Figure 2.19 shows the dependence of the maximum offset current for ±5% resistance nonuniformity and 80 KΩ nominal resistance values upon the total DAC resolution. The used architecture enhances the output offset current more than 4 bits. That is, a 5-bit new system works better than a 9-bit conventional system. However, in the new DAC architecture the circuit area is directly proportional to the square of the DAC resolution. Considering the area and the maximum offset current value, 6-bit DACs are used in the test circuit.

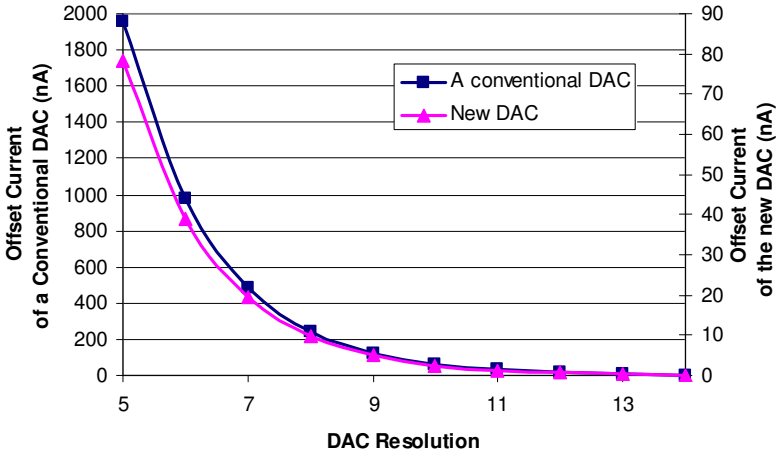


Figure 2.19: Dependence of the maximum offset current for ±5% resistance nonuniformity and 80 KΩ nominal resistance values upon the total DAC resolution.

The other advantages of the design are that the circuit dissipates low power and it has very low output noise. Since there is only one current flowing channel in the whole system, both low power dissipation and low output noise can be achieved by selecting the proper total DAC resistance value. Figure 2.20 shows the dependence of power dissipation and the thermal noise in 4 KHz electrical bandwidth upon the total DAC resistance. 5 KΩ is selected as the optimum value, considering the whole design. Here, the output noise is the thermal noise of 5 KΩ resistor. In fact, the actual output noise is less than this value, because the critical node is connected to both ground and supply voltage, and the effective resistance seen by that node

decreases. This noise value represents the upper limiting value where the resistance between the output node and supply voltage is equal to the resistance between the output node and ground.

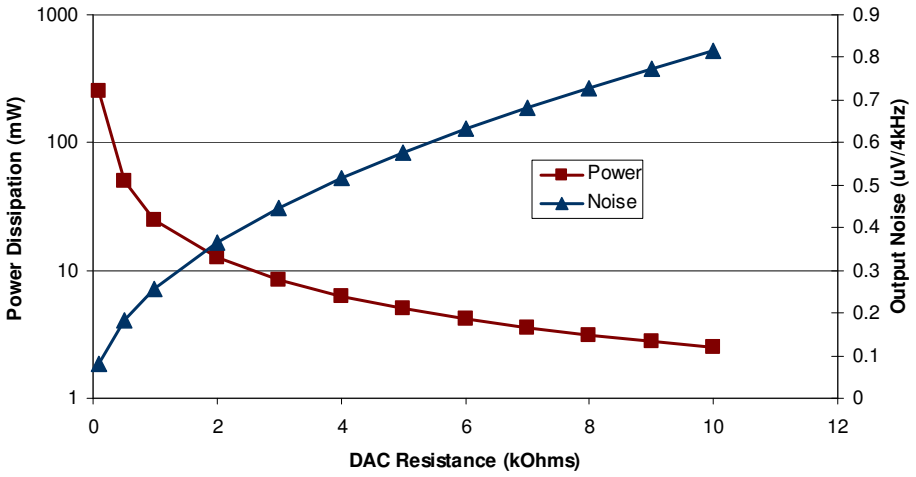


Figure 2.20: Dependence of power dissipation and thermal noise in 4 KHz electrical bandwidth upon the total DAC resistance. 5 KΩ is selected as the optimum value, considering the whole design.

After selecting 5 KΩ as the total DAC resistance, the resistor values in figure 2.16 become as follows: R_1=1095 Ω, R_2=1625 Ω, R_3=1705 Ω, ΔR_N=5 Ω, ΔR_P=4 Ω. The resistor array constructed by these resistors can generate the multi-level analog voltages to adjust the bias current of the detector and reference resistors to 25 µA for microbolometer resistors in the ±5% resistance nonuniformity range.

Figure 2.21 gives the simulation results for (a) the detector and (b) the reference currents with respect to compensation circuit control input for 76 KΩ, 80 KΩ, and 84 KΩ microbolometer resistors. Both the detector and reference currents can be adjusted with a resolution of around 40 nA by the compensation system.

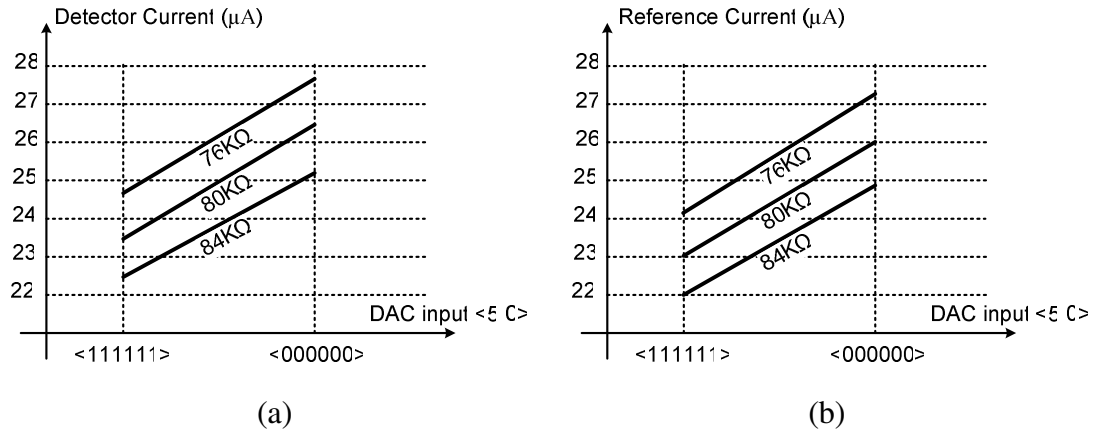


Figure 2.21: Simulated (a) detector and (b) reference currents with respect to DAC inputs. Both of currents can be adjusted with a resolution of 40 nA by DACs.

Noise contribution of these DACs to the readout circuit is very small. Since the total resistance of the voltage division circuit is much smaller than 80 KΩ microbolometer resistors, the thermal voltage noise of the compensation circuit is much smaller than noise of the detector and reference resistors. The rms simulated output current noise of the biasing circuit with compensation DACs 42.88 pA in an electrical bandwidth of 4 KHz where it is 39.62 pA without compensation DACs. Figure 2.22 shows the layout of two 6-bit input DACs. It measures 1278 μm x 311 μm in a 0.6 μm CMOS process.

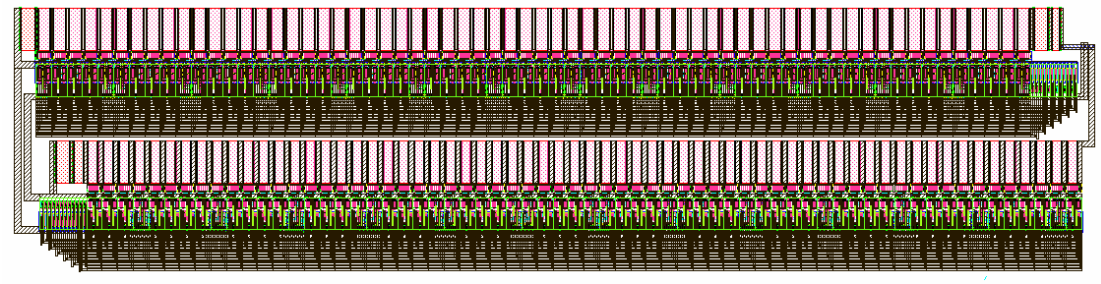


Figure 2.22: Layout of two DACs. The layout measures 1278 μm x 311 μm in a 0.6 μm CMOS process. The circuit which must be implemented in each readout channel of a microbolometer has an area of 1250μm x 180μm.

2.2.4. Operational Amplifier

An operational amplifier (opamp) is used both in the switched capacitor integrator and in the sample-and-hold circuit. This opamp should be low noise because input referred noise of the opamp induces a current noise which distorts the detector output current. Moreover, the opamp should dissipate low power, because each readout channel has two opamps and there are generally many readout channels in a large array format microbolometer chip. A three stage opamp with NMOS input differential pair is used to achieve these specifications, where the first two stages are differential which provide high common mode rejection ratio. Figure 2.23 shows the schematic of the opamp*.

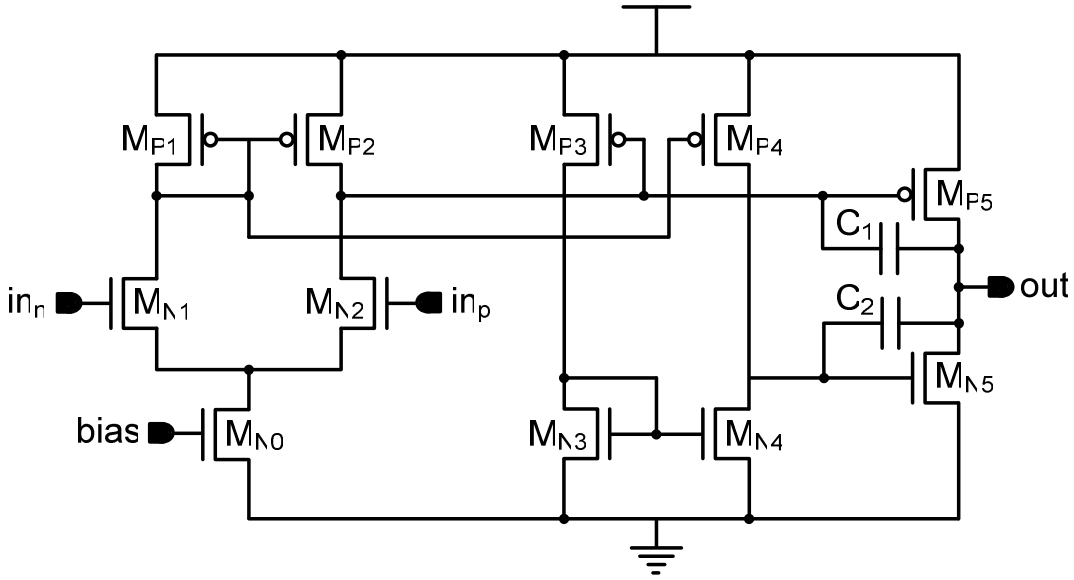


Figure 2.23: Schematic of the opamp used in the switched capacitor integrator and in the sample-and-hold circuit*.

* Schematic of the operational amplifier has been designed by Murat Tepegöz.

The main component of the input referred noise of the opamp is the noise of the first stage, because noise of the second and third stages is divided by the high gain of the first differential stage. The input referred noise power spectral density of the first stage is:

$$V^2_{eq,tot} = V^2_{eq,N1} + V^2_{eq,N2} + \frac{g^2_{m,P}}{g^2_{m,N}}\left(V^2_{eq,P1} + V^2_{eq,P2}\right) \tag{2.13}$$

where, V^2_{eq} is input referred noise power spectral density of a transistor, $g_{m,P}$ is the transconductance of M_{P1} and M_{P2} , and $g_{m,N}$ is the transconductance of M_{N1} and M_{N2}. The input referred noise power spectral density of a transistor is given as:

$$V^2_{eq} = 4kT\left(\frac{2}{3g_m}\right) + \frac{K_{1/f}}{WLC_{ox}}\frac{\Delta f}{f} \tag{2.14}$$

where, g_m is the transconductance of the transistor, C_{ox} is the unit area gate oxide capacitance of the transistor, W and L are the width and length of the transistor, f is the frequency, T is the absolute temperature, k is the Boltzman constant and $K_{1/f}$ is the Flicker noise constant of the transistor. Noise of the bias transistor, N_0, has no effect in the noise expression of the first stage of the opamp, because its noise is eliminated by the differential input stage. Therefore, total noise expression becomes as follows:

$$V^2_{eq,tot} = 8kT\left(\frac{2}{3g_{m,N}}\right) + \frac{2K_{1/f,N}}{(WL)_N C_{ox}}\frac{\Delta f}{f} + \frac{g^2_{m,P}}{g^2_{m,N}}\left[8kT\left(\frac{2}{3g_{m,P}}\right) + \frac{2K_{1/f,P}}{(WL)_P C_{ox}}\frac{\Delta f}{f}\right] \tag{2.15}$$

where, $g_{m,N}=g_{m,N1}=g_{m,N2}$ and $g_{m,P}=g_{m,P1}=g_{m,P2}$. In order to minimize the input referred noise of the opamp, $g_{m,N}$ and $(WL)_N$ should be as large as possible and $g_{m,P}$ should be small. $(WL)_P$ is not so critical, because it is divided by the square of the transconductance of the input transistors. The aspect ratios and the number of gates of the transistors are given in Table 2.3. Compensation capacitors C_1 and C_2 are 3 pF and 1 pF, respectively.

Table 2.3: Aspect ratios and number of gates of the transistors in the opamp.

Transistors	Aspect Ratio (μm/μm)	Number of Gates
M_{N0}	60/6	2
M_{N1}, M_{N2}	90/6	3
M_{N3}, M_{N4}	12/3	1
M_{N5}	160/3	4
M_{P1}, M_{P2}, M_{P3}, M_{P4}	16/3	2
M_{P5}	180/3	4

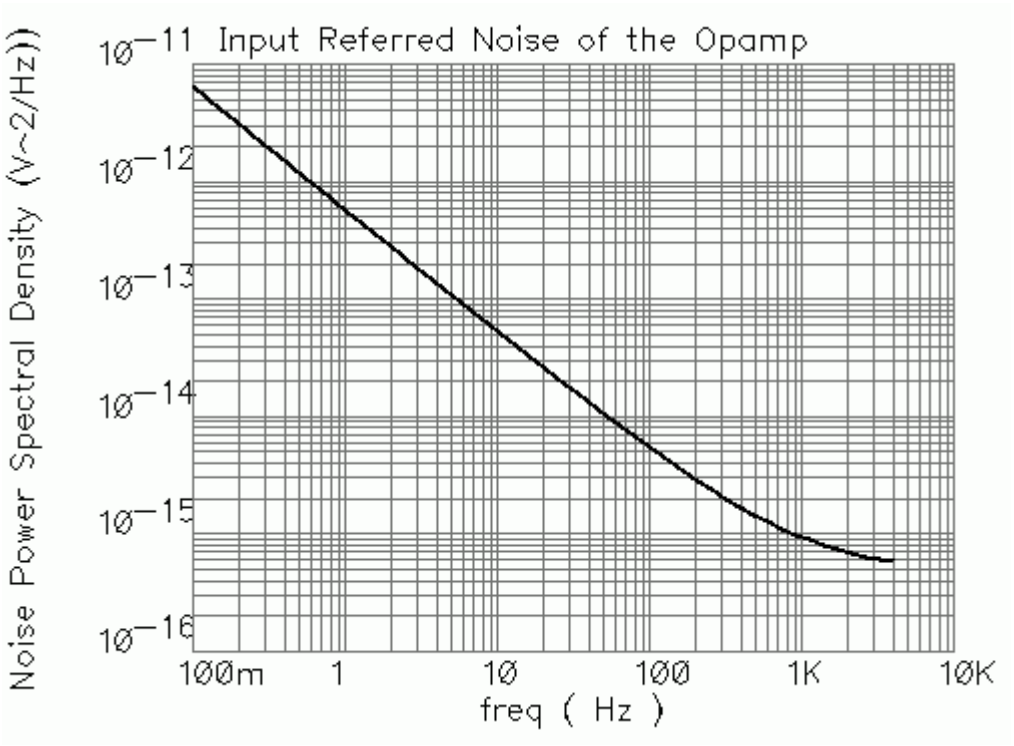


Figure 2.24: Simulated noise power spectral density of the opamp. The rms input referred voltage noise is 2.74 μV in an electrical bandwidth of 4 KHz.

Figure 2.24 shows the simulated input referred noise power spectral density of the opamp. The rms input referred voltage noise is 2.74 μV in an electrical bandwidth of 4 KHz. By dividing this value to the output resistance of the first part of the CTIA, rms current noise of 0.1-0.2 pA is obtained, which is much smaller than rms output noise current of the biasing circuit of the CTIA.

Figure 2.25 shows the AC simulation results of the opamp. The differential open loop gain is 114.7 dB, the phase margin is 72.1°, the gain margin is -18.7 dB, and the unity gain frequency with 1 pF load is 2.92 MHz.

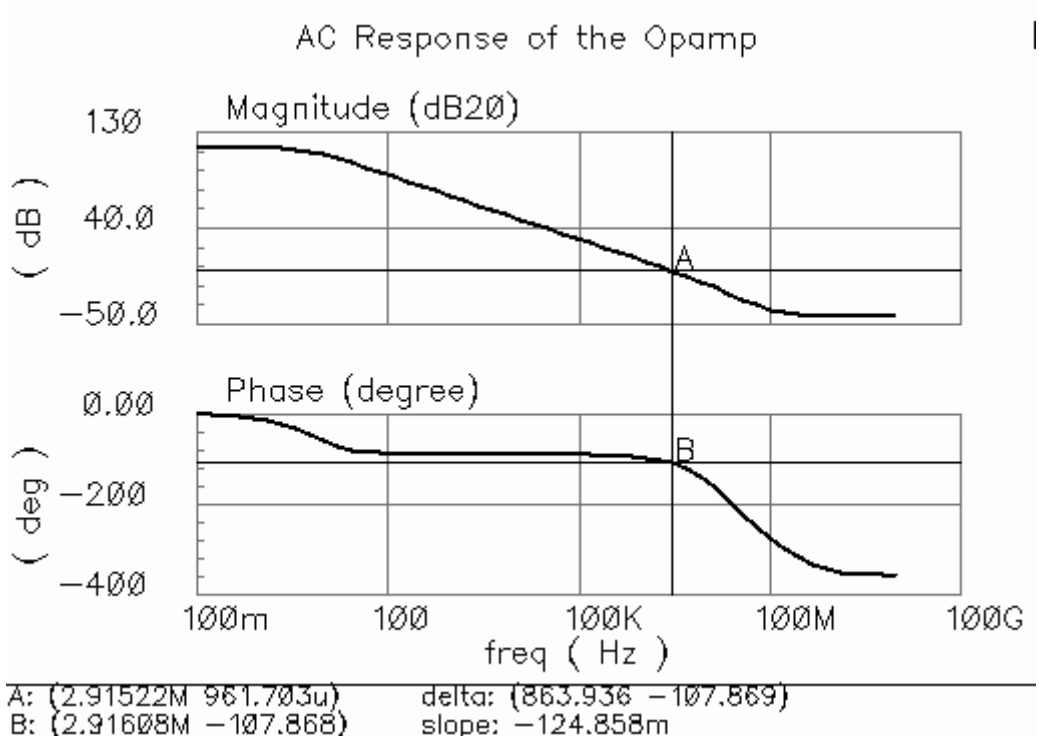


Figure 2.25: Simulated AC response of opamp. The differential open loop gain is 114.7 dB, the phase margin is 72.1°, the gain margin is -18.7 dB, and the unity gain frequency with 1 pF load is 2.92 MHz.

Figure 2.26 shows the output resistance of the opamp. It is around 10 Ω for frequencies larger than 25 Hz. Figure 2.27 shows the transient response of the opamp in a buffered connection. The slew rate is measured 2.15 V/µs for high-to-low transition and 2.20 V/µs for low-to-high transition. This slew rate is high enough in the switched capacitor integrator and sample-and-hold circuit applications of the opamp. Figure 2.28 shows the input offset voltage of the opamp. The offset voltage is 88 nV at 2.5 V DC point which is reasonably small. Also offset cancellation techniques are used both in the switched capacitor integrator and in the sample-and-hold circuit. Finally, Table 2.4 summarizes the simulation results of the schematic and layout of the opamp.

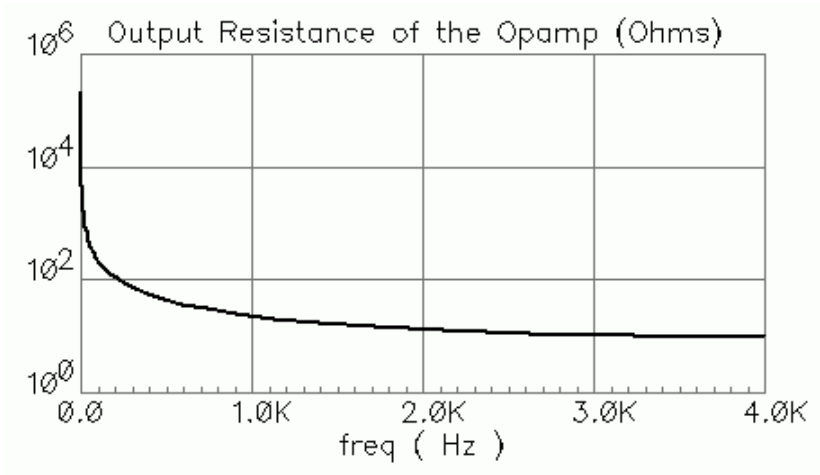


Figure 2.26: Simulated output resistance of the opamp. Output resistance is around 10 Ω for frequencies larger than 25 Hz.

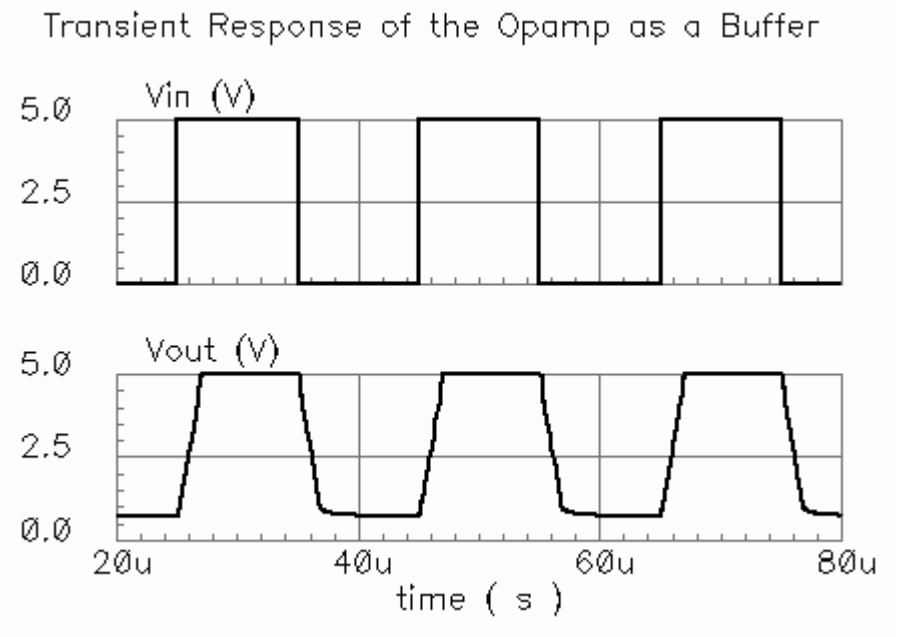


Figure 2.27: **S**imulated transient response of the opamp in a buffered connection. The slew rate is measured 2.15 V/µs for high-to-low transition and 2.20 V/µs for low-to-high transition, which are high enough in the switched capacitor integrator and sample-and-hold circuit applications of the opamp.

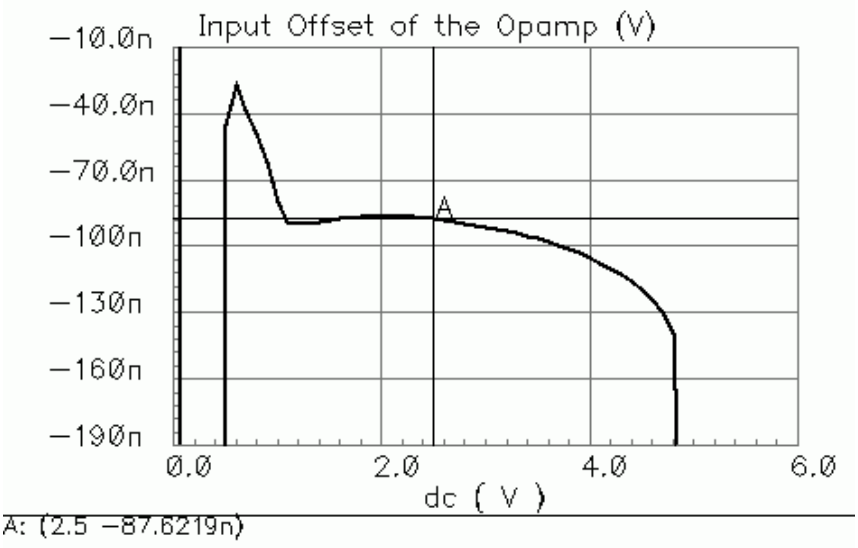


Figure 2.28: Simulated input offset voltage of the opamp. The offset voltage is 88 nV at 2.5 V DC point.

Table 2.4: Simulation summary of the schematic and layout of the opamp.

	Schematic of the opamp	**Layout of the opamp**
Power Dissipation	304 µW	302 µW
Open Loop Gain	109.6 dB	114.7 dB
Phase Margin	70.4°	72.1°
Gain Margin	-20.3 dB	-18.7 dB
Unity Gain Frequency	2.70 MHz (1 pF load)	2.92 MHz (1 pF load)
Slew Rate	2.30 V/µs (5V – 1V) 2.35 V/µs (1V – 5V)	2.15 V/µs (5V – 1V) 2.20 V/µs (1V – 5V)
Input Referred Noise	2.70 μV_{rms} (4 KHz BW) 3.64 μV_{rms} (16 KHz BW)	2.74 μV_{rms} (4 KHz BW) 3.70 μV_{rms} (16 KHz BW)
Output Resistance	8.5 Ω (at 4 KHz)	9.5 Ω (at 4 KHz)
Input Offset	130 nV (2.5V DC point)	88 nV (2.5V DC point)

Figure 2.29 shows the layout of the opamp. It measures 162 µm x 75 µm in a 0.6 µm CMOS process.

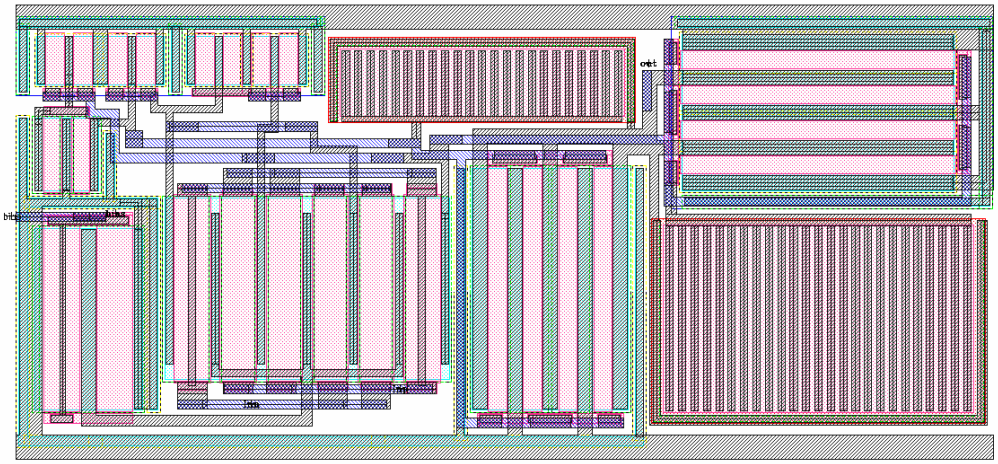


Figure 2.29: The layout of the opamp. It measures 162 µm x 75 µm in a 0.6 µm CMOS process.

2.2.5. Switched Capacitor Integrator

A switched capacitor integrator (SCI) which constructs the main part of the CTIA follows the detector and reference biasing circuit. While Figure 2.1 shows a simple SCI, Figure 2.30 shows the SCI with offset cancellation capability which is used in the design. The circuit consists of an opamp, 10 pF integration capacitor and five minimum size CMOS switches with dummy side transistors.

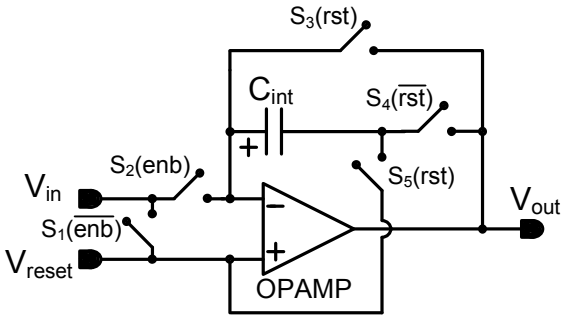


Figure 2.30: Schematic of the switched capacitor integrator.

The circuit needs two non-overlapping control signals *rst* and *enb* which are shown in Figure 2.31. Switches S_1 and S_2 are controlled by the *enb* signal and switches S_3-S_5 are controlled by the *rst* signal. Basically, the circuit firstly resets the output and then integrates the detector current. After the signal integration and before the next reset, the output of the SCI is sampled by the sample-and-hold circuit which follows the CTIA in the readout channel.

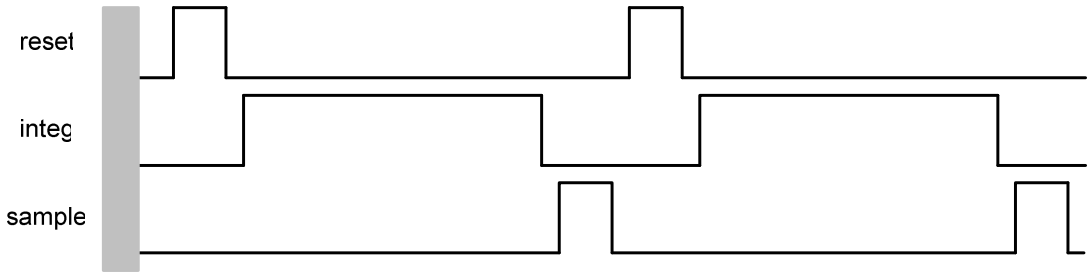


Figure 2.31: Illustrated timing of the *rst* (reset) and *enb* (integ) signals. After the signal integration, and before the next reset, the output of the SCI is sampled by the sample-and-hold circuit

Figure 2.32 gives the schematic of the SCI during reset phase. During this phase, the switches S1, S3, and S5 are closed. The input is connected to the reset voltage, V_{reset}. The offset voltage of the opamp, V_{offset}, is stored as the initial voltage in the integration capacitor, C_{int}. With this configuration, the opamp is in the unity gain buffer mode and the input is isolated from the op-amp, and the capacitor is disconnected from the output.

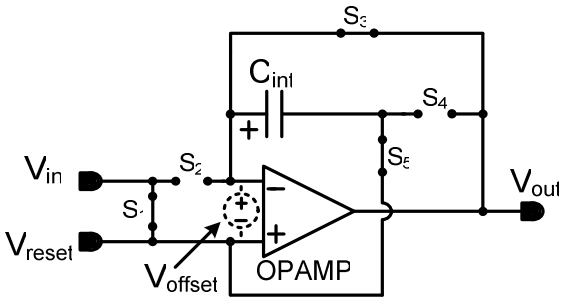


Figure 2.32: Schematic of the SCI when the reset signal is high.

During this phase, the capacitor and output voltages can be expressed as:

$$V_C = V_{reset} + V_{offset} - V_{reset} = V_{offset} \tag{2.16}$$

$$V_{out} = V_{reset} + V_{offset} \tag{2.17}$$

where, V_{offset} is the input offset voltage of the opamp, and V_C is the capacitor voltage. In the reset phase, offset voltage of the opamp is stored in the integration capacitor.

Figure 2.33 shows the schematic of the SCI during the integration phase when switches S2 and S4 are closed. During this phase, the SCI integrates the input current which is coming from the detector and reference biasing circuit.

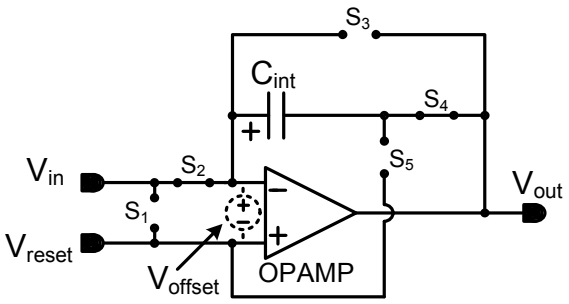


Figure 2.33: Schematic of the SCI when the integration signal is high.

During this phase, the output voltage of the SCI is equal to:

$$V_{out}(t) = V_{-} - V_C(t) = V_{reset} + V_{offset} - V_C(t) \tag{2.18}$$

$$V_C(t) = V_C(t_{initial}) + \frac{1}{C_{\text{int}}} \int_{t_{initial}}^{t} i_{in}(t)dt \tag{2.19}$$

$$V_C(t_{initial}) = V_{offset} \tag{2.20}$$

$$V_{out}(t) = V_{reset} - \frac{1}{C_{\text{int}}} \int_{t_{initial}}^{t} i_{in}(t)dt \tag{2.21}$$

where, V_{-} is the voltage at the inverting input of the opamp, C_{int} is the integration capacitance, and i_{in} is the current coming from the detector and reference biasing

circuit. The output voltage is independent of the offset voltage of the opamp, proving the offset capability of the SCI.

If the input current of the integrator is constant, the output current of the detector and reference biasing circuit, the output voltage of the SCI becomes as follows:

$$V_{out} = V_{reset} - \frac{T_{\text{int}}}{C_{\text{int}}} I_{out} \tag{2.22}$$

where, T_{int} is the signal integration time and I_{out} is the output current of the detector and reference biasing circuit. Thus, the gain of the SCI (A_{SCI}) is:

$$A_{SCI} = -\frac{T_{\text{int}}}{C_{\text{int}}} \tag{2.23}$$

The output current of the biasing circuit includes the offset current due to resistance nonuniformity, the self heating current, and the infrared induced current. This self heating current can be modeled as a ramping current [51] for low thermal conductance detectors with short duration of integration times which is the general case for microbolometers. Figure 2.34 shows the cancellation of self heating current by removing its DC part [51]. If there is no infrared induced current, SCI output is equal to the reset voltage at the end of signal integration. The current due to infrared radiation shifts the detector current and changes the SCI output voltage at the end of signal integration. In this method, the DC portion of the self heating current is removed with the nonuniformity offset current by compensation DACs.

Figure 2.35 shows the simulation result of the SCI when 20 nA constant input current is integrated. The gain of the amplifier is 1.22×10^7, which is equal to the ratio of integration time, 122 μs, to the integration capacitance, 10 pF.

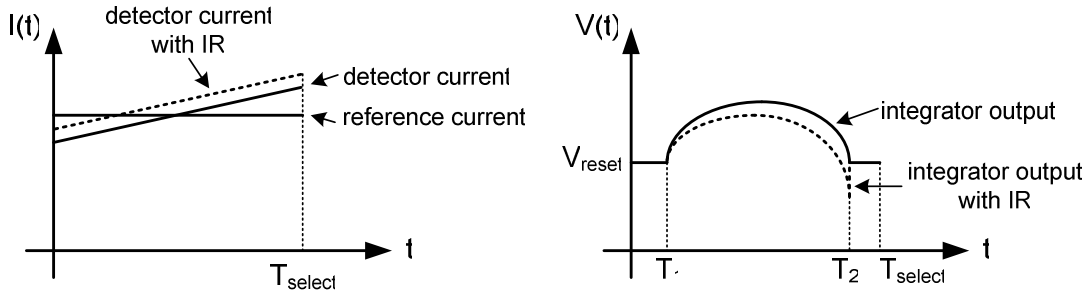


Figure 2.34: Cancellation of self heating current by removing its DC part [51]. The output current of the biasing circuit, which is the difference of the detector and reference currents, is integrated by the SCI, the output of which indicates the amount of infrared radiation.

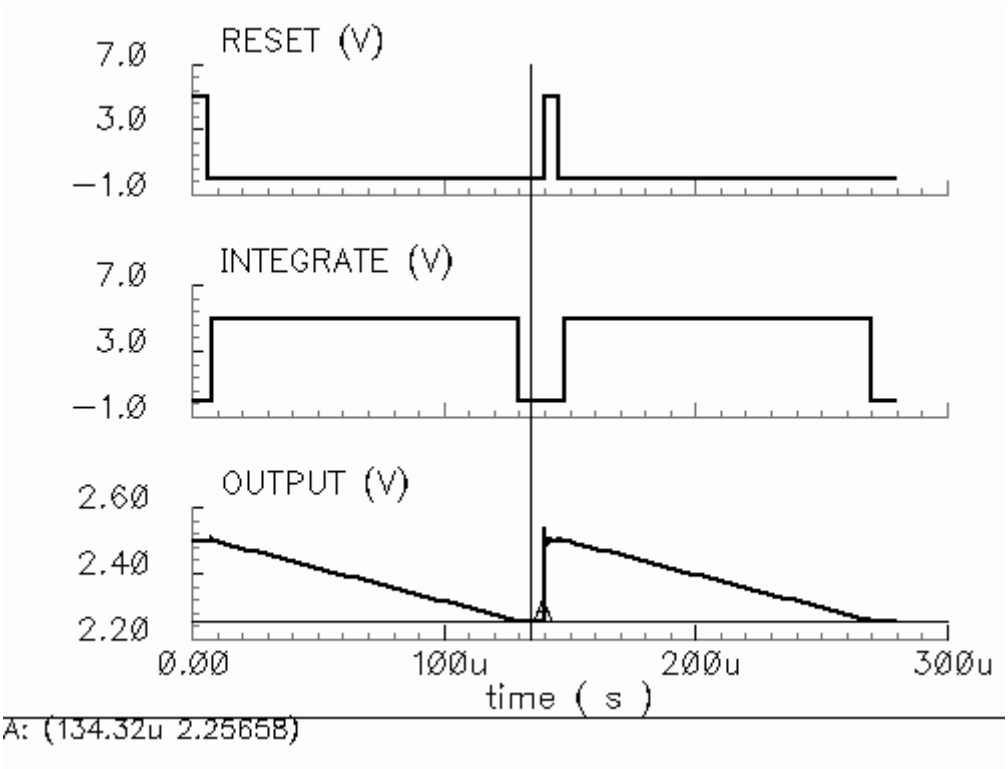


Figure 2.35: Simulation result of the SCI when 20 nA constant input current is integrated. During the *reset* phase, the output is tied to V_{reset}, which is equal to $V_{DD}/2$, and during the *integrate* phase the circuit integrates the input current.

Figure 2.36 gives the integrator output for different input current levels ranging from 50 nA to 250 nA with 50 nA increments. The gain is constant for each input current magnitude. However, when the magnitude of the input current is high output voltage can saturate at ground voltage.

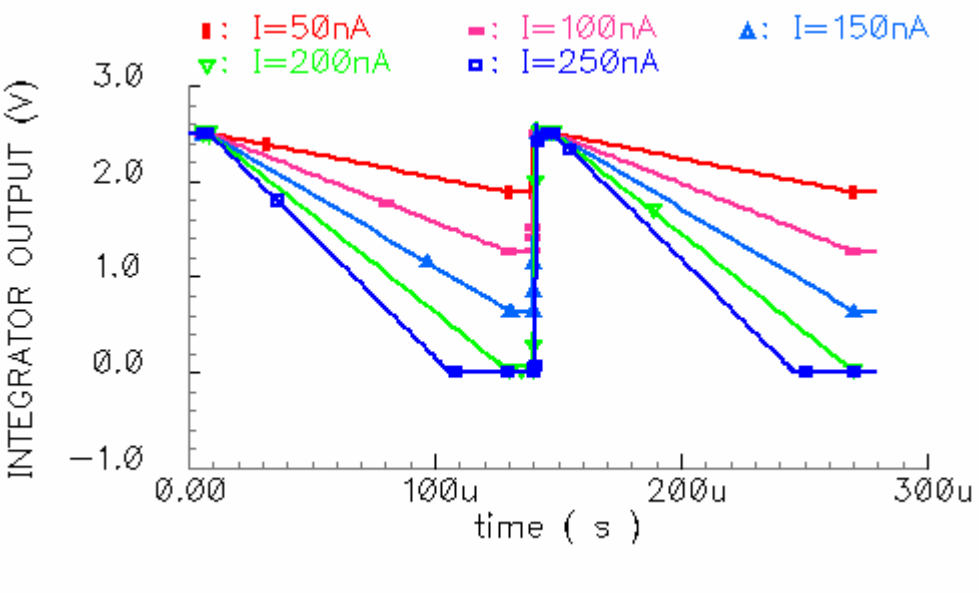


Figure 2.36: Output of the integrator for different input current levels ranging from 50 nA to 250 nA with 50 nA increments.

Figure 2.37 gives the simulation result of the SCI for time-varying input signals. In this case, the integrator output waveform becomes nonlinear. The first two cycles of the SCI output represent the detector current with uncompensated self-heating mechanism, while the last two cycles represent the detector current with compensated self-heating mechanism. Therefore, with a self heating cancellation mechanism, smaller dynamic range of the integrator is used which allows increasing the gain of the SCI without saturation of the integration capacitor.

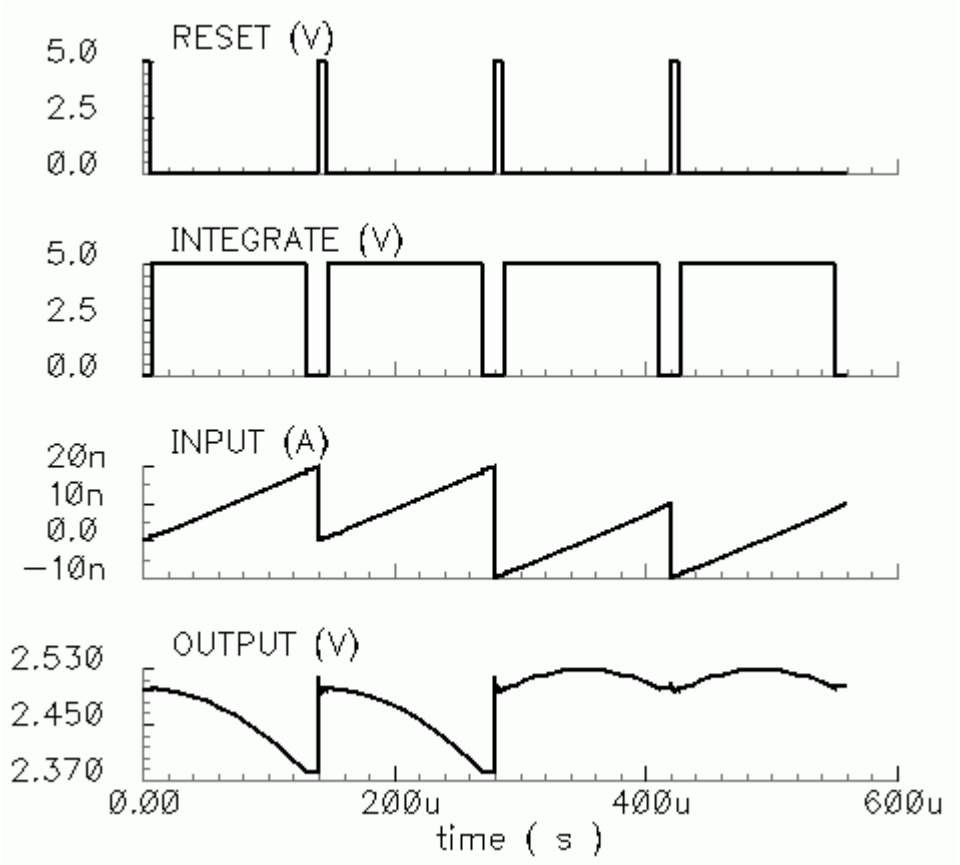


Figure 2.37: The timing, input, and output signals of the integrator for a typical microbolometer application. Integrator output becomes nonlinear due to time-varying input currents. The first two cycles represent the detector current with uncompensated self-heating mechanism, while the last two cycles represent the detector current with compensated self-heating mechanism.

2.2.6. Sample-and-Hold Circuit

The sample-and-hold (S&H) circuit is connected to the output of the SCI in order to sample the integrator output so that the integrator output will be stored and the stored voltage can be multiplexed to the output or readout by an analog-to-digital converter (ADC), even when the integrator completely loses the output voltage and starts to integrate the next detector. While Figure 2.1 includes a simple S&H circuit, Figure

2.38 shows the S&H circuit with unity gain and offset cancellation capability which is used in the design. The circuit consists of an opamp, 10 pF sampling capacitor and three minimum size CMOS switches with dummy side transistors. These switches are controlled by three timing signals, which are *sample* signal, its delayed version, and the complement of the delayed signal. Timing of the *sample* signal is illustrated in Figure 2.31 along with the SCI control signals.

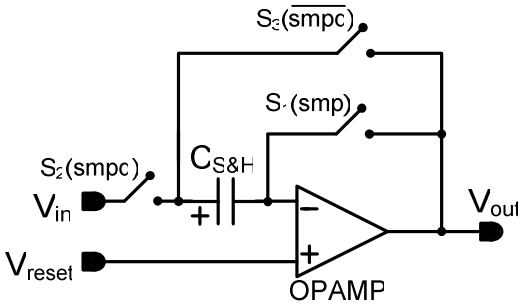


Figure 2.38: Schematic of the sample-and-hold circuit.

Figure 2.39 gives the schematic of the S&H circuit when *smp* signal is high. At this phase, switches S1 and S2 are closed and the capacitor and output voltages can be written as:

$$V_C = V_{in} - V_{reset} - V_{offset} \tag{2.24}$$

$$V_{out} = V_{reset} + V_{offset} \tag{2.25}$$

where, V_{reset} is the reset voltage of the S&H circuit and V_{offset} is the offset voltage of the opamp.

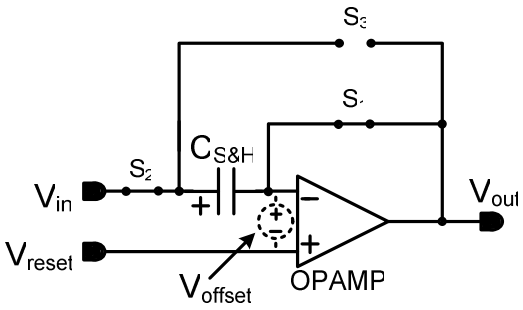


Figure 2.39: Schematic of the sample-and-hold circuit when the *smp* signal is high.

Figure 2.40 shows the schematic of the S&H during *smp* signal is low. At this phase, only S3 is closed and the capacitor and output voltages are equal to:

$$V_C = V_{in} - V_{reset} - V_{offset} \tag{2.26}$$

$$V_{out} = V_{reset} + V_{offset} + V_C = V_{in} \tag{2.27}$$

Therefore, the output voltage follows the input with unity gain and independent of the offset voltage of the opamp.

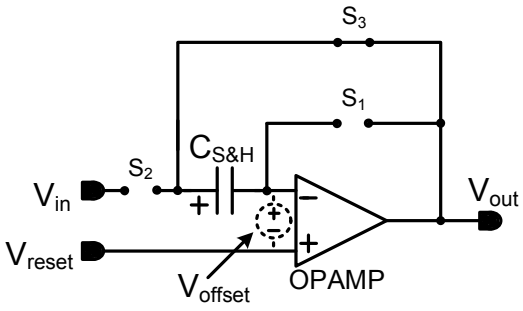


Figure 2.40: Schematic of the sample-and-hold circuit when the *smp* signal is high.

Figure 2.41shows the simulation result of the S&H circuit when a 2 KHz sinusoidal signal is applied to the input of the circuit. The circuit samples the input signal at every negative edge of the sample signal.

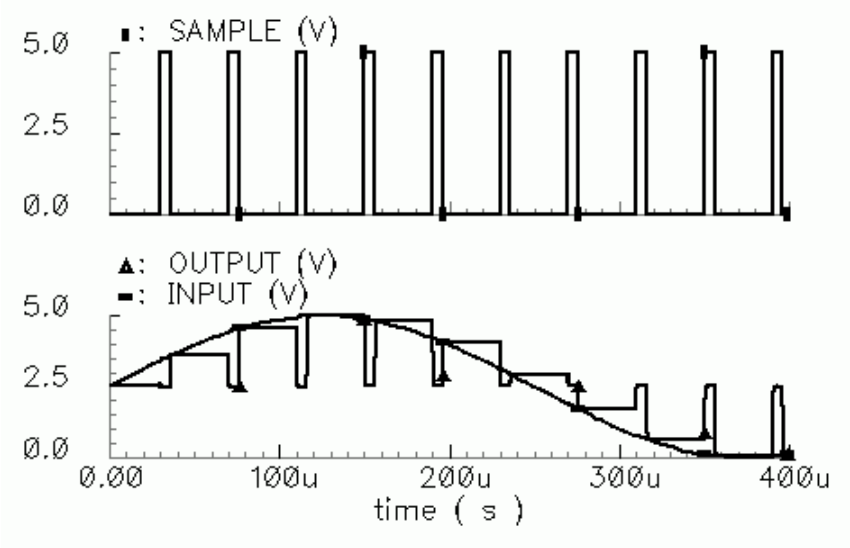


Figure 2.41: Control, input, and output signals of the sample-and-hold circuit.

Figure 2.42 shows the layout of SCI and S&H circuits and digital circuits. The layout measures 415 µm x 215 µm. The layout of digital circuits consisting of SCI and S&H switches and buffers of timing signals measures 348 µm x 110 µm. Digital units are isolated from analog parts by guarding them with substrate and n-well contacts.

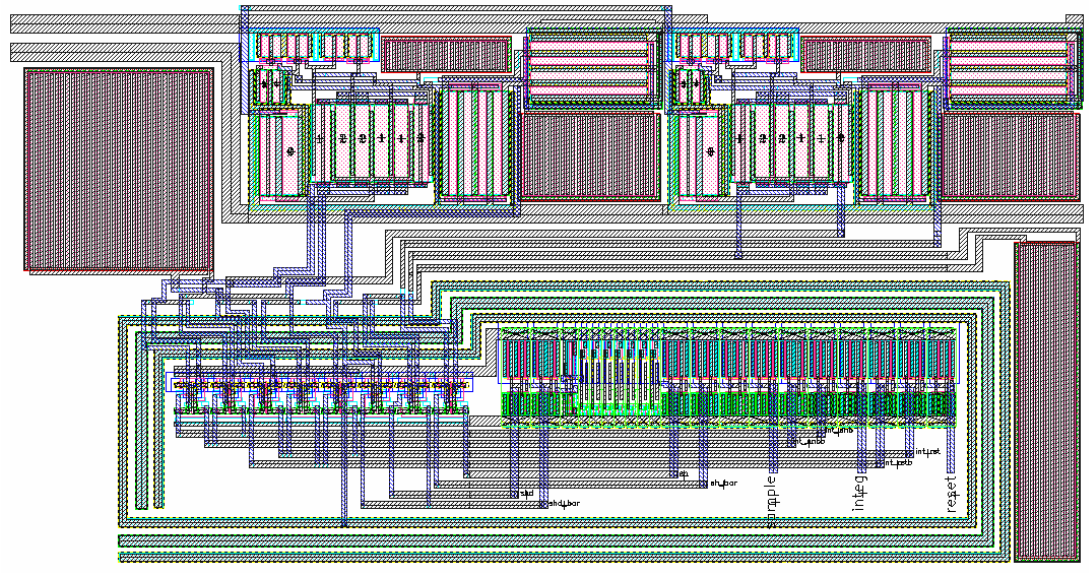


Figure 2.42: The layout of SCI and S&H circuits and digital circuits. The layout measures 415 µm x 215 µm.

2.3. Overall Design

A readout channel including a CTIA, a switched capacitor integrator, a sample-and-hold circuit, two compensation DACs, and digital buffers for control signals is implemented by a standard 0.6 µm 5 V CMOS process. Figure 2.43 shows the overall simplified schematic where the resolution of DACs (N) is 6 and the nominal resistance of the detector and reference resistors is 80 KΩ. In order to test the circuit for resistance nonuniformity, two resistor arrays with 16 resistors between 76 KΩ and 84 KΩ are implemented for the detector and reference resistors.

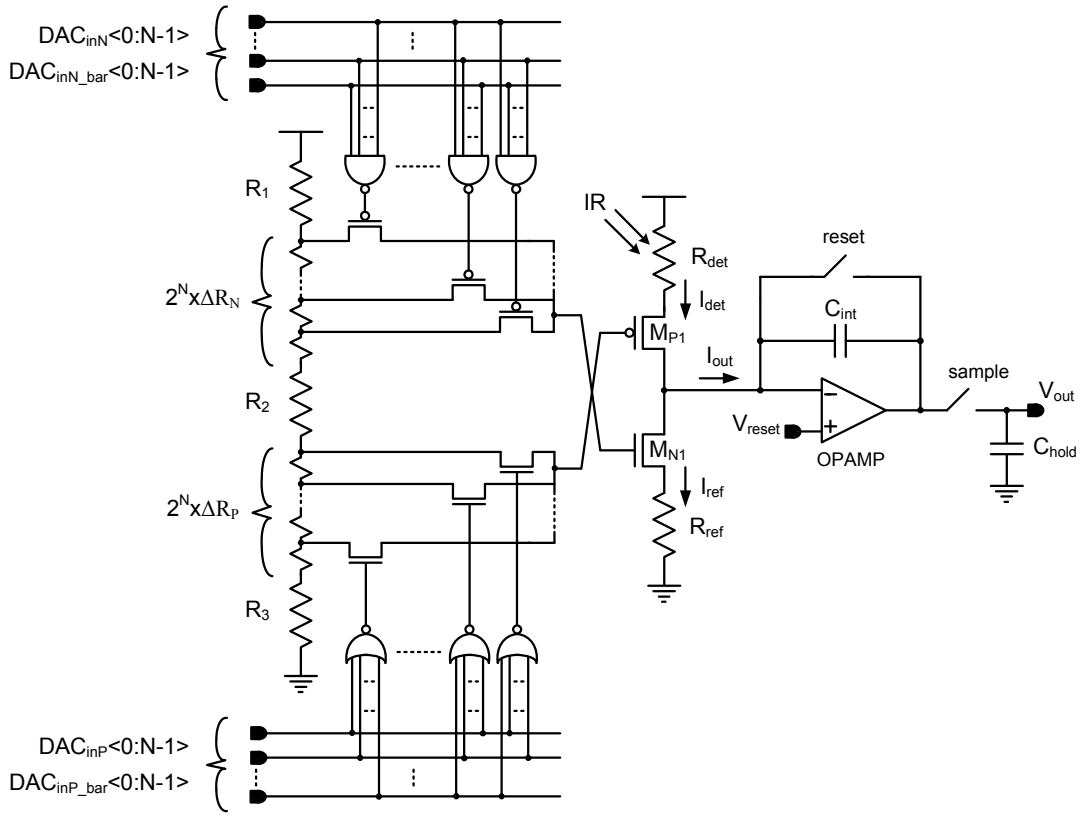


Figure 2.43: Simplified schematic of the test circuit including a CTIA, a sample-and-hold circuit, two compensation DACs. For simplicity, digital buffers for control signals are not shown in the figure.

Figure 2.44 shows the floor plan and pad frame of the CTIA type resistive microbolometer readout test chip where the place of two compensation DACs, two resistor arrays, the CTIA, the SCI, the S&H circuit, and digital buffers are shown. Figure 2.45 shows the complete layout of the chip, which measures 2079 µm x 974 µm (2 mm^2) in a 2-metal/2-poly CMOS process. Figure 2.46 shows the picture of the fabricated chip.

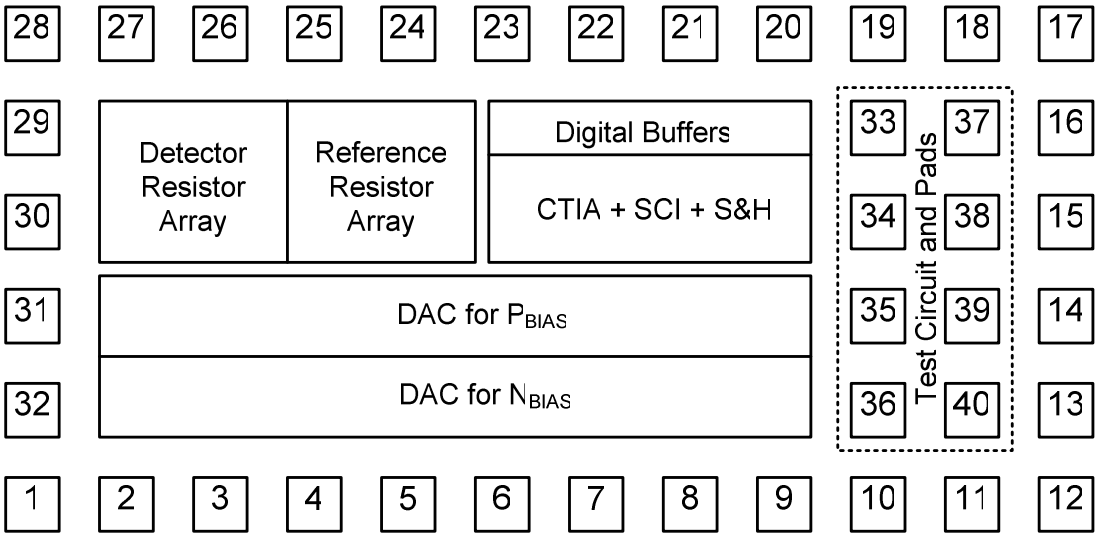


Figure 2.44: Floor plan and pad frame of the chip.

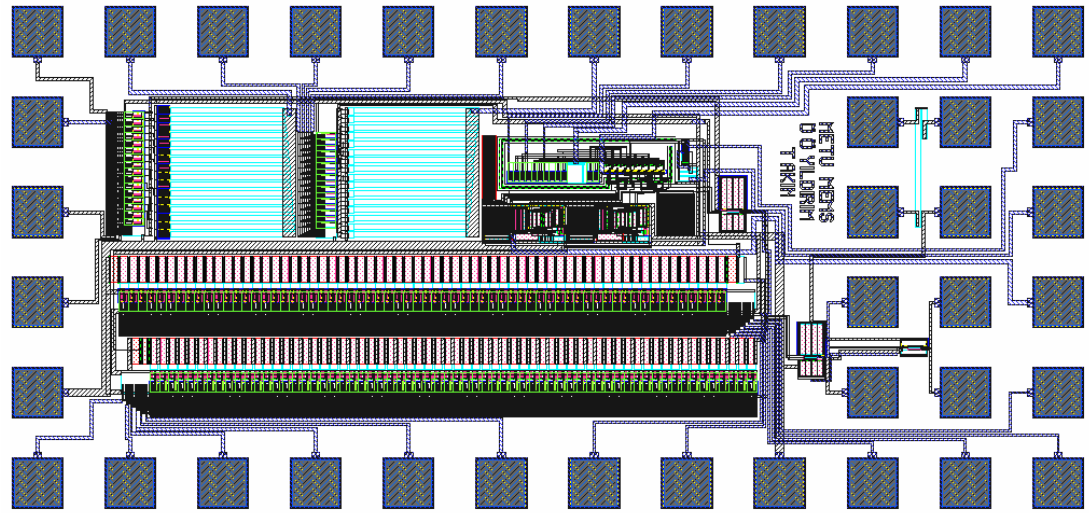


Figure 2.45: Layout of the whole chip which measures 2079 µm x 974 µm (2 mm^2) in a 2-metal/2-poly CMOS process.

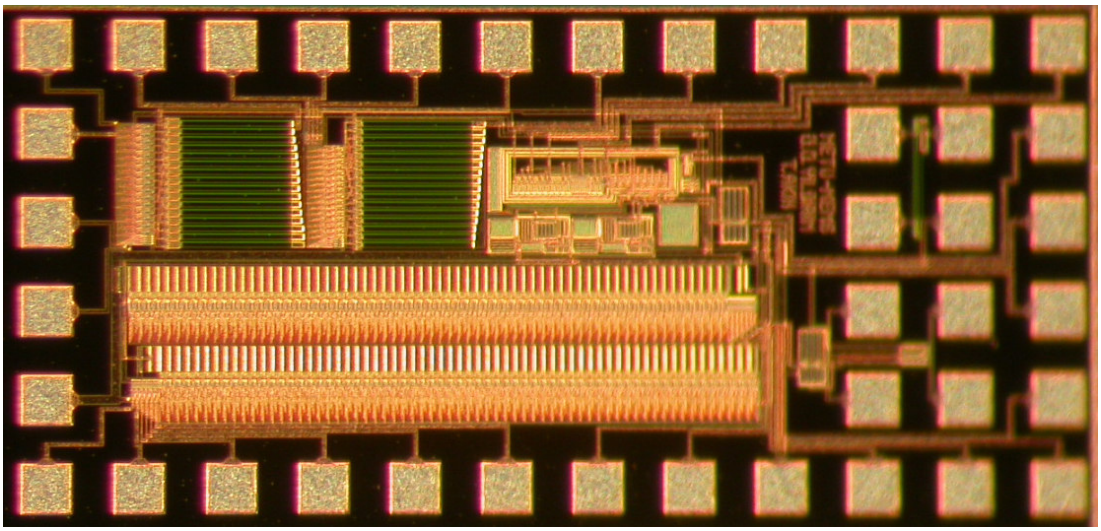
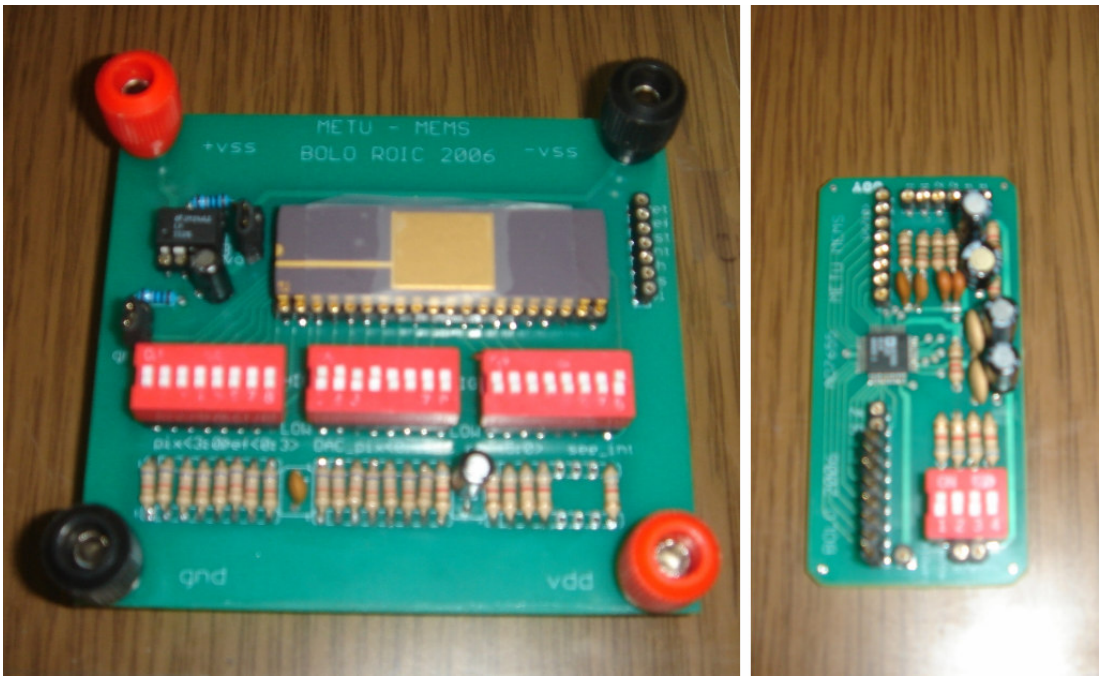


Figure 2.46: Picture of the fabricated chip.

2.4. Test Results

This section gives test results of the fabricated readout chip. As well as verifying the functionally of the circuit, performance parameters including nonuniformity compensation capability and noise of the circuit are measured. A two-layer printed circuit board (PCB) is prepared in order to test the circuit, and a discrete amplifier card is designed for noise measurement. Finally, a 16-bit analog-to-digital converter (ADC) card is prepared for measuring the noise performance of the overall circuit. Figure 2.47 shows the pictures of the test PCB and ADC card.



(a) (b)

Figure 2.47: Pictures of (a) the two-layer printed circuit board for test measurements of the readout chip and (b) the 16-bit ADC card.

2.4.1. Test of Timing Signals

Timing signals of the circuit are generated by a XILINX FPGA circuit board. Figure **2.48** shows the illustrated timing for the FPGA output signals. High phases of *reset* and *sample* signals should be at least 4 µs long in order to guarantee proper operation of the opamp. Moreover, there should be a time period of 1-2 µs between pulses in order to prevent overlapping of signals. The FPGA generates digital signals with 0 V low voltage level and 3.3 V high voltage level, which are compatible with the used 5 V CMOS process.

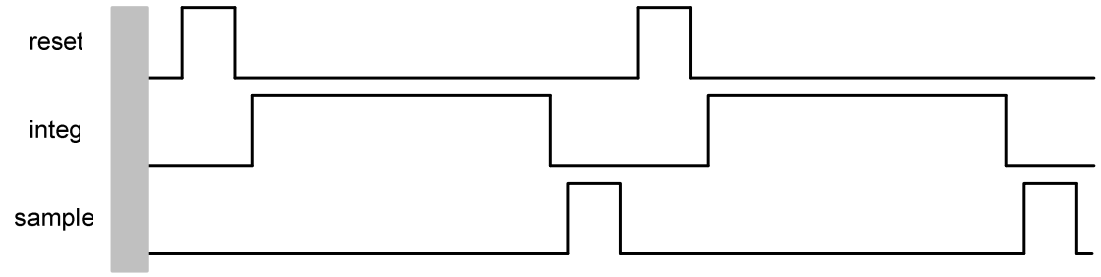


Figure 2.48: Illustrated timing for the FPGA output signals. High phases of *reset* and *sample* signals should be at least 4 µs long in order to guarantee proper operation of the opamp. Moreover, there should be a time period of 1-2 µs between pulses in order to prevent overlapping of signals.

Figure 2.49 and Figure 2.50 gives XILINX simulation results of the designed timing circuit. The timing circuit includes a 16-bit counter, a combinational circuit, and a sampling circuit, which eliminates glitches of the output. Figure 2.49 shows the clock signal and 5 least significant bits of the counter. Figure 2.50 shows the digital control signals, where SGN1, SGN2, and SGN3 represent *reset, integrate*, and *sample* signals, respectively. SGN16, SGN8, and SGN9 represent the same signals for a longer integration time.

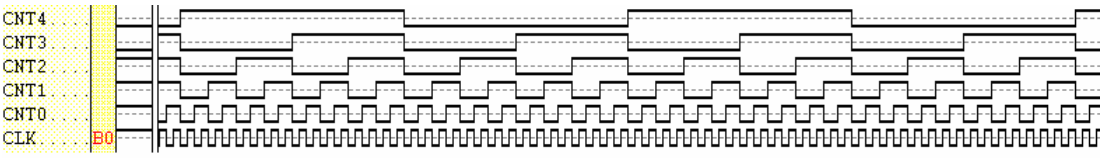


Figure 2.49: XILINX simulation results that show 5 least significant bits of the 16-bit counter which is used to generate digital control signals.

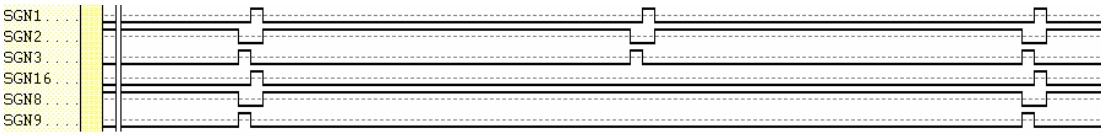


Figure 2.50: XILINX simulation results that show digital control signals: *reset, integrate*, and *sample* for short and long integration modes.

Figure 2.51 gives the scope view that shows 4 least significant bits of the counter, and Figure 2.52 shows digital control signals, *reset, integrate*, and *sample* for short and long integration times, which are 195 µs and 410 µs, respectively. Finally, Figure 2.53 shows the analog-to-digital converter (ADC) sampling signal, *ADC*, along with *reset, integrate*, and *sample* signals.

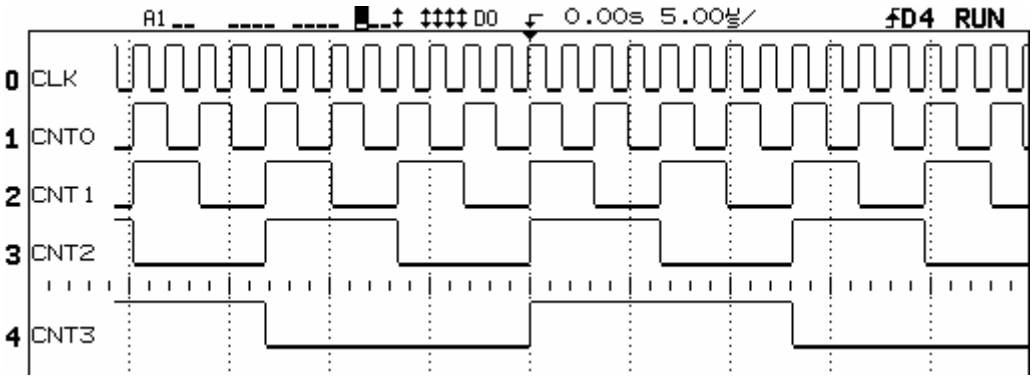


Figure 2.51: Scope view that shows 4 least significant bits of the counter

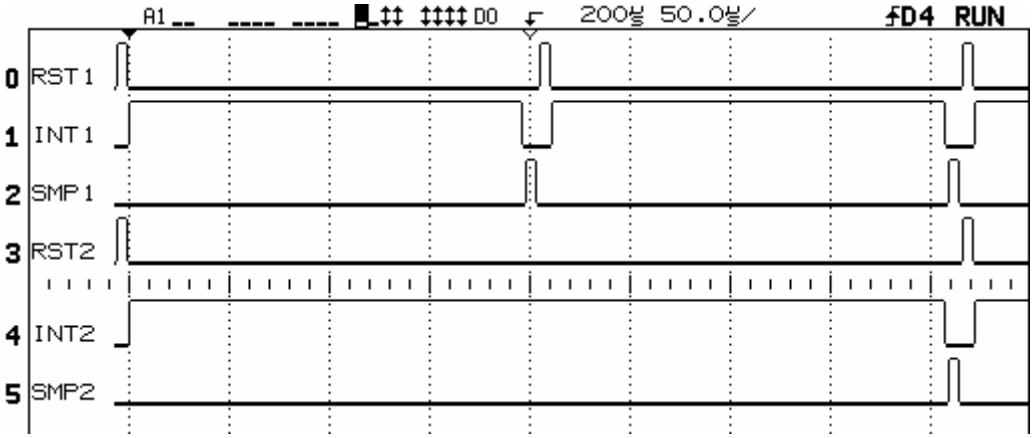


Figure 2.52: Scope view that shows digital control signals, *reset, integrate*, and *sample* for short and long integration times, which are 195 µs and 410 µs, respectively.

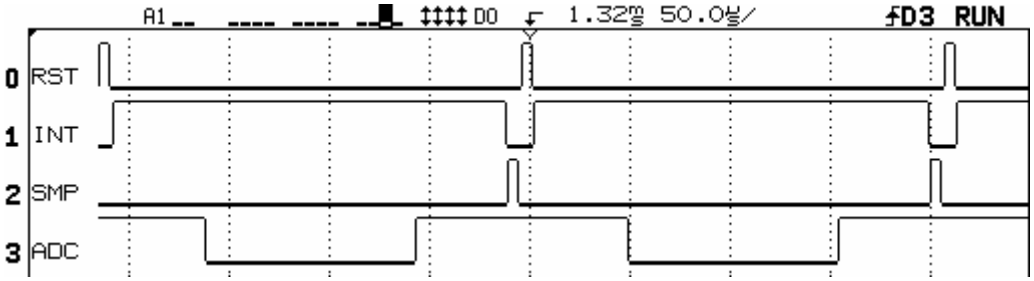


Figure 2.53: Scope view that shows the ADC sampling signal along with *reset, integrate*, and *sample* signals.

2.4.2. Test of Analog Blocks

Analog blocks of the fabricated chip including the biasing circuit with compensation DACs, the CTIA, and the S&H circuit are tested for different detector and reference resistance values and DAC inputs.

2.4.2.1. Transient Simulation of the Biasing Circuit and Compensation DACs

Figure 2.54 shows the measured detector current with respect to compensation circuit control input for 76 KΩ, 80 KΩ, and 84 KΩ detector resistors. The detector current is the highest for 76 KΩ for a fixed DAC input as expected. The detector current can be adjusted with a resolution of less than 50 nA by the compensation structure, which corresponds to more than 50 times current compensation, considering the peak-to-peak variation in the current is around 2.51 μA for ±5% resistance nonuniformity. Measured current values are slightly higher than simulation values because the high resistive poly layer which is used to implement the detector and reference resistors has slightly less resistance than the value in the process data of the simulation tool.

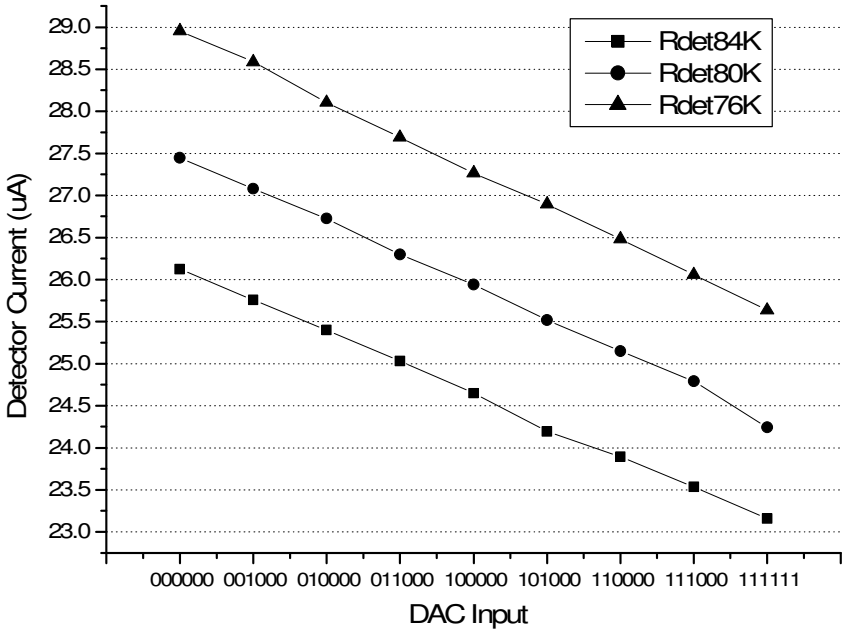


Figure 2.54: Measured detector currents with respect to DAC input for 76 KΩ, 80 KΩ, and 84 KΩ detector resistors. The detector current can be adjusted with a resolution of better than 50 nA.

Figure 2.55 shows the measured reference current with respect to compensation circuit control input for 76 KΩ, 80 KΩ, and 84 KΩ reference resistors. The reference current can be adjusted with a resolution of less than 50 nA by the compensation structure, which is equivalent to more than 50 times current compensation, considering the peak-to-peak variation in the current is around 2.51 μA for ±5% resistance nonuniformity.

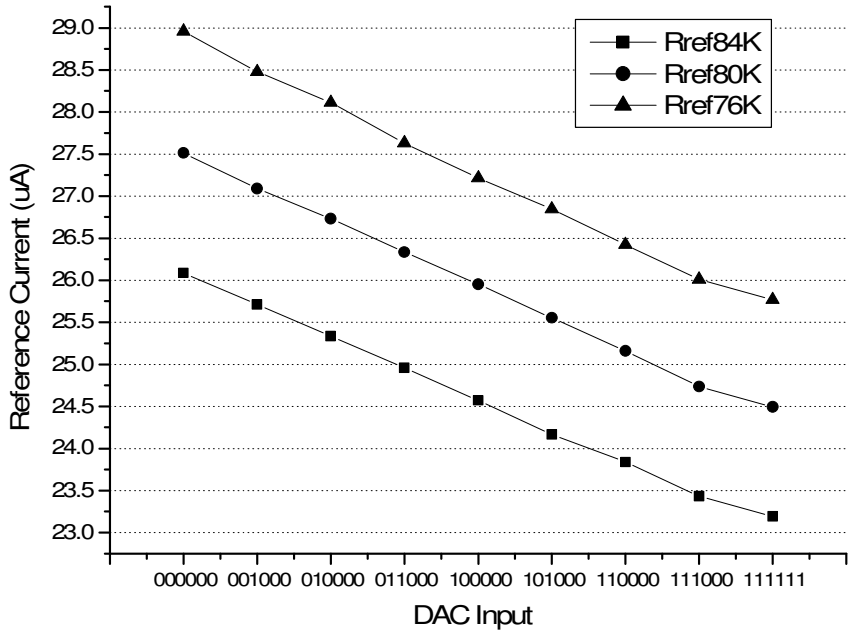


Figure 2.55: Measured detector currents with respect to DAC input for 76 KΩ, 80 KΩ, and 84 KΩ reference resistors. The reference current can be adjusted with a resolution of better than 50 nA, as the detector current.

2.4.2.2. Transient Simulation of the SCI and the S&H Circuit

Figure 2.56 shows the transient simulation result of the SCI and the S&H circuit outputs along with digital control signals. During the *reset* signal is high, the integrator output is tied to 2.5 V. At the positive edge of the *integrate* signal, the SCI starts to integrate the input current coming from the detector and reference biasing

circuit until the negative edge of the *integrate* signal. After the integration process, the S&H circuit samples the integrator output at the negative edge of the *sample* signal. The S&H circuit output is also tied to 2.5 V when the *sample* signal is high. After the sampling process, integrator resets the output and starts integration of the next input. When the DAC input decreased one bit, to illustrate from 101001 to 101000, the detector currents increases around 46 nA and the integrator output decreases around 0.85 V. Therefore, the measured gain of the integrator circuit is 1.85 for 190 µs integration time, which is theoretically equal to 1.9×10^7 by the Equation 2.23.

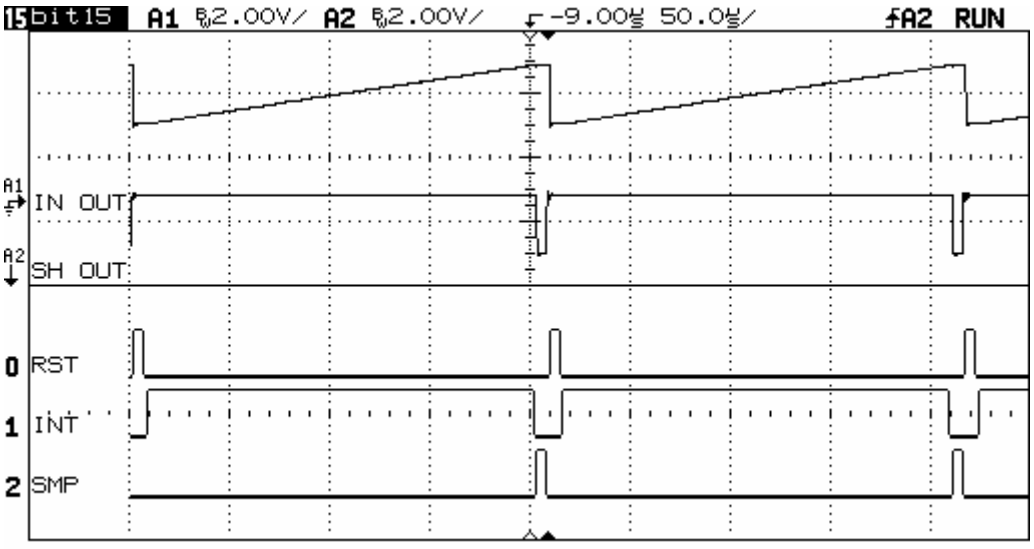


Figure 2.56: Scope view showing the transient simulation result of the SCI and S&H circuit outputs along with digital control signals. The measured gain of the integrator circuit is 1.85×10^7 for 190 µs integration time.

Figure 2.57 shows the transient simulation result of the SCI and S&H circuit outputs along with digital control signals, where the reference current is greater than the detector current, and the integration capacitance saturates at 5 V. The corresponding S&H circuit output is also 5 V.

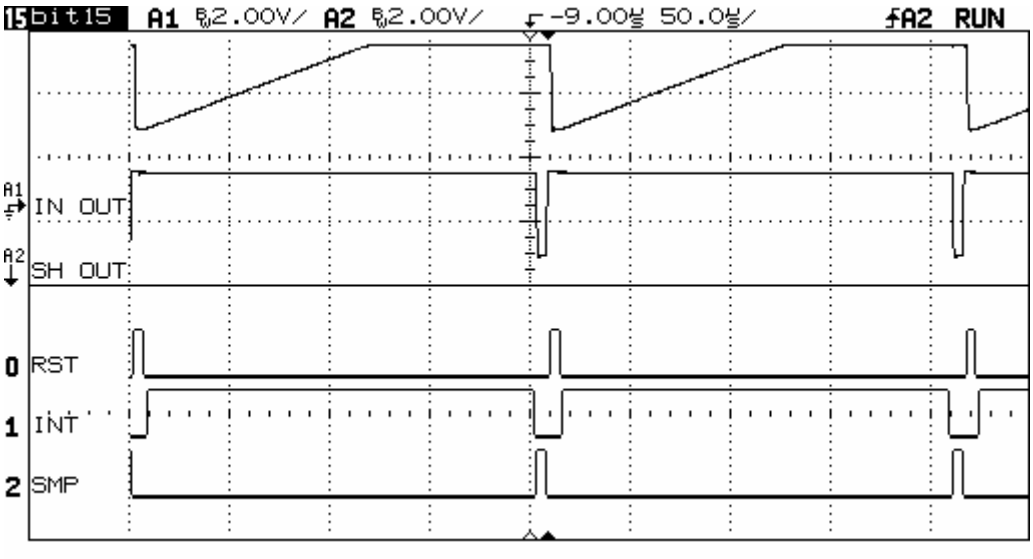


Figure 2.57: Scope view showing the transient simulation result of the SCI and the S&H circuit outputs along with digital control signals where the reference current is greater than the detector current, and the integration capacitance saturates at 5 V.

2.4.2.3. Noise Test of the Biasing Circuit and Compensation DACs

Noise of the biasing circuit and compensation DACs is measured by a dynamic signal analyzer. An amplifier card is prepared for noise measurement. Figure 2.58 gives the schematic of the test configuration. The output of the biasing circuit is followed by a three stage low noise amplifier. The first stage is a transimpedance amplifier with a gain of R_1, the second stage eliminates the DC part of the output of the first stage, and the final stage is a noninverting amplifier with a gain of $1+R_3/R_4$. R1 is selected as 104 KΩ which is high enough for amplifying current noise. The 3 dB point of the AC coupler is chosen smaller than 0.1 Hz for allowing the low frequency noise pass to the input of the second stage. The gain of the final stage is set to 51 by selecting R_4 and R_3 as 20 Ω and 1 KΩ, respectively. Small resistors are used to minimize the voltage noise of this stage.

Figure 2.59 show the picture of the setup used during noise measurements of the circuit. The test is performed in a metal Faraday cage with batteries powered by batteries for eliminating external noise sources. A dynamic signal analyzer is used to observe the noise power spectral density. The connections are taken by utilizing BNC connectors in order to shield the electrical signals from the environment.

Figure 2.60 shows the measured gain of the second stage of the amplifier. Gain is 51.1 V/V for low frequencies and the higher 3 dB corner frequency is at 42.4 KHz which is much greater than the electrical bandwidth of the measured circuit.

In order to measure the exact noise of the biasing circuit, noise of the amplifier should be known. Figure 2.61 gives the measured noise power spectral density of the discrete amplifier when the input of the first stage is connected to reset voltage of the operational amplifier. The measured thermal noise floor is calculated as 2.26×10^{-12} V^2/Hz. The 1/f noise of the discrete amplifier is very low and can be ignored during noise measurement. This measured noise power spectral density is to be subtracted from the measurement result obtained with the biasing circuit. Then by dividing this noise by the square of the gain of the amplifier, the noise power spectral density of the output current of the biasing circuit can be calculated. Figure 2.62 shows the noise power spectral density of the output current of the biasing circuit and the fitted curve.

The measured noise power spectral density of the output current is fitted into a curve which includes thermal and 1/f noise components as:

$$i^2_n(f) = i^2_{th} + \frac{K_{1/f}}{f} \tag{2.28}$$

where, i^2_{th} is the thermal power spectral density and $K_{1/f}$ is the 1/f noise coefficient, and f is the frequency.

From the fitted curve, the thermal noise floor of the biasing circuit with compensation DACs, i_{th}^2 is found as 4.09×10^{-25} A^2/Hz and K_f is found as 1.40×10^{-22}. Hence, the calculated 1/f corner frequency is 342 Hz. Total rms current noise is calculated as 47.2 pA over 2.6 KHz bandwidth and 58.4 pA over 5.2 KHz bandwidth. These values are much higher than simulation results which are 34 pA and 46 pA for 2.6 KHz and 5.2 KHz, respectively. This huge difference is because of the fact that the high 1/f noise of resistors are not calculated in the simulation program, Cadence.

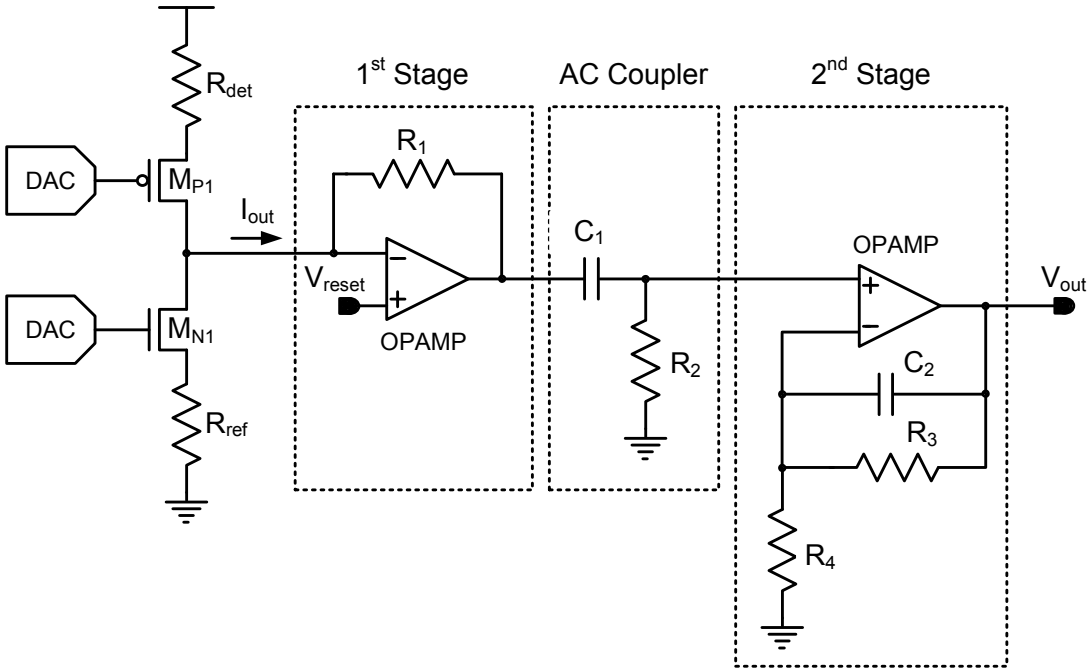


Figure 2.58: Schematic of the test configuration used in noise measurement of the biasing circuit with compensation DACs.

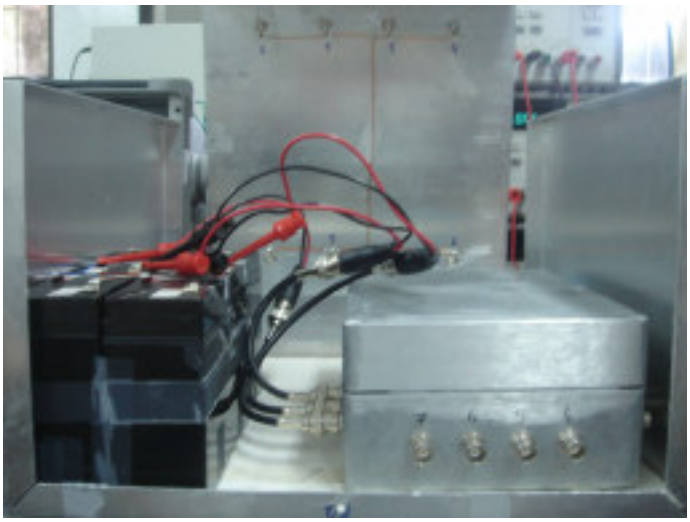


Figure 2.59: Picture of the setup used during noise measurements of the circuit.

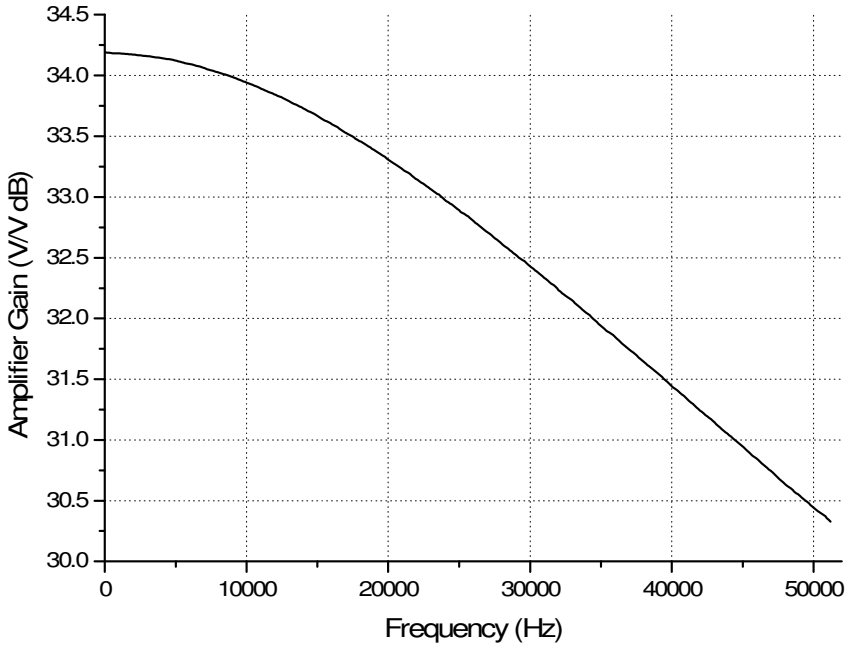


Figure 2.60: Measured gain of the second stage of the amplifier. Gain is 51.1 V/V for low frequencies and the higher 3 dB corner frequency is at 42.4 KHz.

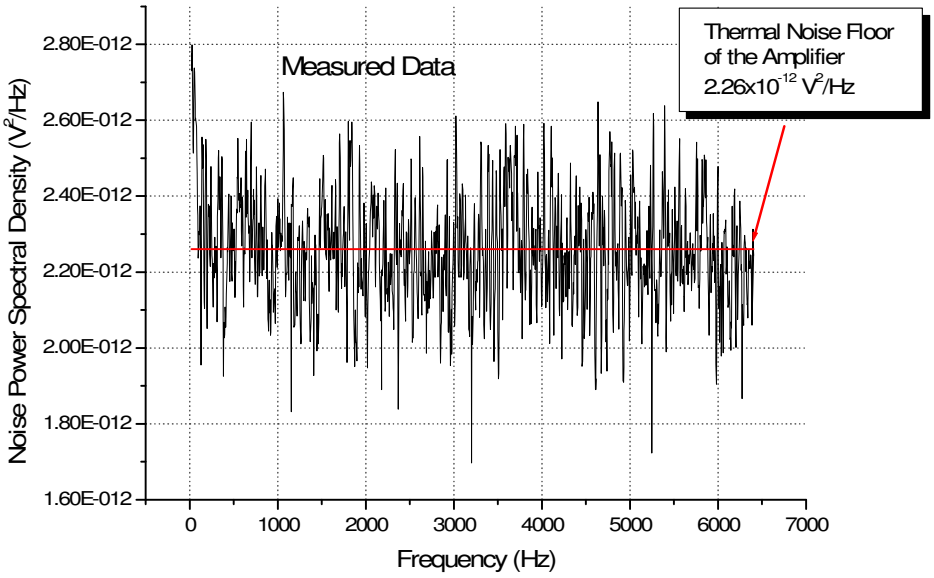


Figure 2.61: Measured noise power spectral density of the discrete amplifier when the input of the first stage is connected to reset voltage of the operational amplifier.

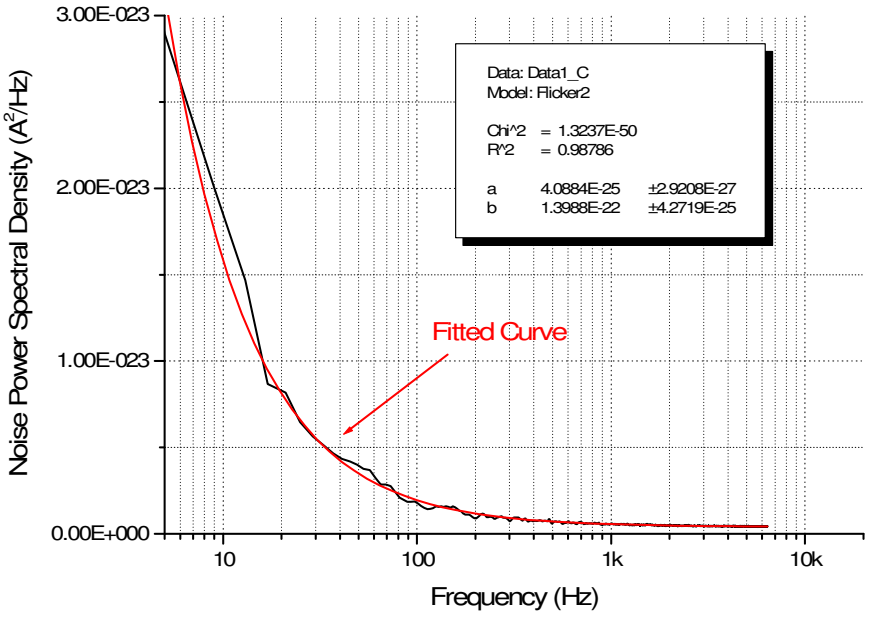


Figure 2.62: Measured noise power spectral density of the output current of the biasing circuit and the fitted curve.

2.4.2.4. Noise Test of the Overall Circuit

A high resolution ADC is connected to the output of the whole circuit in order to observe fluctuations at the digital output due to total noise of the overall circuit. In this case, a discrete amplifier for noise amplification is not necessary since ADC follows the output of the S&H circuit, and this output is already amplified by the SCI. 16-bit AD7655 ADC is used for conversion and output of the ADC is observed by a scope. Figure 2.63 gives the scope view showing the integrator output and 8 least significant bits of the ADC output. Fluctuations are observed on the least significant 6 bits of the output which corresponds to 4.9 mV peak-to-peak noise voltage at the output, considering the step size of the ADC is around 72.5 μV [66]. This result is consistent with the measured detector noise. The rms noise current of the biasing circuit measured as 47.2 pA in an electrical bandwidth of 2.6 KHz, and the gain of the integrator is 1.85×10^7 for the integration period corresponding to 2.6 KHz bandwidth. Thus, the rms voltage noise at the output which is the multiplication of the input current and gain becomes 0.873 mV. Assuming noise power spectral density of the output voltage has a Gaussian distribution, then there is a 98% probability of the voltage values are within $\pm 3\sigma$ of the mean voltage value. Here, σ corresponds to the rms voltage noise, thus the expected output fluctuation is 5.24 mV for 0.873 mV rms noise voltage.

The overall rms noise voltage of the circuit is 0.82 mV for the above noise measurement. 25 nA maximum infrared induced current on 25 μA detector bias current changes the output voltage 0.463 V for 190 μs integration time. Thus, the SNR of the readout circuit becomes almost 530.

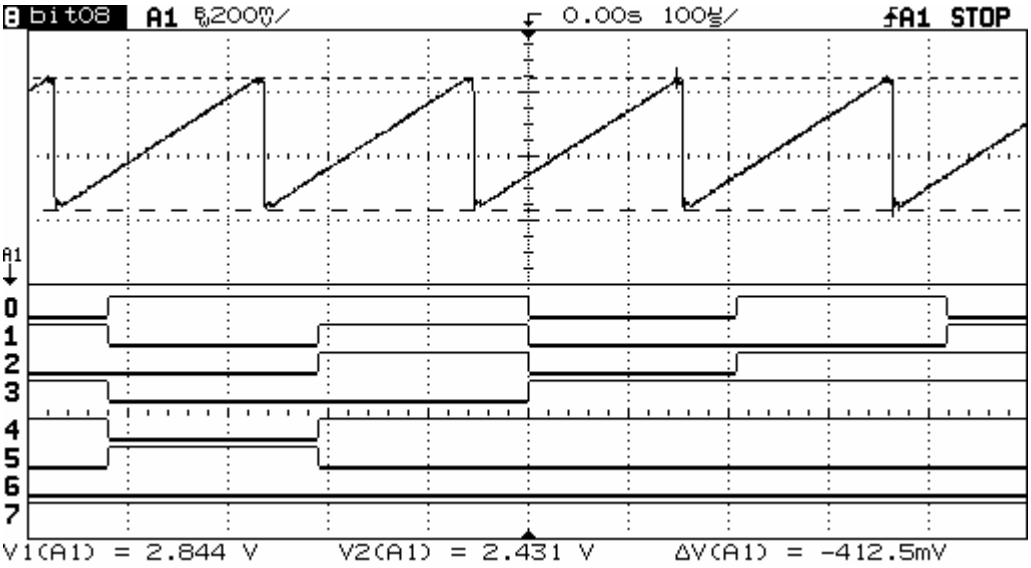


Figure 2.63: Scope view showing the integrator output and 8 least significant bits of the ADC output. Fluctuations at the digital output correspond to 5.24 mV peak-to-peak voltage noise.

2.5. Summary and Conclusions

This chapter presents design details, implementation, and simulation and test results of a high performance readout circuit for resistive uncooled microbolometer detector arrays which is fabricated by a standard 0.6 µm 5 V CMOS process. The fabricated chip occupies an area of 2079 µm x 974 µm (2 mm^2) where the area of the readout circuit measures around 2700 µm x 200 µm (0.54 mm^2).

In order to verify the operation of the circuit, various reference and detector resistors are implemented with the high resistance polysilicon layer of the CMOS process. Nominal resistance value is selected as 80 KΩ, while resistance nonuniformity of ±5% is achieved by implementing 16 reference and detector resistors in the range of 76 KΩ to 84 KΩ. Bias currents of the detector and reference resistors are set by 6-bit DACs, where these currents can be adjusted with a resolution of better than 50 nA. Thus the maximum compensated offset current becomes 100 nA which corresponds

to a current compensation ratio of 51, almost 5.7 bit. The measured rms current noise is 47.2 pA in an electrical bandwidth of 2.6 KHz which causes 0.82 mV rms voltage noise at the output of the readout circuit which is measured by connecting a 16-bit ADC. Considering this amount of output noise and circuit responsivity, the expected SNR of the readout circuit is 530. Table 2.5 summarizes performance parameters of the fabricated chip.

Although the circuit has a comparatively high area due to DACs and needs for a temperature stabilizer during its operation, the fabricated readout circuit is suitable for high performance resistive microbolometer detector arrays considering its high SNR and nonuniformity compensation capability.

Table 2.5: Characteristic of the fabricated chip.

Fabrication Technology	0.6 µm 5 V CMOS
Chip Size	2079 µm x 974 µm (2 mm^2)
Readout Circuit Area	2700 µm x 200 µm (0.54 mm^2)
Resistance	80 KΩ
Resistance Nonuniformity	±5%
Max. Compensated Current	100 nA
Max. Uncompensated Current	5.1 µA
Compensation Ratio	51 (1.96 %)
Compensation Resolution	5.7 bit
Detector current noise	47.2 pA rms (2.6 KHz BW)
Output voltage noise	0.873 mV rms (2.6 KHz BW)
Expected SNR	530

CHAPTER III

A DYNAMIC RESISTANCE NONUNIFORMITY COMPENSATION CIRCUIT

This chapter presents a new readout circuit for resistive uncooled microbolometer detector arrays which uses a novel nonuniformity compensation algorithm. Contrary to readout circuits using conventional nonuniformity compensation structures, this approach eliminates the need for digital-to-analog converters (DACs), which usually occupy a large area, dissipate high power, and require complicated external circuitry with high frequency data transfer to the microbolometer chip. The proposed circuit uses a feedback structure that dynamically changes the bias currents of the reference and detector pixels and does not need complicated external circuitry. A special feature of the circuit is that it provides continuous compensation for the detector and reference resistances due to temperature changes over time.

The conventional nonuniformity compensation circuits, one of which has been explained in detail in Chapter II, need to be adjusted before the signal integration period for each pixel in the microbolometer detector array. These circuits also need to be calibrated after a short period of time due to infrared focal plane array drift [60]. However, the dynamic resistance nonuniformity circuit does not need to be adjusted before the signal integration period. The circuit dynamically adjusts the bias currents of both detector and reference resistors before the signal integration to prevent saturation of the readout circuit due to resistance nonuniformity and infrared

focal plane array drift. After the signal integration corresponding compensation information is to be readout.

This chapter is organized as follows: Section 3.1 presents the operating principle of the circuit. Section 3.2 gives information about the design of the circuit. Section 3.3 gives Cadence simulation results. Section 3.4 explains the overall circuit and shows the overall layout. Section 3.5 gives the test results of the fabricated chip. Finally, Section 3.6 concludes the chapter by summarizing the features of the proposed new readout circuit.

3.1. Operating Principle of the Circuit

In order to explain the advantages of the proposed method, first the conventional nonuniformity compensation technique in resistive microbolometers will be briefly summarized in Section 3.1.1. Then the operating principle of the dynamic nonuniformity compensation circuit for resistive microbolometers will be presented in Section 3.1.2.

3.1.1. Conventional Nonuniformity Compensation in Resistive Microbolometers

Figure 3.1 shows a conventional readout integrated circuit (ROIC) for resistive microbolometers, including a capacitive transimpedance amplifier (CTIA), a sample-and-hold circuit, and two compensation DACs [44]. Resistance nonuniformity of resistive microbolometers should be compensated before the signal integration in order to prevent saturation of the integration capacitor. In conventional circuits, saturation of the integration capacitor is avoided by using DACs, which are connected to the injection transistors of the CTIA and programmed to allow a predefined current through the injection transistors. Ideally, both the detector and reference currents should be equal to each other, and the currents should remain

constant for any value of the detector and reference resistors in the nonuniformity range. Nonetheless, the finite resolution of DACs generates an undesired offset current, limiting the dynamic range of ROIC with the offset current. The offset current of a compensated system depends on the DAC resolution, and the maximum offset current due to nonuniformity decreases with increasing DAC resolution. However, increasing resolution makes the DAC occupy a large area and dissipate high power.

A compensation system including the use of DACs adjusts the bias voltages of the detector and reference resistors according to the bias information stored in the external digital memory. However, changes in system parameters like resistance change over time aggravate the performance of the DAC compensation. In addition, this nonuniformity compensation method requires not only high area, high power DACs, but also complicated external circuitry. These problems are overcome with the design of the dynamic nonuniformity compensation circuit, as explained in the next section.

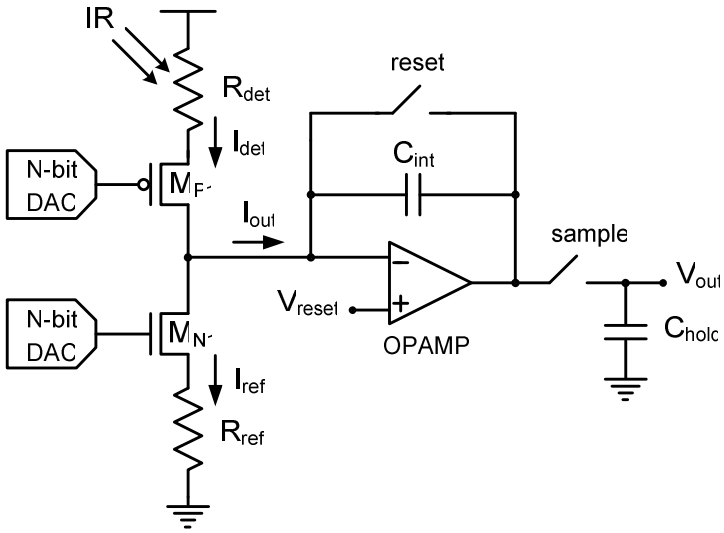


Figure 3.1: Simplified schematic of a conventional ROIC for resistive micro-bolometers, which includes a CTIA, a sample-and-hold circuit, and two compensation DACs.

3.1.2. The Dynamic Resistance Nonuniformity Compensation Circuit

Different from conventional resistive readout circuits, the dynamic nonuniformity compensation circuit adjusts the bias currents of both detector and reference resistors dynamically to prevent saturation of the readout circuit due to the nonuniformity offset current.

In Figure 3.1, the gate voltages of the injection transistors (M_{P1} and M_{N1}) are supplied by DACs; however, in the new dynamic nonuniformity compensation method, these voltages are supplied by a feedback circuit, where the currents through the reference and detector resistors are adjusted consecutively before the signal integration starts.

Figure 3.2 and Figure 3.3 show simplified schematics of the feedback circuit used in the dynamic nonuniformity compensation method, where two phases are shown. Figure 3.2 shows the phase where the bias current of the reference pixel is set to its predefined value. During this time, the PMOS injection transistor, M_{P1}, is turned off by applying supply voltage to its gate. At the beginning of this phase, C_n is discharged, and the bias current of the reference pixel is zero. As C_n is charged, the reference current will increase. When it reaches to its desired value, the comparator output becomes high, preventing further charging of C_n.

Figure 3.3 shows the second phase, where the bias current of the detector pixel is adjusted by the feedback circuitry. At the beginning of this phase, C_p is charged to supply voltage, and the detector current is zero. As C_p is discharged, the detector current will increase. When it becomes equal to the bias current of the reference resistor, the comparator output becomes low, preventing further discharging of C_p. Each of these phases is completed in less than 5 μs. Capacitors connected to the gate of injection transistors can store their charge during the integration period, which is much smaller than the time constant at the gate of injection transistors. After this compensation process, the integration period starts.

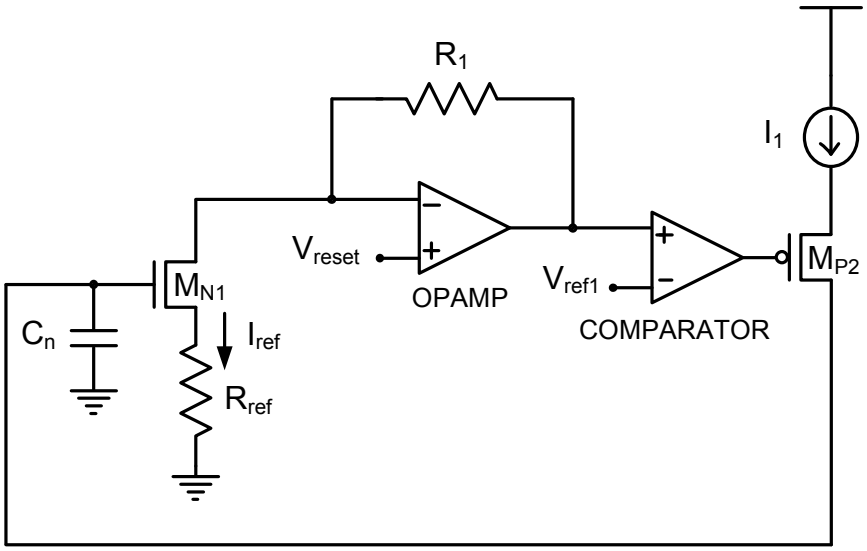


Figure 3.2: The first phase of the feedback circuit used in the dynamic non-uniformity compensation method, where the bias current of the reference pixel is set to its predefined value.

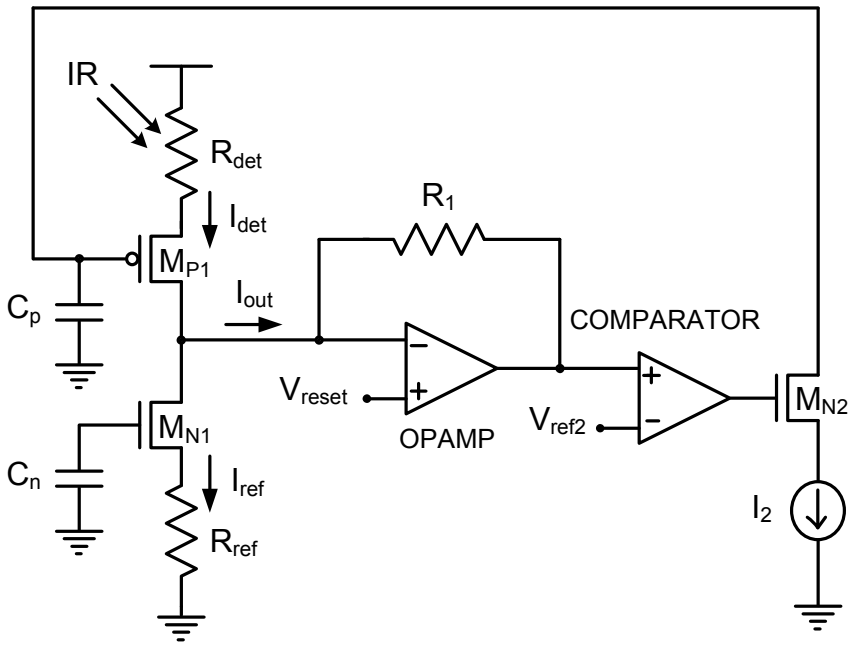


Figure 3.3: The second phase of the feedback circuit used in the dynamic non-uniformity compensation method, where the bias current of the detector pixel is adjusted by the feedback circuitry.

Figure 3.4 shows the simplified schematic of the circuit after the resistance compensation process. After adjusting the bias currents of reference and detector resistors, the signal integration starts. When the integration is completed, the CTIA output and the two gate voltages of the injection transistors are sampled and held. Since the current through the reference and detector resistors are related to the gate voltages of the injection transistors, infrared information can be extracted from these three output voltages by comparing them to initial calibration values. If bias currents deviate from the desired value, for example because of the comparator offset, the gate voltage of the corresponding bias current changes. Wrong evaluation is prevented by the output voltage whose value also changes due to the comparator offset. The absorbed infrared power changes the detector resistance, thus the gate voltage of M_{P1} adapts itself according to the resistance change.

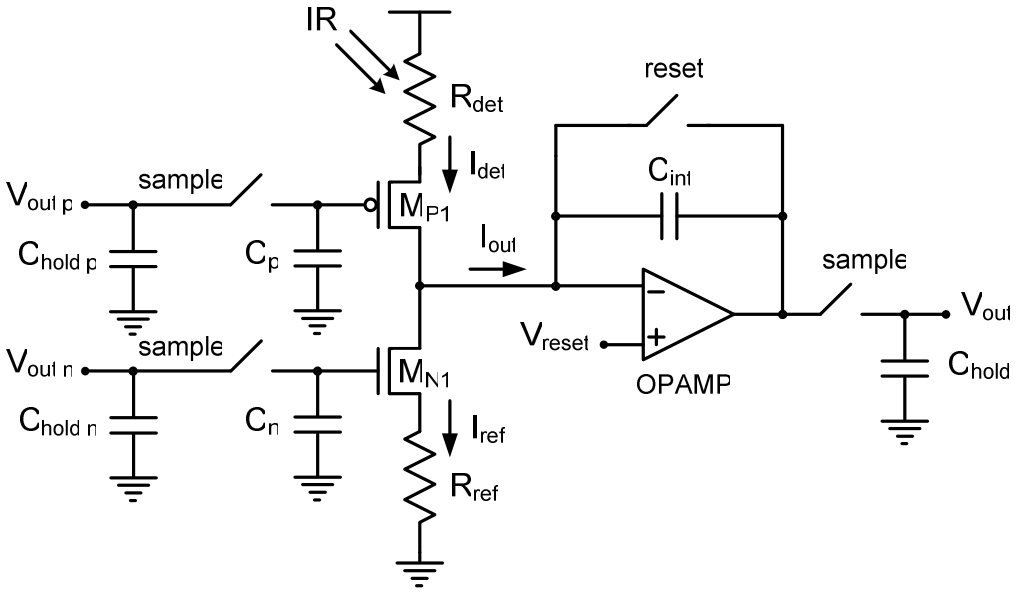


Figure 3.4: Simplified schematic of the dynamic nonuniformity compensation circuit after the resistance compensation process, while the integration occurs.

3.2. Design of the Circuit

Different from the CTIA type readout circuit, which has been explained in Chapter II, the dynamic nonuniformity compensation circuit includes a comparator, two gate capacitors, and two controllable current sources to charge or discharge gate capacitors. A low offset and high speed comparator is used from the analog library of the XFab xc06 CMOS process.

Response time and input offset voltage of the selected comparator are 20 ns and 10 mV, respectively. As explained in the previous section, the comparator controls current sources that supply 8 µA constant current in order to charge or to discharge 10 pF gate capacitors of the CTIA injection transistors. Since the time constant of the charging/discharging path is much larger than the charging/discharging time, charging/discharging of the capacitor is linear. Charging/discharging time can be calculated as fallows:

$$\Delta t = \frac{\Delta V \times C}{I_{source}} \tag{3.1}$$

where, C is the gate capacitance and equal to 10 pF, I_{source} is the magnitude of the supplied current by the current source and equals to 8 µA, and ΔV is the voltage change at gate capacitors and equals to 3.6 V – 3.9 V and 3.1 V – 3.4 V for the NMOS and PMOS injection transistors, respectively. Therefore, charging of the NMOS injection transistor takes around 4.5 µs, and discharging of the PMOS transistor takes around 4 µs.

The comparator controls current sources, and hence actual charging/discharging times. An error voltage occurs at the gate of injection transistors due to the comparator response time. This error voltage is:

$$E_V = \frac{t_R \times I_{source}}{C} \tag{3.2}$$

where t_R is the comparator response time and around 20 ns, I_{source} is the magnitude of the supplied current by the current source and equals to 8 μA, and C is the gate capacitance and equal to 10 pF. Hence, a maximum error voltage of 16 mV occurs at the gate of the injection transistors. This voltage induces 0.2 μA error current on 80 KΩ detector microbolometer resistor. This undesired error current is cancelled by the reference resistor which also has approximately the same amount of error current due to the comparator offset.

Bias currents of the detector and reference resistors can still deviate from the desired value because of the mismatch of the comparator response for adjusting the detector and reference currents and the electrical noise in the feedback circuit. When the bias current deviate from the desired value, the gate voltage of the corresponding bias current changes. Wrong evaluation is prevented by the integrator output voltage whose value also changes due to this current change, considering the integrator integrates the difference current between the detector and reference resistors.

After the current compensation process, the circuit behaves like a CTIA which is shown in Figure 3.4. The current compensation process adjusts the detector and reference currents so that the integration capacitor does not saturate. Each voltage measured at the gate of injection transistors corresponds to a known current for each of microbolometer resistors, and the integrator output is related to the difference between the detector and reference currents. Infrared information can be extracted from these three output voltages by comparing them to initial calibration values.

Table 3.1 gives a series of examples showing how infrared data can be extracted from outputs of the circuit. The detector and reference current values must be known for all the bias range. This is possible by measuring the bias current of each microbolometer resistor for two different bias voltages in the calibration process. Two measurements are sufficient to know bias current values for all the bias range, because the bias current – bias voltage relation is linear as explained in Chapter II. Thus, by measuring the gate voltages of the injection transistors the corresponding detector and reference current values, I_{DET} and I_{REF}, can be calculated. The switched

capacitor integrator integrates the difference current of the detector and reference microbolometers, I_{DET}-I_{REF}, thus the actual I_{DET}-I_{REF} can be extracted from the measured integrator output, where integration time 100 μs and integration capacitor is 10 pF. The infrared induced current equals the difference of the calculated I_{DET}-I_{REF} and the actual I_{DET}-I_{REF}.

Table 3.1: A series of examples showing how infrared data can be extracted from outputs of the circuit.

Example Number	**1**	**2**	**3**	**4**
Detector Resistance (KΩ)	80	82	77	84
Reference Resistance (KΩ)	80	81	82	76
Measured PMOS Gate Voltage (V)	1.86	1.81	1.94	1.76
Measured NMOS Gate Voltage (V)	3.77	3.80	3.83	3.67
Corresponding Det. Current (μA)	25.250	25.244	25.195	25.239
Corresponding Ref. Current (μA)	25.125	25.185	25.244	25.132
Corresponding I_{DET}-I_{REF} (μA)	0.125	0.059	-0.049	0.107
Measured Integrator Voltage (V)	1.10	1.80	2.95	1.40
Actual I_{DET}-I_{REF} (μA)	0.140	0.070	-0.045	0.110
Infrared Induced Current (μA)	0.015	0.011	0.004	0.003

Noise performance of the circuit is determined by three outputs. Noise of the integrator output is the same as the CTIA type readout circuit excluding the effect of DACs. In the CTIA type readout circuit, noise of DACs is also amplified and observed at the integrator output. However, in the dynamic resistance nonuniformity compensation circuit, measured gate voltages include some noise voltage added to the original gate voltages. Thus, the equivalent noise power spectral density of the detector current can be written as:

$$i^2_{n,eq} = i^2_{n,\text{int}} + i^2_{n,NMOS} + i^2_{n,PMOS} \tag{3.3}$$

where, $i_{n,int}$ is the noise power spectral density of the detector current of the CTIA, which is given in Equation 2.7, and $i_{n,NMOS}$ and $i_{n,PMOS}$ are the detector current referred measurement noise power spectral density. The upper limit of the rms noise currents of $i_{n,NMOS}$ (rms) and $i_{n,PMOS}$ (rms) can be expressed as:

$$i_{n,NMOS}(rms) = \frac{\sqrt{kT/C_{NMOS}}}{R_{ref}} \tag{3.4}$$

$$i_{n,PMOS}(rms) = \frac{\sqrt{kT/C_{PMOS}}}{R_{\text{det}}} \tag{3.5}$$

where, R_{ref} and R_{det} are the reference and detector resistors, C_{NMOS} and C_{PMOS} are the gate capacitors of the NMOS and PMOS injection transistors, T is the absolute temperature, and k is the Boltzman constant. Gate voltages are sampled and held by a switched capacitor circuit and the rms voltage noise of a switched capacitor circuit is equal to or less than the square root of kT/C [63]. To minimize this measurement noise, large capacitors should be connected to the gates of the injection transistors.

3.3. Simulation Results

Figure 3.5 gives a transient simulation result showing the operation of the circuit. At the beginning of each detector selection, both detector and reference currents are zero. The reference and detector currents are adjusted to their predefined values, 25 µA, by the feedback circuit, respectively. This compensation process takes less than 12 µs. After adjusting the bias currents of the reference and detector resistors, the signal integration starts through the switched capacitor integrator. When the integration is completed, the integrator output and the two gate voltages of the injection transistors are sampled and held.

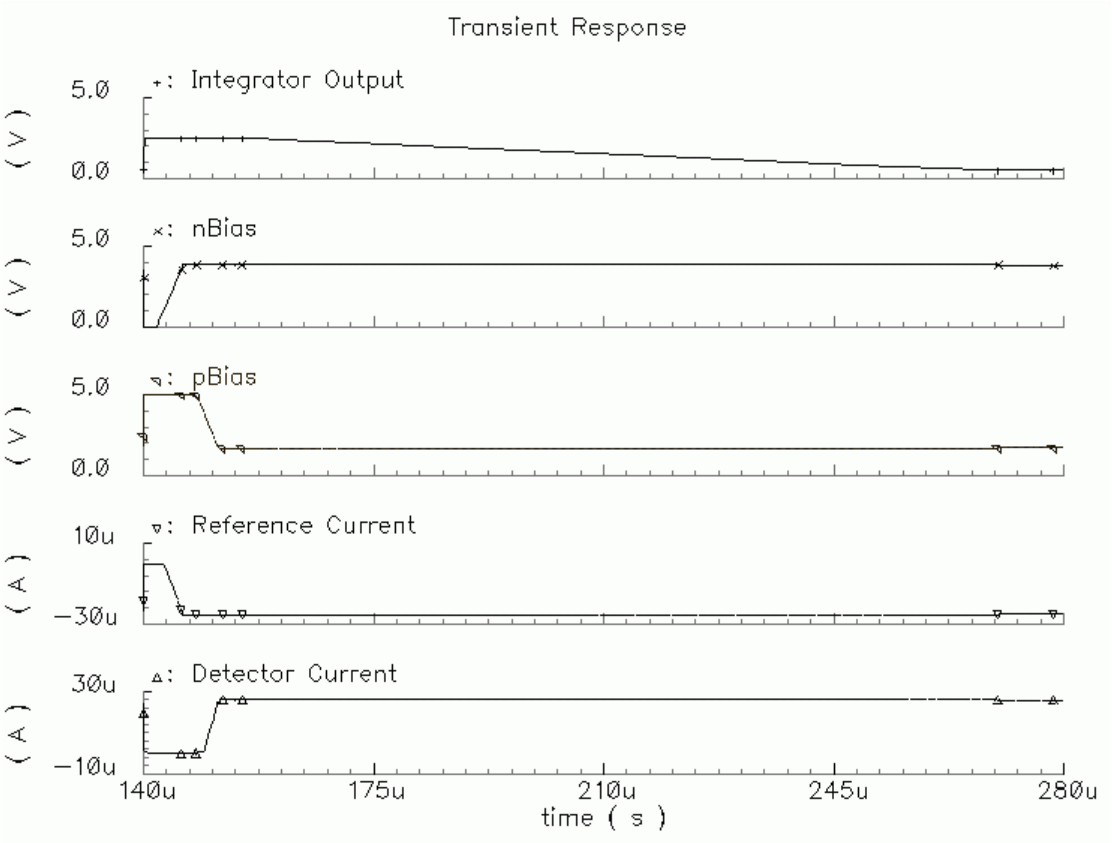


Figure 3.5: Transient simulation result showing the current adjustment process. The compensation process takes less than 12 µs.

Figure 3.6 shows the simulated input referred voltage noise of the whole circuit excluding the gate measurement noise. The rms voltage noise is 4.34 µV in 4 KHz electrical bandwidth, which corresponds to 125 µs signal integration. By dividing the rms input referred noise voltage to the nominal detector resistance of 80 KΩ, the rms detector current is calculated as 54.25 pA, which includes noise of the biasing circuit, the CTIA, and the sample-and-hold circuit. On the other hand, each gate voltage measurement brings at most 254 pA rms noise current by Equations 3.4 and 3.5. Thus, the total rms detector referred noise current is 363 pA.

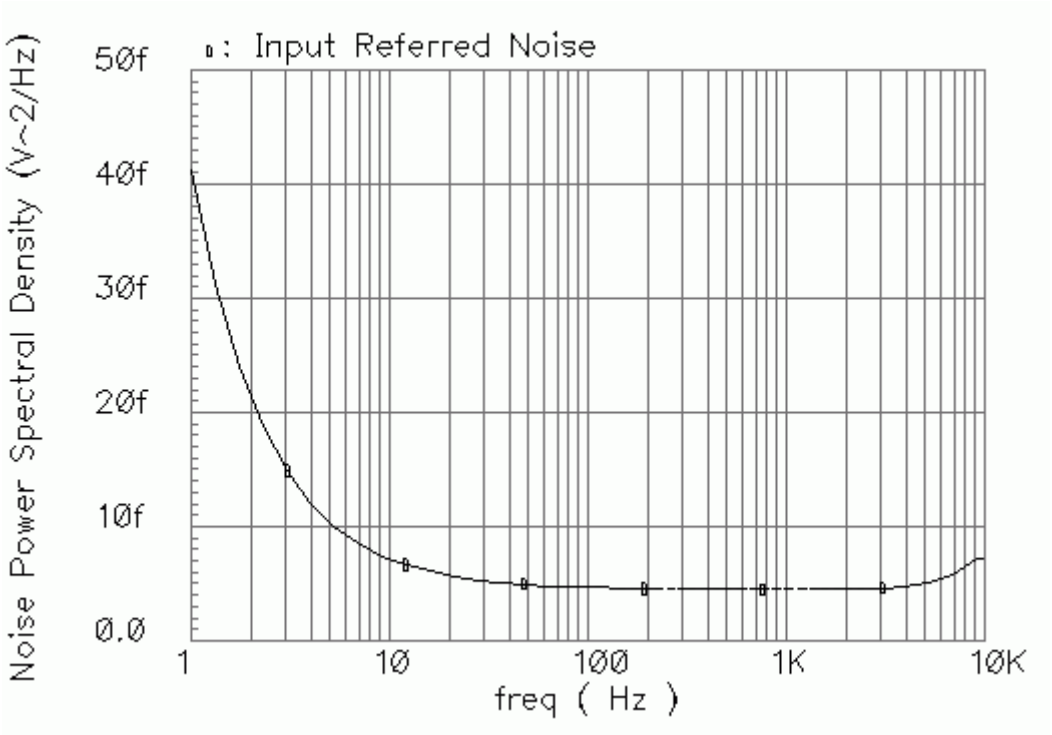


Figure 3.6: Simulated input referred voltage noise of the whole circuit excluding the gate measurement noise. The rms voltage noise is 4.34 μV in 4 KHz electrical bandwidth, which is equivalent to 54.25 pA rms detector current.

3.4. Overall Design

The dynamic nonuniformity compensation circuit is implemented by a standard 0.6 μm 5 V CMOS process. In order to test the circuit for resistance nonuniformity, two resistor arrays with 8 and 16 resistors between 76 KΩ and 84 KΩ are implemented for the reference and detector resistors, respectively. Figure 3.7 shows the complete layout of the chip which measures 4450 μm x 342 μm (1.5 mm^2) in a 3-metal/2-poly CMOS process. Figure 3.8 shows the picture of the fabricated chip.

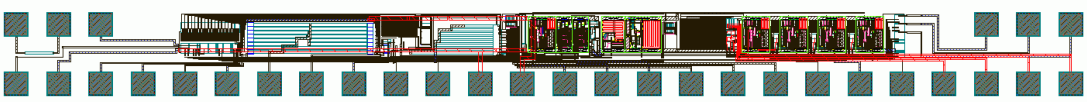


Figure 3.7: Layout of the whole chip which measures 4450 µm x 342 µm (1.5 mm^2) in a 3-metal/2-poly CMOS process.

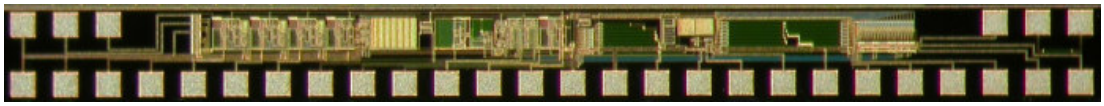


Figure 3.8: Picture of the fabricated chip.

3.5. Test Results

This section gives test results of the fabricated chip. A two-layer printed circuit board (PCB) was prepared in order to test the circuit. Figure 3.9 shows the picture of the two-layer PCB.

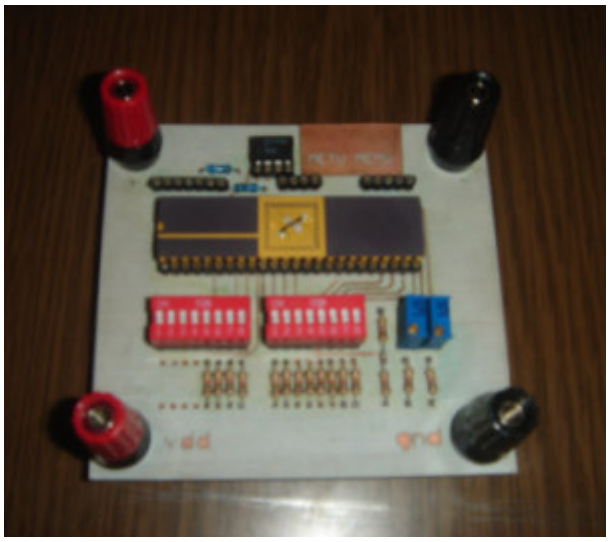


Figure 3.9: Picture of the two-layer printed circuit board for test measurements.

3.5.1. Test of Timing Signals

Timing signals of the circuit are generated by a XILINX FPGA circuit board. Figure **3.10** shows the picture of the FPGA card with the test PCB. Figure 3.11 shows the illustrated timing for the FPGA output signals. While *signal 1*, *signal 2*, and *signal 3* are control signals of the compensation structure, *reset*, *integ*, and *sample* are control signals of the switched capacitor integrator and the sample-and-hold circuit.

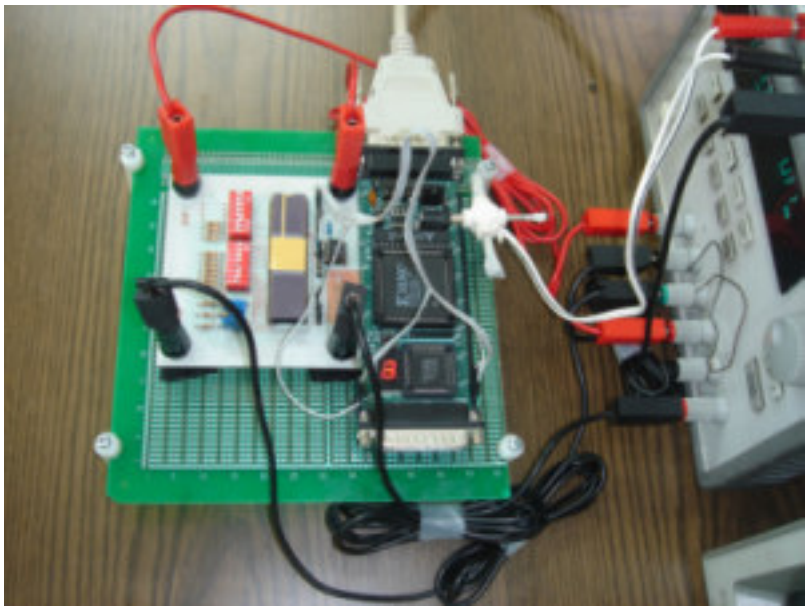


Figure 3.10: Picture of the FPGA card with the test PCB.

In order to guarantee the proper operation of the compensation structure, high phase of *signal 1* should be at least 1 µs long, *signal 2* and *signal 3* should be at least 6 µs longer than *signal 1* and *signal 2*, respectively. Therefore, sufficient time is given to reset, charge, and/or discharge capacitors related with compensation. The *reset* signal should be high during the compensation process, and the sample signal should be at least 4 µs long in order to guarantee proper operation of the sample-and-hold

circuit. Moreover, there should be a time period of 1-2 μs between *reset*, *integ*, and *sample* pulses in order to prevent overlapping of these signals. The FPGA generates digital signals with 0 V low voltage level and 3.3 V high voltage level, which are compatible with the used 5 V CMOS process.

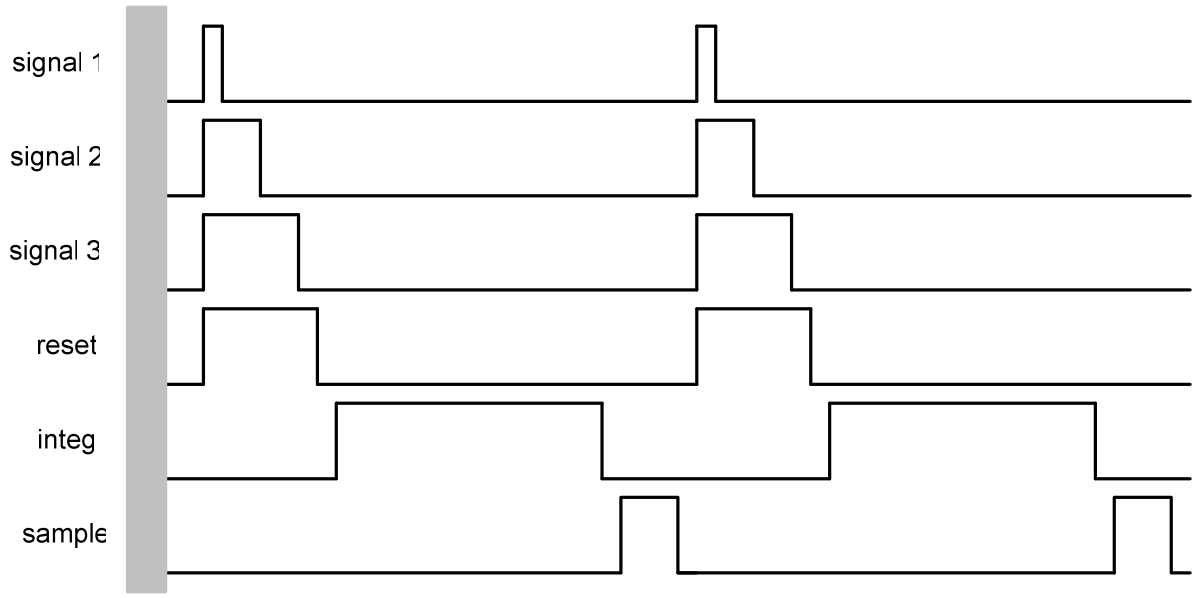


Figure 3.11: Illustrated timing for the FPGA output signals.

Figure 3.12 gives XILINX simulation results of the designed timing circuit. The timing circuit includes a 16-bit counter, a combinational circuit, and a sampling circuit, which eliminates glitches of the output. SGN10, SGN11, SGN12, SGN13, SGN14, and SGN3 represent *signal 1*, *signal 2*, *signal 3, reset, integ*, and *sample* signals, respectively. Figure 3.13 gives the scope view that shows digital control signals of the dynamic resistance nonuniformity compensation circuit. The integration time is 175 μs.

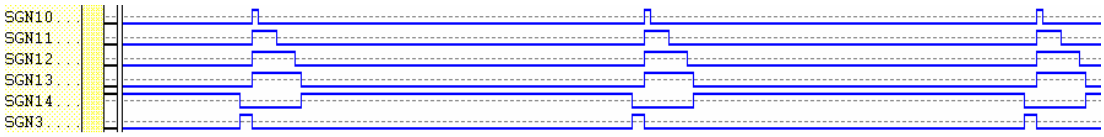


Figure 3.12: XILINX simulation results that show digital control signals: *signal 1*, *signal 2*, *signal 3, reset, integrate*, and *sample.*

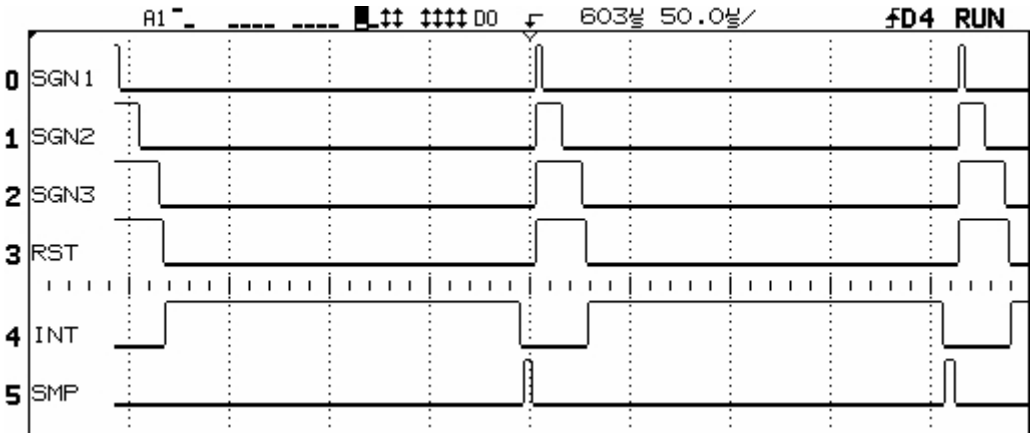
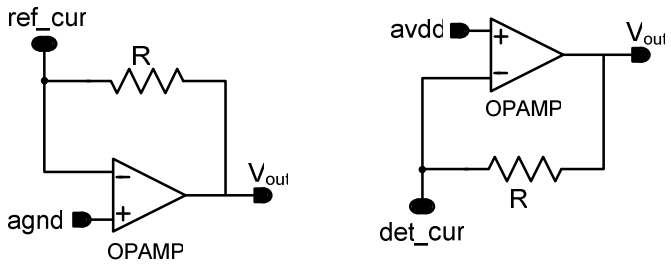


Figure 3.13: Scope view that shows digital control signals of the dynamic resistance nonuniformity compensation circuit, where the signal integration time is 175 µs.

3.5.2. Test of Analog Blocks

Detector and reference currents are measured for different detector and reference resistors in the ±5% nonuniformity range. Figure 3.14 shows schematic of transimpedance amplifiers implemented on the PCB to monitor detector and reference currents. Figure 3.15 gives the picture of the scope showing the reference and detector currents that are amplified by a factor of 10^5 by the transimpedance amplifiers shown in the Figure 3.14. The detector and reference currents are measured for all combinations of 76 KΩ, 78 KΩ, 80 KΩ, 82 KΩ, and 84 KΩ detector and reference resistors. Offset currents, i.e., the difference between the detector and reference currents, are calculated from the measured values. Figure 3.16 (a) shows

the simulated current values of an uncompensated system, and Figure 3.16 (b) shows the measured current values of the fabricated dynamic nonuniformity compensation circuit. The circuit reduces the maximum offset current due to resistance nonuniformity from 5.1 µA to 0.12 µA in only 12 µs, i.e., the maximum offset current reduced to 2.35% of its uncompensated value.



(a) (b)

Figure 3.14: Schematic of transimpedance amplifiers in order to monitor (a) the reference and (b) the detector currents. Both currents are amplified by a factor of R, which is 100 KΩ.

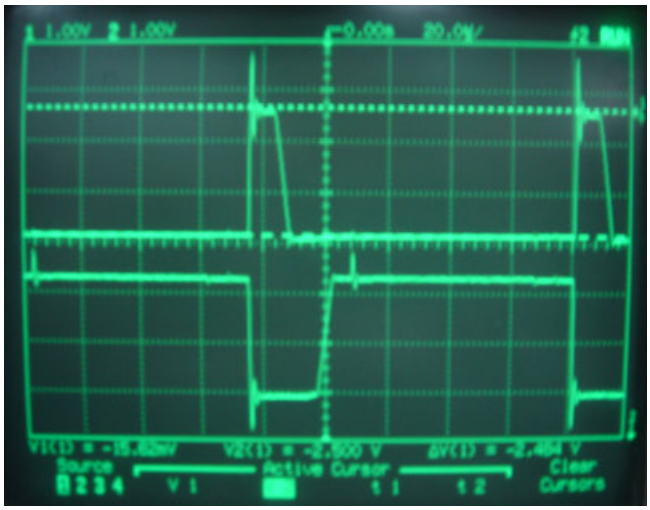
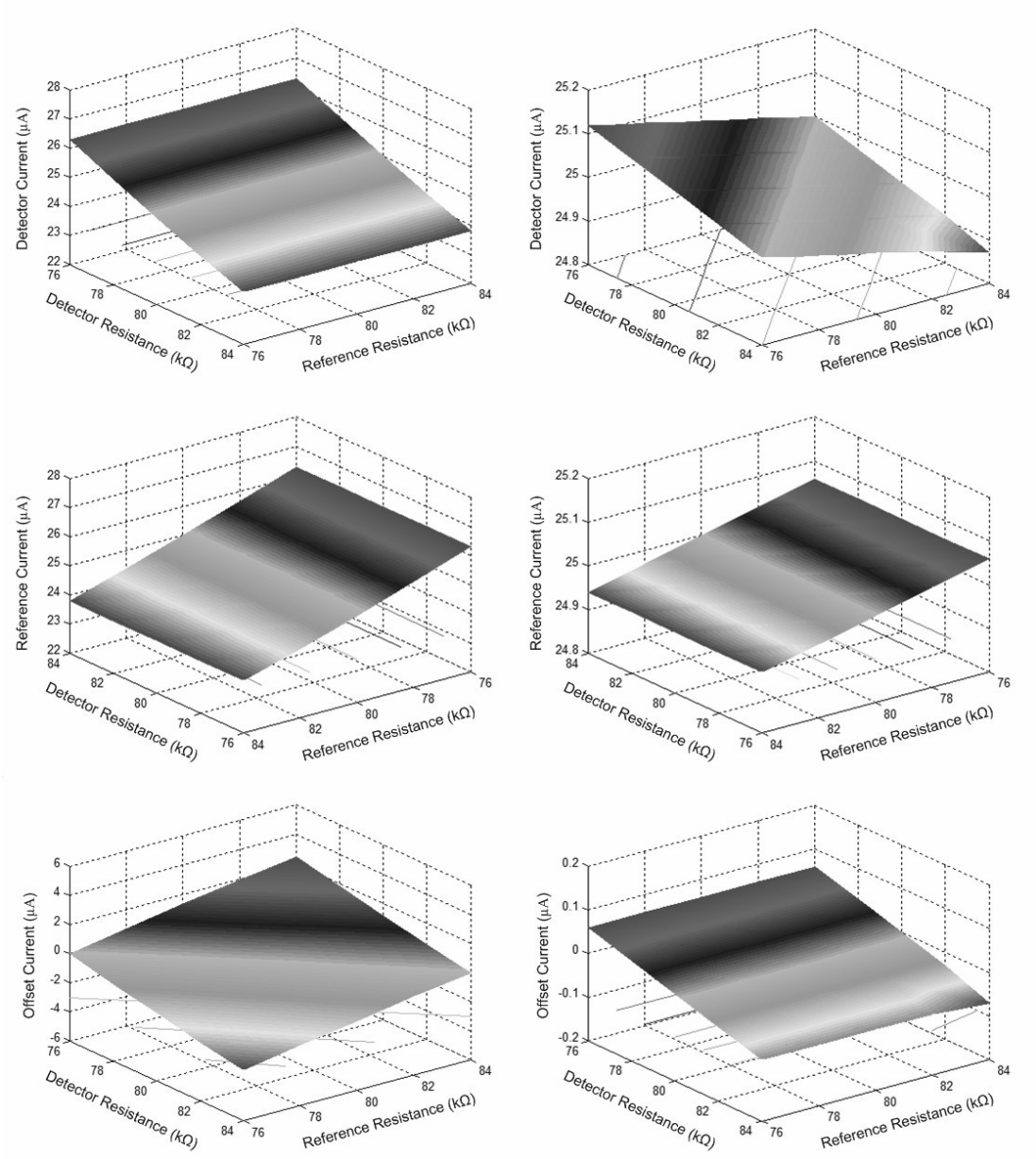


Figure 3.15: Picture of the scope showing the reference and detector currents that are amplified by a factor of 10^5.



(a) (b)

Figure 3.16: Simulation and test results for the detector, reference, and offset currents: (a) simulated values of an uncompensated system (b) measured values of the fabricated dynamic nonuniformity compensation circuit. The offset current due to resistance nonuniformity is reduced to about 2.35% of its uncompensated value.

Figure 3.17 and Figure 3.18 show measured gate voltages of the CTIA injection transistors where resistance changes directly affect the gate voltages. The decrease in the detector resistance due to the absorbed infrared power changes the gate voltage of the PMOS injection transistor in the same manner.

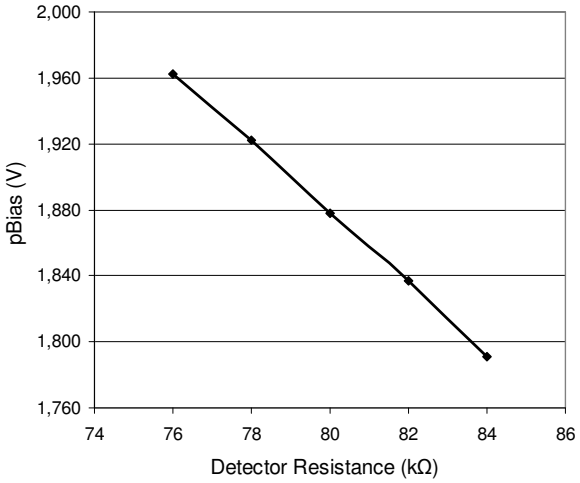


Figure 3.17: Measured gate voltages of the PMOS injection transistor of the CTIA when the reference resistor is 80 KΩ.

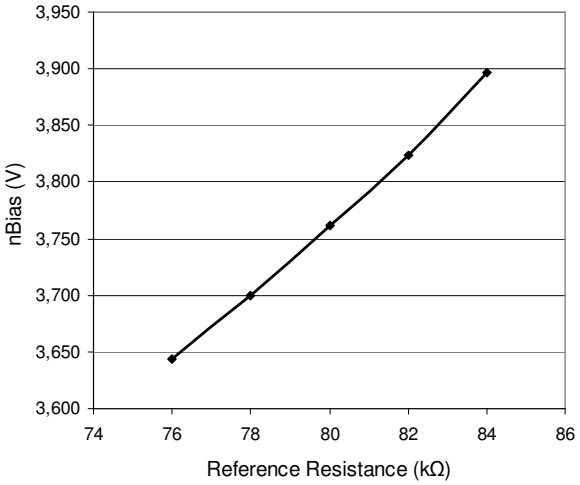


Figure 3.18: Measured gate voltages of the NMOS injection transistor of the CTIA when the detector resistor is 80 KΩ.

Except the gate noise of the injection transistors, noise of the circuit is the same as the noise of the CTIA type readout circuit, whose noise tests are given in Section 2.4.2.3. The gate noise of the injection transistors cannot be measured by classical methods using a dynamic signal analyzer. The only method to measure the noise is to connect three high resolution analog-to-digital converters ADCs to each output and to calculate noise using wrong digital outputs. However, this gate noise is less than 20.3 μV, the kT/C noise, and in order to measure this amount of noise, ADCs with at least 20-bit resolution and 5 μV output noise must be used. Section 2.4.2.4, an ADC with 16-bit resolution is used to measure the noise of the other design. However, even this 16-bit DAC has an output noise of 2-bit, which is equivalent to 50 μV rms noise. Therefore, the gate noise of the circuit cannot be measured, and it is assumed to be equal to the square root of kT/C, 20.3 μV. Hence, the overall rms current is around 360 pA and it is mainly due to the gate noise and almost independent of the electrical bandwidth. Assuming that the maximum infrared induced current on 25 μA detector bias current is 25 nA, the SNR of the readout circuit is almost 70.

3.6. Summary and Conclusions

This chapter presents the operating principle, design details, implementation, and simulation and test results of a novel circuit called the dynamic resistance nonuniformity circuit for uncooled microbolometer detector arrays. The circuit is fabricated by a standard 0.6 μm 5 V CMOS process. The fabricated chip occupies an area of 4450 μm x 342 μm (1.5 mm^2), where the area of the readout circuit measures around 630 μm x 160 μm (0.10 mm^2).

In order to verify the operation of the circuit, various reference and detector resistors are implemented with the high resistance polysilicon layer of the CMOS process. Nominal resistance value is selected as 80 KΩ, while resistance nonuniformity of ±5% is achieved by implementing a number of reference and detector resistors in the

range of 76 KΩ to 84 KΩ. The circuit reduces the maximum offset current due to resistance nonuniformity from 5.1 µA to 0.12 µA in only 12 µs, i.e., a current compensation ratio of 42.5, 5.4 bit. The calculated rms current noise is around 360 pA in an electrical bandwidth of less than 8 KHz. Considering this amount of detector noise and circuit responsivity, the expected SNR of the readout circuit is 70. Table 3.2 summarizes performance parameters of the fabricated chip.

Although the circuit has a comparatively low SNR, it is the first implemented dynamic compensation circuit in the literature [53]. The circuit occupies much smaller area than a conventional readout circuit with compensation capability. Moreover, the readout circuit does not saturate for different microbolometer resistance values in the nonuniformity range, which alleviates the need for a temperature stabilizer during its operation.

Table 3.2: Characteristic of the fabricated chip.

Fabrication Technology	0.6 µm 5 V CMOS
Chip Size	4450 µm x 342 µm (1.5 mm^2)
Readout Circuit Area	630 µm x 160 µm (0.10 mm^2)
Resistance	80 KΩ
Resistance Nonuniformity	±5%
Max. Compensated Current	120 nA
Max. Uncompensated Current	5.1 µA
Compensation Ratio	42.5 (2.35 %)
Compensation Resolution	5.4 bit
Detector current noise	360 pA rms (up to 8 KHz BW)
Expected SNR	70
Response Time	12 µs

CHAPTER IV

AN IMPROVED CTIA TYPE READOUT CIRCUIT FOR RESISTIVE MICROBOLOMETERS

This chapter presents an improved CTIA type readout circuit for resistive microbolometer detector arrays. The circuit modifies the conventional capacitive transimpedance amplifier (CTIA) with achieving almost the same performance, gaining a lot of area, and simplifying the operation. Moreover, small area property of the new circuit enables to put increased number of readout channels in a microbolometer chip, which decreases the electrical bandwidth and noise, and hence increases the microbolometer performance. Furthermore, the circuit also works with dynamic mode, solving some problems of the dynamic resistance nonuniformity compensation circuit, which has been presented in Chapter III. Nevertheless, this new dynamic circuit still has low SNR, and needs to be improved. An improved dynamic resistance nonuniformity compensation circuit is also proposed in this chapter.

This chapter is organized as follows: Section 4.1 presents a new biasing method for resistive microbolometers. Section 4.2 explains operating principles of the fabricated circuit with static and dynamic modes. Section 4.3 presents overall layout and floor plan of the designed chip. Section 4.4 gives the test results of the fabricated chip. Section 4.5 proposes an improved dynamic resistance nonuniformity compensation circuit. Finally, Section 4.6 concludes the chapter by summarizing the features of the readout electronics.

4.1. Double Biasing of Resistive Microbolometers

Figure 4.1 shows the double biasing circuit of the detector and reference resistors. While the current through the reference resistor (I_{ref}) is controlled by the voltage applied to the gate of the PMOS injection transistor (M_{P1}), the current through the detector resistor (I_{det}) is controlled by the bias voltages applied to the gates of the main (M_{N1}) and auxiliary (M_{N2}) injection transistors. The relation between the detector current and the bias voltage of the auxiliary and main injection transistors as follows:

$$I_{\det} \times R_{\det} = V_{bias} - V_{gs2} = N_{bias} - V_{gs1} \tag{4.1}$$

where, N_{bias} and V_{bias} are the gate voltages of M_{N1} and M_{N2}, V_{gs1} and V_{gs2} are the gate-to-source voltages of M_{N1} and M_{N2}, and I_{det} is the current passing through the detector resistor, R_{det}.

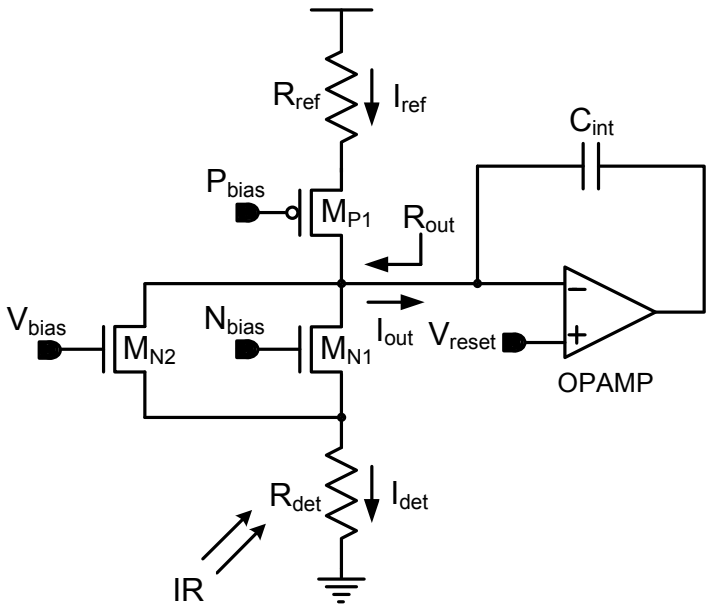


Figure 4.1: Schematic of the double biasing circuit of the detector resistor.

The advantage of this biasing circuit is that the auxiliary transistor increases the control level on the detector current. Figure 4.2 demonstrates the change in the bias voltage of the auxiliary injection transistor to obtain a constant detector current for the detector resistance values of 76 KΩ, 78 KΩ, 80 KΩ, 82 KΩ, and 84 KΩ. The bias voltage spans a 0.4 V range to control the detector current. In a biasing circuit without an auxiliary bias transistor, this control voltage range is smaller and equals to 0.25 V, which is shown in Figure 2.11.

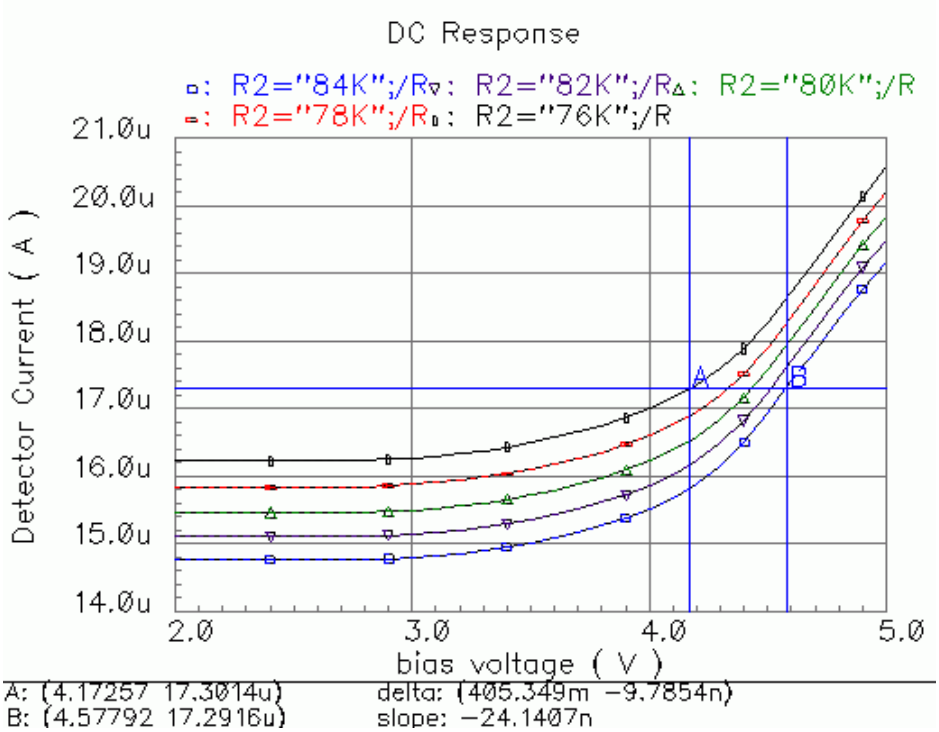


Figure 4.2: Simulated the detector current versus the auxiliary injection transistor bias voltage for different values of the detector resistor. The bias voltage should increase for larger resistors in order to provide constant current for the detector resistance values in the resistance nonuniformity range.

For a small amount of resistance nonuniformity the bias voltage range widens, which increases the controllability on the detector current. Figure 4.3 demonstrates the

change in the bias voltage of the auxiliary injection transistor to obtain a constant detector current for the detector resistance values of 79.2 KΩ, 79.6 KΩ, 80 KΩ, 80.4 KΩ and 80.8 KΩ. The bias voltage spans a 0.5 V range to control the detector current. Hence, 0.1 V bias voltage change corresponds to 320 Ω resistance change. However, for the previous case where the bias voltage span is 0.4 V, 0.1 V bias voltage change is equivalent to 2 KΩ resistance change. For a given resistance nonuniformity, for example ±5%, it is possible to decrease the effect of nonuniformity 4 times by connecting only 2-bit DACs using multiple analog buses to the gate of the main injection transistors, M_{N1} and M_{P1} as explained in detail in Chapter II. Also the effect of nonuniformity decreases 8 times by connecting only 3-bit DACs using multiple analog buses

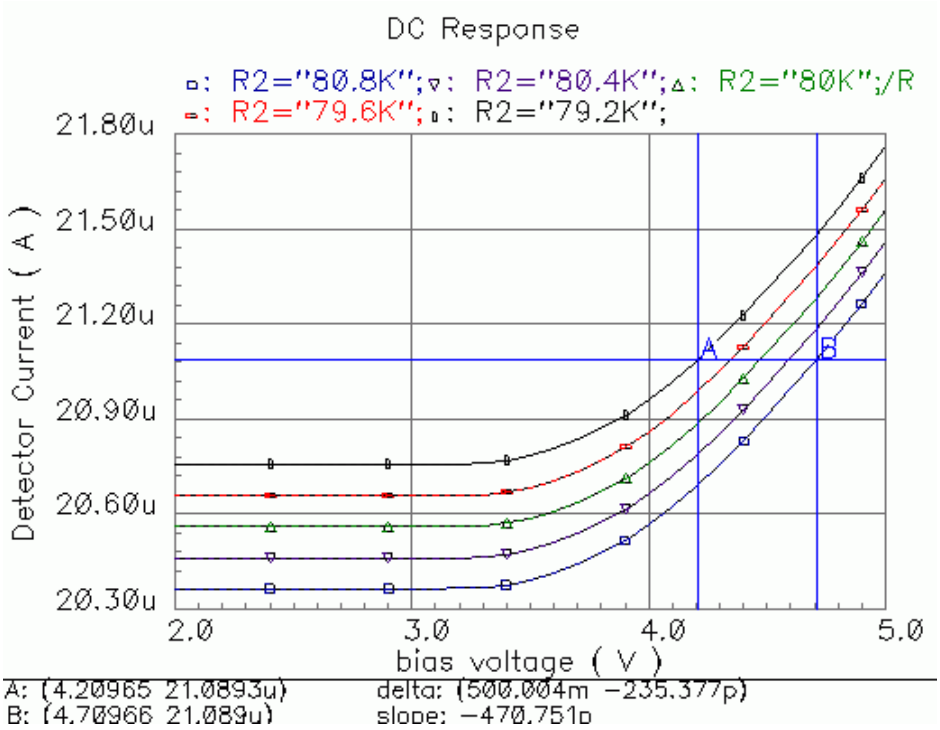


Figure 4.3: Simulated the detector current versus the auxiliary injection transistor bias voltage for 79.2 KΩ, 79.6 KΩ, 80 KΩ, 80.4 KΩ and 80.8 KΩ detector resistances. In this case, the controllability on the detector resistance nonuniformity increases, where 0.1 V bias voltage change is equivalent to 320 Ω resistance change

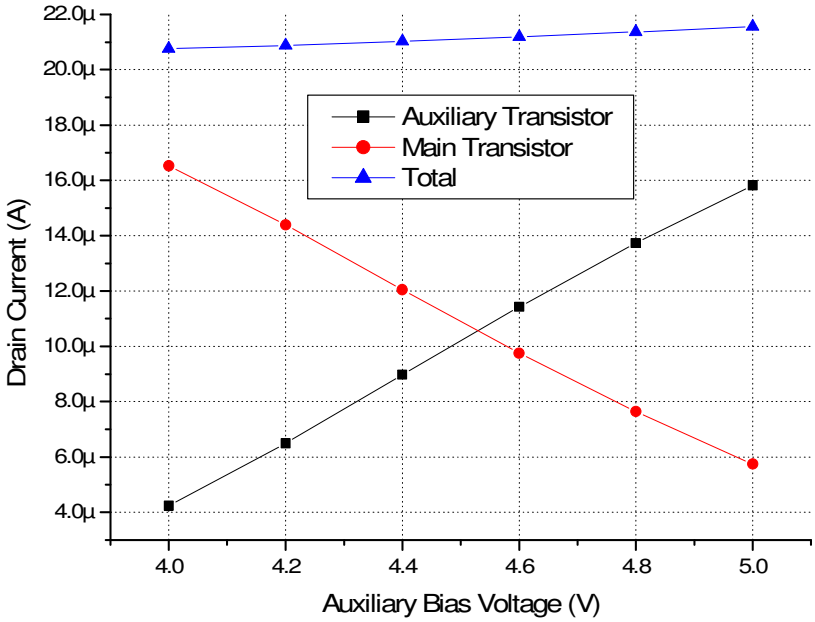


Figure 4.4: Simulated the auxiliary transistor, main transistor, and total currents of the biasing circuit with respect to the bias voltage of the auxiliary transistor.

Bias voltage of the auxiliary transistor affects the transconductance of the main and auxiliary transistors. Ignoring the body effect and the channel length modulation, the trans-conductance of an NMOS transistor in the saturation and triode regions are:

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_{DS}} \qquad \text{Saturation} \qquad (4.2)$$

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right) V_{DS} \qquad \text{Triode} \qquad (4.3)$$

where, μ_n is the electron mobility, C_{ox} is the unite area gate oxide capacitance of the transistor, W and L are the width and length of the transistor, I_{DS} and V_{DS} are the drain-to-source current and voltage of the transistor. Figure 4.5 shows trans-conductance of the auxiliary and main transistors with respect to the bias voltage of the auxiliary transistor. The main bias transistor is in the saturation region in the

whole operation range, and transconductance of the main transistor decreases with increasing auxiliary transistor bias voltage. When the bias voltage of the auxiliary transistor increases, transconductance of the auxiliary transistor increases up to 4.5 V, where the transistor enters in the triode region and transconductance becomes directly proportional to the drain-to-source voltage of the transistor as stated in Equation 4.3.

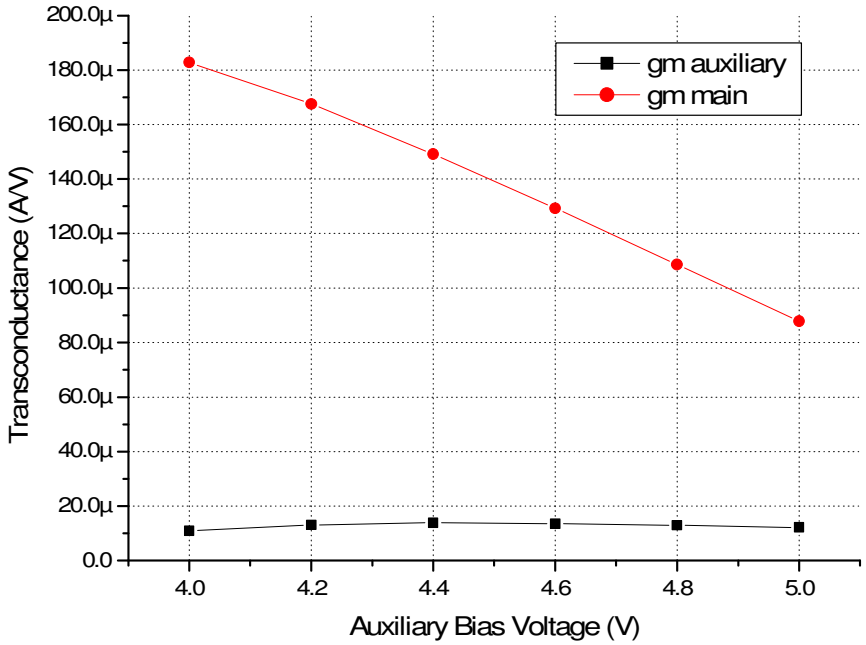


Figure 4.5: Simulated transconductance of the auxiliary and main transistors with respect to the bias voltage of the auxiliary transistor.

Small signal output resistance of the main and auxiliary transistors also depends on the bias voltage of the auxiliary transistor. Figure 4.6 shows small signal output resistance of the auxiliary and main transistors with respect to the bias voltage of the auxiliary transistor. Since the small signal output resistance of a transistor is reversely proportional to the transistor current, small signal output resistance of the main transistor increases and that of the auxiliary injection transistor decreases when the bias voltage of the auxiliary transistor increases.

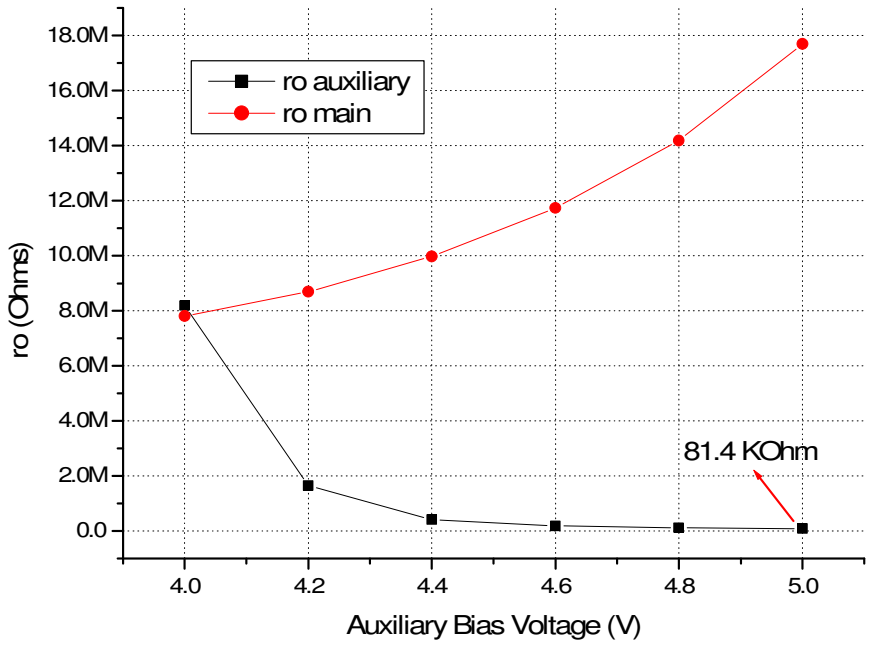


Figure 4.6: Simulated small signal output resistance of the auxiliary and main transistors with respect to the bias voltage of the auxiliary transistor.

The output resistance of the biasing circuit, which is shown in Figure 4.1, should be high for suppressing the input referred noise of the operational amplifier in order to achieve low noise signal integration. In fact, the injection transistors of the conventional biasing circuit are in the saturation region for the whole operation range, and provide high output resistance. Nonetheless, in the double biasing circuit, when the bias voltage of the auxiliary transistor is higher than 4.5 V, that transistor turns is the triode region and its output resistance decreases. In this case, the output resistance of the NMOS part of the biasing circuit can be expressed as:

$$R_{out} = R_{\det} + (r_{o1} // r_{o2})[1 + g_{m1} R_{\det}] \tag{4.4}$$

where, r_{o1} and r_{o2} are the small signal resistance of M_{N1} and M_{N2}, R_{det} is the detector resistance, and g_{m1} is the transconductance of M_{N1}. Figure 4.7 shows the simulated output resistance versus frequency of the all biasing circuit for the worst case where

the auxiliary transistor bias voltage is 4.94 V. Output resistance is almost 1.1 MΩ for the worst case and equal to 43.0 MΩ for the best case, where the bias voltage of the auxiliary transistor is 3.96 V.

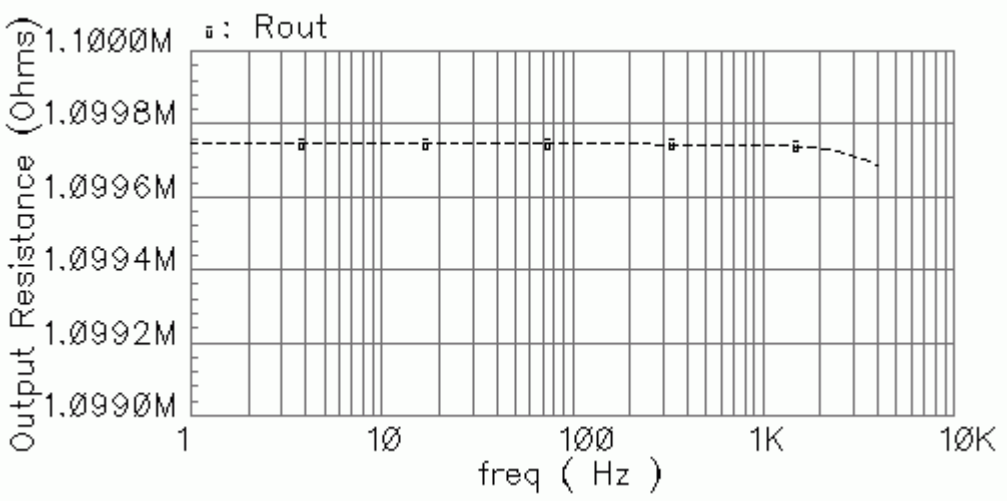


Figure 4.7: Simulated output resistance versus frequency of the all biasing circuit for the worst case where the auxiliary transistor bias voltage is 4.94 V.

An output resistance of 1.1 MΩ is high enough to suppress the input referred voltage noise of the operational amplifier, which is 2.74 μV in an electrical bandwidth of 4 KHz. Hence, the detector referred current noise is around 2.5 pA which is ignorable with respect to the thermal noise of the detector and reference resistors.

4.2. The Improved CTIA Type Readout Circuit for Resistive Micro-bolometers

Double biasing circuit is used in the readout circuit in order to increase the controllability on the detector current. There are two operation modes of the circuit:

static and dynamic modes. Section 4.2.1 and Section 4.2.2 present the static and dynamic modes, respectively.

4.2.1. The Static Mode of the Improved Circuit

Figure 4.8 shows the simplified schematic of the circuit. P_{bias} and N_{bias} voltages are supplied by 3-bit DACs and V_{bias} voltage is supplied by a 4-bit DAC where all DACs have multi channel analog outputs as explained in Section 2.2.3. A switched capacitor integrator is used for low noise current integration. After the signal integration, a sample-and-hold circuit samples the voltage at the output of the CTIA and holds it until the next sample of the next pixel. The switched capacitor integrator and the sample-and-hold circuit are explained in Chapter II.

The operating principle of the circuit is the same as the CTIA type readout circuit which is presented in Chapter II, except the biasing circuit. The biasing circuit of the previous circuit is composed of two main injection transistors, which are supplied by 6-bit DACs. However, the biasing circuit of this circuit is composed of two main transistors supplied by 3-bit DACs and an auxiliary transistor supplied by a 4-bit DAC.

Figure 4.9 shows the simulated transfer characteristic of N_{bias} voltage to integrator output for 190 µs integration time and 10 pF integration capacitance. Gain of the integrator is calculated as 1.9×10^7 V/A by the Equation 2.23. Thus 0.1 voltage change on the N_{bias} voltage corresponds to 0.81 µA detector current change. Figure **4.10** shows the simulated transfer characteristic of V_{bias} voltage to integrator output, where 0.1 V voltage change on the V_{bias} voltage is equivalent to 82 nA detector current change. The graph also shows the electrical bandwidth of the circuit, which is equal to 2.7 KHz.

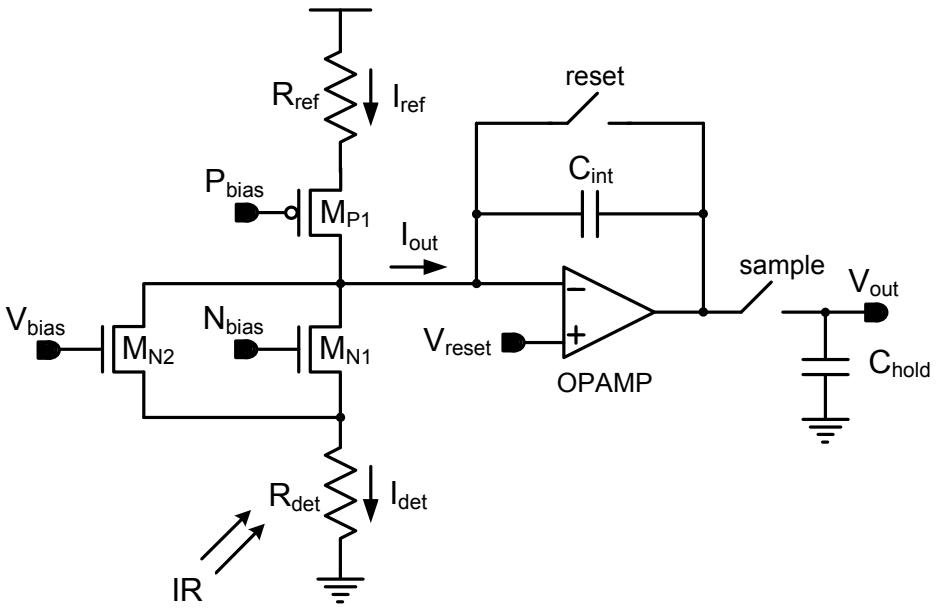


Figure 4.8: Simplified schematic of the static mode of the improved readout circuit for resistive microbolometers.

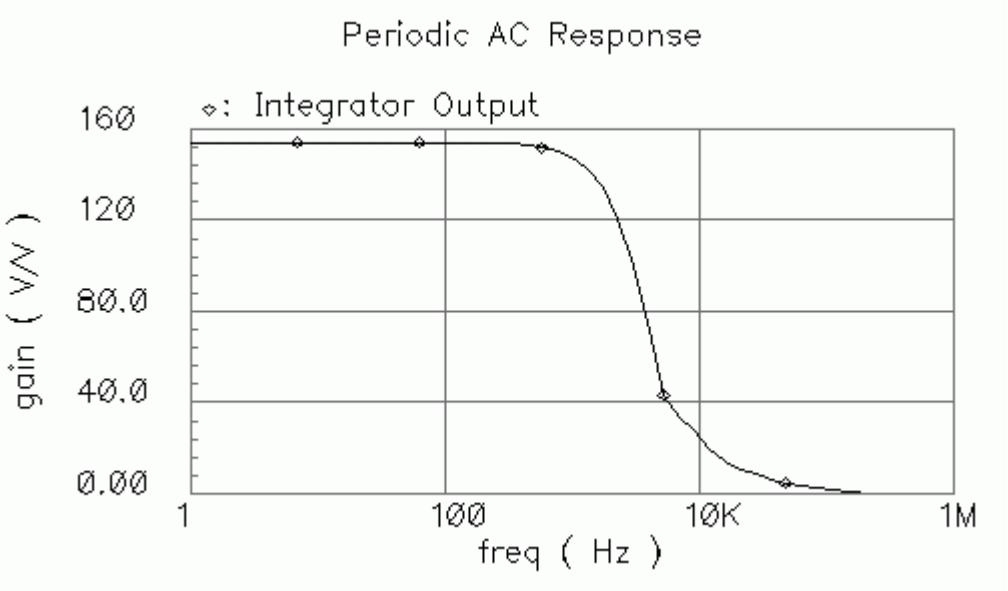


Figure 4.9: **S**imulated transfer characteristic of N_{bias} voltage to integrator output.

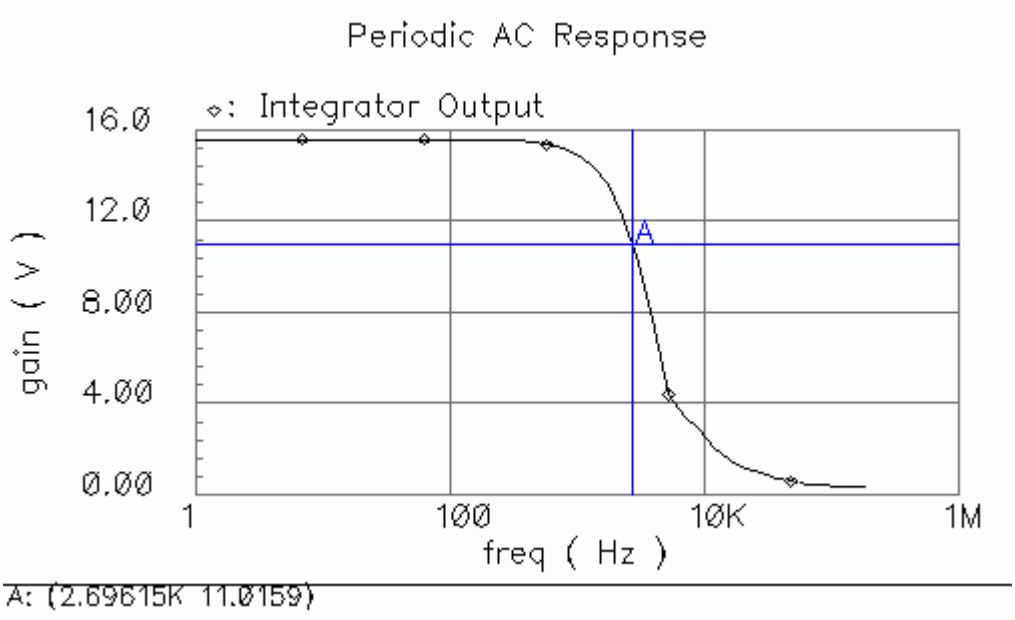


Figure 4.10: **S**imulated transfer characteristic of V_{bias} voltage to integrator output.

For ±5% resistance nonuniformity, 80 KΩ detector resistance and 21 µA nominal bias current, peak-to-peak nonuniformity current is 2.1 µA. 3-bit DAC connected to the main injection transistor, M_{N1}, reduces this offset current 0.26 µA. 4-bit DAC connected to the auxiliary injection transistor, M_{N2}, reduces the offset current from 0.26 µA to 16 nA. Thus the total nonuniformity current reduction of the circuit is 128 times, which is much higher than the previous circuit that uses two 6-bit DACs and occupies 7 times larger area.

Figure 4.11 shows simulated input referred voltage noise of the whole readout circuit, where the input node is the gate of the auxiliary injection transistor. The rms voltage noise is 47.6 µV in an electrical bandwidth of 2.7 KHz corresponding to 39.1 pA detector noise current. Assuming that the maximum infrared induced current is one thousandth of the detector bias current, 21 nA, the expected SNR of the circuit is 537.

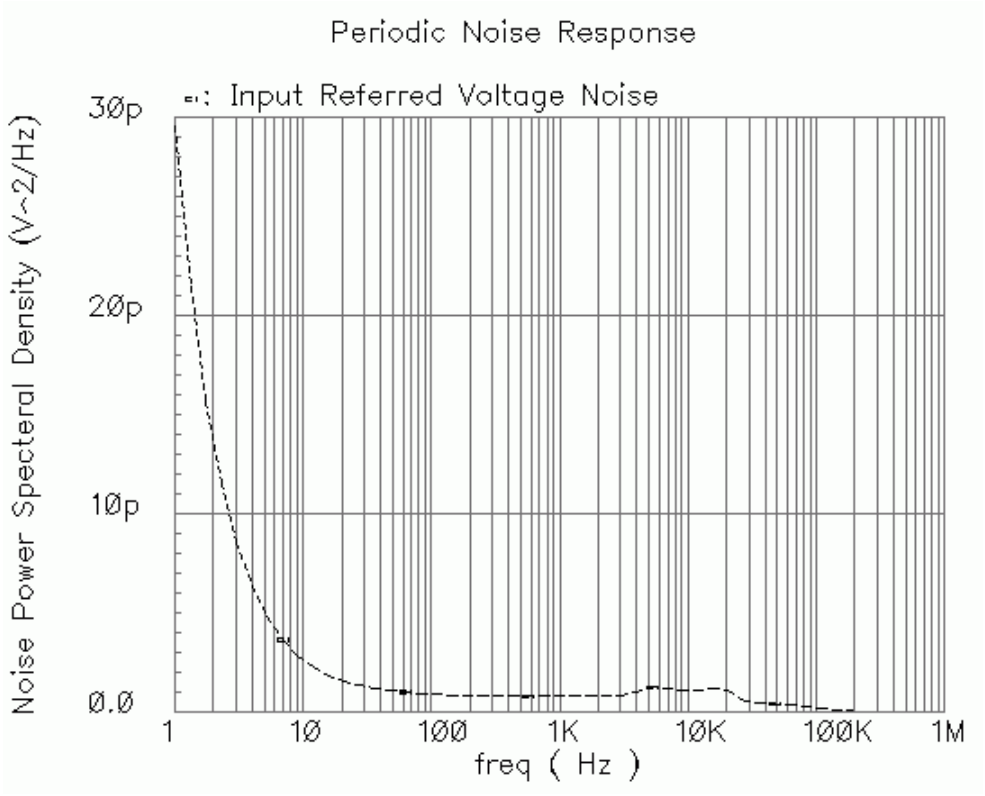


Figure 4.11: Simulated input referred voltage noise of the whole readout circuit, where the input node is the gate of the auxiliary injection transistor.

4.2.2. The Dynamic Mode of the Improved Circuit

Figure 4.12 shows the simplified schematic of the circuit. A feedback loop is formed between the integrator and the bias voltage of the auxiliary injection transistor, M_{N2}. The integrator output affects the bias voltage of the auxiliary injection transistor, and thus the detector current.

Initially, if the detector current is smaller than the reference current, I_{out} is positive, and the integrator output voltage starts to decrease, which increases the bias voltage of the auxiliary injection transistor. As the bias voltage increases, the detector current rises up to the magnitude of the reference current. When the detector and reference currents are equal, I_{out} becomes zero, preventing further current integration.

Thus, the integrator output and the bias voltage become constant. Initially, if the detector current is greater than the reference current, I_{out} is negative, and the integrator output voltage starts to increase, which decreases the bias voltage of the auxiliary injection transistor. As the bias voltage decreases, the detector current reduces up to the magnitude of the reference current. When the detector and reference currents are equal, I_{out} again becomes zero, preventing further current integration, and the integrator output and the bias voltage become constant.

For a constant detector current, as the detector resistance changes the corresponding bias voltage changes as shown in Figure 4.3. Infrared radiation, which also changes the detector resistance, can be extracted from the integrator output. After the feedback circuit reaches its steady state, sample-and-hold circuit samples the integrator output voltage and holds it until the next sample of the next pixel.

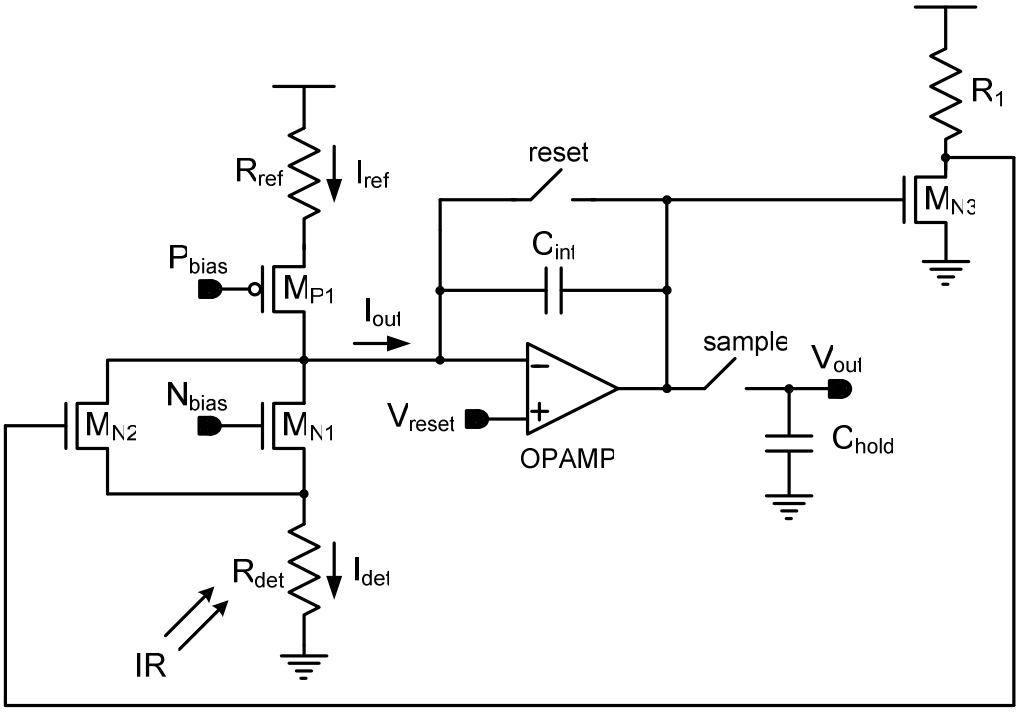


Figure 4.12: Simplified schematic of the dynamic mode of the improved readout circuit for resistive microbolometers.

Figure 4.13 gives the simulation result which shows the circuit operation. Reference resistor is 79.2 KΩ and detector resistor is swept from 79.2 KΩ to 80.8KΩ with 0.4 KΩ increments. For different detector resistance values, bias voltage of the auxiliary injection transistor comes to voltage levels so that the detector current finally reach the same current level, which is equal to the reference current. Different detector resistance values result in different bias voltage levels. Therefore, the infrared radiation, which changes the detector resistance, can be extracted from the bias voltage or the integrator output.

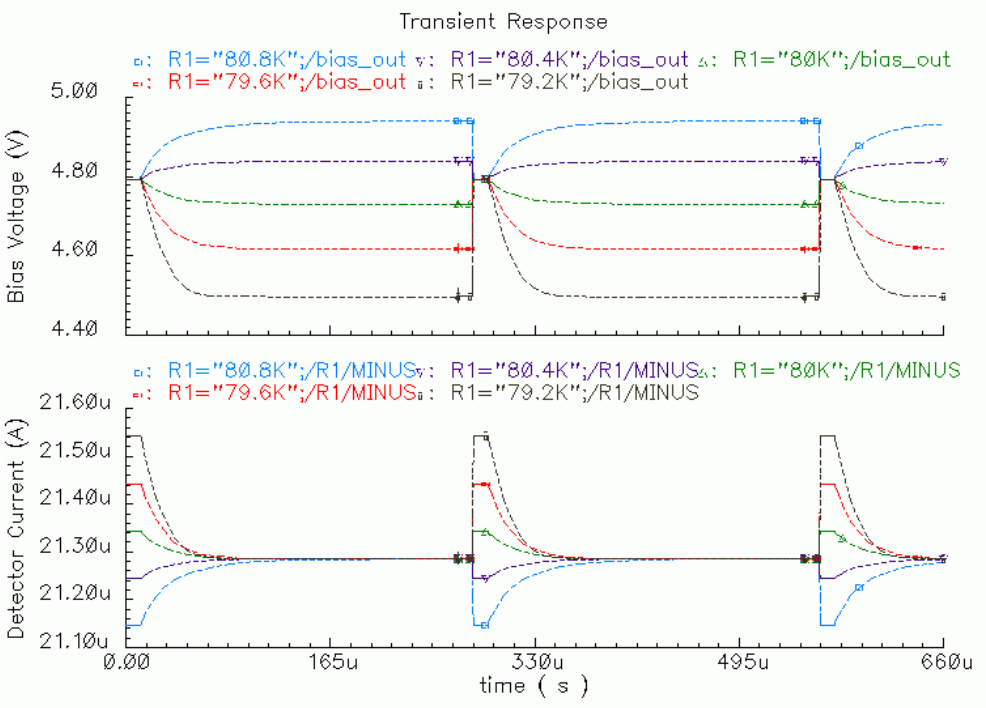


Figure 4.13: Simulation output that shows the circuit operation. Reference resistor is 79.2 KΩ and detector resistor is swept from 79.2 KΩ to 80.8KΩ with 0.4 KΩ increments. Different detector resistance values result in different bias voltage levels.

Self heating of the detector resistor should be considered for such a dynamic circuit, which equalizes the detector and reference currents. Figure 4.14 shows the

simulation result that shows the circuit operation, where the reference resistor is 80 KΩ, detector resistor is swept from 76 KΩ to 84 KΩ with 2 KΩ increments, and the detector resistance changes 1.2 KΩ due to self heating. For each value of the detector resistance, the detector current finally becomes equal to the reference current independent of the detector resistance value. In this case, resistance information can also be extracted from the final bias voltage level.

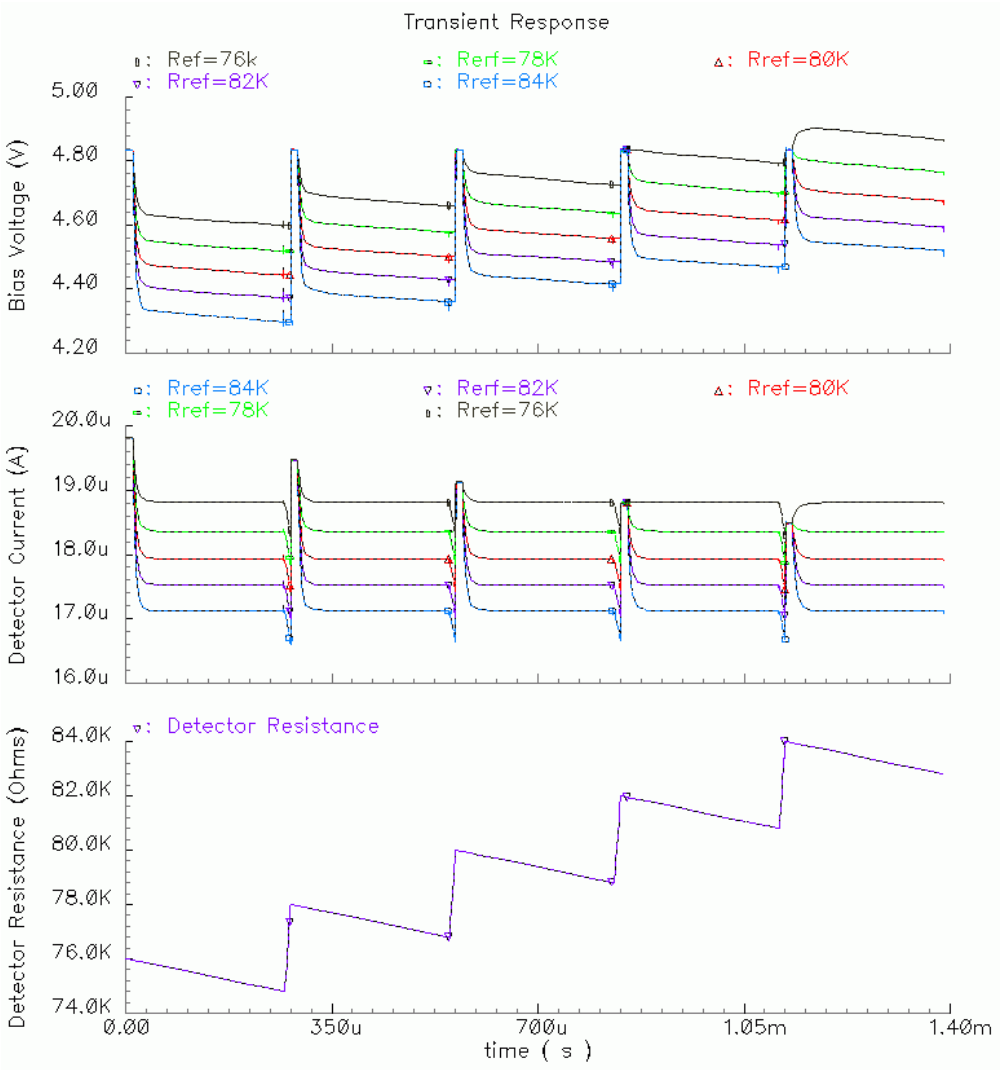


Figure 4.14: Simulation result that shows the circuit operation, where the reference resistor is 80 KΩ, detector resistor is swept from 76 KΩ to 84 KΩ with 2 KΩ increments, and the detector resistance changes 1.2 KΩ due to self heating.

A simple NMOS inverter with resistive load is used in the feedback loop as shown in Figure 4.12. The inverter provides the connection between the integrator output and the bias voltage of the auxiliary injection transistor, where these voltages should change in reverse direction, i.e., one should increase, while the other decreases, for the proper operation of the dynamic circuit. Figure 4.15 shows the transfer characteristic of the inverter for different load resistors ranging from 6 KΩ to 12 KΩ. In this application the minimum bias voltage of the auxiliary injection transistor is 3.9 V. Therefore, the load resistor should be selected as small as possible and be 10 KΩ, considering increased integrator output range.

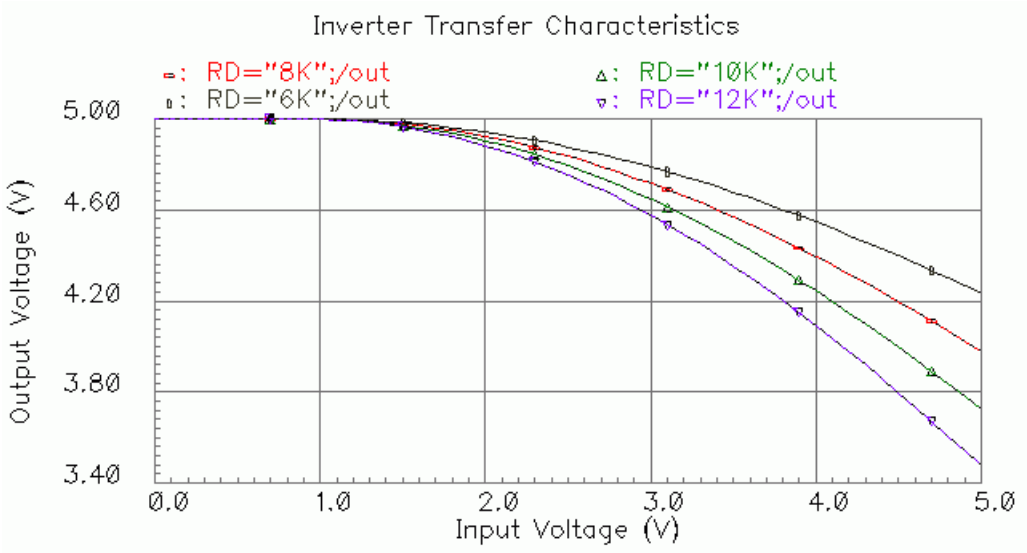


Figure 4.15: Transfer characteristic of the inverter between the integrator output and the bias voltage of the auxiliary injection transistor for different load resistors ranging from 6 KΩ to 12 KΩ.

Noise of the inverter is very critical, because its output is directly connected to the gate of the auxiliary transistor. Figure 4.16 shows simulated rms output voltage noise of the inverter circuit in an electrical bandwidth of 2 KHz for different input levels. For the worst case when the integrator input is 5 V, the rms noise voltage is

1.76 μV, corresponding to 1.47 pA rms detector noise current, which is ignorable with respect to the thermal noise of the detector and reference resistors.

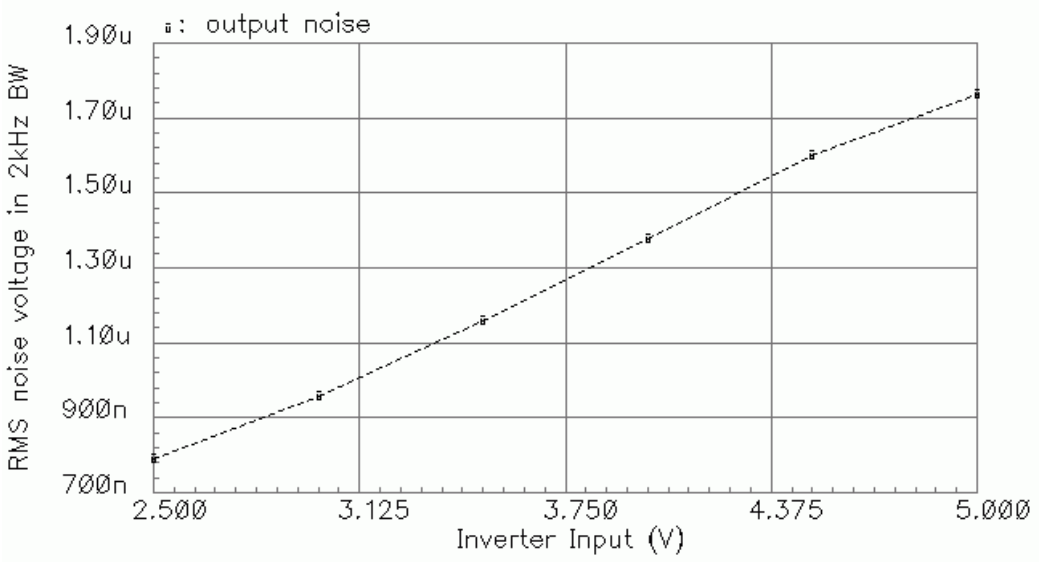


Figure 4.16: Simulated rms output voltage noise of the inverter circuit in an electrical bandwidth of 2 KHz for different input levels. For the worst case when the integrator input is 5 V, the detector referred rms current noise is 1.47 pA, which is ignorable with respect to the thermal noise of the detector and reference resistors.

In this dynamic operation with a feedback circuit, the switched capacitor integrator circuit does not limit the bandwidth of detector current noise as explained in Section 2.1. In the CTIA, the detector current noise is limited by a frequency inversely proportional to the integration time, because when the detector current is integrated through the integrator, the high frequency noise currents cancel out each other. If the integration time is very long, more noise currents cancel out. However, in this dynamic circuit the bias voltage of the auxiliary injection transistor, which is sampled and hold, is not an integrated signal with noise limited. This bias voltage is instantaneous and its noise is limited only by the passive filters seen from that node. In order to find the noise bandwidth of the circuit, periodic steady state analysis is

performed. Figure 4.17 shows the integrator output, which is bandwidth limited by 11.7 KHz.

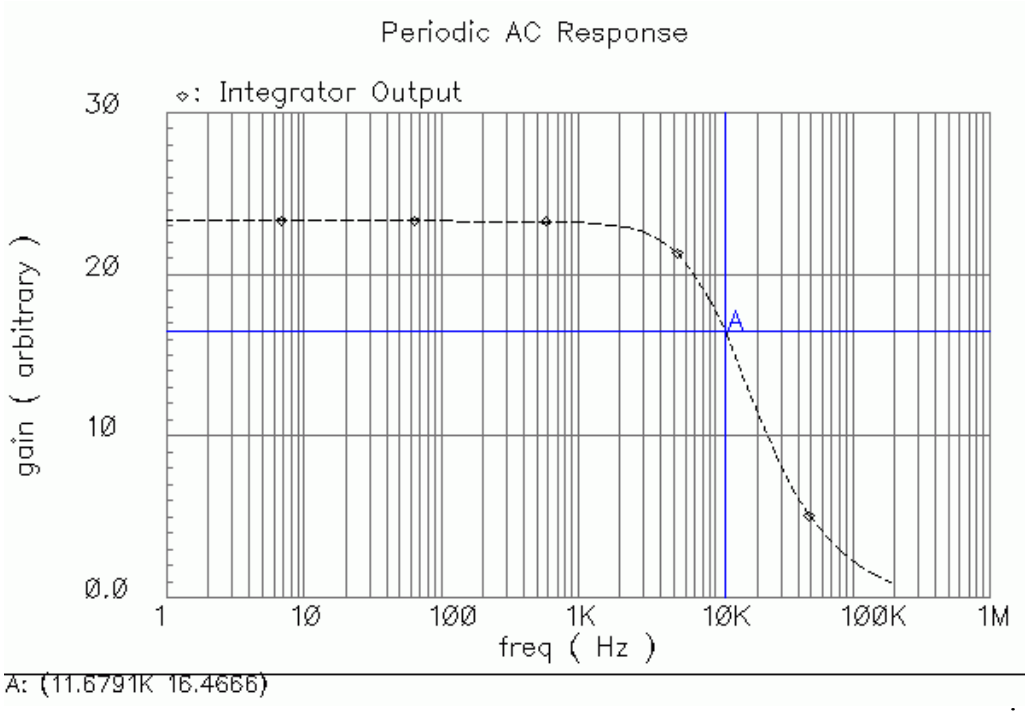


Figure 4.17: Periodic steady state simulation result showing that the integrator output is bandwidth limited by 11.7 KHz.

Figure 4.18 shows the simulated noise power spectral density of the integrator output. The rms noise voltage is 0.17 mV in an electrical bandwidth of 11.7 KHz. When the detector resistance changes by 1.6 KΩ, the integrator output changes 1.27 V. Assuming that the maximum resistance change due to infrared radiation is one thousandth of the detector resistance, 80 Ω, the expected SNR of the circuit is equal to 374.

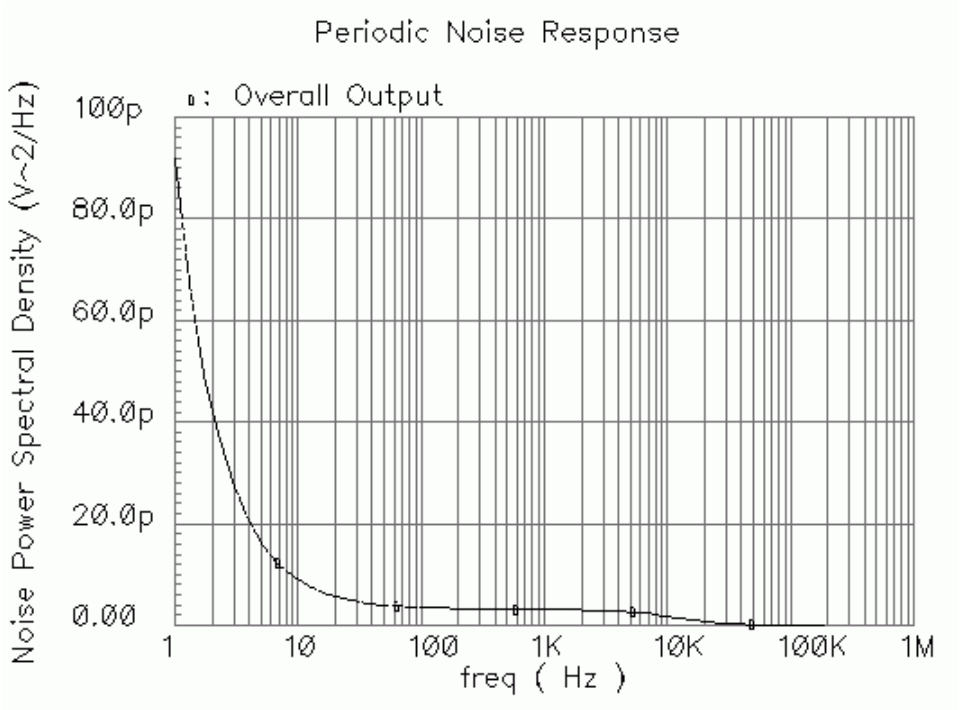


Figure 4.18: Simulated noise power spectral density of the integrator output. The rms noise voltage is 0.17 mV in an electrical bandwidth of 11.7 KHz, which corresponds to 294 pA detector noise current.

4.3. Overall Design

The improved readout circuit for resistive microbolometers with static and dynamic operation modes is implemented by a standard 0.6 µm 5 V CMOS process. Figure **4.19** shows the floor plan and pad frame of the designed chip. Figure 4.20 shows the complete layout of the chip, which measures 1539 µm x 819 µm (1.26 mm^2) in a 2-metal/2-poly CMOS process. Finally, Figure 4.21 shows the picture of the fabricated chip.

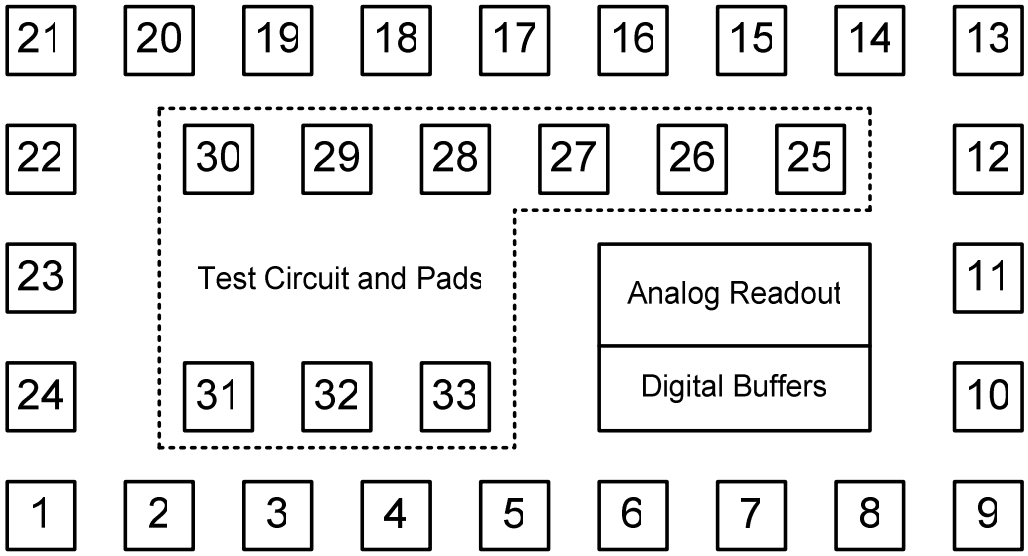


Figure 4.19: Floor plan and pad frame of the chip.

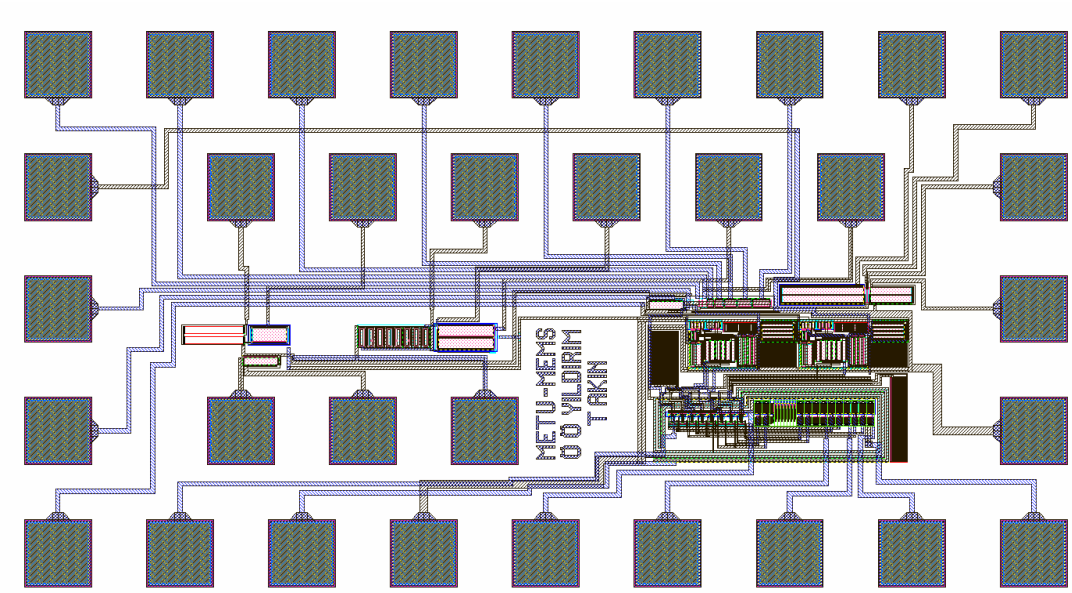


Figure 4.20: Layout of the whole chip, which measures 1539 µm x 819 µm (1.26 mm^2) in a 2-metal/2-poly CMOS process.

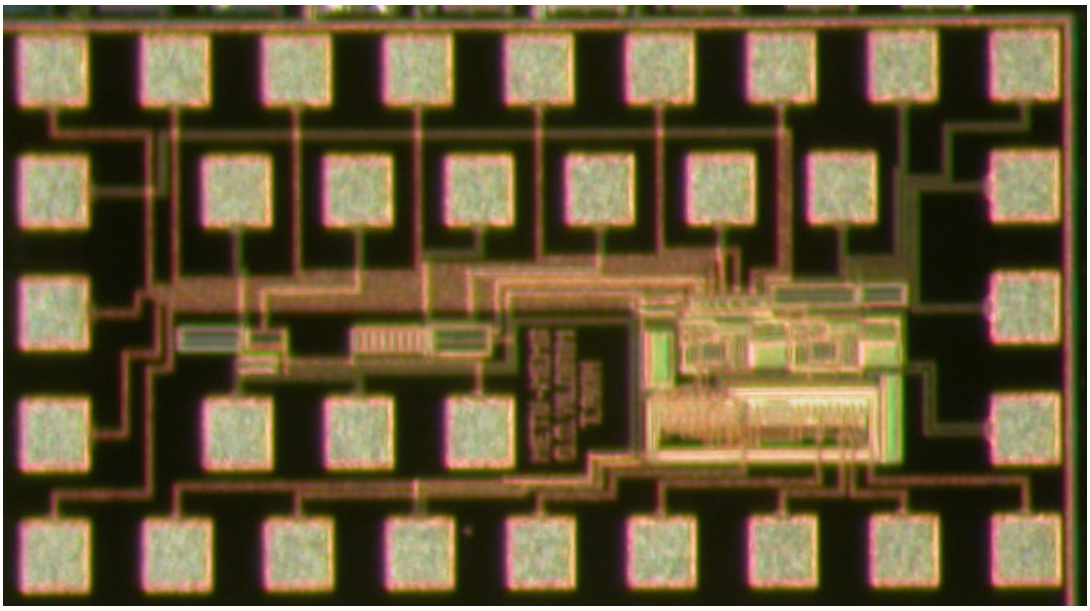


Figure 4.21: Picture of the fabricated chip.

4.4. Test Results

This section gives test results of the fabricated chip. A two-layer printed circuit board (PCB) is prepared in order to test the circuit. Figure 4.22 shows the picture of the two-layer PCB.

Timing control signals of the circuit are generated by a XILINX FPGA circuit board and the same as those of the CTIA type readout electronics. Figure 4.23 shows the illustrated timing control signals, where *reset*, *integ*, and *sample* signals are non-overlapping signals. XILINX simulation results of the designed timing circuit, and the scope views that show generated timing signals are given in Section 2.4.1. While the *integ* signal represents the integration period for the static mode of the circuit, it represents the current equalization period for the dynamic mode of the circuit.

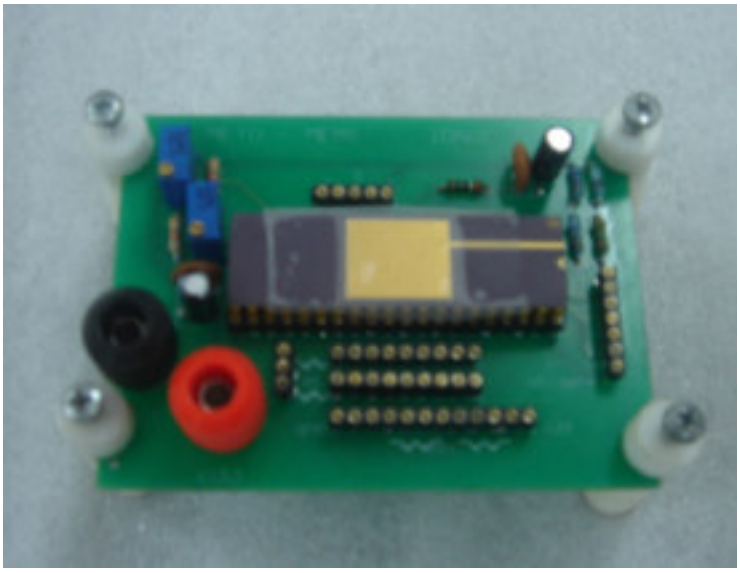


Figure 4.22: Picture of the two-layer printed circuit board for test measurements of the readout chip.

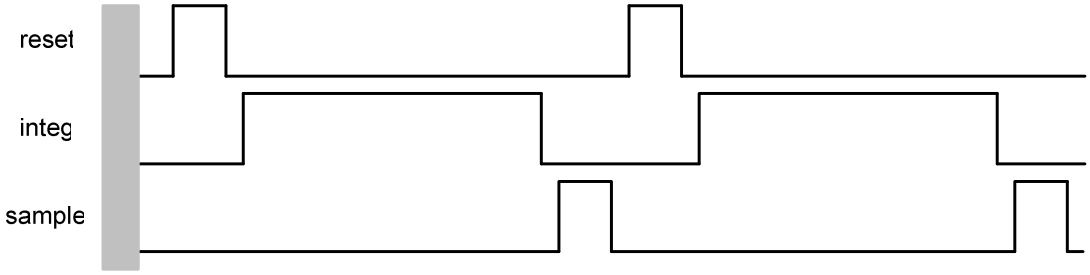


Figure 4.23: Illustrated timing of control signals of the readout chip.

Figure 4.24 shows the measured detector current with respect to bias voltage of the auxiliary injection transistor for 79.5 KΩ, 80 KΩ, and 80.5 KΩ detector resistors, since the resistance nonuniformity is reduced to ±0.625% by using 3-bit DACs connected to the gate of the main injection transistors. The detector current is the highest for 79.5 KΩ detector resistance for a fixed bias voltage, as expected. In order to achieve 21 μA detector current the bias voltage changes in a 0.34 V range. When this range is control by a 4-bit DAC using multiple analog buses, the detector

current can be adjusted with a resolution of less than 20 nA, which corresponds to more than 105 times current compensation considering the peak-to-peak variation in the detector current is around 2.1 μA for ±5% resistance nonuniformity.

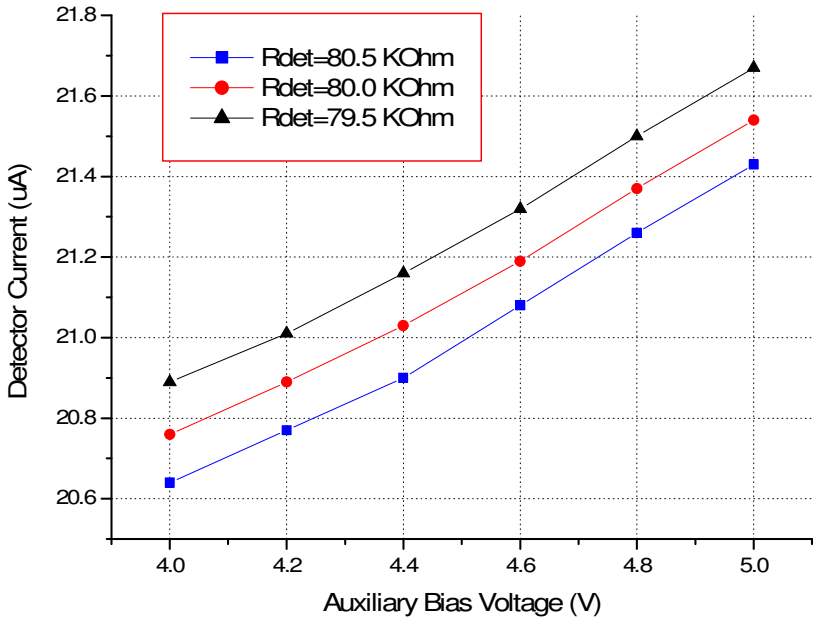


Figure 4.24: Measured detector currents with respect to the bias voltage of the auxiliary injection transistor for 79.5 KΩ, 80KΩ, and 80.5 KΩ detector resistors. The current can be adjusted with a resolution of better than 20 nA by using a 4-bit DAC with multiple analog buses.

Figure 4.25 shows the switched capacitor integrator circuit output when bias voltages of all injection transistors are constant. When the detector resistance increases by 400 Ω, the detector current decreases by 105 nA, and integrator output changes 1.84 V. Therefore, the gain of the switched capacitor integrator circuit is 1.75×10^7 V/A, where the expected value is 1.9×10^7 V/A.

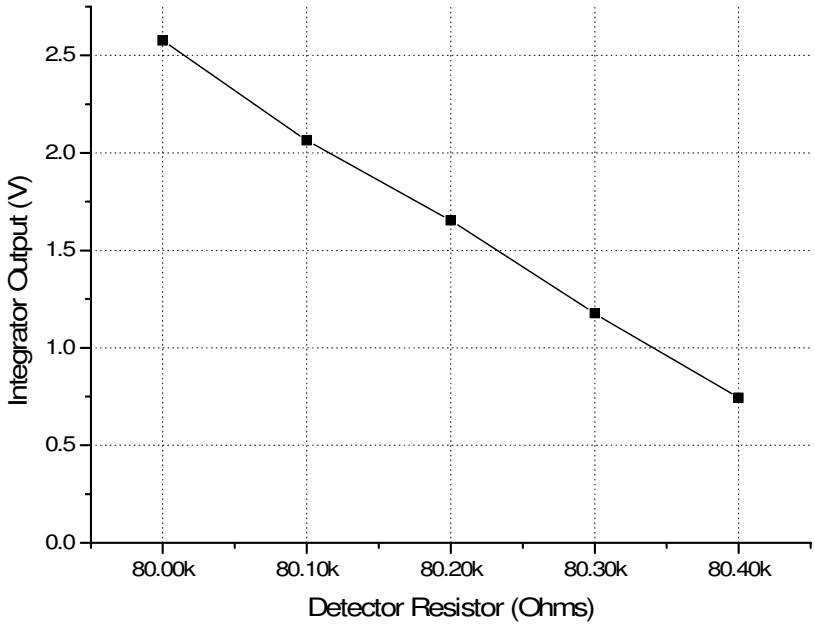


Figure 4.25: The switched capacitor integrator circuit output when the bias voltages of all injection transistors are constant. The gain of the circuit is measured as 1.75×10^{7} V/A, where the expected value is 1.9×10^{7} V/A.

Figure 4.26 shows the noise power spectral density of the output current of the biasing circuit and the fitted curve. From the fitted curve, the thermal noise floor of the biasing circuit with compensation DACs, i_{th}^2, is found as 4.10×10^{-25} A^2/Hz, and K_f is found as 7.33×10^{-23}. Hence, the calculated 1/f corner frequency is 179 Hz. Total rms current noise is calculated as 36 pA in a 1.3 KHz bandwidth, 48.6 pA in a 2.6 KHz bandwidth, and 59.6 pA in a 5.2 KHz bandwidth. These values are higher than simulation results, where the 1/f noise of the resistors is not taken in account. Assuming that the maximum infrared induced current on 21 μA detector bias current is 21 nA, the expected SNR of the readout circuit is 432 in an electrical bandwidth of 2.6 KHz.

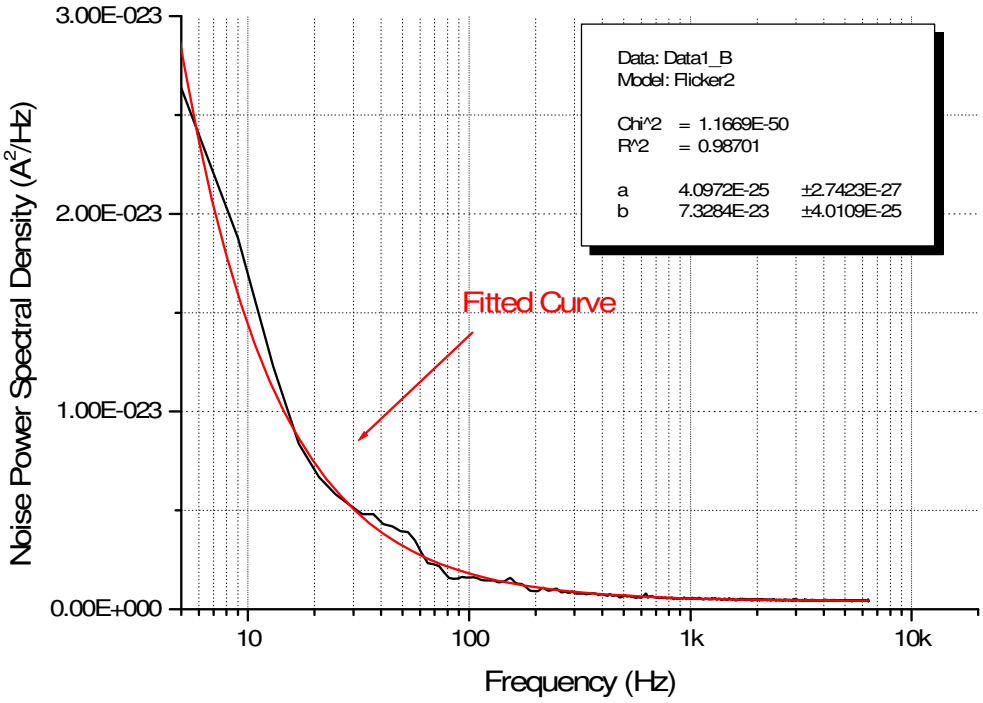


Figure 4.26: Measured noise power spectral density of the output current of the biasing circuit and the fitted curve.

The functionally of the dynamic mode of the circuit is tested by observing the integrator output for different values of the detector and reference resistors. Figure **4.27** shows the measured integrator output voltage after the current equalization process for 79.0 KΩ, 79.8 KΩ, and 80.4 KΩ detector and reference resistors. The integrator output voltage is the highest for 80.4 KΩ reference resistor for a fixed detector resistor value and the lowest for 80.4 KΩ detector resistor for a fixed reference resistor value. Since the output of the integrator is connected to the gate of the auxiliary injection transistor through an inverting stage, increased integrator output means reduced bias voltage, and hence reduced detector current. The dynamic circuit can equalize detector and reference currents successfully. The detector resistance change can be extracted from the integrator output, thus the integrator output also includes information about the amount of infrared radiation.

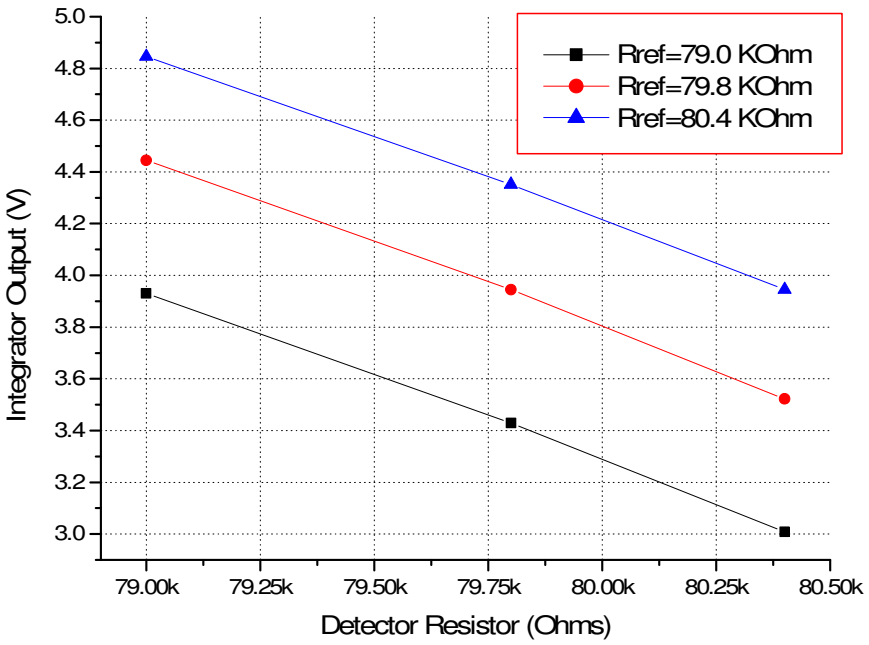


Figure 4.27: Measured integrator output voltage after the current equalization process for 79.0 KΩ, 79.8 KΩ, and 80.4 KΩ detector and reference resistors.

Noise performance of the circuit is tested by connecting a 16-bit analog-to-digital converter (ADC) to the output of the sample-and-hold circuit, which follows the switched capacitor integrator output. Fluctuations are observed on the least significant 10 bits of the output which corresponds to 74 mV peak-to-peak noise voltage at the output, considering the step size of the ADC is around 72.5 μV [66]. Assuming that the noise power spectral density of the output voltage has a Gaussian distribution, and then there is a 98% probability of that the voltage values are within ±3σ range of the mean voltage value. Here, σ corresponds to the rms voltage noise, thus the rms voltage noise at the output of the sample-and-hold circuit is 12.3 mV. Therefore, the measured SNR of the dynamic circuit is only 4, assuming that the maximum infrared induced current on 21 μA detector bias current is 21 nA.

4.5. The Improved Dynamic Nonuniformity Compensation Circuit

Based on the test results of the three fabricated readout chips, an improved dynamic nonuniformity compensation circuit is proposed in this section. A low area and high performance readout circuit with dynamic resistance nonuniformity capability can be designed by combining the static and dynamic readout circuits, which are explained in this chapter.

Figure 4.28 shows the simplified schematic of the improved dynamic nonuniformity compensation circuit. The proposed circuit has two phases of operation. During the first phase, the resistance nonuniformity is compensated, whereas during the second phase, the detector current is integrated. The readout circuit uses double biased detector resistor, where the detector current is integrated by a CTIA amplifier. While the main injection transistors of the biasing circuit are supplied by 3-bit DACs using multi channel analog buses, the gate of the auxiliary injection transistor of the biasing circuit is connected to the inverter output, where the inverter circuit forms the feedback loop between the integrator output and the gate of the auxiliary injection transistor. In the first phase, which can also be called the dynamic phase, the detector and reference currents are equalized by the feedback loop. The bias information of the auxiliary injection transistor is kept at the output of the integrator. After the bias voltage adjustment, the second phase, which can also be called the static phase, starts, where the compensated detector current is integrated through another switched capacitor integrator circuit. When the signal integration is completed, the output voltages of two integrators are sampled and hold. The infrared data can be extracted form these two outputs.

The readout circuit is composed of a double biasing circuit, two 3-bit DACs using multi channel analog buses, two switched capacitor integrator circuits, two sample-and-hold circuits, and an inverter circuit. Therefore, the expected area of the circuit is 780 µm x 130 µm (0.10mm^2) in a standard 0.6 µm 2-metal/2-poly CMOS process. The expected SNR of the circuit is around 430, which is equal to the SNR of the

static readout circuit, which is explained in this chapter. In this circuit, the sampling noise at the gate of the auxiliary injection transistor can be ignored, because transconductance of the auxiliary transistor is low enough to suppress this voltage noise. The feedback circuit reduces the offset current due to the resistance nonuniformity from 4.2 μA to 30 nA, corresponding to a current compensation ratio of 140. Moreover, the circuit has a special feature that it provides continuous compensation for the detector and reference resistances due to temperature changes over time.

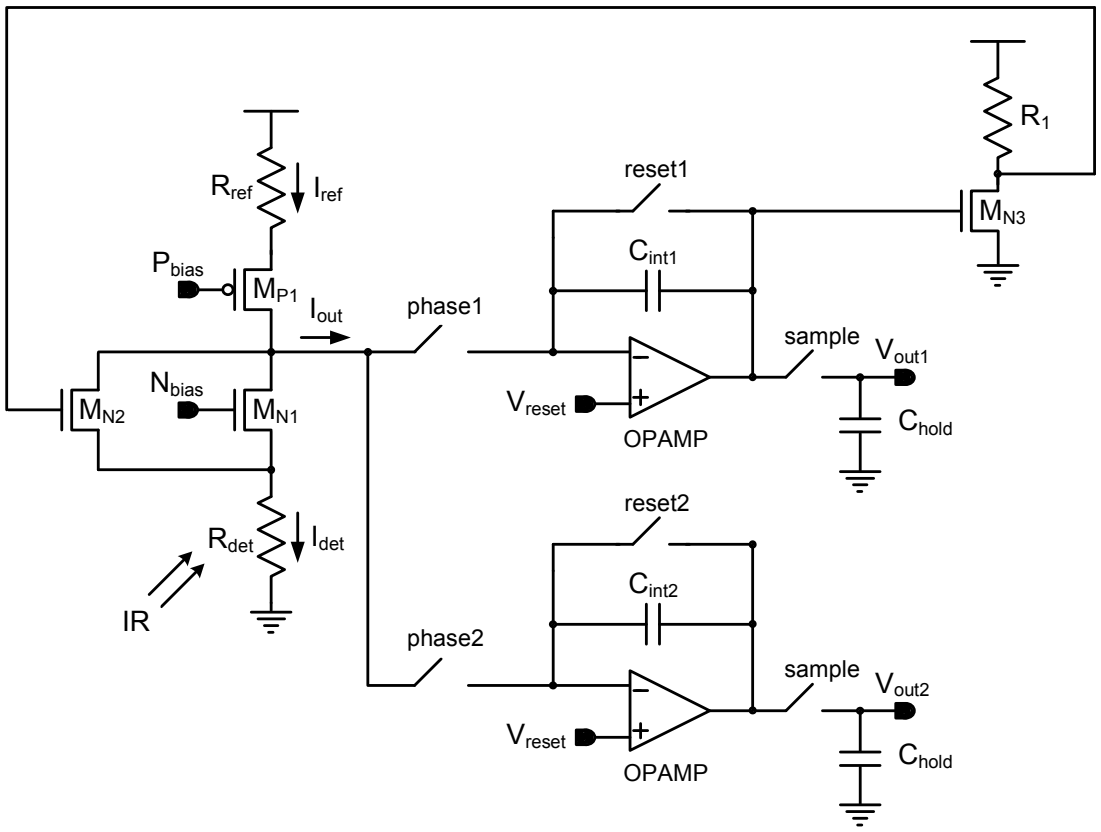


Figure 4.28: Simplified schematic of the improved dynamic nonuniformity compensation circuit.

4.6. Conclusions

This chapter presents an improved CTIA type readout circuit for resistive microbolometer detector arrays. The circuit is fabricated by a standard 0.6 µm 5 V CMOS process. The fabricated chip occupies an area of 1539 µm x 819 µm (1.26 mm^2), where the area of the readout circuit measures around 600 µm x 130 µm (0.08 mm^2). The circuit has two modes of operation, namely the static and dynamic modes.

The static circuit modifies the conventional capacitive transimpedance amplifier (CTIA) with waiving a little performance, gaining a lot of area, and simplifying the operation. Moreover, the small area property of the new circuit enables to put increased number of readout channels in a microbolometer chip, which decreases the electrical bandwidth and electrical noise, and hence increases the microbolometer performance. The bias current of the reference resistor is set by a 3-bit DAC, while the bias current of the detector resistor is set by a 3-bit DAC connected to the main bias transistor and by a 4-bit DAC connected to the auxiliary bias transistor. The maximum compensated offset current of the circuit is equal to 20 nA which corresponds to a current compensation ratio of 210, 7.7 bit. The measured rms current noise is 48.6 pA in an electrical bandwidth of 2.6 KHz. Assuming that the maximum infrared induced current on 21 µA detector bias current is 21 nA, the expected SNR of the readout circuit is 432.

The circuit also works with a dynamic mode, solving some problems of the dynamic resistance nonuniformity compensation circuit, which has been presented in Chapter III, such as the circuit has only one output pin instead of three, and the sampling noise at the output is ignorable in the new circuit. Nevertheless, the circuit has a very low performance, i.e., the measured SNR of the circuit is only 4, while the simulated SNR is 374. This huge difference is because of the fact that the circuit is not bandwidth limited by the integrator circuit, but it is bandwidth limited by the passive filters seen from the output node. Both the standard AC analysis and the

periodic steady state analysis tools of the Cadence simulation program fail to calculate the electrical bandwidth of the circuit. While the periodic steady state simulation results show that the bandwidth of the circuit is 11.7 KHz, the actual bandwidth is much larger than the simulation result, because the noise of the last integrated noise current directly affects the output, which is not considered by the simulation tool. In brief, the circuit has a very low performance in terms of current amplification, but it has a good performance in terms of current nonuniformity compensation.

Furthermore, an improved dynamic resistance nonuniformity compensation circuit is proposed in this chapter. The circuit combines properties of both circuits presented in this chapter; i.e., high SNR with dynamic compensation capability. Expected area of the circuit is 780 µm x 130 µm (0.10mm^2) in a standard 0.6 µm 2-metal/2-poly CMOS process. While the circuit dynamically reduces the maximum offset current 140 times, it provides an expected SNR of 430. Table 4.1 summarizes the performance parameters of the fabricated chip with two different modes and the proposed circuit.

Table 4.1: Performance parameter summary of readout circuits.

	Fabricated Circuit		**Proposed Circuit**
	Static	**Dynamic**	
Circuit Area	600 x 130 µm	600 x 130 µm	780 x 130 µm
Max. Comp. Current	20 nA	30 nA	30 nA
Compensation Ratio	210	140	140
Compen. Resolution	7.7	7.1	7.1
Detector Current Noise	48.6 pA	5.2 nA	48.6 pA
SNR	430	4	430
Dynamic	No	Yes	Yes

CHAPTER V

CONCLUSIONS AND FUTURE WORK

The research performed in this study involves the development of high performance readout electronics for resistive microbolometer detector arrays. Three different preamplifiers are designed and fabricated. The first design is a CTIA type readout circuit with compensation DACs, which is capable of low noise amplification with high SNR and compensating the resistance nonuniformity to prevent the saturation of the readout electronics. The second design introduces totally a new idea: dynamic nonuniformity compensation. However, this novel circuit has comparatively low SNR. The third design has two modes of operation. The first mode improves the first design which uses compensation DACs and achieves almost the same performance with considerably decreasing the circuit area. The second mode of the third design solves some problems of the dynamic nonuniformity compensation circuit; nevertheless, it still has a low performance. Based on the results obtained from all the fabricated preamplifiers, a new preamplifier circuit is proposed.

Achievements carried out during this research can be summarized as follows:

1. Resistive microbolometer readout circuits in the literature are investigated. Performance parameters of resistive microbolometer preamplifiers are defined. Effect of nonuniformities formed in the microbolometer fabrication process is simulated using MATLAB program. Nonuniformity compensation restrictions of a high performance readout circuit are determined.

2. A CTIA type resistive microbolometer readout circuit with compensation DACs, which is capable of low noise amplification with high SNR, is designed and fabricated. DACs using multiple analog buses are used for resistance nonuniformity compensation. Although DACs are controlled by 6-bit input, they have a better resolution than conventional 10-bit DACs because of the multiple analog bus structure of the DAC. The circuit is fabricated by a standard 0.6 µm CMOS process. The fabricated chip occupies an area of 2079 µm x 974 µm (2 mm^2), where the area of the readout circuit measures around 2700 µm x 200 µm (0.54 mm^2). The measured maximum compensated offset current is 100 nA, which corresponds to a current compensation ratio of 51 for 80 KΩ detector and reference resistors with resistance nonuniformity of ±5%. The measured rms detector current noise is 47.2 pA in an electrical bandwidth of 2.6 KHz, corresponding to an expected SNR of 530.

2. A new approach for compensating resistance nonuniformity of uncooled microbolometers is presented. Contrary to conventional nonuniformity compensation circuits, this approach eliminates the need for digital-to-analog converters (DACs), which usually occupy a large area and dissipate high power. The proposed circuit uses a feedback structure that dynamically changes the bias currents of the reference and detector resistors and does not need complicated external circuitry. A special feature of the circuit is that it provides continuous compensation for the detector and reference resistances due to temperature changes over time. The circuit is fabricated by a standard 0.6 µm CMOS process. The fabricated chip occupies an area of 4450 µm x 342 µm (1.5 mm^2) where the area of the readout circuit measures around 630 µm x 160 µm (0.10 mm^2). According to test results, the circuit reduces the maximum offset current due to resistance nonuniformity from 5.1 µA to 0.12 µA in only 12 µsec, i.e., a current compensation ratio of 42.5. The calculated rms current noise is around 360 pA in an electrical bandwidth of less than 8 KHz. Considering this amount of detector noise and the circuit responsivity, the expected SNR of the readout circuit is 70.

3. An improved readout circuit for resistive microbolometer detector arrays is designed and fabricated. The circuit modifies the conventional CTIA circuit with waiving a little performance, gaining a lot of area, and simplified operation. Moreover, the small area property of the new circuit enables to put increased number of readout channels in a microbolometer chip, which decreases the electrical bandwidth and electrical noise, and hence increases the microbolometer performance. The circuit is fabricated by a standard 0.6 µm CMOS process. The fabricated chip occupies an area of 1539 µm x 819 µm (1.5 mm^2), where the area of the readout circuit measures around 600 µm x 130 µm (0.08 mm^2). The measured maximum compensated offset current is 20 nA, which is equivalent to a current compensation ratio of 210 for 80 KΩ detector and reference resistors with resistance nonuniformity of ±5%. The measured rms detector current noise is 48.6 pA in an electrical bandwidth of 2.6 KHz, corresponding to an expected SNR of 430. If the number of readout channels in a microbolometer chip is doubled due to the small area property of this readout circuit, the electrical bandwidth reduces to 1.3 KHz, hence the detector noise current and the microbolometer SNR become 36.0 pA and 585, respectively.

4. Another totally new approach is presented for compensating resistance nonuniformity of uncooled microbolometers. Nevertheless, this new dynamic circuit still has low SNR, and needs to be improved. The circuit occupies an area of 600 µm x 130 µm (0.08 mm^2). The measured maximum compensated offset current is 30 nA, which is equivalent to a current compensation ratio of 140 for 80 KΩ detector and reference resistors with resistance nonuniformity of ±5%. The problem of the circuit is that the electrical bandwidth of the circuit is limited by capacitors instead of a switched capacitor integrator. Hence, the measured detector current noise is very high and equal to 5.2 nA independent of the electrical bandwidth. Considering this amount of the detector noise and the circuit responsivity, the expected SNR of the readout circuit is only 4. The circuit is not proper to be

a low noise preamplifier, but it works well for a compensation circuit. Thus, it needs an additional structure for low noise current integration.

5. Based on the measurement results obtained from the dynamic nonuniformity compensation circuit and improved CTIA type readout circuit, a new readout circuit is proposed. This circuit is capable of low noise amplification with high SNR and dynamic resistance nonuniformity compensation property. The circuit is expected to occupy an area of 780 µm x 130 µm (0.10 mm^2). The calculated maximum compensated offset current is 30 nA, which corresponds to a current compensation ratio of 140 for 80 KΩ detector and reference resistors with resistance nonuniformity of ±5%. Calculated detector current noise is 48.6 pA in an electrical bandwidth of 2.6 KHz and the expected SNR of the readout circuit is 430. Furthermore, the small area property of this circuit enables to put increased number of readout channels in a microbolometer chip, which improves the microbolometer performance.

Table 5.1 gives the characteristic of the three fabricated chips. Table 5.2 compares the performance parameters of the fabricated chips and the proposed circuit.

Table 5.1: Characteristic of the fabricated chips.

Fabrication Technology	0.6 µm 5 V CMOS
Nominal Resistance	80 KΩ
Resistance Nonuniformity	±5%
Detector Bias Current	25 µA (1^{st} and 2^{nd} chips) 21 µA (3^{rd} chip)
Max. Uncompensated Current	5.1 µA (1^{st} and 2^{nd} chips) 4.2 µA (3^{rd} chip)

Table 5.2: Performance parameter summary of the fabricated chips and the proposed circuit.

	1st chip	2nd chip	3rd chip		Proposed Circuit
	CTIA type Readout	Dynamic Readout	Improved Readout		
			Static	Dynamic	
Circuit Area	2700 µm x 200 µm (0.54 mm^2)	630 µm x 160 µm (0.10 mm^2)	600 µm x 130 µm (0.08 mm^2)	600 µm x 130 µm (0.08 mm^2)	780 µm x 130 µm (0.10mm^2)
Max. Comp. Current	100 nA	120 nA	20 nA	30 nA	30 nA
Compensation Ratio	51	42.5	210	140	140
Compensation Resolution	5.7 bit	5.4 bit	7.7 bit	7.4 bit	7.4 bit
Detector Current Noise	47.2 pA	360 pA	48.6 pA	5.2 nA	48.6 pA
SNR	530	70	430	4	430
Number of Output Pins	1	3	1	1	2
Dynamic Compensation	No	Yes	No	Yes	Yes
Fabricated	Yes	Yes	Yes	Yes	No

Although an enormous effort has been expended to reach above achievements, there are still more points that need further study.

1. The proposed improved dynamic nonuniformity compensation circuit, which is explained in Section 4.5, is to be designed and fabricated.

2. A printed circuit board is to be implemented for testing the proposed circuit. Moreover, a high resolution analog-to-digital converter (ADC) card should be

prepared for measuring overall noise of the system. The output resolution of the ADC should be at least 20-bit in order to measure the sampling noise at the gate of the auxiliary injection transistor. Also, the noise of the ADC should be smaller than the sampling noise.

3. Since there are two output pins of the proposed readout circuit, the relation between the output voltages should be modeled. An FPGA card is to be designed to interpret these outputs.

4. Microbolometer chips with 320 x 240 array format can be implemented with the CTIA type readout electronics. Microbolometer chips with larger detector arrays, such as 640 x 480, can be implemented with the improved CTIA type readout electronics, which has a significantly smaller circuit area.

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