REPETITIVE CONTROL OF A THREE PHASE UNINTERRUPTIBLE POWER SUPPLY WITH ISOLATION TRANSFORMER

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

SÜLEYMAN ÇETİNKAYA

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
THE DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

DECEMBER 2006

Approval of the Graduate School of Natural and Applied Sciences

_____
Prof. Dr. Canan Özgen
Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

_____
Prof. Dr. İsmet Erkmen
Head of Department

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

_____
Asst. Prof. Dr. Ahmet M. Hava
Supervisor

Examining Committee Members

Prof. Dr. Aydın Ersak	(METU, EE)	_____
Asst. Prof. Dr. Ahmet M. Hava	(METU, EE)	_____
Prof. Dr. Yıldırım Üçtuğ	(METU, EE)	_____
Prof. Dr. Kemal Leblebicioğlu	(METU, EE)	_____
Dr. Recep Görür	(ELSİS Co.)	_____

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name : Süleyman Çetinkaya

Signature :

ABSTRACT

REPETITIVE CONTROL OF
A THREE-PHASE UNINTERRUPTIBLE POWER SUPPLY
WITH ISOLATION TRANSFORMER

Çetinkaya, Süleyman
M.S., Department of Electrical and Electronics Engineering
Supervisor: Asst. Prof. Dr. Ahmet M. Hava

December 2006, 184 pages

A repetitive control method for output voltage control of a three phase uninterruptible power supply (UPS) with isolation transformer is investigated. In the method voltage control loop is employed in the stationary dq frame. The controller eliminates the periodic errors on the output voltages due to inverter voltage nonlinearity and load disturbances. The controller design and implementation details are given. The controller is implemented on a 5-kVA UPS prototype which is constructed in laboratory. Linear and nonlinear loads for balanced and unbalanced load operating conditions are considered. The steady-state and dynamic performance of the control method are investigated in detail. The theory of the control strategy is verified by means of simulations and experiments.

Keywords: Three-phase, transformer, repetitive control, inverter, UPS, voltage control, PWM, space vector, stationary frame, THD, rectifier, active damping, discrete time control, nonlinear load, unbalanced operation, symmetric components.

ÖZ

ÜÇ FAZLI YALITIM TRANSFORMATÖRLÜ BİR KESİNTİSİZ GÜÇ KAYNAĞININ TEKRARLAMALI DENETİMİ

Çetinkaya, Süleyman
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Yrd. Doç. Dr. Ahmet M. Hava

Aralık 2006, 184 sayfa

Üç fazlı yalıtım transformatörlü bir kesintisiz güç kaynağının (KGK) çıkış gerilim denetimi için tekrarlamalı denetim yöntemi incelenmiştir. Yöntemde gerilim denetim çevrimi durağan dq koordinatlarda uygulanmaktadır. Deneteç, evirici gerilim doğrusalsızlığı ve yükleme bozucu etkilerinden kaynaklanan çıkış gerilimi periyodik bozulmalarını yoketmektedir. Denetecin tasarım ve uygulanma ayrıntıları verilmiştir. Deneteç, laboratuvar ortamında kurulan 5-kVA gücünde bir KGK ilk örnek üzerinde uygulanmıştır. Denetecin başarımı açısından doğrusal ve doğrusal olmayan, dengeli ve dengesiz yük durumları incelenmiştir. Denetim yönteminin kararlı hal ve dinamik davranışı ayrıntılı olarak incelenmiştir. Denetim yönteminin teorisi bilgisayarla benzetim ve deneylerle doğrulanmıştır.

Anahtar Kelimeler: Üç faz, transformatör, tekrarlamalı denetim, evirici, KGK, gerilim denetimi, darbe genişlik modülasyonu, PWM, uzay vektörü, durağan koordinatlar, THD, doğrultucu, etkin sönümlendirme, ayrık zamanlı denetim, doğrusal olmayan yük, dengesiz çalışma, simetrik bileşenler.

To My Family,
Ali İhsan, Sevil, and Seza Çetinkaya
for their patience and support
in all aspects of my life

ACKNOWLEDGMENTS

I would like to express my sincerest thanks to Asst. Prof. Dr. Ahmet M. Hava for his guidance, support and valuable contributions throughout the preparation for this thesis.

I express my deepest gratitude to my family, my father Ali İhsan, my mother Sevil, and my sister Seza for their encouragements throughout my education life.

Special appreciation goes to Eyyup Demirkutlu, Hasan Özkaya, and Mutlu Uslu for sharing their knowledge and valuable times with me during experimental studies. I also would like to thank my officemates Ömer Göksu, Mehmet Can Kaya, Ersin Küçükparmak, Osman Selçuk Şentürk, Emre Ün, Bülent Üstüntepe, Hazem Zubi and all my friends for their help and support.

I am grateful to my housemates Mehmet Deniz, Mahmut Sami Mert and Zülküf Oruç for their encouragements and support. I also thank to my friend Hasan Saim Vural for sharing his valuable experiences in academic life.

I would like to acknowledge TÜBİTAK for the scholarship and financial support for the hardware through the EEEAG research project grant number 104E009. Also partial funding for the hardware in this project was supplied by METU Graduate School of Natural and Applied Sciences project number BAP-2004-07-02-00-33.

I wish to thank to Middle East Technical University Department of Electrical and Electronics Engineering faculty and staff for their help throughout my graduate studies.

TABLE OF CONTENTS

LIST OF FIGURES

FIGURES

LIST OF TABLES

TABLES

CHAPTER 1

INTRODUCTION

1.1 Background

In the modern world, electricity has an indispensable role with its ability to combine power and intelligence. Most of the systems which are located in critical points in daily life need electricity to operate. The electrical energy increases productivity, efficiency, and allows a high degree of safety, reliability, and comfort of life. Contingency (interruption) in the electric power line can not be accepted critical areas involving safety (air traffic control, hospitals, railway systems etc.), security (military installations, police stations etc.), continuous industrial processes (semiconductor wafer processing plant, cement mill, textile machines, etc.), data protection in information technologies (internet service providers, banks etc.). Although in the past backup generators were satisfactory to get power in case of interruption in the utility, long delay of generator starting and switching in (usually a few seconds) today is not acceptable. Such delays badly affect critical loads such as computers, internet providers, telecom service providers, etc. as the power interruption causes data loss, process failure, and the cost for recovery becomes unacceptable. Even though the electric utility industry has made great effort for uninterrupted power line and undistorted line voltage, inevitably still there exist problems such as sag, swell, and spikes. Frequent contingencies are also fact of daily life in most residential areas in Turkey today. In order to avoid such problems, uninterruptible power supply (UPS) systems with continuous and clean output power are utilized.

There are two types of UPS systems. Rotary UPS systems utilize rotating electrical machinery such as electrical motors and generators and are typically utilized at high power ratings and combined with diesel generator systems for continuous power during long lasting power line contingencies. Static UPS which is the most commonly used type, is static (has no moving parts) as the name implies. Static UPS systems primarily employ power electronics components and passive elements (inductor, capacitor, transformer etc.).

Static UPSs are divided into three main types: on-line, off-line, and line-interactive [1]. Shown in Figure 1.1, the on-line UPS is mainly composed of rectifier/charger, DC bus capacitor (and/or batteries), inverter, inductor (and/or a transformer) and a capacitor filter (LC filter), and optionally a static by-pass switch. This topology is also termed as "double conversion UPS." The rectifier converts the AC utility voltage to DC voltage. The inverter converts the DC voltage to AC. The LC filter is employed to suppress the high frequency components of the inverter output voltage. The by-pass switch is utilized for either supplying the load directly from the power line during UPS maintenance/installation or for providing energy efficiency enhancement when there is no critical load operation during certain periods in an installation. Since the on-line UPS is connected to the load in series (it is always active), there is ideally no switching (transitioning) time and also the load is not affected by input voltage variations. In such a UPS system, galvanic isolation can be achieved by using an isolation transformer at the output.

The off-line UPS is connected parallel to the load as shown in Figure 1.2. During normal mode of operation the batteries are charged through the rectifier and the inverter stays in the stand-by mode. If the line voltage is not within the given tolerances, the UPS switches in and remains so until the line voltage returns to normal. The off-line UPS is efficient, however the slow transition (in and out) and limited capability are its main disadvantages.

The line-interactive UPS, shown in Figure 1.3, is connected to the load in parallel. Batteries are charged through the bidirectional converter. If the line voltage is problematic, the UPS provides power from its battery to the load.

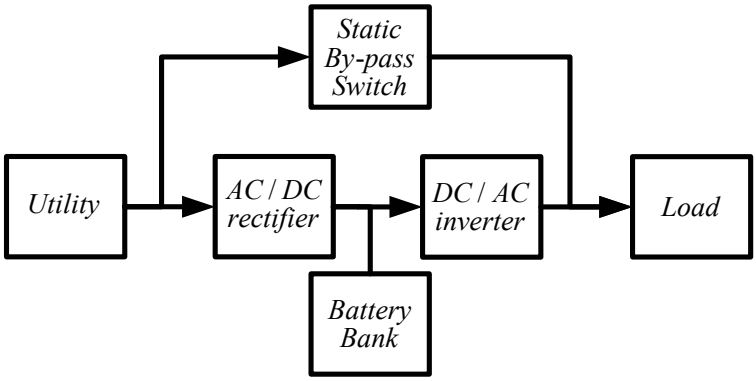

Figure 1.1 On-line UPS.

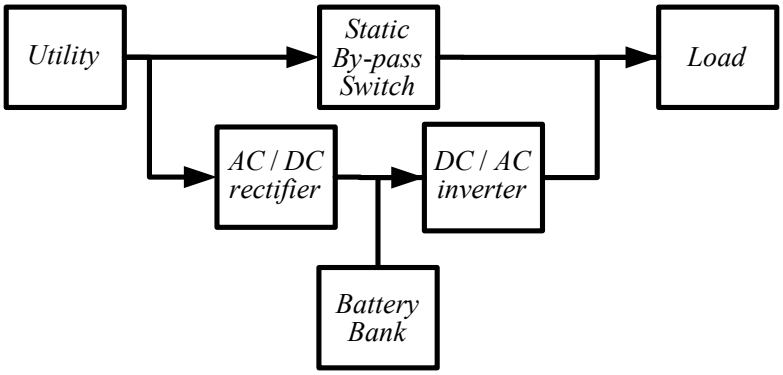

Figure 1.2 Off-line UPS.

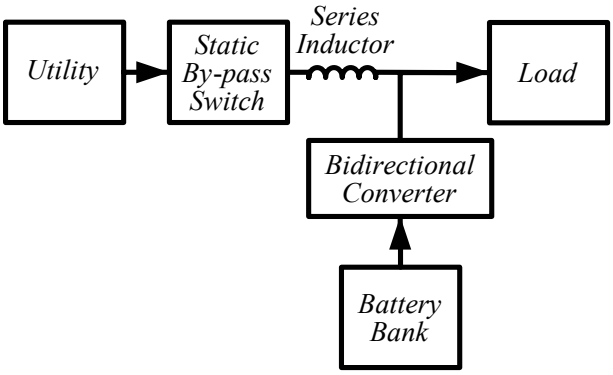

Figure 1.3 Line-interactive UPS.

Of the three static UPS system types, the on-line UPS is by far the most common. Due to the fact that its output performance is independent of the input and provides high performance frequency and voltage regulation, it has gained wide acceptance. This thesis focuses on on-line UPS systems.

In the following section, the standard UPS performance indices will be reviewed and the benchmark values will be provided. Then state of the art UPS systems will be reviewed and their evaluation according to the given benchmarks will be provided.

1.2 UPS Output Performance Criteria

The performance of a UPS is determined by its steady-state and dynamic output voltage characteristics. Nonlinear and unbalanced loading conditions are the most challenging conditions and output voltage quality of the UPS under these types of loads specifies the steady-state performance. Negative and/or zero sequence components of the load current render the output voltages unbalanced. Also, high harmonic content of the nonlinear load currents cause distortion on the output voltages. The shape of the current waveform (deviation from a sine wave) is a determining factor for load type and output voltage distortion. For this purpose the load current crest factor is defined in the following.

Crest Factor: The ratio of the current waveform peak value to its RMS value is defined as the Crest Factor (CF) as given in (1.1). For the non-sinusoidal voltage source and/or nonlinear load case, the CF is high such as 3 to 5 where it is $\sqrt{2}$ for sinusoidal source/load. A diode rectifier with capacitor at its DC bus draws current with a high crest factor from a supply with negligibly small impedance. But in the UPS applications the output impedance is finite and the maximum achievable crest factor depends on the design of the UPS used and its controller.

$$CF = \frac{I_{peak}}{I_{rms}} \tag{1.1}$$

Voltage Regulation: At steady-state the output voltage of a UPS should be maintained at the rated value regardless the operating condition. Since the output voltage variation is mainly loading dependent, the two extreme cases for loading define the two extremes in terms of output voltage RMS value. While the no-load operating condition usually provides the highest UPS output voltage, the rated load defines the lowest output voltage. In a high performance UPS, the output voltage is regulated well such that the output voltage at full-load does not deviate from the no-load value noticeably. Indicating the output voltage variation in terms of the rated output voltage, the Voltage Regulation (VR) is the percent variation of output voltage fundamental component from no-load to full-load and is given in (1.2). In the equation V_{nlrms1} is the no-load output voltage fundamental component RMS value and $V_{ratedrms1}$ (full-load) is the full-load output voltage fundamental component RMS value. Both can be taken as the output line to neutral or line to line quantities. Based on this definition, an ideal UPS has zero VR and in a practical UPS a small VR is required. Typically, a UPS with a VR of 1% or less is accepted as a high quality UPS in terms of output voltage regulation. However, acceptable values are 2% for balanced and 3% for unbalanced loading conditions. Since an unbalanced load poses significant deviations (from normal conditions) in the output voltage fundamental component, the unbalanced load case VR is less constrained and a value of 3% is acceptable under extreme unbalance [2].

$$VR(\%) = \frac{V_{nlrms1} - V_{ratedrms1}}{V_{ratedrms1}} \times 100 \tag{1.2}$$

Output Voltage Total Harmonic Distortion: A UPS system employs a voltage source inverter that generates high frequency output voltage pulses filtered by an LC filter. The LC filter causes finite output impedance to the UPS system. The harmonics on the load current and the effect of deadtimes of the inverter cause distortion on the output voltage waveform. The steady-state output voltage distortion at full loading condition is quantified with the voltage Total Harmonic Distortion (THD_v) given in

(1.3). Standard UPS products guarantee 3% and 5% THD_V for linear and nonlinear loading conditions respectively. But high quality UPS products guarantee 2% THD_V for linear loading and 3% THD_V for nonlinear loading.

$$THD_V(\%) = \sqrt{\frac{V_{rms}^2 - V_{1rms}^2}{V_{1rms}^2}} \times 100 \tag{1.3}$$

Voltage Imbalance: In three-phase UPS systems the output phases may not be loaded equally and load imbalance may exist among the phases. In such cases the output voltages may be affected differently due to different loading conditions. If a proper compensation mechanism is not implemented in the control algorithm, the output voltages may become unbalanced resulting in performance problems both at the load side and in the UPS. The steady-state output voltage imbalance is defined in various forms. According to the NEMA definition given in (1.4) the output voltage imbalance is defined in percentage in terms of UPS output line-to-line voltages [3].

$$V_{unbalance}(\%) = \frac{Maximum\ deviation\ from\ the\ mean\ of\ \{V_{ab}, V_{bc}, V_{ca}\}}{Mean\ of\ \{V_{ab}, V_{bc}, V_{ca}\}} \times 100 \tag{1.4}$$

The more standard and comprehensive definition of voltage imbalance in [4] and [5] is based on the symmetrical components approach. In this approach, the output voltage is decomposed to its positive, negative, and zero sequence components. The steady-state output voltage imbalance is defined for the negative and zero sequence components in percentage of the positive sequence component of the output voltage as given in (1.5) and (1.6). In this thesis, this symmetrical component decomposition based approach will be employed to quantify the output voltage imbalance. In state of the art UPS systems the output voltage imbalance for both components is typically less than 1% under the worst case load imbalances.

$$V_{unbalance\_negative}(\%) = \frac{V_{negative\_sequence}}{V_{positive\_sequence}} \times 100 \quad (1.5)$$

$$V_{unbalance\_zero}(\%) = \frac{V_{zero\_sequence}}{V_{positive\_sequence}} \times 100 \quad (1.6)$$

Dynamic Response: In addition to the steady-state performance characteristics given above, the dynamic performance of a UPS is also a determining factor of the UPS quality. Specifically, the loading transients may be too strong for a UPS that deep output voltage sags followed by oscillatory response may result. Likewise, rapid load reduction may cause significant surges and result in similar effect on the output voltage performance. Such dynamics may degrade the UPS performance and cause nuisances to other loads fed from the same UPS or even result in failure or shutdown of the UPS system disabling all the loads. Therefore, the dynamic performance of the UPS is critical in many applications and it is a measure for the overall acceptance of a UPS. In a UPS with high dynamic performance, the loading and unloading transients are manipulated rapidly and with minimal output voltage deviation from the ideal output voltage waveform. For this purpose the output voltage maximum deviation from the rated value is given as the measure of UPS dynamic performance. Described with the aid of Figure 1.4, the maximum output voltage deviation from the rated value, which is more frequently a lost voltage (corresponding to a sag during a loading transient) than a surge, is given in (1.7) in percentage of the rated output RMS voltage.

In this equation, ΔV is the difference between the initial voltage value given as $V_{initial}$ and the dip point of the voltage given as V_{dip}. For this purpose as the worst case loading transient, the peak of the sinusoidal voltage is considered as the initial voltage and typically the voltage dip percentage should be less than 20% in a high dynamic performance UPS.

$$V_{dip}(\%) = \frac{|\Delta V|}{|V_{initial}|} \times 100 = \frac{|V_{initial} - V_{dip}|}{|V_{initial}|} \times 100 \tag{1.7}$$

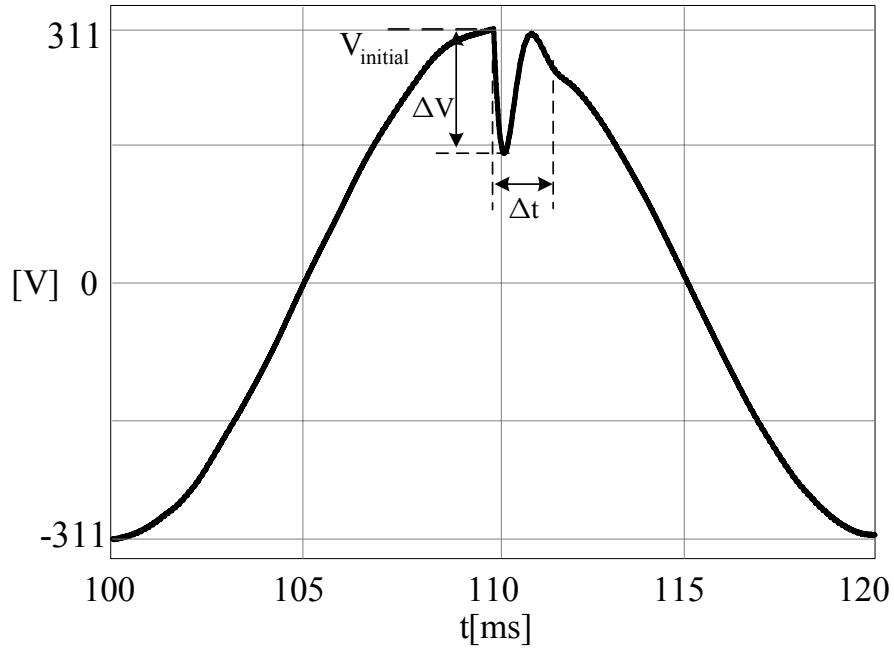

Figure 1.4 Dynamic response of a UPS under impact loading.

In addition to the dip, the duration of the sag (shown in Figure 1.4 as Δt) is also an important factor determining the dynamic performance. If the duration of the sag is small, the voltage dip percentage may not be too harmful to many loads involving energy storage elements (such as power supplies with diode rectifier front end involving large electrolytic capacitors in the DC bus). Thus, dips larger than 20%

may be tolerated provided that the time interval involved remains in several milliseconds. For this purpose the lost volt-seconds could be considered as another (and perhaps the most meaningful) measure to define the UPS dynamic performance.

1.3 State of the Art On-line UPS Systems

For supplying critical loads, on-line UPSs are commonly preferred since the load can fully be decoupled from the utility voltage disturbances. From here on, unless otherwise stated, the term UPS will imply an "on-line UPS." Various UPS power converter topologies have been developed for different application fields. Based on the application requirements, a suitable UPS topology is chosen by compromising advantages and disadvantages of each topology. Also, for each power converter topology various control methods are available. In the following first the power converter topologies and then the control methods are reviewed.

1.3.1 Power Converter Topologies of On-line UPS Systems

The power rating, energy efficiency, galvanic isolation requirement, dynamic performance, size, and the installation location of a UPS system affect the choice of the power converter topology. Usually for domestic low power usage and small office environments single-phase topologies are satisfactory. For high power industrial applications, large offices, public infrastructures (hospitals, railway systems, etc.) the three-phase UPS topologies are preferred.

There are two popular power converter topologies employed in single-phase UPSs: half-bridge inverter and full-bridge inverter. The half-bridge inverter topology (Figure 1.5) is commonly used for low power applications. This topology is more economical due to the reduced number of components. However, for increased magnitude of load currents the midpoint voltage of the DC bus oscillates since the inductor current circulates through the DC bus capacitor. Large size DC bus capacitors are utilized to overcome this problem at the expense of increase in size, and cost. The maximum achievable inverter output voltage is half the DC link voltage.

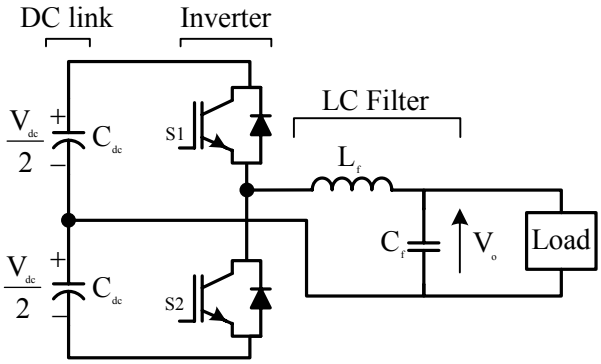

Figure 1.5 The half-bridge inverter topology based single-phase UPS.

For higher power levels the full-bridge inverter topology (Figure 1.6) is used. The maximum inverter output voltage is the DC link voltage in this topology. The frequency of the inverter output voltage can be made double the switching frequency of each leg by using unipolar PWM strategy [6]. Smaller values of the output LC filtering components can be used due to the effectively increased frequency.

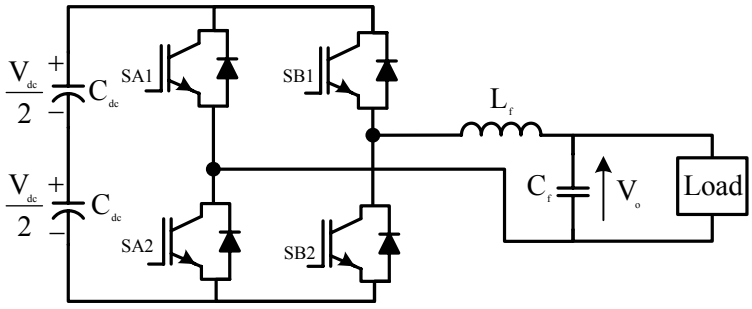

Figure 1.6 The full-bridge inverter topology based single-phase UPS.

In industrial applications, large offices, and public infrastructures (hospitals, railway systems, etc.) three-phase UPSs are preferred. There are several power converter topologies utilized in three-phase UPS systems.

The conventional three-leg three-wire inverter is commonly utilized in three-phase UPS applications. This inverter topology is generally used with a three-phase isolation transformer with Δ/Y (Δ/Z) winding connection in UPS applications (Figure 1.7). For feeding single-phase loads from a three-phase UPS, the Δ/Y (Δ/Z) connection of the transformer provides neutral terminal from the midpoint of Y (Z) connected secondary windings. A zero sequence current flows if the summation of the three-phase load currents is not zero. Single-phase loading of the UPS is the major reason of zero sequence currents. If a current path is not provided, zero sequence currents passes through the output capacitors of the UPS. This causes imbalance at the output voltages of the UPS. In such a transformer configuration, zero sequence currents circulate in the Δ connected primary windings. Thus, a three-leg three-wire inverter can be utilized in UPS systems employing a transformer with Δ/Y (or Δ /Z) connection. The isolation transformer also provides galvanic isolation.

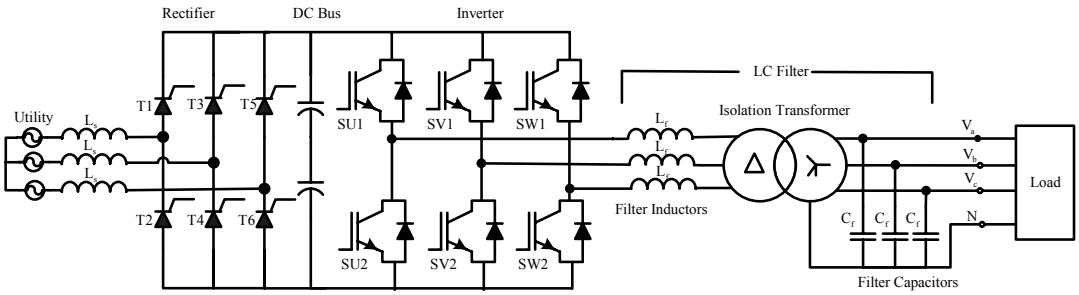

Figure 1.7 The three-phase three-wire inverter topology based UPS with an isolation transformer.

The inverter stage of this UPS is a step-down type converter. If a diode or thyristor rectifier used at the input stage of the UPS, the output voltage of the inverter can not be more than the utility voltage. Considering the inverter PWM voltage linearity limit and the rectifier voltage drop, the output voltage of the UPS is less than the input and typically below 90% of it. Considering that the inverter output filter also results in voltage drop, the available voltage is further reduced. As a result, the

output voltage of a three-leg three-wire inverter based transformer-less UPS can not be regulated to the rated utility voltage. For proper regulation of the output voltage, the DC bus voltage could be increased by using a PWM rectifier at the input stage. Increase in DC bus voltage causes the switches to operate under high stress. This results in increase of switching losses and EMI in the UPS. Therefore, the solution involving a step-up transformer at the output is favorable not only in terms of providing a neutral wire for the load, but also providing regulation at the rated output voltage. With the possibility of arranging the winding ratio of the transformer, the inverter can be operated at reduced DC bus voltage levels. So at the input stage, thyristor rectifier which draws distorted input current from the utility line or step-down type PWM rectifier which draws sinusoidal currents from utility and also regulates the DC bus voltage to a rated value and charge the UPS batteries can be employed.

An additional benefit of employing a transformer in the UPS is regarding paralleling. In order to increase the UPS power rating, either the UPS component ratings are increased or smaller UPS systems are paralleled. Increasing switch ratings usually is limited due to the device technology and can not go beyond several hundred amperes. Paralleling UPS systems increases the cost and complexity of the system. Instead, increasing the UPS power rating by using multi-winding transformer is easier and less costly. While using only one transformer secondary winding (per-phase), multiple primary windings could be utilized. Each primary winding set is fed from an inverter. When all inverters are operated at the same frequency simultaneously, power transfer from each unit to the secondary is nearly equal. The transformer leakage inductances help suppress the circulation currents and support balanced loading of each unit. Therefore, a natural balancing mechanism provides equal load sharing during parallel operation of various primary windings.

In the transformer based topology, the leakage inductance of the transformer can be used for filtering the ripple of the inverter voltages. Therefore, making the transformer leakage inductance sufficiently large, the external filter inductance can be eliminated. If not sufficient, an additional inductance can be integrated to the

same transformer steel lamination frame for lower cost and volume. This integrated magnetic solution has been favored in many commercial UPS systems.

Due to the large size and cost associated with the transformer based UPS; today at low power ratings the technology is loosing its edge to transformerless technologies [7]. However, at high power ratings and where galvanic isolation is required, the topology remains the prime choice. Presently, in the megawatt power range, the only static on-line UPS topology available in the market is this topology.

In the transformerless technologies a neutral current path must be provided. In order to provide a neutral terminal for the single-phase loads in low power applications, the common point of the output filter capacitors can be connected to the midpoint of the DC link (Figure 1.8). Thus, the size of the UPS can be decreased due to the absence of the transformer. In this topology owing to the fact that each leg acts as an independent half-bridge inverter, each output voltage can be controlled independently provided that the mid-point of the DC link is stable. If the current which is passing through the neutral wire is high, mid-point voltage of the DC link oscillates. Therefore, a large DC bus capacitor becomes necessary.

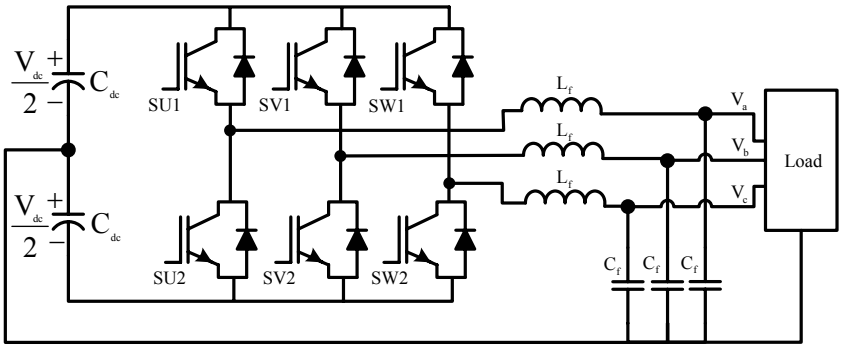

Figure 1.8 The three-phase four-wire transformerless UPS with midpoint connection to the DC bus bar capacitors.

The neutral point terminal can be provided from a fourth inverter leg, instead of the midpoint of the DC link capacitors. This provides neutral point connection by avoiding neutral wire current circulation through the DC bus capacitors. This inverter topology shown in Figure 1.9 is termed as “four-leg inverter.” Since the neutral point voltage is controlled with the fourth leg, zero sequence currents can be controlled and balanced output voltages can be achieved under all loading conditions [8].

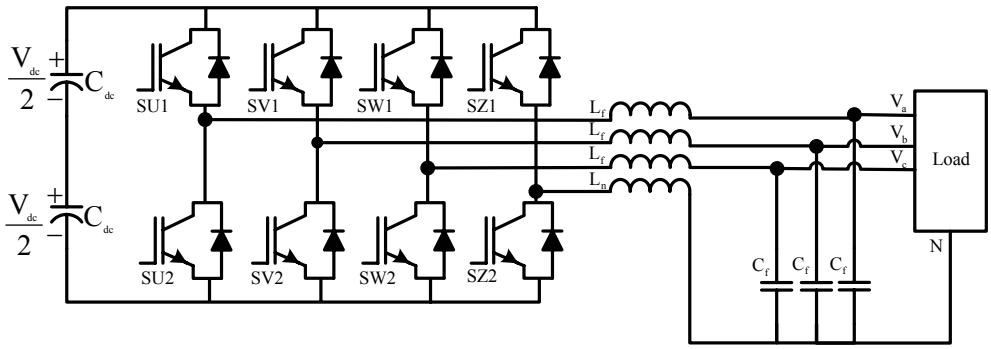

Figure 1.9 The three-phase four-wire transformerless UPS with four-leg inverter.

The transformerless type UPSs are preferable in low power applications due to high dynamic response, ease of maintenance, high energy efficiency and low cost. But in high power applications galvanic isolation, low switching stress, ability to be paralleled are more important than the merits of transformerless UPS listed above. This thesis focuses on the output voltage control of a UPS with Δ/Y connected transformer, under all loading conditions.

1.3.2 Control Methods Employed in On-line UPS Systems

An ideal UPS should provide ideal sinusoidal output voltage with fixed magnitude and frequency. The output voltage should have no harmonics or frequency variation. The ideal UPS should have zero output impedance during normal operation such that when the UPS is loaded, the output voltage should not be changed. Load currents with high crest factor should not distort the output voltage.

In practice, UPS systems deviate from the ideal UPS in terms of output voltage regulation. With a high performance output voltage controller, the practical UPS can approach an ideal UPS performance. However, high performance typically comes at increased controller complexity and increased cost. Therefore, the trade-off between the cost and performance is resolved by utilizing satisfactory but not expensive control methods.

Power is transferred to the load through the output LC filter of a UPS. The voltage drop on the output LC filter impedance deteriorates the voltage quality of the UPS. Thus, the output voltages of the UPS must be controlled in order to achieve regulated output voltages. In many applications, three-phase UPSs are utilized to feed both single-phase and three-phase loads. In such applications, currents drawn from the UPS are not balanced. Unbalanced load currents cause unbalanced output voltages unless the negative sequence and zero sequence components on the output voltage are eliminated. In today's world many of the critical loads utilize rectifiers at the input stage of their power supplies. Due to the switching behavior of the rectifier, input currents are nonlinear that is not sinusoidal. Harmonic content of nonlinear currents causes distortion on the output voltages of the UPS. Also, there are several additional reasons for the degradation of the three-phase UPS output voltage quality: nonlinearity of the PWM inverter (such as deadtime and device on-state voltage drops), nonlinearity of the isolation transformer (nonlinear/saturating magnetic characteristic), fluctuation in the DC bus voltage of the inverter, voltage drop on semiconductors in the rectifier and in the inverter stage.

The output voltage RMS value control method which is commonly used for UPSs in the market is illustrated in Figure 1.10. The RMS value of the output voltage is calculated by an RMS value calculator and the average value of the three-phase RMS voltages is controlled with a linear controller (a Proportional+Integral (PI) regulator). The output of the PI controller is the amplitude of the inverter voltage reference. A 50 Hz sinusoidal wave with unity magnitude is multiplied with the controller output to generate the PWM voltage reference for the inverter.

Although the technique is sufficient for balanced linear loads with slow dynamics, high quality output voltage can not be achieved for highly dynamic or nonlinear loading conditions. The control response is very slow because of the fact that RMS calculator produces output once per fundamental cycle. In order to partially improve bandwidth of the controller, a sliding window RMS calculator can be implemented. The controller performance for unbalanced or nonlinear loads is unsatisfactory. Because the RMS value of the output voltage does not include the knowledge of the imbalance and harmonic content. Therefore, the RMS value control method strongly relies on a large size output capacitor so that all the disturbances, the transients and harmonics are suppressed. The RMS value controller can also be implemented in the single-phase UPS systems. Although the method is simple and its implementation cost is low, the required filter size makes the control method unsatisfactory. As a result, this control method is obsolete and in the modern UPS systems superior control methods are employed.

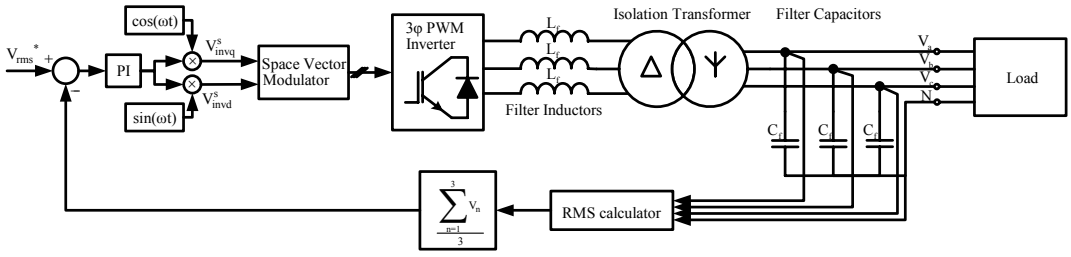

Figure 1.10 The output voltage RMS value control method for three-phase transformer based UPS systems.

In order to provide higher bandwidth output voltage control and reduce the sensitivity to load disturbance, dynamic feedback loops must be considered. Rather than the RMS value of the output voltage, the instantaneous value of the state variables should be utilized in the feedback path.

The output voltage of the single-phase UPS can be controlled by a single voltage feedback control loop (Figure 1.11). Since the controlled plant (LC filter and inverter) is a system with lagging property, the controller must include leading

property which is a derivative action. To reduce low frequency and DC offset errors, an integral control term may also be added. Hence, with proper gains, a proportional plus integral plus derivative (PID) controller structure eliminates the voltage errors with an excellent dynamic response. The output voltage decoupling term which is added to the inverter reference improves the controller command tracking performance. Despite the advantages listed above, derivative control is not preferred in real time application due to its high sensitivity to noise [2]. Any measurement error may cause the system to be unstable. Thus different control methods are proposed to control the output voltage of the UPS by avoiding derivative structure in the controller.

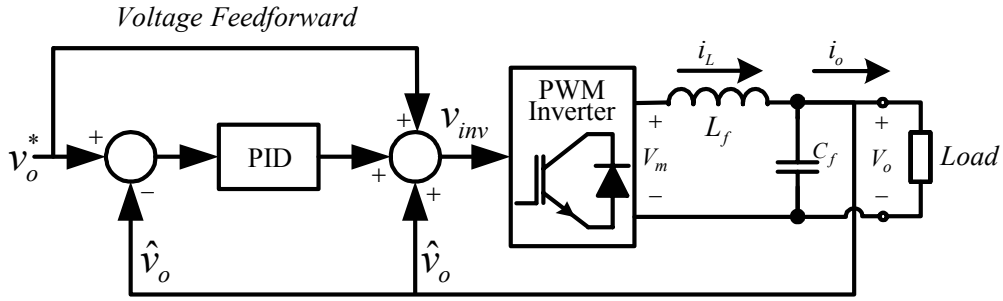

Figure 1.11 Single voltage loop control of the single-phase UPS via PID controller.

Cascade control structure (Figure 1.12) comprises two control loops with different bandwidths [9]. The inner one, which is faster, controls the inductor current and the slow outer control loop controls the UPS output voltage. The output voltage loop generates current reference for the inner loop. The control strategy is mainly based on the assumption that the output capacitor voltage does not change rapidly in a short period of time. This is valid if the capacitor of the UPS is sufficiently large. During this short period, the inductor current can be controlled with a faster current controller provided that the inductance value is small enough. That means before the output voltage changes significantly, the inductor current must catch the current reference. Thus two controllers can be decoupled from each other by choosing

suitable time constants for each controller that is to say; small time constant for the inner loop and bigger time constant for the outer loop. Usually the current control bandwidth is chosen as one fifth of the switching frequency and for the voltage controller one fifth of the current controller as well. Thus, voltage loop control bandwidth decreases significantly. Due to the limited performance of PI controller in controlling AC quantities, the controller can not eliminate steady-state output voltage errors. The bandwidth of the controller can further be increased by implementing additional terms to the controller at the expense of increase in cost [10]. Output voltage decoupling term given to the inverter reference increases the bandwidth of the current controller as it decouples the inductor current control loop from the capacitor voltage. Also if the load current is measured and added to the control structure as in the Figure 1.12, inverter supplies the load current directly. Thus the output voltage gets decoupled from the load current disturbance and the bandwidth increases. Instead of using inductor current, utilizing the capacitor current in the current feedback loop provides similar disturbance rejection as in the load current decoupling case.

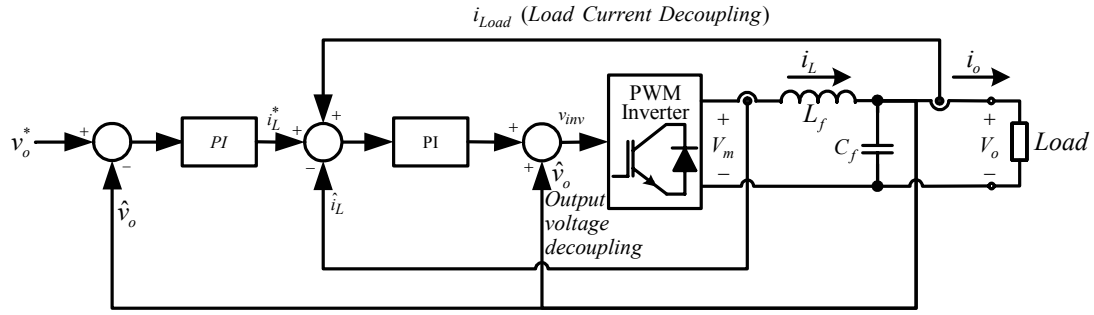

Figure 1.12 Cascade control structure of the single-phase UPS.

Instead of using single-loop voltage controller with PID structure (Figure 1.11), derivative control can also be achieved by utilizing the output capacitor current which is proportional to the output voltage derivative (Figure 1.13). In such a "multi-loop control structure" the capacitor current is multiplied by the active damping gain K_{ad} and subtracted from the inverter reference voltage. This method is also termed as

"active damping method" due to its damping effect on the closed-loop transfer function of the overall system [11]. However, adding a capacitor current sensor (a current transformer, CT) increases the cost and complexity of the control system. Thus, the application of this technique is limited in practice.

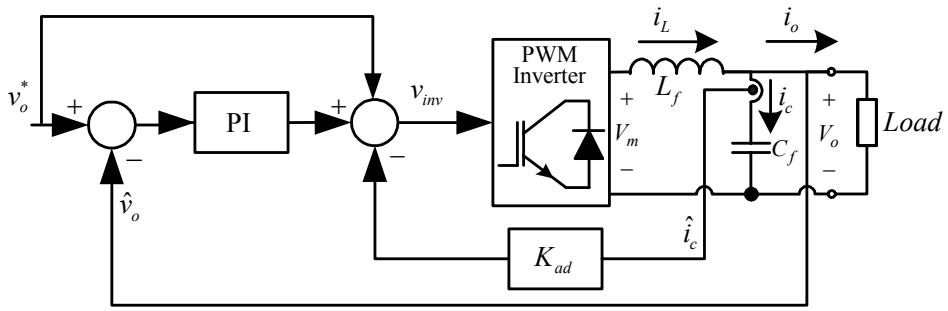

Figure 1.13 The single-phase UPS voltage loop control structure with capacitor current feedback.

Deadbeat control is a model based high bandwidth control technique [12]. As its name implies, theoretically, the deadbeat controller eliminates output voltage error in one PWM cycle. With the precise knowledge of the inverter and filter parameters, controller calculates the correct inverter reference voltage for the next controller output cycle which eliminates the output voltage error. But measurement delays, computational delays, and measurement errors in the feedback strongly degrade the control performance. Although research on the computational delay compensation has succeeded [13] to overcome this problem, measurement delay and measurement quality are still problems. Predictive methods can compensate for these delays, but both deadbeat and predictive control techniques are strongly dependent on the parameters of the UPS for eliminating steady-state error [14]. These methods can hardly be implemented to the transformer based UPS due to the modeling complexity and uncertainty in the parameters of isolation transformer.

In high power applications, the switching losses become significant at the inverter stage of the UPS. Thus high switching frequencies can not be achieved. Under this condition the bandwidth of the voltage controller can not be made sufficient to eliminate the low order voltage harmonics (those close to the filter resonant frequency) which stem from the nonlinear loads. Output voltage harmonic distortion can be reduced by reducing the output impedance ($\sqrt{\frac{L}{C}}$) of the output LC filter. But overrating of the filter components is not a favorable solution due to its effect on increasing the cost and degrading other characteristics of the UPS (increasing the no-load current, decreasing the efficiency, increasing the size, etc.). Therefore, methods that can perform well with low switching frequencies are required. For this purpose, controllers that can manipulate the significant control cycle delay properly, and allow for high control bandwidth and high steady-state performance are required. In the literature there exist three such control methods: synchronous reference frame control, resonant filter type control, and repetitive control. It is easier to apply these methods in the vector coordinates to the transformer based three-phase UPS. Thus, the vector transformation discussion will precede the discussion of these controllers.

In the vector control approach, the three-phase AC quantities are transformed to a complex vector with the complex number transformation given in (1.8). In the transformation x_a, x_b, x_c represent the three-phase AC quantities and α is the conventional 120° phase shift operator which is $e^{j2\pi/3}$ with j being unit imaginary complex number. The resultant vector rotates in a complex plane which is termed as "stationary reference frame." Due to the fact that real (quadrature) and imaginary (direct) components of the vector are 90° phase shifted with respect to each other, each component is independent. So the components of the stationary reference frame vector can independently be controlled. Consequently this transformation transforms the three-phase UPS system into two independent single-phase UPS systems (here, the zero sequence component is not discussed as it is not controllable by the three-leg inverter). All of the AC control methods used in single-phase UPS control can be implemented to the three-phase UPS in stationary frame. In the stationary frame, the output voltage vector follows a perfect circular route if the output voltages are

balanced and nondistorted. Harmonics and imbalance components are seen as deviation from the perfect circle.

$$\vec{X} = \frac{2}{3}(x_a + \alpha\, x_b + \alpha^2 x_c) \tag{1.8}$$

The complex vector of the balanced and nondistorted three-phase quantities can be expressed as (1.9) where X_m is the magnitude of the vector, ω is the angular frequency, and t is time.

$$\vec{X} = X_m.e^{j\omega t} \tag{1.9}$$

If the vector is multiplied by a unity amplitude vector rotating in the opposite direction to the output voltage vector, the exponential angular frequency terms are cancelled therefore the resultant vector becomes a vector with a constant value (not varying in time). By this mathematical transformation, the complex vector is synchronized to the rotating complex frame. This rotating complex frame is termed as "synchronous reference frame" (SRF). Since the real and imaginary components of the SRF vector are DC values, they can be controlled with a PI controller which provides infinite gain to DC error signals and achieves zero steady-state error [15]. Synchronous reference frame control (SRFC) can be used for the three-phase transformer UPS systems. This technique can be implemented with an inner current loop to improve dynamic response and stability of the system. In practical applications, usually voltage loop control is implemented. The basic control structure of the SRFC fundamental frequency controller is shown in Figure 1.14. The fundamental component output voltage is regulated by the synchronous reference frame controller rotating at the fundamental frequency. However, harmonics can not be rejected with this scheme. If harmonics exist on the output voltage, in the

synchronous reference frame they will appear as rotating vectors. For example, the 5th and 7th harmonic voltage vectors will rotate at a frequency equal to six times the fundamental frequency. These harmonic voltage vectors will rotate in the stationary reference frame at five and seven times the fundamental frequency, but in opposite directions. While the fifth harmonic rotates opposite to the fundamental frequency voltage vector, the 7th harmonic rotates in the same direction. In order to suppress these harmonics, each harmonic can be transformed to a reference frame of its own frequency and in opposite direction to its own rotation direction and then appear as a DC voltage vector. Then, a PI controller may be used to regulate the associated harmonic voltage at zero steady-state value. However, this approach is involved as significant number of computations is required and also the phase delay of the system (PWM, measurement, noise filter, computation, LC filter delays) is significant that limits the performance of the system. Furthermore, the method requires decoupling of the synchronous frame direct and quadrature axis components which couple due to the vector transformation.

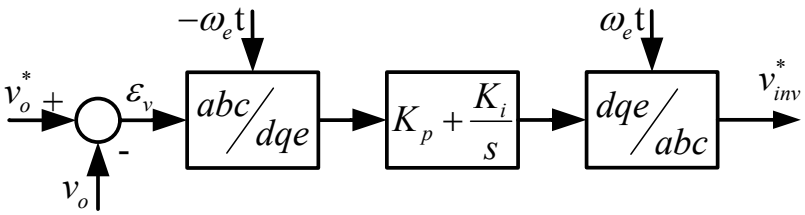

Figure 1.14 Synchronous reference frame control system basic structure.

The synchronous frame control method is complex and simplifications are necessary. For this purpose, the transform of the controller from synchronous to stationary frame rather than the signals from stationary to synchronous frame has been considered and lead to a feasible solution, the resonant filter controller. The control structure given in Figure 1.14 can be transformed to the stationary frame *qs-ds* coordinates. The resultant control matrix from the output voltage error (ε_{qds}) to

inverter voltage reference (v_{invqds}) is given in (1.10). As seen from the matrix, the diagonal terms consist of proportional gain and a resonant term which has infinite gain at the selected frequency which is the fundamental frequency in this case. The off-diagonal terms are also resonant terms but cause cross-coupling between *qs* and *ds* channels. It has been found that the off-diagonal terms are not beneficial to the controller performance and thus they are neglected. As a result, the *qs* and *ds* controllers are no more coupled and employing the control structure of (1.11), the implementation becomes easy. For each axis controller, the resonant filter provides infinite gain and zero phase shift at the selected frequency [16]. In this controller there is no need to identify and separately control the positive and negative sequence components of the output voltages and one controller controls both naturally [17]. For each frequency a dedicated controller is required for each axis. By constructing *N* parallel resonant controllers for *N* dominant harmonics, as given in Figure 1.15, high quality output voltages can be obtained. However the implementation of this controller is still problematic due to the high computational requirement in the construction of *N* different harmonic controllers. With a finite word length microprocessor, implementation is problematic when the filter selectivity is set high and the controller structure should be modified at the expense of reduction in the controller gain at selected frequency. In the literature there exist several methods for handling the finite word length problem [17], [18], [19], [20].

$$\begin{bmatrix} v_{invqs}(s) \\ v_{invds}(s) \end{bmatrix} = \begin{bmatrix} (K_p + \dfrac{K_i \cdot s}{s^2+\omega^2}) & -\dfrac{K_i \cdot \omega}{s^2+\omega^2} \\ \dfrac{K_i \cdot \omega}{s^2+\omega^2} & (K_p + \dfrac{K_i \cdot s}{s^2+\omega^2}) \end{bmatrix} \begin{bmatrix} \varepsilon_{vqs}(s) \\ \varepsilon_{vds}(s) \end{bmatrix} \tag{1.10}$$

$$\begin{bmatrix} v_{invqs}(s) \\ v_{invds}(s) \end{bmatrix} = \begin{bmatrix} (K_p + \dfrac{K_i \cdot s}{s^2+\omega^2}) & 0 \\ 0 & (K_p + \dfrac{K_i \cdot s}{s^2+\omega^2}) \end{bmatrix} \begin{bmatrix} \varepsilon_{vqs}(s) \\ \varepsilon_{vds}(s) \end{bmatrix} \tag{1.11}$$

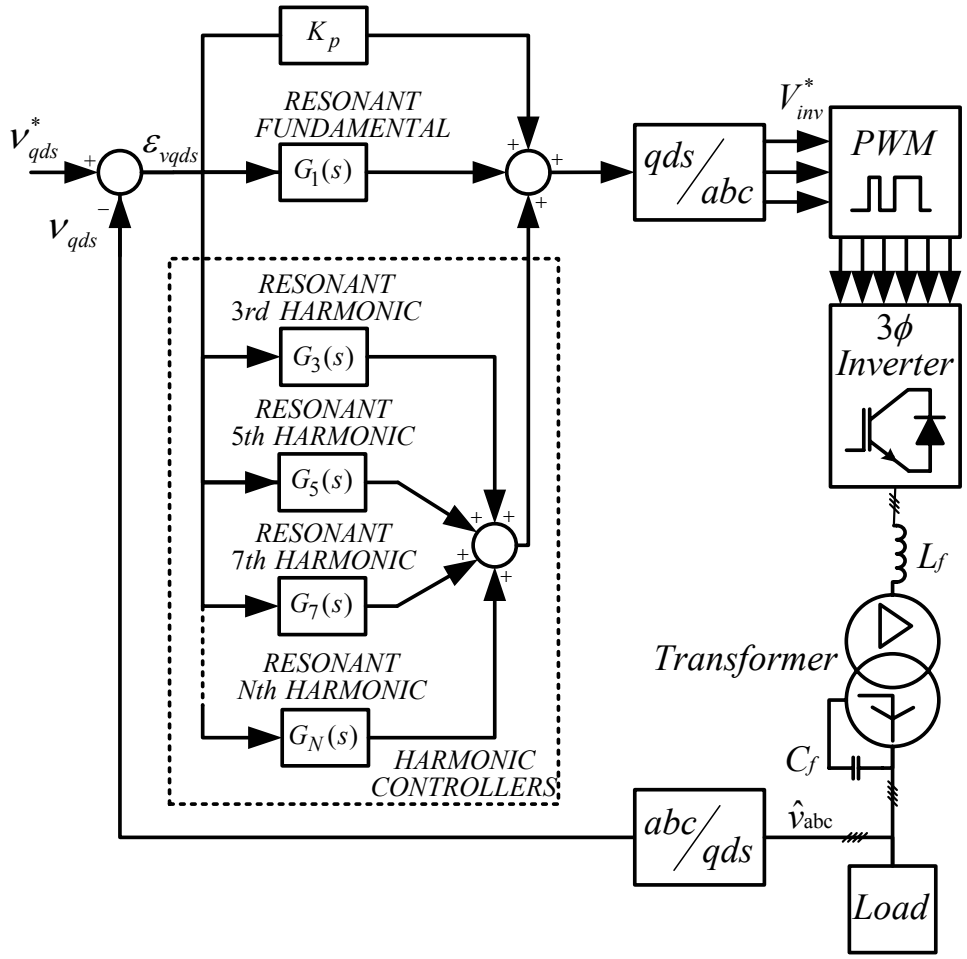

Figure 1.15 Resonant controller structure based UPS control.

The repetitive control method is a method with implementation advantages over the SRFC and resonant filter techniques and has found some applications specifically in either low cost or low switching frequency applications. The repetitive controller mainly learns the periodic output voltage distortion and compensates for the distortion such that the output voltage has high quality waveform even under highly nonlinear loading operating conditions.

In the repetitive controller structure, the output voltage of the UPS and reference voltage are divided into a number of discrete points (commonly ratio of fundamental period to switching period). Each point of the output voltage over the fundamental cycle is controlled via an independent integral controller dedicated to this point. The

control mechanism is a fundamental period based integrator [21]. More clearly one integrator integrates the output voltage error once per fundamental period. Each integrator operates in sequence such that while one integrator is operating others do nothing. Any voltage deviation of output voltage from the voltage reference at any point of the fundamental cycle is kept in the memory of the controller and a correcting inverter voltage is generated for this point in the next fundamental period. In several fundamental cycles the distortion is eliminated. Usually a high bandwidth voltage controller is added to improve the loading transient response of the controller.

Various repetitive control implementation schemes have been reported in the literature. Shown in Figure 1.16., the repetitive control method proposed in [21] is implemented in vector coordinates and brings the advantage of easy anti-windup implementation. The method involves PI controllers, one for each point of the repetitive controller. The method implements a finite impulse response (FIR) filter on the voltage feedback to prevent the high frequency signals from entering the repetitive controller and creating controller output signal drift which could lead to system failure. The paper does not provide detail on the controller design, however demonstrates the performance of the controller via experimental results. The control response of the method is shown to be about ten fundamental cycles which is considerably slow.

The method proposed in [22] involves a single-phase UPS with a two layer control structure which involves repetitive controller and a tracking controller. The repetitive controller operating at outer layer is responsible for the elimination of periodic errors on the output voltage. The function of the tracking controller operating at the inner layer is to improve transient response of UPS. Here, the controller bandwidth is enhanced at the cost of high controller complexity.

The method proposed in [23] involves repetitive control of a single-phase UPS, investigates the filtering structures utilized in the controller in detail and shows the influence of various filter structures on the output performance. Single voltage loop control is employed (no measurements are utilized other than the output voltage). A

notch filter is proposed for the cancellation of resonant peak of LC filter of the UPS such that resonances due to disturbances are suppressed and the output voltage quality does not degrade under nonlinear load operating conditions. It is also shown that the method exhibits satisfactory performance over a reasonable range of LC filter parameter variations, thus shows robustness to parameter variations.

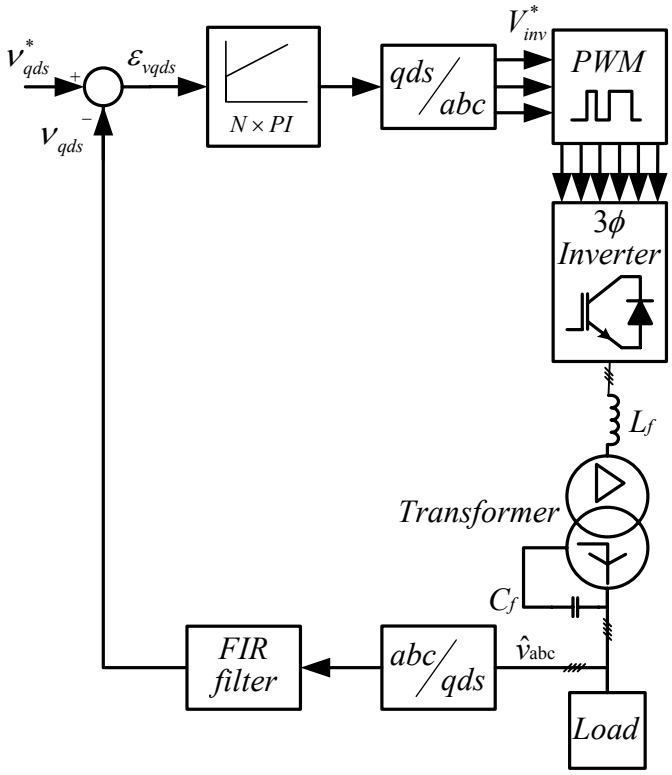

Figure 1. 16 Vector coordinate repetitive controller proposed in [22].

In summary, in terms of control behavior, the transformer based three-phase UPS has a complex structure that makes it difficult to understand, model, and control. With the topology being suitable for high power UPS systems where the switching frequency is low, the bandwidth achievable is limited by the switching frequency substantially. Thus, performance under dynamic conditions (loading transients) and during steady-state for nonlinear load operating conditions is quite limited when using conventional control methods.

The recently developed repetitive control methods, specifically the vector control method in [21] and scalar method in [23] are good candidates for controlling the transformer based three-phase UPS with low switching frequency for they perform satisfactorily under steady-state. These two methods, in a sense complement each other as [21] provides the vector approach with no details on controller design and [23] provides the detailed controller design (specifically the filtering structures involved in the controller and their influence on the UPS performance). The work in this thesis will extend on the work on these two papers and provide further guidance towards successfully applying the repetitive control method to transformer based three-phase UPS systems.

Under the scope of this thesis, design and implementation of the repetitive control is the main topic due to its ability to eliminate any imbalance and/or harmonic distortion without requirement of exact UPS parameters and model.

1.4 Scope and Organization of the Thesis

In this thesis, output voltage control of a UPS with a Δ/Y connected isolation transformer is investigated. Although there exist many papers on the output voltage control of UPS, minority of them involve the transformer based UPS. Due to the difficulty in modeling the Δ/Y connected transformer and uncertainty in the parameters of transformer, model based control algorithms which are the methods discussed in most papers, are not directly applicable to the transformer based UPS. Thus, instead of model based control structures, self converging feedback control structures are investigated. Among various control techniques, synchronous reference frame control (SRFC), resonant filter type control (RFC), and repetitive control (RC) are found suitable for application to the transformer UPS. However, due to the complexity of the first two, only the repetitive control method is considered suitable for the low cost (in terms of control, measurement etc. cost) and/or high power UPS systems. Therefore, the repetitive control method and its application to the three-phase transformer based UPS system will be the main focus of this thesis.

The aim of the thesis is to establish in depth background on the repetitive control method and apply the knowledge to systematically design the output voltage controller of the three-phase transformer based UPS. With the design issues well understood and a proper design completed, the performance of such a system will be investigated in detail to evaluate the feasibility of this technology. Therefore, the main contribution of this thesis is towards high performance repetitive controller design and detailed performance investigation of a three-phase transformer based UPS system.

The organization of the thesis is as follows.

In Chapter 2, the theory of repetitive control method and its application to the three-phase transformer based UPS are discussed in depth. While discussing the elements of the repetitive controller based system, the design rules and guidelines for each element will be provided and exemplified with a numerical design to be utilized in later stages for the purpose of performance verification.

Chapter 3 investigates the detailed performance of the repetitive controller based UPS under various challenging operating conditions by means of computer simulations. In the simulations the inverter PWM cycle average model is utilized. First, the performance issues of open-loop voltage controlled UPS system are demonstrated for various operating conditions. Then, implementing the control structure discussed in Chapter 2, the closed-loop controlled UPS performance is studied in detail and compared to open-loop operating performance. The parameters of the controller are tuned at operation under nonlinear full-load which is the most challenging load type. Following the completion of the repetitive controller design stage, the system performance is evaluated for various operating conditions. First the nonlinear balanced load operating performance is investigated in detail. Then the nonlinear load under unbalanced operating condition is considered. Finally the dynamic performance of the controller is tested by loading the UPS from no-load to balanced linear resistive full-load.

Chapter 4 experimentally verifies the theory and computer simulation results provided in the preceding two chapters. The design and implementation of a laboratory prototype system is discussed. The controller implementation details and issues are given. Then the experimental results are given and discussed in detail.

Chapter 5 provides concluding remarks, summarizes the main attributes of the method and points out towards future work.

Overall, this thesis investigates the analysis, design, implementation, and performance evaluation of the repetitive control method as applied to the isolation transformer based three-phase UPS system. The work is to help the design and implementation engineer understand the repetitive control method, its controller design principle, and application to three-phase UPS systems.

CHAPTER 2

OUTPUT VOLTAGE CONTROL OF THE ISOLATION TRANSFORMER BASED THREE-PHASE UPS BY MEANS OF REPETITIVE CONTROL

2.1 Introduction

Most industrial and electronic equipment involve rectifiers that convert the AC power line to DC voltage. Unless a passive or an active filter circuit is utilized at the input of the equipment, the currents drawn by these rectifiers include high harmonic content. If such equipment is fed from a UPS, the output voltages of the UPS get highly distorted since the UPS output current with high harmonic content flows through the UPS output impedance consisting of an LC filter. Thus, the rectifier load and other equipment fed from the same UPS, experience power quality problems due to the distorted UPS output voltages. The output voltage decreases, the current increases, and the efficiency decreases. Sensitive loads may experience contingency or poor power quality leading to significant cost and downtime. Therefore, no distortion on the UPS output voltage is desired due to the above mentioned reasons.

There are various control methods that reduce the UPS output voltage distortion. The output voltage waveform quality can be improved by increasing the output voltage controller bandwidth. However, high bandwidth control methods require measurement of the system variables with high accuracy and minimum time delay, rapid and accurate calculation of the control signal, and application of the manipulation signal correctly. In order to apply control methods such as deadbeat control, output voltage measurement alone is not sufficient. In addition, measurement of filter inductor currents, filter capacitor currents, and/or the output currents may be required. Furthermore, high switching and sampling frequency operation requires a

high speed signal processor. As result, the cost and structural complexity increase. Therefore, in low power and low cost applications, high bandwidth UPS controllers may be prohibitive [22]. At medium and high power UPS applications also the utilization of such control algorithms can be prohibitive. In such applications which involve high current levels, the inverter switching losses are considerably high and increase with the switching frequency. Therefore, the switching frequency of the semiconductor switches in the inverter is confined by the total loss in the system due to efficiency considerations. Operation at low switching frequency limits the update rate of the controller, increases the system time delay, and results in low control bandwidth [21]. Therefore, regardless the power ratings, in most UPS applications high bandwidth control methods are not applicable. On the other hand, considerable distortion on the UPS output voltage due to loads with high crest factor such as diode or thyristor rectifiers can not be accepted. Therefore, for the low switching frequency and/or low performance signal processor (where the control algorithm is realized) applications, control methods that provide high quality steady-state UPS output voltages under nonlinear load are required. Considering that the harmonic currents caused by nonlinear loads are periodic large signal disturbances, the UPS output voltage control problem can be cured by utilizing the repetitive control method.

2.2 The Basic Principle Of Repetitive Control

Since the UPS output voltage reference value and also the output voltage are periodic, the disturbance effects of all types of loads on the output voltages at steady-state are also periodic. Considering the above discussed limitations, one method to obtain high quality UPS output voltages is to employ the repetitive control method. The repetitive controller learns the influence of the load current on the output voltage by observing the behavior of the output voltage over a fundamental period and then corrects the output voltage by shaping the inverter reference voltage in the following period and so on [24]. Therefore, high quality output voltages can be obtained by measuring the output voltages only. The controller structure, which is built based on the periodicity of the system, can not be expected to respond the start-up and loading dynamics in a time interval shorter than one fundamental period. However, in 5-10 fundamental periods high quality output voltages can be obtained [21]. Furthermore,

the dynamic performance of the system can be improved by combining the repetitive control method with high bandwidth control structures [22].

In the repetitive control method, the inverter reference voltage and the sampled output voltage are divided into N sampling points over one fundamental period T with N being the ratio of the fundamental period to the sampling period T_s. For example, in Figure 2.1 the reference voltage v_o^* and output voltage v_o are defined by 20 sampling points (N=20). In this figure, the output voltage reference is given on top and the distorted UPS output voltage is given at the bottom diagram. As can be observed in this figure, each point on the reference and output voltage repeats itself at every fundamental period. This case is explained mathematically in (2.1). The reference voltage value is the same at the time instants $(k\text{-}N)T_s$, $k\ T_s$, and $(k+N)\ T_s$ as shown in Figure 2.1. Similarly the steady-state output voltage is periodic and at the time instants $(k\text{-}N)T_s$, kT_s, and $(k+N)T_s$ its value is the same. If the reference voltage signal is defined with one point for each fundamental period, it becomes a DC signal. Similarly, if each point of the output voltage in a period is defined separately, the output voltage and the output voltage error at each point become DC quantities. By employing this approach, if an integral controller is utilized for each point, the output voltages can be controlled with zero steady-state error. In this integral controller, the error voltages are summed with one fundamental period time intervals. This controller is called as "repetitive control" since it annihilates the error on periodic signals. Figure 2.2 illustrates the behavior of the controller for one point of the fundamental period. In this figure, the reference signal is given on top and the output voltage is shown at the bottom of the diagram. Both signals in this figure are defined by 20 points over a fundamental period (N=20). One of the defined 20 points of the reference signal is shown with a point symbol (●) and this quantity does not change in time. Similarly, one of the defined 20 points of the output voltage is shown with a triangle symbol (▲). The distorted output voltage signal of the first few periods is corrected by the repetitive controller over the following cycles. As can be observed in Figure 2, the repetitive controller perceives the output voltage distortion as the deviation of each discrete output voltage value from its defined reference value. Each

distorted point of the output voltage is corrected by a dedicated integral controller and high quality output voltages can be obtained.

$$v_o^*(k-N) = v_o^*(k) = v_o^*(k+N) \quad , \quad N = \frac{T}{T_s} \tag{2.1}$$

The discrete time expression of the standard integral controller is given in (2.2). If an error (e) exists on the controlled signal, according to the sign of the error positive or negative terms are added to the controller output (y). When the error becomes zero, the integrator output is fixed to a certain value. In this equation, K_i represents the integral gain and T_s is the sampling period.

$$y[k] = y[k-1] + K_i \times T_s \times e[k-1] \tag{2.2}$$

By employing the integral control structure given in (2.2) once per fundamental period for each point, the repetitive controller structure which is given in (2.3) is obtained. The output of the controller is produced by summing the error signal of the previous fundamental period with the controller output of the previous fundamental period. In the formula K_{rc} is the repetitive controller gain and it is a dimensionless quantity.

$$y[k] = y[k-N] + K_{rc} \times e[k-N] \tag{2.3}$$

By transforming the repetitive controller discrete time equation (2.3) to the z-domain, the transfer function given in (2.4) is obtained. In the equation *Y(z)* is the output of the repetitive controller and *E(z)* is the error signal in the z domain. The block diagram representation of the repetitive controller structure which is derived from the transfer function (2.4) is given in Figure 2.3 [24].

$$G_{rc}(z) = \frac{Y(z)}{E(z)} = \frac{K_{rc} \cdot z^{-N}}{1 - z^{-N}} \tag{2.4}$$

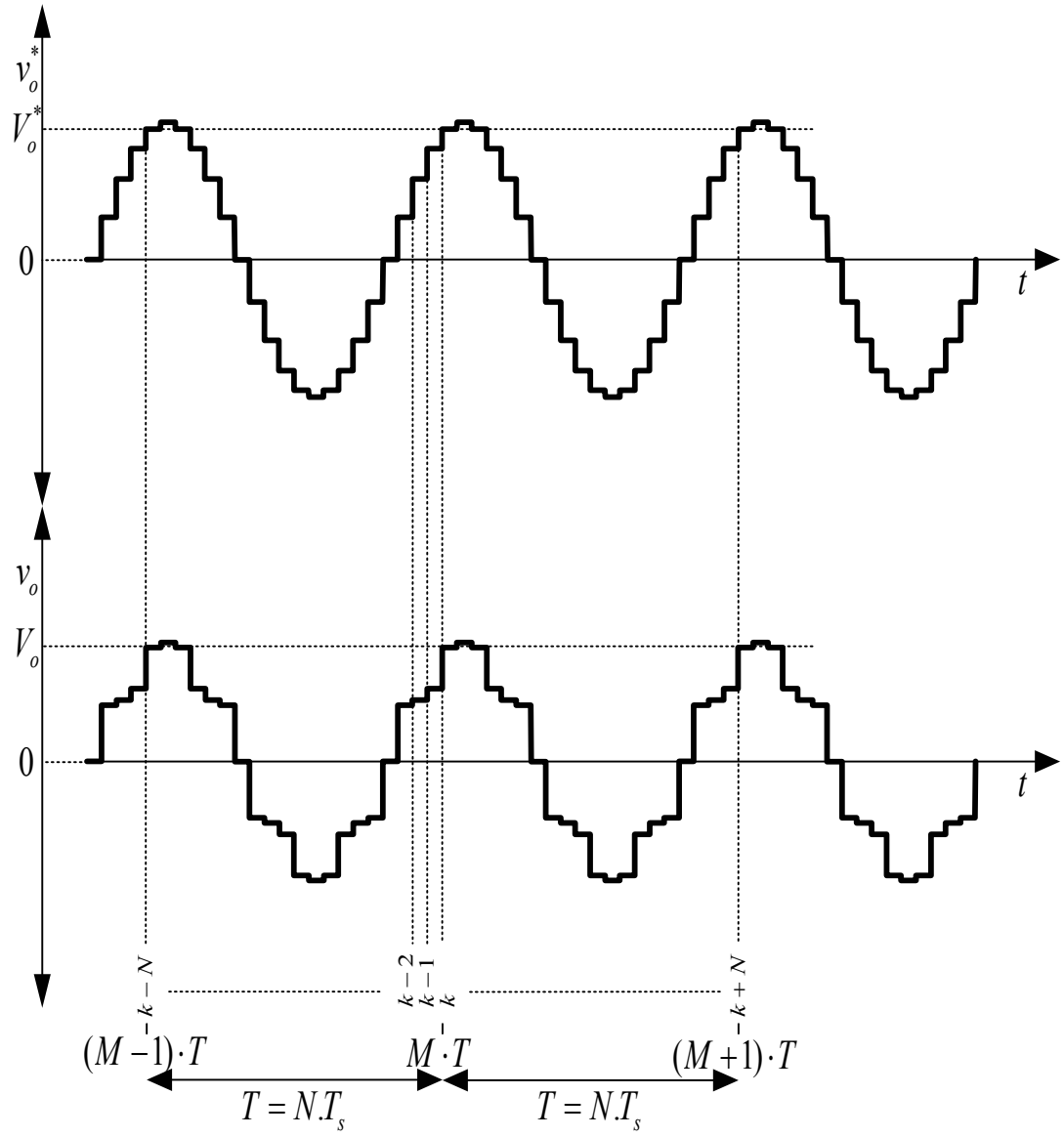

Figure 2.1 Periodic reference voltage (v_o*) and distorted output voltage (v_o).

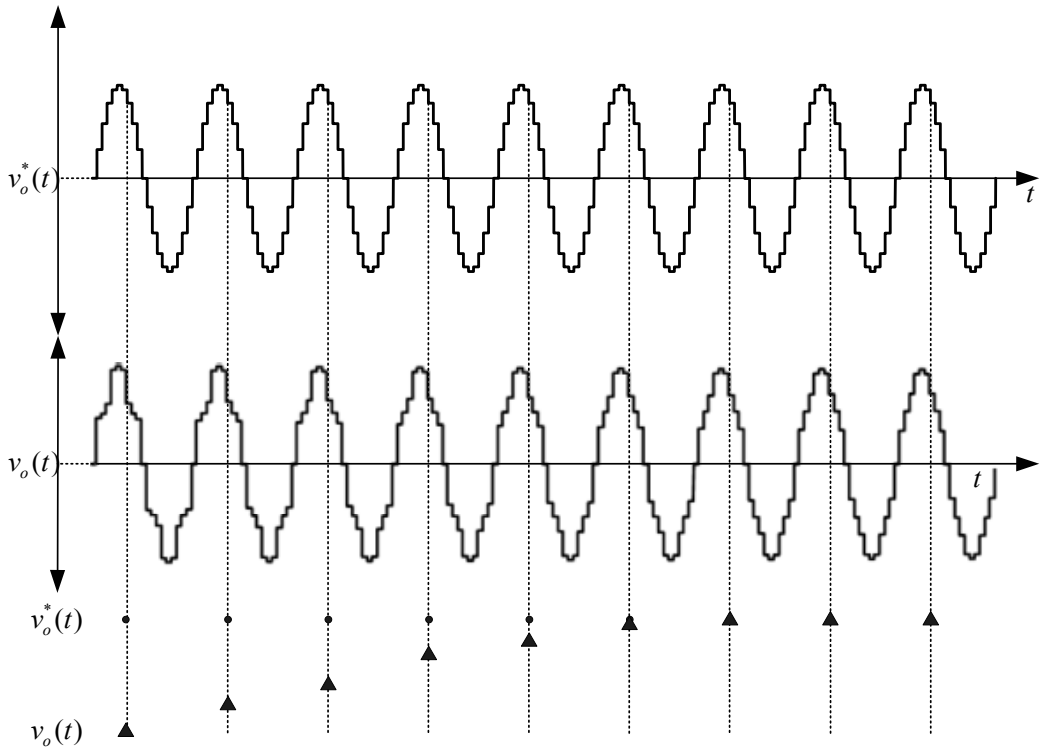

Figure 2.2 The response of the repetitive controller for one point of reference.

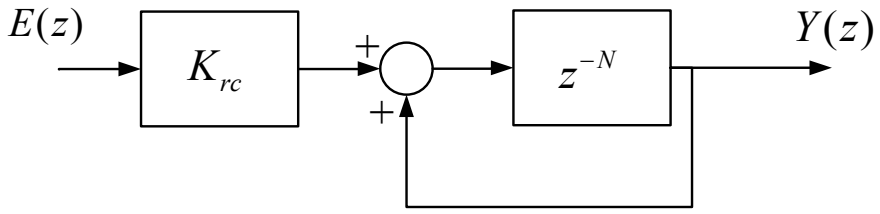

Figure 2.3 Repetitive controller basic block diagram.

To find the transfer function of the repetitive controller in the Laplace domain (*s*-domain), $e^{j\omega Ts}$ is substituted for '*z*' in equation (2.4) and the resulting transfer function in *s* domain is given in (2.5). By utilizing the Euler formula and expanding (2.5), equation (2.6) is obtained. In this equation, the $\cos(2\pi f \cdot N \cdot T_s)$ term takes the value of one and the $\sin(2\pi f \cdot N \cdot T_s)$ term takes the value of zero when the $f \cdot N \cdot T_s$ is an

integer. For such a case, the denominator of the transfer function becomes zero and the controller has infinite gain and zero phase shift. Since the reference signals are DC, the reference signal frequency is zero. Thus, the controller gain at zero frequency is infinity. This is a natural consequence of employing the integral control structure for regulating DC signals. If the error signal has fundamental frequency component and/or harmonics components which are multiples of fundamental frequency component, $f \cdot N \cdot T_s$ becomes an integer. And for such cases also infinite gain is obtained. Thus, the controller gain is infinite for DC, fundamental frequency and harmonic frequency error signals. In Figure 2.4 gain and phase characteristics of the controller are given. As seen in the figure, gain of the controller goes to infinity for each harmonic frequency. The phase characteristic reveals that the phase of the controller crosses 0˚ at the harmonic frequencies. Therefore, the output voltage error of the repetitive controller converges to zero at steady-state. However the number of harmonics to be controlled is specified by the number of sampled points in the fundamental period (N). With N sampling points taken over the fundamental period the maximum controllable harmonic is at frequency of $N\ f_e/2$ where f_e is the fundamental frequency of the output voltage. At higher frequencies controller can not respond to the harmonics. Therefore, the application constraints define the performance of the controller. In addition to the sampling frequency parameter N, the measurement, calculation, and PWM delays further limit the performance of the controller. Furthermore, the phase and magnitude characteristics of the LC filter of the UPS affect and further limit the output voltage quality. In the next section, these topics will be discussed in detail and the repetitive controller design procedure for the three-phase transformer based UPS output voltage control application will be determined.

$$G_{rc}(s) = \frac{K_{rc} e^{-j\omega T_s N}}{1 - e^{-j\omega T_s N}} \tag{2.5}$$

$$G_{rc}(s) = \frac{K_{rc} \cdot \cos(2\pi f \cdot T_s \cdot N) - j \cdot K_{rc} \cdot \sin(2\pi f \cdot T_s \cdot N)}{1 - \cos(2\pi f \cdot T_s \cdot N) + j \sin(2\pi f \cdot T_s \cdot N)} \tag{2.6}$$

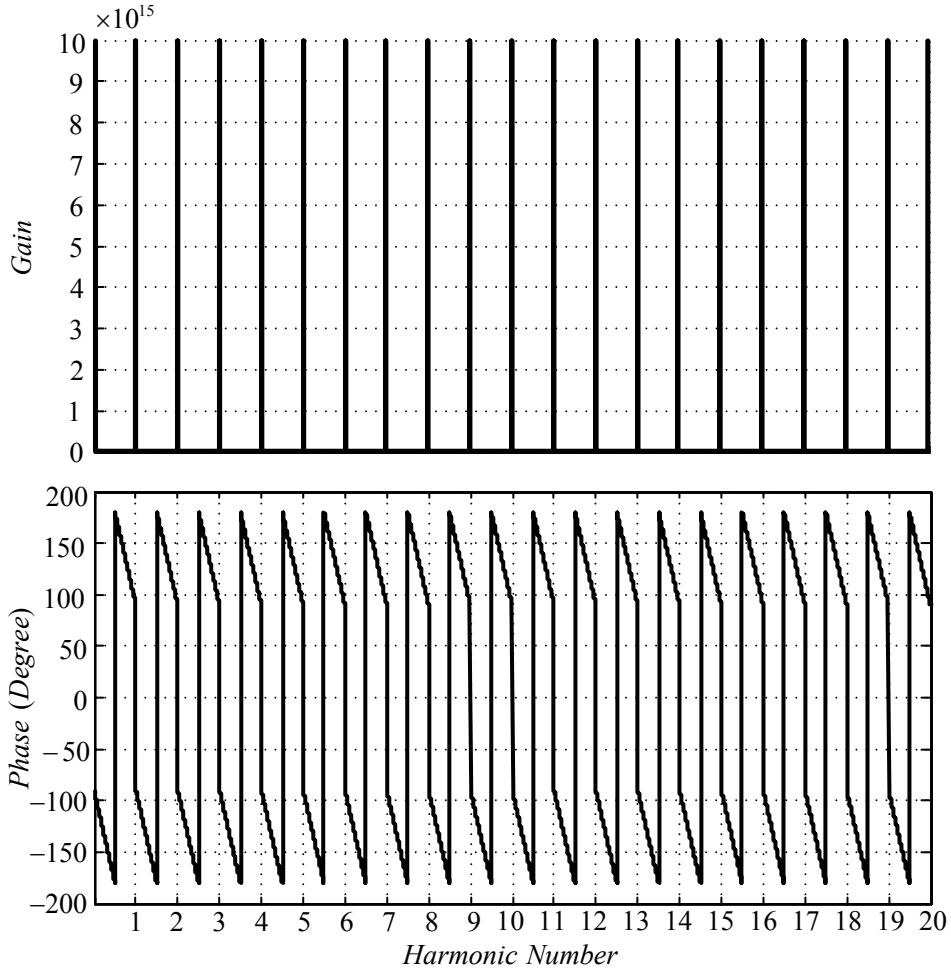

Figure 2.4 Repetitive controller gain and phase characteristics (N=40).

2.3 Application Of The Repetitive Control Method To UPS Systems

In order to apply the repetitive control method to a UPS system successfully, the system behavior of the UPS should be taken into account during the design stage. For this purpose, the characteristics of the inverter, transformer, LC filter, digital signal processor (DSP), and measurement circuits will be investigated and model of the UPS system which will be utilized in the computer simulations and experiments will be obtained by using a given set of parameters of a UPS system. Following, the vector approach which will be used in the repetitive control of the UPS output voltages will be reviewed and the impact of unbalanced and/or nonlinear loads on the output voltage vector and waveform quality will be emphasized. Finally, the

controller components involved in the repetitive control system for the UPS application and the design procedure for these components will be discussed.

2.3.1 Properties of The UPS as The Controlled Plant

The system diagram of the isolation transformer based three-phase UPS is given in Figure 2.5. The components of this system are the measurement and scaling circuits, the digital signal processor, the inverter, the isolation transformer and the LC output filter. From here on, the discussion will be conducted by using a numerical example involving the typical parameters of a 5 kVA three-phase UPS shown in Table 2.1. Throughout this discussion the magnetization inductance of the transformer will be assumed infinity and the leakage inductance will be assumed zero (implying an ideal transformer) in order to simplify the investigations. The practically non-negligible leakage inductance of the transformer shall be included in the inductor of the LC output filter for the purpose of maintaining accuracy in the model involved.

During the control process, feedback variables are taken to the analog to digital converter (ADC) of the digital signal processor with a measurement delay and finite measurement precision. Sampled output voltages are passed through the controller and inverter voltage references for each leg are synthesized by the controller. The inverter voltage reference is transformed to the gate pulses of the IGBTs via a pulse width modulation (PWM) method. In the case that the measurement signals are updated once per PWM cycle, there exists a delay which lasts one PWM switching period between the sampling instant of feedback variables and generation (application) of gate pulses. The PWM pulses provide the same volt×second multiplication (average voltage) as the inverter reference voltage. Thus, when the inverter output voltage is averaged in one switching period, the inverter voltage reference is obtained. When the switching frequency components are filtered, the inverter behaves as an ideal voltage source and preserves this property inside the inverter voltage linearity region. Since the DC bus is limited, saturation occurs if the inverter voltage reference exceeds the carrier wave limits and input-output voltage linearity is lost. By considering the application delay of the PWM pulses, in the

linear region the inverter can be modeled as an ideal voltage amplifier with unity gain which applies the demanded voltage waveform to the LC filter system with a half PWM cycle delay. In the following, the components of the UPS system will be discussed in detail.

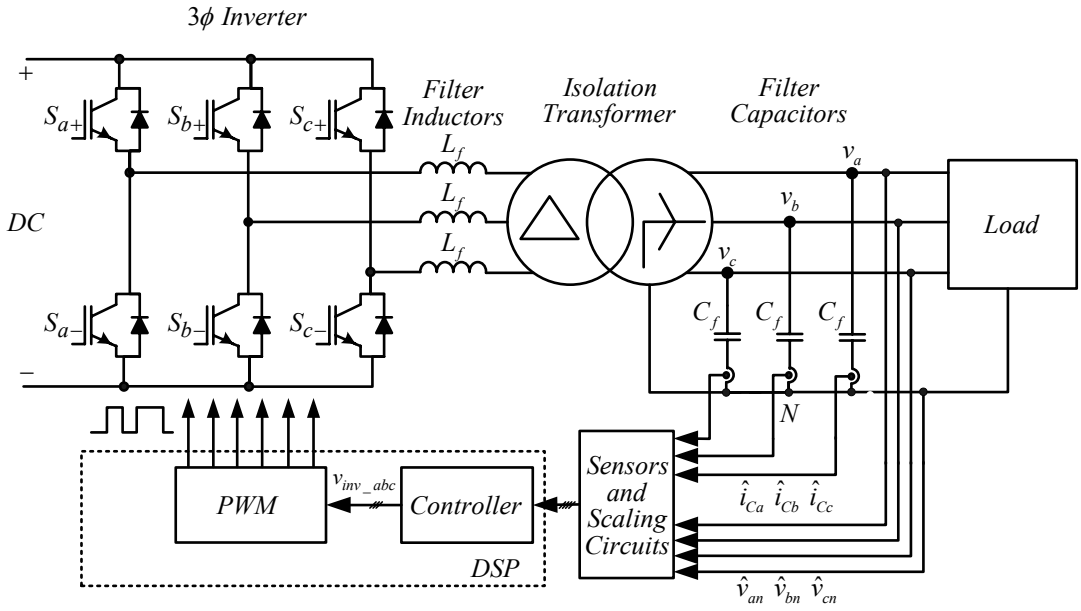

Figure 2.5 Three-phase transformer based UPS and controller system diagram.

Table 2.1 System parameters for the design of repetitive controller

Filter inductor	L	2.25 mH
Inductor equivalent series resistor	r_L	2 Ω
Filter capacitor	C	20 μF
Capacitor equivalent series resistor	r_C	0.2 Ω
Switching frequency	f_{SW}	20 kHz
Sampling frequency	f_S	10 kHz
Measurement delay	t_M	90 μs

2.3.1.1 DSP and Measurement Circuits

Through the process of obtaining the output voltage errors and utilizing them to generate the compensation signals, the output voltages (and if necessary other variables such as capacitor currents) are transferred to the DSP by means of ADC units with a finite measurement delay and resolution. Although measurement circuits have a nonlinear phase characteristic at high frequencies, for the frequency range where the repetitive controller is effective (for the given parameters of Table 2.1, this range is less than 1 kHz), the measurement delay can be approximated as a fixed time delay. Thus, the model of the transducers is a first order delay system with a given fixed time constant. For the UPS defined in Table 2.1, the total measurement delay of the measurement components, circuits and associated noise filters amounts to approximately 90 μs.

Once the measurement results are available inside the DSP, the controller functions are executed and the PWM signals are generated. If the control loop runs at the switching frequency, the computation delay can be considered as one PWM cycle. Thus, the control/computation delay can be modeled with a first order unity gain system with a time constant equal to the PWM cycle. The PWM signals generated by the inverter are applied to the gate drives to generate the rectangular inverter voltages so that the required volt-seconds are applied to the UPS system in order to obtain proper control performance. If the controller has limited computational speed, then the control loop can be updated at lower frequencies than the PWM frequency. In this case the signals are synchronized such that the carrier to sampling frequency ratio is an integer. For example, for the case to be studied in this thesis, the carrier frequency is 20 kHz and the repetitive control loop runs at a sampling rate of 10 kHz. Thus the computational delay is one sampling cycle which is 100 μs.

2.3.1.2 The PWM Inverter

A PWM inverter operates based on the volt-seconds balance principle. Over a PWM cycle, the reference volt-seconds and output volt-seconds are equal. Thus, the PWM cycle average model of the inverter is a unity gain system provided that the inverter

operates within the linear modulation region. If the PWM signals are updated only once per period (at the peak or valleys of the carrier triangle), the PWM delay is half a PWM cycle. Thus, the inverter can be modeled with unity gain and half a PWM cycle delay element. For the data given in Table 2.1, the PWM frequency is 20 kHz and therefore the PWM delay is 25 μs.

Considering the inverter delay, measurement delay, and computation delay all together, the total UPS system (feedback signal to inverter output) delay can be found. For the given system the measurement delay is 90 μs, the computation delay is 100 μs and the PWM delay is 25 μs, leading to a total delay of (t_{Td}) 215 μs which corresponds to approximately two control cycles. Thus, the system can be modeled with a delay element in the s-domain as $e^{-st_{Td}}$.

2.3.1.3 Transformer and LC Filter

The LC filter structure is employed to filter the switching frequency components of the rectangular voltage pulses generated by the inverter. However it increases the output impedance of the UPS and causes distortion due to the harmonics of the load current. An ideal LC filter operating at no-load has a second order transfer function which is the ratio of output voltage to the input voltage as given in (2.7). The gain of the system is infinite at the resonant frequency. Such a case makes control applications difficult to implement.

In practice losses in the LC filter (r_L ve r_C), inverter blanking time and switching/conduction losses provide damping for the filter and bring the resonant peak to a finite value. The inverter switching and conduction losses, the transformer losses, and the inductor filter losses can all be lumped in the inductor equivalent series resistance r_L and thus included in the system. The block diagram representation of the LC filter is given in Figure 2.6. The total damping is given by $\zeta = \frac{r_C + r_L}{2}\sqrt{\frac{C}{L}}$ and it is reflected to the transfer function of the LC filter with a ζ coefficient as given in (2.8). In Figure 2.7 phase and magnitude characteristic of the

LC filter with an inductance value of 2.25 mH, capacitance value of 20 μF and damping ratio (ζ) of 0.1 is given. For frequencies below the resonant frequency of the LC filter gain is close to 1 and phase delay is close to 0°. That is the low frequency voltages applied to the LC filter are almost directly transferred to the output of the LC filter without a change in the magnitude and phase. For the given parameters, the resonant frequency of the LC filter is 750 Hz and the gain of the system is the largest at this frequency. In case a voltage with small magnitude is applied to the input of the LC filter, the output voltage is amplified and phase shifted with respect to the input voltage. It is difficult to control the output voltage harmonic components around this frequency. Beyond the resonant frequency of the LC filter, the system gain falls sharply and the high frequency (switching frequency) components of the inverter generated input voltages are filtered. The high frequency harmonic components of the load current do not cause distortion on the output voltages of the UPS due to the decrease in the output impedance.

$$G_{LC}(s) = \frac{v_o(s)}{v_i(s)} = \frac{\omega_n^2}{s^2 + \omega_n^2} \tag{2.7}$$

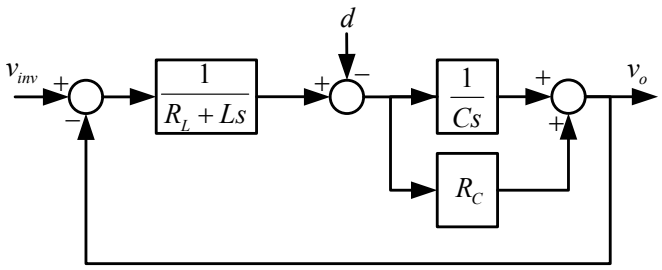

Figure 2.6 Damped LC filter system block diagram.

$$G_{LC}(s) = \frac{v_o(s)}{v_{inv}(s)} = \frac{\frac{R_C}{L}s + \frac{1}{LC}}{s^2 + 2\left(\frac{R_C + R_L}{2}\sqrt{\frac{C}{L}}\right)\frac{1}{\sqrt{LC}}s + \frac{1}{LC}} \tag{2.8}$$

Due to the Δ/Y connection of the isolation transformer, the line-to-line voltages generated by the inverter and applied to the transformer primary (Δ) windings are reflected to the transformer secondary (star or zig-zag) windings with 30° phase rotation. This implies that there is a 30° phase difference between the primary line-to-line and secondary line-to-line voltages. In other words, the output line-to-neutral voltages are determined by input line-to-line voltages. For this reason the transformer can be modeled as a 30° phase rotating element. This rotation operation will be included in the vector transformations to be soon discussed and applied to the UPS. The transfer function of the inverter to the output filter system $G_p(s)$ is given in (2.9) where the delay due to the inverter and controller are represented with the exponential term.

$$G_p(s) = \frac{v_o(s)}{v_{inv}^*(s)} = e^{-st_{T_d}} \cdot \frac{\frac{R_C}{L}s + \frac{1}{LC}}{s^2 + 2\left(\frac{R_C + R_L}{2}\sqrt{\frac{C}{L}}\right)\frac{1}{\sqrt{LC}}s + \frac{1}{LC}} \tag{2.9}$$

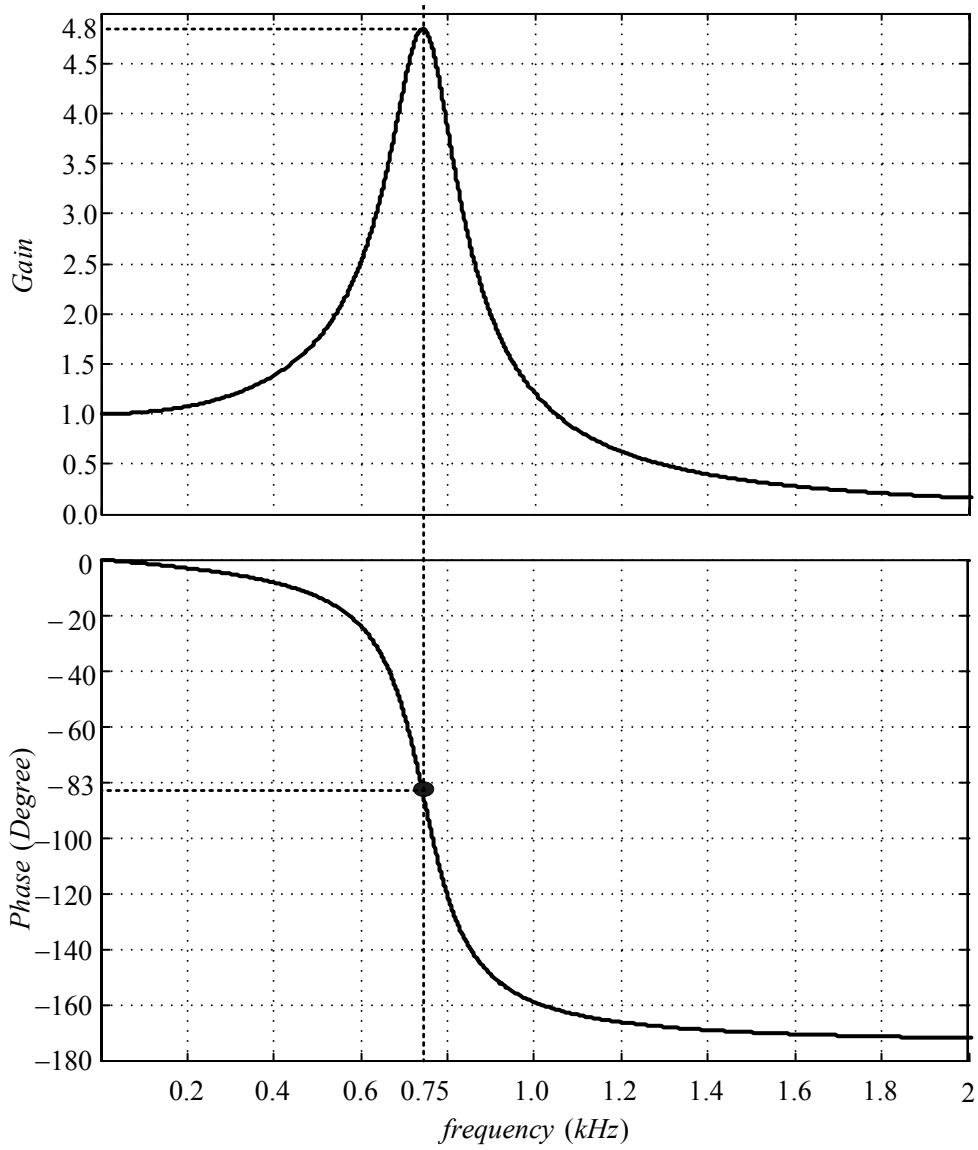

Figure 2.7 The gain and phase characteristics of the LC filter
(L=2.25 mH, C=20 μF, ξ=0.1).

2.3.2 Vector Control Principle in Complex Coordinates

In the three-leg inverter topology, the values of the voltages generated by two legs affect the third one. Because after the positions of the two legs are defined freely, the position of the third leg voltage assigns all the three-phase voltages. Thus three-phase quantities can not be controlled independently in the three-leg inverter topology and

the inverter can generate only two independent voltages. In the space vector approach, the three-phase time domain variables (x_a, x_b, x_c) are transformed to a vector ($\vec{X}$) in the stationary frame complex coordinates. The complex variable transformation formula is given in (2.10). In the formula, a is the 120° phase rotation operator term of $e^{j2\pi/3}$. When transforming the inverter voltages to the complex plane, the number of variables decrease from three to two. Since the angle between the real and imaginary components of the vector is 90°, in the complex coordinates each voltage component can be controlled independently.

$$\vec{X} = \frac{2}{3}(x_a + a\, x_b + a^2 x_c) = x_{qs} + j\, x_{ds} \tag{2.10}$$

When the balanced and nondistorted three-phase sinusoidal quantities (currents, voltages, etc.) are shown as a vector in the complex coordinates, the vector traces an ideal circular route as given in Figure 2.8. In case the output voltages of the UPS are unbalanced, the vector traces an ellipsoidal route due to the negative sequence symmetric component rotating in the opposite direction to the positive sequence symmetric component as given in Figure 2.9. Similarly if the output voltages contain harmonic components, the output voltage vector route deviates from a circular shape and resembles hexagon shape or more complex structural shapes in accordance to the frequency, magnitude and phase of the harmonics as given in Figure 2.10. In case of nonlinear and/or unbalanced loading of the UPS if the inverter reference voltage is pure circle, the output voltage vector trajectory will deviate from the circular trajectory and may take the form of hexagon due to the influence of the load current harmonics on the UPS output voltages [21].

This vector approach will be utilized in the repetitive control of three-phase output voltages for achieving high quality output voltages. In the repetitive control structure the reference vector and the output voltage vector are defined with N different

discrete points. N different integral controllers which are operated independently, control each of the discrete points on the output voltage vector. That is each controller controls only one of N discrete points on the output voltage vector trajectory. Each controller operates once per fundamental period when only the output and reference voltage vector comes to their position and sums the output voltage vector error and controller output at the previous fundamental period. In this control approach the boundaries of the inverter voltage hexagon which is the linearity region of the inverter can easily be defined and the construction of the anti-windup algorithm becomes easier with respect to the scalar method [21]. Consequently the vector approach is preferable for the repetitive output voltage control of three-phase three-leg inverter and isolation transformer based UPS. In Figure 2.11, reference voltage vector, output voltage vector and error vector at an arbitrary discrete point are given. In the figure, the output voltage vector route is turned to hexagon due to nonlinear loading and the route has narrower trajectory due to poor output voltage regulation. Because of the phase lag of the LC filter, the output voltage vector follows the reference voltage vector with a phase lag and decrease in the magnitude. In the application of the repetitive controller to the UPS system, the above mentioned effects of the inverter, LC filter, measurement and signal processing unit must be taken into account and the performance should be improved by modifying structure of the repetitive controller. In the next section, modifications in the repetitive control structure will be discussed.

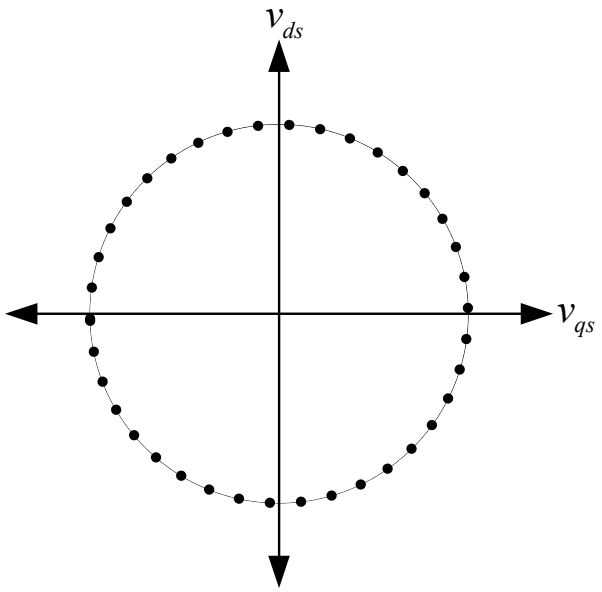

Figure 2.8 The complex voltage vectors corresponding to three-phase balanced and non-distorted sinusoidal voltages.

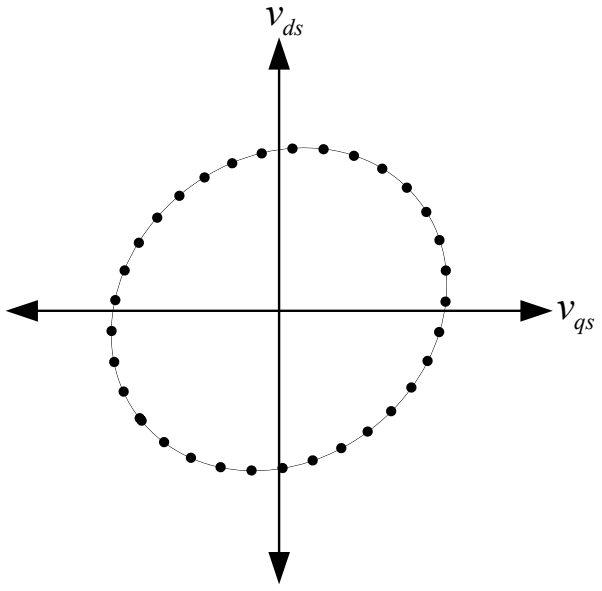

Figure 2.9 The complex voltage vectors corresponding to three-phase unbalanced and non-distorted voltages.

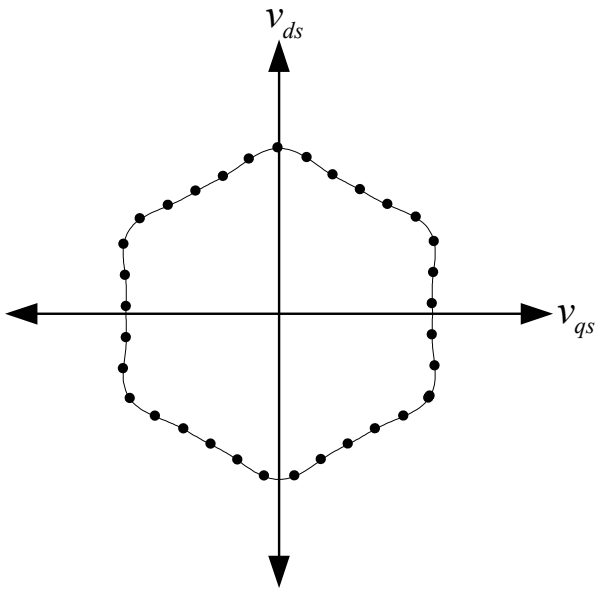

Figure 2.10 The complex voltage vectors corresponding to three-phase balanced and distorted voltages.

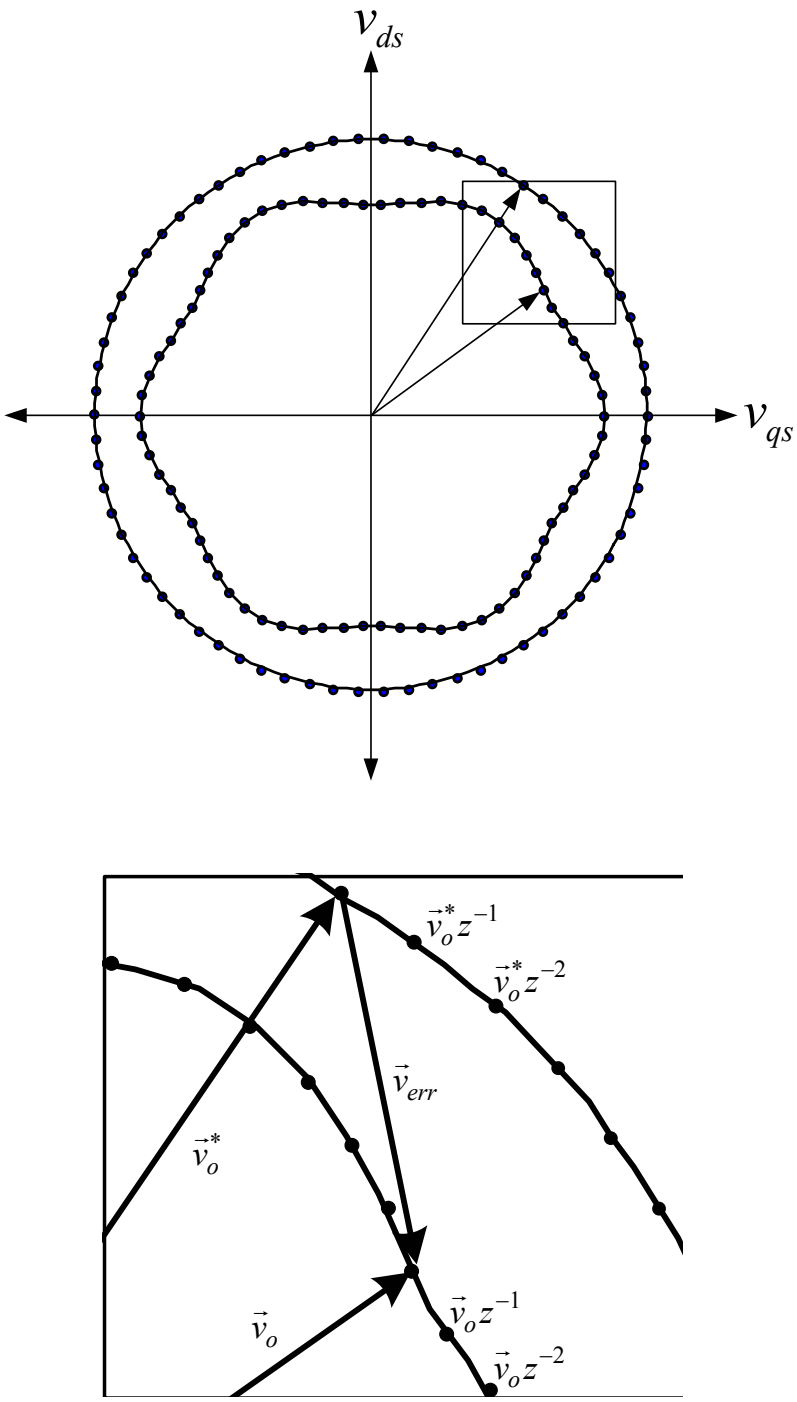

Figure 2.11 Illustration of the UPS reference and output voltage vectors in the complex plane for nonlinear loading and a poor control mechanism where a large output voltage error exists, top: full cycle, bottom:small segment [21].

2.3.3 The Repetitive Control System and Its Components

For stable and high performance operation of the repetitive controlled three-phase UPS, additional structures are required. Figure 2.12 shows the plug-in type repetitive controller including the additional structures that provide the stability of the three-phase UPS control system. In the following, the functions of the controller components will be described and a via the UPS system data given in Table 2.1, their designs will be discussed in detail.

2.3.3.1 Vector Transformation Formulas

In the mentioned controller structure, the three-phase output voltages are sampled and transformed into a vector in the stationary frame. In Figure 2.12, the *abc/qds* block transforms the three-phase quantities into the stationary frame. In (2.10) the equation utilized for the coordinate transformation from three-phase into vector was given. Two separate repetitive controllers are utilized for the control of the real and imaginary components of the output voltage vector. The real and imaginary vector components at the controller output are transformed into three-phase inverter reference voltages by the *qds/abc* inverse transformation. The inverter reference voltages are applied to the PWM unit to generate the required voltage.

If the vector transformation equations are given separately for the real and imaginary components, the transformation equation from three-phase quantities into two-axis quantities in stationary frame (at the same frequency plane) is obtained as given in (2.11) in matrix form. Utilizing this equation, three-phase quantities are transformed into two vector components that are independent from each other. In the transformation, the zero sequence component of the output voltage is neglected since the load current zero sequence component circulates through the transformer Δ windings, and not flow through the inverter. The three-wire inverter can not provide a path for the zero sequence current and therefore it can not control this zero sequence component. Therefore, neglecting the zero sequence component does not reduce the controller performance. The given equations are utilized for the transformation between the measured output voltages (at the star connection side)

and controlled voltages (at the inverter side). While the measurements and the inverter reference voltages signals are carried out for the three-phase quantities, the control is carried out for two-axis quantities. Thus, the computational burden is decreased. This control approach is called the vector control method.

$$\begin{bmatrix} x_{qs} \\ x_{ds} \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.11}$$

The stability of the closed loop control system is affected negatively when the control action is carried out without considering the phase difference between the primary and secondary winding sets of the transformer. To remove the effect of the phase advance, the transformation equation (2.10) is delayed with a phase angle of 30° and the equation (2.12) is obtained. Thus, the phase difference due to the transformer is removed in the closed-loop system. The complete version of this equation is given in (2.13). The output voltage vector components x_{qs} and x_{ds}, which are obtained by the equation (2.13), are rotated by a phase angle of 30° in the transformation equation. In the equation, the vector components, which are rotated by a phase angle of 30°, are represented with x_{qs}^{30} and x_{ds}^{30}.

$$\vec{X} = \frac{2}{3} e^{-j\pi/6} (x_a + a\, x_b + a^2 x_c) \tag{2.12}$$

$$\begin{bmatrix} x_{qs}^{30} \\ x_{ds}^{30} \end{bmatrix} = \begin{bmatrix} \sqrt{3}/2 & 1/2 \\ -1/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} x_{qs} \\ x_{ds} \end{bmatrix} \tag{2.13}$$

Utilizing equations (2.11) and (2.13), the output voltages of the transformer based UPS are transformed to the primary side and the two-axis representation is obtained as in (2.14). This equation is preferred for application due to its simplicity.

$$\begin{bmatrix} x_{qs}^{30} \\ x_{ds}^{30} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sqrt{3}/2 & 0 & -\sqrt{3}/2 \\ -1/2 & 1 & -1/2 \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.14}$$

In the vector control of the output voltages of the three-phase UPS with isolation transformer, the outputs of the controllers are the real and imaginary components of the inverter reference voltage vector that is applied to the LC filter by the inverter. Before the components of the voltage vector are applied to the modulator unit, they are transformed from two-axis quantities into three-phase quantities by utilizing the inverse transformation matrix given in (2.15). Since any zero sequence component does not exist in the two-axis transformation equations, the three-phase quantities, which are obtained by utilizing the inverse transformation equation, do not involve any zero sequence component either. Utilizing the three-phase inverter reference voltages, the modulator unit first calculates the duty cycle values for each leg of the inverter and then outputs the inverter semiconductor switch PWM signals by comparing the duty cycle values with a carrier triangle waveform.

$$\begin{bmatrix} x_a' \\ x_b' \\ x_c' \end{bmatrix} = \begin{bmatrix} \sqrt{3}/2 & 1/2 \\ 0 & 1 \\ -\sqrt{3}/2 & -1/2 \end{bmatrix} \cdot \begin{bmatrix} x_{qs} \\ x_{ds} \end{bmatrix} \tag{2.15}$$

If the inverter semiconductor switch PWM signals are obtained by comparing the three-phase inverter reference voltage signals generated at the controller output with the triangular carrier wave directly, the voltage linearity range of the inverter will be ($\pm V_{dc}/2$). This simple modulation method is called as "Sinusoidal Modulation (SPWM)" and its performance is limited. In the three-leg inverter topology, if a zero sequence signal is injected to the modulation signal there can be no zero sequence signal current flow due to the absence of the return path for this current in the three-wire inverter. Thus, a zero sequence signal can be injected to the sinusoidal modulation waves of the three phases. With an appropriate choice of the zero sequence signal, the inverter voltage linearity range can be widened [25], [26]. In this work the "Space Vector PWM (SVPWM)" method, which provides the widest inverter voltage linearity region and the minimum inverter output current ripple, is utilized. In this modulation method, first, the largest and the smallest signals of the three-phase inverter reference voltage are identified. Then, the mean of these two values gives the zero sequence component voltage that should be injected to the inverter reference voltages [27]. This PWM algorithm will be utilized throughout this thesis work.

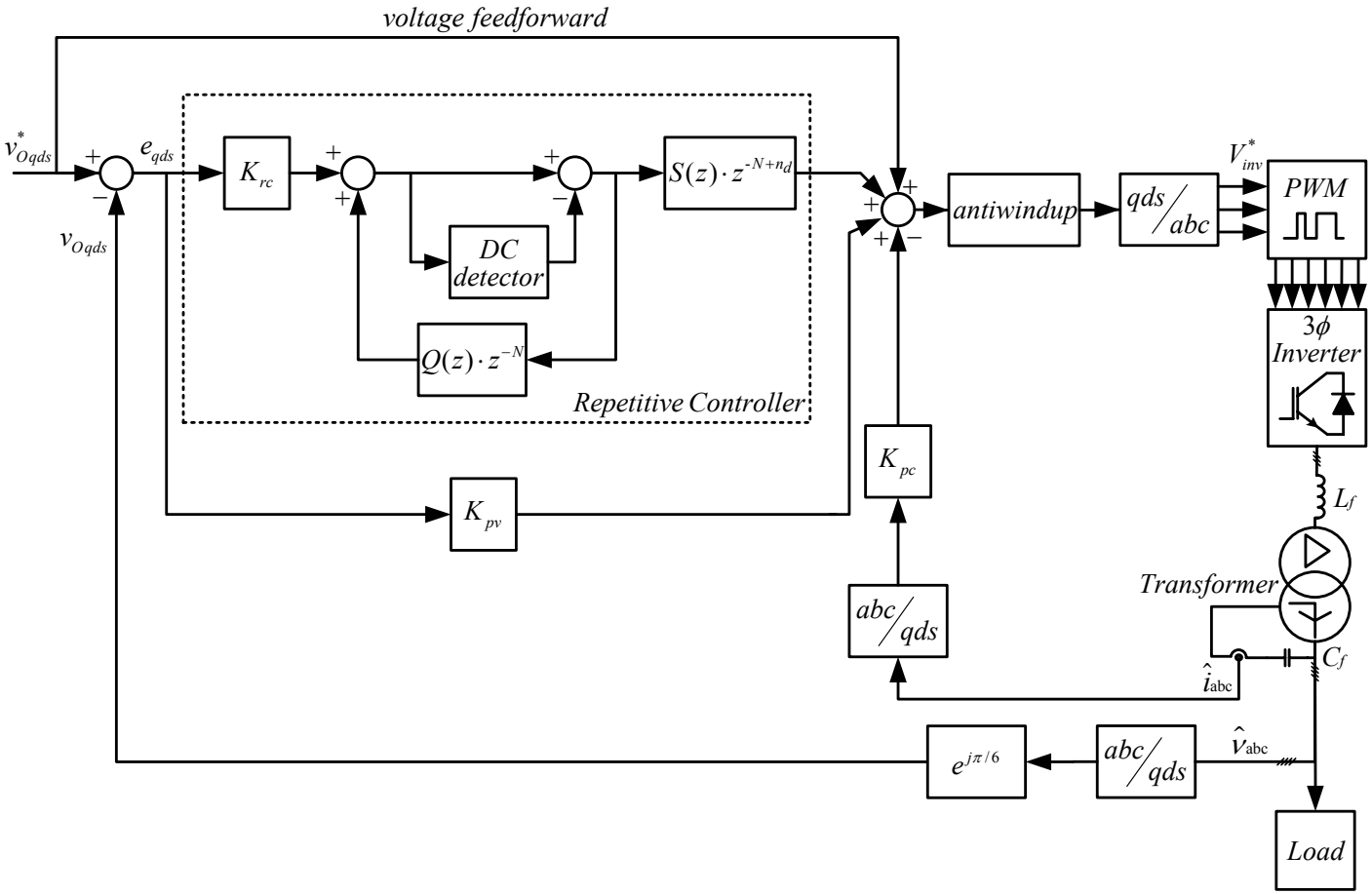

Figure 2.12 The repetitive control system block diagram of the three-phase UPS with isolation transformer.

2.3.3.2 Voltage Feedforward Controller

The voltage feedforward is provided for the purpose of starting up the UPS with a ramp function smoothly (without oscillation), ease in command tracking during normal operation, and providing the large portion of the command signal cleanly and leaving only the small error compensation signals to the feedback controller and therefore providing a room for high resolution gains in finite wordlength applications. The finite wordlength issue is particularly valid for fixed-point signal processors.

2.3.3.3 DC Offset Detector

Since the transformer does not transfer any DC component from the primary to the secondary side, DC component sourced from the primary side of the transformer does not exist on the output voltage of the UPS. Therefore, the output voltages do not include any significant DC component. However, while sensing the output voltage there may be DC component at the voltage transducer output due to noise. Similarly, since the A/D converter, which converts an analog voltage signal to a digital one, has a finite wordlength, it may add a small DC component due to quantization errors. Additionally, since the DC signal is processed in a DSP, which utilizes finite digit during the voltage error calculation, truncation errors occur and they may cause DC component on the feedback signals [28], [29]. If the DSP perceives these offsets as DC components on the output voltage, the repetitive controller integrator adds the error that shifts the inverter reference voltage up or down. As a result of this, the inverter may apply DC voltage to the transformer primary and DC current flows through the primary winding that heats the primary winding. To avoid the integrator from adding DC components, the mean value of the repetitive controller output signals in one period (N values held in the processor memory) is calculated to obtain the DC component and it is subtracted from the value of the integrator output. Thus, the DC component at the inverter output voltage is avoided and the saturation of the integrator can be prevented.

2.3.3.4 Resonant Peak Canceller *S(z)*

The gain of the LC filter is high at the resonant frequency. If the filter is excited with signals in this frequency range, the filter oscillates and the system may loose stability. Therefore, the phase and gain characteristics of the LC filter must be taken into consideration at the controller design stage. The repetitive controller output signals must be applied to the inverter by attenuating the components around the resonance frequency and higher frequencies. The filter structure that provides this attenuation is given as *S(z)* in Figure 2.12. Placed between the repetitive controller and the PWM unit, this filter structure, attenuates the controller output signals at the resonance frequency, changes the problematic structure of the controlled system and makes it controllable. Choosing *S(z)* as the inverse transfer function of the LC filter suppresses the resonance peak and removes the phase delay due to the LC filter. However, this notch filter structure may become problematic and induce instability in the practical application due to the LC filter parameter drift as the cancellation function of the inverse filter function is highly filter parameter sensitive. For this reason, instead of the inverse transfer function of the LC filter, a low-pass filter that brings the LC filter gain at the resonant frequency to practically negligible values is preferrable as it decreases the LC filter parameter sensitivity. In the controlled system, the delays due to computations, measurement, PWM etc. mainly affect the phase characteristic of the system and they have unity gain for the range below the filter resonant frequency. For this reason, the design of the resonant peak cancelling *S(z)* filter mainly involves the LC filter gain characteristic and it is sufficient to know the gain characteristic of the filter. The LC filter phase characteristic is not necessary and the delay term of e^{-st_d} in the $G_p(s)$ transfer function can also be neglected.

In addition to suppressing the resonance, the resonant peak cancelling filter, *S(z),* provides gain reduction above the resonant frequency and helps improve the system stability. Selecting the cut-off frequency of *S(z)* too low helps suppress the resonant peak effectively. However, in this case the system gain for the harmonic frequencies between the fundamental and the resonant frequency will be reduced and as a result the UPS output voltage performance will be degraded. For example, for the given

application the load current 11^{th}, 13^{th}, etc. harmonics will not be efficiently compensated and the output voltage waveform will be distorted. Therefore, there is a trade-off between the design for suppressing the resonant peak very efficiently and the design for high quality output voltage waveform. A compromise between the two is based on the application requirements of the considered UPS system. In a good design, the *S(z)* filter provides unity gain in the low frequency range and as the resonant frequency is approached the gain should drop sharply.

In order to suppress the resonant peak of the LC filter, whose parameters are given in Table 2.1 an *S(z)* filter with sharp cut-off frequency is required. For this purpose a 30th order finite impulse response filter (FIR) is utilized. For the given example, the filter cut-off frequency is selected as 500 Hz. In Figure 2.13, the z-domain gain characteristics of the LC filter $G_p(z)$, designed filter *S(z)*, and the multiplication of the two $G_p(z).S(z)$ are illustrated. As can be seen from the figure, although the gain of $G_p(z).S(z)$ is under unity for all the frequency range, the gain is near unity from zero frequency to nearly the resonant frequency of the system. Thus, the control bandwidth of the repetitive controller is maintained high so that the controller response is not sluggish.

The FIR filter coefficients are calculated by utilizing MATLAB via the FIR subroutine with the command function of fir1(30,0.1). In MATLAB, the filter coefficients are calculated based on the windowing method [30]. The filter coefficients are plotted as a function of the steps in Figure 2.14 and their numerical values are listed in Table 2.2. The discrete time formula of the FIR filter is given in (2.16). In the given structure, the filter is delayless and noncausal. In this structure, the last sampled input (the UPS output voltage) is considered with the previous and future 15 sampled inputs, thus 31 sampled inputs and coefficients are processed in (2.16). Since the UPS system is causal, the future 15 inputs are not available at the sampling instant. Thus, the peroidic property of the inputs is utilized and instead of the future 15 signals, the input values stored in their location in the previous period are utilized. This is illustrated in Figure 2.15 via the sampled inputs (UPS output voltages) over a window of 31 points. In (2.16), the $x[k+n]$ input terms can be replaced with the input terms $x[k-N+n]$ from the previous period such that the filter is

delayless and noncausal. For example, for the considered 10 kHz sampling frequency application, with the sampling number N being 200, the filter input at $x[k+5]$ is replaced with $x[k-195]$.

Since the past and future input signals (total of 31) of the filter array are the repetitive control variables and already stored in the DSP memory, there is no need to reserve additional memory space for them and they can be used from the repetitive controller directly. The filter inputs are updated every sampling interval with a sliding window.

$$y[k] = \sum_{n=-15}^{15} a_n x[k+n] \tag{2.16}$$

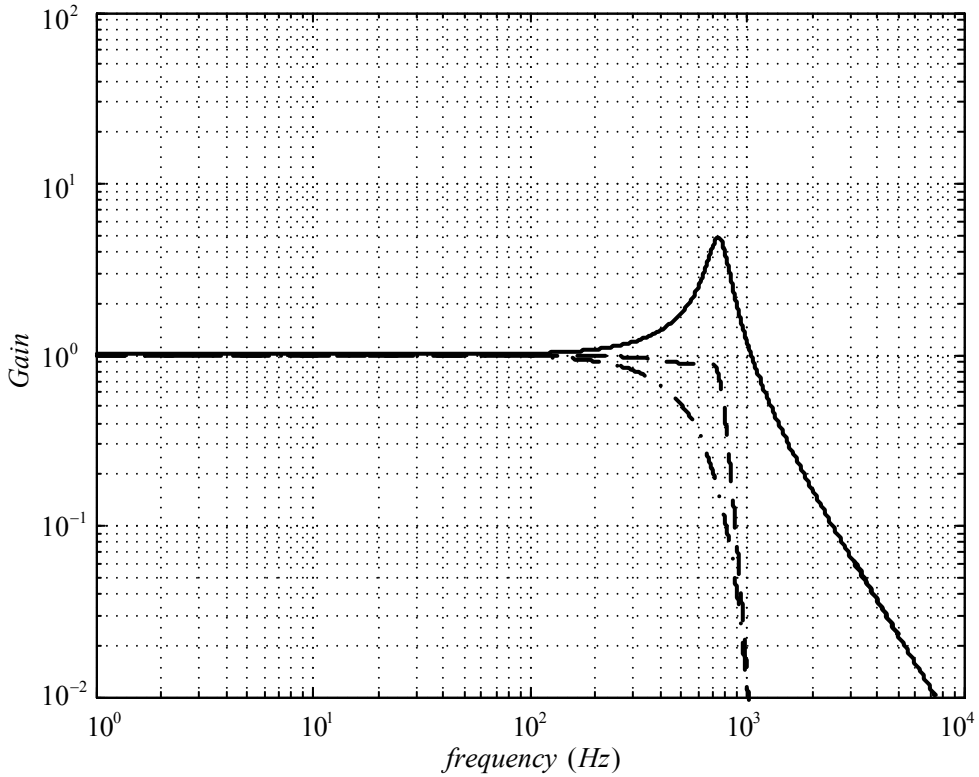

Figure 2.13 LC filter $G_p(z)$ (—), $S(z)$ filter (−·), and $G_p(z).S(z)$ (− −) transfer function gains as a function of the frequency.

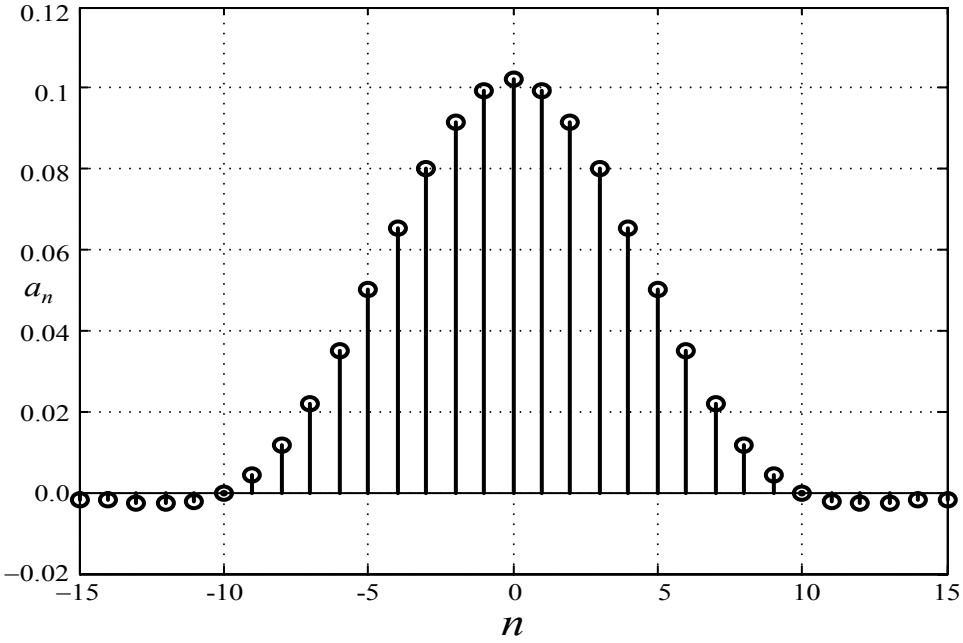

Figure 2.14 The coefficients of the 30th order noncausal delayless FIR filter.

Table 2.2 The coefficients of the 30th order noncausal delayless FIR filter

n	a_n
0	0.10207
±1	0.099386
±2	0.091684
±3	0.079916
±4	0.065489
±5	0.050032
±6	0.035129
±7	0.022082
±8	0.011742
±9	0.0044381
±10	0.0
±11	-0.0021193
±12	-0.0026711
±13	-0.0024215
±14	-0.0019875
±15	-0.0017327

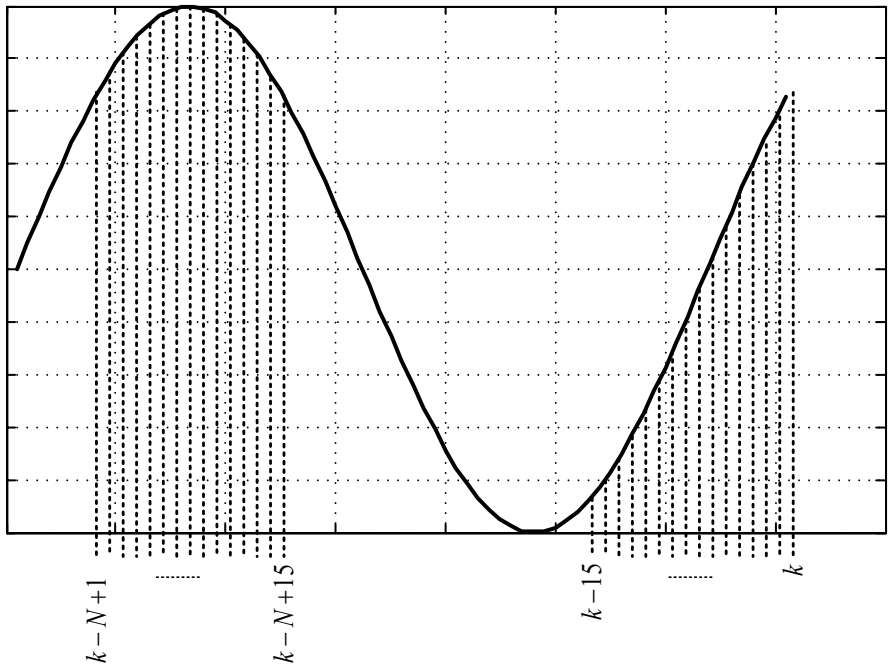

Figure 2.15 The sliding window structure used in the discrete time form of *S(z)*.

2.3.3.5 Delay Compensation

The measurement delay, computation delay, PWM delay and LC filter delay of the UPS result in a phase lag in the system. If the control signals generated by the controller for the purpose of compensating the output voltage error are applied to the inverter with a phase delay of 180^{o} or larger with respect to the output capacitor voltages, at the frequencies that this phase delay occurs the control loop operates with positive feedback and the output voltage waveform gets degraded rather than improved. As a result the system stability and overall performance get degraded.

Above the resonant frequency, although the phase delay is above 180˚, since at these frequencies the filter gain decreases and the capacitor path provides a low impedance to the load current high frequency harmonics, the effect of the harmonics above the resonant frequency can be suppressed. Therefore, performance drop of the repetitive controller above the resonant frequency range is not problematic in terms of UPS performance. However, the same can not be said for the harmonics that are below the

resonant frequency. For the harmonics below the resonant frequency, as the frequency increases the phase delay of the system increases. In this frequency range the LC filter impedance is high and the load current harmonics in this frequency range result in significant output voltage waveform distortion. Therefore, the effect of these harmonics on the output voltage should be suppressed and this implies the phase delay should be compensated for these harmonics via phase advancing.

Once measuring a feedback signal and calculating the error, the repetitive controller can not provide a correction until a fundamental cycle is past. Thus, the correction signal that will be applied after a fundamental cycle should be advanced several sampling cycles so that the phase delay is compensated. In the repetitive controller structure the z^{-N+nd} term is responsible from phase advancing the signals such that the phase delay of the signals belonging to the frequency range between the fundamental and resonant frequency is compensated. In discrete time, the integer ratio of the system delay (t_{Td}) to the sampling period (T_S) is the phase advance step number n_d given in (2.17). In the formula the "round" function rounds the number to the closest integer. To compensate for the delay effect, the controller output is applied to the inverter n_d steps ahead. Since the repetitive controller output is held in the controller memory, the only issue during implementation is regarding which step will be applied to the inverter and does not increase the memory or computational requirements. The phase advance step number is related to system stability and will be discussed in detail in later sections.

$$n_d = round\left(\frac{t_{T_d}}{T_S}\right) \tag{2.17}$$

2.3.3.6 Integral Output Limiter *Q(z)*

The ideal repetitive controller transfer function has the form of $1/(1-z^{-N})$ in the z-domain. In earlier sections it was shown that this controller provides infinity gain at all the harmonic frequencies. For the frequencies where the system open loop transfer function has a 45^{o} phase margin, the controller responds to the harmonics with delay. Although the resonant peak cancelling filter *S(z)* suppresses the high frequency harmonics to a large degree, since the filter is not ideal, the harmonics can not be completely eliminated. Thus small amount of harmonic voltage command is applied by the repetitive controller to the inverter and since the inverter is capable of generating such voltages, applying these voltages to the passive filter components resulting in output voltage distortion. The inverter itself is a high frequency harmonic generator (specifically the 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics are generated doe to inverter deadtime and other inverter nonidealities) and this also must be taken into consideration. In addition due to noise and resolution issues, the measurement equipments will provide limitation to the measurement accuracy and the measured UPS output voltages will have some noise (high frequency harmonics) on them at the DSP stage. Also nonlinear loads with high crest factor generate distortion on the UPS capacitor voltages, specifically when the capacitors are small and this results in feedback signals with harmonic content on them. For all the described reasons, the repetitive controller integrators may oscillate and their value may grow significantly. Since the discussed harmonics can not be compensated by the controller but their value appears as error, the repetitive controller attempts to generate larger voltages to compensate for these harmonics and instability results. As discussed above *S(z)* can not avoid this problem completely and output voltages oscillate and eventually the UPS fails. In summary the integral structure of the repetitive controller integrates the small magnitude high frequency output voltage errors and leads to instability. For this reason the system high frequency gain must be zero or a very small value.

The repetitive control structure of (2.3) is based on pure integration process. In case there exist high frequency terms on the output voltage error that the controller can not compensate, the error will be continuously integrated leading to controller

failure. To avoid the integrator windup, the controller structure is modified and the high frequency inputs to the controller are attenuated such that no windup occurs and the instability is avoided. This goal is achieved with the integral output high frequency attenuating filter *Q(z)* which is located in the repetitive controller memory path as shown in Figure 2.16. When *Q(z)* is a scalar, the discrete time form of the repetitive controller becomes as in (2.18) where Q is the attenuation constant. In case of scalar attenuation filter, for unity attenuation constant the ideal repetitive controller is obtained. In order to attenuate the high frequency harmonics, the attenuation constant should be selected less than unity. As *Q(z)* becomes smaller, the controller diverges from the integral controller structure and the steady-state error becomes nonzero for the harmonics in the control frequency range. As a result the output voltage low frequency harmonic content increases and the output voltage THD becomes large. Therefore, there is a limit on the attenuation rate of *Q(z)*.

$$y[k] = Q \times y[k - N] + K_{rc} \times e[k - N] \tag{2.18}$$

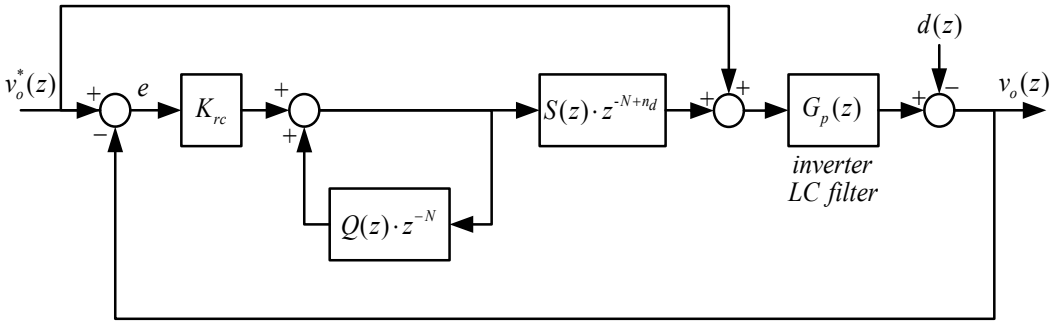

Figure 2.16 The repetitive controller closed-loop system block diagram.

The scalar filter attenuates not only the high frequency harmful signals, but also the useful low frequency harmonics that the controller can normally manipulate. Thus, with this choice the gain can not be too small. Instead of the scalar attenuation filter a low-pass filter may be utilized [23]. In order to retain the high performance of the repetitive controller for the low frequency harmonic compensation, the low frequency content of the feedback signal should not be altered. For this purpose a low-pass filter may be utilized. The low-pass filter gain is unity at low frequency and the low frequency performance of the repetitive controller can be retained. However, due to the simplicity of its implementation and satisfactory performance the scalar attenuation filter is preferrable. In the later stages of this thesis both cases will be considered.

2.3.3.7 Closed-Loop System Stability

In order to study the stability behavior of the repetitive controlled system with phase advance, integral output attenuator, and resonant peak cancellor, and finally the UPS LC filter, the mathematical model of the UPS system is required. For this purpose the closed loop controlled system model shown in Figure 2.16 will be utilized. In the structure the antiwindup controller is not shown/discussed as operation within the linear modulation range is considered. In the diagram, the inverter, the transformer, and the LC filter are modeled as the process $G_p(z)$. All the disturbances due to the load harmonics, switching device nonidealities, etc. are modeled with the disturbance input function $d(z)$. In Figure 2.16, the output voltage error (e), the reference voltage (v_o*), and the disturbance function (d) are related in z-domain with (2.19).

$$E(z)=\frac{(1-G_p(z))(z^N-Q(z))}{z^N-(Q(z)-z^{n_d}K_{rc}S(z)G_p(z))}r(z)+\frac{z^N-Q(z)}{z^N-(Q(z)-z^{n_d}K_{rc}S(z)G_p(z))}d(z) \quad (2.19)$$

The necessary and sufficient condition to operate the system stable is derived from the “small gain theorem.” According to this theorem, with T_s being the sampling

time, $\omega \in [0, \pi / T_s]$, and $H(e^{j\omega T_s}) = Q(e^{j\omega T_s}) - e^{j\omega n_d T_s} K_{rc} S(e^{j\omega T_s})\ G_p(e^{j\omega T_s})$, the condition of (2.20) must be satisfied [23], [31].

$$\left| H(e^{j\omega T_s}) \right| < 1 \tag{2.20}$$

According to this theorem, the closer $H(j\omega T_s)$ is to zero, the more improved is the system stability. Since $Q(j\omega T_s)$ is always positive and less than unity, if the magnitude of $e^{j\omega n_d T_s} K_{rc} S(e^{j\omega T_s})\ G_p(e^{j\omega T_s})$ always remains less than unity, the $H(j\omega T_s)$ avalue will also remain small and less than unity. The $S(z)$ filter utilized to cancel the resonant peak of the LC filter maintains the magnitude of the $S(j\omega T_s)G_p(j\omega T_s)$ vector under unity such that the system is stable and K_{rc} can be selected near unity for superior controller performance. Thus, the repetitive controller convergence speed increases. The harmonic rejection index (HRI) given in (2.21) is an indicator of the degree of harmonic suppression in the repetitive controller [23]. For example, with $Q(z)$ being a scalar with the value of 0.95, and perfect resonant peak suppression via $S(j\omega T_s)G_p(j\omega T_s)$ vector of $1\angle 0^\circ$, the HRI becomes as calculated in (2.22), a value of approximately 5%. This result implies that there will remain 5% of the harmonics on the output voltage at steady-state.

$$HRI = \left| \frac{\left(1 - Q(j\omega T_S)\right)}{\left(1 - H(j\omega T_S)\right)} \right| \tag{2.21}$$

$$HRI = \left| \frac{1 - 0.95}{1 - \left(0.95 - 1.0 \cdot 1\angle 0^\circ\right)} \right| = \frac{0.05}{1.05} = \frac{1}{21} \cong 5\% \tag{2.22}$$

In Figure 2.17 the geometric explanation of the "small gain theorem" is provided. In the figure the $Q(j\omega T_s)$, $e^{j\omega n_d T_s} K_{rc} S(e^{j\omega T_s}) G_p(e^{j\omega T_s})$, and their diffrence which is the $H(j\omega T_s)$ vectors are shown. Since the magnitude of $Q(j\omega T_s)$ is fixed, the magnitude of $H(j\omega T_s)$ can be found by checking whether the $e^{j\omega n_d T_s} K_{rc} S(e^{j\omega T_s}) G_p(e^{j\omega T_s})$ vector leaves the $Q(j\omega T_s)$ centered circle. Since at high frequency values the system delay is too large to be compensated by the phase compensator, the phase of the $e^{j\omega n_d T_s} K_{rc} S(e^{j\omega T_s}) G_p(e^{j\omega T_s})$ vector approaches 180°. In this case, if $Q(j\omega T_s)$ is unity, $e^{j\omega n_d T_s} K_{rc} S(e^{j\omega T_s}) G_p(e^{j\omega T_s})$ leaves the unit circle and the system becomes unstable. When a $Q(j\omega T_s)$ vector is chosen as a scalar less than unity, the center of the unit circle moves to the left and the high frequency phase delayed vector $e^{j\omega n_d T_s} K_{rc} S(e^{j\omega T_s}) G_p(e^{j\omega T_s})$ can not reduce the system stability. In the case that the attenuation filter $Q(j\omega T_s)$ is chosen as a low-pass filter, sinde the gain of $Q(j\omega T_s)$ decreases the center of the circle will move towards left leading to system stability. From the figure the influence of $S(j\omega T_s)$ on the system can also be seen. In case $S(j\omega T_s$ is not present in the system, near the resonant frequency the magnitude of the $e^{j\omega n_d T_s} K_{rc} S(e^{j\omega T_s}) G_p(e^{j\omega T_s})$ vector will increase to large values and leave the circle leading to unstable operation. With the repetitive controller gain (K_{rc}) being selected too small, the vector magnitude is adjusted and the system stability is maintained. In this case, the system settling time incerases and dynamic and steady-state performance is degraded.

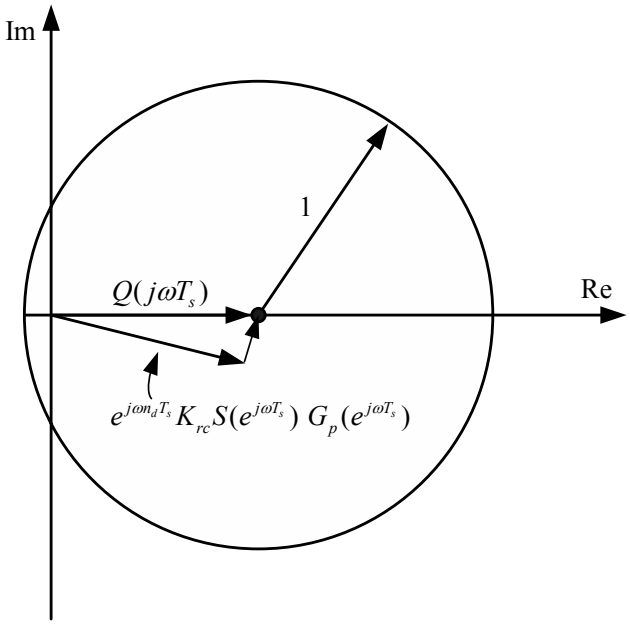

Figure 2.17 Illustration of the sufficient condition of the stability.

The basic rule in the repetitive controller design is to select the gains such that the system operates stably. The waveform quality criteria comes second [23]. The magnitude of $H(j\omega T_s)$ should be as small as the design rules allow. This condition can be imposed on the closed-loop system structure by forcing the magnitude and phase of $e^{j\omega n_d T_s} S(e^{j\omega T_s}) G_p(e^{j\omega T_s})$ to be unity and 0° respectively. Since in practice the filter parameters can not be exactly known or they are not constant, the inverse transfer function of the LC filter is difficult to obtain. Instead a low-pass filter can be utilized and this results in phase delay in the system. The amount of phase delay created by the filter could be compensated by phase advancing the controller.

Since the repetitive controller is a pure integrator, without compensation of the UPS system delay the wrong vector is taken to the integrator and the integrator value grows leading to instability. However, if the delays are compensated for by phase advancing, the system stability can be regained and dynamic performance improved. The closed loop controller system delays are measurement, computation, PWM and LC filter delays. Except for the last one, the delays as previously discussed can be

modeled with a fixed step number delay element and the compensation can be done by simply advancing the controller with the number of steps corresponding to these delays. The LC filter delay, however is neither fixed nor linear. For 10kHz sampling frequency and for the fifth harmonic of 250 Hz, the LC filter delay is 5˚ (55 μs) and for the 650 Hz component the delay is 35˚(150 μs). Thus, the delay and therefore the compensation amount can only be found from the filter phase characteristic. Since *S(z)* is applied with a delayless noncausal filter, the $S(z).G_p(z)$ system delay is only due to the LC filter. Compensating the LC filter term with different step numbers, the various $H(j\omega T_s)$ function trajectories can be obtained. In Figure 2.18, the $H(j\omega T_s)$ trajectory with no phase advance is shown for scalar *Q* of 0.95 value case. As can be seen from the waveform, near the resonant frequency the H function leaves the circle and the system becomes unstable. The breakpoints can be utilized to calculate the phase advance steps so that the system can be stabilized. For the LC filter characteristic given in Figure 2.7, the resonant frequency of 750 Hz has a phase lag 83˚ corresponding to 307μs delay and for the 100 μs sampling time, this involves 3 control step delays. Thus, a three step phase advance can be given due to the LC filter. The above discussed other delays also require 2 step phase advance. This results in five steps as a total phase advance. With the phase advance chosen as 5 steps or 500μs, the $H(j\omega T_s)$ function follows the stable trajectory shown in Figure 2.19.

Of the two *Q(z)* forms utilized each has advantages and disadvantages. The attributes of these filters can also be observed on the $H(j\omega T_s)$ function as they affect the stability of the system. For scalar *Q(z)* of 0.95 the function is shown in Figure 2.19. At high frequencies the $H(j\omega T_s)$ function approaches the right side of the unit circle and the stability is decreased. With the low-pass filter type *Q(z)*, the low frequency harmonics can be compensated with the repetitive controller better. FIR filters can be utilized for this function. For $Q(z)=0.25z^{-1}+0.5+0.25z$ the $H(j\omega T_s)$ function is shown in Figure 2.20. In this case the phase advance is taken as 5 steps. As can be seen the magnitude of $H(j\omega T_s)$ has decreased and the stability of the system is improved. Also the distance from the unit circle has increased compared to the scalar $Q(z)=0.95$ case indicating better stability.

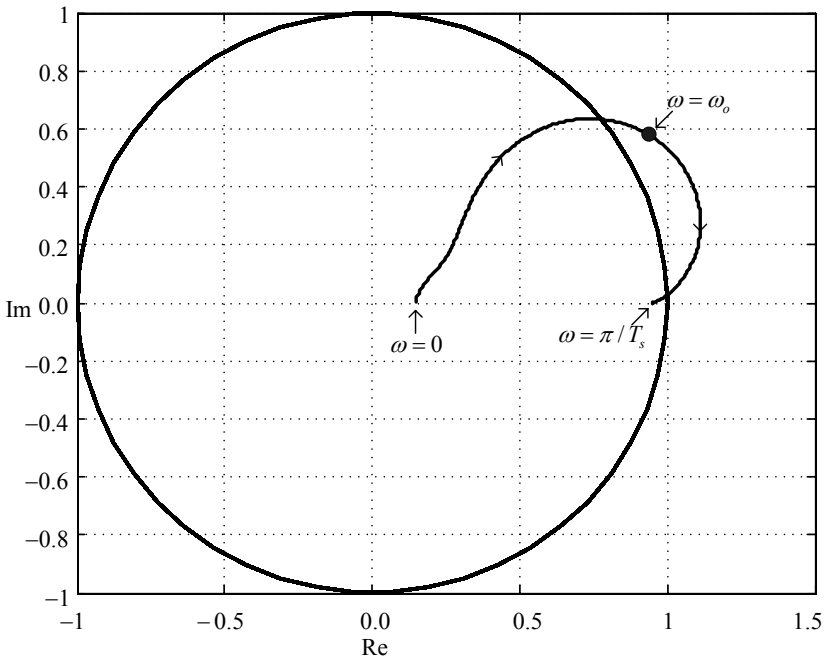

Figure 2.18 The frequency characteristic of $H(j\omega T_s)$ with no phase advance.

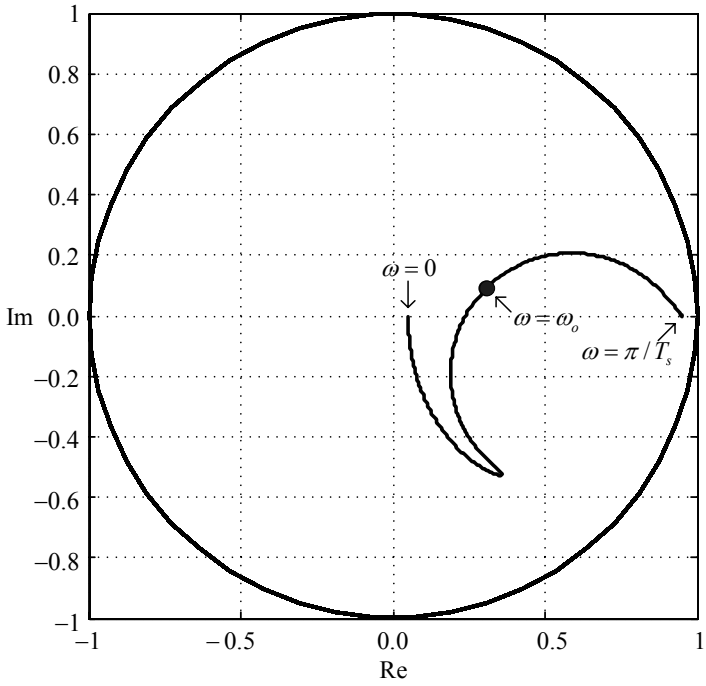

Figure 2.19 The frequency characteristic of $H(j\omega T_s)$ with five-step phase advance.

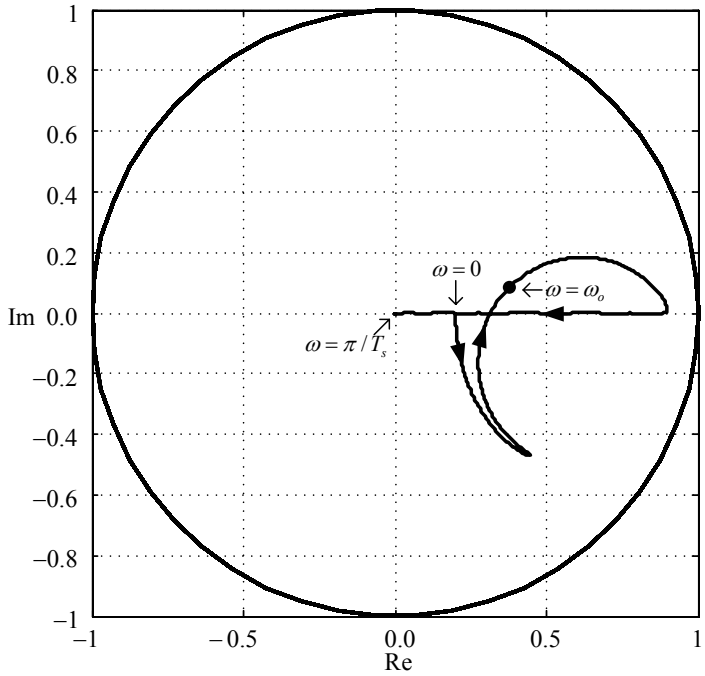

Figure 2.20 The trajectory of $H(j\omega T_s)$ with $Q(z)$ as a low pass filter and n_d=5.

2.3.3.7 Integrator Anti-windup Algorithm

High crest factor loads result in large distortion in specific portions of the output voltages. The repetitive controller attempts to compensate for these distortions by applying a large voltage over these regions and may cause inverter voltage saturation. To avoid this problem, an anti-windup controller is employed. The basic principle of the anti-windup algorithm is as follows. The angle of the reference voltage vector generated by the control algorithm is calculated from the qs and ds components of the reference voltage vector. If the angle is within the first 60^o segment it is kept, otherwise an integer multiple of 60^o values is subtractef from this angle to place this angle in the first 60^o segment of the voltage vector space. Then the largest voltage vector that can be generated from the inverter hexagon for this angle is calculated in (2.23). If the controller output is larger than the inverter voltage vector, then by retaining the angle of the reference voltage vector but modifying its magnitude the inverter output and the integrator value at the memory location are confined. Since a large portion of the inverter output voltage is provided by the

voltage feedforward term, the integrator boundary value can be found from the difference of the voltage feedforward term and the largest inverter output available (a point on the inverter hexagon as shown in Figure 2.21).

$$V_{\max} = \frac{2}{3} \frac{V_{DC} \sin\left(\frac{\pi}{3}\right)}{\sin(\theta) + \sin\left(\frac{\pi}{3} - \theta\right)} \tag{2.23}$$

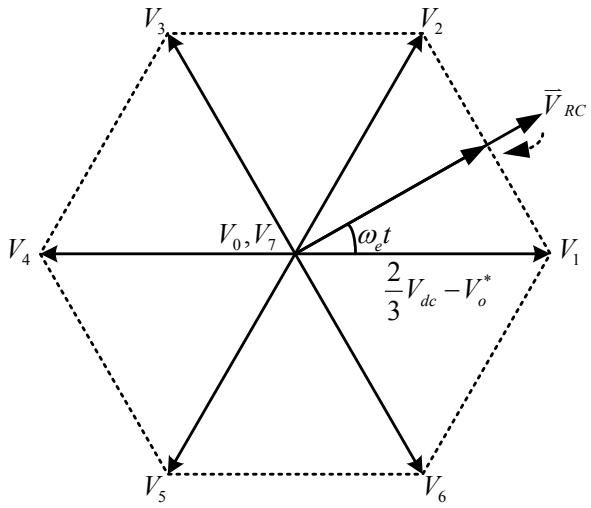

Figure 2.21 Inverter voltage linearity boundaries defining the anti-windup algorithm.

This chapter has founded the repetitive controller algorithm basics. The basic repetitive controller and the additional control units which are vital for the success of a practical repetitive controller have been investigated theoretically. The theory has been supported by illustrations of a numerical study. The following chapter utilizes the numerical case study and provides detailed controller design and performance study by means of computer simulations.

CHAPTER 3

PERFORMANCE EVALUATION OF THE REPETITIVE CONTROL METHOD FOR THE TRANSFORMER BASED THREE-PHASE UPS BY MEANS OF COMPUTER SIMULATIONS

3.1 Introduction

In this chapter, the design and performance evaluation of the repetitive control method for the transformer based UPS system, which was theoretically investigated in the previous chapter, is conducted by means of computer simulations. In the previous section the basic repetitive control system was developed and its design rules discussed. In this chapter, the elements of the control system will be designed according to the discussed design rules. The UPS system computer simulation model will be built and then the trial and error based numerical design for the main control blocks will be conducted by means of computer simulations. Given the trial and error based method optimized control parameters, the computer simulation based detailed steady-state and dynamic performance evaluation of the UPS system will follow. Since nonlinear loads create the largest disturbance to the UPS output voltages, the controller design and general performance tests will be conducted with a three-phase nonlinear diode rectifier load. Before the controller design is pursued, the passive power components, namely the transformer, output capacitors and filter inductors will be sized so that the controller design utilizes these elements as given.

3.2 Design of The Passive Components

In this section, the selection of the output capacitors, isolation transformer and the series inductor filters is discussed. A design for the three-phase, 5-kVA, 220V_{rms}/phase UPS is provided. In practical design, first the output capacitors are selected, the isolation transformer is specified. Then, if the transformer leakage inductance is not sufficient to suppress the inverter PWM ripple current, additional series inductor filters are inserted between the inverter output terminals and transformer Δ primary windings.

3.2.1 Filter Capacitors

Filter capacitors of the UPS trap the switching frequency ripple currents and provide smooth UPS output voltages. They also provide low impedance path (reduce the output impedance) to the load harmonic currents and decrease the distortion on the output voltage under nonlinear loading conditions. Additionally, they limit the voltage sag/surge during loading/unloading transients. The larger the capacitor filter size, the smoother the output voltage during steady-state and the smaller the sag/surge during transients. However, with large filter capacitors, leading power factor load operating conditions result in large inverter currents as the reactive power provided by both the load and the capacitor must be taken by the inverter. A trade-off between the two boundaries provides the design range for the output filter capacitors. In UPS applications, typically, the capacitor value of the LC filter is designed to carry fundamental frequency current equal to 20% of the nominal load current.

For a 5-kVA, 220-V_{rms}, 50-Hz rated UPS system the rated load current is 7.5 A. The fundamental component of capacitor current is calculated from (3.1). For the given ratings, the resulting capacitor value is 22 μF/phase for star connection. A practically available value of 20 μF is chosen in this study. Also the losses of the capacitors are modeled with an equivalent series resistor of 0.2Ω/phase in this study.

$$C_f = \frac{0.2 \cdot I_{rated}}{2\pi f_e V_{rated}} \tag{3.1}$$

3.2.2 Isolation Transformer

The isolation transformer is used in the UPS system for several purposes. The prime purposes are the galvanic isolation and the availability of the path for the zero sequence currents via the star connection of the secondary of the transformer. When the input rectifier is a step-down rectifier, for the three-phase 220Vrms/phase utility grid, the DC bus voltage of the rectifier is in the range of 400-500V. An inverter can not directly provide 220Vrms/phase at the output from this DC bus voltage level. For this purpose an isolation transformer is utilized and via Δ/Y windings with typically 1:1 turns ratio allows to increase the DC bus voltage effectively to $\sqrt{3}$ so that the rated output voltage can be obtained. The leakage inductances of the transformer windings are beneficial for suppressing the PWM current ripple. If the equivalent leakage inductance is not sufficient to suppress the PWM ripple current, additional filter inductances are added in series with the primary windings of the transformer.

A Δ/Y isolation transformer has been designed for the experimental work in this thesis. The 10-kVA transformer ratings are summarized in Table 3.1. The transformer was manufactured by a local manufacturer and its open-circuit test results are shown in Figure 3.1, and the efficiency tests are shown in Figure 3.2. In both tests the transformer was fed from the 50-Hz AC utility via a variable transformer. The transformer single-phase equivalent circuit is shown in Figure 3.3. The equivalent circuit parameters are also given in Table 3.1 and they are calculated from the open-circuit and short-circuit tests.

Table 3.1 The ratings and parameters of the Δ/Y isolation transformer

S	Power rating	10 kVA
V_r	Voltage rating	240 V_{rms}
I_r	Current rating	16 A_{rms}
N_{xfrm}	Turns ratio	1:1
$L_{LK1}+L_{LK2}'$	Equivalent leakage inductance	800 μH
r_1+r_2'	Equivalent winding resistance	0.5 Ω
L_m	Magnetizing inductance	1.42 H
r_c	Core loss equivalent resistance	893 Ω

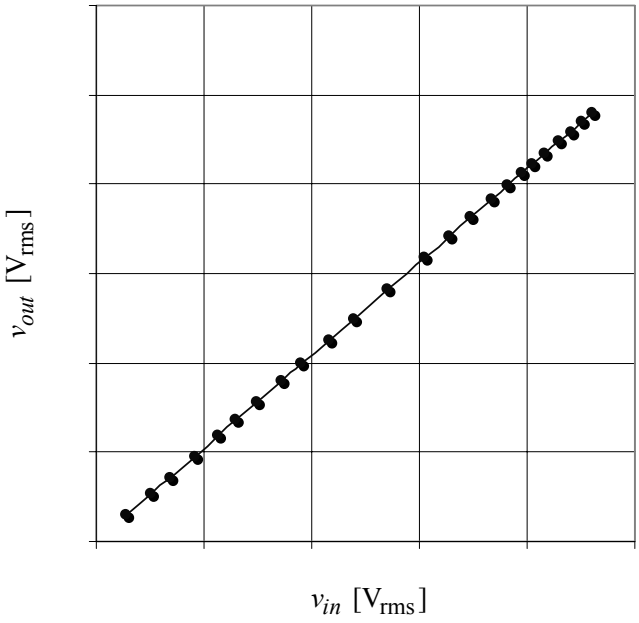

Figure 3.1 The output voltage - input voltage curve of the isolation transformer for Y/Y connection.

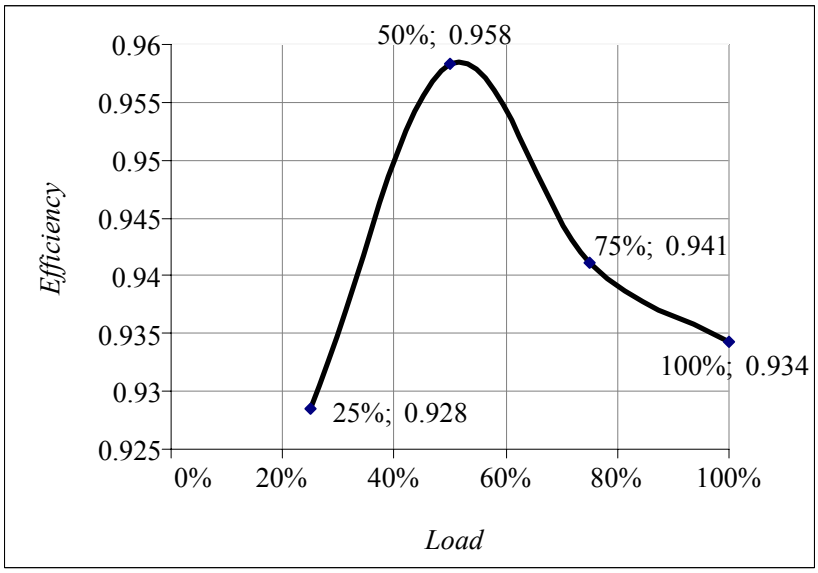

Figure 3.2 Efficiency of the transformer as a function of loading.

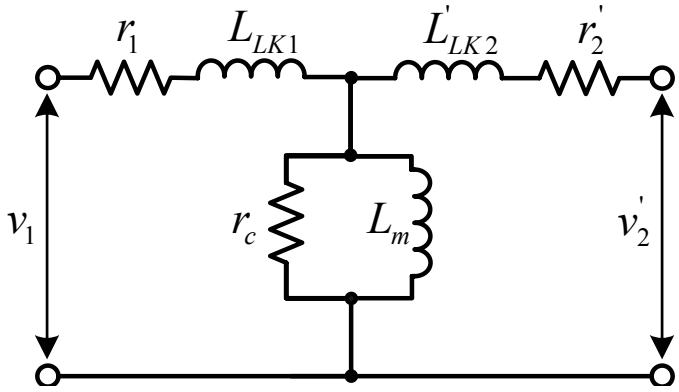

Figure 3.3 The primary referred single-phase equivalent circuit of the transformer.

3.2.3 High Frequency Inductors

The cut-off frequency of the LC filter with capacitors and only the transformer leakage inductance is 1.25 kHz which a high value for a typical UPS. In order to lower the cut-off frequency to 750 Hz (a typical value) additionally 500 μH/phase ferrite core based inductors are connected in series between the inverter terminals and the transformer primary windings. The transformer secondary referred equivalent inductance is 800 μH /phase. Since the added inductor reflects to the transformer secondary as three times due to the Δ/Y connection, its secondary side equivalent is 1500 μH/phase. As a result the equivalent filter inductance at the output is 2300 μH/phase.

With the Δ/Y transformer connection, under unbalanced or nonlinear load operating conditions, zero sequence components of the load currents can be trapped in the Δ connected primary windings of the transformer. In order to reduce the effect of the zero sequence component currents on the output voltages, the zero sequence currents should flow through the transformer rather than the output capacitors. For that purpose, the Δ winding leakage inductances should be small. If the additional filter inductors are placed within the Δ connected primary windings of the transformer or at the secondary side of the transformer, zero sequence current path impedance is increased [33]. Thus the inductors are connected between the inverter and the transformer.

In the system model, the inductor filter ESR will also be modeled. However, its value will not only represent the losses in this element, but the inverter losses (switching, conduction etc.) are also included in it. The value selected for the ESR of the inductor is 1 ohm/phase.

3.3 Building The Computer Simulation Model of The Isolation Transformer Based UPS System

The computer simulation program, which will be used to predict the performance of the designed repetitive controlled UPS system, is established by utilizing the Ansoft-Simplorer computer simulation software [35]. Ansoft-Simplorer is a graphic window based power electronic circuit simulator in which the power electronics system is formed by picking and placing the required components from its library on to its graphic window. This graphic window is also called the circuit schematic diagram of the program. The variables of the simulated program such as currents, voltages etc. are observed from the ViewTool graphic window. In the day-postprocessor window, the waveforms obtained from the simulation results are evaluated by utilizing analysis tools such as the harmonic calculator, THD calculator, power factor calculator, crest factor calculator, etc.

Ansoft-Simplorer allows various integration methods for the purpose of execution of the program. In the given repetitive control application, the UPS system dynamic response is fairly slow. The start-up dynamics and loading/unloading dynamics last for longer durations than several fundamental cycles. Including all these stages in the study requires operating the UPS system for longer than a second. Modeling these transients in one simulation run, and involving the full model of the UPS system, very large memory and simulation run time become necessary. Thus, the approach becomes exhaustive and unnecessarily slow. An alternative approach involves utilization of the inverter average model. In this case the PWM operated inverter is modeled with an ideal voltage amplifier with no switching ripple. In this case, the simulation variables do not change as fast and the integration method can be simple and the integration step size can be made large. Thus the inverter average model based approach is utilized in this work. In the computer simulation, the trapezoidal integration method is utilized. The maximum and minimum step sizes are selected to minimize the computational errors and obtain high accuracy in the simulations without excessive data storage and computational burden. The minimum and maximum simulation step sizes are chosen as 5 μs and 10 μs respectively. The

control blocks are executed in the equation blocks of the software and these are updated at the rate of 50 μs or slower.

In the following, the elements of the computer simulation model, namely the inverter, the DSP, the sensors, load will be discussed and their simulation implementation will be detailed.

3.3.1 The Inverter Average Model

Since the PWM inverter is a linear amplifier with a unity gain below the saturation limit, it can be modeled as a dependent voltage source, the output of which is dependent on the voltage command given to the inverter (by the UPS output voltage controller). The inverter average model provides the same volt·second product (average value) over one switching period as the full inverter model involving switches. The practical implementation to be discussed in the next chapter and the computer simulations considered in this chapter involve a UPS system operating at 20 kHz switching frequency. The PWM signals are updated once per carrier cycle indicating that the average model is updated every 50μs. Over every 50μs, the output voltage of a practical inverter has a pulsating rectangular shape, while the average model generates a constant output voltage at its output terminals. Thus, the minimum integration step size in the simulations is selected one-tenth of the inverter PWM average voltage updating cycle (50 μs vs. 5μs).

Practically the maximum achievable inverter output voltage is limited by the DC bus voltage value. For each inverter leg the output voltage is thus limited to half of the DC bus voltage value. If the command value is within this range the inverter provides an output voltage equal to the reference value. If the reference value is outside this limit, then the inverter saturates and the output voltage can not increase beyond this limit. Thus the linearity is lost. In the average model this behavior is modeled with a limiter for each leg of the inverter. Considering that the DC bus voltage is typically obtained from the three-phase $220V_{rms}$/phase, 50-Hz AC grid via

a three-phase rectifier, the DC bus voltage is 500V DC and thus the voltage linearity limits are set to ±250V.

3.3.2 The Controller (DSP) Simulation Model

In order to emulate the DSP controller, which is a discrete time system, the basic 'Equation Block' module of the Simplorer software which is obtained from "Signal Processing Blocks" toolbox is used. The block provides numerical links between input signals and block internal variables. By executing the written code, the equation block generates data that is sent to the block output. The code can be written with standard mathematical functions and conditionals of the Simplorer software. Also the sampling rate can be adjusted from 'Sample Time' parameter of the block. Inherently the outputs are generated without a computational delay. In order to emulate the calculation delay of the microprocessor, the outputs should be generated with one sampling time delay in the code.

3.3.3 Voltage and Current Sensor Models

In the experiments (to be discussed in the next chapter), the output voltages of the UPS are measured by three 220V/9V measurement transformers. Since isolation transformers do not transfer the DC voltages of the primary side to the secondary side, the output voltages do not have DC components. The measurement transformers do not transfer DC voltages either. As a result the measurement transformer output signals are AC. The measurement transformers were tested in the laboratory at various operating frequencies (50Hz to 1.5 kHz) and their gain and phase characteristics were recorded. For the test the UPS prototype to be studied in the next chapter was utilized as an open-loop programmable voltage source. The inverter was utilized to generate output voltages with two components. The 50Hz signal had $100V_{peak}$ and the injection signal had $50V_{peak}$. The UPS output was measured by a high bandwidth differential probe and by the discussed measurement transformers. Based on these two measurements, the phase difference between the two signals was recorded and considered in time units. It was recorded that the

transformers follow the actual voltage with an approximate delay of 90 μs. In the simulation, this delay is modeled by an analog first order delay element consisting of an RC circuit with a time constant of 90 μs.

In the application, the UPS output capacitor currents are measured with current transformers. Similar to the voltage measurement transformers, the current transformers (CTs) were also characterized experimentally. Based on the measurements it has been found out that the CTs have a bandwidth approximately 20 kHz. For this reason, the CTs are also modeled in the simulation with a first order delay element of 50 μs time constant.

3.3.4 Nonlinear Load

In the simulation environment, UPS system is loaded with a balanced nonlinear load of three-phase diode rectifier with a large capacitor and resistor. The parameters of the nonlinear load shown in Figure 3.4 are given in Table 3.2. The same load may be connected in different connection configurations to load the UPS with balanced, single-phase unbalanced and line-to-line unbalanced loads.

Table 3.2 The parameters of the three-phase diode rectifier based nonlinear load

Inductance of the input cable	L_{cable}	2 μH
Resistance of the input cable	R_{cable}	200 mΩ
DC bus capacitor of the rectifier	C_{DC}	1000 μF
DC load resistance of the rectifier	R_{DC}	96 Ω

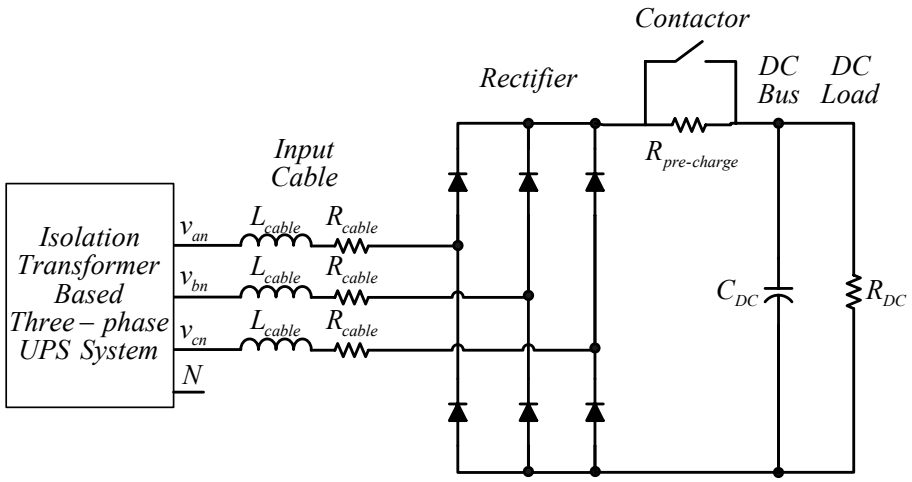

Figure 3.4 The three-phase diode rectifier based nonlinear load circuit diagram.

This section provided detailed information on the system component models to be utilized in the computer simulations. The summary of the simulated system parameters is given in Table 3.3. With the system parameters and models given, the computer simulation program could be built. The Ansoft-Simplorer based system simulation block diagram is given in Figure 3.5. The next section involves the repetitive controller parameter tuning via computer simulations.

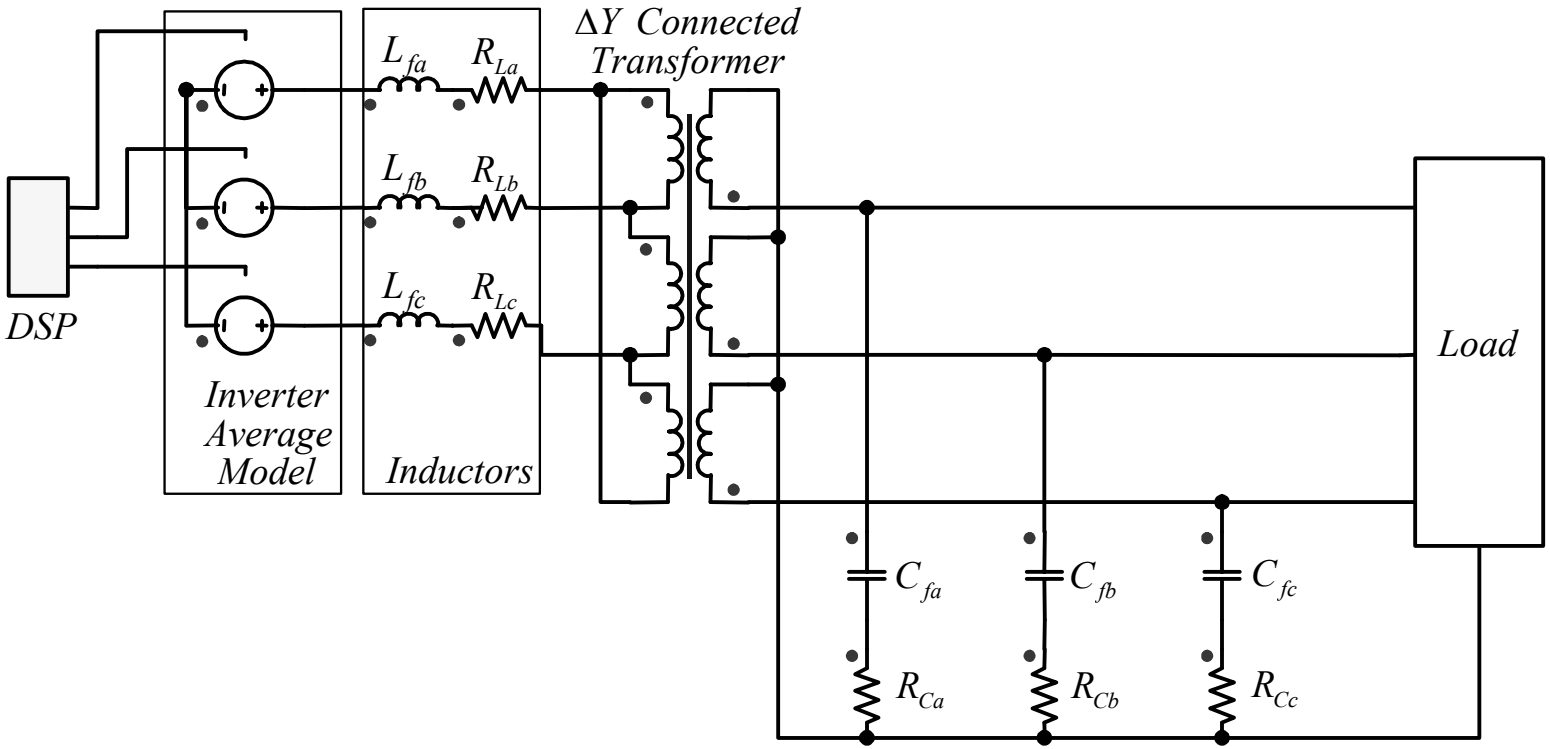

Figure 3.5 Power stage of the transformer based UPS system simulation model circuit diagram (Simplorer V7.0 Schematic ssh file).

Table 3.3 The UPS system parameters to be utilized in the simulations

Inverter	DC bus voltage	V_{dc}	500 V
	Switching frequency	f_{sw}	20 kHz
UPS Output Filter	Filter capacitor (per phase)	C_f	20 μF
	ESR of the filter capacitor	r_C	0.2 Ω
	Transformer leakage inductance	L_{xfrm}	0.8 mH
	Transformer turns ratio	N_{xfrm}	1.0
	High frequency filter inductor (per phase)	L_f	0.5 mH
	ESR of the inductor	r_L	1Ω
UPS Output Ratings	Voltage	V_o	3×220/380 V
	Frequency	f	50 Hz
	Power	S	5 kVA
Controller Update Rate	Update frequency of proportional gain for voltage error and capacitor current feedback	f_p	20 kHz
	Update frequency of the repetitive controller	f_{rc}	10 kHz

3.4 Steady-State Operating Performance of Open-loop Controlled Isolation Transformer Based Three-Phase UPS With Nonlinear Load

The goal of this section is to illustrate the open-loop steady-state performance of the isolation transformer based three-phase UPS under nonlinear load operating condition. The UPS will be voltage feedforward controlled and no feedback loops will be involved. As worst case load type, the nonlinear load will be considered and operation under both balanced and unbalanced loads will be investigated. The open-loop steady-state performance characteristics will be displayed for the purpose of illustration of the performance problems of the UPS under such operating conditions and for comparison with closed-loop controlled UPS case to indicate the degree of improvement the controller provides. First balanced rated load and then unbalanced load cases will be discussed. Here the rated balanced load is defined as 5 kVA at the

nonlinear load terminals. Since this load draws harmonic rich current, the power factor is poor, thus the average power is less than the apparent power of the rectifier.

3.4.1 UPS Output Performance Under Balanced Nonlinear Load

Open-loop controlled steady-state operation under rated kVA nonlinear balanced load is simulated via Simplorer and the resulting waveforms are reported in the following. The three-phase output voltages and the load current for one phase are shown in Figure 3.6. The large DC bus capacitor of the nonlinear load results in nearly triangular output voltage waveform indicating significant output voltage distortion. Since the output voltage deviates from a pure sinusoidal waveform and becomes flat, the current waveform becomes softer and the crest factor is not very high. Executing the steady-state simulation data with the Day Postprocessor of Simplorer, the output voltage THD is found as 6.71% and the crest factor is 1.26 which is a very low value due to the flat current waveform. The harmonic spectrum of the UPS output voltage for one phase again is obtained via Day Postprocessor and plotted in Figure 3.7. The figure shows that the low frequency odd non-triplen harmonics exist and the 5^{th}, 7^{th}, 11^{th}, and 13^{th} are dominant. The voltage regulation is 14.5% indicating significant voltage drop on the filter impedance due to loading.

One phase UPS output voltage, one of three line-to-line inverter voltages, load current, transformer secondary current, and capacitor current waveforms are given in Figure 3.8. Since only voltage feedforward control is utilized the inverter generates voltages with sinusoidal waveform (without harmonics). The harmonic rich current dominantly finds the lowest impedance path as the capacitor rather than the transformer secondary. As a result the capacitor current becomes harmonic rich and the output voltage gets distorted. Illustrating the control variables in the stationary complex coordinates, as Figure 3.9 shows, the inverter output voltage becomes an ideal circle (since the inverter average model is utilized the switching ripple is not considered) while the UPS output voltage approaches a hexagonal shape. In the diagram the inverter output voltage circle is significantly smaller than the UPS output voltage hexagon due to the fact that the Δ/Y transformer involved scales up the inverter voltages with $\sqrt{3}$ to generate the UPS output voltages.

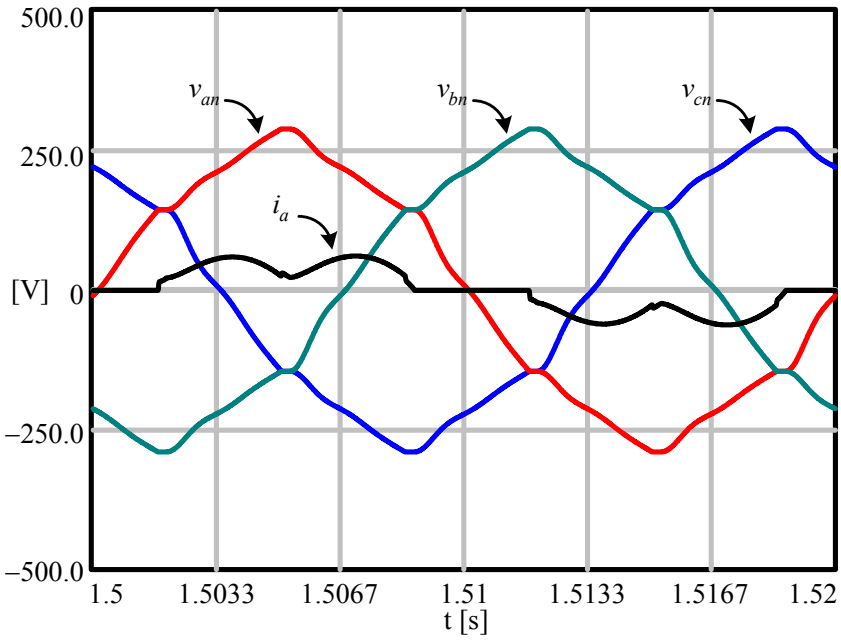

Figure 3.6 UPS output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current (i_a) (×10) for open-loop controlled operation with balanced nonlinear load.

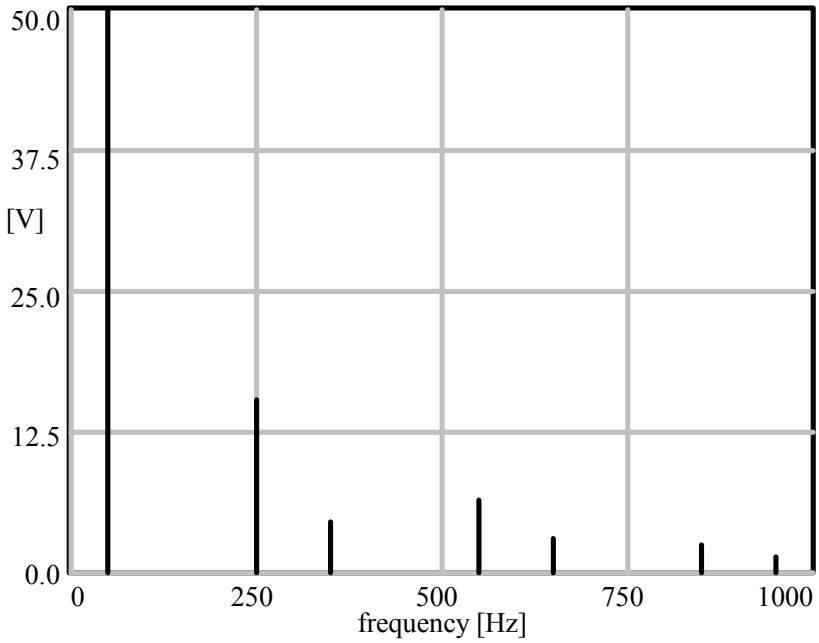

Figure 3.7 Harmonic spectrum of the line-to-neutral output voltage for open-loop controlled operation with balanced nonlinear load.

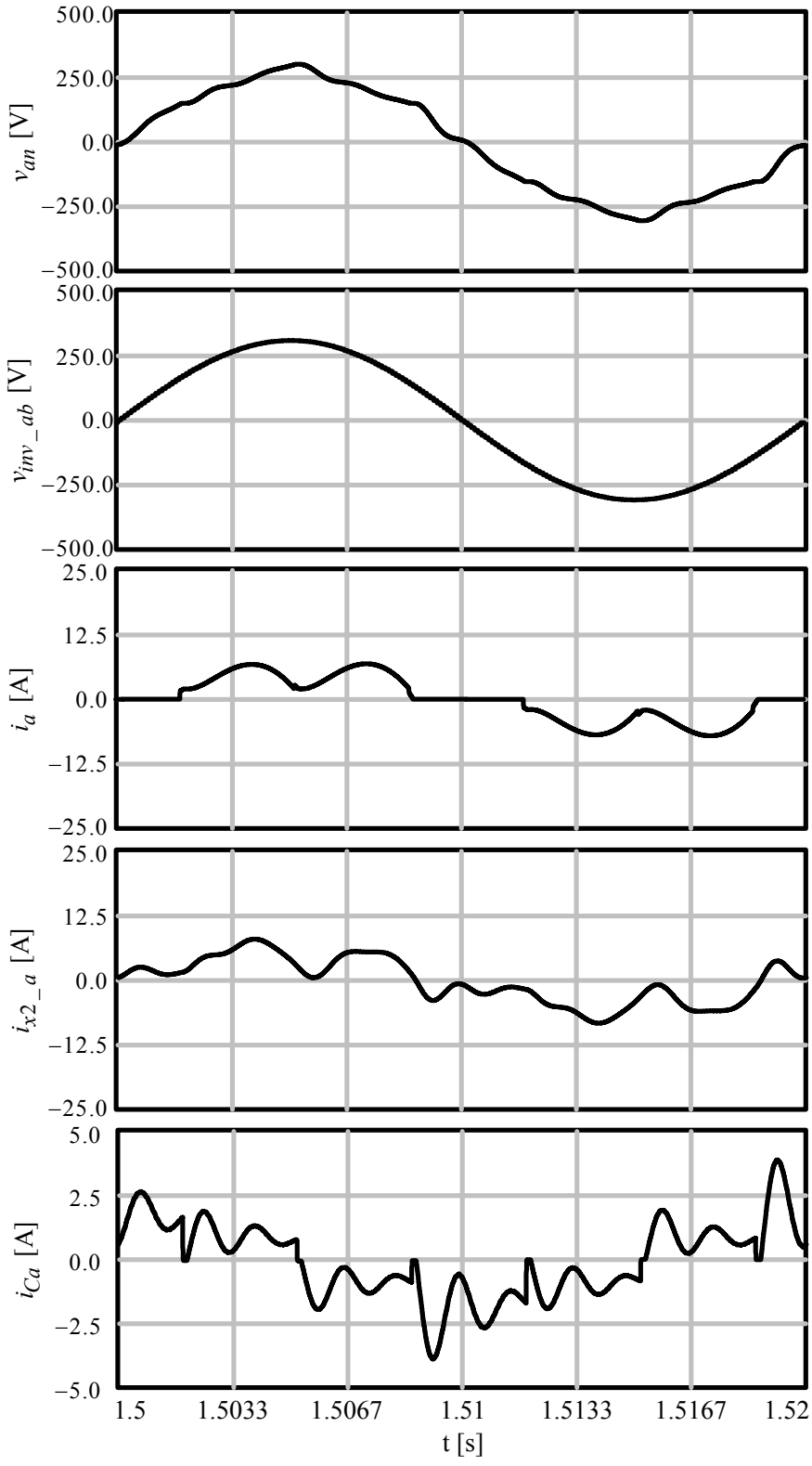

Figure 3.8 UPS line-to-neutral output voltage (v_{an}), line-to-line inverter voltage (v_{inv}), load current (i_a), transformer secondary current (i_{xa2}), output capacitor current (i_{Ca}) for open-loop controlled operation with balanced nonlinear load.

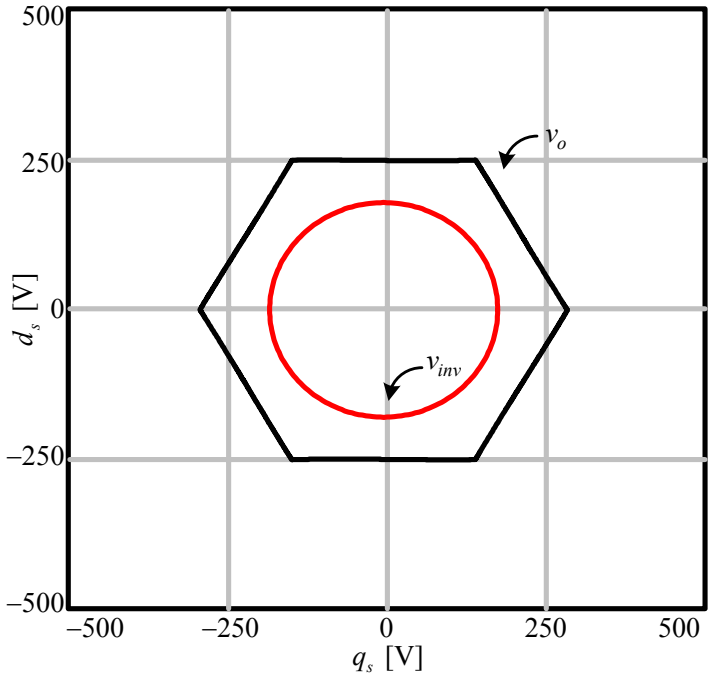

Figure 3.9 Stationary frame vector representation of the output voltages (v_o) and inverter reference voltages (v_{inv}) in complex coordinates for open-loop controlled operation with balanced nonlinear load.

3.4.2 UPS Output Performance Under Single-Phase Unbalanced Nonlinear Load

Open-loop controlled steady-state operation under single-phase unbalanced nonlinear load with 1.3 kVA is simulated via Simplorer. One terminal of the three-phase nonlinear load is open-circuited and the other two form the load terminals. The load terminals are connected to the line-to-neutral terminals of the UPS output. Thus, single-phase unbalanced load connection is configured. The resulting waveforms are reported in the following. The three-phase output voltages and the load current for one phase are shown in Figure 3.10. The loaded phase output voltage (v_{an}) is the most distorted phase and it has a THD value of 5.2% and the load current crest factor is 2.55. During the interval that the load current is drawn from the associated phase of the UPS, the DC bus voltage of the load is seen on the loaded phase of the UPS. Thus, the top segment of the loaded phase voltage v_{an} has almost constant voltage value. The harmonics spectrum shown in Figure 3.11 contains 3rd, 5th, 7th, 9th, and

11^{th} harmonics dominantly. The output voltage regulation is approximately 7.2% for the loaded UPS output phase voltage. One phase UPS output voltage, one of three line-to-line inverter voltages, load current, transformer secondary current, and capacitor current waveforms are given in Figure 3.12. Low frequency harmonics of the load current circulate through the capacitors and transformer. The harmonic current passes through the capacitor and considerably distorts the output voltages. Illustrating the control variables in the stationary frame complex coordinates, Figure 3.13 shows that the inverter output voltage vector traces an ideal circular route while the UPS output voltage vector is pressed at two edges which correspond to the instants that the load current pulses are drawn from the UPS.

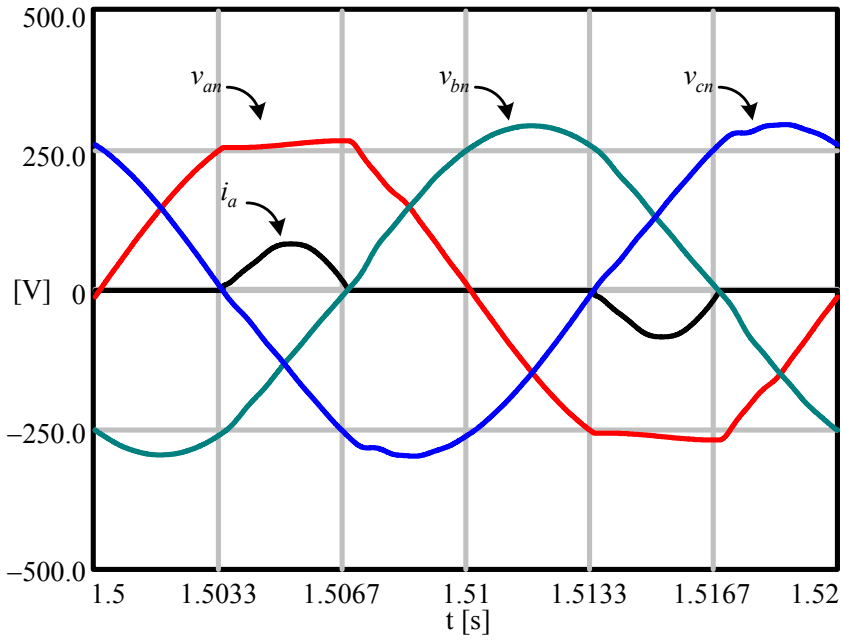

Figure 3.10 UPS output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current (i_a) (×10) for open-loop controlled operation with line-to-neutral connected nonlinear load.

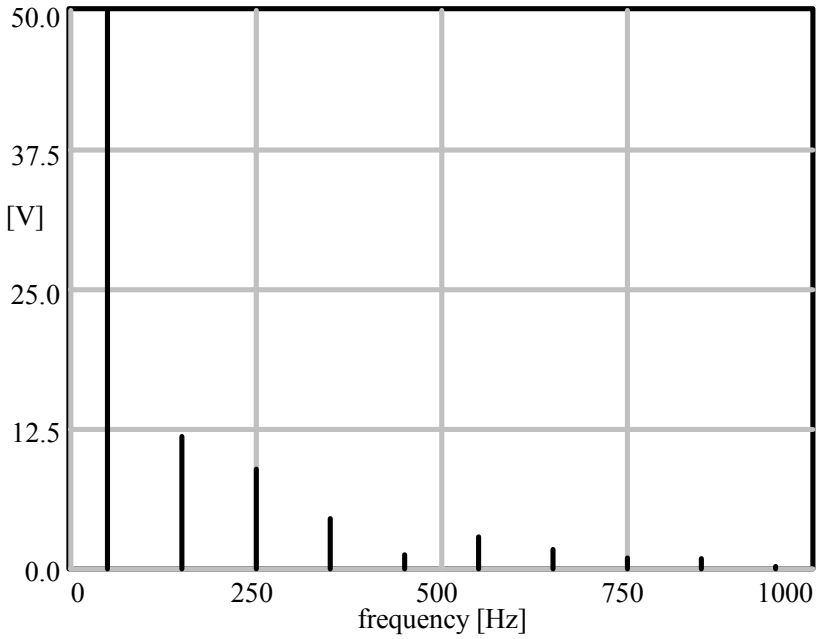

Figure 3.11 Harmonic spectrum of the line-to-neutral output voltage for open-loop controlled operation with line-to-neutral connected single-phase nonlinear load.

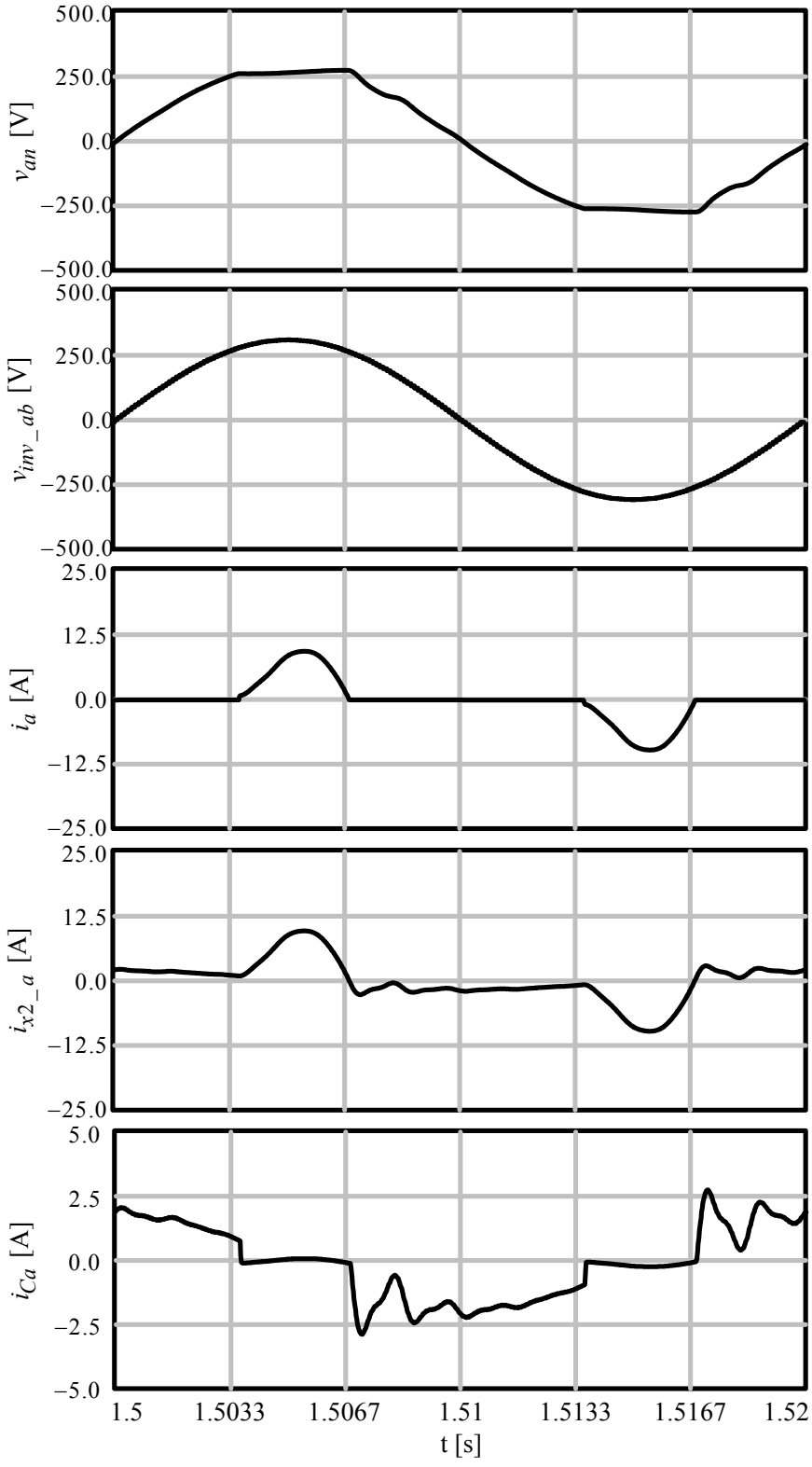

Figure 3.12 UPS line-to-neutral output voltage (v_{an}), line-to-line inverter voltage (v_{inv}), load current (i_a), transformer secondary current (i_{xa2}), output capacitor current (i_{Ca}) for open-loop controlled operation with line-to-neutral connected nonlinear load.

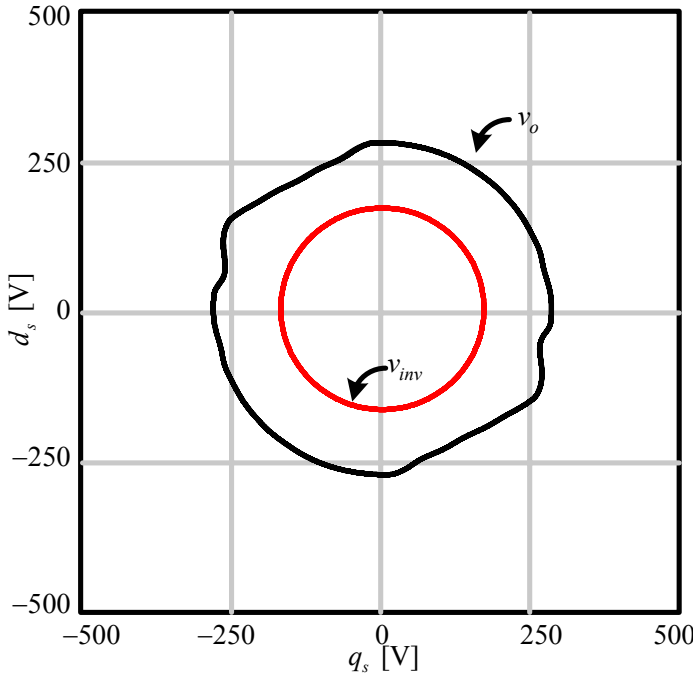

Figure 3.13 Stationary frame vector representation of the output voltages (v_o) and inverter reference voltages (v_{inv}) in complex coordinates for open-loop controlled operation with line-to-neutral connected single-phase nonlinear load.

3.4.3 UPS Output Voltage Under Line-to-line Unbalanced Nonlinear Load

Open-loop controlled steady-state operation under line-to-line unbalanced nonlinear load with 3 kVA is simulated via Simplorer. One terminal of the three-phase nonlinear load is open-circuited and the other two form the load terminals. The load terminals are connected to the line-to-line terminals of the UPS output. Thus, line-to-line unbalanced load connection is configured. The resistor load on the DC bus side of the nonlinear load is adjusted so that the 3 kVA rating is obtained. The resulting waveforms are reported in the following. The three-phase output voltages and the load current for one phase are shown in Figure 3.14. The output voltages of the loaded phases deviate from sine wave and approach triangular shape (similar to the balanced load case) due to nonlinear loading and the steady-state simulation data which is executed in DayPostprocessor reveals that the output voltage THD is 7.38% and the load current crest factor is 2.2. The harmonics spectrum shown in Figure 3.15

contains 3^{rd}, 5^{th}, 7^{th}, 9^{th}, and 11^{th} harmonics dominantly. The output voltage regulation approaches 11% for the loaded UPS output phase voltages. One phase UPS output voltage, one of three line-to-line inverter voltages, load current, transformer secondary current, and capacitor current waveforms are given in Figure 3.16. Low frequency harmonics of the load current circulate through the capacitors and transformer. The harmonic current passing through the capacitor considerably distorts the output voltages especially at low frequencies. Illustrating the control variables in the stationary complex coordinates, as Figure 3.17 shows, the inverter output voltage traces an ideal circular route while the UPS output voltage vector is pressed at two edges which corresponds to the instants when the load current pulses are drawn from the UPS.

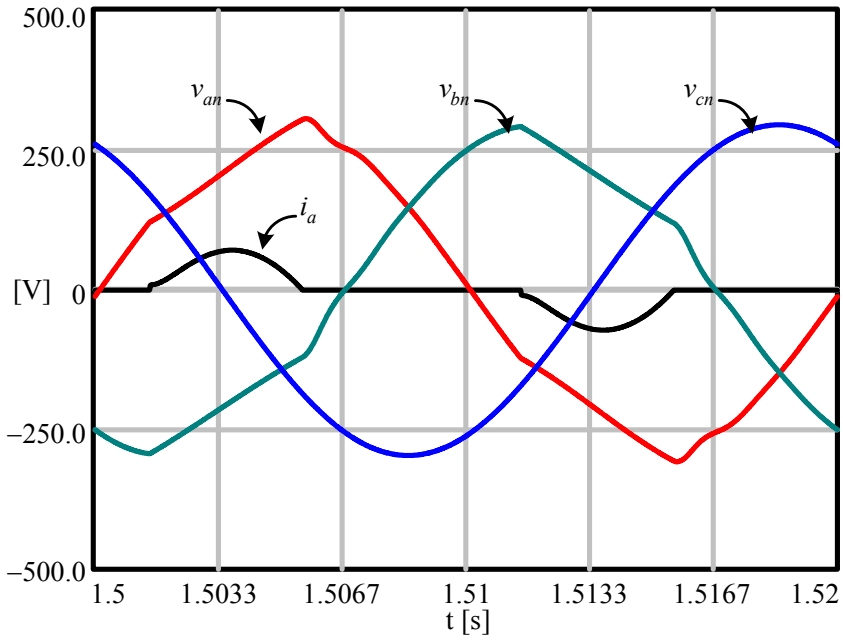

Figure 3.14 UPS output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current (i_a) (×10) for open-loop controlled operation with line-to-line connected nonlinear load.

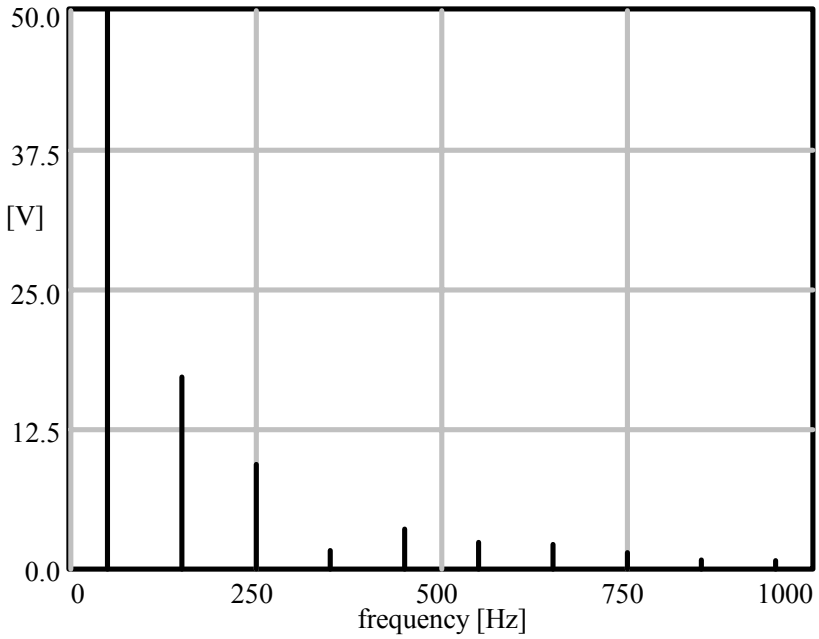

Figure 3.15 Harmonic spectrum of the line-to-neutral output voltage for open-loop controlled operation with line-to-line connected single-phase nonlinear load.

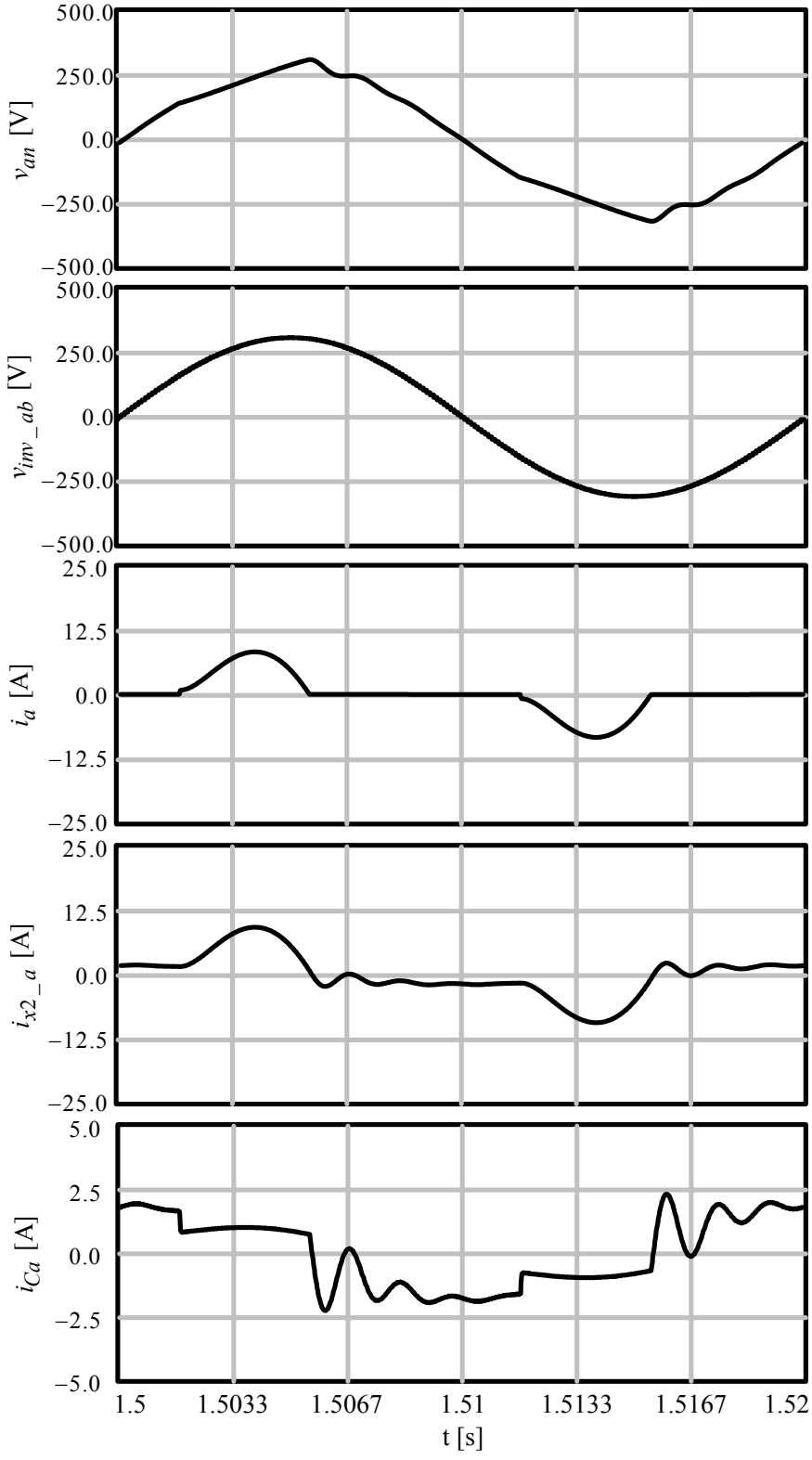

Figure 3.16 UPS line-to-neutral output voltage (v_{an}), line-to-line inverter voltage (v_{inv}), load current (i_a), transformer secondary current (i_{xa2}), output capacitor current (i_{Ca}) for open-loop controlled operation with line-to-line connected nonlinear load.

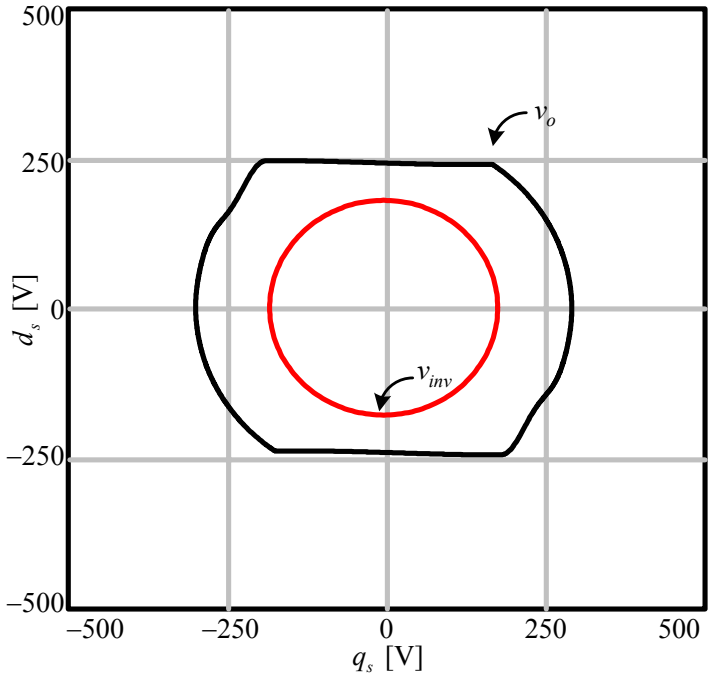

Figure 3.17 Stationary frame vector representation of the output voltages (v_o) and inverter reference voltages (v_{inv}) in complex coordinates for open-loop controlled operation with line-to-line connected single-phase nonlinear load.

3.5 Repetitive Controller Design for UPS Output Voltage Control

In this section a repetitive controller will be designed for the purpose of controlling the output voltages of the three-phase isolation transformer based UPS. The repetitive controller to be utilized is the structure reported in Chapter 2, Figure 2.12. Since the proposed controller includes complementary elements to the basic repetitive controller, the design procedure involves optimization of these elements as well as the repetitive controller itself. For this purpose the design procedure will be trial and error based and the design procedure will consist of steps that are followed according to the degree of vitality. The design is not a single pass design and at least two iterations are necessary for the optimization of the repetitive controller. The design will be carried by means of computer simulations. In the design, the steady-state nonlinear balanced rated load performance will be considered. Since this operating condition poses the worst case operating condition, it is a good candidate

for the trial and error based design. The design assumes the knowledge of passive elements which were discussed in Section 3.2 of this chapter. Also, the switching frequency of the inverter and the sampling frequency of the DSP must be given as inputs for the design to be pursued. The design procedure is summarized in Table 3.4.

The design procedure will be detailed via a numerical example, the 5 kVA rated UPS discussed in Section 3.2 of this chapter. The parameters of the passive elements to be utilized are listed in Table 3.3. In the 5 kVA UPS considered the LC filter resonant frequency is 750 Hz and the output frequency is 50 Hz. The switching (or PWM) frequency for this application is selected as 20 kHz. However, to show that the repetitive controller can perform well at lower frequencies, the repetitive control loop is sampled at 10 kHz. As important parts of the complementary control units, the proportional controller which works on the output voltage error and the active damping controller which works on the capacitor feedback current are updated at the carrier frequency for the purpose of high dynamic response and load disturbance rejection. Therefore, the PWM, active damping and proportional control loops are executed every 50μs, while the repetitive controller and the voltage feedforward are executed every 100μs. But both loops are synchronized. In the following the steps of the design will be detailed.

Table 3. 4 The design procedure of the repetitive controller

Step #	Operation	
1	Cancel the resonant filter peak of LC filter.	$S(z)$
2	Compensate total delay in the system.	n_d
3	Choose the maximum applicable repetitive controller gain (K_{rc}<1). This gain will be updated in step#6.	K_{rc}
4	Choose the best performing filter in the integrator structure.	$Q(z)$
5	Apply the active damping term.	K_{ad}
6	Update (increase) the repetitive controller gain of step#3.	K_{rc}
7	Apply gain to output voltage proportional controller.	K_{pv}

1. The resonant peak of the LC filter degrades the dynamic performance of the controller unless a correction mechanism exists in the closed-loop system. The stability analysis in Chapter 2 revealed that the system stability is strongly dependent on the gain characteristics of the controlled plant (the capacitor output voltage to inverter input voltage gain of the UPS). When the repetitive controller is used alone, the repetitive controller gain K_{rc} should be chosen small in order not to excite the resonant frequency harmonics of the LC filter. With such small gain values, the repetitive controller dynamic performance degrades significantly and the transients can last several seconds. For this reason, the gain characteristic of the UPS should be modified in order to achieve stable operation with reasonably high repetitive controller gain which provides fast dynamic response.

In order to obtain the capacitor output voltage to inverter input voltage gain characteristic of the UPS (per phase) prototype in the laboratory, the inverter was used to generate voltages at various frequencies (from 50 Hz to 800 Hz) and the magnitude of UPS output voltage is measured. From the experimental data collected, the gain characteristic shown in Figure 3.18 is obtained. The plant has a resonant peak at 750 Hz and the second order transfer function given in (2.8) can be used for the plant gain characteristic.

In the previous chapter, the resonant peak suppressing filter, *S(z)*, was designed with a gain characteristic with sharp cut-off frequency for the cancellation of the resonant peak of the LC filter which has a transfer function as given in (2.8). The *S(z)* filter structure was designed as 30th order FIR low-pass filter. The gains given in Table 2.14 are utilized in the filter structure. With such a delayless and noncausal filtering structure no additional delay is included in the closed-loop system. The same *S(z)* filter structure will be used in the simulations.

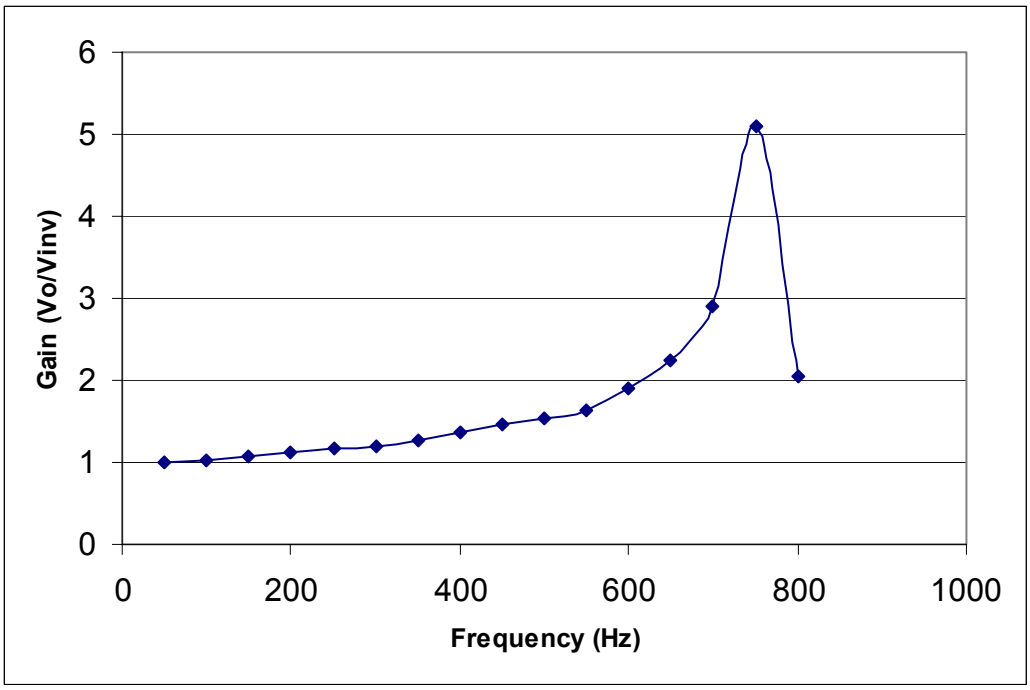

Figure 3.18 The experimental capacitor output voltage to inverter input voltage gain characteristic of the UPS.

2. The delays in the overall system (calculation time of DSP, measurement circuit delay, PWM delay of inverter, and LC filter) are summed in order to find the total system delay. With 10 kHz sampling rate calculation time of the DSP is 100 μs. The measurement delay is 90 μs with measurement transformers. 20 kHz switching frequency yields 25 μs PWM delay. As discussed in Chapter 2, the delay of the LC

filter at the resonant frequency is approximately 300 μs and this value is chosen as the time delay of the LC filter. Overall, the total delay is 515 μs (100μs +90 μs+25 μs+300 μs) and this value corresponds to approximately 5 cycles of the sampling frequency (repetitive controller update rate).

3. With perfect cancellation of the LC resonant peak and phase delay of the system, the maximum achievable gain is one. Practically the repetitive controller gain (K_{rc}) is chosen less than one to insure system stability. By considering the scaling ratio of the transformer (line-to-line input to line-to-line output), $\sqrt{3}$, the maximum achievable repetitive controller gain is $(1/\sqrt{3}) = 0.577$. To ensure stability the gain is chosen as 0.5. This repetitive gain value is an initial value for the iterative controller design and will be updated in the later steps of the design procedure.

4. The steady-state performance of the controller is determined by the integral limiting filter *Q(z)* of the repetitive controller structure. For several choices of *Q(z),* performance of the UPS system will be evaluated by means of computer simulations. For scalar *Q(z)* three values, 0.9, 0.95, and 0.98 are considered. For low pass filter type *Q(z)* two FIR filter structures with different cut-off frequencies are considered and the performance of the controller is investigated. For the given design defined in the above steps and *Q(z)* of this section, computer simulations have been run and the steady-state balanced rated nonlinear load UPS performance results are summarized in Table 3.5. In the table, the voltage feedforward open-loop controlled UPS performance data is also given for the purpose of comparison and illustration of performance improvement due to the repetitive controller.

Table 3.5. Steady-state performance data of repetitive controlled UPS system

Control method		THD_v (%)	CF	VR (%)
Open-loop controlled		6.71	1.26	14.5
Q(z) of repetitive controller (K_{rc}=0.5)	*Q(z)*=0.9	2.28	2.18	1.8
	Q(z)=0.95	1.72	2.38	0.9
	Q(z)=0.98	1.45	2.5	0.3
	$Q(z)= 0.25\cdot z^{-1}+0.5+0.25\cdot z$	1.49	2.7	0.0
	$Q(z)= -0.0127\cdot z^{-2}+0.14578\cdot z^{-1}+0.7338+0.14578\cdot z-0.0127\cdot z^{2}$	1.59	2.65	0.0

With the choice of *Q(z)* as 0.9, the output voltage distortion is reduced as seen in Figure 3.19. The output voltages are closer to sine wave than in the open-loop case (Figure 3.6). Output voltage THD value is brought to 2.28% from the open-loop value of 6.71%. This value is acceptable for many high performance UPS applications. Load current harmonics at the controlled frequencies (between the fundamental and the resonant frequency) are forced to flow through the filter inductors and transformer which form a very low impedance path to the harmonic currents. Decrease in the output impedance of UPS causes the nonlinear load current harmonics to increase. Consequently, the load current crest factor increases from 1.26 at open-loop to 2.18 at closed-loop operation. Harmonics are decreased but low frequency harmonics (5^{th} and 7^{th}) are still high due to low repetitive controller gain as seen in the harmonic spectrum of one phase output voltage in Figure 3.20. The output voltage vector and inverter reference vector are illustrated in Figure 3.21 in complex coordinates. Sharp corners of the output voltage vector are eliminated and the vector has a shape closer to a circle. The inverter voltage vector, on the other hand, is deviated from the circle in order to provide harmonics to the load. Output voltage regulation is improved to 1.8 %. However in most of the applications output voltage regulation is demanded to be less than 1%.

Increasing the integral limiting filter gain from 0.9 to higher values results in overall steady-state performance improvement. For 0.95 and 0.98 the tests are repeated as above. While the performance indices for both are reported in Table 3.5, the waveforms associated for the 0.95 case are not shown. With $Q(z)$=0.95 output voltage THD is 1.72% and the regulation is 0.9%. The regulation is still close to 1% although THD is reduced to reasonably low value. As a final design point, the 0.98 case is discussed in detail.

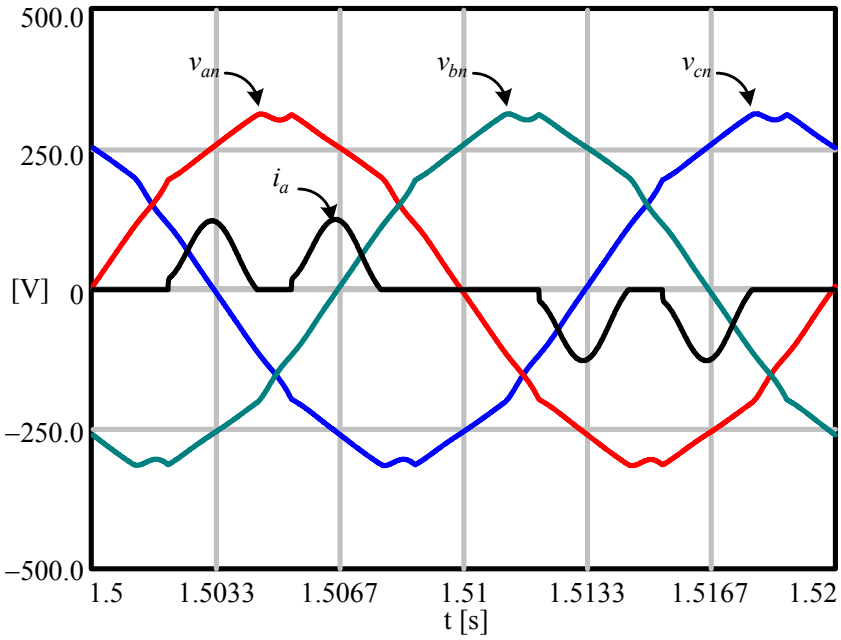

Figure 3.19 UPS output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current (i_a) (×10) for repetitive control with $Q(z)$=0.9 under operation with balanced nonlinear load.

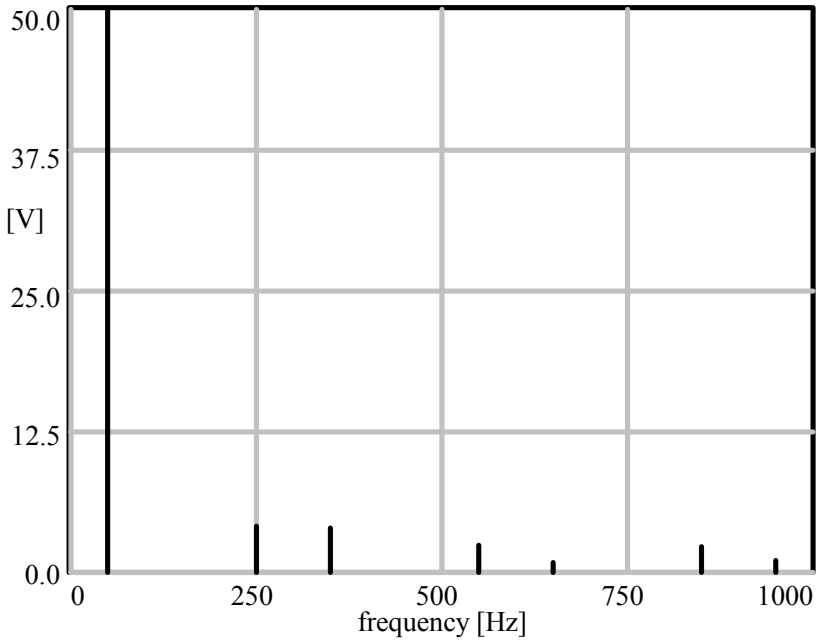

Figure 3.20 Harmonic spectrum of the line-to-neutral output voltage for repetitive control with *Q(z)*=0.9.

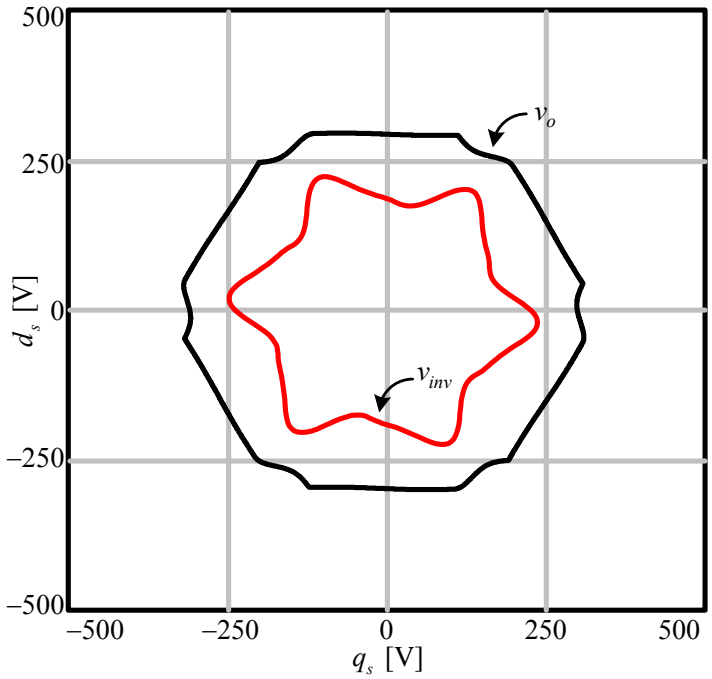

Figure 3.21 Stationary frame vector representation of the output voltages (v_o) and inverter reference voltages (v_{inv}) in complex coordinates for repetitive control with *Q(z)*=0.9.

For *Q(z)* of 0.98, the output voltage THD is observed as 1.45% which is smaller than THD value defined for high performance UPSs. The load current CF is 2.5 for this case. Also the output voltage regulation is at 0.3% which is less than the defined limits for state of the art UPS systems. As seen in Figure 3.22 output voltages are almost sine wave and load current is more peaky due to increase in the load current harmonic content. Harmonics are further suppressed as seen in the harmonic spectrum given in Figure 3.23. Figure 3.24 reveals that inverter generates more harmonic voltages and creates harmonic currents to further suppress output voltage harmonics. The 0.98 *Q(z)* value provides a practically optimum scalar gain value as lower gain values result in performance loss and higher gains result in instability.

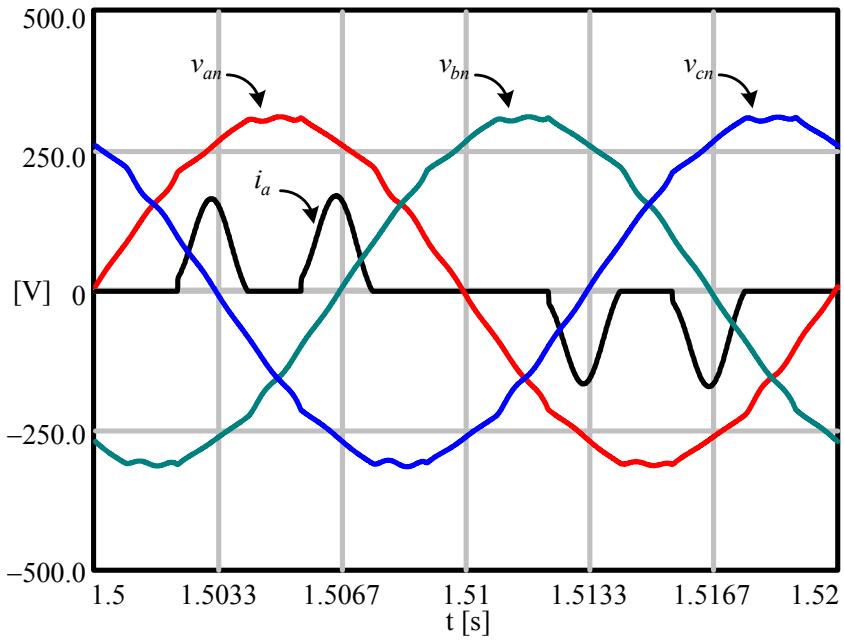

Figure 3.22 UPS output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current (i_a) (×10) for repetitive control with *Q(z)*=0.98 under operation with balanced nonlinear load.

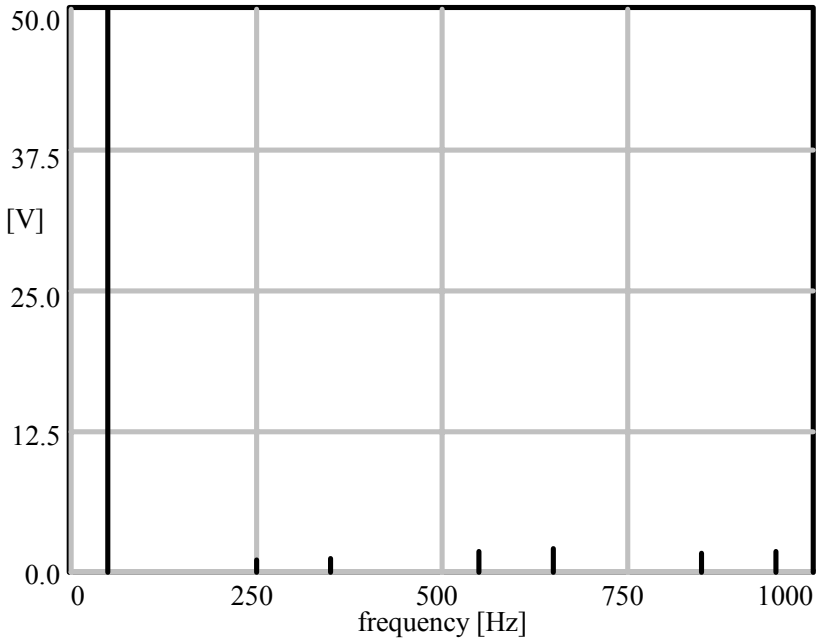

Figure 3.23 Harmonic spectrum of the line-to-neutral output voltage for repetitive control with *Q(z)*=0.98.

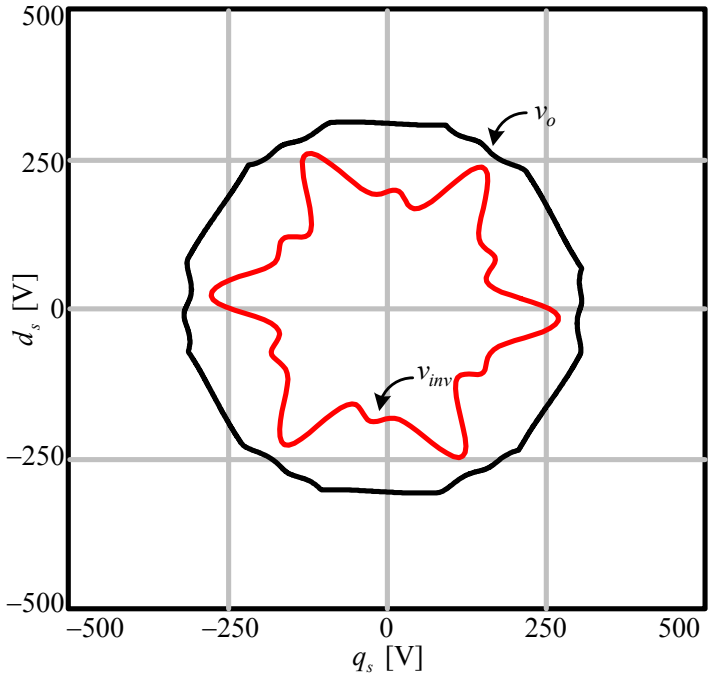

Figure 3.24 Stationary frame vector representation of the output voltages (v_o) and inverter reference voltages (v_{inv}) in complex coordinates for repetitive control with *Q(z)*=0.98.

Instead of scalar *Q(z)* choosing a low-pass filter, repetitive controller low frequency gain becomes substantial while the high frequency gain decreases. This leads to output voltage harmonic spectrum with reduced low frequency content while near the resonant frequency the performance is limited. Also, the positive effect of low-pass filter structure can be seen on the regulation of the output voltages.

Two low-pass filter structures are evaluated in the repetitive controller design study. For $Q(z)=0.25z^{-1}+0.5+0.25z$ FIR filter structure, the output voltages and one phase load current are given in Figure 3.25. The filter is delayless and noncausal as the *S(z)* filter. *Q(z)* has nearly unity gain at the fundamental frequency which leads to almost infinite controller gain. So at the fundamental frequency, output voltage regulation is perfect (0.0%). However the integrator gain decreases at high frequencies and the high frequency harmonics which are close to the resonant frequency of the UPS are weakly suppressed. As seen in Figure 3.26 low frequency harmonics (5^{th} and 7^{th} harmonics) are perfectly suppressed. But harmonics close to resonant frequency are still high. For this type of *Q(z)* output voltage THD is 1.46 % and the load current crest factor is 2.7 which indicates the UPS approaches an ideal voltage source. The output voltage vector of UPS and inverter voltage vector are given in Figure 3.27. The second order low-pass filter tested has resulted in similar performance to the first order filter. Therefore, the performance indices are reported in Table 3.5 but the waveforms are not shown.

Comparing the scalar and low-pass integral limiting filters, the scalar *Q(z)* of 0.98 exhibits satisfactory performance at steady-state (low output voltage regulation and low THD_V) and has implementation simplicity. Therefore, this *Q(z)* will be utilized in the repetitive controller structure from here on. Thus, with the design of *Q(z)* completed, the design procedure continues with the following steps.

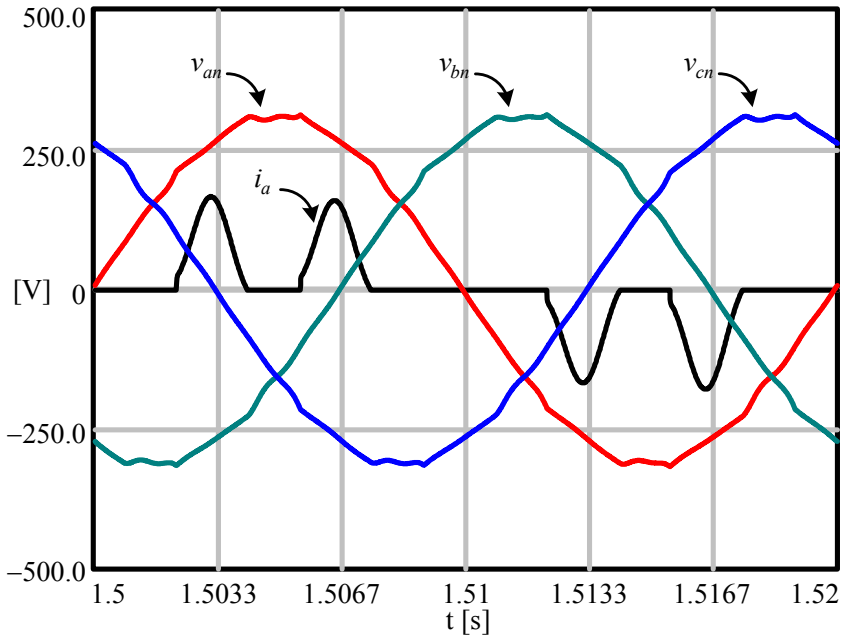

Figure 3.25 UPS output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current (i_a) (×10) for repetitive control with $Q(z)= 0.25z^{-1}+0.5+0.25z$ under operation with balanced nonlinear load.

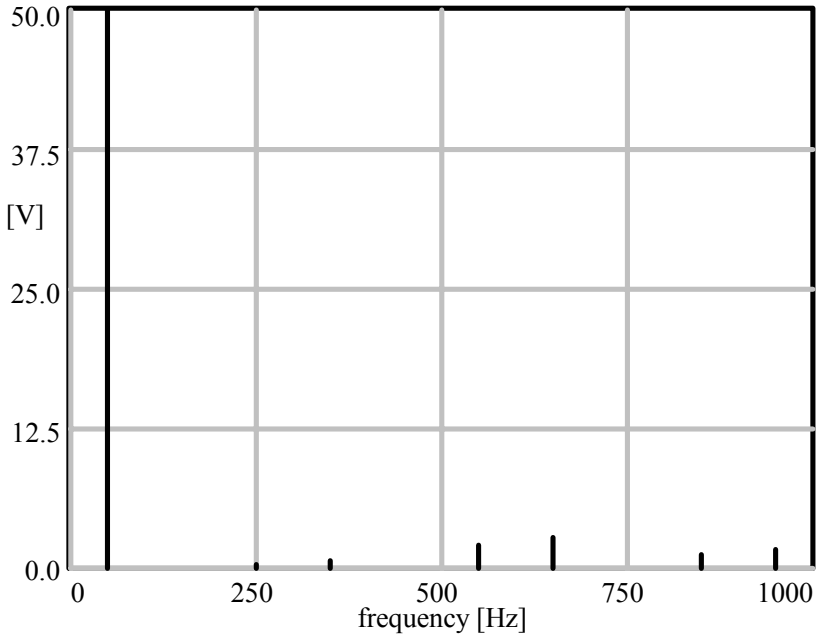

Figure 3.26 Harmonic spectrum of the line-to-neutral output voltage for repetitive control with $Q(z)= 0.25z^{-1}+0.5+0.25z$.

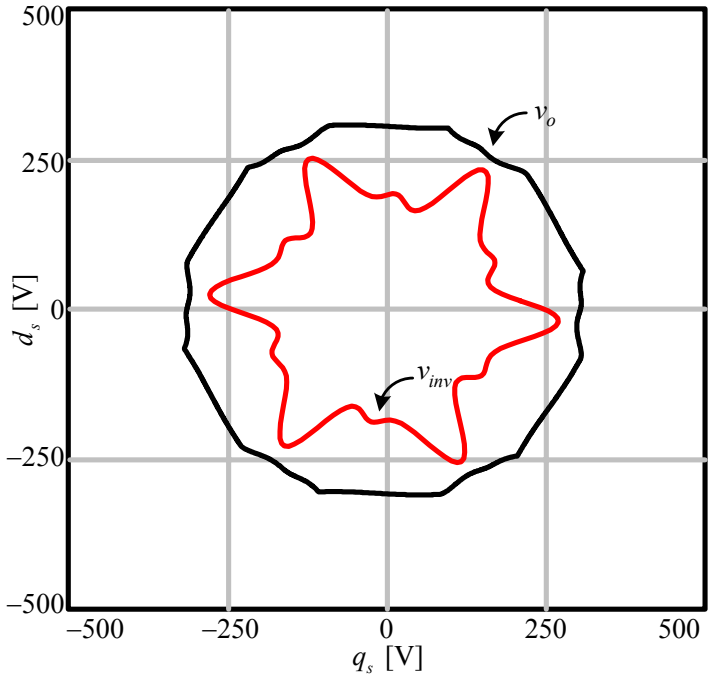

Figure 3.27 Stationary frame vector representation of the output voltages (v_o) and inverter reference voltages (v_{inv}) in complex coordinates for repetitive control with $Q(z)= 0.25z^{-1}+0.5+0.25z$.

5. Capacitor current feedback which provides active damping to the inherently underdamped UPS system is employed in the control structure. Since the capacitor current is a portion of output voltage derivative, derivative action is added in the controller structure to provide active damping. Thus the controller high frequency gain is increased and consequently the steady-state performance involving high frequency harmonics and dynamic response are partially improved. Due to the delays in the UPS system, the capacitor current gain can not be increased beyond the value of 15 in the simulations. Simulating the controller performance with scalar q of 0.98 and adding the capacitor current feedback the performance results are obtained and shown in Table 3.6. Addition of capacitor current feedback reduces output voltage THD value to 1.14 % and other performance indices remain the same. This is mainly achieved due to the higher frequency range harmonic suppression capability of the active damping loop.

6. With the capacitor current feedback loop closed, the system is more damped and the repetitive controller gain can be increased for faster response and better harmonic rejection. Thus the repetitive controller gain is increased from 0.5 to 0.57 and the simulations were obtained. The results are shown in Table 3.6. According to the table, the steady-state performance improvement is marginal. In this case the output voltage THD_V decreases from the previous value of 1.14% to 1.08 %, both of which are highly acceptable compared to the commercial standards.

7. In order to improve the dynamic response of the controller, in addition to the capacitor current feedback based active damping loop, a voltage proportional loop should be added. With this controller added, the repetitive controller becomes a PI controller. However, the gain can not be made large due to the controller delay. In the simulations the gain could be increased to 0.8 and a compromise between the steady-state and dynamic performance (to be discussed in the later stages) could be obtained. For this case, in the simulation THD_V slightly increases to 1.18 %. However the steady-state performance of the UPS system is still satisfactory.

Table 3.6 Steady-state performance data of repetitive controlled UPS system

Control method		THD_V (%)	CF	VR (%)
$Q(z)$=0.98	K_{ad}=15 added	1.14	2.5	0.4
	K_{rc}=0.57 (increased)	1.08	2.53	0.3
	K_{pv}=0.8 added	1.18	2.55	0.29

This section provided a design procedure and the controller gains were tuned. The active damping and proportional control loops are added to the advantage of the system. The scalar $Q(z)$ of 0.98 has been found satisfactory. The repetitive control gain could be increased to a high value with the stabilizing effect of the active damping loop. Thus, a repetitive controller could be designed and preliminary test results could be obtained. With the design completed, the next section involves the steady-state and dynamic performance evaluation of the repetitive controlled system under balanced and unbalanced load operating conditions.

3.6 Steady-state Performance Evaluation of Repetitive Controller

In this section, the steady-state operating performance of the repetitive controlled UPS system will be investigated under balanced rated, single-phase unbalanced rated and line-to-line unbalanced rated nonlinear load. The controller structure is the same as the final structure obtained during the design stage, of which the parameters are listed in Table 3.6. In the following, first different loading cases will be investigated individually and then the results will be cumulatively shown in a table and discussed.

3.6.1 Balanced Nonlinear Load

Repetitive controlled steady-state operation under three-phase rated balanced nonlinear load is simulated. The output voltages of the repetitive controlled UPS and one-phase load current are given in Figure 3.28. The effect of the capacitor current feedback can be observed by comparing the harmonic spectrums given in Figure 2.23 and Figure 2.29. With the capacitor current feedback, the high frequency harmonics (17^{th} and 19^{th}) of the output voltages are suppressed more effectively. One phase UPS output voltage, one of three line-to-line inverter voltages, load current, transformer secondary current, and capacitor current waveforms are given in Figure 3.30. The figure shows that the load current flows through the transformer secondary windings and the capacitor current contains only high frequency harmonics.

In Figure 3.31, the inverter reference voltage vector, UPS output voltage vector, and also the vector, which is the summation of the repetitive controller output vector and feedforward voltage vector, are given in order to show the effect of capacitor current feedback and proportional controller. The correction signal of repetitive controller leads the total inverter voltage reference due to application delay of the proportional gain for output voltage error. Also the inverter voltage reference vector contains also high frequency harmonics due to capacitor current feedback while the vector generated by the repetitive controller traces a smoother route.

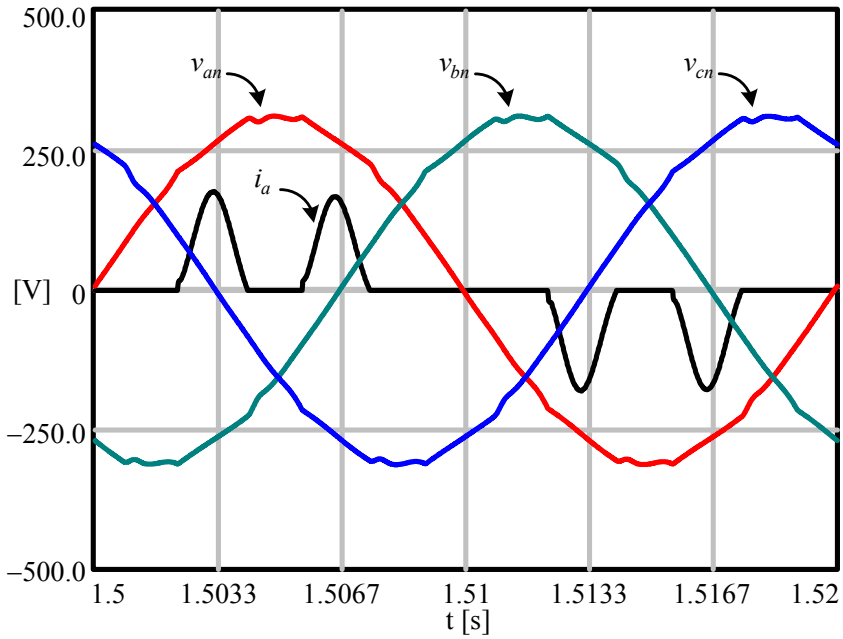

Figure 3.28 UPS output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current (i_a) (×10) for repetitive control with balanced nonlinear load.

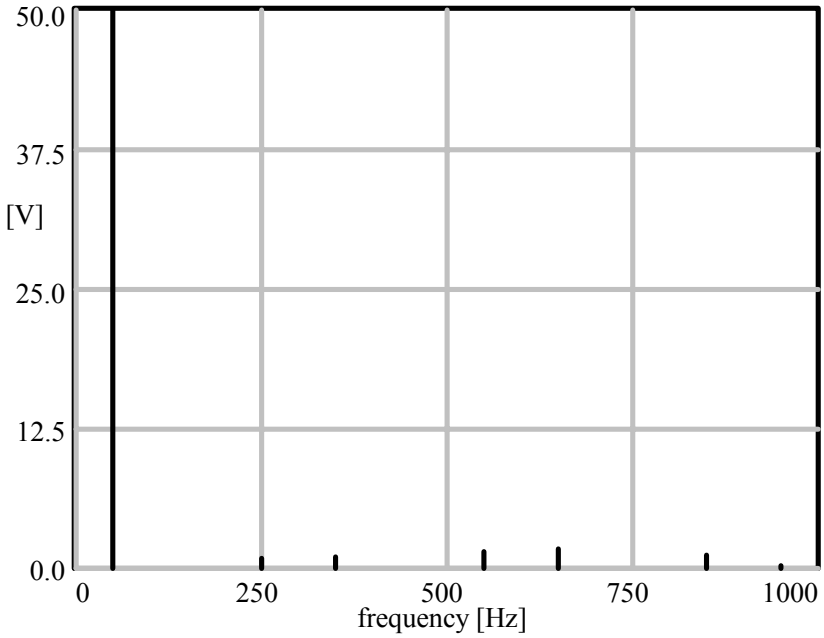

Figure 3.29 Harmonic spectrum of the line-to-neutral output voltage for repetitive control with balanced nonlinear load.

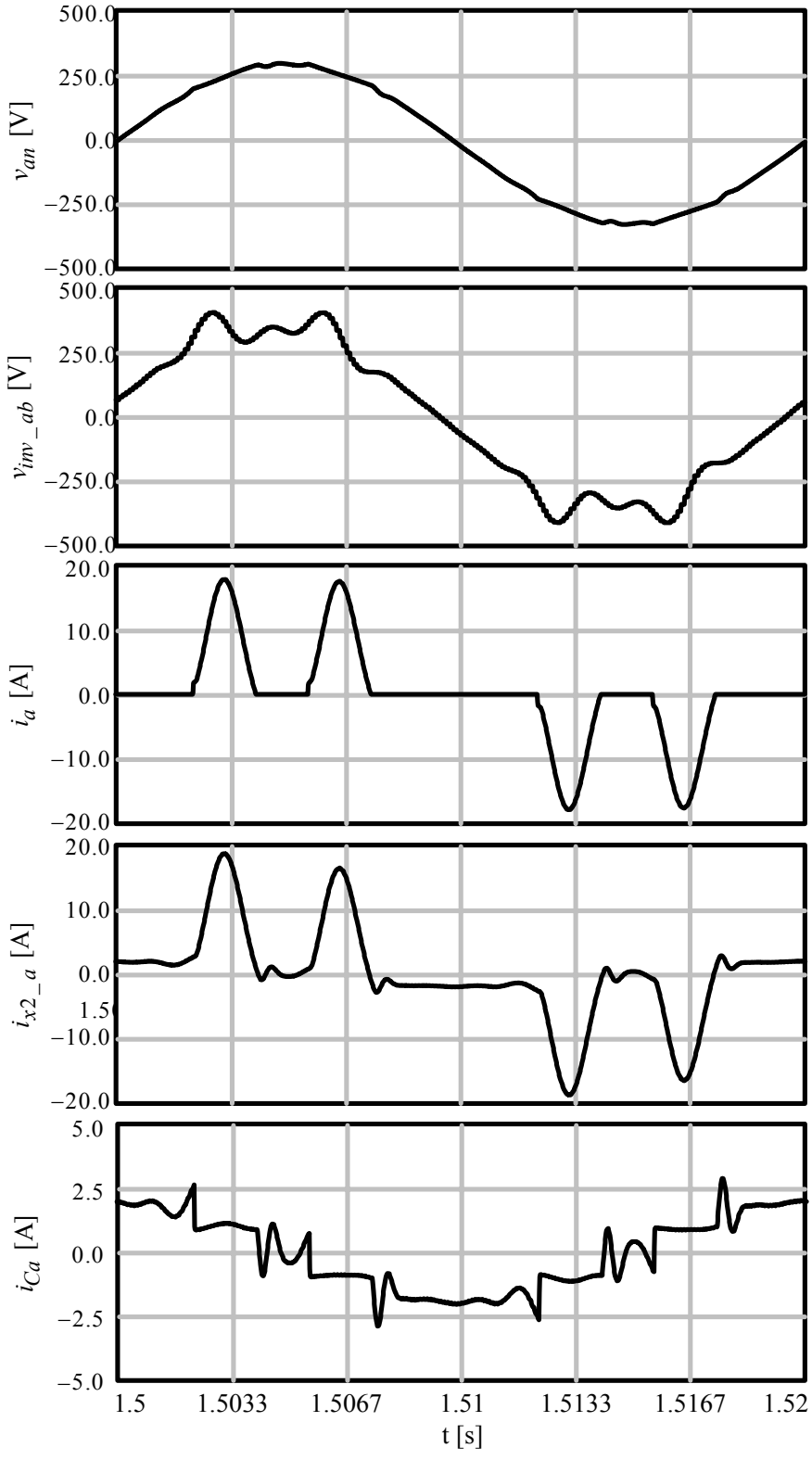

Figure 3.30 UPS line-to-neutral output voltage (v_{an}), line-to-line inverter voltage (v_{inv}), load current (i_a), transformer secondary current (i_{xa2}), output capacitor current (i_{Ca}) for repetitive control balanced nonlinear load.

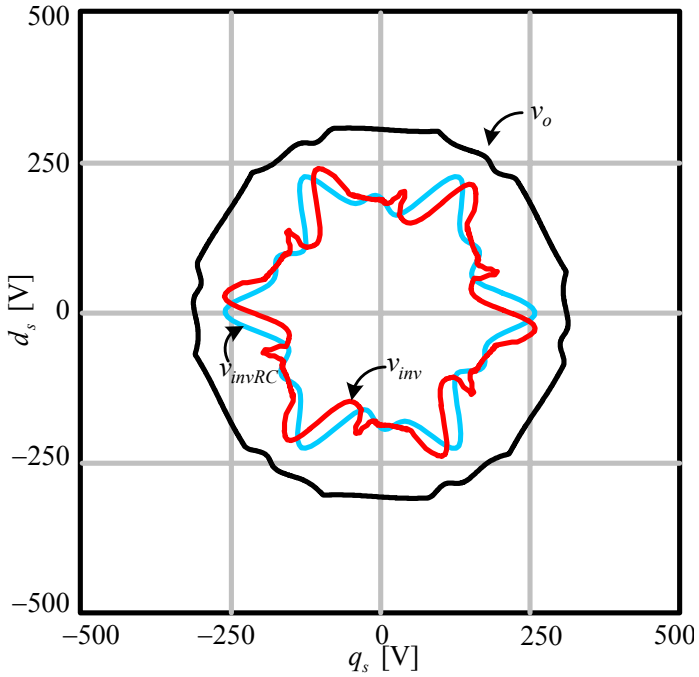

Figure 3.31 Stationary frame vector representation of the output voltages (v_o), inverter reference voltages (v_{inv}), and repetitive controller generated voltages (v_{invRC}) in complex coordinates for repetitive control with balanced nonlinear load.

The adaptation of controller to nonlinear loading is given in Figure 3.32. After the UPS is loaded by three-phase diode rectifier with RC load at the output, in several fundamental cycles the repetitive controller modifies the inverter voltage vector so that the output voltage vector traces a more circular route. In the diagram each box is for a fundamental cycle. This implies the transients are completely settled in 12 cycles from no-load to nonlinear balanced full-load.

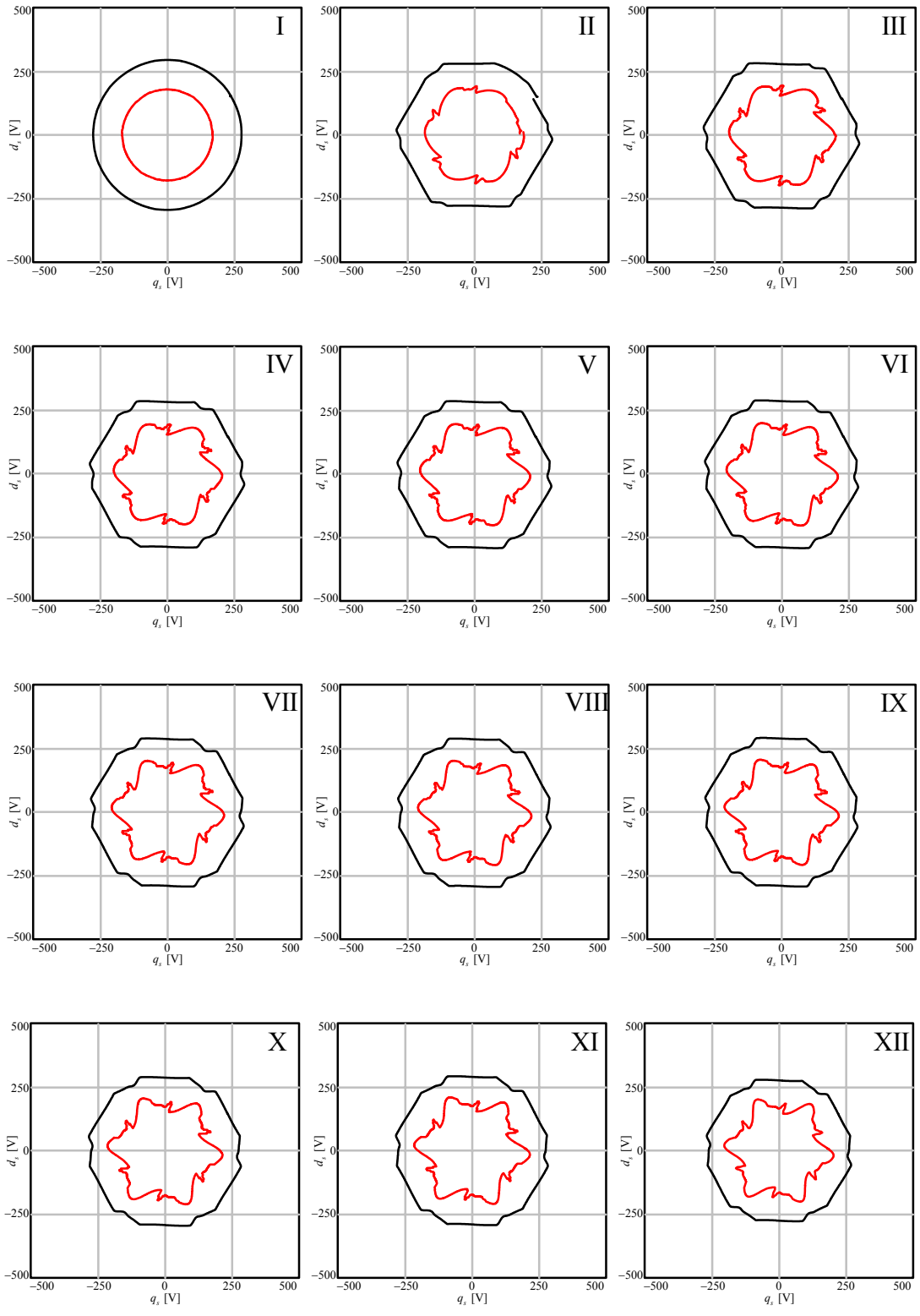

Figure 3.32 The adaptation stages of repetitive controller to nonlinear loading:

UPS output voltage vector (outer) and inverter voltage vector (inner).

3.6.2 Line-to-neutral Connected Single-Phase Nonlinear Load

Repetitive controlled steady-state operation under line-to-neutral connected single-phase rated unbalanced nonlinear load with 1.3 kVA is simulated via Simplorer. The output voltages of the repetitive controlled UPS and one-phase load current are given in Figure 3.33. The harmonic spectrum of Figure 3.34 shows that high amount of harmonics are suppressed. However the output voltages still include low order harmonics, which are zero sequence terms, and the leakage inductances of the transformer limit the zero sequence harmonic flow to the transformer so that the harmonics flow through the capacitors and distort the output voltage. One phase UPS output voltage, one of three line-to-line inverter voltages, load current, transformer secondary current, and capacitor current waveforms are given in Figure 3.35. The figure reveals that the load current flows through the transformer secondary windings and the capacitor current contains only high frequency harmonics when compared with Figure 3.12. In Figure 3.36, the inverter reference voltage vector and the UPS output voltage vector are given. In order to provide circular output voltage trajectory, the inverter reference voltage vector deviates from a circle and since single-phase loading is the case, the rate of distortion per 360^{o} is twice corresponding to two current pulses per fundamental cycle.

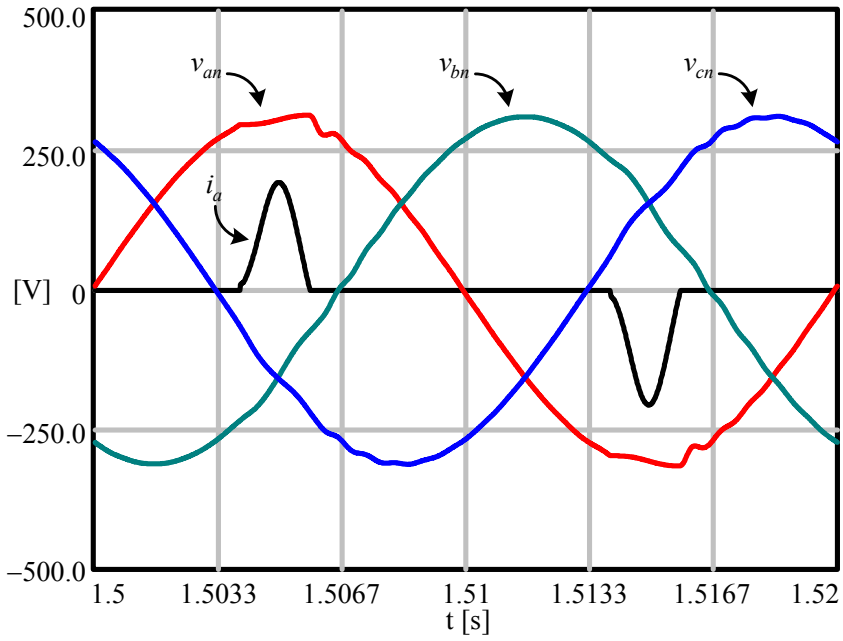

Figure 3.33 UPS output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current (i_a) (×10) for repetitive control with line-to-neutral connected single-phase nonlinear load.

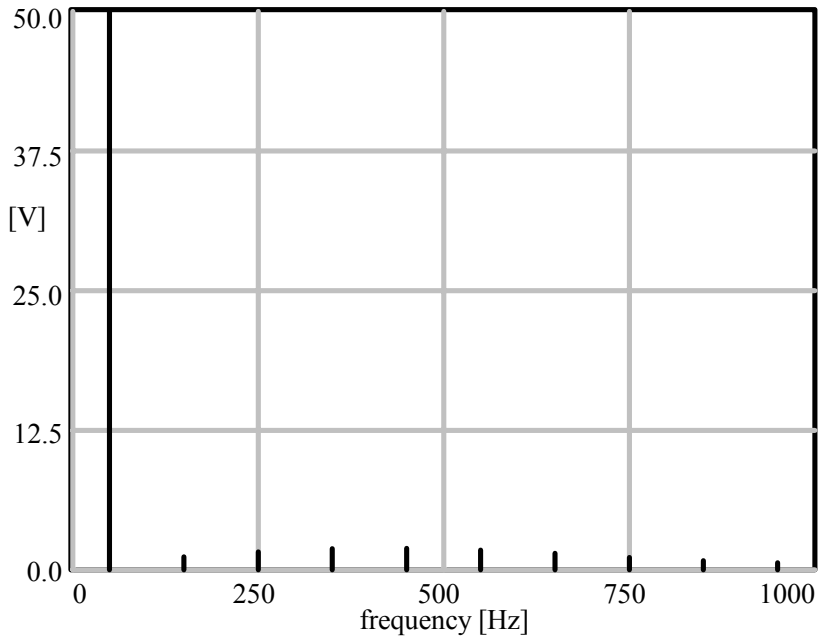

Figure 3.34 Harmonic spectrum of the line-to-neutral output voltage for repetitive control with line-to-neutral connected single-phase nonlinear load.

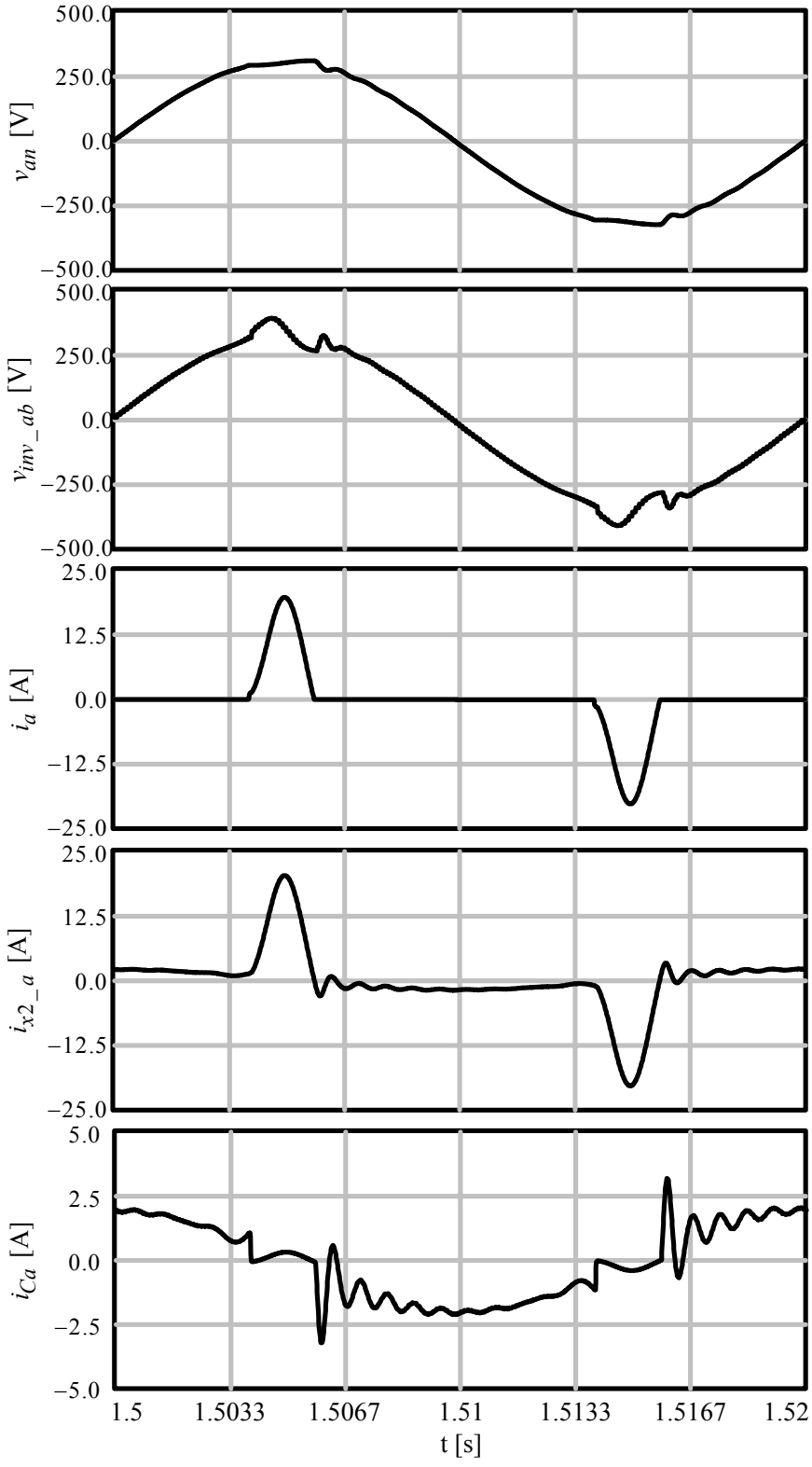

Figure 3.35 UPS line-to-neutral output voltage (v_{an}), line-to-line inverter voltage (v_{inv}), load current (i_a), transformer secondary current (i_{xa2}), output capacitor current (i_{Ca}) for repetitive control with line-to-neutral connected nonlinear load.

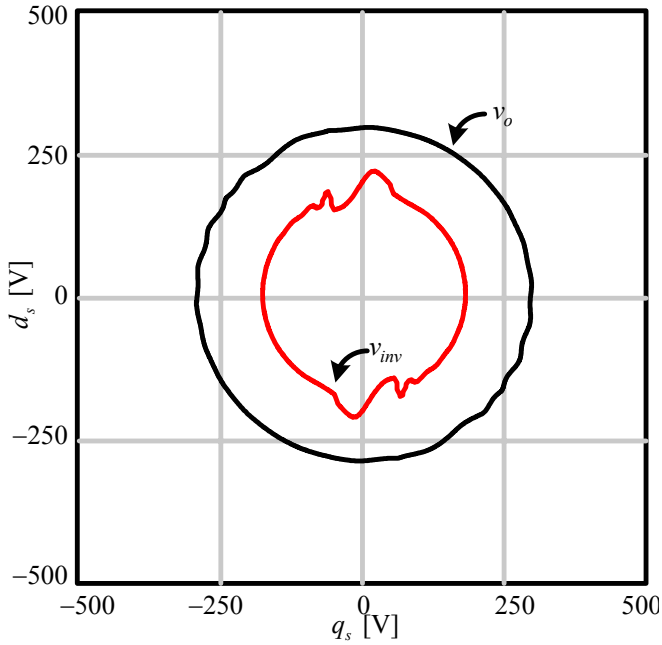

Figure 3.36 Stationary frame vector representation of the output voltages (v_o) and inverter reference voltages (v_{inv}) for repetitive control under line-to-neutral connected single-phase nonlinear loading.

3.6.3 Line-to-Line Connected Single-Phase Nonlinear Load

Repetitive controlled UPS steady-state operation under line-to-line connected single-phase rated unbalanced nonlinear load with 3 kVA is simulated via Simplorer. Since the line-to-line imbalance yields only negative sequence imbalance, the UPS output voltage harmonics can be suppressed more effectively with the repetitive controller compared to the line-to-neutral unbalance. The output voltages of the repetitive controlled UPS and one-phase load current are given in Figure 3.37. The harmonic spectrum of Figure 3.38 shows that harmonics are suppressed. One phase UPS output voltage, one of three line-to-line inverter voltages, load current, transformer secondary current, and capacitor current waveforms are given in Figure 3.39. The figure shows that the load current flows through the transformer secondary windings and the capacitor current contains only high frequency harmonics when compared with the Figure 3.16. In Figure 3.40, the inverter reference voltage vector and UPS output voltage vector are given. The phase difference of 30˚ between the output voltage vector and inverter reference vector can be observed from this figure.

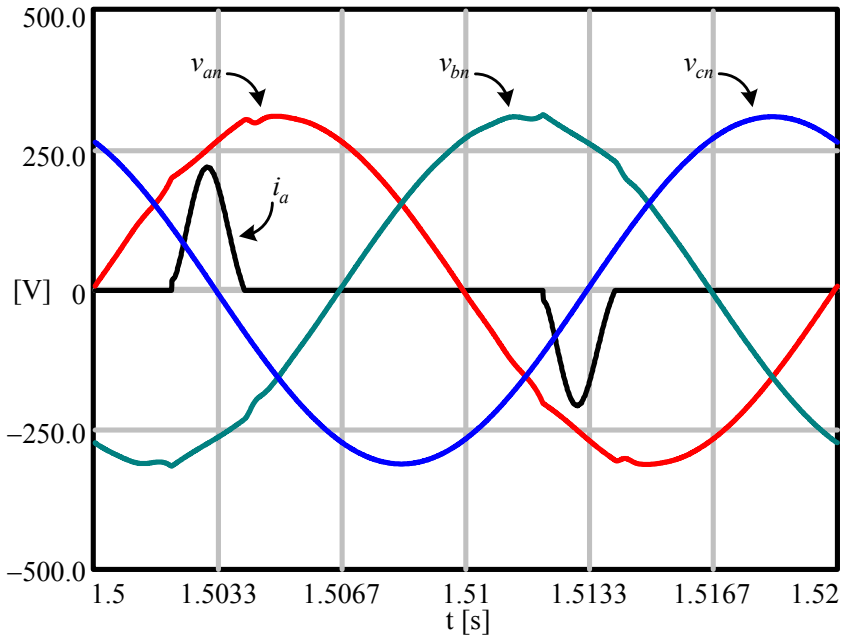

Figure 3.37 UPS output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current (i_a) (×10) for repetitive control at line-to-line connected single-phase nonlinear load.

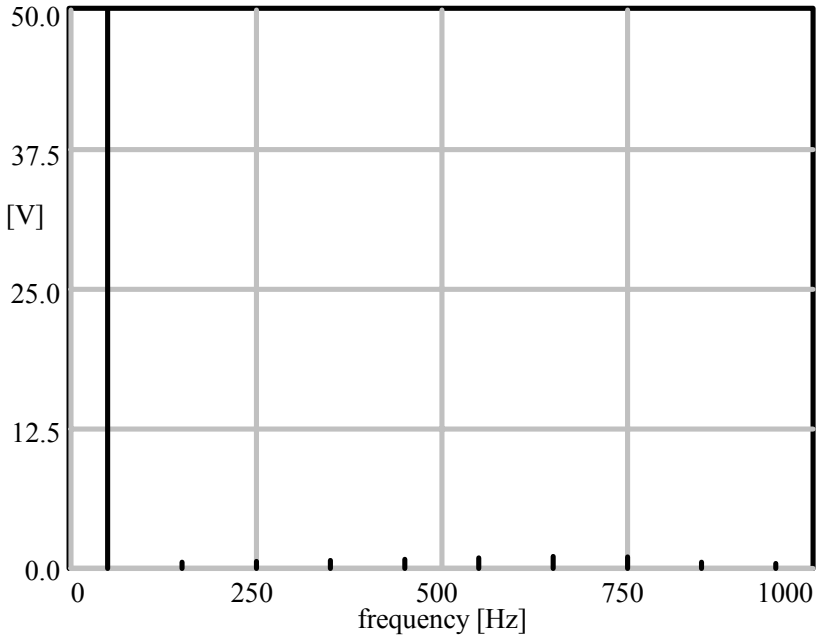

Figure 3.38 Harmonic spectrum of the line-to-neutral output voltage for repetitive control with line-to-line connected single-phase nonlinear load.

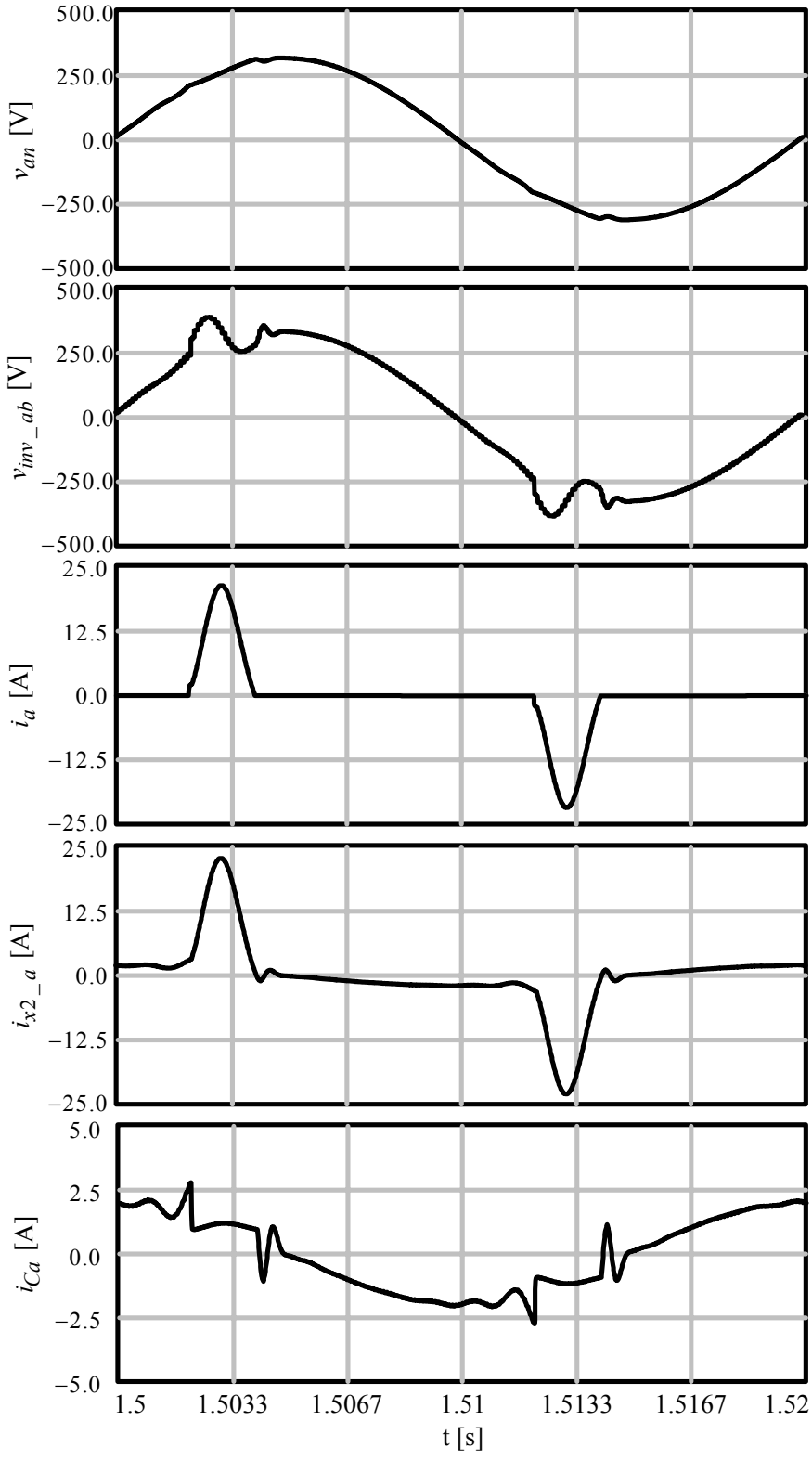

Figure 3.39 UPS line-to-neutral output voltage (v_{an}), line-to-line inverter voltage (v_{inv}), load current (i_a), transformer secondary current (i_{xa2}), output capacitor current (i_{Ca}) for repetitive control with line-to-line connected nonlinear load.

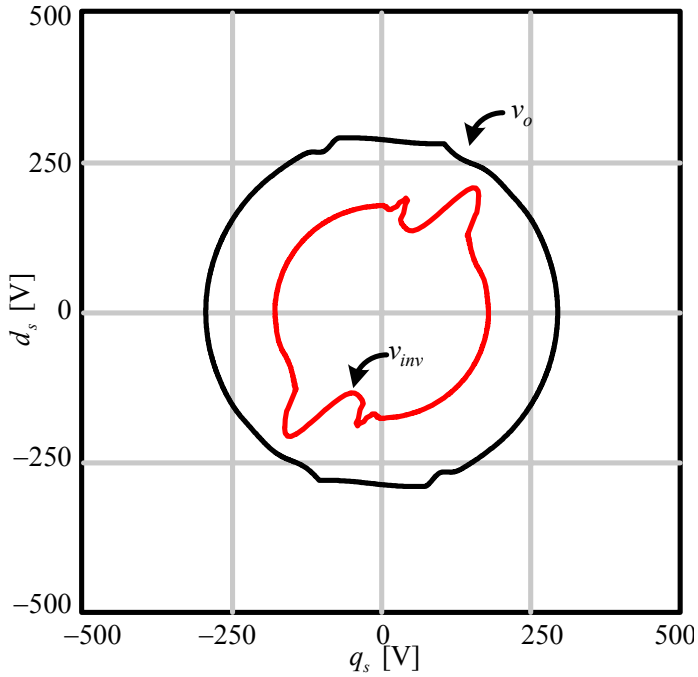

Figure 3.40 Stationary frame vector representation of the output voltages (v_o) and inverter reference voltages (v_{inv}) for repetitive control under line-to-line connected single-phase nonlinear load.

3.7 Dynamic Performance Evaluation of The Repetitive Controlled UPS

In order to evaluate the dynamic performance of the designed controller, the UPS is loaded from no-load to balanced linear resistive full-load. The effect of each controller on the UPS output voltage during the loading transient is investigated. The load is turned on with a switch at the highest voltage level of one phase, in order to achieve the most challenging transient loading condition. Figure 3.41 shows the open-loop operated UPS dynamic performance. At the loading instant, load draws the current form the output filter capacitors. Thus, the output voltages collapse during loading. The UPS output voltage vector and inverter reference vector during the transients are given in Figure 3.42. After the loading instant, output voltage vector can not trace the same route due to the voltage drop on the output impedance of the UPS indicating poor dynamic performance.

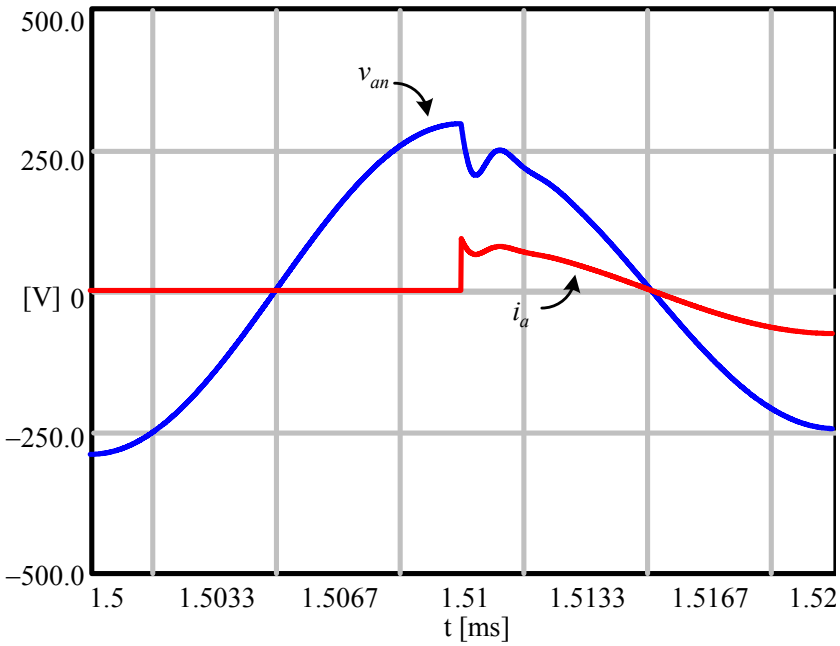

Figure 3.41 One phase of the UPS output voltage (v_{an}) and load current (i_a) during the loading transient for open-loop operation.

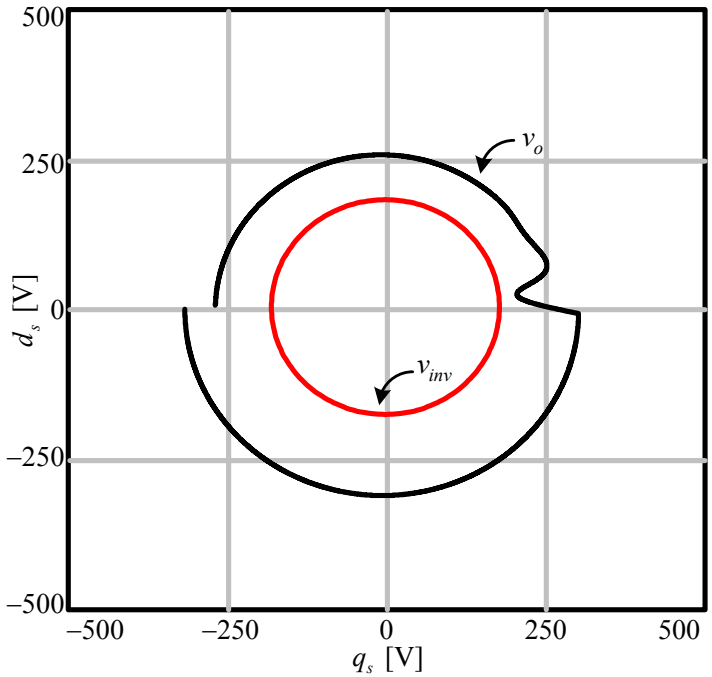

Figure 3.42 Stationary frame vector representation of the output voltages (v_o) and inverter reference voltages (v_{inv}) for open-loop controlled operation during loading transients.

The inclusion of the capacitor current feedback damps the oscillatory response of the LC filter alone. As shown in Figure 3.43, with the capacitor current feedback the transient duration is shorted and the output voltages reach the steady-state in a short period of time. Since the capacitor current feedback has considerable effect only at high frequencies, it has no contribution on the output voltage regulation. The UPS output voltage vector and inverter reference vector are given in Figure 3.44. Following the loading instant, the inverter immediately responds and generates a rapid voltage pulse to correct the output voltage error. However the output voltage vector can not trace the same route due to the voltage drop on the output impedance of the UPS as in the previous case.

In order to improve dynamic response, the output voltage proportional controller is employed. The controller has considerable effect on the loading transient. The output voltage rapidly rises in case of loading as shown in Figure 3.45. The output voltage vector traces a route closer to the no-load case as shown in Figure 3.46.

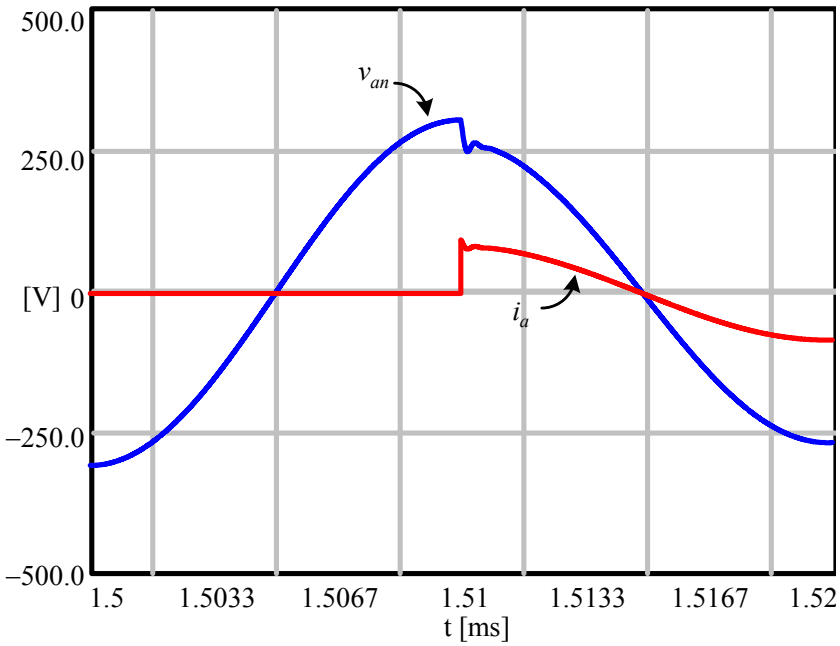

Figure 3.43 One phase of the UPS output voltage (v_{an}) and load current (i_a) during the loading transient for closed-loop operation with capacitor current feedback.

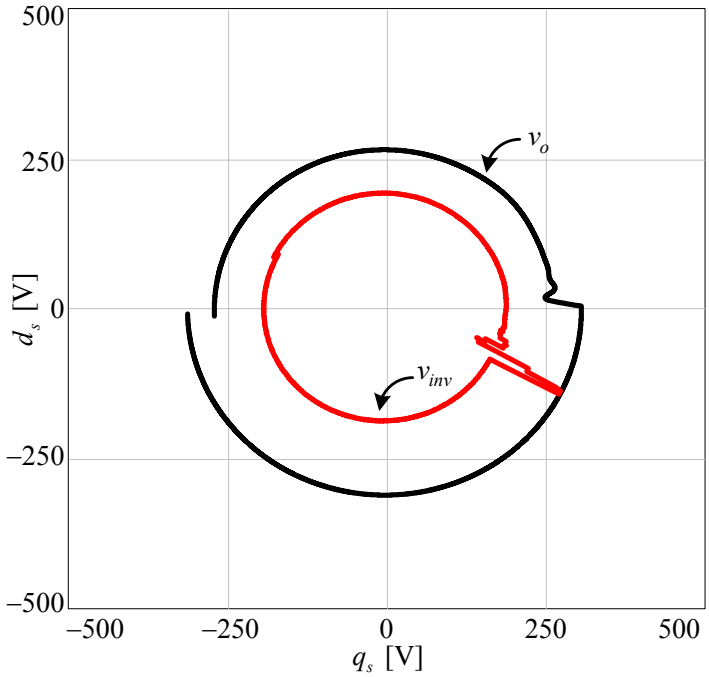

Figure 3.44 Stationary frame vector representation of the output voltages (v_o) and inverter reference voltages (v_{inv}) for closed-loop controlled operation with capacitor current feedback during loading transients.

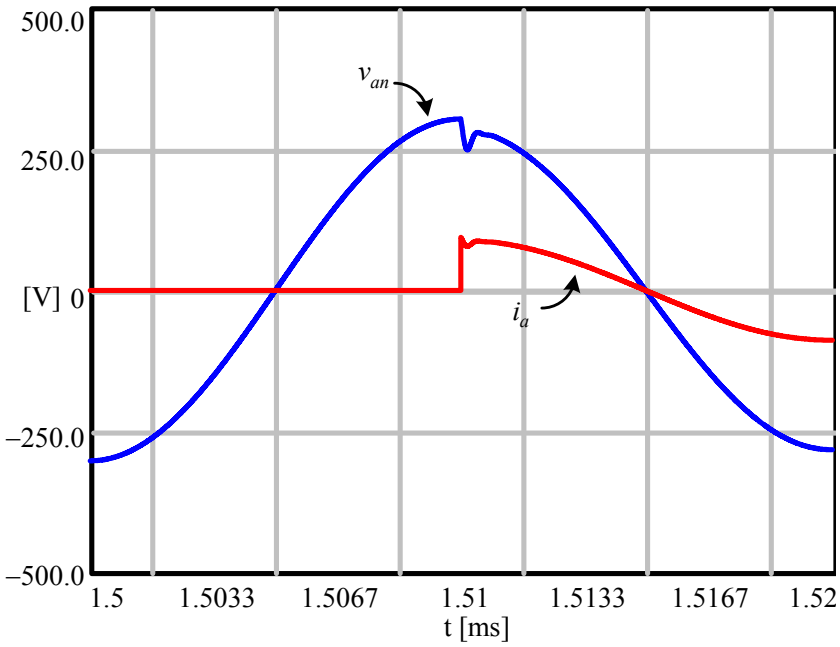

Figure 3.45 One phase of the UPS output voltage (v_{an}) and load current (i_a) during the loading transient for closed-loop operation with capacitor current feedback + proportional controller.

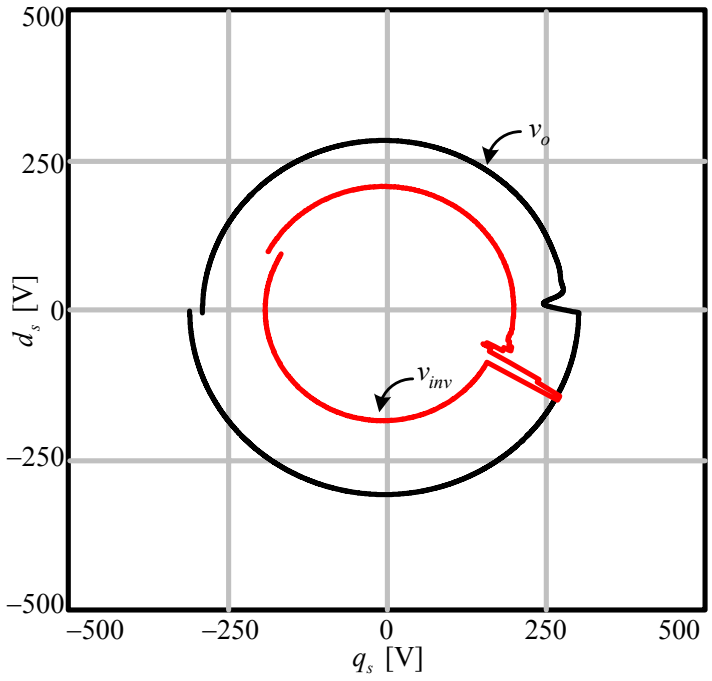

Figure 3.46 Stationary frame vector representation of the output voltages (v_o) and inverter reference voltages (v_{inv}) for closed-loop controlled operation with capacitor current feedback+ proportional controller during loading transients.

This chapter provided a practical repetitive controller design study. The study results were utilized in the UPS system model to simulate the repetitive controlled UPS system and investigate the system behavior under steady-state operating condition for nonlinear balanced and unbalanced load, and under dynamic operating condition for linear resistive load. The results indicate the repetitive controller provides adequate steady-state performance under nonlinear load and low UPS output voltage THD and high output voltage regulation could be obtained. Summarized Table 3.7, the steady-state performance of the repetitive controlled UPS is satisfactory for most applications. Also it has been shown that the dynamic response of the repetitive controlled UPS could be enhanced with capacitor current feedback and proportional control on the voltage feedback loop.

Table 3.7 Steady-state performance data of repetitive controlled UPS system

		Open-loop	Closed-loop
Balanced nonlinear load	THD_v (%)	6.71	1.18
	CF	1.26	2.55
	VR (%)	14.5	0.29
	V_a V_b V_c (V_{rms})	188.1	219.4
	i_a, i_b, i_c (A_{rms})	4.1	6.8
Line-to-neutral connected nonlinear load	THD_v (%)	5.2	1.33~1.76
	CF	2.55	3.55
	VR (%)	7.2	0.1
	V_a V_b V_c (V_{rms})	208.1, 203.1, 206.9	219.75, 219.5, 220
	i_a, i_b, i_c (A_{rms})	0, 2.59, 0	0, 5.62, 0
Line-to-line connected nonlinear load	THD_v (%)	7.38	0.0-0.95
	CF	2.2	3.53
	VR (%)	11	0.0-0.2
	V_a V_b V_c (V_{rms})	209, 197, 195	219.8, 219.6, 219.46
	i_a, i_b, i_c (A_{rms})	0, 3.24,3.24	0, 3.59, 3.59

CHAPTER 4

PERFORMANCE VERIFICATION OF THE REPETITIVE CONTROLLED ISOLATION TRANSFORMER BASED THREE-PHASE UPS BY MEANS OF EXPERIMENTAL STUDY

4.1 Introduction

In this chapter, the repetitive control method for the isolation transformer based three-phase UPS, which was designed in Chapter 3, is investigated experimentally. First, the three-phase UPS prototype system constructed in the laboratory is explained in detail. Then, the experimental test procedure is described and the experimental results, which show the repetitive controlled UPS performance of the UPS, are reported. The experimental results are evaluated and compared with the computer simulation results of Chapter 3. Strong correlation between the theory, computer simulations, and experimental results is shown.

4.2 Hardware Implementation the Isolation Transformer Based UPS

The isolation transformer based UPS system is constructed at METU Electrical and Electronics Engineering Department, in the Electrical Machines and Power Electronics Laboratory as a prototype. The UPS system comprises mainly power circuitry, control platform, and electronic interface circuitry.

The diagram of the electrical power circuitry is given in Figure 4.1. The parameters of the system are the same as those of the simulation studies of Chapter 3 as listed in Table 3.1. The power circuitry is fed from the three-phase 380 V, 50 Hz AC utility grid. Following, a three-phase 20 A fuse and a contactor, which is used as a circuit breaker in case of emergency, are employed. Also a 3% three-phase AC line reactor is utilized at the input stage (L=2.3 mH/phase). at the AC line input stage.

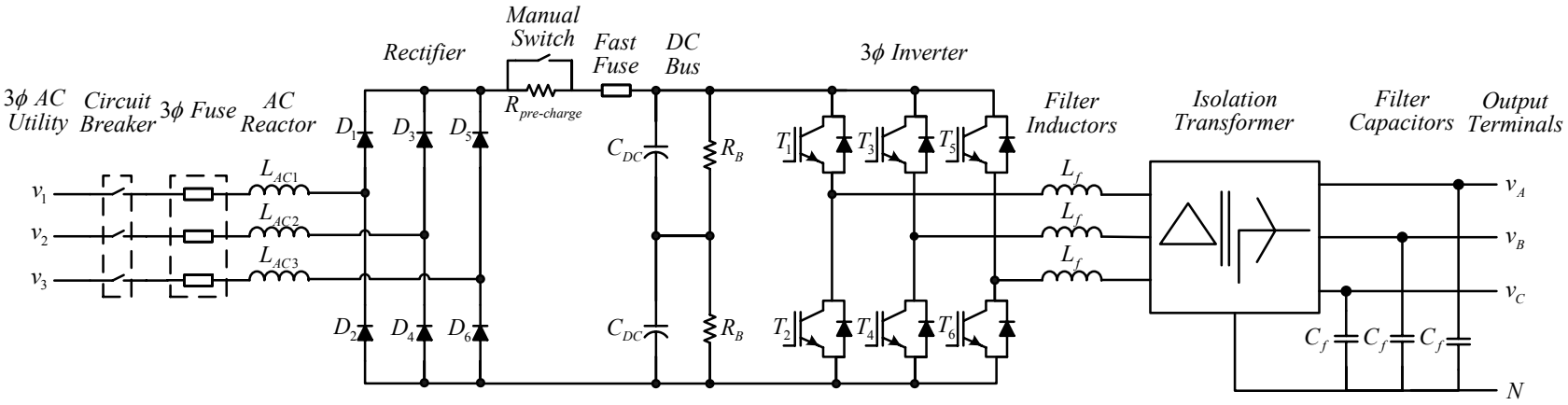

Figure 4.1 The electrical power circuitry of the overall UPS system.

The rectifier, DC bus and inverter stages of the power circuitry are assembled inside the SEMITEACH module, which is a laboratory inverter teaching set manufactured by Semikron. The rectifier is a standard three-phase six-pulse diode rectifier, SKD 51/14 manufactured by Semikron. DC bus voltage is smoothed by two series connected electrolytic capacitors, each having a capacitance value of 2200 μF and a voltage rating of 400 V. Thus, the equivalent capacitance is 1100 μF. A 30 kΩ, 10 W bleeding resistor is connected in parallel with each capacitor to discharge the capacitors at the system turn-off and provide charge balance during normal operation. In order to avoid high inrush current at the start-up during the charging of the DC capacitors, a pre-charge resistor is employed. The DC capacitors are charged through the pre-charge resistor initially and then the resistor is by-passed via a mechanical switch. The pre-charge resistor value is 47 Ω and has a power rating of 50 W. At the pre-charge stage the inverter is not enabled and it draws no current from the rectifier. In series with the pre-charge resistor, a semiconductor fast fuse with a rating of 20 A is employed in order to protect the system from shoot-through/overcurrent hazards. The SEMITEACH module has three dual-pack IGBT modules, the SKM 50GB123 model modules manufactured by Semikron. Also an additional SKM 50GB123 module is employed for breaking purpose in the motor drive applications, however it is not utilized in the given UPS application. In Table 4.1 the basic specifications of the SKM 50GB123 IGBT modules are given. The IGBT modules are driven by the Semikron brand SKHI 22B model gate driver modules. The basic specifications of the gate drive modules utilized in the SEMITEACH inverter module are summarized in Table 4.1. The gate driver module converts the PWM signal at +15/0 voltage levels to an isolated and amplified +15/-7 voltage levels, which is required for the IGBT turn-on and turn-off switching operations. The gate driver circuit also monitors the collector-emitter voltage for short-circuit failure condition. While the IGBT is conducting, the collector-emitter voltage of the IGBT must be lower than the preset desaturation limit voltage value, which is slightly larger than V_{Cesat}. Otherwise the power dissipation on the IGBT increases and the semiconductor switch may be damaged. In order to avoid such a problem, the gate driver module turns off the IGBT and outputs an error signal to the protection board (the desat signal) if the collector-emitter voltage is larger than the

limit value. The gate driver modules have built-in analog dead-time generation facility. However, this hardware deadtime generation mechanism is bypassed in this work and the dead-time is generated with a value of 2μs from the controller (DSP) in as this approach provides higher accuracy PWM outputs.

Table 4.1 Specifications of the power semiconductor and gate driver modules utilized in the experimental UPS system

SKM 50GB123 D (IGBT of the dual pack)		
V_{CES}	Collector-emitter blocking voltage rating	1200 V
I_C	Continuous collector current rating (rms)	50 A
V_{CEsat}	Collector-emitter saturation voltage at 50 A	2.7 V
$t_{d(on)}$	Turn-on delay time	70 ns
t_r	Rise time	60 ns
$t_{d(off)}$	Turn-off delay time	400 ns
t_f	Fall time	45 ns
SKM 50GB123 D (Diode of the dual pack)		
V_F	Forward voltage drop at I_F=50 A	2 V
I_{RRM}	Peak reverse recovery current	23 A
Q_{rr}	Recovered charge at I_F=40 A	2.3 μC
SKHI 22B Gate Driver Module		
V_S	Supply voltage primary side	15 V
I_{SO}	Supply current primary side at no-load/max.	80 / 290 mA
V_i	Input signal voltage ON/OFF	5 / 0 V
V_{iT+}	Input threshold voltage (High)	3.7 V
V_{iT-}	Input threshold voltage (Low)	1.75 V
R_{in}	Input resistance	3.3 kΩ
$V_{G(ON)}$	Turn-on gate voltage output	+15 V
$V_{G(OFF)}$	Turn-off gate voltage output	-7 V
t_{TD}	Top-Bottom interlock dead-time min. / max.	no interlock / 4.3 μs

A three-phase isolation transformer with a power rating of 10 kVA is utilized at the output stage of the UPS system. The parameters of the isolation transformer, which are obtained by utilizing the open-circuit and short-circuit test results, were given in the previous chapter in Table 3.1. The equivalent circuit for one phase of the transformer was also shown in Figure 3.3. The filter inductors, which are employed between the inverter and the isolation transformer, have a value of 500 μH per phase and are manufactured from ferrite core and copper foil windings. The nominal RMS current rating of the inductors is 20 A. The laboratory transformer and inductor filters are shown in Figure 4.2. The filter capacitors, which are employed at the output of the isolation transformer, are AC capacitors having a value of 20 μF and a voltage rating of 500 V.

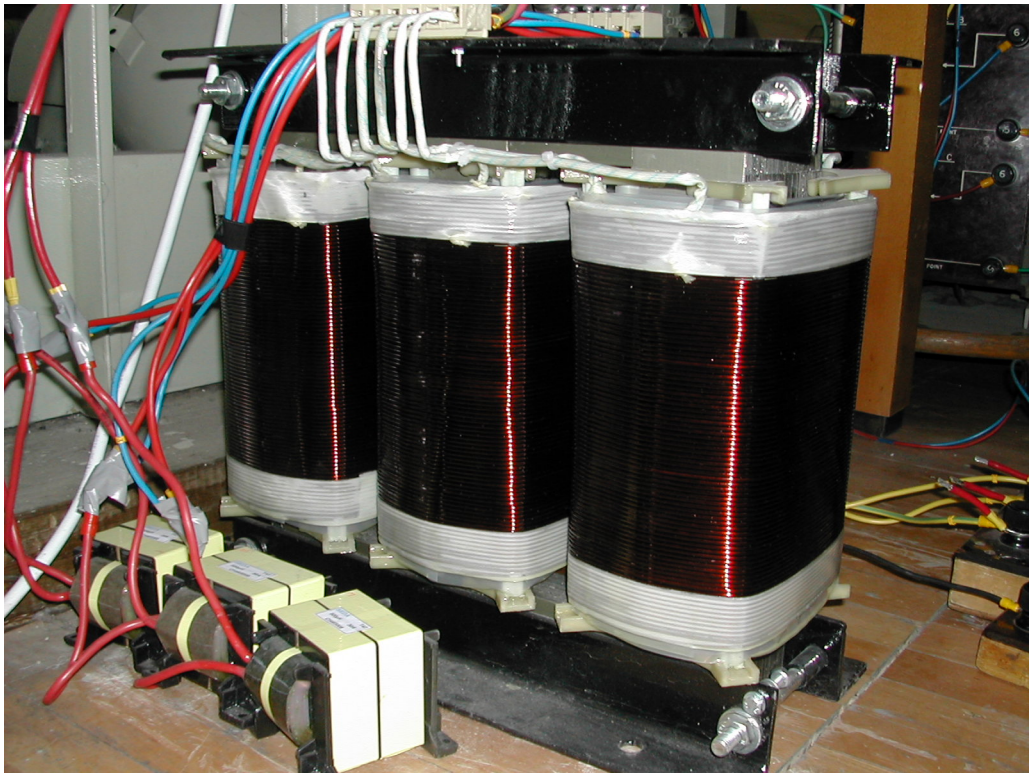

Figure 4.2 The experimental Δ/Y isolation transformer and filter inductors.

The electronic interface circuit diagram of the UPS system is given in Figure 4.2. The interface circuitry comprises voltage and current sensors, a signal conditioning board, protection board and level shifter board. The sensors are utilized for sensing the voltage and current variables, which are utilized either for control or protection purposes. The output voltages of the UPS are sensed by utilizing three Voltage Transformers (VT). These voltage transformers have a voltage transfer ratio of 220V/9V. Since the UPS has an isolation transformer, no DC voltage component exists at the output of the system. Thus, three VTs are adequate for measuring the three-phase output voltages of the UPS system. The three-phase UPS filter inductor currents are sensed for protecting the inverter from overcurrent due to a short-circuit in the system. Since the inverter may output DC voltage components, DC current can flow through the primary winding of the isolation transformer and consequently the transformer may saturate. Thus, the filter inductor currents are measured by a hall-effect current sensor, LA55 manufactured by LEM. The filter capacitor currents are sensed to be utilized for control purpose. Since the filter capacitor currents do not include DC component, Current Transformers (CT) with a current rating of 20 A are utilized for sensing the filter capacitor currents. The DC bus voltage is measured for decoupling the inverter output voltages from the fluctuations in the DC bus voltage by means of a LEM voltage sensor which is based on the Hall effect. In the signal conditioning board, all the sensed variables are scaled to the voltage range (±10V) of the Analog to Digital Converters (ADC) of the dSPACE control platform. Also in the signal conditioning board, the scaled variables are filtered from high-frequency noise. The feedback signals are discretized by the ADC of the dSPACE and PWM signals for the inverter are generated based on the control algorithm performed inside the control platform. The PWM signals are at +5/0 voltage levels for the logic signals 1 and 0, respectively. Since the gate driver demands a voltage level of 15 V for the logic gate signal 1 (for high signal-to-noise ratio), PWM signals are shifted from 5 V to 15 V by the level shifter electronic circuitry. Also a protection circuitry is utilized to set the PWM signals to zero in case of any abnormal condition in the system. The abnormal conditions are excessive filter inductor current, desaturation signal generated by the gate driver of the inverter, and excessive temperature rise in the inverter.

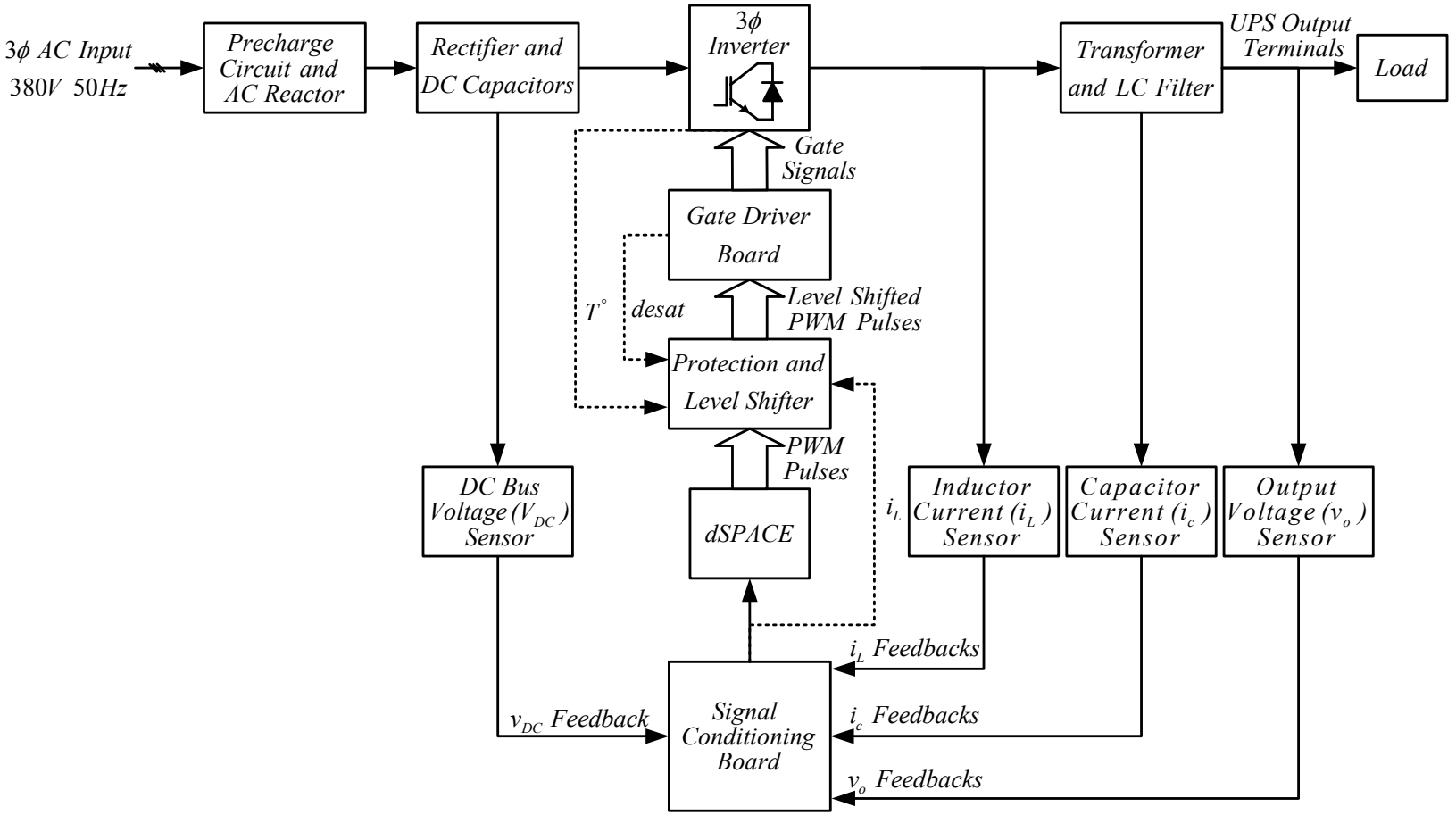

Figure 4.3 The control platform and electronic interface circuitry of the UPS system.

The control algorithms are implemented in the UPS system by utilizing the dSPACE control platform. In Table 4.2 the main features of dSPACE are summarized. The DS1104 R&D Controller Board is a standard electronic board that can be plugged into a Peripheral Communication Interface (PCI) slot of a PC [36]. The DS1104 R&D Controller Board is specifically designed for the development of the high-speed multivariable digital control algorithms and real-time simulations in various fields. It is a complete real-time control system based on a 603 PowerPC floating-point processor having a clock frequency of 250 MHz. For advanced I/O purposes, the board includes a slave Digital Signal Processor (DSP) subsystem based on the TMS320F240 DSP. For purposes of Rapid Control Prototyping (RCP), CLP1104 Connector/LED Panel provides an easy access to all input and output signals of the board. External devices can be individually connected, disconnected or interchanged via BNC connectors and Sub-D connectors. It also provides an array of LEDs indicating the states of the input/output digital signals. This simplifies the system construction, testing and troubleshooting. Thus, the DS1104 R&D Controller Board is an ideal hardware for the dSPACE Prototyper development system for cost-sensitive RCP applications. The control platform has two ADC modules. One of the ADC modules has four multiplexed channels with 16 bit resolution and each conversion takes 2 μs for this module. The input signals at the channels are sampled in sequence. The other ADC module has four parallel channels each equipped with one 12-bit ADC with 800 ns conversion time. The control platform samples the feedback data utilizing the ADCs and generates PWM signals based on the digital control algorithm performed inside the processor.

The complete system hardware of the prototype is shown in Figure 4.4. In the following this hardware will be utilized and first the UPS performance problems for open-loop operation will be demonstrated. In the second stage the repetitive controller will be tuned in a similar manner to the experimental stage. Then the steady-state and dynamic performance tests and performance evaluation studies will follow.

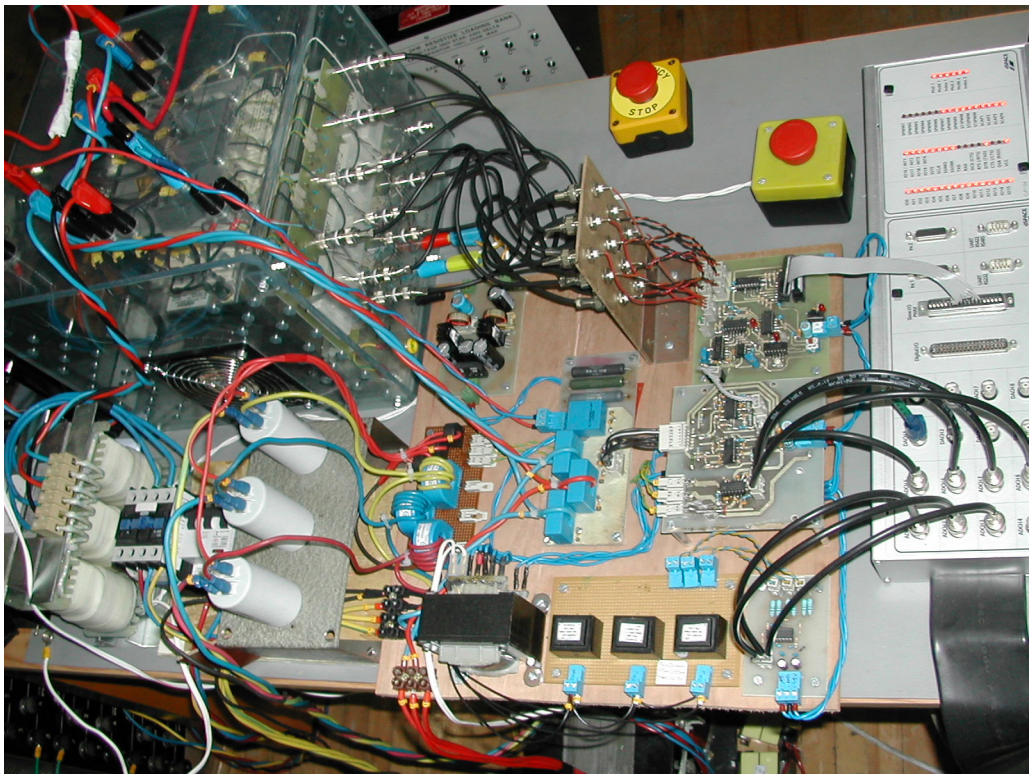

Figure 4.4 The prototype UPS power converter (left), control(right), and electronic interface circuit (middle).

Table 4.2 Main features of the dSPACE control platform

Parameter	Characteristics
Processor	• MPC8240 processor with PPC603e core and on-chip peripherals • 64-bit floating-point processor • 250 MHz CPU • 2 x 16 KB cache; on-chip • On-chip PCI bridge (33 MHz)
Memory	• Global memory: 32 MB SDRAM • Flash memory: 8 MB
Timer	• 1 sample rate timer (decrementer): 32-bit down counter, reload by software, 40 ns resolution • 4 general purpose timer: 32-bit down counter, reload by hardware, 80 ns resolution • 1 time base counter: 64-bit up counter, 40 ns resolution, range 23400 years
Interrupt controller	• 5 timer interrupts • 2 incremental encoder index line interrupts • 1 UART interrupt • 1 slave DSP interrupt • 1 slave DSP PWM interrupt • 5 ADC end of conversion interrupts • 1 host interrupt • 4 user interrupts from the I/O connector
ADC 1 x 16-bit ADC with mux	• 4 muxed channels equipped with one 16-bit S&H ADC • 16-bit resolution • ±10 V input voltage range • 2µs conversion time • >80 dB signal-to-noise ratio (SNR)
ADC 4 x 12-bit ADC	• 4 channels each equipped with one 12-bit S&H ADC • 12-bit resolution • ±10 V input voltage range • 800 ns conversion time • >65 dB signal-to-noise ratio (SNR)
Slave DSP subsystem	• Texas Instruments TMS320F240 DSP • 16-bit fixed-point processor • 20 MHz clock frequency • 64 K x 16 external program memory • 28 K x 16 external data memory • 4 K x 16 dual-port memory for communication • 16 K x 16 flash memory • 1 x 3-phase PWM output • 4 x 1-phase PWM output • 4 capture inputs • Max. 14-bit digital I/O • TTL output/input levels for all digital I/O pins

4.3 Steady-State Operating Performance of Open-loop Controlled Isolation Transformer Based Three-Phase UPS With Nonlinear Load

The goal of this section is to illustrate the open-loop steady-state performance problems of the isolation transformer based three-phase UPS under various load type operating conditions. The UPS will be voltage feedforward controlled and no feedback loops will be involved. All loading conditions (balanced/unbalanced and/or linear/nonlinear loads) will be investigated. The open-loop steady-state performance characteristics will be displayed for the purpose of illustration of the performance problems of the UPS under such operating conditions.

4.3.1 UPS Output Performance Under Balanced Nonlinear Load

In order to show the problem due to nonlinear loading, the UPS is loaded with a rated balanced nonlinear load. The three-phase output voltages and the load current for one phase are shown in Figure 4.5. The distorted voltage waveforms are nearly triangular, which are similar to simulation result given in Figure 3.6. The harmonic spectrum of the UPS output voltages for such a loading condition is given in Figure 4.6. The spectrum is rich in harmonics. The UPS output voltage THD is measured as 10 % and the load current crest factor is measured as 1.78. Output voltage regulation is considerably poor with a value of 13%. The space vector representation of the output voltages in complex coordinates is also given in Figure 4.7. The output voltage vector traces a hexagon shaped route due to nonlinear loading.

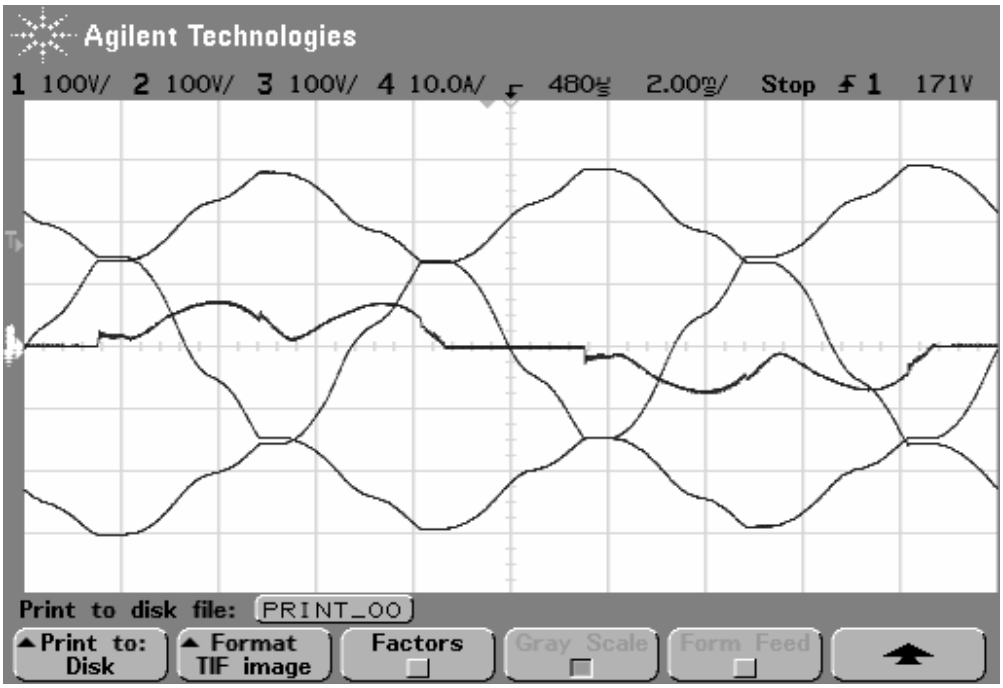

Figure 4.5 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) load current (i_a) for open-loop operation (Scaling: 100 V/div, 10 A/div, and 2ms/div).

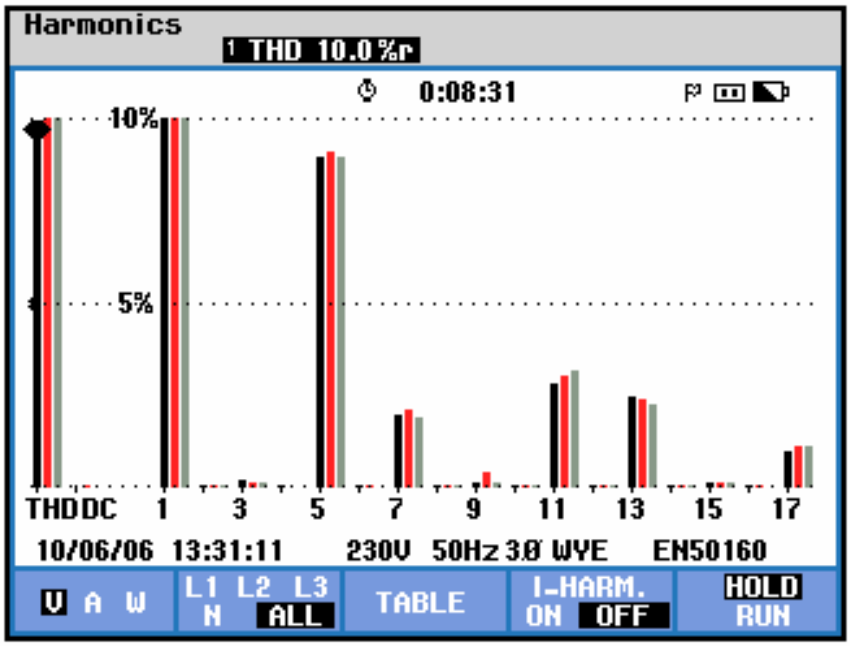

Figure 4.6 Harmonic spectrum of three-phase output voltages for open-loop operation.

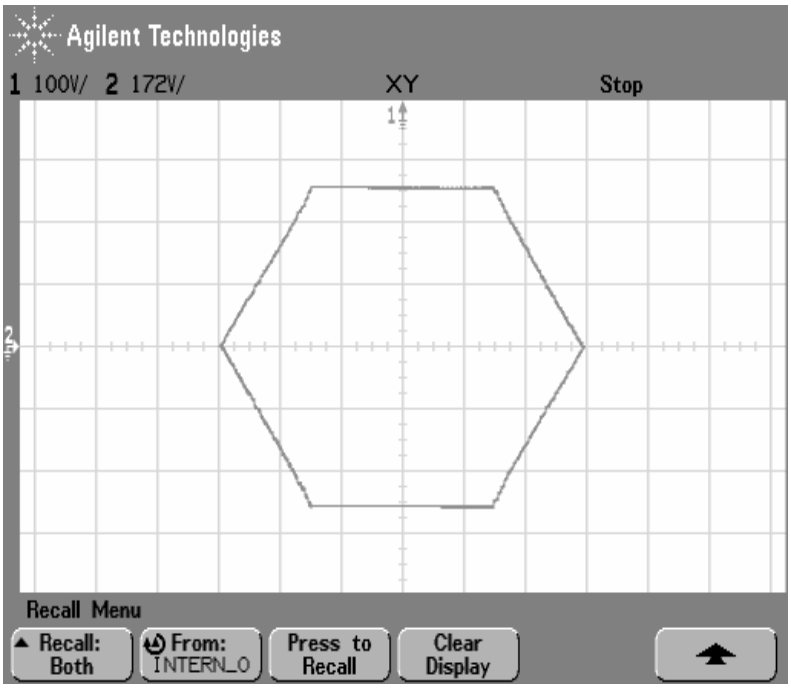

Figure 4.7 Stationary frame vector representation of the output voltages for open-loop operation under balanced nonlinear rated load (Scaling: X:100 V/div, Y:172 V/div).

4.3.2 UPS Output Performance Under Single-Phase Unbalanced Nonlinear Load

Open-loop controlled steady-state operation is observed by loading the UPS with single-phase unbalanced nonlinear load (a diode rectifier load) with 1.3 kVA. The resulting waveforms are reported in the following. The three-phase output voltages and the load current for one phase are shown in Figure 4.8. The loaded phase output voltage (v_{an}) is the most distorted phase and it has a THD value of 7.7% and the load current crest factor is 2.6. The harmonics spectrum shown in Figure 4.9 contains 3^{rd}, 5^{th}, 7^{th}, 9^{th}, and 11^{th} harmonics dominantly. The output voltage regulation is approximately 8% for the loaded UPS output phase voltage. Figure 4.10 shows that the UPS output voltage vector is pressed at two edges which correspond to the instants that the load current pulses are drawn from the UPS. The zero sequence currents, which circulate inside the Δ primary windings, do not cause significant amount of zero sequence distortion on the output voltages (0.8 %). However the negative sequence distortion is still high (9.5 %).

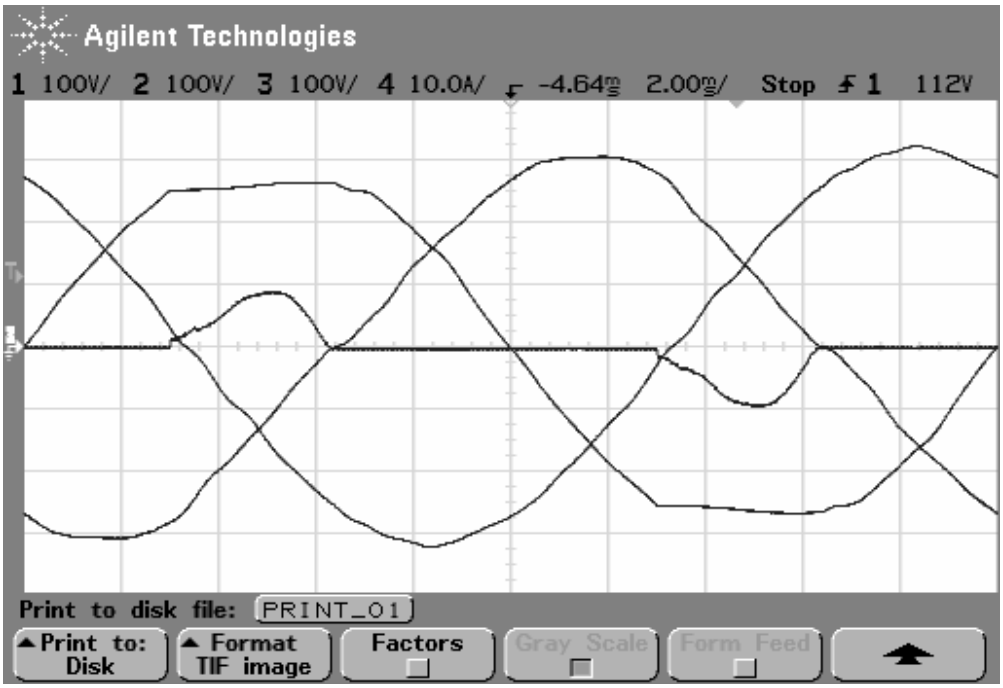

Figure 4.8 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current i_a for open-loop operation at line-to-neutral connected single-phase nonlinear unbalanced rated load (Scaling: 100 V/div, 10 A/div, and 2ms/div).

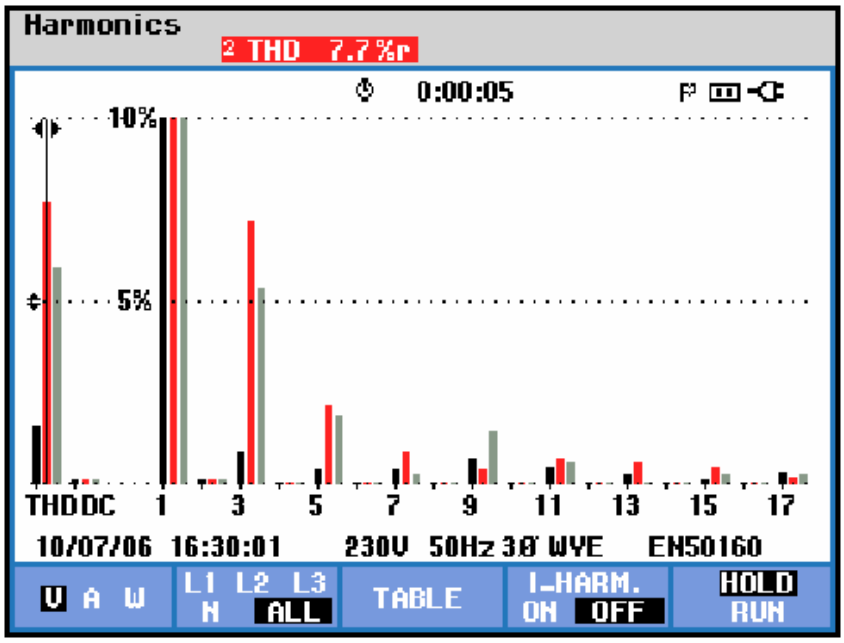

Figure 4.9 Harmonic spectrum of three-phase output voltages for open-loop operation under line-to-neutral connected nonlinear load.

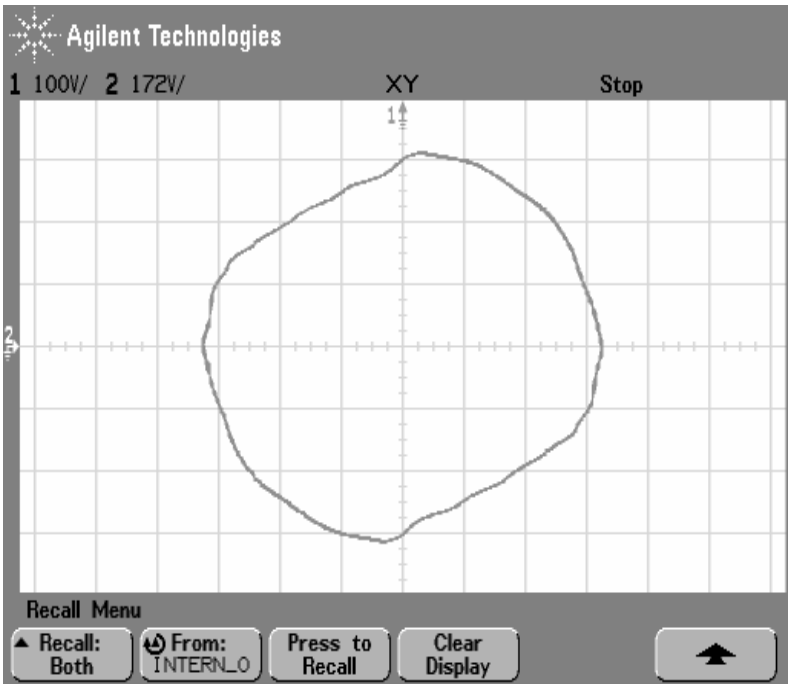

Figure 4.10 Stationary frame vector representation of the output voltages for open-loop operation under line-to-neutral connected nonlinear load (Scaling: X: 100 V/div, Y: 172 V/div).

4.3.3 UPS Output Performance Under Line-to-line Unbalanced Nonlinear Load

Open-loop controlled steady-state operation under line-to-line unbalanced nonlinear load with 3 kVA is observed. The resulting waveforms are reported in the following. The three-phase output voltages and the load current for one phase are shown in Figure 4.11. The output voltage THD is 11.4 % and the load current crest factor is 2.44. The harmonics spectrum shown in Figure 4.12 contains 3^{rd}, 5^{th}, 7^{th}, 9^{th}, and 11^{th} harmonics dominantly. The output voltage regulation approaches 11.5 % for the loaded UPS output phase voltages. Figure 4.13 show the UPS output voltage vector is pressed at two edges which correspond to the instants when the load current pulses are drawn from the UPS. Line-to-line loading leads to only negative sequence imbalance (13.1 %).

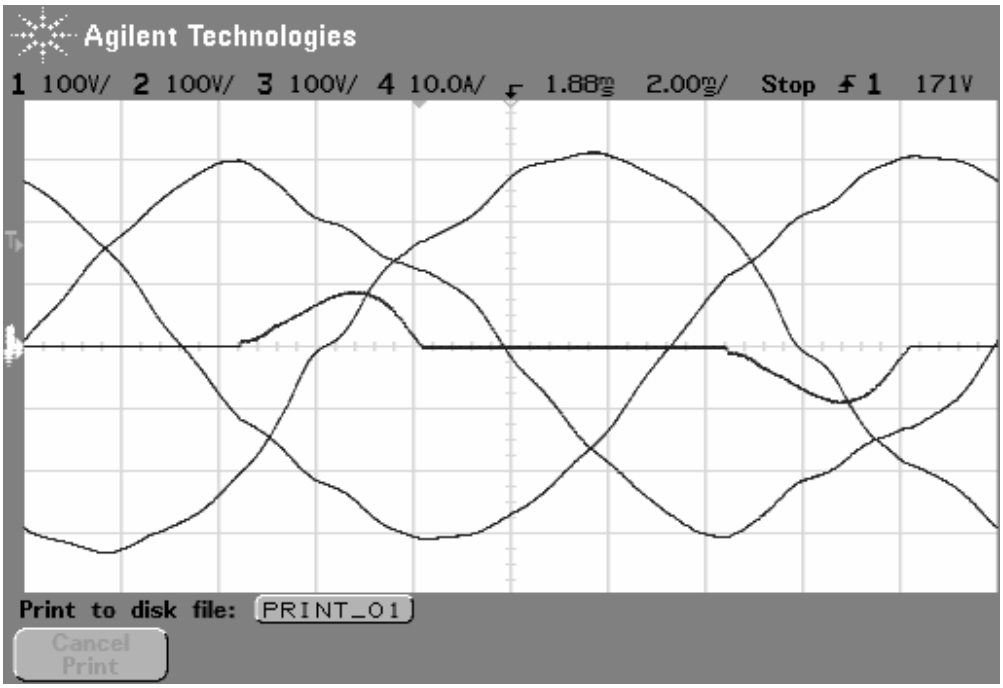

Figure 4.11 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current i_a for open-loop operation at line-to-line connected nonlinear load (Scaling: 100 V/div, 10 A/div, and 2ms/div).

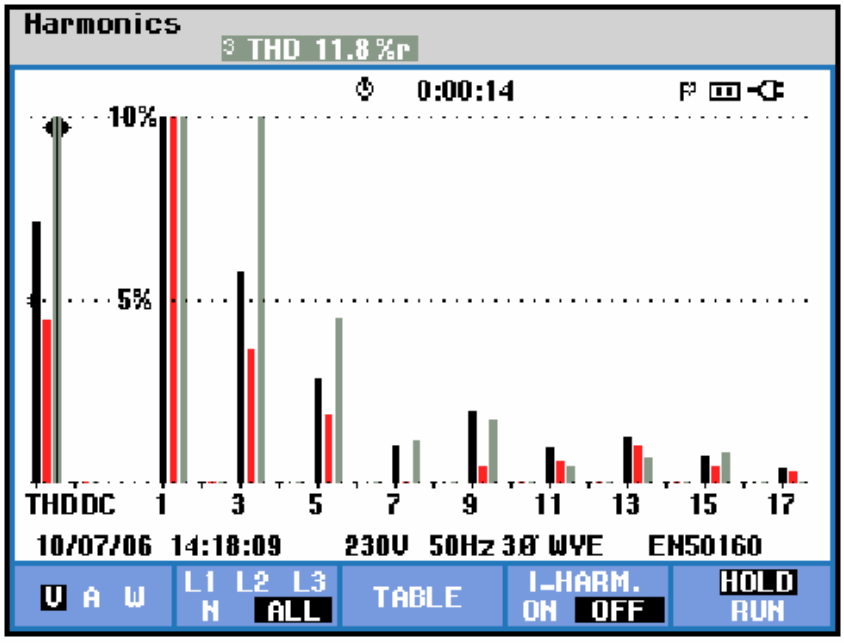

Figure 4.12 Harmonic spectrum of three-phase output voltages for open-loop operation under line-to-line connected nonlinear load.

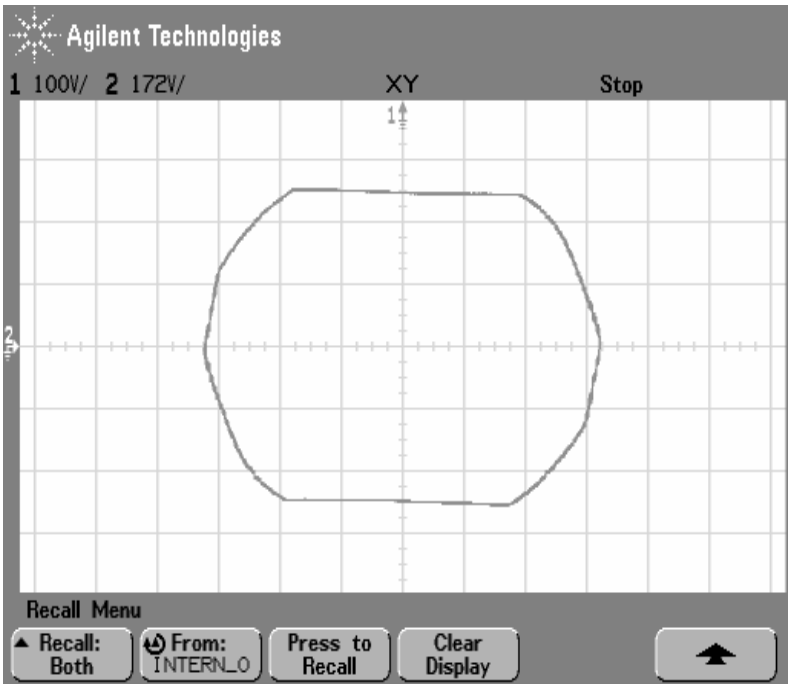

Figure 4.13 Stationary frame vector representation of the output voltages for open-loop operation under line-to-line connected nonlinear load (Scaling: X: 100 V/div, and Y:172 V/div).

4.3.4 UPS Output Performance at No-Load Operating Condition

The UPS system is operated at no-load with open loop control, in order to observe the steady-state behavior at no-load. The resulting waveforms are reported in the following. The three-phase output voltages and the load current for one phase are shown in Figure 4.14. Although the UPS is not loaded there exists small distortion on the output voltages. The distortion stems from the nonlinearities in the inverter such as dead-times in the gate driver, turn on/off times of the semiconductor switches etc. The output voltage THD is observed as 1.5 %. The harmonics spectrum shown in Figure 4.15 contains small amount of only odd harmonics. The output voltage regulation approaches 0.2 %. The UPS output vector, given in Figure 4.16, traces a route with small deviations from circle.

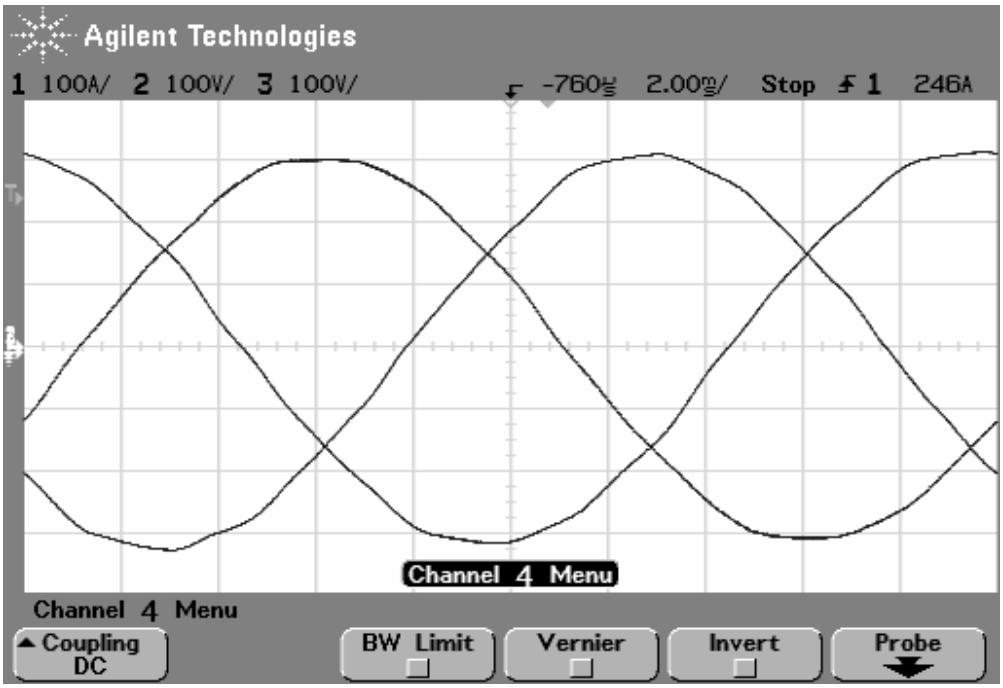

Figure 4.14 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) for open-loop operation at no-load (Scaling: 100 V/div and 2ms/div).

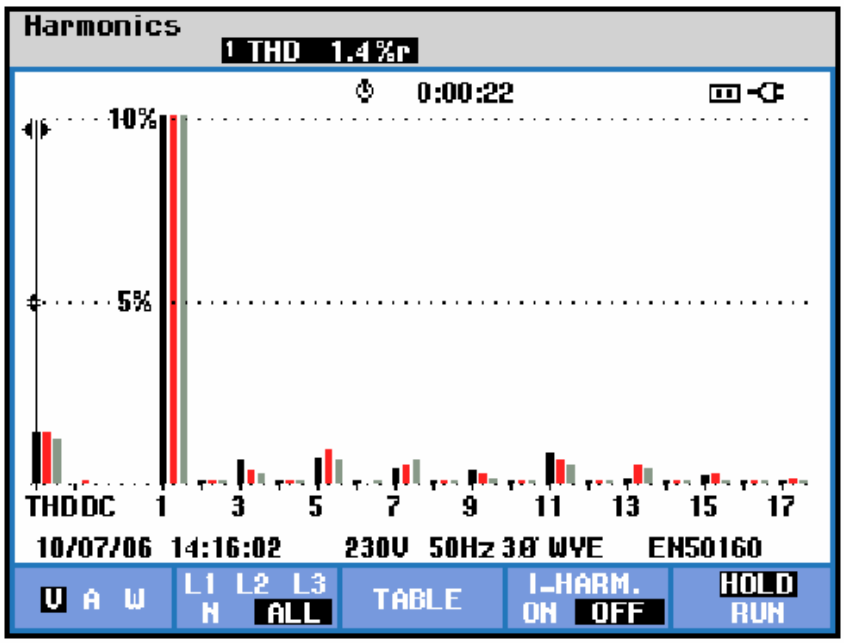

Figure 4.15 Harmonic spectrum of three-phase output voltages for open-loop operation at no-load.

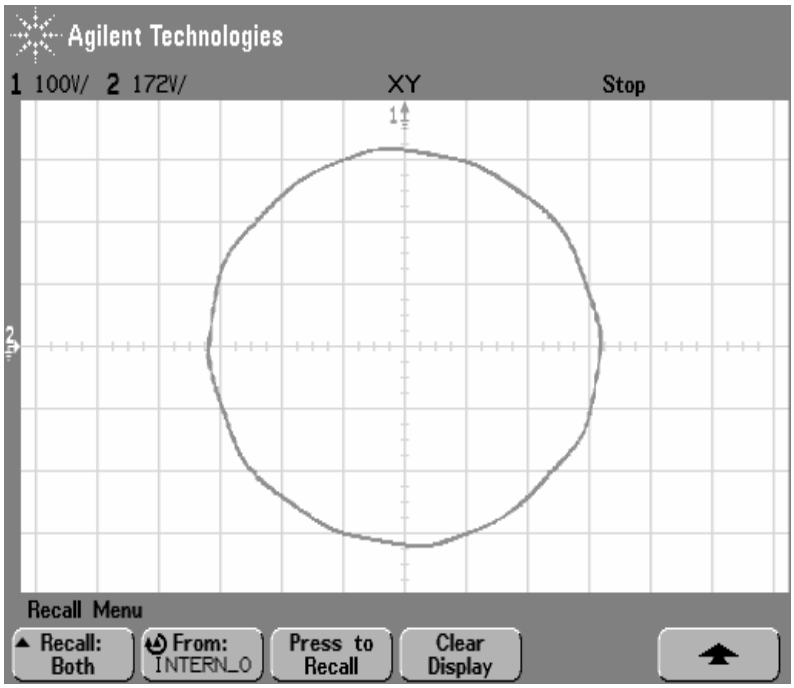

Figure 4.16 Stationary frame vector representation of the output voltages for open-loop operation at no load (Scaling: X:100 V/div and Y: 172 V/div).

4.3.5 UPS Output Performance Under Three-Phase Balanced Rated Linear Load

Open-loop controlled steady-state operation is observed for the UPS with three-phase balanced linear resistive load with 5 kW. The resulting waveforms are reported in the following. The three-phase output voltages and the load current for one phase are shown in Figure 4.17. With high load current, dead-times have considerable distorting effect on the output voltages. The output voltage THD value is 4.3 %. The harmonics spectrum shown in Figure 4.18 contains 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics dominantly. The output voltage regulation is approximately 16.7 %. With considerable amount of 5^{th} and 7^{th} harmonics on the UPS output voltages, UPS output voltage vector, given in Figure 4.19, traces a route, which resembles a hexagon.

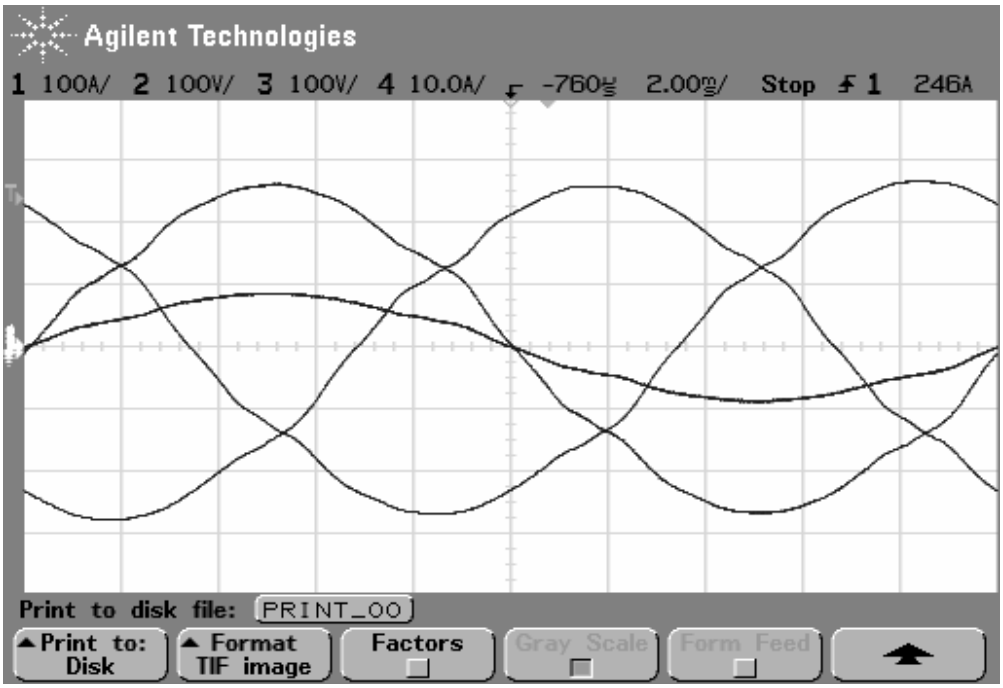

Figure 4.17 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current i_a for open-loop operation under three-phase balanced linear load (Scaling: 100 V/div, 10 A/div, and 2ms/div).

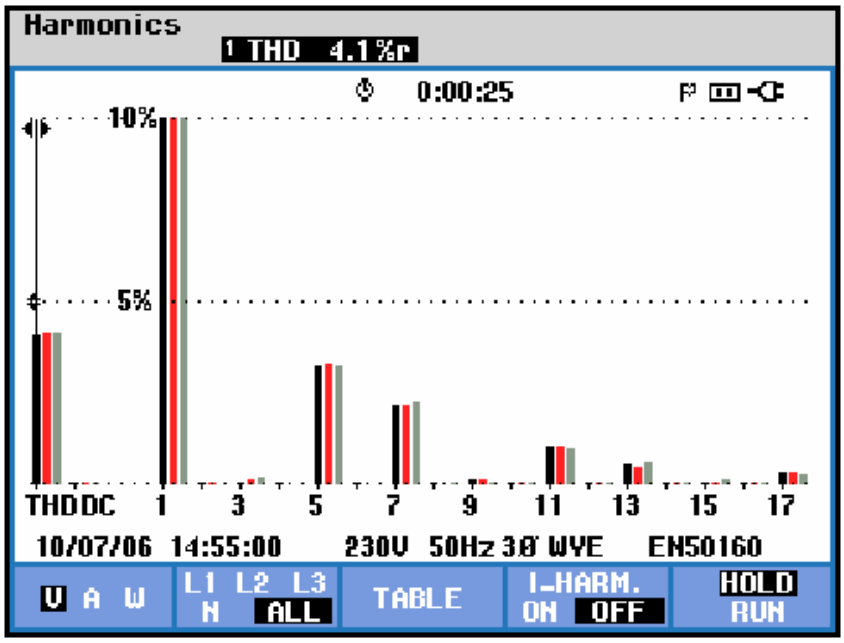

Figure 4.18 Harmonic spectrum of three-phase output voltages for open-loop operation under three-phase balanced linear load of 5 kVA.

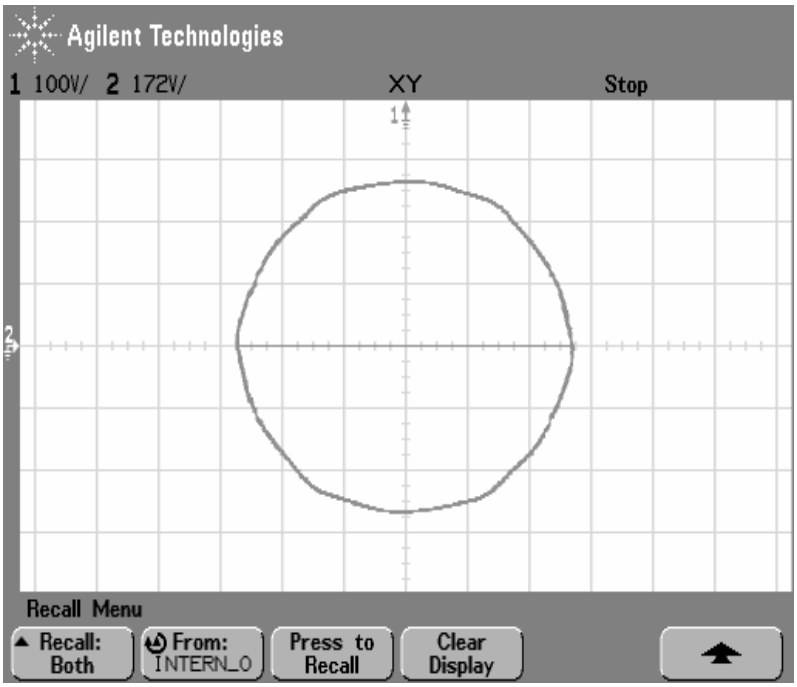

Figure 4.19 Stationary frame vector representation of the output voltages for open-loop operation under three-phase balanced linear load (Scaling: X:100 V/div and Y: 172 V/div).

4.3.6 UPS Output Performance Under Single-Phase Unbalanced Linear Load

Open-loop controlled steady-state operation is observed for the UPS with single-phase unbalanced linear resistive load with 1.3 kW. The resulting waveforms are reported in the following. The three-phase output voltages and the load current for one phase are shown in Figure 4.20. Unbalanced loading causes also the 3^{rd} and 9^{th} harmonics to exist on the output voltages due to the dead-times. Thus the harmonics spectrum shown in Figure 4.21 involves 3^{rd}, 5^{th}, and 7^{th} harmonics dominantly. The output voltage THD value increases up to 7.3 %. The output voltage regulation is 18.1 % for the loaded phase. Due to unbalanced loading, the output voltage vector, given in Figure 4.22, traces an ellipsoidal route, which reveals the existence of the negative sequence component on the output voltages. The percentage of the UPS output voltage negative sequence component is measured as 9.5 %.

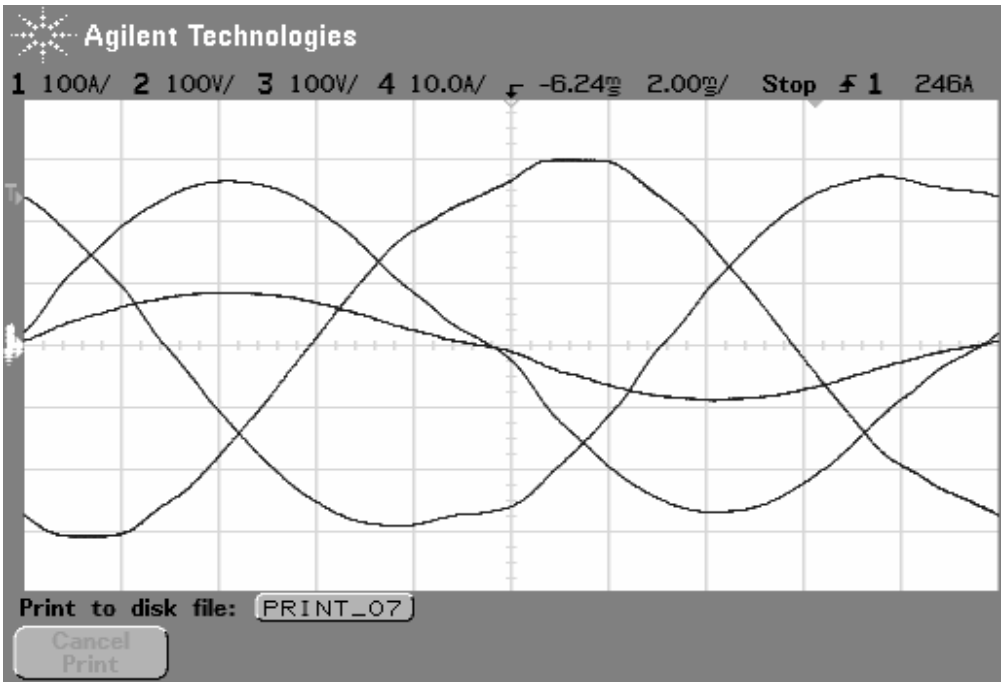

Figure 4.20 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current i_a for open-loop operation at line-to-neutral connected single-phase linear load of 1.3 kVA (Scaling: 100 V/div, 10 A/div, and 2ms/div).

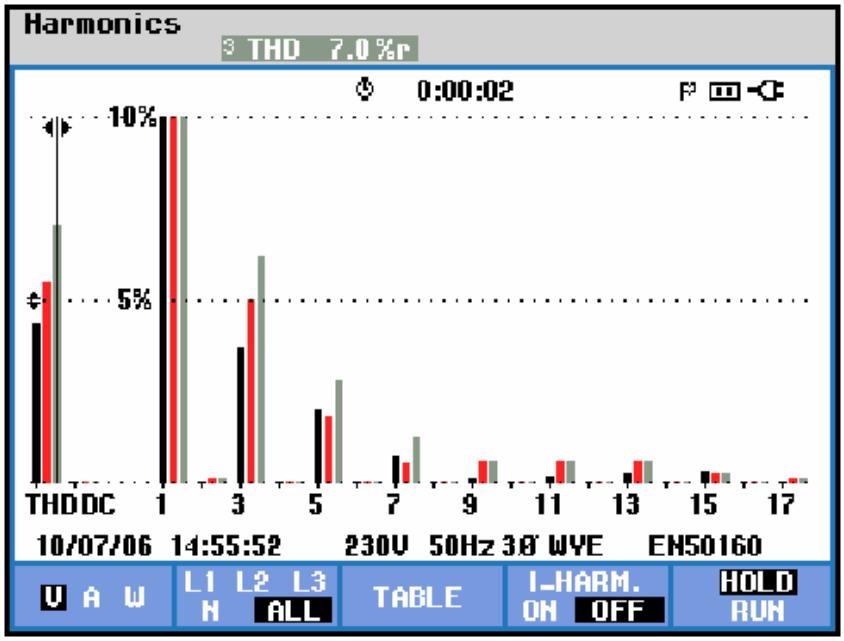

Figure 4.21 Harmonic spectrum of three-phase output voltages for open-loop operation under line-to-neutral connected single-phase linear load of 1.3 kVA.

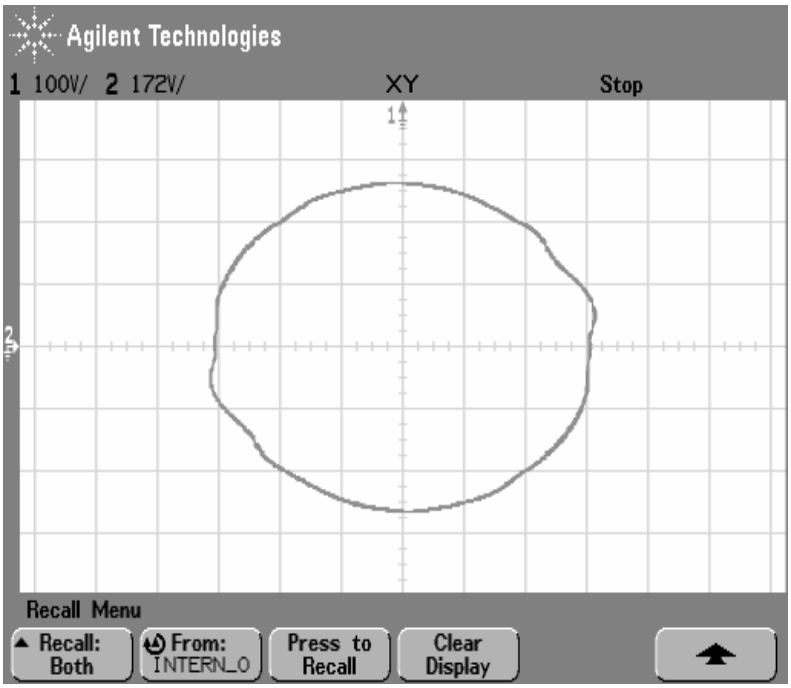

Figure 4.22 Stationary frame vector representation of the output voltages for open-loop operation under line-to-neutral connected single-phase linear load of 1.3 kVA (Scaling: X:100 V/div and Y:172 V/div).

4.3.7 UPS Output Performance Under Line-to-line Unbalanced Linear Load

Open-loop controlled steady-state operation is observed for the UPS with line-to-line unbalanced linear resistive load with 3.3 kW. The resulting waveforms are reported in the following. The three-phase output voltages and the load current for one phase are shown in Figure 4.23. Unbalanced loading causes also the 3rd and 9th harmonics to exist on the output voltages due to the dead-times. The output voltage THD value increases up to 7.6 %. The harmonics spectrum shown in Figure 4.24 contains 3rd, 5th, 7th, 9th, 11th, and 13th harmonics dominantly. The output voltage regulation is 17.3 %. Due to unbalanced loading, the output voltage vector, given in Figure 4.25, traces an ellipsoidal route, which reveals the existence of the negative sequence component on the output voltages. The percentage of the UPS output voltage negative sequence component is measured as 13.1 %.

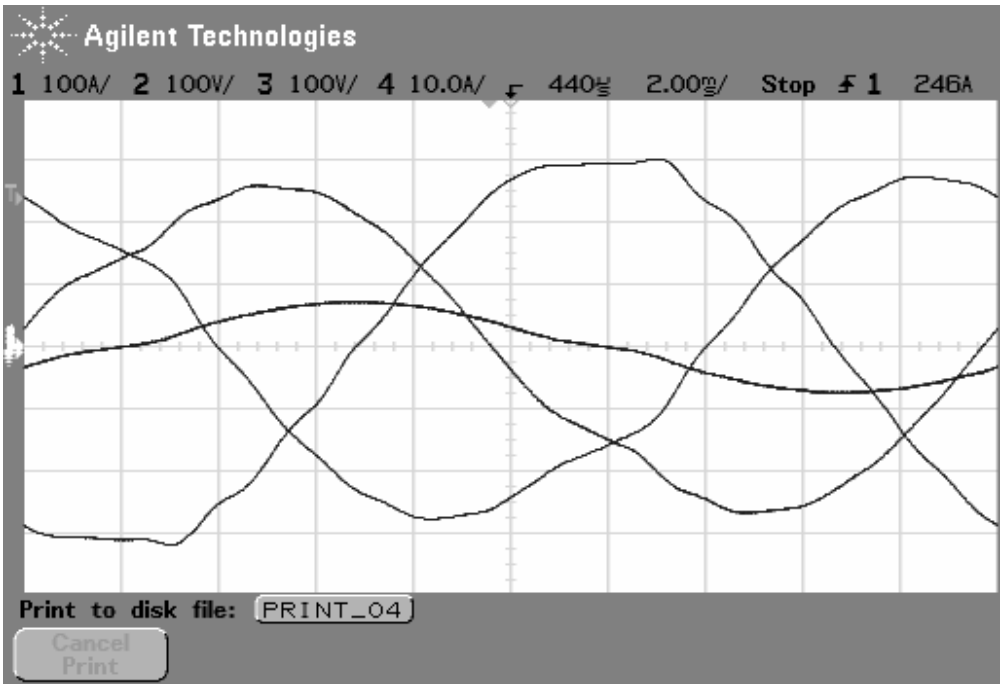

Figure 4.23 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current i_a for open-loop operation under line-to-line connected single-phase linear load of 3 kVA (Scaling: 100 V/div, 10 A/div, and 2ms/div).

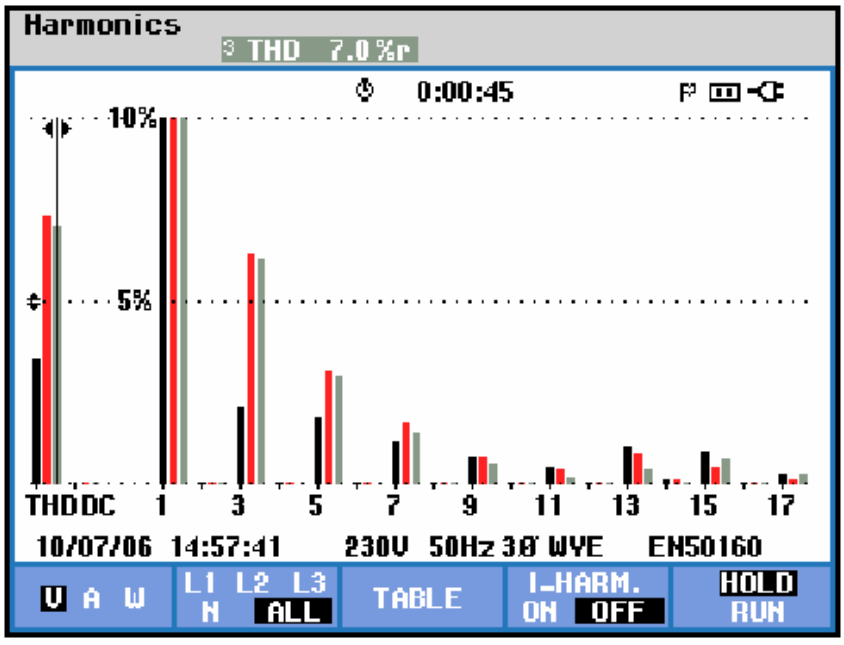

Figure 4.24 Harmonic spectrum of three-phase output voltages for open-loop operation under line-to-line connected single-phase linear load of 3 kVA.

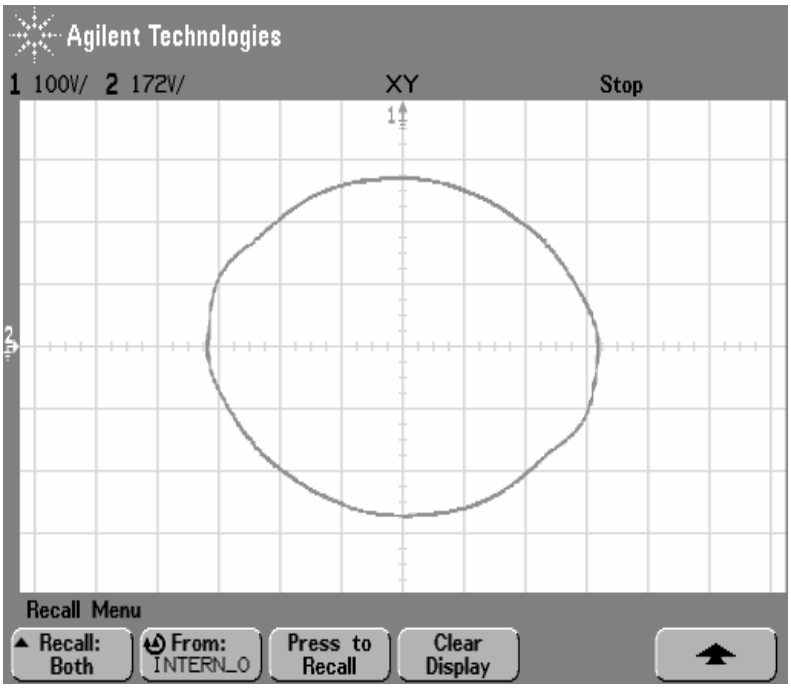

Figure 4.25 Stationary frame vector representation of the output voltages for open-loop operation under line-to-line connected single-phase linear load of 3 kVA (Scaling: X:100 V/div and Y:172 V/div).

4.4 Repetitive Controller Design for UPS Output Voltage Control

The design procedure, given in Section 3.5 of Chapter 3, will be followed. The controller parameters are tuned at operation with balanced nonlinear rated load.

STEP #1: Since the controller was designed for the parameters of the laboratory prototype, the same *S(z)* filter can be employed in the controller structure. As discussed in Chapter 3, the *S(z)* filter was designed as 30^{th} order FIR low-pass filter.

STEP #2: The time delay compensation term was chosen as 5 sampling cycles where the cycle is 100μs corresponding to 10 kHz sampling rate.

STEP #3: The repetitive controller gain was chosen as 0.5 for initial value. This gain will be updated in the following steps.

STEP #4: In order to achieve the best steady-state performance, several integral limiting filter *Q(z)* structures have been experimentally tested. Steady-state performance data of the repetitive controlled UPS system corresponding to the filter structures tested is given in Table 4.3.

Q(z)=0.9: The output voltage THD is reduced to 2.5 % from 10 %. The three-phase output voltages and the load current for one phase are shown in Figure 4.26. The harmonic spectrum given in Figure 4.27 reveals that 5^{th} and 7^{th} harmonics are still at high values. The crest factor of the load current increased to 2.42. The voltage regulation is improved to approximately 1%.

Q(z)=0.95: Increasing the *Q(z)* value decreases the output voltage THD to 1.7 % from 2.5 %. The crest factor of the load current increased to 2.56. the voltage regulation is improved to less than 0.5 %. The figures for this case are not given.

Q(z)=0.98: The output voltage THD is reduced from 1.7 % to 1.3 %. The three-phase output voltages and the load current for one phase are shown in Figure 4.28. The harmonic spectrum given in Figure 4.29 reveals that 5^{th} and 7^{th} harmonics are suppressed more effectively. The crest factor of the load current increased to 2.7. The voltage regulation is improved to less than 0.2 %. In the experiments the *Q(z)* could not be increased beyond 0.98 due to the output voltage stability problems observed during such tests.

Q(z)= $0.25 \cdot z^{-1}+0.5+0.25 \cdot z$: With the low-pass filter structure for *Q(z)* the repetitive controller exhibits excellent performance at low frequencies. The three-phase output voltages and the load current for one phase are shown in Figure 4.30. As shown in Figure 4.31 the low frequency harmonics are suppressed effectively. However the harmonics at the LC filter resonant frequency are weakly suppressed due to the decrease in the integrator gain with increasing frequency. The second order low-pass filter tested has resulted in similar performance to the first order filter. Therefore, the performance indices are reported in Table 3.5 but the waveforms are not shown.

Table 4.3 Experimental steady-state performance data of repetitive controlled UPS system illustrating the effect of *Q(z)*

Control method		THD_V (%)	CF	VR (%)
Open loop controlled		10	1.8	13.5
Q(z) of repetitive controller (K_{rc}=0.5)	*Q(z)*=0.9	2.5	2.42	0.86-1.05
	Q(z)=0.95	1.7	2.56	0.27-0.45
	Q(z)=0.98	1.3	2.7	0-0.13
	$Q(z)= 0.25\cdot z^{-1}+0.5+0.25\cdot z$	1.6	2.7	0.13-0.18
	$Q(z)= -0.0127\cdot z^{-2}+0.14578\cdot z^{-1}+0.7338+0.14578\cdot z-0.0127\cdot z^{2}$	1.3	2.8	0-0.18

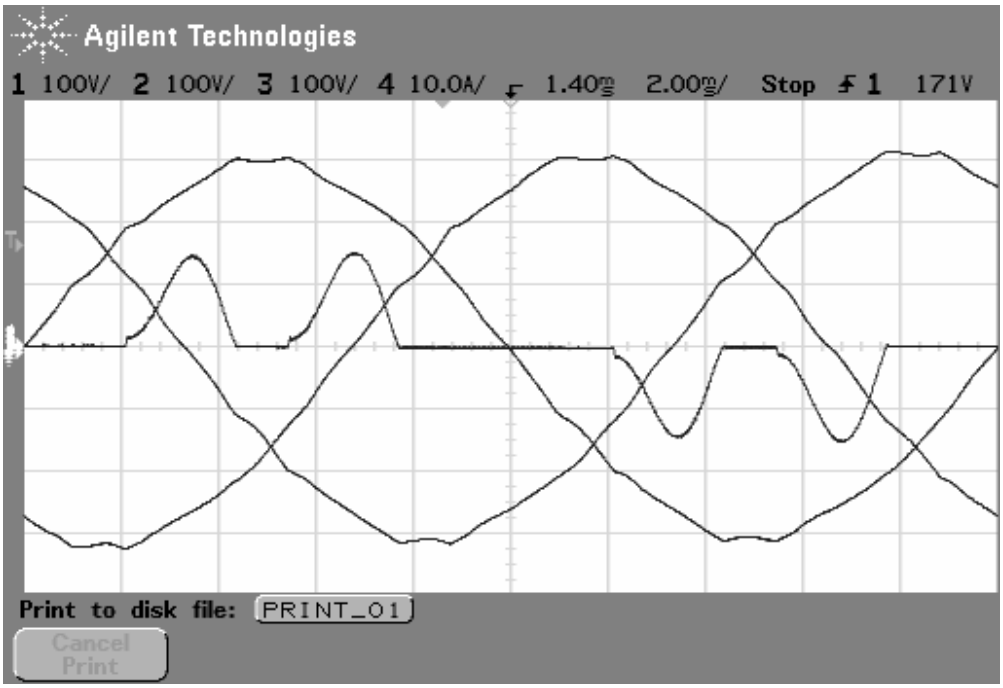

Figure 4.26 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) load current (i_a) for repetitive control with $Q(z)$=0.9 (Scaling: 100 V/div, 10 A/div, and 2ms/div).

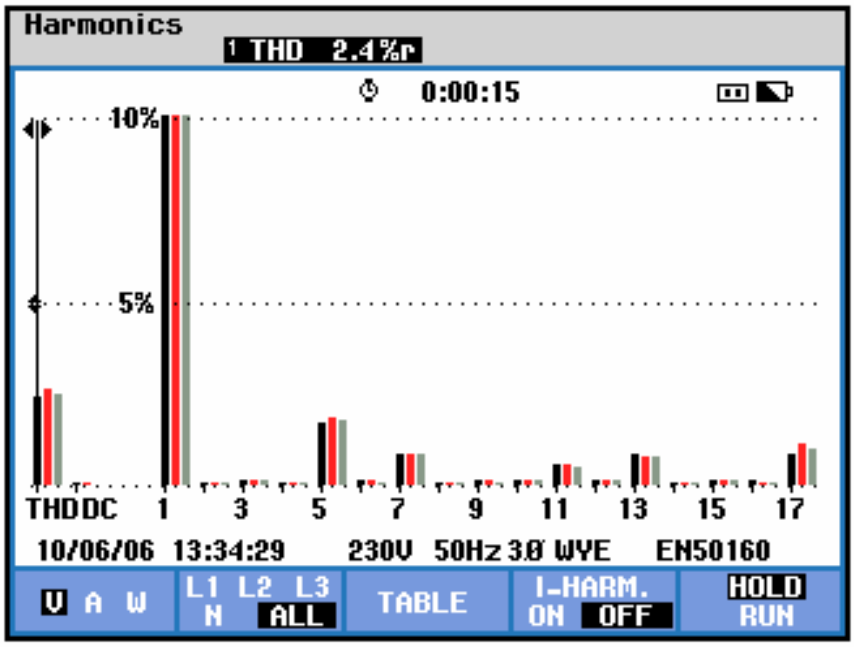

Figure 4.27 Harmonic spectrum of three-phase output voltages for $Q(z)$=0.9.

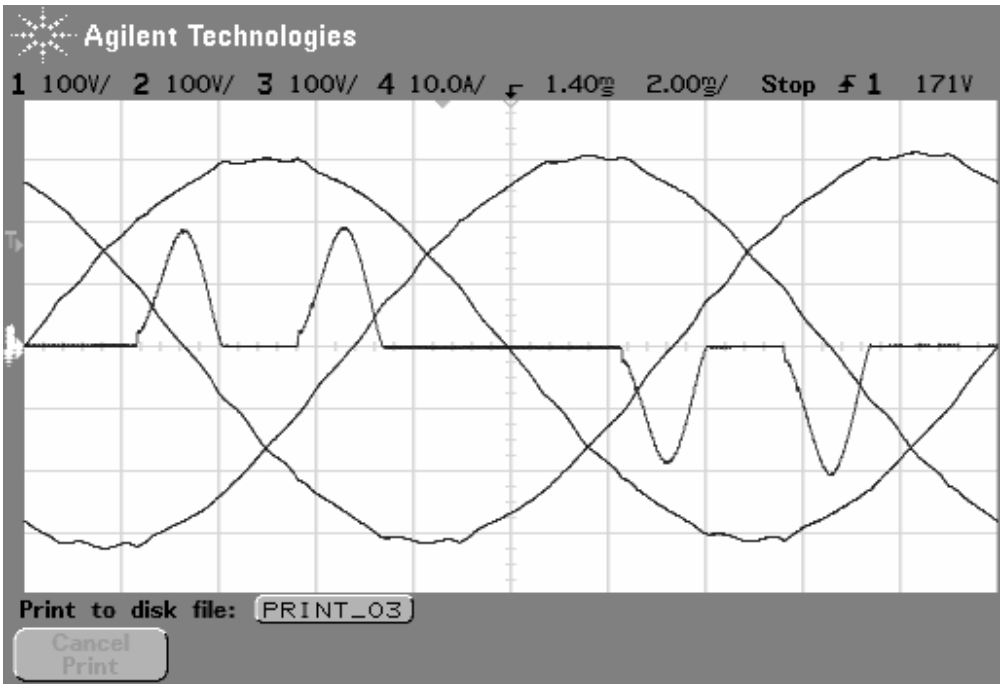

Figure 4.28 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) load current (i_a) for $Q(z)$=0.98 (Scaling: 100 V/div, 10 A/div, and 2ms/div).

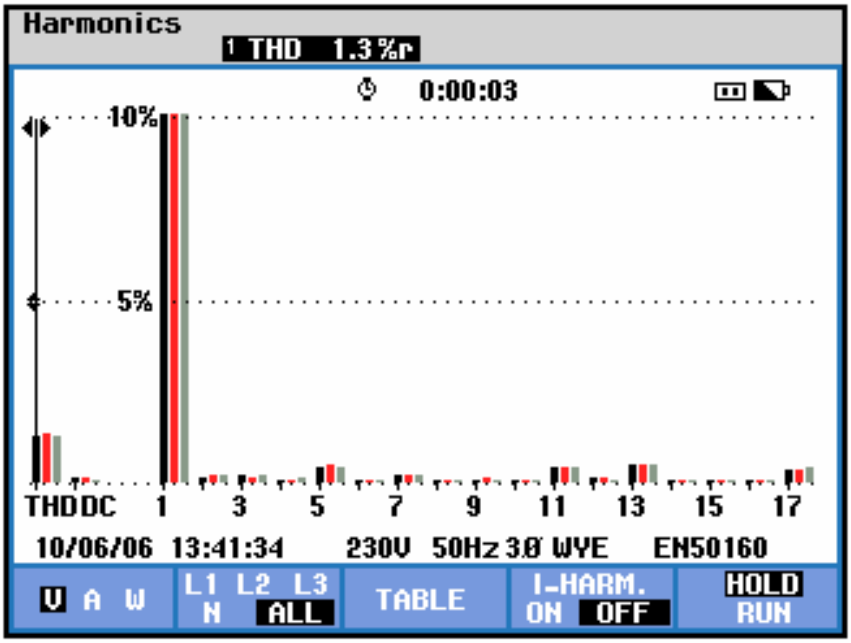

Figure 4.29 Harmonic spectrum of three-phase output voltages for $Q(z)$=0.98.

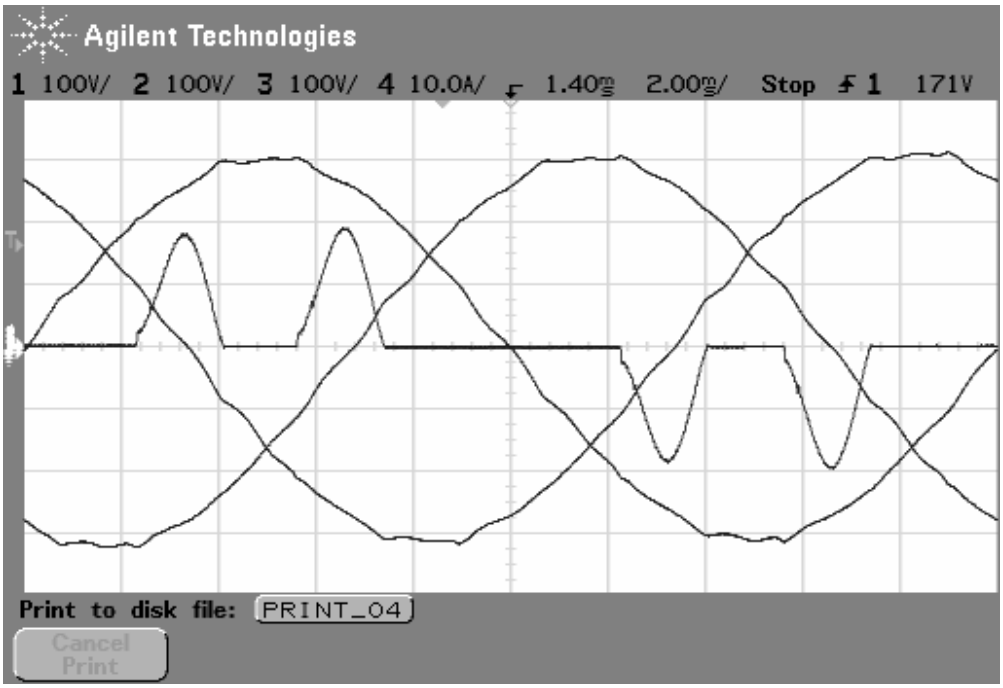

Figure 4.30 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) load current (i_a) for $Q(z)= 0.25z^{-1}+0.5+0.25z$ (Scaling: 100 V/div, 10 A/div, and 2ms/div).

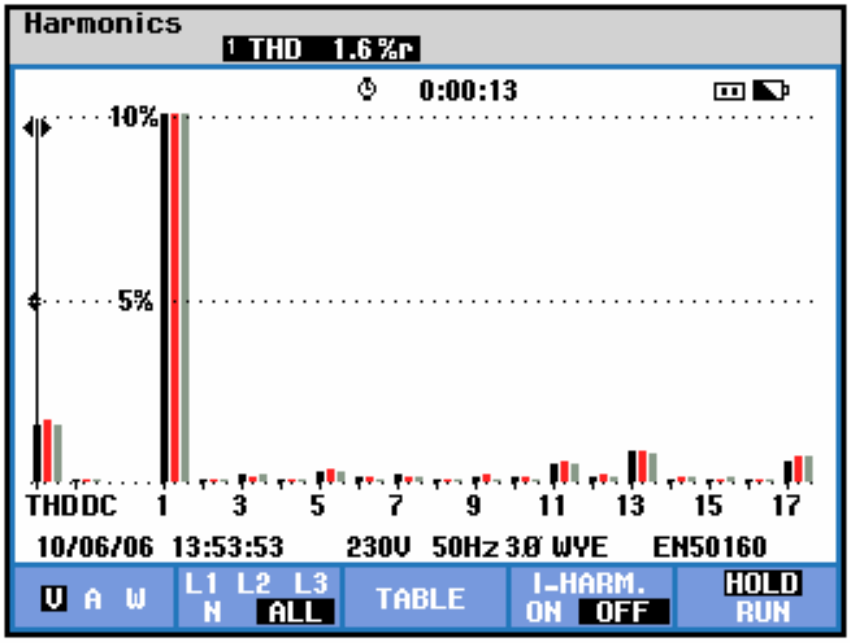

Figure 4.31 Harmonic spectrum of three-phase output voltages for $Q(z)= 0.25z^{-1}+0.5+0.25z$.

STEP #5: *Q(z)* is chosen as 0.98 and the design is followed by the design of the complementary terms in the controller. Capacitor current feedback is added in the controller structure for achieving active damping. The gain is chosen 15, the same as in the simulations. With better rejection of the harmonics at high frequencies, output voltage THD is reduced to 1.0 %. And the crest factor is increased to 2.8 from 2.7.

STEP #6: The repetitive controller gain is increased to 0.57 for faster response and better harmonic rejection. Increase in the repetitive controller gain improves the regulation of the UPS output voltages to 0.36 from 0.68.

STEP #7: A proportional gain of 0.8 for the output voltage control is added in the control structure. The regulation of the UPS output voltages is improved. The output voltage THD is increased by a negligible amount.

With the last step completed, the controller design is concluded. The UPS performance for design steps 5, 6, and 7 is summarized in Table 4.4. The steady-state performance of the designed controller will be evaluated experimentally in the following.

Table 4. 4 Experimental steady-state performance data of repetitive controlled UPS system illustrating the performance for the gains in steps 5, 6, and 7

Control method		THD_V (%)	CF	VR (%)
$Q(z)$=0.98	K_{ad}=15 added	1.0	2.8	0.59-0.68
	K_{rc}=0.57 (increased)	1.0	2.81	0.22-0.36
	K_{pv}=0.8 added	1.1	2.85	0.13-0.22

4.5 Steady-state Performance Evaluation of The Repetitive Controlled UPS

In this section, the steady-state operating performance of the repetitive controlled UPS system will be evaluated for several load types. The controller structure is the same as the final structure obtained during the design stage, of which the parameters are listed in Table 4.5. In the following study, first the different loading cases will be investigated individually and then the results will be cumulatively shown in a table.

Table 4.5 steady-state performance data of the repetitive controlled UPS

		Linear load		Nonlinear load	
		Open-loop	Rep. Cont.	Open-loop	Rep. Cont.
No-load	THD_V	1.5	0.6		
	V_{max}	221.4	220		
	V_{min}	219.5	219.7		
	V_{neg}	0.5	0.1		
	V_{zero}	0	0		
	VR (%)	0.2	0.1		
Balanced load	THD_V	4.3	0.4	10	1.1
	CF	1.44	1.42	1.78	2.76-2.88
	V_{max}	184.8	219.3	191.6	220.7
	V_{min}	184.4	219.1	191	220.3
	V_{neg}	0.1	0.1	0.2	0.1
	V_{zero}	0	0	0	0
	A_{neg}	0.6	0.5	0.6	3.4
	A_{zero}	0.6	0.6	0.1	0.3
	VR(%)	16.7	0.4	13.0	0.2
Line-to-neutral unbalanced load	THD_V	5.2-7.3	0.4	1.6-6.0-7.7	1.6-1.8
	CF	1.48	1.42	2.6	3.46
	V_{max}	214	220.5	220	220
	V_{min}	180	218.2	202	218.7
	V_{neg}	9.5	0.1	4.9	0.1
	V_{zero}	0.7	0.8	0.3	0.4
	A_{neg}	99.8	99.8	100	100
	A_{zero}	102	102	99.3	99.5
	VR(%)	18.1	0.4	8.0	0.6
Line-to-line unbalanced load	THD_V	3.6-7.6	0.5	4.4-7.8-11.4	0.8
	CF	1.38-1.45	1.42	2.44	3.9
	V_{max}	223	220.8	223.5	220.1
	V_{min}	182	219.4	194.6	220.8
	V_{neg}	13.1	0.4	8.2	0.2
	V_{zero}	0	0	0	0
	A_{neg}	99.7	99.7	99.8	99.9
	A_{zero}	0.5	0	0.2	0.2
	VR(%)	17.3	0.3	11.5	0.4

4.5.1 UPS Output Performance Under Balanced Nonlinear Load

Operation of the UPS under balanced nonlinear full load is observed experimentally. The output voltages of the repetitive controlled UPS and one-phase load current are given in Figure 4.32. The harmonic spectrum, given in Figure 4.33, reveals that harmonics are successfully eliminated when compared to open-loop controlled case (Figure 4.2). The UPS output voltage vector, given in Figure 4.34, traces an almost circular route with the elimination of output voltage harmonics. The output voltage THD is reduced to 1.1 % and the regulation is improved to 0.2 %.

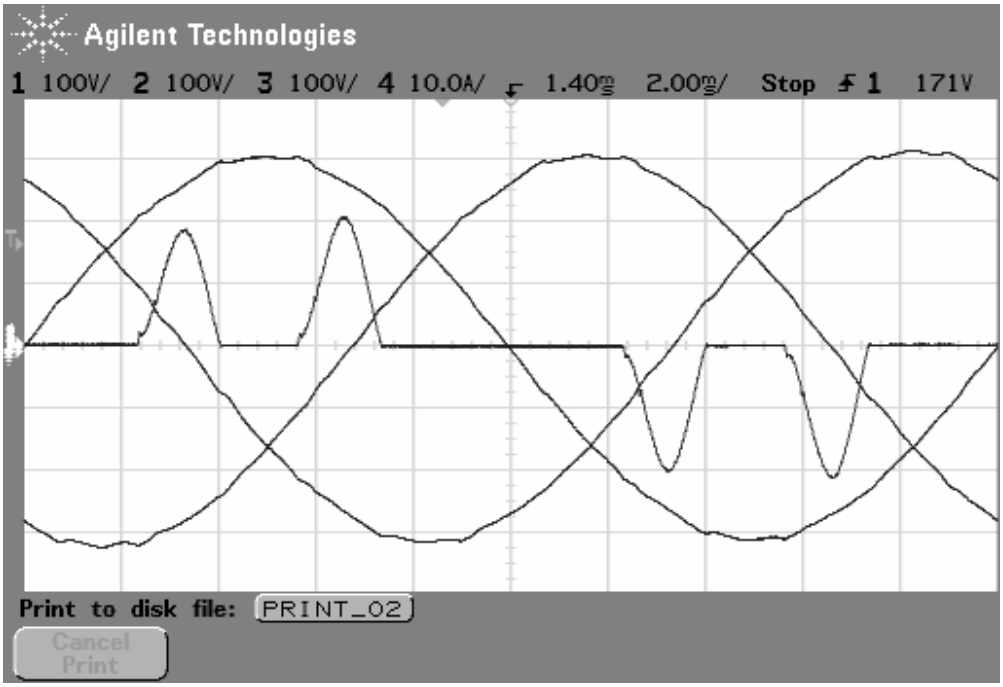

Figure 4.32 UPS output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current (i_a) for repetitive control with balanced nonlinear load
(Scaling: 100 V/div, 10 A/div, and 2ms/div).

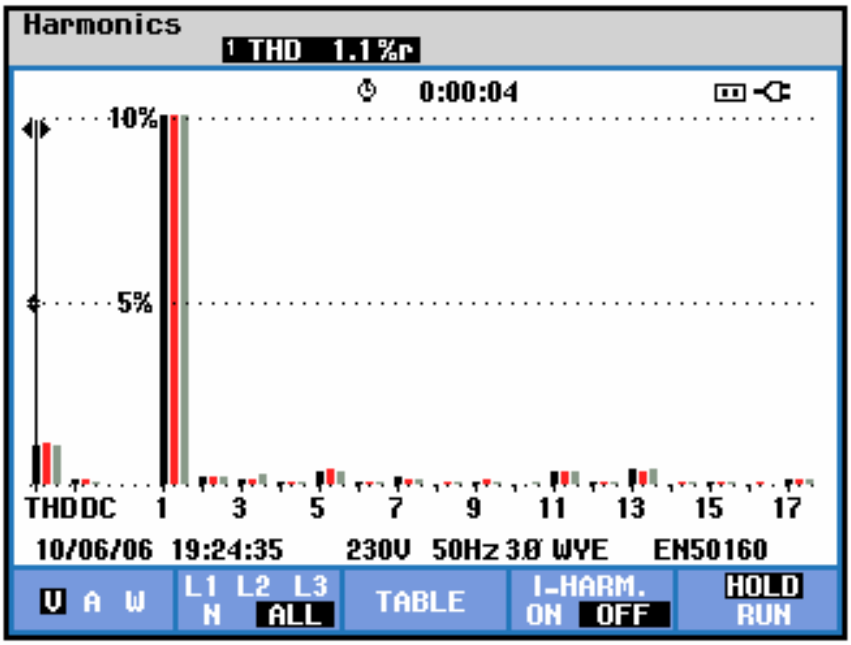

Figure 4.33 Harmonic spectrum of the line-to-neutral output voltages for repetitive control with balanced nonlinear load.

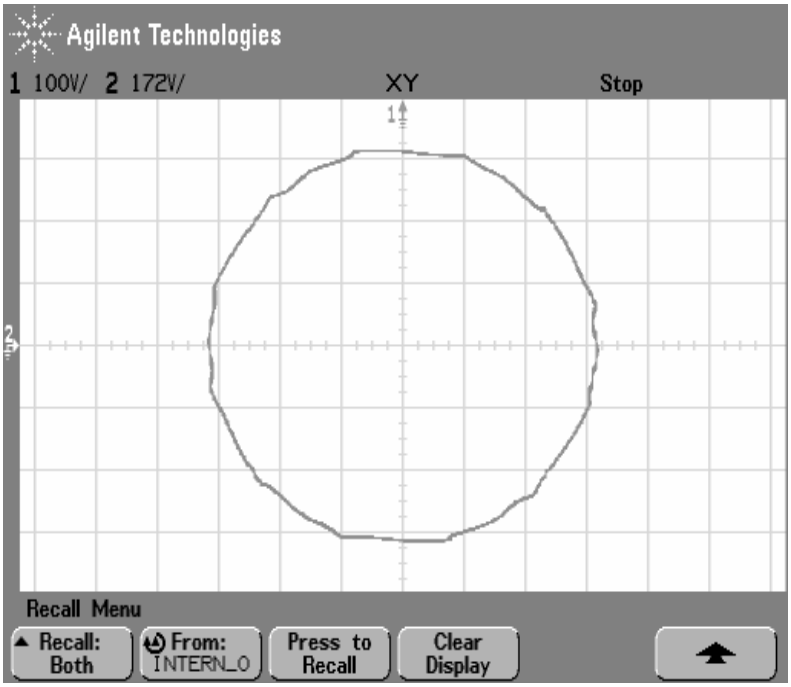

Figure 4.34 Stationary frame vector representation of the output voltages for closed-loop operation at three-phase diode rectifier of 5 kVA (Scaling: X:100 V/div and Y:172 V/div).

4.5.2 UPS Output Performance Under Single-Phase Unbalanced Nonlinear Load

Operation of UPS under line-to-neutral connected single-phase unbalanced nonlinear load is observed experimentally. The output voltages of the repetitive controlled UPS and one-phase load current is given in Figure 4.35. The harmonic spectrum, given in Figure 4.36, reveals that harmonics, except the zero sequence harmonics, are successfully eliminated when compared to open-loop controlled case (Figure 4.5). The UPS output voltage vector, given in Figure 4.37, traces an almost circular route with the elimination of output voltage harmonics. The output voltage THD is reduced to 1.8 % and the regulation is improved to 0.6 %.

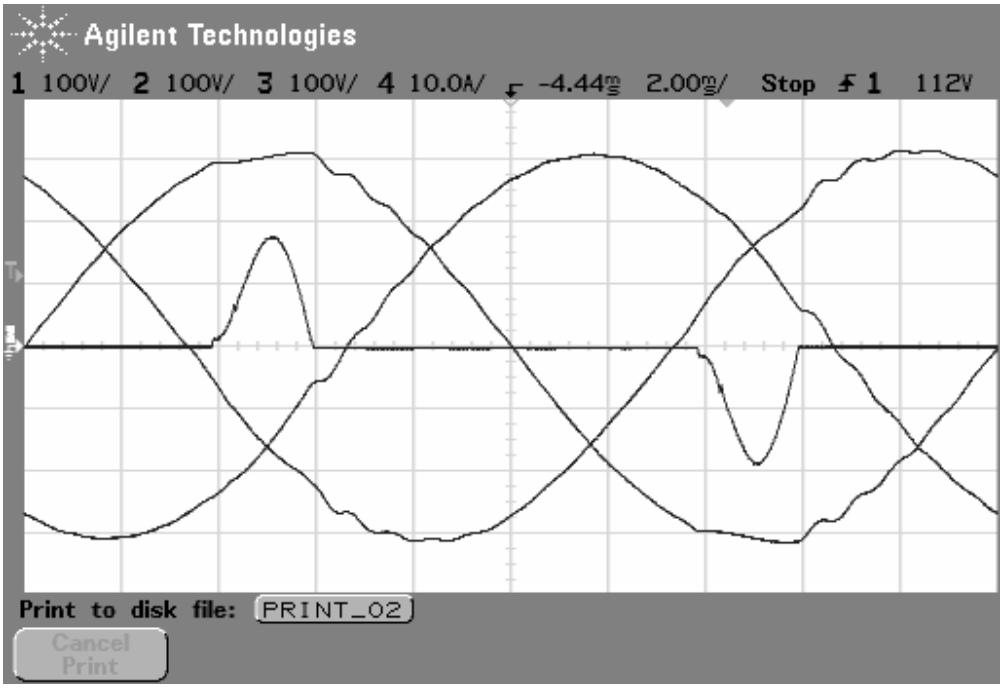

Figure 4.35 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current i_a for closed-loop operation under line-to-neutral connected single-phase linear load of 1.3 kVA (Scaling: 100 V/div, 10 A/div, and 2ms/div).

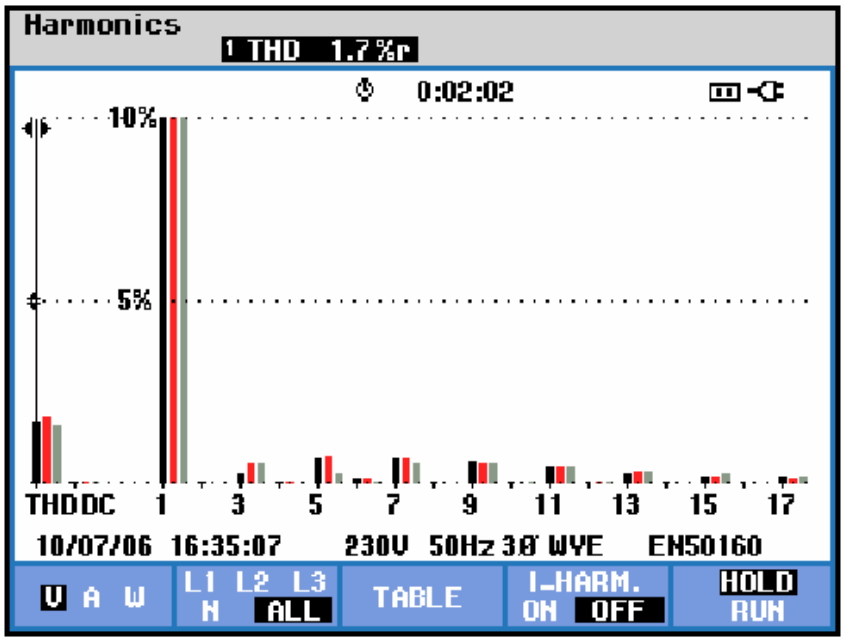

Figure 4.36 Harmonic spectrum of three-phase output voltages for closed-loop operation under line-to-neutral connected single-phase diode rectifier load of 1.3 kVA.

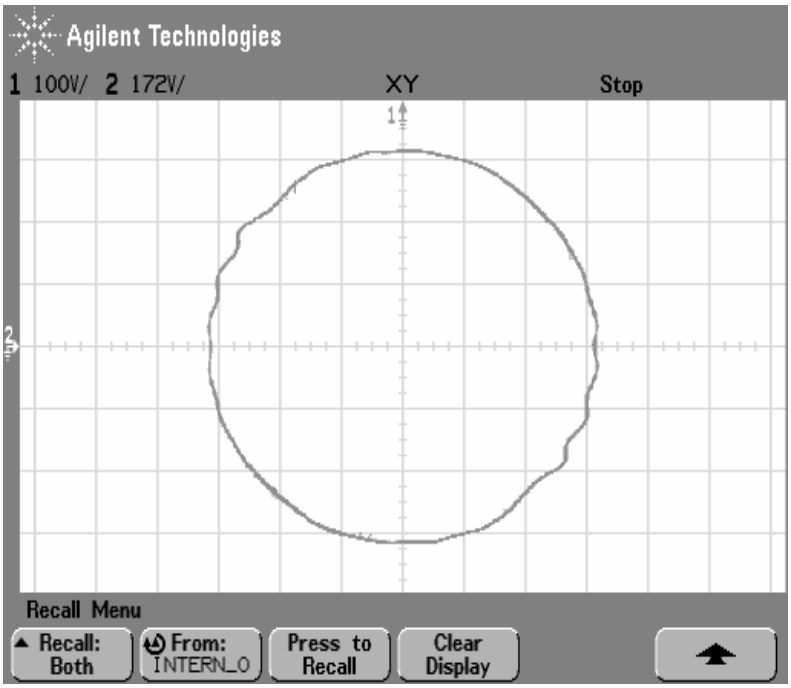

Figure 4.37 Stationary frame vector representation of the output voltages for closed-loop operation under line-to-neutral connected single-phase diode rectifier of 1.3 kVA (Scaling: X:100 V/div and Y:172 V/div).

4.5.3 UPS Output Performance Under Line-to-line Unbalanced Nonlinear Load

Operation of UPS under line-to-line connected single-phase unbalanced nonlinear load is observed experimentally. The output voltages of the repetitive controlled UPS and one-phase load current is given in Figure 4.38. The harmonic spectrum, given in Figure 4.39, shows that harmonics are successfully eliminated when compared to open-loop controlled case (Figure 4.8). The UPS output voltage vector, given in Figure 4.40, traces an almost circular route with the elimination of output voltage harmonics. The output voltage THD is reduced to 0.7 % and the regulation is improved to 0.4 %.

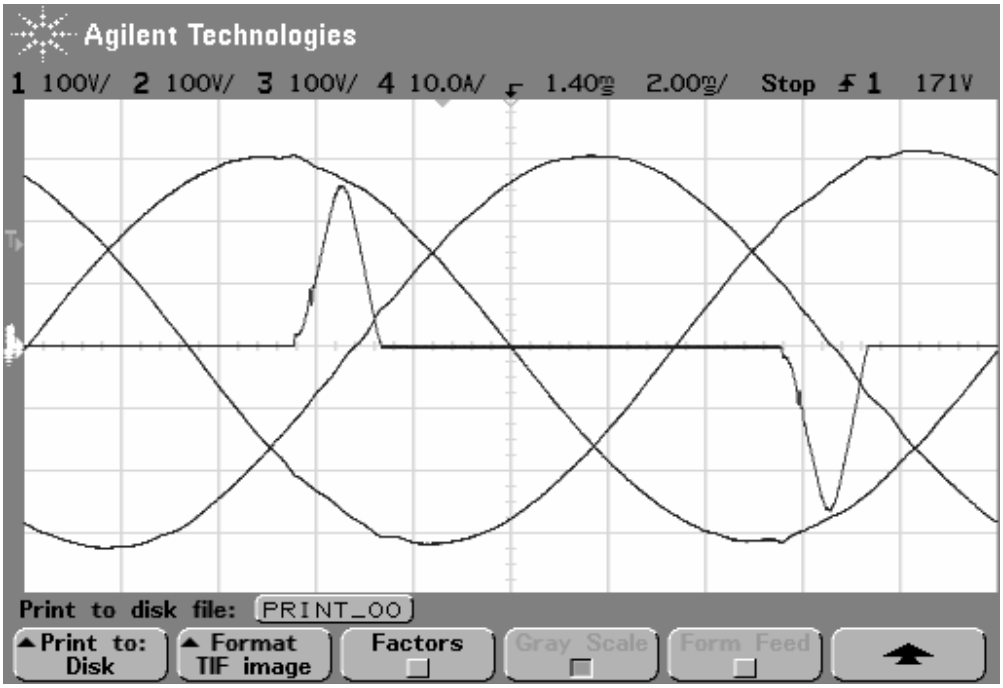

Figure 4.38 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current i_a for closed-loop operation under line-to-line connected single-phase diode rectifier of 3 kVA (Scaling: 100 V/div, 10 A/div, and 2ms/div).

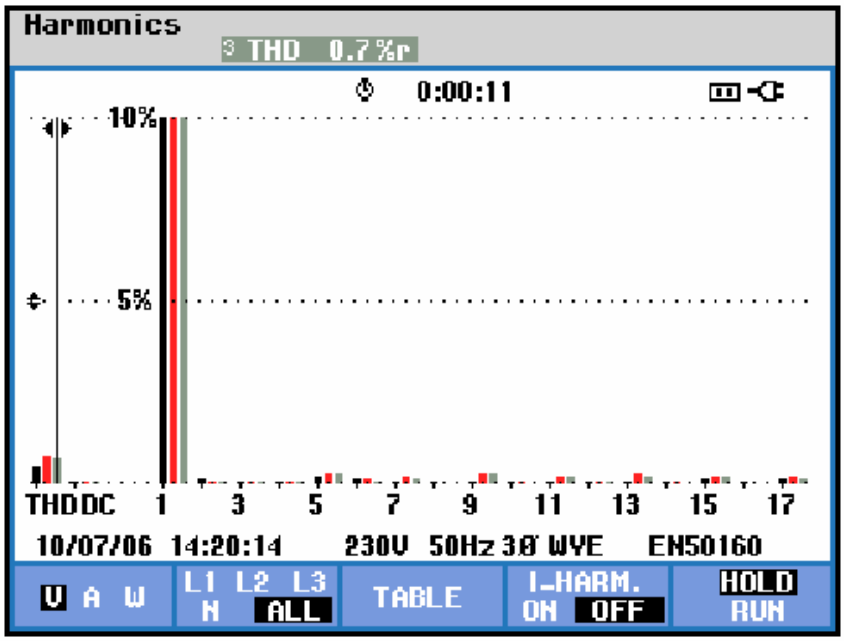

Figure 4.39 Harmonic spectrum of three-phase output voltages for closed loop operation under line-to-line connected single-phase diode rectifier of 3 kVA.

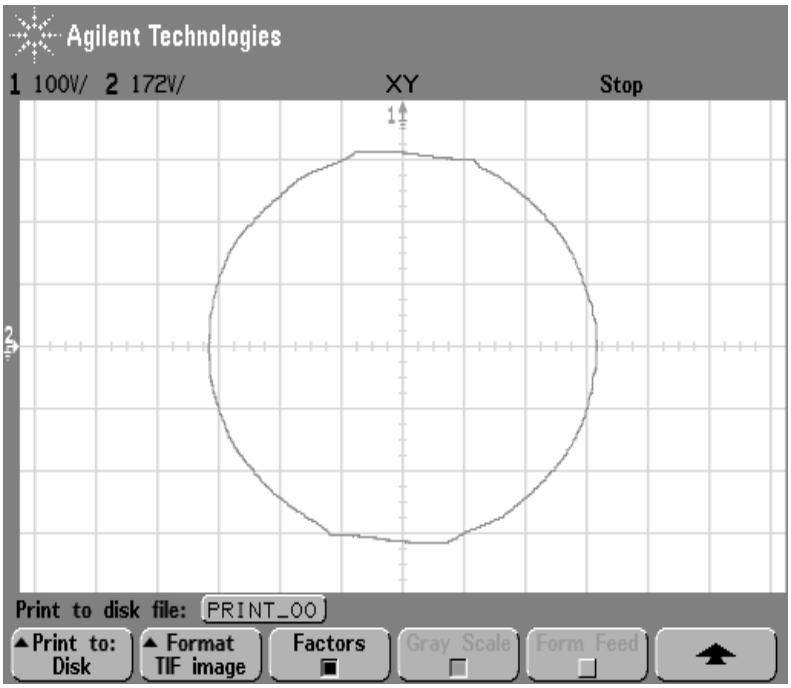

Figure 4.40 Stationary frame vector representation of the output voltages for closed-loop operation under line-to-line connected single-phase diode rectifier of 3 kVA (Scaling: X:100 V/div and Y:172 V/div).

4.5.4 UPS Output Performance Under No-Load

Operation of UPS no-load is observed experimentally. The output voltages of the repetitive controlled UPS and one-phase load current is given in Figure 4.41. The harmonic spectrum, given in Figure 4.42, reveals that harmonics, which stem from nonlinearity of the inverter, are successfully eliminated when compared to open-loop controlled case (Figure 4.11). The UPS output voltage vector, given in Figure 4.43, traces a perfect circular route with the elimination of output voltage harmonics. The output voltage THD is reduced to 0.4 %.

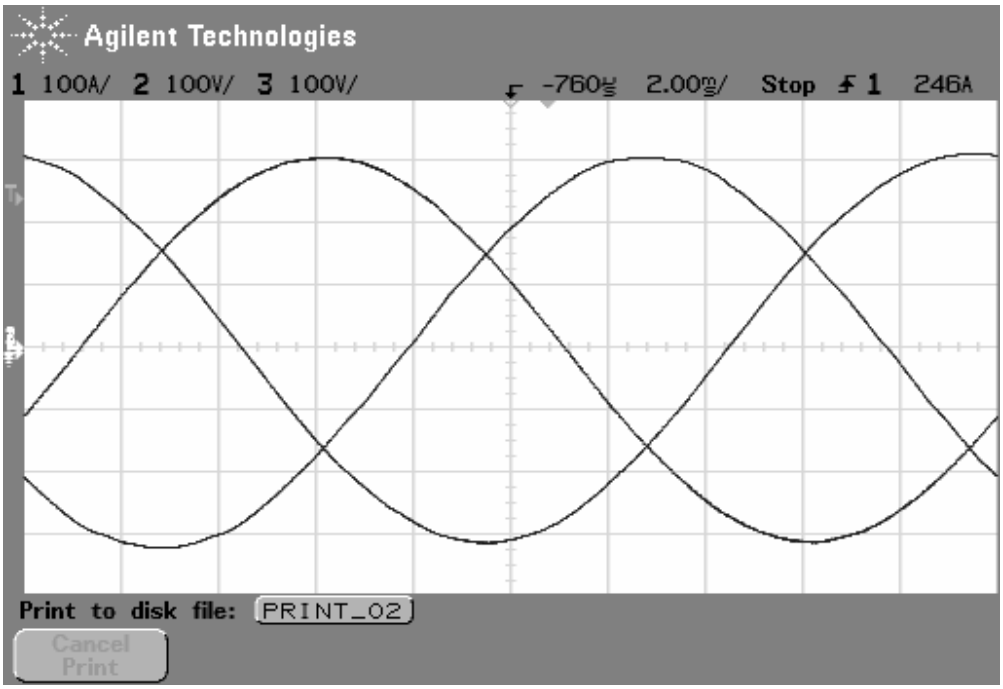

Figure 4.41 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) for closed-loop operation at no-load (Scaling: 100 V/div and 2ms/div).

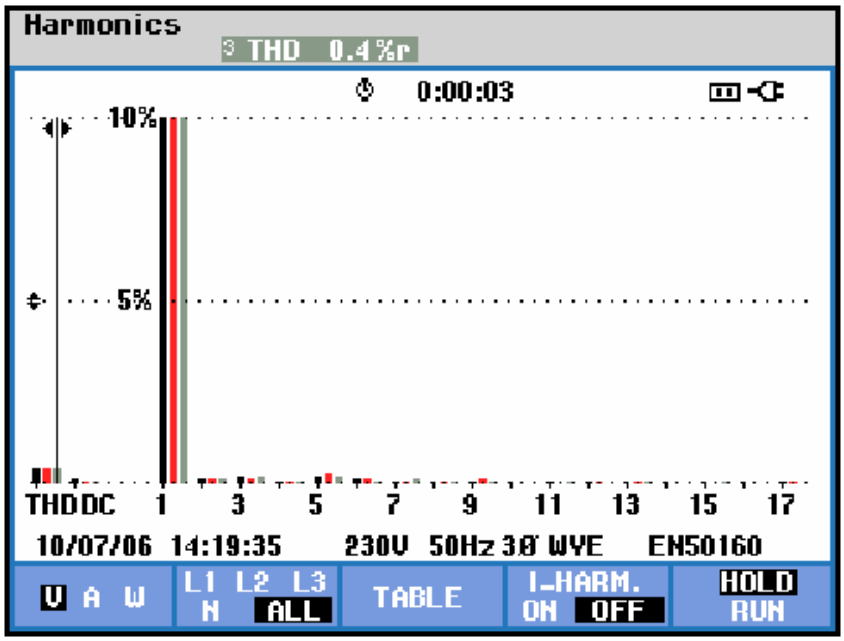

Figure 4.42 Harmonic spectrum of three-phase output voltages for closed-loop operation at no-load.

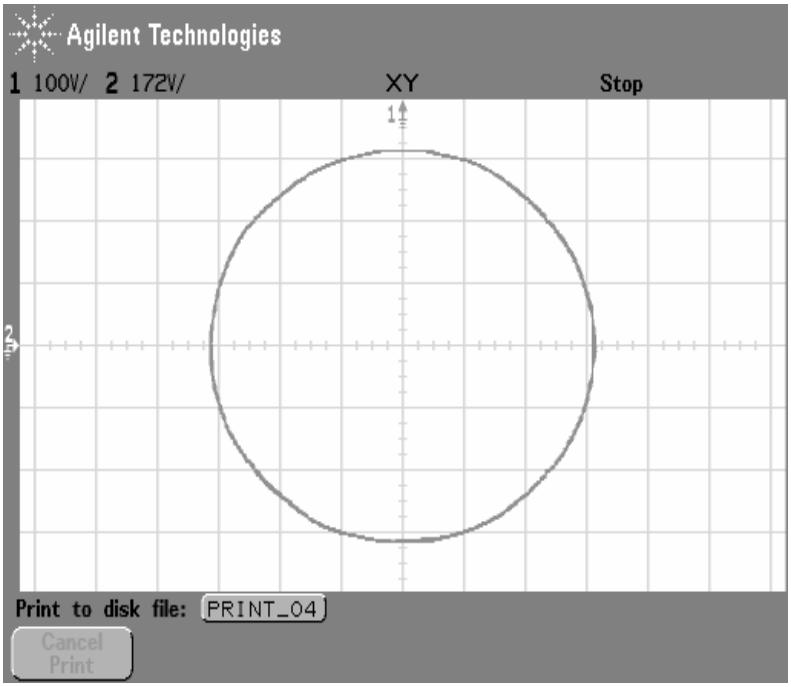

Figure 4.43 Stationary frame vector representation of the output voltages for closed-loop operation at no-load (Scaling: X:100 V/div and Y:172 V/div).

4.5.5 UPS Output Performance Under Balanced Linear Load

Operation of UPS under three-phase balanced linear load is observed experimentally. The output voltages of the repetitive controlled UPS and one-phase load current is given in Figure 4.44. The harmonic spectrum, given in Figure 4.45, reveals that harmonics, which stem from nonlinearity of the inverter, are successfully eliminated when compared to open-loop controlled case (Figure 4.18). The UPS output voltage vector, given in Figure 4.46, traces an almost circular route with the elimination of output voltage harmonics. The output voltage THD is reduced to 0.5 % and the regulation is improved to 0.4 % from 16.7 %.

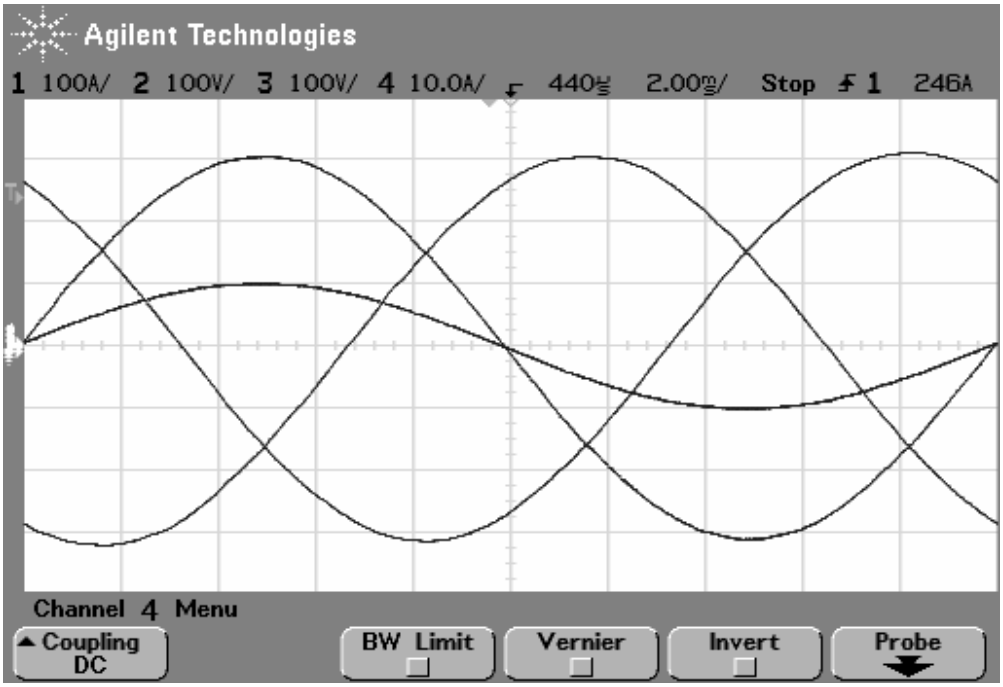

Figure 4.44 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current i_a for closed-loop operation under three-phase balanced linear load of 5 kVA (Scaling: 100 V/div, 10 A/div, and 2ms/div).

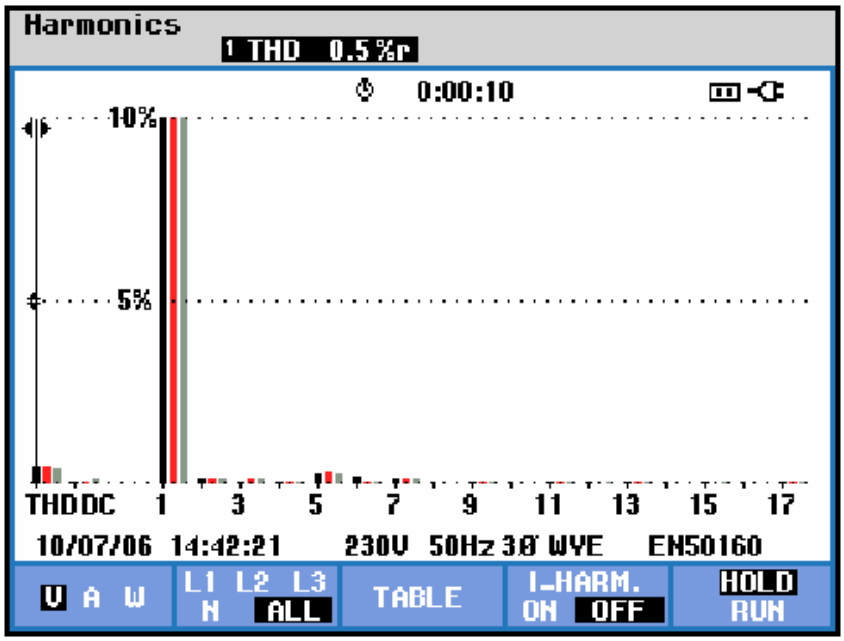

Figure 4.45 Harmonic spectrum of three-phase output voltages for closed-loop operation under three-phase balanced linear load of 5 kVA.

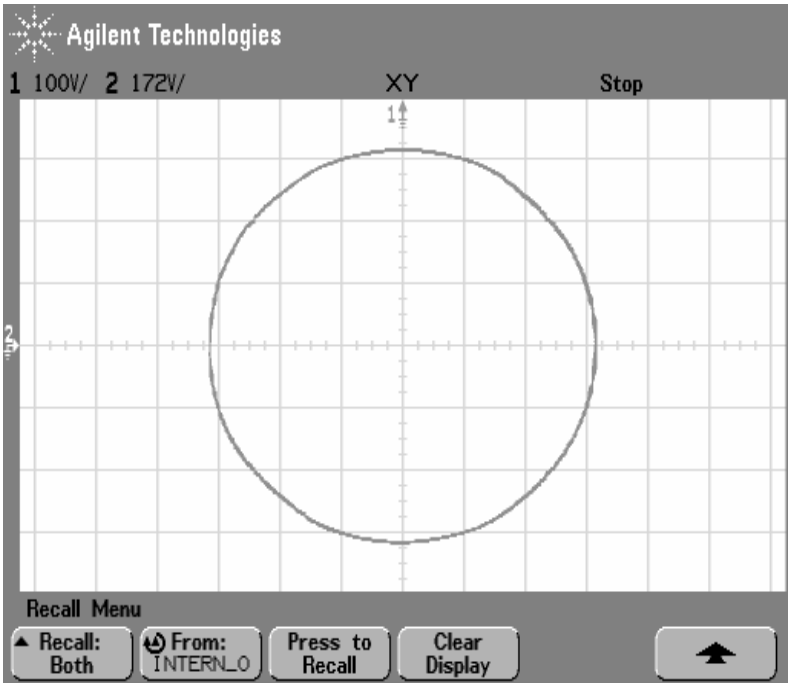

Figure 4.46 Stationary frame vector representation of the output voltages for closed-loop operation under three-phase balanced linear load of 5 kVA (Scaling: X:100 V/div and Y:172 V/div).

4.5.6 UPS Output Performance Under Single-Phase Unbalanced Linear Load

Operation of UPS under line-to-line connected single-phase unbalanced linear load is observed experimentally. The output voltages of the repetitive controlled UPS and one-phase load current is given in Figure 4.47. The harmonic spectrum, given in Figure 4.48, reveals that harmonics, which stem from nonlinearity of the inverter, are successfully eliminated when compared to open-loop controlled case (Figure 4.21). The UPS output voltage vector, given in Figure 4.49, traces an almost circular route with the elimination of output voltage harmonics. The output voltage THD is reduced to 0.5 % from 7.3 % and the regulation is improved to 0.4 % from 18.1 %.

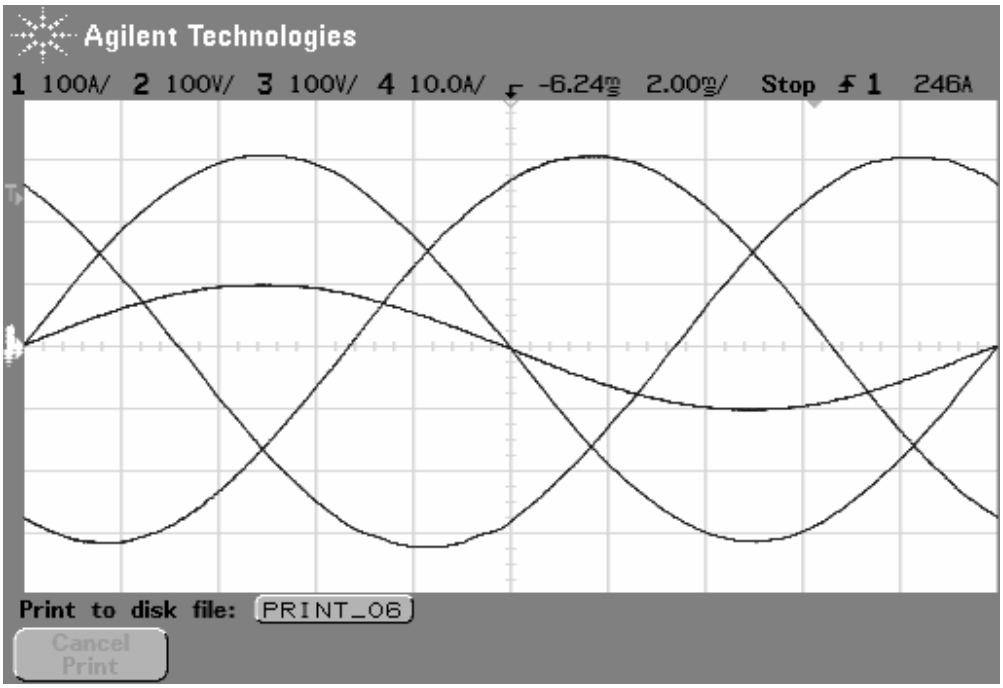

Figure 4.47 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current i_a for closed-loop operation under line-to-neutral connected single-phase linear load of 1.3 kVA (Scaling: 100 V/div, 10 A/div, and 2ms/div).

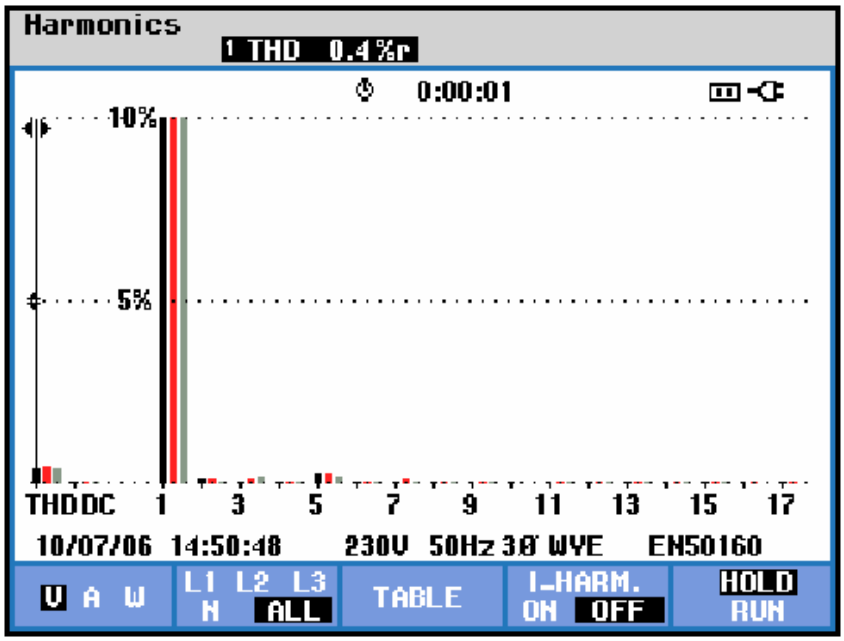

Figure 4.48 Harmonic spectrum of three-phase output voltages for closed-loop operation under line-to-neutral connected single-phase linear load of 1.3 kVA.

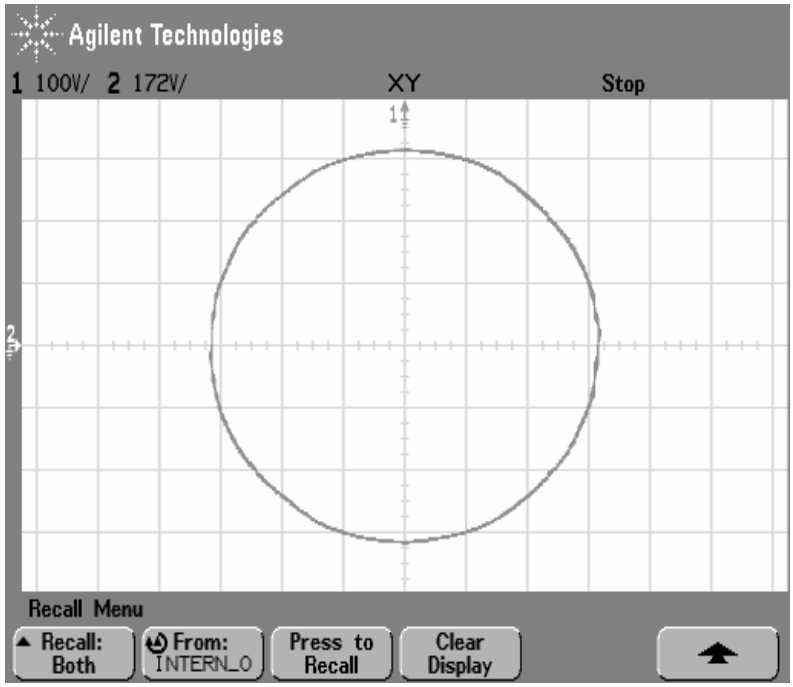

Figure 4.49 Stationary frame vector representation of the output voltages for closed loop operation under line-to-neutral connected single-phase linear load of 1.3 kVA (Scaling: X:100 V/div and 172 V/div).

4.5.7 UPS Output Performance Under Line-to-line Unbalanced Nonlinear Load

Operation of UPS under line-to-line connected single-phase unbalanced linear load is observed experimentally. The output voltages of the repetitive controlled UPS and one-phase load current is given in Figure 4.50. The harmonic spectrum, given in Figure 4.51, reveals that harmonics, which stem from nonlinearity of the inverter, are successfully eliminated when compared to open-loop controlled case (Figure 4.24). The UPS output voltage vector, given in Figure 4.52, traces an almost circular route with the elimination of output voltage harmonics. The output voltage THD is reduced to 0.5 % from 7.6 % and the regulation is improved to 0.3 % from 17.3 %.

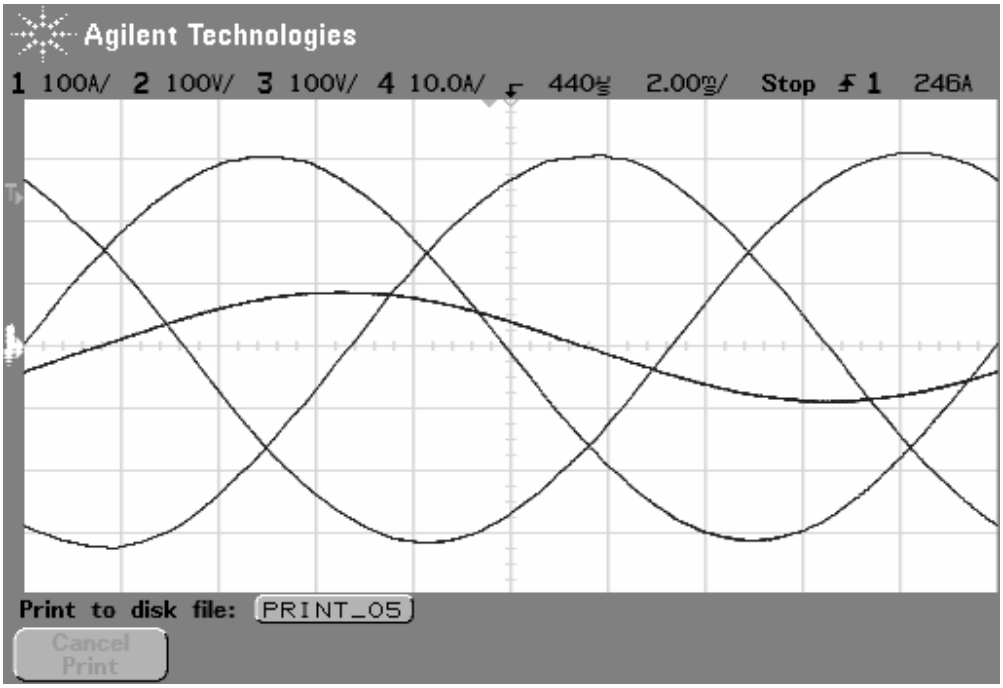

Figure 4.50 Output line-to-neutral voltages (v_{an}, v_{bn}, and v_{cn}) and load current i_a for closed-loop operation under line-to-line connected single-phase linear load of 3 kVA (Scaling: 100 V/div, 10 A/div, and 2ms/div).

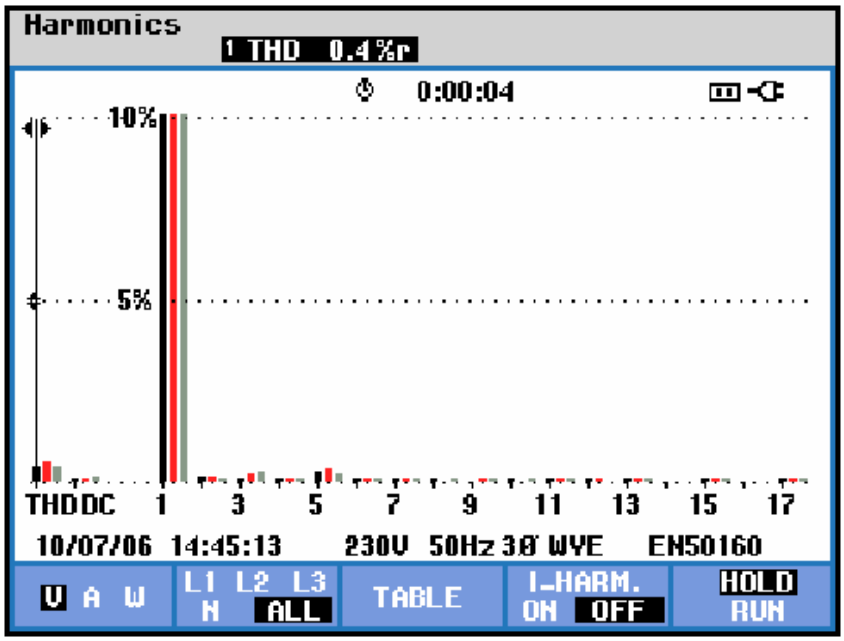

Figure 4.51 Harmonic spectrum of three-phase output voltages for closed-loop operation under line-to-line connected single-phase linear load of 3 kVA.

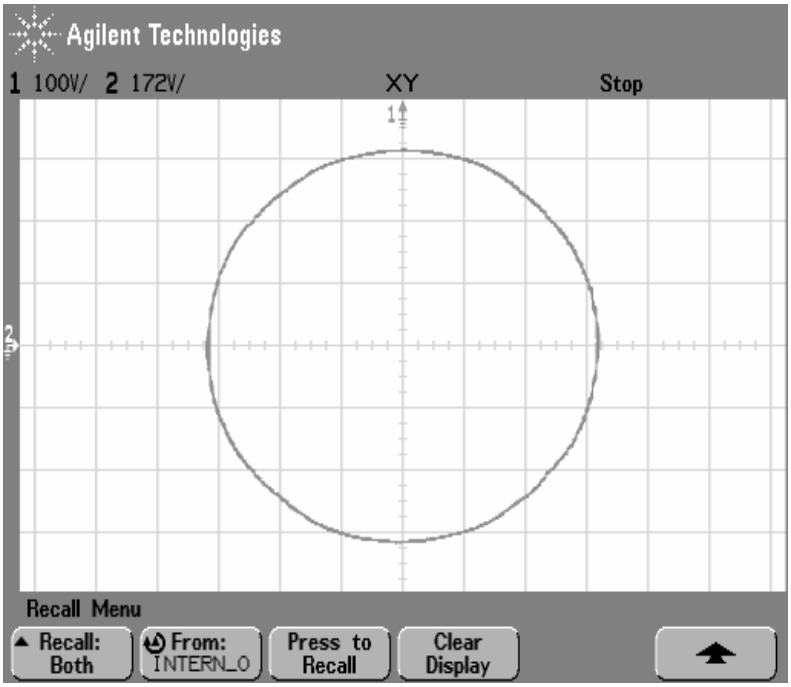

Figure 4.52 Stationary frame vector representation of the output voltages for closed-loop operation under line-to-line connected single-phase linear load of 3 kVA (Scaling: 100 V/div and 172 V/div).

4.6 Dynamic Performance Evaluation of The Repetitive Controlled UPS

In order to evaluate the dynamic performance of the designed controller, the UPS is loaded from no-load to balanced linear resistive full-load. Figure 4.53 shows the open-loop operated UPS dynamic performance. The response is poor.

When the capacitor current feedback is employed in the control structure, system is more damped. As shown in Figure 4.54, the loading transient oscillations are suppressed. However the UPS output voltage can not achieve the rated rms value.

By employing proportional gain for output voltage controller, the regulation partially improves (Figure 4.55). The time duration at which the output voltage collapses is decreased with proportional controller.

The dynamic performance study results are in strong correlation with the theory and the computer simulation results.

In this chapter, the theory of Chapter 2 and the computer simulations of Chapter 3 are verified with the experimental study and it has been shown that the results highly correlate. As a result it has been shown that the repetitive controller with additional control blocks performs satisfactorily under steady-state and dynamic loading conditions for various load types.

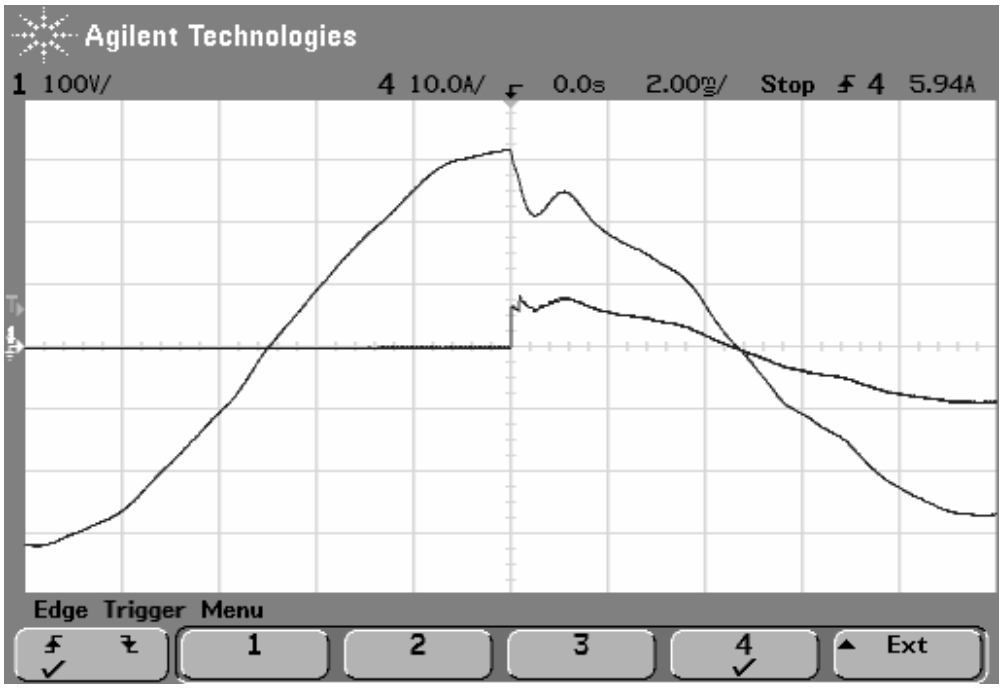

Figure 4.53 One phase output voltage (v_{an}) and load current (i_a) under loading transient for open-loop controlled operation.

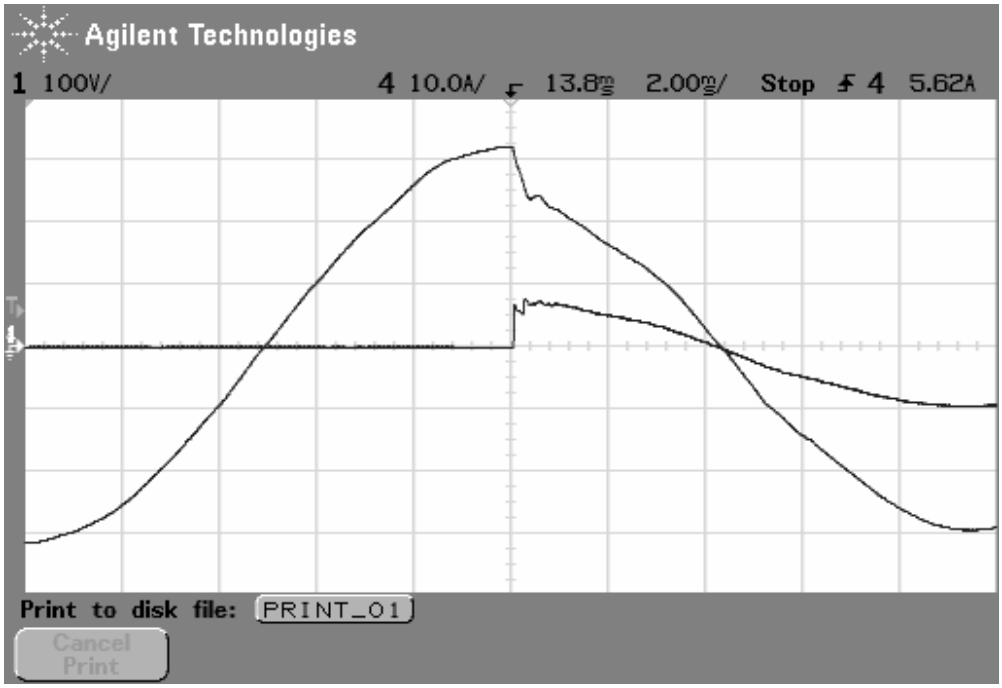

Figure 4.54 One phase output voltage (v_{an}) and load current (i_a) under loading transient at with only capacitor current feedback loop is added.

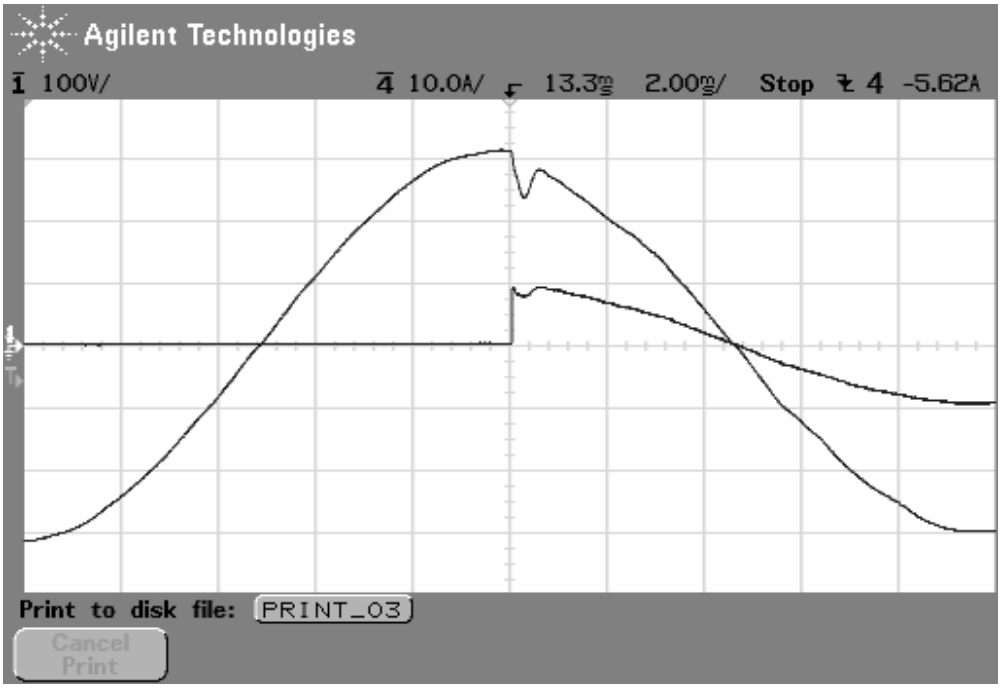

Figure 4.55 One phase output voltage (v_{an}) and load current (i_a) under loading transient at with capacitor current feedback and output voltage proportional controller are added.

CHAPTER 5

CONCLUSIONS

The transformer based UPS topology has many advantages which makes this topology the prime choice in the market for high power applications. Δ/Y connection of the three-phase isolation transformer provides neutral connection terminal from the mid-point of the Y secondary windings. By keeping the leakage inductance of the transformer sufficiently small, zero sequence load currents are shorted in the Δ primary windings of the transformer and the zero sequence output voltage imbalances is suppressed by the transformer. Also by arranging the turns ratio of the transformer, the inverter can be operated at reduced DC bus voltage levels when compared with the transformer-less UPS topologies. So the switching stress and switching losses, which are the most determining factors in high power applications, can be minimized. Also using a transformer eases the UPS paralleling for increasing the power rating of the UPS.

This thesis investigated the application of repetitive control method to the isolation transformer based three-phase UPS. As a method ideal for the periodic nonlinear disturbances this method appears attractive for UPS applications. The repetitive controller in its naive form has several performance issues that prohibit its application to UPS systems unless additional measures are taken. The pure integrator structure of the repetitive controller poses a difficulty in terms of system stability and renders the controller impractical for such applications. This thesis focuses on these additional measures and provides design guidelines for the application of the repetitive control to UPS systems such that high steady-state and dynamic performance can be obtained.

The integrator instability due to high frequency feedback signals that can not be compensated by the controller due to the fact that they are outside the bandwidth of the controller should be attenuated and this is achieved by either a scalar or low-pass filter *Q(z)*. It has been found out that the scalar filter with sufficiently high gain provides adequate results. The resonant peak of the LC filter of the UPS poses problems as the repetitive controller generates signals in the range of the resonant frequency. This issue is addressed with the resonant peak canceling filter *S(z)*. Utilizing a low-pass filter with a sharp cut-off characteristic at the resonant frequency, the resonant peak of the filter is cancelled and also the high frequency signals from the controller are attenuated. As a result the system is stabilized and its high performance for nonlinear periodic loads is retained. DC offset rejection compensator, capacitor current feedback based active damping loop, phase advancing element, and finally the proportional controller acting on the output voltage error have all been found to be useful and in some cases vital elements to the success of a repetitive controlled UPS system.

In the thesis first the UPS system topologies and control methods were reviewed. Then the repetitive control method was studied in depth via theory and numerical examples involving the control blocks existing in the system. A design guideline was established for the main control blocks *Q(z)* and *S(z)* so that these components could be tuned. The system delay has been considered and delay compensation was proposed to improve the system dynamic performance. The design was first verified by computer simulations and later by laboratory experiments. In the final stage the steady-state and dynamic performance of the repetitive controlled UPS system has been studied in detail and performance results were evaluated both by means of computer simulations and laboratory experiments of a 5 kVA UPS. Linear balanced and unbalanced, nonlinear balanced and unbalanced load cases were considered for steady-state operation and linear balanced load was considered for dynamic performance studies.

Based on the results of the study in this thesis, it can be summarized that the repetitive control method is a feasible method for the purpose of controlling the UPS

output voltages. Since it does not require a very high switching frequency and the computational complexity is not high, the method can be applied to both low cost UPS systems with no switching frequency constraint and high power UPS systems with low switching frequency. In the latter, particularly the steady-state performance under nonlinear loading condition can be quite satisfactory with the repetitive controller as the controller is capable of regulating the output voltages even under high crest factor loads.

REFERENCES

[1] S.B. Bekiarov, A. Emadi, "Uninterruptible power supplies: classification, operation, dynamics, and control," Applied Power Electronics Conference and Exposition, vol. 1, pp. 597– 604, 2002.

[2] R.A. Gannett, "Control strategies for high power four-Leg voltage source inverters," M.Sc. Dissertation, Virginia Polytechnic Institute, July 2001.

[3] Motors and generators, NEMA Standards Publication no MG 1-1993.

[4] IEEE Standard 100-1992, "IEEE Standard dictionary of electrical and electronic terms."

[5] IEC 61000-4-30 77A/356/CDV, "Power quality measurement methods," 2001.

[6] N. Mohan, T.M. Undeland, and W.P. Robbins, "Power electronics: converters, applications, and design," John Wiley&Sons, 3rd Edition, 2003.

[7] R. Koffler, "Transformer or transformerless UPS?" IEE Power Engineer, vol. 17 Issue: 3, pp. 34-36, June/July 2003.

[8] R. Zhang, "High performance power converter systems for nonlinear and unbalanced load/source," Ph.D. Dissertation, Virginia Polytechnic Institute, November 1998.

[9] H.J. Jiang, Y. Qin , S. S Du and Z.Y. Yu, S. Choudhury "DSP Based Implementation Of A Digitally-Controlled Single Phase PWM Inverter For UPS, " Telecommunications Energy Conference, vol. 1, pp. 221-224, 1998.

[10] M.J. Ryan, W.E. Brumsickle, R.D. Lorenz, “Control topology options for single phase UPS inverters,” *IEEE Trans. on Industry Appl.*, vol. 33, pp. 493-501, March/April 1997.

[11] N.M. Abdel-Rahim, J.E. Quaicoe, “Analysis and design of a multiple feedback loop control strategy for single-phase voltage source UPS inverters,” *IEEE Trans. on Power Elect.*, vol. 11, pp. 532-541, July 1996.

[12] O. Kükrer, “Deadbeat control of a three-phase inverter with an output LC filter,” *IEEE Trans. on Power Elect.*, vol. 11, pp. 16-23, January 1996.

[13] O. Kükrer, H. Kömürcügil, “Deadbeat control method for single phase UPS inverters with compensation of computation delay,” *IEE Proceeding-Electr. Power Appl.*, vol. 146, pp. 123-128, January 1999.

[14] A. Kawamura, T. Haneyoshi, and R. G. Hoft, “Deadbeat controlled PWM inverter with parameter estimation using only voltage sensor,” *IEEE Power Elect. Spec. Conf.*, pp. 576-583, 1986.

[15] K. Kim, N. Park, D. Hyun, “Advanced synchronous reference frame controller for three-phase UPS powering unbalanced and nonlinear loads,” IEEE PESC Conference, pp. 1699-1704, 2005.

[16] D.N. Zmood, D.G. Holmes, G.H. Bode, “Frequency-domain analysis of three-phase linear current regulators,” *IEEE Trans. on Industry Appl.*, vol. 37, pp. 601-610, April 2001.

[17] Liviu Mihalache, “Single loop DSP control method for low cost inverters,” Applied Power Electronics Conference and Exposition, vol. 1, pp.95-101, 2004.

[18] P. Mattavelli, “Synchronous-frame harmonic control for high-performance AC power supplies,” *IEEE Trans. on Industry Appl.*, vol. 37, pp. 864-872, May/June 2001.

[19] D.N. Zmood, D.G. Holmes, G.H. Bode, “Frequency-domain analysis of three-phase linear current regulators,” *IEEE Trans. On Industry Appl.*, vol. 37, pp. 601-610, April 2001.

[20] E. Demirkutlu, “Output voltage control of a four-leg inverter based three-phase UPS by means of stationary frame resonant filter banks” M.Sc. Dissertation, Middle East Technical University, 2006.

[21] U. Borup, P.N. Enjeti, F. Blaabjerg, “A new space-vector-based control method for UPS systems powering nonlinear and unbalanced loads,” *IEEE Trans. on Industry Appl.*, vol. 37, pp. 1864-1870, Nov./Dec. 2001.

[22] Y.Y. Tzou, R.S. Ou, S.L. Jung, and M.Y. Chang, “High-performance programmable ac power source with low harmonic distortion using DSP-based repetitive control technique,” *IEEE Trans. on Power Elect.,* vol. 12, pp. 715-725, July 1997.

[23] K. Zhang, Y. Kang, J. Xiong, J. Chen, “Direct repetitive control of SPWM inverter for UPS purpose,” *IEEE Trans. on Power Elect.*, vol. 18, pp. 784-792, May 2003.

[24] Y. Dote, R.G. Hoft, “Intelligent control: power electronic system,” Oxford University Press, 1998.

[25] A.M. Hava, “Carrier Based PWM-VSI Drives in the Overmodulation Region,” Ph.D. Dissertation, University of Wisconsin-Madison, 1998.

[26] H.W. Van Der Broeck, H.C. Skundelny, G.V. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Trans. on Industry Appl.*, vol. 24, pp. 142-150, Jan./Feb. 1988.

[27] A.M. Hava, R.J. Kerkman, T.A. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. on Industry Appl.*, vol. 34, pp. 1059-1071, September/October 1998.

[28] H. Pinheiro, F. Botterón, J. R. Pinheiro, H. L. Hey and H. A. Gründling, "A digital controller for single-phase UPS inverters to reduce the output DC component", *IEEE PESC Conf. Rec.*, vol. 1, pp. 1311-1314, 2004.

[29] F. Botterón and H. Pinheiro, "A new discrete-time voltage controller based on the internal model principle for three-phase voltage source PWM inverters with ΔY output transformer," *IEEE PESC Conf. Rec.*, vol. 1, pp. 2508-2514, 2004.

[30] Matlab 6.5. A numerical computation software, Mathworks Inc., 2002.

[31] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, "Feedback Control of Dynamic Systems," MA Addison-Wesley, 1991.

[32] A. King, W. Knight, "Uninterruptible power supplies and standby power systems," McGraw-Hill, 1st edition, 2003.

[33] L. Cuiyan, Z. Dongchun, Z. Xianyi, "Theory and applications of the repetitive control," SICE Annual Conference, vol. 1, pp. 27-34, 2004.

[34] P. Li, B. Dan, K. Yong, and C. Jian, "Research on three-phase inverter with unbalanced load," Applied Power Electronics Conference and Exposition, vol. 1, pp. 128- 133, 2004.

[35] Ansoft-Simplorer V7.0. A power electronics simulation software, Ansoft Corporation, 2004.

[36] “DS1104 R&D controller board, Hardware installation and configuration,” dSPACE manual, for release 4.1, March 2004.