DESIGN OF A SINGLE-PHASE FULL-BRIDGE DIODE RECTIFIER POWER FACTOR CORRECTOR EDUCATIONAL TEST SYSTEM

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

TEOMAN ÜNAL

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

DECEMBER 2006

Approval of the Graduate School of Natural and Applied Sciences.

Prof. Dr. Canan ÖZGEN
Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

Prof. Dr. İsmet ERKMEN
Head of Department

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

Prof. Dr. Yıldırım ÜÇTUĞ
Supervisor

Examining Committee Members

Prof. Dr. Muammer ERMİŞ	(METU, EEE)	_____
Prof. Dr. Yıldırım ÜÇTUĞ	(METU,EEE)	_____
Prof. Dr. H. Bülent ERTAN	(METU,EEE)	_____
Asst. Prof. Dr. Ahmet M. HAVA	(METU,EEE)	_____
Dr. İsmet ARSAN	(KAREL)	_____

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name : TEOMAN ÜNAL

Signature :

ABSTRACT

DESIGN OF A SINGLE-PHASE FULL-BRIDGE DIODE RECTIFIER POWER FACTOR CORRECTOR EDUCATIONAL TEST SYSTEM

Ünal, Teoman

M.S., Department of Electrical and Electronics Engineering

Supervisor : Prof. Dr. Yıldırım Üçtuğ

December 2006, 227 pages

In this thesis an educational test bench for studying the power quality attributes of the commonly used single-phase full-bridge diode rectifiers with power factor correction (PFC) circuits is designed and tested. This thesis covers the active and passive power factor correction methods for single-phase bridge rectifier. Passive filtering approach with dc side inductor and tuned filter along with active filtering approach via single-switch boost converter is considered. Analysis, simulation, and design of a single phase rectifier and PFC circuits is followed by hardware implementation and tests. In the active PFC approach, various control methods is applied and compared. The educational bench is aimed to useful for undergraduate and graduate power electronics course, power quality related laboratory studies.

Keywords: Power Factor Correction, passive filter methods, active PFC control topologies.

ÖZ

TEK FAZLI, TAM KÖPRÜ DİYOTLU DOĞRULTUCU İÇİN GÜÇ KATSAYISI DÜZELTİCİ EĞİTİM TEST SİSTEMİ TASARIMI

Ünal, Teoman
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi : Prof. Dr. Yıldırım Üçtuğ

Aralık 2006, 227 sayfa

Bu tezde, yaygın olarak kullanılan güç katsayısı düzeltmeli tek faz tam köprü diyotlu doğrultucuların güç kalitesi özelliklerini incelemek için eğitim test seti tasarlanmış ve gerekli test düzenekleri geliştirilmiştir. Eğitim amaçlı olarak da kullanılabilecek bu sistem tek fazlı diyotlu doğrultucular için aktif ve pasif çözümleri içermektedir. Pasif çözümler olarak DC tarafa yerleştirilen endüktans filtre ile tuzak filtre yöntemleri incelenmiş ve kullanılmıştır. Aktif yöntem olarak tek anahtarlı gerilim yükseltici dönüştürücü devresi kullanılmıştır. Yapılan bütün uygulamalar için teorik ve bilgisayar benzeşimine dayanan analizler, donanımsal olarak gerçekleştirilmiş ve üzerinde ölçümler alınabilecek seviyeye getirilmiştir. Aktif güç katsayısı düzeltici devresinde çeşitli denetim yöntemleri uygulanmış ve karşılaştırılmıştır. Geliştirilen eğitim seti lisans ve lisansüstü güç elektroniği derslerinde güç kalitesi ile ilgili inceleme uygulamalarında kullanılabilir niteliktedir.

Anahtar Kelimeler: Güç katsayısı düzenleme, pasif filtre uygulamaları, aktif PFC kontrol yöntemleri.

To My Parents

who always support me in all aspects of my life

ACKNOWLEDGMENTS

I would like to express my sincerest thanks to Prof. Dr. Yıldırım Üçtuğ for his guidance, support and encouragements throughout the preparation of this thesis.

I would also like to thank Asst. Prof. Dr. Ahmet Hava for his suggestions and comments.

I express my deepest gratitude to my parents, my father Halis, my mother Refika, my brother Çağlar and all my family members for their encouragements throughout my education life. Their love, care and encouragement has given me a great inner strength to success. This work is dedicated to them.

I would also like to thank YILDIRIM ELEKTRONIK TIC.SAN. LTD. STI, especially to Mr. Süleyman Alkan for their supports during my study period.

I am grateful to my friends in Middle East Technical University for all the support they gave me throughout my study.

TABLE OF CONTENTS

PLAGIARISM iii
ABSTRACT iv
ÖZ v
DEDICATION vi
ACKNOWLEDGEMENTS vii
OF CONTENTS viii
LIST OF FIGURES xii
LIST OF TABLES xvi
CHAPTER
1. INTRODUCTION 1
1.1 Background 1
1.2 Definitions 4
1.3 Harmonics and Effects on the Mains 7
1.4 Harmonic Current Emission Standards 8
1.5 Power Factor Correction Methods 17
1.5.1 PFC Design Criteria 18
1.5.2 Passive Approach 19
1.5.3 Active PFC 20
1.5.3.1 Active Two-Stage Approach 22
1.5.3.2 Active Single-Stage Approach 24
1.5.4 Comparison of PFC Solutions 25
1.6 Objective and Organization 27
2. PASSIVE POWER FACTOR CORRECTION 28
2.1 Single Phase Full-Wave Rectifier 28
2.2 Passive Power Factor Correction Methods 35
2.2.1 LC Filter Method 35
2.2.1.a Experimental Implementation of LC Filter Method 46
2.2.2 Series Connected Parallel Resonant Filter 56
2.2.2.a Experimental Evaluation of 3rd Harmonic Filter ..... …58

2.2.3 Variable Inductance LC Filter Method 60
2.2.3.a Saturated Core Inductors 62
2.2.3.b Step-Gap Variable Inductor 65
2.2.3.c Sloped Air-Gap Inductor 67
2.2.3.d Design of Sloped Gap Inductance 70
2.2.3.e Experimental Evaluation of SAG LC Filter Method 73
2.3 Limitations of Passive PFC Circuits 76
3. AVERAGE CURRENT CONTROL OF PFC 77
3.1 Description of Average Current Mode Control of PFC 77
3.2 Power Balance Analysis of the PFC Circuit 79
3.3 Input Voltage Feed-Forward 83
3.4 Control Loop Design 89
3.4.1 Current Loop Design 90
3.4.2 Voltage Loop Design 96
3.5 Simulation of Average Current Controlled PFC 98
3.6 Hardware Implementation of Average Current Control PFC 105
3.6.1 Functional Description of the Power Circuit 105
3.6.2 Functional Description of the Control Circuit 106
3.7 Design of the Average Current Controlled PFC 108
3.8 Experimental Results 118
3.9 Conclusion 124
4. CRITICAL CONDUCTION MODE CONTROL OF PFC 125
4.1 Introduction 125
4.2 Operation of Critical Conduction Mode 126
4.3 Analysis of Switching Characteristics 129
4.4 Simulation of Boundary Conduction Mode PFC 133
4.5 Hardware Implementation of Boundary Conduction Mode PFC 137
4.5.1 Functional Description of the Power Circuit 138
4.5.2 Functional Description of the Control Circuit 138
4.6 Design of the Boundary Conduction Mode PFC 140
4.7 Experimental Results 148
4.8 Conclusion 153

5.ONE CYCLE CONTROL OF PFC 154
5.1Introduction 154
5.2 Operation of One Cycle Control 155
5.3 Simulation of One Cycle Control of PFC 158
5.4. Hardware Implementation of One Cycle Control PFC Converter 162
5.4.1 Functional Description of the Power Circuit 163
5.4.2 Functional Description of the Control Circuit 163
5.5 Design of the One Cycle Control PFC Converter 165
5.6 Experimental Results 174
5.7 Conclusions 176
6.EXPERIMENTS ON POWER FACTOR CORRECTION 177
6.1Objective 177
6.2 Background Information 178
6.3 Components of the Experimental System 185
6.3.1 Isolated AC Power Supply 185
6.3.2 Passive Power Factor Correction System 187
6.3.3 Active Power Factor Correction System 188
6.4 Required Measurement Equipment 192
6.5 Safety 193
6.6 Experiment 1 – Single-Phase Rectifier with Capacitive Fitler 194
6.6.1 Introduction 194
6.6.2 Demonstrations Circuits 194
6.6.3 Procedure 194
6.6.4 Study Questions 197
6.7 Experiment 2 – L Type Passive Fitler 198
6.7.1 Introduction 198
6.7.2 Procedure 199
6.7.3 Study Questions 205
6.8 Experiment 3– Series Connected Parallel Resonant Filter 206
6.8.1 Introduction 206
6.8.2 Procedure 206
6.8.3 Study Questions 206

6.9 Experiment 4– Variable Inductance (SAG Inductor) Method 210
6.9.1 Introduction 210
6.9.2 Procedure 210
6.9.3 Study Questions 212
6.10 Experiment 5– Active Power Factor Correction 213
6.10.1 Introduction 213
6.10.2 Procedure 214
6.10.3 Study Questions 218
7.CONCLUSIONS AND FURTHER WORK 219
REFERENCES 221
APPENDIX 226

LIST OF FIGURES

FIGURES

1.1 Single Phase Rectifier with Capacitive Smoothing 2
1.2 Waveforms for Single Phase Rectifier with Capacitive Smoothing 2
1.3 Input Current Harmonics of Single Phase Rectifier with Capacitive Smoothing 3
1.4 Different Current and Voltage waveforms of Single Phase Rectifier 6
1.5 Equipment Classification Chart according to IEC 61000-3-2, A14 Standard 13
1.6 Envelope of the input current used to classify Class D equipment, as defined in the first edition of IEC 61000 -3-2 14
1.7 Simple passive PFC circuit 19
1.8 a) two-stage PFC b) single-stage PFC 22
1.9 Boost Type Active PFC 23
1.10 Waveforms without/with PFC a) Without PFC b) Passive PFC c)Active PFC 25
2.1 Typical single phase rectifier 28
2.2 Current and Voltage Waveforms 29
2.3 Current Harmonics 30
2.4.1 Input current and voltage waveforms for single phase rectifier 31
2.4.2 Input Current Harmonics 32
2.5 Simulated input voltage and current waveforms with capacitive filter 33
2.6 Simulated output voltage ripple with capacitive filter 33
2.7 Current harmonics spectrum for Co=100uF 34
2.8 Current harmonics for Co=470uF 34
2.9 Single Phase Rectifier with LC Filter 36
2.10 Normalized single phase rectifier 37
2.11 Simulated waveform for Lo-N=0.01 39
2.12 Simulated waveform for Lo-N=0.043 40
2.13 Simulated waveform for Lo-N=0.09mH 40
2.14 PF, DF and DP as function of L_{O-N} 41

2.15 Normalized Class D harmonic limits and Normalized input current harmonics versus normalized filter inductance L_{O-N} 43
2.16 Minumum required inductance to comply with En 61000- 3-2 Class D harmonic limits 44
2.17 Minumum required inductance to comply with En 61000- 3-2 Class A harmonic limits 45
2.18 Simulated Input Current and Voltage Waveform for Class D-100W 47
2.20 Measured Input voltage and Current for Class D-100W 47
2.21 Harmonic Spectrum for Input Current For Class D – 100W 48
2.22 Simulated Input Current and Voltage Waveform for Class D – 200W 49
2.23 Measured Input voltage and Current for Class D – 200W 50
2.24 Harmonic Spectrum for Input Current for Class D – 200W 50
2.25 Simulated Input Current and Voltage Waveform for Class A – 100W 52
2.26 Measured Input Current Harmonics For Class A-100W 52
2.27 Harmonic Spectrum for Input Current for Class A – 100W 53
2.28 Simulated Input Current and Voltage Waveform for Class A – 200W 54
2.29 Measured Input voltage and Current for Class A – 200W 54
2.30 Harmonic Spectrum for Input Current for Class A – 200W 55
2.31 Series Connected Parallel Resonant Filter 56
2.32 Input Current and Voltage Waveform for Series Connected Paralel Filter 58
2.33 Measured current of series connected parallel resonant filter for 150W System .. 59
2.34 Input current harmonics for series connected parallel resonant filter 59
2.35 Required minimum Inductance for Class D 60
2.36 Relative Permeability versus magnetization force 62
2.37 Constant Air-Gap Inductor 63
2.38 Constant gap Variable Inductor 64
2.39 Swinging Inductor 65
2.40 Swinging inductance variations 66
2.41 Sloped Air-Gap Inductance 67
2.42 Inductance Variations of Sloped Air-Gap Inductor 69
2.43 Inductance Variations of Sloped Air-Gap Inductor 70
2.44 Construction of Sloped Air-Gap Inductor with EI Silicon Steel 71

2.45 Detailed view of the Sloped Air-Gap 72
2.46 Magnetic Circuit of the Sloped Air-Gap Inductance 72
2.47 Variable Inductance Model used in Simulations 73
2.48 Simulation results for input voltage and current 74
2.49 Experimental results for input voltage and current 75
2.50 Input Current Harmonics for 200W Class-D Application 75
3.1 Average current mode control of PFC 78
3.2 Variation on the capacitor voltage. 80
3.3 Multiplier based control. 81
3.4 Rectified line voltage and current for 120-Vac line voltage. 84
3.5 Multiplier inputs I_{AC} and V_{AOUT} at 120-Vac line voltage. 84
3.6 Rectified line voltage and current for 240-Vac line voltage. 84
3.7 Multiplier inputs I_{AC} and V_{AOUT} at 240-Vac line voltage 85
3.8 Block diagram of the average current PFC with feed-forward. 86
3.9 First order input voltage feed-forward sensing scheme. 87
3.10 Second order input voltage feed-forward sensing scheme. 88
3.11 First order input voltage feed-forward sensing scheme. 88
3.12 PFC control loops 89
3.13 PFC current loop. 90
3.14 Laplace domain block-schema of the current loop. 91
3.15 Linearized model of the PFC boost converter 92
3.16 Magnitude and phase plots of the converter transfer function $G_{id}(s)$. 94
3.17 a) Circuit Diagram (b) Gain response of current compensator. 95
3.18 Compensated loop gain and phase plots of the inner current loop. 96
3.19 Voltage control loop 96
3.20 Small signal model of outer loop. 97
3.21 Simulation block diagram of average current mode PFC. 99
3.22 S-Transfer function for the voltage and current controller used in simulation. 101
3.23 Line voltage and line current simulation waveforms for 220-V input voltage at 250-W PFC system 101
3.24 Output voltage and input current simulation waveforms for 220 V input voltage at 250-W PFC system 102

3.25 Line voltage and line current simulation waveforms for 120 V input voltage at 250-W PFC system 103
3.26 Output voltage and input current simulation waveforms for 120V input voltage at 250W PFC system 103
3.27 Step response for output voltage and input current simulation waveforms for 220 V input voltage at half-load to full-load step 104
3.28 Block diagram of the UCC3818 controller IC. 107
3.29 Schematic diagram of the 250-W, average current controlled PFC. 110
3.30 Feed-forward circuit for the UCC3818 IC. 114
3.31 Output voltage compensator configuration. 117
3.32 PCB layout of the average current mode PFC circuit. 119
3.33 Input voltage and input current waveforms 119
3.34 Input current harmonic spectrum. 120
3.35 Output voltage and input current waveform. 120
3.36 Input current distortions around zero crossings. 121
3.37 Input voltage and input current waveforms. 121
3.38 Input current harmonic spectrum. 122
3.39 Output voltage ripple waveform. 122
3.40 Input current distortions around zero crossings. 123
3.41 Start-up behavior of the input current and output voltage 123
4.1 Block diagram of a BCM boost converter. 126
4.2 Current waveforms during half of an AC line cycle. 127
4.3 Switching sequences of PFC Stage. 128
4.4 Inductor Current and Corresponding Gate Signals. 129
4.5 Switching frequency over the AC line cycle. 132
4.6 Block diagram of simulation circuit. 133
4.7 Voltage controller s-transfer function and current controller equation block. 135
4.8 Line voltage, reference inductor current and actual inductor current simulation waveforms for 220 V input voltage at 150 W PFC. 135
4.9 Line voltage and input current simulation waveforms for 220 V input voltage at 150 W PFC system 136

4.10 Output voltage and input current simulation waveforms for 220 V input voltage at 150 W PFC system. 136
4.11 Transient response for output voltage simulation waveforms for 220 V input voltage at start-up and half-load to full-load step. 137
4.12 Block diagram of the MC34262 controller IC. 139
4.13 Schematic diagram of the 150W, critical current mode PFC..... 142
4.14 Switching frequency for 220VAC line voltage for critical current mode PFC.... 144
4.15 Switching frequency for 120VAC line voltage for critical current mode PFC.... 145
4.16 Output voltage ripple..... 146
4.17 Transconductance type amplifier configuration..... 147
4.18 PCB layout of the critical conduction mode PFC circuit. 148
4.19 Input voltage and input current waveforms. 149
4.20 Input current harmonic spectrum. 149
4.21 Output voltage and input current waveforms 150
4.22 Input current distortions around zero crossings. 150
4.23 Input voltage and input current waveforms. 151
4.24 Input voltage and input current waveforms. 151
4.25 Output voltage and input current waveforms. 152
4.26 Input current distortions around zero crossings. 152
4.27 Start-up behavior of the input current and output voltage 153
5.1 One cycle control of PFC. 155
5.2 Transconductance type error amplifier. 156
5.3 Resettable integrator characteristics. 157
5.4 Block diagram of OCC. 157
5.5 PWM signal generation. 158
5.6 Simulation circuit of one cycle control. 159
5.7 Simulation blocks a) Output voltage controller b) Resettable integrator. 160
5.8 Input voltage and current simulation waveforms for 220Vac input voltage 161
5.9 Input voltage and input current simulation waveforms for 150Vac input voltage 161
5.10 Input voltage and input current simulation waveforms for 150Vac input voltage 162
5.11 Block diagram of IR1150 PFC controller. 164
5.12 Schematic of 250W PFC converter with IR1150. 166

5.13 Switching frequency vs. programming resistor. 168
5.13 Outer voltage loop. 170
5.14 Small signal model of outer loop. 171
5.15 Voltage error amplifier. 173
5.16 PCB layout of one cycle control PFC converter. 174
5.17 Input voltage and input current waveforms a) 220Vac 175
5.18 Output voltage and input current waveforms 176
6.1 Single-phase diode rectifier with bulk capacitive filter. 179
6.2 Waveforms for single-phase rectifier with capacitive smoothing. 180
6.3 Input current harmonics for a single-phase rectifier with capacitive smoothing. .. 181
6.4 Simple passive PFC circuit. 183
6.5 Boost type active PFC. 184
6.6 Experiment system for single-phase power factor correction. 185
6.7 Isolated, variable AC power supply. 186
6.8 Passive power factor correction unit. 187
6.9 Active power factor correction circuit. 189
6.10 Circuit layout. 189
6.11 Schematic diagram of 250W average current control PFC. 190
6.12 Single Phase diode rectifier test circuit. 195
6.13 a) Input voltage and Current waveforms b) Input current harmonics. 196
6.14 Output voltage waveforms for different capacitance values. 197
6.15 Minimum required inductance to comply with EN 61000- 3-2 Class A limits. .. 198
6.16 Minimum required inductance to comply with EN 61000- 3-2 Class D limits. .. 199
6.17 Single phase diode rectifier with L filter test circuit. 200
6.18 Input voltage and current waveforms for 100W Class A with 10mH filter 201
6.19 Harmonic spectrums for input current for Class A – 100W. 201
6.20 Input voltage and current waveforms for 200W Class A with 10mH filter 202
6.21 Harmonic spectrums for input current for Class A – 200W. 203
6.22 Measured input voltage and current for Class D a) 100W 204
6.23 Harmonic spectrums for input current for Class D – 100W. 204
6.24 Harmonic spectrums for input current for Class D – 200W. 205
6.25 Single phase diode rectifier with 3rd harmonic filter test circuit. 207

6.26 Current of 3rd harmonic filter for 150W system 208
6.27 Harmonic spectrums for input current for 150W 3rd harmonic filtered rectifier. 208
6.28 Single phase diode rectifier with variable inductance filter test circuit. 211
6.29 Experimental results for input voltage and current. 212
6.30 Input current harmonics for 200W Class-D SAG application. 212
6.31 Block diagram of average current mode PFC. 213
6.32 Connection diagram for active PFC experiments. 214
6.33 a) Input current and voltage waveforms (b) Input current harmonics. 215
6.34 Output voltage ripple for 220 V AC input voltage. 215
6.35 Power Factor vs. Line/Load. 216
6.36 Start-up behavior of the input current and output voltage. 217
6.37 Measurement method of switching characteristics. 218

LIST OF TABLES

TABLES

1.1. Class A absolute maximum harmonic limit 10
1.2. Class B absolute maximum harmonic limits 10
1.3. Class C absolute maximum harmonic limits 11
1.4. Class D absolute maximum harmonic limits 11
1.5. IEC 61000-3-2 changes 16
1.6. Comparison of three solutions 26
2.1. Experimental parameters of 200W rectifier 30
2.2. Experimental results for 200W rectifier 31
2.3. Class D absolute maximum harmonic limits 42
2.4. Class A absolute maximum harmonic limits 44
2.5. Parameters for 100W-Class D application 46
2.6. Measured data for 100W Class-D application 48
2.7. Circuit parameters for 200W-Class D Application 49
2.8 Measured result for 200W Class-D application 50
2.9 Parameters for 100W-Class A Application 51
2.10 Measured results for 100W-Class A application 53
2.11 Parameters for 200W-Class-A Application 53
2.12 Measured results for 200W-Class A application 55
2.13. Simulation parameters of series connected parallel resonant filter 58
2.14. Measured data for 150W series connected parallel resonant filter 60
2.15. Simulation parameters of Variable Inductance LC Filter Method 73
2.16 Parameters of sloped air-gap inductance 74
2.17. Measured data for the variable inductance filter for the single phase Rectifier 76
3.1 Simulation parameters of average current mode PFC 100
3.2 Design parameters of 250W average current PFC 108

4.1 Simulation parameters of critical conduction mode PFC 134
4.2 Design parameters of current conduction PFC 141
5.1 Simulation parameters of active PFC..... 159
5.2 Design parameters of active PFC..... 165
5.3 Comparison of control topologies..... 176
6.1 Classification of electronic equipments by EN 61000-3-2 harmonic Standard..... 182
6.2 Maximum harmonic limits for each class type defined by EN 61000-3-2 182
6.3 Bill of materials..... 191
6.4 Single-phase diode rectifier experiment parameters. 195
6.5 Measurement results for single-phase diode rectifier experiment 196
6.6 Experiment parameters for 100W L filter application - Class A 200
6.7 Measurement results for 100W single-phase diode rectifier L filter experiment .. 201
6.8 Measurement results for 200W single-phase diode rectifier L filter experiment .. 202
6.9 Experiment parameters for L filter application - Class D..... 203
6.10 Experiment parameters for 3rd harmonic filter 206
6.11 Measurement results for 150W single-phase diode rectifier 3rd harmonic filter experiment..... 207
6.12 Experiment parameters for variable inductance filter application 210
6.13 Measurement results for single-phase diode rectifier SAG filter experiment..... 211
6.14 Measured PF for different input voltage level 216
8.1.List of Commercially Available PFC Controllers..... 226

CHAPTER 1

INTRODUCTION

1.1 Background

The usage of electronic equipments is increasing rapidly in the daily life as consumer or industrial needs. All these electronic equipments have power supplies that obtain required energy from utility grid. These electronic systems generally use one or more switch mode power supplies that draw a non-sinusoidal current. This causes current and voltage distortions that effect other equipments connected to the same power grid, thus, lowering the capability of the power source. In order to overcome these problems, new standards have been developed for limiting the harmonic content of the input current. Manufacturers should find solutions for meeting these standards` requirements.

Most of power supplies consist of AC\DC converter stages based on diode or thyristor rectifier circuits. Conventionally, this stage consists of a diode rectifier with an output capacitor. These rectifier circuits constitute a major cause of mains harmonic distortion. Line-frequency diode rectifiers convert AC voltage into DC output voltage in an uncontrolled way. For low power applications (such as PCs, TVs, home appliances, etc…) single-phase diode rectifiers are chosen owing to low cost and simple structure. For high power applications (such as industrial equipments and motor drives) three-phase diode or thyristor rectifiers are used.

A typical offline switch mode power supply contains full-wave bridge rectifier with a large smoothing capacitor. This combination is one of the easiest and lowest cost

solutions for AC-DC conversion. This input rectifier with capacitive filter draws non-sinusoidal input current from utility. The pulsating current waveform is rich of harmonics [6], [7], [8]. A typical single-phase rectifier with capacitive smoothing and its output voltage and input current waveforms are shown in Figure 1.1 and Figure 1.2.

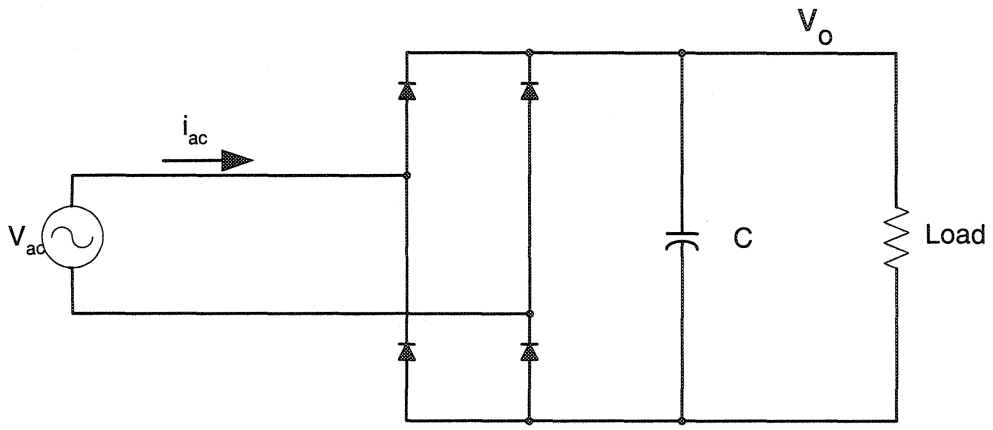


Figure 1.1 Single-phase rectifier with capacitive smoothing.

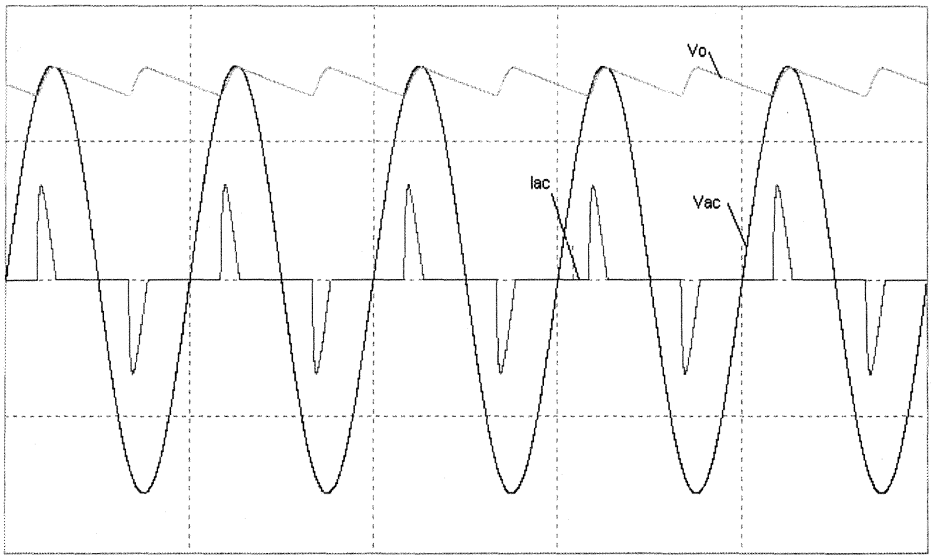


Figure 1.2 Waveforms for single-phase rectifier with capacitive smoothing.

This AC-DC peak detector circuit has some disadvantages. Mainly the input current has higher harmonic content (with an especially dominant third harmonic) and a low power factor due to distorted current waveform. A general harmonic content and THD of single-phase diode bridge rectifier is given below in Figure 1.3. This type of rectifier has some disadvantages such as creating harmonics and EMI, causing high power losses due to higher rms current, requiring over rated components and reducing power line capability.

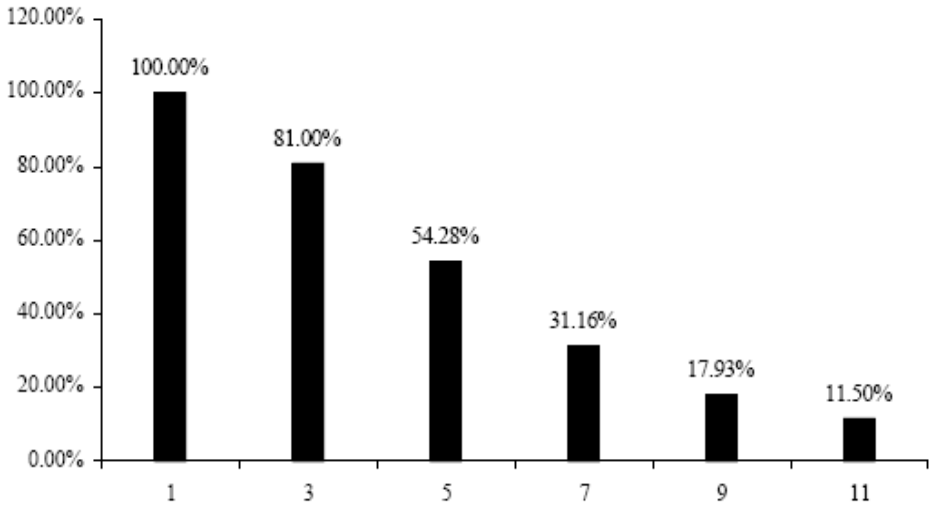


Figure 1.3 Input current harmonics of single-phase rectifier with capacitive smoothing.

This behavior of this circuit has negative effects on the utility line and on the PCC such as deterioration of the line voltage, unbalanced currents on star windings; power loses over line impedances, overheating and EMC problems. In the general usage, different load groups are supplied by different phases. If one of the phases is loaded with nonlinear loads, unbalanced currents flow through the neutral line of star configuration. These unbalanced currents cause heating and power loss in the conductors and voltage distortion and EMC problems occur. Moreover the harmonic content of this pulsating current causes additional losses and dielectric stresses in capacitors and cables, increasing currents in windings of rotating machinery and transformers and noise emissions in many products, and bringing about early failure

of fuses and other safety components. Harmonics can affect other devices that are connected to the same system.

In order to reduce these harmonic polluting effects, international standards such as IEC 61000-3-2 have been developed for limiting harmonic currents. The International Electrotechnical Commission (IEC) sets limits for harmonics in the current of small single-phase or three-phase loads, less than 16 A per phase, in *Electromagnetic compatibility (EMC) - Part 3-2: Limits - Limits for harmonic current emissions* (IEC 61000-3-2) [1]. The circuit classifications and harmonic limits are given in this standard. The power supply manufacturers use different solutions for complying with the specifications. The techniques for reduction of current harmonics are called Power Factor Correction (PFC) solutions. The aim of PFC is providing a resistive load behavior of all power supplies.

1.2 Definitions

Power factor shows how effectively energy is transmitted to load. It also represents a measure of distortion of the line voltage and line current and phase shift between them. PF has range between 0 and 1 and is defined as the ratio of the real power to the apparent power.

$$\text{Power Factor (PF)} = \frac{\text{Real Power (Average)}}{\text{Apparent Power}} \tag{1.1}$$

The real power is defined as the product of the fundamental voltage and fundamental current and the phase displacement between the two.

$$P_{real} = V_{1,rms} \cdot I_{1,rms} \cdot \cos\varphi \tag{1.2}$$

where $V_{1,rms}$, $I_{1,rms}$ are the rms values of the fundamental line current and the fundamental line voltage, respectively, and φ is the phase shift between line current and line voltage.

The apparent power is the product of rms voltage and rms current.

$$P_{app} = V_{rms} \cdot I_{rms} \tag{1.3}$$

In a linear load system, the power factor depends on phase difference between V_{rms} and I_{rms}. Then, the power factor can be expressed as.

$$PF = \frac{V_{rms} \cdot I_{rms} \cdot \cos\varphi}{V_{rms} \cdot I_{rms}} = \cos\varphi \tag{1.4}$$

It is shown that in the case of both sinusoidal voltage and current waveform systems with no phase difference between fundamental component of the current and voltage achieve unity power factor. This situation appears in resistive load circuits.

In a nonlinear load system with distorted current waveform, the rms values of the input current and the fundamental frequency component of the input current are not the same. The various harmonic components of the current appear as distorted power on the line. Then the power factor expression in the case of stable line voltage can be written as.

$$PF = \frac{I_{1,rms}}{I_{rms}} \cos\varphi = k_{distortion} \cdot k_{displacement} \tag{1.5}$$

Where $k_{distortion} = {I_{1,rms}}/{I_{rms}}$ is the distortion factor and $k_{displacement} = \cos\varphi$ is the displacement factor. Distortion factor describes harmonic content of the current. It shows the difference between fundamental component of the current and actual waveform.

Total Harmonic Distortion (THD) shows the ratio of the rms value of the waveform (not including the fundamental component) to the rms value of the fundamental component.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2}}{I_{1,rms}} \tag{1.6}$$

Then distortion factor can be written by using THD definition in Eq. (1.6):

$$k_{distortion} = \frac{1}{\sqrt{1+(THD)^2}} \tag{1.7}$$

In Figure1.4, it can be seen that the different voltage and current waveforms result in different PF and THD due to distortion factor and displacement factor.

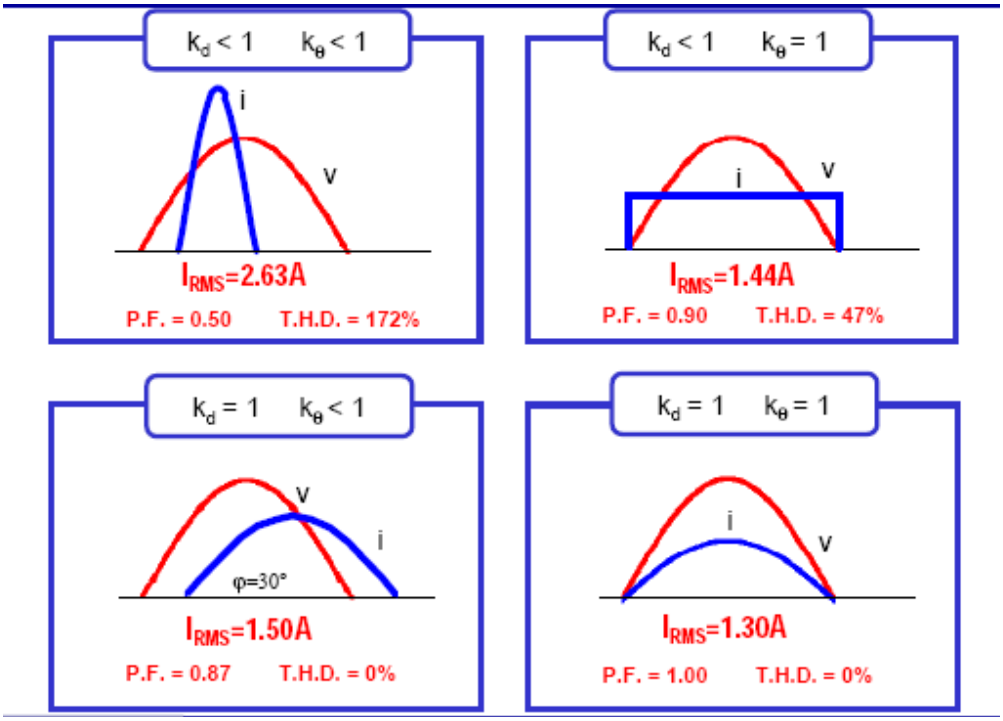


Figure 1.4 Different current and voltage waveforms of single phase rectifier.

1.3 Harmonics and Their Effects on the Mains

Harmonics are the components of any waveform at multiple frequencies of the fundamental component. For a 50-Hz system the harmonic components occur in even and odd multiples of the mains frequency. Generally, non-linear loads draw distorted currents with higher harmonic content that consists of fundamental frequency component plus harmonic components.

Most electrical equipments are designed to operate under ideal sinusoidal environment. In the case of a harmonically polluted system the power line loses its ideal characteristic. The practical problems that may arise from excessive harmonic levels are [4], [5]:

- Harmonic currents flowing in the supply network generate additional energy losses and cause distortion of supply voltage.

- Higher frequency harmonic currents cause power losses (copper and iron losses) which result in an increase in the heating of elements. Equipment ratings must take the presence of harmonics into account. The higher rated neutral conductor is required to carry the added high frequency currents.

- Distorted waveforms result in poor power factor.

- Interference to equipment which is sensitive to voltage waveform

- Damage to power factor correction capacitors. Malfunction of ripple control and other mains signaling systems, protective relays and, possibly, in other control systems. Additional losses in capacitors and rotating machines. Additional acoustic noise from motors and other apparatus, reducing the efficiency of motors.

The diode bridge input circuit in a single-phase AC drive is the same as used in a very wide range of electronic equipment such as personal computers and domestic appliances. All of these cause similar current harmonics. Their effect is cumulative if they are all connected to the same low voltage (e.g. 230V) supply system. This means that to estimate the total harmonic current in an installation of single-phase units, the harmonics have to be added directly.

The power system is designed for predefined current values and all components belonging to this system have standard ratings and protection elements. Low power factor devices that draw higher current from the mains reduce the efficient power supplied by the mains. This means that low power nonlinear loads are reflected to the mains side with higher power ratings. Since the power line system is designed for fixed values, available power at the load side is decreased because of low power factor loads.

Harmonic currents in the AC distribution network require higher current carrying capacity that results in extra cost and power losses. This increasing capacity first affects the device and then the electric utility. The wire sizes and ratings should be increased. In residences and offices, energy meters cannot measure the reactive power that affects dissipative circuit elements so the user is not directly penalized in terms of utility costs for the reactive component of the power.

In ideal case the voltage at the utility side is assumed to be an ideal sinusoidal waveform. But actually AC source has small source impedance. Highly distorted current loads affect power line, resulting in distorting AC source voltage. The movement of the source voltage towards to non sinusoidal waveform can affect other equipments which are connected to the same power system.

1.4 Harmonic Current Emission Standards

The harmonic polluting effects of conventional AC rectification must be limited and this is done in accordance with the standards of electricity utility network. To

maintain power system quality, compliance requirements for current harmonic distortion are being enforced by national and international bodies [1], [2], [3].

The EN 61000-3-2 standard defines measurement requirements, ac power source requirements and limits for testing the harmonic current emissions of electronic and electrical equipment. The purpose of EN 61000-3-2 is limitation of harmonic currents injected to the power system. After some changes, this standard applies to any equipment with rated current up to 16 A RMS per phase for 50-Hz, 230-V single-phase systems or 400-V three-phase mains network.

There are 4 different classes in the EN 61000-3-2 that have different limit values. This classification is made according to:

- Number of pieces of equipment in use (how many are being used by consumers)
- Duration of use (number of hours in operation)
- Simultaneity of use (the same types of equipment used on the same time frame)
- Power consumption
- Harmonics spectrum, including phase (how clean or distorted is the current drawn by the equipment)

There are no limits for:

- Equipment with input power $P \leq 75$ W.
- Professional equipment with input power $P > 1$ kW.
- Symmetrical controlled heating elements with input power $P \leq 200$ W.
- Independent dimming devices for light bulb
- Non-public networks.
- Medical equipment (see also 6.)
- Equipment for rated voltages less than 230 VAC (limit not yet been considered).

Equipment can be grouped into 4 classes based on the above criteria as evaluated by the IEC committee members:

Class A: Balanced 3-phase equipment, and all other equipment, except those stated in one of the following classes. Also all equipment does not fall into Class B, C, and D. The maximum odd and even harmonics limits are given in Table 1.1.

Table 1.1 Class A absolute maximum harmonic limits

Harmonic order n	Maximum permissible harmonic current (A)
Odd harmonics	
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \leq n \leq 39$	2.25/n
Even harmonics	
2	1.08
4	0.43
6	0.30
$8 \leq n \leq 40$	1.84/n

Class B: Portable tools, arc welding equipment that is not professional equipment. Harmonic current limits are absolute maximum values and are approximately 1.5 times Class A limits. The limits are given in Table 1.2.

Table 1.2 Class B absolute maximum harmonic limits

Harmonic order n	Maximum permissible harmonic current (A)
Odd harmonics	
3	3.45
5	1.71
7	1.155
9	0.60
11	0.495
13	0.315
$15 \leq n \leq 39$	3.375/n
Even harmonics	
2	1.62
4	0.645
6	0.45
$8 \leq n \leq 40$	2.76/n

Class C: Lighting equipment containing dimmers and gas discharge lamps. There are limits on the second harmonic and also all odd harmonics. The limits are expressed in terms of a percentage of the fundamental current.

Table 1.3 Class C absolute maximum harmonic limits

Harmonic order n	Maximum permissible harmonic current (% of fundamental)
2	2
3	30 x circuit power factor
5	10
7	7
9	5
$11 \leq n \leq 39$	3

Class D: PC, PC monitors, radio or TV receivers. Input power $P \leq 600$ W.

Table 1.4 Class D absolute maximum harmonic limits

Harmonic order n	75 W < P < 600 W Maximum permissible harmonic current (mA/W)	P > 600 W Maximum permissible harmonic current (A)
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13	0.296	0.21
$15 \leq n \leq 39$	3.85/n	2.25/n

Class D limits are very strict to meet as seen in Table 1.4. These limits depend on the equipments' power rating and apply to equipments that are connected to the utility network for a significant part of its life cycle, resulting in great impact on the power supply network. PCs and TVs are examples of such equipment. The current limits for

class D are expressed in terms of mA per Watt of the power consumed. Low-power equipment has very low absolute limits of harmonic current.

All rectifier based power supplies that are directly connected to the mains are generally classified as Class A or Class D. Such converters that have highly distorted current waveform and used more frequently are classified as in Class D. The lower distorted converters fall into Class A. In the power level less than 600 W, Class A has advantages of having higher harmonic limit values (Table 1.1). So designing the converter according to Class A limits is easier than Class D limits (Table 1.4).

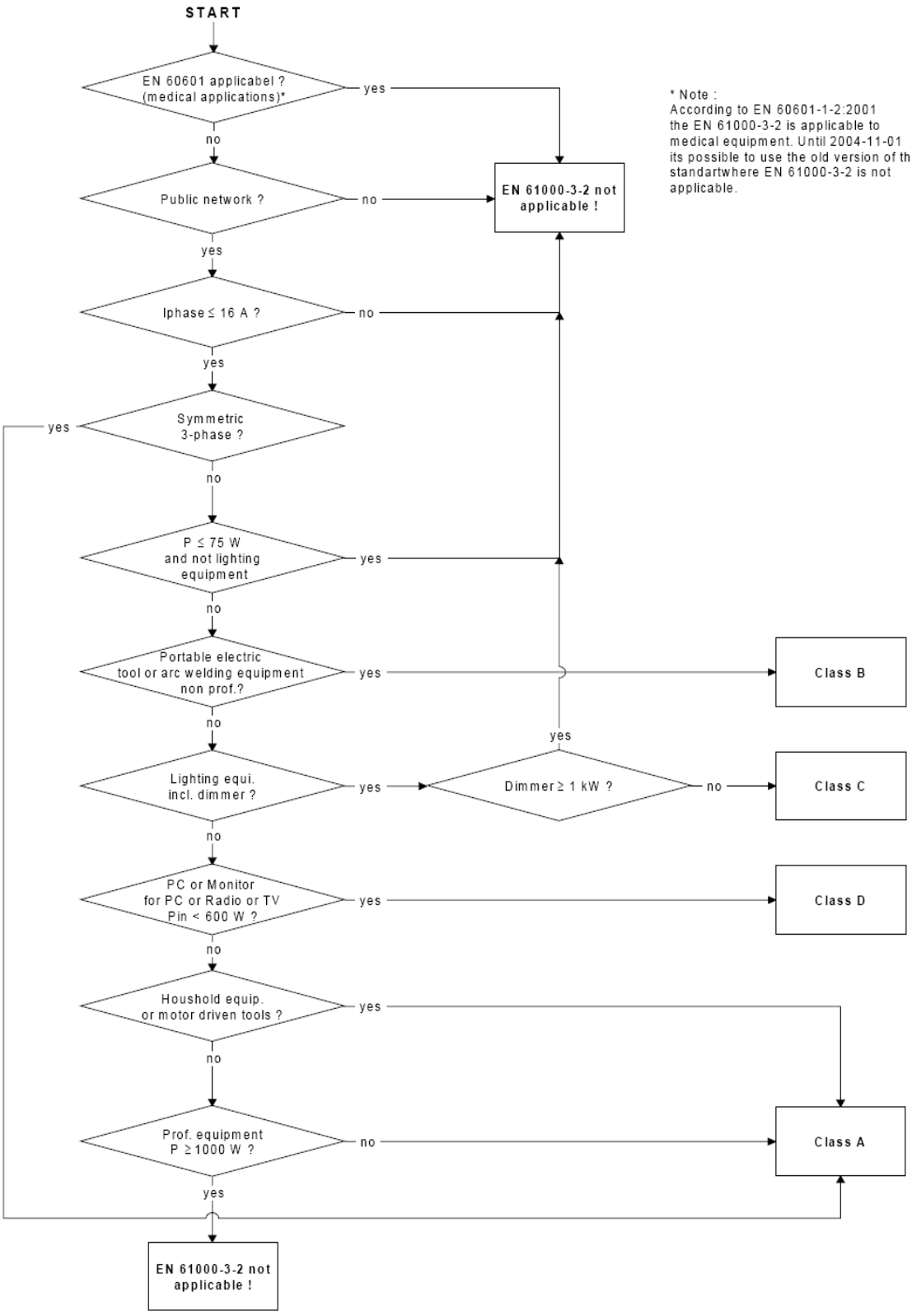


Figure 1.5 Equipment classification chart according to IEC61000-3-2, A14 standard.

The harmonic standards have witnessed some changes during the last decade. At first, The International Electrotechnical Committee- IEC developed the standard IEC 555-2 at 1982. This standard is adapted as European standard as EN 60555-2 at 1987 by the European Committee for Electrotechnical Standardization - GENELEC. Standard IEC 555-2 has been replaced by standard IEC 1000-3-2 in 1995 and this standard is adapted as European standard EN 61000-3-2 by GENELEC.

The version of the standard EN 61000 -3-2 in 1995 has some different classification aspects, especially on Class D equipments. Class D equipments were classified for equipments having an active input power less than or equal to 600 W and a special current waveform. An input current waveform – normalized to its peak value, I_{pk} – which stays within the envelope shown in Figure 1.6 for at least 95% of the duration of each half-period, assuming that the peak of the line current waveform coincides with the center line.

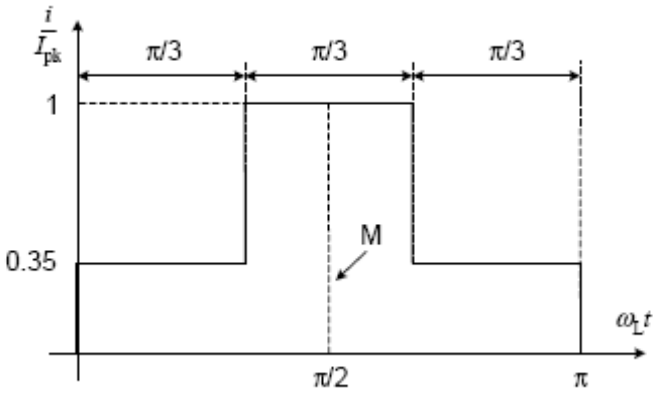


Figure 1.6 Envelope of the input current used to classify Class D equipment, as defined in the first edition of IEC 61000 -3-2.

The standard IEC/EN61000-3-2 has been changed in 2000 and in 2001 with amendment A14. Now the amendment A14 is completely in force. These new changes bring the following specifications:

- Class D is no longer defined by a 'special waveform', and applies now only to television receivers and desktop computers. (Clearly, a switch-mode power supply (SMPS) intended for use in a PC would need to take that into account). In the future, other products may have to be added, but only after a full investigation.

- No limits for equipment using 75 W or less.
- Test configuration with expected maximum THC (Total Harmonic Current, no worst-case search).
- Limits apply only to the power lines, not to the neutral.
- New average power measurement method for fluctuating loads.

Table 1.5 IEC 61000-3-2 changes

	IEC61000-3-2:1995 EDITION 1.0	**IEC61000-3-2:2001 EDITION 2.1**	**IEC61000-3-2:2005 EDITION 3.0**
CLASS D DEFINITION	Special waveform envelope (75W to 600W)	TV, PC and Monitor (75W to 600W)	TV, PC and Monitor (75 to 100W)
MEASUREMENT METHODS	Steady and transitory	Transitory only Transitory only	Transitory only
MEASUREMENT METHODS	16 cycles (320/267ms@50/60Hz)	200 ms (10/12 cycles@50/60 HZ) (16 cycles permitted through 2004)	200 ms (10/12 cycles@50/60 HZ)
DATA MANIPULATION	Transitory only	All data must be smoothed using the 1.5s first order filter	All data must be smoothed using the 1.5s first order filter
PASS/FAIL FOR INDIVIDUAL HARMONICS	Every window result <150% of limit of test time >100% permitted	Every window result <150% of limit 10% of test time >100% permitted	Every window result <150% of limit 10% of test time >100%
CLASS A RELAXATION*	No special provision	No special provision	<200 time of limit only IF >150% for 10% of test time AND average
ODD HARMONICS 21-39*	No special provision	Provision for POHC calculation permitting the average of some individual harmonics to >100%	Provision for POHC calculation permitting the average of some individual harmonics to >100%
CLASS C&D LIMITS	Proportional to measured power (Class D) or current & PF ,Class C	Allows manufacturer o specify test power or current level provided it is within ±10% of the measured value	Allows manufacturer o specify test power or current level provided it is within ±10% of the measured value
TEST/OBSERVATION PERİOD	Not specially defined but to find the max. harmonics emission	Specified to be significantly long enough to acquire ±5% repeatability. If to long select the 2.5 min. max.	Specified to be significantly long enough to acquire ±5% repeatability.
TEST CONDITIONS	Specified to some products	Detailed test procedure for certain product categories	Detailed test procedure for certain product categories. Amended procedure for testing TV from 2001.

1.5 Power Factor Correction Methods

The need for Power Factor Correction brings a lot of new PFC methods and applications. The most important issue is finding optimum PFC solution according to needed application. There are several survey papers in order to help to find the best solution for power factor correction [9], [10], [11], [12], [13]. The Power Factor Correction methods can be classified according to following specifications:

- System level classification (passive, active)
- Number of stages (single stage, two stage)
- Circuit based classification (isolated, non isolated)
- Type of power stages (buck, boost, fly back etc…)
- Waveform based classification (sinusoidal, non-sinusoidal)
- Control methods (current mode, voltage mode)
- The other aspects (power level, cost, complexity, etc…)

Generally, two PFC approaches are commonly used in current power supply products with high power features, i.e., passive approach and active PFC approach. Each one has its merits and limitations and applicable field.

Passive PFC approaches are used in low-power, low-cost applications. Generally, in this approach, an L-C filter is inserted between the AC mains line and the input port of the diode rectifier of ac-to-dc converter. Passive PFC method is simple and low cost but has bulky size and heavy weight and low power factor.

Active solutions are used at high power levels with high PF and low harmonic distortion. We can classify active PFC methods as two stage and single stage by considering number of conversion stages. The most commonly used active approach is the two-stage approach with higher quality. Generally two-stage PFC systems consist of a pre-regulator cascaded with a dc/dc converter. In the first stage, generally called as pre-regulator, a non-isolated boost converter has the role of power factor correction. This front end PFC stage converter generally operates for low harmonic

input current and intermediate dc bus voltage. The second stage operates for required dc voltage level with higher bandwidth. The second stage generally has isolation. The two-stage systems have higher quality with higher PF and low harmonic distortion. However, the two-stage approach causes an increase in the total system cost and manufacturing complexity. Especially in low-power applications, two-stage solutions have higher cost. For reducing system cost and component count, single-stage solutions have been introduced. In the single-stage systems, PFC, isolation and dc voltage regulation are performed in one stage with lower component number.

1.5.1 PFC Design Criteria

Selection of the best PFC method is very important according to application. The following factors are the main selection criteria for a PFC application for selecting right configurations and specifications:

1. What standards and class of equipment needs will the system be required to meet.
2. Required PF, THD, and the other factors
3. Output power level
4. Power flow (unidirectional, bidirectional)
5. Required DC voltage level
6. Input voltage range
7. Isolated or non-isolated
8. Type of load
9. Size and Weight
10. Efficiency
11. Dynamic characteristics such as holding time, ripples, transient, regulation, etc…
12. Environmental effects (temperature, duration, pollution, humidity)
13. Noise level (EMC, EMI, RFI, etc…)
14. Cost

The designer should consider the factors above while designing a PFC circuit with high quality. The right way is finding the best cost-performance solution depending on the application.

1.5.2 Passive Approach

In the passive PFC approaches, passive elements are used to improve the power quality of the power circuit. Passive elements like inductors and capacitors are placed at the inputs or outputs of the diode bridge rectifier in order to improve current waveform. Generally, output voltage is not controlled. Passive PFC systems are dependent on the power system and has low power factor. Generally, line frequency LC filters are used as a passive solution. The simple passive filter with LC components is shown in Figure 1.7. The passive components improve current conduction angle and reduce THD of the input current. Line frequency inductance can be placed either on the dc or ac side of the rectifier. Due to its simplicity, the passive LC filter could be a high-efficiency and low-cost PFC solution in order to meet the IEC 61000-3-2 specifications. Passive power factor correction method meets Class-A/D equipment specifications up to 300 W, at a much lower cost than a comparable switch mode power supply (SMPS) employing active PFC techniques. The passive PFC technique is most suitable for applications with a narrow line voltage range. However, it can be also employed in power supplies operating in the universal line-voltage range (90 - 265 VAC).

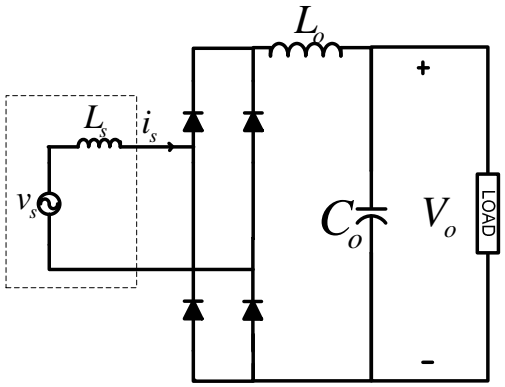


Figure 1.7 Simple passive PFC circuit.

The major advantages of the passive PFC technique are higher efficiency, low complexity, and lower cost. The lower component count and absence of active switches and control circuitry, translate into higher reliability and somewhat smaller size. Also, when compared to active circuits, the losses of the passive filters are lower.

However, the passive filters have heavy and bulky low frequency passive elements like line frequency inductance. The other disadvantage of the passive filters is the unregulated varying dc bus voltage that becomes the input to the dc/dc converter. This varying input voltage has effects on the efficiency of the dc/dc converter. The power factor of passive PFC circuits is around 0.60 - 0.70 and, needs arrangement of component ratings when operated under universal line voltage conditions. Generally a large DC bus capacitance is needed in the output of the rectifier for better hold-up time and low ripple output voltage. Meeting the Class-A harmonic requirements can be easily done by passive filters for low-power applications but class-D applications require passive filters of a bigger size. This bigger size brings higher cost and physically higher dimensions.

1.5.3 Active PFC

Active power factor correction techniques are used for high quality rectifiers. Active PFC circuits shape the input current into a sinusoidal form in phase with line voltage. Besides they provide a regulated dc output voltage. These circuits have resistor behaviors at the line side of the converter. Generally power factor of active PFC circuits is close to unity with lower input current THD around 3 %. Active PFC circuits have small size but these systems have higher manufacturing cost and complexity. A DC-DC converter operates as an active shaper in the range of 10 kHz to hundreds of kHz. Active switches are used in conjunction with reactive elements in order to increase the effectiveness of the line current shaping and to obtain controllable output voltage. Higher operation frequency provides smaller size of reactive components such as inductors.

Traditionally, the implementation of power factor correction circuits has been accomplished by using analog controllers. Active PFC can achieve high power factor controlled by analog circuits using several methods. Various analog PFC ICs are available in the electronic markets, which are manufactured by TI/Unitrode, Fairchild, Onsemi and others manufacturers. Complete list of the available PFC ICs and the specifications will be given in the appendix. Analog control is simple and low cost. Continuous operation and higher operating dynamics make the analog control suitable. But analog control has higher element count. Analog control methods are also application dependent. It is hard to adopt a new operating condition when a change is needed. The system should be redesigned from scratch. Recently, power supplies are implemented by digital controllers. Recent developments in digital control techniques and low cost digital control ICs make digital control optimum for power supply applications. It is not easy to maintain the available control methods with digital controllers, because these control methods require high-speed calculations and high-speed analog to digital conversions. The operating frequency and the speed of the digital control devices are limited. New control strategies have been developed suitable for digital operations. Digital systems need lower component count then analog systems, so size of the digital implementations are smaller. Digital systems are flexible and can be operated under different conditions by software based control strategies.

The single-phase active PFC techniques can be divided into two categories: the two-stage approach and the single-stage approach shown in Figure1.8.

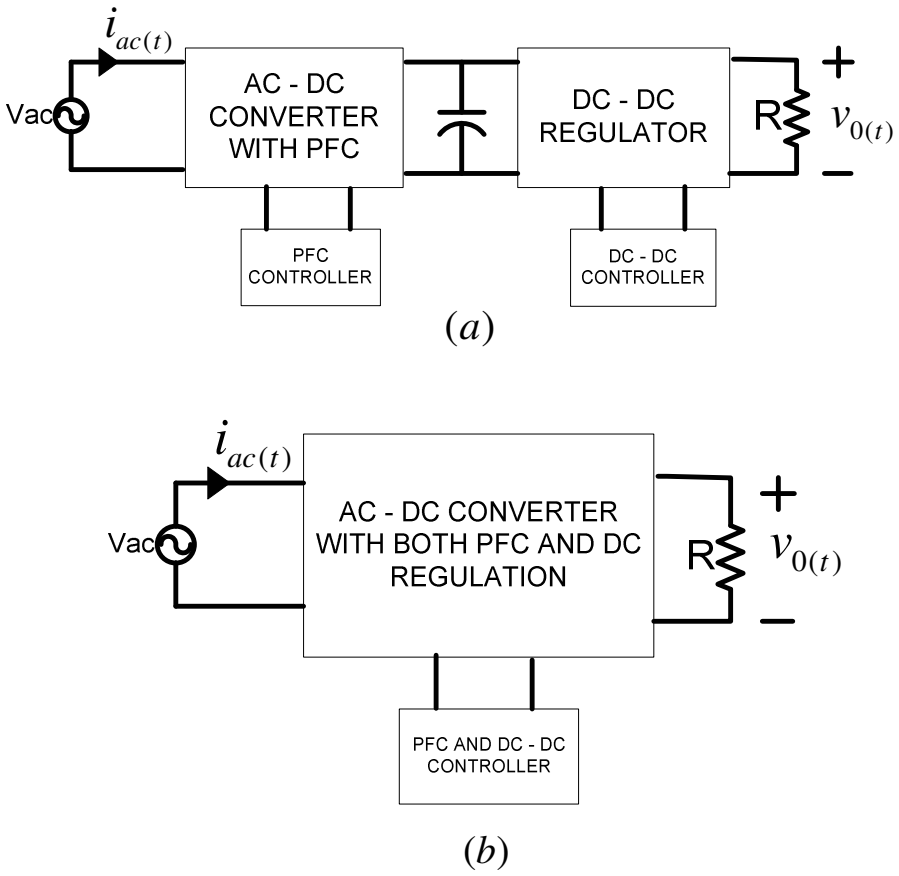


Figure 1.8 a) Two-stage PFC b) Single-stage PFC.

1.5.3.1 Active Two-Stage Approach

The most popular scheme for power factor corrected AC-DC power supplies is the two-stage approach. In this approach, two converters share power factor correction and dc voltage regulation roles. The front-end converter operates as power factor corrector while shaping line current, therefore achieving unity input power factor. The PFC front-end stage operates as dc-dc converter with regulating output voltage and provides isolation if needed. Both converters are controlled separately. Independent PFC controller provides sinusoidal input current with intermediate regulated output voltage. Second DC-DC controller provides tight regulated output voltage with high bandwidth.

The first PFC stage can be a boost, buck/boost or fly back or can assume any other power converter topology. Generally, the boost type topology shown in Figure 1.9 is so far the most popular configuration. It provides input-current shaping with low-bandwidth control. With the boost-type topology, the system has some advantages such as:

- The inductor current and the input current have the same waveform so it is easy to apply current mode control over boost inductor.
- The system has lower EMI with the help of series boost inductor with the ac line. Input current can be continuous or discontinuous.
- The switching element such as MOSFET or IGBT is parallel to the power line. The system has better efficiency and low noise. But it requires extra protection to input- output short circuit and start-up spikes.

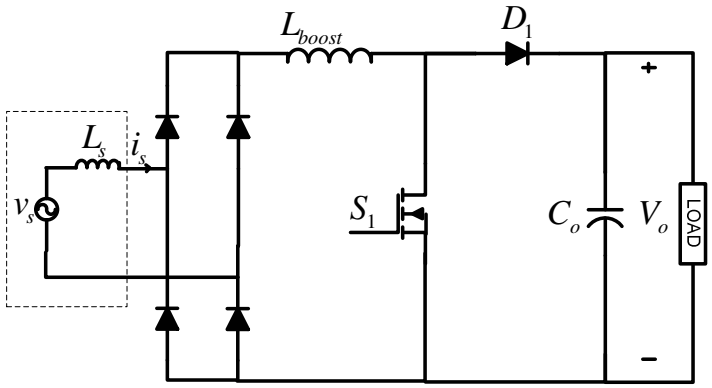


Figure 1.9 Boost type active PFC.

The boost-type PFC can be operated in continuous-conduction-mode (CCM), discontinuous-conduction-mode (DCM), variable-frequency critical (boundary) conduction mode. There are several control methods for high power and low current THD. This thesis is concerned with the control methods of boost type active PFC which are implemented experimentally. Popular control methods are explained and the results are given by computer simulations and experimentally.

In summary, the active two-stage PFC converter has good input power factor and can be used in wide ranges of input voltage and output power. However, the two-stage approach suffers from an increased circuit complexity since it requires two switches and two controllers with associated circuitry. It is very undesirable for low-power supplies used in consumer electronic products. In the high power applications, the two-stage system seems the best solution.

1.5.3.2 Active Single-Stage Approach

If the aim for designing PFC solution for an available AC-DC converter is only meeting the harmonic standards with lower harmonic quality and lower manufacturing cost, the single-stage systems are suitable methods for power factor correction. In the single-stage approach, PFC and dc voltage regulation are made by one controller. Most single-stage topologies combine the input current shaping with the dc/dc down-conversion in a single stage. Single-stage solution with single switch seems to be the right solution at lower power levels (< 200 W), because reduced component count and cost of the PFC stage provide a cheaper solution than two-stage systems. The only controller is the DC/DC controller, which focuses on the tight regulation of the output voltage. The input power factor of a single-stage converter is not unity, but its input current harmonics are small enough to meet the specifications, such as the IEC 61000-3-2 class D. Generally, the active single-stage approach offers a performance (THD and PF) which is better than the corresponding performance of the passive solution, but not as good as that of the active two-stage approach. The primary advantages of this approach are lower part count and cost than two-stage PFC topologies. With these technologies, the PF is typically >0.75 and THD is typically <80%. The major deficiency of any single-stage circuit is that the voltage of the internal energy-storage (bulk) capacitor varies with the line voltage and load current. Because of all process is done by single controller, the system has higher control complexity.

1.5.4 Comparison of PFC Solutions

The above mentioned three solutions for power factor correction have advantages over the other according to application and usage. A summary of the three methods is given below:

Passive harmonic line current reduction

- Simple and not complex circuit
- Large and bulky low frequency reactive elements
- Less costly than active PFC
- Redesign needed for wider operation range
- No sinusoidal input current

Active harmonic line current reduction

- High power factor (close to unity) and lower THD of line current
- Higher cost and component count
- Complex to control and design
- Increased noise such as EMI, RFI

In Figure 1.10, the input voltage and current waveforms are shown for three operations.

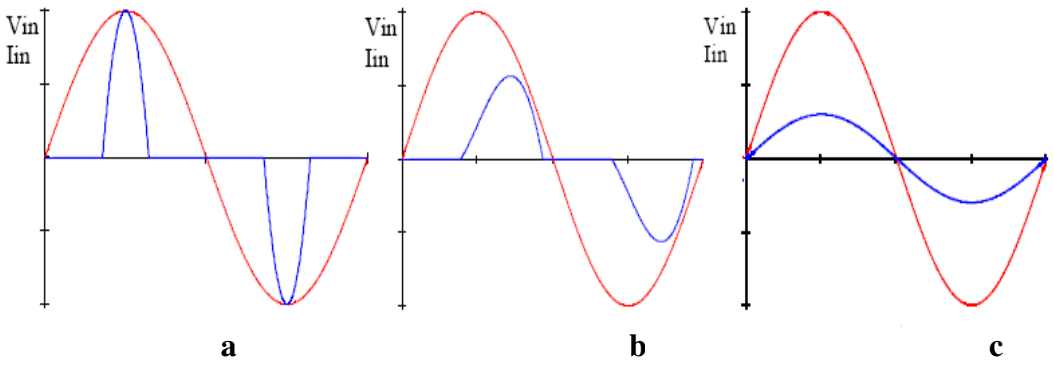


Figure 1.10 Waveforms without/with PFC

a) Without PFC b) passive PFC c) active PFC.

According to the above evaluation, the designer can choose best solution for power factor correction considering selection criteria, especially power level for single-phase power conversion. If the output power is less than 200 W, single-stage PFC and the passive PFC are valid options. Above 200 W, the conventional two-stage PFC seems to be the best choice. If the purpose is to obtain a sinusoidal line current, the classical two-stage approach is the best option mainly if universal line voltage operation is required. Passive solutions are adequate in low power for simplicity. Single-stage solutions are a good option to meet the low frequency harmonic regulations in low power applications with low cost [9]. A comparison chart is given in Table 1.6.

Table 1.6 Comparison table of three solutions

	PASSIVE	**ACTIVE TWO-STAGE**	**ACTIVE SINGLE -STAGE**
THD	High	Low	Medium
POWER FACTOR	Low	High	Medium
EFFICIENCY	High	Medium	Low
SIZE	Medium	Large	Small
WEIGHT	Very High	Low	Low
BULK CAP. VOLTAGE	Varies	Constant	Varies
CONTROL	Simple	Complex	Simple
COMPONENT COUNT	Very low	High	Medium
POWER RANGE	< 200-300W	Any	< 200-300W
DESIGN DIFFICULTY	Low	Medium	High

1.6 Objective and Organization

The aim of this thesis is to design an educational test bench that shows power factor correction basics. The test system will have modular structure with an easy-to-implement PFC application on it. The system consists of required power supplies and load groups, measurement devices, passive solutions and active solutions. Popular solutions will be implemented by the laboratory experiments.

First, the single-phase bridge rectifier will be analyzed and the available solutions will be discussed. Passive filter methods are the easiest way to lower the current harmonics but they are bulky and oversized. The active solutions have the best performance in the power factor correction area but it is more complex to design them. Also manufacturing cost is higher than passive solution. One of the aims of this thesis is to show different solution methods. In fact, it will be shown that, the selection of the solution is application dependent.

This thesis is organized in seven chapters. The current (first) chapter covers the basics of the power factor correction, harmonic current standards and general solutions for power factor correction. The second chapter deals with popular passive power factor correction methods. Different techniques will be analyzed and theoretical and experimental results will be verified. Also, designing passive solutions to comply with harmonic current standards will be discussed. Average current mode controlled active PFC is the main subject of the third chapter. Average current mode control with boost type converter will be implemented by using UCC3818 IC. Borderline control is analyzed in chapter four. The circuit is implemented by MC34262. The other active control technique, One Cycle Control, is discussed in chapter five. The control methods utilized are selected according to their usage, performance, and popularity. An experiment manual is prepared and verified in chapter six to help the user to understand the basics of power factor correction by the experiments carried out in the laboratory. Finally, conclusion chapter covers the advantages and disadvantages of the power factor correction solutions analyzed in the thesis.

CHAPTER 2

PASSIVE POWER FACTOR CORRECTION

2.1 Single Phase Full-Wave Rectifier

Generally, most of the AC-DC power supplies consist of a full bridge diode rectifier as an input stage. A bulk capacitor is installed to the output of the rectifier to regulate the output DC voltage. As mentioned in the previous chapter, the load of the rectifier requires low ripple supply voltage. The large capacitor supplies low ripple DC output voltage but this shortens considerably the input current's conduction duration. Short current conduction interval results in a narrow pulsed current waveform. This current waveform is rich in harmonics that have negative effects on the main side of the system as explained in Chapter 1.

A typical single-phase full bridge diode rectifier is shown in Figure 2.1 with supply impedance and large output capacitor filter.

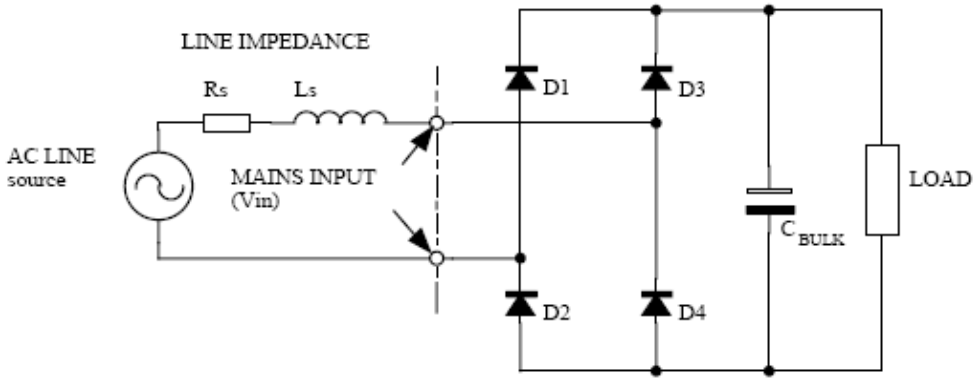


Figure 2.1 Typical single-phase rectifier.

The short conduction times for diode rectifier causes short current conduction interval because the diodes conduct only when the input voltage is greater than the output capacitor voltage. This period is short when the output capacitor is fully charged. The general current and voltage waveforms for a single-phase rectifier with large output capacitor are given in Figure 2.2.

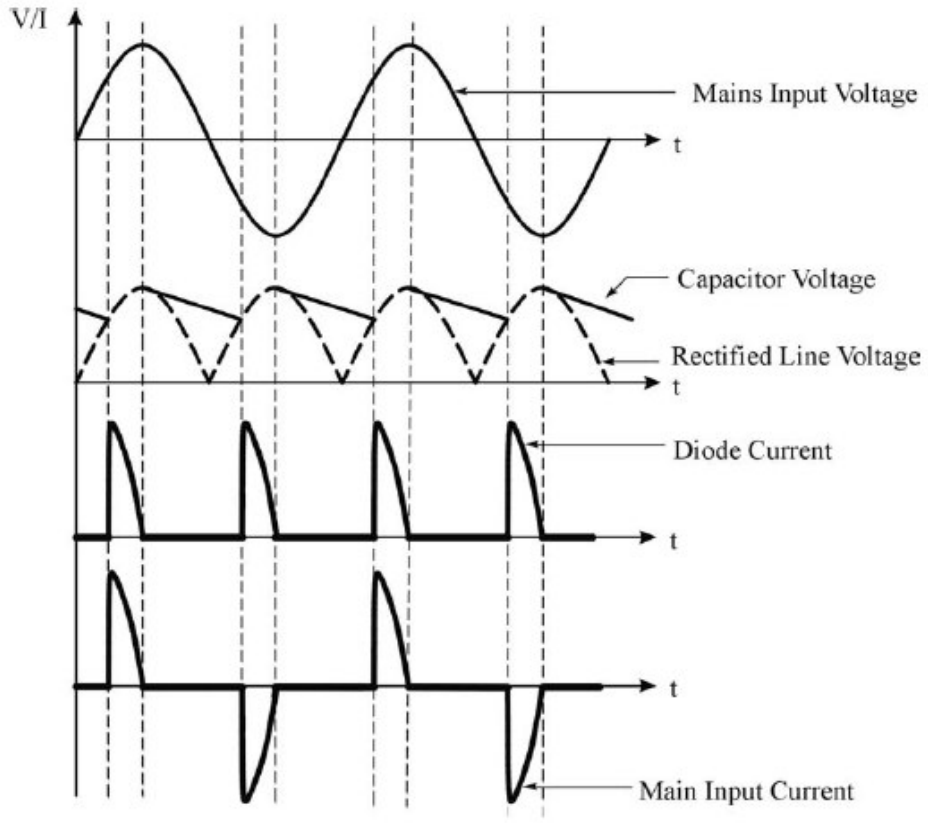


Figure 2.2 Current and voltage waveforms.

The short period, pulsed input current consists of higher amplitude odd harmonics. Higher current harmonics mean higher harmonic distortion of the line current. In the case of very large output capacitor, total harmonic distortion of the current is larger than 100% and the power factor is around 0.5. Typical current harmonics are shown in Figure 2.3.

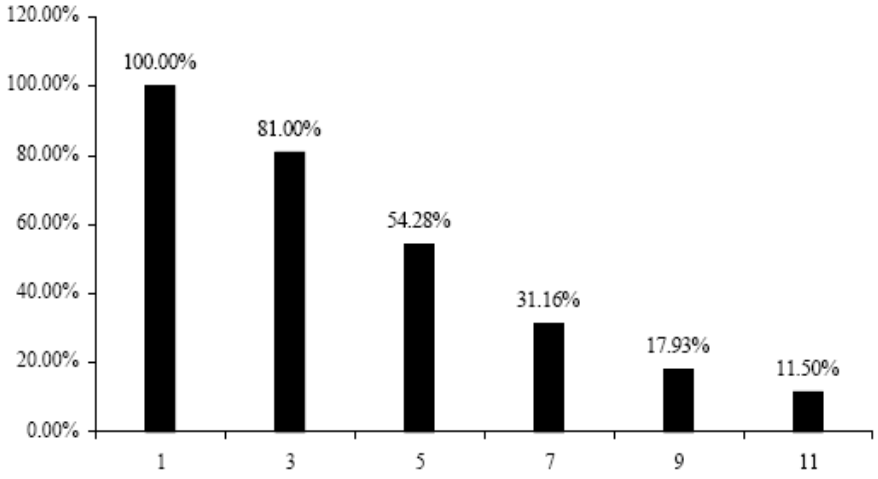


Figure 2.3 Current harmonics.

An experimental system for single-phase full bridge diode rectifier is set up and the voltage and current waveforms are displayed. The output capacitor is large enough to ensure a low-ripple output dc voltage and the load of the system is assumed to be a constant-power DC load such as in a DC-DC converter. As shown in Figure 2.4, input current has pulsed waveform with high peak values. It can be seen that, input voltage has some distortions due to distortion in the line current (voltage drop in line impedance). The line impedance can reduce the peak of the line current. If the AC-DC converter is close to distribution network has lower impedance and diode rectifier draws higher peak current. If the AC-DC converter is far from distribution network has higher line impedance and diode rectifier draws lower peak current. This means line voltage distortion is smaller.

The parameters of the 200-W single-phase rectifier system are given in Table 2.1. The corresponding input current and voltage waveforms are shown in Figure 2.4.1

Table 2.1 Experimental parameters of 200-W rectifier

Output Capacitor	330 μF
Input Voltage (V_{rms})	230 V
Output Power	200 W
R load	480 Ω

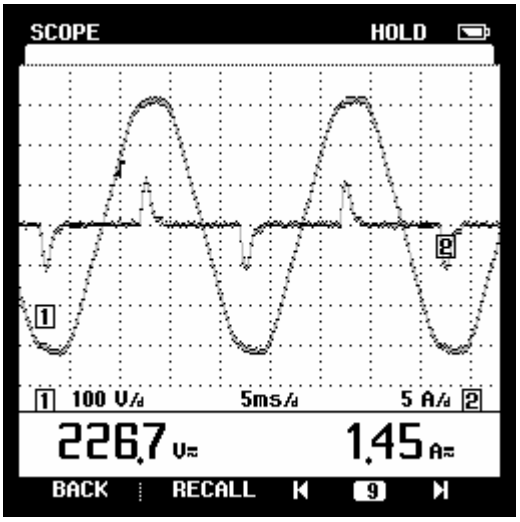


Figure 2.4.1 Input current and voltage waveforms for single-phase rectifier. (Scales: 100V/div, 5A/div)

The input current has higher odd line harmonics as shown Figure 2.4.2. The harmonic content of the line current is above the limits predefined in the EN 61000-3-2 harmonic standard. The designer or manufacturer should reduce the harmonic contents by power factor correction methods.

Table 2.1 Experimental results for 200-W rectifier

V_{in}	I_{in}	P_{in}	V_o	I_o	P_o	THD	I_{fund}	I_{3th}	I_{5th}	PF
226Vrms	1.47Arms	200W	302Vdc	0.6A	180W	85%	0.77A	0.7A	0.6A	0.52

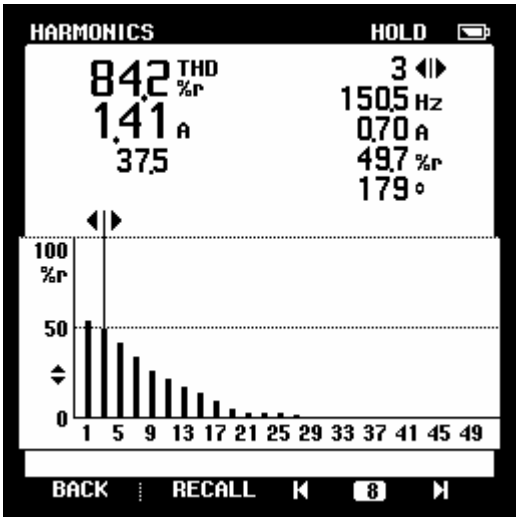


Figure 2.4.2 Input current harmonics spectrum for 200W single-phase rectifier.

The output capacitor defines the shape and the amplitude of the input line current. Large value of output capacitor provides low ripple output voltage, however input current has small conduction period, because diode rectifier conducts only when input voltage is higher than output capacitor voltage. In this condition, input current has significant harmonics and system has lower power factor. Input current distortion can be reduced by using a smaller output capacitor. With smaller capacitance filter, output voltage increases and the current conduction interval widens. This method is very easy to implement and cheaper than other solutions, but the load is directly affected by increased output voltage ripple. In the SMPS applications, generally a DC-DC converter is inserted after diode bridge rectifier. This DC-DC converter is designed assuming that the input voltage is stable and well regulated. In the case of small output filter capacitance, it is hard to implement a constant power DC-DC converter with variable input voltage. This solution can be applied if the load accepts a largely pulsating DC supply voltage and it is used, for example, in some handheld tools.

A single-phase diode bridge rectifier with capacitive filter is simulated for different values of output capacitor filter. The filter capacitor is selected for two different values, 0.5 μF/W and 2.35 μF/W. A 200-W constant power loaded single-phase rectifier is simulated by SIMPLORER simulation tool. The input current waveforms

and output voltage waveforms are shown in Figures 2.6 and 2.7.

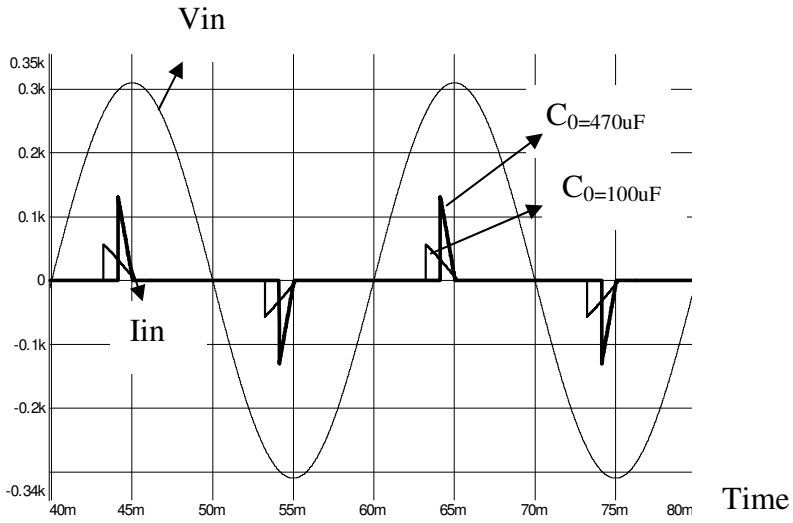


Figure 2.5 Simulated input voltage and current waveforms with capacitive filter.

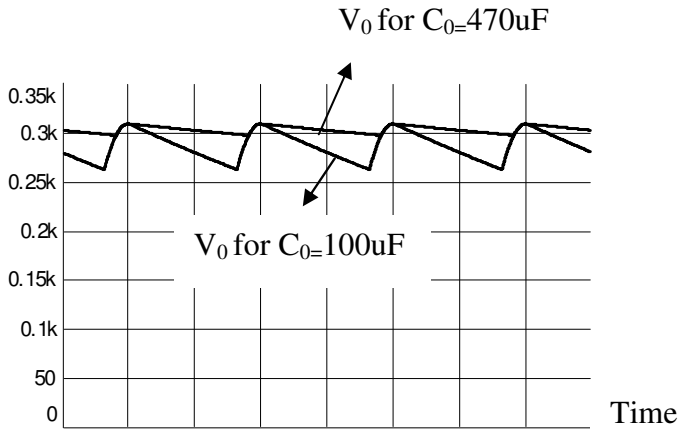


Figure 2.6 Simulated output voltage ripple with capacitive filter.

It can be seen from these figures that, when output capacitor is reduced, input current conduction interval increases, however output voltage ripple increases also. Usually, this increased output ripple is unwanted in the switch mode power supply applications. The input current harmonics for different capacitance filters are shown in Figures 2.8 and 2.9.

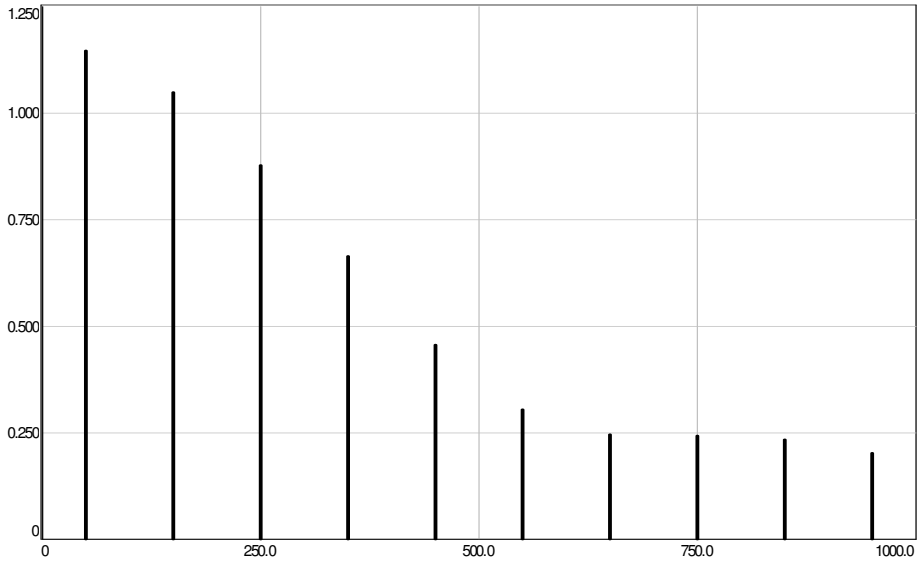


Figure 2.7 Current harmonics spectrum for C_o = 100 μF.

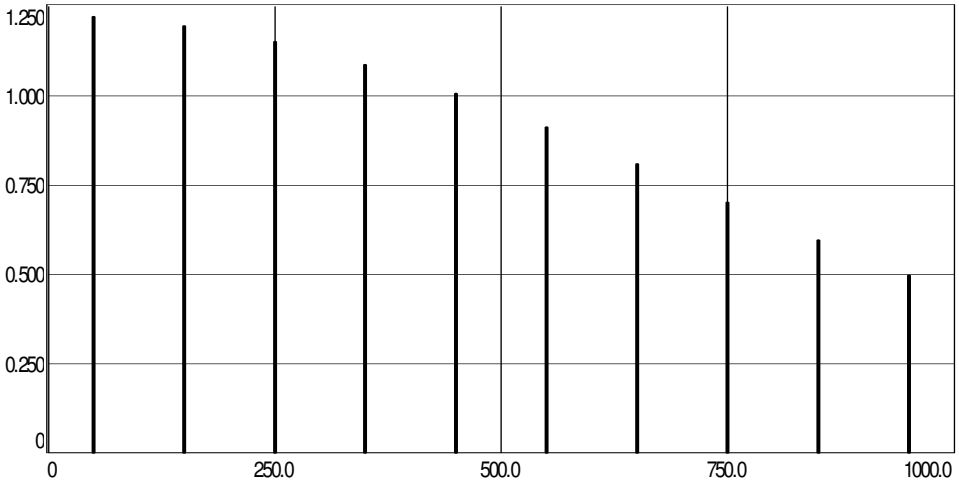


Figure 2.8 Current harmonics for C_o = 470 μF.

Reducing output filter capacitor methods cannot provide full compliance with the EN 61000-3-2 standard and has some drawbacks:

- Higher ripple in the output voltage of rectifier
- Higher THD of line current
- Lower power factor

This method is low cost and easy to implement. There are several passive power factor correction methods in the literature. The most popular and often used passive factor correction methods are investigated next.

2.2 Passive Power Factor Correction Methods

Passive power factor correction is implemented by connecting passive elements to the diode bridge rectifier. There are various combinations of passive elements for power factor correction with different circuit topologies [14], [15], [16], [17], [18]. Before the harmonic limiting standards, the investigators have designed passive solutions for better PF and efficiency because there were no limits for current harmonics. After the IEC 61000-3-2 standard was accepted, the designers had to change the previous solutions or design new circuits obeying the standards. In this thesis, three of the various passive power factor correction techniques are investigated in detail and simulation and experimental results are verified. These are:

- **LC filter**
- **Series Connected Parallel Resonant Filter**
- **Variable Inductance LC filter**

2.2.1 LC Filter Method

The simplest passive solution to comply with the EN 61000-3-2 standard is LC filter method. Passive LC filter power factor correction can be done by connecting one inductor to the capacitive filtered diode bridge rectifier. Filter inductor can be placed either on the AC side or DC side. When the inductor is connected to the AC side, current harmonic distortion can be reduced by large inductance but voltage drop (reduced output power) in the inductor will be large. By connecting the filter

inductor to the DC side, output power will be independent from filter inductance but harmonic limiting capability will be lower than inductor in the AC side.

In this section, the design of single-phase diode bridge rectifier with output LC filter complying with the EN 61000-3-2 standard is given. In the design the following criteria are considered.

- Standard compliance
- Maximum Power Factor
- Minimum Line Current Harmonic
- Cost and Size

Optimum solutions satisfying the above criteria are given. A general single-phase diode rectifier with LC filter is given in Figure 2.10. While designing LC filter, input voltage is assumed as a zero-impedance source and diode rectifier is assumed lossless (ideal diodes). The output power and output voltage are assumed constant (large output capacitor).

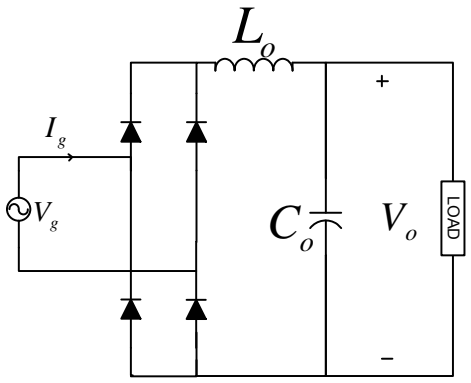


Figure 2.9 Single-phase rectifier with LC filter.

Single-phase rectifier in Figure 2.10 is normalized with respect to the references values in order to analyze the rectifier system with variable elements, especially filter inductance. The normalized diagram of single-phase rectifier with LC filter is given in Figure 2.11.

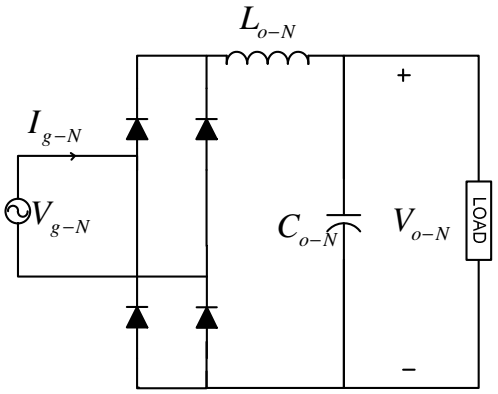


Figure 2.10 Normalized single phase rectifier.

The circuit can be analyzed easily by normalization procedure [19], [20], [21]. The operation modes of the circuit and the current waveforms depending on the output filter inductance can be evaluated using normalization methods. The circuit variables are converted to the normalized values by using reference values. In the rectifier system three main reference values are utilized. These are voltage, current and the time references. The voltage reference value ($V_{g\ (ref)}$) can be defined as the rms input voltage V_g. The current reference ($I_{g\ (ref)}$) can be defined as the ratio of power reference ($P_{g\ (ref)}$) to voltage reference ($V_{g\ (ref)}$). Finally the time reference (T_{ref}) can be defined as the line period (1/50 Hz). The new normalized values are given in the following equations. The –N subscript indicates normalized quantity.

$$t_N = t / T_{ref} \tag{2.1}$$

$$T_N = T / T_{ref} \tag{2.2}$$

$$V_{g-N} = V_g / V_{ref} \tag{2.3}$$

$$I_{g-N} = I \Big/ I_{ref} \tag{2.4}$$

$$V_{o-N} = V_o \Big/ V_{ref} \tag{2.5}$$

$$P_{in-N} = P_{in} \Big/ P_{ref} \tag{2.6}$$

The normalized value of filter inductance can be defined by rearranging voltage balance equation of the inductance. The voltage drop (V_L) on L_0 can be written as:

$$V_L = L_O \frac{dI_L}{dt} \tag{2.7}$$

Equation 2.7 can be rewritten by using normalized values of voltages and currents as:

$$V_{L-N} V_{g(ref)} = L_O \frac{dI_{L-N} I_{g(ref)}}{dt_N T_{ref}} \tag{2.8}$$

The normalized voltage equation can then be written as:

$$V_{L-N} = L_O \frac{I_{g(ref)}}{V_{g(ref)} T_{ref}} \frac{d\dot{I}_{L-N}}{dt_N} = L_{O-N} \frac{d\dot{I}_{L-N}}{dt_N} \tag{2.9}$$

The normalized value of the output filter inductance then becomes:

$$L_{O-N} = L_O \frac{I_{g(ref)}}{V_{g(ref)} T_{ref}} = L_O \frac{P_{g-(ref)}}{V^2_{g-(ref)} T_{ref}} \tag{2.10}$$

Finally the normalized expression of the output capacitor is expressed as:

$$C_{O-N} = C_O \frac{V_{g(ref)}}{I_{g(ref)} T_{ref}} = C_O \frac{V_{g-(ref)}^2}{P_{g-(ref)} T_{ref}} \tag{2.11}$$

The normalized single-phase rectifier is simulated for different values of the inductance filter with the following parameters by using SIMPLORER simulation tool and DAY-POST PROCCESSOR analyzer tool. $V_{g\text{-}N}$ and $P_{in\text{-}N}$ are assumed to be 1.0, and the normalized output capacitance is chosen very large, such as $C_{0\text{-}N}$=1000. Power factor (PF), Displacement factor (K_d) and Distortion factor (K_p) values are verified.

The operation modes of the rectifier can be classified according to the input current waveform characteristics. The output filter inductance defines the input current waveform in the case of large output capacitor and constant power load. In Figures 2.12, 2.13, 2.14, simulation results of the input current waveform with different output filter inductances are given.

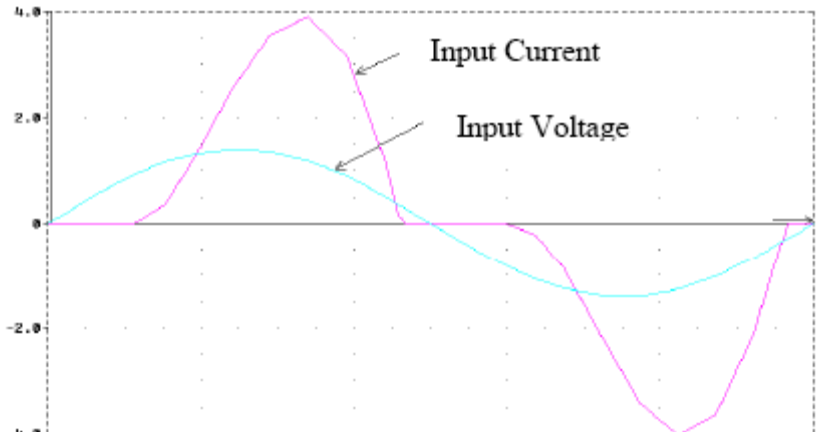


Figure 2.11 Simulation waveforms for $L_{0\text{-}N}$=0.01.

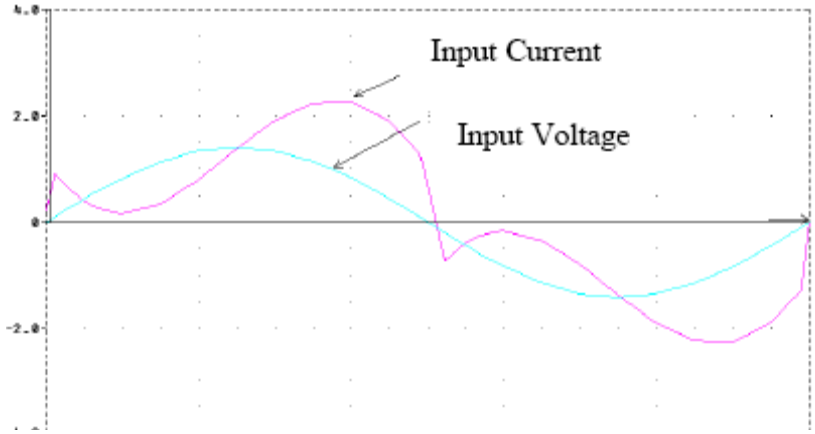


Figure 2.12 Simulation waveforms for $L_{0\text{-}N}$ =0.043.

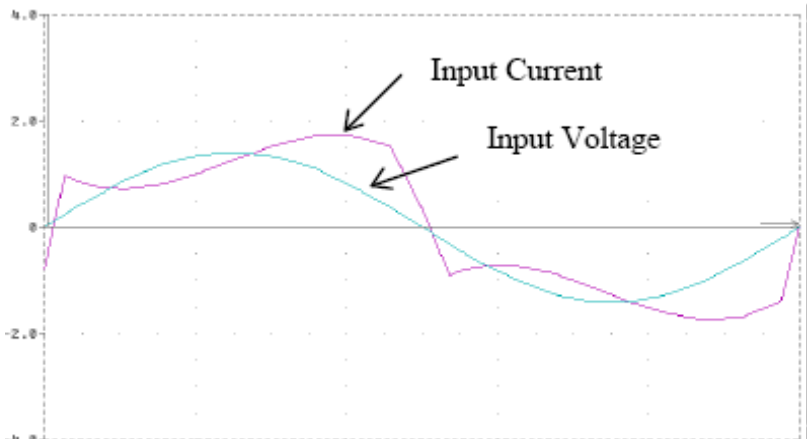


Figure 2.13 Simulation waveforms for $L_{0\text{-}N}$ =0.09.

The operating modes can be defined as Discontinuous conduction mode I (DCM I), Discontinuous conduction mode II (DCM II), and Continuous conduction mode (CCM) [19]. The system operates in the DCM I when the current has short conduction duration and a high peak value with $L_{0\text{-}N}$ =0.01 as shown in Figure 2.12. The system operates in the DCM II when the current has smaller zero time duration with $L_{0\text{-}N}$ =0.043 the figure 2.13. The system operates in the CCM I with $L_{0\text{-}N}$ =0.09 as shown in Figure 2.14 when the current has no zero current interval.

The optimum filter values can be selected according to power factor (PF), displacement factor (K_d) and distortion factor (K_p) curves due to various output filter inductance values. The simulation results are given in Figure 2.15 [20].

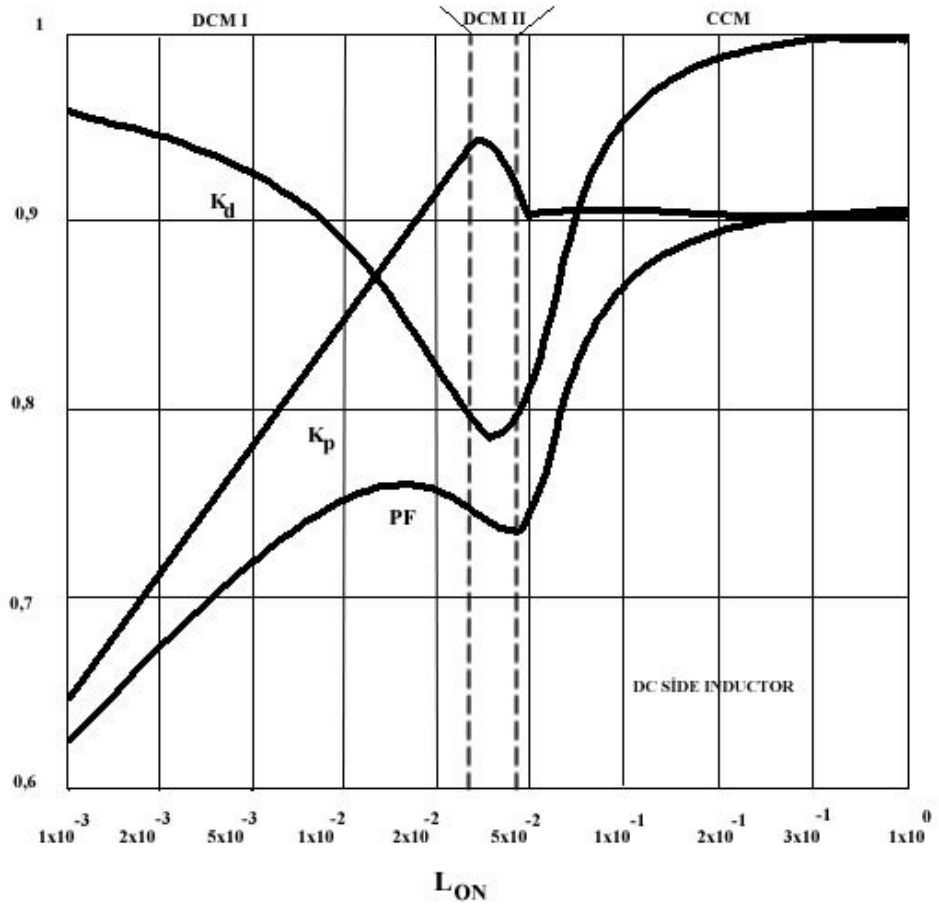


Figure 2.14 Power factor (PF), Displacement factor (K_d) and Distortion factor (Kp) as function of $L_{0\text{-}N.}$

As can be seen from Figure 2.15, the rectifier operates in DCM I for $L_{0\text{-}N} < 0.027$. For $0.027 < L_{0\text{-}N} < 0.043$, the rectifier operates in DCM II. For $L_{0\text{-}N} > 0.043$, the rectifier operates in CCM [19], [20]. The maximum power factor can be evaluated in the CCM region to be approximately equal to 0.9. However in this region the filter inductance has a very large value and it is impractical. The maximum power factor for discontinuous conduction mode operation can be evaluated for $L_{0\text{-}N} = 0.016$ in DCMI.

When the distortion factor is increased, the total harmonic distortion is decreased. The maximum distortion factor is $K_{p\text{-}max} = 0.936$ for $L_{0\text{-}N} = 0.03$ in DCM II, which corresponds to a THD = 37.6%. In the CCM region, K_p is independent of $L_{0\text{-}N}$.

If the aim of designing passive solution is to comply with the EN 61000-3-2 standard, filter elements should be designed according to the current harmonic limits predefined in the standard. The defined classes in the standard have different current harmonic limits so the passive solution changes due to the application class of the converter. In this section, the required minimum filter values are calculated in compliance with the EN 61000-3-2 standard for Class A and D applications.

For Class D application, the harmonic limits according to EN 61000-3-2 standard is given in Table 2.3. For direct comparison of the actual current harmonics with the harmonics standards shown in Table 2.3, the harmonic limits are converted to the normalized values by using reference values.

Table 2.3 Class D absolute maximum harmonic limits

Harmonic order n	75 W < P < 600 W Maximum permissible harmonic current (mA/W)	P > 600 W Maximum permissible harmonic current (A)
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13	0.296	0.21
$15 \leq n \leq 39$	3.85/n	2.25/n

The normalized harmonic limits can be written by using the values in Table 2.1 and the reference values as [21]:

$$I_{Ng(2i+1)} = \frac{P_{ref} HL_{(2i+1)ClassD}}{I_{ref}} = V_{ref} HL_{(2i+1)ClassD} \quad , \quad i = 1.....19 \tag{2.12}$$

where $HL_{(2i+1)ClassD}$ is the limit shown in Table 2.3 for the $(2i+1)^{th}$ order harmonic. The normalized harmonic limits and the simulated results for normalized 3^{rd}, 5^{th} and

7^{th} harmonic currents for 230-V system are given in Figure 2.16.

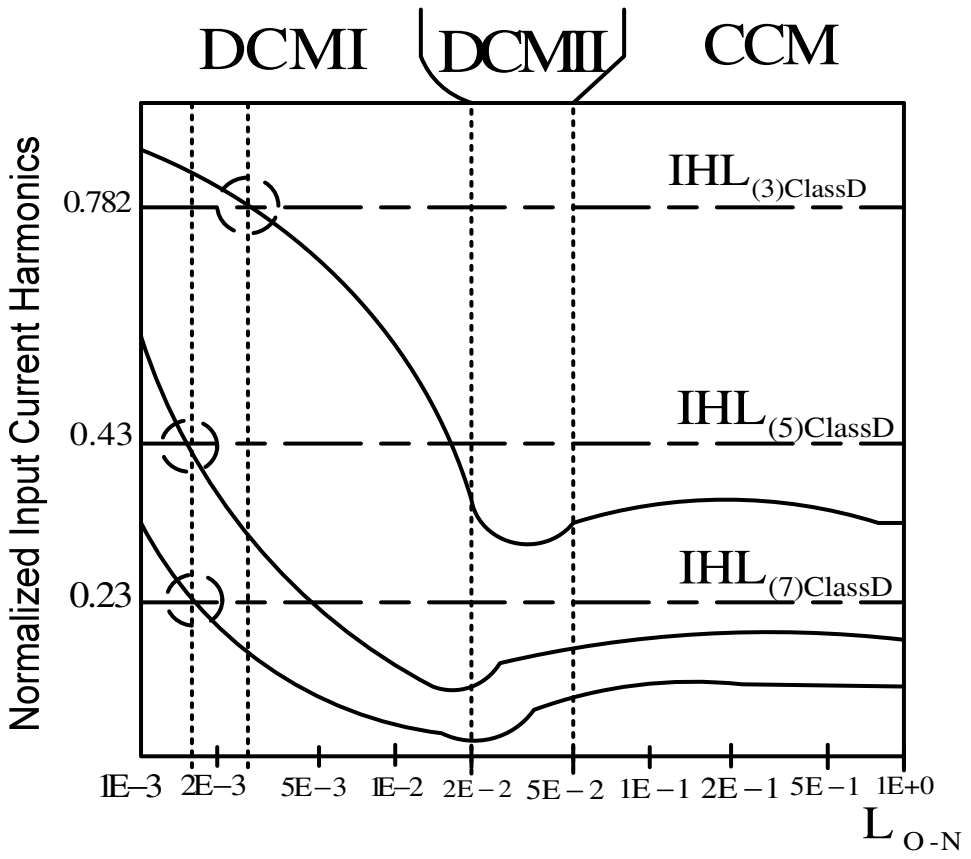


Figure 2.15 Normalized class D harmonic limits and normalized input current harmonics versus normalized filter inductance $L_{0\text{-}N.}$

From Figure 2.16, the required minimum inductance can be selected in order to comply with the EN 61000-3-2 standard for Class D. The value of the minimum normalized inductance is approximately $L_{0\text{-}N}$ = 0.004 and defined by the 3^{rd} harmonic. The required inductance for the power level between 75-600 W can be calculated by using (10) and assuming $L_{0\text{-}N}$ =0.004. The system parameters are Vg = 230 V and f = 50 Hz. Figure 2.17 shows the required minimum inductance for different power levels, obeying to the Class D limits in the standard EN 61000-3-2.

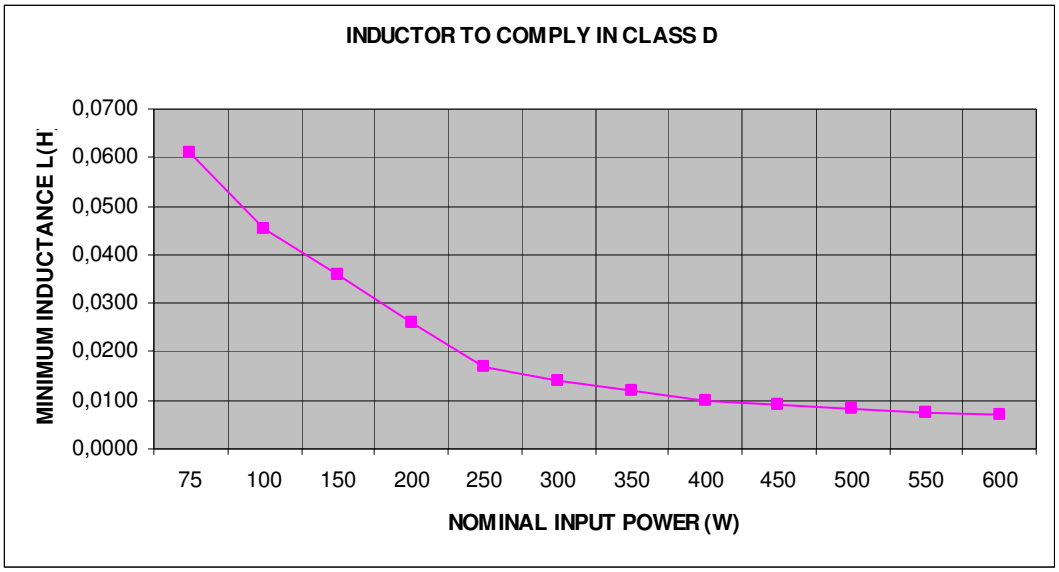


Figure 2.16 Minimum required inductance to comply with EN 61000- 3-2 Class D harmonic limits.

For Class-A application, the harmonic limits according to EN 61000-3-2 standard is given in Table 2.4. For direct comparison of the actual current harmonics with the Class-A harmonics standards in Table 2.4, the Class-A harmonic limits are converted to the normalized values by using reference values.

Table 2.4 Class-A absolute maximum harmonic limits

Harmonic order n	Maximum permissible harmonic current (A)
Odd harmonics	
3 5 7 9 11 13 $15 \leq n \leq 39$	2.30 1.14 0.77 0.40 0.33 0.21 2.25/n
Even harmonics	
2 4 6 $8 \leq n \leq 40$	1.08 0.43 0.30 1.84/n

The normalized harmonic limits can be expressed by using the values in Table 2.4 and the reference values as:

$$I_{Ng(2i+1)} = \frac{IHL_{(2i+1)ClassD}}{I_{ref}} = \frac{V_{ref} HL_{(2i+1)ClassA}}{P_{ref}}, \quad i = 1.....19 \tag{2.13}$$

where $IHL_{(2i+1)ClassD}$ is the limits shown in the table 2.2 for $(2i+1)^{th}$ harmonics. It can be seen from equation (2.13) that the normalized current harmonic limit for Class A is dependent on both the input voltage and the input power. Input voltage reference is assumed to be 230 V. The required minimum normalized inductance is calculated for different power levels. First the normalized harmonic limits are calculated for different power levels for 75-600 W, then the normalized current harmonics of the rectifier are calculated according to various normalized filter inductances. Then the minimum intersections are taken as the required minimum inductance. In Figure 2.18, the required minimum filter inductance for power levels between 75-600 W is shown, which complies with the EN 61000-3-2 Class-A standards.

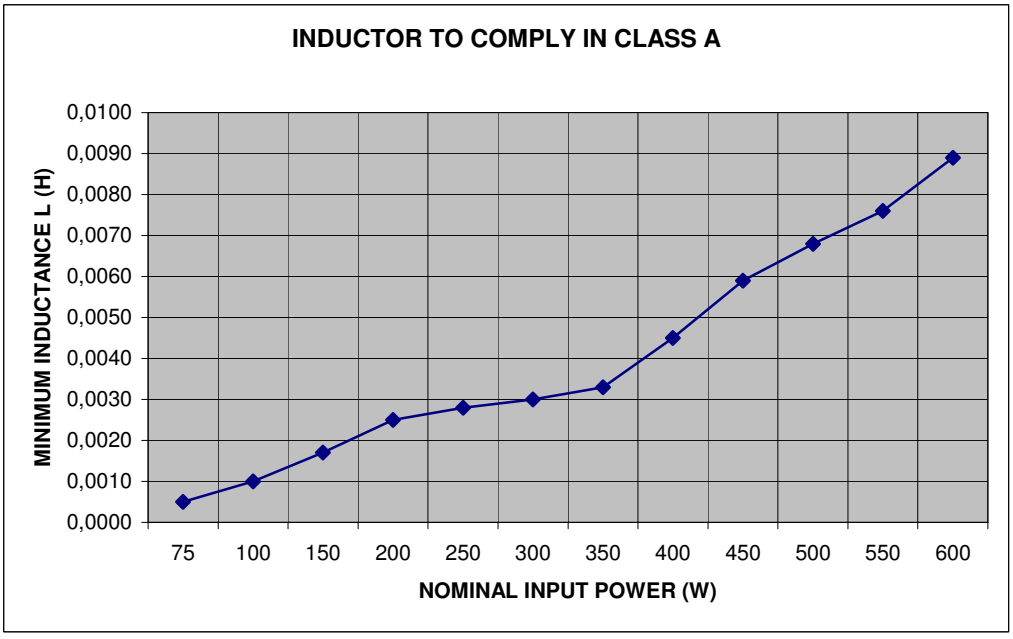


Figure 2.17 Minimum required inductance to comply with EN 61000- 3-2 Class A

It can be seen from Figures 2.17 and 2.18 that, the required filter inductance for Class A is much smaller than for Class D for the same power level. So the size of the inductor is very small for Class-A applications because the harmonic limits for Class A are bigger than Class D limits.

2.2.1.a Experimental Implementation of LC Filter Method

A 200-W single-phase rectifier with LC filter is simulated and verified experimentally with the parameters calculated above in order to meet the harmonic current standard specifications for Class A and Class D. The required minimum inductance values are calculated and the inductors are manufactured.

100W – Class D Application:

For Class D, the single-phase rectifier with LC filter is built with the following parameters given in Table 2.5.

Table 2.5 Parameters at the 100W Class-D application

Input Power	100 W
Input Voltage (V_{rms})	230 V
R Load	770 Ω
Filter inductance L	50 mH
Output Capacitor	330 μF

The minimum filter inductance is calculated as 42 mH but it is selected bigger than that value which is suitable for 100 W applications (Figure 2.17). The simulated current waveform and the harmonic contents are given in Figure 2.19. The experimental result for the current waveform is shown in Figure 2.20. The corresponding current harmonic limits and simulated and measured harmonic spectrum are shown in Figure 2.21.

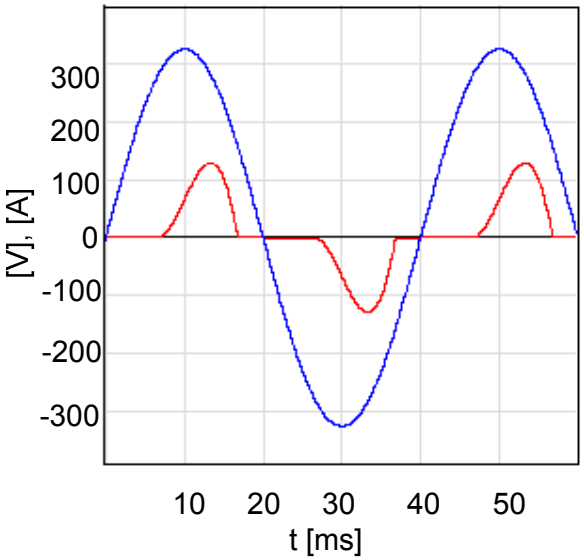


Figure 2.18 Simulation input current and voltage waveforms for Class D – 100W (Current Scale:100x).

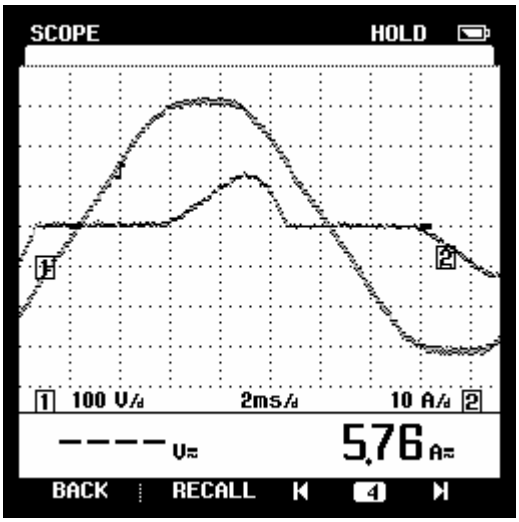


Figure 2.20 Measured input voltage and current for Class D – 100W (Scales: 100V/div, 1A/div).

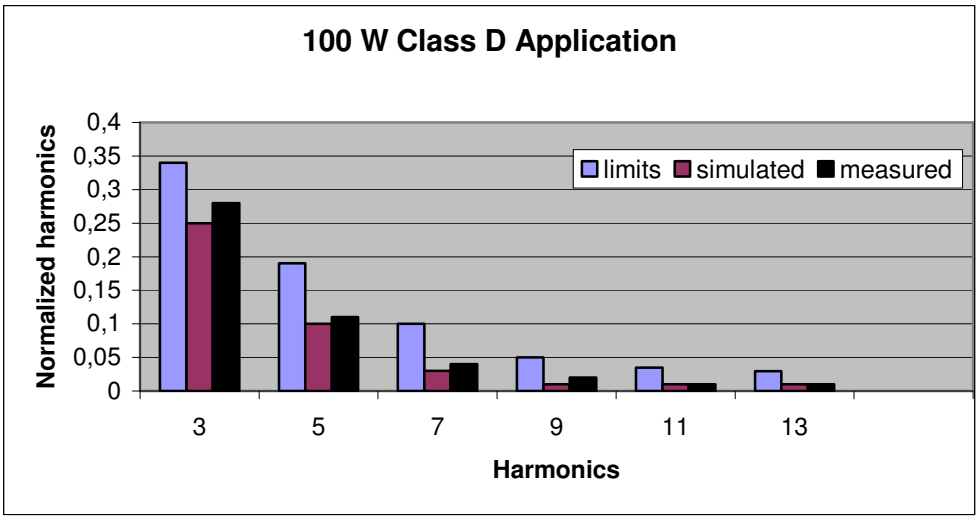


Figure 2.21 Harmonic spectrum for input current for Class D – 100W.

The measured data for the 100-W experimental system are given in Table 2.6.

Table 2.6 Measured results for 100W Class-D applications

V_{in}	I_{in}	P_{in}	V_o	I_o	P_o	THD	I_{fund}	I_{3th}	I_{5th}	PF
226Vrms	0.57A	100W	276Vdc	0.34A	90W	55%	0.45A	0.28A	0.11A	0.81

It is shown that, an LC filter with 50-mH inductance is capable of limiting currents in a single-phase rectifier system that can be classified in Class D 100-W application. The current THD is decreased and also PF is increased. But some voltage drop occurs on the filter inductance.

200W – Class D Application:

The same filter elements are used for 200-W applications with the following parameters given in Table 2.7.

Table 2.7 Parameters of 200W Class-D applications

Input Power	200 W
Input Voltage (V_{rms})	230 V
R load	380 Ω
Filter inductance	50 mH
Output Capacitor	330 µF

In fact, the minimum required inductance for 200-W Class-D application is 24 mH, but the same filter inductance is used for LC applications. The filter inductance is designed for the 200-W systems. The simulated current waveform is given in Figure 2.22. The experimental result for the current waveform is shown in Figure 2.23 and the harmonic contents are given in Figure 2.24.

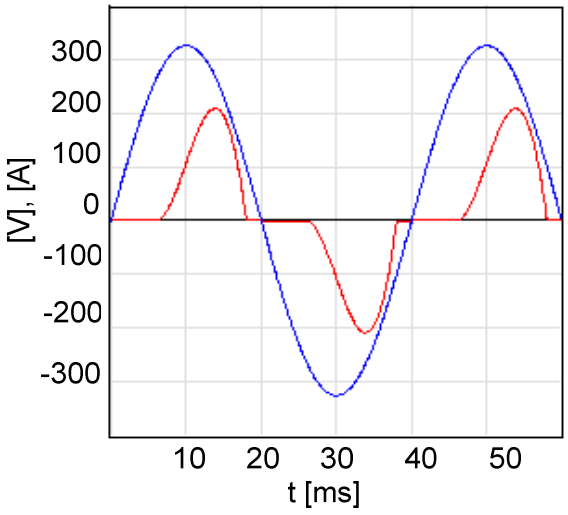


Figure 2.22 Simulation waveforms for Class D – 200W (Current Scale:100x).

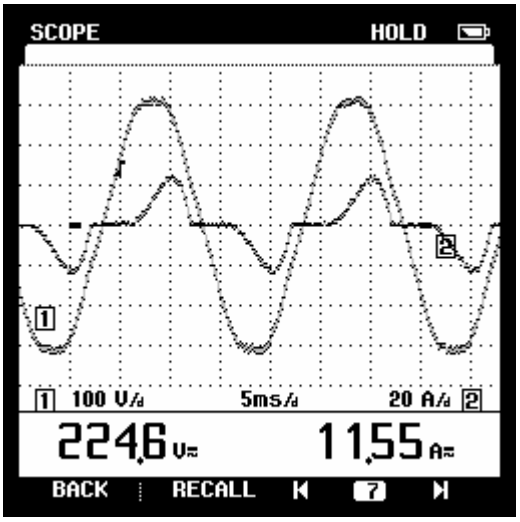


Figure 2.23 Measured input voltage and current for Class D – 200W

(Scales: 100V/div, 2A/div).

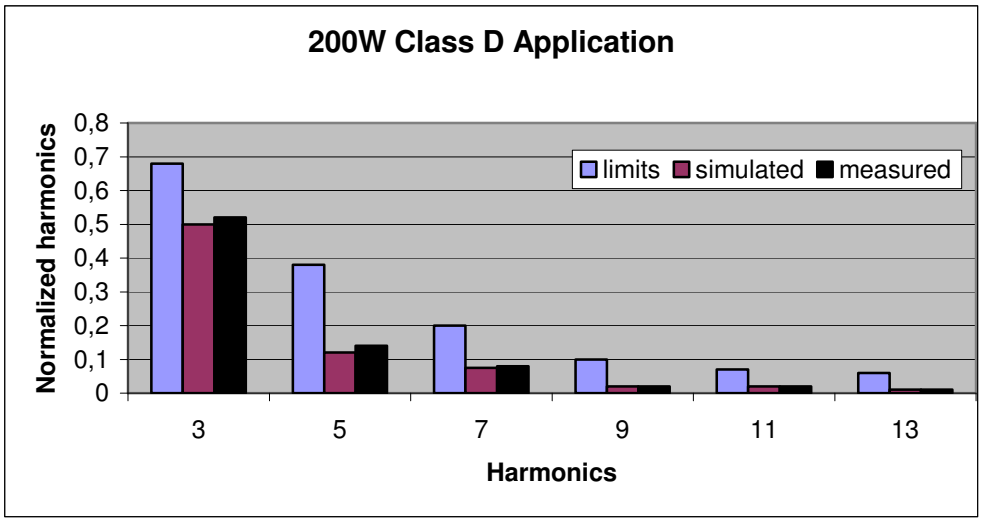


Figure 2.24 Harmonic spectrum for input current for Class D – 200W.

The measured results for the 200-W experimental system are given in Table 2.8.

Table 2.8 Measured results for 200W Class-D applications

V_{in}	I_{in}	P_{in}	V_o	I_o	P_o	THD	I_{fund}	I_{3th}	I_{5th}	PF
226Vrms	1.16A	200W	257Vdc	0.7A	190W	47%	1A	0.52A	0.14A	0.79

The minimum current harmonic limits are high for class-D applications, so the required minimum filter inductance values are high also. The size and the weights of these inductances increase when the operating power levels are increased. It is shown that it is easy to meet harmonic limits for class-D applications by an LC filter connected to bridge rectifier but the filter elements have higher weight and size.

100W – Class A Application:

The required minimum inductance is calculated from Figure 2.18. It is clear that the required filter inductance values for class-A applications are lower than those for class-D applications. However, the inductance values should increase if power level is increased. A 10-mH filter inductor is selected and the experiments are verified with the parameters in Table 2.9.

Table 2.9 Parameters for 200W Class-A applications

Input Power	100 W
Input Voltage (V_{rms})	230 V
R load	870 Ω
Filter inductance	10 mH
Output Capacitor	330 μF

The simulated current waveform is given in Figure 2.25. The experimental result for the current waveform is shown in Figure 2.26 and the harmonic contents are given in Figure 2.27.

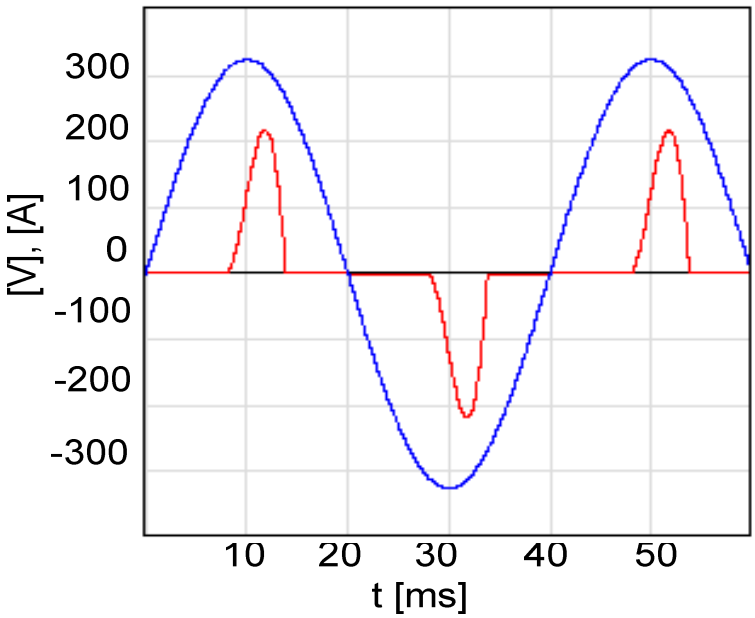


Figure 2.25 Simulation input current and voltage waveforms for Class A – 100W (Current Scale:100x).

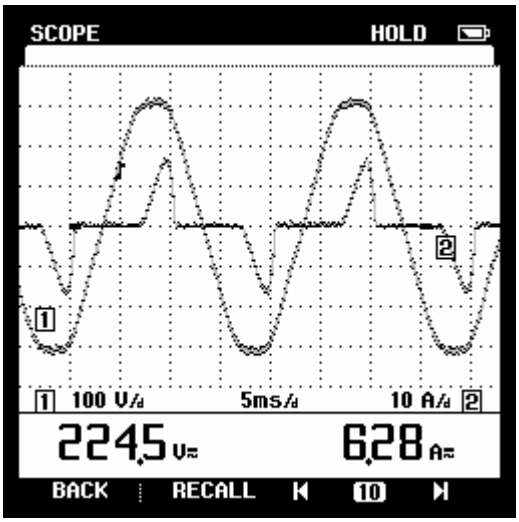


Figure 2.26 Measured input voltage and current for Class A – 100W (Scales: 100V/div, 1A/div).

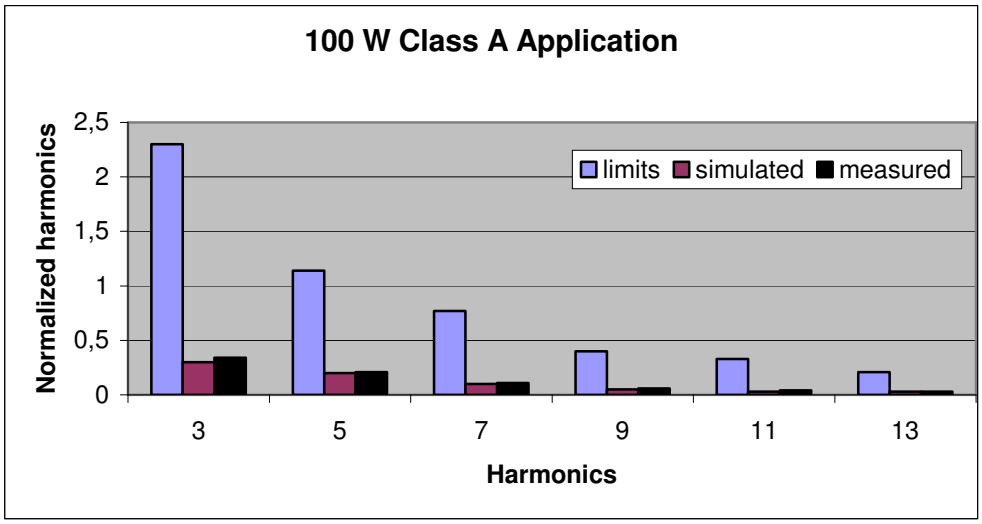


Figure 2.27 Harmonic spectrum for input current for Class A – 100W.

The measured data for the 100-W experimental system are given in Table 2.10.

Table 2.10 Measured results for 100W Class-A application

V_{in}	I_{in}	P_{in}	V_o	I_o	P_o	THD	I_{fund}	I_{3th}	I_{5th}	PF
224Vrms	0.63A	100W	295Vdc	0.3A	88W	70%	0.44A	0.34A	0.21A	0.69

200W – Class A Application:

The same filter elements are used for 200-W Class-A applications with the following parameters given in Table 2.11.

Table 2.11 Parameters for 100W Class-A application

Input Power	200 W
Input Voltage (V_{rms})	230 V
R load	450 Ω
Filter inductance	10 mH
Output Capacitor	330 µF

The simulated current waveform is given in Figure 2.28. The experimental result for the current waveform is shown in Figure 2.29 and the harmonic contents are given in Figure 2.30.

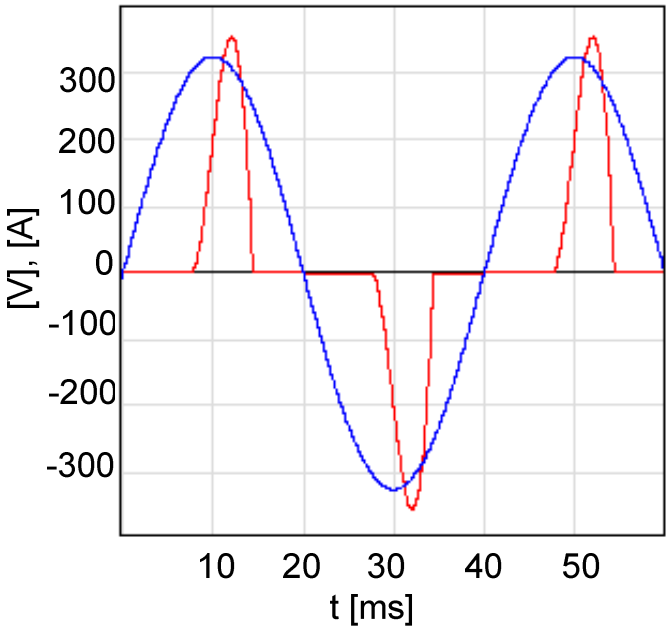


Figure 2.28 Simulation input current and voltage waveform for Class A – 200W (Current Scale:100x).

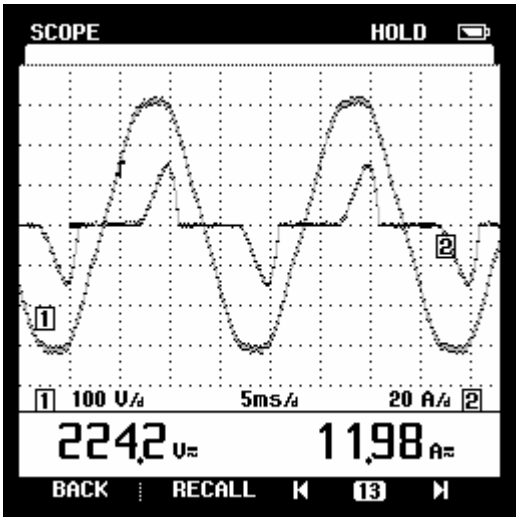


Figure 2.29 Measured input voltage and current for Class A – 200W (Scales: 100V/div, 2A/div).

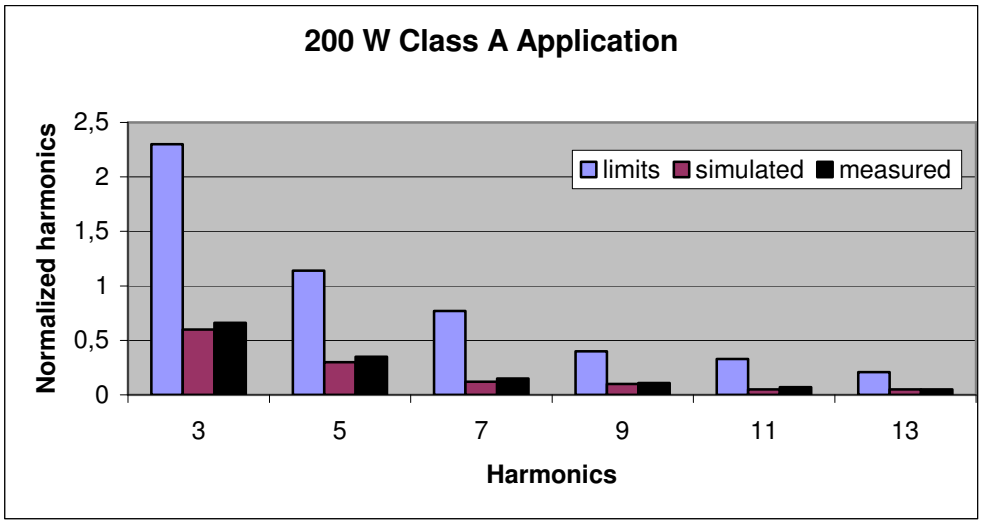


Figure 2.30 Harmonic spectrum for input current for Class A – 200W.

The measured data for the 200-W experimental system are given in Table 2.12.

Table 2.12 Measured results for 200W Class-A applications.

V_{in}	I_{in}	P_{in}	V_o	I_o	P_o	THD	I_{fund}	I_{3th}	I_{5th}	PF
224Vrms	1.14A	200W	290Vdc	0.65A	188W	66%	0.88A	0.66A	0.35A	0.79

It is shown theoretically and experimentally that, single-phase full bridge diode rectifier with an LC filter can be used complying with the EN 61000-3-2 standard. The LC passive filter method is suitable for low power because the required inductance size is very large for higher power levels. For Class-A applications, the required minimum inductance values are smaller and this brings the smaller size of filter inductor. The improved LC filter solutions are given in references [22], [23], [24], [25] and [26].

2.2.2 Series Connected Parallel Resonant Filter

Power factor improvement via reducing input current harmonics for a single-phase rectifier with a capacitive output filter can alternatively be done by using resonant filters. There are different resonant network based passive solutions. Two main resonant solutions are:

- Series connected series resonant band pass filter tuned at line frequency
- Series connected parallel resonant band stop filter tuned at third harmonic [27], [28]

The resonant filters are connected between AC line and diode rectifier. Generally, these systems have larger reactive elements. In this section, the series connected parallel resonant filter shown in Figure 2.31 [27] is investigated and verified experimentally, since it requires lower values of reactive elements compared to other solutions.

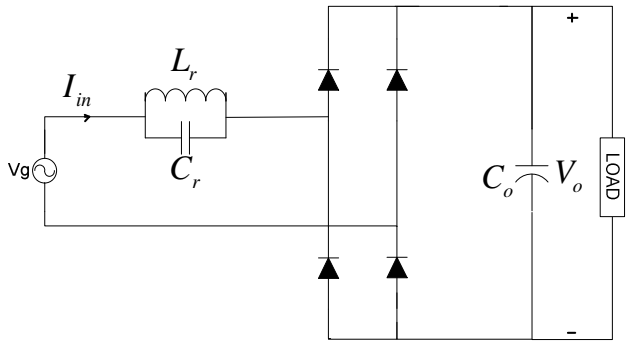


Figure 2.31 Series connected parallel resonant filter.

A single-phase full bridge rectifier with capacitive filter draws higher harmonic currents from line. The most significant harmonic is the third harmonic. If this one is reduced or cancelled, the rectifier will have higher power factor due to lower input RMS current and lower THD. The series connected parallel resonant filter is tuned to 3rd harmonic and, generally, called as a third harmonic filter.

The proposed filter in Figure 2.31 has an input LC parallel resonant tank tuned at 3rd harmonic. The inductance and capacitance values of the resonant tank are selected to behave as an infinite (theoretically) impedance to the third harmonic input current component. So the system will eliminate the third harmonic content of the input current. This condition brings lower input rms current value with lower THD. So the system will have higher power factor and efficiency.

The *n*th order equivalent impedance of the resonant tank can be defined by:

$$Z_n = \frac{nX_{Lr} * \frac{X_{Cr}}{n}}{jnX_{Lr} - j\frac{X_{Cr}}{n}} \tag{2.14}$$

where X_{Lr}, is the impedance of the input resonant inductor L_r at fundamental frequency, X_{Cr}, is the impedance of the input resonant capacitor C_r at fundamental frequency. The third harmonic impedance from (2.14) becomes infinity (theoretically) when;

$$3X_{Lr} = \frac{X_{Cr}}{3} \tag{2.15}$$

or

$$L_r = \frac{1}{9\omega^2 C_r} \tag{2.16}$$

where $\omega = 2\pi f_o$ [27].

The single-phase rectifier is assumed lossless with no voltage drop in the diodes. The output voltage is assumed ripple free with large output capacitor. The line voltage is assumed sinusoidal and the load is assumed to be a constant power load. The values

of the reactive elements in the resonant filters are selected for higher power factor defined in the section 2.2.1.

2.2.2.a Experimental Evaluation of Series Connected Parallel Resonant Filter

The proposed method in Figure 2.31 is simulated with the following parameters given in Table 2.13. The simulation results for the input current waveform are shown in Figure 2.32.

Table 2.13 Simulation parameters of series connected parallel resonant filter

Filter Inductance L_r	140.7 mH
Filter Capacitance C_r	8 µF
Input Voltage (V_{rms})	230 V
Input Power	150 W
R load	530 Ω
Output Capacitance Co	330 µF

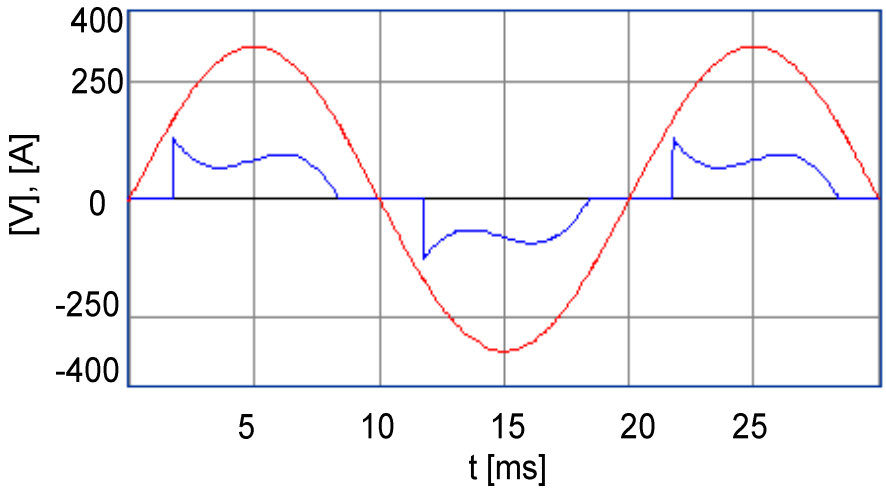


Figure 2.32 Input current and voltage waveform for series connected parallel resonant filter (Current Scale:100x).

The system is implemented in laboratory with the same parameters used in the simulations. The corresponding input voltage and current waveforms are measured. The measured waveforms are shown in Figure 2.33. The harmonic spectrum of the input current is measured and compared with the limit of the class-A and class-D applications. Figure 2.34 shows the harmonic spectrum of the input current with harmonic standard limits.

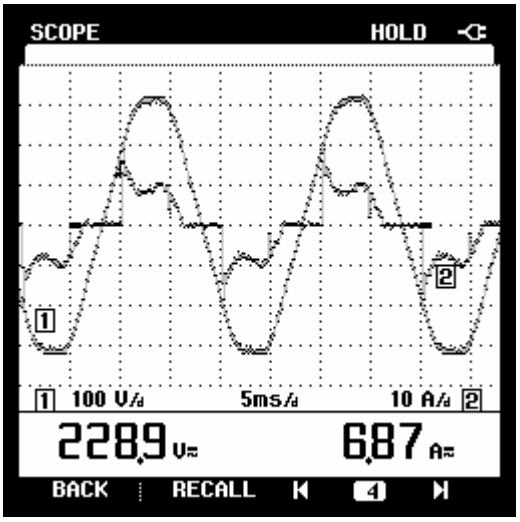


Figure 2.33 Measured current of series connected parallel resonant filter for 150W system (Scales: 100V/div, 1A/div).

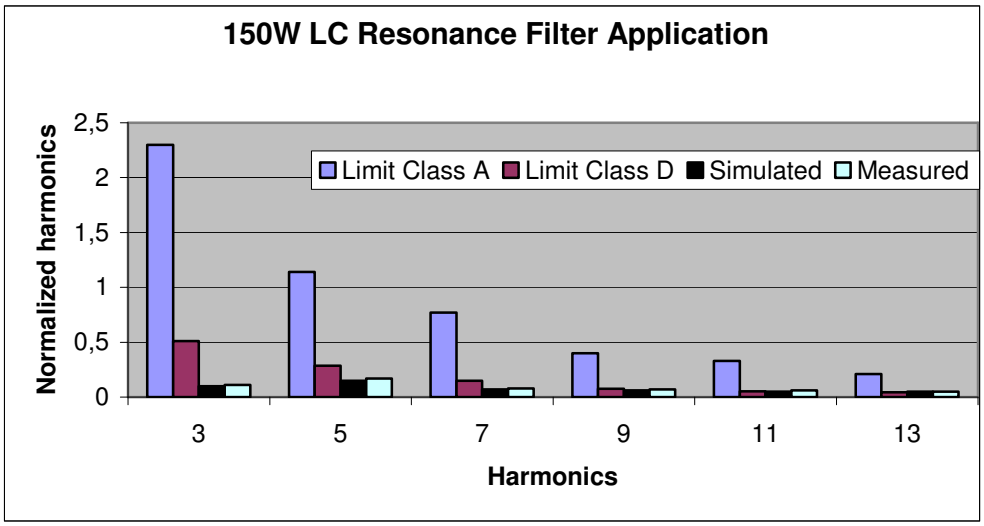


Figure 2.34 Input current harmonics for series connected parallel resonant filter

Table 2.14 Measured data for 150W series connected parallel resonant filter

V_{in}	I_{in}	P_{in}	V_o	I_o	P_o	THD	I_{fund}	I_{3th}	I_{5th}	PF
229Vrms	0.69A	150W	272Vdc	0.5A	136W	40%	0.62A	0.11A	0.17A	0.66

It can be seen from Table 2.14 that, the power factor can be improved by reducing the third harmonic component of the line current. However the filter has limited capability to reduce the other harmonics. So the compliance for the standard EN 61000-3-2 is not easy to meet by this method. On the other hand, higher order harmonics can be amplified because of the parallel resonance at different frequencies.

2.2.3 Variable Inductance LC Filter Method

The LC filter method defined in section 2.2.1 is load dependent. If the rectifier is supposed to operate at various output power levels, the output LC filter should be designed for each power level or a large filter inductance should be used which is suitable for all power levels. In the case of both situations, the inductance will have higher size. For example, the required minimum inductance for a Class-D device is given in Figure 2.35.

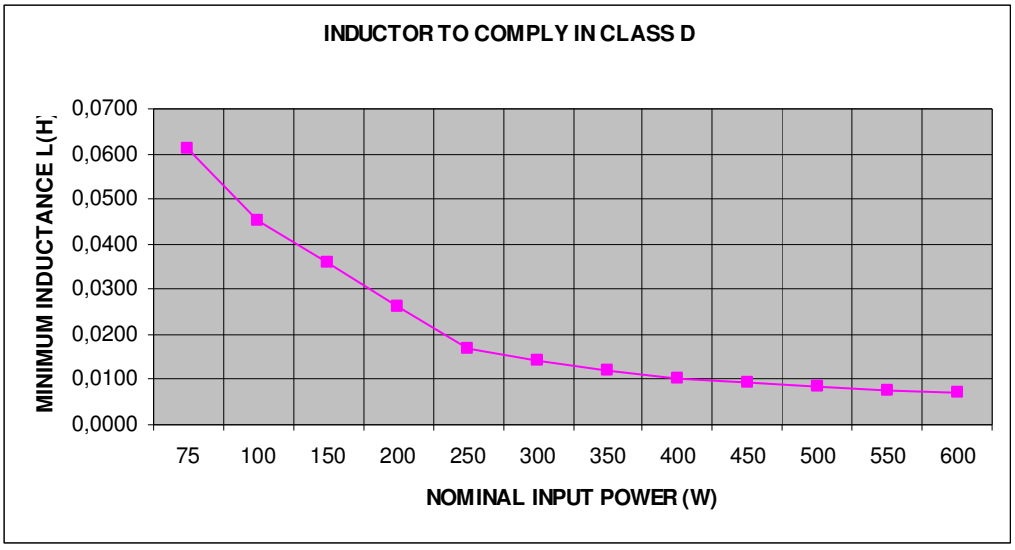


Figure 2.35 Required minimum inductance for Class D.

It can be seen from Figure 2.35 that, the inductance should be selected with higher values to operate in the range of 75-600 W. For example a 68-mH output inductor is enough for all power levels. However the size of the inductor is directly related to the energy stored on it. The stored energy for 600 W is much bigger than the stored energy in the 75 W due to higher current in it. The higher size of the inductor is impractical. So the traditional LC filter method is not suitable for variable load applications. The system needs a reduced inductance while the current is increasing on it. The solution for this problem is to use a variable inductance filter proposed at [29]. In this section, the variable inductance method for passive power factor correction in compliance with the EN61000-3-2 standard is investigated.

This filter method can be achieved by building inductor with different discrete air gaps that saturate under different current values that a load dependent filter provides. The proposed variable inductance filter has lower volume and weight, approximately half the size of the conventional filter. A 70 mH inductance with 600 W (8 A peak) rating is needed for conventional approach in the 75-600 W range. But if a variable inductance is used, a 70 mH inductance with 75 W is suitable for the same range.

The variable inductance can be evaluated by changing the geometrical shape of the magnetic core of the inductor. An inductor with a fixed air-gap has constant inductance that operates under saturation region. If the current on the inductance is increased, the inductor now operates in saturation region and has higher reluctance. The increased reluctance of the core reduces overall inductance.

Variable inductance can be obtained by providing different reluctance paths. This can be done by stepped air gaps and is known as swinging inductance. The core with different stepped air gaps has series reluctances. When the current on the winding is increased, the reluctance path due to smaller air-gap saturates first and this reduces the overall inductance. The optimum variable inductance can be obtained by increasing the number of stepped air gaps in the core. This can be done by a sloped air gap that operates on the same principle as the swinging inductance. The sloped air gap inductance provides accurate rate of change of the inductance according to current change in the winding.

2.2.3.a Saturated Core Inductors

Variable inductance can be obtained in a constant air-gap inductor by operating in the saturation region. If the current passing on the inductor has higher value causing to exceed the maximum magnetic flux density, the inductor operates in the saturation region. In the saturation region, the magnetic core has lower permeability causing the higher reactance. So the total inductance will reduce. If the current increases in the saturation region, the total inductance will reduce according to the current rise. This can be explained by core characteristics. The relative permeability may be described as a function of the magnetic field strength.

$$\mu_r = \frac{H_m}{H_c + H_o} \tag{2.17}$$

H_c is the value of the magnetic field intensity where μ_r is calculated. H_c is related to the coil's magnetization force (NI) by Ampere's Law. Figure 2.36 shows the relation of the relative permeability versus magnetization force according to equation 2.19 for different core materials taken from Waasner Company.

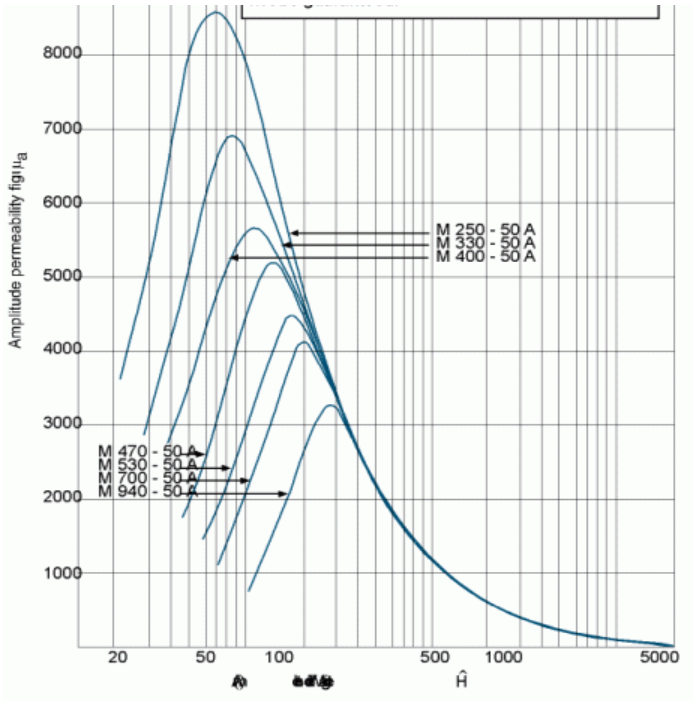


Figure 2.36 Relative permeability versus magnetization force.

A constant air-gap inductance is shown in Figure 2.37.

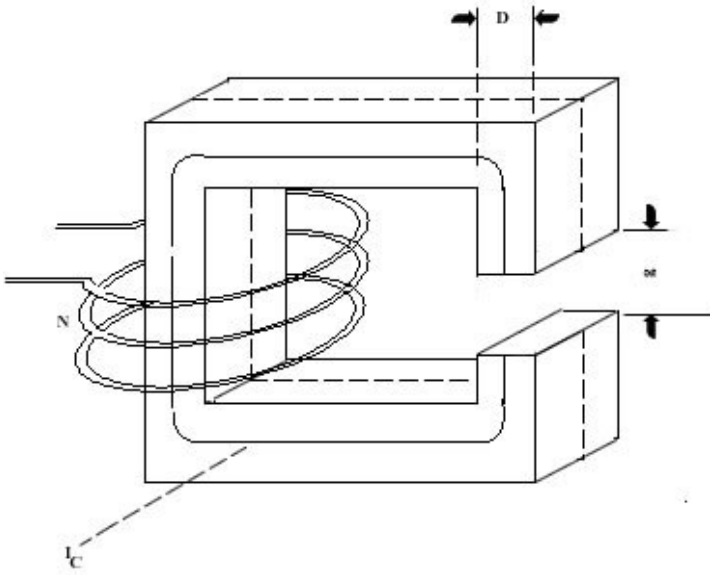


Figure 2.37 Constant air-gap inductor.

The inductance of the constant air-gap inductor by can be expressed as:

$$L = \frac{N^2}{R_c + R_g} = \frac{\mu_0 . N^2 . A_g}{g + \frac{l_c}{\mu_r}} \tag{2.18}$$

The inductor has constant inductance before the saturation region. The relative permeability μ_r of the core can then be ignored because of the very large values. If the inductor operates in the saturation region, the relative permeability μ_r of the core will be lower. In this region, the total inductance will reduce. The variation of the inductance in the saturation region can be explained by using Ampere's law. The magnetic circuit of the constant air-gap inductor has the following equations.

$$N.I = H_c . l_c + \frac{B_g . g}{\mu_o} \tag{2.19}$$

$$B_g = \mu_r.\mu_0.H_c \tag{2.20}$$

$$\mu_r = \frac{H_m}{H_c + H_o} \tag{2.21}$$

These equations can be rearranged as:

$$H_0.g.\mu_r^{\,2} + (N.I + H_0.l_c - H_m.g).\mu_r - H_m.l_c = 0 \tag{2.22}$$

If the second order equation in (2.22) is solved by a change of basis rule regards to μ_r , the variation of the inductance due to relative permeability in the saturation region can be seen. The total inductance when the current changes can be defined by this method. In Figure 2.38, an example of the variable inductance is shown.

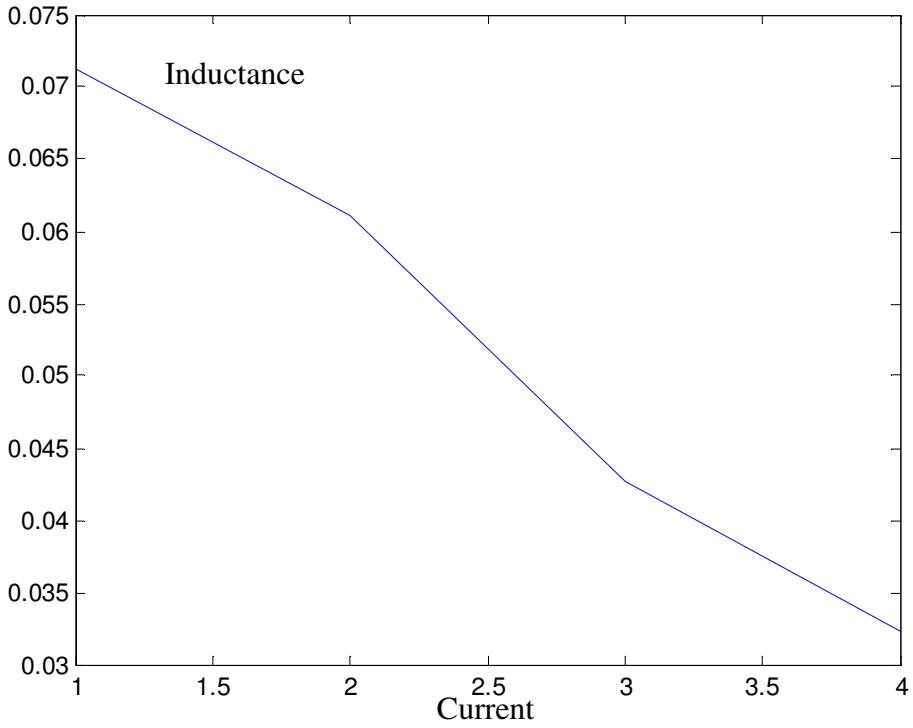


Figure 2.38 Constant gap variable inductor.

It can be seen from Figure 2.38 that, the L versus I curve shows the same characteristic with the required minimum inductance versus power curve in Figure 2.35. The inductor has constant inductance until current reaches the saturation value that is about 1.2 A. The relative permeability (μ_r) determines the shape of the inductance in the saturation range operation. The L-I curve may be accurately controlled by introducing a stepped air-gap, where one or more gaps are operating under saturation.

2.2.3.b Step-Gap Variable Inductor

The characteristic L versus I curve can be modified or controlled effectively by adding more air gaps. This type of inductor is called as swinging inductor. The swinging inductor has a two-stepped air gap as shown in Figure 2.39.

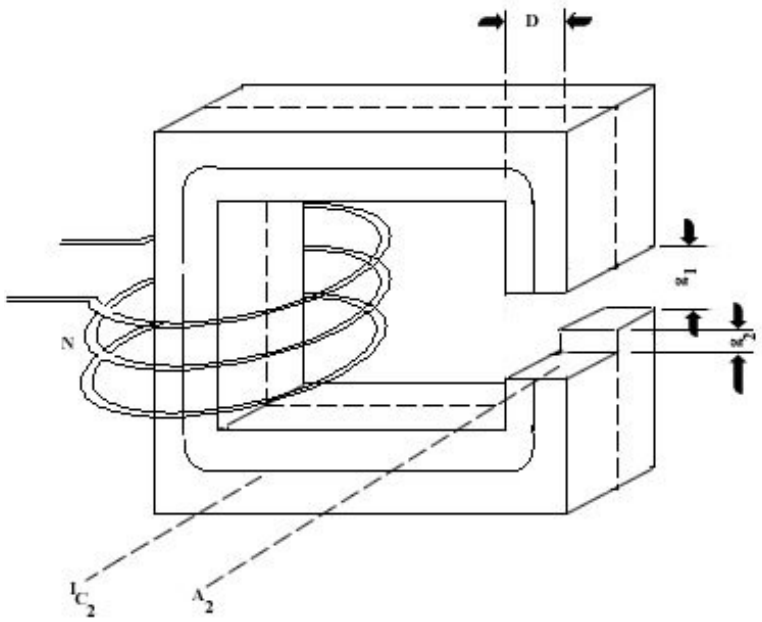


Figure 2.39 Swinging inductor.

The total inductance is assumed as the serial combination of the two gapped inductances. We can write the inductance equation as:

$$L = \frac{N^2}{R_{g1}} + \frac{N^2}{R_{g2}} \tag{2.23}$$

As the current increases, the core with the smallest gap saturates first. The inductance value is defined by the smallest gap. When the current has enough value to saturate the smallest gap reluctance path, the new inductance value is defined by the bigger gap. The theoretical change of the inductance with the current in the swinging inductance is given in Figure 2.40.

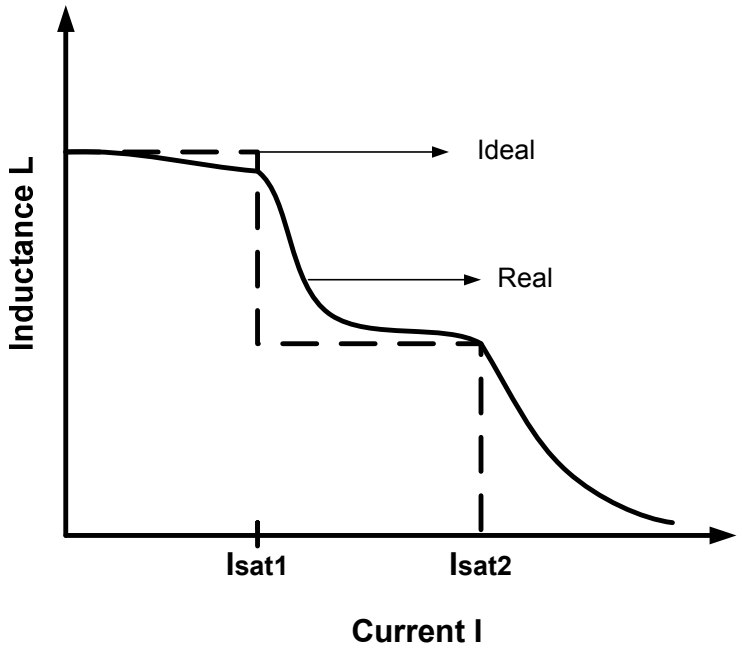


Figure 2.40 Swinging inductance variations.

In the swinging inductance, the lower gapped section of the inductance first saturates then the inductance will have a new, lower value. Sharp changes in the inductance and current values can occur when the first gap side saturates. This is the disadvantage of this type of inductance. This disadvantage can be altered by infinite number of discrete gaps or a sloped air gap as described in the next section.

2.2.3.c Sloped Air-Gap Inductor

Swinging inductance can be improved by making the air gap variable. So we can eliminate the drawbacks of the sharp changes of the inductance in the swinging inductance. A sloped air-gap inductor is shown in Figure 2.41.

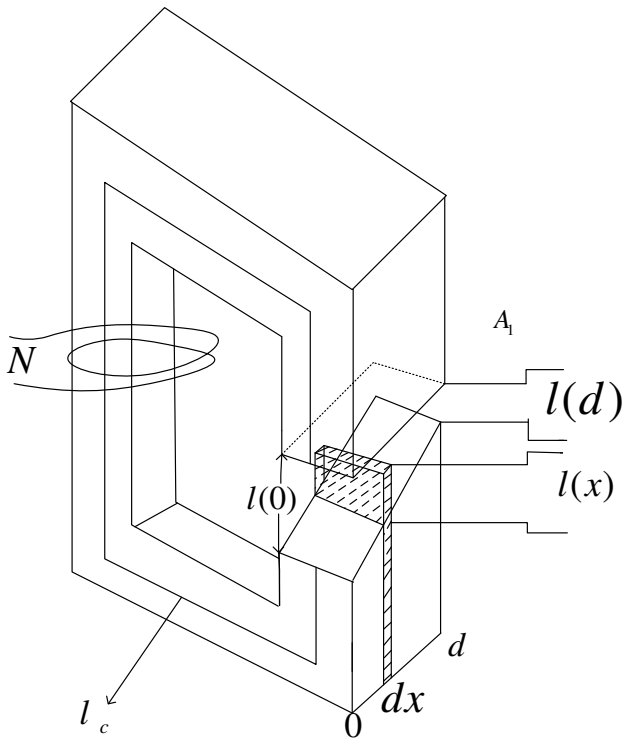


Figure 2.41 Sloped air-gap inductance.

The air gap has the following equation according to Figure 2.41.

$$g(x) = G - \frac{(G-g)x}{d} \tag{2.24}$$

The inductance can be evaluated by the flux linkage for a small area dx in the core as shown in the figure. Then

$$d\lambda = \frac{N^2 I}{dR_g} = \frac{\mu_0 N^2 ID}{g(x)} dx \tag{2.25}$$

where g(x) is the length of the air gap at x as given in Equation 2.24.

Total flux linkage can be derived by the integration of the equation 2.25 between x = 0 and x.

$$\lambda = \int_0^x \frac{\mu_0 N^2 ID}{g(x)} dx \tag{2.26}$$

The inductance is equal to the ratio of the total flux linkage to the current. Then

$$L(x) = \frac{\lambda}{I} = \frac{\mu_0 N^2 dD}{G-g} \ln\left(\frac{G}{g(x)}\right) \tag{2.27}$$

The inductance equation (2.27) gives the change of the inductance due to air-gap geometry. When the entire gap is included the total inductance before saturation (L_d) can be found as:

$$L_d = \frac{\mu_0 N^2 dD}{G-g} \ln\left(\frac{G}{g}\right) \tag{2.28}$$

When the current on the inductor exceeds the saturation current value (I_{sat}), the core begins to saturate with the smallest air gap x = d. By invoking the Ampere's law when the first saturation occurs the saturation flux density and saturation current relationship can be obtained as:

$$I_{sat(x)} = \frac{B_{sat}}{\mu_0 N} g(x) \tag{2.29}$$

The core saturates between x and d due to the value of the saturation current

value $I_{sat(x)}$. The current value instead of saturation current value can be utilized by using $I = I_{sat(x)}$ and the inductance equation as a function of the current for $I > I_{sat}$ can be rewritten as:

$$L(I) = \frac{\mu_0 N^2 dD}{G-g} \ln\left(\frac{GB_{sat}}{\mu_0 NI}\right) \tag{2.30}$$

The inductance before the saturation can be rewritten as:

$$L_d = \frac{\mu_0 N^2 dD}{G-g} \ln\left(\frac{GB_{sat}}{\mu_0 NI_{sat}}\right) \tag{2.31}$$

Then equations (2.30) and (2.31) can be combined to obtain:

$$L(I) = L_d \left(1 - \frac{\ln(I/I_{sat})}{\ln(G/g)}\right) \tag{2.32}$$

The change of the inductance as a function of the current is given in Figure 2.42.

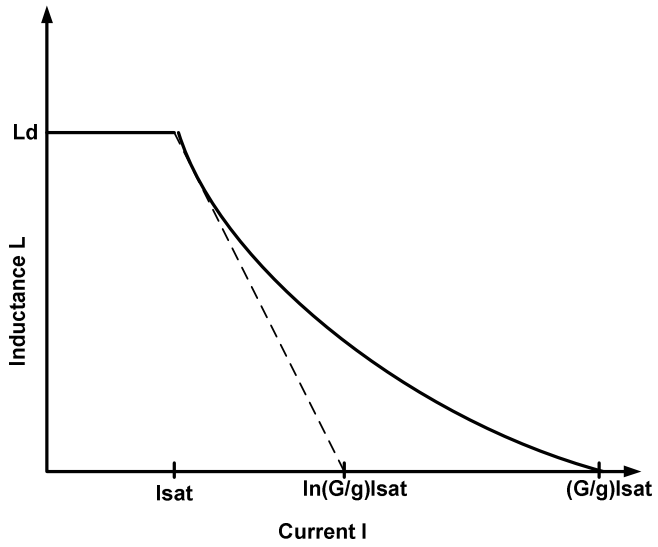


Figure 2.42 Inductance variations of sloped air-gap inductor.

The sloped gap inductance has ideal characteristics for variable load applications. The change of the inductance versus current is more desirable than in other solutions.

2.2.3.d Design of Sloped Gap Inductance

While designing a variable inductance filter, the operating power level and the required minimum inductance filter value should be considered.

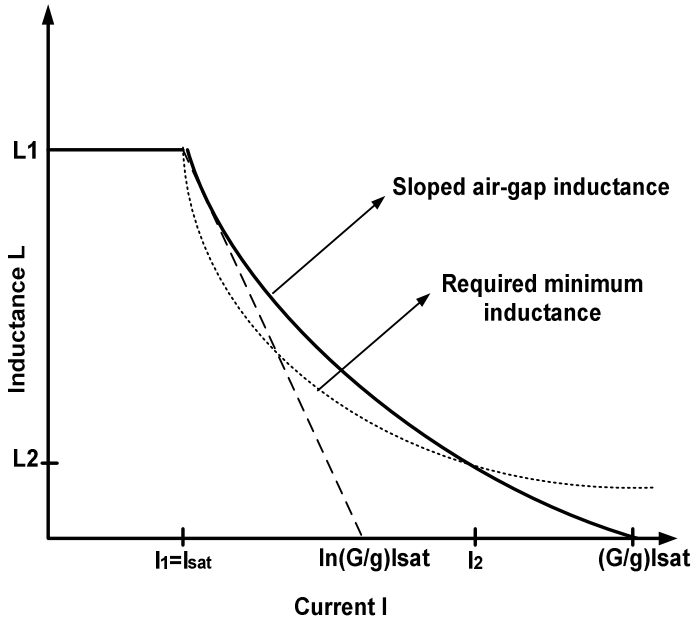


Figure 2.43 Inductance variations of sloped air-gap inductor.

The inductance L_1 is the required inductance for the minimum power level due to the current $I_1 = I_{sat}$. This inductance value is equal to the inductance before saturation $L_1 = L_d$ and defined in the equation 2.29. The inductance L_2 is the required inductance for the minimum power level due to the current I_2. By using the minimum and maximum current and inductance values, the slope of the air gap can be evaluated using Equation 2.30.

$$\ln(G/g) = \frac{\ln(I_2/I_1)}{1 - L_2/L_1} \tag{2.33}$$

The sloped of air gap is defined by the required inductances and the currents due to the operating power levels. The turns ratio N and the required air gap dimensions can be obtained by using Equations (2.28) and (2.29).

$$N = \frac{I_1 L_1 (\frac{G}{g} - 1)}{B_{sat} dD \ln(\frac{G}{g})} \tag{2.34}$$

$$g = \frac{\mu_0 I_1 N}{B_{sat}} \tag{2.35}$$

$$G = g e^{\ln \frac{G}{g}} \tag{2.36}$$

The equations above can be applied to the selected core. While selecting the core, saturation flux density and current carrying capability should be considered. The coil should carry the maximum operating current but the core should saturate at the saturation current. Generally an EI type silicon alloy magnetic core is used for this application. An example of EI type sloped air-gap inductor is shown in Figure 2.44.

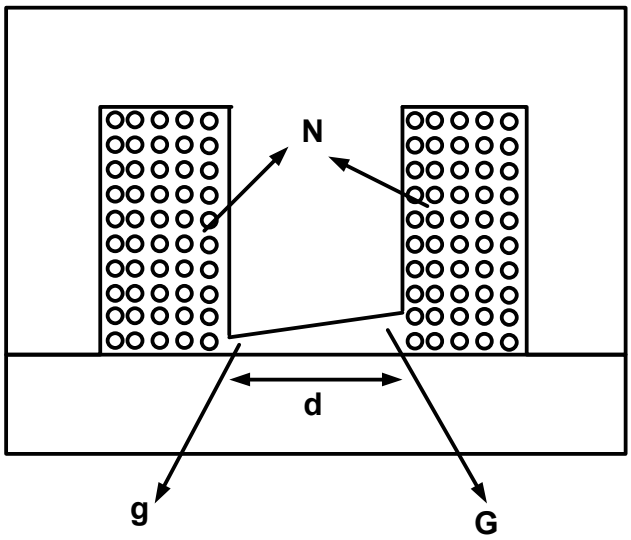


Figure 2.44 Construction of sloped air-gap with EI silicon steel.

The detailed drawing for sloped air-gap inductor is shown in Figure 2.45.

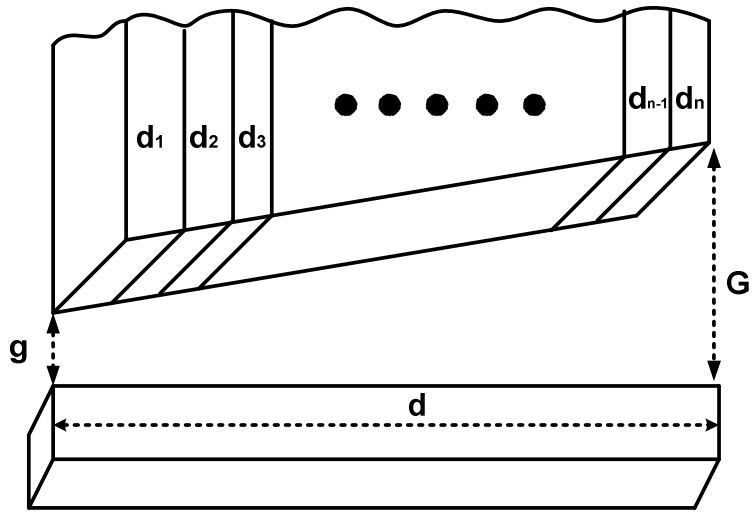


Figure 2.45 Detailed view of the sloped air-gap.

The magnetic circuit of the variable inductor can be drawn as shown in Figure 2.46.

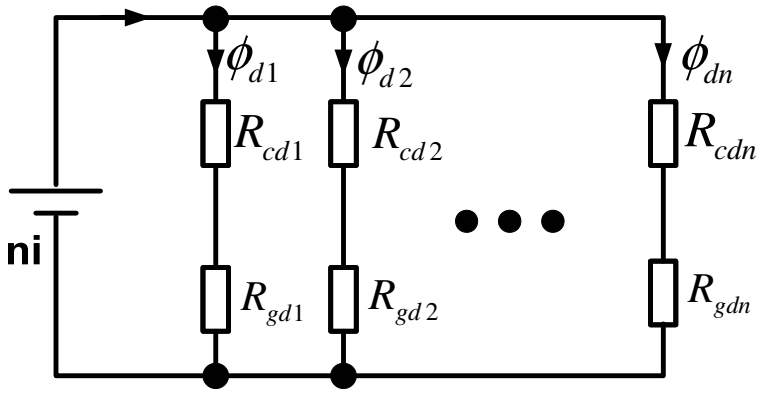


Figure 2.46 Magnetic circuit of the sloped air-gap inductance.

2.2.3.e Experimental Evaluation of Variable Inductance LC Filter Method

A single-phase diode rectifier with variable inductance filter is simulated and verified experimentally. A 200-W system is designed in compliance with class-D standards. The circuit parameters are given in table 2.15.

Table 2.15 Simulation parameters for 200W variable inductance application

Input Power	200 W
Input Voltage (V_{rms})	230 V
R load	380 Ω
Filter inductance	80 mH
Output Capacitor	330 µF

The sloped air-gap inductance is modeled in the SIMPLORER simulation tool by using a nonlinear inductance model. Used inductor model and corresponding inductance are shown in Figure 2.47.

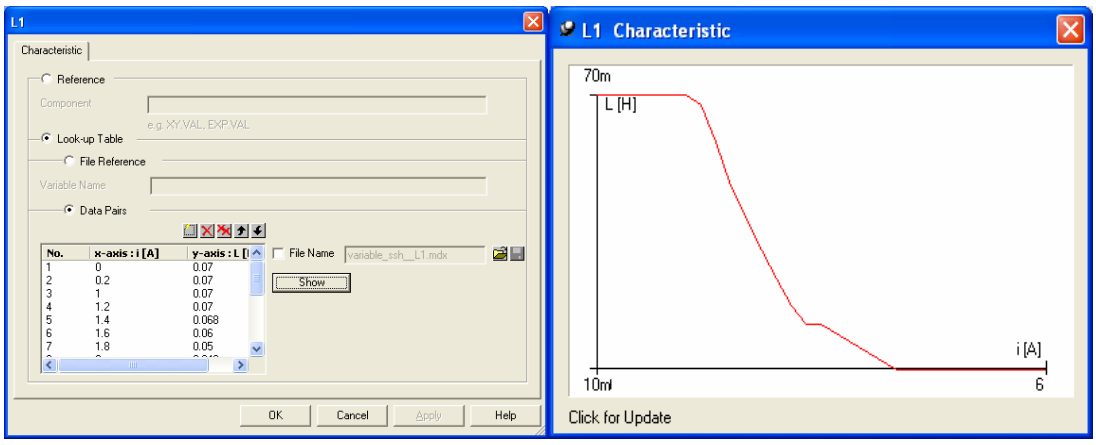


Figure 2.47 Variable inductance model used in simulations.

The simulation results for input current and input voltage of sloped air-gap inductance are shown in Figure 2.48.

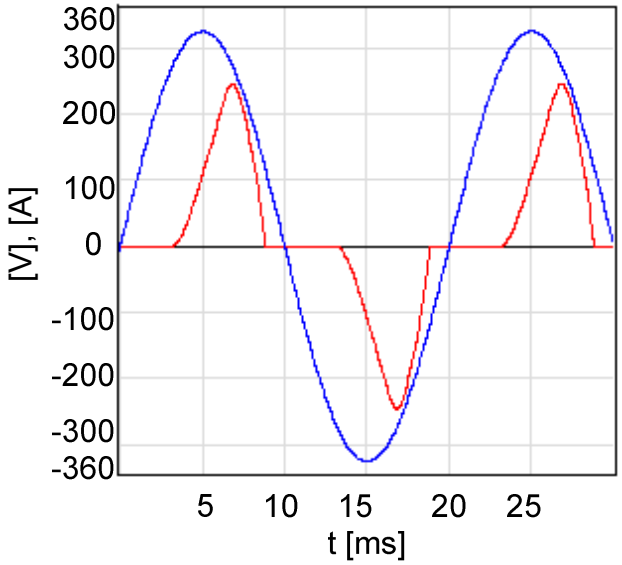


Figure 2.48 Simulation results for input voltage and current

(Current Scale: 100x).

The circuit is implemented experimentally with a sloped air-gap inductance. Sloped air-gap inductance is designed according to section 2.2.3.a. The parameters of inductance are given in Table 2.16.

Table 2.16 Design parameters of variable inductance

Inductance Before Saturation	80 mH
Rated current	3 A
I_{sat1}	1.2A
I_{sat2}	2A
B_{sat}	1.4 Tesla
Core Type	EI Silicon Steel
Number of Turns, N	280
Minimum air-gap, g	0.2mm
Maximum air-gap,G	1.2mm

The measured current and voltage waveforms are shown in Figure 2.49.

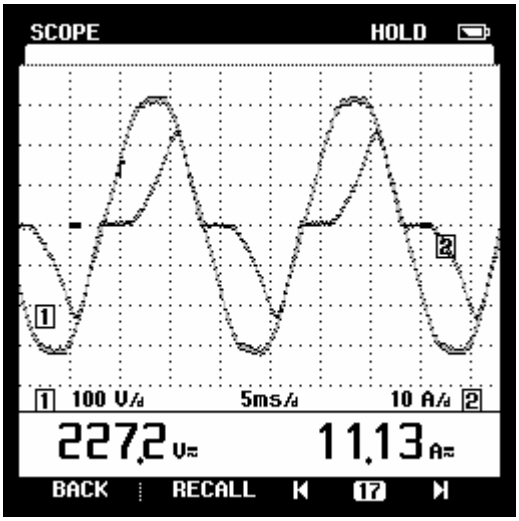


Figure 2.49 Experimental results for input voltage and current (Scales: 100V/div, 1A/div).

The simulated and measured current harmonics are evaluated and compared with the harmonic standards for 200-W Class-D application. The result is shown in Figure 2.50.

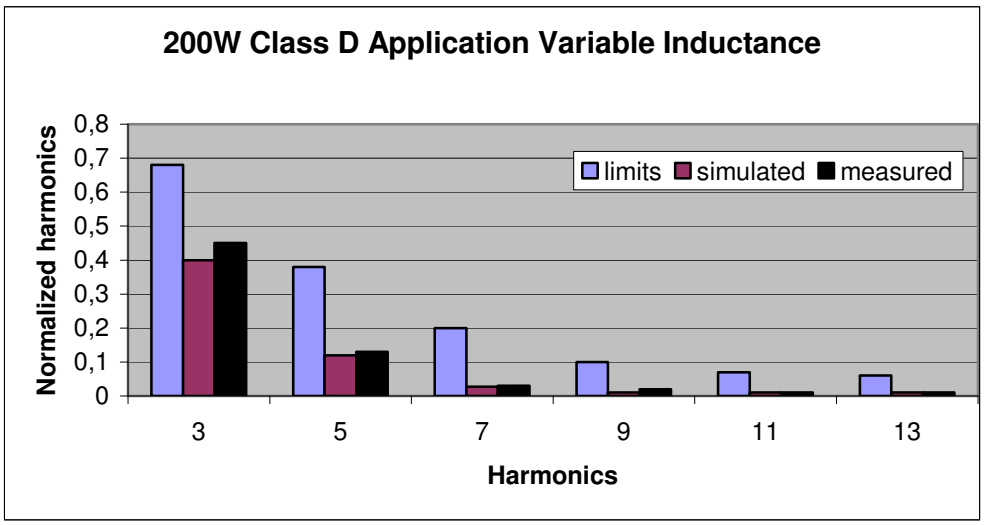


Figure 2.50 Input current harmonics for 200W Class-D application.

The measured values for the variable inductance filter for the single-phase rectifier is given in Table 2.17.

Table 2.17 Measured results for 200W SAG filter application

V_{in}	I_{in}	P_{in}	V_o	I_o	P_o	THD	I_{fund}	I_{3th}	I_{5th}	PF
228Vrms	1.11A	200W	262Vdc	0.7A	183W	42%	0.98A	0.45A	0.13A	0.8

It is seen that the sloped air-gap inductance shows the best performance in the mentioned passive methods. The size of the inductance is lower than in the other cases. This method has better PF and lower input current THD.

2.3 Limitations of Passive PFC Circuits

The simplicity, reliability, insensitivity to noise and surges and the no generation of any high-frequency EMI offered by passive power factor circuits are of significant usefulness. However, the bulky size of these filters, their poor dynamic response, complexity and high cost, the lack of voltage regulation and their sensitivity to line-frequency, limits their use to below 200-W applications. Moreover, even though line current harmonics are reduced, the fundamental component may show an excessive phase shift resulting in reduction in power factor.

CHAPTER 3

AVERAGE CURRENT CONTROL OF PFC

3.1 Description of Average Current Mode Control of PFC

This chapter deals with the average current mode control of a single-phase boost power factor correction circuit [31]. A detailed theoretical analysis of the average current mode control of PFC will be reviewed and supported by hardware implementation. The power factor correction IC, UCC3818, will be used to implement this strategy and design and functional description of the circuit will be explained.

The block diagram of the PFC circuit is given in Figure 3.1. The circuit consists of a single-phase rectifier with a cascaded boost converter that provides active wave shaping of the input current and regulation of the output voltage. Active power factor correction is achieved by the power switch duty cycle. The switching frequency of the converter is higher than line frequency such as 100 kHz for 50-Hz power system. When the switch is turned on, the boost inductor stores energy from input. At the same time, the output rectifier diode is reverse biased and the load is supplied by the output capacitor. When the switch is turned off, the output capacitor and the load are supplied by the input over the boost inductance.

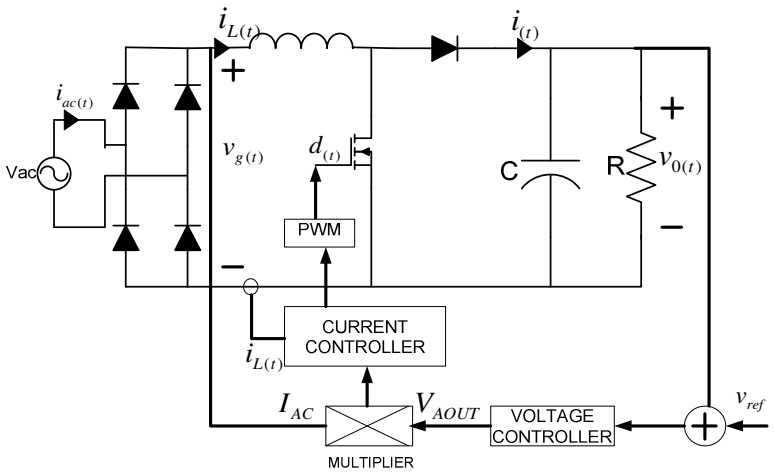


Figure 3.1 Average current mode control of PFC.

The average current controlled PFC system has two control loops. The system has fast inner current loop that enables the input current to follow the reference current. The reference current is multiplication of the reference shape and reference amplitude. The reference current gets the sinusoidal shape of the input voltage. The amplitude of the reference current is defined by the outer voltage loop. The system has a low bandwidth outer voltage loop which programs the required input current reference magnitude according to the power consumption of the load. This function is done by using an output voltage regulator control circuit.

The inner current loop operates in average current mode that controls the average input current. The input current $I_{L(t)}$ is compared with I_{ref} per switching cycle and passed through an error amplifier that produces a control voltage v_c. This control voltage is than compared with constant frequency saw tooth waveform to produce required duty cycle of the power switch. The saw tooth waveform defines the switching frequency. The bandwidth of the current loop is very high such as decade of the switching frequency. The higher bandwidth current controller allows the input current to follow reference current with lower noise.

The output loop has an output voltage controller for regulating the output voltage. The output voltage $v_{0(t)}$ is compared with reference voltage v_{ref}. The voltage controller consists of a voltage error amplifier that produces error voltage V_{AOUT}

according to the variations in the output voltage. This error voltage V_{AOUT} programs the current reference magnitude.

High power factor operation is obtained by average current mode control. The input current follows the sinusoidal reference. Finally, the input current and the voltage of the PFC system will have the same waveform and phase.

3.2 Power Balance Analysis of the PFC Circuit

In a converter system, the output voltage should be regulated to the required level by a voltage controller in a closed system. Generally, the output voltage is constant in a DC-DC converter. The constant dc output voltage $v_{0\ (t)} = V$ is obtained by a wide bandwidth voltage controller. If the converter has constant load, the instantaneous load power is also constant.

$$p_0(t) = P_0 = v_0(t)i_0(t) = VI \tag{3.1}$$

Generally, the load of a PFC system is a DC/DC converter. This load draws constant power. But the instantaneous input power $p_{ac\ (t)}$ is not constant.

$$p_{ac}(t) = v_g(t)i_g(t) \tag{3.2}$$

where $v_g(t)$ and $i_g(t)$ are input ac voltage and current, respectively. The instantaneous input power can be written according to resistor emulation concept by using the peak input voltage value.

$$p_{ac}(t) = \frac{V_M^2}{R_e}\sin^2 \omega t = \frac{V_M^2}{R_e}(1 - 2\cos \omega t) \tag{3.3}$$

The input power varies with time. The output capacitor provides power balance to maintain the input-output power balance. The difference between input and output power flows through output electrolytic capacitor. So the power on the output

capacitor can be written:

$$p_c(t) = p_{ac}(t) - p_0(t) = \frac{d(\frac{1}{2}Cv_c^2(t))}{dt} \tag{3.4}$$

where $v_c(t)$ is output capacitor voltage. When $p_{ac}(t) > p_0(t)$ than energy flows into output capacitor and $v_c(t)$ increases. When $p_{ac}(t) < p_0(t)$, the capacitor voltage $v_c(t)$ decreases. So the capacitor voltage increases and decreases for power balance action. The changes of input power and capacitor voltage are shown in Figure 3.2.

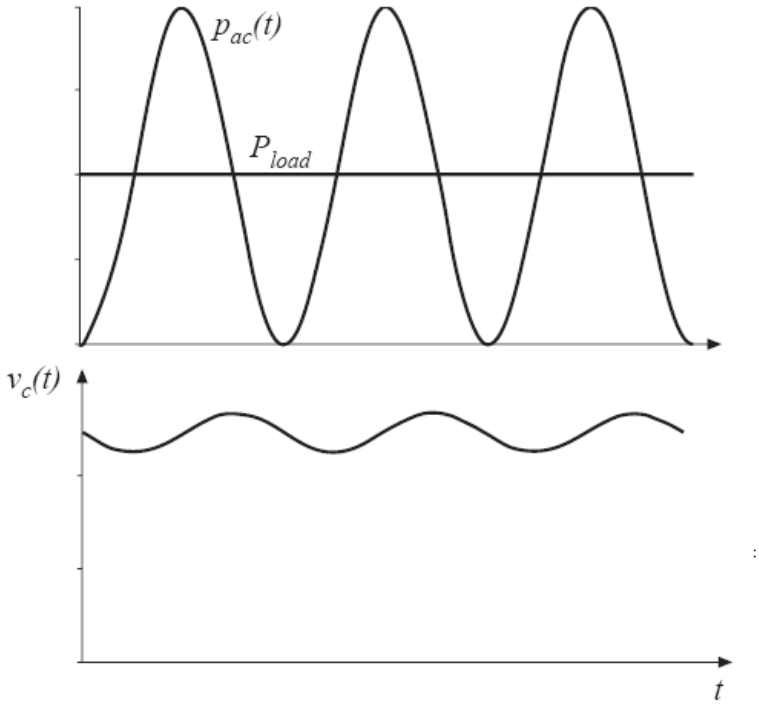


Figure 3.2 Variation on the capacitor voltage.

The output voltage regulation is achieved by comparing the actual output capacitor voltage with reference voltage. The error voltage amplifier provides enough amplitude information for current reference for power balance operation. A block diagram of the outer voltage loop is shown in Figure 3.3.

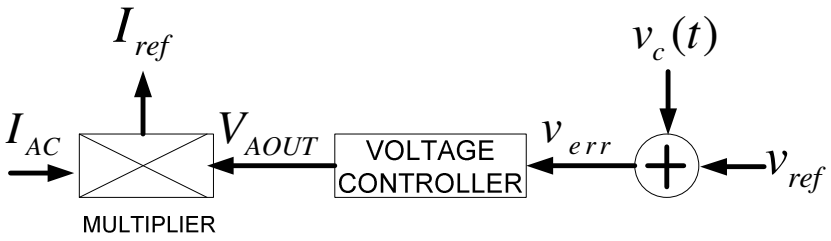


Figure 3.3 Multiplier based control.

It is known that the output capacitor voltage has a 2nd harmonic component (100 Hz) as defined in equation 3.3. The output capacitor voltage can be expressed by the combination of DC voltage plus a second harmonic component as:

$$v_c(t) = V + v_{ripple}(t) \tag{3.5}$$

where $v_{ripple}(t) = V_{ripple}\cos(2\omega t)$ is second harmonic voltage ripple due to second harmonic current component of the output current. This ripple voltage lags the ripple current by 90°. It is assumed that reference voltage v_{ref} is equal to the DC component of $v_c(t)$.

$$v_{ref} = V \tag{3.6}$$

So the error voltage v_{err} is equal to only second harmonic component of the capacitor voltage.

$$v_{err} = V_{ripple}\cos(2\omega t) \tag{3.7}$$

Assume that the voltage controller compensator has wide bandwidth so 2nd harmonic component feeds back through the voltage error amplifier. A general equation for the output of the voltage error amplifier V_{AOUT} can be written as:

$$V_{AOUT} = k_1 V_{ripple}\cos(2\omega t) \tag{3.8}$$

In a multiplier based system shown in Figure 3.3, the current reference I_{ref} is obtained by the multiplication of the current reference waveform I_{AC} with the output of the voltage error amplifier V_{AOUT}.

$$I_{ref} = I_{AC} V_{AOUT} \tag{3.9}$$

It is known that waveform component I_{AC} of the current reference evaluated from the rectified input voltage has only sinusoidal waveform information. So a general equation for this component I_{AC} can be written as:

$$I_{AC} = k_2 . \sin(\omega t) \tag{3.10}$$

So the reference current I_{ref} can be written as:

$$I_{ref} = I_{AC} V_{AOUT} = k_2 . \sin(\omega t) . k_1 V_{ripple} \cos(2\omega t) \tag{3.11}$$

The equation can then be rearranged as:

$$I_{ref} = k_1 k_2 \left(\frac{1}{2} V_{ripple} \sin(\omega t) + \frac{1}{2} V_{ripple} \sin(3\omega t) \right) \tag{3.12}$$

It is shown in the equation above that, the 2nd harmonic distortion on the output voltage distorts the input current reference I_{ref}. The second order harmonic component of the output voltage adds a 3rd harmonic component to reference current with a half magnitude of the second harmonic component.

So in average current mode controlled PFC system, the input current is forced to follow input current reference. If a distortion occurs in reference current also actual input current distorts. This 3rd harmonic distortion in the input current lower PF. The solution for lowering this distortion is to configure the output voltage error amplifier to block the second harmonic component of the output voltage. This is done by using

an error amplifier that has lower bandwidth. The bandwidth of this controller should be lower than 2nd order frequency of the line voltage such as 20 Hz. But lower bandwidth means slower response. The slower transient response makes the dc regulation worse. A designer should consider the trade-off between lower THD and faster transient response. Generally, the load of PFC system is a second DC-DC converter that has a tight output voltage regulation. So the designer should choose better input current waveform. But if the second DC-DC converter needs a narrow range input voltage, the designer should consider transient response. There are some strategies to get better voltage loop response as given in literature [46], [47], [48], [49]. But the solution is inside the application. Detailed analyses of the voltage loop are given in the control circuit description section.

3.3 Input Voltage Feed-Forward

It was mentioned that a power factor pre-regulator is generally the first stage of a two-stage power supply system. The second stage is the load of the PFC stage and composed of a constant power DC-DC converter. So PFC stage has a constant power load that does not change with the input rms voltage. The PFC stage maintains a fairly constant output voltage and the load draws constant power regardless of the variations of output voltage of the PFC stage. In a high efficient PFC circuit, if the output load power is constant, the input power drawn from line does not change with rms line voltage. So if there is a change in input rms voltage, the input rms current should change inversely proportional to the rms input voltage. But it is known that the reference current is directly proportional to the input line voltage in an average current controlled PFC in Figure 3.1. There is a conflict between power balance and control circuit when operated in universal line (90-270 Vac).

Basically, the current reference I_{ref} is obtained by multiplication of the input voltage waveform information signal I_{AC} and the output voltage error signal V_{AOUT}. It is assumed that the PFC circuit operates with 120Vac input voltage V_{IN} with constant output power. The waveforms for the input voltage V_{IN} and the corresponding input current I_{IN} for 120-Vac operation are shown in Figure 3.4.

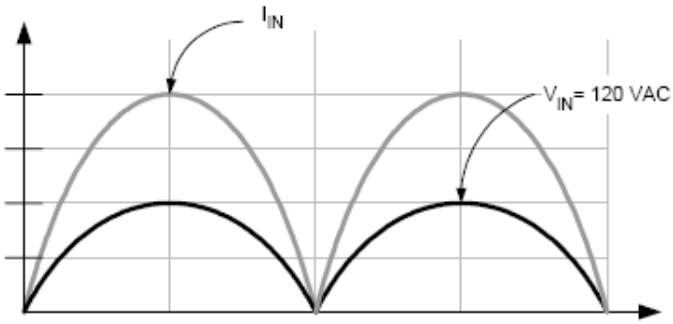


Figure 3.4 Rectified line voltage and current for 120-Vac line voltage.

The multiplier inputs I_{AC} and V_{AOUT} are shown in Figure 3.5 for 120-Vac operation.

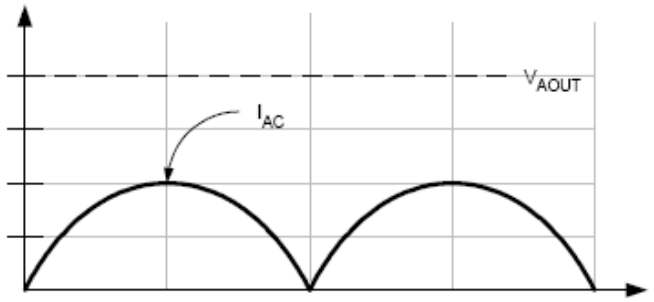


Figure 3.5 Multiplier inputs I_{AC} and V_{AOUT} at 120-Vac line voltage.

Assume PFC is operating in universal input line and the input voltage V_{IN} is doubled from 120 Vac to 240 Vac. When input voltage V_{IN} is doubled, input current I_{IN} should be halved in order to maintain constant power to the load. The waveforms for the input voltage V_{IN} and the corresponding input current I_{IN} for doubled input voltage operation are shown in Figure 3.6.

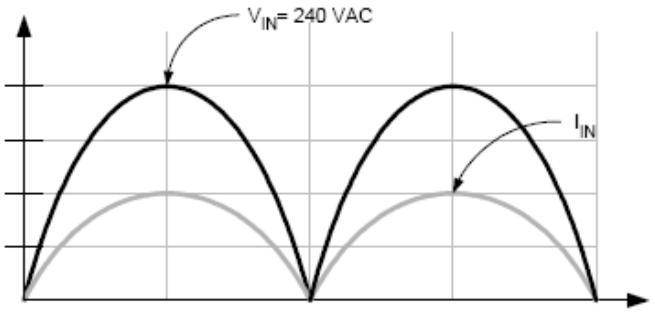


Figure 3.6 Rectified line voltage and current for 240-Vac line voltage.

The multiplier input I_{AC} is directly proportional to the input voltage V_{IN}. When V_{IN} is doubled, I_{AC} is also doubled. The multiplier output I_{ref} is current reference for the actual input current I_{IN}, has to halve, that can only be accomplished by reducing voltage error amplifier voltage V_{AOUT} by factor four. The multiplier inputs I_{AC} and V_{AOUT} are shown in Figure 3.7 for 240-Vac operation.

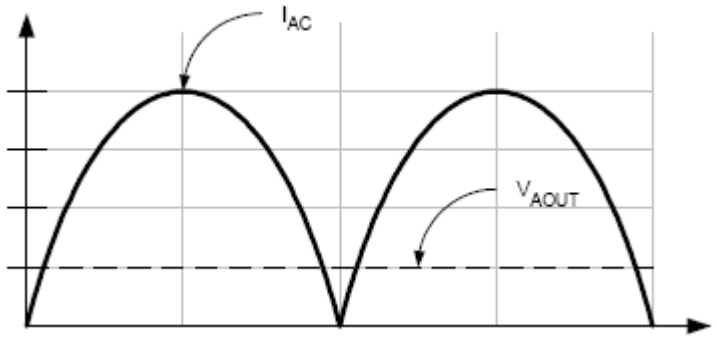


Figure 3.7 Multiplier inputs I_{AC} and V_{AOUT} at 240-Vac line voltage.

So the optimum PFC performance is obtained by fast response voltage loop controller in a universal power line operation. But the voltage loop limitation problem has already been mentioned in the previous section. The outer voltage loop controller should have small bandwidth in order to remove the second harmonic component in the voltage feedback circuit. The output of the voltage feedback controller should be constant in the half cycle of line frequency. If the voltage loop controller has small bandwidth, the control circuit should be independent of the line voltage in order to solve the problems due to the variations of the line voltage. The solution is called as input voltage feed-forward.

The input voltage feed-forward makes the control circuit independent from the input line voltage by modifying the multiplier concept. A new signal proportional to the input voltage is added to the input of the multiplier. This signal is called as feed-forward and represented by V_{FF}. The feed-forward signal V_{FF} is squared and inversed so V_{FF} signal becomes as a divider factor ($1/ V_{FF}^2$). The modified average control system with input voltage feed-forward is shown in Figure 3.8.

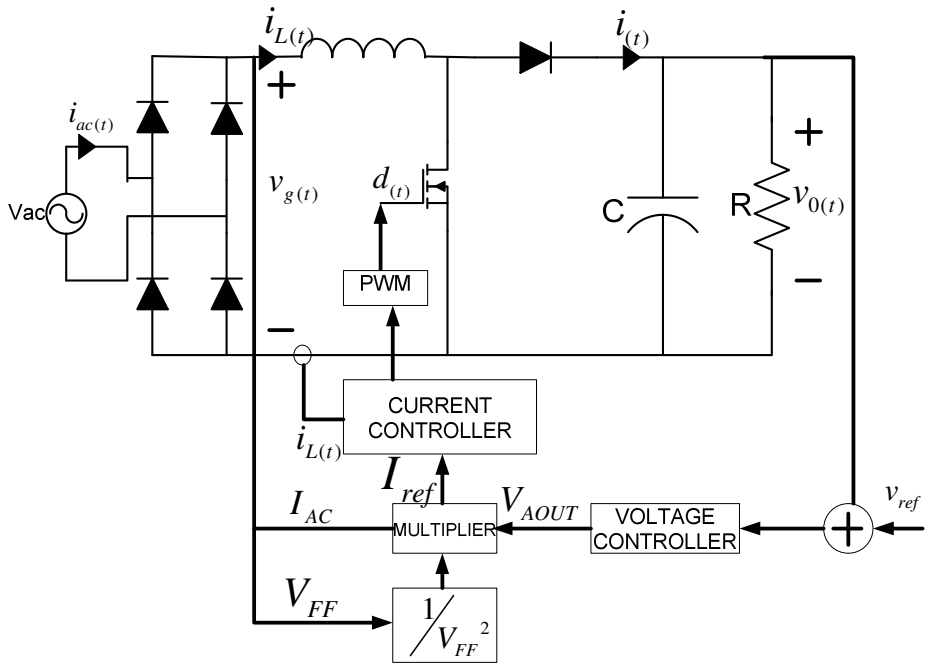


Figure 3.8 Block diagram of the average current PFC with feed-forward.

The new control strategy provides independent operation of voltage error controller to the input voltage variations. In fact, the output voltage error amplifier is only dependent on the output power. If the input voltage doubles, the doubled I_{AC} signal is divided by factor four by the new input feed-forward signal ($1/ V_{FF}^2$). So the new current reference I_{ref} is equal to half of the original signal before doubling line voltage without any change in V_{AOUT}. The new equation for the current reference I_{ref} can be written as:

$$I_{ref} = k\frac{I_{AC}V_{AOUT}}{V_{FF}^2} \tag{3.13}$$

The control system with input voltage feed-forward has all the capabilities for high power factor application for universal input line. The current reference I_{ref} is the combination of I_{AC} that has the waveform of the rectified input voltage and V_{AOUT} that is proportional to the output power. And it is mentioned that the output voltage loop has smaller crossover frequency and the output V_{AOUT} is constant during line

cycle. The other input I_{AC} of multiplier is derived by a resistor dividing circuit of rectified input voltage so I_{AC} varies during line cycle. The third input of the multiplier is the feed-forward signal V_{FF}. Now the design of the feed-forward application will be considered.

Since the feed-forward signal V_{FF} consists of the rms input voltage information, this signal can be obtained by resistor divider connected to the dc side of bridge rectifier. Since the rectified input voltage has large 2nd harmonic component, the feed-forward signal V_{FF} should be filtered. This averaging network is done by low pass filter. The first order averaging low pass filter for the feed-forward signal V_{FF} is shown in Figure 3.9.

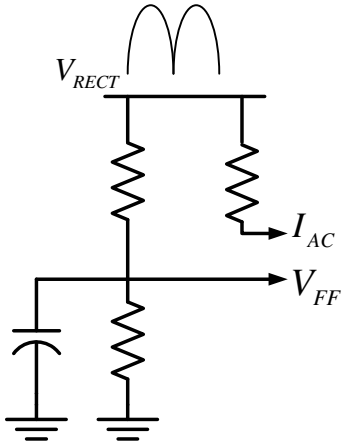


Figure 3.9 First order input voltage feed-forward sensing scheme.

The capacitor averages the rectified input voltage waveform and reduces the 2nd harmonic ripple. The time constant of the filter network defines the amount of the 2nd harmonic ripple in the input of the multiplier. If time constant (RC) is smaller, the feed-forward compensation network will have a faster response but 2nd harmonic ripple will be high. This will reduce power factor. If the time constant is larger, there will be too much feed-forward delay resulting in worse transient response such as higher overshoots. The transient response can be increased with lower 2nd order ripple distortion and can be achieved by a second order low pass filter as shown in Figure 3.10.

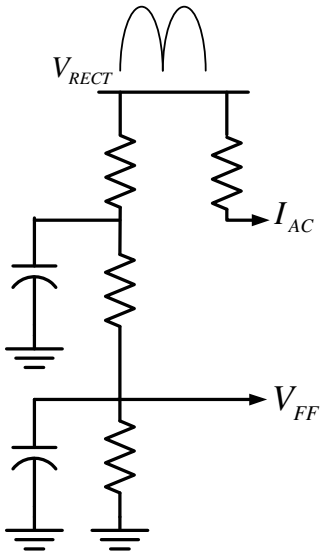


Figure 3.10 Second order input voltage feed-forward sensing scheme.

A second order low pass filter network can increase the complexity and manufacturing cost. In fact, input voltage does not change instantaneously so fast transient response is not really required. Some new generation IC's combines the evaluation of I_{AC} and V_{FF} (e.g. UCC3817). The feed-forward signal V_{FF} is obtained by mirroring I_{AC} signal so a second resistor divider circuit is removed. The new voltage feed-forward sensing schemes is shown in Figure 3.11.

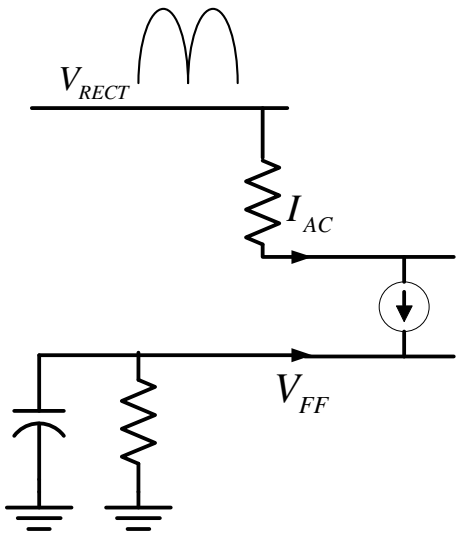


Figure 3.11 First order input voltage feed-forward sensing scheme.

The amount of ripple on the feed-forward signal V_{FF} distorts the input current. The low pass filter attenuates most of 2nd order harmonic but some 2nd order harmonic exists in feed-forward signal. The distortion is the same as the voltage loop distortion explained in the previous section. 2nd harmonic ripple in the feed-forward signal causes 3rd harmonic distortion in the line current. But the amplitude of the 3rd harmonic distortion is equal to the 2nd harmonic ripple amplitude in the feed-forward signal due to squaring process. On the other hand, distortions due to feed-forward sensing scheme and voltage loop have the same phase and are multiplied as the inputs of the multiplier.

3.4 Control Loop Design

In average current controlled PFC application, there are two control loops that provide a sinusoidal input current in phase with input voltage. The design of the voltage and current loops has significant affects in the system performance, such as amount of THD and PF. The control circuit has inner current loop that ensures the form of I_{ref} based on the input voltage. The outer voltage loop determines the amplitude of the current reference I_{ref} based on the output voltage feedback. The outer voltage loop adjusts the inductor current amplitude to bring the output voltage to the reference voltage. The block diagram of the control loops for an average current controlled PFC is shown in Figure 3.12.

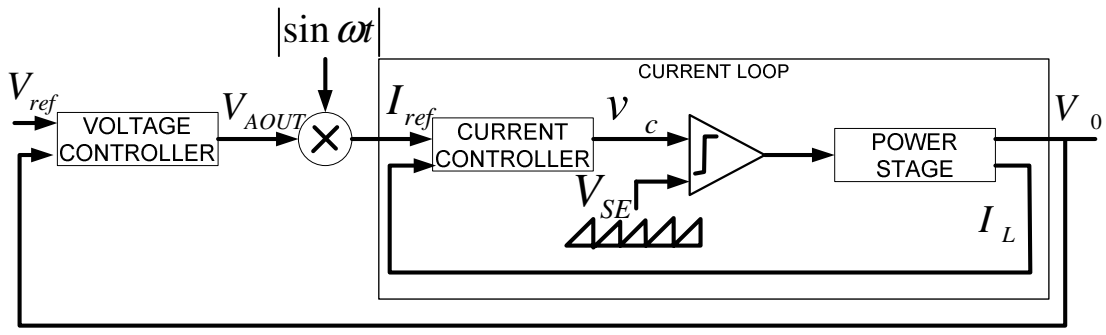


Figure 3.12 PFC control loops.

The control loops are designed separately. The inner current loop has higher bandwidth. The voltage loop has lower bandwidth due to distortion factors.

3.4.1 Current Loop Design

Inner current loop of average current controlled PFC needs inductor current sensing. The sensed current via shunt resistor or current transformer is compared with reference current that is output of the multiplier. The error between actual inductor current and the reference current is amplified with a properly designed current compensator. The output of the compensator is compared with a saw tooth waveform to produce required duty cycle for the PFC boost operation. The main feature of the average current control is the presence of the current error amplifier (compensator) that provides controlling the average inductor current. The inner current loop block diagram can be built with the combination of the current sensing circuit, current error amplifier, PWM generator and power stage of the PFC boost converter as shown in Figure 3.13.

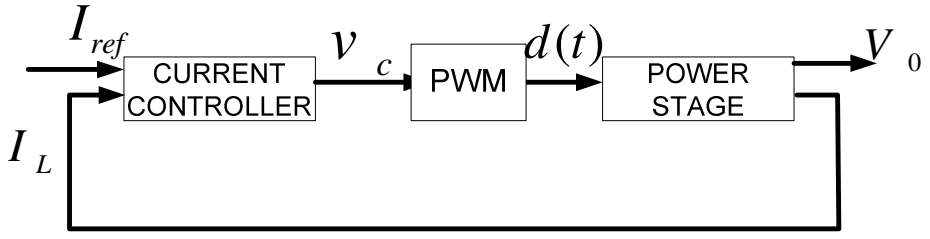


Figure 3.13 PFC current loop.

The inner current loop has large bandwidth around one decade of the switching frequency. A small signal model of the inner current loop is needed to design a proper compensator with optimum performance and stability. A Laplace domain of the inner current loop is shown in the figure 3.14.

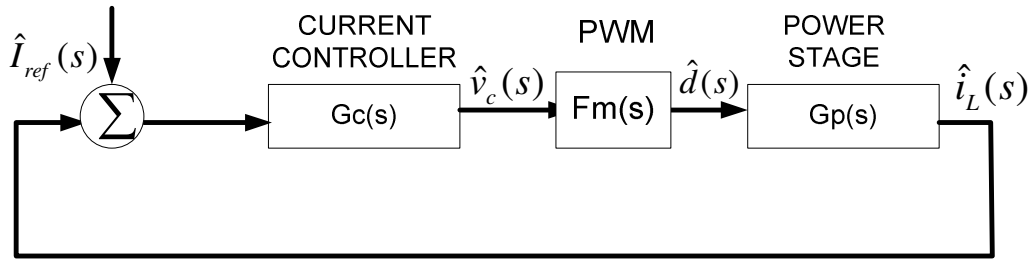


Figure 3.14 Laplace domain block-schema of the current loop.

The open loop transfer function of the inner current loop can be written as:

$$T_i(s) = F_m(s)R_s G_p(s)G_C(s) \tag{3.14}$$

where F_m (s) is modulator gain of the PFC controller, R_s is the current sensing resistor, G_p(s) is power stage transfer function, and G_c (s) is current compensator transfer function.

The transfer function of the modulator is dependent on the peak value of the ramp voltage in the PWM controller. So the transfer function of the modulator can be written as:

$$F_m(s) = \frac{1}{V_{SE}} \tag{3.15}$$

where V_{SE} is equal to the peak-to-peak amplitude of the external ramp.

A small signal model of the power converter is needed for the design of the current compensator. The averaged small-signal model of the converter defines the dependence of the average input current on the duty cycle. When the converter operates at steady-state, the output voltage has small variations around a steady-state component. The output voltage can be expressed as:

$$\left\langle v_0(t)\right\rangle_{Ts} = V + \hat{v}(t) \tag{3.16}$$

where

$$\hat{v}(t) \ll V \tag{3.17}$$

The averaged small signal model of the PFC boost converter with dynamically changed variables is shown in Figure 3.15. The linearization and the perturbation procedure are used for completing the small signal model of the converter.

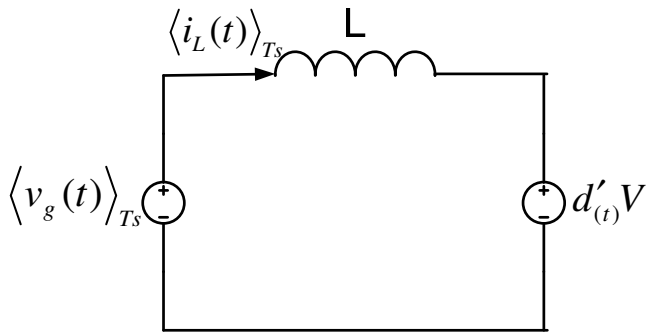


Figure 3.15 Linearized model of the PFC boost converter.

The average inductor voltage of the PFC boost converter can be written as:

$$L\frac{d\left\langle i_L(t)\right\rangle_{Ts}}{dt} = \left\langle v_g(t)\right\rangle_{Ts} - d'(t)\left(V + \hat{v}(t)\right) \tag{3.18}$$

The nonlinear term $d'(t)\hat{v}(t)$ in the equation (3.18) is much smaller than the linear term $d'(t)V$. Therefore, this nonlinear term can be discarded. The average inductor voltage can be obtained as:

$$L\frac{d\left\langle i_L(t)\right\rangle_{Ts}}{dt} = \left\langle v_g(t)\right\rangle_{Ts} - d'(t)V \tag{3.19}$$

The equivalent circuit given in Figure 3.15 is used to obtain control-to-input transfer function by using the equation (3.19) and found by setting the independent inputs to zero and solving the inductor current I_g. The simplified small signal transfer function of the PFC boost converter $G_p(s)$ is written as:

$$G_p(s) = \frac{i_L(s)}{d(s)} = \frac{V}{sL} \tag{3.20}$$

The open loop transfer function of the current loop without the current compensator $G_{id}(s)$ can be written as the combination of the power stage, sensing resistor and PWM modulator.

$$G_{id}(s) = F_m(s) R_s G_p(s) \tag{3.21}$$

and

$$G_{id}(s) = \frac{VR_s}{sLV_{SE}} \tag{3.22}$$

The complete open loop transfer function of the current loop with current compensator $T_i(s)$ is

$$T_i(s) = G_{id}(s) G_C(s) \tag{3.23}$$

The current compensator is designed according to the behavior of the converter without the current compensator. The current compensator should be designed for optimal performance and stability for overall current loop. The Bode blot of the $G_{id}(s)$ is a good reference for the design of the current compensator. The Bode plot of the $G_{id}(s)$ with arbitrary chosen values (L = 1mH, V_0 = 400V, V_{SE} = 4V) is shown in Figure 3.16.

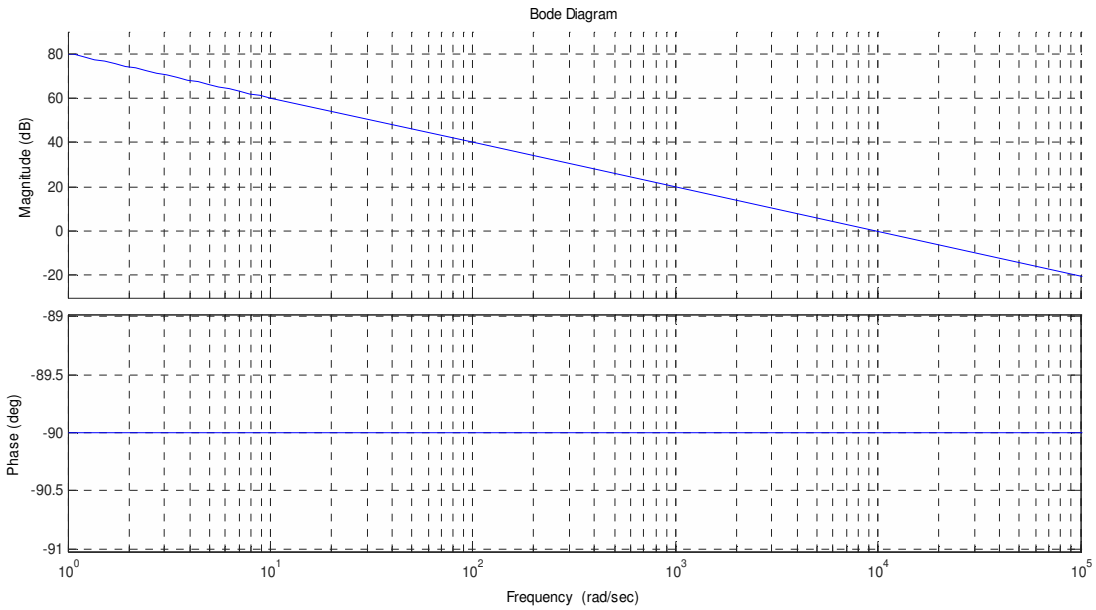


Figure 3.16 Magnitude and phase plots of the converter transfer function $G_{id}(s)$.

It can be seen from Figure 3.16 that the power stage transfer function has a single pole response at the usual frequencies. A two-pole, single-zero error amplifier can be used as a current compensator in the average current control method [31], [33], [50]. A pole placed at the origin provides a higher loop dc gain and zero dc steady-state error in the current controller transfer function G_c (s). The zero is placed to achieve the desired phase margin for stability purposes. The other pole is placed generally at one half of the switching frequency to filter the switching noise. A general equation for a two-pole, single-zero current compensator is given below:

$$G_C(s) = \frac{\omega_i}{s} \frac{(1 + s/\omega_z)}{(1 + s/\omega_p)} \tag{3.24}$$

The construction of a two-pole, single-zero current compensator and a general gain response are shown in Figures 3.17.a and 3.17.b, respectively.

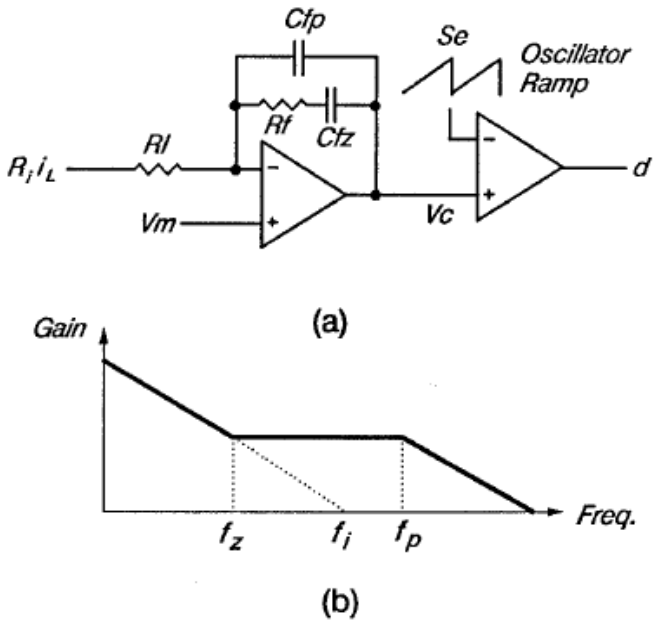


Figure 3.17 (a) Circuit Diagram (b) Gain response of current compensator.

It is shown that, if the high frequency pole is placed at or after half of the switching frequency to filter out the switching ripple of the sensed inductor current, it has no effect on the gain and the phase of the current – loop gain before the half of the switching frequency. Only the pole placed at the origin (acting as integrator) and the zero affect the current loop gain below half of the switching frequency. The current loop should be designed to have maximum low frequency gain and acceptable phase margin at the crossover frequency to minimize the input current distortions. The overall current loop transfer function can be written as:

$$T_i(s) = \frac{VR_s}{sLV_{SE}} \frac{\omega_i}{s} \frac{(1 + s/\omega_z)}{(1 + s/\omega_p)} \tag{3.25}$$

The compensated current loop transfer function has the following gain and phase responses shown in Figure 3.18.

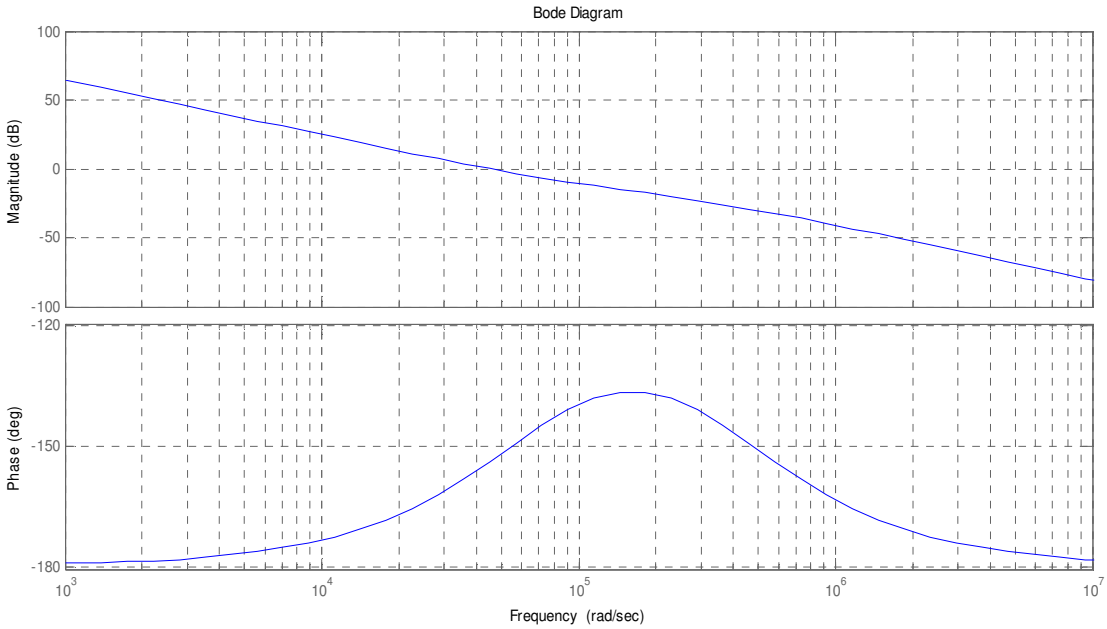


Figure 3.18 Compensated loop gain and phase plots of the inner current loop.

3.4.2 Voltage Loop Design

The outer voltage loop determines the required amplitude of the current reference due to the requirement for the power balance operation. On the other hand, it was mentioned that the outer voltage loop should have limited bandwidth, less than half of the line frequency, for minimum distortion in the line current. This limited bandwidth brings slower transient response. The outer voltage loop should be designed for optimal transient response with minimal input current distortion due to the 2nd harmonic component in the output capacitor voltage. The block diagram of the outer voltage loop can be constructed with closed current loop as shown in Figure 3.19.

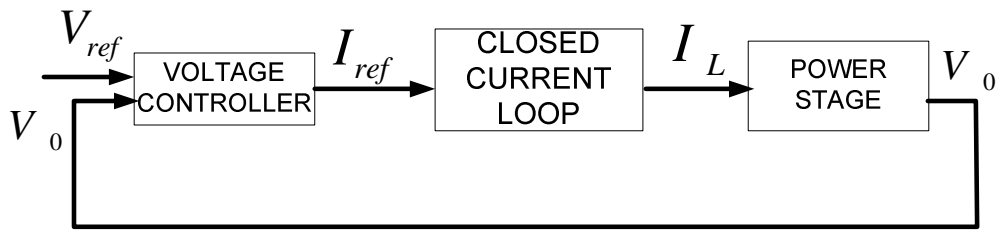


Figure 3.19 Voltage control loop.

Assuming the inner current loop is well designed, it provides a good current regulation according to the predefined current reference. It can be assumed that the closed current loop has no effect in the outer voltage loop, simply behaves as a unity gain block in the block diagram of the voltage loop shown in Figure 3.19. So the only thing is the design of the voltage error amplifier. This voltage compensator should be designed according to low frequency behavior of the power stage of the PFC. Because the outer voltage loop has smaller crossover frequency around 20 Hz, a small signal model of the power stage accurate at frequencies below 100 Hz should be used [7], [31], [51]. The small signal model of the PFC converter consists of a controlled power source modeled as a current source shunted by a resistor as shown in Figure 3.20.

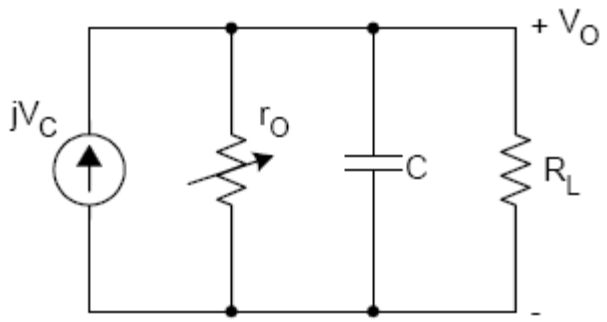


Figure 3.20 Small signal model of outer loop.

The variable source resistance r_o is equal to the load resistance R_L. r_o changes when R_L changes. The load can be a resistive load or a constant power load such as a dc-dc converter. In the case of resistive load, r_o is equal to the load resistance R_L and the parallel combination of these variables defines the single pole response of the transfer function. However, in the case of the constant power load, it has a negative small signal resistance ($-R_L$). The negative resistance is equal and opposite in sign to the dc resistance and parallel combination approaches infinity. So the model becomes a current source driving a dc capacitor. So the power stage transfer function will have a single pole response that is placed at 0 Hz. The power stage transfer function can be written by using this simple circuit, current source driving the dc

capacitor, by using the power changes in the output capacitor.

$$G_{PS}(s) = \frac{P_{in}}{sCV_0\Delta V_{aout}} \tag{3.26}$$

where ΔV_{aout} is equal to the voltage ripple in the capacitor voltage.

The voltage compensator should have a pole at the origin to achieve zero steady-state error. This integral compensation adds another 90 degrees of the phase shift at low frequency, since the transfer function of the power stage has single pole roll-off. A zero is needed to achieve optimal phase margin and placed before the loop crossover frequency. The location of the zero should be chosen as high as possible in frequency considering a zero will be a dominant pole in the closed loop system. So a high frequency zero provides better transient response in the closed loop system. The second pole is placed at the loop crossover frequency. A two-pole, single-zero voltage compensator is the best choice for better transient response and low current distortion. The general definition for the voltage controller is given in the equation (3.27).

$$G_V(s) = \frac{\omega_i}{s}\frac{(1+ s/\omega_z)}{(1+ s/\omega_p)} \tag{3.27}$$

The voltage loop is designed according to chosen output capacitor value, output voltage ripple and allowable input current distortion.

3.5 Simulation of Average Current Control PFC

Single Phase average current mode controlled PFC circuit is simulated by SIMPLORER simulation tool and simulation results are verified. The simulated circuit and control blocks are shown in Figure 3.21.

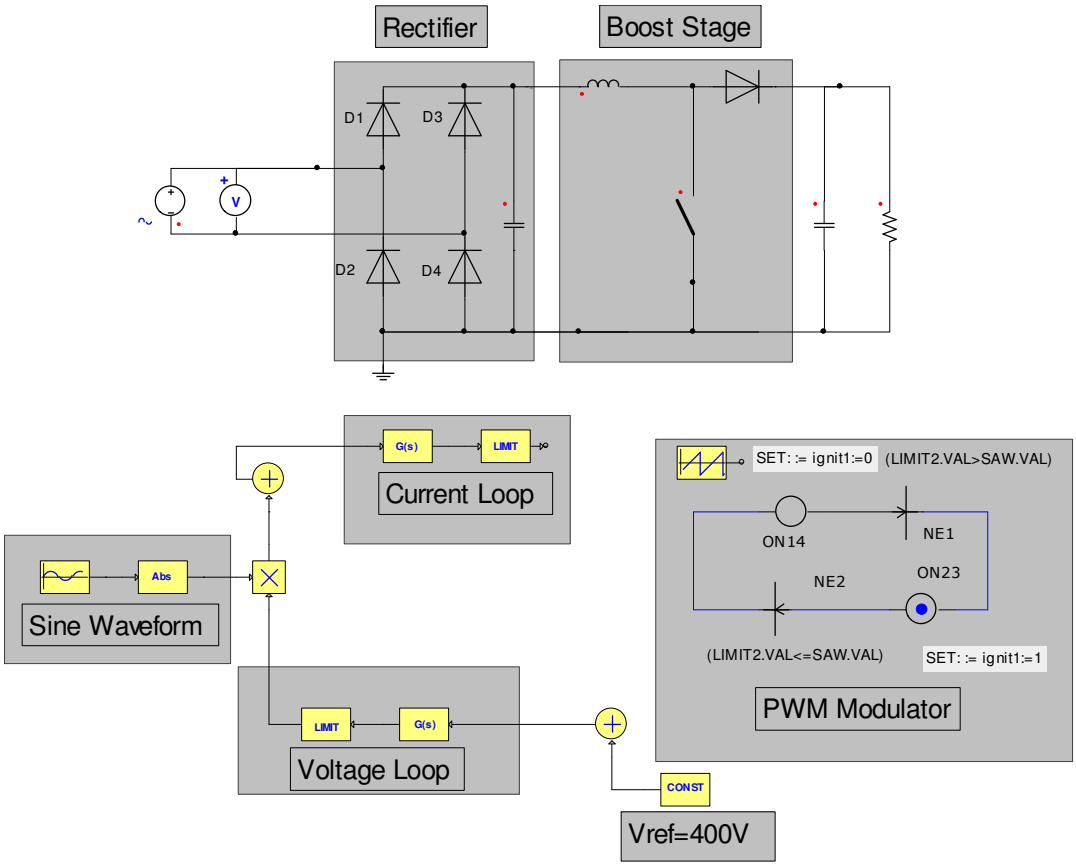


Figure 3.21 Simulation block diagram of average current mode PFC.

The performance analyses of average current controlled PFC is done by simulation methods. The input current and output voltage simulation waveforms are illustrated and analyzed. The current waveform behavior for different input voltages and the output voltage differences at step load conditions are verified. The circuit is simulated with the following simulation parameters given in Table 3.1.

Table 3.1 Simulation parameters of average current mode PFC

Output Power, P_0	250 W
Input Voltage, V_{in}	90-265V
Input Voltage Frequency	50Hz
Switching Frequency	100 kHz
Output Voltage, V_0	400V
Boost Inductor, L	1mH
Output Capacitor, C_0	330uF
Integration Formula	Euler
Minimum Step Time	0.1u

The control loops for average current mode control is implemented by s-block sub-circuit in the simulation system. The output voltage controller is chosen as a low bandwidth error amplifier. The output voltage controller has two poles and one zero characteristics with 20 Hz crossover frequency. A pole is placed at origin where the other pole is placed at crossover frequency. The zero is placed before the crossover frequency for stability reasons. The current controller is also implemented by s-block sub-circuit. The current controller has two poles and one zero with one decade of switching frequency crossover (10 kHz). The zero is placed at crossover frequency and the pole is placed at half of the switching frequency to filter the higher switching frequency noises. The used parameters for the voltage controller (GS1) and current controller (GS2) are shown in Figure 3.22.

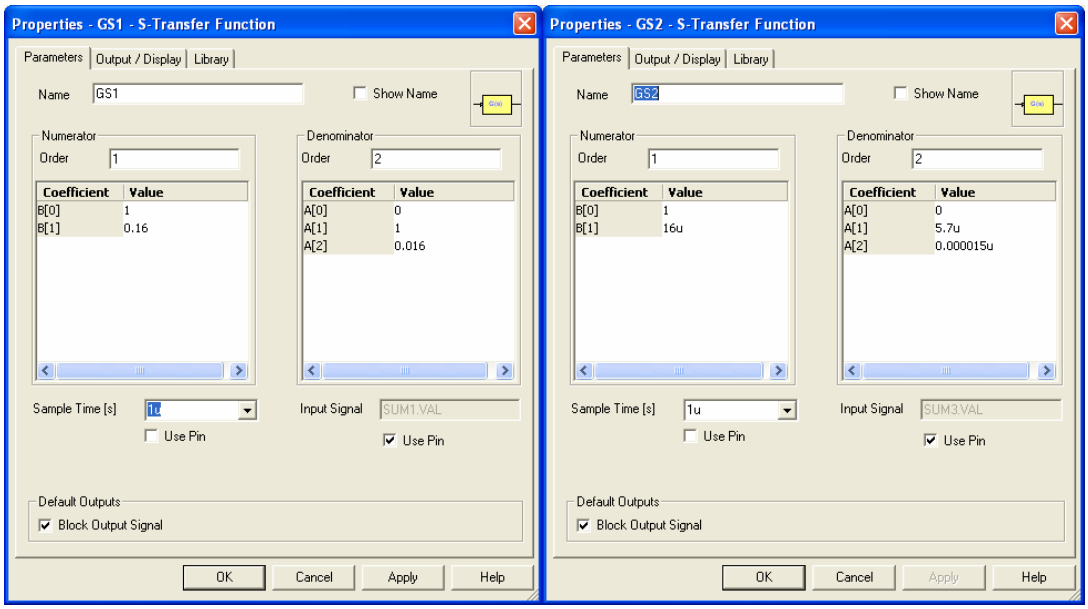


Figure 3.22 S-Transfer function for the voltage and current controller used in simulation.

The simulation results for the input voltage and the input current for 220-V input voltage at full-load is shown in Figure 3.23.

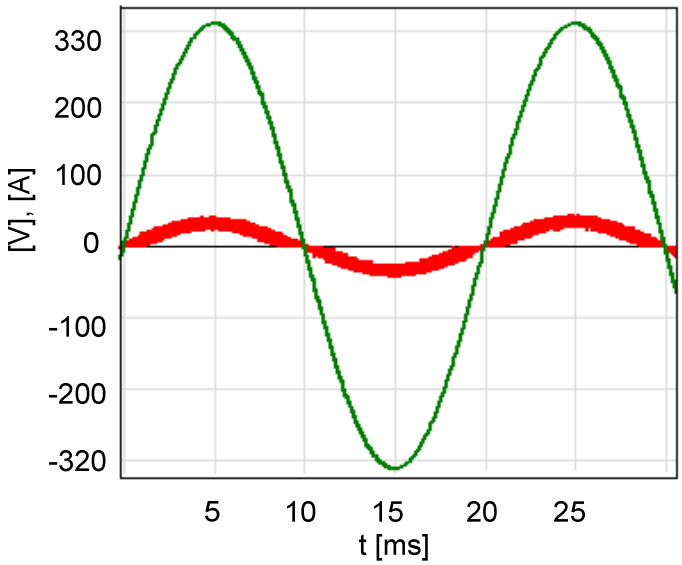


Figure 3.23 Line voltage and line current simulation waveforms for 220-V input voltage at 250-W PFC system (current scale: 10x).

The output voltage reference is defined as 400 Vdc. The output voltage and input current simulation waveforms are at steady state for 220 V input voltage and full-load output power is shown in Figure 3.24.

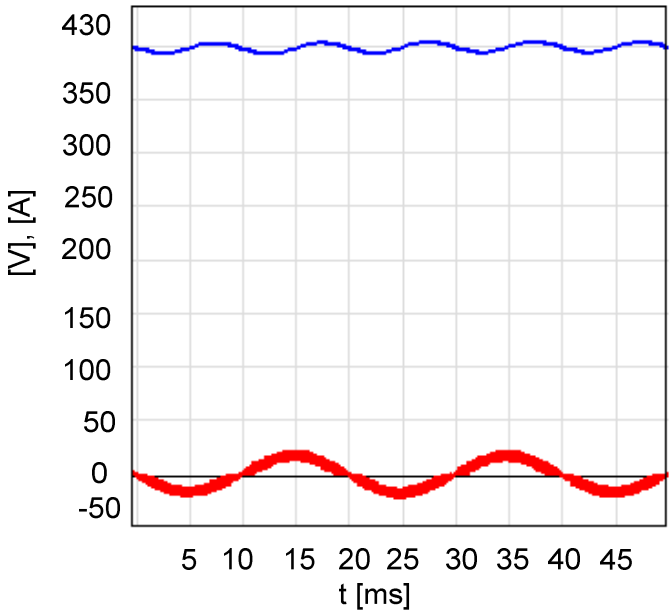


Figure 3.24 Output voltage and input current simulation waveforms for 220 V input voltage at 250-W PFC system (current scale: 10x).

The system is simulated for the lower input voltage conditions. The input voltage is lowered to 120 Vac and the corresponding current and output voltage waveforms are simulated. The input voltage and input current simulation waveforms for 120 Vac at full-load power are shown in Figure 3.25.

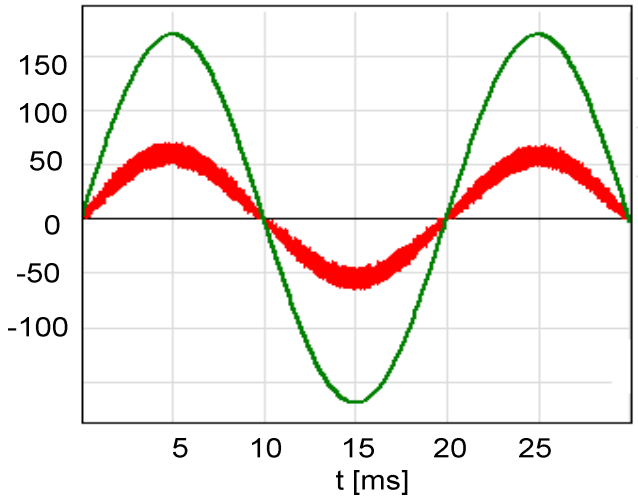


Figure 3.25 Line voltage and line current simulation waveforms for 120 V input voltage at 250-W PFC system (current scale: 10x).

The output voltage and input current simulation waveforms for 120 V input voltage at full-load are shown in Figure 3.26.

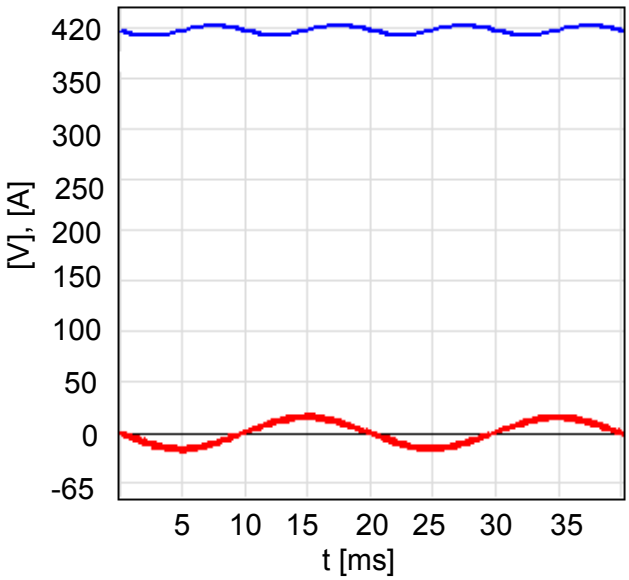


Figure 3.26 Output voltage and input current simulation waveforms for 120V input voltage at 250W PFC system (current scale: 10x).

The transient response for the outer voltage control loop is satisfied with the simulation. The load is increased from half load to full load at steady-state and the corresponding changes at the output voltage and input current are illustrated by the simulation. The step response for the output voltage and input current is shown in Figure 3.27.

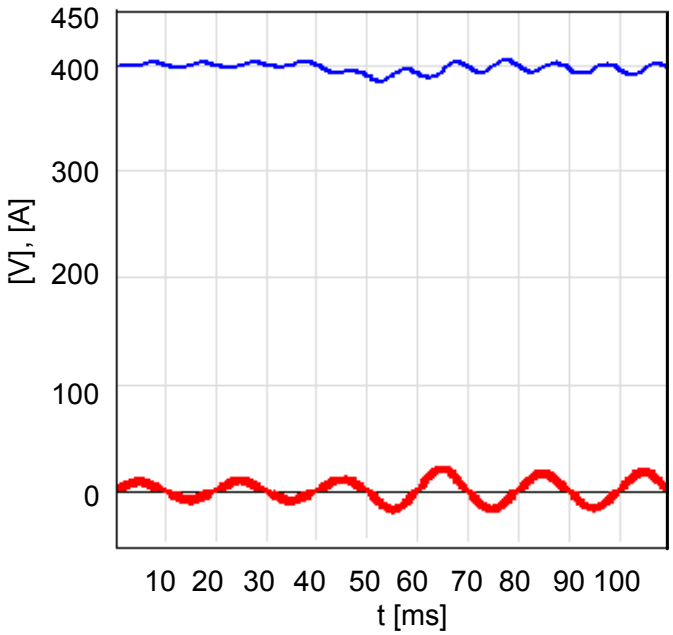


Figure 3.27 Step response for output voltage and input current simulation waveforms for 220 V input voltage at half-load to full-load step (current scale: 10x).

In the above simulation results, it is shown that a sinusoidal input current waveform is achieved for different input voltage values by the average current mode controlled PFC. There are some distortions in the input current at the zero crossings of the input voltage due to the lower inductor voltage at these regions. The lower inductor voltage cannot provide enough inductor current to track reference waveform. In the case of the lower input voltage such as 120 Vac, these distortions are smaller. The output voltage controller has limited bandwidth and shows slower response to transient situations. But it is seen from Figure 3.27 that the voltage and current controller shows optimum response for load changes without any distortions or overshoots.

3.6 Hardware Implementation of Average Current Control PFC

This section describes the general specifications of the power circuit and control circuit elements of an average current controlled power factor correction system. It is known that the single-phase PFC is shaped from a single-phase diode rectifier and a cascaded dc-dc boost converter. The types of the components in the power circuit with their general specifications are summarized briefly in the subsection 3.6.1.

The analog PFC controller IC, UCC3818, is chosen to implement average current mode PFC application. The general parameters and the block diagram of the controller are given in the subsection 3.6.2.

3.6.1 Functional Description of the Power Circuit

The power circuit consists of input bridge rectifier, filtering ac capacitor after bridge, boost inductor, boost switch, boost diode and output capacitor. A current sensing resistor series to power line is placed to sense the inductor current for average current mode control.

An inrush current limiter NTC is placed at the input of the rectifier to limit the start-up current. This inrush current limiter has cold resistance at start-up and a small resistance when the rated current flows through it. A glass fuse is placed at the input of the power line to protect the circuit from high input currents.

A diode is placed between the output of the rectifier and the output capacitor in order to protect the circuit elements during the start-up. It is known that output electrolytic capacitor draws higher currents during initial charging at the start-up so boost diode can saturate at this current level and can damage the circuit elements such as boost diode. This parallel diode conducts only at the start-up because the output voltage is smaller than the input voltage. At steady-state, output voltage will be higher than the input voltage due to boost operation.

Input bridge rectifier is selected according to required ratings of the system. This bridge rectifier is followed by a filtering capacitor. This filtering capacitor reduces the noise in the output of the bridge rectifier and provides a good reference waveform for the current reference. A displacement factor occurs, if the value of this capacitor is high.

The boost inductor, power switch and diode form the boost pre-regulator operation. The boost inductor is made of ferrite core with appropriate ratings. The power switch is selected as a power MOSFET with a small on-resistance. The output diode has fast switching capability with soft recovery characteristics.

The output capacitor is one of the main elements in the power circuit. The value of this electrolytic capacitor affects the output voltage ripple, performance of the voltage error amplifier, hold-up time, and start-up inrush current.

A small current sensing resistor with higher power rating is used to sense the inductor current. This is the easiest way to sense the inductor current but some power dissipation occurs in the sensing resistor. As the system has low power level, current sensing is a good and cheap solution. In high power applications current sensing transformers or Hall-effect devices should be used to sense the current. But these methods need extra circuit to amplify the sensed current to the appropriate value for the controller.

3.6.2 Functional Description of the Control Circuit

The control circuit is implemented with the Texas Instruments integrated circuit UCC3818 and the required external circuit elements. The UCC3818 controller IC provides average current mode. The controller IC needs external passive components chosen according to the application. The IC has internal reference voltage generator, current and voltage error amplifiers, saw tooth oscillator, gate drive circuit with soft start and peak current limiting features. The block diagram of the controller IC is shown in Figure 3.28.

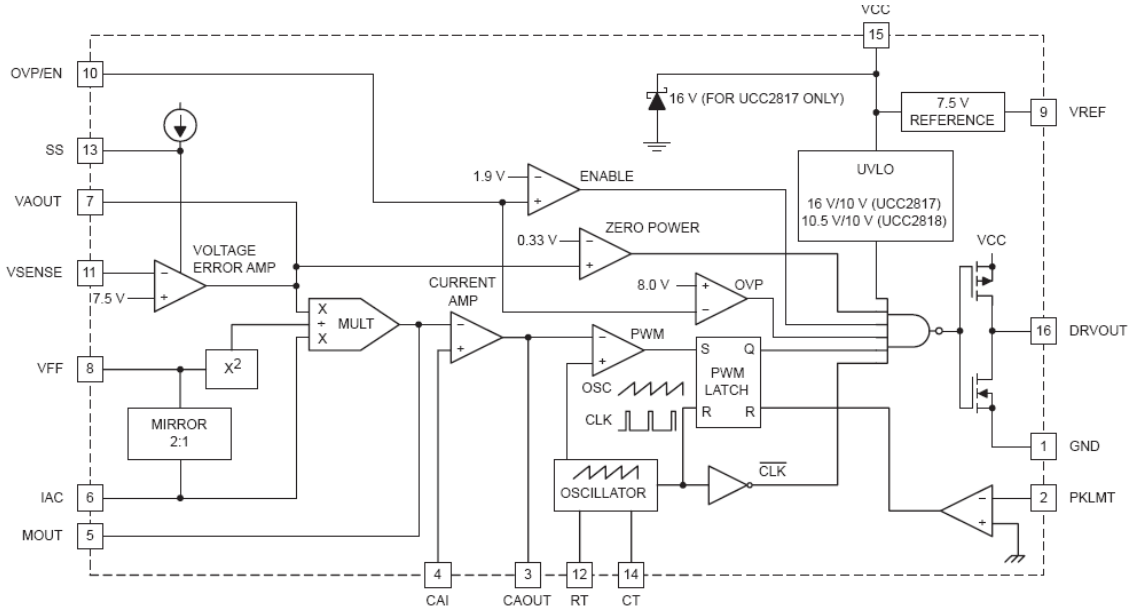


Figure 3.28 Block diagram of the UCC3818 controller IC.

The controller IC operates with constant 12-Vdc power supply. The IC has internal reference voltage generator (7.5V) that is used as an output voltage reference in a voltage negative feedback loop. The power supply of the IC has under-voltage lockout circuit that ensures the turn-off of the power MOSFET in case of low power supply of the IC (around 10 Vdc).

The controller IC has internal multiplier to produce the required reference signal. The inputs for the multiplier are the voltage compensator output, instantaneous input voltage signal and averaged input voltage signal (feed-forward signal). The feed-forward signal is obtained by mirroring the instantaneous input voltage and passed through a voltage averaging network. So there is no need for a new resistor divider circuit to evaluate the feed-forward signal.

The voltage and current error amplifiers are formed by operational amplifiers inside the UCC3818. The outputs of the compensators are pinned out to place the required external passive elements for the operation and the stability of these loops.

UCC3818 has internal oscillator for the PWM circuit inside it. The frequency of the oscillator is defined by the externally connected passive elements. The output of the

current error amplifier is compared with the saw tooth wave and produces required gate signals. The IC has totem pole gate driver with internal clamp.

The controller IC has some internal protection circuits such as peak current limiting, over voltage comparator and soft start circuit. The gate drive output is turned off when the peak current limit is reached or in the case of an over voltage condition in the output capacitor voltage. Soft start features provides a safe starting of the circuit by gradually increasing the duty cycle at the initial operation of the circuit.

3.7 Design of the Average Current Controlled PFC

In this section, design procedure for implementing average current mode controlled PFC with UCC3818 IC is presented. First, the design specification for the circuit is defined as given in Table 3.2.

Table 3.2 Design parameters of 250W average current PFC

Output Power, P_0	250 W
Input Voltage, V_{in}	85-270V AC
Input Voltage Frequency	50Hz
Switching Frequency	100 kHz
Output Voltage, V_0	385Vdc
Input current THD	3%
Efficiency	90%
Hold-up time	50ms
Inductor Current Ripple	20%

The design process is realized by using following procedure.

1) Power stage considerations
2) Selection of the switching frequency f_s
3) Selection of the boost inductor L
4) Selection of the output capacitor C_0
5) Selection of the power switch elements, MOSFET and PFC diode
6) Design of the multiplier and feed-forward circuit elements
7) Design of the current loop controller
8) Design of the voltage loop controller

Average current mode controlled PFC with UCC3818 controller IC is implemented with the selected external elements. The schematic diagram of the hardware is shown in Figure 3.29.

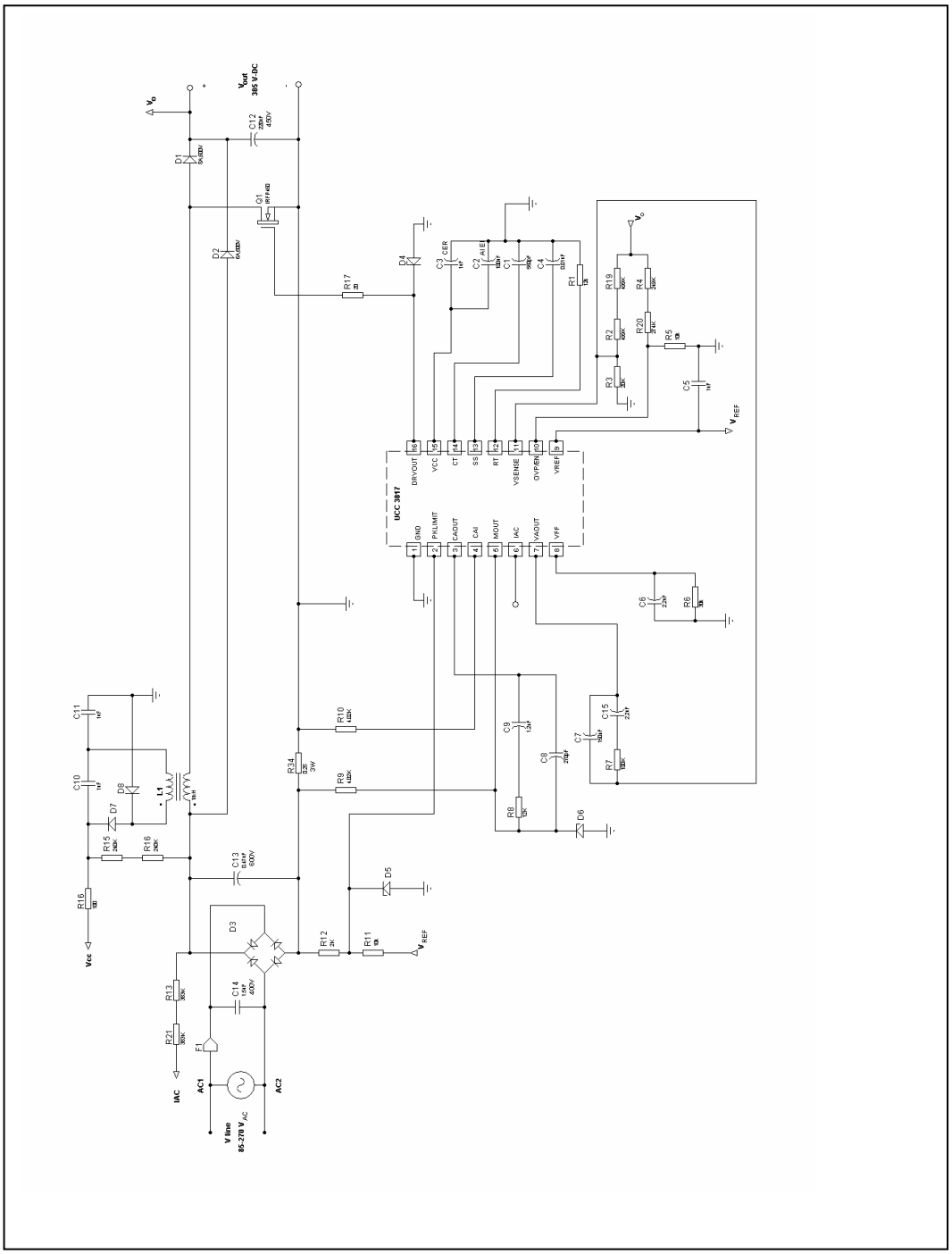


Figure 3.29 Schematic diagram of the 250-W, average current controlled PFC.

1) Power Stage Considerations: A 250-W single-phase power factor correction circuit is implemented and tested in the laboratory conditions. The average current mode control has no limit for the power level of the PFC system. Traditionally, the SMPS has lower power levels that are used in commercial equipments. So, 250-W PFC is a good example to show the basics of the average current mode controlled PFC circuit. The PFC circuit is designed to operate anywhere in the world (universal input line).

The first issue to design the power stage is defining the output voltage level. The output voltage should be greater than the peak of the maximum input voltage. In this example, output voltage reference is selected as 385 Vdc. The main elements of the circuit are boost inductor, power switch, boost diode and output capacitor. The boost inductor is designed for the inductor ripple current at the worst case operation of the circuit. The selection of the power switch is done by considering the rms value of the switch current. The boost diode should have fast reverse recovery characteristics for CCM operation. Both power switch and diode should be rated at about 20 % above of the output voltage. The output capacitor should be selected by considering the output voltage ripple and hold-up time.

2) Selection of the switching frequency f_s: Switching frequency should be high enough to reduce power component size but low enough to reduce the power losses. So selection of the switching frequency is defined by the trade-off between size and switching losses. The controller provides wide range of switching frequency (20 kHz-250 kHz). In this example, 100 kHz switching frequency is selected for better utilization and smaller circuit elements.

3) Selection of the boost inductor L: The boost inductor determines the high frequency ripple for the inductor current. Inductor is designed to handle maximum peak current and defined current ripple. First, the maximum peak current that occurs in operating at minimum input voltage has to be defined. The maximum input peak current $I_{in,peak(max)}$ is ;

$$I_{in,peak(\max)} = \frac{\sqrt{2} \cdot P_0}{\eta \cdot V_{in,rms(\min)}} = \frac{\sqrt{2} \cdot 250W}{0.9 \cdot 85V} = 4.52A \tag{3.28}$$

The peak to peak ripple current is defined as 20% of the maximum input peak current. So the high frequency ripple current is:

$$\Delta I = 0.2 \cdot I_{in,peak(\max)} = 0.9A \tag{3.29}$$

The value of the inductor is selected at the maximum input current and low input voltage with corresponding duty ratio, D.

$$D = \frac{V_0 - V_{in,peak(\min)}}{V_0} = \frac{385 - \sqrt{2} \cdot 85}{385} = 0.69 \tag{3.30}$$

$$L = \frac{V_{in,peak(\min)} \cdot D}{f_s \cdot \Delta I} = \frac{120V \cdot 0.69}{100kHz \cdot 0.9A} = 0.9mH \tag{3.31}$$

where D is the duty cycle, f_s is the switching frequency and ΔI is the inductor current ripple. A 900 μH, ferrite core, high frequency inductor is used with 6-A current handling capacity.

4) Selection of the Output Capacitor C_0: The capacitance and the rated voltage value should be designed according to predefined output voltage, output voltage ripple and hold-up time for the output voltage. Total current through the output capacitor is the rms value of the high frequency ripple current and second harmonic of the line current. The capacitor with voltage and current ratings grater than the normal operating point values with smaller ESR is selected. Hold-up time is the other selection criterion for the selection of the capacitance. Hold-up time is the length of the time where the output voltage remains within the specified range after input voltage is turned off. In this example hold-up time is selected as 20 ms. Calculating the capacitance is done according to the equation (3.32).

$$C_0 = \frac{2 \cdot P_0 \cdot \Delta t}{(V_0^2 - V_{0,\min}^2)} = \frac{2 \cdot 250W \cdot 20ms}{385^2 - 320^2} = 200\mu F \tag{3.32}$$

where ΔI is the hold-up time. 220-μF, 450-V electrolytic capacitor with lower ESR is chosen for 385-V output voltage and 250-W output power.

5) Selection of the power switches elements, MOSFET and PFC diode: The selection of the switch elements, power switch and boost diode, depends on the voltage and current ratings, and switching losses. The power switch and diode should have sufficient operation ratings. Power losses should be considered while selecting power switch. Total power loss is the sum of the switching loss and conduction loss. Choosing a switch with minimum gate charge and switch capacitance reduces the turn-on and turn-off losses. A small on-resistance will reduce the conduction losses. A power MOSFET with current rating higher than the maximum peak current of the inductor and voltage rating greater than the output voltage is chosen as power switch. The power MOSFET, IRFP460 is used in experimental circuits. The fast recovery boost diode, DSEI 12-06A is chosen as the boost diode with 35 ns reverse recovery time.

6) Design of the multiplier and feed-forward circuit elements: Multiplier is the core of the average current mode control of PFC. The output of the multiplier defines the reference for the input current and it is input for the current compensator. So the multiplier should be designed properly. There are three inputs for the multiplier. These are voltage error amplifier output (V_{AOUT}), waveform reference for the input current (I_{AC}) and input voltage feed-forward (V_{FF}). The equation for the multiplier output (I_{MOUT}) can be written considering the multiplier concept explained in sections 3.1 to 3.3 as:

$$I_{MOUT} = I_{AC} \frac{(V_{AOUT} - 1)}{K \cdot V_{FF}^2} \tag{3.33}$$

where K is the multiplier constant and equal to 1/V. The I_{AC} signal is obtained by a

simple resistor divider circuit through rectified ac line. The maximum input current for the I_{AC} pin of the UCC3818 is defined as 500 μA in the datasheet. A 750-kohm resistor provides enough current for the maximum input voltage conditions (265 Vrms).

The feed-forward action is achieved by using the mirrored current signal and a single-pole filter as shown in Figure 3.30. Feed-forward ensures that the control circuit will not be affected by the input voltage variations.

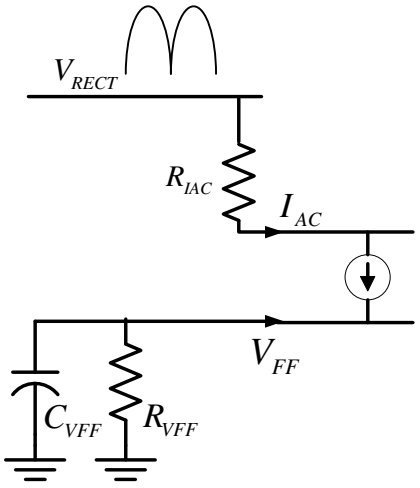


Figure 3.30 Feed-forward circuit for the UCC3818 IC.

The feed-forward resistor (R_{VFF}) can be calculated using the following equation:

$$R_{VFF} = \frac{1.4V}{\frac{V_{in,\min(rms)} \cdot 0.9}{2 \cdot R_{IAC}}} = 30k\Omega \tag{3.34}$$

where R_{IAC} is equal to the total resistance connected between the I_{AC} pin and rectified line voltage. The feed-forward capacitor is designed according to the filter requirements for the controller. The feed-forwards signal contains second harmonic ripple and this ripple distorts the current reference. The low-pass filter is designed for the amount of the attenuation needs to be determined. In the design specifications, the input current THD is determined as 3%. 1.5% of this distortion is allowed for the

feed-forward circuit. 0.75% is left for the output voltage controller and 0.75% for other distortion sources such as noise, parasitic elements etc… It is known that the rectified line voltage is a 100-Hz signal and it will consist of 66.2% second harmonic in the averaged value. So the needed attenuation is equal to (1.5%)/(66.2%) or 0.022. The desired gain at the second harmonic frequency (100 Hz) is 0.022. The filter pole is placed at the crossover of the low-pass filter where the gain of the filter is equal to unity. The pole filter can be determined by using the following linear equation:

$$f_P = 100 \cdot \frac{0.022}{1} = 2.2Hz \tag{3.35}$$

The corresponding filter capacitance at the pole frequency can be calculated by:

$$C_{VFF} = \frac{1}{2 \cdot \pi \cdot R_{VFF} \cdot f_P} = 2.6\mu F \tag{3.36}$$

7) Design of the current loop controller: The theoretical derivations for the current loop controller for the average current mode control are explained in the section 3.4.1. It was shown that, the inner current loop has higher bandwidth around one decade of the switching frequency. It was evaluated that, the open loop transfer function for the current loop is:

$$T_i(s) = G_{id}(s) G_C(s) \tag{3.37}$$

where $G_{id(s)}$ is equal to the power stage transfer function and $G_{C(S)}$ is equal to the current compensator transfer function. The current compensator has two poles and one zero characteristics. The transfer functions for the power stage and current compensator are given as:

$$G_{id}(s) = \frac{V_0 \cdot R_s}{s \cdot L \cdot V_{SE}} \tag{3.38}$$

$$G_C(s) = \frac{\omega_i}{s} \frac{(1 + s/\omega_z)}{(1 + s/\omega_p)} \tag{3.39}$$

The pole and zero frequencies are determined by first selecting the crossover frequency for the current compensator. One decade of the switching frequency (10 kHz) is selected as crossover frequency. It is known that open-loop transfer function of the current loop has unity gain at crossover. The gain for the power stage is at the crossover:

$$\left|G_{id}(10kHz)\right| = \frac{V_0 \cdot R_s}{s \cdot L \cdot V_{SE}} = \frac{385V \cdot 0.25\Omega}{10kHz \cdot 1mH \cdot 4V} = 0.383 \tag{3.40}$$

where V_{SE} is equal to peak-to-peak ramp voltage amplitude and 4 V for UCC3818, R_S is the sensing resistor and equal to 0.25 ohm. The current compensator gain at the crossover frequency is:

$$\left|G_C(10kHz)\right| = \frac{1}{0.383} = 2.611 \tag{3.41}$$

This gain at the crossover frequency determines the resistor value R_f for the current compensator, which is calculated as 12 kΩ. The zero of the compensator is placed at the crossover frequency and calculated by:

$$C_Z = \frac{1}{2 \cdot \pi \cdot R_f \cdot f_c} = \frac{1}{2 \cdot \pi \cdot 12k\Omega \cdot 10kHz} = 1.3nF \tag{3.42}$$

The pole is placed at half of the switching frequency to filter high frequency noises.

$$C_P = \frac{1}{2 \cdot \pi \cdot R_f \cdot \frac{f_s}{2}} = \frac{1}{2 \cdot \pi \cdot 12k\Omega \cdot 50kHz} = 265pF \tag{3.43}$$

8) Design of the voltage loop controller: The output voltage compensator has limited bandwidth to attenuate the second harmonic ripple in the feedback path. A two-pole and one-zero compensator system is used as voltage compensator as shown in Figure 3.31. The input for the voltage amplifier is compared with the constant reference value, 7.5 V for the UCC3818 IC. The ratio for the output voltage divider should be selected to divide the output voltage to this reference voltage (7.5 V).

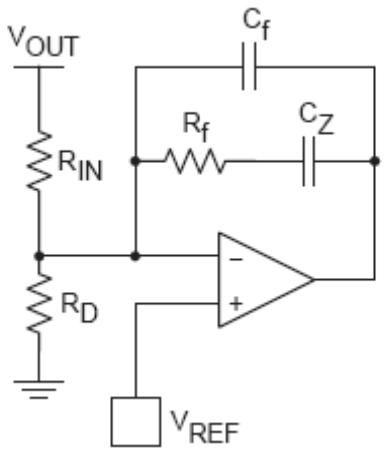


Figure 3.31 Output voltage compensator configuration.

The gain of the error amplifier is defined by the second harmonic ripple in the output voltage. The peak ripple for the output voltage is equal to 4 V. The distortion budget in the current for the voltage controller is defined as 0.75%. We know that 0.75% 3rd harmonic distortion in the input current is the result of the 1.5% 2nd harmonic ripple in the output of the error amplifier. So the allowable ripple in the output of the voltage amplifier can be calculated as:

$$\left|G_V\right| = \frac{0.015 \cdot \Delta V_{VAOUT}}{V_{o,RIPPLE(peak-peak)}} = \frac{0.015 \cdot 5V}{8V} = 7.5 \tag{3.44}$$

where ΔV_{VAOUT} is equal to effective output voltage range of the voltage amplifier for UCC3818. The value of the C_f is determined by:

$$C_f = \frac{1}{2 \cdot \pi \cdot 100Hz \cdot |G_V| \cdot R_{IN}} = 210nF \tag{3.45}$$

The crossover frequency f_{vi} for the voltage loop is selected as 10 Hz and the pole is placed at the crossover frequency. The pole frequency is defined by the resistor R_f and found by:

$$R_f = \frac{1}{2 \cdot \pi \cdot f_{vi} \cdot C_f} = 84k\Omega \tag{3.46}$$

The capacitor C_z is added for the stability of the voltage loop. Since the power circuit has single pole characteristic, this zero improves the phase margin of the voltage loop. Considering that a zero behaves like a pole in a closed loop system, this zero should be placed before the crossover frequency for a good dynamic response. The zero frequency is selected as one decade of the crossover frequency and the value for C_z is found as:

$$C_z = \frac{1}{2 \cdot \pi \cdot \frac{f_{vi}}{10} \cdot R_f} = 2.1\mu F \tag{3.47}$$

3.8 Experimental Results

Average current mode PFC circuit PCB is designed and experimental results are verified in the laboratory. The PCB layout of the circuit is shown in Figure 3.32.

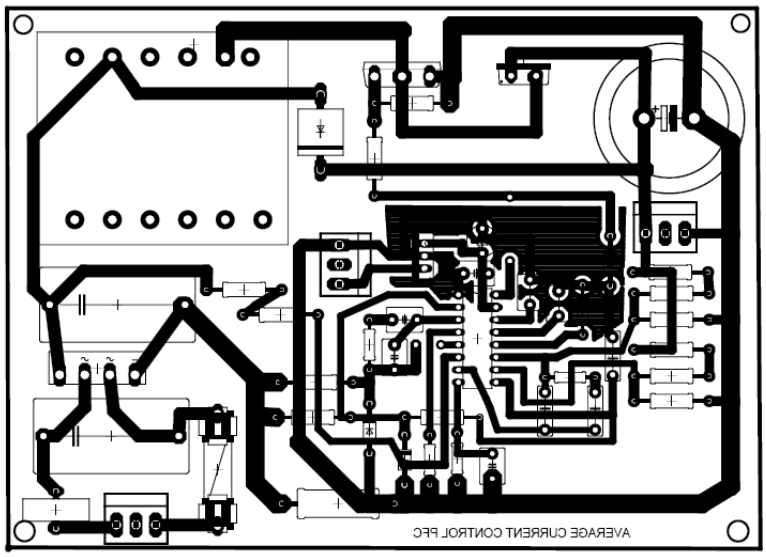


Figure 3.32 PCB layout of the average current mode PFC circuit.

The circuit is supplied with an isolated variac circuit and loaded by a resistive load. First, the circuit is supplied by 220-Vac input voltage and corresponding input current and voltage waveforms are illustrated. The input voltage and input current waveforms are shown in Figures 3.33.a and 3.33.b, respectively. The corresponding harmonic content of the input current is shown Figure 3.33. Input current has some 5^{th} order harmonic due to the input voltage harmonics.

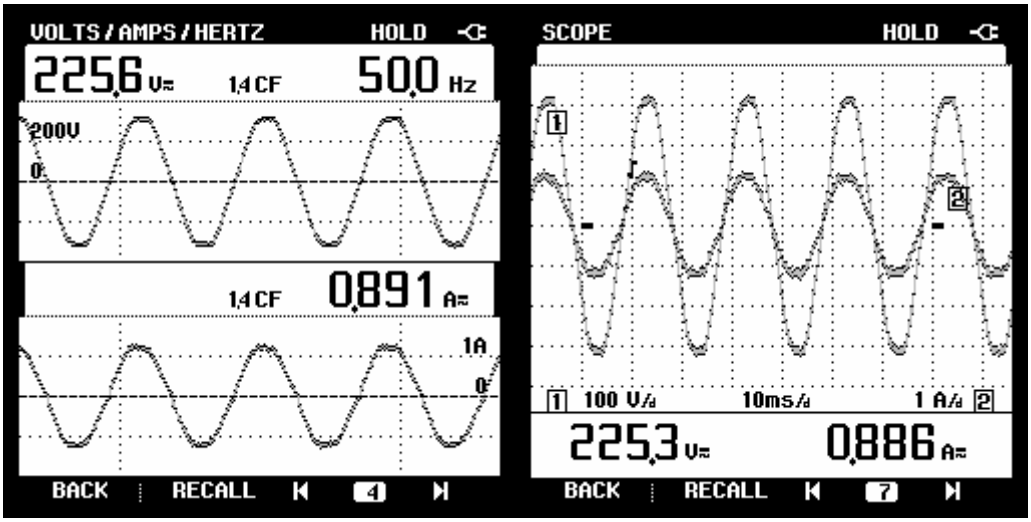


Figure 3.33 Input voltage and input current waveforms (Scales: 100V/div, 1A/div).

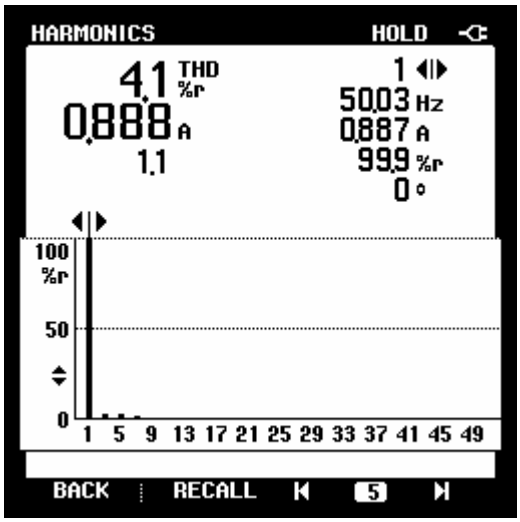


Figure 3.34 Input current harmonic spectrum.

The output voltage and input current harmonic waveforms are illustrated in Figure 3.35. The output voltage has the reference value voltage rating (385 Vdc).

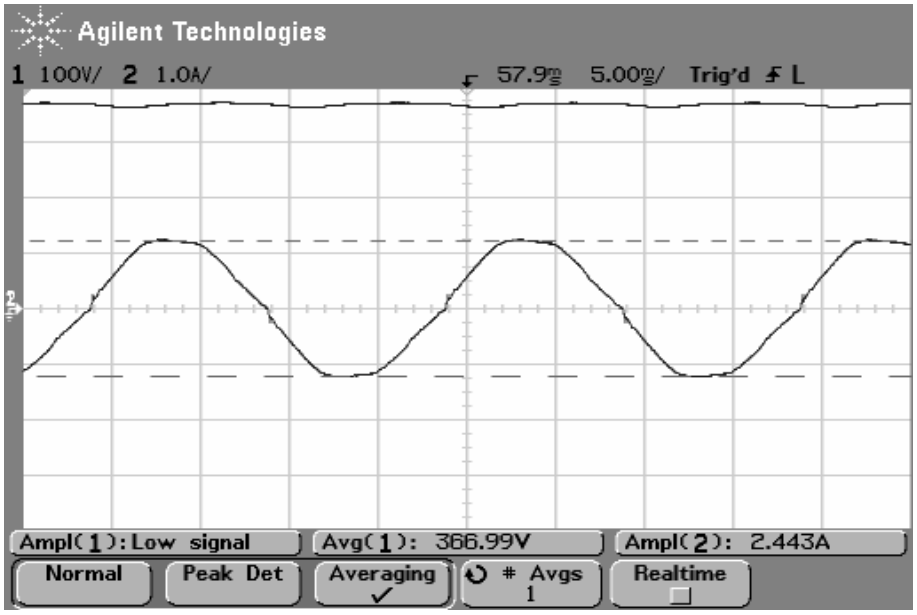


Figure 3.35 Output voltage and input current waveform (Scales: 100V/div, 1A/div).

The input current has some distortions at the zero crossings of the line voltage due to the insufficient inductor voltage to follow the reference current. The distortion in the

line current around the zero crossings of the line voltage is illustrated in Figure 3.36.

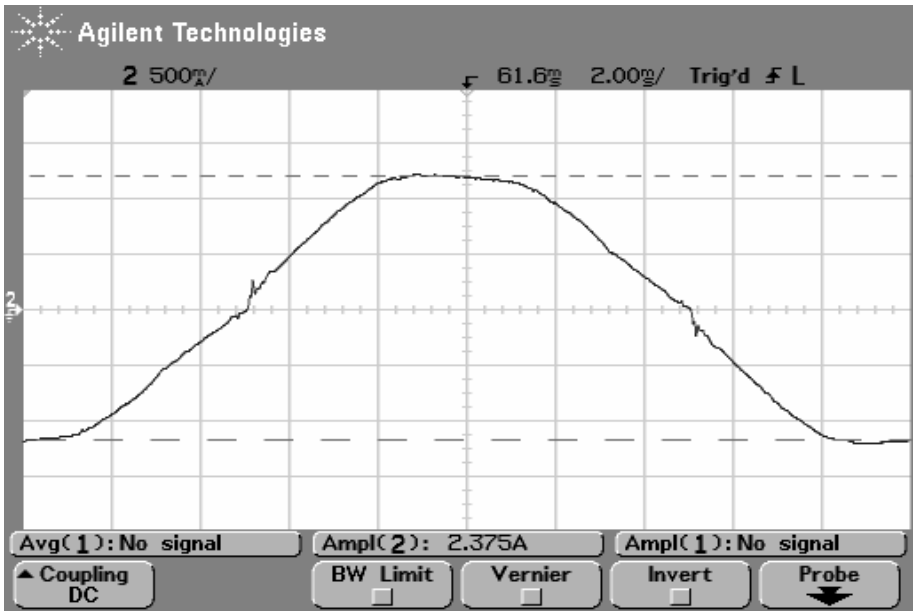


Figure 3.36 Input current distortions around zero crossings (Scale: 0.5A/div).

The input voltage is changed to 120 Vac and corresponding waveforms are illustrated. The input voltage and input current waveforms are shown in Figures 3.37.a and 3.37.b, respectively. The corresponding harmonic content of the input current is shown in Figure 3.38.

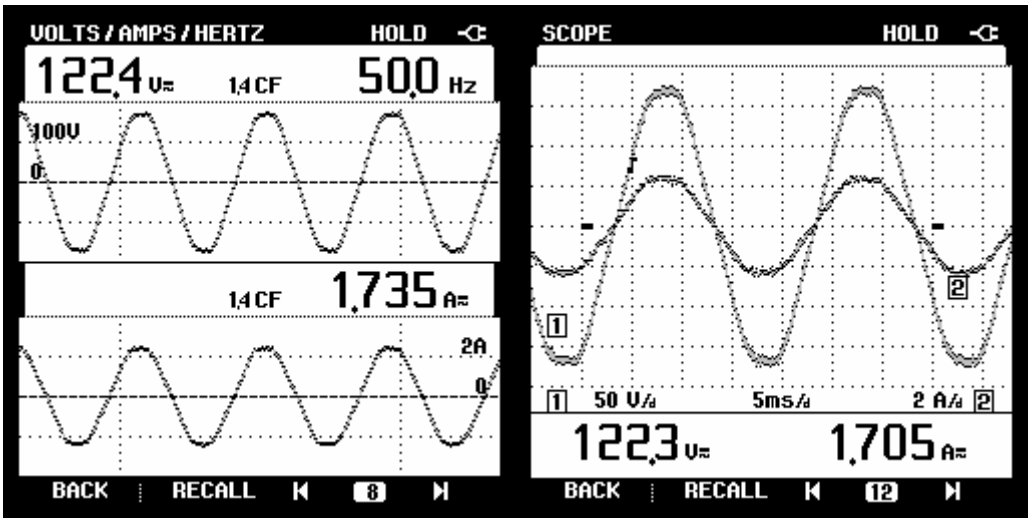


Figure 3.37 Input voltage and input current waveforms (Scales: 50V/div, 1A/div).

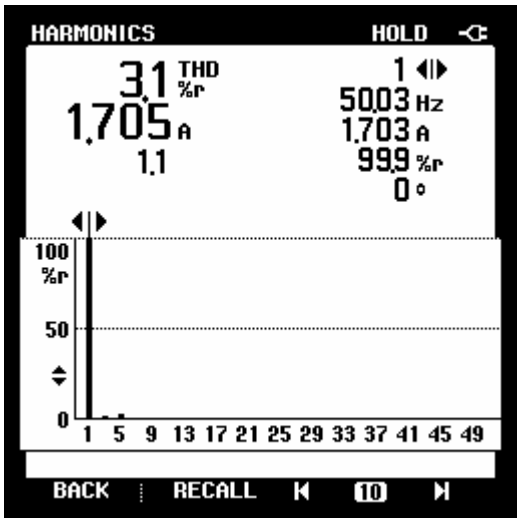


Figure 3.38 Input current harmonic spectrum.

The output voltage ripple waveforms are illustrated in Figure 3.39. The output voltage has the reference value voltage rating (385Vdc). The input current has some distortions at the zero crossings of the line voltage due to insufficient inductor voltage to follow the reference current. The distortion in the line current around the zero crossings of the line voltage is illustrated in Figure 3.40.

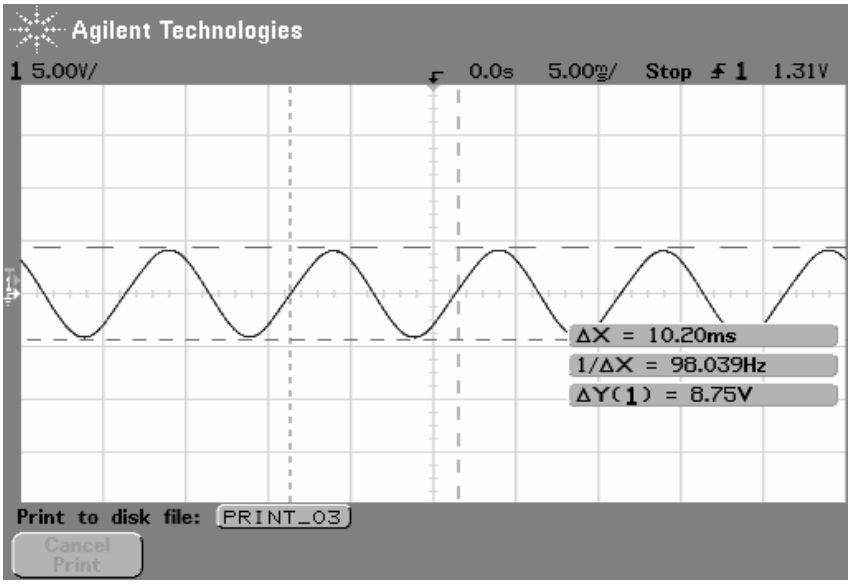


Figure 3.39 Output voltage ripple waveform (Scales: 5V/div, AC coupling).

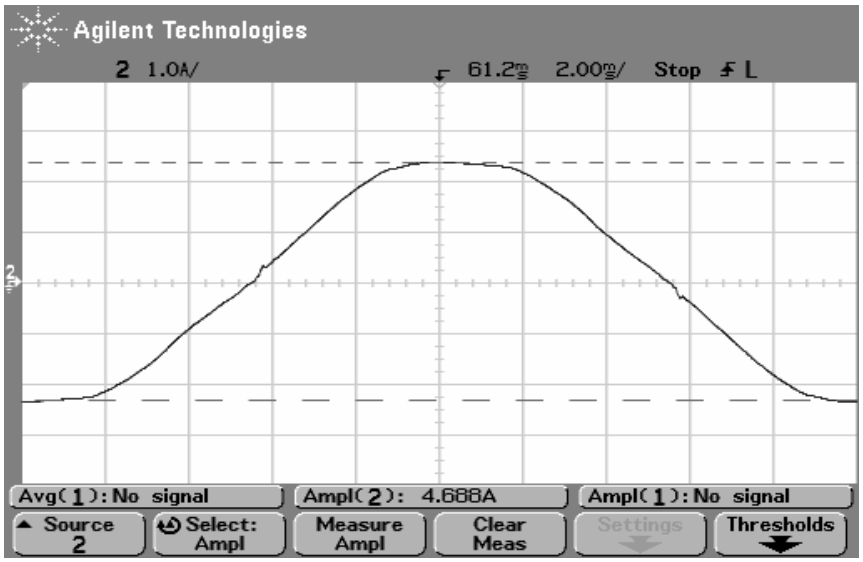


Figure 3.40 Input current distortions around zero crossings (Scale: 1A/div).

Start-up response for the input current and the input voltage is verified. Due to the soft-start structure of the control circuit output voltage reaches the steady-state operation after a few line cycles. The input current has inrush current at start-up but the circuit has the ability to alter this start-up current without damaging any of the circuit elements. The start-up response of the circuit is illustrated in Figure 3.41.

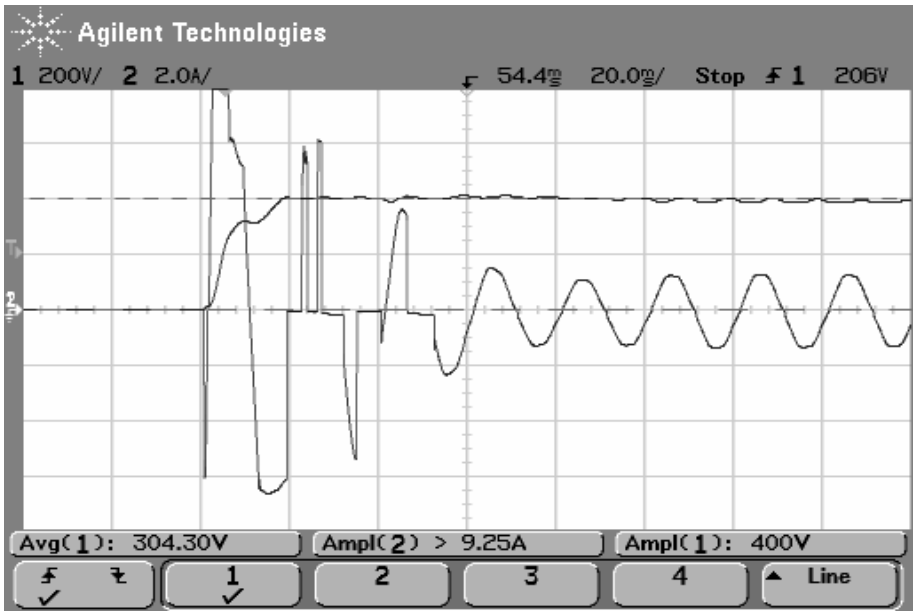


Figure 3.41 Start-up behavior of the input current and output voltage (Scales: 200V/div, 2A/div).

3.8 Conclusions

The average current mode control PFC circuit is analyzed theoretically and simulation and experimental results are verified. It is shown that the average current mode control seems attractive for active power factor correction circuit. However, there is too much design procedure making the system complex. Also the number of elements used in the circuit is high. In the following chapters, another active PFC control method will be analyzed and verified experimentally.

CHAPTER 4

CRITICAL CONDUCTION MODE CONTROL OF PFC

4.1 Introduction

In this chapter, the analysis of single-phase active power factor correction circuit operated in the critical conduction mode is presented. The critical conduction mode is also called as boundary conduction mode or transition mode control. The word "boundary" comes from the operation characteristics of the proposed control method. In the boundary conduction mode control (BCM), the inductor current operates at the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

Critical conduction mode operation is the most popular solution for the low power applications due to the following reasons:

- The control topology needs few external components and serves simple design process
- Low cost solution to achieve near unity power factor application
- Smaller magnetic element sizes due to the CCM operation
- Lower switching losses and stress on the power switch elements in the application. The power switch turns-on at zero current and the reverse recovery loss of the boost diode is minimized.

However, the switching frequency of the boundary conduction mode is not constant and varies over a line cycle. The switching frequency at the zero crossing of the line

is higher in contrary, lower in the peak of the line cycle. So this large switching frequency variation causes distortions in the input current. Because the inductor current peak value is twice of the input current peak value, boundary conduction mode is not suitable for high power applications.

This chapter describes the basics of a PFC boost converter operating at the critical conduction mode. Operation principle and derivation of circuit parameters are discussed. Steady-state characteristics, switching frequency derivation, input and inductor current properties are explained throughout the chapter. Simulation and experimental results are verified and compared.

4.2 Operation of Critical Conduction Mode

PFC boost converter such as in average current mode control is used to analyze the basics of the critical conduction mode. A typical critical conduction mode control is illustrated in Figure 4.1.

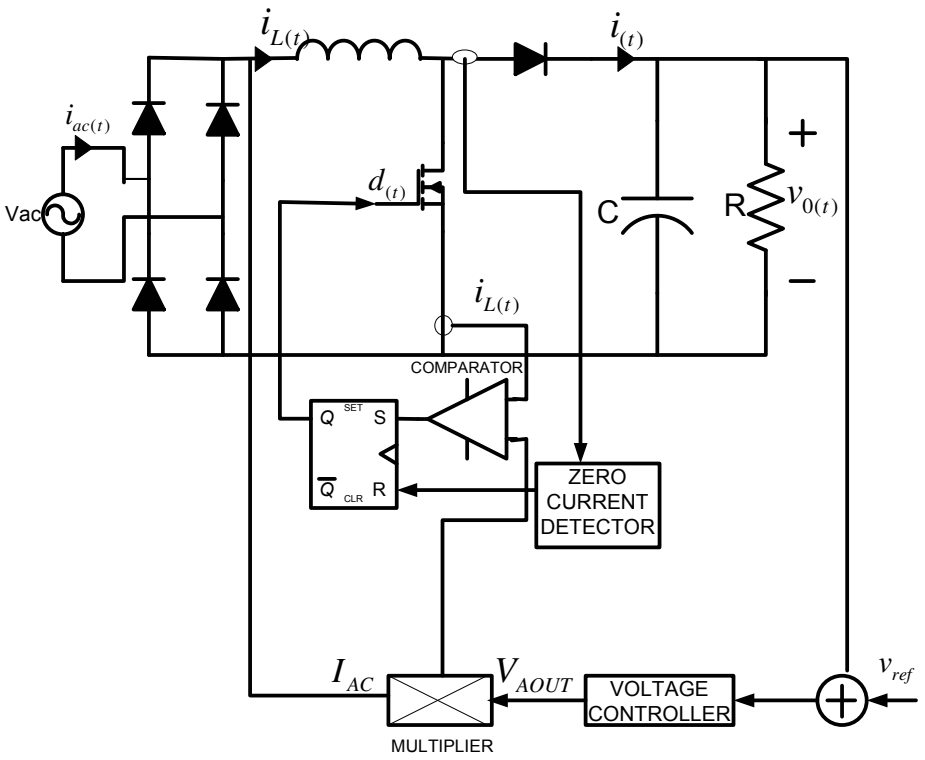


Figure 4.1 Block diagram of a BCM boost converter.

The reference current is obtained by the same method as in the average current mode control scheme. The sensed sinusoidal waveform is multiplied with the output of the voltage error amplifier and required current reference is built. The switch current is sensed. The power switch is turned on when the inductor current drops to zero. The power switch is turned off when the inductor current reaches the reference current. Thus inductor current has a triangular waveshape with a sinusoidal envelope. An input filter capacitor is used to average the triangular waveshape thus providing a sinusoidal input current. The resulting waveforms of inductor current $I_{L,}$ averaged input current I_{AC} and reference current I_{REF} are shown for a half line cycle in Figure 4.2.

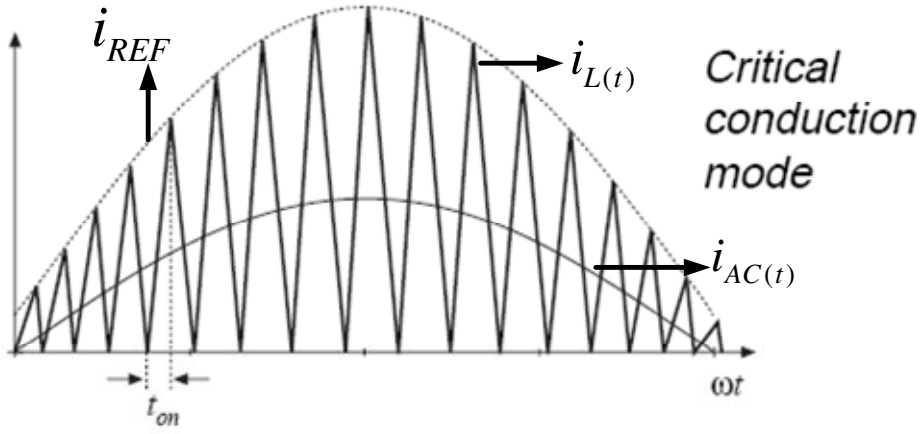


Figure 4.2 Current waveforms during half of an AC line cycle.

In critical conduction mode, boost converter operates in two modes. The inductor current builds up linearly with the slope (V_{in}/L) during on time. Theoretically, the on-time duration of the power switch is constant. However, due to finite switching frequency, the switch on time varies throughout the entire cycle. Second mode begins with the turning-off of the power switch. The inductor current decreases linearly with the slope (V_0 - V_{in} / L). This switching sequence repeats at every zero crossing of the inductor current. So the inductor current is zero when the switch is turned on. This provides a zero current turn-on, hence minimizes the switching losses. These conduction modes are illustrated in Figure 4.3.

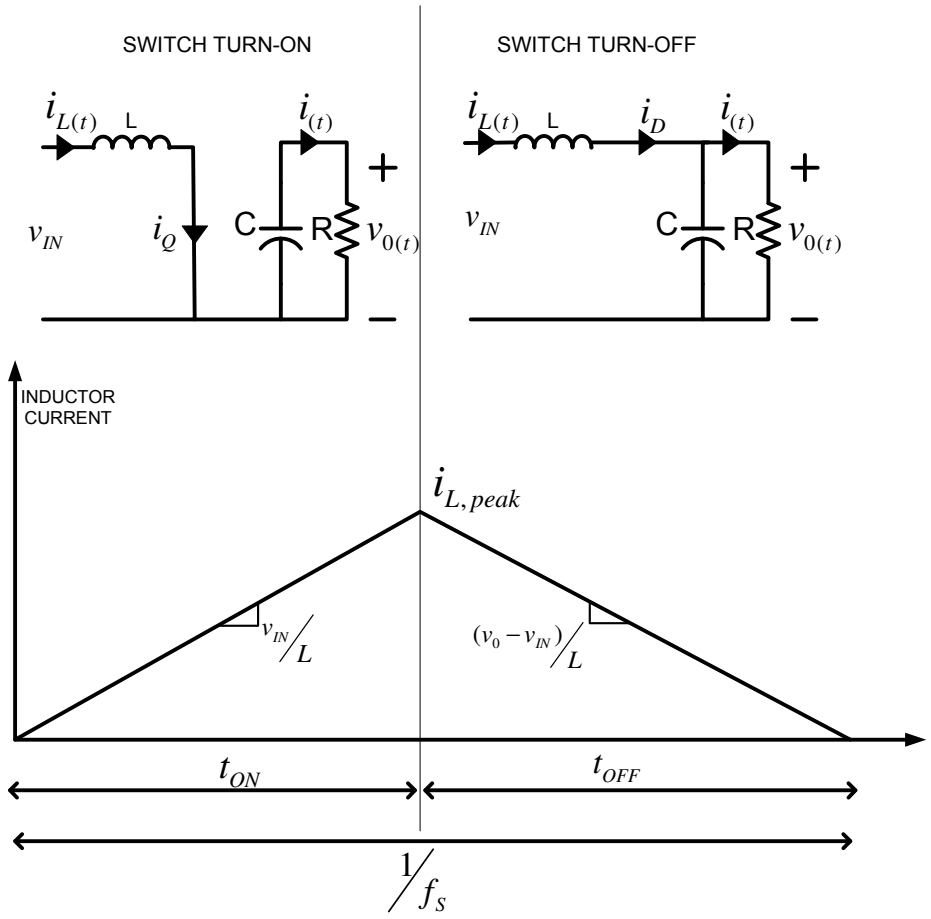


Figure 4.3 Switching sequences of PFC Stage.

The critical conduction mode control eliminates the inner current controller. A simple on-off control with a zero current detector block is enough to implement a boundary conduction mode control. In addition only switch current is sensed.

As a result, the inductor peak current is twice of the line peak current at the boundary conduction mode. This control topology requires smaller boost inductor but requires input filtering capacitor to smooth the current and minimize the EMI. Design procedure is simple and low cost. It is suitable for low power applications due to higher peak currents and variable switching frequency.

4.3 Analysis of Switching Characteristics

In this section, steady-state characteristics, switching-on and -off time, duty cycle, switching frequency and their dependency on ac input voltage and power level are discussed. The BCM boost converter operates as a power factor pre-regulator so the input voltage and input current of the system have sinusoidal waveform without any displacement. Thus the sinusoidal equations for the input voltage $V_{in}(t)$ and input current $I_{in}(t)$ can be expressed as follows:

$$v_{in}(t) = \sqrt{2} \cdot V_{in,rms} \cdot \sin(\omega t) \tag{4.1}$$

And

$$i_{in}(t) = \sqrt{2} \cdot I_{in,rms} \cdot \sin(\omega t) \tag{4.2}$$

The operation of the BCM control is explained in section 4.2. Actual and averaged inductor currents with corresponding gate signals are illustrated in Figure 4.4.

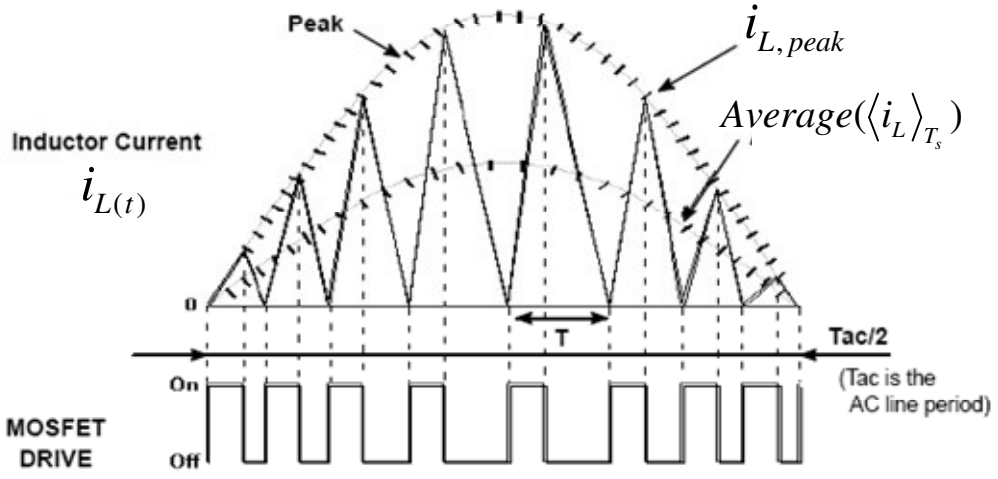


Figure 4.4 Inductor Current and Corresponding Gate Signals.

The input current I_{in} is equal to the averaged inductor current I_L that is half of the peak value of the inductor current $I_{L,peak}$.

$$i_{in}(t) = \langle i_L \rangle_{Ts} = \frac{i_{L,peak}}{2} \tag{4.3}$$

where T_s is the switching period. So peak inductor current can be written by using equation (4.2) as:

$$i_{L,peak} = 2 \cdot \sqrt{2} \cdot I_{in,rms} \cdot \sin(\omega t) \tag{4.4}$$

The basic input power definition can be used for the derivation of the peak inductor current. The averaged input power is equal to the product of the rms values of the input voltage and current. Averaged input power can be expressed as

$$\langle P_{in} \rangle_{T_S} = V_{in,rms} \cdot I_{in,rms} \tag{4.5}$$

Peak inductor current is a function of averaged power and rms value of input voltage.

$$i_{L,peak} = 2 \cdot \sqrt{2} \cdot \frac{\langle P_{in} \rangle}{V_{in,rms}} \cdot \sin(\omega t) \tag{4.6}$$

The BCM converter operates with variable switching frequency as illustrated in Figure 4.3. As already stated, the inductor current consists of two phases. During the on time of the power switch, the inductor voltage is equal to the input voltage and inductor current increases with a V_{in}/L slope. The inductor current in the on time can be expressed as:

$$i_L(t) = \frac{v_{in}(t)}{L} \cdot t \tag{4.7}$$

At the end of the on-time duration, the inductor current I_L is equal to the peak

inductor current $I_{L,peak}$. Thus

$$i_{L,peak} = \frac{v_{in}(t)}{L} \cdot t_{on} \tag{4.8}$$

The on time is then expressed by using equation (4.1) and (4.6) as:

$$t_{on} = \frac{i_{L,peak} \cdot L}{v_{in}(t)} = \frac{2 \cdot \sqrt{2} \cdot \frac{\langle P_{in} \rangle}{V_{in,rms}} \cdot \sin(\omega t) \cdot L}{\sqrt{2} \cdot V_{in,rms} \cdot \sin(\omega t)} = \frac{2 \cdot \langle P_{in} \rangle \cdot L}{V^2_{in,rms}} \tag{4.9}$$

It is clear from equation (4.9) that, the on time t_{on} is constant during line cycle. The on-time duration depends on power level, inductance and input rms voltage. The off-time duration can be explained by using the second phase of the inductor current. During this second phase, inductor current flows through the output diode and feeds the output capacitor and load. The inductor voltage becomes negative and inductor current decreases with a linear $(V_0 - V_{in})/L$ slope. The inductor current is equal to the peak value at the beginning of the off-time duration and drops to zero at the end of this second phase. The variation in the inductor current in the second phase can be written as:

$$i_L(t) = i_{L,peak} - \left(\frac{v_0 - v_{in}(t)}{L} \cdot t \right) \tag{4.10}$$

This second phase ends when the inductor current reaches zero, and the off time is given by the following equation:

$$t_{off} = \frac{i_{L,peak} \cdot L}{v_0 - v_{in}(t)} = \frac{2 \cdot \sqrt{2} \cdot \frac{\langle P_{in} \rangle}{V_{in,rms}} \cdot \sin(\omega t) \cdot L}{v_0 - \sqrt{2} \cdot V_{in,rms} \cdot \sin(\omega t)} \tag{4.11}$$

Off-time duration is not constant and varies during each half cycle. Total switching period is the sum of t_{on} and t_{off}. Thus

$$T_S = t_{on} + t_{off} = i_{L,peak} \cdot L \cdot \frac{v_0}{v_{in}(t)(v_0 - v_{in}(t))} \tag{4.12}$$

The equation for the switching period T_S can be expressed by using equation (4.1) and (4.6) as:

$$T_S = 2 \cdot L \cdot \frac{\langle P_{in} \rangle \cdot v_0}{V^2_{in,rms}(v_0 - v_{in}(t))} \tag{4.13}$$

Thus the switching frequency f_s is the inverse of the switching period T_S. Consequently,

$$f_S = \frac{V^2_{in,rms}}{2 \cdot L \cdot \langle P_{in} \rangle} \left(1 - \frac{\sqrt{2} \cdot V_{in,rms} \cdot \sin(\omega t)}{v_0} \right) \tag{4.14}$$

This equation shows that, the switching frequency consists of a constant component that has a value dependent on the operating point and a variable component that makes the switching frequency vary within AC line cycle. The following figure illustrates the variations of the switching frequency within a half AC line cycle.

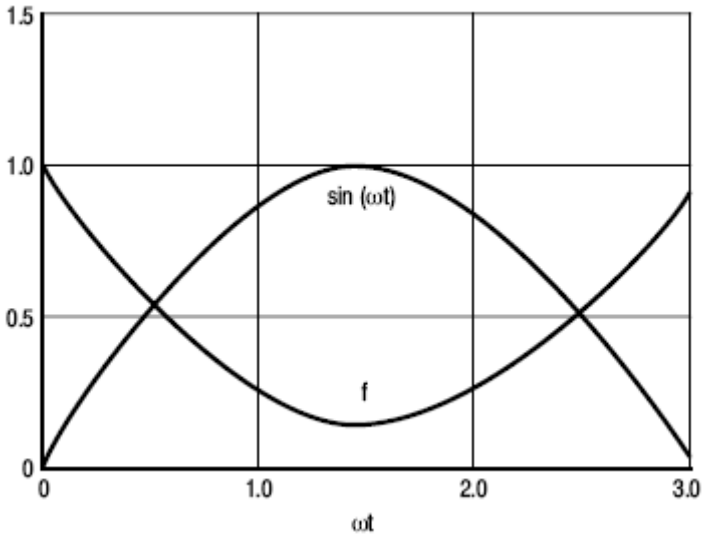


Figure 4.5 Switching frequency over the AC line cycle.

The switching frequency is high near the zero crossings of the line cycle where the inductor current has lower amplitude. Besides, the switching frequency is approximately divided by five at the top of the sinusoid, where the inductor current has higher amplitude. In actual implementation, the rectified input voltage is filtered with a high frequency AC capacitor to provide a clean reference waveform. The output voltage error amplifier determines the amplitude of the current reference. The turn-on time is controlled by the comparison of the reference and the actual inductor current. The power switch is turned on when the actual inductor current drops to zero and turned off when actual inductor current reaches the reference. In the next section, computer simulation analysis of a BCM converter will be verified.

4.4 Simulation of Boundary Conduction Mode PFC

Single-phase critical conduction mode controlled PFC circuit is simulated by SIMPLORER simulation tool and simulation results are verified. The simulated circuit and control blocks are shown in Figure 4.6.

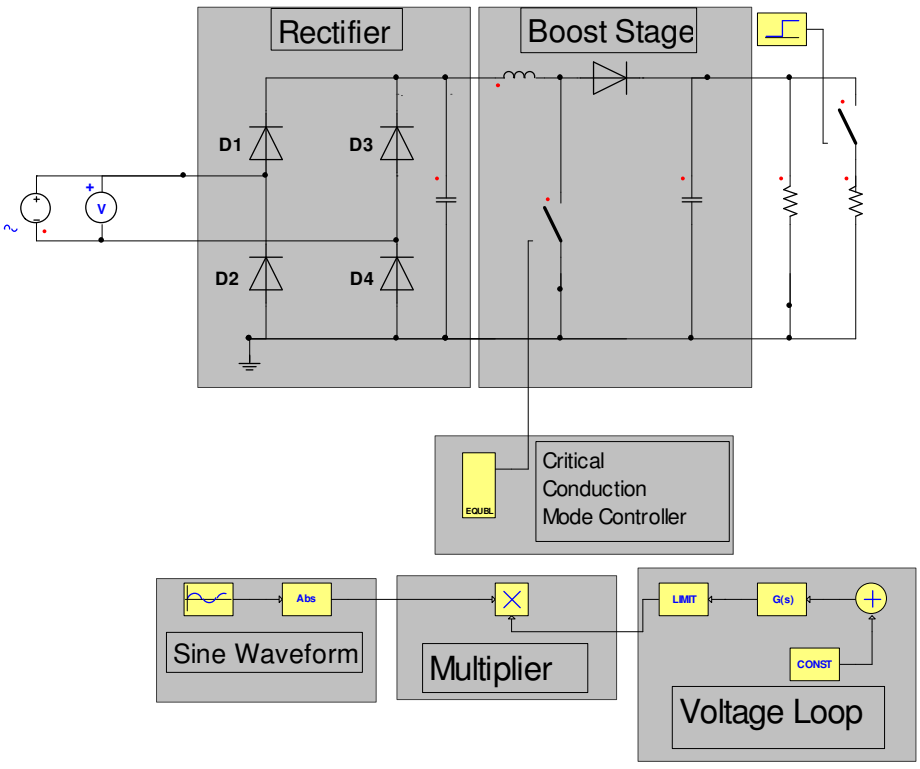


Figure 4.6 Block diagram of simulation circuit.

Computer simulation of critical conduction mode control is used for the analysis of circuit parameters and waveforms at different operating points. The input current, inductor current, switching signals and output voltage waveforms are illustrated and analyzed. The current waveform behavior for different input voltages and the output voltage differences at step load conditions are verified. The circuit is simulated with the following simulation parameters given in Table 4.1.

Table 4.1 Simulation parameters of critical conduction mode PFC

Output Power, P_0	150 W
Input Voltage, V_{in}	90-265V
Input Voltage Frequency	50Hz
Switching Frequency	Variable
Output Voltage, V_0	400V
Boost Inductor, L	0.8mH
Output Capacitor, C_0	330uF
Integration Formula	Euler
Minimum Step Time	0.1u

The output voltage controller is a low bandwidth voltage error amplifier that is built with s-transfer function block in the simulation tool. The crossover frequency of the voltage controller is chosen as 20 Hz. A 400-V reference voltage is used in the comparator at the input of the voltage error amplifier. There is no inner current controller in the critical conduction mode control. Simply an on-off control is applied in the simulation tool. Inductor current is compared with the switch current. The control algorithm for this type of control is realized by using equation block tool in the simulation. The voltage controller s-transfer function block (GS1) and current control equation block (EQUBL1) are shown in Figure 4.7.

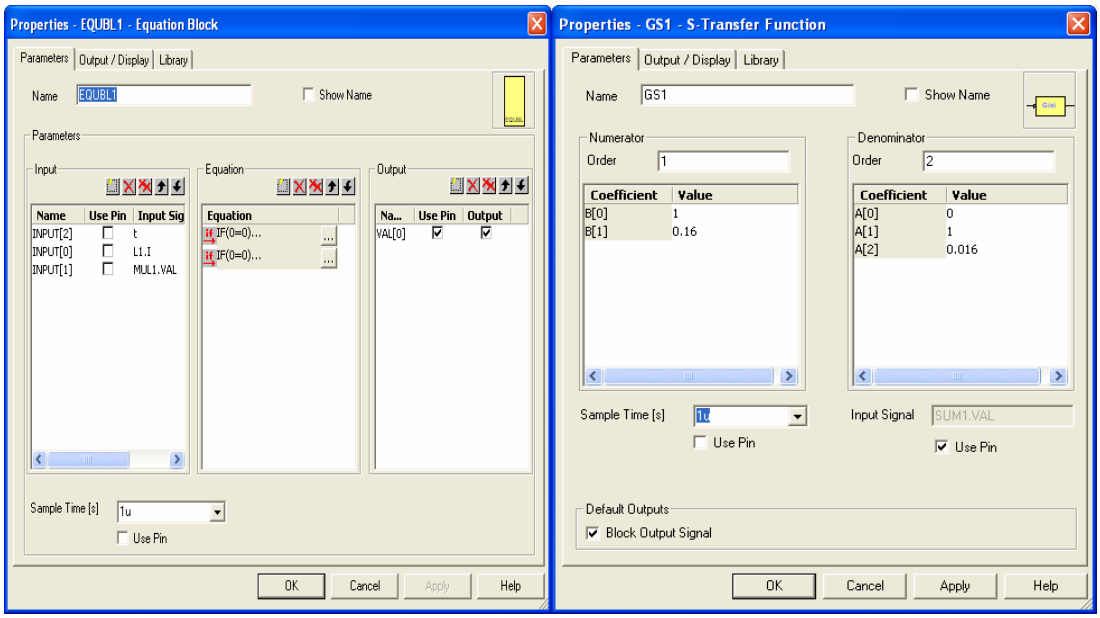


Figure 4.7 Voltage controller s-transfer function and current controller equation block.

The circuit is simulated for 220 Vac input voltage and 150 W output power. The input voltage, and generated inductor current reference and the actual inductor current waveforms are illustrated in Figure 4.8. The corresponding input current is shown in Figure 4.9.

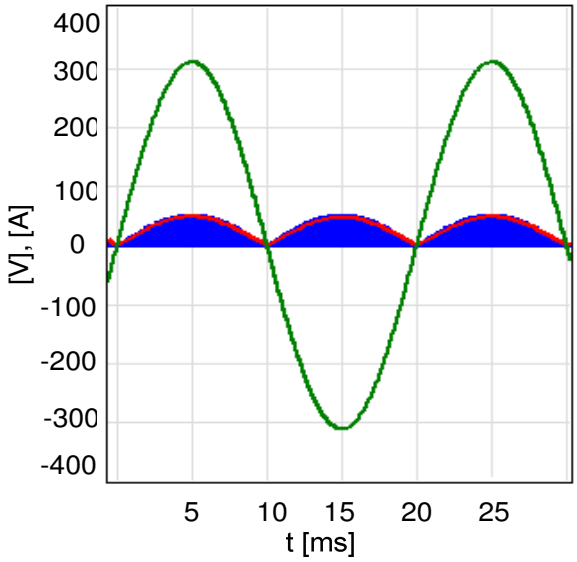


Figure 4.8 Line voltage, reference inductor current and actual inductor current simulation waveforms for 220 V input voltage at 150 W PFC (current scale: 40x).

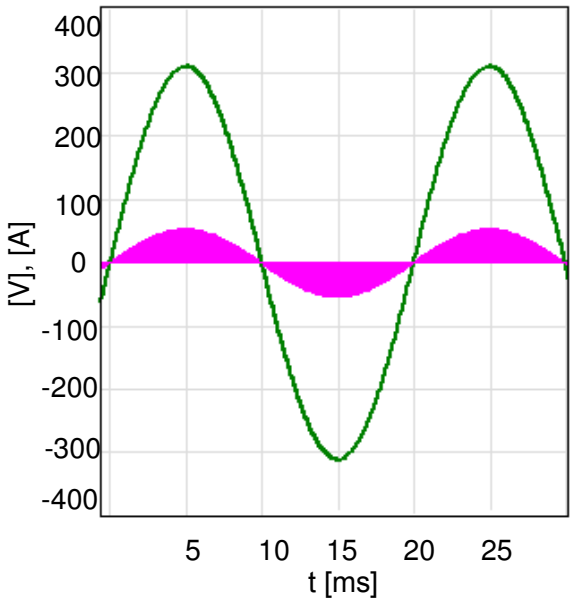


Figure 4.9 Line voltage and input current simulation waveforms for 220 V input voltage at 150 W PFC system (current scale: 40x).

The output voltage reference is set to 400 Vdc level. The output voltage waveform at steady state with the input current is illustrated in Figure 4.10.

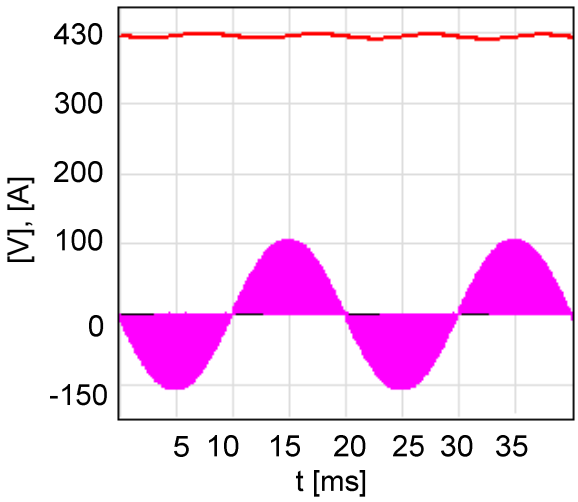


Figure 4.10 Output voltage and input current simulation waveforms for 220 V input voltage at 150 W PFC system (current scale: 100x).

The transient response for the output voltage at the start-up and step load response are verified in the simulation. The load is increased at steady state and corresponding output voltage waveform is illustrated in Figure 4.11.

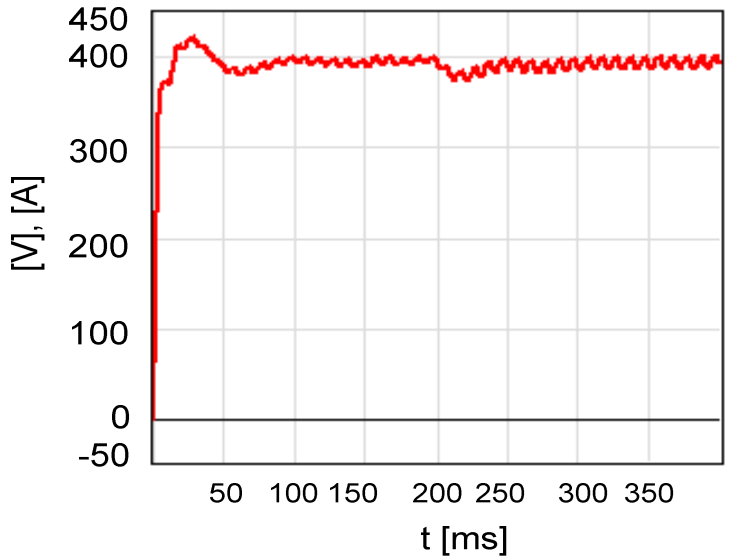


Figure 4.11 Transient response for output voltage simulation waveforms for 220 V input voltage at start-up and half-load to full-load step.

4.5 Hardware Implementation of Boundary Conduction Mode PFC

In this section, the implementation of the borderline control with PFC controller IC is explained. The analog PFC controller IC, MC34262, is chosen to implement critical conduction mode PFC application. General specifications of the power circuit and control circuit elements of an boundary conduction mode power factor correction system is derived. The single-phase PFC is shaped from a single-phase diode rectifier and a cascaded dc-dc boost converter. The types of the components in the power circuit with their general specifications are summarized briefly in subsection 4.4.1. The general parameters and the block diagram of the controller are given in subsection 4.4.2.

4.5.1 Functional Description of the Power Circuit

Single-phase bridge rectifier with a cascaded boost converter is built and critical conduction mode control is applied. The load is chosen as a resistive load. Input is supplied by an isolated variable AC power supply. A high-frequency filtering capacitor is installed after the bridge rectifier to smooth the output of the rectifier. The boost inductor, boost diode, power switch and output capacitor assume the power factor pre-regulator role. The ratings for the switching elements are chosen by considering maximum peak current levels.

A fast acting glass fuse and a bypass diode are placed in the circuit to prevent the components in the case over current. Also an NTC is placed in the input of the circuit to limit the start-up current due to initial charge of the output capacitor. At steady state, the resistance of this NTC is very small, thus provides minimum power loss in the NTC.

A sensing resistor with smaller resistance is placed at the source of the power MOSFET to sense the switch current. Auxiliary windings in the boost inductor are used for the zero current detection of the inductor current. Also these windings are used to supply controller IC.

4.5.2 Functional Description of the Control Circuit

Borderline control is implemented by the ON Semiconductor integrated circuit MC34262 with selected passive elements. The controller is the one of the most popular critical conduction mode IC for PFC due to easy design requirements. The controller has internal voltage reference generator, trans-conductance type voltage error amplifier, multiplier, zero current detector, over voltage comparator etc. The block diagram of the controller IC is shown in Figure 4.12.

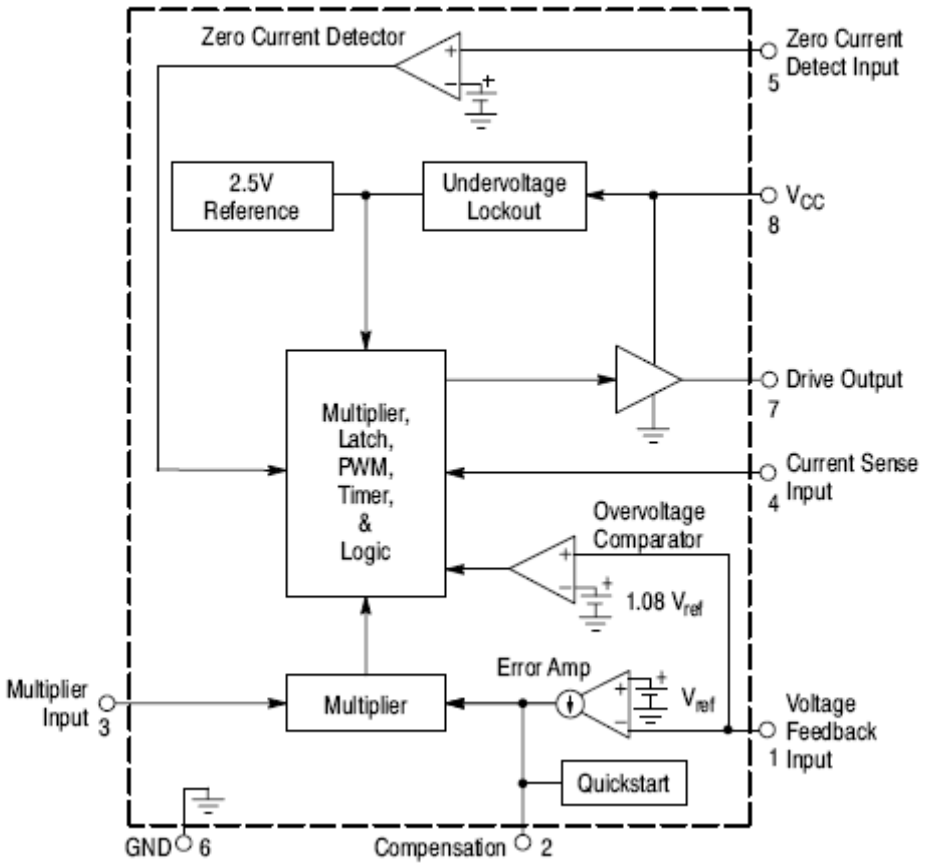


Figure 4.12 Block diagram of the MC34262 controller IC.

The MC34262 is designed for use in a pre-regulator in electronic ballasts and off-line power supplies applications. The controller consists of all required control blocks including protection blocks. Also gate drive circuit is adequate to drive any power switch element such as MOSFET or IGBT.

The controller has internal output voltage error amplifier. The inverting and output pins of this error amplifier are accessible. The non-inverting input is connected internally to the voltage reference (2.5). The output voltage divider feedback should be scaled to this reference level. The error amplifier is a transconductance type, meaning that is has high output impedance with controlled voltage-to-current gain. The gain of transconductance is around 100 μmhos. The transconductance type amplifier provides better performance; also the inverting input of the amplifier can

be used for different purposes such as over voltage comparator. The compensation passive elements are placed between the output of the amplifier and ground.

An overvoltage comparator is used to protect the circuit in case of over voltage at the output capacitor. The overvoltage limit is set to 1.08 of the reference output voltage. When this limit is exceeded, the gate is turned off until safety limits are reached again.

The multiplier is the core of the system. The inputs for the multiplier are the output of the voltage error amplifier and current waveform reference. The output of the multiplier is the reference inductor current. The actual inductor current is forced to flow between this reference and zero.

An internal zero current detector is used to turn on the power switch when the inductor current drops to zero. This inductor current information is taken from the auxiliary windings of the boost inductor. The zero current detector initiates the next on time by setting the RS Latch at the instant the inductor current reaches zero. An internal watch dog timer is used to start or restart the converter if the drive output has been off more than 600 μsec after the inductor current reaches zero.

The control IC is supplied with an auxiliary supply circuit. There is no need of external power supply. An undervoltage lockout comparator has been incorporated to guarantee that the IC is fully functional before enabling the output stage.

In the next section, design of the 150W PFC circuit with MC34262 is explained.

4.6 Design of the Boundary Conduction Mode PFC Converter

In this section, design procedure for implementing critical conduction mode controlled PFC with MC34262 IC is presented. The circuit is implemented for low power applications. First, the design specifications for the circuit are defined as given in Table 4.2.

Table 4.2 Design parameters of current conduction PFC

Output Power, P_0	150 W
Input Voltage, V_{in}	85-270V AC
Input Voltage Frequency	50Hz
Switching Frequency	Variable
Output Voltage, V_0	400Vdc
Input current THD	3%
Efficiency	90%
Hold-up time	50ms

The design process is realized using the following design procedure.

1) Power stage considerations
2) Switching frequency f_s considerations
3) Selection of the boost inductor L
4) Selection of the output capacitor C_0
5) Design of the voltage loop controller

Critical conduction mode controlled PFC with MC34262 controller IC is implemented with the selected external elements. The schematic diagram of the hardware is shown in Figure 4.13.

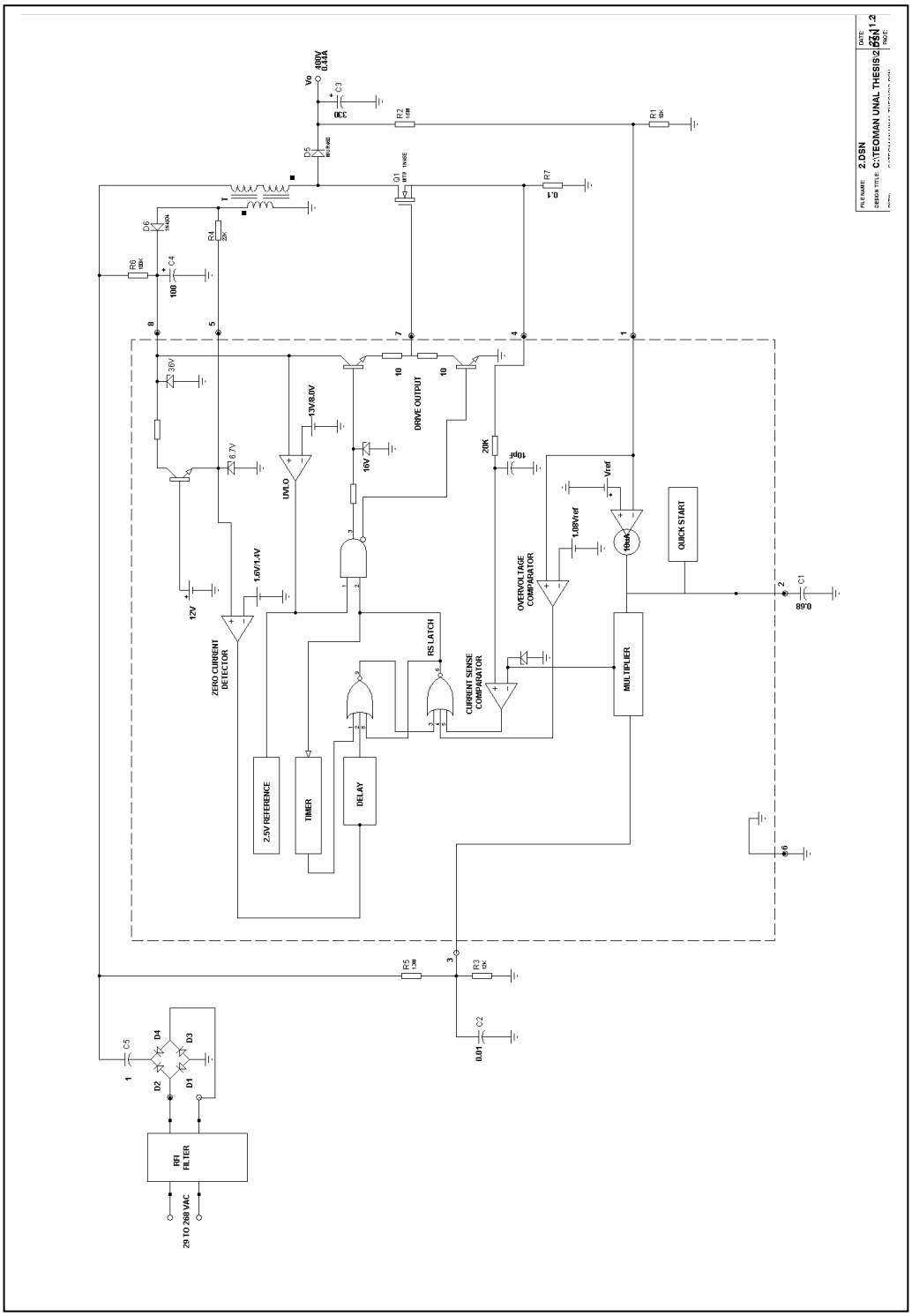


Figure 4.13 Schematic diagram of the 150W, critical current mode PFC.

1) Power Stage Considerations: A 150-W single-phase power factor correction circuit is implemented and tested in the laboratory conditions. The critical conduction mode control is suitable for the low power applications. The circuit is designed to operate with universal input voltage range. A resistive load or a dc-dc converter can be used as load of the circuit. A resistive load is used to carry out experiments in the laboratory.

The output voltage reference is set to 400 Vdc with 430 Vdc over voltage protection. The main elements of the circuit are boost inductor, power switch, boost diode and output capacitor. The boost inductor is designed with auxiliary windings to be used in the zero current detector. The selection of the power switch is done by considering the rms value of the switch current. The boost diode should have fast reverse recovery characteristics for CCM operation. Both power switch and diode should be rated about 20% above of the output voltage. The output capacitor should be selected by considering the output voltage ripple and hold-up time.

2) Switching frequency f_s considerations: The switching frequency is variable in the critical conduction mode control. The variation of the switching frequency during a line cycle is explained in section 4.3. The switching frequency characteristics for different input level are analyzed by using equation (4.14). The deviations in the switching frequency for the 220 Vac input voltage is shown in Figure 4.14. Figure 4.15 shows the switching frequency variations for 120 Vac input voltage.

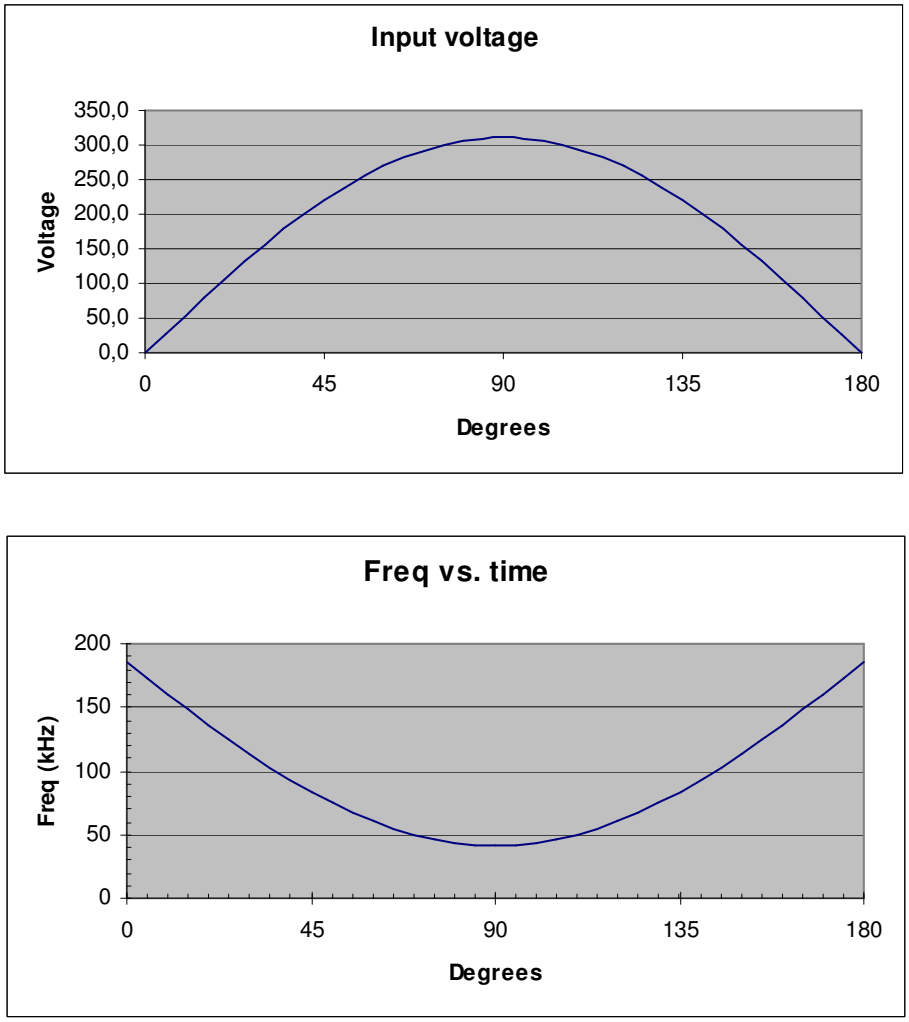
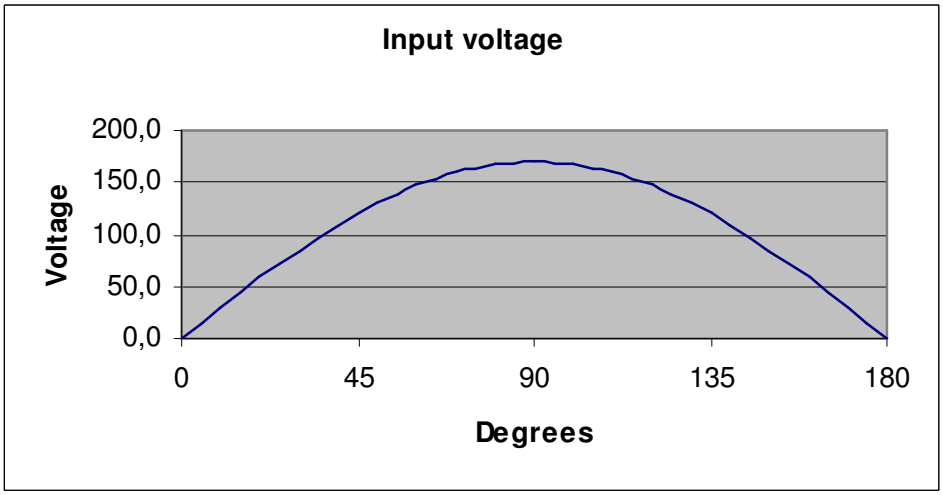


Figure 4.14 Switching frequency for 220VAC line voltage for critical current mode PFC.



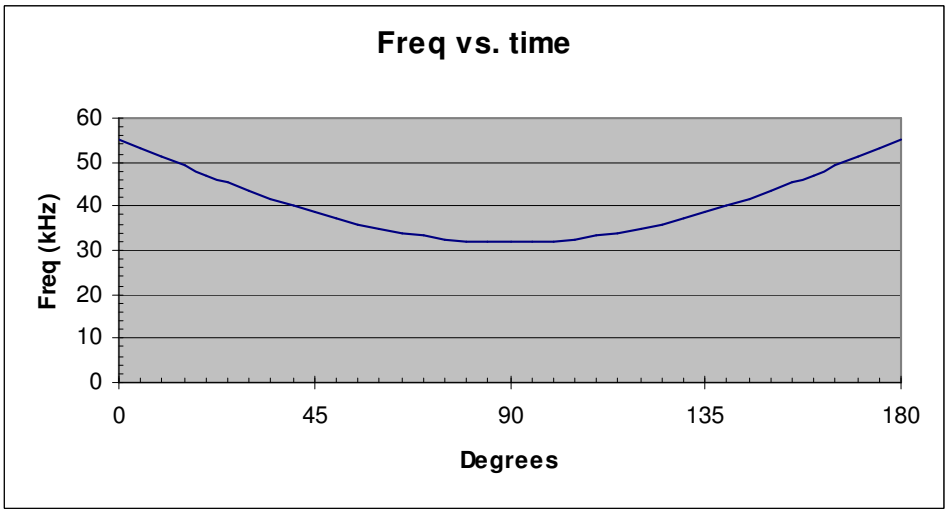


Figure4.15 Switching frequency for 120VAC line voltage for critical current mode PFC.

3) Selection of the boost inductor L: The inductance is designed for minimum switching period. Assuming that the minimum switching period is equal to 40 µsec for the universal line (85-270), the inductance value can be calculated as:

$$L_P = \frac{t \cdot \left(\frac{v_0}{\sqrt{2}} - V_{in,rms(low)} \right) V^2_{in,rms(low)}}{\sqrt{2} \cdot v_0 \cdot P_0} = \frac{40\mu\text{sec} \cdot \left(\frac{400V}{\sqrt{2}} - 85V \right) 85^2}{\sqrt{2} \cdot 400V \cdot 150W} = 600\mu H \quad (4.15)$$

The inductor is built from ferrite core material. The primary of the inductor is measured as 700 µH. 80 turns are placed in the primary of the inductor. Auxiliary windings are placed in the secondary for zero current detection and power supply for the controller IC. 5 turns are placed in the secondary.

4) Selection of the Output Capacitor C: The output capacitor defines the output voltage ripple and hold-up time for the PFC. The capacitance and the rated voltage value should be designed regarding the predefined output voltage, output voltage ripple and hold-up time for the output voltage. The capacitor with voltage and current rating greater than the normal operating point values with smaller ESR is selected. In this example a 330 µF electrolytic capacitor is used and corresponding output voltage ripple is shown in Figure 4.16.

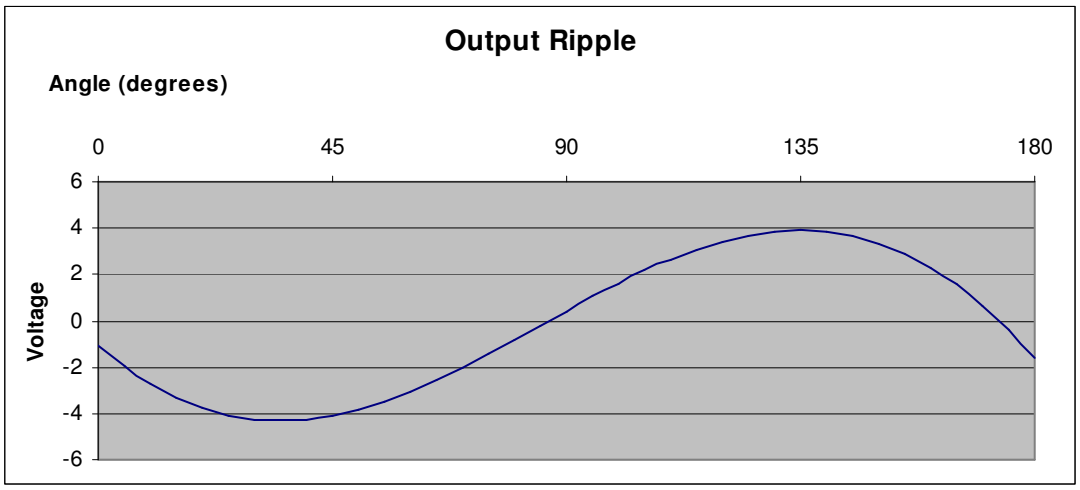


Figure 4.16 Output voltage ripple.

5) Design of the voltage loop controller: MC34262 PFC controller employs a transconductance type amplifier. This is done so that multiple functions, such as over voltage detection, can be incorporated in one IC pin. The traditional voltage type error amplifier precludes this since in a closed loop system the Vsense pin is not proportional to Vout. A transconductance type amplifier's sense pin gives the true measure of the output voltage whether the loop is in regulation or not due to connecting compensation passive elements to output. Integral compensation can be used as in the error amplifier. Figure 4.17 shows a transconductance type

error amplifier with capacitive compensation network.

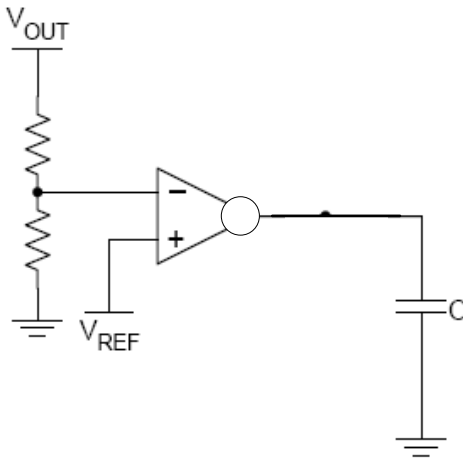


Figure 4.17 Transconductance type amplifier configuration.

All concepts for the outer voltage loop control in average current mode control are valid for critical conduction mode. The voltage controller should have low crossover frequency to limit the second harmonic ripple in the output voltage. The design for the transconductance type amplifier is straightforward. It is assumed that amplifier has 100 μs gain and the bandwidth is set to 200 Hz. So the compensation capacitor can be calculated as:

$$C = \frac{gm}{2 \cdot \pi \cdot BW} = 560nF \tag{4.16}$$

where gm is the amplifier gain and BW is the bandwidth of the output voltage controller.

4.7 Experimental Results

Critical Conduction mode PFC circuit PCB is designed and experimental results are verified in the laboratory. The PCB layout of the circuit is shown in Figure 4.18.

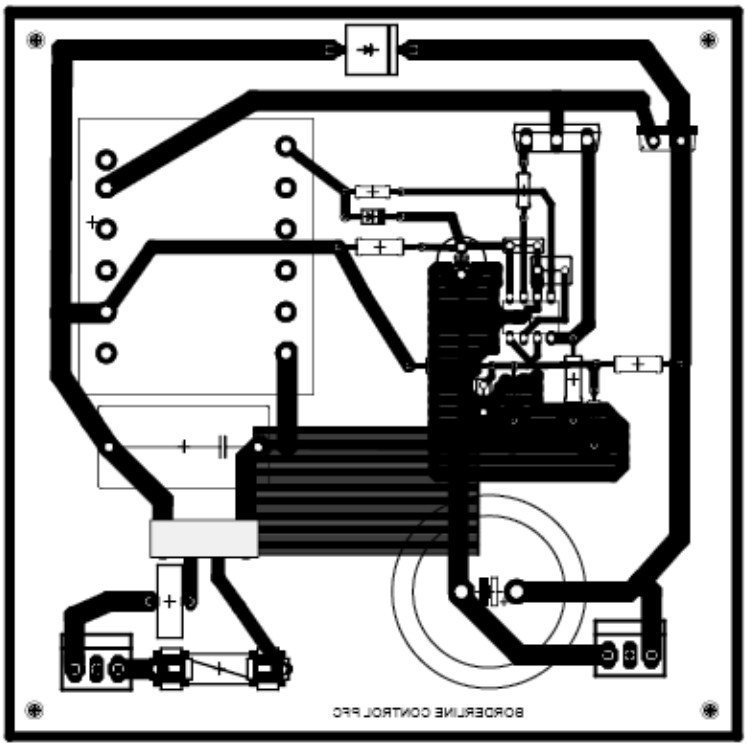


Figure 4.18 PCB layout of the critical conduction mode PFC circuit.

The circuit is supplied with an isolated variac circuit and loaded by a resistive load. First, the circuit is supplied by 220 Vac input voltage and corresponding input current and voltage waveforms are illustrated. The input voltage and input current waveforms are shown in Figures 4.19.a and 4.19.b, respectively. The corresponding harmonic content of the input current is shown in Figure 4.20. Input current has some 5^{th} order harmonic due to the input voltage harmonics.

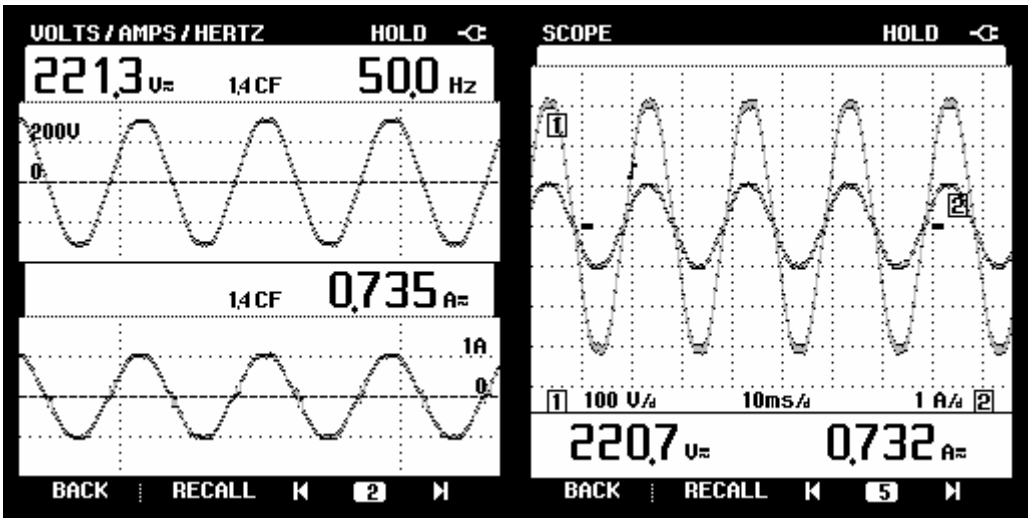


Figure 4.19 Input voltage and input current waveforms (Scales: 100V/div, 1A/div).

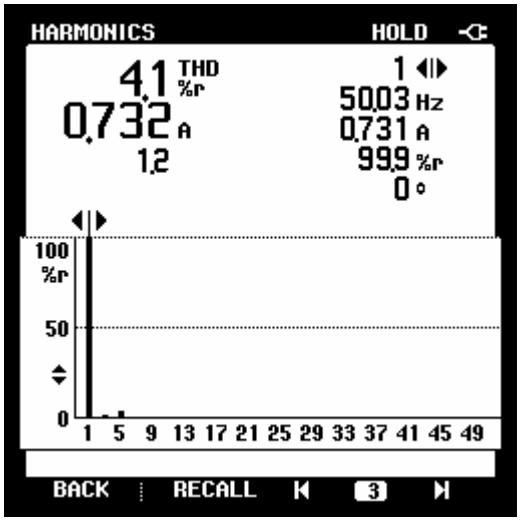


Figure 4.20 Input current harmonic spectrum.

The output voltage and input current harmonic waveforms are illustrated in Figure 4.21. The output voltage has the reference value voltage rating (400 Vdc).

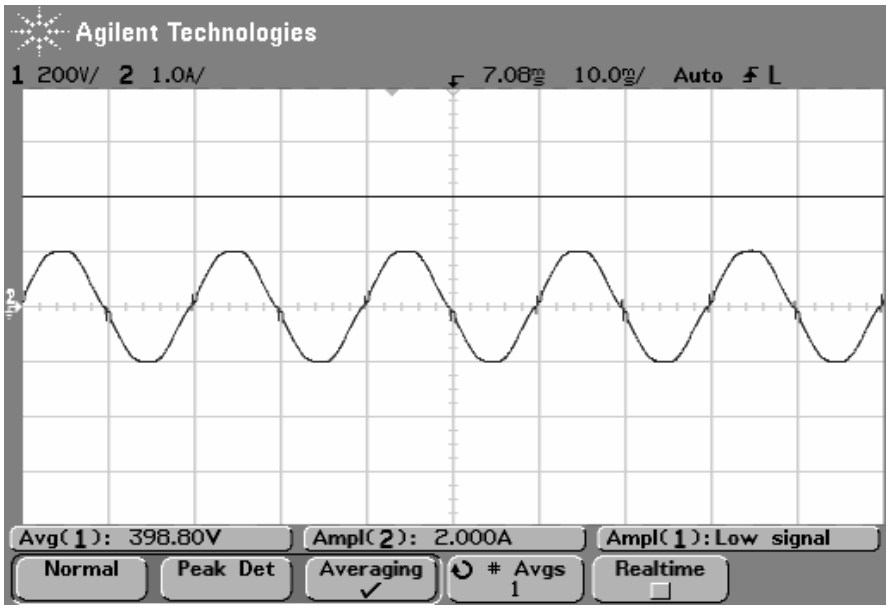


Figure 4.21 Output voltage and input current waveforms (Scales: 200V/div, 1A/div).

The input current has some distortions in the zero crossings of the line voltage due to the insufficient inductor voltage to follow the reference current. In these regions the switching frequency is very high. The controller limits the switching frequency. The distortion in the line current around the zero crossings of the line voltage is illustrated in Figure 4.22.

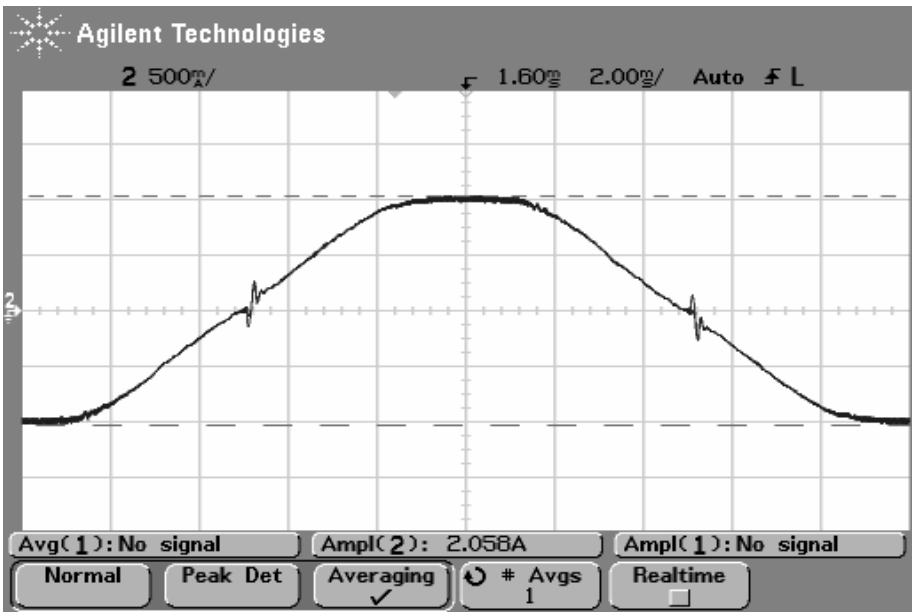


Figure 4.22 Input current distortions around zero crossings (Scale: 0.5A/div).

The input voltage is changed to 120 Vac and corresponding waveforms are illustrated. The input voltage and input current waveforms are shown in Figures 4.23.a and 4.23.b, respectively. The corresponding harmonic content of the input current is shown in Figure 4.24.

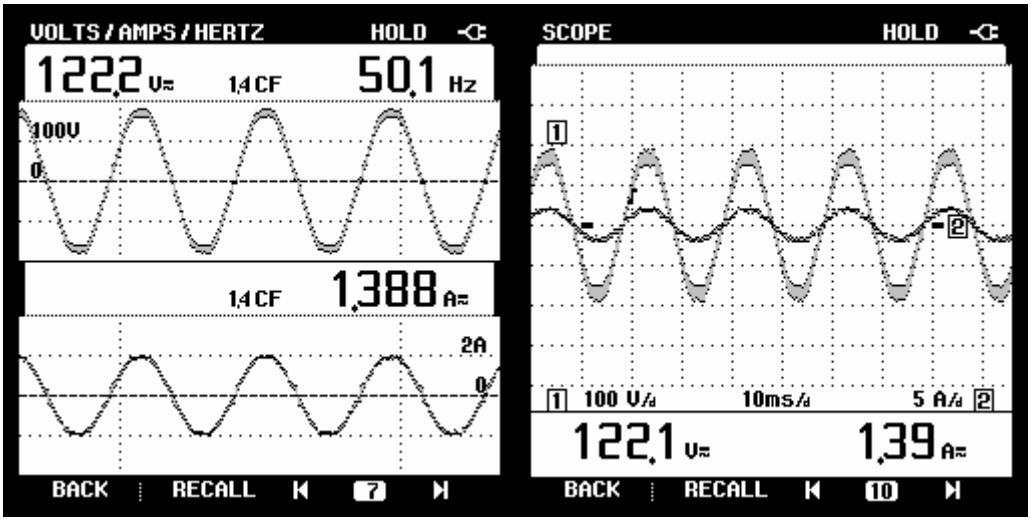


Figure 4.23 Input voltage and input current waveforms (Scales: 100V/div, 5A/div).

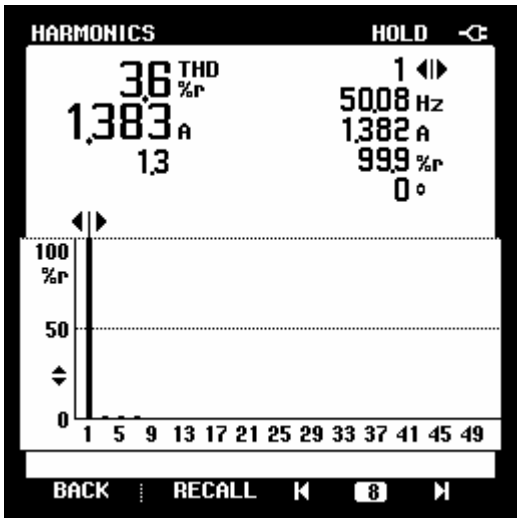


Figure 4.24 Input voltage and input current waveforms.

The output voltage and input current harmonic waveforms are illustrated in Figure 4.25. The output voltage has the reference value voltage rating (400 Vdc). The input current has some distortions in the zero crossings of the line voltage due to the insufficient inductor voltage to follow the reference current. The distortion in the line current around the zero crossings of the line voltage is illustrated in Figure 4.26.

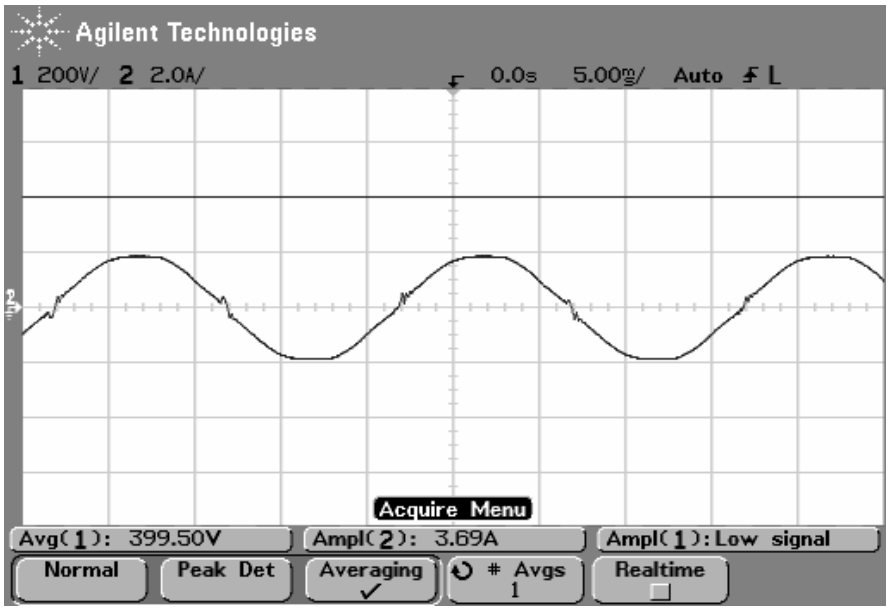


Figure 4.25 Output voltage and input current waveforms (Scales: 200V/div, 2A/div).

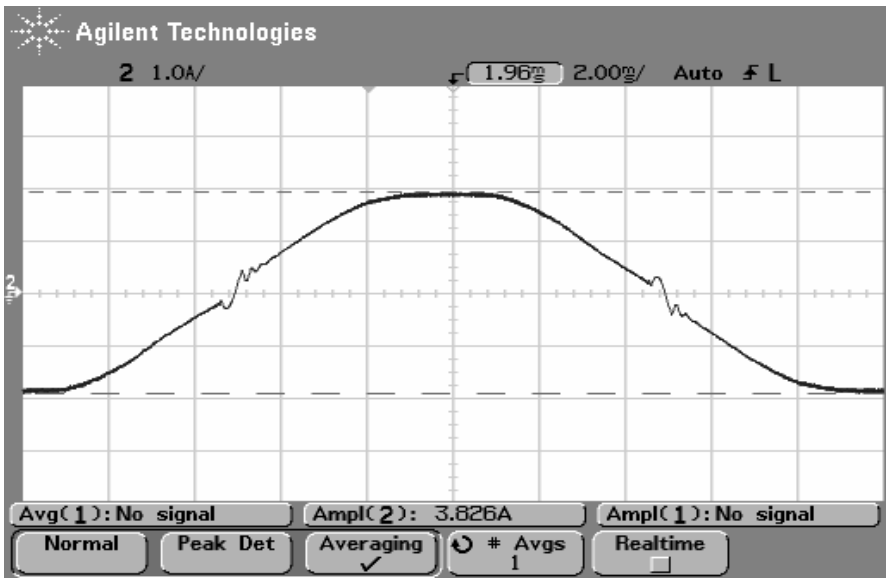


Figure 4.26 Input current distortions around zero crossings (Scale: 1A/div).

Start-up response for the input current and the input voltage is verified. Due to the soft-start structure of the control circuit output voltage reaches the steady-state operation after a few line cycles. The input current has inrush current at the start up but the circuit has the ability to alter this start-up current without damaging any of the circuit elements. The start-up response of the circuit is illustrated in Figure 4.27.

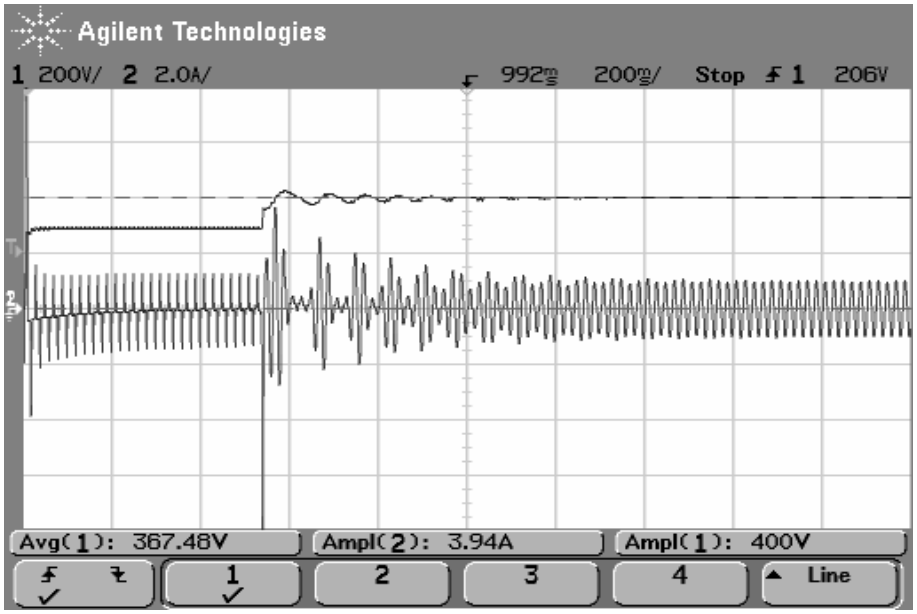


Figure 4.27 Start-up behavior of the input current and output voltage (Scales: 200V/div, 2A/div).

4.8 Conclusion

In this chapter, the critical conduction mode control of PFC is discussed. The operation characteristics and dynamic responses are analyzed. Simulation and experimental implementations are presented. The conceived system is suitable to test the performance of a borderline control of a power factor pre-regulator.

CHAPTER 5

ONE CYCLE CONTROL OF PFC

5.1 Introduction

In this chapter, an implementation of the One Cycle Control (OCC) method, that simplifies the design procedure for the continuous conduction mode PFC converters. The average current and borderline control methods were analyzed in Chapter 4 and 5. Both control methods consist of a multiplier as a core element in the PFC control with input voltage sensing. One cycle control method reduces the design complexity and manufacturing cost of a PFC converter. A resettable integrator is the core element of one cycle control so this control method also called as integration reset technique [45], [55].

One cycle control technique has ability to real time response to the non-linear nature of the switching converters. Any step chances in the voltages or the currents in the PFC circuit can be controlled instantaneously. Duty cycle of the boost converter is modulated to force the input to appear purely resistive. OCC control can be applied any converter topologies.

The basic operation principle is as follows. The output of the voltage error amplifier is integrated over the switching cycle. Since the voltage controller has small bandwidth, the output of the voltage error amplifier is constant in a switching cycle thus the output of the integrator is a ramp voltage. The slope of the ramp voltage depends on the output voltage variations. This ramp voltage is compared to a voltage reference generated by a combination of the sum of the inductor current and the voltage error amplifier's output. PWM generator determines the duty cycle according

to the output of the comparator. A one cycle controlled PFC converter block diagram is shown in Figure 5.1.

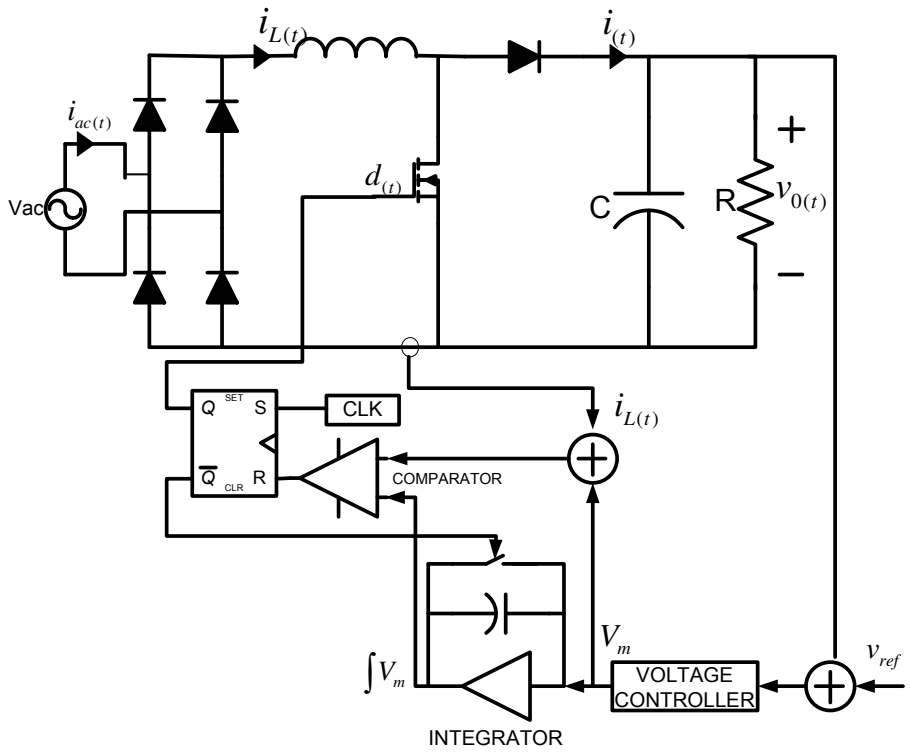


Figure 5.1 One cycle control of PFC.

As it is illustrated in Figure 5.1, the integrator is the main control element of one cycle control. The ramp generated by this integrator is reset at the end of each switching cycle and ramp starts again from zero in the new switching cycle. So a cycle-by-cycle control is achieved and called as “One Cycle Control”.

5.2 Operation of One Cycle Control

The one cycle control method requires no input voltage sensing, no analog multiplier, and no sawtooth waveform generator. The output of the voltage error amplifier is integrated over the switching cycle and a ramp voltage is generated. This ramp voltage has the characteristics of outer voltage loop dynamics. The dynamics are evaluated in switching periods providing fast response. The sensed inductor current is compared with the output of the integrator to generate required duty cycle

for unity power factor correction. So the regulation of the output voltage is done by the resettable integrator and sinusoidal input current waveform is achieved by PWM generating algorithm.

The type of the voltage error amplifier is the same as with the other control methods. The output voltage Vo is scaled to reference value. The error amplifier compensates the error between the actual output voltage and reference. The bandwidth of the error amplifier is small to reduce 2nd harmonic distortion. The output of the voltage error amplifier V_m is constant during each switching cycle. A transconductance type error amplifier is shown in Figure 5.2.

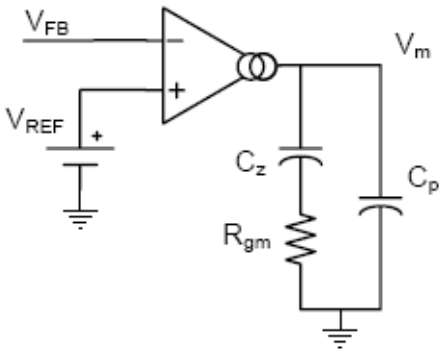


Figure 5.2 Transconductance type error amplifier.

The output of the integrator is a ramp voltage due to the constant output voltage of the error amplifier in a switching cycle. The slope of the ramp is the function of the output voltage error amplifier and proportional to the output voltage variations. However, the output of the integrator $\int V_m$ must match the integrated value V_m in each switching period. The resettable integrator characteristic is shown in Figure 5.3.

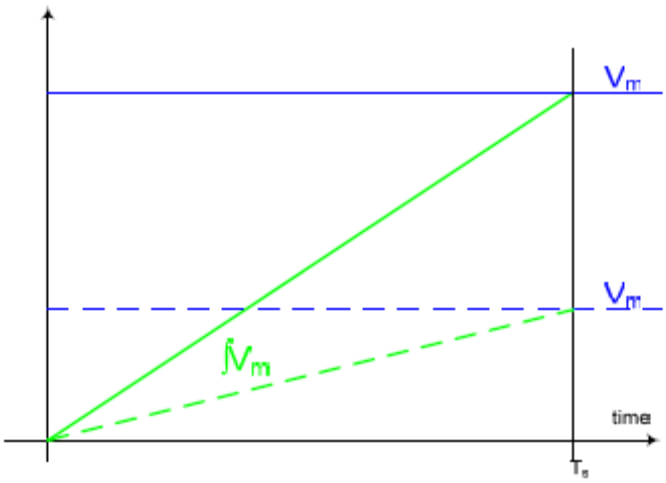


Figure 5.3 Resettable integrator characteristics.

Inductor current is sensed with sense circuit such as sense resistor or current transformer. A reference for the PWM generator is obtained by subtracting the sensed voltage from the modulation voltage V_m. The control block diagram is illustrated in Figure 5.4.

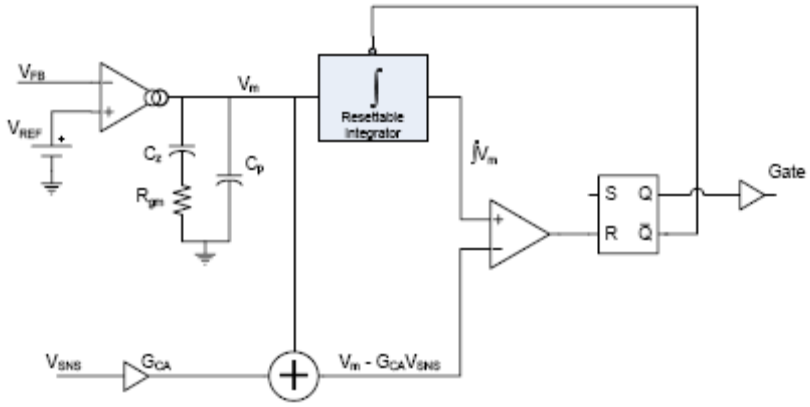


Figure 5.4 Block diagram of OCC.

The corresponding integrator output voltage $\int V_m$, PWM reference signal (V_m-G.V_{sense}) and gate signal for an example circuit is illustrated in Figure 5.5.

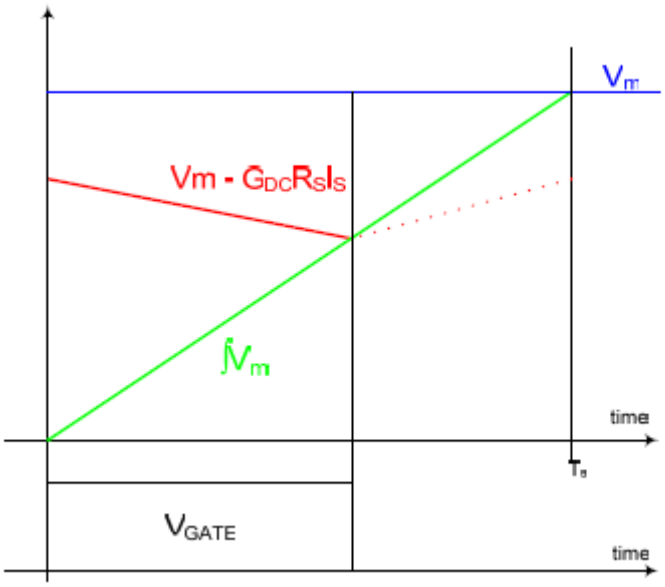


Figure 5.5 PWM signal generation.

As a result, a PWM reference signal dependant on the input current and a ramp signal dependant on the output voltage are generated in one cycle control. The required gate signal is generated for high power factor correction and regulated output voltage. The input voltage sensing and multiplier block in the control system is removed. The design process includes fewer stages.

5.3 Simulation of One Cycle Control of PFC

The simulation analysis of a one cycle controlled single-phase PFC converter is analyzed by the SIMPLORER simulation tool. Simulated circuit is shown in Figure 5.6. The performance analysis, verification of input current and voltage waveforms, output voltage waveforms are illustrated.

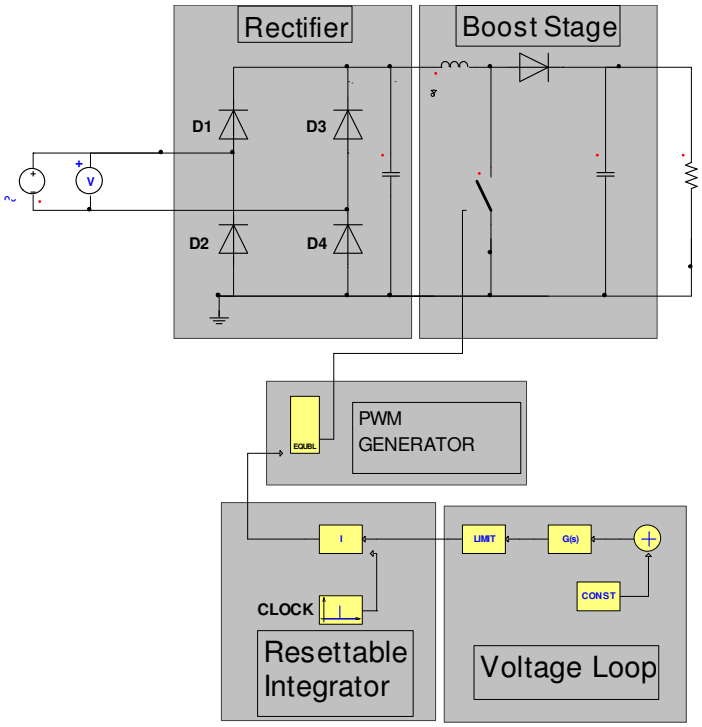


Figure 5.6 Simulation circuit of one cycle control.

Basically, simulation circuit consists of a single-phase diode rectifier with a cascaded boost converter as power circuit. The voltage loop controller, resettable integrator and a PWM generator is used to implement control circuit. Simulation parameters are given in Table 5.1.

Table 5.1 Simulation parameters of active PFC

Output Power, P_0	250 W
Input Voltage, V_{in}	90-265V
Input Voltage Frequency	50Hz
Switching Frequency	100kHz
Output Voltage, V_0	400V
Boost Inductor, L	1mH
Output Capacitor, C_0	330uF
Integration Formula	Euler
Minimum Step Time	0.1u

The voltage loop controller has the same specification with the other control methods. The low bandwidth voltage controller is implemented by the s-transfer function block in the simulation tool. The resettable integral is implemented by analog integrator in the SIMPLORER. The reset signal is obtained from a clock source that defines the switching frequency. The block properties of the voltage controller and integrator are shown in Figure 5.7.a and 5.7.b.

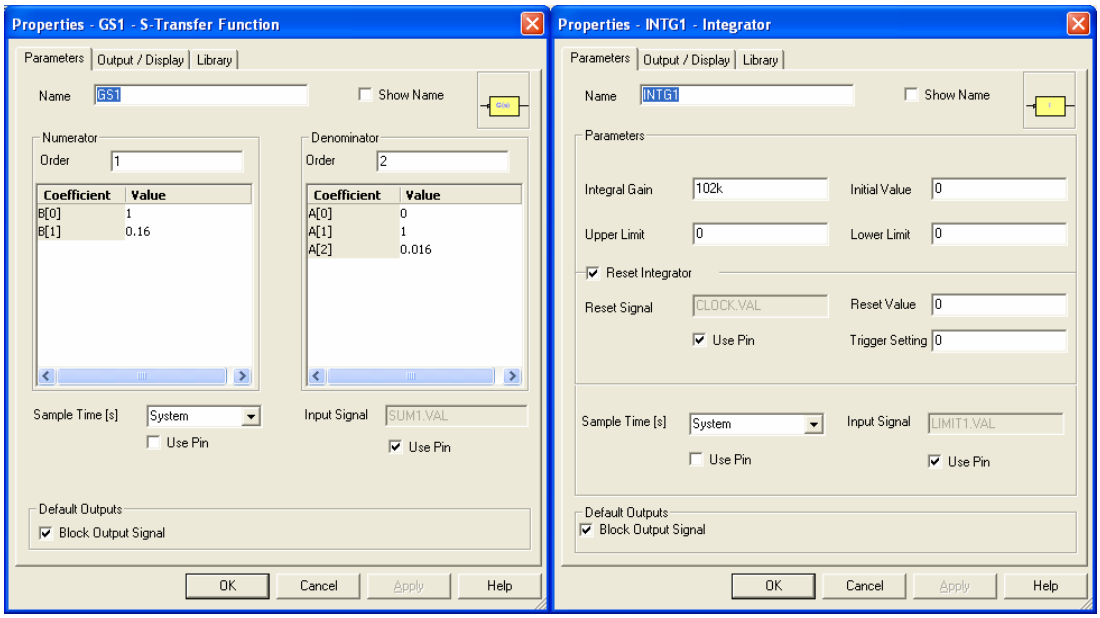


Figure 5.7 Simulation blocks a) Output voltage controller b) Resettable integrator.

The simulation waveforms for the different input voltages are verified for a 250W PFC converter. Two different level input voltage is applied and corresponding input current and output voltage waveforms are illustrated. The input voltage and current simulation waveforms for the 220Vac input voltage are shown in Figure 5.8. The simulation waveforms for the input voltage and input current for a 150Vac input voltage are shown in Figure 5.9.

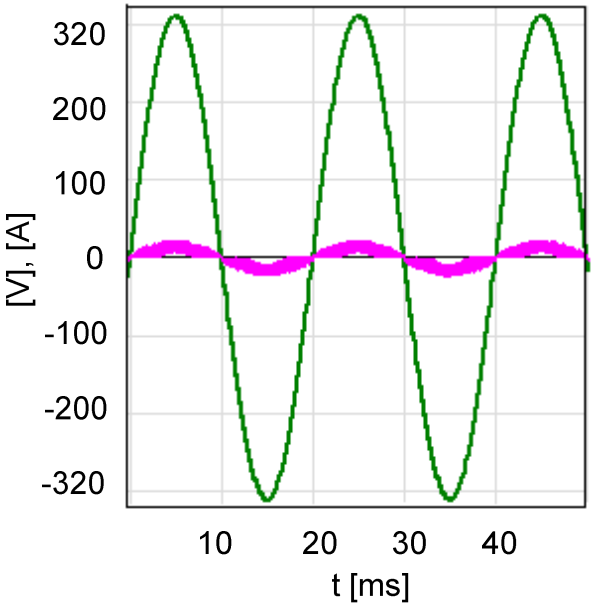


Figure 5.8 Input voltage and current simulation waveforms for 220Vac input voltage (Current Scale: 5x).

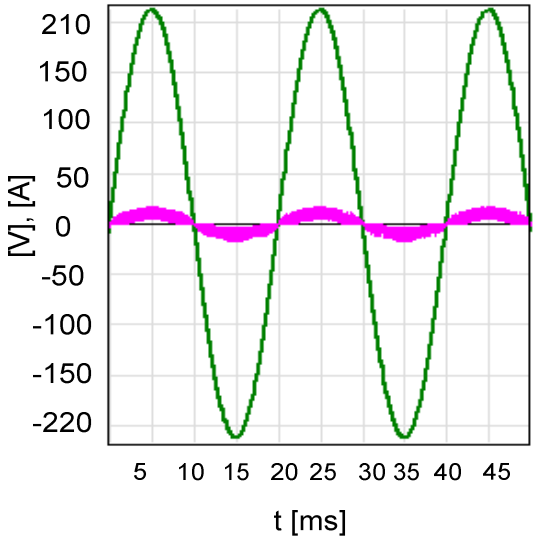


Figure 5.9 Input voltage and input current simulation waveforms for 150Vac input voltage (Current Scale: 5x).

The steady-state output voltage simulation waveform with input current is illustrated in Figure 5.10.

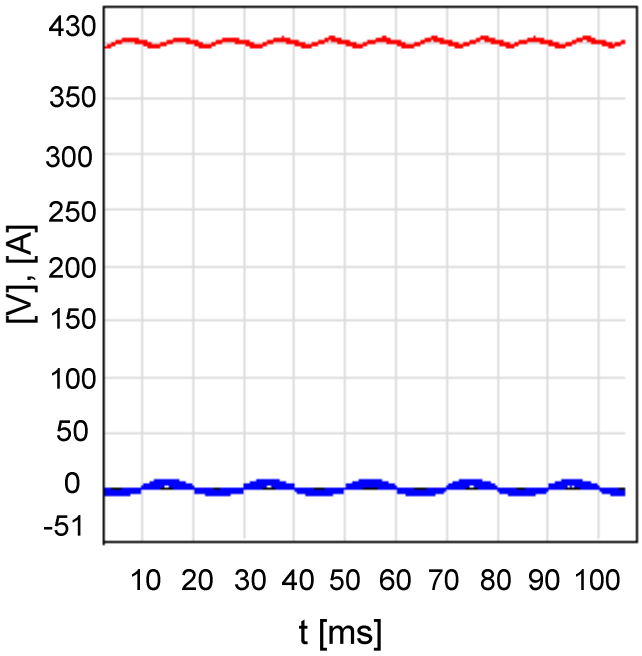


Figure 5.10 Input voltage and input current simulation waveforms for 150Vac input voltage (Current Scale: 5x).

5.4 Hardware Implementation of One Cycle Control PFC Converter

General specifications for a one cycle control of PFC converter with an analog PFC controller are explained in this section. The International Rectifier IR1150 analog PFC controller is used to implement one cycle control. The power stage is similar with the previously mentioned control methods. The OCC control technique serves low complexity in design process also needs fewer external components. The types of the components in the power circuit with their general specifications are summarized briefly in the subsection 5.4.1. The general parameters and the block diagram of the controller are given in the subsection 5.4.2.

5.4.1 Functional Description of the Power Circuit

Design of the power stage is similar to the average current mode control. A single-phase bridge rectifier with a cascaded boost converter is built and critical conduction mode control is applied. The load is chosen as a resistive load. Input is supplied by an isolated variable AC power supply. A high frequency filtering capacitor is installed after the bridge rectifier to smooth the output of the rectifier. The boost inductor, boost diode, power switch and output capacitor provides the power factor pre-regulator role. The ratings for the switching elements are chosen by considering maximum peak current levels.

A fast acting glass fuse and a bypass diode is placed in the circuit to prevent the components in the case over current. Also a NTC is placed in the input of the circuit to limit the start-up current due to initial charge of the output capacitor. In the steady state, the resistance of this NTC is very small thus provides minimum power loss in the NTC.

Only inductor current is sensed through a sense resistor. A current transformer or hall-effect devices can be used for current sensing providing smaller power loss.

5.4.2 Functional Description of the Control Circuit

IR1150 PFC controller IC simplifies the design of PFC converter. The number of required external elements to implement a PFC converter is very low. The controller IC has inner voltage loop controller with reference voltage generator, resettable integrator, duty cycle generator and protection sub-circuits [56]. The block diagram of the IR1150 controller IC is given in Figure 5.11.

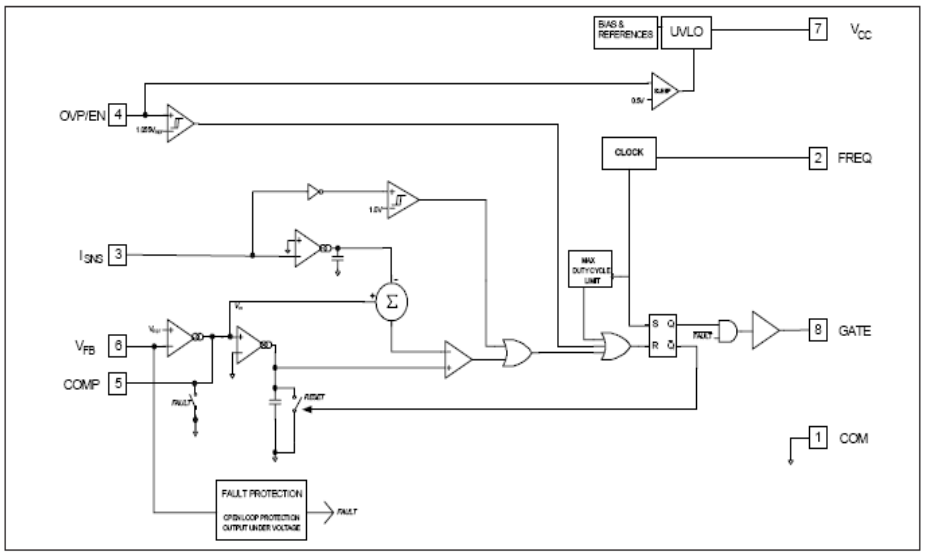


Figure 5.11 Block diagram of IR1150 PFC controller.

IR1150 PFC controller is designed for boost converter that operates with a fixed frequency in continuous conduction mode. A current controller provides to create a sinusoidal input current profile analogous to input voltage in continuous conduction mode. There are some zero crossing distortions in the input current due to the smaller inductor voltage at zero crossing regions. A transconductance type voltage error amplifier is used for the outer voltage loop controller. The output of this error amplifier is integrated with a resettable integrator. A ramp signal is produced by the integrator which defines the amplitude of the average input current. So the current controller defines the shape of the input current and the voltage controller with integrator defines the magnitude of the input current.

IR1150 PFC controller IC includes an internal oscillator that is programmable by connecting external resistor. The controller IC has ability to operate between 50 kHz and 200 kHz range. It is possible to operate at lower frequency but the size of magnetic components will be larger.

The PFC controller IC has internal protection circuits such as over current, over voltage, under voltage and brownout. The UVLO circuit provides safety operating point by controlling supply voltage V_{cc} of the IC. Over voltage protection OVP

function protect the system from over voltage conditions. When the over voltage limit is exceeded, gate drive will be turned off. The controller also limits the current in the case of brownout and overload.

5.5 Design of the One Cycle Control PFC Converter

In this section, design procedure for implementing one cycle control method for a PFC converter is presented. The circuit is implemented for 250W applications. First, the design specifications for the circuit is define as follows;

Table 5.2 Design parameters of active PFC

Output Power, P_0	250 W
Input Voltage, V_{in}	85-270V AC
Input Voltage Frequency	50Hz
Switching Frequency	100kHz
Output Voltage, V_0	385Vdc
Input current THD	5% max
Efficiency	90%
Hold-up time	50ms

The design process is maintained by using following design procedure.

1) Power stage considerations
2) Selecting switching frequency f_s
3) Selection of the boost inductor L
4) Selection of the output capacitor C_0
5) Current Loop Considerations
6) Design of the voltage loop controller

The schematic diagram of the one cycle controlled, 250W PFC converter is shown in Figure 5.12.

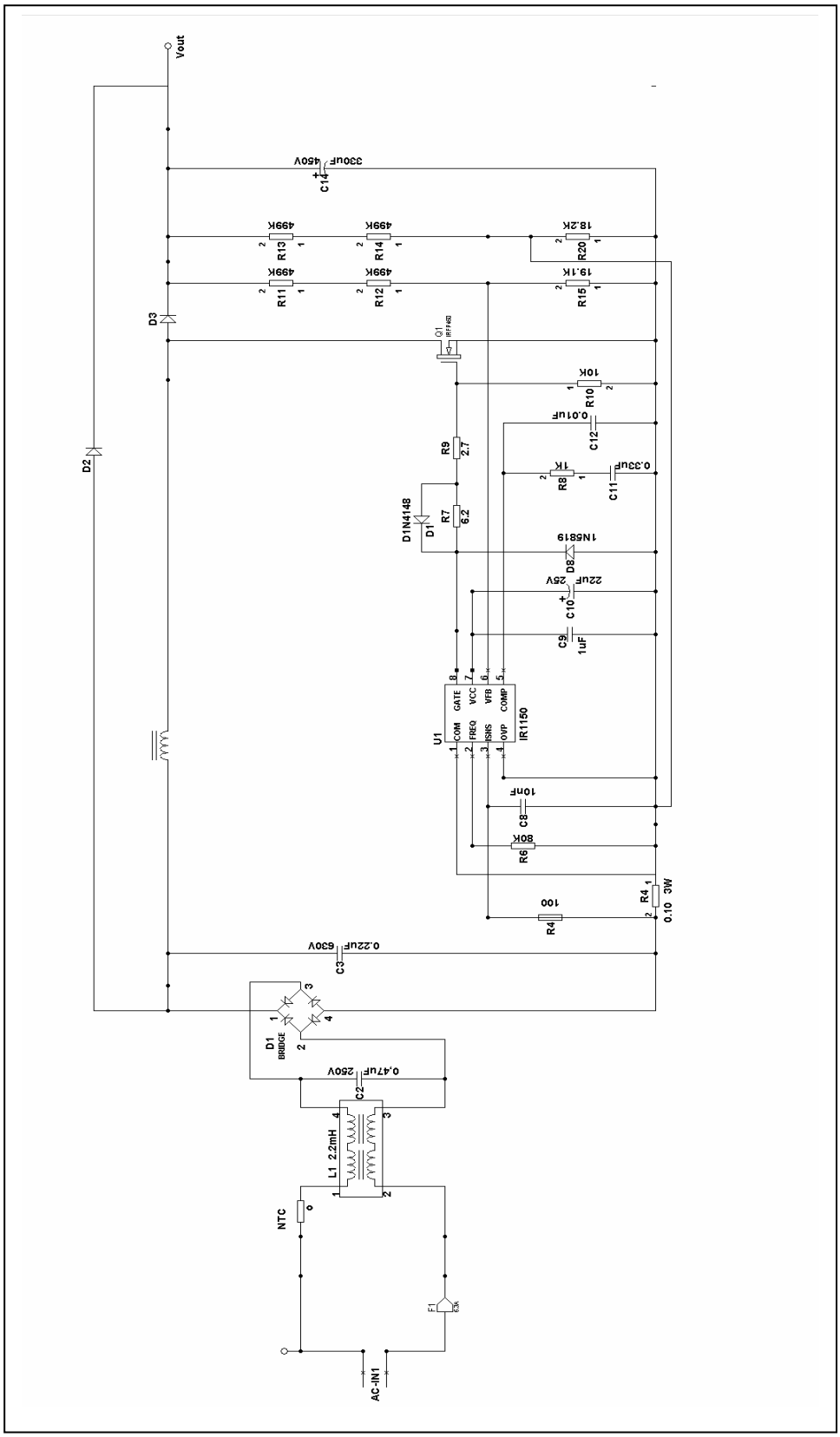


Figure 5.12 Schematic of 250W PFC converter with IR1150.

1) Power Stage Considerations: As the system is supposed to operate in universal input line, the design of the power stage should be done according to the worst case conditions. The selection of the circuit elements will be done for the low input line voltage and high input current. A 250W single-phase power factor correction circuit is implemented and tested in the laboratory conditions. The circuit is designed to operate in continuous conduction mode. A resistive load or a dc-dc converter can be used as load of the circuit. A resistive load is used to make required experiments in the laboratory.

The output voltage reference is set to 385Vdc with 420Vdc overvoltage protection. The main elements of the circuit are boost inductor, power switch, boost diode and output capacitor. The selection of the input diode, power switch and boost diode is done by considering the rms value of the switch current. Both power switch and diode should be rated about 20% above of the output voltage. The output capacitor should be selected by considering the output voltage ripple and hold-up time.

Maximum input power can be calculated assuming 90% efficiency at low input voltage:

$$P_{in(\max)} = \frac{P_0}{\eta} = \frac{250W}{0.9} = 278W \tag{5.1}$$

The maximum peak input current is the key point for designing circuit element's values and ratings. Selection of the over current limit and the design of the boost inductor power rating are based on the maximum peak inductor current.

$$I_{in,peak(\max)} = \frac{\sqrt{2} \cdot P_0}{\eta \cdot V_{in,rms(\min)}} = \frac{\sqrt{2} \cdot 250W}{0.9 \cdot 85V} = 4.62A \tag{5.2}$$

A high frequency AC capacitor is placed at the output of the rectifier to filter the high frequency noise. The value of capacitor should not be high to avoid the phase distortion in the input current. A 220 uF, 630V AC capacitor is used for this purpose.

2) Switching frequency f_s considerations: One cycle control method operates in constant switching cycle. The switching frequency is defined by external resistor connected to the frequency pin in the IR1150 IC. The controller datasheet illustrates the switching frequency versus programming resistor diagram in Figure 5.13. A 80K metal film is used to make the operating switching frequency as 100kHz.

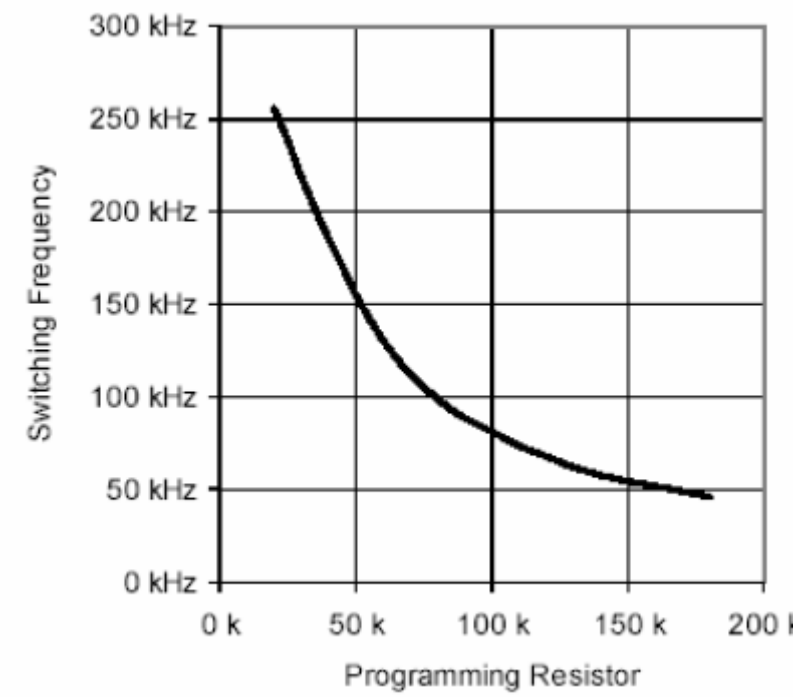


Figure 5.13 Switching frequency vs. programming resistor.

3) Selection of the boost inductor L: Selection of the boost converter is made according to the maximum peak input current, maximum output power and maximum duty cycle. These are worst case conditions and the selected inductor should satisfy all these worst case requirements. The boost inductor determines the high frequency ripple for the inductor current. The maximum peak current was defined in the first step as 4.6A. The peak to peak ripple current is defined the 20% of the maximum input peak current. So the high frequency ripple current is:

$$\Delta I = 0.2 \cdot I_{in,peak(\max)} = 0.9A \tag{5.3}$$

Maximum duty cycle is determined at the low input line voltage's peak value.

$$D = \frac{V_0 - V_{in,peak(\min)}}{V_0} = \frac{385 - \sqrt{2} \cdot 85}{385} = 0.69 \tag{5.4}$$

Required inductance is calculates as follows:

$$L = \frac{V_{in,peak(\min)} \cdot D}{f_s \cdot \Delta I} = \frac{120V \cdot 0.69}{100kHz \cdot 0.9A} = 0.89mH \tag{5.5}$$

Where D is the duty cycle, f_s is the switching frequency and ΔI is the inductor current ripple. A 900uH, ferrite core, high frequency inductor is used with 6A peak current handling capacity.

4) Selection of the Output Capacitor C_0: Typically, 1uF and 2uF per output power capacitance value is optimum for the output capacitor selection. The required capacitance can be calculated based on the hold-up time and minimum output voltage as:

$$C_0 = \frac{2 \cdot P_0 \cdot \Delta t}{(V_0^2 - V_{0,\min}^2)} = \frac{2 \cdot 250W \cdot 20ms}{385^2 - 320^2} = 200\mu F \tag{5.6}$$

220uF, 450Velectrolytic capacitor is used as a standard value.

5) Current Loop Considerations: The inductor current is sensed with a sense resistor. The range for the sense voltage V_{SNS} is between 0V and 1V. The current amplifier has a DC gain G_{DC} is equal to 2.5. The current sense resistor should be selected at the minimum input voltage and maximum output power. The maximum sensed voltage is 0.75V and maximum allowable input current is 5.5A. So the selection of the sense resistor value is straightforward.

$$R_{sns} = \frac{V_{sns,\max}}{I_{in,peak(\max)}} = \frac{0.75V}{6.5A} = 0.115\Omega \tag{5.7}$$

The sensed current is filtered by a simple RC filter to attenuate the high frequency noise. An RC filter is placed at the input of the current sense pin.

6) Design of the voltage loop controller: The outer voltage loop controller design is similar with the average current control technique. First, the stability analysis of the power circuit is done. Then required compensation parameters are calculated for the error amplifier. The block diagram for the outer voltage loop is shown in Figure 5.14.

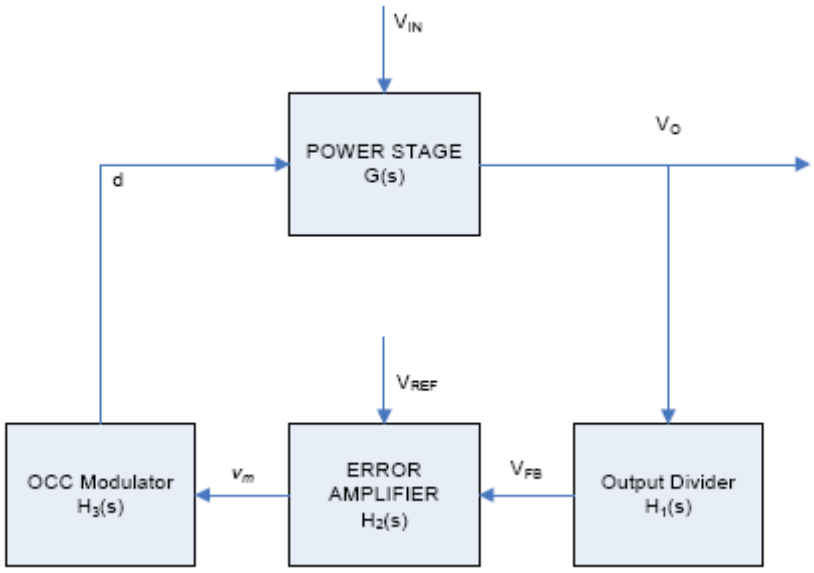


Figure 5.13 Outer voltage loop.

The open loop gain of the voltage loop T (s) is:

$$T(s) = H_1(s).H_2(s).H_3(s).G(s) \tag{5.8}$$

Output voltage divider consists of resistive divider circuit. The output voltage is scaled down to the reference value (7.5 V). So the output divider transfer function $H_1(s)$ is:

$$H_1(s) = \frac{V_{REF}}{V_0} \tag{5.9}$$

Because the outer voltage loop has smaller crossover frequency around 20Hz, a small signal model of the power stage accurate at frequencies below 100Hz should be used. The small signal model of the PFC converter consists of a controlled power source modeled as a current source shunted by a resistor shown in Figure 5.15.

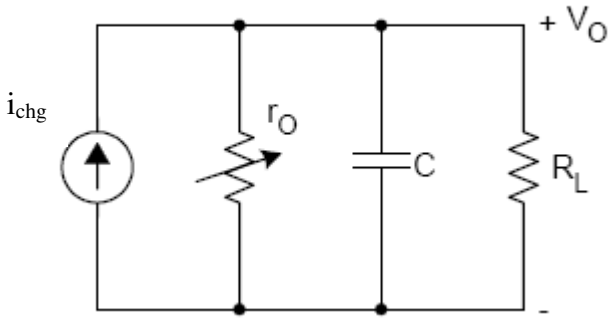


Figure 5.14 Small signal model of outer loop.

The variable source resistance r_o is equal to the load resistance R_L. r_o changes when R_L changes. The load can be a resistive load or a constant power load such as a dc-dc converter. In the case of resistive load, the r_o is equal to the load resistance R_L and the parallel combination of these variables defines the single pole response of the transfer function. However, in the case of the constant power load, it has a negative small signal resistance ($-R_L$). The negative resistance is equal an opposite in sign to the dc resistance and parallel combination approaches infinity. So the model becomes a current source driving a dc capacitor. In the case of constant power source the current to output transfer function of the converter is:

$$\frac{\hat{v}_0}{\hat{i}_{chg}} = \frac{1}{sC_0} \tag{5.10}$$

The multiplication of the transfer function of the power stage G(s) and PWM modulator $H_3(s)$ is

$$H_3(s).G(s) = \frac{\widehat{v_0}}{\widehat{v_m}} = \frac{\widehat{v_0}}{\widehat{i_{chg}}} \cdot \frac{\widehat{i_{chg}}}{\widehat{v_m}} \tag{5.11}$$

The first term in Eq. 5.11 is derived in Eq. 5.10. The second term $\frac{\widehat{i_{chg}}}{\widehat{v_m}}$ can be derived by analyzing the control method of the one cycle control. The conversion ratio in the one cycle control is:

$$M(d) = \frac{\widehat{v_0}}{\widehat{v_g}} = \frac{\widehat{v_m}}{G_{DC} \cdot R_S \cdot \widehat{i_g}} \tag{5.12}$$

where v_g is input voltage and consists of small signal variations.

$$\widehat{v_g} = V_{in} + \widehat{v_{in}} \tag{5.13}$$

By linearization and perturbation process the nonlinear terms can be eliminated.

$$\frac{\widehat{i_g}}{\widehat{v_m}} = \frac{V_{in}}{V_0 \cdot G_{DC} \cdot R_S} \tag{5.14}$$

The output average current can be calculated from the input current:

$$\widehat{i_g} = \frac{\widehat{i_{chg}} \cdot V_0}{V_{in}} \tag{5.15}$$

Thus:

$$\frac{\widehat{i_{chg}}}{\widehat{v_m}} = \frac{V^2_{in}}{V^2_0 \cdot G_{DC} \cdot R_S} \tag{5.16}$$

The control to output transfer function of the power stage can be derived by using Eq. (5.10) and (5.16) as:

$$H_3(s).G(s) = \frac{\widehat{v_0}}{\widehat{v_m}} = \frac{\widehat{v_0}}{\hat{i}_{chg}} \cdot \frac{\hat{i}_{chg}}{\widehat{v_m}} = \frac{1}{sC_0} \cdot \frac{V^2_{in}}{V^2_0 \cdot G_{DC} \cdot R_S} \tag{5.17}$$

The transfer function of power stage has a single pole roll-off characteristic that varies with input voltage. The voltage error amplifier should be designed according to this characteristic. A two pole and one zero voltage compensator is used in the outer voltage loop. IR 1150 has internally transconductance type error amplifier. The diagram of the transconductance type error amplifier with externally connected compensator elements are shown in Figure 5.16.

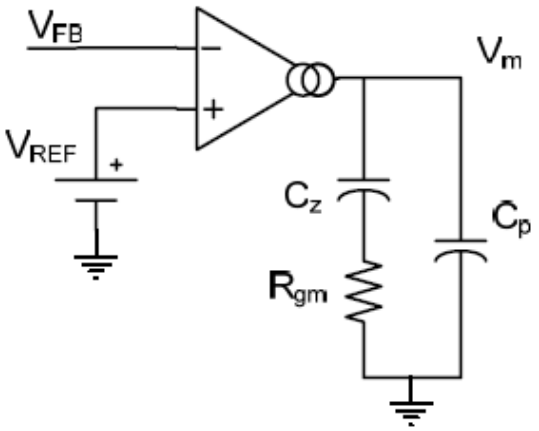


Figure 5.15 Voltage error amplifier.

The transfer function of the error amplifier $H_2(s)$ is:

$$H_2(s) = \frac{g_m \cdot (1 + sR_{gm}C_Z)}{s(C_Z + C_P + sR_{gm}C_Z C_P)} \tag{5.18}$$

A pole is placed at the origin to reduce steady-state error. The zero is required to make the loop stable. The other pole is placed at the crossover frequency of the voltage loop. A crossover frequency is selected around 20Hz to attenuate 2nd harmonic ripple in the voltage loop. The effects of low bandwidth controller were mentioned in chapter 4. The same procedure is maintained in average current mode control to determine the values of the external elements. The corresponding compensator elements values are:

$$\begin{aligned} R_{gm} &= 8k\Omega \\ C_{Z} &= 330nF \\ C_{P} &= 10nF \end{aligned} \tag{5.19}$$

5.6 Experimental Results

The hardware of the one cycle control PFC converter is implemented according to above design process. The PCB layout of the circuit is shown in Figure 5.17.

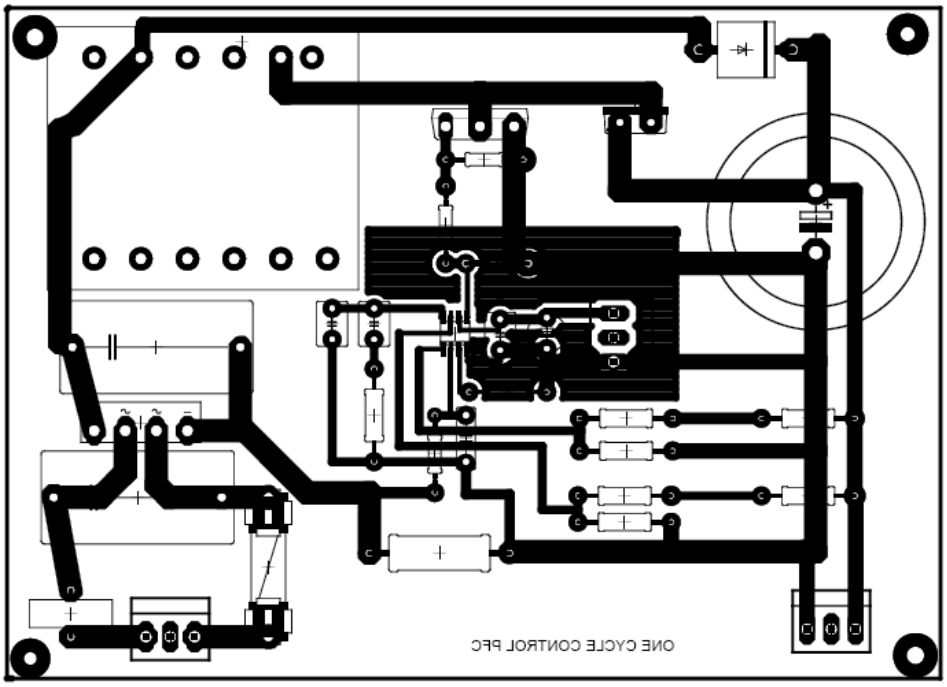


Figure 5.16 PCB layout of one cycle control PFC converter.

The circuit is supplied with an isolated variac circuit and loaded by a resistive load. The results for the input current are verified for two different input voltage levels. The input voltage and input current waveforms are shown in Figure 5.18.a and 5.18.b for 220Vac and 120Vac input voltage respectively.

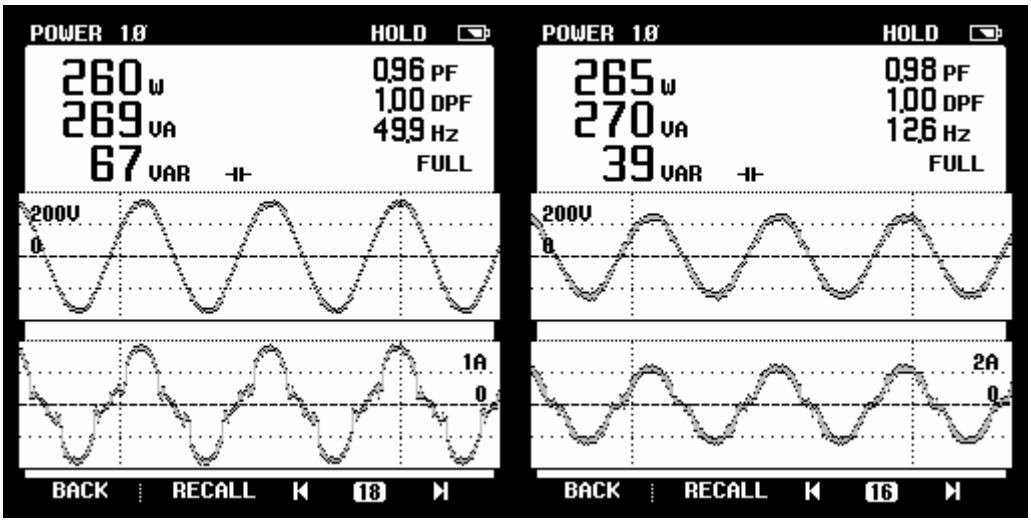


Figure 5.17 Input voltage and input current waveforms a) 220Vac (Scales: 200V/div, 1A/div) b) 150Vac (Scales: 200V/div, 2A/div).

The output voltage is monitored with the input current. The output voltage and input current waveforms for 250W one cycle control PFC converter is shown in Figure 5.19.

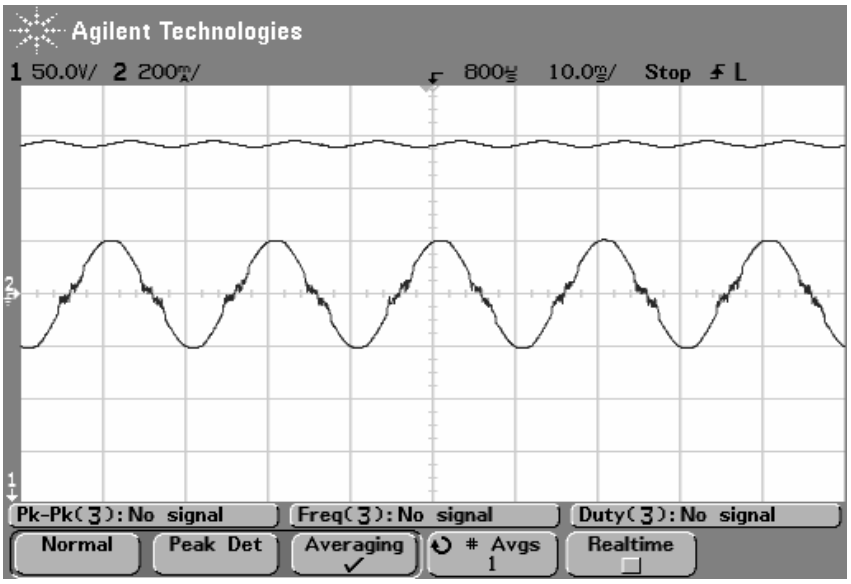


Figure 5.18 Output voltage and input current waveforms (Scales: 150V/div, 2A/div).

The output voltage has about 5V second harmonic ripple. The input current has some distortions near the zero crossings of line voltage. As the system is designed for the worst case conditions that occur in minimum input line and maximum output power, the circuit performance is better at minimum line voltages.

5.7 Conclusions

The verified results show that, one cycle control technique is also optimum solution for active power factor correction. The one cycle control based design requires lower component count that reduces manufacturing cost. A comparison table of the analog multiplier based approaches with the one cycle control is given.

Table 5.3 Comparison table of control topologies

Design Parameter	**Analog Multiplier**	**OCC**
IAC Input current reference	√	X
VFF feed forward filter	√	X
Multiplier Output	√	X
Current Amp Comp	√	X
Soft Start	√	√
Output Voltage Sensing & Comp	√	√
Current Sensing	√	√

CHAPTER 6

EXPERIMENTS ON POWER FACTOR CORRECTION

6.1 Objective

This chapter covers the experiments based on the power factor correction concept for single phase diode rectifiers. Implemented power factor correction system hardware is introduced first. Then the different experiment scenarios are built and some measurement results are illustrated. The experiments are prepared according to undergraduate and graduate curricula and are intended to help the user to understand the basics of power factor correction. All experiments are supported with connection diagrams, block schemes, measurement procedure and experimental results. The sequence of the experiments is chosen from basic to detail.

First, an experiment for a single phase diode rectifier with capacitive filter is maintained. The aim of this first experiment is to show the sources of current harmonics, results of these harmonic currents, international harmonic limiting standards and needs for power factor correction. Secondly, experiments based on the passive power factor correction solutions are maintained. Different combinations of the passive filter elements are made and experimental results are obtained. Three popular passive power factor correction methods are reviewed; L filter method, 3^{rd} harmonic filter method and variable inductor method (SAG). Finally, average current controlled active PFC circuit is analyzed in the experiment. Current and voltage waveforms are observed and the PF, efficiency of the system are obtained at different operating conditions. Also switching characteristics and the power loss analyses are made through the experiments. Connection of the systems, required measurement and test equipment and experiment results are given in detail in all experiments.

6.2 Background Information

Most of electronic devices consist of power converter as input stage to convert the 50 Hz or 60 Hz utility power to the required voltage level. Generally, these power converters use a diode rectifier with followed by a capacitive bulk filter to supply a DC voltage from utility grid. This simplest way to convert AC voltage to DC voltage has negative affects on mains. Unless some correction circuit is used, the input rectifier with a capacitive filter circuit will draw pulsating currents from the utility grid resulting in poor power quality and high harmonic contents that adversely affect other users. Combination of these low quality power supplies results non-negligible problems by the utility side. Power quality regulation companies and organizations defined various harmonic limiting standards to limit these black affects. So, all electronic equipment should obey the harmonic current limits defined by related standard. Through this experiment procedure, the student will become familiar with the importance of power factor correction (PFC) in single-phase diode rectifier by exploring some concepts related to standards, THD and PFC circuits.

Most of power supplies consist of AC\DC converter stages based on diode or thyristor rectifier circuits. Conventionally, for low power applications (such as PCs, TVs, home appliances, etc…) single-phase diode rectifiers are chosen owing to low cost and simple structure. The conventional input stage of an off-line switching power supply design is shown in Figure 6.1. The bulk filter capacitor reduces the ripple on the voltage waveforms into the DC converter stage. The problem with this input circuit is that it produces excessive peak input currents and high harmonic distortion on the line. The pulsating current waveform is rich of harmonics. This interval corresponds to the time when the mains instantaneous voltage is greater than the capacitor voltage. Since the capacitor must meet hold-up time requirements (during fault conditions, the mains are disconnected from the circuit for some cycles) its time constant is much grater than the frequency of the mains.

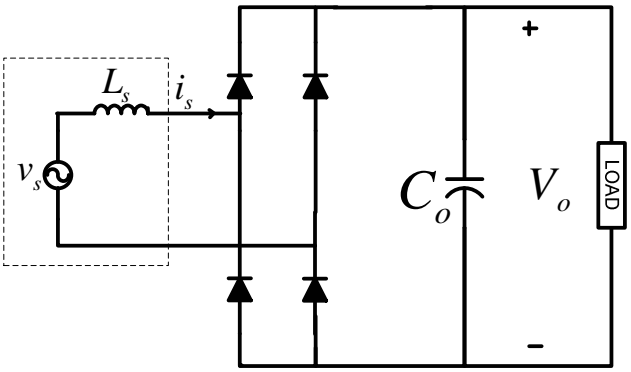


Figure 6.1 Single-phase diode rectifier with bulk capacitive filter.

The performance of the power converter is defined by the power factor (PF) of the circuit. Power factor shows how effectively energy is transmitted to load. It also represents a measure of distortion of the line voltage and line current and phase shift between them. PF has range between 0 and 1 and is defined as the ratio of the real power to the apparent power.

$$\text{Power Factor (PF)} = \frac{\text{Real Power (Average)}}{\text{Apparent Power}} \tag{6.1}$$

Diode rectifiers behave as nonlinear loads seen by the utility side. So the PF of a nonlinear load is defined by both displacement factor and distortion factor. Distortion factor describes harmonic content of the current. It shows the difference between fundamental component of the current and actual waveform.

$$PF = \frac{I_{1,rms}}{I_{rms}} \cos\varphi = k_{distortion} \cdot k_{displacement} \tag{6.2}$$

Overall performance of a single-phase diode rectifier that shown in Figure 6.1 can be best analyzed by evaluating the steady-state waveforms shown in Figure 6.2.

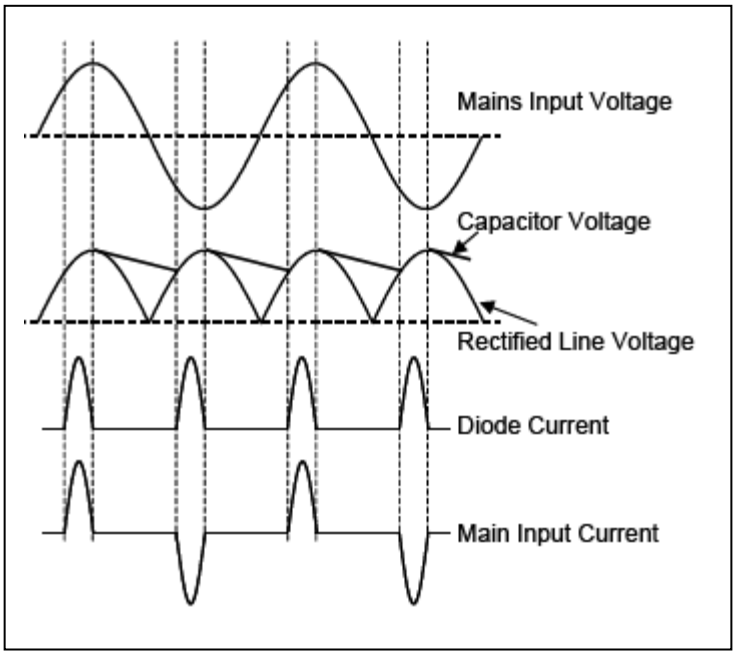


Figure 6.2 Waveforms for single-phase rectifier with capacitive smoothing.

Therefore, large pulses of current are drawn from the line over a very short period of time, as shown in Figure 6.2. The low-order current harmonics are quite large, close to that of the fundamental. The total harmonic distortion (THD) of the input current shows the distortion and crest factor of the current. Total Harmonic Distortion (THD) shows the ratio of the rms value of the waveform (not including the fundamental component) to the rms value of the fundamental component.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2}}{I_{1,rms}} \tag{6.3}$$

A general harmonic content and THD of single-phase diode bridge rectifier is given below in Figure 6.3.

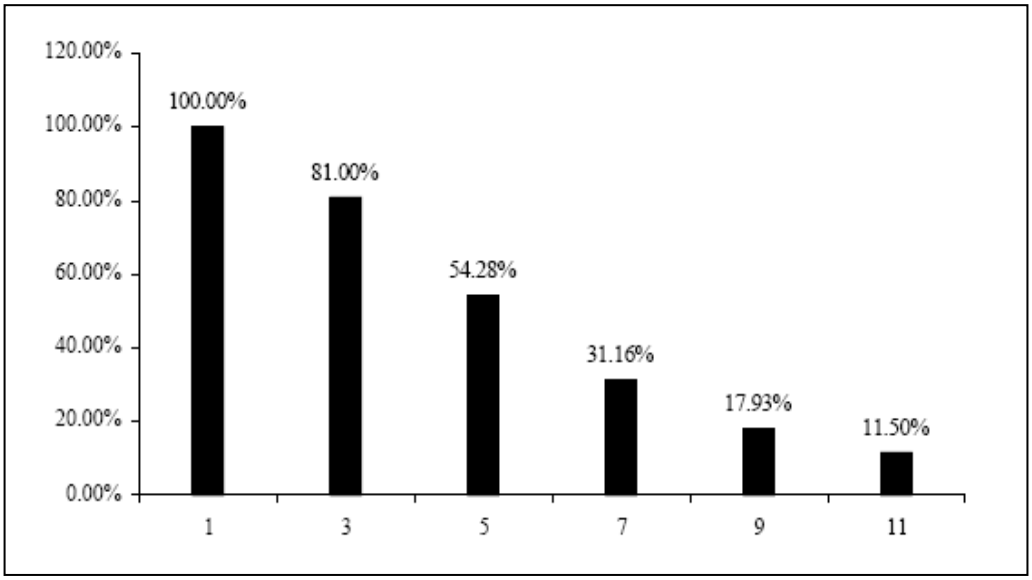


Figure 6.3 Input current harmonic spectrum for a single-phase rectifier with capacitive smoothing.

The diode bridge input circuit in a single-phase AC drive is the same as used in a very wide range of electronic equipment such as personal computers and domestic appliances. All of these cause similar current harmonics. Their effect is cumulative if they are all connected to the same low voltage (e.g. 230V) supply system. This means that to estimate the total harmonic current in an installation of single-phase units, the harmonics have to be added directly. These current harmonics result in waveform distortion on the mains. Current harmonics may interfere with other equipments and produce electromagnetic interference (EMI). The power utility requires over-dimensioning of parts. Another problem is that the power utility line cabling, the installation, and the transformer must all be designed to withstand these peak current values.

The harmonic polluting effects of conventional AC rectification must be limited and this is done in accordance with the standards of electricity utility network. To maintain power system quality, compliance requirements for current harmonic distortion are being enforced by national and international bodies. The EN 61000-3-2 standard defines measurement requirements, ac power source requirements and

limits for testing the harmonic current emissions of electronic and electrical equipment. After some changes, this standard applies to any equipment with rated current up to 16 A RMS per phase for 50-Hz, 230-V single-phase systems or 400-V three-phase mains network. There are 4 different class types for electronic equipments defined by the EN 61000-3-2 that have different limit values. The classification of electronic equipments is given in Table 6.1.

Table 6.1 Classification of electronic equipments by EN 61000-3-2 harmonic standard

Class-A	Balanced 3-phase equipment; household appliances excluding equipment identified as Class-D; tools (except portable), dimmers for incandescent lamp (but not other lighting equipment); anything not otherwise classified
Class-B	Portable power tools
Class-C	All lighting equipment except incandescent lamp dimmers
Class-D	Single phase, under 600 W, personal computer, PC monitor, TV receiver

Each class type has own harmonic current limits so a device should have lower input current harmonics than the limit values. The maximum allowable input current harmonics are listed in Table 6.2 for EN 61000-3-2 standard.

Table 6.2 Maximum harmonic limits for each class type defined by EN 61000-3-2

n	**Class A (A rms)**	**Class B (A rms)**	**Class C (% fun.)**	**Class D (mA/W)**
3	2.3	3.45	30PF	3.4
5	1.14	1.71	10	1.9
7	0.77	1.155	7	1.0
9	0.40	0.60	5	0.5
2	1.08	1.62	2	-
4	0.43	0.645	-	-
6	0.30	0.45	-	-
8<n<40	1.84/n	2.76/n	-	-

Compliance with related standard and improvements in the PF and harmonic distortion can be achieved by modifying the input stage of the off-line converter. The most important issue is finding optimum PFC solution according to needed application. Generally, two PFC approaches are commonly used in current power supply products with high power features, i.e., passive approach and active PFC approach. Each one has its merits and limitations and applicable field.

Passive PFC approaches are used in low-power, low-cost applications. In the passive PFC approaches, passive elements are used to improve the power quality of the power circuit. Passive elements like inductors and capacitors are placed at the inputs or outputs of the diode bridge rectifier in order to improve current waveform. Passive PFC method is simple and low cost but has bulky size and heavy weight and low power factor. Generally, line frequency LC filters are used as a passive solution. The simple passive filter with LC components is shown in Figure 6.4.

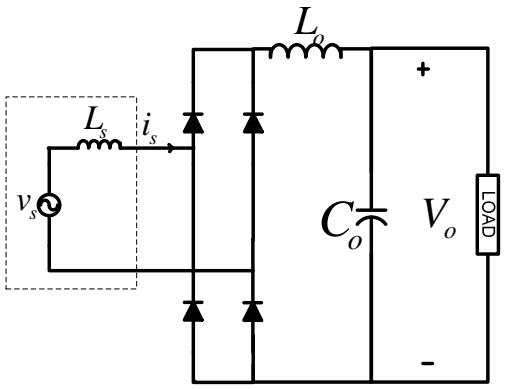


Figure 6.4 Simple passive PFC circuit.

For example, with a large DC filter inductor, the single-phase full-wave rectifier produces a square wave line current waveform, attaining a PF of 90% and 48% THD. With smaller values of inductance, these achievements are degraded. Through the experiments, three popular passive power factor correction methods are reviewed; L filter method, 3rd harmonic filter method and variable inductor method (SAG) in experiments 1, 2, 3 and 4 respectively.

Active solutions are used at high power levels with high PF and low harmonic distortion. Active PFC circuits shape the input current into a sinusoidal form in phase with line voltage. Besides they provide a regulated dc output voltage. Generally power factor of active PFC circuits is close to unity with lower input current THD around 3 %. Active PFC circuits have small size but these systems have higher manufacturing cost and complexity. Generally, a diode rectifier cascaded with a dc-dc converter build an active PFC system. The PFC stage can be a boost, buck/boost or fly back or can be any other power converter topology. Generally, the boost type topology shown in Figure 6.5 is so far the most popular configuration.

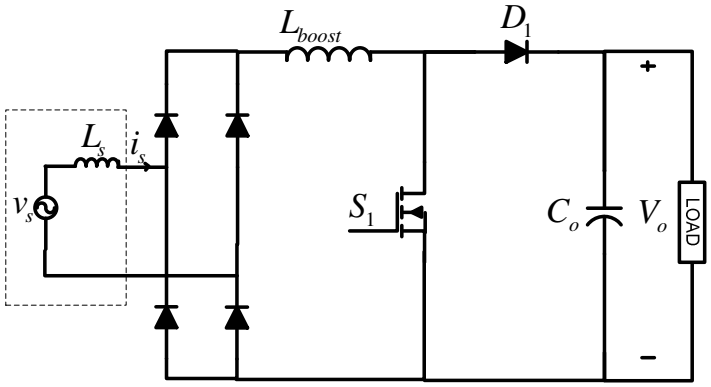


Figure 6.5 Boost type active PFC.

The function of this converter is to behave as an ideal resistive load for the output of the diode rectifiers in order to eliminate the generation of line current harmonics. Due to this characteristic, the converter is also known as a *power factor pre-regulator* or *resistor emulator*. Average current mode controlled single-phase active power factor circuit is analyzed in the experiment 5.

6.3 Components of the Experimental System

The user can see the performance of a single-phase rectifier circuit with or without power factor correction and can discuss the compliance to the standard of each PFC solution by this experimental system. The complete experiment system is shown in Figure 6.6.

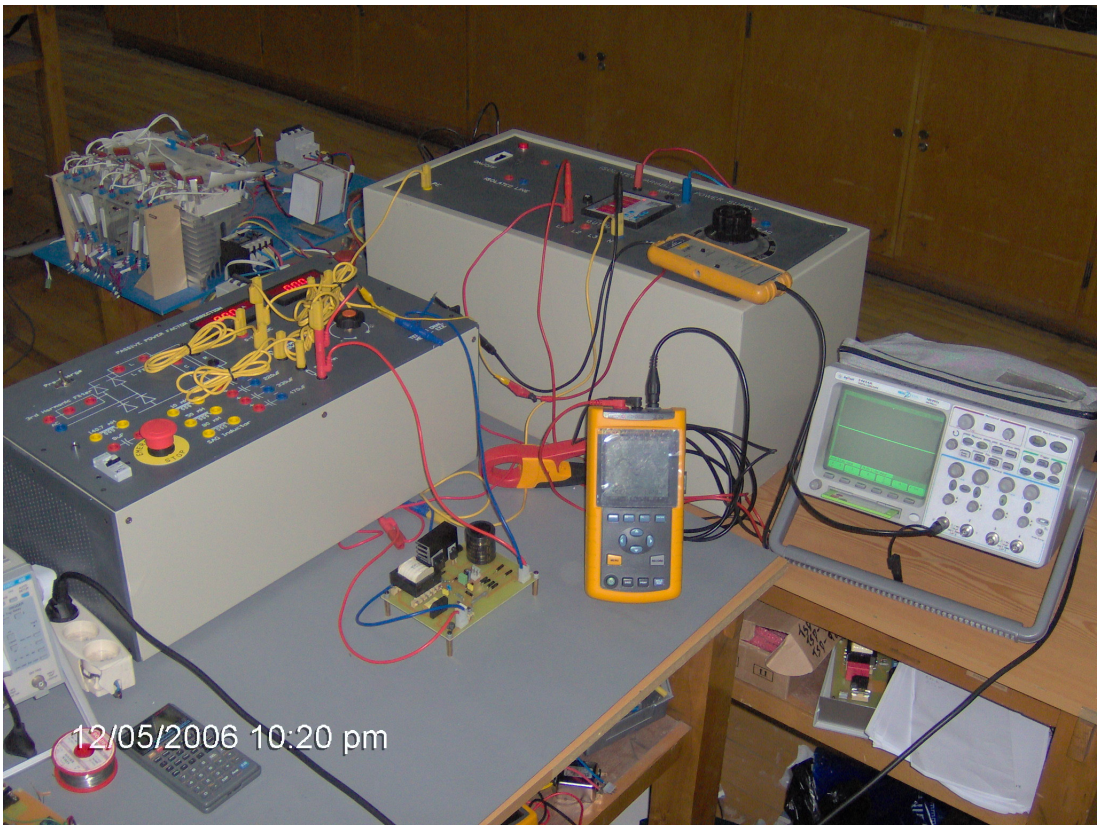


Figure 6.6 Experiment system for single-phase power factor correction.

6.3.1 Isolated AC Power Supply

Isolated AC variable power supply can be used to simulate the input voltage connections of the power factor correction systems. This unit consists of an isolation transformer, a variac and an energy analyzer. The isolation transformer isolates the connected PFC system from the utility grid. The variac has capability of adjustable 0- 265V AC voltage output. This variac can simulate different input voltage level of

the active power factor correction circuits. The universal line operation and duty cycle variation of the active PFC circuits can be tested by changing the input voltage level. The energy analyzer has free input and output terminals. The voltage output such as isolated or variac output can be connected to the inputs of the energy analyzer and the output of the energy analyzer can be connected to the device under test. The front view of the isolated adjustable AC power supply is given in Figure 6.7.

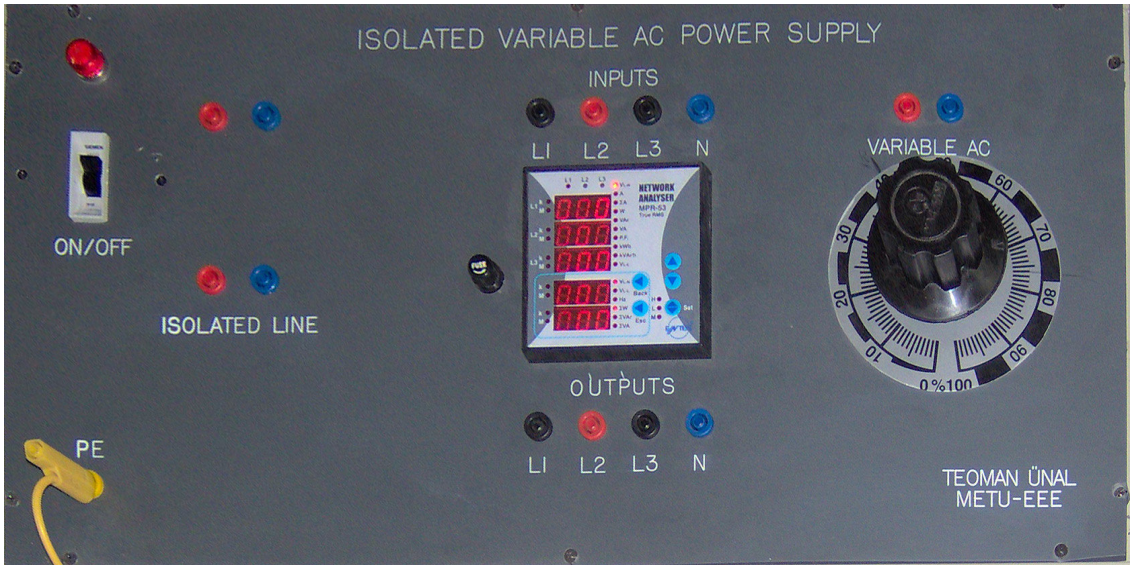


Figure 6.7 Isolated, variable AC power supply.

The specifications of the AC power supply are given below:

- Single Phase Power line output
- Isolated single phase output, 2kW
- Variable single phase output, 0-265V AC, 2kW
- 3-Phase energy meter, line-to-line, line-to-neutral voltage and current measurements, active, reactive and total power measurements, PF, THD and frequency measurements.
- Fuse protected, LED indicated front view, durable metal cover.

6.3.2 Passive Power Factor Correction System

The passive power factor correction unit is built to make easy combination of different passive elements with single-phase diode rectifier in order to carry out passive power factor correction experiments. The inputs and outputs of the single-phase diode rectifier are ready to connect any passive filter and measurement elements. The unit has single-phase diode rectifier, inductances and capacitances for passive filtering solutions, DC voltmeter and ampermeter for measurements, constant and variable resistors for loading the system. The front view of the passive power factor correction unit is given in Figure 6.8.

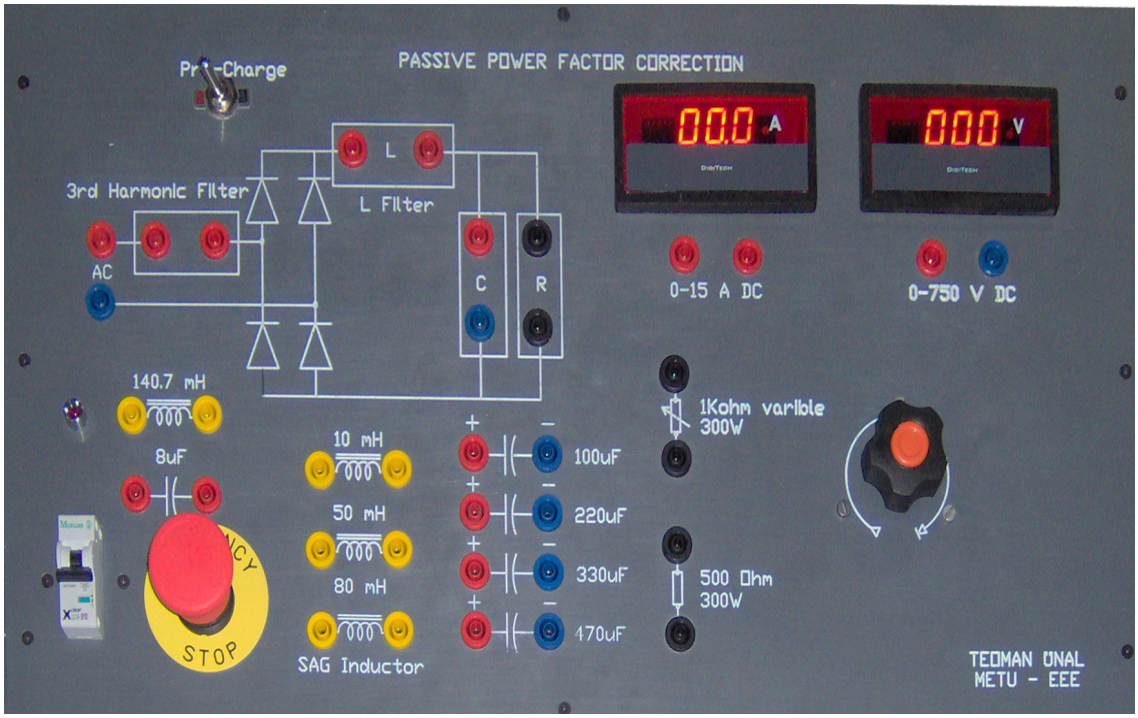


Figure 6.8 Passive power factor correction unit.

The components of the passive PFC unit are:

- Single-phase diode rectifier, IRF GBPC25 (400V, 25A)
- Pre-charge
- Filter Inductances

- 10 mH, 3 A, filter inductance for Class A applications
- 50 mH, 3 A, filter inductance for Class D applications
- 80 mH, 3 A, variable inductance filter (SAG) for Class D applications
- 140.7 mH, 3 A, filter inductance for 3rd harmonic input filter

- Capacitances
  - 100 μF, Electrolytic capacitor
  - 220 μF, Electrolytic capacitor
  - 330 μF, Electrolytic capacitor
  - 470 μF, Electrolytic capacitor
  - 8 μF, AC capacitor for 3rd harmonic filter
- Resistive loads
  - 1kΩ, 300 W, adjustable resistive load
  - 500Ω, 300 W, constant resistive load
- Measurement Devices
  - 0-15 A, DC digital ampermeter
  - 0-750 V, DC digital voltmeter
- Emergency stop, fuse protection

6.3.3 Active Power Factor Correction System

Average current mode controlled active PFC circuit is designed to be used in the experiments. The input and output connections, measurement points are made by connectors. The user should combine the isolated, variable AC power supply as an input and a resistive load as an output. The resistive loads in the passive PFC unit can be used as load of this active PFC circuit. Average current mode controlled active PFC circuit is shown in Figure 6.9. The circuit PCB layout and detailed circuit schematic are shown in Figures 6.10 and 6.11 respectively. The component list is given in Table 6.3.

Figure 6.9 Active power factor correction circuit.

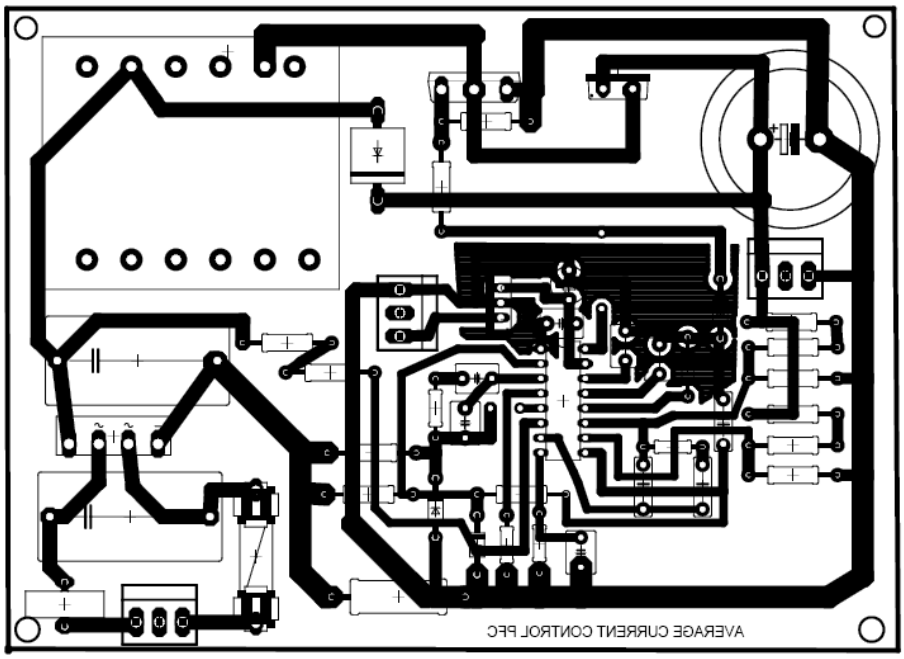


Figure 6.10 Circuit layout.

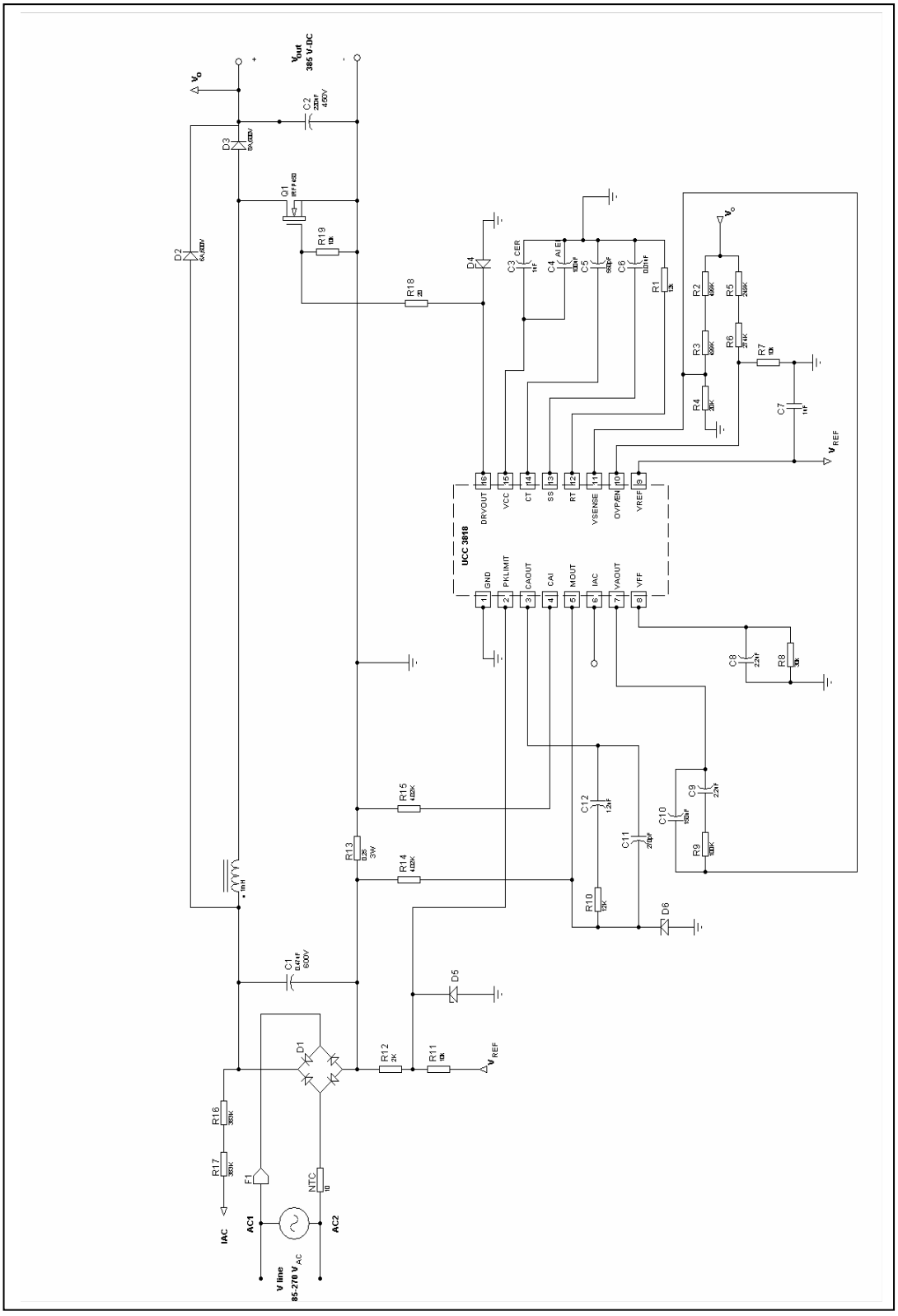


Figure 6.11 Schematic diagram of 250W average current control PFC.

Table 6.3 Bill of materials

	Reference	Qty	DESCRIPTION	Part Number - Manufacturer
Capacitors	C1	1	0.47 µF, 600 V	WIMA
	C2	1	220 µF, 450 V electronic, low ESR	KANDEIL
	C3	2	1 µF, 50 V, ceramic	
	C4	1	100 µF, 25 V, electronic	
	C5	2	560 pF, 50 V, ceramic	
	C6	1	0.01 µF, 50 V, ceramic	
	C7	1	1 µF, 50 V, ceramic	
	C8	1	2.2 µF, 50 V, ceramic	
	C9	2	2.2 µF, 50 V, ceramic	
	C10	1	150 nF, 50 V, ceramic	
	C11	1	270 pF, 50 V, ceramic	
	C12		1.2 nF, 50 V, ceramic	
Diodes	D1	1	8 A, 600 V, bridge	
	D2	1	8 A, 600 V, 400 A surge	
	D3	1	14 A, 600 V, ultra fast diode,35ns	IXYS DSEI12-06A
	D4	4	1 A, 40 V, schottky	1N5819
	D5	1	1 A, 40 V, schottky	1N5819
	D6	1	1 A, 40 V, schottky	1N5819
Fuses	F1	1	6 A, 250 V glass fast acting type	
Inductors	L1	1	1 mH, 6.5 A Boost inductor	Coil-Craft N2880-AL
MOSFETs	Q1	1	600V, 10A	IR - IRFP450
Resistors	R1	1	12 kΩ, 1/4 W	
	R2, R3	1	20 kΩ, 1 W	
	R4	1	20 kΩ, 1/4 W	
	R5	2	249 kΩ, 1 W	
	R6	1	274 kΩ, 1 W	
	R7, R11	1	10 kΩ, 1/4 W	
	R8	1	30 kΩ, 1/4 W	
	R9	2	100 kΩ, 1/4 W	
	R10, R19	1	12 kΩ, 1/4 W	
	R12	2	2 kΩ, 1/4 W	
	R13	1	0.25 Ω, 5 W sense resistor	
	R14, R15	2	4.02 kΩ, 1/4 W	
	R16,R17	1	383 kΩ, 1 W	
	R18	1	20 Ω, 1/4 W	
IC's	U1	1	Average current mode PFC controller IC	TI UCC3818N

The following experiment can be carried out by using the experimental system and measurement devices.

- Observing waveforms for input current, input voltage and output voltage waveforms.
- Obtaining power factor (PF) vs. output power (P) graphics
- Start-up response, transient response and hold-up time characteristics
- Power elements' switching characteristics

6.4 Required Measurement Equipment

The following measurement and test equipment is required to maintain the experiments related to power factor correction.

- AC voltmeter, min. 400V AC
- DC Voltmeter, min 600V DC
- AC Ampermeter, min 10 A AC
- DC ampermeter, min 10 A DC
- Wattmeter
- 2-channel, 80MHz, digital storage oscilloscope with higher sampling rate
- Differential voltage probes
- Magnetic, high bandwidth current probes
- Single phase power analyzer, recommended Fluke 43B power quality analyzer
- Connection cables, AC power cables

6.5 Safety

The experiments discussed here are designed for lower than 250 W power levels and safety concerns are minimized. The user should make proper connections and show extra care while performing the experiments. Since the user will work with potentially higher levels of the input and output voltages, all safety precautions should be taken before or during experiments.

Do not touch any part of the circuits (power stage or control) when the circuits are connected to the AC sources and are up and running. Also, be extremely careful when connecting measuring equipment to the circuit. Make all the necessary connections when the AC source is turned off. All voltage and current measurements should be done using isolated measurement probes. Differential voltage probes should be used in voltage measurements while performing current measurements by a magnetic current probe.

The load resistances are rated to maximum 300 W power rating. The maximum output power of the circuits must not exceed this level. Also, the user should follow the heat on these resistors. In the case of overheat on these resistors, the system should be turned off and the user must wait until these loads get cold. An NTC is placed to the input of the active PFC circuit to limit the inrush current. The NTC should be cold while starting the system. Fast acting fuses and emergency stop buttons are placed to protect the system.

6.6 Experiment 1 – Single-Phase Diode Rectifier with Capacitive Filter

6.6.1 Introduction

This experiment is intended to show the basic behaviors of the single-phase diode rectifier with capacitive filter. It is commonly used that single-phase diode rectifiers with capacitive filter are used mainly in the SMPS applications as an input stage. These circuits have black effects in the mains such as higher harmonic content input current.

In this experiment, the input current characteristics of single-phase diode rectifier with different output capacitive filters will be analyzed. Also output voltage and current waveforms will be observed. The PF, THD and efficiency of the circuit will be measured and compliance with the IEC 61000-3-2 harmonic current standard will be analyzed.

6.6.2 Demonstrations Circuits

For this demonstration, isolated AC power source and passive power factor correction units will be used. The input and output filter connection terminals of the single-phase diode rectifier will be shorted and only a capacitive filter and resistive load will be connected to the output of the diode rectifier. Input characteristics will be analyzed by single-phase power quality analyzer and output characteristics will be analyzed by DC ammeter and voltmeter and oscilloscope with differential voltage probe.

6.6.3 Procedure

1. Connect the isolated 220 V AC source to the input terminals of the single-phase diode rectifier. Short all external filter connections of the diode rectifier. Take the pre-charge switch to ON position.

2. Make the required connections with the following experiment parameters given in Table 6.4. Complete connection diagram of the circuit is illustrated in Figure 6.12.

Table 6.4 Single-phase diode rectifier experiment parameters.

Output Capacitor	330 μF
Input Voltage (V_{rms})	230 V
Output Power	200 W
R load	480 Ω

Input current and voltage waveforms are measured by single-phase power quality analyzer. The output voltage waveform will be observed by a differential voltage probe.

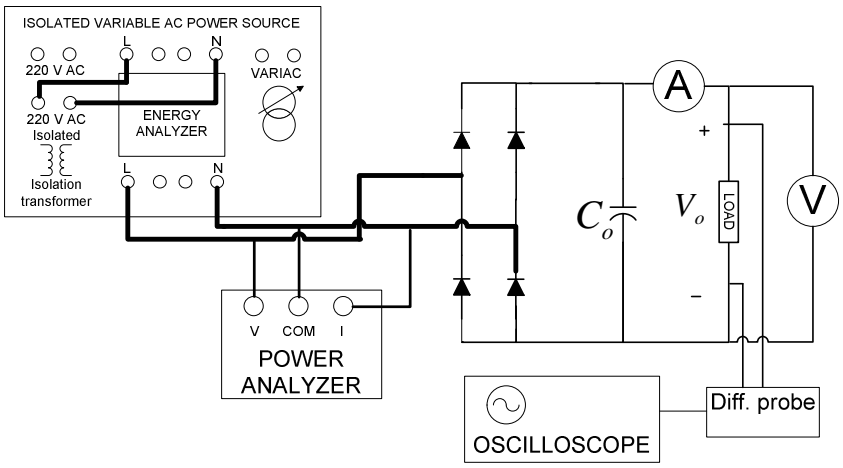


Figure 6.12 Single Phase diode rectifier test circuit.

3. Turn on both power switch in power supply and passive power factor correction unit. After 3-4 seconds, take the pre-charge switch to the OFF position. Observe input voltage and current waveforms in the scope screen of single-phase power quality analyzer. Observe input current harmonics in the harmonic screen. Note PF, THD, voltage and current values, harmonic current values. The measured waveforms are illustrated in Figure 6.13.

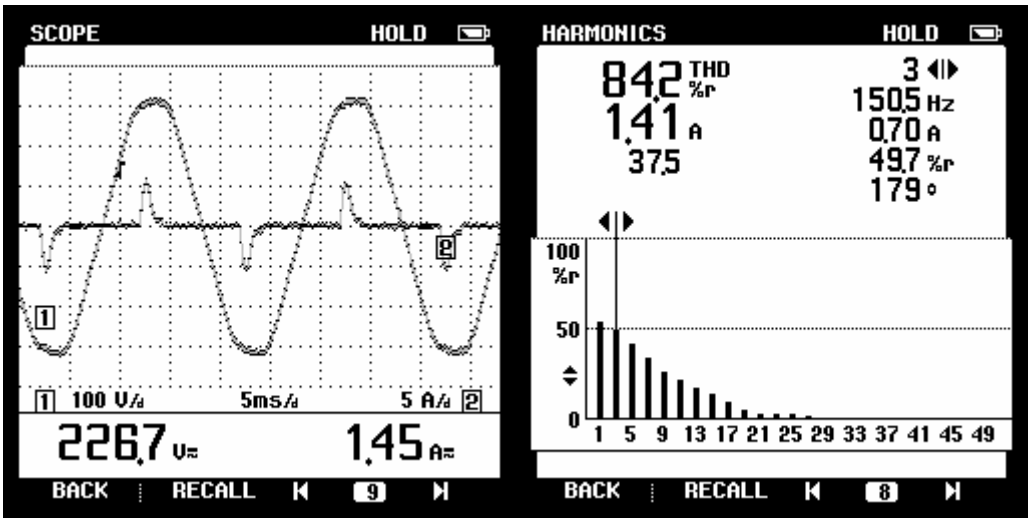


Figure 6.13 a) Input voltage and Current waveforms b) Input current harmonics.

Measure the output voltage and current DC values and prepare a table consisting of all collected parameters of the experimental circuit as follows.

Table 6.5 Measurement results for single-phase diode rectifier experiment

V_{in}	I_{in}	P_{in}	V_o	I_o	P_o	THD	I_{fund}	I_{3th}	I_{5th}	PF
226Vrms	1.47Arms	200W	302Vdc	0.6A	180W	85%	0.77A	0.7A	0.6A	0.52

4. Change the output capacitance values to 100uF. Make all measurements mentioned step 3.

5. By the help of a differential probe and oscilloscope, observe the output voltage waveforms and hold-up time for both different output capacitance values. The output voltage waveforms are given in Figure 6.14.

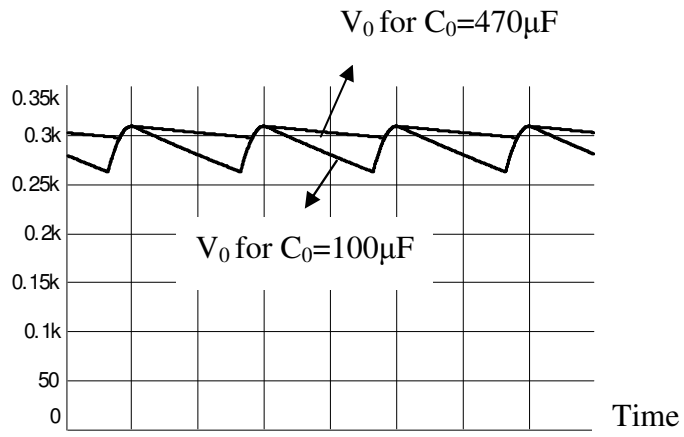


Figure 6.14 Output voltage waveforms for different capacitance values.

6.6.4 Study Questions

1. Discuss the main causes of harmonic currents and the effects on the utility side. Why is harmonic current limiting standard applied? Analyze the IEC 61000-3-2 current harmonic limiting standard and see how the equipments are classified and what the maximum allowable current harmonics limits are for each class type.

2. Comment on the harmonic current levels for different capacitance values. Also comment on the output voltage waveforms and hold-up time. If the load is a constant power load such as a dc-dc converter, what qualifications should the output voltage have?

3. Are current harmonic levels the same at the equipment near the utility supply with the equipment far away from utility supply? Explain why.

6.7 Experiment 2 – L Type Passive Filter

6.7.1 Introduction

In this experiment, the harmonic current eliminating method by an inductive filter is analyzed. An inductor is placed at the output of the single-phase diode rectifier. The conduction time for the rectifier diodes are increased by this inductive filter. Required minimum inductance for passive power factor correction that complies with the IEC 61000-3-2 harmonic limiting standard is analyzed. The graphics of the required minimum inductance versus power for Class A and Class D equipment are shown in Figure 6.15 and 6.16, respectively. It is shown that, different class types have different harmonic current limits so the required minimum inductance value differs for different classes.

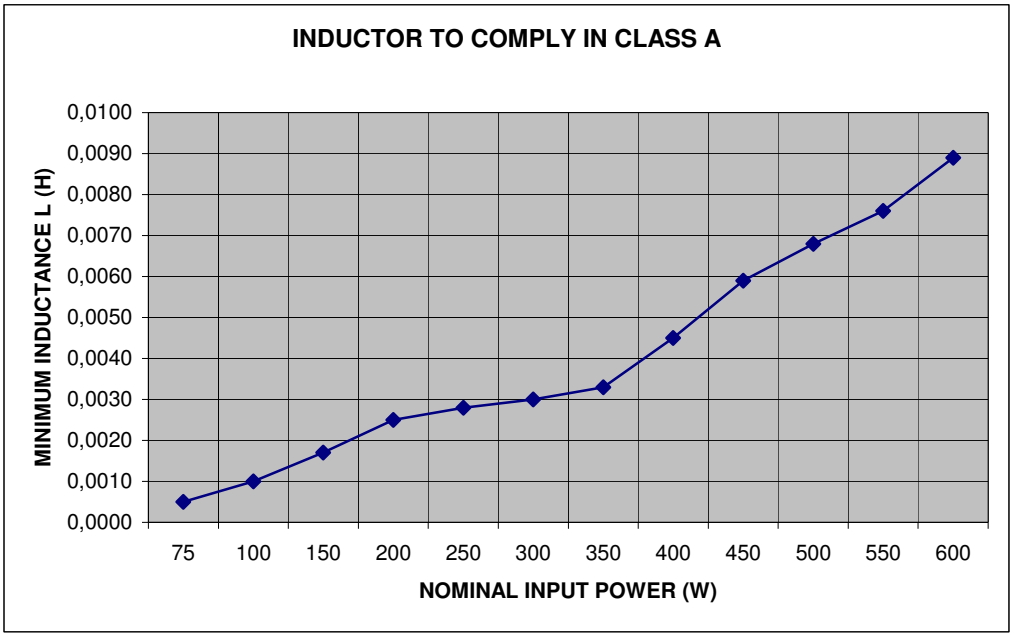


Figure 6.15 Minimum required inductance to comply with EN 61000- 3-2 Class A harmonic limits.

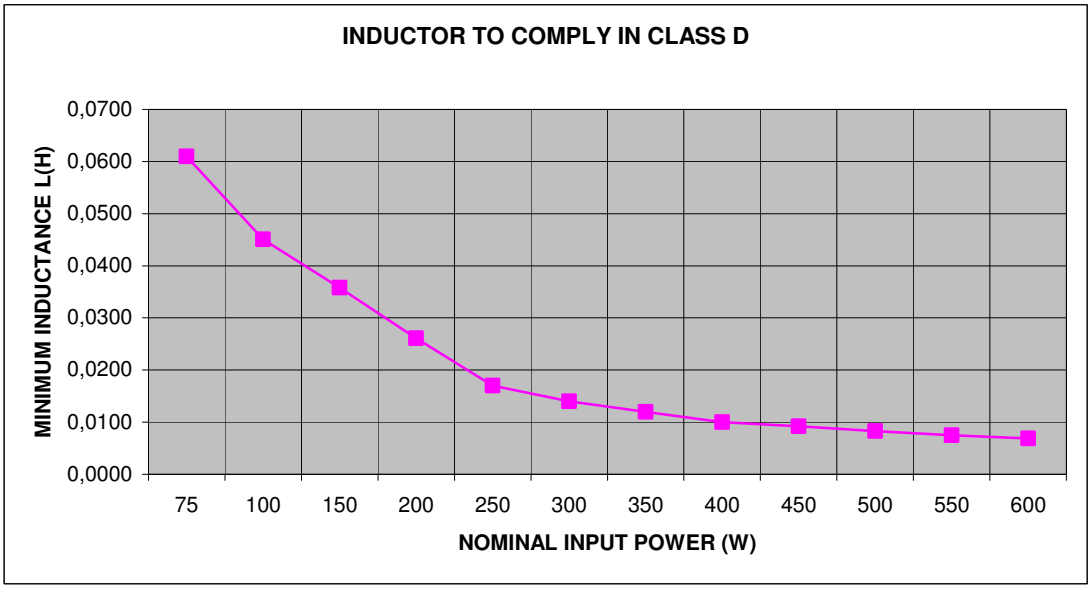


Figure 6.16 Minimum required inductance to comply with EN 61000- 3-2 Class D harmonic limits.

Two different experiment scenarios are devised assuming operating at different class type equipment (Class A and Class D). First, 200W, Class A type single-phase diode rectifier with inductive filter is analyzed. Then, 200W, Class D type single-phase diode rectifier with inductive filter is analyzed. The filter inductance values are chosen according to minimum required inductance values for each class. Also, for each class type, the power level is applied to show the usage at different power levels.

6.7.2 Procedure

1. Connect the isolated 220 V AC source to the input terminals of the single-phase diode rectifier. Short all external filter connections of the diode rectifier except L filter connection at the output. Take the pre-charge switch to ON position.

2. Make the required connections with the following experiment parameters. Complete connection diagram of the circuit is illustrated in Figure 6.17.

Table 6.6 Experiment parameters for 100W L filter application - Class A.

Input Power	100 W
Input Voltage (V_{rms})	230 V
R load	870 Ω
Filter inductance	10 mH
Output Capacitor	330 μF

10 mH inductor is enough to operate at both 100W and 200W class A applications.

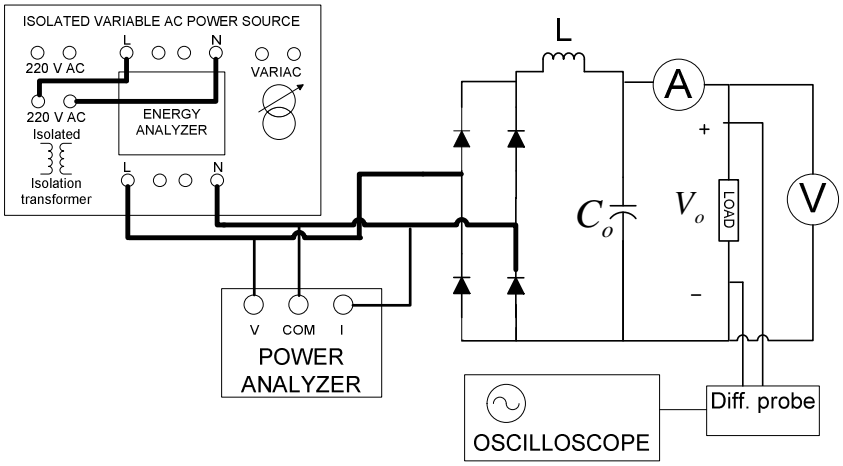


Figure 6.17 Single phase diode rectifier with L filter test circuit.

3. Turn on both power switch in power supply and passive power factor correction unit. After 3-4 seconds, take the pre-charge switch to the OFF position. Observe input voltage and current waveforms on the scope screen of single phase power quality analyzer. Observe input current harmonics on the harmonic screen. Note PF, THD, voltage and current values, harmonic current values and make a table. The measured input current and voltages are illustrated in Figure 6.18.

Table 6.7 Measurement results for 100W single-phase diode rectifier L filter experiment

V_{in}	I_{in}	P_{in}	V_o	I_o	P_o	THD	I_{fund}	I_{3th}	I_{5th}	PF
224Vrms	0.63A	100W	295Vdc	0.3A	88W	70%	0.44A	0.34A	0.21A	0.69

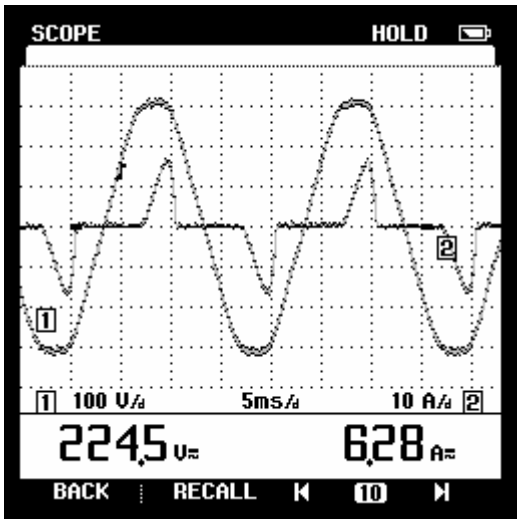


Figure 6.18 Input voltage and current waveforms for 100W Class A with 10mH inductive filter (Scales: 100V/div, 2A/div).

Measure the input current harmonic values and compare with the limit values stated in the IEC 61000-3-2. The comparison graphic is shown in Figure 6.19.

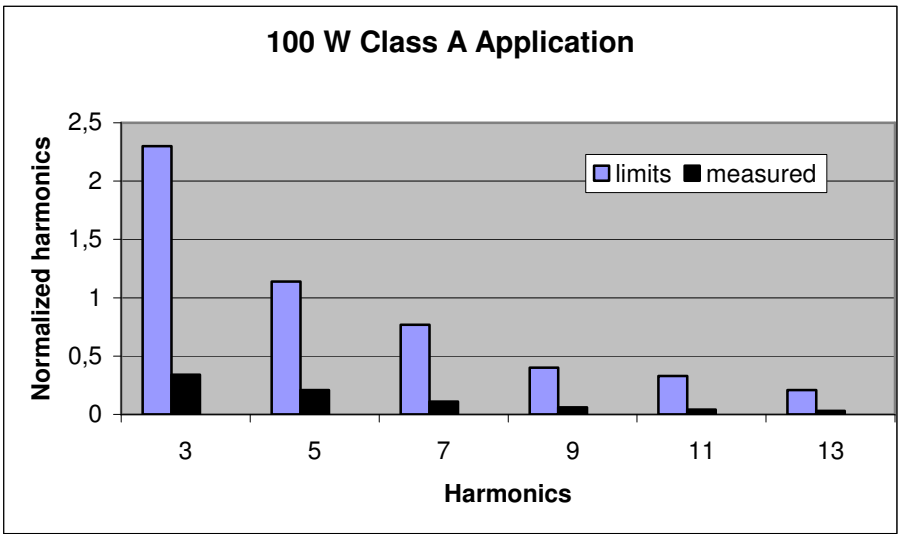


Figure 6.19 Harmonic spectrums for input current for Class A – 100W.

4. Adjust the input power to 200W by changing the load resistor approximately to 480 Ω. Measure the input current and harmonic spectrum. Also make the same measurements mentioned in step 3.

Table 6.8 Measurement results for 200W single-phase diode rectifier L filter experiment

V_{in}	I_{in}	P_{in}	V_o	I_o	P_o	THD	I_{fund}	I_{3th}	I_{5th}	PF
224Vrms	1.14A	200W	290Vdc	0.65A	188W	66%	0.88A	0.66A	0.35A	0.79

The measured input current waveform and harmonic spectrum are shown in Figure 6.20 and 6.21, respectively.

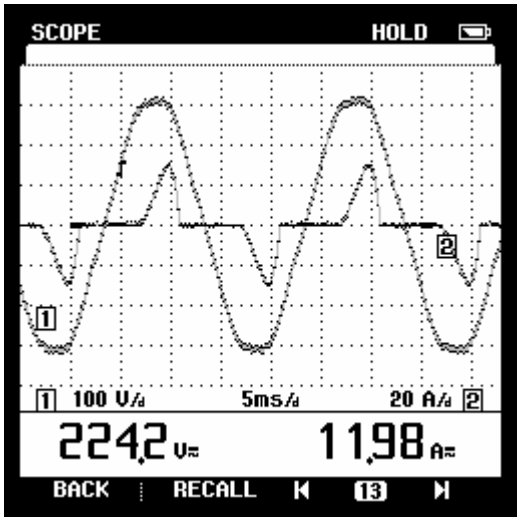


Figure 6.20 Input voltage and current waveforms for 200W Class A with 10mH inductive filter (Scales: 100V/div, 2A/div).

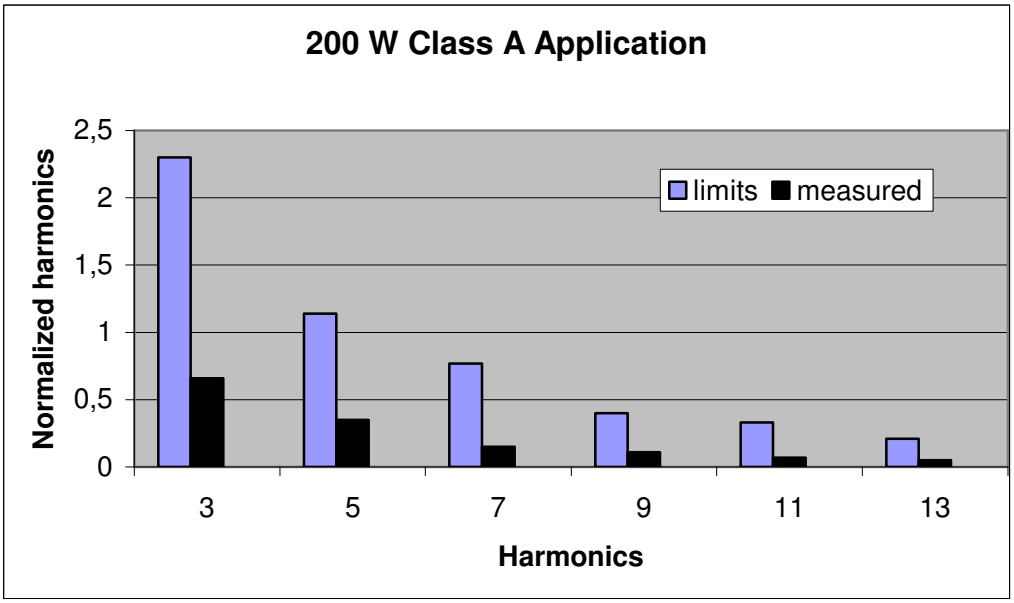


Figure 6.21 Harmonic spectrums for input current for Class A – 200W.

5. Now consider the operation with equipment belonging to Class D type. It is clear from Figure 6.16 that, a 50mH filter inductance is enough for both 100W and 200W applications. Replace the filter inductance with a 50mH inductor. Make the necessary measurements mentioned in steps 3 and 4 for both 100W and 200W power levels. The experiment parameters are given in Table 6.9.

Table 6.9 Experiment parameters for L filter application - Class D

Input Power	100 W	200 W
Input Voltage (V_{rms})	230 V	230 V
R Load	770 Ω	380 Ω
Filter inductance L	50 mH	50 mH
Output Capacitor	330 µF	330 µF

The input current waveforms for different power levels are shown in Figures 6.22.a and 6.22.b.

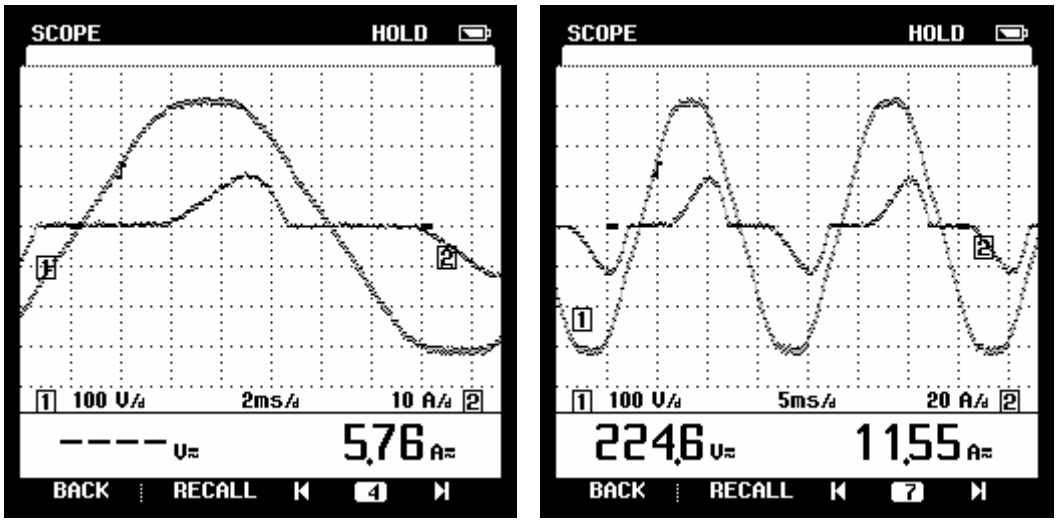


Figure 6.22 Measured input voltage and current for Class D a) 100W (Scales: 100V/div, 1A/div) b) 200W (Scales: 100V/div, 2A/div).

The evaluated input current harmonic spectrum and corresponding standard limits are shown in Figure 6.23 and 6.24.

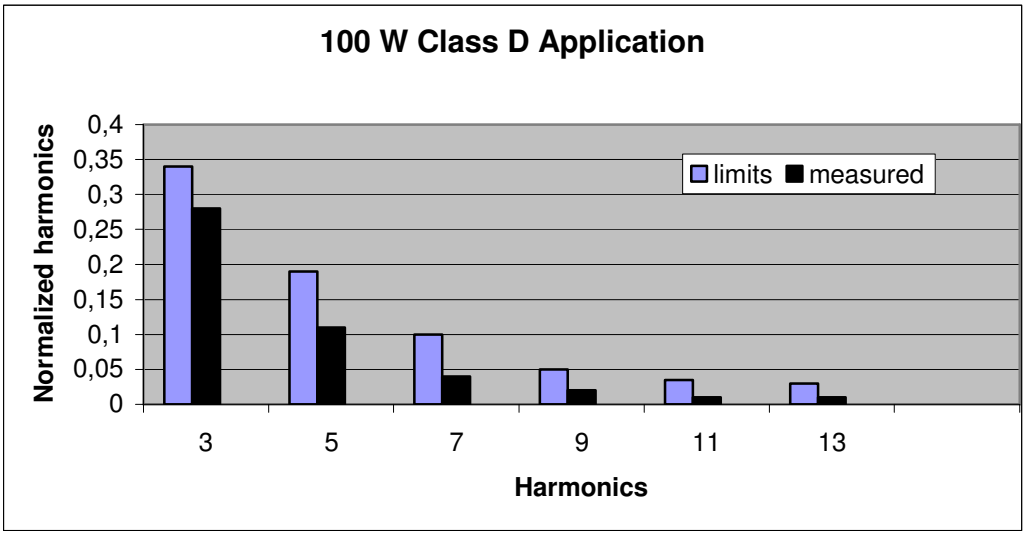


Figure 6.23 Harmonic spectrums for input current for Class D – 100W.

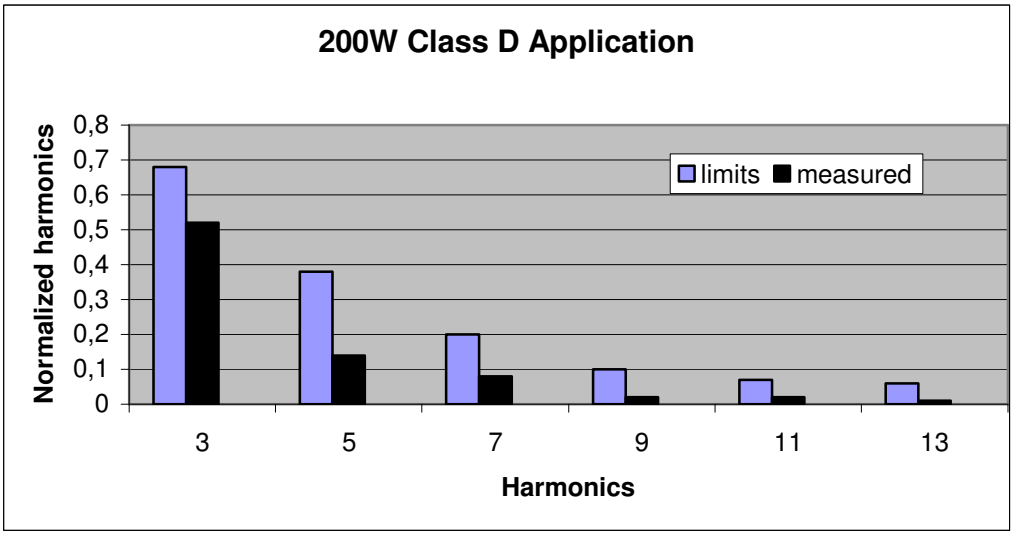


Figure 6.24 Harmonic spectrums for input current for Class D – 200W.

6.7.3 Study Questions

1. What are the advantages and disadvantages of passive power factor correction solutions? Consider design complexity, usage, manufacturing and total cost, size and weight.

6.8 Experiment 3– Series Connected Parallel Resonant Filter (3rd Harmonic Filter)

6.8.1 Introduction

The 3rd harmonic is dominant in the single-phase diode rectifier with capacitive filter. The power factor of the circuit can be improved by removing 3rd harmonic currents. This can be done by connecting a tuned resonant filter to the input of the diode rectifier. The operating principle of the circuit is discussed in section 2.2.2. In this experiment, a series connected parallel resonant filter will be analyzed. Current waveforms will be observed. The PF, THD and efficiency of the circuit will be measured and compliance with the IEC 61000-3-2 harmonic current standard will be investigated.

6.8.2 Procedure

1. Connect the isolated 220 V AC source to the input terminals of the single-phase diode rectifier. Short L filters connection in the output. Take the pre-charge switch to ON position.

2. Make the required connections with the following experiment parameters. Complete connection diagram of the circuit is illustrated in Figure 6.25.

Table 6.10 Experiment parameters for 3rd harmonic filter

Filter Inductance L_r	140.7 mH
Filter Capacitance C_r	8 μF
Input Voltage (V_{rms})	230 V
Input Power	150 W
R load	530 Ω
Output Capacitance C_o	330 μF

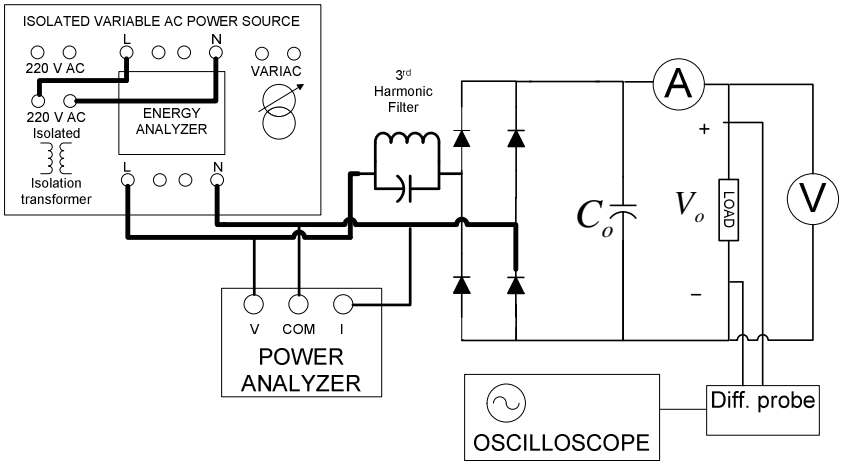


Figure 6.25 Single phase diode rectifier with 3rd harmonic filter test circuit.

3. Turn on both power switch in power supply and passive power factor correction unit. After 3-4 seconds, take the pre-charge switch to the OFF position. Observe input voltage and current waveforms in the scope screen of single phase power quality analyzer. Observe input current harmonics in the harmonic screen. Note PF, THD, voltage and current values, harmonic current values and prepare a table.

Table 6.11 Measurement results for 150W single-phase diode rectifier 3rd harmonic filter experiment

V_{in}	I_{in}	P_{in}	V_o	I_o	P_o	THD	I_{fund}	I_{3th}	I_{5th}	PF
229Vrms	0.69A	150W	272Vdc	0.5A	136W	40%	0.62A	0.11A	0.17A	0.66

Measure the harmonic current values and compare with harmonic current standard limits for class A and class D types.

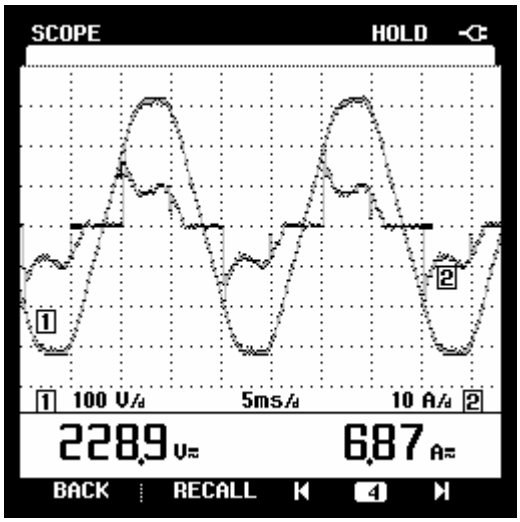


Figure 6.26 Current of 3rd harmonic filter for 150W system (Scales: 100V/div, 1A/div).

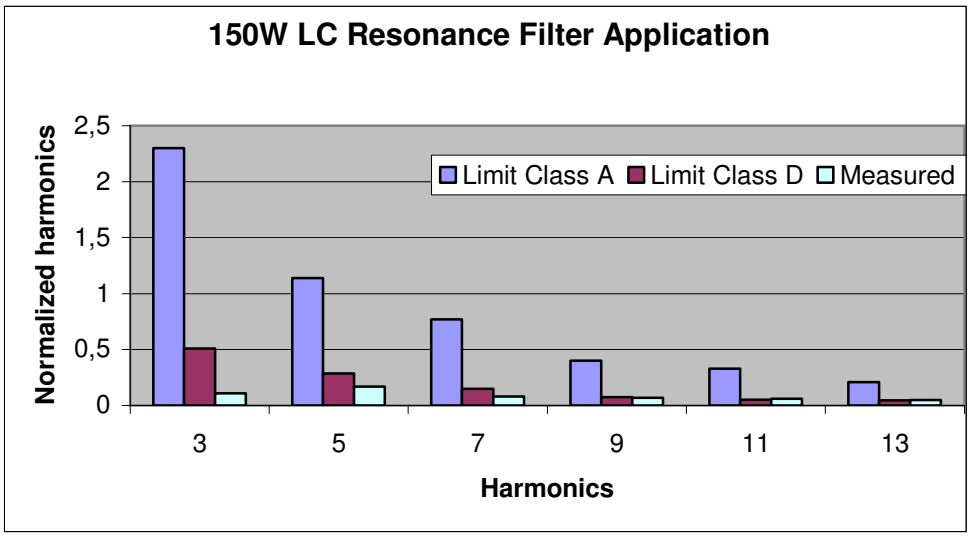


Figure 6.27 Harmonic spectrums for input current for 150W 3rd harmonic filtered single phase diode rectifier.

6.8.3 Study Questions

1. Considering the measured higher order harmonics, does the 3rd harmonic filter method fully comply with IEC 61000-3-2 harmonic limiting standard?

2. Is it possible to design a complete 3rd harmonic tuned filter? Consider the tolerances, losses and non-linearity of the passive elements.

3. Why isn't the 3rd harmonic component completely removed? Compare the circuit with an unfiltered single-phase diode rectifier circuit and explain the reasons for the boosts in the higher order harmonics considering the resonance concept.

6.9 Experiment 4– Variable Inductance (SAG Inductor) Method

6.9.1 Introduction

A filter inductor that covers all power levels for Class D applications has higher size and weight due to the higher inductance and higher energy level. It is possible to make smaller inductance that is suitable for passive power factor correction. This can be achieved by operating the inductance in saturation region. A variable air-gap inductor, called as sloped Air-Gap (SAG), can be used for this purpose and has different inductances for different current levels. In this experiment, the operation of a SAG inductor with single-phase diode rectifier is analyzed.

6.9.2 Procedure

1. Connect the isolated 220 V AC source to the input terminals of the single-phase diode rectifier. Take the pre-charge switch to ON position.

2. Make the required connections with the following experiment parameters. Complete connection diagram of the circuit is illustrated in Figure 6.28.

Table 6.12 Experiment parameters for variable inductance filter application

Input Power	200 W
Input Voltage (V_{rms})	230 V
R load	380 Ω
Filter inductance	80 mH (SAG)
Output Capacitor	330 μF

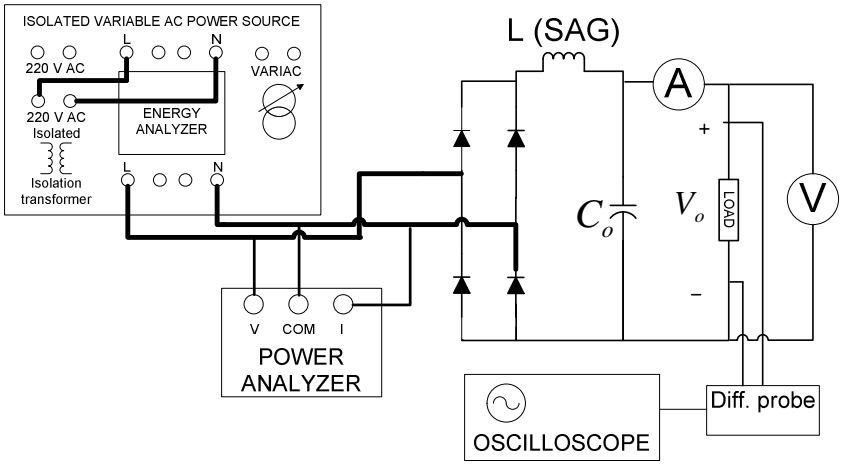


Figure 6.28 Single phase diode rectifier with variable inductance filter test circuit.

3. Turn on both power switch in power supply and passive power factor correction unit. After 3-4 seconds, take the pre-charge switch to the OFF position. Observe input voltage and current waveforms on the scope screen of single-phase power quality analyzer. Observe input current harmonics on the harmonic screen. Note PF, THD, voltage and current values, harmonic current values and prepare a table.

Table 6.13 Measurement results for single-phase diode rectifier SAG filter experiment

V_{in}	I_{in}	P_{in}	V_o	I_o	P_o	THD	I_{fund}	I_{3th}	I_{5th}	PF
228Vrms	1.11A	200W	262Vdc	0.7A	183W	42%	0.98A	0.45A	0.13A	0.8

The measured input current waveform and harmonic spectrum are shown in Figures 6.29 and 6.30 respectively.

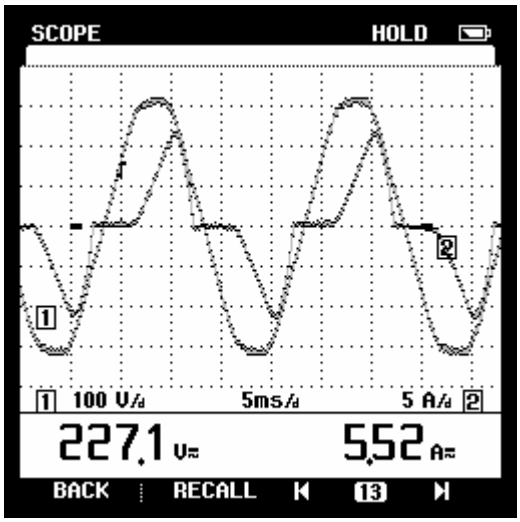


Figure 6.29 Experimental results for input voltage and current (Scales: 100V/div, 1A/div).

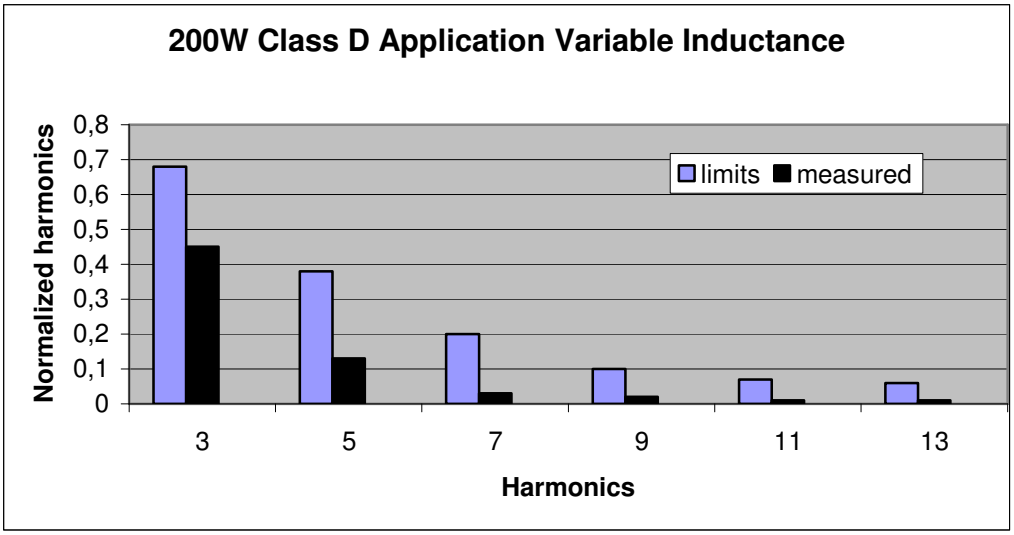


Figure 6.30 Input current harmonics for 200W Class-D SAG application.

6.9.3 Study Questions

1. Simulate a single-phase diode rectifier with a variable inductance filter. Use SIMPLOER simulation tool and non-linear inductance model. Compare simulation results with the experimental results.
2. Compare all mentioned passive PFC solutions and define limitations of passive PFC.

6.10 Experiment 5– Active Power Factor Correction

6.10.1 Introduction

Active power factor correction can be achieved by combining a pre-regulator circuit with a single-phase diode rectifier. In this experiment, a single phase diode rectifier with cascaded boost converter circuit is used as active PFC pre-regulator. The experiment circuit is controlled with UCC3818 average current mode controller IC. The input and output connections and test points can be used for different measurements. The main features of experiment board are listed as follows:

- Designed to comply with IEC 61000-3-2
- Worldwide line operation RMS voltage range from 85 V to 265 V
- Regulated 385V, 250W (max) DC output
- Accurate power limiting and overvoltage protection

The block diagram of the average current controlled PFC is shown in Figure 6.31.

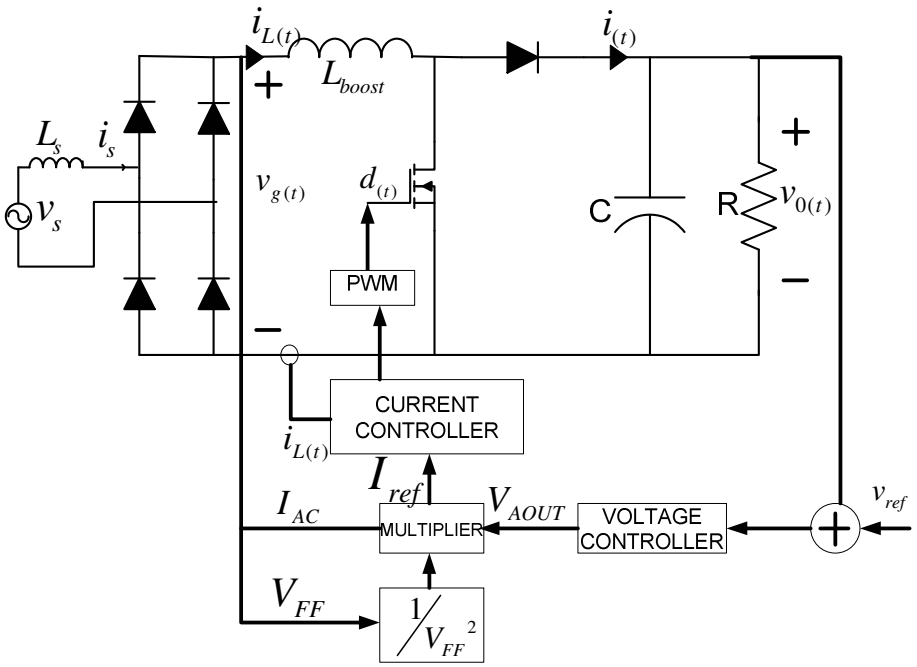


Figure 6.31 Block diagram of average current mode PFC.

6.10.2 Procedure

1. In this experiment, an isolated variable AC power source will be used as an input AC voltage. Adjust variac to 220V AC and connect the output of the variac to the input of the PFC circuit via energy analyzer. Connect a 250W resistive load (R=600 Ω) to the output of the PFC circuit. Connect a 15 V dc power supply as the control circuit power supply. The complete connection diagram for the experiment is shown in Figure 6.32. Once all the connections are made the system can be powered up. Power up the DC supply for the control circuitry and then provide AC voltage.

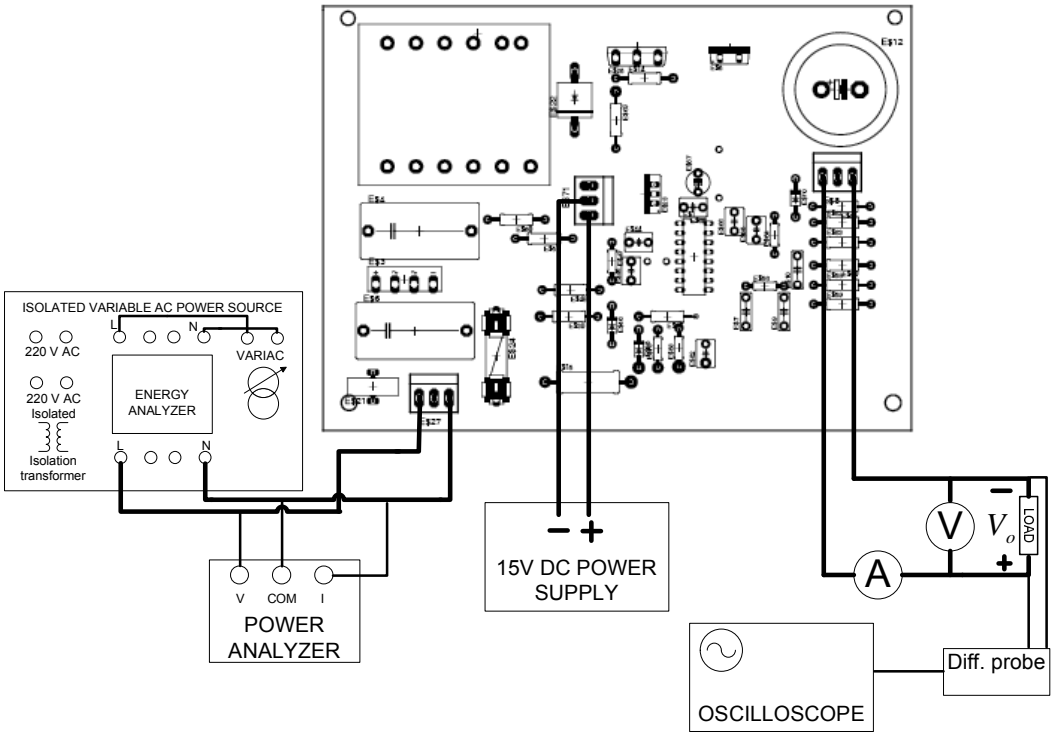


Figure 6.32 Connection diagram for active PFC experiments.

2. Adjust the output power to 250W and measure the input current waveform and the output voltage waveform for two different input voltage levels, 220V AC and 120 V AC. Display the input current waveforms by the single-phase power quality analyzer and also display the input current THD at harmonic screen. The measured input current waveform and harmonics' spectrum for 220 V AC input voltage are shown in Figures 6.33.a and 6.33.b.

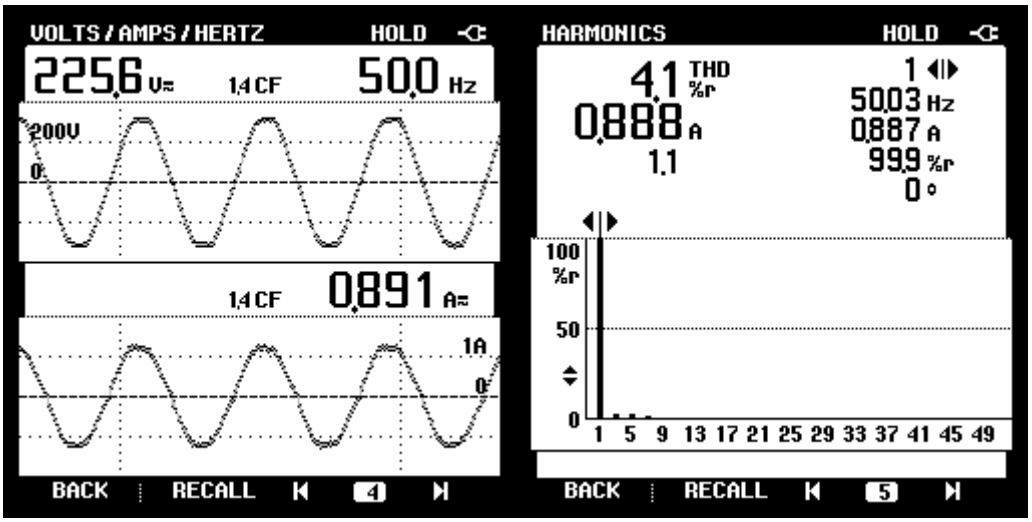


Figure 6.33 a) Input current and voltage waveforms for 220 V AC input voltage (Scales: 100V/div, 1A/div) b) Input current harmonics.

The output voltage should be monitored by a differential probe and digital storage oscilloscope. The measured output voltage ripple for 220 V AC input voltage is shown in Figure 6.34. The output voltage ripple can be best monitored by AC coupling mode. Measure the output voltage ripple.

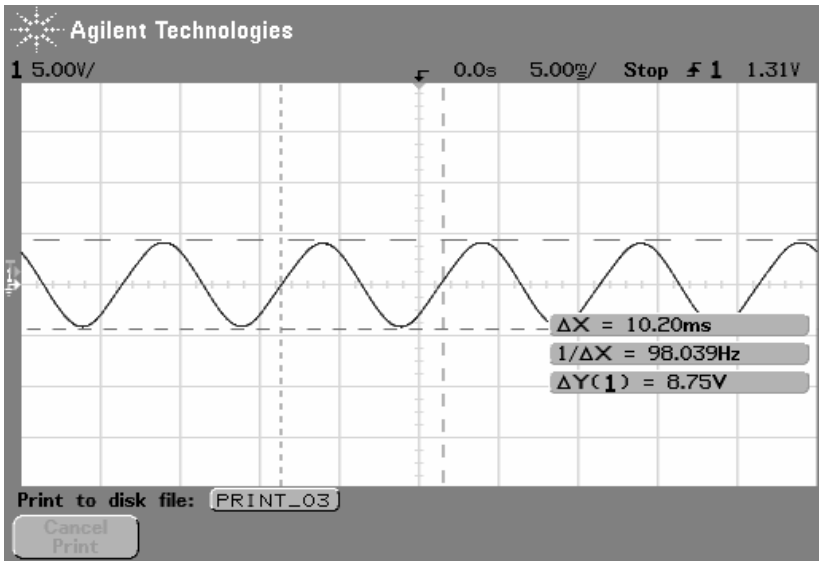


Figure 6.34 Output voltage ripple for 220 V AC input voltage.

Now, adjust the input voltage to 120V AC and take the same measurements described in above.

3. In this step, the power factor of the circuit will be analyzed. Adjust the output power from 50W to 250W by 25W steps. For each power level, measure the PF and efficiency of the circuit by using single-phase power quality analyzer for two different input voltage levels, 220V and 120 V AC. The measured PF for different power level is given in Table 6.14.

Table 6.14 Measured PF for different input voltage level

	Power Factor (PF)	
P_{out}	**V_{in}=120 V**	**V_{in}=220 V**
50 W	0.96	0.87
75 W	0.96	0.90
100 W	0.97	0.95
125 W	0.975	0.96
150 W	0.975	0.97
175 W	0.98	0.975
200 W	0.99	0.98
225 W	0.995	0.985
250 W	0.999	0.99

The power factor versus line voltage and load power graphic is shown in Figure 6.35.

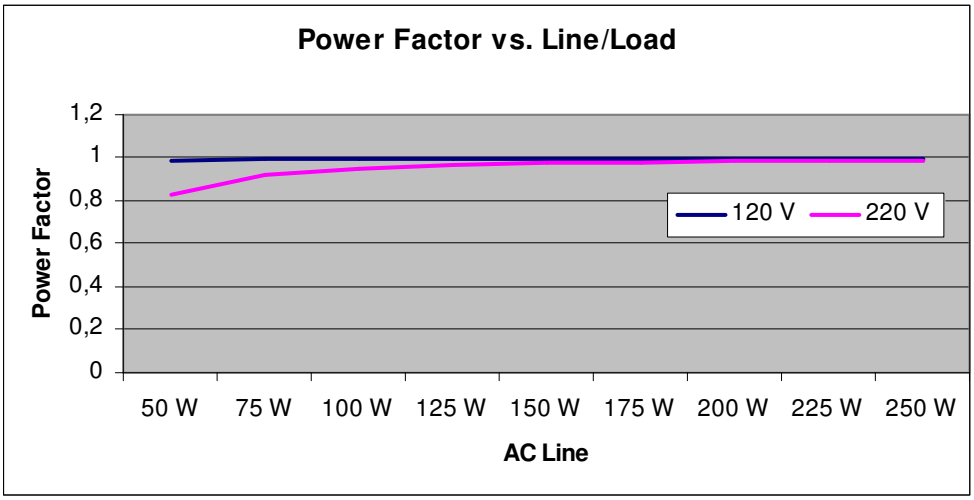


Figure 6.35 Power Factor vs. Line/Load.

4. Active PFC circuits have high start-up currents due to the initial charge of the output bulk capacitor. An NTC is placed in the input of the circuit to limit the inrush current. Adjust input voltage to 220V AC and output power to 250W. Acquire the start-up response for the input current and output voltage. Measure the inrush current, settling time for the input current and output voltage. The measured start-up response for input current and output voltage is shown in Figure 6.36.

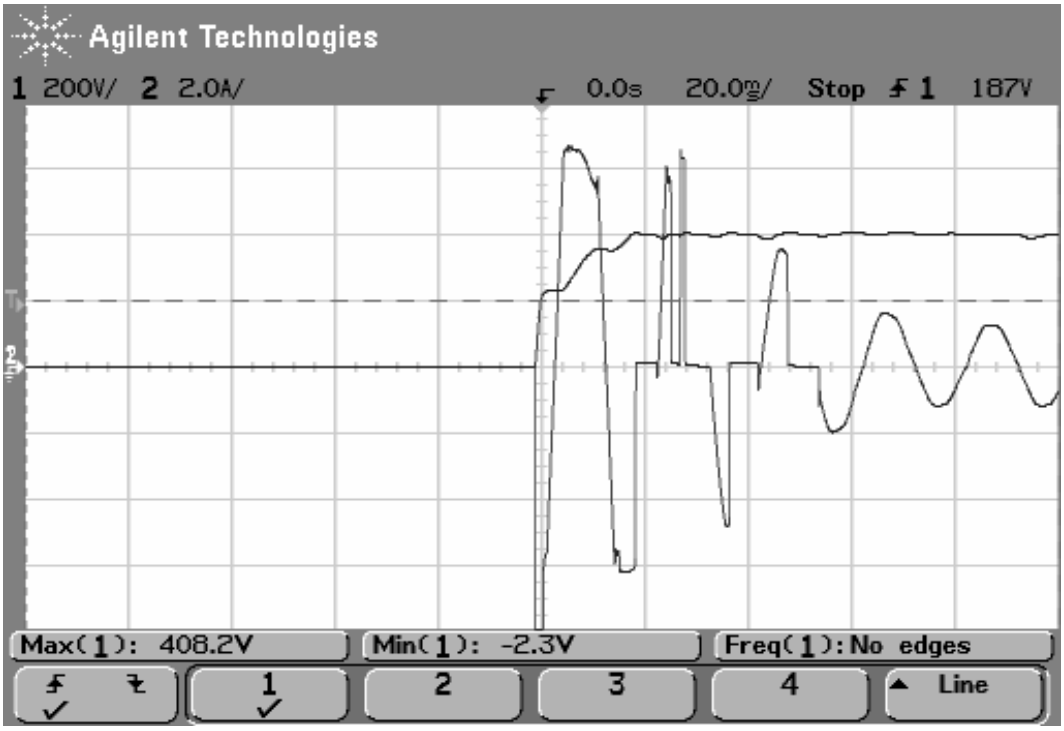


Figure 6.36 Start-up behavior of the input current and output voltage.

The active PFC circuits have slower transient response due the low bandwidth output voltage loop controller. Connect a transient load to the output of the circuit. Power up the system with 100W (1600 Ω) and switch to 200W (800 Ω) at the steady state. Obtain the output voltage transient response. Comment on results.

5. In the experiment board, the inductor current is sensed via a sense resistor. The user can monitor the inductor current by the voltage drop in this sense resistor. A low pass filter is placed to attenuate the noise in the inductor current waveform measurements. The drain-to-source voltage of MOSFET and anode-cathode

voltage of the boost diode can be measured with a high voltage differential probe by connecting directly to the components. The measurement method for the switching characteristics of the power semiconductor elements in the PFC circuit is shown in Figure 6.37.

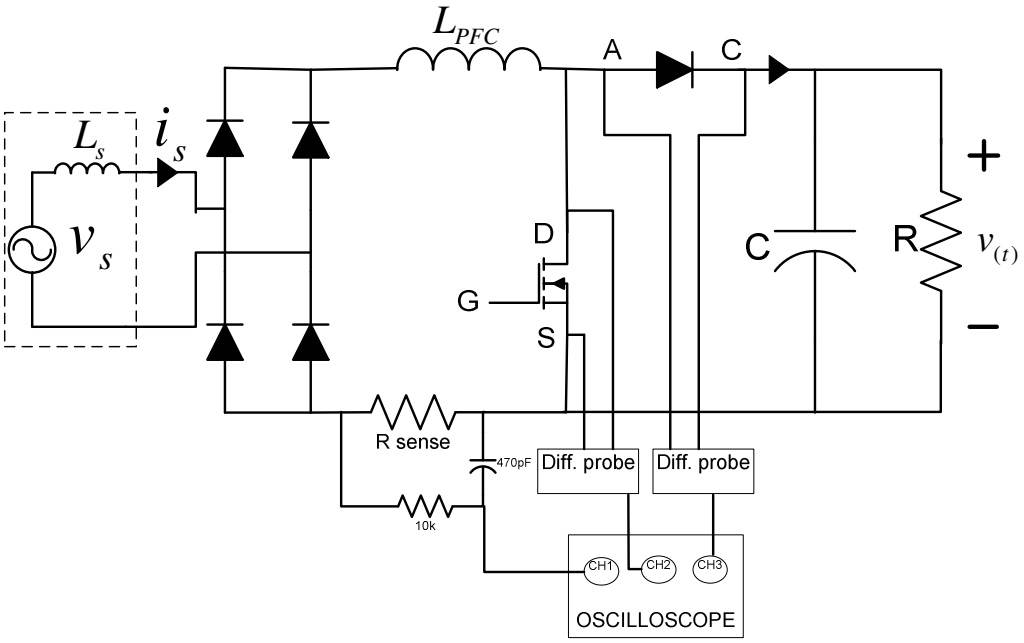


Figure 6.37 Measurement method of switching characteristics.

Adjust input voltage to 220 V AC and output power to 250W. Acquire the inductor current, drain-to-source voltage of the MOSFET and anode-cathode voltage of the boost diode. Comment on the switching waveforms for the boost converter.

6.10.3 Study Questions

1. Considering the design of the circuit, why the performance is better in the low level input voltage conditions? Why the input current has distortions at the zero crossings of the input voltage?
2. What are the other solutions to limit the inrush current at the start-up?
3. Why does the output voltage controller have a low bandwidth?
4. What are the solutions to reduce the switching losses in the PFC applications? Consider soft-switching techniques, developments in semiconductor technology.

CHAPTER 7

CONCLUSIONS AND FURTHER WORK

This thesis is concerned with the power factor correction methods for single-phase converters. A complete experiment system is designed and implemented that including passive and active solutions. The analyzed solutions are selected to their benefits, performance and popularity.

In the first chapter of this thesis provide a general knowledge about harmonic emission standards, classification of single-phase converters, harmonics and their effects and solutions for power factor correction. A general survey about the passive and active power factor correction methods are reviewed.

The second stage of the thesis involves in the passive power factor correction methods for a single-phase bridge rectifier. Three types of harmonic filters are analyzed and designed according to harmonic emission standard IEC 61000-3-2. A test bench suitable for the show the performance of the DC side LC filter method, 3^{rd} harmonic filter method and Sloped air-gap inductor method is designed. All theoretical and experimental results show that, a passive filtering method seems attractive for low power application due to their low cost and few complexity characteristics. But the size and weight of the filtering elements are the disadvantages of the passive filtering methods.

Third stages of the thesis active power factor correction methods are evaluated. A single-phase diode rectifier with a cascaded boost converter has advantages over the other topologies. Then, the control techniques for active PFC are analyzed. Three of the control methods are implemented. These are average current control, critical

conduction mode and one cycle control. The selected control methods are chosen according to their performance, popularity and design complexity. The experimental results show that all implemented control techniques have trade-off among them. The average current control seems more attractive with its performance but the design of this type control is more complex. The critical conduction mode reduces design complexity however it is suitable for low power applications due to operating with higher peak current levels. Finally one cycle control is implemented. The one cycle control simplifies the design process with lower component count.

The third chapter of the thesis was dedicated to an experiment system for single-phase power factor correction. A complete experiment procedure with the basic information to detailed experiment procedure is prepared. The experiment steps are supported with measurement results and waveforms. Also comments on the results and study questions are stated in all experiments.

As a result, the harmonic polluting affects of the single-phase diode rectifier based power converters are reviewed theoretically and experimentally. The harmonic limiting standards and the common solutions for power factor correction are analyzed. The popular passive and active power factor correction schemes are analyzed and verified with simulation and experimental results. An experiment system is built and optimized to be used by the students to help understanding the basics of the power factor correction in the laboratory experiments.

The experiment system can be improved by using latest developments in semiconductor technology. Power loss considerations and new techniques to reduce these losses can be implemented. Hence this thesis is intended to be used for educational purposes advance points can be used in power factor correction to show the latest developments in this area.

REFERENCES

[1] IEC61000-3-2, *Electromagnetic Compatibility (EMC)—Part 3: Limits—Section 2: Limits for Harmonic Current Emissions (Equipment Input Current <16A per Phase)*,

[2] TS EN 61000-3-2, *Elektromanyetik Uyumluluk (EMU)-Bolum 3-2: Sınır Değerler-Harmonik Akim Emisyonları İçin Sınır Değerler (Faz Başına Donanım Giriş Akımı <16A)*, TSE, MART 2003

[3] EPSMA, *Harmonic Current Emissions Guidelines to the standard EN 61000-3-2 including amendment A14*, 2004, www.epsma.org

[4] R. Redl, P.Tenti, V.Wyk, *Power electronics polluting effects*, IEEE Spectrum, Volume 34, Issue 5, May 1997

[5] R. Redl, Electromagnetic Environmental Impact of Power Electronics Equipment, Proceedings of the IEEE, Vol 89, No:6, June 2001

[6] N. Mohan, T. Udeland, andW. Robbins, *Power Electronics: Converters, Applications and Design*, 2nd ed. New York: Wiley, 1995.

[7] R. W. Erickson, *Fundamentals of Power Electronics*. New York: Chapman & Hall, 1997.

[8] M. H. Rashid, *Power Electronics: Circuits, Devices, and Applications*, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 1993.

[9] B. Sharifipour, J. S. Huang, P. Liao, L. Huber and M. M. Jovanovic, "*Manufacturing and cost analysis of power-factor-correction circuits,*" IEEE Applied Power Electronics Conf. (APEC) Proc., 1997, pp.490-494

[10] Oscar Gracia,Jose A. Cobos,Roberto Prieto and JavierUceda, "*Single Phase Power Factor Correction:A Survey*", IEEE Transactions on Power Electronics,Voi 18,No3,May 2003,pp-749-755.

[11] Singh, B.; Singh, B.N.; Chandra, A.; Al-Haddad, K.; Pandey, A.; Kothari, D.P. "*A review of single-phase improved power quality AC-DC converters*" Industrial Electronics, IEEE Transactions on Volume 50, Issue 5, Oct. 2003 Page(s): 962 – 981

[12] Supratim Basu, T.M.Undeland, Fellow, IEEE. "*PFC Strategies in light of EN 61000-3-2*". (EPE-PEMC 2004 Conference in Riga, LATVIA, 1- 3 September 2004)

[13] Fernandez, A.; Sebastian, J.; Hernando, M.M.; Villegas, P.; Garcia, J. "*Helpful hints to select a power-factor-correction solution for low- and medium-power single-*

phase power supplies" Industrial Electronics, IEEE Transactions on Volume 52, Issue 1, Feb. 2005 Page(s): 46 – 55

[14] JS Lai, D. Hurst, T. Key, "*Switch-mode Power Supply Power Factor Improvement via Harmonic Elimination Methods*", IEEE APEC 1991

[15] Richard Redl and Laszlo Balogh, "*Power-Factor Correction in Bridge and Voltage-Doubler Rectifier Circuits with Inductors and Capacitors*" APEC´95, pp.466-472

[16] E. Maset, E. Sanchis J. Sebastián y E. de la Cruz ,"*Improved Passive Solutions to Meet IEC 1000-3-2 Regulation in Low-Cost Power Supplies*" , IEEE International Telecommunications Energy Conference. Boston (EE.UU) Octubre de 1996. pp. 99-106.

[17] Richard Redl and ELFI S.A., "*An Economical Single-Phase Power- Factor-Corrected Rectifier: Topology, Operation, Extensions, and Design For Compliance*" APEC´98, pp.454-460

[18] Mangesh Borage, Sunil Tiwari and S. Kotaiah, "*Passive Techniques for Compliance of Single-phase Rectifiers with IEC 1000-3-2 Norms*", Proc. of International conference on Electromagnetic Interference and Compatibility (INCEMIC) 2003, pp. 1-8.

[19] A. W. Kelley and W. F. Yadusky, "*Rectifier design for minimum line current harmonics and Maximum power factor*", APEC´89, pp. 13-22

[20] Jovanovic, D. E. Crow, "*Merits and Limitations of Full-Bridge Rectifier with LC Filter in Meeting IEC 1000-3-2 Harmonic-Limit Specifications*". IEEE Applied Power Electronics Conf.(APEC), March 1996, pp. 354-360.

[21] W.M.Lin, J.Sebastian, A.Fernandez, " *Design of the basic rectifier with LC filter to comply with the new edition of the IEC1000-3-2 current harmonic limit specifications* " IEEE 2002

[22] Sanz, M.; Llombart, A.; Ortiz, S.; Gomez, F., **"***Merits and limitations of full-bridge rectifier with LC filter in meeting IEC 61000-3-4 harmonic-limit specifications***"** Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual Volume 3, Issue,2000Page(s):1133-1136vol.3

[23] Lin, W.M.; Villarejo, J.A.; Sebastian, J.; Fernandez, A.; Hernando, M.M.; "*Designing single-stage power factor correctors and LC passive filters to comply with the new version of the IEC 1000-3-2 regulations* **"** Power Electronics Specialists Conference,2002.pesc2002,

[24] Doval-Gandoy, J.; "*Low-cost design of the input section of mains-connected consumer electronics equipment classified as class A in the new version of the IEC 1000-3-2 regulations",* Consumer Electronics, IEEE Transactions on Volume 50, Issue 2, May 2004 Page(s):505 - 511

[25] Fernandez, A.; Sebastian, J.; Hernando, M.M.; Villegas, P.; Lamar, D.G.; ”*Design trade-offs to meet class a IEC 61000-3-2 regulations with passive circuits in low power applications”,* Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual Volume 1, 20-25 June 2004 Page(s):309 - 315 Vol.1

[26] Carbone, R.; Scappatura, A., “*A high efficiency passive power factor corrector for single-phase bridge diode rectifiers***”,** Power Electronics Specialists Conference, 2004. 2004 IEEE 35th Annual Volume 2, 20-25 June 2004 Page(s):1627 - 1630 Vol.2

[27] A.R. Prasad, P. D. Ziogas, and S. Manias, “*A novel passive waveshaping method for single-phase diode rectifiers,*” in IEEE IECON Conf. Proc., 1990, pp. 1041-1050

[28] Ji Yanchao; Liang Xiaobing; Liu Zhuo; Jin Jisheng; Liu Xinhua, “*An improved passive input current waveshaping method for single-phase diode rectifier***”** IEEE IECON 22nd International Conference on Volume 2, 5-10 Aug. 1996 Page(s):695 – 699,vol.2

[29] W. Wölfle, W. G. Hurley, and S. Lambert, “*Quasiactive power factor correction: The role of variable inductance,*” in Proc. IEEE 32nd Power Electron. Spec. Conf. (PESC’01), vol. 4, Vancouver, BC, Canada, June 2001, pp. 2078–2083

[30] Sebastian, J. Jaureguizar, M. Uceda, J. , *An overview of power factor correction in single-phase off-linepower supply systems,* Industrial Electronics, Control and Instrumentation, 1994. IECON '94.

[31] L. H. Dixon, *High Power Factor Preregulators for Off-Line Power Supplies*, Unitrode Power Supply Design Seminar Manual SEM600, 1988

[32] L. Rossetto, G. Spiazzi, P. Tenti, *Control techniques for power factor correction converters,* Pemc94

[33] C. Zhou, M. Jovanovic, "*Design Trade-offs in Continuous Current-mode Controlled Boost Power-Factor Correction Circuits'*," HFPC Conf. proc., 1992, pp. 209-220.

[34] C. Silva, "*Power Factor Correction with the UC3854*," Application Note, Unitrode Integrated Circuit.

[35] B. Andreycak, "*Optimizing Performance in UC3854 Power Factor Correction Applications,*" Unitrode, Products & Applications Handbook, 1993/94.

[36] M. K. Nalbant, J. Klein, "*Design of a 1kW Power Factor Correction Circuit',"* PCIM Conf. proc., 1990, pp. 17-24.

[37] J. Klein, M. K. Nalbant, "*Power Factor Correction - Incentives, Standards and Techniques',*" PCIM Conf. proc., 1990, pp. 26,28-31.

[38] R. Redl, B. P. Erisman, *"Reducing distortion in Peak- Current-Controlled Boost Power-Factor Correctors,"* APEC Conf. Proc., 1994, pp. 576-583.

[39] D. Maksimovic, *"Design of the Clamped-Current High-Power-Factor Boost Rectifier,"* APEC Conf. Proc., 1994, pp. 584-590.

[40] C. Zhou, R. B. Ridley and F. C. Lee, "*Design and Analysis of a Hysteretic Boost Power Factor Correction Circuit*," PESC Conf. Proc., 1990, pp. 800-807.

[41] J. S. Lai, D. Chen, "*Design consideration for Power Factor Correction Boost converter Operating at the Boundary of Continuous Conduction mode and Discontinuous Conduction mode'*, APEC Conf, proc., 1993, pp. 267-273.

[42] R. Erickson, M. Madigan, S. Singer, "*Design of a Simple High-Power-Factor Rectifier Based on the Flyback Converter,*" APEC Conf. Proc., 1990, pp. 792-801.

[43] K. H. Liu, Y. L. Lin, *"Current Waveform Distortion in Power Factor Correction Circuits Employing Discontinuous-Mode Boost Converters*," PESC Conf. Proc. 1989, pp. 825-829.

[44] Maksimovic, Dragan, Yungtaek Jang, and Robert W. Erickson. *"Nonlinear-Carrier Control for High-Power-Factor Boost Rectifiers"* IEEE Transactions on Power Electronics vol. 11 No. 4 (Jul. 1996): p. 578-84.

[45] K. Smedley. S. Cuk. "*One Cycle Control of Switching Converters*". 22nd Annual IEEE Power Electronics Specialists Conference (Cat. No.91CH3008-0), Cambridge, MA, 1991. pp. 888-96. See also US patent 5,278,490 and IEEE Transactions on Power Electronics, Nov. 1995, Vol. 10, No. 6, P625-633.

[46] L. H. Dixon, *Optimizing the Design of High Power Factor Switching Preregulator*, Unitrode Power Supply Design Seminar Manual SEM700, 1990

[47] J. B. Williams, "*Design of Feedback Loop in Unity Power Factor AC to DC Converter*", PESC Conf. Proc., 1989, pp. 959-967.

[48] J.P. Noon, D.Dalal, *Practical design issues for PFC circuits*, IEEE APEC 1997.

[49] G. Spiazzi, P. Mattavelli, L. Rossetto, "*Methods to Improve Dynamic Response of Power Factor Preregulators: an Overview*", European Power Electronics Conf. (EPE), Sevilla (Spain), September 1995, Vol.3, pp.754-759.

[50] L. Dixon, "*Average current mode control of switching power supplies*," Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM-700,1990.

[51] R. B. Ridley, "*Average Small-Signal Analysis of the Boost Power- Factor-Correction Circuit*", VPEC Seminar Proc., 1989, pp. 108-120.

[52] Philip C. Todd, "*U-134,UC3854 Controlled Power Factor Correction Circuit Design*,"Available: http://www- s.ti.com/sc/psheets/slua144/slua144.pdf

L. Dixon, Unitrode Magnetics Design Handbook, MAG 100A. Texas Instruments

[53] *UCC3817 data sheet*, Texas Instruments Power Supply Control Products. www.ti.com

[54] MC34262 *data sheet*, On Semiconductor PFC controller IC. www.onsemi.com

[55] Lai Z.; Smedley, K.M.; "*A family of continuousconduction-mode power-factor-correction controllers based on the general pulse-width modulator*", IEEE transactions on Power Electronics, Volume: 3 , Issue:3, May 1998, Pages:501 - 510

[56] IR1150 *data sheet*, International Rectifier PFC controller IC. www.irf.com

APPENDIX

LIST of PFC CONTROL ICs

Part No.	Company	Description	Year
IPS101C-D	ASIC Advantage	Power Factor Correction Controller	2005
IPS101I-D	ASIC Advantage	Power Factor Correction Controller	2005
FAN4803CP-1	Fairchild Semiconductor	8-Pin PFC and PWM Controller Combo	2002
FAN7527BM	Fairchild Semiconductor	Power Factor Correction Controller	2003
FAN7528M	Fairchild Semiconductor	Dual Output Critical Conduction Mode PFC Controller	2006
ML4812	Fairchild Semiconductor	Peak Current Mode PFC Controller	1998
ICE1PCS01	Infineon Technologies	Standalone Power Factor Correction (PFC) Controller in Continuous Conduction Mode (CCM)	2005
ICE1QS01	Infineon Technologies	Controller fo Switchmode Power Supplies Supporting Low Power Standby & Power Factor Correction	2004
TDA4862	Infineon Technologies	Power Factor Controller (PFC) IC for High Power Factor and Active Harmonic Filter	2003
TDA4862G	Infineon Technologies	Power Factor Controller (PFC) IC for High Power Factor and Active Harmonic Filter	2003
TDA4863-2	Infineon Technologies	Power Factor Controller IC for High Power Factor and Low THD	2004
TDA4863-2G	Infineon Technologies	Power Factor Controller IC for High Power Factor and Low THD	2004
IR1150S	International Rectifier	One Cycle Control PFC IC	2005
NCP1601ADR2	ON Semiconductor	Compact Fixed Frequency Discontinuous or Critical Conduction Voltage Mode PFC Controller	2005
NCP1653AD	ON Semiconductor	Compact, Fixed-Frequency, Continuous Conduction Mode PFC Controller	2005
MC33260D	ON Semiconductor	GreenLine(tm) Compact Power Factor Controller	2003
NCP1601AP	ON Semiconductor	Compact Fixed Frequency Discontinuous or Critical Conduction Voltage Mode PFC	2005

NCP1603D100R2	ON Semiconductor	PFC/PWM Combo Controller with Integrated High Voltage Startup & Standby Capability	2005
NCP1650D	ON Semiconductor	Power Factor Controller	2003
L6561P	STMicroelectronics	Power Factor Corrector	2002
UCC2819AN	Texas Instruments	Programmable Output Power Factor Pre-Regulator	2003
UCC28512N	Texas Instruments	BiCMOS PFC/PWM Combination Controller	2004
UCC28514N	Texas Instruments	BiCMOS PFC/PWM Combination Controller	2004
UCC28516N	Texas Instruments	BiCMOS PFC/PWM Combination Controller	2004
UCC38050D	Texas Instruments	Transition Mode PFC Controller	2006
UCC3817D	Texas Instruments	BiCMOS Power Factor Preregulator	2003
UCC3819AD	Texas Instruments	Programmable Output Power Factor Pre-Regulator	2003
UCC38050P	Texas Instruments	Transition Mode PFC Controller	2006
UCC38051P	Texas Instruments	Transition Mode PFC Controller	2006
UCC3817N	Texas Instruments	BiCMOS Power Factor Preregulator	2003
UCC3818N	Texas Instruments	BiCMOS Power Factor Preregulator	2003
UCC3819AN	Texas Instruments	Programmable Output Power Factor Pre-Regulator	2003
UC1854BJ	Texas Instruments	Advanced High Power Factor Preregulator	2003
UC2854AN	Texas Instruments	Advanced High Power Factor Preregulator	2003
UC3854AN	Texas Instruments	Advanced High Power Factor Preregulator	2003
UCC28050D	Texas Instruments	Transition Mode PFC Controller	2006
UCC28051D	Texas Instruments	Transition Mode PFC Controller	2006
UCC2818D	Texas Instruments	BiCMOS Power Factor Preregulator	2003