DESIGN OF A ZVS QRC CONVERTER FOR EDUCATIONAL TEST BENCH

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ABSTRACT

DESIGN OF A ZVS QRC CONVERTER FOR
EDUCATIONAL TEST BENCH

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In this thesis, the conventional pulse-width modulated (PWM) and zero-voltage switching (ZVS) quasi-resonant buck converters are analyzed and a variable-frequency control technique is proposed to regulate the output voltage due to the immediate input line and load changes. The quasi-resonant technique provides favorable switching conditions for active switch to reduce switching losses and electromagnetic interference (EMI). The method is based on shaping the voltage across the active switch in quasi-sinusoidal fashion and the switching action occurs with nearly zero voltage across the active switch. This requires only two additional components to the conventional PWM buck converter. The proposed quasi-resonant converter is capable of operating in megahertz range with a significant improvement in performance and power density. Detailed analytic and small-signal models of the ZVS quasi-resonant buck converter are established and the switching behavior is investigated in order to provide nearly zero-voltage turn-on. The performance of the ZVS quasi-resonant technique is verified with

the computer simulations. The results are compared with the experiments in the laboratory involving both the open-loop and closed-loop operations. The detailed experiment procedure is added to use this converter for educational purposes.

Keywords: Quasi-Resonant Converter, Buck Converter, Variable Frequency, Pulse-Width Modulation (PWM), Zero-Voltage Switching

ÖZ

EĞİTİM AMAÇLI ZVS-QRC DÖNÜŞTÜRÜCÜ TASARIMI

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Bu tezde, süregelen darbe-genişlik modülasyonlu ve sıfır akım anahtarlamalı yarı çınlamalı gerilim düşürücü analiz edilmiş ve giriş geriliminde ve çıkış yükünde meydana gelen ani değişimlerine karşı çıkış gerilimini ayarlayan değişken frekanslı bir kontrol yöntemi önerilmiştir. Yarı çınlamalı anahtarlama tekniği, anahtarlama kayıplarını ve elektromanyetik girişimi azaltmak için devredeki aktif anahtarlama elemanına uygun anahtarlama koşulları sağlamaktadır. Bu metot, aktif anahtarlama elemanı üzerindeki gerilimi yarı sinüssel yapmaya dayanmaktadır ve anahtarlama faaliyeti aktif anahtarlama elemanı üzerindeki gerilim neredeyse sıfır iken gerçekleşmektedir. Bu metot için, süregelen darbe-genişlik modülasyonlu dönüştürücülere sadece ek olarak iki devre elemanı eklenmesi gerekmektedir. Önerilen yarı çınlamalı dönüştürücüler, performansta ve güç yoğunluğunda dikkate değer bir iyileştirme ile MHz frekans değerlerine kadar çalışabilmektedir. Sıfır gerilim anahtarlamalı yarı çınlamalı gerilim düşürücünün detaylı analitik ve küçük sinyal

modelleri kurulmuştur ve sıfır gerilimde anahtarlama sağlaması için anahtarlama davranışları incelenmiştir. Sıfır gerilim anahtarlamalı yarı çınlama yönteminin başarımı bilgisayar benzeşimleriyle doğrulanmıştır. Sonuçlar, hem açık çevrim hem de kapalı çevrim için laboratuar deneyleri ile karşılaştırılmıştır. Bu dönüştürücünün eğitim amaçlı kullanılması için detaylı deney prosedürleri eklenmiştir.

Anahtar Kelimeler: Yarı Çınlamalı Dönüştürücü, Gerilim Düşürücü, Değişken Frekans, Darbe Genişlik Modülasyonu (PWM), Sıfır Gerilim Anahtarlama

To My Parents and My Love

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CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

Power electronics, in a broad sense, is concerned with the processing of given electrical power into output suitable for specific load or loads, using electronic devices. Like many other areas of engineering, power electronics is an application-driven field. The demands for smaller and efficient power processing equipment have been the main motivation factors behind the introduction of new circuit topologies and the development of the new power semiconductor devices [1].

Switching converters are the basic blocks in power electronics. These systems use semiconductor switches along with other passive elements (capacitors, inductors and transformers) to transfer electrical energy from input to different kinds of output load or loads as shown in Figure 1.1. The circuit topology changes as these switches open and close as a function of time under the guidance of the controller. If all elements are ideal, theoretically 100% efficiency could be achieved. In practice, these semiconductor switches and elements have both conduction and switching losses that lower the efficiency [2].

The power processing technique has evolved around three fundamentally different circuit schemes: linear-mode, Pulse-Width Modulation (PWM) and resonance. The linear power processing technique offers several advantages such as simplicity in design,

noise immunity, fast dynamic response time and low cost. However linear power processing applications are limited due to several disadvantages: only step down voltage conversion, only one output of each application and very-low efficiency (%30-%60).

Conventional Pulse-Width Modulation (PWM) power processing technology has been widely used in today's power electronics industry, particularly in low-power application due to circuit simplicity and ease of control. In PWM converters, the output voltage is directly controlled by the duty cycle of the switch gate signal. That is to say, the PWM is duty cycle controlled power processing technique and power flow is interrupted by this phenomena. The PWM power processing technique maintains a constant switching frequency and varies the duty cycle. The current and voltage waveforms are non-sinusoidal. The semiconductor devices in many switching converters are either completely turned on (into the saturation state) or completely turned off (into the cut-off state). Since the switching frequency is fixed, this modulation scheme has a relatively narrow noise spectrum allowing a simple low pass filter to sharply reduce peak-to-peak ripple in the output voltage. This requirement is achieved by arranging an inductor and a capacitor in the converter in order to form a low pass filter network. This requires the frequency of low pass filter to be much less than the switching frequency [3].

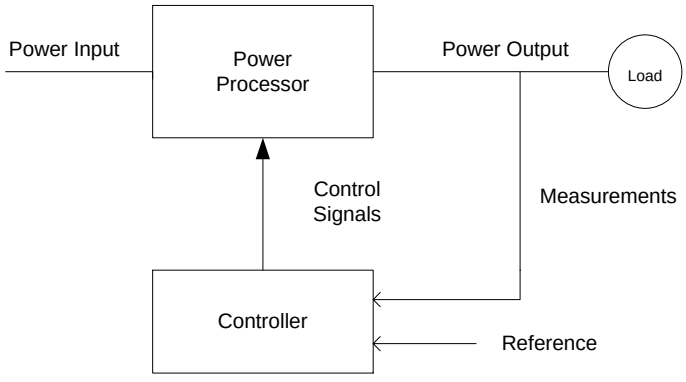

Figure 1.1 Power electronics system: A block diagram.

The basic PWM converters include buck, boost, buck-boost and Cuk converters as shown in Figure 1.2. Energy is stored in the inductor when the active switch is ON ($0 < t < t_{on}$), when the switch is OFF ($t_{on} < t < T$), the stored energy will be delivered to the load. The flow of energy can be controlled by the duty ratio D of the gate signal.

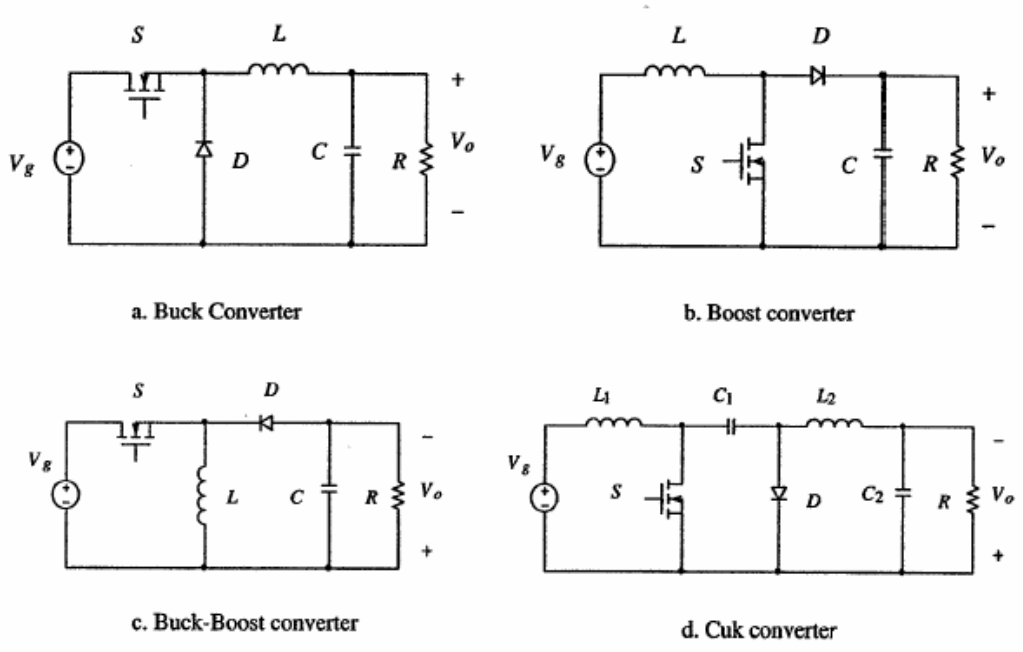

Figure 1.2 Basic PWM converters.

The single transistor version, without voltage isolation between the input and output, as shown above, is used in low power applications. For any application over a few hundred watts, or any case where isolation is needed, the transformer isolated PWM converters such as Forward, Flyback, Push-Pull, Half-Bridge and Full-Bridge are usually employed. In general, PWM converters are controlled by either voltage-mode control or current-mode control. Figure 1.3 shows a voltage-mode controlled buck converter. The output voltage is sensed and compared with the reference voltage. The error signal is

compensated by a proportional-plus-integral (PI) controller and then fed to a comparator to generate the duty cycle signal. The single feedback loop makes it easier to design and analyze. However, the output filter adds two poles to the control loop, which will affect dynamic specifications such as gain margin, phase margin and crossover frequency.

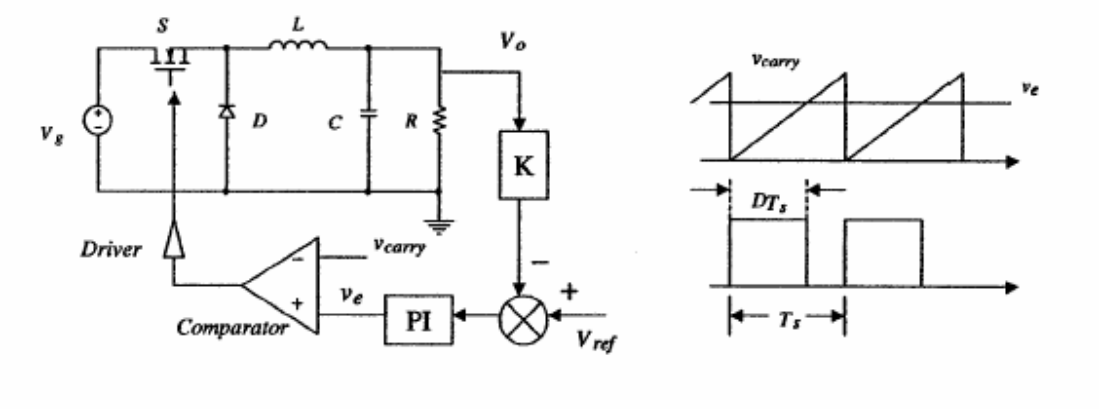

Figure 1.3 Voltage mode controlled buck converter.

To improve the dynamic performance, current mode control is used. Peak current mode control and average current control are the two common forms. The most common current mode control scheme of buck converter is shown in Figure 1.4. The output voltage and the inductor current are sampled. The output of the voltage loop is the input for the current loop. The switch is turned on at the beginning of each cycle. When the inductor current reaches the value output of the voltage loop, the switch is turned off.

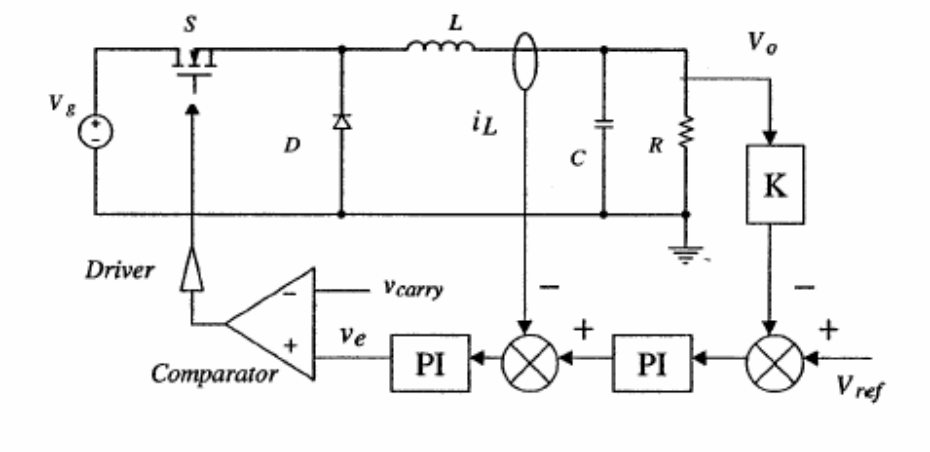

Figure 1.4 Average current mode controlled buck converter.

There are two switching events that take place in the generalized switching model as mentioned before called as turn-on and turn-off. However, transition between on and off states produces switching losses because of the simultaneously occurring high current and voltage values. During the switching intervals, instantaneous power dissipated in the semiconductor switch can be larger than the power loss occurring while conducting. The average loss depends on the speed of the switching interval and switching frequency of the switching converter [2].

The amount of energy lost in a switch during the turn-on and turn-off transitions depends on whether the load is resistive or inductive and the performance of the power diodes. Moreover, when the switch is off, there is a small amount of charge stored internally in the switch. For metal-oxide semiconductor field-effect transistors (MOSFETs), this internal charge is higher.

In most power processing circuits, efficiency is of paramount importance. In designing power processing circuits, there is an increasing demand to increase the switching frequency in order to reduce the weight and size of the energy storage elements

(capacitors, inductors and transformers) and to improve the dynamic performance of the converter circuit. This demand for high power density and high performance is critical for the power processing circuits to be used in the computer, telecommunication, military and even aerospace applications. Due to the increasing switching frequencies, the switching losses and switching stresses are also increased. This situation results in poor system performance and low power density and makes many conventional converters impractical [4].

The main factors that contribute to the high frequency switching losses are [5]:

- Semiconductor devices used as switches in power processing converters have non-zero turn-on and turn-off times, and as a result, during switching transitions between on-state and off-state, the semiconductor devices can be conducting significant current while a large voltage is applied across them. This current and voltage overlap results in a large amount of energy being dissipated in the switching device. At high frequencies, this energy lost in the overlap becomes the largest part of the total losses in the semiconductor switches.
- At high frequencies, voltage and current oscillations are induced in junction capacitance and leakage inductance in the transformer during the transition between on and off states due to the sharp di/dt and dv/dt. These oscillations result in higher losses with increasing peak current and voltage values. Furthermore, EMI (Electromagnetic Interference) is caused by high frequency harmonic components associated with non-sinusoidal voltage and current waveforms.
- When the semiconductor switch turns on with applied large voltage across them, the energy storage of the device's output capacitance ($0.5CV^2f$) is dissipated internally due to the turn-on transition.

To lower these losses and improve system performance, power density and the switching behavior of the semiconductor devices, a technique called ***soft switching*** is

used. Soft switching methods add passive components (inductors and capacitors) to the conventional hard switching converters in order to reduce power dissipation, allowing higher switching frequencies up to a few megahertz, reduced converter size and weight and reduced electromagnetic interference (EMI). The switching losses are reduced by ensuring that either the voltage or current of the semiconductor switch is nearly zero during the switching intervals. Due to the resonance concept, EMI resulting from switching transitions is lowered by replacing the high di/dt and dv/dt of the semiconductor switches by means of passive components with slower resonant edges [2].

Soft switching for the semiconductor devices can be either the *zero-current switching* (ZCS) or the *zero-voltage switching* (ZVS). By using the LC resonant network in different structures, these soft switching converters can be generated. Semiconductor switch with this LC resonant network constitutes the resonant switch concept. By simply replacing the power switch or switches in conventional PWM converters with the resonant switch, a family of *quasi-resonant converters* (QRC) has been derived. Quasi-resonant converters store the inductive or capacitive energy and transfer it to the load or loads similar to PWM converters. But, the LC resonant network shapes the current or voltage waveforms in a quasi-sinusoidal form in order to create the zero-current or zero-voltage conduction for the switch without any switching loss during switching transitions [6]. Figure 1.5 shows some of the standard resonant switch networks.

The families of quasi-resonant converters, either ZVS or ZCS, contain a large number of topologies, including buck, boost, buck-boost and different isolated topologies. All ZVS and ZCS topologies share the common structure of resonant switch network in their categories.

The arrangement of the resonant components (L and C) with respect to the semi-conductor switching devices determines the absorption of the parasitic reactance by the resonant network. But, quasi-resonant technique is not capable of utilizing all major parasitic reactance. ZCS-QRCs are insensitive to the junction capacitance of the rectifier

diode, while ZVS-QRCs are insensitive to the MOSFET output capacitance [7]. The ZCS converters can eliminate turn off losses and switching stresses but due to their turn-on losses associated with discharging of energy in the junction capacitance of the MOSFET, these converters are practical at frequencies up to 1-2 MHz. Furthermore, non-zero voltage conduction and oscillations that are caused by MOSFET output capacitance and parasitic inductance in the circuit result in noise and EMI. Practical ZVS quasi-resonant converters operating at frequencies up to 10 MHz can be implemented. The excessive voltage stresses in the switching device proportional to the load range make difficult to implement these converters in wide load range.

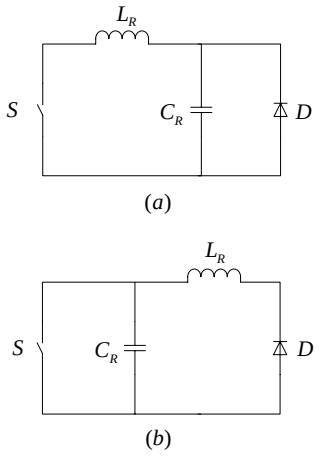

Figure 1.5 Quasi-resonant switches
(a) zero-current quasi-resonant switch
(b) zero-voltage quasi-resonant switch.

The ultimate principle of the *multi-resonant converters* (MRCs) is to utilize all major parasitic elements in any converter circuit. This allows favorable switching conditions for all switching devices (active and passive switch or switches). This technique employs multi-element resonant network no less than three energy storage components. As a result, the basic idea of multi-resonant switches is to extend the resonant-switch

concept to both active switch and diode. Figure 1.6 shows the two basic multi-element resonant networks, either ZCS or ZVS. However, in high frequency operations, MOSFET output capacitance and rectifier diode junction capacitance effects in ZCS-MRCs are still present and parasitic oscillations cannot be eliminated. The ZVS-MRCs are much more suitable for high frequency operations. This technique absorbs parasitic capacitances and provides good switching conditions for both MOSFET and rectifier diode.

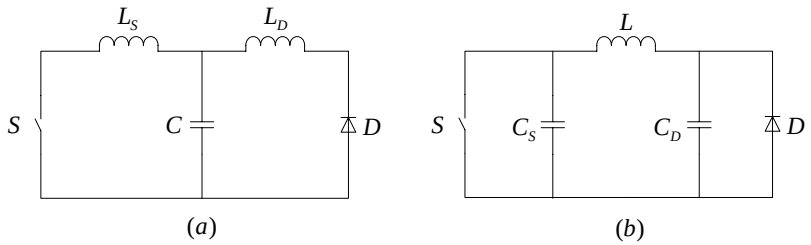

Figure 1.6 Multi-resonant switches
(a) zero-current multi-resonant switch
(b) zero-voltage multi-resonant switch.

Two major disadvantages of the resonant converters are variable frequency operation and excessive voltage and/or current stresses of the active and/or passive semiconductor components. The ZCS converters require constant on-time variable frequency control, while the ZVS converters require constant off-time variable frequency control. To operate in a wide input voltage and load range, the frequency variations are also wide.

Even though there exists no general classification of resonant converter topologies, these types of resonant converters can be represented as in Figure 1.7.

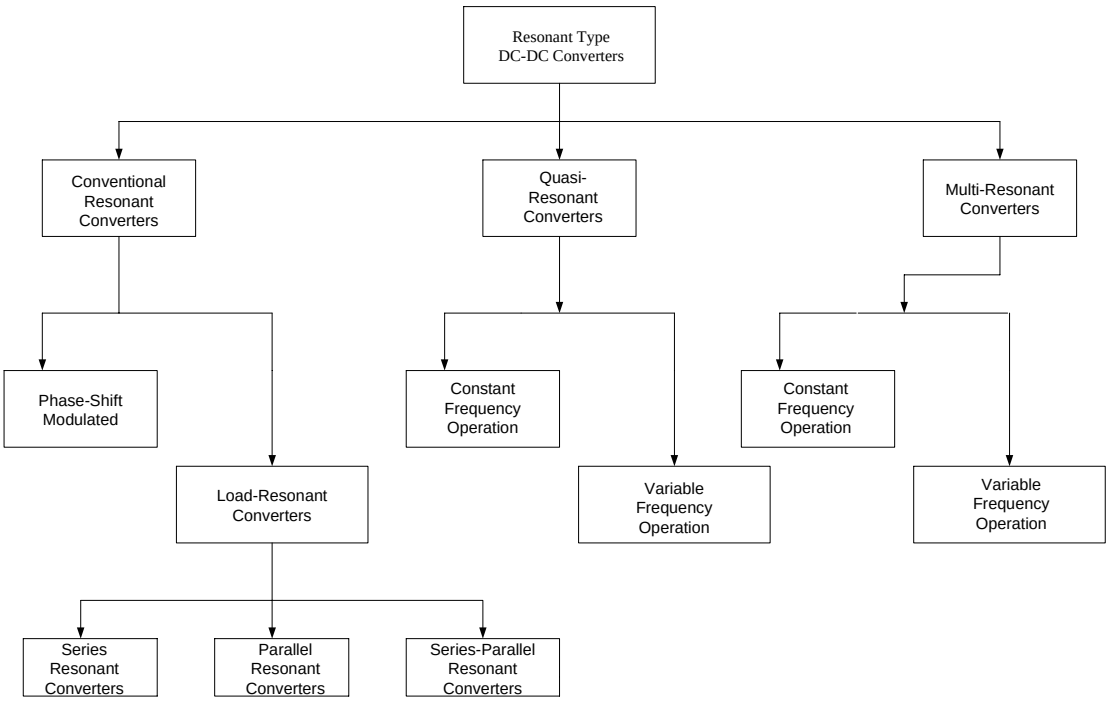

Figure 1.7 Resonant type dc-dc converters.

Output regulation in many resonant converters, such as QRCs and MRCs, is achieved by controlling the switching frequency. The ZCS applications require controlled on times while ZVS applications require controlled off times. The closed-loop control of the resonant converters can be achieved by feedback of the output voltage. A commonly used single-loop control scheme for the buck converter is shown in Figure 1.8.

A compensation network is used to provide high low-frequency gain and improved phase margin. The output of the error amplifier controls the Voltage Controlled Oscillator (VCO) to determine the frequency of operation.

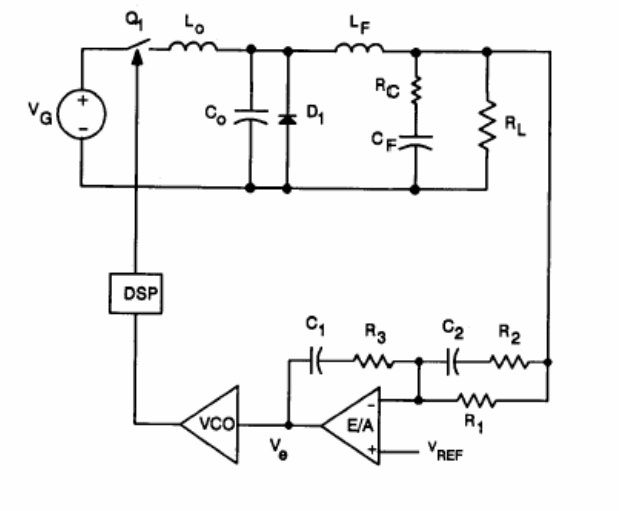

Figure 1.8 Single-loop controlled buck QRC.

Multi-loop control is effective for controlling PWM converters, providing good stability margin and high crossover frequency. For QRCs and MRCs, Current-Sense Frequency Modulation (CSFM) offers the same advantage. The VCO used for single-loop control of resonant converters is replaced with a comparator. Figure 1.9 shows the basic concept for implementation of CSFM for the buck converter.

Like current-mode control of PWM converters, several possible ways of implementing CSFM exist. The most direct method uses resistive sensing with an operational amplifier. A second method uses a current transformer in series with the diode. The last and most effective method uses the auxiliary winding of filter inductor to sense the inductor voltage and integrate through resistor and capacitor to reconstruct the inverted portion of the inductor current [8].

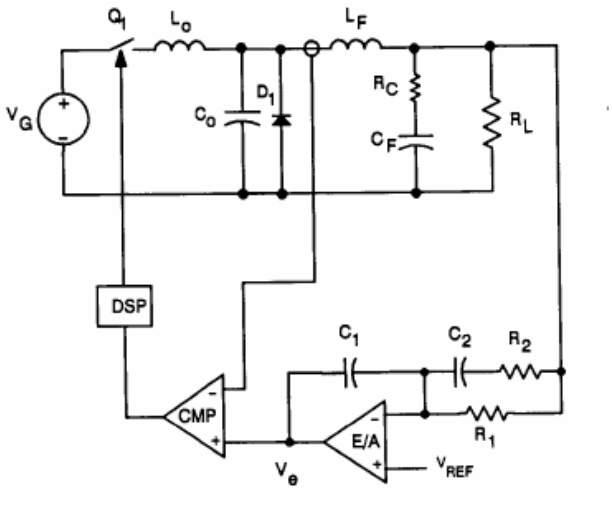

Figure 1.9 CSFM controlled QR buck converter.

1.2 Outline of Report

In Chapter 2, conventional PWM converters are presented in details. Topological variations and control methods of these techniques are also presented in Chapter 2.

In Chapter 3, quasi resonant converter topology is presented in details. The topological variations, switch networks control techniques are presented in this chapter.

In Chapter 4, circuit description, modes of operation and steady-state characteristics of the ZVS quasi-resonant buck converter are presented. The controller considerations and small-signal analysis are also presented in Chapter 4.

In Chapter 5, design considerations and procedure are presented. The overall circuit description is also presented in this chapter. Furthermore, simulation and experimental results and comparison between the simulation and experimental results are presented in

this chapter.

In Chapter 6, the experiment test procedure is presented in details. The requirements of the experiment and the experiment steps are also presented in this chapter.

CHAPTER 2

CONVENTIONAL PULSE-WIDTH MODULATION CONVERTERS

Modern electronic systems require high-quality, small, light-weight, reliable and efficient power supplies. Linear power regulators, whose principle of operation is based on a voltage or current divider, are inefficient [9]. Since their semiconductor devices operate in linear mode, these types of regulators dissipate much of their energy across the regulating semiconductor devices. Efficiency of these types of converters is very low (%30 to %60 for an output voltage less than 20 V). Moreover, they can only be used as step down regulators. Their main area of application is at low power levels.

Switching regulators use semiconductor switches in on and off states. Because there is a small power loss in those states (low voltage across a switch in the on state, zero current through a switch in the off state), switching regulators can achieve high-energy conversion efficiencies [9]. Modern power electronic switches can operate at high frequencies. As a result, switching regulators are preferred over linear regulators for their high efficiency and providing step-up, step-down or inverter output unlike linear regulators. Table 2.1 summarizes the differences between linear regulators and switching regulators.

In switching regulator circuits, semiconductor switches control the dynamic transfer of power from input to output with very short time transients. Because of this switching action there is ripple added to output voltage. The output requirement is a dc voltage

with a minimum superimposition of ac ripple. Pulse Width Modulation (PWM) is the most widely used method for controlling the output voltage. The switching frequency is kept constant and voltage regulation is achieved by controlling the duty cycle. Duty cycle is defined as the ratio of switch on time to reciprocal of the switching frequency.

Table 2.1 A comparison between the linear regulators and switching regulators

	Linear regulator	**Switching regulator**
Function	Only steps down.	Steps up or down, or inverts.
Efficiency	Low to medium and high if $V_{in} - V_{out}$ difference is small.	High.
Power loss	High if the average load or the input/output voltage differences are high.	Low, where components usually run cool.
Complexity	Low. Usually requires only the regulator and low-value bypass capacitors.	Medium to high. Usually requires inductor, diode, and filter caps in addition to IC.
Total cost	Low.	Medium to high, due to external components.
Ripple/Noise	Low. No ripple, low noise. Better noise rejection.	Medium to high, due to ripple at switching rate.

The output capacitor and output inductor are set in PWM converters to extract a clean dc voltage from the chopped AC voltage. They act as energy storage devices, smoothing out the pulsating energy drawn from the source.

The conventional PWM converters are not the scope of this thesis, therefore only buck converter will be considered throughout this thesis.

2.1 Basic Principles of PWM Buck Converter

Buck converter has non-isolated power stage topology, sometimes called a step-down power stage. It consists of dc input voltage source *V*, controlled switch *S*, diode *D*, filter inductor *L*, filter capacitor *C* and load resistance *R*. Figure 2.1 shows a simplified schematic of buck converter.

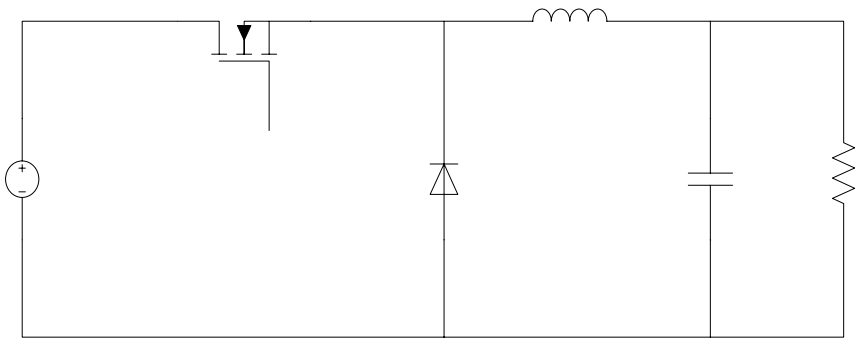

Figure 2.1 PWM buck converter.

The output voltage is always less than the input voltage. The input current for a buck converter is discontinuous, or pulsating, because the semiconductor switch current pulses from zero to the output current I_0 in every switching cycle. The output current of the buck converter is continuous, or non-pulsating, because the output current is supplied by the output filter network [10].

A power stage can operate in continuous or discontinuous inductor current mode. In continuous inductor current mode, current flows continuously through the inductor during the entire switching cycle in steady-state operation. In discontinuous inductor current mode, inductor current is zero for a portion of the switching cycle. It starts at

zero, reaches peak value, and returns to zero during each switching cycle. It is desirable for a buck power stage to stay in only one mode over its expected operating range because the power stage frequency response changes significantly between the two modes of operation [10].

2.2 Continuous Conduction Mode (CCM)

In continuous conduction mode, the entire switching period consists of two basic states. In the *on* state, the semiconductor switch *S* is *on* and the diode is *off*. On the other hand, in the *off* stage, the semiconductor switch *S* is *off* and the diode is *on*. Figure 2.2 shows two operation stages of CCM buck converter.

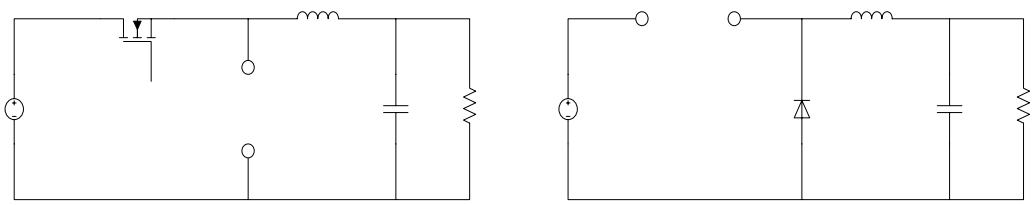

Figure 2.2 Power stages of buck converter.

The duration of the *on* state is:

$$DxT_S = T_{on} \tag{2.1}$$

where *D* is the duty cycle.

Typical waveforms of the CCM buck converter are shown in Figure 2.3.

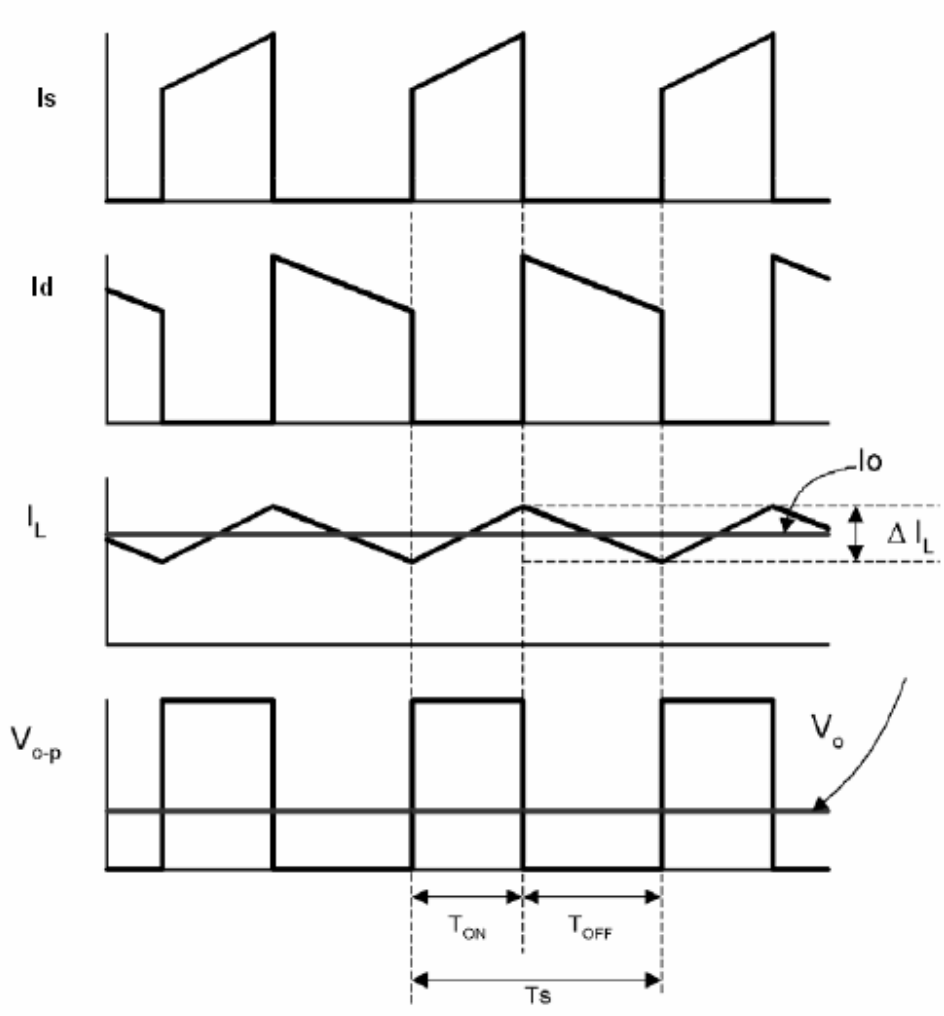

Figure 2.3 CCM buck converter basic waveforms.

The inductor current increase can be calculated by using the following formula:

$$V_L = Lx\frac{di_L}{dt} \Rightarrow \Delta i_L = \frac{V_L}{L}\Delta T \tag{2.2}$$

The inductor current increase (ripple current) during the *on* stage is given by:

$$\Delta i_L(+) = \frac{V - (V_S - I_L x R_L) - V_0}{L} x T_{on} \tag{2.3}$$

where V_S is the voltage drop on the semiconductor switch and R_L is the series resistance of the inductor.

The inductor current decrease during the *off* stage is given by:

$$\Delta i_L(-) = \frac{V_0 + (V_D + I_L x R_L)}{L} x T_{off} \tag{2.4}$$

where V_D is the forward voltage drop of the diode and R_L is the series resistance of the inductor.

At steady-state conditions, the current increase, $\Delta i_L(+)$, during the *on* time and the current decrease, $\Delta i_L(-)$, during the *off* time are equal because of the volt-second balance of the inductor. Therefore, these two equations can be equated and solved for V_0 to obtain the continuous conduction mode (CCM) buck voltage conversion relationship:

$$V_0 = (V - V_S)x\left(\frac{T_{on}}{T_{on} + T_{off}}\right) - V_D x\left(\frac{T_{on}}{T_{on} + T_{off}}\right) - I_L x R_L \tag{2.5}$$

And,

$$D = \frac{T_{on}}{T_{on} + T_{off}} = \frac{T_{on}}{T_S} \qquad \Rightarrow \qquad (1 - D) = \frac{T_{off}}{T_S} \tag{2.6}$$

The steady-state voltage conversion ratio is:

$$V_0 = (V - V_S)xD - V_D(1 - D) - I_L x R_L \tag{2.7}$$

The above voltage conversion relationship for output voltage illustrates that the output voltage can be adjusted by changing the duty cycle, D, and is always less than the input because D lies between 0 and 1. A common simplification is to assume V_S, V_D and R_L small enough to ignore. The above equation then simplifies to [10]:

$$V_0 = DxV \tag{2.8}$$

It is noted that the inductor delivers current to the output capacitor and load resistor combination during the whole switching cycle. The inductor current averaged over the switching cycle is equal to the output current. This is expected because the average current in the output capacitor must be zero [10].

2.3 Discontinuous Conduction Mode (DCM)

Figure 2.4 shows the inductor current condition where the power stage is at the boundary between continuous and discontinuous modes. This is where the inductor current just falls to zero and the next switching cycle begins immediately after the current reaches zero. From charge and discharge of output capacitor, the output current is given by [10]:

$$I_o x(T_{on} + T_{off}) = \frac{I_{pk}}{2} x(T_{on} + T_{off}) \Rightarrow I_{pk} = \Delta I_L = 2I_o \tag{2.9}$$

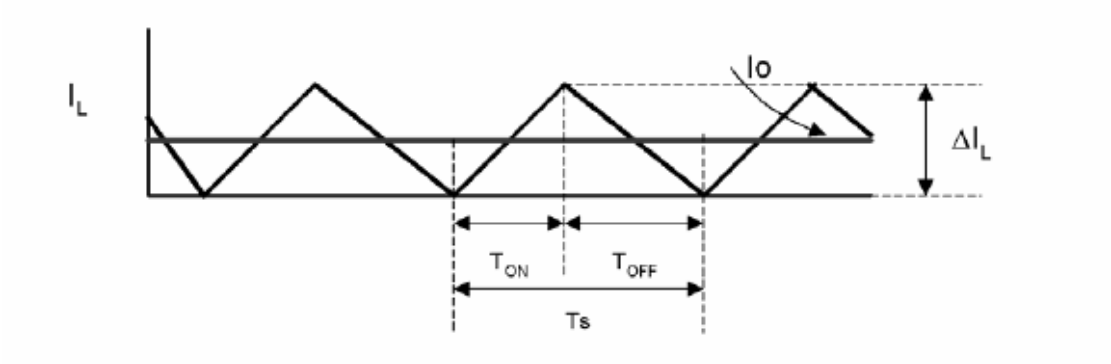

Figure 2.4 Boundary between continuous and discontinuous modes.

Further reduction in output load current puts the power stage into discontinuous conduction mode (DCM). The discontinuous mode converter input-to-output relationship is quite different from the continuous mode. Figure 2.5 shows the discontinuous mode output inductor current waveform.

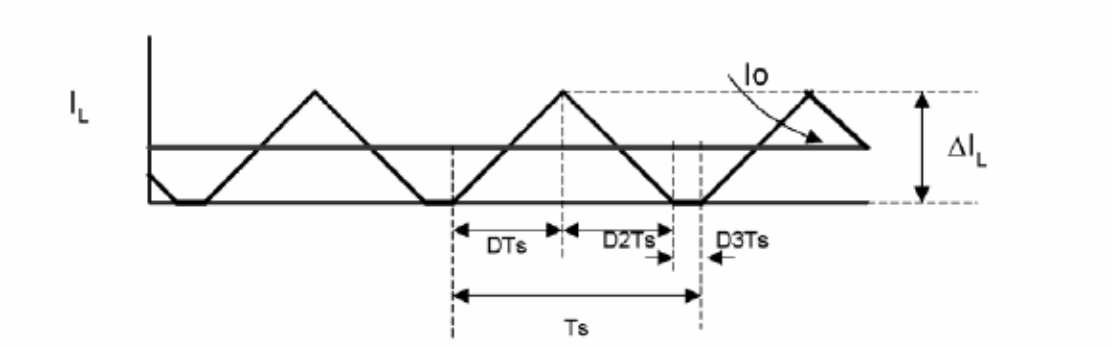

Figure 2.5 Discontinuous mode inductor current.

The duration of the *on* state is:

$$T_{on} = DxT_S \tag{2.10}$$

where *D* is the duty cycle of the converter.

The duration of the *off* state is:

$$T_{off} = D2xT_S \tag{2.11}$$

The idle time is the remainder of the switching cycle and is given as:

$$T_S - T_{on} - T_{off} = D3xT_S \tag{2.12}$$

The inductor current increase during the *on* state is given by:

$$\Delta I_L(+) = \frac{V - V_0}{L} xT_{on} = \frac{V - V_0}{L} xDxT_S = I_{pk} \tag{2.13}$$

The ripple current magnitude, $\Delta I_L(+)$, is also the peak current in discontinuous mode. The current starts from zero in each cycle. The inductor current decrease during the off state is given by:

$$\Delta I_L(-) = \frac{V_0}{L} xT_{off} = \frac{V_0}{L} xD2xT_S \tag{2.14}$$

As in the continuous mode case, the current increase during the *on* time and the current decrease during the *off* time are equal for critical mode. So,

$$V_0 = Vx\frac{T_{on}}{T_{on}+T_{off}} = Vx\frac{D}{D+D2} \tag{2.15}$$

From Eq.(2.9) to Eq.(2.15), the voltage relationship of the discontinuous mode buck converter is given by:

$$V_0 = Vx\frac{2}{1+\sqrt{1+\frac{4xK}{D^2}}} \tag{2.16}$$

where

$$D = Mx\sqrt{\frac{K}{1-M}} \tag{2.17}$$

$$K = \frac{2xL}{RxT_S} \tag{2.18}$$

$$M = \frac{V_0}{V} \tag{2.19}$$

2.4 Critical Inductance

The conduction mode of the power stage is a function of input voltage, output voltage, output current and the value of the inductor. A buck converter can be designed to operate in continuous mode for load currents above a certain level, generally 5 to 10% of full load. The input voltage range, the output voltage and load current are defined by the power specifications of the converter. The inductor value as the design parameter is used to maintain continuous conduction mode [10].

For the boundary situation between CCM and DCM, the following expression can be written:

$$I_{OB} = I_{LB} = \frac{\Delta I_L}{2} \tag{2.20}$$

where I_{OB} is the minimum output current to maintain continuous conduction mode.
On boundary:

$$V_0 = DxV \tag{2.21}$$

$$I_{OB} = \frac{V - V_0}{2xL} xDxT_S = \frac{V_0 x(1-D)xT_S}{2xL} = \frac{VxDx(1-D)xT_S}{2xL} \tag{2.22}$$

Continuous conduction mode:

$$I_0 \geq I_{OB} = \frac{VxDx(1-D)xT_S}{2xL} \tag{2.23}$$

$$L_{\min} \geq \frac{V_0 x(1-D)xT_S}{2xI_{OB}} = \frac{V_0 x(1-\frac{V_0}{V_{(\max)}})xT_S}{2x\frac{P_{0(\min)}}{V_0}} \tag{2.24}$$

2.5 Output Capacitor

In switching power supply power stage, the function of the output capacitor is to store energy. The output capacitance of the buck converter is generally selected to limit output voltage ripple to the level required by the specification. The series impedance of the output capacitor and the power stage output current determine the output voltage

ripple. The three elements of the capacitor that contribute to its impedance are equivalent series resistance (ESR), equivalent series inductance (ESL) and capacitance (C). The value of its capacitance can be calculated from the following expression [10]:

$$C = \frac{Q}{\Delta V_0} \tag{2.25}$$

The value of ΔV_0 is the maximum change of the output voltage, and Q is the charge transferred from the capacitor C to the load during one cycle. The capacitor will be charged provided that the current in the inductor is larger than the load current I_0. The area shaded corresponds to the change of the charge Q in the capacitor C as shown in Figure 2.6 [10].

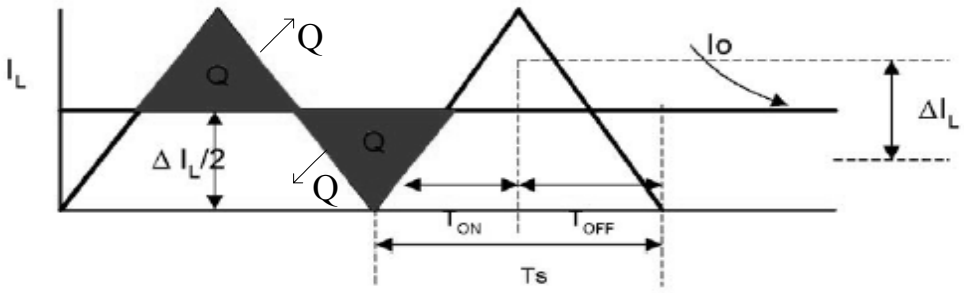

Figure 2.6 Charge Q change in capacitor.

$$Q = \Delta I_L xt = \frac{1}{2}(\frac{1}{2}\Delta I_L x \frac{1}{2f}) = \frac{\Delta I_L}{8f} \tag{2.26}$$

For CCM:

$$C \geq \frac{Q}{\Delta V_0} = \frac{\Delta I_L}{8\, f x \Delta V_0} \tag{2.27}$$

$$\Delta I_L = \frac{(V - V_0) x T_{on}}{L} = \frac{(V - V_0) x D x T_S}{L} \tag{2.28}$$

For DCM:

$$C \geq \frac{I_{0(\max)} x (1 - \frac{I_{0(\max)}}{\Delta I_L})^2}{f_s x \Delta V_0} \tag{2.29}$$

The ripple voltage across the output capacitance is determined by the size of the filter capacitor. The equation (2.29) is based on the assumption that all inductor ripple current flows through the capacitor and the ESR is zero.

2.6 Control Principles

A dc-dc converter must provide a regulated dc output voltage under varying load and input voltage conditions. The two most common closed-loop control methods for PWM converters, namely, the voltage-mode control and the current-mode control, are presented in Figure 2.7.

In the voltage-mode control, the output voltage of the converter is sampled and subtracted from an external reference voltage in an error amplifier. The error amplifier produces a control signal. This control signal is compared to a constant-amplitude constant-frequency sawtooth waveform. The comparator produces a PWM signal in order to control the semiconductor switch in the dc-dc converters. The duty cycle of the PWM signal depends on the value of the control voltage. The frequency of the PWM signal is the same as the frequency of the sawtooth waveform. The voltage-mode control

method is simple and flexible. The main control scheme of the voltage-mode control is shown in Figure 2.7 (a).

The current-mode control has an additional inner control loop feeds back an inductor current signal. This signal is converted into its voltage equivalent, and is compared to the control voltage. The main control scheme of the current-mode control is shown in Figure 2.7 (b).

The inner loop is used to control the inductor current, thus eliminating the inductor effects on the power stage transfer function. The transfer function of the power stage includes the closed loop and current loop. The effect of the inductor is completely absorbed by the loop controlling it. Advantages of the current-mode control are the input voltage feedforward, the limit on the peak switch current and the reduction in the converter dynamic order. The main disadvantage of the current-mode control is its complicated hardware [3].

2.7 Control Schemes and Compensation Considerations

Negative feedback is applied to maintain voltage regulation due to disturbances in input voltage, load current or variations in component values. The duty cycle is varied in the feedback loop to compensate for these variations.

Almost any feedback or any loop can be divided into two major portions. One is the power-processing portion that takes a control signal as an input and outputs the variable to be controlled. This portion is called the modulator or plant. The other portion is error amplifier, which compares a sample of the controlled output to a reference, amplifies the difference, and outputs a control signal to the modulator or plant. This portion is usually called the amplifier. Figure 2.8 shows the definition of these two blocks in a typical dc-dc converter [11].

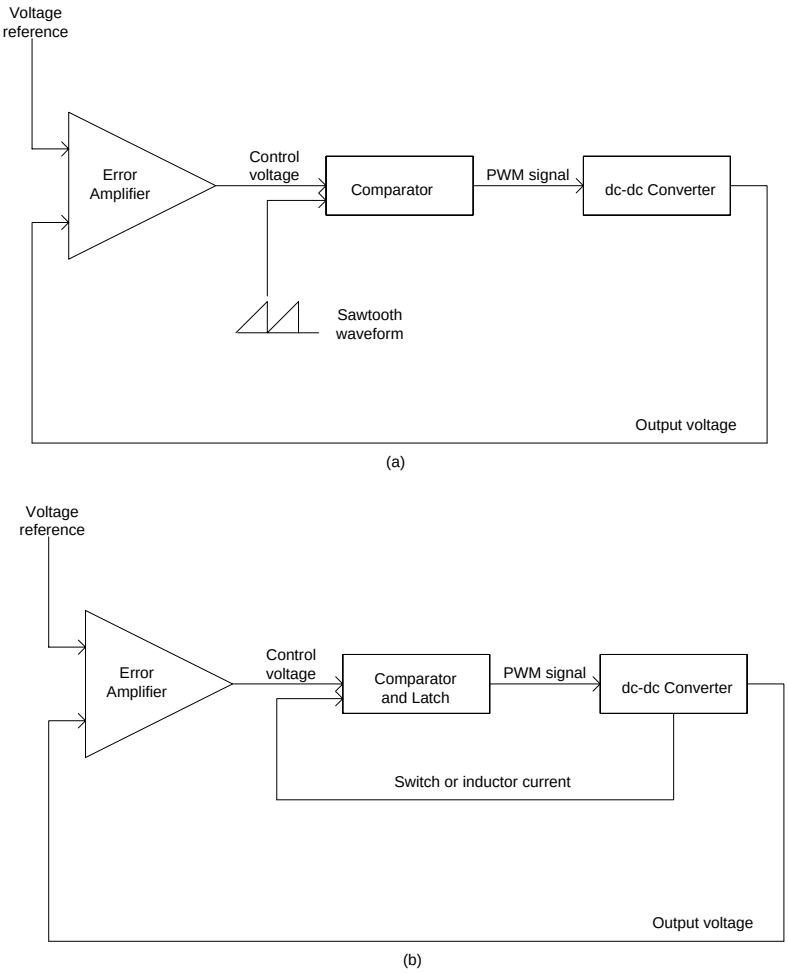

Figure 2.7 Main control schemes for dc-dc converters:
(a) voltage-mode control
(b) current-mode control.

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In multi-loop control systems, the basic idea is the same. The difference is that the reference usually comes from an outer loop. Each loop must be considered starting with the innermost loop for multi-loop control systems.

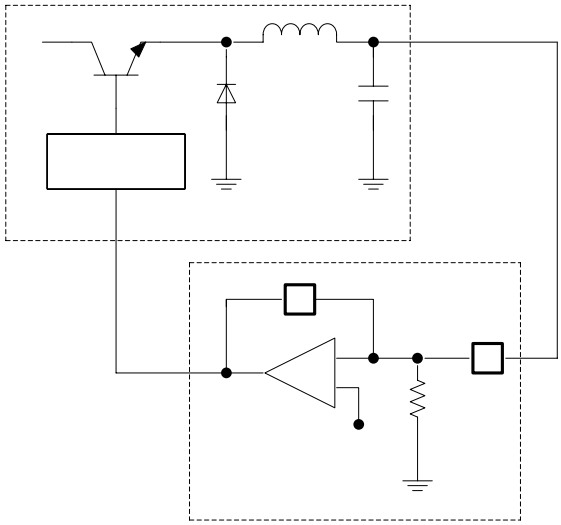


Figure 2.8 Typical feedback control loop.

2.7.1 Frequency Response of Buck Converter

The first step in designing the feedback loop after selecting the components of the converter is to plot the open-loop response of buck converter. The transfer function of output voltage to duty cycle is derived in the beginning of this chapter. The transfer function reveals a left-half plane zero associated with Equivalent Series Resistor (ESR) of the capacitor and a double pole at approximately resonant frequency of LC. Typically, the transfer characteristic peaks at resonant frequency. The magnitude of this peak is given by the quality factor. Ignoring the inductor series resistance and transistor on resistance, a simple expression for quality factor Q can be derived in terms of L, C, R and ESR of the capacitor. It can be easily deduced that Q gets lowered as a result of ESR of the capacitor [11].

$$Q \cong \frac{1}{\left[\sqrt{\frac{L}{C(R+R_c)R}} + R_c\sqrt{\frac{R_c}{R+R_c}}\right]} \approx \frac{R}{\sqrt{\frac{L}{C}}} = R\sqrt{\frac{nC'}{L}} \tag{2.30}$$

The asymptotic plot for open-loop response with corner frequencies is as shown in Figure 2.9. The corner frequencies are approximated as:

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} = \frac{Q}{2\pi RC} = \frac{Q}{2\pi nRC'} \tag{2.31}$$

$$f_{ESR} \cong \frac{1}{2\pi R_c C} = \frac{1}{2\pi R_c' C'} \tag{2.32}$$

where

$$C = nC' \tag{2.33}$$

$$R_c = \frac{R_c'}{n} \tag{2.34}$$

The inductor is fixed by current ripple requirement and the capacitor is chosen large enough such that Q is small. Thus, in a well constructed system,

$$BW \le 1/4\, f_{sw} \tag{2.35}$$

$$BW \ge 8-10\, f_{LC} \tag{2.36}$$

$$f_{ESR} \ge 2\, f_{LC} \tag{2.37}$$

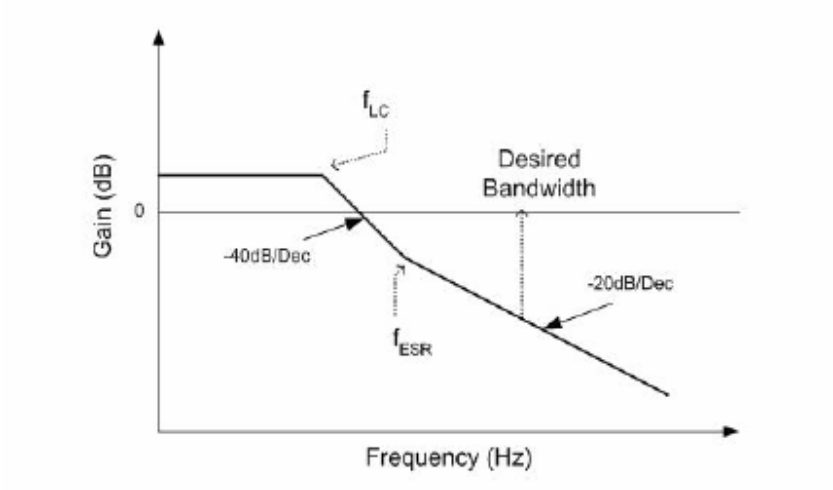


Figure 2.9 Open-loop response of buck converter.

Compensation is designed in such a way that the total loop gain transfer function crosses 0 dB point with -20 dB/dec slope. This ensures sufficient phase margin and in turn closed loop stability. Typical phase margins range from 45º to 75º. Lower margins, like 45º, give good transient response at the expense of peaking of the closed-loop transfer function and output impedance. Higher margins, like 75º, give flat closed-loop transfer functions and minimum peaking of output impedance, but at the expense of speed and settling time [11].

2.7.2 Optimum Compensator Design

Since optimum performance is obtained from maximizing low frequency gain and minimizing high frequency gain, it stands to reason that an integrator is the logical starting choice for a compensator design. General compensator circuits and their Bode diagram are investigated from this point [11].

Since the phase lag of one-pole error amplifier is 270º at all frequencies, no opportunity

exists to control the amount of phase lag through the amplifier. By placing a zero-pole pair in the transfer function, however, the phase lag can be reduced to less than 270º over some range of frequencies. A zero in a transfer function causes the slope of the gain curve of a Bode plot to break upward with increasing frequency, and is accompanied by a reduction of phase lag 45º at the corner, and up to 90º at frequencies much higher than the frequency at which the zero occurs. A pole in the transfer function has the opposite effect, causing the slope of the gain curve of a Bode plot to break downward, and is accompanied by an increase in phase lag of 45º at the corner, and up to 90º at frequencies much higher than the frequency at which the pole occurs. A zero-pole pair introduced into the transfer function of an integrator creates a region of frequencies in which the Bode gain plot goes flat and the phase lag is reduced by an amount related to the frequency spread between the zero and pole. This reduction in lag through the error amplifier can be named as a phase boost, and this concept of phase boost is very powerful in understanding the nature of loop compensation. The amount of phase boost can be varied easily by adjusting the spread of the zero-pole pair, and desired phase margin can be obtained by adjusting the spread of the zero-pole pair [11].

CHAPTER 3

QUASI-RESONANT CONVERTERS

In most solid-state power processing circuits, efficiency is very important. To achieve high efficiency, it is necessary to operate the power processing circuit in the switch-mode. The semiconductor switch of the power processing circuit is either completely turned on (saturation state) or completely turned off (cut-off state).

In order to achieve desired power conversion, output voltage regulation, isolation and noise suppression, magnetic components and capacitors are vital for design of power converters. The use of these energy storage passive devices creates extraneous burden on the power semiconductor devices.

The increasing demand for higher power density and high performance converters has led to an increase of the switching frequency. Operating at high frequencies, the size and weight of the energy storage elements are reduced and the dynamic performance of the converter circuit is improved. High power density and high performance converters are important for applications in military, aerospace and computer and telecommunication areas. Due to the increasing high frequency and switching under sharp transitions of both current and voltage, power semiconductor devices are subjected to high switching losses and high switching stresses.

As the power semiconductor technology is rapidly evolving, many power devices are made available for power processing applications. Each type of power semiconductor

device has its special merits and limitations. Among other semiconductor devices, the majority carrier devices, such as power MOSFET, have ultra-high switching speed and are ideal for high frequency, low-power applications. Its turn-off time is very short due to the absence of carrier recombination phenomena. However, like all other power semiconductor devices, the MOSFET has parasitic junction capacitances. When operated at very high frequency, the turn-on switching loss due to the discharging of the junction capacitances can be a limiting factor [12].

When the MOSFET switch turns on at a high voltage level, the energy stored in the semiconductor device's output capacitance, $0.5CV^2$, is dissipated internally when the device is turned on. The switching loss due to this turned-on discharging of the output capacitance is a major concern. The detrimental effects of parasitic elements are more pronounced as the switching frequency increased.

Soft switching techniques have been developed to reduce switching losses, switching stresses and allowing efficient power conversion in high frequency operations. Soft switching techniques for the switching devices can be either zero-current switching (ZCS) or zero-voltage switching (ZVS). Zero-current switching is achieved by turning off the switches when no current circulating through them. Zero-voltage switching is achieved by turning on the switches when there is no voltage applied across them [13].

Several soft switching power conversion techniques have been proposed to decrease the detrimental effects of the parasitic reactances and improve the switching conditions of the semiconductor devices. These techniques include: resonant converters, quasi-resonant converters, class-E converters, multi-resonant converters, forward resonant converters and resonant transition converters. Each of these techniques reduces losses in the power switch by operating with either zero-current turn-off or zero-voltage turn-on.

All soft switching techniques use the resonant network (L-C) for QRCs and (L-C-C or L-L-C) for MRCs added around the switches. These energy storage elements shape the

current or voltage to achieve zero-current switching or zero-voltage switching of the switching devices.

3.1 Quasi-Resonant Converters

Quasi-resonant conversion technique offers a general approach for improvement of switching conditions. The quasi-resonant converters are directly derived from conventional PWM topologies. This family of circuits can be viewed as a hybrid of PWM and resonant converters. The resonant action takes place only one mode of these converters and this is why they are called the “quasi-resonant converters”.

When energy is applied into an L-C resonant tank circuit, the energy is exchanged between the inductor and the capacitor in a periodical and quasi-sinusoidal form. Because of this quasi-sinusoidal oscillation, L-C resonant tank circuit can be used as a lossless or low-loss waveform-shaping device.

3.2 Quasi-Resonant Switch

A quasi-resonant switch network consists of semiconductor switch and resonant elements, inductor and capacitor. By replacing the conventional switch by the resonant switch network, a favorable condition is created for the switching device during switching transitions. The quasi-resonant switch is divided into two different resonant networks: zero-current resonant switch, zero-voltage resonant switch.

a) Zero-Current Quasi-Resonant Switch

In zero-current quasi-resonant switch, the active switch S is in series with the resonant inductor, while the rectifier diode is in parallel with the resonant capacitor. Figure 3.1 shows the basic zero-current resonant switch network. The resonant circuit is formed either in M-type or L-type with respect to the resonant capacitor. The inductor and the

capacitor constitute a series resonant circuit and this resonance action occurs during the major portion of the on time. The arrangement of the zero-current resonant switch absorbs the parasitic reactance of the transformer and the rectifier diode [14].

If the ideal switch is implemented by a unidirectional one, the switch current is permitted to resonate only in the positive half cycle. A diode is connected in series with the active switch S; therefore the zero-current resonant switch is implemented as a *half-wave network*. On the other hand, if a diode is connected in anti-parallel with the active switch allowing bidirectional current flow, this implementation is called *full-wave network*. Figure 3.2 shows half-wave and full-wave zero-current resonant switching networks in both M-type and L-type [15].

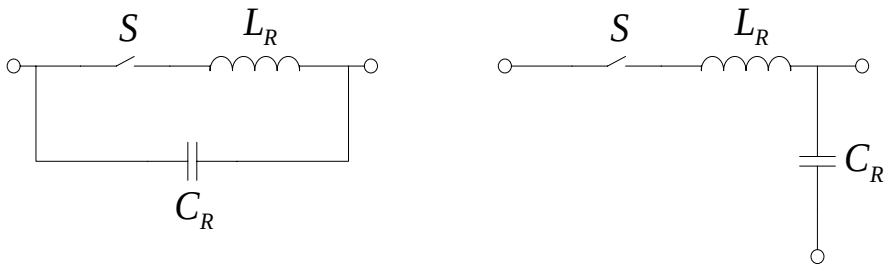


Figure 3.1 Zero-current resonant switches.

In general, most switching converters need to turn on or turn off the full load current at high voltage applied across them, resulting in hard switching. The switching behavior of the PWM, shown as trajectory A in Figure 3.3, traverses high stresses region because of simultaneous high voltage and high current. As stated before, in soft-switching converter topologies, an LC resonant network is added to shape the switching device's current or voltage waveforms in such a way that zero-current or zero-voltage condition is created. Since no simultaneous high voltage and current are subjected to switching

device, the switching stresses and losses are reduced as shown by the trajectory B in Figure 3.3 [5].

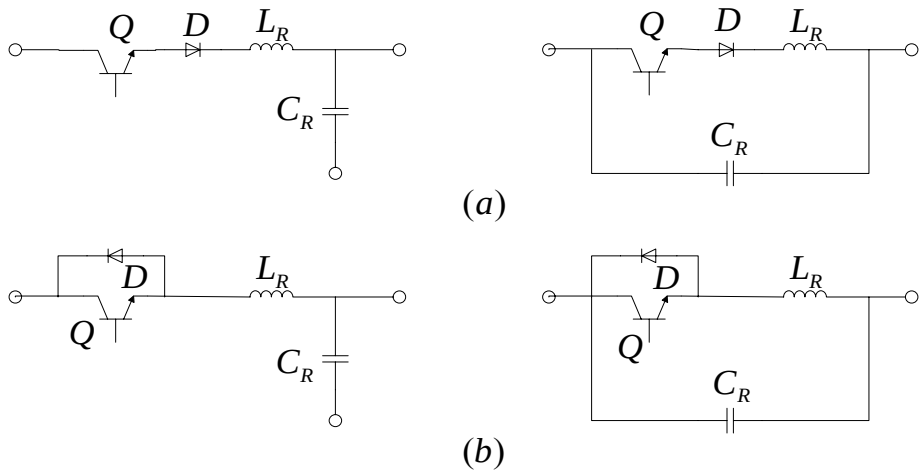


Figure 3.2 ZC-resonant switch configurations
(a) half-wave configuration
(b) full-wave configuration.

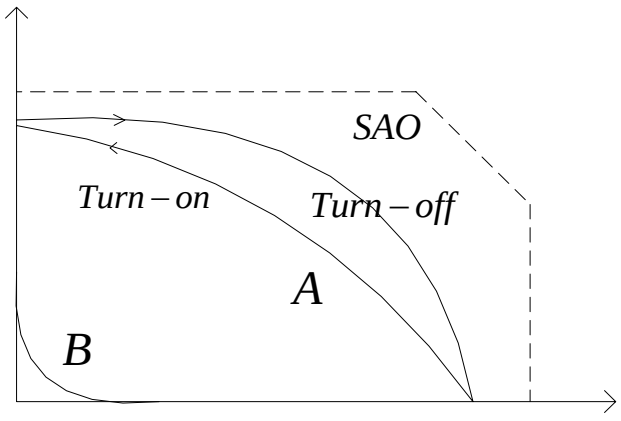


Figure 3.3 Load line trajectories.

b) Zero-Voltage Quasi-Resonant Switch

In zero-voltage quasi-resonant switch, the active switch S is in parallel with the capacitor, and the diode is in series with the inductor. Figure 3.4 shows the basic zero-current resonant switch network. The resonant network is again either of M-type or L-type as in the zero-current resonant network. In zero-voltage resonant switches, the resonant interaction occurs during the major portion of the off time. The arrangement of the zero-voltage resonant switch absorbs the parasitic reactance of the transformer and the active switching device [16].

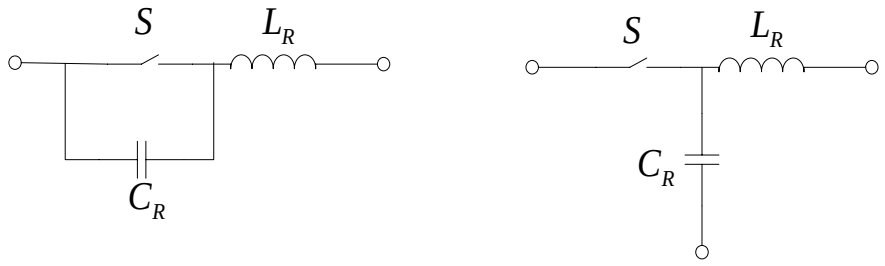


Figure 3.4 Zero-voltage resonant switches.

If a diode is connected in anti-parallel with the active switch, the voltage across capacitor C_R is clamped by the diode at zero during negative half of the resonant cycle. This implementation is called *half-wave network*. If this diode is connected in series with the active switch, the voltage across capacitor C_R oscillates freely, and this arrangement is called *full-wave network*. Figure 3.5 shows half-wave and full-wave zero-voltage resonant switching networks in both M-type and L-type.

Table 3.1 summarizes the major characteristics of the zero-current and zero-voltage quasi-resonant converters.

3.3 Topological Variations

The concept of resonant switch can be applied to a large number of conventional PWM switching converters. Simply by replacing the switch in any conventional PWM converters by a zero-current resonant switch or zero-voltage resonant switch, a family of quasi-resonant converters is derived. Some basic converter topologies and their resonant counterparts are presented in Figure 3.6 as ZCS quasi-resonant converters and Figure 3.7 as ZVS quasi-resonant converters. For a given family of QRCs, M-type and L-type resonant switch topologies have the same set of state equations; therefore they have the same circuit operations. The only difference is in the voltage waveform of the resonant capacitors [14].

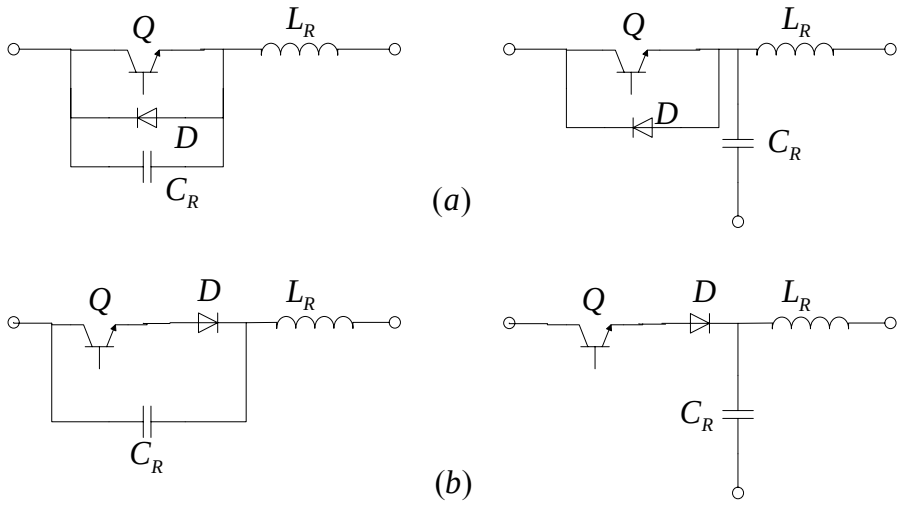


Figure 3.5 ZV-resonant switch configurations
(a) half-wave configuration
(b) full-wave configuration.

Table 3.1 Major characteristics of the zero-current and zero-voltage QRCs

	Zero-Current Switching	**Zero-Voltage Switching**
Control	Constant on-time	Constant off-time
Switch voltage waveform	Quasi-square	Quasi-sinusoidal
Switch current waveform	Quasi-sinusoidal	Quasi-square
Load range	$\{R_{min}, R_{\infty}\}$	$\{0, R_{max}\}$
V_0/V_i increases as	f_s increases	f_s decreases
V_0/V_i increases as	R increases	r increases
Full-wave mode	D in anti-parallel with Q	D in series with Q
Half-wave mode	D in series with Q	D in anti-parallel with Q

3.4 Control of Quasi-Resonant Converters

The quasi-resonant converters can be controlled by variable frequency control technique. In ZCS quasi-resonant converters, the resonant frequency of resonant inductor and resonant capacitor dictates the duration of the on time. As a result, these converters operate with a fixed on time, and the output is regulated by varying the off time. On the other hand, ZVS quasi-resonant converters operate with fixed off time, and output is regulated by varying the on time. General variable frequency control scheme of the resonant converters is illustrated in Figure 3.8.

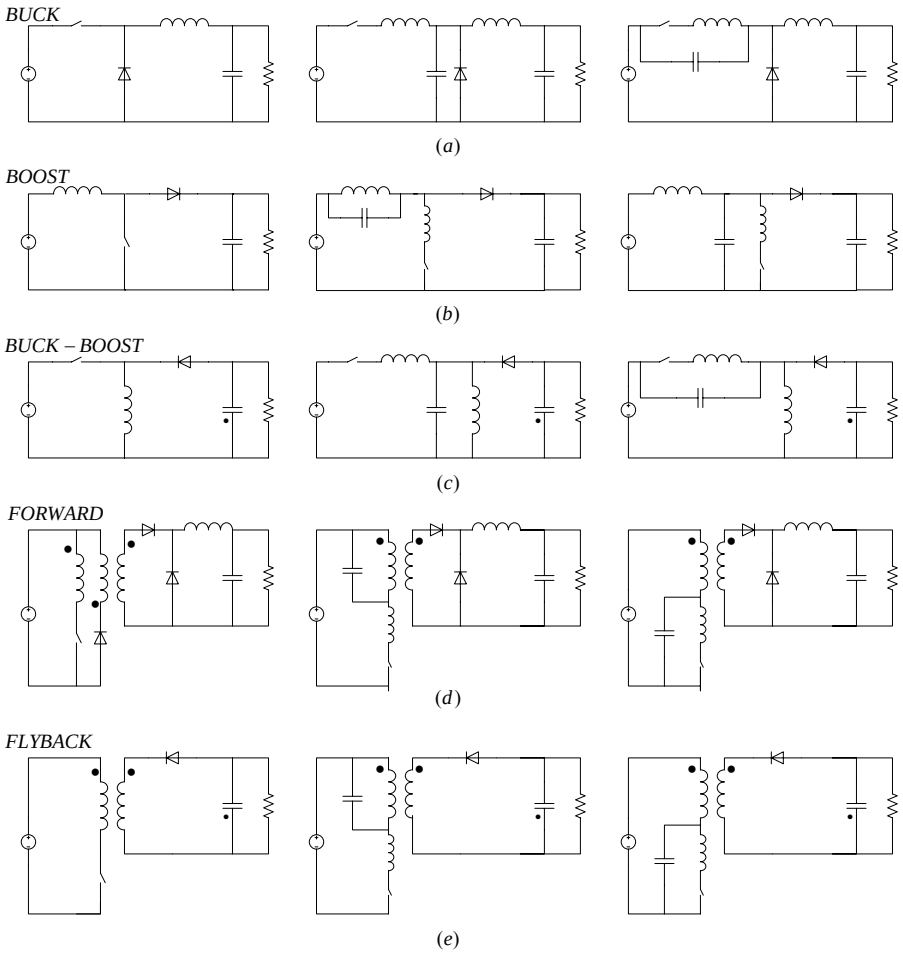


Figure 3.6 A family of ZCS quasi-resonant converters
(a) buck
(b) boost
(c) buck-boost
(d) forward
(e) flyback.

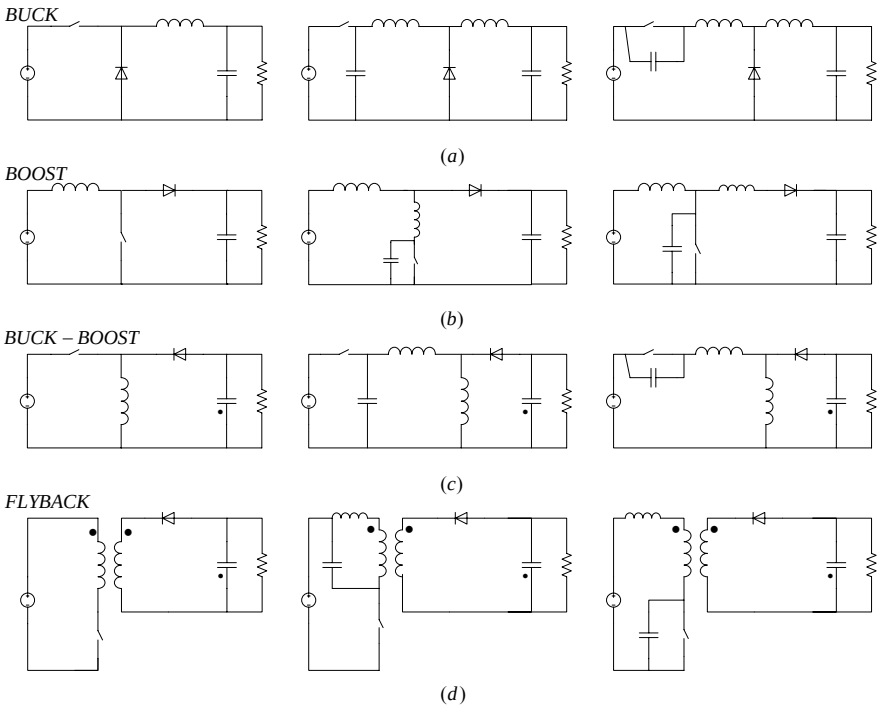


Figure 3.7 A family of ZVS quasi-resonant converters
(a) buck
(b) boost
(c) buck-boost
(d) flyback.

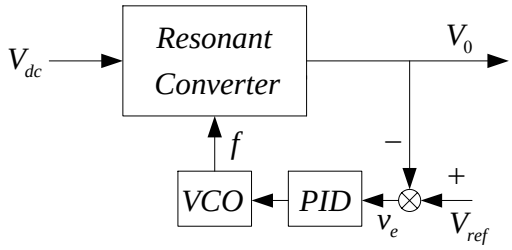


Figure 3.8 General variable frequency control scheme.

The quasi-resonant converters have two main control schemes: single-loop control and multi-loop control. For single-loop controlled converters, closed-loop regulation of the output voltage can be achieved by feedback of the output voltage through an error amplifier circuit and voltage controlled oscillator (VCO). This control scheme is very similar to constant on-time or constant off-time duty-cycle modulation of PWM converters. The output of the error amplifier controls the VCO that determines the on time or off time of the active switch. Finally, DSP (Digital Signal Processor) or other control logics converts the output signal of the VCO into constant on-time or constant off-time pulses. The single loop control scheme can be very difficult to compensate the converters such as boost, buck-boost and flyback because of their right-half plane zeros. Multi-loop control is very effective for controlling the quasi-resonant converters. By sensing the inductor current, two loops, namely voltage and current, is formed. Furthermore, the VCO is replaced with a simple comparator; therefore the output signal is less noise sensitive.

Current-mode control is actually a very simple form of multi-loop feedback. There is very little freedom in the design of the current loop. Its gain can be adjusted with the addition of an external ramp, but its frequency response is usually unchanged. The gain of the current loop should always be as high as possible without causing instability [14].

To design the control circuit for dc-dc converters, a dynamic analysis has to be carried out and the loop gain has to be obtained. The loop gain will help to design a control circuit that satisfies the system closed loop requirements. The concepts of loop gain crossover frequency, phase margin, gain margin and stability of a system are directly related to the closed loop characteristics and the system feedback loop gain can be used to obtain the dynamic characteristics [17].

CHAPTER 4

ZVS QUASI-RESONANT BUCK CONVERTER ANALYSIS

As mentioned before, a resonant switch represents a network consisting of a semiconductor switch and resonant elements such as inductors and capacitors. In voltage-mode resonant switch, the resonant capacitor is in parallel with the semiconductor switch to achieve zero voltage switching. Buck-type is the basic PWM converter where the quasi-resonant concept can easily be applied.

When operating in the half-wave mode, voltage-conversion ratio is sensitive to load variations and when operating in the full-wave mode, voltage-conversion ratio is insensitive to load variations. Although full-wave mode of operation has an advantage of load insensitivity, the diode should be connected in series with the semiconductor switch, because semiconductor power switches have no reverse voltage blocking capacity. The switching losses due to the parasitic junction capacitance lower the efficiency of the converter in the full-wave operation. Nevertheless, the parasitic junction capacitance can be utilized as part of resonant element in the half-wave operation [6].

The major benefit of the full-wave operation is greatly-reduced frequency range hence small filter requirements for the load [18].

4.1 ZVS Quasi-Resonant Buck Converter

A basic circuit diagram of the buck ZVS QRC is shown in Figure 4.1. Inductance L_R and capacitor C_R form a resonant network. This network shapes the voltage across switch S during its off time for zero-voltage turn-on. The circuit operates in half-wave mode. The output filter consists of L_F and C_F, and D_0 is a freewheeling diode (typically Schottky rectifier).

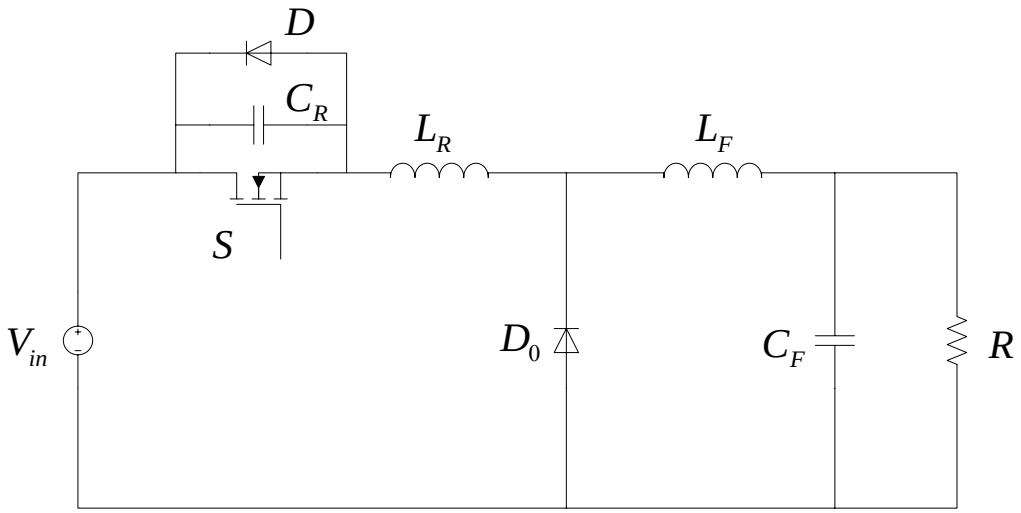


Figure 4.1 Basic circuit diagram of buck ZVS QRC.

For buck converters, the conversion ratio M is defined by:

$$M = \frac{V_0}{V_{in}} \tag{4.1}$$

where V_0 is the output voltage and V_{in} is the input dc voltage.

The operation and characteristics of the converter depend mainly on the design of the resonant circuit L_R and C_R. The following parameters determine the converter characteristics:

Characteristic Impedance Z_N:

$$Z_N = \sqrt{\frac{L_R}{C_R}} \tag{4.2}$$

Resonant Frequency f_R:

$$f_R = \frac{1}{2\pi\sqrt{L_R C_R}} \tag{4.3}$$

Normalized Load Resistance r:

$$r = \frac{R}{Z_N} \tag{4.4}$$

where R is the load resistance of the converter.

4.2 Modes of Operation

Typical theoretical waveforms of the buck ZVS QRC are shown in Figure 4.2. A complete converter switching cycle is divided into four intervals; capacitor charging stage (t_0-t_1), resonant stage (t_1-t_2), inductor discharging stage (t_2-t_3) and freewheeling stage (t_3-t_4) [13].

Prior to t_0, switch S is conducting. Consequently, the diode D_0 is reverse-biased, and the output current flows through the load.

4.2.1 Capacitor-Charging Stage (t_0-t_1)

At the beginning of this interval, at t_0, the switch S is turned off, the output current starts to flow through the resonant capacitor (diode D_0 is still reverse-biased) and voltage v_{DS} increases linearly. When v_{DS} is equal to the input voltage, diode D_0 turns on.

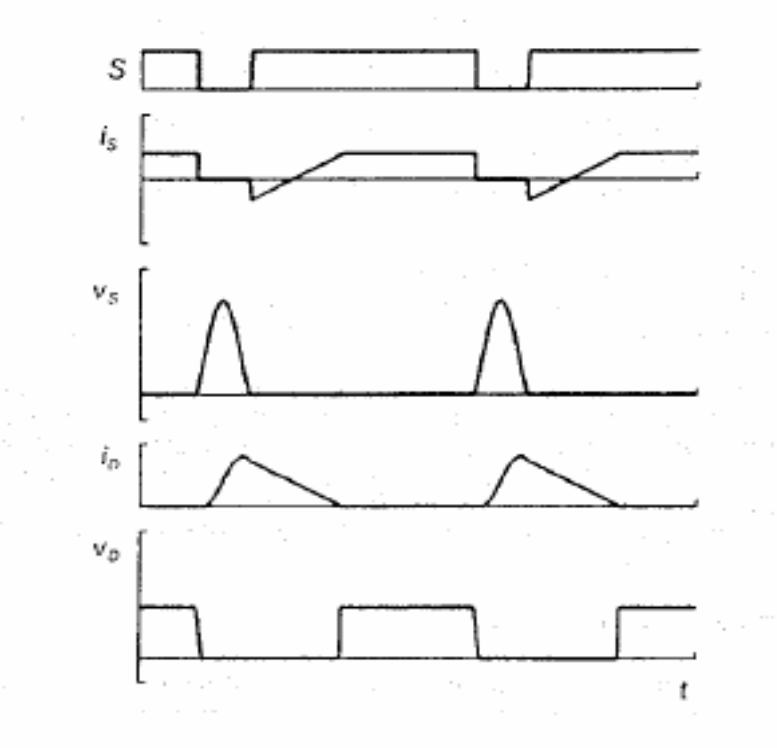


Figure 4.2 Theoretical Waveforms of buck ZVS QRC.

Initial Condition:

$$V_{DS}(0) = 0 \tag{4.5}$$

State Equation:

$$C_R \frac{dv_c}{dt} = I_0 \tag{4.6}$$

Time Solution:

$$T_{01} = \frac{C_R V_{in}}{I_0} = \frac{1}{w} \frac{r}{M} \tag{4.7}$$

where

$$w = 2\pi f_R \tag{4.8}$$

4.2.2 Resonant Stage (t_1-t_2)

This interval begins when the capacitor voltage V_{DS} reaches V_{in} and the rectifier diode D_0 becomes forward biased. This causes the resonant element to resonate. During resonance, the voltage of the resonant capacitor C_R across the switch reaches its peak value:

$$V_{DSpeak} = I_0 Z_N + V_{in} \tag{4.9}$$

The resonant action of C_R and L_R causes V_{DS} to decrease to zero at t_2.

Initial Conditions:

$$I_{LR}(0) = I_0 \tag{4.10}$$

$$V_{DS} = V_{in} \tag{4.11}$$

State Equations:

$$L_R \frac{dI_{LR}}{dt} = V_{in} - V_{DS} \tag{4.12}$$

$$C_R \frac{dV_{DS}}{dt} = I_{LR} \tag{4.13}$$

Time Solutions:

$$I_{LR}(t) = I_0 \cos wt \tag{4.14}$$

$$V_{DS}(t) = V_{in} + I_0 Z_N \sin wt \tag{4.15}$$

$$T_{12} = \frac{\alpha}{w} \tag{4.16}$$

where

$$\alpha = \begin{cases} \pi + \arcsin\left(\frac{V_{in}}{Z_N I_0}\right) \text{ for half-wave mode } t_2 = T_a \\ 2\pi - \arcsin\left(\frac{V_{in}}{Z_N I_0}\right) \text{ for full-wave mode } t_2 = T_b \end{cases} \tag{4.17}$$

In the half-wave mode, when V_{DS} drops to zero at T_a, it is clamped at that value by the anti-parallel diode, which carries the reverse current. While in the full-wave mode of operation, V_{DS} continues to oscillate to a negative value and returns to zero at time T_b. For half-wave operation, the end of this stage, t_2, is equal to T_a; for the full-wave operation, it is equal to T_b.

4.2.3 Inductor-Charging Stage (t_2-t_3)

When V_{DS} reaches zero, the anti-parallel diode turns on. Now the resonant capacitor is shorted and the input voltage is applied to L_R. Therefore, the current I_{LR} starts increasing linearly until it reaches the value of the output current.

Initial Condition:

$$I_{LR}(0) = I_0 \cos\alpha \tag{4.18}$$

State Equation:

$$L_R \frac{di_{LR}}{dt} = V_i \tag{4.19}$$

Time Solution:

$$T_{23} = \frac{1}{w}\frac{Z_N I_0}{V_{in}}(1-\cos\alpha) \tag{4.20}$$

4.2.4 Free-Wheeling Stage (t_3-t_4)

At this moment, diode D_0 turns off. During this interval, active switch S conducts the output current. The duration of this interval is a control parameter and is determined by:

$$T_{34} = T_S - T_{01} - T_{12} - T_{23} \tag{4.21}$$

where T_S is the period of a switching cycle.

A condition for achieving zero-voltage switching in the ZVS quasi-resonant buck converter is [19]:

$$r \le M \tag{4.22}$$

4.3 Steady-State Characteristics

The steady-state characteristics can be obtained by solving the state equations of the four stages in a switching cycle. The dc voltage conversion ratio, V_0/V_i, as a function of the load resistance and the switching frequency, can be derived by equating the input energy per cycle E_i, and the output energy per cycle, E_0.

The expression for conversion ratio of a ZVS quasi-resonant buck converter can be derived by the method described above:

$$M = \frac{V_0}{V_{in}} = 1 - \frac{f_S}{2\pi f_R}\left[\alpha + \frac{r}{2M} + \frac{M}{r}\left(1 - \cos\alpha\right)\right] \tag{4.23}$$

where

$$\alpha = \pi + \arcsin\left(\frac{r}{M}\right) \text{ for half-wave mode} \tag{4.24}$$

$$\alpha = 2\pi - \arcsin\left(\frac{r}{M}\right) \text{ for full-wave mode.} \tag{4.25}$$

$$V_{DSpeak} = I_0 Z_N + V_{in} \tag{4.26}$$

In general, a constant off-time control is employed to regulate the output voltage for the load and the line variations. Higher switching frequency with constant off time means

shorter equivalent on time and, therefore the voltage-conversion ratio decreases as the switching frequency is increased.

4.4 Peak Voltages and Currents in ZVS QR Buck Converter

In order to find M as a function of f_S, it is necessary to use a numerical procedure. Rearrangement of Eq. (4.23) yields

$$\frac{f_S}{f_R} = \frac{2\pi(1-M)}{\left[\alpha + \frac{r}{2M} + \frac{M}{r}(1-\cos\alpha)\right]} \tag{4.27}$$

The switching frequency can be calculated from the above equation. The regulation characteristics for different values of the normalized load resistance are plotted in Figure 4.3. The characteristics are plotted for only lossless conditions. From Figure 4.3, it can be easily seen that the conversion ratio is load dependent. For example, for fixed switching frequency, conversion ratio M increases when normalized load resistance r increases. Therefore, to regulate the output voltage for variable load resistance, the switching frequency should be varied accordingly [19].

Peak voltage on the power switch and peak current in output diode occur during resonance. The solutions of four topological modes result in the following peak values of voltage and current

$$\frac{V_{DS-pk}}{V_0} = \frac{1}{M}\left(1 + \frac{M}{r}\right) \tag{4.28}$$

$$\frac{I_{SW-pk}}{I_0} = 1 \tag{4.29}$$

$$\frac{V_{D-pk}}{V_0} = \frac{1}{M} \tag{4.30}$$

$$\frac{I_{D-pk}}{I_0} = 2 \tag{4.31}$$

4.5 Small-Signal Analysis

In previous chapter, three-terminal PWM switch is used to derive the equivalent circuit model of the conventional PWM converters. By averaging the terminal voltages and currents, the small signal model was obtained.

The averaging technique [20, 21] is a very effective tool for studying the switched mode dc-dc converters. It provides a method to undertake both the static and dynamic analyses of a large number of converters in a systematic manner. The method was originally proposed to model PWM converters and it was extended later to converters incorporating resonant switches [22].

The same procedure can be applied to the quasi-resonant converters with enough accuracy. For frequencies below the modulation frequency (approximately half of the switching frequency), the added resonant components, capacitor and inductor, have no effect on the small signal model for quasi-resonant converters.

The equivalent circuit model of a switch is replaced by a three-terminal switch in any quasi-resonant converter topology.

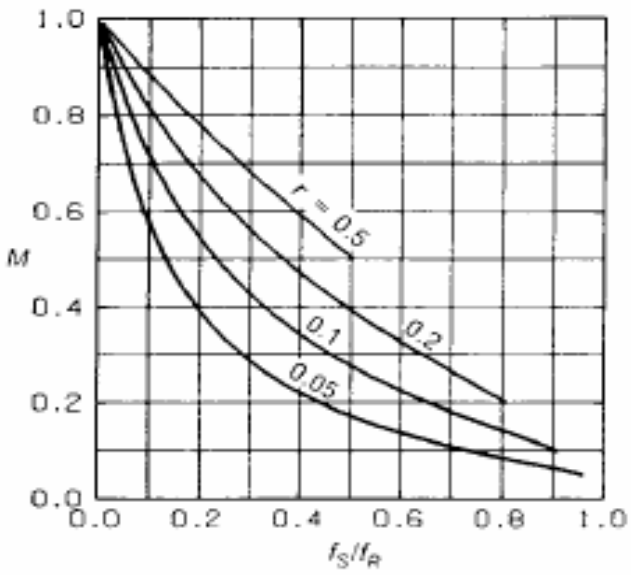


Figure 4.3 Normalized output voltage versus normalized switching frequency for different normalized load resistance in buck ZVS QRC.

4.6 ZVS Three-Terminal Switching Devices

Figure 4.4 shows the basic ZVS quasi-resonant converters and their three-terminal switch illustrations. The three-terminal device is shown in Figure 4.5. The terminal designations ***a***, ***p*** and ***c*** refer to active, passive and common, respectively. This symbolic representation of the ZVS resonant switch has two single pole switches.

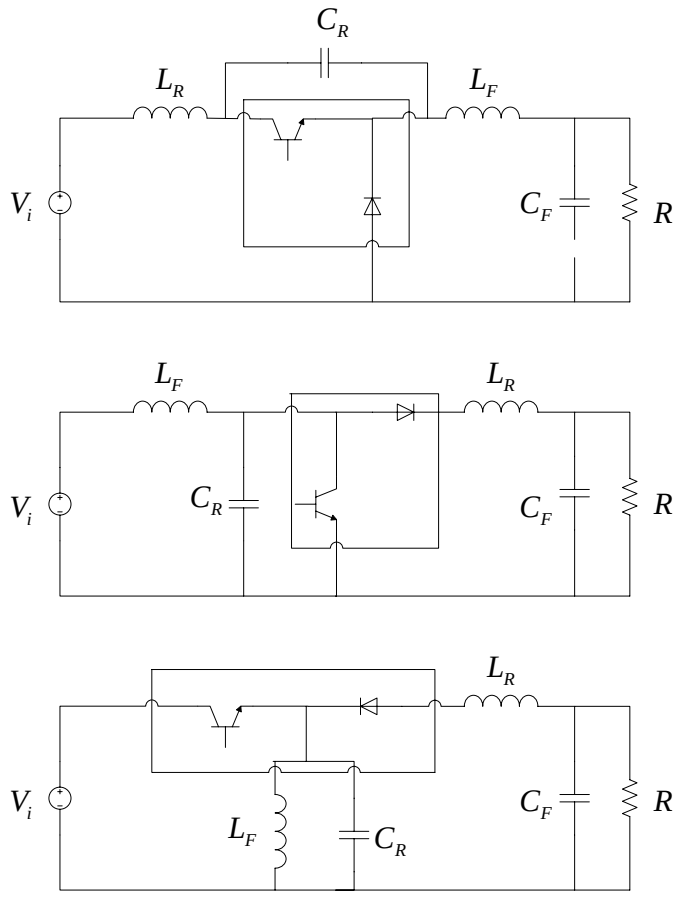


Figure 4.4 Basic zero-voltage switching quasi-resonant converters.

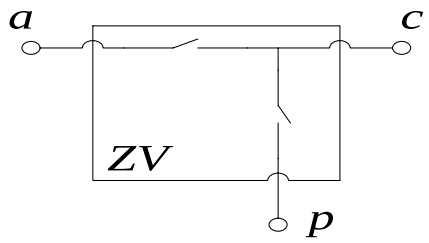


Figure 4.5 A three-terminal ZVS switch.

4.7 Equivalent Circuit Model of the ZVS Device

The three-terminal zero-voltage switching device is drawn again in Figure 4.6 with all the terminal voltages and currents. From average voltage and current equations, the circuit model of three-terminal device can be obtained. The equation of the ZVS resonant device is:

$$\frac{i_a}{i_c} = \frac{v_{cp}}{v_{ap}} = 1 - \frac{1}{2\pi}\frac{f_S}{f_R} f\left(\alpha_V, n\right) = \mu_V \tag{4.32}$$

where

$$\alpha_V = r_{ac} G_N \tag{4.33}$$

$$r_{ac} = \frac{v_{ap}}{i_c} \tag{4.34}$$

$$G_N = \frac{1}{Z_N} \tag{4.35}$$

Furthermore, f_S is the switching frequency and f_R is the resonant frequency as mentioned before. It is assumed that below half of the switching frequency, the resonant elements in the small signal model and dc model are negligible. The function $f(\alpha_v,n)$ is defined as *zero-voltage quasi-resonant function* and is given by:

$$f\left(\alpha_V, n\right) = \frac{\alpha_V}{2} + n\pi - \left(-1\right)^n \arcsin \alpha_V + \frac{1}{\alpha_V} - \left(-1\right)^n \sqrt{\frac{1}{\alpha_V^2} - 1} \tag{4.36}$$

where

$n = 1$ for half-wave mode (4.37)

$n = 2$ for full-wave mode (4.38)

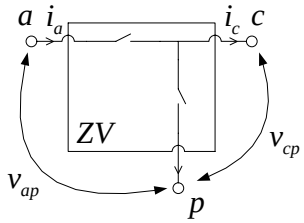


Figure 4.6 Terminal voltages and currents of ZVS device.

4.8 DC Model of ZVS Device

A steady-state or dc model of the ZVS device is shown in Figure 4.7, and all the quantities are replaced by their dc values.

$$\mu_V = 1 - \frac{1}{2\pi}\frac{F_S}{F_R}F\left(\alpha_V, n\right) = \frac{I_a}{I_c} = \frac{V_{cp}}{V_{ap}} \tag{4.39}$$

$$\alpha_V = R_{ac}G_N \tag{4.40}$$

$$R_{ac} = \frac{V_{ap}}{I_c} \tag{4.41}$$

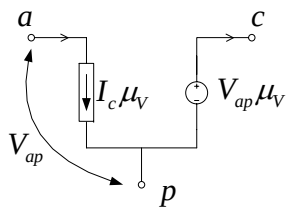


Figure 4.7 Dc equivalent circuit model of ZVS device.

4.9 Small Signal Model of ZVS Device

Eq. (4.39) and Eq. (4.40) are perturbed. These perturbations are in switching frequency and the average terminal voltages and currents form Eq. (4.39) is rewritten as:

$$v_{cp} = \left(1 - \frac{1}{2\pi}\frac{f_S}{f_R} f\left(\alpha_V, n\right)\right) v_{ap} \tag{4.42}$$

and the perturbations of variables are as follows from Eq. (4.43) to Eq.(4.48):

$$v_{cp} = \hat{v}_{cp} + V_{cp} \tag{4.43}$$

$$v_{ap} = \hat{v}_{ap} + V_{ap} \tag{4.44}$$

$$f_S = \hat{f}_S + F_S \tag{4.45}$$

$$i_c = \hat{i}_c + I_c \tag{4.46}$$

$$i_a = \hat{i}_a + I_a \tag{4.47}$$

$$f\left(\alpha_V, n\right) = \hat{f}\left(\alpha_V, n\right) + F\left(\alpha_V, n\right) \tag{4.48}$$

By considering that departures from the steady-state values are small compared to the steady-state values themselves, nonlinear terms such as the second (or higher) order terms due to the product of two or more ac perturbations can be neglected [23].

The corner frequency of LC filter is so lower than the switching frequency and resonant frequency in general that the low-frequency characteristics of the converter are dominated almost by these low-frequency LC elements [24].

After the assumptions and rearrangements are performed, the small-signal model of three-terminal ZVS device can be obtained.

$$\hat{i}_c = -\hat{v}_{cp} g_0 + \hat{v}_{ap} g_f + \hat{f}_c k_0 \tag{4.49}$$

$$\hat{i}_a = \hat{f}_c k_i + \hat{i}_c k_r + \hat{v}_{ap} g_i \tag{4.50}$$

where

$$\hat{f}_c = \frac{\hat{f}_S}{F_S} \tag{4.51}$$

Eq. (4.49) and Eq. (4.50) correspond to the small-signal equivalent circuit model of the ZVS device shown in Figure 4.8.

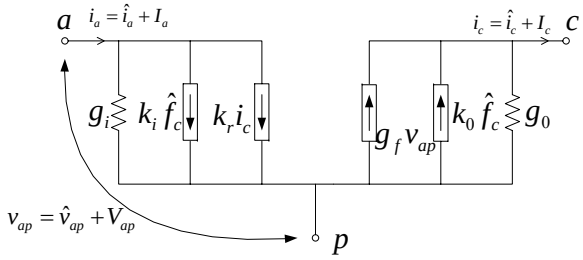


Figure 4.8 Small-signal equivalent circuit of ZVS device.

For the full-wave operation, α is much smaller than 1 and therefore $\alpha^2 << 1$, Eq. (4.49) and Eq. (4.50) can be approximated as follows when n = 2;

$$f\left(\alpha_V, 2\right) \approx 2\pi \tag{4.52}$$

An approximate model of ZVS device operating in full-wave mode is easily obtained. This model is shown in Figure 4.9.

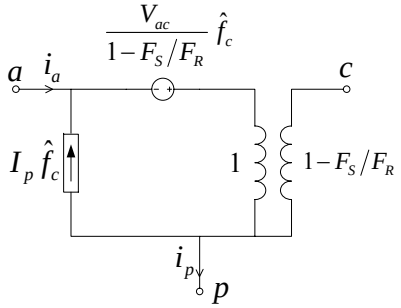


Figure 4.9 Approximate small-signal model of full-wave ZVS device.

4.10 Small-Signal Model of Buck ZVS QRC

The circuit diagram of the buck converter is shown in Figure 4.10.

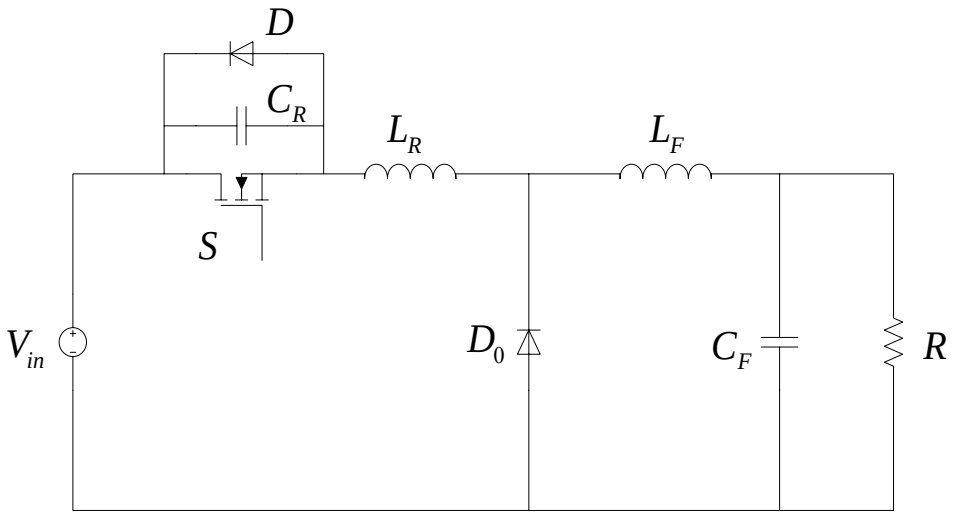


Figure 4.10 ZVS quasi-resonant buck converter.

For modulation frequencies below half the switching frequency, the small-signal model is approximated by eliminating the resonant components. These components do not affect the small-signal model of the QR buck converter, because magnitudes of the output filter components are much higher than the magnitudes of the resonant network.
The three-terminal switch is simply replaced by its dc equivalent model as derived above, and all passive elements are either shorted or opened. The resultant equivalent circuit with dc switch model is shown in Figure 4.11. Under dc conditions all small-signal sources vanishes. Eqs.(4.53) to Eq.(4.55) show the dc characteristics.

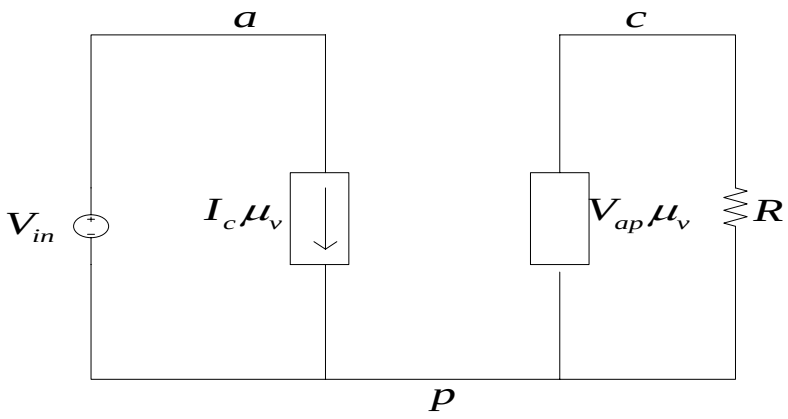


Figure 4.11 Dc conditions of equivalent buck converter.

$$V_{cp} = V_0 = V_{ap}\mu_v \tag{4.53}$$

$$V_{ap} = V_{in} \tag{4.54}$$

$$V_{in} = \frac{V_0}{\mu_v} \tag{4.55}$$

Once the operation point of the buck converter is determined from the dc model, the small-signal analysis can be performed simply by using the small-signal model of the ZVS device. The three-terminal switch is replaced by its small-signal model to obtain control-to-output and line-to-output transfer functions. The small-signal equivalent circuit for obtaining the control-to-output transfer function is shown in Figure 4.12. The input dc voltage is shortened and the necessary perturbations are performed.

Obtained from dc analysis, the operation point values are:

$$V_{ac} = V_{ap} - V_{cp} = \frac{V_0}{\mu_v} - V_0 = \frac{V_0\left(1-\mu_v\right)}{\mu_v} \tag{4.56}$$

$$\mu_v = 1 - \frac{F_S}{F_R} \tag{4.57}$$

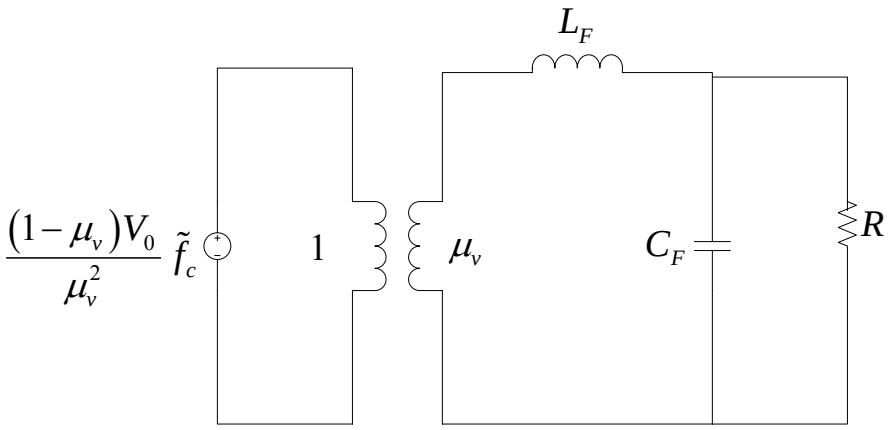


Figure 4.12 Small-signal equivalent circuit for control-to-output transfer function.

Node analysis can be performed as follows:

$$\frac{\tilde{v}_0 - \frac{(1-\mu_v)V_0}{\mu_v}\tilde{f}_c}{sL_F} + \tilde{v}_0 sC_F + \frac{\tilde{v}_0}{R} = 0 \tag{4.58}$$

$$\tilde{v}_0\left[s^2 L_F C_F R + sL_F + R\right] = \frac{\mu_v' R V_0}{\mu_v}\tilde{f}_c \tag{4.59}$$

The Eq.(4.59) is rearranged and the control-to-output transfer function is obtained:

$$\frac{\tilde{v}_0}{\tilde{f}_c} = \frac{\frac{\mu_v' V_0}{\mu_v}}{s^2 L_F C_F + s\frac{L_F}{R} + 1} \tag{4.60}$$

As a conclusion, the order of the small-signal model of QRC is nearly the same as that of the parent PWM converter. The resonant elements do not increase the order of the small-signal model since they do not contribute state variables to the system of the converter [25].

CHAPTER 5

DESIGN PROCEDURES AND SIMULATION & EXPERIMENTAL RESULTS

This chapter presents the design procedure of ZVS QR buck converter. The computer simulation and experimental results are also shown. In the experimental study, the steady-state and dynamic performance of the ZVS quasi-resonant buck converter are investigated under open-loop and closed-loop operations. The simple block diagram of the experimental set-up is shown in Figure 5.1.

The open-loop PWM buck converter and open-loop ZVS QR buck converter are driven at predefined duty-cycle values at various frequencies. The design is performed according to required specifications, such as the input voltage range, output voltage, switching frequency and maximum output power. The analysis presented in previous chapters is used.

Open loop control signals are provided by PIC 16F877 microcontroller from Microchip. The microcontroller is operated with an external clock of 20 MHz. Each operation cycle takes 200 ns by using this external clock. Open loop control signals are adjusted such that the microcontroller gives fixed off-time and variable on-time at frequencies from 50 kHz to 100 kHz in 11 discrete steps. This is because operation conditions are kept the same for both PWM buck and ZVS QRC buck converters. Design procedure is only applied to the ZVS QRC buck converter. Closed loop control is performed by a high performance resonant mode controller MC34067 from ON Semiconductor. The application areas of MC34067 are zero-voltage switching off-line switch-mode power

supplies and zero-voltage switching dc-dc converters.

The structure of this chapter is as follows. In section 5.1, the design procedure of the ZVS QR buck converter is presented. Design procedures cover both open loop and closed loop operations. In section 5.2, the design of the zero-voltage switching quasi resonant buck converter is presented. In section 5.3 and section 5.4, the important properties of the controller IC MC34067 and small-signal considerations are presented. In the last section, the simulation and experimental results are presented with comparison.

5.1 Design Procedure of ZVS QR Buck Converter

The guidelines presented in this section are based on the stress analysis in previous chapter. The objective is to make the proper choice of resonant and filter elements so that the current and voltage stresses are as low as possible for the specified input voltage and output load ranges. The desired specifications are assumed as:

$V_{in\text{-}min} - V_{in\text{-}max}$	-	Input voltage range
$I_{0\text{-}min} - I_{0\text{-}max}$	-	Output load range
V_0	-	Output voltage
$f_{S\text{-}max}$	-	Maximum switching frequency
ξ_f	-	Maximum percent ripple in filter inductor

The operation and characteristics of the converter depend mainly on the design of the resonant circuit L_R and C_R. The parameters that are defined below determine the converter characteristics:

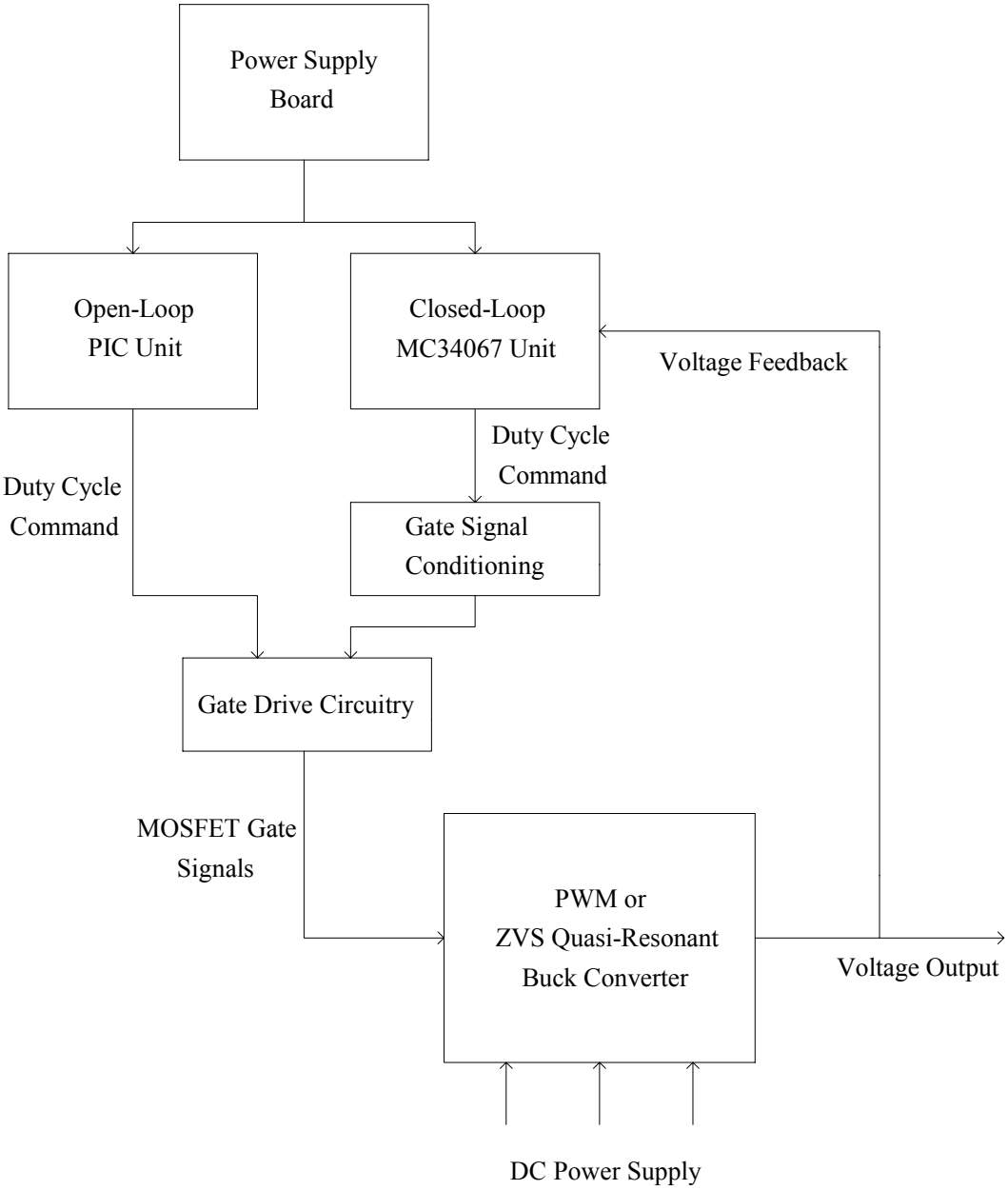


Figure 5.1 The simple block diagram of the experimental set-up.

Characteristic Impedance Z_N:

$$Z_N = \sqrt{\frac{L_R}{C_R}} \tag{5.1}$$

Resonant Frequency f_R:

$$f_R = \frac{1}{2\pi\sqrt{L_R C_R}} \tag{5.2}$$

Normalized Load Resistance r:

$$r = \frac{R}{Z_N} \tag{5.3}$$

where R is the load resistance of the converter.

The minimum and the maximum values of voltage conversion ratio are given by the following formulas:

$$M_{\min} = \frac{V_0}{V_{i\max}} \tag{5.4}$$

and

$$M_{\max} = \frac{V_0}{V_{i\min}} \tag{5.5}$$

respectively. The switching frequency can be directly calculated as a function of M and r.

Following equations are obtained by input voltage and output current specifications for ZVS operation.

$$R_{\max} = \frac{V_0}{I_{0-\min}} \tag{5.6}$$

$$\xi_v = \frac{M_{\min}}{r_{\max}} \geq 1 \tag{5.7}$$

From the above equations, the worst condition that still provides zero-voltage turn-on is:

$$Z_N = \xi_v \frac{R_{\max}}{M_{min}} \tag{5.8}$$

When load resistance increases the switching frequency increases. For any conversion ratio M, there is a maximum load resistance that provides zero-voltage turn-on. It is also known that when the load resistance decreases the peak voltage across the power switch increases because of the output current. Therefore, a trade-off exists between the load range and maximum peak voltage of the power switch. The key design parameter is the characteristic impedance Z_N. The characteristic impedance should be minimized to reduce voltage across the power switch and the characteristic impedance should be maximized to increase the load range at zero-voltage switching.

The characteristic impedance formula in Eq. (5.8) will result in the lowest possible voltage stress on the power switch for the desired output load range.

The maximum switching frequency occurs at light load (r_{max}) and high input voltage ($V_{in\text{-}max}$). The DC conversion ratio is also given by using quasi-resonant function

$$F\left(\frac{r}{M},n\right)=n\pi-(-1)^n\arcsin\left(\frac{r}{M}\right)+\frac{r}{2M}+\frac{M}{r}-(-1)^n\sqrt{\left(\frac{M}{r}\right)^2-1} \tag{5.9}$$

n = 1 for half-wave mode

n = 2 for full-wave mode

and the resonant frequency is

$$f_R=\frac{3(1+\pi)f_{s\max}}{4\pi(1-M_{\min})} \tag{5.10}$$

The resonant components, L_R and C_R, are easily found as follows

$$L_R=\frac{\xi_v R_{\max}(1-M_{\min})}{2\pi f_{S\max}M_{\min}} \tag{5.11}$$

$$C_R=\frac{M_{\min}(1-M_{\min})}{2\pi f_{S\max}\xi_v R_{\max}} \tag{5.12}$$

The relative size of filter inductor L_f is also obtained by using the volt-second balance on L_f [26]. To satisfy the ripple specifications over the whole range of operation, the following approximate equation can be used with denoting the load variation by $\Delta R = R_{max}/R_{min}$

$$\frac{L_f}{L_R}\approx\frac{M_{min}}{2\Delta R\xi_v\xi_f}\left[F\left(\frac{r_{\min}}{M_{\max}},n\right)-\frac{r_{\min}}{2M_{\max}}\right] \tag{5.13}$$

where ξ_f is the maximum percentage ripple

$$\xi_f = \frac{\Delta I_L / 2}{I_{L\max}} \tag{5.14}$$

For properly designed converters (with minimal values of ζ_v), it is clear that quasi-resonant converters always have stresses greater than or equal to those of PWM converters [26].

5.2 MOSFET Gate Drive Circuitry

The semiconductor switch in buck converter is in high-side (MOSFET source connected to high voltage rail). Gate voltage must be 10-15 V higher than the source voltage of any power device. The gate voltage of MOSFET must be controllable from the logic or controller IC drive output, which is normally referenced to ground. Thus, the control signals have to be level-shifted to the source of the high side power device. The power absorption of the gate circuitry should not affect the overall efficiency.

Several techniques are used to drive the high side power device. Table 5.1 summarizes high side power device drive techniques with advantages or disadvantages [27].

The transformer coupled gate drive technique is used to drive power device in buck converter, because efficient gate drive with minimum delay can be performed with this technique. The integrated high side drivers are convenient. They have significant turn-on and turn-off delays. The properly designed transformer coupled solution has negligible delays and it can operate across higher potential differences. Figure 5.2 shows the basic transformer coupled gate drive circuit.

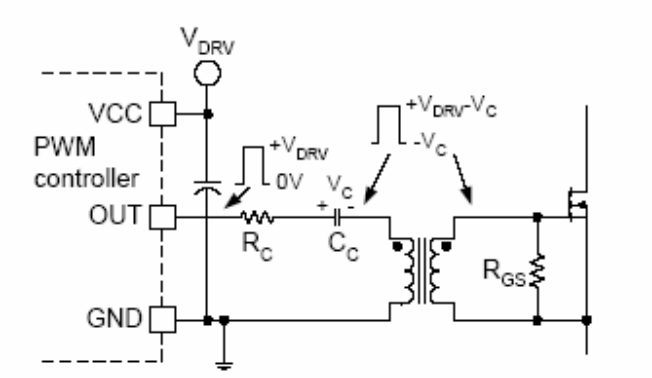
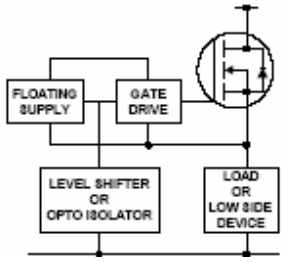
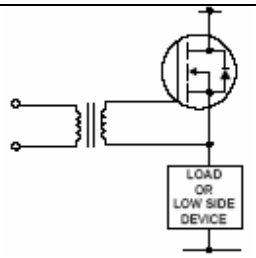
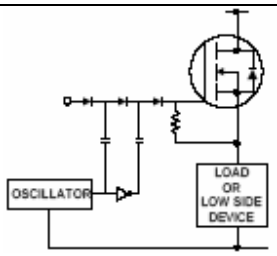
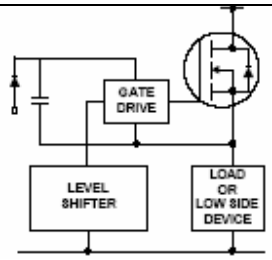
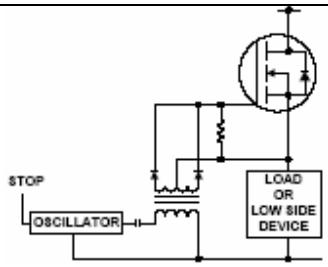


Figure 5.2 The basic transformer coupled gate drive circuit.

The coupling capacitors must be placed in series with the primary winding of the gate drive transformer to provide the reset voltage for the magnetizing inductance. Without the coupling capacitor, there would be a duty cycle dependent dc voltage across the primary winding and the transformer would saturate.

The control signals for open loop buck converter is provided by microcontroller, as mentioned before. The logic control signal must be boosted to a level of 10-15 V before the gate drive transformer. This is achieved by a high and low side driver integrated circuit IR2110 from International Rectifier.

Table 5.1 High side power device drive techniques

METHOD	BASIC CIRCUIT	KEY FEATURES
FLOATING GATE DRIVE SUPPLY		• Level shifting a ground referenced signal can be tricky. • Opto isolators are relatively expensive.
PULSE TRANSFORMER		• Simple and cost effective. • Significant parasitics create less than ideal operation with fast switching waveforms.
CHARGE PUMP		• Turn on times can be too long. • Level shifter has to be tackled.
BOOTSTRAP		• Simple and inexpensive. • Requires level shifter.
CARRIER DRIVE		• Gives full gate control. • Limited in switching performance. • Improved with added complexity.

5.3 Design of ZVS QR Buck Converter

Designing a quasi-resonant converter requires the selection of resonant components, output filter components and semiconductor devices. Typically, design specifications for a dc-dc converter include those parameters shown in Table 5.2. A basic ZVS QR buck converter is shown in Figure 5.3.

- Output voltage V_0
- Input voltage range V_{imin} to V_{imax}
- Load resistance range R_{min} to R_{max}
- Maximum switching frequency f_{Smax}
- Maximum percentage ripple ξ_f

Table 5.2 Design specifications of ZVS QR buck converter

	Max.	**Min.**
V_0	15 V	-
V_i	20 V	30 V
R	5 Ω	15 Ω
$f_{S\max}$	100 kHz	-
ξ_f	1.5 A	-

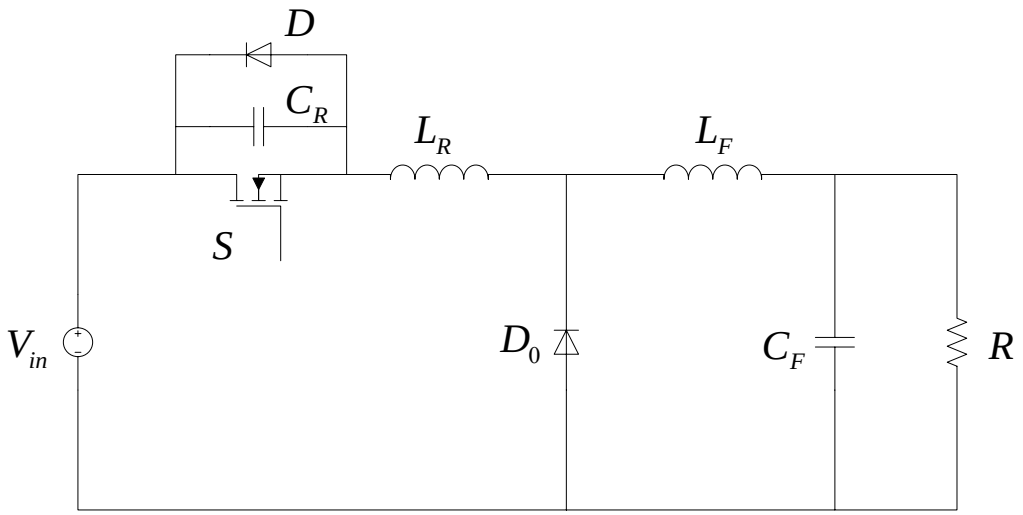


Figure 5.3 A basic ZVS QR buck converter.

$$M_{\min} = \frac{V_0}{V_{i\max}} = \frac{15}{30} = 0.5 \tag{5.15}$$

$$M_{\max} = \frac{V_0}{V_{i\min}} = \frac{15}{20} = 0.75 \tag{5.16}$$

To achieve zero voltage turn-on, the amplitude of ac component of switch voltage should be greater or equal to the input voltage. The normalized form of this condition is

$$r \le M \tag{5.17}$$

The peak value of resonant capacitor voltage is

$$V_{DSpeak} = I_o Z_N + V_{in} \tag{5.18}$$

In lowest possible voltage stress on the power switch for the desired load range by guaranteeing zero-voltage switching, the characteristic impedance is

$$Z_N = \xi_v \frac{R_{\max}}{M_{\min}} = 1.1\frac{15}{0.5} = 33\Omega \tag{5.19}$$

The voltage and current stresses of the ZVS QR buck converter with given specifications are given as follows:

- Peak voltage stress on the power switch 120 V
- Peak current stress through the power switch 3A
- Peak voltage stress in output diode 30 V
- Peak current stress in output diode 6A

From Eq.(5.9) to Eq.(5.14), the design values of ZVS QRC buck converter are easily calculated and given in Table 5.3.

Table 5.3 Design parameters of ZVS QR buck converter

Characteristic Impedance, Z_N	33 Ω
Resonant Frequency, f_R	200 kHz
Resonant Inductor, L_R	26.3 μH
Resonant Capacitor, C_R	22 nF
Filter Inductor, L_f	160 μH
Filter Capacitor, C_f	220 μF
Minimum Frequency, $f_{S\min}$	20 kHz

As mentioned before, the switching cycle of the quasi resonant buck converter can be divided into four stages. The following formulas are introduced to calculate the stage durations of quasi resonant buck converter.

$$T_{0-1} = \frac{C_R V_{in}}{I_o} = \frac{1}{w}\frac{r}{M} = \frac{1}{2\pi 200kHz}\frac{0.4}{0.4} \approx 0.8us \tag{5.20}$$

$$T_{1-2} = \frac{\alpha}{w} \approx 3.7us \quad \text{where } \alpha = \pi + \arcsin(\frac{V_{in}}{Z_N I_o}) \tag{5.21}$$

$$T_{2-3} = \frac{1}{w}\frac{M}{r}(1-\cos\alpha) = 1.65us \tag{5.22}$$

The last stage duration is control parameter. The regulation of output voltage can be achieved by this duration.

5.4 The Controller IC MC34067

The closed loop operation is achieved using high performance zero-voltage switching resonant mode controller MC34067. The IC operates with constant off-time variable on-time. This integrated circuit features a variable frequency oscillator, a precise retriggerable one-shot timer, high gain wide bandwidth error amplifier, steering flip-flop and dual high current totem pole outputs. Also protective features consist of a high speed fault comparator, programmable soft-start circuitry and input under voltage lockout with selectable thresholds. Figure 5.4 shows the simplified block diagram of the resonant mode controller IC.

The primary purpose of this control chip is to provide a fixed-off time to the gates of external MOSFETs at a repetition rate regulated by a feedback control loop. Additional

features of the IC ensure that system startup and fault conditions are administered in a safe, controlled manner [28].

The output pulse width and repetition rate are regulated through the interaction of the variable frequency oscillator, one-shot timer and error amplifier. The error amplifier can control the oscillator frequency over a 1000:1 frequency range, and both the minimum and maximum frequencies are easily programmed by the proper selection of external components [28].

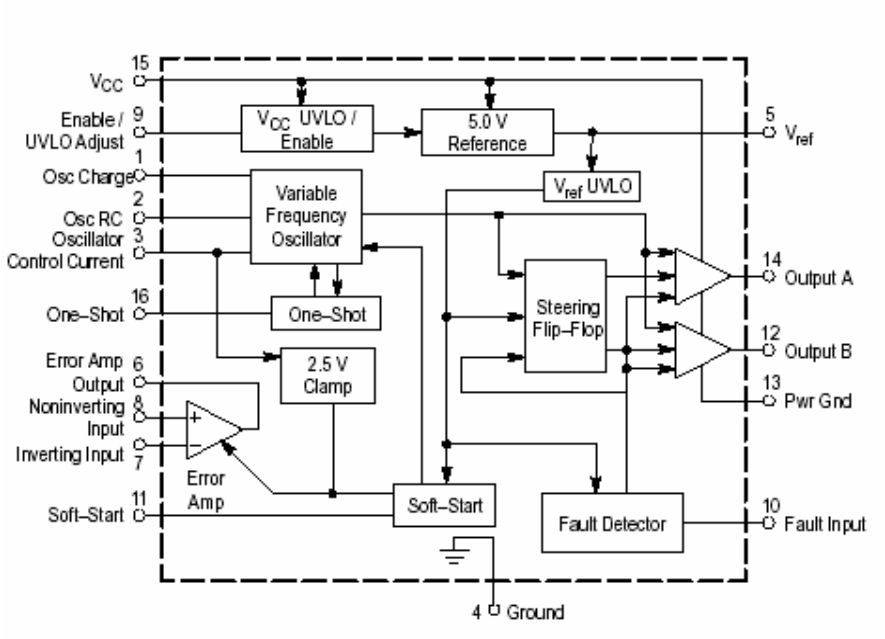


Figure 5.4 The simplified block diagram of MC34067.

The frequency of the oscillator is modulated by varying the current flowing out of the Oscillator Control Current (I_{OSC}) pin. This pin is the output of a voltage regulator. The minimum oscillator frequency will result when the I_{OSC} current is zero. The minimum frequency is programmed by R_{OSC} using the following equation:

$$R_{OSC} = \frac{\frac{1}{f_{\min}} - t_{PD}}{0.348 x C_{OSC}} \tag{5.23}$$

The maximum oscillator frequency is set by the current through resistor R_{VFO}. The current required to discharge C_{OSC} at the maximum oscillator frequency can be calculated below equations:

$$I(\max) = 1.5 C_{OSC} f_{S\max} \tag{5.24}$$

$$I_{R_{OSC}} = \frac{1.5}{R_{OSC}} \varepsilon^{\left(-\frac{1}{f_{S\min} R_{OSC} C_{OSC}}\right)} \tag{5.25}$$

$$R_{VFO} = \frac{2.5 - V_{EAsat}}{I(\max) - I_{R_{OSC}}} \tag{5.26}$$

The one-shot is designed to disable both outputs simultaneously providing a deadtime t_{OS} before either output is enabled. R_T and C_T can be chosen by solving the following equation:

$$R_T = \frac{t_{OS}}{0.348 C_T} \tag{5.27}$$

The control IC is specially designed for zero-voltage switching quasi-resonant converters applications and is optimized for double-ended push-pull or bridge type converters operating in continuous conduction mode. Therefore, for one-switch dc-dc converters, the outputs of the IC must be rearranged. Two fast diodes and two npn transistors are used to obtain one-output control signal for one-switch zero-voltage switching dc-dc converters. The two outputs of controller IC are logically summing up

through the fast diodes and npn transistors turn the output into constant-off time gate drive signals. The operation frequency is changed between the maximum and minimum frequencies defined by the external components to regulate the output voltage. This additional circuitry is shown in Figure 5.5.

5.5 Small Signal Considerations of ZVS QR Buck Converter

The small signal model of the ZVS buck converter is derived in previous chapters. For frequencies of modulation below half the switching frequency, the desired small signal model is similar to that of PWM counterparts. The small-signal model of the ZVS QRC buck converter is

$$\frac{V_0}{V_i} = \frac{sCR_C + 1}{s^2\left[L_f C_f\left(1+\frac{R}{R_C}\right)\right] + s\left[CR_C + \frac{L_f}{R}\right] + 1} \tag{5.28}$$

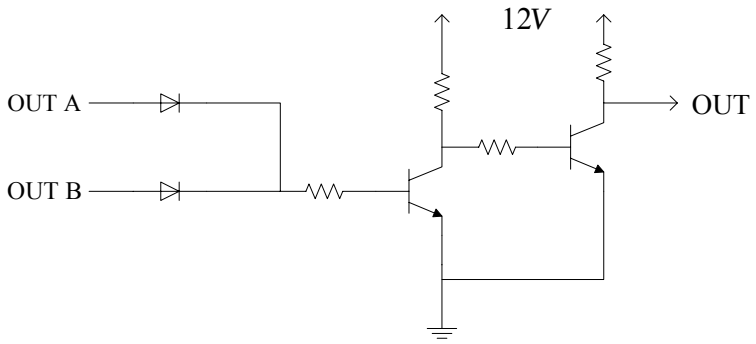


Figure 5.5 Additional circuit that summing up two outputs of the IC.

The Bode plot of the ZVS QR buck converter with calculated circuit parameters is shown in Figure 5.6.

A compensation network can be designed in a similar manner to that of a PWM converter to meet closed-performance specifications. A two-pole, two-zero compensation network is used for this circuit to provide high low-frequency gain and good phase margin at the crossover frequency [8]. Figure 5.7 shows the two-pole, two-zero compensation network. To design the compensator following steps should be taken

- A pole should be used in the compensation network to provide the desired high dc gain at low frequencies to achieve zero steady state error at the output of the converter.

- Another pole should be introduced to cancel the equivalent series resistor (ESR) of the filter capacitor at the output.

- A zero should be introduced before the cut-off frequency of the filter elements.

The compensator obtained from these considerations is as follows and the Bode diagram of overall system is shown in Figure 5.8.

$$G(s) = \frac{2.26x10^{-8}s^2 + 3.058x10^{-4}s + 1}{21.824x10^{-10}s^2 + 9.92x10^{-4}s} \tag{5.29}$$

The external components of the resonant mode controller IC MC34067 are summarized in Table 5.4. The parameters include both external components that control the frequency and off-time of the output signal and compensation network parameters. These parameters are calculated for the converter to regulate the output in predefined specifications.

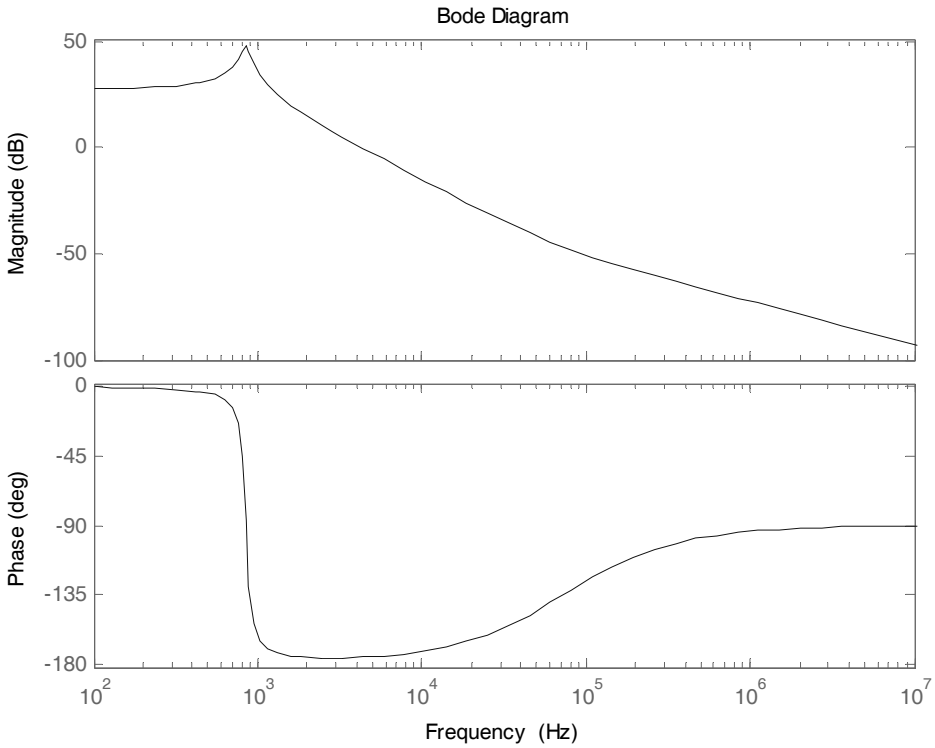


Figure 5.6 Bode diagram of the ZVS QR buck converter.

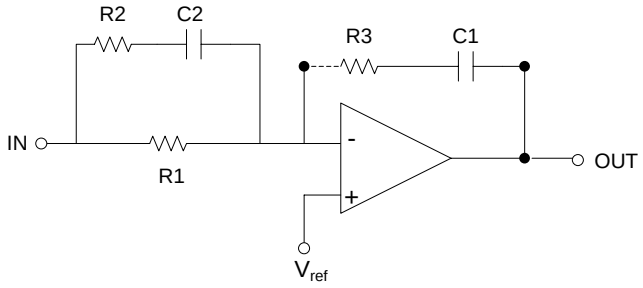


Figure 5.7 A two-pole, two-zero compensation network.

Table 5.4 The Resonant controller IC external components

$\mathbf{R_{OSC}}$	15 KΩ	$\mathbf{R_1}$	80 KΩ
$\mathbf{C_{OSC}}$	10 nF	$\mathbf{R_2}$	1 KΩ
$\mathbf{R_T}$	4.7 KΩ	$\mathbf{R_3}$	10 KΩ
$\mathbf{C_T}$	4.7 nF	$\mathbf{C_1}$	10 nF
$\mathbf{R_{VFO}}$	1.6 KΩ	$\mathbf{C_2}$	2.2 nF
$\mathbf{C_{SOFT\text{-}START}}$	10 nF		

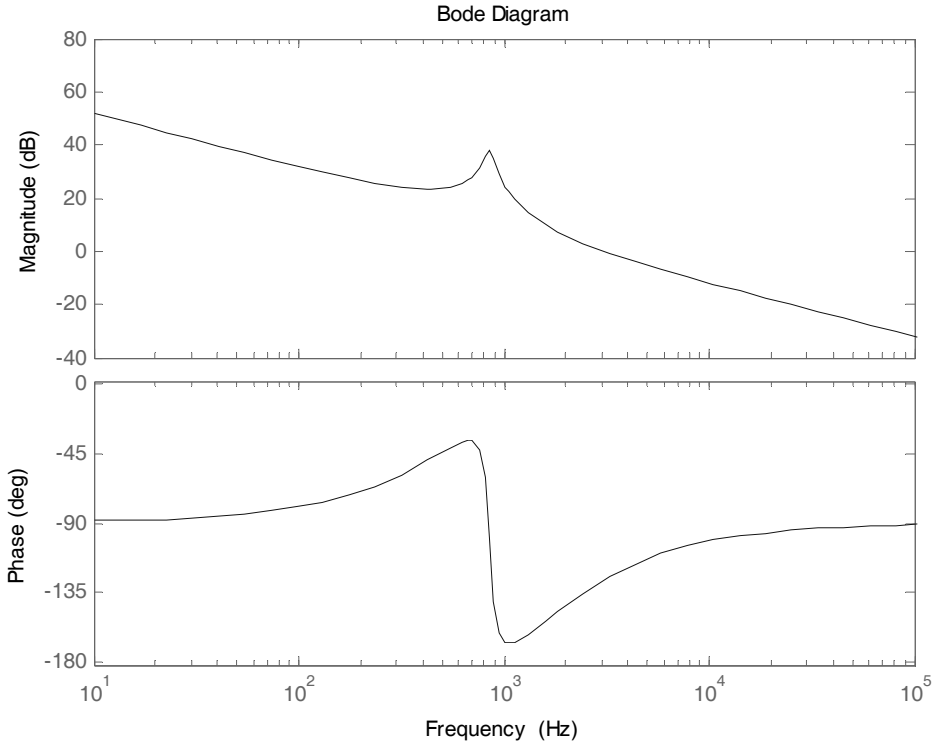


Figure 5.8 Bode diagram of the overall system.

5.6 Overall Hardware Description

The circuit parameters of PWM buck and ZVS QR buck converters are summarized in Table 5.5. The overall hardware roughly consists of two parts: open-loop stage and closed-loop stage. The transitions between open-loop and closed-loop stages are realized by two external on-off switches.

When the external on-off switches are on open-loop position, two possibilities arise. The first one is the open-loop PWM buck converter. This configuration is obtained by opening the connectors connected to the resonant capacitor and the diode across the power switch and by shorting the connector connected to the resonant inductor. The gate signals are obtained by a PIC 16F877 microcontroller. The gate signals have fixed-off time about 4.5 μs and variable on-time by adjusting the potentiometer. These logic gate signals are converted to MOSFET gate signals by a MOSFET gate driver IC IR2110 from International Rectifier. These signals are applied to the gate drive transformer to drive the high-side power switch in buck converter.

The second configuration is the open-loop ZVS QR buck converter. This is obtained by shorting the connectors connected to the resonant connector and the diode across the power switch and by inserting the resonant inductor in series with the power switch. The procedure of driving the MOSFET is the same as in PWM buck converter.

When the external switches are on closed-loop position, the system operates as single loop controlled quasi-resonant converter with Variable Frequency Oscillator (VFO). The resonant mode controller IC MC34067 provides the fixed-off time gate signals at a repetition rate regulated by a feedback controller loop. These two signals are summing up through the additional circuitry to obtain gate signal for one-switch zero-voltage switching circuit topologies as mentioned before. The output of the additional circuitry is connected to high-side MOSFET driver IC IR2125.

Table 5.5 Overall converter parameters

Output voltage, V_0	15 V
Input voltage range	20 V – 30 V
Load range	5 Ω – 15 Ω
Maximum frequency	100 kHz
Resonant frequency	200 kHz

The current measurements are performed with the current transducers LAH 25-NP. The nominal current of the current transducers are set to 8 A in order to achieve minimum measurement error. The current outputs are connected through the measurement resistors to turn the current signals into measurable voltage waveforms.

5.7 The Simulation and Experimental Results

This chapter presents the simulation and experimental results of PWM buck and ZVS QR buck converters. The simulations are performed in Ansoft's SIMPLORER. In order to confirm converter characteristics with calculated design parameters, simulations are an important part of the analysis. The open-loop and closed-loop simulations are performed with active and passive semiconductor switches close to real-time behaviors. The circuit parameters' selection is based on the calculated design parameters. The experimental verifications are performed with these parameters and semiconductor switches are selected well-suited for this topology.

5.7.1 Open-Loop PWM Buck Converter

The circuit schematic for the open-loop PWM buck is shown in Figure 5.9. The quasi-resonant converter is obtained by inserting some additional components such as a diode,

a capacitor and an inductor into this conventional circuit. The drive signals are the same for these converters. The circuit input parameters are summarized in Table 5.6.

Table 5.6 The design inputs for the system simulation

Input voltage	20 V – 30 V
Output voltage (for closed-loop)	15 V
Load range	5 Ω – 15 Ω
Frequency range (for open-loop)	50 kHz – 100 kHz
Resonant components	25.6 uH – 22 nF
Filter components	160 uH – 220 uF
Parasitic inductance (for PWM buck)	200 nH

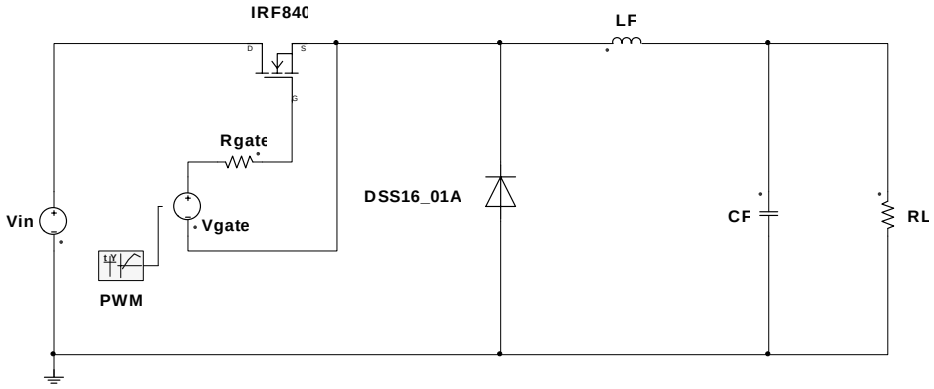


Figure 5.9 Open-loop PWM buck converter.

The selected semiconductor switches (active and passive) are summarized in Table 5.7 with critical specifications.

Table 5.7 Specifications of the semiconductor switches

IRF 840 Power MOSFET	
Maximum Drain-Source voltage	500 V
Maximum continuous drain current	8A
On-state resistor	0.75Ω
Output capacitance	200 pF
Input capacitance	1300 pF
DSS16-01A Power Schottky Rectifier	
Maximum reverse voltage	100 V
Maximum average forward current	16A
Forward voltage drop	0.64 V
Junction capacitance	250 pF

The conventional PWM converters especially operated in high frequencies (switching frequency > 50 kHz) are faced with some problems such as switching losses and undesirable oscillations caused by parasitic reactances of the power stage. The parasitic capacitances are associated with the semiconductor devices. The parasitic inductances are package and lead inductances of semiconductor devices and stray inductances of the interconnections. The parasitic reactances are considered in simulation examples. The parasitic capacitances are included in device characteristics and the parasitic inductances are characterized as an inductance of 200 nH in series with the active switch in simulation.

The simulation result of the MOSFET characteristics is shown in Figure 5.10. The green waveform illustrates the Drain-Source voltage of the MOSFET at 50 kHz switching frequency. The blue one illustrates the current through the MOSFET. The transition between the on and the off states produces switching losses because the switch is subjected to simultaneously high voltage and current at transition. The average value of the MOSFET Drain-source voltage is about 21 V. The peak value of the current through the MOSFET is approximately 2 A which is very close to the experimental result of the MOSFET characteristics shown in Figure 5.11.

The focused turn-off characteristic of the MOSFET is shown in Figure 5.12. The switching losses occur at turn-off transition because of the simultaneously high voltage and current.

The turn-on characteristics of the MOSFET again occur with switching losses because of the finite rise-time of the drain current and the finite fall time of the drain voltage. This turn-on loss is directly related to the gate-drive circuitry. Higher the current capability of the gate drive, lower the turn-on loss of the MOSFET. Furthermore, the presence of the parasitic inductance can reduce the overlap of the drain current and the drain voltage. The experimental result of the turn-on MOSFET characteristic is shown in Figure 5.13 at 50 kHz.

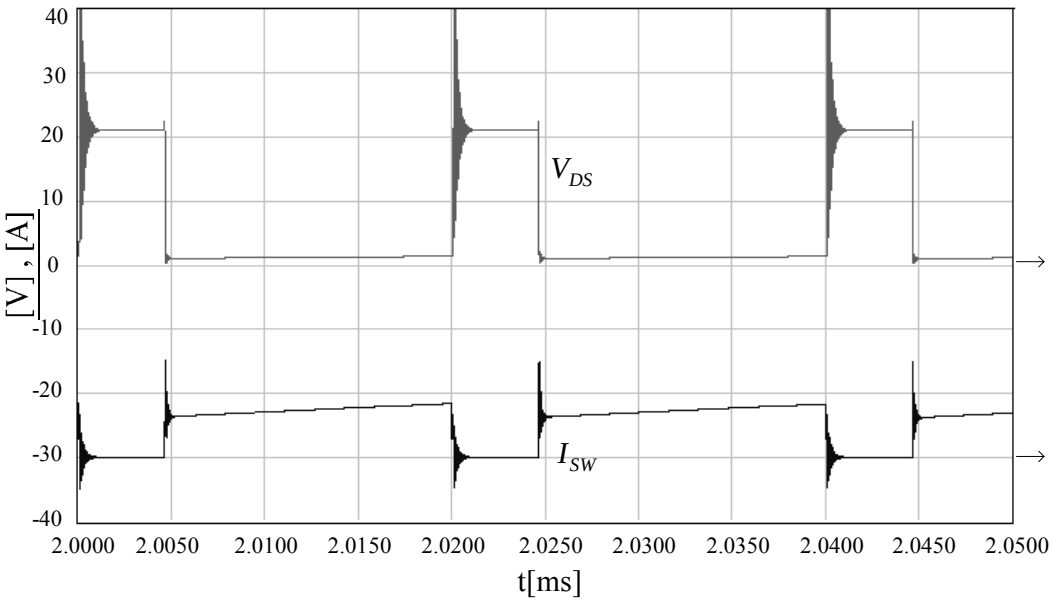


Figure 5.10 Simulation results of the MOSFET characteristics at 50 kHz (scales: 10 V/div, 2 A/div, 5 μs/div and current probe x5).

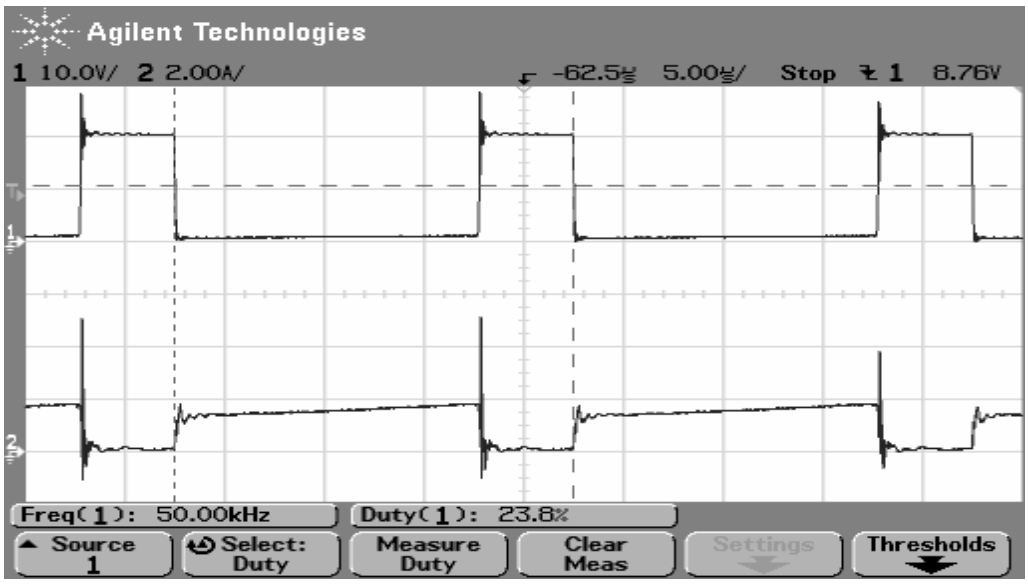


Figure 5.11 Experimental results of the MOSFET characteristics at 50 kHz (scales: 10 V/div, 2 A/div, 5 μs/div).

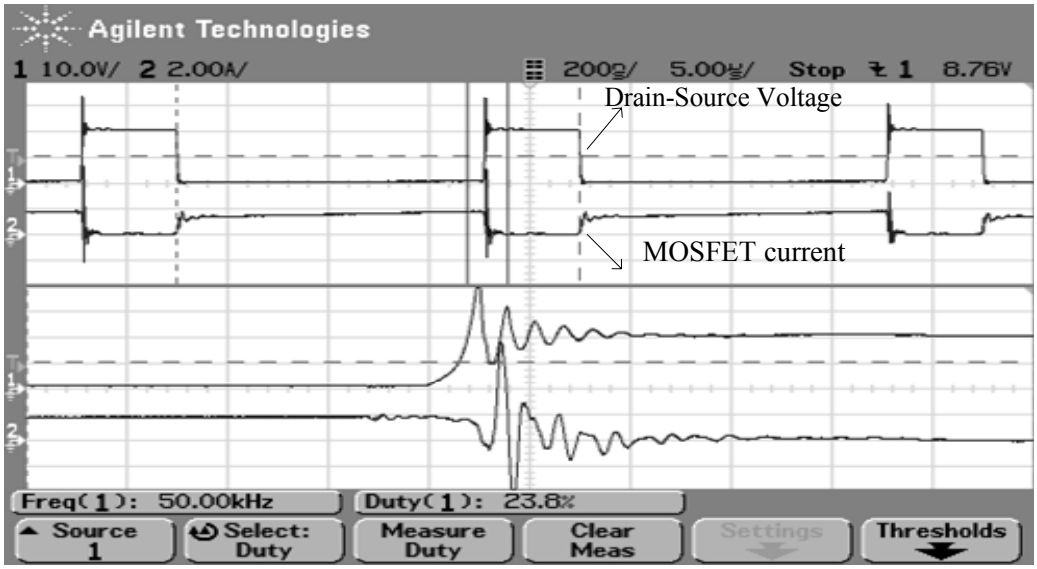


Figure 5.12 Experimental results of the MOSFET turn-off characteristics at 50 kHz (scales: 10 V/div, 2 A/div, 5 µs/div).

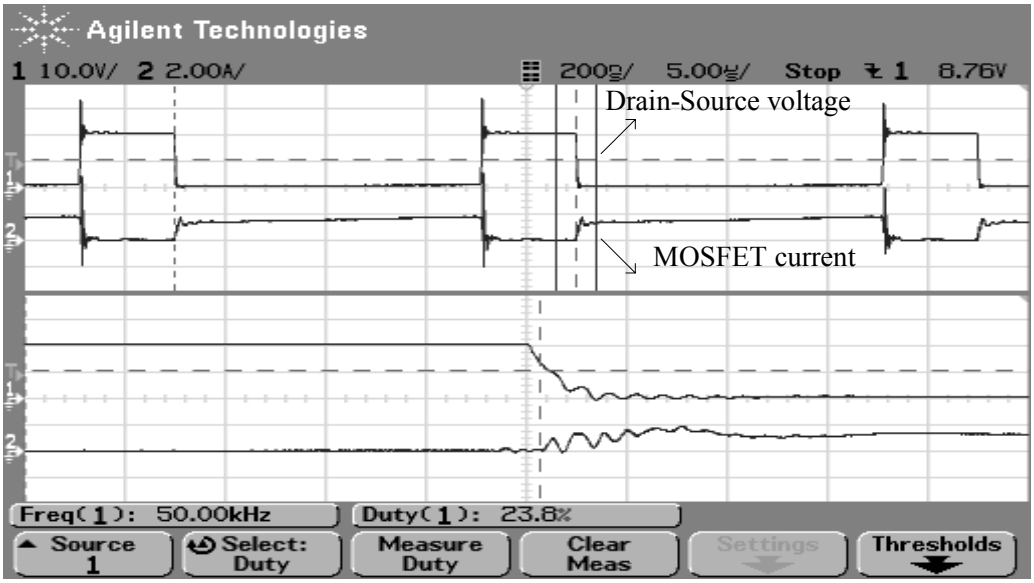


Figure 5.13 Experimental results of the MOSFET turn-on characteristics at 50 kHz (scales: 10 V/div, 2 A/div, 5 µs/div).

The simulation result of the oscillatory Drain-Source voltage of the MOSFET in PWM buck converter is shown in Figure 5.14. Because of the parasitic inductance in series with the MOSFET, during conduction of the MOSFET, load current is flowing through the parasitic inductance and magnetic field energy is stored. At turn-off, this energy induces a voltage spike across the MOSFET and the oscillations occur between the parasitic inductance and MOSFET output capacitance. The experimental result of the MOSFET Drain-Source voltage is shown in Figure 5.15.

The oscillation frequency is determined by the values of the parasitic inductance and the MOSFET output capacitance. The close look of the oscillations with simulation is shown in Figure 5.16. The frequency of the oscillations is about 20 MHz in simulation and the experimental result is about 17.5 MHz shown in Figure 5.17 at 50 kHz.

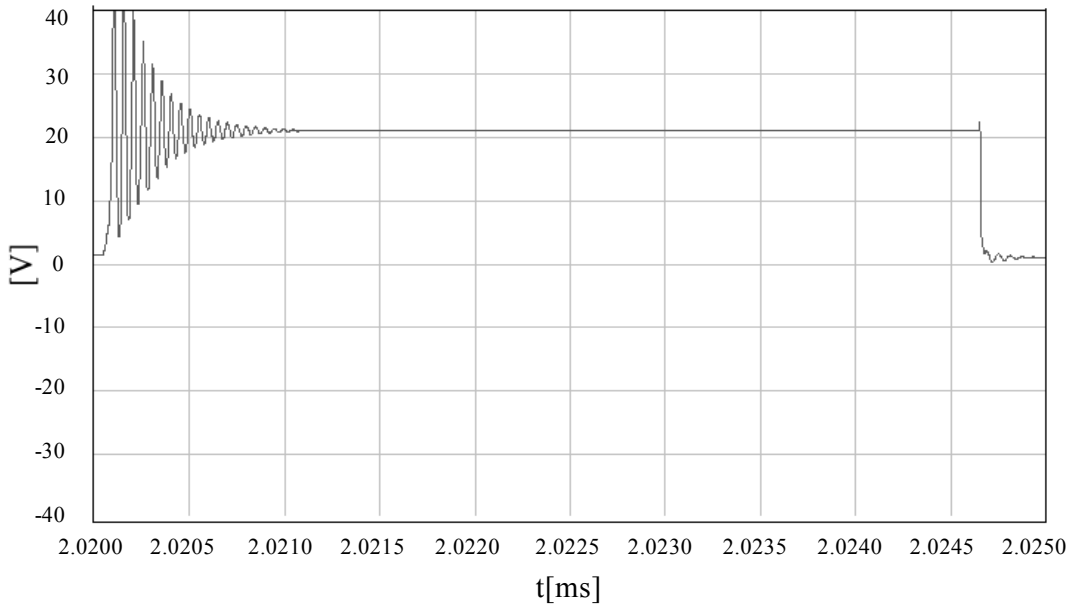


Figure 5.14 MOSFET Drain-Source voltage in PWM buck converter at 50 kHz (scales: 10 V/div and 500 ns/div).

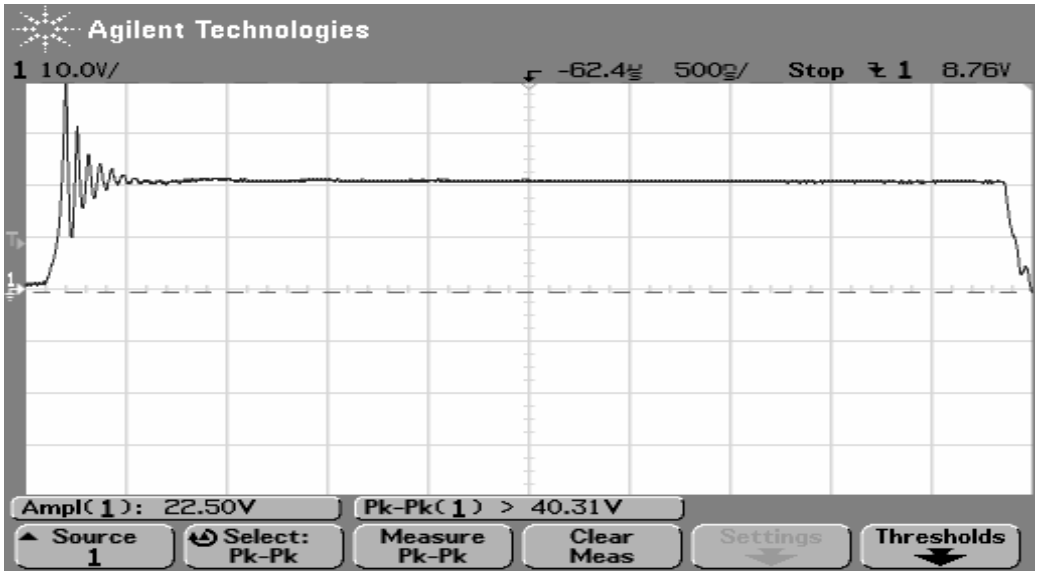


Figure 5.15 Experimental result of the MOSFET Drain-Source voltage at 50 kHz (scales: 10 V/div and 500 ns/div).

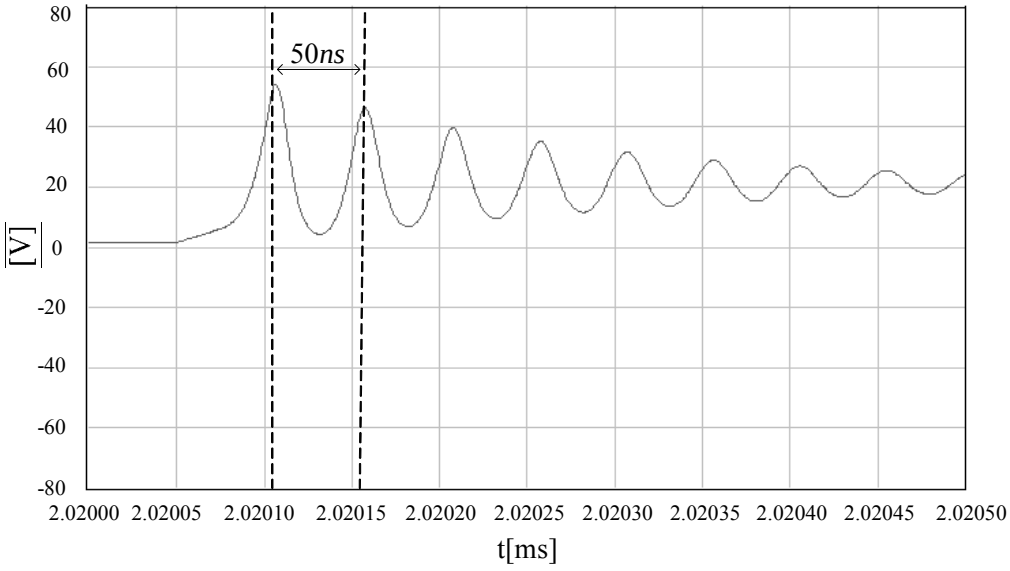


Figure 5.16 Simulation result of the MOSFET Drain-Source voltage oscillations (scales: 20 V/div and 50 ns/div).

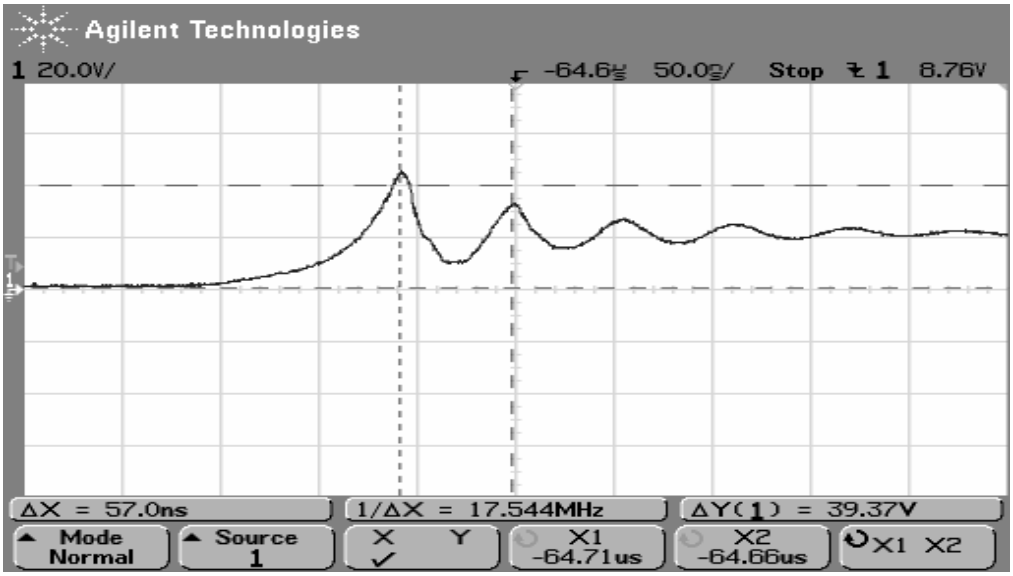


Figure 5.17 Experimental result of the MOSFET Drain-Source voltage oscillations (scales: 20 V/div and 50 ns/div).

Immediately after the diode current reduces to zero, voltage applied to the diode changes abruptly from zero to input voltage. In practice such an abrupt voltage change induces parasitic oscillations between the junction capacitance of the diode and the parasitic inductance. The simulation result of the output diode voltage waveforms is shown in Figure 5.18 at 100 kHz. The experimental result is also shown in Figure 5.19.

Output voltage is in PWM buck converter is insensitive to frequency change. The duty ratio of the gate signal is determined by the output voltage. The simulation result of the output voltage of the PWM buck converter with 100 kHz and an approximate duty ratio of %50 is shown in Figure 5.20. The average value of the output voltage is about 9.25 V. The experimental result of the output voltage is shown in Figure 5.21 with average value of 9.8 V. The mismatch of the load values may cause output voltage difference between the simulation and the experimental results.

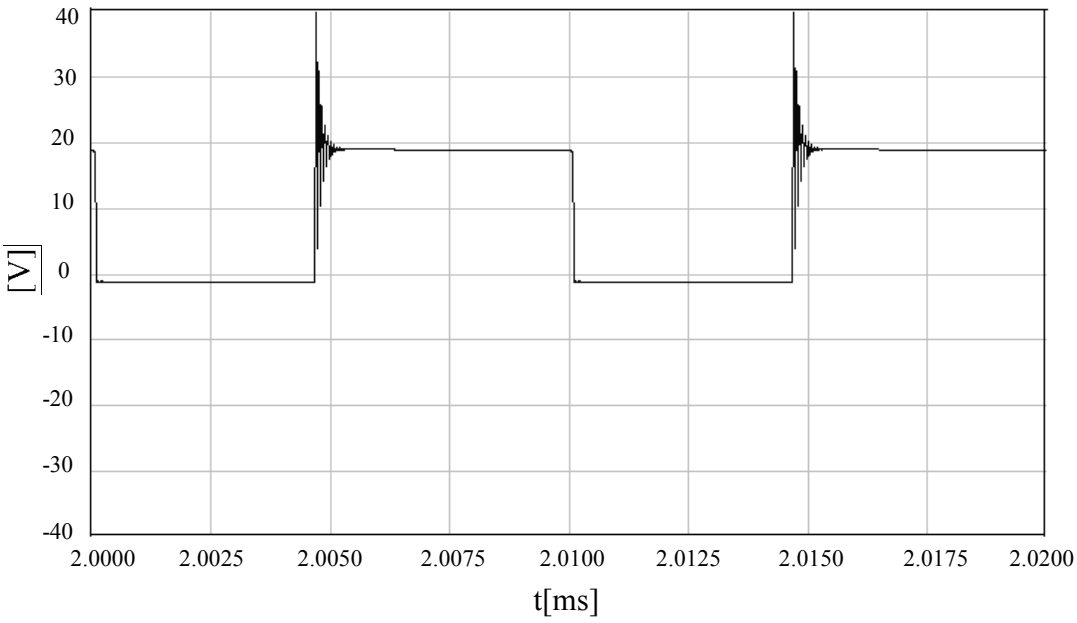


Figure 5.18 The simulation result of the output diode voltage at 100 kHz (scales: 10 V/div and 2.5 μs/div).

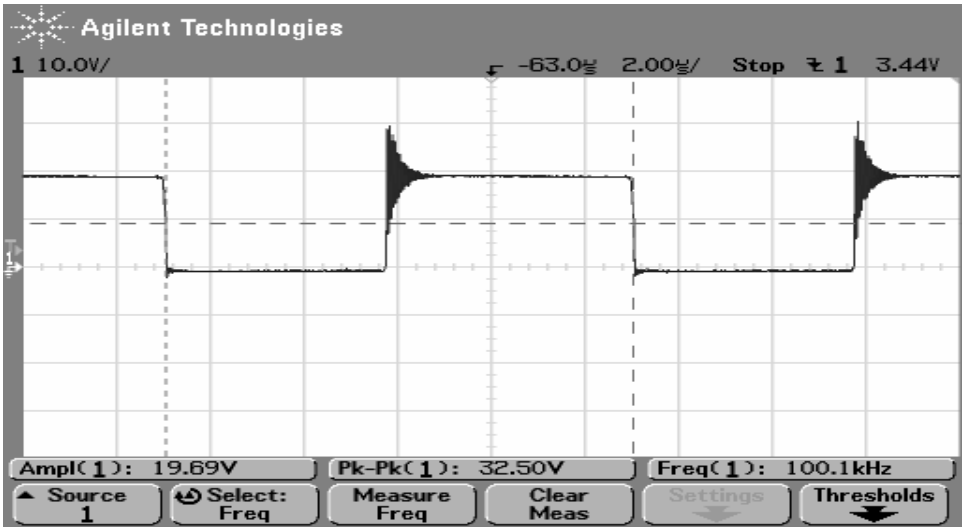


Figure 5.19 The experimental result of the output diode voltage at 100 kHz (scales: 10 V/div and 2 μs/div).

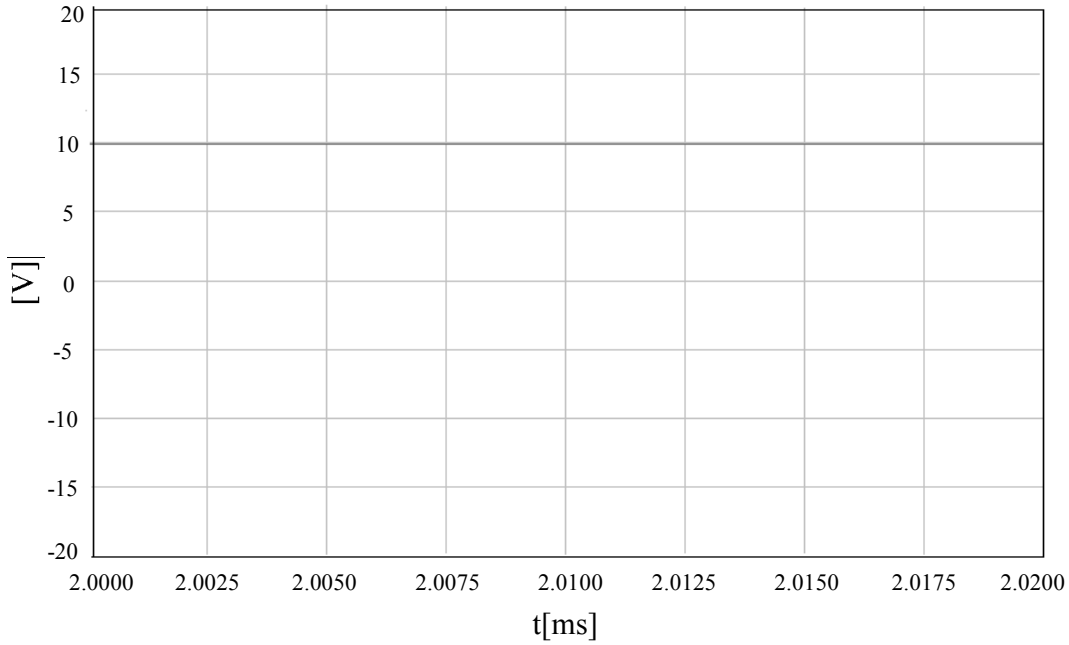


Figure 5.20 The simulation result of the output voltage (100 kHz, %50 duty ratio) (scales: 5 V/div and 2.5 µs/div).

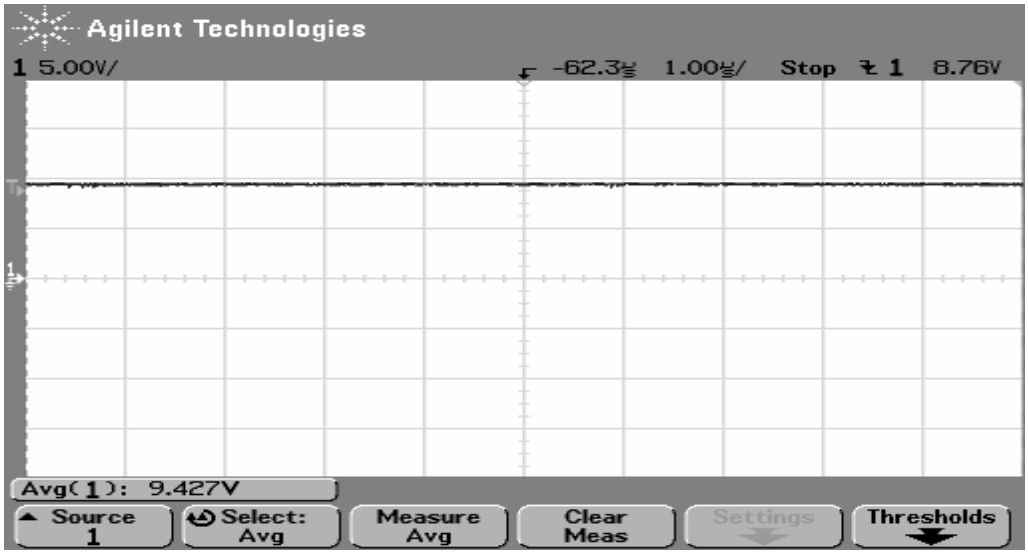


Figure 5.21 The experimental result of the output voltage (100 kHz, %50 duty ratio) (scales: 5 V/div and 1 µs/div).

5.7.2 Open-Loop ZVS Quasi-Resonant Buck Converter

The open loop zero-voltage switching quasi-resonant converter is achieved by inserting a resonant capacitor and a diode in parallel with the MOSFET and a resonant inductor in series with the MOSFET. The MOSFET Drain-Source voltage in ZVS QRC converters is quasi-sinusoidal because of the resonance between the capacitor and the inductor as mentioned before. When the voltage across the MOSFET reduces to zero, the MOSFET is turned on with zero voltage and switching losses are eliminated even at high frequencies. The simulation result of the Drain-Source voltage (V_{DS}) and the resonant inductor current (I_{Lr}) waveforms are shown in Figure 5.22 with 20 V dc supply voltage and load resistor of 10 Ω. The frequency of the gate signal is 50 kHz and the off-time is fixed at about 4.5 μs. The amplitude of the resonant capacitor voltage is approximately 75 V in simulation. The experimental results for the Drain-Source voltage and the resonant inductor waveforms are shown in Figure 5.23. The amplitude of the resonant capacitor voltage is 76.3 V. The experimental resonant inductor current is nearly same as the simulation one. The simulation and experimental results match quite perfectly.

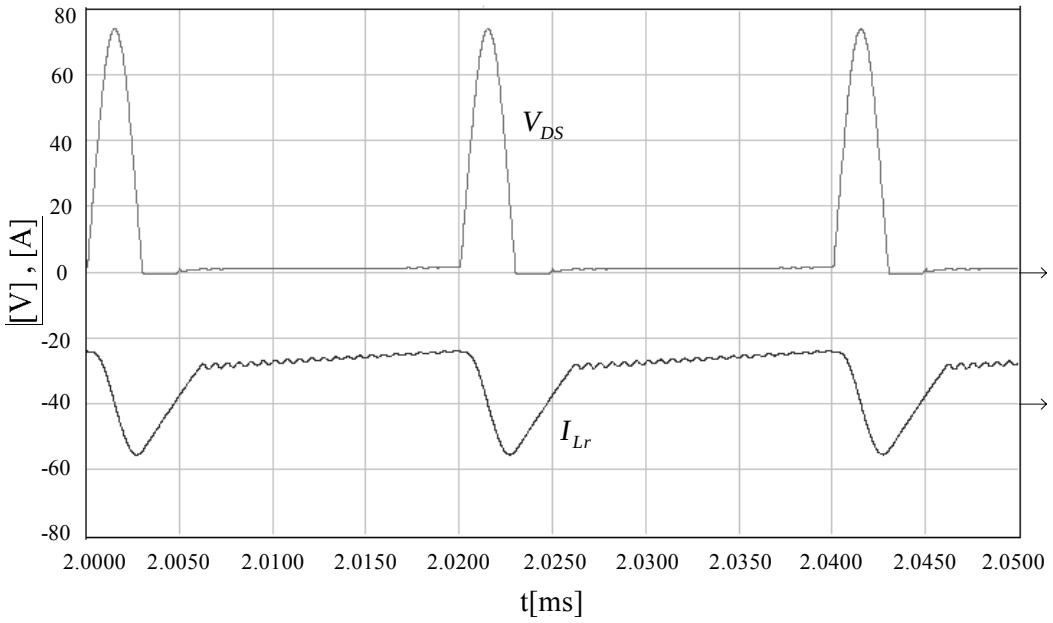


Figure 5.22 The simulation result of the Drain-Source voltage and the resonant inductor waveforms (50 kHz, 10 Ω) (scales: 20 V/div and 2 A/div, current probe x10).

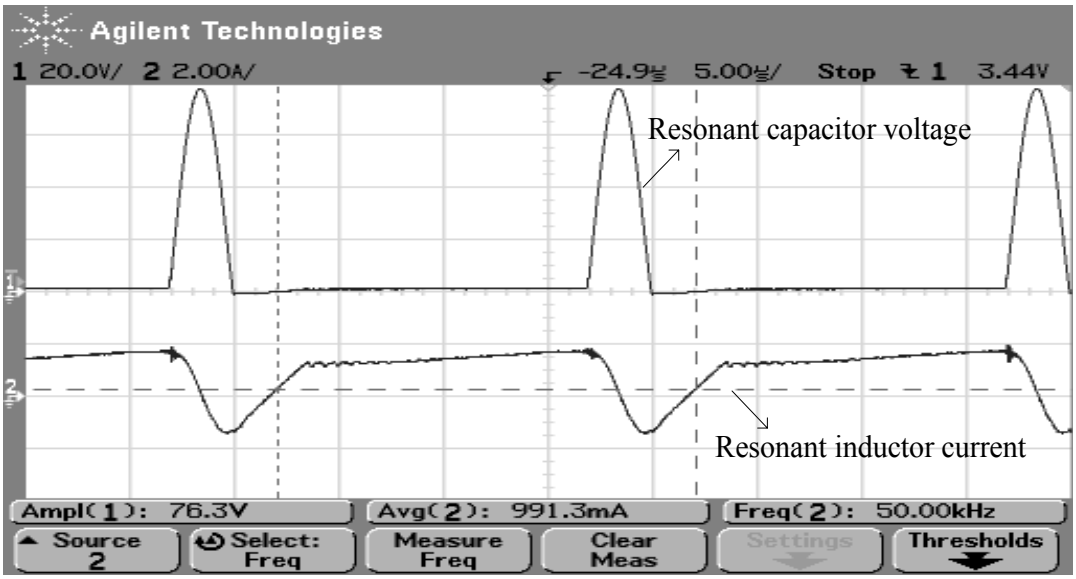


Figure 5.23 The experimental results of the Drain-Source voltage and the resonant inductor waveforms (50 kHz,10 Ω) (scales: 20 V/div, 2 A/div, 5 µs/div).

The simulation results for the Drain-Source voltage and the resonant inductor waveforms are shown in Figure 5.24 with 20 V dc supply voltage and a load resistance of 10 Ω at 71.5 kHz. The amplitude of the resonant capacitor voltage is reduced when the frequency increases. This is because the voltage conversion ratio is dependent on the switching frequency. If the switching frequency is reduced, the output voltage also decreases. The resonant capacitor voltage is proportional to load current. The amplitude of the resonant capacitor voltage is 67 V in simulation. The experimental results for the Drain-Source voltage (V_{DS}) and the resonant inductor current (I_{Lr}) waveforms are shown in Figure 5.25. The amplitude of the resonant capacitor voltage is 67.7 V.

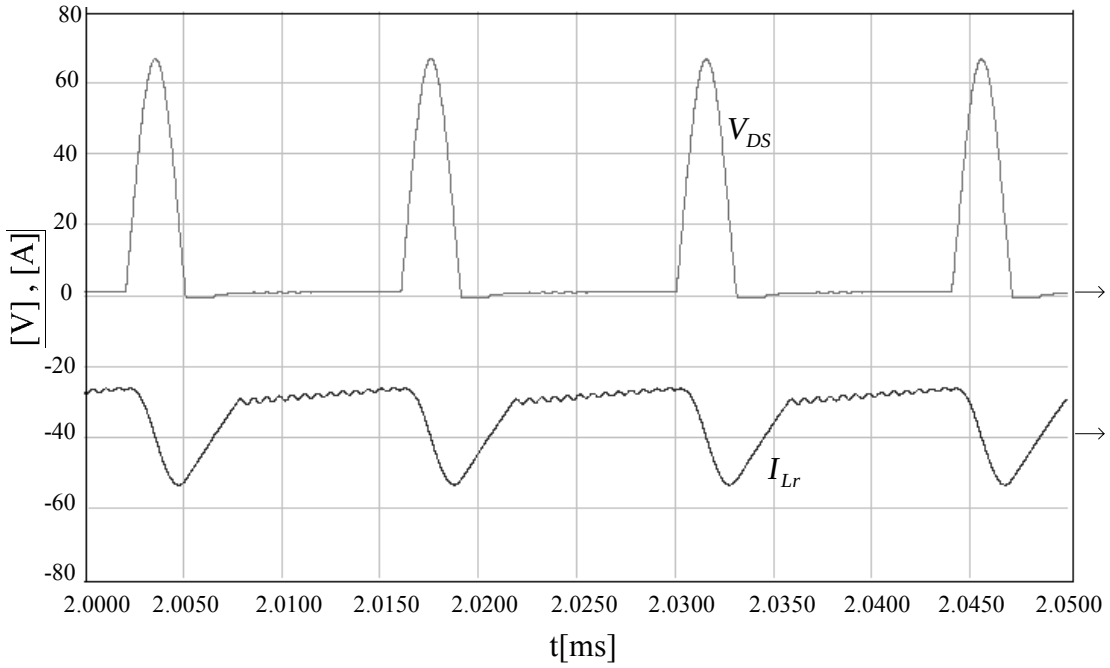


Figure 5.24 The simulation result of the Drain-Source voltage and the resonant inductor waveforms (71.5 kHz, 10 Ω) (scales: 20 V/div, 2 A/div, 5 μs/div and current probe x10).

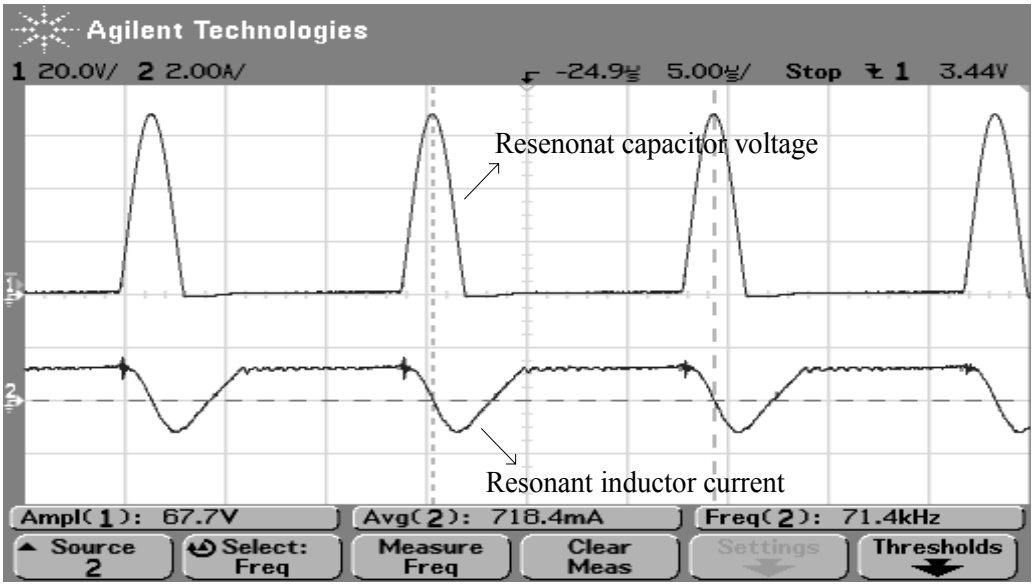


Figure 5.25 The experimental results of the Drain-Source voltage and the resonant inductor waveforms (71.5 kHz, 10 Ω) (scales: 20 V/div, 2 A/div, 5 μs/div).

The simulation results for the Drain-Source voltage and the resonant inductor waveforms are shown in Figure 5.26 at 100 kHz. The experimental results for the Drain-Source voltage and the resonant inductor waveforms are shown in Figure 5.27 at 100 kHz. The amplitude of the capacitor voltage is 57.5 V in simulation. The experimental value is 58 V.

The resonant capacitor voltage and the resonant inductor current are simulated at different load levels at 71.5 kHz. When the load resistor decreases, the resonant capacitor voltage amplitude increases. The simulation result of the Drain-Source voltage (V_{DS}) and the resonant inductor current (I_{Lr}) waveforms are shown in Figure 5.28 with 20 V dc supply voltage and a load resistance of 5 Ω at 71.5 kHz. The experimental results for the Drain-Source voltage and the resonant inductor waveforms are shown in Figure 5.29. The amplitude of the MOSFET Drain-Source voltage is 81 V in simulation. The simulation and the experimental results match quite perfectly.

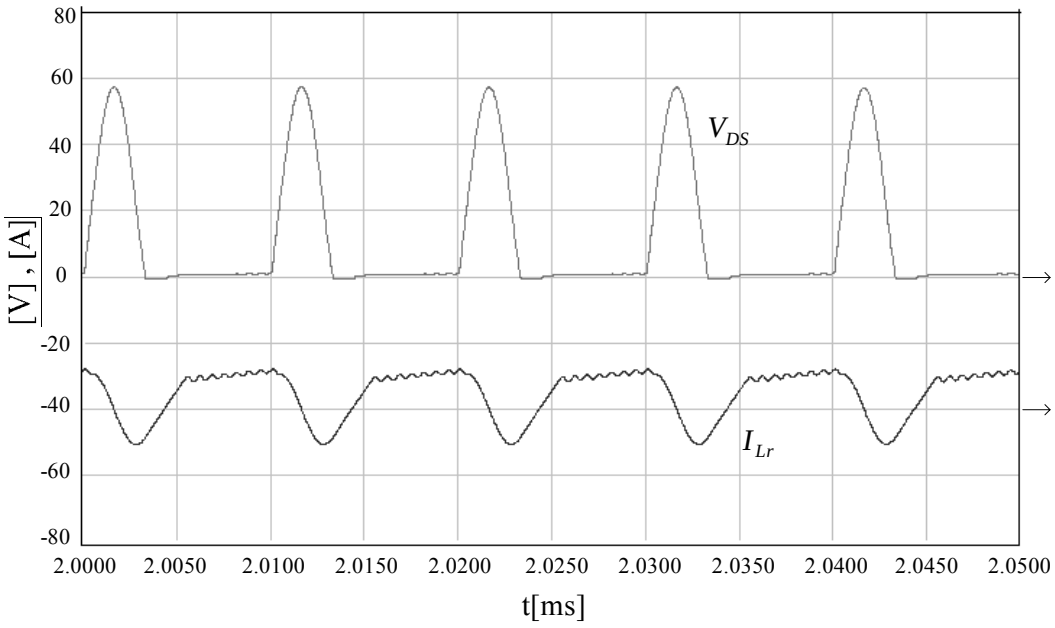


Figure 5.26 The simulation result of the Drain-Source voltage and the resonant inductor waveforms (100 kHz, 10 Ω) (scales: 20 V/div, 2 A/div, 5 μs/div and current probe x10).

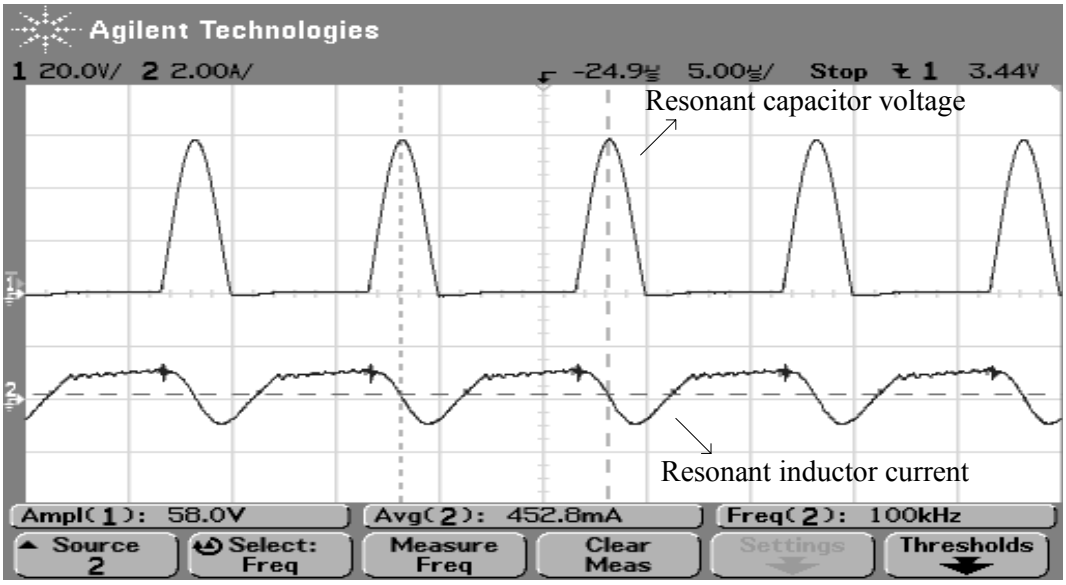


Figure 5.27 The experimental results of the Drain-Source voltage and the resonant inductor waveforms (100 kHz, 10 Ω) (scales: 20 V/div, 2 A/div).

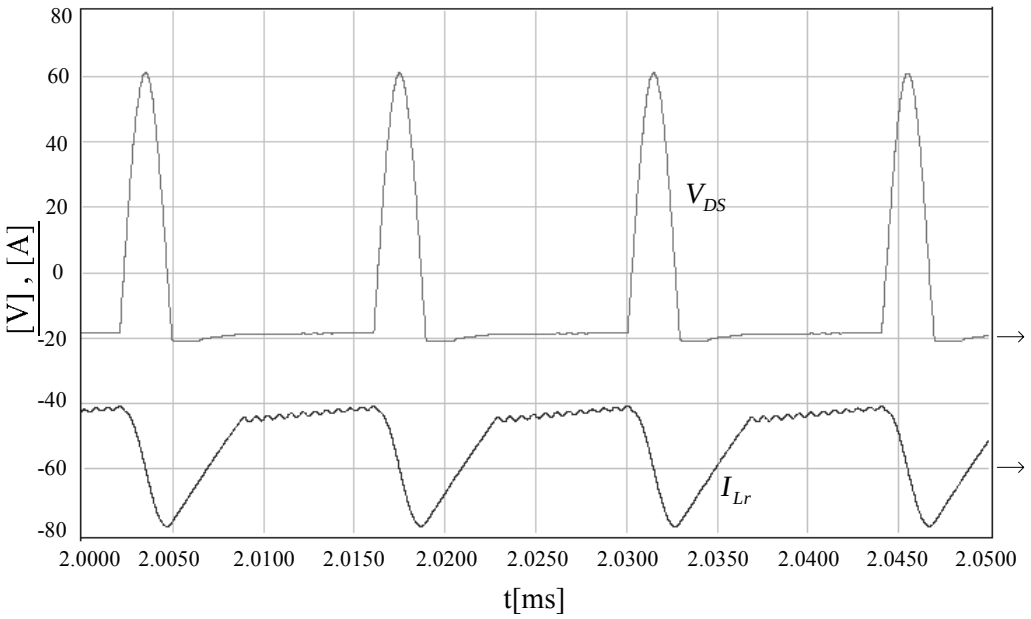


Figure 5.28 The simulation result of the Drain-Source voltage and the resonant inductor waveforms (71.5 kHz, 5 Ω) (scales: 20 V/div, 2 A/div, 5 μs/div and current probe x10).

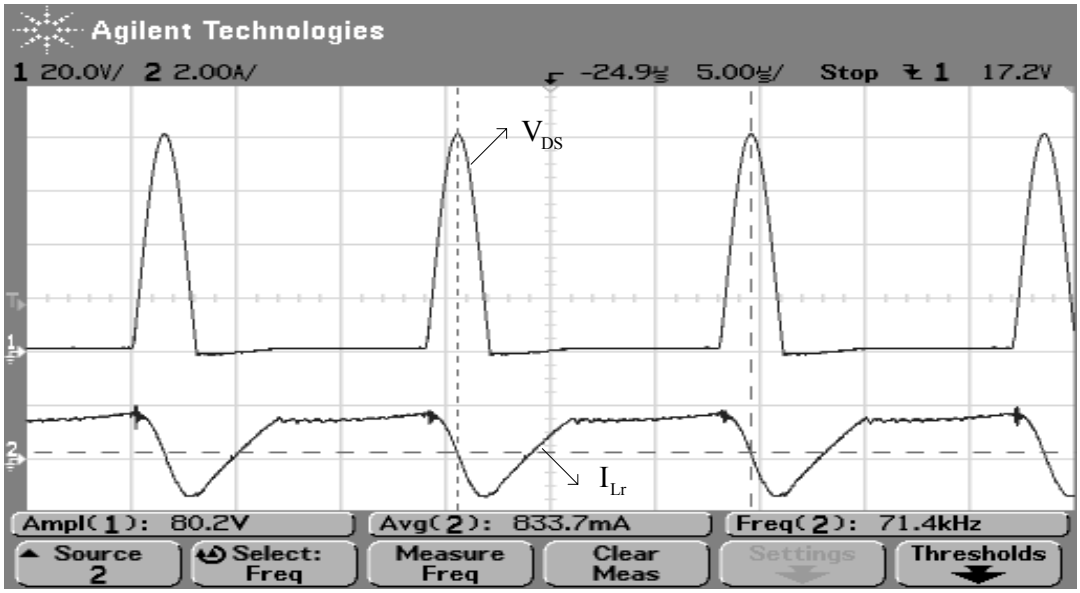


Figure 5.29 The experimental results of the Drain-Source voltage and the resonant inductor waveforms (71.5 kHz, 5 Ω) (scales: 20 V/div, 2 A/div, 5 μs/div).

When the load decreases until the M < r, the zero-voltage switching property may be lost. The simulation result of the non-zero turn-on of the MOSFET Drain-Source voltage is shown in Figure 5.30 with 20 V dc supply voltage and a load resistance of 40 Ω at 71.5 kHz. The experimental result is shown in Figure 5.31.

The simulation result of the output voltage is shown in Figure 5.32 when the dc supply voltage 24 V and the load resistor is 10 Ω at 50 kHz. The output voltage is approximately 14.9 V. The experimental result of the output voltage is shown in Figure 5.33 under the same conditions. The approximate value of the output voltage is 14.3 V and is very close to the simulated value.

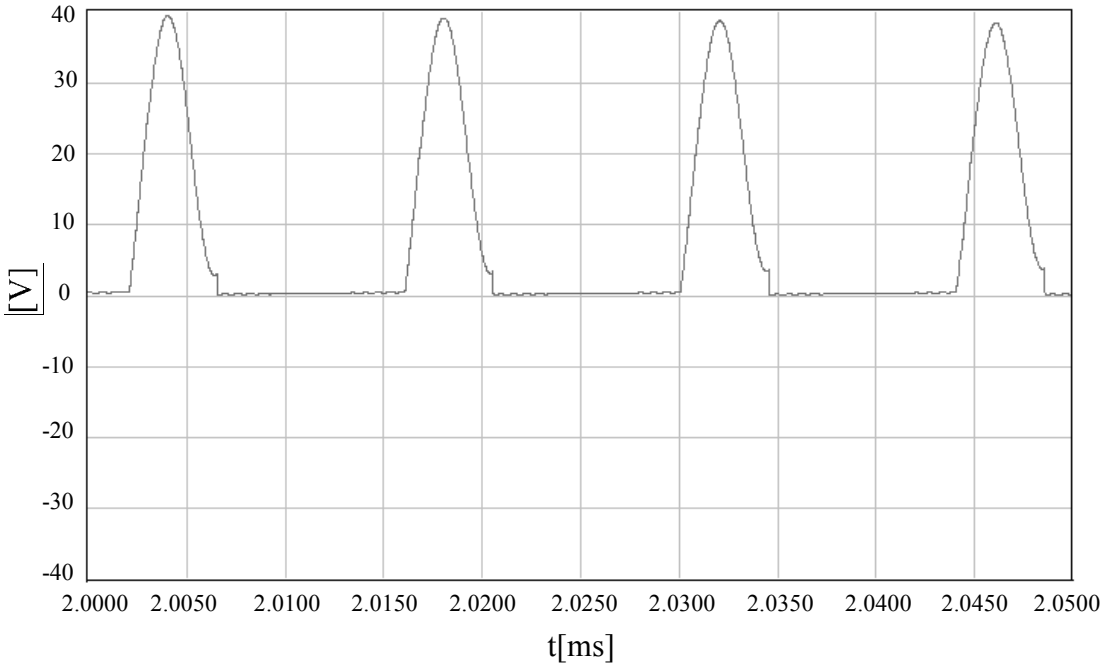


Figure 5.30 The simulation result of the Drain-Source voltage with non-zero turn-on (71.5 kHz, 40 Ω) (scales: 10 V/div, 5 μs/div).

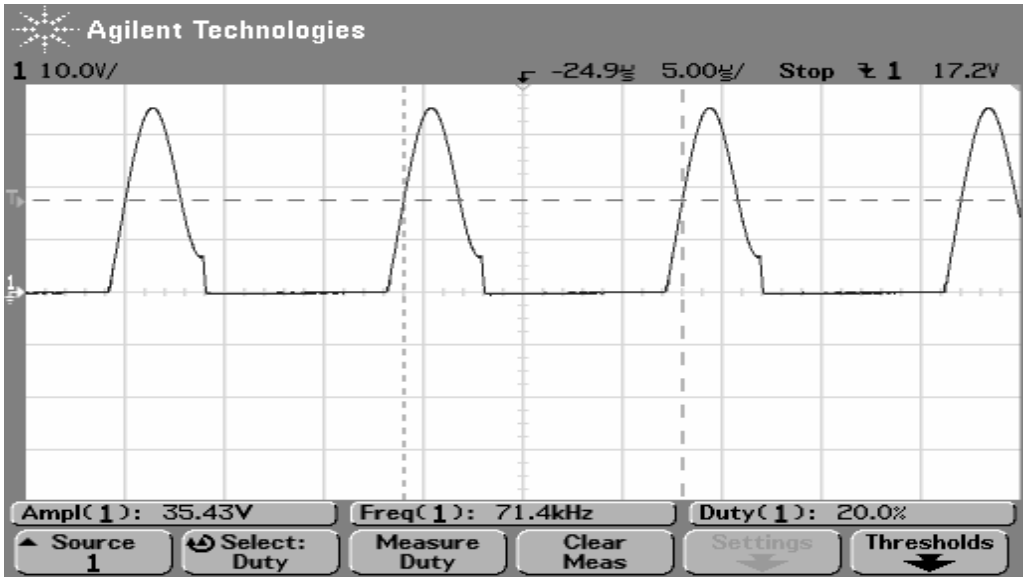


Figure 5.31 The experimental result of the Drain-Source voltage with non-zero turn-on (71.5 kHz, 40 Ω) (scales: 10 V/div, 5 µs/div).

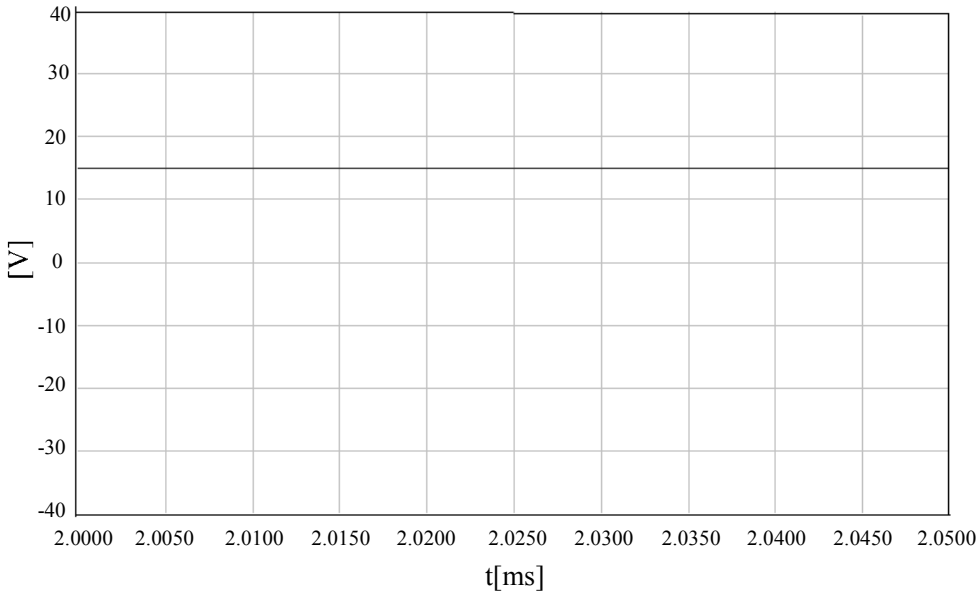


Figure 5.32 The simulation result of the output voltage (50 kHz, 4.5 µs off-time, 24 V DC and 10 Ω) (scales: 10 V/div, 5 µs/div).

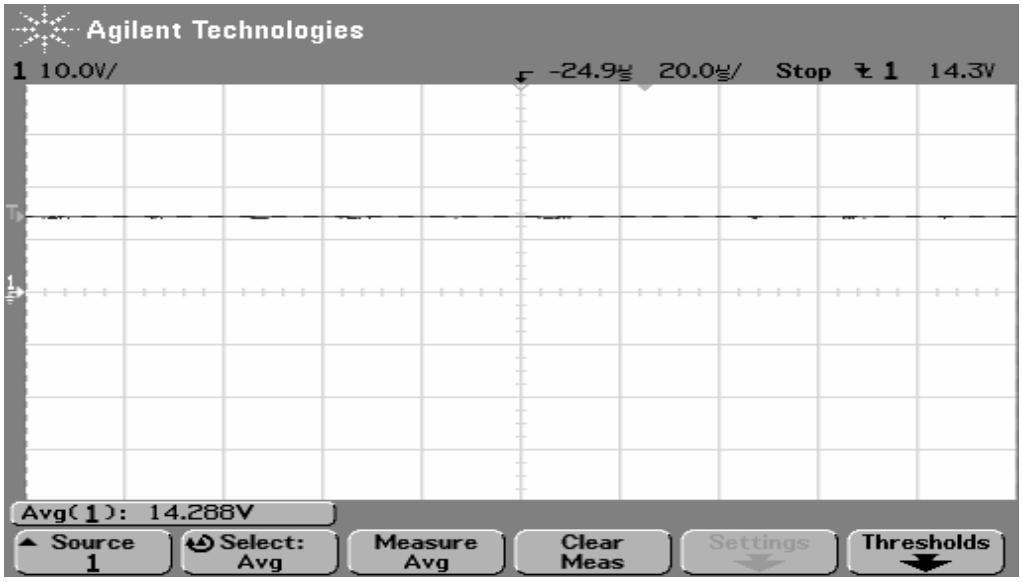


Figure 5.33 The experimental result of the output voltage (50 kHz, 4.5 μs off-time, 24 V DC and 10 Ω) (scales: 10 V/div, 20 μs/div).

The simulation result of the voltage waveform of the output diode is shown in Figure 5.34 at 50 kHz. The voltage applied to the diode changes abruptly when the current through the diode reduces to zero. This voltage change induces parasitic oscillations between the resonant inductor and the junction capacitance of the diode. The zero-voltage switching QRC technique does not provide favorable switching conditions for the output diode and therefore the output diode voltage waveform is oscillatory. The experimental result for the voltage waveform of the output diode is shown in Figure 5.35.

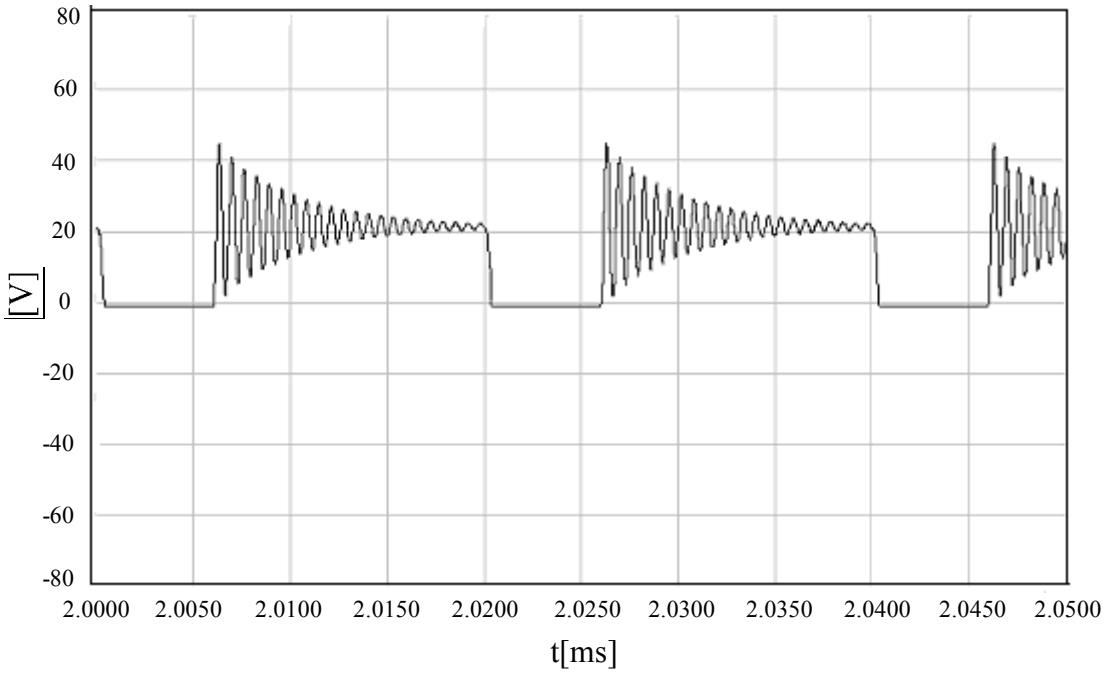


Figure 5.34 The simulation result of the voltage of the output diode at 50 kHz (scales: 20 V/div, 5 μs/div).

5.7.3 Closed-Loop ZVS Quasi-Resonant Buck Converter

The closed-loop circuit parameters are the same as the open-loop ZVS QRC buck converter. The DC input voltage is 24 V and the load resistance is 12 Ω. Another 12-Ω load resistor is connected in parallel with the load through a switch. When the switch is turned on, the load is switched from half load to full load. The simulation result of the output voltage when the switch is turned on is shown in Figure 5.36. The experimental result for the output voltage when the switch is turned on is shown in Figure 5.37.

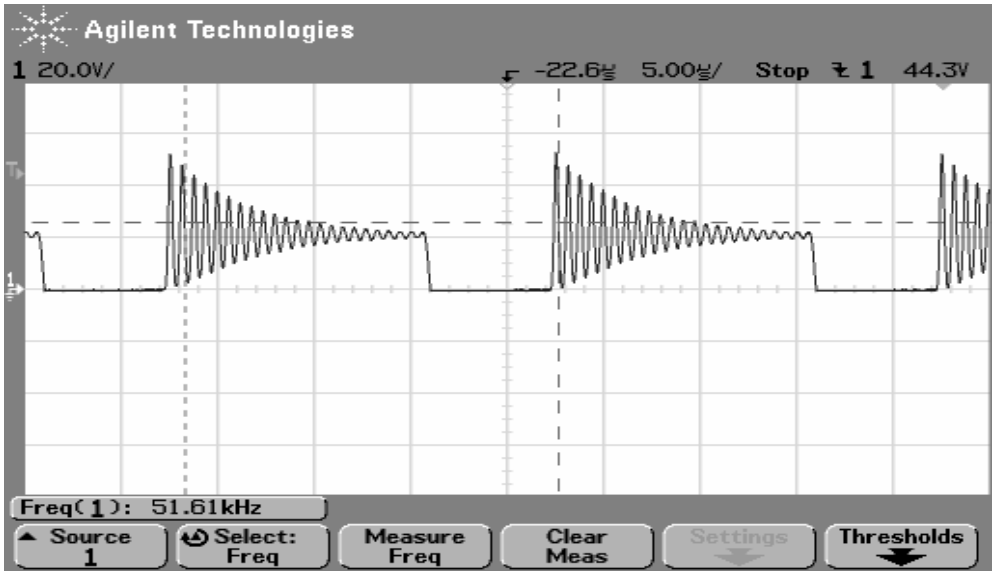


Figure 5.35 The experimental result of the voltage of the output diode at 50 kHz (scales: 20 V/div, 5 µs/div).

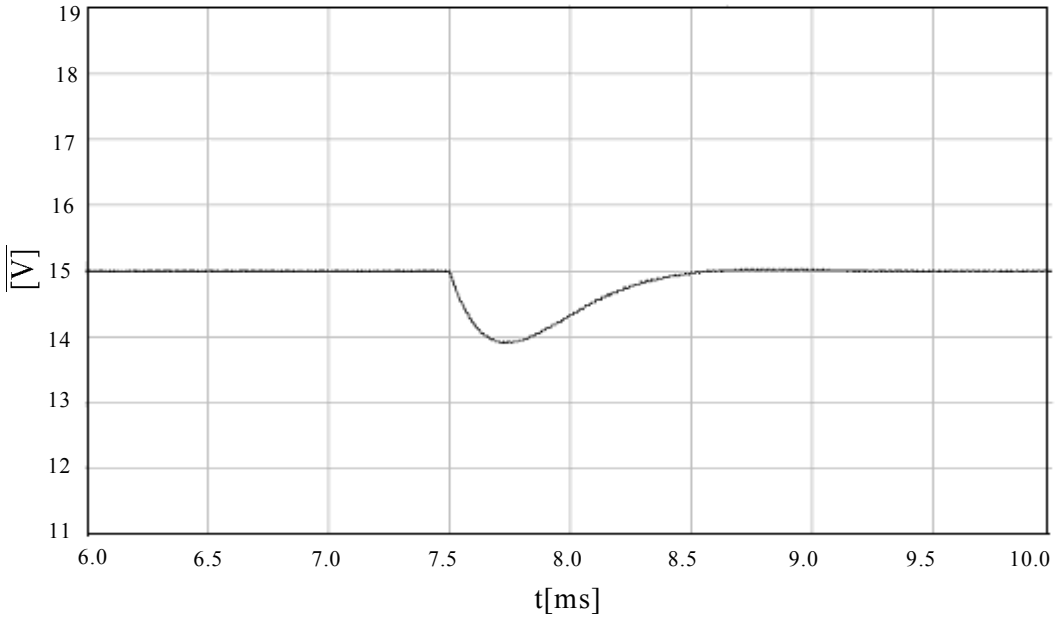


Figure 5.36 The simulation result of the output voltage from half-load to full-load (scales: 1 V/div, 0.5 ms/div).

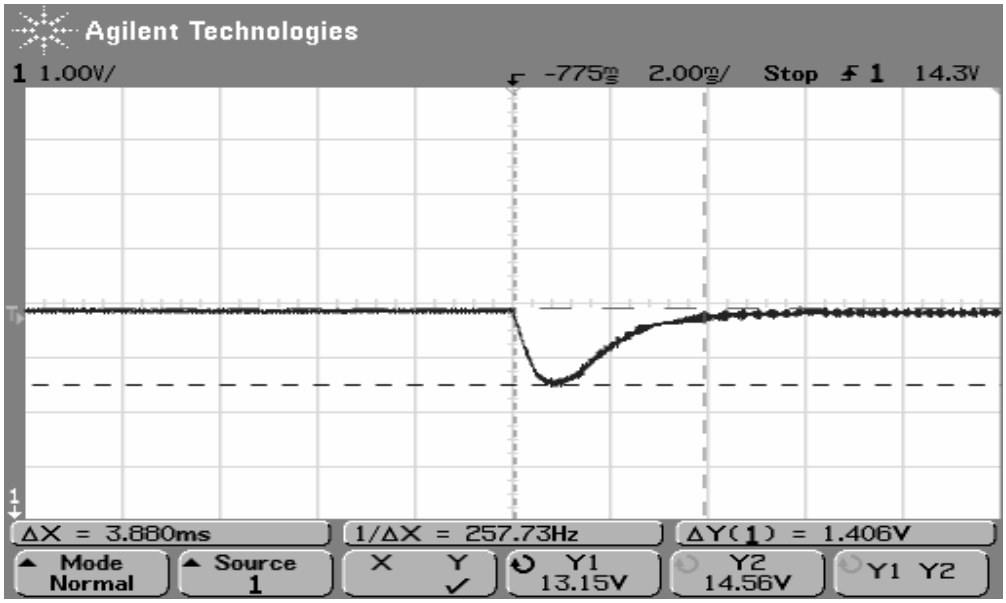


Figure 5.37 The experimental result of the output voltage from half-load to full-load (scales: 1 V/div,2 ms/div).

The simulation result of the output voltage when the load changes from full-load to half-load is shown in Figure 5.38. The experimental result of the output voltage when the switch is turned off is shown in Figure 5.39.

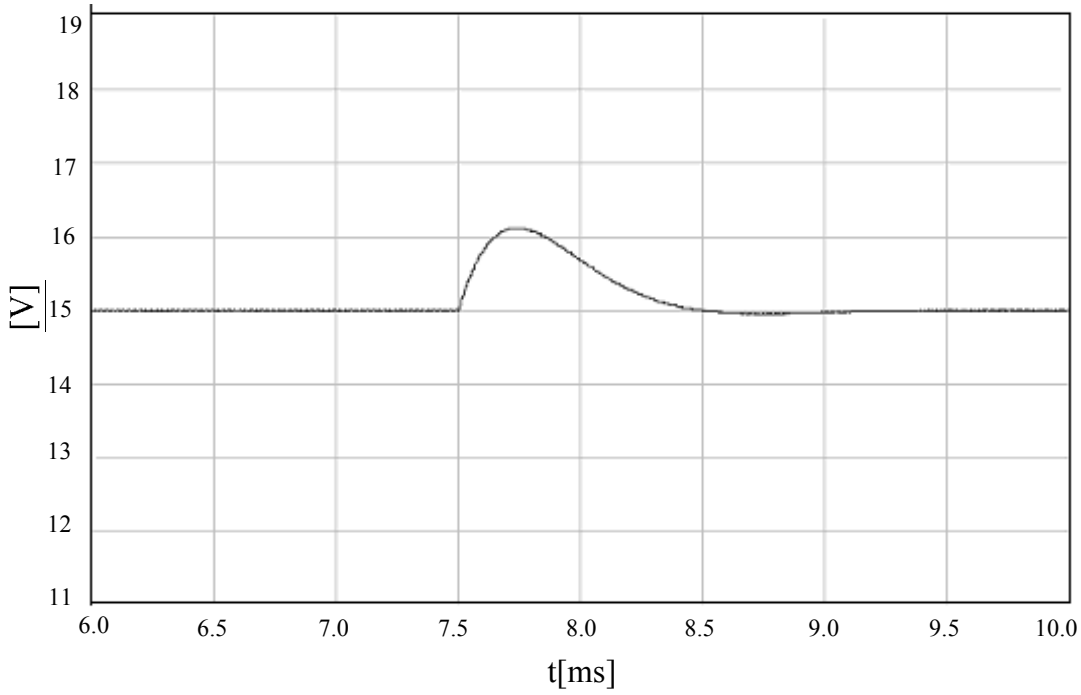


Figure 5.38 The simulation result of the output voltage from full-load to half-load (scales: 1 V/div, 0.5 ms/div).

When the circuit operates at 50 kHz in closed-loop, the step change in line voltage occurs with the amplitude of 6 V. The simulation result for the output voltage when the load changes from full-load to half-load is shown in Figure 5.40. The experimental result for the output voltage when the switch is turned off is shown in Figure 5.41.

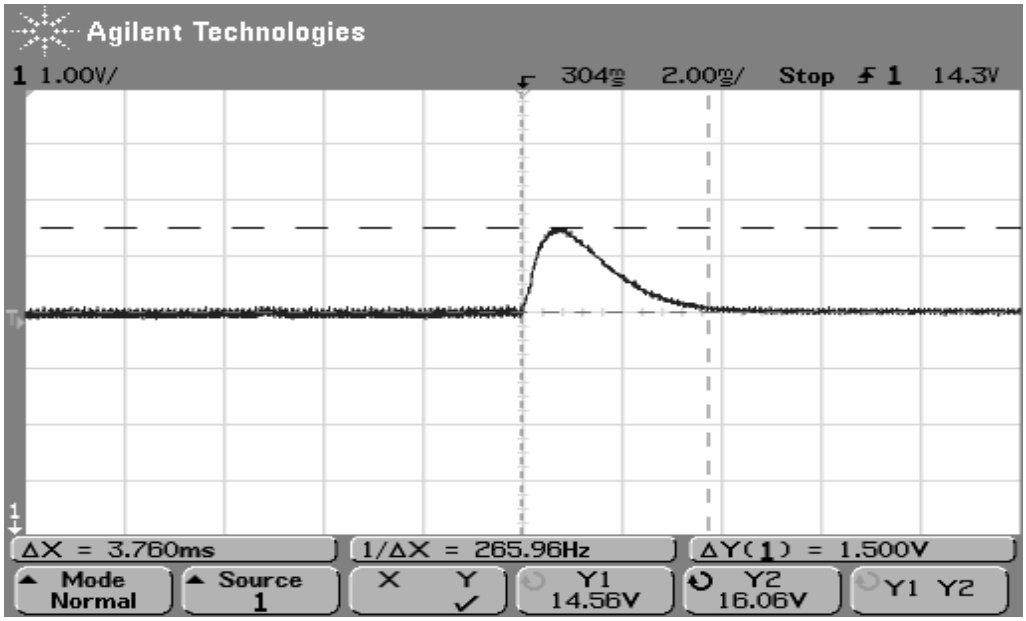


Figure 5.39 The experimental result of the output voltage from full-load to half-load (scales: 1 V/div, 2 ms/div).

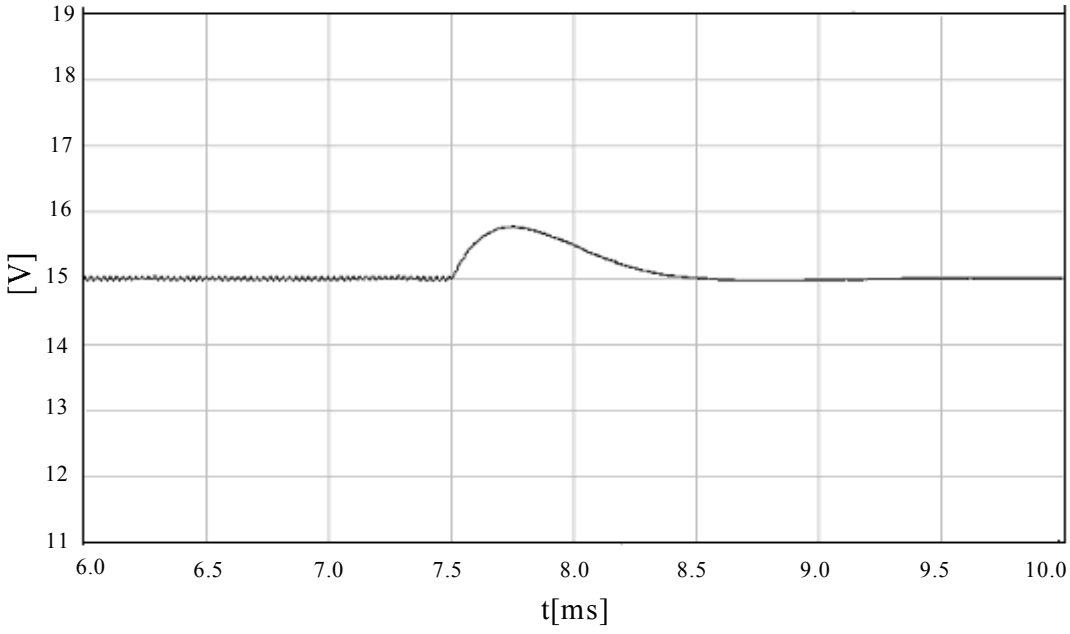


Figure 5.40 The simulation result of the output voltage for %25 line voltage change (scales: 1 V/div, 0.5 ms/div).

The response of the single-loop controlled ZVS QR buck converter is presented. The step change occurs, and 15 V output has an overshoot of 1.5 V for the step load and approximately 2.1 V for the step line, both with a settling time of less than 4ms. The experimental result of the output voltage of the closed loop ZVS QR buck converter is shown in Figure 5.42.

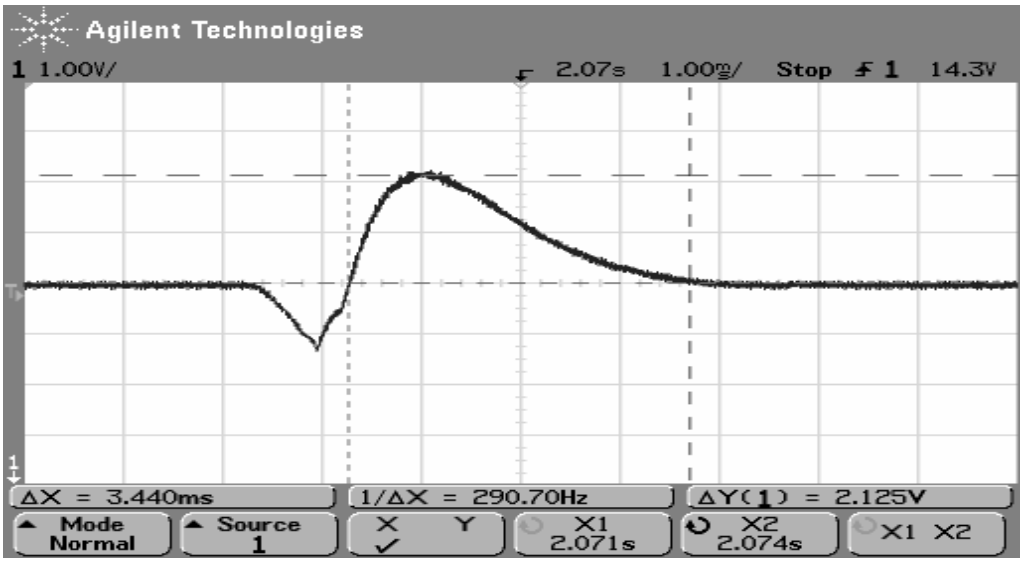


Figure 5.41 The experimental result of the output voltage for %25 line voltage change (scales: 1 V/div, 1 ms/div).

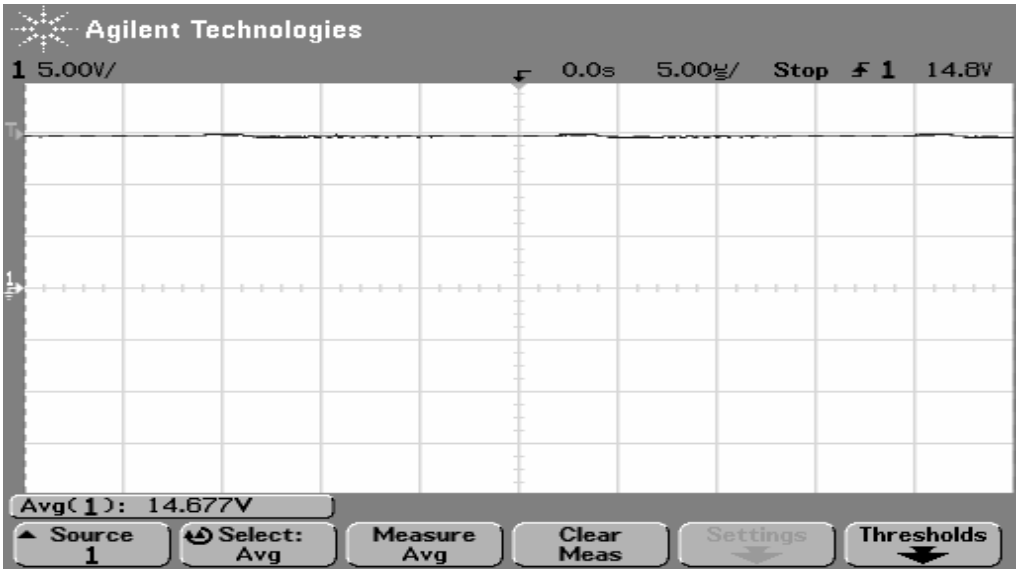


Figure 5.42 The experimental result of the output voltage (24 V DC in and 12 Ω) (scales: 5 V/div, 5 s/div).

In summary, for conventional PWM converters the high frequency oscillations present on the switch voltage were illustrated experimentally and the results could be correlated to the computer simulations and analysis. However, differences between the simulation and the experimental results were noticed and these differences could be caused by the un-modeled behavior of the parasitic components in the circuit. Moreover, unfavorable switching conditions for both active and passive switches were illustrated experimentally.

The oscillation problems could be eliminated by the soft-switching method more effectively than the other passive snubber methods. Moreover, this method presents the advantage of superior switching conditions for the active switch in the converter. The switching waveforms were illustrated experimentally without any oscillations on them and the experimental results obtained have supported the simulation results. The experiments also illustrated that the voltage conversion ratio of the proposed converter

were mainly dependent on the load and the switching frequency values. The differences between the simulation and the experimental results for the output voltage could be mainly attributed to the unpredictable behavior of the gate drive circuitry. Moreover, the settling time and the overshoot of the output voltage were different. The differences could be caused by the controller component variations.

CHAPTER 6

EXPERIMENT MANUAL

6.1 Objective

The main object of this experiment is to investigate the properties of the soft-switching technique. This chapter covers the experiments based on the soft-switching concept for dc-dc converters. Firstly, introduction of the implemented soft-switching system is carried out. The experiments are prepared according to undergraduate curricula with different experiment scenarios and are intended to help the user to understand the basics of soft-switching technique. All steps of the experiment include connection diagrams, block schemes, measurement procedure and experimental results. The experiment procedure from simple to complex may help to concentrate the user's attention on the experiments.

The first step is to analyze the switching behaviors of power MOSFET and output diode operating under hard switching conditions. Focus is on turn-on and turn-off conditions. Moreover, the oscillations which are present on the voltage waveforms are illustrated. The second step is to demonstrate the operation of zero-voltage switching quasi-resonant buck converter. Also the switch properties and important waveforms are to be verified under varying load and frequency conditions. Furthermore, it is aimed to observe the voltage conversion ratio for the resonant buck converter. The last step is to investigate the output voltage characteristics when changes occur in input voltage and load. The settling time, overshoot and controller performance are obtained.

6.2 Theory of the Experiment

Conventional Pulse-Width Modulation (PWM) power processing technology has been widely used in today's power electronics industry, particularly in low-power application due to circuit simplicity and ease of control. In PWM converters, the output voltage is directly controlled by the duty cycle of the switch gate signal. That is to say, the PWM is duty cycle controlled power processing technique and power flow is interrupted by this phenomena. The PWM power processing technique maintains a constant switching frequency and varies the duty cycle. The current and voltage waveforms are quasi-square.

There are two switching events that take place in the generalized switching model called as turn-on and turn-off in PWM converters. However, transition between on and off states produces switching losses because of the simultaneously occurring high current and voltage values. During the switching intervals, instantaneous power dissipated in the semiconductor switch can be larger than the power loss occurring while conducting. The average loss depends on the speed of the switching interval and switching frequency of the switching converter.

Quasi-resonant conversion technique offers a general approach for improvement of switching conditions. The quasi-resonant converters are directly derived from conventional PWM topologies by adding only two additional components. This family of circuits can be viewed as a hybrid of PWM and resonant converters. The resonant action takes place only one mode of these converters and this is why they are called the "quasi-resonant converters".

When energy is injected into an L-C resonant tank circuit, the energy is exchanged between the inductor and the capacitor in a periodical and quasi-sinusoidal fashion. Because of this quasi-sinusoidal oscillation, L-C resonant tank circuit can be used as a lossless or low-loss waveform-shaping device.

The quasi-resonant technique is divided into two different parts: zero-current switching technique and zero-voltage switching technique. By incorporating the L-C resonant circuit, the current waveform of the switch is forced to oscillate in a sinusoidal manner, therefore, creating zero-current switching conditions during both turn-on and turn-off. The second technique is used to shape the voltage waveform of the switching device into a quasi-sine wave, such that zero voltage condition is created for the switch to turn on and turn off without any switching losses.

A resonant switch represents a subcircuit consisting of power switch and auxiliary resonant elements L_R and C_R. In order to achieve zero-voltage switching, the resonant capacitor is in parallel with switch and the resonant inductor is in series with them shown in Figure 6.1.

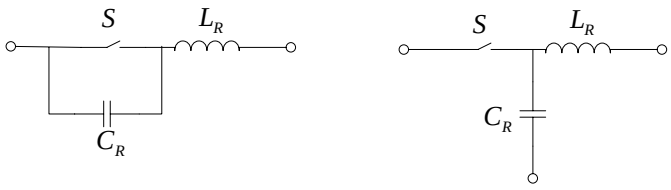


Figure 6.1 Zero-voltage resonant switches.

If a diode is connected in anti-parallel with the active switch, the voltage across capacitor C_R is clamped by the diode at zero during negative half of the resonant cycle. This implementation is called half-wave network. If this diode is connected in series with the active switch, the voltage across capacitor C_R oscillates freely, and this arrangement is called full-wave network.

A basic circuit diagram of the half-wave ZVS quasi-resonant buck converter is shown in Figure 6.2. Inductance L_R and capacitor C_R form a resonant network. This network shapes the voltage across switch S during its off time for zero-voltage turn-on. The output filter consists of L_F and C_F, and D_0 is a freewheeling diode.

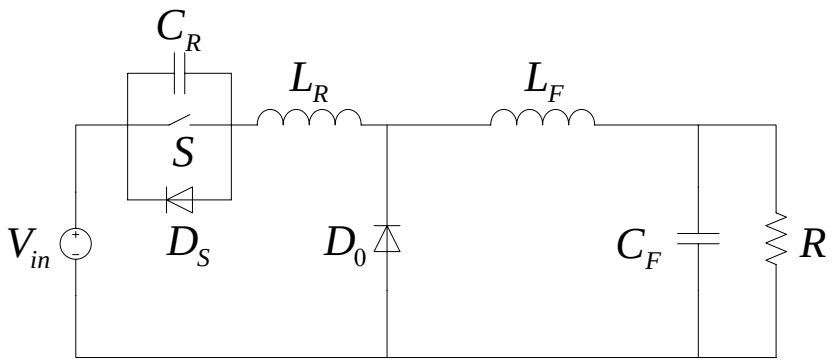


Figure 6.2 Basic circuit diagram of half-wave ZVS QR buck converter.

For buck converters, the conversion ratio M is defined by:

$$M = \frac{V_o}{V_{in}} \tag{6.1}$$

where V_0 is the output voltage and V_{in} is the input dc voltage.

The operation and characteristics of the converter depend mainly on the design of the resonant circuit L_R and C_R. The following parameters determine the converter characteristics:

Characteristic Impedance Z_N:

$$Z_N = \sqrt{\frac{L_R}{C_R}} \tag{6.2}$$

Resonant Frequency f_R:

$$f_R = \frac{1}{2\pi\sqrt{L_R C_R}} \tag{6.3}$$

Normalized Load Resistance r:

$$r = \frac{R}{Z_N} \tag{6.4}$$

where R is the load resistance of the converter.

Typical theoretical waveforms of the ZVS quasi-resonant buck converter are shown in Figure 6.3. In steady-state operation, a complete converter switching cycle is divided into four intervals; capacitor charging stage (t_0-t_1), resonant stage (t_1-t_2), inductor discharging stage (t_2-t_3) and freewheeling stage (t_3-t_4).

Prior to t_0, switch S is conducting. Consequently, the diode D_0 is reverse-biased, and the output current flows through the load.

6.2.1 Capacitor-Charging Stage (t_0-t_1)

At the beginning of this interval, at t_0, the switch S is turned off, the output current starts to flow through the resonant capacitor (diode D_0 is still reverse-biased) and voltage V_{DS} increases linearly. When V_{DS} is equal to the input voltage, diode D_0 turns on.

$$T_{01} = \frac{C_R V_{in}}{I_0} = \frac{1}{w}\frac{r}{M} \tag{6.5}$$

where

$$w = 2\pi f_R \tag{6.6}$$

6.2.2 Resonant Stage (t_1-t_2)

This interval begins when the capacitor voltage V_{DS} reaches V_{in} and the rectifier diode D_0 becomes forward biased. This causes the resonant element to resonate. During resonance, the voltage of the resonant capacitor C_R across the switch reaches its peak value:

$$V_{DSpeak} = I_0 Z_N + V_{in} \tag{6.7}$$

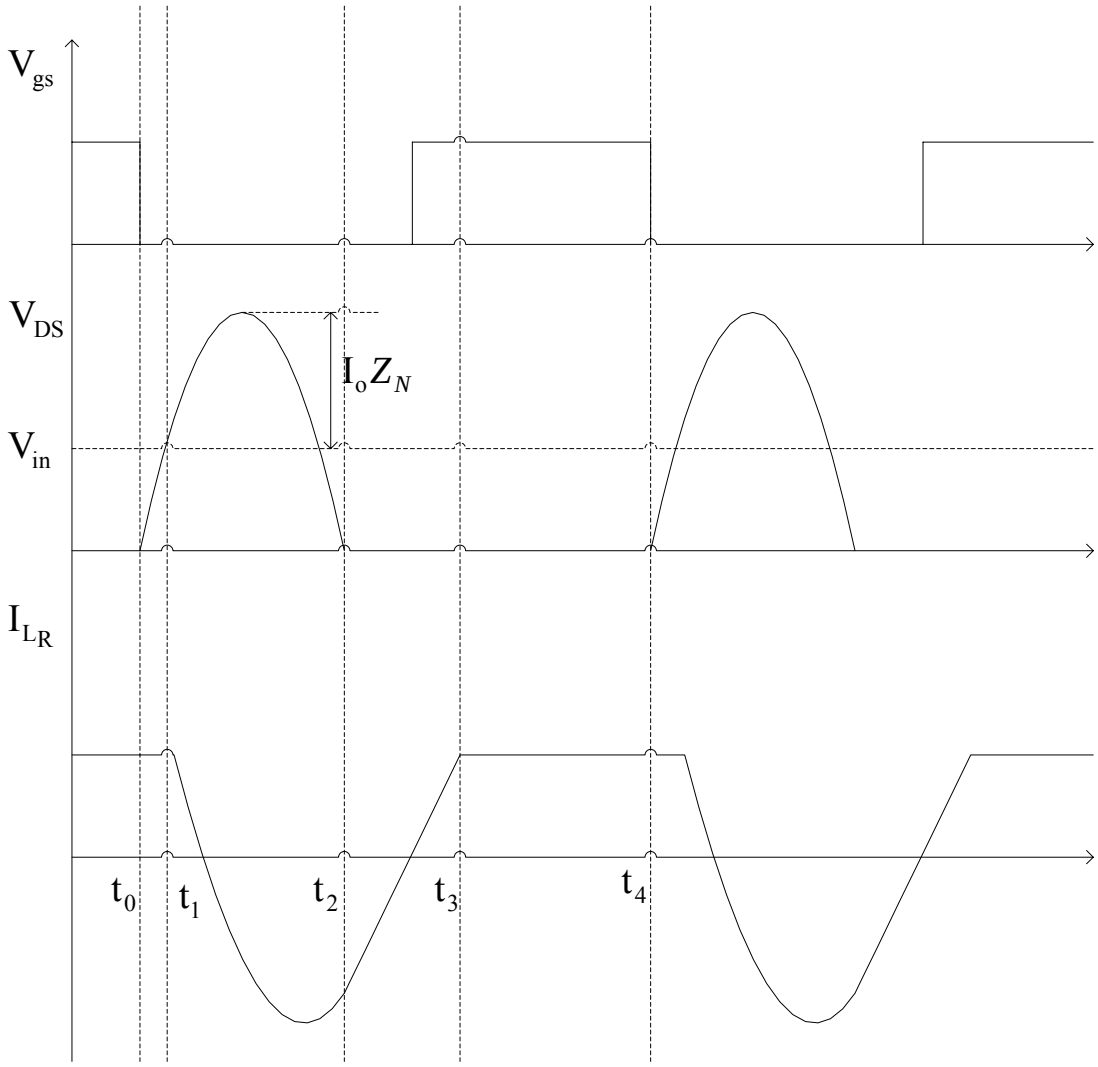


Figure 6.3 Typical waveforms of half-wave ZVS QR buck converter.

The resonant action of C_R and L_R causes V_{DS} to decrease to zero at t_2.

$$I_{LR}(t) = I_0 \cos wt \tag{6.8}$$

$$V_{DS}(t) = V_{in} + I_0 Z_N \sin wt \tag{6.9}$$

$$T_{12} = \frac{\alpha}{w} \tag{6.10}$$

where

$$\alpha = \begin{cases} \pi + \arcsin\left(\frac{V_{in}}{Z_N I_0}\right) \text{ for half-wave mode } t_2 = T_a \\ 2\pi - \arcsin\left(\frac{V_{in}}{Z_N I_0}\right) \text{ for full-wave mode } t_2 = T_b \end{cases} \tag{6.11}$$

6.2.3 Inductor-Charging Stage (t_2-t_3)

When V_{DS} reaches zero, the anti-parallel diode turns on. Now the resonant capacitor is shorted and the input voltage is applied to L_R. Therefore, the current I_{LR} starts increasing linearly until it reaches the value of the output current.

$$T_{23} = \frac{1}{w}\frac{Z_N I_0}{V_{in}}(1 - \cos\alpha) \tag{6.12}$$

6.2.4 Free-Wheeling Stage (t_3-t_4)

At this moment, diode D_0 turns off. During this interval, active switch S conducts the output current. The duration of this interval is a control parameter and is determined by:

$$T_{34} = T_S - T_{01} - T_{12} - T_{23} \tag{6.13}$$

where T_S is the period of a switching cycle.

A condition for achieving zero-voltage switching in the ZVS quasi-resonant buck converter is:

$$r \le M \tag{6.14}$$

The steady-state characteristics can be obtained by solving the state equations of the four stages in a switching cycle. The dc voltage conversion ratio, V_0/V_i, as a function of the load resistance and the switching frequency, can be derived by equating the input energy per cycle E_i, and the output energy per cycle, E_0.

The expression for conversion ratio of a buck ZVS QRC can be derived by the method described above:

$$M = \frac{V_0}{V_{in}} = 1 - \frac{f_S}{2\pi f_R}\left[\alpha + \frac{r}{2M} + \frac{M}{r}\left(1 - \cos\alpha\right)\right] \tag{6.15}$$

where

$$\alpha = \pi + \arcsin\left(\frac{r}{M}\right) \text{ for half-wave mode} \tag{6.16}$$

$$\alpha = 2\pi - \arcsin\left(\frac{r}{M}\right) \text{ for full-wave mode.} \tag{6.17}$$

Peak voltage on the power switch and peak current in output diode occur during resonance. The solutions of four topological modes result in the following peak values

of voltage and current:

$$\frac{V_{DS-pk}}{V_0} = \frac{1}{M}\left(1+\frac{M}{r}\right) \tag{6.18}$$

$$\frac{I_{SW-pk}}{I_0} = 1 \tag{6.19}$$

$$\frac{V_{D-pk}}{V_0} = \frac{1}{M} \tag{6.20}$$

$$\frac{I_{D-pk}}{I_0} = 2 \tag{6.21}$$

6.3 Components of the Experimental System

The user can see the performance of a dc-dc converter circuit with or without soft-switching technique and can discuss the operation of zero-voltage switching quasi-resonant technique and important waveforms.

6.3.1 DC Power Supply Circuit for ICs

Power supply circuit is designed to start up the integrated circuits for the experiments. Three different transformers (five-output 12-0-12 and 9-0, a three-output 15-0-15 and a three-output 12-0-12) are used to obtain different low power dc voltages from the mains. The input and output connections are made by connectors. The different voltage outputs of this circuit provide the inputs to the buck converter unit. Low power dc supply circuit

PCB layout and detailed circuit schematic are shown in Figures 6.4 and 6.5 respectively. The component list is given in Table 6.1.

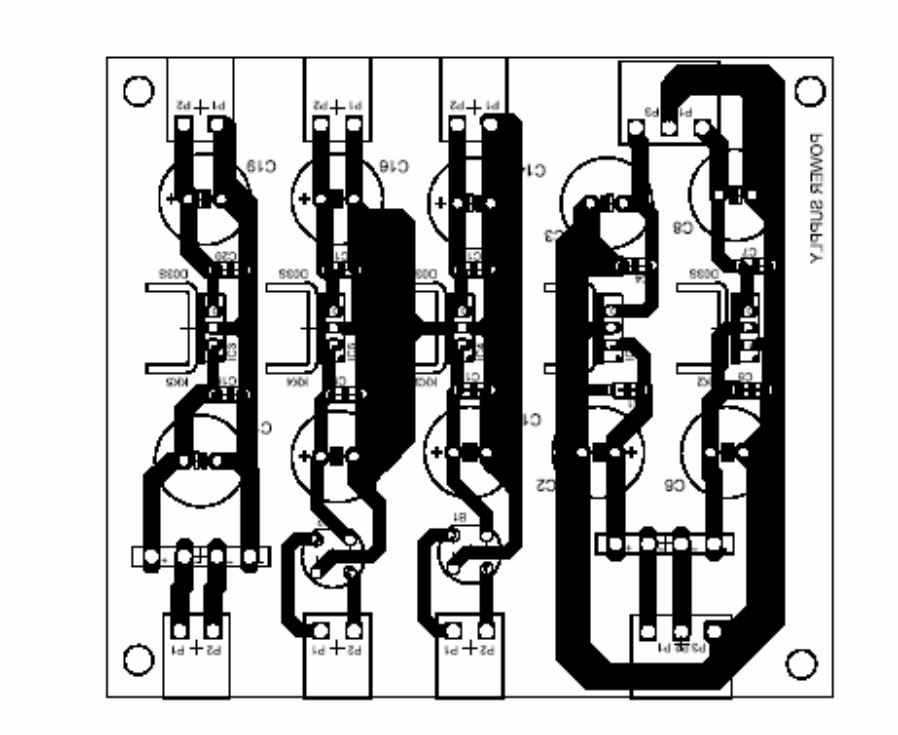


Figure 6.4 Power supply circuit PCB layout (bottom layer).

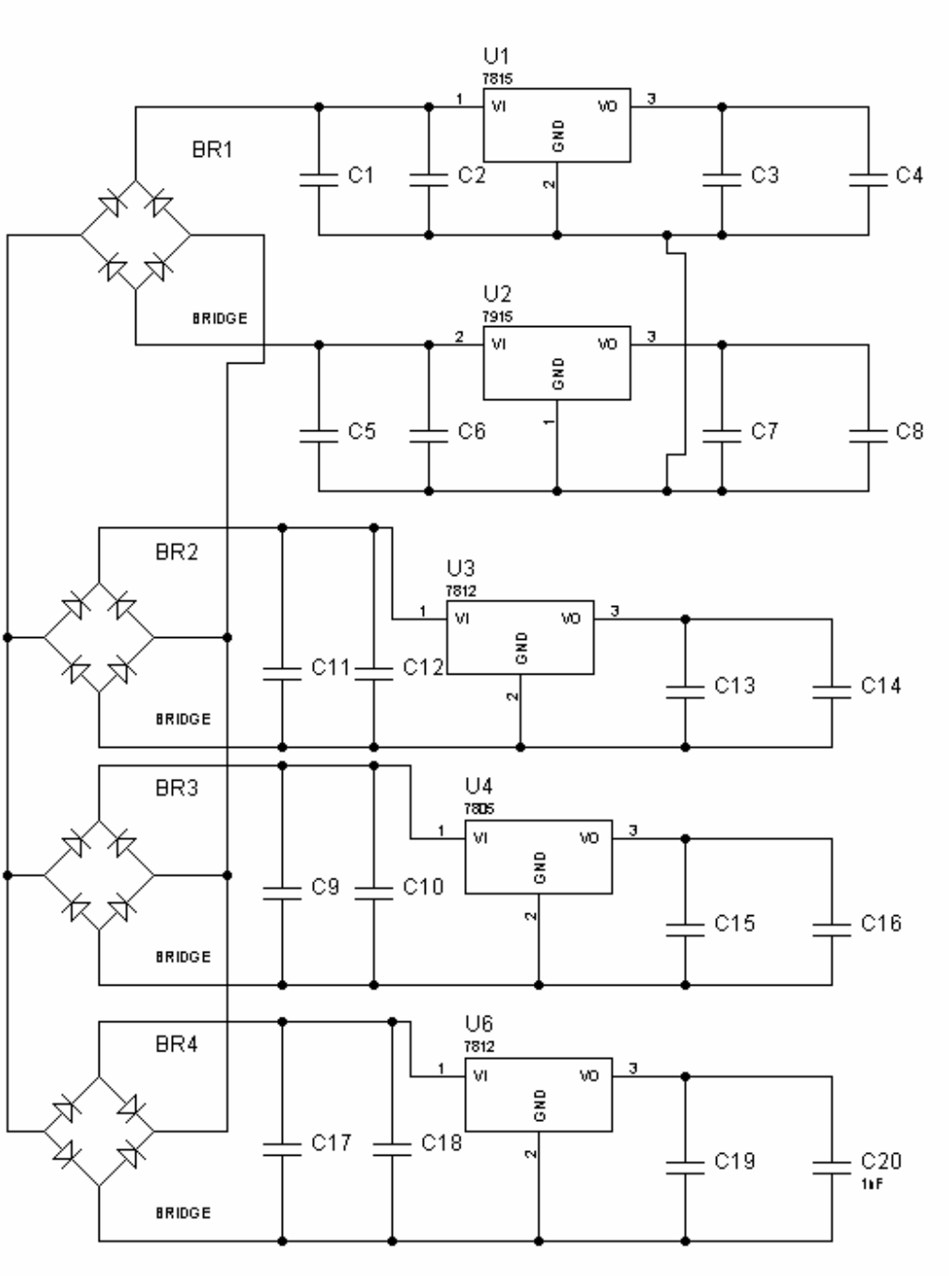


Figure 6.5 Schematic diagram of power supply circuit.

Table 6.1 Bill of materials

	Reference	Qty	DESCRIPTION	Part Number - Manufacturer
Capacitors	C1	1	100 nF, multilayer	
	C2	1	1000 µF, 25 V, electronic	
	C3	1	330 µF, 50 V, electronic	
	C4	1	100 nF, multilayer	
	C5	1	100 nF, multilayer	
	C6	1	1000 µF, 25 V, electronic	
	C7	1	100 nF, multilayer	
	C8	1	330 µF, 50 V, ,electronic	
	C9	1	100 nF, multilayer	
	C10	1	1000 µF, 25 V, electronic	
	C11	1	100 nF, multilayer	
	C12	1	1000 µF, 25 V, electronic	
	C13	1	100 nF, multilayer	
	C14	1	330 µF, 50 V, electronic	
	C15	1	100 nF, multilayer	
	C16	1	330 µF, 50 V, electronic	
	C17	1	1000 µF, 25 V, electronic	
	C18	1	100 nF, multilayer	
	C19	1	330 µF, 50 V, electronic	
	C20	1	100 nF, multilayer	
Diodes	D1	2	8 A, 600 V, bridge	
	D2	2	8 A, 600 V, bridge	
IC's	U1	1	15 V Regulator IC	L7815
	U2	1	-15 V Regulator IC	L7915
	U3	1	12 V Regulator IC	L7812
	U4	1	12 V Regulator IC	L7812
	U5	1	5 V Regulator IC	L7805

6.3.2 PWM and ZVS Quasi-Resonant Buck Converter

The PWM and ZVS quasi-resonant buck converter is designed to be used in the experiments. The user should combine the low power dc supply circuit as an input and a resistive load as an output. Both open-loop and closed-loop operations are performed with this circuit. The two switches are used to pass from open-loop operation to closed-loop operation or vice versa. The other connections (dc power supply, load and measurement points) are made by connectors. The varying frequency is achieved by the potentiometer for open-loop operations. The switching frequencies between 50 kHz and 100 kHz are available in eleven discrete steps. The off-time duration of the gate signals are fixed at 4.5 μs and the on-time duration varies with the switching frequency for open-loop operation. The rheostat can be used as a varying resistive load for both open-loop and closed-loop operations. The circuit PCB layout for bottom and top views and detailed circuit schematic are shown in Figures 6.6, Figure 6.7 and Figure 6.8 respectively. The component list is given in Table 6.2. The circuit specifications are given in Table 6.3.

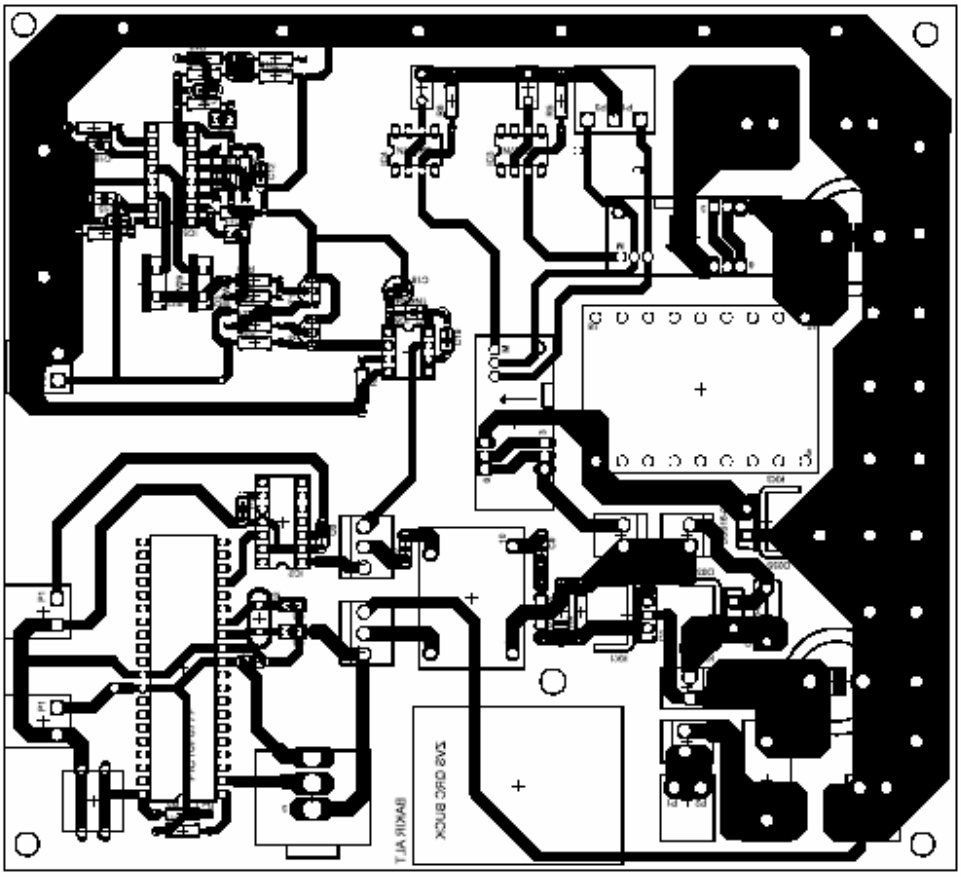


Figure 6.6 PCB layout (bottom view).

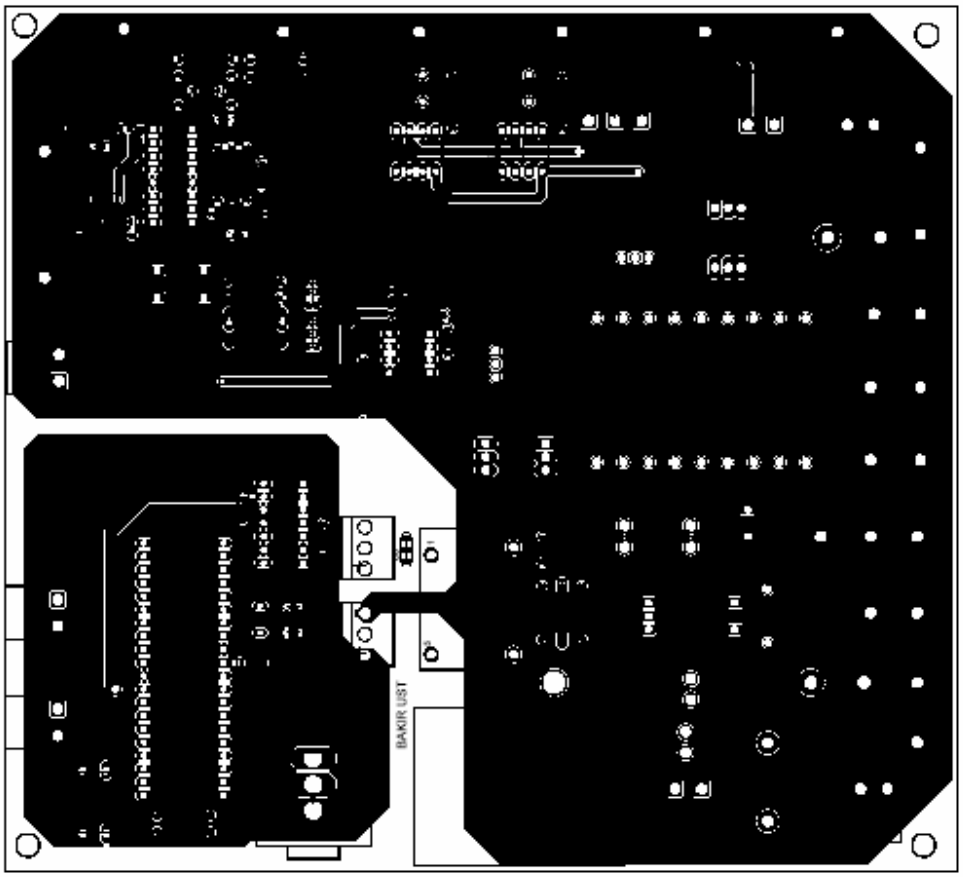


Figure 6.7 PCB layout (top view).

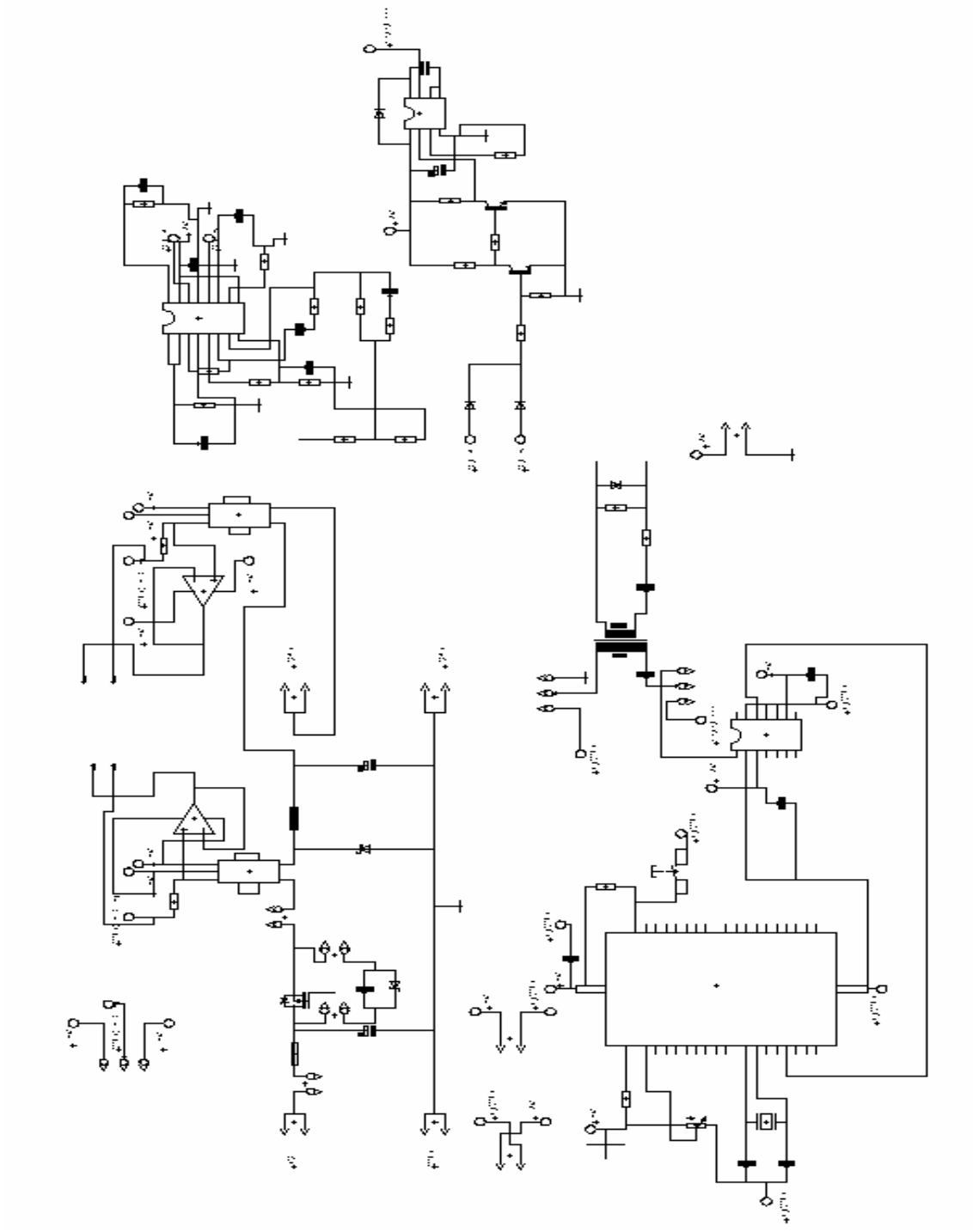


Figure 6.8 Schematic diagram of buck converter.

Table 6.2 Bill of materials

	Reference	Qty	DESCRIPTION	Part Number - Manufacturer
Capacitors	C1	1	100 µF, 400 V, electronic	SAMSUNG
	C2	1	22 nF, 600 V	
	C3	1	22 pF, ceramic	
	C4	1	220 µF, 400 V, electronic	
	C5	1	22 pF, 50 V, ceramic	
	C6	1	100 nF, multilayer	
	C7	1	100 nF, multilayer	
	C8	1	100 nF, multilayer	
	C9	1	100 nF, multilayer	
	C10	1	100 nF, multilayer	
	C11	1	10 nF, ceramic	
	C12	1	100 nF, multilayer	
	C13	1	10 nF, ceramic	
	C14	1	2.2 nF, ceramic	
	C15	1	100 nF, multilayer	
	C16	1	10 nF, ceramic	
	C17	1	4.7 nF, ceramic	
	C18	1	4.7 µF, 25 V, electronic	
	C19	1	100 nF, multilayer	
Diodes	D1	1	15 V, 1W, zener	
	D2	1	8 A, 100 V, ultrafast	BYW29-100
	D3	1	8 A, 100 V, ultrafast	BYW29-100
	D4	1	1 A, 1000 V,silicon	1N4007
	D5	1	16 A, 100 V, schottky	DSS16-01A
	D6	1	8 A, 200 V, ultrafast	BYW29-200
Fuses	F1	1	3 A, 250 V glass fast acting type	
Inductors	L1	1	160 µH, buck filter inductor	
	L2	1	25.6 µH, resonant inductor	
MOSFETs	Q1	1	500 V, 8 A	IRF840
Resistors	R1, R2	1	10 kΩ, 1/4 W	
	R3	1	10 Ω, 1/4 W	
	R4	1	10 kΩ, 1/4 W	
	R5, R6	1	332 Ω, 1/4 W	
	R7	1	15 kΩ, 1/4 W	
	R8	1	1.6 kΩ, 1/4 W	
	R9	1	10 kΩ, 1/4 W	
	R10	1	9.6 kΩ, 1/4 W	
	R11	1	10 kΩ, 1/4 W	

Table 6.2 (continued)

	Reference	Qty	DESCRIPTION	Part Number - Manufacturer
Resistors	R12	1	80 kΩ, 1/4 W	
	R13	1	1 kΩ, 1/4 W	
	R14	1	20 kΩ, 1/4 W	
	R15	1	4 kΩ, 1/4 W	
	R16, R19	1	10 kΩ, 1/4 W	
	R17	1	4.7 kΩ, 1/4 W	
	R18, R20	1	4.7 kΩ, 1/4 W	
	R21	1	4.7 kΩ, 1/4 W	
	R22	1	560 Ω, 1/4 W	
	R23	1	10 kΩ, 1/4 W	
	R24	1	10 kΩ, pot	
Transducers	T1	2	LAH25-NP	LEM
Transformers	TR1	1	Gate drive transformer	Coilcraft SD250-1
ICs	U1	1	Microcontroller	Microchip PIC 16F877
	U2	1	High side, low side gate driver	IR2110
	U3,U4	1	Op-amp	LM307
	U5	1	Resonant mode controller	ON Semiconductor MC34067
	U6	1	High side driver	IR2125

The following experiment can be carried out by using the experimental system and measurement devices.

- Observing waveforms for input current, output current, output voltage, MOSFET drain-source voltage and output diode voltage for PWM buck converter.
- Obtaining waveforms for resonant inductor current, output current, output voltage MOSFET drain-source voltage and output diode voltage for ZVS QR buck converter.
- Start-up response and transient response.

Table 6.3 The specifications of the half-wave zero-voltage switching quasi-resonant buck converter

Input Voltage	20 V-30 V
Load	5 Ω-15 Ω
Inductor	160 μH
Output Capacitor	220 μF
Input Capacitor	100 μF
Resonant Capacitor	22 nF
Resonant Inductor	25.6 μH
Operation Frequency	20 kHz - 100 kHz
Resonant Frequency	200 kHz

6.4 Required Measurement Equipment

The following measurement and test equipment is required to maintain the experiments related to power factor correction.

- DC Voltmeter, min 600V DC
- DC ampermeter, min 10 A DC
- Wattmeter
- 2-channel, 80MHz, digital storage oscilloscope with higher sampling rate
- Differential voltage probes
- Connection cables

6.5 Experiment 1 – Switching Characteristics of the PWM Buck Converter

6.5.1 Introduction

The experiment is intended to illustrate the basic switching behaviors of the PWM buck converter operating under open-loop conditions. The PWM converters are widely used in today's power electronics industry, particularly in low-power application due to circuit simplicity and ease of control. However, the detrimental effects of the switching loss and EMI are more pronounced especially at high switching frequencies.

In this experiment, the turn-on and turn-off characteristics of the MOSFET at different switching frequencies will be analyzed. Also input current and the output diode voltage will be observed. The frequency of oscillations on MOSFET and diode voltage waveforms will be calculated.

For this demonstration, low power supply circuit, a dc power supply and a PWM and ZVS quasi-resonant buck units will be used. The resonant capacitor and the diode connection terminals of the buck converter will be opened and the resonant inductor

connection terminals will be shorted. The open-loop/closed-loop switches should be in open-loop position. The potentiometer will be used to adjust the frequency of the gate signals. Switching characteristics of the MOSFET and the output diode will be analyzed by oscilloscope with differential voltage probe.

6.5.2 Procedure

1. Connect the dc power supply to the input terminals of the PWM buck converter unit. Take the open-loop/closed-loop switches to OPEN-LOOP position. Make the connections between the low power dc supply and PWM buck converter unit shown in Figure 6.9.

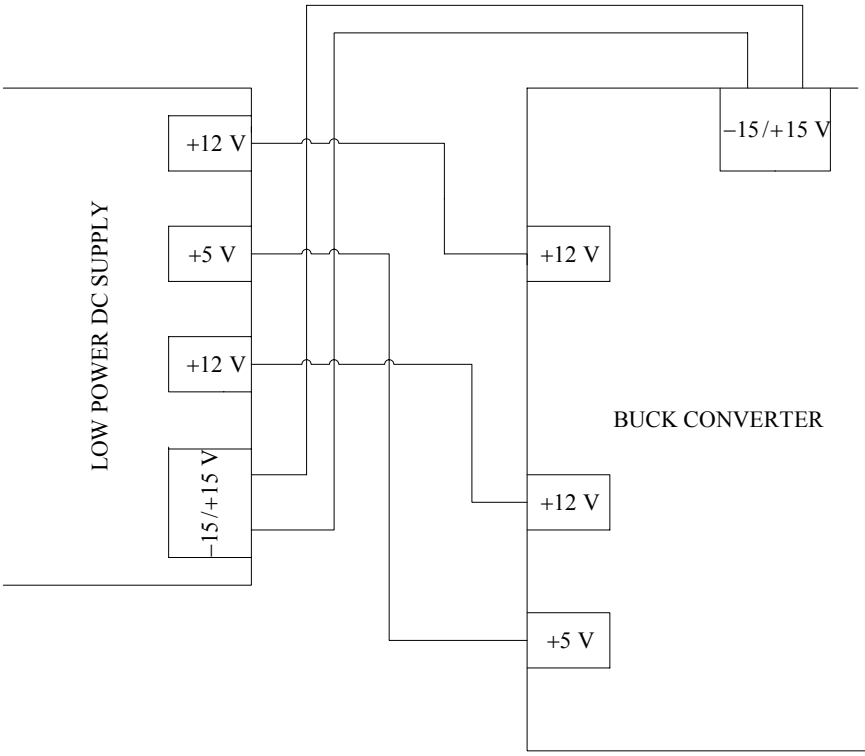


Figure 6.9 Open-loop buck converter and low power dc power supply connections.

2. Make the required connections with the following experiment parameters. Complete the connection diagram of the circuit shown in Figure 6.10.

Table 6.4 PWM buck converter experiment parameters.

Input Voltage	20 V
Switching Frequency	50 kHz
R load	10 Ω

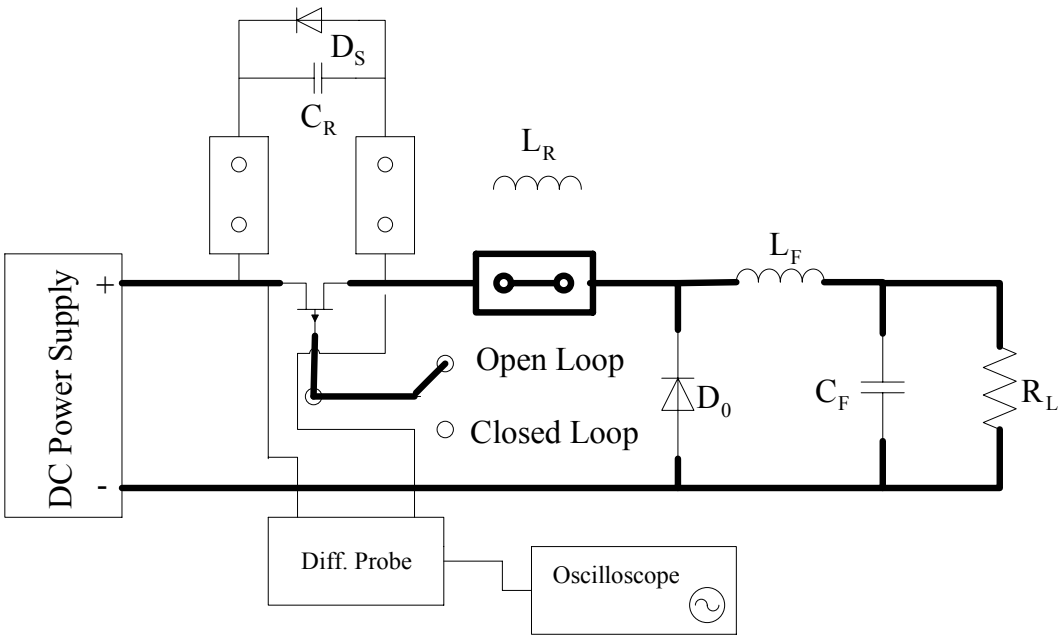


Figure 6.10 Circuit connections of PWM buck converter.

3. Connect the plug of the low power dc supply circuit to the mains and turn on the power switch of the dc power supply. Observe the MOSFET drain-source voltage waveform in the oscilloscope screen. If you see any oscillations, calculate the oscillation frequencies. The measured waveform is illustrated in Figure 6.11.

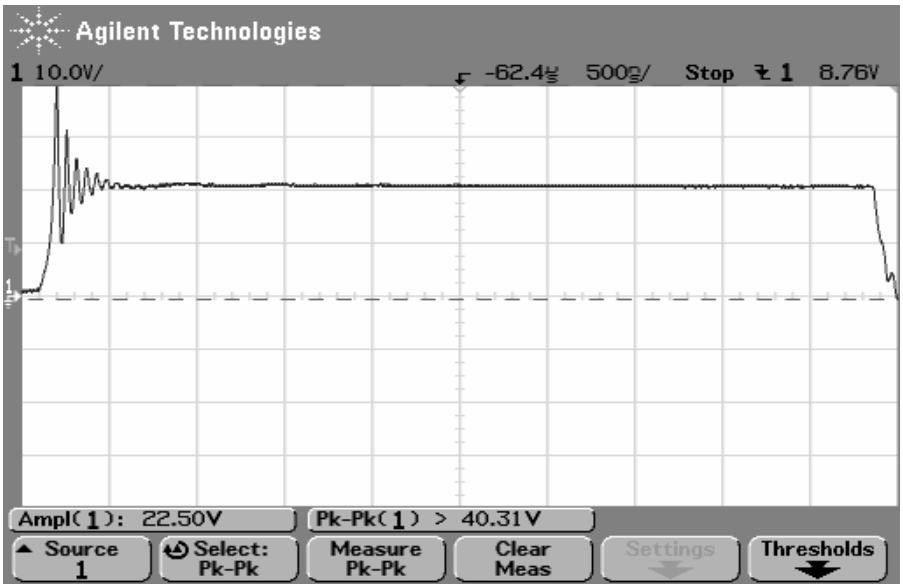


Figure 6.11 MOSFET drain-source voltage (scales: 10 V/div, 500 ns/div).

4. Connect the probe to MOSFET current measurement pins and observe the switch current and voltage waveforms while the differential probe is connected to the power MOSFET's Drain and Source. Focus on the turn-on and turn-off conditions. The measured waveform is illustrated in Figure 6.12, Figure 6.13 and Figure 6.14 respectively.

5. Connect the differential probe to the output diode of the PWM buck converter. If you see any oscillations on the voltage waveforms, calculate the oscillation frequencies. The measured waveform is illustrated in Figure 6.15.

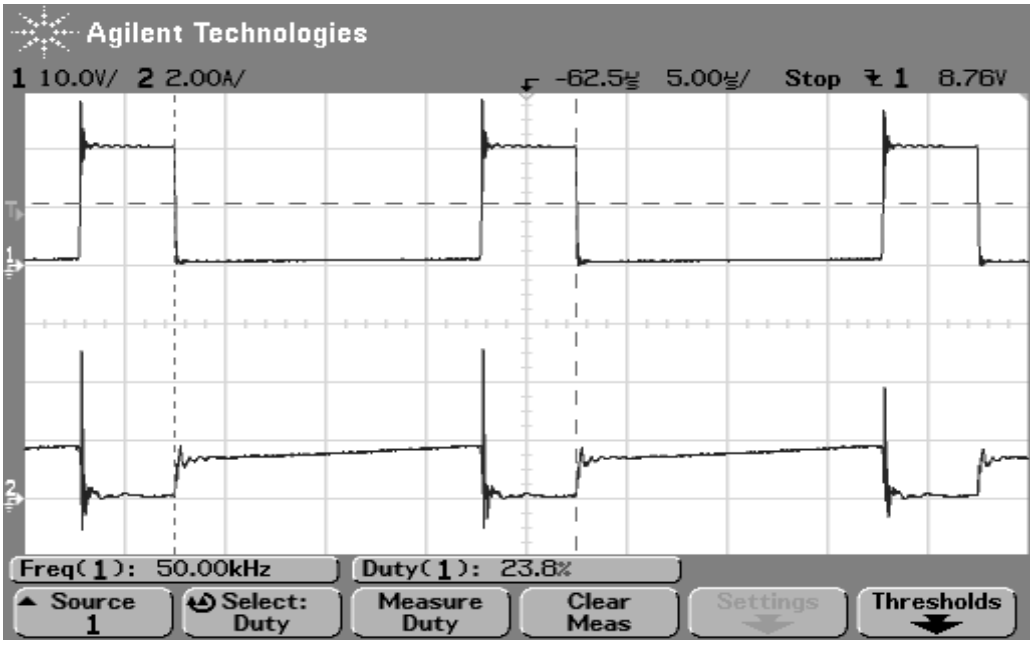


Figure 6.12 MOSFET current and voltage waveforms (The upper is switch voltage and the lower is switch current) (scales: 10 V/div, 2 A/div and 5 µs/div).

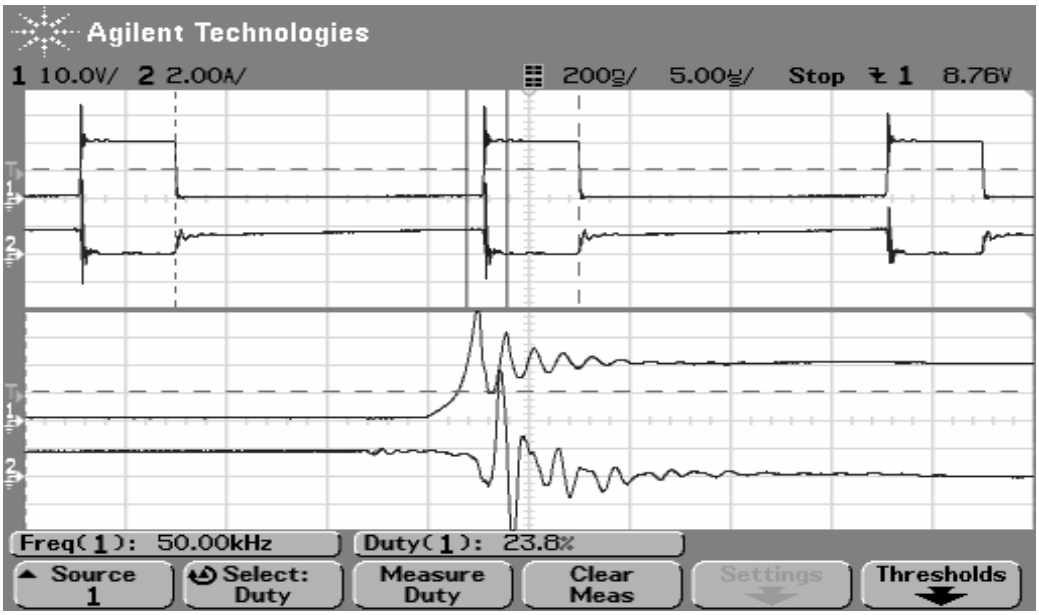


Figure 6.13 MOSFET turn-off characteristics (The upper is switch voltage and the lower is switch current for both views) (scales: 10 V/div, 2 A/div and 5 µs/div).

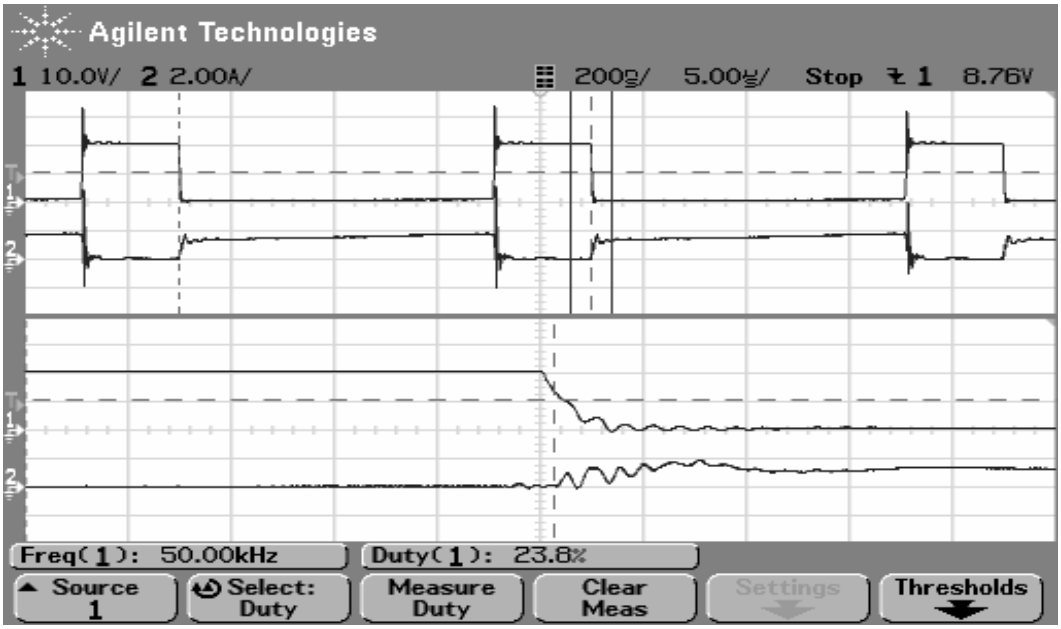


Figure 6.14 MOSFET turn-on characteristics (The upper is switch voltage and the lower is switch current for both views) (scales: 10 V/div, 2 A/div and 5 µs/div).

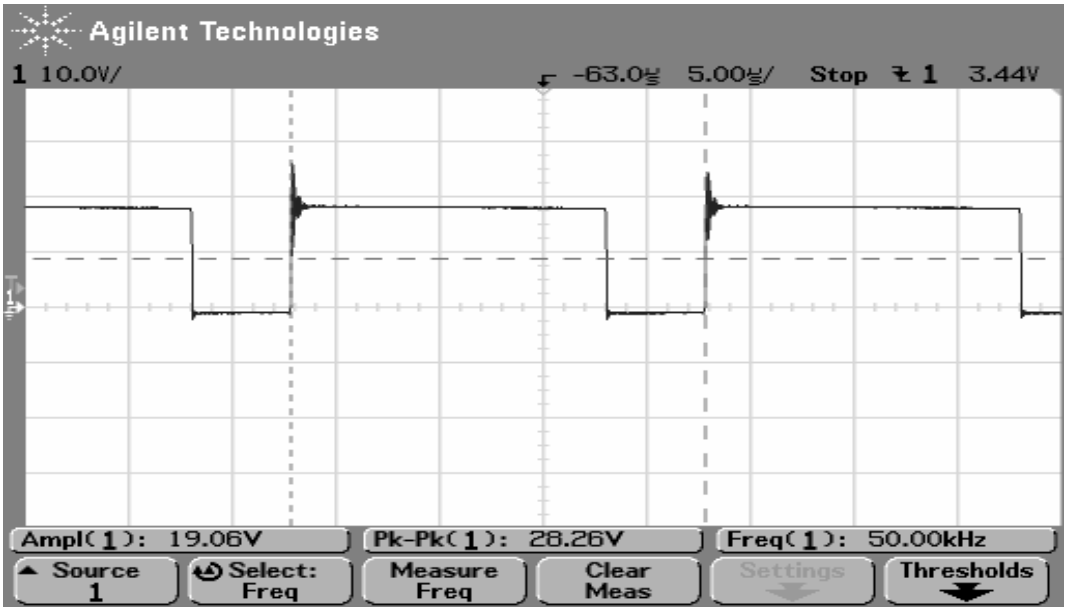


Figure 6.15 Output diode voltage waveform (scales: 10 V/div, 5 µs/div).

6.5.3 Study Questions

1. Discuss the reason of the oscillations on the MOSFET voltage waveform. Which factors can affect the oscillation frequency? Explain briefly.

2. Assuming that your PWM buck converter contains a slow silicon diode. Write a few sentences that should explain: (1) why it takes time to switch off the diode, and (2) how the diode induces switching loss in the MOSFET. You may assume that the MOSFET switching times are much shorter than the diode reverse recovery time.

3. Comment on the oscillations on the output diode voltage waveform.

6.6 Experiment 2 – Component and Converter Based Characteristics of the ZVS Quasi-Resonant Buck Converter

6.6.1 Introduction

In this experiment, quasi-resonant soft-switching technique is analyzed. A resonant network consisting of an inductor and a capacitor is connected to the active switch in order to shape the switch voltage into a quasi-sinusoidal form. Therefore, the switching action occurs when the switch voltage drops to zero (i.e. zero-voltage switching). The switching losses and EMI are reduced, thus higher switching frequencies up to 1 MHz can now be available with this technique.

In this experiment, turn-on and turn-off characteristics of the MOSFET operating under zero-voltage switching conditions will be analyzed. Also resonant inductor current and output diode voltage waveforms will be observed. The load and frequency dependency of the resonant capacitor voltage (MOSFET drain-source voltage) will be discussed.

Also maximum load resistor values the converter has still zero-voltage switching property will be found.

6.6.2 Procedure

1. Connect the dc power supply to the input terminals of the buck converter unit. Take the open-loop/closed-loop switches to OPEN-LOOP position. Make again the connections between the low power dc supply and buck converter unit shown in Figure 6.9.

2. Make the required connections with the following experiment parameters. Complete connection diagram of the circuit is illustrated in Figure 6.16. The experiment parameters are summarized in Table 6.5.

Table 6.5 ZVS quasi-resonant buck converter experiment parameters

Input Voltage	20 V
Switching frequency	50 kHz
R load	10 Ω
Resonant Inductance	25.6 μH
Resonant Capacitor	22 nF

3. Connect the plug of the low power dc supply circuit to the mains and turn on the power switch of the dc power supply. Observe the MOSFET drain-source voltage waveform in the oscilloscope screen while the other probe is connected to the command signal. Observe the turn-on and turn-off characteristics. The measured waveform is illustrated in Figure 6.17.

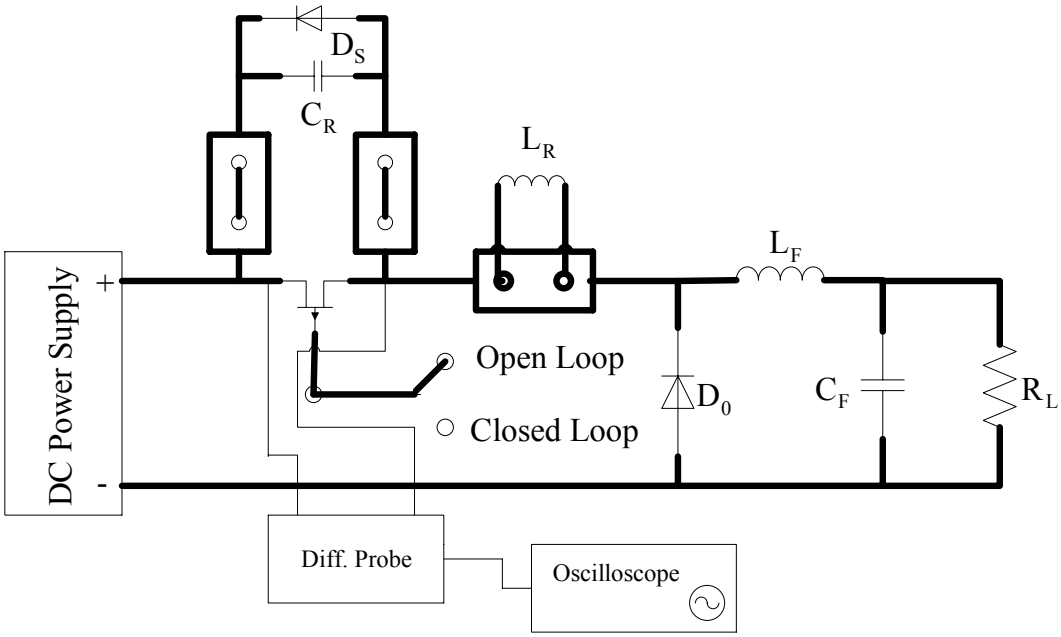


Figure 6.16 Circuit connections of open-loop ZVS quasi-resonant buck converter.

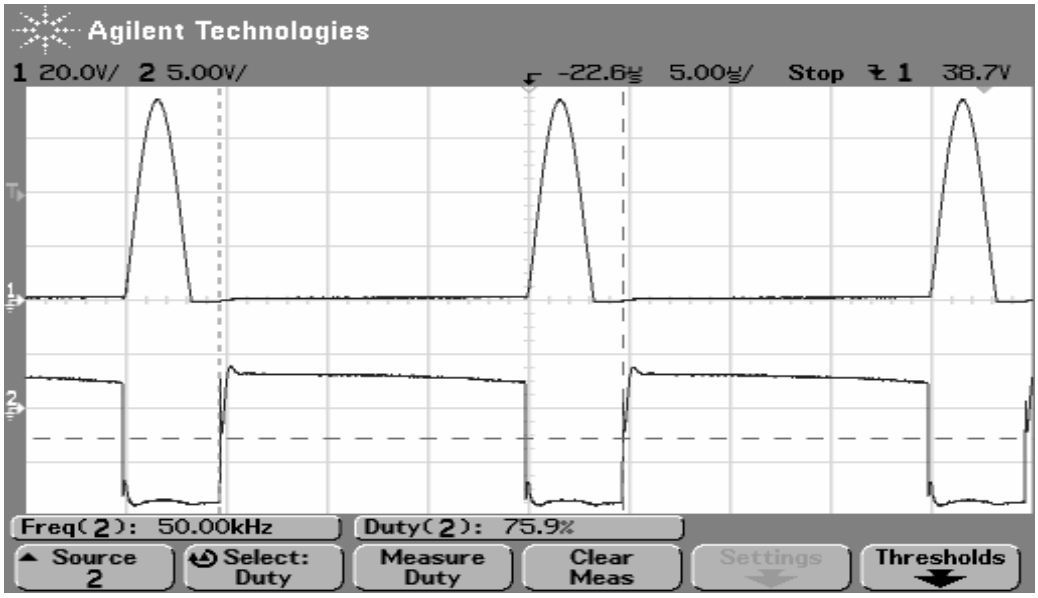


Figure 6.17 MOSFET turn-on and turn-off characteristics (the upper is switch voltage, the lower is command signal) (scales: 20 V/div, 5 V/div and 5 μs/div).

4. Connect the differential probe to the resonant inductor current measurement pins while the other differential probe is connected to the voltage across the switch. Observe and match the results with the theoretical waveforms of ZVS quasi-resonant buck converter. The measured waveform is illustrated in Figure 6.18.

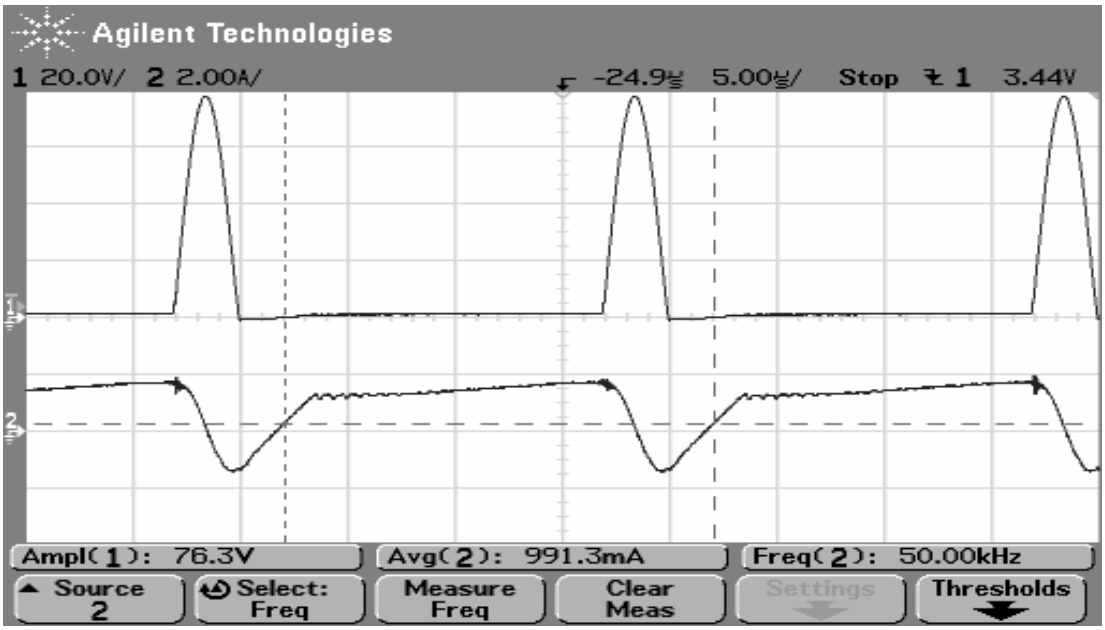


Figure 6.18 Resonant capacitor voltage and resonant inductor current (the upper is capacitor voltage, the lower is inductor current) (scales: 20 V/div, 2 A/div and 5 μs/div).

5. Connect the differential probe to Cathode and Anode of the output diode. Observe the output diode characteristics. If you see any oscillations on the voltage waveforms, calculate the oscillation frequencies. The measured waveform is illustrated in Figure 6.19.

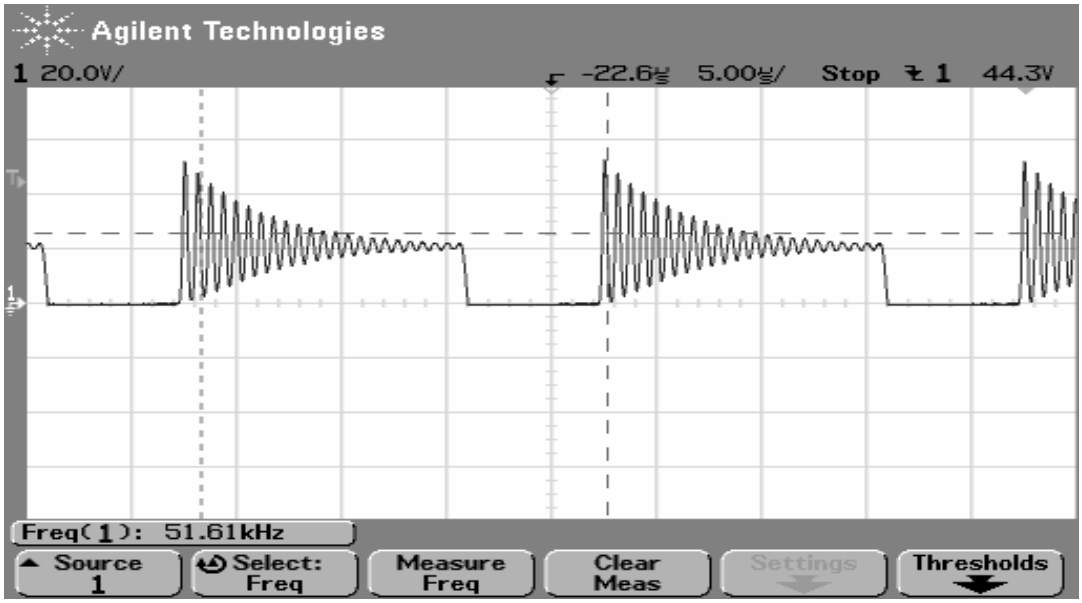


Figure 6.19 Output diode voltage waveform (scales: 20 V/div, 5 μs/div).

6. Connect the differential probe to Drain and Source of the power MOSFET and the other probe to the current measurement pins. Set the potentiometer in order to have 71.5 kHz command signals. Increase the load value in steps up to the maximum load (5 Ω – 15 Ω), observe the voltage waveform across the switch for all the load levels. Tabulate the amplitude of the resonant capacitor voltage with the load values. The measured values for different load levels are shown in Figure 6.20 and 6.21. Then increase the resistor beyond the maximum resistor at the output to obtain maximum load resistance the converter has still zero-voltage switching property. The measured waveform is illustrated in Figure 6.22.

7. Adjust the rheostat to obtain 10 Ω of load resistance at the output. Increase the input voltage in steps up to maximum input voltage level, observe and sketch the voltage waveforms across the switch. Note all the data.

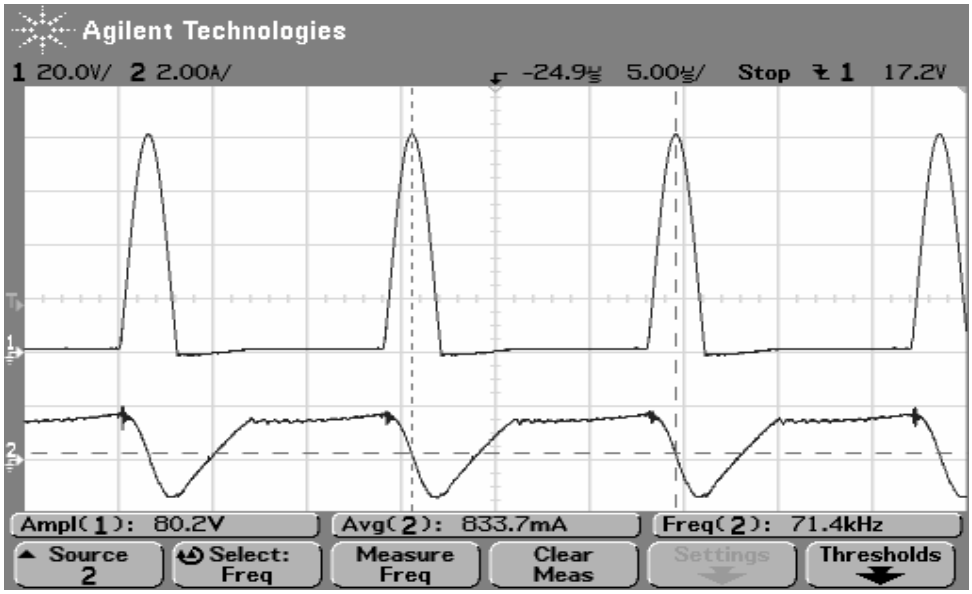


Figure 6.20 Resonant capacitor voltage and resonant inductor current at 5 Ω (the upper is capacitor voltage, the lower is inductor current)
(scales: 20 V/div, 2 A/div and 5 µs/div).

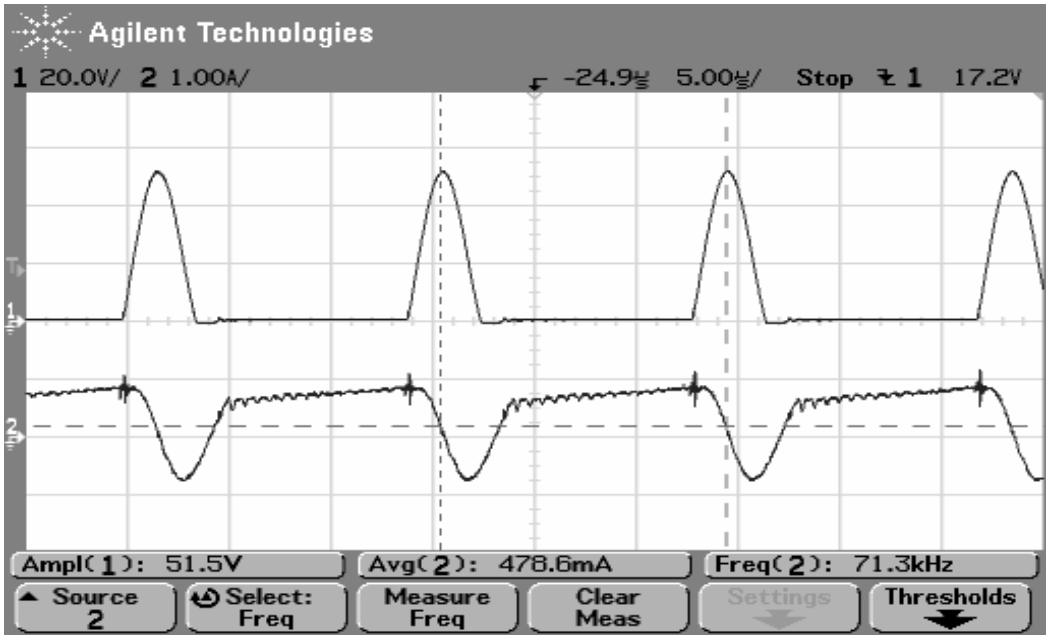


Figure 6.21 Resonant capacitor voltage and resonant inductor current at 15 Ω (the upper is capacitor voltage, the lower is inductor current)
(scales: 20 V/div, 1 A/div and 5 µs/div).

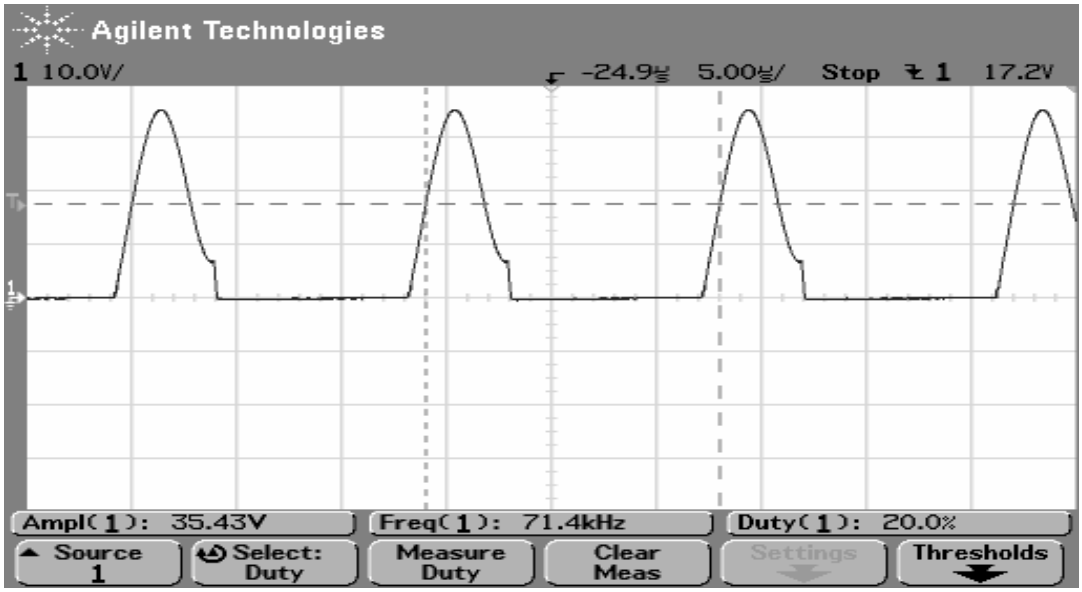


Figure 6.22 Resonant capacitor voltage at 40 Ω (scales: 10 V/div, 5 μs/div).

8. Adjust the resistance of rheostat to 10 Ω. Adjust the input voltage to 24 V. Connect the probe to the output terminals of the converter. Increase the frequency command by turning the potentiometer in clockwise direction for all values of frequency. Observe the output voltage and plot the normalized output voltage characteristics ($M = V_0/V_{in}$) of the ZVS quasi-resonant buck converter versus the normalized frequency ($f_n = f_s/f_r$). Increase the resistance in steps up to the maximum load and repeat the same procedure as mentioned above for different load levels. The measured waveform is illustrated in Figure 6.23.

6.6.3 Study Questions

1. Why the oscillations increase on the output diode voltage waveform operating under zero-voltage switching quasi-resonant conditions according to the PWM buck converter? Explain briefly.

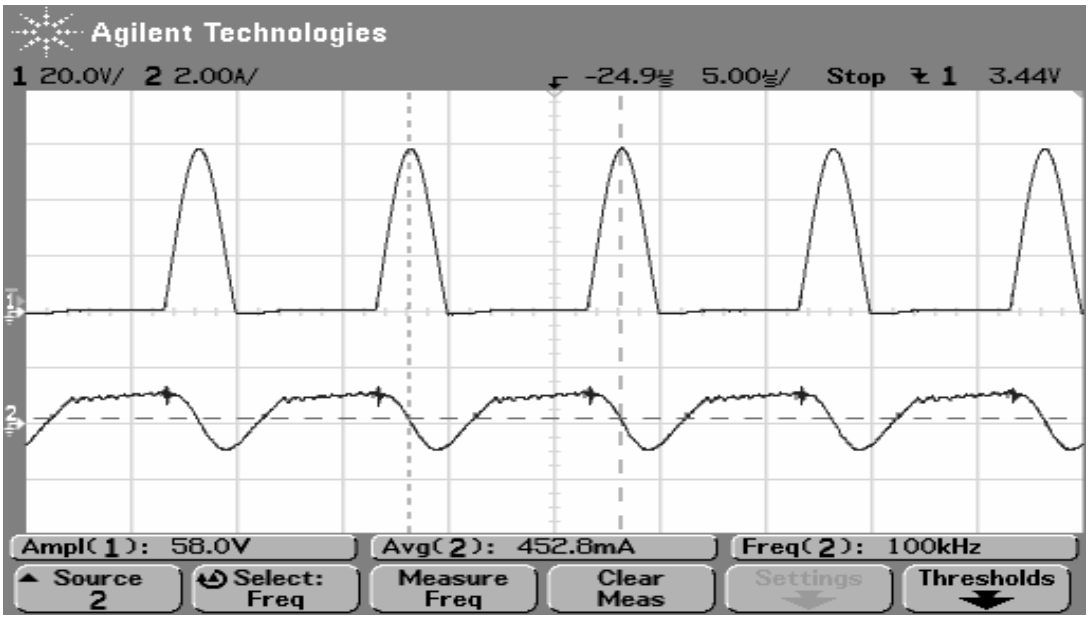


Figure 6.23 Resonant capacitor voltage and resonant inductor current at 100 kHz (the upper is capacitor voltage, the lower is inductor current)
(scales: 20 V/div, 2 A/div and 5 μs/div).

2. If you need to use an off-line converter (directly connected to the AC mains) operating under quasi-resonant technique, which type of quasi-resonant techniques is suitable for the off-line converters? Explain your reasoning.

3. What are the advantages and disadvantages of soft-switching solutions? Consider switching losses, operating frequency, manufacturing and total cost, size and weight.

6.7 Experiment 3 - Closed-Loop Characteristics of the ZVS Quasi-Resonant Buck Converter

6.7.1 Introduction

In this experiment, closed-loop performance of the ZVS quasi-resonant buck converter is analyzed. The quasi-resonant converters are controlled either fixed turn-on, variable turn-off times or fixed turn-off, variable turn-on times according to the quasi resonant technique. In order to regulate the output voltage, the operating frequency changes when changes occur in line voltage and load.

The output voltage is analyzed due to the immediate change in line voltage and load levels. The settling time and overshoot are calculated and discussed in a control manner. The overall performance of the closed-loop buck converter is investigated.

6.7.2 Procedure

1. Connect the dc power supply to the input terminals of the buck converter unit. Take the open-loop/closed-loop switches to CLOSED-LOOP position. Make again the connections between the low power dc supply and buck converter unit.

2. Make the required connections with the following experiment parameters. Complete connection diagram of the circuit is illustrated in Figure 6.24. The experiment parameters are summarized in Table 6.6.

Table 6.6 Closed-loop ZVS quasi-resonant buck converter experiment parameters

Power Supply 1	24 V
Power supply 2	30 V
R Load 1	12 Ω
R Load 2	12 Ω
Resonant Inductance	25.6 μH
Resonant Capacitor	22 nF

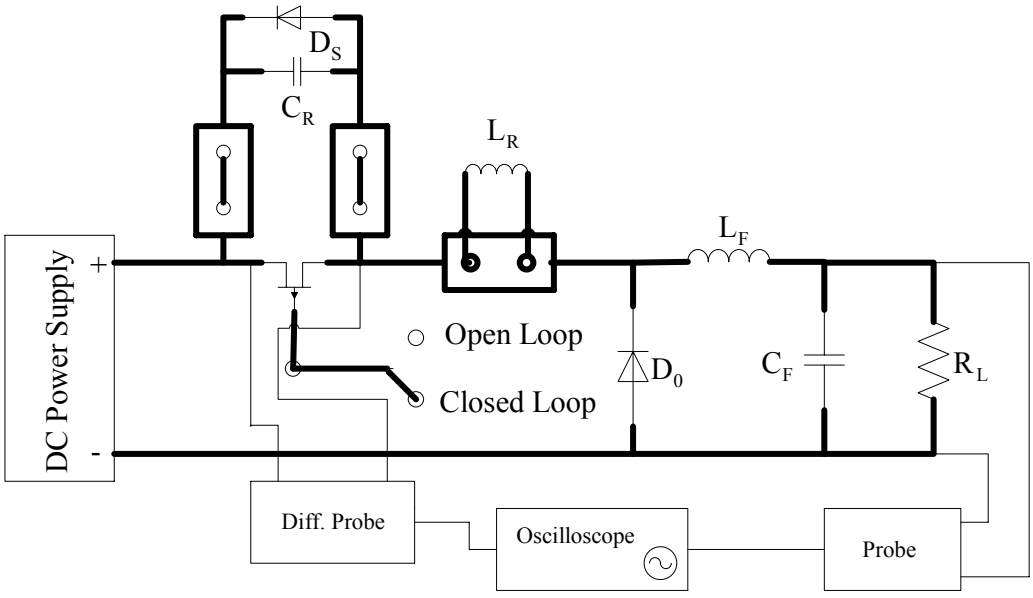


Figure 6.24 Circuit connections of closed-loop ZVS quasi-resonant buck converter.

3. Connect the plug of the low power dc supply circuit to the mains and turn on the power switch of the dc power supply. Make the connections of the overall system shown in Figure 6.25 for load regulation test.

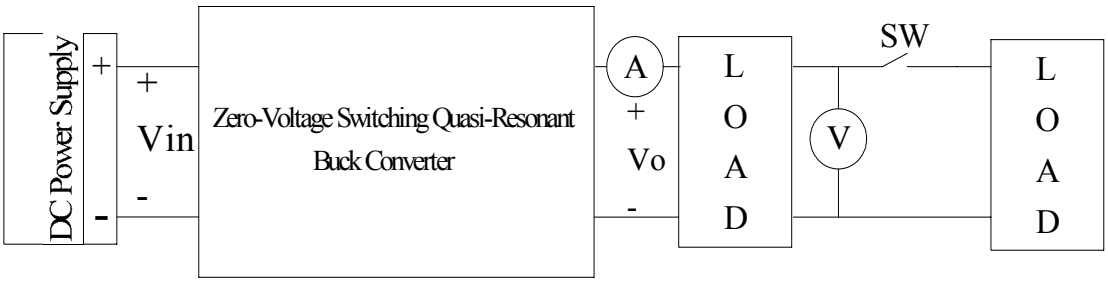


Figure 6.25 Load connections for load regulation closed-loop test.

4. Connect the probe to the output terminals of the converter. Turn the system on. Make sure that the output voltage is 15 V. Close the switch to change the output load and observe the output voltage transient by using an oscilloscope. Save the oscilloscope result and determine the settling time and overshoot of the output voltage. For this time, open the switch to halve the output load and observe the output voltage transient by using an oscilloscope. Again, save the oscilloscope result and determine the settling time and overshoot of the output voltage. The measured waveforms are illustrated in Figure 6.26 and Figure 6.27 respectively.

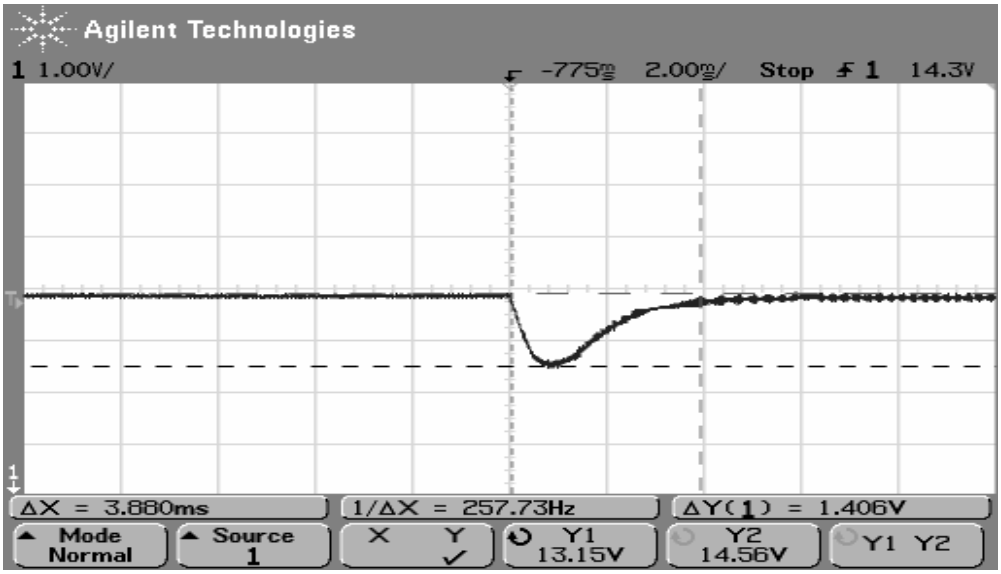


Figure 6.26 Output voltage waveform from half-load to full-load (scales: 1 V/div, 2 ms/div).

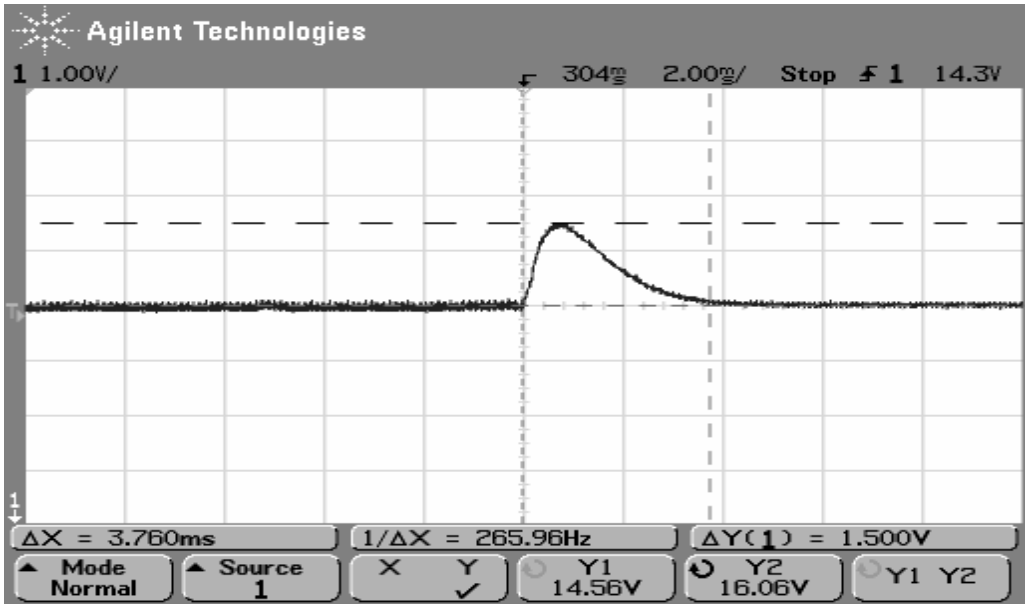


Figure 6.27 Output voltage waveform from full-load to half-load (scales: 1 V/div, 2 ms/div).

5. Make the connections of the circuit shown in Figure 6.28. Before starting, the power supplies should be turned off and the switch should be in position 1. Adjust the power supply-1 to 24 V DC and power supply-2 to 30 V DC. Make sure that they are turned off before starting. Switch on the DC supplies. Change the switch position from position 1 to position 2 quickly. Observe the output voltage transient by using an oscilloscope. Save the oscilloscope result and determine the settling time and overshoot of the output voltage. The measured waveform is illustrated in Figure 6.29.

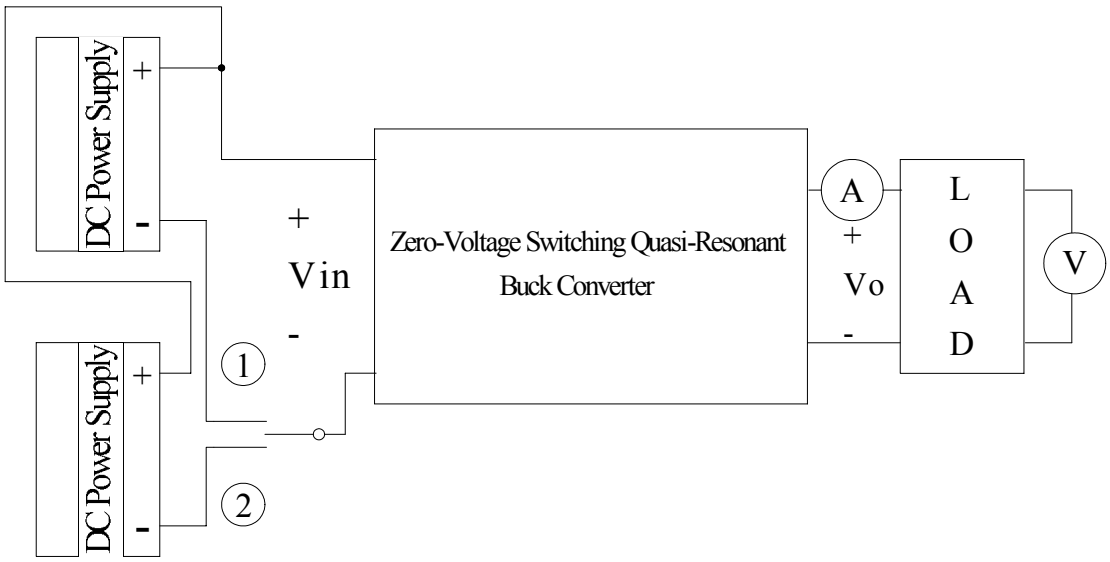


Figure 6.28 DC supply connections for line regulation closed-loop test.

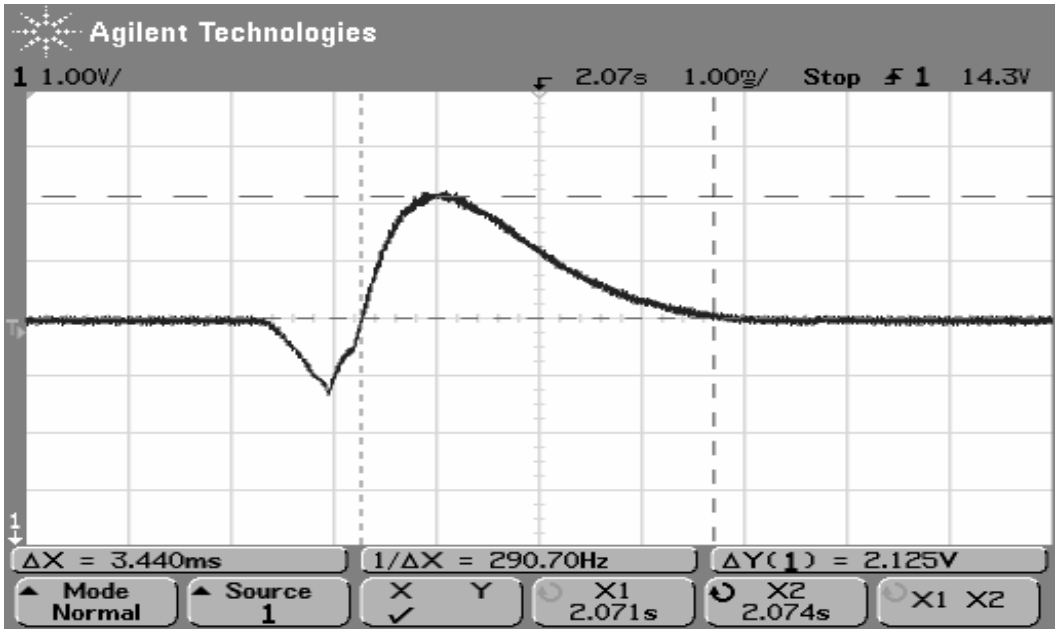


Figure 6.29 Output voltage waveform for line regulation
(scales: 1 V/div, 1 ms/div).

6.7.3 Study Questions

1. What are the other control methods for the quasi-resonant converters? Consider multi-loop control.

CHAPTER 7

CONCLUSIONS AND FURTHER WORK

7.1 Summary

In this thesis, conventional pulse-width modulated and quasi-resonant zero-voltage switching (ZVS) buck converters have been analyzed, simulated, designed and implemented. Both topologies are very important because they constitute the basic level of understanding the difference between switched-mode converters and resonant converters. Moreover, the basic quasi-resonant buck converter is the milestone to understand the resonant power conversion.

This thesis can be summarized as follows: In chapter 1, existing pulse-width modulated and quasi-resonant converters are briefly reviewed. Overall advantages and drawbacks of these converter topologies are summarized.

In chapters 2, 3, and 4, conventional PWM converters and quasi-resonant converters are reviewed in detail. The modes of operation of basic buck topology are presented for each of these topologies. The given key parameters are helpful for designing switch-mode power supply topologies. Furthermore, analysis of the quasi-resonant converter topology is discussed.

In chapter 5, design procedures for the two basic topologies are presented in detail. The overall hardware description, small-signal model and the controller IC parameters are also discussed in this chapter. Open-loop and closed-loop operations of the ZVS quasi-

resonant buck converter are reviewed. Furthermore, simulation and experimental results are obtained and presented. It can be seen throughout this chapter that most of the simulation and experimental results are in agreement. Two different topological examples are reviewed in this chapter.

In the last chapter, the educational experiment procedure is discussed. The experiment steps are explained in detail, and the throughout this procedure, the experiment is very instructive.

7.2 Conclusions and Comments

The following conclusions and comments can be made.

1. Especially the voltage across the MOSFET is made sinusoidal to have good switching conditions in ZVS quasi-resonant converters. The oscillations that are seen in conventional PWM converters are thus eliminated. The switching action occurs when the voltage across the switch is nearly zero. The switching losses and EMI are reduced by achieving zero-voltage switching.
2. The switching condition for the output diode is not favorable. The abrupt change in voltage when the diode current drops to zero, causes oscillations in the diode output voltage waveform. This condition is expected because ZVS technique has not been extended to the output diode in ZVS quasi-resonant converters. The current through the diode is in quasi-sinusoidal form (zero-current switching) and the voltage across the diode is oscillatory.
3. The voltage across the MOSFET in conventional PWM converters is oscillatory. The major parasitic inductances are package and lead inductances of semiconductor devices and stray inductances of the interconnections. Abrupt change in voltage across the MOSFET when the MOSFET is turned

off causes oscillations because of the resonance between parasitic inductances and the output diode of the MOSFET.

4. Half-wave ZVS quasi-resonant converters are load dependent. The voltage across the MOSFET changes with load variations. Wider the load range, larger the voltage in amplitude across the MOSFET. For example, if the load range is 10:1, the amplitude of the voltage across the MOSFET is approximately 11 times the input voltage. For this reason, the zero-voltage technique cannot be applied to off-line converters having wide load ranges. In dc-dc converters, the load is selected in a narrow range especially in low power applications, because on-state resistance increases with increasing maximum voltage rating. The optimal selection of the MOSFET becomes an important process.
5. The efficiency decreases with increasing load level (smaller load resistance), because the conduction losses are much more pronounced when the circulating RMS current increases. The efficiency increases until the value of minimum load. Another important thing happens when the load resistance increases beyond the maximum load resistance. The efficiency again decreases because of non-zero voltage switching condition for the MOSFET. The maximum resistance at which the converter still keeps its zero-voltage switching property is variable. This variation depends on the input voltage and the switching frequency of the converter. The minimum of the maximum load resistances is calculated and used throughout the thesis for the worst case as a design parameter when the input voltage and the switching frequency are at their maximum. But for different conditions, the maximum value of the load resistance is different.
6. The high side gate drive circuitry is very simple and efficient without any switching delay that occurs in high side driver ICs. Theoretically, the disadvantage of the gate drive circuitry is not to have high duty cycle ratios such as 80% or further. The coupling capacitors are inserted for wide duty ratios, as in the buck converter. The presence of the coupling capacitors

causes an increase in the negative bias during off-time and a decrease in turn-on voltage thus providing a reset voltage for the magnetizing inductance.

To obtain experimental results a laboratory prototype buck converter is built and tested with hard-switching and soft-switching techniques. The results obtained are compared with the results of the theoretical analysis and computer simulations. Furthermore, the steady-state and the dynamic performance of the conventional PWM buck and zero-voltage switching quasi-resonant buck converters are investigated. The experimental results are obtained for various loads and switching frequencies. It is observed that the experimental results obtained are in agreement with the computer simulation results in chapter 5. The amplitude of the oscillations in PWM buck converter is much greater than the computer simulation results. This may be due to a misinterpretation of the parasitic components. Furthermore, the output voltage overshoot and the rising time are much higher in experimental waveforms in closed-loop ZVS quasi-resonant buck converter due to the immediate change in line voltage and load. This may be caused by the variations in compensation network components.

As a conclusion, the switching losses could be considerably reduced with zero-voltage switching quasi-resonant buck topology by shaping the voltage across the switch in quasi-sinusoidal fashion. The oscillations which are present in PWM buck converter caused by the resonance between the parasitic components could be eliminated in ZVS quasi-resonant buck converter. It has been shown that the only two drawbacks of the ZVS quasi-resonant topology are the increase in the peak value of the voltage across the MOSFET depending on the load range and the unfavorable switching conditions for the output diode.

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