DESIGN AND IMPLEMENTATION OF A VOLTAGE SOURCE CONVERTER BASED STATCOM FOR REACTIVE POWER COMPENSATION AND HARMONIC FILTERING

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Approval of the Graduate School of Natural and Applied Sciences

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ABSTRACT

DESIGN AND IMPLEMENTATION OF A VOLTAGE SOURCE CONVERTER BASED STATCOM FOR REACTIVE POWER COMPENSATION AND HARMONIC FILTERING

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In this thesis, design and implementation of a distribution-type, voltage source converter (VSC) based static synchronous compensator (D-STATCOM) having the simplest converter and coupling transformer topologies have been carried out. The VSC STATCOM is composed of a +/- 750 kVAr full-bridge VSC employing selective harmonic elimination technique, a low-pass input filter, and a Δ/Y connected coupling transformer for connection to medium voltage bus. The power stage of VSC based STATCOM is composed of water-cooled high voltage IGBT modules switched at 850 Hz for the elimination of 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23^{rd}, and 25^{th} voltage harmonics. Special care has been taken in the laminated busbar design to minimize stray inductances between power semiconductors and dc link capacitor. Reactive power control is achieved by applying the phase angle control technique. The effect of input filter on total demand distortion has been investigated theoretically by mathematical derivations.

The proposed VSC STATCOM has been implemented for reactive power compensation of Coal Preparation System in Kemerköy Thermal Power Plant. The

field test results have shown the success of the implemented system in view of fast response in reactive power compensation, and minimum input current harmonic content, and compliance with the IEEE Std. 519-1992 even for the weakest power systems. The application of selective harmonic elimination technique and phase angle control to VSC STATCOM has led to optimum switching frequency and device utilization for high voltage IGBTs at the expense of slower response as compared to other PWM techniques.

Keywords: Distribution Static Synchronous Compensator (D-STATCOM), Flexible AC Transmission Systems (FACTS), Power Quality, Reactive Power Control, Voltage Source Converter (VSC)

ÖZ

REAKTİF GÜÇ KOMPANZASYONU VE HARMONİK FİLTRELEME AMACIYLA KULLANILACAK GERİLİM KAYNAKLI ÇEVİRGECE DAYALI STATKOMUN TASARIMI VE GERÇEKLENMESİ

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Bu tez çalışmasında, en basit çevirgeç ve kuplaj trafosu topolojisine sahip dağıtım tipi ve gerilim kaynaklı çevirgece (GKÇ) dayanan statik senkron kompanzatör (D-STATKOM) tasarlanmış ve gerçekleştirilmiştir. GKÇ STATKOM seçici harmonik eliminasyonuna dayalı +/- 750 kVAr tam köprü GKÇ, alçak geçirgen giriş filtresi ve orta gerilim baraya bağlantıda kullanılan Δ/Y bağlı kuplaj trafosundan oluşmaktadır. GKÇ'e dayalı STATKOM'un güç katı 5., 7., 11., 13., 17., 19., 23. ve 25. gerilim harmoniklerinin eliminasyonu için 850Hz'de anahtarlanan su soğutmalı yüksek gerilim IGBT modüllerinden oluşmaktadır. Güç yarıiletkenleri ile da bağ kondansatörler arasındaki parazitik endüktans değerini azaltmak için lamine bara tasarımına özel önem gösterilmiştir. Reaktif güç kontrolü faz açısı kontrolü tekniğini uygulayarak sağlanmıştır. Alçak geçirgen giriş filtresinin Toplam Talep Bozulumu üzerindeki etkisi matematiksel çıkartımlarla incelenmiştir.

Önerilen GKÇ STATKOM Kemerköy Elektrik Üretim A.Ş.'nde kullanılan Kömür Hazırlama Sistemi'nin reaktif güç kompanzasyonu için uygulanmıştır. Sahada alınan kayıtlar reaktif güç ihtiyacına hızlı tepki, sistem akımlarının harmonik dağılımı, IEEE Std. 519-1992 standartlarının zayıf şebekeler için geçerli olan değerleri açısından incelenmiş ve kayıt sonuçları GKÇ'e dayalı STATKOM'un başarısını göstermiştir. Seçici harmonik eliminasyonu ve faz açısı kontrolü tekniklerinin GKÇ STATKOM'a uygulanması PWM tekniklerine göre daha yavaş bir reaktif güç tepkisi vermesine rağmen yüksek gerilim IGBT'ler için optimum anahtarlama frekansı elde edilmiş ve yüksek gerilim IGBT modülleri gerilim ve akım değerleri açısından güvenli bir bölgede kullanılmıştır.

Anahtar Kelimeler: Dağıtım Tipi Statik Senkron Kompanzatör (D-STATKOM), Esnek AA İletim Sistemleri (FACTS), Güç Kalitesi, Reaktif Güç Kontrolü, Gerilim Kaynaklı Çevirgeç (GKÇ)

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NOMENCLATURE

C_b	Busbar Capacitance
C_d	DC Link Capacitance
C_f	STATCOM Input Filter Capacitance
E_{off}	Turn-Off Energy of HV IGBT Module
E_{on}	Turn-On Energy of HV IGBT Module
E_{rec}	Reverse Recovery Energy of HV IGBT Module
G_b	Busbar Conductance
I_c	VSC Current
I_d	DC Link Current
I_f	Input Filter Capacitor Line Current
I_L	Load Current
I_s	Source Current
I_{VSC}	VSC Line Current
I_{swt}	HV IGBT Module Switch Current
I_{1kV}	1kV Line Current
$I_{6.3kV}$	6.3 kV Line Current
$I_{31.5kV}$	31.5 kV Line Current
L	Total referred inductance to 1 kV bus including source inductance, transformer leakage inductance and STATCOM input filter inductance
L_i	Internal Inductance of Laminated Busbar
L_{e1}, L_{e2}	External Inductance of Laminated Busbar
L_{eff}	Effective DC Link Inductance
L_s	STATCOM Input Filter Inductance

L_t	Total referred inductance to 1 kV bus including source inductance and transformer leakage inductance
m_a	Amplitude Modulation
m_f	Frequency Modulation
P_{con}	Conduction Losses of HV IGBT Module
P_{swt}	Switching Losses of HV IGBT Module
R	Equivalent Resistance representing the Active Power Losses of STATCOM
R_{ac}	AC Resistance of Laminated Busbar
R_d	Permanent Dc Link Resistance
R_{dc}	DC Resistance of Laminated Busbar
R_{dr}	Discharging Resistance of Precharging Circuit
R_g	Gate Resistance of HV IGBT Module
R_{ha}	Heatsink-to-Ambient Thermal Impedance
R_{pr}	Charging Resistace of Precharging Circuit
Q_c	VSC Reactive Power
Q_L	Load Reactive Power
Q_s	Source Reactive Power
V_{A0}	Line-to-Neutral VSC Voltage
V_c	Fundamental Line-to-Neutral VSC Voltage
V_{ce}	HV IGBT Module Collector-Emitter Voltage
V_d	DC Link Voltage
V_{ge}	HV IGBT Module Gate-Emitter Voltage
V_n	Line-to-Neutral VSC Voltage Harmonics
V_s	Fundamental Line-to-Neutral Source Voltage
V_{VSC}	Line-to-Line VSC Voltage
V_{1kV}	Line-to-Line 1kV Voltage
$V_{6.3kV}$	Line-to-Line 6.3 kV Voltage

$V_{31.5kV}$	Line-to-Neutral 31.5 kV Voltage
δ	Phase Angle between AC Grid Voltage and VSC Voltage
δ_s	Skin depth
θ	Load Angle

ABBREVIATIONS

CSC	Current Source Converter
D-STATCOM	Distribution Static Synchronous Compensator
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FACTS	Flexible AC Transmission Systems
FFM	Fundamental Frequency Modulation
FIT	Failure in Time
FWD	Freewheeling Diode of IGBT Module
GRP	Glass Reinforced Polyester
GTO	Gate Turn-Off Thyristor
HV IGBT	High Voltage Integrated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
IPM	Intelligent Power Module
LTDS	Long Term DC Stability
LV	Low Voltage
MKK	Metallized Polypropylene Film
MV	Medium Voltage
NPC	Neutral Point Clamped
PAM	Pulse Amplitude Modulation
PCC	Common Coupling Point
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RBSOA	Reverse Biase Safe Operating Area

RRSOA	Reverse Recovery Safe Operating Area
SCSOA	Short Circuit Safe Operating Area
SHEM	Selective Harmonic Elimination Modulation
SPWM	Sinusoidal Pulse Width Modulation
SSG	Static Synchronous Generator
STATCOM	Static Synchronous Compensator
SVC	Static VAR Compensator
TCR	Thyristor Controlled Reactor
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
TSC	Thyristor Switched Capacitor
VSC	Voltage Source Converter

CHAPTER 1

INTRODUCTION

1.1 Static Shunt Compensators

Today's critical manufacturing processes require a stable flow of electricity. Sags, swells, harmonics and flickers are the main power quality problems. Although static shunt compensators in both transmission systems and distribution systems have the same structure, their objectives are different due to their concerns on the power quality issues.

The objectives of shunt compensators in a transmission system are as given below in order to increase the transmitted power in the transmission lines.

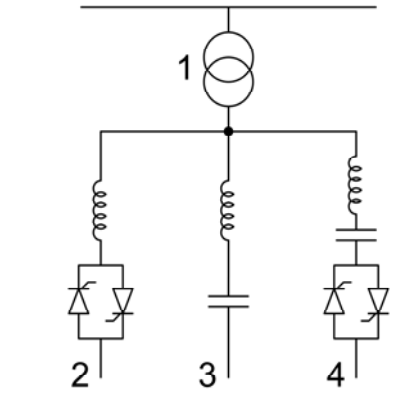
- Midpoint voltage regulation for line segmentation in order to increase transmittable power in the transmission system.
- End of line voltage support requires the compensation of loads having poor power factor. This increases the maximum power transmission capability of the transmission line while improving the voltage instability limits.
- Improvement of transient stability margin by increasing the maximum transmittable power in the transmission line.

The primary objectives of a shunt compensator in a distribution system are given below:

- Compensation of loads with poor power factor in order to obtain nearly unity power factor
- Voltage regulation for the loads that cause fluctuations in the supply voltage
- Load balancing by cancelling the effect of unbalanced loads
- Filtering out the load harmonic currents in order to form a nearly sinusoidal supply current
- Power oscillation damping by exchanging active (real) power with power system

Shunt Connected Reactive Power Compensators can be analyzed in two parts according to IEEE definitions. The first part is Static VAR Compensators (SVC) and the second part is Static Synchronous Generators (SVG).

IEEE defines Static VAR Compensator as a shunt connected static var generator or absorber whose output is adjusted to exchange capacitive or inductive power in order to control reactive power flow [1]. Static VAR compensators were first developed in the late 1960s for the compensation of large fluctuating loads such as electric arc furnaces [2]. SVC based systems use Thyristor Switched Capacitors (TSC) or Thyristor Controlled Reactors (TCR) with fixed filters employing capacitive/inductive reactive power and harmonic filtering. SVC systems cause harmonic current problems while they solve reactive power problems. This requires constant shunt filters or special transformer connections for these systems. Different types of Static VAR Compensators are shown in Fig.1.1.



1: Coupling Transformer
2: Thyristor controlled reactor (TCR)
3: Fixed connected capacitor/filter bank
4: Thyristor switched capacitor bank (TSC)

Figure 1.1 SVC Examples

A capacitor is connected in series with two back-to-back connected thyristors in TSC systems. The control of TSC is obtained by cycle selection principle such that capacitor is totally connected to line by firing thyristors or disconnected by blocking thyristors.

A reactor is connected in series with back-to-back connected thyristors in TCR systems. The delay angle is defined as the angle between the zero-crossing of line-to-line voltage and firing signal of thyristors. Reactive power of the reactors is controlled by holding the delay angle between 90º and 180º. Furthermore, each phase can be compensated independently by TCR systems .

Starting from late 1970s, dynamic compensation of electric power systems have been achieved by using TSC and TCR combinations with permanent capacitive filters connected to the secondary of a coupling transformer.

V-I characteristics of SVCs is shown in Fig. 1.2 [3]. As seen from Fig. 1.2, reactive power capability of SVCs is directly related to the source voltage and any decrease in the source voltage reduces the reactive power compensation capability of SVCs.

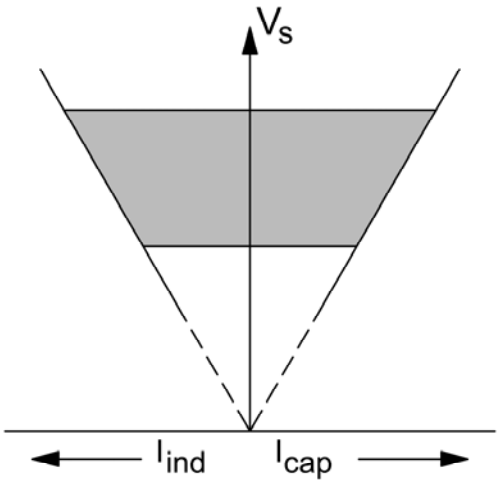


Figure 1.2 V-I Characteristic of SVCs

An example of SVC system consisting of Thyristor Controlled Reactors with fixed capacitors is shown in Fig. 1.3 [4].

IEEE defines Static Synchronous Generators as self-commutated switching power converters supplied from an appropriate electric energy source and operated to produce a set of adjustable multiphase voltages, which may be coupled to an ac power system for the purpose of exchanging independently controllable real and reactive power [1].

The possibility of generating controllable reactive power directly, without the use of ac capacitors or reactors by various switching power converters was disclosed by Gyugi in 1976 [5]. From the standpoint of reactive power generation, their operation is similar to that of a synchronous condenser. Synchronous condenser is an ideal synchronous machine connected to utility voltage and working in no load condition. Reactive power is varied by changing field current. Armature current versus field current relation of synchronous condenser is given in Fig. 1.4. However, reactive power can not be controlled fast enough for rapid load changes by using synchronous condenser. Switching power converters can also exchange real power with the ac system if supplied from an appropriate, usually dc energy source. Because of these similarities with a rotating synchronous generator, they are

termed as Static Synchronous Generator (SSG). When the active energy source is replaced by a DC capacitor or DC reactor which can not absorb or deliver real power except for short durations, SSG becomes a Static Synchronous Compensator (STATCOM) [1].

Figure 1.3 SVC-Thyristor Controlled Reactor

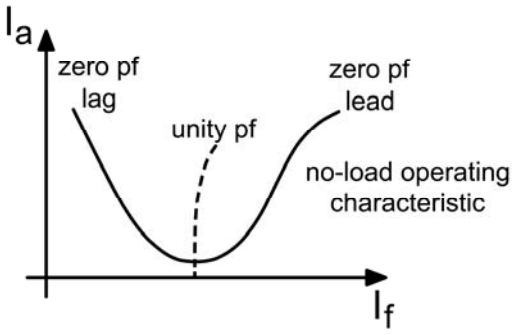


Figure 1.4 Armature Current versus Field Currrent for Synchronous Condenser

STATCOM produces controllable generating or absorbing reactive power by using power electronic switching converters. These converters do not use any capacitor or reactor banks to produce reactive power. However, they need low pass input filters,

formed as LC generally, to suppress the switching frequency harmonics of the converter. They perform reactive power compensation by forming magnitude and phase controlled three phase sinusoidal voltages at the supply terminals.

V-I characteristic of STATCOM is shown in Fig. 1.5 [3]. The advantage of STATCOM over SVCs can be seen if the V-I caharacteristics are compared. In SVCs, reactors or capacitors directly determine the reactive power ratings of the SVC system. However, in STATCOM systems, the reactive power is determined by the switching converter part and reactive power can be kept constant irrespective of the supply voltage fluctuations.

STATCOM systems are used in distribution and transmission systems for different purposes. STATCOMs are used in transmission systems to control reactive power and to supply voltage support to buses. Transmission STATCOMs are high power systems (20MVAr-100MVAr). Switching frequencies are kept low because of high voltages and currents in the converters. Integrated Gate Commutated Thyristor (IGCT) , Gate Turn-Off Thyrsitor (GTO) and High Voltage (HV) IGBT are the candidate power semiconductors for Transmission STATCOMs.

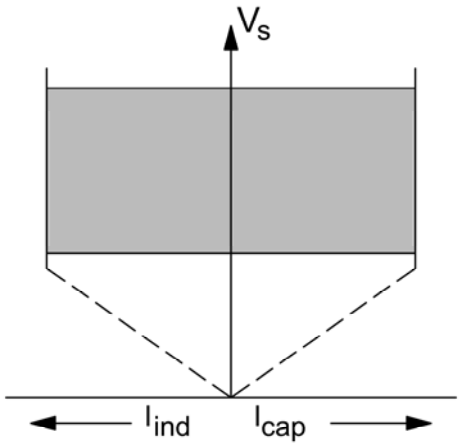


Figure 1.5 V-I Characteristic of STATCOM

STATCOM is installed in distribution systems or near the loads to improve power factor and voltage regulation. This type of STATCOM is called D-STATCOM. D-STATCOMs are medium power systems (up to 5MVAr). D-STATCOMs have faster response when compared with Static VAR Compensators and Transmission STATCOMs. D-STATCOMs can use high switching frequencies and IGBT, HV IGBT and IGCT are the candidate power semiconductors for D-STATCOMs.

The first installation of STATCOM is a ±100 MVAr Static Condenser (STATCON, now renamed as STATCOM) at the TVA Sullivan substation commissioned in 1995 [2,6]. Leading or lagging reactive current is drawn from the AC system to regulate the bus voltage.

This was followed by the American Electric Power (AEP) Unified Power Flow Controller (UPFC) project at the Inez Kentucky station which has two ±160 MVA inverters. During Phase I of the project, the first inverter was connected in shunt [7]. In Phase II, the second inverter was installed in series with the Big Sandy to Inez transmission line to allow the installation to operate as a UPFC [8].

EPRI and Westinghouse have developed a ±2 MVAr D-STATCOM for BC-Hydro Company in 1997 which is connected to 25 kV busbar [9]. This D-STATCOM is employed to mitigate sawmill generated voltage flicker polluting a 25kV feeder.

Henan Electric Power Company and Tsinghua University have jointly developed a 20 MVA STATCOM in 1999 which is connected to 220 kV [10]. This STATCOM system is used to improve the stability of power transmission system.

As a result of the faced power quality problems in some parts of UK, STATCOM is viewed as an important step towards long-term objectives intended to encourage new technologies with the potential of improving the efficiency and security of the system. Hence, Areva has developed a ±75 MVAr STATCOM for UK National Grid which is connected to 275 kV /400 kV [11].

Toshiba and Mitsubishi Transmission and Distribution (TM T&D) has developed a ±2 MVAr D-STATCOM System for Seattle Iron&Metals Corp to 4.16 kV in 2000

[12]. D-STATCOM system is employed in voltage flicker compensation of a 4.000 Hp shredder motor. TM T&D has also developed Transmission STATCOMs having reactive powers of 100-200 MVAr [13]-[14].

Fuji Electric has developed a 60 MVAr STATCOM for Central Japan Railway Company in 2003 which is connected to 77 kV [15]. STATCOM is used to compensate negative-phase sequence power of Japanese bullet trains.

TUBITAK-UZAY developed the first Current Source Converter (CSC) based STATCOM for Turkey Coal Enterprises in 2004 [16]. CSC STATCOM is used to solve the reactive power compensation problem of coal mining excavators.

An example of VSC based STATCOM is shown in Fig. 1.6.

A majority part of the implemented systems are transmission STATCOMs and a few implementations of D-STATCOMs exist in the literature.

Figure 1.6 Voltage Source Converter Based STATCOM

The literature survey of STATCOMs can be grouped as follows :

- Analysis and design of STATCOM [17-20]
- Modeling and control of STATCOM [21-25]
- Frequency domain model and harmonic analysis of STATCOM [26-28]
- STATCOM operation with unbalanced voltages and currents [29-31]
- Linear and nonlinear models as an alternative of PI Controllers in STATCOM [32-35]

Analysis and design of a three-phase synchronous solid-state var compensator is discussed in [17]. Control circuit description, Selective Harmonic Elimination Modulation (SHEM) technique application, passive components selection are given and the theory is tested on a 1kVA prototype.

Theory, modeling and applications of STATCOM are discussed in [18]. Theory is discussed based on single line diagram, and simulation results are given for 12 pulse and 24 pulse converters.

Models using phasor algebra can not accurately describe the STATCOM behaviour during compensation of subcycle transients in the PCC voltage. The small-signal model of STATCOM system is derived in [19] to find a valid mathematical model of the system and STATCOM behaviour during subcycle transients in the PCC voltage are accurately found. Simulation results are given to support the model.

Steady-state and transient models of STATCOM are derived in [21] by transforming abc axis voltage equations into synchronously rotating reference frame (d-q axis) equations. Models are given in s-domain. The results are verified by simulations.

A per unit STATCOM model is proposed in [22] and open loop response time constant is defined in terms of system parameters. The results are given by simulation results.

Average circuit model of angle-controlled STATCOM is discussed in [23]. An average operator is defined and applied to the state equation to get an averaged mathematical model. The results are verified for a 75kVAr STATCOM.
Control system design for a Pulse Width Modulation (PWM) based STATCOM is discussed in [24] by using decoupled pq theory. Control of capacitor voltage is discussed and the results are given for a 15kVAr laboratory setup.

Analytical expressions for the admittances and impedances of STATCOM are presented in [26] as a function of frequency and thereby steady state frequency response is obtained. Simulation results are given to verify the theoretical work.

Harmonic resonance phenomena caused by source voltage harmonics and system parameters are discussed in [27] by using the per unit model found in [22]. The results are given for a 10kVAr laboratory setup.

Unbalance compensation with D-STATCOM is given in [29]. Dynamic characteristics of Sinusoidal Pulse Width Modulation (SPWM) VSC based D-STATCOM are given and adjustment of PWM pulse width for unbalanced load compensation is described. Transition times from full inductive mode to full capacitive mode is found as 40ms in the experimental tests.

A pole placement controller for D-STATCOM is given in mitigation of three phase fault in [32]. Pole placement controller is one of the alternative methods of PI controller when linear controllers are considered. Pole placement controller is simulated with D-STATCOM in MATLAB and the results are given.

Different non-linear control methods are recommended in the literature. However, they are generally supported only by the simulations. Linear controllers have satisfactory performance around the linearized operating point. However, performance of linear controllers get worse at different operating points, different loads and in case of parameter changes. Nonlinear control methods such as sliding mode controller [33], artificial neural networks [34] and fuzzy control [35] are studied in order to eliminate the disadvantages of linear controllers.

1.2 Scope of the Thesis

Within the scope of this thesis, VSC based D-STATCOMs employing Selective Harmonic Elimination Modulation (SHEM) technique, having simplest converter topology with HV IGBT modules are investigated. Different reactive power control techniques are studied and phase angle control is selected among them as the reactive power control technique. Modulation techniques are investigated to approximate the input voltage and current waveforms to pure sine wave and SHEM technique eliminating 5^{th}, 7^{th}, 11^{th}, 13^{nd}, 17^{th}, 19^{th} , 23^{rd}, 25^{th} voltage harmonics is decided to be the most appropriate technique for the studied D-STATCOM. A prototype D-STATCOM system is designed to be used in medium voltage applications by using the theoretical work. The designed system is implemented in Kemerköy Thermal Power Plant to solve the reactive power compensation problem of coal conveyor belts. Theoretical work is verified by laboratory and field tests.

This research work has made the following original contributions to the area of STATCOM systems:

- SHEM technique is applied to medium power Voltage Source Converter (VSC) based Distribution STATCOMs for the first time [36].
- Reactive power compensation problem of belt conveyors in Coal Transportation Systems is solved by VSC based D-STATCOM for the first time [37].
- Investigation of the effect of input filter size on the Total Demand Distortion (TDD) of VSC based D-STATCOM.
- Optimization of the number of harmonics to be eliminated in the line-to-line converter voltage waveform of VSC based D-STATCOM in view of switching capability of HV IGBT modules.

The outline of the thesis is given below :

In Chapter 2, system description is given and and harmonic reduction techniques for transmission and distribution STATCOMs are discussed. Operating principles of D-STATCOM are discussed in detail for the lossless and lossy systems. After discussing the different control methods that can be applied to D-STATCOMs,

Pulse Width Modulation (PWM) techniques are studied for 2 level, 3 leg Voltage Source Converters. Principles of Sinusoidal PWM and SHEM techniques are given. Optimization of the number of harmonics to be eliminated by SHEM technique is discussed for 7-Angle, 9-Angle and 11-Angle SHEM and the optimum solution for HV IGBT modules is given. Reactive power measurement methods are discussed briefly at the end of Chapter 2.

In Chapter 3, design principles of VSC based D-STATCOM are given and design specifications of VSC based D-STATCOM are stated. Selection of the appropriate power semiconductor among the available power semiconductors and the effect of modulation index on the device specifications are discussed. Design of power stage layout are stated including the details of laminated busbar design. Theoretical calculation and experimental verification of the effective DC link inductance are given. Design criteria of input filter and DC link capacitor are given with the theoretical calculations including the STATCOM line current TDD, line-to-line voltage THD and DC link capacitor current. Design of control system, typical open and closed loop responses found in MATLAB and PSCAD programs are discussed. Protection circuits designed, implemented and integrated into resulting VSC based D-STATCOM are given at the end of Chapter 3.

In Chapter 4, field results obtained from the application of developed system for group compensation of coal conveyor belts are presented. Field results include technical performance indices such as converter waveforms, input filter waveforms, harmonic spectra of the converter voltages and line currents, LV/MV voltage and current waveforms and active power losses of the VSC based D-STATCOM system. The results of the field tests have also shown that the prototype D-STATCOM successfully compensates the reactive power demand of coal conveyor belts driven by MV and LV induction motor and comply with the reactive energy penalty limits that will have been imposed by the end of 2007.

General conclusions are given in Chapter 5. Suggestions for a further study are also proposed.

In Appendix A, active and reactive power flow calculations between source and STATCOM are presented.

In Appendix B, simulation model of VSC based STATCOM in PSCAD/EMTDC is presented.

In Appendix C, measurement apparatus used in the laboratory and field tests are presented.

CHAPTER 2

OPERATING PRINCIPLES OF VOLTAGE SOURCE CONVERTER BASED STATCOM

2.1 Basic Circuit Configuration

STATCOM is a shunt connected Flexible AC Transmission System (FACTS) device which generates a set of three phase sinusoidal voltages at fundamental frequency with controlled amplitude and phase angle. STATCOM consists of the coupling transformer, input filter, Voltage Source Converter and a controller. The connection of STATCOM to AC bus is shown in Fig. 2.1.

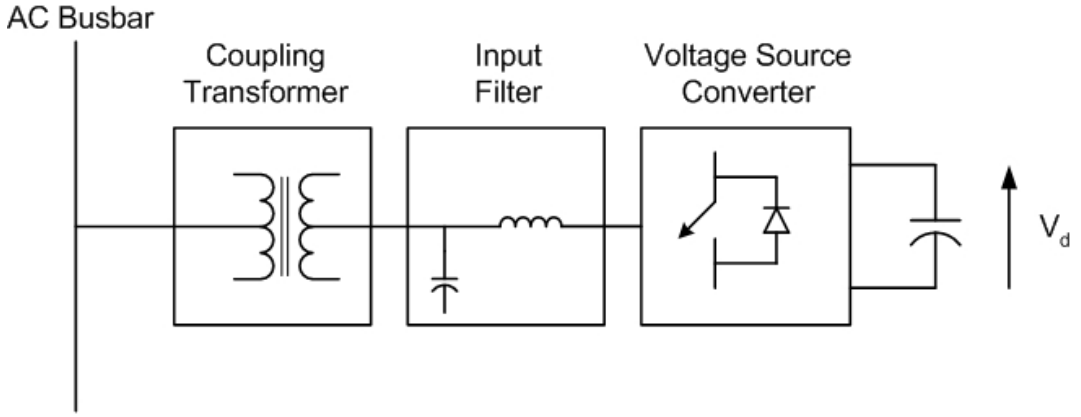


Figure 2.1 Connection of STATCOM to AC Busbar

When two AC sources of same frequency are connected through a series inductance, active power flows from leading source to lagging source and reactive power flows from higher voltage magnitude AC source to lower voltage magnitude AC source. Active power flow is determined by the phase angle difference between the sources and the reactive power flow is determined by the voltage magnitude difference between the sources [1]. Hence, STATCOM can control reactive power

flow by changing the fundamental component of the converter voltage with respect to the AC busbar voltage both phasewise and magnitudewise.

Power stage selection of Voltage Source Converter depends on the harmonic reduction technique, load characteristics and control method preferred in the design. Harmonic reduction techniques can be classified in two groups which can be named as 'Fundamental Frequency Modulation (FFM)' techniques and 'SPWM/ SHEM' techniques [38].

Each power semiconductor is switched on and off only one time over a fundamental period in FFM techniques. Basic FFM schemes can be described as follows :

- Multi-pulse converters in which multiple 6 pulse converters are connected parallel on the dc side and with phase shifting transformers on the ac side [38]. Selected harmonics are eliminated with transformer connections and complicated transformer connections are required for lower harmonic spectra.
- A multi-level converter is used in which the dc link capacitor is divided into the converters. AC side is connected to the selected converter by switching control and staircase waveforms are obtained with reduced harmonics. This topology allows the use of simpler transformer connections at the expense of complicated control systems to maintain capacitor voltage equalization.

SPWM and SHEM techniques have become more popular when compared to FFM techniques with the advances in power semiconductor technologies. Each power semiconductor is switched at higher frequencies (250Hz-5kHz) to offer minimum harmonic spectra.

- A two level, 3 leg or a 3 level neutral point clamped (NPC) converter is used with SPWM technique. This method offers small quantities of harmonics since the switching is done in the kHz range at the expense of higher switching losses.

- A two level, 3 leg converter is used with SHEM technique. This method offers small quantities of harmonics with optimised switching frequency.

The choice of the power stage depends on the system voltage, power ratings of required STATCOM. The scope of this thesis is based on the 2 level, 3 leg Voltage Source Converter topology which is shown in Fig. 2.2.

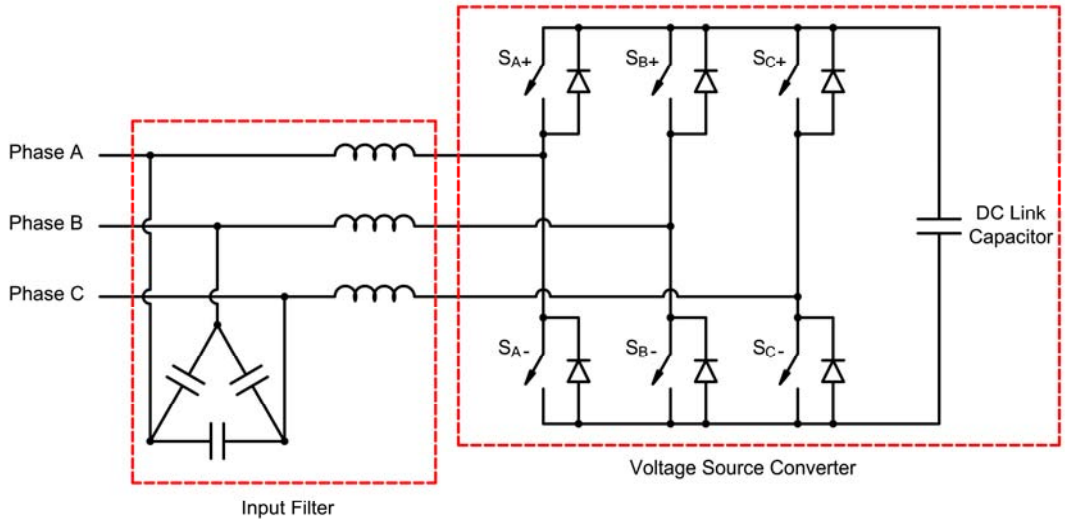


Figure 2.2 2 Level, 3 Leg Voltage Source Converter

Input filter is used to filter out the switching harmonics of the converter. It can be designed as an inductance only filter or a low pass LC filter depending on the reactive power generation limits of the system and IEEE 519-1992 standard.

2.2 Principles of Reactive Power Control

Simplified single phase Y equivalent model of STATCOM is given in Fig. 2.3.

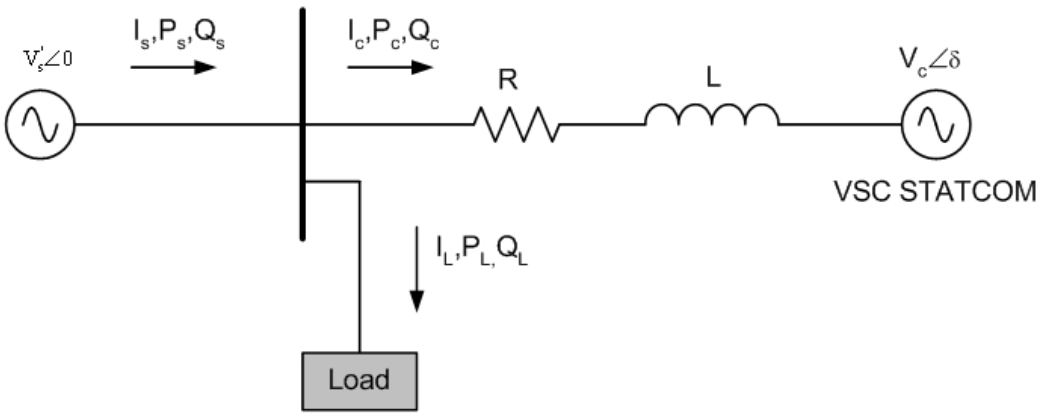


Figure 2.3 Simplified Model of STATCOM

V_s' : RMS line-to-neutral AC grid voltage with a phase angle of 0 referred to STATCOM side.

V_c : RMS line-to-neutral STATCOM fundamental voltage

I_S : RMS source current

I_L : RMS load current

I_c : RMS STATCOM current

Q_S : Source reactive power

Q_L : Load reactive power

Q_c : STATCOM reactive power

δ : Phase angle between fundamental voltage of STATCOM and AC grid

R : Y equivalent total loss resistance including coupling transformer losses, series inductor losses and converter losses

L : Y equivalent total inductance including source inductance, leakage inductance of coupling transformer and input filter inductance.

The phasor diagram for Fig. 2.4 is given below :

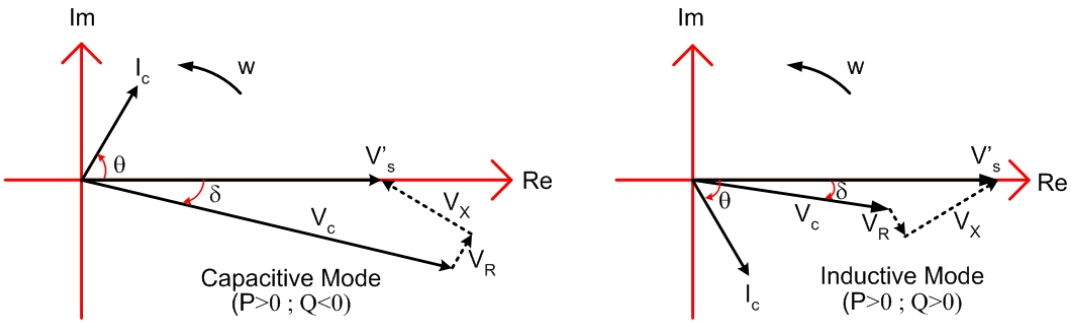


Figure 2.4 Phasor Diagrams for Lossy Systems
(Not-to-scale, phase angles are exaggerated)

Kirchoffs voltage equations for the circuit in Fig.2.3 can be written as follows by using the phasor diagrams in Fig. 2.4.

$$\overline{V}_s^{'} = \overline{V}_c + \overline{V}_R + \overline{V}_X \qquad (2.1)$$

where $X = 2\pi fL$, $\overline{V}_R = RI_c$ and $\overline{V}_X = jXI_c$

By resolving $\overline{V}_R$ and $\overline{V}_X$ along Re and Im axes in Fig 2.4, (2.2) and (2.3) can be obtained.

$$V_s^{'} - V_c \cos\delta = (R\cos\theta + X\sin\theta)I_c \qquad (2.2)$$

$$V_c \sin\delta = (X\cos\theta - R\sin\theta)I_c \qquad (2.3)$$

On the other hand, active and reactive power consumed by the STATCOM from the supply can be expressed as in (2.4) and (2.5)

$$P_c = V_s^{'} I_c \cos\theta \qquad (2.4)$$

$$Q_c = V_s^{'} I_c \sin\theta \qquad (2.5)$$

Power sink convension has been used in the formulations given above. This convention associates a positive sign with the reactive power flowing into an

inductive reactance. It occurs when STATCOM input current $\bar{I}_c$ lags behind supply voltage $\bar{V}_s'$ by θ as defined in Fig. 2.4.

Active and reactive power inputs (P_c and Q_c) to the STATCOM can also be expressed in terms of line-to-neutral voltages V_s' and V_c, system parameters R and X and angles θ and δ as derived in Appendix A and given in (2.6) and (2.7).

$$P_c = \frac{V_s'}{X}\left[\frac{RV_s'\sin\theta + XV_c\sin\theta\sin\delta - RV_c\sin\theta\cos\delta + RV_c\cos\theta\sin\delta}{R\cos\theta + X\sin\theta}\right] \tag{2.6}$$

$$Q_c = V_s'\frac{V_s' - V_c\cos\delta}{R\cos\theta + X\sin\theta}\sin\theta \tag{2.7}$$

There is no power dissipation for an ideal STATCOM. It means that R in Fig. 2.3 and P_c in (2.6) should be set to zero. Equating P_c to zero implies that sin δ and hence δ should be zero. Therefore, phasor diagrams given in Fig. 2.4 turn out to be those in Fig. 2.5 for a lossless STATCOM. Also (2.7) simplifies to (2.8)

$$Q_c \cong V_s\frac{V_s - V_c}{X} \tag{2.8}$$

Phasor diagrams for the ideal condition (R = 0) is given in Fig. 2.5.

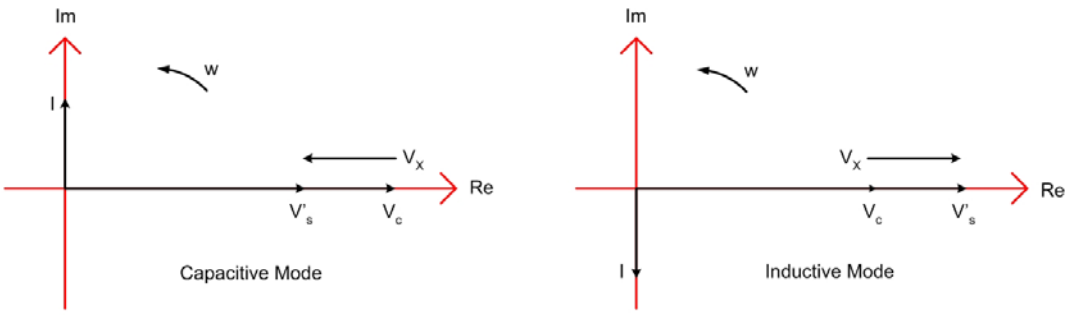


Figure 2.5 Phasor Diagrams for Lossless System

In the lossless system, STATCOM voltage is in phase with the AC line voltage and line current is purely reactive.

If V_c is equal to V_s, reactive power generation is zero.

If $V_c<V_s$, a current is induced which lags V_X. This current also lags V_s since V_X is in phase with V_s. Therefore, AC grid sees this current as inductive and STATCOM is said to be operating in inductive mode.

If $V_c>V_s$, a current is induced which lags V_X. However, this current leads V_s since V_X is in opposite direction with V_s. Therefore, AC grid sees this current as capacitive and STATCOM is said to be in operating capacitive mode.

Voltage and current waveforms of AC grid and STATCOM is shown in Fig. 2.6 for the ideal case.

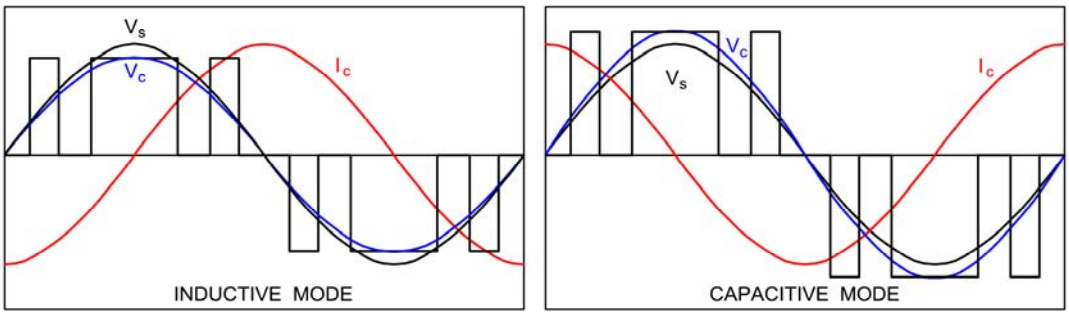


Figure 2.6 Inductive and Capacitive Modes of STATCOM (modulation index = 1.16)

During operation of STATCOM in transient state, the DC link capacitor is to be charged and discharged periodically or aperiodically. Active power will flow from the supply to the DC link or vice versa through the converter. This condition makes necessary a finite load angle δ between $\overline{V}_s'$ and $\overline{V}c$ although its value is small. Furthermore, input filter and VSC have their own losses which necessiates the flow from the supply for operation even in the steady-state (DC link voltage is constant).

Therefore, one can conclude that the ideal STATCOM model in Fig. 2.5 is not an adequate model in describing the operation of a STATCOM especially in transient state.

On the other hand, the model can be simplified by making for R<<X while preserving the active power flow equation in an approximate manner. Phasor diagrams Fig. 2.4 can be simplified as in Fig. 2.7 under this assumption.

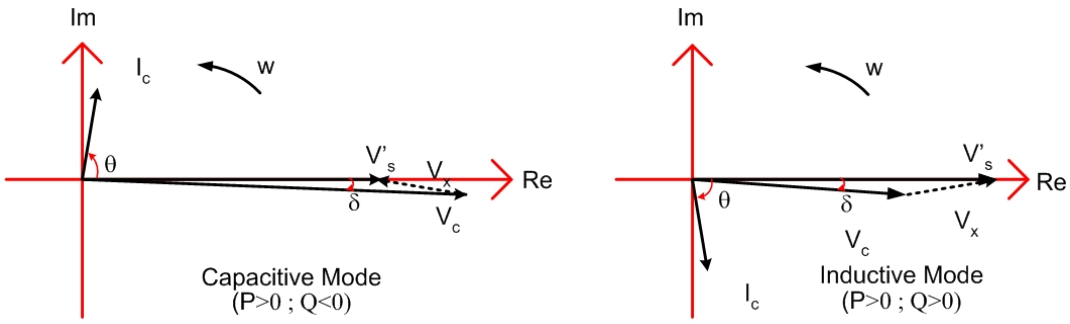


Figure 2.7 Phasor Diagrams for R<<X

In addition to this assumption for the prototype system developed in this thesis, following inequalities hold over the entire operating range (from full inductive to full capacitive).

$$\left.\begin{array}{l} 0 \le \delta \le 2.5^\circ \\ 89 \le \theta \le 90^\circ \end{array}\right\} \text{in the steady state}$$

$-5 \le \delta \le 5^\circ$ in the transient state

Therefore in the steady-state following approximations can be made whereever needed.

$\sin\delta \cong \delta$ where δ is expressed in radians

$\sin\theta \cong 1$ and $\cos\theta \cong 0$

These approximations yield alternative equation sets given below:

$$P_c \cong \frac{V_s V_c}{X} \sin\delta \tag{2.9}$$

$$Q_c \cong V_s \frac{V_s - V_c \cos\delta}{X} \tag{2.10}$$

or

$$P_c \cong \frac{V_s V_c}{X} \delta \tag{2.11}$$

$$Q_c \cong V_s \frac{V_s - V_c}{X} \tag{2.12}$$

It can be deduced from (2.9) and (2.10) that STATCOM absorbs active power even at zero reactive power because of converter losses.

Let us assume the relationship betwen V_c and dc link voltage V_d is given in terms of a constant k.

$$V_c = kV_d \tag{2.13}$$

By subtituting (2.13) in (2.9) and (2.10), (2.14) and (2.15) are obtained.

$$P_c \cong \frac{V_s'}{X} kV_d \sin\delta \tag{2.14}$$

$$Q_c \cong \frac{V_s'}{X}(V_s' - kV_d \cos\delta) \tag{2.15}$$

In order to approximate input voltage of VSC to a pure sinewave at fundamental frequency, Pulse Width Modulation (PWM) or Pulse Amplitude Modulation (PAM) technique can be applied.

For this case, peak value of fundamental component of VSC input voltage (line-to-neutral, $\hat{V}_c$) can be related to dc link voltage in terms of modulation index m_a as given in (2.16) by assuming a two-level line-to-neutral ac voltage.

$$\hat{V}_c = m_a \frac{V_d}{2} \tag{2.16}$$

By using (2.13) and (2.16) one obtains

$$k = \frac{m_a}{2\sqrt{2}} \cong 0.35 m_a \tag{2.17}$$

$$V_c \cong 0.35 m_a V_d \tag{2.18}$$

Substituting of (2.17) in (2.14) and (2.15) yields

$$P_c \cong \frac{0.35 V_s'}{X} m_a V_d \sin\delta \tag{2.19}$$

$$Q_c \cong \frac{V_s'}{X}(V_s' - 0.35 m_a V_d \cos\delta) \tag{2.20}$$

Two different operation modes arise from (2.20).

1) If $0.35 m_a V_d \cos\delta$ can be made smaller than V_s', then Q_c becomes positive and hence VSC absorbs reactive power (inductive operation mode).
2) If $0.35 m_a V_d \cos\delta$ can be made larger than V_s', then Q_c becomes negative and hence VSC delivers reactive power to the supply (capacitive operation mode).

Therefore, different control techniques can be applied in order to change $0.35 m_a V_d \cos\delta$ term. Since δ is smaller than 2.5° in the normal working range of STATCOM, $\cos\delta \cong 1$ can be assumed.

This assumption simplifies the term which is going to be controlled to $0.35 m_a V_d$. It can therefore be concluded that reactive power absorbed or delivered by STATCOM can be controlled by one of the following techniques.

i) varying modulation index m while keeping DC link voltage V_d constant
ii) varying V_d while keeping m constant, or
iii) a combination of (i) and (ii)

Various control strategies have been exercised in the control of two-level STATCOM and Active Power Filter Converters as reported in the literature.

- Modulation index is kept constant and reactive power is controlled by changing the DC link voltage. This is called 'Phase Angle Control' in the literature [38].
- DC link voltage is kept constant and reactive power is controlled by changing the modulation index of PWM waveforms. This technique is called 'Constant DC Link Voltage Scheme' by some authors in the literature [1].
- DC link voltage is kept constant and a current reference is formed according to active/reactive power set by using Instantaneous pq theory. STATCOM line current is directly controlled. It is known as 'Direct Current Control with Instantenous pq Theory' in the literature [39].
- DC link voltage is kept constant and a voltage reference is formed according to active/reactive power set by using Instantaneous pq theory. STATCOM line current is indirectly controlled. It is known as 'Indirect Current Control with Instantaneous pq Theory' in the literature [25].

2.2.1 Phase Angle Control

Modulation index is kept constant and DC link voltage is allowed to change to control the fundamental voltage component of STATCOM. The control variable is the phase angle δ.

In order to increase reactive power delivered or to decrease reactive power absorbed by STATCOM, DC link voltage should be increased by charging further the DC link capacitor. On the other hand, if DC link voltage reduces by discharging the capacitor, then reactive power delivered decreases in capacitive operation mode or reactive power absorbed by STATCOM increases in the inductive operation mode.

STATCOM voltage lags behind AC line voltage ($\delta > 0$) for both capacitive and inductive operation modes in the steady-state (Fig. 2.4).

Power can be extracted from DC link by making phase angle δ in (2.19) negative. If the extracted power is made greater than STATCOM losses, P_c in (2.19) becomes

negative and STATCOM starts to deliver active power to the source. During this operation in transient state, V_d gradually decreases. On the other hand, if δ is momentarily made greater than steady-state value δ_{ss}, the active power absorbed by STATCOM in excess of STATCOM losses will then be stored in the DC link capacitor, thus resulting in a gradual rise in V_d.

Exaggerated phasor diagrams which illustrate power flow between the ac supply and the DC link in transient state are as shown in Fig. 2.8.

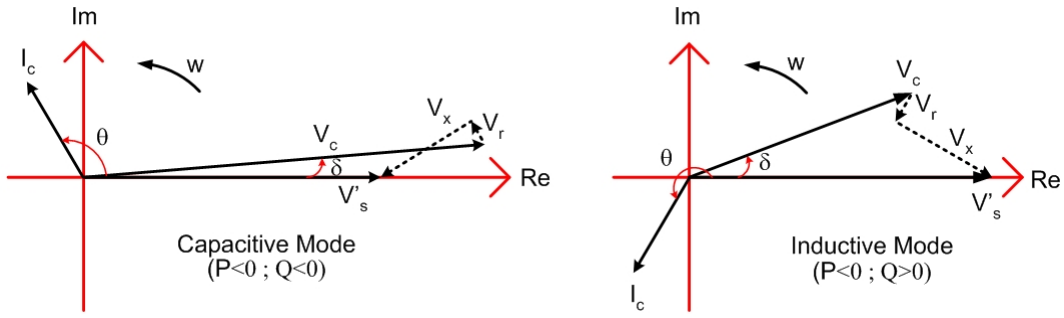


Figure 2.8 Phasor Diagrams In Transient State
(Not-to-scale, phase angles are exaggerated)

The open loop response time of the system involving phase angle control is determined by the input filter inductance and DC link capacitor. Input filter inductance is employed to filter out converter harmonics and the use of higher values for this inductance minimizes STATCOM current harmonics.

However, a large filter inductance than usual will cause a greater voltage regulation value in the DC link as well as at the input of the converter from full inductive mode to full capacitive mode of STATCOM operation (2.20).

Therefore, the selection of passive elements must be done carefully for satisfactory responses in both steady-state and transient state. Block diagram of phase angle control is given in Fig. 2.9.

Reactive power on the supply should be measured in a time period less than 10 ms in order to obtain a fast transient response. Reactive power can be measured by using Average Basis Concept or Instantaneous pq theory which are described at the end of this chapter.

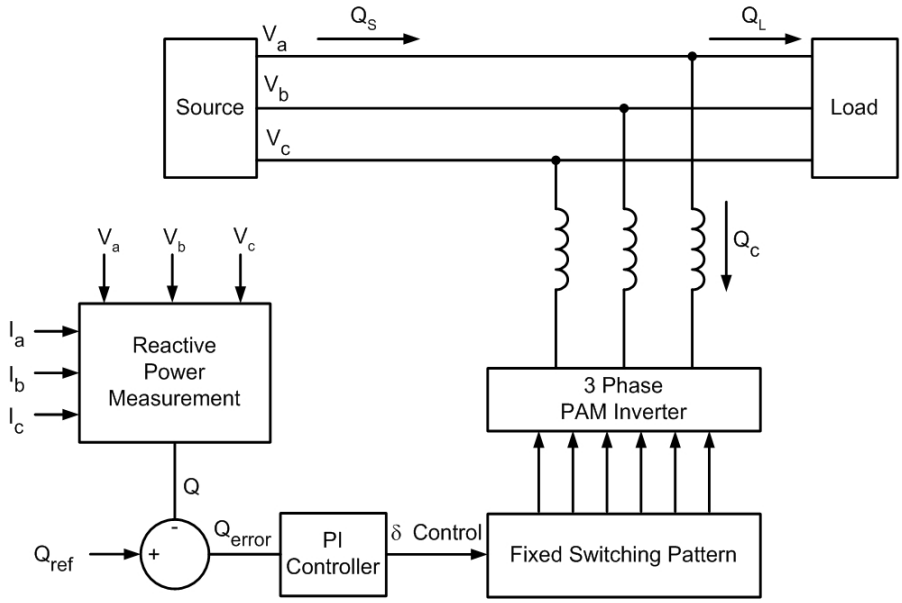


Figure 2.9 Phase Angle Control

Measured reactive power (Q) is compared with reactive power reference (Q_{ref}) which is formed by another control block in real applications. Reactive power error is processed in PI controller and output of PI controller determines the phase angle of STATCOM fundamental voltage with respect to source voltage. The step response of the control loop to reactive power changes can be kept in between 2-5 a.c. cycles by suitable controllers and passive components [1].

2.2.2 Constant DC Link Voltage Scheme

DC Link voltage is kept constant by phase angle control and reactive power input to STATCOM is varied by controlling the modulation index in SPWM STATCOM. There are two seperate control loops which interact with each other. However, it is

possible to minimize the interaction between the loops by separating reaction time of dynamics.

Fundamental component of converter voltage is varied by controlling the modulation index. Hence, this control is preferred mainly in STATCOMs with Sinusoidal Pulse Width Modulation (SPWM). Block diagram of SPWM STATCOM with Constant DC Link Voltage is given in Fig. 2.10 [1].
PLL & counter generates a fixed amplitude sine wave. Modulation signal is obtained by changing the phase angle and amplitude of this fixed amplitude sine wave.

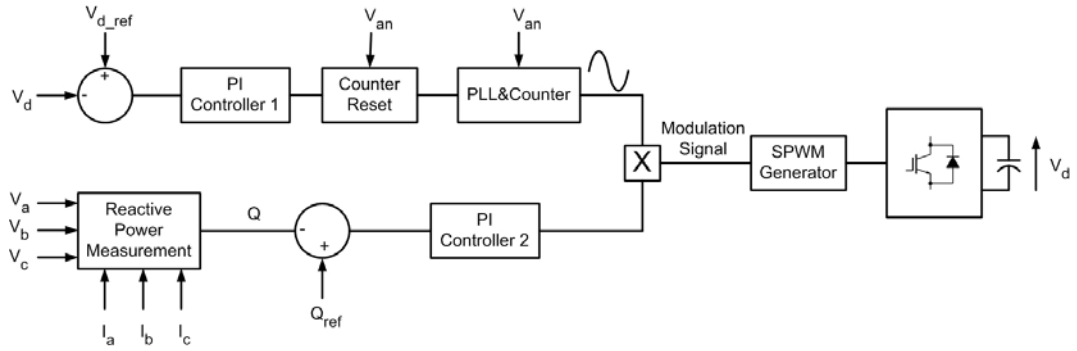


Figure 2.10 Constant DC Link Voltage Scheme

DC link voltage is kept constant by controlling the active power flowing to/from the converter. DC link voltage is compared with the DC link voltage reference and DC link voltage error is processed in PI Controller 1. Output of PI Controller 1 is used to reset the counter in phase locked sine generator. Therefore, PI Controller 1 determines the phase angle of the converter voltage with respect to source voltage.

Reactive power in the line is measured and measured reactive power (Q) is compared with the reactive power set (Q_{ref}). Reactive power error is processed in PI Controller 2 and output of PI Controller 2 is used to scale up/down the amplitude of the sine wave.

DC link voltage can be kept constant by slow changes in the phase angle. Hence, DC link voltage control loop (PI Controller 1) has slow response. Reactive power loop should be fast in order to have rapid reactive power control. (< 2 cycle).

2.2.3 Direct Current Control with pq Theory

STATCOM line current is regulated according to active/reactive power set by using Instantenous pq theory [39]. The block diagram for this case is given in Fig. 2.11.

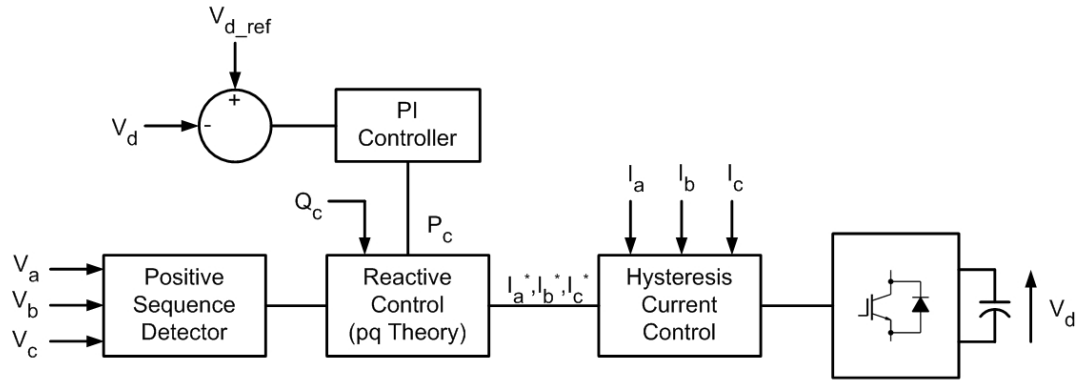


Figure 2.11 Direct Current Control with pq Theory

Positive sequence detector is used to obtain the positive voltage sequence frequency, phase and amplitude signals and to send them to reactive power control block. Reactive power block uses Instantaneous pq theory (pq theory). Reactive power and active power sets are the input references of this block. The line voltages are transformed to V_α and V_β in the $\alpha\beta 0$ frame as given in (2.21).

$$\begin{bmatrix} V_o(t) \\ V_\alpha(t) \\ V_\beta(t) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a(t) \\ V_b(t) \\ V_c(t) \end{bmatrix} \tag{2.21}$$

Current reference signals can be calculated as shown below.

$$i_{c\alpha} = \frac{1}{\Delta}(V_{\alpha}.P_c + V_{\beta}.Q_c) \quad (2.22)$$

$$i_{c\beta} = \frac{1}{\Delta}(V_{\beta}.P_c - V_{\alpha}.Q_c) \quad (2.23)$$

$$\Delta = V_{\alpha}^2 + V_{\beta}^2 \quad (2.24)$$

The current references calculated in the αβ frame are transformed back to ABC coordinates and processed in the current control block. P_c represents the amount of active power in/from the converter and DC link voltage is kept constant by controlling P_c.

2.2.4 Indirect Current Control with pq Theory

Converter voltage is regulated according to active/reactive power set by using Instantenous pq theory [25]. The real power (p) and the reactive power (q) injected into the system can be expressed in the dq reference frame by using Instantaneous pq theory [40].

$$p = v_d i_d + v_q i_q \quad (2.25)$$

$$q = v_q i_d - v_d i_q \quad (2.26)$$

The quadrature component of the voltage is always zero for a balanced three-phase three-wire system. Hence i_d completely describes the instantaneous value of real power and i_q completely describes the instantaneous value of reactive power when the system voltage remains constant. The block diagram for this case is given in Fig. 2.12.

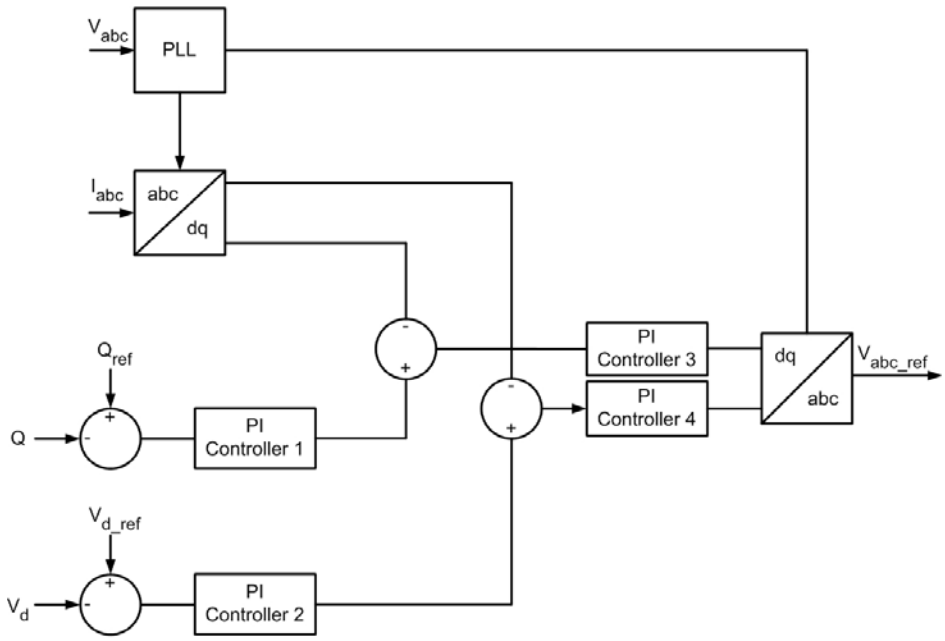


Figure 2.12 Indirect Current Control with pq Theory

Three phase instantaneous currents are transformed using abc to dq0 transformation. The d-axis component i_d and q-axis component i_q are regulated by two separate PI loops. I_d reference is calculated from the control of DC link voltage and I_q reference is calculated from the control of reactive power. Therefore, instantaneous current tracking control is achieved by using four PI loops. Dq0 to abc transformation and a Phase Locked Loop (PLL) is used to find the voltage reference for the switching patterns.

Different control techniques are discussed for the control of reactive power in STATCOM. The step response of each technique depends on the passive parameters such as input filter reactor / DC link capacitor and the reactive power measurement technique used. Phase Angle Control employs SHEM/PAM technique and other control algorithms employ PWM technique.

Phase Angle Control is the only algorithm in which DC link voltage is allowed to vary according to reactive power reference. DC link voltage is kept constant in other algorithms. This situation deterioriates the step response of Phase Angle

Control since the DC link voltage is charged or discharged through the input filter inductance and DC link capacitor. Reactive power measurement by Average Basis Concept is used generally in Phase Angle Control. However, Instantaneous pq theory can be used to fasten the step response of Phase Angle Control.

Constant DC link voltage scheme has a faster step response when compared to Phase Angle Control. Reactive power changes are done only by changing the modulation index of the converter voltage. The delay coming from the charging or discharging of DC link capacitor through the input filter inductance is eliminated in this algorithm. Input filter inductance can be choosen smaller to fasten the step response. However, this necessiates the use of higher switching frequencies for the same Total Demand Distortion (TDD) which increases the switching losses of power semiconductors. Reactive power measurement by Average Basis Concept or Instantenous pq theory can be used according to the aimed step response of STATCOM.

Direct Current Control Algorithm regulates STATCOM line current by using Instantaneous pq theory and a hysteresis band controller. Hysteresis band is made narrower by using higher frequencies. Hence, hysteresis band of the line current is a compromise between tracking error and switching losses. Direct Current Control has a faster response than Indirect Control Control since there is only one PI loop in this algorithm.

Indirect Current Control has a much faster response than Phase Angle Control and slower response than Direct Current Control. Indirect current control regulates the converter output voltage by using four PI loops and this is the main disadvantage of this technique.

Efficient control algorithm for STATCOM is chosen by considering the reactive power rating of the converter and the step response needed for the reactive power compensation of the load. Constant DC Link Voltage Scheme and Direct/Indirect Current Control algorithms propose faster responses at the expense of higher switching frequency in the converter. High power STATCOMs use HV (High

Voltage) IGBT Modules, IGCT or GTO as the power semiconductor. Well known STATCOM applications with these power semiconductors use switching frequencies between 50 Hz-2 kHz because of higher switching losses of the power semiconductors [15,41]. Hence, PWM algorithms are better suited for low power/low voltage applications.

2.3 PWM Techniques Employed in STATCOM Application

The ultimate purpose in the design of a STATCOM for medium voltage (MV) applications is to generate fully controllable sinusoidal line currents on the MV side of STATCOM system. Line current waveforms of STATCOM can be approximated to a sine wave which should comply with IEEE 519-1992 primarily by the use of a proper PWM technique and secondly by carefully designing the input filter of STATCOM. In the case where reactive power control is based on the variation of modulation index m_a, PWM becomes an indispensable part of the reactive power control algorithm.

This subsection will therefore be devoted to the evaluation of some PWM techniques in conjunction with the reactive power control algorithms described in subsection 2.2.

Table 2.1 Modulation Techniques Used in STATCOM Control Algorithms

Control Algorithm	Modulation Technique
Phase Angle Control	Selective Harmonic Elimination Modulation (SHEM)
Constant DC Link Voltage Scheme	Sinusoidal Pulse Width Modulation (SPWM)
Direct Current Control	On/off control is excluded in PWM techniques
Indirect Current Control	Sinusoidal Pulse Width Modulation (SPWM)

The circuit diagram of the two level, three leg Voltage Source Converter is given in Fig. 2.13.

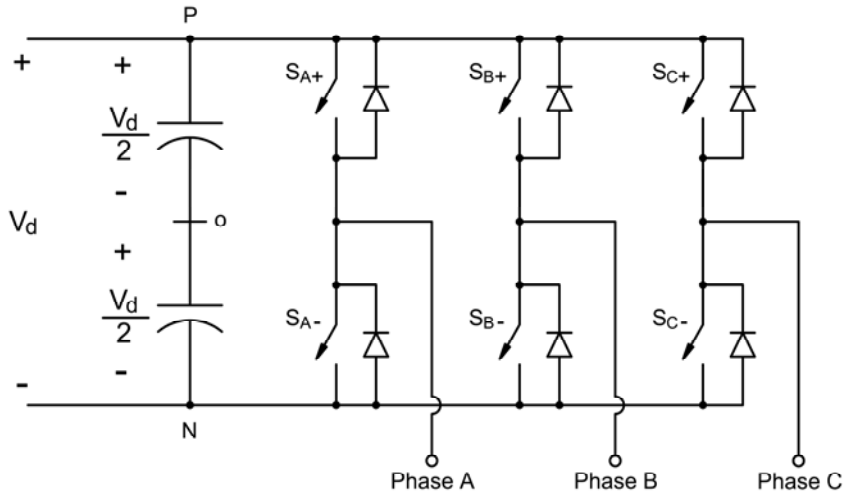


Figure 2.13 2 Level, 3 Leg Voltage Source Converter

2.3.1 Sinusoidal Pulse Width Modulation Technique

Sinusoidal Pulse Width Modulation (SPWM) technique is used to control the fundamental component of the line-to-line converter voltage. Three-phase converter voltages are obtained by comparing the same triangular voltage with three sinusoidal control voltages as shown in Fig. 2.14 [42].

The frequency of the triangular voltage (f_s, carrier frequency) determines the converter switching frequency and the frequency of the control voltages determine the fundamental frequency of the converter voltage (f_1,modulating frequency). Hence, modulating frequency is equal to supply frequency in STATCOM.

Amplitude modulation ratio m_a is defined as :

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \tag{2.27}$$

where $\hat{V}_{control}$ is the peak amplitude of the control voltage and $\hat{V}_{tri}$ is the peak amplitude of the triangular voltage. The magnitude of the triangular voltage is kept constant and the amplitude of the control voltage is allowed to vary.

Linear range of SPWM is defined for $0 \leq m_a \leq 1$ and overmodulation is defined for $m_a > 1$.

Frequency modulation ratio m_f is defined as :

$$m_f = \frac{f_s}{f_1} \tag{2.28}$$

m_f must be choosen as an odd integer to form an odd and half wave symmetric converter line-to-neutral voltage (V_{A0}). Therefore, even harmonics are eliminated from the V_{A0} waveform. Moreover, m_f is choosen as a multiple of 3 in order to eliminate the harmonics at m_f and odd multiples of m_f in the converter line-to-line voltages.

Harmonics in the converter voltages appear as sidebands, centered around the switching frequency and its multiples. This is true for all values of m_a in the linear range.

The frequencies of converter output voltage harmonics can be expressed as :

$$f_h = (jm_f \pm k)f_1 \tag{2.29}$$

The fundamental component of the converter line-to-neutral voltage varies linearly with the amplitude modulation ration m_a irrespective of the the frequency modulation ratio m_f as shown in (2.30). Fundamental component of the converter line-to-line voltage is also expressed in (2.31).

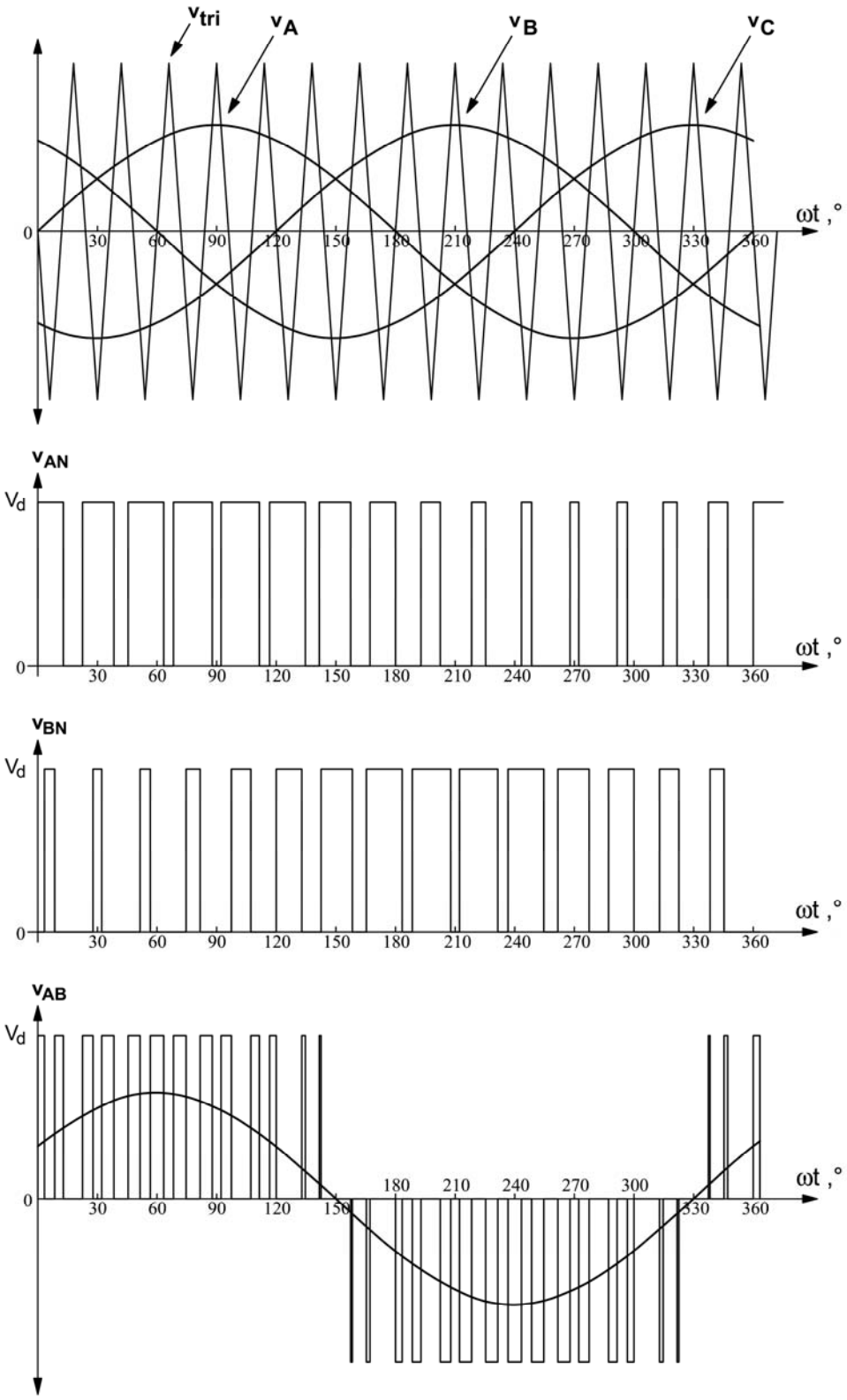


Figure 2.14 Sinusoidal Pulse Width Modulation Technique

$$\left(\hat{V}_{A0}\right)_1 = m_a \frac{V_d}{2} \;;\; m_a \leq 1 \tag{2.30}$$

$$V_{LL1} = \frac{\sqrt{3}}{2\sqrt{2}} m_a V_d = 0.612 m_a V_d \;;\; m_a \leq 1 \tag{2.31}$$

In SPWM, switching harmonics occur in high-frequency range around the switching frequency and its multiples in the linear range. Maximum available amplitude of the fundamental frequency component is $0.612m_aV_d$. However, amplitude of fundamental frequency component is $0.78V_d$ for square wave operation. Therefore, maximum amplitude of fundamental frequency component is reduced in linear range. This problem can be solved by entering into overmodulation region. Overmodulation causes the converter voltage to contain many more harmonics in the side-bands as compared with the linear range. The harmonics with dominant amplitudes in the linear range may not be dominant during overmodulation. However, the amplitude of fundamental frequency component of converter voltage changes nonlinearly with amplitude modulation ratio, m_a and is also dependent on the frequency modulation ratio m_f in overmodulation as given in Fig. 2.15. The relation between fundamental component of line-to-line converter voltage and modulation index for m_f =15 is given in Fig. 2.15 [42].

Linear range can be extended beyond $0 \leq m_a \leq 1$ by including a third harmonic term into the control signals V_A, V_B and V_C. Third harmonic component does not affect line-to-line fundamental converter voltage but it reduces the peak of the control voltages and control voltage are kept lower than triangular reference. Therefore, linear range can be increased to $0 \leq m_a \leq 1.15$ by third-harmonic reference injection [43].

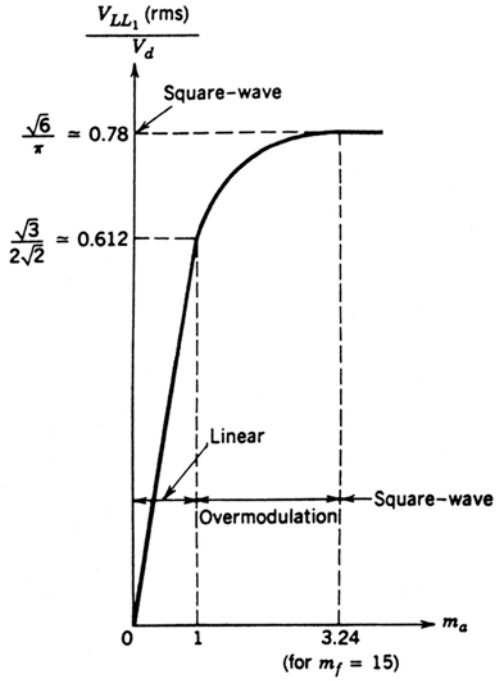


Figure 2.15 Fundamental Component of Line-to-Line Converter Output Voltage versus Modulation Index in SPWM

STATCOM with Constant DC Link Voltage Scheme regulates the DC link voltage to a fixed value in all modes of operation. The constant value of DC link voltage is determined according to highest STATCOM fundamental voltage in the operation range from full inductive to full capacitive mode at minimum and maximum supply voltages.

Therefore, for $0 \leq m_a \leq 1$;

$$V_d \rangle \frac{V_{LL1},max}{0.612} \tag{2.32}$$

STATCOM fundamental voltage is changed by controlling the amplitude modulation ratio in the linear range.

Line-to-line converter voltage harmonics are shown in Fig. 2.16 as a percentage of fundamental voltage.

Amplitude modulation ratio is taken as 0.9 and frequency modulation ratio is taken as 33. Harmonics at m_f and odd multiples are eliminated since m_f is choosen odd and a multiple of 3. Amplitude and frequency modulation ratios are chosen in order to make a comparison between SPWM and 8-Angle SHEM technique which is described in the next subsection (Fig. 2.32).

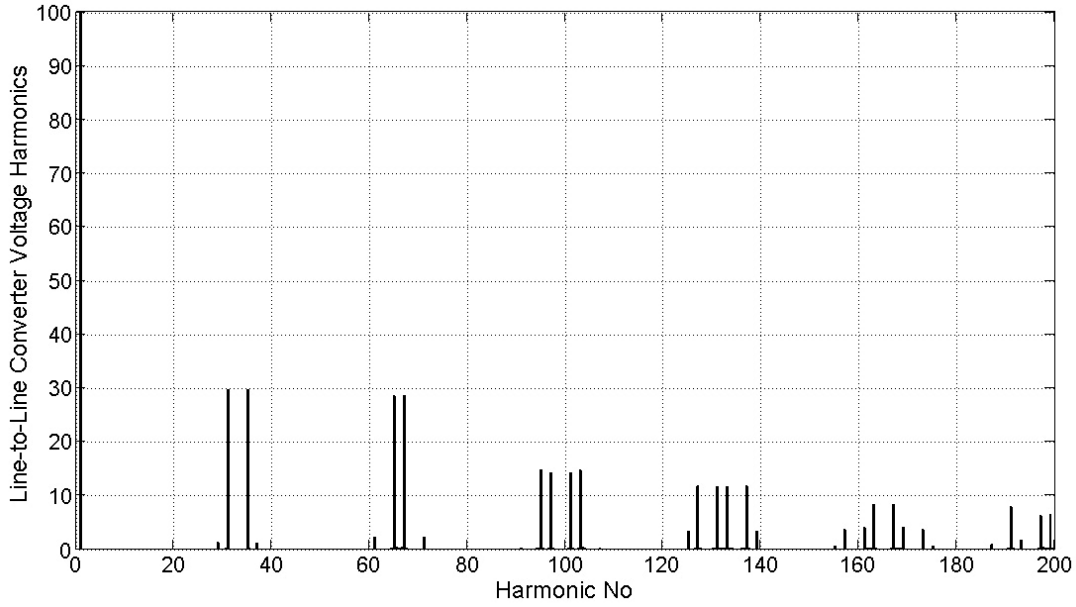


Figure 2.16 Converter Output Voltage Harmonics as a Percentage of Fundamental Component (SPWM with m_a=0.9 and m_f=33)

Voltage harmonics are seen in the sidebands of m_f and multiples of m_f as seen from Fig. 2.16. Switching frequency is found to be 1650 Hz from (2.28). It can be seen from (2.29) that first voltage harmonic is seen at 1550 Hz. Therefore, SPWM technique requires switching frequencies higher than the frequency of first expected dominant voltage harmonic of the line-to-line converter voltage.

2.3.2 Selective Harmonic Elimination Modulation Technique

Selective Harmonic Elimination Modulation (SHEM) technique is based on the elimination of predetermined harmonics and the control of the modulaton index. Available harmonic elimination patterns applicable to three phase inverters are shown in Fig. 2.17 [44].

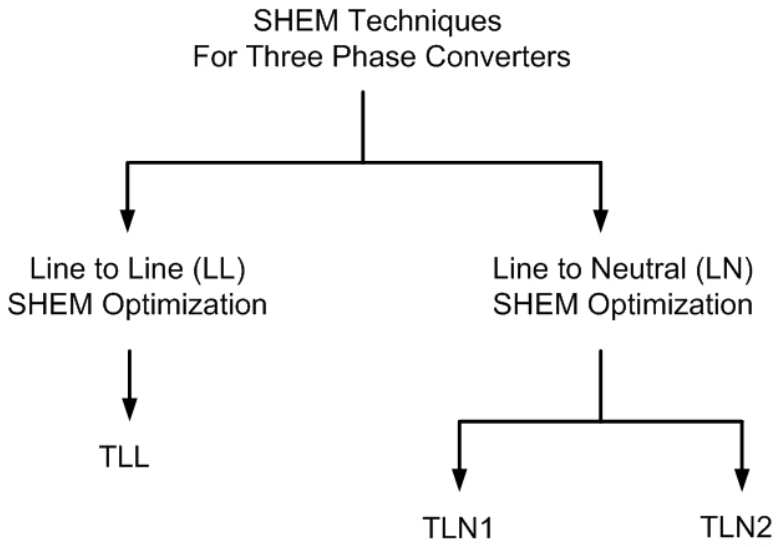


Figure 2.17 SHEM Techniques for Three Phase Converters

TLN1 and TLN2 techniques are based on the elimination of harmonics in line-to-neutral converter output voltages. TLN1 and TLN2 differ only in the odd/even nature of the total number of harmonics to be eliminated. TLL technique is based on the elimination of harmonics directly in the line-to-line converter voltages.
The Fourier expansion of converter voltage is as given below :

$$v(t) = a_v + \sum_{n=1}^{\infty} a_n \cos(nw_o t) + b_n \sin(nw_o t) \qquad (2.33)$$

where

$$a_v = \frac{1}{T}\int_{t_o}^{t_0+T} v(t)dt \tag{2.34}$$

$$a_k = \frac{2}{T}\int_{t_o}^{t_0+T} v(t)\cos(kw_o t)dt \tag{2.35}$$

$$b_k = \frac{2}{T}\int_{t_o}^{t_0+T} v(t)\sin(kw_o t)dt \tag{2.36}$$

TLN1 and TLN2 are used in line-to-neutral SHEM techniques. If fundamental component is also controlled in SHEM, N denotes the sum of the number of harmonics to be eliminated and the fundamental component. TLN1 technique is used if N is odd and TLN2 technique is used if N is even. All triplen harmonics are absent in a three-phase three-wire system and need not be eliminated by SHEM techniques [44].

Fourier coefficients of a quarter-wave and odd symmetric function are as follows :

$$a_v = 0 \tag{2.37}$$

$$a_k = 0 \tag{2.38}$$

$$b_k = 0 \quad \text{for k even} \tag{2.39}$$

$$b_k = \frac{8}{T}\int_{0}^{\frac{T}{4}} v(t)\sin(kw_o t)dt \quad \text{if k is odd} \tag{2.40}$$

2.3.2.1 TLN1 Technique

Line-to-neutral converter voltage (V_{A0}) is shown in Fig. 2.18 for TLN1 technique. This voltage has quarter-wave and odd symmetry.

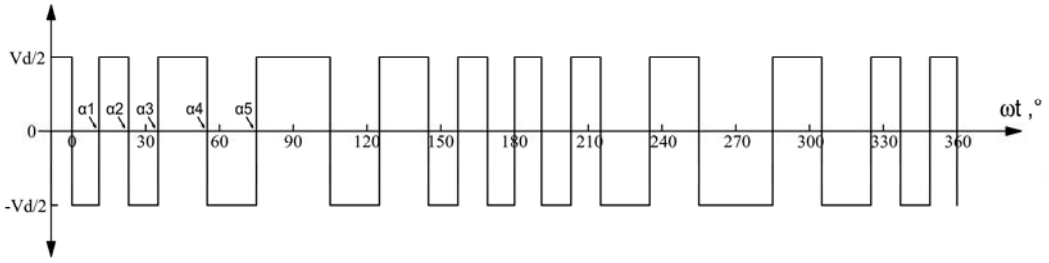


Figure 2.18 Line-to-Neutral Converter Voltage for TLN1 Technique

b_n is found for odd harmonics by using Fig. 2.18 and (2.40).

$$b_n = \frac{4}{n\pi}\left[-1-2\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k)\right] \tag{2.41}$$

(2.41) has N variables (α_1, α_2 , α_3 ,... α_N) and solutions can be found when (N-1) harmonics are set to zero and fundamental component is set to a predetermined value.

$$\begin{bmatrix} 2\cos\alpha_1 & -2\cos\alpha_2 & . & 2(-1)^{N+1}\cos\alpha_N \\ 2\cos5\alpha_1 & -2\cos5\alpha_2 & . & 2(-1)^{N+1}\cos5\alpha_N \\ . & . & . & . \\ . & . & . & . \\ . & . & . & . \\ 2\cos(x_1)\alpha_1 & -2\cos(x_1)\alpha_2 & . & 2(-1)^{N+1}\cos(x_1)\alpha_N \end{bmatrix} . = \begin{bmatrix} 1+\frac{\pi b_1}{4} \\ 1 \\ . \\ . \\ . \\ 1 \end{bmatrix} \tag{2.42}$$

where $x_1 = 3N-2$

$$\alpha_1 < \alpha_2 < \alpha_3 <... \alpha_N < \frac{\pi}{2} \tag{2.43}$$

Converter switching frequency, f_c can be expressed as

$$f_c = (2N+1)f_1 \tag{2.44}$$

where f_1 is the frequency of fundamental component (supply frequency).

Maximum obtainable fundamental converter voltage is 1 p.u. peak for 1 p.u. DC link voltage.

Most significant harmonic voltages in the converter output voltage occur at the frequencies (3N+2) and (3N+4).

N equations found from (2.42) have to be solved simultaneously to obtain the solution. The difficulty is that N equations are nonlinear and can be solved only by iterative methods. Multiple solutions can be found satisfying (2.42) and (2.43).

2.3.2.2 TLN2 Technique

Line-to-neutral converter voltage is shown in Fig. 2.19 for TLN2 technique. This voltage has quarter-wave and odd symmetry.

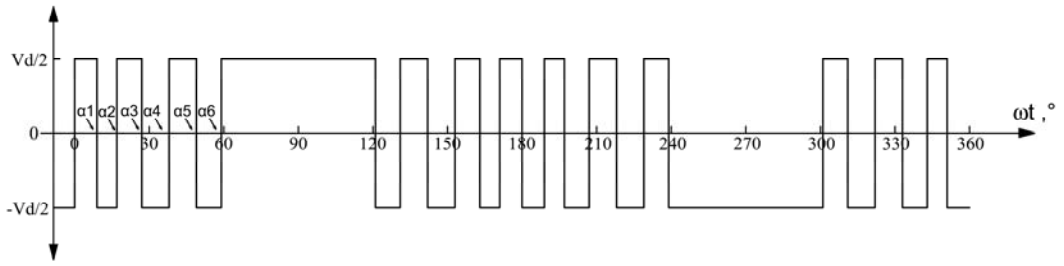


Figure 2.19 Line-to-Neutral Converter Voltage for TLN2 Technique

b_n is found for odd harmonics by using Fig. 2.19 and (2.40).

$$b_n = \frac{4}{n\pi}\left[1 + 2\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k)\right] \tag{2.45}$$

$$\begin{bmatrix} 2\cos\alpha_1 & -2\cos\alpha_2 & . & 2(-1)^{N+1}\cos\alpha_N \\ 2\cos 5\alpha_1 & -2\cos 5\alpha_2 & . & 2(-1)^{N+1}\cos 5\alpha_N \\ . & . & . & . \\ . & . & . & . \\ . & . & . & . \\ 2\cos(x_1)\alpha_1 & -2\cos(x_1)\alpha_2 & . & 2(-1)^{N+1}\cos(x_1)\alpha_N \end{bmatrix} \cdot = \begin{bmatrix} 1-\frac{\pi b_1}{4} \\ 1 \\ . \\ . \\ . \\ 1 \end{bmatrix} \qquad (2.46)$$

where $x_1 = 3N-1$

$$\alpha_1 < \alpha_2 < \alpha_3 < \ldots \alpha_N < \frac{\pi}{3} \qquad (2.47)$$

Maximum obtainable fundamental converter voltage is 1 p.u. peak for 1 p.u. DC link voltage.

Most significant harmonic voltages in the converter voltage occur at the frequencies (3N+1) and (3N+3).

2.3.2.3 TLL Technique

Line-to-line converter voltage is shown in Fig. 2.20 for TLL technique. This voltage has quarter-wave and odd symmetry.

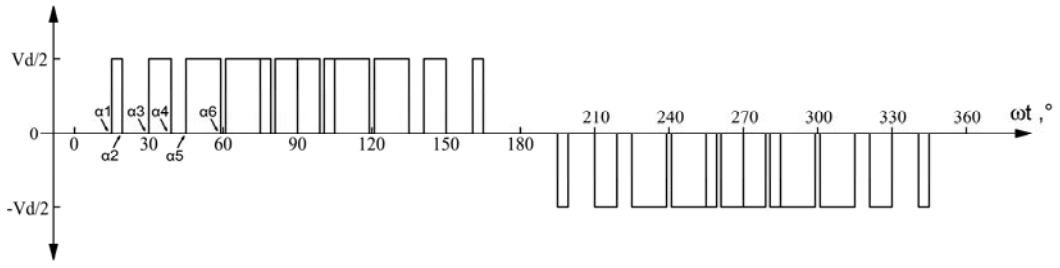


Figure 2.20 Line-to-Line Converter Voltage for TLL Technique

b_n is found for odd harmonics by using Fig. 2.20 and (2.40).

$$b_n = \frac{4}{n\pi}\left[\sum_{k=1}^{2N}(-1)^{k+1}\cos(n\alpha_k)\right] \;;\; \text{N even} \tag{2.48}$$

$$\begin{bmatrix} \cos\alpha_1 & -\cos\alpha_2 & . & -\cos\alpha_{2N} \\ \cos 5\alpha_1 & -\cos 5\alpha_2 & . & -\cos 5\alpha_{2N} \\ . & . & . & . \\ . & . & . & . \\ . & . & . & . \\ \cos(x_1)\alpha_1 & -\cos(x_1)\alpha_2 & . & -\cos(x_1)\alpha_{2N} \end{bmatrix} = \begin{bmatrix} \frac{\pi b_1}{4} \\ 0 \\ . \\ . \\ . \\ 0 \end{bmatrix} \tag{2.49}$$

where $x_1 = 3N - 1$

$$\alpha_1 < \alpha_2 < \alpha_3 < \ldots \alpha_N < \frac{\pi}{3} \tag{2.50}$$

The first 60° interval of the switching pattern is found by solving (2.49) and (2.50). The last 60° interval of the half cycle is the same as the first 60° interval. The 60° to 120° interval is obtained by folding the first and last 60° intervals around the 60° to 120° points. α_{N+1} to α_{2N} are obtained by folding symmetry [44].

Maximum obtainable fundamental converter voltage is 0.85 p.u. peak for 1 p.u. DC link voltage. The reduction in fundamental converter voltage is a disadvantage of VLL technique.

Most significant harmonic voltages in the converter voltage occur at the frequencies (3N+1), (3N+5) and (3N+7).

Lower modulation index in TLL technique causes 18 % increase in DC link voltages in STATCOM operation with phase angle control. Hence, TLN1 and TLN2 techniques are preferred in the optimization of SHEM techniques.

2.3.2.4 Optimization of Number of Harmonics to be Eliminated in the Application Of TLN1 and TLN2 Techniques

Maximum switching frequency of HV IPM IGBT modules is limited at 2 kHz [45] by some power semiconductor manufacturers. This limitation is a result of the optimization between the gate drive circuitry and heat dissipation capability with single side cooling. 1 % converter loss is achieved with the switching frequencies around 1kHz [46]. Therefore, well known applications of HV IGBT modules uses switching frequencies in the range of 800 Hz-2 kHz [15, 41]. Hence, 7 degree SHEM, 9 degree SHEM and 11 degree SHEM are compared to find the optimum switching pattern for HV IGBT modules.

SHEM equations given in (2.42) or (2.46) are to be solved for each case. $\alpha_1 ... \alpha_N$ are broadly found by a hybrid optimization method that uses genetic algorithm as the first phase of the solution and then Matlab`s gradient based constraint optimization method is used for fine tuning. Gradient based methods converge fast, however, it can easily be trapped at the local minima. Choosing correct initial conditions is important to reach global minima. Genetic algorithm is a well known optimization method that always converges to global minima as it can escape from local minima because of its stochastic nature. The problem here is that genetic algorithm converges more slowly than gradient based methods. Therefore, a hybrid algorithm is developed that uses genetic algorithm to find a good initial condition and gradient based method is used with this condition point to reach the minima faster.

The following equations are used in the optimization process.

$$\left|b_1 - m_a\right| \le err_1 \tag{2.51}$$

$$\left|b_n\right| \le err_2 \quad n \ge 5 \tag{2.52}$$

where n denotes the number of harmonics to be eliminated.

The design flowchart for the solution of SHEM equations is given in Fig. 2.21.

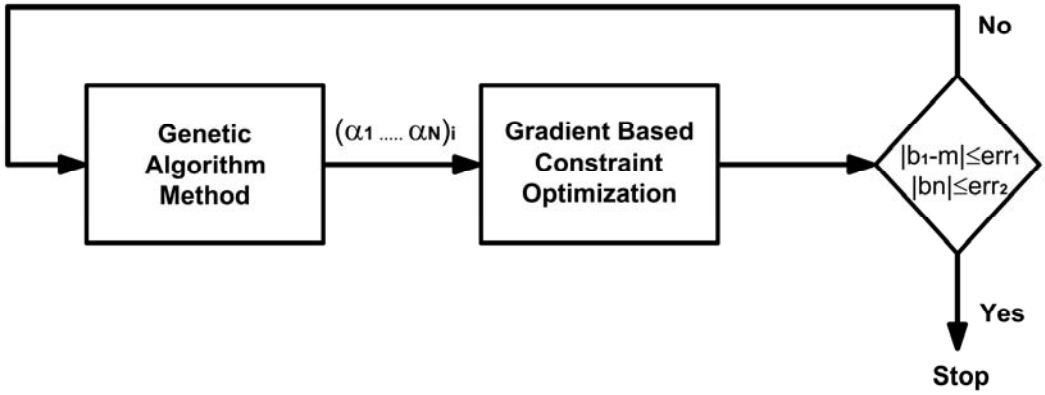


Figure 2.21 Design Flowchart for the Solutions of SHEM Equations

err_1 and err_2 are set to 10^{-3} in the calculations. However, err_1 and err_2 are increased if no solutions exist.

Line-to-neutral converter peak fundamental voltage is found as follows :

$$\hat{V}_{AN} = b_1 \frac{V_d}{2} \tag{2.53}$$

It is seen from (2.16) and (2.53) that b_1 stands for the modulation index (m_a) of the SHEM technique. The value of the modulation index is 1.273 ($4/\pi$) for square wave operation. There is a maximum modulation index that can be obtained by each SHEM technique and this value is always smaller than 1.273. This is a natural result of the notches in the line-to-line converter voltage.

2.3.2.4.1 Minimum Pulse Width Constraint

2 level, 3 leg Voltage Source Converter can be thought as 3 'One Leg Converter' connected to each phase. 'One Leg Converter' is shown in Fig. 2.22.

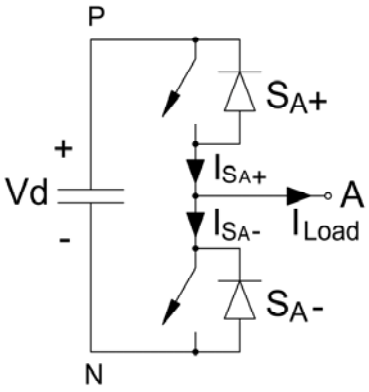


Figure 2.22 One-Leg Converter

When the load current is positive, if S_{A+} is switched on, IGBT part of S_{A+} carries the load current. If S_{A+} is switched off and S_{A-} is switched on, load current diverges to the FWD of S_{A-}. Therefore, if the load current is positive, FWD of S_{A-} carries the load current during on the period of S_{A-} switching pulse.

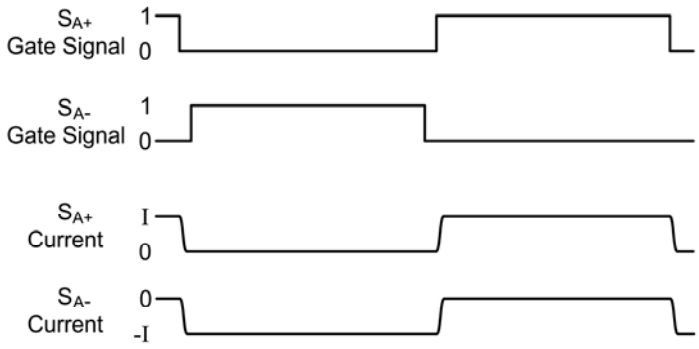


Figure 2.23 S_{A+} and S_{A-} Switch Waveforms for Positive Load Current

When the load current is negative, if S_{A-} is switched on, IGBT part of S_{A-} carries the load current. If S_{A-} is switched off and S_{A+} is switched on, load current diverges to the FWD of S_{A+}. Therefore, if the load current is negative, FWD of S_{A+} carries the load current during on the period of S_{A+} switching pulse.

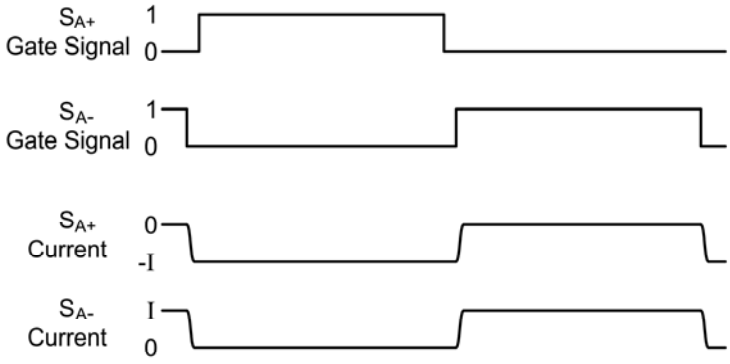


Figure 2.24 S_{A+} and S_{A-} Switch Waveforms for Negative Load Current

As seen from Fig. 2.23 and Fig. 2.24, the minimum on-time of the FWD part of HV IGBT module is equal to the minimum on-time of IGBT part.

The minimum on-time of the FWD part of the HV IGBT module is important. Because, in case of short on-times when charges are still built in, e.g. the turn-on process is not really finalized, application of a reverse bias may cause high electric field strength inside the diode in addition to an oscillation in diode anode-cathode voltage waveform. This might generate also a very bad EMI. Hence, minimum on-time of freewheeling diode must be kept much larger than the reverse recovery time of FWD. Therefore, minimum on-time of FWD which is equivalent to minimum on- time of IGBT part is taken as 16.5 μs (0.3º) in the optimization of SHEM techniques.

2.3.2.4.2 7-Angle SHEM Technique

Modulation index for 7-Angle SHEM technique is given below:

$$m_a = \frac{4}{\pi}\begin{bmatrix} -1 + 2\cos\alpha_1 - 2\cos\alpha_2 + 2\cos\alpha_3 - 2\cos\alpha_4 \\ +2\cos\alpha_5 - 2\cos\alpha_6 + 2\cos\alpha_7 \end{bmatrix} \tag{2.54}$$

Modulation index is changed between 0.1 p.u. and 0.95 p.u and 5^{th}, 7^{th}, 11^{th}, 13^{nd}, 17^{th}, 19^{th} harmonics are eliminated in the calculations. Chopping angles as a function of modulation index (p.u.) are found as shown in Fig. 2.25.

$$\text{Modulation Index (p.u.)} = \frac{\text{Modulation Index}}{1.273} \tag{2.55}$$

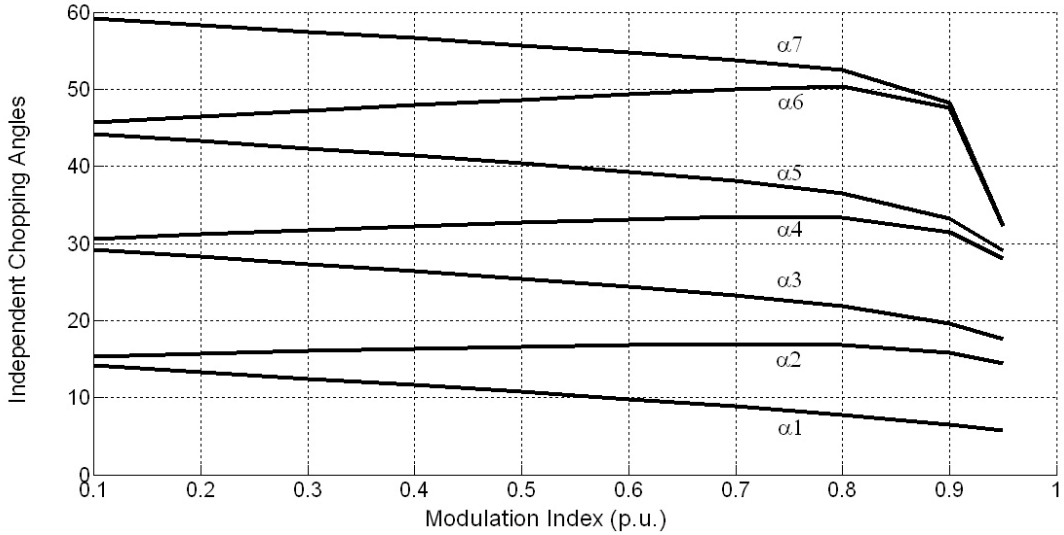


Figure 2.25 Independent Chopping Angles versus. p.u. Modulation Index (N=7)

Table 2.2 shows the duration of independent pulses in each switching pattern for different modulation indices.

Chopping angles found for m_a = 0.95 p.u. can not satisfy Minimum Pulse Width Constraint and must not be used as the chopping angles set.

Line-to-line converter voltage harmonics are shown in Fig. 2.26 as a percentage of fundamental voltage (m_a = 0.9 p.u.). Triplen harmonics do not exist in line-to-line voltage although they exist in line-to-neutral voltages. Most significant voltage harmonics occur at 23^{rd} and 25^{th} components as expected. The switching frequency is 750 Hz for 7-Angle SHEM Technique.

Table 2.2 The duration of independent pulses in switching patterns with respect to p.u. modulation index (N=7)

T_i (º)	Modulation Index (p.u.)									
	0.1	**0.2**	**0.3**	**0.4**	**0.5**	**0.6**	**0.7**	**0.8**	**0.9**	**0.95**
T_1	14.2	13.3	12.5	11.6	10.7	9.8	8.8	7.8	6.5	5.7
T_2	1.2	2.4	3.5	4.7	5.9	7	8.1	9	9.3	7.6
T_3	13.8	12.6	11.3	10.1	8.8	7.6	6.3	5.1	3.8	3.2
T_4	1.4	2.9	4.3	5.8	7.3	8.8	10.2	11.5	11.8	10.5
T_5	13.5	12.1	10.6	9.2	7.7	6.2	4.7	3.2	1.8	1
T_6	1.6	3.2	4.9	6.5	8.2	10	11.8	13.8	14.4	3.1
T_7	13.4	11.9	10.3	8.7	7.1	5.5	3.8	2.2	0.5	0.03
T_8	61.6	63.3	65.1	66.8	68.6	70.4	72.5	75	83.7	115.6

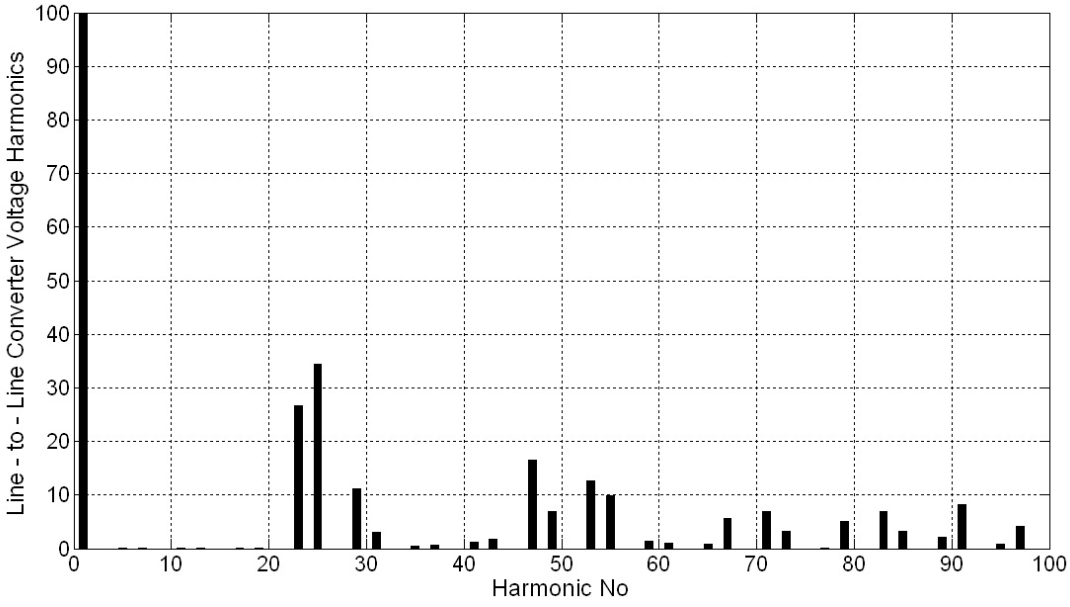


Figure 2.26 Line-to-Line Converter Voltage Harmonics as a Percentage of Fundamental Component (N=7)

2.3.2.4.3 9-Angle SHEM Technique

Modulation index is changed between 0.1 p.u. and 0.95 p.u and 5^{th}, 7^{th}, 11^{th}, 13^{nd}, 17^{th}, 19^{th} ,23^{rd}, 25^{th} harmonics are eliminated in the calculations. Chopping angles as a function of modulation index (p.u.) are found as shown in Fig. 2.27.

$$m_a = \frac{4}{\pi}\begin{bmatrix} -1+2\cos\alpha_1 - 2\cos\alpha_2 + 2\cos\alpha_3 - 2\cos\alpha_4 + 2\cos\alpha_5 \\ -2\cos\alpha_6 + 2\cos\alpha_7 - 2\cos\alpha_8 + 2\cos\alpha_9 \end{bmatrix} \tag{2.56}$$

Table 2.3 shows the duration of independent pulses in each switching pattern for different modulation indexes. Solutions for $m_a = 0.95$ satisfy Minimum Pulse Width Constraint. However, err_1 and err_2 tolerances are made 0.02 to find a solution.

Line-to-line converter voltage harmonics are shown in Fig. 2.28 as a percentage of fundamental voltage ($m_a = 0.9$ p.u.). Most significant voltage harmonics occur at 29^{th} and 31^{st}components as expected. The switching frequency is 950 Hz for 9-Angle SHEM Technique.

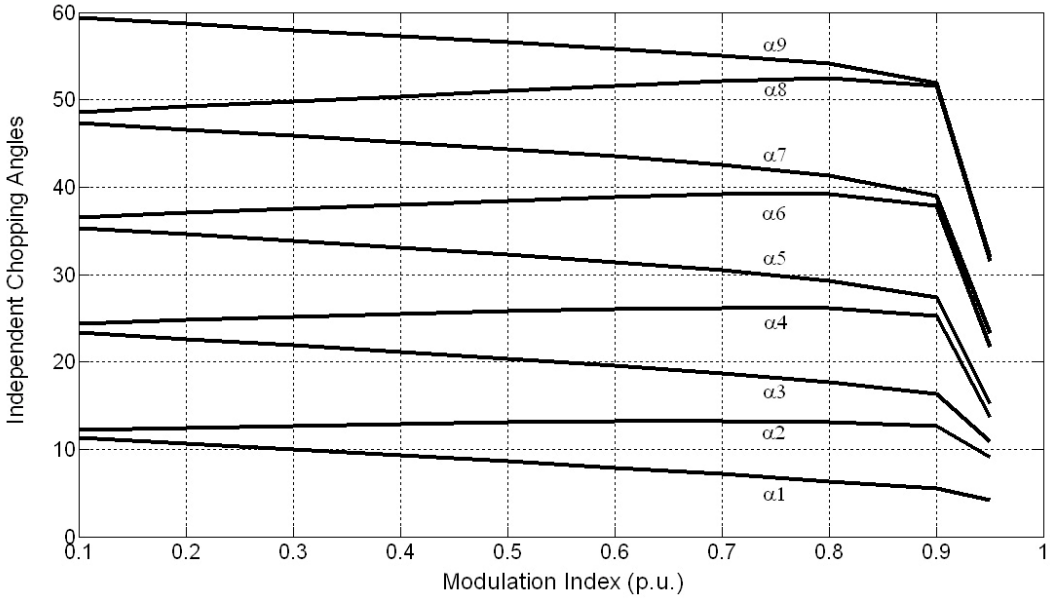


Figure 2.27 Independent Chopping Angles versus p.u. Modulation Index (N=9)

Table 2.3 The duration of independent pulses in switching patterns with respect to p.u. Modulation Index (N=9)

T_i (°)	Modulation Index (p.u.)									
	0.1	**0.2**	**0.3**	**0.4**	**0.5**	**0.6**	**0.7**	**0.8**	**0.9**	**0.95**
T_1	11.3	10.7	10	9.3	8.6	7.9	7.2	6.4	5.5	4.2
T_2	0.9	1.8	2.7	3.6	4.4	5.3	6.1	6.8	7.2	4.9
T_3	11.1	10.2	9.2	8.3	7.4	6.4	5.5	4.5	3.6	1.8
T_4	1.1	2.2	3.2	4.3	5.4	6.5	7.5	8.4	8.9	2.8
T_5	10.9	9.8	8.7	7.6	6.5	5.4	4.3	3.2	2.2	1.5
T_6	1.2	2.4	3.7	4.9	6.2	7.4	8.7	9.9	10.5	6.6
T_7	10.8	9.6	8.3	7.1	5.9	4.7	3.4	2.2	1.1	1.5
T_8	1.3	2.6	3.9	5.3	6.6	8.1	9.5	11.2	12.6	8.2
T_9	10.7	9.5	8.2	6.9	5.6	4.3	3	1.6	0.4	0.5
T_{10}	61.3	62.7	64	65.4	66.8	68.3	69.8	71.7	76.1	116.2

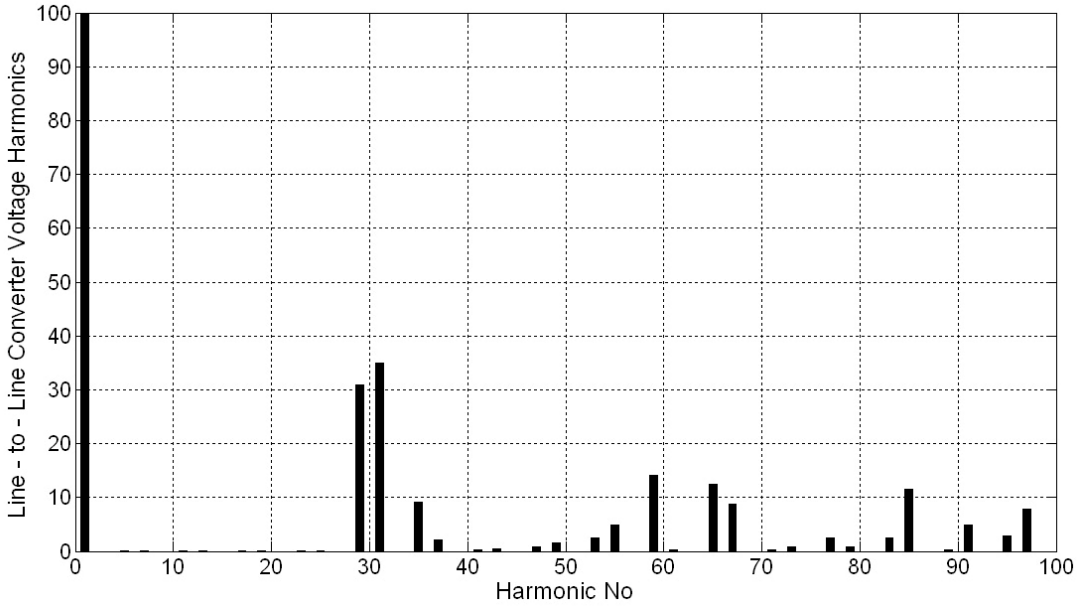


Figure 2.28 Line-to-Line Converter Voltage Harmonics as a Percentage of Fundamental Component (N=9)

2.3.2.4.4 11-Angle SHEM Technique

Modulation index is changed between 0.1 p.u. and 0.95 p.u and 5^{th}, 7^{th}, 11^{th}, 13^{nd}, 17^{th}, 19^{th} ,23^{rd}, 25^{th} ,29^{rd}, 31^{st} harmonics are eliminated in the calculations. Chopping angles as a function of modulation index (p.u.) are found as shown in Fig. 2.29.

$$m_a = \frac{4}{\pi}\begin{bmatrix} -1+2\cos\alpha_1 - 2\cos\alpha_2 + 2\cos\alpha_3 - 2\cos\alpha_4 + 2\cos\alpha_5 - 2\cos\alpha_6 \\ +2\cos\alpha_7 - 2\cos\alpha_8 + 2\cos\alpha_9 - 2\cos\alpha_{10} + 2\cos\alpha_{11} \end{bmatrix} \quad (2.57)$$

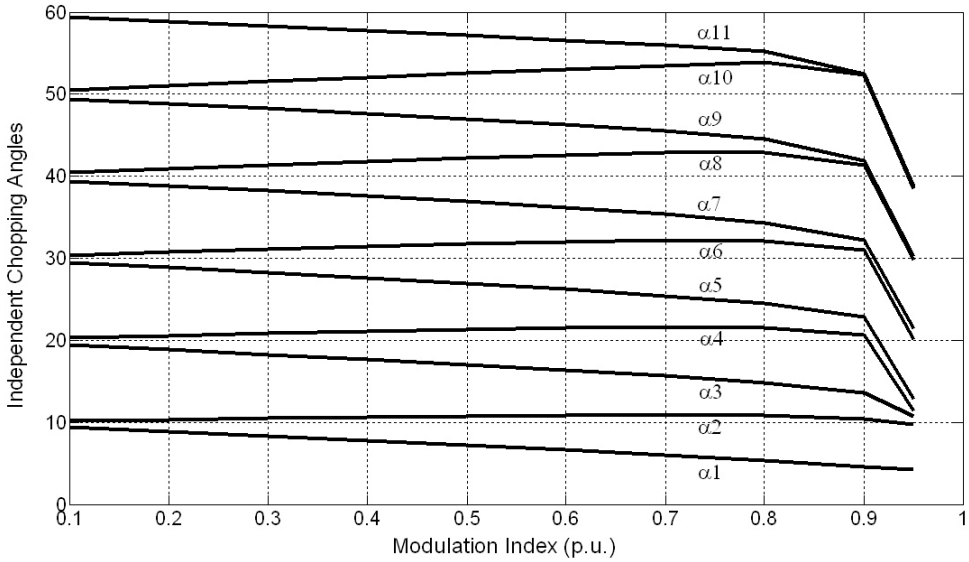


Figure 2.29 Independent Chopping Angles versus. p.u. Modulation Index (N = 11)

Table 2.4 shows the duration of independent pulses in each switching pattern for different modulation indexes. Solutions m_a = 0.9 and m_a = 0.95 can not satisfy minimum pulse width criteria.

Line-line converter voltage harmonics are shown in Fig. 2.30 as a percentage of fundamental voltage (m_a = 0.9 p.u.). Most significant voltage harmonics occur at 35^{th} and 37^{th} components as expected. The switching frequency is 1150 Hz for 11-Angle SHEM Technique.

Table 2.4 The duration of independent pulses in switching patterns with respect to Modulation Index (p.u.). (N=11)

T_i (°)	Modulation Index (p.u.)									
	0.1	**0.2**	**0.3**	**0.4**	**0.5**	**0.6**	**0.7**	**0.8**	**0.9**	**0.95**
T_1	9.5	8.9	8.3	7.8	7.2	6.6	6	5.4	4.6	4.2
T_2	0.7	1.4	2.2	2.8	3.5	4.2	4.8	5.5	5.8	5.5
T_3	9.3	8.5	7.8	7.1	6.3	5.5	4.8	4	3.3	1.1
T_4	0.8	1.7	2.5	3.4	4.2	5.08	5.9	6.6	7	0.6
T_5	9.1	8.3	7.4	6.5	5.6	4.8	3.9	3	2.2	1.5
T_6	1	1.9	2.8	3.8	4.8	5.8	6.8	7.7	8.1	7.2
T_7	9	8.1	7.1	6.1	5.1	4.2	3.2	2.2	1.3	1.3
T_8	1	2.1	3.1	4.2	5.3	6.4	7.5	8.6	9.1	8.3
T_9	9	7.9	6.9	5.9	4.8	3.7	2.7	1.6	0.6	0.5
T_{10}	1.1	2.2	3.3	4.4	5.5	6.7	7.9	9.3	10.4	8.3
T_{11}	8.9	7.9	6.8	5.7	4.6	3.5	2.5	1.3	0.2	0.2
T_{12}	61.1	62.2	63.4	64.5	65.6	66.8	68.1	69.6	75	102.6

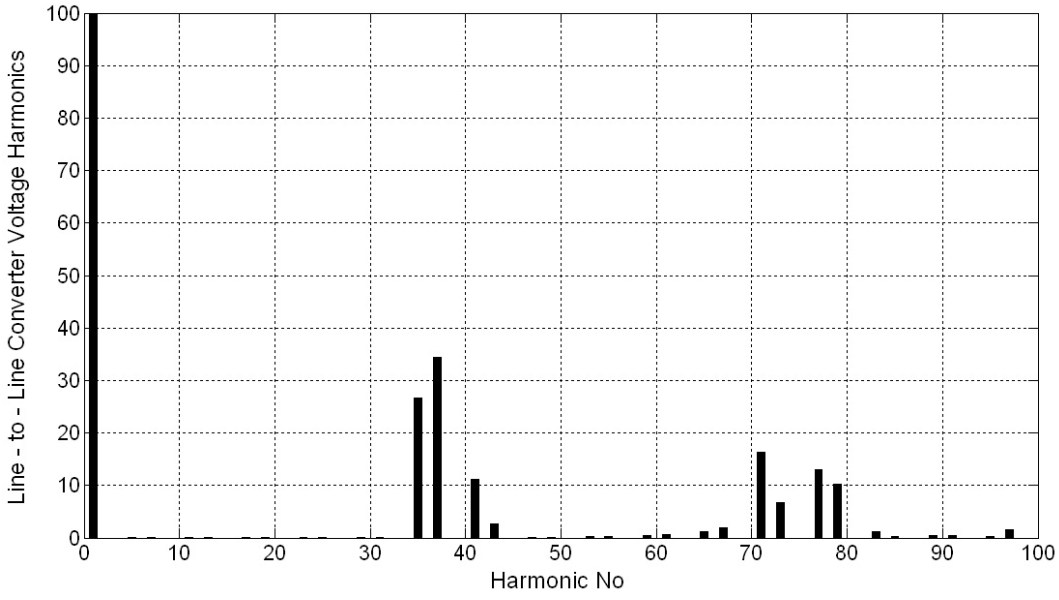


Figure 2.30 Line-to-Line Converter Voltage Harmonics as a Percentage of Fundamental Component (N=11)

Constraints in (2.51) and (2.52) (err_1 and err_2) are set to 10^{-3} to find a solution for these nonlinear equations. However, these constraints are increased to 10^{-2} if a solution can not be found. This deteriorates the success of the harmonic elimination method since the harmonic content of line-to-line converter voltage is not zero at the eliminated harmonics.

An optimum SHEM technique is chosen in view of the following constraints.

1) For the safe operation of HV IGBT modules, the duration of each pulse should be at least 16.5 μs as a result of Miminum Pulse Width Constraint.
2) DC link voltage increases as the modulation index decreases for a predetermined value of generated reactive power. Higher DC link voltages cause higher switching losses in HV IGBT modules. Lower modulation index increases the size of input filter for the same TDD specification as can be seen from (3.42) and (3.52).
3) TDD of the line current is decreased by using a higher number of chopping angles. However, switching losses of HV IGBT modules increases also with higher number of chopping angles.
4) Dead time causes harmonics in the line-to-line converter voltage at every odd harmonic irrespective of the harmonic elimination method. Magnitude of these voltage harmonics increases with switching frequency.

Solutions for m_a = 0.95 p.u are eliminated because of constraint 1. Modulation index is chosen 0.9 p.u by considering first and second constraint given above.

STATCOM line current TDD of the discussed SHEM techniques with respect to input filter corner frequency is given in Fig. 2.31.

9-Angle SHEM technique (5^{th}, 7^{th}, 11^{th}, 13^{nd}, 17^{th}, 19^{th} ,23^{rd}, 25^{th} harmonics elimination with modulation index control is chosen as the optimum solution by considering constraint 3 and Fig. 2.31.

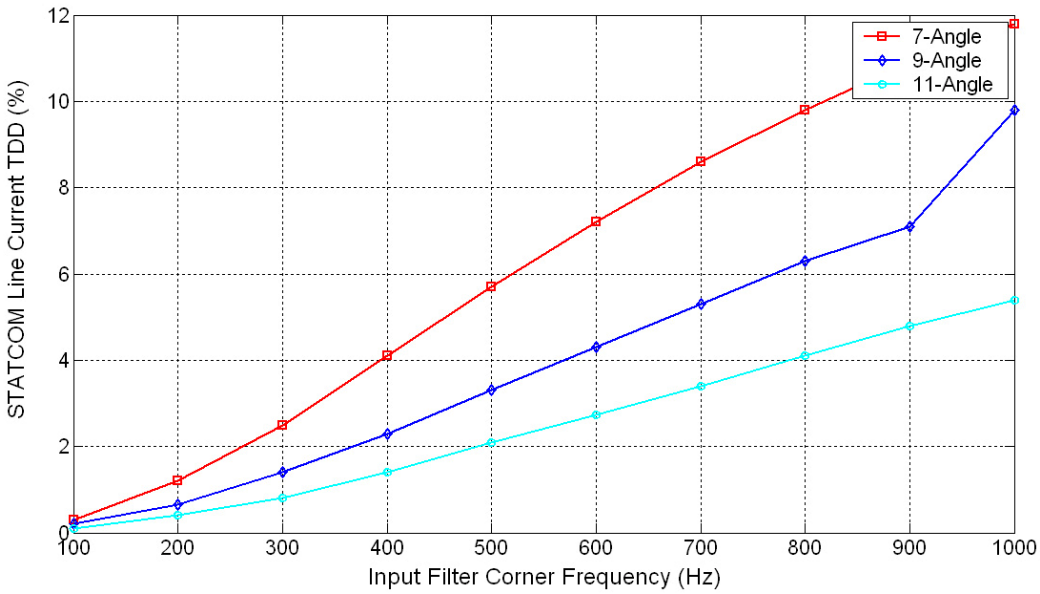


Figure 2.31 STATCOM Line Current TDD for different SHEM Techniques

Elimination of 8 harmonics (5^{th}, 7^{th}, 11^{th}, 13^{nd}, 17^{th}, 19^{th} ,23^{rd}, 25^{th} harmonics) with m_a = 0.9 p.u is chosen as the optimum TLN1 technique.

TLN2 technique is solved for 8 harmonics elimination with no constraint on the modulation index. The solutions are analyzed if there is a solution having a modulation index around 0.9 p.u. The aim is to find 8-Angle TLN2 technique which gives the same harmonic spectra with 9-Angle TLN1 technique. If this can be achieved, the switching frequency is reduced from 950 Hz to 850 Hz. The following chopping angles are found with a modulation index of 0.91 p.u for 8-Angle TLN2 technique.

Table 2.5 Chopping Angles for 8-Angle SHEM Technique

α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8
6.194	10.456	18.407	21.057	30.498	31.864	42.449	42.915

Chopping angles in Table 2.5 satisfy Minimum Pulse Width Constraint. The harmonic spectrum is shown in Fig. 2.32 and converter voltages are shown in Fig. 2.33.

Line-to-neutral and line-to-line converter fundamental voltages are expressed in terms of modulation index and DC link voltage as below :

$$V_{statcom\,L-N} = \frac{m_a}{2} \times V_d \times \frac{1}{\sqrt{2}} = \frac{m_a}{2\sqrt{2}} V_d = 0.35 m_a V_d \tag{2.58}$$

$$V_{statcom\,L-L} = \frac{m_a \sqrt{3}}{2\sqrt{2}} V_d = 0.612 m_a V_d \tag{2.59}$$

m_a is found as 1.16 from (2.55).

Therefore;

$$V_{statcom\,L-N} = 0.4103 V_d \tag{2.60}$$

$$V_{statcom\,L-L} = 0.7107 V_d \tag{2.61}$$

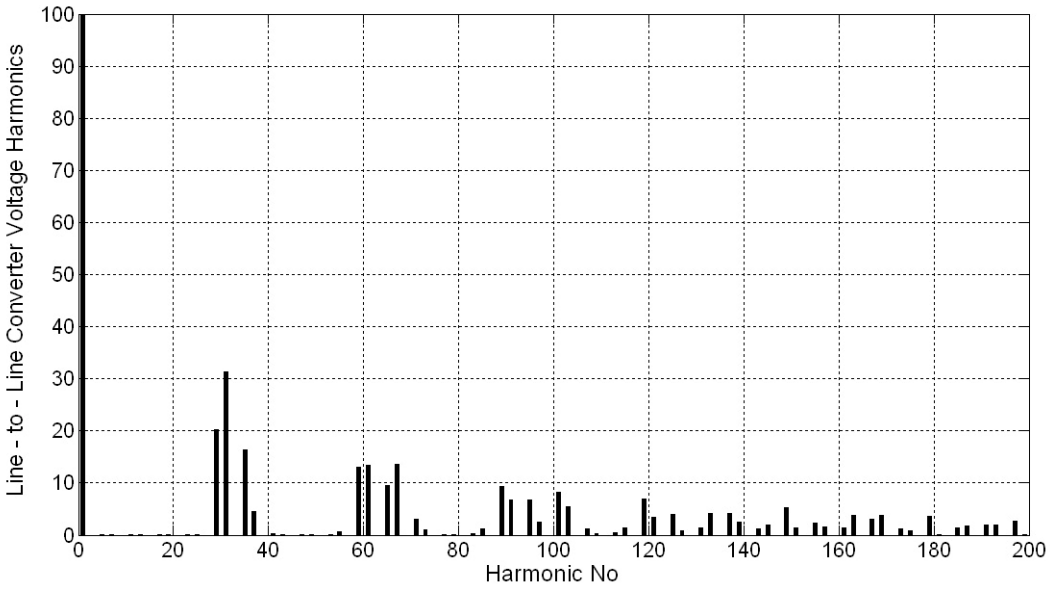


Figure 2.32 Line-to-Line Converter Voltage Harmonics as a Percentage of Fundamental Component (N=8)

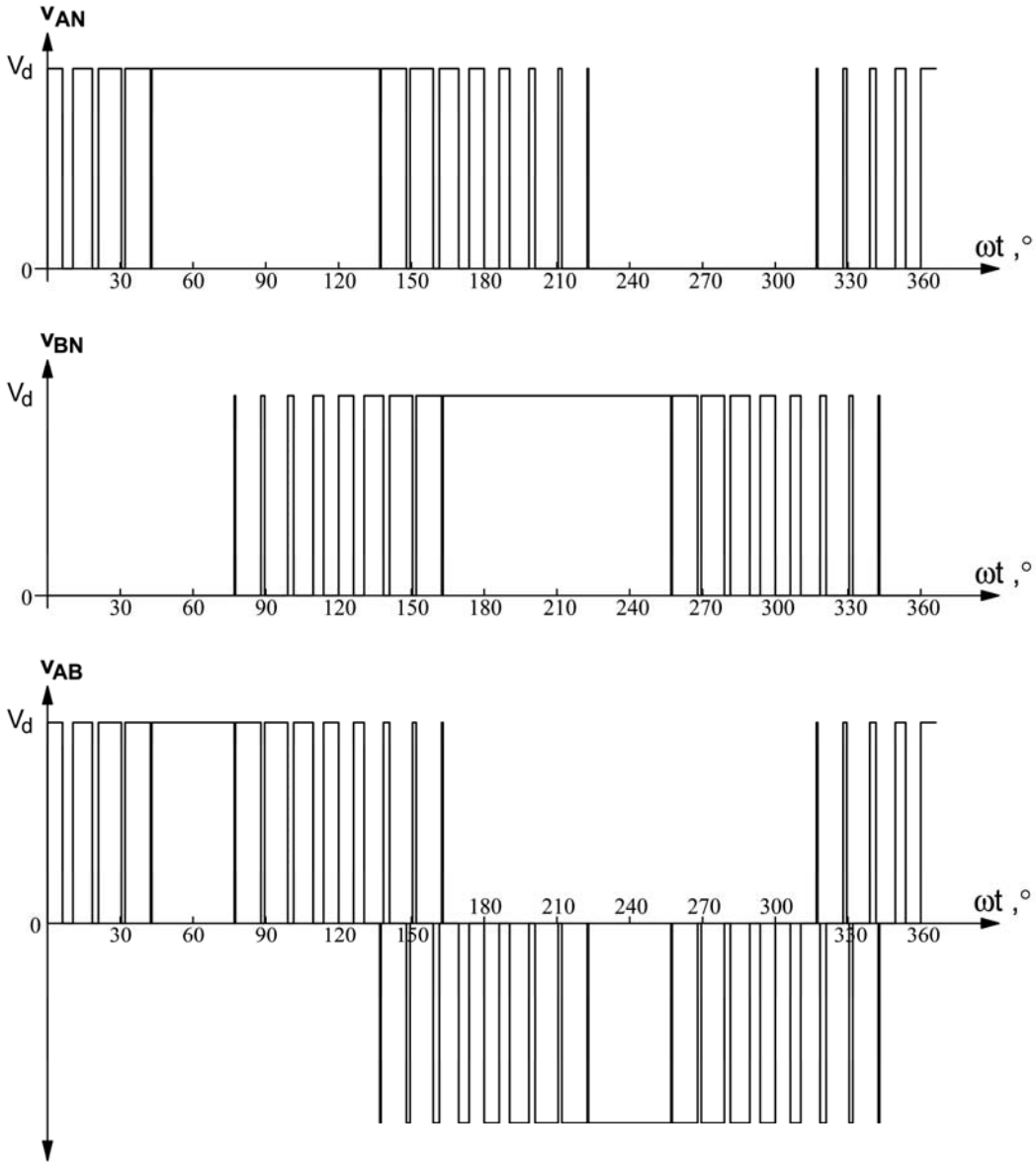


Figure 2.33 Converter Voltages for 8-Angle SHEM

2.3.3 Selection of the Optimum Modulation Technique

SPWM and SHEM techniques are studied for VSC STATCOM. Both techniques are analysed for the elimination of 5^{th}, 7^{th}, 11^{th}, 13^{nd}, 17^{th}, 19^{th} ,23^{rd}, 25^{th} harmonics.

SPWM technique employs a switching frequency of 1650 Hz in order to eliminate the eight harmonics given above. First dominant harmonic is seen at 1550 Hz as shown in Fig. 2.16.

However, 8-Angle TLN2 SHEM technique employs a switching frequency of 850 Hz in order to eliminate the eight harmonics. First dominant harmonic is seen at 1450 Hz as shown in Fig. 2.28. Therefore, switching frequency is reduced approximately by 50 % using SHEM technique for the same TDD level.

SHEM technique has superior advantages than SPWM technique when switching frequency and harmonic spectra optimization are considered. Switching frquency optimization is especially very important for HV IGBT modules where switching losses at higher frequencies are not optimised yet as in LV IGBT modules.

Phase Angle Control is used in the implementation as described in Chapter 3. Phase angle control does not require the control of modulation index and modulation index is kept constant during the operation of VSC STATCOM. Reactive power delivered or absorbed is controlled by changing DC link voltage. Hence, SHEM technique is better suited for Phase Angle Control than the SPWM technique.

Considering the points discussed above, 8-Angle SHEM technique is used in the implementation.

2.4 Reactive Power Measurement

The response of reactive power measurement block is effective on the step response of STATCOM. Reactive power is measured by using Average Basis Concept or Instantaneous pq Theory. Average Basis Concept measures reactive power at discrete time periods. However, Instantaneous pq Theory calculates the reactive power without any averaging process and gives a faster reactive power

measurement. STATCOMs having a step response smaller than 2 period must use Instantaneous pq Theory. However, Averaging Basis Concept based reactive power measurement can be used when slower responses are needed with STATCOM.

2.4.1 Average Basis Concept

AC busbar current of a non-linear load current is modelled as given below [1] :

$$i(t) = I_o+I_1\sin(wt+\theta_1)+I_5\sin(5wt+\theta_5)+I_7\sin(7wt+\theta_7)+... \quad (2.62)$$

$$v(t) = V_o\cos(wt); \quad (2.63)$$

$$Q(t)= I_oV_o\cos(wt)+ I_1V_o\cos(wt)\sin(wt+\theta_1)+I_5V_o\cos(wt)\sin(5wt+\theta_5)+... \quad (2.64)$$

$$\int_0^T Q(t)dt = \frac{I_1V_0\sin(\theta_1)}{2} \quad ; \ T = 10ms \quad (2.65)$$

Average of the reactive power of harmonics over half fundamental period is zero and do not contribute to any reactive power assuming that ac busbar voltage does not contain any significant harmonics. Instantaneous line reactive powers for each phase are formed as follows:

$$Q_a = i_a v_{bc} \quad (2.66)$$

$$Q_b = i_b v_{ca} \quad (2.67)$$

$$Q_c = i_c v_{ab} \quad (2.68)$$

Instantaneous line reactive powers are processed in an integral unit, output is sampled in every 10 msec, sampled output is hold and and the integral process is reset for the next 10 msec. The output is used as the reactive power signal in the control system.

2.4.2 Instantaneous pq Theory

Instantaneous pq Theory uses a generalised definition of Instantaneous real and imaginary power which is true for all three phase sytems having nonsinusoidal, unbalanced or zero sequence components [40].

Instantaneous pq Theory uses α-β coordinates. Hence, three phase voltages and currents have to be transformed to α-β coordinates.

$$C = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{2.69}$$

$$\begin{bmatrix} v_\alpha \\ v\beta \\ v_0 \end{bmatrix} = C\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}; \qquad \begin{bmatrix} i_\alpha \\ i\beta \\ i_0 \end{bmatrix} = C\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.70}$$

Instantaneous real power and instantenous imaginary power is defined below :

$$p = v_a i_a + v_b i_b + v_c i_c = v_\alpha i_\alpha + v_\beta i_\beta + v_0 i_0 \tag{2.71}$$

$$q = v_\alpha i_\beta - v_\beta i_\alpha \tag{2.72}$$

q can be re-writen in terms of abc components.

$$q = -\frac{1}{\sqrt{3}}\left[(v_a - v_b)i_c + (v_b - v_c)i_a + (v_c - v_a)i_b\right] \tag{2.73}$$

(2.73) is the expression used in the measurement of conventional three phase reactive power when only fundamental frequency is considered. The variable in α-β frame takes into account all the frequency components in voltages and currents. This is the reason q is defined as instantaneous imaginary power. It is seen from (2.73) that q is not influenced by zero sequence components [40].

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.74}$$

It is shown in [40] that

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} i_{\alpha p} \\ i_{\beta p} \end{bmatrix} + \begin{bmatrix} i_{\alpha q} \\ i_{\beta q} \end{bmatrix} \tag{2.75}$$

where

α-axis instantaneous active current : $$i_{\alpha p} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2} p \tag{2.76}$$

α-axis instantaneous reactive current : $$i_{\alpha q} = \frac{-v_\beta}{v_\alpha^2 + v_\beta^2} q \tag{2.77}$$

β-axis instantaneous active current : $$i_{\beta p} = \frac{v_\beta}{v_\alpha^2 + v_\beta^2} p \tag{2.78}$$

β -axis instantaneous reactive current : $$i_{\beta q} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2} q \tag{2.79}$$

$$i_\alpha = \underbrace{\frac{v_\alpha}{v_\alpha^2 + v_\beta^2} \bar{p}}_{(1)} + \underbrace{\frac{v_\alpha}{v_\alpha^2 + v_\beta^2} \tilde{p}}_{(2)} + \underbrace{\frac{-v_\beta}{v_\alpha^2 + v_\beta^2} \bar{q}}_{(3)} + \underbrace{\frac{-v_\beta}{v_\alpha^2 + v_\beta^2} \tilde{q}}_{(4)} \tag{2.80}$$

$\bar{p}$ and $\tilde{p}$ are the fundamental and harmonic components of the instantaneous real power. $\bar{q}$ and $\tilde{q}$ are the fundamental and harmonic components of the instantenous imaginary power.

The first term in (2.80) is the instantaneous value of conventional fundamental active current.

The second term in (2.80) is the instantaneous value of the harmonic currents which represent the ac component of the instantaneous real power.

The third term in (2.80) is the instantaneous value of conventional fundamental reactive current.

The fourth term in (2.80) is the instantaneous value of the harmonic currents which represent the ac component of the instantaneous imaginary power.

STATCOM makes the displacement factor unity in steady state by compensating the third term.

STATCOM makes the displacement factor unity also in transient states by compensating the third and fourth terms.

CHAPTER 3

DESIGN OF VOLTAGE SOURCE CONVERTER BASED STATCOM

3.1 Design Specifications

A prototype VSC based D-STATCOM employing 8-Angle SHEM technique and having simplest converter topology with HV IGBT modules (2 level, 3 leg) is designed. Prototype testing of the designed VSC STATCOM is performed in Kemerköy Thermal Power Plant to solve the reactive power compensation problem of Coal Preparation System.

Conveyor belts are used in coal mines and thermal power plants for the preparation and transportation of coal. They are driven by different types of motor drives ranging from traditional induction motor drives to unity power factor ac motor drives [47]. The major power quality problems arising from these drives are:

- very low power factors, and high starting currents for conventional drives
- current harmonics injected into the supply for old generation static drives

These problems can be solved partially by permanently connected capacitor banks and circuit breaker or contactor-switched shunt, passive filters. However, a complete solution to such problems makes necessary the use of fully-static or hybrid systems such as thyristor controlled reactor based SVCs, D-STATCOMs and/or active/hybrid power filters.

The layout diagram of the coal conveyor belts which are used for the preparation and transportation of coal from Yeniköy Open-cast Lignite Mines to Kemerkoy Thermal Power Plant is given in Fig. 3.1. These are driven by conventional induction motor drives of both types (squirrel-cage motors and wound-rotor

induction motors with external rotor resistance control for starting and direct current injection for braking).

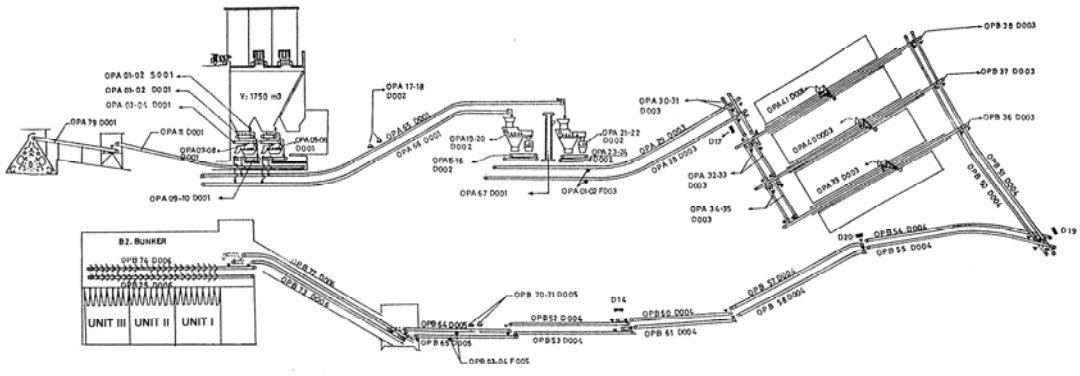


Figure 3.1 Layout of Conveyor Belts

Each section of conveyor belt system is either uphill, downhill, or mixed as shown in Fig. 3.2.

Figure 3.2 General View of Conveyor Belts

The power ratings of 0.4 kV, 50 Hz motors are ranging from 10 to 55 kW, while 6.3 kV, 50 Hz motors from 250 to 640 kW. Individual compensation of these motors by permanently-connected capacitors chosen according to IEEE Std. 141- 193, and gives rise to inadequate average power factor on monthly basis, and unnecessarily high installed capacity [48]. Although active and reactive power demands of conveyor belt systems are slowly varying, these demands are varying in a wide range in the medium and long terms according to needs of the thermal power plant (up to 2 MW, and 2.2 MVAr for each line, when operated independently).

This necessitates the use of controllable, shunt capacitor banks in addition to shunt capacitors permanently connected to motor terminals according to new regulations in TURKEY for VAr compensation given in Table 3.1.

Table 3.1 Reactive Energy Penalty Limits Recently Imposed by the Energy Market Regulatory Authority of TURKEY (In 2007)

Validity Of The Regulations	Energy Demand/Month		
	Active, %	Reactive, %	
		Inductive	Capacitive
Currently In Use	100	≤ 33	≤ 20
By January 2008	100	≤ 20	≤ 15

Coal Preparation System is fed by two different overhead lines coming from Yeniköy Thermal Power Plant as shown in Fig. 3.3. Two conveyor belt lines are working as the spare of each other. Hence, the conveyor belt line switches to the other conveyor belt line if there is a problem.

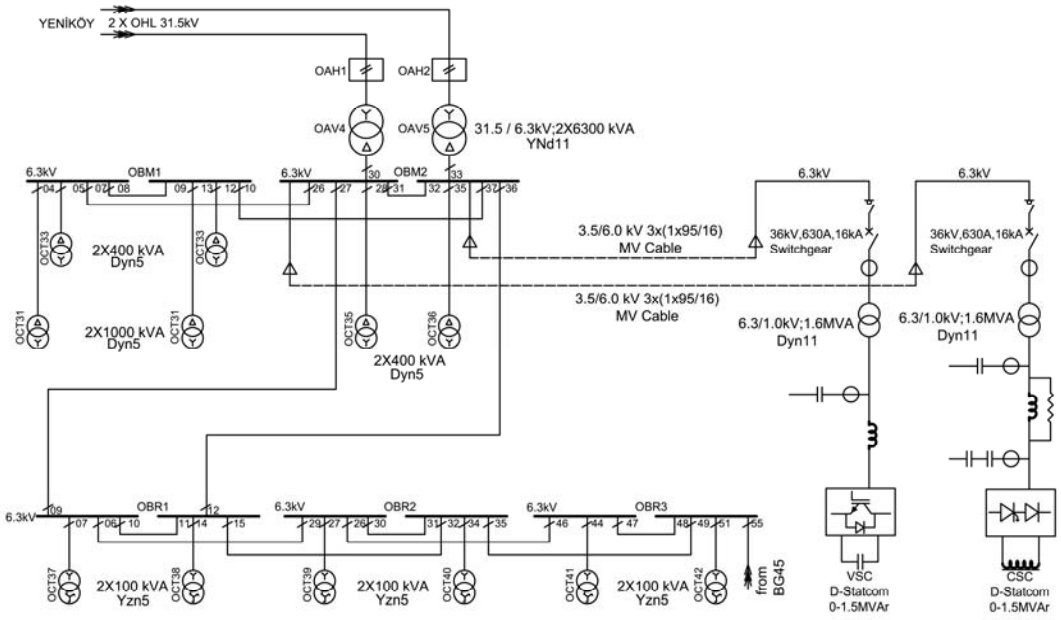


Figure 3.3 Single Line Diagram of KEAS Coal Preparation System

Existence of large amounts of coal powder in the motor environment (Fig. 3.4), space limitations, and significant distances between motors for inspection and maintenance are considered to be further drawbacks of conventional reactive power compensation techniques described above.

Group compensation technique by the use of a fully-static solution is therefore chosen for Kemerköy Coal Conveyor Belts. Since the conventional drives do not produce current harmonics, power system of Kemerköy Thermal Power Plant complies with IEEE Std. 519-1992 and the problem reduces to reactive power compensation only. Harmonic current spectrum of KEAS OAH2 feeder is given in Fig. 3.5. Active and reactive power consumed by KEAS OAH1/OAH2 feeder and power factor of KEAS OAH1/OAH2 feeder are given in Fig. 3.6 and Fig. 3.7, respectively.

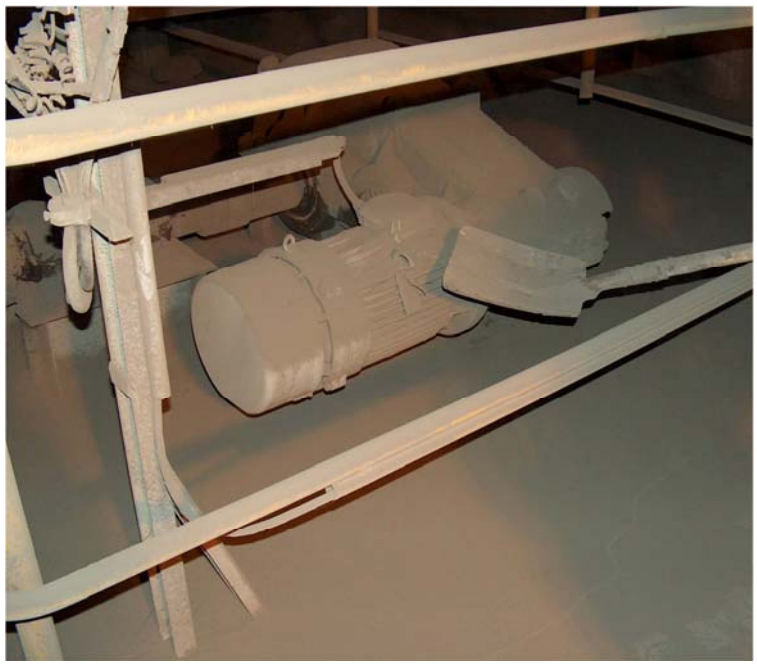


Figure 3.4 Belt Conveyor Motors with Excessive Coal Dust

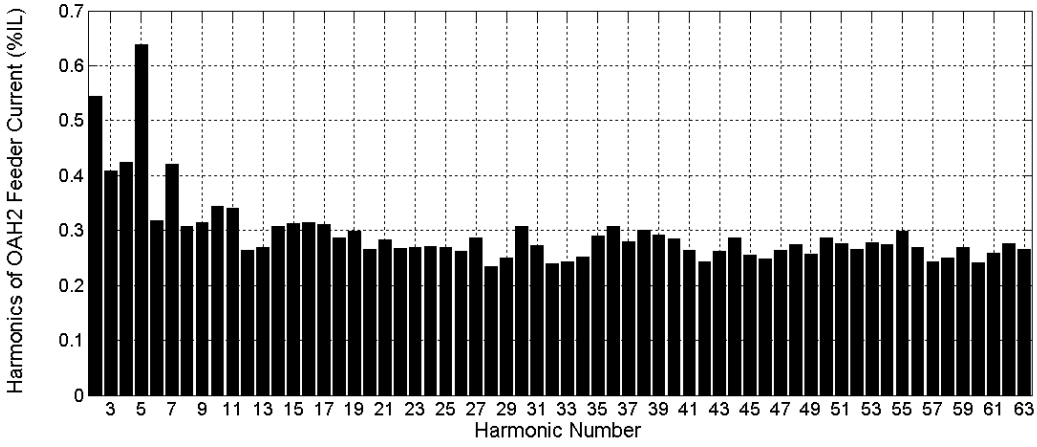
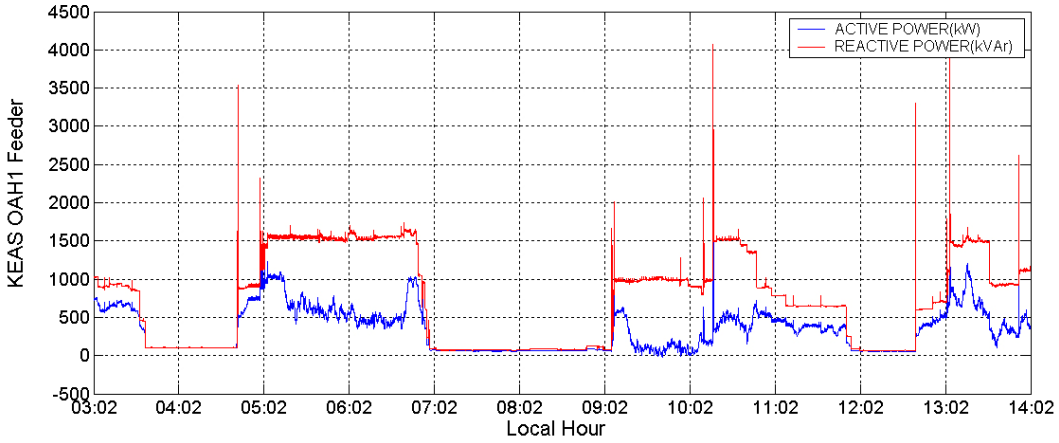
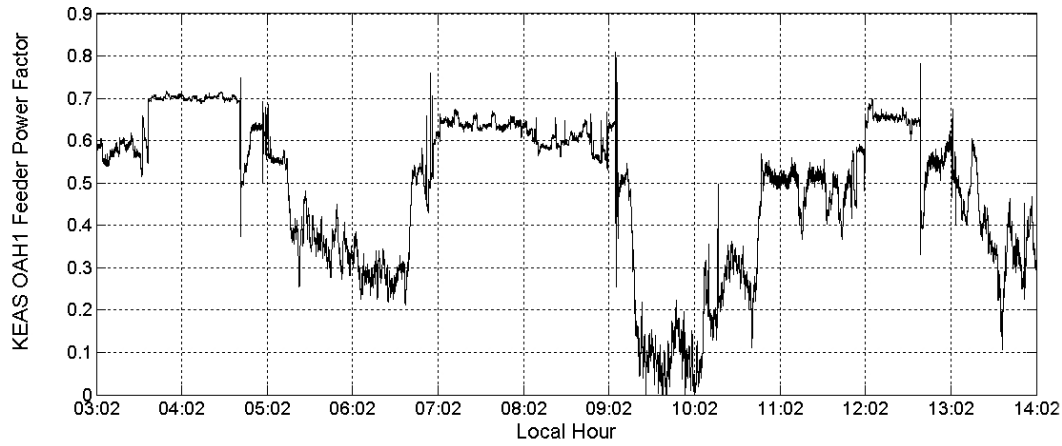


Figure 3.5 KEAS OAH2 Feeder Current Harmonic Spectrum

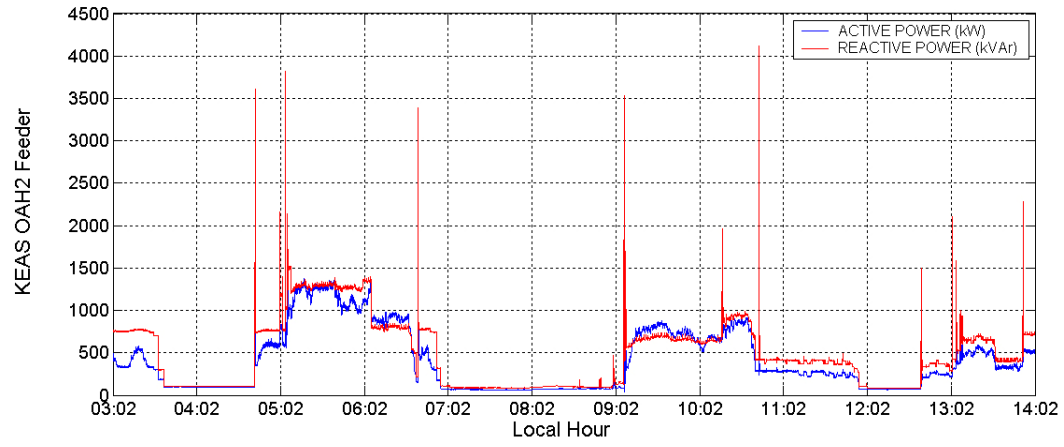


(a)

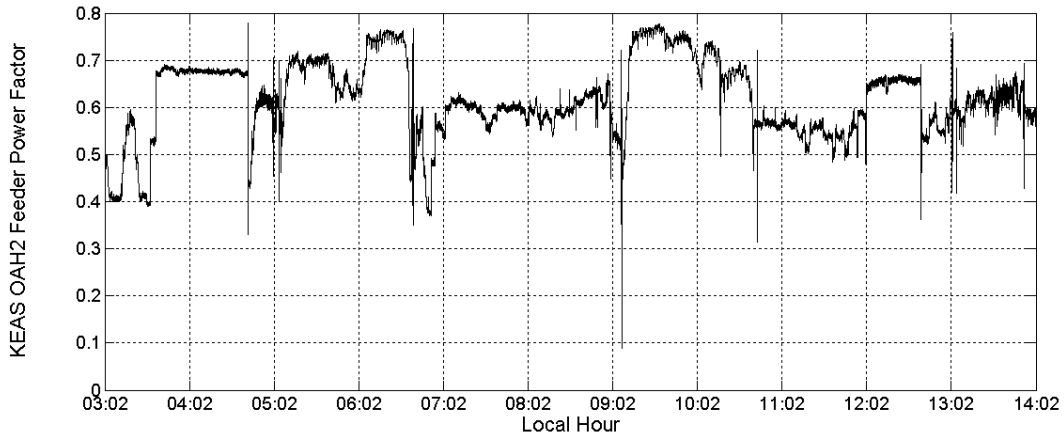


(b)

Figure 3.6 KEAS OAH1 Feeder
a : Active and Reactive Power; b : Power Factor



(a)



(b)

Figure 3.7 KEAS OAH2 Feeder
a : Active and Reactive Power; b : Power Factor

It is understood from Fig. 3.6 and Fig. 3.7 that the induction motors work at partial loads resulting in very poor power factors. The reactive power demand of coal conveyor belt drives are therefore met by distribution type STATCOMs. The reactive power compensation problem of coal conveyor belt drives fed from OAH2 feeder is solved by Voltage Source Converter based distribution type STATCOM and the reactive power compensation problem of coal conveyor belt drives fed from OAH1 feeder is solved by Current Source Converter based distribution type STATCOM.

It is seen from Table 3.1 that nearly unity p.f. (inductive p.f. = 0.98 and capacitive p.f. = 0.99) operation is needed with STATCOM. Maximum capacitive reactive power generation of STATCOM is chosen as 1.5 MVAr by considering the reactive power change given in Fig.3.7.

STATCOM produces the same reactive power both in inductive and capacitive region as shown in Fig.3.8. The capacitive reactive power generation of STATCOM is doubled by adding an input filter having the same Var rating with STATCOM. Therefore, a VSC with a Var rating of ± 750 kVAr and a + 750 kVAr input filter is used in STATCOM. Input filter is used as shunt capacitor bank and also in filtering out the switching harmonics of VSC.

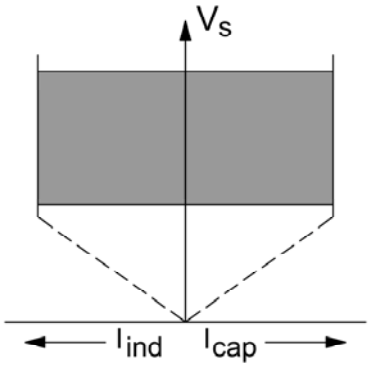


Figure 3.8 Current-Voltage Characteristic of STATCOM

Much higher input filter capacity could be used according to needs of industrial loads, and part of it may be designed either as a tuned filter for current harmonics injected by the compensated plant or as a detuned filter against the risk of sinking low order harmonics from other industrial loads connected to the point of common coupling.

Harmonic distortion in line currents at the Common Coupling Point (PCC) recommended by IEEE Std. 519-1992 with respect to I_{sc}/I_L values is given in Table 3.2. Maximum demand STATCOM curent (fundamental frequency component) at PCC is taken as 138A corresponding to 1.5MVAr capacitive reactive power generation. Maximum short circuit current (I_{sc}) is 5.29kA and I_{sc}/I_L is equal to 38.5. Therefore, second column in Table 3.2 corresponding to $20<I_{sc}/I_L<50$ (weak supply) is used in the design. Voltage THD is specified as 5 % in the standard.

Table 3.2 IEEE Std. 519-1992 Recommendations for Current Harmonic Distortion

Harmonic Number,n	Limit Recommended by IEEE Std. 519-1992		
	$100<I_{sc}/I_L<1000$	$20<I_{sc}/I_L<50$	$I_{sc}/I_L<20$
3	12 %	7 %	4 %
5	12 %	7 %	4 %
7	12 %	7 %	4 %
11	5.5 %	3.5 %	2 %
13	5.5 %	3.5 %	2 %
17	5 %	2.5 %	1.5 %
19	5 %	2.5 %	1.5 %
23	2 %	1 %	0.6 %
25	2 %	1 %	0.6 %
TDD	15 %	8 %	5 %

Design specifications of STATCOM are given in Table 3.3.

Table 3.3 Design Specifications of VSC Based STATCOM

Converter Reactive Power	± 750 kVAr
Filter Reactive Power	750 kVAr
System Voltage	1kV ± %10, 50Hz
I_TDD	≤ 5 %
V_THD	≤ 3 %

Reactive power generation of STATCOM, VSC and input filter are given in Table 3.4 for three different cases of generated reactive power. It is seen from Table 3.4 that continous reactive power control is obtained by STATCOM in the range of 0-1.5 MVAr.

Table 3.4 Reactive Power Generation Limits of STATCOM

STATCOM	VSC	Input Filter
1.5MVAr	750 kVAr	750 kVAr
750kVAr	0	750 kVAr
0	- 750 kVAr	750 kVAr

VSC has been designed and implemented at maximum value of low voltage level i.e., 1 kV l-to-l, and connected to 6.3kV level via a specially designed coupling transformer. 1 kV is chosen as the system voltage, because:

1) 1kV is the highest standard low voltage level [49] and permits the use of standard components and switchgear equipments.
2) Simplest converter topology is chosen in the design and a two level, three leg converter without any series/parallel operation is used. Converters having a power level in the neighbourhood of 1 MVA use mostly high voltage (HV) power semiconductors. The voltage ratings of available HV power semiconductors for these power levels are 2500 V, 3300 V and 4500 V. Therefore, 1 kV is a well suited system voltage level.

3.2 Selection of Power Semiconductor Switches

Voltage and current ratings of power semiconductors are found for capacitive and inductive modes of operation.

Single line diagram of STATCOM system is given in Fig. 3.9.

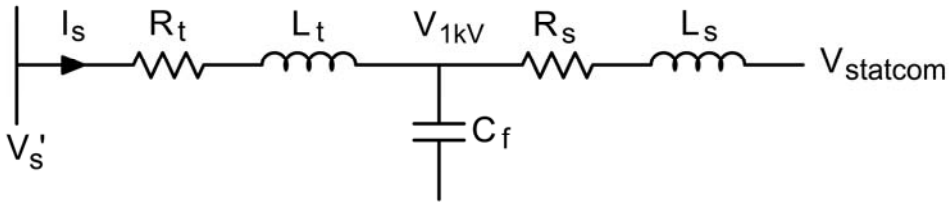


Figure 3.9 Single Line Diagram of STATCOM System

V_s', V_{1kV} and $V_{Statcom}$ refers to line-to-neutral voltages. L_t represents the given inductances referred to 1kV side

- Source inductance
- Overhead line inductance
- OAV5 transformer leakage inductance
- Coupling transformer leakage inductance

31.5 kV source impedance and overheadline impedance are specified by the manufacturer of KEAS Thermal Power Plant as below :

$$X_{sc} = 2.222\Omega/\text{phase} \Rightarrow L_{sc} = \frac{2.222}{2\pi 50} = 7.07\text{mH} \ (31.5\text{kV side})$$

$R_{ohl} = 4.611\Omega/\text{phase}$

$$X_{ohl} = 4.728\Omega/\text{phase} \Rightarrow L_{ohl} = \frac{4.728}{2\pi 50} = 15.05\text{mH} \ (31.5\text{kV side})$$

Specifications of OAV5 and coupling transformer are given in Table 3.5.

Table 3.5 OAV5 and Coupling Transformer Specifications

	OAV5 Transformer	Coupling Transformer
Rated Power	6300kVA	1600kVA
Primary Voltage	31.5 kV	6.3 kV
Secondary Voltage	6.3 kV	1 kV
U_k	6.5 %	6.5 %

$$X_{OAV5} = \frac{V^2}{S} u_k = 10.23\,\Omega/\text{phase} \quad \Rightarrow L_{oav5} = \frac{10.23}{2\pi 50} = 32.59\text{mH}\,(31.5\text{kV side})$$

$$X_{CP\_TR} = \frac{V^2}{S} u_k = 40.31\,\Omega/\text{phase} \Rightarrow L_{ct} = \frac{40.31}{2\pi 50} = 128.3\text{mH}\,(31.5\text{kV side})$$

L_t referred to 1kV side is found as in Table 3.6.

Table 3.6 Calculation of L_t at 31.5kV and 1kV Voltage Level

Voltage Level	31.5kV	1 kV
Source Inductance (L_{sc})	7.07mH	7.13uH
Overheadline Inductance (L_{ohl})	15.05mH	15.17uH
OAV4 Transformer Leakage Inductance (L_{oav5})	32.59mH	32.84uH
Coupling Transformer Inductance (L_{ct})	128.31mH	129.31uH
L_t	**183.02mH**	**184.45uH**

C_f represents the input filter capacitance of STATCOM. C_f is found as below :

$$Q_f = 3\frac{V_{1kV}^2}{X_{Cf}} \tag{3.1}$$

C_f is found to be 2.38mF for 750kVAr capacitive reactive power. C_f is formed as a delta connected shunt capacitor bank and 9x90 μF are paralelled in each phase as described in 3.4.2. Therefore, Y equivalent value of C_f is 2.43 mF.

$$X_{Cf} = \frac{1}{wC_f} \tag{3.2}$$

$$R_t = \frac{R_{ohl}}{31.5^2} + \frac{w_s L_{oav5}}{10} + \frac{w_s L_{ct}}{10} \tag{3.3}$$

$$Z_t = \sqrt{R_t^2 + (wL_t)^2} \tag{3.4}$$

$$Z_s = \sqrt{R_s^2 + (wL_s)^2} \tag{3.5}$$

R_s represents the active power losses of the converter and input filter.

$$V_{1kV} = \frac{V_s' + \frac{Z_t}{Z_s} V_{statcom}}{1 + \frac{Z_t}{Z_s} - \frac{Z_t}{X_{Cf}}} \tag{3.6}$$

$$\text{From Equation (2.60)} \Rightarrow V_{statcom} = 0.4103 V_d \tag{3.7}$$

where V_d represents the average DC link voltage.

$$V_{1kV} = \frac{V_s' + 0.4103 \frac{Z_t}{Z_s} V_d}{1 + \frac{Z_t}{Z_s} - \frac{Z_t}{X_{Cf}}} \tag{3.8}$$

$$Q_{statcom} = 3\left[I_s^2 X_{ct} - \frac{V_{1kV}\left(Vstatcom - V_{1kV}\right)}{Z_s} - \frac{V_{1kV}^2}{X_{C_f}} \right] \tag{3.9}$$

Power sink convension has been used. Therefore, (+) sign denotes the inductive reactive power and (-) sign denotes capacitive reactive power.

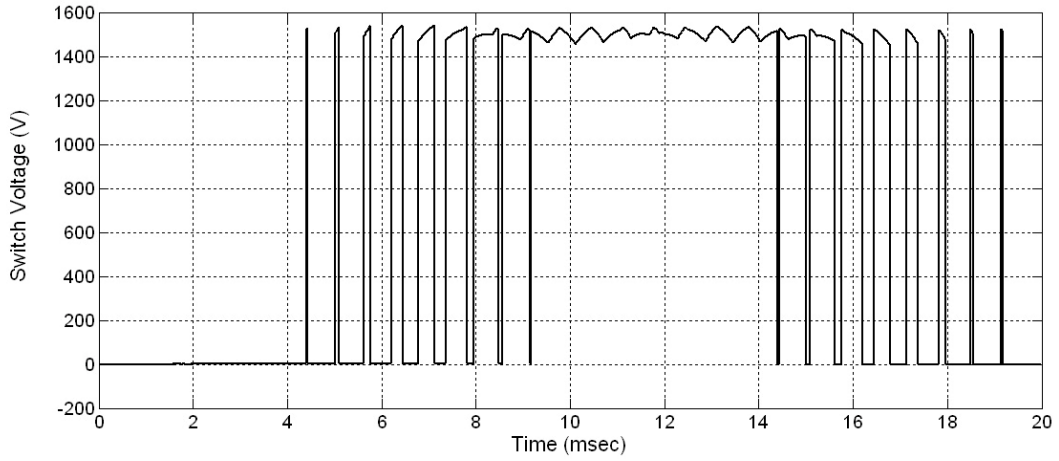
DC link voltages and VSC fundamental currents are given in Table 3.7 for the source voltages of 31.5 kV, 36 kV and 28 kV for L_f = 300 μH and L_f = 600 μH.

The simulation results are given for two different values of input filter inductance to observe its effect on the DC link voltage swing from full capacitive to full inductive

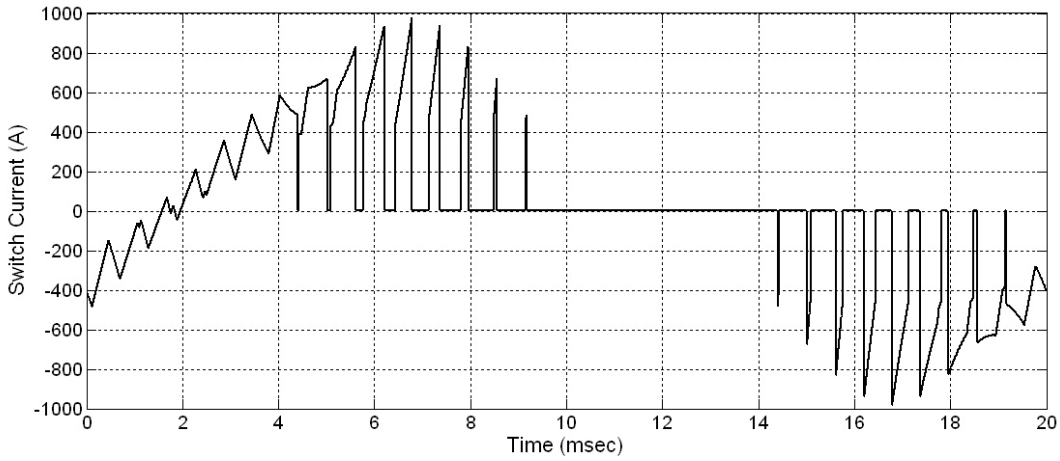
mode. DC link voltage changing from 1157 V to 1763 V for 300 μH input filter inductance and from 1068 V to 1810 V for 600 μH input filter inductance. Maximum STATCOM fundamental current is 510 A. Peak power semiconductor current is 980 A as seen from Fig. 3.10. The switching waveforms for the power semiconductors are given in Fig. 3.10 for the conditions marked by * in Table 3.7.

Table 3.7 Simulation Results for Steady-State Analysis of STATCOM

Source (kV)	**L_f (μH)**	**$V_{statcom}$ (V)**	**$Q_{statcom}$ (kVAr)**	**V_{1kV} (V)**	**I_{VSC} (A)**	**V_d (V)**
31.5	300	1148	-1503	1086	367	1615
	600	1206	-1500	1086	365	1697
	300	925	4	1000	443	1302
	600	854	3.5	1000	443	1202
36	300	1253	-1499	1218	205	1763
	600	1286	-1499	1218	205	1810
	300	1057	6	1143	507	1487
	600	976	5	1143	506	1373
28	300 *	1071	-1501	985	510	1507
	600	1153	-1502	985	510	1622
	300	822	4	889	395	1157
	600	759	3	889	394	1068



(a)



(b)

Figure 3.10 Switching Waveforms of Power Semiconductor
a : Switch Voltage ; b : Switch Current
(PSCAD/EMTDC)

The ratings of the candidate power semiconductors that must be used in VSC are estimated to be as in Table 3.8 by considering the available voltage and current ratings in the market.

Table 3.8 Ratings of Power Semiconductors in STATCOM

Voltage Rating	≥ 3300V
Current Rating	≥ 800A
Switching Frequency	≥ 1kHz

3.3 kV High Voltage (HV) IGBT Modules and 4.5 kV Asymmetric IGCTs are the candidate power semiconductors for this application. A comparison based on the on-state voltages and switching losses of 3.3kV/1.2kA HV IGBT modules and 4.5kV/4kA asymmetric IGCT from different manufacturers is given in Table 3.9. All specifications are given for V_{cc}=1800 V, I_c=1200 A and T_j= 125 °C.

IGCTs are optimised for applications up to 1 kHz. 1 kHz is the absolute maximum switching frequency that can be used with IGCTs and maximum turn-off current decreases with switching frequency in order to have lifetime of 20 years for on-board capacitors. This relation is shown in Fig. 3.11.

Switching frequency decreases below 450 Hz for 1 kA switching current. 850 Hz switching frequency is also at the edge of absolute maximum switching frequency of IGCTs. Therefore, IGCT is not preferred in this application.

Table 3.9 Comparison of HV Power Semiconductors

Manufacturer Product No	$V_{ce(sat)}$ (V)	V_f (V)	E_{on} (J)	E_{off} (J)	E_{rec} (J)
Mitsubishi CM1200HC-66H	3.6	2.7	1.75	1.7	0.98
ABB 5SNA 1200E330100	3.8	2.35	1.89	1.95	1.53
Dynex DIM1200ESM33-F000	3.6	2.35	2.4	1.44	0.84
Eupec FZ1200 R 33 KF2	4.3	2.8	2.88	1.53	1.5
Hitachi MBN1200E33D	4.2	2.5	1.75	1.42	1.31
ABB 5SHY 35L4510 IGCT 5SDF 10H4502 Diode	1.7	3.75	0	4.2	2.33

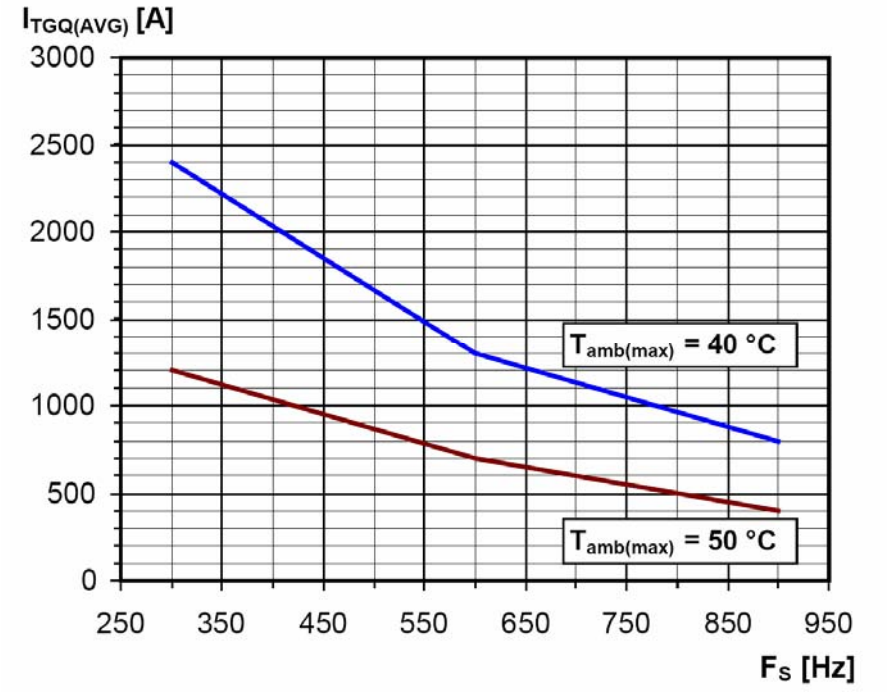


Figure 3.11 Maximum Turn-Off Current of 5SHY 35L4510

Maximum switching frequency is not specified for HV IGBT modules by the manufacturers. However, some HV IPM module manufacturers limit the maximum switching frequency to 2 kHz. Maximum switching frequency of HV IGBT modules depends on the cooling system. Switching frequency of 3.3 kV HV IGBT modules should be kept around 1 kHz in order to have 1 % converter active power loss [46]. Nevertheless, commercially available drivers limit the maximum switching frequency to 7 kHz [50].

Extremely powerful cosmic rays may enter into the power semiconductors when a high DC voltage is applied continuously to the power semiconductor modules over a long time. This can destroy the device suddenly. Therefore, cosmic ray withstand capability has become an important design criterion for power semiconductor devices. A semiconductor device may be destroyed abruptly, without current leakage increase either at the moment of device destruction or before and after it. Destruction occur randomly in the device, melting down the device on the spot [51]. This destruction phenomenon is known to be related to voltage, and the failure rate is exponentially dependent on the applied voltage (electric field strength). Fig. 3.12 shows dependency between DC voltage and the failure rate (FIT) for CM1200HB-66H. 1 FIT is equivalent to one failure in 10^9 hours of operation. DC Voltage value at 100 FIT failure rate is called V_{LTDS}. Therefore, the cosmic ray withstand capability is 100 FIT at V_{LTDS}. It is seen from Fig. 3.12 that maximum DC voltage for CM1200HB-66H is 2100 V for a failure rate of 100. Hence, maximum DC link voltage of VSC must be kept below 2100 V for the whole range of operation.

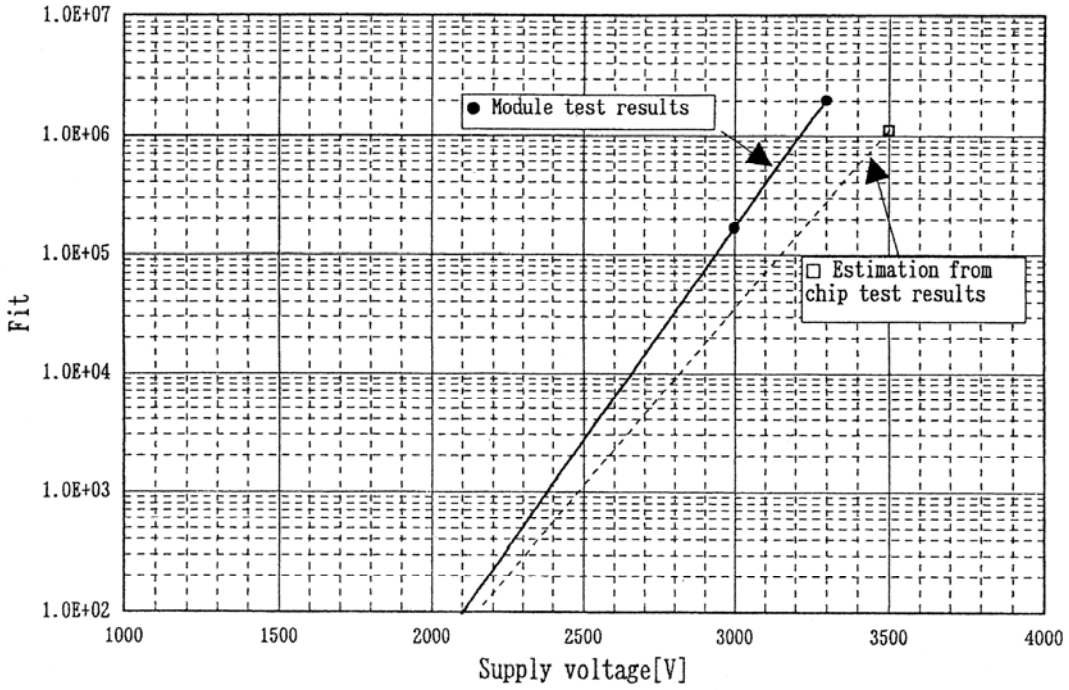


Figure 3.12 Dependence between LTDS Failure Rates and Supply (DC Link) Voltage for CM1200HB-66H HV IGBT Module

SPWM technique requires switching frequencies in the range from 1 to 5 kHz. Switching losses of HV IGBT modules in this frequency range are higher than conduction losses and SPWM technique with HV IGBT modules necessitates the use of cooling systems with bigger capacities. Well known applications of HV IGBT modules uses switching frequencies in the range of 0.8-2 kHz [15, 41]. However, in low power applications, SPWM technique can be used with low voltage IGBT modules (600 V-1700 V) without any significant cooling problems. DC link voltage is kept constant with SPWM and this value must be kept smaller than V_{LTDS} for the whole range of operation.

SHEM technique is better suited for HV IGBT modules because of 50 % reduction in switching frequency for the same current TDD when compared to SPWM technique. This results in significant reduction in switching losses.

In phase angle control with SHEM technique, DC link voltage increases as the modulation index decreases for a predetermined value of generated reactive power. Maximum capacitive reactive power generation specification and modulation index determines maximum DC link voltage in the application. Therefore, modulation index must be chosen as follows :

- Voltage regulation of the DC link voltage from full inductive mode to full capacitive mode decreases with higher values of modulation index. A higher modulation index also minimizes the switching losses because of lower DC link voltages for a predetermined value of generated reactive power. Higher DC link voltages also cause higher converter harmonic voltages and dead time related harmonics increase at higher DC link voltages.
- Maximum DC link voltage must be smaller than V_{LTDS}.
- Minimum Pulse Width Constraint given in 2.3.2.4.1 limits the modulation index in the application.

From the discussed HV IGBT modules, CM1200HC-66H (Mitsubishi) and DIM1200ESM33-F000 (Dynex) products have the best technical specifications when conduction and switching losses are considered together. However, CM1200HC-66H HV IGBT Module is preferred in the implementation because of short delivery time and lower costs.

Switching test circuit and turn-off switching waveform of CM1200HC-66H are given in Fig. 3.13 and Fig. 3.14 for the following test conditions [52]:

V_{cc}=2400 V, I_c=2400 A, T_j=125 °C, V_{GE}=±15 V ,
R_G=1.6 Ω, C=2 mF, Cs=20 μF, L_{S1}=500 nH, L_{S2}=100 nH

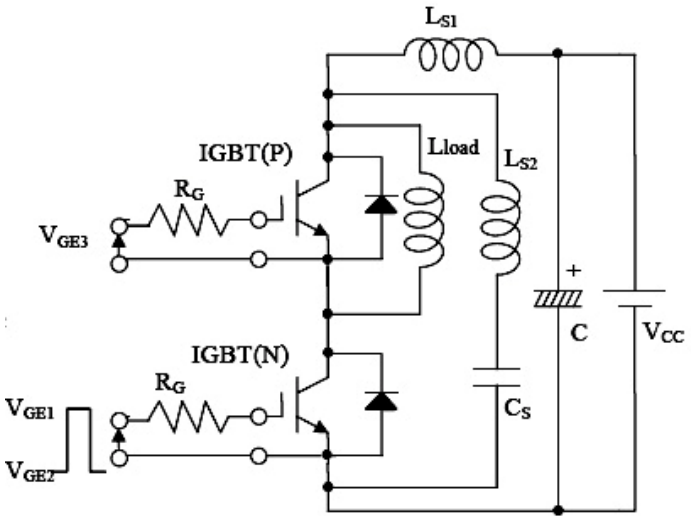


Figure 3.13 Switching Test Circuitry

C is a bulky capacitor and supports the DC link voltage in the steady state. L_{s1} represents the inductance of the cable between C and 'one leg' in test. C_s is a low ESL, low ESR capacitor and L_{s2} represents total effective dc link inductance which should be kept low in order to have small overshoot during turn-off. It is seen from Fig. 3.14 that voltage overshoot on the HV IGBT module is 500 V even at 2400 A current during turn-off through a dc link inductance of 100nH. Basic specifications CM1200HC-66H are given in Table 3.10.

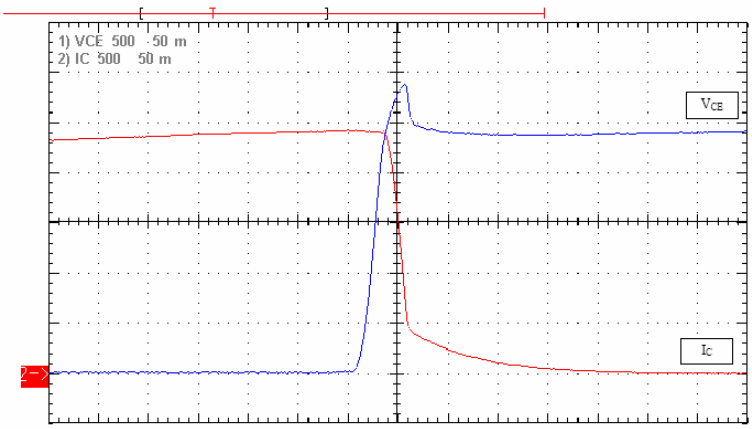


Figure 3.14 Turn-Off Switching Waveform
Ch1 : VCE :500V/div (Blue) ; Ch2 : Ic :500A/div (Red); time :1µs/div

Table 3.10 Basic Specifications of CM1200HC-66H

Item	Symbol	Conditions		Ratings
Collector-emitter voltage	V_{CES}	V_{GE}=0, T_j=25°C		3300V
Gate-emitter voltage	V_{GES}	V_{CE}=0, T_j=25°C		±20V
Collector current	I_C	T_C=25°C		1200A
	I_{CM}	Pulse		2400A
Emitter Current (FWDi)	I_{CE}	T_C=25°C		1200A
	I_{EM}	Pulse		2400A
Isolation Voltage	V_{iso}	Charged part to base plate, rms sinusoidal, AC 60Hz, 1 min.		6000V
Junction Temperature	T_j	-		-40 ~ +150°C
Collector-emitter saturation voltage	$V_{CE(sat)}$	I_C=1200A, V_{GE}=15V	T_j=25°C	3.3V
			T_j=125°C	3.6V
Emitter-collector voltage (FWDi)	V_{EC}	I_E=1200A, V_{GE}=0V	T_j=25°C	2.80V
			T_j=125°C	2.70V
Turn-On switching energy	E_{on}	VCC=1650V, T_j=125°C IGBT(N): IGBT Operation I_C=1200A, V_{GE1}= -V_{GE2}=15V RG=1.6Ω IGBT(P): FWDi Operation I_E=1200A, V_{GE3} =-15V, RG=1.6Ω		1.6 J/P
Turn-Off switching energy	E_{off}			1.55 J/P
Reverse recovery energy	E_{rec}			0.9 J/P

3.3 Design of Power Stage Layout

Schematic diagram and footprint of overall power system layout is given in Fig. 3.15 and Fig. 3.16.

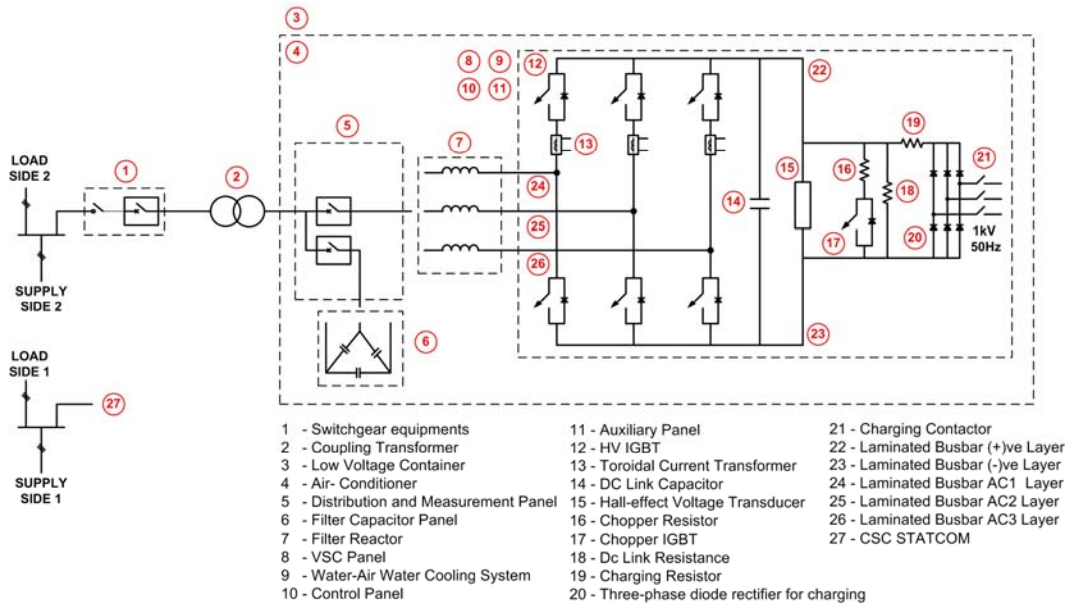


Figure 3.15 Schematic Diagram of the Implemented VSC STATCOM

Dark grey parts in Fig. 3.16 show the parts of VSC STATCOM connected to KEAS OAH2 feeder and light grey parts show the parts of CSC STATCOM connected to KEAS OAH1 feeder.

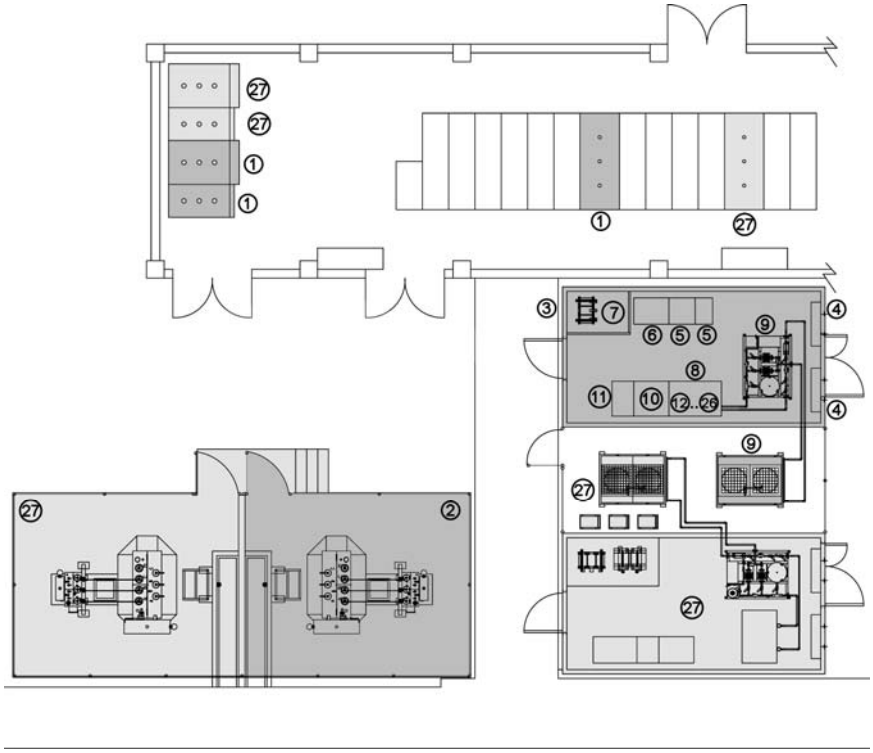


Figure 3.16 Footprint of VSC STATCOM

Switchgear cubicles are shown in Fig. 3.17.

Figure 3.17 6.3kV Switchgear Cubicles

Low voltage part of STATCOM including the circuit breakers, input filter, converter, control panel and water-to-air water cooling system pump unit are put in a custom designed container because of excessive coal dust in the environment (Fig. 3.18).

Only the coupling transformer and the heat exchanger (HX) unit of the water-to-air water cooling system are put in open area as shown in Fig. 3.19.

Figure 3.18 STATCOM LV Container

Figure 3.19 HX Unit and Coupling Transformer

3.3.1 Laminated Busbar Design

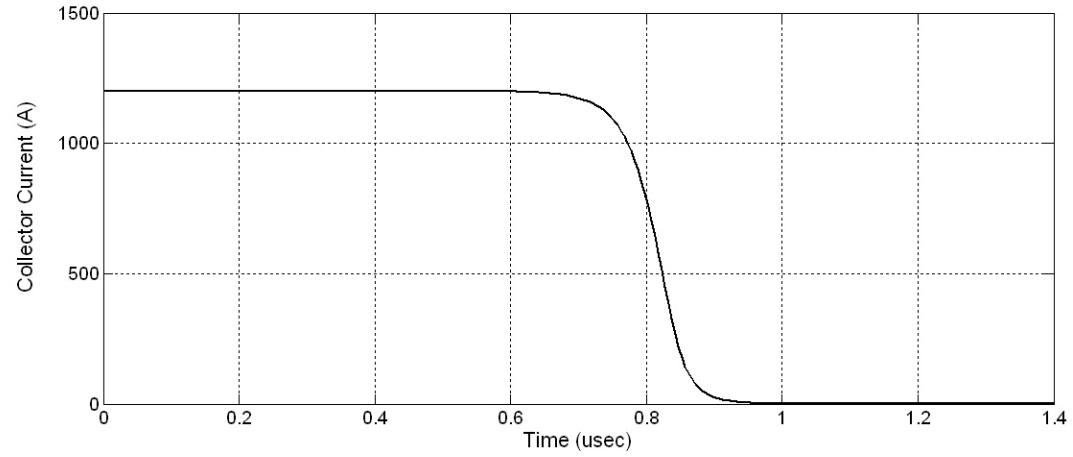
Switching of power semiconductors causes voltage overshoots because of the parasitic inductances present in the power circuit. These voltage overshoots are seen across the power semiconductors and it must be verified that the maximum permissible blocking voltage of the power semiconductor is never exceeded. Turn-off switching waveform of an IGBT are given in Fig. 3.20 with two different busbar inductances such as 100 nH and 150 nH. Simulations are done by ORCAD/PSPICE program for V_d=1800 V and I_c=1200 A. The voltage overshoot rises from 700V to 1400V when the busbar inductance of 100 nH is increased to 150 nH. This result shows the importance of laminated busbar for voltage source converters with IGBT modules.

For HV IGBTs, there is no limitation for the values of di/dt and dv/dt as long as the limits specified in the HV IGBT reverse biase safe operating area (RBSOA), FWD reverse recovery safe operating area (RRSOA) and short circuit safe operating area (SCSOA) are met safely.

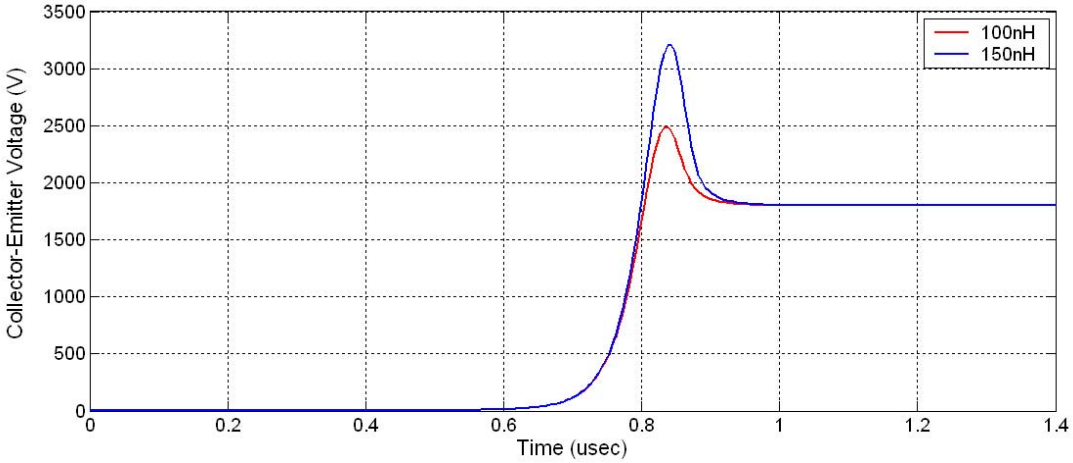
HV IGBTs have high switching speeds and the current change di/dt is very high at turn-off and also at turn-on. Definition of switching time and energy for both IGBT part and diode part are given in Fig. 3.21 and Fig. 3.22. [53].

Turn-off gate resistor can be increased to suppress the voltage overshoots at turn-off. However, higher turn-off gate resistor also increases turn-off switching losses. A better solution is to minimize the effective dc link inductance of the converter.

HV IGBT modules have also high turn-on di/dt. Turn-on di/dt must be kept lower than the value specified in RRSOA. Turn-on switching losses and RRSOA determines the value of turn-on gate resistor.



(a)



(b)

Figure 3.20 Turn-Off Switching Waveforms
(a) HV IGBT Collector Current (b) HV IGBT Collector-Emitter Voltage

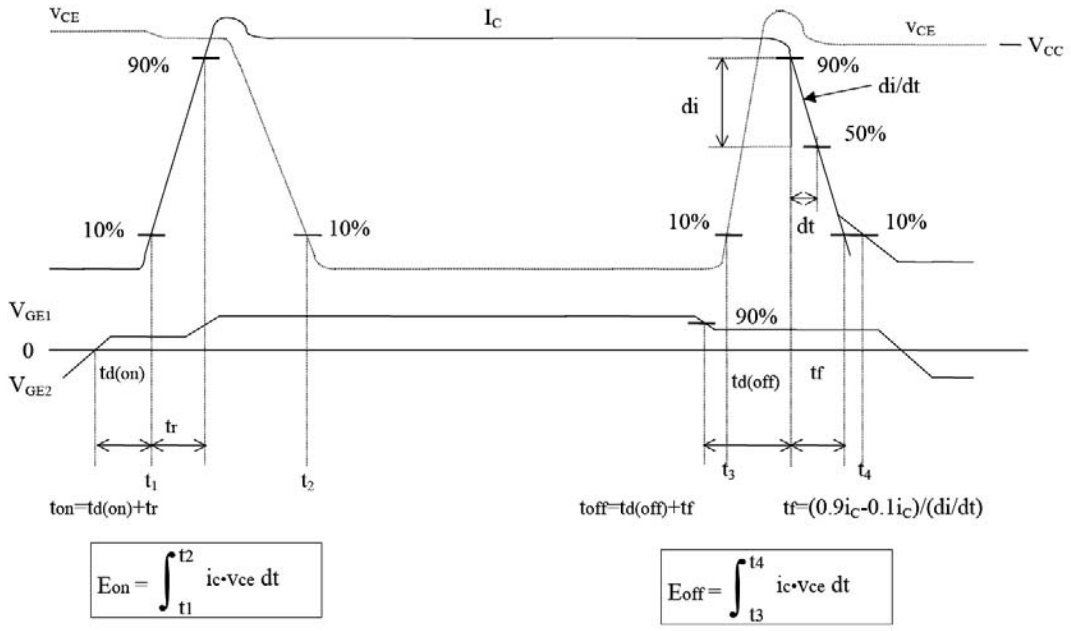


Figure 3.21 Definitions of Switching Time and Energy for IGBT part

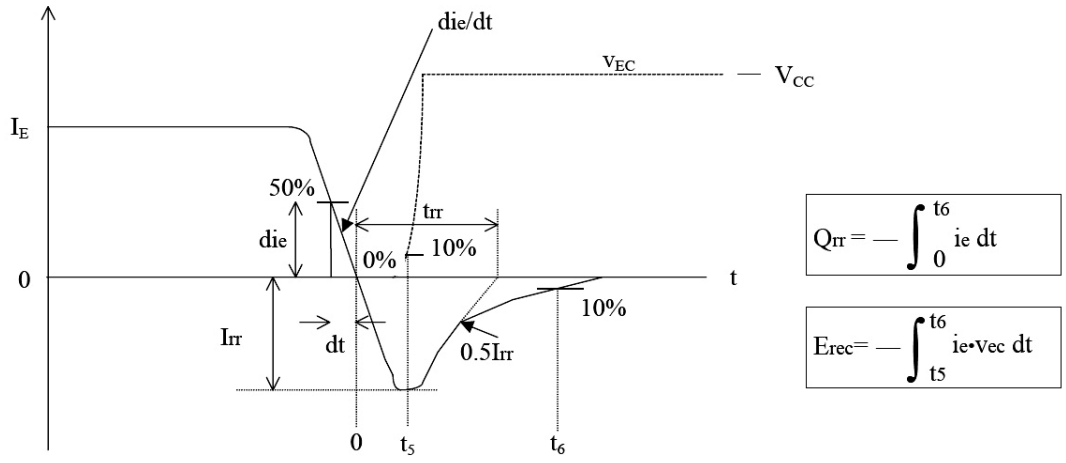


Figure 3.22 Definitions of Switching Time, Charge and Energy for Diode part

Inductance of various line types that are used in the construction of the converter and at the connections among the components are shown in Fig. 3.23 [54]. The advantages of stripline (laminated busbar) and coaxial cable is seen from Fig. 3.23. Commercially available HV IGBT driver manufacturers propose a minimum stray inductance of the order of 50-100 nH for the proper operation of the driver. Use of separate wires should be avoided in order to reach a stray inductance value below 100 nH and therefore, laminated busbar is a must.

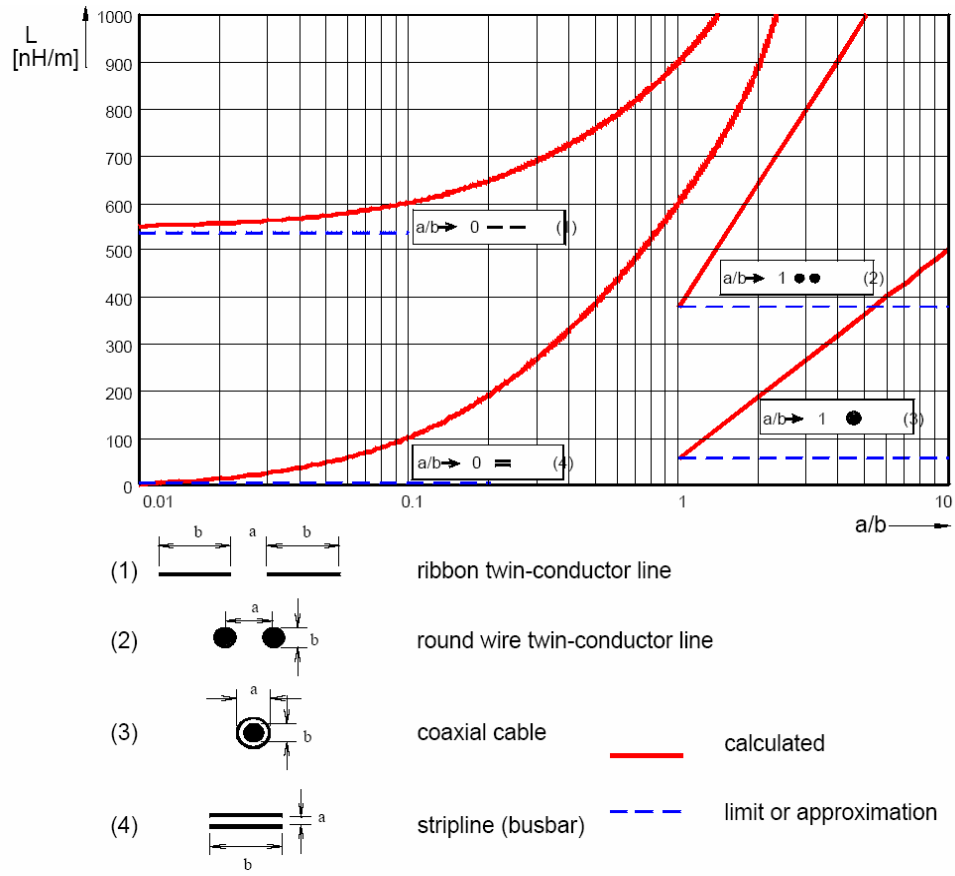


Figure 3.23 Inductance of Different Lines

The busbar structure is formed by two parallel conducting plates of resistivity ρ [Ωm], relative permeability μ_r [p.u.] separated by a dielectric material with relative permittivity ε_r [p.u.] and dielectric conductivity σ [1/ Ωm]

A physical representation for the laminated busbar is shown in Fig. 3.24 [55].

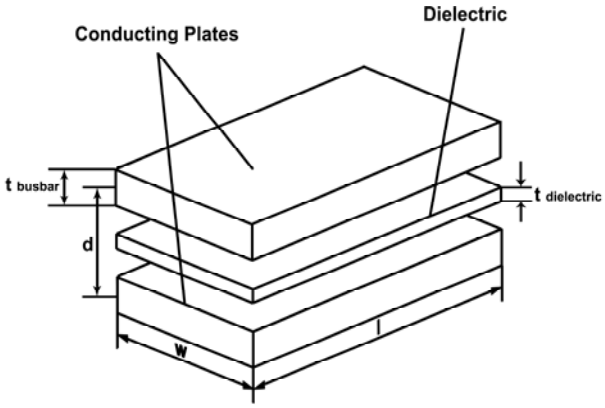


Figure 3.24 Physical Representation of Laminated Busbar

The choice between a lumped parameter model and a transmission line model for the laminated busbar is decided by the highest frequency component of the converter [55]. Highest criticial frequency is defined as :

$$f_c = \frac{1}{2\pi t_f} \tag{3.10}$$

where t_f represents the device fall time. t_f decreases with switching current in HV IGBT modules. t_f value is 200ns at a switching current of 2000A for the selected HV IGBT module which implies that f_c = 0.8 MHz .

The wavelength is defined in (3.11).

$$\lambda = \frac{c}{f_c} \tag{3.11}$$

Transmission line analysis is required when standing waves are present. Standing waves may occur whenever one-quarter of the wavelength can be compared with the dimensions of the busbar [55].

λ/4 is equal to 93.75 m and is not comparable with the dimensions of the busbar. Therefore, lumped stray inductance model shown in Fig. 3.25 is sufficient for the converter implemented with HV IGBT modules.

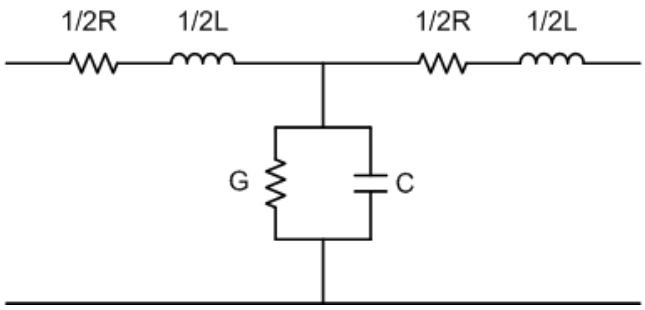


Figure 3.25 Equivalent Circuit Model of Laminated Busbar

The capacitance between the busbars are given as in (3.12) :

$$C_b = \varepsilon_0 \varepsilon_r \frac{w.l_{busbar}}{t_{dielectric}} \tag{3.12}$$

The busbar dielectric losses is represented by shunt conductance G in Fig. 3.25.

$$G_b = \sigma \frac{w.l_{busbar}}{t_{dielectric}} \tag{3.13}$$

Laminated busbar inductance decreases by :

- decreasing the dielectric thickness (d)
- increasing the conductor width (w)
- increasing the frequency

Laminated busbar inductance is the sum of internal and external inductances. Internal inductance is the result of flux linkages within the busbar plates. It is calculated from the attenuation of fields as they penetrate to conductors [55]. Internal inductance changes with frequency because of skin and proximity effects. Current tends to concentrate near the surface at high frequencies and internal inductance can be neglected as seen in Fig. 3.26 [56].

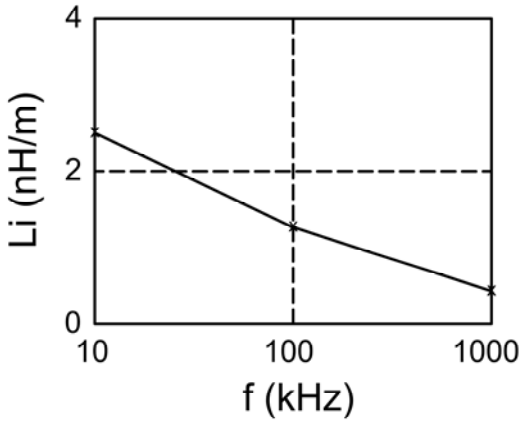


Figure 3.26 Internal Inductance for 1mm Copper plate (width=10cm)

However, internal inductance is very important for low frequency applications such as laminated busbars. It can be calculated in low frequency applications as below [55]:

$$L_i = \frac{\mu_o \mu_r}{8\pi} l \tag{3.14}$$

External inductance is determined by the geometry of the laminated busbars and it is a frequency independent inductance. It can be calculated per unit length from (3.15) as given in [56] :

$$L_{e_l} = \mu_o \frac{t_{dielectric}}{w} \tag{3.15}$$

DC link capacitors are either directly mounted on the laminated busbar or on the sides of the laminated busbar as illustrated in Fig. 3.27.

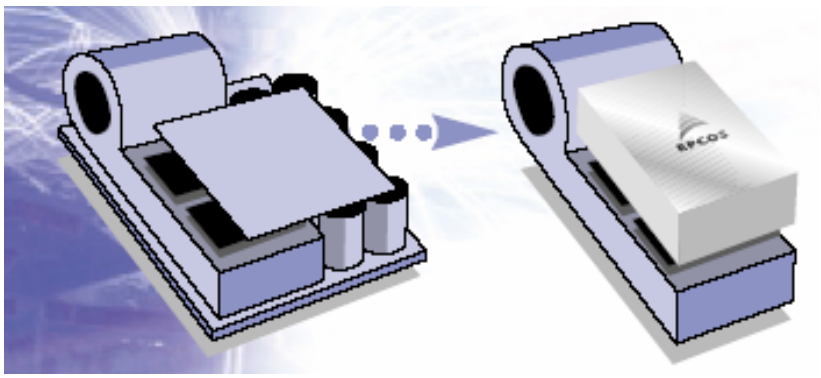


Figure 3.27 Mounting of DC Link Capacitors on the Laminated Busbar

In the converter shown on the left in Fig. 3.27, there are parts on the laminated busbar which are not near to the return path of the current. If the distance between the current return path and the capacitor current path is long, then the inductance in this path is to be calculated from (3.16) and (3.17) [56] :

$$L_{e_2} = 2\times10^{-7} l\left[\ln\left(\frac{2l}{w + t_{busbar}}\right) + 0.5 + 0.2235\left(\frac{w + t_{busbar}}{l}\right)\right] \qquad (3.16)$$

$$L_{eff} = L_i + L_{e_1} + L_{e_2} \qquad (3.17)$$

Laminated busbar inductances are calculated for w = 30 cm ; t_2 = 2 mm and t << w

$L_i = 50\,\text{nH/m}$

$L_{e1} = 8.4\text{nH/m}$

$L_{e2} = 439\ \text{nH}\quad \text{for}\ l = 1\text{m}$

The external inductance of L_{e_1} and L_{e_2} are extremely different for a length of 1m. Hence, the distance between current return path and the capacitor current path must be decreased in order to have a low laminated busbar inductance.

A converter design with HV IGBT modules and standard electrolytic capacitors in which L_{e_2} can not be neglected is shown in Fig. 3.28 [54].

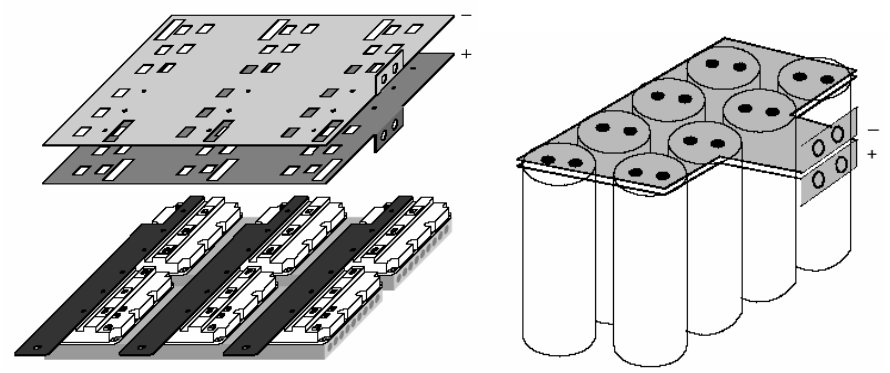


Figure 3.28 A Converter with Standard Electrolytic Capacitors

For obtaining a low inductance dc link design :

- Positive and negative dc link busbars must be brought closely.
- Positive dc link and ac output busbars must be brought closely.
- Negative dc link and ac output busbars must be brought closely.

AC output busbars must be designed as close as possible to the positive and negative dc link busbars in high current converters to minimize the stray inductance.

DC resistance of the laminated busbar and skin depth are given respectively in (3.18) and (3.19) [55].

$$R_{dc} = \rho \frac{2l}{w.t} \tag{3.18}$$

$$\delta_S = \sqrt{\frac{\rho}{\pi f \mu_o}} \tag{3.19}$$

where ρ is the resistivity of the busbars and f is the frequency.

Skin effect has to be considered for high frequency operation and t>2δ. Hence, AC resistance as defined in (3.20) must be used instead of dc resistance.

$$R_{ac} = \rho \frac{4l}{w.\delta_s} \tag{3.20}$$

Effective dc link inductance is found by adding

- Laminated busbar inductance
- Equivalent series inductance of DC Link Capacitors
- Screw and spacer inductance (~ 10nH)
- Internal Inductance of IGBT (10nH)

Specifications of the busbar is found by steady-state analysis given in Table 3.7 and PSCAD simulations. The specifications are given in Table 3.11.

Maximum laminated busbar inductance is specified as 30 nH in order to have a maximum effective DC link inductance lower than 100 nH.

DC link capacitor is selected from Epcos PC HP High Power Capacitors family. PCC HP products have low self-inductance (< 40 nH) and they are designed to be directly mounted on the laminated busbar. This is very important to minimize effective dc link inductance as seen from the HV IGBT modules in medium power converters.

Table 3.11 Technical Specifications of VSC STATCOM

Max. RMS AC Voltage	1500 V
Max. RMS AC Current	700 A
Max.. Average DC Link Voltage	2200 V
Max. RMS DC Link Current	500 A
Max. Peak IGBT Voltage	3300 V
Max. RMS IGBT Current	300 A
Max. Peak IGBT Current (During Operation)	1200 A
Max. Peak IGBT Current (During Short Circuit, $t_{pw} \leq 10\mu s$)	6000 A
Isolation Voltage (RMS, Sinusoidal, f = 50Hz, t = 1 min)	6 kV
Laminated Busbar Inductance	≤ 30 nH

DC link capacitors are designed in the form of 3 parallel capacitors. Positive (P) terminal of each capacitor is placed near to the collector terminal of upper HV IGBT module in one leg, and negative (N) terminal of each capacitor is placed near to the emitter terminal of lower HV IGBT module of the same one leg. Inductance L_{e_2} is negligible because of the converter layout and dc link capacitor placement shown in Fig. 3.29.

Glass reinforced polyester (GRP) based isolation layers with 2 mm thickness are used between the layers. Busbar layers are formed by copper plates with 2 mm thickness. Designed busbar layers are as shown in Fig. 3.30. Implemented busbar layers are as given in Fig. 3.31.

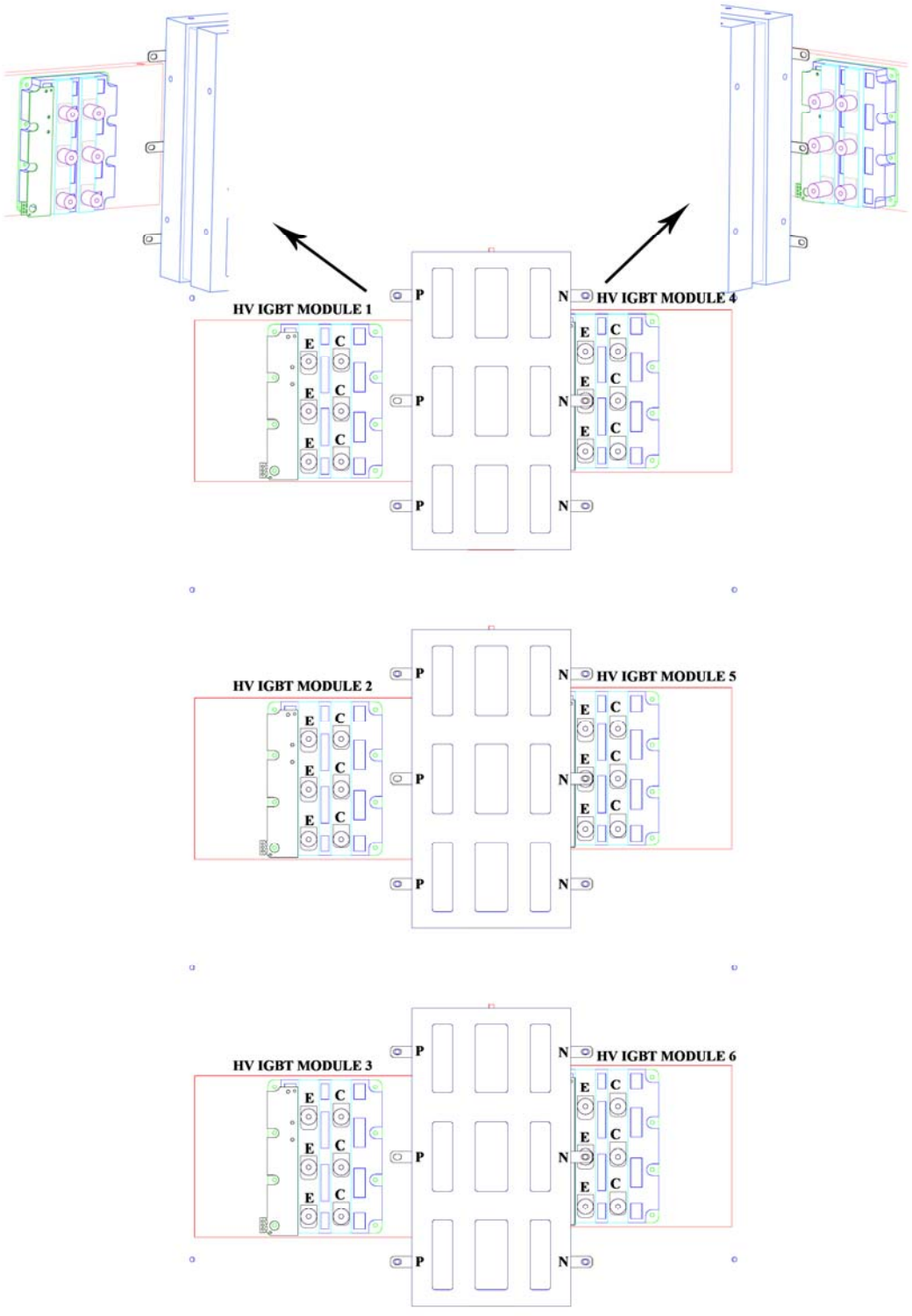


Figure 3.29 Converter Layout and Placement of DC Link Capacitors

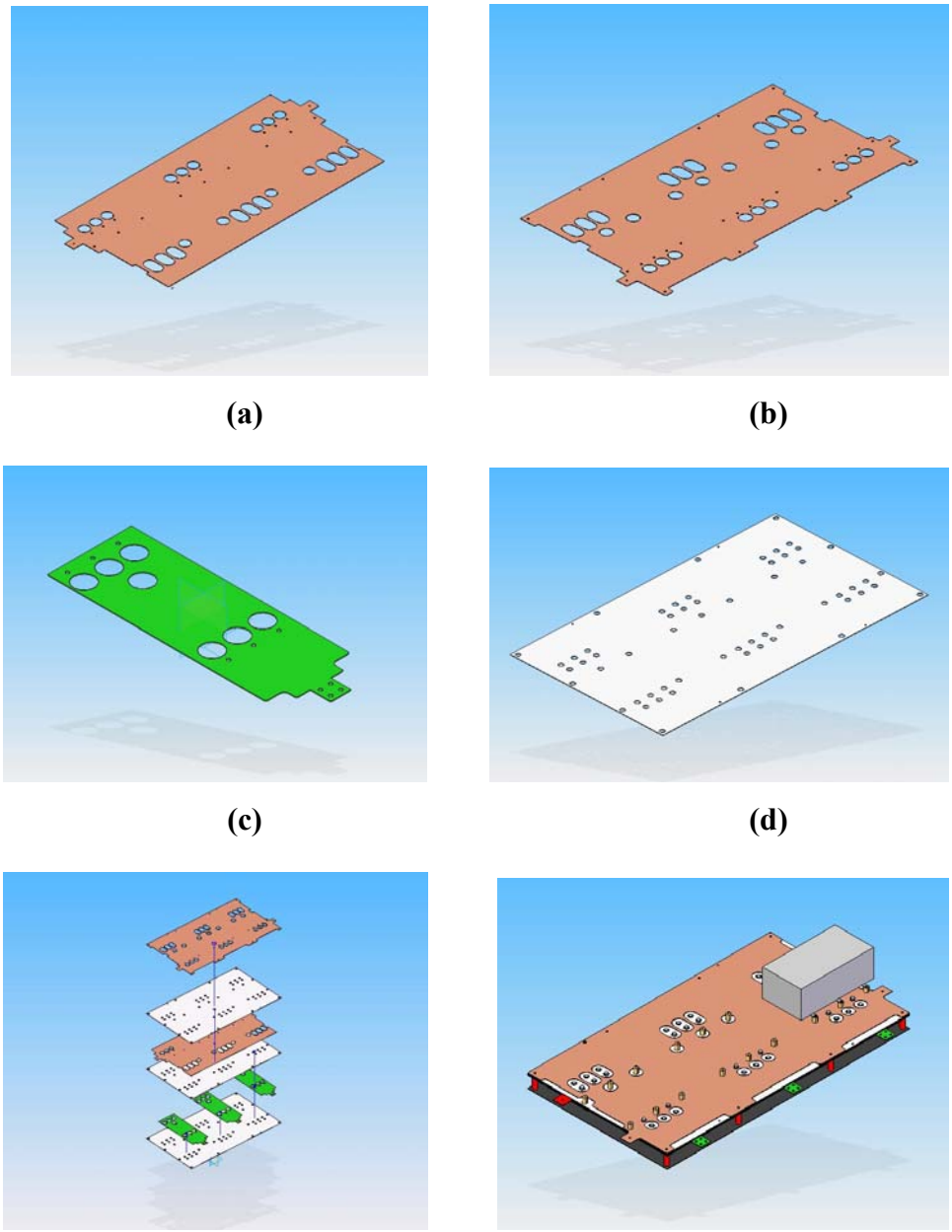
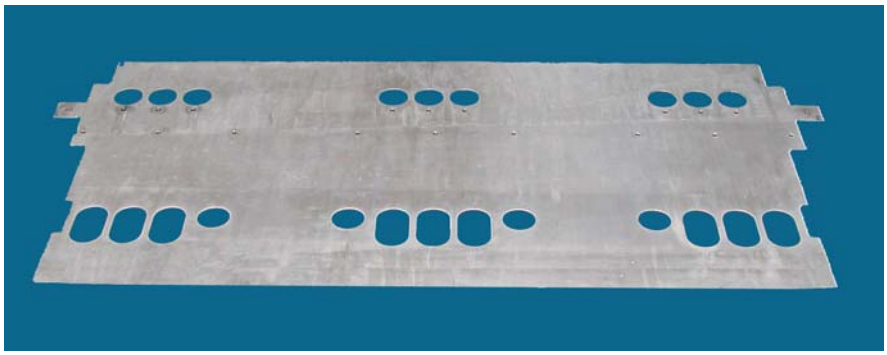
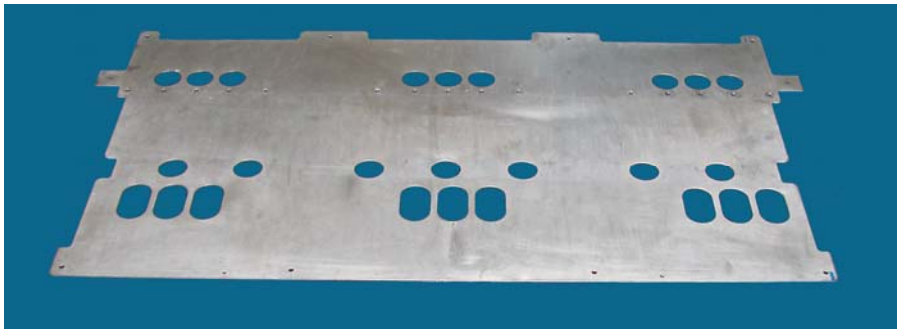


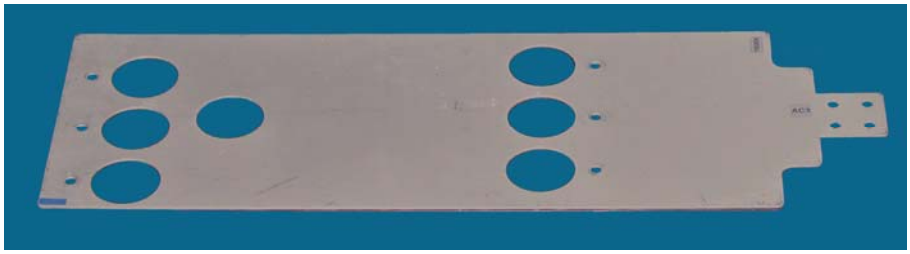
Figure 3.30 Designed Laminated Busbar Layers
(a) : Positive Busbar Layer ; (b) : Negative Busbar Layer
(c) : AC Busbar Layer ; (d): Isolation Layer
(e) : All Layers ; (f): Complete Laminated Busbar



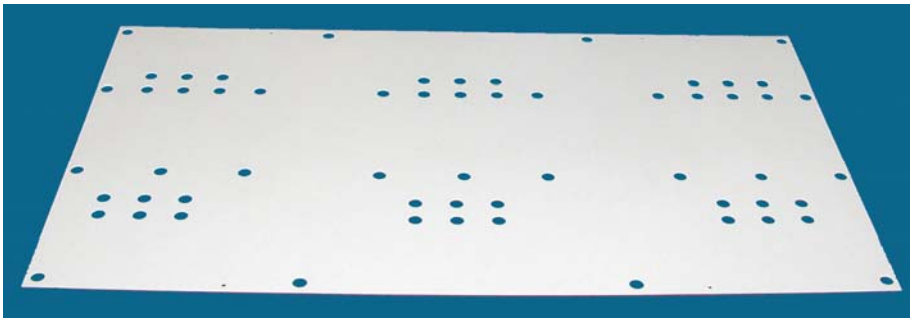
(a)



(b)



(c)



(d)

Figure 3.31 Implemented Laminated Busbar Layers
(a) : Positive Busbar Layer ; (b) : Negative Busbar Layer
(c) : AC Busbar Layer ; (d): Isolation Layer

Verification of the effective DC link inductance can be done by two different techniques.

The first technique finds effective DC link inductance by measuring the resonance frequency which is caused by the DC link capacitors and the effective DC link inductance within the path. Test circuitry is shown in Fig. 3.32 [54].

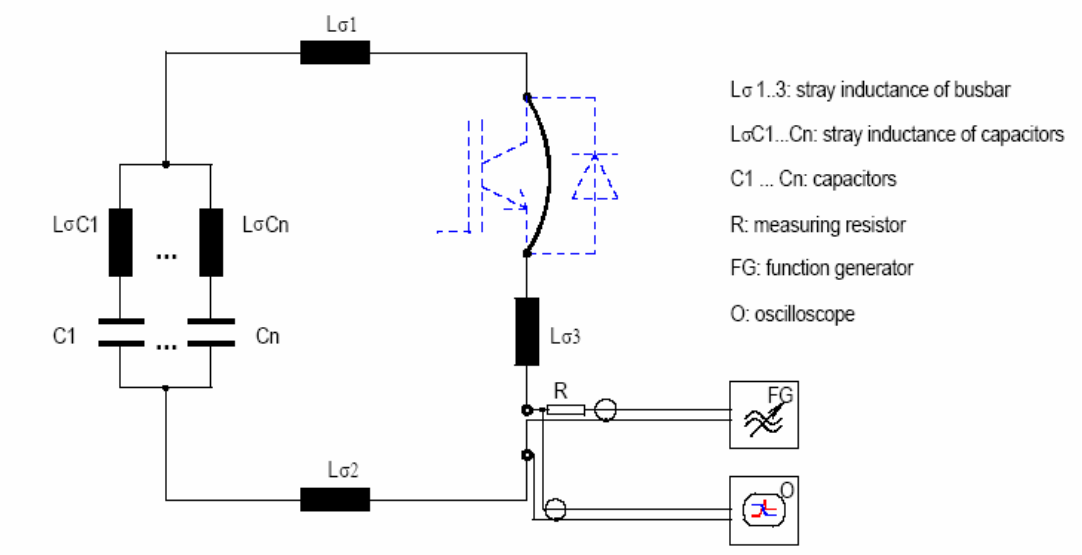


Figure 3.32 Test Circuitry For Measuring Effective DC Link Inductance

The upper HV IGBT module is shorted in the test and a sinusoidal voltage with varying frequency is applied on the terminals of lower HV IGBT module through a resistance which is needed to limit the test current. Therefore, this test must be carried out before assembling the converter. Frequency is changed until the phase angle between the collector-emitter voltage and the current through the resistance is reduced to zero.

$$L_{eff} = \frac{1}{(2\pi f_{res})^2 C_d} \tag{3.21}$$

C_d represents the total DC link capacitor. L_{eff} represents effective dc link inductance excluding the inner inductances of HV IGBT modules. f_{res} is found to be 18 kHz in the tests. Hence test inductance is found to be 52 nH. Hence, effective DC link inductance is 72 nH including the inner inductances of HV IGBT modules.

The second technique employs the half-bridge switching test and founds the effective DC link inductance from turn-off and turn-on switching voltage waveforms of HV IGBT module [57].

Switching test circuitry is shown in Fig. 3.33.

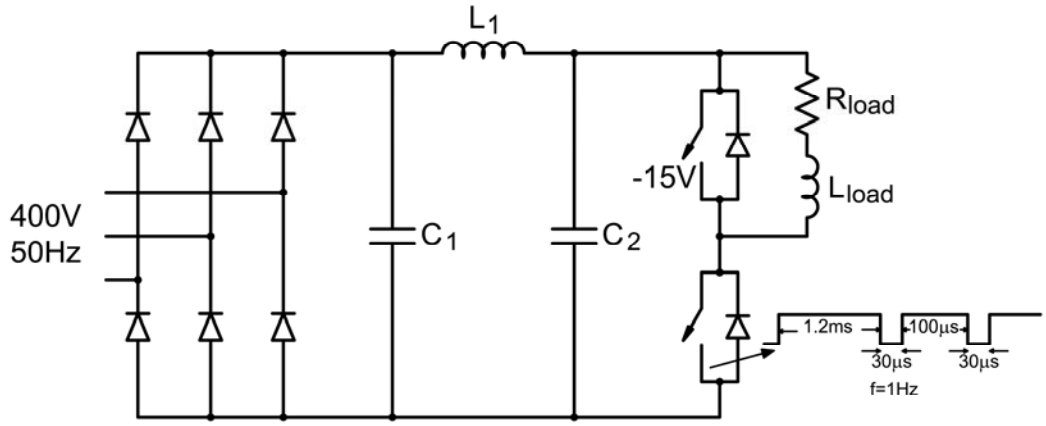


Figure 3.33 Switching Test Circuitry For Measuring DC Link Inductance

The test is carried out at 1200 A which is the rated current of CM1200HC-66H. C_1 represents the bulk capacitance needed to support the DC link voltage when lower HV IGBT module is on. L_1 is the cable inductance between the diode rectifier and the inverter. C_2 represents the DC link capacitors of the inverter and switching currents circulate through C_2. Test values of the passive elements are given below :

$C_1 = 15.6$ mF ; $L_1 = 500$ nH; $C_2 = 1.527$ mF; $R_{load} = 0.3\Omega$, $L_{load} = 200\mu H$

A pulse of 1.2 ms is applied in order to constitute 1200 A load current through the HV IGBT module. Following the freewheeling operation of load current in the

FWD of upper HV IGBT module for a duration of 30 µs, the lower HV IGBT module is turned on at 1200 A. Hence, switching waveforms are recorded at 1200 A during both the turn-on and turn-off process.

Turn-off switching waveform recorded in the laboratory is shown in Fig. 3.34. Turn-off peak voltage is calculated from (3.22).

$$V_{CE_p} = V_d - L_{eff}\frac{dI_{c,off}}{dt} \tag{3.22}$$

$$\Delta V_{off} = 320\ V;\ \frac{di_{off}}{dt} = 5.4\ kA/\mu S$$

L_{eff} is found to be 59.3 nH which is much smaller than the effective dc link inductance prespecified and CM1200HC-66H is kept in RBSOA safely at the rated current.

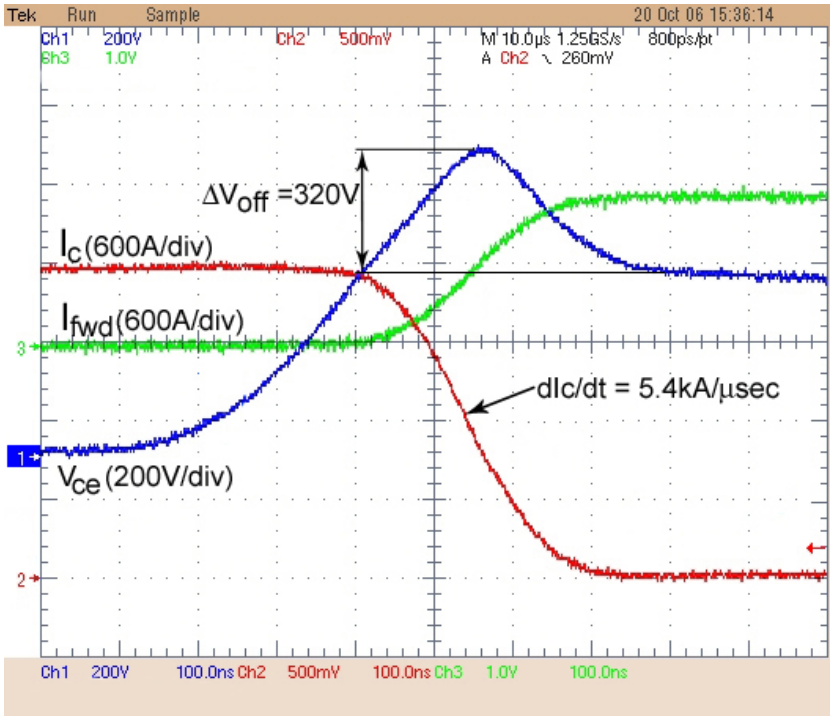


Figure 3.34 Turn-Off Switching Waveform of CM1200HC-66H at 1200A
Ch1 : Collector-emitter voltage, 200V/div, Ch2 : Collector Curent :1.67mV/A
Ch3 : FWDi current : 1.67mV/A

Effective DC link inductance is also found from turn-on switching waveform by measuring the voltage drop across the HV IGBT module in (3.23) when HV IGBT is blocking and collector current is rising.

$$\Delta V_{on} = L_{eff} \frac{dI_{c,on}}{dt} \tag{3.23}$$

Turn-on switching waveform which is recorded in the laboratory is as shown in Fig. 3.35. One can obtain from the waveforms $\Delta V_{on} = 150\,V$ and $\frac{di_{on}}{dt} = 3.3\,kA/\mu S$. These yield the value of effective dc link inductance as 45.3 nH.

Turn-on di/dt is also measured in order to check RRSOA of HV IGBT module at rated current. $dI_{c,on}/dt$ is found as 3.3 kA/μs in the tests**.** This value must be smaller than 5.5kA/μs according to the manufacturer specification. Hence, CM1200HC-66H is kept in RRSOA safely at the rated current.

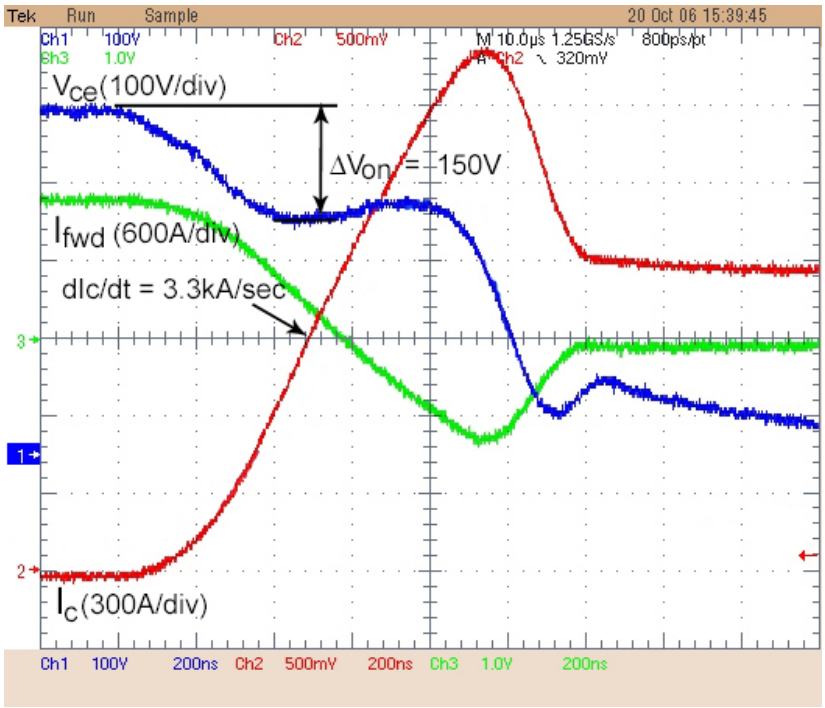


Figure 3.35 Turn-On Switching Waveform of CM1200HC-66H at 1200A
Ch1 : Collector-emitter voltage, 200V/div, Ch2 : Collector Curent :1.67mV/A
Ch3 : FWDi current : 1.67mV/A

Theoretical effective DC link inductance is given in Table 3.12. Busbar dimensions are taken as 30cm x 40cm (wxl) in the calculations. Internal and external inductances are calculated by using (3.14) and (3.15). DC link capacitors are sprinkled down each leg and self inductance of the selected DC link capacitor is assumed to be 25nH. It is very difficult to find an accurate analytical calculation of the effective busbar inductance because of the complex geometry of the busbar. However, it can be approximated by (3.24).

$$L_{eff} = L_i + L_{e_1} + L_{e_2} + \frac{L_{dc,cap}}{3} + L_{spacer} + 2L_{IGBT} \quad (3.24)$$

Table 3.12 Theoretical Calculation of Effective DC Link Inductance

Internal Inductance	20nH
External Inductance (L_{e1})	3.3 nH
HV IGBT Internal Inductance (x2)	20 nH
Screw and Spacer Inductance	10nH
DC link capacitor inductance (x3)	9nH
Total	62.3 nH

L_{e2} is neglected in the calculation because of the layout of DC link capacitors on the laminated busbars. Inductances between the DC link capacitors which is caused by the busbar structure are also neglected in the calculations. Theorotical and experimental effective DC link inductances are nearly the same (Theorotical : 62.3nH; Technique 1 : 72 nH; Technique 2: 45.3-59.3 nH). Therefore, effective DC link inductance is kept under recommended upper limit of 100 nH safely.

3.3.2 Heatsink Design

PSCAD simulations are carried out for capacitive and inductive mode of operations at source voltages of 28kV, 31.5kV and 36kV. Total power loss of a HV IGBT module can be calculated as in (3.25) and (3.26).

$$P_{tot} = P_{con} + P_{swt} \tag{3.25}$$

$$P_{con} = I_{c_{av}} \times V_{ce,sat} \tag{3.26}$$

Switching curves are given in the datasheets for V_{CC}=1650V; R_g=1.6Ω and T_j=125°C. However, the turn-on and turn-off resistances are fixed by the driver as R_{gon} = 1.7 Ω and R_{goff} = 3.7 Ω. The relation between the switching energies and turn-on/turn-off resistors of CM1200HC-66H are specified in the datasheets [53].

$$E_{on\ 1.7\Omega} = 1.2 \times E_{on1.6\Omega} \tag{3.27}$$

$$E_{off\ 3.7\Omega} = 1.1 \times E_{off3.7\Omega} \tag{3.28}$$

$$E_{rec\ 1.7\Omega} = 0.95 \times E_{rec1.6\Omega} \tag{3.29}$$

A typical HV IGBT current waveform (only IGBT part) is shown in Fig. 3.36.

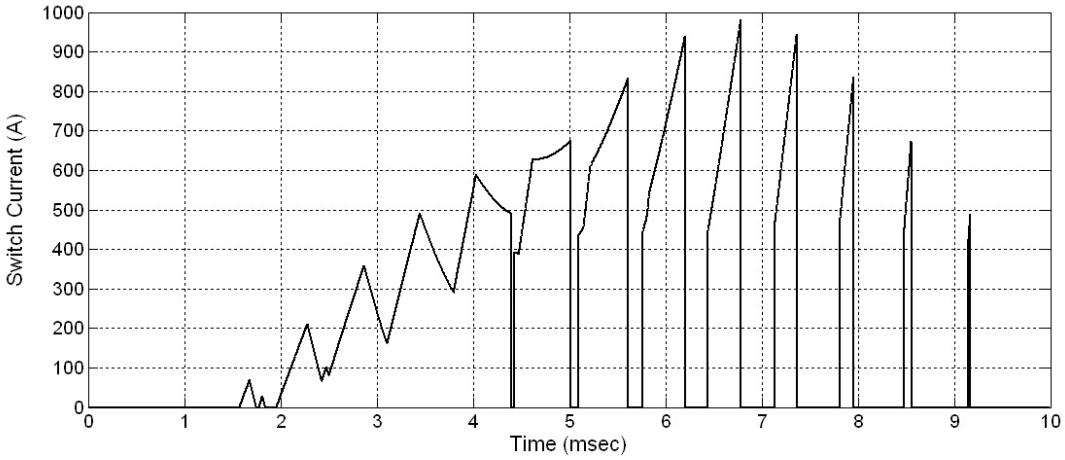


Figure 3.36 A Typical HV IGBT Module Current (IGBT Part, PSCAD/EMTDC)

E_{on} and E_{off} are calculated from (3.30) and (3.31) for each pulse shown in Fig. 3.37. E_{rec} is similiarly calculated from the current waveform of FWD of the HV IGBT module by using (3.32).

$$E_{on} = \frac{V_d}{1650} \sum_{k=1}^{n} E_{on}(k) \tag{3.30}$$

$$E_{off} = \frac{V_d}{1650} \sum_{k=1}^{n} E_{off}(k) \tag{3.31}$$

$$E_{rec} = \frac{V_d}{1650} \sum_{k=1}^{n} E_{rec}(k) \tag{3.32}$$

where n represents the number of pulses in the switching waveform and V_d is given in Table 3.7.

Switching losses part of active power loss can then be expressed as in (3.33).

$$P_{swt} = (E_{on} + E_{off} + E_{rec})50 \tag{3.33}$$

Calculated active power losses of the converter is given in Table 3.13.

Table 3.13 Active Power Losses of HV IGBT Modules in STATCOM

Source Voltage	Mode of Operation	P_{con} (W)	P_{swt} (W)	P_{total} (W)
31.5 kV	Capacitive	1090	410	1500
31.5 kV	Inductive	1058	460	1518
28 kV	Capacitive	1327	550	1877
28 kV	Inductive	895	392	1287
36 kV	Capacitive	945	323	1268
36 kV	Inductive	1318	564	1891

20 % safety margin is added to the calculated maximum power dissippation in Table 3.13 and heatsinks are designed for a conduction loss of 1.6 kW and a switching loss of 0.7 kW. Therefore, the maximum power dissipation on one HV IGBT module is accepted as 2.3kW in the calculations. Heatsink design is carried out for two HV IGBT module mounted on a common heatsink and each HV IGBT

module on a separate heatsink cases. Thermal model of the two designs are shown Fig. 3.37.

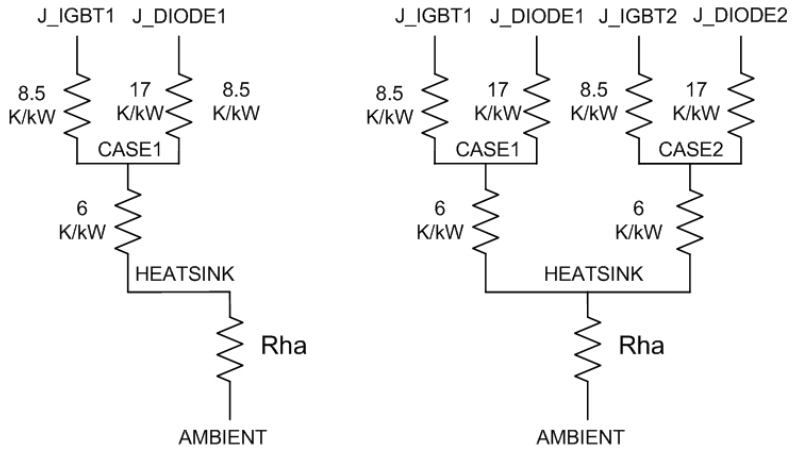


Figure 3.37 Heatsink Models

$$R_{ha} = \frac{T_j - T_a - R_{ch}P_{module} - \max(R_{jc,igbt}P_{igbt}, R_{jc,diode}P_{diode})}{nP_{module}} \qquad (3.34)$$

where n represents the number of modules on the heatsink.

$$R_{ha} = \begin{Bmatrix} 5.50\ \text{K/kW} & 1\ \text{HV IGBT Module on each heatsink} \\ 2.75\ \text{K/kW} & 2\ \text{HV IGBT Module on each heatsink} \end{Bmatrix}$$

Heatsink is selected according to 5.5K/kW specification since 2.75K/kW is very low and can be obtained only by custom designed expensive water cooled heatsinks.

5.5K/kW thermal impedance is obtained by water cooled heatsinks made out of copper with turbulators and the thermal impedance versus water flow rate curve of the selected heatsink is given in Fig.3.38. KSK200-320 water cooled heatsink is designed by Dau and a thermal impedance of 5.5K/kW is obtained at a water flow rate of 17lt/min.

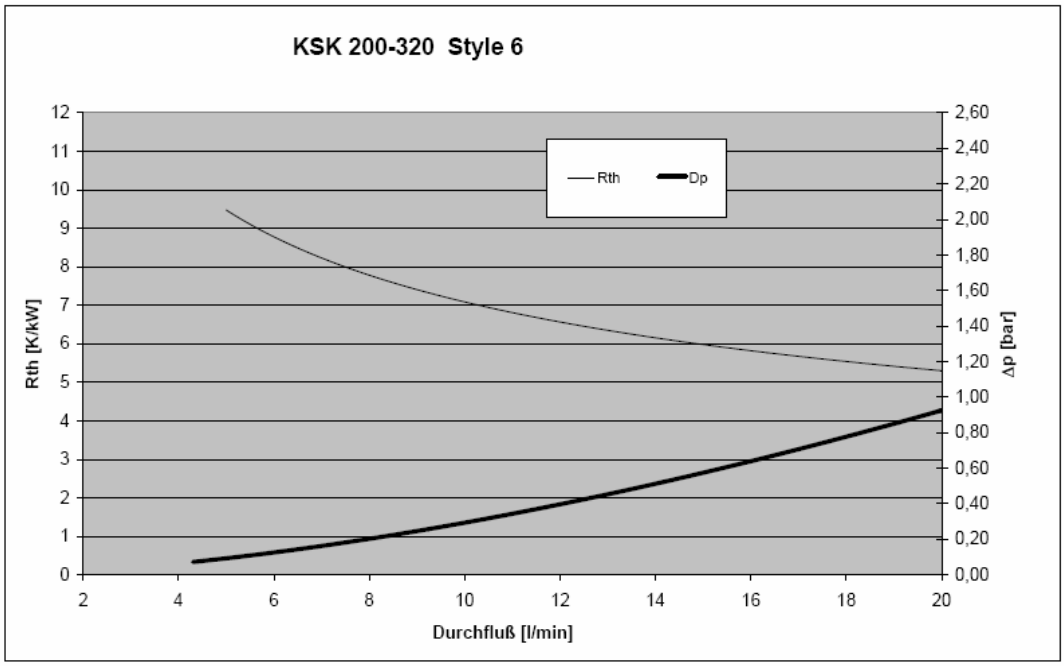


Figure 3.38 KSK200-320 R_{th} versus Water Flow Relation

3.3.3 Optimum Utilization of HV IGBT Modules

The following criteria must be guaranteed in the capacitive and inductive mode of operations in order to extend the life time of HV IGBT modules :

- DC link voltage must be kept lower than V_{LTDS} which is 2100V for CM1200HB-66H.
- HV IGBT module can be switched at two times the rated current as long as peak collector-emitter voltage is kept below 3300V and junction temperature is kept below 125°C. Driver card of CM1200HC-66H enters into active clamping after 2400V peak collector-emitter voltage. Therefore, it is aimed at keeping the peak collector-emitter voltage under 2400V in normal operation.

Peak collector-emitter voltage expected in the normal operation is calculated by using (3.22) and results are given in Table 3.14. Busbar inductance is assumed to be 60nH and turn-off current fall time is taken as 200 ns. Peak collector current values are found by PSCAD simulations.

Table 3.14 Peak HV IGBT Voltage and Current Values in Normal Operation

Source (kV)	$V_{statcom}$ (V)	$Q_{statcom}$ (kVAr)	I_{VSC} (A)	$I_{c,peak}$ (A)	V_d (V)	$V_{ce,peak}$ (V)
31.5	1148	-1503	367	820	1615	1861
36	1253	-1499	205	620	1763	1949
28	1071	-1501	510	980	1507	1801

HV IGBT module is operating safely in normal operating conditions. Simulations are carried out in order to find the reactive power limits of two level, three leg VSC with HV IGBT modules at nominal source voltage (31.5 kV). Input filter values are kept the same as in the present implementation. The reactive power rating has been found to be 2 MVAr from PSCAD simulations and the results are given in Table 3.15.

Table 3.15 Peak HV IGBT Voltage and Current Values for 2 MVAr VSC

Source (kV)	$V_{statcom}$ (V)	Q_{VSC} (kVAr)	I_{VSC} (A)	$I_{c,peak}$ (A)	V_d (V)	$V_{ce,peak}$ (V)
31.5	1323	-2000	1003	1782	1862	2397

As can be understood from Table 3.15, DC link voltage, peak collector-emitter voltage and peak collector current can be kept respectively below 2100 V, 2400 V and 2400 A by a careful design while the VSC is producing 2 MVAr.

DC link capacitor, input filter and coupling transformer should be redesigned because of increased line currents and DC link voltages.

The only difficulty with 2 MVAr converter is the increased power losses of HV IGBT modules. Active power losses of the converter is approximately 26 kW for 2MVAr converter. This dissipation necessiates the use of custom design water cooled heatsinks for single side cooled wire bond HV IGBTs. Second alternative is to use presspack HV IGBT modules because of double side cooling advantage. However, converter design must be renewed according to the presspack HV IGBT module specifications.

As a result, the reactive power rating of the converter can be increased up to 2 MVAr in the expense of special water cooled heatsinks and water cooling system with bigger capacity.

3.4 Design of Input Filter

Input filter design includes the selection of filter inductance and filter capacitor. Converter harmonics with 8-Angle SHEM are shown in Fig. 2.32. Fundamental and harmonic components of the line-to-neutral converter voltage are can be expressed as follows :

$$V_n = \frac{V_d}{2\sqrt{2}} b_n \tag{3.35}$$

$$b_n = \frac{4}{n\pi}\left[\begin{matrix} 1 - 2\cos n\alpha_1 + 2\cos n\alpha_2 - 2\cos n\alpha_3 + 2\cos n\alpha_4 \\ - 2\cos n\alpha_5 + 2\cos n\alpha_6 - 2\cos n\alpha_7 + 2\cos n\alpha_8 \end{matrix}\right] \tag{3.36}$$

Input filter is used to filter out switching harmonics of the converter and to improve the voltage THD and current TDD at PCC.

Input filter can be formed either by a single L or by a LC filter. Use of a single L filter necessiates higher inductance values when compared to LC filter combination in order to reach the same voltage THD and current TDD specification. Higher inductance values cause higher voltage regulation on the DC link capacitor from

full inductive mode to full capactive mode and slow down the step response to a reactive power change. Usage of higher filter inductance also causes higher DC link voltages for a predetermined value of reactive power which effect the rating of power semiconductors and DC link capacitor.

3.4.1 L Filter Design

Per phase equivalent circuit of the power system for converter harmonics is given in Fig. 3.39 for inductance only filter case (L). Source side behaves as short circuit at converter voltage harmonics. Current harmonics and total harmonic current at PCC can be expressed as in (3.37) – (3.39).

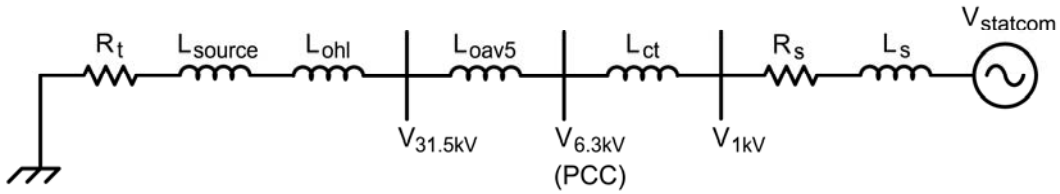


Figure 3.39 Single Line Model for Voltage Harmonics with L Filter

$$L_t = L_{source} + L_{ohl} + L_{OAV5} + L_{ct} \tag{3.37}$$

$$I_{statcom}(n) = \frac{V_d}{4\pi\sqrt{2}f_s(L_t + L_s)}\frac{b_n}{n} \quad , n\geq 5 \tag{3.38}$$

$$I_{statcom,har} = \frac{V_d}{4\pi\sqrt{2}f_s(L_t + L_s)}\sqrt{\sum_{k=5}^{\infty}\frac{b_k^2}{k^2}} \tag{3.39}$$

where f_s is the source frequency. Σ term in equation (3.39) is constant for 8-Angle SHEM and found to be 0.0162 according to the chopping angles given in Table 2.5. Hence, total harmonic current is simplified as given in (3.40).

$$I_{statcom,har} = \frac{1.823x10^{-5}V_d}{(L_t + L_s)} \tag{3.40}$$

Fundamental current is calculated from the rated power of VSC (3.41).

$$I_{fund} = \frac{Q_{statcom}}{\sqrt{3}V_{lkV}} \tag{3.41}$$

Percentage TDD of STATCOM line current can be expressed as in (3.42).

$$I_{statcom,TDD} = \frac{3.157x10^{-3} V_d V_{lkV}}{(L_t + L_s)Q_{statcom}} \ (\%) \tag{3.42}$$

$$L_s = \frac{3.157x10^{-3} V_d V_{lkV}}{I_{statcom,TDD} Q_{statcom}} - L_t \tag{3.43}$$

Voltage harmonics and total harmonic voltage at PCC are given in (3.44) - (3.47).

$$V_{statcom}(n) = \frac{V_d (L_{source} + L_{ohl} + L_{oav5})}{2\sqrt{2}(L_t + L_s)} b_n \tag{3.44}$$

$$V_{statcom,har} = \frac{V_d (L_{source} + L_{ohl} + L_{oav5})}{2\sqrt{2}(L_t + L_s)} \sqrt{\sum_{k=5}^{\infty} b_k^2} \tag{3.45}$$

Σ term in (3.45) is constant for 8-Angle SHEM and found 0.6181 according to the chopping angles given in Table 2.5.

$$V_{statcom,har} = \frac{0.218 V_d (L_{source} + L_{ohl} + L_{oav5})}{(L_t + L_s)} \tag{3.46}$$

$$V_{statcom,THD} = \frac{21.8 V_d (L_{source} + L_{ohl} + L_{oav5})}{(L_t + L_s)V_{lkV}} \ (\%) \tag{3.47}$$

$$L_s = \frac{21.8 V_d (L_{source} + L_{ohl} + L_{oav5})}{V_{statcom,THD} V_{lkV}} - L_t \tag{3.48}$$

Converter voltage harmonics are directly related to DC link voltage. Harmonic voltages increases in capacitive mode of operation and decreases in inductive mode of operation.

Current TDD and Voltage THD values are tabulated in Table 3.16 for different filter inductances. Current TDD is given as a percentage of VSC line current at rated reactive power (± 750 kVAr).

Table 3.16 Current TDD and Voltage THD for Different L Input Filter Parameters

Filter Inductance (µH)	I_TDD (%)	V_THD (%)
500	10.5	5
1000	6.7	3.2
1500	5.1	2.4

As seen from Table 3.16, current TDD and voltage THD specification can be reached with a filter inductance of 1.5 mH. However, higher inductance value has the drawbacks discussed in the beginning of this section. Therefore, if the drawbacks of higher filter inductance values are not acceptable for a successful performance, a lowpass LC filter is to be used as the input filter.

3.4.2 Low Pass LC Filter Design

Per phase equivalent circuit for converter harmonics is given in Fig. 3.40 for lowpass LC filter case.

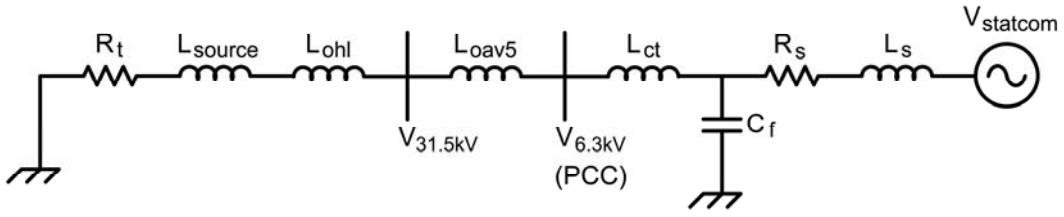


Figure 3.40 Single Line Model for Voltage Harmonics with Lowpass LC Filter

Converter and STATCOM current harmonics are calculated in terms of converter harmonic voltage and passive elements shown in Fig. 3.40 and given in (3.49) - (3.51).

$$I_{VSC}(n) = \frac{V_d}{4\pi\sqrt{2}f_s} \frac{b_n(1+4\pi^2 f_s^2 L_t C_f n^2)}{n(L_t + L_s + 4\pi^2 f_s^2 L_t L_s C_f n^2)} \tag{3.49}$$

$$I_{statcom}(n) = \frac{V_d}{4\pi\sqrt{2}f_s} \frac{b_n}{n(L_t + L_s + 4\pi^2 f_s^2 L_t L_s C_f n^2)} \tag{3.50}$$

$$I_{statcom,har} = \frac{V_d}{4\pi\sqrt{2}f_s} \sqrt{\sum_{k=5}^{\infty} \frac{b_k^2}{k^2(L_t + L_s + 4\pi^2 f_s^2 L_t L_s C_f k^2)^2}} \tag{3.51}$$

$$I_{statcom,TDD} = \frac{0.195 V_d V_{1kV}}{Q_{statcom}} \sqrt{\sum_{k=5}^{\infty} \frac{b_k^2}{k^2(L_t + L_s + 4\pi^2 f_s^2 L_t L_s C_f k^2)^2}} \ (\%) \tag{3.52}$$

Voltage harmonics and total harmonic voltage at PCC are given in (3.53) and (3.55).

$$V_{statcom}(n) = \frac{V_d L_t}{2\sqrt{2}} \frac{b_n}{(L_t + L_s + 4\pi^2 f_s^2 L_t L_s C_f n^2)} \tag{3.53}$$

$$V_{statcom,har} = \frac{V_d L_t}{2\sqrt{2}} \sqrt{\sum_{k=5}^{\infty} \frac{b_k^2}{(L_t + L_s + 4\pi^2 f_s^2 L_t L_s C_f k^2)^2}} \tag{3.54}$$

$$V_{statcom,THD} = \frac{35.3 V_d L_t}{V_{1kV}} \sqrt{\sum_{k=5}^{\infty} \frac{b_k^2}{(L_t + L_s + 4\pi^2 f_s^2 L_t L_s C_f k^2)^2}} \ (\%) \tag{3.55}$$

Voltage harmonics and total harmonic voltage at 1kV can be expressed as in (3.56) and (3.58).

$$V_{statcom}(n) = \frac{V_d L_x}{2\sqrt{2}} \frac{b_n}{(L_t + L_s + 4\pi^2 f_s^2 L_t L_s C_f n^2)} \tag{3.56}$$

$$V_{statcom,har} = \frac{V_d L_x}{2\sqrt{2}} \sqrt{\sum_{k=5}^{\infty} \frac{b_k^2}{(L_t + L_s + 4\pi^2 f_s^2 L_t L_s C_f k^2)^2}} \quad (3.57)$$

$$V_{statcom,THD} = \frac{35.3 V_d L_x}{V_{1kV}} \sqrt{\sum_{k=5}^{\infty} \frac{b_k^2}{(L_t + L_s + 4\pi^2 f_s^2 L_t L_s C_f k^2)^2}} \ (\%) \quad (3.58)$$

where $L_x = L_{source} + L_{ohl} + L_{oav5}$

Curent TDD and voltage THD are tabulated in Table 3.16 for different LC filter parameters. Current TDD is given as a percentage of VSC line current at rated reactive power (± 750 kVAr).

As seen from Table 3.17, a filter capacitance with a reactive power rating of 10-20 % of the converter rating is enough to filter out the switching harmonics. The main problem appears in the voltage THD at 1kV level. IEEE 519-1992 does not limit the voltage THD at 1kV as long as the voltage THD at PCC is kept lower than 5 %. However, higher voltage THD at 1kV brings EMC problems to the system and can disturb the operation of sensitive electronic equipment of STATCOM system. Therefore, it is also aimed to keep voltage THD value at 1kV lower than 3 %. This necessiates the use of higher filter inductance values for the same filter capacitor value.

Table 3.17 Current TDD and Voltage THD for Different Lowpass LC Input Filter Parameters (Q_f=750kVAr)

Filter Reactor (µH)	Filter Capacitance (mF)	I_TDD PCC (%)	V_THD PCC (%)	V_THD 1kV (%)
380	0.1215 (Q_f/20)	4.9	6.1	1.8
1000	0.1215 (Q_f/20)	2.3	2.8	0.8
220	0.243 (Q_f/10)	4.9	6.0	1.8
600	0.243 (Q_f/10)	2.3	2.8	0.8
200	2.43 (Q_f)	0.8	0.9	0.3
300	**2.43 (Q_f)**	**0.5**	**0.6**	**0.2**
400	2.43 (Q_f)	0.4	0.5	0.1

An input filter capacitance with a reactive power production capacity of 750kVAr is chosen in the design. This is done in order to double the reactive power rating of the converter and to supply the reactive power demand of the load. 750kVAr filter capacitor can be obtained by one of the following approaches.

1) 750kVAr filter capacitor can be divided into two groups of capacitor banks. First group is designed with a reactive power rating of 10-20 % of the converter to filter out the switching harmonics and formed by power electronic capacitors. The second group is designed by power capacitors as a tuned filter to filter out the harmonics of the load or as a detuned filter to prevent the risk of sinking of load harmonic currents. However, higher filter inductance values are required to keep voltage THD value lower than 3 % at 1kV as seen from Table 3.17.
2) 750kVAr filter capacitor is designed by power electronic capacitors as a single capacitor bank and filter capacitor suppresses most of the harmonic content of the converter current. Therefore, input filter inductance value is decreased at the expense of increased voltage and current ratings of the filter capacitor. This approach has also higher cost than the first approach because of 40 % price difference between power and power electronics capacitors.

Harmonic current content of the loads in KEAS Coal Preparation System is low as shown in Fig. 3.5. Higher filter inductance values are not preferred also because of the drawbacks discussed. Therefore, second approach is selected and 750kVAr filter capacitor is designed by power electronic capacitors at the expense of higher costs. From the given filter inductance values for Q_f in Table 3.17, 300μH is selected.

Filter inductance is designed as a three-phase reactor placed on the common iron core. 5 % saturation is allowed in the inductance value from 50Hz to 10kHz. Simulations are carried out at 31.5kV, 36kV and 28kV source voltages for capacitive and inductive mode of operation and specifications found are given in Table 3.18. Filter inductance is designed by Mangoldt according to the specifications given in Table 3.18. Designed filter inductance is shown in Fig. 3.41.

Table 3.18 Harmonic Spectrum of Filter Inductance Current

f (Hz)	I_n(A)	f (Hz)	I_n(A)
50	550	3650	5
1450	60	4450	10
1550	80	4550	10
1750	40	4750	10
1850	15	4850	5
2950	20	5050	10
3050	20	5150	5
3250	15	5950	5
3350	20	6050	5
3550	5	6050<f<10000	< 5

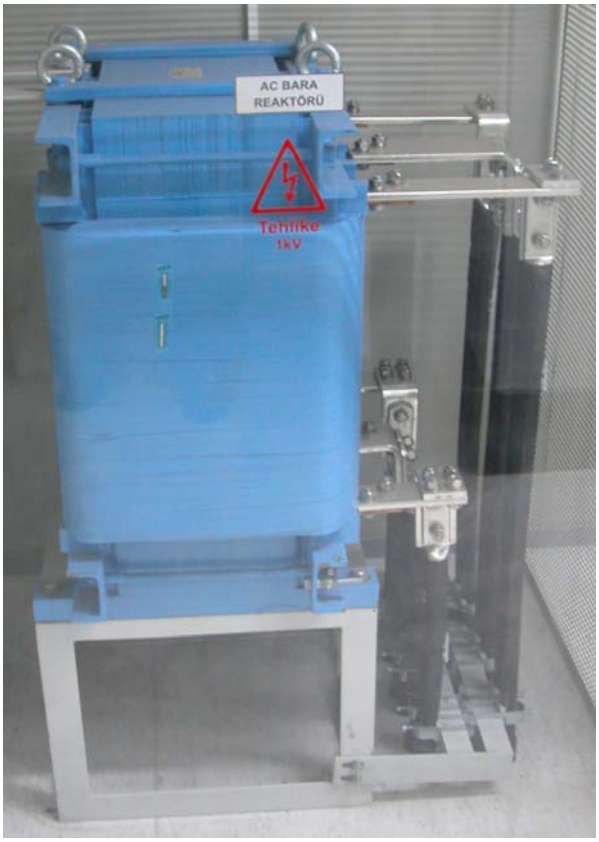


Figure 3.41 Filter Inductance

Filter capacitors have to be chosen from power electronic capacitors as discussed before. Simulations are carried out at 31.5kV, 36kV and 28kV source voltages for capacitive and inductive mode of operation. Voltage rating is found as the sum of fundamental and harmonic voltages. Current rating is expressed in rms value. The results are given in Table 3.19.

Filter capacitors must have low equivalent series resistors and high resonant frequencies. Filter capacitors are delta connected as shown in Fig. 3.15. Reactive power rating of the filter capacitors is 750kVAr at 1kV.

Table 3.19 Voltage and Current Ratings of Filter Capacitor

Source (kV)	**$Q_{statcom}$ (kVAr)**	**V_{1kV} (V)**	**V_d (V)**	**ΣV_k (V)**	**I_{rms} (A)**
31.5	-1502	1085	1614	1100	488
	4	1000	1302	1012	448
36	-1505	1218	1763	**1234**	**547**
	6	113	1487	1157	512
28	-1500	984	1506	998	443
	4	889	1157	900	398

C_f is found from (3.1). Phase values are C_Y = 2.38 mH and C_Δ = 793 μH. Filter capacitors are designed as 9 parallel capacitors and are chosen from Electronicon E62 series [58]. Technical specifications of this capacitor are given in Table 3.20.

Table 3.20 Filter Capacitor Specifications

U_N	3400VDC/2000VAC	
U_{RMS}	1400V	
C_N	90µF	
R_S	1.1mΩ	
F_{res}	38kHz	
I_{max}	100A	

Therefore, a capacitor having electrical ratings of 810 µF/1400 V/ 900 A is obtained by delta connected capacitors and electrical specifications of the filter capacitor are met safely. This capacitor group is shown in Fig. 3.42.

Figure 3.42 Filter Capacitance

AC analysis is carried out for VSC side and source side harmonics by using the choosen filter parameters. Fig. 3.43 shows converter and source side harmonic current spectrum caused by unit AC voltage VSC harmonics.

Converter produces harmonic voltages and thereby harmonic current components higher than 29th harmonic as a result of 8-Angle SHEM and it is seen that converter current harmonics are suppressed successfully.

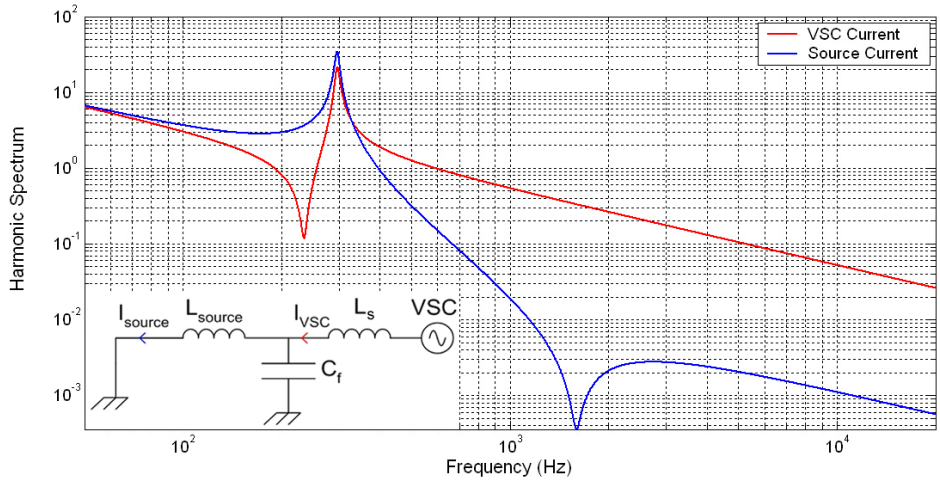


Figure 3.43 AC Analysis of STATCOM for Converter Current Harmonics

Source impedance is firstly calculated when VSC is disconnected from the 1kV bus and shown in Fig. 3.44.

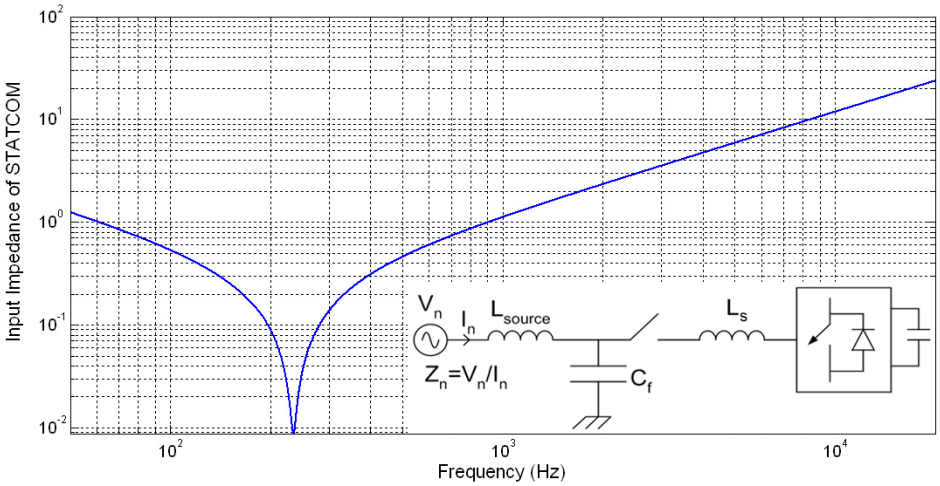


Figure 3.44 AC Analysis of STATCOM for AC Grid Harmonics when VSC is disconnected from the 1kV bus

Source impedance when VSC is connected to the 1kV bus is shown in Fig. 3.45.

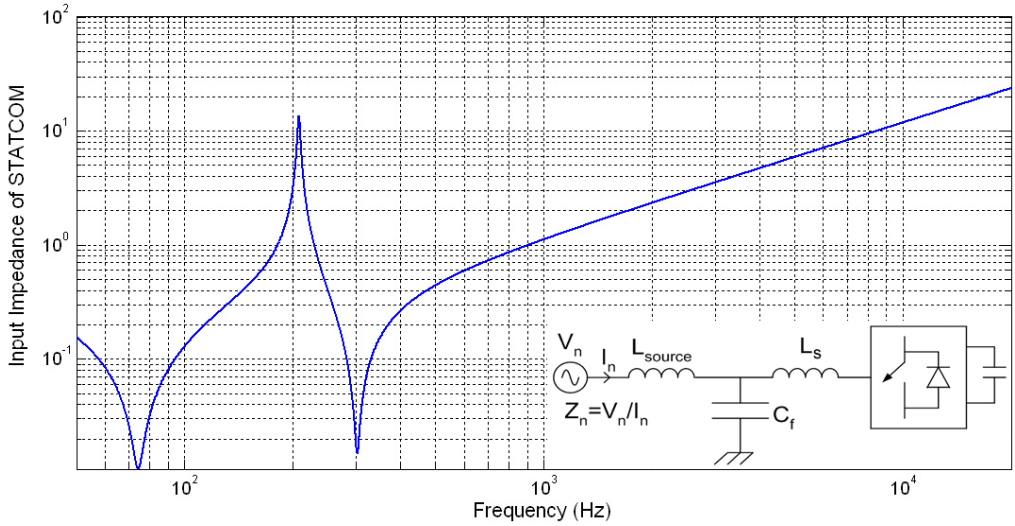


Figure 3.45 AC Analysis of STATCOM for AC Grid Harmonics when VSC is connected to the 1kV bus

Table 3.21 Source Impedance for 5th and 7th Harmonics

Condition	Source Impedance At 5th Harmonic	Source Impedance At 7th Harmonic
VSC is disconnected from 1kV Bus	35mΩ	228mΩ
VSC is connected to 1kV Bus	415mΩ	155mΩ

It is seen that VSC operation changes the source impedance characteristic. Sinked 5th harmonic current decreases significantly and sinked 7th harmonic current increases slightly when VSC is in operation.

3.5 Design of DC Link Capacitor

Following points should be considered carefully in the design of DC link capacitor.

i) Peak-to-peak ripple voltage of DC link capacitor must be lower than 5-10 % of average DC link voltage. Large capacitor size is better for lower harmonic distortion in AC side.

ii) Open loop response of STATCOM is dependent on the value of DC Link capacitor. Smaller capacitor size is better for fast response.

iii) DC link capacitor must have very low equivalent series inductance in order to form a low inductance DC link construction.

Harmonic content of the DC link capacitor voltage is found by writing energy balance equations in (3.59) for the converter [17].

$$V_d I_d = V_{A0} i_a + V_{B0} i_b + V_{C0} i_c \tag{3.59}$$

V_{A0}, V_{B0} and V_{C0} represent the converter line-to-neutral voltages and i_a, i_b and i_c the converter line currents. These are given in (3.60) – (3.65).

$$V_{A0} = \frac{V_d}{2} \sum_{k=1}^{\infty} a_n \sin(k w_0 t) \tag{3.60}$$

$$V_{B0} = \frac{V_d}{2} \sum_{k=1}^{\infty} a_n \sin(k(w_0 t - \frac{2}{3}\pi)) \tag{3.61}$$

$$V_{C0} = \frac{V_d}{2} \sum_{k=1}^{\infty} a_n \sin(k(w_0 t + \frac{2}{3}\pi)) \tag{3.62}$$

$$i_a = \sum_{k=1}^{\infty} I_n \cos(k w_0 t) \tag{3.63}$$

$$i_b = \sum_{k=1}^{\infty} I_n \cos(k(w_0 t - \frac{2}{3}\pi)) \tag{3.64}$$

$$i_c = \sum_{k=1}^{\infty} I_n \cos(k(w_0 t - \frac{2}{3}\pi)) \tag{3.65}$$

where I_n is given by Table 3.7 and (3.49). DC link current can then be expressed as in (3.66).

$$I_d = \frac{1}{2}\left\{\begin{array}{l} \sum_{k=1}^{\infty} a_n \sin(kw_0 t) \sum_{k=1}^{\infty} I_n \cos(kw_0 t) + \\ \sum_{k=1}^{\infty} a_n \sin(k(w_0 t - \frac{2}{3}\pi)) \sum_{k=1}^{\infty} I_n \cos(k(w_0 t - \frac{2}{3}\pi)) + \\ \sum_{k=1}^{\infty} a_n \sin(k(w_0 t + \frac{2}{3}\pi)) \sum_{k=1}^{\infty} I_n \cos(k(w_0 t - \frac{2}{3}\pi)) \end{array}\right\} \quad (3.66)$$

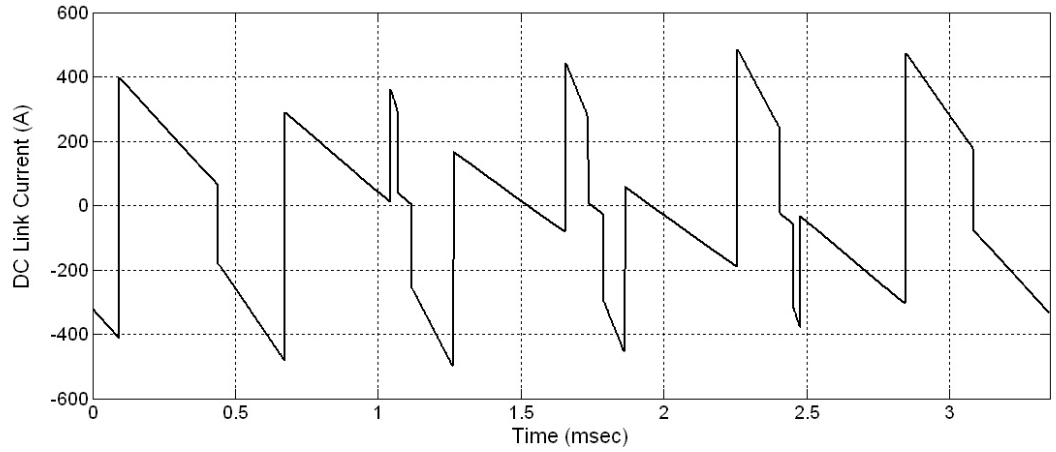
DC link capacitor voltage harmonics in (3.67) and (3.68) are found by using DC link current harmonics.

$$V_{d_n} = \frac{1}{2\pi f_s C_d} \frac{I_{d_n}}{n} \quad (3.67)$$

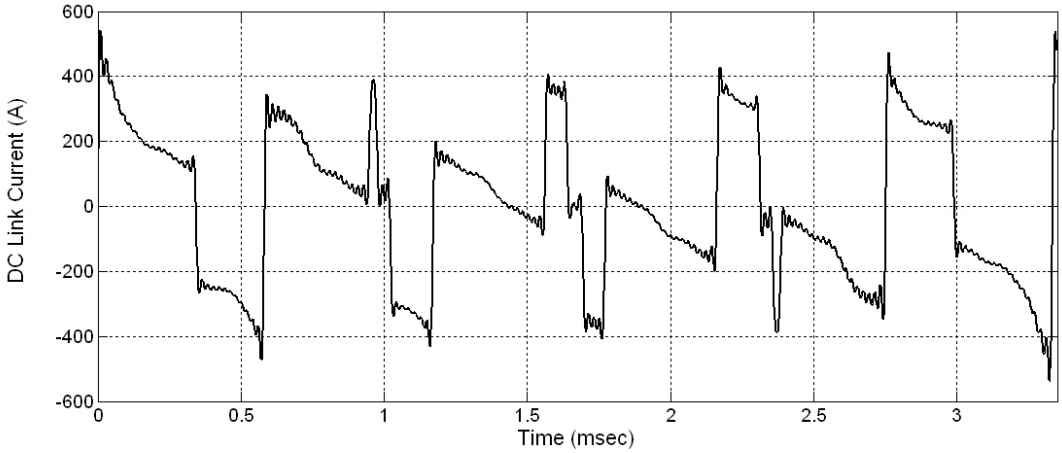
$$V_d = +V_{dc} \sum_{k=1}^{\infty} V_{d_n} \sin(kw_0 t) \quad (3.68)$$

Validity of the equations are checked by comparing the DC link current waveforms in MATLAB and PSCAD programs. Comparison is done at 1.5 MVAr reactive power generation at a source voltage of 31.5 kV. Waveforms found by MATLAB and PSCAD are similiar to each other as seen from Fig. 3.46.

It is seen from (3.66) that DC link capacitor harmonic current content depends on the chopping angles found in Chapter 2 and the converter input current. Hence, DC link capacitor current harmonics are independent of the DC link voltage. DC link voltage determines the maximum permissible peak-to-peak ripple voltage and limits the minimum value of DC link capacitor.



(a)



(b)

Figure 3.46 DC Link Capacitor Current Waveform
a : PSCAD ; b : MATLAB

Percentage DC link ripple voltage is given in (3.69).

$$K_v = \frac{(V_{d_{max}} - V_{d_{min}})}{V_{d_{av}}} \times 100 \tag{3.69}$$

Simulation results for different DC link capacitor values are as given in Table 3.22. Results include the operation in capacitive and inductive mode of operations at different source voltages. DC link capacitor values greater than 1.5mF keeps the percentage peak-to-peak voltage at a value lower than 5 % in all cases.

Table 3.22 Percentage Peak-to-Peak Ripple Voltage of the DC Link Capacitor

Source (kV)	$Q_{statcom}$ (kVAr)	I_{VSC} (A)	V_d (V)	I_{drms} (A)	C_d (mF)	K_v (%)
31.5	-1503	367	1615	215	1	4.6
					1.5	3.1
					2	2.3
	4	443	1302	264	1	7
					1.5	4.7
					2	3.5
36	-1499	205	1763	125	1	2.4
					1.5	1.6
					2	1.2
	6	507	1487	305	1	7.1
					1.5	4.7
					2	3.5
28	-1501	510	1507	304	1	7
					1.5	4.6
					2	3.5
	4	395	1157	236	1	7
					1.5	4.7
					2	3.5

Second point which is important in the selection of DC link capacitor is open loop response of STATCOM. Open loop dynamics of STATCOM system features a third order transfer function for small phase angles [1] as given in (3.70) – (3.73).

$$\frac{Q_{statcom}(s)}{\delta(s)} = \frac{V_{1kV}^2}{L} \frac{s^2 + \frac{R}{L}s + \frac{n^2}{2LC_d}}{s^3 + \frac{2R}{L}s^2 + \left\{\left(\frac{R}{L}\right)^2 + \frac{n^2}{2LC_d} + w^2\right\}s + \frac{n^2 R}{2L^2 C_d}} \tag{3.70}$$

where

$$R = R_t + R_s \tag{3.71}$$

$$L = L_t + L_s \tag{3.72}$$

$$n = \frac{\sqrt{3}}{2} m \tag{3.73}$$

n is found as 1.005 by using Table 2.5 and (3.36).

Effect of the filter capacitor on the open loop response of STATCOM is neglected since it is not required in every STATCOM application and has negligible effect on the open loop response. Root locus of the designed STATCOM with two different DC link capacitor value is shown in Fig. 3.47.

There are three poles of the characteristic equation for the STATCOM. One of the poles is on the negative real axis (s_1) and the other two poles (s_2 and s_3) are complex conjugate poles with negative real parts. Complex conjugate poles determine the oscillatory components and does not effect the open loop response of STATCOM. Pole on the negative real axis determines the open loop response of STATCOM. Open loop response time constant [22] is defined in (3.74).

$$T = -\frac{1}{s_1} \tag{3.74}$$

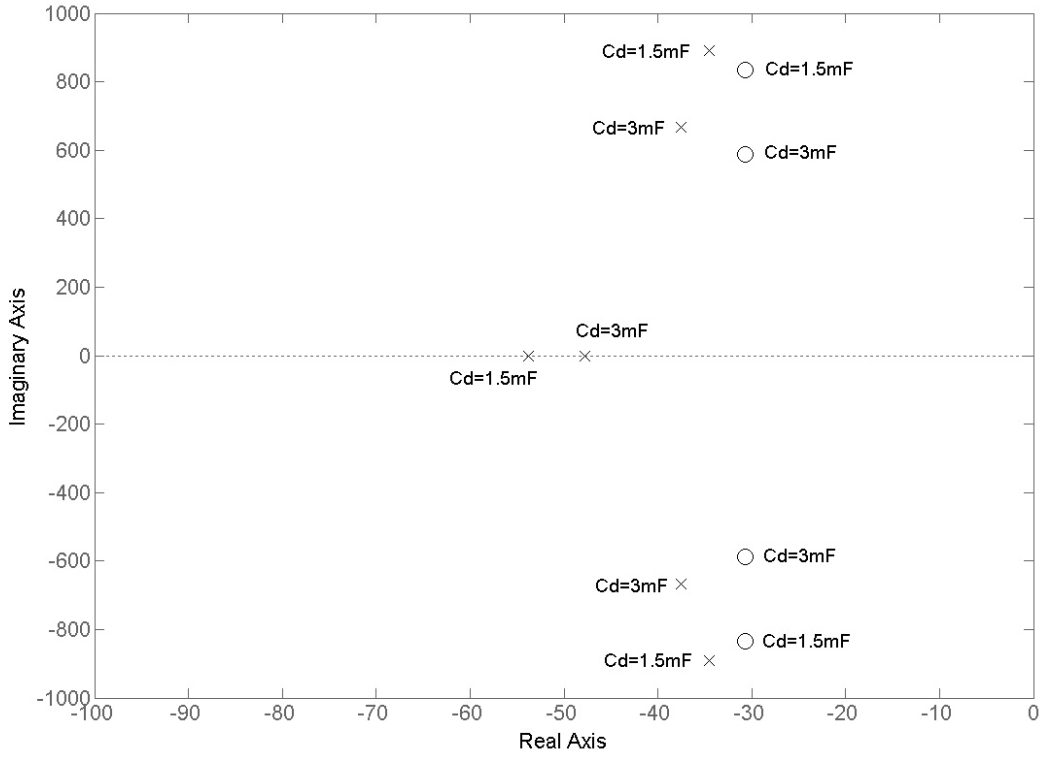


Figure 3.47 Effect of DC Link Capacitor on the Root Locus of Open Loop Transfer Function of STATCOM

s_1 decreases as the DC link capacitor increases and hence open loop response time constant increases too.

DC link capacitor must have low ESL and ESR values as discussed in 3.3.1. At low power applications, DC link capacitors are formed by paralelling electrolytic capacitors. However, this approach can not be used in medium power applications because of the voltage and current ratings of the DC link capacitor. The rating of the DC link capacitor is given in Table 3.23.

Table 3.23 Electrical Characteristics of the DC Link Capacitor

U_N	> 2000V DC
I_{max}	> 500 A
C_N	1.5-2mF
R_S	1mΩ
L_s	20< nH

The value of the DC link capacitor is specified according to Table 3.22. DC link capacitors meeting the specifications in Table 3.23 are not commercially available in the market with every capacitor value and voltage rating. Manufacturers prefer to design custom design capacitors according to the specifications only in case of high quantities. Epcos produces PCC- high power (HP) capacitors for converters with MKK (Metallized Polypropylene Film) technology. This product is preferred in VSC because of its outstanding advantages listed below :

1) PCC series capacitors are directly mounted on the laminated busbar. This decreases the effective dc link inductance when compared to the parallel combination of electrolytic/dry capacitors since it eliminates the cross connection between the DC link capacitor and laminated busbar. It also eliminates the need of decoupling capacitors on the DC link near to one leg.

2) Voltage and current ratings can be met in a single capacitor and this simplifies the design of the power stage.

3) PCC series capacitor have very low self inductances (~ 25nH) .

DC link capacitor is selected from the existing designs of PCC family meeting the required voltage and current levels. Three capacitor are used in VSC design and each capacitor is placed across each one-leg (Fig. 3.48). 509µF and 660µF are the alternative capacitor values which satisfy the specifications given in Table 3.23. 509 µF is selected since 5 % peak-to-peak ripple specification is satisfied and open loop response is better with 509 µF. Technical specifications of the selected DC link capacitor are given in Table 3.24.

Table 3.24 Technical Specifications of the DC Link Capacitor

U_N	2300V DC	
I_{max}	230A	
C_N	509µF	
R_S	0.7mΩ	
L_s	25 nH	
I_{max}	230A	

Figure 3.48 DC Link Capacitor Placament in VSC

3.6 Design of Control System

Control system strategy is chosen according to the required response time of STATCOM, load types and modulation techniques. Control techniques can be collected in two groups those using linear models and those nonlinear models.

DSTATCOM is a nonlinear system and linearized around the operating point to form a linear model [33]. PI controllers give superior responses around the operating point and typical choosen response time with PI controller is of the order of ~ 0.1 s. State feedback methods [32] using pole placement methods or linear quadratic regulator are the alternatives of PI controller for having fast responses than PI controllers. State feedback methods use input-output feedback linearization and dq transformation of the reference currents.

The performance of control system performance get worse with linear control methods when the operating condition changes as a result of parameter variation, nonlinearity or different loads. Nonlinear control methods such as sliding mode controller, fuzzy logic control and artifical neural networks are studied in the literature to overcome the problems of linear techniques and results are given only for computer simulations [33-35].

Active and reactive power change of KEAS OAH1 and OAH2 feeders are shown in Fig. 3.6 and Fig. 3.7 Active and reactive power demands of Coal Preparation System are slowly varying, these demands are varying in a wide range in the medium and long terms according to needs of the thermal power plant (up to 2 MW, and 2.2 MVAr for each line, when operated independently). The load structure is also definite for Coal Preparation System. Therefore, the problem is to supply the exact reactive energy demand of the load in the long time with a slow response. Phase angle control with PI controller is best suited for this application because of the required reactive power response, choosen modulation technique (8-Angle SHEM) and load structure.

Reactive power compensation of Coal Preparation System is achieved by measuring the reactive power demand on the source side and holding the source reactive power around zero by STATCOM. The control variable is the source reactive power in phase angle control. Hence, DC link voltage is indirectly controlled. Limits of the reactive power generation of STATCOM determines the voltage variation across the DC link capacitor from full inductive mode to full capacitive mode.

$$Q_{VSC} = 3\frac{V_{1kV}(V_{1kV} - 0.4103V_d)}{X_{L_s}} \tag{3.75}$$

Power stage of STATCOM is designed according to the reactive power specifications given in Table 3.3. for source voltages of V_{smin} = 28 kV, V_{srated} = 31.5 kV and V_{smax} = 36 kV. Putting a limit to the current requires different current limits for different source voltages. Reactive power generation at 6.3 kV is limited instead of putting a limit to the current. This automatically changes the the current limit at different source voltages. Error in reactive power which is the input of the PI loop can be expressed as in (3.76).

$$Q_{err} = Q_{ref} - Q_{source} \tag{3.76}$$

Q_{ref} can be different than zero if overall system needs to be operated at inductive or capacitive reference point. However, Q_{ref} is equal to zero in our application since the reactive power compensation is done at the active & reactive power metering point.

$$Q_{err} = -Q_{source} = (Q_{statcom} - Q_{source}) - Q_{statcom} = -Q_{load} - Q_{statcom} \tag{3.77}$$

Negative load reactive power is obtained by subtracting source reactive power from STATCOM reactive power. Reactive power of source side (KEAS OAH2 feeder) and STATCOM are measured by Reactive Power Measurement Cards (QR) which employ Average Basis Concept Technique described in 2.4.1. Reactive Power Measurement Card is shown in Fig. 3.49.

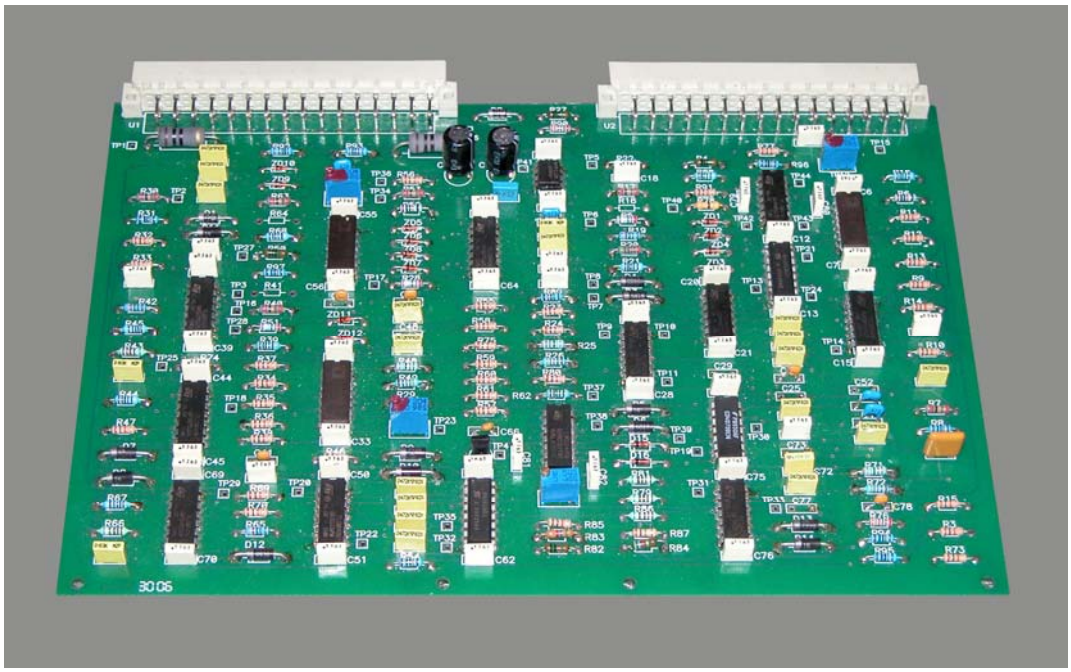


Figure 3.49 Reactive Power Measurement Card

Load reactive power goes above the limits of STATCOM at starting instants and in the period when there is a problem in KEAS OAH1 feeder or in the coal conveyor belt lines connected to KEAS OAH1 feeder (Fig. 3.3). Therefore, the reactive power generation of STATCOM must be limited by putting upper and lower limits on the measured negative load reactive power as given in (3.78) – (3.80).

$$\left[-Q_{load}\right]_{lim} = \begin{cases} -Q_{load} & 0 \le Q_{load} \le 1500 \\ -1500 & Q_{load} \ge 1500 \\ 0 & Q_{load} \le 0 \end{cases} \quad \text{(kVAr)} \qquad (3.78)$$

$$Q_{err} = \left[-Q_{load}\right]_{lim} - Q_{statcom} \qquad (3.79)$$

$$Q_{err} = \begin{cases} -Q_{source} & 0 \le Q_{load} \le 1500 \\ -1500 - Q_{statcom} & Q_{load} \ge 1500 \\ -Q_{statcom} & Q_{load} \le 0 \end{cases} \quad \text{(kVAr)} \qquad (3.80)$$

Limiting the load reactive power and processing the Q_{err} in PI loop are implemented in Control Card (KK) shown in Fig. 3.50.

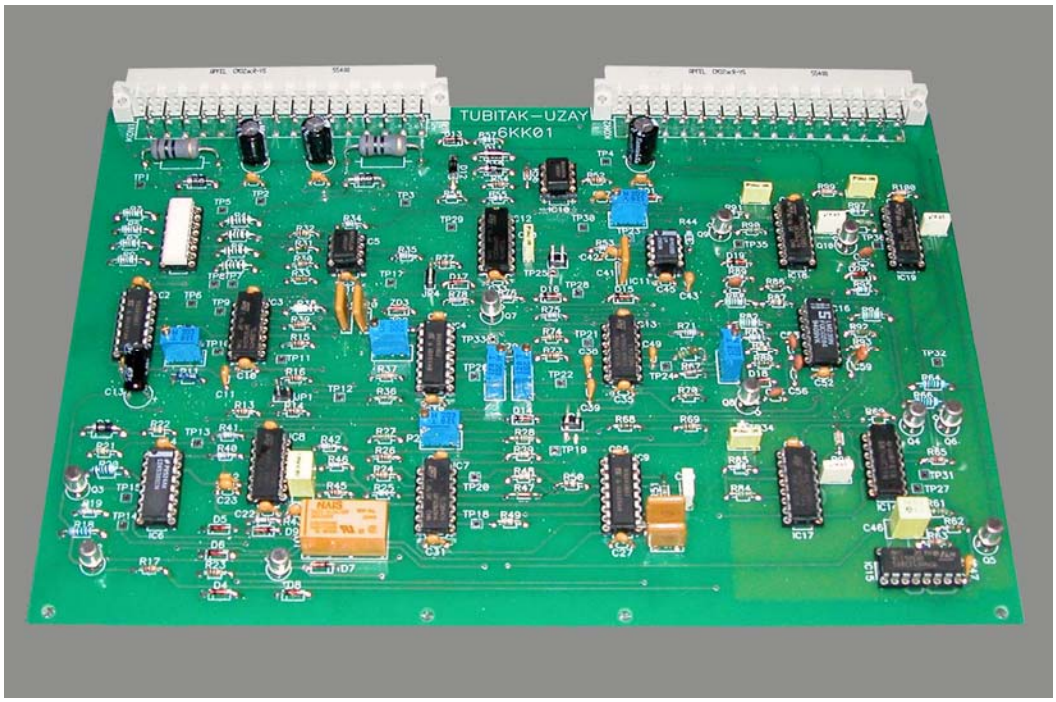


Figure 3.50 Control Card

Therefore, reactive power compensation is done at the source point as long as the reactive power limits of STATCOM are not exceeded. Maximum capacitive reactive power generation of STATCOM is limited to 1500 kVAr and maximum inductive reactive power generation of STATCOM is limited to 0 kVAr. If load reactive power exceeds the limits given in equation (3.78), STATCOM operates at the prespecified limit values.

Block diagram of the control system is shown in Fig. 3.51.

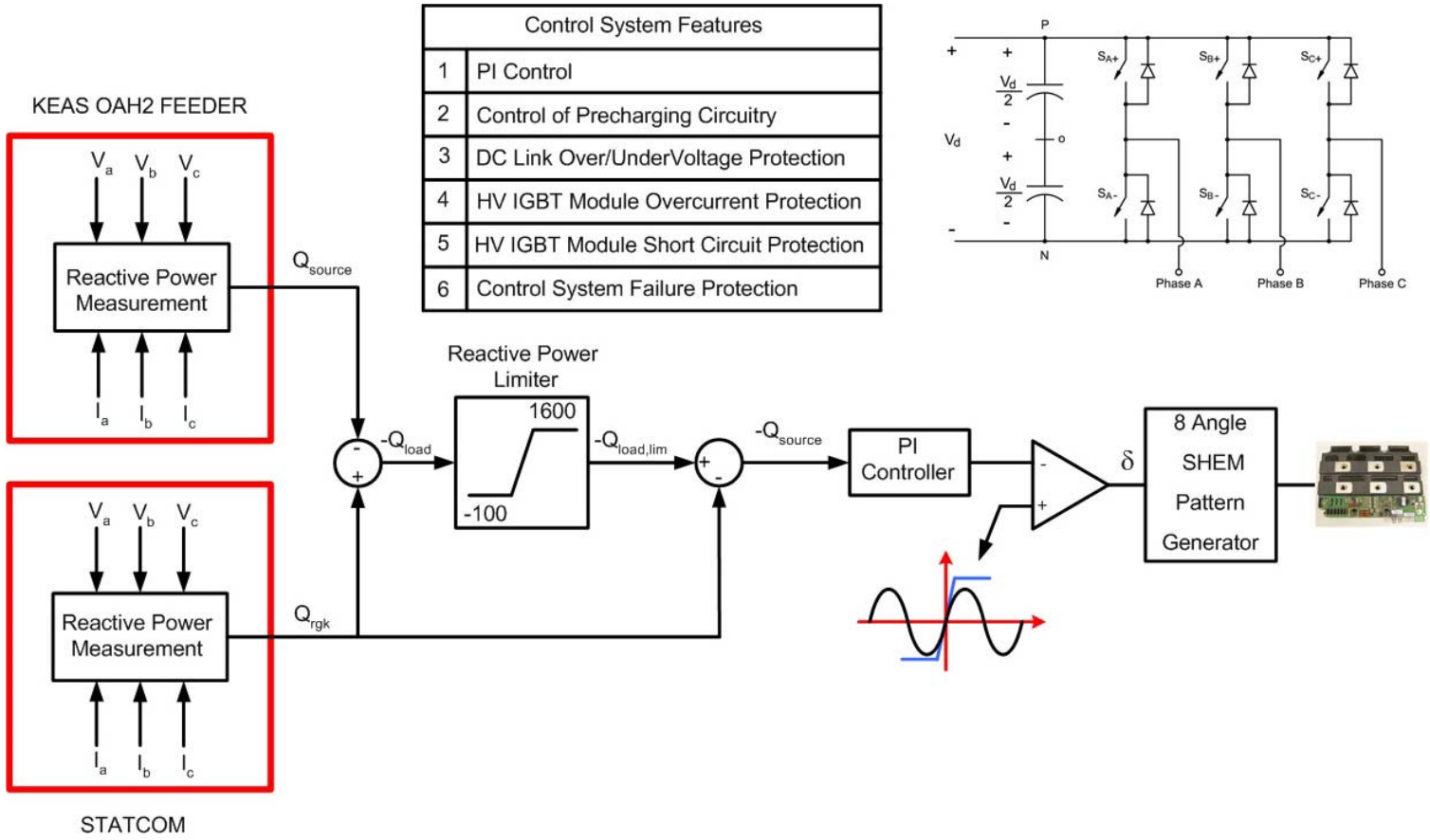


Figure 3.51 Control System of VSC STATCOM

Open loop transfer function of STATCOM is given in (3.81).

$$\frac{Q_{statcom}(s)}{\delta(s)} = \frac{V_{1kV}^2}{L} \frac{s^2 + \frac{R}{L}s + \frac{n^2}{2LC_d}}{s^3 + \frac{2R}{L}s^2 + \left\{\left(\frac{R}{L}\right)^2 + \frac{n^2}{2LC_d} + w^2\right\}s + \frac{n^2R}{2L^2C_d}} \tag{3.81}$$

The parameters of the transfer function are given below :

L = 484.5μH ; R=31.75mΩ ; C_d = 1.527mF ; n = 1.005

In the implementation, phase angle (δ) between line-to-line STATCOM fundamental voltage and line-to-line AC grid voltage is adjusted by comparing the output of PI controller with a ramp which is sychronised to the zero crossing of 6.3kV line-to-line voltage. The output of PI controller is adjusted to a fixed value for the open loop simulations.

$$\delta = \frac{V_{open\_loop}}{10} \times \frac{\delta_{max}}{180} \tag{3.82}$$

where δ_{max} denotes the maximum phase angle (º) allowed by the control system and δ denotes the phase angle (rad) input of the open loop transfer function. Response time is measured from 0 to 100 % of the final value since the step response of STATCOM is optimised to have either critically damped or underdamped responses. Open loop model is as shown in Fig. 3.52.

Open loop response obtained from MATLAB simulations is given in Fig. 3.53. Open loop response time is found to be 100 ms. Open loop response time is calculated the same from full inductive mode to full capacitive mode and from full capacitive mode to full inductive mode.

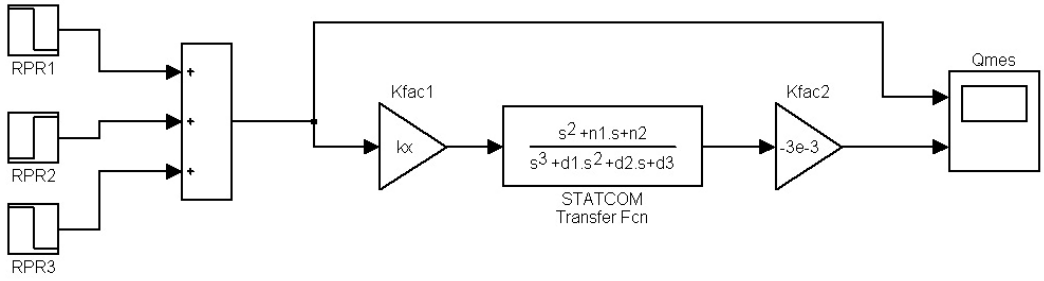


Figure 3.52 Open Loop Model of STATCOM (MATLAB)

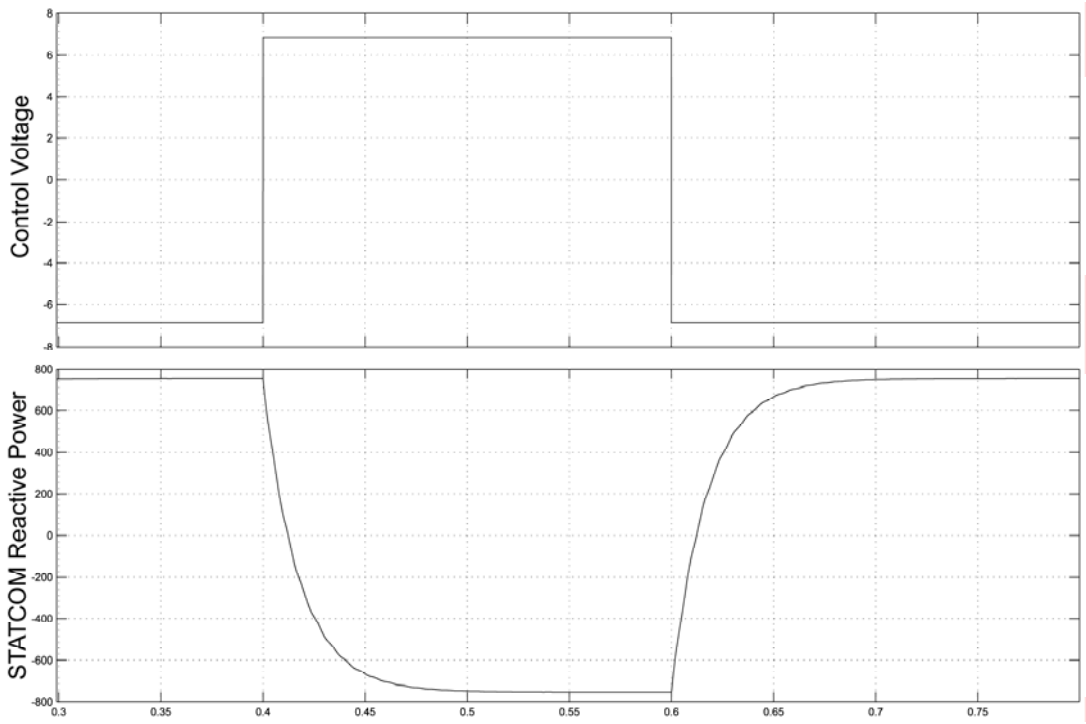


Figure 3.53 Open Loop Response of STATCOM (MATLAB)

Open loop response obtained from PSCAD simulations is given in Fig. 3.54. Open loop response time are found to be 118 ms from 750 kVAr inductive reactive power to 750 kVAr capacitive reactive power transition and 110 ms from 750 kVAr inductive reactive power to 750 kVAr capacitive reactive power transition.

Open loop model of MATLAB neglects the effect of filter capacitor on the transient response. PSCAD simulations are carried out for different filter capacitor values and it is verified that input filter capacitor has negligible effect on the transient response. On the other hand, PSCAD simulates all parts of the implemented system.

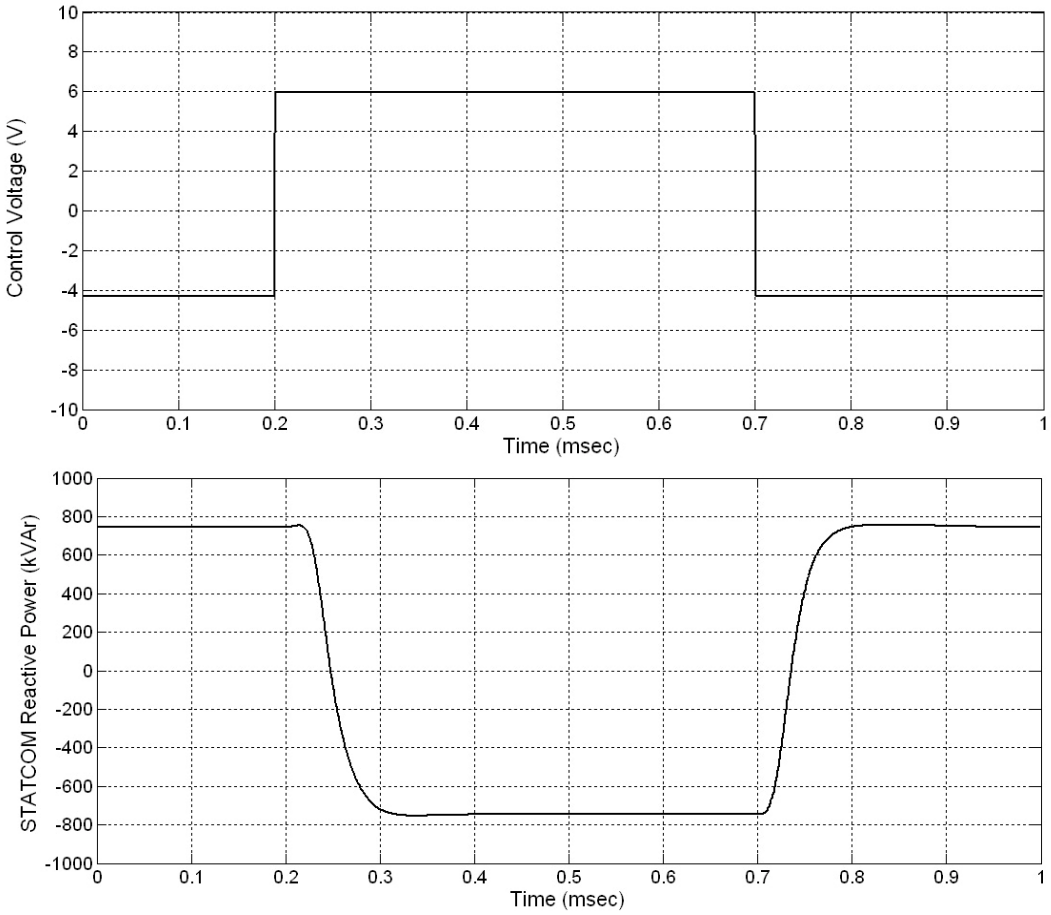


Figure 3.54 Open Loop Response of STATCOM (PSCAD)

PI controller can be modelled as in (3.83).

$$y(s) = \left(K_p + \frac{1}{K_I s} \right) e(s) \tag{3.83}$$

Where K_p represents the proportional gain and K_I represents the integral time constant. Closed loop model for MATLAB is given in Fig. 3.55.

In the MATLAB closed loop model, reactive power error is found by subtracting the output of STATCOM transfer function from the reference reactive power. Error is processed by the PI controller and output of PI controller is applied to the input of transfer function as the phase angle information. Reactive power is sampled at every 10 ms in order to model the reactive power measurement by Average Basis Concept. In addition to this, PI controller output is sampled at every 20ms to model the switching pattern update period (U_p) at every zero crossing of the line-to-line voltage. Switching pattern update period is effective on the optimisation of PI parameters. Integral time constant can be reduced for lower switching pattern update periods and faster responses can be obtained.

Closed loop response is given in Fig. 3.56 with K_p = 0.75 and K_I = 30 ms and U_p = 20 ms and in Fig. 3.57 with K_p = 0.85 and K_I = 20 ms and U_p = 5 ms.

Closed loop response time is calculated as 120 ms from Fig. 3.56 and 75 ms from Fig. 3.57. Therefore, switching pattern update period is important for a faster response. Closed loop response is found to be the same from full inductive mode to full capacitive mode and from full capacitive mode to full inductive mode.

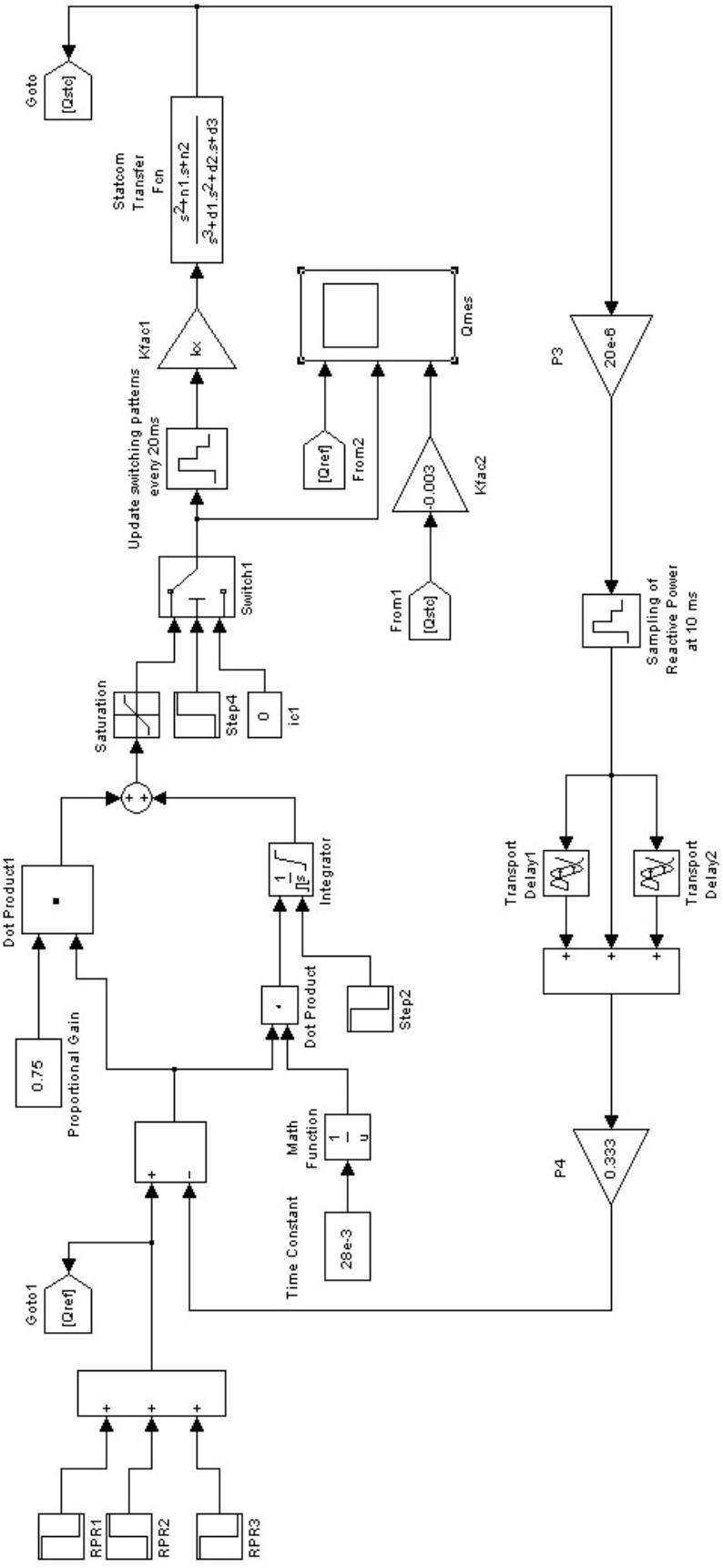


Figure 3.55 Closed Loop Model of STATCOM (MATLAB)

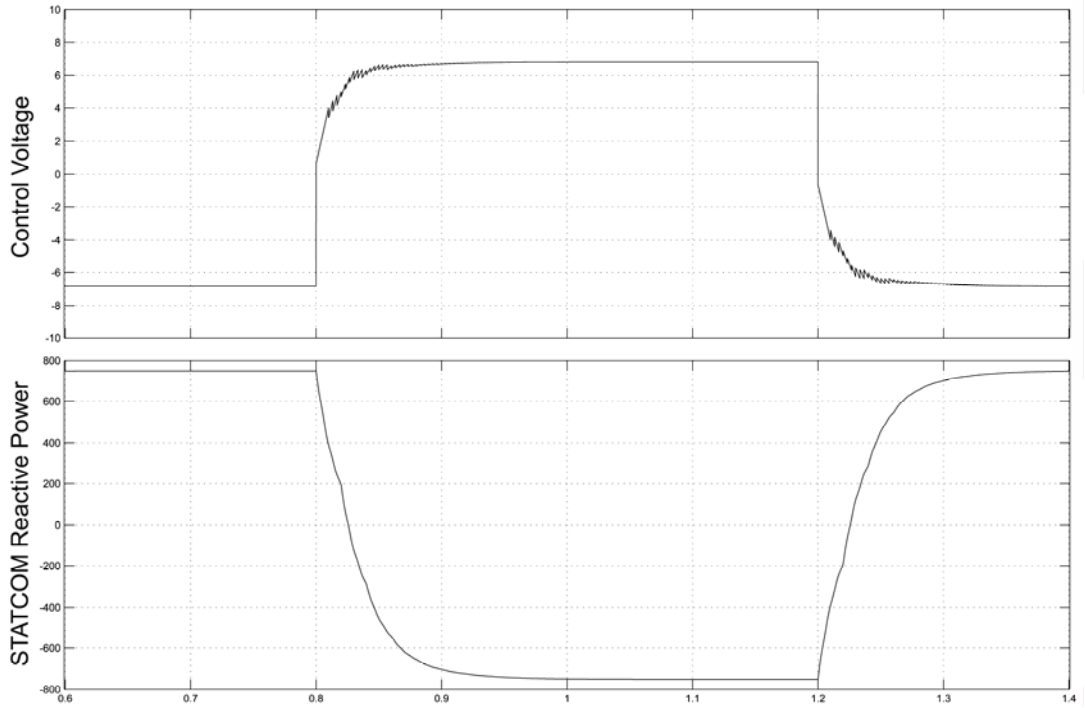


Figure 3.56 Closed Loop Response of STATCOM (MATLAB)
K_c=0.75; K_I = 30 ms; U_p=20 ms

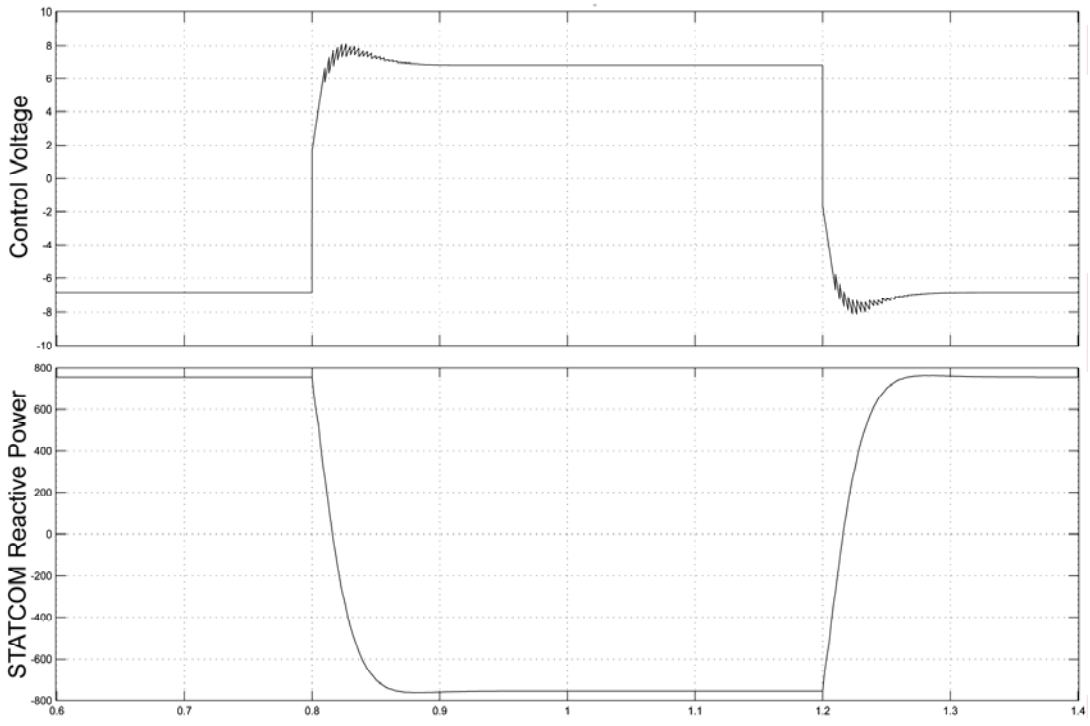


Figure 3.57 Closed Loop Response of STATCOM (MATLAB)
K_c=0.85; K_I=20ms; U_p=5ms

PSCAD simulations are also carried out for the analyses of the closed loop performance of STATCOM. It is observed that having different PI parameters according to the sign of reactive power error makes faster the closed loop response. Closed loop response is given in Fig. 3.58 for the following PI parameters.

$$Q_{err} \rangle 0 \Rightarrow \begin{pmatrix} K_c = 0.85 \\ K_I = 26\,\text{ms} \end{pmatrix} \text{ and } Q_{err} \langle 0 \Rightarrow \begin{pmatrix} K_c = 0.9 \\ K_I = 20\,\text{ms} \end{pmatrix}$$

Closed loop response is found as 140ms from full inductive mode to full capacitive mode and 150ms from full capacitive mode to full inductive mode. Therefore, proportional gain is kept constant during the operation of STATCOM both in capacitive and inductive modes of operation in the implementation and integral time constant is changed according to the sign of reactive power error (Q_{err}).

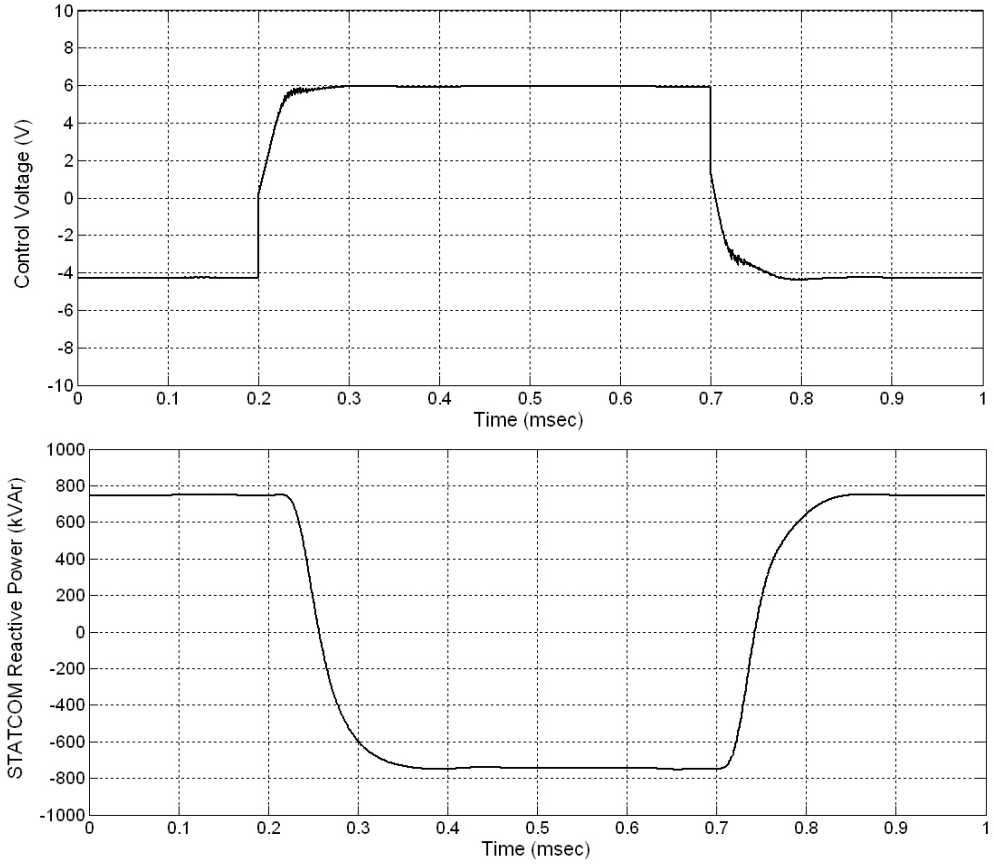


Figure 3.58 Closed Loop Response of STATCOM (PSCAD)

Block diagram of control system is given in in Fig. 3.59.

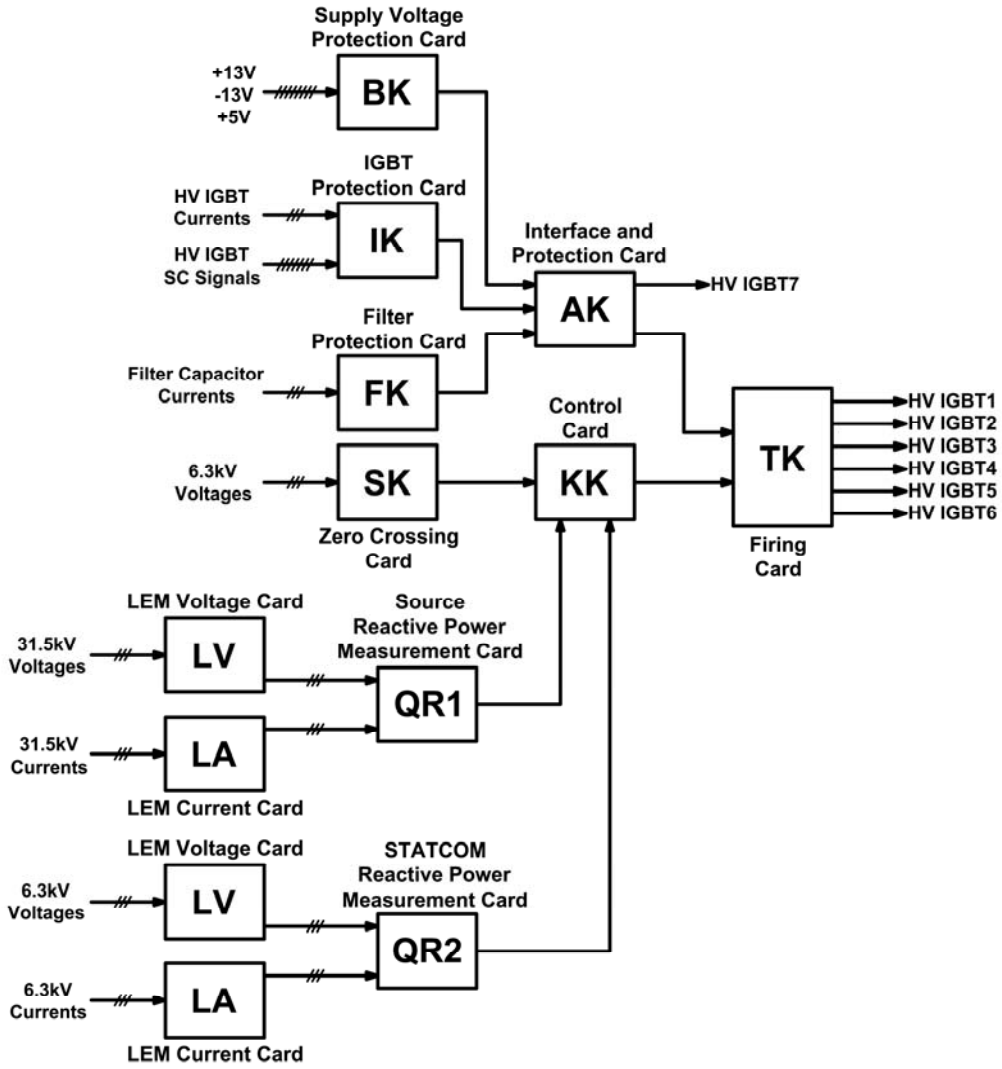


Figure 3.59 Block Diagram of Control System

Control system hardware is shown in Fig. 3.60.

Figure 3.60 Control System Hardware

3.7 Design of Protection System

VSC STATCOM utilizes HV IGBT modules in the power stage. HV IGBT modules presumably has no dv/dt and di/dt limitations. However, voltage and current rate of rise are in the order of 1.5kV/µs and 4kA/µs in the operating range of VSC based STATCOM. This necessitates the use of special protection circuits in order to prevent power semiconductor failures in the converter. The following protection circuits are designed for proper operation of VSC based D-STATCOM :

- Arm Short Protection in One-Leg
- Overcurrent Protection of HV IGBT Module
- Controlled Start of VSC (Precharging Circuit)
- Overvoltage/Undervoltage Protection of DC Link

3.7.1 Arm Short Protection in One-Leg

In 2 level, 3 leg voltage source converters, a short duration must be included between turn-off of one of the HV IGBT modules in one-leg and turn-on of the complementary HV IGBT module in the same leg to prevent short circuit in the DC link. This short duration is named as dead-time and defined in (3.84).

$$\text{dead time} = 1.5 \times (t_{d(off)} + t_f - t_{d(on)}) \quad (3.84)$$

$t_{d(off)}$ denotes turn-off delay time and $t_{d(on)}$ denotes turn-on delay time. These values depend on the gate resistors of the HV IGBT driver. t_f denotes the time passed during active clamping of the collector-emitter voltage if the driver has active-clamping feature. Therefore, dead time depends on the turn-on and turn-off resistor values of the driver and HV IGBT module characteristics.

Dead-time has a detrimental effect which occurs at every switching instant [43]. This effect can be examined by considering one leg shown in Fig. 3.61.

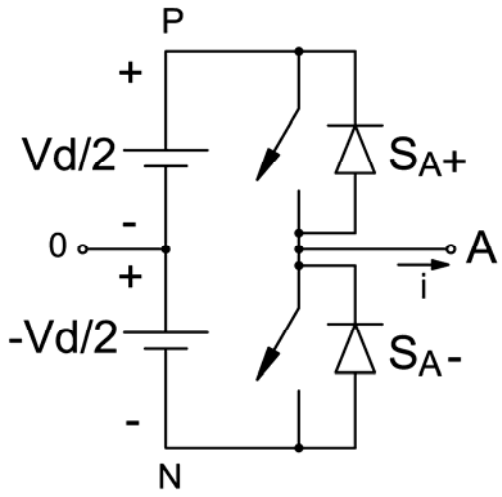


Figure 3.61 One-Leg

Effect of the dead time on the switching patterns for positive and negative load currents are shown in Fig. 3.62 [43].

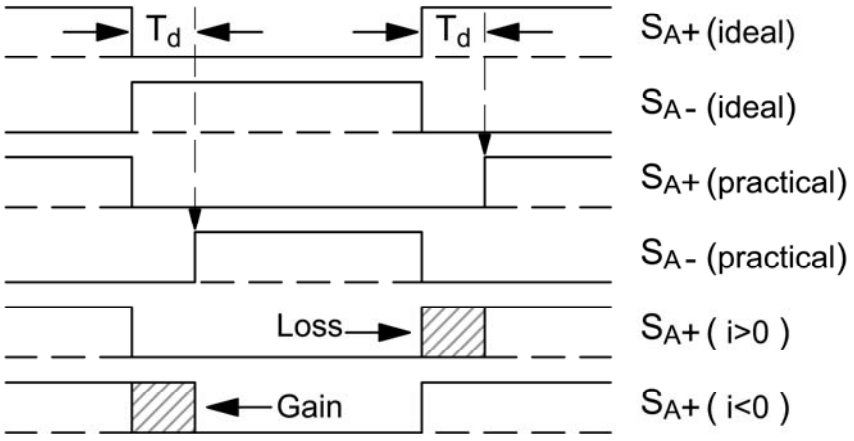


Figure 3.62 Ideal and Practical Switching Patterns for S_{A+} and S_{A-}

Practical waveforms including the effect of dead time are shown in Fig. 3.63 [43]. V_{A0} denotes the ideal line-to-neutral converter voltage and $V_{A0'}$ denotes the practical line-to-neutral converter. V_{err} is defined as

$$V_{err} = V_{A0} - V_{A0'} \tag{3.85}$$

It is seen that error voltage is rectangular since the width of all error pulses are equal to the dead time. Therefore, low-frequency odd voltage harmonics appear as a result of this rectangular voltage.

Average voltage deviation over a half cycle of the line-to-neutral converter voltage can be expressed as in (3.86) [43].

$$\Delta V = \frac{N T_d V_d}{T_s} \tag{3.86}$$

where N denotes the number of switching pulses in one period, T_d denotes dead time

and T_s denotes the fundamental period of the supply voltage.

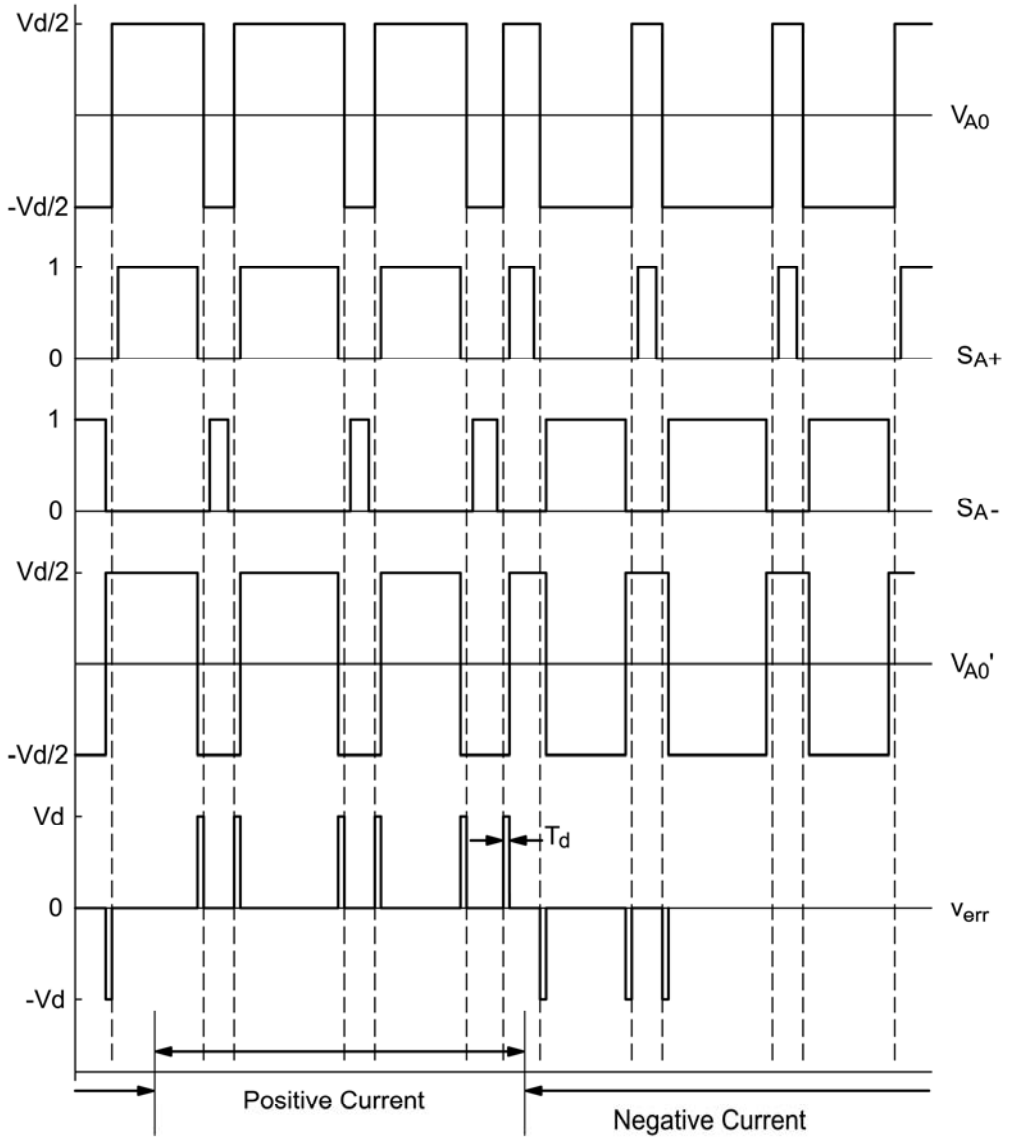


Figure 3.63 Practical Waveforms With Dead Time

As seen from Fig. 3.63, dead time causes line-to-neutral converter voltage to increase for negative load current and to decrease for positive load current. Therefore, average voltage deviation can be represented by a square wave and rms fundamental component of this square wave is expressed as in (3.87).

$$\Delta V_1 = \frac{2\sqrt{2}}{\pi}\Delta V \tag{3.87}$$

Let V_1^* be the ideal fundamental component of the line-to-neutral converter voltage with no dead time. Then we have to add ΔV_1 to V_1^* in order to find the resultant fundamental component. Phasor diagrams for the ideal and practical case are shown in Fig. 3.65 [43] :

I_1 represents inductive load current. It is seen from Fig. 3.64 that dead time changes both in magnitude and phase angle of the line-to-neutral converter voltage with respect to the ideal line-to-neutral converter voltage.

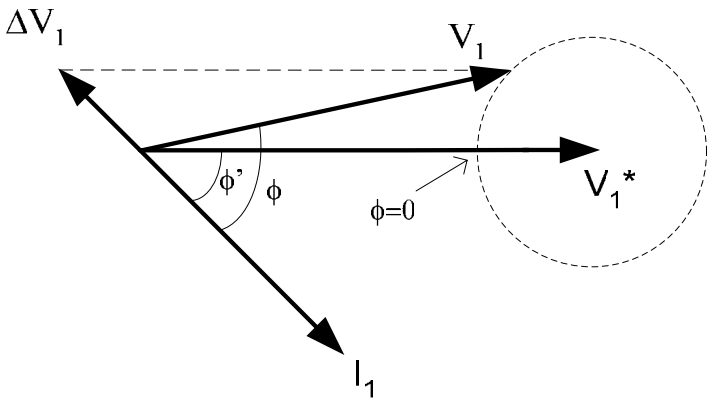


Figure 3.64 Phasor Diagrams Illustrating The Effect of Dead Time

Actual line-to-neutral converter voltage as a percentage of the ideal line-to-neutral converter voltage is obtained as below [43].

$$\frac{V_l}{V_l^*} = -\frac{\Delta V_l}{V_l^*} + \sqrt{(1 - \frac{\Delta V_l}{V_l^*}\sin^2\phi)} \tag{3.88}$$

$$\frac{\Delta V_l}{V_l^*} = \frac{8}{\pi}\frac{f_s T_d}{m_a} \tag{3.89}$$

where m_a denotes the modulation index of the switching pattern.

Hence, we can conclude that the effect of dead time on the magnitude of the line-to-neutral converter voltage depends on the dead time, modulation index and the switching frequency of the HV IGBT modules.

RMS voltage harmonics in the line-to-neutral converter voltage caused by the dead time can be found from the harmonic spectrum of square wave as given in (3.90).

$$(V_{A0})_n = \frac{2\sqrt{2}}{\pi}\frac{V_d T_d f_s}{n} \tag{3.90}$$

Phase angle controlled STATCOM controls both the magnitude and the phase of the converter voltages. Therefore, the error caused by dead time is compensated. However, dead time related harmonics must be considered especially at high switching frequencies.

Dead time control is implemented in the Firing Card (TK) shown in Fig. 3.65.

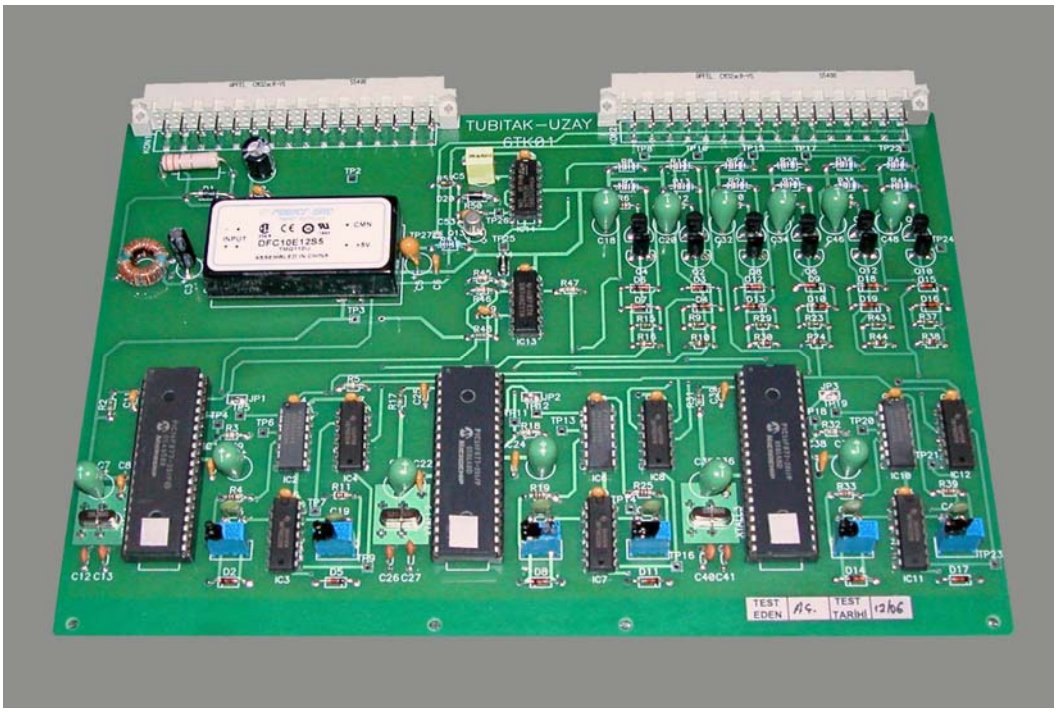


Figure 3.65 Firing Card

3.7.2 Overload Protection of HV IGBT Module

HV IGBT modules can be turned off at two times the rated current in saturation region without no limitations. However, this behaviour deviates in short circuit region. HV IGBT modules can withstand the short circuit currents specified in the Short Circuit Safe Operating Area (SCSOA) for 10μs. Short circuit currents can be accepted roughly as five times of the rated current for 3.3 kV HV IGBT modules. Nevertheless, HV IGBT modules can withstand short circuit currents totally 1000 times. Short circuit protection is already provided by the commercially available drivers.

A new overload protection circuit is designed for the HV IGBT module. Overload protection is available for commercial HV IPM IGBT modules [45]. Overload protection is performed by a current mirror circuit inside the module and the current limit is fixed by the HV IPM IGBT module manufacturer. However, overload protection is not included in any of the commercially available drivers.

HV IGBT module currents are sensed by the use of high bandwidth (Epcos N30 material, 5MHz bandwith) toroidal current transformers as shown in Fig. 3.66 and Fig. 3.67.

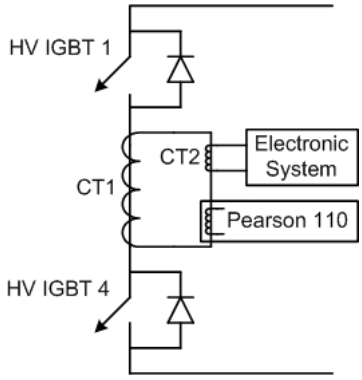


Figure 3.66 HV IGBT Module Current Sensing

Figure 3.67 CT1 and CT2 Current Transformers

As can be seen from Fig. 3.67, HV IGBT module has three parallel collector and emitter terminals. Current Transformer 1 (CT1) has a turn ratio of 1:20 and reduces 1200A collector current to 20A at the secondary of CT1. Secondary current of CT1 is used for measurement and for protection purposes. HV IGBT module currents are recorded by Pearson 110 current monitor which senses the secondary current of CT1.

For the overload protection of HV IGBT module, a second toroidal current transformer (CT2) with a ratio of 1:200 is used at the secondary of CT1 and 1200A HV IGBT module current is reduced to 100 mA for direct application to the input of the control system.

Secondary current of CT2 current transformer is processed by very high bandwith (AD8129, 200MHz) differential amplifiers and current limit is adjusted in the electronic circuitry. Resulting control system output is shown in Fig. 3.68 with HV IGBT module current waveform. Proper shielding must be used in order to obtain actual current signals without any distortion. The shielding is an important part of the current transformer design as can be understood from Fig. 3.67. Control system output with improper shielding is shown in Fig. 3.69.

Therefore, overload protection of HV IGBT modules is successfully implemented with special current transformers and electronic circuitry.

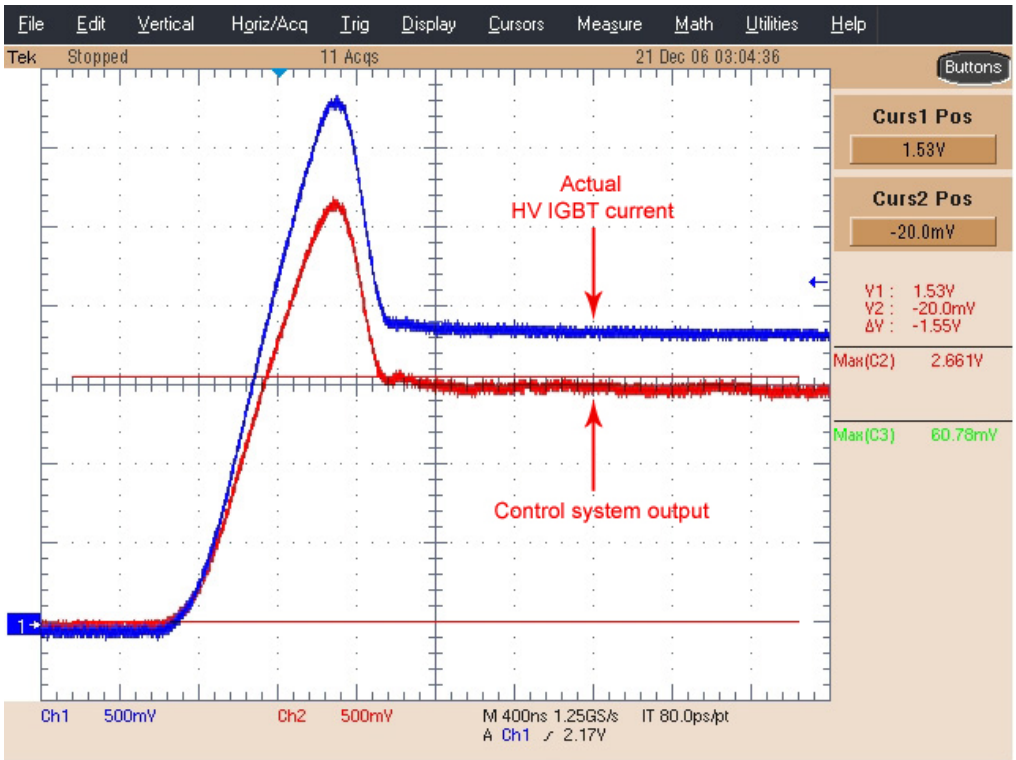


Figure 3.68 HV IGBT Module Turn-On Currents
Ch1 : HV IGBT Module Current ; Ch2 : Control System Output

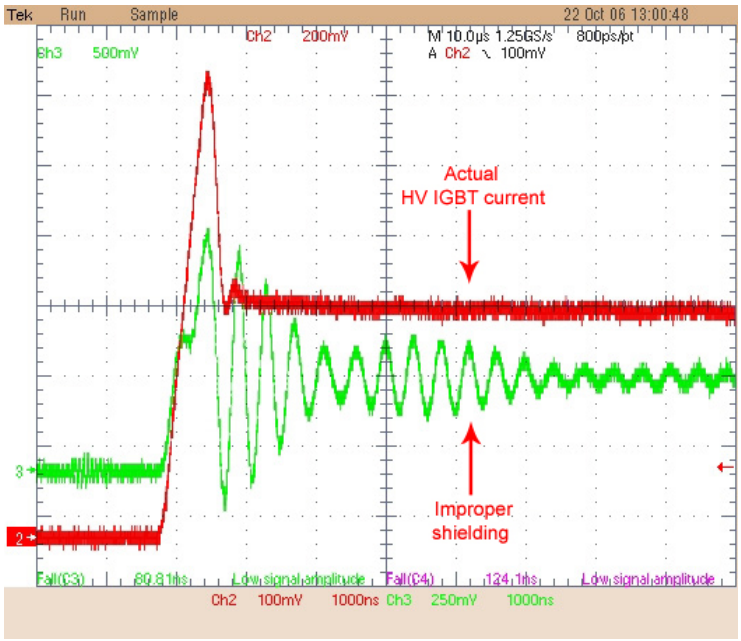


Figure 3.69 Control System Output with Improper Shielding
Ch1 : HV IGBT Module Current ; Ch2 : Control System Output

3.7.3 Controlled Start of VSC (Precharging Circuit)

DC link voltage of voltage source converters has to be charged prior to the STATCOM operation in order to prevent inrush currents in the DC link. Otherwise, FWDs of HV IGBT modules draw high inrush currents which is destructive for the converter. Alternative circuit topologies used for controlled charging of DC link voltage are shown in Fig. 3.70 where R_{pr} denotes charging resistor, R_{dr} denotes discharging resistor and R_d denotes the permanent dc link resistance in the converter.

Charging circuits shown in Fig. 3.70 (a) and (b) employ a three-phase diode bridge rectifier connected to the dc link of the converter through charging resistors, R_{pr}. Charging circuit in (a) uses resistors (R_{pr}) in the ac side to limit the charging current, charging circuit in (b) however, uses only one resistor (R_{pr}) in the dc side to limit the charging current. Charging circuit in (c) does not require a three-phase diode bridge rectifier and charging current is limited by the resistors (R_{pr}) in the ac side (R_{pr}). However, a second contactor (Cont2) bypassing the charging resistors (R_{pr}) is needed for this circuit.

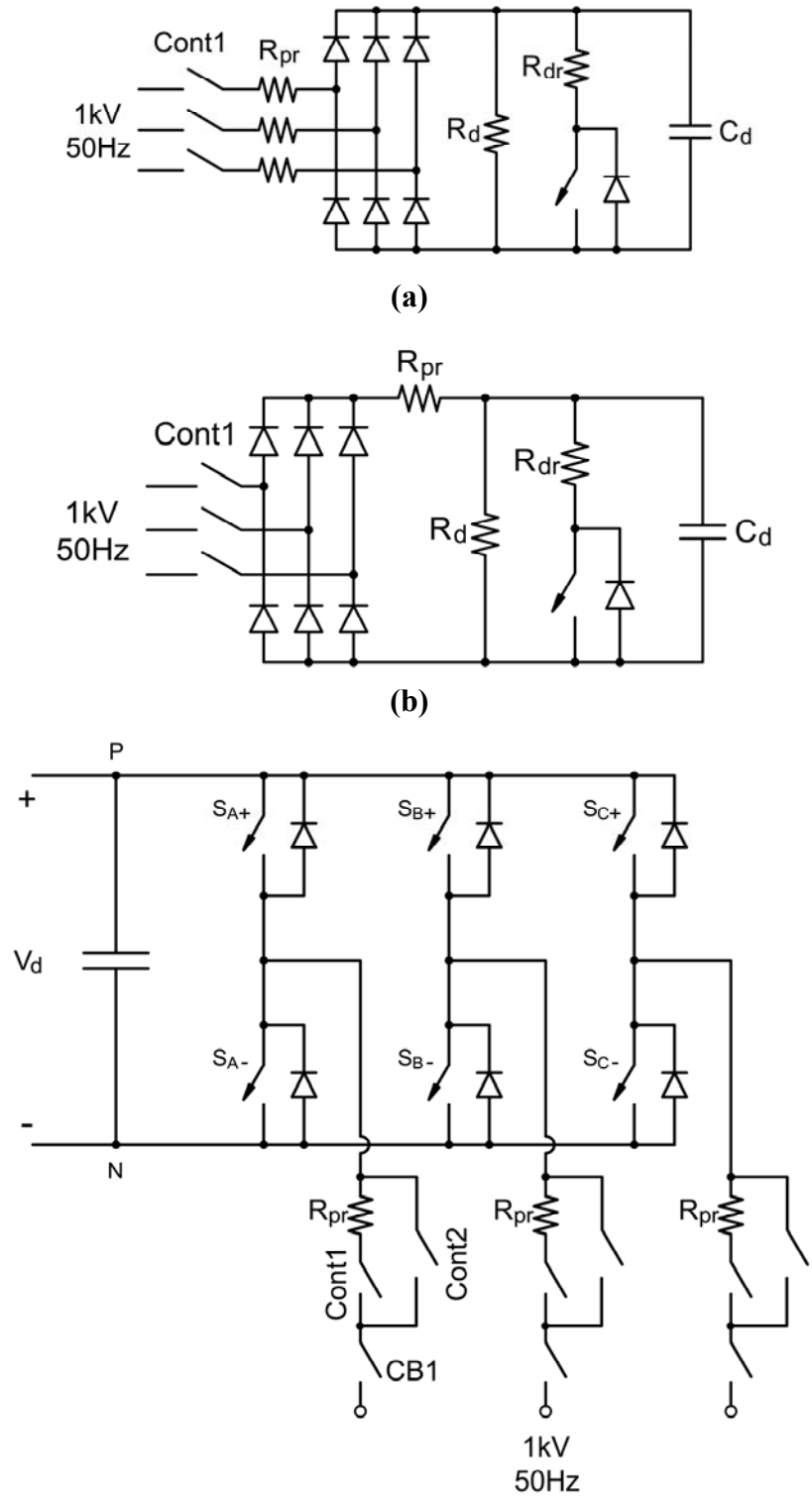


Figure 3.70 Alternatives of Charging and Discharging Circuits

Charging circuits in (a) and (b) do not need the bypass contactor and are preferred especially in low voltage applications. However, the use of a separate three-phase diode bridge rectifier is not practical in medium voltage applications, and charging circuit in (c) is preferrable for the converters connected directly to the medium voltage bus. In that case, the inherent FWDs present in the VSC are used for this purpose.

In this application, charging circuit in (b) is preferred in order not to use a second contactor for bypassing the charging resistors. Rapid discharge of the DC link is also performed by a HV IGBT module connected to the DC link through discharging resistors. Electrical specifications of the discharging and charging resistors are found to be the same and only one charging resistor is used in the DC side instead of three charging resistors in the AC side.

Implementation of the charging and discharging circuits are shown in Fig. 3.71.

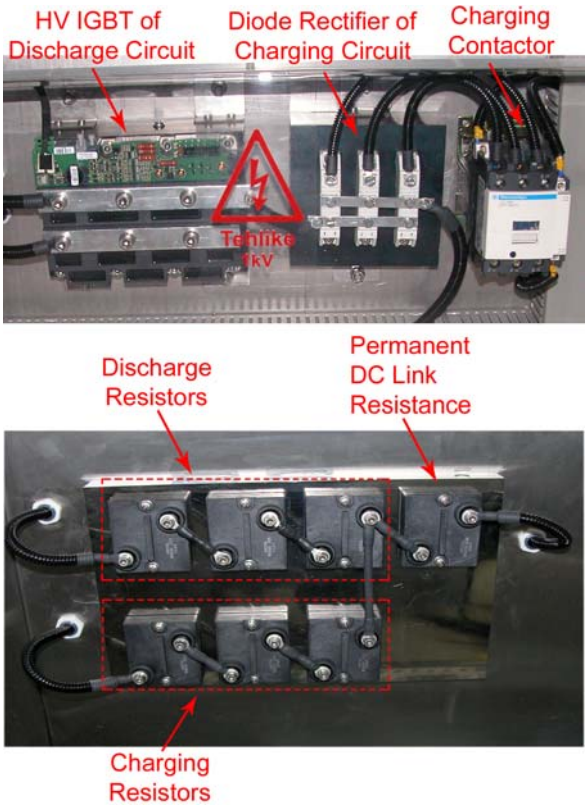


Figure 3.71 Implemented Charging and Discharging Circuit

3.7.4 Overvoltage/Undervoltage Protection of DC Link

As can be seen from Table 3.7, DC link voltage of VSC changes between 1157V and 1763V in the normal operation. However, DC link voltages can differ than the normal operating range in case of loss of control, higher voltage fluctuations in the supply voltage than permitted or in case of failure in the voltage and current sensors used at the end of voltage and current transformers of STATCOM system. Therefore, DC link voltage of VSC is measured by the control system and VSC is turned off if unexpected DC link voltages are measured. Normal operation and trip range of DC link voltage is shown in Fig. 3.72.

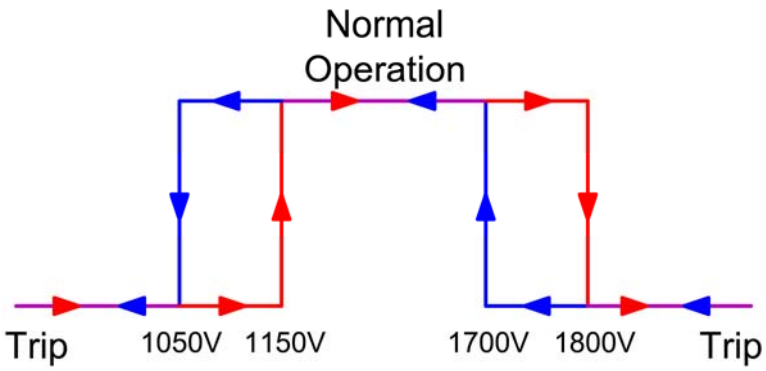


Figure 3.72 Normal Operation and Trip Range of DC Link Voltage

Following the turn-off process of VSC, the energy stored in the input filter inductance charges the DC link capacitor. Discharging resistor is inserted into the DC link by switching HV IGBT module immediately after turning off VSC (Fig. 3.71-b), and DC link voltage is discharged rapidly. Overvoltage and undervoltage protection are integrated into the Interface and Protection card (AK) shown in Fig. 3.73.

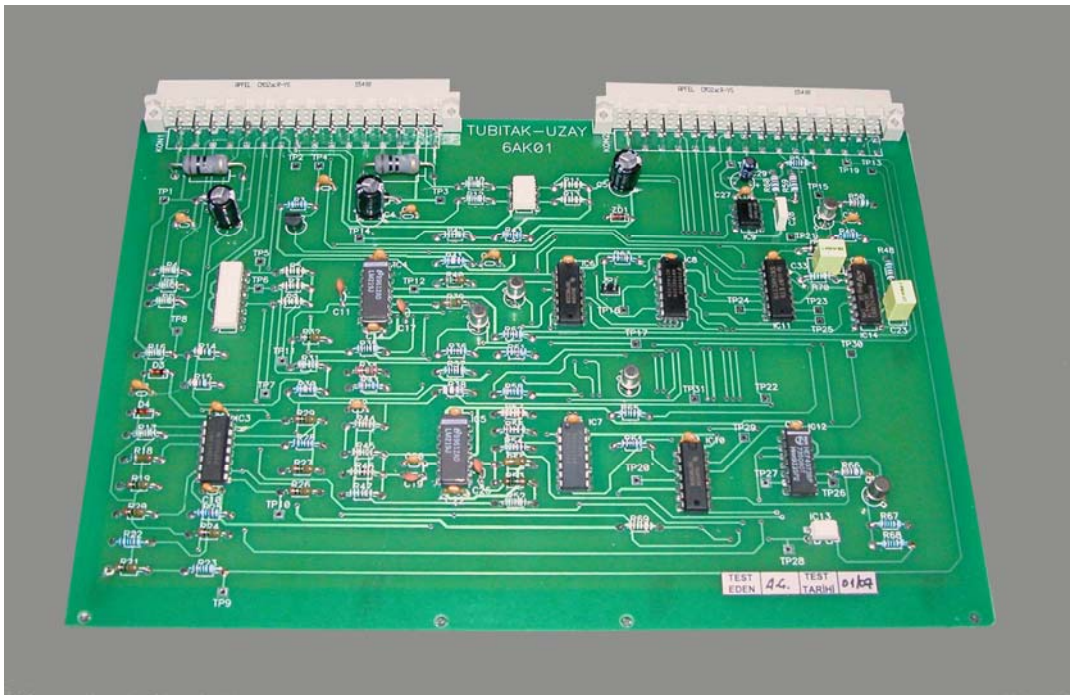


Figure 3.73 Interface and Protection Card

CHAPTER 4

FIELD TEST RESULTS

4.1 System Description

A ± 750kVAr VSC STATCOM is designed according to the specifications given in Chapter 3. The developed system is applied to Kemerköy Thermal Power Plant (KEAS) in order to provide reactive power compensation of coal conveyor belts. The complete circuit diagram of STATCOM system is shown in Fig. 3.15. The implemented system is shown in Fig. 4.1.

Figure 4.1 VSC D-STATCOM (On The Left)

The modulation technique of the VSC part is 8-Angle SHEM with the elimination of 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th} ,23^{rd} and 25^{th} voltage harmonics and thereby current harmonics at a fixed modulation index of 1.16.

Several records have been taken from the developed system in order to illustrate its performance. Measurement points are marked on the single line diagram of KEAŞ Coal Preparation System in Fig. 4.2.

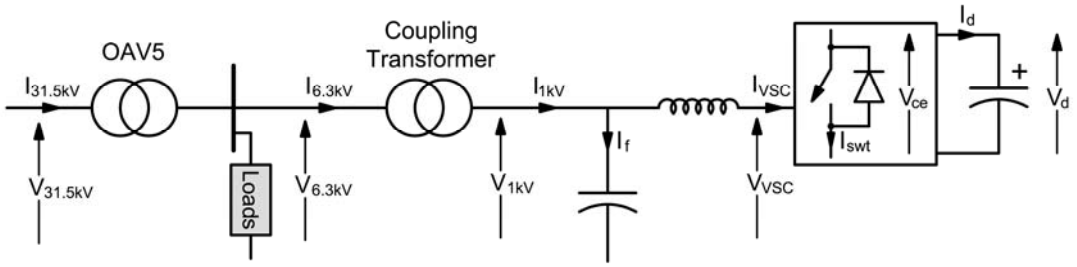


Figure 4.2 Measurement Points On the STATCOM System

The list of the measuring apparatus is given in Appendix C.

4.2 Field Results

Measurements are recorded for 1500 kVAr capacitive and zero reactive power generation of STATCOM at 6.3 kV. 1500 kVAr capacitive reactive power generation of STATCOM corresponds to 750 kVAr capacitive reactive power generation of VSC and zero reactive power generation of STATCOM corresponds to 750 kVAr inductive reactive power generation of VSC. 750 kVAr capacitive reactive power generation of VSC is described as capacitive operation mode and 750 kVAr inductive reactive power generation of VSC is described as inductive operation mode in the results.

Schematic diagram and implemented power stage of VSC are as shown in Fig. 4.3 and Fig. 4.4 respectively.

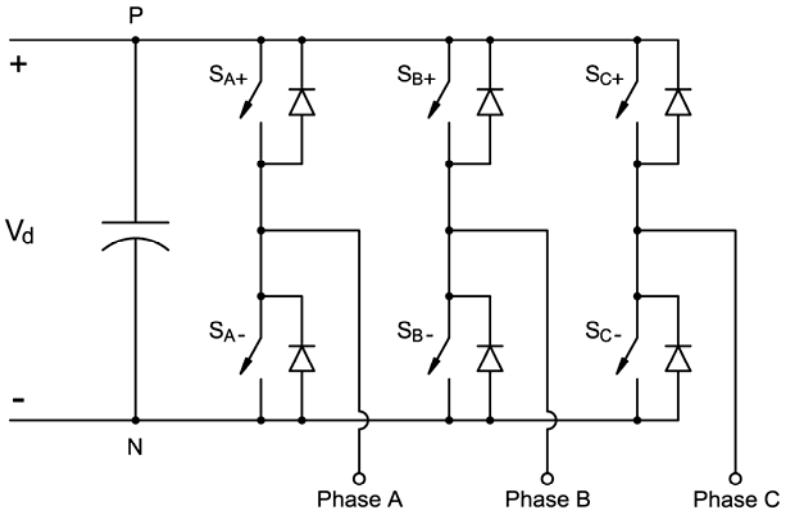


Figure 4.3 Schematic Diagram of VSC

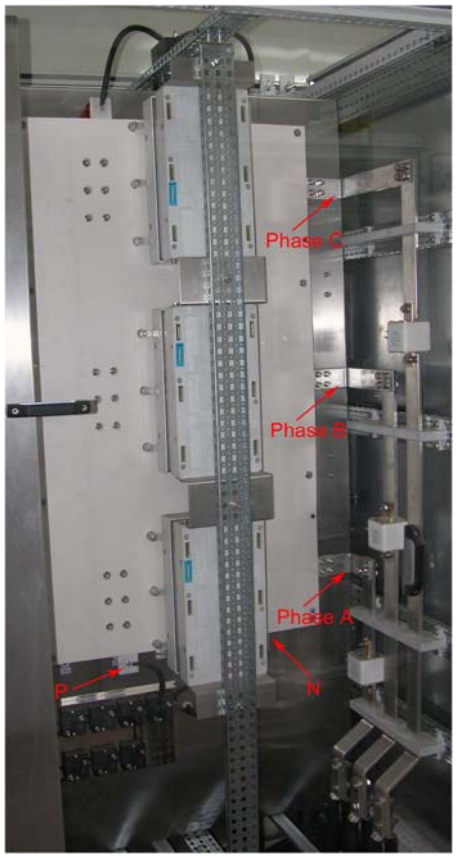


Figure 4.4 Implemented Power Stage of VSC

Collector-emitter voltage waveform of switch S_{A+} is recorded by Tektronix P5210 HV probe. Physical measurement points of HV IGBT voltage waveform (V_{ce}) is shown in Fig. 4.5.

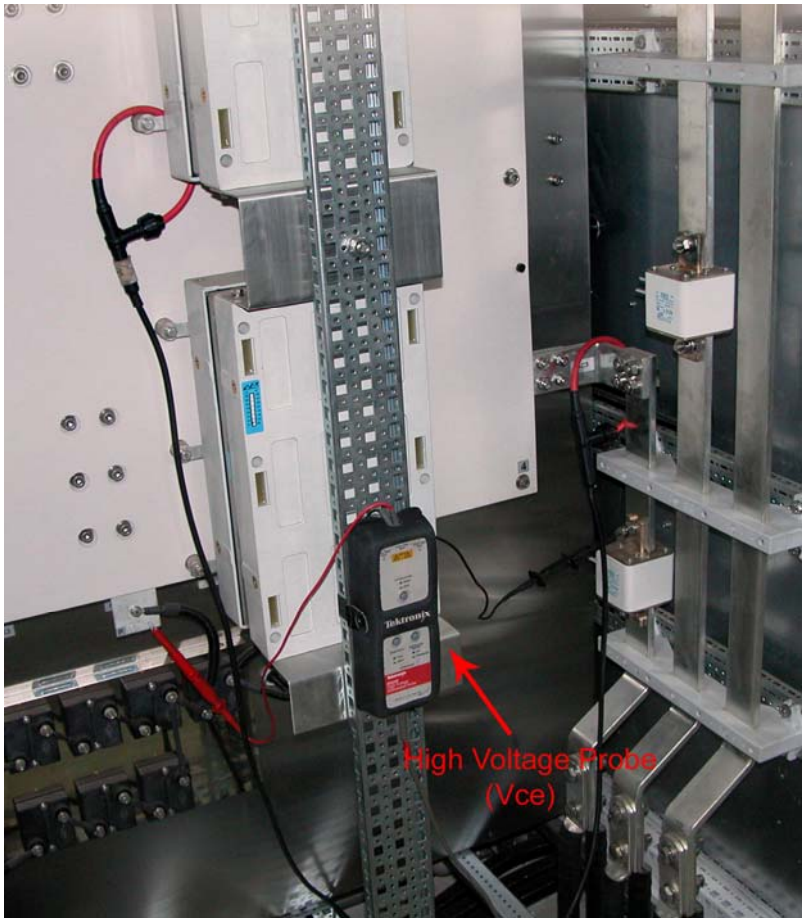


Figure 4.5 Measurement Points (V_{ce})

HV IGBT module current waveforms are recorded by Pearson current monitor 110. In HV IGBT module current measurements, Pearson current monitors are preferred instead of the Rogowski coils because of the delay (~ 40ns) introduced by Rogowski coils. Pearson current monitor measures the HV IGBT module current from the secondary of a toroidal ferrite transformer mounted on the terminals of HV IGBT module. Pearson current monitor is shown in Fig. 4.6 and toroidal ferrite transformer mounted on the HV IGBT module is shown in Fig. 4.7.

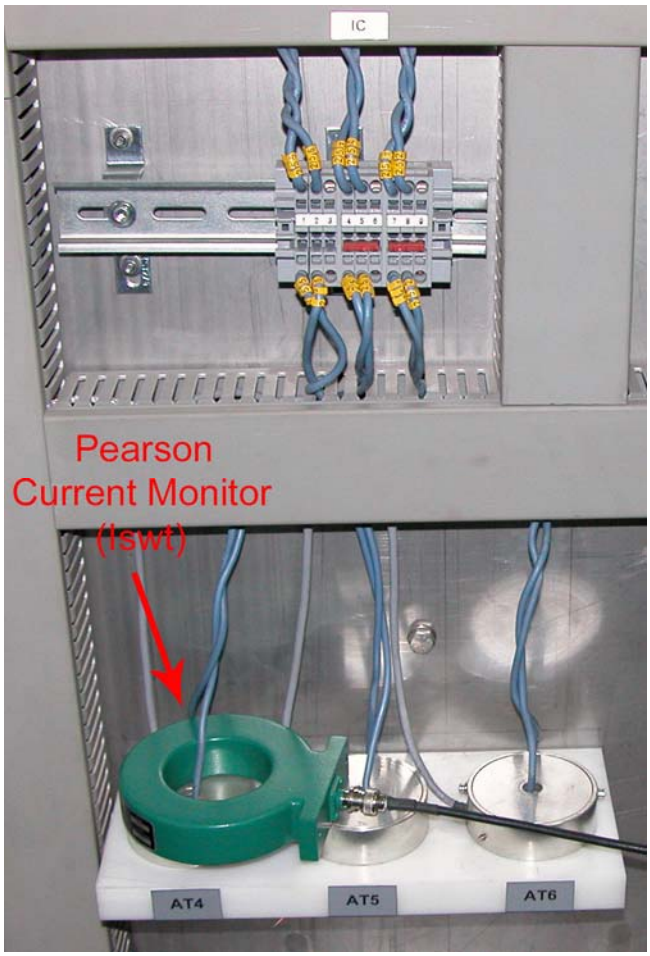


Figure 4.6 Measurement Points (I_{swt})

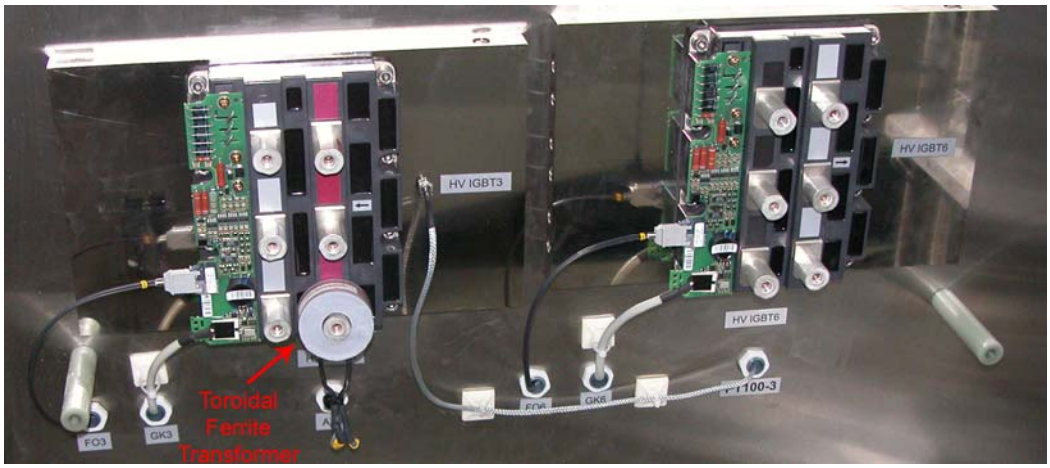


Figure 4.7 One-Leg Implementation of VSC

DC link voltage is recorded by Tektronix P5210 probe and DC link current is meausured by Rogowski coils from one of the terminals of DC link capacitor as shown in Fig. 4.8. Three parallel DC link capactitors are used in VSC, therefore, total DC link current is found by multiplying the measured current by 9 since each DC link capacitor has three terminals in parallel as seen from Fig. 4.4.

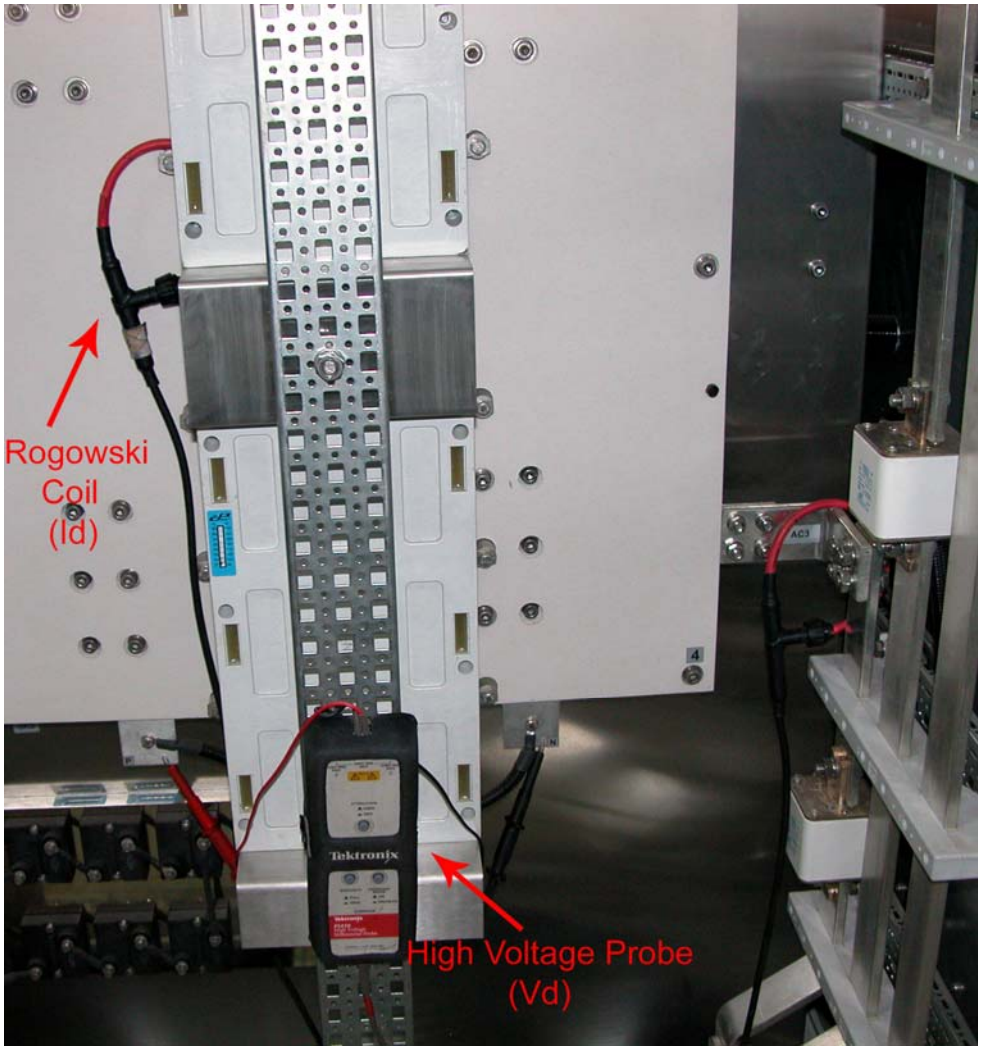


Figure 4.8 Measurement Points (V_d, I_d)

1kV line-to-line voltage and VSC voltage is recorded by Tektronix P5210 probe. 1kV line current and VSC current is meausured by Rogowski coils from the busbar connections of Distribution Panel (Fig. 4.9).

Input filter capacitor line current is meausured by Rogowski coils.

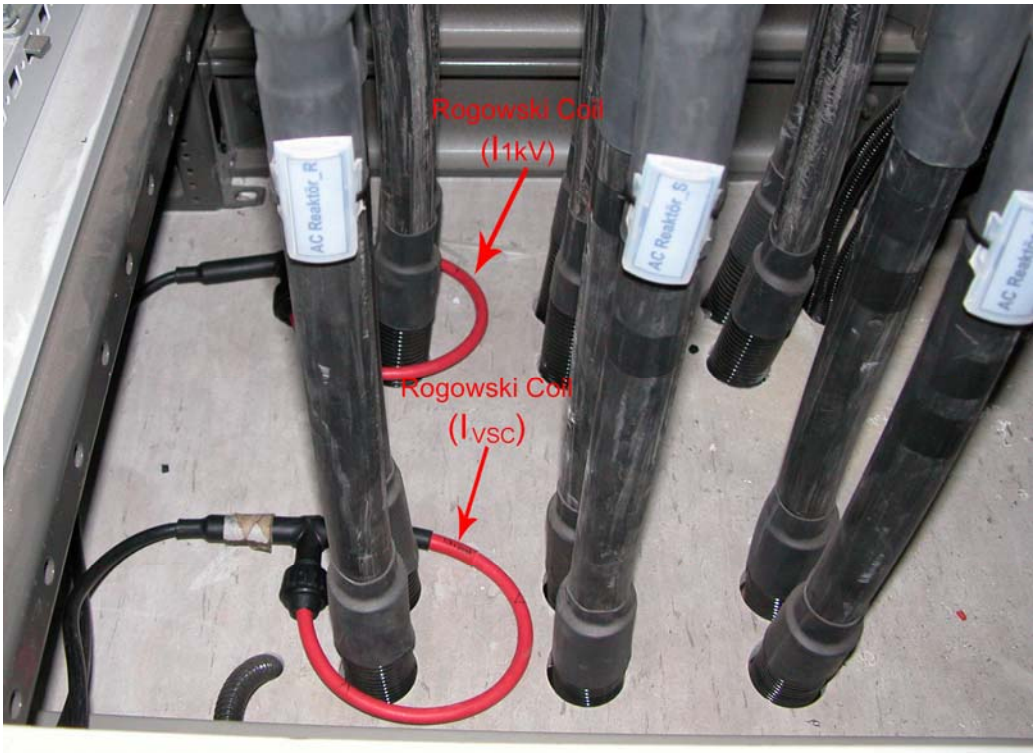
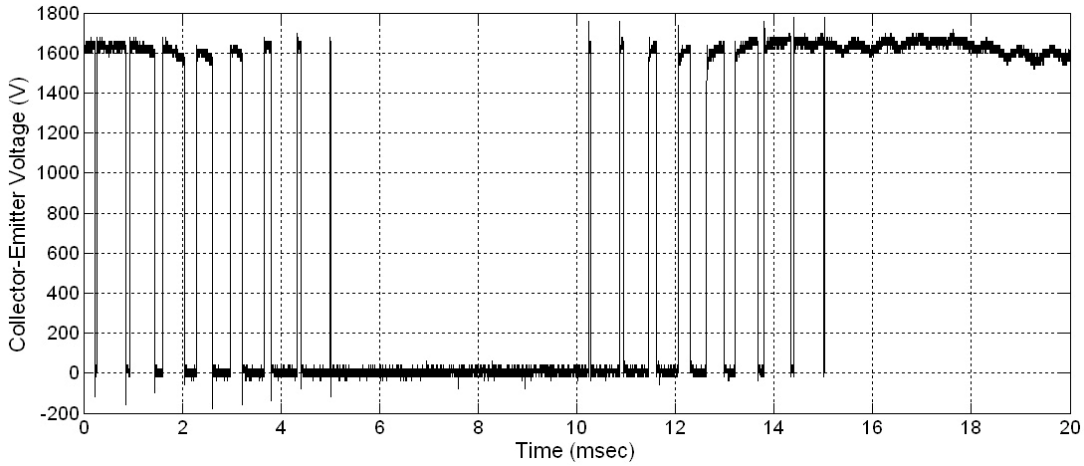


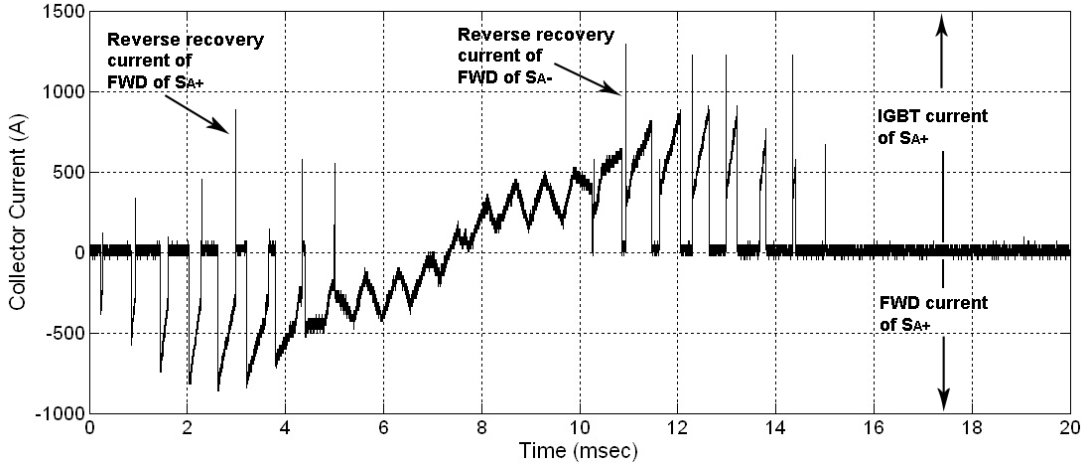
Figure 4.9 Measurement Points (I_{1kV} ,I_{VSC})

4.2.1 Voltage and Current Waveforms of Power Semiconductors (V_{ce} and I_{swt} in Fig. 4.2)

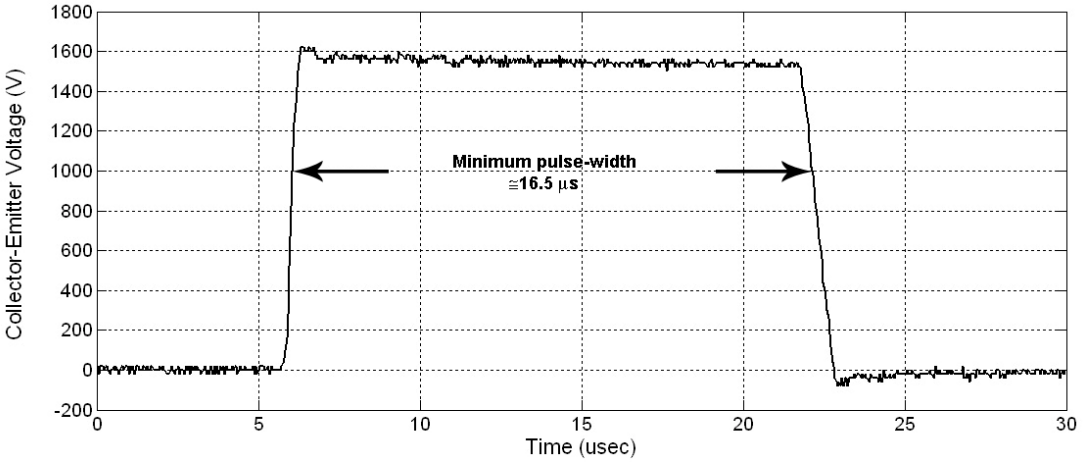
S_{A+} collector-emitter voltage and collector current waveform are shown in Fig. 4.10 for capacitive operation mode of STATCOM system. Gate-emitter and collector-emitter voltages of S_{C+} and S_{C-} during switching instant are shown in Fig. 4.11.



(a)



(b)



(c)

Figure 4.10 HV IGBT Module Waveforms in Capacitive Operation Mode
a : Collector-Emitter Voltage ; b: Collector Current ;
(c) : Minimum Pulse Width in Collector-Emitter Voltage

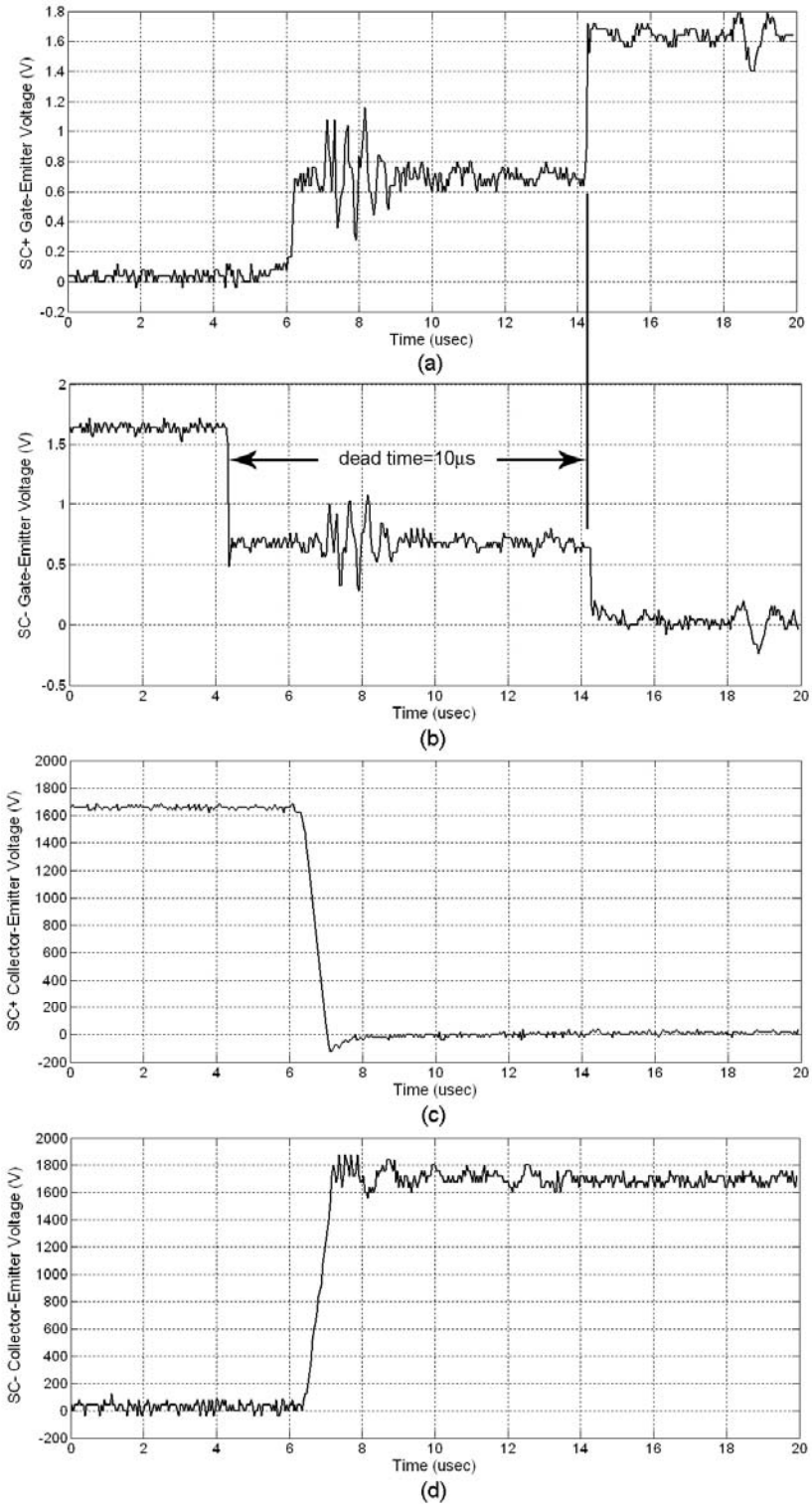


Figure 4.11 Gate Emitter and Collector-Emitter Voltages in One-Leg
(a) : S_{C+} Gate-Emitter Voltage ; (b) : S_{C-} Gate-Emitter Voltage
(c) : S_{C+} Collector-Emitter Voltage ; (d) : S_{C-} Collector-Emitter Voltage

When S_{C+} is turned off, FWD of S_{C+} becomes on immediately and dead time can not be observed from collector-emitter voltages. Therefore, gate-emitter voltages are also recorded with collector-emitter voltages to measure the dead time between switching patterns of S_{C+} and S_{C-}. Dead time is found to be 10μs as shown in Fig. 4.11.

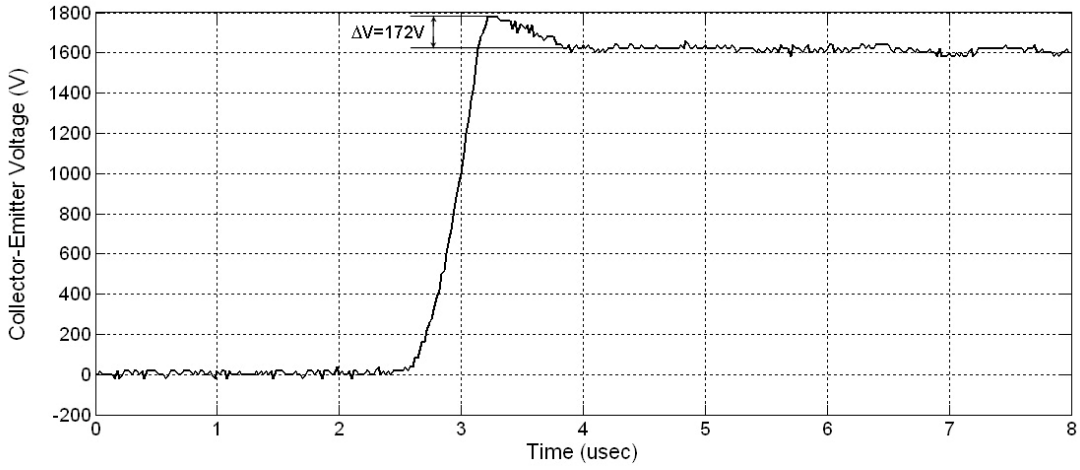
Turn-off switching waveforms of the HV IGBT module in capacitive operation mode are given in Fig. 4.12.

Turn-on switching waveforms of the HV IGBT module in capacitive operation mode are given in Fig. 4.13.

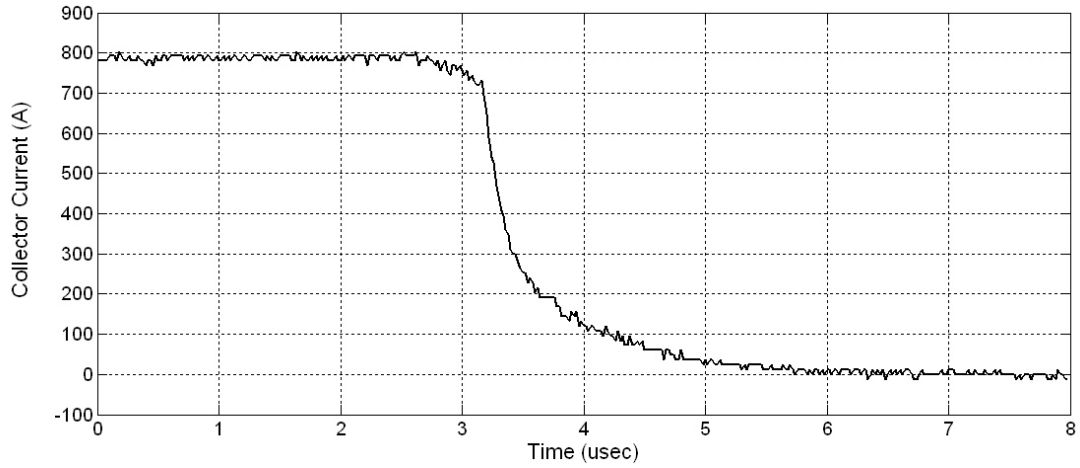
It is seen from turn-off collector-emitter voltage waveform that the peak collector-emitter voltage is 1780 V and DC link voltage is 1608 V DC. Maximum switched collector current is 800 A and maximum collector current is 1175 A as a result of the reverse recovery current of the S_{A-} FWD.

Collector-emitter voltage has 172 V overshoot as a result of turn-off process. In the laboratory tests, 250 V overshoot is recorded for a collector current of 1200 A. Therefore, 167 V overshoot is expected for a collector current of 800 A assuming di/dt is the same both for 800 A and 1200 A. The collector current waveform illustrating turn-on di/dt = 3.3 kA/μs has already been given in Fig. 3.35. in Chapter 3. This result also validates the effective dc link inductance found in the labaratory tests.

Negative overshoot at the collector-emitter voltage waveform occur because of the inductance between the measurement points shown in Fig. 4.5 and collector-emitter terminals of the HV IGBT Module.

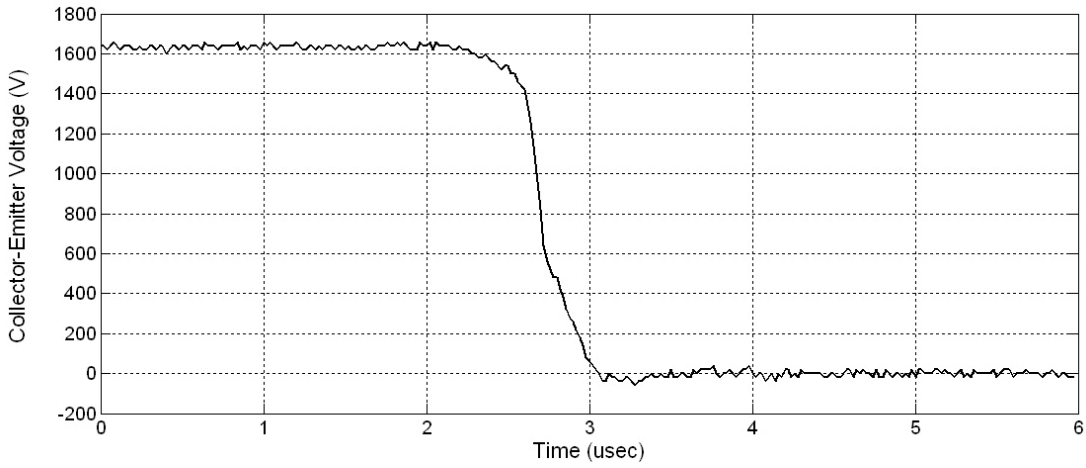


(a)

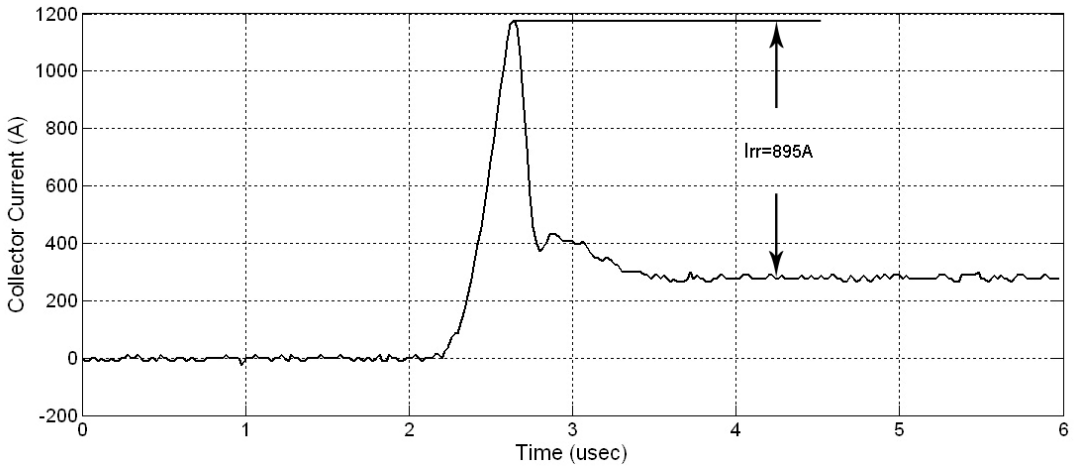


(b)

Figure 4.12 HV IGBT Module Turn-Off Switching Waveforms in Capacitive Operation Mode
a : Collector-Emitter Voltage ; b: Collector Current ;



(a)



(b)

Figure 4.13 HV IGBT Module Turn-On Switching Waveforms in Capacitive Operation Mode
a : Collector-Emitter Voltage ; b: Collector Current ;

Collector-emitter voltage with minimum pulse width is shown in Fig. 4.10. Minimum pulse width is set to 26.5 μs by the switching pattern. However, 10 μs dead time reduces the minimum pulse width to 16.5 μs as seen from Fig. 4.10. All other pulses in the switching pattern have longer pulse widths and Minimum Pulse Width constraint is satisfied in the implementation.

HV IGBT module is working safely if RBSOA, RRSOA, V_{LTDS} value and minimum pulse width constraint is satisfied. Therefore, maximum DC link voltage must be lower than 2100 V, maximum peak collector-emitter voltage must be lower than 2400 V (driver's limitation), maximum collector current must be lower than 2400 A and minimum pulse width must be larger than 16.5 μs. Hence, HV IGBT module is working safely in capacitive operation mode.

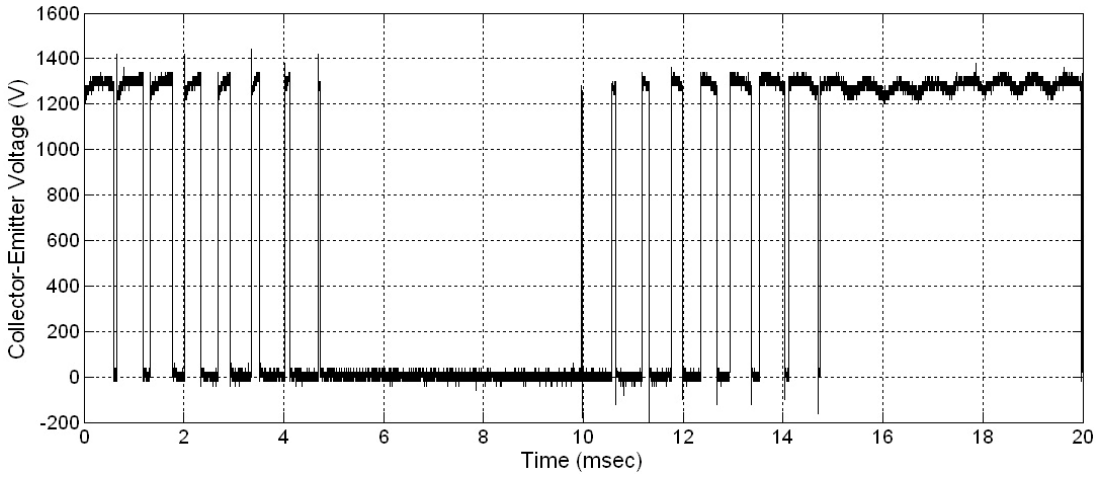
S_{A+} collector-emitter voltage and collector current waveform are shown in Fig. 4.14 for inductive operation mode.

Turn-off switching waveforms of the HV IGBT module in inductive operation mode are given in Fig. 4.15.

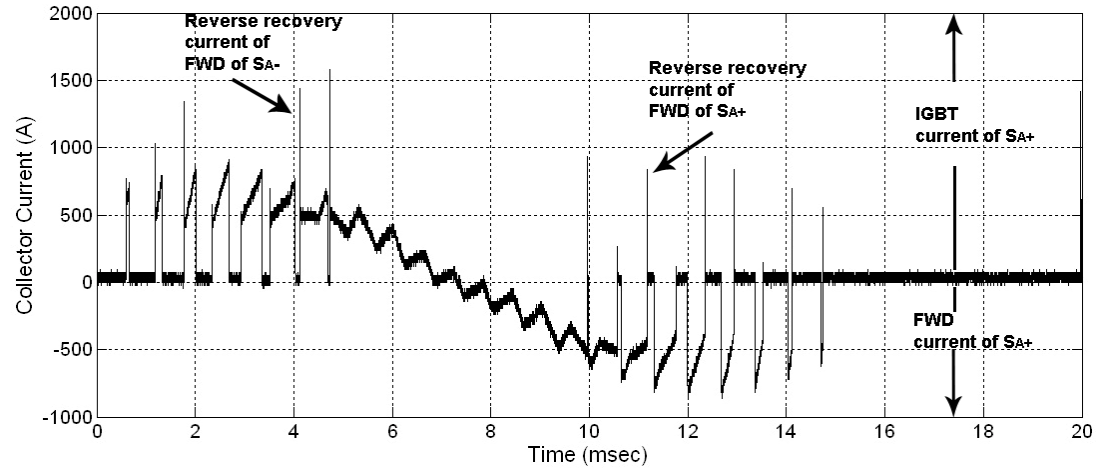
Turn-on switching waveforms of the HV IGBT module in inductive operation mode are given in Fig. 4.16.

It is seen from turn-off collector-emitter voltage waveform that the peak collector-emitter voltage is 1480 V and DC link voltage is 1289 V DC. Maximum switched collector current is 850 A and maximum collector current is 1400 A as a result of the reverse recovery current of the S_{A-} FWD.

Collector-emitter voltage has 191 V overshoot as a result of turn-off process. In the laboratory tests, 250 V overshoot is recorded for a collector current of 1200 A. Therefore, 177 V overshoot is expected for a current of 850 A by assuming di/dt is the same both for 850 A and 1200 A. Therefore, effective dc link inductance found in the labaratory tests is also verified in inductive mode of operation.

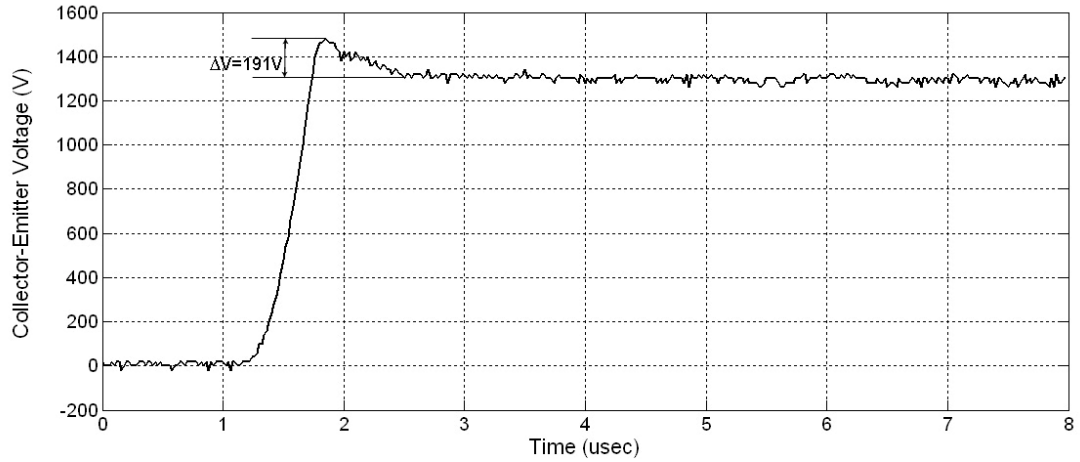


(a)

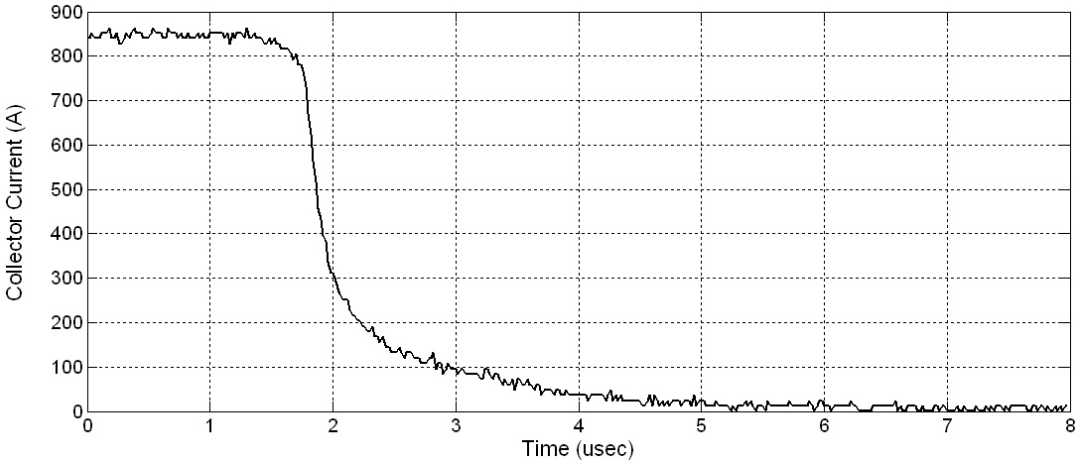


(b)

Figure 4.14 HV IGBT Module Waveforms in Inductive Operation Mode a : Collector-Emitter Voltage ; b: Collector Current

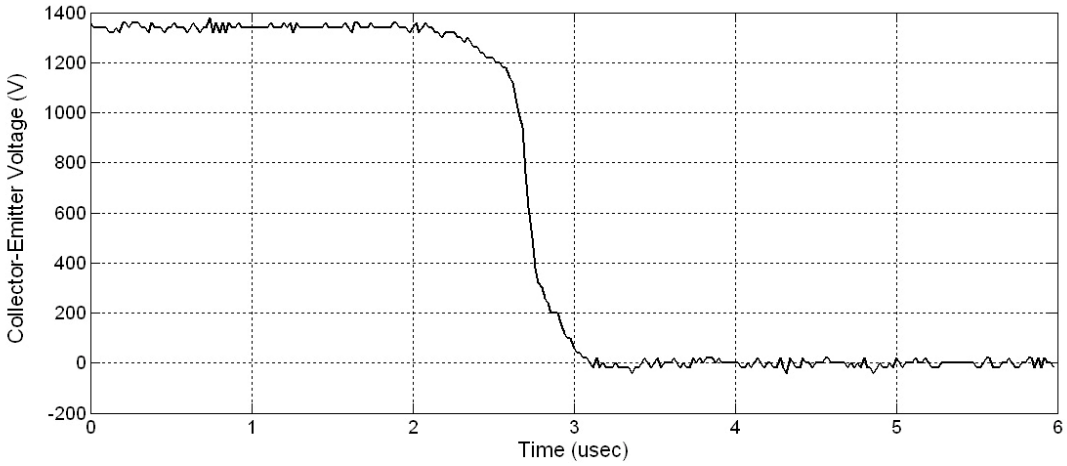


(a)

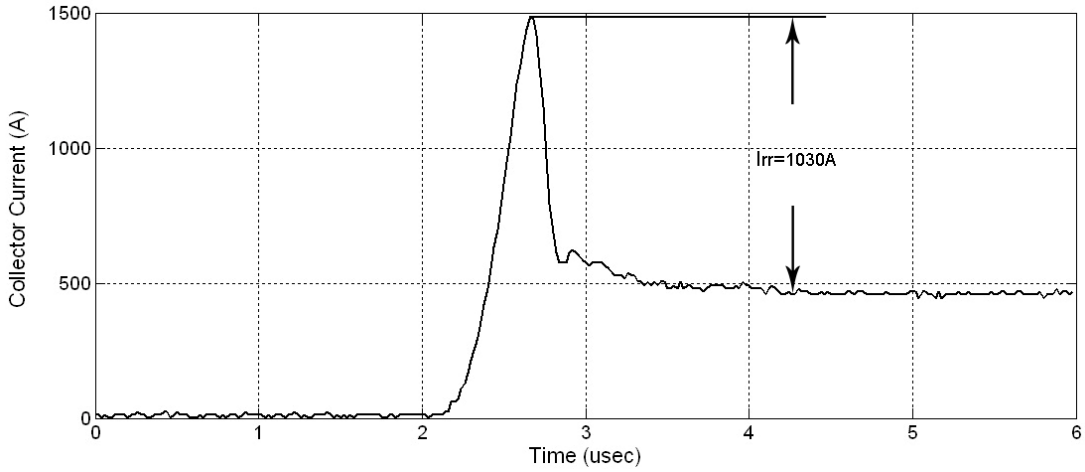


(b)

Figure 4.15 HV IGBT Module Turn-Off Switching Waveforms in Inductive Operation Mode
a : Collector-Emitter Voltage ; b: Collector Current



(a)



(b)

Figure 4.16 HV IGBT Module Turn-On Switching Waveforms in Inductive Operation Mode
a : Collector-Emitter Voltage ; b: Collector Current

The positive part of collector current shows the conduction periods of IGBT part and negative part of collector current shows the conduction periods of FWD. It is seen that on periods of IGBT and FWD changes with respect to switching pattern in capacitive and induction operation modes.

It is concluded that HV IGBT module is working safely also in the inductive operation mode.

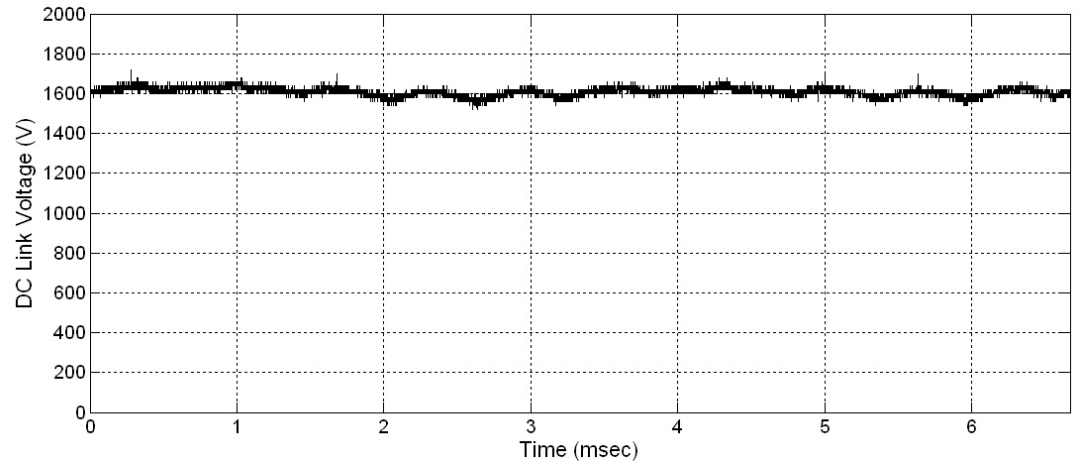
4.2.2 DC Link Voltage and Current Waveforms (V_d and I_d in Fig. 4.2)

DC link voltage, DC link ripple voltage and DC link current are given in Fig. 4.17 for capacitive operation mode and in Fig. 4.18 for inductive operation mode.

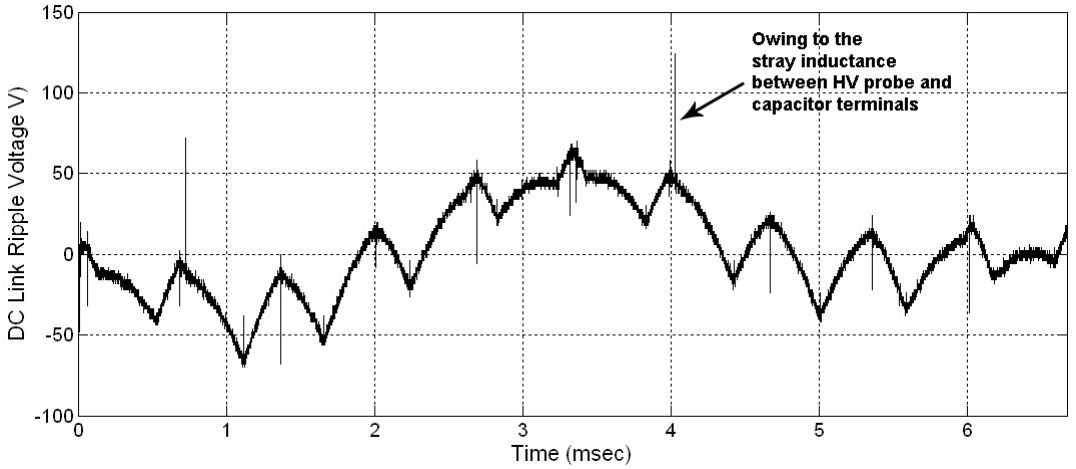
DC link voltage is 1608 V DC for 1500kVAr reactive power generation and 1289 V DC for zero reactive power generation. Calculated values are 1615 V DC and 1302 V DC as given in Table 3.7. Therefore, calculated and measured DC link voltages are very close to each other.

Percentage DC link ripple voltage is found as 8 % for 1500 kVAr reactive power generation and 6 % for zero reactive power generation. This value is larger than the theoretical values found by MATLAB and PSCAD simulations. DC link ripple voltage can be decreased by using capacitors with higher values at the expense of worse open loop response and thereby closed loop response. Voltage overshoots seen on the DC link ripple voltage waveforms occur because of the inductance between the measurement points shown in Fig. 4.8 (P and N) and terminals of the DC link capacitor.

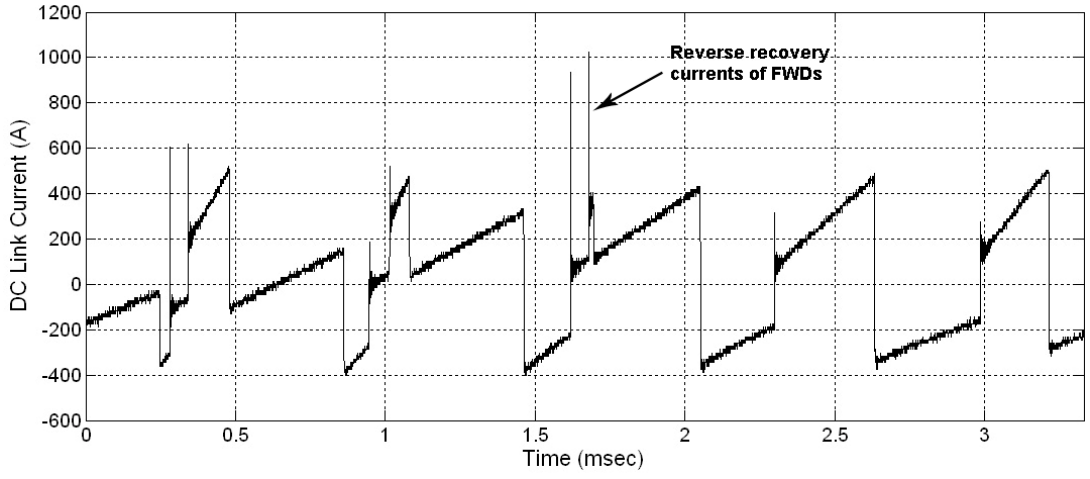
Reverse recovery current of HV IGBT modules are supplied by the DC link capacitors. These are seen as positive current overhoots in Fig. 4.17 and Fig. 4.18.



(a)

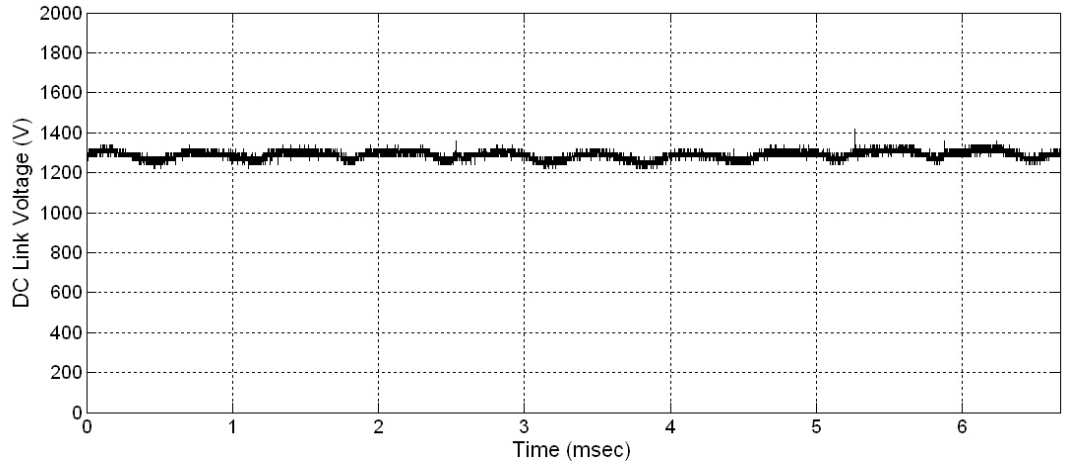


(b)

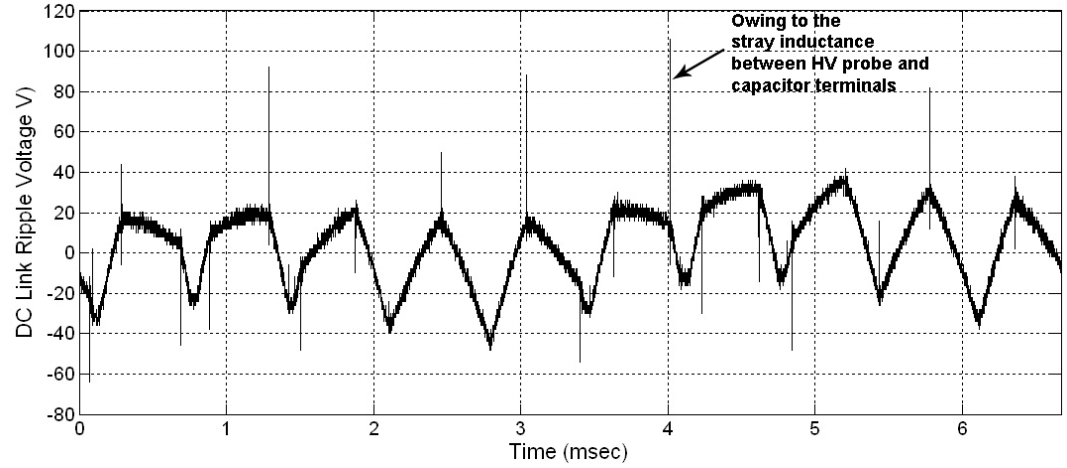


(c)

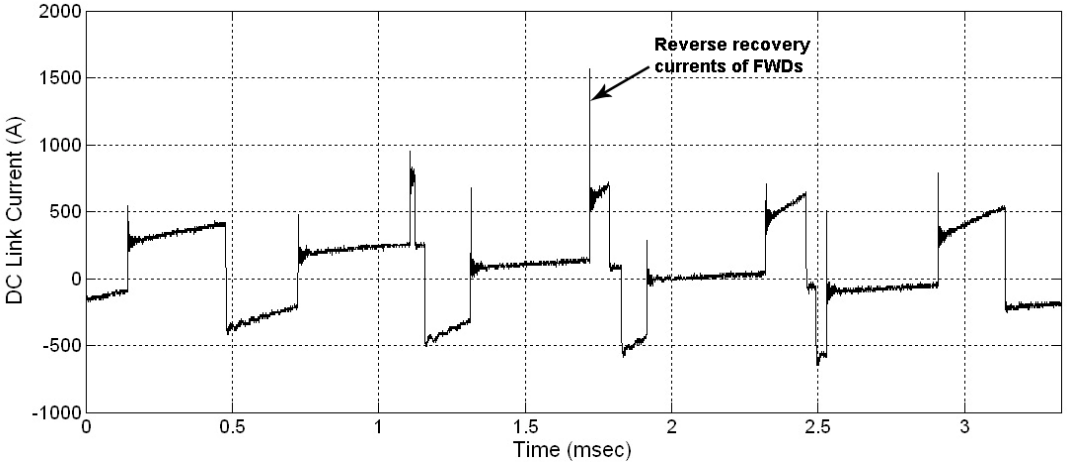
Figure 4.17 DC Link Voltage and Current Waveforms in Capacitive Operation Mode
a : DC Link Voltage ; b: DC Link Ripple Voltage c : DC Link Current



(a)



(b)



(c)

Figure 4.18 DC Link Voltage and Current Waveforms
in Inductive Operation Mode
a : DC Link Voltage ; b: DC Link Ripple Voltage ; c : DC Link Current

4.2.3 VSC Voltage and Current Waveforms (V_{VSC} and I_{VSC} in Fig 4.2)

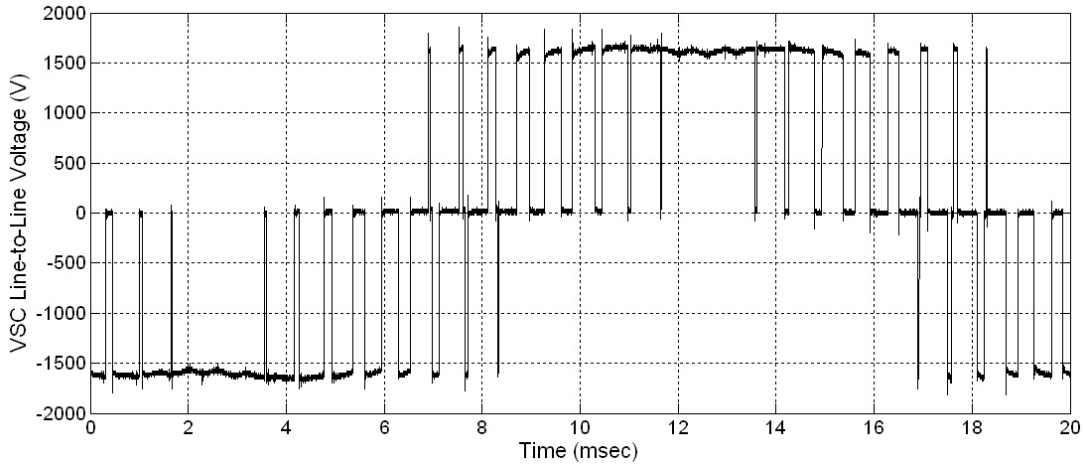
VSC line-to-line voltage and line current waveforms are given in Fig. 4.19 for capacitive operation mode and and in Fig. 4.20 for inductive operation mode.

Variation of the fundamental component of VSC line-to-line voltage in capacitive and inductive operation modes is seen from Fig. 4.19 and Fig. 4.20. Fundamental component of VSC line-to-line voltage is controlled by changing the DC link voltage.

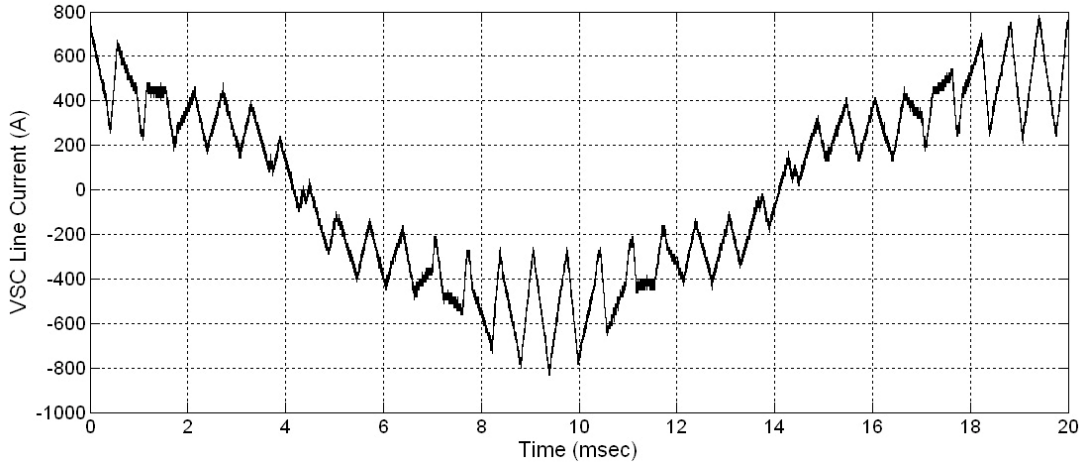
DC link voltage is reduced in inductive operation mode. Therefore, VSC voltage harmonics and thereby VSC current harmonics are lower for inductive operation mode.

Harmonic spectrum of VSC line-to-line voltage in capacitive and inductive operation modes are given in Fig. 4.21.

Modulation index is kept constant by 8-Angle SHEM technique. Hence, VSC line-to-line voltage harmonics as a percentage of the line-to-line fundamental voltage are same irrespective of the DC link voltage and we expect the same VSC voltage harmonic spectrum both in capacitive and inductive operation modes. This is apparent in Fig. 4.21. VSC line-to-line voltage harmonics between 250Hz(5^{th}) and 1250Hz (25^{th}) are eliminated as expected. The first dominant voltage harmonic is observed at 1450 Hz. Percentage of 5^{th} and 7^{th} harmonics are 0.7 % and 0.65 %, respectively.

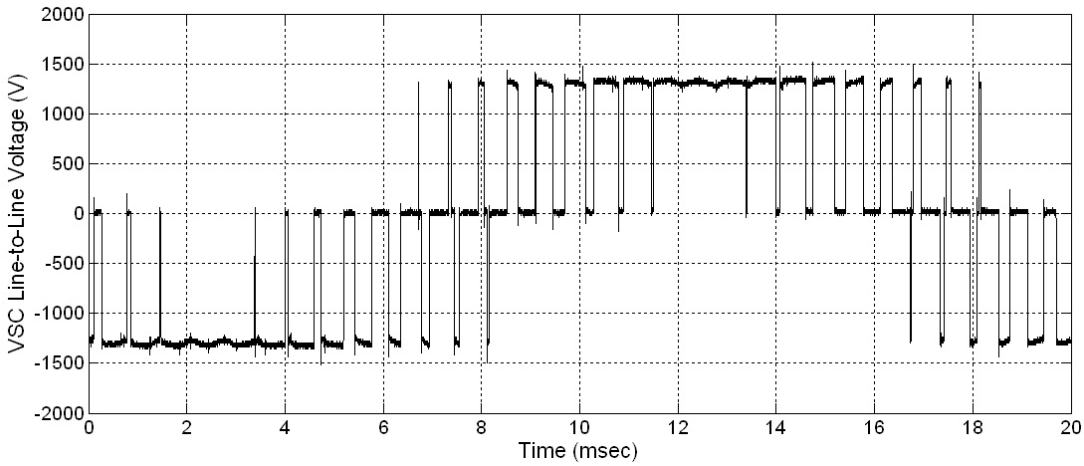


(a)

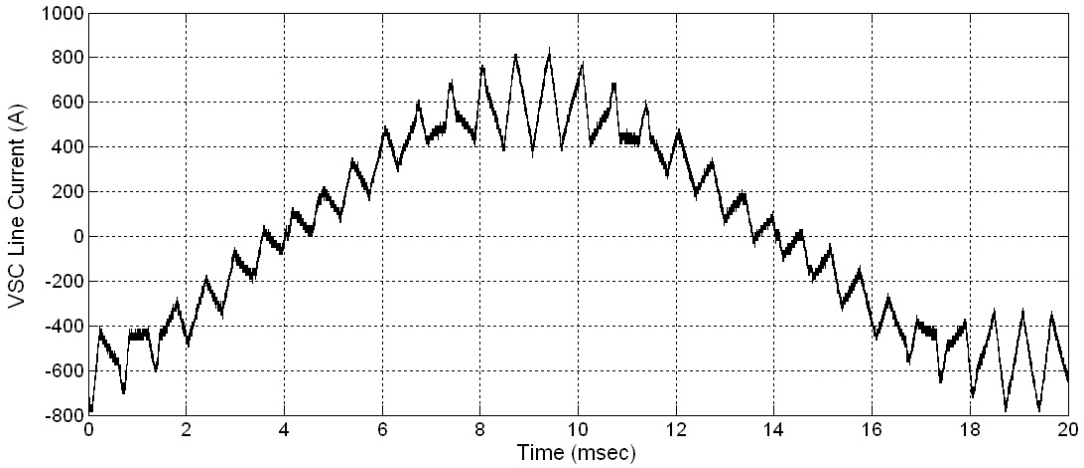


(b)

Figure 4.19 VSC Waveforms in Capacitive Operation Mode
a : VSC Line-to-Line Voltage ; b: VSC Line Current

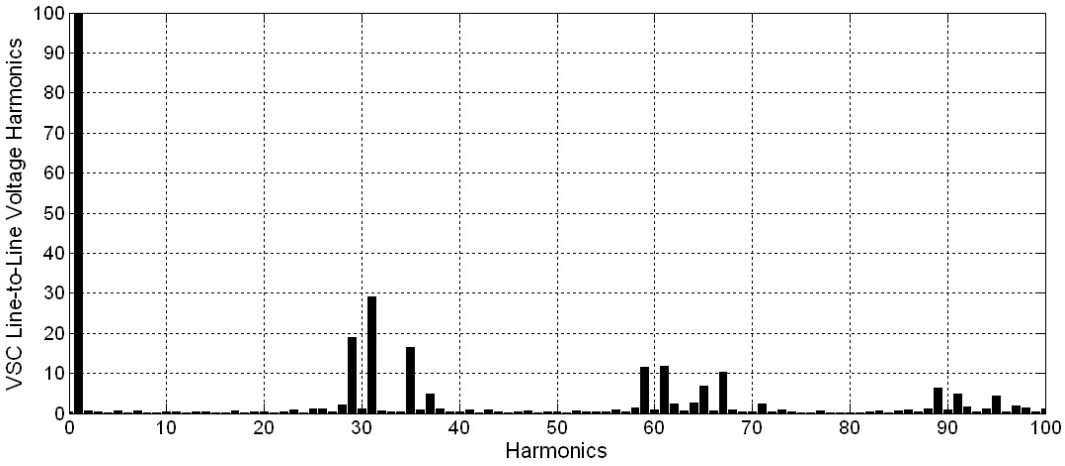


(a)

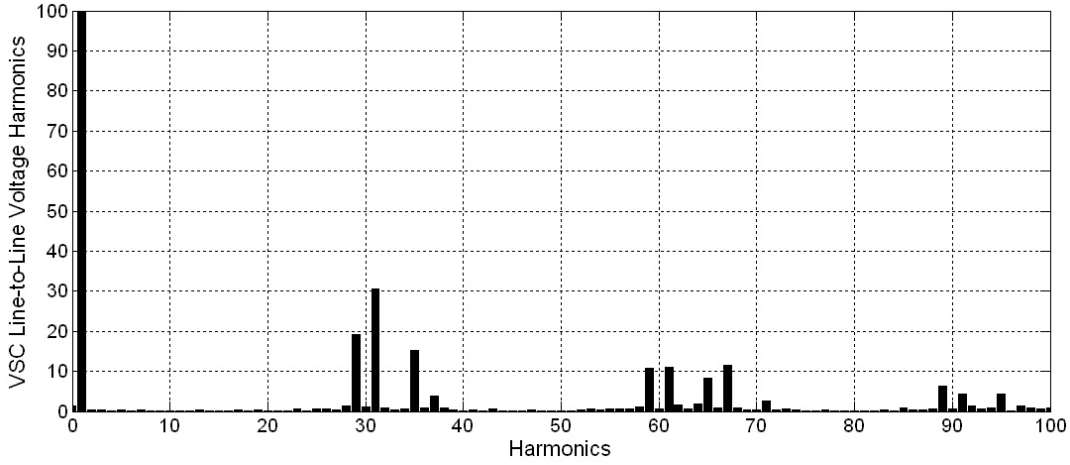


(b)

Figure 4.20 VSC Waveforms in Inductive Operation Mode
a : VSC Line-to-Line Voltage ; b: VSC Line Current



(a)



(b)

Figure 4.21 VSC Line-to-Line Voltage Harmonics (% V_{fund})
a : Capacitive Operation Mode ; b: Inductive Operation Mode

4.2.4 Input Filter Capacitor Waveforms (I_f in Fig. 4.2)

Filter line currents are given in Fig. 4.22 for capacitive and inductive operation modes.

VSC line current waveforms given in Fig. 4.19 and Fig. 4.20 are similiar to the filter capacitor line current waveforms given in Fig. 4.22. Therefore, it can be concluded that switching harmonic currents of VSC are filtered out by the input filter of STATCOM to a certain extend.

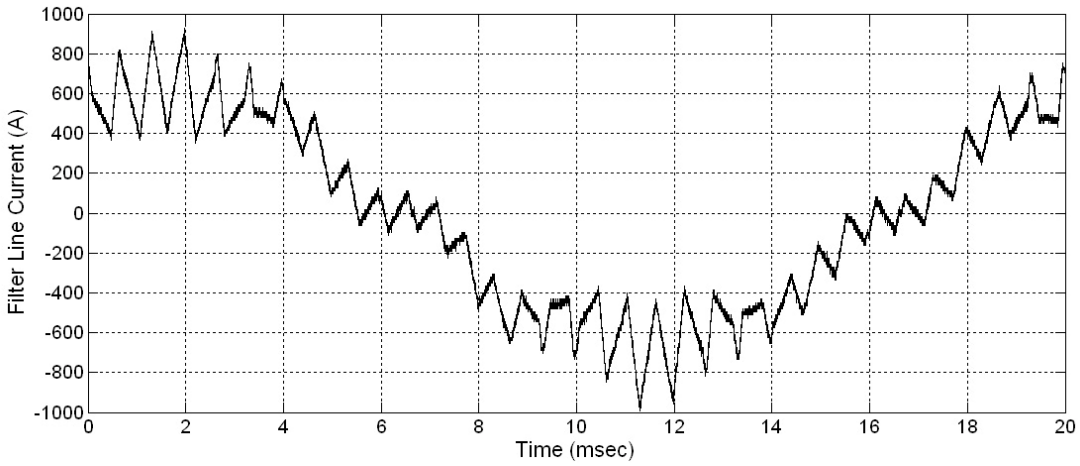
4.2.5 1kV Waveforms (V_{1kV} and I_{1kV} in Fig. 4.2)

1kV line-to-line voltage and line current waveforms are shown in Fig. 4.23 for capacitive operation mode and in Fig. 4.24 for inductive operation mode.

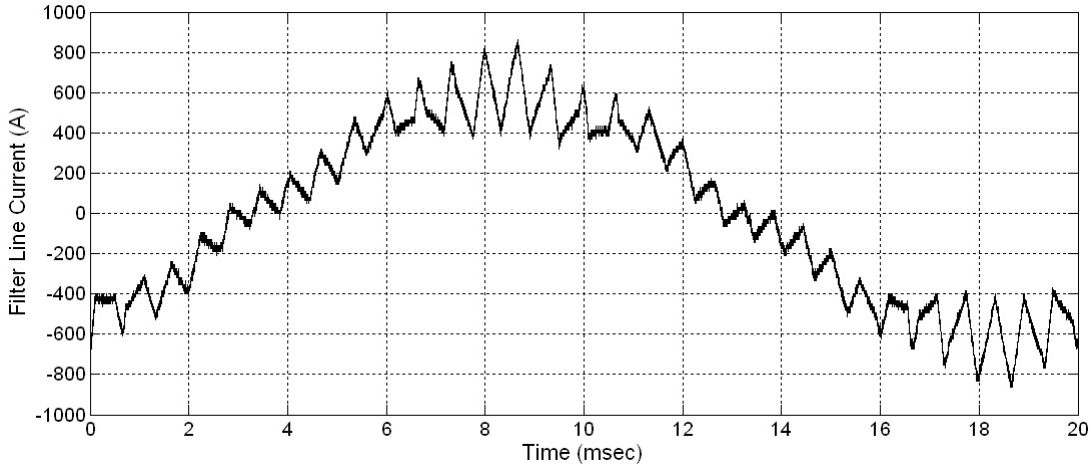
Noise pick-up is seen in the line-to-line voltage waveforms because of the switching harmonics of the converter. Noise pick-up is not seen on the line current waveforms as expected.

Fig. 4.24 is recorded for zero reactive power generation. Fundamental VSC current is canceled by the fundamental input filter current. This is the reason of the line current waveform in Fig. 4.24.

5^{th} and 7^{th} harmonics are observed in 1kV line-to-line voltage and line current waveforms as shown in Fig. 4.25. However, VSC does not produce any voltage harmonics at these frequencies as given in Fig. 4.21. 1kV line current waveform is given in Fig. 4.26 when VSC is disconnected from 1kV bus. 18 % of 5^{th} harmonic current and 1% of 7^{th} harmonic current are observed in the line current for this case. Therefore, we can conclude that 5^{th} and 7^{th} harmonic currents are the supply harmonics sinked by the input filter of STATCOM. However, magnitude of 5^{th} harmonic current decreases when VSC is connected to 1kV bus and STATCOM line current TDD is calculated as 4.9 % for 1500kVAr capacitive reactive power generation.

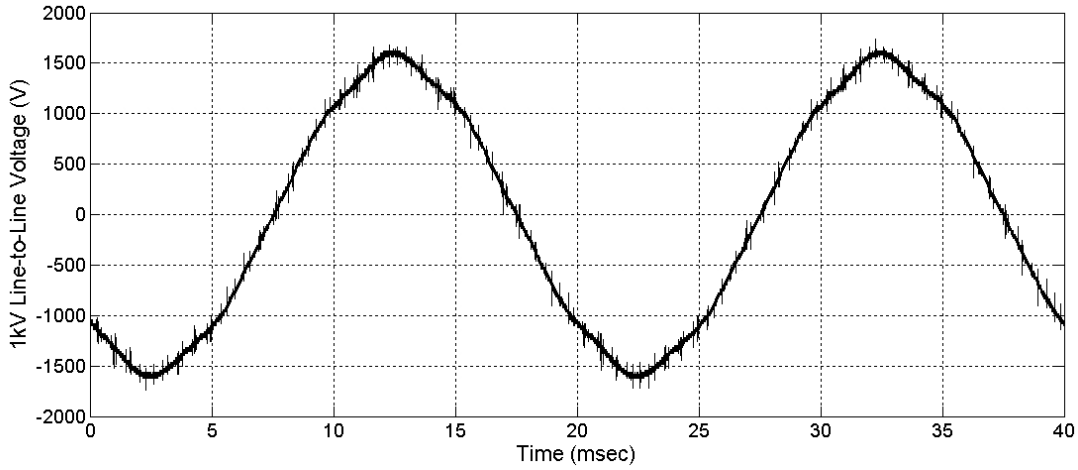


(a)

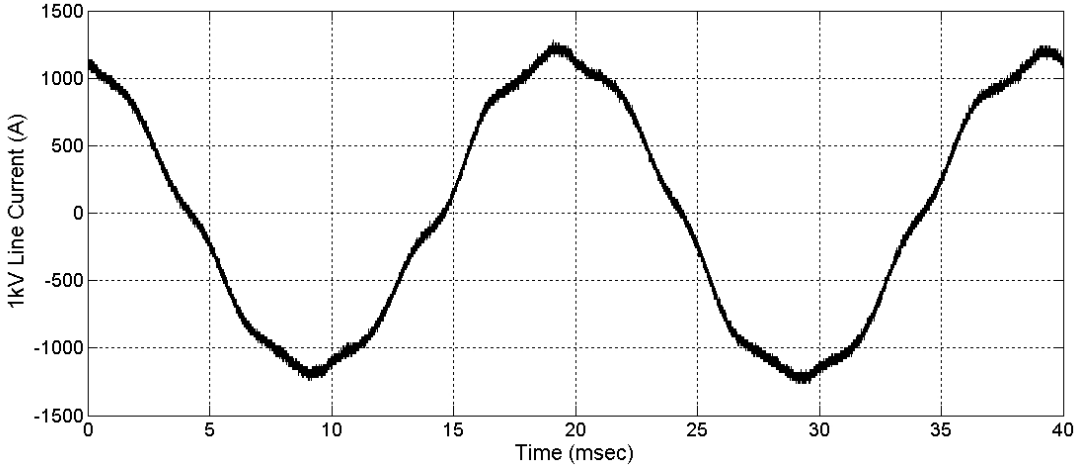


(b)

Figure 4.22 Input Filter Capacitor Line Current
a : Capacitive Operation Mode ; b: Inductive Operation Mode

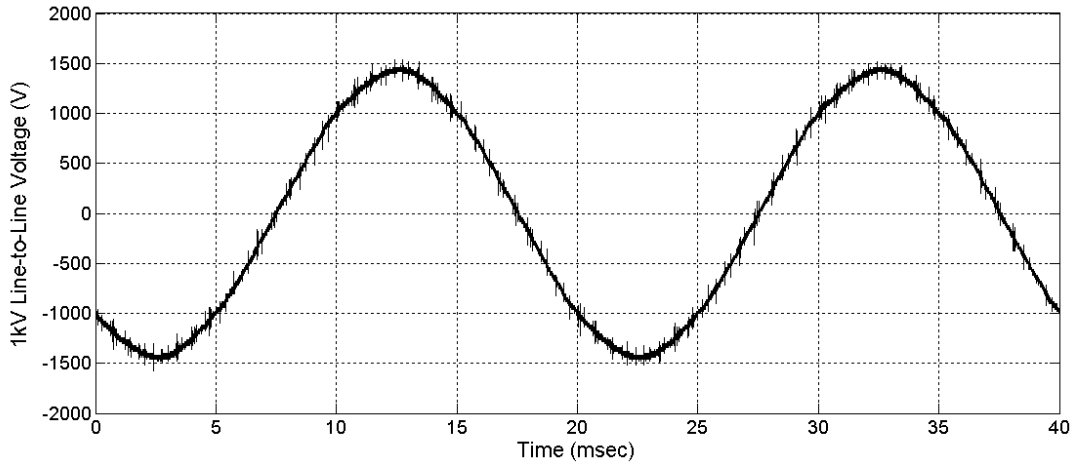


(a)

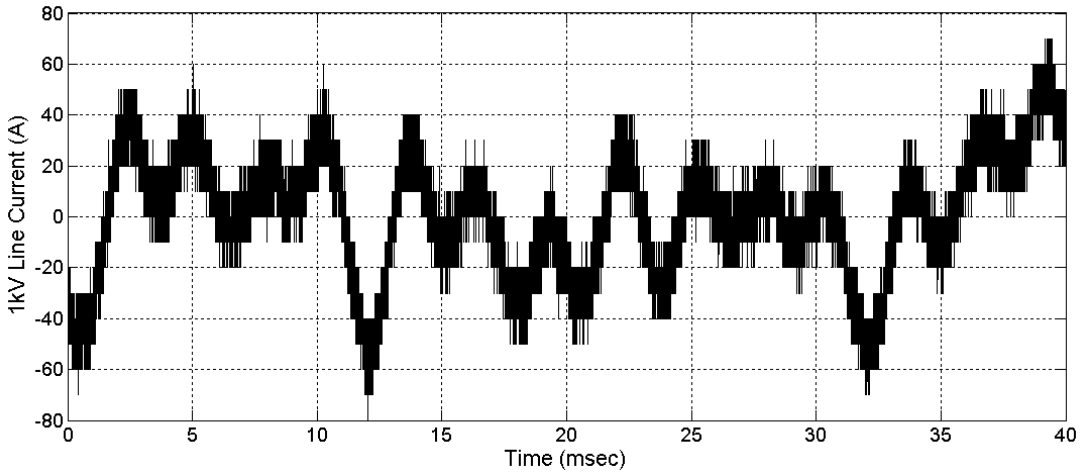


(b)

Figure 4.23 1kV Waveforms in Capacitive Operation Mode
A: Line-to-Line Voltage ; b :Line Current

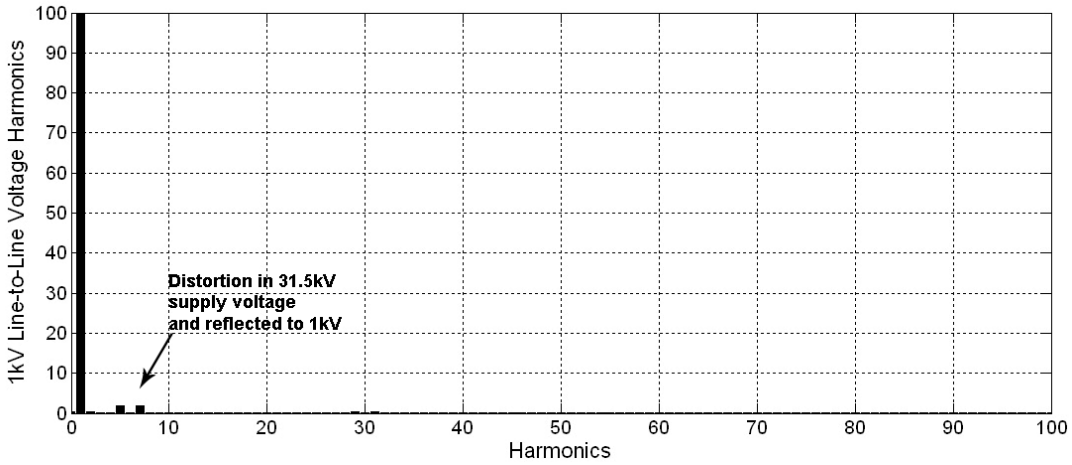


(a)

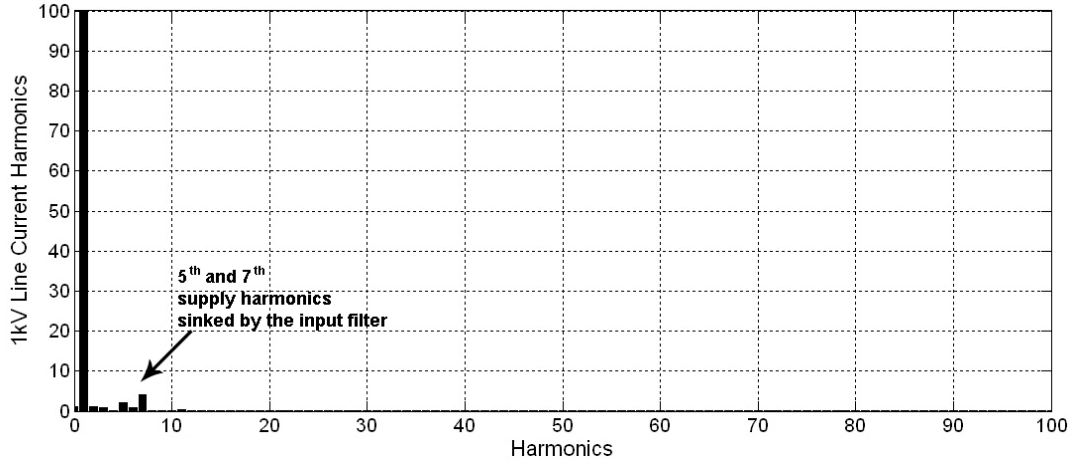


(b)

Figure 4.24 1kV Waveforms in Inductive Operation Mode
a: Line-to-Line Voltage ; b :Line Current



(a)



(b)

Figure 4.25 1kV Waveforms Harmonic Spectra in Capacitive Operation Mode a: Line-to-Line Voltage ; b : and Line Current

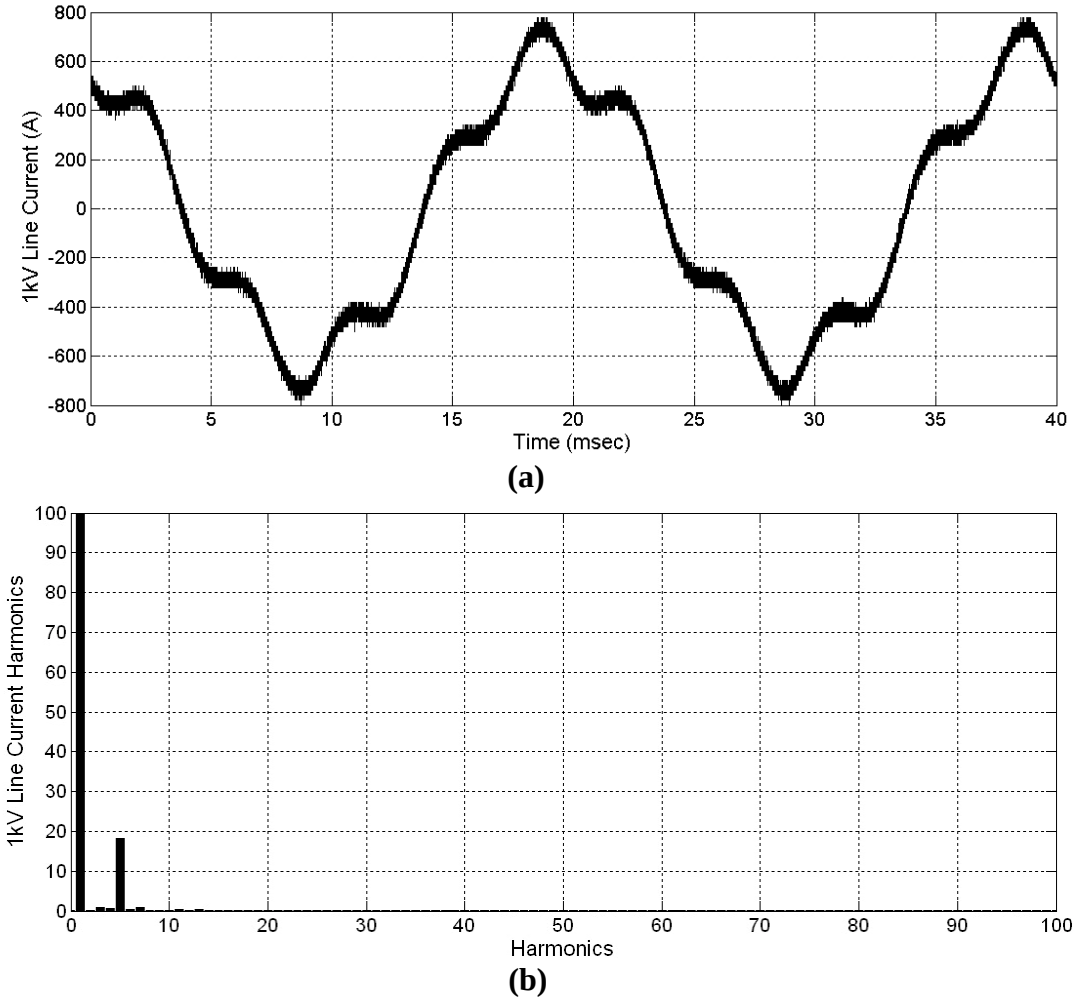


Figure 4.26 1kV Line Current when VSC is disconnected from 1kV bus
a: Waveform ; b : Harmonic Spectra

Variations in THD at STATCOM 1kV line current is shown in Fig. 4.27 with respect to STATCOM reactive power generation. It is seen from DC link voltage waveforms that DC link voltage changes between 1608V and 1289V from capacitive operation mode to inductive operation mode. Line-to-line VSC voltage harmonics are directly related to the DC link voltage since modulation index is constant. Therefore, minor voltage harmonic content is obtained in the the inductive operation mode. However, 1kV fundamental line current increases in capacitive operation mode and 1kV line current THD decreases as the reactive power generation of STATCOM increases as seen from Fig. 4.27.

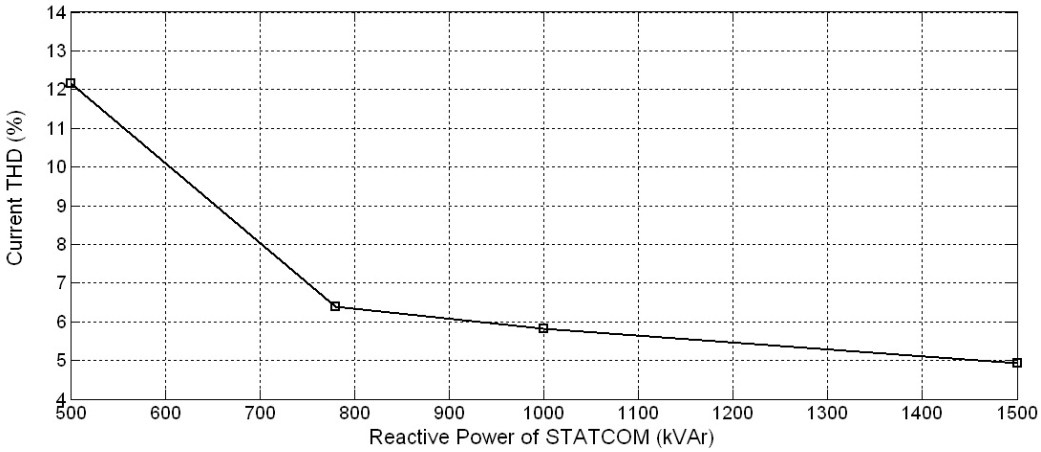


Figure 4.27 1kV Line Current THD (Experimental)

TDD of 1kV line current is found to be 4.9 % and THD of 1kV line-to-line voltage is found to be 2.7 %.

4.2.6 Characterization of Power Losses

Total power losses of STATCOM sytem including the coupling transformer, input filter, VSC and water cooling system are measured on 6.3kV side. The results are given in Fig. 4.28.

Main sources of power losses are given below :

- Coupling transformer
- VSC
- Input filter inductance
- Water Cooling System

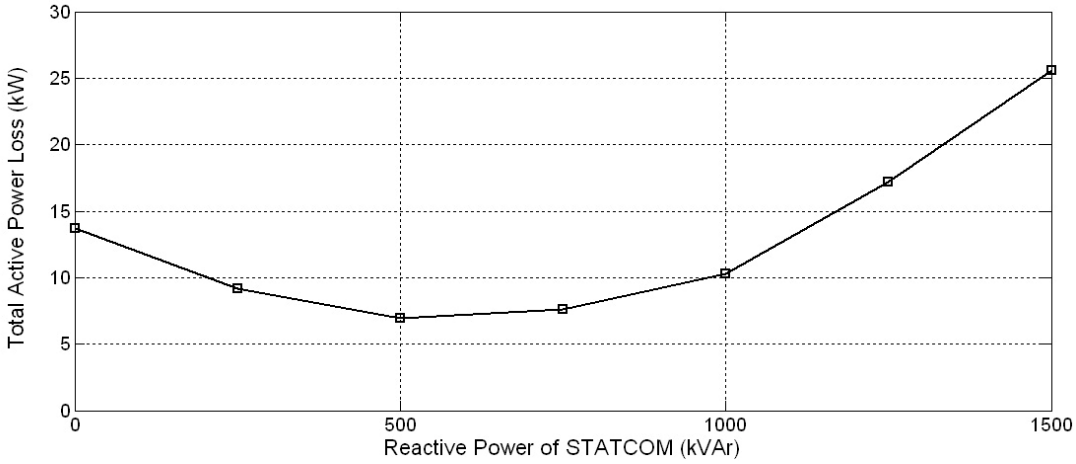


Figure 4.28 Total Active Power Losses of STATCOM System with respect to Generated Capacitive Reactive Power

Water cooling system is composed of pump unit having a power rating of 2.2 kW and heat exchanger fan having a power rating of 0.85 kW. Voltage and current measurements are recorded for 2 minutes at each reactive power level. Hence, heat exchanger fan did not work during this test.

Input filter inductance fundamental current is measured as 370 A for 1500kVAr capacitive reactive power generation and 440 A for zero reactive power generation.

Therefore, power loss of input filter inductance is found to be 2.1 kW and 2.9 kW, respectively.

VSC power loss is found to be 8.57 kW from the power loss at zero reactive power generation (inductive operation mode). Calculated power loss for zero reactive power generation is 9 kW and this value is very near to the measured value.

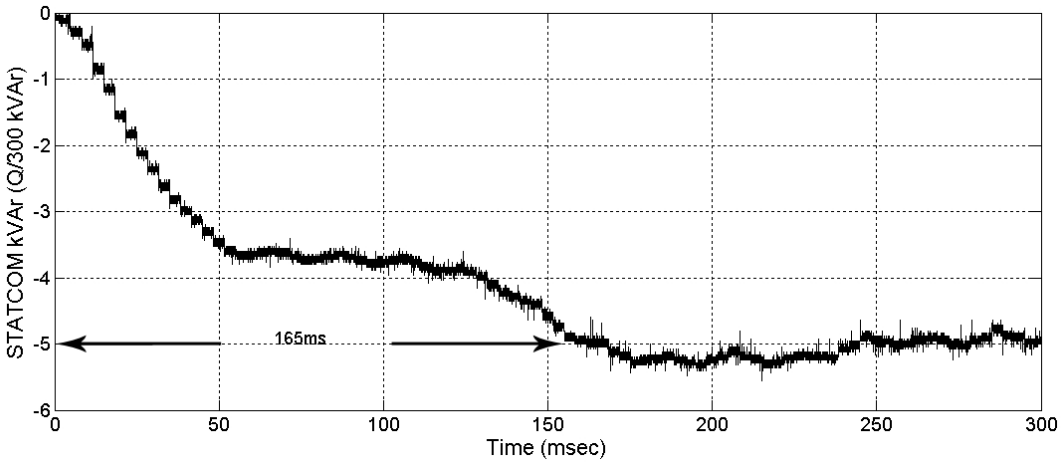
Total power loss of STATCOM system at 1500 kVAr capacitive reactive power generation is 1.7 % of STATCOM system reactive power rating and can be said to be very low.

4.2.7 Reactive Power Compensation Performance

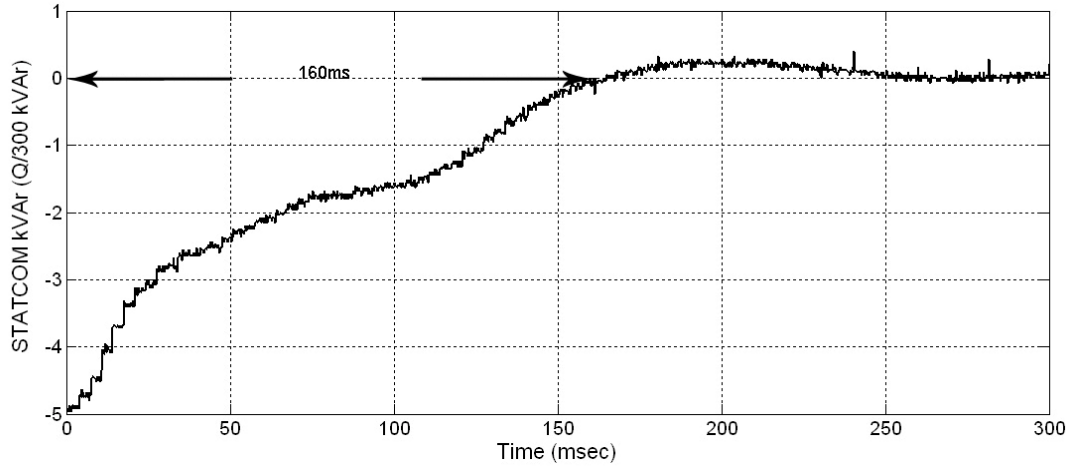
Transient response of STATCOM is found by applying a step input to the reactive power reference of the control system. Control system of STATCOM accepts 1500 kVAr as -5 V. A step input from 0 V to -5 V is applied to the control system to obtain the transient response from inductive operation mode to capacitive operation mode and a step input from -5 V to 0 V is applied to the control system to obtain the transient response from capacitive operation mode to inductive operation mode. Results are given in Fig. 4.29.

Closed loop response time is found to be 160 ms from capacitive operation mode to inductive operation mode and 165 ms from inductive operation mode to capacitive operation mode.

In PSCAD simulations, closed loop response time is found to be 150 ms from capacitive operation mode to inductive operation mode and 140 ms from inductive operation mode to capacitive operation mode.



(a)



(b)

Figure 4.29 Transient Response
a: Inductive Operation Mode to Capacitive Operation Mode
b : Capacitive Operation Mode to Inductive Operation Mode

In MATLAB simulations, closed loop response time is found to be 120 ms for both cases.

It is seen that PSCAD simulations are more realistic than MATLAB simulations since MATLAB model depends solely on the transfer function of STATCOM and PSCAD models power system, power electronic circuits and the control block. Therefore, it gives more accurate results. Satisfactory responses are obtained with closed loop control of STATCOM.

4.2.8 Waveforms at PCC ($V_{6.3kV}$ and $I_{6.3kV}$ in Fig. 4.2)

Voltage and current waveforms are recorded at STATCOM 6.3 kV side for capacitive operation mode. Results are given in Fig. 4.30.

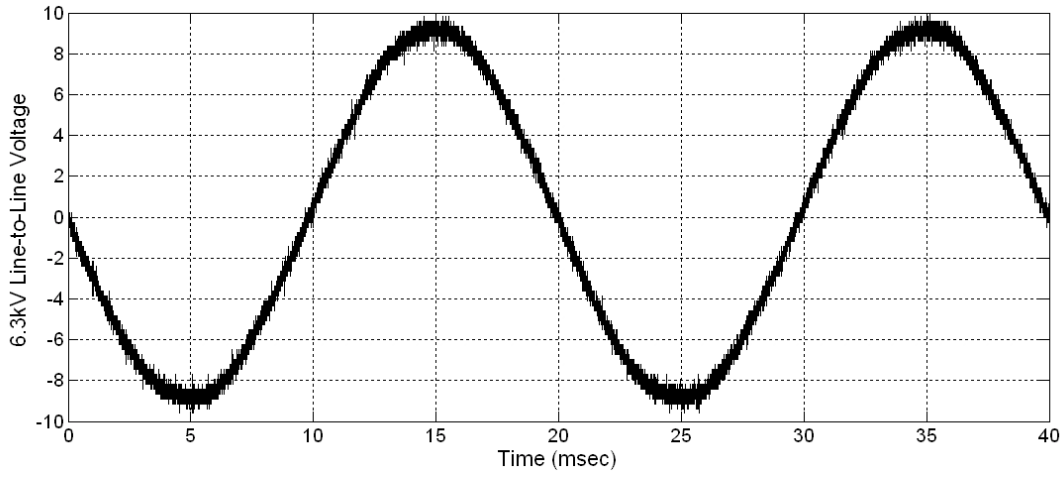
TDD of 6.3 kV (PCC) line current is found to be 4.8 % and THD of 6.3kV (PCC) line-to-line voltage is found to be 1 %.

Therefore, current TDD and voltage THD design specifications given in Chapter 3 are said to be satisfied.

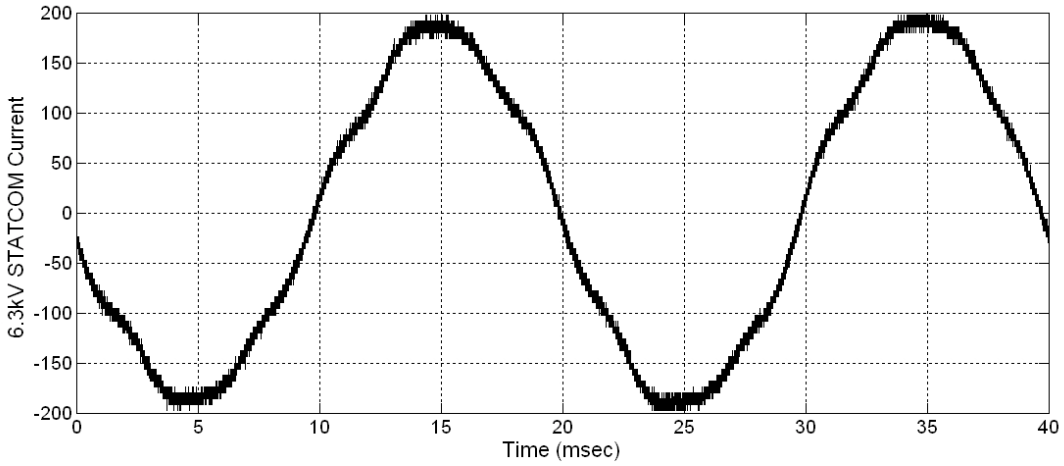
4.2.9 Waveforms at PCC ($V_{31.5kV}$ and $I_{31.5kV}$ in Fig. 4.2)

Voltage and current measurements are recorded at 31.5 kV and 6.3 kV side to obtain 31.5 kV source reactive power and STATCOM reactive power. Load reactive power is found by subtracting STATCOM reactive power from 31.5 kV source reactive power. Measurements are performed simultaneously for this purpose. Results are given in Fig.4.31.

It is seen from Fig. 4.31 that STATCOM produces the negative of the load reactive power semand as long as the load reactive power does not exceed the limits of STATCOM. A zoomed-in part of Fig. 4.31. is also given in Fig. 4.32.

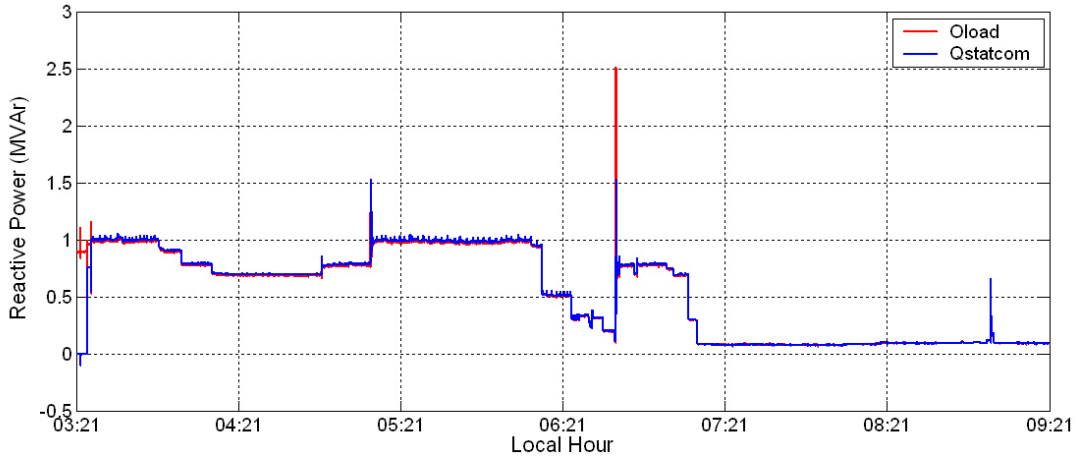


(a)

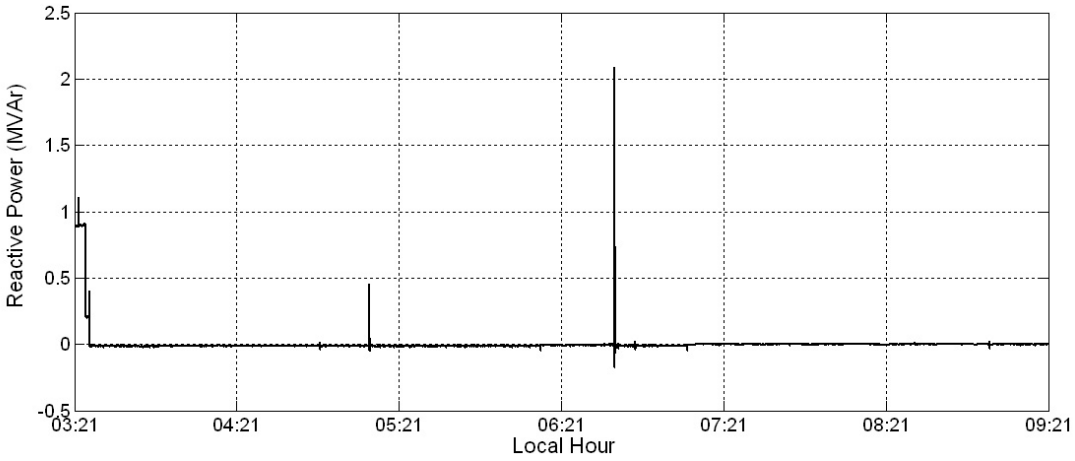


(b)

Figure 4.30 STATCOM Voltages and Currents at 6.3 kV
a: Line-to-Line Voltage ; b : Line Current



(a)



(b)

Figure 4.31 Measured Reactive Powers
A : Load and STATCOM Reactive Power ; b : 31.5kV Source Reactive Power

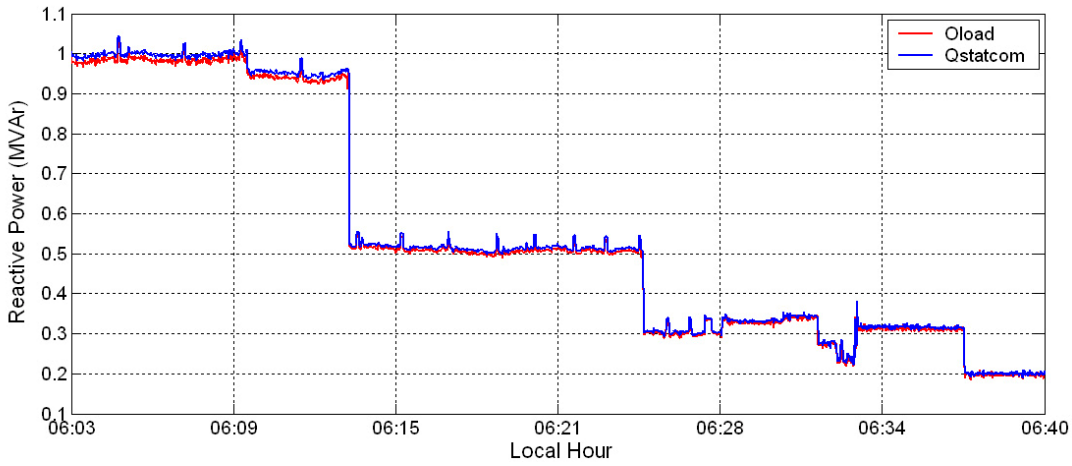


Figure 4.32 Load and STATCOM Reactive Power (Zoomed-In)

31.5 kV side voltage and current waveforms recorded before compensation are shown in Fig. 4.33.

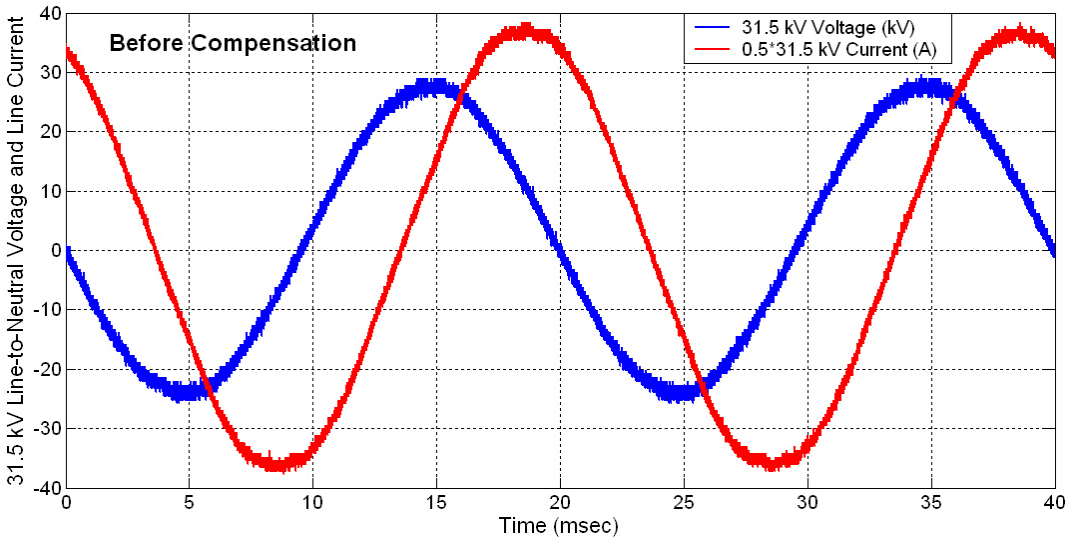


Figure 4.33 Line-to-Line Voltage and Line Current Before Compensation

31.5 kV side voltage and current waveforms recorded after compensation are shown in Fig. 4.34.

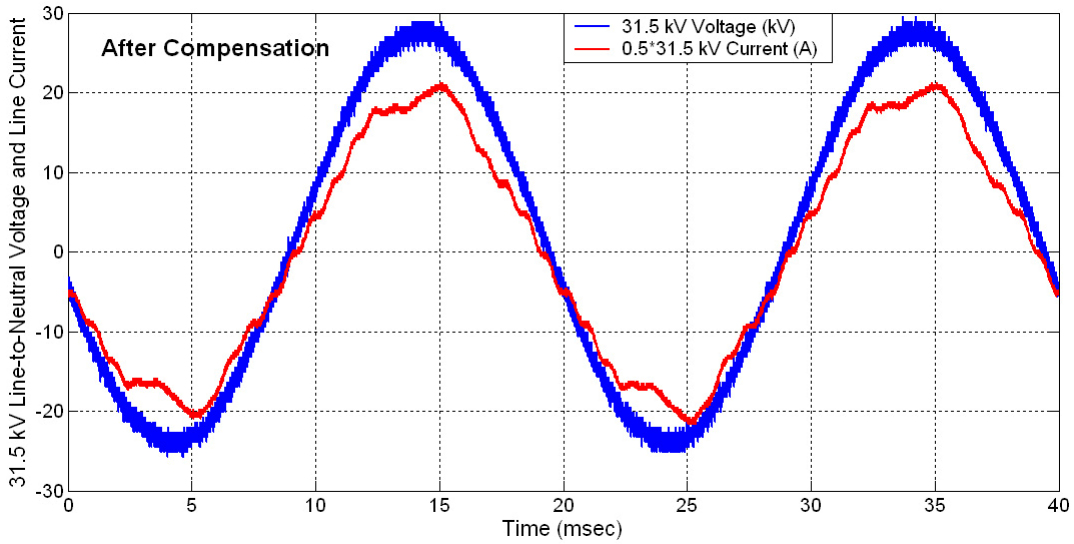


Figure 4.34 Line-to-Line Voltage and Line Current After Compensation

Following conclusions can be drawn from Fig. 4.33 and Fig. 4.34.

- Reactive power compensation of coal conveyor belt motors reduces the line current drawn from the supply by nearly 45 % for the corresponding operating conditions.
- After compensation, line current on supply side is observed to be slightly distorted. This is an expected result, because input filter sinks part of the supply side harmonics.

4.2.10. Energy Meter Results

STATCOM system is tested for one week in the field. Recorded active and reactive energy meter readings are given in Table 4.1. Daily results show the ratio of inductive and capacitive energy meter changes as a percentage of the active energy meter change on the daily basis and weekly results show the ratio of inductive and capacitive energy meter changes as a percentage of the active energy meter change with respect to the active and reactive meter reading in 12/03/2007.

Table 4.1 STATCOM One Week Field Test Energy Meter Results

Date	Active Meter (A)	Inductive Reactive Meter (I)	Capacitive Inductive Meter (C)	$\frac{\Delta I}{\Delta A}$ (%)	$\frac{\Delta C}{\Delta A}$ (%)	$\frac{\Delta I}{\Delta A}$ (%)	$\frac{\Delta C}{\Delta A}$ (%)
				Daily		Weekly	
12/03/07	169.227	165.546	7.668				
13/03/07	170.435	165.666	7.727	9.93	4.88	9.93	4.88
14/03/07	171.722	165.692	7.803	2.02	5.91	5.85	5.41
15/03/07	173.333	165.719	7.891	1.68	5.46	4.21	5.43
16/03/07	174.692	165.739	7.976	1.47	6.25	3.53	5.64
17/03/07	175.935	165.759	8.051	1.61	6.03	3.18	5.71
18/03/07	177.576	165.782	8.134	1.40	5.06	2.83	5.58
19/03/07	179.110	165.808	8.210	1.69	4.95	2.65	5.48

Ratio of inductive energy meter change as a percentage of active energy meter change on the weekly basis is found to be 2.65 %. This corresponds to a displacement factor of 0.9996.

Ratio of capacitive energy meter change as a percentage of active energy meter change on the weekly basis is found to be 5.48 %. This corresponds to a displacement factor of 0.99985.

It can therefore be concluded that STATCOM system fulfills the reactive power compensation of coal conveyor belts successfully in accordance with current regulations.

CHAPTER 5

CONCLUSIONS

Critical industrial processes have been increasingly affected by power quality problems caused by distorting loads in electric power systems. To cope with this problem, Static VAR compensators become necessary both at the utility and at the load sides. STATCOM systems constitute a good alternative for reactive power compensation problems with the advantages such as faster response, minimum harmonic content and smaller system size.

Reactive energy penalty limits imposed by Energy Market Regulatory Authority of Turkey necessitate nearly unity power factor operation, and therefore the use of static reactive power compensators. D-STATCOMs have outstanding features as compared to the other SVC systems, such as the capability of supplying the same reactive power irrespective of the supply voltage fluctuations, with faster response and smaller system size. VSC based D-STATCOM, designed and implemented within the scope of this work, has been applied to solve the reactive power compensation problem of coal conveyor belts for the first time in the literature.

In this research work, a prototype VSC based -STATCOM with phase angle control, and employing SHEM technique has been designed and implemented with the simplest converter topology (2 level, 3 leg) employing HV IGBT modules by using the theoretical work given in Chapters 2 and 3.

D-STATCOM implementations reported in the literature so far employ high frequency PWM technique. However, in this thesis, SHEM technique is applied to to medium power VSC based D-STATCOM for the first time, for reactive power compensation of industrial loads. It is shown that SHEM technique is superior to PWM technique when switching losses of HV IGBT modules are considered. IEEE Std. 519-1992 for weak supply conditions is satisfied with the use of SHEM

technique and STATCOM currents close to sine wave are obtained with a current THD less than 5 %.

STATCOM system parameters have been optimized for phase angle control technique, making a compromise between system performance and transient response. In view of these considerations, input filter size has been investigated in order to meet the IEEE Std. 519-1992 standard. Current TDD and voltage THD formulations are found for only L and low pass LC filters, for the selected SHEM technique. Only L filter necessitates the use of higher filter inductances for weak supply cases. When using lowpass LC filters, a filter capacitance having a power rating of 10-20 % of the converter is sufficient to filter out the switching frequency harmonics of the converter. However, larger input filter size can be used to lower the voltage THD at the PCC, where VSC is connected (secondary of the coupling transformer). This can be achieved either by using higher inductances or higher capacitance values. Input filter size is also effective on the open loop response time of D-STATCOM. In addition to this, input filter size determines the voltage regulation on the DC link capacitor and thereby limits the maximum reactive power that can be generated by the converter because of LTDS (Long Time DC Stability) voltage of HV IGBT modules.

In MV converters, different from LV ones, high switching frequencies are not feasible because of higher switching losses, and single side cooling of the HV IGBT modules. Therefore, switching frequency optimization must be carried out by considering the converter part, input side voltage and current TDD specifications. By taking the present status of HV IGBT technology into account, the number of harmonics to be eliminated and the value of modulation index have been optimised by a hybrid method that uses genetic algorithm as the first phase of the solution and then MATLAB`s gradient based constraint optimization method for fine tuning. By this way, the switching frequency of VSC STATCOM and modulation index have been determined. In the thesis, 7-Angle (6 Harmonics Elimination with Modulation Index Control) SHEM, 9-Angle (8 Harmonics Elimination with Modulation Index Control) SHEM and 11-Angle (10 Harmonics Elimination with Modulation Index Control) SHEM techniques have been compared and 9-Angle SHEM technique

with a modulation index of 0.9 p.u. is found to be the optimum solution considering the design constraints for the modulation index. Finally, to decrease the switching frequency further, 8-Angle (8 Harmonics Elimination with No Modulation Index Control) SHEM technique is searched for a solution having a modulation index of 0.9 p.u., and the found solution is used as the switching pattern in the implemented converter.

Different reactive power control methods described in Chapter 2 have been studied in the thesis. Phase angle control has been found as the most suitable control method for SHEM technique and has been used in the implemented converter. Transient response of the STATCOM system is measured as 160ms from full capacitive to full inductive mode, and 165ms from full inductive to full capacitive mode. These response times are adequate for the performance needed in coal conveyor belts. Switching pattern is updated at every zero crossing of the line-to-line voltage in the implementation. Updating the switching pattern at every half cycle will decrease the closed loop response under 100 ms. Other control methods discussed in Chapter 2 can be used when faster closed responses are needed by different loads.

Simulation studies have been performed by PSCAD/EMTDC, MATLAB and ORCAD programs. All parts of the STATCOM system including medium voltage transformers, power stage and control block are simulated in PSCAD successfully. Since, PSCAD program can not simulate switching transients of HV IGBT modules, switching transient simulations are carried out in ORCAD/PSPICE. Control system of STATCOM is simulated both in MATLAB and PSCAD. MATLAB model is not a complete model of STATCOM as in PSCAD, only the control system performance and the variation of the system parameters on the response have been obtained from the MATLAB simulations. PSCAD simulation results are consistent with the field results obtained for the converter, input filter part and the closed loop system response. However, shorter closed loop response times are obtained with MATLAB when compared with the field test results.

It is worth to note that, in the medium power converter implementation, careful design of laminated busbar of the converter, and thereby minimization of the effective dc link inductance is very important. Correct design of the laminated busbar is not sufficient, also dc link capacitors must be selected carefully in order to use the HV IGBT modules efficiently. Higher effective dc link inductances necessiate the use of decoupling capacitors over one-leg for low power converters, and RCD clamping snubbers for medium power converters. 59.3 nH effective DC link inductance is obtained in the designed system according to the measurements carried out in laboratory and field test. Laminated busbar design becomes even more important for higher power converters.

Based on these operating principles described in this research work, not only qualitative but also quantative design criteria for developing a VSC based STATCOM have been given. These are summarized in Table 5.1.

Table 5.1 Effect of Main System Parameters On Cost and Performance

System Component Choosen	Advantages	Disadvantages
The use of larger filter inductance	• lowers harmonic current content	• higher cost • worse closed loop response • higher voltage regulation on the DC link capacitor and thereby limiting STATCOM reactive power rating
The use of bigger input filter capacitance	• lowers harmonic current content • low cost compensation of fixed part of the load VAR demand	• makes VAR characteristic asymmetric • series resonant risk at low order supply harmonics

Table 5.1 (Cont'd) Effect of Main System Parameters On Cost and Performance

System Component Choosen	Advantages	Disadvantages
DC link capacitor with minimum storage capacity	• fast closed loop response • lower cost	• higher harmonic current content
Higher switching frequency	• lowers harmonic content • permits the use of minimised intermagnetic components	• higher switching losses • more costly cooling system
The use of presspack HV IGBTs instead of wirebond HV IGBTs	• higher power dissipation capability • higher VAR generation capability	• few candidate presspack IGBTs • higher cost
The use of SHEM with phase angle control instead of on-line PWM techniques with simultaneous control of modulation index and phase angle	• allows optimised fixed PWM • allows lower switching frequencies • easier in implementation	• slower transient response • coupled active and reactive power control

The subsitution of PI controllers with other linear and nonlinear control methods, and performance comparisons will be one of the future work.

Reactive power capability of two level, three leg Voltage Source Converter can be increased beyond 2 MVAr with presspack HV IGBT modules. Redesign of the VSC STATCOM with presspack HV IGBBT modules will be another future work.

SHEM is known as an off-line PWM technique with fixed modulation index. However, the modulation index can be varied in steps. Due to advantages of SHEM over on-line PWM techniques, control of the phase angle and modulation index with the use of SHEM technique in VSC STATCOM will be an interesting future work topic.

In this research work, VSC based STATCOM is designed for reactive power compensation of balanced loads. Another future work can be the modification of the developed system for reactive power compensation of unbalanced loads.

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APPENDIX A

P, Q FLOW BETWEEN SOURCE and STATCOM

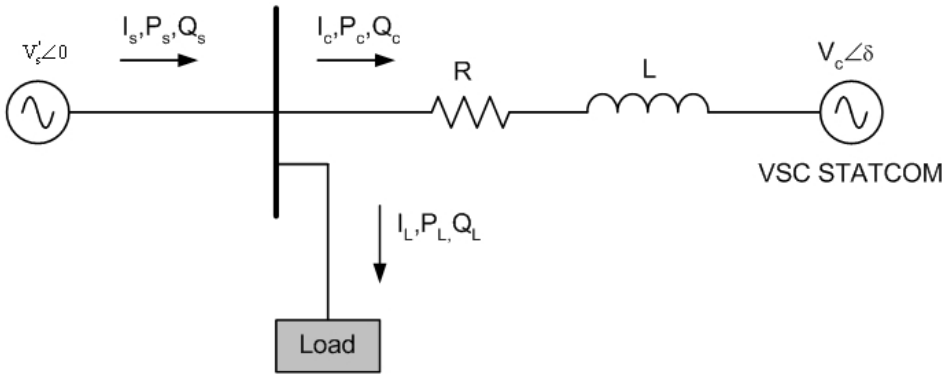

Figure A.1 Single Line Diagram of STATCOM

V_s' : RMS Line-to-neutral AC grid voltage with a phase angle of 0 referred to STATCOM side.

V_c : RMS Line-to-neutral STATCOM Fundamental Voltage

I_S : RMS source current

I_L : RMS load current

I_C : RMS STATCOM current

Q_s : Source reactive power

Q_L : Load reactive power

Q_C : STATCOM reactive power

δ : Phase angle between fundamental voltage of STATCOM and AC grid

R : Y equivalent total loss resistance including coupling transformer losses, series inductor, losses and converter losses

L : Y equivalent total inductance including series inductance and leakage inductance of coupling transformer.

The phasor representation of the single line diagram of STATCOM is given in Fig.A.2. The phasors are drawn for the case in which inductive reactive power is absorbed by STATCOM.

Power sink convension has been used in the formulations given (A.1)-(A.6). This convention associates a positive sign with the reactive power flowing into an inductive reactance. Real power (P_c) and reactive power (Q_c) are given according to phase quantities.

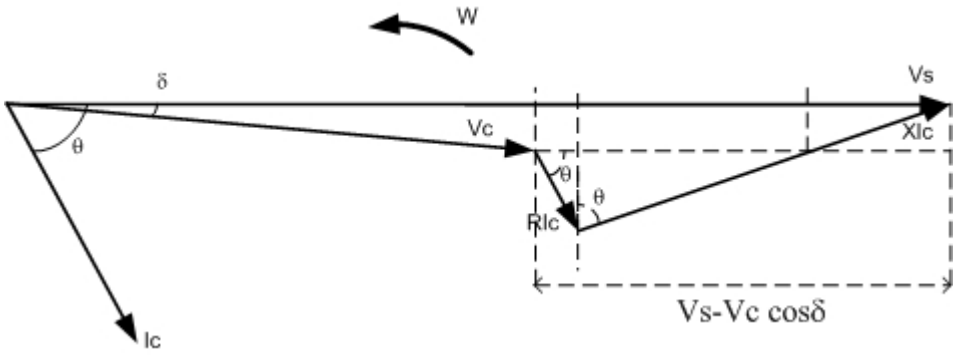

Figure A.2 Phasor Diagram

$$V_s - V_c \cos\delta = XI_c \sin\theta + RI_c \cos\theta = I_c(X\sin\theta + R\cos\theta) \quad \text{(A.1)}$$

$$V_c \sin\delta = XI_c \cos\theta - RI_c \sin\theta = I_c(X\cos\theta - R\sin\theta) \quad \text{(A.2)}$$

$$Q_c = V_s I_c \sin\theta = V_s \frac{V_s - V_c \cos\delta}{X\sin\theta + R\cos\theta}\sin\theta \quad \text{(A.3)}$$

$$P_c = V_s I_c \cos\theta = V_s \frac{V_c \sin\delta + RI_c \sin\theta}{X} \quad \text{(A.4)}$$

$$P_c = \frac{V_s}{X}\left[V_c \sin\delta + R\sin\theta \frac{V_s - V_c \cos\delta}{X\sin\theta + R\cos\theta} \right] \quad \text{(A.5)}$$

$$P_c = \frac{V_s}{X}\left[\frac{RV_s \sin\theta + XV_c \sin\theta\sin\delta - RV_c \sin\theta\cos\delta + RV_c \sin\delta\cos\theta}{X\sin\theta + R\cos\theta} \right] \quad \text{(A.6)}$$

APPENDIX B

PSCAD/EMTDC MODEL FOR VSC BASED STATCOM

VSC based STATCOM system is simulated in PSCAD/EMTC program. Converter waveforms, input filter waveforms, line currents are analyzed and closed loop control of STATCOM system is tested.

6.3 kV feeder model is given in Fig. B.1.

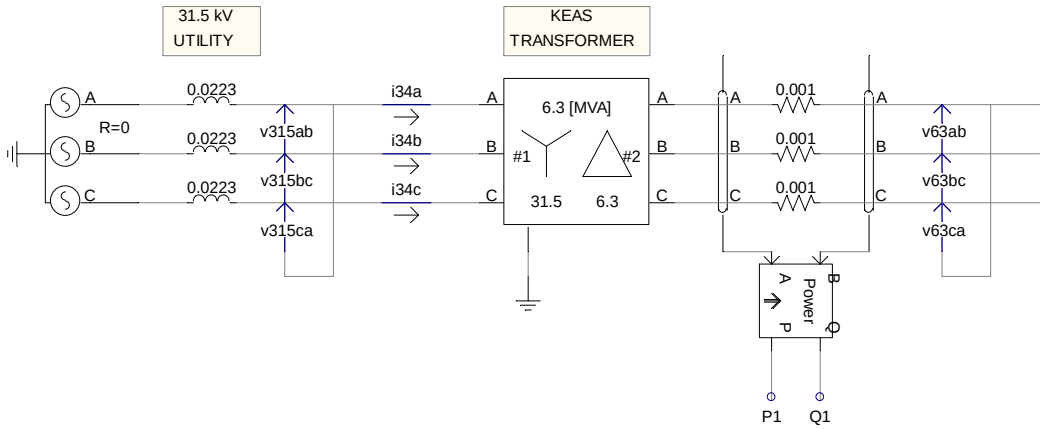

Figure B.1 6.3 kV Feeder Model

Coupling transformer model is given in Fig. B.2.

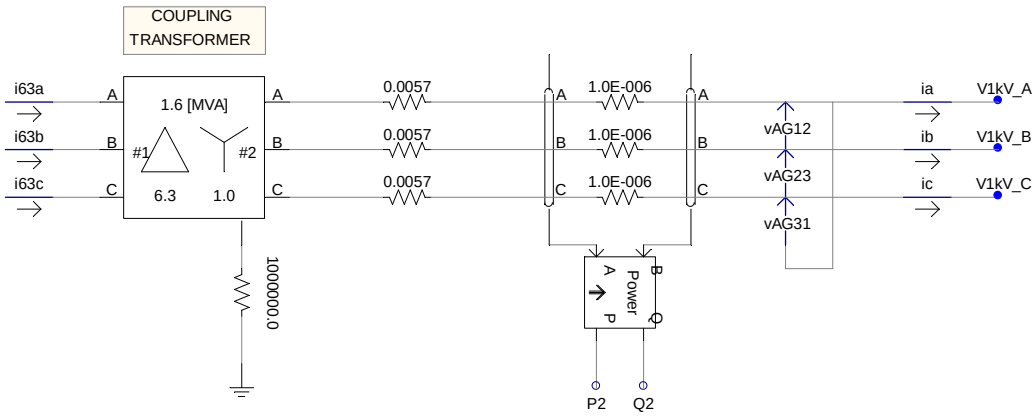

Figure B.2 Coupling Transformer Model

Input filter inductance model is given in Fig. B.3.

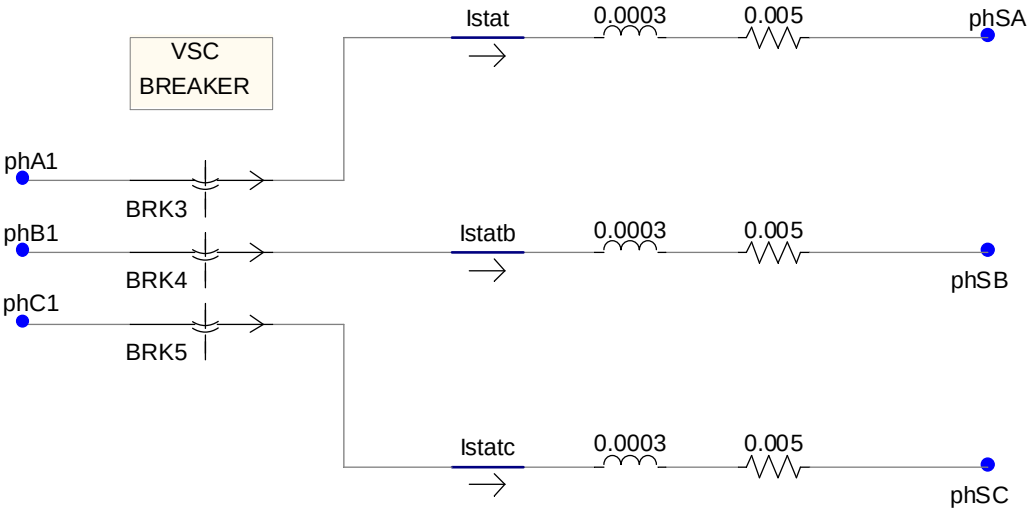

Figure B.3 Input Filter Inductance Model

Input filter capacitor model is given in Fig. B.4.

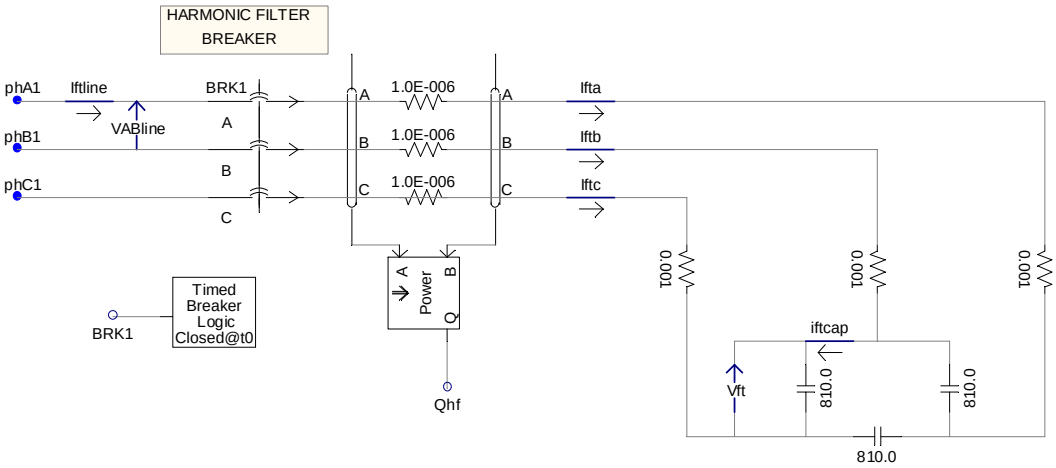

Figure B.4 Input Filter Capacitance Model

Converter model is given in Fig. B.5.

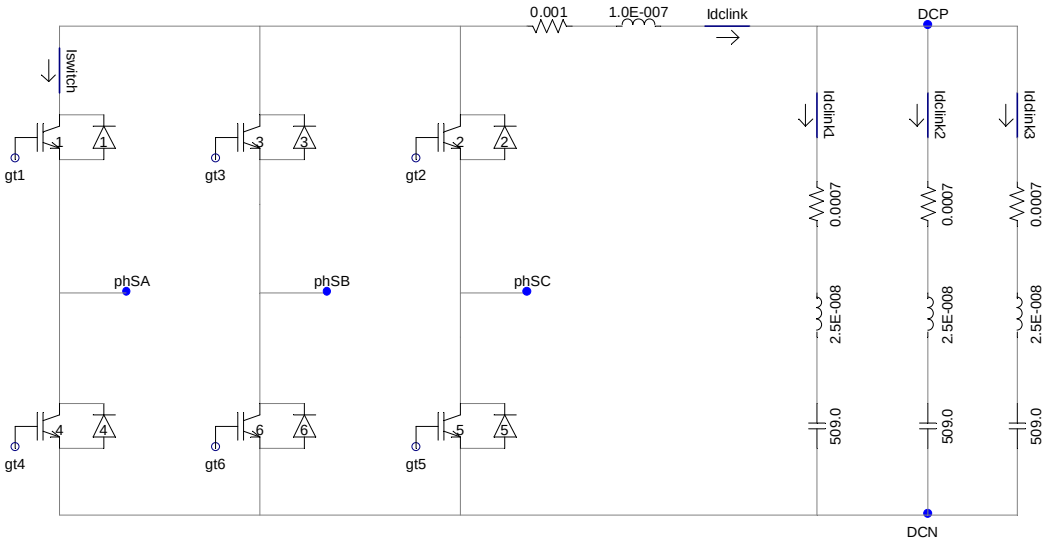

Figure B.5 Converter Model

Precharging and discharging circuit model is given in Fig. B.6.

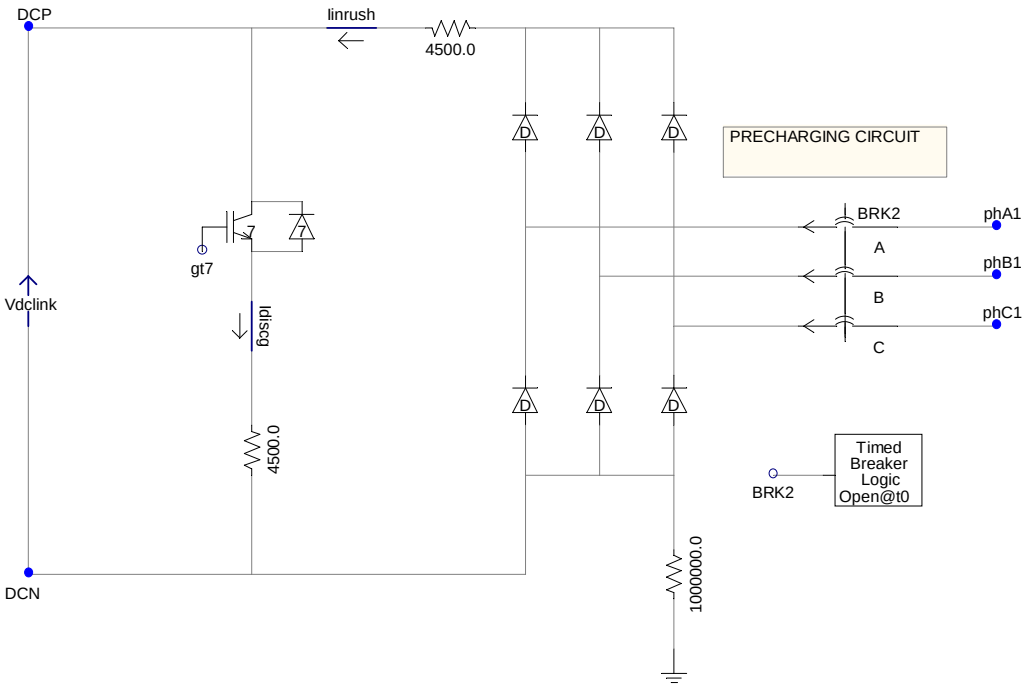

Figure B.6 Precharging and Discharging Circuit Model

APPENDIX C

MEASUREMENT APPARATUS

- Tektronix TDS5054 Digital Phosphor Oscilloscope
- Tektronix P5210 High Voltage Differential Probe
- Tektronix P5050 Voltage Probe
- Pearson Current Monitor 110
- Powertek, Rogowski Current Waveform Transducers
  - CWT 15B (2mV/A)
  - CWT 6B (5mV/A)
- National Instruments
  - DAQ 6062 E Data Acquisition System
  - SC2040 Sample and Hold Card
- Fluke 80i-110S AC/DC Current Probe

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