PARALLEL ACTIVE FILTER DESIGN, CONTROL, AND IMPLEMENTATION

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Approval of the Graduate School of Natural and Applied Sciences

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I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

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This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

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ABSTRACT

PARALLEL ACTIVE FILTER DESIGN,
CONTROL, AND IMPLEMENTATION

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The parallel active filter (PAF) is the modern solution for harmonic current mitigation and reactive power compensation of nonlinear loads. This thesis is dedicated to detailed analysis, design, control, and implementation of a PAF for a 3-phase 3-wire rectifier load. Specifically, the current regulator and switching ripple filter (SRF) are thoroughly investigated. A novel discrete time hysteresis current regulator with multi-rate current sampling and flexible PWM output, DHCR3, is proposed. DHCR3 exhibits a high bandwidth while limiting the maximum switching frequency for thermal stability and its implementation is simple. In addition to the development of DHCR3, in the thesis state of the art current regulation methods are considered and thoroughly compared with DHCR3. Since the current regulator type determines the SRF topology choice, various SRF topologies are considered and a thorough design study is conducted and SRF topology selection and parameter determination methods are presented via numerical examples. Through a PAF designed for a 10kW diode/thyristor rectifier load, the superior performance of DHCR3 is verified through simulations and experiments and via comparison to other current regulators. The sufficient switching ripple attenuation of the SRF structures

for the designed PAF system and the overall performance of the designed and built PAF system are demonstrated via detailed computer simulations and laboratory experiments. This thesis aids the PAF current regulator and SRF selection, design, and implementation.

Keywords: Paralel active filter, current regulation, linear current regulator, resonant filter, hysteresis current regulator, discrete time control, inverter, switching ripple filter, current harmonics, reactive power, design.

ÖZ

PARALEL ETKİN SÜZGEÇ TASARIMI,
DENETİMİ VE GERÇEKLEŞTİRİLMESİ

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Paralel etkin süzgeç (PES), doğrusal olmayan yüklerin harmonik akımlarını bastırmada ve tepkin güç kompanzasyonunda modern çözümdür. Bu tez, üç-faz üç-iletkenli doğrultucu yükler için PES'in ayrıntılı analizi, tasarımı, denetimi ve gerçeklenmesine üzerinedir. Özellikle, akım deneteci ve anahtarlama dalgacık süzgeci (ADS) ayrıntılı olarak incelenmiştir. Çok kat akım örneklemeli ve esnek darbe genişlik modülasyon (DGM) çıktılı özgün bir ayrık zamanlı histerezis akım deneteci, DHCR3, önerilmiştir. DHCR3, ısıl güvenlik için enyüksek anahtarlama frekansını sınırlarken yüksek bant genişliği göstermektedir ve DHCR3'ün gerçeklenmesi kolaydır. Tezde, DHCR3'ün geliştirilmesine ek olarak, modern akım denetim yöntemleri incelenmiş ve ayrıntılı olarak DHCR3'le karşılaştırılmıştır. Akım deneteç tipi ADS topoloji seçimini belirlediği için, çeşitli ADS topolojileri incelenmiş, ayrıntılı tasarım çalışması yapılmış ve ADS tolopoloji seçimi ve parametre belirleme yöntemleri sayısal örneklerle sunulmuştur. DHCR3'ün üstün başarımı, 10 kW'lık diyotlu/tristörlü doğrultucu yük için tasarlanan bir PES'te benzetimler ve deneylerle ve diğer akım deneteçleriyle karşılaştırmayla kanıtlanmıştır. Tasarlanan PES sistemi için ADS yapılarının yeterli oranda

anahtarlama dalgacıklarını azaltması ve tasarlanan ve üretilen PES sisteminin genel başarımı, ayrıntılı bilgisayarla benzetim çalışmalarıyla ve laboratuvar deneyleriyle gösterilmiştir. Bu tez, PES akım deneteci ve ADS'nin seçimi, tasarımı ve gerçeklenmesinde faydalıdır.

Anahtar Kelimeler: Paralel etkin süzgeç, akım denetimi, doğrusal akım deneteci, rezonant süzgeç, histerezis akım deneteci, ayrık zamanlı denetim, evirici, anahtarlama dalgacık süzgeç, akım harmonikleri, tepkin güç, tasarım.

To My Family,

Ömer Ali Özkaya and Ziynet Özkaya

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CHAPTER 1

INTRODUCTION

1.1. Background

In all aspects of modern life, utilization of electrical energy involves power electronics and microelectronics technologies. These technologies have considerably improved the quality of the modern life by allowing the introduction of sophisticated energy efficient controllable equipment to industrial and domestic applications. Examples of such applications are Adjustable Speed Drives (ASDs), Uninterruptible Power Supplies (UPSs), computer and their peripherals, consumer electronics appliances, etc. Such power electronic devices offer economical and reliable solutions to better manage and control the utilization of electric energy and are inevitable devices of modern life [1]. For example, ASDs widely employed in driving induction and permanent magnet motors due to the high static and dynamic performance, reduce energy consumption (20-30% saving) and decrease pollutant emission levels to the environment while increasing productivity. If an estimated 65% of industrial electrical energy used in by electric motors [2] is considered, the importance of power electronics in energy efficiency becomes clearer. Although the power electronics technology provides efficiency enhancement in energy utilization, it results in economic losses by creating power quality problems in electric distribution systems. Therefore, a conflict exists.

As inevitable parts of industrial and domestic loads fed from AC utility grid, many power electronic circuits utilizing modern semiconductor switching devices present nonlinear load characteristics and draw non-sinusoidal currents from the AC utility

grid supplying sinusoidal voltages. These power electronic devices injecting non-sinusoidal (harmonic) currents into the AC utility grid become the main polluters of the power system and result in power quality problems in the grid and affect sensitive loads. The harmonics injected to the power system cause line voltage distortions at the Point of Common Coupling (PCC) where the linear and nonlinear loads are connected, as shown in Figure 1.1. PCC is defined as the closest point of the customer to the utility grid where another utility customer is (or could be) supplied and the point at which harmonic limits are evaluated [2], [3]. Therefore, voltage distortions at the PCC caused by harmonic currents of nonlinear loads may result in malfunctioning or failure of voltage sensitive linear and/or nonlinear loads (such as computers and allied equipments, medical instruments, and loads utilizing supply voltage phase angle information, etc.) connected to the same PCC.

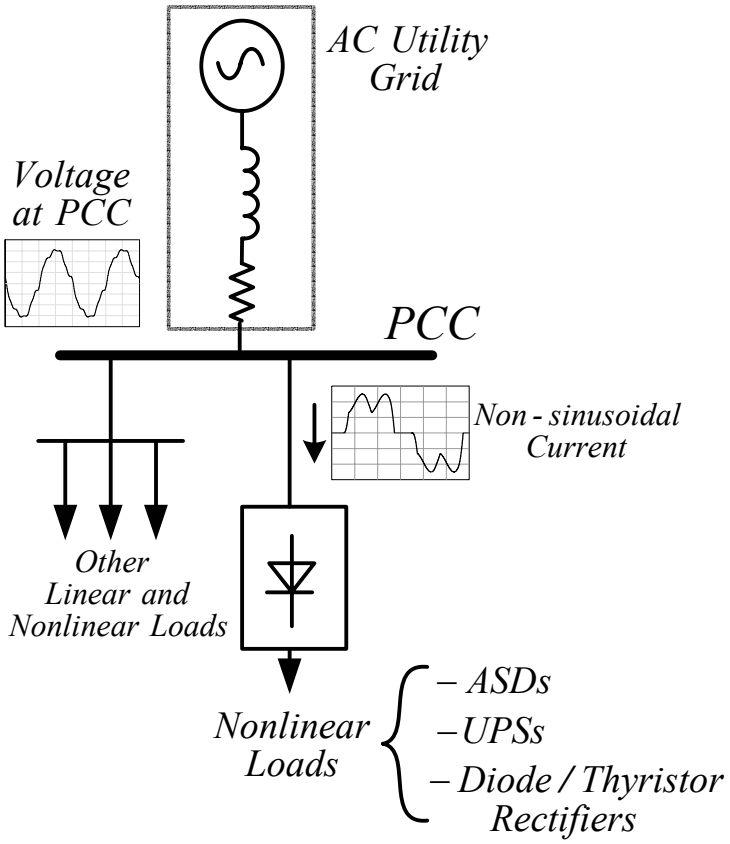

Figure 1.1 Definition of point of common coupling (PPC).

Harmonic currents result in not only voltage distortions at PCC, but also increase of RMS-value and peak-value of the line current causing addition losses, overheating and overloading, sometimes failure of power system equipments like capacitors, transformers and motors, frequent tripping of circuit breakers, and blowing of the fuses. Moreover, they can also cause interference with telecommunication lines, errors in power metering, and resonances in distribution systems, therefore power quality problems [3], [4]. Studies by the Canadian Electrical Association indicate that power quality problems are estimated to Canada about $1.2 billion annually in loss production [1]. This economic loss is an indication of the importance of the power quality for not only Canada, but also other countries. Although no detailed results have been reported about such issues in Turkey (to the knowledge of the author), it is well known that power quality problems are significant and result in large revenue loss and degradation in quality of life due to power line disturbances and interruptions. Therefore, these power quality problems are to be solved.

To alleviate harmonic related problems, recommended harmonic standards like EN61000-3-4 by IEC and IEEE 519-1992 by IEEE have been introduced and these standards have been regarded as a guideline for harmonic mitigation. For instance, the IEEE 519-1992 proposes limitations both for the customer and the utility side. In general, customers (end-users) are responsible for limiting the current harmonics caused by nonlinear loads utilizing power electronic circuits, while the utility is responsible for voltage harmonics at the PCC at distribution level. IEEE 519 proposes limits both for individual harmonic components and total distortion indices. To define the harmonic content of a waveform (or distortion level of a waveform), the term 'Total Harmonic Distortion (THD)' is used and can be applied to either voltage or current. The THD of current is defined as

$$THD_I = \frac{\sqrt{\sum_{h=2}^{h_{max}} I_h^2}}{I_1} \qquad (1.1)$$

where the I_h is the rms value of the current harmonic components and I_1 is the rms value of the fundamental current component. Similarly, the THD of voltage is defined as

$$THD_V = \frac{\sqrt{\sum_{h=2}^{h_{max}} V_h^2}}{V_1} \tag{1.2}$$

where V_h is the rms value of the voltage harmonic components and V_1 is the rms value of the fundamental voltage component.

The THD_I defining the distortion level can exhibit quite high (misleadingly, unacceptable) values for nonlinear loads operating under light load conditions. However, since the magnitude of harmonic components is low, this high THD_I value is not critical and the influence of the harmonic current on the PCC voltage distortion is insignificant. In order to avoid such misinterpretation, IEEE 519 defines the term Total Demand Distortion (TDD), which is given as

$$TDD = \frac{\sqrt{\sum_{h=2}^{h_{max}} I_h^2}}{I_L} \tag{1.3}$$

where I_h is the rms value of current harmonic h^{th} component and I_L is the rated rms value of the load current at fundamental frequency. This definition accounts for the loading effect of nonlinear loads. Therefore, the harmonic current limits proposed by IEEE 519 are expressed in terms of TDD rather than THD and are given in Table 1.1 for the customers. To define the TDD limits as well as individual harmonic current limits for customers having various utilization capacities, IEEE 519 uses the short circuit ratio (I_{SC}/I_L), which is the ratio of the short circuit current (I_{SC}) at the PCC to the rated current (demand current, I_L) of the customer, where the limits in Table 1.1 are expressed as percentages. As seen in Table 1.1, systems with low I_{SC}/I_L ratio (high impedance or weak distribution systems or customers with large capacity) are

bounded by lower distortion limits in order to keep voltage distortion at the PCC at reasonably low levels.

For the utility which is responsible for maintaining a power supply with low voltage harmonics at the PCC in distribution level, IEEE 519 proposes voltage THD limits as well as individual harmonic voltage limits shown in Table 1.2. The limits for voltage THD can have lower values than 5% for the special customers such as hospitals and airports operating at low voltage levels (e.g. 400Vrms) [3]. Although the utility should ensure these limits, the main reason for voltage distortion is the load current harmonic content passing through the impedance of power system. Therefore, customers injecting harmonics currents to the line should mitigate their own harmonics in order to comply with the recommended IEEE 519 limits for the high power quality of the system. Therefore, filtering for individual customers is mandatory for the mitigation of the injected harmonic currents to power system.

Until recently, power line harmonic standards such as IEEE-519 have been considered as technical references for the Turkish electric utility but neither enforced nor carefully studied in terms of their effects on the power system. The only harmonic study on the local harmonic pollution and local standards is reported in [5]. However, the recently established electric power regulation authority EMRA has established power quality guidelines which include harmonic limits that are almost identical to the IEEE-519 harmonic limits [6].

Table 1.1 IEEE 519 harmonic current limits

I_{SC}/I_{L1}	h<11	11≤h<17	17≤h<23	23≤h<35	35≤h	TDD (%)
<20	4.0	2.0	1.5	0.6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Table 1.2 IEEE 519 voltage distortion limits

Bus voltage at PCC	Maximum individual harmonic component (%)	Maximum THD (%)
69kV and below	3.0	5.0
69.001kV through 161kV	1.5	2.5
161.001kVand above	1.0	1.5

Besides the harmonic current problems and voltage distortion problems, reactive power flow is another power quality problem in a power system. Reactive current drawn by many linear/nonlinear loads connected to the PCC results in reactive power, which is a type of power that does no real work and is generally associated with the reactive elements in the system. Reactive power current component in the power system overloads the elements that it passes through and causes additional losses since it increases the RMS value of the line current [4]. Although there exist no international standards for reactive current unlike the harmonics drawn by the loads, many countries post limitations and monetary punishments to the end-users for the reactive power they draw. For instance, EMRA has limited the reactive power drawn by the customers directly connected to the transmission line (through a step down transformer) such that the maximum ratio of the inductive reactive power demand to the real power demand is less 0.25 and the maximum ratio of the capacitive reactive power demand to the real power demand is less than 0.15 as of January 1st, 2007. Customers exceeding these limits will be subjected to monetary punishments. These limits will be 0.14 and 0.1 for the inductive and capacitive reactive power respectively as of January 1st, 2009 [6]. The limits for customers feeding from the distribution system have wider limits of 0.33 inductive and 0.25 capacitive reactive power ratios currently. It should also be mentioned that single phase loads and loads with power rating of less than 9 kW are exempt from the reactive power penalty regulations [7]. As a summary, it can be stated that in particular industrial customers and large facilities have to limit the reactive power current component at their terminals as well as the harmonic current components.

1.2. Harmonic Mitigation Techniques

Harmonic pollution problems can be approached in two different methods. The first and most favorable approach is to utilize appropriate circuit topologies such that harmonic pollution is not created. Phase multiplying rectifiers (12-pulse rectifiers, 18-pulse rectifiers, etc.) for the nonlinear load with large power demand (several hundred kW and above), PWM rectifiers for regenerative ASD applications (typically less than a few hundred kW), and transformer-less UPS systems employing PWM rectifiers are the examples of applications utilizing circuit topologies creating low harmonic current content. In such cases either a small distortion remains and requires small capacity filtering equipment or no additional filtering is required at all.

The second approach involves filtering and this approach is utilized in standard six-pulse rectifiers which have significant harmonic distortion, phase multiplying rectifiers for compensation of the remaining dominant harmonics, and other nonlinear load applications. These loads make the larger percent of industrial loads and involve power ratings from several kW to multi MW range. Harmonic filtering techniques are generally utilized to reduce the current THD and filters based on these techniques are classified in three main categories:

1. Passive filters
2. Active filters
3. Hybrid filters

The traditional harmonic mitigation technique is the passive filtering technique. The basic principle of passive filtering is to prevent harmonic currents from flowing trough the power system by either diverting them to a low impedance shunt filter path (parallel passive filter) or blocking them via a high series impedance (series passive filter) depending on the type of nonlinear load. Passive broadband filters employ the duties of series and parallel passive filters via a combination of them. Traditional passive filters have been preferred over other methods for harmonic mitigation for years due to their simplicity, low cost, and high efficiency.

Parallel tuned passive filters, which are the most commonly utilized type, present a low impedance path so that the load current harmonics are diverted to the filters rather than the AC line. Tuned filters offers very low impedance path at the frequency of tuning. Therefore, each tuned filter sinks the harmonic current at its tuning frequency. As a result, if the number of dominant harmonic components to be sinked increases, the filter size increases considerably. Tuned filters also have the additional function of power factor correction of inductive loads. However, they have several significant drawbacks. The supply impedance affects the compensation characteristics of the filter and it is likely that series and/or parallel resonant with utility and/or load will be invoked. Moreover, in order to prevent the shunt passive filter from sinking harmonic currents from ambient loads, they are usually off-tuned. In this case, the filtering capacity for the stiff utility grid (low system impedance utility) degrades. Therefore, passive filter designs require excessive system studies, relatively high engineering effort, and cost.

The basic principle of active filters was established around 1970s [8], [9]. However, the idea could not become technologically and economically feasible until the last two decades when fast and cost effective semiconductor devices such as Insulated Gate Bipolar Transistors (IGBTs) and MOSFETs, and high performance and cost effective Digital Signal Processors (DSPs) became available. Moreover, the advances in control theory and application of modern control methods in power electronics have played a significant role in the practical realization and commercial success of active filters. Modern active filters are superior in filtering performance since the basic principle of the active filter is to precisely inject to the system voltage/current harmonics of nonlinear loads with same magnitude and opposite sign so they cancel each other and clean waveforms are obtained at the power line. Active filters are also smaller in physical size and unlike traditional passive filters they have additional functions to harmonic filtering. They form effective solutions to many power quality problems. Depending on the active filter type, controllable reactive power compensation for power factor correction, voltage regulation, load balancing, voltage-flicker reduction, harmonic damping, harmonic isolation and/or their combinations could be provided. Although active filters are superior in filtering

performance and functionality variety, their application is generally limited to several MW levels and typically below a megawatt. For higher power ratings they generally suffer from the high cost due to their large VA ratings and operating losses.

Hybrid filters combine passive and active filters in various configurations in order to reduce initial cost and increase the efficiency of the filter structure. The basic principle of hybrid filtering is to improve the filtering capacity of a passive filter and to damp series and parallel resonances with a small rated active filter. However, the functionalities of hybrid filters are limited compared to pure active filters and they involve higher engineering effort than passive filter design [2], [4], [8], [9], [10].

The choice of filtering solution for harmonic mitigation is mainly cost dependent, and leads to different filter types for different kVA levels. In [9], a comparison study for the cost of filtering solutions including system engineering and study cost has been carried out as a function of kVA rating of harmonic producing loads. The cost of active filters is lower than other methods for nonlinear loads up to 1 MVA rating. Above this rating, the cost of active filters increases exponentially, where hybrid filters become cost-effective solutions up to 30 MVA ratings of non-linear loads. At higher ratings, passive filters become a viable choice. The above discussion illustrates that active filters are viable choice for low-power applications and they offer solutions to various power quality problems with their various functionalities besides their harmonic current compensation.

1.3. Active Filters

The increased severity of the harmonic pollution in power systems over the last couple of decades has lead the power electronics engineers to develop high performance solutions to power quality problems created by power electronic circuits. This technological development for power quality problems involves active filters. With various successful circuit topologies and control strategies, active filters are capable of not only harmonic current compensation, but also reactive power, negative sequence current and neutral wire current (zero sequence current)

compensation. Active filters are also utilized to suppress voltage harmonics and voltage flickering, regulate load terminal voltages, balance voltages in a power system, and damp resonances. Active filters can be parallel (shunt) type, series type, and combination of both depending on the type of nonlinear loads and the required functionalities [10], [11].

The Parallel Active Filter (PAF), shown in Figure 1.2, is the earliest and most recognized active filter configuration in the technical literature and it has been utilized in practical applications. Due to the parallel connection to the load, it is also termed as shunt filter. PAF is controlled as a current source and it is utilized to inject a compensating current into the system (to the load), so that its current cancels the harmonic current, the reactive power current and the unbalanced current components on the AC side of a nonlinear load. When it is employed to three-phase four-wire systems, PAF also has the capability of compensating the neutral current (zero sequence current) component. Therefore, with the application of PAF, the current drawn form utility grid becomes harmonic free, balanced, and in phase with utility voltage, and zero-sequence free in three-phase four-wire systems. The nonlinear load in the PAF application shown in Figure 1.2 is presented as a general purpose thyristor rectifier with DC link inductor for illustration. In fact, PAF is suitable and generally employed for diode/thyristor rectifiers with AC and/or DC side inductors. Such rectifier loads generally constitute the front-end circuits of systems such as ASDs and UPSs, which behave as harmonic current generator/source nonlinear loads (inductive loads) [12], [13]. PAF also has the capacity of damping harmonic resonance between an existing passive filter and the supply impedance. Although it is shown for three-phase circuit in Figure 1.2, PAF can be employed for single-phase nonlinear loads.

The parallel active filtering technology is well matured and the PAF performance attributes are attractive such that many leading power electronic companies manufacture PAFs. ABB [14], Meidensha [15], MGE [16], AIM [17], Nokian [18], and Staco [19] manufacture PAFs complying with the harmonic standards of IEEE 519 and EN61000-3-4 for the industrial and domestic applications. With ratings of

10 kVA to 300kVA, and paralleling capability (which allows higher ratings), most such PAF products offer adjustable harmonic mitigation up to the 50^{th} harmonic, and adjustable reactive power and negative sequence current compensation. While most PAF products are for 3-phase and 3-wire applications, PAFs for 3-phase and 4-wire systems are also in the market and utilized for wide range of applications.

The basic system configuration of Series Active Filter (SAF) is shown in Figure 1.3. Controlled as a voltage source, SAF is connected before the nonlinear load in series with utility grid through a coupling transformer to isolate the harmonics voltages and to balance and regulate the terminal voltages of the nonlinear load. Moreover, SAF is utilized to isolate the customer from power quality problems of the utility. By injecting a voltage component with utility, SAF compensates the voltage sags, swells and flickers. It is also utilized to damp out harmonic resonances and improve the filtering performance of the passive filters connected between SAF and nonlinear load. The nonlinear load in SAF application shown in Figure 1.3 is presented as a general purpose diode rectifier with a DC link capacitor for illustration. In fact, SAF is suitable and generally employed for the nonlinear loads which behave as harmonic voltage generator/source loads (loads with the front-end circuits of diode/thyristor rectifiers with DC side capacitors and end terminal loads) [12], [13]. SAF can also be employed for single-phase nonlinear loads as in the PAF case. If the operating and application principle of SAF is compared to PAF, these two active filters have a dual relationship with each other.

In order to combine functionalities of PAF and SAF, two systems can be connected back-to-back. Such as system is named as Unified Power Quality Conditioner (UPQC) and illustrated in Figure 1.4. The system can be considered as an ideal active filter which eliminates all the power quality problems with the utility and nonlinear load. While the PAF part compensates the harmonics current, reactive power current, and unbalanced current components of a nonlinear load, the SAF part suppress the voltage harmonics, sags, swells and flickers, and balances and regulates the load terminal voltages. Since UPQC provides clean power, the customers can apply it to their own critical and power quality sensitive loads such as computers,

medical equipments, etc at low voltage distribution voltage level (named as 'specific UPQC'). Moreover, it is applied by the utility at medium voltage distribution levels between subtransmission systems and distribution systems with the same functionalities above (named as 'general UPQC') [13], [20]. The main drawback of UPQC is its cost and control complexity as this system proposes a challenging control problem.

Customers select the type of active filters depending on the performance requirement on the utility grid connected side. PAF is a good candidate for applications involving inductive load type with low line current THD requirements, applications involving the harmonic resonance risk, applications requiring very dynamic loads involving dynamic reactive power compensation, applications with sensitive loads connected to the same PCC. In these cases the PAF rating is selected to meet the power quality standards enforced in the specific power grid. In such applications SAF is not preferred due to its form and functionalities, not to mention its high cost and complexity. In fact, while PAF has been in the market for longer than a decade, SAF is still a not common product and only is utilized in specific applications. This thesis focuses on PAF which will be discussed in further detail in the following.

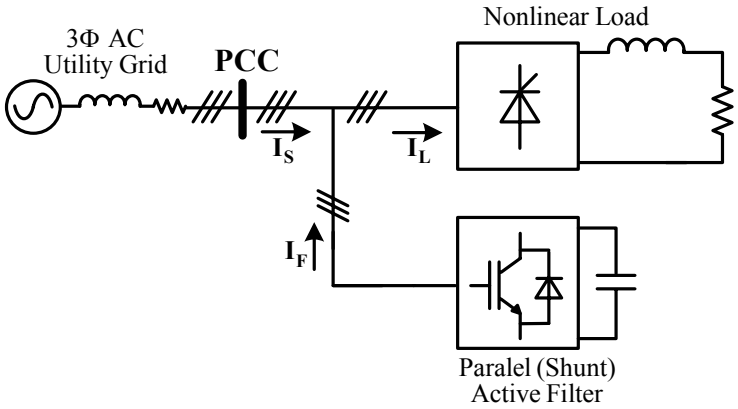

Figure 1.2 The parallel (shunt) active filter.

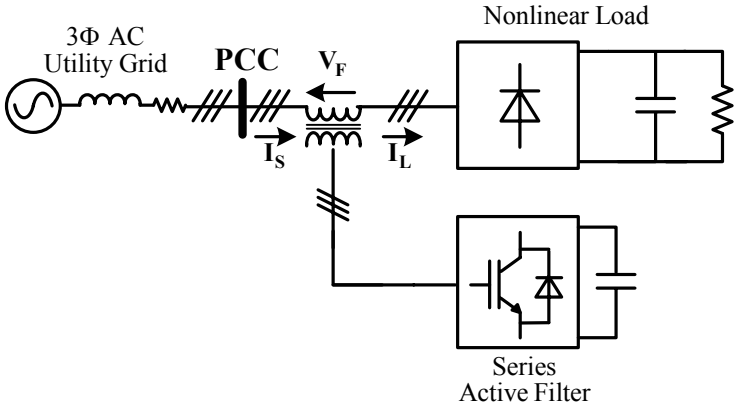

Figure 1.3 The series active filter.

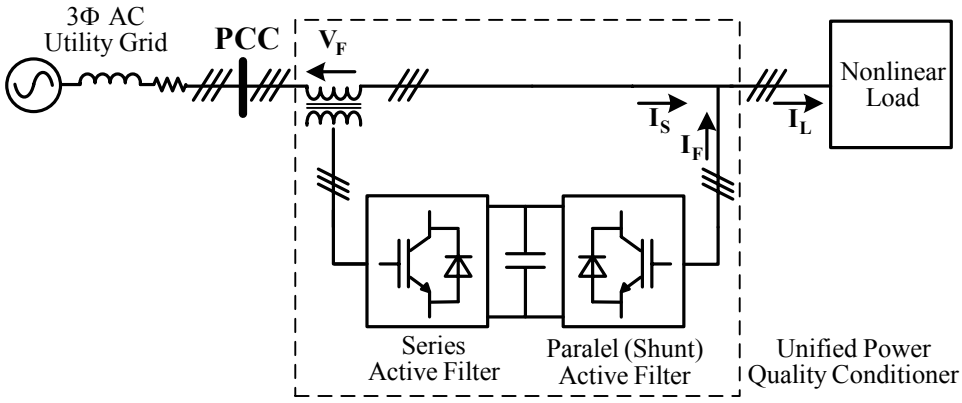

Figure 1.4 The combination of parallel and series active filter:
unified power quality conditioner.

1.4. The Parallel Active Filter (PAF)

Implemented as a harmonic current source, PAF compensates the harmonic currents of nonlinear loads. As shown in Figure 1.5, the controller of the PAF system detects the instantaneous load current, extracts its harmonics content, and injects the compensating harmonic currents to cancel the load harmonic currents. As a result, a sinusoidal current is drawn form the utility grid. Since the parallel active filter is implemented as a controlled current source, depending on the control strategy, in addition to compensating the harmonics, it can also compensate the reactive power

current component, the load current negative sequence component, and neutral wire current in 3-phase 4- wire systems.

To realize a current source for three-phase three-wire PAF, shown in Figure 1.6, two power electronic circuit topologies are available. Figure 1.6.a illustrates a Pulse Width Modulation (PWM) Voltage Source Inverter (VSI) with a dc bus capacitor and Figure 1.6.b illustrates a PWM Current Source Inverter (CSI) with a dc link inductor. The VSI utilizes IGBTs with anti-parallel diodes, which are available in market, while CSI utilizes IGBTs with series connected diodes for reverse-blocking capability, which have higher conduction and switching losses than IGBTs with anti-parallel diodes. Moreover, the dc link inductor for the CSI makes the inverter more bulky and costly compared to the DC bus capacitor for the VSI. The protection circuitry for CSI is more complicated than the one of VSI. Therefore, VSIs are more efficient, more cost-effective, and smaller in size compared to CSIs [10], [21]. In PAF applications, a current source is realized via current-controlled mode operation of the PWM-VSI connected to the AC utility grid at the PCC with coupling inductors on the AC side. The connection diagram of the PWM VSI for three-phase three-wire PAF is illustrated in Figure 1.7.

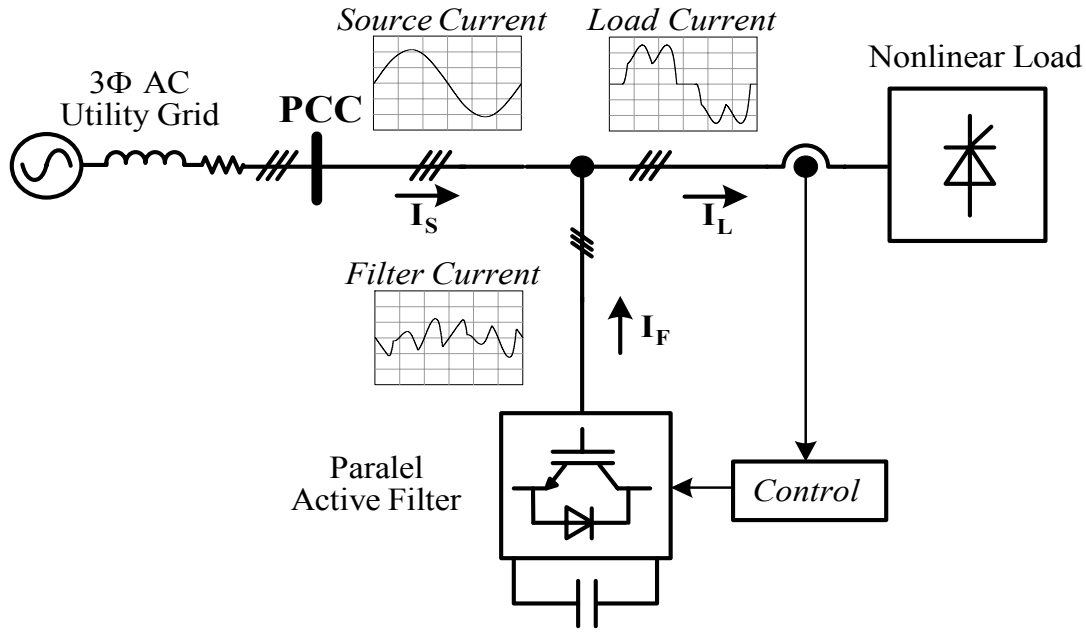

Figure 1.5 PAF implemented as a harmonic compensating current source.

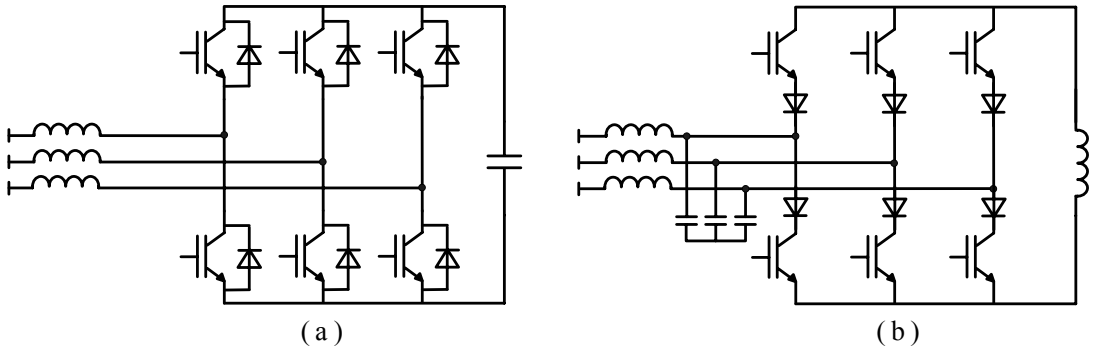

Figure 1.6 The power electronic circuit topologies for 3-phase 3-wire PAF: a) PWM voltage source inverter, b) PWM current source inverter.

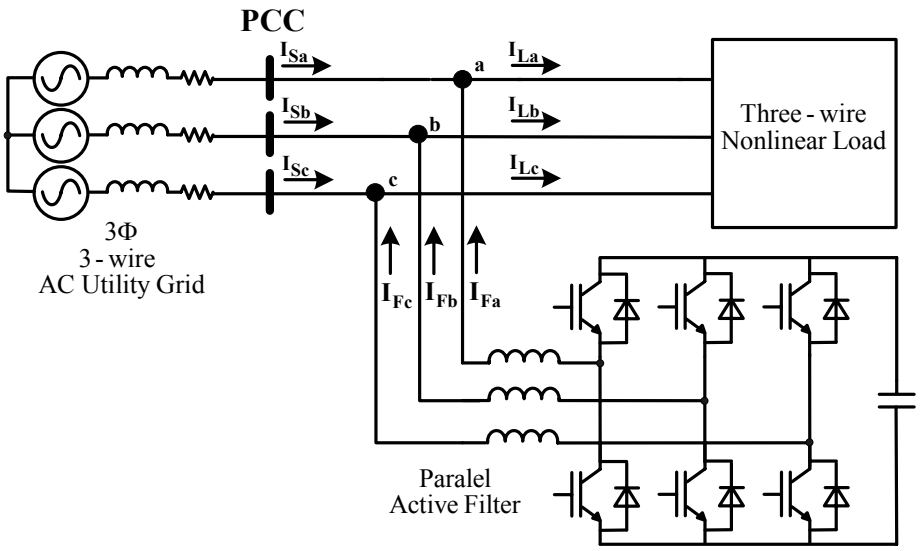

Figure 1.7 The connection diagram of the PWM VSI for 3-phase 3-wire PAF.

The PAF employing system illustrated in Figure 1.7 is applied to three-wire three phase nonlinear loads in high power applications such as ASDs and UPSs. However, there exist single phase nonlinear loads (computers, ballasts, single phase UPSs, and etc.) supplied from 3-phase 4-wire AC utility grid in low voltage distribution systems. In these systems, the neutral wire current may have nearly three times higher rms value than the rms value of the phase currents and the neutral wire and the distribution transformers may be overloaded. To avoid these problems in such systems, 3-phase 4-wire PAF topologies are utilized at the entrance of the factory or

large office building needing such compensation. Figure 1.8 illustrates 4-leg PWM VSI PAF utilized in 3-phase 4-wire PAF systems to compensate the nonzero sequence harmonic currents as well as the neutral wire current which includes the fundamental and triplen harmonic zero sequence currents. Harmonic current free AC utility grid neutral wire current is achieved with increased rating of PAF. Having an extra leg leads to 16 possible switching combinations and makes the control of the topology challenging. Another topology utilized in 3-phase 4-wire PAF applications is the capacitor midpoint connected half-bridge inverter, illustrated in Figure 1.9. The fourth wire of PAF is connected to the midpoint of DC bus capacitors. Since the neutral current flows trough the DC bus capacitors, the topology requires larger capacitor size compared to the previous one. Also the switching losses are higher due to the larger DC bus operating voltage of the topology. A comparison study is carried out in [22] for various 3-phase 4-wire PAF topologies. Although the 3-phase 4-wire PAFs are more suitable for residential and office type environments involving single phase nonlinear loads in low voltage distribution system, a large number of industrial loads with large power ratings feed from three-phase three-wire AC utility grid. Therefore, the 3-phase 3-wire PWM VSI based PAF shown in Figure 1.7 is widely utilized in such applications [10], [11], [13], [23]. This thesis focuses on the 3-phase, 3-wire PAF topology.

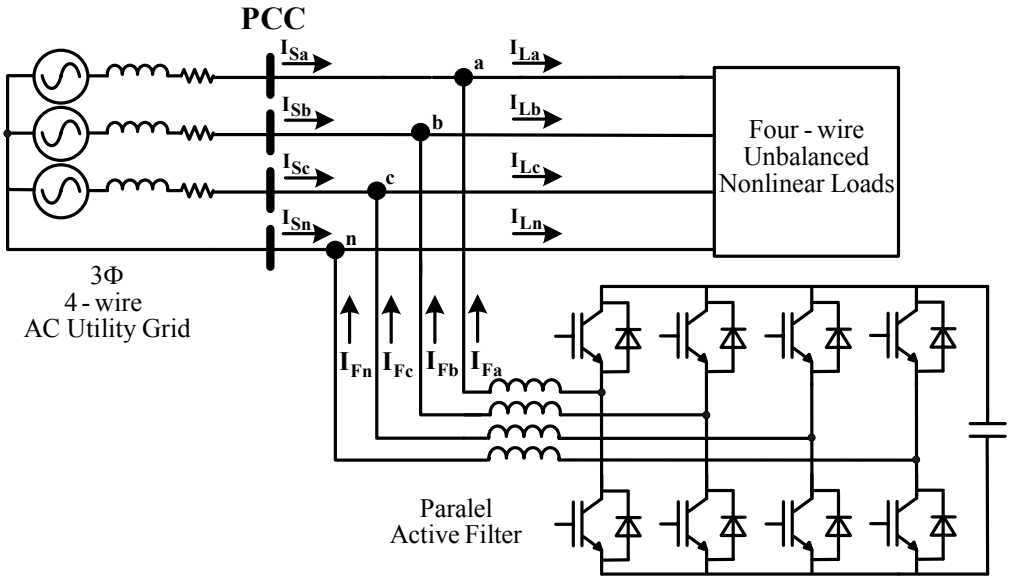

Figure 1.8 Three-phase four-leg VSI based PAF for 3-phase, 4-wire applications.

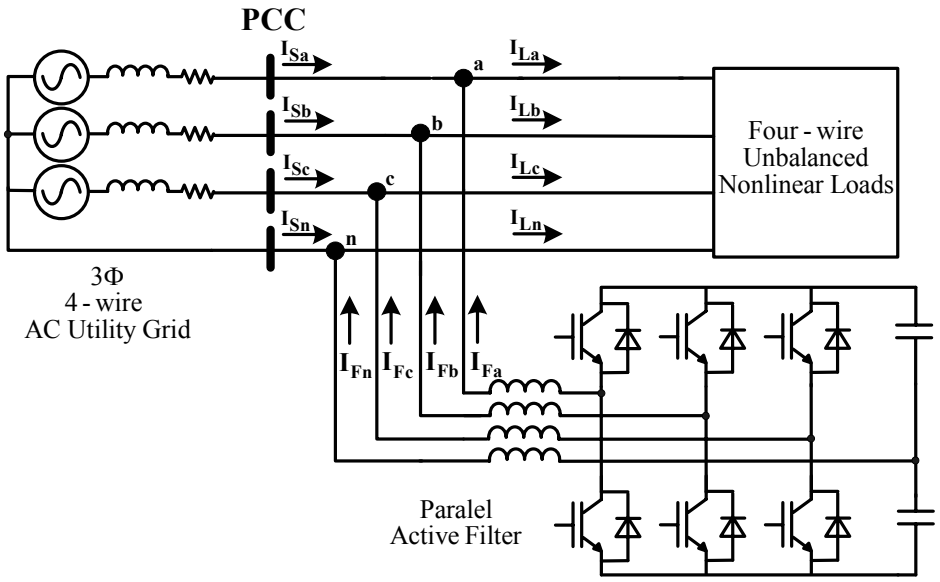

Figure 1.9 Half-bridge PWM-VSI based 3-phase, 4-wire PAF topology.

Given the power electronic converter topology, the aim of the PAF control system is to measure the distortion and provide a compensation such that the power quality is enhanced. Since the PAF converter is operated as a controlled harmonic current source, the controlled variable is the PAF current and proper extraction of its reference value (reference current, I^*_F) is critical for the PAF performance. Summarized in the following, three harmonics current reference extraction (harmonic detection) methods have been proposed [13], [24].

- Load current detection such that $I^*_F = I_{Lh}$, where I_{Lh} is the load current harmonic
- Utility current detection such that $I^*_F = K_I \cdot I_{Sh}$, where I_{Sh} is the utility current harmonic
- Utility voltage detection such that $I^*_F = K_V \cdot V_{Fh}$, where V_{Fh} is the utility voltage harmonic

The utility voltage detection method is suitable for PAFs if they are implemented by the electric utilities for the purpose of voltage harmonic damping at a distribution feeder. However, the load and utility current detection methods are suitable for PAFs implemented for the purpose of the harmonic current compensation by the individual

customers. The load current detection method is commonly preferred and has become a standard in many products installed for individual high-power consumers [10], [13], [14], [15], [16], [17], [18], [19], [23], [24].

The general system block diagram of the PAF operated in current-controlled mode is illustrated in Figure 1.10. The control system of PAF consists of two main blocks; current reference generator and current controller. The detected load currents are sent to current reference generator block to obtain the harmonic current reference. The PCC terminal voltages are measured as they are necessary for harmonic current extraction. Another measured control variable is the DC bus voltage of PAF, which is necessary to hold DC bus voltage at its desired value. For this purpose, a current reference different from the harmonic current reference is created for DC bus regulation. Moreover, if the reactive power and negative sequence current components of the nonlinear load are to be compensated via PAF, the current reference generator is adapted such that current reference for PAF includes these components. Since PAF is controlled as a current source, the current reference should be generated accurately for high performance compensation.

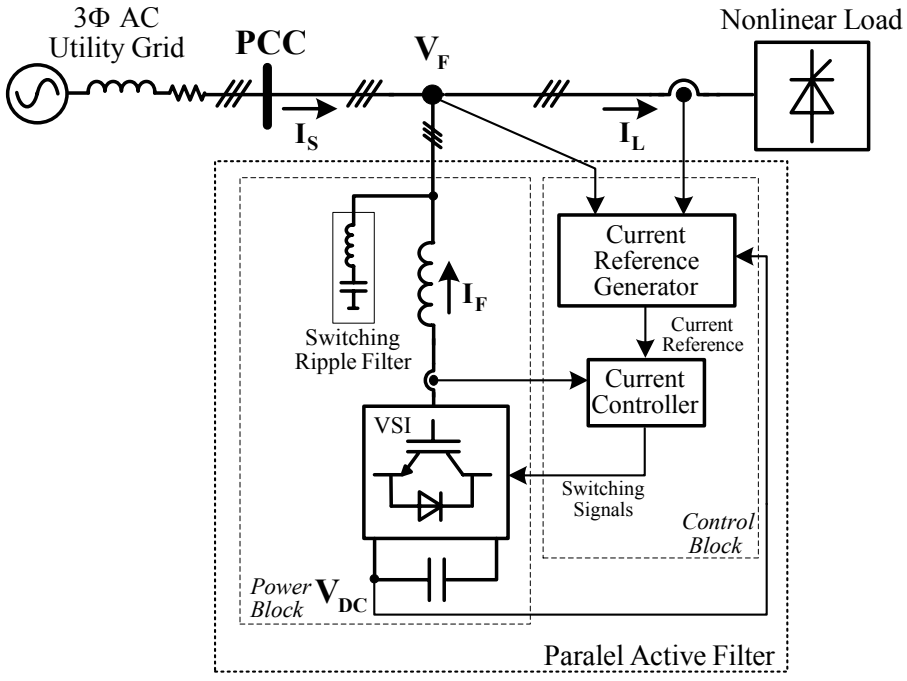

Figure 1.10 General system block diagram of the PAF.

The generated PAF current reference is sent to the PWM-VSI current controller, which is the other main block of the PAF control system. The current controller takes the feedback signal of PAF current and the reference current and it creates switching signals to VSI for the regulation of the PAF current. PAF current control is the most challenging task among the PAF control algorithms since the PAF current reference is characterized by its non-sinusoidal multiple frequency content and high di/dt. In order to meet the stringent power quality harmonic standards (Table 1.1), PAF should compensate for wide range of harmonics, which requires a current controller with high bandwidth and resolution. Therefore, the current controller is the most critical part of the PAF control algorithm and should be designed properly for a better current tracking. The technical literature involves too many proposed current controller types for the PAF application. However, a current controller choice suitable for the PAF application involves a detailed comparison of current controllers in terms of the current tracking capability, implementation simplicity, and efficiency.

The generated switching signals by the current controller are sent to semiconductor devices involved in the VSI. The PWM-VSI chops the DC bus voltage by the PWM technique to obtain the desired AC voltage at the output terminal for the creation of the PAF current through the filter coupling inductors. As a result, the compensating current is obtained to achieve a harmonic free utility grid current. Figure 1.10 also shows a Switching Ripple Filter (SRF) to sink the high frequency switching harmonics created by the VSI. SRF is mandatory in this application since the PAF is directly connected to utility grid and high frequency voltage pulses created by VSI result in high frequency distortion on the PCC voltage [10], [13], [23]. High frequency voltage distortion at PCC creates noise problems for the utility grid and other customers connected to the same PCC. Therefore, adequate attenuation of switching frequency harmonics via SRF is critical from the point of view of power quality, and this issue makes its design as important as the design of PAF current controller. Although the SRF topologies in the PAF application are well known, the technical literature lacks detailed SRF design guidelines and comparisons of SRF topologies.

In summary, PAF is a high performance, efficient, and economical means of filtering and it has found wide range of applications. Its technology has been maturing and its applications have been rapidly broadening over the last decade. However, the research and development work related to this technology has not reached saturation level and progress has been continuing. This thesis involves design, control, and implementation of 3-phase, 3-wire PAF and in the following the focus of the thesis will be discussed in detail.

1.5. Scope of The Thesis

This thesis is dedicated to detailed analysis, design, control, and implementation of a 3-phase 3-wire PAF with the main application being the harmonic current and reactive power compensation of 3-phase rectifier load, which is the most commonly utilized industrial nonlinear load. In the following the thesis scope and outline will be provided.

This thesis has four main contributions. The first contribution involves the thorough analysis, design, hardware construction, and laboratory experiment of a PAF for 10 kW rectifier load. Therefore, this thesis provides a design and implementation guideline for PAF design engineers.

The second contribution involves the development of a new current control method which has a simple structure and exhibits superior performance characteristics when compared to the methods known in the literature. In the thesis, this current regulator is described, analyzed, and its performance evaluated.

The third contribution of the thesis involves performance comparisons among various high performance current regulators for the PAF application, including the above mentioned new current regulator. With thorough performance comparisons, it is illustrated some regulators are favorable not only in terms of performance, but also simplicity while others have not been found useful. Therefore, the study provides a current regulator selection and implementation guide for the PAF design engineers.

The final main contribution of the thesis involves the switching ripple filter design for PAF applications. Since there is no detailed literature regarding the SRF design, a study of SRF topologies and their parameter design rules has been conducted and the research results are reported here for the purpose of proper selection and sizing of SRFs for the PAF application.

The organization of this thesis is given as follows. The second chapter involves a system level study of PAF. It thoroughly reviews the operation principle of the PAF implemented as a current source, provides the theoretical analysis of the filtering performance, discusses the suitable load characteristics, and reviews the basic control blocks in the PAF system. The general characteristics of the nonlinear loads and the application consideration of the PAF to these loads are investigated in detail. The control blocks of the PAF operated in current controlled mode are analyzed in detail. The harmonic reference generator block is analyzed with the case studies to provide a full understanding of the reference current generation issue in the PAF application. Moreover, a theoretical PAF rating analysis is carried out.

The third chapter is dedicated to current control (regulator), which is the most critical part of PAF. A detailed literature survey is carried out for suitable current regulators for the PAF application. The current regulators applicable in practice and their design issues and implementations are investigated in detail. Moreover, a novel discrete time hysteresis current regulator with multirate sampling and flexible PWM output showing superior tracking performance in the PAF application is proposed.

The fourth chapter analyzes the switching ripple filter topologies for a PAF application and provides analytical design rules for these topologies with the current regulation methods taken into consideration. A comparison study is carried out in terms of the performance, size, cost, and efficiency of the analyzed topologies.

In the fifth chapter, the computer simulation results of the designed PAF for harmonic current compensation of 10 kW diode rectifier are presented. The performance of the PAF system is verified and the performance of various current

regulators analyzed in Chapter 3 is illustrated. The proposed discrete time hysteresis current regulator is investigated by means of computer simulation. Moreover, a comparison study for the implemented current regulators is carried out in terms of their current tracking capability, implementation simplicity, and efficiency. The performance of the designed SRFs for two general types of current regulators is investigated. Following the part by part performance study of the system, the system overall performance is investigated for two load types. First the detailed steady-state and dynamic performance of the designed PAF system is provided for a 10kW diode rectifier. Second the current tracking, reactive power compensation, and the negative sequence current compensation capability of the designed PAF system is illustrated for a 10 kW thyristor rectifier.

The sixth chapter summarizes the manufacturing process and the experimental results of the PAF designed for harmonic current and reactive power compensation of a 10 kW diode rectifier. First, the hardware and the software implementation of the PAF prototype are explained in detail. Then, the experimental results, which show the performance of the PAF for various current regulators are presented. The performance of the proposed current regulator is analyzed in detail and a comparison study is carried out. Also the experimental performance of the designed and manufactured SRFs is evaluated and PAF performance comparison with and without SRF is provided. The experimental steady-state and dynamic performance of the manufactured PAF system applied to the diode rectifier is investigated in detail. Finally, the reactive power compensation of a 10 kW thyristor rectifier is achieved experimentally by the manufactured PAF. Throughout this chapter, experimental results are evaluated in comparison with the simulation results of the previous chapter in the same order. The strong correlation between the computer simulations and experiments is verified.

The final chapter summarizes the contributions of the thesis, provides the concluding remarks, and recommends future work.

CHAPTER 2

THE PARALLEL ACTIVE FILTER SYSTEM

2.1 Introduction

This chapter studies the parallel active filter (PAF) system. The PAF, the load it compensates, and the power system both units are connected result in a complex system. The success of the PAF as a compensator depends on the PAF control algorithm as well as the load type. Although the PAF is normally designed as a controlled current source type compensator, if the load it compensates does not have a current sink type characteristic, the success of the compensation may be unsatisfactory. Therefore, the characteristics of the load and the PAF are important and must be well understood.

This chapter is dedicated to the general features of the PAF in harmonic current, reactive power current component, and negative sequence current component compensation of nonlinear loads. First the characteristics of nonlinear loads and the application of PAF implemented as current source to different types of nonlinear loads are investigated. The control architecture of PAF with its main blocks, which allows the realization of PAF as controlled current source is analyzed. In this chapter also a theoretical power rating analysis of the parallel active filter is carried out.

2.2 Characteristics Analysis and Application Consideration of The Parallel Active Filter

2.2.1 Harmonic Producing Nonlinear Loads

In order to understand the characteristics and application considerations of the parallel active filter, it is important to discuss the general characteristics of nonlinear loads. Since many industrial loads with high VA ratings feed from 3-phase 3-wire AC utility grid and have 3-phase diode/thyristor rectifier (or known 6-pulse rectifiers) front-end topologies, the discussion will be on the characteristics of 3-phase diode/thyristor rectifiers as nonlinear loads. As it is well-known, these loads are sources of either harmonic currents or harmonic voltages. Therefore nonlinear loads are discussed in two categories: harmonic current source type nonlinear loads and harmonic voltage source type nonlinear loads. Figure 2.1.a illustrates a typical 3-phase thyristor rectifier with a dc side inductance and a resistor. Due to the sufficient inductance value at its DC side, it produces nearly constant DC current. The harmonic current content of the rectifier input current (load current) is less dependent on the ac side with a typical THD_I value of 25-30% (Figure 2.1.a). Therefore, this type of load behaves like a current source, and called as harmonic current source type nonlinear load (stiff current source type nonlinear load). However, as shown in Figure 2.1.b, a diode rectifier with sufficient smoothing dc capacitors is an example of harmonic voltage source type nonlinear load. Although the harmonic content of the rectifier input current is affected by ac side impedance and highly distorted (typically THD_I>70%), the voltage at the input terminals of the rectifier (Figure 2.1.b) is less dependent on the AC side. Therefore these types of nonlinear loads behave like a voltage source rather than a current source, so called harmonic voltage source type nonlinear loads. Based on the above discussion, the per-phase equivalent circuit of a harmonic current source type nonlinear load can be represented as Norton's equivalent circuit as shown in Figure 2.2.a and per-phase equivalent circuit of a harmonic voltage source type nonlinear load as Thevenin's equivalent circuit as shown in Figure 2.2.b. The pure harmonic current source is a special case of Norton's equivalent with $Z_L \to \infty$ and the pure harmonic voltage source is a special

case of Thevenin's equivalent with $Z_L \to 0$ [12], [13]. The subscripts, h and f, in Figure 2.2 and in the rest of figures and equations in this thesis represent harmonic component and fundamental component of the mentioned quantity respectively.

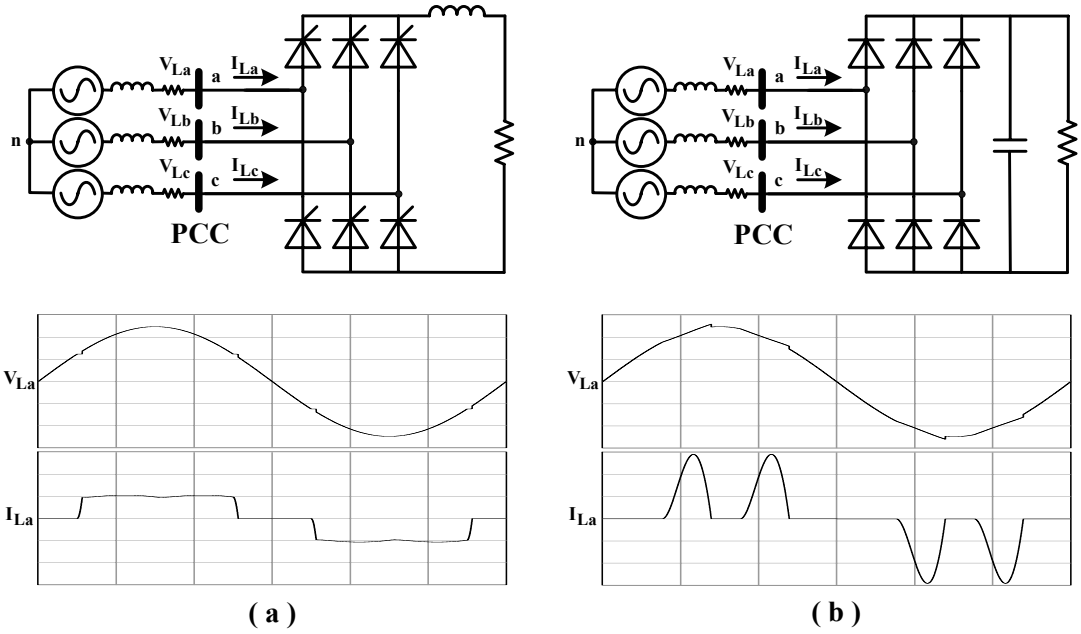

Figure 2.1 Typical 3-phase nonlinear diode rectifier loads and their input waveforms: a) 3-phase thyristor rectifier with a DC side inductor, b) a diode rectifier with sufficient smoothing DC capacitor.

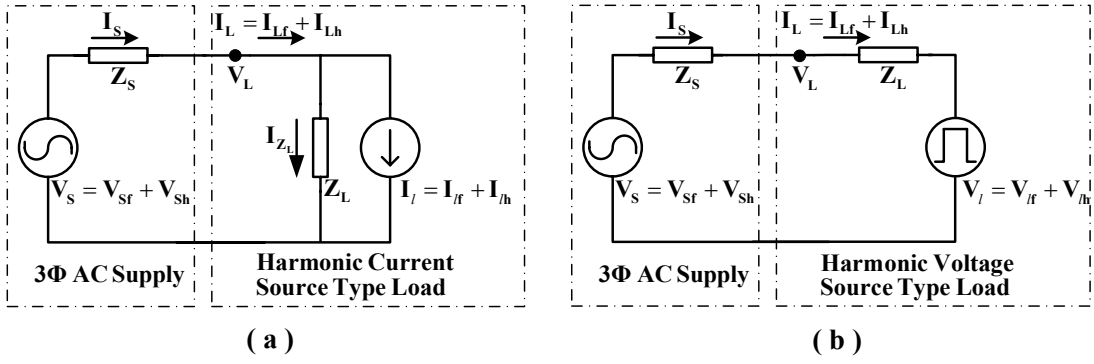

Figure 2.2 Per-phase equivalent circuit model of rectifier type nonlinear loads: a) harmonic current source type nonlinear load represented as Norton's equivalent, b) harmonic voltage source type nonlinear load represented as Thevenin's equivalent.

2.2.2 Parallel Active Filter for Harmonic Current Source Type Nonlinear Loads

Figure 2.3 illustrates the application of the PAF to harmonic current source type nonlinear load represented Norton's equivalent circuit. The current source, I_l, and the parallel impedance Z_L represent the equivalent current source. I_L is the total current drawn by the load. The 3-phase AC supply is represented as a voltage source, V_S, and supply impedance, Z_S. Since the aim of the PAF is to compensate load current harmonics to provide sinusoidal line (supply) current, the PAF is implemented as a harmonic current generator, which generates harmonic currents equal in magnitude and opposite in phase to that of the load current harmonics. Thus the PAF in the figure is represented as a current source of I_F. The filter current is defined by the following equation,

$$I_F = G(s)I_L \tag{2.1}$$

where *G(s)* is the transfer function of the PAF. By circuit analysis, the line current I_S and the total load current I_L are given as in (2.2) and (2.3) respectively.

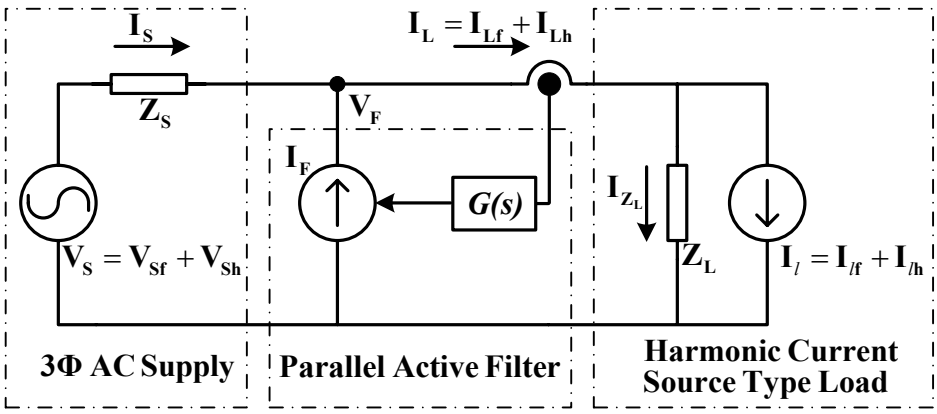

Figure 2.3 Application of the parallel active filter to a harmonic current source type nonlinear load which is represented as Norton's equivalent.

$$I_S = \frac{Z_L}{Z_S + \frac{Z_L}{1-G(s)}} I_l + \frac{1}{Z_S + \frac{Z_L}{1-G(s)}} V_S \tag{2.2}$$

$$I_L = \frac{\frac{Z_L}{1-G(s)}}{Z_S + \frac{Z_L}{1-G(s)}} I_l + \frac{1}{(1-G(s))\left(Z_S + \frac{Z_L}{1-G(s)}\right)} V_S \tag{2.3}$$

In an ideal PAF, *G(s)* is equal to zero at fundamental frequency ($|G(s)|_f = 0$) and approximately equal to unity at all harmonic frequencies, $|G(s)|_h \approx 1$. Therefore *G(s)* is assumed to have a characteristic of a notch filter at the fundamental frequency. If the condition given by

$$\left|\frac{Z_L}{1-G(s)}\right|_h >> |Z_S|_h \tag{2.4}$$

is satisfied for the harmonic frequencies, Equations (2.1), (2.2) and (2.3) can be written as

$$I_F \cong I_{Lh} \tag{2.5}$$

$$I_{Sh} \cong (1-G(s)) I_{lh} + \frac{1-G(s)}{Z_L} V_{Sh} \cong 0 \tag{2.6}$$

$$I_{Lh} \cong I_{lh} + \frac{1}{Z_L} V_{Sh} \tag{2.7}$$

Equation (2.5) shows that the active filter current is approximately equal to the load harmonic currents and (2.6) implies that line current becomes harmonic free because of $|1-G(s)|_h \approx 1$ if the condition in (2.4) is satisfied. Therefore, (2.4) is the required condition for the PAF to compensate the load current harmonics and to provide sinusoidal line current. Moreover, (2.7) implies that the active filter current does not

flow through the load impedance (Z_L). Satisfying the condition requires that Z_L should be large compared to Z_S and $|1\text{-}G(s)|_h << 1$. This condition also shows that performance of the PAF is determined by the system parameters Z_L and Z_S, and the PAF transfer function *G(s)* which is the design parameter. As Z_L increases compared to Z_S, harmonic compensation increases. The compensation characteristics of the PAF seem to depend on the supply impedance and load impedance magnitudes. However, when it is applied to a pure harmonic current source type nonlinear load, PAF cancels the load current harmonics since $Z_L \rightarrow \infty$. Moreover, the condition is also satisfied for harmonic current source type nonlinear loads such as thyristor controlled nonlinear loads with a sufficient dc side inductance since $| Z_L | >> | Z_S |$. For such nonlinear loads, (2.2) and (2.4) can be reduced to (2.8) and (2.9) respectively

$$\frac{I_S}{I_l} = 1 - G(s) \tag{2.8}$$

$$\left|1 - G(s)\right|_h << 1 \tag{2.9}$$

Equation (2.8) implies that compensation characteristics of PAF are not influenced by the supply impedance Z_S and only determined by the PAF transfer function as given by (2.9) as long as the condition $| Z_L | >> | Z_S |$ is satisfied. This is the reason that the PAF is suitable for harmonic current source type nonlinear loads. In general, the value of $|1\text{-}G(s)|_h$ ranges between 0.1 and 0.3 for different frequencies depending on the harmonic current detection circuit and extraction, control circuit, switching frequency, and DC bus voltage of PWM inverter. Therefore, the compensation rate of the PAF for harmonic currents obtained (2.9) as a percentage ranges between 70% and 90% and is fully determined by the PAF implementation.

Another important consideration is that if a parallel passive filter or a power factor correction capacitor is connected in front of harmonic current source type nonlinear load, the condition $| Z_L | >> | Z_S |$ may not be satisfied since the load impedance Z_L may be low at the harmonic frequencies. In this case, the compensation

characteristics of the PAF will also depend on the supply impedance Z_S. Therefore special considerations and control algorithms are required for a PAF utilized in such cases [12], [13].

2.2.3 Parallel Active Filter for Harmonic Voltage Source Type Nonlinear Loads

Figure 2.4 illustrates the application of the PAF to harmonic voltage source type nonlinear load represented with Thevenin's equivalent circuit. The voltage source, V_l, and the series impedance Z_L represent the Thevenin's equivalent voltage source. The aim of the PAF in this case is again to compensate the load current harmonics to provide sinusoidal line current similar to the case of the previous section. Therefore, the representation of the PAF in this case also is a current source I_F defined by (2.1) with the same *G(s)* transfer function. *G(s)* is equal to zero at the fundamental frequency ($|G(s)|_f = 0$) and approximately equal to unity at all harmonic frequencies ($|G(s)|_h \approx 1$).

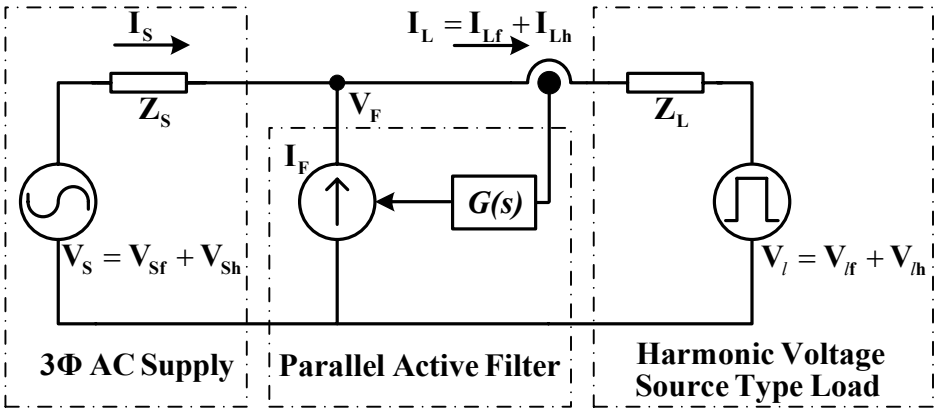

Figure 2.4 Application of the parallel active filter to a harmonic voltage source type nonlinear load which is represented as Thevenin's equivalent.

By circuit analysis, the line current I_S and the total load current I_L are derived as in (2.10) and (2.11) respectively.

$$I_S = \frac{1}{Z_S + \frac{Z_L}{1 - G(s)}}\left(V_S - V_L\right) \tag{2.10}$$

$$I_L = \frac{1}{\left(1 - G(s)\right)\left(Z_S + \frac{Z_L}{1 - G(s)}\right)}\left(V_S - V_L\right) \tag{2.11}$$

Equation (2.10) implies that line current becomes sinusoidal when the condition given by

$$\left|Z_S + \frac{Z_L}{1 - G(s)}\right|_h >> 1 \text{ p.u.} \tag{2.12}$$

is satisfied. In this case, (2.1), (2.10), and (2.11) are reduced respectively to

$$I_F \cong I_{Lh} \tag{2.13}$$

$$I_{Sh} \cong 0 \tag{2.14}$$

$$I_{Lh} \cong \frac{1}{Z_L}\left(V_{Sh} - V_{lh}\right) \tag{2.15}$$

For the case of the application of the PAF to harmonic voltage source type nonlinear load, (2.13) shows that the PAF current is approximately equal to the load current harmonics and (2.14) implies that line current I_S becomes harmonic free if the condition in (2.12) is satisfied. Therefore (2.12) is the required condition for the PAF to compensate the load current harmonics and to provide sinusoidal line current. This condition requires that Z_L should be large compared to Zs and $|1\text{-}G(s)|_h << 1$.

Although the condition $|1-G(s)|_h << 1$ is satisfied by the PAF, the overall satisfaction of (2.12) is difficult when it is applied to a pure harmonic voltage source type non-linear load with $Z_L \rightarrow 0$ (e.g. diode rectifier with sufficient smoothing dc capacitors representing very low internal impedance with $Z_L \approx 0$). Therefore, the line current will no longer become sinusoidal. Moreover, the injected current by the PAF will flow into the load and can result in overcurrent for this type of load since $Z_L \approx 0$ and $Z_L < Z_S$ where the typical value of Z_S is lower than 0.1 p.u. As the load current harmonic content increases, so does the PAF current, thus the rating of the PAF increases. As a result, the above discussion implies that the application PAF to harmonic voltage source type nonlinear loads does not provide harmonic compensation of the load current and does not yield sinusoidal line current [12], [13].

Many industrial loads such as ASDs and UPSs utilize smoothing capacitors at their DC buses in order to keep their voltage at constant level. In such cases, the utilization of the PAF does not seem reasonable for the harmonic current compensation since these nonlinear loads behave as harmonic voltage sources. However, such nonlinear loads utilize DC side inductor or AC side inductor at the DC side or AC side of the rectifier with typical values of 3%-5% to smooth the input current (in order to obtain a quasi-square waveform input current with lower distortion) and to reduce the harmonic current stresses on the DC bus capacitor. Figure 2.5 illustrates two front-end circuits for these loads, where a DC side inductor is utilized before the DC bus capacitor of diode (or thyristor) rectifier (Figure 2.5.a) and a three phase AC side inductor is utilized before the diode (or thyristor) rectifier (Figure 2.5.b). Their AC line input voltage and current waveforms are also illustrated in the same figure. By inserting inductors in series with a harmonic voltage source type nonlinear load, its characteristics are converted to those of a harmonic current source type nonlinear load. The effect of the inserted inductor to a harmonic voltage source type nonlinear load can be observed by comparing the waveforms of Figure 2.1.b to those of Figure 2.5. With the insertion of the inductors, the originally pulsating load current waveform of Figure 2.1.b is smoothed and flattened to a shape that has lower peak values. It resembles the input current waveform of a harmonic current source type nonlinear load as in Figure 2.1.a. With the load type converted to a harmonic current

source type, the PAF can be applied for compensation as discussed in the previous section, and its compensation characteristics will be completely defined by the active filter transfer function.

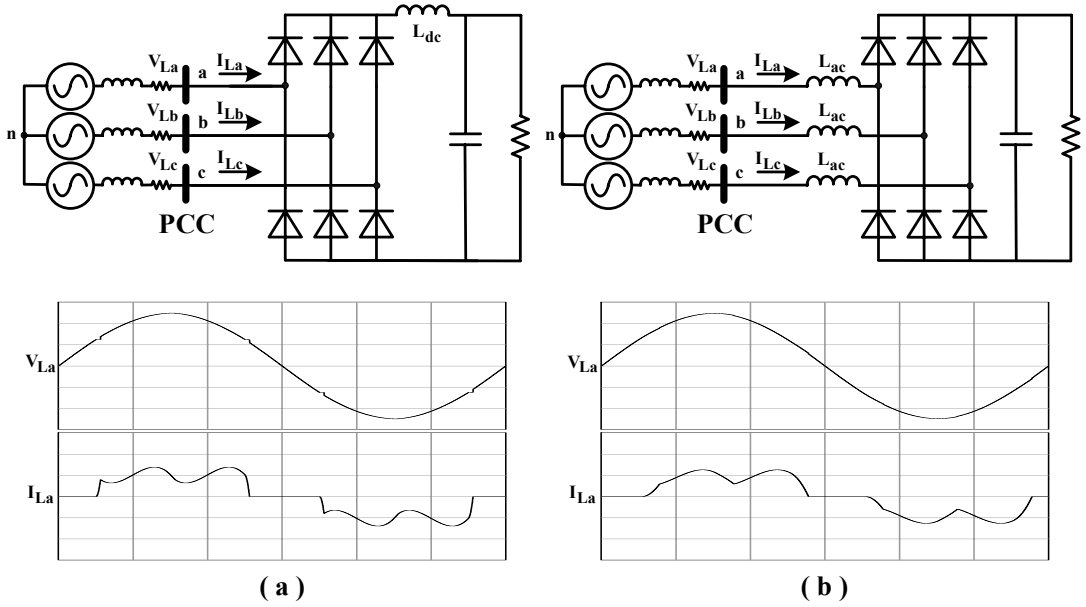

Figure 2.5 A typical 3-phase nonlinear diode rectifier with DC bus capacitor and its input waveforms: a) with a DC side inductor, b) with an AC side inductor.

The utilization of only DC side inductance to achieve a lower input current distortion and lower stresses on DC bus capacitor is a cost effective solution for the front-end rectifiers of many industrial loads compared to rectifiers with only AC side inductors. Although they result in notable voltage drop, AC side in-line reactors are utilized in many industrial loads for the immunity to the supply side transients and ride-trough capabilities during voltage sags and surges. Moreover, AC side in-line reactors reduce di/dt value of the input current during the commutation intervals. Reducing di/dt value of the input current results in a lower bandwidth requirement for PAF and plays an important role for a stable and proper operation of a PAF [9], [10]. Some industrial loads utilize both DC side and AC side inductors for their front-end rectifiers as shown in Figure 2.6. Although this topology has the highest cost, it is an optimal front-end circuit with the features of both inductors discussed above and

behaves as a harmonic current source type nonlinear load. Moreover, the 6-pulse rectifiers with DC capacitor and 3-5% DC and/or AC side inductors have typical THD_I values of 25-40% similar to the stiff current sources with THD_I values of 25-30%. The typical input current harmonic spectrum of a 6 pulse rectifier with DC side capacitor and 3-5% DC and/or AC side resembles the input current harmonic spectrum of the stiff current source, which is illustrated in Figure 2.7. While the harmonics generated by the 6 pulse rectifier have the same harmonic order of h = 6k±1 (k=1, 2, 3…), the 5^{th} harmonic current is a bit larger for the 6-pulse rectifier with DC bus capacitor and 3-5% DC and/or AC side inductor than that of the 6-pulse rectifier illustrated in Figure 2.1.a (stiff current source 6-pulse rectifier). The typical THD_I values and harmonic spectrums of 6-pulse rectifiers with DC bus capacitor and 3-5% DC and/or AC side inductor are similar those of the stiff current source 6-pulse rectifier. This also proves the characteristics of the 6-pulse rectifiers with DC capacitor and 3-5% DC and/or AC side inductor are the same as those of harmonic current source type nonlinear loads.

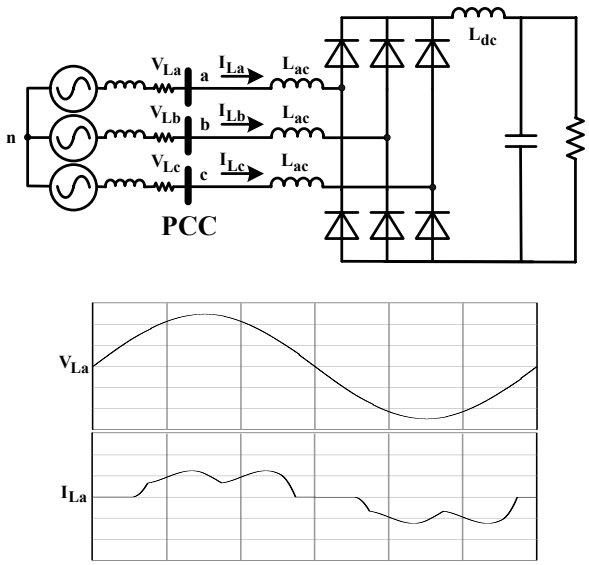

Figure 2.6 A typical 3-phase nonlinear rectifier with DC bus capacitor, DC side inductor and AC side inductor and its typical input waveforms.

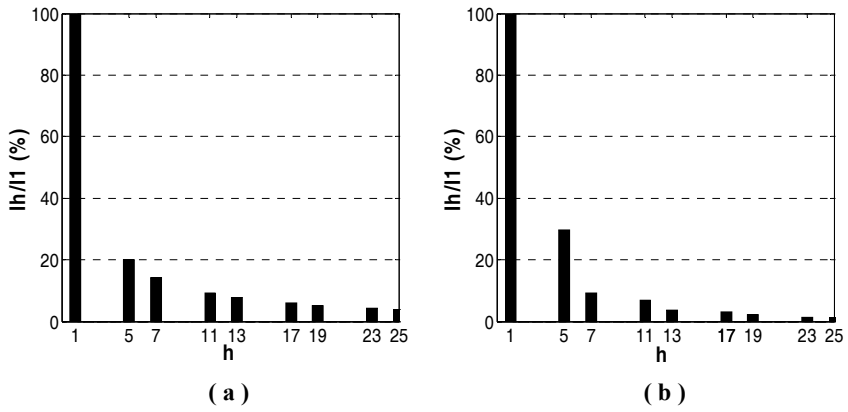

Figure 2.7 The typical input current harmonic spectrums for: a) a stiff current source 6-pulse rectifier, b) a 6-pulse rectifier with DC capacitor and 3-5% DC and/or AC side inductor.

If a PAF is applied to diode/thyristor rectifiers with AC and/or DC side inductors, in other words to harmonics current source type nonlinear loads, its compensation characteristics are independent of the supply impedance and load impedance and are only determined by the transfer function *G(s)* of the PAF. Therefore, for harmonic free line current, the parallel active filter should be implemented such that *G(s)* has a characteristic of a notch filter at fundamental frequency, where *G(s)* is equal to zero at fundamental frequency ($|G(s)|_f = 0$) and approximately equal to unity at all harmonic frequencies ($|G(s)|_h \approx 1$). This characteristic is obtained with the control algorithm of the PAF, to be discussed in the next section.

2.3 Control of The Parallel Active Filter

The implementation of the PAF as a controlled current source first requires the generation of the reference signal and then the regulation of the generated reference signal. For this purpose, the control algorithm of the PAF consists of two main blocks as illustrated in Figure 2.8: Current reference generator and current controller. The current reference generator block involves two blocks; the harmonic current reference generator and the DC bus voltage regulator. The harmonic current reference generator extracts the harmonic components of the load current by the

utilization of the measured load current (I_L) and terminal voltage (V_F). Moreover, this unit extracts the reactive power and the negative sequence current component of the load current, if the PAF is desired to compensate these currents. The DC bus voltage regulator with DC bus voltage (V_{dc}) feedback creates a current reference to hold DC bus voltage at its desired value. The output signals of the reference harmonic current generator and DC bus voltage regulator constitute the total current reference of the PAF (I^*_F). This current reference is sent to current controller, which regulates the reference signal with the feedback signal of PAF current and creates switching signals to the VSI for the desired current at the PAF output terminals. In order to achieve a high performance PAF, the implementation of each control block in the PAF control algorithm is critical. The following sections discuss these control blocks and their implementation issues.

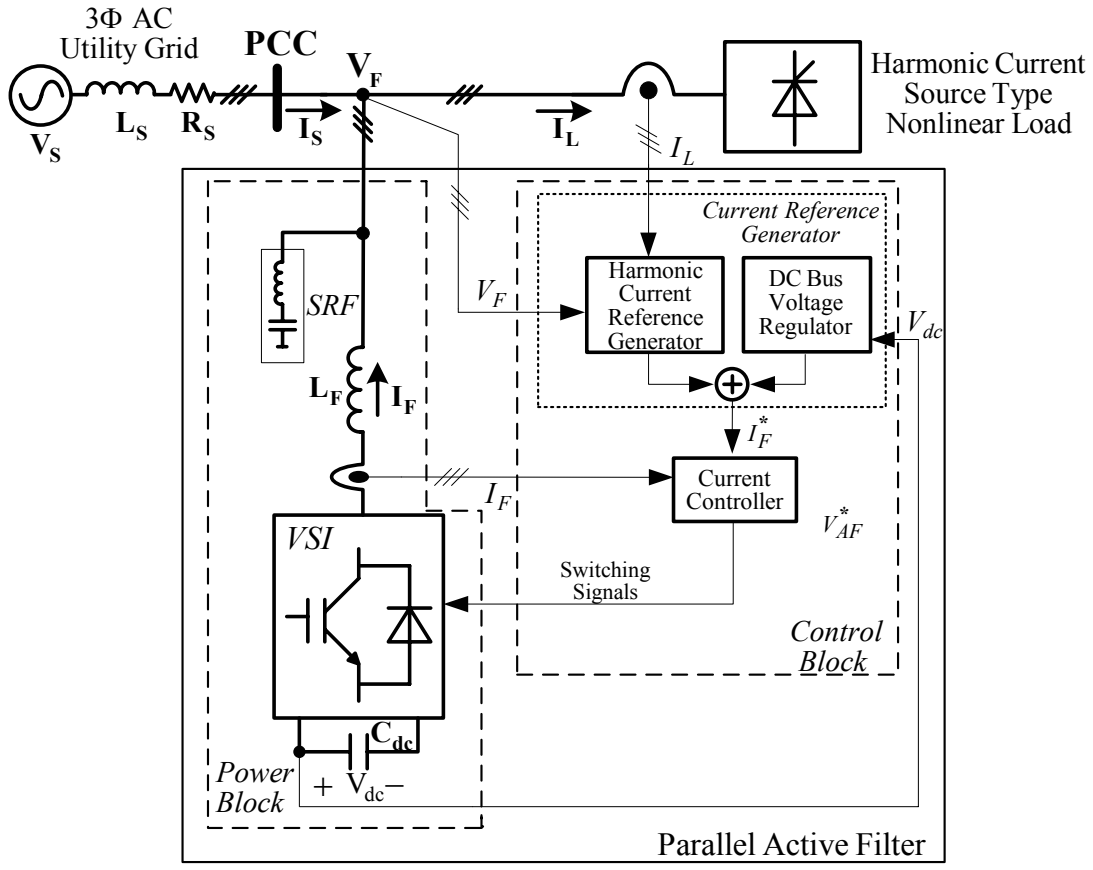

Figure 2.8 Parallel active filter system.

2.3.1 Harmonic Current Reference Generator

Implemented as a current controlled VSI, PAF generates a current equal to the load current harmonics, reactive power component at fundamental frequency and negative sequence component to achieve a utility grid current which is balanced, sinusoidal, and in-phase with the voltage at the PCC. The accuracy of the PAF current reference generation determines the performance of the PAF. Therefore the current reference generation of PAF implemented as a current controlled VSI is a critical part in the PAF control algorithm.

Harmonic current extraction methods utilized in the PAF application can be classified into two groups as frequency domain methods and time domain methods. Frequency domain methods are recently utilized in harmonic current extraction with the utilization of digital signal processors (DSPs) in real-time implementations. The frequency domain methods are based on Fourier analysis method of discrete signals such as Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT). Once the desired reference signal (load current harmonics, fundamental reactive power current and/or negative sequence current in PAF application) is identified by Fourier analysis, the back transform is applied to construct the reference signal in time domain easily. However, since the frequency domain methods utilize a window function to analyze the frequency spectrum of the signal, the methods suffers from large memory requirement and large computational power for DSPs. Moreover, the settling time of the generated signal is large and the accuracy is lost during the transient conditions. The time domain methods are mainly preferred over frequency domain methods due to their less number of calculations and response speed during transients. The desired reference signal is identified by either analog or digital filtering approach in time domain methods. There exist two well known time domain methods for harmonic current extraction in the PAF application which are the Instantaneous Reactive Power Theory (IRPT) and the Synchronous Reference Frame Controller (SRFC) [13], [24], [25].

2.3.1.1 Instantaneous Reactive Power Theory

Instantaneous reactive power theory (IRPT) known as "Akagi-Nabae Theory" defines the instantaneous real power and instantaneous reactive power in a 3-phase 3-wire system where no zero-sequence voltage is included. IRPT is utilized to derive the fundamental and harmonic components of load current via measured line voltages and currents. Since the IRPT involves vectors, in the following the vectors and their convention will be summarized and then the IRPT will be explained.

Any three-phase vector variables (voltages or currents) without zero sequence components (as in the 3-phase 3-wire system) can be expressed as in (2.16). This illustrates that the third variable is a function of the other two. In other words, in such a system there are only two independent variables. Hence, the vector variables can be represented in the two dimensional complex coordinates, which is named as 'ds-qs' reference frame in this thesis. Any three-phase vector variables are transformed to 'ds-qs' reference frame by utilizing (2.17). The 'C' matrix in (2.17) is referred as the the 'a-b-c' reference frame to 'ds-qs' reference frame transformation matrix. Figure 2.9 illustrates the relationship between the 'a-b-c' reference frame and two-dimensional 'ds-qs' reference frame. The variables, 'x_{ds}' and 'x_{qs}' in (2.17) constitutes a vector ('x_{dqs}' vector) in complex coordinates ('ds-qs' reference frame), which is expressed as in (2.18), such that the 'x_{ds}' vector is the projection of the 'x_{dqs}' vector on the 'ds' axis and the 'x_{qs}' vector is the projection of the 'x_{dqs}' vector on the 'qs' axis as in the Figure 2.9. In (2.18), "*j*" represents the imaginary unity vector. The 'x_{qs}' vector, which defines any 'a-b-c' reference frame vector variables in the 'ds-qs' reference frame, can be interpreted as a vector rotating with the angular velocity of 'θ'. The rotation with the 'x_{qs}' vector is defined by the '$e^{j\theta}$' term in (2.18).

$$x_a + x_b + x_c = 0 \tag{2.16}$$

$$\begin{bmatrix} x_{ds} \\ x_{qs} \end{bmatrix} = C \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.17}$$

$$x_{\mathrm{dqs}} = x_{\mathrm{ds}} + jx_{\mathrm{qs}} = \left|x_{\mathrm{dqs}}\right| e^{j\theta} \tag{2.18}$$

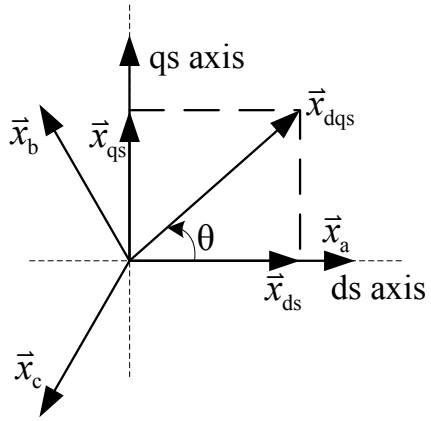

Figure 2.9 The relation between the a-b-c and ds-qs coordinates.

In IRPT, the instantaneous real power (*P*) and instantaneous reactive power (*Q*) are defined as in (2.19) and (2.20) respectively by 'ds-qs' reference frame (α-β reference frame) voltages and currents. These voltages and currents are obtained by the transformation of the measured line voltages and the load currents as in (2.21) and (2.22) respectively via the 'a-b-c' frame to 'ds-qs' frame transformation matrix C given in (2.17). By defining the IRPT matrix of V as in (2.23) and utilizing the 'ds-qs' frame voltages, *P* and *Q* can be written as in (2.24). According to the theory, if the load current consists of harmonics, (2.24) consist of DC terms and AC terms, where the DC terms correspond to the conventional real and reactive power at fundamental frequency and the AC terms correspond to the harmonic power provided that line voltages are sinusoidal at fundamental line frequency. Therefore, the fundamental and the harmonic power components of the system can be decomposed and separated by utilizing appropriate filtering of *P* and *Q* terms and the reference power quantities P^* and Q^* are obtained as in Figure 2.10, which illustrates the basic block diagram of the IRPT.

$$P = \frac{3}{2}\left(V_{Fds} I_{Lds} + V_{Fqs} I_{Lqs}\right) \tag{2.19}$$

$$Q = \frac{3}{2}\left(-V_{Fqs} I_{Lds} + V_{Fds} I_{Lqs}\right) \tag{2.20}$$

$$\begin{bmatrix} V_{Fds} \\ V_{Fqs} \end{bmatrix} = \mathrm{C} \begin{bmatrix} V_{Fa} \\ V_{Fb} \\ V_{Fc} \end{bmatrix} \tag{2.21}$$

$$\begin{bmatrix} I_{Lds} \\ I_{Lqs} \end{bmatrix} = \mathrm{C} \begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} \tag{2.22}$$

$$\mathrm{V} = \frac{3}{2} \begin{bmatrix} V_{Fds} & V_{Fqs} \\ -V_{Fqs} & V_{Fds} \end{bmatrix} \tag{2.23}$$

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \mathrm{V} \begin{bmatrix} I_{Lds} \\ I_{Lqs} \end{bmatrix} = \frac{3}{2} \begin{bmatrix} V_{Fds} & V_{Fqs} \\ -V_{Fqs} & V_{Fds} \end{bmatrix} \begin{bmatrix} I_{Lds} \\ I_{Lqs} \end{bmatrix} \tag{2.24}$$

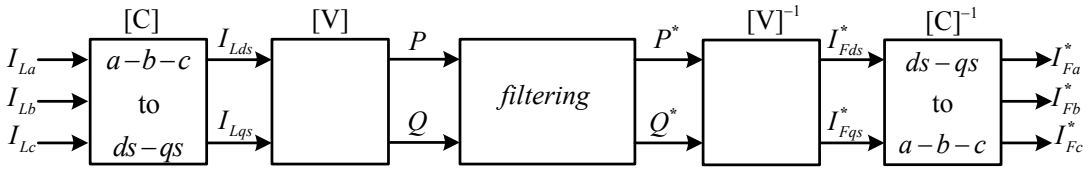

Figure 2.10 Block diagram of instantaneous reactive power theory.

Applying the back transformation matrix V^{-1} given in (2.25) and defined as the inverse of the IRPT matrix V in (2.23), the reference currents of (2.26) in 'ds-qs' frame are obtained. Finally, three phases reference currents of (2.27) are derived by utilizing the 'ds-qs' frame to a-b-c' frame transformation matrix C^{-1} given in (2.28). A case study illustrating the theory behind IRPT for the harmonic current reference generation and limitations of IRPT in the presence of line voltage harmonics can be performed as follows:

$$\mathrm{V}^{-1} = \frac{2}{3(V_{Fds}^2 + V_{Fqs}^2)} \begin{bmatrix} V_{Fds} & -V_{Fqs} \\ V_{Fqs} & V_{Fds} \end{bmatrix} \tag{2.25}$$

$$\begin{bmatrix} I_{Fds} \\ I_{Fqs} \end{bmatrix}^* = \mathrm{V}^{-1} \begin{bmatrix} P \\ Q \end{bmatrix}^* \tag{2.26}$$

$$\begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix}^* = \mathrm{C}^{-1} \begin{bmatrix} I_{Fds} \\ I_{Fqs} \end{bmatrix}^* \tag{2.27}$$

$$\mathrm{C}^{-1} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{2.28}$$

The block diagram of the case study is illustrated in Figure 2.11, where an ideal high pass filter is utilized to extract the load current harmonics by the IRPT. Assume that the 3-phase balanced load currents given in (2.29) consist of a fundamental current component at frequency of ω_1 with the peak value $\hat{I}_1$ and phase angle delay φ_1 and 5th harmonic current component at frequency of $5\omega_1$ with a peak value of $\hat{I}_5$ and phase angle delay φ_5. Similarly, 3-phase balanced voltages at PCC given in (2.30) are defined as the sum of fundamental frequency component taken as a reference with a peak value of $\hat{U}_1$ and zero phase angle delay and 5th harmonic voltage component at frequency of $5\omega_1$ with a peak value of $\hat{U}_5$ and phase angle delay of β_5. The P and Q terms for the currents and voltages in (2.29) and (2.30) respectively can be obtained as in (2.31) with the equations (2.21) through (2.24). The P and Q terms in (2.31) consist of DC and AC terms as mentioned earlier, where the AC terms correspond to the harmonic power according to the IRPT. By utilizing an ideal HPF filter as illustrated in Figure 2.11, the reference AC terms in (2.31) can be extracted as in

(2.32). The 'ds-qs' frame currents I^*_{Lds} and I^*_{Lqs} supposed to be the load current harmonics are formed as in (2.33) and (2.34) respectively by utilizing the back transformation defined in (2.26). The term 'Δ' in (2.33) and (2.34) is defined in (2.35). Although, the 'ds-qs' reference frame load currents I_{Lds} and I_{Lqs} defined in (2.29) consist of only the 5th frequency harmonic component, the reference 'ds-qs' frame currents I^*_{Lds} and I^*_{Lqs} in (2.33) and (2.34) respectively consist of fundamental, 7th, and 11th frequency components in addition to 5th frequency component in the presence of the 5th harmonic voltage at voltages at PCC. Moreover, the denominator term given in (2.35) has an AC component at $6\omega_1$ frequecy. In order to illustrate the effect of the 5th harmonic component of the PCC voltages to the magnitude of derived reference signals, a simple calculation can be carried out by assuming that $\hat{U}_1$ is 1 p.u., $\hat{I}_1$ is 1 p.u., and $\hat{U}_5$ is 0.02 p.u. (2%). In this case, I^*_{Lds} in (2.31) and I^*_{Lqs} in (2.32) have 7th harmonic frequency components with approximately 2% (0.02 p.u.). Moreover, the denominator term has 6th harmonic component with 4% (0.04 p.u.). This case study clearly illustrates the limitation of the IRPT utilized for load current harmonic extraction in the presence of voltage harmonics. If the 5th harmonic voltage component is equated to zero ($\hat{U}_5 = 0$) in the 'ds-qs' reference frame currents I^*_{Lds} and I^*_{Lqs} in (2.33) and (2.34), I^*_{Lds} and I^*_{Lqs} reduce to (2.36) and (2.37). I^*_{Lds} and I^*_{Lqs} in (2.36) and (2.37) are the 'ds-qs' frame currents of the 5th harmonic component in (2.29) and equivalent to load current harmonics. Therefore, the IRPT extracts load current harmonics successfully in the absence of voltage distortions at PCC. However, the harmonic voltage distortions on AC utility grid voltage are always present due to the nonlinear loads connected to the PCC. Therefore, the IRPT has limitations in extraction of load current harmonics utilized as reference signals in PAF [13].

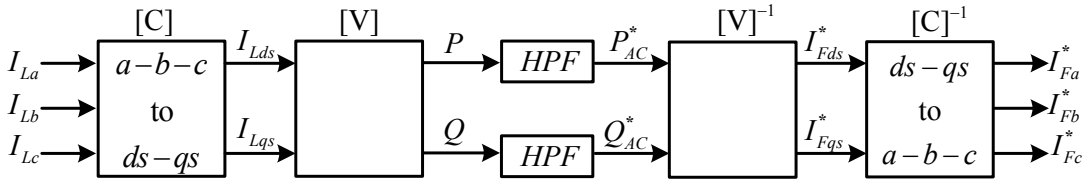

Figure 2.11 Block diagram of instantaneous reactive power theory for load harmonic current extraction.

$$\begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} = \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t + \varphi_1) \\ \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t - \frac{2\pi}{3} + \varphi_1) \\ \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t + \frac{2\pi}{3} + \varphi_1) \end{bmatrix} + \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L5}} \sin(5\omega_1 t + \varphi_5) \\ \hat{\mathrm{I}}_{\mathrm{L5}} \sin(5\omega_1 t + \frac{2\pi}{3} + \varphi_5) \\ \hat{\mathrm{I}}_{\mathrm{L5}} \sin(5\omega_1 t - \frac{2\pi}{3} + \varphi_5) \end{bmatrix} \tag{2.29}$$

$$\begin{bmatrix} V_{Fa} \\ V_{Fb} \\ V_{Fc} \end{bmatrix} = \begin{bmatrix} \hat{\mathrm{U}}_1 \sin(\omega_1 t) \\ \hat{\mathrm{U}}_1 \sin(\omega_1 t - \frac{2\pi}{3}) \\ \hat{\mathrm{U}}_1 \sin(\omega_1 t + \frac{2\pi}{3}) \end{bmatrix} + \begin{bmatrix} \hat{\mathrm{U}}_5 \sin(5\omega_1 t + \beta_5) \\ \hat{\mathrm{U}}_5 \sin(5\omega_1 t + \frac{2\pi}{3} + \beta_5) \\ \hat{\mathrm{U}}_5 \sin(5\omega_1 t - \frac{2\pi}{3} + \beta_5) \end{bmatrix} \tag{2.30}$$

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \frac{3}{2} \begin{bmatrix} \hat{\mathrm{U}}_1 \hat{\mathrm{I}}_{\mathrm{L1}} \cos(\varphi_1) + \hat{\mathrm{U}}_5 \hat{\mathrm{I}}_{\mathrm{L5}} \cos(\beta_5 - \varphi_1) - \hat{\mathrm{U}}_1 \hat{\mathrm{I}}_{\mathrm{L5}} \cos(6\omega_1 t + \varphi_5) - \hat{\mathrm{U}}_5 \hat{\mathrm{I}}_{\mathrm{L1}} \cos(6\omega_1 t + \beta_5 + \varphi_5) \\ \mathrm{U}_1 \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\varphi_1) + \hat{\mathrm{U}}_5 \hat{\mathrm{I}}_{\mathrm{L5}} \sin(\beta_5 - \varphi_1) + \hat{\mathrm{U}}_1 \hat{\mathrm{I}}_{\mathrm{L5}} \sin(6\omega_1 t + \varphi_5) - \hat{\mathrm{U}}_5 \hat{\mathrm{I}}_{\mathrm{L1}} \sin(6\omega_1 t + \beta_5 + \varphi_5) \end{bmatrix} \tag{2.31}$$

$$\begin{bmatrix} P \\ Q \end{bmatrix}_{AC}^{*} = \frac{3}{2} \begin{bmatrix} -\hat{\mathrm{U}}_1 \hat{\mathrm{I}}_{\mathrm{L5}} \cos(6\omega_1 t + \varphi_5) - \hat{\mathrm{U}}_5 \hat{\mathrm{I}}_{\mathrm{L1}} \cos(6\omega_1 t + \beta_5 + \varphi_5) \\ \hat{\mathrm{U}}_1 \hat{\mathrm{I}}_{\mathrm{L5}} \sin(6\omega_1 t + \varphi_5) - \hat{\mathrm{U}}_5 \hat{\mathrm{I}}_{\mathrm{L1}} \sin(6\omega_1 t + \beta_5 + \varphi_5) \end{bmatrix} \tag{2.32}$$

$$I_{Fds}^{*} = \frac{1}{\Delta} \Big(\hat{\mathrm{U}}_5^2 \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t + \varphi_1) + \hat{\mathrm{U}}_1^2 \hat{\mathrm{I}}_{\mathrm{L5}} \sin(5\omega_1 t + \varphi_5) - \hat{\mathrm{U}}_1 \hat{\mathrm{U}}_5 \hat{\mathrm{I}}_{\mathrm{L1}} \sin(7\omega_1 t + \varphi_1 + \beta_5) - \hat{\mathrm{U}}_1 \hat{\mathrm{U}}_5 \hat{\mathrm{I}}_{\mathrm{L5}} \sin(11\omega_1 t + \varphi_5 + \beta_5) \Big) \tag{2.33}$$

$$I_{Fqs}^{*} = \frac{1}{\Delta} \Big(-\hat{\mathrm{U}}_5^2 \hat{\mathrm{I}}_{\mathrm{L1}} \cos(\omega_1 t + \varphi_1) + \hat{\mathrm{U}}_1^2 \hat{\mathrm{I}}_{\mathrm{L5}} \cos(5\omega_1 t + \varphi_5) + \hat{\mathrm{U}}_1 \hat{\mathrm{U}}_5 \hat{\mathrm{I}}_{\mathrm{L1}} \cos(7\omega_1 t + \varphi_1 + \beta_5) - \hat{\mathrm{U}}_1 \hat{\mathrm{U}}_5 \hat{\mathrm{I}}_{\mathrm{L5}} \cos(11\omega_1 t + \varphi_5 + \beta_5) \Big) \tag{2.34}$$

$$\Delta = \Big(\hat{\mathrm{U}}_1^2 + \hat{\mathrm{U}}_5^2 - 2\hat{\mathrm{U}}_1 \hat{\mathrm{U}}_5 \cos(6\omega_1 t + \beta_5) \Big) \tag{2.35}$$

$$I^*_{Fds} = \hat{\mathrm{I}}_{\mathrm{L5}} \sin(5\omega_1 t + \varphi_5) \tag{2.36}$$

$$I^*_{Fqs} = \hat{\mathrm{I}}_{\mathrm{L5}} \cos(5\omega_1 t + \varphi_5) \tag{2.37}$$

2.3.1.2 Synchronous Reference Frame Controller

The basic principle of the synchronous reference frame controller (SRFC) [13] [23] for the current reference generation in PAF is illustrated in Figure 2.12. The measured load currents in 'a-b-c' frame are first transformed to 'ds-qs' frame via the 'a-b-c' frame to 'ds-qs' frame transformation matrix C in (2.17) and then to 'ds-qs' reference frame to 'de-qe' reference frame (synchronous reference frame) via the 'de-qe' reference frame transformation matrix T. The T matrix, which will be defined later, utilizes the phase angle information θ_e (=$\omega_e t$) of the AC utility voltage for the transformation of the quantities to synchronous reference frame. Since the SRFC involves the 'ds-qs' reference frame to 'de-qe' reference frame transformation, the 'de-qe' reference frame transformation and its convention will be summarized in the following and then the SRFC will be explained.

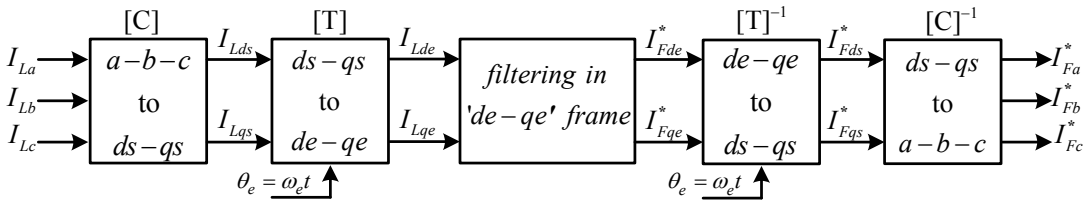

Figure 2.12 The basic principle of the synchronous reference frame controller.

The 'ds-qs' reference frame to 'de-qe' reference frame transformation is the transformation of the 'x_{dqs}' vector in (2.18) to the 'de-qe' reference frame which is synchronized to the phase angle θ_e of the AC utility voltage. Once the transformation is performed, the new vector in the 'de-qe' reference frame is defined as the 'x_{dqe}' vector given in (2.38). To perform the synchronization of the 'x_{dqs}' vector to the phase angle θ_e of the AC utility voltage, the 'x_{dqs}' vector is multiplied by the '$e^{-j\theta e}$' term so that the 'x_{dqe}' vector is derived as in (2.39). In fact, the equation in (2.39)

presents the relation between the 'ds-qs' reference frame and the 'de-qe' reference frame. Once the (2.39) is written in matrix form in terms of 'cosine' and 'sine' functions, the relation between the components of 'x_{dqe}' vector and 'x_{dqs}' vector is obtained as in (2.40). The matrix T, which is mentioned at the beginning of this section, in (2.40) is the 'ds-qs' reference frame to the 'de-qe' reference frame transformation function.

$$x_{\mathrm{dqe}} = x_{\mathrm{de}} + jx_{\mathrm{qe}} \tag{2.38}$$

$$x_{\mathrm{dqe}} = x_{\mathrm{dqs}} e^{-j\theta_e} = (x_{\mathrm{ds}} + jx_{\mathrm{qs}}) e^{-j\theta_e} = \left| x_{\mathrm{dqs}} \right| e^{j\theta} e^{-j\theta_e} \tag{2.39}$$

$$\begin{bmatrix} x_{\mathrm{de}} \\ x_{\mathrm{qe}} \end{bmatrix} = \begin{bmatrix} \cos(\theta_e) & \sin(\theta_e) \\ -\sin(\theta_e) & \cos(\theta_e) \end{bmatrix} \begin{bmatrix} x_{\mathrm{ds}} \\ x_{\mathrm{qs}} \end{bmatrix} = \mathrm{T} \begin{bmatrix} x_{\mathrm{ds}} \\ x_{\mathrm{qs}} \end{bmatrix} \tag{2.40}$$

The equations in (2.38), (2.39), and (2.40) defines the general convention with the 'de-qe' reference frame. These general conventions are defined by taking the 'cosine' function as reference. However, the variables in this thesis are defined by taking the 'sine' function as reference. Therefore, the derived T matrix in (2.40) should be adjusted based on the 'sine' function as reference. Since the 'sine' function lags the cosine functions by π/2 rad, the T matrix in (2.40) can be adjusted based on the 'sine' function as reference by replacing the θ_e in (2.40) as

$$\theta_e = \theta_e - \frac{\pi}{2} \tag{2.41}$$

In this case, the T matrix (2.40) becomes as

$$\mathrm{T} = \begin{bmatrix} \cos(\theta_e - \frac{\pi}{2}) & \sin(\theta_e - \frac{\pi}{2}) \\ -\sin(\theta_e - \frac{\pi}{2}) & \cos(\theta_e - \frac{\pi}{2}) \end{bmatrix} = \begin{bmatrix} \sin(\theta_e) & -\cos(\theta_e) \\ \cos(\theta_e) & \sin(\theta_e) \end{bmatrix} \tag{2.42}$$

which defines the 'ds-qs' reference frame to the 'de-qe' reference frame transformation matrix by taking the 'sine' function as reference. The above discussion has presented the 'de-qe' reference frame convention utilized in this thesis and has defined the 'ds-qs' reference frame to 'de-qe' reference frame transformation matrix T illustrated in Figure 2.12.

In SRFC, once the transformation to the 'de-qe' reference frame is carried out, the positive sequence current components at the frequency of ω_e appear as DC quantities where the negative sequence current components at the frequency of ω_e and the current components at the other frequencies (harmonics) appear as AC quantities in the 'de-qe' reference frame. By employing appropriate filtering in the 'de-qe' reference frame, the DC and AC quantities can be identified easily. Once the filtering in 'de-qe' reference frame is carried out, the desired 'de-qe' reference frame reference signals are obtained and transformed back to 'ds-qs' reference frame via the back transformation matrix T^{-1} given in (2.43) which is defined as the inverse of matrix T in (2.42). Finally, 3-phase reference currents are obtained by utilizing the 'ds-qs' reference frame to 'a-b-c' reference frame transformation matrix C^{-1} given in (2.28). The SRFC utilizes only the measured load currents in order to derive the reference signals compared to the IRPT. However, the 'de-qe' frame transformation matrix T needs the phase angle information θ_e, which is obtained via a phase locked loop (PLL) circuit. The accuracy of the phase angle information θ_e from PLL is critical to obtain the correct current references via the SRFC. Therefore, this section includes the implementation of the PLL which is a part of SRFC in the PAF application. In this section, first the PLL will be discussed and then case studies illustrating the extraction of the desired signals (harmonics, reactive power current, and the negative sequence current component) in the PAF application will be analyzed and the principles of SRFC will be highlighted.

$$T^{-1} = \begin{bmatrix} \sin(\theta_e) & \cos(\theta_e) \\ -\cos(\theta_e) & \sin(\theta_e) \end{bmatrix} \tag{2.43}$$

2.3.1.2.1 Vector Phase Locked Loop for SRFC

The phase angle of AC utility grid is a critical piece of information in transforming the measured control variables to the synchronous reference frame for control purposes in PAF application. Therefore, the quality of the obtained phase angle information determines the PAF control loop performance. In PAF application, this information is obtained by a vector PLL algorithm [26]. The vector PLL generates the AC utility grid phase angle information (θ) by utilizing the synchronous reference frame ('de-qe' reference frame) transformation and PI controller with 3-phase AC utility grid voltages as inputs. The basic block diagram of vector PLL system is illustrated in Figure 2.13. The operation of the vector PLL system which utilizes V_{Fqe} as a feedback signal can be understood by obtaining the synchronous reference frame phase voltages V_{Fde} and V_{Fqe} that are derived via the output angle θ_e of the vector PLL system. Assuming a balanced 3-phase system with 3-phase stationary reference frame (or named as 'a-b-c' frame) positive sequence voltages V_{Fa}, V_{Fb}, and V_{Fc} defined as

$$\begin{bmatrix} V_{Fa} \\ V_{Fb} \\ V_{Fc} \end{bmatrix} = \begin{bmatrix} \hat{U}_1 \sin(\theta_1) \\ \hat{U}_1 \sin(\theta_1 - \frac{2\pi}{3}) \\ \hat{U}_1 \sin(\theta_1 - \frac{4\pi}{3}) \end{bmatrix} \tag{2.44}$$

The 'ds-qs' reference frame voltages V_{Fds} and V_{Fqs} in (2.39) are obtained by utilizing 'a-b-c' frame to 'ds-qs' frame transformation matrix C in (2.17).

$$\begin{bmatrix} V_{Fds} \\ V_{Fqs} \end{bmatrix} = C \begin{bmatrix} V_{Fa} \\ V_{Fb} \\ V_{Fc} \end{bmatrix} = \begin{bmatrix} \hat{U}_1 \sin(\theta_1) \\ -\hat{U}_1 \cos(\theta_1) \end{bmatrix} \tag{2.45}$$

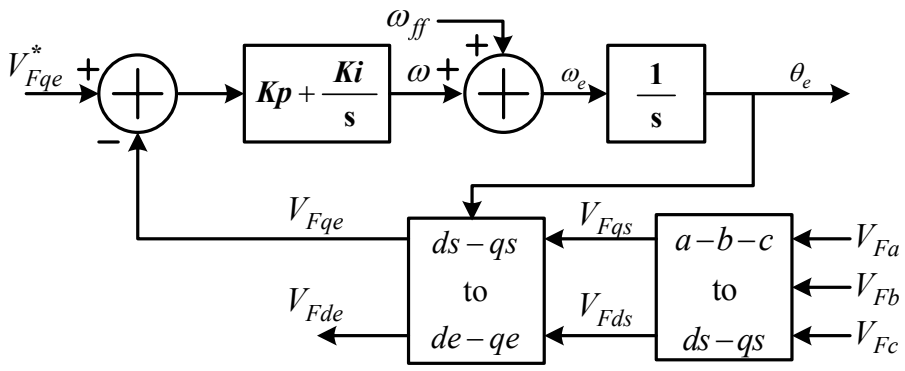

Figure 2.13 Basic block diagram of the vector PLL system.

The 'ds-qs' reference frame voltages V_{Fds} and V_{Fqs} in (2.45) are then transformed to 'de-qe' frame to obtain V_{Fde} and V_{Fqe} in (2.46) by utilizing 'ds-qs'frame to 'de-qe' frame transformation matrix T in (2.36) which includes the angle θ_e.

$$\begin{bmatrix} V_{Fde} \\ V_{Fqe} \end{bmatrix} = \mathrm{T} \begin{bmatrix} V_{Fds} \\ V_{Fqs} \end{bmatrix} = \begin{bmatrix} \hat{\mathrm{U}}_1 \cos(\theta_1 - \theta_e) \\ \hat{\mathrm{U}}_1 \sin(\theta_1 - \theta_e) \end{bmatrix} \tag{2.46}$$

If the output of the vector PLL, which is phase angle information θ_e is identical to the AC utility grid phase information θ_1, the synchronous reference frame phase voltages V_{Fde} and V_{Fqe} in (2.46) appear as DC quantities where V_{Fde} is equal to $\hat{\mathrm{U}}_1$ and $\mathrm{V_{Fqe}}$ is equal to zero. Therefore, by setting the V^*_{Fqe} reference to zero (V_{Fqe} = 0), the error between the reference signal and feedback signal (V^*_{Fqe} - V_{Fqe}) can be regulated via a PI controller, which presents zero steady-state error for DC signal references. The error compensation signal ω of the PI regulator is added to the feed-forward AC utility grid frequency signal ω_{ff} (= $2\pi f_e$) to obtain the AC Utility grid frequency information ω_e. The phase angle information θ_e obtained by integrating the ω_e signal is the output of the vector PLL system utilized in 'ds-qs' reference frame to 'de-qe' reference frame transformation. Therefore, the vector PLL control loop is closed and the phase angle information θ_e for the transformation matrix T utilized in harmonic current reference generator of PAF is locked to AC utility grid phase angle θ such that

$$\theta_1 = \theta_e \tag{2.47}$$

or equivalently

$$\omega_1 = \omega_e \tag{2.48}$$

Since vector PLL system utilizes measured 3-phase voltages, the harmonics and the notches on AC utility grid voltage enter the PLL control loop. However, since the PLL system utilizes two integrators regarded as low-pass filters to obtain the phase information θ_e, the output signal is clean under these distorted conditions. Moreover, by adjusting the gains of the PI regulator (in other words changing the cut-off frequency of low-pass filter), the stability of the phase angle information θ_e is adjusted under the distorted line voltage conditions [26].

2.3.1.2.2 Extraction of The Current Reference Signals via SRFC

A case study illustrating the extraction of the current reference signals via SRFC is as follows: The balanced positive sequence AC utility grid voltages at the PCC are defined as in (2.49) and taken reference. The 3-phase load currents given in (2.50) are assumed to have a positive sequence fundamental component at frequency of ω_1 with the peak value $\hat{I}_{L1}$ and phase angle delay φ_1 and to have 5^{th} and 7^{th} harmonic components with peak values $\hat{I}_{L5}$ and $\hat{I}_{L7}$ and phase angle delays φ_5 and φ_7 respectively. Note that the 5^{th} harmonic current in (2.50) is a negative sequence component and the 7^{th} harmonic current in (2.50) is a positive sequence component. The currents in (2.50) are transformed to 'ds-qs' reference frame via matrix C and given as in (2.51). The 'ds-qs' reference frame currents (I_{Lds} and I_{Lqs}) are transformed to 'de-qe' reference frame' via the matrix T utilizing phase information $\omega_e t$ and are obtained as in (2.52). If the phase information $\omega_e t$ (θ_e) from the PLL is identical to the fundamental phase information $\omega_1 t$ as in (2.47), the 'de-qe frame' currents (I_{Lde} and I_{Lqe}) in (2.52) reduce to the currents in (2.53).

$$\begin{bmatrix} V_{Fa} \\ V_{Fb} \\ V_{Fc} \end{bmatrix} = \begin{bmatrix} \hat{\mathrm{U}}_1 \sin(\omega_1 t) \\ \hat{\mathrm{U}}_1 \sin(\omega_1 t - \frac{2\pi}{3}) \\ \hat{\mathrm{U}}_1 \sin(\omega_1 t + \frac{2\pi}{3}) \end{bmatrix} \tag{2.49}$$

$$\begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} = \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t + \varphi_1) \\ \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t - \frac{2\pi}{3} + \varphi_1) \\ \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t + \frac{2\pi}{3} + \varphi_1) \end{bmatrix} + \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L5}} \sin(5\omega_1 t + \varphi_5) \\ \hat{\mathrm{I}}_{\mathrm{L5}} \sin(5\omega_1 t + \frac{2\pi}{3} + \varphi_5) \\ \hat{\mathrm{I}}_{\mathrm{L5}} \sin(5\omega_1 t - \frac{2\pi}{3} + \varphi_5) \end{bmatrix} + \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L7}} \sin(7\omega_7 t + \varphi_7) \\ \hat{\mathrm{I}}_{\mathrm{L7}} \sin(7\omega_7 t - \frac{2\pi}{3} + \varphi_7) \\ \hat{\mathrm{I}}_{\mathrm{L7}} \sin(7\omega_7 t + \frac{2\pi}{3} + \varphi_7) \end{bmatrix} \tag{2.50}$$

$$\begin{bmatrix} I_{Lds} \\ I_{Lqs} \end{bmatrix} = \mathrm{C} \begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} = \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t + \varphi_1) \\ -\hat{\mathrm{I}}_{\mathrm{L1}} \cos(\omega_1 t + \varphi_1) \end{bmatrix} + \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L5}} \sin(5\omega_1 t + \varphi_5) \\ \hat{\mathrm{I}}_{\mathrm{L5}} \cos(5\omega_1 t + \varphi_5) \end{bmatrix} + \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L7}} \sin(7\omega_1 t + \varphi_7) \\ -\hat{\mathrm{I}}_{\mathrm{L7}} \cos(7\omega_1 t + \varphi_7) \end{bmatrix} \tag{2.51}$$

$$\begin{aligned} \begin{bmatrix} I_{Lde} \\ I_{Lqe} \end{bmatrix} &= \mathrm{T} \begin{bmatrix} I_{Lds} \\ I_{Lqs} \end{bmatrix} = \begin{bmatrix} \sin(\omega_e t) & -\cos(\omega_e t) \\ \cos(\omega_e t) & \sin(\omega_e t) \end{bmatrix} \begin{bmatrix} I_{Lds} \\ I_{Lqs} \end{bmatrix} \\ &= \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L1}} \cos(\omega_1 t - \omega_e t + \varphi_1) \\ \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t - \omega_e t + \varphi_1) \end{bmatrix} + \begin{bmatrix} -\hat{\mathrm{I}}_{\mathrm{L5}} \cos(5\omega_1 t + \omega_e t + \varphi_5) \\ \hat{\mathrm{I}}_{\mathrm{L5}} \sin(5\omega_1 t + \omega_e t + \varphi_5) \end{bmatrix} + \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L7}} \cos(7\omega_1 t - \omega_e t + \varphi_7) \\ \hat{\mathrm{I}}_{\mathrm{L7}} \sin(7\omega_1 t - \omega_e t + \varphi_7) \end{bmatrix} \end{aligned} \tag{2.52}$$

$$\begin{bmatrix} I_{Lde} \\ I_{Lqe} \end{bmatrix} = \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L1}} \cos(\varphi_1) \\ \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\varphi_1) \end{bmatrix} + \begin{bmatrix} -\hat{\mathrm{I}}_{\mathrm{L5}} \cos(6\omega_1 t + \varphi_5) \\ \hat{\mathrm{I}}_{\mathrm{L5}} \sin(6\omega_1 t + \varphi_5) \end{bmatrix} + \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L7}} \cos(6\omega_1 t + \varphi_7) \\ \hat{\mathrm{I}}_{\mathrm{L7}} \sin(6\omega_1 t + \varphi_7) \end{bmatrix} \tag{2.53}$$

The first terms in (2.53) corresponding the fundamental frequency components of the 3-phase load currents in (2.50) appear as DC quantities. The 5th and 7th harmonic current components appear as AC quantities at $6\omega_1$ rotating in negative and positive

direction respectively. Therefore, I_{Lde} and I_{Lqe} currents in 'de-qe' reference frame can be expressed as the sum two components with subscripts of 'DC' and AC as in (2.54). The DC and AC components of (2.54) are given as in (2.55) and (2.56) respectively.

$$\begin{bmatrix} I_{Lde} \\ I_{Lqe} \end{bmatrix} = \begin{bmatrix} I_{Lde} \\ I_{Lqe} \end{bmatrix}_{DC} + \begin{bmatrix} I_{Lde} \\ I_{Lqe} \end{bmatrix}_{AC} \tag{2.54}$$

$$\begin{bmatrix} I_{Lde} \\ I_{Lqe} \end{bmatrix}_{DC} = \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L1}}\cos(\varphi_1) \\ \hat{\mathrm{I}}_{\mathrm{L1}}\sin(\varphi_1) \end{bmatrix} \tag{2.55}$$

$$\begin{bmatrix} I_{Lde} \\ I_{Lqe} \end{bmatrix}_{AC} = \begin{bmatrix} -\hat{\mathrm{I}}_{\mathrm{L5}}\cos(6\omega_1 t + \varphi_5) \\ \hat{\mathrm{I}}_{\mathrm{L5}}\sin(6\omega_1 t + \varphi_5) \end{bmatrix} + \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L7}}\cos(6\omega_1 t + \varphi_7) \\ \hat{\mathrm{I}}_{\mathrm{L7}}\sin(6\omega_1 t + \varphi_7) \end{bmatrix} \tag{2.56}$$

If the fundamental frequency real (active) power (P_1) in (2.57) and the reactive power (Q_1) in (2.58) of the nonlinear load with the PCC voltages given in (2.49) and the load currents given in (2.50) are compared to the DC component of 'de-qe' reference frame currents in (2.55), the DC 'de' axis current I_{Lde} in (2.55) corresponds the fundamental frequency active power current component of the load current and the DC 'qe' axis current I_{Lqe} in (2.55) corresponds the fundamental reactive power current component of the load current. Therefore, the 'de-qe' reference frame transformation of the load currents decomposes the load current components as the fundamental frequency active and reactive power current components given as in (2.59) and harmonic frequency current components given as in (2.60) if the phase angle information $\omega_e t$ from the PLL is identical to fundamental angle $\omega_1 t$. This analysis also illustrates the importance of the PLL system in the SRFC.

$$P_1 = \frac{3}{2}\hat{\mathrm{U}}_1\hat{\mathrm{I}}_{\mathrm{L1}}\cos(\varphi_1) \tag{2.57}$$

$$Q_1 = \frac{3}{2}\hat{\mathrm{U}}_1\hat{\mathrm{I}}_{\mathrm{L1}}\sin(\varphi_1) \tag{2.58}$$

$$\begin{bmatrix} I_{Lde} \\ I_{Lqe} \end{bmatrix}_{DC} = \begin{bmatrix} \hat{I}_{L1}\cos(\varphi_1) \\ \hat{I}_{L1}\sin(\varphi_1) \end{bmatrix} = \begin{bmatrix} \text{fundamental active power current} \\ \text{fundamental reactive power current} \end{bmatrix} \tag{2.59}$$

$$\begin{bmatrix} I_{Lde} \\ I_{Lqe} \end{bmatrix}_{AC} = \begin{bmatrix} -\hat{I}_{L5}\cos(6\omega_1 t + \varphi_5) \\ \hat{I}_{L5}\sin(6\omega_1 t + \varphi_5) \end{bmatrix} + \begin{bmatrix} \hat{I}_{L7}\cos(6\omega_1 t + \varphi_7) \\ \hat{I}_{L7}\sin(6\omega_1 t + \varphi_7) \end{bmatrix} = \begin{bmatrix} \text{harmonic} \\ \text{currents} \end{bmatrix} \tag{2.60}$$

If the load current given in (2.50) has also higher order harmonics (11^{th}, 13^{th}, 17^{th}, 19^{th}, and so on), the load currents in 'de-qe' reference frame will consist of AC components of frequency $12\omega_1$ corresponding 11^{th} and 13^{th} harmonic orders, $18\omega_1$ corresponding 17^{th} and 19^{th} harmonic orders, and so on. Since the fundamental and harmonic components of the load current are identified via SRFC, the fundamental and/or harmonic components of the load current can be decomposed by appropriate filtering in 'de-qe' reference frame. As shown in Figure 2.14, the 'de' axis and 'qe' axis fundamental components of load current can be extracted by LPFs. The selected LPFs should have maximally flat and unity gain characteristics at their pass-band and should provide adequate attenuation for the first harmonic components (harmonic components at $6\omega_1$) in the 'de-qe' reference frame. In fact, the LPFs should be designed such that they provide adequate attenuation for the AC components at $2\omega_1$ corresponding the negative sequence current component of load current in the case of an unbalance condition. Because, if there exists an unbalanced condition with load currents (negative sequence fundamental component of the load currents), the SRFC utilizing the transformation matrix T will transform the negative sequence fundamental frequency components to AC components with $2\omega_1$ frequency. In fact, the SRFC with the transformation matrix T is a positive sequence synchronous reference frame controller which transforms the positive sequence fundamental components to DC quantities and the negative sequence fundamental and the harmonic components to AC quantities. Therefore, to extract the positive sequence fundamental components of the load currents, the selected filters should provide adequate attenuation of AC components with $2\omega_1$ frequency. For this purpose, higher order LPFs with maximally flat gain characteristics at their pass-band (butterworth type LPFs) or cascaded first order LPFs with cut-off frequency of 5-20 Hz (for 50Hz

AC line applications) are utilized for accurate signal extraction. However, the lower cut-off frequencies result in a higher attenuation of AC components with a slower transient response while higher cut-off frequencies results in poor attenuation with a fast transient response [13], [23].

By assuming ideal LPFs in Figure 2.14, the positive sequence fundamental components of the load currents in 'de-qe' frame given in (2.59) can be extracted and can be transformed to 'de-qe' frame as in (2.61) and to 'a-b-c' frame as in (2.62). The obtained positive sequence fundamental components via SRFC in (2.62) are exactly the same of positive sequence fundamental components of load currents in (2.50). This illustrates the accuracy of SRFC in reference generation contrary to IRPT.

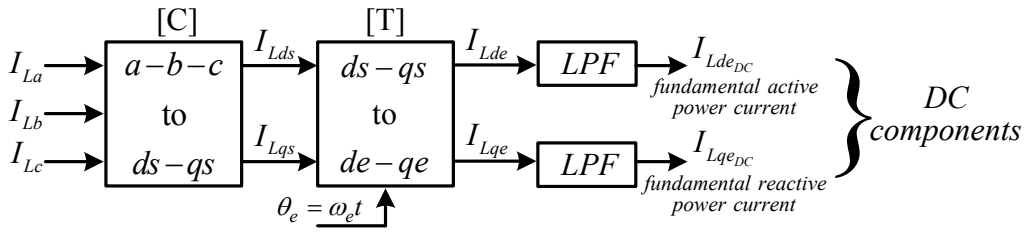

Figure 2.14 The extraction of fundamental frequency components via SRFC.

$$\begin{bmatrix} I_{Lds} \\ I_{Lqs} \end{bmatrix}^* = \mathrm{T}^{-1} \begin{bmatrix} I_{Lde} \\ I_{Lqe} \end{bmatrix}_{DC} = \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t + \varphi_1) \\ -\hat{\mathrm{I}}_{\mathrm{L1}} \cos(\omega_1 t + \varphi_1) \end{bmatrix} \tag{2.61}$$

$$\begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix}^* = \mathrm{C}^{-1} \begin{bmatrix} I_{Lds} \\ I_{Lqs} \end{bmatrix}^* = \begin{bmatrix} \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t + \varphi_1) \\ \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t - \frac{2\pi}{3} + \varphi_1) \\ \hat{\mathrm{I}}_{\mathrm{L1}} \sin(\omega_1 t + \frac{2\pi}{3} + \varphi_1) \end{bmatrix} \tag{2.62}$$

Similarly, the harmonic components of the load currents can be extracted by filtering the AC components of the 'de-qe' reference frame currents via high-pass filters (HPFs) as illustrated in Figure 2.15. In this case, the designed HPF structures should provide adequate attenuation of DC components while providing unity gain for the minimum frequency components (for $6\omega_1$) of 'de-qe' reference frame currents. In the case of unbalanced load currents, the cut-off frequency of HPFs should be low for the extraction of negative sequence load currents at $2\omega_1$. Although practical HPFs provide unity gain at their pass-bands, there exists a phase difference between the input signals and output signals. This results in inaccurate extraction of harmonic components (the inaccurate current reference for PAF). To avoid this problem, the HPF structure can be implemented as the complementary (1-LPF) structure for the harmonic current extraction via SRFC as in Figure 2.16. Since the LPFs extract the DC signals in 'de-qe' reference frame, the phase error between input and output signals is zero, and the 1-LPF structure extracts the harmonic components without any phase error [13], [23]. The LPFs in the structure have same characteristics as the case of LPFs for the fundamental components extraction via SRFC. With the cut-off frequency of 5-20 Hz, the LPFs should have maximally flat gain characteristics at their pass-band and provide adequate attenuation of the first AC components at $6\omega_1$ or at $2\omega_1$ in the case of unbalance.

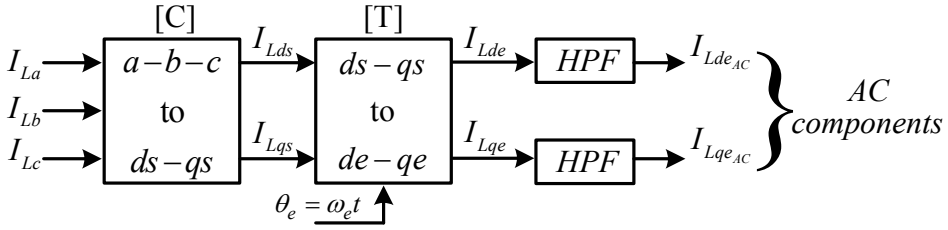

Figure 2.15 The extraction of harmonic frequency components via SRFC.

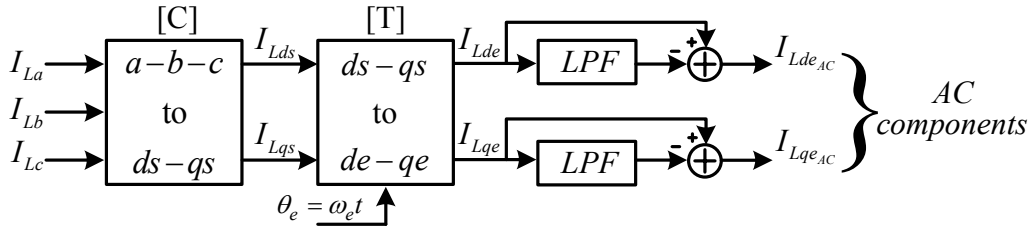

Figure 2.16 The extraction of harmonic frequency components by utilizing 1-LPF structure via SRFC.

By assuming ideal 1-LPF structures in Figure 2.16, the harmonic components of the load currents in 'de-qe' reference frame given in (2.60) can be extracted and can be transformed to 'ds-qs' reference frame via the matrix T^{-1} in (2.43) and obtained as in (2.63). Then, 'ds-qs' frame currents in (2.63) are transformed to 'a-b-c' reference frame via the matrix C^{-1} in (2.28) and obtained as in (2.64). The obtained harmonic components via SRFC in (2.64) are exactly the same as the harmonic components of the load currents in (2.50). Contrary to the IRPT, the generated harmonic current references do not include any frequency components other than the expected frequencies due to pure sinusoidal nature of the unit vectors '$\sin\theta_e$' and '$\cos\theta_e$' in matrix T and T^{-1} [13].

$$\begin{bmatrix} I_{Lds} \\ I_{Lqs} \end{bmatrix}_{AC} = \begin{bmatrix} \hat{I}_{L5}\sin(5\omega_1 t + \varphi_5) \\ \hat{I}_{L5}\cos(5\omega_1 t + \varphi_5) \end{bmatrix} + \begin{bmatrix} \hat{I}_{L7}\sin(7\omega_1 t + \varphi_7) \\ -\hat{I}_{L7}\cos(7\omega_1 t + \varphi_7) \end{bmatrix} \tag{2.63}$$

$$\begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix}_{AC} = \begin{bmatrix} \hat{I}_{L5}\sin(5\omega_1 t + \varphi_5) \\ \hat{I}_{L5}\sin(5\omega_1 t + \frac{2\pi}{3} + \varphi_5) \\ \hat{I}_{L5}\sin(5\omega_1 t - \frac{2\pi}{3} + \varphi_5) \end{bmatrix} + \begin{bmatrix} \hat{I}_{L7}\sin(7\omega_7 t + \varphi_7) \\ \hat{I}_{L7}\sin(7\omega_7 t - \frac{2\pi}{3} + \varphi_7) \\ \hat{I}_{L7}\sin(7\omega_7 t + \frac{2\pi}{3} + \varphi_7) \end{bmatrix} \tag{2.64}$$

Harmonic current extraction via the positive sequence SRFC includes the harmonic current and negative sequence components of the load current. Since the 'qe' axis DC component in 'de-qe' reference frame gives the reactive power component of load current, this component can be included to the reference signal by eliminating the 1-LPF structure in 'qe' axis as shown in Figure 2.17. With the utilization of this structure which is shown in Figure 2.17, the extracted signal will include the harmonic components, reactive power component, and negative sequence component of the load current. Provided that the active filter provides exact compensation for the reference signal, such an implementation results in harmonic free, in-phase and a balanced line current.

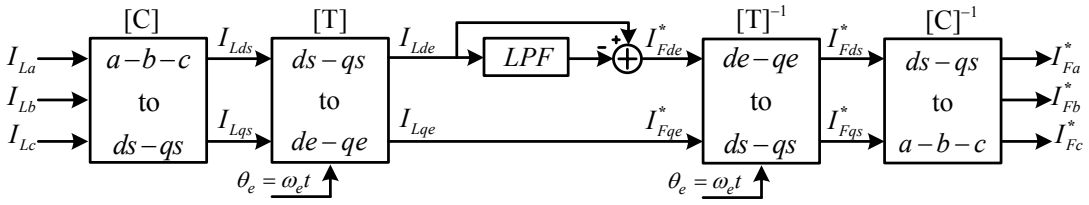

Figure 2.17 The extraction of harmonic frequency components and reactive power component of the load current via SRFC.

If the negative sequence component of the load current is desired to be excluded in the reference current for the PAF, a negative sequence SRFC should be implemented as a parallel structure to positive sequence SRFC as illustrated in Figure 2.18 [13], [23]. The negative sequence SRFC transforms the 'ds-qs' reference frame current to negative sequence 'de-qe' frame with matrix T of (2.42) utilizing $-\theta_e$ instead of θ_e. With these transformations, the negative sequence fundamental frequency components of the load currents appear as DC quantities while the positive sequence and the harmonic frequency components of the load currents appear as AC quantities. By LPF structures, the negative sequence fundamental frequency components can be extracted. The extracted components can be transformed back to 'ds-qs' reference frame with matrix T^{-1} of (2.43) utilizing $-\theta_e$ instead of θ_e. If the reference signals of the negative sequence SRFC in 'ds-qs' frame are subtracted from the reference signals of positive sequence SRFC in 'ds-qs' frame, the obtained signals do not include the negative sequence fundamental frequency components of the load current. This will avoid the compensation of the negative sequence load current components and reduce the rating of the PAF [13], [23].

The above discussion reviewed the basic principle and the implementation issues of SRFC in extracting the current references for the PAF application. Moreover, the accuracy of the extracted signals is illustrated by case studies and different reference signals are generated by appropriate filtering and utilizing the positive and negative sequence controllers. The two well known time domain methods for harmonic current extraction in the PAF application are analyzed. The limitation of IRPT and the superior performance of the SRFC in current reference generation are illustrated.

This section completes the discussion of the harmonic current reference generator part of the current reference generator block in Figure 2.8.

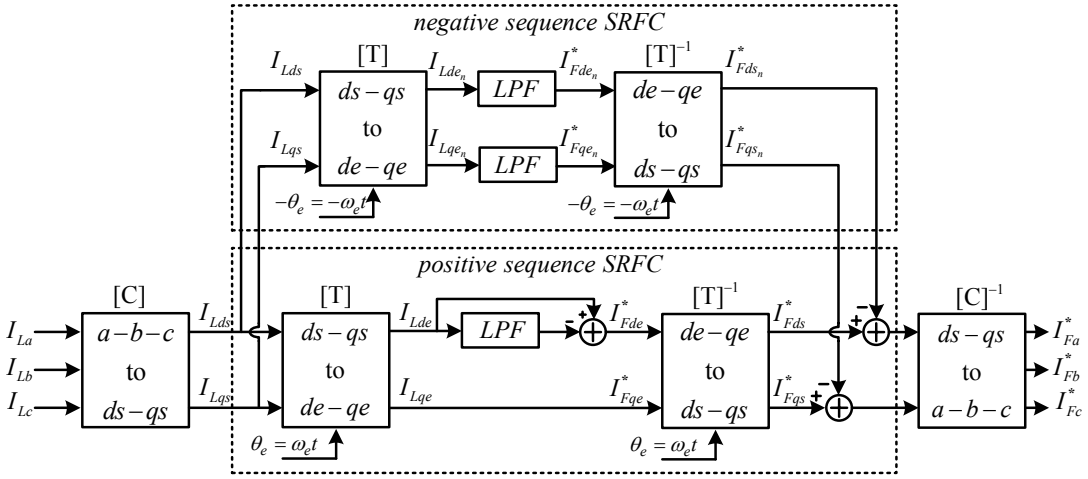

Figure 2.18 Elimination of negative sequence component of the load current via negative sequence SRFC.

2.3.2 DC Bus Voltage Regulator

In addition to compensating the load harmonics, reactive power, and load unbalance currents, the PAF control algorithm should create a current reference in order to regulate the DC bus voltage to its reference value and compensate for the losses of VSI. As a DC bus voltage regulator, a PI regulator shown in Figure 2.19 is utilized to generate a fundamental current reference I^*_{Fdc} for the regulation of the DC bus voltage to its reference value V^*_{dc} and the compensation of VSI losses. The feedback signal of the DC bus voltage V_{dc} requires filtering since the PAF DC bus voltage has dominant voltage ripple at $6\omega_1$ (300 Hz) and its multiples. Because, the filter current consists of load current harmonics of which the 5th and 7th are dominant. At the DC bus, these currents are transformed to 300 Hz AC components since the 5th harmonic current is a negative sequence current while 7th harmonic current is a positive sequence current. Unless the ripple on the feedback signal is filtered, the PI regulator creates a current reference for the dominant 300 Hz components and its multiples.

This results in inaccurate reference for the harmonic current compensation since the DC bus voltage regulator output signal is added to the output signal of the harmonic current reference generator. The cut-off frequency and the order of the LPF is selected to magnitude of voltage ripple and the adequate attenuation of the dominant 300 Hz ripple on DC bus voltage. However, the low cut-off frequency and higher order LPFs will result in slower transient response. Although the DC bus capacitor is sized to the desired voltage ripple, another constraint for DC bus capacitor is the rms value of the current passing through DC bus. In the PAF application, large size DC bus capacitor is utilized due to rms value of the current, which results in small voltage ripple. Therefore, in the DC bus voltage feedback low-pass filter, lower order LPFs with cut-off frequency of 20-100 Hz can be utilized. The gains of the PI regulator in DC bus voltage regulator can be obtained by deriving the mathematical model of the system [27] or experimentally via trial and error.

Since the regulation of the DC bus voltage and compensation of the VSI losses requires real power transfer from the AC utility grid at fundamental frequency, the obtained current reference from the DC bus voltage regulator is added to the 'de' axis current reference component of the harmonic current reference generator as shown in Figure 2.20. The block diagram in the figure illustrates the current reference generator consisting of the harmonic current reference generator and DC bus voltage regulator, which generates the total current reference of the PAF that compensates for load current harmonics, reactive power current component, and negative sequence current component and regulates its DC bus voltage. The generated current reference of the PAF is then sent to the current controller, which generates the switching signals for the VSI to form the desired current at the PAF output terminal.

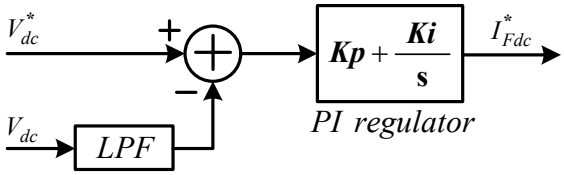

Figure 2.19 The PI compensator based DC bus voltage regulator of the PAF.

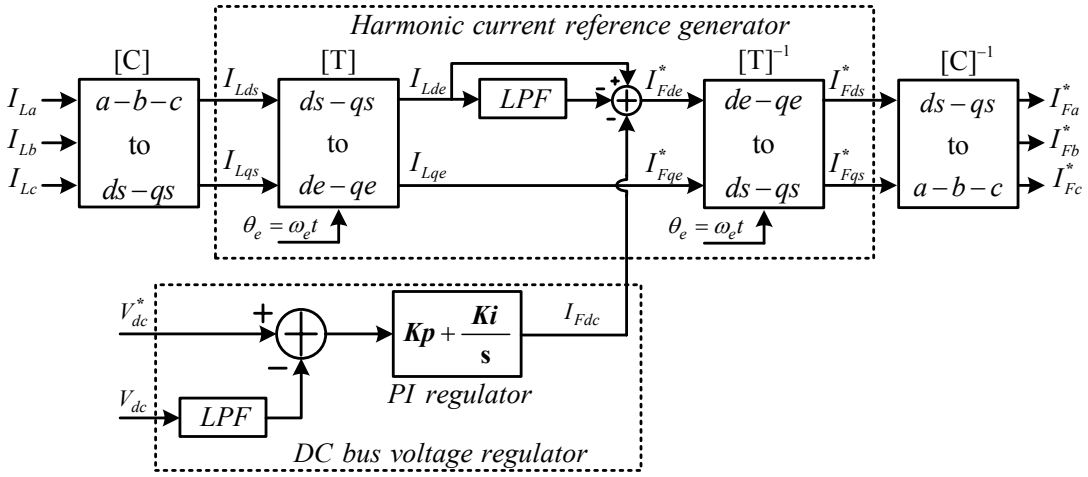

Figure 2.20 The complete control block diagram of the current reference generator in PAF application.

2.3.3 Current Controller

The accuracy of the generated current reference is a critical issue in the performance of the current controlled PAF. However, the realization of the PAF implemented as a current generator is fully determined by the current controller since it creates the switching signals to VSI which chops the DC bus voltage to obtain the desired AC voltage at the output terminal. The generated AC voltage creates the PAF current via the filter coupling inductors. If the current regulator is ideal, the PAF current becomes equal to the reference and the compensation becomes perfect. Hence, the current controller is the most critical part in high performance current controlled applications as in the PAF case. Since the PAF is mainly designed to inject a current to the power system at the PCC for compensation of load current harmonics, the PAF reference current is the load current harmonics, which is characterized by its non-sinusoidal multiple frequency and high di/dt specifications. Figure 2.21 illustrates a typical load current and its harmonic content, which is the PAF current reference. To track the non-sinusoidal, multiple frequency, and high di/dt current reference properly, the current controller should have a high current controller bandwidth and resolution. A high bandwidth and high di/dt current tracking requires small filter inductance value and high switching frequency. However, the switching frequency is

limited due to the thermal stability of the system. Limited switching frequency results in low frequency current errors in low inductance applications, therefore limited bandwidth. The above requirements for the current controller in PAF application result in a challenging control problem and require special design considerations. The current controller, which is the most critical part of PAF, is analyzed in detail in the next chapter. Following a detailed literature survey of current controller architectures in the PAF application, design issues and implementations will be investigated. However, at this stage it is relevant to discuss the PAF ratings.

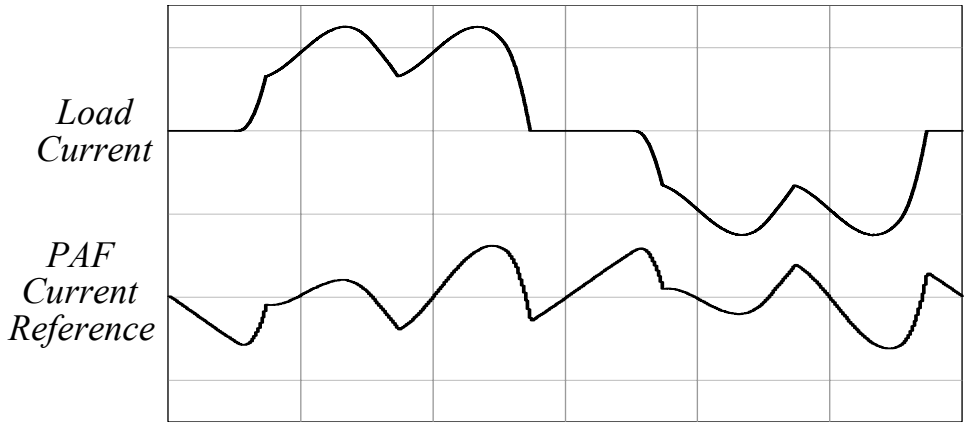

Figure 2.21 The typical load current and PAF current reference in a PAF application.

2.4 Parallel Active Filter Ratings

The determination of the closed-form expression of PAF ratings is not a simple task, since the filter current consists of harmonics and reactive power component of the load current when the PAF is applied to harmonic current source type non-linear load and implemented as a current source. Therefore, the closed-form expression of PAF rating is approximated by making some assumptions [28], [29]. In this rating analysis, the nonlinear load is assumed to be a harmonic current source type rectifier with a constant DC side current of I_{dc} and AC side current with a displacement power factor angle of φ_1. Moreover, the PAF implemented as a current source which compensates

the whole harmonic and reactive current components of load such that the line (source) current is purely sinusoidal at the fundamental frequency and in phase with the voltage at PCC. In this case the line current is expressed as follows:

$$i_S(\omega t) = \sqrt{2}\mathrm{I_S}\sin(\omega_1 t) = \sqrt{2}\mathrm{I_{S1}}\sin(\omega_1 t) \tag{2.65}$$

Figure 2.22 illustrates the AC side current of the rectifier $i_L(\omega t)$, the line current $i_S(\omega t)$, and filter current $i_F(\omega t)$ waveforms which are utilized in rating analysis of a PAF. If the rectifier input current $i_L(\omega t)$ is expressed by fourier series as

$$i_L(\omega t) = \sqrt{2}\mathrm{I_{L1}}\sin(\omega_1 t)\cos(\varphi_1) - \sqrt{2}\mathrm{I_{L1}}\cos(\omega_1 t)\sin(\varphi_1) + \sum_{h\neq 1}\sqrt{2}\mathrm{I_{Lh}}\sin(\omega_h t - \varphi_h) \tag{2.66}$$

the line current, the rms value of its fundamental component, and the filter current are expressed as follows:

$$i_S(\omega t) = \sqrt{2}\mathrm{I_{L1}}\sin(\omega_1 t)\cos(\varphi_1) \tag{2.67}$$

$$\mathrm{I_{S1}} = \mathrm{I_{L1}}\cos(\varphi_1) \tag{2.68}$$

$$\begin{aligned} i_F(\omega t) &= i_L(\omega t) - i_S(\omega t) \\ &= -\sqrt{2}\mathrm{I_{L1}}\cos(\omega_1 t)\sin(\varphi_1) + \sum_{h\neq 1}\sqrt{2}\mathrm{I_{Lh}}\sin(\omega_h t - \varphi_h) \end{aligned} \tag{2.69}$$

The first term in (2.69) corresponds to the reactive current component of the load current while the second term corresponds to the load current harmonics. From (2.69), the rms value of filter current $\mathrm{I_F}$ is found as

$$\mathrm{I_F} = \sqrt{\mathrm{I_{L1}^2}\sin^2(\varphi_1) + \sum_{\mathrm{h}\neq 1}\mathrm{I_{Lh}^2}} \tag{2.70}$$

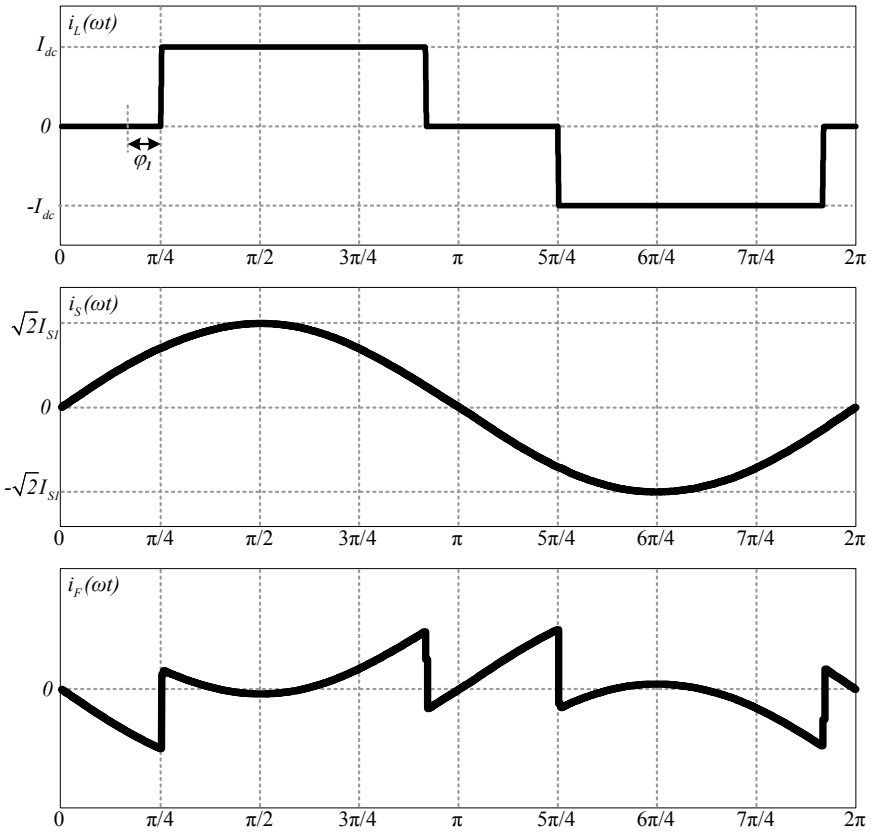

Figure 2.22 Load, line, and PAF current waveforms utilized in rating analysis of PAF.

If the sum of the load current harmonic rms values (second term in (2.70)) and the load current rms value I_L in this case is expressed in terms of rms value of load current fundamental component I_{L1} as

$$\sum_{h\neq 1} I_{Lh}^2 = I_L^2 - I_{L1}^2 \tag{2.71}$$

$$I_L = \frac{\pi}{3} I_{L1} \tag{2.72}$$

the filter current rms value is obtained from (2.70), (2.71), and (2.72), as

$$I_F = I_{L1}\cos(\varphi_1)\sqrt{\left(\frac{\pi}{3\cos(\varphi_1)}\right)^2 - 1} \tag{2.73}$$

By assuming that the voltage at the PCC given as

$$v_S(\omega t) = \sqrt{2}\mathrm{V}_{\mathrm{S1}} \sin(\omega_1 t) \tag{2.74}$$

is purely sinusoidal, the rectifier output power $\mathrm{P}_{\mathrm{out}}$ is expressed in terms of supply voltage and supply current rms values as

$$\mathrm{P}_{\mathrm{out}} = 3\mathrm{V}_{\mathrm{S1}}\mathrm{I}_{\mathrm{S1}} = 3\mathrm{V}_{\mathrm{S1}}\mathrm{I}_{\mathrm{L1}} \cos(\varphi_1) \tag{2.75}$$

Since the PAF is connected to utility grid at the PCC, the PAF apparent power $\mathrm{S}_{\mathrm{PAF}}$ from (2.73) and (2.75) is given as

$$\mathrm{S}_{\mathrm{PAF}} = 3\mathrm{V}_{\mathrm{S1}}\mathrm{I}_{\mathrm{F}} = \mathrm{P}_{\mathrm{out}} \sqrt{\left(\frac{\pi}{3\cos(\varphi_1)}\right)^2 - 1} \tag{2.76}$$

The equation (2.76) expresses the PAF VA rating in terms of only the output power of the harmonic current source type rectifier and the displacement power factor angle φ_1. In the case of a diode rectifier, the displacement power factor angle φ_1 is approximately zero; therefore the PAF VA rating given by (2.76) is a simple expression only related to only $\mathrm{P}_{\mathrm{out}}$. For instance, the PAF VA rating is approximately 3.1 kVA for a diode rectifier with an output power of 10 kW. However, if the displacement power factor angle is increased, the PAF VA rating increases since the PAF also compensates the fundamental reactive power current component of the nonlinear load in this case. For instance, the PAF VA rating is approximately 6.8 kVA for a thyristor rectifier with an output power of 10 kW and firing angle of 30°. Compared to the diode rectifier case, the PAF VA rating is increased considerably. Therefore, the PAF cannot be a cost effective solution for the nonlinear load with a high displacement power factor angle. In such a case, the PWM rectifier may constitute a cost effective solution [28]. The selection of the topology for nonlinear loads with a high displacement power factor angle depends on the characteristic of the nonlinear load and the cost of the topology, which is the beyond the scope of this thesis.

The equation (2.76) for the PAF VA rating is derived by making too many assumptions and approximations. However, it is illustrated in [28] and [29] such that the value given by (2.76) is a good approximation to the practical PAF VA rating.

2.5 Summary

The characteristics of the harmonic producing loads are critical in the PAF application, since the performance of the PAF designed for the compensation of the load current harmonics, the reactive power component, the negative sequence component in 3-phase 3-wire applications depends on whether the nonlinear load type is a harmonic current source or harmonics voltage source. When it is implemented as a current source and applied to the harmonic current source type nonlinear loads, the PAF compensation characteristics are independent of the source and the load side parameters and are fully determined by the PAF transfer function. The PAF transfer function is realized by its control block which consists of two main blocks of current reference generator and current controller. The detailed control block diagram of the PAF is illustrates in Figure 2.23. The current reference generator creates the compensation reference signals via the harmonic current reference generator and the fundamental frequency current reference for the DC bus voltage regulation via the DC bus voltage regulator. The desired compensation signals (load current harmonics, reactive power component, and/or negative sequence component) are extracted via the synchronous reference frame controller, which utilizes the measured load currents and the phase angle information of the AC utility grid derived via the vector phase locked loop. The desired compensation signals are added to the DC bus voltage regulator current reference to form the PAF total current reference signal. Once the PAF current reference is created, the current controller regulates the reference signal via the feedback signals of the PAF output currents and creates the switching signals for the VSI that forms AC voltages at the its output terminals and hence the desired currents through the filter inductors. The injected current from the PAF to the power system at the PCC cancels the load current harmonics, reactive power component and/or negative sequence component depending upon its compensation current reference.

In this chapter, the characteristics of the harmonics producing nonlinear loads and the application consideration of the PAF to these loads are analyzed. The control architecture of the PAF is presented in detail. The important issues in PAF current reference generation are highlighted and the current controller part is summarized. Moreover the PAF VA rating is derived as a closed form expression in terms of nonlinear load output power and the displacement power factor angle. The next chapter analyzes the current controller part of the PAF control in detail.

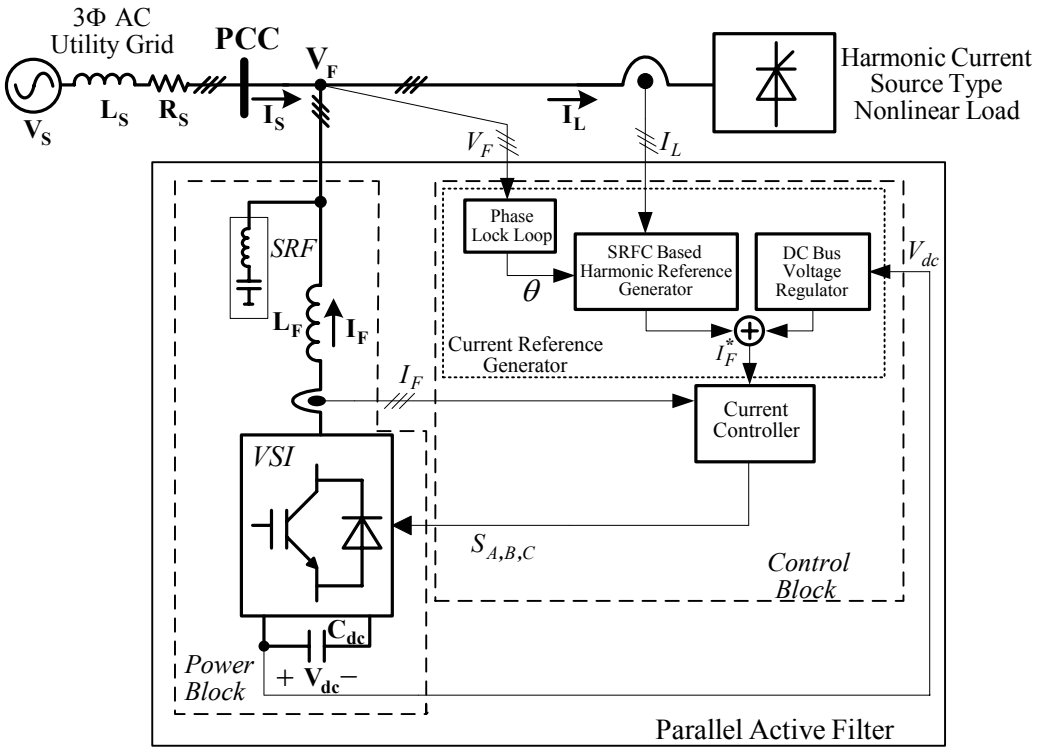

Figure 2.23 The detailed control block diagram of the PAF.

CHAPTER 3

CURRENT REGULATORS FOR THE PARALLEL ACTIVE FILTER APPLICATION

3.1 Introduction

The parallel active filter, of which power circuit diagram is illustrated in Figure 3.1, is operated as a controlled current source such that it injects a current to the power system at the PCC for the compensation of the load current harmonics, fundamental reactive power component and negative sequence component. Therefore the reference current of the PAF consists of the harmonics, fundamental reactive power component and negative sequence component of the load current. The reference current, as discussed in the previous chapter, is characterized by its non-sinusoidal multiple frequency and high di/dt properties. Once the reference current is generated accurately, it is the current controller (regulator) part that achieves the tracking of this reference. Thus, the tracking capability of the current regulator determines the performance of the PAF. Hence, the current regulator is the most critical part of the PAF.

This chapter first discusses the current regulator requirements and reviews the state of the art PAF current regulators. The analysis of the state of the art current controllers is included under the subsections of the linear current regulators and the on-off current regulators. The linear current regulators are discussed under the subsections of linear proportional gain current regulator (LPCR), charge error current regulator (CECR), and resonant filter current regulator (RFCR), which are reported to be utilized in industrial applications. The design of the linear current controllers for the PAF is analyzed in detail by modeling the system. Then, the on-off current

regulators showing superior current tracking performance are analyzed and discrete time implementation of the hysteresis current regulator is investigated. The improvements on the discrete time hysteresis current regulator to increase the bandwidth and to achieve thermal stability are given for the PAF application.

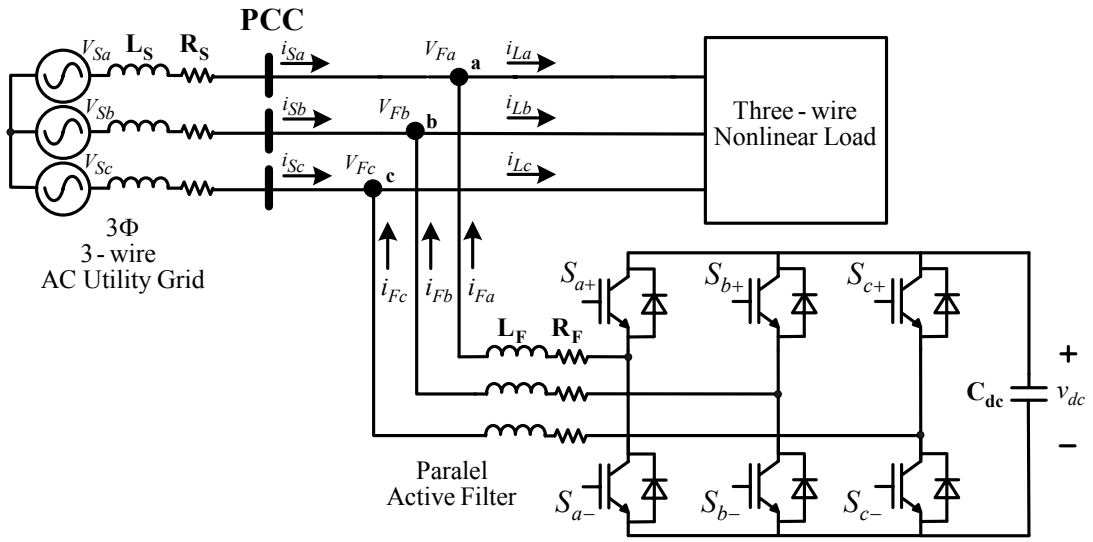

Figure 3.1 Power circuit of the parallel active filter.

3.2 The Requirements and Review of Current Regulators for The PAF Application

The realization of a current regulator in the PAF application brings some requirements since it is the most critical part of the PAF. The current regulator in the PAF application should be able to track non-sinusoidal multiple frequency and high di/dt current reference. The high frequency current reference signals have small magnitude. Therefore, the PAF application requires a high current regulator bandwidth and resolution for the tracking of the high frequency harmonics. The high bandwidth and high di/dt current tracking capabilities result in a small filter inductance (L_F) value. Therefore, the designed current regulator is able to operate with low filter inductance values (typically L_F < 5%). The performance of the designed current regulator should not be sensitive to system parameter values such as L_F and to the voltage at the PCC (V_F). Moreover, a high switching frequency is

required for a high bandwidth. However, the implemented current regulator should restrict the switching frequency (f_{SW}) for thermal stability of the system and the limited switching frequency results in high frequency current errors in low inductance applications, therefore limited bandwidth. Also, its implementation should be as simple as possible, practically applicable and allow discrete time implementation due to the control flexibility and robustness advantages of the discrete time control over the analog one. The above mentioned requirements for a current regulator in PAF application are utilized as criteria for the choice of the current regulator [13], [23], [30].

The realization of a PAF connected to the power system at the PCC as a current source is achieved by a VSI and three-phase filter inductors. The mathematical model of the filter inductor between AC utility grid and VSI is an integrator representing a delay. Therefore, the current regulator for a PAF should not be an integral type regulator for tracking of the high frequency current reference. As a result, among the existing current regulators, synchronous and stationary frame based PI current regulators are not viable solutions due to their limited bandwidth for the PAF application [30]. Predictive methods in the literature involve system parameters which are often not accurately known. Also, their implementations are generally complex and unsuitable for today's desired high switching frequency applications [13]. The methods based on the derivative control seem to be viable solution for this application. However, derivative controllers are unsatisfactory in applications due their sensitivity to noise problems. In practice, the linear proportional gain current regulator (LPCR) is widely utilized [10] and the practical application of charge error based current regulator (CECR) is reported in [13], [23]. Although the charge error part of CECR includes an analog integrator, its integrator is resetted at high rate and it is analyzed in this thesis due to its announced superior performance and comparison reasons. Implemented for the selective harmonic compensation of the load current, the recently reported resonant filter current regulator (RFCR) for the PAF illustrates high bandwidth and superior compensation characteristics at steady state for the well defined load current harmonics [31]. Therefore, LPCR, CECR and RFCR seem to be viable and practically applicable choices for the PAF application.

The common property of these current regulators is the generation of an average voltage reference to be synthesized by the carrier based PWM modulator and they are classified as the linear current regulators.

Hysteresis current regulators are on-off type current regulators and widely utilized for tracking of non-sinusoidal, multiple frequency and high di/dt current references. When analog implementation is utilized, hysteresis current regulators exhibit high bandwidth and superior tracking capability of the reference currents with high di/dt. Moreover, the discrete time implementation of some parts of hysteresis current regulators to obtain several advantages of discrete time solutions and their satisfactory performance are reported in the literature. Although their well known drawbacks such as variable switching frequency and phase interaction, their superior tracking performance makes hysteresis current regulators viable solutions for the PAF application [13], [30], [32], [33].

Viable current regulator solutions in PAF application classified as the linear and the on-off current regulators are analyzed in the next two sections respectively in terms of their advantages, implementation issues and application complexity.

3.3 Linear Current Regulators

The basic principle of the linear current regulators is shown in Figure 3.2. The difference between the current reference and the current feedback constitutes the current error signal which is converted to the inverter voltage reference via the linear current regulator. The inverter voltage reference is synthesized by carrier based PWM modulator, which is discussed later. The modulator creates the switching signals for the VSI to form the desired current through the filter inductor which is connected between the VSI output terminals and AC utility grid. The advantage of the linear current regulators involves the carrier based PWM modulator implementation. In the carrier based implementation, the switching frequency f_{SW} can be adjusted to a fixed value. The fixed f_{SW} results in well defined switching current harmonics on the current waveform. The switching current harmonics for a

fixed value of f_{SW} appear at the frequency of f_{SW} and multiple frequencies of f_{SW}. Also, the fixed f_{SW} is kept high to achieve high bandwidth in PAF application. Therefore, since the frequency of the switching harmonics is known and high, the elimination of them is simple by a simple passive switching ripple filter structure at the output terminals of the PAF (This topic is discussed in the following chapter). Another advantage of fixed f_{SW} is that the thermal reliability is achieved due to known value of f_{SW}. The drawback of PWM implementation is that a sudden change of the reference signal (a characteristic attribute in the PAF application) results in unavoidable delay nearly equal to one or one-half carrier period (PWM period = T_S = $1/f_{SW}$) depending on the utilized PWM implementation technique [30]. Therefore, the switching frequency is kept as high as possible to overcome this drawback while considering thermal stability and capability limits of semiconductor switches on the other hand.

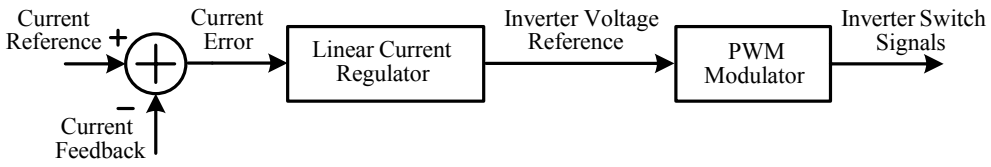

Figure 3.2 Basic principle of linear current regulators.

The practically utilized linear current regulators for the PAF application are LPCR, CECR and RFCR. Before the analysis of the mentioned current regulators, the PWM modular, which is indispensable part of the linear current regulators, will be investigated.

3.3.1 The PWM Modulator

In the PAF application, a controllable AC voltage is required at the output terminals of the VSI to create voltage difference across the filter inductor and hence, to achieve a controllable current. The AC voltage reference (inverter voltage reference) created by the linear current regulators is synthesized by carrier based PWM modulator that

employs the per-carrier cycle volt-second balance principle to generate rectangular output voltage pulses that meet the output voltage requirement. Given the reference voltage, the inverter switches should be manipulated such that the reference volt-seconds and output volt-seconds must be equal over each PWM cycle. PWM method to generate the switching signals for the inverter switches operate based on this principle. The modulation methods for the PWM are divided into two main groups; scalar PWM and space vector PWM. In the scalar PWM method, the voltage reference wave (modulation wave) is compared with a triangular carrier wave and the intersections define the switching instants for the switches of VSI. In the space vector PWM method, the switch on-state durations are calculated from the complex number volt-seconds balance equation for the inverter voltage and the switch pulse pattern is programmed via digital PWM hardware/software. Being the simplest method, the scalar PWM methods are commonly preferred.

A variety of scalar PWM methods have appeared in the technical literature due to the simplicity of the volt-second balance principle. Each method results from a unique placement of the voltage pulses in isolated neutral type loads [34]. In the three-phase motor drive and AC utility grid connected applications where the neutral point is isolated and no neutral current path exists, any zero-sequence signal can be added to the modulation wave to extend the volt-second linearity range of the PWM due to limited DC bus voltage, to improve the output waveform quality, and/or to reduce switching losses. The general block diagram of the zero-sequence injection method for the scalar PWM methods is illustrated in Figure 3.3. Adding a zero-sequence signal (v_o) shifts the three reference signal (v_a^*, v_b^*, v_c^*) in vertical direction and changes the switching instants and hence the position of the output line-to-line voltage pulses. However, the width of these pulses remains same and the volt-second principle is preserved, where the Figure 3.4 illustrates the time lengths of switching signals and the line-to-line output voltage waveform over a PWM cycle.

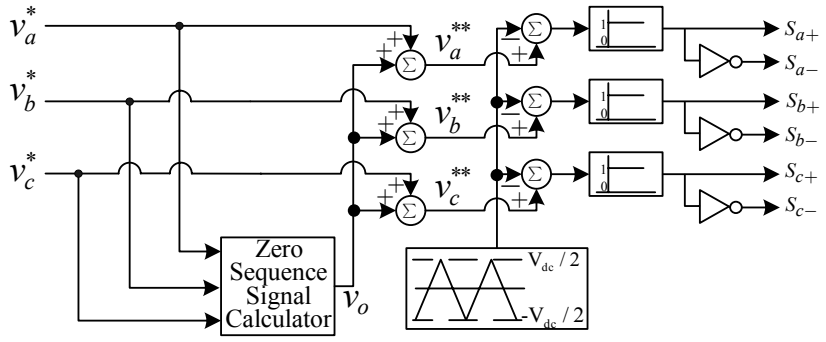

Figure 3.3 The general block diagram of the zero-sequence signal injection in triangular-based PWM.

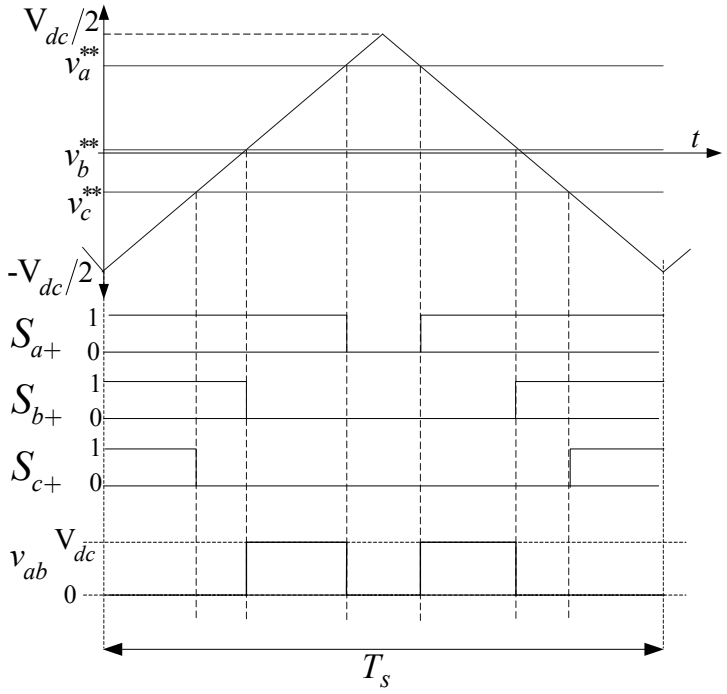

Figure 3.4 The modulation, carrier, and switching signals and output line-to-line voltage over a PWM cycle.

Although an infinite number of zero-sequence injection PWM methods can be derived theoretically, a few well known scalar PWM methods have gained acceptance due to the performance and simplicity constraints of the PWM-VSI. Further, these well known scalar PWM methods are classified into two groups; Continuous PWM (CPWM) methods and Discontinuous PWM (DPWM) methods. While in the linear modulation range, the modulation waveforms of the CPWM

methods are always within the peak limits of the carrier-wave and therefore switchings always occur. In the DPWM methods, the modulation wave is clamped to positive or negative DC rail for one segment; therefore the switching does not occur for that segment which results in no switching losses. The choice of them is application and performance dependent. For instance, the triangle intersection implementation of space-vector PWM (SVPWM) is commonly utilized as a CPWM method in the applications operating at low modulation index due to its waveform quality. However, applications operating at high-modulation range favor DPWM methods due to their lower switching losses [34]. Therefore, for the utility grid connected applications as in the case of the PAF, DPWM methods are preferable. Although many DPWM methods exist, the classical DPWM method (DPWM1) for the three-leg inverter is well known and simple. In the DPWM1 method, the original modulation waves (v_a^*, v_b^*, v_c^*) are compared and the one with the largest magnitude is considered as the phase to be locked. The zero-sequence signal is the difference between the DC rail voltage and the modulation signal with the largest magnitude based on the polarity of it. Since the zero-sequence signal is added to all the modulation signals, the modulation signal with the largest magnitude is locked to the positive or negative DC voltage while the remaining modulation signals are shifted based on the zero-sequence value. Figure 3.5 illustrates the DPWM1 method with the three-phase balanced sinusoidal original modulation signals (v_a^*, v_b^*, v_c^*), zero-sequence signal (v_o), and the generated modulation signals (v_a^{**}, v_b^{**}, v_c^{**}) over a fundamental cycle. Since each modulation signal is clamped for an angle of 120°, the switch of the associated inverter leg does not perform switching, and hence no switching losses occur. However, the total switching losses are significantly influenced by the DPWM method and load power factor angle. Because, the unmodulated segments of the switch for an angle of 120° over a fundamental cycle together with the magnitude of the current through that switches determines the total switching power loss. For instance, for a unity power application with the sinusoidal output voltages and currents, DPWM1 has the minimum switching loss since the magnitude of the current passing through unmodulated switch has the maximum value. Therefore, the choice of the DPWM method with the high-modulation range applications for the lowest switching loss depends on the current waveform [34]. To

achieve a minimum switching loss, a minimum loss DPWM (MLDPWM) is proposed for a four-leg inverter in UPS application where the unbalanced operation conditions take place [35] and for a three-leg inverter in PAF application where the injected currents has non-sinusoidal multiple frequency characteristics [36]. The principle of the MLDPWM involves clamping of one inverter leg having the maximum current value to the positive or negative DC rail, if the clamp of that inverter leg is permissible. The zero-sequence signal is created accordingly. Figure 3.6 illustrates MLDPWM with the three-phase balanced sinusoidal original modulation signals (v_a^*, v_b^*, v_c^*) and the current waveforms in PAF application (harmonic current references) and the generated zero-sequence signal (v_o), and the generated modulation signals ($v_a^{**}, v_b^{**}, v_c^{**}$) over a fundamental cycle. Note that the inverter leg with maximum current is unmodulated such that switching losses are minimized.

An incremental improvement in switching loss reduction is obtained with the MLDPWM with a bit complex implementation algorithm for the PAF application in [36]. Therefore, the DPWM1 method can also preferred due to its implementation simplicity and comparable switching loss to MLDPWM.

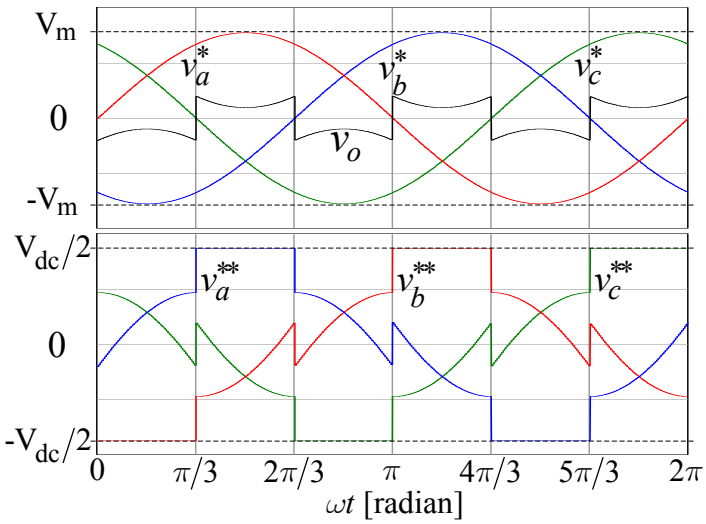

Figure 3.5 The illustration of DPWM1.

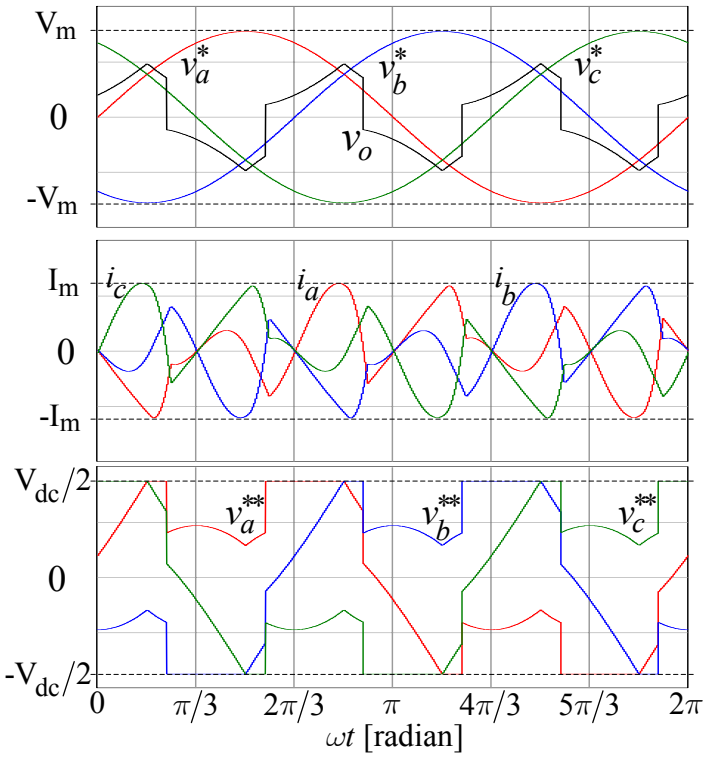

Figure 3.6 The illustration of MLDPWM in PAF application.

3.3.2 The Linear Proportional Gain Current Regulator

The linear proportional gain current regulator allows the application of the carrier based PWM methods by generating an average inverter voltage that matches a reference voltage at a fixed switching period, T_S. The detailed block diagram of LPCR implemented in the 'ds-qs' reference frame is illustrated in Figure 3.7. The regulator generates an average voltage reference on the filter inductance L_F (V_{Fds_FB} & V_{Fqs_FB}, feedback voltage references) to reduce the current error (the error between the reference current and actual current) by multiplying the sampled current error by proportional gain, K_P. The current error can be sampled once (known as single update mode) or twice (known as double update mode) in T_S in discrete time applications using PWM counters depending on the capability of the utilized microcontroller. Double update of the feedback voltage references results in improved tracking capability of the current references with high di/dt. Directly adding the measured line voltage signals (V_{Fds_FF} & V_{Fqs_FF}) known as feed-forward

control to the feedback voltage references, the inverter voltage references (V^*_{Fds} & V^*_{Fqs}) are generated. The feed-forward control signal in the current regulator provides the large proportion of the control signal and reduces the required gain of current regulator loop, therefore increases the stability of the feedback control loop. The obtained inverter voltage references in the 'ds-qs' reference frame are transformed to 'a-b-c' reference frame, and then compared with a triangular carrier wave in the case of analog implementation or PWM counters in the case of discrete time implementation to obtain on-off switching signals for the VSI (S_{a+}, S_{a-},…).

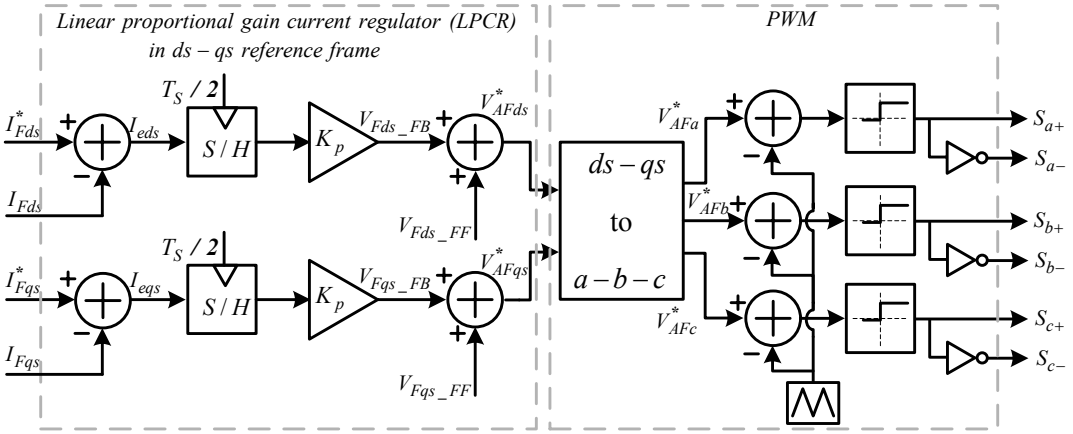

Figure 3.7 Block diagram of the linear proportional gain current regulator (LPCR) in the 'ds-qs' stationary reference frame with the PWM modulator included.

In classical PI controllers, the proportional gain determines the dynamic response of the system to a rapid change in reference signal. The integral gain determines the damping of the system and makes the steady-state error zero if the applied reference is a DC signal. However, the reference signal in the PAF application is a non-sinusoidal, multiple frequency, and high di/dt signal and is referred as a dynamic reference. Therefore, integral control is not beneficial and the proportional gain controller is the most suitable controller for the PAF application.

Proportional gain of the LPCR is determined based on the desired phase margin (φ_m) for the system [37]. The phase margin of a system is defined as the angular distance in degrees to the point where the system stability is lost. In control theory, it is

measured as the difference between the angle where the open loop transfer function gain is unity and -180°. For this purpose, the model of the PAF system is required. Figure 3.8 illustrates the single phase representation of the PAF system connected to the AC utility grid. In the figure, the VSI is modeled by a black box which converts the DC voltage (V_{dc}) into the AC voltage (V_{Finv}) at its output terminals. The VSI is connected to the AC utility grid at the PCC, which is represented by an AC voltage source of V_F, via the filter inductor L_F and resistor R_F. The injected PAF current through the AC utility grid is represented by the current of I_F. The block diagram of the current control loop for the LPCR is illustrated in Figure 3.9 by assuming an ideal VSI. Since the measured AC utility grid voltage (the feedforward voltage V_{F_FF}) is added in the current control loop, which decouples the AC utility grid voltage (V_F), the open loop transfer function of the system utilizing LPCR ($T_{OL}(s)$) is given as in (3.1). Equation (3.1) represents a first order system where the gain is determined by the K_P value. The gain and phase characteristics of the (3.1) is obtained via MATLAB 6.5 [38] for various K_P values, L_F value of 2 mH and R_F value of 250 mΩ and illustrated in Figure 3.10. Also, Figure 3.10 illustrates the phase margin of the system for the considered K_P values. For a feedback control system, if the phase margin is positive, then the system is stable. However, the common design point for systems is the phase margin of 45°. From Figure 3.10, the phase margin for all the K_P values is 90°, which means that the system is always stable for the all K_P values. Theoretically, the high bandwidth values can be obtained for the higher values of K_P in an ideal PAF system. However, the non-idealities for the system (the delays and the discrete nature of the VSI) limit the value of K_P by reducing the phase margin of the system. Moreover, as the current regulator gain is increased, the PWM modulator saturates due to limited DC bus voltage of PAF system. Therefore an accurate model of the PAF system including the non-idealities is required for the determination of the K_P value theoretically.

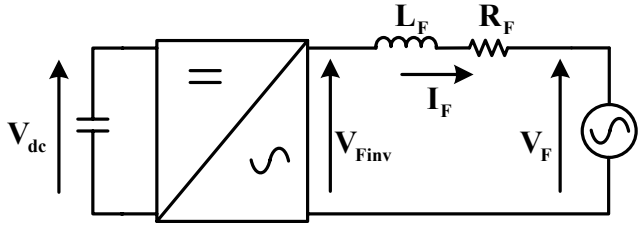

Figure 3.8 The single phase representation of the AC utility grid connected PAF.

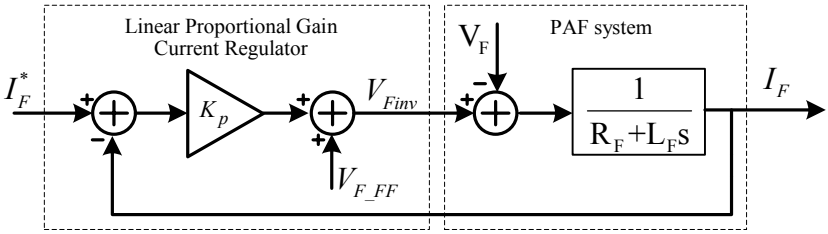

Figure 3.9 The block diagram of the closed current control loop of the LPCR for an ideal PAF system.

$$T_{OL}(s) = \frac{K_P}{R_F + L_F s} \tag{3.1}$$

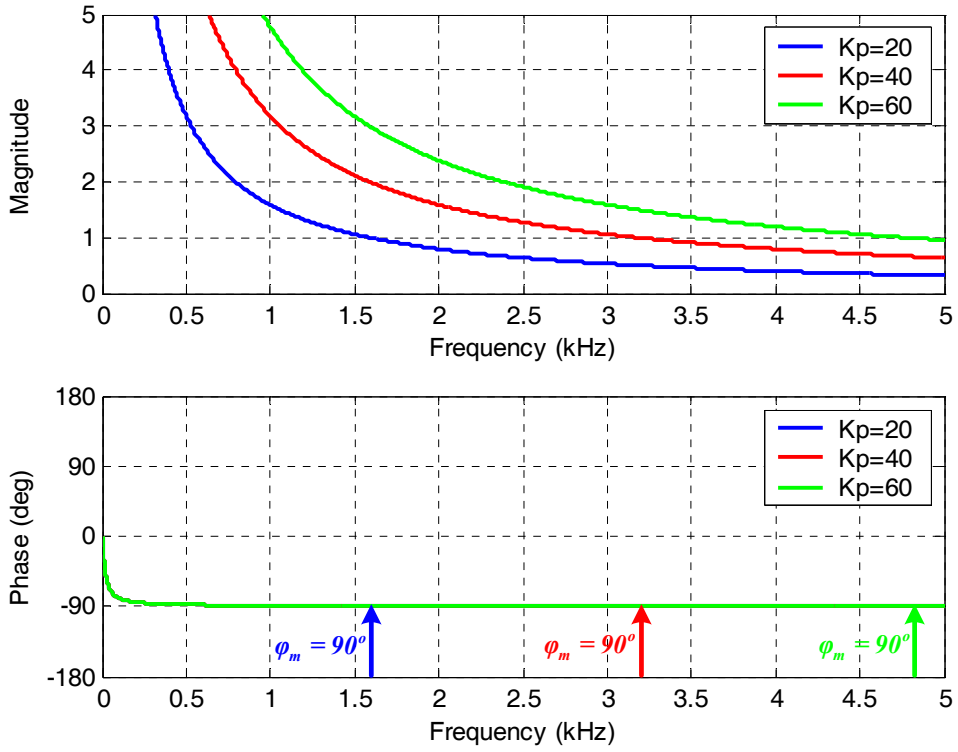

Figure 3.10 The open loop transfer function gain and phase characteristics of the LPCR in an ideal PAF system for various K_P values, L_F=2 mH and R_F=250 mΩ.

The practical application of the PAF involves the system delay originating from the individual delays of the PAF system stages. All these individual delays have significant influence on the phase margin of the system and should be modeled for an accurate design. In practice, there exist a measurement delay ($\tau_{measure}$) occurring at the stage of the measurement and signal conditioning of the feedback signals, signal processor delay (τ_{samp}) due to transferring and processing of the measured signals in the signal processor, and inverter output delay (τ_{PWM}) due to the discrete nature of the VSI. All these individual delays can be mathematically modeled as a first order delay blocks. The block diagram of the PAF current control loop including these individual delay blocks is illustrated in Figure 3.11. These delays are also illustrated with respect to a PWM cycle (T_S) in Figure 3.12. In the PAF current control loop in the Figure 3.11, the main control variables are the filter output currents which are measured by the hall-effect sensor type current transducers with the bandwidth (bw_{lem}) of 200 kHz. This results in a time delay of 5 μs. Moreover, the measured feedback signal is scaled to proper voltage level for the A/D (analog to digital) conversion with an electronic circuit which involves a low pass filter with the cut-off frequency of 150 kHz (6.7 μs time delay). Thus, the total $\tau_{measure}$ in Figure 3.11 and 3.12 is 11.7 μs. For the double update mode PWM, at least a time period of $T_S/2$ is required for the transfer of the measured signals to the microprocessor and processing of these signals in the microprocessor. At least a time period of $T_S/2$ is again required for the single update mode PWM, if the feedback signals are measured at the instant when the triangular carrier or PWM counter has a maximum value as illustrated in Figure 3.12. For the f_{SW} value of 20 kHz, τ_{samp} then becomes 25 μs for both single and double update PWM modes. The PWM block can be presented as a voltage amplifier with unity gain and first order delay element with a PWM time delay (τ_{PWM}). If the PWM signal is updated every half PWM cycle, the PWM delay is a quarter PWM cycle. If the PWM signal is updated once per PWM cycle, the PWM delay is half of a PWM cycle. For the case of single update mode in Figure 3.12, τ_{PWM} is 25 μs for the f_{SW} value of 20 kHz. The sum of all these individual delays is the total delay of τ_T as illustrated in Figure 3.12, which is expressed in the following equation.

$$\tau_{\mathrm{T}} = \tau_{measure} + \tau_{samp} + \tau_{PWM} \tag{3.2}$$

The value of τ_T is 61.7 μs for the individual delays that are discussed above and is approximately 1.2 times of the T_S value of 50 μs. For the sake of simplicity, each delay block in Figure 3.11 can be modeled with an equivalent single delay block with a time constant of τ_T as shown in Figure 3.13 and hence, the order of the system can be reduced [35]. If the first order total delay block with a time constant of τ_T is included to the open loop transfer function for the LPCR in (3.1), the new open loop transfer function becomes as

$$\mathrm{T_{OL}(s)} = \frac{\mathrm{K_P}}{(1+\tau_{\mathrm{T}}\mathrm{s})(\mathrm{R_F}+\mathrm{L_F s})} \tag{3.3}$$

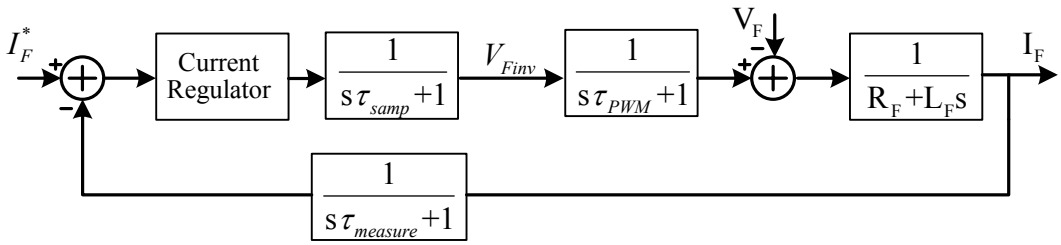

Figure 3.11 The per-phase block diagram of the PAF closed current control loop including the individual delay blocks.

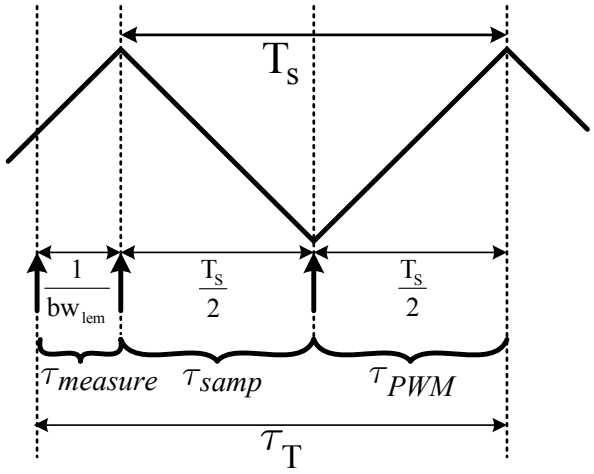

Figure 3.12 The illustration of the system delay elements over a PWM cycle.

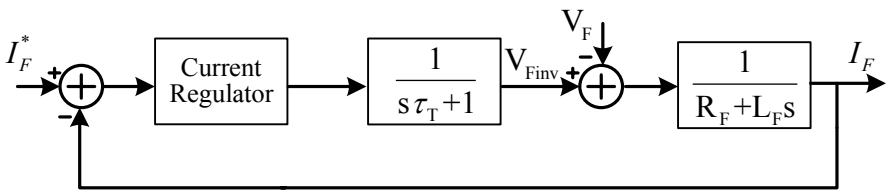

Figure 3.13 The reduced order per-phase block diagram of the PAF closed current control loop.

The gain and phase characteristics of (3.3) is obtained for various K_P values, L_F value of 2 mH and R_F value of 250 mΩ and illustrated in Figure 3.14. Further, Figure 3.14 illustrates the phase margin of the system for the considered K_P values. As the frequency increases, the phase margin of the system decreases for the system including the total delay block contrary to the Figure 3.10, which has constant phase margin for all K_P values. From Figure 3.14, the K_P value of 40, which results in a phase margin of 45°, is the proportional gain of the analyzed system. Based on Figure 3.14, higher values can be selected for the K_P value to achieve a high bandwidth. However, the delays which are not modeled in digital application may result in the excessive degradation of phase margin for the higher values of K_P [37]. Moreover, the saturation of the current controller due to the limited DC bus voltage in practice may result in oscillations for the higher values of K_P. Therefore, the value of K_P should be limited for a stable system.

Since the PAF system is modelled in terms of the system parameters and the implementation delays, the gain and phase characteristics of the system can be obtained for the other values of the system parameters and delays. Moreover, the current controller model in Figure 3.13 can be utilized for the other current regulator in the PAF application.

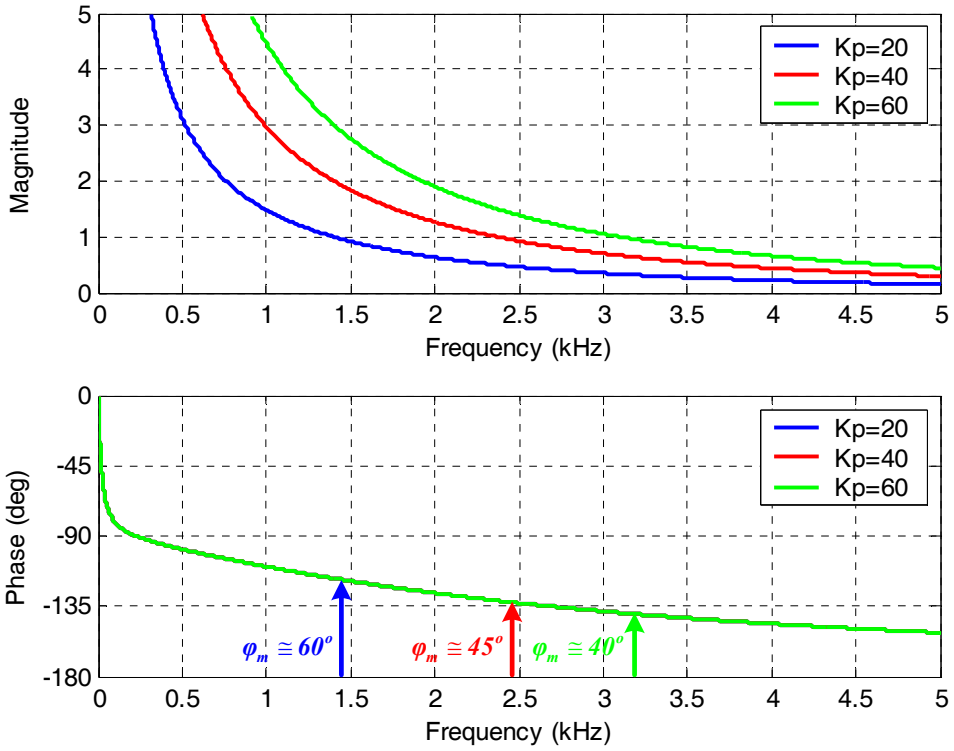

Figure 3.14 The open loop transfer function gain and phase characteristics of the LPCR in the modeled PAF system for various K_P values, L_F=2 mH and R_F=250 mΩ.

3.3.2 The Charge Error Based Current Regulator

The charge error based current regulator allows to the application of the carrier based PWM the same as LPCR. The detailed block diagram of CECR implemented in the stationary 'ds-qs' reference frame is illustrated in Figure 3.15. The proportional gain portion of the CECR updates the voltage reference on the filter inductance L_F twice in T_S as in the LPCR. The charge error portion of CECR aims to reduce the integral of current error (charge error) considering the change of current reference in every T_S and non-idealities of the inverter. The output of the integrator is sampled at every T_S and multiplied by the integral gain (K_I). After each sample, the integrator is reset to avoid the saturation of it. The charge error part can be analyzed as a correction part for the reference voltage signal of the next switching period. The references from the proportional controller and the charge error portion generate the feedback voltage references (V_{Fds_FB} & V_{Fqs_FB}) and are added to the measured line voltage signals

(V_{Fds_FF} & V_{Fqs_FF}) as in the LPCR to create the inverter voltage references (V^*_{Fds} & V^*_{Fqs}). The generated inverter voltage references in the 'ds-qs' stationary reference frame are transformed to the 'a-b-c' reference frame, and then the on-off switch signals for the VSI (S_{a+}, S_{a-},…) are obtained by the PWM modulator as in the LPCR. The proportional gain of the CECR (K_P) is defined as $\hat{L}_F/(T_S/2)$ for the sampling of the current error twice in per PWM cycle as in a conventional predictive controller, where $\hat{L}_F$ is the estimated value of the filter inductor L_F [12]. An observation can be performed such that if sampling is performed once per PWM cycle, the K_P value of CECR can be reduced to $\hat{L}_F/T_S$, which is 40 for L_F value of 2 mH and T_S value of 50 μs in 20 kHz switching application. The obtained value of K_P is the same as the value of K_P in LPCR for a phase margin of nearly 45°.

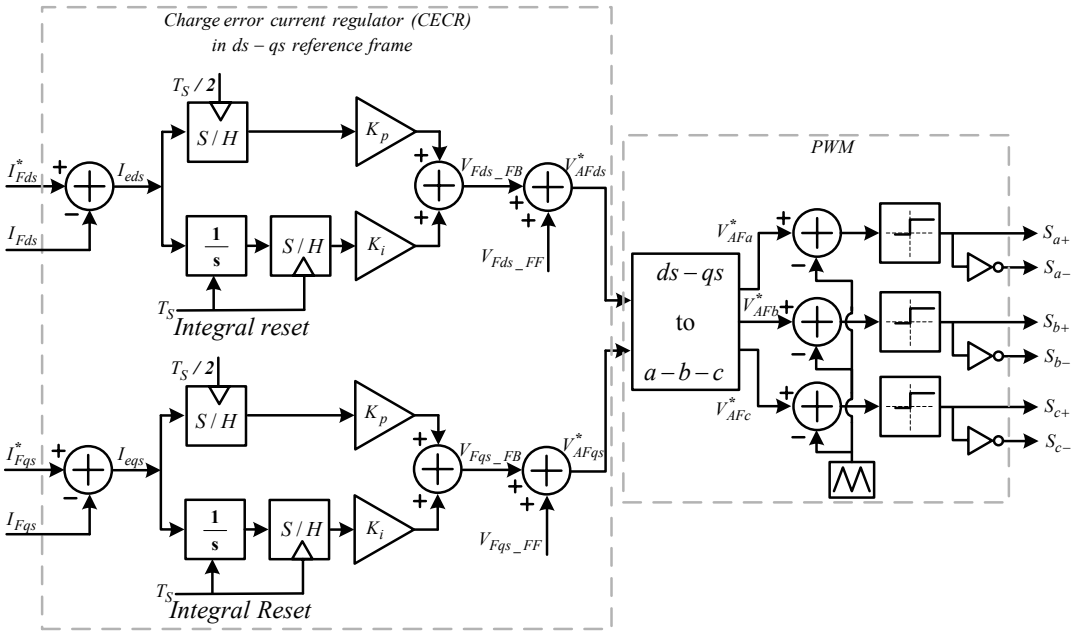

Figure 3.15 Block diagram of CECR in the 'ds-qs' reference frame.

Although specifications like double update of voltage reference in a modulation period and charge error part that minimize current errors of the CECR illustrate high performance current regulation, the practical realization of the CECR is hard due to the analog implementation of the charge error portion of the regulator for a satisfactory performance. Therefore, the analog implementation is a drawback of the CECR. Another drawback of the CECR is that the controller gains are dependent on filter inductance estimated value and switching frequency as in conventional predictive control [13], [23]. Therefore the controller performance depends on system parameter values. In this thesis, only simulation studies on the CECR are carried out to observe the claimed superior performance of the regulator and to compare it with other regulators.

3.3.3 The Resonant Filter Current Regulator

The current controllers discussed up to now utilize one set of gains for current regulation of the PAF system. This means that the controllers utilize the same gains for all frequencies within their bandwidth. However, the system parameters may change as the frequency changes. With one set of gains, the changes of system parameters are not compensated well in a current regulator. If the regulated current consists of multiple frequencies as in PAF case, this results in inadequate current regulation and inadequate harmonic mitigation in the PAF application.

Linear current regulators, for example, LPCR and CECR, have a bandwidth depending on switching frequency and controller gains. But it is a known fact that the controller gain response is not unity and phase response is not zero for different frequencies within its bandwidth. As the frequency increases, the controller gain decreases (it is 3 dB at its cut-off frequency) and the phase difference increases for a first order system as in the PAF case. The resonant filter current regulator (RFCR), which is proposed as a solution to this problem utilizes parallel controllers, each of which is tuned to provide unity gain and zero phase for a selected harmonic frequencies [31]. Since the reference current for the PAF is the harmonics of the load current and reactive power component of the load current at the fundamental

frequency and the active current component at the fundamental frequency for DC bus voltage regulation, their frequencies are well defined, the tuning of the controllers in the RFCR structure is performed based on these well defined frequencies. The RFCR consists of two parallel current controller structures such that one creates voltage reference for the compensation of the harmonic currents called the harmonic current controller and one is the conventional proportional gain controller as in LPCR and CECR.

3.3.3.1 The Harmonic Current Controller of The RFCR

The main task of a three-phase three-wire PAF is to compensate the harmonics of the current source type nonlinear load. In the case of 6-pulse rectifiers, the order of the nonlinear load harmonics, k, exists in the form as

$$k = 6n \pm 1 \tag{3.4}$$

where n is an integer (n=1,2,3,…). While the harmonics with the order of

$$k_{+} = 6n+1 \tag{3.5}$$

and with angular speed of '$k\omega_e$' rotating in the positive direction of the stationary reference frame are known as the positive sequence harmonics, the harmonics with the order of

$$k_{-} = 6n-1 \tag{3.6}$$

and with angular speed of '$k\omega_e$' rotating in the negative direction of the stationary reference frame are known as the negative sequence harmonics. For instance, while the 5^{th} harmonic current with n=1, k=5 is a negative sequence harmonic rotating with the angular speed of $-5\omega_e$, where the negative sign illustrates the direction of rotation, the 7^{th} harmonic current with n=1, k=7 is a positive sequence harmonic with the angular speed of $7\omega_e$. If the synchronous reference frame ('de-qe') transformation is carried out for the harmonic currents, the order of the positive sequence harmonics

with the order of (3.5) becomes as

$$k_{+} = 6n \tag{3.7}$$

and with the angular speed of $k\omega_e$ rotating in the positive direction of the 'de-qe' reference frame and the order of the negative sequence harmonics with the order of (3.6) becomes as

$$k_{-} = 6n \tag{3.8}$$

and with angular speed of '$k\omega_e$' rotating in the negative direction of the 'de-qe' reference frame since the 'de-qe' reference frame transformation provides a frequency shift of $-\omega_e$. For instance, while the 5^{th} harmonic current in the 'de-qe' reference frame is a negative sequence harmonic rotating with the angular speed of $-6\omega_e$, the 7^{th} harmonic current in the 'de-qe' reference frame is a positive sequence harmonic rotating with the angular speed of $6\omega_e$.

The structure of the harmonic current controller of the RFCR is as follows. A single controller in the 'de-qe' reference frame tuned for the each harmonic order of k=6n, which is designed for both sequences, can compensate the harmonic current pairs with the order of k=6n±1 in the stationary reference frame with unity gain and zero phase error. For example, the 5^{th} and 7^{th} load current harmonics can be eliminated with a single controller in the synchronous frame. The controller in this case must be a $6\omega_e$ resonant controller. By increasing the number of the controllers, the order of the compensated harmonic currents can be increased.

The harmonic current controller of the RFCR is designed in the harmonic reference frame so that each controller regulates DC quantities and then the designed controller is transformed to the 'de-qe' reference frame and implemented in the 'de-qe' reference frame. The model of the PAF system in a reference frame of the harmonic order k (reference frame rotating with an angular speed of $k\omega_e$, where ω_e is positive for positive sequence harmonics and negative for negative sequence harmonics) is given in vector notation by

$$\vec{V}_{Finv}^{k} - \vec{V}_F = R_F \vec{I}_F^{k} + L_F \frac{d\vec{I}_F^{k}}{dt} + jk\omega_e L_F \vec{I}_F^{k} \tag{3.9}$$

In (3.9), R_F and L_F are resistance and inductance of the filter inductor, $\vec{V}_F$ is the filter terminal voltage vector at PCC, $\vec{V}_{Finv}^{k}$ is the inverter output voltage vector, $\vec{I}_F^{k}$ is filter current vector, and superscript 'k' denotes the reference frame harmonic order. From the system model in (3.9), the system has a single complex pole defined as

$$p_k = \frac{-R_F}{L_F} + jk\omega_e \tag{3.10}$$

for the harmonic order 'k' where ω_e is positive for the positive sequence harmonics and negative for the negative sequence harmonics. In a three-phase system designing a complex frame regulator rather than scalar regulator, a cross-coupling decoupling controller is not required [39]. Therefore in this study the complex frame controller will be utilized. A complex frame PI current regulator for the harmonic order of $k\omega_e$, which results in zero steady-state error, has a complex-coefficient transfer function of $H_k(s)$ given as

$$H_k(s) = K_{pk} + \frac{\left(K_{ik} + jk\omega_e K_{pk}\right)}{s} \tag{3.11}$$

where K_{pk} and K_{ik} represent the proportional gain and integral gain of the controller. The closed current loop of the PAF modeled in (3.9) for the reference frame of harmonic order k with the harmonic current controller of (3.11) is illustrated in Figure 3.16 by assuming an ideal VSI.

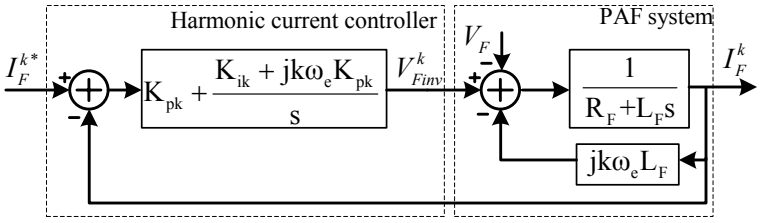

Figure 3.16 The closed current loop of the PAF system for the reference frame of the harmonic order k.

The transfer function of the harmonic current controller in (3.11) becomes as

$$H_{k+}(s) = K_{pk} + \frac{\left(K_{ik} + jk\omega_e K_{pk}\right)}{s} \tag{3.12}$$

for positive sequence harmonics and becomes as

$$H_{k-}(s) = K_{pk} + \frac{\left(K_{ik} - jk\omega_e K_{pk}\right)}{s} \tag{3.13}$$

for negative positive sequence harmonics. The above equations represent the PI vector controllers with cross-coupling decoupling. Since the controllers are implemented in the 'de-qe' reference frame, these transfer functions should be transferred to 'de-qe' reference frame by taking a frequency shift of $-k\omega_e$ for positive sequence harmonics, and $k\omega_e$ for negative sequence harmonics. Then the controller $H_{k+}(s)$ in (3.12) for the positive sequence components becomes as $H_{k+}(s\text{-}jk\omega_e)$ which is given by

$$H_{k+}(s - jk\omega_e) = K_{pk} + \frac{\left(K_{ik} + jk\omega_e K_{pk}\right)}{s - jk\omega_e} = \frac{\left(K_{pk}s + K_{ik}\right)}{s - jk\omega_e} \tag{3.14}$$

and the controller $H_{k-}(s)$ in (3.13) for the negative sequence components becomes as $H_{k-}(s+jk\omega_e)$ which is given by

$$H_{k-}(s + jk\omega_e) = K_{pk} + \frac{\left(K_{ik} - jk\omega_e K_{pk}\right)}{s + jk\omega_e} = \frac{\left(K_{pk}s + K_{ik}\right)}{s + jk\omega_e} \tag{3.15}$$

The transfer function, $H_{kh}(s)$, required to control the harmonic order 'k' for the both sequences in 'de-qe' reference frame is the superposition of $H_{k+}(s\text{-}jk\omega_e)$ in (3.14) and $H_{k-}(s+jk\omega_e)$ in (3.15) given by

$$H_{kh}(s) = H_{k+}(s - jk\omega_e) + H_{k-}(s + jk\omega_e) = \frac{2K_{pk}s^2 + 2K_{ik}s}{s^2 + \left(k\omega_e\right)^2} \tag{3.16}$$

Equation (3.16) represents a transfer function of a resonant filter controller with real coefficients, which theoretically gives infinite gain and zero phase value at the resonant frequency of $k\omega_e$ and approximately zero gain for all other frequencies. Since the controller manipulates two harmonic frequency components with one complex controller (one scalar 'de' axis and one scalar 'qe' axis controller), its implementation is advantageous. Because of this characteristic, in the implementation the cancelled harmonics will be termed as harmonic pairs, such as the $6\omega_e$ pair which involves the 5^{th} and 7^{th} harmonics.

The transfer function of the harmonic current controller loop can be obtained by assuming an ideal inverter and taking the model of the PAF in stationary frame for one harmonic pair as

$$\frac{\vec{I}_F^{k*}}{\vec{I}_F^{k}} = \frac{2\left(K_{pk}s^2 + K_{ik}s\right)}{L_F s^3 + \left(2K_{pk} + R_F\right)s^2 + \left(2K_{ik} + L_F\left(k\omega_e\right)^2\right)s + R_F\left(k\omega_e\right)^2} \tag{3.17}$$

The frequency response of the harmonic controller current loop in (3.17) can be obtained for one harmonic pair with the order of k for PAF system parameters of L_F and R_F. If the K_{pk} and K_{ik} values of the controller are selected as

$$\frac{K_{pk}}{K_{ik}} = \frac{L_F}{R_F} \tag{3.18}$$

in order to realize a pole-zero cancellation, the transfer function in (3.17) becomes as

$$\frac{\vec{I}_F^{k*}}{\vec{I}_F^{k}} = \frac{\frac{2K_{pk}}{L_F}s}{s^2 + \frac{2K_{pk}}{L_F}s + \left(k\omega_e\right)^2} \tag{3.19}$$

Equation (3.19) represents a second order band-pass filter with a resonant frequency of $k\omega_e$. The frequency response of the harmonic controller current loop in (3.19) is obtained for one harmonic pair with the order of k=6 for two K_{pk} values of 0.1 and 0.5, L_F = 2 mH, R_F = 0.25 Ω, and ω_e=50 Hz and illustrated in Figure 3.17. Figure

3.17 illustrates that the designed controller for k=6 has a gain of unity and zero phase shift for the resonant frequency of $k\omega_e$ (300 Hz in this case for f_e=50 Hz) and zero gain for dc signals. The unity gain and zero phase shift at the resonant frequency imply that the compensation of the respective harmonic current is superior compared to other current regulators. The frequency response for the negative frequencies is not shown in Figure 3.17, but it is symmetrical with respect to the 'y' axis and the same frequency response for the negative sequences components are obtained with the designed controller as mentioned earlier. The value of K_{pk} determines the selectivity of the filter. While lower values of K_{pk} increase the sharpness of the band-pass filter and make the filter more selective, but decrease the transient response time, higher values of K_{pk} decrease the selectivity but increase the transient response time.

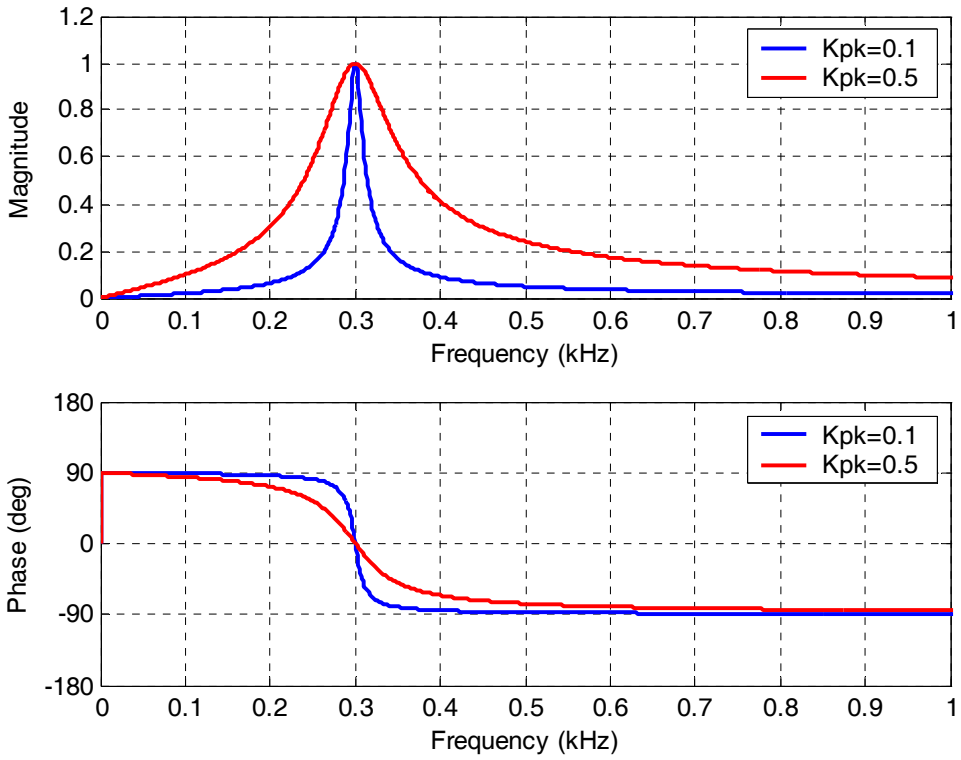

Figure 3.17 The closed current loop transfer function frequency response of the resonant filter controller tuned for k=6, $\omega_e=2\pi 50$ rad/s, K_{pk}=0.1 and K_{pk}=0.5.

The resonant filter controller in (3.16) compensates one harmonic pair with the harmonic order of k=6n±1 at the stationary frame. If the harmonic current pairs that will be compensated are increased, different resonant filter controllers for each

harmonic pair should be implemented as parallel structures. The transfer function of the resonant filter controllers for the harmonic current compensation is the sum of the individual resonant filter controllers with different harmonic orders of k and given as

$$H_h(s) = \sum_{k=6}^{6n} \frac{2K_{pk}s^2 + K_{ik}s}{s^2 + (k\omega_e)^2},\ n = 1,2,3... \tag{3.20}$$

The block diagram of the paralleled resonant filter controllers is illustrated in Figure 3.18 for the 'de' axis of the 'de-qe' reference frame. The same structure is repeated for the 'qe' axis controller. As the figure illustrates, while the resonant filter controller with the harmonic order of k=6 and the resonant frequency of $6\omega_e$ in 'de-qe' reference frame compensates the 5th and 7th harmonic currents in stationary reference frame, the resonant filter controller with the harmonic order of k=12 and the resonant frequency of $12\omega_e$ in 'de-qe' reference frame compensates the 11th and 13th harmonic currents in stationary reference frame. If the harmonic current pairs that will be compensated are increased, additional resonant filters become necessary. The frequency response of the harmonic controller current loop is obtained for four harmonic pairs with the order of k={6, 12, 18, 24}, $\omega_e=2\pi50$ rad/s and K_{pk} values of 0.1 and 0.5 and shown in Figure 3.19. The figure illustrates that the harmonic current controller utilizing paralleled resonant filter controllers has unity gain and zero phase shift at the tuned frequencies of 300 Hz, 600 Hz, 900 Hz and 1200 Hz for this case.

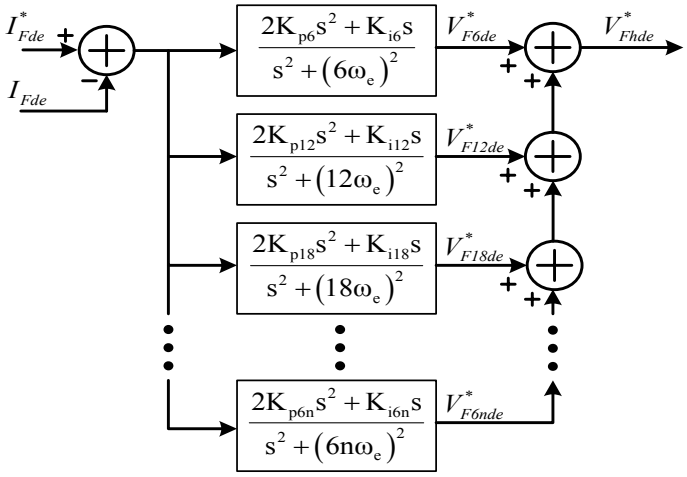

Figure 3.18 The block diagram of the harmonic current controller with the paralleled resonant filter controllers for the 'de' axis in the 'de-qe' reference frame.

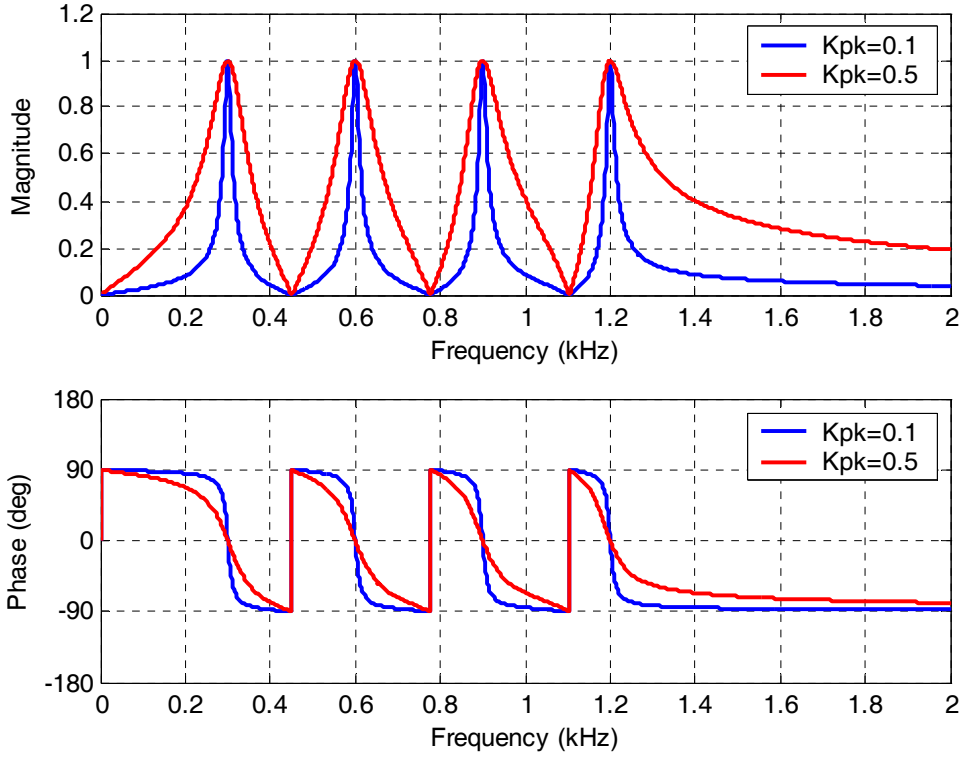

Figure 3.19 The closed current loop transfer function frequency response of the resonant filter controller for k= {6, 12, 18, 24}, ω_e=2π50 rad/s, K_{pk}=0.1 and K_{pk}=0.5.

In the above discussion, the analysis of the resonant filter controller is carried out by assuming an ideal PAF system excluding the system delays. The effect of the total system delay (τ_T) can be observed by utilizing the system model derived in the section of the LPCR and illustrated in Figure 3.13. By utilizing this model with the transfer function of resonant filter controller in (3.16) for harmonic pair with the order of k, the closed current loop transfer function of the system including the system delay of τ_T is given as

$$\frac{\vec{I}_F^{k*}}{\vec{I}_F^{k}} = \frac{2K_{pk}s}{L_F\tau_T s^3 + L_F s^2 + \left(2K_{pk} + L_F\left(k\omega_e\right)^2\tau_T\right)s + L_F\left(k\omega_e\right)^2 s} \tag{3.21}$$

if the controller gains in (3.16) is chosen to achieve a pole-zero cancellation as in (3.18). Figure 3.20 compares the frequency response of (3.21) including the system

delay τ_T to the frequency response of (3.17) excluding the system delay τ_T for k=6, $\omega_e=2\pi50$ rad/s, $K_{pk}=0.5$, $L_F=2$ mH, and $R_F=0.25$ Ω. Figure 3.21 is the detailed illustration of Figure 3.20 around the resonant frequency of $k\omega_e$. The peak point of the magnitude response shifts slightly to the right in the case of τ_T, however the magnitude of the response is unity at the resonant frequency of 300 Hz for this case. Moreover, the phase response around 300 Hz is zero as in case of the ideal system. Figure 3.22 compares the frequency response of the closed loop transfer function including the system delay τ_T to the frequency response of the closed loop transfer function excluding and including the system delay τ_T for k={6, 12, 18, 24}, $\omega_e=2\pi50$ rad/s, $K_{pk}=0.5$, $L_F=2$ mH, and $R_F=0.25$ Ω. Figure 3.23 is the detailed illustration of Figure 3.22 around the designed resonant frequencies. The peak points of the magnitude response of the resonant controller shift slightly to the right and the magnitude of the peak points increases in the case of the τ_T as the frequency increases, however the magnitude of the response is unity at the considered resonant frequencies of 300 Hz, 600 Hz, 900 Hz, 1200 Hz. Moreover, the phase response around the considered resonant frequencies is zero as in case of the ideal system. Therefore, the total system delay does not affect the magnitude and phase of the designed resonant controllers at the considered resonant frequencies.

Each resonant filter controller compensates the harmonic pairs of the well defined harmonic frequencies in the ‘de-qe’ reference frame. However, the PAF does not only compensate the harmonic currents but also the reactive power current component and the negative sequence current component of the nonlinear load. Meanwhile it regulates its DC bus voltage by regulating a current reference at the fundamental frequency. For this purpose, additionally, a controller other than the harmonic current controller should be designed.

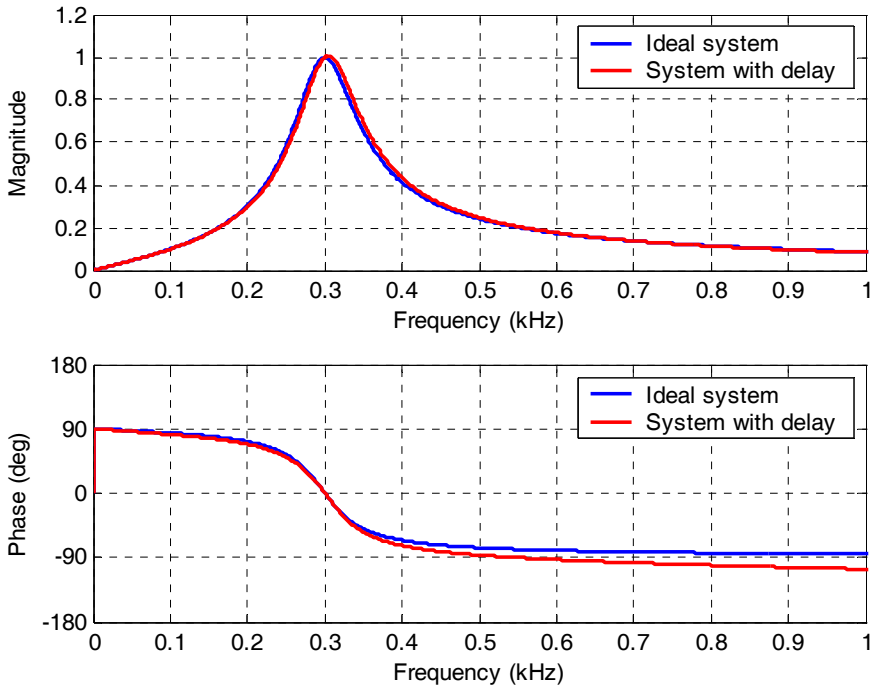

Figure 3.20 The closed current loop transfer function frequency response of the resonant filter controller with k=6, $\omega_e=2\pi 50$ rad/s, $K_{pk}=0.5$ for the ideal system and the system with the delay of $1.2T_S=60\mu s$

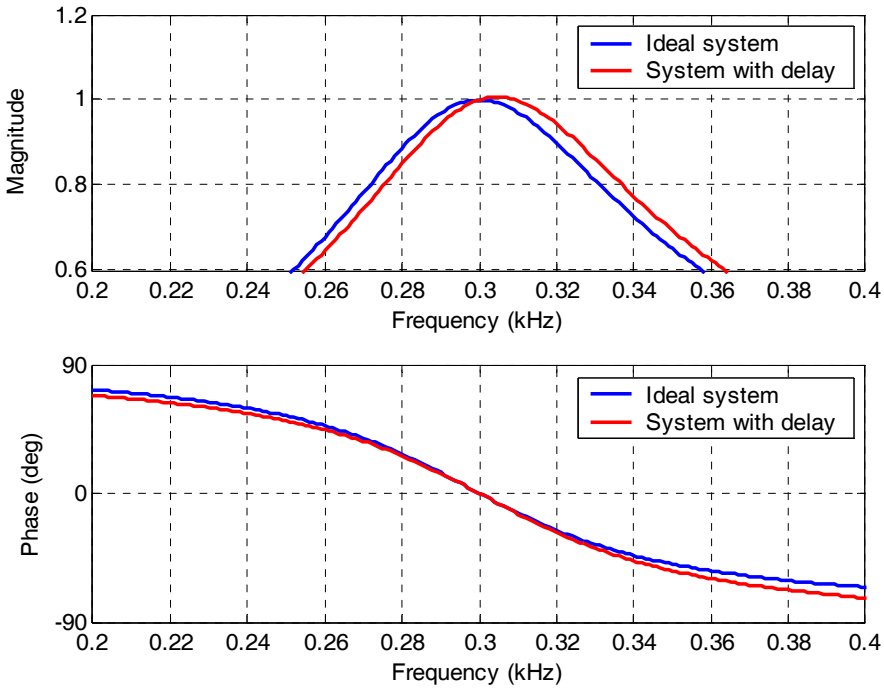

Figure 3.21 The detailed illustration of Figure 3.20.

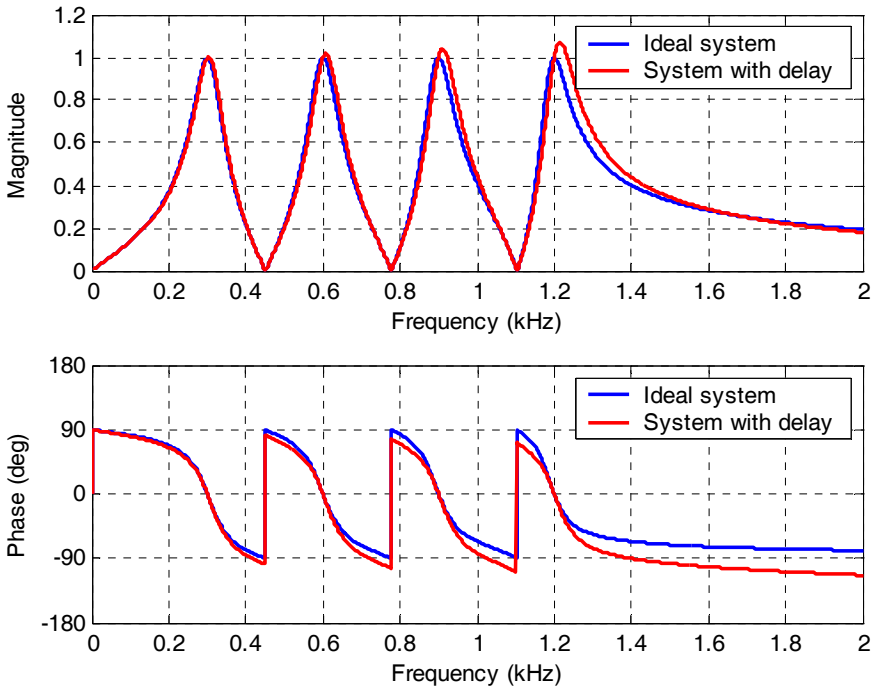

Figure 3.22 The closed current loop transfer function frequency response the resonant filter controller with k= {6, 12, 18, 24}, $\omega_e=2\pi 50$ rad/s, $K_{pk}=0.5$ for the ideal system and the system with the delay of $1.2T_S=60\mu s$.

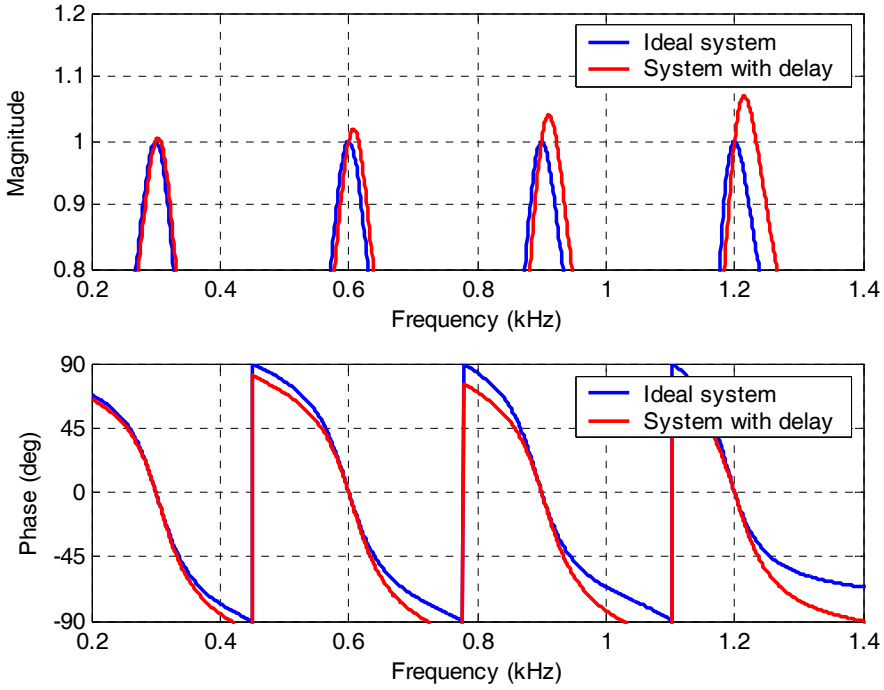

Figure 3.23 The detailed illustration of Figure 3.22.

3.3.3.2 The Proportional Gain Controller of The RFCR

For the compensation of the current components other than the harmonic pairs manipulated by the above discussed resonant frame controller, a proportional gain current controller can be utilized as in the case of LPCR. The proportional gain current controller with line voltage feed-forward compensation is paralleled to the resonant frame harmonic current controller for the compensation of the reactive power current component and the negative sequence current component of the nonlinear load. Since the PAF regulates its DC bus voltage at fundamental frequency, this proportional gain current controller will also create a voltage reference for the regulation of the PAF DC bus voltage. Moreover, the proportional gain current controller should compensate the higher order harmonics if the resonant current controllers are designed for the most dominant harmonic pairs of the nonlinear load current like 5^{th}, 7^{th}, 11^{th} and 13^{th}. The block diagram of the RFCR with the harmonic current controller and the proportional gain current controller is illustrated in Figure 3.24. Note that the reference for the harmonic current controller implemented in 'de-qe' reference frame is not only harmonic current reference of the PAF, but the total current reference of PAF which also includes fundamental reference current components. However, the output of the resonant frame harmonic controller does not include any fundamental frequency reference voltage component since its gain is zero for DC signals in the 'de-qe' reference frame which represents the fundamental frequency components in the stationary reference frame. The proportional gain current controller avoids the cross coupling between the phase currents since it is implemented in 'ds-qs' reference frame. At the output of the controller, the reference voltages from the proportional gain current controller, V^*_{F1ds} & V^*_{F1qs}, and from harmonic components, V^*_{Fhds} & V^*_{Fhqs}, are added to create the PAF voltage references, V^*_{Fds} & V^*_{Fqs}. The generated inverter voltage references in the 'ds-qs' reference frame are synthesized by PWM, which is not illustrated in Figure 3.24, as in the LPCR and the CECR to generate on-off switch signals for VSI. Note that the harmonic current controller consisting of resonant filter controllers is implemented in the 'de-qe' reference frame, while the proportional gain current controller is implemented the 'ds-qs' reference frame.

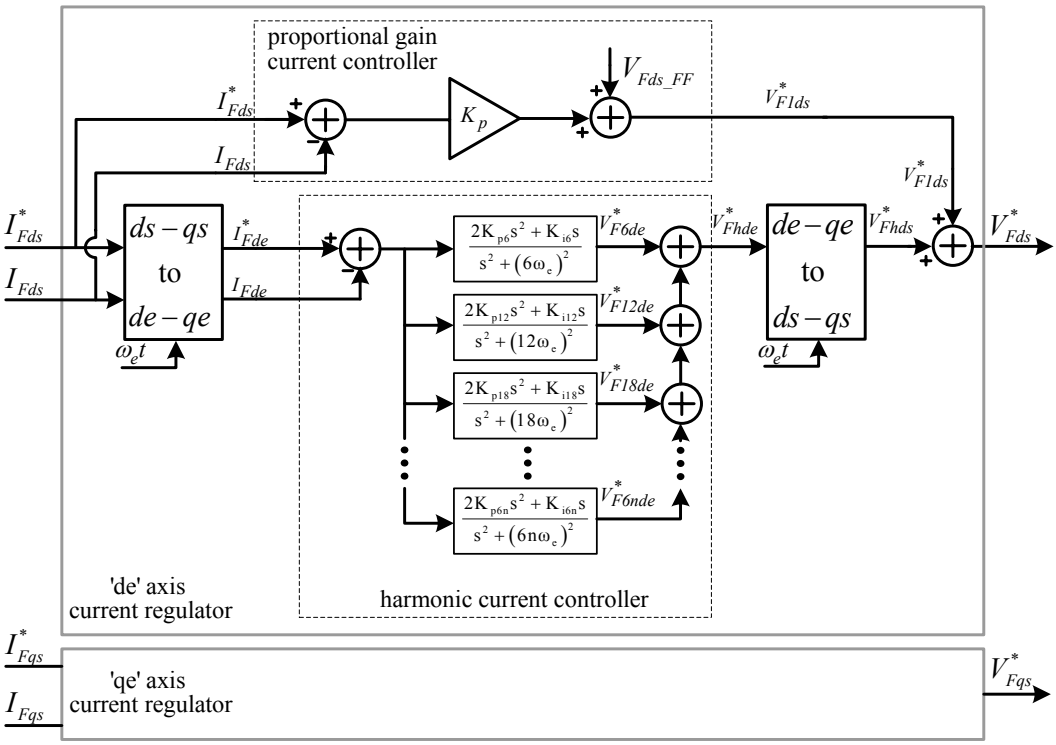

Figure 3.24 The block diagram of the resonant filter current regulator (RFCR).

The proportional gain (K_P) of the RFCR can be selected based on the desired phase margin of the open loop transfer function of the overall system as in the case of LPCR. Figure 3.25 illustrates the simplified block diagram of the RFCR including the total system delay block and PAF system. In the figure, K(s) represents the transfer function of the proportional gain current controller while H(s) represents the transfer function of the harmonic current controller which consists of the paralleled resonant filter controllers. The open loop transfer function of the system is defined as in (3.22) and the frequency response of (3.22) is illustrated in Figure 3.26 for various K_P values, three harmonic pair controllers with the order of k={6, 12, 18}, $\omega_e=2\pi 50$ rad/s, $K_{pk}=0.5$, $L_F=2$ mH, and $R_F=0.25$ Ω. Further, the figure illustrates the phase margins for various K_P values. Based on the frequency response of the open loop transfer function, the K_P value of 40 gives the phase margin value of 45°, which is considered as the design value as in the case of the LPCR. Since the designed resonant filter controllers respond only to the tuned frequencies, the obtained K_P value is equal to the value of K_P for the LPCR.

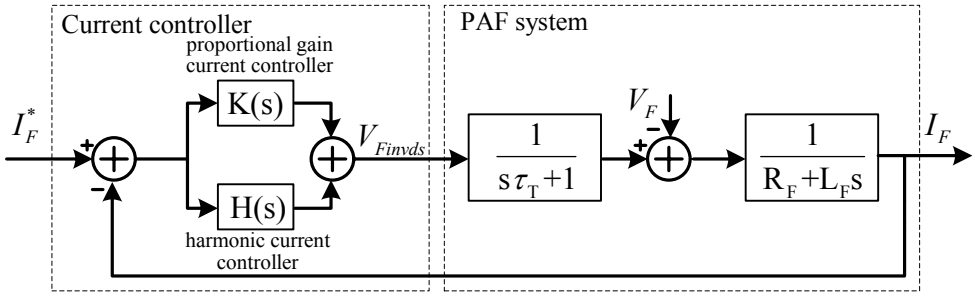

Figure 3.25 The simplified block diagram of the RFCR current control loop.

$$T_{OL}(s) = \big(K(s) + H(s)\big)\left(\frac{1}{\tau_T s + 1}\right)\left(\frac{1}{L_F s + R_F}\right) \tag{3.22}$$

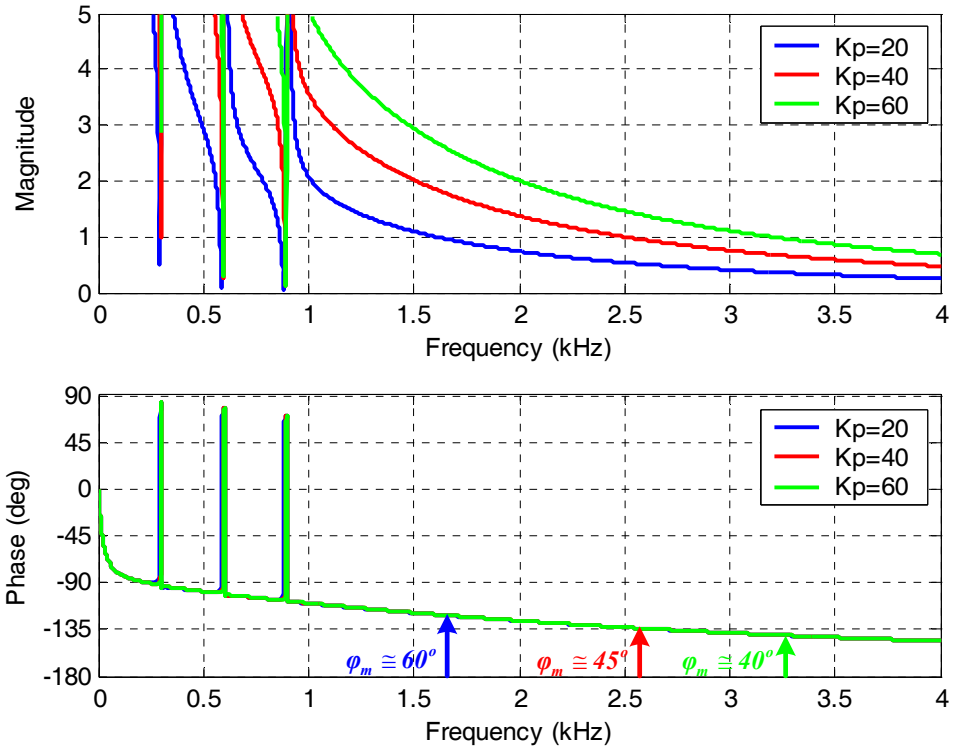

Figure 3.26 The open loop transfer function frequency response the RFCR for various K_P values, three harmonic pairs with the order of k={6, 12, 18}, ω_e=2π50 rad/s, K_{pk}=0.5, L_F=2 mH, and R_F=0.25 Ω.

Since the K_P value is determined based on the phase margin value of 45°, the closed current loop frequency response can be investigated for the RFCR including the K_P value of 40. Figure 3.27 illustrates the closed current loop frequency response of the RFCR for K_P=40, three harmonic pairs with the order of k={6, 12, 18} and K_{pk}={0.1, 0.5}, ω_e=2π50 rad/s, L_F=2 mH and R_F=0.25 Ω. Figure 3.28 is the detailed illustration of Figure 3.27. Based on the figures, the gain and phase response of the controller is unity and zero respectively for the fundamental frequency of 50 Hz and the resonant frequencies of 300 Hz, 600 Hz, and 900 Hz. This illustrates the superior compensation characteristics of the RFCR for the defined resonant frequencies. Other observation with the closed current loop transfer frequency response in Figure 3.27 and Figure 3.28 is that the closed current loop gain for the frequencies just below the resonant filters tuned frequencies is approximately zero. With the addition of the proportional gain (K_P) controller parallel to the harmonic current controllers, zeros are created in the open loop transfer function in (3.22). These zeros make the open loop transfer function value zero for frequencies just below the resonant filters tuned frequencies. For instance, for k={6, 12, 18}, K_{pk}=0.5, K_P=40 ω_e=2π50 rad/s, L_F=2 mH and R_F=0.25 Ω, the system has zero open loop gain at the frequencies of 298 Hz , 596 Hz, 895 Hz approximately. This can also be observed in Figure 3.26 such that open loop transfer function gain drops considerably and approach zero value at these frequencies. As a result, the closed loop transfer function gain at these frequencies degrades as Figure 3.27 and Figure 3.28 illustrate.

The closed current loop frequency response of the RFCR with k={6, 12, 18}, K_{pk}=0.5, ω_e=2π50 rad/s is compared to that of LPCR which utilizes same K_P value of 40, L_F=2 mH and R_F=0.25 Ω in Figure 3.29 and Figure 3.30. The frequency response of the two current controllers is nearly same for higher frequencies. However, the frequency response of the RFCR is superior to that of the LPCR for resonant frequencies of 300 Hz, 600 Hz, and 900 Hz since the RFCR provides unity gain and zero phase shift for these frequencies. The discussion above illustrates that each resonant filter controller tuned to the well defined frequency represents zero steady-state error for the harmonic current compensation.

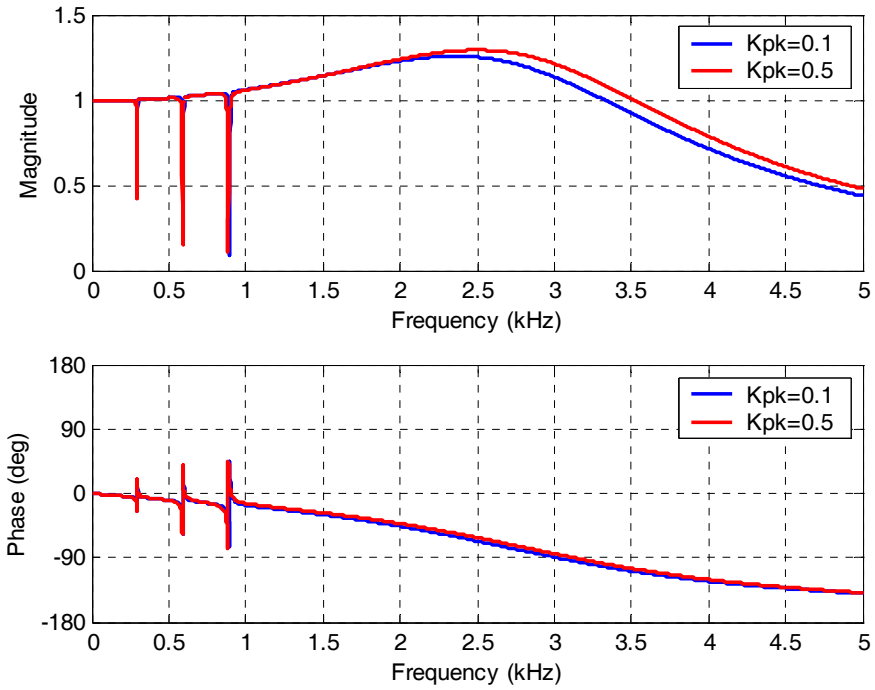

Figure 3.27 The closed loop transfer function frequency response of the RFCR for K_P=40, three harmonic pairs with the order of k={6, 12, 18} and K_{pk}={0.1, 0.5}, ω_e=2π50 rad/s, L_F=2 mH and R_F=0.25 Ω.

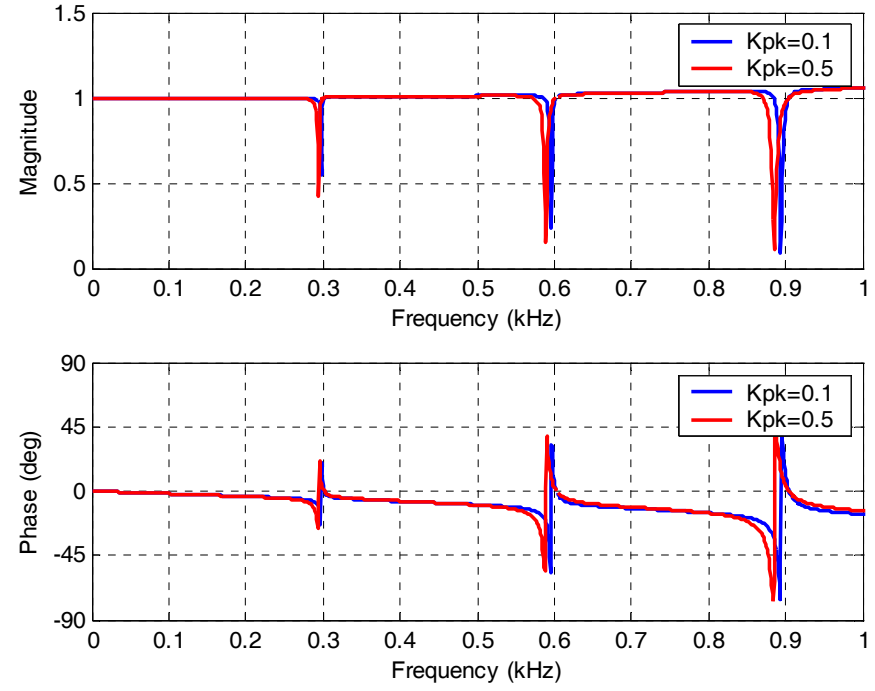

Figure 3.28 The detailed illustration of Figure 3.27 for lower frequencies.

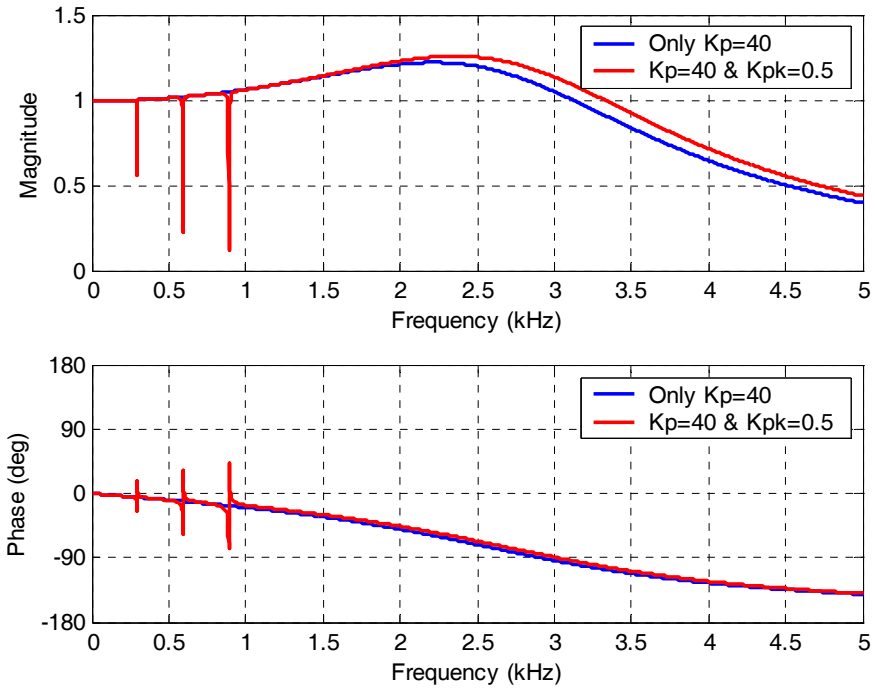

Figure 3.29 The closed loop transfer function frequency response of the RFCR with k={6, 12, 18}, K_{pk}=0.5, ω_e=2π50 rad/s and the LPCR with same K_P=40, L_F=2 mH, and R_F=0.25 Ω.

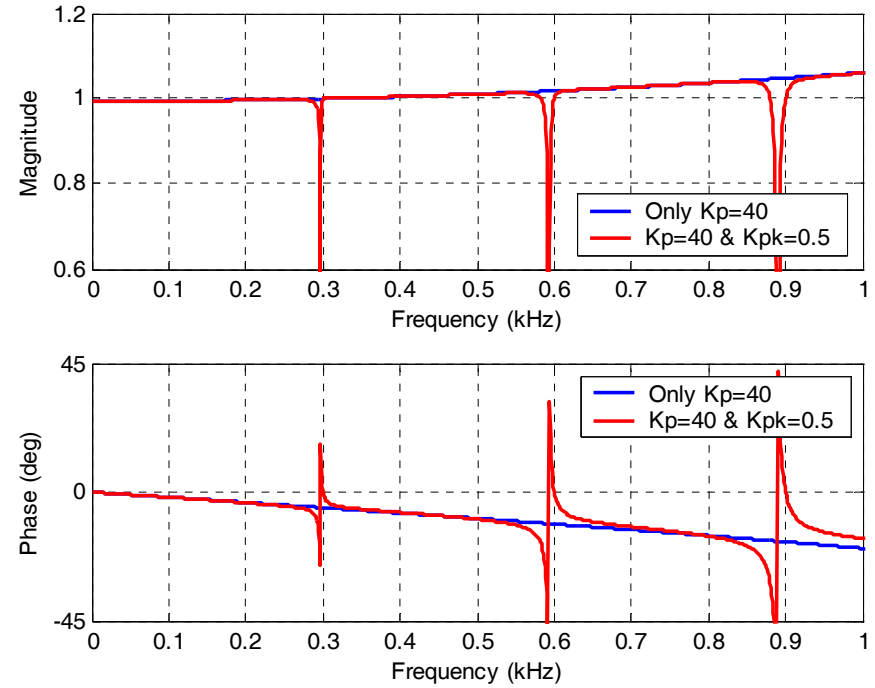

Figure 3.30 The detailed illustration of Figure 3.29 for lower frequencies.

The analysis of the RFCR is carried out in s-domain due to its analysis simplicity, which does not mean that implementation of the resonant filter controller is an analog one. The designed resonant filter controller in s-domain can be transformed to the 'z' domain, which allows the discrete time implementation of the designed resonant filter. The next section discusses the discrete time implementation of the resonant filter controller.

3.3.3.3 Discrete Time Implementation of the RFCR

The PAFs applications commonly utilize digital controllers in real time implementations. Therefore, the derived transfer functions for the resonant filter controllers should be transformed into z-domain for the discrete time implementation. There exist various transformation techniques for the s-domain to the z-domain transformation. However, Tustin transformation in (3.23) is generally preferred in order to include angular frequency ω_e in transformation. The coefficient A defined in (3.24) includes the angular frequency ω_e and the sampling time T_S.

$$s = \frac{z-1}{z+1} A \tag{3.23}$$

$$A = \frac{k\omega_e}{\tan\left(k\omega_e \frac{T_S}{2}\right)} \tag{3.24}$$

When the Tustin transformation is utilized, the resonant filter controller transfer function in (3.16) is transformed to the z-domain in the form of

$$H_{kh}(z) = \frac{\beta_0 + \beta_1 z^{-1} + \beta_2 z^{-2}}{1 + \alpha_1 z^{-1} + \alpha_2 z^{-2}} \tag{3.25}$$

The coefficients in (3.25) are given in terms of K_{pk}, $K_{ik,}$ ω_e and k by the Equations (3.26) through (3.31).

$$\beta_0 = \frac{2K_{pk}A^2 + 2K_{ik}A}{A^2 + \left(k\omega_e\right)^2} \tag{3.26}$$

$$\beta_1 = \frac{-4K_{pk}A^2}{A^2 + \left(k\omega_e\right)^2} \tag{3.27}$$

$$\beta_2 = \frac{2K_{pk}A^2 - 2K_{ik}A}{A^2 + \left(k\omega_e\right)^2} \tag{3.28}$$

$$\alpha_1 = \frac{2\left(k\omega_e\right)^2 - 2A^2}{A^2 + \left(k\omega_e\right)^2} \tag{3.29}$$

$$\alpha_2 = \frac{A^2 + \left(k\omega_e\right)^2}{A^2 + \left(k\omega_e\right)^2} \tag{3.30}$$

$$A = \frac{k\omega_e}{\tan\left(k\omega_e \frac{T_S}{2}\right)} \tag{3.31}$$

In a discrete time implementation, $H_{kh}(z)$ in (3.25) is implemented as

$$y[k] = \beta_0 x[k] + \beta_1 x[k\text{-}1] + \beta_2 x[k\text{-}2] - \alpha_1 y[k\text{-}1] - \alpha_2 y[k\text{-}2] \tag{3.32}$$

where x[k] is the input signal value, x[k-1] is the previous input signal value, x[k-2] is the second previous input signal value, y[k] is the output signal value, y[k-1] is the previous output signal value, and y[k-2] is the second previous output signal value. The discrete time control block diagram of the resonant filter defined in (3.32) is shown in Figure 3.31. For the selected gains, K_{pk} and K_{ik}, the selected harmonic order of k with the fundamental frequency of ω_e, the coefficients are calculated and given as the constants for the discrete implementation for each resonant filter controller. Therefore, no computational time is consumed for the coefficients determination. The proportional gain current controller implementation is simple task since it only includes a multiplication of the sampled input signal with the K_P gain.

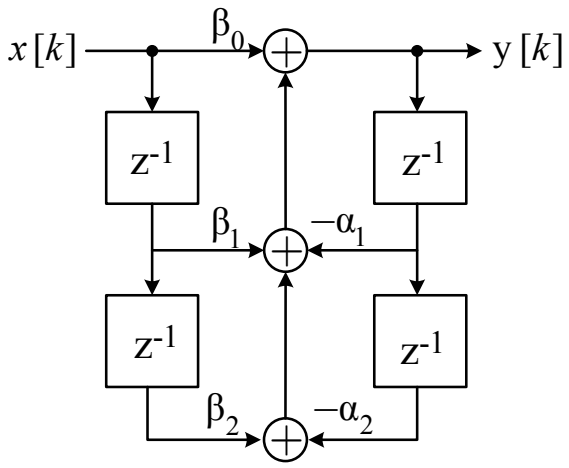

Figure 3.31 The z-domain signal flow chart of the resonant filter controller.

The theoretical analysis of RFCR is showed that the resonant filter controller has unity gain and zero phase shift for the selected frequency. Moreover, the regulation of the harmonics pairs can be increased by paralleling the resonant filter controllers. The main drawback of the RFCR is the increased number of controllers since the RFCR necessitates an additional controller for each harmonic pair to be compensated, which results in computational burden for the digital controller. Moreover, although the number of the parallel resonant controller can be increased theoretically, it is restricted in the discrete time implementation with fixed sampling frequency due to the insufficient samples for higher frequencies. This results in a limited bandwidth for the higher order harmonics. In practice, the resonant filter controllers are designed for the most dominant harmonic currents like 5^{th}, 7^{th}, 11^{th}, and 13^{th} which appear at low frequencies. Therefore, the computational burden of the digital controller is eliminated with this approach.

A second drawback of the RFCR involves the line frequency. Since the line frequency is not fixed but varies in a range, the resonant filter harmonic current controllers which are tuned for specific frequencies may exhibit poor gain for the varying line frequency conditions. Typically the line frequency varies less than 0.5% in high quality electric utilities (for example, in Japan) and in Turkey the typical maximum variation involves 1% which corresponds to 0.5 Hz for the 50 Hz line. As a result the line frequency may vary between 49.5 Hz and 50.5 Hz. Since the

resonant filter harmonic current controllers are tuned for the 50 Hz line operating point, deviation from this value results in controller gain reduction. In the RFCR proposed in [31], large number of harmonic pair controllers is utilized (k={6, 12, 18, 24, 30, 36}). With this wide range of compensation there is no need for an additional proportional controller with large gain. When the line frequency varies, the gains drop drastically implying poor compensation of the harmonics. In addition to the heavy computational burden, the method does not yield efficient suppression of higher frequency harmonics (specifically for k={30,36}). In the RFCR utilized in this work, a small number of RFCRs is utilized (k={6, 12, 18}) and the computation requirement is not heavy. To suppress the higher frequency harmonics, a large gain proportional controller is added. This controller however may have a counter effect on the regulator overall performance under the condition of operating at a frequency below the rated frequency. This is because as the line frequency decreases the zero gain frequencies of the controller coincide with the harmonic frequencies. This issue must be taken into consideration during the design procedure.

With the discussion of the resonant filter current regulator in PAF application, the analysis of the practically utilized and reported linear current regulators, LPCR, CECR and RFCR is completed. The next section investigates the on-off current regulators in the PAF application.

3.4 On-Off Current Regulators

On-off current regulators are proven to be most suitable solution for all applications of the current regulated VSI where high performance is required like in the PAF case. The on-off current regulators are characterized by their unconditioned stability, high response speed and good accuracy. The reason for that is the direct evaluation of current error and the generation of switch on-off signals without PMW modulator delay unlike the linear current regulators as illustrated in Figure 3.32. The variable switching frequency, the limit cycle and the interaction among the phases, which results in low frequency current error, in the case of a three phase system with insulated neutral are the drawbacks of the on-off current regulators. Despite the

drawbacks of the on-off current regulators, their superior current tracking performance makes them a viable solution for the multiple frequencies, high di/dt current tracking applications as in the PAF [13], [30], [32], [33].

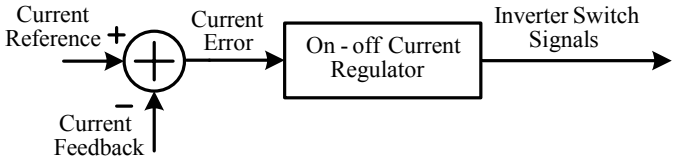

Figure 3.32 The basic principle of the on-off current regulators.

A well known, generally preferred on-off current regulator due to its simple structure and high bandwidth in the PAF application is the hysteresis current regulator. Lower limit ($-\Delta I$) and upper limit (ΔI) of the current error (I_e) are defined in a hysteresis current regulator. If the current error is between the limits, the position of the switch is preserved. However, if the current error exceeds one of the limits, 'on' or 'off' command based on the current error direction is sent to the switch. The hysteresis current regulators implemented in scalar form for three phase systems evaluate each phase current error independent from the others and are simple to implement. The block diagram of the basic three phase hysteresis current regulator is illustrated in Figure 3.33. Also, the hysteresis current regulator can be implemented in vector form in space vector coordinates [40]. However, it is not preferred due to its implementation difficulty. If the analog implementation is performed for the hysteresis current regulators, the current tracking performance is superior for the multiple frequencies, nonsinusoidal, and high di/dt current references. However, the change of the switching frequency is a drawback of the hysteresis current regulator. Moreover, the excessive increase of the switching frequency based on the operating conditions, the position of the line voltage in space in AC utility grid connected applications, or the phase interaction among the phase may result in thermal runaway of the semiconductors utilized for the VSI. Figure 3.34 illustrates the typical tracking performance of the analog hysteresis current regulator in PAF application and its switching signals for one phase over a fundamental cycle. The line voltage is also illustrated as a reference point. While the regulator tracks its reference properly, the

switching frequency changes over a fundamental cycle. However, the switching frequency reaches up to an excessive value of 40 kHz, which can be calculated by counting the switching signals over a defined time period as illustrated in Figure 3.34. This may result in excessive heat generation due to over-switching, and hence thermal instability of the system. Moreover, the variable switching frequency results in a wide band switching ripple currents. Since the switching ripple currents spread over a wide frequency band, it is difficult to design of a passive filter at the output terminals of the PAF to eliminate these ripple currents resulting in high frequency voltage distortions at PCC.

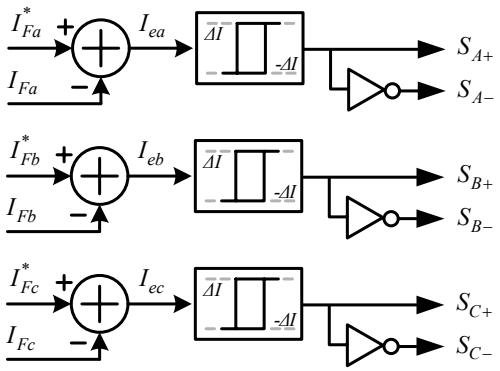

Figure 3.33 The block diagram of an analog hysteresis current regulator.

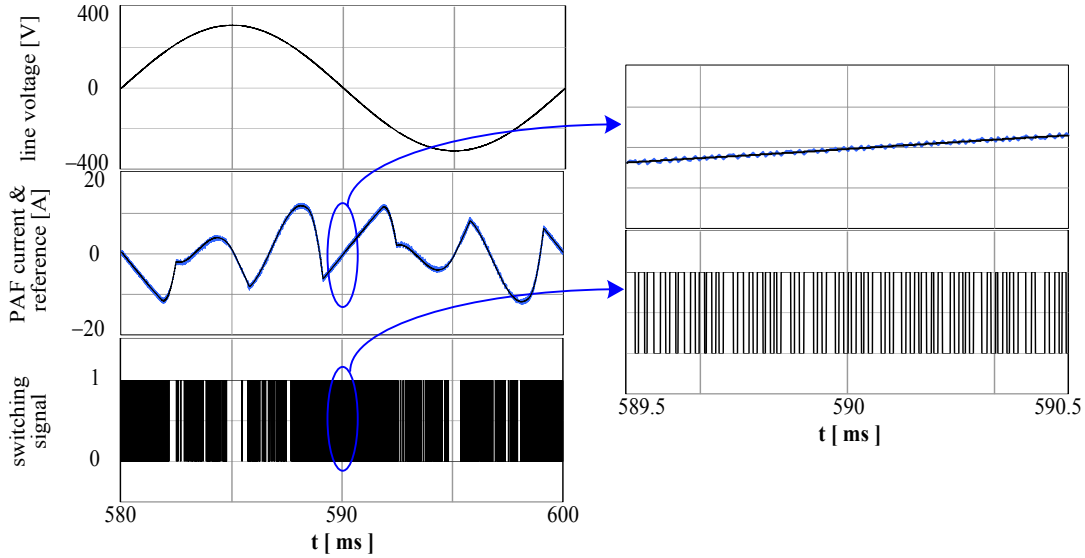

Figure 3.34 The tracking and switching performance of the analog hysteresis current regulator in the PAF application.

In the literature, the effective methods to eliminate inconveniences of hysteresis current regulators have been introduced and demonstrated to be a viable solution to achieve high performance control [32], [33]. But, the practical implementation of these methods, which usually necessitates complex analog circuitry, has been under discussion and has not been reported in today's industrial applications preferring discrete time solutions due to its advantages yet.

Fully discrete time implementation of the hysteresis current regulator is simple since it includes only utilization of the sampled current error to determine switch positions. Moreover, the sampling is done in a determined switching period (T_S). Therefore it is possible to limit the maximum switching frequency contrary to the analog implementation. However, in this case, the ripple on the current waveform is unpredictable and large in magnitude and the average switching frequency is very low. This results in a low current regulator bandwidth. Moreover, this approach limits the dynamic response of the hysteresis current regulator. Sampling is increased to achieve a high bandwidth value and a satisfactory dynamic response at the expense of over-switching resulting in thermal instability. The above requirements conflict with each other in a discrete time application. Fully discrete time hysteresis implementation is proposed in [33]. However, this method includes switching time prediction including system parameter knowledge and does not hold hysteresis current regulator in its basic form.

In this thesis, the discrete time implementation of the hysteresis current regulator is improved to achieve a high bandwidth and a high dynamic response for better current tracking capability while limiting the maximum switching frequency for thermal stability and keeping the current regulator in its basic form for implementation simplicity. For this purpose, the multi-rate current sampling and flexible PWM output programming is proposed. The block diagram of the proposed discrete time hysteresis current regulator (DHCR) for one phase is given in Figure 3.35. The figure includes two extra blocks compared to the analog hysteresis current regulator in Figure 3.33: a sample/hold (S/H) block representing multi-rate feedback current sampling with a sampling coefficient, K, and a switching decision block representing

an appropriate switch release mechanism. The bandwidth of the DHCR can be increased with high K and with flexible switch release mechanism allowing at most two switchings per cycle (T_S) but providing degree of freedom in the switching location within the cycle. Thus, the sampling delay and PWM output signal delay disadvantages are overcome in the discrete time implementation. The proposed DHCRs and the improvements with them will be shown in three increments and thus three current regulators, named DHCR1, DHCR2, and DHCR3.

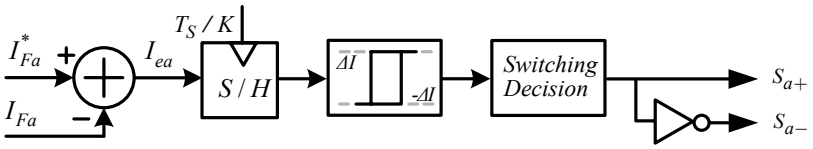

Figure 3.35 Block diagram of proposed discrete time hysteresis current regulator.

3.4.1 DHCR1

DHCR1 is known as the conventional discrete time hysteresis regulator (delta regulator). The method is illustrated in Figure 3.36. In the figure, T_S is defined as the switching period and determined by the maximum switching frequency f_{max}. The sampling coefficient K is 2. The current error is obtained by the current values ($\hat{i}(k)$ & $\hat{i}(k+1)$) sampled at the beginning and at the middle of T_S respectively. The 'on' or 'off' signals for the inverter switches are obtained based on the current error direction. A possible switch signal (S_{a+}, logical 1 or 0) is illustrated in Figure 3.36. The switch can change position only twice in a switching period since the sampling coefficient is 2. Therefore the f_{max} is confined to $1/T_S$. The method yields a measurement delay of $T_S/2$ and a maximum output delay of $T_S/2$, hence a maximum total delay of T_S. This maximum total delay value results in high ripple content, poor bandwidth and a low dynamic response in the application. Figure 3.37 proves the poor current tracking and switching performance of the DHCR1 in a PAF application over a fundamental cycle. Although f_{max} is limited compared to the analog hysteresis current controller case in Figure 3.34, the high current ripple content and the low average frequency result in poor current regulator performance. Therefore, multi-rate sampling of the current becomes mandatory to decrease the total delay value.

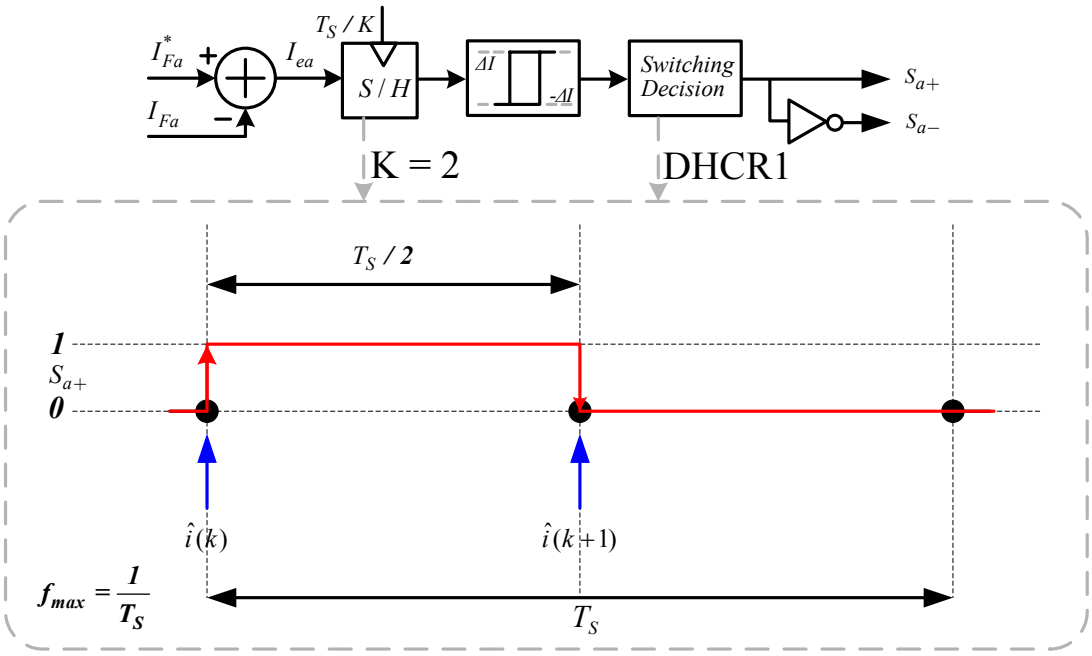

Figure 3.36 The description of DHCR1.

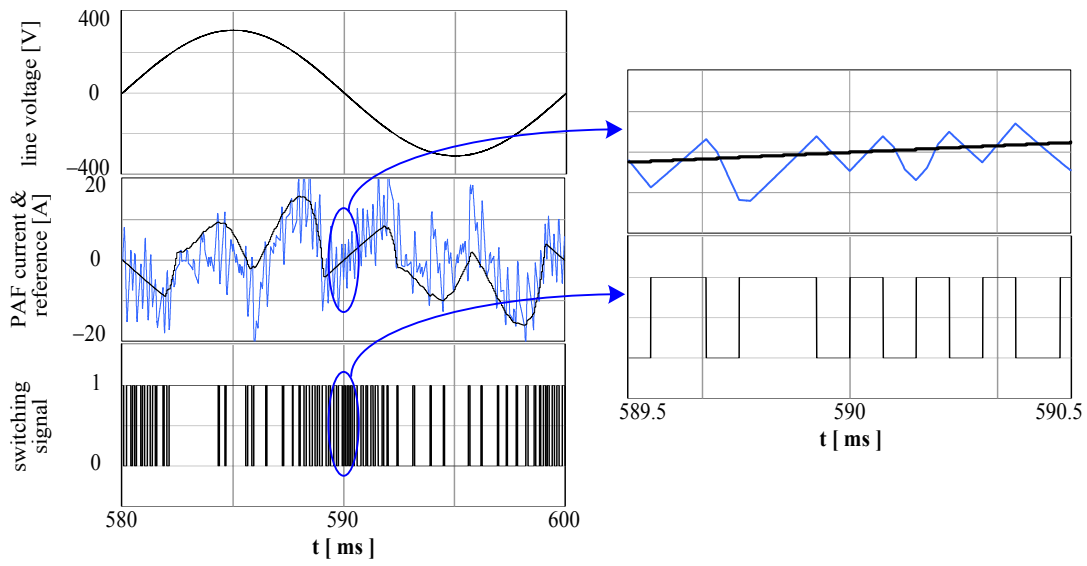

Figure 3.37 The tracking and switching performance of DHCR1 in a PAF application.

3.4.2 DHCR2

In DHCR2 described in Figure 3.38, the multi-rate sampling method is illustrated for K=10. The current samplings are illustrated as $\hat{i}(k)$, $\hat{i}(k+1)$, ... , $\hat{i}(k+9)$ in the figure. Due to oversampling, the measurement delay is decreased from $T_s/2$ to $T_s/10$. In DHCR2, once its position changes, the switch is locked for a time period of $T_S/2$ in order to limit maximum switching frequency in the time period of T_S. One possible switching signal is also illustrated in Figure 3.38. However, this lock mechanism results in maximum output release delay of $T_S/2$ if the current error exceeds the other limit just after the switch is locked. Therefore, the maximum total delay is considered to be $6T_S/10$. Figure 3.39 illustrates the current tracking and switching performance of the DHCR2 in the PAF application over a fundamental cycle. In DHCR2, the ripple content, bandwidth and the average switching frequency are partially improved due to decrease in measurement delay compared to the DHCR1 case in Figure 3.37. However, the dynamic response under high di/dt is limited due to switch lock mechanism. Therefore, appropriate switch release mechanism is necessary.

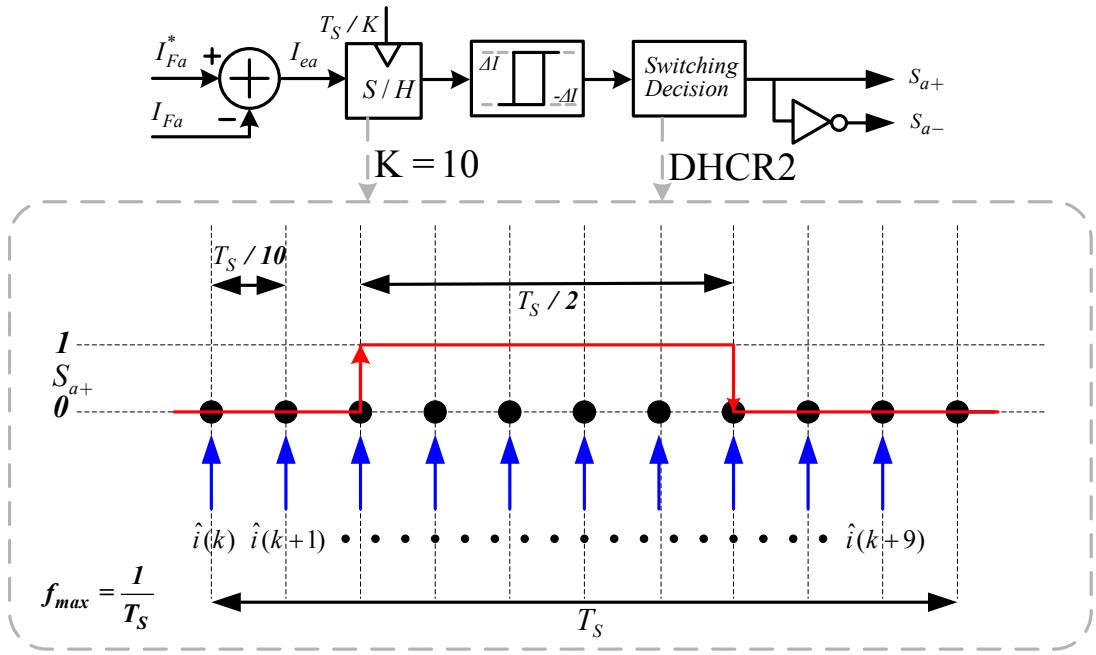

Figure 3. 38 The description of DHCR2.

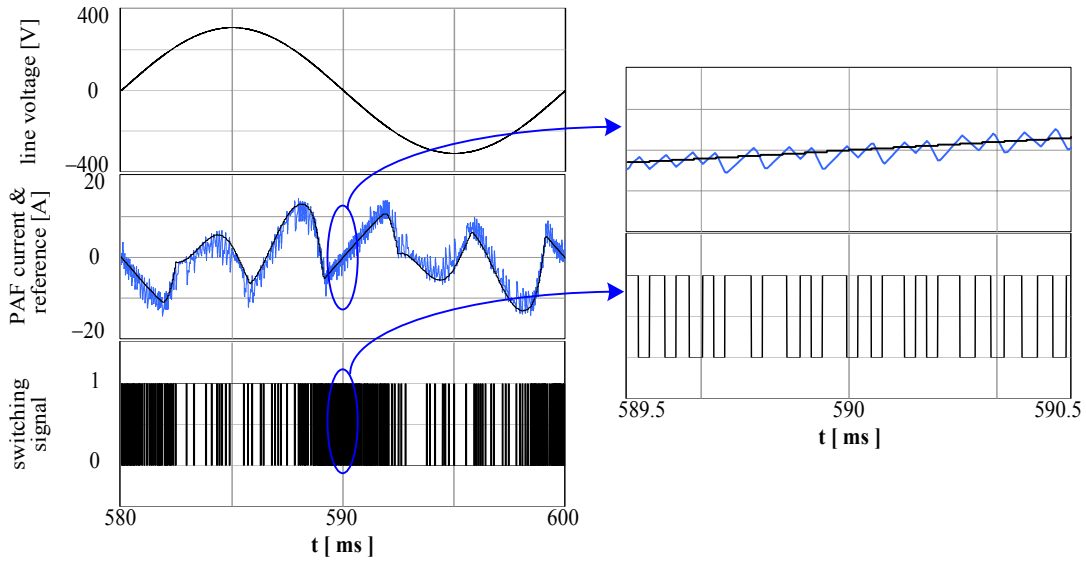

Figure 3.39 The tracking and switching performance of DHCR2 in a PAF application.

3.4.3 DHCR3

In DHCR3, described in Figure 3.40, the sampling coefficient K is 10 like in DHCR2. The output switch signals can be released such that the switch at most turns on and off once within T_S. Thus, the maximum switching frequency is confined to $1/T_s$. With this approach, the minimum measurement and output delays are reduced to $T_S/10$ each resulting in a minimum delay of $2T_S/10$. In addition to the ripple content and bandwidth improvement compared to DHCR2, the current tracking capability in high di/dt regions is improved by the release mechanism of DHCR3, as shown in Figure 3.41. If in consecutive oversampling intervals switchings occur, the total delay may become $7T_S/10$. However, in the PAF applications due to operation at high voltage utilization level, where the voltage margin for inductor current regulation is small, this condition is not practical. DHCR3 can be interpreted as high proportional gain linear CR with K discrete duty cycle outputs.

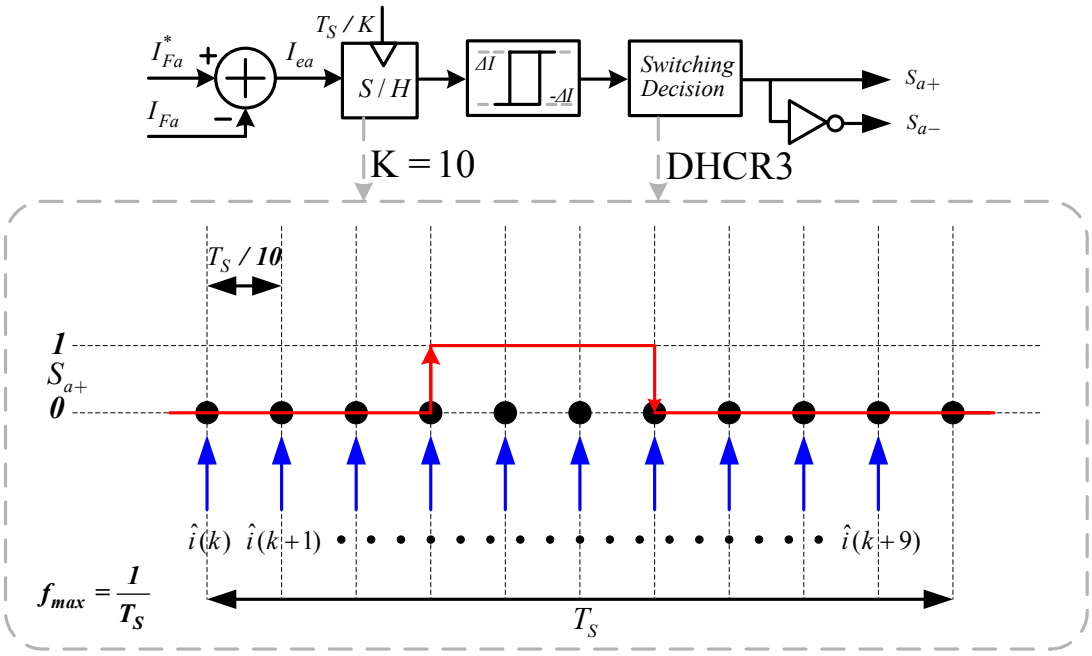

Figure 3.40 The description of DHCR3.

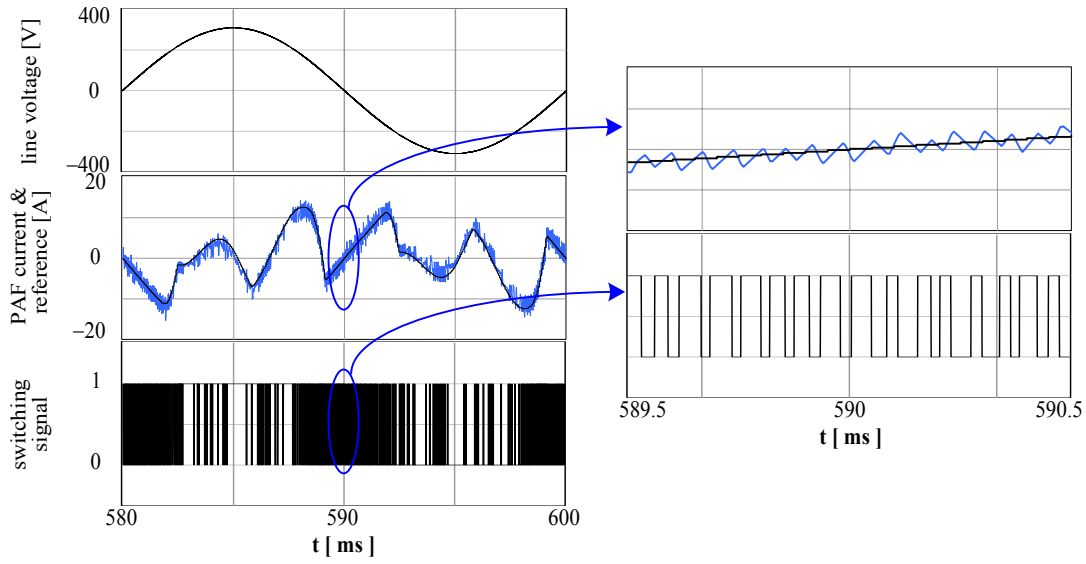

Figure 3.41 The tracking and switching performance of DHCR3 in a PAF application.

3.5 Summary

In this chapter, the existing and practically reported current regulators in PAF application classified as the linear current regulators; the LPCR, the CECR, and the RFCR, and the on-off current regulators; the AHCR and the proposed DHCR, are investigated in detail. The general features of the discussed regulators are given with the discussions of their design issues, implementations, advantages, disadvantages and performances. Besides the discussion of the existing current regulators, the most valuable contribution of this chapter is the improvisions on the discrete time hysteresis current regulator with its multi-rate feedback and switch release mechanism. These contributions reduce the ripple content and improve the tracking performance, so the bandwidth increases while considering the thermal stability in the PAF application. Before the performance analysis of the discussed current regulators by means of computer simulations and verification by the experimental results of the implemented system in Chapters 5 and 6, respectively, the next chapter discusses the switching ripple filter topologies in PAF application for the elimination of the high frequency current ripples due to the switching of the VSI.

CHAPTER 4

SWITCHING RIPPLE FILTER TOPOLOGY SELECTION AND DESIGN FOR PARALEL ACTIVE FILTER APPLICATIONS

4.1 Introduction

The PWM voltage and current ripple generated by the VSI of the PAF power circuitry can spread to the power line through the PCC where the PAF system is coupled to the power system. High frequency switching harmonics create noise problems for other loads connected to the same PCC. To filter the high frequency switching ripple currents due to the switchings of the VSI, as a result to eliminate high frequency distortions on the voltage at PCC due to these ripple currents, passive switching ripple filters (SRFs) are placed at the PCC as an integral part of the PAF. While linear current regulators generate regular PWM ripples around the switching frequency and its multiples and sidebands over the frequency spectrum, discrete hysteresis current regulators generate switching ripple in a frequency range starting from the lower sideband of the average switching frequency (f_{avg}), continuing to the maximum PWM output frequency and its wide higher sideband. Thus, the harmonic spectrum of DHCRs is spread over a very wide frequency band. Based on this discussion, it can be concluded that the current regulator type utilized in the PAF system determines the SRF type to be utilized in PAF application.

This chapter discusses the SRF topologies commonly utilized in PAF applications based on the current regulator type. By modeling the nonlinear load and the PAF without the knowledge of their parameters, the SRFs for different type of current regulators are designed based on the typical distribution of the switching ripple

current over the frequency spectrum. The SRF topologies, their filtering characteristics and sizes are investigated and compared theoretically.

4.2 Switching Ripple Filter Topologies

The choice of SRF topology is directly related to the distribution of ripple currents over the frequency spectrum, hence that is related to the current regulator type utilized in the PAF control system. While the switching ripple currents of linear current regulators is observed at switching frequency (f_{SW}) and its multiples ($2f_{SW}$, $3f_{SW}$...), switching ripple currents of hysteresis current regulators spread over a wide frequency range starting just above the frequency defined as the bandwidth of PAF current regulator. Therefore, a tuned (trap) type SRF which is tuned to f_{SW} should be utilized to filter the switching ripple currents of the PAF when utilizing linear current regulators. A high-pass type SRF should be utilized to filter the switching ripple currents of the PAF utilizing the hysteresis current regulators since the ripple currents spread over a wide frequency range. Figure 4.1 illustrates various SRF topologies utilized in the PAF application [13]. The topologies (a) and (b) in the Figure 4.1 illustrate tuned filter characteristics and are utilized for linear current regulators. The topologies (c) and (e) illustrate high-pass filter characteristics and are utilized for hysteresis current regulators. However, the topology (d) exhibits both trap and high-pass filter characteristics based on the design of the filter components and can be utilized for both current regulators. In this section, these topologies are investigated and their design specifications are given. Moreover, the numerical design of these topologies is performed for the system parameters of the AC utility grid, the nonlinear load and the PAF system utilizing different current regulator types. The advantages, disadvantages, and practical implementation of the designed SRFs are discussed. During the design procedure of the SRF topologies, the nonlinear load and the PAF system are modeled such that no system parameters are required for them. Only the AC utility grid system parameters are required since the design of the passive filters includes the harmonic resonance studies. Since the laboratory experiments will be hold in METU laboratory, the AC utility grid parameters of METU campus given in Table 4.1 are considered.

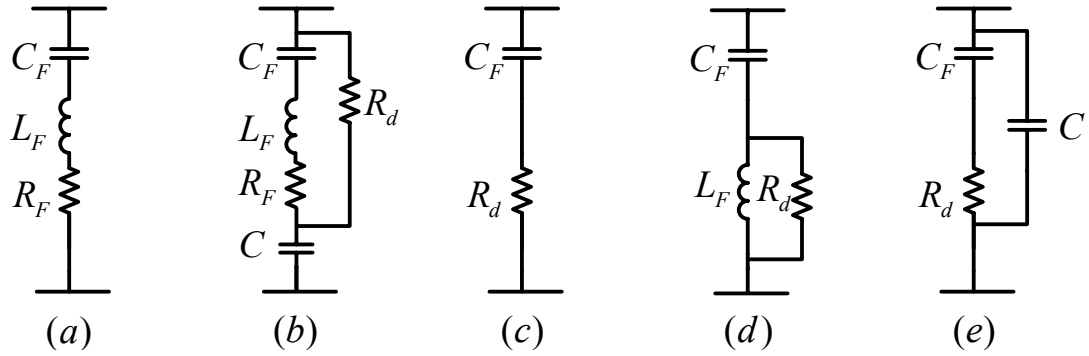

Figure 4.1 SRF topologies used in the PAF application.

Table 4.1 The AC utility grid parameters at the METU Power Electronics Laboratory

	Parameter	Value
AC utility grid	V_S (Line voltage)	380 V
	f_e (Line frequency)	50 Hz
	L_S (Line inductance)	100 µH
	R_S (Line resistance)	50 mΩ

4.2.1 Tuned LCR Type SRF

Linear current regulators create switching ripple currents at f_{SW} and its multiples when they are applied with regular sampling PWM with the modern microcontrollers/DSPs. Figure 4.2 illustrates a typical source current harmonic spectrum of a linear current regulator with f_{SW} of 20 kHz in a PAF application. The most dominant switching ripple currents appear at 20 kHz and as the frequency increases, the magnitude of the ripple current decreases. In PAF applications where linear current regulators are utilized, the tuned LCR type SRF illustrated in Figure 4.1.a is generally utilized for a switching ripple current free AC utility grid line (source) current.

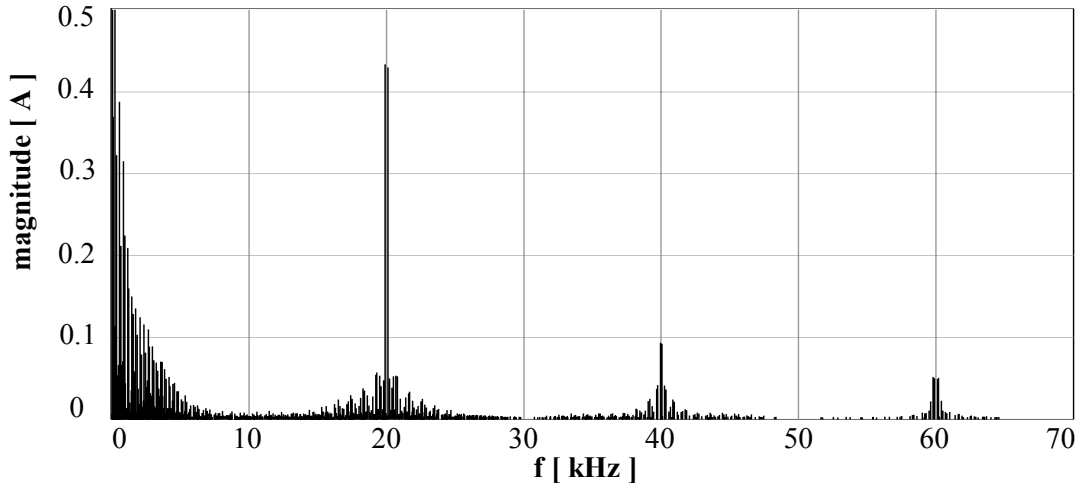

Figure 4.2 Typical line current harmonic spectrum in a PAF application with the linear current regulators.

The series resonant frequency (f_s) of the filter is defined as

$$f_s = \frac{1}{2\pi\sqrt{L_F C_F}} \tag{4.1}$$

where L_F is the filter inductance and C_F is the filter capacitance. The impedances of C_F and L_F are equal in magnitude with opposite signs at f_s. Therefore they cancel each other and the total impedance of filter is equal to filter resistance R_F at f_s. Since the aim of the filter is to sink the switching ripple currents through its path by providing low impedance, the value of R_F should be low. Hence, the internal resistance of L_F typically constitutes the R_F value. By tuning f_s of the LCR filter to f_{SW}, the most dominant switching ripple currents at f_{SW} are filtered through the low impedance path.

When a tuned LCR filter is designed to sink the low frequency harmonics of the load current (conventional approach), the filter capacitor C_F is sized according to the reactive power demand of the load at the fundamental frequency. However, when it is utilized as SRF, C_F is sized according to the attenuation of the second dominant switching ripple currents at $2f_{SW}$. Figure 4.3 illustrates impedance characteristics

(magnitude of filter impedance $Z_F(s)$) of LCR filter tuned to 20 kHz for various C_F sizes. The utilized R_F value for the filter is 100 mΩ, which is assumed to be the internal resistance value of the filter inductor L_F. Since the filter is tuned to 20 kHz, the impedance of the filter at 20 kHz is low. However, as the filter capacitor size decreases, the sharpness of the filter increases. This results in poor filtering of switching ripple currents at the sidebands of f_{SW}. Moreover, as filter capacitor size decreases, the filter impedance at $2f_{SW}$ (40 kHz) increases, which means that the attenuation of the second dominant switching ripple currents at $2f_{SW}$ is poor. Therefore, the capacitor size should be kept as high as possible for a better attenuation of the switching ripple currents.

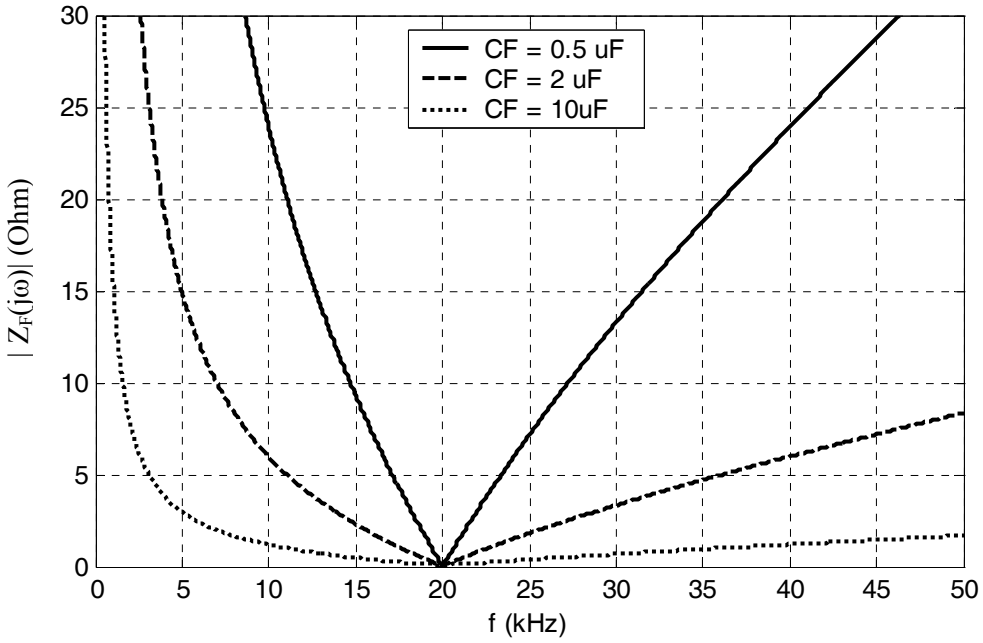

Figure 4.3 Impedance characteristics of an LCR filter tuned to 20 kHz for various C_F values.

However, as the capacitor size increases, the parallel resonant frequency (f_p) in (4.2) that occurs between the filter components and the line inductance (L_S) decreases. A low f_p value is undesired since it increases the possibility of the oscillations at this frequency, which will be explained in the following. Therefore, f_p restricts the C_F size in tuned LCR type SRF design.

$$f_p = \frac{1}{2\pi\sqrt{(L_S + L_F)C_F}} \tag{4.2}$$

The parallel resonance condition can be explained by examining Figure 4.4 illustrating the equivalent circuit model of the load, PAF, SRF and AC utility grid (source) at harmonic frequencies. In Figure 4.4, the load and the PAF are modeled as a current source of I_H at harmonic frequencies. This current source of I_H models the uncompensated current harmonics at the range of the PAF bandwidth, the load current harmonics above the PAF bandwidth and the switching ripple currents of linear current regulators at f_{SW} and its multiples. By neglecting the AC utility grid voltage harmonics, the AC utility grid is modeled by the line inductance L_S at harmonic frequencies. Since the aim of SRF is to filter the switching ripple currents, the SRF current I_{HF} is desired to be switching ripple currents, which are the components of I_H. The line current I_{HS} is then desired to be the sum of the uncompensated current harmonics at the range of the PAF bandwidth and the load current harmonics above PAF bandwidth. Therefore, if the s-domain transfer function T(s) in (4.3) giving the proportion of I_{HS} to I_H is defined, the filtering characteristics of the SRF can be obtained. Ideally, the magnitude of T(s) (frequency response, $|T(j\omega)|$) is '0' for switching ripple current frequencies and '1' for other frequencies. This constraint means that the designed SRF only filters (sinks) the switching ripple currents that the PAF system generates.

$$T(s) = \frac{I_{HS}(s)}{I_H(s)} \tag{4.3}$$

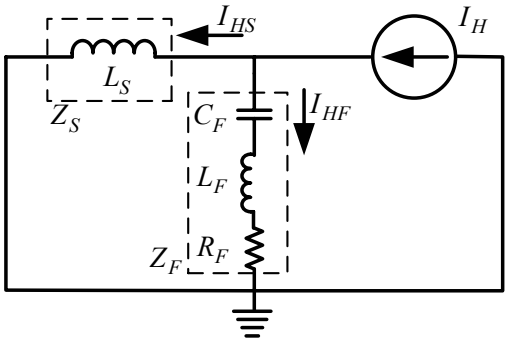

Figure 4.4 Equivalent circuit model of the load, PAF, tuned LCR type SRF, and AC utility grid at harmonic frequencies.

If the low R_F value is neglected, the magnitude of T(s) in terms of the tuned LCR filter components is as in (4.4).

$$\left|\mathrm{T(s)}\right| = \left|\frac{I_{HS}(\mathrm{s})}{I_H(\mathrm{s})}\right| = \left|\frac{Z_F(\mathrm{s})}{Z_F(\mathrm{s})+Z_S(\mathrm{s})}\right| = \frac{(2\pi f)^2 L_F C_F - 1}{(2\pi f)^2 (L_F + L_S) C_F - 1} \tag{4.4}$$

Equation (4.4) implies that the T(s) magnitude is '0' at the series resonant frequency f_s defined in (4.1) and infinite at the parallel resonant frequency f_p defined in (4.2). The meaning of the infinite magnitude can be explained as follows. If the system is excited by the harmonic currents at f_p, the parallel impedance constituted by the line inductance impedance and SRF impedance has a high value, resulting in high amplitude voltage harmonics and oscillations (harmonic resonance amplification) in the system. The above discussion explains why the parallel resonance is an undesired condition in the power system.

Although they create parallel resonance risk, the utilization of tuned LCR filters as SRF is unavoidable due to their simple structure, efficiency, and low cost. In tuned LCR type SRF, the design constraints can be summarized as follows. The created parallel resonant frequency should be tuned to safe frequency range where the possibility of the parallel resonance occurrence is low, the series resonant frequency should be tuned to f_{SW}, and capacitor size in SRF structure should be large for a better attenuation of switching ripple currents. Figure 4.5 illustrates the magnitude of T(s) in (4.4) for various C_F sizes where f_s is 20 kHz, R_F is 0.1 Ω and L_S is 100 μH. In the figure, the peak values of parallel resonance for various C_F are finite since R_F is not assumed to be zero. The figure illustrates that f_p decreases as the C_F size increases. While f_p is around 15 kHz for C_F=0.5 μF, f_p is around 5 kHz for C_F= 10 μF. Figure 4.6 is the detailed illustration of Figure 4.5 for low magnitude values. As C_F size increases, the T(s) magnitude for higher frequencies decreases. Low T(s) magnitude means that the filtering capability increases for switching ripple currents at higher frequencies. A safe frequency range for parallel resonant frequency is determined by investigating the line current harmonic spectrum (FFT) without SRF. While investigating the equivalent circuit in Figure 4.4, it is mentioned that the

current source I_H involves the uncompensated current harmonics at the range of the PAF bandwidth and the load current harmonics above PAF bandwidth. These harmonics spread over a frequency range up to 10 kHz as the line current harmonic spectrum for linear current regulators in PAF application in Figure 4.2 illustrates. Moreover, there exists a harmonic free frequency range between 10 kHz and 15 kHz in Figure 4.2. When f_p in (4.2) is chosen as 10 kHz for large C_F size and f_s in (4.1) is chosen as 20 kHz, two unknown circuit parameters C_F and L_F are found from two equations as

$C_F = 1.9$ μF

$L_F = 33.3$ μH

for L_S value of 100 μH. Therefore, the design values of L_F and C_F are determined for the PAF utilizing linear current regulator with f_{SW} of 20 kHz.

It is mentioned that filter resistance R_F should be low for better switching ripple filter attenuation and the internal resistance of L_F typically constitutes R_F value. However, the peak values of the parallel resonance can be decreased by increasing R_F value or employing an external resistor to the filter structure. Figure 4.7 illustrates the effect of R_F value to the magnitude of T(s) for the designed SRF with $C_F = 1.9$ μF and $L_F = 33.3$ μH. As the R_F value increases, the parallel resonance is damped out since the T(s) magnitude approaches towards its ideal value of '1' for low frequencies. However, the increase in R_F value results in T(s) magnitude increase at f_s of 20 kHz, which means that filtering capability of the SRF decreases. The T(s) magnitude at 20 kHz is 0.6 for a R_F value 10 Ω. That illustrates that 60% of the most dominant switching ripple currents at 20 kHz is observed on the line current and the SRF does not attenuate these currents. Therefore, the sensitivity of the tuned LCR type SRF to the R_F value is high and R_F should be kept as low as possible for better switching ripple current attenuation.

In this section, the tuned LCR type filter utilized as SRF in PAF applications with linear current regulators is investigated and designed. Although, the filter has the risk

of parallel resonance with the line inductance, it provides a low impedance path for the switching ripple currents of the linear current regulators at f_{SW} and its multiples. As a result, the switching ripple harmonic free AC utility grid is obtained. Moreover, the effect of parallel resonance at power system is investigated. Although the parallel resonant frequency is tuned to a safe frequency value for the analyzed system, it should be damped out since there exists an excitation possibility of the parallel resonance by the loads connected to the power system at PCC and creating harmonic currents. The topology in the next section is an effective solution to the parallel resonance problem with the addition of the passive circuit components to the tuned LCR type filter.

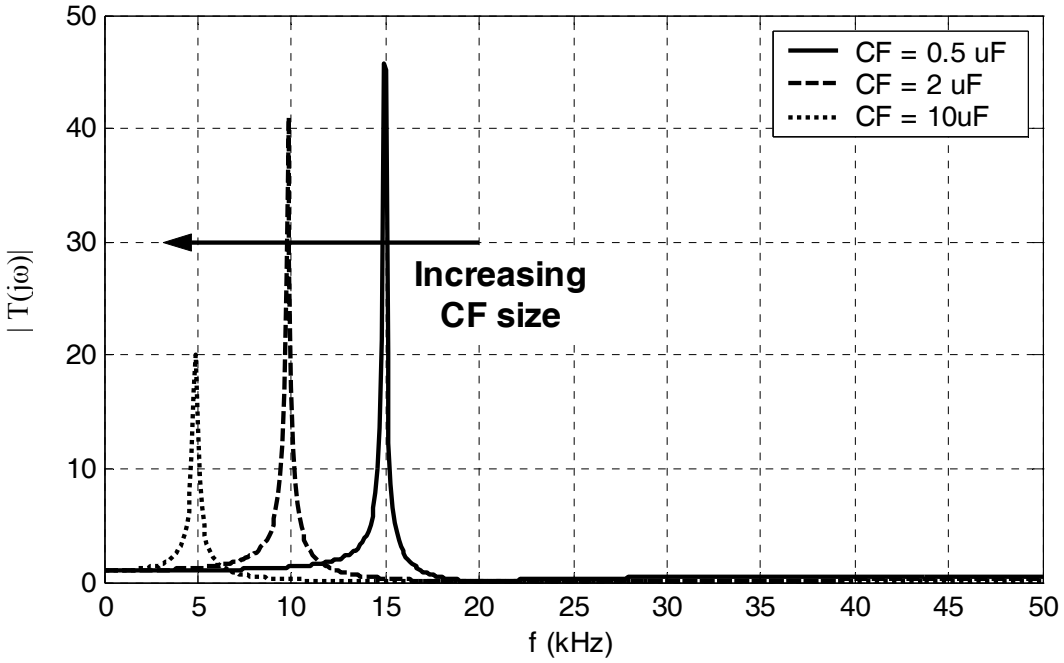

Figure 4.5 T(s) magnitude of the tuned LCR type SRF for various capacitor C_F sizes.

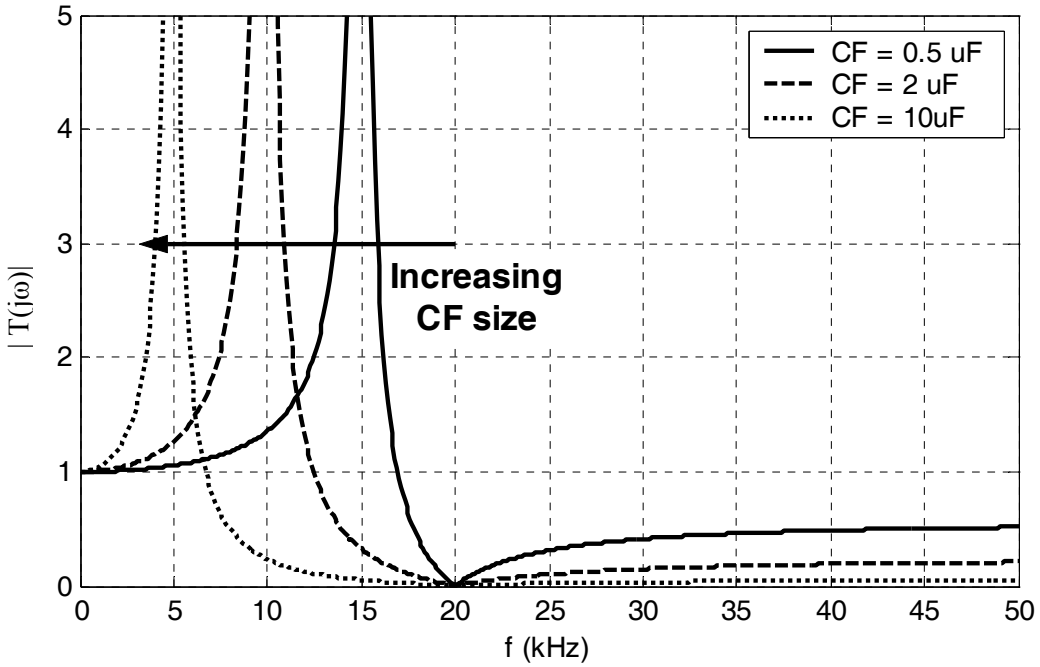

Figure 4.6 The detailed illustration of T(s) magnitude of the tuned LCR type SRF for various capacitor C_F sizes.

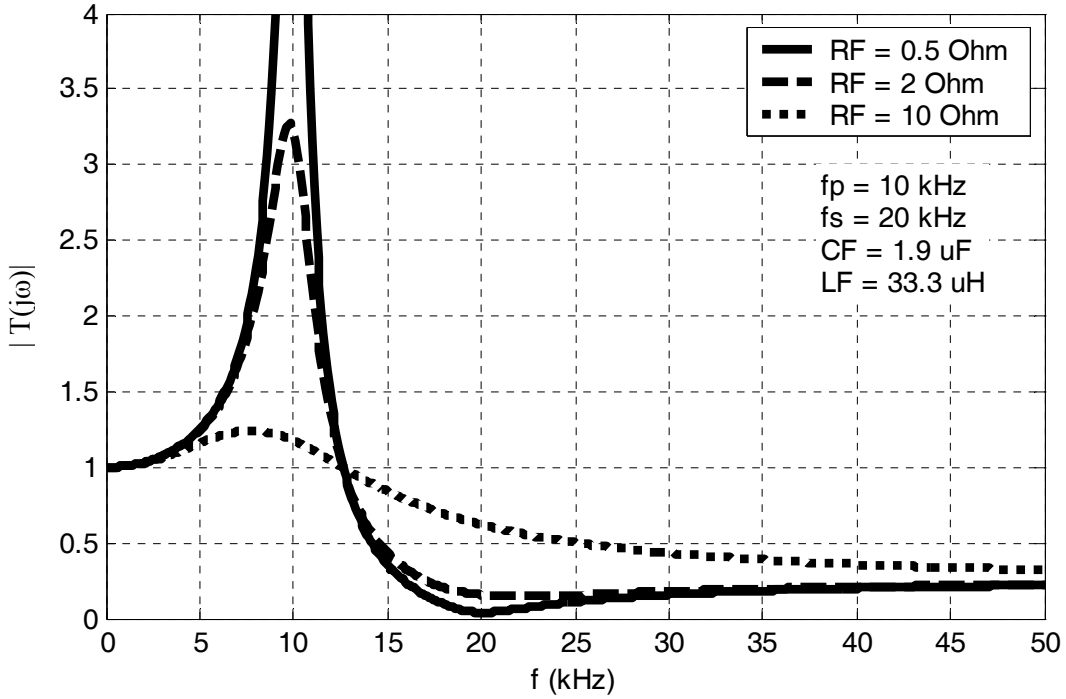

Figure 4.7 T(s) magnitude of the tuned LCR type SRF for various resistor R_F values.

4.2.2 Broad-band Tuned Type SRF

The broad-band tuned type SRF illustrated in Figure 4.1.b is utilized to filter the switching ripple currents created by the linear current regulators in the PAF application while providing passive damping of the parallel resonance for a wide frequency range. The filter involves two separate paths; one for the attenuation of the switching ripple currents and the other for wide frequency range damping of the load and/or source side induced resonances. While the series resonant frequency of L_F-C_F arm of the filter (4.1) is tuned to f_{SW} as in the case of the tuned LCR type to filter the switching ripple currents, the value of the filter damping resistor R_d is selected such that it will damp out the resonances for a wide frequency range with the capacitor C connected in series with the two parallel connected arms.

The series resonant frequency of the broad-band tuned type filter f_s is defined as

$$f_s = \frac{1}{2\pi\sqrt{L_F \dfrac{C_F C}{C_F + C}}} \tag{4.5}$$

with the inclusion of C to the filter structure compared to the series resonant frequency of tuned LCR type filter defined in (4.1). In order to approximate f_s tuned to f_{SW} as

$$f_s \cong \frac{1}{2\pi\sqrt{L_F C_F}} \tag{4.6}$$

in terms of L_F and C_F values for the design simplicity, the size of C should be

$$C_F << C \tag{4.7}$$

compared to the size of C_F. In order to satisfy inequality (4.7), small C_F size can be utilized. However, small C_F sizes increase the sharpness of the filter such that the

attenuation of the switching ripple currents at sidebands of f_{SW} and $2f_{SW}$ is poor as discussed for the tuned LCR type filter case in Section 4.2.1. Moreover, (4.6) illustrates that small C_F sizes result in large L_F values for a fixed f_{SW} value. The large L_F values increases the total cost of the filter. Therefore, the C_F and L_F values for the broad-band tuned type SRF are chosen the same as the designed values of C_F = 1.9 μF and L_F = 33.3 μH for the tuned LCR type SRF. As a result, the size of C is to be selected in order to satisfy (4.7). The size of C is chosen as 20 μF such that

$$10C_F < C \tag{4.8}$$

is satisfied for C_F = 1.9 μF. Larger C sizes can be selected for the topology. However, the larger C sizes are not preferred since they result in excessive reactive power at the fundamental frequency and the reactive power demand of the load is compensated by the PAF. In the latter part of the section, the effect of larger C size to filter characteristics will be illustrated.

The reactive power Q defined in (4.9) is 900 VAr for the selected C value of 20 μF and line voltage of 380 V and line frequency of 50 Hz. This reactive power results in a leading power factor value of 0.94 if the diode rectifier load with full load rating of 10 kW is operated at 25% load without the PAF. This power factor value provides information about the size of designed C for the filter structure. Moreover, f_s defined in (4.5) is 21 kHz for C = 20 μF and is close enough to f_{SW} value of 20 kHz.

$$Q = 2\pi f V^2 C \tag{4.9}$$

The value of the damping resistance R_d should be selected such that it provides sufficient damping for frequencies below f_{SW}. For this purpose, the equivalent system model and T(s) of the broad-band tuned filter should be derived as in the tuned LCR type SRF case. By utilizing the system model illustrated in Figure 4.4 and replacing the tuned LCR type SRF with the broad-band tuned type SRF, the harmonic equivalent circuit model of the system for broad-band tuned type SRF can be obtained and is illustrated in Figure 4.8. The transfer function T(s) defined as the

proportion of the line current I_{HS} to harmonic current source I_H for broad-band tuned type SRF case is given in terms of filter circuit components C_F, L_F, C, and R_d as follows.

$$\mathrm{T}(s) = \frac{\mathrm{s}^3 L_F C_F C R_d + \mathrm{s}^2 L_F C_F + \mathrm{s}(C_F + C)R_d + 1}{\mathrm{s}^4 L_S L_F C_F C + \mathrm{s}^3 (L_F + L_S) C_F C R_d + \mathrm{s}^2 (L_F C_F + L_S C) R_d + \mathrm{s}(C_F + C) R_d + 1} \qquad (4.10)$$

The magnitude of T(s) (| T(s)|) in (4.10) should be analyzed for various R_d values and the designed values of C_F, L_F, and C and then, the R_d value should be selected such that it provides sufficient damping for a wide frequency range. Figure 4.9 illustrates T(s) magnitude for various R_d values, the designed filter parameters and line inductance value of 100 μH.

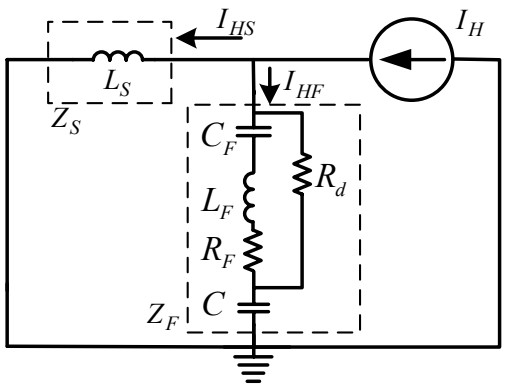

Figure 4.8 Equivalent circuit model of load, PAF, broad-band tuned LCR type SRF, and AC utility grid at harmonic frequencies.

Figure 4.9 illustrates that as the R_d value decreases, the effect of parallel resonant frequency which occurs between filter capacitor C and line inductance L_S ($\mathrm{f_{p1}}$) given as

$$\mathrm{f_{p1}} \cong \frac{1}{2\pi\sqrt{L_S C}} \qquad (4.11)$$

is dominant and the T(s) magnitude increases around f_{p1}. As R_d increases, the effect of parallel resonant frequency which occurs between filter capacitor C_F, filter inductor L_F and line inductance L_S (f_{p2}) given as

$$f_{p2} \cong \frac{1}{2\pi\sqrt{(L_S + L_F)C_F}} \tag{4.12}$$

is dominant and T(s) magnitude increases around f_{p2}. Therefore, the R_d value should be selected such that harmonics between the two resonant frequencies are damped effectively. For R_d = 5 Ω in Figure 4.9, the two resonant frequencies are damped and T(s) magnitude has a concave shape where the value of T(s) magnitude is just above the value of '1' for the frequencies below f_{SW}. As a result damping for a wide frequency range is achieved with R_d = 5 Ω.

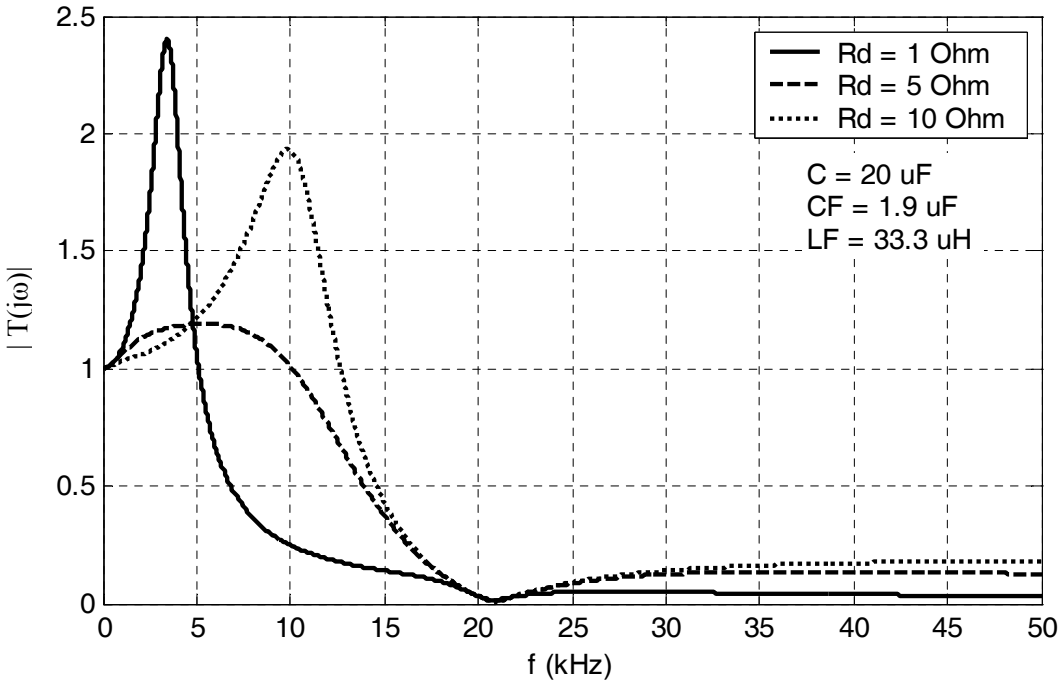

Figure 4.9 T(s) magnitude of the broad-band tuned SRF for various R_d values.

The magnitude of T(s) is desired to be as close as possible to unity for low frequencies. The T(s) magnitude for low frequencies can be approximated to unity by increasing the C size with constant C_F, L_F and R_d values. Figure 4.10 illustrates T(s) magnitude for various C sizes where C_F, L_F and R_d values are the designed values. As C size increases, T(s) magnitude comes closer to unity. This illustrates the effect of larger C values to damping. However, as C size increases, the fundamental frequency current passing through R_d instead of high impedance L_F -C_F arm of the filter increases. This results in power loss increase at the fundamental frequency. Moreover, as the C size increases, the capacitive reactive power supplied to system increases. Consequently, large C sizes result in filter size, cost, power loss, and reactive power increase and large C sizes are not practically preferred.

As discussed at the beginning of the section, (4.7) should be satisfied in order to approximate f_s tuned to f_{SW}. As a discussion, it is mentioned that small C_F sizes can be utilized instead of utilizing large C size to satisfy (4.7) in design procedure. Figure 4.11 illustrates the magnitude of T(s) for various L_F and C_F values tuned to 20 kHz and R_d values selected as to provide sufficient damping for a wide frequency range while keeping C at its design value of 20 μF. Filter parameters for this case are illustrated on the figure. As C_F size decreases, the sharpness of the filter increases at around the switching frequency of 20 kHz, which results in poor filtering of switching harmonic currents at the sidebands of f_{SW}. The magnitude of T(s) increases at 40 kHz for small C_F sizes such that the filtering of the 2nd dominant harmonics is poor. Moreover, small C_F sizes results in large L_F and R_d values, thus resulting in high cost and power loss for the designed filter. As a result, small C_F sizes results in poor filtering capability and cost and power loss increase, are not preferred in the practical design procedure.

When the broad-band tuned type SRF discussed in this section is compared to the tuned LCR type SRF in the previous section, the new topology has the same filtering capability for switching ripple currents while it provides broad-band damping with R_d in its structure. However, the new topology is big in size and costly, has power loss component in its structure compared to tuned LCR type SRF.

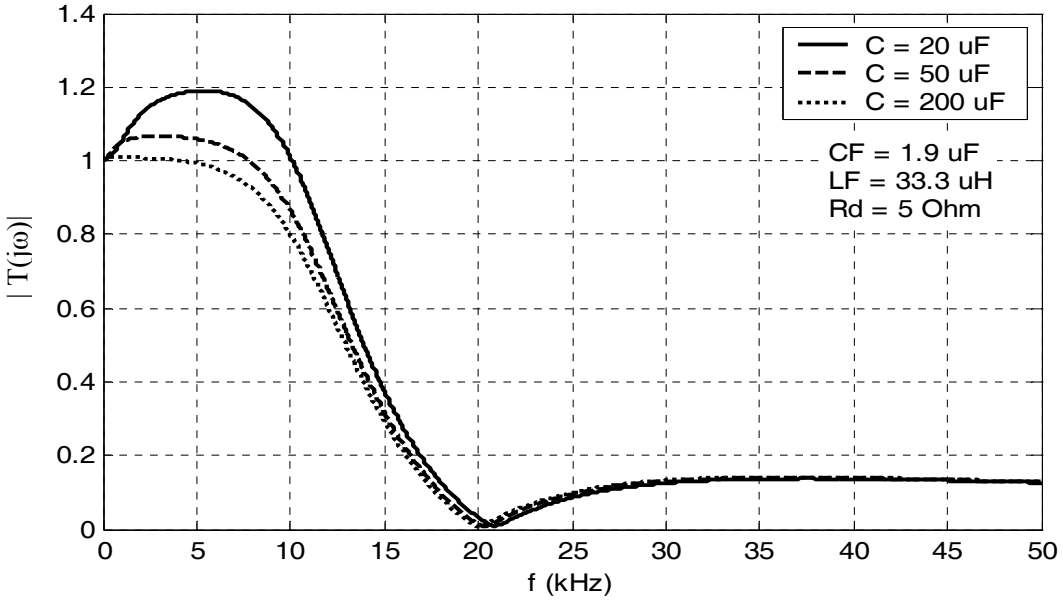

Figure 4.10 T(s) magnitude of the broad-band tuned type SRF for various *C* values.

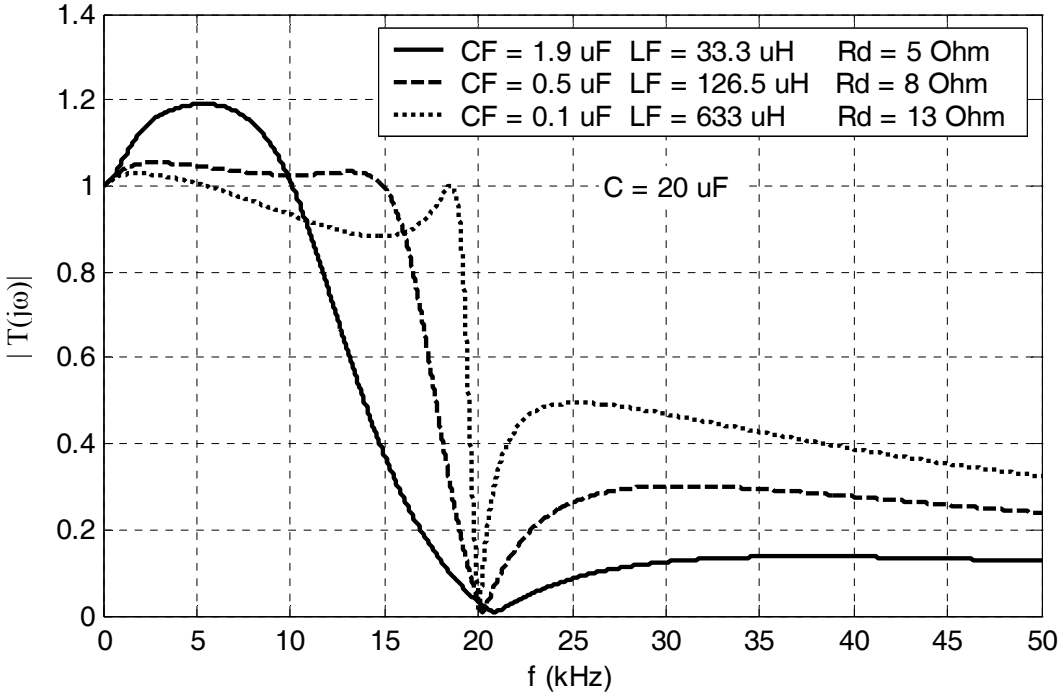

Figure 4.11 T(s) magnitude of the broad-band tuned type SRF for various C_F, L_F and R_d values.

4.2.3 High-pass RC Type SRF

Hysteresis current regulators create switching ripple currents spreading over a wide frequency range starting from just above the frequency defining their bandwidth (f_{bw}). Figure 4.12 illustrates line current harmonic spectrum of the PAF utilizing DHCR3 as current regulator. If the line current harmonic spectrum in Figure 4.12 is compared to the line current harmonic spectrum of linear current regulators in Figure 4.2, it can be noticed that the switching ripple currents do not concentrate at fixed frequency range contrary to the linear current regulator case and spread over a wide frequency range starting from low frequencies due to the variable switching frequency. In PAF applications where hysteresis current regulators are utilized, high-pass RC type SRF illustrated in Figure 4.1.c is utilized to provide wide frequency range attenuation of the switching ripple currents. While the impedance of filter has a high value of ($1/\omega C_F$) below its cut-off frequency (for low frequencies), it is the value of R_F for high frequencies. The R_F component in the filter structure is utilized to damp out the source and/or load side resonances.

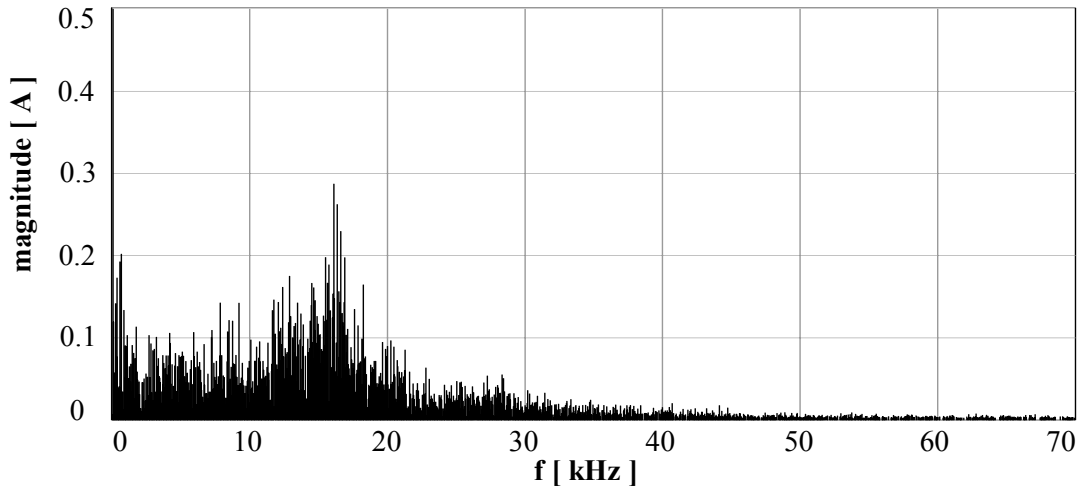

Figure 4.12 Line current harmonic spectrum in the PAF application with DHCR3.

Harmonic frequency equivalent circuit model of the system for high-pass RC type SRF is illustrated in Figure 4.13. The current source I_H in the figure models the uncompensated current harmonics at the range of the PAF bandwidth, the load current harmonics above the PAF bandwidth and the switching ripple currents of the

hysteresis current regulator spreading over a wide frequency range (switching ripple currents below and above the average switching frequency). Since the aim of the SRF is to sink the switching ripple currents, the SRF current I_{HF} is desired to consist of the switching ripple currents of the hysteresis current regulator starting from just above f_{bw}. Therefore I_{HF} involves load current harmonics above the PAF bandwidth and the switching ripple currents of hysteresis current regulator contrary to the linear current regulator case.

The cut-off frequency of the filter is just above the parallel resonant frequency given in (4.13) which occurs between capacitor C_F and line inductor L_S. Therefore, the bandwidth of current regulator should be known to find C_F size from (4.13) for a known L_S value. The f_{bw} value of the DHCR3 obtained from computer simulations and experimental results in Chapter 5 and 6 respectively is nearly between 2.5 and 3 kHz. In order to have small C_F size in (4.13), f_p is taken as 3 kHz and C_F is found as 30 μF from (4.13) for line inductance L_S value of 100 μH.

$$f_p = \frac{1}{2 \times \pi \times \sqrt{L_S \times C_F}} \tag{4.13}$$

The effect of R_d on damping and filtering characteristics can be analyzed by obtaining the transfer function T(s) defined as the proportion of the line current I_{HS} to harmonic current source I_H for high-pass RC type SRF in (4.14). Figure 4.14 illustrates the magnitude of T(s) for various R_d values and C_F value of 30 μF. The figure illustrates that when the low R_d values are utilized, the filtering capacity can be enhanced for the frequencies above 5 kHz. However, the parallel resonance peak at low frequencies has a high value in this case. If the R_d value is increased to damp out the resonance, filtering capacity for higher frequencies degrades and filtering of switching ripple current of the hysteresis current regulator spreading over a wide frequency range is poor. Moreover, since the low cut-off frequency of the filter results in large C_F size, the current at fundamental frequency through filter is large in magnitude due to large C_F size and results in excessive power loss for high R_d values. Therefore, in the high-pass RC type filter design, the value of R_d is to be as low as possible for low power loss while providing sufficient damping for induced

resonances. Although the high-pass RC type filter has the disadvantages of power loss and parallel resonance, it is preferred in industrial applications due to its simple structure and small size. Since the effect of parallel resonance is observable on the line current THD and waveform, and line voltage THD at PCC, the R_d value will be determined by means of computer simulations and experimental studies.

$$\mathrm{T}(s) = \frac{I_{HS}(\mathrm{s})}{I_H(\mathrm{s})} = \frac{\mathrm{s}C_F R_d + 1}{\mathrm{s}^2 L_S C_F R_d + \mathrm{s}C_F R_d + 1} \tag{4.14}$$

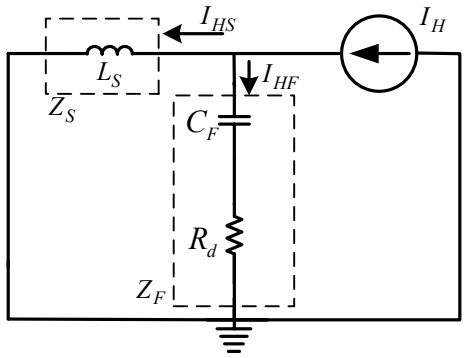

Figure 4.13 Equivalent circuit model of load, PAF, high-pass RC type SRF, and AC utility grid at harmonic frequencies.

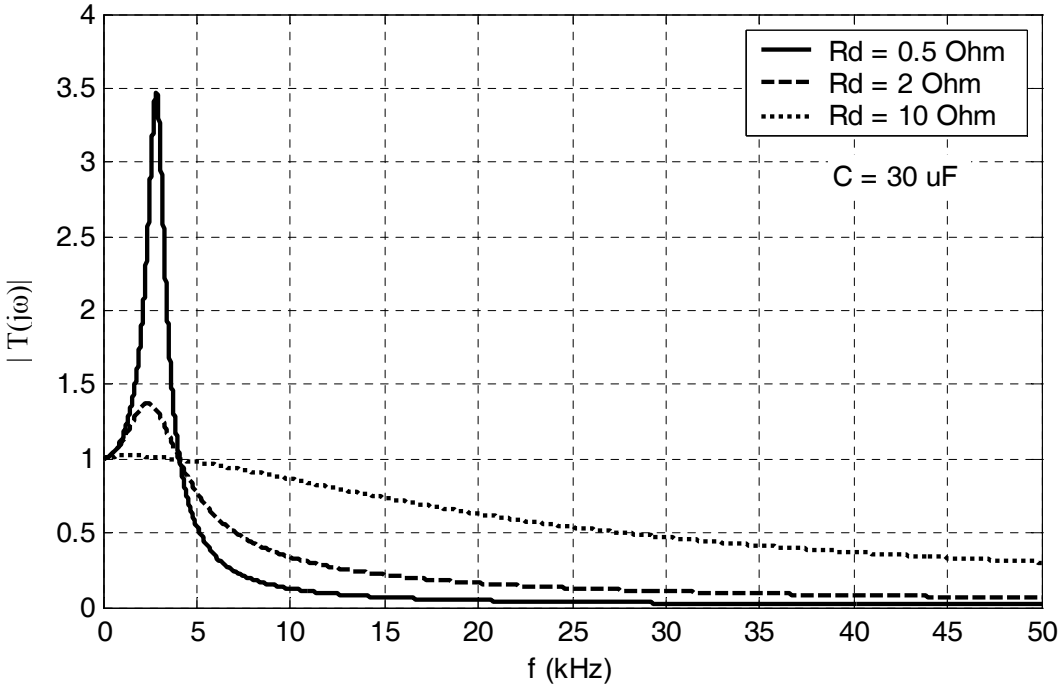

Figure 4.14 T(s) magnitude of the high-pass RC type SRF for various R_d values and C_F =30 μF.

4.2.4 High-pass LCR type SRF

The high-pass LCR type filter illustrated in Figure 4.1.d exhibits a tuned filter characteristic if the series resonant frequency of C_F and L_F in its structure is tuned to f_{SW}. Moreover, it exhibits high-pass filter characteristics due to resistor R_d in its structure. R_d also provides damping for resonances.

For tuned filter characteristics, the impedance of L_F should be smaller than R_d at the switching frequency f_{SW}. Figure 4.15 illustrates the impedance characteristics of the high-pass LCR type SRF for various R_d values and C_F = 1.9 µF and L_F = 33.3 µF, which are the design values for the tuned LCR type SRF in section 4.2.1. As the R_d value increases, the filter impedance characteristic resembles the impedance characteristics of tuned filter and looses its high-pass characteristics. Therefore, its impedance characteristic exhibits tuned filter characteristics to filter the most dominant switching ripple currents at f_{SW} for the linear current regulators with high R_d values. The transfer function T(s) defined as the proportion of the line current I_{HS} to the harmonic current source I_H for high-pass LCR type SRF is given as follows.

$$T(s) = \frac{s^2 L_F C_F R_d + sL_F + R_d}{s^3 L_S L_F C_F + s^2 (L_F + L_S) C_F R_d + sL_F + R_d} \tag{4.15}$$

Figures 4.16 and 4.17 illustrate the magnitude of T(s) for various R_d values and C_F=1.9 µF and L_F=33.3 µF including line inductance L_S value of 100 µH. The figures illustrate that as the R_d value decreases, the parallel resonance is damped out, however the filtering capacity of the dominant switching ripple currents at 20 kHz decreases. The filtering capacity increases for larger values of R_d. However, the resonance can not be damped efficiently such that the filter characteristic in this case does not differ from the tuned LCR type case. The resistor R_d in this structure increases the size of the filter. Therefore, this topology is not favoured as an SRF for linear current regulators.

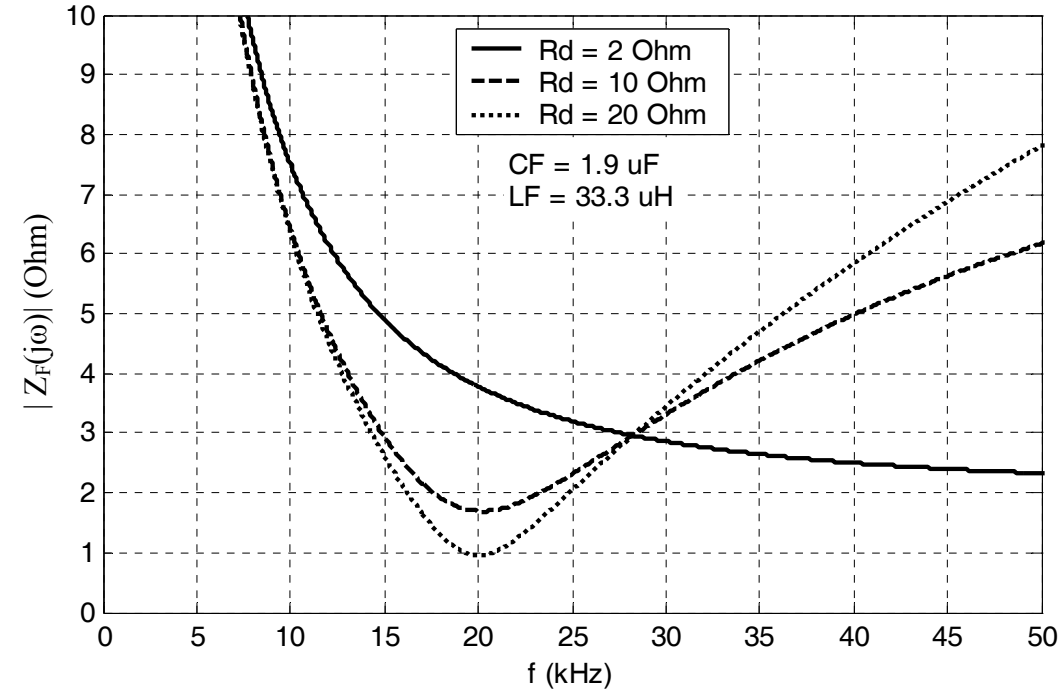

Figure 4.15 Impedance characteristics of the high-pass LCR type filter tuned to 20 kHz for various R_d values.

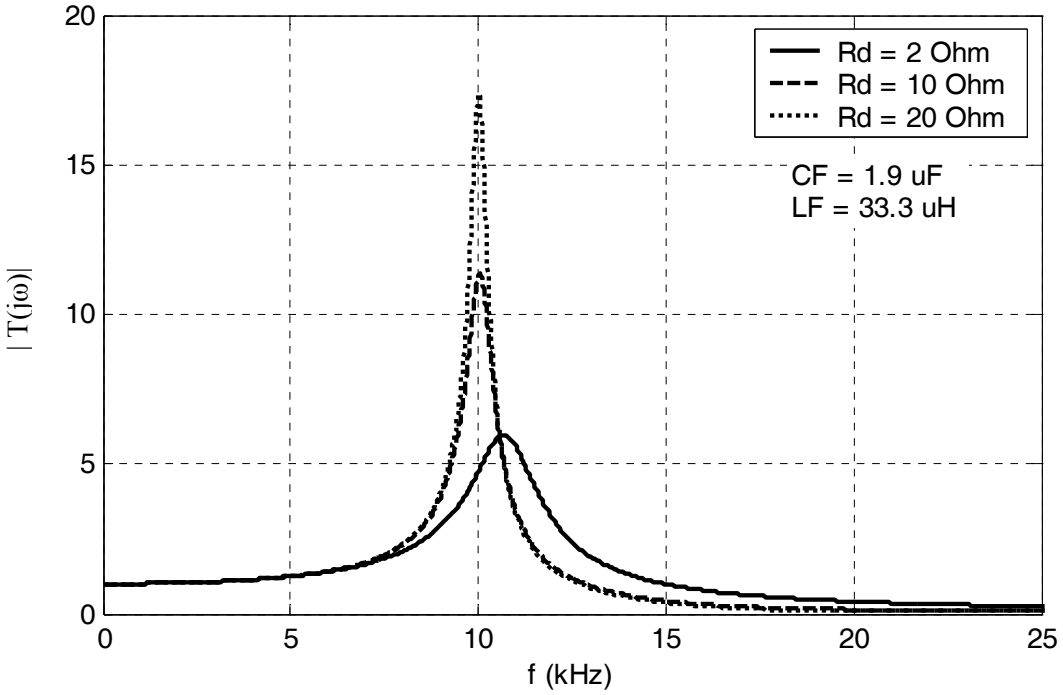

Figure 4.16 T(s) magnitude of the high-pass LCR type SRF tuned to 20 kHz for various R_d values.

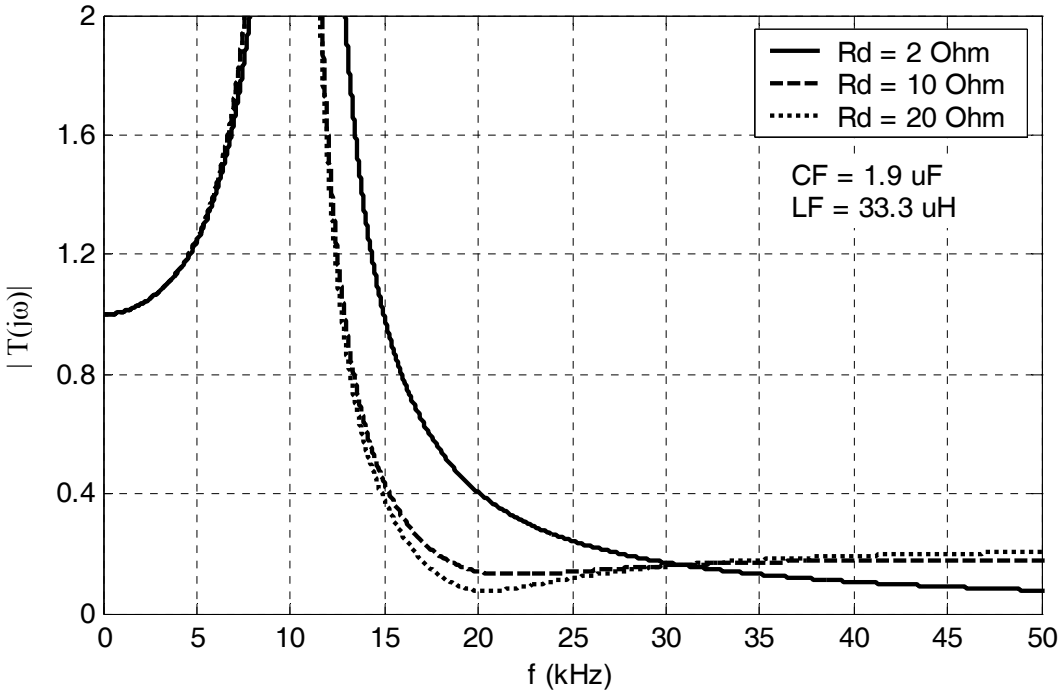

Figure 4.17 The detailed illustration of T(s) magnitude of the high-pass LCR type SRF tuned to 20 kHz for various R_d values.

The high-pass characteristics of the topology can be utilized to filter the switching ripple currents of the hysteresis current regulators spreading over a wide frequency range. For this purpose, the capacitor size in the filter structure should be as large as possible as in the high-pass RC filter case. In order to provide sufficient attenuation for the switching ripple currents above f_{bw}, the inductance L_F in the filter structure should satisfy the inequality given in (4.16). The advantage of the topology compared to the high-pass RC type filter topology in hysteresis current regulator applications is that the large fundamental current due to large C_F size drawn from AC utility grid passes through the L_F branch. Therefore, power loss at fundamental frequency on R_d is eliminated compared to the high-pass RC type topology.

$$2\pi f_{bw} L_F >> R_d \tag{4.16}$$

The topology size can be compared to the high-pass RC type topology size by utilizing the designed values of C_F = 30 μF and R_d= 2 Ω for the high-pass RC type SRF. In order to satisfy (4.16), the value of L_F is chosen such that

$$2\pi f_{bw} L_F > 10 R_d \tag{4.17}$$

for R_d = 2 Ω and f_{bw} = 3 kHz. Therefore, the minimum inductance value of L_F is found as follows.

$$L_{F\min} \cong 1 \text{ mH} \tag{4.18}$$

The T(s) magnitude of the designed high-pass LCR filter is compared to T(s) magnitude of the designed high-pass RC filter in Figure 4.18 for C_F = 30 μF and R_d = 2 Ω. The figure shows that the characteristics of both designed filters are nearly the same. The power loss of the high-pass LCR type filter is much less than that of the high-pass RC filter. However, the inductance value of 1 mH has a large size and increases the total cost of the designed SRF. As a result, this topology is not preferred as SRF for the hysteresis current regulators.

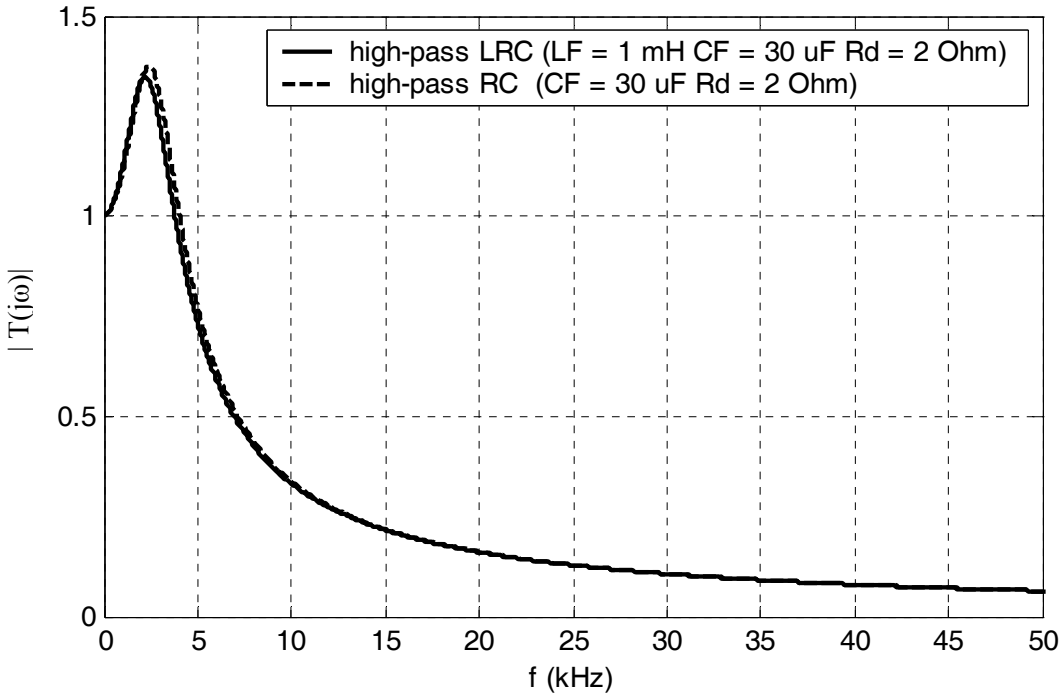

Figure 4.18 The T(s) magnitude of the high-pass LCR and RC type filters for the same C_F and R_d values.

4.2.5 High-pass RCC type SRF

As the value of damping resistor R_d at the high-pass RC type filter structure increases, the filtering of the high frequency switching ripple currents degrades. The high-pass RCC type filter illustrated in Figure 4.1.e provides sufficient filtering of switching ripple currents due to parallel connected small size capacitor C compared to C_F size in its structure. The transfer function T(s) defined as the proportion of the line current I_{HS} to the harmonic current source I_H for high-pass RCC type SRF is given as follows.

$$\mathrm{T}(s) = \frac{I_{HS}(\mathrm{s})}{I_H(\mathrm{s})} = \frac{\mathrm{s}C_F R_d + 1}{\mathrm{s}^3 L_S C_F C R_d + \mathrm{s}^2 L_S (C_F + C) + \mathrm{s}C_F R_d + 1} \tag{4.19}$$

The effect of C in the high-pass RCC type filter to filtering characteristics can be observed by utilizing the designed values of C_F = 30 μF and R_d= 2 Ω for the high-pass RC type SRF. Figure 4.19 illustrates T(s) magnitude of the high-pass RCC type filter for various C values, C_F = 30 μF and R_d = 2 Ω. The filtering capacity of the topology increases for high frequency switching ripple currents as the C value increases. However, as the C value increases, the parallel resonance peaks increase compared to the case where the capacitor C is excluded from the topology (marked on the figure as C = 0). If the C value decreases, filter capability of the topology is poor for high frequencies. Although, there exists an increase in the parallel resonance peak for C = 5 μF, the filtering of high frequency switching ripple currents is slightly enhanced. Therefore, the inclusion of C to the high-pass RC type SRF structure slightly increases performance while it increases filter size and cost. As a result it is not preferred as SRF in the PAF applications.

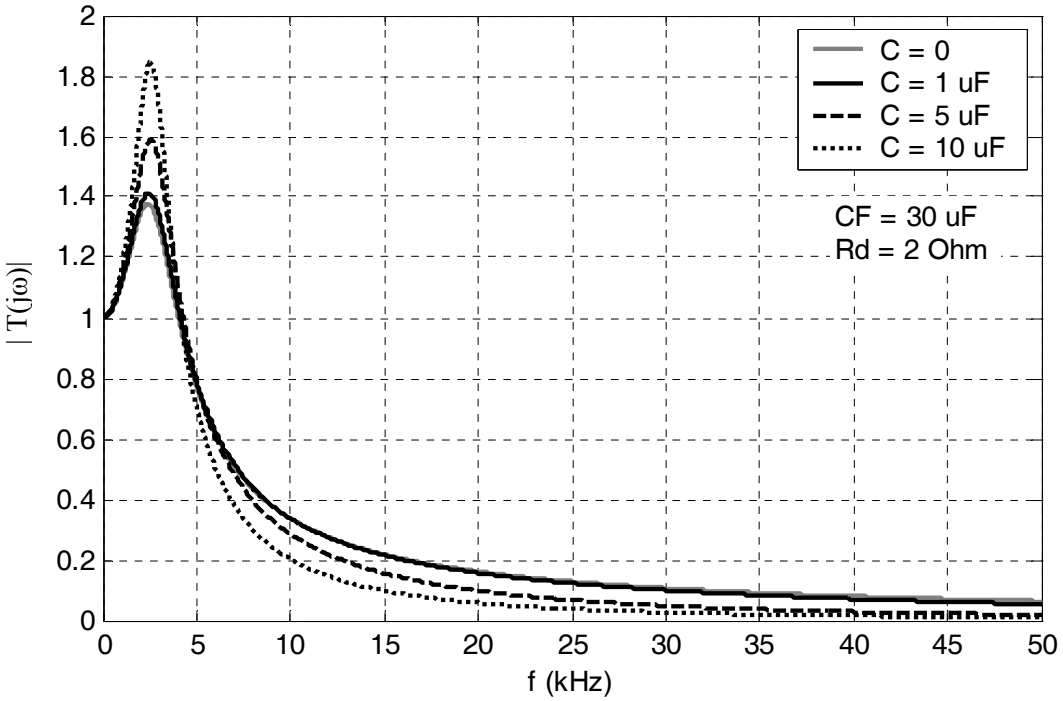

Figure 4.19 The T(s) magnitude of the high-pass RCC type SRF for various *C* values.

4.3 SRF Performance Comparisons and Summary

Among the investigated SRF topologies, the tuned LCR, broad-band tuned and high-pass LCR type filters for the linear current regulators are designed and their performances are analyzed via the defined transfer function T(s). T(s) magnitudes and $Z_F(s)$ impedances of the designed filter topologies for linear current regulators are illustrated in Figure 4.20 and Figure 4.21 respectively for comparison purposes. The two topologies preferred for the linear current regulators are the tuned LCR and the broad-band tuned type SRF. As Figure 4.20 and Figure 4.21 illustrate, performances of the two topologies are nearly same in filtering of the switching ripple currents at f_{SW}. The broad-band tuned type SRF is superior compared to tuned LCR type SRF since it has broad-band damping capability. However, the topology is not preferred in industrial applications due its large size, cost, and power loss compared to tuned LCR type SRF. When the high-pass LCR type filter is utilized for the linear current regulators, its characteristics resemble the tuned filter

characteristics. Its performance in filtering the switching ripple currents at f_{SW} increases for larger values of damping resistor R_d. However, the damping resistor in its structure increases the size, cost, and power loss of the filter compared to the tuned LCR type SRF.

The high-pass RC, high pass RCC, and high-pass LCR type filters for the hysteresis current regulators are designed and their performances are analyzed via the defined transfer function T(s). The T(s) magnitudes and $Z_F(s)$ impedances of the designed filter topologies for hysteresis current regulators are illustrated in Figure 4.22 and Figure 4.23 respectively for comparison purposes. The high-pass RC type SRF is generally preferred for the hysteresis current regulators due to its simple and small structure, and low cost. Although, power loss at fundamental frequency is eliminated with the inductor connected in parallel with the damping resistor in the designed high-pass LCR type SRF, the large size of the inductor increases the size and cost of the SRF. Therefore the high-pass LCR type SRF is not preferred in industrial applications. Although, the performance of high-pass RC type SRF is enhanced with the parallel connected small size capacitor in high-pass RCC type SRF, the topology is not preferred due to an additional capacitor in its structure and increased possibility of the parallel resonance risk.

In this chapter, the switching ripple topologies utilized in the PAF application are investigated and SRFs are designed for the PAF system utilizing different types of current regulators. Moreover, the tuned LCR type SRF preferred for linear current regulators and high-pass RC type SRF preferred for hysteresis current regulators are analyzed in detail. The effects of the filter parameters on the filtering characteristics are analyzed and illustrated via the transfer function T(s) derived from the equivalent circuit model of the load, PAF, SRF, and the AC utility grid system. Further, a comparison study is held for all the topologies. In the following chapters, the performances of the designed SRFs will be investigated and their switching ripple current attenuation effectiveness will be verified by means of computer simulations and experimental studies.

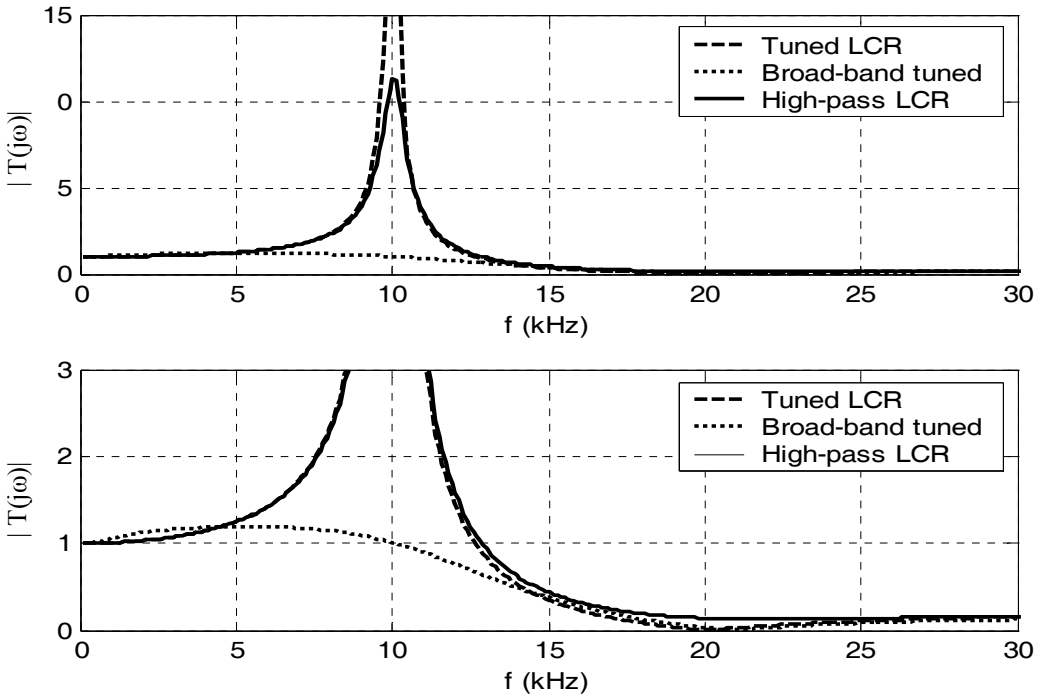

Figure 4.20 The T(s) magnitudes of the designed tuned LCR, broad-band tuned and high-pass LCR type SRFs for linear current regulators.

Top: full view, bottom: zoom in view of the switching ripple frequency range.

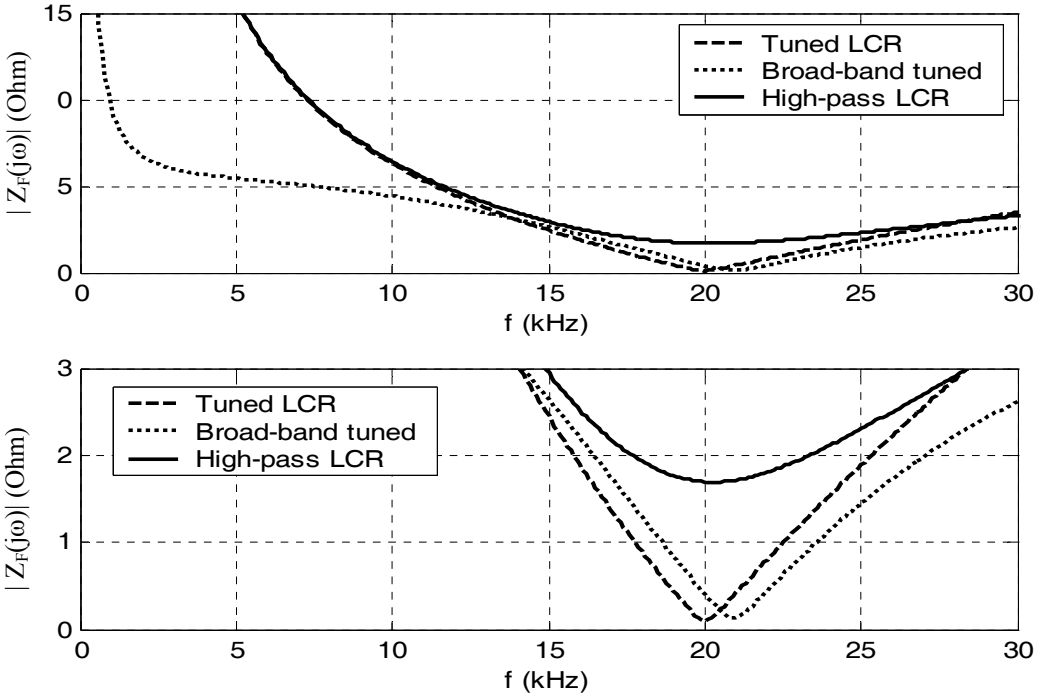

Figure 4.21 The $Z_F(s)$ magnitudes of the designed tuned LCR, broad-band tuned and high-pass LCR type SRFs for linear current regulators.

Top: full view, bottom: zoom in view of the switching ripple frequency range.

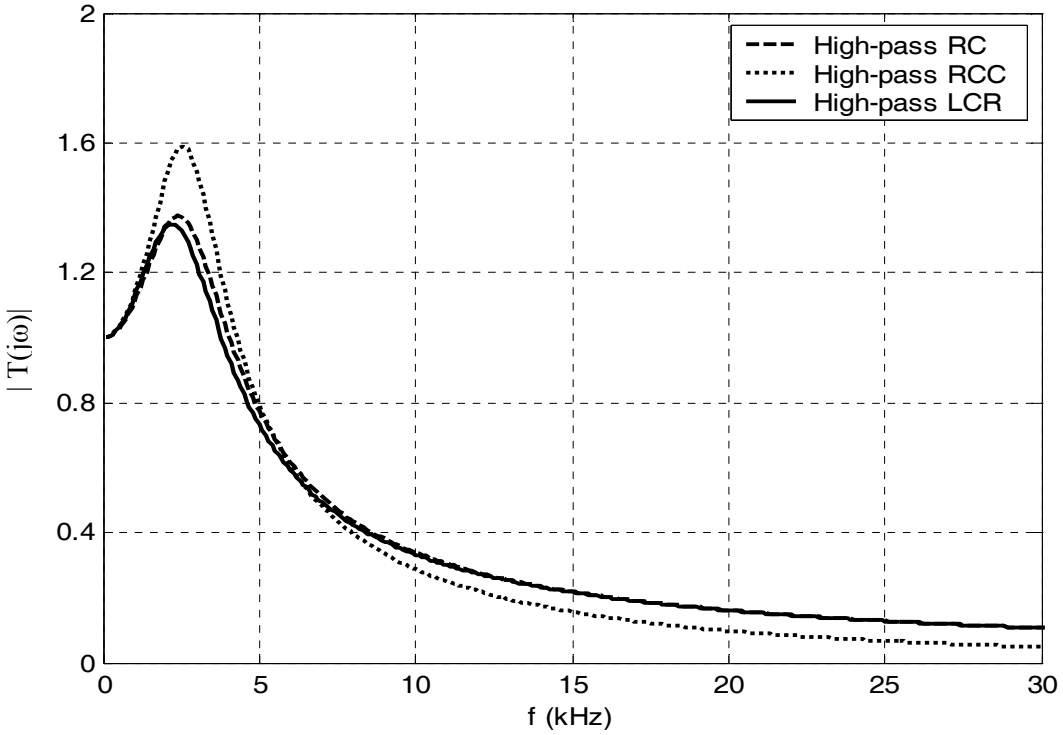

Figure 4.22 T(s) magnitudes of the designed high-pass RC, high-pass RCC, and high-pass LCR type SRFs for hysteresis current regulators.

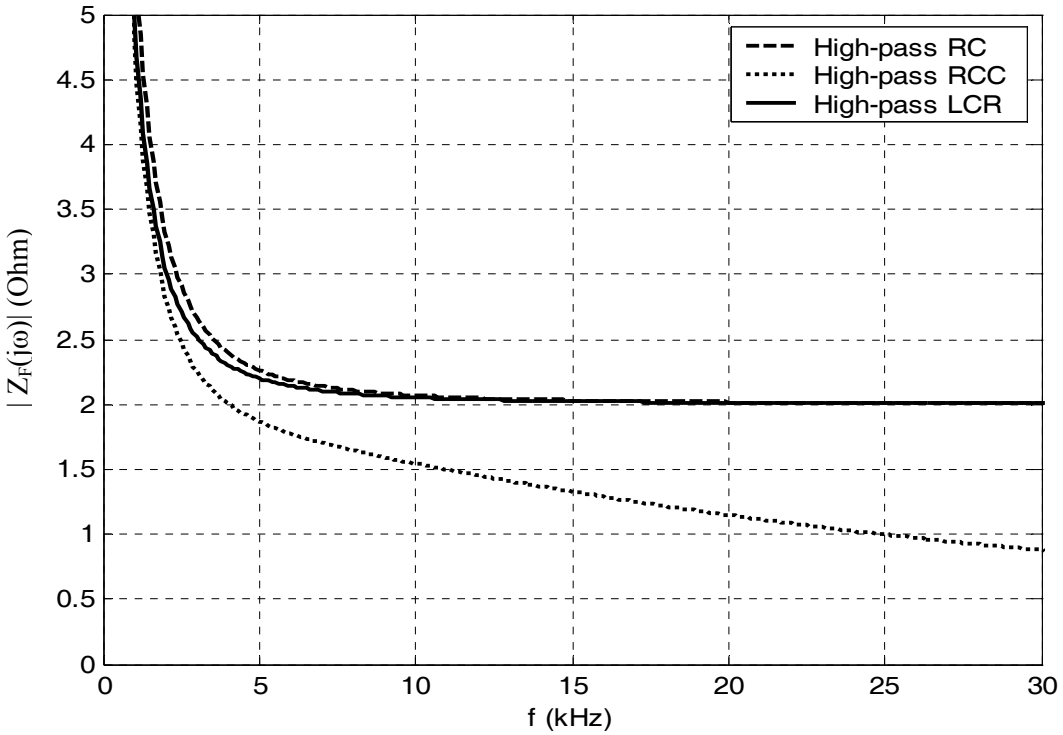

Figure 4.23 $Z_F(s)$ magnitudes of the designed high-pass RC, high-pass RCC, and high-pass LCR type SRFs for hysteresis current regulators.

CHAPTER 5

THE PARALLEL ACTIVE FILTER PERFORMANCE ANALYSIS BY MEANS OF COMPUTER SIMULATIONS

5.1 Introduction

In this chapter, the PAF performance is investigated by means of detailed computer simulations. First, the PAF computer simulation model is constructed. The nonlinear load connected to the AC utility grid for the PAF application is modeled. The performance criteria and system parameters of the PAF system are given. Once the whole system is modeled in the computer simulation environment, the basic steady-state performance of the PAF without SRF for the linear proportional gain current regulator is analyzed. Then the performances of the other current regulators analyzed in Chapter 3 are investigated and a comparison study is carried out. The current regulator performances in the PAF application are conducted without SRFs since the SRF type depends on the current regulator type utilized. The performance comparisons determine the high performance current regulators. Then the performances of the designed SRF in Chapter 4 are investigated and their circuit parameter determination procedure is completed. Further, the detailed steady-state and dynamic performance of the PAF system (with appropriate SRFs) for the selected high performance current regulators are investigated. Finally, reactive power and negative sequence current compensation capability of the designed PAF system is analyzed for a thyristor rectifier.

5.2 Parallel Active Filter Computer Simulation Model

For the purpose of modeling the system, a computer simulation package program, Ansoft-Simplorer V7.0 has been utilized [41]. Ansoft-Simplorer is a graphic window based power electronics circuit simulator, in which the power electronics system is formed by picking and placing the required components on its graphic window. The program involves a circuit schematic diagram, a graphic view window, and the Day-postprocessor window. In the schematic window, the circuit is drawn via pick and place, the control blocks are created, and simulation parameters and circuit component values are assigned. The graphic window has the properties of an oscilloscope which displays the simulation results (voltage and current waveforms, etc.). In the Day-postprocessor window, the waveforms obtained from the simulation results are evaluated by utilizing the analysis tools such as the power analyzer, harmonic analyzer, THD calculator, etc.

In the computer simulation, the trapezoidal integration method is utilized for the solution of the differential equation system. The maximum and minimum step sizes are selected to minimize the computational errors and obtain high accuracy in the simulations without excessive data storage and computational burden. Since the maximum switching frequency (f_{max}) is determined as 20 kHz, which corresponds a switching period of 50 μs, the minimum integration size selected as 500 ns (1/100 of 50 μs) provides sufficient accuracy for the computer simulation of the system.

It is critical to model the AC utility grid and the nonlinear load in order to evaluate the PAF performance since the PAF is designed to compensate the harmonic currents, reactive power current component and the negative sequence current component of the nonlinear load which is supplied from the AC utility grid. The characteristics, ratings and parameters of the AC utility grid system and nonlinear load primarily determine the performance criteria, ratings, and system parameters of the designed PAF system. For this reason, analysis of the nonlinear load connected to AC utility grid will be performed as a first step of computer simulation model part. Then the PAF model for computer simulation will be created so that the whole system (the AC

utility grid, harmonic current source type nonlinear load, and parallel active filter) is modelled for detailed computer simulation studies.

5.2.1 The AC Utility Grid and Non-linear Load Computer Simulation Models for The PAF Application.

The performance of a PAF is determined based on the AC utility grid and nonlinear load system parameters. Since the designed PAF should meet the IEEE 519 harmonic recommendations, the knowledge of the value of the load current fundamental component, the THD of the load current (I_{L1}), and the short circuit current of the AC utility grid at the PCC (I_{SC}) is critical to determine the parameters and performance limits of the PAF connected parallel to the nonlinear load at the PCC.

Since the laboratory experiments will be held at the METU Electrical Machinery and Power Electronics Laboratory, the AC utility grid information utilized in the computer simulations is chosen as the parameters of distribution system of the METU campus. At the METU campus, the electric power is provided via a distribution transformer of 500 kVA with a secondary supply voltage (V_S) of 380 V and the frequency (f_e) of 50 Hz respectively. The distribution system line inductance (L_S) and resistance (R_S) are 100 μH and 50 mΩ respectively. The nonlinear load is chosen as a 3-phase diode-rectifier with a rated output power (P_{load}) of 10 kW. This type of load generally constitutes the front-end circuit of ASDs and UPSs in industrial applications. The single line circuit diagram of the AC utility grid and 3-phase diode rectifier load used as the application circuit of the PAF in the computer simulations is shown in Figure 5.1. Note that the 3-phase diode rectifier is harmonic current source type nonlinear load with an AC side inductor (line reactor) and DC side inductor although it has a DC bus capacitor as discussed in Chapter 2. The full-bridge 3-phase diode rectifier is connected to the AC utility grid at the PCC with an AC line reactor (L_{ac}) of 1.43 mH (%3.4). The full-bridge diode rectifier is modelled with “system level devices”. In the system level model, the switch model involves a simple switch with a pair of series and parallel resistors. Thus, the semiconductor device switching dynamics are not modeled. The DC link of diode rectifier is

constituted with a DC link inductor (L_{dc}) of 1.46 mH (%3.4), a pre-charge resistor (R_{pre}) of 20 Ω, and a DC link capacitor of 1 mF. The inverter side of ASD and UPS systems is modeled with an equivalent resistor (R_{load}) of 25 Ω such that the output power of the diode rectifier is 10 kW at the DC link voltage of 500 V. Since the DC link capacitor of the diode rectifier decouples the PWM dynamics of the inverter from the rectifier side, this approximation is highly acceptable and does not result in loss of accuracy. The diode rectifier load parameters are determined based on the data of the recent industrial products and the availability of circuit components in laboratory environment. The AC line and load parameters are summarized in Table 5.1.

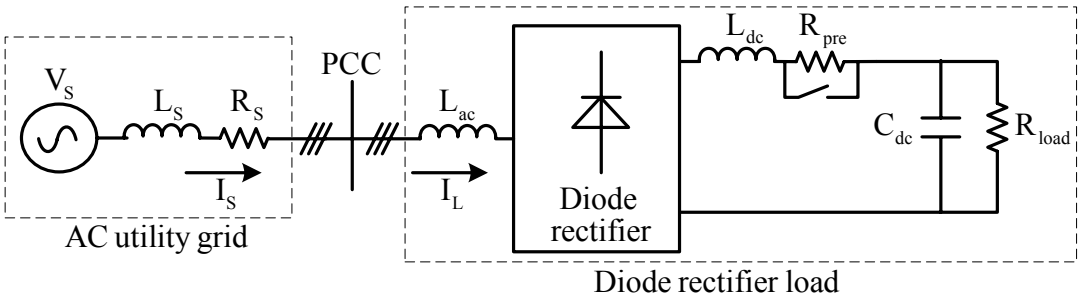

Figure 5.1 Single line diagram of the rectifier and AC line.

Table 5.1 The AC utility grid and load parameters used in the computer simulation

	Parameter	Value
AC utility grid	V_S (Line voltage)	380 V
	f_e (Line frequency)	50 Hz
	L_S (Line inductance)	100 µH
	R_S (Line resistance)	50 mΩ
Diode rectifier load	L_{ac} (AC line reactor)	1.43 mH
	L_{dc} (DC Link inductor)	1.46 mH
	R_{pre} (Precharge resistor)	20 Ω
	C_{dc} (DC link capacitor)	1 mF
	R_{load} (Load resistor)	25 Ω
	P_{load} (Load output power)	10 kW

Given the AC utility grid parameters, its short-circuit current I_{SC} can be calculated in the following.

$$I_{SC} = \frac{V_S}{\sqrt{3}\left(2\pi f_e L_S + R_S\right)} \tag{5.1}$$

From Equation (5.1), I_{SC} is found as 2703 A. In order to find the rated fundamental load current I_{L1}, computer simulations are conducted. Figure 5.2 illustrates the voltage at the PCC (V_L), the diode rectifier load current (I_L) and harmonic spectrum of I_L for 'phase *a*' of the 3-phase system. Computer simulations result in I_{L1} value as 15.6 A, which results in an I_{SC}/I_{L1} value of 173. The THD_I and harmonic current limits for the I_{SC}/I_{L1} value of 173 are found based the IEEE 519 harmonic current limits given in Table 1.1. The THD_V limit at the PCC is found for the AC utility grid voltage of 380 V based on the IEEE 519 voltage distortion limits in Table 1.2. These limits will constitute the performance limits of the PAF performing harmonic current and reactive power compensation of the diode rectifier load with the parameters given above. Table 5.2 gives the harmonics components and THD_I of the load current and THD_V and PF at PCC for the simulated system and IEEE 519 limits up to the 50^{th} harmonic order obtained from Table 1.1 for I_{SC}/I_{L1} value of 173 and Table 1.2 for 380 V. From Table 5.2, the THD_I value of the load current is 32.6%, which is above the limit of 15%. Moreover, the 5^{th}, 7^{th} and 11^{th} harmonic current components of the load current are above the limits given in Table 5.2. Although the THD_V value at the PCC is 0.49%, which is below the limit of %5, the THD_V will increase when the PAF is implemented for harmonic current and reactive power compensation of load due to the inverter switching harmonics. Therefore the final value of THD_V should be kept below the limit of 5%. There is no limit in the IEEE 519 recommendations for PF at the PCC. However, the value will be kept between 0.95 lagging and 0.98 leading due to the restrictions of EMRA for PF at the PCC as mentioned in Chapter 1.

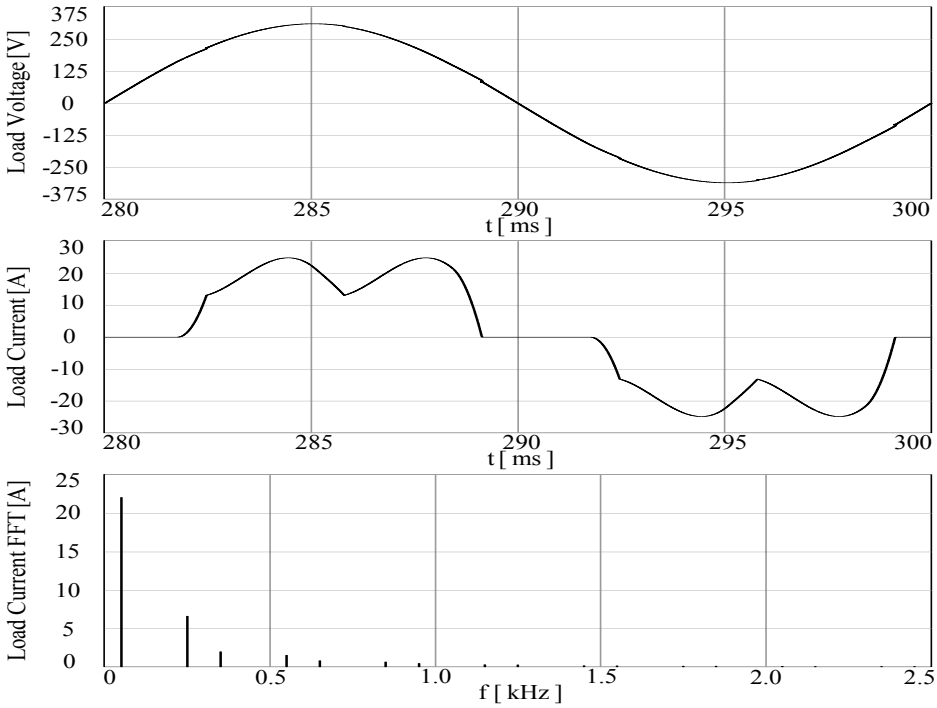

Figure 5.2 Diode rectifier load computer simulation waveforms top to bottom: Load voltage at the PCC, load current and its harmonic spectrum (FFT) for one phase.

Table 5.2 Load current harmonics, THD_I, THD_V, PF at the PCC, and the IEEE 519 limits

	Load current harmonics (%)	IEEE 519 limits for I_{SC}/I_{L1}=173 (%)
I_1	100.0	100.0
I_5	30.0	12.0
I_7	9.0	12.0
I_{11}	7.0	5.5
I_{13}	3.7	5.5
I_{17}	3.0	5.0
I_{19}	2.2	5.0
I_{23}	1.4	2.0
I_{25}	1.3	2.0
I_{29}	0.8	2.0
I_{31}	0.7	2.0
I_{35}	0.5	1.0
I_{37}	0.5	1.0
I_{41}	0.4	1.0
I_{43}	0.4	1.0
I_{47}	0.3	1.0
I_{49}	0.3	1.0
THD_I (%)	32.6	15.0
THD_V (%)	0.5	5.0
PF	0.930	---

5.2.2 Parallel Active Filter Computer Simulation Model

The topology utilized in the parallel active filter in this thesis is a VSI connected to the PCC via a 3-phase filter inductor as discussed in the previous chapters. The single-line circuit diagram of the PAF connected to the PCC is illustrated in Figure 5.3. The parallel active filter model utilizes pre-charge resistors (R_{Fpre}) of 11.8 Ω/phase to limit the charging current of the DC bus capacitor through the antiparallel diodes during start-up. The filter inductor (L_F) value should have a low percentage in order to have a high bandwidth for the PAF and is typically less than 5% as discussed in Chapter 3. In this thesis, it is selected as 2 mH (%1.7). The filter resistor (R_F) is not an external resistor, but the internal resistance of L_F (representing the winding and core losses of the inductor) with value of 250 mΩ, which is also included in computer simulations. The inverter switches of the PAF are modeled with IGBTs with anti-parallel diodes. The switches for inverter are "system level devices." Thus they are assumed ideal (with the exception of their conduction losses). The DC bus capacitor of the PAF (C_{DC}) is chosen as 2.35 μF considering the DC bus voltage ripple, the current at the DC side of the inverter and ratings/parameters of the products available in the market. Table 5.3 summarizes the parameters of the PAF utilized in the computer simulations. The circuit parameters of the SRFs connected to the output terminals of the PAF will be provided in the related section of this chapter.

The whole system simulation model circuit diagram including the modeled AC utility grid, diode rectifier load, and PAF is given in Figure 5.4. The 3-phase 3-wire PAF is connected to the PCC for the harmonic current and reactive power compensation of a diode rectifier load fed from 3-phase AC utility grid.

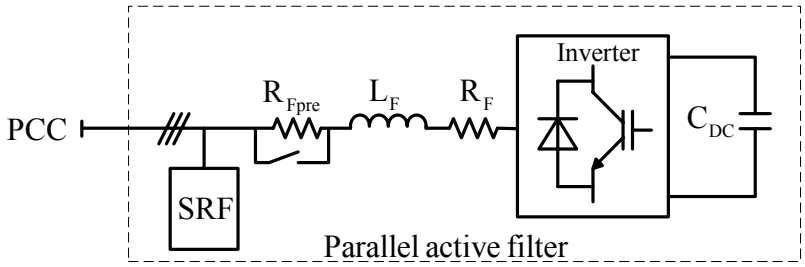

Figure 5.3 Single-line diagram of the PAF utilized in the computer simulation.

Table 5.3 The PAF parameters utilized in the computer simulation

	Parameter	Value
Parallel active filter	R_{Fpre} (Pre-charge resistor)	11.8 Ω
	L_F (Filter inductor)	2 mH
	R_F (Filter resistor)	250 mΩ
	C_{DC} (DC bus capacitor)	2.35 mF

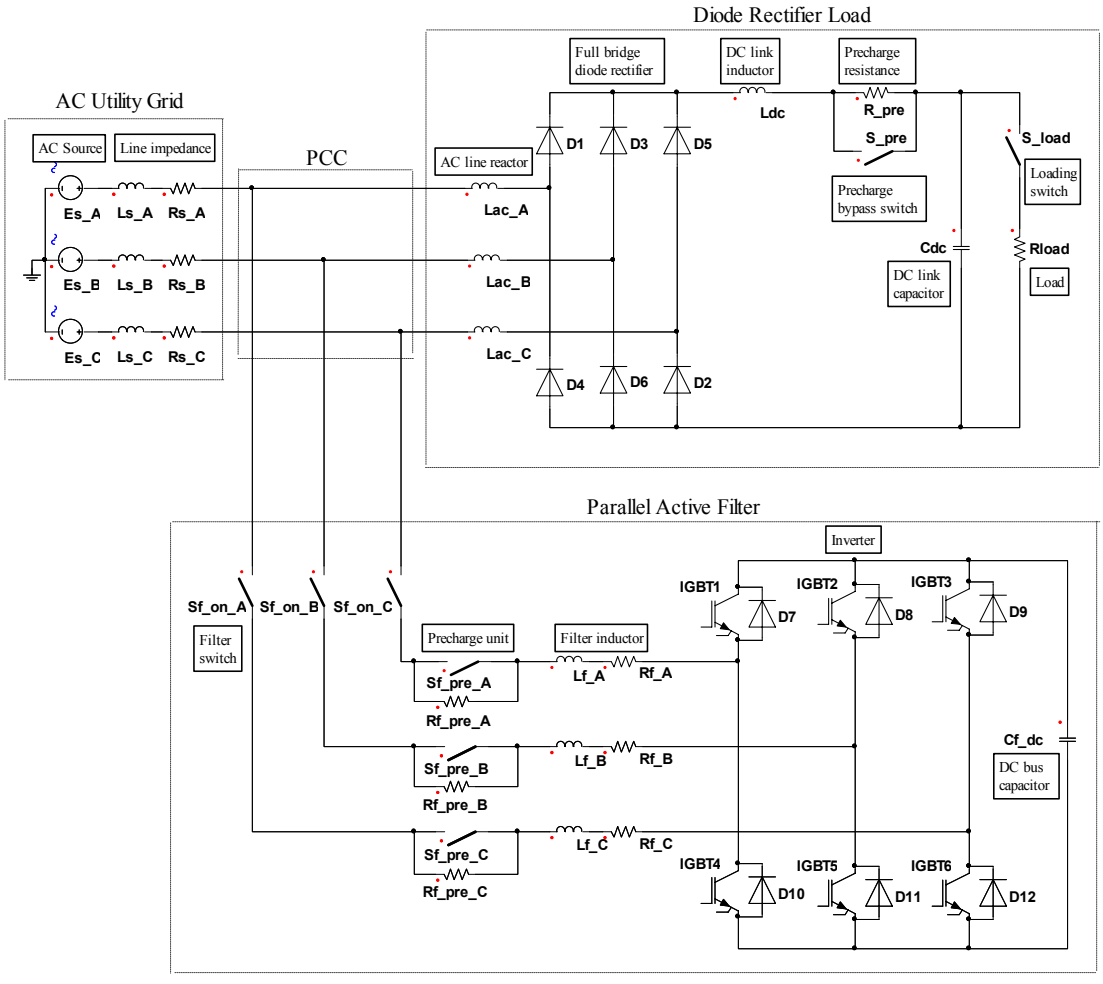

Figure 5.4 Simplorer simulation diagram of the PAF system (Simplorer V7.0 Schematic file).

5.3 Illustration of The PAF Basic Performance Utilizing The LPCR

In this section, the basic performance analysis and simulation waveforms of the PAF system utilizing the LPCR are presented. First the performance of the basic blocks of the PAF control algorithm is illustrated and then the performance of the whole system is presented. Moreover, the THD_I performance of the current regulator for different proportional gain (K_P) values is presented and limitations are discussed. The THD_I, THD_V, PF at PCC, and f_{AVG} performance of the current regulator is presented. The line current harmonics after the PAF is connected to the PCC is compared to the IEEE 519 harmonic limits up to the 50^{th} harmonic.

The PAF control algorithm consists of two main control blocks; the current reference generator and the current controller as discussed in Chapter 2. The implemented harmonic current reference generator of the current reference generator block utilizes the synchronous reference frame controller (SRFC) for the extraction of the load current harmonics, reactive power component and the negative sequence component. The SRFC utilizes the AC utility grid phase angle information for the transformation, which is obtained via a phase locked loop (PLL) circuit. The cut-off frequency of the vector PLL is chosen as 100 Hz with the proportional gain of '2' and the integral gain of '40' based on [25]. Figure 5.5 illustrates the line voltage for phase '*a*' and the obtained phase angle information ($\theta_e=\omega_e t$) and the unit vectors of $\sin(\omega_e t)$ and $\cos(\omega_e t)$ from the designed PLL at steady-state over two fundamental cycles. As the figure illustrates the PLL gives the phase angle information accurately such that the obtained θ_e has ramp waveform characteristics and the unit vector '$\sin(\omega_e)$' is locked to the line voltage with zero phase error. The SRFC utilizing the phase angle information from the PLL for the harmonic current extraction utilizes two first order cascade connected low-pass filters with the cut-off frequencies of 20 Hz. The filter is designed such that it has a gain of 0.03 at 100 Hz. This means that the designed filter will attenuate 97% of the negative sequence component of the load current. The output of the harmonic current reference generator for phase '*a*', which is the current reference for the PAF, is illustrated in Figure 5.6. Moreover, the line voltage, load current and line current, which is obtained by adding the reference current to the load

current mathematically via a summation block in Simplorer simulation software, is also included in figure. When the obtained reference current waveform is added to the load current, the line current is sinusoidal and in phase with the line voltage. This illustrates that the SRFC extracts the harmonics and the reactive power component of the load current. Since the diode rectifier is operated under balanced conditions, no negative sequence current component is observed. This case will be illustrated at the end of this chapter for a thyristor rectifier, where an unbalanced operation condition is created.

For the current regulator part of the PAF, LPCR is utilized. The performance of other current regulators will be illustrated in the next section. Based on the discussions in Chapter 3, the value of K_P can be increased according to the desired bandwidth theoretically and it is shown that the phase margin of the delayless system is 90°. However, if the PAF system is modeled including the implementation delays, the phase margin degradation becomes unavoidable. The determination of the K_P value based on the desired phase margin of 45° has been carried out for the PAF system with the L_F value of 2 mH, R_F value of 250 mΩ and the K_P value is determined as 40. In the computer simulation, the delays of the system are modelled and a further study is carried out for the final value of the K_P. Since, the value of THD_I is the most critical performance evaluation parameter in the PAF application, THD_I versus K_P graph is obtained for various values of K_P in the computer simulation environment. Figure 5.7 illustrates the THD_I performance of the PAF system utilizing LPCR for different values of K_P. The lower values of K_P result in lower bandwidth and high THD_I value. The higher values of K_P result in oscillations due to the excessive phase margin degradation. Therefore, the THD_I value increases rapidly for the values of K_P greater than 70. The figure illustrates that the acceptable range for K_P value is between 30 and 70. Although the computer simulation illustrates that system has the lowest THD_I value for K_P value of 60, as will be shown in the next chapter, the experimental studies limit the K_P value to 40 for a more stable system. Moreover, the resolution in discrete time application and inverter saturation problems limit the value of K_P in practice. Further, Figure 5.7 illustrates a marginal THD_I value difference (nearly 1%) between the K_P value of 40 and the K_P value of 60. Therefore,

the K_P design value of 40 for a phase margin 45° is consistent with the computer simulation results and is utilized as the K_P gain of the LPCR in the computer simulation. As a PWM modulator, scalar DPWM1 is utilized with a carrier frequency of 20 kHz for the PAF system operating in high modulation range due to its low switching losses, low current ripple, and simple implementation. At the distribution systems of 380Vrms (or 400Vrms) line-to-line voltage level, the DC bus voltage of practically available PAF systems is between 650 V and 750 V to achieve enough voltage margin for current regulation. While the low values of DC bus voltage result in poor current tracking in high di/dt regions of current reference, but small current ripple, the higher values of DC bus voltage result in a better current tracking in the high di/dt regions, but large current ripple in magnitude. In this work, the DC bus voltage of PAF system is selected as 700 V.

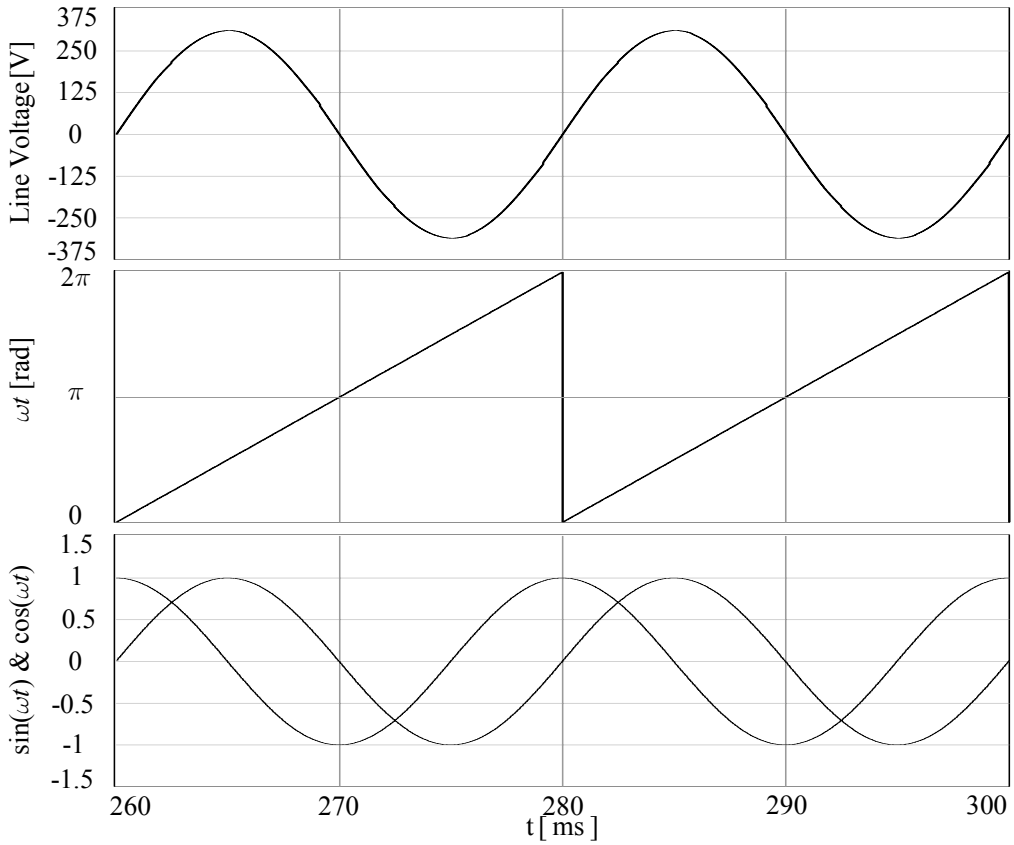

Figure 5.5 The performance of the PLL at steady-state.

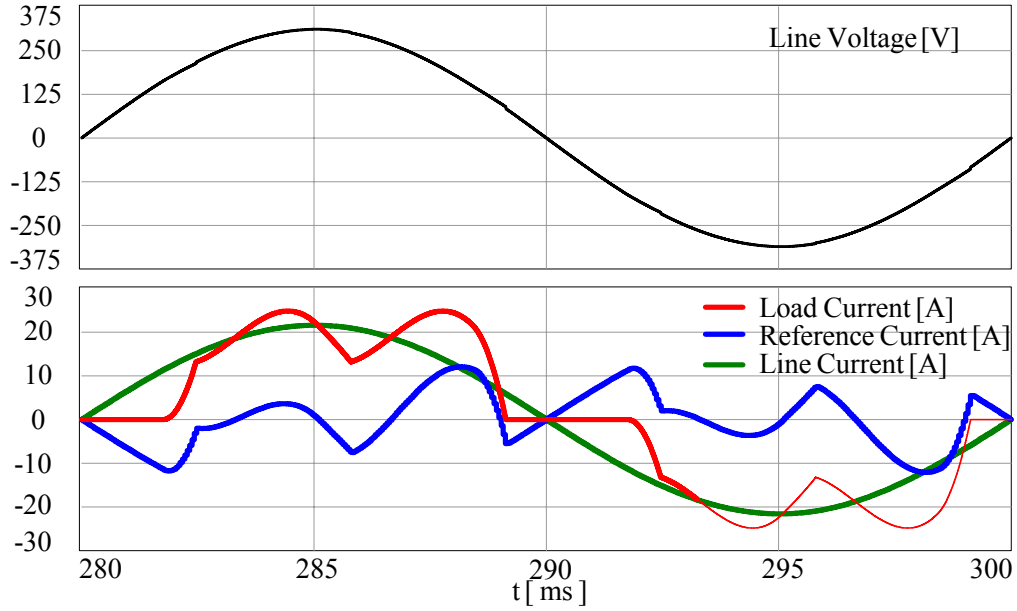

Figure 5.6 The steady-state harmonic current extraction performance of the SRFC.

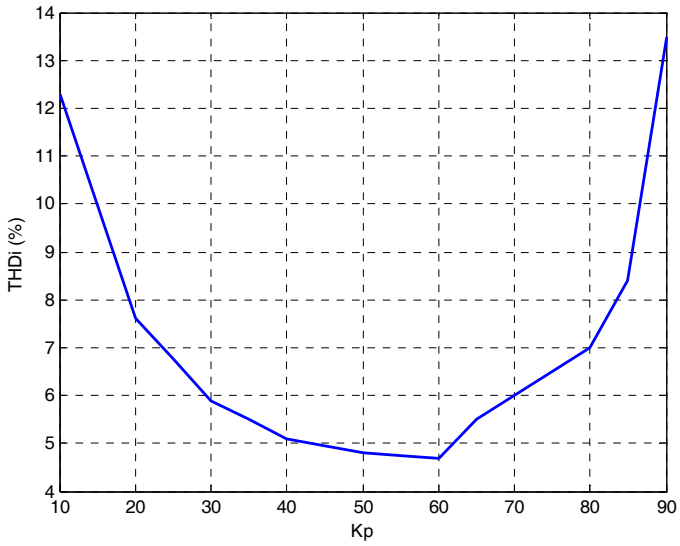

Figure 5.7 THD_I performance of the LPCR for different K_P values.

Figure 5.8 illustrates the voltage at the PCC, the line current, the load current, the PAF current reference, and the PAF current waveforms for 'phase *a*', and the DC bus voltage waveform of the PAF system that compensates the harmonics and reactive current component of the diode rectifier load with the output power rating of 10 kW. Moreover, the steady state performance of the PAF for LPCR is summarized in Table 5.4. Table 5.4 includes the load current harmonics, line current harmonics, and IEEE 519 harmonic limits up to 50^{th} harmonic current component. Moreover, it includes THD_I, THD_V, PF at PCC, and f_{AVG} for LPCR. It can be seen from the table that all the current harmonics are well below the IEEE 519 limits and the load current harmonics are suppressed up to the 41^{st} harmonic. In fact, this illustrates the current regulator bandwidth of LPCR, which is around 2.0 kHz. The line current waveform in Figure 5.8 is nearly sinusoidal with the THD_I value of 5.1%, which illustrates that the PAF system performs the harmonic current compensation of the harmonics current source type nonlinear load. Moreover, the line current waveform is in phase with line voltage in Figure 5.8 that results in a PF value of 0.998. This illustrates that the reactive current compensation of diode rectifier load is performed by the PAF system. The THD_V value at the PCC is 3.8%. The reason that THD_V is slightly high although a pure sinusoidal AC utility voltage is utilized in the computer simulations is that there exist switching ripple voltages on the voltage waveform. Since the SRF is not included in this part, the switching ripple currents are not diverted through the SRF. As a result, the line current includes switching ripple currents on it, which result in high frequency voltage distortion on the voltage waveform. The effect of the SRF on the voltage and current waveforms will be analyzed in a later part of this chapter. Since DPWM1 is utilized as PWM modulator, the average switching frequency of the inverter for LPCR is 13.3 kHz for the selected carrier frequency of 20 kHz. In Figure 5.8, the DC average bus voltage of the PAF is kept at its reference voltage value of 700 V. This illustrates that the DC bus voltage regulation of the PAF is performed satisfactorily. The 300 Hz ripple on the DC bus voltage waveform results from the dominant 5^{th} and 7^{th} harmonics current components existing in the filter current. Figure 5.8 and Table 5.4 clearly illustrate that PAF system utilizing LPCR satisfactorily performs compensation of the load current harmonics and reactive current component of the load current, DC bus regulation of the PAF system.

Although Figure 5.8 and Table 5.4 illustrate the basic performance of the PAF system, another important point involves the performance of the utilized current regulator in PAF system. Although the THD_I value of the line current is a critical evaluation criterion while analyzing the performance of a current regulator, the tracking capability of the current regulator during high di/dt regions is another important evaluation point. The computer simulation waveform of the line current in detail is illustrated in Figure 5.9 for the PAF system utilizing the LPCR. Current spikes exist on the waveforms at six times the line frequency resulting from the tracking performance degradation of the current regulator. These spikes occur during diode rectifier commutation where high di/dt occurs. Figure 5.9 also illustrates the PAF current and its reference. From the figure, the current tracking performance degradation of the regulator can be observed during the high di/dt regions. The line current harmonic spectrum in Figure 5.10 is included to provide a visualization of the switching ripple currents created by the LPCR. It is known that linear current regulators create switching ripples at the switching frequency and its multiples. The harmonic spectrum of the line current illustrates a dominant switching ripple at the switching frequency, 20 kHz as expected.

This section involved the basic performance illustration of the PAF and the LPCR performance. The next section illustrates the performance of the other current regulators analyzed in Chapter 3 and a comparison study for the performances of the current regulators will be carried out. Since the basic waveforms of PAF are similar for other current regulators, they are not included in this thesis for other current regulators. Only basic results and waveforms such as the line current, line current harmonic spectrum and filter current, which differ at the microscopic level for other current regulators, are provided in next section.

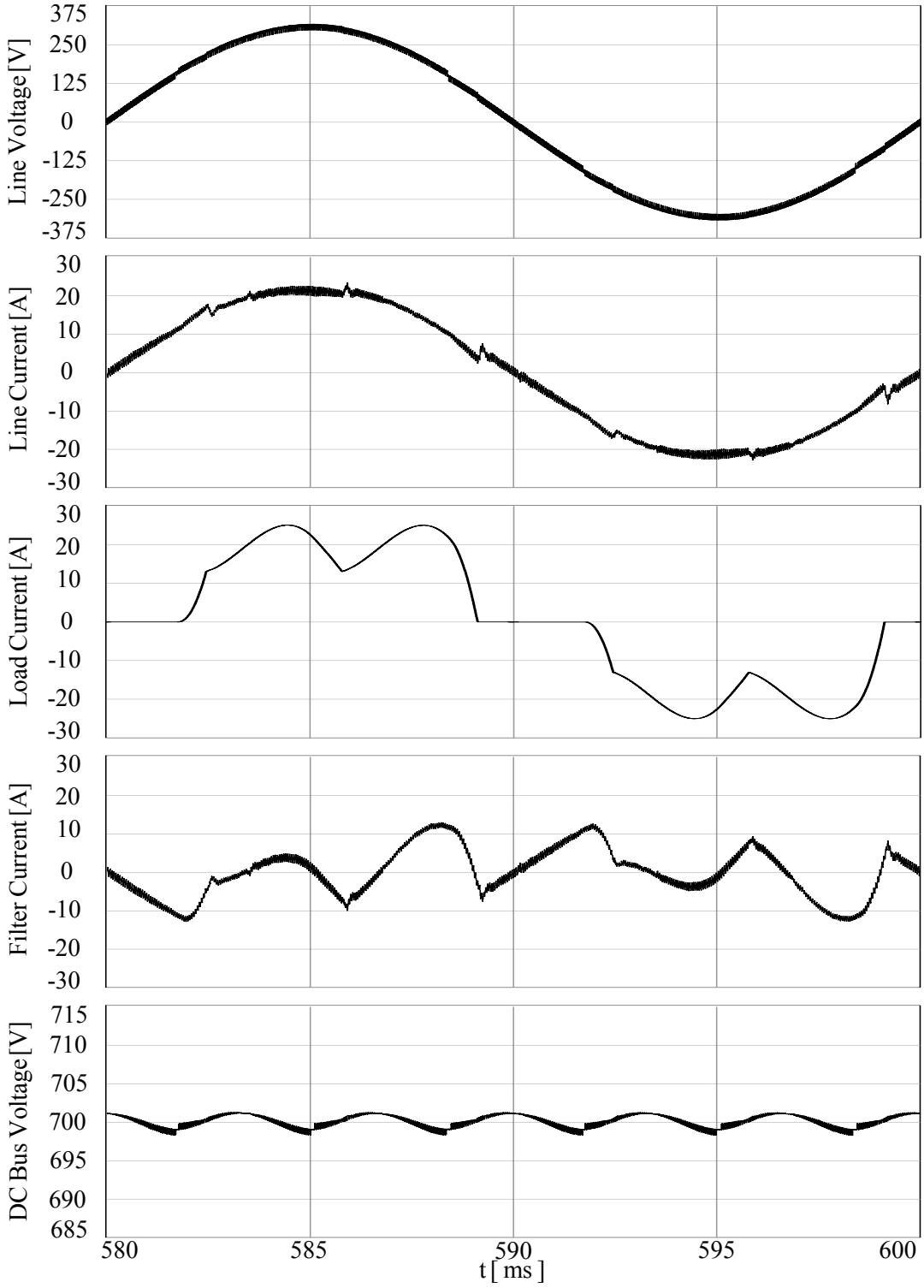

Figure 5.8 Steady-state waveforms over a fundamental cycle illustrating the basic performance of the PAF utilizing LPCR: The voltage at the PCC, line current, load current, and the PAF current for 'phase *a*', and the DC bus voltage.

Table 5.4 Line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for LPCR, and IEEE 519 limits

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%)	IEEE 519 Harmonic Current Limits for I_{SC}/I_{L1}=173 (%)
I_1	100.0	100.0	100.0
I_5	30.0	2.5	12.0
I_7	9.0	0.9	12.0
I_{11}	7.0	1.3	5.5
I_{13}	3.7	0.8	5.5
I_{17}	3.0	1.0	5.0
I_{19}	2.2	0.6	5.0
I_{23}	1.4	0.6	2.0
I_{25}	1.3	0.5	2.0
I_{29}	0.8	0.4	2.0
I_{31}	0.7	0.4	2.0
I_{35}	0.5	0.5	1.0
I_{37}	0.5	0.3	1.0
I_{41}	0.4	0.4	1.0
I_{43}	0.4	0.2	1.0
I_{47}	0.3	0.4	1.0
I_{49}	0.3	0.3	1.0
THD_I (%)	32.6	5.1	15.0
THD_V (%)	0.5	3.8	5.0
PF	0.930	0.998	---
f_{AVG} (kHz)		13.3	

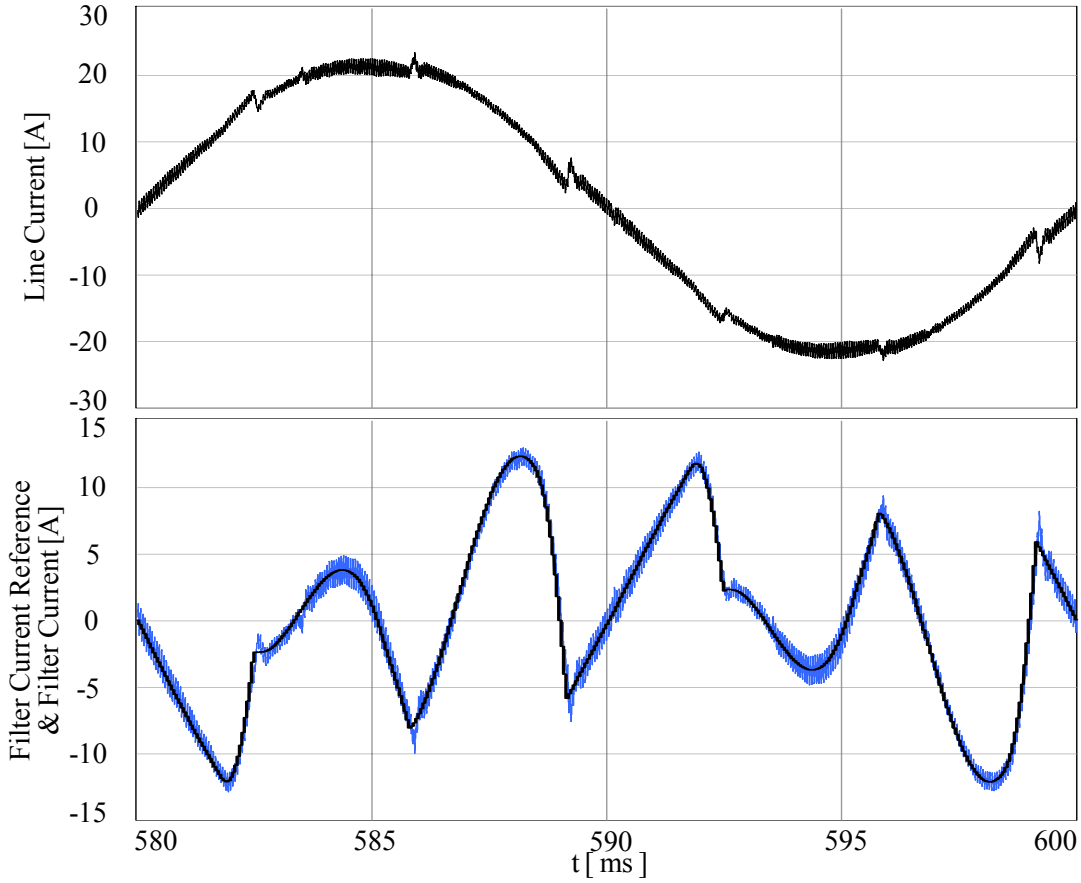

Figure 5.9 Line current, filter current reference (black) and filter current (blue) waveforms over a fundamental cycle for LPCR.

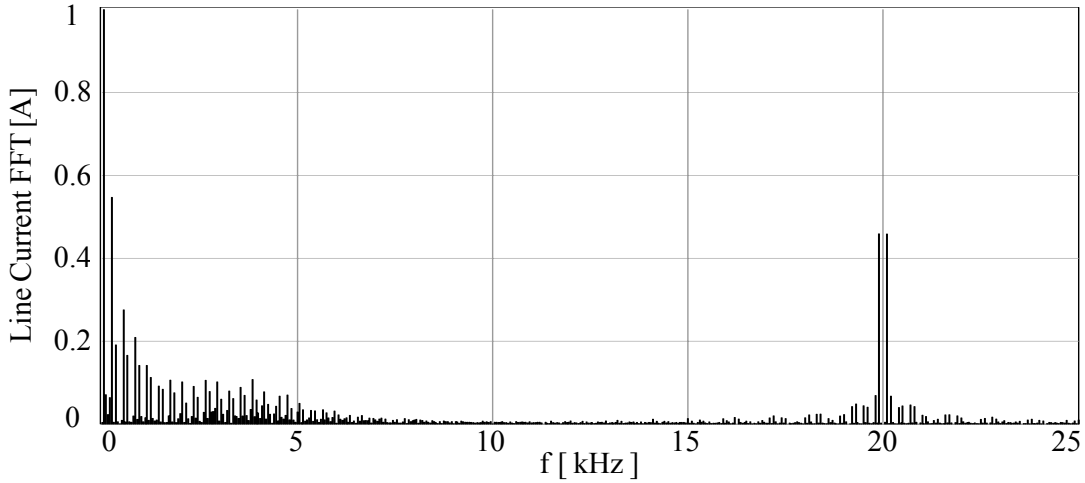

Figure 5.10 Line current harmonic spectrum for LPCR.

5.4 Performance Comparison of Various Current Regulators by Means of Computer Simulations

Of the many current regulators reported in the literature, the practically feasible current regulators for the PAF application were analyzed in detail in Chapter 3. In this section, the performance of these current regulators is analyzed by means of computer simulations. The simulation results of LPCR and RFCR of the linear regulators, and DHCR1, DHCR2, and DHCR3 of hysteresis regulators are given in this section. Although the experimental studies of the CECR are not carried out in this thesis due to the difficulty of realizing an analog charge error compensator, the performance of the CECR is simulated for comparison purposes in this chapter. Similarly, the analog hysteresis current regulator is evaluated in this thesis due to its superior current tracking performance and comparison reasons. During the performance analysis of the current regulators and their comparisons in this section, the SRF is not included in the PAF system for a fair comparison since SRF type differs for the linear current regulators and on-off current regulators as discussed in Chapter 4. The THD calculator in Ansoft-Simplorer package utilizes all the frequency components of the defined quantities while calculating THD_I and THD_V [41]. Therefore, the mentioned THD_I and THD_V values in this section include switching frequency components. As a result, a fair comparison is achieved in the current regulator performances analysis by including switching ripple currents and voltages that the current regulators create. For these reasons, simulations in this section involve the basic load and PAF main circuit but do not include an SRF in the model.

Throughout the simulations in this section, the carrier frequency is selected as 20 kHz corresponding to a maximum switching frequency of the inverter (f_{MAX}) of 20 kHz for linear current regulators. Similarly, T_S is selected as 50 μs to achieve f_{MAX} value of 20 kHz by the switching decision block discussed in Chapter 3 for the discrete time current regulators. The reason for such a high f_{MAX} selection is to keep the bandwidth of the current regulator as high as possible for better tracking of high frequency current references. Since f_{MAX} is the same for all current regulators, a fair

comparison is achieved. The DC bus voltage of the PAF system is 700 V and is kept constant for the current regulators analyzed in this section as in the LPCR case of the previous section.

5.4.1 CECR Simulation Results

In this subsection, the simulation results of charge error based current regulator (CECR) are presented. As discussed in Chapter 3, CECR includes a charge error portion in addition to the proportional gain controller. The value of the proportional gain (K_P) of CECR is $\hat{L}_F / T_S$ and the integral gain K_I is $\hat{L}_F / (T_S . T_S)$ [23]. Therefore, K_P is found as 40 and K_I is 800000 for the system with $L_F = 2$ mH and $f_S = 20$ KHz. The K_P gain of CECR is the same as in the LPCR case for a phase margin of 45°.

As mentioned at the end of the previous section, the basic results are included in this section due to the similarity of the waveforms. Table 5.5 gives the steady-state performance of the CECR by including the load current harmonics, line current harmonics and IEEE 519 harmonic limits up to the 50^{th} harmonic current component in addition to THD_I, THD_V, PF and f_{AVG}. Based on the table, all the current harmonics are well below the IEEE 519 limits and the load current harmonics are suppressed up to the 35^{th} harmonic. For higher order harmonics, the suppression is marginal as in the LPCR case. Another important point with CECR is that the low frequency harmonic compensation capability of the CECR is better than LPCR. When harmonic components up to the 49^{th} harmonic in Table 5.5 are compared to the harmonic components up to the 49^{th} harmonic in Table 5.4, the percentages of the harmonics for the CECR are lower than the ones for the LPCR for the same proportional gain. This illustrates the effect of charge error part in the minimization of the low frequency current errors. Moreover, this capability of the CECR regulator results in a lower THD_I value of %3.9 compared to the value of %5.1 in the LPCR case. The THD_V value for CECR is %3.8 and the same as in LPCR. The PF value is 0.998, which illustrates that the PAF compensates the reactive power component of the load current. As in the LPCR case, DPMW1 is utilized as PWM modulator,

which results in f_{AVG} of 13.3 kHz. Figure 5.11 illustrates the line current for CECR, which is similar to the waveform obtained for LPCR. Current spikes exist on the waveform illustrating tracking performance degradation of the current regulator. The filter current reference and filter current waveforms are also illustrated in Figure 5.11. The PAF system utilizing the CECR tracks the reference current except the high di/dt regions of current reference. This degradation explains the spikes on the source current waveform. Figure 5.12 illustrates the harmonic spectrum of the line current. The dominant switching ripple current occurs at 20 kHz as expected. When the harmonic spectrum of the line current between the fundamental frequency and 5 kHz in Figure 5.12 for the CECR is compared to Figure 5.10 for the LPCR, the harmonic components up to 5 kHz for CECR are lower than the ones for LPCR. This is another illustration of better compensation capability of CECR for low frequencies.

Table 5.5 Line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for CECR, and IEEE 519 limits

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%)	IEEE 519 Harmonic Current Limits for I_{SC}/I_{L1}=173 (%)
I_1	100.0	100.0	100.0
I_5	30.0	1.5	12.0
I_7	9.0	0.5	12.0
I_{11}	7.0	0.6	5.5
I_{13}	3.7	0.4	5.5
I_{17}	3.0	0.5	5.0
I_{19}	2.2	0.3	5.0
I_{23}	1.4	0.3	2.0
I_{25}	1.3	0.3	2.0
I_{29}	0.8	0.2	2.0
I_{31}	0.7	0.2	2.0
I_{35}	0.5	0.2	1.0
I_{37}	0.5	0.2	1.0
I_{41}	0.4	0.1	1.0
I_{43}	0.4	0.1	1.0
I_{47}	0.3	0.1	1.0
I_{49}	0.3	0.2	1.0
THD_I (%)	32.6	3.9	15.0
THD_V (%)	0.5	3.8	5.0
PF	0.930	0.998	---
f_{AVG} (kHz)		13.3	

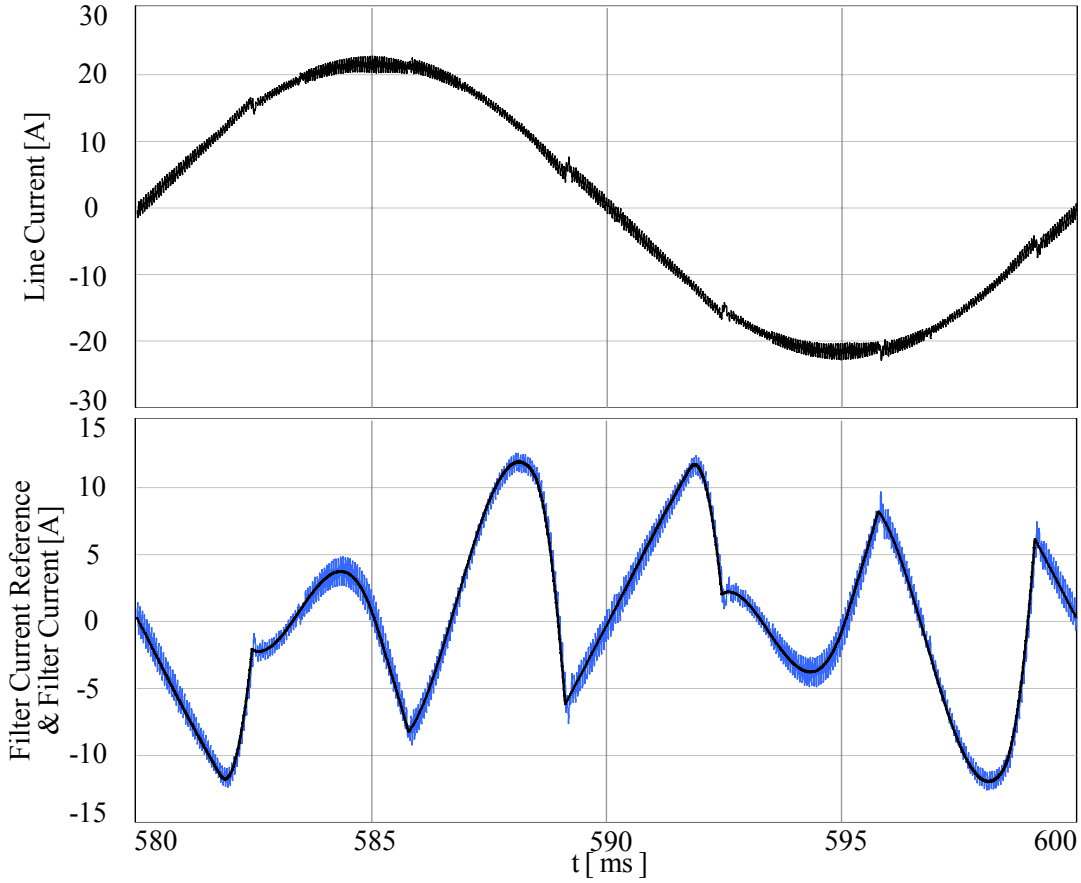

Figure 5.11 Line current, filter current reference (black) and filter current (blue) waveforms over a fundamental cycle for CECR.

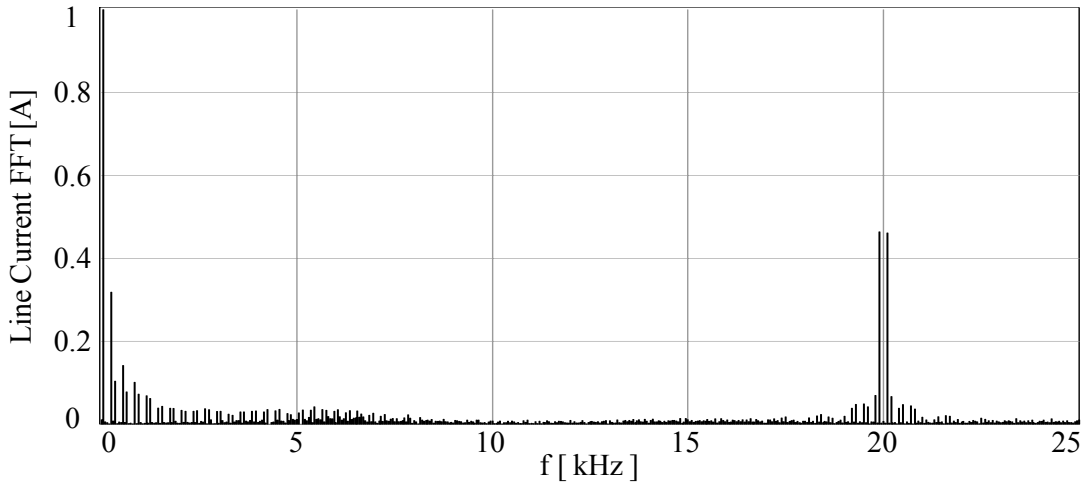

Figure 5.12 Line current harmonic spectrum for CECR.

5.4.2 RFCR Simulation Results

In this subsection, the simulation results of the resonant filter current regulator (RFCR) are presented. As analyzed in Chapter 3, each resonant filter controller compensates one harmonic pair with the harmonic order of k=6n±1 at the stationary frame. If the harmonic current pairs to be compensated are increased, different resonant filter controllers for each harmonic pair should be implemented in parallel.

When the load current and line current harmonics in Table 5.4 for LPCR and Table 5.5 for CECR are analyzed, the most dominant harmonic components are the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th}. For the RFCR in this thesis, three resonant filter controllers are implemented as parallel structures for these most dominant harmonic pairs with n=1, 2, and 3 (k=6n±1, 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th}). As a result, the number of harmonic controllers and the complexity of the current regulator will be reduced. The resonant filter controller gains for the harmonic order of k=6, which corresponds to the 5^{th} and 7^{th} harmonic components, are chosen as K_{p6}=1 and K_{i6}=125. The resonant filter controller gains for the harmonic order of k=12, which corresponds to the 11^{th} and 13^{th} harmonic components, are chosen as K_{p12}=0.5 and K_{i12}=62.5. Similarly, the resonant filter controller gains for the harmonic order of k=18, which corresponds to the 17^{th} and 19^{th} harmonic components, are chosen as K_{p12}=0.5 and K_{i12}=62.5. Note that the resonant filter controller gains are selected to realize a pole-zero cancellation such that $K_{pk}/ K_{ik} = L_F/R_F$. The proportional gain (K_P) of the RFCR is selected in Chapter 3 based on the desired phase margin of 45° for the PAF system. Its value is 40 as in the LPCR and CECR case. It is obvious that the K_P value for all linear current regulators is the same such that a fair comparison will be carried out.

Table 5.6 gives the steady-state performance of the RFCR by including the load current harmonics, line current harmonics, and IEEE 519 harmonic limits up to the 50^{th} harmonic current component in addition to THD_I, THD_V, PF, and f_{AVG}. Based on the table, all the current harmonics are well below the IEEE 519 limits and the load current harmonics are suppressed up to the 35^{th} harmonic as in the case of LPCR and CECR. However, when the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} line current harmonic

components for RFCR are compared to the harmonic components in LPCR and CECR case (Table 5.4 and Table 5.5 respectively), the percentage reduction of the mentioned harmonics is noticeable. While the 5^{th} harmonic component is 2.5% for the LPCR and 1.5% for the CECR, it is 0.6% for the RFCR. Similarly, the percentage reduction in the 7^{th}, 11^{th}, 13^{th}, 17^{th} and 19^{th} harmonic components for the RFCR can be observed by comparing Table 5.4, Table 5.5 and Table 5.6. This percentage reduction in the most dominant harmonic components results in the THD_I reduction for the RFCR. The THD_I value for the RFCR is 3.1%, which is lower than the THD_I value of 5.1% for the LPCR and the THD_I value of 3.9% for the CECR. Since the switching harmonics constitute voltage distortion for the linear current regulator, the THD_V for the RFCR, which is 3.8%, has the same value as in the LPCR and the CECR. The PF value is 0.998 and f_{AVG} is 13.3 kHz for the RFCR. Figure 5.13 illustrates the line current, filter current reference and filter current for the RFCR. Although the RFCR results in a lower THD_I value compared to the LPCR and the CECR, tracking performance of the current regulator in high di/dt regions of current reference similar to the LPCR and CECR. Current spikes still exits on the line current waveform. Figure 5.14 illustrates the harmonic spectrum of the line current. The dominant switching ripple current occurs at 20 kHz as in LPCR and CECR. Moreover, when the harmonic spectrum of the line current below 1 kHz in Figure 5.14 for the RFCR is compared to Figure 5.10 for the LPCR and Figure 5.12 for the CECR, the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonic components magnitude reduction can be easily observed. The higher order line current harmonic percentages in Table 5.6 for the RFCR are similar to the ones for the LPCR in Table 5.4 utilizing the same K_P value.

Table 5.6 Line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for RFCR, and IEEE 519 limits

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%)	IEEE 519 Harmonic Current Limits for I_{SC}/I_{L1}=173 (%)
I_1	100.0	100.0	100.0
I_5	30.0	0.5	12.0
I_7	9.0	0.1	12.0
I_{11}	7.0	0.1	5.5
I_{13}	3.7	0.1	5.5
I_{17}	3.0	0.1	5.0
I_{19}	2.2	0.1	5.0
I_{23}	1.4	0.5	2.0
I_{25}	1.3	0.5	2.0
I_{29}	0.8	0.4	2.0
I_{31}	0.7	0.5	2.0
I_{35}	0.5	0.3	1.0
I_{37}	0.5	0.3	1.0
I_{41}	0.4	0.3	1.0
I_{43}	0.4	0.4	1.0
I_{47}	0.3	0.3	1.0
I_{49}	0.3	0.3	1.0
THD_I (%)	32.6	3.1	15.0
THD_V (%)	0.5	3.8	5.0
PF	0.930	0.998	---
f_{AVG} (kHz)		13.3	

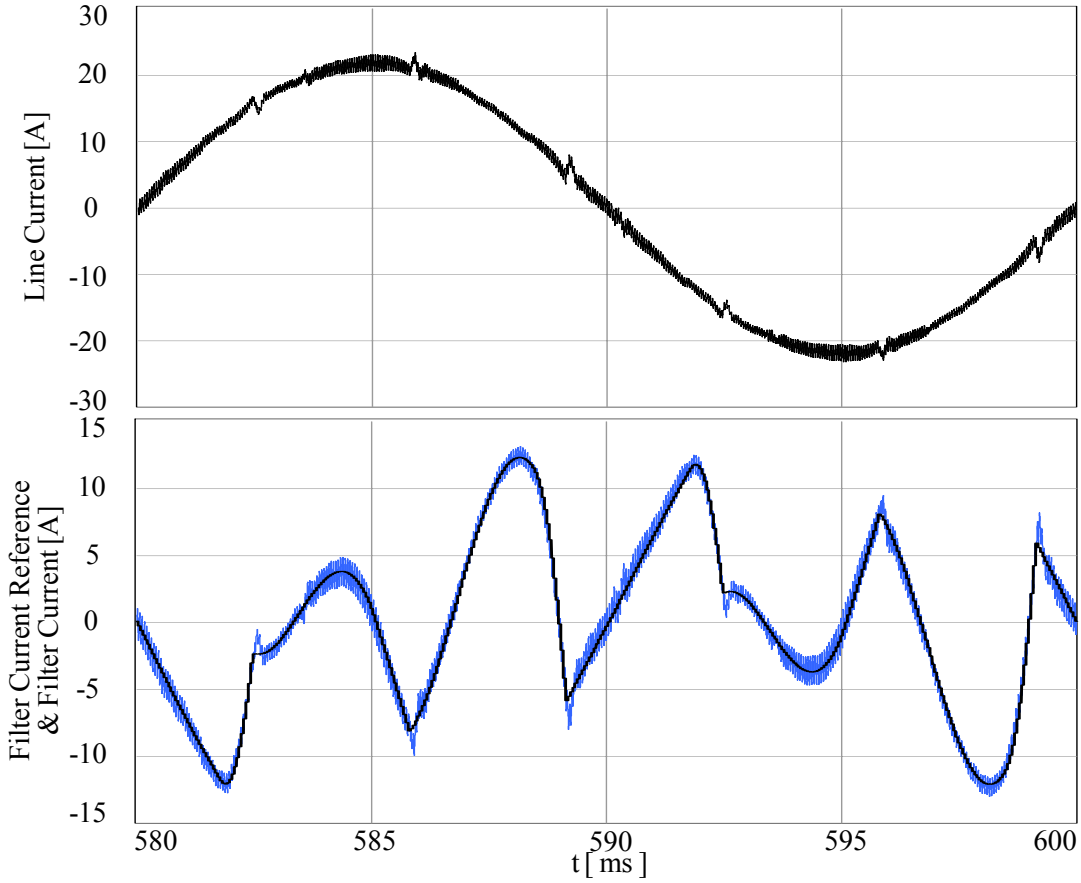

Figure 5.13 Line current, filter current reference (black) and filter current (blue) waveforms over a fundamental cycle for RFCR.

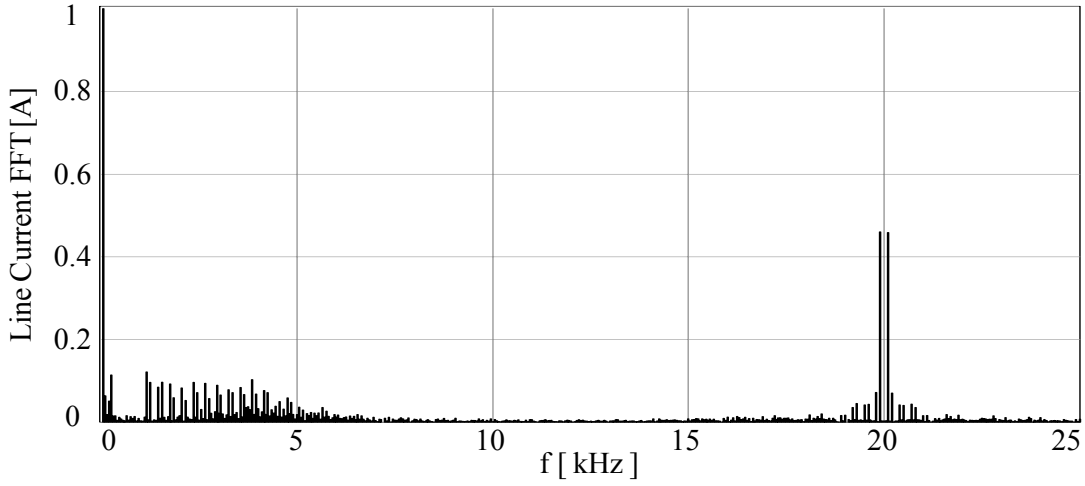

Figure 5.14 Line current harmonic spectrum for RFCR.

5.4.3 AHCR Simulation Results

This subsection includes the computer simulation results of the analog hysteresis current regulator (AHCR). As mentioned previously, since the experimental realization of the PAF in this thesis is performed by a discrete time controller, the practical implementation of AHCR is not realized in this thesis. However, it is important to observe and compare the current tracking performance of the AHCR for the current reference characterized by its multiple frequency and high di/dt content.

The upper and lower hysteresis band for the hysteresis current regulator is determined as 0.5 A and -0.5 A in order to minimize the current ripple. Table 5.7 summarizes the steady-state performance of the AHCR. When the table is analyzed, all the current harmonics are well below the IEEE-519 limits and the load current harmonics are suppressed considerably, which illustrates the high bandwidth of the AHCR. This high bandwidth results in a low THD_I value of 2.5%. Compared to previously discussed and analyzed current regulators, the THD_I performance of the AHCR is superior. The THD_V value of the AHCR is 4.5%. The reason of such a high THD_V value for AHCR compared to the linear current regulators is that high frequency current ripple due to analog application, which is to be eliminated by the SRF. The PF value is 0.998 and f_{AVG} is 28.6 kHz. The f_{AVG} for the PAF system with the AHCR is high compared to linear current regulators due to analog application, and this high f_{AVG} is prohibitive due to the thermal instability. The tracking performance of the AHCR observed by the line current waveform, filter current reference and filter current waveforms is illustrated in Figure 5.15. The current spikes do not exist on the line current waveform, which illustrates the high current bandwidth of the AHCR and its superior tracking capability for the current reference with high di/dt. Figure 5.16 illustrates the harmonic spectrum of the source current up to 25 kHz. Superior low frequency harmonic compensation of the AHCR can be observed by comparing the harmonic current spectrum of the line current in Figure 5.16 to the harmonic spectrums of line current for the previously discussed current regulators. The switching harmonic current spectrum spreads over a wide frequency range and differs from linear current regulators.

Table 5.7 Line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for AHCR, and IEEE 519 limits

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%)	IEEE 519 Harmonic Current Limits for I_{SC}/I_{L1}=173 (%)
I_1	100.0	100.0	100.0
I_5	30.0	1.1	12.0
I_7	9.0	0.2	12.0
I_{11}	7.0	0.4	5.5
I_{13}	3.7	0.2	5.5
I_{17}	3.0	0.3	5.0
I_{19}	2.2	0.2	5.0
I_{23}	1.4	0.2	2.0
I_{25}	1.3	0.1	2.0
I_{29}	0.8	0.2	2.0
I_{31}	0.7	0.2	2.0
I_{35}	0.5	0.1	1.0
I_{37}	0.5	0.2	1.0
I_{41}	0.4	0.1	1.0
I_{43}	0.4	0.1	1.0
I_{47}	0.3	0.1	1.0
I_{49}	0.3	0.1	1.0
THD_I (%)	32.6	2.5	15.0
THD_V (%)	0.5	4.5	5.0
PF	0.930	0.998	---
f_{AVG} (kHz)		28.6	

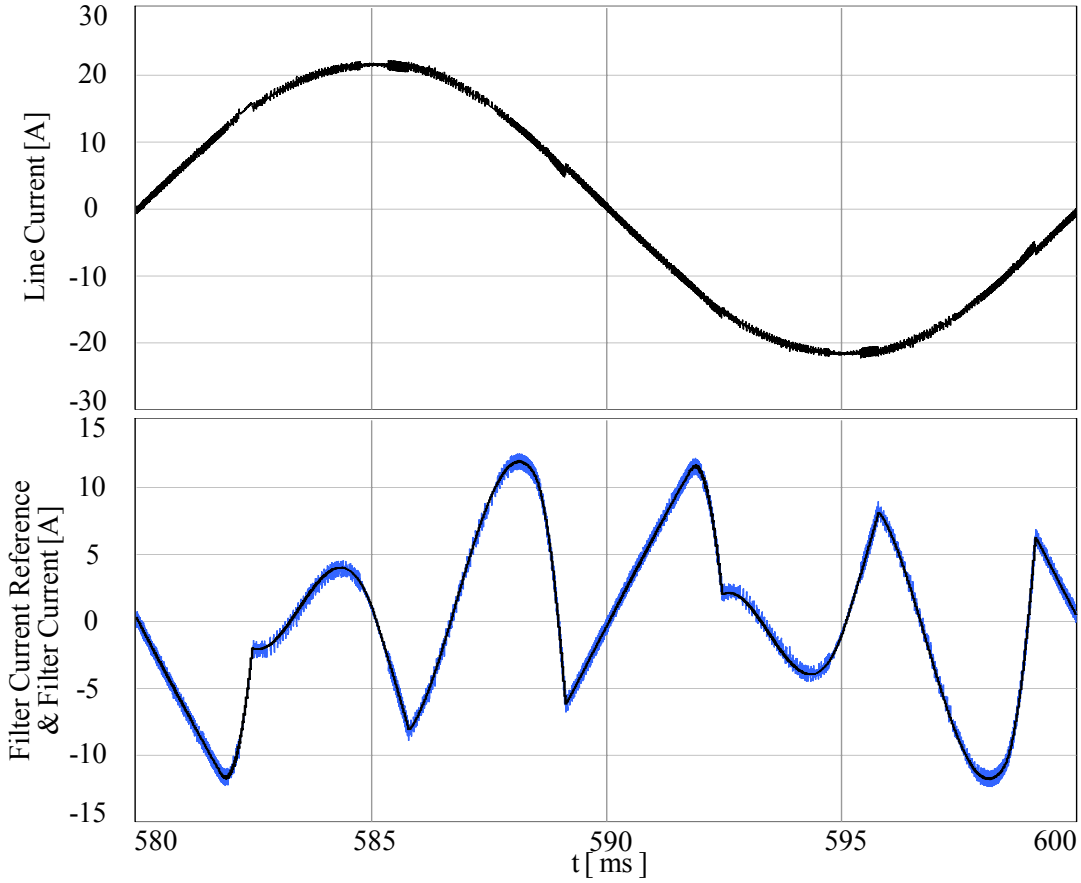

Figure 5.15 Line current, filter current reference (black) and filter current (blue) waveforms over a fundamental cycle for AHCR.

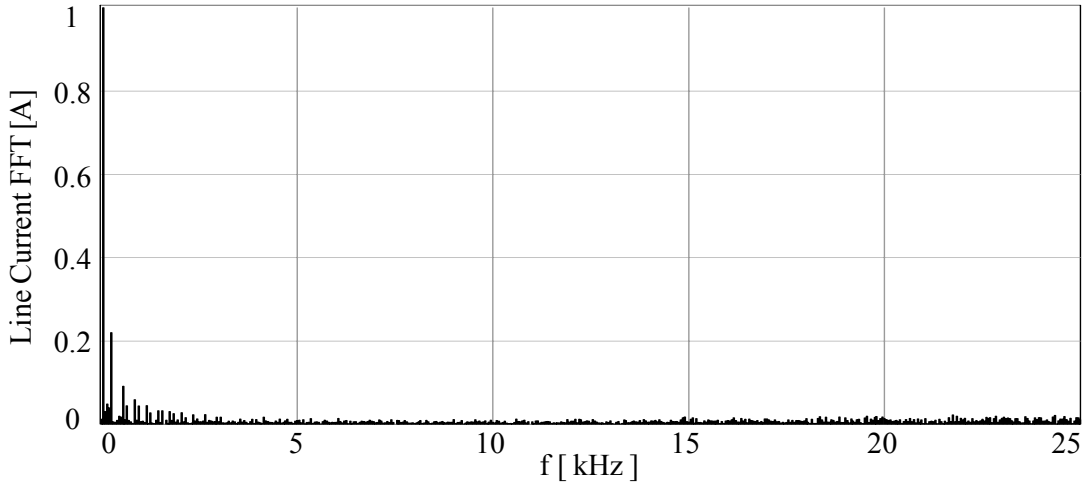

Figure 5.16 Line current harmonic spectrum for AHCR.

5.4.4 DHCR1 Simulation Results

The implementation of the DHCR1, which is the basic form of the discrete time current regulators, has been explained in Chapter 3. This subsection illustrates the simulation results of the DHCR1. The hysteresis band limit is chosen as 0.5 A as in the AHCR case. The sampling coefficient K is 2 and switching period (T_S) is 50 μs, which limits the maximum switching frequency to 20 kHz in DHCR1.

Table 5.8 summarizes steady-state performance of the DHCR1. When the table is analyzed, the poor bandwidth of the DHCR1 is noticeable. Although some dominant harmonic components such as the 5^{th} and 7^{th} are suppressed, the DHCR1 creates harmonic currents, which are greater than the load current harmonics in magnitude. When the line current harmonics above the 19^{th} harmonic order of Table 5.8 are analyzed, they are greater than the load current harmonics. The reason is the total delay in DHCR1, which results in poor bandwidth and high current ripple especially for the applications with low inductance value. Figure 5.17 illustrates the line current, filter current reference and filter current waveforms for DHCR1. Although, the line current waveform has a sinusoidal shape, the high current ripple on it is noticeable. The THD_I value for the DHCR1 is 30.4%, which is well above the IEEE 519 limit of 15% and close the load current THD_I value of 32.6%. Although, the characteristic harmonics of the load current up to 50^{th} order listed in Table 5.8 do not have high percentages, non-characteristic harmonics that the PAF system with DHCR1 creates appear on the line current waveform. Switching harmonics around 4 kHz, illustrated in the harmonic spectrum of the line current (Figure 5.18), are the reason of such a high THD_I value. The DHCR1 creates switching frequency harmonics around 4 kHz with unacceptable magnitude. The f_{AVG} of the DHCR1 is very low with the value of 2.8 kHz, which is the other reason of such a low bandwidth. Although the PAF compensates for reactive power of load, the highly distorted line current results in a poor PF of 0.955 compared to the other regulators discussed previously. The above discussion shows that DHCR1, the conventional discrete time current regulator which samples the filter current twice in a 50 μs for control purposes, is not an acceptable current regulator in the PAF application due to its poor bandwidth and

high ripple content. Therefore, multi-rate sampling is mandatory in the discrete time application of the hysteresis current regulators as discussed in Chapter 3.

Table 5.8 Line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for DHCR1, and IEEE 519 limits

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%)	IEEE 519 Harmonic Current Limits for I_{SC}/I_{L1}=173 (%)
I_1	100.0	100.0	100.0
I_5	30.0	1.2	12.0
I_7	9.0	1.2	12.0
I_{11}	7.0	5.9	5.5
I_{13}	3.7	0.8	5.5
I_{17}	3.0	0.5	5.0
I_{19}	2.2	1.3	5.0
I_{23}	1.4	2.8	2.0
I_{25}	1.3	2.2	2.0
I_{29}	0.8	1.1	2.0
I_{31}	0.7	7.1	2.0
I_{35}	0.5	2.1	1.0
I_{37}	0.5	1.4	1.0
I_{41}	0.4	0.8	1.0
I_{43}	0.4	1.9	1.0
I_{47}	0.3	3.8	1.0
I_{49}	0.3	0.4	1.0
THD_I (%)	32.6	30.4	15.0
THD_V (%)	0.5	5.0	5.0
PF	0.930	0.955	---
f_{AVG} (kHz)		2.8	

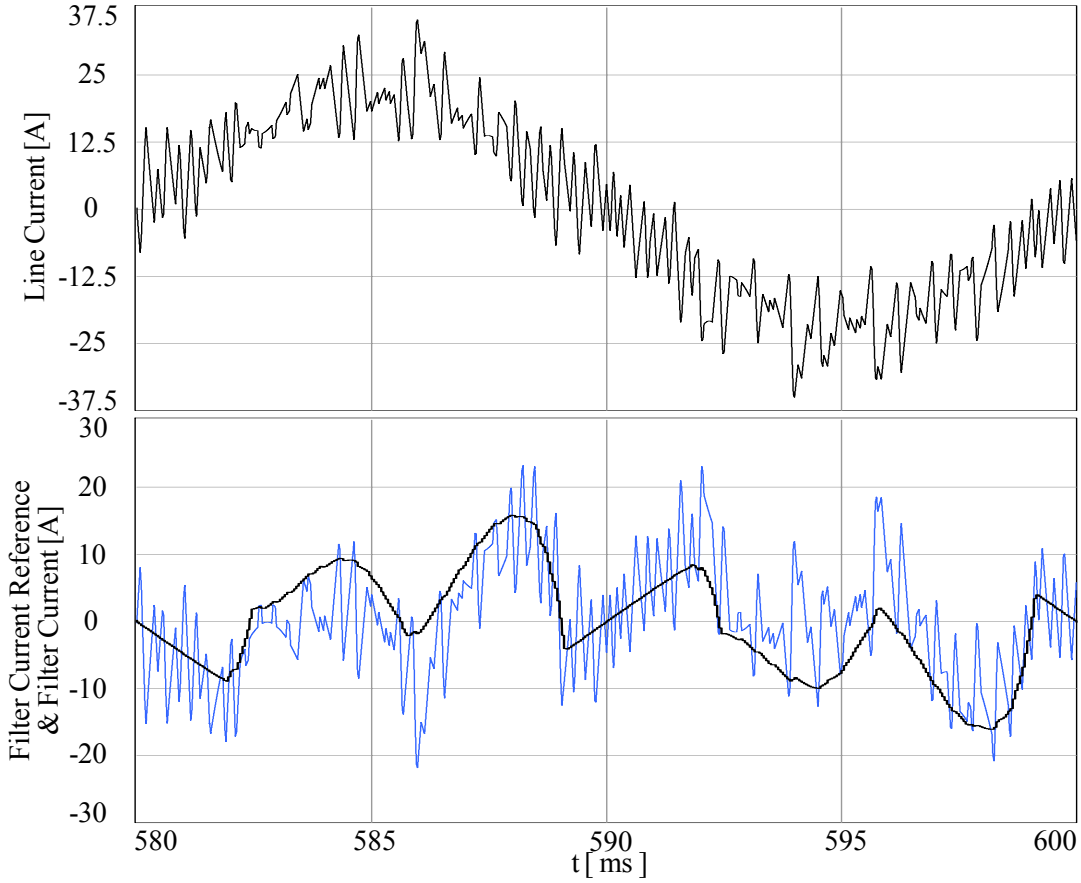

Figure 5.17 Line current, filter current reference (black) and filter current (blue) waveforms over a fundamental cycle for DHCR1.

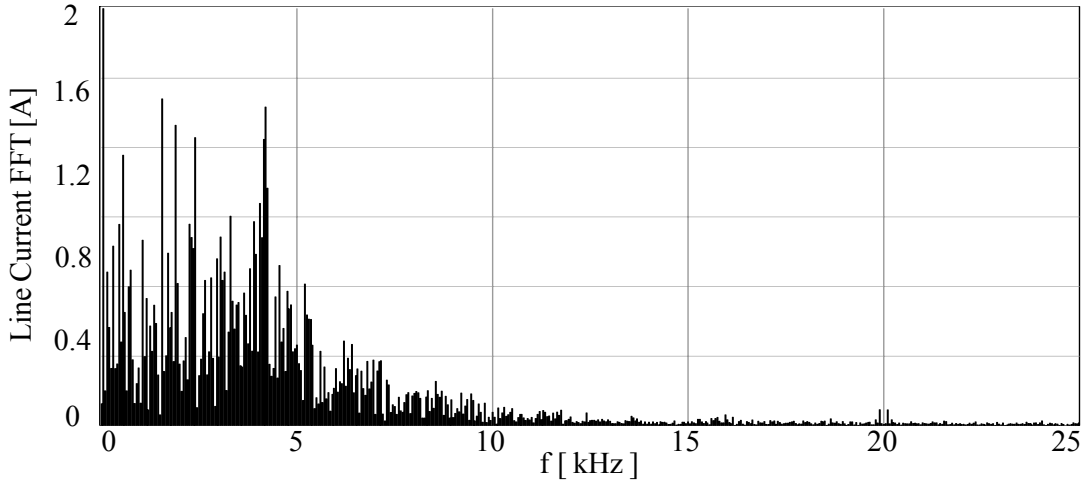

Figure 5.18 Line current harmonic spectrum for DHCR1.

5.4.5 DHCR2 Simulation Results

The DHCR2 is the improved version of the DHCR1 with sampling coefficient K of 10 in order to decrease measurement delay. T_S is again 50 μs to limit the maximum switching frequency of the PAF system to 20 kHz by the switch lock mechanism described in Chapter 3. The hysteresis band limit is again 0.5 A as in the previously analyzed hysteresis current regulators.

Table 5.9 summarizes the simulation results of the DHCR2. The bandwidth improvement is easily observed by analyzing the line current harmonics. The regulator compensates the load current harmonics up to 29^{th} harmonic order. Compared to the DHCR1, the THD_I is improved from 30.4% to 10.4%. Reducing the measurement delay in the DHCR2 enhances the steady-state performance of the discrete time current regulator. Moreover, the improvement in the DHCR2 compared to the DHCR1 can be observed from the line current, current reference, and filter current waveforms in Figure 5.19. The ripple content is reduced and tracking capability of the current regulator is enhanced with the utilization of the DHCR2. The THD_V value for DHCR2 is 5.0% due to high frequency ripple content of line current. PF is enhanced from 0.955 to 0.993. The f_{AVG} value for DHCR2 is 7.8 kHz. Figure 5.20 illustrates harmonic current spectrum of the line current for DHCR2. The switching frequency harmonic currents spread over a wide frequency range, which is a typical characteristic of the hysteresis current regulators. Moreover, when the line current harmonic spectrum for the DHCR1 in Figure 5.18 is compared to Figure 5.20, the switching harmonic ripple reduction in magnitude is noticeable for the DHCR2. Decreasing the measurement delay from $T_S/2$ in DHCR1 to $T_S/10$ in the DHCR2 improves the performance of a discrete time hysteresis current regulator. Moreover, the switching algorithm described in Chapter 3 for DHCR2 limits f_{MAX} ensuring thermal reliability. Although the performance improvement for the DHCR2 compared to the DHCR1 is noticeable, the performance of the DHCR2 is poor compared to linear current regulators in terms of THD_I, bandwidth of the regulator, current ripple magnitude, and current tracking capability.

Table 5.9 Line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for DHCR2, and IEEE 519 limits

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%)	IEEE 519 Harmonic Current Limits for I_{SC}/I_{L1}=173 (%)
I_1	100.0	100.0	100.0
I_5	30.0	0.5	12.0
I_7	9.0	1.1	12.0
I_{11}	7.0	1.9	5.5
I_{13}	3.7	0.3	5.5
I_{17}	3.0	1.5	5.0
I_{19}	2.2	0.4	5.0
I_{23}	1.4	1.0	2.0
I_{25}	1.3	0.6	2.0
I_{29}	0.8	0.9	2.0
I_{31}	0.7	0.6	2.0
I_{35}	0.5	0.3	1.0
I_{37}	0.5	0.9	1.0
I_{41}	0.4	0.8	1.0
I_{43}	0.4	0.7	1.0
I_{47}	0.3	0.7	1.0
I_{49}	0.3	0.2	1.0
THD_I (%)	32.6	10.4	15.0
THD_V (%)	0.5	5.1	5.0
PF	0.930	0.993	---
f_{AVG} (kHz)		7.8	

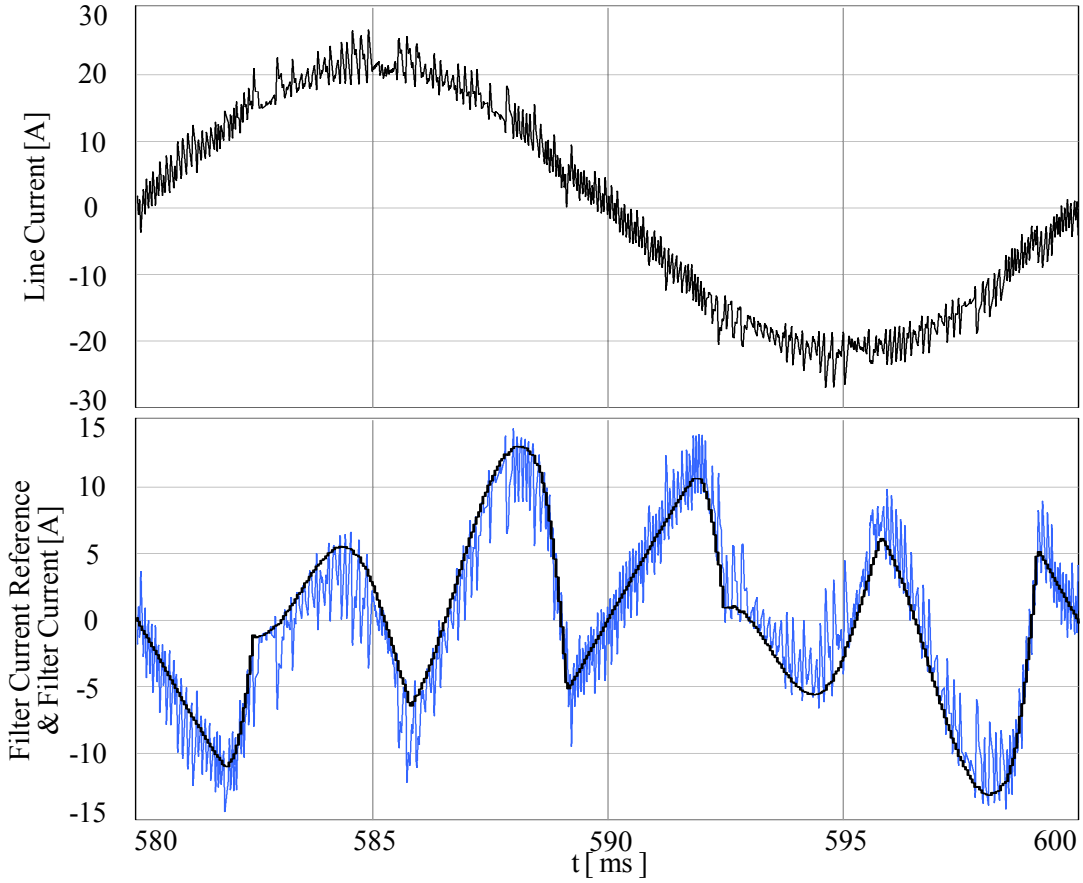

Figure 5.19 Line current, filter current reference (black) and filter current (blue) waveforms over a fundamental cycle for DHCR2.

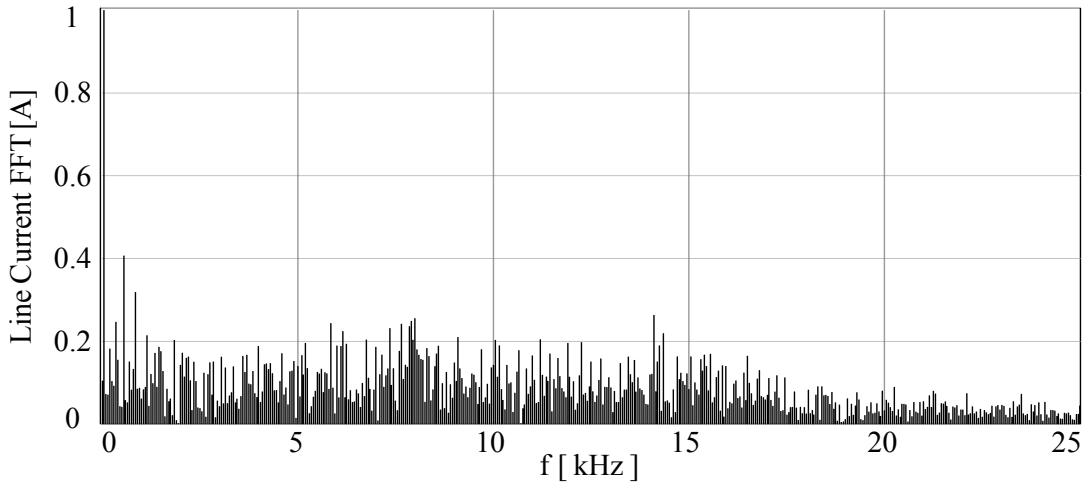

Figure 5.20 Line current harmonic spectrum for DHCR2.

5.4.6 DHCR3 Simulation Results

As in the DHCR2, the sampling coefficient K is 10 and T_S is 50 μs in the DHCR3. By the switch release mechanism described in Chapter 3, the maximum switching frequency is limited to 20 kHz while the bandwidth of the current regulator is enhanced. The hysteresis band limit for the DHCR3 is 0.5 A as in the analyzed hysteresis current regulators. Table 5.10 summarizes the simulation results of the DHCR3. The DHCR3 suppresses the load current harmonics up to the 47^{th} harmonic order. This illustrates the high bandwidth of the DHRC3. Compared to the DHCR2, the bandwidth improvement is noticeable while still limiting the maximum switching frequency to 20 kHz as in the DHCR1 and the DHCR2. This bandwidth improvement results in a THD_I value of 7.6%, which is well below THD_I value of 10.4% for DHCR2. The line current, the filter current reference and filter current waveforms in Figure 5.21 illustrate the tracking capability of the DHCR3 with reduced current ripple content on the waveforms compared to the DHCR2. Although the line current harmonic percentages for the DHCR3 in Table 5.10 are generally lower than the linear current harmonic percentages for linear current regulators in Table 5.4, Table 5.5 and Table 5.6, the reason that the DHCR3 has a higher THD_I value than the THD_I values of linear current regulators is that the harmonic spectrum of the DHCR3 which spreads over a wide frequency range as illustrated in Figure 5.22. When the figure is analyzed, the line current includes switching ripple current content spreading over a wide frequency range, which is a typical characteristic of hysteresis current regulator as mentioned in previous sections. Further, the THD calculator in Ansoft-Simplorer package utilizes all the frequencies components of the defined quantity while calculating the THD_I and the THD_V. Therefore it is logical to observe a high THD_I value for DHCR3 due its harmonic spectrum. However, compared to the harmonic spectrum of the DHCR2 in Figure 5.20, the switching ripple current magnitude above the bandwidth of the DHCR3 is considerably reduced. Moreover, the spectrum has a density at around 16 kHz, which is close to 20 kHz value, which can be interpreted as the linearization of the DHCR3. In fact, if the switching mechanism of DHCR3 is analyzed, DHCR3 utilizes duty cycles with the resolution of 0.1. This can be interpreted as an approximation of DHCR3 to linear

current regulators. Moreover, the f_{AVG} of 10.0 kHz for DHCR3, which gets closer to f_{AVG} of 13.3 kHz for the linear current regulators compared to the DHCR1 and DHCR2 can be another interpretation of the linearization of DHCR3. The THD_V value and PF of DHCR3 are 5.1% and 0.996. Another observation is that the dynamic performance of the DHCR3 is better than the linear current regulators by analyzing the line current waveforms of current regulator. Although the ripple content of the DHCR3 is high compared to linear current regulators, the current spikes on the source current waveform of the DHCR3 occurring during the high di/dt regions are lower in magnitude due to the increased sampling rate and switch release mechanism involved in the DHCR3. The above discussion illustrates that the steady-state performance and tracking capability of discrete time hysteresis current regulators can be improved with multi-rate sampling and proper switch release mechanism as in the DHCR3.

Table 5.10 Line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for DHCR3, and IEEE 519 limits

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%)	IEEE 519 Harmonic Current Limits for I_{SC}/I_{L1}=173 (%)
I_1	100.0	100.0	100.0
I_5	30.0	0.7	12.0
I_7	9.0	0.8	12.0
I_{11}	7.0	0.9	5.5
I_{13}	3.7	0.9	5.5
I_{17}	3.0	0.6	5.0
I_{19}	2.2	0.4	5.0
I_{23}	1.4	0.2	2.0
I_{25}	1.3	0.3	2.0
I_{29}	0.8	0.4	2.0
I_{31}	0.7	0.4	2.0
I_{35}	0.5	0.5	1.0
I_{37}	0.5	0.2	1.0
I_{41}	0.4	0.1	1.0
I_{43}	0.4	0.2	1.0
I_{47}	0.3	0.1	1.0
I_{49}	0.3	0.3	1.0
THD_I (%)	32.6	7.6	15.0
THD_V (%)	0.5	5.1	5.0
PF	0.930	0.996	---
f_{AVG} (kHz)		10.0	

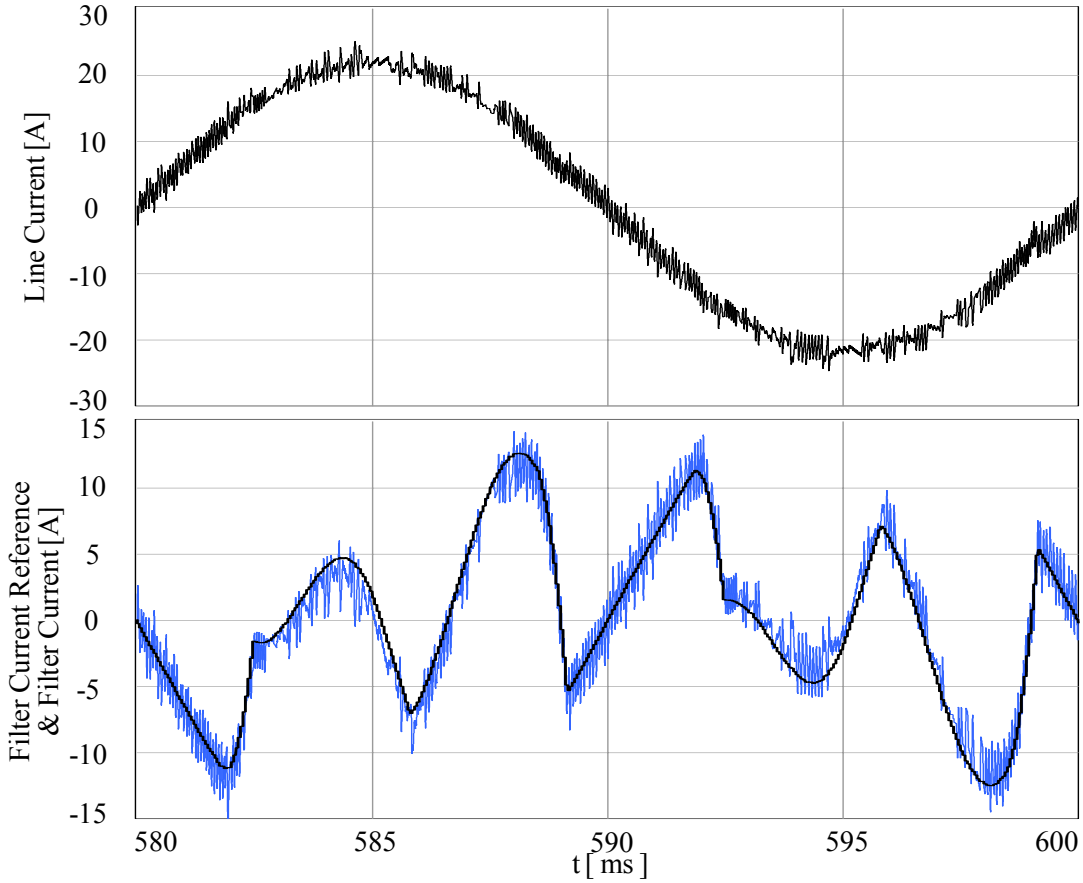

Figure 5.21 Line current, filter current reference (black) and filter current (blue) waveforms over a fundamental cycle for DHCR3.

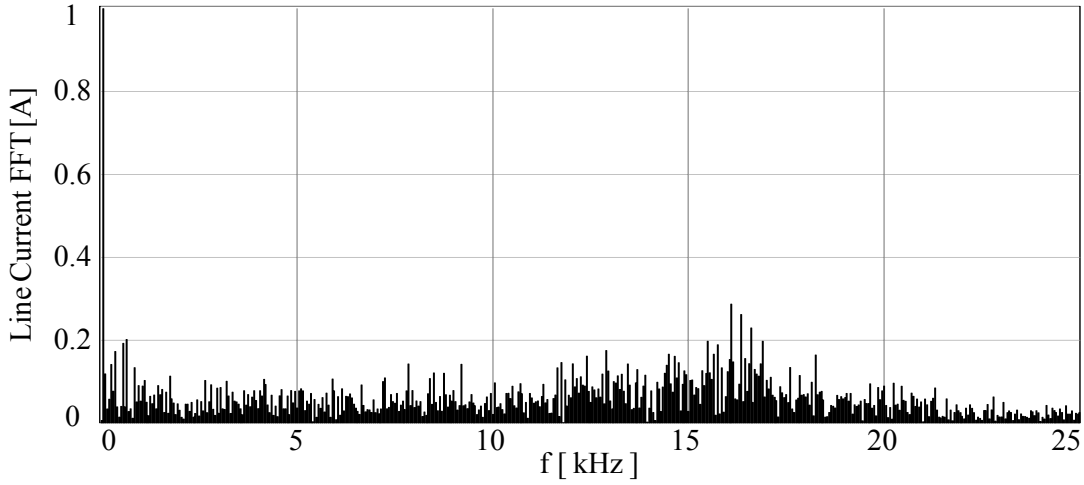

Figure 5.22 Line current harmonic spectrum for DHCR3.

5.4.7 Summary of The Current Regulator Performance Comparison without SRF by Means of Computer Simulation

Although a comparison study is carried out during the analysis of the computer simulation results of the discussed current regulators, it is important to illustrate the simulations results of the current regulators in one table in order to provide a better comparison. This section summarizes and thoroughly compares the simulation results of the discussed current regulators. It is known that switching characteristics, as a result switching harmonics, of the linear current regulators and the on-off current regulators are different. Therefore, it is difficult to provide a fair comparison between the linear and the on-off current regulators. However, by including the switching frequency harmonics in the THD_I and THD_V values of the discussed regulators and utilizing the same maximum switching frequency of 20 kHz for all current regulators, a fair comparison could be provided.

Table 5.11 collects all the data available in Table 5.4 through Table 5.10. According to the table, all the current regulators except DHCR1 meet IEEE 519 harmonic and THD_I limits. The reason for poor performance of the DHCR1 is the total measurement delay and switch signal output delay. Among the current regulators, the AHCR has the best THD_I value of 2.5% due to superior tracking performance of the analog implementations. However, this superior tracking performance results in a considerable high f_{AVG} value of 28.6 kHz, which is prohibitive when the thermal reliability of the system is considered.

However, when the f_{MAX} limit of 20 kHz is applied, the RFCR has the lowest THD_I value of 3.1% due to its superior gain characteristics at the most dominant harmonic frequencies. Although the CECR has the second lowest THD_I value and the limited f_{AVG} value of 13.3 kHz, the analog implementation of the CECR is prohibitive. The THD_I performance of the LPCR, which is 5.1%, is better than THD_I performance of the DHCR3, which is 7.6%. However, as it is mentioned earlier and it is obvious from Table 5.11 that the suppression capability of the DHCR3 for the most of the harmonics orders up to 50^{th} is better than the suppression

capability of discrete time applicable linear current regulators, the LPCR and the RFCR. The reason is the contribution of the switching ripple harmonics, which the DHCR3 creates and spreads over a wide frequency range, to the THD_I value. When the bandwidth, the THD_I value and f_{AVG} of 10.0 kHz, of the DHCR3 are considered, its performance gets closer to the performance of practically utilized LPCR. When the THD_V values of current regulators are analyzed, hysteresis current regulators have higher THD_V values due to the wide frequency range switching harmonic currents resulting in high frequency voltage distortion on the voltage waveform at PCC. The THD_V values of the discrete time hysteresis current regulators are above IEEE 519 limit of 5% while the THD_V values of the linear current regulators are below IEEE 519 limit of 5%. However, the THD_V values of the linear current regulators are close to the 5% limit. These values will be reduced with the inclusion of the SRF in the PAF system. The PF values are close to unity, which is an illustration of reactive power compensation of the PAF.

Among the all discrete time applicable current regulators, the RFCR illustrates superior steady-state performance. Although, the LPCR has a better performance than the DHCR3, the steady-state performance of the DHCR3 is close to that of the LPCR. Although the DHCR2 meets IEEE 519 limits, the THD_I value is a bit high compared to the LPCR, the RFCR and the DHCR3. However, the f_{AVG} value of the DHCR2 is lower than the discrete time applicable linear current regulator and the DHCR3. The poor performance of the DHCR1 with its low f_{AVG} value of 2.8 kHz due to measurement and output release delay eliminates the DHCR1 as an applicable current regulator in PAF system. When the THD_I value and the f_{AVG} of discrete time applicable current regulators are compared, the conclusion is that a lower average switching frequency of PAF system results in THD_I value increase, or vice versa. The above discussion illustrates that the LPCR, the RFCR and the proposed DHCR3 are the viable chooses for the PAF system implemented in discrete time and the future discussion for the PAF system will include only these regulators. The next section analyzes the SRF which is a mandatory part for the PAF system in order to eliminate high frequency switching harmonics that VSI creates.

Table 5.11 Computer simulation results of the line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for all the simulated current regulators and IEEE 519 limits without SRF

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%) LPCR	Line Current Harmonics with PAF (%) CECR	Line Current Harmonics with PAF (%) RFCR	Line Current Harmonics with PAF (%) AHCR	Line Current Harmonics with PAF (%) DHCR1	Line Current Harmonics with PAF (%) DCHR2	Line Current Harmonics with PAF (%) DHCR3	IEEE 519 Harmonic Current Limits (I_{SC}/I_{L1}=173) (%)
I_1	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
I_5	30.0	2.5	1.5	0.5	1.1	1.2	0.5	0.7	12.0
I_7	9.0	0.9	0.5	0.1	0.2	1.2	1.1	0.8	12.0
I_{11}	7.0	1.3	0.6	0.1	0.4	5.9	1.9	0.9	5.5
I_{13}	3.7	0.8	0.4	0.1	0.2	0.8	0.3	0.9	5.5
I_{17}	3.0	1.0	0.5	0.1	0.3	0.5	1.5	0.6	5.0
I_{19}	2.2	0.6	0.3	0.1	0.2	1.3	0.4	0.4	5.0
I_{23}	1.4	0.6	0.3	0.5	0.2	2.8	1.0	0.2	2.0
I_{25}	1.3	0.5	0.3	0.5	0.1	2.2	0.6	0.3	2.0
I_{29}	0.8	0.4	0.2	0.4	0.2	1.1	0.9	0.4	2.0
I_{31}	0.7	0.4	0.2	0.5	0.2	7.1	0.6	0.4	2.0
I_{35}	0.5	0.5	0.2	0.3	0.1	2.1	0.3	0.5	1.0
I_{37}	0.5	0.3	0.2	0.3	0.2	1.4	0.9	0.2	1.0
I_{41}	0.4	0.4	0.1	0.3	0.1	0.8	0.8	0.1	1.0
I_{43}	0.4	0.2	0.1	0.4	0.1	1.9	0.7	0.2	1.0
I_{47}	0.3	0.4	0.1	0.3	0.1	3.8	0.7	0.1	1.0
I_{49}	0.3	0.3	0.2	0.3	0.1	0.4	0.2	0.3	1.0
THD_I (%)	32.6	5.1	3.9	3.1	2.5	30.4	10.4	7.6	15.0
THD_V (%)	0.5	3.8	3.8	3.8	4.5	5.0	5.1	5.1	5.0
PF	0.930	0.998	0.998	0.998	0.998	0.955	0.993	0.996	---
f_{AVG}(kHz)		13.3	13.3	13.3	28.6	3.8	7.8	10.0	

5.5 Computer Simulation Results of The Designed SRF Topologies

Through the theoretical analysis in Chapter 4, the designed tuned LCR type SRF will be utilized for the linear current regulators and the designed high-pass RC type SRF will be utilized for the hysteresis current regulators due to their performance, simple structure, small size and low cost. The performances of the designed SRFs will be investigated by means of computer simulations in this section. Moreover, the damping resistor R_d of the high-pass RC type SRF will be determined through the computer simulations.

5.5.1 Computer Simulation Results of The Tuned LCR Type SRF

In the Chapter 4, the tuned LCR type SRF for the PAF application is designed for the series resonant frequency of 20 kHz and parallel resonant frequency of 10 kHz. Based on the design constraints, C_F and L_F are found as 1.9 μF and 33.3 μH (Y connected) respectively for the line inductance (L_S) value of 100 μH. R_F is assumed to be the internal resistance of L_F and has a value of 100 mΩ. However, the C_F value of 2.2 μF, which is a practically available size and close to designed C_F value of 1.9 μF, will be utilized through simulations and experimental studies. The f_p value is 9.5 kHz for C_F =2.2 μF and is close to the design value of 10 kHz for the same f_s value of 20 kHz. The designed filter with the R_F value of 100 mΩ creates oscillations on the waveforms since the circuit parameters are assumed to be ideal in the computer simulation environment. Due to this reason, the R_F value is chosen as 660 mΩ such that the SRF attenuates 95% of the switching ripple currents at 20 kHz. That value of R_F damps the oscillations sufficiently and does not considerably affect the filtering characteristics of the tuned LCR type SRF. Table 5.12 summarizes the designed circuit parameters and the utilized circuit parameters of the tuned LCR type SRF for linear current regulators.

Figure 5.23 illustrates line current and its harmonic spectrum (FFT) and line voltage (voltage at PCC) and its FFT for the PAF utilizing the LPCR without and with tuned LCR type SRF. For the system without SRF, there exist ripple currents and voltages

on the line current in Figure 5.23.a and line voltage in Figure 5.23.c respectively due to switching at 20 kHz. Moreover the harmonic spectrums of line current and voltage verify the dominant switching ripple currents and voltages on the same figures. If the waveforms and their FFTs are investigated in Figure 5.23.b and 5.23.d for the tuned LCR type SRF and compared to Figure 5.23.a and 5.23.c where the SRF is not utilized, the attenuation of switching ripples is clear at 20 kHz and its multiples. As a result, the line current and voltage become switching ripple free. If the line current FFT in Figure 5.23.b is investigated for the SRF case, there exists an amplification of current harmonics at around 10 kHz due to parallel resonance of the SRF with the line inductance. Although, the effect of parallel resonance is not considerable due to the damping resistor R_F, this amplification illustrates the parallel resonance phenomena in the system.

Table 5.12 Circuit parameters of the designed and computer simulated tuned LCR type SRF

Parameters	Design	Simulation
Filter capacitor C_F (μF)	1.9	2.2
Filter inductor L_F (μH)	33.3	28.8
Filter resistor R_F (Ω)	0.1	0.66
Series resonant frequency (kHz)	20	20
Parallel resonant frequency (kHz)	10	9.5

Although, the performance of the designed tuned LCR type SRF is obvious on waveforms and their FTTs, another performance evaluation for SRF can be held by investigating the THD_I and THD_V values of the system without and with SRF. Table 5.13 illustrates the THD_I and THD_V performance of the system for the cases of without and with SRF. While THD_I of 5.1% is reduced to 4.1%, THD_V of 3.8% is reduced to 0.8% with the inclusion of SRF to the system. The reason that the effect of the SRF is most observable on the THD_V value is the high impedance value of line inductance at high frequencies. The switching ripple currents through the AC utility grid result in switching ripple voltages on the line inductance and result in voltage distortions of high frequencies. However, the line voltage at the PCC becomes

switching ripple voltage free with the inclusion of appropriate SRF type to the system.

The design for the tuned LCR type SRF can be performed for a f_p value of 15 kHz and the same f_s value of 20 kHz in order to have a small size C_F. However, it is mentioned in the theoretical analysis of Chapter 4 that C_F should be as large as possible for a better attenuation of switching ripple currents at the sidebands of f_{SW} and $2f_{SW}$. Figure 5.24 illustrates and compares the line current FFTs without SRF, with tuned LCR type SRF where C_F = 2.2 μF such that f_p = 9.5 kHz, f_s =20 kHz and R_F = 0.66 mΩ, and with tuned LCR type SRF where C_F = 0.5 μF such that f_p = 15 kHz, f_s =20 kHz and R_F = 0.66 mΩ. The attenuation of the switching ripple currents at the sidebands of 20 kHz and 40 kHz for the case of C_F = 0.5 μF (Figure 5.24.c) is less compared to for the case of C_F = 2.2 μF (Figure 5.24.b). That illustration verifies the effect of large C_F sizes on the performance of the tuned LCR type SRF.

Table 5.13 The THD performance of the PAF utilizing LPCR without and with tuned LCR type SRF

	THD_I (%)	THD_V (%)
Without SRF	5.5	3.8
With SRF	4.1	0.8

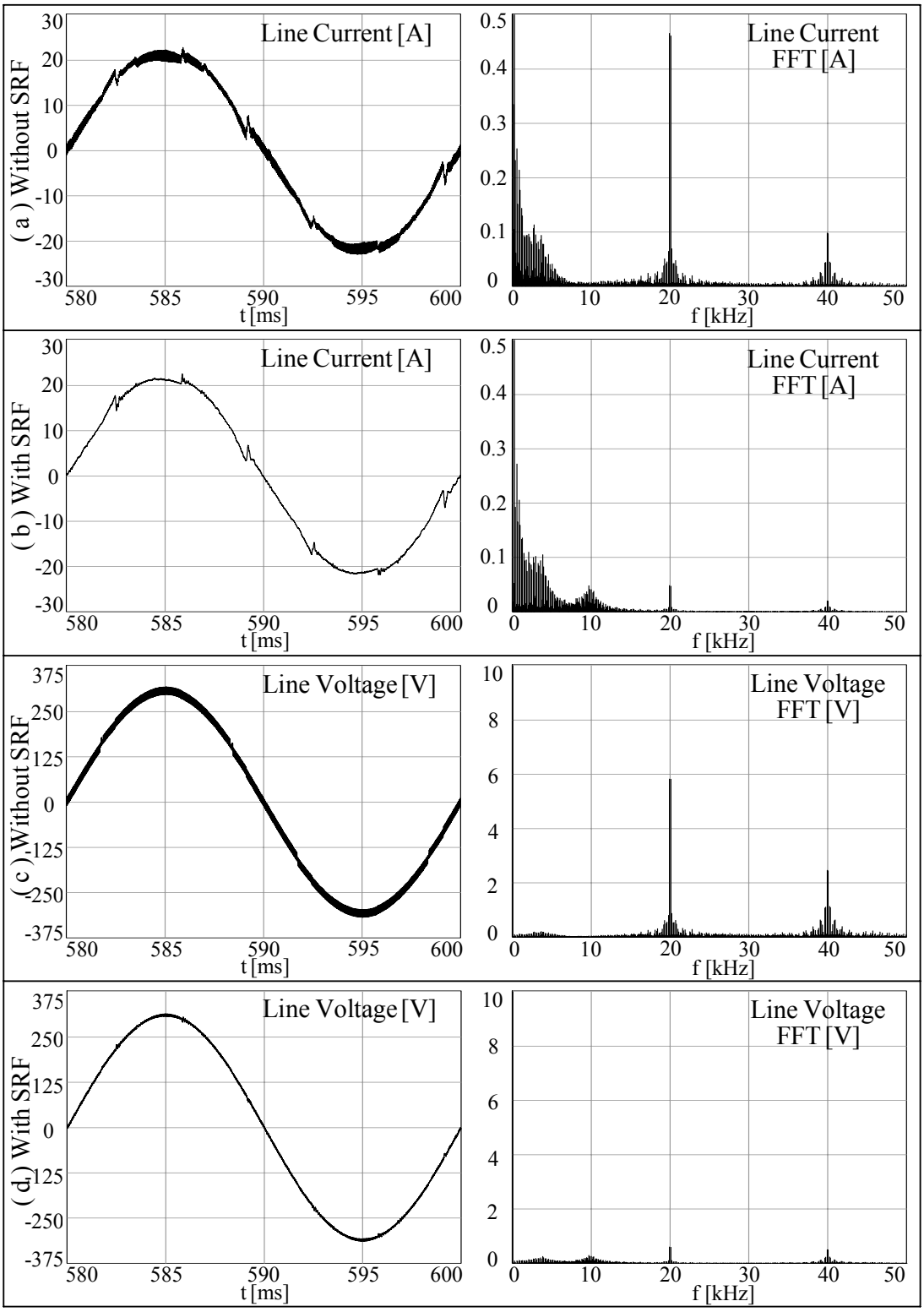

Figure 5.23 Line current, line voltage, and their FTTs in the PAF system utilizing LPCR without and with the tuned LCR type SRF.

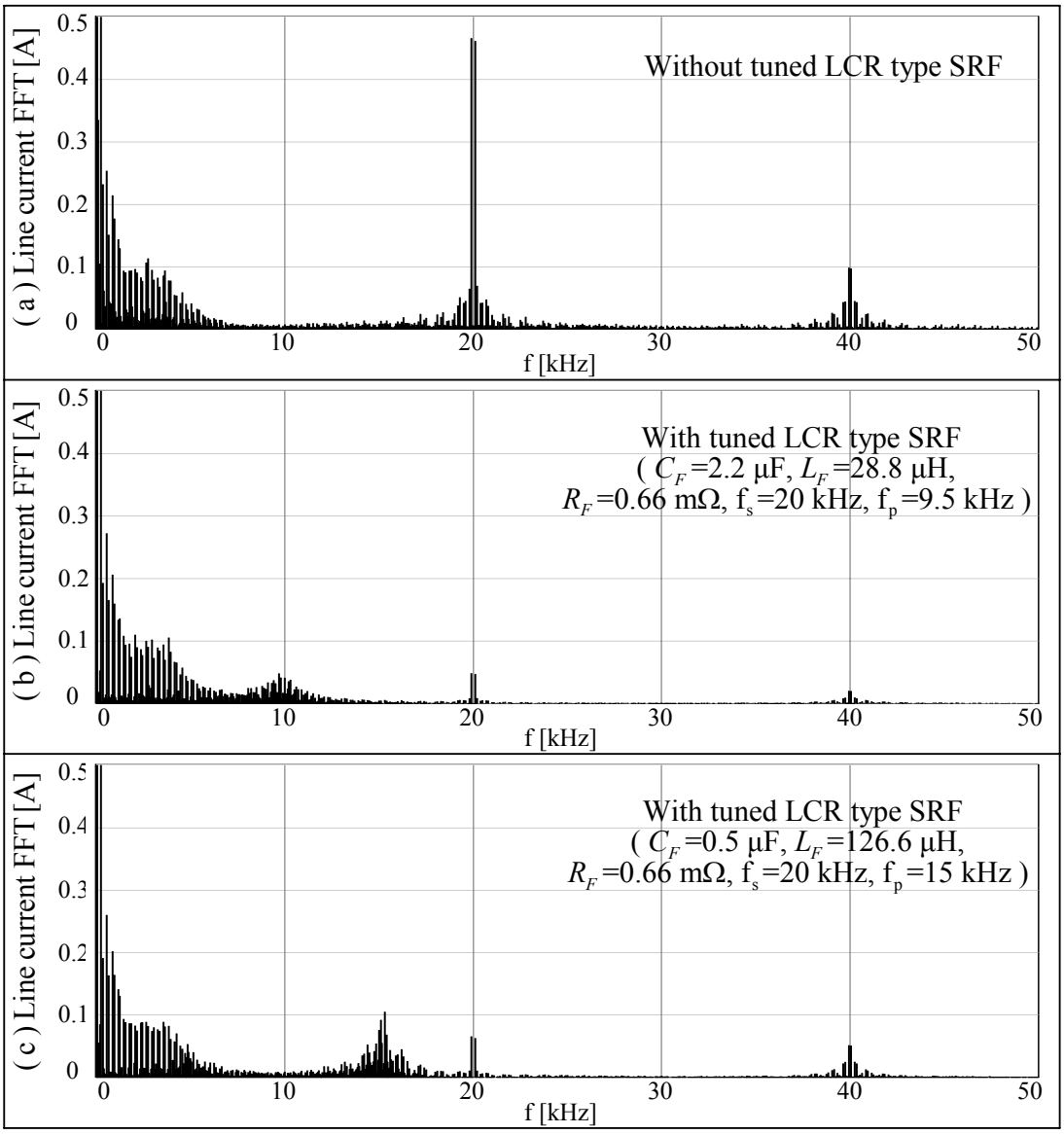

Figure 5.24 Line current FTTs of the PAF system utilizing LPCR:
a) without SRF, b) with the tuned LCR type SRF where C_F =1.9 µF,
and c) with the tuned LCR type SRF where C_F =0.5 µF.

5.5.2 Computer Simulation Results of The High-pass RC Type SRF

In Chapter 4, only the C_F value of the high-pass RC type SRF was determined as 30 µF according to the bandwidth of the DHCR3 in the PAF application. In this section, first, the damping resistor R_d value of the high-pass RC type SRF will be determined in terms of the THD_I and THD_V values and the amount of oscillations on the

waveforms due to parallel resonance phenomena through the computer simulations, and then the performance of the designed SRF will be investigated. Figure 5.25 illustrates THD_I and THD_V performances of the PAF system utilizing the DHCR3 for various R_d values and C_F =30 μF. As the figure illustrates, the THD_I values are above the THD_I value of 7.6% without SRF for low R_d values due to the insufficient damping of the parallel resonance. Although, the THD_I values are below the THD_I value of 7.6% without SRF for high R_d values, THD_V value increases as R_d value increases. However, the THD_V value is well below the THD_V value of 5.1% without the SRF for the considered R_d values. The optimum R_d value for SRF is between 1 Ω and 4 Ω. Low R_d values are preferable due to low power loss at fundamental frequency and better attenuation of high frequency switching ripple currents. Although low R_d values result in low THD_I and THD_V values, they result in low frequency oscillations on the line current waveform. Figure 5.26 illustrates the line current waveform where the high-pass RC type SRF is utilized for the system with C_F =30 μF and three different R_d values of 1 Ω, 2 Ω, and 3 Ω. There exists low frequency oscillations for R_d = 1 Ω in Figure 5.26.a due to parallel resonance. As the R_d value increases the oscillations are damped out while the high frequency switching ripple currents appear on the line current waveform (Figure 5.26.c). Therefore, the R_d value should be selected such that it will damp out the low frequency oscillations as in Figure 5.26.c for R_d = 3 Ω. Moreover, the THD_I and THD_V values in Figure 5.25 for R_d = 3 Ω do not change too much for R_d = 1 Ω and are well below the THD_I and THD_V values without SRF. As a result, R_d value for the high-pass RC type SRF is determined as 3 Ω where C_F was 30 μF through the previous discussions in the Chapter 4.

Since the designed filter will be realized in practice, R_d value of 2.8 Ω, which is a practically available size and close to the determined R_d value of 3 Ω through the computer simulation analysis, will be utilized in the simulations and experimental studies. Figure 5.27 illustrates line current and its harmonic spectrum (FFT) and line voltage (voltage at PCC) and its FFT for the PAF utilizing the DHCR3 without and with the high-pass RC type SRF. For the system without SRF, there exist ripple currents and voltages on the line current in Figure 5.27.a and the line voltage in

Figure 5.27.c respectively due to the switchings. Moreover the harmonic spectrums of the line current and voltage verify the switching ripple currents and voltages spread over a wide frequency range (5-25 kHz) and concentrated around 15-17 kHz on the same figure. If the waveforms and their FFTs are investigated in Figure 5.27.b and 5.27.d for the high-pass RC type SRF and compared to Figure 5.27.a and 5.27.c where the SRF is not utilized, the attenuation of switching ripples for a wide frequency range is clear. As a result, the line current and voltage become nearly switching ripple free. Moreover, The THD_I and THD_V values of the system without and with the SRF are given in Table 5.14. The THD_I of 7.6% is reduced to 4.2% and the THD_V of 5.1% is reduced to 1.5% with the inclusion of the SRF to the system. As a result, Figure 5.27 and Table 5.14 illustrate the performance of the designed high-pass RC type SRF for DHCR3 in PAF application such that line current and line voltage at the PCC become nearly switching ripple voltage free.

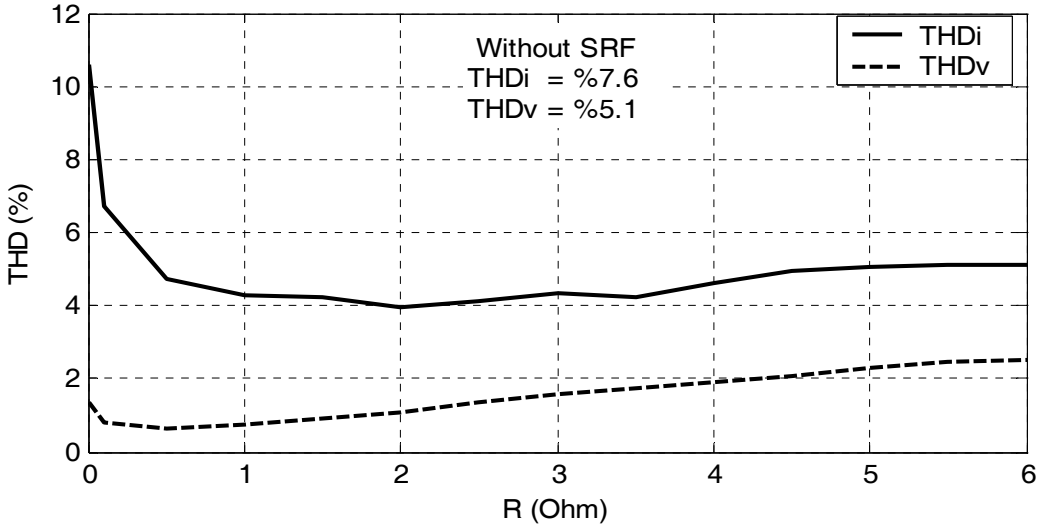

Figure 5.25 THD_I and THD_V performance of the PAF utilizing DHCR3 with the high-pass RC type SRF for C_F = 30 μF and various R_d values.

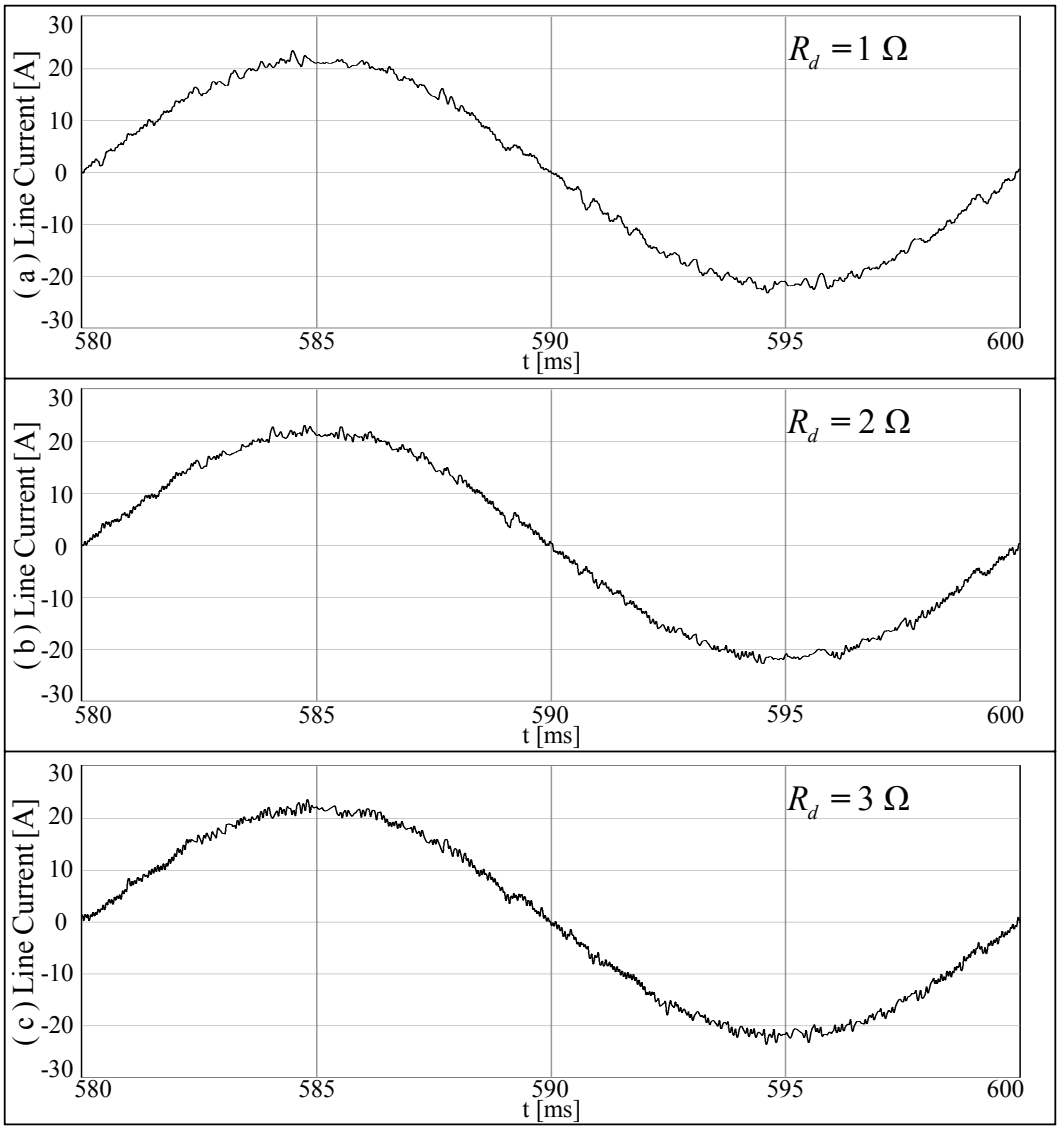

Figure 5.26 Line current waveform of the PAF utilizing DHCR3 with the high-pass RC type SRF for C_F = 30 μF and R_d values: a) R_d = 1 Ω, b) R_d = 2 Ω, and c) R_d = 3 Ω.

Table 5.14 THD performance of the PAF utilizing DHCR3 without and with the high-pass RC type SRF

	THD_I (%)	THD_V (%)
Without SRF	7.6	5.1
With SRF	4.2	1.5

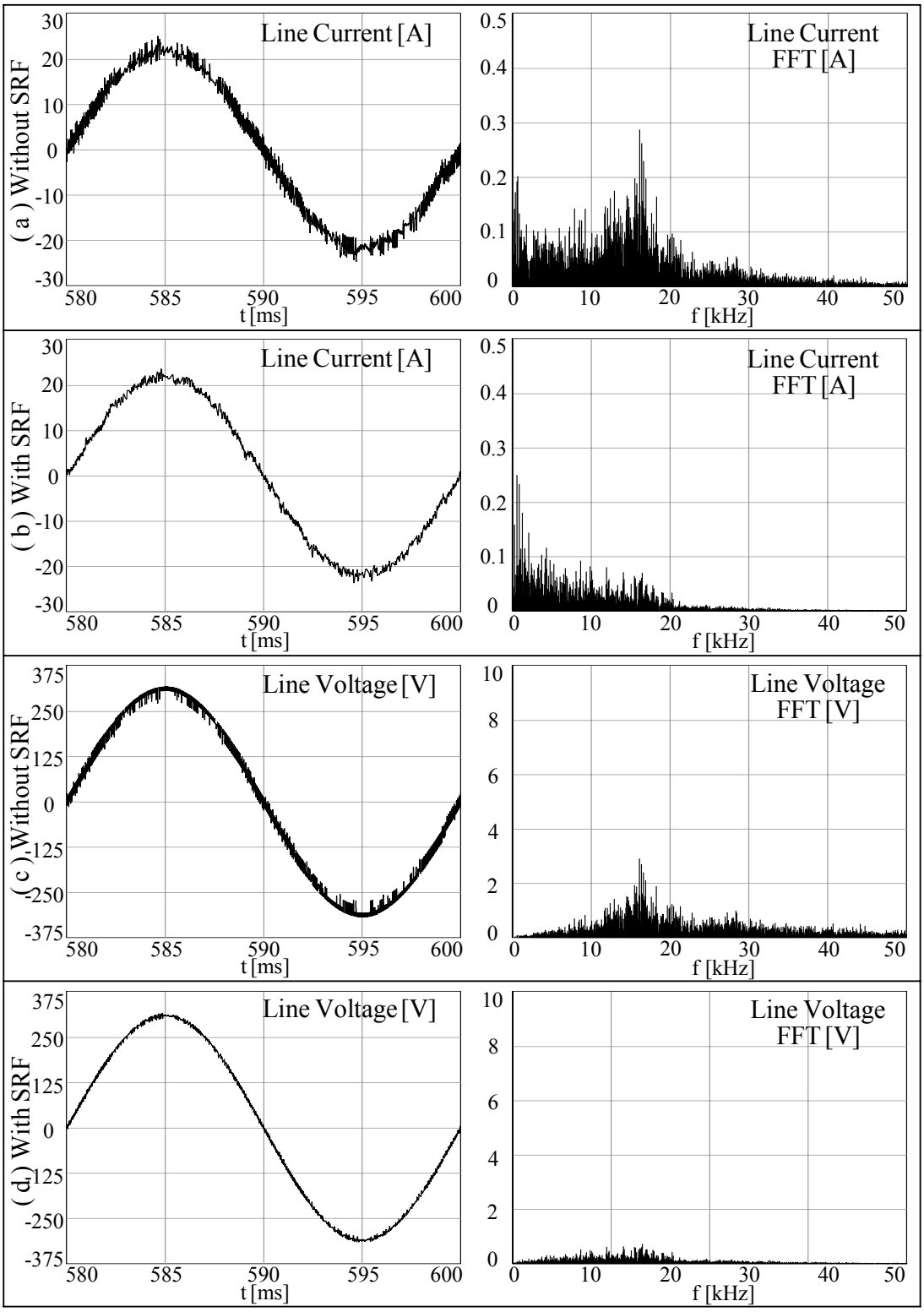

Figure 5.27 Line current, line voltage and their FTTs of the PAF utilizing DHCR3 without and with the high-pass RC type SRF.

5.6 Illustration of The Detailed PAF Performance

This section illustrates the detailed PAF performance since the current regulator choice and the performance analysis of the designed SRF for both the linear and on-off current regulators is completed in the previous sections. Although the high performance current regulators in the discrete time application of the PAF are determined in Section 5.4, this section first discusses the PAF performance with the designed SRFs for various current regulators to provide full analysis of the current regulators in the PAF application. Then the steady-state performance of the PAF will be illustrated for the improved DHCR3, where the PAF includes the designed high-pass RC type SRF. Moreover, the steady-state performance of the RFCR with superior THD_I performance will also be included in this section. Finally, the dynamic response of the PAF when it starts the harmonic compensation will be analyzed and the response characteristics of the PAF will be illustrated.

5.6.1 Performance Comparison of The Current Regulators with The Designed SRFs by Means of Computer Simulation

This section analyzes computer simulation results of the current regulators discussed when the SRF is included in the PAF system. Since the THD_I and THD_V values for the current regulators in Table 5.11 include the switching frequency harmonic currents and voltages, their values are high. When the SRF is included in the PAF system, the switching frequency harmonics are eliminated, so the performance of the current regulators by means of computer simulation get closer to the performance of current regulators obtained in experimental studies which will be discussed in the next chapter. Because, practical power quality analyzers calculate the THD_I and THD_V values based on the harmonic percentages up to a defined harmonic order such as up to 50^{th} order or 100^{th} order. With the inclusion of the SRF in the system in the computer simulation environment, the effect of high frequency components on the THD_I and THD_V values will be eliminated. Therefore the contribution of low frequency harmonics to THD_I and THD_V values will be observed in computer

simulation and the consistency of computer simulation results with experimental results will be provided.

The SRF topology differs based on the type of the current regulator utilized in the PAF system since the different class of current regulators creates different harmonic spectrums as discussed in Chapter 4 and previous section. The designed tuned LCR type SRF is utilized for all linear current regulators, and the designed high-pass RC type SRF is utilized for all on-off current regulators in this section. Table 5.15 summarizes the computer simulation results of the current regulators with SRF. Table 5.15 includes the harmonic components of the line current up to 50^{th} harmonics order, THD_I value of line current, THD_V value of line voltage, and PF at PCC, and IEEE limits for these quantities. The percentage of the harmonic components is nearly same with the inclusion of the SRF to the system, and can be compared to Table 5.11. The noticeable changes are in THD_I and THD_V values of current regulators with the SRF inclusion. Therefore, to provide a better comparison, Table 5.16 provides computer simulations results of current regulator with and without SRF by only including THD_I, THD_V, PF and f_{AVG} values. Based on Table 5.16, all current regulators THD_I and THD_V performances except the DHCR1 are improved with the SRF. The THD_I and THD_V values of the LPCR are enhanced from 5.1% and 3.8% to 4.1% and 0.8% respectively. Similarly, the improvements for other current regulators can be followed from Table 5.16. The reason that there exists no improvement in the THD_I performance of the DHCR1 is that the cut-off frequency of the RC type filter is above the frequency at which the switching harmonic exists for DHCR1. Based on Table 5.16, the AHCR illustrates the best THD_I performance as expected. Among the current regulators applicable in discrete time, the RFCR performance is the best. However, the most important conclusion with Table 5.16, the THD_I performances of LPCR and DHCR3 are nearly same with THD_I values of 4.1% and 4.2% respectively. This illustrates that DHCR3 is compatible with practically utilized the LPCR in terms of THD_I performance with the inclusion of the SRF. Moreover, when the f_{AVG} of the LPCR and the DHCR3 are compared, f_{AVG} of DHCR3 is 25% less than that of the LPCR. This means that DHCR3 provides nearly same THD_I performance compared to LPCR with a lower number of switching. It

should be remembered that the maximum allowable switching frequency of 20 kHz is equal for all current regulators. When the THD_V performance of the two current regulators are compared, the DHCR3 has a higher THD_V value of 1.5% compared to the LPCR THD_V value of 0.8% when the SRF is included to the PAF system. The reason is that although SRF is included to eliminate high frequency switching, the high-pass RC type SRF utilized in hysteresis current regulators does not totally eliminate the switching ripples spreading over a wide frequency range. This reflects on the THD_V value for the DHCRs in the computer simulation environment. However, the THD_V values for both current regulators; LPCR and DHCR3, are well below the IEEE 519 limit of 5% with the inclusion of the SRF. The performance enhancement for the DHCR2 is also noticeable from Table 5.16. The THD_I and THD_V values are enhanced from 10.4% and 5.1% to 7.6% and 1.9% respectively. As mentioned earlier, no improvement exists with DHCR1 due to switching harmonics that DHCR1 creates. This is also another illustration of poor performance of the DHCR1, conventional discrete time hysteresis current regulator. The PF values for all current regulators except DHCR1 are unity and slightly improved with the inclusion of the SRF to PAF system.

This subsection provides the performance analysis and comparison of current regulators discussed previously with the inclusion of the SRF in the PAF system and completes the discussion of the current regulator performances in the PAF application. Among the discrete time applicable current regulators, the THD_I performance of the RFCR is superior compared to others; LPCR, DHCR1, DHCR2 and DHCR3, and THD_I performance of improved discrete time current regulator DHCR3 with 25% lower switchings is compatible with practically utilized LPCR in PAF application. This discussion can be concluded as the RFCR among the discrete time applicable linear current regulators and the DHCR3 among the discrete time applicable hysteresis current regulators illustrate superior THD_I performance. Although, THD_I of 4.2% for the DHCR3 is high compared to the THD_I value of 2.1% for the RFCR, the DHCR3 is favorable in terms of the f_{AVG} and the implementation simplicity compared to the RFCR. From now on, the performance of the PAF will be based on these two regulators.

Table 5.15 Computer simulation results of line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for all the simulated current regulators and IEEE 519 limits with SRF

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%) LPCR	Line Current Harmonics with PAF (%) CECR	Line Current Harmonics with PAF (%) RFCR	Line Current Harmonics with PAF (%) AHCR	Line Current Harmonics with PAF (%) DHCR1	Line Current Harmonics with PAF (%) DCHR2	Line Current Harmonics with PAF (%) DHCR3	IEEE 519 Harmonic Current Limits (I_{SC}/I_{L1}=173) (%)
I_1	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
I_5	30.0	2.5	1.4	0.3	1.1	3.7	0.9	0.7	12.0
I_7	9.0	0.9	0.4	0.3	0.1	1.5	1.5	0.3	12.0
I_{11}	7.0	1.3	0.7	0.1	0.4	4.0	1.4	1.1	5.5
I_{13}	3.7	0.8	0.4	0.1	0.2	1.0	1.0	0.3	5.5
I_{17}	3.0	1.0	0.5	0.1	0.3	1.6	1.4	1.1	5.0
I_{19}	2.2	0.6	0.3	0.1	0.2	3.7	1.1	0.4	5.0
I_{23}	1.4	0.6	0.3	0.5	0.3	4.4	0.4	0.3	2.0
I_{25}	1.3	0.5	0.3	0.5	0.2	5.8	1.1	0.8	2.0
I_{29}	0.8	0.5	0.2	0.3	0.2	4.4	0.4	0.4	2.0
I_{31}	0.7	0.4	0.2	0.4	0.1	3.1	0.2	0.5	2.0
I_{35}	0.5	0.5	0.2	0.4	0.2	4.8	0.5	0.2	1.0
I_{37}	0.5	0.4	0.2	0.3	0.1	3.8	0.8	0.3	1.0
I_{41}	0.4	0.5	0.2	0.3	0.2	3.5	0.5	0.7	1.0
I_{43}	0.4	0.3	0.2	0.3	0.1	2.6	0.8	0.2	1.0
I_{47}	0.3	0.4	0.2	0.3	0.1	1.7	0.6	0.3	1.0
I_{49}	0.3	0.3	0.2	0.3	0.1	3.7	1.2	0.4	1.0
THD_I(%)	32.6	4.1	2.6	2.1	1.4	31.1	7.6	4.2	15.0
THD_V(%)	0.5	0.8	0.9	0.8	0.5	4.6	1.9	1.5	5.0
PF	0.930	0.998	0.999	0.999	0.999	0.953	0.997	0.999	---
f_{AVG}(kHz)		13.3	13.3	13.3	28.6	3.8	7.8	10.0	

Table 5.16 PAF system performance computer simulation results for various current regulators with SRF and without SRF

		without SRF			with SRF			
	CR Type	THD_I (%)	THD_V (%)	PF	THD_I (%)	THD_V (%)	PF	f_{avg} (kHz)
Load Current		32.6	0.5	0.93	32.6	0.5	0.93	
Line Current	LPCR	5.1	3.8	0.998	4.1	0.8	0.998	13.3
	CECR	3.9	3.8	0.998	2.6	0.9	0.999	13.3
	RFCR	3.1	3.8	0.998	2.2	0.8	0.999	13.3
	AHCR	2.5	3.5	0.998	1.4	0.5	0.999	28.6
	DHCR1	30.4	5.0	0.955	31.1	4.6	0.953	2.8
	DHCR2	10.4	5.1	0.993	7.6	1.9	0.997	7.8
	DHCR3	7.6	5.1	0.996	4.2	1.5	0.999	10.0
IEEE 519 Limits		15.0	5.0		15.0	5.0		

5.6.2 The PAF Steady-state Performance

In this subsection, the steady-state performance of the PAF with the designed SRF will be illustrated for the two high performance current regulators; the DHCR3 and the RFCR. The THD_I, THD_V, PF, and f_{AVG} performances of both current regulators were given in the previous subsection. Therefore, they will not be analyzed here. Only the steady-state waveforms and the power rating of the PAF will be presented.

Figure 5.28 respectively illustrates the voltage at the PCC (line voltage), the line current, the load current, the PAF current, the SRF current for 'phase *a,*' and the DC bus voltage waveforms of the PAF system that utilizes the DHCR3 and the designed high-pass RC type SRF and compensates harmonics and reactive current component of diode rectifier load with the output power rating of 10 kW. The line current waveform in Figure 5.28 is nearly sinusoidal with THD_I value of 4.2%, which

illustrates that PAF system performs the harmonic current compensation of the harmonics current source type nonlinear load and in phase with the line voltage with PF value of 0.999, which illustrates the reactive power compensation capability of the PAF. The switching ripple current is eliminated from the line current via the SRF. As a result, there exists no high frequency distortion on the line voltage waveform. The switching ripple current waveform also illustrates that the SRF sinks the high frequency switching ripple currents that the PAF creates. Further, the DC average bus voltage of PAF is at its reference voltage 700 V with a nearly 5 V peak to peak 300 Hz ripple due to the dominant 5^{th} and 7^{th} harmonic current components existing in the filter current. The detailed illustration of the line current, the PAF current reference and the PAF current is provided in Figure 5.29 for the PAF system with the designed high-pass RC type SRF and the DHCR3. The line current harmonic spectrum in Figure 5.30 is included to provide a visualization of the harmonic content of the line current over a wide frequency range. The line current becomes harmonic current free and switching ripple current free in the presence of the PAF with an appropriate SRF.

Figure 5.31 respectively illustrates the voltage at the PCC (line voltage), the line current, the load current, the PAF current, the SRF current for 'phase *a,*' and the DC bus voltage waveforms of PAF system that utilizes the RFCR and the designed tuned LCR type SRF and compensates harmonics and reactive current component of diode rectifier load with the output power rating of 10 kW as in the DHCR3 case. The line current waveform in Figure 5.31 is nearly sinusoidal with THD_I value of 2.1% and in phase with the line voltage with PF value of 0.999. The high frequency switching distortions on the line voltage and current due to utilization of the designed tuned LCR type SRF for the RFCR. The DC average bus voltage of the PAF is at its reference voltage 700 V with a nearly 5 V peak to peak 300 Hz as in the DHCR3 case. The detailed illustration of the line current, the PAF current reference and the PAF current are illustrated in Figure 5.32 for the PAF system with the designed tuned LCR type SRF and the RFCR. The line current harmonic spectrum in Figure 5.33 over a wide frequency range presents a visualization of the harmonic content of the line current, and proves the well defined harmonic spectrum for the linear current

regulators. The low frequency harmonic content is considerably eliminated by the PAF, while the dominant switching ripple current of the line current at 20 kHz is eliminated with the designed tuned LCR type SRF for linear current regulators.

Table 5.17 presents the steady-state power flow data for the load current, line current, PAF current, and SRF current and the line voltage in magnitude, the input power rating of the diode rectifier load with the output power rating of 10 kW (load power), the power drawn from the AC utility grid (line power), and the power rating of the PAF (filter power) for the DHCR3 and RFCR. While the load power and the line power for both regulators are same as expected, the filter rating in kVA differs. The power rating of the PAF system utilizing the DHCR3 is less than the PAF system utilizing RFCR since the SRF differs in type for both current regulators. While the PAF system with DHCR3 utilizes high-pass RC type SRF with C_F=30 μF, the PAF system with RFCR utilizes tuned LCR type SRF with C_F=2.2 μF. Since the C_F for the high-pass RC type is greater in size compared to the C_F for the tuned LCR type, the C_F for the high-pass RC type provides much more reactive power to the system, thus reducing the VA rating of the PAF, compared to the C_F for the tuned LCR type. As a result, VA rating of the PAF with DHCR3 and high-pass RC type SRF is less than the PAF system with RFCR and tuned LCR type SRF. This also illustrates the reduction of the PAF VA rating with the passive elements.

This section involved the detailed steady-state performance illustration of the PAF system for two superior current regulators in PAF application; DHCR3 and RFCR, to provide a better a visualization and comparison. The next subsection investigates the dynamic response of the PAF system with DHCR3. The start-up dynamics of the harmonic compensator and the transients during load (output power) change are investigated for the diode rectifier type nonlinear load studied in throughout the simulations.

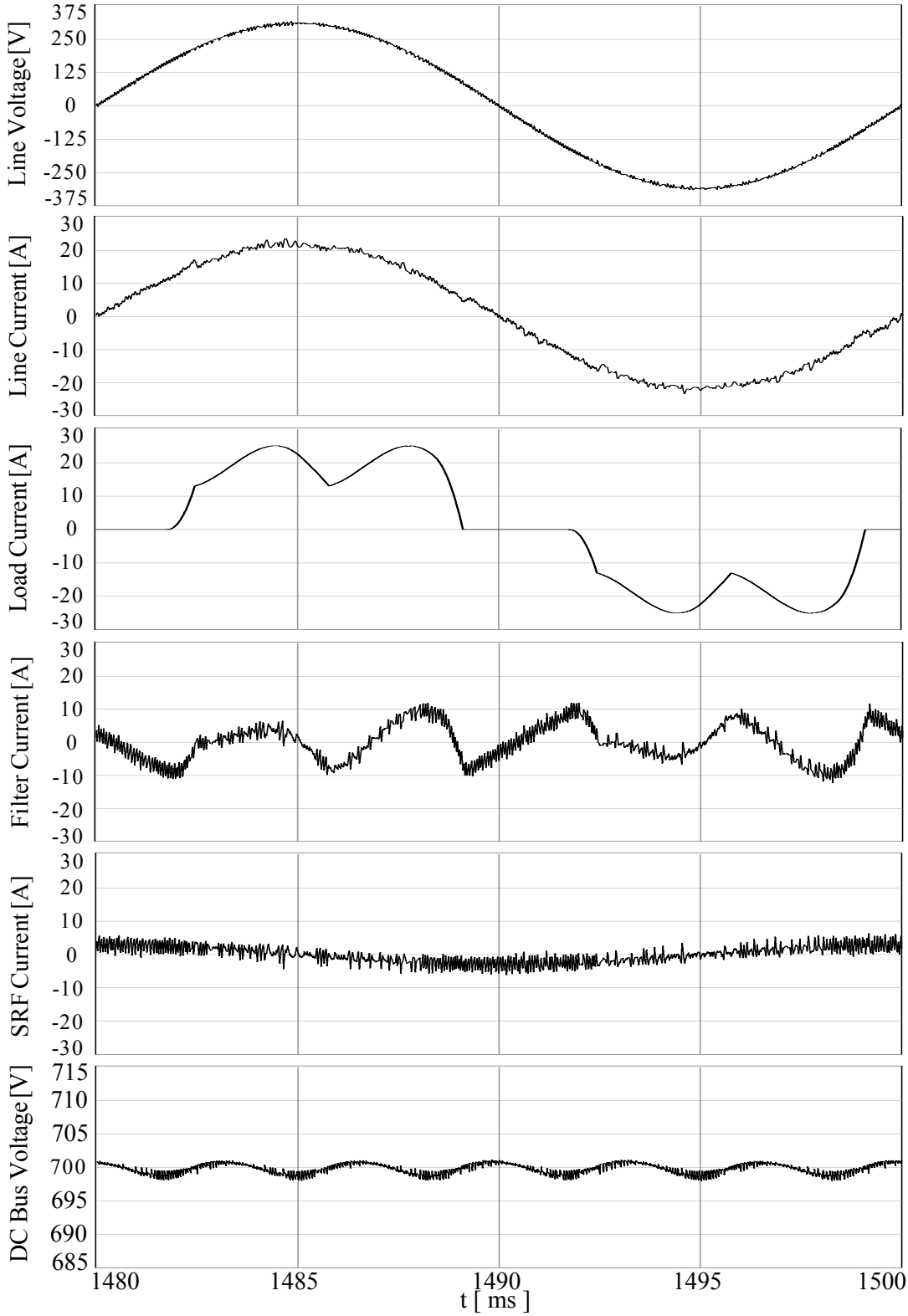

Figure 5.28 Steady-state waveforms over a fundamental cycle illustrating the detailed performance of the PAF utilizing the DHCR3 with the high-pass RC type SRF: The voltage at the PCC, line current, load current, PAF current, SRF current waveforms for 'phase *a,*' and the DC bus voltage.

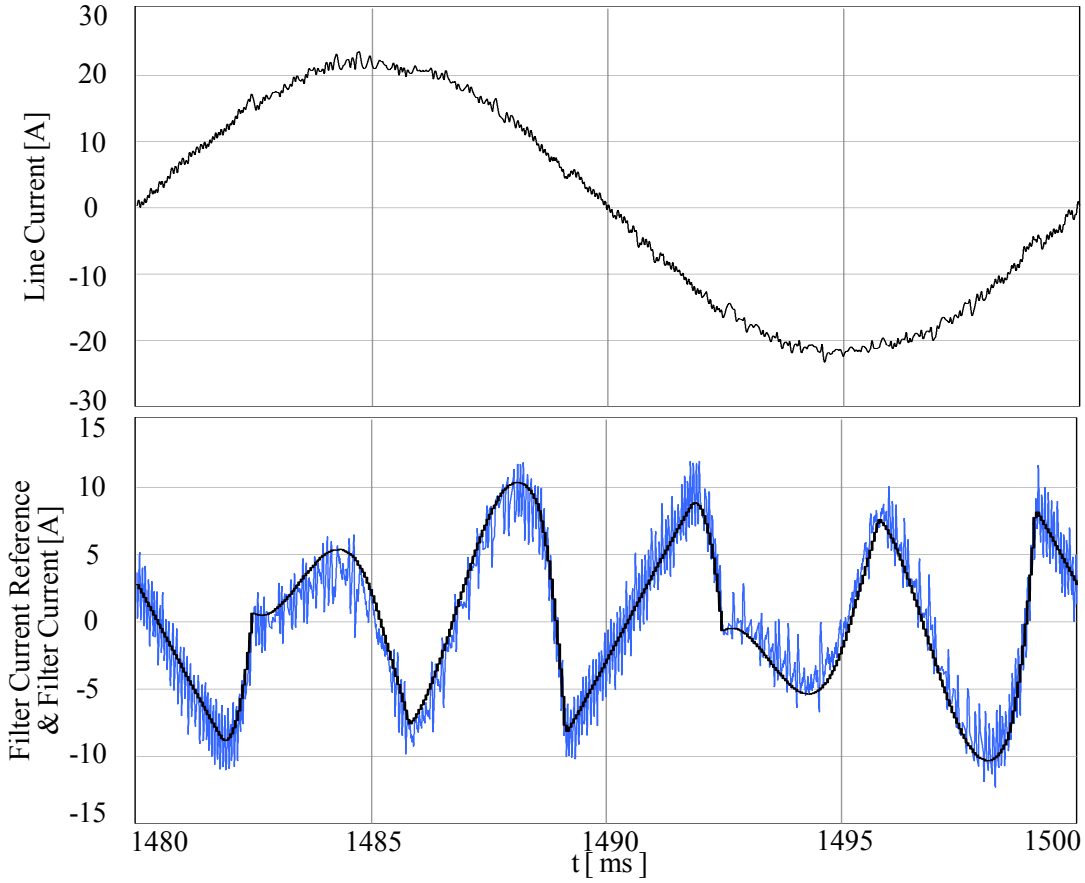

Figure 5.29 Steady-state line current, filter current reference (black) and filter current (blue) over a fundamental cycle for the DHCR3 with SRF.

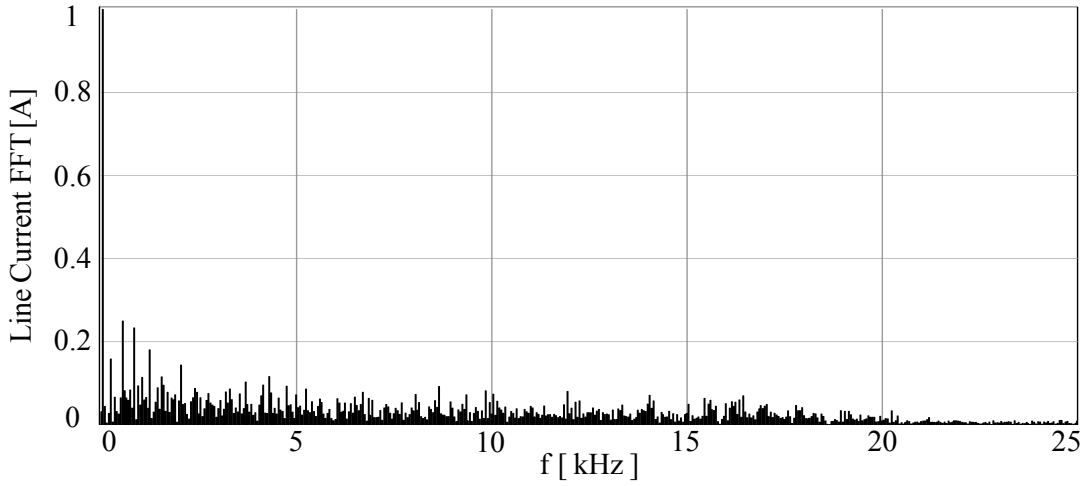

Figure 5.30 Steady-state line current harmonic spectrum for the DHCR3 with SRF.

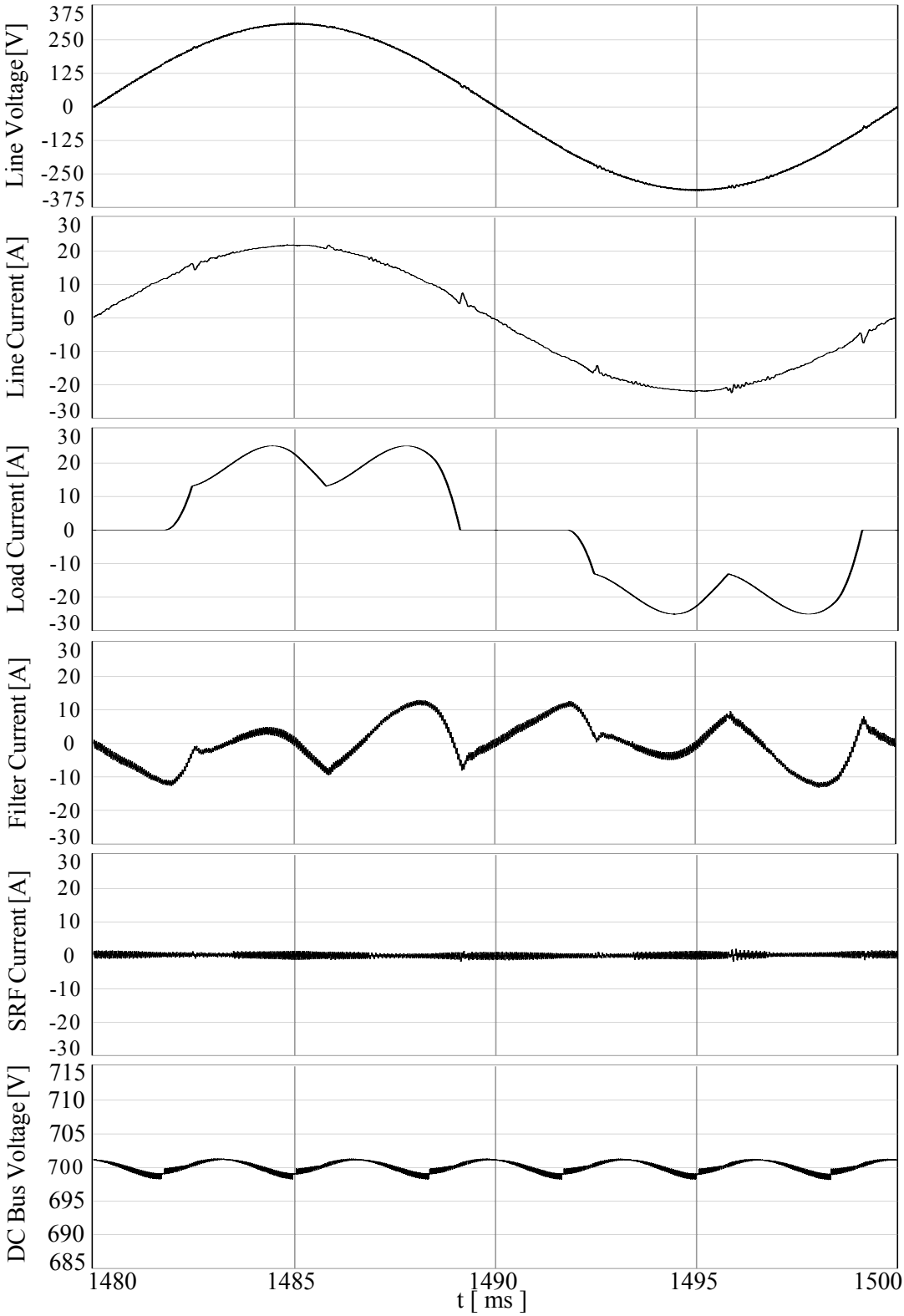

Figure 5.31 Steady-state waveforms over a fundamental cycle illustrating the detailed performance of the PAF utilizing the RFCR with the tuned LCR type SRF: The voltage at the PCC, line current, load current, PAF current, SRF current waveforms for 'phase *a,*' and the DC bus voltage.

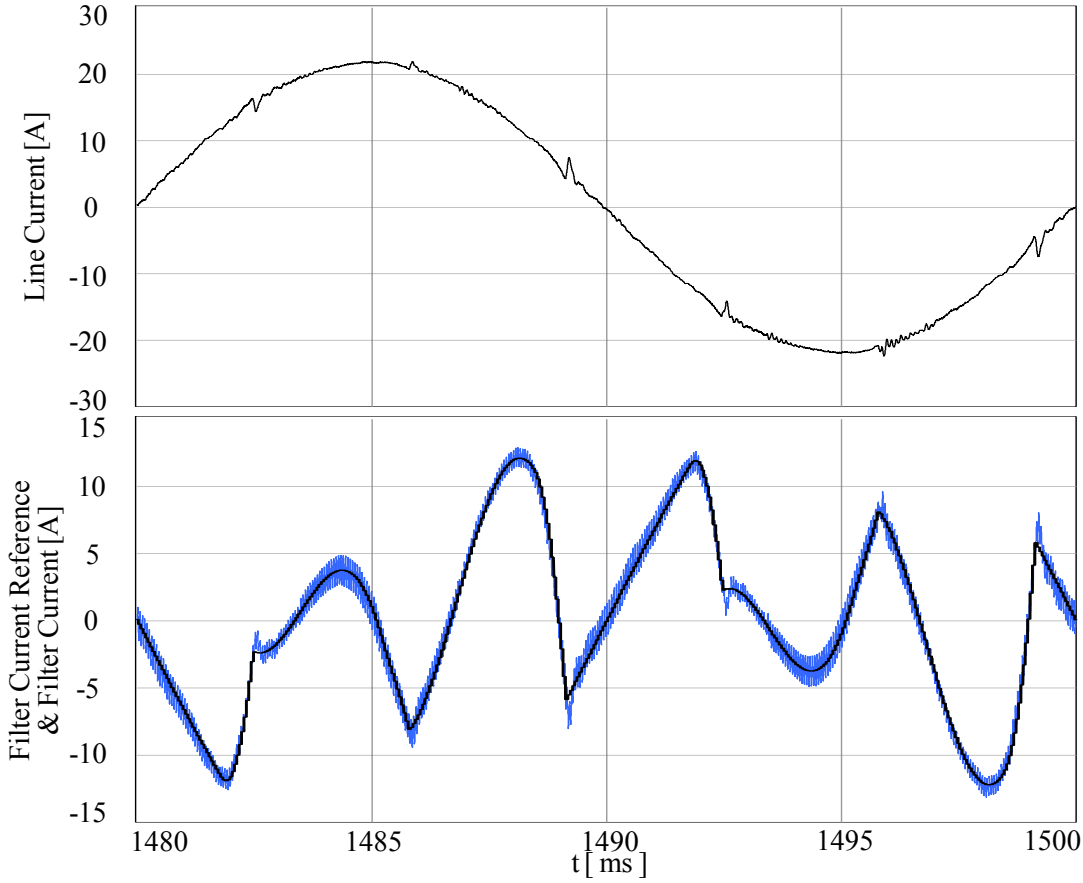

Figure 5.32 Steady-state line current, filter current reference (black) and filter current (blue) over a fundamental cycle for the RFCR with SRF.

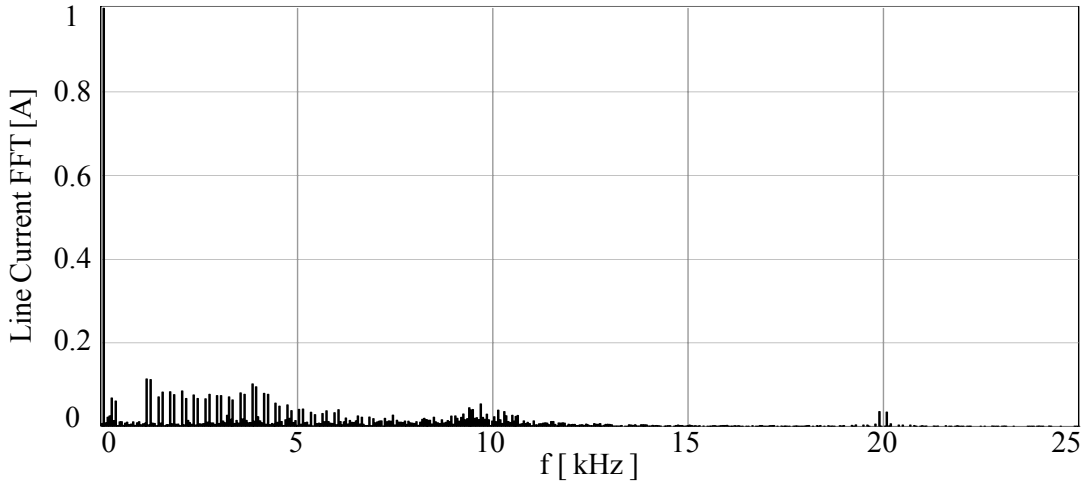

Figure 5.33 Steady-state line current harmonic spectrum for the RFCR with SRF.

Table 5.17 Steady-state power flow data for the AC utility grid, diode rectifier load and the PAF system with DHCR3 and RFCR

	Load current/phase (Arms)	Line current/phase (Arms)	Filter current/phase (Arms	SRF current/phase (Arms)	Line Voltage/phase (Vms)	Load Power (kVA) (PF=0.930)	Line Power (kVA) (PF=0.999)	Filter Power (kVA)
DHCR3	16.5	15.5	5.4	2.4	220	10.9	10.2	3.6
RFCR	16.5	15.5	6.3	0.6	220	10.9	10.2	4.2

5.6.3 The PAF Dynamic Performance

The dynamic response of the PAF system means the performance of the system under the changes in operating conditions involving the start-up of the harmonic compensation of the nonlinear load or output power demand of the nonlinear load changes. The behavior of the PAF system under such conditions illustrates the performance of each controller involved in the PAF control algorithm. This subsection investigates the performance of the designed controllers by introducing disturbances to the PAF which waits for the harmonic compensation of the defined nonlinear load. The studies will only be illustrated for the DHCR3 and as the results for other regulators are practically the same, they will not be repeated.

The behavior of the PAF system when it start the harmonic compensation of the nonlinear load operating at the rated output power of 10 kW is the first dynamic performance study. Figure 5.34 illustrates the system waveforms of line voltage at the PCC, line current, load current, filter current, and DC bus voltage of the PAF system when it starts the harmonic compensation of the nonlinear load operating at the rated output power of 10 kW. Figure 5.35 is the detailed illustration of Figure 5.34 at the instant of the harmonic compensation start including the waveform of the filter current reference. Just after the PAF system receives the harmonic compensation command at t = 1 s while its DC bus voltage is at its rated value of 700

V, the line current becomes sinusoidal and in phase with the line voltage. The PAF system tracks its reference current properly and the settling time of the line current to its sinusoidal shape is nearly zero since the current reference from the harmonic current reference generator is ready in the control algorithm of the PAF. The bus voltage of the PAF system is nearly constant. This study is a realistic study such that in practice, first the DC bus voltage of the PAF system is brought to its reference value while the control algorithm detects the load current and creates the current reference, and then the filter starts the harmonic and/or the reactive power compensation of the nonlinear load. The PAF system behavior under such a realistic case is as expected. However, with the case study discussed above, the performance of the harmonic reference generator block can not be observed properly since the block output signal is at its steady-state value. In order to observe the response of the block while the change in DC bus voltage, the nonlinear load is brought from 0% loading to the 75% loading suddenly meanwhile the PAF system has received the harmonic compensation start command. Figure 5.36 illustrates the waveforms of the system for the above mentioned case study. Moreover, the zoom out of Figure 5.36 around the loading instant is illustrated in Figure 5.37 including the current reference signal. The harmonic reference generator output is zero since the load current is zero up to the instant of the loading. Just after loading, the output of the harmonic reference generator can not be brought to its steady-state value immediately due to the low cut-off frequency of the LPF utilized in the harmonic reference generator block. Therefore the line current gradually increases to its rated value following a sinusoidal shape based on the setting time of the LPFs. The settling time with the harmonic reference generator block utilizing two cascaded LPFs with the cut-off frequency of 20 Hz is around 80 ms from Figure 5.36. Moreover, since the LPF strategy is utilized for harmonic current extraction due to its zero magnitude and phase error at the steady-state, the output of the harmonic reference generator block is the load current. Therefore, the PAF operated in current control mode meets the load real power demand, which results in a DC voltage drop of nearly 50 V at the DC bus of the PAF. However, since the PAF is also designed to regulate its DC bus voltage, the DC bus voltage increases gradually to its reference value making an overshoot at around 400 ms based on the DC bus voltage regulator control bandwidth.

The overshoot of the DC bus voltage is unavoidable since the measured DC voltage for the regulation is passed trough a LPF with the cut-off frequency of 50 Hz for the magnitude reduction of the 300 Hz ripple content on the DC bus voltage as discussed in Chapter 2. The response of the DC bus voltage regulator can be increased by increasing the gains of the DC bus voltage regulator, which utilizes the proportional gain (K_P) of 0.05 and the integral gain (K_I) of 0.5. Although the utilization of the higher gains for the DC bus voltage regulator is possible in computer simulation environment, the restriction comes from the experimental studies. The DC bus voltage regulator gains are experimentally adjusted due the noise problems with the higher gain values. The simulation utilizes the same gains for the DC bus voltage regulator as in the experiment in order to have consistency with simulation and experimental studies. From Figures 5.36 and 5.37, the DC bus voltage is brought above the reference value of 700 V at around 100 ms and it settles down to its reference value at around 400 ms.

Another case study to investigate the dynamic performance of the PAF system is the response of the PAF under the case of the output power of the nonlinear load is brought from 75% to 0% load suddenly while the PAF system is under operation. Figure 5.38 illustrates the system waveforms of line voltage at PCC, line current, load current, filter current, and DC bus voltage of the PAF system which encounters the change of the nonlinear load output power from its rated value of 7.5 kW to 0 kW while the PAF compensates the load current harmonics and reactive power component. Figure 5.39 is the detailed illustration of Figure 5.38 at the instant when the loading of the nonlinear load changes from 75% to 0%. The line current comes to nearly zero value at around 20 ms while it preserves its sinusoidal shape. The DC bus voltage encounters an overshoot of 50 V due to the real power transfer from the line since the harmonic reference generator gives a real power component due to the LPF structure in this case of the nonlinear load change from 75% to 0% (the reverse of the previous case study). The DC voltage regulator brings the DC bus voltage of the PAF system to its reference value of 700 V at around 400 ms by providing real power transfer to the AC utility grid system. If the PAF system encounters a load change from 100% to 0%, the overshot DC bus voltage will be higher than 50 V. In this case,

the overshoot protection voltage level of the system which has a limit of 780 V may be exceeded and the filter circuit breaker will turn off in order to protect the system. Since the experimental system will be explained in the next chapter has such a protection, the dynamic response case study of the nonlinear load from 75% to 0% is illustrated to provide a consistency with the experimental studies.

Among the three case studies analyzed above, the first one presents the normal operation condition the PAF system where the PAF system is started to operate when the harmonic reference command is ready. In such a case, the PAF starts its operation without any response delay. The last two cases illustrating different loading change of the nonlinear load to observe the response time of the reference signal generator block may take place in real life; however, the load change generally occurs gradually. Therefore, the dynamic response of the PAF system will not be worse than the one analyzed above.

In this section, the detailed PAF performance illustration for the harmonic and the reactive power compensation of the diode rectifier with a rated output power of 10 kW has been presented with the analysis of the all current regulators with the SRF, the steady-state performance of the PAF system for two superior current regulators of DHCR3 and RFCR in PAF application, and the dynamic response of the PAF system utilizing the DHCR3 for difference cases.

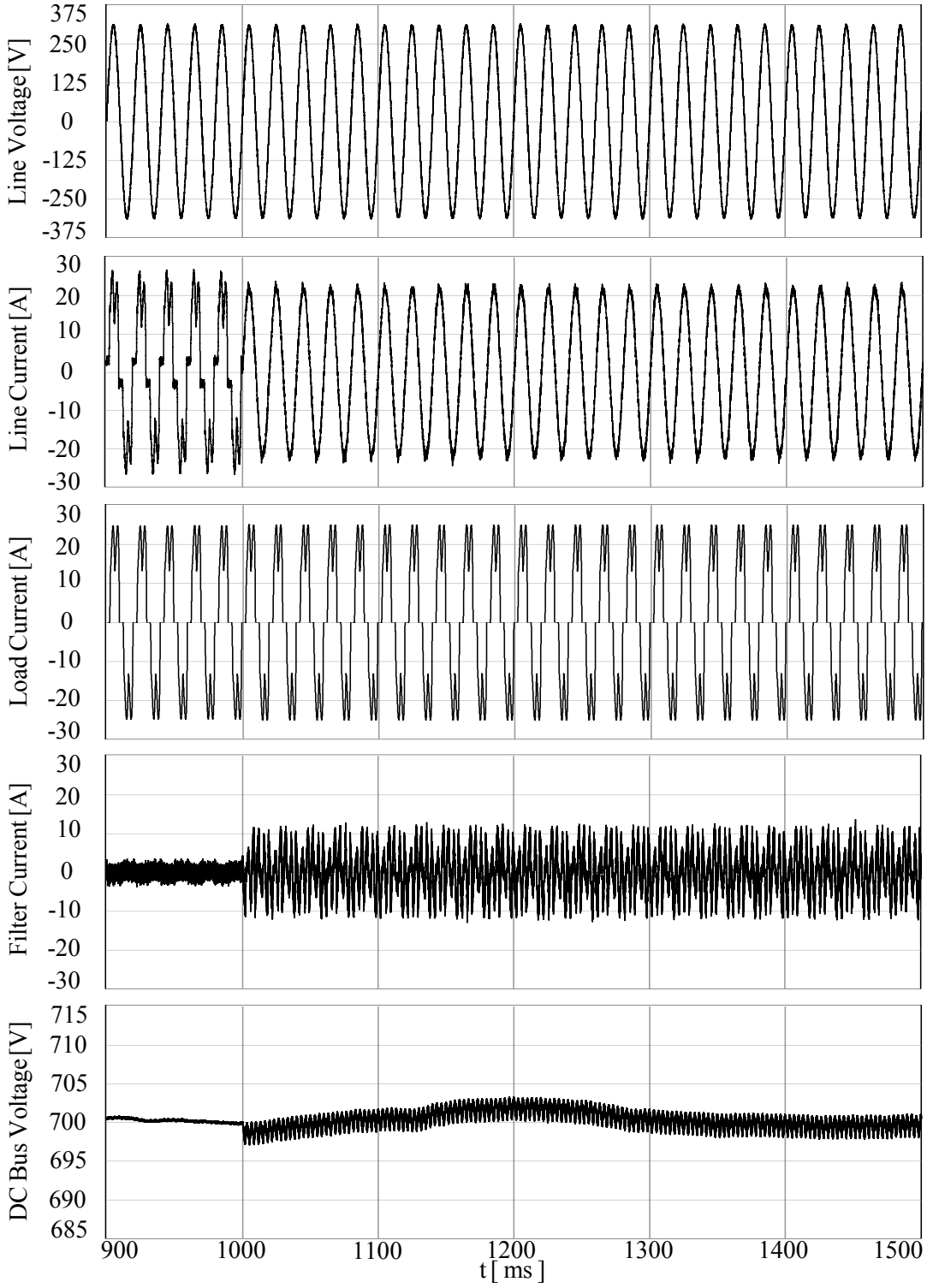

Figure 5.34 The waveforms of the PAF system utilizing DHCR3 when it starts the harmonic compensation of the diode rectifier load operating at the rated output power of 10 kW.

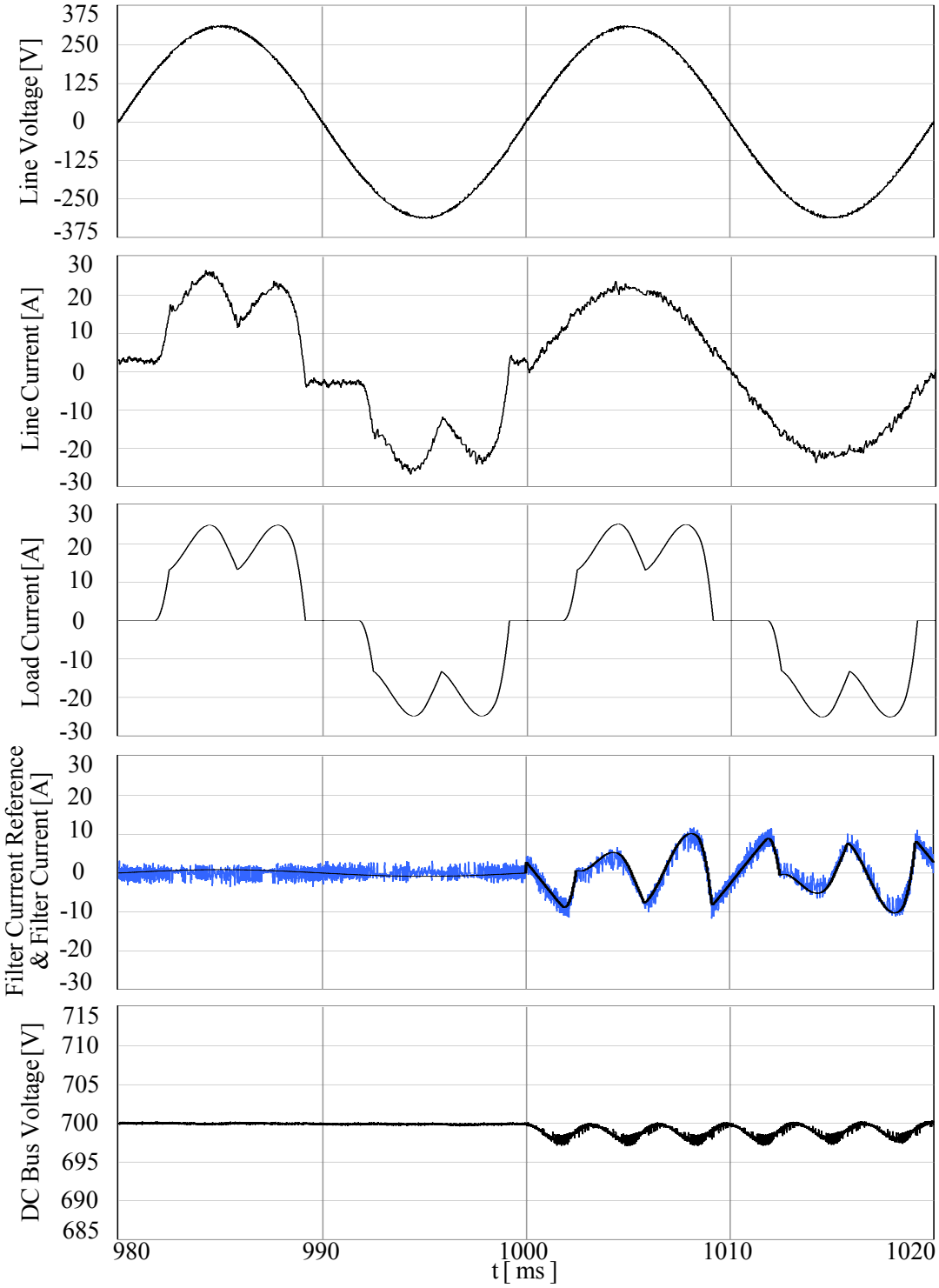

Figure 5.35 The detailed illustration of Figure 5.34 at the instant when the PAF starts the harmonic compensation.

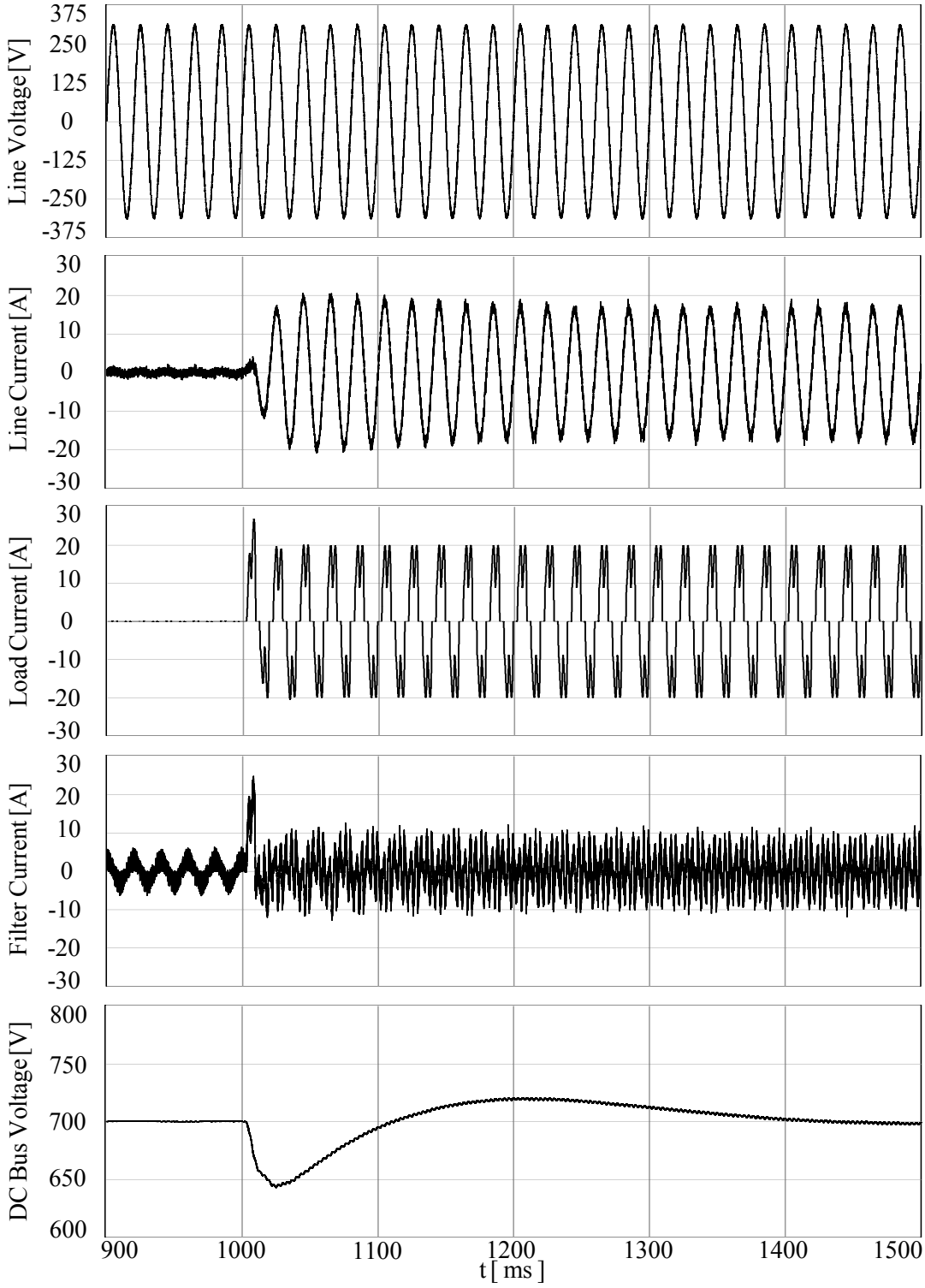

Figure 5.36 The waveforms of the PAF system with the DHCR3 illustrating its dynamic response when the diode rectifier load is brought from 0% loading to 75% loading suddenly.

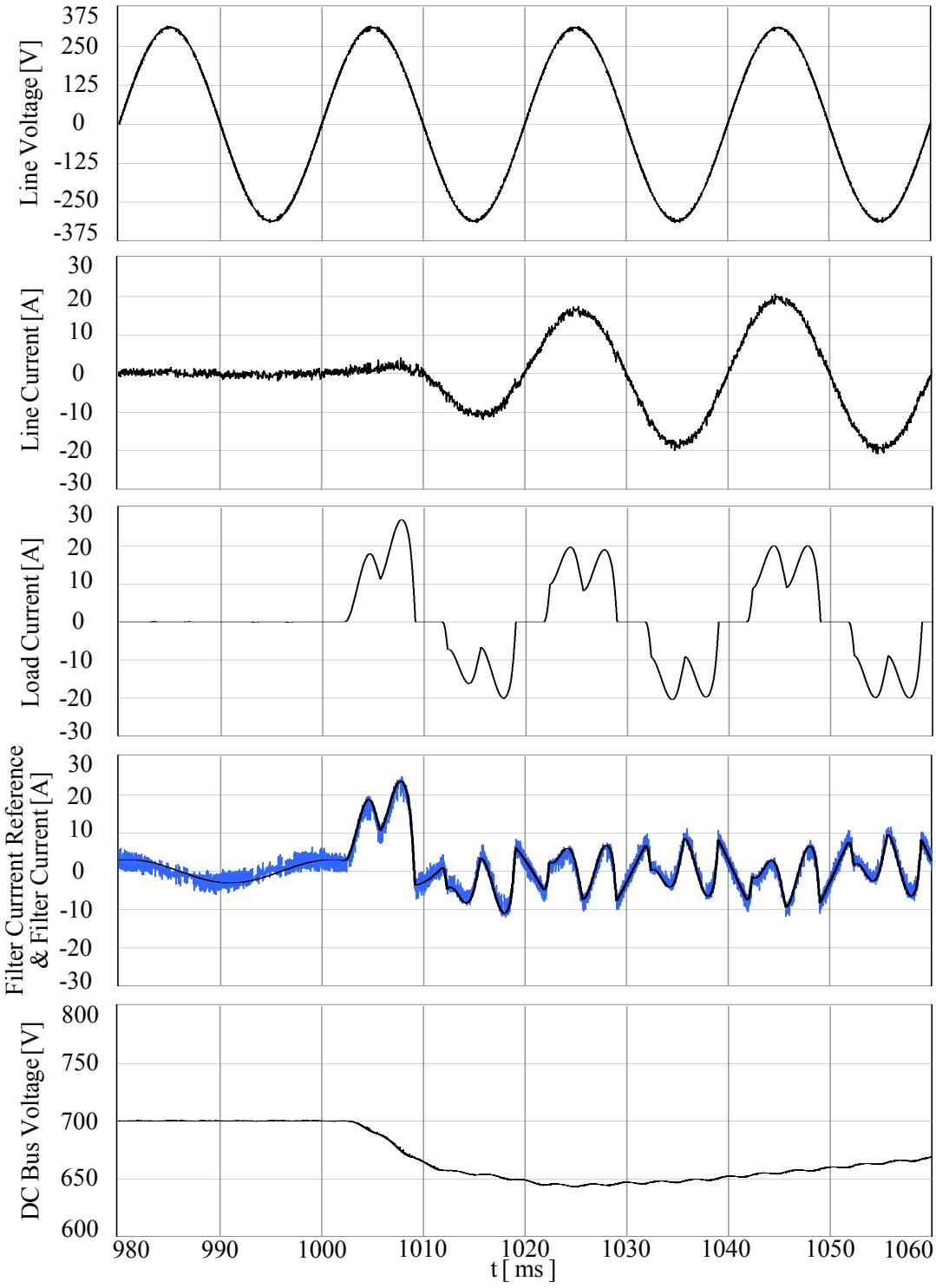

Figure 5.37 The detailed illustration of Figure 5.36 at the instant when the diode rectifier load is brought from 0% loading to 75% loading suddenly.

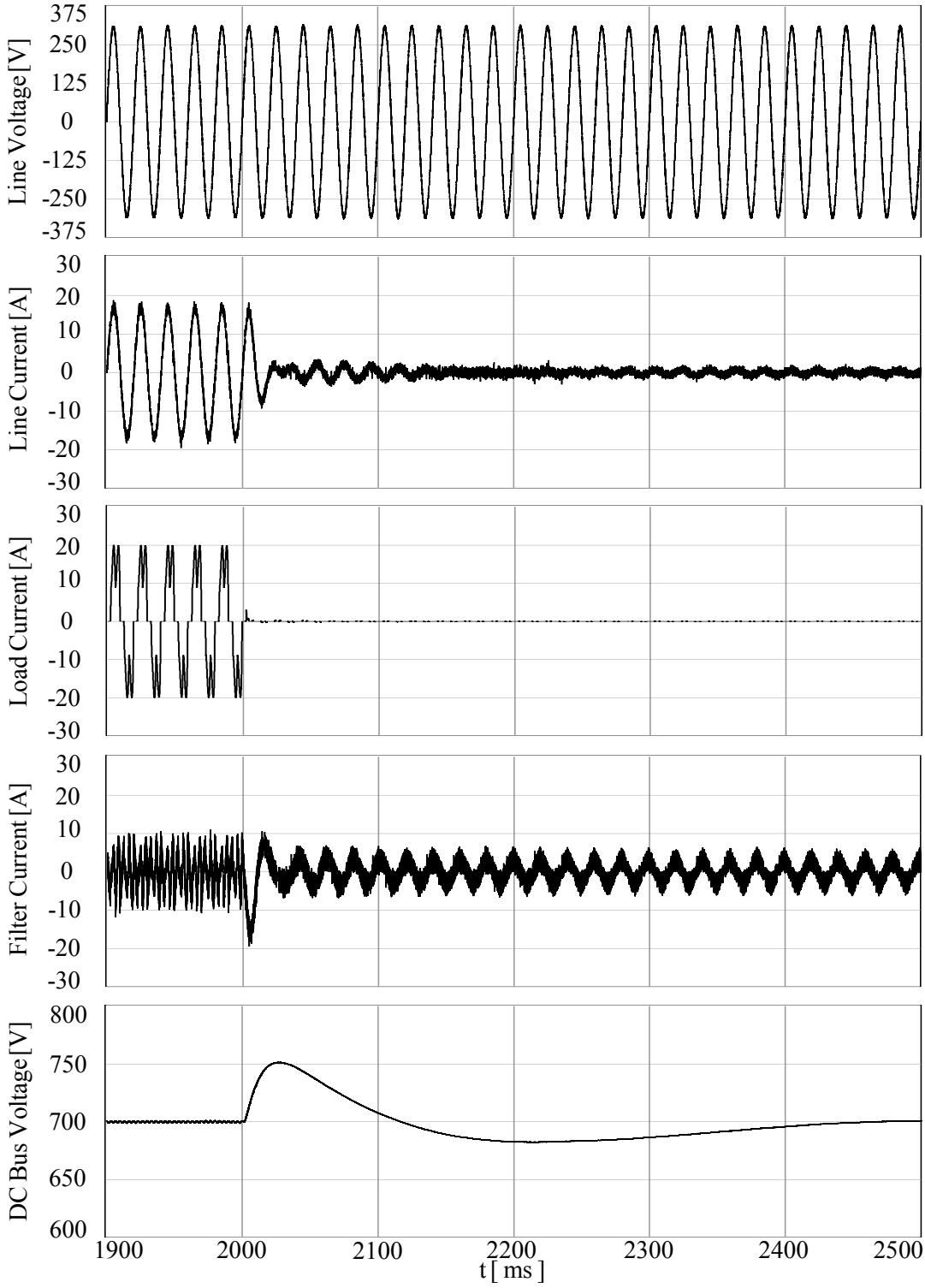

Figure 5.38 The waveforms for the PAF system with the DHCR3 illustrating its dynamic response when the diode rectifier load is brought from 75% loading to 0% loading suddenly.

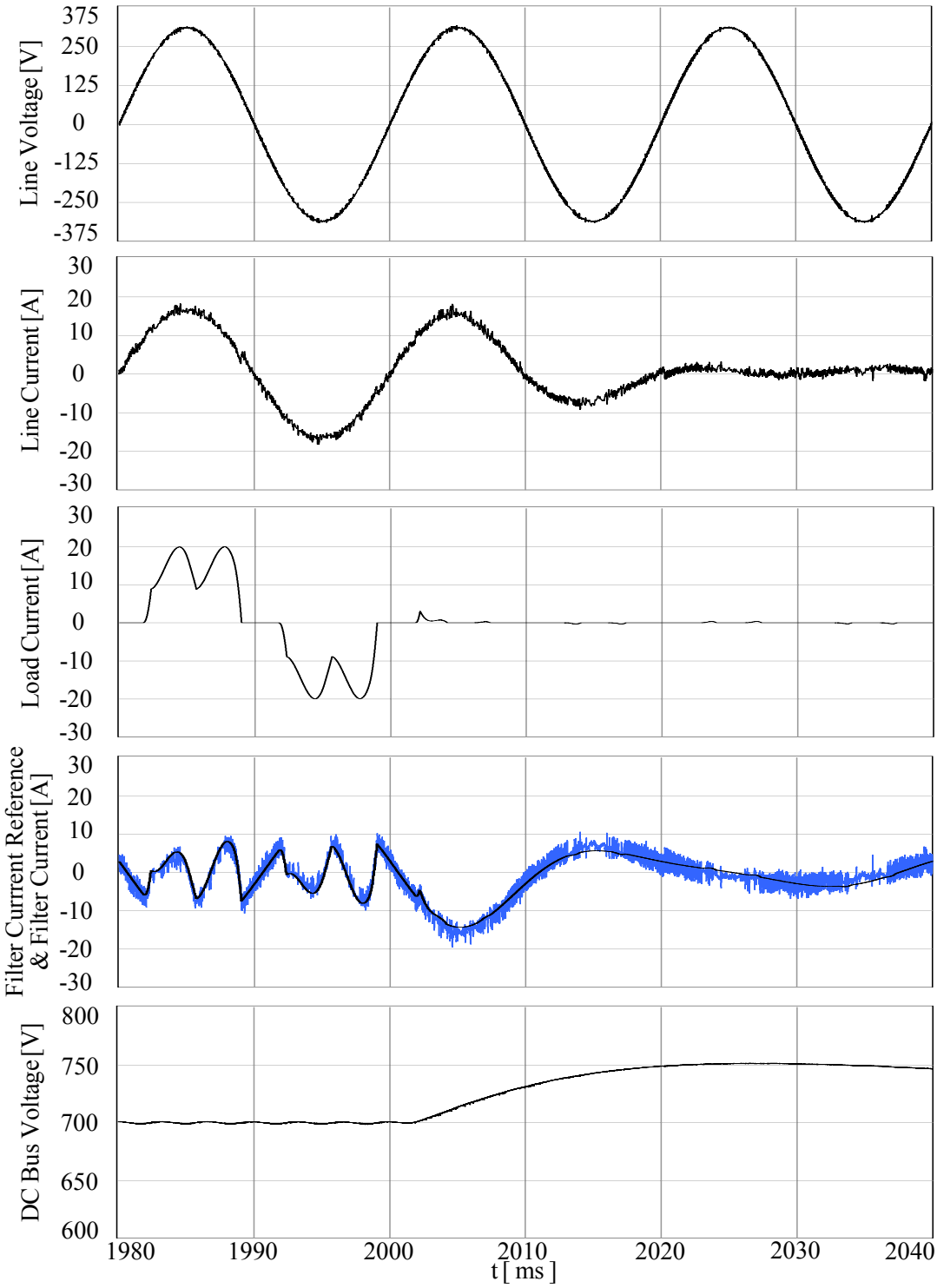

Figure 5.39 The detailed illustration of Figure 5.38 at the instant when the diode rectifier load is brought from 75% loading to 0% loading suddenly.

5.7 Performance Analysis of The PAF for The Thyristor Rectifier Load

The diode rectifier demands a small amount of reactive power at the fundamental frequency for the AC utility grid due to the AC side reactor. The reactive power demand of the nonlinear load can be increased by utilizing a thyristor rectifier such that the firing angle *a* can be adjusted based on the desired reactive power demand. Moreover, a negative sequence load current can be created via a thyristor by adjusting the firing angle value for each leg in the computer simulation environment. In this section the performance of the PAF for a thyristor rectifier load will be investigated to illustrate the reactive power and negative sequence current compensation capability of the PAF.

Figure 5.40 illustrates the single line diagram of the thyristor rectifier utilized in the computer simulation. The parameters of the thyristor rectifier are given Table 5.18. The AC utility grid and the PAF system parameters are the same as in the case of the diode rectifier load. When the thyristor rectifier is operated at the output power of 10 kW with a=0°, the commutation of the current from one phase to the other phase occurs at the instant of the corresponding line voltages have the same instantaneous value for a balanced three phase AC utility as in the case of a diode rectifier. Moreover, the thyristor rectifier with a=0° does not demand significant reactive power from the AC utility grid. Therefore, the behavior of the thyristor rectifier load with a=0° is not different from the diode rectifier load. The computer simulation waveforms for the AC utility grid, thyristor rectifier with a=0°, the PAF system will not be illustrated due to the similarity of the waveforms as in diode rectifier load. Only the basic results will be summarized in a table for the thyristor rectifier with a=0° and two superior current regulators of the DHCR3 and the RFCR. Then the performance of the PAF for the thyristor rectifier operation at an output power of 10 kW and the firing angle of 30°, which results in load PF value of 0.82, will be investigated. Finally the negative sequence compensation capability of the PAF will be illustrated for a case study involving the thyristor rectifier load.

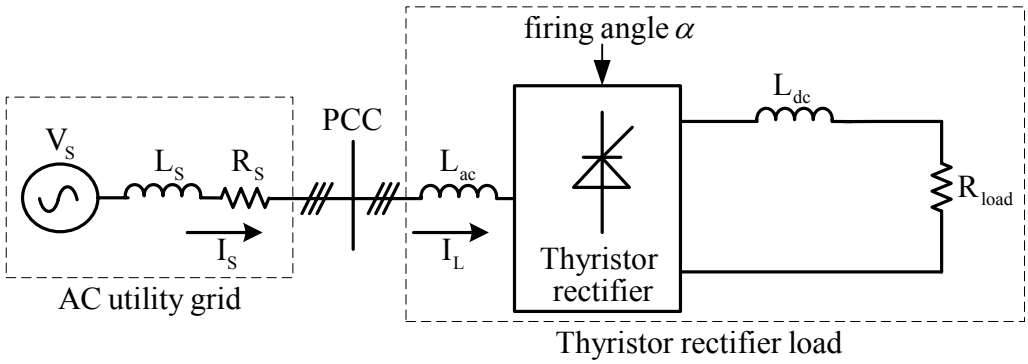

Figure 5.40 Single line diagram of the thyristor rectifier as nonlinear load in the PAF application.

Table 5.18 The thyristor rectifier parameters used in the computer simulation

	Parameter	Value
Thyristor rectifier load	L_{ac} (AC line reactor)	2 mH
	L_{dc} (DC Link inductor)	1.46 mH
	R_{load} (Load resistor)	25 Ω
	P_{load} (Load output power)	10 kW

5.7.1 The PAF Performance for The Thyristor Rectifier Load with *a*=0°

Table 5.19 summarizes the steady-state performance of the PAF which is connected in parallel to the thyristor rectifier operating at the output power of 10 kW and firing angle of 0°. Table 5.19 includes the load current harmonics, line current harmonics, and IEEE 519 harmonic limits up to 50^{th} harmonic current component. Moreover, it involves THD_I, THD_V, PF, and f_{AVG} for the two high performance current regulators, DHCR3 and RFCR. If Table 5.19 is compared to Table 5.15 and Table 5.16 for the diode rectifier case, it is clear that the similar results are obtained for the thyristor rectifier case operating at the output power of 10 kW and the firing angle of 0°. The THD_I and THD_V values are well below the IEEE 519 limits. Moreover, the individual harmonic current component percentages for two regulators are also

below the individual harmonic current component limits of IEEE 519. The PF value for both current regulators is unity and the f_{AVG} value for RFCR is 13.3 kHz while the f_{AVG} value for DHCR3 is 10.0 kHz as in the diode rectifier case. The steady-state power flow data for the AC utility grid, thyristor rectifier load operating at a=0° and the PAF system with DHCR3 and RFCR is given in Table 5.20. While the load power and the line power for both regulators are same as expected, the power rating of the PAF is different for the DHCR3 and the RFCR due to the different capacitor sizes of the utilized SRFs as in the case of the diode rectifier. Moreover, the power rating of the PAF for the thyristor rectifier is less than the power rating of the PAF for the diode rectifier (Table 5.17). The reason is that the load current THD value of 25.6% for the thyristor rectifier is lower than the load current THD value of 32.6% for the diode rectifier load. This means that the rms value of the harmonic current component of the load current for the thyristor rectifier is less than the rms value of the harmonic current component of the load current for the diode rectifier, which results in a lower PAF power rating. The above discussion illustrates that the thyristor rectifier load operating at the firing angle value of 0° does not differ from the diode rectifier load and the performance of the PAF for the thyristor rectifier with a=0° is nearly same as the performance of the PAF for diode rectifier case.

Table 5.19 Computer simulation results of the line current harmonics, THD_I, THD_V, PF at PCC, f_{AVG} for the thyristor recitifer load with $a = 0^o$, and IEEE 519 limits.

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%) DHCR3	Line Current Harmonics with PAF (%) RFCR	IEEE 519 Harmonic Current Limits (I_{SC}/I_{L1}=173) (%)
I_1	100.0	100.0	100.0	100.0
I_5	22.4	0.7	0.2	12.0
I_7	9.1	1.0	0.1	12.0
I_{11}	6.8	1.2	0.1	5.5
I_{13}	3.7	1.1	0.1	5.5
I_{17}	2.6	0.2	0.1	5.0
I_{19}	1.6	0.3	0.1	5.0
I_{23}	1.2	0.7	0.4	2.0
I_{25}	0.7	0.2	0.3	2.0
I_{29}	0.8	0.4	0.3	2.0
I_{31}	0.5	0.2	0.2	2.0
I_{35}	0.6	0.3	0.4	1.0
I_{37}	0.4	0.3	0.3	1.0
I_{41}	0.4	0.3	0.3	1.0
I_{43}	0.3	0.4	0.3	1.0
I_{47}	0.3	0.2	0.4	1.0
I_{49}	0.2	0.5	0.2	1.0
THD_I (%)	25.6	4.2	2.2	15.0
THD_V (%)	0.4	1.4	0.8	5.0
PF	0.950	0.999	0.999	---
f_{AVG}(kHz)		10.0	13.3	

Table 5.20 Steady-state power flow data for the AC utility grid, thyristor rectifier load operating at a=0° and the PAF system with the DHCR3 and the RFCR

	Load current/phase (A rms)	Line current/phase (A rms)	Filter current/phase (A rms)	SRF current/phase (A rms)	Line Voltage/phase (V rms)	Load Power (kVA) (PF=0.950)	Line Power (kVA) (PF=0.999)	Filter Power (kVA)
DHCR3	16.1	15.5	4.4	2.4	220	10.6	10.2	2.9
RFCR	16.1	15.5	5.2	0.6	220	10.6	10.2	3.4

5.7.2 The PAF Performance for The Thyristor Rectifier Load with *a* =30°

The reactive power demand of the thyristor rectifier can be increased by increasing the firing angle value such that the output real power is kept constant. In this case study, the thyristor rectifier is operated with a firing angle value of 30° at the rated output power of 10 kW such that the load resistor value is decreased to 19 Ω. This operating condition for the rectifier increases the reactive power demand such that the resulting PF value at the input terminals of the rectifier is 0.82. The reactive power compensation capability and the performance of the PAF for both superior current regulators of the DHCR3 and the RFCR will be investigated with this study.

The steady-state performance of the PAF for the DHCR3 and the RFCR is summarized in Table 5.21. Table 5.21 includes the load current harmonics of the thyristor rectifier with *a*=30°, line current harmonics, and IEEE 519 harmonic limits up to 50^{th} harmonic current component. Moreover, it involves THD_I, THD_V, PF and f_{AVG} for both current regulators as in the previous cases. Figure 5.41 illustrates the voltage at the PCC, the line current, the load current, the PAF current waveforms for 'phase *a,*' and the DC bus voltage waveforms of PAF system with the DHCR3 that compensates harmonics and reactive current component of thyristor rectifier load with the output power rating of 10 kW and firing angle of 30° at steady-state over a fundamental cycle. The detailed illustration of the line current, the PAF current reference and the PAF current is illustrated in Figure 5.42 for the PAF system with the DHCR3. Figure 5.43 provides a visualization of the line current harmonic spectrum over a wide frequency range for the DHCR3. Similarly, Figure 5.44 illustrates the waveforms of PAF system with RFCR at steady-state over a fundamental cycle, Figure 5.45 illustrates the line current, the PAF current reference and the PAF current in detail, and Figure 5.46 illustrates the line current harmonic spectrum over a wide frequency range for the thyristor rectifier load with the output power rating of 10 kW and firing angle of 30°. Based on the data in the table, the load current harmonics are suppressed up to 31^{st} harmonic. The compensation of the higher order harmonics is partial. This illustrates the performance degradation of the PAF system due to the increase of the di/dt value during the commutation intervals

for thyristor rectifier with a=30° compared to the diode rectifier case or thyristor rectifier with a=0°. The tracking capability of the DHCR3 in Figure 5.42 and the RFCR in Figure 5.45 degrades during high di/dt regions, which results in the performance degradation of the PAF system with two superior current regulators and the current spikes on the line current waveform for both current regulators. In order to eliminate this performance degradation during high di/dt regions, the bandwidth of the current regulators should be increased, which requires higher switching frequency. However, the utilization of the higher switching frequency is limited in practical application since it results in excessive power loss in high power application and thermal instability of the system.

However, although current spikes exist due to the high di/dt value of the load current during the commutation intervals, the line current THD_I value is 6% for DHCR3 and 5.6% for the RFCR, which is below the IEEE 519 THD_I limit of 15%. Moreover, the PF at the line side is nearly unity with the value of 0.998 while the load side PF value is 0.82, which illustrates the reactive power compensation capability of the PAF. Moreover, the high di/dt demand of the current reference results in the saturation of the inverter during the commutation intervals of the load current and results in a lower f_{AVG} value. The f_{AVG} value for the DHCR3 is 9 kHz in the case of the thyristor rectifier with a=30° while the value is 10 kHz in the case of the diode rectifier case and thyristor rectifier with a=0°. Similarly, due to partial inverter saturation in the RFCR case the f_{AVG} value changes to the value of 12.5 kHz from the value of 13.3 kHz for the thyristor rectifier with a=0°.

The steady-state power flow data for the AC utility grid, thyristor rectifier load operating at a=30° and the PAF system with the DHCR3 and the RFCR is given in Table 5.22. In the case of the thyristor rectifier with a=30°, the load power is increased compared to the diode rectifier case and thyristor rectifier with a=0° since the reactive power demand of the nonlinear load is increased for the same real output power demand. However, since the PAF compensates the harmonics and the reactive power demand of the thyristor rectifier, the line power is nearly the same with the nearly unity PF for the thyristor rectifier with a=30°, thyristor rectifier with a=0°,

and the diode rectifier case. The power rating of the PAF is increased compared to the previous nonlinear load cases since the reactive power demand of the load is increased and different for the DHCR3 and the RFCR due to the different capacitor sizes for the utilized SRFs. While the power rating of the PAF utilizing DHCR3 is 2.9 kVA for thyristor rectifier with a=0°, it is 6 kVA for thyristor rectifier with a=30°. Similarly, the power rating of the PAF utilizing RFCR is 3.4 kVA for thyristor rectifier with a=0°, it is 7.2 kVA for thyristor rectifier with a=30°.

The subsection illustrated that the PAF compensates the rectifier power demand of the nonlinear load with the increased rating of the PAF. Although the performance degradation of the PAF is unavoidable due to the increased di/dt of the current reference with a=30°, the THD_I value for both current regulators is below the IEEE 519 limits. Further, this section is the verification of the superior performance of the new current regulator, DHCR3. It gives a comparable THD_I value of 6% with lower f_{AVG} value of 9 kHz compared to the RFCR in the case of the thyristor rectifier with a=30°.

Table 5.21 Computer simulation results of the line current harmonics, THD_I, THD_V, PF at PCC, f_{AVG} for the thyristor recitifer load with $a = 30^o$, and IEEE 519 limits.

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%) DHCR3	Line Current Harmonics with PAF (%) RFCR	IEEE 519 Harmonic Current Limits (I_{SC}/I_{L1}=173) (%)
I_1	100.0	100.0	100.0	100.0
I_5	27.3	1.9	0.5	12.0
I_7	9.4	1.0	0.3	12.0
I_{11}	9.9	1.5	0.1	5.5
I_{13}	4.2	1.0	0.1	5.5
I_{17}	5.3	1.9	0.1	5.0
I_{19}	2.7	0.8	0.1	5.0
I_{23}	3.3	1.3	2.0	2.0
I_{25}	2.0	1.0	1.4	2.0
I_{29}	2.2	1.5	1.8	2.0
I_{31}	1.6	1.0	1.2	2.0
I_{35}	1.5	1.3	1.6	1.0
I_{37}	1.2	0.4	1.0	1.0
I_{41}	1.0	0.5	1.4	1.0
I_{43}	1.0	1.0	0.8	1.0
I_{47}	0.6	0.3	1.2	1.0
I_{49}	0.8	0.7	0.7	1.0
THD_I (%)	31.8	6.0	5.6	15.0
THD_V (%)	0.8	1.5	1.1	5.0
PF	0.82	0.998	0.998	---
f_{AVG} (kHz)		9.0	12.5	

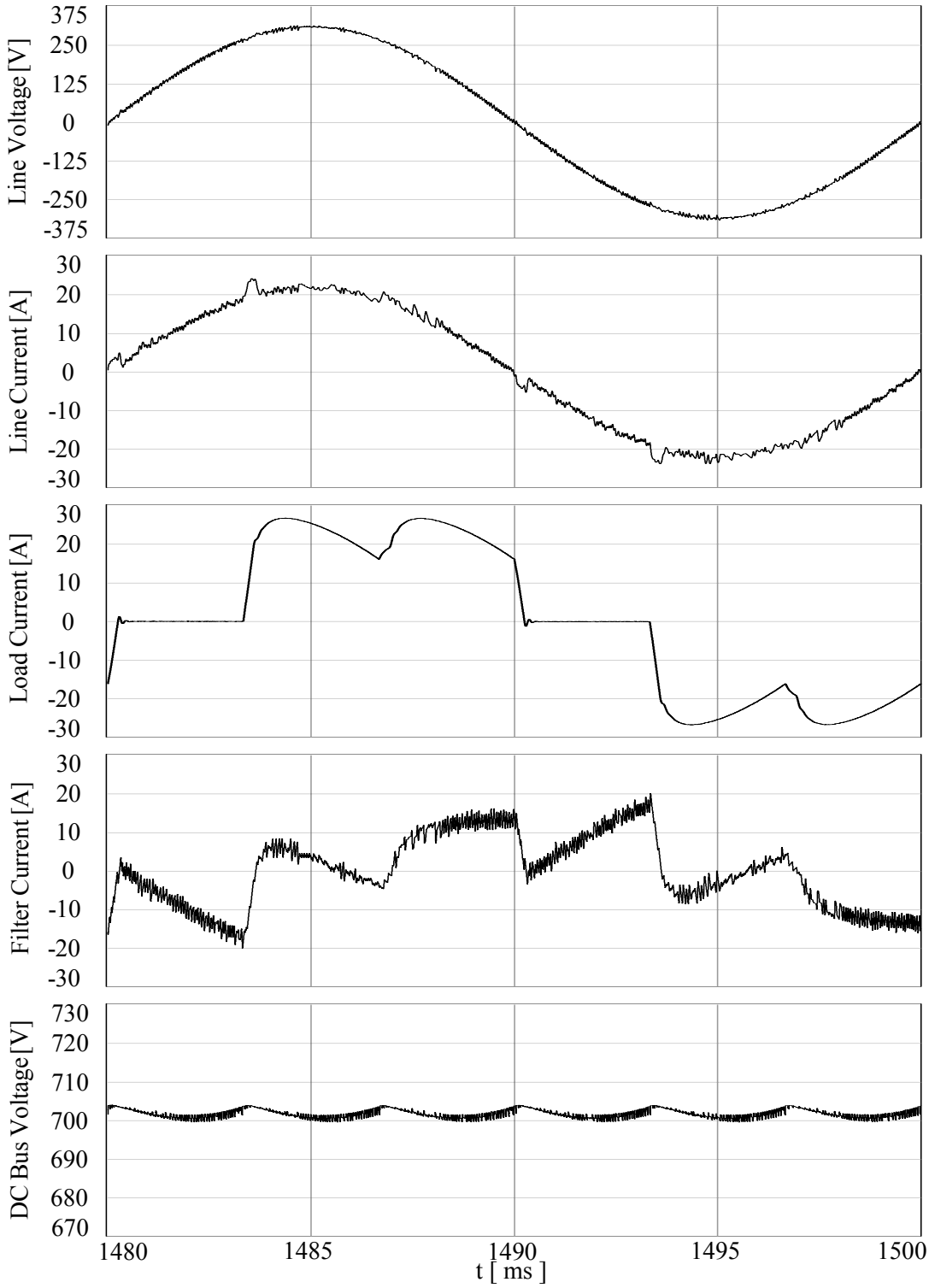

Figure 5.41 Steady-state waveforms over a fundamental cycle illustrating the performance of the PAF utilizing the DHCR3 for the thyristor rectifier with *a*=30°: Voltage at the PCC, line current, load current, the PAF current for 'phase *a,*' and DC bus voltage.

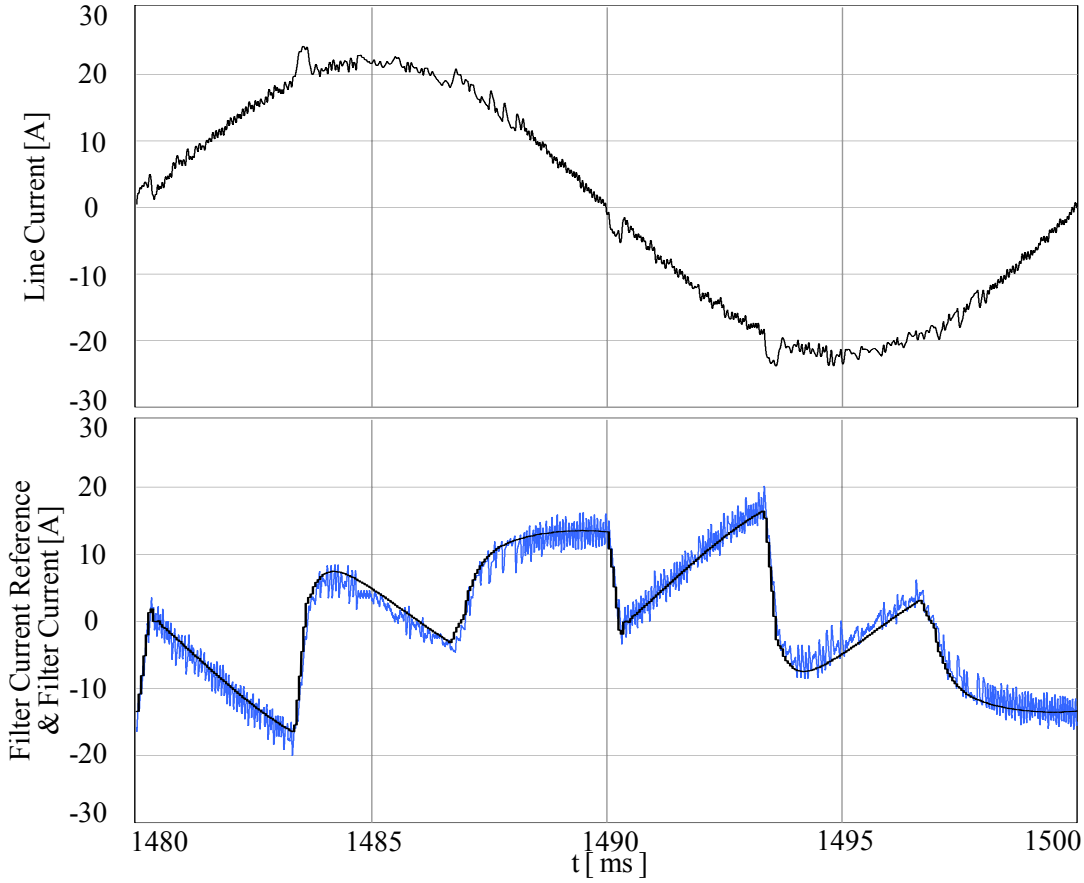

Figure 5.42 Steady-state line current, filter current reference (black) and filter current (blue) over a fundamental cycle for the DHCR3 with SRF and the thyristor rectifier load with a=30°.

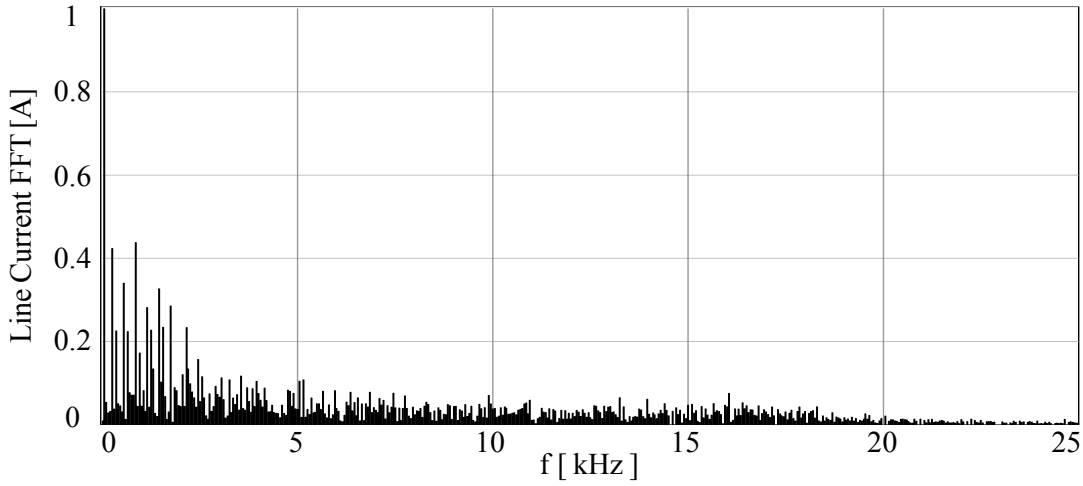

Figure 5.43 Steady-state line current harmonic spectrum for the DHCR3 with SRF and the thyristor rectifier load with a=30°.

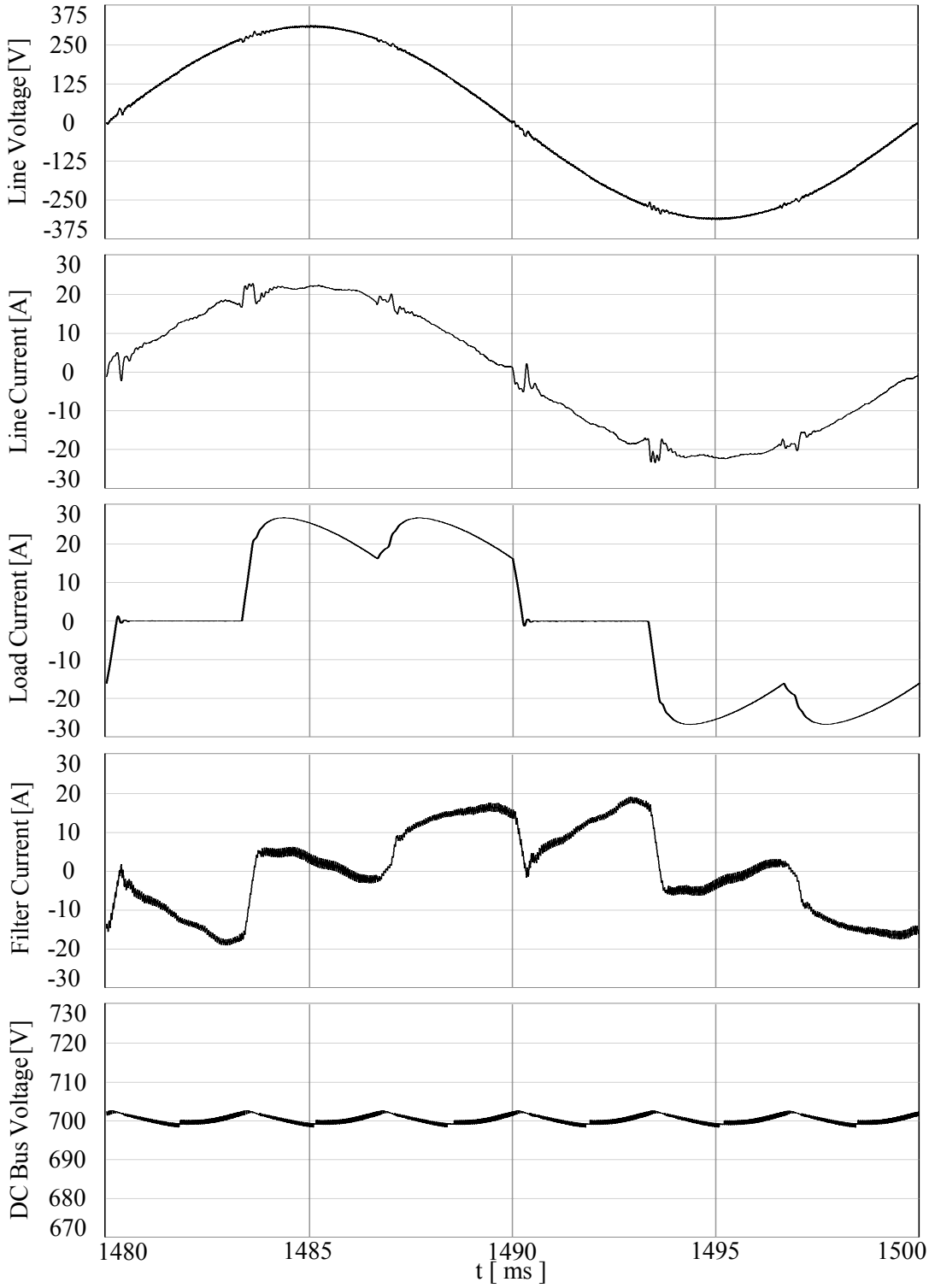

Figure 5.44 Steady-state waveforms over a fundamental cycle illustrating the performance of the PAF utilizing the RFCR for the thyristor rectifier with a=30°: Voltage at the PCC, line current, load current, the PAF current for 'phase *a,*' and DC bus voltage.

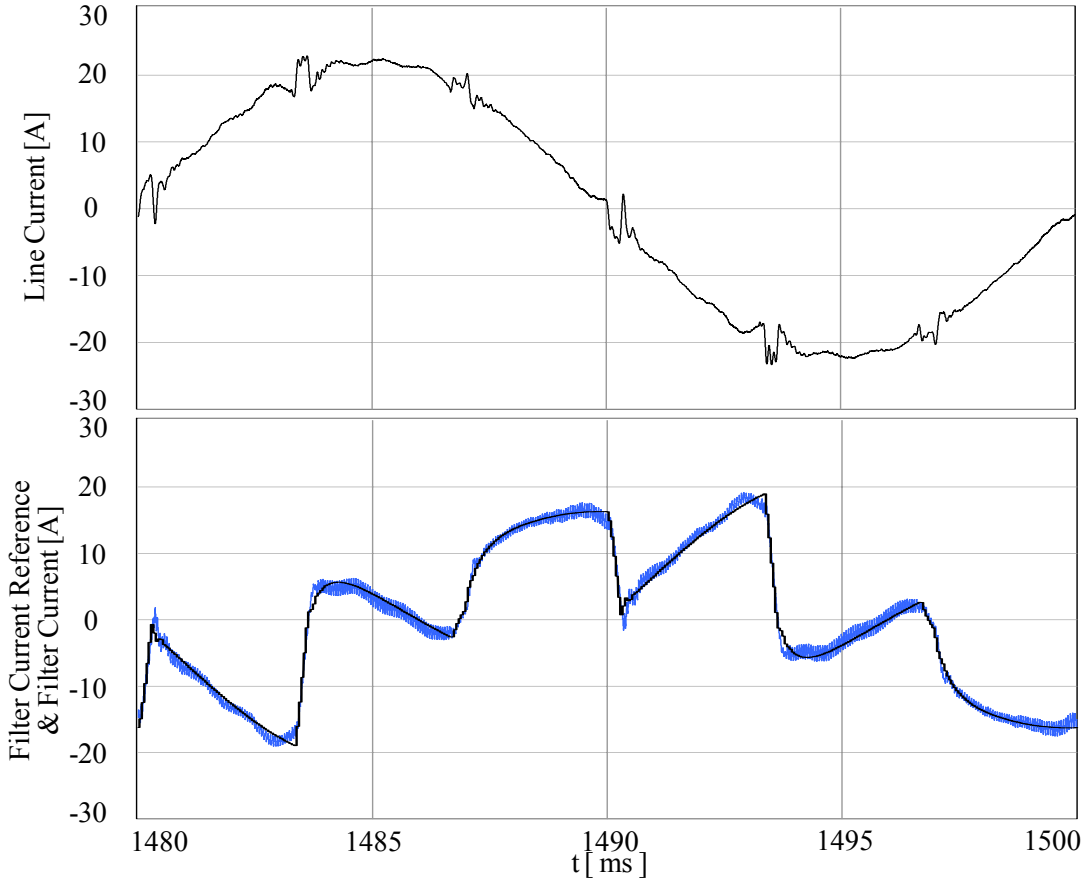

Figure 5.45 Steady-state line current, filter current reference (black) and filter current (blue) over a fundamental cycle for the RFCR with SRF and the thyristor rectifier load with a=30°.

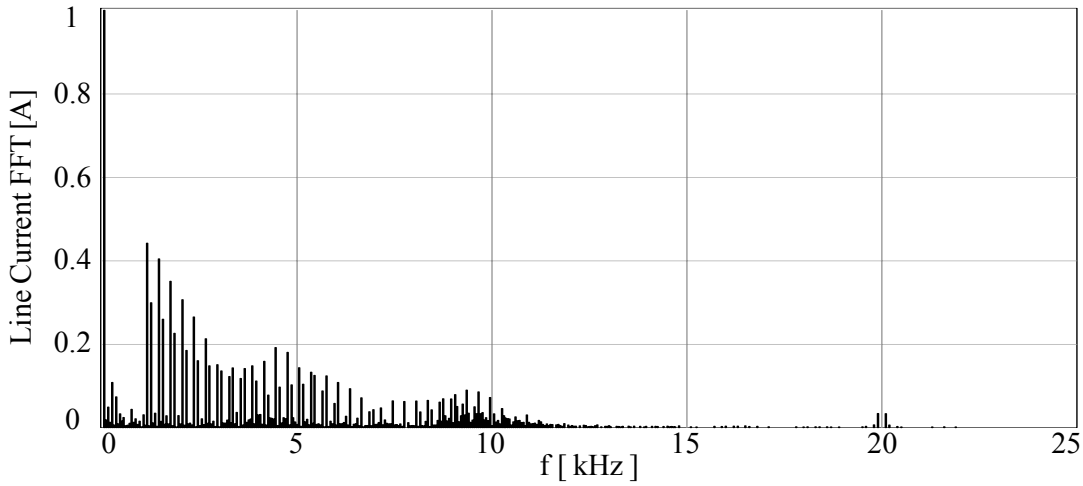

Figure 5.46 Steady-state line current harmonic spectrum for the RFCR with SRF and the thyristor rectifier load with a=30°.

Table 5.22 Steady-state power flow data for the AC utility grid, thyristor rectifier load operating at *a*=30°, and the PAF system with the DHCR3 and the RFCR

	Load current/phase (Arms)	Line current/phase (Arms)	Filter current/phase (Arms)	SRF current/phase (Arms)	Line Voltage/phase (Vms)	Load Power (kVA) (PF=0.820)	Line Power (kVA) (PF=0.998)	Filter Power (kVA)
DHCR3	18.7	15.7	9.1	2.4	220	10.6	10.4	6.0
RFCR	18.7	15.7	10.9	0.6	220	10.6	10.4	7.2

5.7.3 Negative Sequence Current Compensation Capability of The PAF

The PAF utilizing the SRFC for harmonic current extraction is capable of compensating negative sequence load current in the case of unbalance condition. However, if the compensation of the negative sequence load current is not desired, the negative sequence SRFC should be designed parallel to the positive sequence SRFC as discussed in Chapter 2. This section illustrates the negative sequence compensation capability of the PAF by creating negative sequence load current, which is illustrated via two case studies. The first case study named as 'Case A' is carried out on the thyristor rectifier such that the firing angle of the leg of the thyristor rectifier corresponding to the phase '*a*' is adjusted to 30° while the firing angle of the other legs is adjusted to 0° in computer simulation environment. The second case study named as 'Case B' is the creation of the negative sequence current by adjusting the rms value of the line voltage for the phase '*b*' to its 75% rated value while the other line voltages remain the same as their rated values of 220 V and all the firing angles for three legs of the thyristor rectifier are 0°.

The normal operating condition of the thyristor rectifier should be illustrated before the analysis of the cases. Figure 5.47 illustrates the voltage at the PCC, the line current, the load current, and the PAF current waveforms for all phases, the rectifier DC bus voltage and the DC bus voltage waveforms of the PAF system with the

DHCR3 that compensates harmonics and reactive current component of thyristor rectifier load with the output power rating of 10 kW and firing angle of 0° at the steady-state over a fundamental cycle. The operation of the thyristor rectifier is balanced since the load currents are balanced and the DC bus voltage of the rectifier consists of regular six pulses. In this case, the PAF compensates the load current harmonics and reactive power component such that the line current is nearly sinusoidal and in phase with the line voltage. Figure 5.48 illustrates the waveforms for the thyristor rectifier operated as in the Case A. In this case, the load currents differs in rms value and the DC bus voltage of the rectifier has a 100 Hz component on it, which illustrates the negative sequence current components at the AC side of the rectifier. Moreover, the conduction interval for phase '*a*' is retarded by 30° which results in a reactive power demand increase for phase '*a*'. In order to observe the unbalanced condition for this case, the waveforms with the rectifier load in this case can be compared to the waveforms of the rectifier load operating in balance case in Figure 5.47. For the this case, the PAF control algorithm utilizing only the positive sequence SRFC creates also the reference signal for the compensation of the negative sequence load current in addition to the load current harmonics and reactive power component. As a result, the line currents are balanced, sinusoidal and in phase with the line voltage. If a negative sequence SRFC parallel to the positive sequence SRFC is designed for the elimination of the negative sequence current reference from the total current reference as discussed in Chapter 2, the compensation of the negative sequence load current is avoided. Figure 5.49 illustrates the waveforms for the thyristor rectifier operated as in the Case A and the PAF system with negative sequence SRFC parallel to the positive sequence controller. The cut-off frequencies of the LPFs in the negative sequence SRFC is selected as 20 Hz as in the positive sequence SRFC. From Figure 5.49, since the negative sequence load current compensation capability of the PAF system eliminated via a negative sequence SRFC, the line currents sinusoidal and in phase line voltage, but they are not balanced as expected.

Figure 5.50 illustrates the waveforms for the thyristor rectifier operated as in Case B such that PAF compensates the negative sequence load current component. From the figure, the negative sequence current is clear such that load current for phase '*b*' has a lower rms value than the rms values of the other phases. Moreover, the DC bus voltage of the rectifier has a 100 Hz component on it as in the previous case. For this case, the PAF control algorithm does not include the negative sequence SRFC controller and the PAF creates filters currents which result in sinusoidal, in phase, and balanced line currents. Figure 5.51 illustrates the waveforms for the thyristor rectifier operated as in the Case B and the PAF system with negative sequence SRFC parallel to the positive sequence controller. Although the PAF compensates the load current harmonics and reactive power component, it does not compensate the negative sequence component of the load current due to negative sequence SRFC in its control algorithm. In this case, the line current for the phase '*b*' has lower peak value than the peaks values for other phase line currents as expected. Although this case study illustrates the negative sequence compensation capability of the PAF, it also illustrates the operation and the performance of the PAF under line voltage drops.

The steady-state power flow data of the AC utility grid, the thyristor rectifier load and the system for the Case A and Case B is given in Table 5.23. Table 5.23 includes the rms value of the line voltages (V_F), load currents (I_L), line currents (I_S), filter current (I_F), and switching ripple filter current (I_{SRF}) for all phases, the mean value of the rectifier DC bus voltage (V_{dc_load}) and filter DC bus voltage (V_{DC}) Moreover, it includes the load power (S_L), line power (S_S), and the filter power (S_F) for all phases. From the data in the table, if the negative sequence load current component is not compensated by the PAF, the line currents differ in rms values. However, if it is compensated, line currents have close rms values. In the table, THD_I values for the line currents and the PF values at the line side is also included for the illustration of the harmonic and reactive power current compensation performance of the PAF in addition to its negative sequence current compensation performance for the cases analyzed.

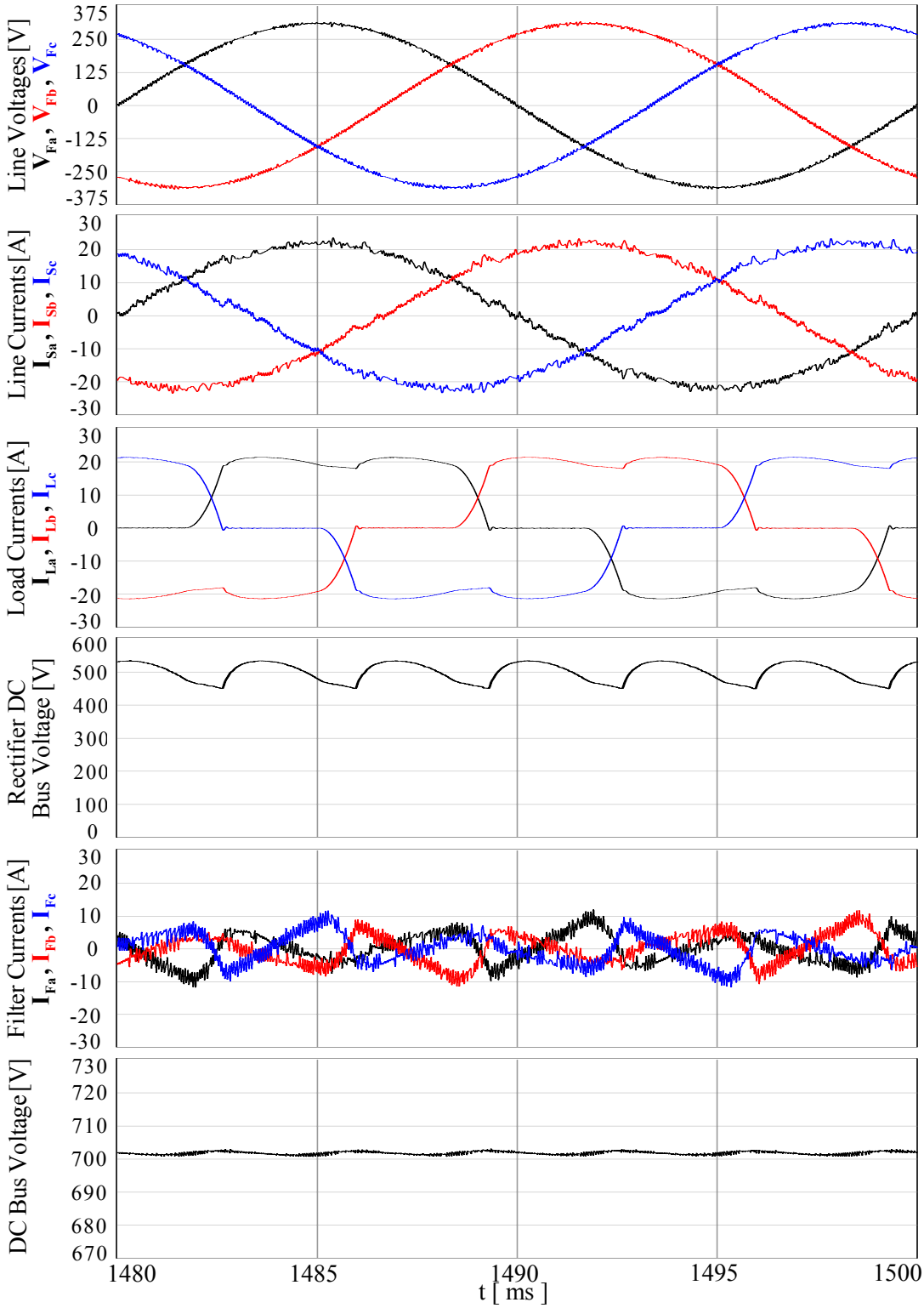

Figure 5.47 Steady-state waveforms over a fundamental cycle for the PAF utilizing the positive sequence SRFC and the DHCR3 and the thyristor rectifier with a=0°: Line voltages, line currents, load currents, the rectifier DC bus voltage, the PAF currents, and the DC bus voltage.

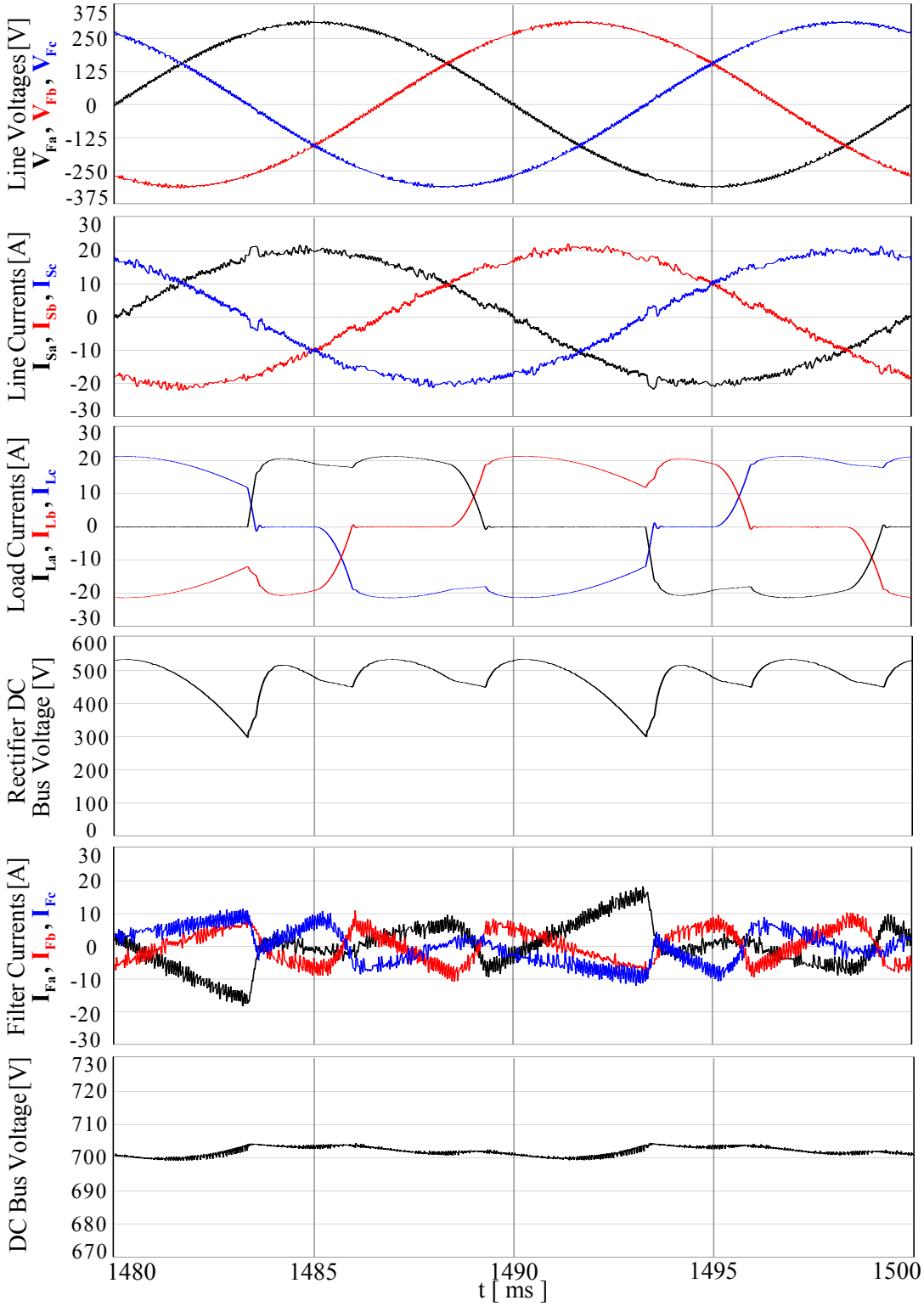

Figure 5.48 Steady-state waveforms over a fundamental cycle for the PAF utilizing the positive sequence SRFC and the DHCR3 and the thyristor rectifier operating under Case A: Line voltages, line currents, load currents, the rectifier DC bus voltage, the PAF currents, and the DC bus voltage.

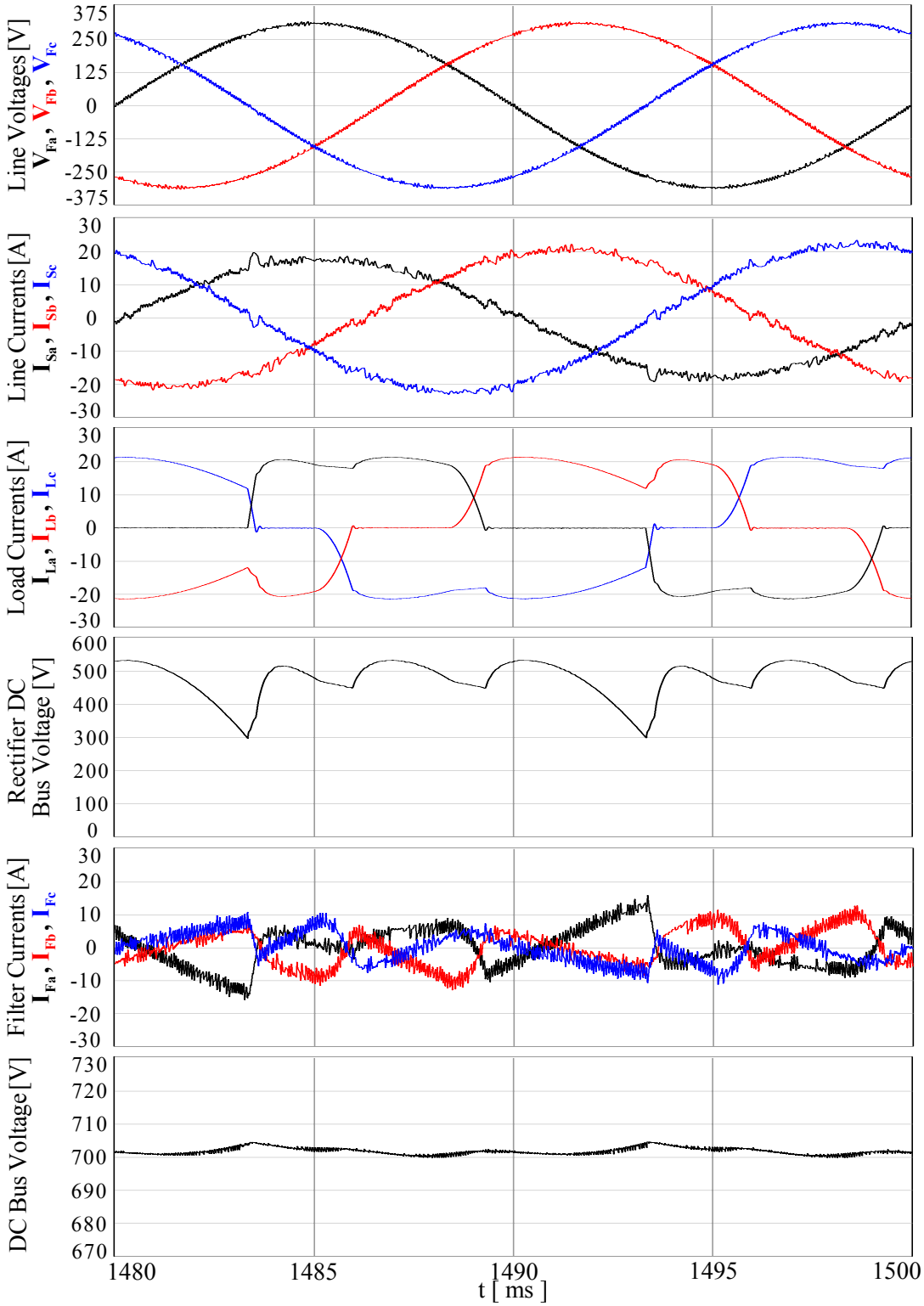

Figure 5.49 Steady-state waveforms over a fundamental cycle for the PAF utilizing the positive and negative sequence SRFC and the DHCR3 and the thyristor rectifier operating under Case A: Line voltages, line currents, load currents, the rectifier DC bus voltage, the PAF currents, and the DC bus voltage.

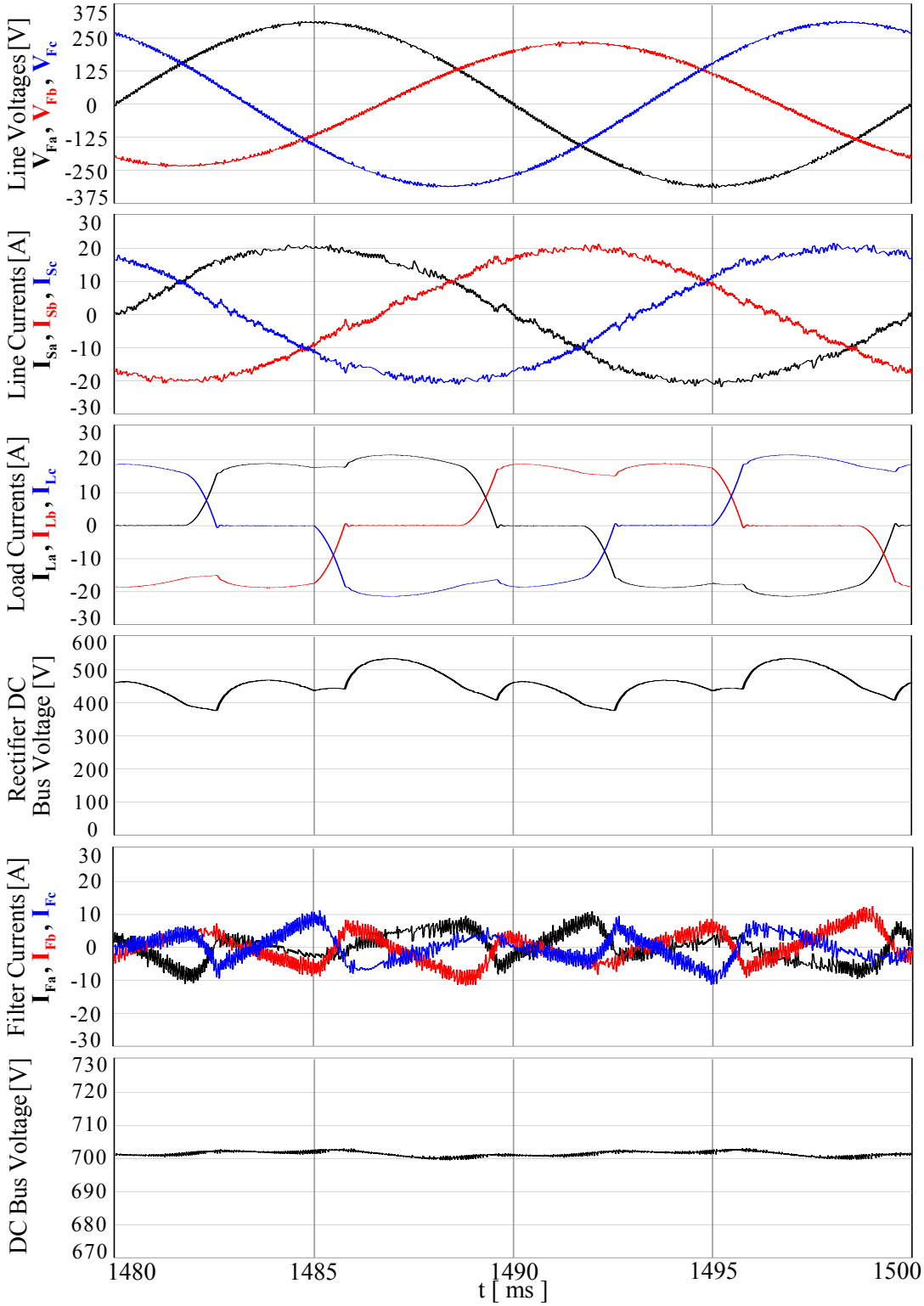

Figure 5.50 Steady-state waveforms over a fundamental cycle for the PAF utilizing the positive sequence SRFC and the DHCR3 and the thyristor rectifier operating under Case B: Line voltages, line currents, load currents, the rectifier DC bus voltage, the PAF currents, and the DC bus voltage.

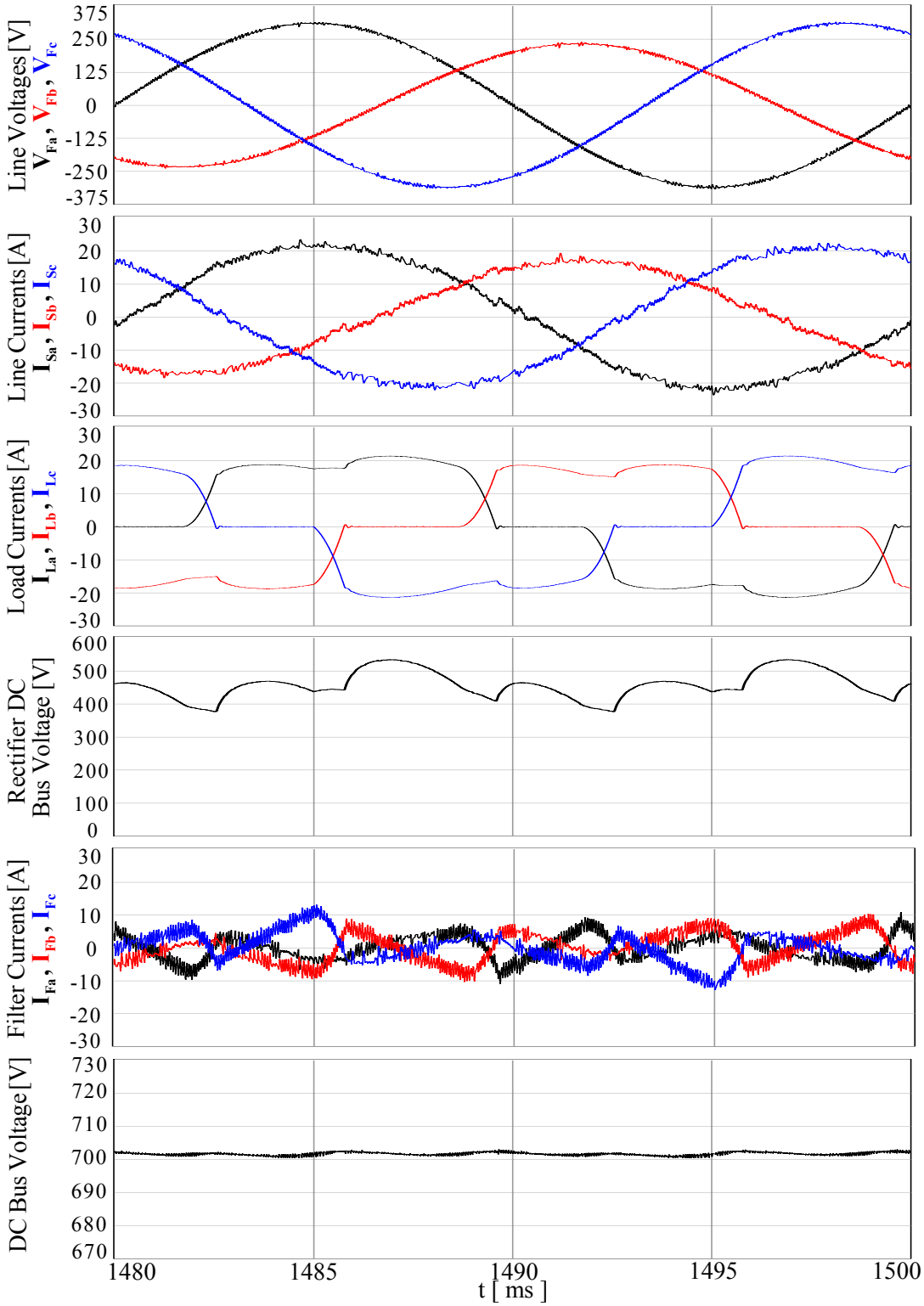

Figure 5.51 Steady-state waveforms over a fundamental cycle for the PAF utilizing the positive and negative sequence SRFC and the DHCR3 and the thyristor rectifier operating under Case B: Line voltages, line currents, load currents, the rectifier DC bus voltage, the PAF currents, and the DC bus voltage.

Table 5.23 The steady-state power flow data of the AC utility grid, thyristor rectifier load, and the system for negative sequence compensation capability of the PAF system under Case A and Case B.

	PHASE	Normal thyristor load operation $a=0^0$	CASE A Phase '*a*' thyristor is delayed by 30^0 ($a= a+30^0$) such that 2.2 A negative sequence current generated		CASE B Phase '*b*' line voltage is dropped %25 of its nominal value such that 2.6 A negative sequence current generated	
			compensated via PAF	not compensated via PAF	compensated via PAF	not compensated via PAF
V_F (V rms)	*a*	220	220	220	220	220
	b	220	220	220	165	165
	c	220	220	220	220	220
I_L (A rms)	*a*	16.1	14.5	14.5	15.6	15.6
	b	16.1	15.2	15.2	13.5	13.5
	c	16.1	16.9	16.9	15.2	15.2
V_{dc_load} (V)		500	478	478	460	460
I_S (A rms)	*a*	15.5	14.4	12.8	14.6	15.4
	b	15.5	14.6	14.7	13.9	12.0
	c	15.5	14.2	15.8	14.5	15.2
I_F (A rms)	*a*	4.4	6.5	5.8	4.2	4.5
	b	4.4	4.8	5.3	4.5	4.3
	c	4.4	5.2	4.4	4.0	3.7
I_{SRF} (A rms)	*a*	2.4	2.4	2.4	2.4	2.4
	b	2.4	2.4	2.4	2.1	2.1
	c	2.4	2.4	2.4	2.4	2.4
S_L (kVAr) & PF	*a*	3.5 / 0.95	3.2 / 0.87	3.2 / 0.87	3.4 / 0.94	3.4 / 0.94
	b	3.5 / 0.95	3.3 / 0.94	3.3 / 0.94	2.2 / 0.93	2.2 / 0.93
	c	3.5 / 0.95	3.7 / 0.93	3.7 / 0.93	3.3 / 0.96	3.3 / 0.96
S_S (kVAr) & PF	*a*	3.4 / 1.00	3.2 / 1.00	2.8 / 1.00	3.2 / 1.00	3.4 / 0.99
	b	3.4 / 1.00	3.2 / 1.00	3.2 / 0.99	2.3 / 1.00	2.0 / 1.00
	c	3.4 / 1.00	3.1 / 1.00	3.5 / 1.00	3.2 / 1.00	3.3 / 0.99
S_F (kVAr)	*a*	1.0	1.4	1.3	0.9	1.0
	b	1.0	1.1	1.2	0.7	0.7
	c	1.0	1.1	1.0	0.9	0.8
THD_I (%)	*a*	4.2	5.4	6.1	5.2	4.9
	b	4.2	4.7	4.6	5.2	5.7
	c	4.2	4.9	4.6	5.2	5.0

5.8 Summary

In this chapter, the PAF performance was investigated by means of computer simulations. The computer simulation model of the AC utility grid, nonlinear load, and the PAF system was built. As a nonlinear load, a diode rectifier with the output power rating of 10 kW was selected and the performance criteria based on the IEEE 519 harmonic recommendation was determined for the whole system. Then the detailed computer simulations were conducted for the whole system. First, the PAF control algorithm was analyzed via computer simulation. Computer simulation results of theoretically analyzed current regulators in Chapter 3 were presented and verification of the discussed issues with the current regulators in PAF application was performed. Moreover, a comparison study was carried out in order to determine the superior performance current regulators in the PAF application. The expected superior performance with the resonant filter current regulator and the improved discrete time hysteresis current regulator, DHCR3 was verified by means of the computer simulation. Further, the switching ripple filter design for the linear and hysteresis current regulators was completed in this section and their performances were illustrated. The determination of the suitable current regulator for PAF application and the verification of the designed switching ripple filters lead the illustration of the overall performance of the PAF. The steady-state performance and the dynamic response were analyzed and the discussion with the control algorithm of the PAF was completed. Finally, the performance of the designed PAF was investigated for a thyristor rectifier with an output power of 10 kW and its reactive power and negative sequence compensation capability in addition to the harmonic compensation capability was illustrated. With the investigation of the PAF performance completed by means of the computer simulation, the following chapter experimentally verifies this performance.

CHAPTER 6

THE PARALLEL ACTIVE FILTER PERFORMANCE ANALYSIS BY MEANS OF EXPERIMENTAL STUDIES

6.1 Introduction

This chapter experimentally investigates the performance of the PAF system for the harmonic, reactive power, and negative sequence current components compensation of the diode rectifier load. The PAF basic performance is investigated first, and then the current regulators are analyzed experimentally. As in the computer simulation part, in the experiments also, a comparison study will be carried out for the current regulators without SRF. Following, the designed SRFs in Chapter 4 and Chapter 5 are included and experimentally analyzed and their performances will be illustrated. Then the detailed performance illustration of the PAF with the steady-state performance and dynamic response analysis is performed via experimental studies. Moreover, the designed PAF is experimentally tested for the thyristor rectifier in order to illustrate its reactive power compensation capability. Moreover, the performances of the discrete time current regulators with superior performances, DHCR3 and RFCR, are verified for the current references with high di/dt. Briefly, this chapter is the experimental verification of the computer simulation results. Before the PAF system experimental performance investigation, the experimental hardware and the software description of the system are presented.

6.2 Hardware Description of The Nonlinear Load and Manufactured PAF System

The designed PAF for harmonic current and reactive current component compensation of a 10 kW nonlinear load system is constructed at METU Electrical and Electronics Engineering Department, in the Electrical Machines and Power Electronics Laboratory as a prototype and an experimental setup is established. The block diagram of the experimental setup is given in Figure 6.1. The electrical power circuitry of the overall system is shown in Figure 6.2. Additionally, Figure 6.3 and Figure 6.4 illustrate the laboratory prototype of the manufactured PAF.

For the purpose of laboratory evaluation, an experimental three-phase 380V, 50 Hz, 10 kW uncontrollable rectifier connected to the 380V, 50 Hz three-phase AC utility grid at the PCC is utilized as a harmonic current source type nonlinear load for the PAF application. The uncontrolled rectifier is constructed by a 1600 V, 100 A three-phase full-bridge diode rectifier module connected to the PCC via a three-phase 20 A automatic fuse and a three-phase 25 A circuit breaker for protection purposes and a three-phase in-line smoothing reactor (L_{ac} = 1.43 mH/phase, 20 A rms current rating), which lowers the distortion of the input current waveform. A DC link current smoothing inductor (L_{dc}=1.46 mH with 20 A rms current rating) is inserted between the rectifier output and the DC bus of the inverter in order to further improve the input current waveform and reduce the rms current stress on the DC bus capacitors. Two pre-charge resistors connected series (R_{pre}) are utilized to limit the inrush current during the start-up of the uncontrolled rectifier. The value of each pre-charge resistor is equal to 10 Ω and each has a 40 W power rating. A manual by-pass switch is utilized to short-circuit (by-pass) the pre-charge resistors after the DC bus capacitors are charged to their steady-state value. The non-linear load DC bus consists of four capacitors. As shown in Figure 6.2, two pairs of parallel connected capacitors are connected in series to form a 1000 μF equivalent capacitance with sufficient voltage and high current ratings. Each capacitor (C_{dc}) has 1000 μF capacitance, 450 V DC voltage rating, and 5.5 A rms current rating. Bleeding resistors are connected in parallel with the DC bus capacitors to balance the voltages

of the DC bus capacitors and discharge DC bus capacitors when the load is disconnected. Each bleeding resistor (R_{dc_B}) has 30 kΩ resistance value and 10 W power rating. A 28 kW, 51 A, 550 V DC load bank represented as R_L in Figure 6.2 is utilized as a resistive load. The output power of the nonlinear load is adjusted by switches on load bank. Therefore, the desired power level at the output of the non-linear load is obtained. The parameters of the AC utility grid and the diode rectifier are the same as in the computer simulation part and are tabulated in Table 5.1.

The power circuitry of the PAF system is as follows. A three-phase 20 A automatic fuse for protection purposes and a three-phase 25 A circuit breaker to protect the system and to isolate the PAF from the AC utility grid when the PAF is in its off mode are in series with the PAF and they connect the PAF system to the PCC. A pre-charge unit is employed at the AC side of the PAF to limit the inrush current during the start-up of the PAF system. The pre-charge unit consists of a three-phase circuit breaker and three pre-charge resistors (R_{Fpre}) one for each phase. Each pre-charge resistor is constructed by two resistors connected in series (each is 5.6 Ω and 50 W) to obtain an equivalent resistance value of 11.2 Ω. The pre-charge unit circuit breaker which is controlled by the Digital Signal Processor (DSP) unit automatically bypasses the pre-charge resistors when DC bus voltage of the PAF reaches a voltage limit (the procedure with this part is explained in the section of the start-up procedure of PAF). The filter inductors are manufactured from distributed gap powder metal material (Sendust, Kool Mμ brand name, product of Magnetics Inc.) and have a relative initial permeability value of 26. The inductor is built from E-80 size Kool-Mμ cores. The feature of inductors utilizing Kool Mμ cores is that the inductance value of the inductor changes by a roll-off coefficient determined by DC magnetizing force, H (oersteds) created by the current. The inductors are designed to obtain a roll-off coefficient of 0.45 for the inductor at 50 A instantaneous values. The design value for an inductor constructed by six E cores at zero DC magnetizing force is 2 mH.

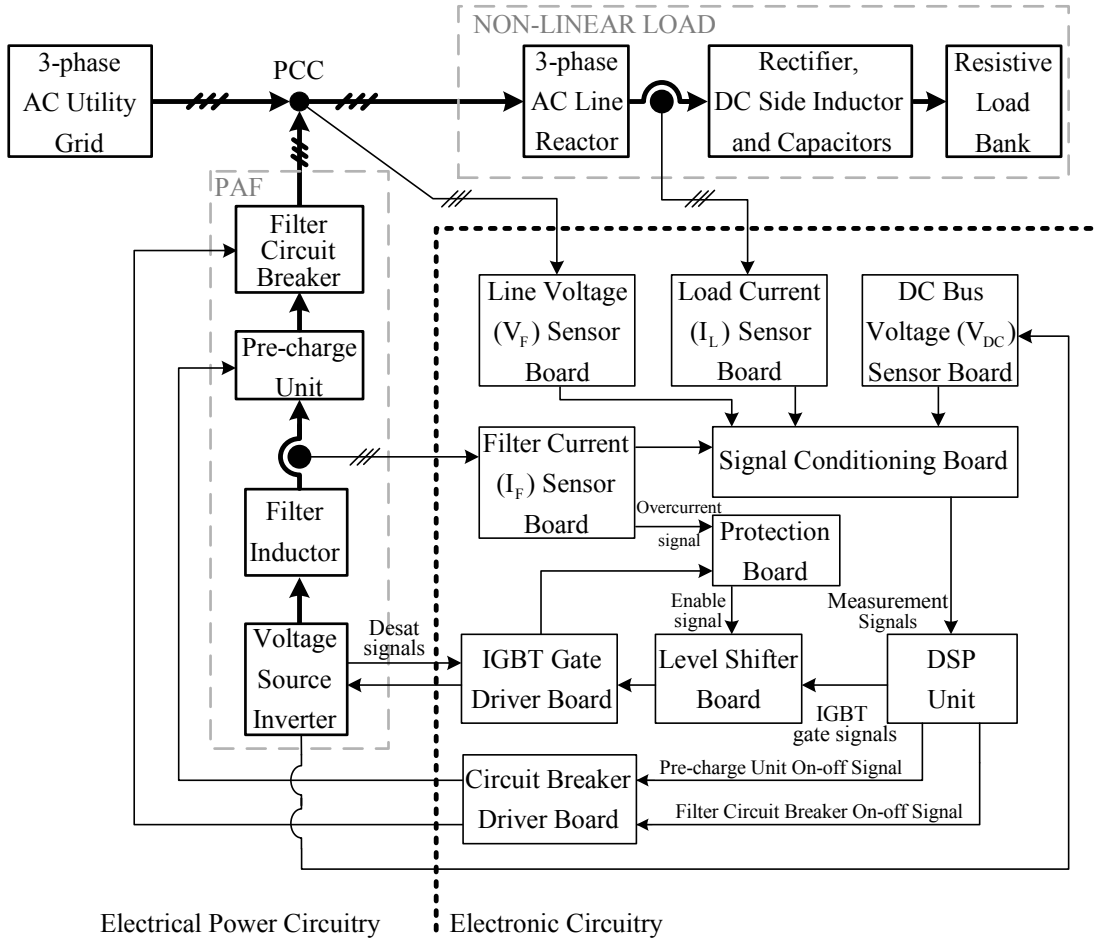

Figure 6.1 The basic system block diagram of the experimental setup.

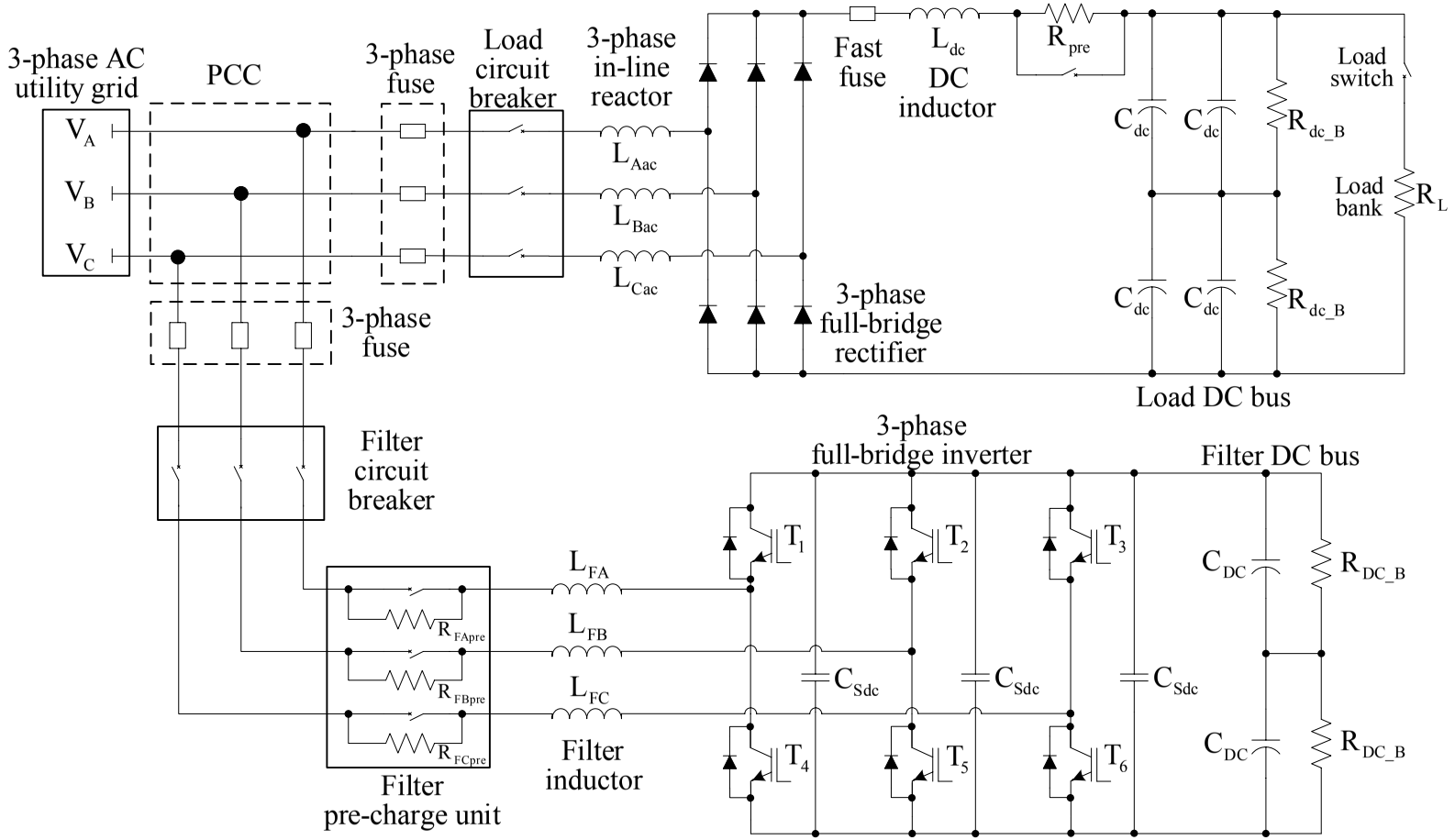

Figure 6.2 The electrical power circuitry of the overall system.

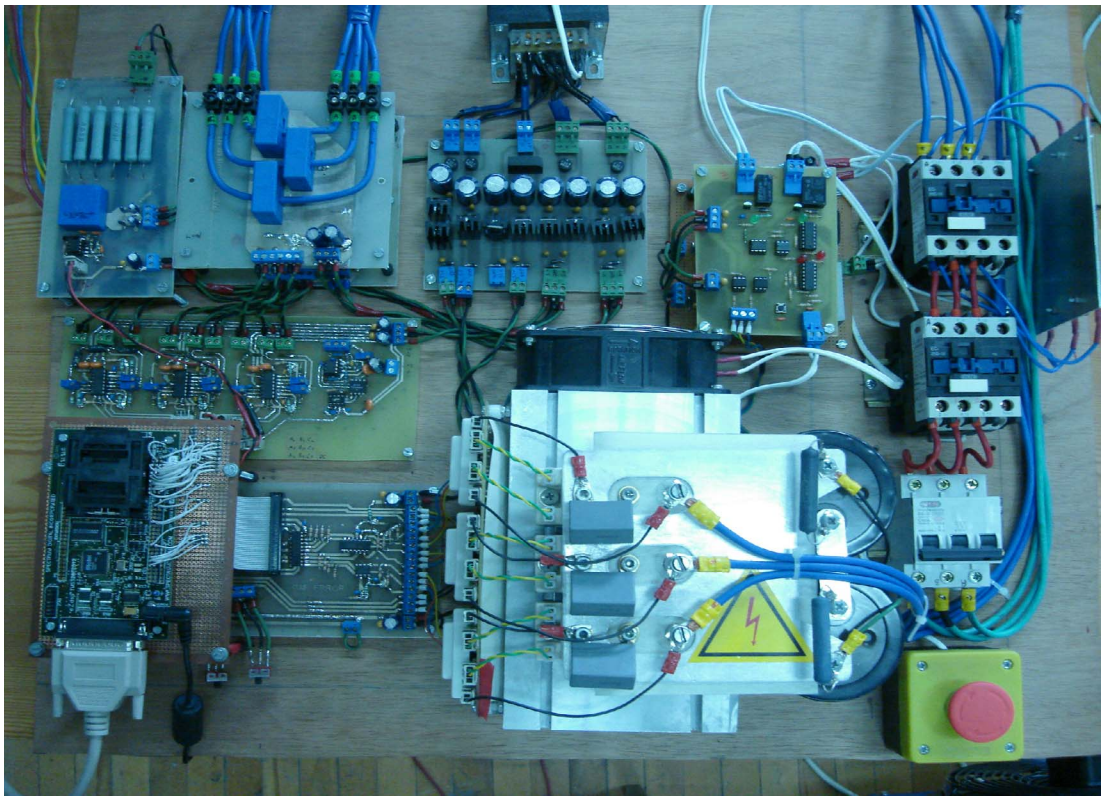

Figure 6.3 Laboratory prototype of the 3-phase 3-wire PAF (top view).

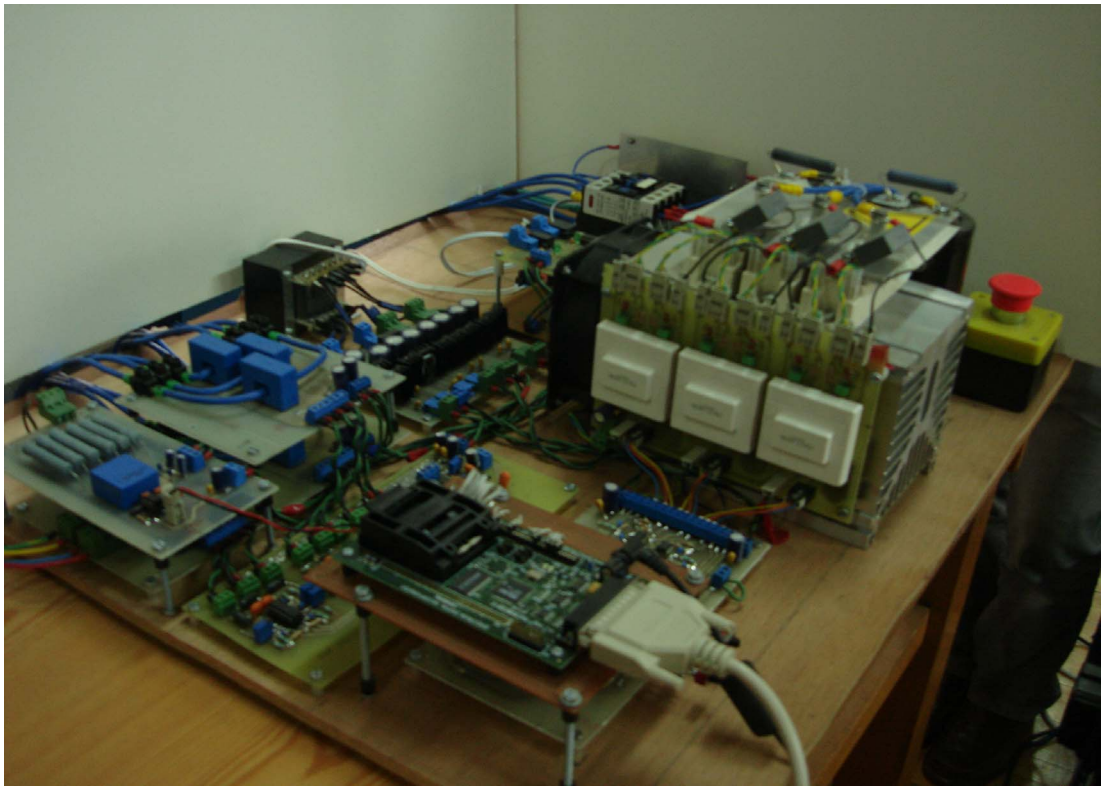

Figure 6.4 Laboratory prototype of the 3-phase 3-wire PAF (side view).

The three-phase full-bridge inverter of the PAF system consists of three dual-pack IGBT modules, the SKM75GB128D model modules manufactured by Semikron. Table 6.1 summarizes the basic specifications of this IGBT module. The IGBT modules are mounted on a 99AS model heatsink. Two aluminum plates separated by an insulation material having an insulation level of 10 kV are mounted on the IGBT modules to form a planar bus structure to obtain low parasitic inductance on the DC bus of the PAF. A snubber capacitor (C_{Sdc}) having a 220 nF capacitance and 1000 V voltage rating is inserted across the DC bus terminals of each IGBT module. Thus, the switching stress on the IGBTs due to the DC bus stray inductance is reduced.

The IGBT modules are driven by the Semikron SKHI 22B gate driver modules mounted on the gate driver electronic circuit board. The basic specifications of the gate driver modules are given in Table 6.1. The gate driver modules have three pins to select the built-in analog dead time generation facility. The dead-time can be set as 0 μs (no interlock), 1.3 μs, 2.3 μs, 3.3 μs or 4.3 μs by different combinations of the voltage (5 V or GND) applied to these pins externally. In the laboratory prototype, the dead-time is set to no interlock level for the gate driver modules since the DSP unit is utilized to generate precise dead-times for PWM pulses. The gate driver board includes three IGBT gate driver modules, where each gate driver module drives the two complementary switches in each IGBT module. The gate driver board converts a PWM signal with +5/0 V voltage levels to an isolated and amplified +15/-7 V voltage levels, which is required for the IGBT turn-on and turn-off operations. The +15 V voltage level is required to turn on and the -7 V voltage level is required to turn off the IGBT. The -7 V voltage level guarantees the turn-off operation of the IGBT. The gate driver module also monitors the collector-emitter voltage for short-circuit failure condition. While the IGBT is conducting, if the collector-emitter voltage of the IGBT is higher than the preset desaturation limit voltage value, which is slightly larger than V_{CEsat}, the gate driver module turns off the IGBT and outputs an error signal (the desat signal shown in Figure 6.1) to the protection board.

Two electrolytic capacitors (C_{DC}), having 4700 μF capacitance, 400 V DC voltage rating, and 18 A rms current rating each, are connected in series to form the DC bus

of the PAF system. A bleeding resistor (R_{DC_B}), which has a resistance value of 30 kΩ and a power rating of 10 W, is connected across each DC bus capacitor as shown in Figure 6.2 to balance the charges of DC bus capacitors and to discharge these capacitors when the PAF system is turned off.

In the PAF system, the load currents, PAF currents, line voltages and PAF DC bus voltage are measured for control and protection purposes. The load currents and PAF currents are measured by utilizing hall-effect current sensors, which are LA 55-P/SP1 manufactured by LEM. Voltage measurement transformers manufactured by SEDA are utilized to measure the AC line voltages. The DC bus voltage of the PAF system is measured by utilizing the hall-effect based isolated voltage sensor, LV25-P model manufactured by LEM. All the measured signals, load currents, PAF currents, line voltages and PAF DC bus voltage are scaled and filtered by utilizing basic operational amplifier circuits and passive noise filters in the signal conditioning board. The signal conditioning board provides the measured signals at the required voltage level (between 0 and 3 V) for the DSP unit. The PAF currents measurement is also utilized for overcurrent protection of the PAF system. The scaled and filtered filter current sensor output, which is named as the overcurrent signal in Figure 6.1, is also supplied to the protection board. The protection board monitors the overcurrent and desat signals. If an error does not occur, it enables the IGBT gate signals to be applied to the IGBT gate driver board. If a fault occurs, all IGBT gate signals are set to 0 level so that the inverter is disabled. This mode of the inverter is named as the base block state of the inverter.

A DSP unit is utilized in the experimental system to control the PAF system and to generate IGBT gate signals. In the DSP unit, analog to digital (A/D) conversion, general purpose input output (GPIO), control block calculation, and PWM output signal generation functions are carried out. In the experimental set-up, the eZdsp F2812 starter kit manufactured by Spectrum Digital is employed for DSP unit. The starter kit includes the TMS320F2812 DSP manufactured by Texas Instruments. Table 6.2 summarizes the main features of TMS320F2812 DSP [42].

Table 6.1 Specifications of the SKM 75GB128D model IGBT module to be utilized in the manufactured PAF system

IGBT of the dual module		
V_{CES}	Collector-emitter blocking voltage rating	1200 V
I_C	Continuous collector current rating (rms) (at 25 ^oC)	100 A
V_{CEsat}	Collector-emitter saturation voltage at 50 A (at 25 ^oC)	1.9 V
$t_{d(on)}$	Turn-on delay time at I_C = 50 A (R_{gate} = 6Ω)	160 ns
t_r	Rise time at I_C = 50 A (R_{gate} = 6Ω)	35 ns
$t_{d(off)}$	Turn-off delay time at I_C = 50 A (R_{gate} = 6Ω)	310 ns
t_f	Fall time at I_C = 50 A (R_{gate} = 6Ω)	65 ns
C_{ies}	Input capacitance (at 25 ^oC)	4.5 nF
C_{oes}	Output capacitance (at 25 ^oC)	0.6 nF
C_{res}	Reverse transfer capacitance (at 25 ^oC)	0.55 nF
Diode of the dual module		
V_F	Forward voltage drop at I_F = 50 A (at 25 ^oC)	2 V
I_{RRM}	Peak reverse recovery current at I_F = 50 A (at 25 ^oC)	55 A
Q_{rr}	Recovered charge at I_F = 50 A (at 25 ^oC)	7.3 µC
SKHI 22B Gate Driver Module		
V_S	Supply voltage primary side	15 V
I_{SO}	Supply current primary side (no-load/max.)	80/290 mA
V_I	Input signal voltage ON/OFF	5/0 V
V_{IT+}	Input threshold voltage (High)	3.7 V
V_{IT-}	Input threshold voltage (Low)	1.75 V
R_{in}	Input resistance	3.3 kΩ
$V_{G(on)}$	Turn-on gate voltage output	+15 V
$V_{G(off)}$	Turn-off gate voltage output	-7 V
t_{TD}	Top-Bottom interlock dead-time min. / max.	no interlock/4.3 µs

Table 6.2 Main features of TMS320F2812 DSP

Operating Frequency	150 MHz
Clock and System Clock	• On-Chip Oscillator • Watchdog Timer • Dynamic PLL Ratio Changes Supported
Central Processing Unit (CPU)	32-bit high performance CPU
On-Chip Memory	• 128K×16 Flash Memory • 18K×16 RAM • 1K×16 One-Time Programmable ROM
Timers	Three 32-Bit CPU Timers
Motor Control Peripherals	Two Event Manager (EVA, EVB)
Analog-Digital Converter(ADC)	• 12-Bit ADC • 16 Channels • Fast Conversion Rate: 80ns/12.5 MSPS
General Purpose Input/Output	Up to 56 Pins
External Interface	• Up to 1M Total Memory • Three Individual Chip Selects
Serial Port Peripherals	• Serial Peripheral Interface • Two Serial Communications Interfaces • Enhanced Controller Area Network • Multi-channel Buffered Serial Port

The systems and control algorithms are all time-based procedures. The DSP has a power hardware module called ‘Event Manager’ (EV), which is able to deal with time-based procedures, the systems and control algorithms. The event manager produces time based digital hardware signals directly from an internal time event, which is determined by the event manager timer unit. This signal is digital pulse with binary amplitude, ‘0’ or ‘1’. The frequency and/or pulse width of these pulses is modified to create PWM modulation signals by EV logic. Moreover, the internal time events create regular interrupts, in which control algorithms (system codes) are implemented and are executed regularly in time.

One of the DSP’s two event manager, ‘Event Manager A’ (EVA), which is able to generate 6 PWM (PWM1, PWM2… PWM6) signals and 4 interrupts [43], is employed to control the PAF system. The timer 1 counter (T1CNT) of EVA is set to continuous up/down to create symmetric PWM pulses. Counting time of the T1CNT

is determined by period register of timer 1 counter (T1PR), which is uploaded according to the desired switching time. The value for the T1PR is 3750 for up/down counting mode since the DSP system clock is 6.67 ns and switching period is 50 μs in this application. Three compare registers of EVA (CMPR1, CMPR2 and CMPR3) continuously compared to T1CNT for PWM pulse generation. Each compare register is responsible from the generation of two complementary pulses to be utilized by each IGBT module constituting an inverter leg in the VSI in a three-phase application. For example, if CMPR1 value first time matches T1CNT value in a period, PWM1 signal is pulled up to the high logic level while PWM2 is pulled down to low logic level. When a second match of CMPR1 and T1CNT occurs, PWM1 signal is pulled down to the low logic level while PWM2 is pulled up to the high logic level in continuous up/down mode. Moreover, a dead-time between the switches in the same inverter leg, which EVA is able to create, is implemented as 2.56 μs, which corresponds to 384 cycles of the system clock. Similarly, complementary pulses for other IGBT modules in the VSI are employed by using CMPR2 and CMPR3 registers. Figure 6.5 illustrates the generated outputs (PWM1 and PWM2) and dead-times for a CMPR1 value of 1875. Also figure illustrates four generated interrupts of the EVA: two compare match interrupts occur when T1CNT value is equal to CMPR1 value, a period occurs when T1CNT value is equal to T1PR (T1PR = 3750 in this case) and an underflow interrupt occurs when T1CNT is equal to zero. The illustration of these interrupts will simplify the understanding of the flow of the control algorithm later.

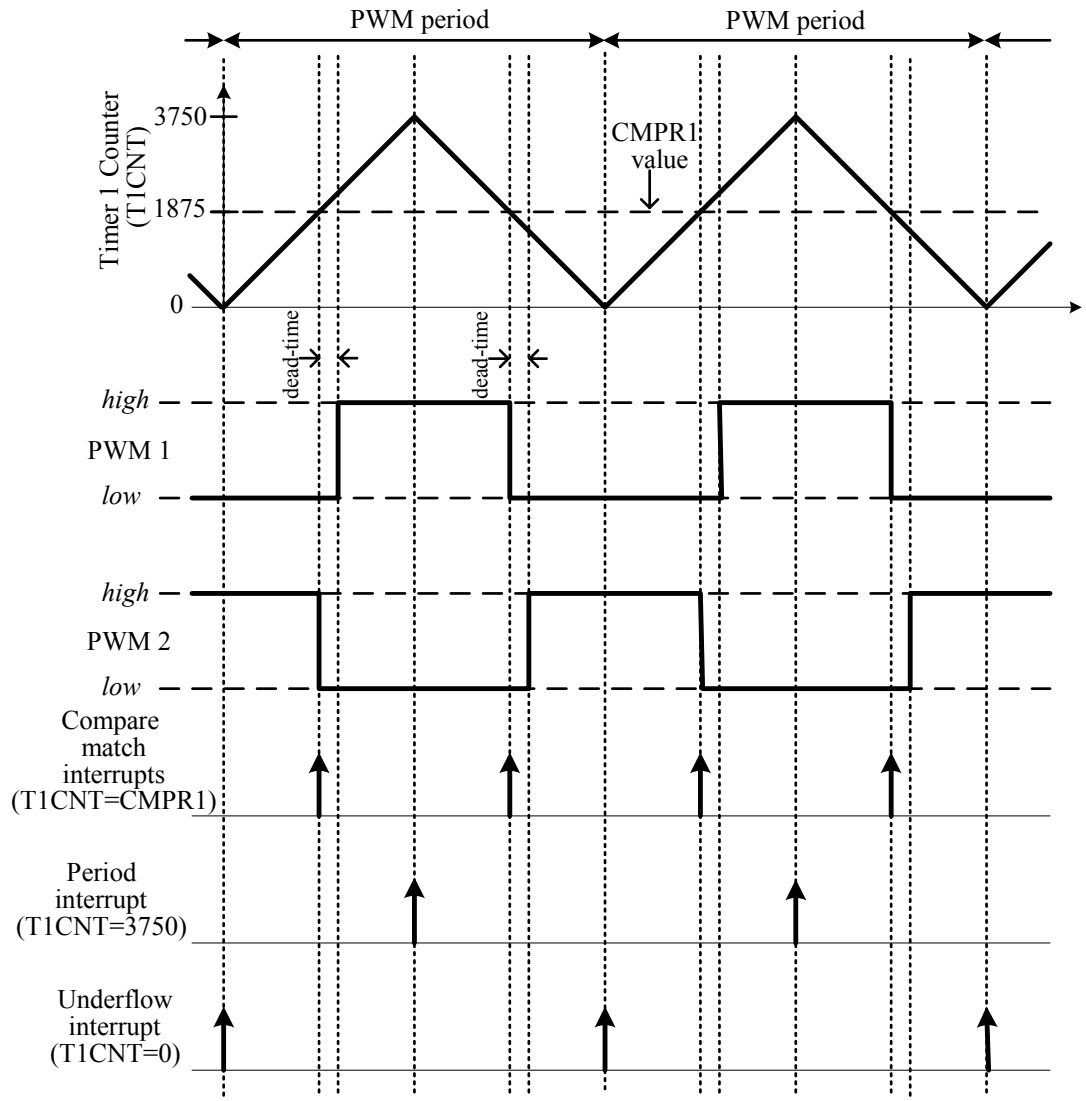

Figure 6.5 Generated PWM signals and interrupts by EVA hardware module of DSP.

The control algorithm, which is written in C programming language, implemented in the DSP unit is executed once in every switching cycle by using the interrupts of the EVA. However, a different control algorithm and different number of interrupts are utilized for linear current regulators and on-off current regulators since the switching signal updates and sampled feedback and control quantities in a period of T_S are different for two types of current regulators as discussed in the Chapter 3 and the Chapter 5.

Discrete time implemented linear current regulators, LPCR and RFCR, utilize two interrupts; EVA timer 1 underflow interrupt (T1UFI) and period interrupt (T1PRI). At each time, when T1UFI occurs, the program code in that interrupt is executed. Once the execution of the program code in the T1UFI time interval is completed, the program code in the T1PRI time interval is waited to be executed with the request of T1PRI. When T1PRI is requested, the program in that interrupt is executed. The T1UFI request is waited with the completion of the program code in T1PRI time interval. The execution of the control algorithms repeats itself in time.

Figure 6.6 illustrates two interrupts created, and the sampled quantities for the implemented linear current regulators. Moreover, Figure 6.7 illustrates the flow chart of the control algorithm for linear regulators. The flow of the system code is as follows: At the beginning of T1UFI, the analog digital conversion (ADC) operation is performed. Three line voltages (V_{FA}, V_{FB}, V_{FC}) to be utilized in the PLL block and current regulator block as feed-forward signals and the DC bus voltage of the PAF to be utilized in the DC bus voltage regulator block are sampled. The program waits until the ADC finishes. Then the PAF circuit breaker on-off signal (FBCS) is checked whether it is '1' or '0'. If it is '1', the PAF circuit breaker is on, and program continues. Otherwise it is off, the base block command is set to '1' in order to avoid the IGBTs from being fired on by the DSP. The FBCS signal is initially set to zero. If the PAF is to be started, the signal is set to one to control the system operation manually to avoid any mistakes during start-up procedure. Then the line voltage check signal (LVCS) created by checking the line voltage whether the line voltage vector is below 20% of its rate value or not is checked. If the line voltage vector is above 80% of its rated value, the LVCS is set to one and the program continues, otherwise it is set to zero and the system is directed to the base block state and the FBCS is set to zero to turn off the PAF circuit breaker or to hold it in off position. Then the maximum allowable DC bus voltage (V_{DCmax}) check is performed. The V_{DCmax} value is set to 750 V in this application, while the rated DC bus voltage ($V_{DCrated}$) is determined as 700 V. If V_{DC} is greater than 750 V, the FBCS and the pre-charge circuit breaker on-off signal (PCS) are set to zero, and the system is directed to base block state. If it is below the V_{DCmax} value, FBCS is set to one and

leading the program to the minimum DC bus voltage required turning on pre-charge circuit breaker (V_{DCmin}) check. The V_{DCmin} value is set to 400 V in this application. If V_{DC} is below the V_{DCmin}, PCS is set to zero to hold the pre-charge circuit breaker in its off state and the system is still held in base block state. If it is above V_{DCmin}, the PCS is set to one to by-pass the pre-charge resistors. In order to start PWM operation, V_{DC} is to be greater than the minimum value of DC bus voltage to start PWM operation of PAF (V_{DCpwm}). If it is not, the program holds the system in base block state. If it is greater than V_{DCpwm}, base block command is set to zero, which means that system is ready to start PWM operation. Then the PLL calculations for the SRFC to generate the line voltage angular frequency and the operation of the DC bus voltage regulation block which creates the current reference to regulate DC bus of PAF (I^*_{Fdc}) take place. The zero output command of the base block is not the only command to allow the PWM operation of the PAF. The externally given START command is to be set to one to start PWM operation. This is done due to control purposes at the start-up of the system. At the end of T1UFI, if the base block command is zero and START command is one, the program enables the PWM signals, and waits for the T1PRI.

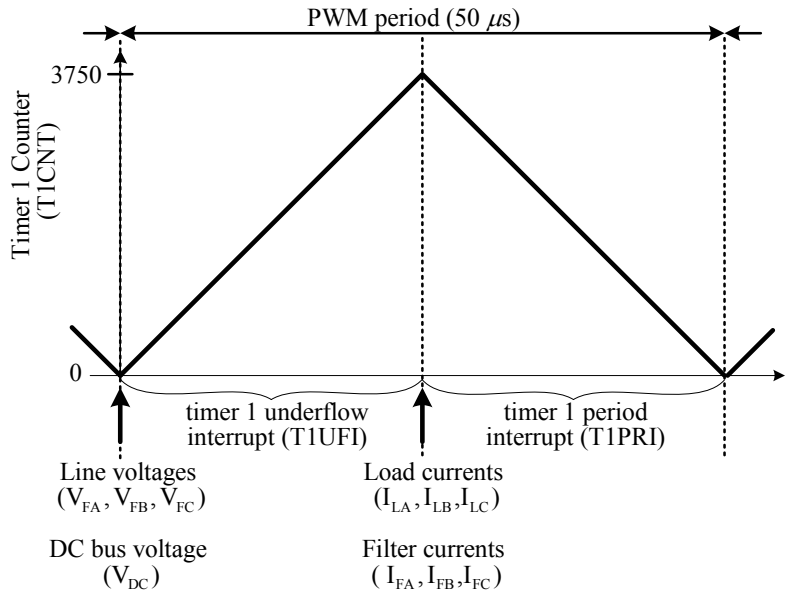

Figure 6.6 Generated interrupts and sampled quantities for linear current regulators.

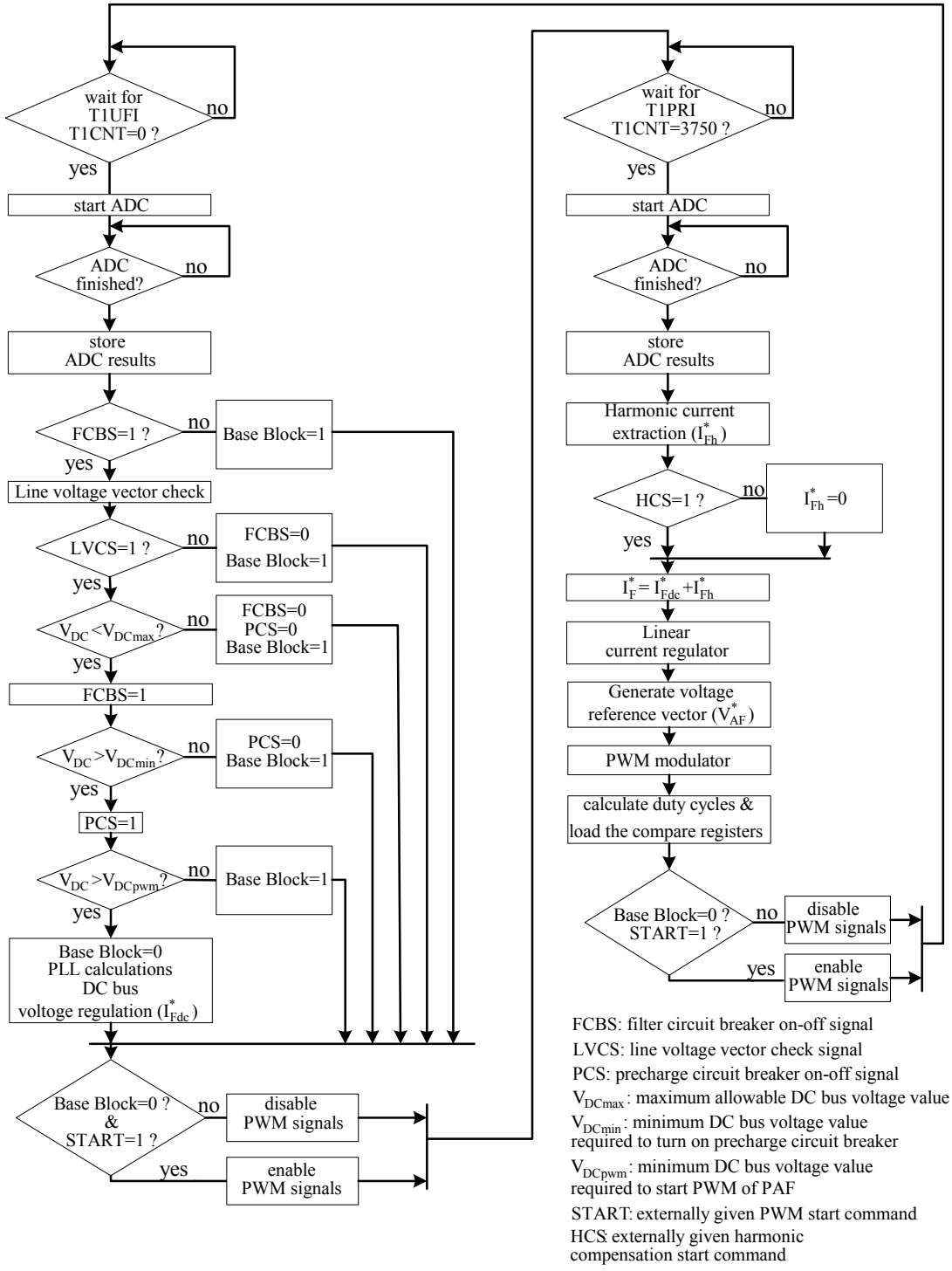

Figure 6.7 Flow chart of the main program code for linear current regulators.

When T1PRI request is encountered, the ADC starts and the load currents (I_{LA}, I_{LB}, I_{LC}) to be utilized in the reference signal generator block and the filter currents (I_{FA}, I_{FB}, I_{FC}) to be utilized in the current regulator block are sampled. After the ADC is ended, the harmonic reference generator utilizing the SRFC creates the harmonic, the fundamental reactive power, and the negative sequence current component (I^*_{Fh}) for the PAF. If the externally given harmonic compensation start command (HCS) is zero, I^*_{Fh} is set to zero to avoid harmonic compensation. Otherwise, I_{Fh} is taken as which value it has. Then I^*_{Fh} and I^*_{Fdc} signals are added to create total harmonic current reference of PAF (I^*_F). I^*_F together with the sampled filter currents constitutes the input of current regulator block. Then the current regulator calculations take place based on the utilized current regulator type. Once the voltage reference (V^*_{AF}) is generated via a current regulator, it is evaluated by the PWM modulator and the duty cycle information of the switches are created and loaded to three compare registers of EVA for PWM operation. At the end of T1PRI, the base block and START command check is performed to decide whether PWM signals will be enabled or not.

The implemented hysteresis current regulators, DHCR2 and DHCR3, utilize four interrupts; EVA T1UFI, T1PRI, timer 2 underflow interrupt (T2UFI) and timer 2 period interrupt (T2PRI). The reason of utilization of four interrupts is that the sampling frequency of the filter currents is different in DHCR2 and DHCR3 to decrease measurement delay and maximum output delay as discussed in Chapter 3. Figure 6.8 illustrates four interrupts created by the EVA, and the sampled quantities for the implemented discrete time hysteresis current regulators. Timer 1 counter and Timer 2 counter are synchronized to obtain the counter waveforms shown in Figure 6.8. Timer 1 interrupt has higher priority than timer 2 interrupt and timer 1 counter is utilized for PWM signal generation [43]. Therefore, timer 1 interrupts are utilized for the hysteresis current regulator block operations and the switch on-off signals, while timer 2 interrupts are utilized for the control purposes and the reference signal generation.

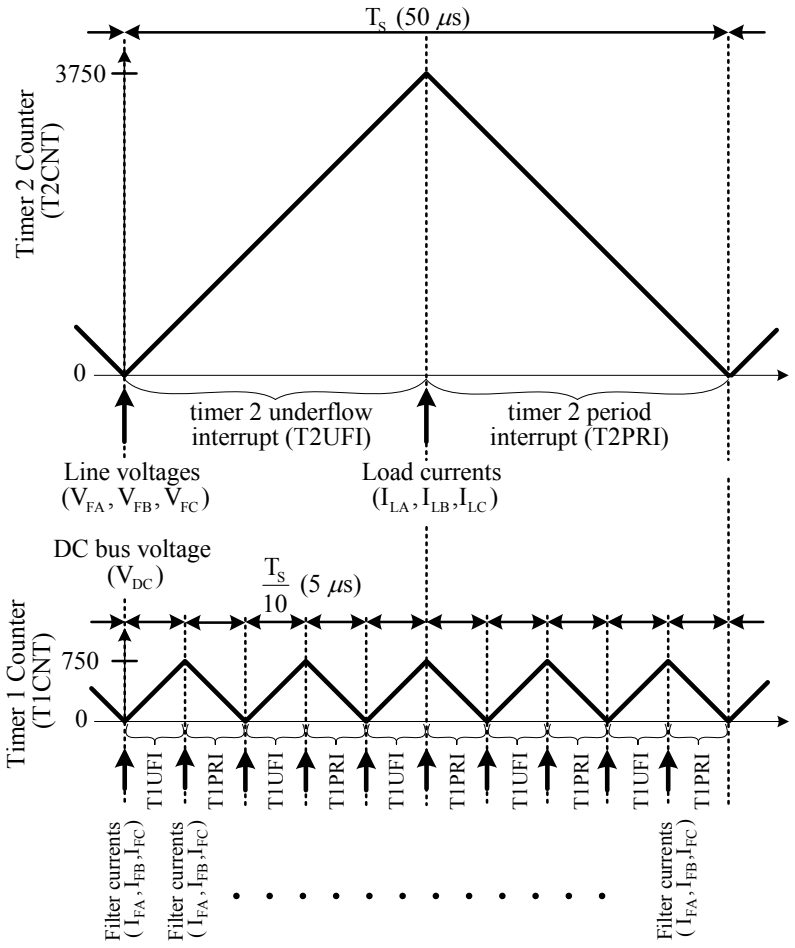

Figure 6.8 Generated interrupts and sampled quantities for on-off current regulators.

Since the sampling frequency for the line voltages, the DC bus voltage and the load currents is 20 kHz, timer 2 period register is set 3750 for system clock of 6.67 ns as in the linear current regulator program algorithm. However, the sampling frequency for filter currents is 200 kHz for a sampling coefficient K of 10. The filter currents are sampled both at the beginning of T1UFI and T1PRI as shown in Figure 6.8, the timer 1 counter period register is set to 750. The flow chart of the timer 2 interrupts is shown Figure 6.9. The program flow algorithms and the check quantities are the same as in the linear current regulator program algorithm. However, the base block and START command check block at the end of T1UFI and T1PRI for the linear current regulator program algorithm is removed to the end of the T1UFI and T1PRI for the hysteresis current regulator program algorithm since the current regulator and

switching decision block of the discrete hysteresis current regulators are implemented in T1UFI and T1PRI as mentioned earlier. The flow chart of program code for the discrete time hysteresis current regulator and switching decision block implemented in T1UFI and T1PRI is shown in Figure 6.10. Note that the program code for T1UFI and T1PRI is same. The program starts with the ADC. Then the hysteresis current regulator block takes places and the switching decision block decides the final values of switch on-off signals based on the restrictions mentioned in Chapter 3 for the DHCR2 and DHCR3. At the end of the interrupt, the base block and START command check block exists to decide whether the PWM signals are to enabled or not. Although the generated output signals of the hysteresis current regulator are not PWM signals, but on-off signals, the reason that they are named PWM signals for the hysteresis current regulator is utilization of compare register and counter match logic in DSP. The loaded value to the compare register is 0 while creating a switch on signal in DSP, as a result PWM1 is pulled up to high logic level. The loaded value to the compare register is period register value (750 in this case) while creating a switch off signal in DSP, as a result PWM1 is pulled down to low logic level. At each time the program code execution in the T1UFI or the T1PRI is completed, the execution of the main program code implemented in T2UFI and T2PRI is continued.

The program algorithm repeats itself regularly in time. The generated PWM signals are transferred from the DSP unit to the gate driver board via the level shifter electronic board. The level shifter board shifts the high logic voltage level of the PWM signal output of the DSP unit, which is 3.3V, to the required voltage level for the gate driver modules, which is 5 V. As described earlier, the protection board must enable the level shifter to operate. If an error (either overcurrent or desat) occurs in the converter system, the output signals of the level shifter board are all set to low voltage level (0 V) due to the disable signal generated by the protection board. Meanwhile, the DSP unit still continues to output the PWM signals. The PWM signal outputs of the level shifter board are transferred to the gate driver board, which is discussed earlier.

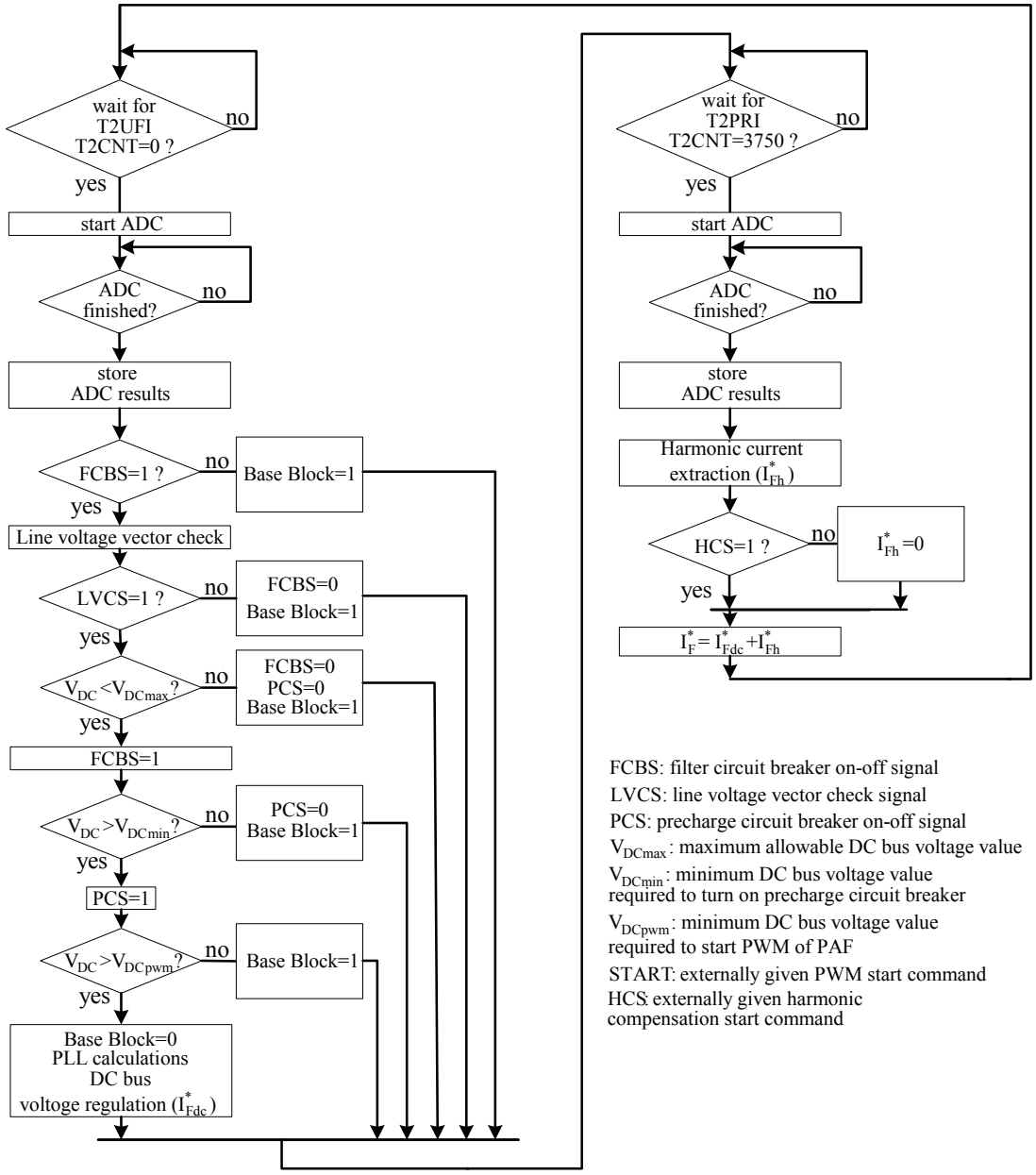

Figure 6.9 Flow chart of the main program code for hysteresis regulators.

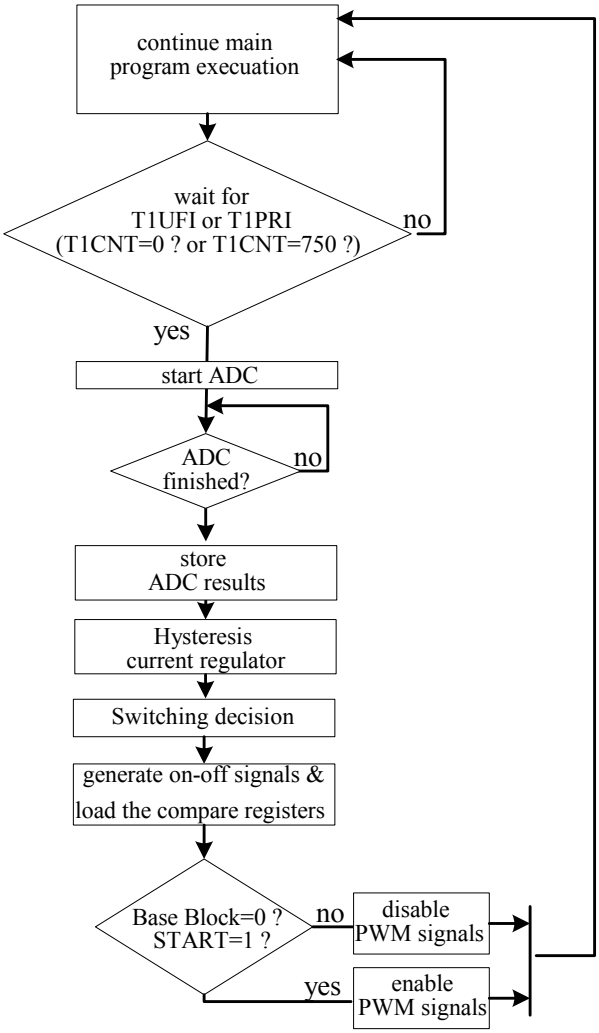

Figure 6.10 Flow chart of the program code utilized for hysteresis regulators.

The PAF and pre-charge circuit breaker on-off signals explained in the program algorithm are digital output signals, which are employed by the utilization of GPIO feature of the DSP. These outputs are sent to the circuit breaker driver board. Once these signals are isolated by optocouplers, they are transferred to bipolar junction transistors (BJTs) utilized as on-off switches for the relays that transfer or block 220 V AC voltage needed for turning on or turning off of the circuit breakers.

6.3 Illustration of The Experimental PAF Basic Performance Utilizing The LPCR

This section gives the basic experimental results of the PAF system utilizing the LPCR without SRF and designed for harmonic current and reactive current component compensation of three-phase diode rectifier load with 10 kW output power. The experimental waveforms are obtained with LeCroy WaveRunner 500 MHz oscilloscope [44]. The harmonic analysis of currents and voltages during experiments is obtained with ZesZimmer Power Quality Analyzer [45]. The power quality analyzer calculates THD_I and THD_V values according to the harmonic component percentages up to the 100^{th} harmonic order. Since the SRF is not included in the PAF system for this section, the switching ripple voltages and currents are present at the AC line terminals. However, the switching ripple harmonics are far above the 100^{th} harmonic order. Therefore, the contribution of the switching ripple currents and voltages to the THD values is not observable by the measurements with ZES. The system parameters for the experimental set-up are the same as those in the computer simulation and will not be repeated in this chapter.

The hardware description of the experimental test set-up was provided in the previous section. Moreover, the IEEE 519 limits for the system were determined in Chapter 5. Thus, directly the experimental results will be reported in this section. The experimental line current harmonics, line current THD_I, line voltage THD_V, and PF at the PCC is to be determined first for the case where the designed PAF system is not enabled. Figure 6.11 illustrates the line voltage at the PCC and line current, in order words, the load current of diode rectifier load with the output power of 10 kW when the PAF system does not connected at PCC. The line current harmonics, line current THD_I, line voltage THD_V, and PF at PCC are summarized in Table 6.3. The experimental harmonic spectrum of the load current is illustrated in Figure 6.12. Based on the data in Table 6.3, the THD_I value of the load current is 37.7%, which is above the IEEE 519 limit of 15% for the I_{SC}/I_L of 173, and the THD_V value at PCC is %2.4. The reason the values for THD_I and THD_V are slightly high compared to the THD_I and THD_V values in Table 5.2 for the computer simulation is that the

harmonics existing on the line voltage. The experimental set-up is supplied from AC utility grid where many computer loads in the METU campus are supplied. The harmonics they create results in line voltage distortion which affects the operation of the other linear/nonlinear loads as in this case. Also the wiring of the laboratory power system involves thin wires not able to support large currents and as a result with large load currents the voltage waveform gets flat top at the peak current regions. The nonsinusoidal shape of the line voltage is obvious from Figure 6.11. Moreover, the THD_V value at PCC differs in value during the time intervals of the day. For instance, the THD_V has higher values during the working hours while it has lower values at the night. However, in the computer simulations, the AC utility grid is assumed ideal. Therefore, the harmonic current components of the load current in the experiment, which are listed in Table 6.3 are above the ones in the computer simulation listed in Table 5.2.

The 5^{th}, 7^{th}, and 11^{th} harmonic current components of the load current in the experiment are above the limits mentioned in Table 6.3 as in the computer simulation section in Table 5.2. The PF value at the PCC is 0.92 lagging. With the implementation of the PAF at PCC, the harmonic, the reactive power, and the negative sequence current compensation of the diode rectifier load will be performed as in the computer simulation part. The basic performance analysis and experimental waveforms of the PAF system utilizing LPCR are presented as in the computer simulation part. Since the design of the PAF system and the current regulators is performed in the previous chapters, the parameters with control blocks and the system will not be discussed again. Moreover, the performance of the current regulators will be presented by means of the THD_I, THD_V, PF at PCC, f_{AVG}, and the line current harmonic components after PAF is connected to the PCC and the line current harmonic components is compared to IEEE 519 harmonic limits up to 50^{th} harmonic as in the computer simulation chapter.

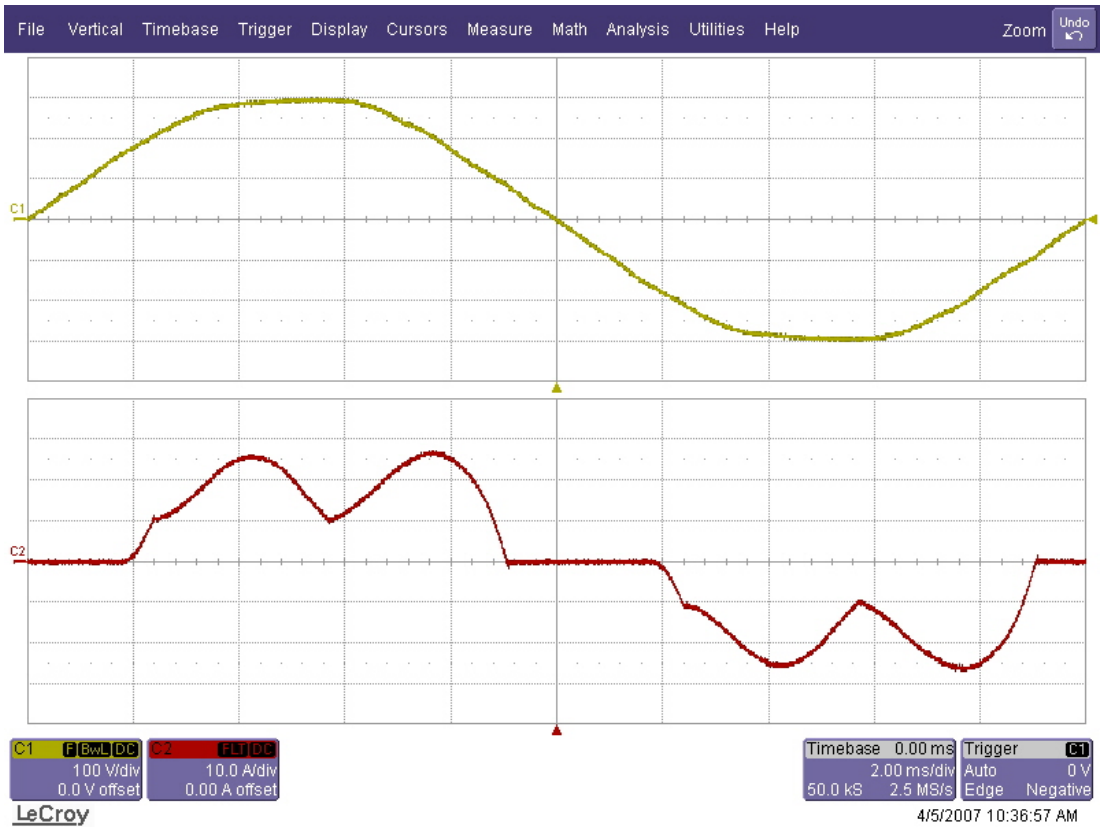

Figure 6.11 The experimental waveforms of the line voltage at the PCC (yellow, 100V/div) and the load current (red, 10 A/div), (time axis: 2 ms/div).

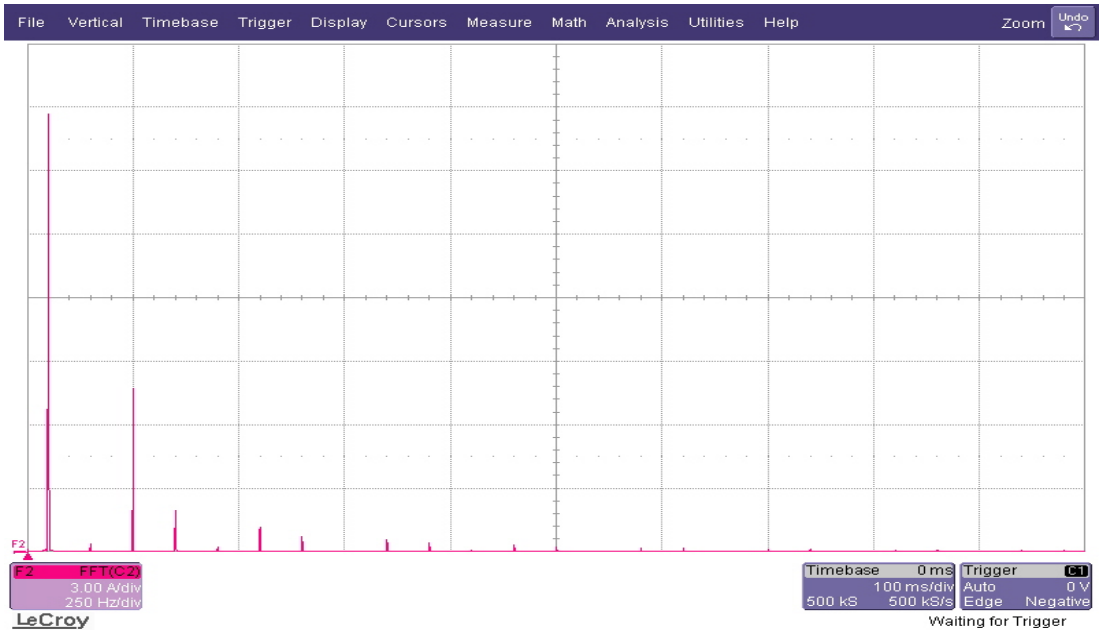

Figure 6.12 The experimental load current harmonic spectrum of the diode rectifier load (scales: 3 A/div, 250 Hz/div).

Table 6.3 The experimental line current harmonics, THD_I, THD_V, PF at PCC of the diode rectifer load, and IEEE 519 limits

	Line Current Harmonics without PAF (%)	IEEE 519 Harmonic Current Limits for I_{SC}/I_{L1}=173 (%)
I_1	100	100.00
I_5	35.5	12.0
I_7	9.5	12.0
I_{11}	6.5	5.5
I_{13}	3.5	5.5
I_{17}	3.0	5.0
I_{19}	2.0	5.0
I_{23}	1.5	2.0
I_{25}	1.0	2.0
I_{29}	0.8	2.0
I_{31}	0.7	2.0
I_{35}	0.5	1.0
I_{37}	0.4	1.0
I_{41}	0.4	1.0
I_{43}	0.3	1.0
I_{47}	0.4	1.0
I_{49}	0.3	1.0
THD_I (%)	37.5	15.0
THD_V (%)	2.4	5.0
PF	0.920	---

The experimental waveforms for the AC utility grid, diode rectifier load with the output power of 10 kW, and the PAF system utilizing the LPCR with the K_P value of 40, which illustrates the basic PAF performance, are presented in Figure 6.13 and Figure 6.14. Figure 6.13 respectively illustrates experimental waveforms of the voltage at the PCC, the line current, the load current, and the PAF current for phase '*a*' over a time interval of 50 ms. Additionally, Figure 6.14 respectively illustrates experimental waveforms of the voltage at the PCC, the line current, the PAF current for phase '*a*', and the DC bus voltage over a time interval of 50 ms. The steady-state performance of the PAF utilizing LPCR is summarized in Table 6.4. Table 6.4 involves the load current harmonics, line current harmonics, and IEEE 519 harmonic limits up to the 50^{th} harmonic current component. Moreover, it involves THD_I, THD_V, PF, and f_{AVG} for LPCR as in the computer simulations. According to the table, all the current harmonics are well below the IEEE 519 limits and the load current

harmonics are suppressed up to the 35th harmonic. The line current waveform in Figure 6.13 and Figure 6.14 is nearly sinusoidal with THD_I value of 4.0%, which illustrates that the PAF system satisfactorily performs the harmonic current compensation. Moreover, the line current is in phase with line voltage in Figure 6.13 and Figure 6.14 that results in a PF value of 0.997, which illustrates that the reactive current compensation capability of the PAF system. The THD_V value at the PCC is 2.4%. The THD_I and THD_V values obtained in experimental studies are lower than the values obtained in computer simulation part (Table 5.4). The reason is that the THD_I and THD_V values obtained in experimental studies do not include the switching frequency harmonic components as mentioned at the beginning of Section 6.3. Since DPWM1 is utilized as PWM modulator, the f_{AVG} value is 13.3 kHz for the selected carrier frequency of 20 kHz. In Figure 6.14, the DC average bus voltage of the PAF is kept at its reference voltage value of 700 V. This illustrates that the PAF DC bus voltage regulation is performed satisfactorily. The 300 Hz ripple on the DC bus voltage waveform results from the dominant 5th and 7th harmonics current components existing in filter current. Figure 6.13, Figure 6.14, and Table 6.4 clearly illustrate experimentally that the PAF system utilizing LPCR satisfactorily performs the compensation of the load current harmonics, the reactive power current component, and DC bus regulation of the PAF.

As Figure 6.13, Figure 6.14, and Table 6.4 illustrate the PAF basic performance, the performance of the utilized current regulator for PAF system can be observed by analyzing the line current and the PAF current in detail. The experimental line current and PAF current waveforms are illustrated in detail in Figure 6.15 for the PAF system utilizing LPCR. Since the current reference for the PAF is an internal digital variable of the DSP and could not be output as an analog variable from the DSP, it could not be observed in the oscilloscope. Therefore, the tracking performance of the current regulator could not be directly observed through the oscilloscope (though it could be observed via the computer screen and utilizing the code composer software). For this reason, the tracking performance of the current regulator could be best observed from the line current. The closer the line current to a sine, the better the tracking of the current regulator. The line current and the PAF

current are quite similar to those obtained in the computer simulation part and the line current has spikes existing at six times the line frequency resulting from the tracking performance degradation of the current regulator. The line current harmonic spectrum in Figure 6.16 is included to provide a visualization of the switching ripple currents created by the LPCR. The harmonic spectrum of the line current illustrates a dominant switching ripple at the carrier frequency of 20 kHz as illustrated in the computer simulation.

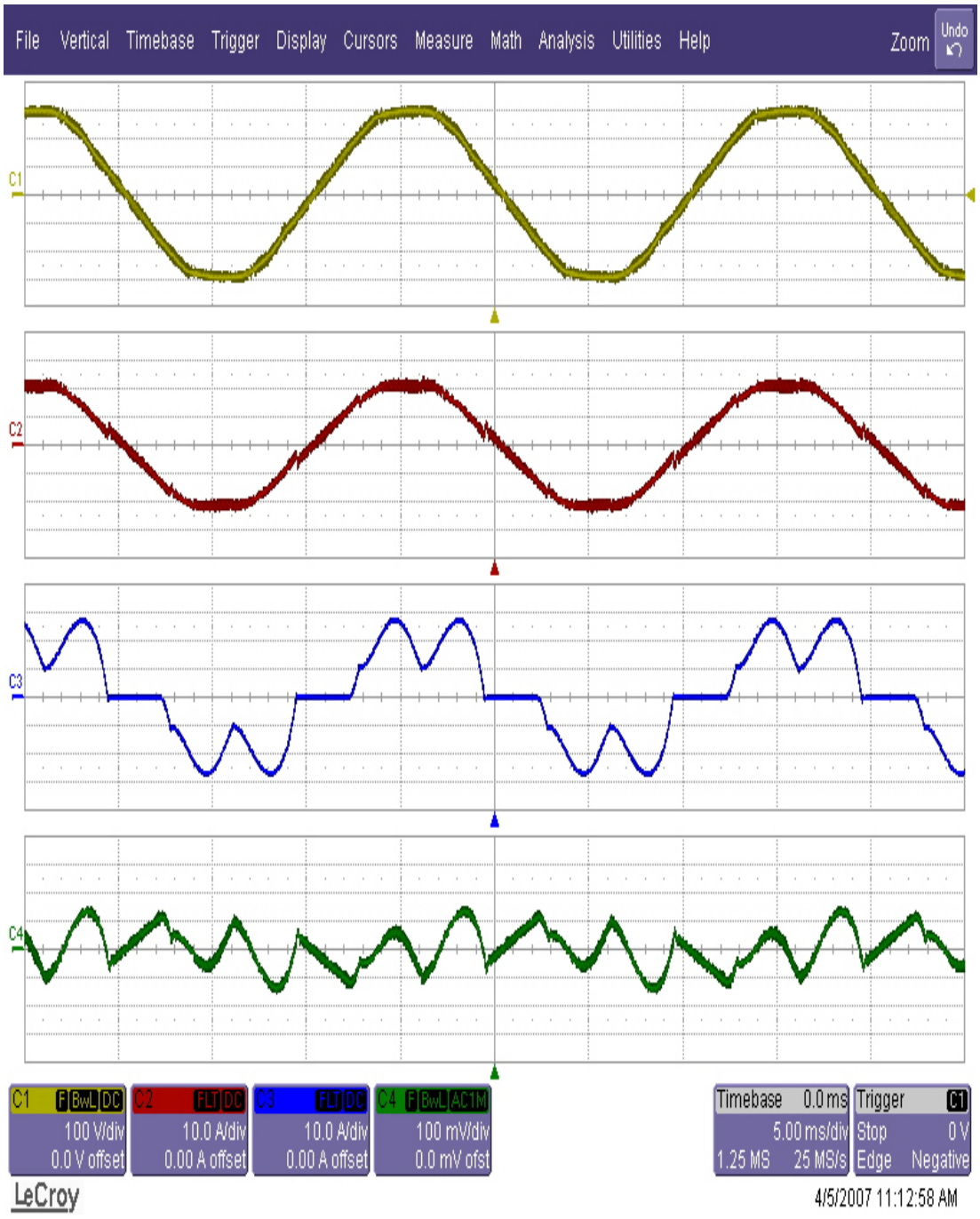

Figure 6.13 The experimental waveforms of the PAF system utilizing the LPCR without SRF: line voltage (yellow, 100 V/div), line current (red, 10 A/div), load current (blue, 10 A/div), and the PAF current (green, 10 A/div) (time axis: 5 ms/div).

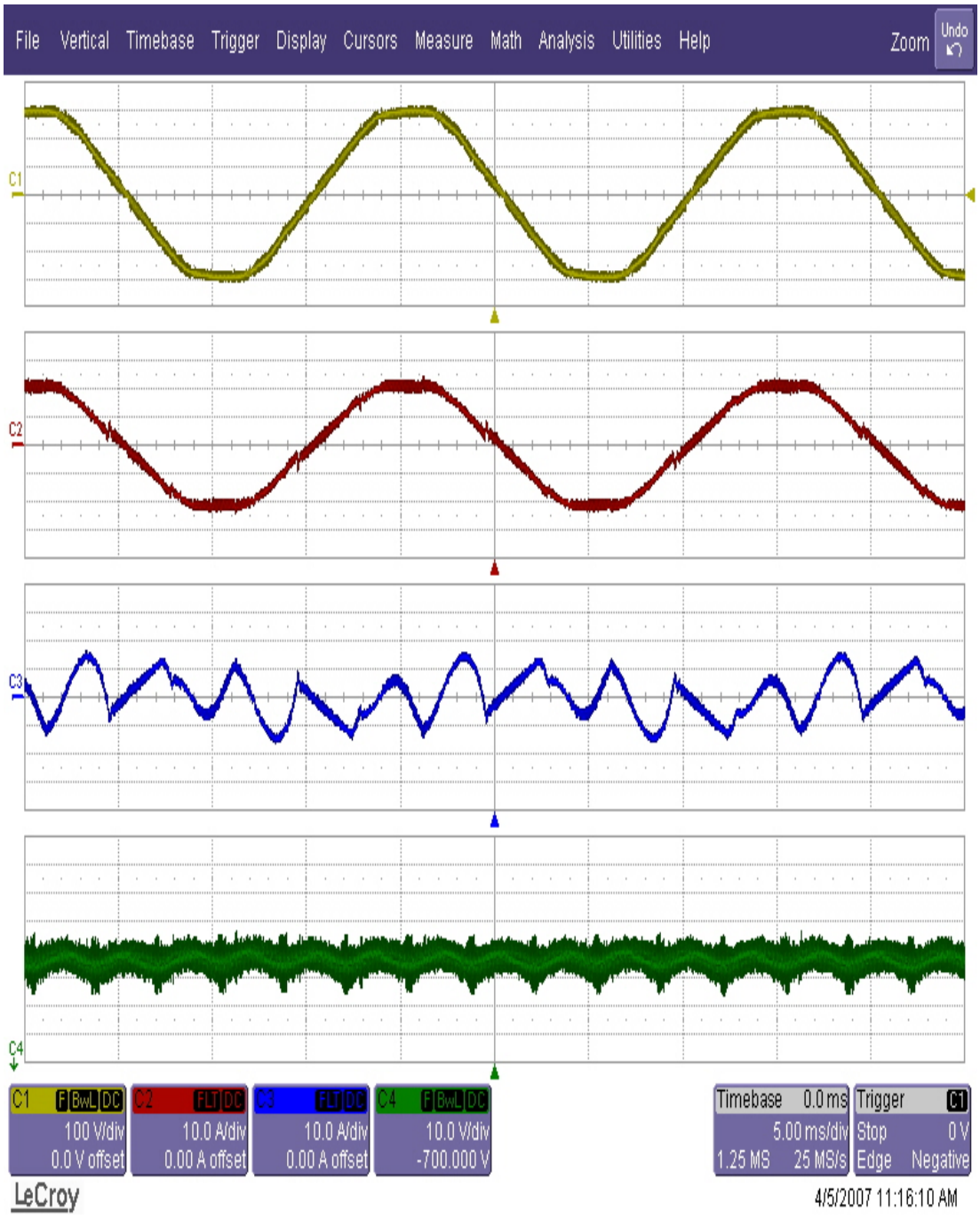

Figure 6.14 The experimental waveforms of the PAF system utilizing the LPCR without SRF: line voltage (yellow, 100 V/div), line current (red, 10 A/div), PAF current (blue, 10 A/div), and PAF DC bus voltage (yellow, 10 V/div, -700 V offset) (time axis: 5 ms/div)

Table 6.4 The experimental line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for LPCR, and IEEE 519 limits

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%)	IEEE 519 Harmonic Current Limits for I_{SC}/I_{L1}=173 (%)
I_1	100.0	100.0	100.0
I_5	35.5	2.8	12.0
I_7	9.5	1.0	12.0
I_{11}	6.5	1.1	5.5
I_{13}	3.5	0.9	5.5
I_{17}	3.0	0.8	5.0
I_{19}	2.0	0.5	5.0
I_{23}	1.5	0.6	2.0
I_{25}	1.0	0.5	2.0
I_{29}	0.8	0.4	2.0
I_{31}	0.7	0.4	2.0
I_{35}	0.5	0.3	1.0
I_{37}	0.4	0.3	1.0
I_{41}	0.4	0.3	1.0
I_{43}	0.3	0.3	1.0
I_{47}	0.4	0.3	1.0
I_{49}	0.3	0.3	1.0
THD_I (%)	37.5	4.0	15.0
THD_V (%)	2.4	2.4	5.0
PF	0.920	0.997	---
f_{AVG}		13.33	

This section clearly illustrates the experimental PAF basic performance. Moreover, the LPCR performance in PAF application is presented for the designed K_P value of 40. The next section illustrates the performance of the other current regulators analyzed in Chapter 3 and Chapter 5 and a comparison study for the performances of the current regulators will be carried out as in the computer simulation chapter. Since the PAF system basic waveforms are similar for other current regulators, they are not included in this thesis for other current regulators. Only basic results and waveforms such as the line current, filter current, and line current harmonic spectrum which differ in microscopic level for other current regulators, are provided in the next section.

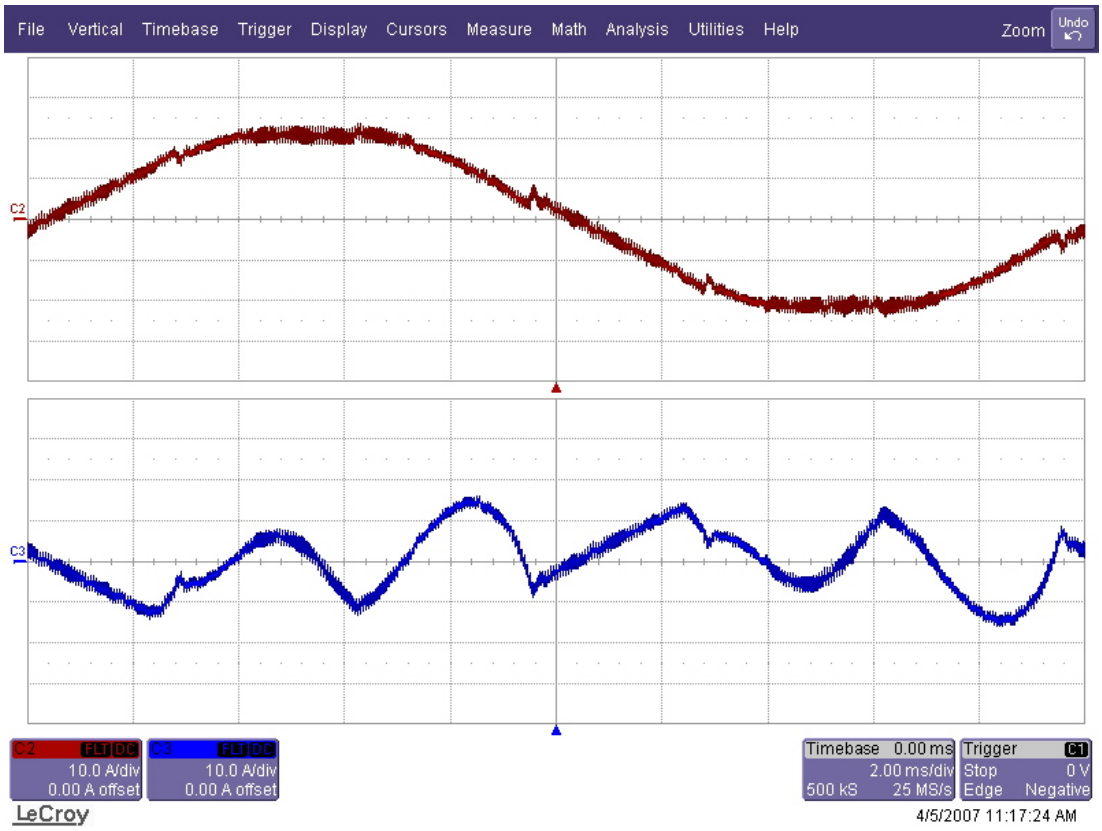

Figure 6.15 The experimental line current (red, 10 A/div) and PAF current (blue, 5 A/div) waveforms for LPCR (time axis: 2 ms/div).

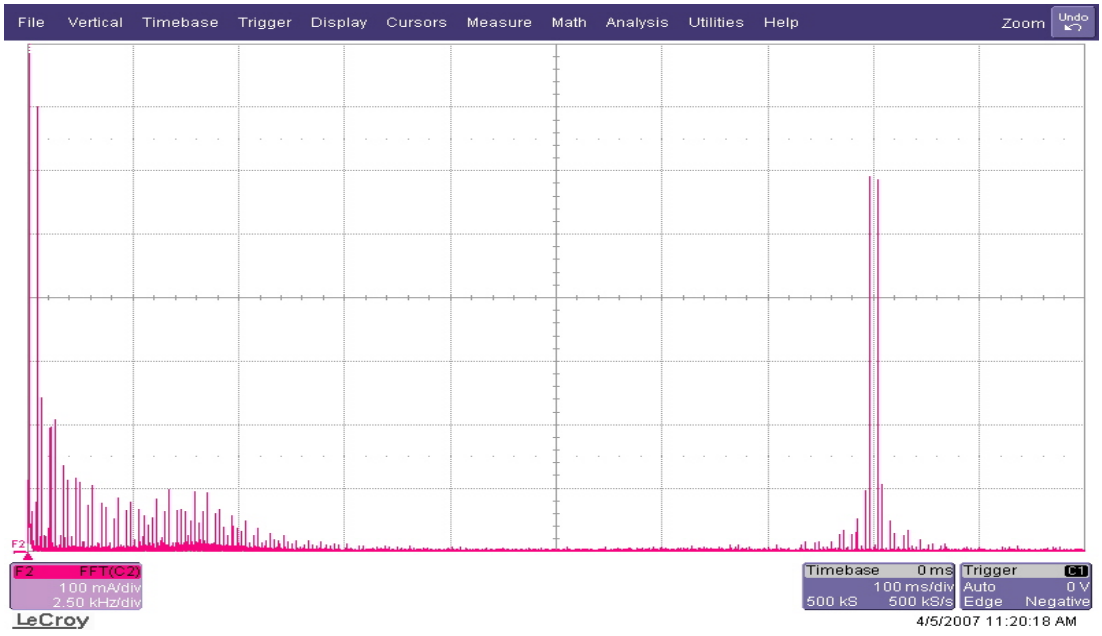

Figure 6.16 The experimental line current harmonic spectrum for LPCR (scales: 100 mA/div, 2.5 kHz/div).

6.4 Performance Comparison of Various Current Regulators by Means of Experimental Studies

The practically available current regulators for the PAF application were analyzed in detail in Chapter 3 and the computer simulation results and the performance comparison of the various current regulators were presented in Chapter 5. In this section, the experimental performances of the current regulators implemented by a discrete time controller are presented since a DSP is utilized for the manufactured PAF system control. Therefore, LPCR, RFCR, DHCR1, DHCR2, and DHCR3 performances are evaluated experimentally and a performance comparison study is carried out for the PAF system without SRF. Although, the DHCR1 implementation is realized for the PAF system utilizing larger filter inductance values, the PAF system with a 2 mH filter inductor and DHCR1 fails in experiments due to its large ripple content, which results in overcurrent error for the system. Therefore, the DHCR1 performance illustration is eliminated in the experimental studies due to its low performance as illustrated in the computer simulation chapter. Moreover, the LPCR performance will not be presented in this section as it is analyzed in the previous section in this chapter.

Throughout the experimental studies for the PAF system without SRF in this section, the f_S for linear current regulators is selected as 20 kHz and T_S is selected as 50 μs for discrete time hysteresis current regulators to achieve f_{MAX} value of 20 kHz as in the computer simulations. Since the f_{MAX} value is same for all current regulators and the SRF is not included for the PAF system, a fair comparison is achieved. Further, the PAF DC bus voltage is 700 V and is kept constant for the current regulators analyzed in this section as in the LPCR case of the previous section.

6.4.1 RFCR Experimental Results

In this subsection, the experimental results of the resonant filter current regulator (RFCR) are presented. In the experimental studies, three resonant filter controller are implemented as parallel structures for the most dominant three harmonic pairs with

k=1, 2, and 3 (5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th}) where the gains of the resonant filter controller are same as in the computer simulation part. In Chapter 3, the value of the proportional gain is determined as 40 based on the desired phase margin of the PAF system. The K_P value of 40 for RFCR is same as the K_P value for LPCR such that a fair comparison will be carried out.

Table 6.5 gives the steady-state performance of the RFCR by including the load current harmonics, line current harmonics, and IEEE 519 harmonic limits up to 50^{th} harmonic current component in addition to THD_I, THD_V, PF, and f_{AVG}. Based on Table 6.5, all the current harmonics are well below the IEEE 519 limits and the load current harmonics is suppressed up to 35^{th} harmonics as in the LPCR case. However, when the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} line current harmonic components for RFCR are compared to the harmonic components in the LPCR case (Table 6.4), the percentage reduction for the mentioned harmonic pair components is noticeable. While the 5^{th} harmonic component is 2.8% for the LPCR, it is 0.5% for the RFCR for the same K_P value. Similarly, while the 7^{th} harmonic component is 1.0% for the LPCR, it is 0.3% for the RFCR. The percentage reduction in 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonics components for the RFCR can be observed by comparing Table 6.4 and Table 6.5. However, the higher order line harmonic current percentages in Table 6.5 for the RFCR are similar to the ones for the LPCR in Table 6.4 utilizing the same K_P value. This percentage reduction in the most dominant harmonic components results in THD_I reduction for RFCR as in the computer simulation part. The THD_I value for the RFCR is 2.3%, which is lower than THD_I value of 4.0% for the LPCR. The THD_V value at the PCC is 2.4% and same as in the LPCR case since the contribution of switching frequency harmonics to THD_V value is not observable in experimental studies due to the ZES measurement limitations. The PF value and the f_{AVG} value are 0.997 and 13.3 kHz as in the LPCR case. Figure 6.17 illustrates the experimentally obtained line current waveform and PAF current waveform. Additionally, Figure 6.18 illustrates the harmonic spectrum of the line current. Compared to the figures in the previous section for LPCR, the ripple content and current spikes on the line current waveform are same as in the LPCR case. If the harmonic spectrum of the line current for the LPCR in 6.16 is compared to the harmonic spectrum of the line

current for the RFCR in Figure 6.18, the superior compensation capability of the RFCR for the most dominant harmonic components (for 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th}) is clear while the most dominant switching harmonic content at 20 kHz for RFCR is approximately equal in magnitude as for LPCR. The current spikes on the line current waveform corresponding the high di/dt region of the current reference is due to the unavoidable tracking degradation of the RFCR as in the LPCR case.

Table 6.5 The experimental line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for RFCR, and IEEE 519 limits

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%)	IEEE 519 Harmonic Current Limits for I_{SC}/I_{L1}=173 (%)
I_1	100.0	100.0	100.0
I_5	35.5	0.5	12.0
I_7	9.5	0.3	12.0
I_{11}	6.5	0.2	5.5
I_{13}	3.5	0.1	5.5
I_{17}	3.0	0.1	5.0
I_{19}	2.0	0.1	5.0
I_{23}	1.5	0.6	2.0
I_{25}	1.0	0.5	2.0
I_{29}	0.8	0.5	2.0
I_{31}	0.7	0.4	2.0
I_{35}	0.5	0.4	1.0
I_{37}	0.4	0.3	1.0
I_{41}	0.4	0.3	1.0
I_{43}	0.3	0.3	1.0
I_{47}	0.4	0.3	1.0
I_{49}	0.3	0.3	1.0
THD_I (%)	37.5	2.3	15.0
THD_V (%)	2.4	2.4	5.0
PF	0.920	0.997	---
f_{AVG}		13.33	

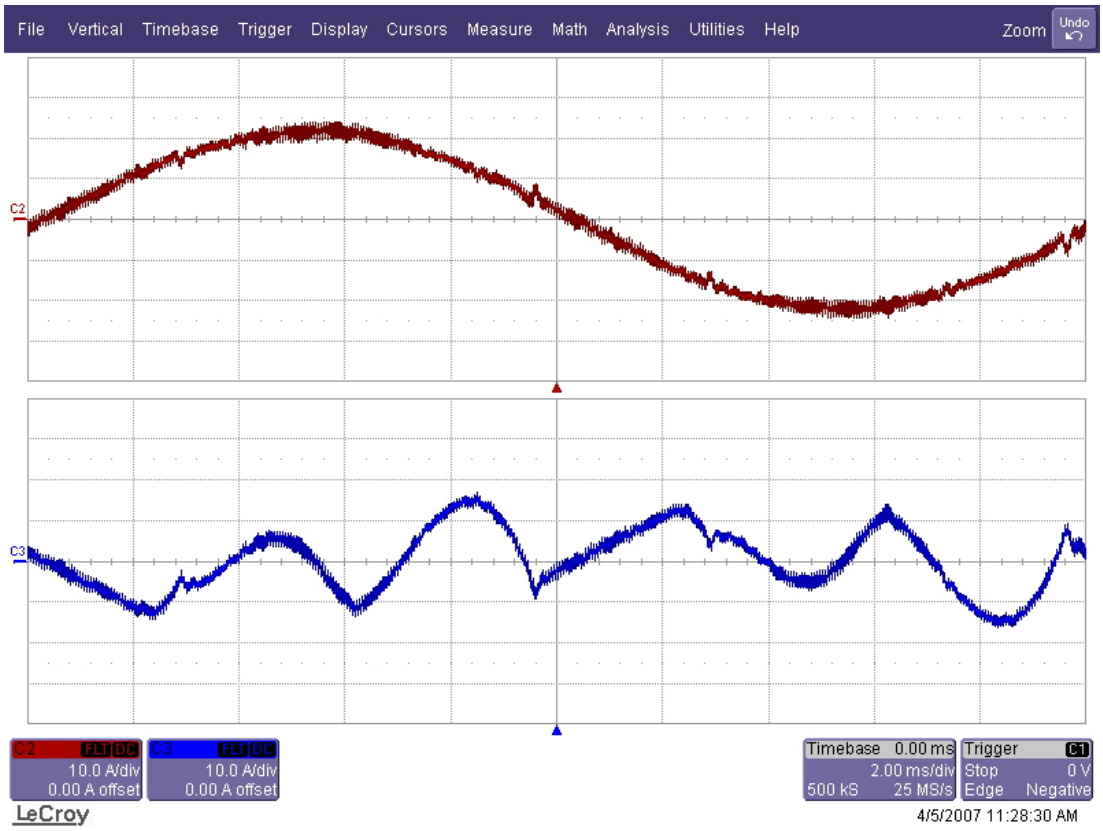

Figure 6.17 The experimental line current (red, 10 A/div) and PAF current (blue, 5 A/div) waveforms for RFCR (time axis: 2 ms/div).

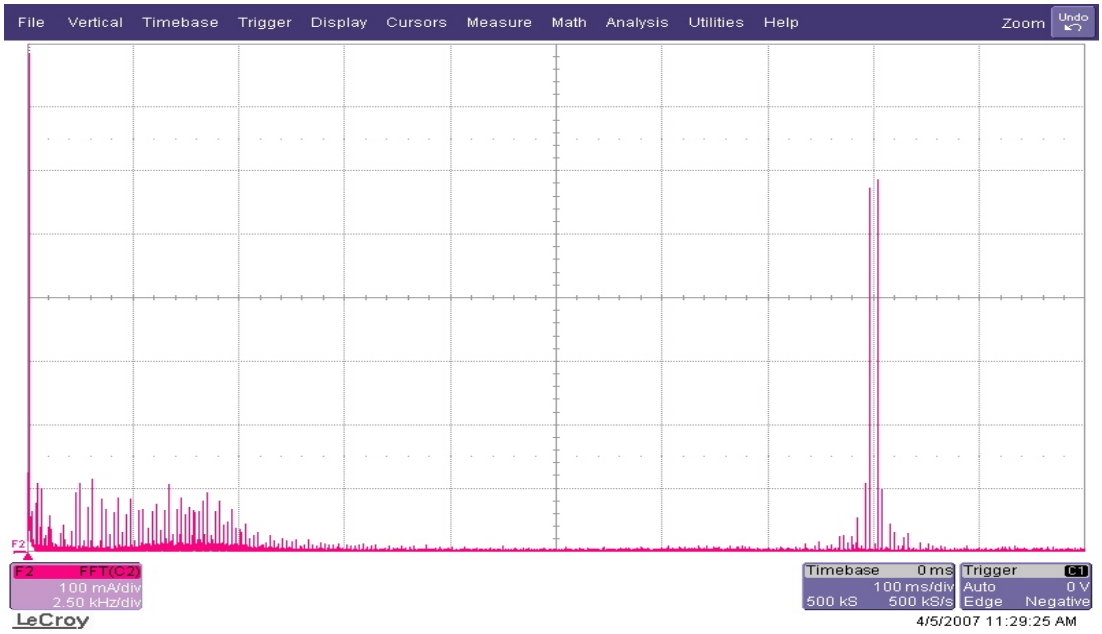

Figure 6.18 The experimental line current harmonic spectrum for RFCR (scales: 100 mA/div, 2.5 kHz/div).

6.4.2 DHCR2 Experimental Results

In this section, the experimental studies for the PAF system utilizing the DHCR2 without SRF are presented. The sampling coefficient K is 10 and T_S is 50 μs to limit the PAF system f_{MAX} value to 20 kHz. The hysteresis band limit is 0.5 A as in the computer simulation part.

Table 6.6 summarizes the experimental results for DHCR2 in terms of harmonic current percentages up to the 50^{th} harmonic order, THD_I, THD_V, PF, and f_{AVG}. The harmonic compensation capability of DHCR2 can be easily compared to previously analyzed current regulators, LPCR and RFCR, by analyzing Table 6.4 and Table 6.5 respectively. Although the PAF system with DHCR2 meets IEEE 519 limits, the harmonic compensation capability of the harmonics above the 17^{th} order of DHCR2 is poor compared to the LPCR and RFCR. The DHCR2 poor current tracking is due to the limitation for the switch on-off signal in order to limit f_{MAX} value as described in Chapter 3. The poor compensation capability results in a THD_I value of 5.1%, which is slightly high compared to THD_I values of 4.0% for the LPCR and 2.3% for the RFCR. The THD_V value is 2.4% and PF is 0.992 for the DHCR2. However, the f_{AVG} value of 8.3 kHz is 38% lower than the f_{AVG} value of 13.3 kHz for the linear current regulators, which results in lower power losses. Figure 6.19 illustrates the experimentally obtained line current waveform and PAF current waveform while Figure 6.20 illustrates the harmonic spectrum of line current. If Figure 6.17 is compared to Figure 6.15 for the LPCR and Figure 6.17 for the RFCR in the previous sections, the ripple content is slightly high due to switch lock mechanism utilized for the DHCR2. Although the ripple is increased, the current spikes corresponding high di/dt regions on the line current waveform are reduced due to the increased sampling rate. The harmonic current spectrum for DHCR2 obtained in the experimental studies spreads over a wide frequency range and is as expected for the hysteresis current regulators. The experimental results verify the computer simulation results of the improved discrete time hysteresis current regulator, DHCR2.

Table 6.6 The experimental line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for DHCR2, and IEEE 519 limits

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%)	IEEE 519 Harmonic Current Limits for I_{SC}/I_{L1}=173 (%)
I_1	100.0	100.0	100.0
I_5	35.5	2.1	12.0
I_7	9.5	0.9	12.0
I_{11}	6.5	1.6	5.5
I_{13}	3.5	0.7	5.5
I_{17}	3.0	1.3	5.0
I_{19}	2.0	0.6	5.0
I_{23}	1.5	0.9	2.0
I_{25}	1.0	0.6	2.0
I_{29}	0.8	0.5	2.0
I_{31}	0.7	0.7	2.0
I_{35}	0.5	0.4	1.0
I_{37}	0.4	0.4	1.0
I_{41}	0.4	0.4	1.0
I_{43}	0.3	0.4	1.0
I_{47}	0.4	0.4	1.0
I_{49}	0.3	0.5	1.0
THD_I (%)	37.5	5.1	15.0
THD_V (%)	2.4	2.4	5.0
PF	0.920	0.992	---
f_{AVG}		8.3	

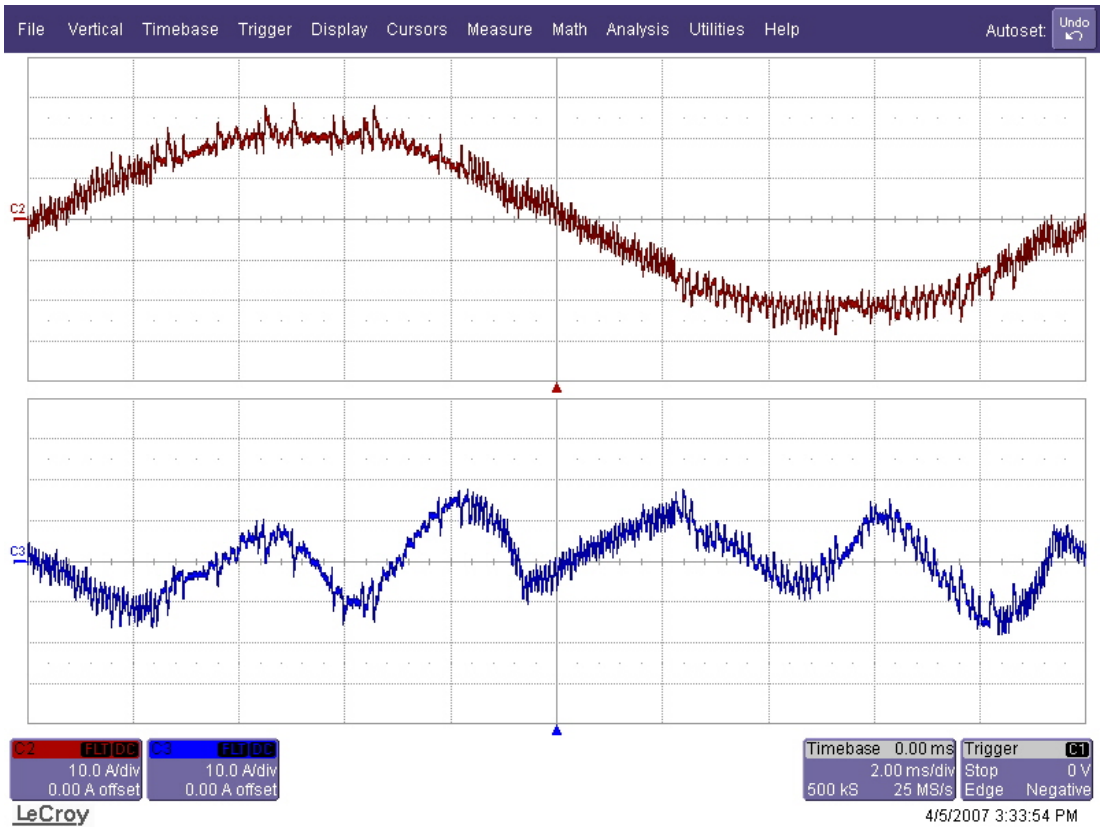

Figure 6.19 The experimental line current (red, 10 A/div) and PAF current (blue, 5 A/div) waveforms for DHCR2 (time axis: 2 ms/div).

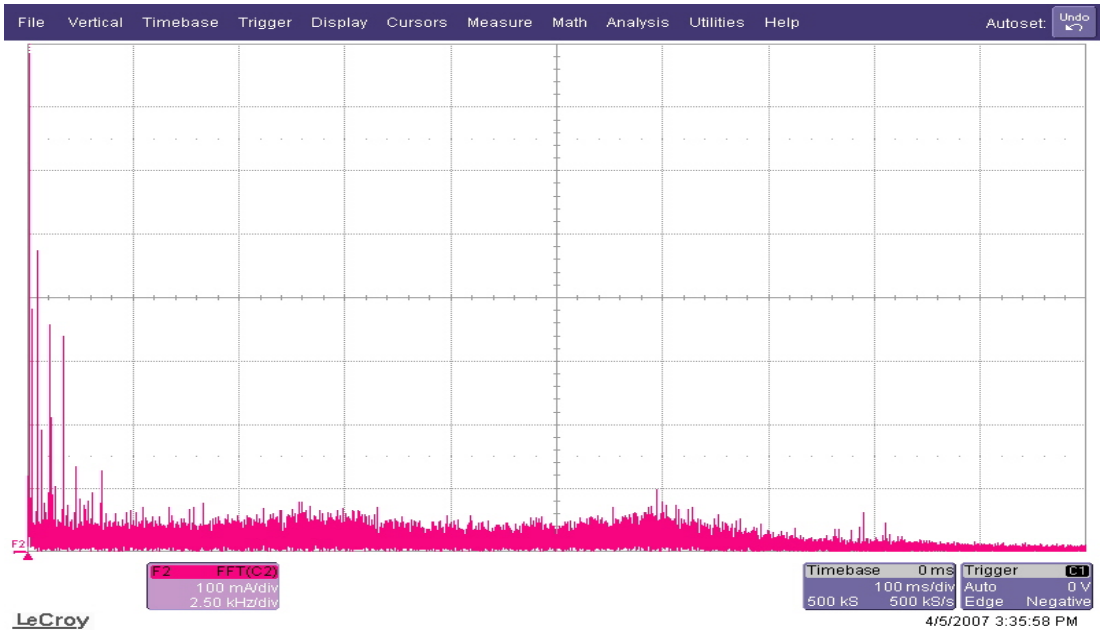

Figure 6.20 The experimental line current harmonic spectrum for DHCR2 (scales: 100 mA/div, 2.5 kHz/div).

6.4.3 DHCR3 Experimental Results

In this section, DHCR3 experimental performance is presented. The sampling coefficient K is 10, T_S is 50 μs to limit the PAF system f_{MAX} value to 20 kHz to 20 kHz, and hysteresis band limit is again 0.5 A as in DHCR2 case.

Table 6.7 summarizes the experimental results for the DHCR3. The harmonic compensation capability of the DHCR3 can be easily compared to previously analyzed DHCR2 if Table 6.6 and Table 6.7 are compared. The DHCR3 harmonic compensation capability for the harmonics components above the 17^{th} order is enhanced due to switch release mechanism involved in DHCR3. Moreover, the DHCR3 harmonic compensation capability for the harmonics components above the 17^{th} order is nearly same as the values for linear current regulators. This bandwidth improvement results in a lower THD_I value of 3.7% compared to the THD_I value of 5.1% for the DHCR2. Further, while the f_{AVG} value of 10.3 kHz is 23% lower than the f_{AVG} value of 13.3 kHz for the LPCR, THD_I value of 3.7% is lower than THD_I value of 4.0% for the practically utilized LPCR in PAF application. The THD_V value is 2.4% and PF is 0.995 for the DHCR3. Figure 6.21 illustrates experimental line current waveform and PAF current waveform while Figure 6.22 illustrates the harmonic spectrum of line current for the DHCR3. If the line current and the PAF current waveform for the DHCR3 is compared to the line current and the PAF current waveform for DHCR2 in the previous section, the ripple content is reduced and tracking capability of current regulator is enhanced due to switch release mechanism involved in DHCR3. The current spikes corresponding high di/dt regions on the line current waveform are reduced due to the increased sampling rate and switch release mechanism compared to the previously analyzed current regulators. Experimental line current spectrum has density at around 15 kHz as in computer simulation results for DHCR3. Although the computer simulation results of THD_I and THD_V values for DHCR3 are higher than the ones obtained in experimental studies due to the contribution of the switching frequency harmonics to the THD_I and THD_V values, the experimental waveforms are consistent with computer simulation results. The experimental results presented in this section illustrate that the steady-

state performance and tracking capability of the discrete time hysteresis current regulators can be improved with the multi-rate sampling and switch release mechanism. Further, the experimental performance of the DHCR3 with the reduced f_{AVG} value is comparable with the linear current regulators and is superior for the current references with high di/dt content.

Table 6.7 The experimental line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for DHCR3, and IEEE 519 limits

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%)	IEEE 519 Harmonic Current Limits for I_{SC}/I_{L1}=173 (%)
I_1	100.0	100.0	100.0
I_5	35.5	1.9	12.0
I_7	9.5	0.9	12.0
I_{11}	6.5	1.2	5.5
I_{13}	3.5	0.5	5.5
I_{17}	3.0	0.9	5.0
I_{19}	2.0	0.5	5.0
I_{23}	1.5	0.5	2.0
I_{25}	1.0	0.6	2.0
I_{29}	0.8	0.5	2.0
I_{31}	0.7	0.4	2.0
I_{35}	0.5	0.3	1.0
I_{37}	0.4	0.3	1.0
I_{41}	0.4	0.3	1.0
I_{43}	0.3	0.3	1.0
I_{47}	0.4	0.3	1.0
I_{49}	0.3	0.3	1.0
THD_I (%)	37.5	3.7	15.0
THD_V (%)	2.4	2.4	5.0
PF	0.920	0.995	---
f_{AVG}		10.3	

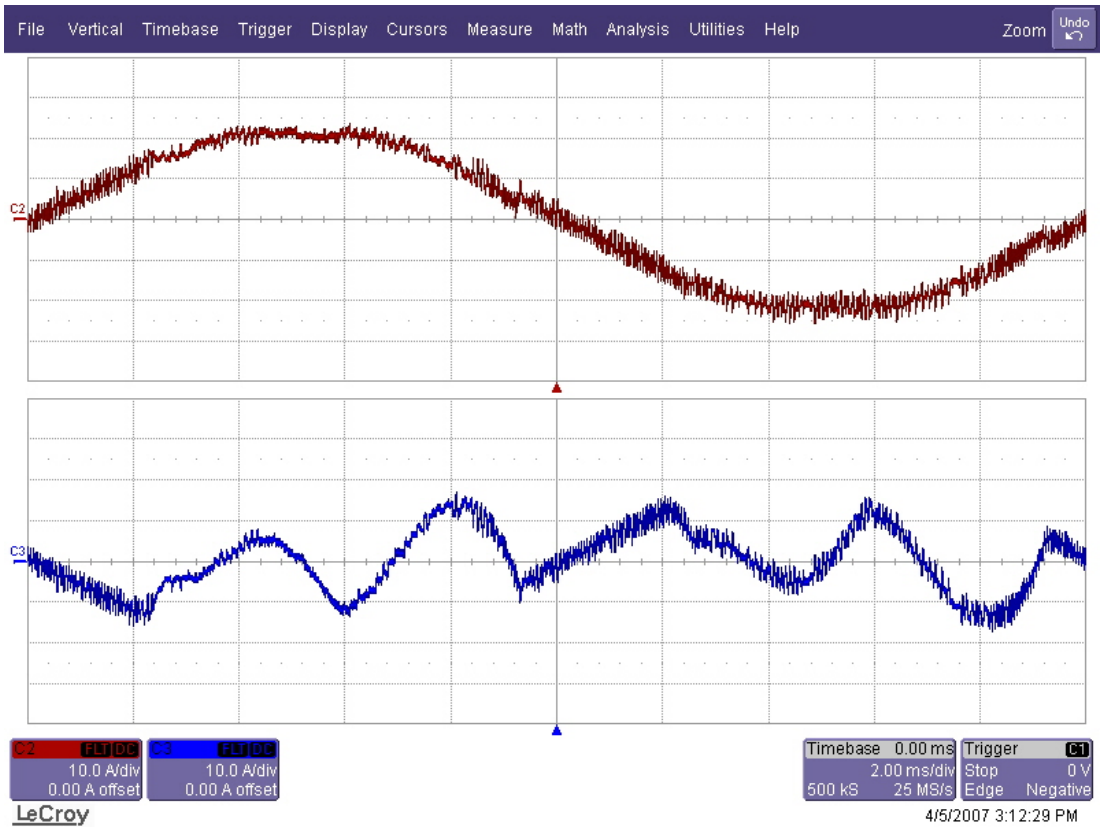

Figure 6.21 The experimental line current (red, 10 A/div) and PAF current (blue, 5 A/div) waveforms for DHCR3 (time axis: 2 ms/div).

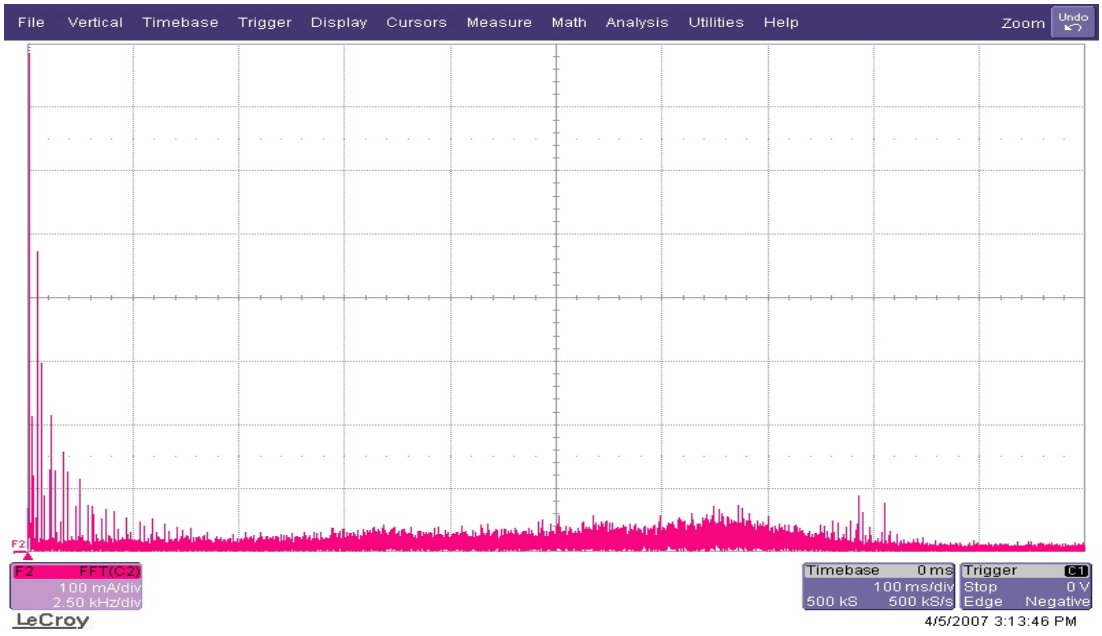

Figure 6.22 The experimental line current harmonic spectrum for DHCR3 (scales: 100 mA/div, 2.5 kHz/div).

6.4.4 Summary of The Current Regulator Performance Comparison without SRF by Means of Experimental Studies

Although a comparison study is held during the analysis of the experimental results of discussed current regulators, it is important to illustrate the experimental results of current regulators in one table in order to perform a better comparison. Moreover, it is important to compare computer simulation results with experimental obtained data to discuss the consistency of the results. Although, the contribution switching frequency harmonics to the THD_I and THD_V values is not observable in experimental study contrary to computer simulation study, this section summarizes the experimental results of discrete time current regulators for the PAF system without SRF by making a comparison study. Moreover, a comparison study is held by analyzing the performances of current regulators obtained in computer simulation study and experimental study.

Table 6.8 collects all the experimental data available in Table 6.4 through Table 6.7. Based on the data in the table, all the implemented discrete time current regulators in experimental study meet IEEE 519 harmonic, THD_I, and THD_V limits. Among the current regulators, the RFCR has the lowest THD_I value of 2.3% due to the inclusion of the resonant based harmonic current controllers tuned to the most dominant harmonic frequencies (5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonic frequencies). The THD_I value of 3.7% for the DHCR3 is the second lowest THD_I value and is better than the THD_I value of 4.0% for the LPCR. Moreover, the f_{AVG} value of 10.3 kHz for the DHCR3 is nearly 25% less than the f_{AVG} value of 13.3 kHz for linear current regulators. The THD_I value for the DHCR2 is the highest THD_I value with the lowest f_{AVG} value of 8.3 kHz compared to other current regulators. Therefore, the DHCR2 is favorable in terms of converter efficiency than the other experimentally verified current regulators with a satisfactory THD_I performance. However, when a lower THD_I value is desired with a lower f_{AVG} value, DHCR3 is more favorable than DHCR2 and LPCR. The PF values for all current regulators are approximately the same and unity. Since the effect of switching frequency harmonics is not observable

in THD_V values, the THD_V values for all current regulators have the same value of 2.4% and equal to THD_V value at PCC when the PAF is not connected to the PCC.

Table 6.9 compares and summarizes the computer simulation and experimental results of the current regulators without SRF by means of their performances. The experimental results are consistent with the computer simulation results in terms of PF and f_{AVG} values. However, the THD_I and THD_V values in computer simulation results are higher than the values in experimental study. Moreover, while THD_I value of 7.6% for the DHCR3 is higher than THD_I value of 5.1% for the LPCR in computer simulation, the THD_I value of 3.7% for the DHCR3 is lower than THD_I value of 4.0% for the LPCR in experiment. The reason is the contribution of switching frequency harmonics to the THD_I and THD_V values in computer simulation studies unlike in experimental studies. Since the contribution of the switching harmonics to the THD_I and THD_V values can not be observed in the experimental studies unlike the computer simulation studies, the comparison of the experimental results and computer simulation results for the PAF system with SRF is more meaningful, which will be analyzed in the later parts of the chapter.

This section has presented the experimental performance of the theoretically analyzed current regulators in Chapter 3. The experimental performances for the current regulators in the PAF application verify the computer simulation results such that the RFCR has superior THD_I performance while the DHCR3 THD_I performance is comparable with the RFCR and LPCR THD_I performances. Moreover, as in the computer simulation part, the nearly 25% lower f_{AVG} value for the DHCR3 compared to linear current regulators makes the DHCR3 favorable in terms of converter efficiency. Further, although it has slightly higher ripple content compared to linear current regulators, the superior tracking performance of the DHCR3 due to the over-sampling and the switch release mechanism is verified by experimental studies. However, the switching ripple content will be decreased with the inclusion of the SRF to the PAF experimental set-up, where the section presents the experimental studies of the designed SRFs.

Table 6.8 The experimental line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for the implemented current regulators, and IEEE 519 limits without SRF

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%) LPCR	Line Current Harmonics with PAF (%) RFCR	Line Current Harmonics with PAF (%) DCHR2	Line Current Harmonics with PAF (%) DHCR3	IEEE 519 Harmonic Current Limits (I_{SC}/I_{L1}=173) (%)
I_1	100.0	100.0	100.0	100.0	100.0	100.0
I_5	35.5	2.8	0.5	2.1	1.9	12.0
I_7	9.5	1.0	0.3	0.9	0.9	12.0
I_{11}	6.5	1.1	0.2	1.6	1.2	5.5
I_{13}	3.5	0.9	0.1	0.7	0.5	5.5
I_{17}	3.0	0.8	0.1	1.3	0.9	5.0
I_{19}	2.0	0.5	0.1	0.6	0.5	5.0
I_{23}	1.5	0.6	0.6	0.9	0.5	2.0
I_{25}	1.0	0.5	0.5	0.6	0.6	2.0
I_{29}	0.8	0.4	0.5	0.5	0.5	2.0
I_{31}	0.7	0.4	0.4	0.7	0.4	2.0
I_{35}	0.5	0.3	0.4	0.4	0.3	1.0
I_{37}	0.4	0.3	0.3	0.4	0.3	1.0
I_{41}	0.4	0.3	0.3	0.4	0.3	1.0
I_{43}	0.3	0.3	0.3	0.4	0.3	1.0
I_{47}	0.4	0.3	0.3	0.4	0.3	1.0
I_{49}	0.3	0.3	0.3	0.5	0.3	1.0
THD_I (%)	37.5	4.0	2.3	5.1	3.7	15.0
THD_V (%)	2.4	2.4	2.4	2.4	2.4	5.0
PF	0.920	0.997	0.997	0.992	0.995	---
f_{AVG}(kHz)		13.33	13.33	8.3	10.3	

Table 6.9 The comparison of the PAF system performance without SRF for various current regulators in terms of computer simulation and experimental results

		Computer Simulation				Experiment			
	CR Type	THD_I (%)	THD_V (%)	PF	f_{AVG} (kHz)	THD_I (%)	THD_V (%)	PF	f_{AVG} (kHz)
Load Current		32.6	0.5	0.930		37.5	2.4	0.920	
Line Current	LPCR	5.1	3.8	0.998	13.3	4.0	2.4	0.997	13.3
	RFCR	3.1	3.8	0.998	13.3	2.4	2.4	0.997	13.3
	DHCR2	10.4	5.1	0.993	7.8	5.1	2.4	0.992	8.3
	DHCR3	7.6	5.1	0.996	10.0	3.7	2.4	0.995	10.3
IEEE 519 Limits		15.00	5.00			15.00	5.00		

6.5 Experimental Results of The Designed SRF Topologies

This section involves the experimental performance evaluation of the PAF system with the designed SRFs in Chapter 4 and Chapter 5. The designed tuned LCR type SRF for the linear current regulators and high-pass RC type SRF for the hysteresis current regulators are manufactured at METU Electrical and Electronics Engineering Department, in the Electrical Machines and Power Electronics Laboratory. Figure 6.23 illustrates the laboratory prototype of the designed SRFs. The manufactured tuned LCR type filter with circuit parameters of C_F = 2.2 μF and L_F = 28.8 μH is illustrated on the left side of Figure 6.23. The damping resistor R_F value of 0.66 Ω utilized in computer simulation part is not implemented in experimental studies since the filter inductor internal resistance provides sufficient damping. The manufactured high-pass RC type filter with circuit parameters of C_F = 30 μF and R_d = 2.8 Ω is illustrated on the right side of Figure 6.23. The manufactured SRFs are connected to the PCC via 20 A automatic fuses for switching and protection purposes.

In this section, first the experimental performance of the designed tuned LCR type SRF for the linear current regulator will be illustrated for diode rectifier load of 10

kW and the PAF system with the circuit parameters and operating conditions are given in Table 5.1 and Table 5.3. The experimental results will be compared to computer simulation results. Then the same experimental study will be carried out for the designed high-pass RC type SRF for the hysteresis current regulators.

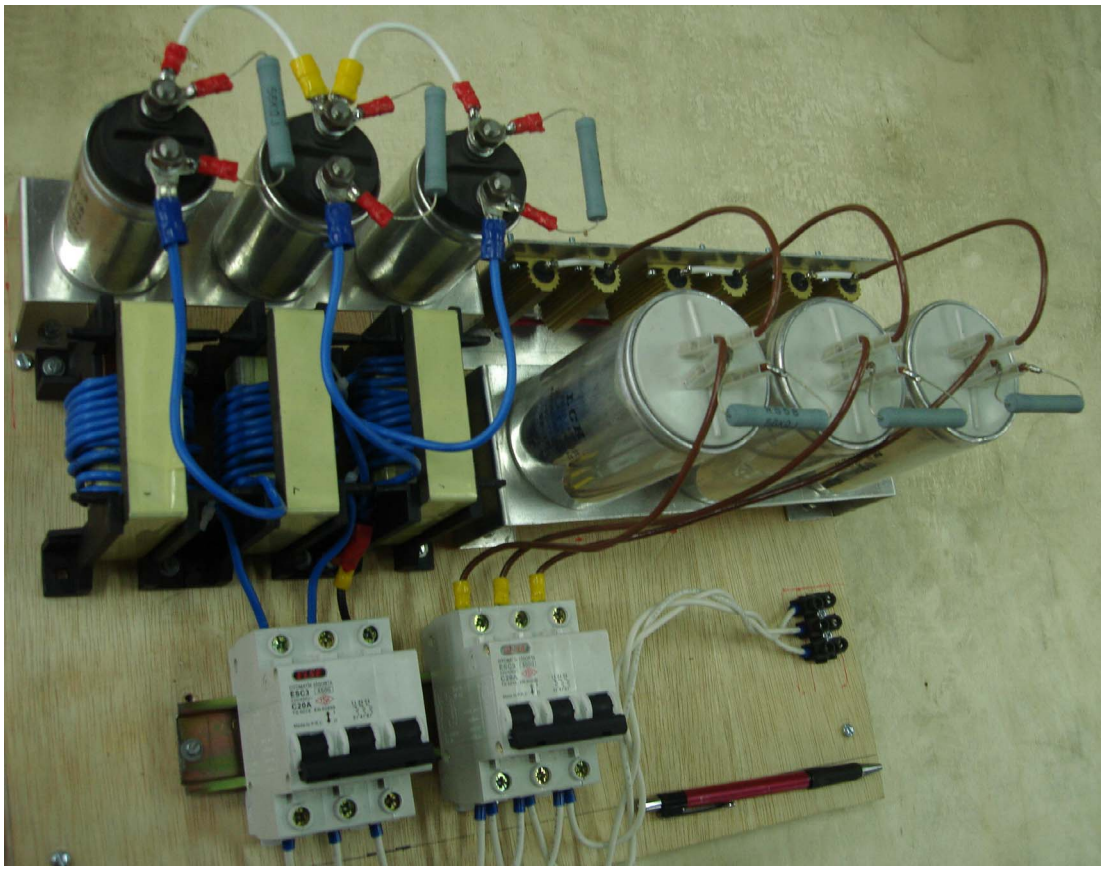

Figure 6.23 Laboratory prototype of the manufactured SRFs:
tuned LCR type SRF (left), high-pass RC type SRF (right).

6.5.1 Experimental Results of The Tuned LCR Type SRF

The experimental line voltage, line current, and PAF current waveforms are illustrated and compared for the PAF system utilizing LPCR without and with tuned LCR type SRF in Figure 6.24. The experimental harmonic spectrums of the voltage and line current are illustrated and compared without and with SRF in Figure 6.25. For the system without SRF, there exist high-frequency ripple currents and voltages on line voltage and current waveforms in Figure 6.24.a and harmonic spectrums in Figure 6.25.a. These ripples are concentrated at the switching frequency of 20 kHz as in the computer simulation part. If the waveforms and their FFTs are investigated in Figure 6.24.b and 6.25.b respectively for the PAF system with the tuned LCR type SRF and compared to the waveforms and their FFTs in Figure 6.24.a and 6.25.a where the SRF is not utilized, the attenuation of the switching ripples are obvious at 20 kHz. As a result, the line current and voltage become nearly switching ripple free. If the line current FFT in Figure 6.25.b is investigated for the SRF case, there exists no amplification of current harmonics at 10 kHz due to parallel resonant of the SRF circuit components with line inductance since the internal resistance of the filter components provide sufficient damping. These waveforms and their FFTs without and with SRF verify the experimental performance of the designed tuned LCR type for the liner current regulators.

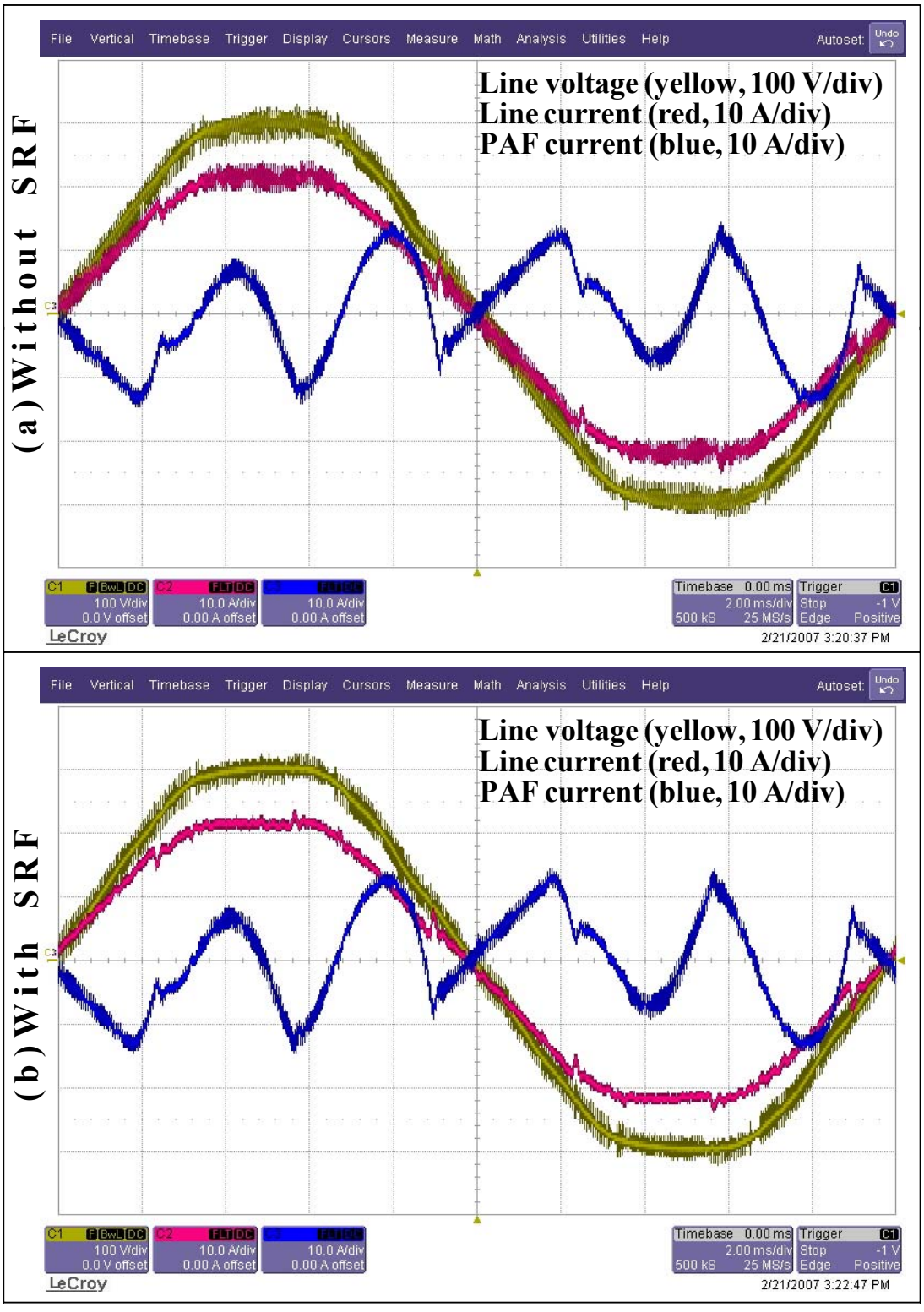

Figure 6.24 The experimental line voltage, line current, and PAF current for the PAF utilizing LPCR without and with the designed tuned LCR type SRF (time axis: 2 ms/div).

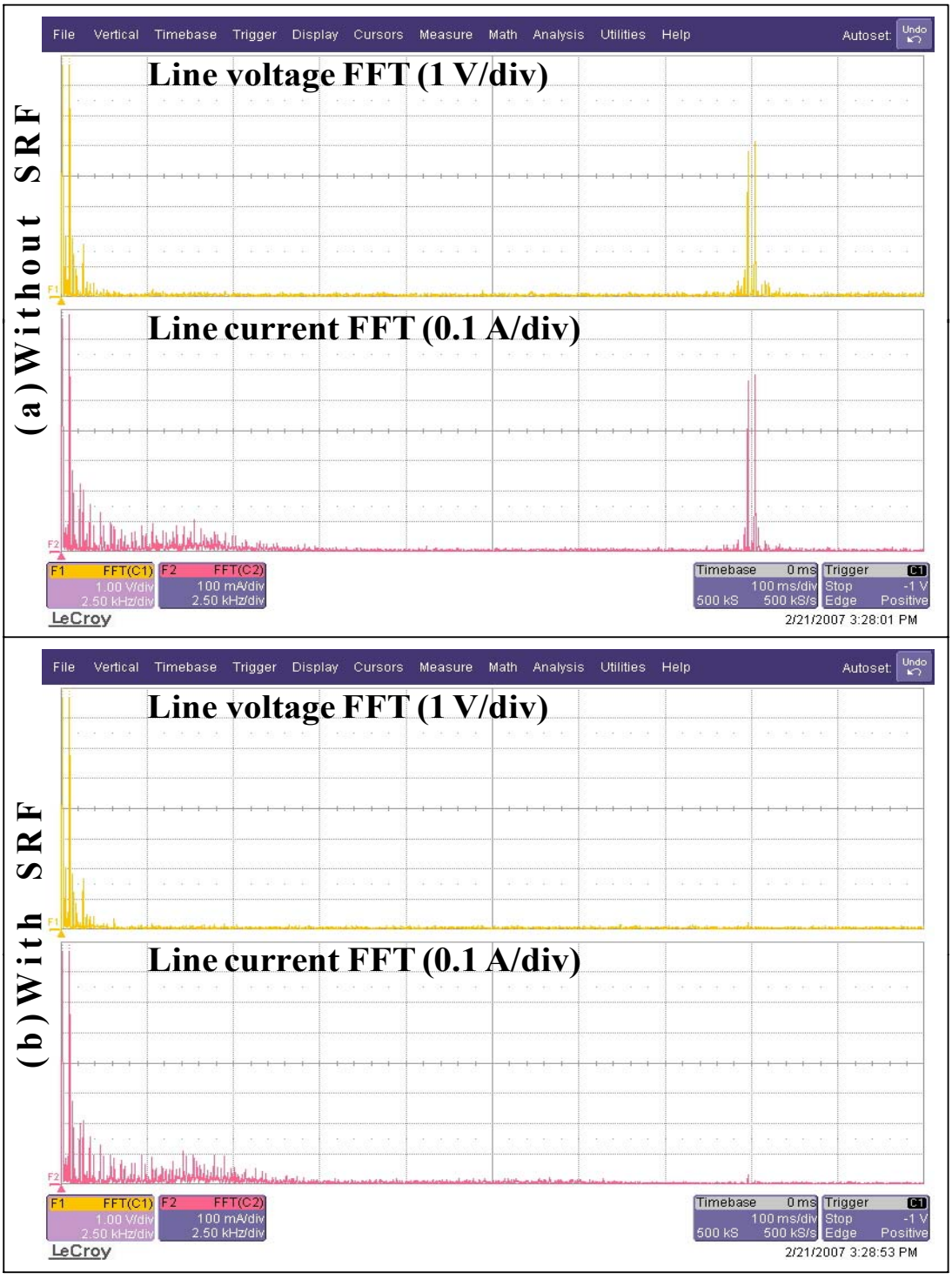

Figure 6.25 The experimental line voltage and line current FFTs for the PAF utilizing LPCR without and with the designed tuned LCR type SRF (frequency axis: 2.5 kHz/div).

The experimental THD_I and THD_V values of the system without and with the designed tuned LCR type SRF are given and compared with the THD_I and THD_V values of the system obtained in computer simulation in Table 6.10. The experimental THD_I and THD_V values are same for the cases of the system without SRF and with SRF. The reason is that the utilized ZesZimmer Power Analyzer calculates the THD_I and THD_V values up to 100^{th} harmonic order (up to 5 kHz). Therefore the effect of switching ripples on the THD_I and THD_V values cannot be observed via power analyzer measurements. However, the Ansoft-Simplorer software utilized for computer simulations calculates THD_I and THD_V values up to MHz frequencies such that the contribution of the switching frequency ripples to the THD_I and THD_V values can be observed as mentioned previously. Therefore, the experimental THD_I value without SRF differs than computer simulation THD_I value without SRF. For the case of the system with SRF, the experimental THD_I value of 4.0% is close to computer simulation THD_I value of 4.1% due to the sufficient attenuation of switching ripple currents. The experimental THD_V value of 2.4% differs than computer simulation THD_V value of 0.8% due to the low frequency harmonic distortion on AC utility grid voltage in the experimental studies, which is independent from the PAF and SRF system.

Experimentally obtained waveforms and their FFTs without/with the SRF verify the experimental performance of the designed tuned LCR type SRF for the linear current regulators. Moreover, the experimental waveforms and their FFTs and THD_I values for the PAF system with SRF are consistent the waveforms and their FFTs and THD_I values for the PAF system with SRF obtained in computer simulation in Section 5.5.1 such that the performance of the designed tuned LCR type SRF for the linear current regulators is experimentally verified.

Table 6.10 Computer simulation and experimental THD performances for the PAF utilizing LPCR without and with the designed tuned LCR type SRF

	Computer Simulation		Experiment	
	THD_I (%)	THD_V (%)	THD_I (%)	THD_V (%)
Without SRF	5.1	3.8	4.0	2.4
With SRF	4.1	0.8	4.0	2.4

6.5.2 Experimental Results of The High-pass RC Type SRF

The line voltage, line current, and PAF current are illustrated and compared for the PAF system utilizing DHCR3 without and with high-pass RC type SRF in Figure 6.26. The harmonic spectrums of line voltage and line current are illustrated and compared without and with SRF in Figure 6.27. For the system without SRF, there exist high-frequency ripple currents and voltages on line voltage and current in Figure 6.26.a and harmonic spectrums in Figure 6.27.a. These high frequency ripples spread over a wide frequency range (5-25 kHz) and concentrated around 15-17 kHz as illustrated in the computer simulations. If the waveforms and their FFTs are investigated in Figure 6.26.b and 6.27.b for the PAF system with the high-pass RC type SRF and compared to Figure 6.26.a and 6.27.a where the SRF is not utilized for the PAF system, the attenuation of switching ripples are obvious for wide frequency range. As a result, line current and voltage become nearly switching ripple free and the waveforms and their FTTs verify the experimental performance of the designed high-pass RC type filter for hysteresis current regulators in the PAF application.

The experimental THD_I and THD_V values of the system without and with the designed high-pass RC type SRF are given and compared with the THD_I and THD_V values obtained in computer simulation in Table 6.11. The experimentally obtained THD_V values are the same for the cases of the system without SRF and with SRF since the power analyzer utilizes first 100^{th} harmonics components for the calculation of THD_V. However, experimentally obtained THD_I value of 3.7% for the case of without SRF rises to the experimentally obtained THD_I value of 4.1% for the case of with SRF due to the parallel resonant which occurs between capacitor of the SRF and line inductance around 3 kHz and the low frequency voltage harmonics on the line voltage waveform. The THD_I and THD_V values obtained in experiment differ than THD_I and THD_V values obtained in computer simulation for the case of the system without SRF since power analyzer calculates THD values by evaluating the first 100^{th} harmonics components while computer simulation software calculates THD values by evaluating harmonics components up to MHz range. For the case of the system with SRF, since the high-frequency ripple components are attenuated in the

computer simulation, the experimental THD_I value of 4.1% is close to the computer simulation THD_I value of 4.2%. The experimental THD_V value of 2.4% differs than computer simulation THD_V value of 1.5% due to the low frequency harmonic distortion on AC utility grid voltage, which is independent of PAF and SRF system as in the tuned LCR type SRF case.

The experimental waveforms and their FFTs without/with SRF verify the experimental performance of the designed high-pass RC type SRF for hysteresis current regulators. Moreover, the waveforms and their FFTs and THD_I values with SRF for experimental studies are consistent the waveforms and their FFTs and THD_I values with SRF for computer simulations in Section 5.5.2.

In this section, the performances of the designed SRFs are investigated and their effectiveness for the switching ripple current attenuations is verified by means of experimental studies. The strong correlation between the theory, simulations and experiments has been shown.

Table 6.11 Computer simulation and experimental THD performances for the PAF utilizing DHCR3 without and with the designed high-pass RC type SRF

	Computer Simulation		Experiment	
	THD_I (%)	THD_V (%)	THD_I (%)	THD_V (%)
Without SRF	7.6	5.1	3.7	2.4
With SRF	4.2	1.5	4.1	2.4

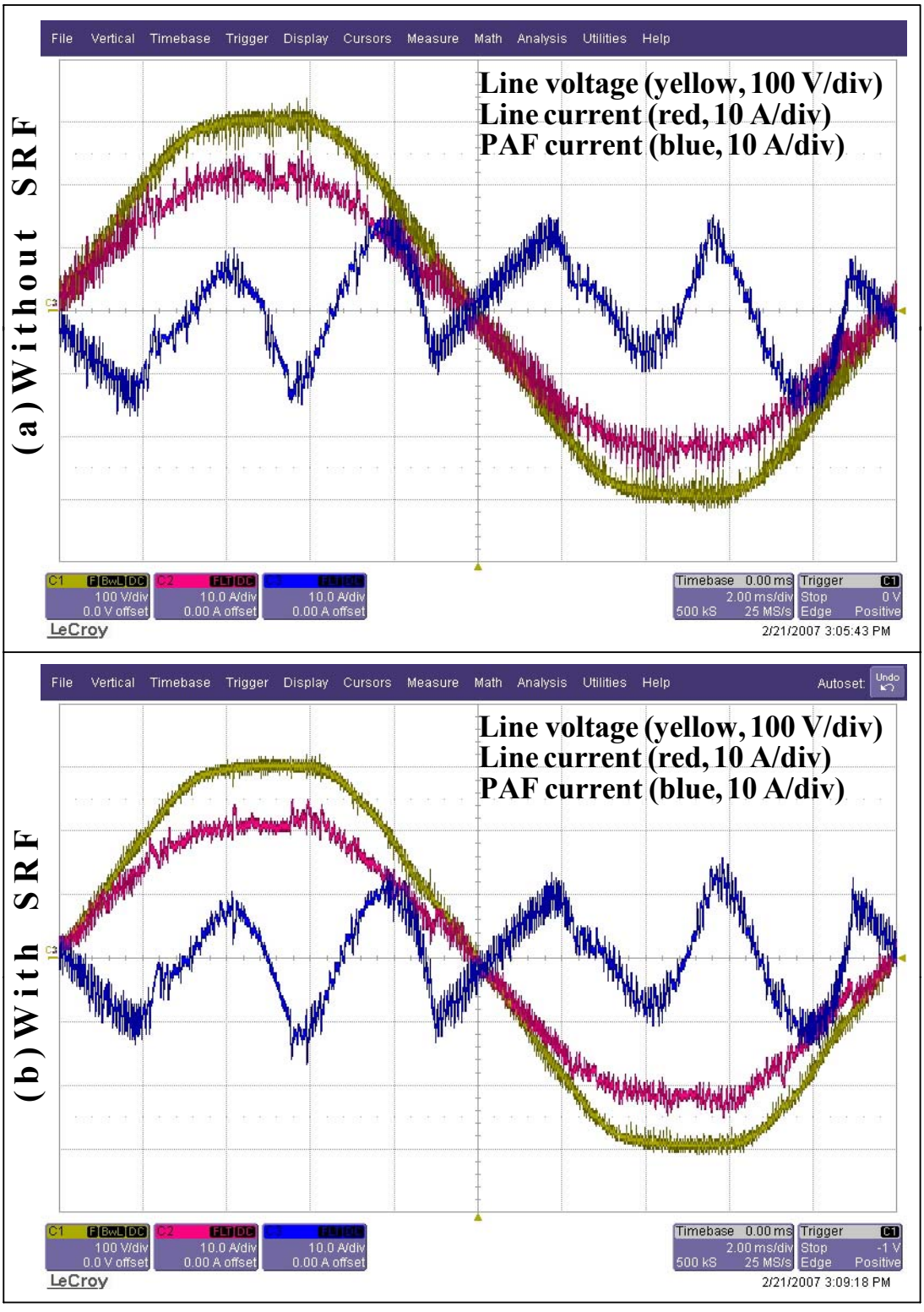

Figure 6.26 The experimental line voltage, line current, and PAF current for the PAF utilizing DHCR3 without and with the designed high-pass RC type SRF (time axis: 2 ms/div)

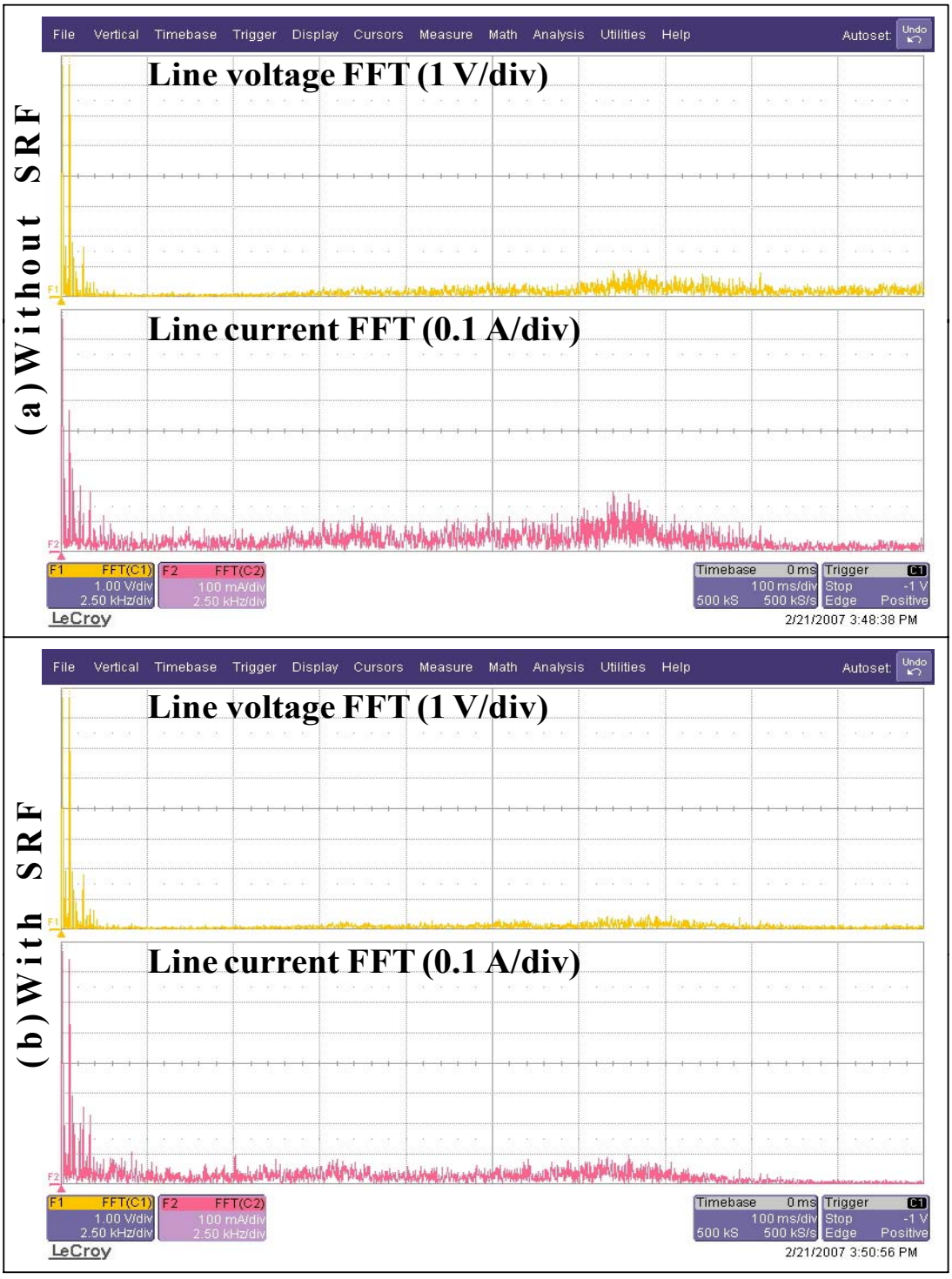

Figure 6.27 The experimental line voltage and line current FFTs for the PAF utilizing DHCR3 without and with the designed high-pass RC type SRF (frequency axis: 2.5 kHz/div).

6.6 Illustration of The Experimental Detailed PAF Performance

This section illustrates the detailed PAF performance experimentally. As in the section of 'The illustration of the Detailed PAF Performance' in Chapter 5, this section first discusses the experimental PAF performance with the designed SRFs for the implemented current regulators in the Section 6.4. Then the experimental steady-state performance of the PAF will be illustrated for DHCR3, where the PAF system includes the designed high-pass RC type SRF, and for RFCR with superior THD_I, where the PAF system includes the designed tuned LCR type SRF. Finally, the PAF dynamic response will be illustrated as in the computer simulation chapter.

6.6.1 Performance Comparison of The Current Regulators with The Designed SRFs by Means of Experimental Studies

This section summarizes experimental results of discrete time current regulators implemented for the PAF system and compares them with computer simulation results when the SRF is included in the PAF system. Although the effect of the SRF is more visible on the line current waveform and line current harmonic spectrum and the SRF slightly changes the THD_I performances, it is better to analyze the experimental performance of the current regulators with and without SRF in a table. Further, the comparison of the experimental and computer simulation results for PAF system with the SRF for different current regulators is involved in this subsection.

Table 6.12 summarizes the experimental results of the PAF system with SRF for the implemented current regulators, LPCR, RFCR, DHCR2, and DHCR3. Table 6.12 includes harmonic components of line current up to 50^{th} harmonics order, THD_I value of line current, THD_V value of line voltage, PF at PCC, and the f_{AVG} for the analyzed current regulators, and IEEE limits. The percentage of harmonic components is approximately same with the SRF included in the PAF system, and can be compared with Table 6.8. Table 6.13 provides the experimental results of the PAF system with and without SRF utilizing different current regulators by only including THD_I, THD_V, PF at PCC, and f_{AVG} values. Based on the data, while the

THD_I values for the linear current regulators do not change for the PAF system with and without SRF, the THD_I values for the discrete time hysteresis current regulators increases slightly for the PAF system with and without SRF due to the lower parallel resonant frequency (3 kHz) of the designed high-pass RC type SRF for hysteresis current regulators compared to the parallel resonant frequency of 9.5 kHz for the linear current regulators and the low frequency voltage distortion on the line voltage waveform. While the THD_I value of 3.7% without SRF increases to the THD_I value of 4.1% with SRF for DHCR3 as discusses in the previous section, the THD_I value of 5.1% without the SRF increases to the THD_I value of 5.4% with SRF for DHCR2. The other values in Table 6.13 do not change considerably with the SRF included in the PAF since SRF only eliminates the high frequency harmonic content on the line current and voltage waveform.

Table 6.14 compares the experimental and computer simulation results of the PAF system with SRF for the implemented current regulators in terms of THD_I, THD_V, PF at PCC, and f_{AVG} values. When the SRF is included to PAF system, the switching frequency harmonics are eliminated, so the performance of the current regulators by means of computer simulation gets closer to the performance of current regulators obtained in experimental studies. For instance, the THD_I value for the RFCR is 2.1% in computer simulation; it is 2.3% in experiment studies. The only inconsistency in Table 6.14 is with the THD_V values due to the low frequency voltage harmonics on the line voltage observed in the experimental studies.

This subsection provides the experimental performance analysis and comparison of current regulators discussed previously with the SRF inclusion to the PAF system and completes the discussion of the current regulator performances in PAF application by making a comparison study with the experimental results and computer simulation results. The discussion in this subsection is another experimental verification of the superior current regulators for the PAF with SRF, where the RFCR illustrates the lowest THD_I performance while the DHCR3 illustrates a comparable THD_I performance and a considerable reduced f_{AVG} value compared to the practically utilized linear current regulators.

Table 6.12 The experimental line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for the implemented current regulators, and IEEE 519 limits with SRF

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%) LPCR	Line Current Harmonics with PAF (%) RFCR	Line Current Harmonics with PAF (%) DCHR2	Line Current Harmonics with PAF (%) DHCR3	IEEE 519 Harmonic Current Limits (I_{SC}/I_{L1}=173) (%)
I_1	100	100.00	100.00	100.00	100.00	100.00
I_5	35.5	2.8	0.5	2.6	2.5	12.0
I_7	9.5	1.0	0.3	0.7	0.7	12.0
I_{11}	6.5	1.1	0.2	1.6	1.4	5.5
I_{13}	3.5	0.9	0.1	0.7	0.4	5.5
I_{17}	3.0	0.8	0.1	1.5	0.9	5.0
I_{19}	2.0	0.5	0.1	0.7	0.7	5.0
I_{23}	1.5	0.6	0.6	0.7	0.5	2.0
I_{25}	1.0	0.5	0.5	0.4	0.4	2.0
I_{29}	0.8	0.5	0.5	0.5	0.5	2.0
I_{31}	0.7	0.4	0.4	0.5	0.4	2.0
I_{35}	0.5	0.4	0.4	0.5	0.3	1.0
I_{37}	0.4	0.3	0.3	0.4	0.3	1.0
I_{41}	0.4	0.3	0.3	0.3	0.3	1.0
I_{43}	0.3	0.3	0.3	0.3	0.3	1.0
I_{47}	0.4	0.3	0.3	0.4	0.3	1.0
I_{49}	0.3	0.3	0.3	0.4	0.2	1.0
THD_I (%)	37.5	4	2.3	5.4	4.1	15.0
THD_V (%)	2.4	2.4	2.4	2.4	2.4	5.0
PF	0.920	0.997	0.997	0.995	0.996	---
f_{AVG} (kHz)		13.3	13.3	8.3	10.3	

Table 6.13 The experimental performance results of the PAF system with SRF and without SRF for the implemented current regulators

		without SRF			with SRF			
	CR Type	THD_I (%)	THD_V (%)	PF	THD_I (%)	THD_V (%)	PF	f_{AVG} (kHz)
Load Current		37.5	2.4	0.920	37.5	2.4	0.920	
Line Current	LPCR	4.0	2.4	0.997	4.0	2.4	0.997	13.3
	RFCR	2.3	2.4	0.997	2.3	2.4	0.997	13.3
	DHCR2	5.1	2.4	0.992	5.4	2.4	0.995	8.3
	DHCR3	3.7	2.4	0.995	4.1	2.4	0.996	10.3
IEEE 519 Limits		15.00	5.00		15.00	5.00		

Table 6.14 Computer simulation and experimental performance results of the PAF system with SRF for the implemented current regulators with SRF

		Computer Simulation				Experiment			
	CR Type	THD_I (%)	THD_V (%)	PF	f_{avg} (kHz)	THD_I (%)	THD_V (%)	PF	f_{AVG} (kHz)
Load Current		32.6	0.5	0.93		37.5	2.4	0.920	
Line Current	LPCR	4.1	0.8	0.999	13.3	4.0	2.4	0.997	13.3
	RFCR	2.1	0.8	0.999	13.3	2.3	2.4	0.997	13.3
	DHCR2	7.6	1.9	0.997	7.8	5.4	2.4	0.995	8.3
	DHCR3	4.2	1.5	0.999	10.0	4.1	2.4	0.996	10.3
IEEE-519 Limits		15.00	5.00			15.00	5.00		

6.6.2 The Experimental PAF Steady-state Performance

In this subsection, the experimental PAF steady-state performance with the designed SRF will be illustrated for the high performance current regulators; DHCR3 and RFCR. Since the THD_I, THD_V, PF, and f_{AVG} performances of both current regulators were given in the previous subsection, they will not be analyzed in this subsection. Only the waveforms and PAF system power rating with the SRF will be presented.

Figure 6.28 respectively illustrates the experimental steady-state the line voltage, the line current, the load current, the PAF current for 'phase *a*', and Figure 6.29 respectively illustrates the experimental steady-state line voltage, the PAF current and the SRF current for phase '*a*', and the DC bus voltage waveforms of PAF system, which utilizes the DHCR3 and the designed high-pass RC type SRF for the compensation of the harmonics and reactive current component of the diode rectifier load with the output power rating of 10 kW. The line current waveform in Figure 6.29 is nearly sinusoidal with THD_I value of 4.1% and in phase with line voltage with a PF value of 0.997. The SRF current in Figure 6.29 is an illustration of high frequency switching currents attenuation that PAF with DHCR3 creates. Further, the PAF DC average bus voltage is at its reference voltage 700 V with a nearly 5 V peak to peak 300 Hz ripple. The detailed illustration of the line current, and the PAF current is illustrated in Figure 6.30 for the PAF system with the designed high-pass RC type SRF and the DHCR3. Moreover, the line current harmonic spectrum in Figure 6.31 is included to provide a visualization of line current harmonic content over a wide frequency range. The experimental steady-state waveforms for the PAF system with the SRF for DHCR3 in Figure 6.28 trough Figure 6.31 is nearly same as the ones obtained in computer simulation and illustrates the detailed experimental steady-state performance of the PAF system with the SRF for DHCR3.

Figure 6.32 respectively illustrates experimental steady-state the voltage at the PCC, the line current, the load current, the PAF current for 'phase *a*', and Figure 6.33 respectively illustrates the experimental steady-state line voltage, the PAF current, and the SRF current for phase '*a*', and the DC bus voltage waveforms of PAF system,

which utilizes the RFCR and the designed tuned LCR type SRF and connected in parallel to the 10 kW diode rectifier load. The line current waveform in Figure 6.32 is approximately sinusoidal with THD_I value of 2.3% and in phase with the line voltage with PF value of 0.997. The SRF current contains the high frequency switching ripple currents as expected. The PAF DC average bus voltage is at its reference voltage 700 V with a nearly 5 V peak to peak 300 Hz as in DHCR3 case. The detailed illustration of the line current and the PAF current is illustrated in Figure 6.34 for the PAF system with the designed tuned LCR type SRF for RFCR. The line current harmonic spectrum in Figure 6.35 over a wide frequency range presents a visualization of line current harmonic content and proves the well defined harmonic spectrum for linear current regulators. The detailed experimental steady-state waveforms of the PAF system with the designed SRF for the RFCR are consistent with the ones obtained in the computer simulation.

Table 6.15 presents the experimental steady-state power flow data for the load current, line current, PAF current, SRF current, and the line voltage in magnitude. Moreover, it involves the input power rating of the diode rectifier load of 10 kW output power rating, the power drawn from the AC utility grid, the PAF power rating for DHCR3 and RFCR. While the load power and the line power for both regulators have the values, the filter rating in kVA differs due to the sizes of the capacitors utilized in the SRF structure, which differs for the DHCR3 and RFCR. Moreover, the experimental data in Table 6.15 has higher values compared to the data in Table 5.17 obtained for the computer simulation due to the power losses with the circuit elements involved in the experimental studies. Since many circuit elements in computer simulations are assumed ideal, the power ratings obtained in the computer simulations are slightly lower than the power ratings obtained in experimental studies for the same output power (10 kW) of the diode rectifier load. However, the data in both tables are consistent with each other. Since the detailed experimental steady-state performance illustration of the PAF system for two superior current regulators in PAF application; DHCR3 and RFCR, are presented, the next subsection analyzes the experimental dynamic response of the PAF system with DHCR3 as in computer simulation chapter.

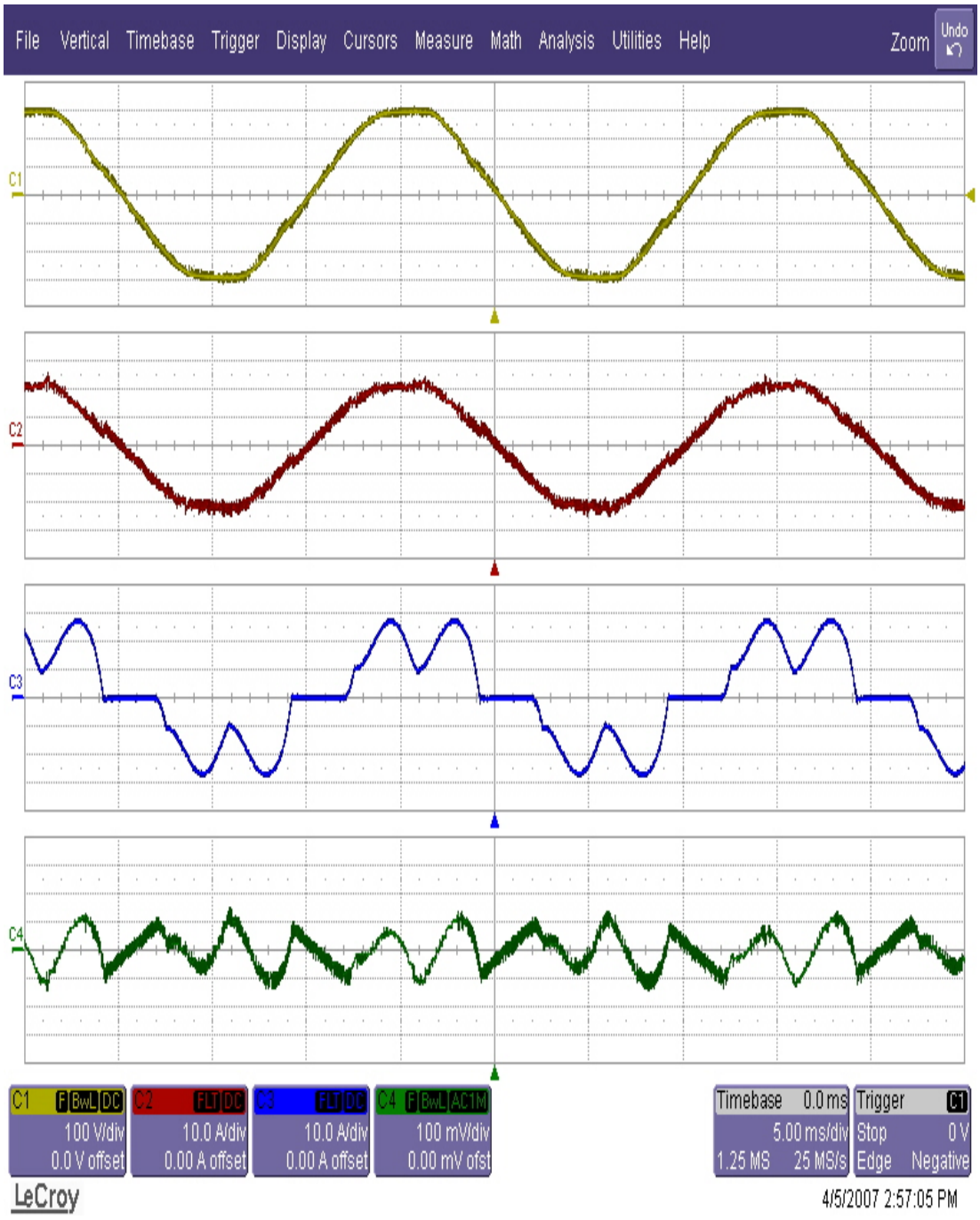

Figure 6.28 The experimental steady-state waveforms illustrating the detailed performance of the PAF system with SRF for DHCR3: line voltage (yellow, 100 V/div), line current (red, 10 A/div), load current (blue, 10 A/div), and the PAF current (green, 10 A/div) (time axis: 5 ms/div).

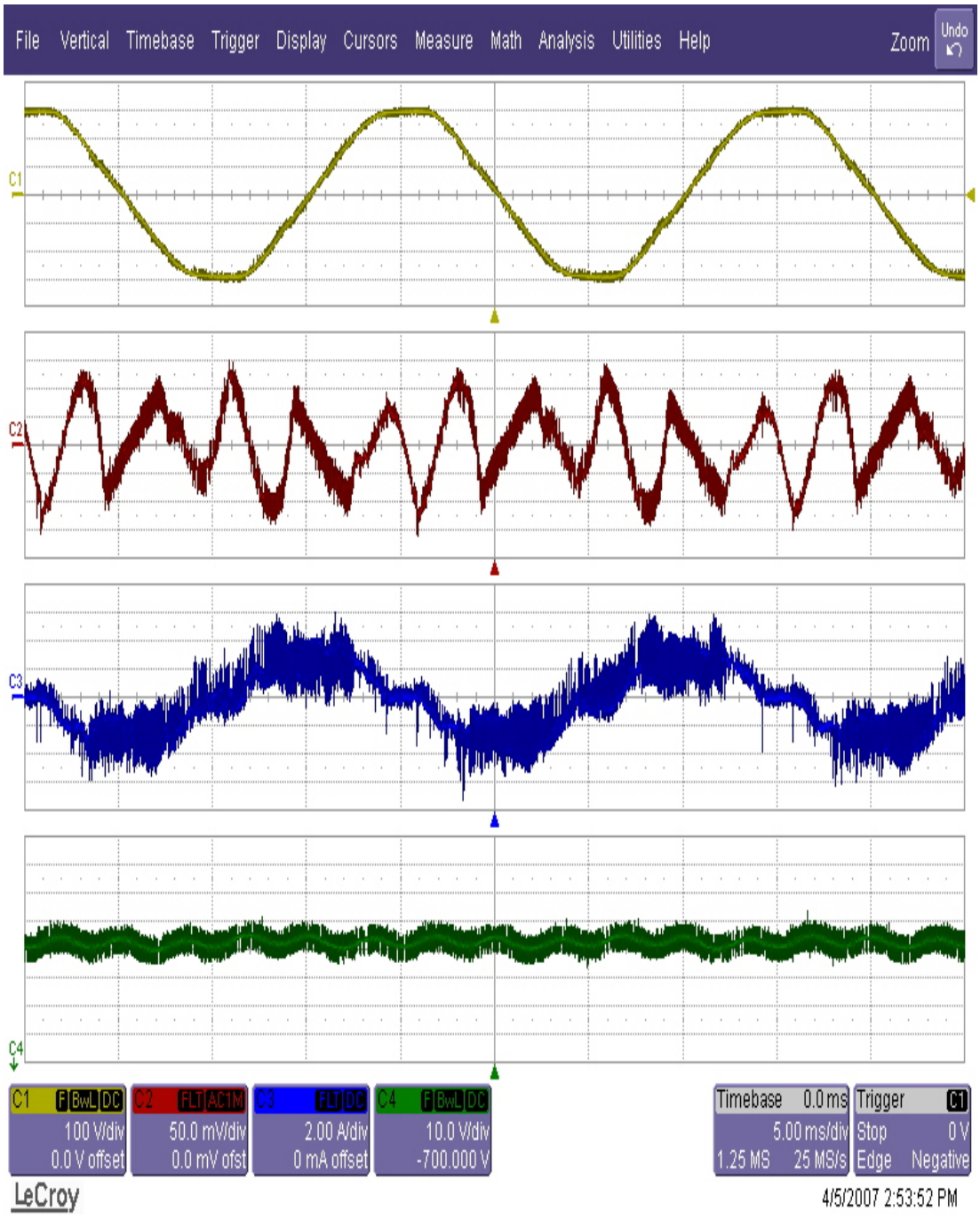

Figure 6.29 The experimental steady-state waveforms illustrating the detailed performance of the PAF system with SRF for DHCR3: line voltage (yellow, 100 V/div), the PAF current (red, 10 A/div), the SRF current (blue, 2 A/div), and the PAF DC bus voltage (green, 10 V/div, -700 V offset) (time axis: 5 ms/div).

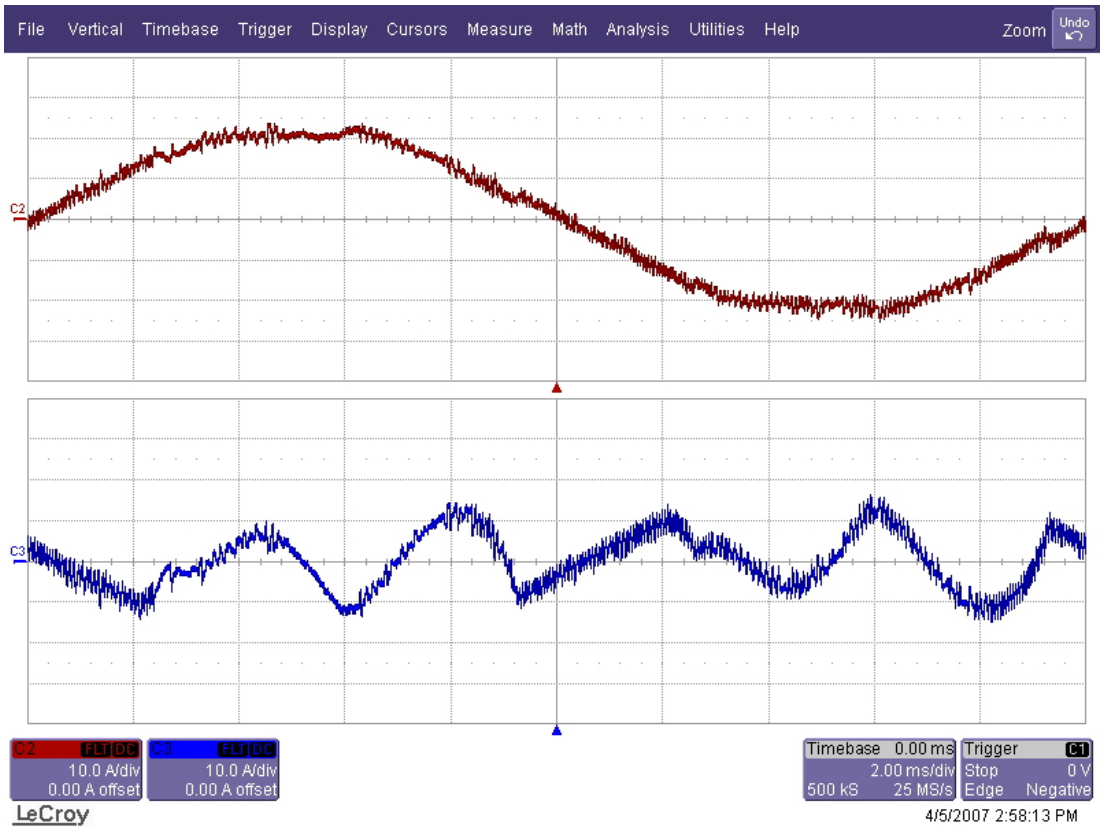

Figure 6.30 The experimental steady-state line current (red, 10 A/div) and filter current reference (blue, 10 A/div) of the PAF system with the SRF for DHCR3 (time axis: 2 ms/div).

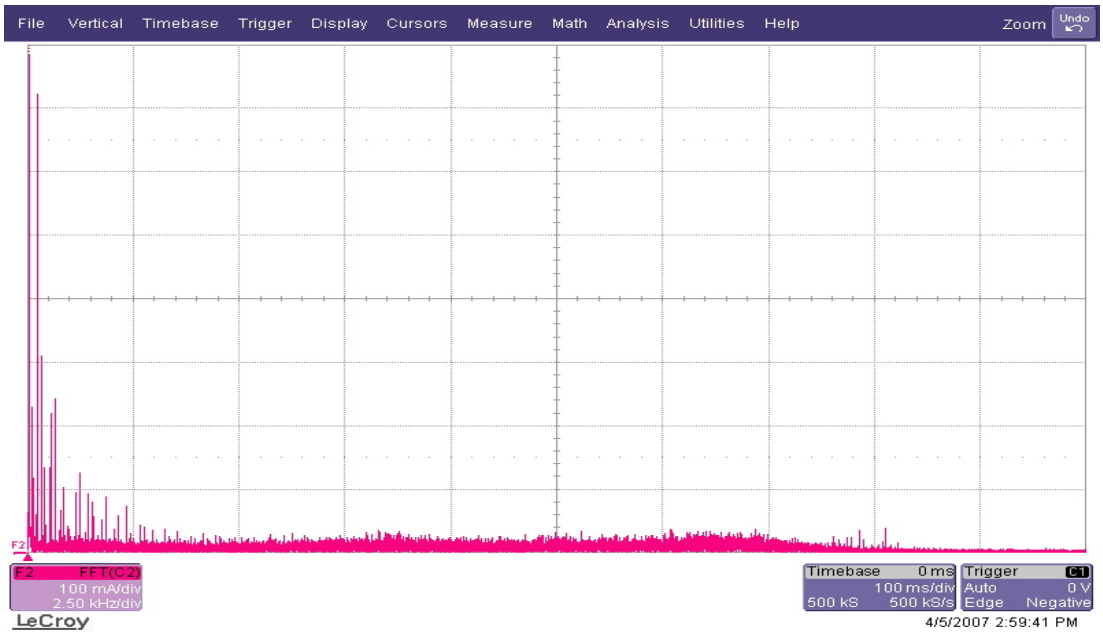

Figure 6.31 The experimental line current harmonic spectrum of the PAF system with SRF for DHCR3 (scales: 100 mA/div, 2.5 kHz/div).

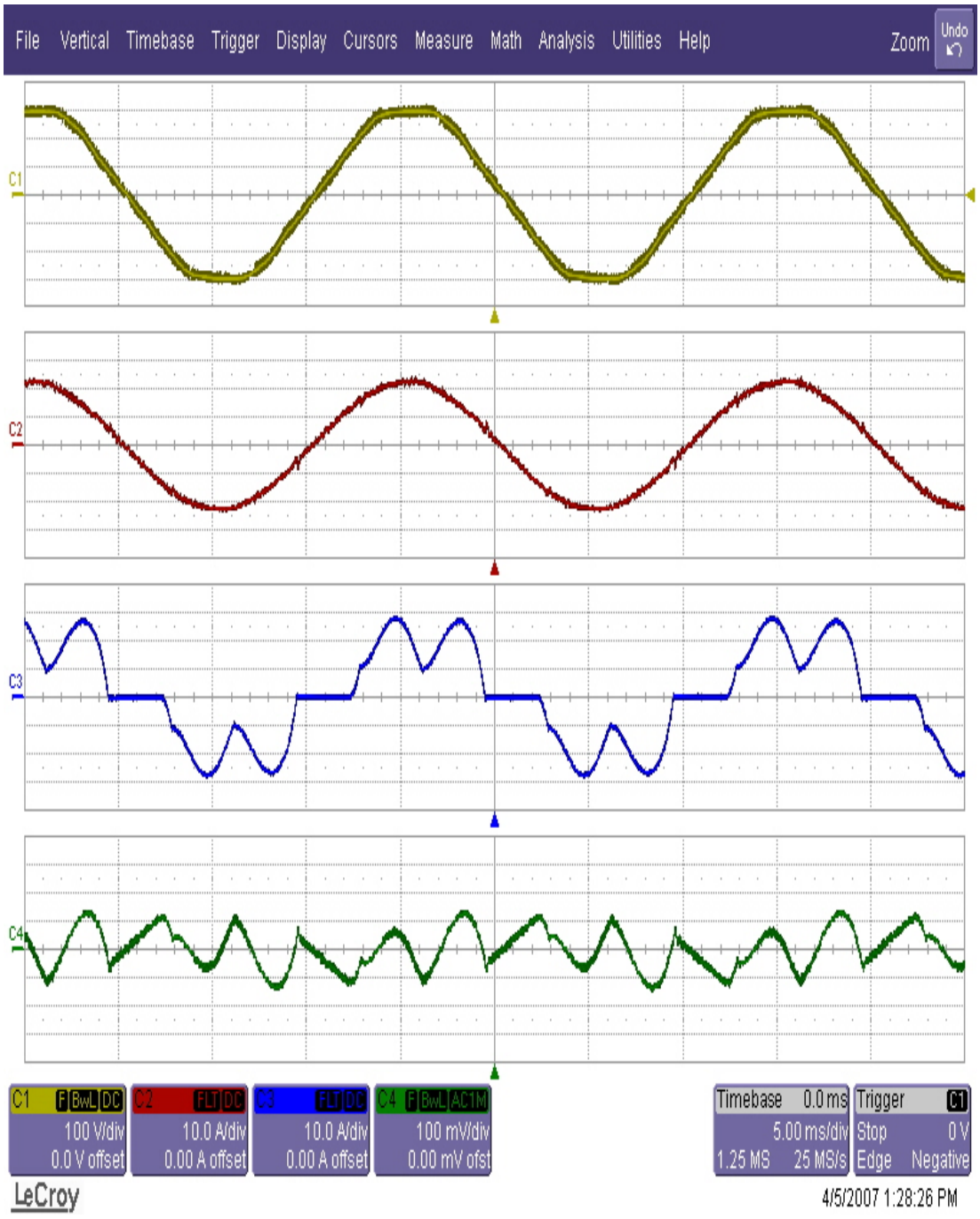

Figure 6.32 The experimental steady-state waveforms illustrating the detailed performance of the PAF system with SRF for RFCR: line voltage (yellow, 100 V/div), line current (red, 10 A/div), load current (blue, 10 A/div), and the PAF current (green, 10 A/div) (time axis: 5 ms/div).

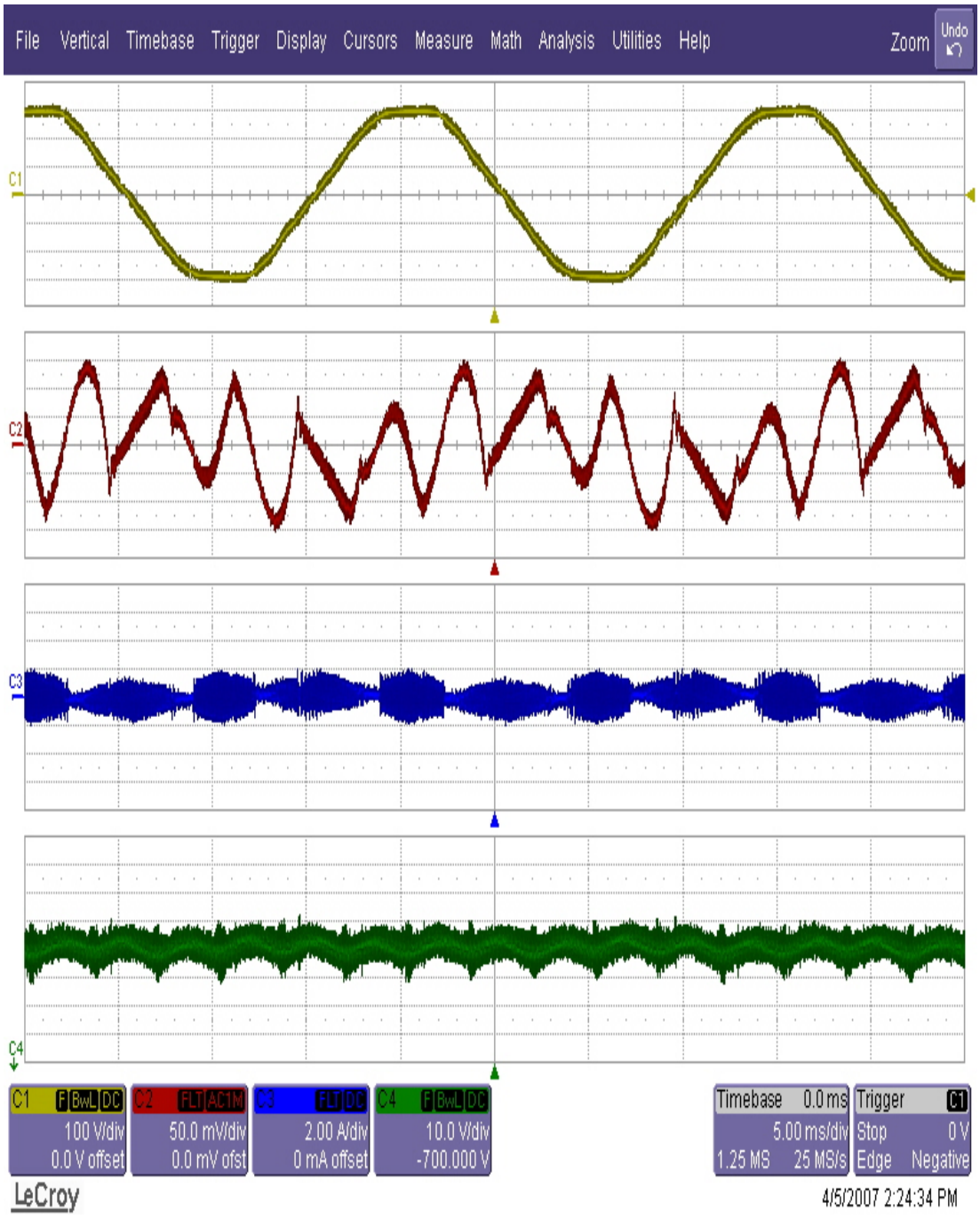

Figure 6.33 The experimental steady-state waveforms illustrating the detailed performance of the PAF system with SRF for RFCR: line voltage (yellow, 100 V/div), the PAF current (red, 10 A/div), the SRF current (blue, 2 A/div), and the PAF DC bus voltage (green, 10 V/div, -700 V offset) (time axis: 5 ms/div).

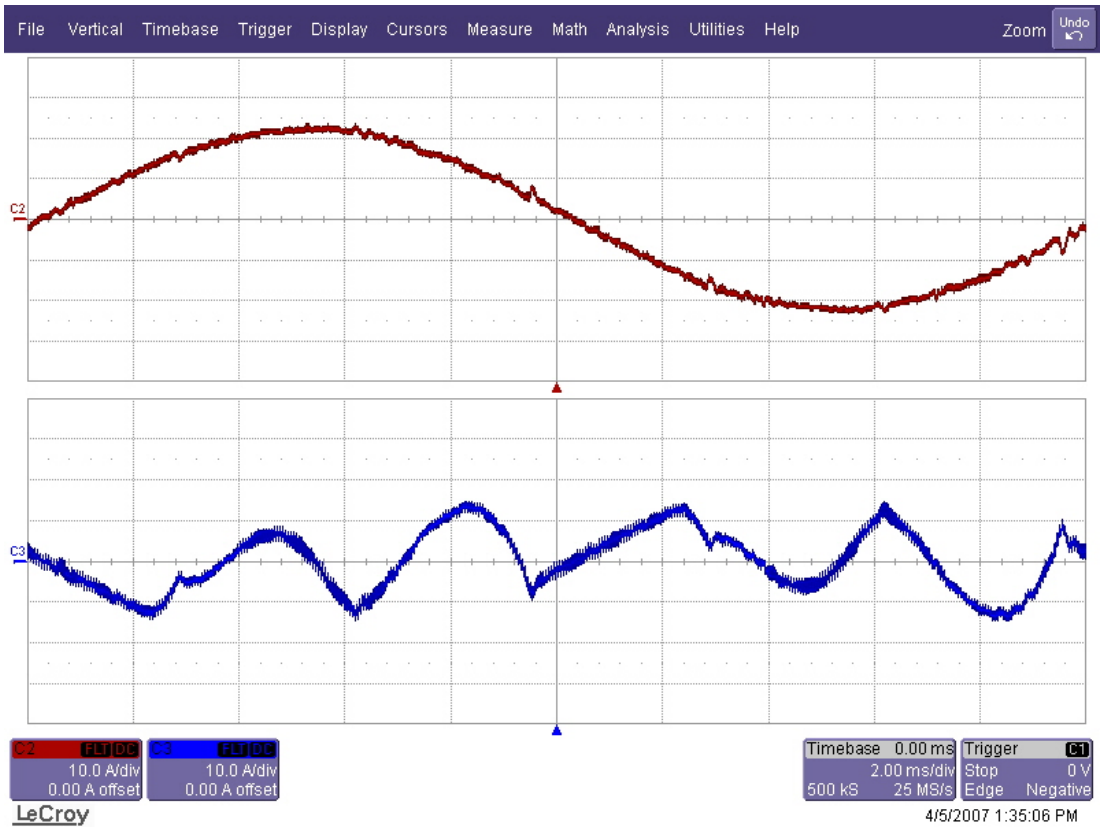

Figure 6.34 The experimental steady-state line current (red, 10 A/div) and filter current reference (blue, 10 A/div) of the PAF system with the SRF for RFCR (time axis: 2 ms/div).

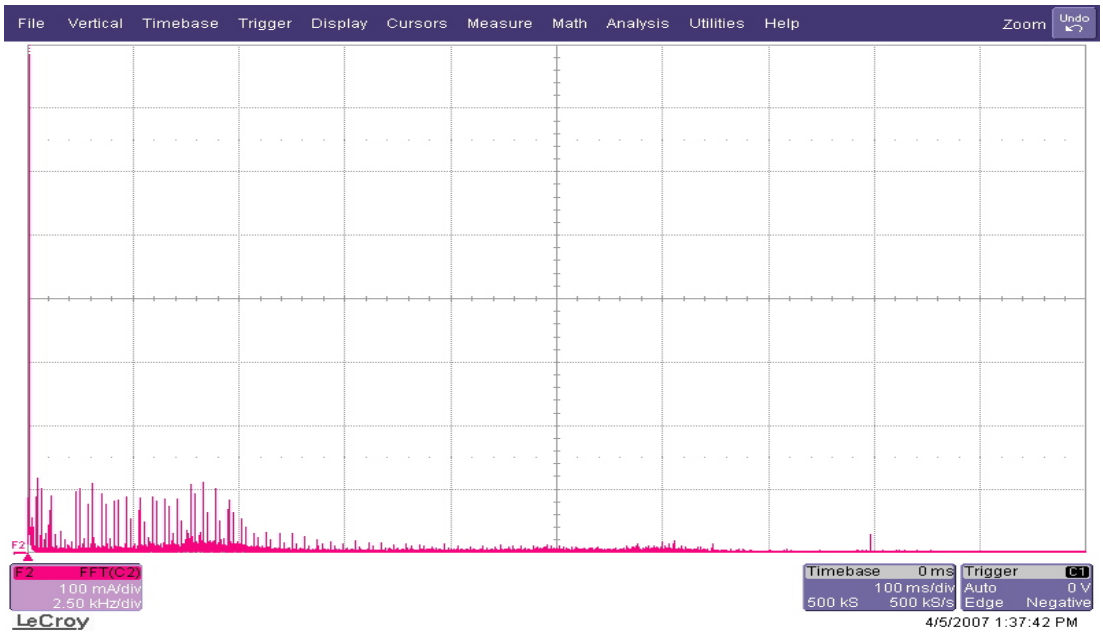

Figure 6.35 The experimental line current harmonic spectrum of the PAF system with the SRF for RFCR (scales: 100 mA/div, 2.5 kHz/div).

Table 6.15 The experimental steady-state power flow data for the AC utility grid, diode rectifier load, and the PAF system with SRF for DHCR3 and RFCR

	Load current/phase (Arms)	Line current/phase (Arms)	Filter current/phase (Arms	SRF current/phase (Arms)	Line voltage/phase (Vms)	Load Power (kVA) (PF=0.920)	Line Power (kVA) (PF=0.997)	Filter Power (kVA)
DHCR3	16.8	16.0	6.4	2.2	220	11.1	10.6	4.2
RFCR	16.8	16.0	7.3	0.7	220	11.1	10.6	4.8

6.6.3 The Experimental PAF Dynamic Performance

The dynamic response of the PAF system for the changes in operation conditions will be investigated experimentally in this subsection in order to verify the computer simulation results. As in the computer simulation part, the behavior of the PAF system when it start the harmonic compensation of the diode rectifier load operating at the rated output power of 10 kW is the first dynamic performance study. In this subsection, the PAF system with SRF utilizes the DHCR3. Figure 6.36 illustrates the experimental waveforms of load current, line current, PAF current, and PAF DC bus voltage when PAF starts the harmonic compensation of the diode rectifier load operating at the rated output power of 10 kW. Moreover, Figure 6.36 is the detailed illustration of Figure 6.34 at the instant of the harmonic compensation start. Since the current reference from the harmonic current reference generator is ready in the PAF control algorithm, the line current becomes sinusoidal with nearly zero settling time. The DC bus voltage of the PAF is nearly constant at its reference value of 700 V. The experimental waveforms in Figure 6.36 and Figure 6.37 are similar to the ones obtained in the computer simulation for the same case analyzed above, which verifies the PAF dynamic response obtained in computer simulation when the PAF system starts the harmonic compensation of the diode rectifier load operating at the rated output power of 10 kW.

The experimental waveforms of the load current, line current, PAF current, and PAF DC bus voltage for the system is illustrated in Figure 6.38 for the case when the

diode rectifier load is brought from 0% loading to the 75% loading suddenly meanwhile the PAF system has received the harmonic compensation start command. Figure 6.39 is the detailed illustration of Figure 6.38 at the instant of the loading. Just before the loading, the line current is nearly zero and contains only the switching ripple currents although the SRF sinks the most of the ripple currents that VSI creates. Just after the loading, the output of the harmonic reference generator can not be brought to its steady-state value immediately due to the low cut-off frequency (20 Hz) of the LPF utilized in the harmonic reference generator block. Therefore the line current gradually increases to its rated value following a sinusoidal shape. Since the LPF structure is utilized in harmonic current reference generator, the load real power demand is met by PAF, which results in 70 V drop at the DC bus of the PAF as explained and observed in the computer simulation part. Since the DC bus regulator in the experimental set-up has the same gains as in the PAF model in the computer simulation, the DC bus voltage is brought above the reference value of 700 V at around 100 ms and it settles down to its reference value at around 400 ms such that the experimental PAF dynamic response under the case when the diode rectifier load is brought the 0% loading to the 75% loading suddenly verifies the computer simulations results.

Another case study to investigate the PAF dynamic performance is the inverse of the previous case study such that the diode rectifier load is brought from 75% loading to the 0% loading suddenly. Figure 6.40 illustrates the system experimental waveforms of the load current, line current, filter current and DC bus voltage of the PAF system which encounters the change of the nonlinear load output power from 7.5 kW to 0 kW while the PAF compensates the load current harmonics and reactive power component. The DC bus voltage encounters an overshoot of nearly 60 V due to the real power transfer from the line since the harmonic reference generator gives an real power component due to the LPF structure in this case of the nonlinear load change from 75% loading to 0% loading (the reverse of the previous case study). The settling time for the DC bus voltage to its reference value is nearly 400 ms. The above experimental dynamic response studies for the PAF system with SRF for DHCR3 verify the computer simulation results and waveforms.

Figure 6.36 The experimental waveforms of the PAF system with SRF for DHCR3 when it starts the harmonic compensation of the diode rectifier load operating at the rated output power of 10 kW: Load current (yellow, 10 A/div), line current (red, 10 A/div), the PAF current (blue, 10 A/div), and the PAF DC bus voltage (green, 10 V/div, -700 V offset) (time axis: 50 ms/div).

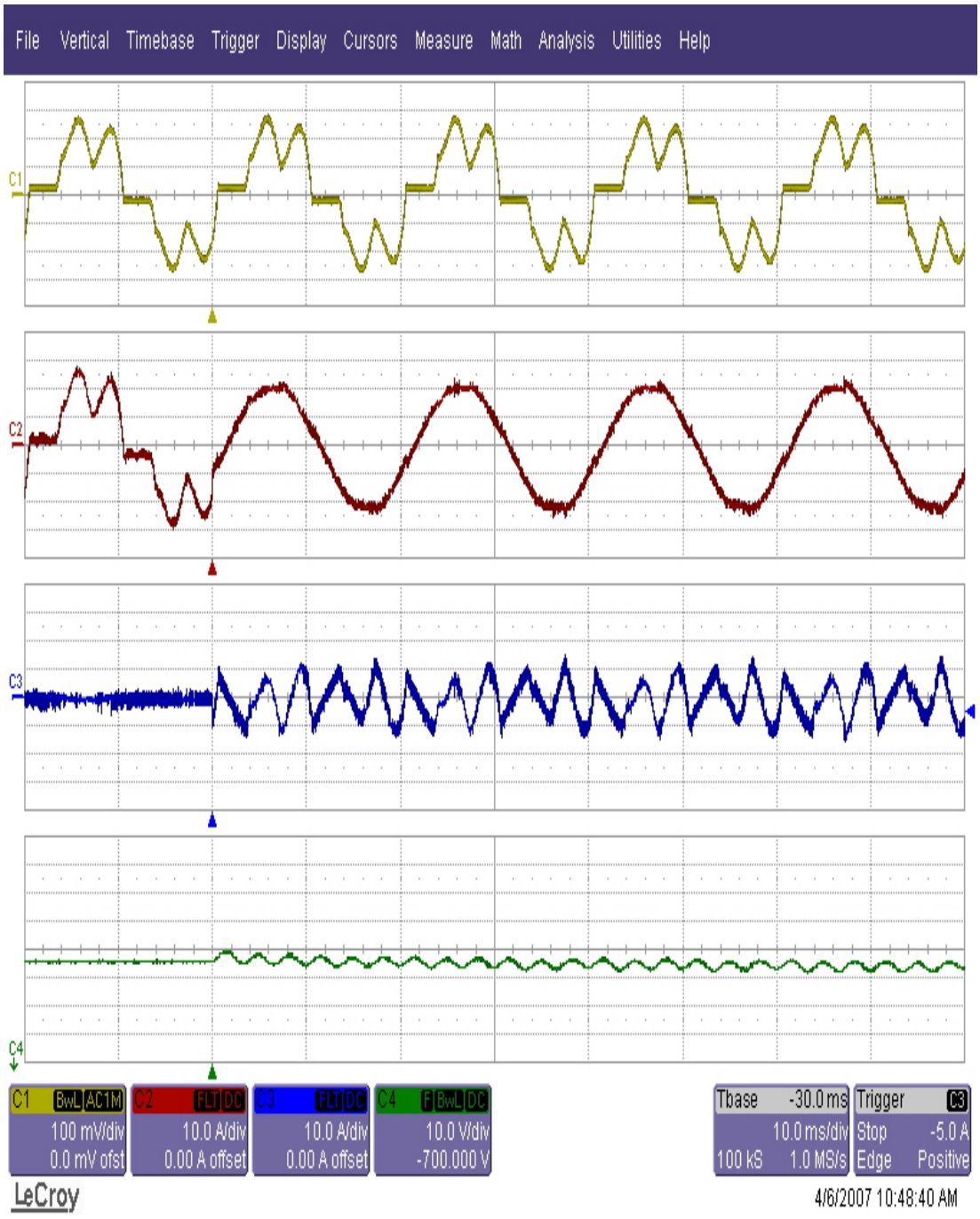

Figure 6.37 The detailed illustration of Figure 6.36 at the instant when the PAF starts the harmonic compensation.

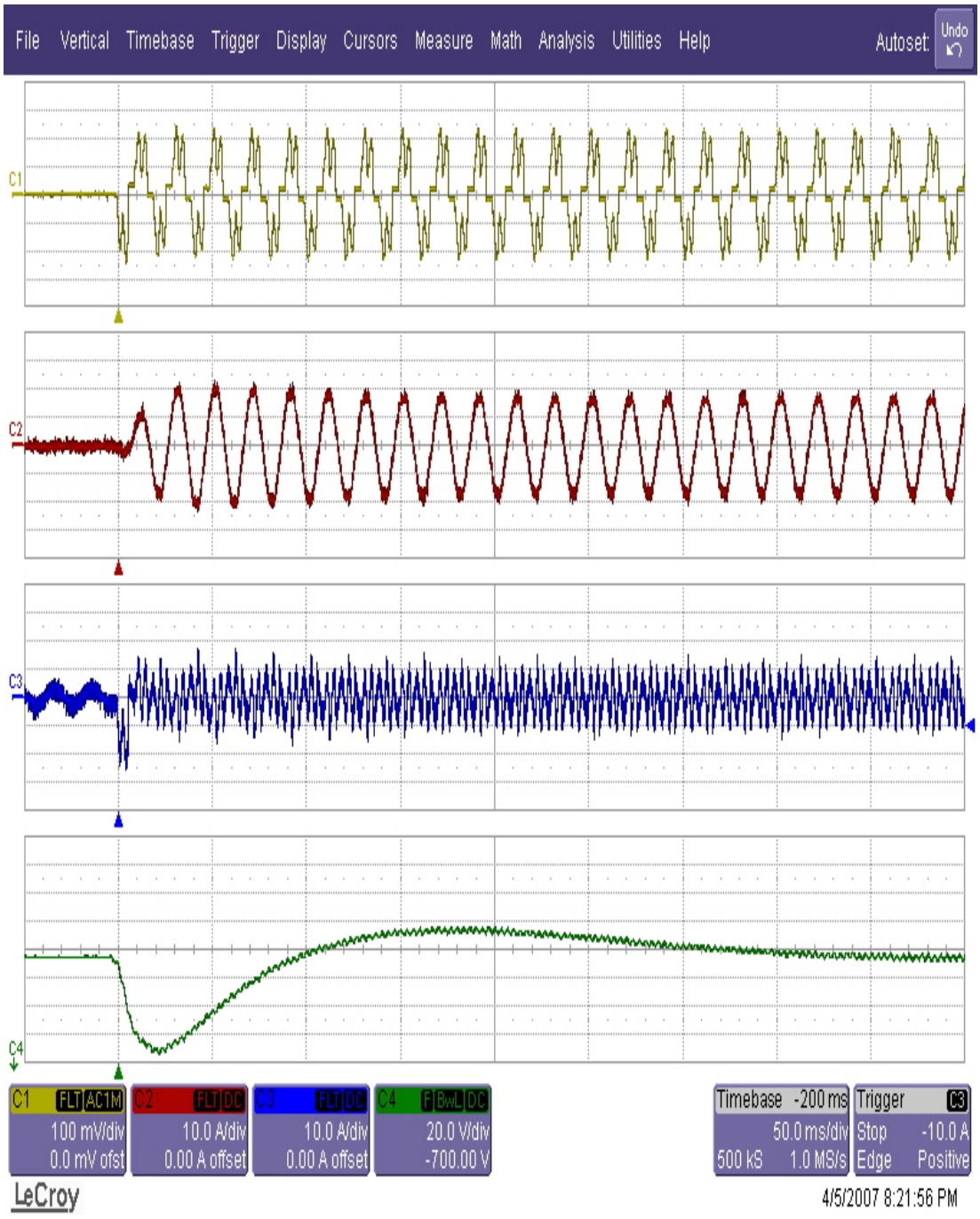

Figure 6.38 The experimental waveforms of the PAF system with SRF for DHCR3 when it starts the harmonic compensation of the diode rectifier load brought from 0% loading to 75% loading suddenly: Load current (yellow, 10 A/div), line current (red, 10 A/div), the PAF current (blue, 10 A/div), and the PAF DC bus voltage (green, 20 V/div, -700 V offset) (time axis: 50 ms/div).

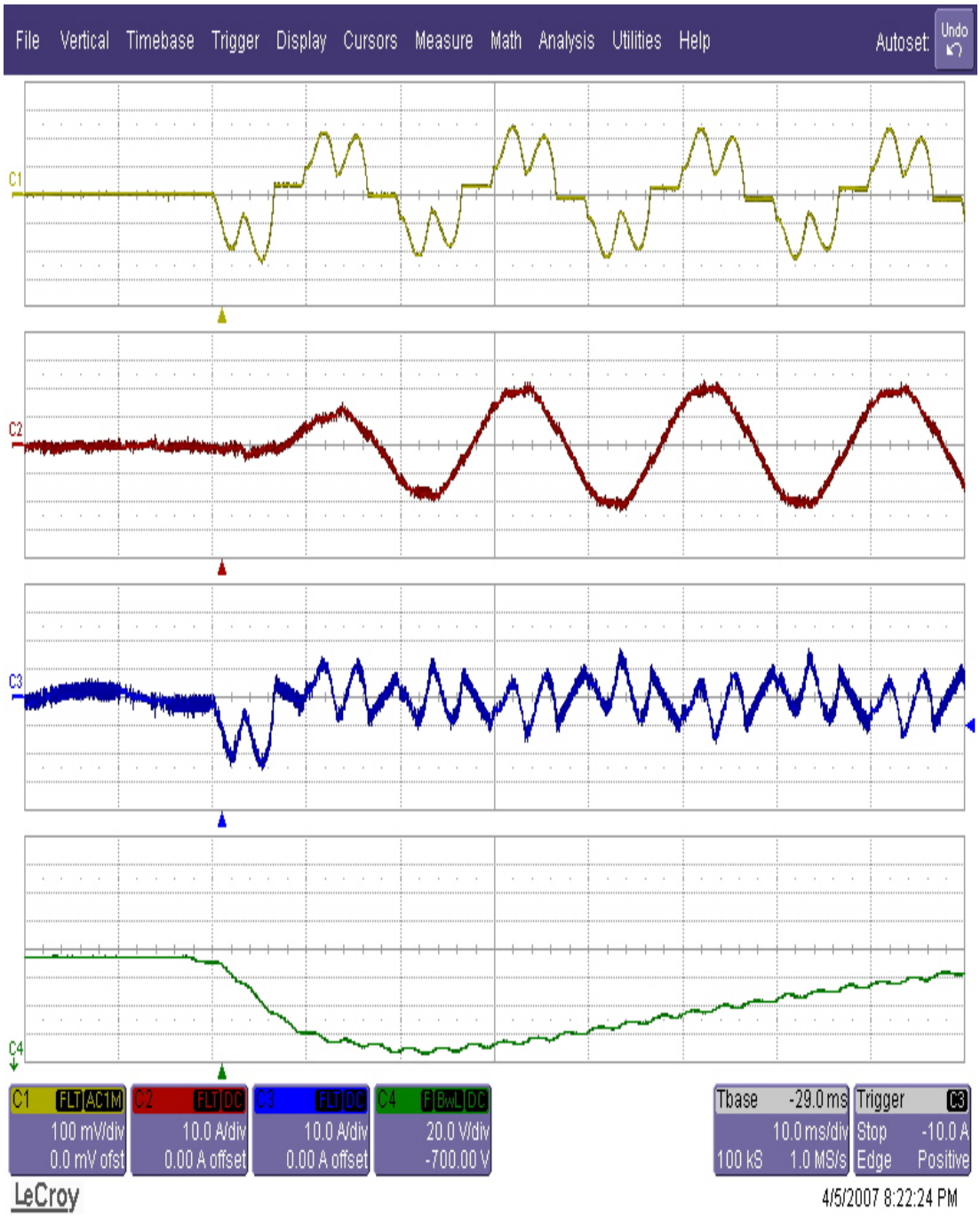

Figure 6.39 The detailed illustration of Figure 5.38 at the instant when the diode rectifier load is brought from 0% loading to 75% loading suddenly.

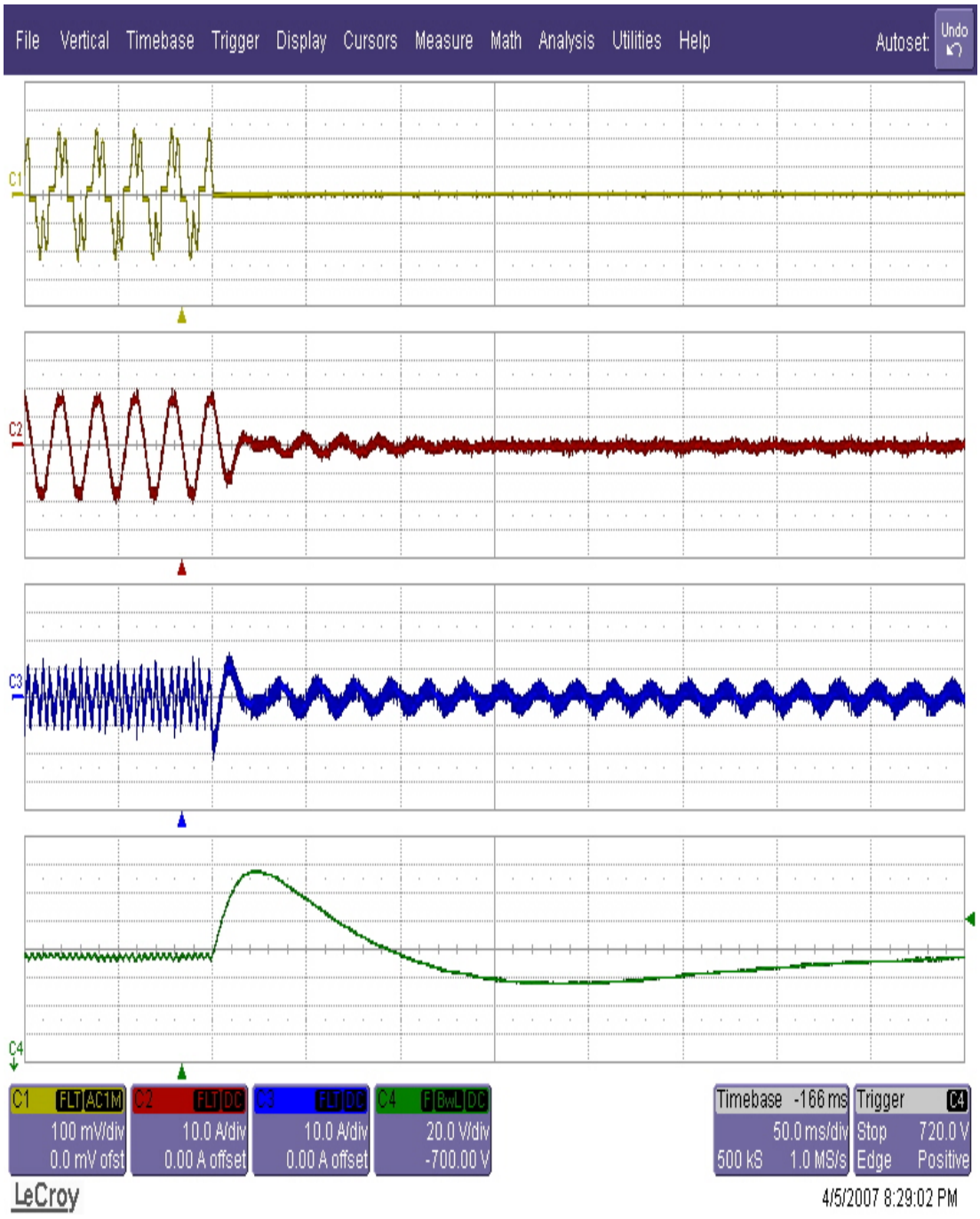

Figure 6.40 The experimental waveforms of the PAF system with SRF for DHCR3 when it starts the harmonic compensation of the diode rectifier load brought from 75% loading to 0% loading suddenly: Load current (yellow, 10 A/div), line current (red, 10 A/div), the PAF current (blue, 10 A/div), and the PAF DC bus voltage (green, 20 V/div, -700 V offset) (time axis: 50 ms/div).

6.7 Experimental PAF Performance Analysis for The Thyristor Rectifier Load

In this section, the experimental results of the designed PAF system connected in parallel to the thyristor rectifier are presented. The firing angle of the tyristor rectifier can be adjusted such that the reactive power demand of the nonlinear load can be increased to the desired reactive power demand as in the computer simulation part. The parameters of the thyristor rectifier utilized in the experimental studies are same as in computer simulation part and are given in Table 5.18. When the thyristor rectifier is operated with the output power of 10 kW with a=0°, the behavior of the thyristor rectifier load is not different from the diode rectifier load as explained in the computer simulation part. Therefore, the experimental waveforms for the AC utility grid, thyristor rectifier with a=0°, the PAF system will not be illustrated due to the similarity of the waveforms as in diode rectifier load case. The basic results will be summarized in a table for the thyristor rectifier with a=0° and the PAF utilizing two superior current regulators, DHCR3 and RFCR. Then the PAF performance for the thyristor rectifier operation at an output power of 10 kW and a=30°, which results in load PF value of 0.82, will be presented as in the computer simulation part.

The negative sequence current compensation capability of the PAF system with only positive sequence SRFC will not be illustrated experimentally contrary to the computer simulation studies since the adjusting the firing angle of the thyristor rectifier or the creation of the line voltage unbalanced is hard task in practice.

6.7.1 The Experimental PAF Performance for The Thyristor Rectifier Load with a=0°

Table 6.16 summarizes the experimental steady-state performance of the PAF system for the harmonic current and reactive power compensation of the thyristor rectifier operating at the output power of 10 kW and firing angle of 0°. Table 6.16 includes the load current harmonics, line current harmonics, and IEEE 519 harmonic limits up to 50^{th} harmonic current component for two current regulators, DHCR3 and RFCR, utilized for PAF system. Moreover, it includes THD_I, THD_V, PF, and f_{AVG}

for the two high performance current regulators, DHCR3 and RFCR. The THD_I and THD_V values and the individual harmonic current component percentages for two regulators are below the IEEE 519 limits. The PF value for both current regulators is unity and the f_{AVG} value for RFCR is 13.3 kHz while the f_{AVG} value for DHCR3 is 10.0 kHz as in the diode rectifier case. The computer simulation and experimental results for the thyristor rectifier with a=0°are compared in Table 6.17 in terms of THD_I, THD_V, PF, and f_{AVG} values for both current regulators. The experimental results are consistent with the computer simulations results except the THD_V value due to the voltage harmonics on the line voltage as discussed previously. The steady-state power flow data for the AC utility grid, the thyristor rectifier load operating at a=0° and the PAF system with DHCR3 and RFCR is given in Table 6.18. As in the diode rectifier case, while the load power and the line power for both regulators are same as expected, the power rating of the PAF is different for the DHCR3 and the RFCR due to the different capacitor sizes of the utilized SRFs. Since the load current THD value of 25.9% for the thyristor rectifier with a=0° is lower than the load current THD value of 37.5% for the diode rectifier load, the power rating of the PAF for the thyristor rectifier is less than the power rating of the PAF for the diode rectifier which given in Table 6.15 for the same nonlinear load output power of 10 kW and both current regulators. The experimental steady-state results for the thyristor rectifier load operating at the firing angle value of 0° verifies the computer simulations results such that the performance of the PAF for the thyristor rectifier with a=0° is as expected.

Table 6.16 The experimental line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for the PAF system with DHCR3 and RFCR for the thyristor rectifier load with $a = 0^o$, and IEEE 519 limits.

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%) DHCR3	Line Current Harmonics with PAF (%) RFCR	IEEE 519 Harmonic Current Limits (I_{SC}/I_{L1}=17 3) (%)
I_1	100.0	100.0	100.0	100.0
I_5	23.4	2.6	0.3	12.0
I_7	8.2	1.2	0.4	12.0
I_{11}	6.4	0.8	0.2	5.5
I_{13}	3.5	0.3	0.1	5.5
I_{17}	2.3	0.8	0.1	5.0
I_{19}	1.6	0.6	0.1	5.0
I_{23}	1.0	0.3	0.4	2.0
I_{25}	0.6	0.2	0.2	2.0
I_{29}	0.8	0.4	0.4	2.0
I_{31}	0.4	0.2	0.2	2.0
I_{35}	0.5	0.4	0.4	1.0
I_{37}	0.4	0.3	0.3	1.0
I_{41}	0.4	0.4	0.4	1.0
I_{43}	0.3	0.3	0.3	1.0
I_{47}	0.3	0.2	0.4	1.0
I_{49}	0.2	0.2	0.3	1.0
THD_I (%)	25.9	3.8	2.1	15.0
THD_V (%)	2.6	2.6	2.6	5.0
PF	0.960	0.995	0.997	---
f_{AVG}(kHz)		10.0	13.3	

Table 6.17 Computer simulation and experimental performance results of the PAF system for DHCR3 and RFCR in the case of the thyristor rectifier with a=0°

		Computer Simulation				Experiment			
	CR Type	THD_I (%)	THD_V (%)	PF	f_{AVG} (kHz)	THD_I (%)	THD_V (%)	PF	f_{AVG} (kHz)
Load Current		25.6	0.4	0.950		25.9	2.6	0.960	
Line Current	DHCR3	4.2	1.4	0.999	10.0	3.8	2.6	0.995	10.0
	RFCR	2.2	0.8	0.999	13.3	2.1	2.6	0.997	13.3
IEEE 519 Limits		15.00	5.00			15.00	5.00		

Table 6.18 The experimental steady-state power flow data for the AC utility grid, thyristor rectifier load operating at a=0°, and the PAF system with the SRF for DHCR3 and RFCR

	Load current/phase (Arms)	Line current/phase (Arms)	Filter current/phase (Arms)	SRF current/phase (Arms)	Line voltage/phase (Vms)	Load Power (kVA) (PF=0.960)	Line Power (kVA) (PF=0.997)	Filter Power (kVA)
DHCR3	16.7	16.2	4.5	2.2	220	11.0	10.7	3.0
RFCR	16.7	16.2	5.8	0.7	220	11.0	10.7	3.8

6.7.2 The Experimental PAF Performance for The Thyristor Rectifier Load with a= 30°

This subsection presents the experimental results of the PAF system for the thyristor rectifier operated with a firing angle value of 30° at the rated output power of 10 kW. This operating condition for the rectifier increases the reactive power demand such that the resulting PF value at the input terminals of the rectifier is 0.82 as in the computer simulation part. The reactive power compensation capability and the performance of the PAF for both superior current regulators, DHCR3 and the RFCR, will be investigated experimentally.

The experimental steady-state performance of the PAF for DHCR3 and RFCR is summarized in Table 6.19. Table 6.19 includes load current harmonics of the thyristor rectifier with a=30°, line current harmonics, IEEE 519 harmonic limits up to 50th harmonic current component, THD_I, THD_V, PF, and f_{AVG} for DHCR3 and RFCR. Figure 6.41 respectively illustrates experimental steady-state the voltage at the PCC (line voltage), the line current, the load current, and the PAF current for 'phase a' and Figure 6.42 respectively illustrates the experimental steady-state line voltage, the PAF current and the SRF current for phase 'a', and the DC bus voltage waveforms of PAF system, which utilizes the DHCR3 and the designed high-pass

RC type SRF for the compensation of the harmonics and reactive current component of the thyristor rectifier load with *a*=30°. The detailed illustration of the line current and the PAF current is illustrated in Figure 6.43 for the PAF system with DHCR3. The experimental line current harmonic spectrum over a wide frequency range for DHCR3 is illustrated in Figure 6.44. Similarly, Figure 6.45 respectively illustrates experimental steady-state the voltage at the PCC (line voltage), the line current, the load current, and the PAF current for 'phase *a*' and Figure 6.46 respectively illustrates the experimental steady-state line voltage, the PAF current and the SRF current for phase '*a*', and the DC bus voltage waveforms of PAF system, which utilizes the RFCR and the designed tuned LCR type SRF for the thyristor rectifier load with *a*=30°. Figure 6.47 presents the detailed illustration of the line current and the PAF current while Figure 6.48 illustrates the line current harmonic spectrum or the PAF system with RFCR. As in computer simulation part, the load current harmonics are suppressed up to the 31st harmonic where the compensation of the higher order harmonics is partial. The thyristor rectifier operating with *a*=30° results in the higher di/dt value (approximately 50 A/ms) compared to the thyristor rectifier operating with *a*=0° of diode rectifier (approximately 20 A/ms). The increase in di/dt value results the performance degradation of the PAF system. This current reference tracking degradation in high di/dt creates current spikes on the line current waveform for both current regulators as discussed in the computer simulation part. Although there exist current spikes due to the high di/dt value of the load current during the commutation intervals, the experimental line current THD_I value is 6.2% for DHCR3 and 5.4% for RFCR illustrates the PAF system superior performance in harmonic current compensation. Moreover, the PF value is approximately unity with the value of 0.99 for both current regulators while the load side PF value is 0.82. This illustrates the reactive power compensation capability of the PAF. As in the computer simulation part, the high di/dt demand of the current reference results in the saturation of the inverter during the commutation intervals of the load current and results in a lower f_{AVG} values for both current regulators compared to the case of thyristor rectifier with *a*=0° or diode rectifier. The computer simulation and experimental results for the thyristor rectifier with *a*=0° are compared in Table 6.20 in terms of THD_I, THD_V, PF, and f_{AVG} values for both current regulators. The

experimental waveforms and the performance of the PAF for the thyristor rectifier are consistent with the computer simulation results such that the experimental performance of the PAF meets IEEE 519 and reactive power limitations in Turkey.

Table 6.21 presents the experimental steady-state power flow data for the AC utility grid, thyristor rectifier load operating at a=30°, and the PAF system for DHCR3 and RFCR. The load power is increased compared to the diode rectifier case or thyristor rectifier with a=0° since the reactive power demand of the nonlinear load is increased for the same real power demand in the case of the thyristor rectifier with a=30°. Therefore, since the PAF compensates the harmonics and the reactive power demand of the thyristor rectifier, the PAF power rating also increases. However, the PAF power rating is different for the DHCR3 and RFCR cases due to the different capacitor sizes for the utilized SRFs. The experimental data in Table 6.21 has higher values compared to the data in Table 5.22 obtained for the computer simulation due to the power losses with the circuit elements involved in the experimental studies. However, the data in both tables is consistent with each other.

In this subsection, the reactive power compensation of the designed and manufactured PAF system, which results in increase of the PAF rating, is illustrated with a strong correlation with the computer simulation results. Unavoidable performance degradation of the PAF current regulation due to the high di/dt content of the current reference in the case of the thyristor rectifier with a=30° is experimentally illustrated. However, this performance degradation does not result in violation of IEEE 519 harmonic limitations. Further, this section is the experimental verification of the superior performance of the DHCR3 with its reduced f_{AVG} compared to the linear current regulators in the case of the thyristor rectifier with a=30°. In this operating condition, the PAF system with DHCR3 results in a comparable THD_I value of 6.2% with a lower f_{AVG} value of 9.2 kHz compared to the RFCR with THD_I value of 5.4% and a f_{AVG} value of 12.2 kHz.

Table 6.19 The experimental line current harmonics, THD_I, THD_V, PF at PCC, and f_{AVG} for the PAF system with DHCR3 and RFCR and the thyristor recitifer load with $a = 30^{\circ}$, and IEEE 519 limits.

	Line Current Harmonics without PAF (%)	Line Current Harmonics with PAF (%) DHCR3	Line Current Harmonics with PAF (%) RFCR	IEEE 519 Harmonic Current Limits (I_{SC}/I_{L1}=173) (%)
I_1	100.0	100.0	100.0	100.0
I_5	26.5	1.8	0.5	12.0
I_7	12.8	2.4	0.6	12.0
I_{11}	10.0	2.1	0.4	5.5
I_{13}	5.1	1.5	0.3	5.5
I_{17}	5.1	1.6	0.4	5.0
I_{19}	3.2	1.9	0.4	5.0
I_{23}	3.2	1.2	1.2	2.0
I_{25}	2.1	1.2	1.2	2.0
I_{29}	2.2	1.1	1.0	2.0
I_{31}	1.5	1.0	1.1	2.0
I_{35}	1.6	0.9	1.0	1.0
I_{37}	1.1	0.7	0.7	1.0
I_{41}	1.2	0.7	0.8	1.0
I_{43}	0.7	0.6	0.6	1.0
I_{47}	0.9	0.6	0.7	1.0
I_{49}	0.5	0.5	0.4	1.0
THD_I (%)	31.1	6.2	5.4	15.0
THD_V (%)	2.6	2.6	2.6	5.0
PF	0.82	0.990	0.991	---
f_{AVG} (kHz)		9.2	12.2	

Table 6.20 Computer simulation and experimental performance results of the PAF system for DHCR3 and RFCR in the case of the thyristor rectifier with a=30°

		Computer Simulation				Experiment			
	CR Type	THD_I (%)	THD_V (%)	PF	f_{AVG} (kHz)	THD_I (%)	THD_V (%)	PF	f_{AVG} (kHz)
Load Current		31.8	0.8	0.820		31.1	2.6	0.960	
Line Current	DHCR3	6.0	1.5	0.998	9.0	6.2	2.6	0.990	9.2
	RFCR	5.6	1.1	0.998	12.5	5.4	2.6	0.991	12.2
IEEE 519 Limits		15.00	5.00			15.00	5.00		

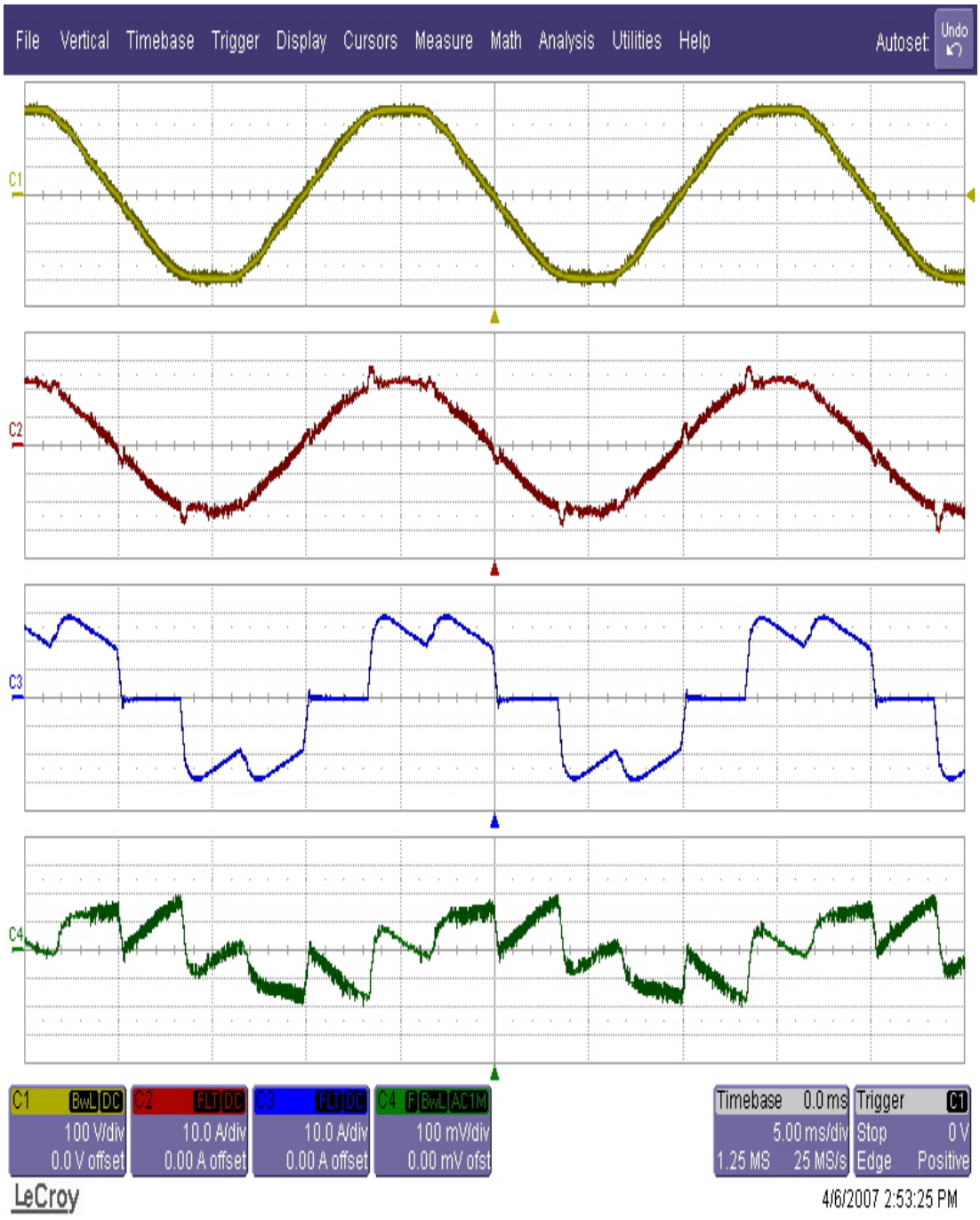

Figure 6.41 The experimental steady-state waveforms of the PAF system with SRF for DHCR3 for the thyristor rectifier load with a=30°: line voltage (yellow, 100 V/div), line current (red, 10 A/div), load current (blue, 10 A/div), and the PAF current (green, 10 A/div) (time axis: 5 ms/div).

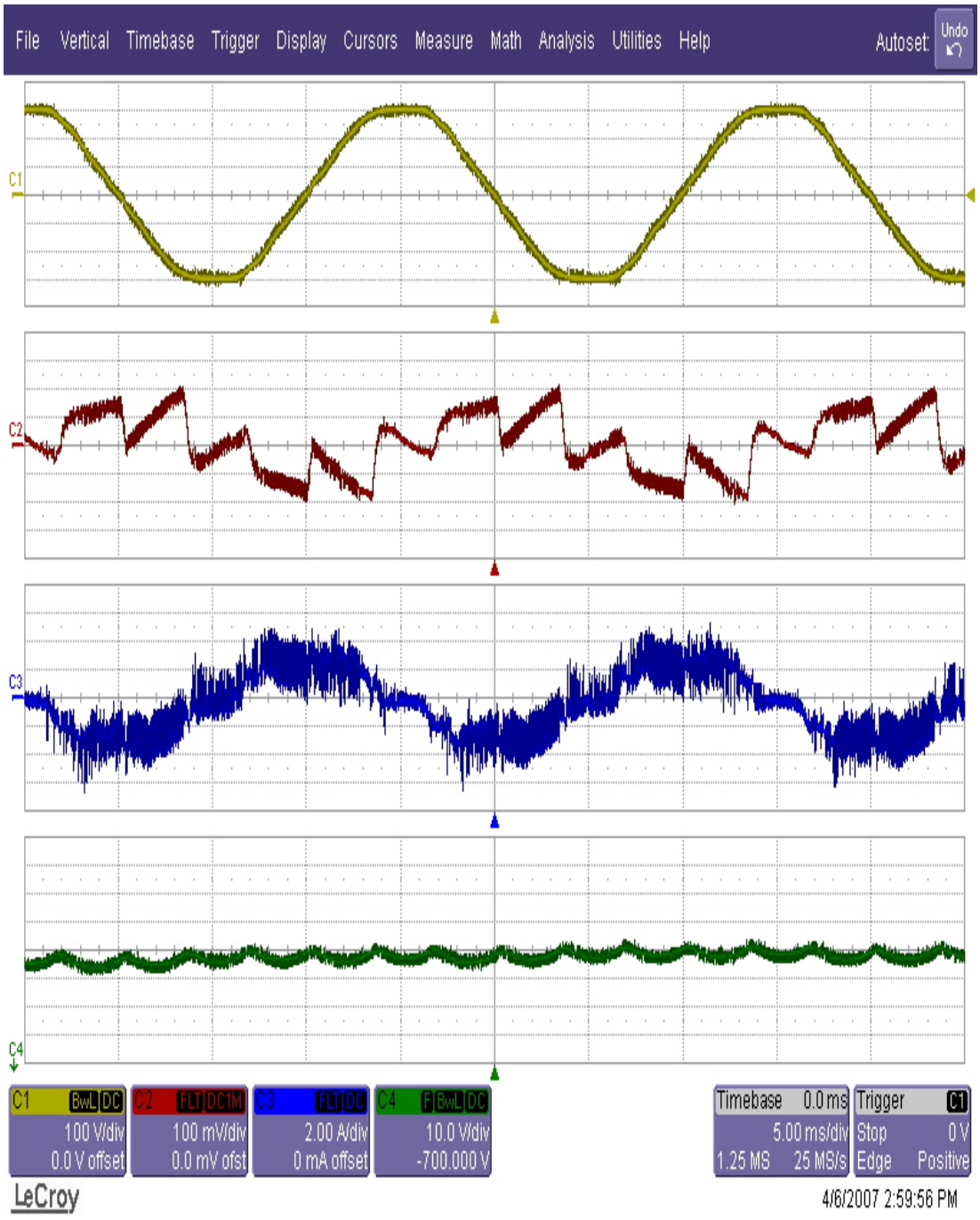

Figure 6.42 The experimental steady-state waveforms of the PAF system with SRF for DHCR3 for the thyristor rectifier load with a=30°: line voltage (yellow, 100 V/div), PAF current (red, 10 A/div), SRF current (blue, 2 A/div), and PAF DC bus voltage (green, 10 V/div, -700 V offset) (time axis: 5 ms/div).

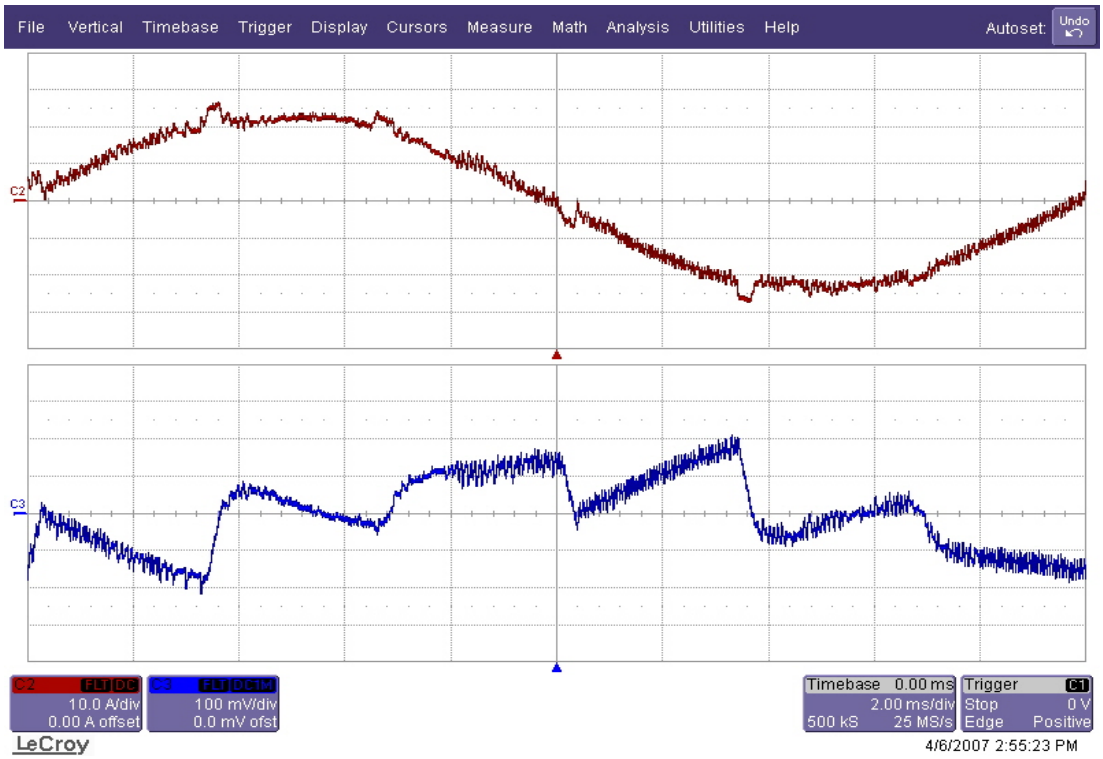

Figure 6.43 The experimental steady-state line current (red, 10 A/div) and filter current reference (blue, 10 A/div) waveforms of the PAF system with SRF for DHCR3 for the thyristor rectifier load with a=30° (time axis: 2 ms/div).

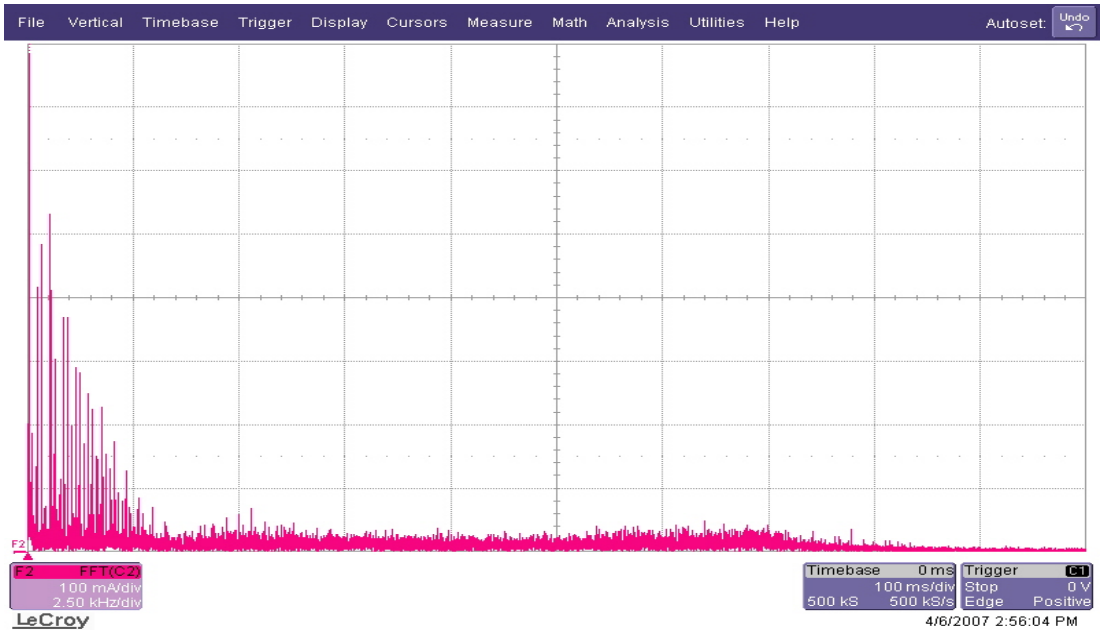

Figure 6.44 The experimental line current harmonic spectrum of the PAF system with SRF for the DHCR3 for the thyristor rectifier load with a=30° (scales: 100 mA/div, 2.5 kHz/div).

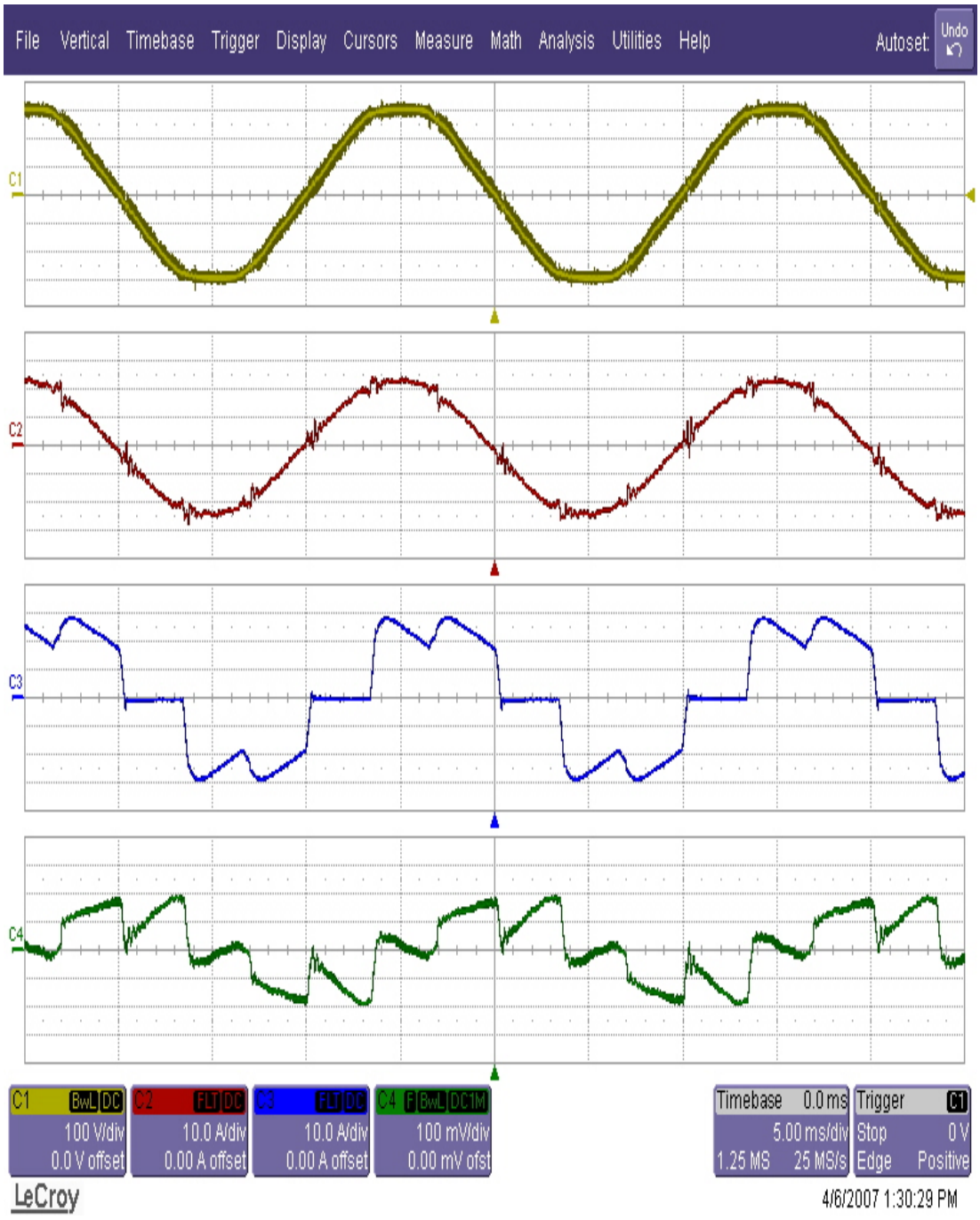

Figure 6.45 The experimental steady-state waveforms of the PAF system with SRF for RFCR for the thyristor rectifier load with a=30°: line voltage (yellow, 100 V/div), line current (red, 10 A/div), load current (blue, 10 A/div), and the PAF current (green, 10 A/div) (time axis: 5 ms/div).

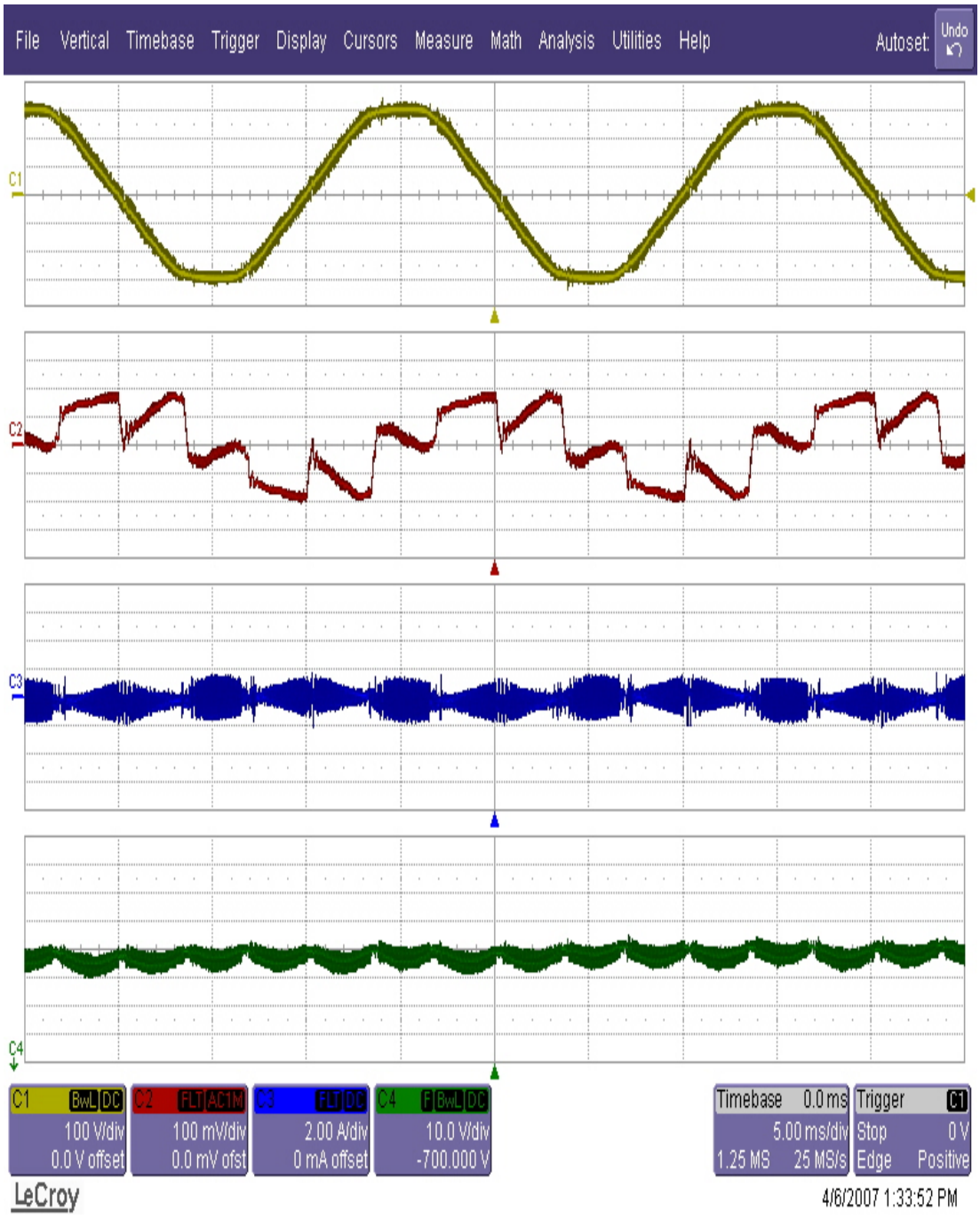

Figure 6.46 The experimental steady-state waveforms of the PAF system with SRF for RFCR for the thyristor rectifier load with a=30°: line voltage (yellow, 100 V/div), PAF current (red, 10 A/div), SRF current (blue, 2 A/div), and PAF DC bus voltage (green, 10 V/div, -700 V offset) (time axis: 5 ms/div).

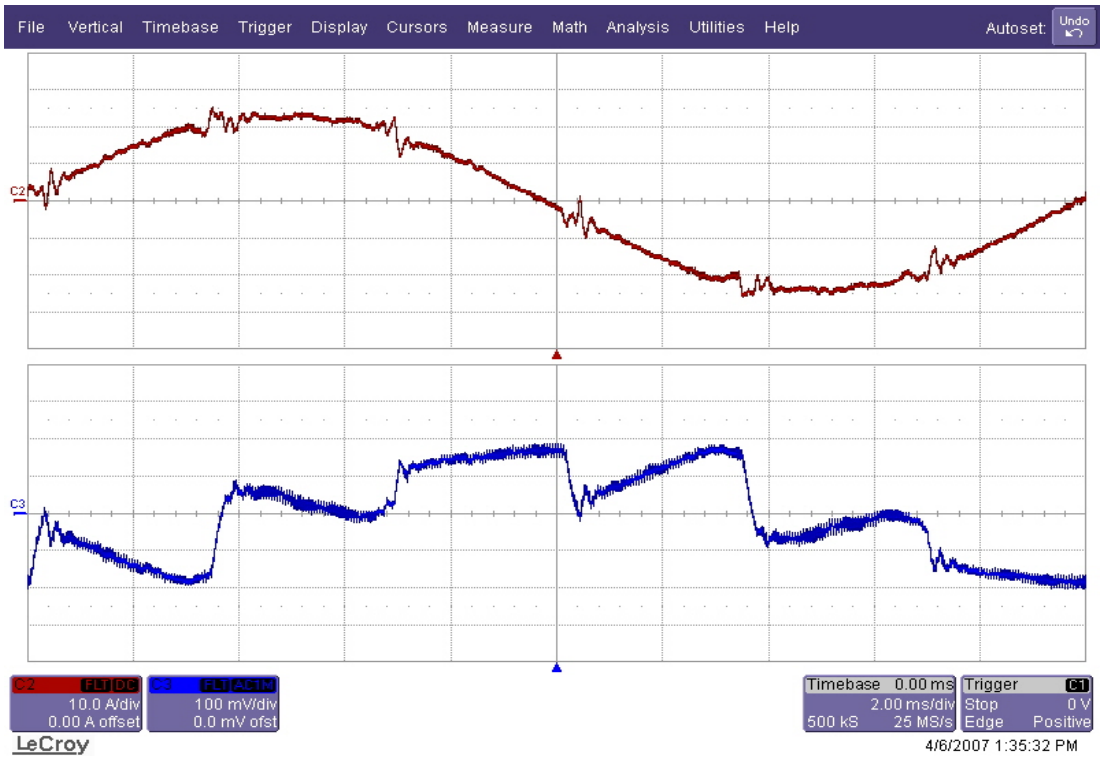

Figure 6.47 The experimental steady-state line current (red, 10 A/div) and filter current reference (blue, 10 A/div) waveforms of the PAF system with SRF for the RFCR for the thyristor rectifier load with a=30° (time axis: 2 ms/div).

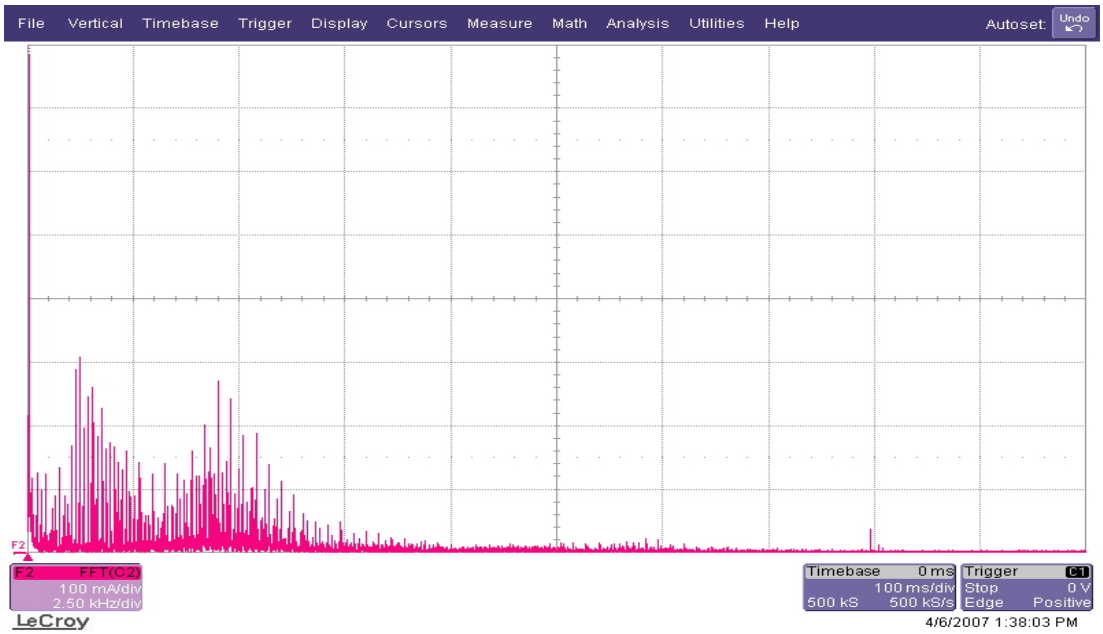

Figure 6.48 The experimental line current harmonic spectrum of the PAF system with SRF for RFCR for the thyristor rectifier load with a=30° (scales: 100 mA/div, 2.5 kHz/div).

Table 6.21 The experimental steady-state power flow data for the AC utility grid, thyristor rectifier load operating at a=30°, and the PAF system with the SRF for DHCR3 and RFCR

	Load current/phase (Arms)	Line current/phase (Arms)	Filter current/phase (Arms)	SRF current/phase (Arms)	Line voltage/phase (Vms)	Load Power (kVA) (PF=0.82)	Line Power (kVA) (PF=0.99)	Filter Power (kVA)
DHCR3	18.8	16.3	9.8	2.2	220	12.4	10.8	6.5
RFCR	18.8	16.3	11.9	0.7	220	12.4	10.8	7.9

6.8 Summary

In this chapter, the designed PAF system for the harmonic and the reactive power compensation of the harmonic current source type nonlinear load was investigated by means of experimental studies. First, the hardware description of the system was presented and the control algorithm implemented via DSP was explained in detail. The performance of the discrete time current regulator in the PAF application was analyzed by means of experimental studies such that the design studies in Chapter 3 and computer simulations studies of Chapter 5 were verified and an experimental comparison study was carried out. The experimental studies for the current regulators in this chapter illustrated that the RFCR and the proposed DHCR3 in this thesis have superior performances in PAF application as concluded in the computer simulation chapter. Moreover, the designed SRFs performances in Chapter 4 were verified by experimental work verifying the computer simulation results in Chapter 5. The detailed experimental steady-state and the dynamic response of the PAF system applied to the diode rectifier with the output power rating of 10 kW were illustrated. With the study of the reactive power compensation capability of the PAF system for the thyristor rectifier with the firing angle value of 30°, this chapter concludes such that experimental studies are in strong correlation with the theoretical studies of Chapter 2, Chapter 3, and Chapter 4 and computer simulation studies of Chapter 5.

CHAPTER 7

CONCLUSIONS

The parallel active filter is the modern solution to eliminate the harmonic current and reactive power related power quality problems in power systems. It is suitable for current sink type loads and it is applicable for loads with power ratings up to MVA levels. Implemented as a controlled current source, the PAF injects a compensating current into the system so that it cancels the harmonic current, the reactive power current, and the unbalanced current components of a harmonic current generating nonlinear load. As a result, the current drawn form the AC utility grid becomes sinusoidal, in phase with the line voltage, and balanced. This thesis is concerned with the design, control, and the implementation of a PAF for 3-phase 3-wire systems to comply with the harmonic standards of IEEE 519 and the reactive power limitations of the Turkish Electricity Authority.

The realization of the PAF as a controlled current source is directly related to its control algorithm which this thesis mainly deals with. The control algorithm of the PAF involves two main blocks; the current reference generator and current regulator. For high performance compensation, the current reference which consists of the harmonic current reference and the DC bus voltage regulating current reference should be as accurate as possible. The generated current reference signal is then sent to the current regulator that generates the switching signals of the VSI which chops the DC bus voltage to obtain the desired AC voltage at the VSI output terminals for the creation of the PAF reference current through the filter inductors. The current regulator tracking capability determines the PAF performance since the current reference in the PAF application consists of mainly the load current harmonics which

are characterized by their non-sinusoidal, multiple frequency, and high di/dt specifications. Hence, the current regulator is the most critical controller in the PAF control algorithm to achieve high performance current injection. In order to meet the stringent power quality harmonic standards, the PAF should compensate for a wide range of harmonics, which require a current regulator with high bandwidth and resolution. Hence, the task of the PAF current regulator is quite challenging. This thesis mainly involves the current regulation algorithms.

Since the VSI of the PAF operates at high switching frequencies in the range of kHz, high frequency switching ripple is generated at the PCC and power quality problems arise for the other loads connected to the same PCC. Therefore, adequate attenuation of the switching harmonics via a switching ripple filter (SRF) is mandatory from the point of power quality. Although the SRF topologies for the PAF application are well known, the technical literature lacks detailed SRF design guidelines and comparisons of SRF topologies. In addition to the current regulator study, this thesis also investigates the SRF topologies and their design.

This thesis is dedicated to the detailed analysis, design, control, and implementation of a 3-phase 3-wire PAF. Specifically, the current regulator and SRF parts are thoroughly investigated and contributions are made towards them. Further, the state of the art current regulation methods and the methods developed in this work are thoroughly compared such that the performance trade-offs well understood and the current regulator selection becomes an easy task for a given set of performance criteria. Additionally, comprehensive design, manufacturing, implementation, and performance test of a PAF for 10 kW diode rectifier is presented.

The main contribution of this thesis involves the PAF current regulators. State of the art current regulators are evaluated, a novel discrete time current regulator is proposed, and a thorough performance comparison is provided among these current regulators by means of simulations and experiments. Linear and hysteresis current regulators are considered. Through a case study of a 10kW rectifier load active filtering system, it is shown that the proposed discrete time hysteresis current

regulator with multi-rate current sampling and flexible PWM output, namely the DHCR3 method, exhibits a high bandwidth and a high dynamic response while limiting the maximum switching frequency for thermal stability and keeping the current regulator in its basic form for implementation simplicity. Through detailed simulations and laboratory tests the method is evaluated and compared to other high performance current regulators. Strong correlation between simulations and experiments was obtained and the experimental comparison study showed that LPCR, the recently developed RFCR, and DHCR3 provide satisfactory performance. With the properly designed SRFs included in the system, at rated rectifier load, the line current THD_I performances of these regulators are 4.0%, 2.3%, and 4.1% respectively. The average switching frequencies for these regulators are 13.3 kHz for the first two and 10.3 kHz for DHCR3 (25% less than the others) for the same maximum switching frequency of 20 kHz for all regulators. Considering that all the regulators meet the IEEE 519 THD_I requirements (which is 15%) quite safely and their THD_I values are very close to each other, DHCR3 becomes advantageous as it provides significant switching loss reduction and allows an easy/economical implementation. In addition to illustrating the DHCR3 performance via comparison to other regulators, the results of the current regulator performance comparison study could be a helpful guide for the PAF design and implementation engineers.

Another contribution of this thesis involves the SRF design. Based on the current regulator type employed, various SRF topologies are considered. These topologies are analyzed and based on the filtering characteristics and size investigations the SRF parameter design rules have been established. It has been concluded that the tuned LCR type SRF for linear current regulators and the high-pass RC type SRF for hysteresis current regulators are favorable due to their filtering efficiency, simple structures, and low cost for the designed PAF. Following the current regulator studies, this thesis provided detailed analysis, design, implementation, and test results of the PAF with the properly designed LCR and RC filters. It has been shown that with a properly designed SRF, the switching ripples could be suppressed such that the line current and the voltage at the PCC become switching ripple free.

With the major contributions being in the current regulator and SRF development and design, this thesis utilizes them to build a high performance PAF system. Utilizing a modern DSP system and programming all the control algorithms, the prototype PAF which has approximately 8 kVA was built and a 10 kW rating diode rectifier load and a 12.4 kVA thyristor rectifier load were tested. The steady-state and dynamic performance capabilities of the built system were demonstrated via laboratory tests. The manufactured PAF for the 10 kW diode rectifier satisfies the IEEE 519 THD_I harmonic limitations of 15% by providing THD_I value of less than 5% for all the discussed high performance current regulators. With its near unity power factor performance, quite safely it satisfies the power factor limitations of the Turkish Electric Authority. As a more demanding application of the PAF compared to the diode rectifier, the 12.4 kVA thyristor rectifier load which demands not only harmonic compensation but also significant amount of reactive power compensation. Also with its high di/dt requirement during the load current commutation intervals, it tests the current tracking capability of the current regulator. The experimental study showed that although current spikes exist on the line current waveform due to the high di/dt current reference in such an operation condition, the designed PAF system meets the IEEE 519 THD_I harmonic limitations of 15% by providing 5.6% THD_I value for RFCR and 6.0% THD_I value for DHCR3. Also the power factor limitations of the Turkish Electric Authority are met safely by providing approximately 0.99 for both regulators. The thyristor load case study for the PAF system illustrates that the designed PAF system performs satisfactorily under hard operation conditions while providing approximately harmonic free line current with unity power factor.

Overall, this thesis provides the detailed design, control, and implementation of a high performance 3-phase 3-wire PAF system. As the heart of the PAF system, a novel discrete time hysteresis current regulator, DHCR3, comparable THD_I performance to, lower average switching frequency than, and simpler implementation than the practically utilized current regulators is proposed and its performance is verified through simulations and experiments and via comparison to other current regulators. Including the SRF, the complete PAF system is designed and its experimental performance is demonstrated for a 10 kW rectifier load.

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