# A SINGLE TRANSISTOR UNITY POWER FACTOR RECTIFIER

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Approval of the Graduate School of Natural and Applied Sciences

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## ABSTRACT

### A NEW SINGLE TRANSISTOR UNITY POWER FACTOR RECTIFIER

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This thesis analyzes unity power factor rectifiers since this type of rectifiers use energy as efficient as possible.

Throughout the thesis, some unity power factor rectifier topologies are investigated and some of them selected to investigate in detail. Afterwards, a new single transistor unity power factor rectifier topology is proposed, simulated, implemented and compared with one of the selected unity power factor rectifier topology on the basis of efficiency, total harmonic distortion, input current ripple and output voltage ripple.



**Keywords:** rectifier, unity power factor, single transistor unity power factor rectifier

# ÖZ

## YENİ TEK TRANSİSTÖRLÜ BİRİMSEL GÜÇ FAKTÖRLÜ DOĞRULTMAÇ

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Bu tez birimsel güç faktörlü doğrultmaçları, bu tip doğrultmaçlar elektriksel enerjiyi oldukça efektif kullandıkları için incelemektedir.

Tez boyunca bazı birimsel güç faktörlü doğrultmaçlar incelenmiştir ve bunlardan bazıları daha detaylı incelenmek için seçilmiştir. Daha sonra yeni bir birimsel güç faktörlü doğrultmaç devresi önerilmiştir, simüle edilmiştir, gerçekleştirilmiştir ve daha önce seçilen bir birimsel güç faktörlü doğrultmaç devresi ile verimlilik, toplam harmonik bozulma, giriş akımı dalgalanması ve çıkış voltajı dalgalanması baz alınarak kıyaslanmıştır.

**Anahtar kelimeler :** doğrultmaç, birimsel güç faktörü , tek transistörlü birimsel güç faktörlü doğrultmaç

To My Parents

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# CHAPTER I

# INTRODUCTION

## 1.1 Introduction

Electrical power consumers such as motor drives, controlled or uncontrolled rectifiers are major pollutant of the ac power distribution network. As the number of devices used in the ac distribution network increase, pollution of the ac power distribution increases due to their non-linear electrical characteristics. Detrimental effects of the distortion in ac power distribution network is known. In addition to the pollution on the distribution network, usage of electrical energy as efficiently as possible is another research area in power electronics. To decrease pollution in ac power distribution network and use electrical energy as efficient as possible, power factor correction techniques are often used.

The objective of the use of power factor correction circuits is to make input voltage and input current of a rectifier or a power consuming electrical device in phase so that the power factor of the device as seen by the ac power distribution network is unity or close to unity. These type of rectifiers are called unity power factor rectifiers.

The basic classification of the unity power factor rectifiers in this work is single phase or three phase unity power factor rectifiers on the basis of whether the rectifier is supplied from three phase or single phase mains supply. According to the relative magnitude of rectifier's input voltage and output voltage , there is the classification of buck, boost and buck-boost type of rectifier. Unity power factor

rectifiers can also be classified as those using single switching transistor or more than one switching transistor.

The basic control modes of unity power factor rectifiers are current mode control and voltage mode control. With respect to the operation mode of the power stage, unity power rectifier (UPF rectifier) may be divided in to three categories: Discontinuous Conduction Mode (DCM), Critical Conduction Mode (CrCM), and Continuous Conduction Mode (CCM). CCM mode unity power factor rectifiers are preferred due to their low conducted noise, low conduction losses in the semiconductor switches and inductors, and low inductor core losses at high power applications. Peak current control, average current control, hysteresis control are generally used to control CCM operated rectifiers while the UPF rectifier used borderline control operates at the boundary between CCM and DCM.

The aim of the thesis is to investigate unity power factor rectifiers and looking for a new unity power factor rectifier topology with possible performance improvement. The application area is a device supplying 3 kW power to the load, from a dc bus of 400 and 550 volt. The unity power factor rectifier's output voltage is desired to be constant. For this purpose, first the literature is studied and some of the existing topologies are studied.

## 1.2 Outline

In chapter 2, unity power factor rectifiers are categorized as single phase and three phase unity power factor rectifiers. 6 UPF rectifier topologies are selected and investigated in detail.

Chapter 3 is assigned to calculations of the ratings of main semiconductors in the topologies on the basis of given specifications. Then, they are compared with each other and the findings are summarized in a table. One of them is selected for further study.

In chapter 4, a new unity power factor rectifier topology is developed and its working principle is explained. Analytical expressions for the new topology is given also in this chapter, and its performance is compared with the topology selected in

chapter 3.

Control techniques for power factor correction converters are given in chapter 5. The control techniques are explained briefly in this chapter.

Chapter 6 is assigned to simulations of the selected unity power factor rectifier in chapter 3 and the new single switching transistor unity power factor rectifier topology. These rectifiers' simulation results are given in this chapter.

In chapter 7, the proposed new single switching transistor unity power factor rectifier and the rectifier selected in chapter 3 are implemented on a single printed circuit board (PCB), and the proposed rectifier's performance is measured in a laboratory by using 1 kW and 2 kW purely resistive loads. The proposed rectifier is simulated in nearly same condition with the implemented rectifier. After that, the simulation results and the measured results are compared in this chapter.

Chapter 8 is conclusion chapter and it summarizes all of the thesis briefly**.**

# CHAPTER II

# UNITY POWER FACTOR RECTIFIERS

## 2.1 Introduction

There are lots of study , papers and documents upon unity power factor rectifiers. To investigate UPF (Unity Power Factor) rectifiers, some documents are read and the topologies in this documents are classified in this chapter. Some of them are selected to investigate in detail.

Unity power factor rectifiers can be classified as single phase unity power factor rectifiers and three phase unity power factor rectifiers considering mains supply type; buck, boost, and buck-boost type unity power factor rectifiers according to the rectifier's relative input and output voltage magnitudes; and also UPF rectifiers used single switching power transistor or multi switching power transistor. There are so many papers about UPF rectifiers. 32 papers were investigated to find cheap and best solution. Reference 2, 18, 26 express single phase single power switch boost type rectifier and reference 23 express single phase single power switch buck type rectifier. In reference 1, 3, 12, 14, 19, 20, 22, 29, 30 single phase boost type, in reference 7, 27 single phase buck type and in reference 25, 31, 32 single phase buck-boost type rectifiers are investigated. These rectifiers have switching power transistors more than one. Reference 6 explain three phase single switch power transistor boost type rectifier, but reference 4 buck type rectifier. Topologies in reference 7, 8, 9, 10, 11, 13, 15, 17, 21 are three phase boost type ones. Rectifiers in reference 16, 24, 28 are three phase buck type UPF rectifiers, and these use more

than one switching power transistor as well as ones in reference 5, 8, 9, 10, 11, 13, 15, 17, 21. Among these 32 papers, reference 1-6 are selected. The selected papers and the rectifier topologies in these papers are summarized in the following sections in this chapter. The most suitable and cheapest rectifier is tried to be picked out, and calculations of the rectifiers' main electrical component ratings are given in chapter 3.

## 2.2 Single Phase Unity Power Factor Rectifiers

In this section, the selected papers in reference [1], [2], [3] are summarized and the rectifier topologies, whose mains supply is single phase supplies in these papers are investigated. The rectifier topologies are a single phase half-bridge boost topology, well known front-end rectifier followed by a boost converter and a low conduction loss AC/DC UPF rectifier topologies.

### 2.2.1 Single Phase Half-Bridge Boost Topology

This topology is boost type rectifier had a half controlled full bridge configuration except the lack of two diodes reduced the conduction losses and its working and control principles are given in this section [1].

In this topology, at any time there is only one semiconductor on-state voltage drop. Hence conduction loss in this rectifier topology is very low, so it is expected that the rectifier operates at high operating efficiencies.

For proper boost operation, the rectifier's output voltage will be at least twice the value of the peak input voltage. For example, when its mains supply's voltage is 230 V rms, the rectifier's output voltage will have to be greater than 760 V. This means that high-voltage rated semiconductors and passive components are needed in this topology due to the high voltage at the output side of the rectifier. However, when its mains supply's voltage is e.g. 130 Vrms, the rectifier's output voltage will

have to be greater than only 370V. This topology is good option for mains supply had nominal 110 V rms.

Figure 2.1 shows the rectifier topology. It is essential that voltage across the capacitor C1 and C2 greater than the rectifier's instantaneous input voltage for the control action to be effective throughout the line cycle. In order to make its input current and input voltage in phase, fixed-band hysteresis current control technique can be used.

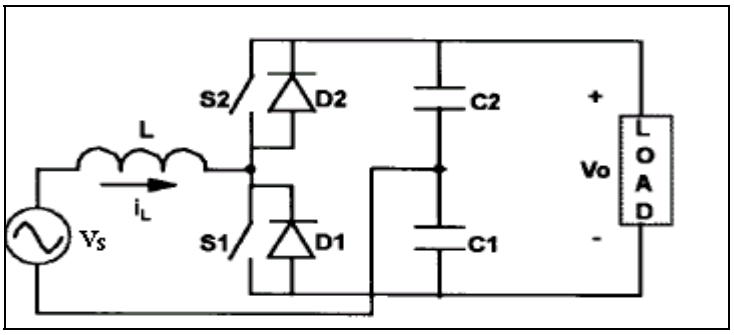
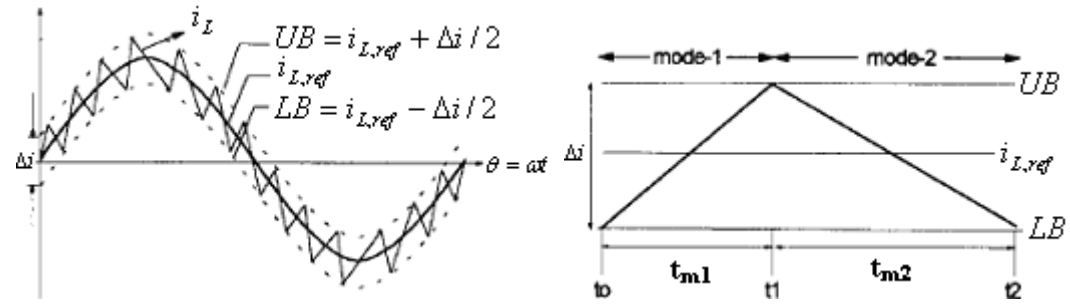



**Figure 2.1** Half-bridge boost PFC circuit.

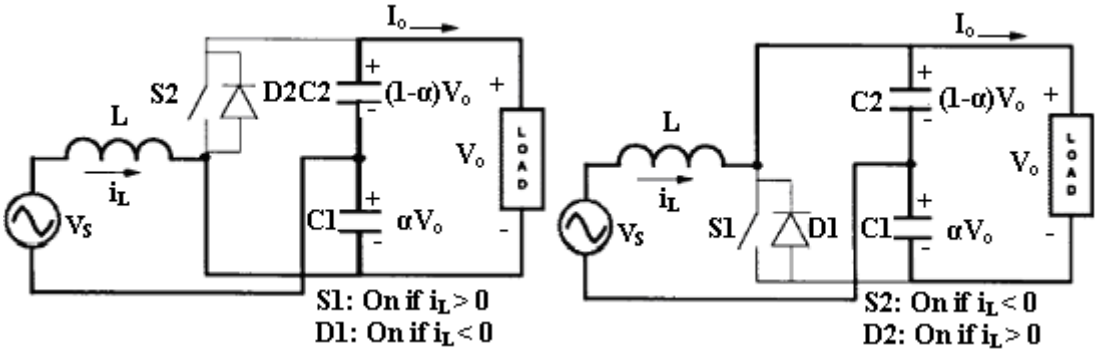
In the fixed-band hysteresis current control technique, by appropriately switching the transistors S1 and S2, the input current $i_L$ is tried to be kept in a $\Delta i$ current band about the current reference $i_{L,ref}$ . figure 2.3 (a) and (b) show the two modes of the circuit operation, named mode 1 and mode 2. In mode 1, at the time the inductor current hits the lower bound (LB) at time $t_o$, the switching transistor S1 is turned on, and whenever $i_L$ greater than zero S1 conducts, else D1 conducts. The voltage across the output capacitor C1 is greater than the supply voltage peak either S1 or D1 conducts, so the operation is boost operation, and the inductor current slope will be positive. In mode 2, the inductor current hits the upper bound (UB) at time $t_1$, the switching transistor S2 is turned on, and depending on the $i_L$ polarity, S2 or the diode D2 conducts. Also, the voltage across the output capacitor, C2 is greater than the mains supply's voltage peak in mode 2. However, the inductor current slope will

be negative in this mode. At time $t_2$, the inductor current hits the lower bound. In this way, one switching cycle is completed. The switching frequency is much more higher than the mains supply frequency, so the inductor current tracks the reference current $i_{L,ref}$ easily.




**(a)** **(b)**

**Figure 2.2** Current waveforms in HCC technique, (a) Over one line cycle, (b) Over one switching cycle.




**(a)** **(b)**

**Figure 2.3** The two modes of operation of the half-bridge circuit, (a) Mode 1: positive inductor-current-slope mode, (b) Mode 2: negative inductor-current-slope mode.

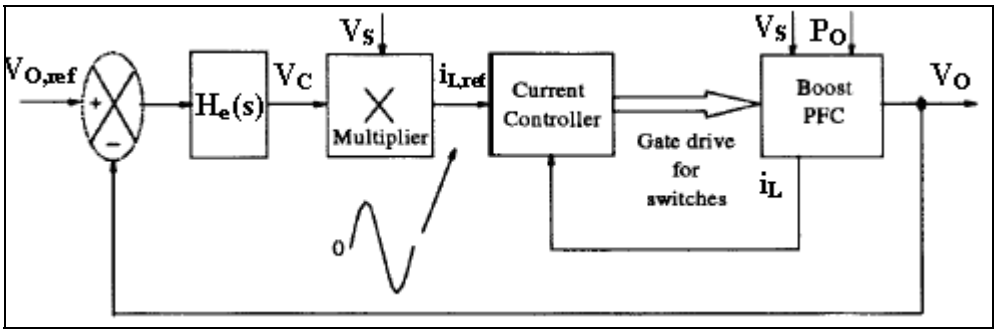



**Figure 2.4** Block schematic representation of a typical closed-loop system for PFC.

The rectifier's output voltage is the sum of the voltages on the capacitor C1 and C2, so the rectifier's output voltage must be greater than twice its input peak voltage. In order to regulate the rectifier's output voltage ($V_o$) to a desired level, closed loop control system is applied to the rectifier and it is shown in figure 2.4.

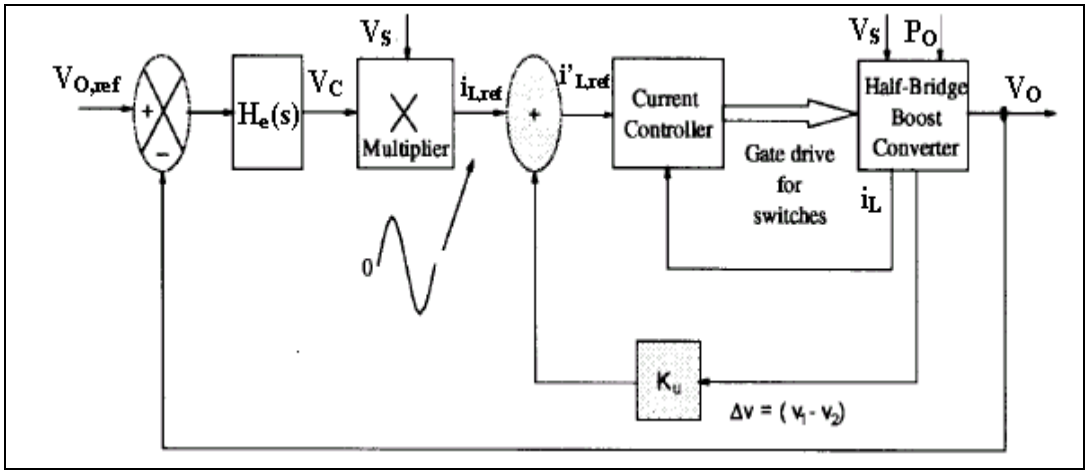



**Figure 2.5** Closed-loop control system with imbalance control.

Main drawback of the rectifier topology is imbalance of the capacitor voltages. However, changing the closed loop control system as in figure 2.5 can eliminate this imbalance. Error voltage, ΔV is introduced due to voltage difference over the

capacitors C1 and C2. The voltage difference over the capacitors should be eliminated. Feeding ΔV through gain block ($K_u$) and adding its output $i_{L,ref}(t)$, new reference current $i'_{L,ref}$ is obtained. In this way, voltage difference over the output capacitors are forced to be zero.

$$i'_{L,ref} = i_{L,ref} + K_u \Delta V \tag{2.1}$$

The new block schematic is shown in figure 2.5 and input current tracks $i'_{L,ref}(t)$ instead of $i_{L,ref}(t)$ when the new closed-loop control system is used.

### 2.2.2 Front-End Rectifier Followed By A Boost Converter

Front-end rectifier followed by a boost converter is a well-known unity power factor rectifier. The rectifier topology and its working principle are explained briefly in this section. Average current control technique expressed in detail in chapter 5 is used as its control technique here [2].

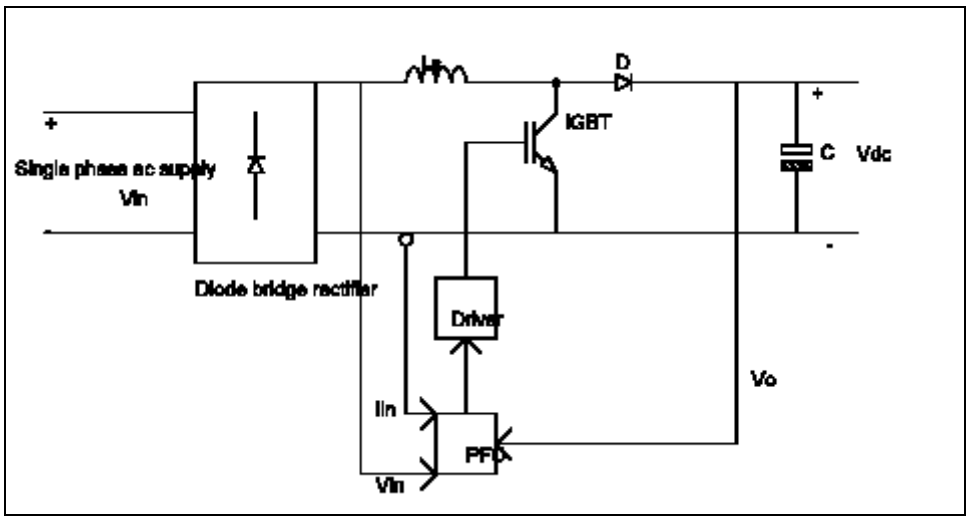



**Figure 2.6** Front-end rectifier followed by a boost converter.

In figure 2.6, the rectifier topology with active power factor correction is shown. Sinusoidal input voltage is converted to DC voltage with ripple via the diode bridge rectifier. Boost inductor, Ls begins to store energy when the IGBT is on. In this time, the output capacitor C supplies necessary voltage and current to the load. Stored energy in the boost inductor and the energy from the mains supply is given to the load and the output capacitor when IGBT is off. A power factor corrector integrated circuit (PFC IC) such as UC3854 measures the output voltage, rectified input current, it processes these signals, gives PWM signal with correct duty cycle to a power semiconductor switch such as an IGBT's gate to achieve sinusoidal input current in phase with the input voltage. In this way, unity power factor at the input side, regulated and correct output voltage at the output side is achieved. In order to turn on and off the IGBT properly, an IGBT driver externally can be used for giving appropriate voltage to the IGBT's gate while some PFC ICs such as UC3854 has an IGBT driver internally.

The power factor corrector integrated circuit (PFC IC) in figure 2.6 is an IC such as UC3854 whose datasheet is given in Appendix B. It operates the rectifier in continuous conduction mode and uses the average current control technique. In continuous conduction mode, the rectifier's input current follows the input voltage waveform, so the input voltage and input current are nearly in phase. This means that nearly unity power factor is achieved at the input side of the rectifier.

The IGBT in figure 2.6 is switched in fixed frequency but the duty cyle of the signal is varying due to the nature of average current control technique.

Amount of high frequency ripple current in the input side of the rectifier is determined by the value of the boost inductor, Ls for the continuous conduction mode of the operation. The ripple current, $\Delta I$ must not exceed the twice the input peak current value to become inductor current continuous.

Increasing the value of the boost inductor, ripple current can be made arbitrarily small. As the ripple current on the input current is low, injected high frequency noise to the supply line becomes low. The boost inductor's value can be calculated using the equation 2.2. In this equation, $V_{in(min)}$ is the minimum input peak voltage. D stands for duty cyle of the PWM signal given to the switching transistor's gate. The input sine wave peak current, $I_{peak}$ can be calculated by using the equation 2.3.

$$L = V_{in(\min)} D / (f_s \Delta I) \tag{2.2}$$

, where $D = (V_o - V_{in(\min)}) / V_o$ and $V_{in(\min)} = \sqrt{2} V_{in(rms)\min}$.

$$I_{peak} = \sqrt{2} I_{in(rms)\max} + \Delta I / 2 \tag{2.3}$$

, where $I_{in(rms)\max} = P_{in(\max)} / V_{in(rms)\min}$.

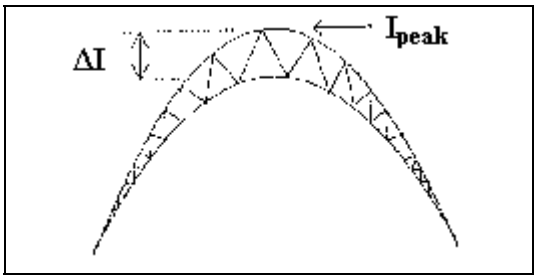



**Figure 2.7** Inductor current waveform.

Current variations in $i_L$ in continuous conduction mode for the average current control technique is shown in figure 2.7. When switching transistor is on, boost inductor's current ramps upwards from its initial value. When switching transistor is off, inductor current, $i_L$ ramps down and stored energy in the inductor is given to the load and the output capacitor.

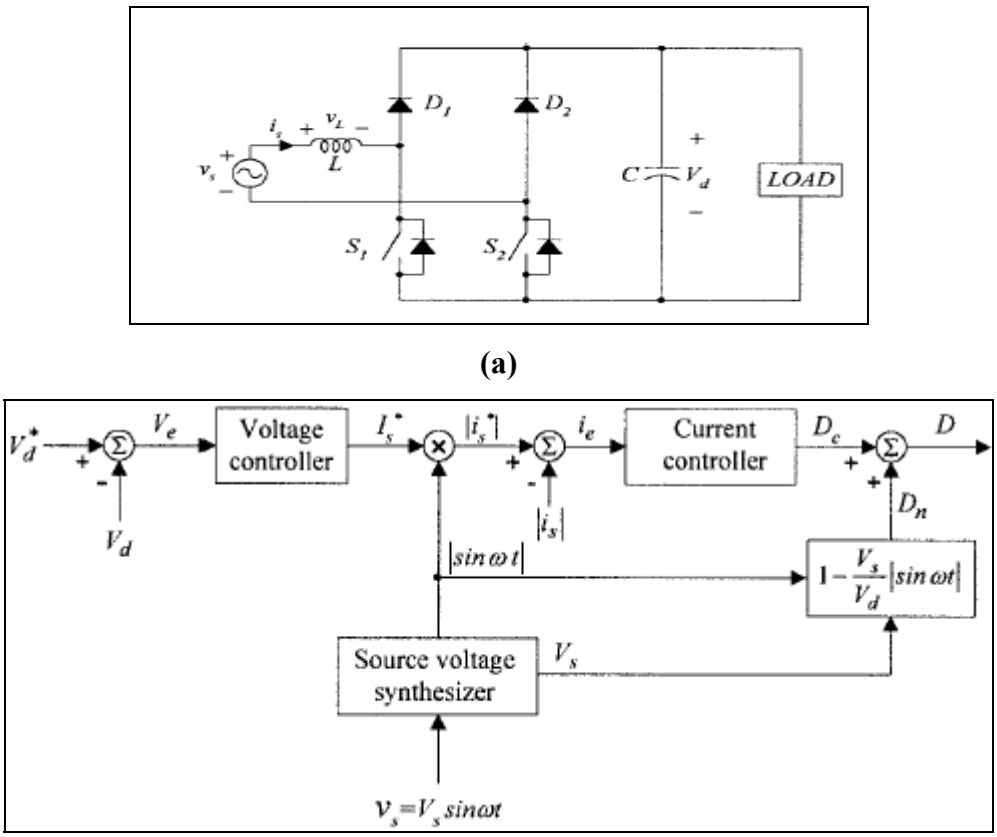
The output capacitance can be calculated by using equation 2.4. Derivation of the equation is based on the energy transfer capability of the capacitor from $V_o$ to $V_{min.}$

$$C_o = 2P_{out} \Delta t / (V_o^2 - V_{o\min}^2) \tag{2.4}$$

As shown from the equation 2.4, the rectifier's output voltage ripple is decreased as the output capacitor's value is increased. Also, larger value of the output capacitor means longer hold-up time (Δt). When hold-up time is high, the designed rectifier can tolerate supply interruptions with short durations at the expense of bulky and costly capacitor banks.

### 2.2.3 Low Conduction Loss AC/DC UPF Rectifier

A novel unity-power-factor controller for single-phase PWM rectifier is shown in figure 2.8. This rectifier has controllable DC link voltage, high efficiency, high power factor, and simple power circuits. Using the "feedback linearization concept", the current controller to obtain sinusoidal input current in phase with input voltage of the rectifier is derived. Two active switches with reverse recovery diodes and two diodes are used for ac-to-dc voltage conversion. The rectifier topology, its working principle and controller are given in reference [3] and they are summarized in this section.




**(a)**

**(b)**

**Figure 2.8** Single phase, low conduction loss AC/DC UPF rectifier with input power factor correction (a) Power circuit (b) its controller block diagram.

In this topology, boost diode in figure 2.6 is eliminated to avoid the conduction loss of the diode and boost inductor on DC side of the rectifier in figure 2.6 is located to the AC side of the rectifier to reduce the EMI (Electro Magnetic Interference). This rectifier has a simple power circuit compared with the one in figure 2.6. However, this topology requires more complicated control circuit than the one in figure 2.6.

The converter in figure 2.8(a) is controlled by turning on and off the switching transistor simultaneously. There is an assumption that current of the inductor in figure 2.8(a) is continuous. When the switching transistors are turned on simultaneously, the inductor current increases through one of the switches and the other antiparallel diode. In this way, the inductor stores magnetic energy. Diodes, D1 and D2 prevent electrical energy stored in the output capacitor to flow to the AC side of the rectifier since the diodes are reverse biased, and the output capacitor, C provides the load current when the switching transistors are turned on simultaneously. Then,

$$V_s - L\frac{di_s}{dt} = 0 \tag{2.5}$$

, where $i_s$ and $V_s$ are the source current and voltage respectively. L is the inductance of the inductor located on the AC side of the rectifier. When the switching transistors are turned off simultaneously, magnetic energy stored in the inductor and electrical energy from the mains supply given to the load and output capacitor through one diode, D1 or D2 and one parallel diode of the two switching transistors, depending on the direction of input current, $i_s$. Then,

$$V_s - L\frac{di_s}{dt} - V_d \operatorname{sgn}(i_s) = 0 \tag{2.6}$$

In this equation, $V_d$ is the converter's output voltage, and $\operatorname{sgn}(i_s)$ denotes the sign of the rectifier's input current. Since it is a unity power factor rectifier, $\operatorname{sgn}(V_s)$ is equal to $\operatorname{sgn}(i_s)$. Depending on the duty ratio, D of the PWM signal given the switching transistors' base and direction of the current, average inductor voltage over one switching period, Ts gives the following source current variation, $\Delta i_s$:

$$V_s D + \left[V_s - V_d \operatorname{sgn}(i_s)\right](1-D) = L\frac{\Delta i_s}{T_s} \tag{2.7}$$

Hence, the duty ratio, D is equal to:

$$D = D_n + D_c \tag{2.8}$$

, where $D_n = 1 - \frac{V_s|\sin wt|}{V_d}$, $D_c = \frac{L\Delta|i_s|}{V_d T_s}$. In equation 2.8, w and $V_s$ are angular frequency and its maximum input voltage respectively. The proportional and integral (PI) current controller can be used so that the source current tracks the current command, and duty cyle. PI is expressed by equation 2.9.

$$D_c = k_{pc} i_e + k_{ic} \int i_e dt \tag{2.9}$$

In this equation, $k_{ic}$ and $k_{pc}$ are the integral and proportional gains respectively. The current error, $i_e$ is given in the equation 2.10.

$$i_e = |i_s^*| - |i_s| \tag{2.10}$$

The rectifier's controller block diagram is given in figure 2.8(b). The duty cycle, $D_c$ is necessary to make its input current in phase with the input voltage. The rectifier is originally a nonlinear dynamic system; but with the addition of the nominal duty cycle, $D_n$ to the rectifier, the relation between the input $D_c$ and output $|i_s|$ becomes a first-order linear dynamic system. Thus, the addition of the nominal duty cycle to the duty cycle, $D_c$ relaxes the burden of PI controller and this improves the input current waveform and makes controllability of the rectifier easier.

## 2.3 Three Phase Unity Power Factor Rectifiers

In this section, the rectifiers, which have three phase mains supply, namely, single transistor three phase multiresonant high power factor (HPF) rectifier, pulse voltage source rectifier with PWM-SHE (Pulse Width Modulation- Specific Harmonic Elimination) and single controlled switch three phase rectifier with unity power factor and sinusoidal input current are expressed in detail in reference [4], [5], [6]. The papers in these references are summarized and the rectifier topologies are expressed briefly here.

### 2.3.1 Single Transistor Three-Phase Multiresonant ZCS HPF Rectifier

A single transistor three-phase multiresonant ZCS high power factor rectifier topology and its working principle are given in reference [4]. These are summarized in this section.

The unity power factor rectifier is a new family of a three-phase single switch high power factor (HPF) multiresonant buck type rectifier. It has continuous input and output current. The three phase multiresonant ZCS (Zero Current Switching) cell and resonant capacitor, $C_{r1}$'s voltage shapes are shown in figure 2.9. The transistor operates with ZCS and the diodes operate with ZVS (Zero Voltage Switching) by using a multiresonant scheme. These single transistor multiresonant rectifiers draw higher quality of input current waveform at nearly unity power factor, have lower stresses than the quasi-resonant rectifiers and PWM boost type rectifiers, which operate in discontinuous conduction mode (DCM), since the portions of periods, B and C in a switching interval shown in figure 2.9(c) are shorter than those of other type of topologies. More linear input characteristic is produced due to the dominance of the period, A and the voltage, $V_{Cr1}$ is proportional to the input current in this time interval. Since this rectifier is buck type rectifier, the rectifier's output voltage lower than the rectifier's input peak voltage. This type of rectifiers has low stresses on the semiconductor devices and wide load range.

$L_a$, $L_b$, $L_c$ and $L_f$ are the filter inductors had small switching-frequency current ripples. The resonant capacitors, $C_{r1}$, $C_{r2}$, $C_{r3}$'s average voltage during a switching period are equal to the input voltages, $\Phi_a$, $\Phi_b$ and $\Phi_c$ respectively at steady state. Furthermore, their peak voltages and the input currents, $i_a$, $i_b$, $i_c$ are proportional to each other. Since the switching frequency is much higher than input line frequency, the input current waveshape follows the input voltage waveshape easily. High power factor and low harmonic input current content are results of this phenomenon.

It is sufficient to consider a $30^0$ interval of the AC input line waveform by assuming the three phase line voltage is well balanced and symetric to make analysis of the three phase multiresonant buck type rectifier shown in figure 2.9(a). Also, it is assumed that the switching frequency of the rectifier is much higher than the input

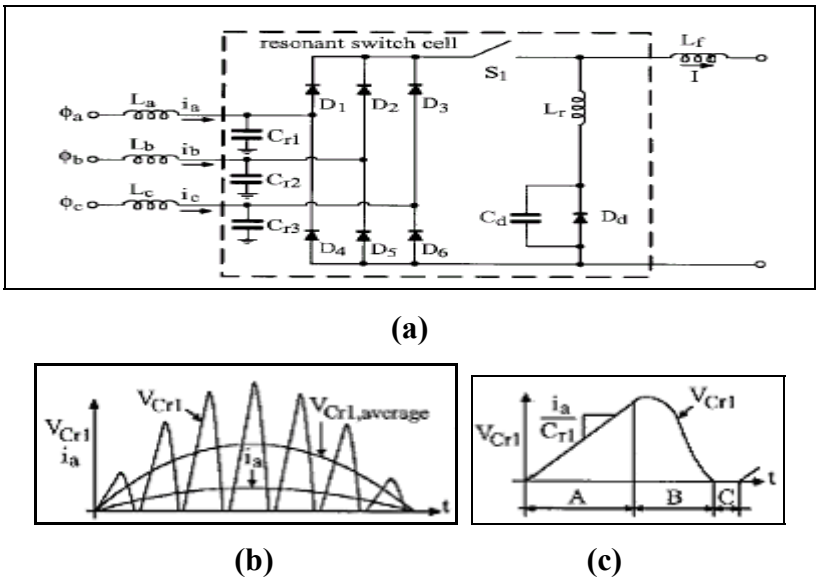



**Figure 2.9** (a) Three-phase multiresonant ZCS cell. (b) The input-side resonant-tank capacitor-voltage waveform together with the input-current waveform. (c) The enlarged waveform of $V_{Cr1}$ during one switching period.

line frequency. Analysis of rectifier in $30^0$ interval, where $i_a>0>i_c>i_b$ , is described here[4]:

1) **Interval 1:to ≤ t ≤ t1**, All switches are off except $D_d$: In this interval, each tank capacitor, $C_{r1}$ –$C_{r3}$ charges up linearly at a rate proportional to its respective line current. This will continue until switch $S_1$ is turned on. During this interval, resonant-tank inductor, $L_r$ supplies the output load current. When switch $S_1$ turns on, the input line-to-line voltage, $V_{ab}$ is maximum and this forces $D_1$ and $D_5$ to conduct.
2) **Interval 2: t1 ≤ t ≤ t2,** $D_1$, $D_5$, $D_d$, and $S_1$ are on: In this interval, the capacitor voltage, $V_{Cr3}$ continues to increase while the other two capacitor voltages ring with resonant-tank inductor, $L_r$ until the tank inductor current increases to zero from the negative output current. Then, the diode, $D_d$ turns off, initiating the next interval.
3) **Interval 3: t2 ≤ t ≤ t3,** $D_1$, $D_5$, and $S_1$ are on: In this interval, the capacitor voltage, $V_{Cr3}$ continues to increase, while the other two capacitor voltages ring with resonant-tank inductor, $L_r$. This will continue until $V_{Cr3}$ becomes equal to

$V_{Cr2}$. Then, diode, $D_6$ also conducts. Depending on the magnitudes of $i_b$ and $i_c$, the order of interval 2 and 3 may be reversed. Interval 3 occurs before interval 2 when currents $i_b$ and $i_c$ are similar in magnitude.

4) **Interval 4: $t3 \leq t \leq t4$,** $D_1$, $D_5$, $D_6$ and $S_1$ are on: In this interval, the resonant-tank capacitors, $C_{r1}$– $C_{r3}$, parallel capacitor, $C_d$ and resonant-tank inductor, $L_r$ form a resonant-tank circuit. This interval ends when the resonant-tank capacitor's voltages, $V_{Cr1} - V_{Cr3}$ discharge to zero.
5) **Interval 5: $t4 \leq t \leq t5$,** All switches are on except $D_d$: In this interval, the parallel capacitor, $C_d$ and resonant-tank inductor, $L_r$ ring until the tank inductor current decreases to the negative load current. At this point, the input bridge rectifiers become reverse biased. Hence, the switch current becomes zero.
6) **Interval 6: $t5 \leq t \leq t6$**, All switches are off: Interval 6 is actually a subset of Interval 1 as shown in the waveforms of figure 2.10. The capacitor, $C_d$'s voltage linearly decreases until it reaches zero voltage and the diode, $D_d$ turns on. During the input diode bridge are reverse biased, the complete load current is supplied by parallel capacitor $C_d$. Therefore, the switch, $S_1$ can be turned off with ZCS as shown in figure 2.10.

The system behaviour in the entire line period can be investigated by the extension of the interval [0, π/6] due to the three-phase input voltages' symmetry. One operating point at the time π /2 is chosen to simplify the three phase input and single ended output circuit shown in figure 2.10. At the time π /2, the phase voltage, $V_{an}$ has its peak value. The other phase voltages, $V_{bn}$, $V_{cn}$ are equal in magnitude to one half of $V_{an}$ and both are negative. At this condition, capacitors $C_{r2}$ and $C_{r3}$ shown in figure 2.10 are charged and discharged exactly in the same manner. Thus, the capacitors $C_{r2}$ and $C_{r3}$ are considered as parallel connected capacitors. At this operating point, the phase current, $i_{an}$ has its peak value. Also, $i_{bn}$ and $i_{cn}$ are both one half of the negative phase current, $i_{an}$. Hence, current source $I_g$ as shown in figure 2.11 can be placed instead of the input voltage sources and the input filter inductors. $I_g$ in figure 2.11 is the peak phase current, $i_{an\text{-}peak}$. The effective capacitor, $C_x$ shown in figure 2.11 can be put instead of the input side resonant capacitors, $C_{r1} - C_{r3}$. $C_x$ is equal to the series connection of $C_{r1}$ and parallel-connected $C_{r2}$ and $C_{r3}$. The three phase input diode bridge in figure 2.10 is represented by the diodes $D_1$ and $D_2$ in figure 2.11. The current source, I in figure 2.11 is placed instead of the output filter

inductor in figure 2.10. Simplified single input and single ended circuit diagram is obtained and shown in figure 2.11.

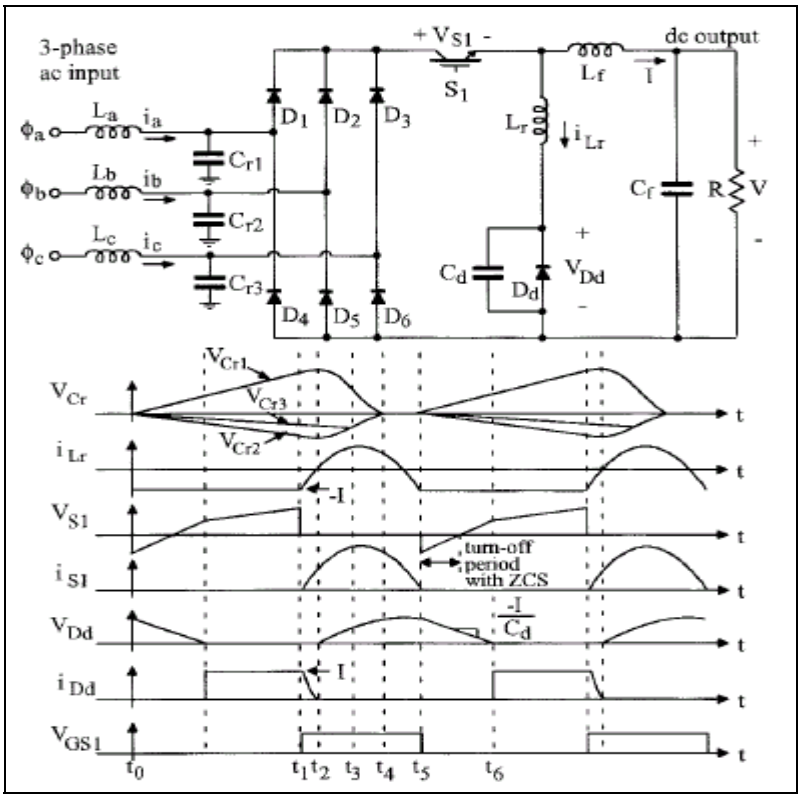



**Figure 2.10** Basic single transistor three-phase multiresonant ZCS HPF rectifier circuit and its ideal waveforms.

This simplified single input, single ended output model and the relations between the actual three phase input circuit are given approximately as follows:

1) $C_x = C_r \times 2/3$, where input-resonant capacitors $C_{r1} - C_{r3}$ have the same values and are represented as $C_r$.
2) $I_g$ = peak phase current, $i_{an\text{-}peak}$.
3) $V_g$ = 3/2 times the peak-phase voltage, $V_{an\text{-}peak}$, where $V_g$ is also the same as the average voltage of $V_{Cx}$ during one switching period.
4) Three-phase input power $P_{in} = V_g \times I_g = 3/2 \times V_{an\text{-}peak} \times i_{an\text{-}peak}$.

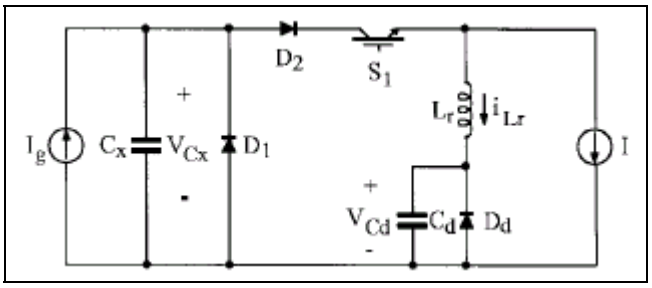



**Figure 2.11** The simplified single-input and single-output model of the single-transistor three-phase multiresonant ZCS HPF rectifier.

The converter equations are normalized with respect to the DC output voltage and they are given in the following equations:

Base voltage $= V$ (2.11)

Base current, $I_o = V / R_o$ (2.12)

Base impedance, $R_o = \sqrt{\frac{L_r}{C_x}}$ (2.13)

Base frequency, $f_o = \frac{1}{2\Pi\sqrt{L_r C_x}}$ (2.14)

V in equation 2.11 and 2.12 is the rectifier's output voltage.

The normalized values of the input and output quantities can be given as $M_g = V_g/V$, $J_g = I_g R_o/V$, $J = IR_o/V = M_g J_g$, $\alpha = 2\pi f_o(t_1-t_0)$, $\beta = 2\pi f_o(t_5-t_1)$, and $\gamma = (\alpha+\beta)/2$ if it is assumed that the rectifier is an ideal loss-free system. The switch, $S_1$'s off time is $t_1-t_0$ and its on time is $t_5-t_1$ as shown in figure 2.10.

### 2.3.2 12-Pulse Voltage Source Rectifier With PWM-SHE

12-pulse voltage source rectifier with PWM-SHE is explained in detail in reference [5]. It is summarized briefly in this section.

AC drive system used with medium to high voltage systems is shown in

figure 2.12. Two identical voltage source rectifiers connected in series are used as active front-end rectifier. The rectifier shown in figure 2.12 is a 12-pulse rectifier and its lowest order input current harmonics are $11^{th}$ and $13^{th}$ harmonics with a balanced input voltage source. The input dual transformer in the rectifier eliminates the input current harmonics in the order of $6k \pm 1$, where $k = 1,3,5,...(2n-1)$. Hence, the input dual transformer eliminates $5^{th}$, $7^{th}$, $17^{th}$ and $19^{th}$ harmonics. To eliminate all the harmonics lower than $23^{rd}$, only $11^{th}$ and $13^{th}$ harmonics are required to be eliminated by the PWM-SHE (PWM-Specific Harmonic Elimination) method. Hence, a quite low switching frequency can be obtained and it is an advantage. The minimum switching frequency can be 350 Hz for this topology, but 750 Hz for the single converter to eliminate all the harmonics with the order lower than $23^{rd}$ is necessary.

Dynamic and steady state voltage-sharing problem seen for the series devices in a single bridge topology are avoided in this topology. This high-power medium-voltage PWM AC/DC voltage source rectifier has the ability to deliver nearly sinusoidal current from mains supply at unity power factor while phase controlled high-power medium-voltage rectifiers don't have this ability.

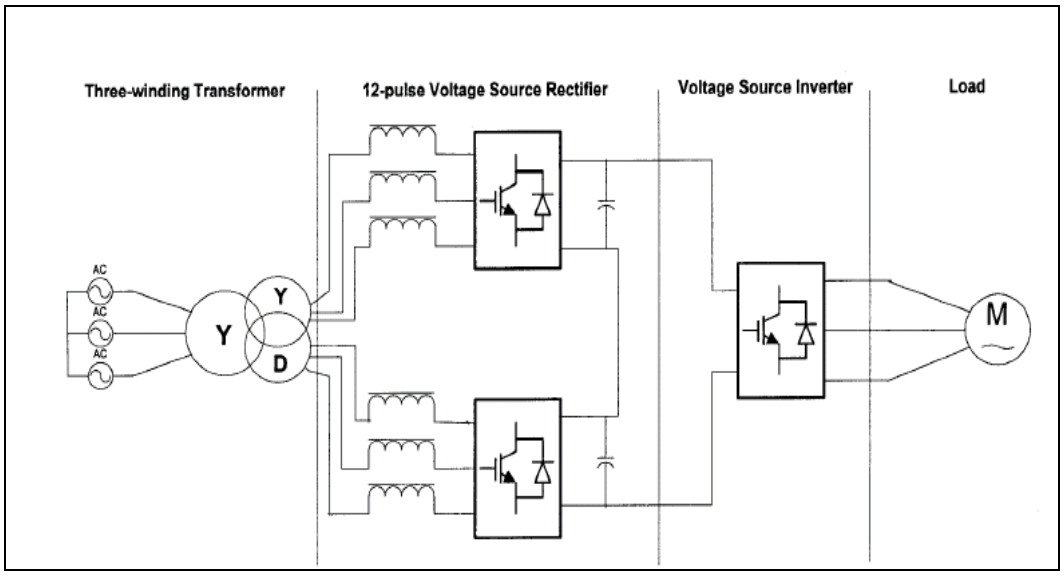



**Figure 2.12** Main circuit of the voltage source converter drive system.

The AC and DC systems are interfaced by the rectifier using bi-directional current and unidirectional voltage blocking switches in figure 2.12. The rectifier exhibits voltage source characteristics at the DC terminal (DC link capacitors) and it exhibits current source characteristics at the AC supply terminal. On the basis of minimum ripple requirement of the DC bus voltage, $V_{dr}$, the DC link capacitor should be chosen. The relationship of switching frequency, $F_s$, DC voltage ripple, $V_{dr}$, input line current, $I_m$, and modulation index, M are given in equation 2.15.

$$C = \frac{I_m}{4F_s V_{dr}}\left[\cos(\frac{\Pi M}{4}) - \cos(\frac{\Pi M}{2})\right] \tag{2.15}$$

In order to maintain nearly unity power factor at its input side, there are various control strategies such as hysteresis current control, phase and amplitude control. However, their performance is not same. One different current control strategy is suitable for PWM-SHE (Pulse Width Modulation-Specific Harmonic Elimination) method and it is applied here. According to this control method, the rectifier's AC input voltage is made equal to the AC line voltage. The resulting power factor is greater than 0.98 with the assumption that the link reactor is less than 0.4 p.u. Figure 2.13 shows the corresponding phasor diagram and $V_{rec}$ is the rectifier input voltage in this figure.

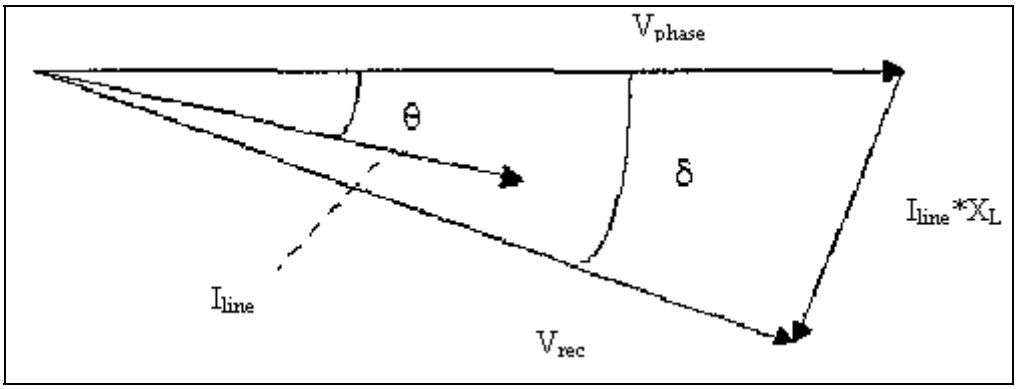



**Figure 2.13** Phasor diagram of front-end voltage source converter.

In order to evaluate the performance of different kinds of PWM patterns, there are various criteria. Pulse width modulation-specific harmonic elimination method has lower total harmonic distortion (THD), harmonic loss factor (HLF), and second order distortion factor (DF2) when it is compared with other control strategies under similar conditions. Hence, the most effective high performance results can be obtained by using pulse width modulation-specific harmonic elimination patterns.

All of angles of pulse width modulation-specific harmonic elimination can be precalculated and stored in memory so that the unexpected narrow switching pulses produced randomly by other online PWM patterns disappear. In order to prevent to destroy the switching devices, too narrow pulses (1-100μs) are avoided to apply the gate of the switching devices since they may violate the restrictions on minimum on time and turn off delay of switching devices.

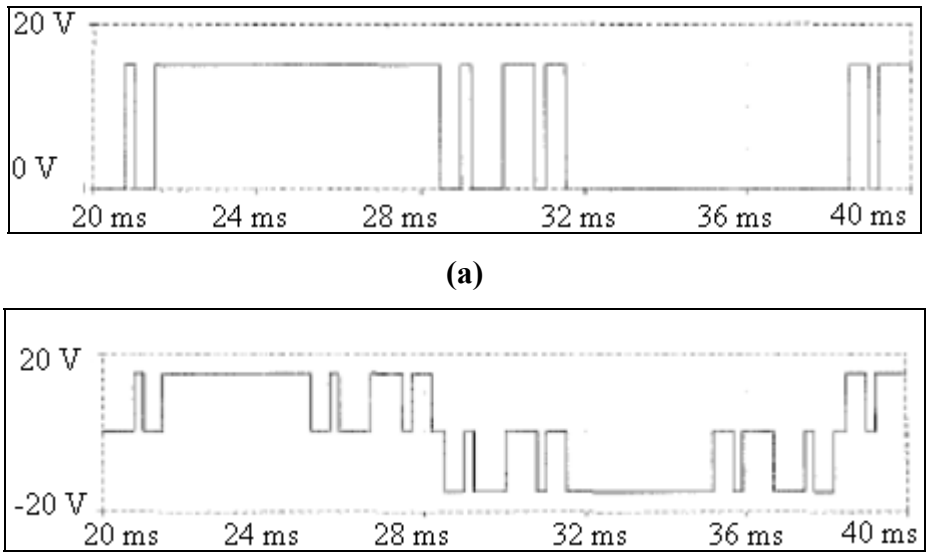



**Figure 2.14** PWM-SHE switching pattern for $11^{th}$ and $13^{th}$ harmonic elimination (modulation index M=0.9). (a) Switch gating signal. (b) Line-to-line voltage.

There are well known advantages of pulse width modulation-specific harmonic elimination (PWM-SHE) patterns. Since over-modulation is possible, high voltage gain can be obtained. The ripple on the DC link current is small due to the high quality output current and voltage, so reduction in the size of the DC link filter components can be achieved. Moreover, elimination of the lower order harmonics prevents harmonic interference such as resonance with external line filtering networks.

The switching pattern, which especially eliminates the $11^{th}$ and $13^{th}$ harmonics, is just common two-level line-to-neutral PWM pattern, and it has quarter and half wave symmetries. Fourier coefficients of the switching pattern are given in equation 2.16 and 2.17.

$$a_n = \frac{4}{n\Pi}\left[-1-2\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k)\right] \tag{2.16}$$

$$b_n = 0 \tag{2.17}$$

The switching pattern can be obtained by solving three nonlinear functions ($a_{11}$= 0, $a_{13}$= 0,and $a_l$ = M), and it is shown in figure 2.14.

### 2.3.3 Single Controlled Switch Three Phase Rectifier With Unity Power Factor and Sinusoidal Input Current

A single controlled switch three phase rectifier with unity power factor and sinusoidal input current and its working principle are expressed in detail in reference [6]. They are summarized in this section.

Single controlled switch three phase rectifier is possible with low harmonic rectification, without active control of the line currents, and without the use of bulky low-frequency passive elements. The three phase rectifier topology, the voltage waveshape of the input capacitor, $C_{sa}$, and the input current, $i_{sa}$ is shown in figure 2.15.

The rectifier has two stages. Three phase diode bridge with the capacitors,

$C_{sa}$, $C_{sb}$, $C_{sc}$ and inductors, $L_{sa}$, $L_{sb}$, $L_{sc}$ connected to there phase mains supply is one of the two stages. The other stage is the active output stage consisting of the boost type single ended converter.

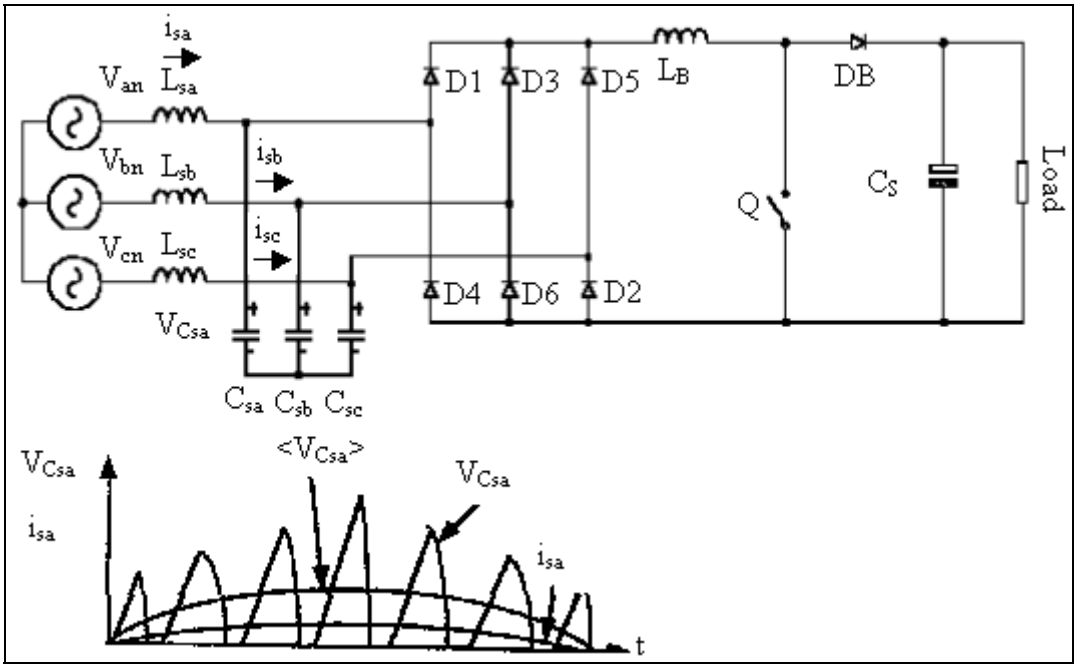



**Figure 2.15** Topology of the converter.

Discontinuous current control technique with variable frequency is employed to the active switching device of the output stage. In this rectifier topology, only one boost inductor, $L_B$ is used. The rectifier has a pulsating input voltage during each switching period. The pulsating input peak voltage, $V_{Csa}$ is proportional to the input line current, $i_{sa}$ and this provides an average of line current nearly sinusoidal and approximately proportional to the phase voltage, $V_{an}$. The input inductors, $L_{sa}$, $L_{sb}$, $L_{sc}$ filter the input line currents, $i_{sa}$, $i_{sb}$ and $i_{sc}$ respectively.

In order to obtain a high quality input current, the input inductors are forced to operate in discontinious current mode in this high frequency converter. The input capacitors $C_{sa}$, $C_{sb}$, and $C_{sc}$, which are chosen to be sufficiently small to operate the

circuit in discontinuous voltage mode are used in the boost rectifier shown in figure 2.15 to obtain low harmonic rectification.

Operation mode of the rectifier includes energy transfer from capacitors $C_{sa}$, $C_{sb}$, and $C_{sc}$ to the inductor $L_B$. Switch Q is turned on and the capacitors are discharged by the resonating switch current to achieve this energy transfer. All bridge diodes are conducting when the capacitors voltages are reduced to zero. The magnetic energy stored in the inductor, $L_B$ is transferred to the load and the output capacitor through the diode, $D_B$ when the switching transistor, Q is turned off. The input capacitors, $C_{sa}$, $C_{sb}$, and $C_{sc}$ are charged linearly by the currents, $i_{sa}$, $i_{sb}$ and $i_{sc}$ respectively when the diode, $D_B$ turns off until the switching transistor Q is turned on again.

The system behaviour with suitable phase shifts for the entire fundamental period can be analysed in a $60^0$ interval. The interval which corresponds to the condition: $V_{sa}>0>V_{sb}>V_{sc}$ is considered here. It is assumed that the mains supply's phase voltages are sinusoidal, balanced, and approximately constant within a pulse period. Operation modes of the rectifier within the $60^0$ interval is as the following:

1. **Mode 1: t0<t<t1, diodes D1, D6 and switch Q are on**. At $t=t_0$, switch Q turns on; during this interval, the capacitor voltage $V_{Csc}$ continues to increase, while the other capacitors, $C_{sa}$, $C_{sb}$ and the inductor, $L_B$ resonate until the capacitor voltage, $V_{Csb}$ reaches to the capacitor voltage, $V_{Csc}$. The diode, D2 then also conducts during the next interval.
2. **Mode 2: t1<t<t2, diodes D1, D2, D6 and switch Q are on**. The three capacitors, C1, C2, C3 and the inductor $L_B$ resonate until all the capacitors are discharged by a pulsed current.
3. **Mode 3: t2<t<t3, all diodes are on, switch Q is off**. This mode starts when the voltages across the capacitors are equal to zero and the switch, Q is then turned off and energy is transferred from the boost inductor to the load through diode $D_B$ . All diodes in this rectifier conduct. This mode ends when the boost-inductor current becomes equal to value of the line current, $i_{sa}$.
4. **Mode 4: t3<t<t4, diodes D1, D6 and $D_B$ are on**. The capacitors, $C_{sa}$, $C_{sb}$ and the inductor, $L_B$ resonate. The capacitor, $C_{sc}$ is charged linearly by its line current. The duration of this mode is negligible. The diodes, D1, D6 and $D_B$ are conducting during this interval. This mode ends when the boost inductor

current becomes zero.

5. **Mode 5: t4<t<t5, all switches are off**. The input capacitors, $C_{sa}$, $C_{sb}$, $C_{sc}$ are charged linearly to their peak values by currents $i_{sa}$, $i_{sb}$ and $i_{sc}$. This mode ends when the switch Q turns on.

# CHAPTER III

# SELECTION OF UPF RECTIFIER TOPOLOGY

## 3.1 Introduction

Some UPF (Unity Power Factor) rectifier topologies were investigated in previous chapter. One of the topologies should be selected to simulate. Cheapest, simplest and best suitable rectifier among the ones investigated in previous chapter is tried to be picked out in this chapter. Transistor ratings, value of inductors and capacitors of the selected rectifier topologies in previous chapter are calculated and number of all critical components are given. At the end of the chapter, these values and ratings are given in a table. The calculations of the unity power factor rectifiers are made on the basis of the following specifications:

- Rectifiers' output power = 3 kW
- Switching frequency, $f_{sw}$ = 20 kHz (it may be different)
- Rectifiers' output voltage = 530 ± 2 % V
- Mains supply's voltage = 220V rms if single phase rectifier
- Mains supply's voltage = 380V (line to line) rms if three phase rectifier
- Mains supply's frequency = 50 Hz
- Input current ripple, $\Delta I$ = 5 % peak to peak current
- Rectifier efficiency, $\eta \geq 95$ % at full load
- Input power factor, pf ≈ 1

The rectifiers' efficiency is equal to or greater than 95 % according to above specifications. Then, their maximum input power is calculated as 3158 VA by using

the equation 3.1. In calculation of the component ratings, the rectifiers' output power is taken as 3158 VA.

$$Efficiency = \frac{Power(output)}{Power(input)} \tag{3.1}$$

Diodes and switching power transistors' current and voltage ratings are taken as two times what is calculated in the following sections to prevent possible failure of the semiconductor devices except in section 3.3.1 since necessary safety margins are taken in the calculations in section 3.3.1.

## 3.2 Calculations Of Single Phase Unity Power Factor Rectifiers

In this section, single phase half-bridge boost rectifier, front-end rectifier followed by a boost converter and low conduction loss AC/DC UPF rectifier's switching transistors' voltage and current ratings are calculated according to the specifications given in section 3.1. Values of power inductors and capacitors used in these rectifiers, which have single phase AC mains supply are also calculated and number of critical components are given.

### 3.2.1 Calculations Of Unity Power Factor Converter Using Half-Bridge Boost Topology

Single phase half-bridge boost topology is investigated before in section 2.2.1. In this section, its switching transistors and their free-wheeling diodes' voltage and current ratings, value of its boost inductor and power capacitors are calculated according to the specifications given in section 3.1. These are listed at the end of this section together with number of the switching transistors and boost inductor and power capacitors.

Using the specifications in section 3.1 and equation 2.3 describing that the boost inductor's peak current is sum of the high frequency ripple current and the sum

of the power frequency line current [2], the rectifier's maximum input rms current, $I_{in(rms)\max}$, its boost inductor's ripple current, $\Delta I$, and peak current, $I_{peak}$ are calculated as 16.887 A, 1.2247 A and 24.494 A respectively.

Since this rectifier topology's output voltage is greater or equal to two times its peak input voltage, modulation index, $M$ is equal or greater to 2 [1]. Modulation index formula is given in equation 3.2.

$$M = \frac{V_o}{V_p} \geq 2 \tag{3.2}$$

, where $V_p = \sqrt{2}V_{in(rms)}$. The voltage, $V_p$ is equal to 311.12 V when the rectifier's input voltage is equal to 220 V rms. The rectifier's output voltage becomes its minimum output voltage when the modulation index is taken as 2. Its minimum output voltage, $V_{omin}$ is calculated as 622.25 V when the voltage, $V_p$ and the modulation index, M are taken as 311.12 V and 2 respectively. Hence, the output voltage specification in section 3.1 can't be achieved in this topology. The rectifier's peak output voltage is sum of its DC output voltage and output voltage ripple. Its peak voltage is found as 634.695 V by taking the output voltage ripple as ± 2 % of the pure DC output voltage. The modulation index is found as 2.04 when the rectifier's output voltage is at its peak by putting the peak output voltage to the equation 3.2 and taking $V_p$ voltage as 311.12 V. This value of modulation index is used in the following calculations in this section.

The maximum switching frequency, $f_{s\max}$ is given in equation 3.3 and its derivation is given in reference 1.

$$f_{s\max} = \frac{V_o}{4L\Delta i} \tag{3.3}$$

The boost inductance in this rectifier topology is calculated as 6.47 mH by putting the values of $\Delta I$ and $V_o$ in to equation 3.3 and taking $f_{s\max}$ as 20 kHz. The minimum switching frequency is given by the equation 3.4 and it occurs when the mains supply's voltage is at its peak value [1].

$$f_{s\min} = 4 f_{s\max}\left(\alpha + \frac{1}{M}\right)\left((1-\alpha) - \frac{1}{M}\right) \tag{3.4}$$

Using the equation 3.4 and taking α (average duty cycle of switching transistor, S2 in figure 2.1) as 0.5, the minimum switching frequency, $f_{s\min}$ is calculated as 776.619

Hz. The output current, $I_o$ given to the rectifier's load is found as nearly 4.73 A by dividing its 3 kW output power to its 634.695 V output voltage. The overall output voltage ripple expression is given by equation 3.5 [1].

$$\delta V_o = \frac{I_o}{2\Pi f_s C}\left[2M(1-2\alpha)\cos\theta - \sin 2\theta\right] \tag{3.5}$$

, where $\alpha \geq \alpha_{\min} = \frac{1}{M}$. $C$, $f_s$, $\alpha$, and $M$ are one of its output capacitances, switching frequency of the switching transistors, average duty cycle of switching transistor, S2 ($(1-\alpha)$ is the average duty cycle of the transistor S1) in figure 2.1, and modulation index respectively. $\theta$ is equal to $wt$ and $w$ is the angular frequency of the rectifier's input voltage. Minimum capacitance value of the rectifier is calculated using the equation 3.5. Minimum capacitance of the capacitor, C1 or C2 in figure 2.1 is calculated as 204 uF by taking $\delta V_{o\max}$, $\theta$, $\alpha$, and $f_s$ as 12.445V (+2 % ripple voltage at the output), $-36.375^0$ (because output voltage ripple has its peak value at $\theta = -36.75^0$), $\alpha_{\min}$ (it is equal to 0.49 at modulation index, $M = 2.04$) and 20 kHz maximum switching frequency.

There are the derivations of the following equations 3.6, 3.7, 3.8, 3.9 in reference [1].

$$I_{s1,avg} = I_o\left(\frac{2(1-\alpha)M}{\Pi} - 0.5\right) \tag{3.6}$$

$$I_{s2,avg} = I_o\left(\frac{2\alpha M}{\Pi} - 0.5\right) \tag{3.7}$$

$$I_{D1,avg} = I_o\left(\frac{2(1-\alpha)M}{\Pi} + 0.5\right) \tag{3.8}$$

$$I_{D2,avg} = I_o\left(\frac{2\alpha M}{\Pi} + 0.5\right) \tag{3.9}$$

$I_{s1,avg}$, $I_{s2,avg}$, $I_{D1,avg}$, $I_{D2,avg}$ are calculated as 0.7075 A, 0.7075 A, 5.43 A, 5.43 A by using the equations 3.6, 3.7, 3.8, 3.9 and taking $\alpha$, $M$, $I_o$ as 0.5 (since average ratings of the diodes and switches are calculated here), 2.04, 4.73 A respectively. Voltage stresses of the switches, S1, S2, the diodes, D1, and D2 in figure 2.1 are same as the rectifier's peak output voltage, which is equal to 634.695 V. The necessary diode, switching transistor, inductor and capacitor ratings, their number, and an expression about the rectifier's control circuit are listed as following:

**Needed:**

1. 2 IGBT (1269 V, 1.414A)
2. 2 reverse recovery diode (1269 V, 10.86 A)
3. 1 inductor (L=6.47 mH)
4. 2 capacitor (Each $C \geq 204uF$)
5. UPF IC or special control circuit to switch the IGBTs.

### 3.2.2 Calculations Of Front-End Rectifier Followed By A Boost Converter

Front-end rectifier followed by a boost converter topology is expressed before in section 2.2.2. In this section, its boost inductance and output capacitance and switching transistor's voltage and current rating are calculated according to the specifications given in section 3.1. They are listed at the end of this section.

Its peak input current and input current ripple are calculated as 24.494 A and 1.2247 A respectively by using the equations 2.2 and 2.3 and the specifications given in section 3.1. Its minimum input peak voltage, $V_{in(min)peak}$ is calculated as 264.46 V since its minimum input rms voltage, $V_{in(min)rms}$ is equal to 187 V rms according to the specifications. Putting the values of the minimum input peak voltage, $V_{in(min)peak}$ and the input current ripple, $\Delta I$ in to equation 2.2 and taking switching frequency as 20 kHz, value of the boost inductor, Ls is calculated as 5.4 mH.

Its output capacitance is calculated as 1124.2 uF by taking hold-up time, $\Delta t$, worst-case output voltage drop, the rectifier's output power as 10 ms, 10 % of its mean output voltage, 3 kW and using the equation 2.4.

The switching transistor's current stress is equal to the rectifier's peak input current, and it is 24.494A. Its voltage stress is same as the rectifier's output voltage. Hence, the transistor's voltage stress is 530 V.

The bridge diodes' voltage stresses in this rectifier is same as its input peak voltage and it is 311 V. These diodes' current stresses are equal to the rectifier input peak current.

The boost diode in the rectifier has same voltage and current stresses as the switching transistor's ones and it should be fast diode. Main components of the

rectifier, value of the output capacitor and boost inductor, the switching transistor and the diodes current and voltage ratings, and which type of IC can control the rectifier are summarized as the following:

**Needed:**

1. Four bridge diode (622 V, 49A)
2. One fast boost diode (1060V, 49A).
3. One IGBT with reverse recovery diode (1060V, 49A)
4. One capacitor (1124.2uF)
5. One inductor (5.4mH)
6. UPF (unity power factor) IC.

### 3.2.3 Calculations Of Low Conduction Loss AC/DC UPF Rectifier

In this section, equations related with the boost inductance and output capacitance in low conduction loss AC/DC UPF rectifier expressed before in section 2.2.3 are derived. The rectifier's boost inductance, output capacitance, power semiconductor diodes and switching transistor's voltage and current ratings are calculated according to the specifications given in section 3.1.

In order to calculate the output capacitance and boost inductance, L in figure 2.8(a), equations related with the inductance and capacitance are derived as the following:

**1st stage:** When switching transistors, S1 and S2 are on:

Using the following inductor voltage equation, and integrating the two sides of the equation, equation 3.10 is obtained.

$$V_{in} = L\frac{di}{dt} \Rightarrow Ldi = V_{in}dt$$

$$\int_0^{\Delta I} Ldi = V_{in}T_1$$

$$L\Delta I = V_{in}T_1 \Rightarrow T_1 = \frac{L\Delta I}{V_{in}} \tag{3.10}$$

**2nd stage:** When switching transistors, S1 and S2 are off,

$$L\frac{di}{dt} = V_{in} - V_O$$

Two sides of the equation is integrated as the following,

$$\int_{\Delta I}^{0} Ldi = \int_{T_1}^{T_S} (V_{in} - V_O)dt$$

Calculating the above equation, equation 3.11 is derived.

$$-L\Delta I = (V_{in} - V_O)(T_S - T_1) \tag{3.11}$$

In order to remove $T_1$ from the equation 3.11, $T_1$ in equation 3.10 is put in to equation 3.11.

$$-L\Delta I = (V_{in} - V_O)(T_S - \frac{L\Delta I}{V_{in}})$$

$$\Rightarrow L = V_{in(\min)} \frac{(V_O - V_{in(\min)})}{V_O} \Big/ (f_S \Delta I) \tag{3.12}$$

Equation 3.12 expresses the boost inductance, L in terms of the rectifier's output voltage, $V_O$, minimum peak input voltage, $V_{in(\min)}$, the switching frequency, $f_S$ and the input ripple current, $\Delta I$.

Derivation of the output capacitance value using the energy transfer capability of a capacitor is given below:

$E = \frac{CV^2}{2}$, this is the well-known energy formula of a capacitor.

C is the output capacitance and $V$ stands for the voltage over C.

$E_1 = \frac{CV_O^2}{2}$, where $V_O$ is the desired output voltage of the UPF rectifier.

$E_2 = \frac{CV_{O\min}^2}{2}$, where $V_{O\min}$ is the rectifier's permissible output voltage.

Using the energy difference between $E_1$ and $E_2$,

$$E_1 - E_2 = P_{out}\Delta t$$

$$C = \frac{2P_{out}\Delta t}{V_0^2 - V_{O\min}^2} \tag{3.13}$$

In equation 3.13, $P_{out}$ and $\Delta t$ are the rectifier's output power and hold-up time. Equations 3.12 and 3.13 are equal to equations 2.2 and 2.4 respectively. Thus, the boost inductance and output capacitance in figure 2.8(a) are calculated and same

results are found as in section 3.2.2.

The transistors, S1 and S2, and the diodes, D1 and D2 have voltage stresses equal to the rectifier's output voltage. The two transistors and the diodes' current stresses are equal to the rectifier's input peak current. Therefore, their voltage and current stresses are 530 V, 24.494 A. The two transistors' reverse recovery diodes have the same voltage and current stresses as the transistors.

**Needed:**

1. Two diode (1060V, 49 A)
2. Two IGBT with reverse recovery diodes (1060V, 49 A)
3. One capacitor (1124.2uF)
4. One inductor (5.4mH)
5. Complex control circuit or PFC IC to switch IGBTs.

## 3.3 Calculations Of Three Phase Unity Power Factor Rectifiers

Switching transistors' voltage and current ratings, value of power inductors and capacitors, and number of critical components in the single transistor three phase multiresonant ZCS HPF rectifier, 12-pulse voltage source rectifier with PWM-SHE and single controlled switch three phase rectifier with unity power factor and sinusoidal input current, whose mains supply is 3 phase AC supply are calculated according to the specifications in section 3.1 and given in this section.

### 3.3.1 Calculations Of Single Transistor Three-Phase Multiresonant ZCS HPF Rectifier

It is a buck type rectifier so it does not give necessary output voltage 530V. Hence input voltage 3Φ AC 380V(l-l,rms) and output voltage 400V DC is taken for calculations in this configuration. Output power is taken as 3 kW like for other configurations.

In calculations, simplified single input and single output model of the single

transistor three phase multiresonant zero voltage switching high power factor rectifier in figure 2.11 is used. All the equations and the figures below used in calculations are taken from reference 4.

Effective input voltage is given by the equation 3.14 and equation 3.15 expresses the normalized input voltage equation.

$$V_g = \frac{3}{2} V_{an-peak} \tag{3.14}$$

$$M_g = \frac{V_g}{V} \tag{3.15}$$

, where $V$ is the rectifier's output voltage in figure 2.9(a). Effective input voltage for this rectifier is calculated as 465 V by using equation 3.14. Normalized input voltage is found as 1.1625 by putting 400 V as $V$ and 465 V as $V_g$ in to equation 3.15.

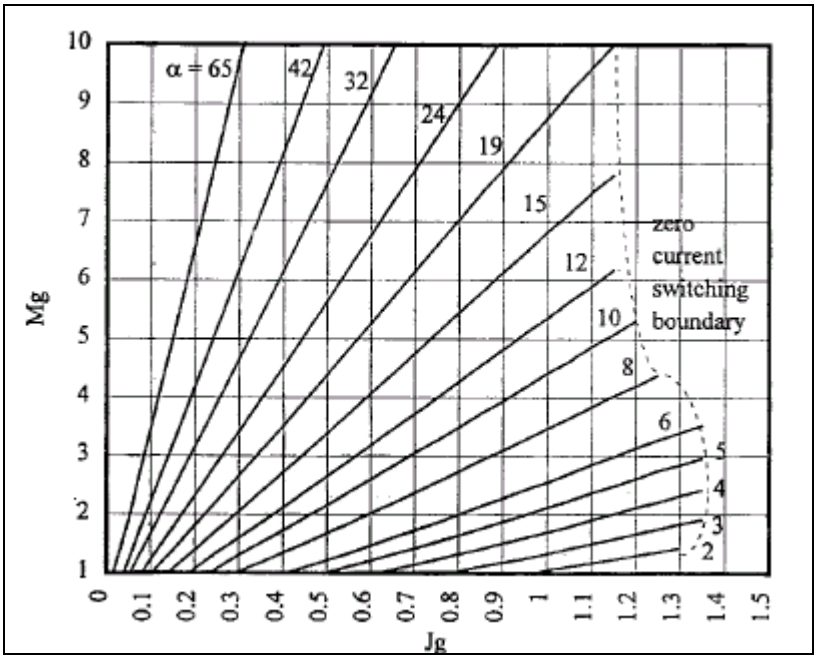



**Figure 3.1** The normalized input characteristic of the single-transistor three-phase multiresonant ZCS HPF rectifier. The normalized transistor off time α is expressed in radians.

Maximum normalized peak input current, $J_g$ is calculated as 1.3 by using the graphic in figure 3.1 at $M_g$ = 1.1625 for 3 kW rectifier. Normalized frequency, F is calculated as 1.22 by using the equation 3.16 and taking $\alpha$ as 2 ($\alpha$ is calculated as 2 using the figure 3.1 when $M_g$ is equal to 1.1625 and $J_g$ is taken as 1.3).

$$\text{Normalized frequency, } F = \frac{2\Pi}{\alpha + \Pi} \tag{3.16}$$

The rectifier's output current, $I_{out}$ is calculated as 7.5 A since its output power is 3 kW, and its output voltage is 400V. Characteristic impedance equation is given in the following equation. The characteristic impedance is calculated as 80.6 Ω putting the necessary values calculated above in to equation 3.17.

$$R_o = M_g J_g \frac{V}{I} \tag{3.17}$$

Base frequency, $f_o$ is calculated as 16.39 kHz by taking switching frequency, $f_s$ as 20 kHz and putting the value of normalized frequency, F in to equation 3.18.

$$f_o = \frac{f_s}{F} \tag{3.18}$$

$$R_o = \sqrt{\frac{L_r}{C_x}} \tag{3.19}$$

, where $C_x$ is effective capacitance, and $L_r$ is resonant tank inductor in figure 2.11. Another base frequency equation is given in equation 3.20.

$$f_o = \frac{1}{2\Pi\sqrt{L_r C_x}} \tag{3.20}$$

Values of $C_x$ and $L_r$ are calculated as 0.12 uF and 0.78 mH respectively by using equation 3.19 and 3.20.

$$C_x = \frac{2}{3} C_r \tag{3.21}$$

, where $C_r$ is the capacitance of one of the input side resonant tank capacitors $C_{r1}$, $C_{r2}$, and $C_{r3}$. $C_x$ and $C_r$ are related with each other as in the equation 3.21. Using the equation 3.21, $C_r$ is calculated as 0.18uF.

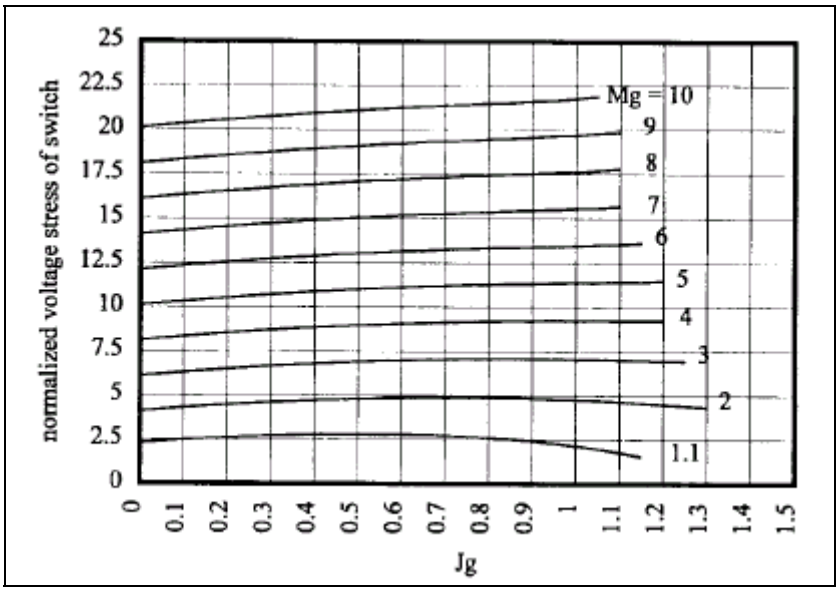



**Figure 3.2** Normalized voltage stress of switch $S_1$.

Normalized voltage stress is calculated as 3 for this rectifier at $M_g$ = 1.1625 and $J_g$ = 0.7 by using the figure 3.2. $J_g$ is taken as 0.7 at $M_g$ = 1.1625 since the switch's normalized voltage stress is at its peak when $J_g$ is equal to 0.7.

$$V_{s1} = M_{s1} \times V \tag{3.22}$$

, where $M_{s1}$ is normalized voltage stress and $V_{s1}$ is the switch, S1's peak voltage. The switch, S1's voltage stress with safety margin is calculated as 1200 V by using equation 3.22.

The switch, S1's normalized maximum current stress is observed as 3.75 from figure 3.3 when $M_g$ and $J_g$ are equal to 1.1625 and 0.8 respectively.

Peak switch current is given by the equation 3.23.

$$I_{s1} = J_{s1} \times \frac{V}{R_o} \tag{3.23}$$

, where $J_{s1}$ is normalized peak switch current. The peak switch current is calculated as 18.6 A by using the equation 3.23.

The output diode, $D_d$'s normalized maximum voltage stress is observed as 3 from figure 3.4 when $M_g$ and $J_g$ are equal to 1.1625 and 0.4 respectively. Its peak voltage stress is expressed by equation 3.24.

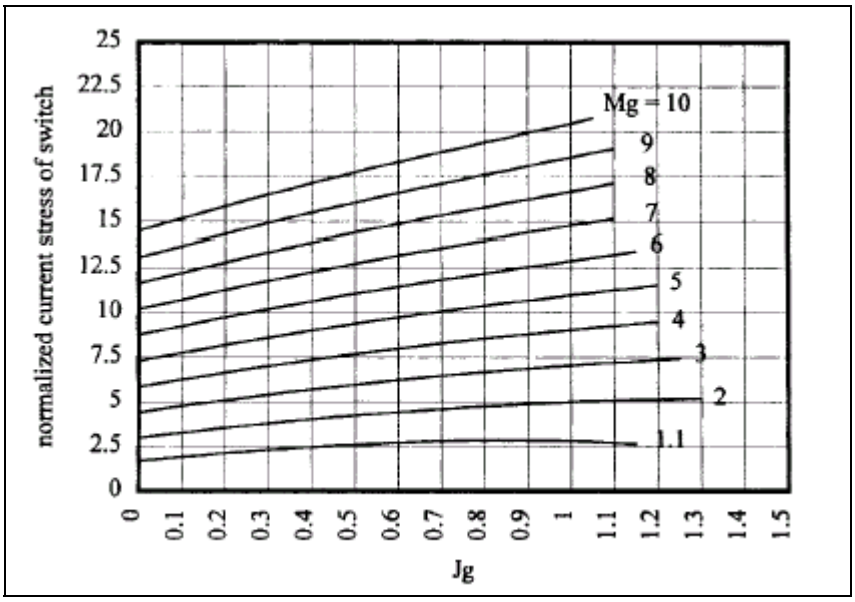



**Figure 3.3** Normalized current stress of switch S1.

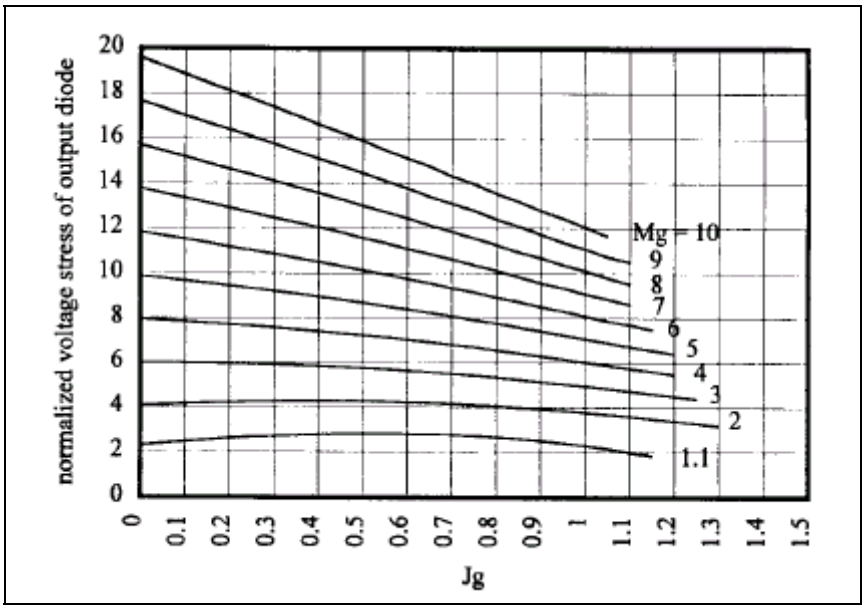



**Figure 3.4** Normalized voltage stress of output diode.

$$V_{Dd} = M_{Dd} \times V \tag{3.24}$$

, where $V_{Dd}$ stands for the diode's peak voltage stress and $M_{Dd}$ is its normalized voltage stress. Its current stress is equal to the rectifier's output current (7.5 A). Input diodes, D1, D2, D3, D4, D5, D6 in figure 2.9(a) have the same rating as the switching transistor.

**Needed:**

1. Five inductor ($L_r$ = 0.78 mH critical)
2. Five capacitor ($C_r$ = 0.12 uF critical)
3. One output diode (1200 V, 7.5 A), 6 input diode
4. One IGBT or power transistor (1200 V, 18.6 A)
5. Microcontroller or an special IC to calculate and switch the IGBT at proper times.

### 3.3.2 Calculations Of 12-Pulse Voltage Source Rectifier With PWM-SHE

12-Pulse voltage source rectifier with PWM-SHE is explained before in section 2.3.2. Its output capacitances, input inductances and switching transistors' current and voltage stresses are calculated by using the specifications given in section 3.1 in this section.

Switching angles, $\alpha_1$, $\alpha_{11}$ and $\alpha_{13}$ are calculated as $31.41^0$, $5.2611^0$ and $2.5667^0$ respectively by using equation 2.16, 2.17, and taking $a_{11}$, $a_{13}$, $a_1$, M as 0, 0, 0,9, 0,9 as in reference [5].

$e_1$ and $e_2$ are two of three phase voltages of the upper part of the rectifier and they are expressed in equation 3.25 and equation 3.26 respectively.

$$e_1 = 190\sqrt{2}\cos wt \tag{3.25}$$

$$e_2 = 190\sqrt{2}(\cos(wt - 120)) \tag{3.26}$$

$$(L_1 + L_2)\frac{di}{dt} + e_1 + u_C - e_2 = 0 \tag{3.27}$$

Equation 3.27 is the node voltage equation of the rectifier's upper part in the converter in figure 2.12. In this equation, $u_C$ stands for the rectifier's upper part's output voltage and $L_1$ and $L_2$ are two of the three inductors in the upper part of the

rectifier.

$$i_1 = I\cos wt \tag{3.28}$$

, where $i_1$ is the current flowing through the inductor, $L_1$ and $i_2$ is the current flowing through the inductor, $L_2$ and it is $120^0$ phase delayed version of the current, $i_1$. I is the magnitude of $i_1$or $i_2$. I is calculated as 3.9176 A by dividing its output power to $i_1$ in rms and multiplying by $\sqrt{2}$.

Assuming its input ripple current can be 5 % peak to peak, ΔI is calculated as 0.20089A. $f_s$ can be as small as 350 Hz in this configuration [5].

$$\Delta wt = 5.2611^0 - 2.5667^0 = 2.6944^0$$

$$\Rightarrow \Delta wt = 2\Pi f\Delta t = 2.6944^0 \Rightarrow \Delta t = 0.003309\,\text{s}$$

Equation 3.29 is derived by investigating the rectifier when $\Delta t$ is equal to 0.003309 s and putting the $e_1$ in equation 3.25 and the $e_2$ in equation 3.26 in to equation 3.27 and splitting the currents $i_1$ and $i_2$ in to two parts, one with ripple and the other without ripple.

$$L_1(\frac{di_1}{dt} + \frac{\Delta I}{\Delta t}) + L_2(\frac{di_2}{dt} + \frac{\Delta I}{\Delta t}) + 190\sqrt{2}[\cos(wt - 120) - \cos wt] + u_C = 0 \tag{3.29}$$

$L_1$ and $L_2$ are calculated as 128.337 mH by using the calculated values of Δt and ΔI when wt is equal to $120^0$. When switching frequency is taken as 20 kHz, each of these inductances will be nearly 2.25 mH. In these calculations, $u_C$ is taken as 275 V since the rectifier's output voltage is 550 V and the rectifier has two part and their output voltage is assumed as $1/2$ times the rectifier's output voltage.

$$C = \frac{I_m}{4 f_s V_{dr}}\left[\cos(\frac{\Pi M}{4}) - \cos(\frac{\Pi M}{2})\right] \tag{3.30}$$

The relationship between its output capacitance, C, input line current, $I_m$, switching frequency, $f_s$, modulation index, M and output voltage ripple, $V_{dr}$ is given by the equation 3.30, and total output capacitance is calculated as 1.6 uF (modulation index, M = 0.667, $I_m$ = 3.9176 A, switching frequency, $f_s$ = 20 kHz, 2 % of its output voltage = output voltage ripple = 11 V) but its total output capacitance is calculated as 93 uF when its switching frequency, $f_s$ is equal to 350 Hz. Since there are two capacitors in series at its output side, each of the two capacitances is 3.2 uF but 186 uF when its switching frequency, $f_s$ is equal to 350 Hz.

IGBT voltage stress is equal to half of its output voltage. IGBT current stress is equal to $I + \Delta I$ (4.12A).

**Needed**

1. Three winding transformer
2. 12 IGBT (550V, 8.24A)
3. 6 inductor (each 2.25 mH)
4. 2 capacitor (3.2 uF)
5. Microcontroller (and EEPROM) or DSP IC is required to calculate the necessary switching angles.

### 3.3.3 Calculations Of Single Controlled Switch Three Phase Rectifier With Unity Power Factor And Sinusoidal Input Current

In this section, main power semiconductors' current and voltage stresses and the boost inductance and main capacitances in the rectifier expressed in section 2.3.3 are calculated according to the specifications given in section 3.1.

Normalized value of the boost inductor, $I_{LBn}$, normalized switching frequency, $F_{sn}$, normalized output resistance of the rectifier, $R_{outn}$ can be selected as 4, 0.954 and 50 respectively by considering silicon utilization, voltage stress across the semiconductor devices and the cost and size of reactive elements [6].

Normalized base current, base impedance, base voltage, base frequency are given in equation 3.31, 3.32, 3.33, 3.34 [6].

Base current, $I_b = V_b / Z_b$ (3.31)

Base impedance, $Z_b = \frac{\sqrt{L_B}}{\sqrt{C_e}}$ (3.32)

, where $L_B$ is the boost inductance and $C_e$ is the equivalent capacitance of the capacitors, $C_{sa}$, $C_{sb}$, and $C_{sc}$ in figure 2.15 when the capacitors are connected parallel.

Base voltage, $V_b = V_{out}$ (3.33)

Base frequency, $F_b = \frac{1}{2\Pi\sqrt{L_B C_e}}$ (3.34)

Taking switching frequency, fs as 20 kHz and the rectifier's output voltage, $V_{out}$ as 550 V and using the equations 3.35 and 3.36 given in reference [6], the boost

inductor, $L_B$ and equivalent input capacitance, $C_e$ are calculated as 15.3 uH and 3.76 uF respectively.

$$L_B = \frac{R_{out} F_{sn}}{2\Pi R_{outn} f_s} \tag{3.35}$$

, where $R_{out}$ is the rectifier's output resistance or load resistance.

$$C_e = \frac{R_{outn} F_{sn}}{2\Pi R_{out} f_s} \tag{3.36}$$

$$C_e = \frac{2}{3} C_{sa} \tag{3.37}$$

Putting the calculated value of the equivalent input capacitance, $C_e$ in to the equation 3.37 given in reference [6], the input capacitance, $C_{sa}$ is calculated as 5.65 uF. Since the input capacitances, $C_{sb}$ and $C_{sc}$ have same capacitance with $C_{sa}$, their values are also 5.65 uF. In this topology, equation 3.13 can be used for the calculation of the output capacitor. The output capacitance is calculated as 1044 uF by taking hold-up time, output power, output voltage and worst-case minimum output voltage as 10 ms, 3 kW, 550 V, 495 V respectively and using equation 3.13.

The switching transistor's voltage stress is calculated as 550V by ignoring voltage drop of $D_B$. Its current stress is same as one of the rectifier's input peak phase current, which is equal to 3.38 A. Current and voltage stresses of the power diodes in figure 2.15 are same as those of the IGBT.

**Needed:**

1. 1 IGBT (1100 V, 6.76 A)
2. 4 capacitor (three of them is 5.65 uF and one is 1044 uF)
3. 1 boost inductor (15.3 uH) and 3 input inductor
4. 7 power diode (1100 V, 6.76 A)
5. Unity power factor integrated circuit is needed.

### 3.4 Results of Calculations

Critical electrical components in the rectifier topologies investigated in chapter 2 are calculated in this chapter. The calculation results are summarized in

| TOPOLOGY | TRANSISTOR | Critical L | C | COMMENT |
|---|---|---|---|---|
| **Single Phase Half-Bridge Boost Topology** | 2 IGBT (1269, 1.414A) | 6.47 mH | 2 capacitor (each 204 uF) | UPF IC or specific IC to drive IGBTs. Output voltage should be 2 times input voltage amplitude |
| **Front-End Rectifier Followed By A Boost Converter** | 1 IGBT (1060, 49A) | 5.4 mH | 1 capacitor (1124.2 uF) | This topology is very cheap and easy to implement and also it satisfies all necessary specification. This configuration needs UPF IC |
| **Low Conduction Loss AC/DC UPF Rectifier** | 2 IGBT (1060, 49A) | 5.4mH | 1 capacitor (1124.2uF) | Conduction loss is lower than front-end rectifier followed by a boost converter |
| **Single Transistor Three Phase Multiresonant ZCS HPF Rectifier** | 1 IGBT (1200V, 18.6 A) | 0.78mH | No comment about its output capacitor in reference [4] | Microcontroller or special IC needed to calculate and switch the IGBT at proper times |
| **12-Pulse Voltage Source Rectifier with PWM-SHE** | 12 switching transistor (550V, 8.24A) | 6 inductor (each 2.25 mH) | 2 capacitor (each 3.2 uF) | DSP or microcontroller is needed to switch the IGBTs using SHE technique |
| **Single Controlled Switch Three Phase Rectifier with Unity Power Factor and Sinusoidal Input Current** | 1 IGBT (1060V, 6.76 A) | 15.3 uH | 1044uF | UPF IC is needed |

**Table 3.1** Comparison of the rectifiers.

table 3.1.

Single transistor three phase multiresonant ZCS (zero current switching) HPF (high power factor) rectifier scheme uses single switching transistor, but it needs microcontroller or special integrated circuit to switch the IGBT at proper times.

In 12-pulse voltage source rectifier with pulse width modulation-specific harmonic elimination method, the switching frequency can be as low as 350 Hz. However, it uses 12 switching transistor such as IGBT or GTO. Microcontroller or DSP integrated circuit is needed to control the switching transistors. It is suitable for high power applications (e.g. 100 kVA).

Single controlled switch three phase rectifier with unity power factor and sinusoidal current uses a single switching transistor, and a PFC integrated circuit is enough to control the switching transistor.

Single phase mains supply is much more available than three phase mains

supply. Hence a single phase unity power factor rectifier topology is more convenient to design a 3 kW unity power factor rectifier although a 3 kW three phase unity power factor rectifier can also be designed.

Single phase half-bridge boost topology requires two switching power transistor. Output voltage can not be smaller than two times of the mains supply's voltage amplitude. In Turkey, single phase mains supply's voltage amplitude is 311 V ($220 \times \sqrt{2}$) and two times of this value is equal to 622 V. Its required output voltage should be between 400 and 550 V, so single phase half-bridge boost topology mentioned in chapter 3 is not selected to simulate.

In front-end rectifier followed by a boost converter topology, one transistor is used for switching purposes, but diode, D in figure 2.6 increases conduction losses.

Low conduction loss AC/DC UPF rectifier uses two switching transistor, but there is no diode bridge. It has relatively complex control circuit given in figure 2.8 comparing the front-end rectifier followed by a boost converter's control circuit, but it can be controlled with a PFC integrated circuit as the front-end rectifier followed by a boost converter. However, application of PFC integrated circuit with the low conduction loss AC/DC UPF rectifier topology is not tested. This is beyond the scope of the thesis.

Front-end rectifier followed by a boost converter topology is selected to simulate and compare with a proposed single transistor unity power factor rectifier expressed in chapter 4 since the front-end rectifier followed by a boost converter topology's mains supply is single phase supply and it is much more available than three phase mains supply, it has simple control circuit using only one PFC integrated circuit, and it can give necessary output voltage and power.

# CHAPTER 4

# PROPOSED SINGLE PHASE SINGLE SWITCHING TRANSISTOR UPF RECTIFIER TOPOLOGY

## 4.1 Introduction

Front-end rectifier followed by a boost converter configuration in figure 2.6 uses single switching transistor and it has simple control circuit, but its conduction loss higher than low conduction loss AC/DC unity power factor rectifer in figure 2.8 while it uses two switching transistors. On the other hand, proposed single phase single switching transistor unity power factor rectifier has simple control circuit and lower conduction loss than front-end rectifier followed by a boost converter and the low conduction loss AC/DC unity power factor rectifier in figure 2.8.

The theory behind proposed single switching transistor low conduction loss unity power factor rectifier is that one switching power transistor can be used instead of two switching power transistor in the low conduction loss AC/DC unity power factor rectifier since the two transistors are turned on an off at the same time. In addition, the proposed single switching transistor low conduction loss unity power factor rectifier should be controlled with a standart unity power factor rectifier integrated circuit.

In this chapter, a new single switching transistor unity power factor topology with low conduction loss is proposed. Its operation principle and analytic analysis are given in the following sub-chapters in this chapter.

## 4.2 Proposed Single Phase Single Switching Transistor UPF Configuration

A single phase, single switching transistor unity power factor rectifier topology is proposed and its operation principle is given in this sub-chapter. It has one single phase diode bridge, two boost inductors, two ultrafast diodes, one output capacitor and single switching transistor. Actually, one boost inductor can be used instead of two boost inductor since these two boost inductors are serially connected to each other with respective to the mains supply. Two boost inductors whose total inductance is same as the boost inductor are used for making the topology symmetric with respective to mains supply. The proposed topology is shown in figure 4.1.

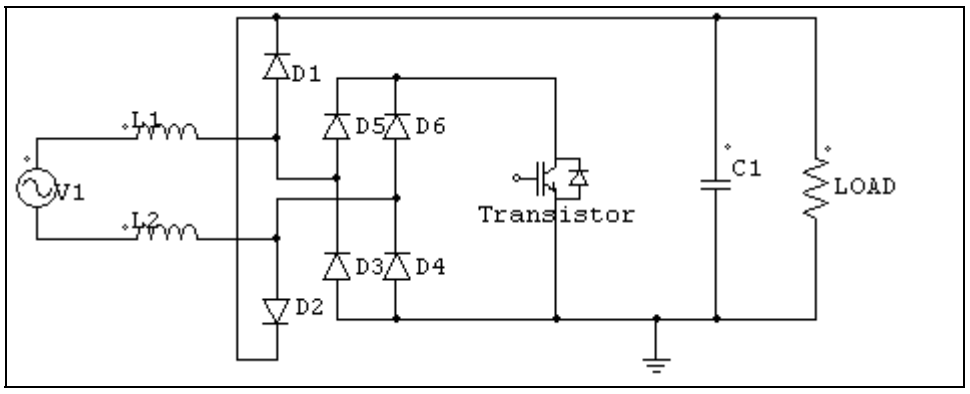



**Figure 4.1** Proposed single phase single switching transistor UPF rectifier.

Operation principle of proposed low conduction loss UPF rectifier configuration in figure 4.1 described below:

**1st step:** When switching transistor is on and mains supply's voltage phase is between 0 and $180^0$, current flows through inductor L1, D5, transistor, diode D4 and inductor L2. Since transistor is on, it is seen that these inductors are connected to supply directly and they begin to store energy. Topology looks like in figure 4.2 at this time.

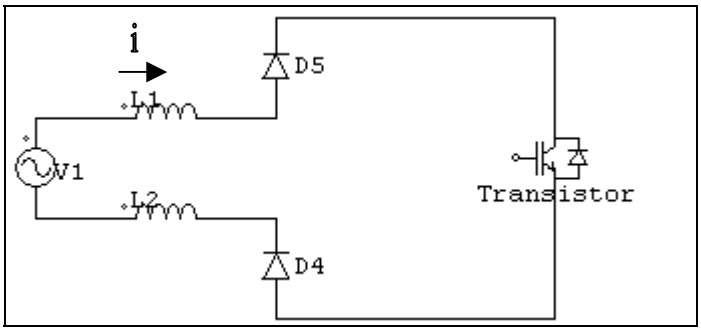



**Figure 4.2** Equivalent circuit when switching transistor on and mains supply's voltage phase is between 0 and $180^0$.

**2nd step:** Switching transistor is off and mains supply's voltage phase between 0 and $180^0$, current i flows through L1, D1, C1, D4, L2 and the mains supply. In this way, inductor L1, L2 start to give stored energy to load and capacitor C1.

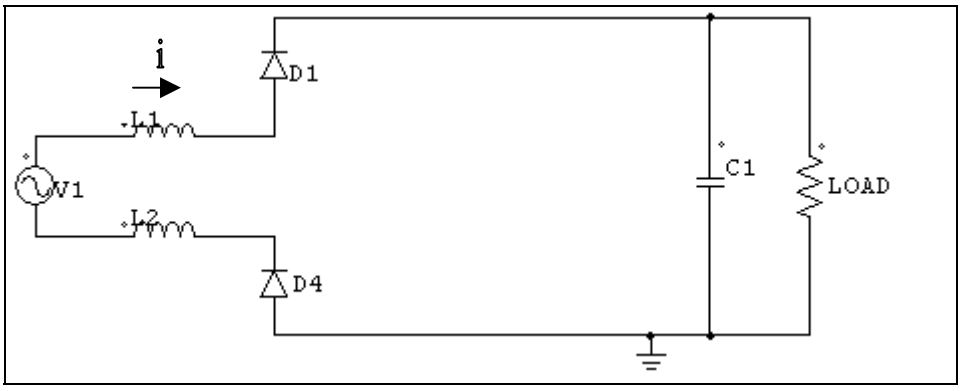



**Figure 4.3** Equivalent circuit when switching transistor is off and mains supply's voltage phase is between 0 and $180^0$.

**3rd step:** When mains supply's voltage phase is between 180 and $360^0$ and the switching transistor is on, current flows through L2, D6, the switching transistor, D3, L1, and the inductors store energy. However, current direction and inductor voltage polarity is reversed. The topology looks like as in figure 4.4 at this time.

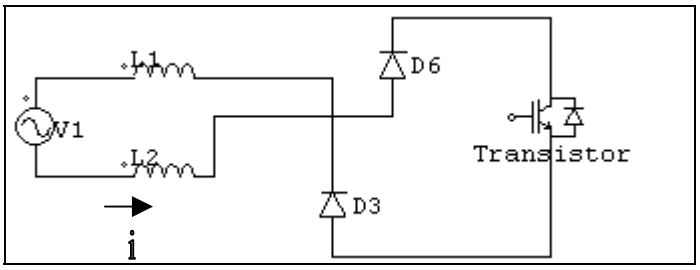



**Figure 4.4** Equivalent circuit when mains supply's voltage phase is between 180 and $360^0$, switching transistor is on.

**4th step:** When mains supply's voltage phase is between 180 and $360^0$ and the switching transistor is off, current flows through D2, C1, D3 and L1. The topology looks like in figure 4.5 now.

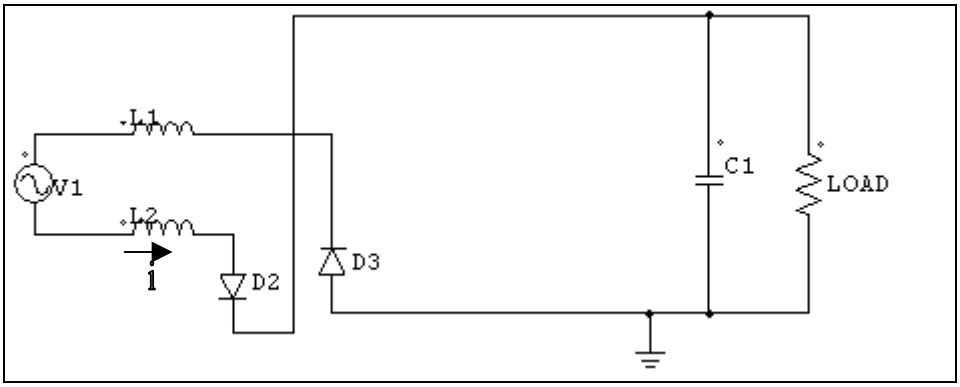



**Figure 4.5** Equivalent circuit when mains supply's voltage phase is between 180 and $360^0$ and switching transistor is off.

The boost inductors, L1 and L2, store electrical energy in 1st and 3rd step while they destore and give the electrical energy to the output capacitor, C1 and the load in 2nd and 4th step. In this way, the proposed topology achieves boost operation.

### 4.2.1 Comparison Of The Proposed Rectifier With Front-End Rectifier Followed By A Boost Converter And Low Conduction Loss AC/DC UPF Rectifier

Proposed unity power factor rectifier is compared with the front-end rectifier followed by a boost converter in figure 2.6 and the low conduction loss AC/DC unity power factor rectifier in figure 2.8 on the basis of efficiency, number of semiconductors. Comparisons are made roughly here. The proposed rectifier and front-end rectifier followed by a boost converter are compared in detail in chapter 6 by making simulations.

Proposed rectifier topology in figure 4.1 is better than front end rectifier followed by a boost converter in figure 2.6 with respect to following characteristics:

1. In the proposed topology, the boost diode, D in figure 2.6 is eliminated. In front-end rectifier followed by a boost converter, two bridge diode is on when the transistor is on as in the proposed topology. Two bridge diode and the boost diode, D in figure 2.6 is on in the front- end rectifier followed by a boost converter while only one bridge diode and one boost diode, D1 or D2 is on according to the mains supply's polarity when the transistor is off. Hence, proposed rectifier's conduction loss is less than the front-end rectifier followed by a boost converter. Front-end rectifier followed by a boost converter topology is redrawn in figure 4.6. Its equivalent circuit when the transistor is on and off is shown in figure 4.7 and figure 4.8.
2. In the proposed rectifier topology, inductor core resetting is achieved naturally due to reversing of input current direction at every half cycle of the input voltage, so free-wheeling diode is not necessary and it can not be used with parallel to boost inductors, L1 and L2. In front-end rectifier followed by a boost converter, one free wheeling diode has to be used and connected

parallel to boost inductor, $L_S$ and the boost diode, D in figure 2.6.

Although proposed topology has the mentioned advantages, the bridge diodes, D3, D4, D5, D6 in proposed topology have higher voltage stresses than the bridge diodes in front-end rectifier followed by a boost converter since the boost inductors L1 and L2 are connected between mains supply and the bridge diodes in proposed topology. The bridge diodes D3, D4, D5, D6 in proposed topology will have voltage stresses same with switching transistor in figure 4.1 since the diode bridge is connected parallel with the transistor.

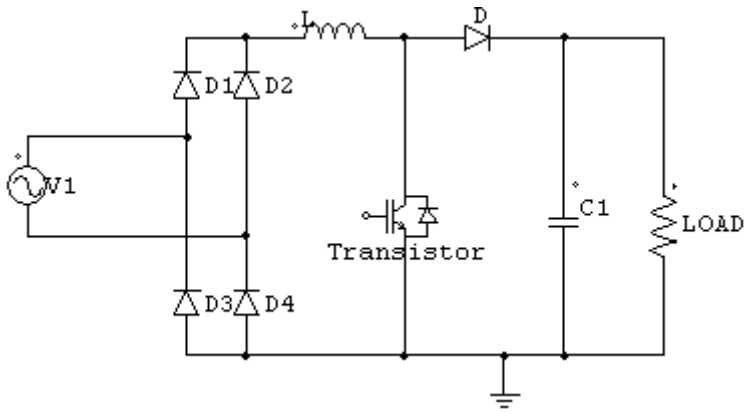



**Figure 4.6** Front-end rectifier followed by a boost converter topology.

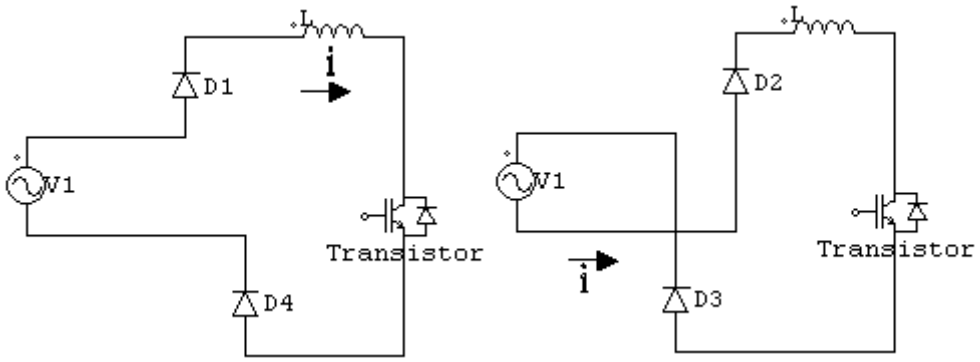
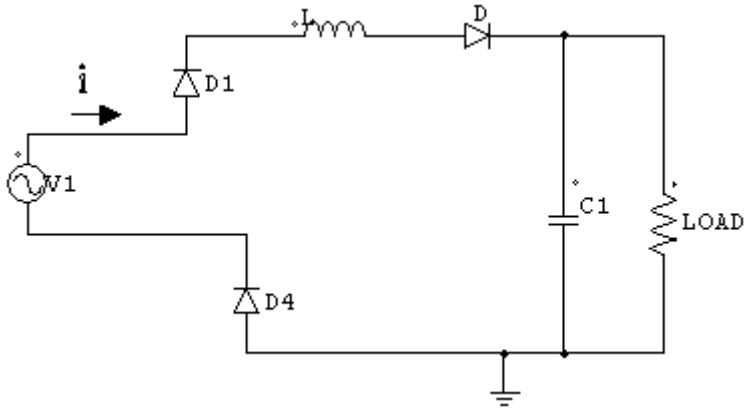
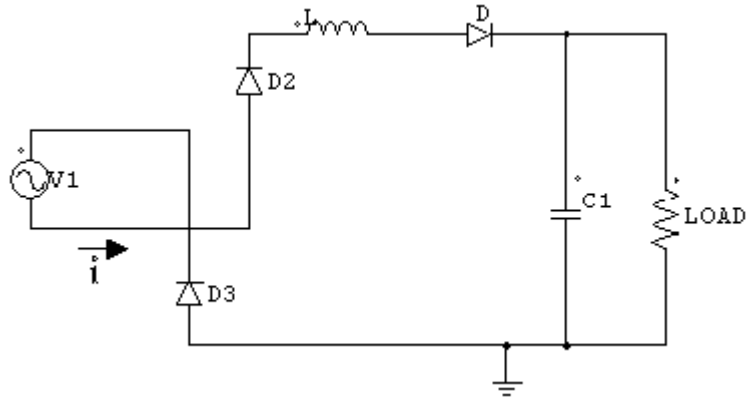



**Figure 4.7** Front-end rectifier followed by a boost converter's equivalent circuit when the switching transistor is on (a) mains supply's voltage phase is between 0 and $180^0$, (b) mains supply's voltage phase is between 180 and $360^0$.




**(a)**




**(b)**

**Figure 4.8** Front-end rectifier followed by a boost converter's equivalent circuit when the switching transistor is off (a) mains supply's voltage phase is between 0 and $180^0$, (b) mains supply's voltage phase is between 180 and $360^0$.

Performance of the proposed rectifier topology and low conduction loss AC/DC UPF rectifier in figure 2.8 are compared, their advantages and disadvantages are listed:

1. Proposed rectifier scheme uses only one switching transistor while other one uses two switching transistor (the three transistor ratings are nearly equal). Proposed UPF rectifier has one diode bridge but the other one don't have diode bridge, it uses two ultrafast diodes and two switching transistors' freewheeling diode as diode bridge.

2. In the rectifier in figure 2.8(a), two switching transistor turned on and off simultaneously. When the transistors are on, input current flows through one transistor such as an IGBT and the second transistor's freewheeling diode. When the transistor is on in proposed topology, input current flows through two bridge diodes and one transistor. At this time, the rectifier in figure 2.8 has low conduction loss but the difference is small since freewheeling diodes have relatively higher voltage drop than bridge diodes in general. On the other hand, the transistors in figure 2.8 are off, input current flows through the boost diode, D1 or D2 and one of the transistor's free-wheeling diode in low conduction loss AC/DC unity power factor rectifier while the transistor in figure 4.1 is off, the current flows through boost diode D1 or D2 and bridge diode D4 or D3 depending on the mains supply's polarity in proposed topology. Hence, proposed topology has lower conduction loss than the ones in figure 2.8 since the transistors' freewheeling diode have generally higher conduction voltage drop than the bridge diode's conduction voltage drop.

The rectifier topology in figure 2.8 is redrawn in figure 4.9 and its equivalent circuits when the transistors are on and off are shown in figure 4.10 and 4.11.

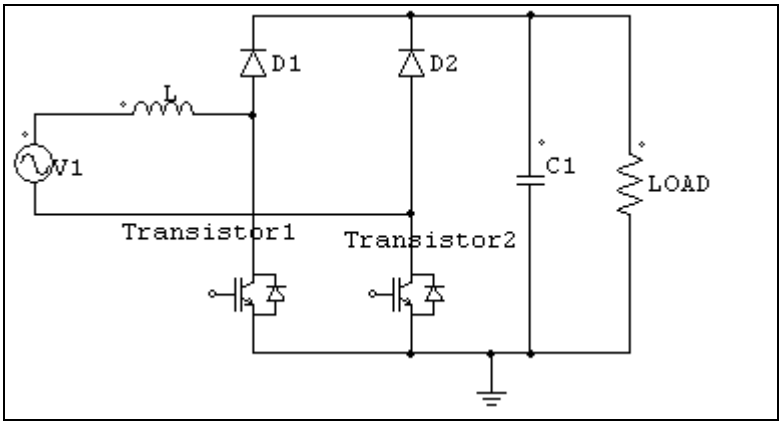
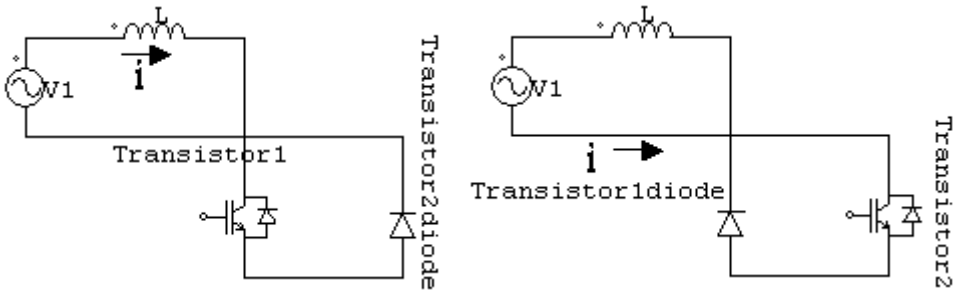
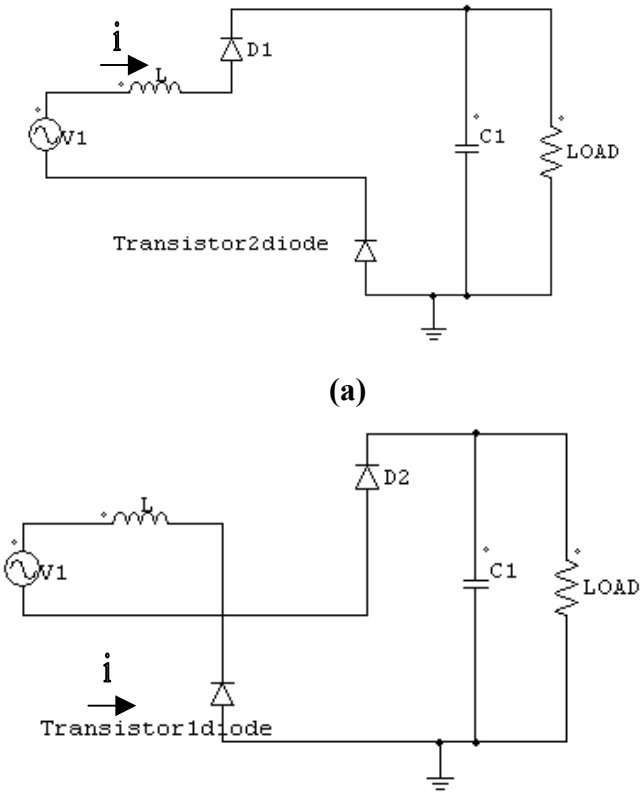



**Figure 4.9** Low conduction loss AC/DC UPF rectifier topology.




**(a)** **(b)**

**Figure 4.10** Low conduction loss AC/DC UPF rectifier's equivalent circuit when the switching transistor is on (a) mains supply's voltage phase is between 0 and $180^0$, (b) mains supply's voltage phase is between 180 and $360^0$.




**(a)**

**(b)**

**Figure 4.11** Low conduction loss AC/DC UPF rectifier's equivalent circuit when the switching transistor is off (a) mains supply's voltage phase is between 0 and $180^0$, (b) mains supply's voltage phase is between 180 and $360^0$.

In order to understand whether proposed unity power factor rectifier topology or the one in figure 2.8 has lower conduction loss, the rectifier topology specifications and diodes and switching transistors used in implementation have to be known. In unity power factor rectifier implementation part in this thesis, HGTG20N60A4D IGBT, RURG5060 ultra fast diode, VBO30-12N07 diode bridge are used as switching transistor, boost diode and single-phase diode bridge respectively. Also, the boost rectifier implemented has nominal 220 V rms input voltage, 440 V output voltage and 3 kW output power. These specifications are given in chapter 6. Equation 2.2 is applicable to front-end rectifier followed by a boost converter in figure 2.6, low conduction loss AC/DC unity power factor rectifier in figure 2.8 and proposed rectifier topology since they are all boost rectifier topologies and their operation principle is similar. Average duty ratio can be calculated using equation 2.2 and putting rectified input voltage's average value instead of input minimum voltage to this equation as input voltage, and it is 0.55. The rectifiers' efficiencies are assumed as 100 % to simplify the semiconductors' conduction loss calculations. The rectifiers input current can be calculated using equation 4.1.

$$I_{in(rms)} = \frac{P_{in}}{V_{in(rms)}} \tag{4.1}$$

, where $V_{in(rms)}$ is the rectifiers' input voltages, and $P_{in}$ is their input voltage. Then, the rectifiers' input currents are nearly 13.64 A rms. HGTG20N60A4D IGBT and its free-wheeling diode have 1.6 V, 1.8 V conduction voltage drop while their junction temperatures and currents are 125 $^0$C, 13.64 A. RURG5060 ultra fast diode has 0.9 V conduction voltage drop when its junction temperatures and currents are 100 $^0$C, 13.64 A. One diode in VBO30-12N07 diode bridge has 1 V conduction voltage drop when its current is 13.64 A. Proposed rectifier topology and the other ones' semiconductor conduction loss can be calculated using the equation 4.2 when the transistors are on, the equation 4.3 when they are off.

$$Conductionloss = Semiconductorsvoltagedrop \times rmscurrent \times D \tag{4.2}$$

$$Conductionloss = Semiconductorsvoltagedrop \times rmscurrent \times (1 - D) \tag{4.3}$$

The rectifier in figure 2.8 has nearly 25.5 watts when the transistors are on, 16.57 watts while the transistors are off, and so total semiconductor conduction losses are 42.07 watts. Proposed rectifier has 27 watts semiconductor conduction losses when the switching transistor is on and 11.66 watts when it is off. Hence, its total

semiconductor conduction losses are 38.66 watts.

Proposed unity power factor rectifier topology has lower semiconductor conduction losses than the ones in low conduction loss AC/DC unity power factor rectifier in figure 2.8 when HGTG20N60A4D IGBT and RURG5060 ultrafast diode are used as power semiconductors in these topologies. IGBTs' free-wheeling diodes have to be very fast and their conduction voltage drop has generally a higher value than bridge diodes and boost diodes which are also ultrafast diode but not needed to be so fast as much as IGBTs' free-wheeling diodes. Low conduction loss AC/DC unity power factor rectifier in figure 2.8 uses IGBTs' freewheeling diodes to conduct the current, i in figure 4.10 and 4.11. Therefore, proposed rectifier has higher efficiency than the one in figure 2.8 considering the semiconductor conduction losses.

### 4.2.2 Analysis Of The Proposed UPF Rectifier Analytically

Proposed unity power factor rectifier topology's inductance and capacitance values are investigated analytically in this section. Expressions to its output capacitance and boost inductance value are derived.

Basic relationship formula of the inductor is

$$V_{LS} = L\frac{di}{dt} \tag{4.4}$$

The voltage over the inductor in figure 4.1 equal to $V_{LS} = V_{in} - V_o$.

**1st stage:** When the power transistor is on and $0 \le V_{in} < 180^0$,

$$V_{in} = L\frac{di}{dt} \Rightarrow Ldi = V_{in}dt$$

Equation 4.5 is obtained by integrating two sides of the above equation.

$$\int_0^{\Delta I} Ldi = V_{in}T_1$$

$$L\Delta I = V_{in}T_1 \Rightarrow T_1 = \frac{L\Delta I}{V_{in}} \tag{4.5}$$

**2nd stage:** When the power transistor is off, $0 \le V_{in} < 180^0$,

$$L\frac{di}{dt} = V_{in} - V_O .$$

Integrating two sides of the above equation, equation 4.6 is derived.

$$\int_{\Delta I}^{0} Ldi = \int_{T_1}^{T_S} (V_{in} - V_O)dt$$

$$-L\Delta I = (V_{in} - V_O)(T_S - T_1) \tag{4.6}$$

In order to remove $T_1$ from the equations, $T_1$ in equation 4.5 is placed in to equation 4.6. Then, equation 4.7 is derived.

$$-L\Delta I = (V_{in} - V_O)(T_S - \frac{L\Delta I}{V_{in}})$$

$$\Rightarrow L = V_{in(\min)} \frac{(V_O - V_{in(\min)})}{V_O} \Big/ (f_S \, \Delta I) \tag{4.7}$$

Equation 4.7 gives the proposed rectifier's boost inductance value. L1 and L2 in figure 4.1 have an inductance value, which is half of the inductance value calculated using equation 4.7 since L1 and L2 are serially connected to each other.

Using "capacitor energy equation" given below, derivation of equation 4.8 is made.

$$E = \frac{CV^2}{2}$$

In above equation, E is the energy stored in C and V is the voltage over C.

$E_1 = \frac{CV_O^2}{2}$, where $V_O$ is the rectifier's desired output voltage.

$E_2 = \frac{CV_{O\min}^2}{2}$, where $V_{O\min}$ is the rectifier's permissible minimum output voltage. Taking difference of $E_1$ and $E_2$, the following equation is obtained.

$$E_1 - E_2 = P_{out}\Delta t$$

In this equation, $P_{out}$ is the rectifier's output power and $\Delta t$ is hold-up time. Using above last three equations, equation 4.8 is derived.

$$C = \frac{2P_{ouuu}\Delta t}{V_0^2 - V_{O\min}^2} \tag{4.8}$$

Longer hold-up time, $\Delta t$ chosen in a design can tolerate supply interruptions with short duration at the expense of bulky and costly capacitor banks. A

compromise can be made between these factors [2].

Equation 4.7 and 4.8 are same with equation 2.2 and 2.4, so the output capacitances and boost inductances in the proposed rectifier and the popular front-end rectifier followed by a boost converter can be calculated with these equations. Also, they are applicable to the low conduction loss AC/DC unity power factor rectifier in figure 2.8.

### 4.3 Result

Proposed unity power factor rectifier topology is investigated analytically, and expressions given its boost inductance and output capacitance values are derived. These expressions are directly applicable to the front-end rectifier followed by a boost converter in figure 2.6 and the low conduction loss AC/DC unity power factor rectifier in figure 2.8.

The low conduction loss AC/DC unity power factor rectifier uses two switching transistors while the proposed rectifier and the front-end rectifier followed by a boost converter use only one switching transistor. However, number of diodes used in the low conduction loss AC/DC unity power factor rectifier is less than the two unity power factor rectifier topologies. The proposed rectifier uses two boost diode but one conducts in mains supply's one half cyle, the other one in the other half cycle. On the other hand, the front-end rectifier followed by a boost converter needs free-wheeling diode parallely connected to boost inductor and boost diode to achieve the boost inductor's core resetting. Thus, total power diode number including bridge diode, boost diode and free-wheeling diode is same in these two rectifier topologies. Bridge diodes' voltage stresses in proposed topology are higher than the front-end rectifier followed by a boost converter.

Proposed topology has lower semiconductor conduction losses than the other two rectifier topologies. It is chosen to implement since it has single switching power transistor as the front-end rectifier followed by a boost converter and has higher efficiency considering the semiconductor conduction losses. Front-end rectifier followed by a boost converter and proposed topology are selected to compare with

each other since they have single switching transistor and front-end rectifier followed by a boost converter is more popular topology than the one in figure 2.8, so they are investigated in detail by making simulations in chapter 6.

The classical unity power factor rectifier, called front-end rectifier followed by a boost converter and proposed rectifier's advantages and disadvantages are summarized as the following by comparing with each other:

1. **Classical UPF rectifier:**

   **Advantages:**

   - Requires only one ultrafast boost diode.
   - Needs a diode bridge had lower voltage stress.

   **Disadvantages:**

   - Has higher conduction losses.
   - Needs a free-wheeling diode parallely connected to boost inductor and boost diode to achieve the boost inductor's core resetting.

2. **Proposed UPF rectifier:**

   **Advantages:**

   - Has lower conduction losses.
   - The free-wheeling diode is not needed.

   **Disadvantages:**

   - Needs two ultrafast boost diodes.
   - Needs a diode bridge had higher voltage stress.

# CHAPTER 5

# CONTROL TECHNIQUES FOR UNITY POWER FACTOR RECTIFIERS

## 5.1 Introduction

Standard bridge rectifier followed by output capacitor result in low efficiency, higher total harmonic distortion and higher reactive power and lower active power with different output loads that can be resistive, inductive, capacitive, and switching loads such as an inverter. In order to develope interface systems that improves the power factor of standard electronic loads, and improve the quality of the currents, there are many efforts being done and various control techniques.

The boost topology shown in figure 5.1 together with power factor corrector controller is the most popular topology in PFC (power factor corrector) applications. The diode bridge rectifier is used for AC/DC conversion, and the controller operates to properly shape the input current $i_g$ with respect to its current reference. The output capacitor absorbs the input power pulsation and allows small output voltage ripple. The boost topology can operate with different control techniques allowing low distorted input current waveforms and achieve nearly unity power factor.

There are various control schemes such as peak current control, average current control, hysteresis current control, borderline control, discontinuous current PWM (pulse width modulation) control [33], [35], nonlinear carrier control (NCC), input current shaping, charge and quasi-charge control [34]. In this chapter, the most popular control techniques that are peak current control, average current control, hysteresis current control, borderline control, discontinuous current PWM control

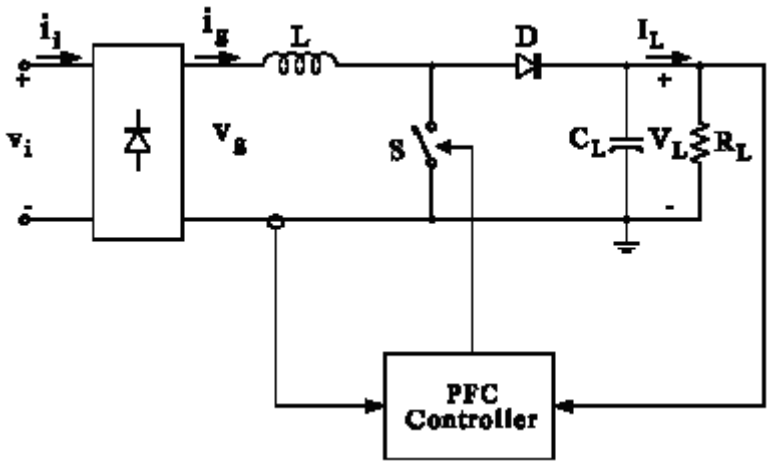


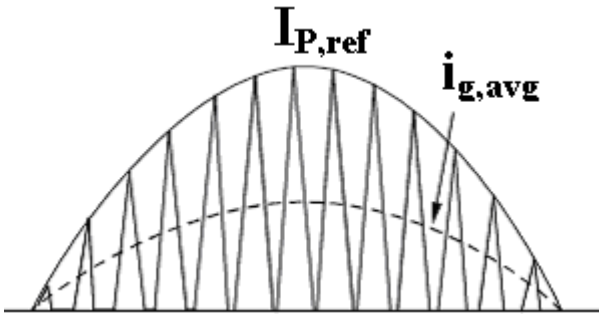

**Figure 5.1** Principle scheme of a boost PFC.

are reviewed and compared on the basis of the boost topology in order to express advantages and drawbacks of each solution.

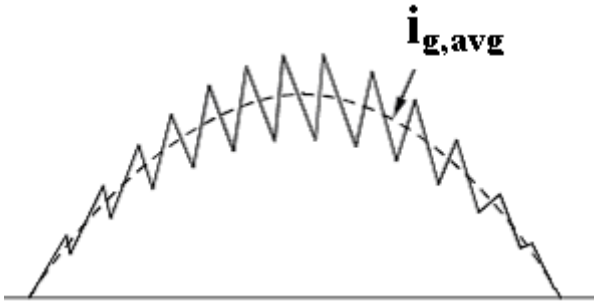
## 5.2 Popular PFC Control Techniques

Unity power factor rectifiers can be used in “Continuous Conduction Mode”, “ Discontinuous Conduction Mode”, and boundary between these conduction modes. “Continuous Conduction Mode” is used in high and middle power applications while “ Discontinuous Conduction Mode” is used in low power applications generally.

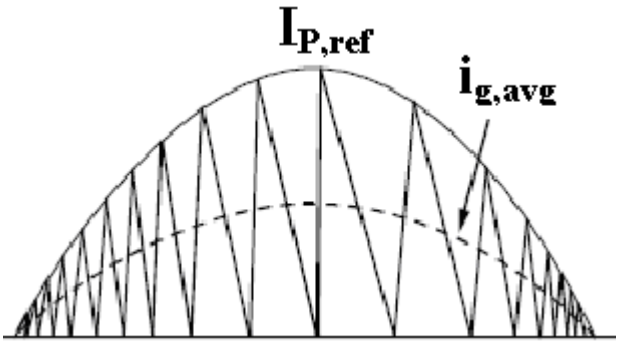
In “Discontinuous Conduction Mode”, current amplitude goes zero and stays zero then it rises. It means that the current is not continuous whereas in “Continuous Conduction Mode”, the current magnitude doesn’t reach zero. On the other hand, in “Boundary Conduction Mode”, the current amplitude goes zero but don’t stay at zero current level and it rises immediately. The current waveforms in these conduction modes are shown in figure 5.2.




**(a)** Current Waveform in “Discontinuous Conduction Mode”




**(b)** Current Waveform in “Continuous Conduction Mode”




**(c)** Current Waveform in “Boundary Conduction Mode”

**Figure 5.2** Current Waveforms in “Discontinuous Conduction Mode” , “Continuous Conduction Mode”, “Boundary Conduction Mode”.

Peak current control, average current control, hysteresis current control work in “Continuous Conduction Mode” but borderline control in “Boundary Conduction Mode”. Discontinuous current PWM control works in “Discontinuous Conduction Mode”. Their current waveforms are listed in table 5.1.

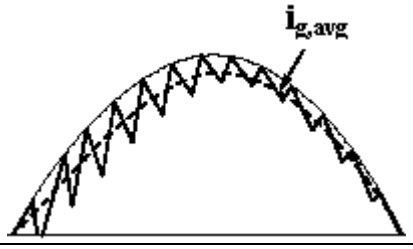
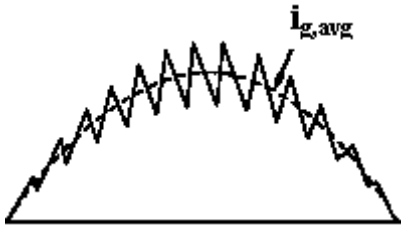
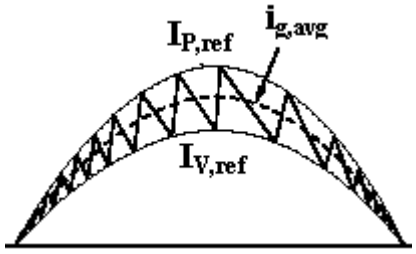
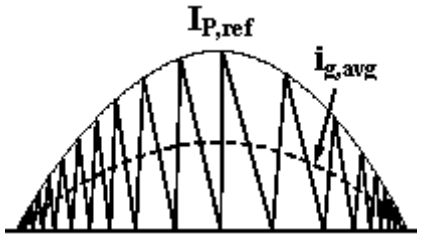
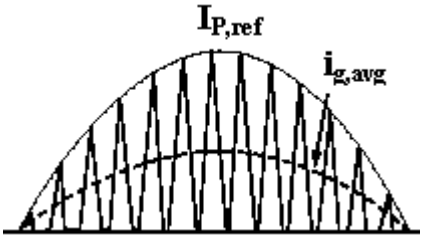
| | Current Waveform |
|---|---|
| **Peak Current Control** |  |
| **Average Current Control** |  |
| **Hysteresis Current Control** |  |
| **Borderline Current Control** |  |
| **Discontinuous Current PWM Control** |  |

**Table 5.1** Current waveforms in popular current control techniques.

These control techniques are considered here on the basis of the boost PFC (boost power factor corrector). However, these control techniques can be applied to other topologies [33], [35].

### 5.2.1 Peak Current Control

The basic peak current control scheme is shown in figure 5.2. The switch is turned on by a clock signal at the beginning of each cycle. It is turned off when the inductor current (if there is external ramp (compensating ramp), sum of the inductor current and external ramp) reaches sinusoidal current reference [33], [34], [35]. This sinusoidal current reference is generally obtained by multiplying the output of the voltage error amplifier and the scaled replica of the rectified line voltage. The voltage error amplifier sets the current reference amplitude. The current reference signal is always proportional to and synchronized with the line voltage, so unity power factor is achieved. The converter operates in continuous inductor current mode (CICM) as shown in figure 5.3. Continuous inductor current mode provides reduced devices current stress and input filter requirements [33]. The bridge diodes can be slow devices with continuous input current while the boost diode has to be fast diode.

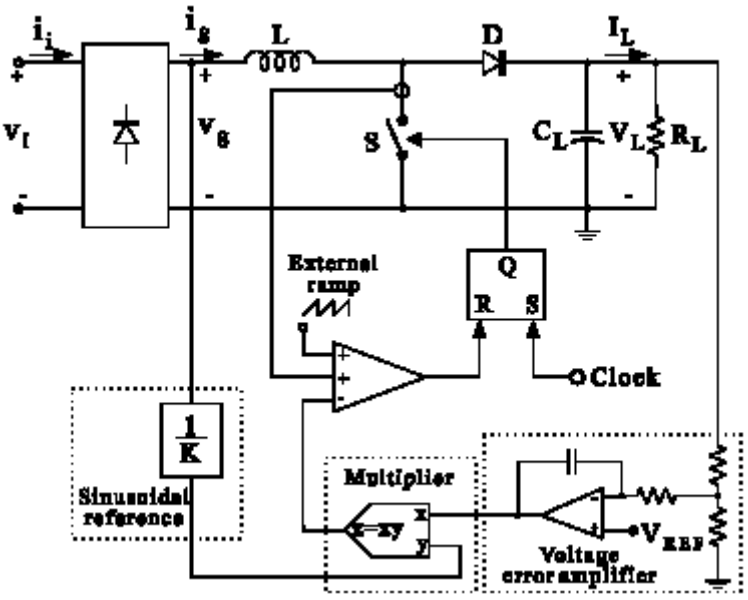



**Figure 5.3** Peak Current Control Scheme.

Advantages and disadvantages of peak current control method are listed here [33]:

**Advantages:**

- Constant switching frequency,
- Only the switch current must be sensed and this can be accomplished by a current transformer, thus avoiding the losses due to the sensing resistor,
- No need of current error amplifier and its compensation network,
- Possibility of a true switch current limiting.

**Disadvantages:**

- Presence of subharmonic oscillations at duty cycles greater than 50%, so a compensation ramp is needed,
- Input current distortion which increases at high line voltages and light load is worsened by the presence of the compensation ramp,
- Control more sensitive to commutation noises.

Changing the current reference waveshape, the input current distortion can be reduced and better input current waveform can be obtained. Also, the compensation ramp can be avoided by keeping the duty cycle below 50% if the power factor corrector is not designed for universal input operation [33].

### 5.2.2 Average Current Control

Average current control scheme shown in figure 5.4 has better input current waveform. In this control method, the inductor current is sensed and filtered by the current error amplifier. The current error amplifier's output drives a PWM (pulse width modulation) modulator. The inner current loop tends to minimize the error between the input current and the current reference [33], [35]. The current reference signal is obtained in a similar way as in the peak current control [33], [34]. The rectifier with average current control method works also in continuous inductor current mode. Hence, the same considerations done with regard to the peak current control is applicable to the average current control method [33]. The current control has the following advantages and disadvantages [33], [35]:

**Advantages:**

- Constant switching frequency,
- No need of compensation ramp,
- Control is less sensitive to commutation noises, due to current filtering,
- Better input current waveforms than for the peak current control since the duty cycle is close to one at near the zero crossing of the line voltage, so reducing the dead angle in the input current.

**Disadvantages:**

- Inductor current must be sensed,
- A current error amplifier is needed and its compensation network design must be taken into account with the different converter operating points during the line cycle.

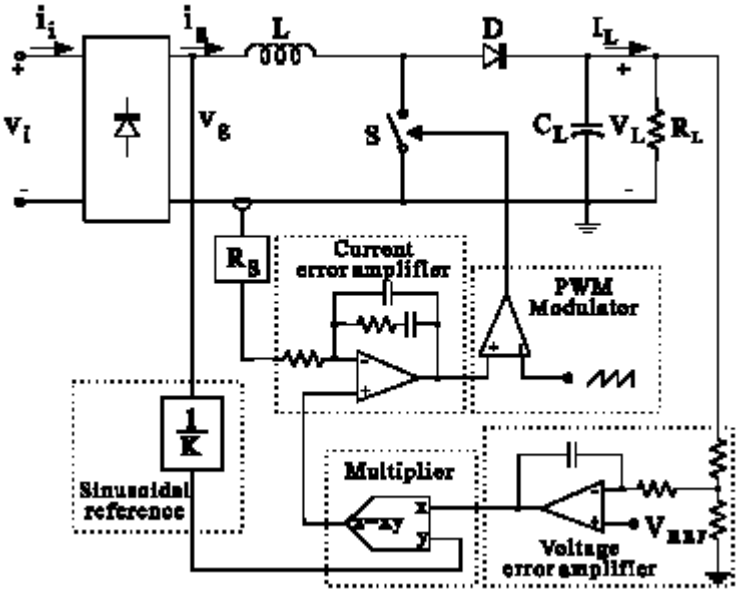



**Figure 5.4** Average Current Control Scheme.

### 5.2.3 Hysteresis Control

Hysteresis current control scheme is shown in figure 5.5. Two sinusoidal current references namely $I_{P,ref}$, which is the peak current reference for the inductor current, $I_{V,ref}$, which is the current reference for the valley of the inductor current are generated in this type of control. The switch is turned on when the inductor current goes below the lower current reference, $I_{V,ref}$ and it is turned off when the inductor current goes above the upper current reference, $I_{P,ref}$ in this control technique in which the converter also works in CCIM (Continuous Inductor Current Mode)[33].

**Advantages:**

- No need of compensation ramp,
- Low distorted input current waveforms.

**Disadvantages:**

- Variable switching frequency,
- Inductor current must be sensed,
- Control sensitive to commutation noises.

Its advantages and disadvantages [33] are given above. This current control technique has very high control stability and robustness [35].

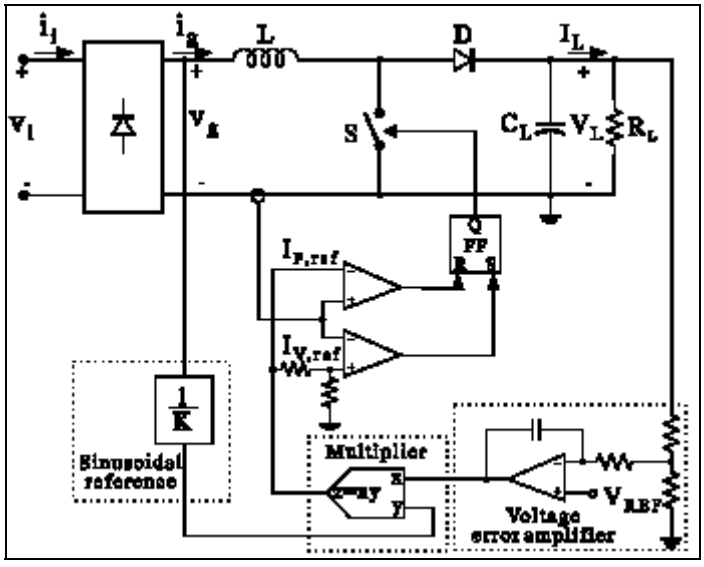



**Figure 5.5** Hysteresis Control Scheme.

### 5.2.4 Borderline Control

Borderline control scheme is shown in figure 5.6. The switch on-time is held constant during the line cycle and switch is turned on when the inductor current falls to zero. In this approach, the converter operates at the boundary between CCM ("Continuous Conduction Mode") and DCM ("Discontinuous Conduction Mode"). In this way, the boost diode is turned off softly, so there is no recovery loss of the boost diode. The switch is turned on at zero current, and this reduces the commutation losses of the switch. However, the higher current peaks increases the conduction losses and the device stresses. This may result in heavier input filters for some topologies. The instantaneous input current has triangular waveshape, whose peak is proportional to line voltage [33], [35]. In this way, the average input current of the rectifier becomes proportional to the line voltage without duty-cycle modulation. The switch current sensing can be eliminated by modulating the switch-on time with respect to the voltage error amplifier's output without using the multiplier [33].

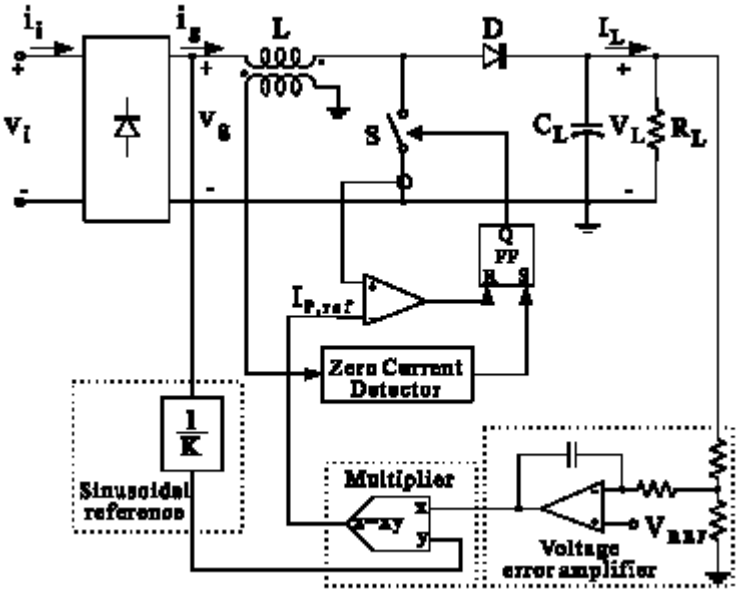



**Figure 5.6** Borderline Control Scheme.

**Advantages:**

- No need of a compensation ramp,
- No need of a current error amplifier,
- For controllers using switch current sensing, switch current limitation can be introduced.

**Disadvantages:**

- Variable switching frequency,
- Inductor's voltage must be sensed in order to detect the zeroing of its current,
- For controllers in which the switch current is sensed, control is sensitive to commutation noises [33].

### 5.2.5 Discontinuous Current PWM Control

Discontinuous current PWM control scheme is shown in figure 5.7 and it eliminates the internal current control loop to operate the switch at constant on time and switching frequency. This control technique causes some harmonic distortion in the line current with the boost PFC, but allows unity power when it is used with converter topologies like Flyback, Cuk and Sepic with the converter operating in "Discontinuous conduction mode" (DCM) [33], [35].

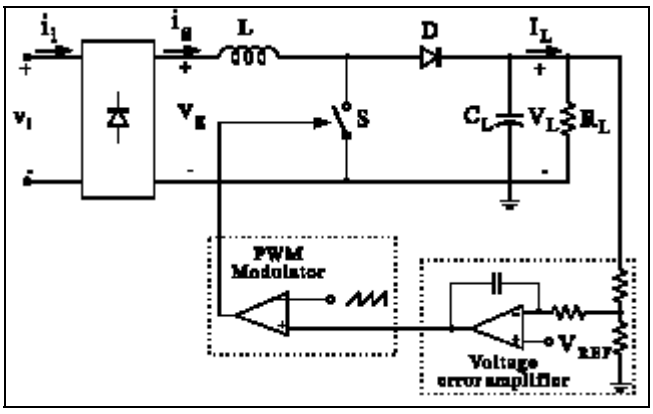



**Figure 5.7** Discontinuous current PWM control scheme.

**Advantages:**

- Constant switching frequency,
- No need of current sensing,
- Simple PWM control.

**Disadvantages:**

- Higher device current stress than for borderline control,
- Input current distortion with boost topology [33].

# CHAPTER 6

# SIMULATIONS OF PROPOSED CONVERTER AND CLASSICAL UNITY POWER FACTOR RECTIFIER

## 6.1 Introduction

Control techniques for UPF (unity power factor) rectifiers are discussed in chapter 5. Discontinuous current PWM control has high input current distortion with boost topology. Proposed converter and classical converter are boost converter topologies, so discontinuous current PWM control is not much convenient for the converter topologies. Peak current control, hysteresis control, borderline control techniques are sensitive to commutation noise. Hysteresis control and borderline control techniques have variable switching frequency, but peak current control has fixed switching frequency. However, average current control technique is less sensitive to commutation noise, has fixed switching frequency and better input current waveforms than peak current control [33]. Thus, average current control technique is chosen for the implementation of the proposed converter and classical converter's simulations. Several integrated circuits exist in the market that use average current control technique such as UC3854A/B, UC3855, TK3854A, ML4821, TDA4815, TDA4819 etc. UC3854B (UC1854B, UC2854B, and UC3854B are only different from each other in thermal characteristics) is chosen as PFC IC (Power Factor Corrector Integrated Circuit) used average current control technique.

Average current control technique, and circuit scheme and necessary calculations are given in the Unitrode application note “UC3854 Controlled Power Factor Correction Circuit Design” in Appendix A and related information about

rectifier design with UC3854B is found reference [42].

In the design procedure, the rectifiers' specifications used are as follows:

1. Pout = 3 kW
2. Output voltage = 440 V
3. Output voltage ripple = 10 %
4. Input voltage, $V_{in}$ = 220 – 15 % + 30 % V rms
5. Line frequency = 50 Hz
6. Switching frequency, $f_{sw}$ = 50 kHz
7. Maximum input current ripple, $\Delta I$ = 10 % peak to peak
8. Efficiency, $\eta \geq 95$ %
9. Input power factor, pf $\cong$ 1

In this chapter, it is decided which simulation program and the IC model in simulation program are used for the simulations made. In these simulations, inductors used are ideal inductors and snubbers for power semiconductors in the simulation circuits are not used. Afterwards, power semiconductors to be used in the rectifiers' implementation stage are selected since their parameters are used in the simulations for comparing the classical and proposed rectifier's performances here.

Then, the followings are decided through this chapter:

1. Whether the proposed rectifier can be controlled with the UC3854B IC or not is decided.
2. Do the designed proposed rectifier and classical rectifier's specifications coincide with the specifications given above via simulations made with the selected simulation software? If not, the rectifiers' circuit will be redesigned.
3. The proposed rectifier and the classical rectifier's performances are investigated at steady state and in dynamic conditions. Also, their power semiconductor stresses are investigated and compared via the simulations. It is decided whether the proposed rectifier will be implemented or not according to the results. These are the most important decision and purposes in this chapter.

The two rectifiers' performances are compared in the following ways:

1. Their performances are investigated at steady state by connecting different 3 kW loads to their outputs in each simulation. The followings are used as the 3 kW load:

- 3 kW purely resistive load
- Two different inductive resistive loads. One of them is 10 uH inductor serially connected to a resistor and the other is 100 uH inductor serially connected to the resistor.

2. The two rectifiers are simulated in dynamic conditions. One purely resistive 3 kW load is connected to the proposed rectifier's output, after a while it is disconnected and then connected again in the simulation environment. The classical unity power factor rectifier's performance in dynamic conditions is investigated similarly.

In chapter 7, whether the simulations made in this chapter and its results are correct or not is investigated by checking simulations and implementation results with 1 and 2 kW purely resistive load connected each time to proposed rectifier's output in simulation and laboratory environment.

## 6.2 Choice Of The Simulation Software And The Simulation Models

At this stage it is very important to determine which simulation medium is most suitable for the purpose here. This is very important as there will be a large number of simulations and the time taken for a simulation should be short while the accuracy is good. In this section, various alternatives for simulation shall be evaluated.

For simulation of electronic circuits, PSPICE is a common choice. This software is best if details on device level are important, but the solution time may be excessive for studying long duration behaviour of electronic circuits. The other alternatives available are MATLAB-Simulink, PSIM, a combination of PSIM and Simulink and SIMPLORER. Here, only the first 3 options are studied.

In this section, PSIM with UC3854B unity power factor IC model using discrete components, PSIM with UC3854B model already found in PSIM model library, PSIM and MATLAB-Simulink R14 with UC3854B model found in PSIM model library, MATLAB-Simulink R14 with UC3854B IC model using discrete blocks in Simulink are used for simulating the unity power factor rectifier and

compared especially for their simulation speed.

UC3854B IC model drawn using discrete components in PSIM, the same IC model already in PSIM, and the IC model drawn using discrete components in Simulink R14 are shown respectively in figure 6.1, 6.2, 6.3. Working principle of the IC is explained in section 6.4 by using classical and proposed rectifier topologies and their control circuits' block diagram given in figure 6.7 and figure 6.8. Hence, detailed description about working principle of the IC simulation models is not given in this section.

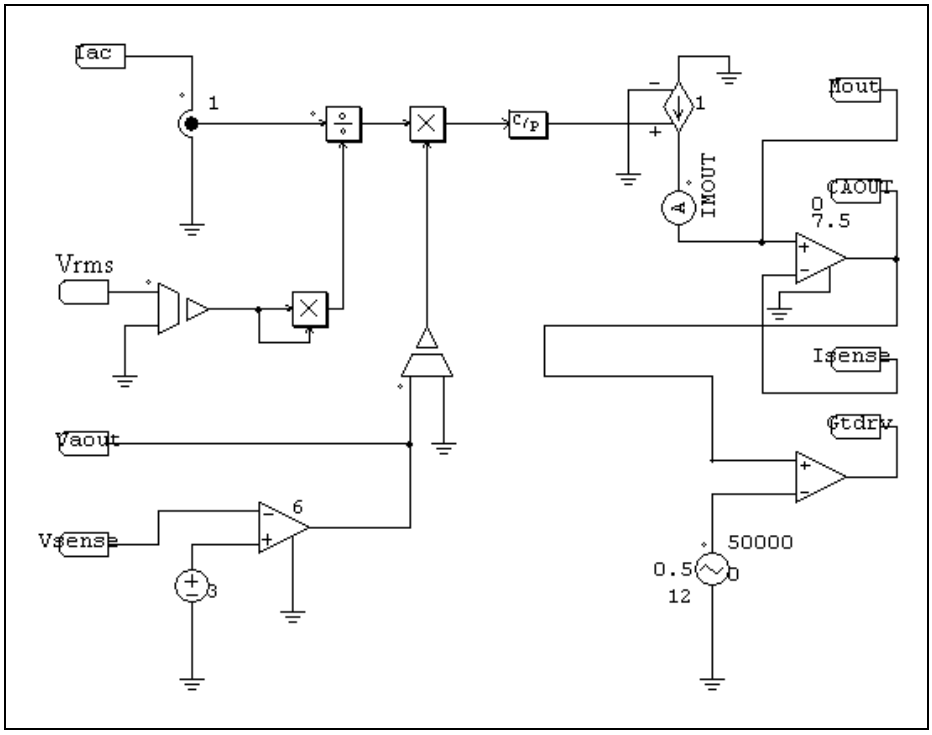



**Figure 6.1** UC3854B model created using discrete components for PSIM 6.1 simulation program.

UC3854B IC model in figure 6.2 is found already in PSIM 6.1 as stated above. In order to increase the simulation speed, this model is simplified but the model's main characteristics are maintained. In this way, the model in figure 6.1 is

obtained. The modifications are:

- PKLMT, VCC, CT, SS, RSET, ENA, VREF pins and their related circuit are removed from the model in figure 6.2 since they are unnecessary to make simulations at steady state and the simulations made in this chapter.
- Setting of the PWM signal frequency, which is the switching frequency, $f_{sw}$ is achieved by using CT, RSET, their related circuits and an extra circuit in UC3854B model in figure 6.2 while it is achieved via "triangle voltage source" whose frequency is at the switching frequency.

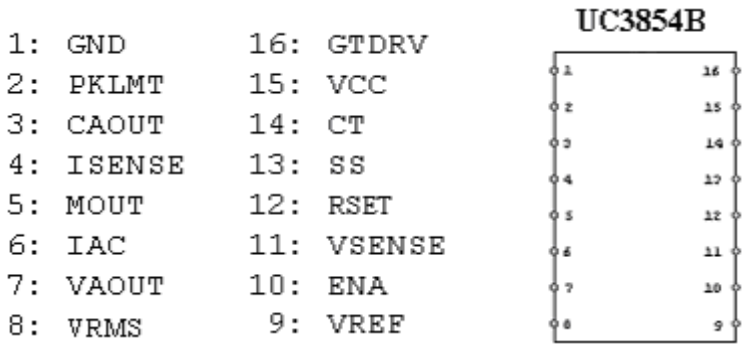



**Figure 6.2** UC3854B model in PSIM.

The IC model in figure 6.3 is similar to the one in figure 6.1, Simulink R14 has no opamp and comparator model, so subtract and PID blocks are used instead of the opamps and the comparator in figure 6.1. The "triangle voltage source" in figure 6.1 is replaced by "repeating sequence" in figure 6.3 since the "repeating sequence" in Simulink R14 is the counterpart of "triangle source" in PSIM 6.1. On the other hand, the model in figure 6.1 and the one in figure 6.3 have same functions and they are sufficient to study the performance of the proposed and classical unity power factor rectifier.

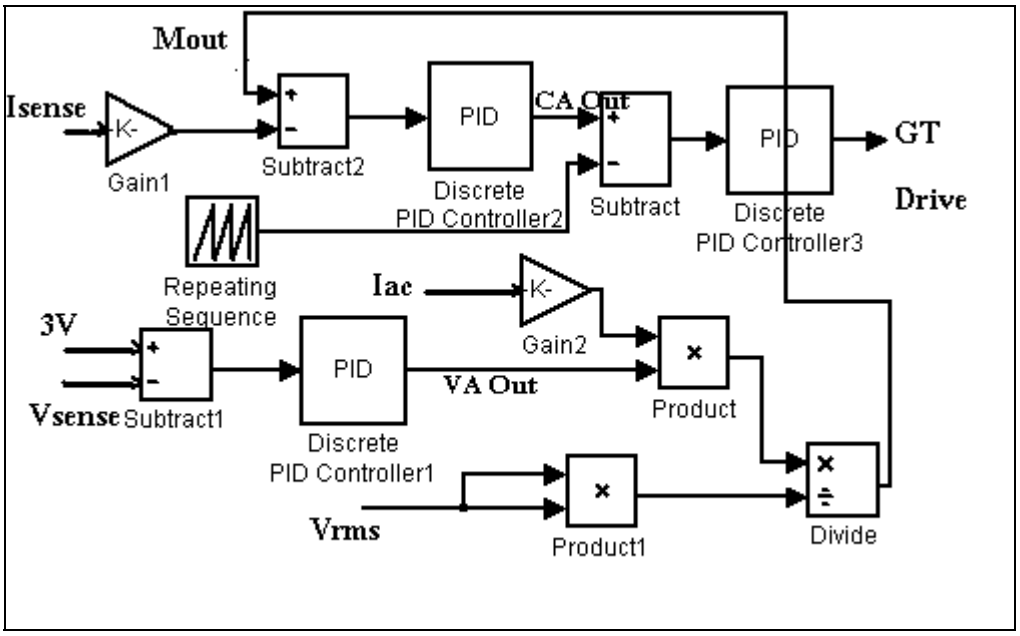



**Figure 6.3** UC3854B model drawn using discrete blocks in Simulink R14.

In figure 6.1, 6.2 and 6.3; VSENSE, IAC, VAOUT, VRMS, MULTOUT, ISENSE, CAOUT, GTDRIVE are the UC3854B's pins and detailed descriptions are given in its datasheet in Appendix B.

In order to compare the PSIM and Simulink simulation programs, classical unity power factor rectifier shown in figure 6.7 is simulated by using International Rectifier IRGP50B60PD IGBT and ST BYT30PI800 power diode's parameters at steady state. The IGBT and diode are chosen arbitrarily to use their parameters in simulations to compare their speed. The diode block forward voltage drop parameter is taken as 1.9 V; it is the voltage drop over ST BYT30PI800 power diode in conduction. Snubber resistance parameter in the diode block used in the simulations is taken as 500 kΩ in Simulink. The diode block's other parameters are not altered. In PSIM simulation, only the IRGP50B60PD and BYT30PI800 power semiconductor's forward voltage drop parameter is used since current fall time, rise time, tail time for the IGBT and transit time for the diodes can not be entered in PSIM's IGBT and diode model. The rest of the block parameters are taken as the default values.

The rectifier is simulated by using MATLAB-Simulink, PSIM 6.1 simulation programs, PSIM 6.1 and MATLAB-Simulink R14 co-simulation with 3 kW purely

resistive load at steady state.

In PSIM and MATLAB-Simulink co-simulation, the UC3854B model in figure 6.1 is used in PSIM, but diode and IGBT blocks are used in Simulink. Simulink's accelerator mode is used for increasing the simulation speed. In the co-simulation, Simulink doesn't permit the use of fixed step solver in Simulink side due to IGBT block used in it. According to PSIM user manual, in co-simulation, fixed step solver should be used to obtain correct results, otherwise zero-order-hold blocks must be placed at the Simcoupler model block's input, and it is what is done in the simulation. Fixed step size is used and the time step is taken as 1E-07 s in PSIM side while variable step size is used in Simulink side.

In MATLAB-Simulink simulation, simulation is done in the accelerator mode and the UC3854B in figure 6.3 is used. Variable step size is used in the simulation.

Two simulations are made with the PSIM simulation program. The UC3854B IC model in figure 6.1 is used in one simulation while the model in figure 6.2 is used in the other one. Also, the time step is taken as 1E-07 s and fixed step size is used for the two simulations since only fixed step size can be used in PSIM simulation program.

The simulations' results are given in table 6.1 and table 6.2. The results of the simulations made by using PSIM 6.1 with the UC3854B IC model in figure 6.1 and figure 6.2 are given in table 6.1 while table 6.2 shows the results of simulations made with MATLAB-Simulink R14, PSIM and MATLAB co-simulation. The simulations of PSIM 6.1 with the UC3854B IC model in figure 6.1 and figure 6.2, MATLAB-Simulink R14 with the IC model in figure 6.3 gives similar results. On the other hand, the PSIM and MATLAB co-simulation predicts the IGBT and boost diode's power loss extremely higher than the others, so this simulation result is relatively unrealistic compared to the others.

The simulations are made by using a computer, which has 256 MB RAM and Pentium 4 1.7 GHz CPU. Investigating table 6.1, fastest simulation speed is achieved using the PSIM 6.1 with UC3854B IC model in figure 6.1. Hence, PSIM 6.1 with this IC model is used for the rectifiers' simulation due to its highest speed in the rest of this chapter.

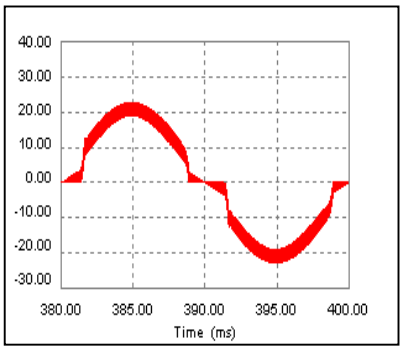
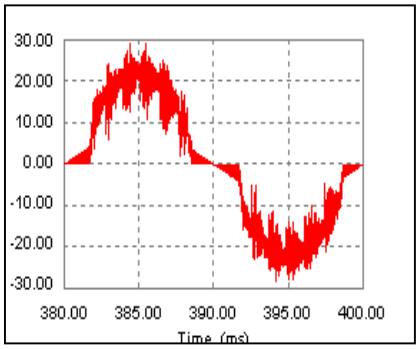
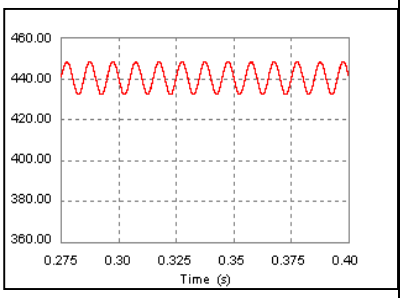
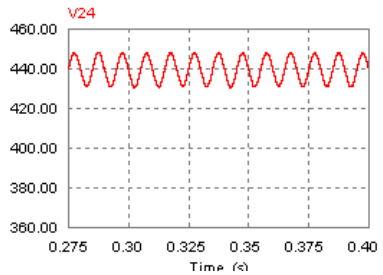
| | PSIM (with UC3854B model in figure 6.1) | PSIM (with UC3854B model in figure 6.2) |
|---|---|---|
| **Input power** | 3118 VA | 3175 VA |
| **Input power factor** | 0.9866 | 0.96605 |
| **Output power** | 3004.77 watt | 2992.57 watt |
| **Input current** | 22.68 A peak, 19.05 A peak, 11.88 A (average) | 29.25 A peak, 10.75 A peak, 11.57 A (average) |
| **Input current waveform** |  |  |
| **Output voltage** | 432.28 V -448.14 V | 430.88 V -447.75 V |
| **Output voltage waveform** |  |  |
| **D1 power loss** | 11.3178 watt | 10.55152 watt |
| **D2 power loss** | 11.3178 watt | 11.46776 watt |
| **D3 power loss** | 11.3178 watt | 10.55056 watt |
| **D4 power loss** | 11.3178 watt | 1146672 watt |
| **Boost diode power loss** | 12.9899 watt | 12.92504 watt |
| **IGBT power loss** | 10.1791 watt | 9.6094 watt |
| **Step size** | 1.00E-07 | 1.00E-07 |
| **Solution time** | 0.5 s | 0.5 s |
| **Total simulation time** | 9.5 minute | 19 minute |

**Table 6.1** Results of classical unity power factor rectifier's simulation made by using PSIM 6.1 with the UC3854B IC model in figure 6.1, figure 6.2 at steady state with 3 kW purely resistive load and comparison of the simulations' speed.

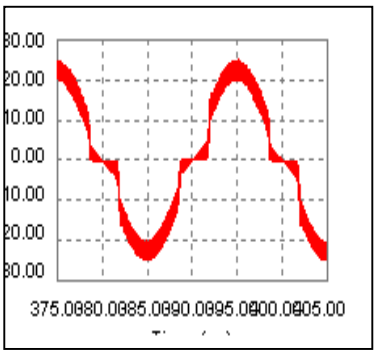
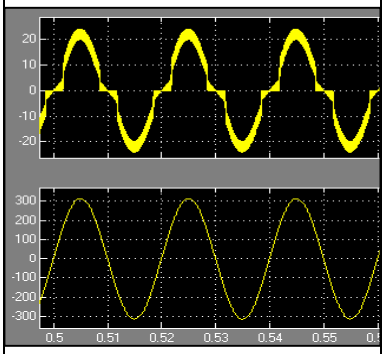
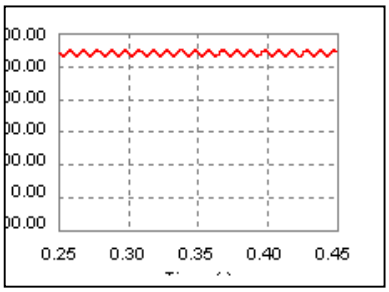
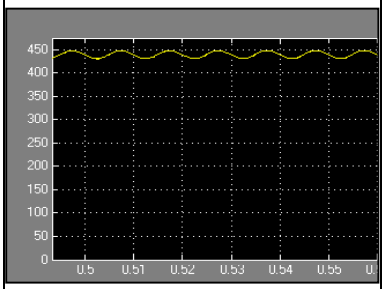
| | PSIM MATLAB co-simulation (with UC3854B model in figure 6.1) | MATLAB (with UC3854B model in figure 6.3) |
|---|---|---|
| **Input power** | 3300 VA | 3122.6 VA |
| **Input power factor** | 0.98927 | 0.9898 |
| **Output power** | 3022.46 watt | 3000 watt |
| **Input current** | 25 A peak, 20.10 A peak, 13.5 A (average) | 23.9 A peak, 19.95 A peak |
| **Input current waveform** |  |  |
| **Output voltage** | 432.97 V-450.23 V | 431.0 V-448.7 V |
| **Output voltage waveform** |  |  |
| **D1 power loss** | 11.9809 watt | 11.165 watt |
| **D2 power loss** | 11.9823 watt | 11.165 watt |
| **D3 power loss** | 11.9708 watt | 11.165 watt |
| **D4 power loss** | 11.9808 watt | 11.165 watt |
| **Boost diode power loss** | 85.714 watt | 13.115 watt |
| **IGBT power loss** | 100.09 watt | 11.95 watt |
| **Step size** | Step size in PSIM = 1e-7<br>Step size in Matlab = auto<br>Blocks' step size in Matlab = 5e-7 | Step size in Matlab = auto<br>Blocks' step size in Matlab=5e-7 |
| **Solution time** | 0.5 s | 0.5 s |
| **Total simulation time** | 45 minute | 2.5-3 hour |

**Table 6.2** Results of classical unity power factor rectifier's simulation made by using MATLAB-Simulink R14, PSIM 6.1 and Simulink co-simulation at steady state with 3 kW purely resistive load and comparison of the simulations' speed.

## 6.3 Component Selection

The classical unity power factor rectifier and proposed rectifier are simulated using PSIM 6.1 simulation program with the UC3854B IC model in figure 6.1 and simulation results are given in the following sections. In order to use IGBT and diode parameters in these simulations, International Rectifier, Fairchild Semiconductor, ON Semiconductor, IXYS' IGBTs and diodes are compared.

ON Semiconductor company doesn't have IGBT whose absolute maximum voltage stress is 600 V or higher. Consequently there is no ON Semiconductor IGBT in table C.1 in Appendix C to compare. The IGBT in the rectifier in this project is hard switched at 50 kHz, so the selected IGBT have to be capable of operating at least at 50 kHz hard switching operation. Also, the rectifier should give 3000 W output power and its input current can be as much as 28 A while mains supply permissible minimum voltage is 187 Vrms. The rectifier's average output voltage is 440 V. There is an output capacitor rated 450 V nominal, 500 V maximum at its output side. These prevents voltage between the IGBT's collector and emitter terminal to exceed 500 V; so an IGBT whose absolute maximum voltage stress is 600 V and it is enough in these rectifier circuits. While maximum permissible current in the rectifier circuit is 28 A, the transistor current rating should be higher than 28 A due to possible failure or unknown spikes in the circuit. Figure 6.4 shows that maximum voltage seen between the IGBT's collector and emitter terminal is 450 volts, and its collector current is 28 A. Its current rating should be nearly 1.5 times its maximum collector current due to mentioned reasons, then it is 42 A. IXSH30N60B2D1 and IRG4PC50UD has higher fall time than the other IGBTs in the table C.1 in Appendix C. Comparing IRGP50B60PD, IRGP50B60PD1 and IRG4PC50W-ND; IRGP50B60PD has highest price, IRGP4PC50W-ND has highest saturation voltage drop, fall time and rise time but the lowest price. HGTG20N60A4D has lowest rise time and fall time than the other IGBTs except IRGP50B60PD1 and it has lowest price than the others in table C.1 in Appendix C, so HGTG20N60A4D IGBT is selected to use in the design and the unity power factor rectifier implementation.

Ultrafast diode selection is next issue. In order to determine the ultrafast

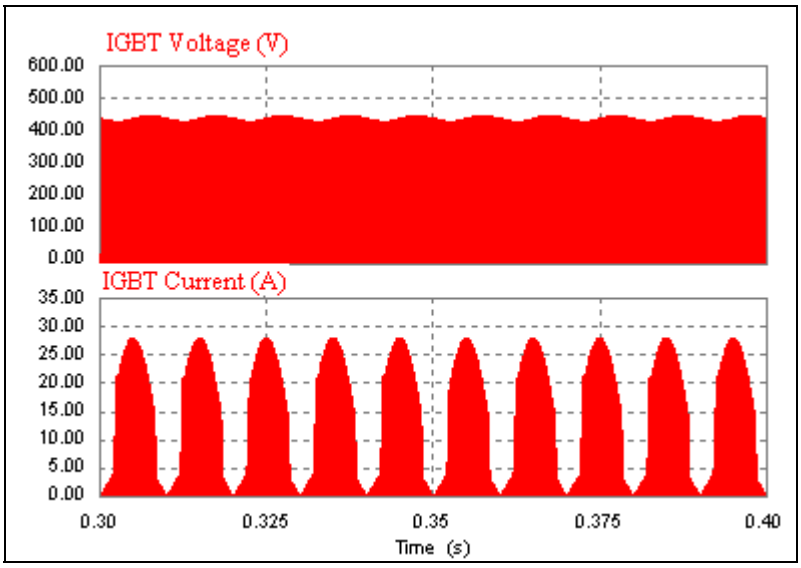



**Figure 6.4** IGBT's voltage and current waveform while input voltage is 187 V rms.

diode's parameters, one should know that UC3854B PFC IC can operate up to 95 % duty cycle. The PFC boost stage diode's current and voltage waveform are shown in figure 6.5. Also, the voltage and current waveform are given between 395 and 395.5 ms in figure 6.6 to show the waveforms in detail.

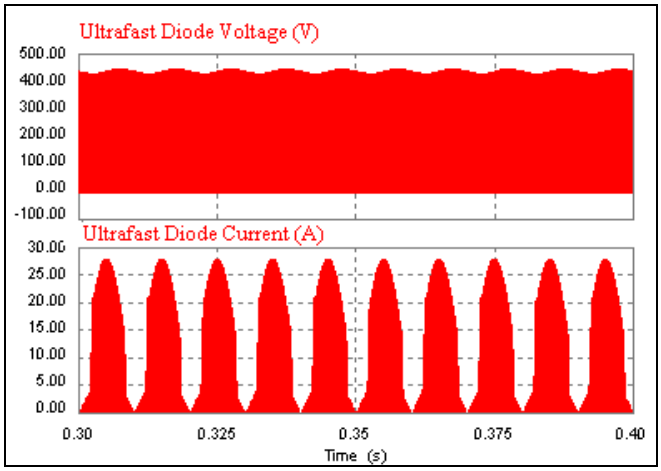



**Figure 6.5** Ultrafast diode current and voltage waveform when $V_{in}$ is equal to 187 V rms.

The current waveform in figure 6.5 is PWM waveform drawing a nearly rectified sinusoidal waveform boundary. The current waveform has 28A maximum value when mains supply's voltage is 187 Vrms. Due to the maximum 95 % duty cycle, the ultrafast diode's current rating should be determined using the sinusoidal waveform boundary.

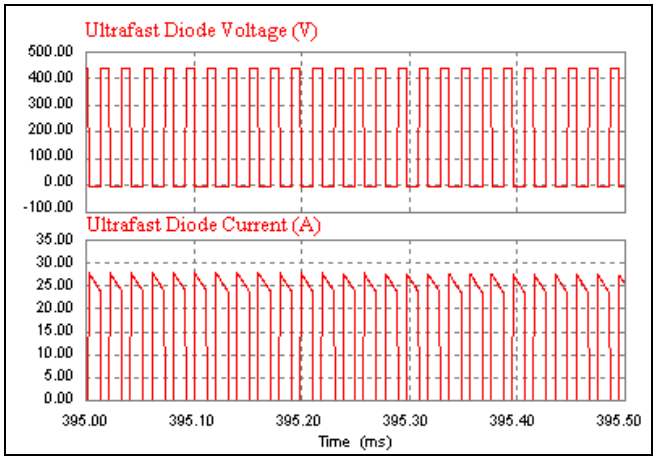



**Figure 6.6** Figure 6.5's zoomed version.

The ultrafast diodes' average rectified forward current ratings are given in table C.2 in Appendix C. Average value of a sinusoidal waveform is equal to peak value of a sine wave multiplied by $2/\pi$. The rectified sinusoidal current waveform with 28 A maximum value in figure 6.5 has nearly 17.83 A average value. At least 1.5 times the value should be selected to prevent possible spikes or unknown failures and it is 26.7 A. Ultrafast diode with 30 A current rating will be proper for the PFC application.

International Rectifier, Fairchild Semiconductor, ON Semiconductor, IXYS' ultrafast diodes are compared and ultrafast diodes whose voltage and current rating match the criteria in table 6.3 is listed in table 6.4. ISL9R3060P2, 30EPH06, DSEP30-06A/B diodes are faster than the other diodes in table C.2 in Appendix C while RURP3060 is the cheapest ultrafast diode in this table. Properties of some

ultrafast diode models are listed in table 6.4, and there is not so much difference based on their selection criteria, so cheapest one, namely RURP3060 is selected.

| Heat Sink Temp | Current Waveform Boundary (Continuous) | Turn On Voltage | Reverse Blocking Voltage | Operating Frequency | Transit Time |
|---|---|---|---|---|---|
| 80 Celsius | 28 A | Between 1 V and 2.2 V | 600 V | 50 kHz | less than 1 us |

**Table 6.3** Ultrafast Diode Selection Criteria.

| Model | Turn on Voltage | Transit Time | USD Price (Each/1000) |
|---|---|---|---|
| **RURP3060** | $I_F$=30 A T=25 $^0$C 1.5 V max, T=150 $^0$C 1.3V max | $I_F$=1A $dI_F/dt$=100A/us 55 ns max, $I_F$=30A $dI_F/dt$=100A/us 60 ns max | 1.11384 |
| **DSEP30-06A/B/BR** | Version A 1.25 V ($I_F$=30 A T=25 $^0$C 1.6 V max, T=150 $^0$C 1.25 V max), Version B 1.56 V ($I_F$=30 A T=25 $^0$C 2.51 V max, T=150 $^0$C 1.56 V max) | $I_F$=1 A, di/dt=100A/us, $V_R$=30 V, $T_{VJ}$=25 $^0$C Version A 35 ns max, Version B 30 ns max | 1.68 |
| **ISL9R3060P2** | 2.4 V ($I_F$=30 A T=25 $^0$C 2.1 V typical 2.4 V max, T=125 $^0$C 1.7 V typical 2.1 V max) | 35 ns ($I_F$=30 A T=25 $^0$C 36ns typical 110 ns max) | 1.581 |
| **30EPH06** | 2.1 V ($I_F$=30 A, T=25 $^0$C 2.0 V typical, 2.6 V max); $I_F$=30 A, T=150 $^0$C 1.34 V typical 1.75V max) | 40 ns (T=25 $^0$C $I_F$=30 A, trr=31 ns typical; T=125 $^0$C $I_F$=30 A, trr=77 ns typical) | 1.3427 |

**Table 6.4** Ultrafast diode selection table.

Similar to the IGBT and ultrafast diode selection, International Rectifier, Fairchild Semiconductor, ON Semiconductor, IXYS bridge diodes are investigated to identify bridge diode's parameters to use in the simulations. International Rectifier, Fairchild Semiconductor, ON Semiconductor don't produce bridge diodes as discrete

diodes. Also, IXYS company generally does not produce bridge diodes as discrete diodes except some bridge diodes. Bridge diodes have to be discrete diodes to measure the diode's power loss one by one if necessary. Proper discrete diodes for our rectifier is shown in table 6.5. DSI30-08A has higher non-repetitive peak surge current, $I_{FSM}$, than DSI30-08AC and the rest of their parameters are nearly same, and their prices are same. Hence DSI30-08A diode is selected for the simulations.

| Diode Code | VRRM Max (V) | Io (rectified) Max (A) | IFSM Max (A) | VFM Max (V) | Price | Comment |
|---|---|---|---|---|---|---|
| **DSI30-08AC** | 800 | 30 | 210 | 1.45 V ($I_F$=45 A, T=25 $^0$C) | 2.9095 $ (Future electronics e-store) | Proper for rectifier bridge |
| **DSI30-08A** | 800 | 30 | 300 | less than 1.45 V ($I_F$=45 A, T=25 $^0$C) | 2.9095 $ (Future electronics e-store) | Proper for rectifier bridge |

**Table 6.5** Bridge diode selection table.

## 6.4 Proposed and Classical Unity Power Factor Rectifiers' Comparison Via Simulations

In this section, performances of the proposed rectifier and classical unity power factor rectifier, which are designed according to the specifications given in section 6.1 are investigated and compared at steady state and in dynamic conditions via simulations as stated before in the section. These simulations are made by using PSIM 6.1 simulation program and UC3854B IC model in figure 6.1 since the simulation program with the IC model in figure 6.1 has the highest simulation speed and enough accuracy as mentioned before in section 6.2. In these simulations, the rectifiers' mains supply is 50 Hz, 220 V rms sinusoidal single phase mains supply.

The proposed rectifier and classical unity power factor rectifier are simulated, their performance is compared on the basis of efficiency, input power factor, input

current ripple, input current's THD, output voltage ripple, output voltage stability, etc. The investigation is done at steady state and their steady state input current, voltage waveform and output voltage waveform are given in the following sections by using:

1. A 3 kW purely resistive load.
2. Two 3 kW inductive resistive loads. These loads are used for understanding whether the rectifiers can maintain their unity power factor operation with different inductive loads. One of the loads has 100 uH inductor serially connected to a resistor and the other 10 uH. The range is chosen large enough to observe the effect of the inductor size.

One purely resistive 3 kW load is connected to the proposed and classical rectifier's output, after a while it is disconnected and then connected again in the simulation environment. In this way, their behaviour, especially their output voltage's settling time, in dynamic conditions are investigated.

PSIM 6.1 simulation program's time step is taken as 1E-7 s between 0 and 1 s in simulation time at their steady state analysis. After that, the time step is decreased to 1E-8 s between 1s and 1050 ms to increase the simulations' accuracy although the 1E-7 s time step is enough for the analysis. On the other hand, the simulation program's time step is taken as only 1E-7 s in the rectifiers' dynamic analysis with the simulations.

In these simulations, no snubbers for the IGBT and the diodes are used while the implemented circuit has R-C and overvoltage snubbers for the IGBT as mentioned in chapter 7. Also, the inductors used in these simulations are ideal inductors.

The selected power semiconductors are given in section 6.3. Only their conduction voltage drop parameters are used in these simulations since the PSIM 6.1 simulation program permits to use only the parameters in the simulations.

The classical unity power rectifier topology and its operation are explained in section 4.3. This simulated rectifier and its control circuit's block diagram is given in figure 6.7. The boost inductor, $L_S$, the output capacitor, $C_{out}$ and their calculated values according to the specifications given in section 6.1 are also shown in this figure.

In this block diagram, low pass filter is necessary to filter the harmonics in

the line voltage. $I_{ac}$ signal is a current signal, which represents the mains supply voltage in its circuit. It is proportional to the mains supply and taken over the diode bridge. The proportionality is shown with K2 block and a 650 kΩ resistor is used instead of the K2 block in the simulation environment. Its shape is a rectified sinusoidal one. $V_{rms}$ is the voltage sample over the diode bridge and it is taken by using the low pass filter. Also, its shape is rectified sinusoidal one. This extra circuitry ($V_{rms}$ and DIVIDER SQUARER part of AXB/$C^2$ MULTIPLIER DIVIDER SQUARER circuitry in figure 6.7) is needed to keep the rectifier's power constant irrespective of the input voltage changes. $I_{ac}$ signal is multiplied by the voltage controller's output signal and divided by the square of $V_{rms}$ signal. When the voltage controller's output signal is constant, and the mains supply's voltage is halved, $I_{ac}$ and $V_{rms}$ signal is halved. Half of the $I_{ac}$ signal times one fourth of $V_{rms}$ signal gives two times the original $I_{multout}$ current. Although the mains supply's voltage is halved and mains supply's current is duplicated, the rectifier's power is kept constant in this way.

The diode bridge's current is sensed and K1 block represents the ratio between the sensed current and the current, $I_{sense}$ in the control circuit block diagram. The ratio is taken as 0.04 in the simulations made through the following sections. The current, $I_{sense}$ is subtracted from the $I_{multout}$ current, it is processed by current controller and the current controller's output forces the PWM block to produce correct duty cycle and fixed frequency PWM so that the mains supply's voltage and current is in phase. Sinusoidal voltage and current in phase denote unity power factor system. Hence, irrespective of whether the load is resistive, capacitive or inductive, mains supply experiences resistive load. In the block diagram and in the simulation environment, $V_{sense}$ voltage is taken by using a voltage divider which consists of the resistors, RVI and RVD. The voltage is subtracted from the reference voltage (reference voltage is 3V in UC3854B), this error voltage is given to the voltage controller, it is multiplied by $I_{ac}$ signal and divided by the square of the $V_{rms}$ signal. This means that when the voltage error signal is decreased, $I_{multout}$ signal becomes lower, so the PWM signal's duty cycle given to the IGBT's gate is decreased. When the voltage error signal is high, duty cycle of the PWM signal becomes higher in the same way. This forces the output voltage, $V_{out}$ to be higher. In this way, the output voltage is kept constant and proportional to the reference voltage in the block

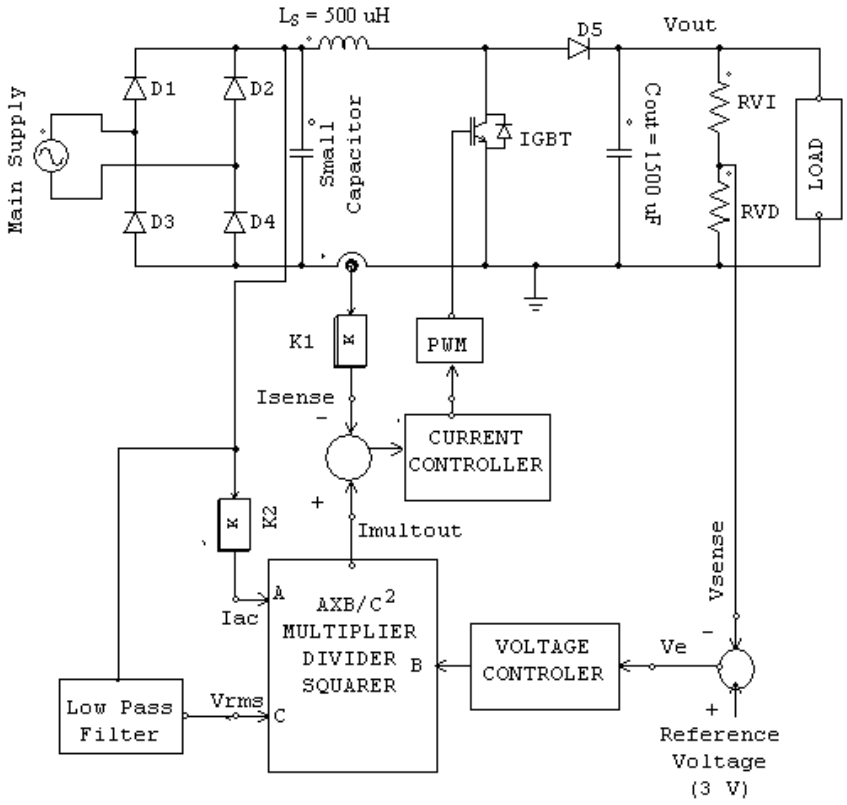



**Figure 6.7** Classical unity power factor rectifier and its control circuit's block diagram.

diagram. The current controller, voltage controller are actually current error amplifier and voltage error amplifier respectively. Their detailed descriptions are given in Appendix A and reference [42].

The proposed single phase, single switch unity power factor rectifier topology's working principle is illustrated and explained in detail in section 4.2. The rectifier topology and its control block diagram are shown altogether in figure 6.8. The boost inductors, L1 and L2, the output capacitor, $C_{out}$ and also, their calculated values according to the specifications given in section 6.1 are shown in figure 6.8. The output capacitor's capacitance is equal to the one in figure 6.7 and the inductors, L1 and L2's total inductance are same with the boost inductance, $L_S$. These should be emphasized.

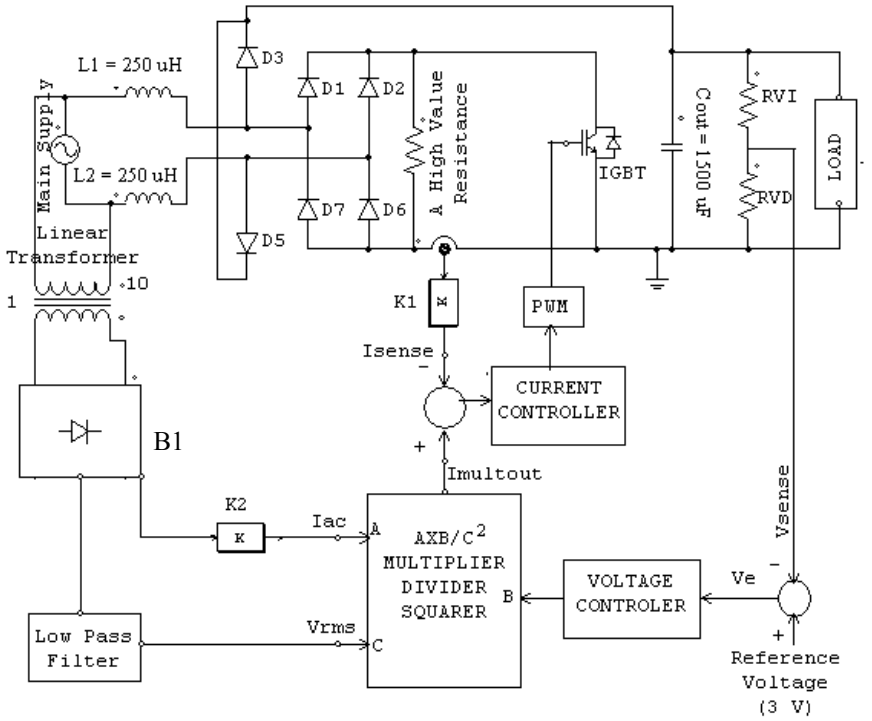



**Figure 6.8** Proposed rectifier topology and its control block diagram.

With respect to the control system, the only difference between in figure 6.7 and figure 6.8 is where $I_{ac}$ and $V_{rms}$ signals are taken to the controller. D1, D2, D6 and D7 form a diode bridge. The signals can not be taken from this diode bridge 's output side since boost inductors, L1 and L2 are connected between mains supply and this diode bridge in figure 6.8, and the $I_{ac}$ signal waveshape have to be rectified sinusoidal one in the suggested rectifier circuit as in the classical unity power factor rectifier circuit. The $I_{ac}$ and $V_{rms}$ signals are taken from a 10:1 transformer connected to the mains supply as in figure 6.8 for the suggested rectifier. In this topology, there should be a low pass filter to reduce the harmonics, which are due to the transistor switching and possible harmonics on the mains supply too. The low pass filter circuit design for classical unity power factor rectifier with the PFC IC is given in detail in Appendix A. However, resistance and capacitance values in the low pass filter circuit and K2's value in the classical unity power factor rectifier and the proposed rectifier are different. Their values are given in section 7.2.4.

The rest of the UPF controller design in Appendix A and reference [42] is

applicable to this configuration and its control circuitry. "AXB/$C^2$ MULTIPLIER DIVIDER SQUARER", the voltage controller, current controller, K1 and PWM blocks in figure 6.8 are equal to the ones in figure 6.7. In order to inhibit the diodes, D1, D2, D6, D7's switching losses, a high value resistance such as 500 kohm is connected parallel to them as in figure 6.8. Its value should be high enough to minimize the $I^2R$ losses over the resistance and low enough to keep the diodes in conduction.

The classical unity power factor rectifier's $I_{ac}$ and $V_{rms}$ signals can be taken by using a transformer and a diode bridge like B1 as in figure 6.8, and the same low pass filter in figure 6.8 can be used in the classical unity power factor rectifier as in the proposed rectifier when UC3854B IC is used. The classical unity power factor rectifier is simulated with PSIM 6.1 simulation program and UC3854B IC model in figure 6.1 with 3 kW purely resistive load at steady state to observe the classical unity power factor rectifier's performance by taking $I_{ac}$ and $V_{rms}$ signals via a 10:1 transformer and a diode bridge like B1 as in figure 6.8. The simulation program's time step is taken same as the two rectifier's simulations at steady state with 3 kW loads mentioned before in this section. This simulation results are given briefly in section 6.4.3.

### 6.4.1 Classical And Proposed UPF Rectifier Simulation With 3 kW Purely Resistive Load And Their Performance Comparison

Classical unity power factor rectifier and proposed rectifier, whose block diagrams are given in figure 6.7 and figure 6.8 respectively are simulated by using PSIM 6.1 simulation program and the UC3854B IC model in figure 6.1 with 3 kW purely resistive load at steady state in this section. In this way, whether the two rectifiers, especially proposed rectifier can be controlled with this IC will be understood. Then, the two rectifiers' performances will be compared considering upon their efficiency, input power factor, THD (Total Harmonic Distortion), input current ripple, output voltage ripple, IGBT and diodes' stresses and losses, etc.

### 6.4.1.1 Classical UPF Rectifier Simulation With 3 kW Purely Resistive Load

The classical unity power factor rectifier with 3 kW purely resistive load is simulated. 64.5 ohm resistor is connected to the output of the unity power factor rectifier whose block diagram is displayed in figure 6.7 as the 3 kW load.

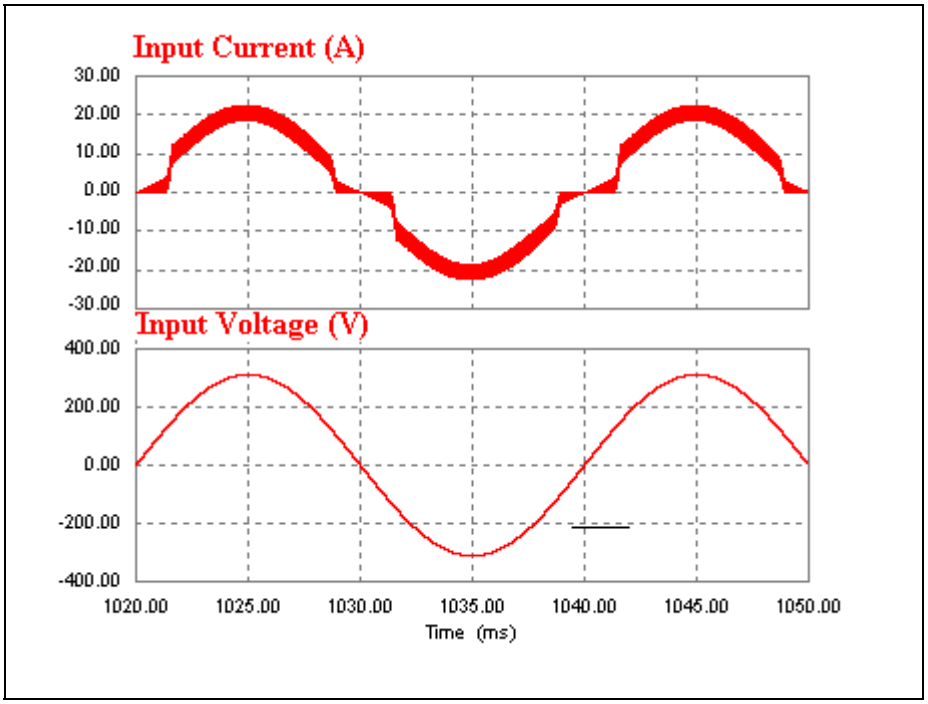



**Figure 6.9** Classical unity power rectifier's input voltage and current waveform with 3 kW purely resistive load at steady state.

The rectifier's input current and output voltage waveforms are shown respectively in figure 6.9 and 6.10 respectively. The input current is in phase with the input voltage, so this rectifier with the 3 kW purely resistive load achieves unity power factor operation. The output voltage in figure 6.10 swings between 432.26 and 448.1 V. Hence, 3.6 % output voltage ripple is obtained while the rectifier is designed for maximum 10 % output voltage ripple. On the other hand, the rectifier's

mean output voltage stays constant at steady state and this means that the output voltage is stable. Its output power obtained from the figure 6.10 for the given load is 3006 W. The peak input current's magnitude changes between 22.46 A and 18.77 A. This means that the rectifier's input current ripple is 8.95 % peak to peak. It is lower than the given input current ripple specification, which is 10 % peak to peak in section 6.1.

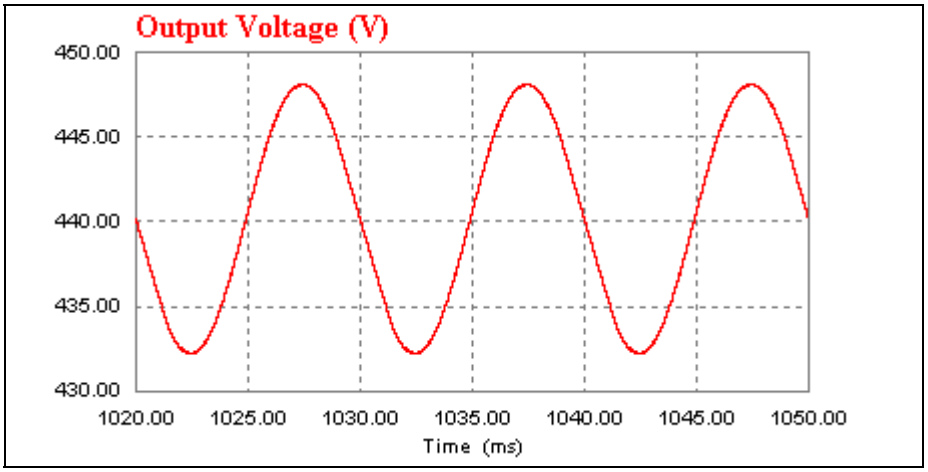



**Figure 6.10** Classical unity power rectifier's output voltage waveform with 3 kW purely resistive load at steady state.

Power viewed from the mains line connected to the rectifier's input is shown in figure D.1(a) and its power factor is displayed in figure D.1(b) in Appendix D.1.1. Figures D.2, D.3, D.4, D.5, D.6 in Appendix D.1.1 show its input current FFT waveform and THD, IGBT's current, voltage waveform, one of the bridge diode, namely D1's current, voltage waveform and the boost diode, D5's current and voltage waveform respectively.

The power loss of the IGBT in figure 6.7 is calculated by using equation 6.1. In this equation, $T$, $V_{CE}$, $i_C$ are the mains supply's voltage period, the IGBT's voltage between its collector and emitter terminals, and its collector current

respectively.

$$Powerloss = \frac{1}{T}\int_{t=t_1}^{t=t_1+T}(V_{CE}\cdot i_C)dt \tag{6.1}$$

Power losses of the power diodes shown in figure 6.7 are also calculated by using equation 6.1, but the voltage between their anode and cathode is used instead of the voltage, $V_{CE}$ .

The rectifier's efficiency, input power factor, THD of its input current, input current ripple, output voltage ripple and the IGBT, boost diode, D5, bridge diodes, D1, D2, D3, D4's voltage and current stresses, and their power losses are given in table 6.6. Its input current's harmonics up to $50^{th}$ harmonic is listed in the part related with the classical UPF rectifier in table 6.7.

#### 6.4.1.2 Proposed Converter's Simulation With 3 kW Purely Resistive Load

Proposed rectifier is simulated to compare its performance with the classical unity power factor rectifier when the 3 kW purely resistive load, specifically 64.5 resistor, is connected to their output at steady state.

In order to calculate the proposed rectifier's input current ripple, its input current waveform with input voltage waveform is shown in figure 6.11. According to this figure, input peak current changes between 19.07 and 22.74 A, this means that input current ripple is 8.78 %. Figure 6.12 shows the rectifier's output voltage at steady state and it swings between 448.24 and 432.16 V. The rectifier's mean output voltage is 440.20 V. Hence, the output voltage ripple is nearly 3.65 %. On the other hand, its mean output voltage stays constant. This means that its output voltage is stable at steady state. The rectifier's output power is calculated using wattmeter block in PSIM 6.1 and it is 3006.32 watts. According to the figure 6.11 and 6.12, unity power factor operation at its input side and DC voltage at its output side are achieved and the output voltage ripple and input current ripple are lower than the related specifications given in section 6.1. This means that the proposed rectifier can be controlled by using UC3854B IC.

The proposed rectifier's input power and power factor graph is given in figure

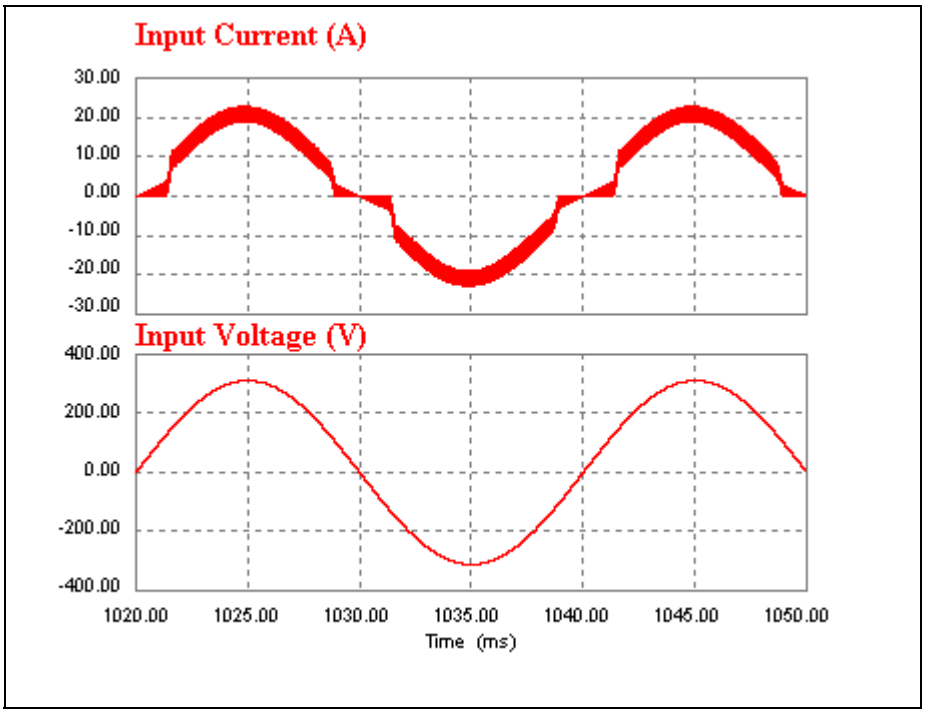



**Figure 6.11** Proposed rectifier's input voltage and current waveform with 3 kW purely resistive load at steady state.

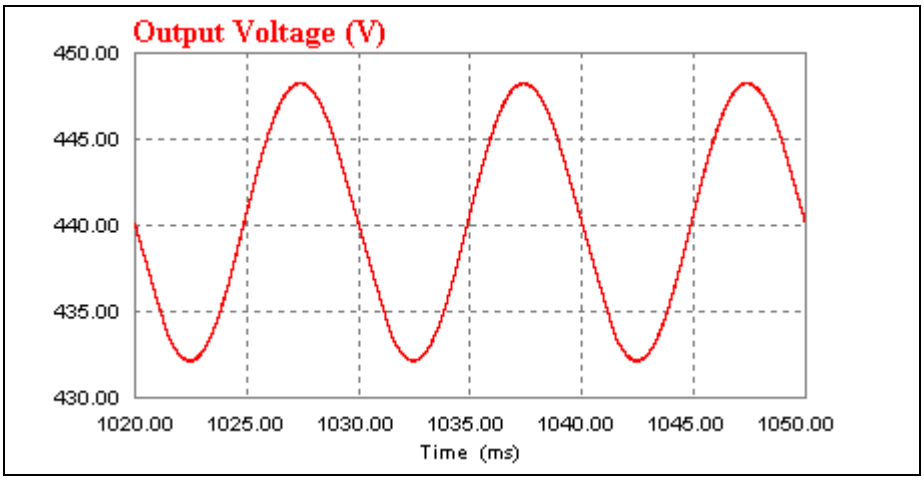



**Figure 6.12** Proposed rectifier's output voltage waveform with 3 kW purely resistive load at steady state.

D.7(a) and D.7(b) in Appendix D.2. Its input current's FFT waveform and THD, IGBT's current and voltage waveform, one of the boost diodes, D3's current and voltage waveform are given in figure D.8, D.9, D.10, D.11 in Appendix D.2 respectively. The bridge diodes, D1 and D7's current and voltage waveforms are given in figure D.12 and D.13 in the same part in Appendix D.

The rectifier's efficiency, input power factor, THD of its input current, input current ripple, output voltage ripple and the IGBT, boost diodes, D3 and D5, bridge diodes, D1, D2, D6, D7's voltage and current stresses, and their power losses are given in the part related with the proposed rectifier in table 6.6. Its input current's harmonics up to $50^{th}$ harmonic is listed in the part related with the classical UPF rectifier in table 6.7.

#### 6.4.1.3 Evaluation Of Simulation Results Of Classical And Proposed UPF Rectifier With 3 kW Purely Resistive Load

The classical UPF rectifier and proposed rectifier's efficiency, input power factor, input current's THD, input current ripple, output voltage ripple, IGBT and power diodes' stresses and their power losses are obtained via the simulations with the 3 kW purely resistive load at steady state and are listed in table 6.6.

Proposed rectifier's efficiency and input current ripple are better than the classical unity power factor rectifier's ones according to the data in table 6.6 while classical unity power factor rectifier's input power factor, input current's THD, output voltage ripple are better than the proposed rectifier's ones. The diode bridge consisting the diodes, D1, D2, D6, D7 in the proposed rectifier has lower power losses than the classical unity power factor rectifier's diode bridge. This is main reason of why the proposed rectifier's efficiency higher than the classical UPF rectifier's one.

Voltage and current stresses of the IGBT and boost diodes in proposed rectifiers are nearly the same as in the classical UPF rectifier while the diode bridge in proposed rectifier has higher voltage stresses than the one in classical UPF rectifier.

| | Classical UPF Rectifier With 3 kW Purely Resistive Load | Proposed UPF Rectifier With 3 kW Purely Resistive Load |
|---|---|---|
| **Efficiency (%)** | 97.29 | 97.45 |
| **Input Power Factor** | 0.9873 | 0.9864 |
| **THD (%)** | 16.06 | 16.59 |
| **Input Current Ripple (%)** | 8.95 | 8.78 |
| **Output Voltage Ripple (%)** | 3.6 | 3.65 |
| **IGBT Stress** | 449.42 V, 22.46 A | 448.71 V, 22.74 A |
| **Boost Diode Stress** | 446.1 V, 22.46 A | 445.27 V, 22.74 A |
| **Bridge Diodes' Stresses** | 309.87 V, 22.26 A | 449.73 V, 22.74 A for D1, D2<br>449.57 V, 22.74 A for D6, D7 |
| **IGBT's Power Loss** | 10.04 W | 9.88 W |
| **Boost Diodes' Power Loss** | 8.89 W | 8.90 W |
| **Diode Bridge's Power Loss** | 25.28 W | 2.6 W for each D1, D2<br>6.28 W for each D6, D7<br>(Total 17.76 W) |

**Table 6.6** Performance comparison table between proposed rectifier and classical unity power factor rectifier with 3 kW purely resistive load (simulated).

The proposed rectifier and classical unity power factor rectifier's input current harmonics up to 50$^{th}$ harmonic are obtained by using the FFT waveforms in figure D.2 and figure D.8 in Appendix D.1 and they are listed in table 6.7. The two rectifiers' input current harmonics have similar magnitudes and don't have even harmonics.

THD (Total Harmonic Distortion) in their input current can be calculated by using equation 6.1 for the first 50 harmonics in table 6.7.

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \tag{6.1}$$

, where $I_h$ is rms value of h$^{th}$ harmonic and h is an integer, and $I_1$ is fundamental current component in rms [39]. In this way, THDs of the classical unity power factor rectifier and proposed rectifier's input currents are calculated as 14.12 % and 14.76 % respectively. On the other hand, the THD values in table 6.6 are higher than the THD calculated by considering the first 50 harmonics as expected. This indicates that

| | Classical UPF Rectifier | Proposed UPF Rectifier | | Classical UPF Rectifier | Proposed UPF Rectifier |
|---|---|---|---|---|---|
| **Harmonic #** | **Magnitude (A)** | **Magnitude (A)** | **Harmonic #** | **Magnitude (A)** | **Magnitude (A)** |
| **1** | 19.60 | 19.56 | **26** | 0.00 | 0.00 |
| **2** | 0.00 | 0.00 | **27** | 0.11 | 0.10 |
| **3** | 1.75 | 2.08 | **28** | 0.00 | 0.00 |
| **4** | 0.00 | 0.00 | **29** | 0.20 | 0.19 |
| **5** | 1.46 | 1.40 | **30** | 0.00 | 0.00 |
| **6** | 0.00 | 0.00 | **31** | 0.17 | 0.15 |
| **7** | 1.16 | 1.06 | **32** | 0.00 | 0.00 |
| **8** | 0.00 | 0.00 | **33** | 0.05 | 0.05 |
| **9** | 0.55 | 0.48 | **34** | 0.00 | 0.00 |
| **10** | 0.00 | 0.00 | **35** | 0.10 | 0.10 |
| **11** | 0.12 | 0.12 | **36** | 0.00 | 0.00 |
| **12** | 0.00 | 0.00 | **37** | 0.15 | 0.14 |
| **13** | 0.44 | 0.41 | **38** | 0.00 | 0.00 |
| **14** | 0.00 | 0.00 | **39** | 0.10 | 0.10 |
| **15** | 0.47 | 0.42 | **40** | 0.00 | 0.00 |
| **16** | 0.00 | 0.00 | **41** | 0.03 | 0.03 |
| **17** | 0.23 | 0.20 | **42** | 0.00 | 0.00 |
| **18** | 0.00 | 0.00 | **43** | 0.09 | 0.08 |
| **19** | 0.12 | 0.12 | **44** | 0.00 | 0.00 |
| **20** | 0.00 | 0.00 | **45** | 0.10 | 0.10 |
| **21** | 0.29 | 0.27 | **46** | 0.00 | 0.00 |
| **22** | 0.00 | 0.00 | **47** | 0.06 | 0.06 |
| **23** | 0.28 | 0.25 | **48** | 0.00 | 0.00 |
| **24** | 0.00 | 0.00 | **49** | 0.03 | 0.03 |
| **25** | 0.11 | 0.10 | **50** | 0.00 | 0.00 |
| THD (considering first 50 harmonics) = 14.12 % for classical UPF rectifier | | | THD (considering first 50 harmonics) = 14.76 % for proposed UPF rectifier | | |
| THD (all harmonics) = 16.06 % for classical UPF rectifier | | | THD (all harmonics) = 16.59 % for proposed UPF rectifier | | |

**Table 6.7** Proposed and classical UPF rectifier's input current harmonics' number and magnitudes up to $50^{th}$ harmonic with 3 kW purely resitive load at steady state.

most of the distortion is due to the first 50 harmonics. As discussed in section 7.4, the harmonics around the carrier frequency are the main contributors to THD from the remaining harmonics.

The proposed rectifier is implemented and it is tested with 1 kW and 2 kW purely resistive loads and it is simulated with these loads. Its simulation and measured results are given in section 7.4.1 and 7.4.2. Also, it is simulated with 300 W and 600 W purely resistive loads by using the simulation circuit with the conditions mentioned in section 7.4, but this simulation results are not given in detail

in this thesis. The proposed rectifier's efficiency, its input current's THD and input power factor graphs are drawn by combining these results with the results given in the related part of table 6.6.

The followings are observed from the figure 6.13, 6.14 and 6.15:

1. The simulated and measured input power factor, THD and the simulated efficiency become better as the load is increased to its nominal value, which is 3 kW.
2. $I^2R$ losses in the implemented circuit and the non-ideal boost inductors used in the circuit increase and the measured efficiency is decreased as the load increases according to the measurements with 1 kW and 2 kW purely resistive load. However, it is expected that the measured efficiency will decrease as its load is decreased to such values of 600 W, 300 W or more as the efficiency graph obtained via simulations and shown in figure 6.13.

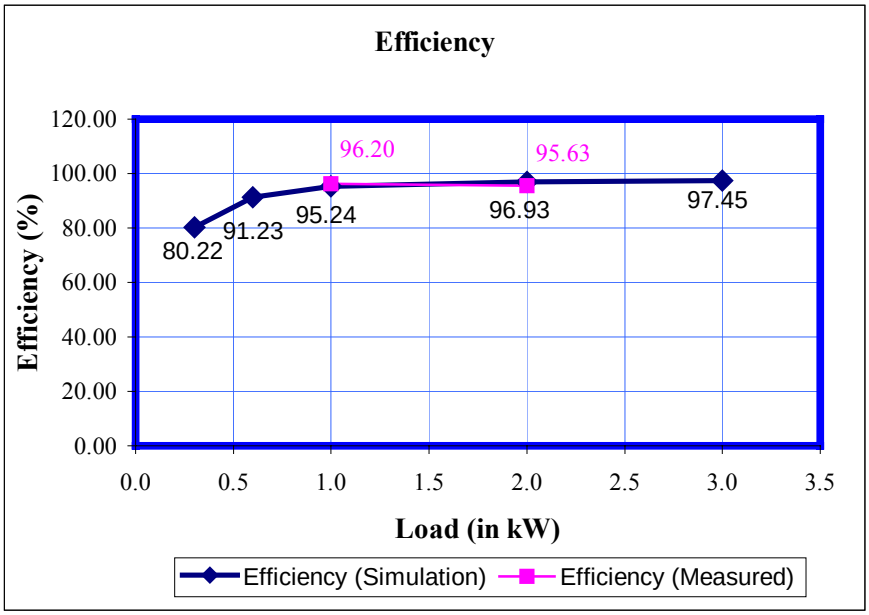



**Figure 6.13** Proposed rectifier's efficiency graphs obtained with measurements in laboratory and simulation with different purely resistive loads at steady state.

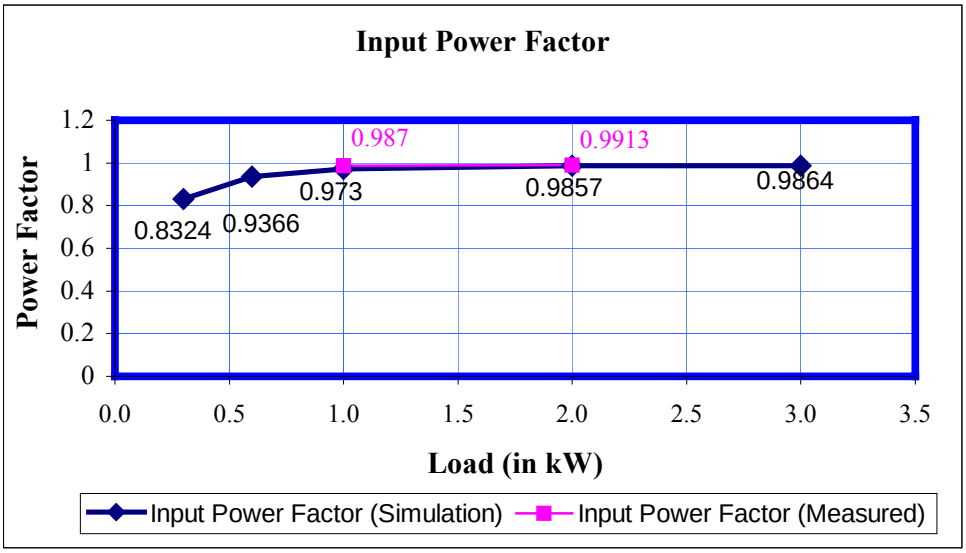



**Figure 6.14** Proposed rectifier's input power factor graphs obtained with measurements in laboratory and simulation with different purely resistive loads at steady state.

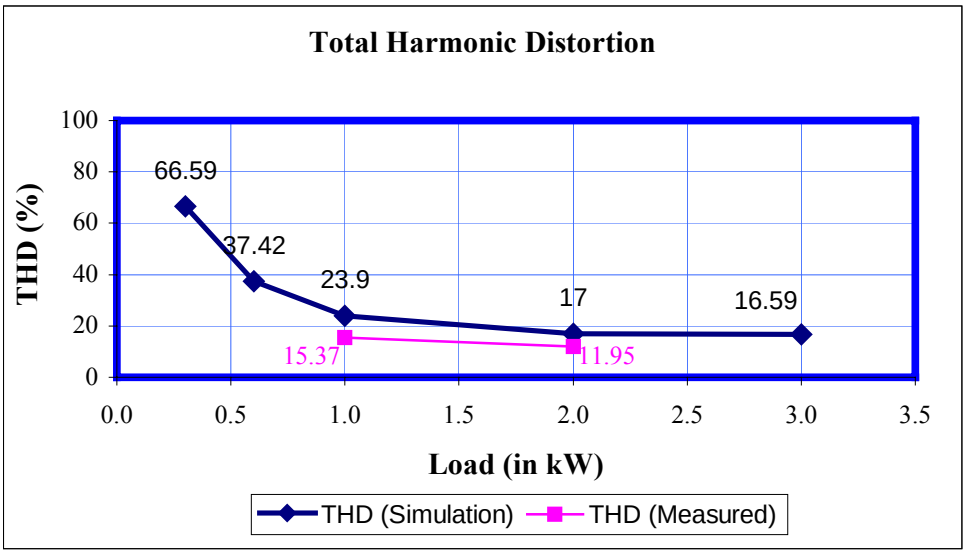



**Figure 6.15** THD graphs of proposed rectifier's input current obtained with measurements in laboratory and simulation with different purely resistive loads at steady state.

Also, the proposed rectifier is re-simulated with 1 kW and 2 kW purely resistive loads at steady state by using the simulation circuit with the conditions mentioned in section 7.4 and connecting the 36 mΩ measured winding resistance serially to boost inductors, L1 and L2 in this simulation circuit. Its input power and output power are 1048.31 VA, 996.88 W with 1 kW purely resistive load and 2091.03 VA, 2023.78 W with 2 kW purely resistive load respectively, and its output voltage is nearly 435 V with 219.2 V rms input voltage according to these simulations. The efficiency is calculated as 95.09 % with 1 kW purely resistive load and 96.78 % with 2 kW purely resistive load with the boost inductor resistance included in the simulations. These efficiency values are less than the corresponding efficiency values in figure 6.13. Note that the switching losses of power semiconductors in proposed rectifier are not included in these simulations.

HGTG20N60A4D IGBT's total switching energy loss graph vs. its gate resistance is given in its datasheet in Appendix B. 6 Ω gate resistance is used in implemented proposed rectifier. According to this graph, the IGBT's switching loss for one switching is nearly 0.35 mJ when its collector to emitter current is 10 A and the voltage difference between its collector and emitter is 390 V. The simulation circuit's average input current and output voltage are 4.3 A, 435 V with 1 kW purely resistive load and 8.56 A, 435 V with 2 kW purely resistive load respectively. It is assumed that the switching loss is directly proportional to the current magnitude and voltage magnitude. The IGBT's switching losses are calculated as 8.4 W with 1 kW purely resistive load and 16.9 W with 2 kW purely resistive load by using the current and voltage values and the total switching energy loss graph at steady state. The simulation circuit's efficiency will be 94.34 % with 1 kW purely resistive load and 96.01 % with 2 kW purely resistive load at steady state by including the IGBT's switching losses.

It can be observed that the losses of the converter are predicted somewhat higher but still the difference between the measurements and predictions is very small, and is about 1.5 %.

### 6.4.2 Classical UPF Rectifier And Proposed Rectifier's Simulation With 3 kW Inductive-Resistive Load And Their Performance Comparison

Classical unity power factor rectifier and proposed rectifier, whose block diagrams are given in figure 6.7 and figure 6.8 respectively are tested via simulations to understand whether they lose their unity power factor operation with inductive-resistive loads or not. Two different 3 kW inductive-resistive loads are used in the simulations made in this section to verify this. One of them is 100 uH inductor, whose inductance is big enough to check the unity power factor operation, serially connected to a 64.5 Ω resistor, the other is 10 uH inductor serially connected to a 64.5 Ω resistor. Also, their performances considering upon their efficiency, input power factor, THD (Total Harmonic Distortion), input current ripple, output voltage ripple, IGBT and diodes' stresses and losses are investigated with these inductive loads at steady state by making the simulations. PSIM 6.1 simulation program and the UC3854B IC model in figure 6.1 are used in this section as the previous section.

#### 6.4.2.1 Classical Unity Power Factor Rectifier's Simulation With Inductive-Resistive Load

In this section, only the classical unity power factor rectifier with the 3 kW inductive-resistive loads are simulated and its performances are investigated with the simulations made.

##### 6.4.2.1.1 Classical Unity Power Factor Rectifier's Simulation With Inductive-Resistive Load (100uH)

Aim of the simulations is here to observe the classical unity power factor rectifier’s output voltage ripple, input current ripple, efficiency and input power

factor and input current's THD (Total Harmonic Distortion) with a inductive-resistive 3 kW load which has 100 uH ideal inductor serially connected to a 64.5 Ω resistor at steady state.

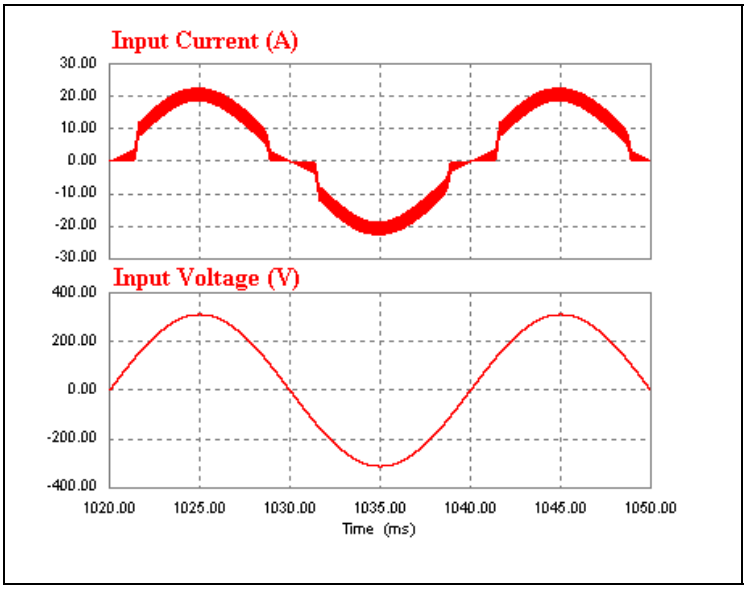



**Figure 6.16** Classical unity power rectifier's input voltage and current waveform with 3 kW inductive-resistive load (100 uH) at steady state.

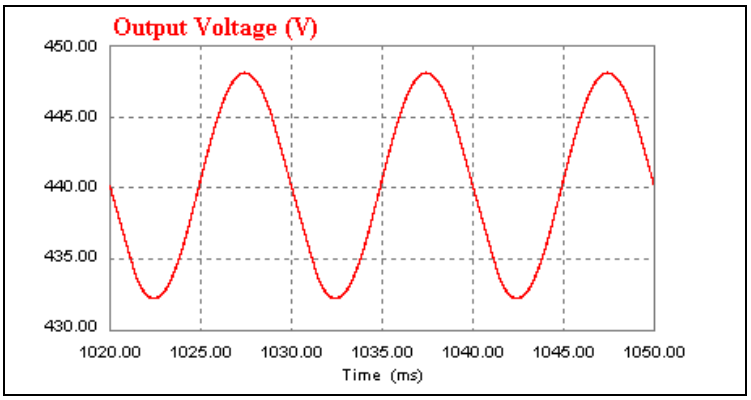



**Figure 6.17** Classical unity power rectifier's output voltage waveform with 3 kW inductive-resistive load (100 uH) at steady state.

The rectifier's input current and voltage together are given in figure 6.16. The figure shows that input voltage and current are almost in phase. Its input current ripple is obtained by finding the peak input current's magnitude from this figure. It is 8.95 % peak to peak since the input current changes between 22.46 and 18.82 A. The rectifier's output voltage swings between 432.26 and 448.1 volts, so the output voltage ripple is 3.6 %. On the other hand, its mean output voltage stays constant. This means that the output voltage is stable. The rectifier's input current ripple and output voltage ripple is less than the ones in the specifications given in section 6.1 with this load. Also, unity power factor operation is maintained with this inductive-resistive load.

Power viewed from the mains line connected to the rectifier's input is shown in figure D.14(a) and its power factor is displayed in figure D.14(b) in Appendix D.1.1. Figures D.15, D.16, D.17, D.18, D.19 in Appendix D.1.1 show its input current's FFT waveform and THD, IGBT's current, voltage waveform, one of the bridge diode, namely D1's current, voltage waveform and the boost diode, D5's current, voltage waveform respectively.

The rectifier's efficiency, input power factor, THD of its input current, input current ripple, output voltage ripple and the IGBT, boost diode, D5, bridge diodes, D1, D2, D3, D4's voltage and current stresses, and their power losses are given in the related part of table 6.8. Its input current's harmonics up to $50^{th}$ harmonic is listed in the part related with the classical UPF rectifier in table 6.9.

#### 6.4.2.1.2 Classical Unity Power Factor Rectifier's Simulation With Inductive-Resistive Load (10uH)

UPF rectifiers should not change their behaviors as much as possible whether the load is inductive, capacitive or purely resistive. In section 6.4.2.1.1, the classical unity power factor rectifier is simulated with 100 uH inductor serially connected to 64.5 Ω resistor. In this section, our goal is to study whether THD, input current and output voltage ripple, etc. change or not at steady state when the rectifier's load is changed with 10 uH inductor serially connected to 64.5 Ω resistor.

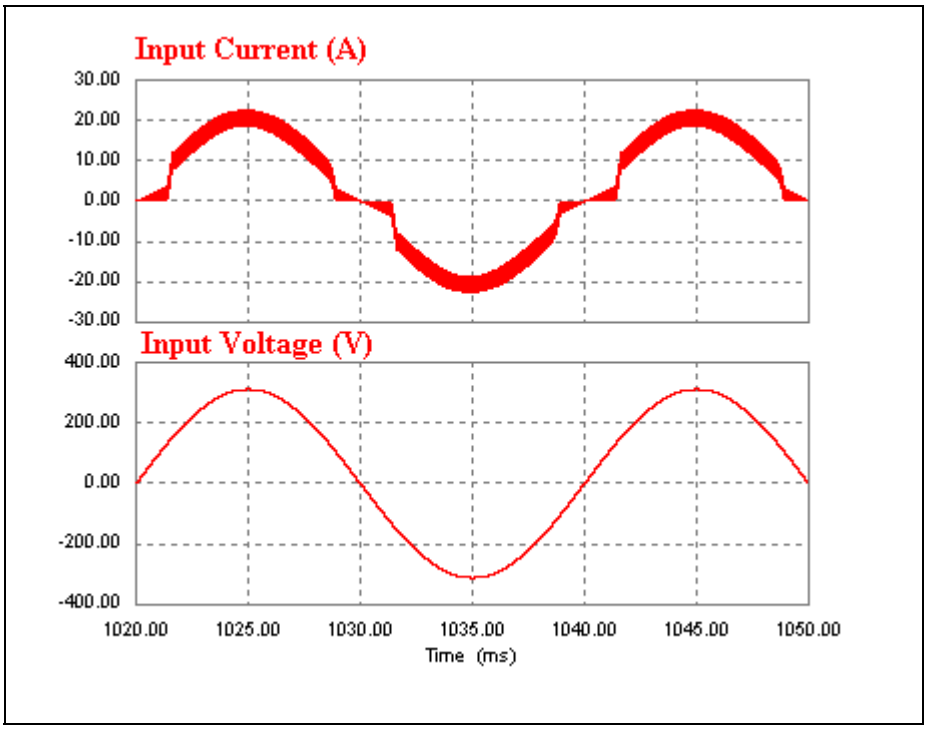



**Figure 6.18** Classical unity power rectifier's input voltage and current waveform with 3 kW inductive-resistive load (10 uH) at steady state.

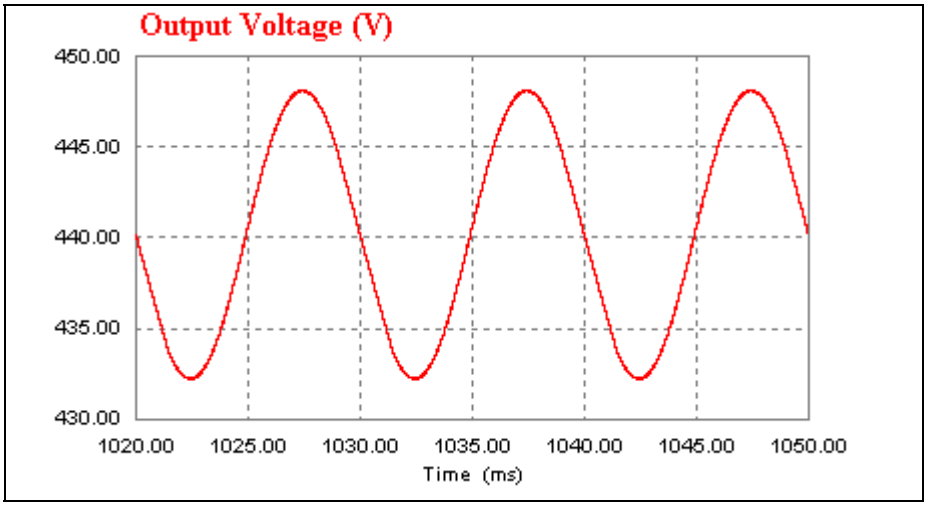



**Figure 6.19** Classical unity power rectifier's output voltage waveform with 3 kW inductive-resistive load (10 uH) at steady state.

Figure 6.18 and 6.19 show the rectifier's input voltage, input current and output voltage respectively. The input current changes between 22.45 and 18.84 A at its peak. The rectifier's maximum output voltage is 448.102 V and its minimum output voltage is 432.168 V. However, the rectifier's mean output voltage stays constant and this means that it is stable. Output voltage and input current ripple are calculated as 3.62 %, 8.74 % respectively. The rectifier gives 3006 W with this load.

The IGBT and diodes' voltage and current waveform are not given in this section since their waveform shapes are similar to ones in previous section. The rectifier's input power and input power factor are shown in figure D.20(a) and D.20(b) in Appendix D.2.1.2. Its input current's FFT waveform and THD graph are given in figure D.21 and D.22 in also Appendix D.2.1.2.

The rectifier's efficiency, input power factor, THD of its input current, input current ripple, output voltage ripple and the IGBT, boost diode, D5, bridge diodes, D1, D2, D3, D4's voltage and current stresses, and their power losses are given in the related part of table 6.8. Its input current's harmonics up to $50^{th}$ harmonic is listed in the part related with the classical UPF rectifier in table 6.10.

#### 6.4.2.2 Proposed Converter's Simulation With Inductive-Resistive Load

In this section, only the proposed rectifier with the 3 kW inductive-resistive loads is simulated and its performances are investigated with the simulations made.

##### 6.4.2.2.1 Proposed Converter's Simulation With Inductive-Resistive Load (100 uH)

The classical unity power factor rectifier is simulated when its loads are inductive and purely resistive, and also, the proposed rectifier is simulated by connecting purely resistive load to its output before. The related results are given before in previous sections. In this section, proposed rectifier's simulation results

with 3 kW inductive-resistive load which consists of a 100 uH inductor and 64.5 Ω resistor serially connected to the inductor at steady state are given. Its output voltage ripple, input current ripple, efficiency and the THD (total harmonic distortion), etc are investigated.

Figure 6.20 and figure 6.21 show the proposed rectifier's input current with its input voltage and its output voltage waveform respectively. Its output voltage swings between 448.244 and 432.151 V with this load at steady state, and its mean output voltage is closely 440.2 V. This mean output voltage stays constant through the simulation at steady state. The output voltage ripple is nearly 3.66 %. Also, its output power is 3006.32 W. Input peak current changes between 22.74 and 19.07 A, so input current ripple is 8.78 %. Proposed converter's output voltage ripple and input current ripple with this inductive-resistive load are moderately higher than the ones with 3 kW purely resistive load given in section 6.4.1.2.

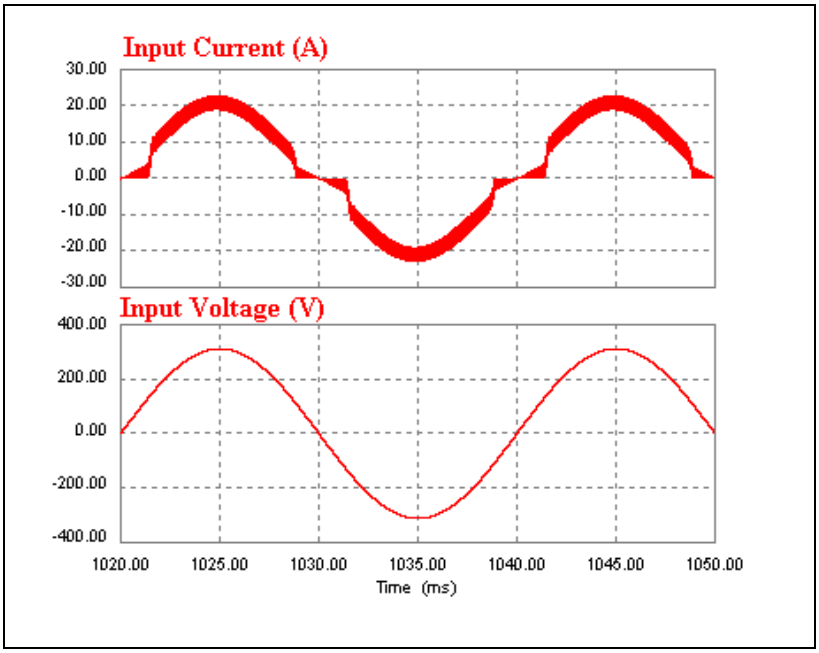



**Figure 6.20** Proposed rectifier's input voltage and current waveform with 3 kW inductive-resistive load (100 uH) at steady state.

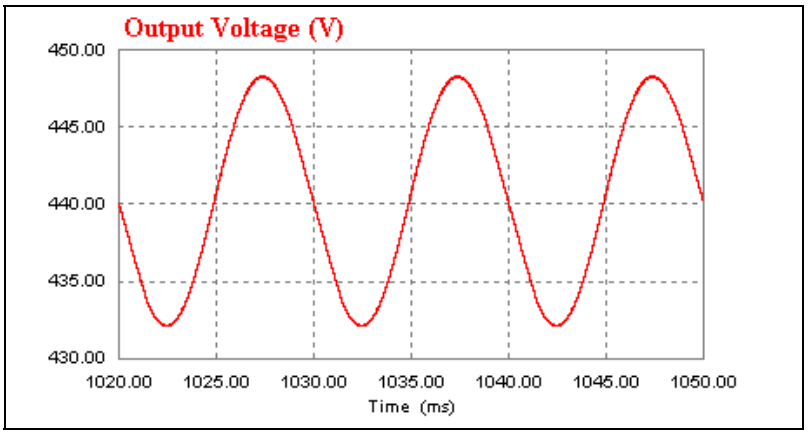



**Figure 6.21** Proposed rectifier's output voltage waveform with 3 kW inductive-resistive load (100 uH) at steady state.

The proposed rectifier's input power and power factor graph is given in figure D.23(a) and D.23(b) in Appendix D.2.2.1. Its input current's FFT waveform and THD, IGBT's current and voltage waveform, one of the boost diodes, D3's current and voltage waveform are given in figure D.24, D.25, D.26, D.27 in Appendix D.2.2.1 respectively. The bridge diodes, D1 and D7's current and voltage waveforms are given in figure D.28 and D.29 in the same part in Appendix D.

The rectifier's efficiency, input power factor, THD of its input current, input current ripple, output voltage ripple and the IGBT, boost diodes, D3 and D5, bridge diodes, D1, D2, D6, D7's voltage and current stresses, and their power losses are given in the part related with the proposed rectifier in table 6.8. Its input current's harmonics up to $50^{th}$ harmonic is listed in the part related with the classical UPF rectifier in table 6.9.

#### 6.4.2.2.2 Proposed Converter's Simulation With Inductive-Resistive Load (10 uH)

Proposed converter is simulated by placing a 100 uH inductor serially connected to 64.5 ohm to its output as a load and the simulation results are given in

previous section. In this section, the load is changed with 10 uH inductor serially connected to 64.5 Ω resistor and the converter is resimulated to investigate whether its power factor, total harmonic distortion, input current ripple, etc changes or not.

Proposed rectifier's input current and input voltage waveform are given in figure 6.22, and figure 6.23 shows its output voltage waveform. Its output voltage ripple and input current ripple do not change much to observe their differences when the load's inductance is 10 uH or 100 uH. This means that its output voltage varies between 448.244, 432.151 V and input peak current changes between 22.74 and 19.07 A. Similarly, its mean output voltage stays constant at steady state. The input current ripple and output voltage ripple are 8.78 % and 3.66 % as in the previous section. Also, its output power is 3006.32 W.

The IGBT and diodes' voltage and current waveform are not given in this section since their waveform shapes are similar to ones in previous section. The rectifier's input power and input power factor are shown in figure D.30(a) and D.30(b) in Appendix D.2.2.2. Also, its input current's FFT waveform and THD graph are given in figure D.31 and D.32 in Appendix D.2.2.2 respectively.

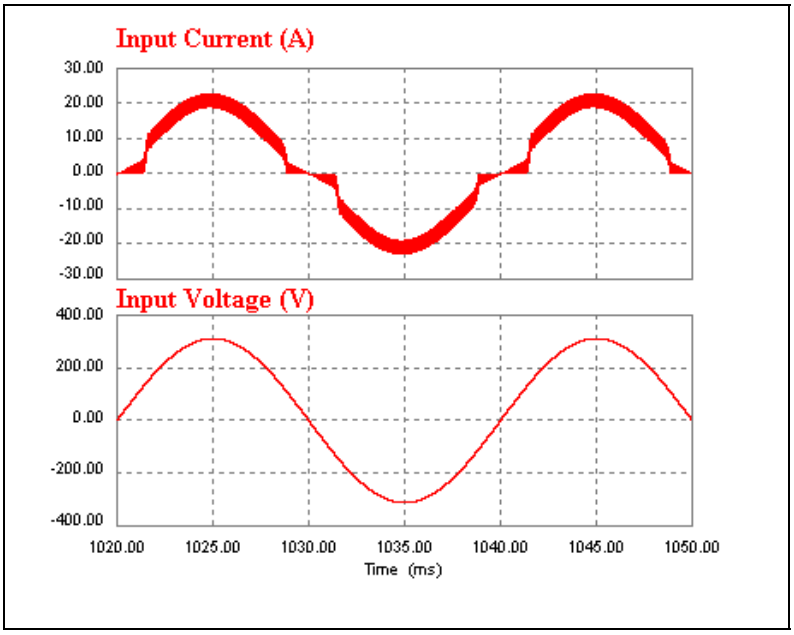



**Figure 6.22** Proposed rectifier's input voltage and current waveform with 3 kW inductive-resistive load (10 uH) at steady state.

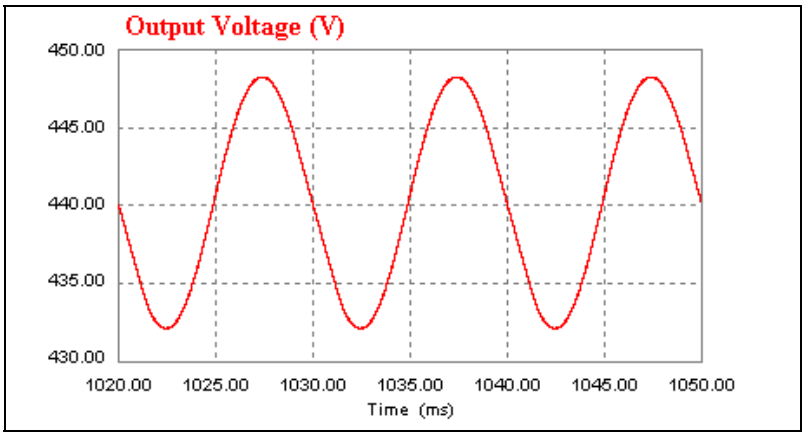



**Figure 6.23** Proposed rectifier's output voltage waveform with 3 kW inductive-resistive load (10 uH) at steady state.

All important data such as the rectifier's efficiency, input power factor are given in table 6.8. Its input current's harmonics up to 50$^{th}$ harmonic is also listed in the part related with the proposed rectifier in table 6.10. The results are evaluated in section 6.4.2.3.

### 6.4.2.3 Evaluation Of Simulation Results Of Classical And Proposed UPF Rectifier With 3 kW Inductive-Resistive Loads (100 uH and 10 uH)

Proposed and classical unity power factor rectifier are investigated upon their efficiency, input power factor, input current's THD, input current ripple, output voltage ripple, IGBT and diodes' stresses and losses with the two different 3 kW inductive-resistive loads. They are listed in table 6.8.

The proposed rectifier gives same results with the 3 kW loads, which are 100 uH inductor serially connected to a 64.5 Ω resistor load and 10 uH inductor serially connected to a 64.5 Ω resistor load according to data in table 6.8. Similarly, the classical unity power factor rectifier gives same results with this two loads.

| | Classical UPF Rectifier With 3 kW Inductive-Resistive Load (100 uH) | Proposed UPF Rectifier With 3 kW Inductive-Resistive Load (100 uH) | Classical UPF Rectifier With 3 kW Inductive-Resistive Load (10 uH) | Proposed UPF Rectifier With 3 kW Inductive-Resistive Load (10 uH) |
|---|---|---|---|---|
| **Efficiency (%)** | 97.29 | 97.45 | 97.29 | 97.45 |
| **Input Power Factor** | 0.9873 | 0.9864 | 0.9873 | 0.9864 |
| **THD (%)** | 16.06 | 16.59 | 16.06 | 16.59 |
| **Input Current Ripple (%)** | 8.95 | 8.78 | 8.74 | 8.78 |
| **Output Voltage Ripple (%)** | 3.60 | 3.66 | 3.62 | 3.66 |
| **IGBT Stress** | 449.0 V, 22.46 A | 448.72 V, 22.75 A | 449.42 V, 22.45 A | 448.71 V, 22.75 A |
| **Boost Diode Stress** | 446.12 V, 23.47 A | 445.27 V, 22.74 A for D3 and D5 | 446.12 V, 22.47 A | 445.27 V, 22.74 A for D3 and D5 |
| **Bridge Diodes' Stresses** | 309.87 V, 22.45 A for each diode | 449.72 V, 22.74 A for D1, D2 449.56 V, 22.73 A for D6, D7 | 309.87 V, 22.43 A for each diode | 449.73 V, 22.74 A for D1, D2 449.56 V, 22.74 A for D6, D7 |
| **IGBT's Power Loss** | 10.04 W | 9.88 W | 10.04 W | 9.88 W |
| **Boost Diodes' Power Loss** | 8.89 W | 8.9 W (4.45 W for each D3 and D5) | 8.89 W | 8.9 W (4.45 W for each D3 and D5) |
| **Diode Bridge's Power Loss** | 25.28 W (6.32 W for each diode) | 2.6 W for each D1, D2 6.28 W for each D6, D7 (Total 17.76 W) | 25.28 W (6.32 W for each diode) | 2.6 W for each D1, D2 6.28 W for each D6, D7 (Total 17.76 W) |

**Table 6.8** Performance comparison table between proposed rectifier and classical unity power factor rectifier with two 3 kW inductive-resistive (100 uH and 10 uH) load.

| | Classical UPF Rectifier (100 uH) | Proposed UPF Rectifier (100 uH) | | Classical UPF Rectifier (100 uH) | Proposed UPF Rectifier (100 uH) |
|---|---|---|---|---|---|
| **Harmonic #** | **Magnitude (A)** | **Magnitude (A)** | **Harmonic #** | **Magnitude (A)** | **Magnitude (A)** |
| 1 | 19.6 | 19.56 | 26 | 0 | 0 |
| 2 | 0 | 0 | 27 | 0.11 | 0.1 |
| 3 | 1.75 | 2.08 | 28 | 0 | 0 |
| 4 | 0 | 0 | 29 | 0.2 | 0.19 |
| 5 | 1.46 | 1.4 | 30 | 0 | 0 |
| 6 | 0 | 0 | 31 | 0.17 | 0.15 |
| 7 | 1.16 | 1.06 | 32 | 0 | 0 |
| 8 | 0 | 0 | 33 | 0.05 | 0.05 |
| 9 | 0.55 | 0.48 | 34 | 0 | 0 |
| 10 | 0 | 0 | 35 | 0.1 | 0.09 |
| 11 | 0.12 | 0.12 | 36 | 0 | 0 |
| 12 | 0 | 0 | 37 | 0.15 | 0.14 |
| 13 | 0.44 | 0.41 | 38 | 0 | 0 |
| 14 | 0 | 0 | 39 | 0.1 | 0.09 |
| 15 | 0.47 | 0.42 | 40 | 0 | 0 |
| 16 | 0 | 0 | 41 | 0.03 | 0.03 |
| 17 | 0.23 | 0.2 | 42 | 0 | 0 |
| 18 | 0 | 0 | 43 | 0.09 | 0.08 |
| 19 | 0.12 | 0.12 | 44 | 0 | 0 |
| 20 | 0 | 0 | 45 | 0.1 | 0.1 |
| 21 | 0.3 | 0.27 | 46 | 0 | 0 |
| 22 | 0 | 0 | 47 | 0.06 | 0.06 |
| 23 | 0.28 | 0.25 | 48 | 0 | 0 |
| 24 | 0 | 0 | 49 | 0.03 | 0.03 |
| 25 | 0.11 | 0.1 | 50 | 0 | 0 |

**Table 6.9** Proposed and classical UPF rectifier's input current harmonics' number and magnitudes up to 50$^{th}$ harmonic with 3 kW inductive-resistive load (100 uH) at steady state.

The rectifiers' harmonic number and magnitudes up to 50$^{th}$ harmonic with the 3 kW inductive-resistive loads (100 uH and 10 uH) at steady state are given in table 6.9 and table 6.10. There are small differences between the two rectifiers' harmonic magnitudes up to 50$^{th}$ harmonic in table 6.9 and table 6.10. Also, the even harmonic magnitudes in table 6.9 and table 6.10 are 0 for the two rectifiers. The harmonic magnitudes are the same except the 21$^{st}$ harmonic magnitudes in the parts related with the classical unity power factor rectifier in the two table. However, the difference between the 21$^{st}$ harmonic magnitude in table 6.9 and the one in table 6.10 is negligibly small.

| | Classical UPF Rectifier (10 uH) | Proposed UPF Rectifier (10 uH) | | Classical UPF Rectifier (10 uH) | Proposed UPF Rectifier (10 uH) |
|---|---|---|---|---|---|
| **Harmonic #** | **Magnitude (A)** | **Magnitude (A)** | **Harmonic #** | **Magnitude (A)** | **Magnitude(A)** |
| 1 | 19.60 | 19.56 | 26 | 0.00 | 0 |
| 2 | 0.00 | 0 | 27 | 0.11 | 0.1 |
| 3 | 1.75 | 2.08 | 28 | 0.00 | 0 |
| 4 | 0.00 | 0 | 29 | 0.20 | 0.19 |
| 5 | 1.46 | 1.4 | 30 | 0.00 | 0 |
| 6 | 0.00 | 0 | 31 | 0.17 | 0.15 |
| 7 | 1.16 | 1.06 | 32 | 0.00 | 0 |
| 8 | 0.00 | 0 | 33 | 0.05 | 0.05 |
| 9 | 0.55 | 0.48 | 34 | 0.00 | 0 |
| 10 | 0.00 | 0 | 35 | 0.10 | 0.09 |
| 11 | 0.12 | 0.12 | 36 | 0.00 | 0 |
| 12 | 0.00 | 0 | 37 | 0.15 | 0.14 |
| 13 | 0.44 | 0.41 | 38 | 0.00 | 0 |
| 14 | 0.00 | 0 | 39 | 0.10 | 0.09 |
| 15 | 0.47 | 0.42 | 40 | 0.00 | 0 |
| 16 | 0.00 | 0 | 41 | 0.03 | 0.03 |
| 17 | 0.23 | 0.2 | 42 | 0.00 | 0 |
| 18 | 0.00 | 0 | 43 | 0.09 | 0.08 |
| 19 | 0.12 | 0.12 | 44 | 0.00 | 0 |
| 20 | 0.00 | 0 | 45 | 0.10 | 0.1 |
| 21 | 0.29 | 0.27 | 46 | 0.00 | 0 |
| 22 | 0.00 | 0 | 47 | 0.06 | 0.06 |
| 23 | 0.28 | 0.25 | 48 | 0.00 | 0 |
| 24 | 0.00 | 0 | 49 | 0.03 | 0.03 |
| 25 | 0.11 | 0.1 | 50 | 0.00 | 0 |

**Table 6.10** Proposed and classical UPF rectifier's input current harmonics' number and magnitudes up to $50^{th}$ harmonic with 3 kW inductive-resistive load (10 uH) at steady state.

The rectifiers maintain their unity power factor operation with these inductive-resistive loads. Their efficiency, input current ripples and output voltage ripples given in table 6.8 with the inductive resistive loads are within the specified values given in section 6.1.

### 6.4.3 Classical Unity Power Factor Rectifier's Simulation With 3 kW Resistive Load By Taking Reference Voltage From A Transformer Connected To Mains Supply

Classical unity power factor rectifier, whose block diagram is shown in figure 6.7, is simulated by taking $I_{ac}$ and $V_{rms}$ signal feedbacks from a transformer connected to mains supply as in figure 6.8 with PSIM 6.1 simulation program and UC3854B IC model in figure 6.1 to investigate whether taking these signals in this way affects its performance with 3 kW purely resistive load considering THD, output voltage ripple, input current ripple, etc.

The rectifier's input power and input power factor graphs are shown in figure D.33(a) and D.33(b) in Appendix D.3. Its input current with input voltage and its output voltage waveforms are shown in figure D.34(a) and D.34(b) in Appendix D.3. On the other hand, its input current's FFT waveform and input current's THD graph are shown in figure D.35(a) and D.35(b) in the same part in Appendix D. These figures are obtained via the simulation.

| | **Classical UPF Rectifier With 3 kW Purely Resistive Load Taking Reference Voltage By Using A Transformer** |
|---|---|
| **Efficiency (%)** | 97.21 |
| **Input Power Factor** | 0.9864 |
| **THD (%)** | 16.63 |
| **Input Current Ripple (%)** | 8.70 |
| **Output Voltage Ripple (%)** | 3.66 |
| **IGBT Stress** | 449.46 V, 22.79 A |
| **Boost Diode Stress** | 446.16 V, 22.80 A |
| **Bridge Diodes' Stresses** | 309.90 V, 22.80 A |
| **IGBT's Power Loss** | 9.93 W |
| **Boost Diodes' Power Loss** | 8.89 W |
| **Diode Bridge's Power Loss** | 25.20 W (Each diode has 6.3 W loss) |

**Table 6.11** Classical UPF rectifier performance table when its reference voltage is taken by using a transformer.

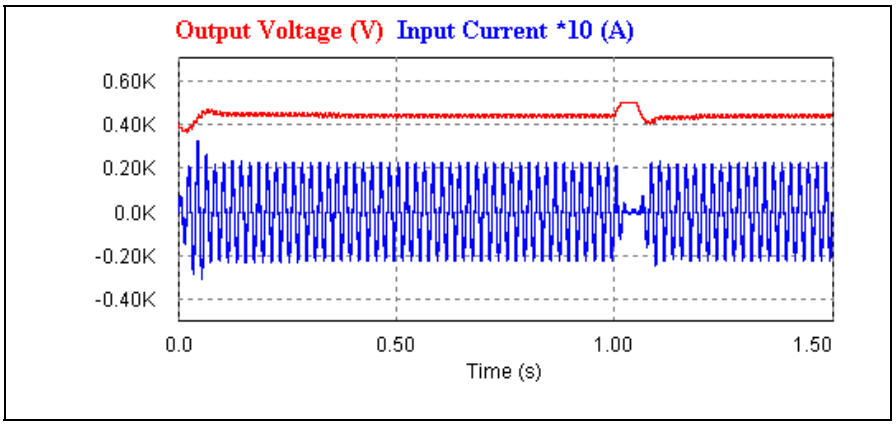
The rectifier's results such as efficiency, input power factor obtained via the simulation are listed in table 6.11. When the $I_{ac}$ and $V_{rms}$ signal feedbacks are taken from a transformer connected to mains supply as in figure 6.8, classical unity power factor rectifier has worse results than the ones when the feedbacks are taken from the bridge rectifier as in figure 6.7 by considering its input power factor, efficiency, output voltage ripple, THD, but its input current ripple given in table 6.11 is lower than its input current ripple in table 6.6. Also, the proposed rectifier with 3 kW purely resistive load has better efficiency, output voltage ripple and input current's THD given in table 6.6 than the classical unity power factor rectifier's ones in table 6.11. Proposed rectifier's power factor given in table 6.6 and the power factor in table 6.11 are same, but its input current ripple given in table 6.11 is lower than the one given in table 6.6. These show that the classical unity power factor rectifier's performance results are related with where the signal feedbacks are taken.

### 6.4.4 Classical Unity Power Factor And Proposed Rectifier's Simulation With 3 kW Purely Resistive Load In Dynamic Conditions And Their Comparison

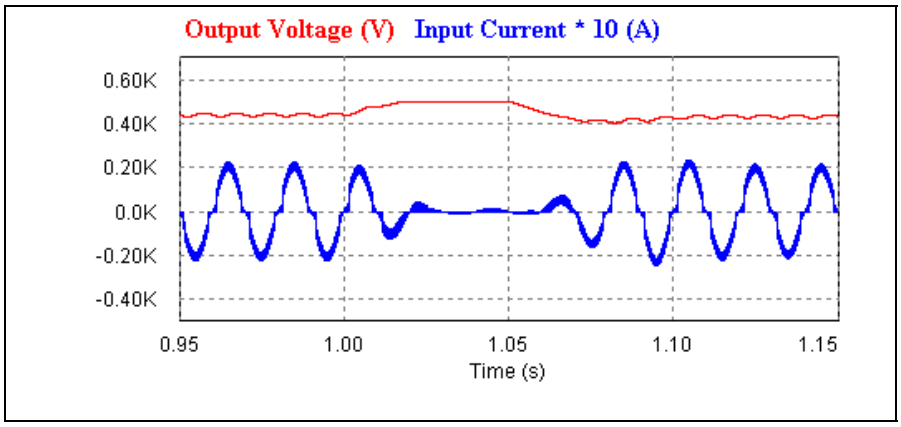
The classical unity power factor rectifier and proposed rectifier, whose block diagrams are given in figure 6.7 and 6.8 respectively, are simulated in dynamic conditions. In the simulations, PSIM 6.1 simulation program and the UC3854B IC model in figure 6.1 are used. 3 kW purely resistive loads are connected to the rectifiers' output, after a while they are disconnected and then connected again in PSIM 6.1 simulation environment. In this way, the rectifiers' output voltage and input current waveforms are obtained in the dynamic conditions, and their settling times are calculated.

### 6.4.4.1 Classical Unity Power Factor Rectifier's Simulation With 3 kW Purely Resistive Load In Dynamic Conditions

Classical unity power factor rectifier whose block diagram is shown in figure 6.7 is simulated by connecting 3 kW purely resistive load and disconnecting it between 1s -1.05 s. and connecting again at the end of this period.




**(a)**

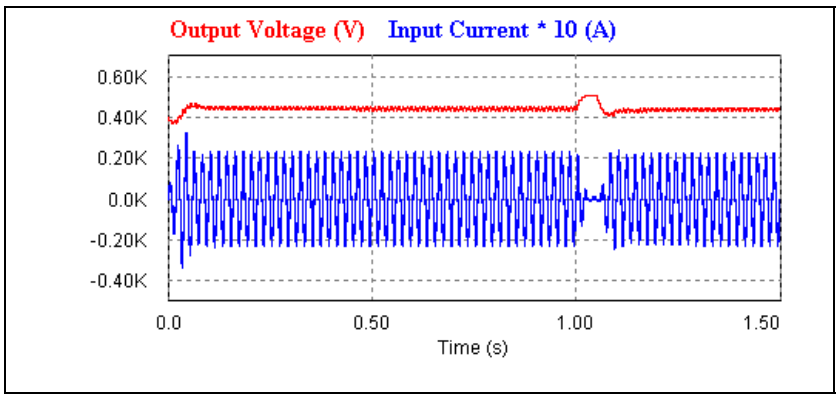



**(b)**

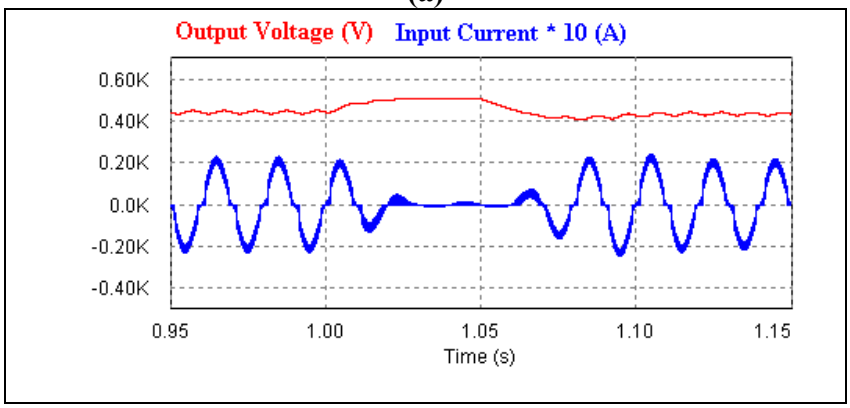
**Figure 6.24** (a) Classical unity power factor rectifier's output voltage and input current waveform when 3 kW purely resistive load is connected, it is disconnected between 1 s. and 1.05 s. and connected again, (b) its zoomed version.

Figure 6.24 shows the rectifier's input current and output voltage in mentioned conditions above. Its maximum output voltage is nearly 447.84 V at steady state before the 3 kW purely resistive load is disconnected. Its ± 5 % values are 424.45 V and 473.23 V. Time difference between the time, which 3 kW purely resistive load is reconnected at and the first time, which the rectifier's maximum output voltage reaches between these values at, gives settling time. The rectifier's maximum output voltage reaches 433.496 V at 1.09765 s. 433.496 V is between the voltage values. Then, the rectifier's settling time is 47.65 ms.

### 6.4.4.2 Proposed Rectifier's Simulation With 3 kW Purely Resistive Load In Dynamic Conditions




**(a)**




**(b)**

**Figure 6.25 (a)** Proposed rectifier's output voltage and input current waveform when 3 kW purely resistive load is connected, it is disconnected between 1 s. and 1.05 s. and connected again, **(b)** its zoomed version.

3 kW purely resistive load is connected to the proposed rectifier's output and it is disconnected between 1 s. and 1.5 s in PSIM 6.1 simulation environment. Then it is reconnected. In this way, the rectifier's settling time is calculated similarly in section 6.4.4.1. The rectifier's input current and output voltage waveform obtained by making a simulation with the simulation program and the waveforms are given in figure 6.25.

The proposed rectifier's maximum output voltage is 449.821 V. First time, its maximum output voltage reaches a value, which is between $\pm 5$ % of 449.821 V at 1.09761 s. It is 434.193 V and the rectifier's settling time is 47.61 ms. The settling time is nearly same with the classical unity power factor rectifier's one given in section 6.4.4.1.

## 6.5 Conclusion

Classical unity power factor rectifier and proposed rectifier with 3 kW purely resistive load are compared on basis of their efficiency, power factor, input current's THD, input current ripple, output voltage ripple, transistor and diode number, and their stresses, etc. Some of them are given in table 6.12.

Proposed rectifier is better than the other one on the basis of efficiency and input current ripple. On the other hand, the proposed rectifier's output voltage ripple and input current's THD are a little bit higher than the other one and its power factor is lower than the other. However, these are nearly same for the two rectifiers. An extra ultrafast boost power diode is needed in the proposed rectifier. On the other hand, the classical unity power factor rectifier needs an extra free-wheeling diode to achieve the boost inductor's core resetting. The two rectifier's transistor and boost diode current and voltage stresses are nearly same. Proposed rectifier's bridge diodes voltage stresses are higher than the classical unity power factor rectifier's ones.

Proposed rectifier and classical unity power factor rectifier's simulation results are also obtained before by connecting serially connected 64.5 Ω resistor and 100 uH inductor to their outputs. They are given in table 6.13.

The efficiencies, power factors and THDs are same in table 6.12 and table

6.13. The rest of the parameters are nearly same. Proposed rectifier and classical unity power factor rectifier are simulated before by connecting serially connected 64.5 Ω resistor and 10 uH inductor to their outputs and similar performance results are obtained to the ones in table 6.13, so they are not given here. Thus, the rectifiers' performances don't differ much whether their loads are inductive or purely resistive.

| | **Classical unity power factor rectifier with 3 kW purely resistive load** | **Proposed rectifier with 3 kW purely resistive load** |
|---|---|---|
| **Efficiency (%)** | 97.29 | 97.45 |
| **Power Factor** | 0.9873 | 0.9864 |
| **THD (%)** | 16.06 | 16.59 |
| **Input Current Ripple (%)** | 8.95 | 8.78 |
| **Output Voltage Ripple (%)** | 3.6 | 3.65 |
| **Transistor Stress** | 449.42 V, 22.46 A | 448.71 V, 22.74 A |
| **Boost Diode Stress** | 446.1 V, 22.46 A | 445.27 V, 22.74 A |
| **Bridge Diode Stress** | 309.87 V, 22.26 A for each | 449.73 V, 22.74 A for D1, D2<br>449.57 V, 22.74 A for D6, D7 |
| **Number of Power Transistors** | 1 IGBT with reverse-recovery diode | 1 IGBT with reverse-recovery diode |
| **Number of Power Diodes** | 1 ultrafast boost diode, 4 bridge diode. 1 ultrafast free-wheeling diode | 2 ultrafast boost diode, 4 bridge diode |

**Table 6.12** Performance comparison table between proposed rectifier and classical unity power factor rectifier with 3 kW purely resistive load.

Proposed rectifier topology has better efficiency, output voltage ripple and THD than classical unity power factor rectifier's ones when its $I_{ac}$ and $V_{rms}$ signal feedbacks are taken from a transformer connected to mains supply as in figure 6.8 and with 3 kW purely resistive load. The simulation results in this way are given before in section 6.4.3. These show that the rectifiers' performance depends on where the $I_{ac}$ and $V_{rms}$ signal feedbacks are taken.

The rectifiers are simulated by using dynamic load connected to their outputs and results are given in section 6.4.4.1 and 6.4.4.2. The proposed rectifier's settling

| | Classical unity power factor rectifier with 3 kW inductive-resistive load (100 uH) | Proposed rectifier with 3 kW inductive-resistive load (100 uH) |
|---|---|---|
| **Efficiency (%)** | 97.29 | 97.45 |
| **Power Factor** | 0.9873 | 0.9864 |
| **THD (%)** | 16.06 | 16.59 |
| **Input Current Ripple (%)** | 8.95 | 8.78 |
| **Output Voltage Ripple (%)** | 3.6 | 3.66 |
| **Transistor Stress** | 449.0 V, 22.46 A | 448.72 V, 22.75 A |
| **Boost Diode Stress** | 446.12 V, 23.47 A | 445.27 V, 22.74 A |
| **Bridge Diode Stress** | 309.87 V, 22.45 A for each | 449.72 V, 22.74 A for D1, D2<br>449.56 V, 22.73 A for D6, D7 |

**Table 6.13** Performance comparison table between proposed rectifier and classical unity power factor rectifier with serially connected 64.5 Ω resistor and 100 uH inductor load.

time is lower than the other one's settling time, but they are nearly same.

Consequently, proposed rectifier is decided to implement due to its higher efficiency and the reasons given above.

In the next chapter, implementation of the proposed rectifier is described. The following chapter also presents the measurement results on this rectifier. These results are used for assessing how reliable the simulations given in this chapter are.

# CHAPTER 7

# HARDWARE DESIGN IMPLEMENTATION AND RESULTS

## 7.1 Introduction

In this chapter, the proposed unity power factor rectifier, whose specification given in chapter 6 is implemented. Its block diagram is given in figure 7.1. The inductor used in proposed unity power factor rectifier topology is designed and its design procedure is given in this chapter. Information about snubbers is given briefly. In order to protect IGBT used in the unity power factor rectifier circuit, overvoltage and R-C snubber is designed and design procedure is given. Information about power semiconductors used in the proposed rectifier are also given. The proposed rectifier circuit's control circuit is explained.

Unity power factor boost rectifier's hardware implemented uses average current control and it contains a control circuit in the same electronic card to run the proposed rectifier and classical unity power factor rectifier, whose specifications are mentioned in chapter 6. In this way, the two rectifiers can work using the same electronic card and electronic components used in their control circuit are efficiently used. Otherwise; the number of resistors, capacitors and current sensor, diode bridge, ultrafast diodes, IGBT, etc would be doubled on the electronic card implemented or two electronic cards would had to be designed and implemented.

The proposed rectifier is tested in laboratory enviroment by connecting 1 kW and 2 kW nearly purely resistive loads. The results are presented in this chapter. Simulations are made in same conditions to identify whether the simulations are

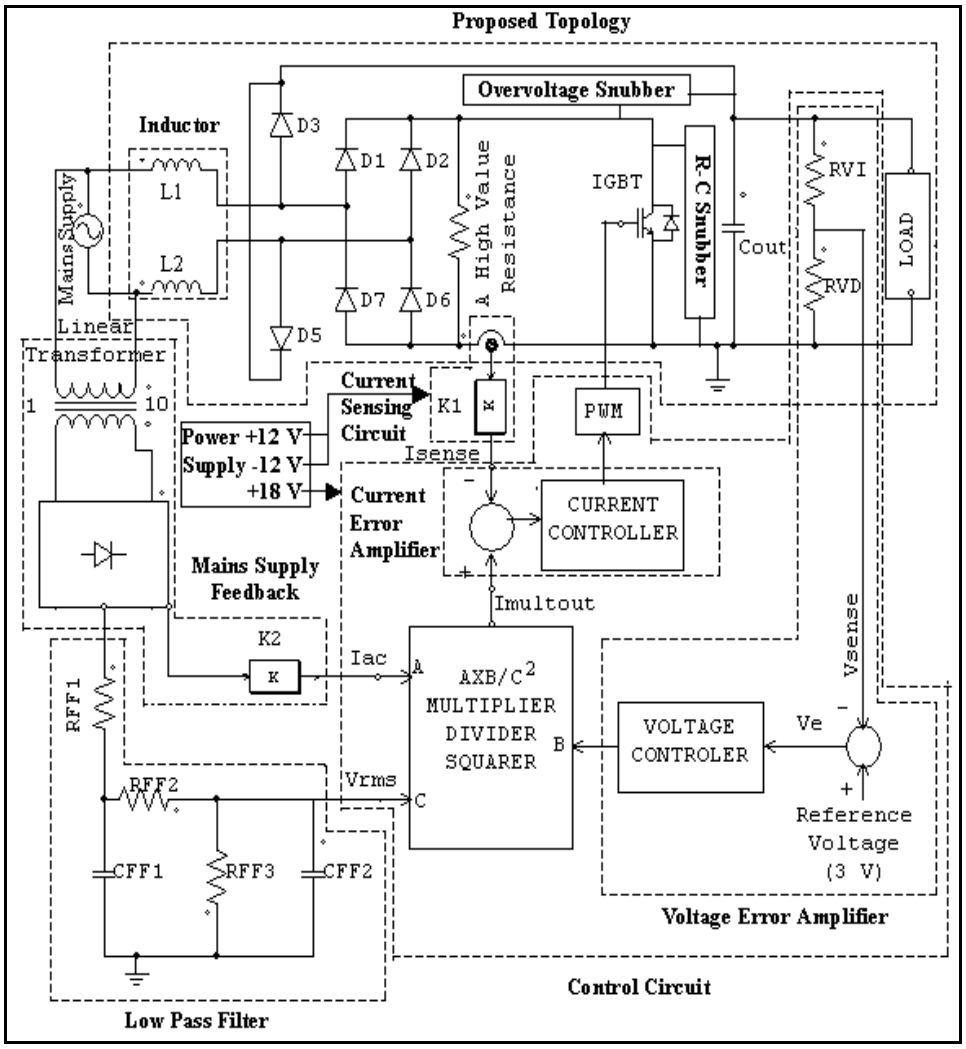



**Figure 7.1** Implemented proposed rectifier's block diagram.

reliable, so that some other tests can be performed in the simulation environment. In this manner, considerable time saving can be achieved in improving the circuit.

### 7.2 Hardware Design And Implementation

Implemented proposed rectifier's block diagram given in figure 7.1 contains some blocks and they are given in the same figure. They are inductor, overvoltage snubber, R-C snubber, current sensing circuit, low pass filter, the mains supply

feedback block, control circuit, power supply, the proposed topology blocks. Each block diagram and its corresponding circuit is explained in this section.

### 7.2.1 Inductor Design

The inductors, L1 and L2 shown in figure 7.1 are designed on a same core. Each inductor has 250 uH inductance and their total inductance is 500 uH. Its power rating is nearly 3100 W and its maksimum permissible current flowing through the inductors are 27.5 A. The inductors are designed as if one 500 uH inductor is designed. There are two coils on a C core, each represents a 250 uH inductance.

Selection of best magnetic core in inductor design stage is very critical in a given application. There are various magnetic cores such as ferrite, powdered iron, electrical steel, orthonol etc[2], [36]. Amorphous metal cores has high saturation flux density, low frequency dependent losses. Implementation of an efficient and small size inductor operating at high frequencies e.g. 50 kHz is possible by using amorphous metal cores [37].

In order to begin inductor design, the unity power factor rectifier's necessary specifications should be remembered since they are used in inductor design stage. Inductor efficiency should be decided since overall rectifier efficiency is dependent upon the inductor's efficiency. It should be as high as possible. 99 % or higher inductor efficiency is enough for this application. It will decrease the rectifier's efficiency 1 % and it will cause nearly 30 W power loss in the rectifier. In inductor design procedure given below, the rectifier's efficiency is taken as 97 % according to the simulation results in chapter 6. The inductor is designed and design procedures are given in the following steps [37], [38]:

Step #1:

Thus, necessary specifications are taken as the following ones:

- The rectifiers' output power, $P_{out} = 3000\,\mathrm{W}$
- Their switching frequency, $f_{sw} = 50\,\mathrm{kHz}$
- Their output dc voltage, $V_{out} = 440\,\mathrm{V}$

- Their minimum input voltage, $V_{in(ac)\min} = 187$ V rms
- Their maximum input voltage = 286 V rms
- The inductor's maximum temperature rise above ambient temperature, $\Delta T = 50\,^{0}$C
- Its efficiency, $\eta_{preg} \geq 99$ %
- Assumed rectifiers' efficiencies = 97 %
- The rectifiers' input current ripple, $\Delta I = 10$ % peak to peak.

The total inductance, L1+L2 in figure 7.1 used in the proposed unity power factor rectifier or classical unity power factor rectifier must be calculated before the inductor design stage. The rectifiers' peak input current without considering its input current ripple calculated as 23.37 A by taking the rectifiers' input power, $P_{in}$ as 3090 W and their minimum input voltage, $V_{in(rms)\min}$ 187 V rms, and using equation 7.1. Hence; the rectifiers' input current ripple, $\Delta I$ is 4.674 A since it is taken as 0.1 times the input current's peak to peak value.

$$I_{pk} = \frac{\sqrt{2} \times P_{in}}{V_{in(rms)\min}} \tag{7.1}$$

Duty cycle, D expression is given in chapter 2 in equation 2.2. Equation 2.2 gives D nearly 0.4 by taking the output DC voltage, $V_o$, input minimum peak voltage, $V_{in(peak)\min}$ as 440 V and 265 V respectively [2]. The inductance is calculated as 0.454 mH by using equation 2.2 and taking $\Delta I$ as calculated before. Taking inductance as 0.5 mH is appropriate to reduce the current ripple and guarantee it to be within the specified tolerances.

For a teoritically optimum design [37], inductor cupper and core losses should be nearly equal and this is stated in equation 7.2.

$$Powerloss = P_{tot} = 2 \times P_{core} = 2 \times P_{cu} \tag{7.2}$$

Metglas amorphous metal C-cores have a core loss equation and it is given by the following formula.

$$P_{core} = 6.5 \times f_{sw}^{1.51} \times B_{ac}^{1.74} \times wt \text{ in watts} \tag{7.3}$$

In equation 7.3, the switching frequency, $f_{sw}$; ac flux density, $B_{ac}$; core weight, $wt$ are in kHz, tesla, kg respectively.

Equation 2.2 can be rewritten as in (7.4) and taking inductance, L as 0.5 mH

,and placing the necessary parameter values in this equation; $\Delta I$ is recalculated as 4.22 A peak to peak for this inductance value.

$$L = \frac{\sqrt{2}V_{in(ac)\min} \times \left[1 - ((\sqrt{2}V_{in(ac)\min}) / V_{out}\right]}{\Delta I \times f_{sw}} \tag{7.4}$$

The current ripple, $\Delta I$, flux density, B and AC flux density, $B_{ac}$ are expressed in equation 7.5.

$$\Delta I = \left(\frac{2B_{ac}}{B}\right)\left[\frac{\sqrt{2} \times (P_{out})}{\eta_{preg} \times V_{in(ac)\min}}\right] \tag{7.5}$$

By putting maximum peak flux density, $B_{\max}$ in equation 7.5 instead of $B$, and using the values in specifications given before, following statement is derived for the inductor being designed.

$$\frac{B_{ac}}{B_{\max}} = 0.09021$$

Energy storage requirement of an inductor, $E$ can be calculated using equation 7.6

$$E = 0.5(L \times I_{peak}^2) \tag{7.6}$$

$I_{peak}$ in this equation is here the rectifiers' input peak current with considering the its input current ripple and equation 2.3 expressed $I_{pk}$ and $\Delta I$. $I_{peak}$ is calculated as nearly 25.5 A using equation 2.3 but control circuit designed using UC3854B IC permits 27.5 A peak current. Hence, $I_{peak}$ current is taken 27.5 A in equation 7.6 and the rest of the calculations. The inductance L is 0.5 mH, and then E is 0.189 joules.

Core area product, $W_a A_c$ is given in equation 7.7. In this equation, energy storage requirement of inductor, $E$ is in joules, $J$ is current density in A/cm$^2$, k is the window utilization factor. Current density, J is taken as 500 A/cm$^2$ to reduce the core volume since amorphous metal cores have generally higher prices than other types of core [2].

If the current flowing through the inductor has high frequency component, cupper resistance in the inductor will increase due to skin effect. Litz wire or foil winding can be used to reduce the resistance due to this effect [37]. The inductor design is made by the assumption that foil winding is used in the inductor. Hence, k can be taken as 0.4.

$$W_a A_c = \frac{2E}{B_{\max} \times J \times k} \tag{7.7}$$
$$= \frac{2 \times (0.189\, joules) \times 10^4}{B_{\max} \times 500 \times 0.4} = \frac{18.4}{B_{\max}}$$

Above statement is derived by placing the necessary parameter values in equation 7.7. Efficiency should be equal or higher than 99 % and inductor should not be exceed 50 $^0$C from ambient temperature according to the specifications given before. Placing $B_{ac} / B_{\max} = 0.09021$ expression in equation 7.3 to simplify and rewriting the equation in terms of $B_{\max}$ for the inductor being designed, the following expression is derived.

$$P_{core} = 36.35 \times (B_{\max})^{1.74} \times wt$$

Using two above statements, core area product, $W_a A_c$ is calculated, core number which has equal or higher and nearest core area product in table 7.2 is selected, and then the core loss is calculated by different $B_{\max}$ values in Tesla. Total inductor losses are also calculated. The results are given in table 7.1.

B-H curve for the Metglas amorphous metal is given in figure 7.2 according to its datasheet and saturation flux density can be acquired from this curve. The saturation flux density for the Metglas amorphous metal cores is 1.56 T and its datasheet is given in Appendix B in the thesis. Value of $B_{\max}$ can be taken as high as 1.4 T for the amorphous metal cores [38].

However, the core losses in the inductor can be reduced by using smaller $B_{\max}$ values as shown in table 7.1. The purpose here to find the smallest core size and the designed inductor, whose efficiency is equal or higher than 99 % while carrying the peak current of 27.5 A, and the converter transfers 3 kW power. Also, selected core's temperature rise must not exceed 50 $^0$C above ambient temperature. When $B_{\max}$ is equal to 0.8, 0.9, 1, 1.1, the inductor's efficiency is higher or equal to 99 % according to table 7.1.

Table 7.2 taken from reference [38] gives core numbers, their core area product, convective surface area and approximate power dissipation in watts for a given temperature rise. When $B_{\max}$ is equal to 1 or 1.1, total inductor loss causes

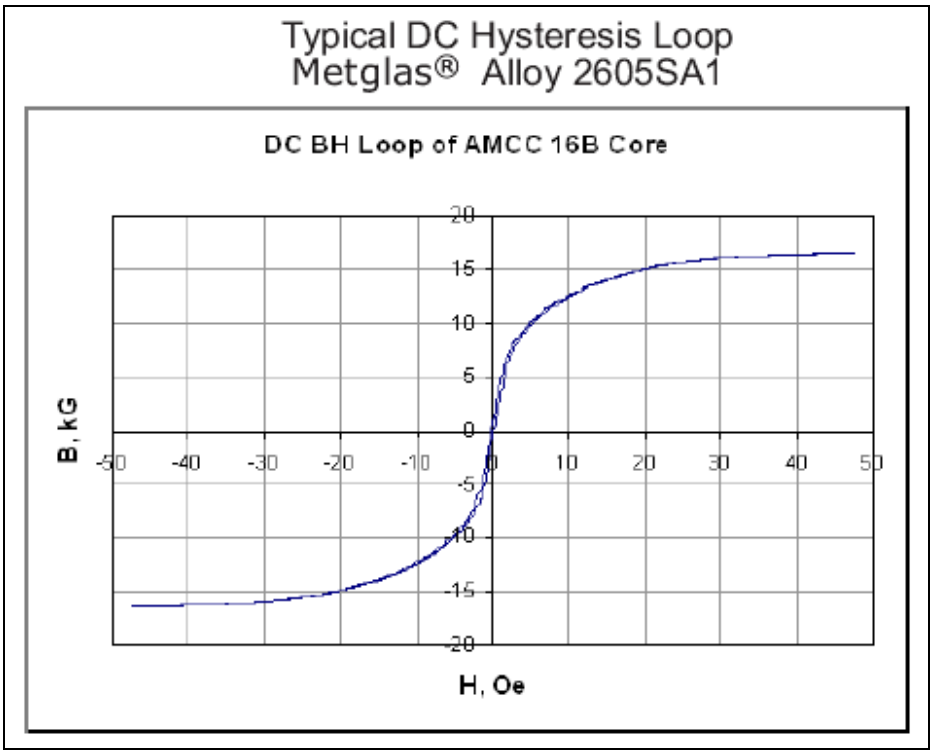



**Figure 7.2** B-H curve for Metglas amorphous metal cores in kilogauss and oersted.

| $B_{max}$ (Tesla) | $W_aA_c(cm^4)$ (Required) | Core Number | Core loss (watts) | Total inductor loss (watts) |
|---|---|---|---|---|
| 0.8 | 23 | AMCC-32 | 11.339 | 22.7 |
| 0.9 | 20.44 | AMCC-25 | 11.5 | 23 |
| 1 | 18.4 | AMCC-25 | 13.813 | 27.6 |
| 1.1 | 16.72 | AMCC-20 | 14.586 | 29.2 |
| 1.2 | 15.33 | AMCC-20 | 16.9728 | 34 |
| 1.3 | 14.15 | AMCC-16B | 16.0664 | 32.1 |
| 1.4 | 13.14 | AMCC-16B | 18.2756 | 36.6 |

**Table 7.1** Required core area product, core number, core and total inductor losses for the 500 uH inductor by different $B_{max}$ values.

temperature rise higher than 50 $^0$C above ambient temperature according to table 7.2. While $B_{max}$ is equal to 0.8 T, the inductor temperature rise is lower than 50 $^0$C, but higher volume core, namely AMCC-32 is required. On the other hand, total inductor

loss gives nearly 50 $^0$C temperature rise above the ambient temperature and the inductor's efficiency is higher than 99 % when $B_{max}$ is equal to 0.9 T. Hence, AMCC-25 amorphous metal core is selected and its $B_{max}$ value will be taken as nearly 0.9 T.

| | | | Approximate Power Dissipation in Watts for a Given Temperature Rise | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Core Number** | **$W_aA_c$ ($cm^4$)** | **SA ($cm^2$)** | **20 $^0$C** | **25 $^0$C** | **30 $^0$C** | **35 $^0$C** | **40 $^0$C** | **50 $^0$C** |
| AMCC-6.3 | 5.8 | 103.4 | 3.8 | 4.9 | 6.1 | 7.4 | 8.7 | 11.3 |
| AMCC-8 | 7 | 115.9 | 4.2 | 5.5 | 6.9 | 8.3 | 9.7 | 12.7 |
| AMCC-10 | 9.4 | 132.1 | 4.8 | 6.3 | 7.8 | 9.4 | 11 | 14.5 |
| AMCC-16A | 12 | 143.1 | 5.2 | 6.8 | 8.5 | 10.2 | 12 | 15.7 |
| AMCC-16B | 15 | 160.3 | 5.8 | 7.6 | 9.5 | 11.4 | 13.4 | 17.6 |
| AMCC-20 | 17.6 | 172.3 | 6.3 | 8.2 | 10.2 | 12.3 | 14.4 | 18.9 |
| AMCC-25 | 22.7 | 202.2 | 7.4 | 9.6 | 12 | 14.4 | 16.9 | 22.2 |
| AMCC-32 | 26.9 | 216 | 7.9 | 10.3 | 12.8 | 15.4 | 18.1 | 23.7 |
| AMCC-40 | 31.2 | 230 | 8.4 | 11 | 13.6 | 16.4 | 19.3 | 25.2 |
| AMCC-50 | 46.2 | 303.5 | 11.1 | 14.5 | 18 | 21.7 | 25.4 | 33.2 |

**Table 7.2** Approximate power dissipation values in watts for a given temperature rise and core number.

Step #2:

When AMCC-25 amorphous metal core is selected and its $B_{max}$ value is 0.9 T, the inductor efficiency is 99.23 % according to the total inductor loss in table 7.1 by taking the rectifiers' efficiency as if 100 %. Inductor total loss formula is given in equation 7.8. In this equation, $\eta_L$ is inductor efficiency, $P_{out}$ is rectifier's output power and $\eta_{preg}$ is its efficiency. Using this formula, total inductor losses are recalculated.

$$P_{tot} = (1-\eta_L) \times (P_{out} \div \eta_{preg}) \text{ in watts} \quad (7.8)$$

Then, the inductor loss, $P_{tot}$ is nearly 23.8 watts. $P_{core}$ and $P_{cu}$ losses in the inductor are 11.9 W. 22 W dissipated in an AMCC-25 will give temperature rise to nearly 50 $^0$C. Thus, these show that right core, namely AMCC-25 is selected in step 1. Power loss for the core weight formula is given in equation 7.9.

$$P = P_{tot} / 2wt \quad (7.9)$$

The core weight, $wt$ is 0.38 kg for AMCC-25 core and then $P$ is 31.32 W/kg. Equation 7.3 and 7.9 gives equation 7.10 expressing ac flux density, $B_{ac}$ in terms of $P$ and $f_{sw}$.

$$B_{ac} = \left[P / (6.5 f_{sw}^{1.51}\right]^{1/1.74} \quad (7.10)$$

In equation 7.10, $B_{ac}$, $P$, $f_{sw}$ are in terms of T, W/kg, kHz. Then, $B_{ac}$ is 0.0828 T.

In step 1, $L$ and $\Delta I$ are calculated as 0.5 mH, 4.22 A. $B_{\max}$ is recalculated more precisely by putting these values in equation 7.5 and it is found to be 0.9179 T, which is acceptable.

Step #3:

Core area product, $W_a A_c$ is recalculated for given $J$, $k$ values and by using equation 7.7 and taking $B_{\max}$ as 0.9179 T in order to check that the selected core in step 1 has enough core area product. The core area product is found to be 20.59 cm$^4$. AMCC-25's core area product is 22.7 cm$^4$ as seen in table 7.2. Then, it is right core to implement the inductor. The amorphous metal core has the following dimensions related with figure 7.3:

- $a = 1.3$ cm
- $b = 1.5$ cm
- $c = 5.6$ cm
- $d = 2.5$ cm
- $e = 4.1$ cm
- $f = 8.2$ cm

Also, the AMCC-25 core has the characteristics given below:

- Magnetic path length of core, $l_m = 19.6$ cm
- Core cross-section, $A_c = 2.7$ cm$^2$

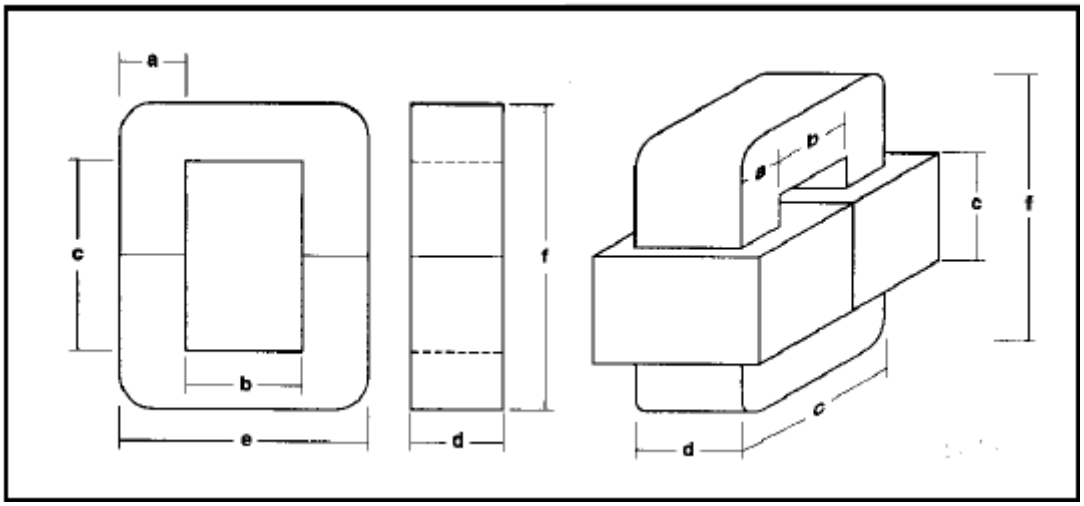



**Figure 7.3** C core dimensions.

- Core weight, $wt = 0.38$ kg
- Core area product, $W_a A_c = 22.7\,\text{cm}^4$
- Convective surface area, $SA = 202.2\,\text{cm}^2$.

Step #4:

In this step, the number of turns required, N is calculated. It is expressed in terms of $L$, $I_{peak}$, $B_{\max}$, $A_c$ in equation 7.11 and the values of these variables are 0.5 mH, 27.5 A, 0.9179 T and 2.7 cm$^2$ for the inductor being designed and core selected. N is calculated as 56 turns.

$$N = \frac{L \times I_{peak} \times 10^4}{B_{\max} \times A_c} \text{ turns} \tag{7.11}$$

Step #5:

In this step, the inductor's airgap value is calculated. Total air gap value required is expressed in equation 7.12 where $l_m$ is magnetic core length, $\mu\Delta$ is incremental permeability at operating on B-H loop in figure 7.2. $\mu\Delta$ is nearly equal to 1000 for the operating point.

$$l_g = \frac{0.4 \times \pi \times N \times I_{peak} \times 10^{-4}}{B_{\max}} - \frac{l_m}{\mu\Delta} \tag{7.12}$$

$$l_g = \frac{0.4 \times \pi \times 56 \times 27.5 \times 10^{-4}}{0.9179} - \frac{19.6}{1000}$$

Necessary parameters is put in equation 7.12; total air gap, $l_g$ is calculated as 0.19 cm and then it is 0.095 cm/leg.

Step #6:

Fringing flux decreases the air gap reluctance and so increases inductance by a factor F. It can be calculated using the following formula approximately. In the equation, $l_g$ is inductor's total air gap calculated in step 5 and the rest of the parameters related with the core's dimension and they are given in step 3.

$$F = \frac{(a + (l_g / 2)) \times (d + (l_g / 2))}{a \times d} \tag{7.13}$$

Then, the amount of fringing flux, F is calculated as 1.114.

Step #7:

In this step, the turn number is corrected by taking into account the fringing flux. In step 1; number of turns, N is calculated. However, the amount of fringing flux, F affects the effective core cross-section. Equation 7.14 expresses the number of turns, N by including the fringing flux affect. Necessary parameter values in the equation are given before in this sub-chapter. N is calculated as 52.65 by putting them in equation 7.14. N should be higher or equal to what is calculated. The core has two coils on both sides of the C cores as in figure 7.3. N must be even number, so it is taken as 54.

$$N = \sqrt{\frac{L \times \left[l_g + (l_m / \mu\Delta)\right] \times (10^8)}{0.4 \times \pi \times A_c \times F}} \text{ turns} \tag{7.14}$$

Step #8:

The cross-sectional area of the conductor used in the inductor is calculated as 0.062 $cm^2$ by taking b, c, k, N as 1.5 cm, 5.6 cm, 0.4 and 54 and putting them in equation 7.15.

$$A_x = \frac{b \times c \times k}{N} \tag{7.15}$$

The resistivity of copper as a function of temperature is expressed in equation 7.16. Assuming that the maximum ambient temperature is 30 $^0$C and the inductor gives 50 $^0$C additional temperature rise, $T$ is taken 80 $^0$C. Then, the resistivity of copper is 2.16 μΩ-cm.

$$\rho = 1.724 \times [1 + 0.0042 \times (T - 20)] \times (10^{-6})\ \Omega\text{-cm} \tag{7.16}$$

The resistance per unit length for the conductor is 34.7 μΩ-cm and is calculated by using (7.17)

$$R_{unit} = \frac{\rho}{A_x} \tag{7.17}$$

Step #9:

Total cupper losses are calculated in this step. Total resistance for the winding is expressed by equation 7.18.

$$\Omega_{Tot} = R_{unit} \times MTL \times N \tag{7.18}$$

Mean turn length is approximated by equation 7.19 for the C-core.

$$MTL = 2 \times (a + 2b + d) \tag{7.19}$$

Then it is 13.6 cm for AMCC-25 amorphous metal core. Hence, the coil resistance is for the inductor is 25.48 mΩ. Equation 7.20 gives total cupper losses in watts without regarding the skin effect.

$$P_{cu} = I_{rms}^2 \times \Omega_{tot} \tag{7.20}$$

Total cupper losses without including the skin effect is calculated nearly 5W by taking the rectifiers' input current, $I_{rms}$ in rms as 14 A.

Step #10:

The ac flux density in the air gap and the core is recalculated with regarding the corrected number of turns, N and air gap, $l_g$ by using the equation 7.21. $B_{ac}$ is calculated as 0.075 T by taking N, $\Delta I$, $l_g$ as 54, 4.22 A, 0.19 cm respectively.

$$B_{ac} = \frac{0.4 \times \pi \times N \times (\Delta I / 2) \times (10^{-4})}{l_g} \tag{7.21}$$

Step #11:

The core losses are recalculated by using the recalculated AC flux density in the air gap and the core. It is nearly 10 W by using equation 7.3 since the recalculated $B_{ac}$, switching frequency, $f_{sw}$, the core weight, $wt$ are 0.075 T, 50 kHz, 0.38 kg.

Step #12:

The estimated convective surface area for the C-core is calculated in this step. It is expressed in equation 7.22. Necessary parameters in this equation are given

before for the AMCC-25 core in step 3. Hence, it is 202.2 $cm^2$ for the core.

$$SA = 2f \times (b+d) + 2 \times (b+d) \times (b+e) + 2f \times (b+e) \tag{7.22}$$

Step #13:

Total power loss in the inductor is sum of the core and cupper losses and it is expressed in equation 7.23. Total power loss in the inductor is nearly 15 watts.

$$P_{tot} = P_{core} + P_{cu} \tag{7.23}$$

Approximate temperature rise in the inductor can be calculated by using the equation 7.24.

$$\Delta T = \left[ \frac{P_{tot}}{SA} \right]^{0.833} \tag{7.24}$$

In equation 7.24, total power loss in the inductor, $P_{tot}$ and $SA$ are in mW and $cm^2$ respectively. $\Delta T$ is temperature rise above the ambient temperature in $^0$C and nearly 36 $^0$C.

The inductor is designed by assuming that copper foil winding is used for the winding. However, the copper foil winding couldn't be used in the inductor because a copper foil with electrical insulation and specifications calculated above created practical problems. Litz wire, which has 10 wires with 0.7 mm diameter, is used instead of the copper foil. The Litz wire's copper cross-section is nearly 0.0385 $cm^2$. It is less than what is calculated above. On the other hand, the rectifiers' input current and current passing through the inductor is 14 A rms as stated in step 9. Thus, current density in the Litz wire is nearly 364 A/$cm^2$ for the inductor implemented. The Litz wire's total resistance, $\Omega_{Tot}$ is measured by a micro-ohm meter and it is 36 mΩ. Total copper losses are recalculated by using equation 7.20 and it is nearly 7 W. Sum of the core and copper losses is 17 W since the core losses is what is calculated in step 11. The approximate temperature rise is recalculated by using equation 7.24 and it is nearly 40 $^0$C. This temperature rise is lower than the maximum permissible temperature rise given in step 1. The implemented inductor has two coils with each one having 250 uH inductance and its total inductance is 500 uH. The inductance values are what are measured by RLC meter in a laboratory. Each part had 250 uH represents the L1 and L2 in figure 7.1. When the two parts is serially connected, it represents the $L_s$ in figure 6.7. It has 27 turns on one leg and 27 turns on the other leg of the AMCC-25 amorphous metal core.

### 7.2.2 Snubber Design

In power converters, power semiconductor devices can be under stresses beyond its ratings due to noise, voltage or current transients, etc. This problem can be solved by either using a power semiconductor with higher rating or using snubbers. In the proposed unity power factor rectifier circuit, snubbers are used only for the IGBT in implemented circuit .

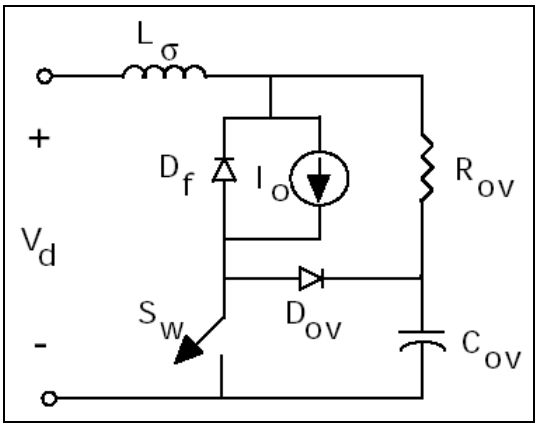
Snubber circuits are used with transistors to enhance their switching trajectory. Basic types of the snubbers[39] are:

- **Turn-off snubbers:** Turn-off snubbers are used for reducing the voltage stress across the transistor while the transistor turns off. There are various turn-off snubbers such as RCD, RC, C snubber.
- **Turn-on snubbers:** Turn-on snubbers are used for reducing the current stress over the transistor while the transistor turns on. It also reduces the voltage across the transistor during turn on. A simple turn-on snubber can be implemented by connecting a small inductance serially to the transistor. A large inductance causes lower turn-on voltages and lower turn-on losses. However, the large inductance causes overvoltages across the transistor and inceases the transistor's turn-off voltages.
- **Overvoltage snubber:** Stray inductances cause overvoltages across the transistor during the turn-off. It can be reduced by using a overvoltage snubber. It should be used with turn-off snubber.

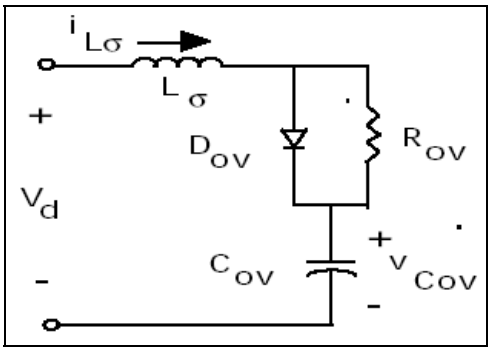
An overvoltage and turn-off, namely R-C snubber is used in the implemented rectifier.

#### 7.2.2.1 Overvoltage Snubber Design

Overvoltages across the transistor occur during the transistor turn-off due to stray inductances. In order to prevent the overvoltage, an overvoltage snubber as shown in figure 7.4(a) is used in the rectifiers' circuit [39,40].




**(a)**




**(b)**

**Figure 7.4** (a) Overvoltage snubber, (b) its equivalent circuit during transistor turn-off.

The switch, actually a switching transistor is conducting initially. Voltage across the capacitor, $C_{ov}$ is equal to $V_d$. During turn-off, the circuit in figure 7.4(a) is equal to the one in figure 7.4(b). The energy stored in stray inductance, $L_\sigma$ during the switch in conduction is transferred to $C_{ov}$ through the diode, $D_{ov}$. During this stage, the overvoltage across the switch, $\Delta V_{CE}$ is equal to voltage change across the capacitor, $\Delta V_{Cov}$. Hence [39, 40],

$$\frac{C_{ov} \times \Delta V_{CE,\max}^2}{2} = \frac{L_\sigma \times I_o^2}{2} \tag{7.24}$$

When the current through $L_\sigma$ is decreased and the current direction is reversed; the

overvoltage, $\Delta V_{CE}$ is diminishing and voltage across the capacitor, $C_{ov}$ becomes equal to $V_d$ by decreasing through the resistance, $R_{ov}$. Hence, recovery time of $C_{ov}$ must satisfy the following condition, where $t_{off\,(\min)}$ is minimum turn-off time of the transistor like an IGBT [39, 40].

$$2.3 \times R_{ov} \times C_{ov} \approx t_{off\,(\min)} \tag{7.25}$$

In $C_{ov}$ calculation, stray inductance, $L_\sigma$ value is not known and not measured; only it is taken 20 nH as in reference [40]. $C_{ov}$ is calculated as 343.75 nF by using equation 7.24, setting the $\Delta V_{CE}$ to 0.1 times the rectifiers' output voltage, taking $L_\sigma$ nearly 20 nH and $I_o$ equal to $I_{peak}$ (27.5 A as in inductor design stage). Its value is taken as 300 nF.

The UC3854B IC can gives PWM signals had up to 95 % duty cycle. In order to guarantee the recovery time of $C_{ov}$ through the resistance, $R_{ov}$, $t_{off\,(\min)}$ is calculated 0.5 μs by using equation 7.26 as if the maximum duty cycle, $D_{\max}$ is 97.5 %.

$$t_{off\,(\min)} = \frac{1 - D_{\max}}{f_{sw}} \tag{7.26}$$

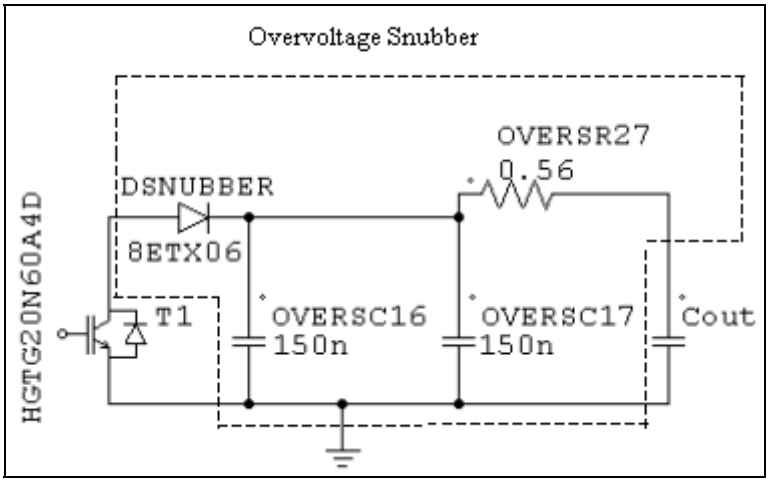



**Figure 7.5** Overvoltage snubber in implemented circuit.

The value of $R_{ov}$ is found as 0.724 Ω by using the equation 7.25. It is taken as 0.56 ohm. Power loss over the resistor is checked by making a simulation and it is nearly 0.5 W. However, 0.56 ohm, 5W power resistor is used in the overvoltage snubber circuit to prevent damage on the resistor due to possible excessive heat. International Rectifier's 8ETX06 ultrafast diode is used as snubber diode in the circuit and its datasheet is given in Appendix B. The implemented overvoltage snubber circuit whose block diagram is shown in figure 7.1 is given in figure 7.5.

#### 7.2.2.2 R-C Snubber Design

C snubber is simplest turn-off snubber and it is connected to paralel to the switching device. However, it can cause oscillations with stray inductances or inductance such as boost inductor in proposed rectifier or classical unity power factor rectifier. A series resistance to the capacitor is added to prevent the possible resonance and oscillations with the inductances. This snubber type is R-C snubber. There are other turn-off snubber types such as RCD snubber, but RC snubber is the simplest snubber type except C snubber to protect the IGBT from overvoltages during the turn-off [39, 44].

R-C snubber connected to a transistor with a stray inductance is shown in figure 7.6. The stray inductance, $L_\sigma$ causes an overvoltage during transistor turn-off since it is unclamped with the free-wheeling diode, $D_f$. This overvoltage is decreased to an acceptable level by the R-C snubber absorbing the energy associated with the stray inductance, $L_\sigma$ [39, 44].

R-C snubber optimal design curves are given in figure 7.7 [41]. R and C values in R-C snubber are calculated by using these curves based on the overshoot, $\hat{V}$ and initial current factor, $\chi$ [41].

$$C = L_\sigma \times (\frac{I_l}{\chi \times V_s})^2 \tag{7.27}$$

$$R = 2 \times \xi \times V_s \times \chi / I_l \tag{7.28}$$

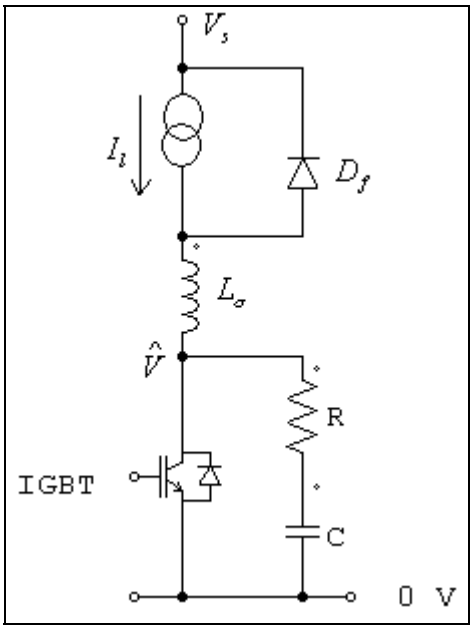



**Figure 7.6** R-C snubber connected to a transistor.

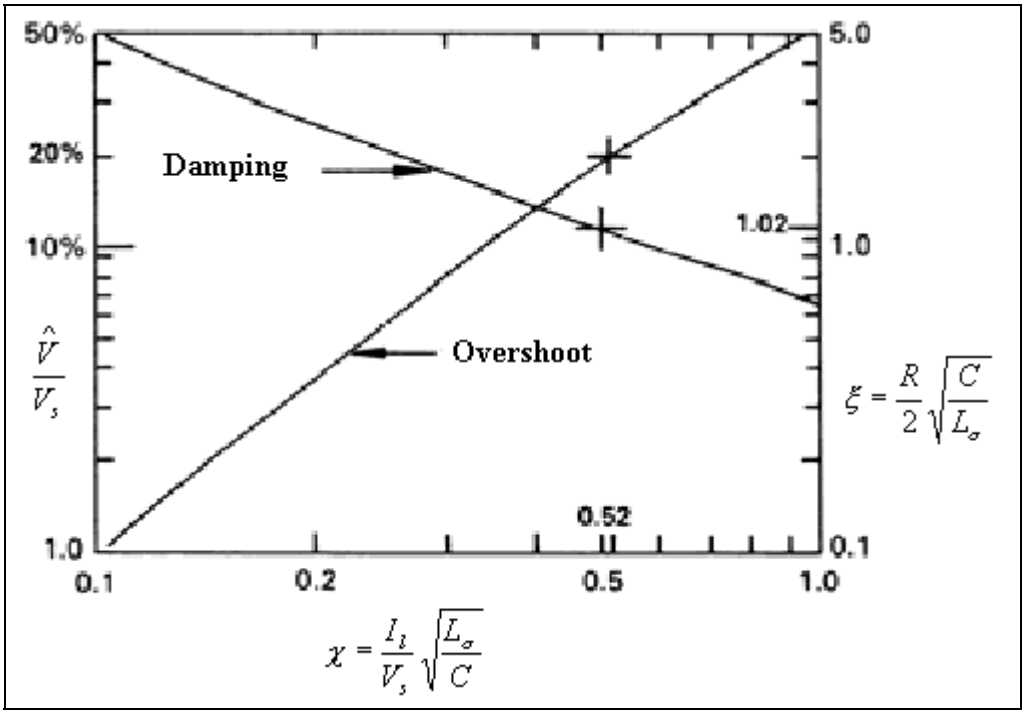



**Figure 7.7** R-C snubber optimal design curves.

The value of stray inductance, $L_\sigma$ is not known and it is assumed to be 20 nH. The overshoot, $\hat{V}$ is taken as 0.05 times the $V_s$ equal to 440 V for the rectifiers, so $\chi$ is nearly 0.25 according to figure 7.7. $I_l$ is taken as 27.5 A as the rectifiers' peak input current in inductor design stage in this chapter. Then, $C$ is calculated as 1.25 nF. In implemented circuit, two 400 V, 2.2 nF capacitors are serially connected to each other and it has 1.1 nF equivalent capacitance. $\xi$ is taken as 2 according to the curves. Then, equation 7.28 gives R as 16 ohm. Each 33 ohm two resistors are parallel connected to each other, their equivalent resistance is 16.5 ohm in the implemented circuit. Equation 7.29 gives the power loss on the resistor when the IGBT's fall time, $t_{fv}$ and rise time, $t_{rv}$ are higher than $R \times C$ time constant. Otherwise, the power loss on the resistor will be equal to $2P_{CO} + P_{LO}$ [41].

$$P_R = P_{Ron} + P_{Roff} = \frac{R \times C}{R \times C + t_{fv}} \times P_{CO} + \frac{R \times C}{R \times C + t_{rv}} \times (P_{CO} + P_{LO}) \tag{7.29}$$

$$P_{CO} = \frac{C \times V_s^2 \times f_{sw}}{2} \tag{7.30}$$

$$P_{LO} = \frac{L_\sigma \times I_l^2 \times f_{sw}}{2} \tag{7.31}$$

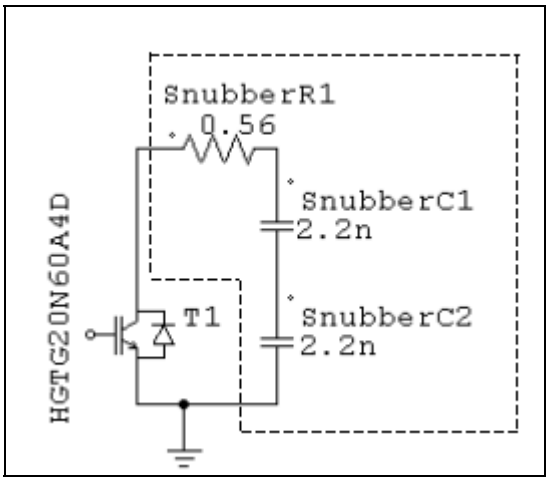


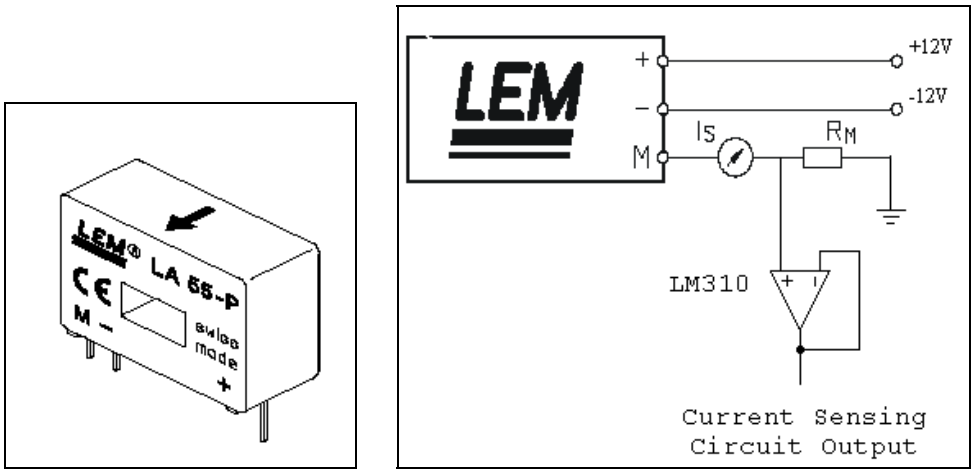

**Figure 7.8** R-C snubber circuit.

$P_{CO}$ and $P_{LO}$ are calculated as nearly 5.3 W and 0.38 W by using equation 7.30 and 7.31 and taking switching frequency, $f_{sw}$ 50 kHz. The IGBT used in implemented circuit has typical 13 ns rise and 55 ns fall times. Then, equation 7.29 gives the power loss on the resistor as nearly 4.6 W.

Each of the two resistors used in implemented circuit has 4W power rating and this is enough according to the calculations. The implemented R-C snubber circuit is given in figure 7.8.

### 7.2.3 Current Sensing Circuit

UC3854B power factor corrector integrated circuit needs a current feedback which represents the rectifiers' input current in rectified form. The current feedback can be taken by using current sense resistor if the rectifiers' input power are low such as 100 W, 250 W. If the rectifiers' input power are on the order of kilowatts, power consumed over the current sense resistor will be high, so the rectifiers' efficiency will be severely downgraded.




**(a)** **(b)**

**Figure 7.9** (a) LEM current sensor module, (b) current sensing circuit with the current sensor.

In order to prevent the efficiency downgrading severely, a current sensing circuit is used and its block diagram is shown in figure 7.1. LA 55-P/SP1 current sensor module is used in the current sensing circuit shown in figure 7.9(b) and its datasheet is given in Appendix A. A current carrying conductor is inserted in the current sensor module's hole shown in figure 7.9(a). In order to achieve best magnetic coupling, the conductor have to be wound over the top edge of the device according to its datasheet and this is what is done in the current sensing circuit implemented.

This current sensor output acts as a current source proportional to the current measured. A 40 ohm resistor is connected between ground and the sensor output. Voltage drop over the resistor gives voltage signal proportional the current sensed. This voltage is buffered by using LM310 voltage buffer in implemented circuit. The current sensing circuit whose block diagram is shown in figure 7.1 is given in figure 7.9(b). The implemented current sensing circuit's overall gain is 0.04.

### 7.2.4 Low Pass Filter and Mains Supply Feedback Circuit

Low pass filter and mains supply's sample blocks are shown in figure 7.1. $I_{ac}$ signal in figure 7.1 is a current signal proportional to mains supply's voltage and in rectified form. The control circuit with the power factor corrector IC forces the rectifier's input current to follow the $I_{ac}$ signal waveshape. $V_{rms}$ is also mains supply's voltage sample in rectified form. Low pass filter in the block diagram is necessary to filter the harmonics in the line voltage. In order to reduce the effects of harmonics to produced PWM signal, $V_{rms}$ is taken from the low pass filter. On the other hand, a unity power factor rectifier design with some different PFC ICs such as UCC3818 needs different low pass filter. The low pass filter and its design are specific to UC3854B IC. Thus, its design is not given here. The application note in Appendix A should be used for a low pass filter design in circuits contain the IC. This extra circuitry with MULTIPLIER DIVIDER SQUARER block is needed to keep the rectifier's power constant irrespective of the input voltage changes and this is explained in chapter 6 in detail.

Proposed rectifiers' low pass filter design with UC3854B and the application note, and where mains supply's voltage sample is taken somewhat differ from the classical unity power factor rectifier's one which is given straight forward in the application note. The differences are:

- Mains supply's sample block in figure 7.1 contains the proportional block, K2, whose output is $I_{ac}$ current signal. Its input and output signals are voltage and current signal respectively, so it is accomplished by using a resistor in implemented circuit. The resistor has 65 kΩ resistance in proposed rectifier circuit and 650 kΩ resistance is used in classical unity power factor rectifier circuit because the sample is taken by using a 10:1 transformer as shown in figure 7.10 in the proposed rectifier circuit. In order to prevent the $I_{ac}$ current signal to be affected by the capacitances in the low pass filter in figure 7.11, a diode is placed between the resistor and the low pass filter. The diode, namely 1N4004's datasheet is given in Appendix B.

  The transformer, named reference transformer inputs are connected to mains supply. An R-C low pass filter, whose cut-off frequency is 10 kHz is connected to its output to decrease the possible noise that is comming from the rectifiers' other parts as shown in figure 7.10.

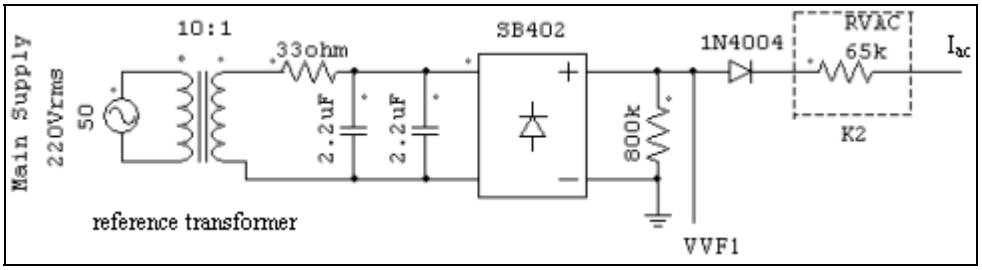



**Figure 7.10** Circuit of mains supply's sample block in implemented circuit.

- The voltage signal, VVF1 in implemented circuit over RFF1NEW in figure 7.11 is taken by using a 10:1 transformer and a diode bridge, namely SB402,

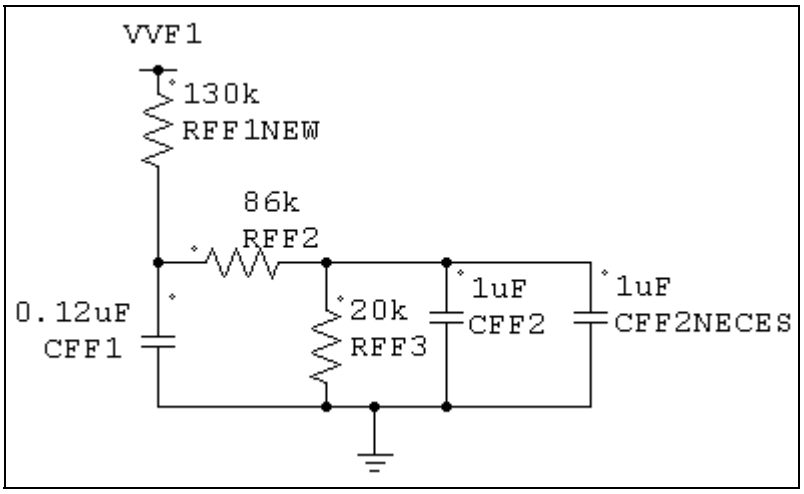



**Figure 7.11** Low pass filter in proposed rectifier circuit.

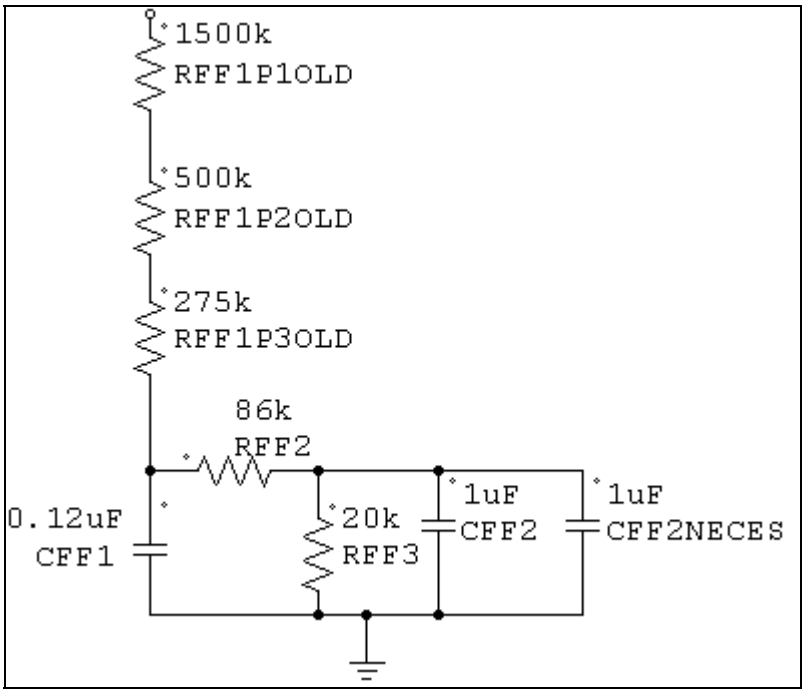



**Figure 7.12** Low pass filter in classical unity power factor rectifier.

whose datasheet is given in Appendix B. Hence, this have to be considered when their values are calculated by using the application note. This signal's voltage value have to be used in their calculations. Two capacitors, CFF2 and

CFF2NECES's equivalent capacitance is important in this figure. Their equivalent capacitance and CFF1's capacitance values are depends upon the values of the resistors, RFF2 and RFF3. This should be cared about.

For the conventional rectifier configuration, it is possible to take the voltage feedback from a transformer and use the low pass filter in figure 7.11. However, these may affect the conventional rectifier performance negatively. This is given in detail in section 6.4.3. Hence, the low pass filter in figure 7.12 is required for better performance for the conventional rectifier configuration and the voltage feedback is taken and the low pass filter in the figure is connected as in figure 6.7. RFF1P1OLD, RFF1P2OLD and RFF1P3OLD's equivalent resistance is important in the figure. The equivalent resistance and RFF1NEW in figure 7.11 are different. Calculated values of RFF2, RFF3 is same for the two rectifiers' control circuit, so the ones of CFF1, CFF2 and CFF2NECES. The rest of the capacitances and resistances is same for the two rectifiers.

### 7.2.5 Control Circuit

The control block contains the current error amplifier, voltage error amplifier and PWM block. In order to obtain the sinusoidal input current nearly in phase with the rectifier's input voltage and DC output voltage at its output side, the control circuit gives necessary PWM signals to the IGBT.

Necessary circuit to implement the PWM block is inside the UC3854B IC. Hence, the circuit is not given here. The IC datasheet is given in Appendix B. The circuit converts the signal coming from the current error amplifier to PWM signals and the PWM signals are given to the IGBT's gate pin.

Current error amplifier and voltage error amplifier are originally simple integrator implemented by using an opamp. The simple integrator is shown in figure 7.13. The integrator's transfer function is given in equation 7.32.

$$G(s) = \frac{1}{s \times R_{ci} \times C_{cp}} \tag{7.32}$$

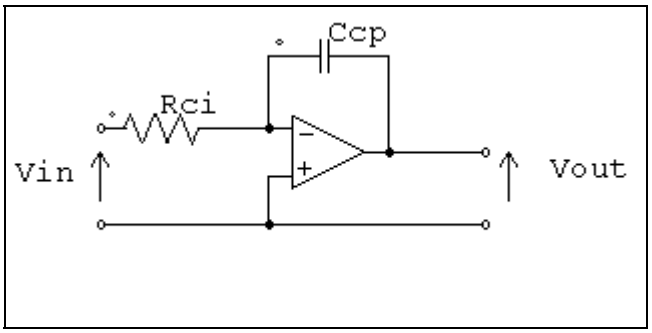



**Figure 7.13** An integrator.

In order to increase a unity power factor rectifier's performance, which uses average current control, a pole and a zero are added the transfer function in equation 7.32. Then, the transfer function will be as in equation 7.33 [43].

$$G_{ca}(s) = \frac{1}{R_{ci} \times C_{cp}} \times \frac{s + \omega_z}{s \times (s + \omega_p)} \tag{7.33}$$

, where $\omega_z = \frac{1}{R_{cz} \times C_{cz}}$ and $\omega_p = \frac{C_{cz} + C_{cp}}{R_{cz} \times C_{cz} \times C_{cp}}$.

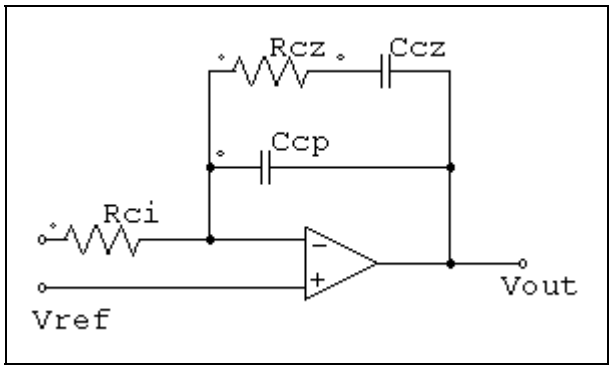



**Figure 7.14** Error amplifier with compensator.

The transfer function in equation 7.33 consists one integrator ($1/s$), one zero at $\omega_z$ and one pole at $\omega_p$. The integrator eliminates steady state error. The zero is used for guaranteeing the stability of the rectifier's input current, and the pole eliminates high frequency noise due to the power transistor's switching in the rectifier. The zero should be set to $f_{sw}/2\pi$ [43], the pole must be above $f_{sw}/2$ according to the application note in Appendix A. The current error amplifier has a zero at nearly 7900 Hz, and a pole at 50 kHz and its gain is nearly 7.4 in implemented circuit. It is shown in figure 7.15.

Though current error amplifier and voltage error amplifier can be implemented with same type of error amplifier, the pole and zero must be set at different frequencies [43].

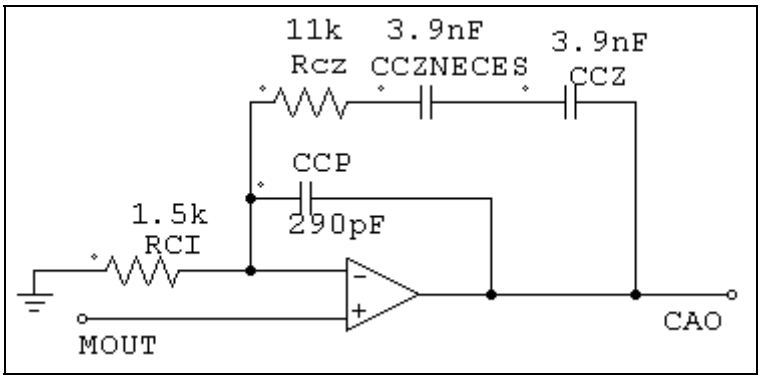



**Figure 7.15** Current error amplifier in implemented circuit.

The voltage error amplifier has a pole at nearly 12 Hz, a zero at a $10^{th}$ of the pole frequency in implemented circuit and its gain is nearly 0.008. It is shown in figure 7.16. The resistors, R9 and R10's total resistance in figure 7.16 represents the $R_{ci}$ in figure 7.14. The total resistance and R6 in figure 7.16 form a voltage divider. In this way, the rectifier's output voltage is sensed. The opamps in figure 7.15 and 7.16 are in UC3854B IC and the other electrical components are connected to the IC.

The current error amplifier forces the rectifier's input current to become

nearly in phase with the input voltage while the voltage error amplifier forces the rectifier's output voltage to be DC voltage. The voltage error amplifier gain must be much more less than the current error amplifier gain to decrease the effect of the output voltage ripple to the input current's THD. A detailed description is given in Appendix A.

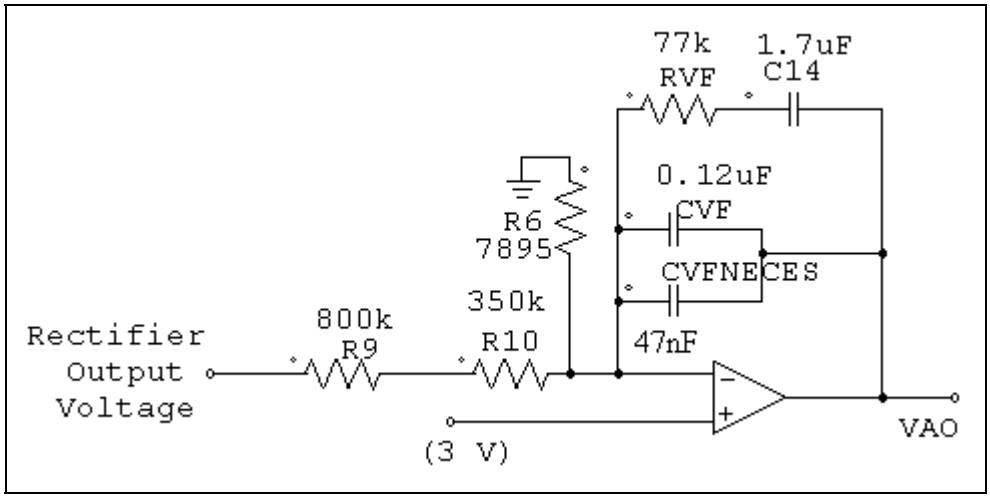



**Figure 7.16** Voltage error amplifier in implemented circuit.

### 7.2.6 Power Supply Block

LEM current sensor, LM310 buffer and UC3854B IC needs DC supply voltages. The DC supply produced +18 V, +12 V and –12 V DC voltages is given in figure 7.17. The connector, named SUPPLYTRANSOUTPUT's inputs are connected a 5 W transformer which has two +25 V and 0 V outputs. One 0 V and +25 V is shorted to each other. These are used as grounding purpose and also these are shorted to earthground. The other +25 V and 0 V output are connected to diode bridge. The tranformer input is also connected to mains supply.

LM7812, LM7912 and LM7818 are used for producing +12 V, -12 V, +18 V respectively. Their datasheets is given in Appendix A. +12 V and –12 V supplies are used for giving necessary supply voltages to the LEM current sensor and LM310

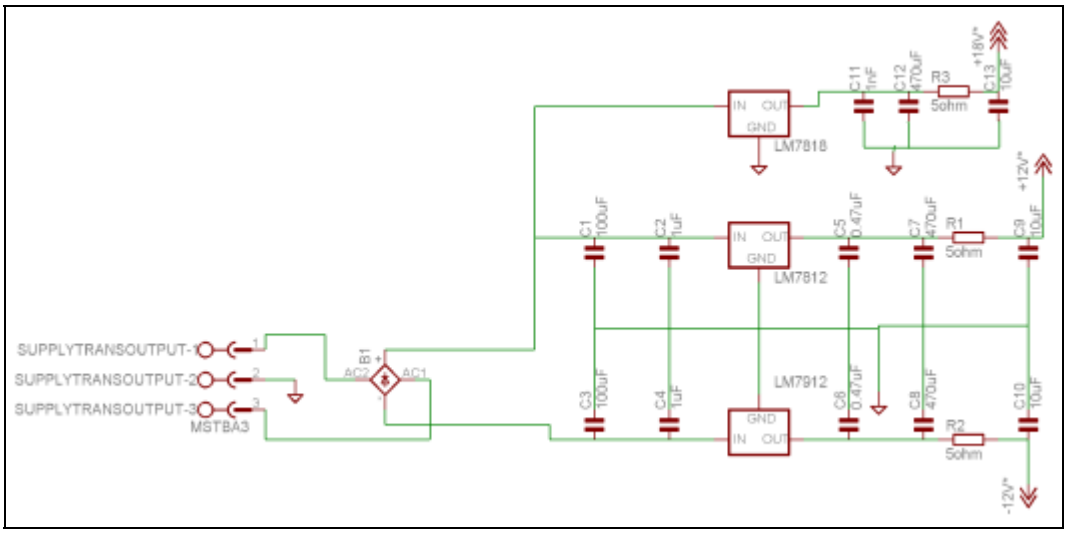



**Figure 7.17** Power supply which produces +12 V, -12 V, +18 V DC voltage.

buffer. UC3854B is supplied by the +18 V.

R1 and C9 form a low pass filter whose cut-off frequency is nearly 3.1 kHz and it is used to prevent 10 kHz noise coming from the LM7812 IC to pass through the +12 V supply output. The detailed descriptions about the noise is found from its datasheet in Appendix B. Similarly, R2 and C10, R3 and C13 are used for -12 V and +18 V supply and same reason.

### 7.2.7 Proposed Topology Block

Proposed topology block in figure 7.1 contains the inductors, L1 and L2, the ultrafast diodes D3, D5, bridge diodes, D1, D2, D6, D7, a switching transistor, output capacitor, $C_{out}$. Information about the inductors and their design stage are given in section 7.2.1. The power semiconductors are selected in chapter 6 and why they are selected are given in the chapter. Fairchild Semiconductor's RURG5060 ultrafast diodes are used as the ultrafast diodes. Its average rectified forward current rating is 50 A at case temperature of 102 $^0$C and its voltage rating is 600 V. The diodes, D1,

D2, D6 and D7 form a diode bridge and IXYS VBO 30-12N07 diode bridge module is used instead of these diodes. The bridge diode module has 35 A average current rating and 1200 V maximum voltage stress. Fairchild HGTG20N60A4D IGBT is used as the switching transistor. Its voltage rating is 600 V. It has maximum 40 A continuous collector current rating at case temperature of 110 $^0$C. However, its current rating downgrades to 37 A at 50 kHz switching speed and junction temperature of 125 $^0$C. The power semiconductor's datasheets are given in Appendix B.

### 7.3 Proposed Rectifier And Classical UPF Rectifier's Schematic Diagram

The proposed rectifier and classical unity power factor rectifier are simulated by using average current control technique in chapter 6. The two rectifiers' control circuit can be implemented in the same printed circuit board since the same current control technique and same power factor corrector integrated circuit is used in the two boost rectifiers. This is what is done in this thesis work.

Implemented proposed rectifier and classical unity power factor rectifier's schematic diagram is given in same schematic diagram in this section. The schematic diagram is splitted in to two parts and they are given in figure 7.18 and figure 7.19. The boost inductor and output capacitor are placed outside the printed circuit board and so the schematic. They are connected in the rectifiers' circuit according to figure 6.7 and 6.8.

The output capacitor is charged initialy by using 200 ohm, 200 W power resistor and it is disconnected from the circuit by using a power switch manually. A load is connected after the capacitor is fully charged and the voltage upon the capacitor is reached the specified output voltage given in chapter 6. A circuit for automatically disconnecting the charging resistance is also designed. However, it is not tested in this thesis work and it is not shown in the schematic. On the other hand, it is shown in the printed circuit board given in figure E.1 in Appendix E.

Passing from classical unity power factor rectifier's control circuit to proposed rectifier's one is achieved by using and connecting jumpers to connectors,

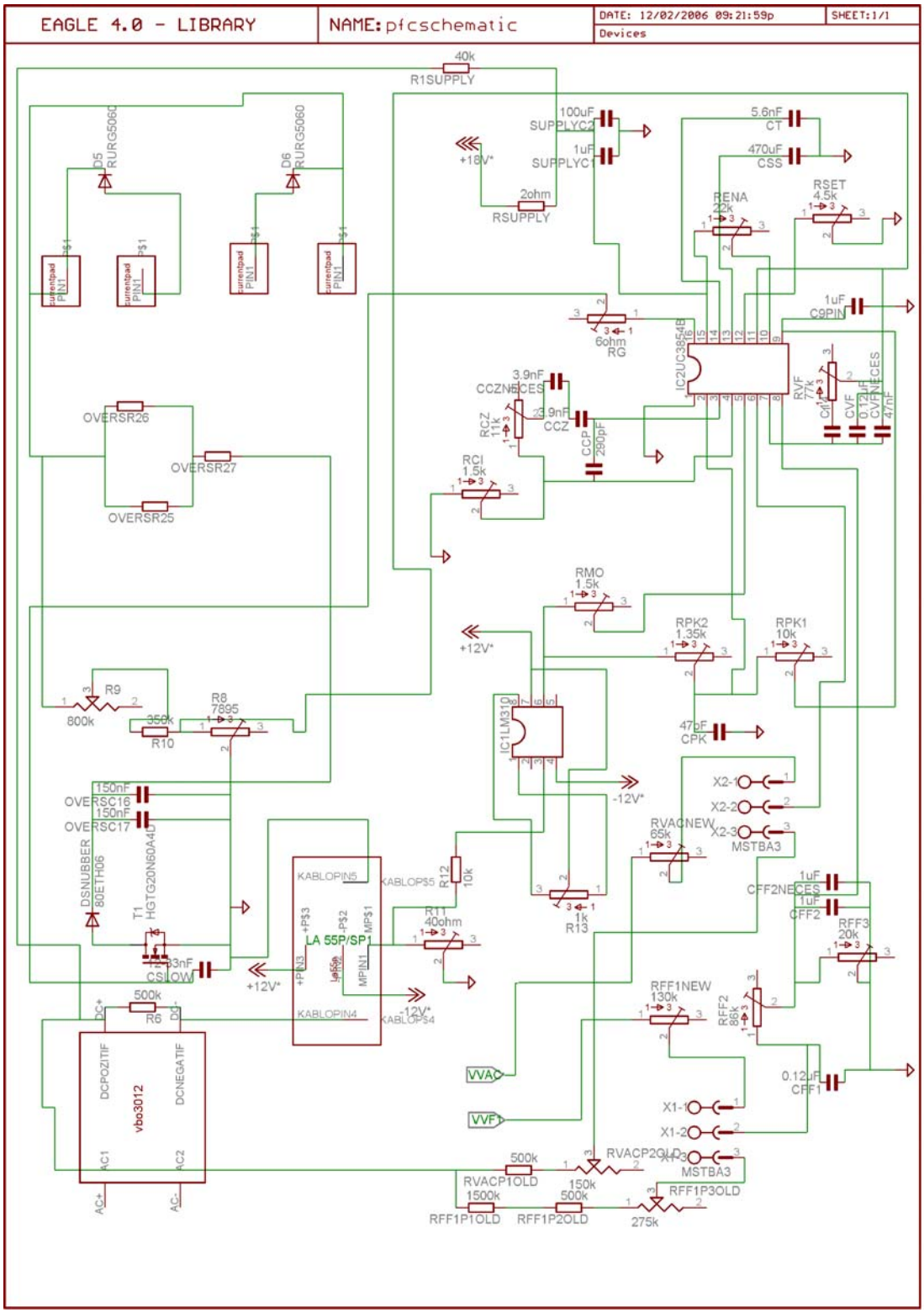



**Figure 7.18** The proposed and classical unity power factor rectifier PCB schematic not including +12 V, -12 V, +18 V supply voltages and reference voltages, VVAC and VVF1.

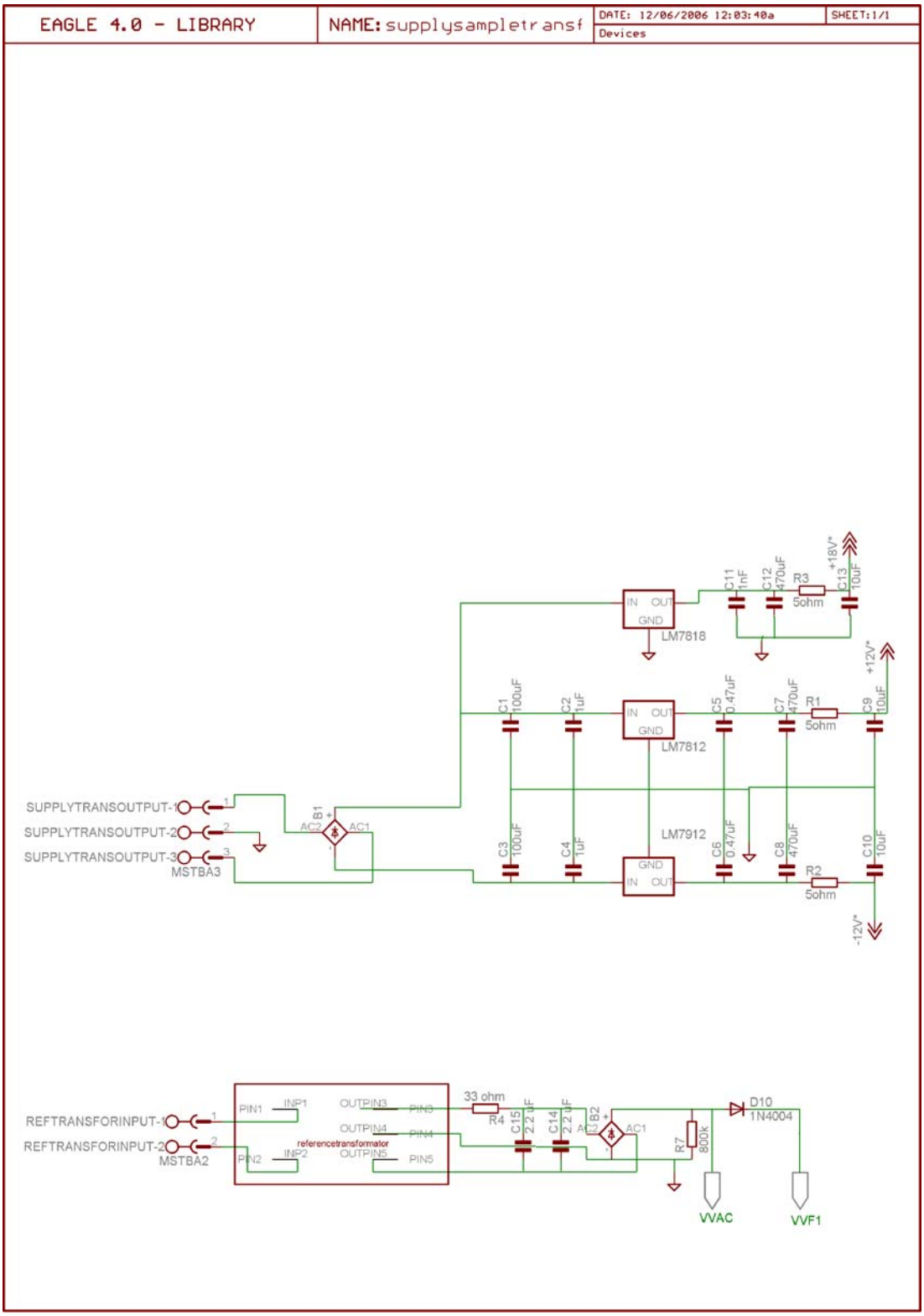



**Figure 7.19** Printed circuit board schematic shown +12 V, -12 V, +18 V voltage supply and reference voltages, VVAC and VVF1 proportional to the mains supply in rectified form.

X1 and X2 shown in figure 7.18 manually. The proposed rectifier's control circuit works, when pins, X1-1, X1-2 are shorted to each other; and X2-1, X2-2 are connected to each other by using jumpers. On the other hand, when X1-2, X1-3 are connected to each other, and X2-2, X2-3 are shorted to each other; classical unity power factor rectifier's control circuit is established.

The rectifiers' printed circuit board is given in figure E.1. Its top and bottom layers are shown in figure E.2 and figure E.3.

## 7.4 Experimental Results And Comparison With Simulations In Same Conditions

In this section, proposed rectifier circuit implemented is tested in laboratory and the results are given. The proposed rectifier is tested by connecting 1 kW and 2 kW resistive loads. Nearly unity power factor in mains supply side and DC voltage at the output side are achieved . The rectifier's output voltage ripple, FFT (Fast Fourier Transform) up to $50^{th}$ harmonic and THD (Total Harmonic Distortion) of input current are given.

The rectifier's input current harmonics are measured by HIOKI 3194 Motor/Harmonic Hi Tester. It shows the harmonics up to $50^{th}$ harmonic. Also, the FFT waveform is obtained by Agilent 100 MHz DSO6014A scope. Important harmonics near the rectifier's switching frequency is obtained by using the FFT waveform and the important harmonics and the harmonics up to $50^{th}$ harmonic measured by the HIOKI 3194 together with the harmonics obtained via simulation are given in a table. On the other hand, HIOKI 3194 is capable of measuring THD by considering first 3000 harmonics. The tester measures the harmonics more precisely than the scope's FFT measurement option. Hence, the THD measured by the tester is more reliable. This is also given in this section.

Simulations are made in same conditions with experiments to identify whether the results taken in laboratory is similar or not. In simulation circuit, R-C snubber and overvoltage snubber designed are connected to the IGBT. However, fall time and rise time parameters can not be entered in power semiconductors parameter

part in PSIM 6.1 simulation software, but their conduction voltage drop parameters are used in the simulations. Also, UC3854 B IC model in figure 6.1 is used in these simulations. Simulation time step is taken as 1E-007. Also, ideal inductors are used in the simulations.

### 7.4.1 Proposed Rectifier's Experimental Results With 1 kW Resistive Load And Comparison With Simulation In Same Conditions

Proposed rectifier is tested by connecting 1 kW nearly purely resistive load. Its input current, input voltage and output voltage waveform is acquired by using Agilent DS06014A oscilloscope. Its input power, power factor, input rms current, input rms voltage, output power, output mean voltage, output rms current and input current harmonics up to $50^{th}$ harmonic are measured by using HIOKI 3194 Motor/Harmonic Hi Tester. The results are given below.

Figure 7.20 shows the rectifier's input voltage in green color and input current in yellow color. The waveforms are acquired by using the scope in real time mode, a current probe and differential probe. There are voltage ripples on the input voltage due to the IGBT switching at 50 kHz. The input current waveshape and the ripples on it are due to nature of the average current control technique used in implemented circuit. The recording in figure 7.20 shows that the input voltage and current are nearly in phase. Hence, nearly unity power factor operation is achieved.
The rectifier's input current, voltage, input power and power factor are measured as 4.7590 A rms, 219.49 V rms, 1044.6 VA and 98.7 % respectively by HIOKI 3194 Motor/Harmonic Hi Tester. Its output power is also measured by same equipment and is 1004.8 W. Therefore; the rectifier's efficiency is nearly 96.2 % at steady state.

The rectifier's output voltage is measured by the scope in the averaging mode. It is shown in green color in figure 7.21. Also, the input current measured in averaging mode is shown in yellow color in the figure. The output voltage swings between maximum 437.8 V and minimum 433.5 V at steady state. Its output voltage ripple is calculated by dividing the difference between the maximum and minimum voltages to the rectifier's average output voltage. The output voltage ripple is less

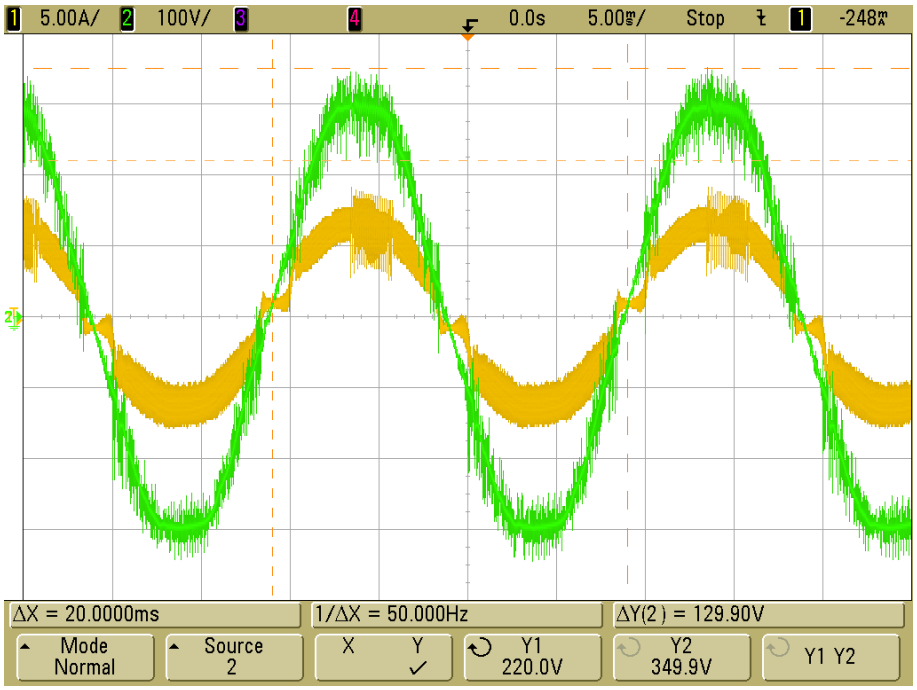



**Figure 7.20** Proposed rectifier's input current and input voltage waveform with 1 kW nearly purely resistive load.

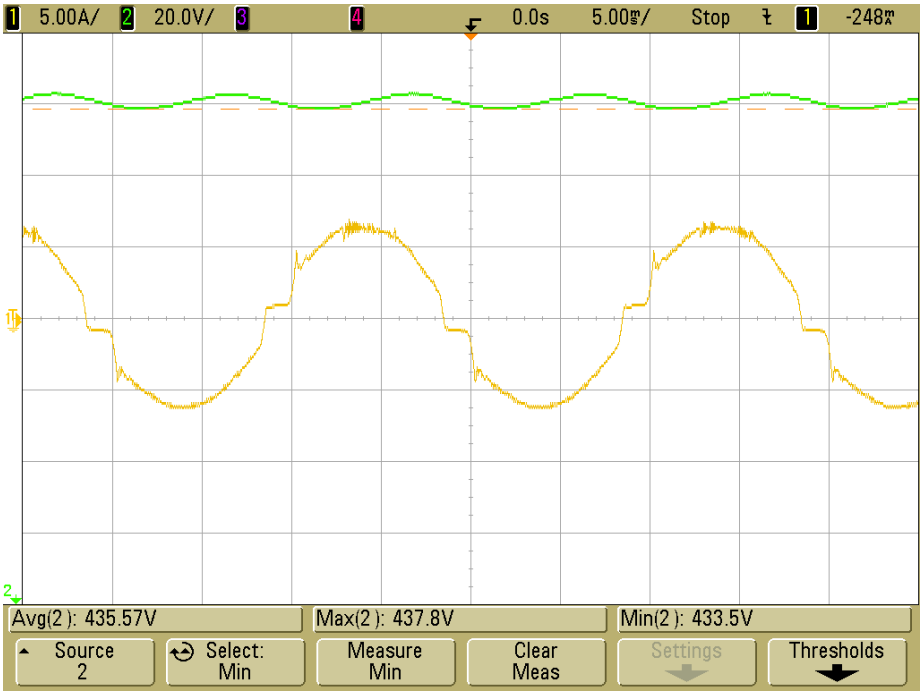



**Figure 7.21** Proposed rectifier's input current and input voltage waveform at 1 kW nearly purely resistive load.

than 1 % (0.99 %) according to the figure 7.21.

The rectifier's input current harmonics up to 50$^{th}$ are measured by HIOKI 3194 Motor/ Harmonic Hi Tester and they are given in table 7.3. The input current's FFT is obtained by using the scope at its 50 kHz center frequency and given in figure 7.22. Note that these harmonic numbers correspond to about 50 kHz switching frequency. The harmonics had relatively higher magnitudes near the switching frequency are obtained by using the FFT waveform and given also in this table. They are 997 and 999$^{th}$ harmonics and their magnitudes are relatively higher than the nearest harmonics and their magnitudes are shown in figure 7.22.

The input current's THD is calculated as 6.91 % from the equation 6.1 and the data correspond to the measurement in table 7.3. The THD is measured as 15.37 % by using the HIOKI 3194 Motor/Harmonic Hi Tester and considering up to first 3000$^{th}$ harmonics. This result indicates that for accurate prediction of THD, it is essential to consider all the harmonics up to the switching frequency.

The proposed rectifier is simulated by using PSIM simulation program and connecting 1 kW purely resistive load to the rectifier's output. Its input current and input voltage waveform are given in figure 7.23.

The rectifier's input current and input voltage are 4.85 A rms and 219.2 V rms according to the figure 7.23. Its input power and power factor are obtained by using " power factor meter" block in the PSIM simulation program. They are 1062.5 VA and 97.3 % respectively.

Figure 7.24 shows its output voltage with the mentioned conditions. Its steady state maximum, minimum and average output voltages are 436.98 V, 431.54 V and 434.28 V respectively. Hence, its output voltage ripple is 1.25 %. Its output power is obtained by using wattmeter block in the PSIM simulation program and it is 1011.9 W. Its efficiency is 95.24 % since its input power is 1062.5 VA.

The rectifier's input current harmonics up to 50$^{th}$ harmonic and the harmonics had high magnitudes near the switching frequency are obtained by using PSIM 6.1 simulation program and they are also listed in table 7.3.

The relevant FFT waveforms are given in figure 7.25. THD of the input current is calculated by using equation 6.1, the data in table 7.3 in simulation and it is nearly 22.28 %. THD of the input current is also calculated by using THD block in PSIM 6.1 and it is nearly 23.9 %. The THD block in PSIM 6.1 considers the input

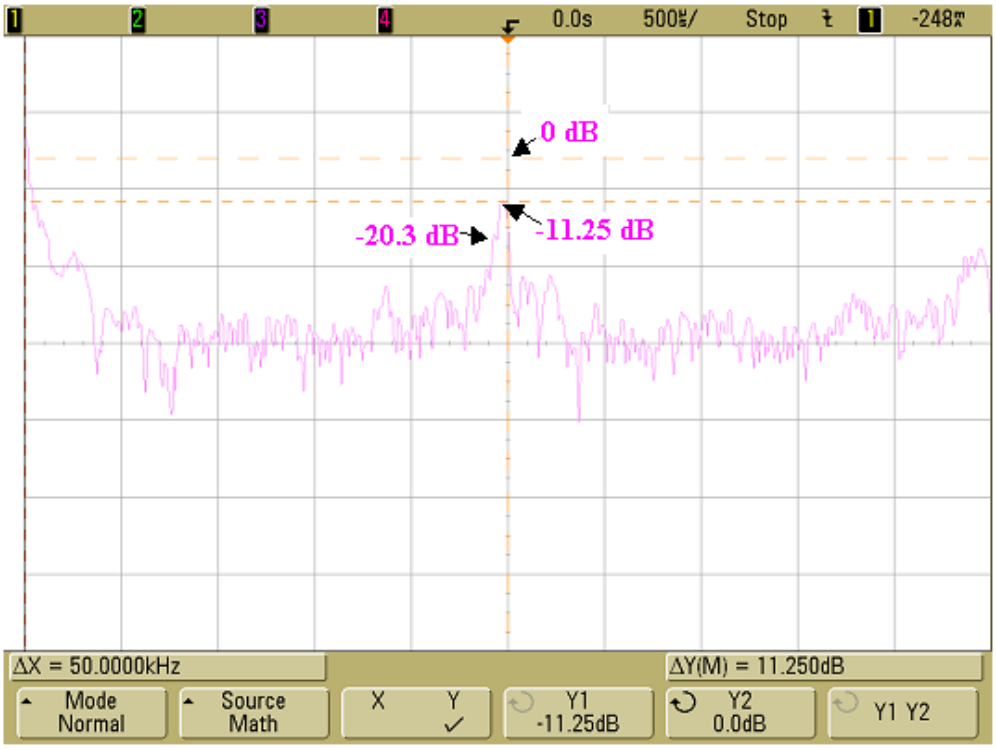



**Figure 7.22** FFT of proposed rectifier's input current when 1 kW purely resistive load is connected to the rectifier's output and 100 MHz DSO6014A scope's scale, offset, span, center frequency and sample rate are 20 dB/division, –48 dB, 100 kHz, 50 kHz and 200 kSa/s respectively.

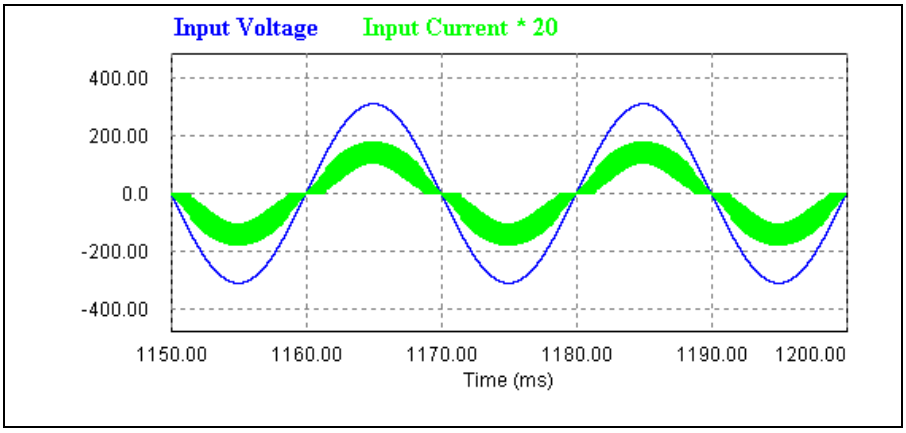



**Figure 7.23** Proposed rectifier's input current and input voltage waveform obtained using PSIM 6.1 simulation program at steady state when 1 kW purely resistive load is connected.

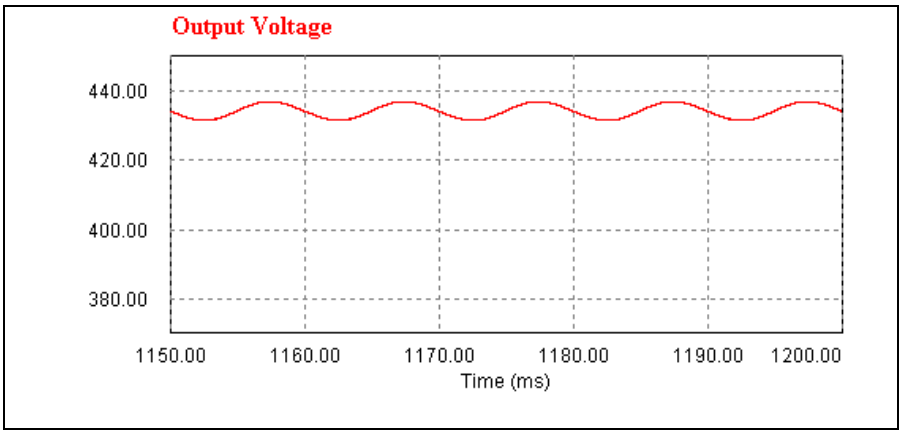
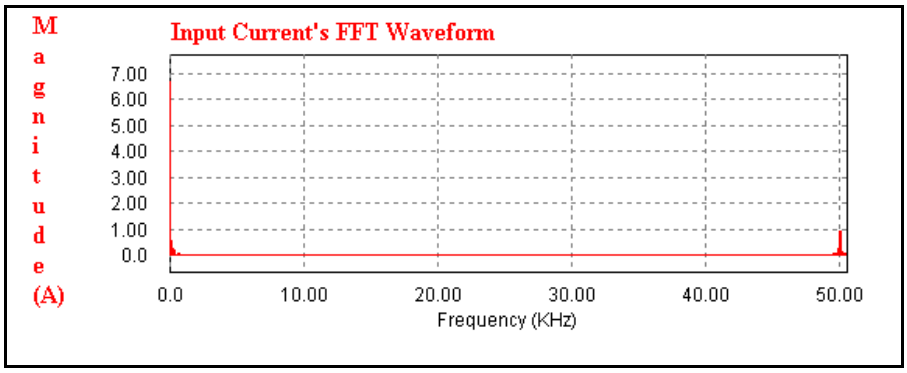
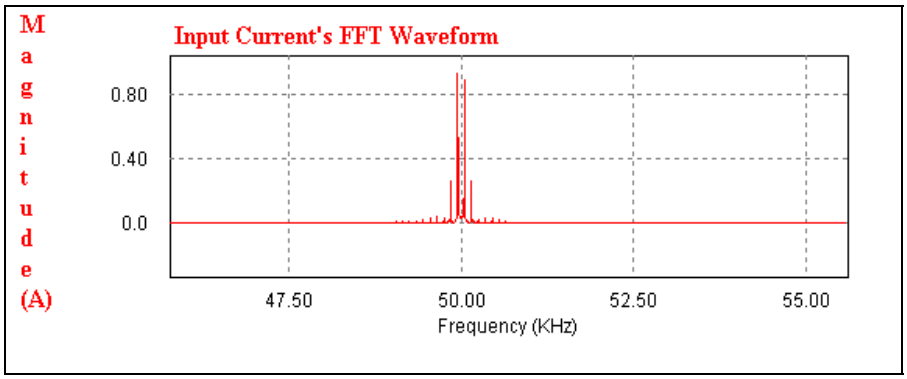



**Figure 7.24** Proposed rectifier's output voltage waveform obtained using PSIM 6.1 simulation program at steady state when 1 kW purely resistive load is connected.




**(a)**




**(b)**

**Figure 7.25** (a) FFT waveform of proposed rectifier's input current obtained using PSIM 6.1 simulation program between 0 and 50500 Hz at steady state when 1 kW purely resistive load is connected, (b) the FFT waveform between 47 and 55 kHz.

| | Measured | Simulation | | Measured | Simulation |
|---|---|---|---|---|---|
| **Harmonic #** | **Magnitude (A)** | **Magnitude (A)** | **Harmonic #** | **Magnitude (A)** | **Magnitude (A)** |
| **1** | 6.5288 | 6.667 | **28** | 0.0031 | 0.000 |
| **2** | 0.0368 | 0.000 | **29** | 0.0257 | 0.022 |
| **3** | 0.2560 | 0.549 | **30** | 0.0054 | 0.000 |
| **4** | 0.0118 | 0.000 | **31** | 0.0308 | 0.012 |
| **5** | 0.1539 | 0.233 | **32** | 0.0068 | 0.000 |
| **6** | 0.0262 | 0.000 | **33** | 0.0695 | 0.006 |
| **7** | 0.1498 | 0.166 | **34** | 0.0084 | 0.000 |
| **8** | 0.0083 | 0.000 | **35** | 0.0683 | 0.018 |
| **9** | 0.2632 | 0.081 | **36** | 0.0060 | 0.000 |
| **10** | 0.0079 | 0.000 | **37** | 0.0606 | 0.018 |
| **11** | 0.2556 | 0.010 | **38** | 0.0061 | 0.000 |
| **12** | 0.0083 | 0.000 | **39** | 0.0267 | 0.007 |
| **13** | 0.2033 | 0.040 | **40** | 0.0063 | 0.000 |
| **14** | 0.0054 | 0.000 | **41** | 0.0278 | 0.008 |
| **15** | 0.1290 | 0.044 | **42** | 0.0058 | 0.000 |
| **16** | 0.0044 | 0.000 | **43** | 0.0380 | 0.015 |
| **17** | 0.0350 | 0.020 | **44** | 0.0068 | 0.000 |
| **18** | 0.0060 | 0.000 | **45** | 0.0421 | 0.012 |
| **19** | 0.0562 | 0.013 | **46** | 0.0060 | 0.000 |
| **20** | 0.0054 | 0.000 | **47** | 0.0364 | 0.002 |
| **21** | 0.0943 | 0.028 | **48** | 0.0058 | 0.000 |
| **22** | 0.0076 | 0.000 | **49** | 0.0128 | 0.011 |
| **23** | 0.1157 | 0.022 | **50** | 0.0054 | 0.000 |
| **24** | 0.0050 | 0.000 | **997** | 0.0966 | 0.267 |
| **25** | 0.0955 | 0.003 | **999** | 0.2738 | 0.934 |
| **26** | 0.0033 | 0.000 | **1001** | | 0.893 |
| **27** | 0.0546 | 0.018 | **1003** | | 0.260 |

**Table 7.3** Proposed rectifier's input current harmonics up to 50$^{th}$ harmonic measured by using HIOKI 3194 Motor/Harmonic Hi Tester, 997$^{th}$ and 999$^{th}$ harmonic obtained by DSO6014A scope and the input current harmonics up to 50$^{th}$ harmonic and the harmonics had higher magnitudes near the 50 kHz switching frequency obtained by PSIM 6.1 simulation program with 1 kW load at steady state.

current's all harmonics in the calculation.

Important harmonics correspond to measurement part in table 7.3 are between 1$^{st}$ and 25$^{th}$ harmonic and near the 50 kHz switching frequency while the important harmonics correspond to simulation part are between 1$^{st}$ and 9$^{th}$ harmonic and near the switching frequency except even harmonics. The all even harmonics' magnitudes are very small for the parts correspond to the simulation and measurement part in table 7.3. The 1$^{st}$ harmonics in simulation part and the one in measurement part in

table 7.3 have similar magnitudes, but the other harmonics somewhat differ in the two part in this table due to non ideal behaviors of the mains supply and electrical components in the implemented circuit.

### 7.4.2 Proposed Rectifier's Experimental Results With 2 kW Resistive Load And Comparison With Simulations In Same Conditions

Similarly, the proposed rectifier is tested by connecting 2 kW nearly purely resistive load and using same test equipments in the laboratory enviroment. Its input current, input voltage and output voltage waveform, input power, power factor, input rms current, input rms voltage, output power, output mean voltage, output rms current and input current harmonics up to fifth harmonic are obtained in the laboratory.

The rectifier's input voltage in green color and input current in yellow color obtained by using scope are shown in figure 7.26. Its input current and voltage are 9.689 A rms and 218.99 V rms. Also, its input power and power factor are 2120.8 VA and 99.13 % respectively. These measurements are made by HIOKI Hi Tester. The rectifier's efficiency is 95.63 % because its output power is 2028.3 W at steady state.

The rectifier's output voltage in green color and input current obtained by using the scope in averaging mode are shown in figure 7.27. The output voltage has maximum 438.5 V, minimum 429.0 V and average 433.6 V values. Its output voltage ripple is about 2 % (2.19 %) and it is calculated similarly as in section 7.5.1.

The input current's FFT waveform is given in logarithmic scale in figure 7.28 and the harmonic that has relatively higher magnitude near the switching frequency is marked in the figure. The harmonic and first 50 harmonics measured with HIOKI 3194 are given in table 7.4 in measurement part. The harmonic corresponding to about 50 kHz switching frequency is $999^{th}$ harmonic and its magnitude is 0.328 A.

THD of the rectifier's input current is calculated as nearly 8.72 % by using equation 6.1 and the values listed in table 7.4 in measurement part. The THD is more precisely measured as 11.95 % by using the HIOKI 3194 Motor/Harmonic Hi Tester

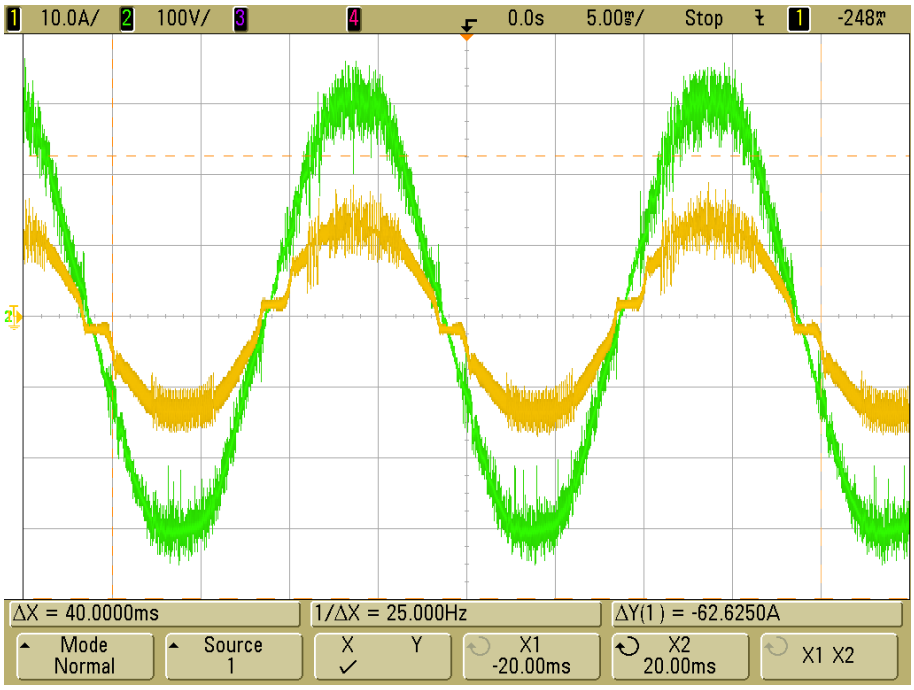



**Figure 7.26** Proposed rectifier's input current and input voltage waveform with 2 kW nearly purely resistive load.

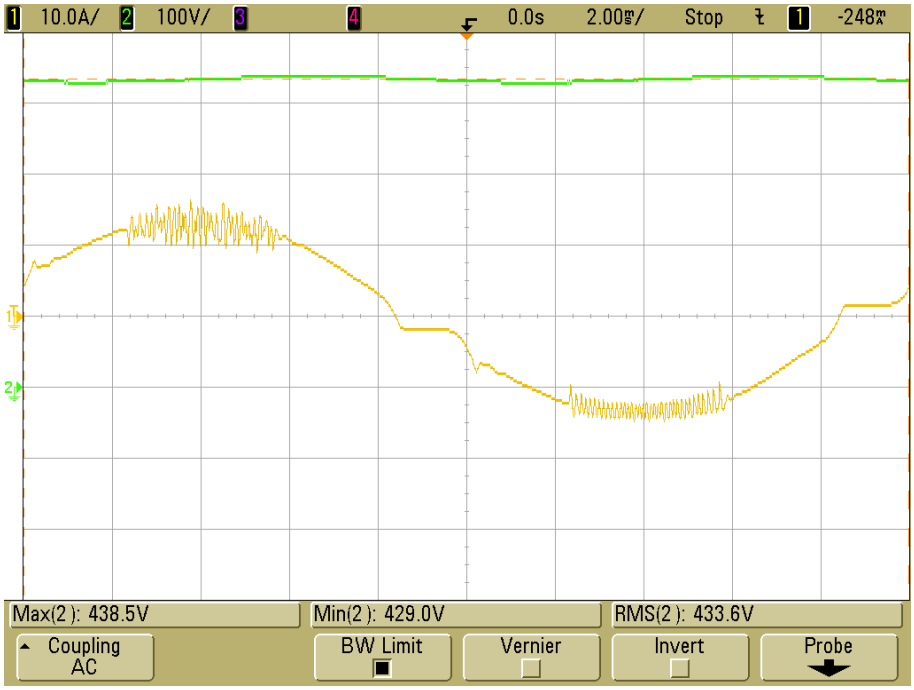



**Figure 7.27** Proposed rectifier's input current and input voltage waveform with 2 kW nearly purely resistive load.

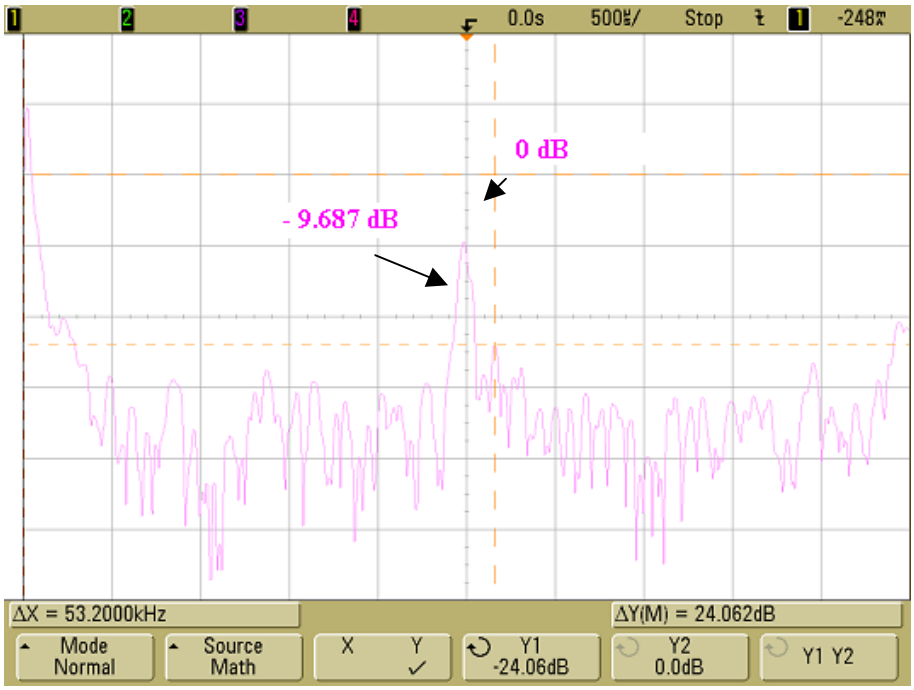



**Figure 7.28** FFT of proposed rectifier's input current when 2 kW purely resistive load is connected to the rectifier's output and 100 MHz DSO6014A scope's scale, offset, span, center frequency and sample rate are 10 dB/division, -20 dB, 100 kHz, 50 kHz and 200 kSa/s respectively.

and considering up to first 3000$^{th}$ harmonics.

The rectifier's input current and input voltage waveform obtained via PSIM 6.1 simulation program are shown in figure 7.29, and their values are 9.523 A rms and 219.2 V rms respectively. Its input power and output power are 2087.64 VA and 2023.6 W respectively. Hence, its efficiency is nearly 96.93 %. Also, its input power factor is 98.57 %.

Its average output voltage obtained by its output voltage waveform shown in figure 7.30 is 434.28 V. Maximum and minimum voltages in figure 7.30 are 439.74 V and 428.72 V respectively. Thus, its output voltage ripple is nearly 2.54 %.

FFT waveform of the proposed rectifier's input current is obtained by using the simulation program and it is given in figure 7.31. The harmonics that are up to 50$^{th}$ harmonic and have higher magnitudes near at the switching speed are obtained by using the figure 7.31, and given in the part corresponds to the simulation in table

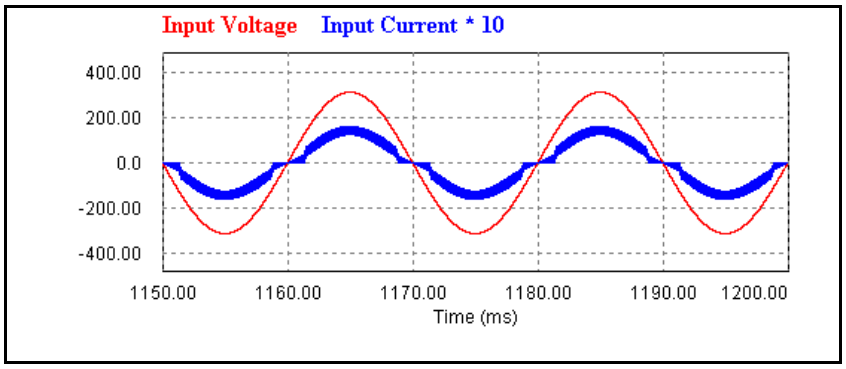



**Figure 7.29** Proposed rectifier's input current and input voltage waveform obtained using PSIM 6.1 simulation program at steady state when 2 kW purely resistive load is connected.

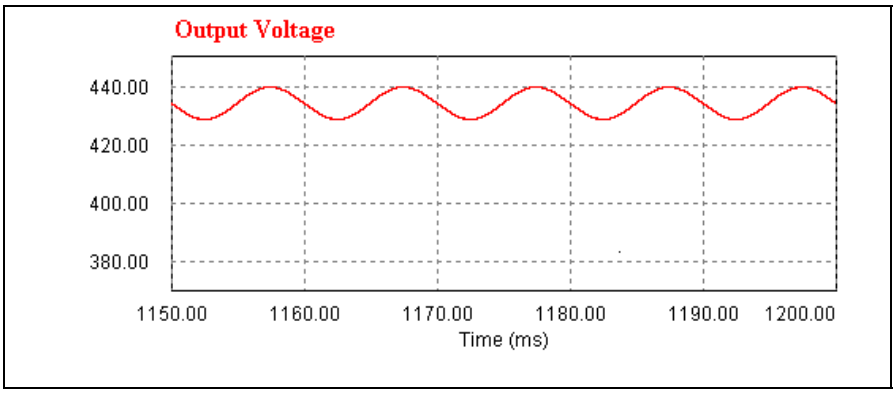
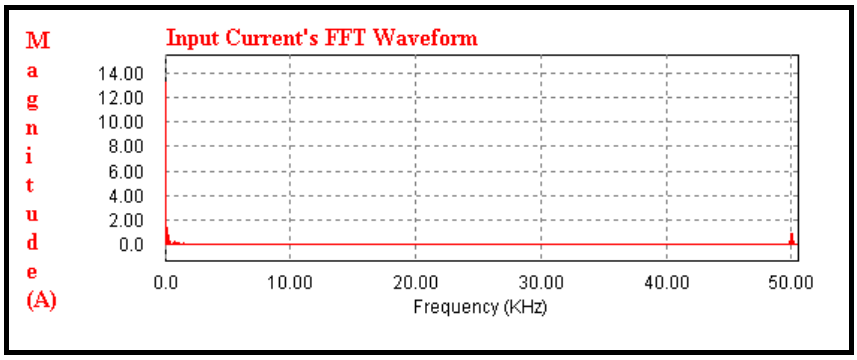
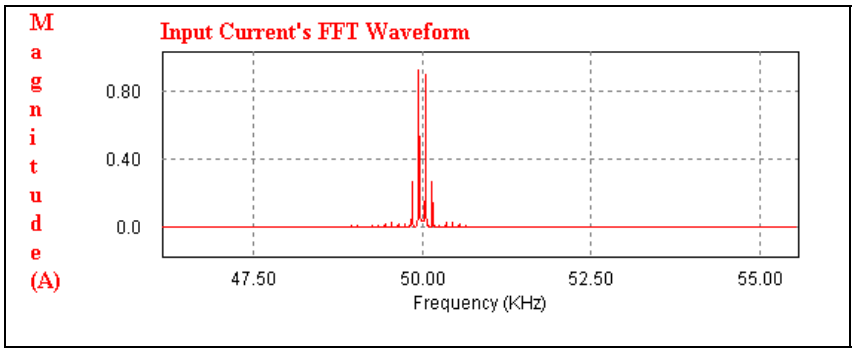



**Figure 7.30** Proposed rectifier's output voltage waveform obtained by using PSIM 6.1 simulation program at steady state when 2 kW purely resistive load is connected.

7.4. The rectifier's input current's THD is calculated as 16.79 % by using them. THD block in PSIM 6.1 measured its input current's THD as 17.0 % considering on the current's all harmonics. This value is more correct.




**(a)**




**(b)**

**Figure 7.31** (a) FFT waveform of proposed rectifier's input current obtained by using PSIM 6.1 simulation program between 0 and 50500 Hz at steady state when 2 kW purely resistive load is connected, (b) the FFT waveform between 47 and 55 kHz.

The harmonics between the 1st and 35th harmonic and the one near the 50 kHz switching frequency are important in measurement part in table 7.4. However, all even harmonics except the 2nd harmonic don't have important magnitudes in the part in table 7.4. On the other hand, the harmonics between 1st and 31st harmonic and near the switching frequency have important magnitudes except the even harmonics in simulation part in this table. There are some differences between the harmonic magnitudes in simulation part and measurement part in table 7.4. Cause of the differences is same with the differences between the harmonic magnitudes in the parts correspond to the simulation and measurement in table 7.3.

| | Measured | Simulation | | Measured | Simulation |
|---|---|---|---|---|---|
| **Harmonic #** | **Magnitude (A)** | **Magnitude (A)** | **Harmonic #** | **Magnitude (A)** | **Magnitude (A)** |
| 1 | 12.928 | 13.278 | 28 | 0.011 | 0.001 |
| 2 | 0.117 | 0.004 | 29 | 0.023 | 0.095 |
| 3 | 0.364 | 1.332 | 30 | 0.012 | 0.000 |
| 4 | 0.012 | 0.001 | 31 | 0.047 | 0.094 |
| 5 | 0.448 | 0.766 | 32 | 0.014 | 0.001 |
| 6 | 0.033 | 0.001 | 33 | 0.099 | 0.038 |
| 7 | 0.342 | 0.580 | 34 | 0.009 | 0.001 |
| 8 | 0.011 | 0.000 | 35 | 0.099 | 0.031 |
| 9 | 0.479 | 0.284 | 36 | 0.018 | 0.001 |
| 10 | 0.020 | 0.001 | 37 | 0.066 | 0.071 |
| 11 | 0.458 | 0.015 | 38 | 0.012 | 0.000 |
| 12 | 0.008 | 0.001 | 39 | 0.034 | 0.063 |
| 13 | 0.303 | 0.196 | 40 | 0.011 | 0.001 |
| 14 | 0.011 | 0.000 | 41 | 0.050 | 0.017 |
| 15 | 0.190 | 0.222 | 42 | 0.011 | 0.001 |
| 16 | 0.019 | 0.001 | 43 | 0.054 | 0.033 |
| 17 | 0.033 | 0.118 | 44 | 0.012 | 0.000 |
| 18 | 0.014 | 0.001 | 45 | 0.054 | 0.058 |
| 19 | 0.102 | 0.030 | 46 | 0.014 | 0.000 |
| 20 | 0.008 | 0.001 | 47 | 0.046 | 0.045 |
| 21 | 0.157 | 0.132 | 48 | 0.012 | 0.001 |
| 22 | 0.014 | 0.000 | 49 | 0.016 | 0.011 |
| 23 | 0.173 | 0.142 | 50 | 0.009 | 0.001 |
| 24 | 0.019 | 0.001 | 997 | | 0.279 |
| 25 | 0.137 | 0.070 | 999 | 0.328 | 0.980 |
| 26 | 0.008 | 0.001 | 1001 | | 0.945 |
| 27 | 0.071 | 0.030 | 1003 | | 0.282 |

**Table 7.4** Proposed rectifier's input current harmonics up to 50$^{th}$ harmonic measured by using HIOKI 3194 Motor/Harmonic Hi Tester, 999$^{th}$ harmonic obtained by DSO6014A scope and its harmonics up to 50$^{th}$ harmonic, harmonics that have higher magnitudes near at switching speed obtained by using PSIM 6.1 with 2 kW load at steady state.

## 7.5 Conclusion

The proposed rectifier's circuit block is given and it is explained block by block in this chapter. The rectifier's schematic and printed circuit board is shown. Experimental results and simulation results in same conditions are also given. They are listed in table 7.5.

| | Simulation Circuit (1 kW load) | Implemented Circuit (1 kW load) | Error Magnitude (%) | Simulation Circuit (2 kW load) | Implemented Circuit (2 kW load) | Error Magnitude (%) |
|---|---|---|---|---|---|---|
| **Efficiency (%)** | 95.24 | 96.2 | 0.96 | 96.93 | 95.63 | 1.3 |
| **Power Factor** | 0.973 | 0.987 | 1.4 | 0.9857 | 0.9913 | 0.56 |
| **Output Voltage Ripple (%)** | 1.25 | 0.99 | 0.26 | 2.54 | 2.19 | 0.35 |
| **THD (%)** | 23.9 | 15.37 | 8.53 | 17.0 | 11.95 | 5.05 |

**Table 7.5** Simulation and implemented rectifier circuit results with different loads.

The THD values in this table are the ones measured by the THD block in PSIM 6.1 for the simulation circuit with 1 kW and 2 kW purely resistive load while the THD values measured by the THD measurement menu in HIOKI 3194 Motor Harmonic/ Hi Tester for the implemented circuit with the two loads are entered in this table since their measurements are very accurate.

Implemented rectifier with 1 kW load has higher efficiency, power factor, lower output voltage ripple and THD than the simulated circuit. Simulated circuit contains same snubbers and power semiconductors parameters as the implemented circuit. However, fall time and rise time parameters can not be entered in power semiconductors parameter part in PSIM 6.1 simulation software. Also, the boost inductors, L1 and L2 in figure 6.8 are ideal inductors in simulation circuit while the inductor designed by using amorphous metal core in this chapter is used in implemented circuit. UC3854B IC drives the IGBT better in implemented circuit than the approximate model in figure 6.1 used in the simulations. Hence, actual circuit has better performance than the simulation circuit with 1 kW load. However, as the load is increased, $I^2R$ losses in the boost inductors and power carrying conductors in real circuit increase. Thus, the simulation circuit with 2 kW load has

higher efficiency than the real rectifier circuit with same load. On the other hand, the real rectifier circuit has better performance than the simulation circuit considering power factor, THD and output voltage ripple with 2 kW load.

However, the error magnitudes (%) between the simulation circuit's results and implemented circuit's ones given in table 7.5 are less than 1.5 % for the circuits with 1 kW and 2 kW purely resistive loads, but the THD errors between their results are less than 9 %. The causes of the errors are not only that UC3854B IC drives the IGBT better in the implemented circuit than the approximate model in figure 6.1 used in the simulations but the measurement equipments' measurements errors. On the other hand, the errors between the simulation and implemented circuit's results are very small. These results clearly indicate that performance of the proposed circuit can be investigated and its comparison with the conventional circuit can be reliably made in the simulation environment. In this way, considerable time saving can be achieved in improving the circuit.

# CHAPTER 8

# CONCLUSION

## 8.1 General

Electrical power consumers are generally a pollutant of AC electrical power distribution network. As number of electrical power consumer increases, the distortion over electrical power distribution network becomes very important. Total harmonic distortion of unity power factor rectifiers is very small, they are used for reducing overall distortion on the AC electrical power distribution network.

Unity power factor rectifiers use energy as efficient as possible since mains supply seems unity power factor rectifiers nearly a resistance whether their load is inductive, capacitive or purely resistive. This means that their reactive powers at the input sides of the rectifiers are nearly zero.

The unity power factor rectifiers' efficiency depends on their topologies. There are various unity power factor rectifier topologies. Research upon higher efficiency unity power factor rectifier topologies is very popular.

In this thesis, the main objective is to study unity power factor rectifiers and if possible develope a new single transistor unity power factor rectifier topology.

Fist of all, some unity power factor rectifier topologies are investigated. Then, one of them is selected for further study.

Afterwards, a new unity power factor topology is proposed and compared with the selected unity power factor rectifier topology.

Control techniques for power factor converters are investigated to find a

proper control technique. Average current control technique is selected to use in the selected unity power factor rectifier and proposed unity power factor rectifier's simulations and their implementations.

The two rectifier topologies are compared with each other on the basis of efficiency, output voltage ripple, total harmonic distortion, input curent ripple, etc. by simulating them.

Also, the two rectifiers are implemented on a same PCB (Printed Circuit Board). The implemented proposed rectifier is tested in a laboratory and it is simulated with 1 kW and 2 kW purely resistive load by using PSIM 6.1 simulation program. The implemented proposed rectifier's measured results and the simulation results are compared with each other in this thesis.

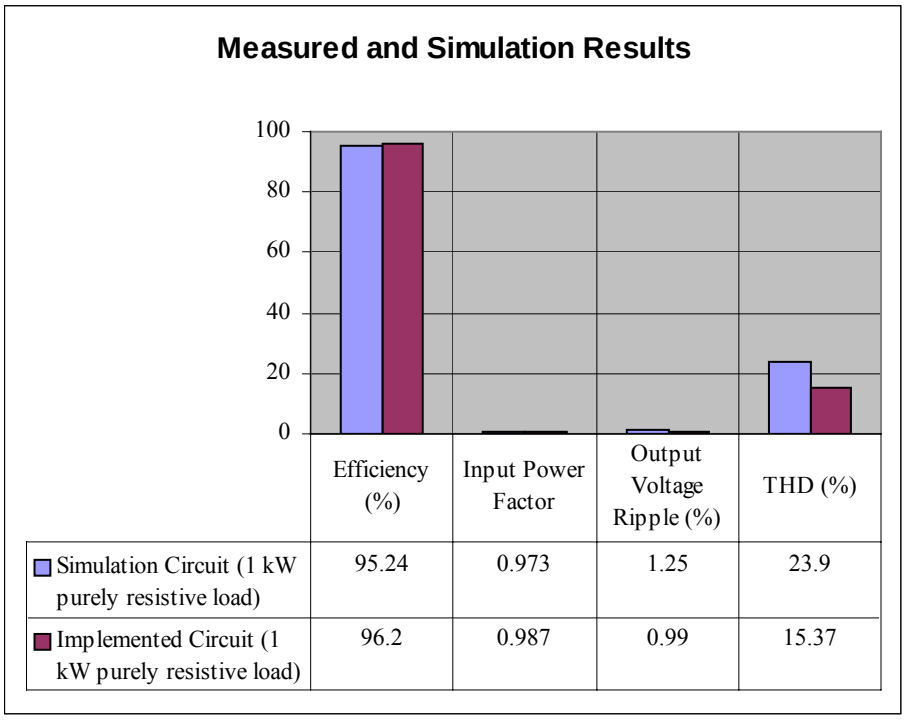
## 8.2 Experimental And Simulation Results

Simulation speed is very important, so first a good model is sought for the controller IC, namely UC3854B. PSIM 6.1 has already UC3854B IC model in its library. This model is simplified to increase the simulation speed, so two UC3854B IC models are developed. The IC model given in figure 6.1 is for PSIM 6.1 simulation program and the other one given in figure 6.2 is for MATLAB-Simulink R14 simulation program.

The classical unity power factor rectifier is simulated within 0.5 s with 3 kW purely resistive load by using PSIM 6.1 with the IC model in figure 6.1, PSIM 6.1 with the IC model in its library, PSIM MATLAB co-simulation with the IC model in figure 6.1, MATLAB-Simulink R14 with the IC model in figure 6.3. Their simulation speeds are 9.5 minutes, 19 minutes, 45 minutes and 2.5-3 hours respectively. PSIM 6.1 with the IC model in figure 6.1 is selected to use in all simulations made through this thesis work due to its higher speed.

Classical and proposed unity power factor rectifiers are designed according to the specifications given in section 6.1. Their output capacitance and boost inductance are calculated as 1.5 mF and 500 uH. The boost inductor is designed by using an amorphous metal core and its design is given in section 7.2.1 in detail.

The proposed rectifier is implemented and tested in a laboratory with 1 kW and 2 kW purely resistive loads and their results are measured. Also, the proposed rectifier are simulated in nearly same conditions with the tested circuit in a laboratory. The proposed rectifier's simulation circuit has same snubbers and power semiconductors parameters as the implemented circuit. However, only conduction voltage drop parameter can be entered in power semiconductors parameter part in PSIM 6.1 simulation software and this is made in the simulation circuit. Also, UC3854B IC model in figure 6.1 is used in the simulation circuit, and ideal boost inductors are used in this circuit while the inductor designed by using amorphous metal core in section 7.2.1 is used in implemented circuit.




| | Efficiency (%) | Input Power Factor | Output Voltage Ripple (%) | THD (%) |
|---|---|---|---|---|
| Simulation Circuit (1 kW purely resistive load) | 95.24 | 0.973 | 1.25 | 23.9 |
| Implemented Circuit (1 kW purely resistive load) | 96.2 | 0.987 | 0.99 | 15.37 |

**Figure 8.1** Proposed UPF rectifier's implemented and simulation circuits' performance diagrams with 1 kW purely resistive load at steady state.

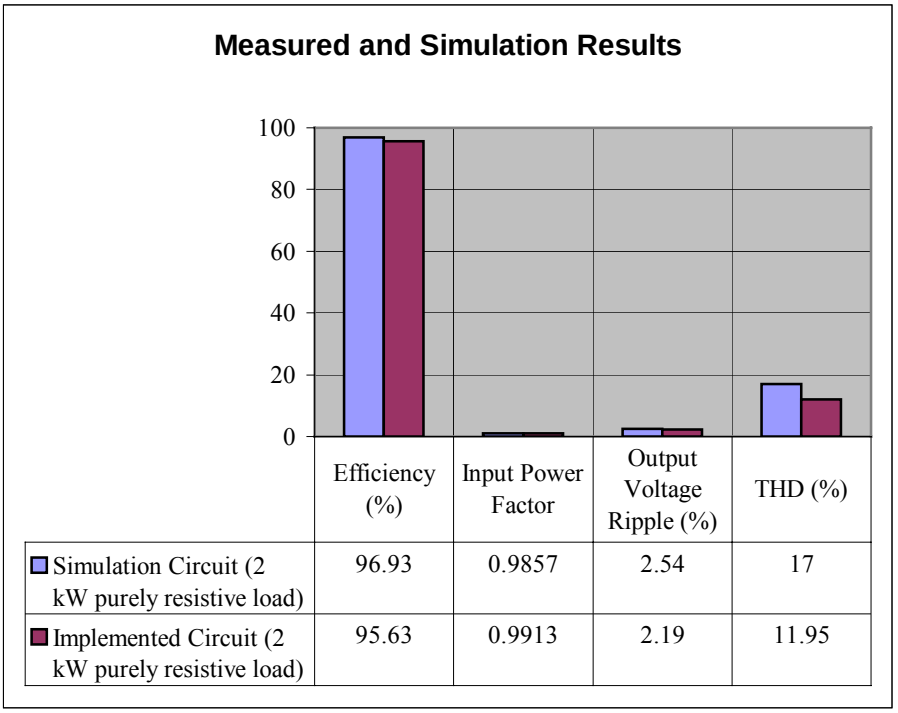



**Figure 8.2** Proposed UPF rectifier's implemented and simulation circuits' performance diagrams with 2 kW purely resistive load at steady state.

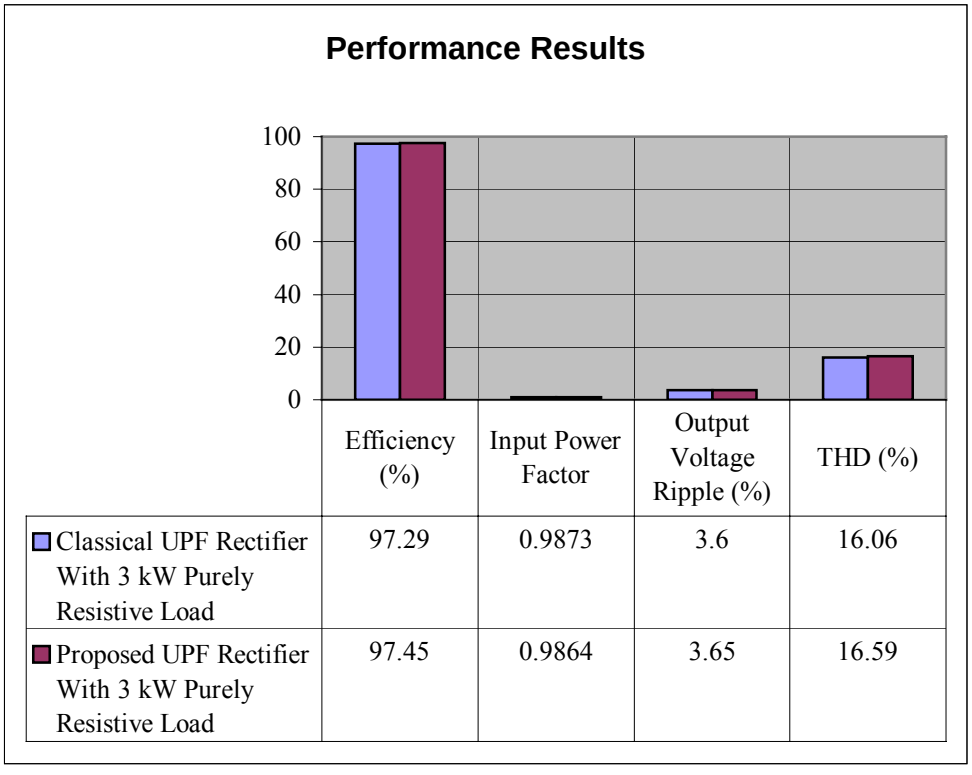
The proposed rectifier's implemented circuit and simulation circuit's results with 1 kW and 2 kW purely resistive loads at steady state are given in figure 8.1 and figure 8.2 respectively. The implemented circuit has better input power factor, input current's THD and output voltage ripple with 1 kW and 2 kW purely resistive loads than the simulation circuit. This shows that UC3854B IC drives the IGBT better in implemented circuit than the approximate model in figure 6.1 used in the simulations. On the other hand, implemented circuit has higher efficiency than the simulation circuit with 1 kW purely resistive load while simulation circuit has higher efficiency than the implemented circuit with 2 kW purely resistive load because $I^2R$ losses in the boost inductors and power carrying conductors in real circuit increase as the load is increased.

However, the errors between the simulation and implemented circuit's results are less than 1.5 %, but the THD errors between their results are less than 9 %. This shows that the simulations are found to be in an agreement with measurements and

the approximate UC3854B IC model in figure 6.1 is correct. Therefore, the rest of the study is done via simulations.

The implemented circuit's measured performance results are within the design specifications given in section 6.1. This indicates that proposed rectifier design is correctly made.

The performances of the two topologies are studied with 3 kW purely resistive load and inductive-resistive loads in the simulation environment. Classical and proposed unity power factor rectifier are compared with each other on the basis of their efficiency, input power factor, output voltage ripple and input current's THD (Total Harmonic Distortion) by simulating them using PSIM 6.1 simulation software with the UC3854B IC model in figure 6.1.




| | Efficiency (%) | Input Power Factor | Output Voltage Ripple (%) | THD (%) |
|---|---|---|---|---|
| Classical UPF Rectifier With 3 kW Purely Resistive Load | 97.29 | 0.9873 | 3.6 | 16.06 |
| Proposed UPF Rectifier With 3 kW Purely Resistive Load | 97.45 | 0.9864 | 3.65 | 16.59 |

**Figure 8.3** Classical and proposed UPF rectifier's performance diagrams obtained via simulation with 3 kW purely resistive load at steady state.

In these simulations, the rectifiers' output power, output voltage, mains supply's voltage, mains supply's frequency, and switching frequency are taken as 3 kW, 440 V, 220 V rms, 50 Hz, 50 kHz respectively. The simulation circuit used in these simulations doesn't contain any snubber. Ideal boost inductors are used in these simulations.

The classical UPF rectifier and proposed converter's performances are summarized in figure 8.3 for a 3 kW resistive load. It can be observed that the proposed unity power factor rectifier efficiency is higher than the classical UPF rectifier but not significiantly. However, the classical UPF rectifier's input power factor, input current's THD and output voltage ripple are better than the proposed rectifier.

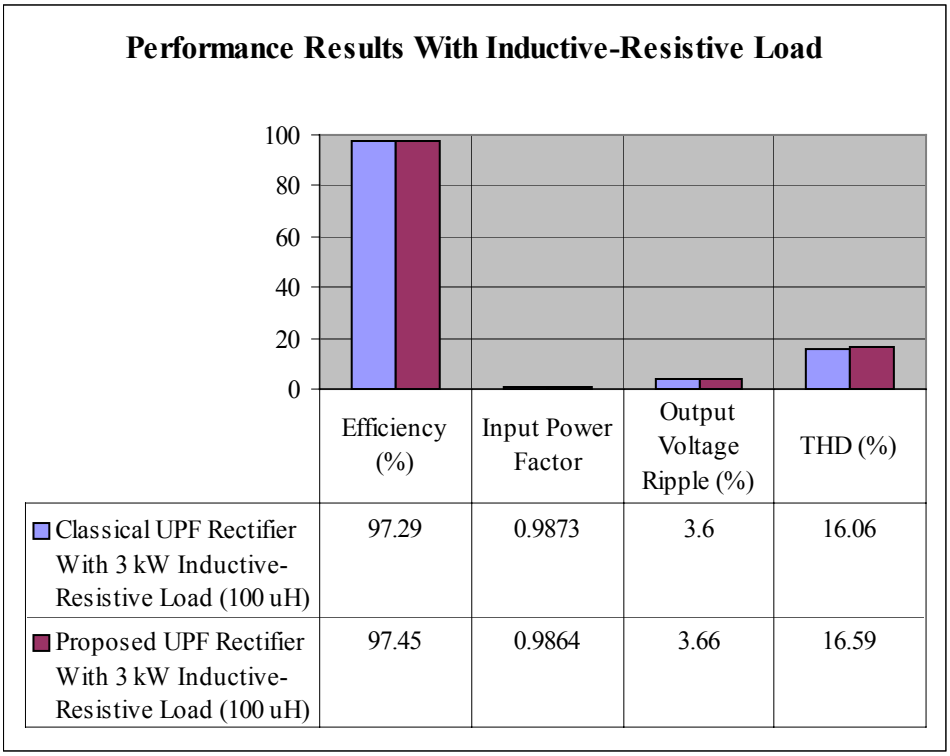



**Figure 8.4** Classical and proposed UPF rectifier's performance diagram with 3 kW inductive-resistive load (100 uH).

The two rectifiers give similar results in simulations made in this thesis work with 3 kW purely resistive load and inductive-resistive loads. The rectifiers' simulation results with 3 kW purely resistive load (100 uH) are given in figure 8.4 and the figure proves this. Hence, the study is pursued with resistive load alone.

The results given in figure 8.3 and figure 8.4 also show that the classical and proposed unity power factor rectifiers' design methodology and their design are correct since their simulation results are within their design specifications given in section 6.1.

The proposed rectifier's experimental and simulation results with purely resistive loads are combined and its efficiency, input power factor, input current's THD variations with different resistive loads are obtained. They are given before in figure 6.13, figure 6.14 and figure 6.15 respectively. According to these figures, these performances of the proposed rectifier's implemented circuit and simulation circuit become better as the load is increased to its 3 kW nominal value, but the implemented rectifier's efficiency with 2 kW purely resistive load is 0.57 % less than the one with 1 kW purely resistive load since $I^2R$ losses in the implemented circuit increase as the load increases.

The two rectifiers are simulated in dynamic conditions. The proposed and classical unity power factor rectifier's settling times with respect to their output voltages are 47.61 ms and 47.65 ms respectively according to the simulations. Their settling times are nearly same.

## 8.3 Conclusion And Future Work

A new single switching transistor unity power factor rectifier topology is developed in this thesis. The classical UPF rectifier needs one free-wheeling diode parallely connected to its boost inductor and boost diode to reset the boost inductor's core while the proposed rectifier doesn't need this free-wheeling diode since the proposed rectifier's boost inductors are placed at its AC side. However, the proposed rectifier uses one extra boost diode. Thus, these two rectifier topologies have the same number of power diodes and switching power transistor.

On the other hand, this proposed rectifier and the classical unity power factor rectifier give similar performance results, so more investigation up on this proposed rectifier topology is not necessary.

In this thesis work, modeling of a power factor corrector IC, namely UC3854B IC and implementation of the unity power factor rectifier are learned. These experiences will be used for development of a SEPIC converter in TUBITAK-BAP project whose project number is 105E053.

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# APPENDIX A: UC3854 Controlled Power Factor Correction Circuit Design

UNITRODE

U-134

APPLICATION NOTE

## UC3854 Controlled Power Factor Correction Circuit Design

PHILIP C. TODD

ABSTRACT

This Application Note describes the concepts and design of a boost preregulator for power factor correction. This note covers the important specifications for power factor correction, the boost power circuit design and the UC3854 integrated circuit which controls the converter. A complete design procedure is given which includes the tradeoffs necessary in the process. This design procedure is directly applicable to the UC3854A/B as well as the UC3854. The recommendations in Unitrode Design Note DN-39 cover other areas of the circuit and, while not discussed here, must be considered in any design. This application note supersedes Application Note U- 125 "Power Factor Correction With the UC3854. "

### INTRODUCTION

The objective of active power factor correction is to make the input to a power supply look like a simple resistor. An active power factor corrector does this by programming the input current in response to the input voltage. As long as the ratio between the voltage and current is a constant the input will be resistive and the power factor will be 1.0. When the ratio deviates from a constant the input will contain phase displacement, harmonic distortion or both and either one will degrade the power factor.

The most general definition of power factor is the ratio of real power to apparent power.

$$PF = \frac{P}{(Vrms \times Irms)} \text{ or } PF = \frac{Watts}{V.A.}$$

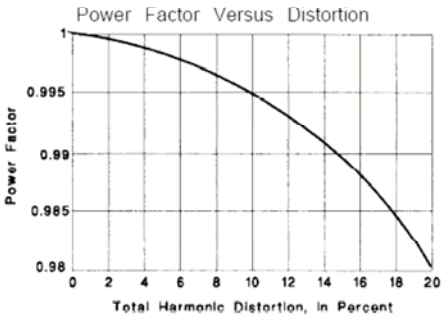
Where P is the real input power and Vrms and Irms are the root mean square (RMS) voltage and current of the load, or power factor corrector input in this case. If the load is a pure resistance the real power and the product of the RMS voltage and current will be the same and the power factor will be 1.0. If the load is not a pure resistance the power factor will be below 1.0.

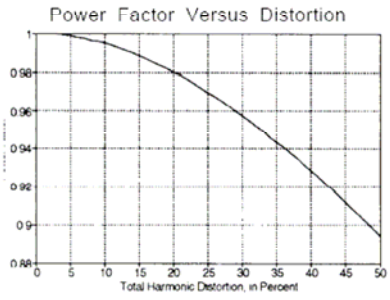
Phase displacement is a measure of the reactance of the input impedance of the active power factor corrector. Any amount of reactance, either inductive or capacitive will cause phase displacement of the input current waveform with respect to the input voltage waveform. The phase displacement of the voltage and current is the classic definition of power factor which is the cosine of the phase angle between the voltage and current sinusoids.

$$PF = \cos\theta$$

The amount of displacement between the voltage and current indicates the degree to which the load is reactive. If the reactance is a small part of the impedance the phase displacement will be small. An active power factor corrector will generate phase displacement of the input current if there is phase shift in the feedforward signals or in the control loops. Any filtering of the AC line current will also produce phase displacement.

Harmonic distortion is a measure of the non-linearity of the input impedance of the active power factor corrector. Any variation of the input impedance as a function of the input voltage will cause distortion of the input current and this distortion is the other contributor to poor power factor. Distortion increases the RMS value of the current without increasing the total power being drawn. A non-linear load will therefore have a poor power factor because the RMS value of the current is high but the total power delivered is small. If the non-linearity is small the harmonic distortion will be low. Distortion in an active power factor corrector comes from




| Harmonic Order | Permissible current | Maximum permissible current |
|---|---|---|
| n | mA/W | A |
| Odd harmonics | | |
| 3 | 3.4 | 2.30 |
| 5 | 1.9 | 1.14 |
| 7 | 1.0 | 0.78 |
| 9 | 0.5 | 0.40 |
| 11 | 0.35 | 0.33 |
| 13 | 0.3 | 0.21 |
| 15 up | 3.85/n | $0.15 \times \frac{15}{n}$ |
| Even harmonics | | |
| 2 | 1.8 | 1.08 |
| 4 | 0.7 | 0.42 |
| 6 | 0.5 | 0.30 |
| >8 | $\frac{3}{n}$ | $\frac{1.80}{n}$ |

Table 1

several sources: the feedforward signals, the feedback loops, the output capacitor, the inductor and the input rectifiers.

An active power factor corrector can easily achieve a high input power factor, usually much greater than 0.9. But power factor is not a sensitive measure of the distortion or the displacement of the current waveform. It is often more convenient to deal with these quantities directly rather than with the power factor. For example, 3% harmonic distortion alone has a power factor of 0.999. A current with 30% total harmonic distortion still has a power factor of 0.95. A current with a phase displacement of 25 degrees from the voltage has a power factor of 0.90.

The trend among the world standards organizations responsible for power quality is to specify maximum limits for the amount of current allowed at each of the harmonics of the line frequency. IEC 555-2 specifies each harmonic up through and beyond the 15th and the amount of current permissible at each. Table 1 lists the requirements for IEC 555-2 as of the time of this writing. There are two parts to the specification, a relative distortion and an absolute distortion maximum. Both limits apply to all equipment. This table is included here as an example of a line distortion specification. It is not intended to be used for design purposes. The IEC has not finalized the requirements of IEC 555 at this time and major changes are possible.

Active Power Factor Correction

A boost regulator is an excellent choice for the power stage of an active power factor corrector because the input current is continuous and this produces the lowest level of conducted noise and the best input current waveform. The disadvantage of the boost regulator is the high output voltage required. The output voltage must be greater than the highest expected peak input voltage.

The boost regulator input current must be forced or programmed to be proportional to the input voltage waveform for power factor correction. Feedback is necessary to control the input current and either

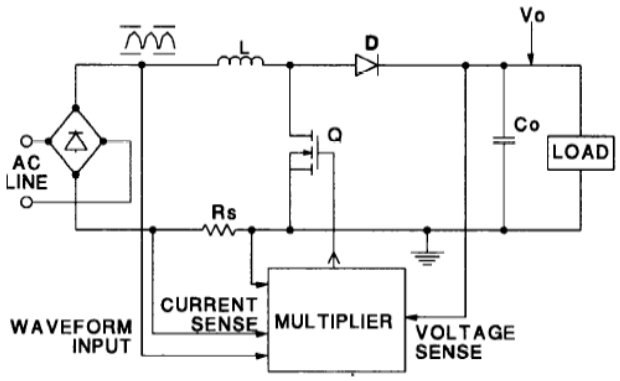



Figure 1

Basic Configuration of High Power Factor Control Circuit

peak current mode control or average current mode control may be used. Both techniques may be implemented with the UC3854. Peak current mode control has a low gain, wide bandwidth current loop which generally makes it unsuitable for a high performance power factor corrector since there is a significant error between the programming signal and the current. This will produce distortion and a poor power factor.

Average current mode control is based on a simple concept. An amplifier is used in the feedback loop around the boost power stage so that input current tracks the programming signal with very little error. This is the advantage of average current mode control and it is what makes active power factor correction possible. Average current mode control is relatively easy to implement and is the method described here.

A block diagram of a boost power factor corrector circuit is shown in Figure 1. The power circuit of a

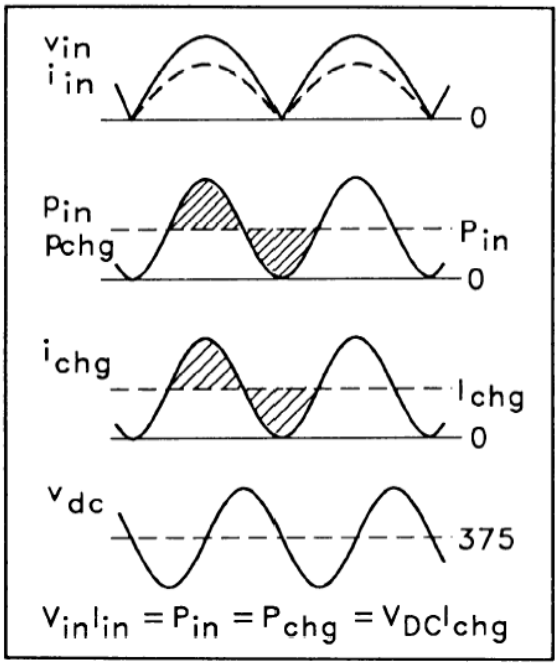



Figure 2. Preregulator Waveforms

boost power factor corrector is the same as that of a dc to dc boost converter. There is a diode bridge ahead of the inductor to rectify the AC input voltage but the large input capacitor which would normally be associated with the AC to DC conversion function has been moved to the output of the boost converter. If a capacitor follows the input diode bridge it is a small one used only for noise control.

The output of the boost regulator is a constant voltage but the input current is programmed by the input voltage to be a half sine wave. The power flow into the output capacitor is not constant but is a sine wave at twice the line frequency since power is the instantaneous product of voltage an current. This is shown in Figure 2. The top waveform shows the voltage and the current into the power factor corrector and the second waveform shows the flow of energy into and out of the output capacitor. The output capacitor stores energy when the input voltage is high and releases the energy when the input voltage is low to maintain the output power flow. The third waveform in Figure 2 shows the charging and discharging current. This current has a different shape from the input current and is almost entirely at the second harmonic of the AC line voltage. This flow of energy into and out of the capacitor results in ripple voltage at the second harmonic also and this is shown in the fourth waveform in Figure 2. Note that the voltage ripple is displaced by 90 degrees relative to the current since this is reactive energy storage. The output capacitor must be rated to handle the second harmonic ripple current as well as the high frequency ripple current from the boost converter switch which modulates it.

Control Circuits

An active power factor corrector must control both the input current and the output voltage. The current loop is programmed by the rectified line voltage so that the input to the converter will appear to be resistive. The output voltage is controlled by changing the average amplitude of the current programming signal. An analog multiplier creates the current programming signal by multiplying the rectified line voltage with the output of the voltage error amplifier so that the current programming signal has the shape of the input voltage and an average amplitude which controls the output voltage. Figure 3 is a block diagram which shows the basic control circuit arrangement necessary for an active power factor corrector. The output of the multiplier is the current programming signal and is called Imo for multiplier output current. The multiplier input from the rectified line voltage is shown as a current in Figure 3 rather than as a voltage signal because this is the way it is done in the UC3854.

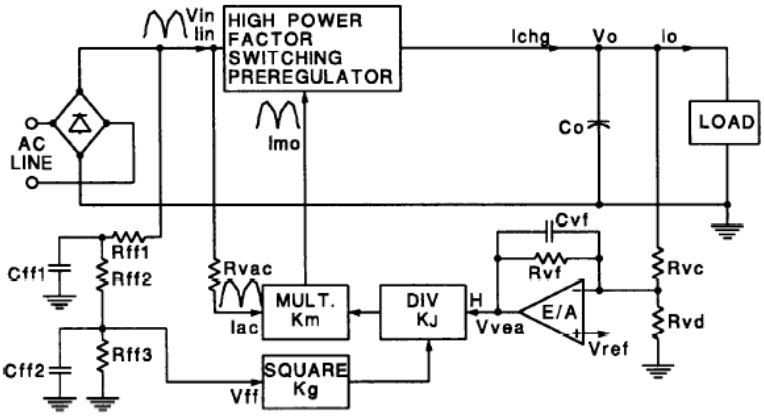



Figure 3. High Power Factor

Figure 3 shows a squarer and a divider as well as a multiplier in the voltage loop. The output of the voltage error amplifier is divided by the square of the average input voltage before it is multiplied by the rectified input voltage signal. This extra circuitry keeps the gain of the voltage loop constant, without it the gain of the voltage loop would change as the square of the average input voltage. The average value of the input voltage is called the feedforward voltage or Vff since it provides an open loop correction which is fed forward into the voltage loop. It is squared and then divided into the voltage error amplifier output voltage (Vvea).

The current programming signal must match the rectified line voltage as closely as possible to maximize the power factor. If the voltage loop bandwidth were large it would modulate the input current to keep the output voltage constant and this would distort the input current horribly. Therefore the voltage loop bandwidth must be less than the input line frequency. But the output voltage transient response must be fast so the voltage loop bandwidth must be made as large as possible. The squarer and divider circuits keep the loop gain constant so the bandwidth can be as close as possible to the line frequency to minimize the transient response of the output voltage. This is especially important for wide input voltage ranges.

The circuits which keep the loop gain constant make the output of the voltage error amplifier a power control. The output of the voltage error amplifier actually controls the power delivered to the load. This can be seen easily from an example. If the output of the voltage error amplifier is constant and the input voltage is doubled the programming signal will double but it will be divided by the square of the feedforward voltage, or four times the input, which will result in the input current being reduced to half its original value. Twice the input voltage times half the input current results in the same input power as before. The output of the voltage error amplifier, then, controls the input power level of the power factor corrector. This can be used to limit the maximum power which the circuit can draw from the power line. If the output of the voltage error amplifier is clamped at some value that corresponds to some maximum power level, then the active power factor corrector will not draw more than that amount of power from the line as long as the input voltage is within its range.

Input Distortion Sources

The control circuits introduce both distortion and displacement into the input current waveform. These errors come from the input diode bridge, the multiplier circuits and ripple voltage, both on the output and on the feedforward voltage.

There are two modulation processes in an active power factor corrector. The first is the input diode bridge and the second is the multiplier, divider, squarer circuit. Each modulation process generates cross products, harmonics or sidebands between the two inputs. The description of these mathematically can be quite complex. Interestingly enough, however, the two modulators interact and one becomes a demodulator for the other so that the result is quite simple. As shown later, virtually all of the ripple voltages in an active power factor corrector are at the second harmonic of the line frequency. When these voltages go through the multiplier and get programmed into the input current and then go through the input diode bridge the second harmonic voltage amplitude results in two frequency components. One is at the third harmonic of the line frequency and the other is at the fundamental. Both of these components have an amplitude which is half of the amplitude of the original second harmonic voltage. They also have the same phase as the original second harmonic. If the ripple voltage is 10% of the line voltage amplitude and is phase shifted 90 degrees the input current will have a third harmonic which is 5% of the fundamental and is shifted 90 degrees and a fundamental component which is 5% of the line current and is displaced by 90 degrees.

The feedforward voltage comes from the rectified AC line which has a second harmonic component that is 66% of the amplitude of the average value. The filter capacitors of the feedforward voltage divider greatly attenuate the second harmonic and effectively remove all of the higher harmonics but some of the second harmonic is still present at the feedforward input. This ripple voltage is squared by the control circuits as shown in Figure 3. This doubles the amplitude of the ripple since it is riding on top of a large DC value. The divider process is transparent to the ripple voltage so it passes on to the multiplier and eventually becomes third harmonic distortion of the input current and a phase displacement. The doubling action of the squarer means that the amplitude of the input current distortion in percent is the same as the amplitude of the ripple voltage, in percent, at the feedforward input.

Needless to say, the feedforward ripple voltage must be kept small to achieve a low distortion input current. The ripple voltage could be made small with a single pole filter with a very low cutoff frequency. However, fast response to changes of the input voltage is also desirable so the response time of the filter must be fast. These two requirements are, of course, in conflict and a compromise must be found. A two pole filter on the feedforward input has a faster transient response than a single pole filter for the same amount of ripple attenuation. Another advantage of the two pole filter has is that the phase shift is twice that of the single pole filter. This results in 180 degrees of phase shift of the second harmonic and brings both the resulting third harmonic and the displacement component of the input current back in phase with the voltage. A second harmonic ripple voltage of 3% at the feedforward input results in a 0.97 power factor just from the displacement component if a single pole filter is used for the feedforward voltage. With a two pole filter there is no displacement component to the power factor because it is in

phase with the input current. The third harmonic component of the input current resulting from the second harmonic at the feedforward input will have the same amplitude as the second harmonic ripple voltage. If 3% second harmonic is present on the feedforward voltage the line current waveform will contain 3% third harmonic distortion.

The output voltage has ripple at the second harmonic due to the ripple current flowing through the output capacitor. This ripple voltage is fed back through the voltage error amplifier to the multiplier and, like the feedforward voltage, programs the input current and results in second harmonic distortion of the input current. Since this ripple voltage does not go through the squarer the amplitude of the distortion and displacement are each half of the amplitude of the ripple voltage. The ripple voltage at the output of the voltage error amplifier must be in phase with the line voltage for the displacement component to be in phase. The voltage error amplifier must shift the second harmonic by 90 degrees so that it will be in phase with the line voltage.

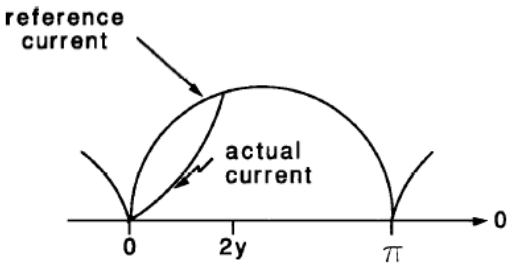



Figure 4. Cusp Distortion

The voltage loop of a boost converter with average current mode control has a control to output transfer function which has a single pole roll off characteristic so it could be compensated with a flat gain error amplifier. This produces a very stable loop with 90 degrees of phase margin. However, it provides less than optimum performance. The ripple voltage on the output capacitor is out of phase with the input current by 90 degrees. If the error amplifier has flat gain at the second harmonic frequency the distortion and displacement generated in the input current will be 90 degrees out of phase with the rectified AC line. The power factor can be improved by introducing phase shift into the voltage error amplifier response. This shifts the displacement component of the power factor back into alignment with the input voltage and increases the power factor. The amount of phase shift which can be added is determined by the need to keep the voltage loop stable. If the phase margin is reduced to 45 degrees the phase at the second harmonic will be very close to 90 degrees and this brings the displacement component back in phase with the input voltage.

The bandwidth of the voltage control loop is determined by the amount of input distortion to be contributed by the output ripple voltage. If the output capacitor is small and the distortion must be low then the bandwidth of the loop will be low so that the ripple voltage will be sufficiently attenuated by the error amplifier. Transient response is a function of the loop bandwidth and the lower the bandwidth the slower the transient response and the greater the overshoot. The output capacitor may need to be large to have both fast output transient response and low input current distortion.

The technique used to design the loop compensation is to find the amount of attenuation of the output ripple voltage required in the error amplifier and then work back into the unity gain frequency. The loop will have the maximum bandwidth when the phase margin is the smallest. A 45 degree phase margin is a good compromise which will give good loop stability and fast transient response and which is easy to design. The voltage error amplifier response which results will have flat gain up to the loop unity gain frequency and will have a single pole roll off above that frequency. This gives the maximum amount of attenuation at the second harmonic of the line frequency from a simple circuit, gives the greatest bandwidth and provides a 45 degree phase margin.

Cusp Distortion

Cusp distortion occurs just after the AC line input has crossed zero volts. At this point the amount of current which is required by the programming signal exceeds the available current slew rate. When the input voltage is near zero there is very little voltage across the inductor when the switch is closed so the current cannot ramp up very quickly so the available slew rate is too low and the input current will lag behind the desired value for a short period of time. Once the input current matches the programmed value the control loop is back in operation and the input current will follow the programming signal. The length of time that the current does not track the programmed value is a function of the inductor value. The smaller the inductor value the better the tracking and the lower the distortion but the smaller inductor value will have higher ripple current. The amount of distortion generated by this condition is generally small and is mostly higher order harmonics. This problem is minimized by a sufficiently high switching frequency.

UC3854 Block Diagram

A block diagram of the UC3854 is shown in Figure 5 and is the same as the one in the device data sheet. This integrated circuit contains the circuits necessary to control a power factor corrector. The UC3854 is designed to implement average current mode control but is flexible enough to be used for a wide variety of power topologies and control methods.

The top left corner of Figure 5 contains the under voltage lock out comparator and the enable comparator. The output of both of these comparators must be true to allow the device to operate. The inverting input to the voltage error amplifier is connected to pin 11 and is called Vsens. The diodes shown around the voltage error amplifier are intended to represent the functioning of the internal circuits rather than to show the actual devices. The diodes shown in the block diagram are ideal diodes and indicate that the non-inverting input to the error amplifier is connected to the 7.5Vdc reference voltage under normal operation but is also used for the slow start function. This configuration lets the voltage control loop begin operation before the output voltage has reached its operating point and eliminates the turn-on overshoot which plagues many power supplies. The diode shown between pin 11 and the inverting input of the error amplifier is also an ideal diode and is shown to eliminate confusion about whether there might be an extra diode drop added to the reference or not. In the actual device we do it with differential amplifiers. An internal current source is also provided for charging the slow start timing capacitor.

The output of the voltage error amplifier, Vvea, is available on pin 7 of the UC3854 and it is also an input to the multiplier. The other input to the multiplier is pin 6, Iac, and this is the input for the programming wave shape from the input rectifiers. This pin is held at 6.0 volts and is a current input. The feedforward input, Vff, is pin 8 and its value is squared before being fed into the divider input of the multiplier. The Iset current from pin 12 is also used in the multiplier to limit the maximum output current. The output current of the multiplier is Imo and it flows out of pin 5 which is also connected to the non-inverting input of the current error amplifier.

The inverting input of the current amplifier is connected to pin 4, the Isens pin. The output of the current error amplifier connects to the pulse width modulation (PWM) comparator where it is compared to the oscillator ramp on pin 14. The oscillator and the comparator drive the set-reset flip-flop which, in turn, drives the high current output on pin 16. The output voltage is clamped internally to the UC3854 at 15 volts so that power MOSFETs will not have their gates over driven. An emergency peak current limit is provided on pin 2 and it will shut the output pulse off when it is pulled slightly below ground. The reference voltage output is connected to pin 9 and the input voltage is connected to pin 15.

DESIGN PROCESS

Power Stage Design

This analysis of the power stage design makes use of a 250W boost converter as an example. The control circuit for a boost power factor corrector does not change much with the power level of the converter. A 5000 watt power factor corrector will have almost the same control circuits as a 50 watt

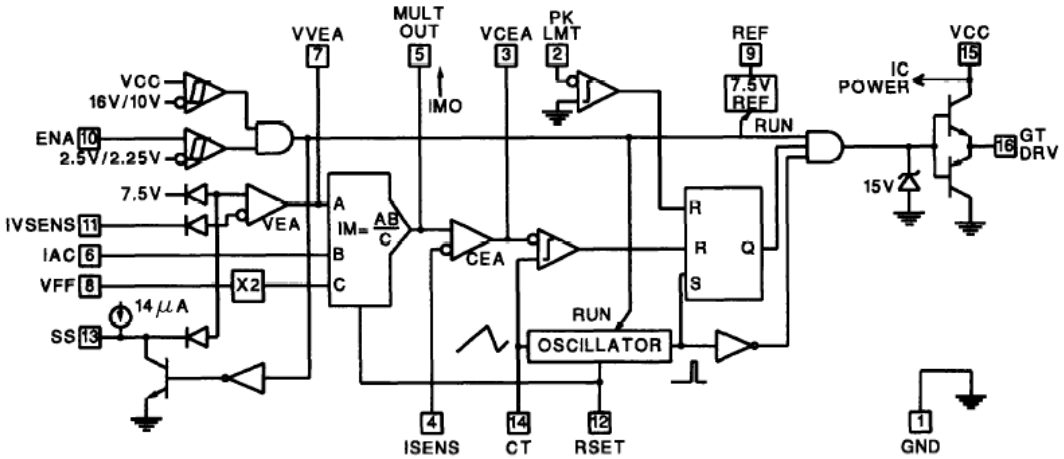



Figure 5. UC3854 Block Diagram

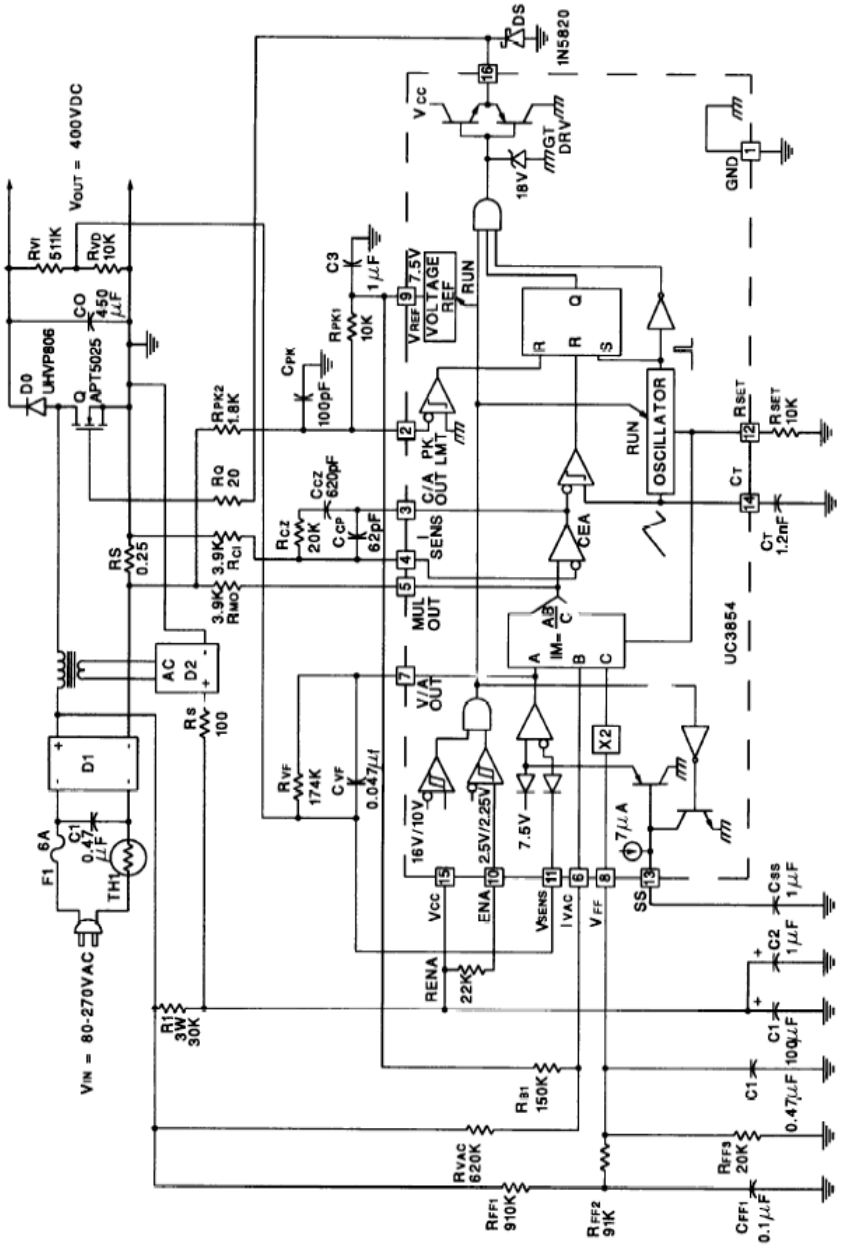



Figure 6.
Complete Schematic of 250W Power Factor Preregulator

corrector. The power stage will be different but the design process will remain the same for all power factor corrector circuits. Since the design process is the same and the power stage is scalable a 250 watt corrector serves well as an example and it can be readily scaled to higher or lower output levels. Figure 6 is the schematic diagram of the circuit. Please refer to this schematic in the discussion of the design process which follows.

Specifications

The design process starts with the specifications for the converter performance. The minimum and maximum line voltage, the maximum output power, and the input line frequency range must be specified. For the example circuit the specifications are:

Maximum power output: 250W

Input voltage range: 80-27OVac

Line frequency range: 47-65Hz

This defines a power supply which will operate almost anywhere in the world. The output voltage of a boost regulator must be greater than the peak of the maximum input voltage and a value 5% to 10% higher than the maximum input voltage is recommended so the output voltage is chosen to be 400Vdc.

Switching Frequency

The choice of switching frequency is generally somewhat arbitrary. The switching frequency must be high enough to make the power circuits small and minimize the distortion and must be low enough to keep the efficiency high. In most applications a switching frequency in the range of 20KHz to 300KHz proves to be an acceptable compromise. The example converter uses a switching frequency of I00KHz as a compromise between size and efficiency. The value of the inductor will be reasonably small and cusp distortion will be minimized, the inductor will be physically small and the loss due to the output diode will not be excessive. Converters operating at higher power levels may find that a lower switching frequency is desirable to minimize the power losses. Turn-on snubbers for the switch will reduce the switching losses and can be very effective in allowing a converter to operate at high switching frequency with very high efficiency.

Inductor Selection

The inductor determines the amount of high frequency ripple current in the input and its value is chosen to give some specific value of ripple current. Inductor value selection begins with the peak

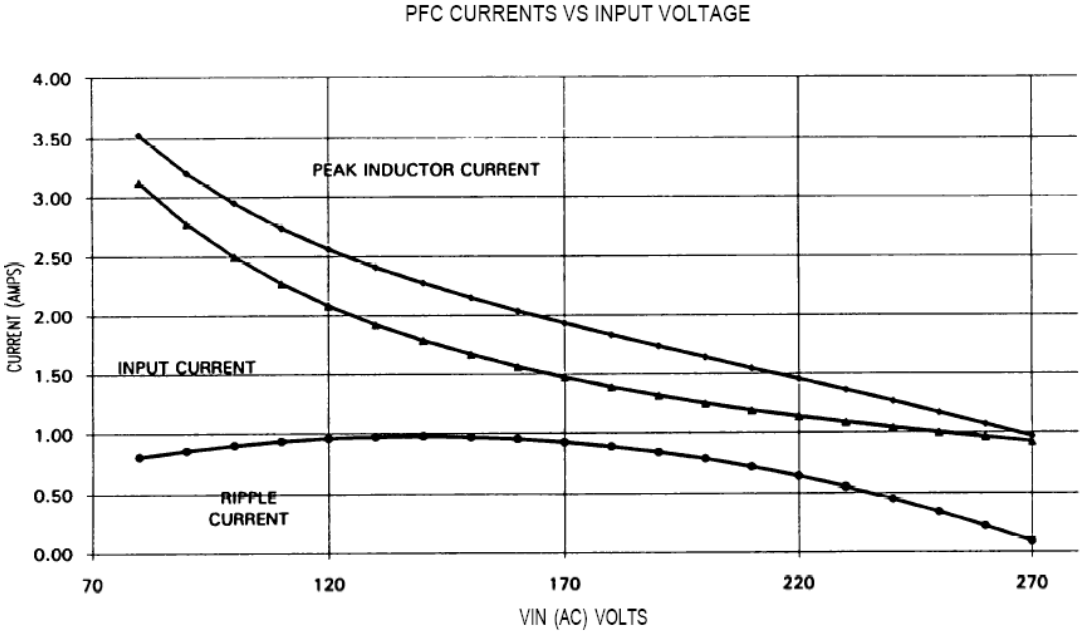



Figure 7

current of the input sinusoid. The maximum peak current occurs at the peak of the minimum line voltage and is given by:

$$I_{line(pk)} = \frac{\sqrt{2} \times P}{Vin(min)}$$

For the example converter the maximum peak line current is 4.42 amps at a Vin of 80Vac.

The maximum ripple current in a boost converter occurs when the duty factor is 50% which is also when the boost ratio M=Vo/Vin=2. The peak value of inductor current generally does not occur at this point since the peak value is determined by the peak value of the programmed sinusoid. The peak value of inductor ripple current is important for calculating the required attenuation of the input filter. Figure 7 is a graph of the peak to peak ripple current in the inductor versus input voltage for the example converter.

The peak-to-peak ripple current in the inductor is normally chosen to be about 20% of the maximum peak line current. This is a somewhat arbitrary decision since this is usually not the maximum value of the high frequency ripple current. A larger value of ripple current will put the converter into the discontinuous conduction mode for a larger portion of the rectified line current cycle and means that the input filter must be larger to attenuate more high frequency ripple current. The UC3854, with average current mode control, allows the boost stage to move between continuous and discontinuous modes of operation without a performance change.

The value of the inductor is selected from the peak current at the top of the half sine wave at low input voltage, the duty factor D at that input voltage and the switching frequency. The two equations necessary are given below:

$$D = \frac{Vo - Vin}{Vo}$$

$$L = \frac{Vin \times D}{fs \times \Delta I}$$

Where $\Delta I$ is the peak-to-peak ripple current. In the example 250W converter D=0.71, $\Delta I$=900ma, and L=0.89mH. For convenience the value of L is rounded up to 1.0mH.

The high frequency ripple current is added to the line current peak so the peak inductor current is the sum of peak line current and half of the peak-to-peak high frequency ripple current. The inductor must be designed to handle this current level. For our example the peak inductor current is 5.0 amps. The peak current limit will be set about 10% higher at 5.5 amps.

Output Capacitor

The factors involved in the selection of the output capacitor are the switching frequency ripple current, the second harmonic ripple current, the DC output voltage, the output ripple voltage and the hold-up time. The total current through the output capacitor is the RMS value of the switching frequency ripple current and the second harmonic of the line current. The large electrolytic capacitors which are normally chosen for the output capacitor have an equivalent series resistance which changes with frequency and is generally high at low frequencies. The amount of current which the capacitor can handle is generally determined by the temperature rise. It is usually not necessary to calculate an exact value for the temperature rise. It is usually adequate to calculate the temperature rise due to the high frequency ripple current and the low frequency ripple current and add them together. The capacitor data sheet will provide the necessary ESR and temperature rise information.

The hold-up time of the output often dominates any other consideration in output capacitor selection. Hold-up is the length of time that the output voltage remains within a specified range after input power has been turned off. Hold-up times of 15 to 50 milliseconds are typical. In off-line power supplies with a 400Vdc output the hold-up requirement generally works out to between 1 and 2µF per watt of output. In our 250W example the output capacitor is 450µF. If hold-up is not required the capacitor will be much smaller, perhaps 0.2µF per watt, and then ripple current and ripple voltage are the major concern.

Hold-up time is a function of the amount of energy stored in the output capacitor, the load power, output voltage and the minimum voltage the load will operate at. This can be expressed in an equation to define the capacitance value in terms of the hold-up time.

$$Co = \frac{2 \times Pout \times \Delta t}{Vo^2 - Vo(min)^2}$$

Where Co is the output capacitor, Pout is the load power, $\Delta t$ is the hold-up time, Vo is the output voltage and Vo(min) is the minimum voltage the load will operate at. For the example converter Pout is 250W, $\Delta t$ is 64msec, Vo is 400V and Vo(min) is 300V so Co is 450µF.

Switch and Diode

The switch and diode must have ratings which are sufficient to insure reliable operation. The choice of these components is beyond the scope of this Application Note. The switch must have a current rating at least equal to the maximum peak current in

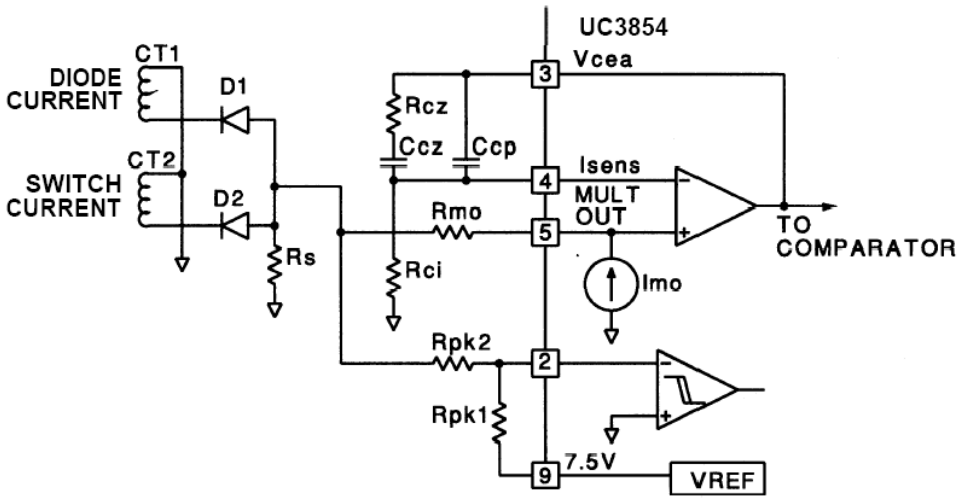



Figure 8.
Current Transformers Used
with Negative Output

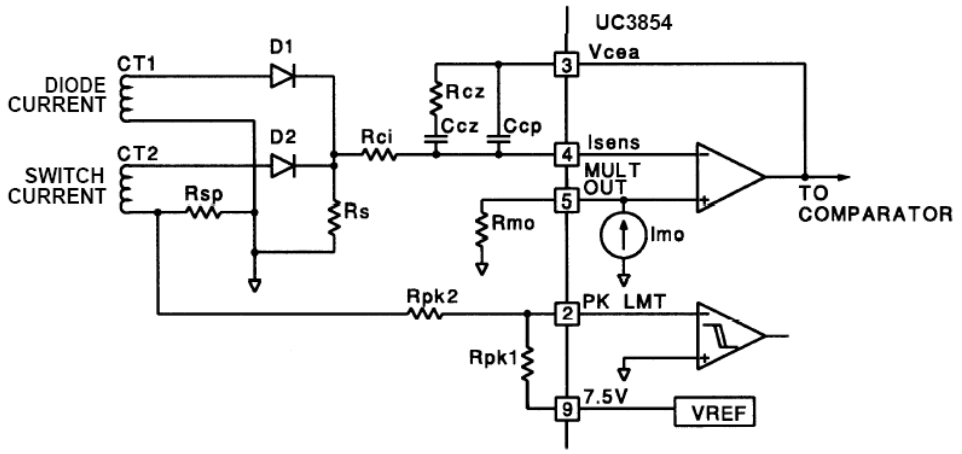



Figure 9.
Current Transformers Used
with Positive Output

the inductor and a voltage rating at least equal to the output voltage. The same is true for the output diode. The output diode must also be very fast to reduce the switch turn-on power dissipation and to keep its own losses low. The switch and diode must have some level of derating and this will vary depending on the application.

For the example circuit the diode is a high speed, high voltage type with 35ns reverse recovery, 600Vdc breakdown, and 8A forward current ratings. The power MOSFET in the example circuit has a 500Vdc breakdown and 23Adc current rating. A major portion of the losses in the switch are due to the turn-off current in the diode. The peak power dissipation in the switch is high since it must carry full load current plus the diode reverse recovery current at full output voltage from the time it turns on until the diode turns off. The diode in the example circuit was chosen for its fast turn off and the switch was oversized to handle the high peak power dissipation. A turn on snubber for the switch would have allowed a smaller switch and a slightly slower diode.

Current Sensing

There are two general methods for current sensing, a sense resistor in the ground return of the converter or two current transformers. The sense resistor is the least expensive method and is most appropriate at low power or current levels. The power dissipation in the resistor may become quite large at higher current levels and in that case the current transformers are more appropriate. Two current transformers are required, one for the switch current and one for the diode current, to produce an analog of the inductor current as is required for average current mode control. The current transformers must operate over a very wide duty factor range and this can be difficult to achieve without saturating them. Current transformer operation is outside the scope of this paper but Unitrode has Design Note DN-41 which discusses the problem in some detail.

The current transformers may be configured for either a positive output voltage or a negative output voltage. In the negative output configuration, shown in Figure 8, the peak current limit on pin 2 of the UC3854 is easy to implement. In the positive output configuration, shown in Figure 9, this feature may be lost. It can be added back by putting another resistor in series with the ground leg of the current transformer which senses the switch current.

The configuration of the multiplier output and the current error amplifier are different depending on whether a resistor is used for current sensing or whether current transformers with positive output voltages are used for current sensing. Both work equally well and the configurations of the current error amplifier are shown in Figures 8 and 9 respectively. The positive output current transformer configuration requires the inverting input to the integrator be connected to the sense resistor and the resistor at the output of the multiplier be connected to ground. (see Figure 9) The voltage at the output of the multiplier is not zero but is the programming voltage for the current loop and it will have the half sine wave shape which is necessary for the current loop.

The resistor current sense configuration is used in the example converter (Figure 6) so the inverting input to the current error amplifier (pin 4) is connected to ground through Rci. The current error amplifier is configured as an integrator at low frequencies for average current mode control so the average voltage at the non-inverting input of the current error amplifier (pin 5, which it shares with the multiplier output) must be zero. The non-inverting input to the current error amplifier acts like a summing junction for the current control loop and adds the multiplier output current to the current from the sense resistor (which flows through the programming resistor Rmo). The difference controls the boost regulator. The voltage at the inverting input of the current error amplifier (pin 4) will be small at low frequencies because the gain at low frequencies is large. The gain at high frequencies is small so relatively large voltages at the switching frequency may be present. But, the average voltage on pin 4 must be zero because it is connected through Rci to ground.

The voltage across Rs, the current sense resistor in the example converter, goes negative with respect to ground so it is important to be sure that the pins of the UC3854 do not go below ground. The voltage across the sense resistor should be kept small and pins 2 and 5 should be clamped to prevent their going negative. A peak value of 1 volt or so across the sense resistor provides a signal large enough to have good noise margin but which is small enough to have low power dissipation. There is a great deal of flexibility in choosing the value of the sense resistor. A 0.25 ohm resistor was chosen for Rs in the example converter and at the worst case peak current of 5.6 amps gives a maximum voltage of 1.40V peak.

Peak Current Limit

The peak current limit on the UC3854 turns the switch off when the instantaneous current through it exceeds the maximum value and is activated when pin 2 is pulled below ground. The current limit value is set by a simple voltage divider from the reference voltage to the current sense resistor.

The equation for the voltage divider is given below:

$$Rpk2 = \frac{Vrs \times Rpk1}{Vref}$$

Where Rpk1 and Rpk2 are the resistors of the voltage divider, Vref is 7.5 volts on the UC3854, and Vrs is the voltage across the sense resistor Rs at the current limit point. The current through Rpk2 should be around 1 mA. The peak current limit in the example circuit is set at 5.4 amps with an Rpk1 of 10K and Rpk2 of 1.8K. A small capacitor, Cpk, has been added to give extra noise immunity when operating at low line and this also increases the current limit slightly.

Multiplier Set-up

The multiplier/divider is the heart of the power factor corrector. The output of the multiplier programs the current loop to control the input current to give a high power factor. The output of the multiplier is therefore a signal which represents the input line current.

Unlike most design tasks where the design begins at the output and proceeds to the input the design of the multiplier circuits must begin with the inputs. There are three inputs to the multiplier circuits: the programming current Iac (pin 6) the feedforward voltage Vff from the input (pin 8) and the voltage error amplifier output voltage Vvea (pin 7). The multiplier output current is Imo (pin 5) and it is related to the three inputs by the following equation:

$$Imo = \frac{Km \times Iac \times (Vvea - 1)}{Vff^2}$$

Where Km is a constant in the multiplier and is equal to 1.0, Iac is the programming current from the rectified input voltage, Vvea is the output of the voltage error amplifier and Vff is the feedforward voltage.

Feedforward Voltage

Vff is the input to the squaring circuit and the UC3854 squaring circuit generally operates with a Vff range of 1.4 to 4.5 volts. The UC3854 has an internal clamp which limits the effective value of Vff to 4.5 volts even if the input goes above that value. The voltage divider for the Vff input has three resistors (Rff1, Rff2 and Rff3 - see Figure 6) and two capacitors (Cff1 and Cff2) and so it filters as well as providing two outputs. The resistors and capacitors of the divider form a second order low pass filter so the DC output is proportional to the average value of the input half sine wave. The average value is 90% of the RMS value of a half sine wave. If the RMS value of the AC input voltage is 270Vac the average value of a half sine will be 243Vdc and the peak will be 382V.

The Vff voltage divider has two DC conditions to meet. At high- input line voltage Vff should not be greater than 4.5 volts. At this voltage the Vff input clamps so the feedforward function is lost. The voltage divider should be set up so that Vff is equal to 1.414 volts when Vin is at its low line value and the upper node of the voltage divider, Vffc, should be about 7.5 volts. This allows Vff to be clamped as described in Unitrode Design Note DN-39B. There is an internal current limit which holds the multiplier output constant if the Vff input goes below 1.414 volts. The Vff input should always be set up so that Vff is equal to 1.414 volts at the minimum input voltage. This may cause Vff to clip on the high end of the input voltage range if there is an extremely wide AC line voltage input range. However, it is preferable to have Vff clip at the high end rather than to have the multiplier output clip on the low end of the range. If Vff clips the voltage loop gain will change but the effect on the overall system will be small whereas the multiplier clipping will cause large amounts of distortion in the input current waveform.

The example circuit uses the UC3854 so the maximum value of Vff is 4.5 volts. If Rff1, the top resistor of the divider, is 910K and Rff2, the middle resistor, is 91 K and Rff3, the bottom resistor, is 20K the maximum value of Vff will be 4.76 volts when the input voltage is 270Vac RMS and the DC average value will be 243 volts. When the input voltage is 80Vac RMS the average value is 72 volts and Vff is 1.41Vdc. Also at Vin=80Vac the voltage at the upper node on the voltage divider, Vffc, will be 7.83 volts. Note that the high end of the range goes above 4.5 volts so that the low end of the range will not go below 1.41 volts.

The output of the voltage error amplifier is the next piece of the multiplier setup. The output of the voltage error amplifier, Vvea, is clamped inside the UC3854 at 5.6 volts. The output of the voltage error amplifier corresponds to the input power of the converter. The feedforward voltage causes the power input to remain constant at given Vvea voltage regardless of line voltage changes. If 5.0V is established as the maximum normal operating level then 5.6V gives an overload power limit which is 12% higher.

The clamp on the output of the voltage error amplifier is what sets the minimum value of Vff at 1.414 volts. This can be seen by plugging these values into the equation for the multiplier output current given above. When Vff is large the inherent errors of the multiplier are magnified because Vvea/Vff becomes small. If the application has a wide input voltage range and if a very low harmonic distortion

is required then Vff may be changed to the range of 0.7 to 3.5 volts. To do this an external clamp MUST be added to the voltage error amplifier to hold its output below 2.00 volts. In general, however, this is not a recommended practice.

Multiplier Input Current

The operating current for the multiplier comes from the input voltage through Rvac. The multiplier has the best linearity at relatively high currents, but the recommended maximum current is 0.6mA. At high line the peak voltage for the example circuit is 382Vdc and the voltage on pin 6 of the UC3854 is 6.0Vdc. A 620K value for Rvac will give an Iac of 0.6mA maximum. For proper operation near the cusp of the input waveform when Vin=0 a bias current is needed because pin 6 is at 6.0Vdc. A resistor, Rb1, is connected from Vref to pin 6 to provide the small amount of bias current needed. Rb1 is equal to Rvac/4. In the example circuit a value of 150K for Rb1 will provide the correct bias.

The maximum output of the multiplier occurs at the peak of the input sine wave at low line. The maximum output current from the multiplier can be calculated from the equation for Imo, given above, for this condition. The peak value of Iac will be 182 microamps when Vin is at low line. Vvea will be 5.0 volts and Vff will be 2.0. Imo will then be 365 microamps maximum. Imo may not be greater than twice Iac so this represents the maximum current available at this input voltage and the peak input current to the power factor corrector will be limited accordingly.

The Iset current places another limitation on the multiplier output current. Imo may not be larger than 3.75 / Rset. For the example circuit this gives Rset = 10.27K maximum so a value of 10K is chosen.

The current out of the multiplier, Imo, must be summed with a current proportional to the inductor current to close the voltage feedback loop. Rmo, a resistor from the output of the multiplier to the current sense resistor, performs the function and the multiplier output pin becomes the summing junction. The average voltage on pin 5 will be zero under normal operation but there will be switching frequency ripple voltage which is amplitude modulated at twice the line frequency. The peak current in the boost inductor is to be limited to 5.6 amps in the example circuit and the current sense resistor is 0.25 ohms so the peak voltage across the sense resistor is 1.4 volts. The maximum multiplier output current is 365 microamps so the summing resistor, Rmo, must be 3.84K and a 3.9K resistor is chosen.

Oscillator Frequency

The oscillator charging current is Iset and is determined by the value of Rset and the oscillator frequency is set by the timing capacitor and the charging current. The timing capacitor is determined from:

$$Ct = \frac{1.25}{Rset \times fs}$$

Where Ct is the value of the timing capacitor and fs is the switching frequency in Hertz. For the example converter fs is 100KHz and Rset is 10K so Ct is **0.00125μF.**

Current Error Amplifier Compensation

The current loop must be compensated for stable operation. The boost converter control to input current transfer function has a single pole response at high frequencies which is due to the impedance of the boost inductor and the sense resistor (Rs) forming a low pass filter. The equation for the control to input current transfer function is:

$$\frac{Vrs}{Vcea} = \frac{Vout \times Rs}{Vs \times sL}$$

Where Vrs is the voltage across the input current sense resistor and Vcea is the output of the current error amplifier. Vout is the DC output voltage, Vs is the peak-to-peak amplitude of the oscillator ramp, sL is the impedance of the boost inductor (also jwL), and Rs is the sense resistor (with a current transformer it will be Rs/N). This equation is only valid for the region of interest between the resonant frequency of the filter (LCo) and the switching frequency. Below resonance the output capacitor dominates and the equation is different.

The compensation of the current error amplifier provides flat gain near the switching frequency and uses the natural roll off of the boost power stage to give the correct compensation for the total loop. A zero at low frequency in the amplifier response gives the high gain which makes average current mode control work. The gain of the error amplifier near the switching frequency is determined by matching the down slope of the inductor current when the switch is off with the slope of the ramp generated by the oscillator. These two signals are the inputs of the PWM comparator in the UC3854.

The downslope of the inductor current has the units of amps per second and has a maximum value when the input voltage is zero. In other words, when the voltage differential between the input and output of the boost converter is greatest. At this point (Vin=0) the inductor current is given by the ratio of the converter output voltage and the inductance (Vo/L). This current flows through the current sense resistor Rs and produces a voltage

with the slope VoRs/L (with current sense transformers it will be VoRs/NL). This slope, multiplied by the gain of the current error amplifier at the switching frequency, must be equal to the slope of the oscillator ramp (also in volts per second) for proper compensation of the current loop. If the gain is too high the slope of the inductor current will be greater than the ramp and the loop can go unstable. The instability will occur near the cusp of the input waveform and will disappear as the input voltage increases.

The loop crossover frequency can be found from the above equation if the gain of the current error amplifier is multiplied with it and it is set equal to one. Then rearrange the equation and solve for the crossover frequency. The equation becomes:

$$fci = \frac{Vout \times Rs \times Rcz}{Vs \times 2\pi L \times Rci}$$

Where fci is the current loop crossover frequency and Rcz/Rci is the gain of the current error amplifier. This procedure will give the best possible response for the current loop.

In the example converter the output voltage is 400Vdc and the inductor is 1.0mH so the down slope of inductor current is 400mA per microsecond. The current sense resistor is 0.25 ohms so the input to the current error amplifier is 100mV per microsecond. The oscillator ramp of the UC3854 has a peak to peak value of 5.2V and the switching frequency is 100KHz so the ramp has a slope of 0.52 volts per microsecond. The current error amplifier must have a gain of 5.2 at the switching frequency to make the slopes equal. With an input resistor (Rci) value of 3.9K the feedback resistance (Rcz) is 20K to give the amplifier a gain of 5.2. The current loop crossover frequency is 15.9KHz.

The placement of the zero in the current error amplifier response must be at or below the crossover frequency. If it is at the crossover frequency the phase margin will be 45 degrees. If the zero is lower in frequency the phase margin will be greater. A 45 degree phase margin is very stable, has low overshoot and has good tolerance for component variations. The zero must be placed at the crossover frequency so the impedance of the capacitor at that frequency must be equal to the value of Rcz. The equation is: Ccz = 1 / ($2\pi$ x fci x Rcz). The example converter has Rcz=20K and fci=l5.9KHz so Ccz=500pF. A value of 620pF was chosen to give a little more phase margin.

A pole is normally added to the current error amplifier response near the switching frequency to reduce noise sensitivity. If the pole is above half the switching frequency the pole will not affect the frequency response of the control loop. The example converter uses a 62pF capacitor for Ccp which gives a pole at 128KHz. This is actually above the switching frequency so a larger value of capacitor could have been used but 62pF is adequate in this case.

Voltage Error Amplifier Compensation

The voltage control loop must be compensated for stability but because the bandwidth of the voltage loop is so small compared to the switching frequency the requirements for the voltage control loop are really driven by the need to keep the input distortion to a minimum rather than by stability. The loop bandwidth must be low enough to attenuate the second harmonic of the line frequency on the output capacitor to keep the modulation of the input current small. The voltage error amplifier must also have enough phase shift so that what modulation remains will be in phase with the input line to keep the power factor high.

The basic low frequency model of the output stage is a current source driving a capacitor. The power stage and the current feedback loop compose the current source and the capacitor is the output capacitor. This forms an integrator and it has a gain characteristic which rolls off at a constant 20dB per decade rate with increasing frequency. If the voltage feedback loop is closed around this it will be stable with constant gain in the voltage error amplifier. This is the technique which is used to stabilize the voltage loop. However, its performance at reducing distortion due to the second harmonic output ripple is miserable. A pole in the amplifier response is needed to reduce the amplitude of the ripple voltage and to shift the phase by 90 degrees. The distortion criteria is used to define the gain of the voltage error amplifier at the second harmonic of the line frequency and then the unity gain crossover frequency is found and is used to determine the pole location in the voltage error amplifier frequency response.

The first step in designing the voltage error amplifier compensation is to determine the amount of ripple voltage present on the output capacitor. The peak value of the second harmonic voltage is given by:

$$Vopk = \frac{Pin}{2\pi fr \times Co \times Vo}$$

Where Vopk is the peak value of the output ripple voltage (the peak to peak value will be twice this), fr is the ripple frequency which is the second harmonic of the input line frequency, Co is the value of the output capacitance and Vo is the DC output voltage. The example converter has a peak ripple voltage of 1.84Vpk.

The amount of distortion which the ripple contributes to the input must be decided next. This deci-

sion is based on the specification for the converter. The example converter is specified for 3% THD so 0.75% THD is allocated to this component. This means that the ripple voltage at the output of the voltage error amplifier is limited to 1.5%. The voltage error amplifier has an effective output range ($\Delta$Vvea) of 1.0 to 5.0 volts so the peak ripple voltage at the output of the voltage error amplifier is give by Vvea(pk) = %Ripple x $\Delta$Vvea. The example converter has a peak ripple voltage at the output of the voltage error amplifier of 60mVpk.

The gain of the voltage error amplifier, Gva, at the second harmonic ripple frequency is the ratio of the two values given above. The peak ripple voltage allowed on the output of the voltage error amplifier is divided by the peak ripple voltage on the output capacitor. For the example converter Gva is 0.0326.

The criteria for the choice of Rvi, the next step in the design process, are reasonably vague. The value must be low enough so that the opamp bias currents will not have a large effect on the output and it must be high enough so that the power dissipation is small. In the example converter a 511 K resistor was chosen for Rvi and it will have power dissipation of about 300mW.

Cvf, the feedback capacitor sets the gain at the second harmonic ripple frequency and is chosen to give the voltage error amplifier the correct gain at the second harmonic of the line frequency. The equation is simply:

$$Cvf = \frac{1}{2\pi fr \times Rvi \times Gva}$$

The example converter has a Cvf value of 0.08µF. If this value is rounded down to Cvf=0.047µF the phase margin will be a little better with only a little more distortion so this value was chosen.

The output voltage is set by the voltage divider Rvi and Rvd. The value of Rvi is already determined so Rvd is found from the desired output voltage and the reference voltage which is 7.50Vdc. In the example Rvd=I0K will give an output voltage of 390Vdc. This could be trimmed up to 400VDC with a 414K resistor in parallel with Rvd but for this application 390Vdc is acceptable. Rvd has no effect on the AC performance of the active power factor corrector. Its only effect is to set the DC output voltage.

The frequency of the pole in the voltage error amplifier can be found from setting the gain of the loop equation equal to one and solving for the frequency. The voltage loop gain is the product of the error amplifier gain and the boost stage gain, which can be expressed in terms of the input power. The multiplier, divider and squarer terms can all be lumped into the power stage gain and their effect is to transform the output of the voltage error amplifier into a power control signal as was noted earlier. This allows us to express the transfer function of the boost stage simply in terms of power. The equation is:

$$Gbst = \frac{Pin \times Xco}{\Delta Vvea \times Vo}$$

Where Gbst is the gain of the boost stage including the multiplier, divider and squarer, Pin is the average input power, Xco is the impedance of the output capacitor, $\Delta$Vvea is the range of the voltage error amplifier output voltage (4 volts on the UC3854) and Vo is the DC output voltage.

The gain of the error amplifier above the pole in its frequency response is given by:

$$Gva = \frac{Xcf}{Rvi}$$

Where Gva is the gain of the voltage error amplifier, Xcf is the impedance of the feedback capacitance and Rvi is the input resistance.

The gain of the total voltage loop is the product of Gbst and Gva and is given by the this equation:

$$Gv = \frac{Pin \times Xco \times Xcf}{\Delta Vvea \times Vo \times Rvi}$$

Note that there are two terms which are dependent on f, Xco and Xcf. This function has a second order slope (-40dB per decade) so it must be a function of frequency squared. To solve for the unity gain frequency set Gv equal to one and rearrange the equation to solve for fvi. Xco is replaced with $1/(2\pi fCo)$ and Xcf is replaced with $1/(2\pi fCvf)$.

The equation becomes:

$$fvi^2 = \frac{Pin}{\Delta Vvea \times Vo \times Rvi \times Co \times Cvf \times (2\pi)^2}$$

Solving for fvi in the example converter gives fvi=19.14Hz. The value of Rvf can now be found by setting it equal to the impedance of Cvf at fvi. The equation is: $Rvf=1/(2\pi fviCvf)$.

In the example converter a value of 177K is calculated and 174K is used.

Feedforward Voltage Divider Filter Capacitors

The percentage of second harmonic ripple voltage on the feedforward input to the multiplier results in the same percentage of third harmonic ripple current on the AC line. The capacitors in the feedforward voltage divider (Cff1 and Cff2) attenuate the ripple voltage from the rectified input voltage. The

second harmonic ripple is 66.2% of the input AC line voltage. The amount of attenuation required, or the "gain" of the filter, is simply the amount of third harmonic distortion allocated to this distortion source divided by 66.2% which is the input to the divider. The example circuit has an allocation of 1.5% total harmonic distortion from this input so the required attenuation is Gff = 1.5 / 66.2 = 0.0227.

The recommended divider string impliments a second order filter because this gives a much faster response to changes in the RMS line voltage. Typically, it is about six times faster. The two poles of the filter are placed at the same frequency for the widest bandwidth. The total gain of the filter is the product of the gain of the two filter section so the gain of each section is the square root of the total gain. The two sections of the filter do not interact much because the impedances are different so they can be treated separately. In the example converter the gain of each filter section at the second harmonic frequency is 0.0227 or 0.15 for each section. This same relationship holds for the cutoff frequency which is needed to find the capacitor values. These are simple real poles so the cutoff frequency is the section gain times the ripple frequency or:

$$fc = \sqrt{Gff} \times fr$$

The example converter has a filter gain of 0.0227 and a section gain of 0.15 and a ripple frequency of 120Hz so the cutoff frequency is fc=0.15x120=18Hz.

The cutoff frequency is used to calculate the values for the filter capacitors since, in this applivation, the impedance of the capacitor will equal the impedance of the load resistance at the cutoff frequency. The two equations given below are used to calculate the two capacitor values.

$$Cff1 = \frac{1}{2\pi \times fp \times Rff2}$$

$$Cff2 = \frac{1}{2\pi \times fp \times Rff3}$$

In the example converter Rff2 is 91K and Rff3 is 20K; so,

**Cff1=1/2πx18x91K=0.1μF;**

**Cff2=1/2πx18x20K=0.44μF;**

**so choose Cff2=0.47μF.**

This completes the design of the major circuits of an active power factor corrector.

DESIGN PROCEDURE SUMMARY

This section contains a brief, step-by-step summary of the design procedure for an active power factor corrector. The example circuit used above is repeated here.

1. Specifications: Determine the operating requirements for the active power factor corrector.

   Example:

   Pout (max): 250W
   Vin range: 80-270Vac
   Line frequency range: 47-65Hz
   Output voltage: 400Vdc

2. Select switching frequency:

   Example:

   100KHz

3. Inductor selection:

   A. Maximum peak line current. Pin = Pout(max)

   $$Ipk = \frac{\sqrt{2} \times Pin}{Vin\ (\ min\ )}$$

   Example:

   Ipk=1.41 x250/80=4.42 amps

   B. Ripple current.

   $\Delta I$ = 0.2 x Ipk

   Example:

   $\Delta I$=0.2x4.42= = 0.2x4.42 = 0.9 amps peak to peak

   C. Determine the duty factor at Ipk where Vin(peak) is the peak of the rectified line voltage at low line.

   $$D = \frac{Vo - Vin\ (\ peak\ )}{Vo}$$

   Example:

   D=(400-113)/400=0.71

   D. Calculate the inductance. fs is the switching frequency.

   $$L = \frac{Vin \times D}{fs \times \Delta I}$$

   Example:

   L=(113x.71)/(100,000x0.9)=0.89mH

   Round up to 1.0mH.

4. Select output capacitor. With hold-up time, use the equation below. Typical values for Co are 1 μF to 2μF per watt. If hold-up is not required use the second harmonic ripple voltage and total capacitor power dissipation to determine minimum size of the capacitor. $\Delta t$ is the hold-up time in seconds and V1 is the minimum output

capacitor voltage.

$$Co = \frac{2 \times Pout \times \Delta t}{Vo^2 - V1^2}$$

Example:
Co=(2x250x34msec)/(400-350)=450µF

5. Select current sensing resistor. If current transformers are used then include the turns ratio and decide whether the output will be positive or negative relative to circuit common. Keep the peak voltage across the resistor low. 1.0V is a typical value for Vrs.

A. Find $Ipk(max) = Ipk + \frac{\Delta I}{2}$

Example:

Ipk(max)=4.42+0.45 = 5.0amps peak

B. Calculate sense resistor value.

$$Rs = \frac{Vrs}{Ipk(max)}$$

Example:

Rs=1.0/5.0=0.20 ohms. Choose 0.25ohms

C. Calculate the actual peak sense voltage.

Vrs(pk)=Ipk(max)xRs

Example:

Vrs(pk)=5.0x0.25=1.25V

6. Set independent peak current limit. Rpk1 and Rpk2 are the resistors in the voltage divider. Choose a peak current overload value, Ipk(ovld). A typical value for Rpk1 is 10K.

$$Vrs(ovld) = Ipk(olvd) \times Rs$$

Example:

Vrs(ovld)=5.6x0.25=1.4V

$$Rpk2 = \frac{Vrs(ovld) \times Rpk1}{Vref}$$

Example:

Rpk2=(1.4x10K)/7.5=1.87K. Choose 1.8K

7. Multiplier setup. The operation of the multiplier is given by the following equation. Imo is the multiplier output current, Km=1 , Iac is the multiplier input current, Vff is the feedforward voltage and Vvea is the output of the voltage error amplifier.

$$Imo = \frac{Kmxlacx(Vvea-1)}{vff^2}$$

A. Feedforward voltage divider. Change Vin from RMS voltage to average voltage of the rectified input voltage. At Vin(min) the voltage at Vff should be 1.414 volts and the voltage at Vffc, the other divider node, should be about 7.5 volts. The average value of Vin is given by the following equation where Vin(min) is the RMS value of the AC input voltage:

$$Vin(av) = Vin(min) \times 0.9$$

The following two equations are used to find the values for the Vff divider string. A value of 1 Megohm is usually chosen for the divider input impedance. The two equations must be solved together to get the resistor values.

$$vff = 1.414v = \frac{Vin(av) \times Rff3}{Rff1 + Rff2 + Rff3}$$

$$Vnode = 7.5V = \frac{Vin(av)x(Rff2+Rff3)}{Rff1 + Rff2 + Rff3}$$

Example:

Rff1=910K, Rff2=91K, and Rff3=20K

B. Rvac selection. Find the maximum peak line voltage.

$$Vpk(max) = \sqrt{2} \times Vin(max)$$

Example:

Vpk(max)=1.414x270=382Vpk

Divide by 600 microamps, the maximum multiplier input current.

$$Rvac = \frac{Vpk(max)}{600E\text{-}6}$$

Example:

Rvac=(382)/6E-4=637K. Choose 620K

C. Rb1 selection. This is the bias resistor. Treat this as a voltage divider with Vref and Rvac and then solve for Rb1. The equation becomes:

Rb1 = 0.25 Rvac

Example:

Rb1=0.25Rvac=155K. Choose 150K

D. Rset selection. Imo cannot be greater than twice the current through Rset. Find the multiplier input current, Iac, with Vin(min). Then calculate the value for Rset based on the value of Iac just calculated.

$$Iac(min) = \frac{Vin(pk)}{Rvac}$$

Example:

Iac(

$$Rset = \frac{3.75}{2 \times Iac(min)}$$

Example:

Rset=3.75V/(2x182μA)=10.3Kohms.

Choose 10 Kohms

E. Rmo selection. The voltage across Rmo must be equal to the voltage across Rs at the peak current limit at low line input voltage.

$$Rmo = \frac{Vrs\ (pk)\ x\ 1.12}{2\ x\ Iac(min)}$$

Example:

Rmo=(l.25x1.12)/(2x182E-6)=3.84K.

Choose 3.9Kohms

8. Oscillator frequency. Calculate Ct to give the desired switching frequency.

$$Ct = \frac{1.25}{Rset \times fs}$$

Example:

Ct=1.25/(10K x 100K)=1.25nF.

9. Current error amplifier compensation.

A. Amplifier gain at the switching frequency. Calculate the voltage across the sense resistor due to the inductor current downslope and then divide by the switching frequency. With current transformers substitute (Rs/N) for Rs. The equation is:

$$\Delta Vrs = \frac{Vo \times Rs}{L \times fs}$$

Example:

ΔVrs=(400x0.25)/(0.001 =(400x0.25)/(0.001 x100,000)=1.0Vpk

This voltage must equal the peak to peak amplitude of Vs, the voltage on the timing capacitor (5.2 volts). The gain of the error amplifier is therefore given by:

$$Gca = \frac{Vs}{\Delta Vrs}$$

Example:

Gca=5.2/1.0=5.2

B. Feedback resistors. Set Rci equal to Rmo.

Rci = Rmo

Rcz = Gca x Rci

Example:

Rcz=5.2x3.9K=20Kohms

C. Current loop crossover frequency.

$$fci = \frac{Vout \times Rs \times Rcz}{Vs \times 2\pi L \times Rci}$$

Example:

fci=(400x0.25x20K)/(5.2x2πx0.001

=15.7KHz

D. Ccz selection. Choose a 45 degree phase margin. Set the zero at the loop crossover frequency.

$$Ccz = \frac{1}{2\pi \times fci \times Rcz}$$

Example:

Ccz=1/(2πx15.7Kx20K)=507pF.

Choose 620pF

E. Ccp selection. The pole must be above fs/2.

$$Ccp = \frac{1}{2\pi \times fs \times Rcz}$$

Example:

Ccp=1/(2πx1 100Kx20K)=80pf.

Choose 62pF

10. Harmonic distortion budget. Decide on a maximum THD level. Allocate THD sources as necessary. The predominant AC line harmonic is third. Output voltage ripple contributes 1/2% third harmonic to the input current for each 1% ripple at the second harmonic on the output of the error amplifier. The feedforward voltage, Vff, contributes 1% third harmonic to the input current for each 1% second harmonic at the Vff input to the UC3854.

Example:

3% third harmonic AC input current is chosen as the specification. 1.5% is allocated to the Vff input and 0.75% is allocated to the output ripple voltage or 1.5% to Vvao. The remaining 0.75% is allocated to miscellaneous nonlinearities.

11. Voltage error amplifier compensation.

A. Output ripple voltage. The output ripple is given by the following equation where fr is the second harmonic ripple frequency:

$$Vo\ (pk) = \frac{Pin}{2\pi fr \times Co \times Vo}$$

Example:

Vo(pk)=250/(2π120x450E-6x400)=1.84Vac

B. Amplifier output ripple voltage and gain. Vo(pk) must be reduced to the ripple voltage allowed at the output of the voltage error amplifier. This sets the gain of the voltage error amplifier at the second harmonic frequency. The equation is:

$$Gva = \frac{\Delta Vvao \times \%Ripple}{Vo\ (pk)}$$

For the UC3854 Vvao is 5-1=4V

Example:

Gva=(4x0.015)/1.84=0.0326

C. Feedback network values. Find the component values to set the gain of the voltage error amplifier. The value of Rvi is reasonably arbitrary.

Example:

Choose Rvi=511K

$$Cvf = \frac{1}{2\pi \times fr \times Rvi \times Gva}$$

Example:
Cvf=1/(2πx120x511Kx0.0326)=0.08µF.

Choose 0.047µF

D. Set DC output voltage.

$$Rvd = \frac{Rvi \times Vref}{Vo - Vref}$$

Example:

Rvd=(511Kx7.5)/(400-7.5)=9.76K.

Choose 10.0K

E. Find pole frequency. fvi = unity gain frequency of voltage loop.

$$fvi^2 = \frac{Pin}{\Delta Vvao \times Vo \times Rvi \times Co \times Cvf \times (2\pi)^2}$$

Example:

$$fvi = \sqrt{(250/(4x400x511Kx450E-6x47E-9x39.5))} =$$

19.1 Hz

F. Find Rvf.

$$Rvf = \frac{1}{2\pi \times fvi \times Cvf}$$

Example:

Rvf=1/(2πx19.1 x47E-9)=177K. Choose 174K

12. Feedforward voltage divider capacitors. These capacitors determine the contribution of Vff to the third harmonic distortion on the AC input current. Determine the amount of attenuation needed. The second harmonic content of the rectified line voltage is 66.2%. %THD is the allowed percentage of harmonic distortion budgeted to this input from step 10 above.

$$Gff = \frac{\%THD}{66.2\%}$$

Example:

Gff=1.5/66.2=0.0227

Use two equal cascaded poles. Find the pole frequencies. fr is the second harmonic ripple frequency.

$$fp = \sqrt{Gff} \times fr$$

Example:

fp=0.15xl20=18Hz

Select Cff1 and Cff2.

$$Cff1 = \frac{1}{2\pi \times fp \times Rff2}$$

$$Cff2 = \frac{1}{2\pi \times fp \times Rff3}$$

Example:

Cff1=1/(2πx18x91K)=0.097µF. Choose 0.10µF

Cff2=1/(2πx18x20K)=0.44µF. Choose 0.47µF

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S. Freeland, "Input-Current Shaping for Single-Phase Ac-Dc Power Converters," Ph.D. Thesis, California Institute of Technology, 1988

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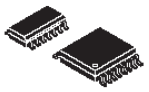
# APPENDIX B: Datasheets Of The Components

TEXAS INSTRUMENTS



**UC1854B**
**UC2854A, UC2854B**
**UC3854A, UC3854B**

SLUS329A – JUNE 1998 – REVISED AUGUST 2003

## ADVANCED HIGH-POWER FACTOR PREREGULATOR

### FEATURES

- Controls Boost PWM to Near-Unity Power Factor
- Limits Line Current Distortion To < 3%
- World-Wide Operation Without Switches
- Accurate Power Limiting
- Fixed-Frequency Average Current-Mode Control
- High Bandwidth (5 MHz), Low-Offset Current Amplifier
- Integrated Current- and Voltage Amplifier Output Clamps
- Multiplier Improvements: Linearity, 500 mV $V_{AC}$ Offset (Eliminates External Resistor), 0 V to 5 V Multout Common-Mode Range
- $V_{REF}$ GOOD Comparator
- Faster and Improved Accuracy ENABLE Comparator
- UVLO Options (16 V/10 V or 10.5 V/10 V)
- 300-μA Start-Up Supply Current

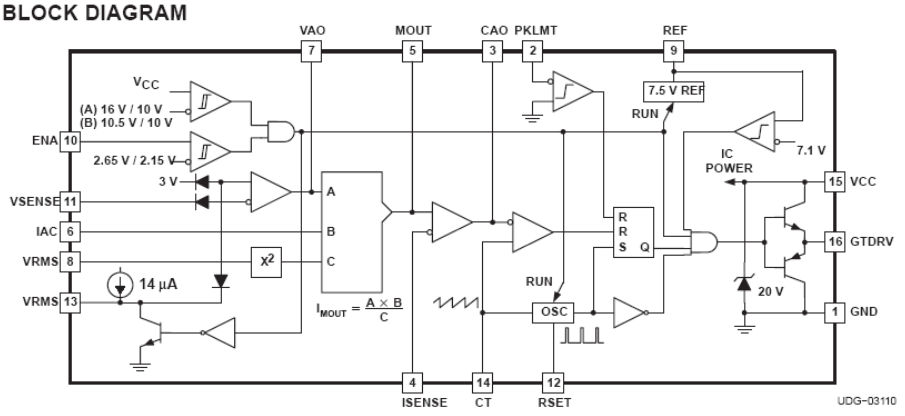
### DESCRIPTION

The UC3854A/B products are pin compatible enhanced versions of the UC3854. Like the UC3854, these products provide all of the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage. To do this the UC3854A/B uses average current mode control. Average current mode control maintains stable, low distortion sinusoidal line current without the need for slope compensation, unlike peak current mode control.

A 1% 7.5 V reference, fixed frequency oscillator, PWM, voltage amplifier with soft-start, line voltage feedforward ($V_{RMS}$ squarer), input supply voltage clamp, and over current comparator round out the list of features.

Available in the 16-pin N (PDIP), DW (SOIC-Wide), and J (CDIP) and 20-pin Q (PLCC) package. See ordering information on page 3 for availability by temperature range.

### BLOCK DIAGRAM



## DESCRIPTION (continued)

The UC3854A/B products improve upon the UC3854 by offering a wide bandwidth, low offset current amplifier, a faster responding and improved accuracy enable comparator, a VREF GOOD comparator, UVLO threshold options (16 V/10 V for offline, 10.5 V/10 V for startup from an auxiliary 12 V regulator), lower startup supply current, and an enhanced multiply/divide circuit. New features like the amplifier output clamps, improved amplifier current sinking capability, and low offset VAC pin reduce the external component count while improving performance. Improved common mode input range of the multiplier output/current amplifier input allow the designer greater flexibility in choosing a method for current sensing. Unlike its predecessor, $R_{SET}$ controls only oscillator charging current and has no effect on clamping the maximum multiplier output current. This current is now clamped to a maximum of $2 \times I_{AC}$ at all times which simplifies the design process and provides foldback power limiting during brownout and extreme low line conditions.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | UCX854A, UCX854B | UNIT |
|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 22 | V |
| GTDRV current, $I_{GTDRV}$ | Continuous | 0.5 | A |
| GTDRV Current, $I_{GTDRV}$ | 50% duty cycle | 1.5 | A |
| Input voltage | VSENSE, VRMS, ISENSE MOUT | 11 | V |
| | PKLMT | 5 | V |
| Input current | RSET, IAC, PKLMT, ENA | 10 | mA |
| Power dissipation | | 1 | W |
| Junction temperature, $T_J$ | | −55 to 150 | °C |
| Storage temperature, $T_{stg}$ | | −65 to 150 | |
| Lead temperature, $T_{sol}$, 1,6 mm (1/16 inch) from case for 10 seconds | | 300 | |

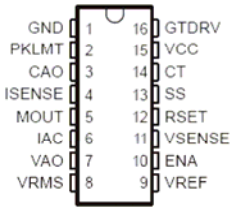
(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal. ENA input is internally clamped to approximately 10 V.

## RECOMMENDED OPERATING CONDITIONS

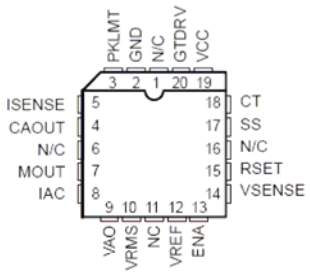
| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | | 10 | 20 | V |
| Operating junction temperature, $T_J$ | UC1854X | | −55 | 125 | °C |
| | UC2854X | | −40 | 85 | |
| | UC3854X | | 0 | 70 | |

## PACKAGE DESCRIPTION

J, N and DW PACKAGES
(TOP VIEW)




Q PACKAGE
(TOP VIEW)




N/C – No connection

## ORDERING INFORMATION

| $T_A$ | UVLO TURN-ON (V) | UVLO TURN-OFF (V) | PART NUMBERS | | | |
|---|---|---|---|---|---|---|
| | | | CDIP–16 (J) | PDIP–16 (N) | SOIC–16 (DW) | PLCC–20 (Q) |
| –55°C to 125°C | 16 | 10 | – | – | – | – |
| | 10.5 | 10 | UC1854BJ | – | – | – |
| –40°C to 85°C | 16 | 10 | UC2854AJ | UC2854AN | UC2854ADW | UC2854AQ |
| | 10.5 | 10 | UC2854BJ | UC2854BN | UC2854BDW | UC2854BQ |
| 0°C to 70°C | 16 | 10 | – | UC3854AN | UC3854ADW | – |
| | 10.5 | 10 | – | UC3854BN | UC3854BDW | – |

(1) The DW and Q packages are available taped and reeled. Add TR suffix to device type (e.g. UC2854ADWTR) to order quantities of 2,000 devices per reel for the DW package and 1,000 devices per reel for the Q package.

## THERMAL RESISTANCE

| RESISTANCES | PACKAGED DEVICES | | | |
|---|---|---|---|---|
| | CDIP–16 (J) | PDIP–16 (N) | SOP–16 (DW) | PLCC–20 (Q) |
| $\theta_{JC}$ (°C/W) | 28(2) | 45 | 27 | 34 |
| $\theta_{JA}$ (°C/W) | 80–120 | 90(3) | 50–130(3) | 43–75(3) |

(2) $\theta_{JC}$ data values stated are derived from MIL-STD-1835B which states "the baseline values shown are worst case (mean +2s) for a 60 × 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14,400 square mils. For device die sizes greater than 14,400 square mils use the following values, dual-in-line, 11°C/W; flat pack and pin grid array, 10°C/W.

(3) $\theta_{JA}$ (junction-to-ambient) applies to devices mounted to five square inch FR4 PC board with one ounce copper where noted. When resitance range is given, lower values are for five square inch aluminum PC board. Test PWB is 0.062 inches thick and typically uses 0.635 mm trace widths for power packages and 1.3 mm trace widths for non-power packages with a 100 × 100 mil probe land are at the end of each trace.

## ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 18 V, $R_T$ = 8.2 kΩ, $C_T$ = 1.5 nF, $V_{PKLMT}$ = 1 V, $V_{VRMS}$ = 1.5 V, $I_{IAC}$ = 100 µA, $I_{ISENSE}$ = 0 V, $V_{CAO}$ = 3.5 V, $V_{VAO}$ = 5 V, $V_{VSENSE}$ = 3 V, −40°C < $T_A$ < 85°C for the UC2854A and UC2854B, and 0°C < $T_A$ <70°C for the UC3854A and UC3854B, and $T_A$ = $T_J$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| OVERALL | | | | | | |
| | Supply current, off | CAO = 0 V, VAO = 0 V, $V_{CC}$ = $V_{UVLO}$−0.3 V | | 250 | 400 | µA |
| | Supply current, on | | | 12 | 18 | mA |
| | $V_{CC}$ turn-on threshold voltage | UCx854A | 15.0 | 16.0 | 17.5 | V |
| | | UCx854B | 8.0 | 10.5 | 11.2 | |
| | $V_{CC}$ turn-off threshold voltage | | 9 | 10 | 12 | |
| | $V_{CC}$ clamp | $I_{VCC}$ = $I_{VCC(on)}$ + 5 mA | 18 | 20 | 22 | |
| VOLTAGE AMPLIFIER | | | | | | |
| | Input voltage | | 2.9 | 3.0 | 3.1 | V |
| | $V_{SENSE}$ bias current | | −500 | −25 | 500 | nA |
| | Open loop gain | 2 V ≤ $V_{OUT}$ ≤ 5 V | 70 | 100 | | dB |
| $V_{OH}$ | High-level output voltage | $I_{LOAD}$ = −500 µA | | 6 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{LOAD}$ = 500 µA | | 0.3 | 0.5 | V |
| $I_{SC}$ | Output short-circuit current | $V_{OUT}$ = 0 V | | 1.5 | 4.5 | mA |
| | Gain bandwidth product(1) | $f_{IN}$ = 100 kHz, 10 $mV_{P-P}$ | | 1 | | MHz |
| CURRENT AMPLIFIER | | | | | | |
| | Input offset voltage | $V_{CM}$ = 0 V, $T_A$ = 25°C | −4 | | 0 | mV |
| | | $V_{CM}$ = 0 V, overtemperature | −5.5 | | 0 | |
| | Input bias current, $I_{SENSE}$ | $V_{CM}$ = 0 V | −500 | | 500 | nA |
| | Open loop gain | 2 V ≤ $V_{OUT}$ ≤ 6 V | 80 | 110 | | dB |
| $V_{OH}$ | High-level output voltage | $I_{LOAD}$ = −500 µA | | 8 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{LOAD}$ = 500 µA | | 0.3 | 0.5 | |
| $I_{SC}$ | Output short-circuit current | $V_{OUT}$ = 0 V | | 1.5 | 4.5 | mA |
| CMRR | Common mode rejection range | | −0.3 | | 5.0 | V |
| | Gain bandwidth product(1) | $f_{IN}$ = 100 kHz, 10 $mV_{P-P}$ | 3 | 5 | | MHz |
| REFERENCE | | | | | | |
| | Output voltage | $I_{REF}$ = 0 mA, $T_A$ = 25°C | 7.4 | 7.5 | 7.6 | V |
| | | $I_{REF}$ = 0 mA | 7.35 | 7.50 | 7.65 | |
| | Load regulation | 1 mA ≤ $I_{REF}$ ≤ 10 mA | 0 | 8 | 20 | mV |
| | Line regulation | 12 V ≤ $V_{CC}$ ≤ 18 V | 0 | 14 | 25 | |
| $I_{SC}$ | Short circuit current | $V_{REF}$ = 0 V | 25 | 35 | 60 | mA |

(1) Ensured by design. Not production tested.

(2) Gain constant, $(K) = \dfrac{I_{IAC} \times (V_{VAO} - 1.5\ V)}{\left[(V_{VRMS})^2 \times I_{MOUT}\right]}$

## ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 18 V, $R_T$ = 8.2 kΩ, $C_T$ = 1.5 nF, $V_{PKLMT}$ = 1 V, $V_{VRMS}$ = 1.5 V, $I_{IAC}$ = 100 µA, $I_{ISENSE}$ = 0 V, $V_{CAO}$ = 3.5 V, $V_{VAO}$ = 5 V, $V_{VSENSE}$ = 3 V, −40°C < $T_A$ < 85°C for the UC2854A and UC2854B, and 0°C < $T_A$ <70°C for the UC3854A and UC3854B, and $T_A$ = $T_J$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | | |
| | Initial accuracy | $T_A$ = 25°C | 85 | 100 | 115 | kHz |
| | Voltage stability | 12 V ≤ $V_{CC}$ ≤ 18 V | | 1% | | |
| | Total variation | Line, temperature | 80 | | 120 | kHz |
| | Ramp amplitude (peak-to-peak) | | 4.9 | | 5.9 | V |
| | Ramp valley voltage | | 0.8 | | 1.3 | |
| **ENABLE/SOFT-START/CURRENT LIMIT** | | | | | | |
| | Enable threshold voltage | | 2.35 | 2.55 | 2.80 | V |
| | Enable hysteresis | $V_{FAULT}$ = 2.5 V | | 500 | 600 | mV |
| | Enable input bias current | $V_{ENA}$ = 0 V | | −2 | −5 | µA |
| | Propagation delay to disable time(1) | Enable overdrive = 100 mV | | 300 | | ns |
| | Soft-start charge current | $V_{SS}$ = 2.5 V | 10 | 14 | 24 | |
| | Peak limit offset voltage | | −15 | | 15 | mV |
| | Peak limit input current | $V_{PKLMT}$ = −0.1 V | −200 | −100 | | µA |
| | Peak limit propagation delay time(1) | | | 150 | | ns |
| **MULTIPLIER** | | | | | | |
| | Output current, $I_{AC}$ limited | $I_{AC}$ = 100 µA, $V_{RMS}$ = 1 V, $R_{SET}$ = 10 kΩ | −220 | −200 | −170 | µA |
| | Output current, zero | $I_{AC}$ = 0 µA, $R_{SET}$ = 10 kΩ | −2.0 | −0.2 | 2.0 | |
| | Output current, power limited | $V_{RMS}$ = 1.5 V, Va = 6 V | −230 | −200 | −170 | |
| | Output current | $V_{RMS}$ = 1.5 V, Va = 2 V | | −22 | | µA |
| | | $V_{RMS}$ = 1.5 V, Va = 5 V | | −156 | | µA |
| | | $V_{RMS}$ = 5 V, Va = 2 V | | −2 | | |
| | | $V_{RMS}$ = 5 V, Va = 5 V | | −14 | | |
| | Gain constant(2) | $V_{RMS}$ = 1.5 V, Va = 6V, $T_A$ = 25°C | −1.1 | −1.0 | −0.9 | A/A |
| **GATE DRIVER** | | | | | | |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = −200 mA, $V_{CC}$ = 15 V | 12.0 | 12.8 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 200 mA | | 1.0 | 2.2 | |
| | | $I_{OUT}$ = 10 mA | | 300 | 500 | mV |
| | Low-level UVLO voltage | $I_{OUT}$ = 50 mA, $V_{CC}$ = 0 V | | 0.9 | 1.5 | V |
| | Output rise time(1) | $C_{LOAD}$ = 1 nF | | 35 | | ns |
| | Output fall time(1) | $C_{LOAD}$ = 1 nF | | 35 | | |
| | Output peak current(1) | $C_{LOAD}$ = 10 nF | | 1.0 | | A |

(1) Ensured by design. Not production tested.

(2) Gain constant. $(K) = \dfrac{I_{IAC} \times \left(V_{VAO} - 1.5\ V\right)}{\left[\left(V_{VRMS}\right)^2 \times I_{MOUT}\right]}$

## TERMINAL FUNCTIONS

| NAME | TERMINAL PACKAGES J/N/DW | TERMINAL PACKAGES Q/L | I/O | DESCRIPTION |
|---|---|---|---|---|
| CAO | 3 | 4 | O | Output of the wide bandwidth current amplifier and one of the inputs to the PWM duty-cycle comparator. The output signal generated by this amplifier commands the PWM to force the correct input current. The output can swing from 0.1 V to 7.5 V. |
| CT | 14 | 18 | I | Capacitor from CT to GND sets the PWM oscillator frequency |
| ENA | 10 | 13 | I | A nominal voltage above 2.65 V on this pin allows the device to begin operating. Once operating, the device shuts off if this pin goes below 2.15 V nominal. |
| GND | 1 | 2 | – | All bypass and timing capacitors connected to GND should have leads as short and direct as possible. All voltages are measured with respect GND. |
| GTDRV | 16 | 20 | O | Output of the PWM is a 1.5-A peak totem-pole MOSFET gate driver on GTDRV. This output is internally clamped to 15 V so that the device can be operated with VCC as high as 35 V. Use a series gate resistor of at least 5 Ω to prevent interaction between the gate impedance and the GTDRV output driver that might cause the GTDRV output to overshoot excessively. Some overshoot of the GTDRV output is always expected when driving a capacitive load. |
| IAC | 6 | 8 | I | Current input to the multiplier, proportional to the instantaneous line voltage. This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (IAC) to MOUT, so this is the only multiplier input that should be used for sensing instantaneous line voltage. The nominal voltage on IAC is 6 V, so in addition to a resistor from $I_{AC}$ to rectified 60 Hz, connect a resistor from IAC to VREF. If the resistor to VREF is one-fourth of the value of the resistor to the rectifier, then the 6-V offset is cancelled, and the line current has minimal cross-over distortion. |
| ISENSE | 4 | 5 | I | Switch current sensing input. This is the inverting input to the current amplifier. This input and the non-inverting input MOUT remain functional down to and below GND. Care should be taken to avoid taking these inputs below −0.5V, because they are protected with diodes to GND. |
| MOUT | 5 | 7 | I/O | Multiplier output and current sense plus. The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at MOUT. The cautions about taking ISENSE below −0.5V also apply to MOUT. As the multiplier output is a current, this is a high-impedance input similar to $I_{SENSE}$, so the current amplifier can be configured as a differential amplifier to reject GND noise. |
| PKLMT | 2 | 3 | I | Peak limit. The threshold for PKLMT is 0.0 V. Connect this input to the negative voltage on the current sense resistor. Use a resistor to REF to offset the negative current sense signal up to GND. |
| RSET | 12 | 15 | I | Oscillator charging current and multiplier limit set. A resistor from RSET to ground programs oscillator charging current and maximum multiplier output. Multiplier output current does not exceed 3.75V divided by the resistor from RSET to ground. |
| SS | 13 | 17 | I | Soft-start. SS remains at GND as long as the device is disabled or $V_{CC}$ is too low. SS pulls up to over 8 V by an internal 14-mA current source when both $V_{CC}$ becomes valid and the device is enabled. SS acts as the reference input to the voltage amplifier if SS is below VREF. With a large capacitor from SS to GND, the reference to the voltage regulating amplifier rises slowly, and increase the PWM duty cycle slowly. In the event of a disable command or a supply dropout, SS will quickly discharge to ground and disable the PWM. |
| VAO | 7 | 9 | I | Voltage amplifier output |
| VCC | 15 | 19 | I | Positive supply rail |
| VREF | 9 | 12 | O | Used to set the peak limit point and as an internal reference for various device functions. This voltage must be present for the device to operate. |
| VRMS | 8 | 10 | I | One of the inputs into the multiplier. This pin provides the input RMS voltage to the multiplier circuitry. |
| VSENSE | 11 | 14 | I | This pin provides the feedback from the output. This input goes into the voltage error amplifier and the output of the error amplifier is another of the inputs into the multiplier circuit. |

## FUNCTIONAL DESCRIPTION

The UC3854A and UC3854B family of products are designed as pin compatible upgrades to the industry standard UC3854 active power factor correction circuits. The circuit enhancements allow the user to eliminate in most cases several external components currently required to successfully apply the UC3854. In addition, linearity improvements to the multiply, square and divide circuitry optimizes overall system performance. Detailed descriptions of the circuit enhancements are provided below. For in-depth design applications reference data refer to the application notes, *UC3854 Controlled Power Factor Correction Circuit Design* (SLUA144) and *UC3854A and UC3854B Advanced Power Factor Correction Control ICs* (SLUA177).

### Multiply/Square and Divide

The UC3854A/B multiplier design maintains the same gain constant (K=−1) as the UC3854. The relationship between the inputs and output current is given as:

$$I_{MOUT} = I_{iAC} \times \frac{\left(V_{VAO} - 1.5\ V\right)}{K \times \left(V_{VRMS}\right)^2} \quad (1)$$

This is nearly the same as the UC3854, but circuit differences have improved the performance and application.

The first difference is with the IAC input. The UC3854A/B regulated this pin voltage to the nominal 500 mV over the full operating temperature range, rather than the 6.0 V used on the UC3854. The low offset voltage eliminates the need for a line zero crossing compensating resistor to VREF from IAC that UC3854 designs require. The maximum current at high line into IAC should be limited to 250 µA for best performance.

Therefore, if $V_{VAC(max)}$ = 270 V,

$$R_{IAC} = \frac{270 \times 1.414}{250\ \mu A} = 1.53\ M\Omega \quad (2)$$

The $V_{RMS}$ pin linear operating range is improved with the UC3854A/B as well. The input range for VRMS extends from 0 V to 5.5 V. Since the UC3854A squaring circuit employs an analog multiplier, rather than a linear approximation, accuracy is improved, and discontinuities are eliminated. The external divider network connected to VRMS should produce 1.5 V at low line (85 VAC). This puts 4.77 V on VRMS at high line (27 VAC) which is well within its operating range.

The voltage amplifier output forms the third input to the multiplier and is internally clamped to 6.0 V. This eliminated an external zener clamp often used in UC3854 designs. The offset voltage at this input to the multiplier has been raised on the UC3854A/B to 1.5 V.

The multiplier output pin, which is also common to the current amplifier non-inverting input, has a −0.3 V to 5.0 V output range, compared to the −0.3 V to 2.5 V range of the UC3854. This improvement allows the UC3854A/B to be used in applications where the current sense signal amplitude is very large.

### Voltage Amplifier

The UC3854A/B voltage amplifier design is essentially similar to the UC3854 with two exceptions. The first is with the internal connection. The lower voltage reduces the amount of charge on the compensation capacitors, which provides improved recovery form large signal events, such as line dropouts, or power interruption. It also minimizes the dc current flowing through the feedback. The output of the voltage amplifier is also changes. In addition to a 6.0 V temperature compensated clamp, the output short circuit current has been lowered to 2 mA typical, and an active pull down has replaced the passive pull down of the UC3854.

### Current Amplifier

The current amplifier for an average current PFC controller needs a low offset voltage in order to minimize AC line current distortion. With this in mind, the UC3854A/B current amplifier has improved the input offset voltage from ±4 mV to 0 V to ±3 mV. The negative offset of the UC3854A/B guarantees that the PWM circuit will not drive the MOSFET is the current command is zero (both current amplifier inputs zero.) Previous designs required an external offset cancellation network to implement this key feature. The bandwidth of the current amplifier has been improved as well to 5 MHz typical. While this is not generally an issue at 50 Hz or 60 Hz inputs, it is essential for 400 Hz input avionics applications

### Miscellaneous

Several other important enhancements have been implemented in the UC3854A/B. A $V_{CC}$ supply voltage clamp at 20 V allows the controller to be current fed if desired. The lower startup supply current (250 mA typical), substantially reduces the power requirements of an offline startup resistor. The 10.5 V/10 V UVLO option (UC3854B) enables the controller to be powered off of an auxiliary 12 V supply.

The VREF GOOD comparator guarantees that the MOSFET driver output remains low if the supply of the 7.5 V reference are not yet up. This improvement eliminates the need for external Schottky diodes on the PKLMT and Mult Out pins that some UC3854 designs require. The propagation delay of the disable feature has been improved to 300 ns typical. This delay was proportional to the size of the VREF capacitor on the UC3854, and is typically several orders of magnitude slower.

## TYPICAL CHARACTERISTICS

GATE DRIVE TIMING
vs
LOAD CAPACITANCE

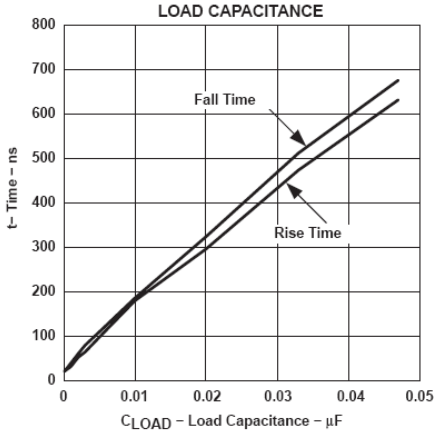



Figure 1

GATE DRIVE MAXIMUM DUTY CYCLE
vs
OSCILLATOR CHARGING RESISTANCE

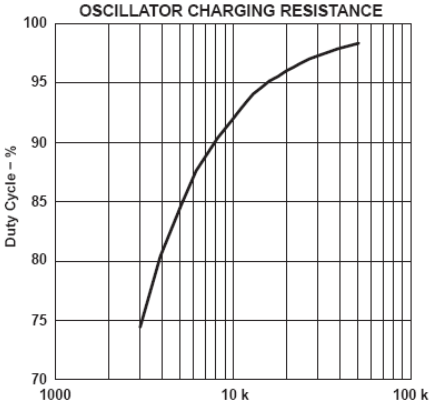



Figure 2

MULTIPLIER GAIN CONSTANT
vs
SUPPLY CURRENT

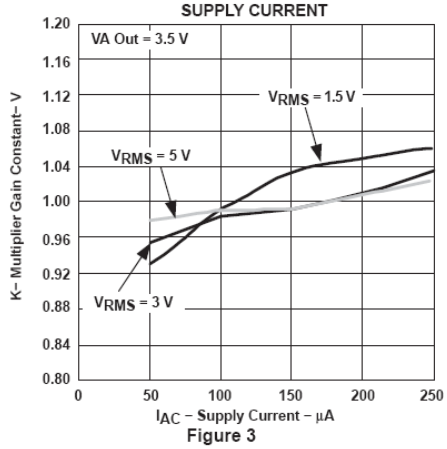



Figure 3

MULTIPLIER GAIN CONSTANT
vs
SUPPLY CURRENT

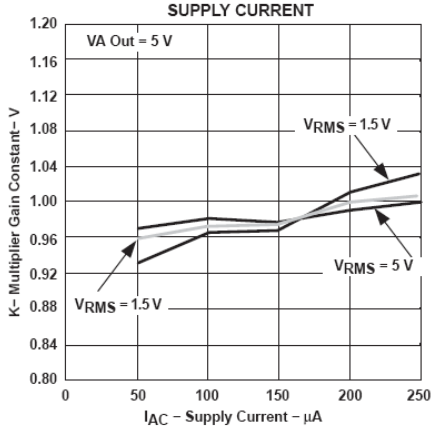



Figure 4

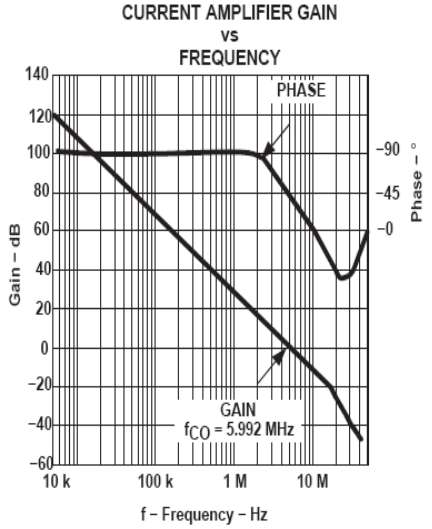



Figure 5

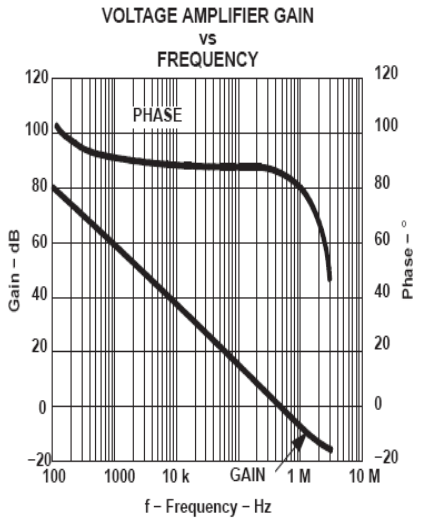



Figure 6

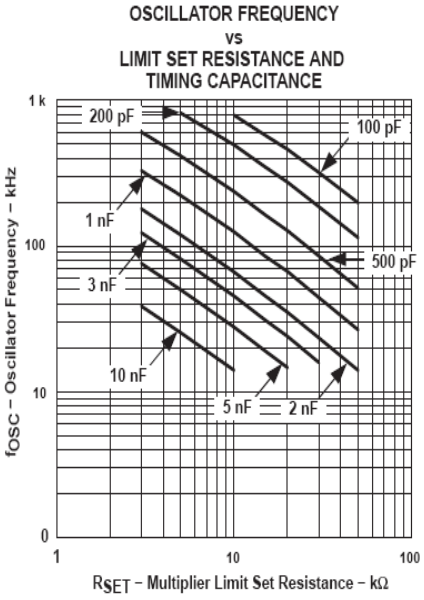
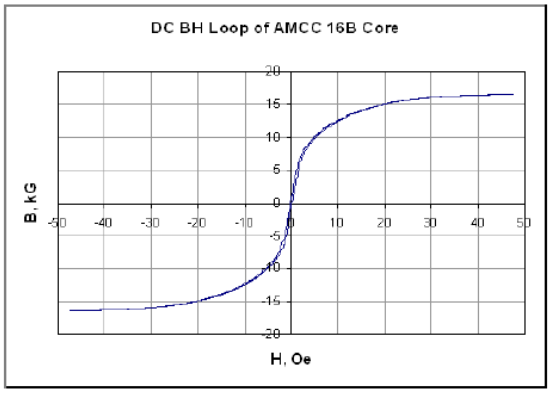



Figure 7

Typical DC Hysteresis Loop
Metglas® Alloy 2605SA1




***POWERLITE® C-Cores*** are manufactured with iron based Metglas® amorphous Alloy 2605SA1. Their unique combination of low loss and high saturation flux density provide for size reduction and improvements in energy efficiency making them an ideal solution for automotive inductor applications

## Benefits

Manufactured in a variety of ultra-efficient core configurations, POWERLITE C-Cores provide significant cost, design and performance benefits over ordinary Si-Fe, ferrite and MPP cores such as:

- High Saturation Flux Density (1.56 T)
- Low Profile – enables weight and volume reductions of up to 50%
- Low Temperature Rise – enabling smaller compact designs
- Low Loss – resulting from micro-thin Metglas ribbon (25 µm)

**Physical Properties METGLAS Alloy 2605SA1**

| | |
|---|---|
| Ribbon Thickness (µm) | .25 |
| Density (g/cm3) | 7.18 |
| Thermal Expansion (ppm/°C) | 7.6 |
| Crystallization Temperature (°C) | 505 |
| Curie Temperature (°C) | 392 |
| Continuous Service Temperature (°C) | 150 |
| Tensile Strength (MN/m2) | 1k-1.7k |
| Elastic Modulus (GN/m2) | 100-110 |
| Vicker's Hardness (50g load) | 860 |

**Magnetic Properties METGLAS Powerlite Cores**

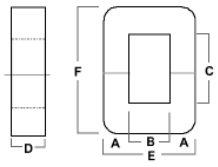
| | |
|---|---|
| Saturation Flux Density (Tesla) | 1.56 |
| Permeability (depending on gap size) | VARIABLE |
| Saturation Magnetostriction (ppm) | 27 |
| Electrical Resistivity (µΩcm) | 137 |

e-mail: metglas@metglas.com
1-800-581-7654

## Standard Core Specifications

**AMCC1000**

*Amorphous Metal*
*C-Core*
*Part Designation*




| | Core Dimensions | | | | | | | | | | Performance Parameters | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | a(mm) | ± | b(mm) | c(mm) | d(mm) | ± | e(mm) | ± | f(mm) | ± | (lm) cm | ac ($cm^2$) | Wa ($cm^2$) | Ap ($cm^4$) | (gms) |
| **AMCC 4** | 9.00 | 0.50 | 10.50 | 32.75 | 15.25 | 0.25 | 28.50 | 0.50 | 51.00 | 1.00 | 12.70 | 1.11 | 3.44 | 3.82 | 102 |
| **AMCC 6.3** | 10.0 | 0.50 | 11.00 | 33.0 | 20.00 | 0.50 | 31.00 | 1.00 | 53.00 | 2.00 | 13.10 | 1.60 | 3.60 | 5.80 | 150 |
| **AMCC 10** | 11.0 | 0.80 | 13.00 | 40.0 | 20.00 | 0.50 | 35.00 | 1.00 | 62.00 | 2.00 | 15.40 | 1.80 | 5.20 | 9.40 | 200 |
| **AMCC 8** | 11.0 | 0.80 | 13.00 | 30.0 | 20.00 | 0.50 | 35.00 | 1.00 | 52.00 | 2.00 | 13.20 | 1.80 | 3.90 | 7.00 | 170 |
| **AMCC 16B** | 11.0 | 0.80 | 13.00 | 50.0 | 25.00 | 0.50 | 35.00 | 1.00 | 72.00 | 2.00 | 16.90 | 2.30 | 6.50 | 15.0 | 280 |
| **AMCC 16A** | 11.0 | 0.80 | 13.00 | 40.0 | 25.00 | 0.50 | 35.00 | 1.00 | 62.00 | 2.00 | 15.10 | 2.30 | 5.20 | 12.0 | 250 |
| **AMCC 20** | 11.0 | 0.80 | 13.00 | 50.0 | 30.00 | 0.50 | 35.00 | 1.00 | 72.00 | 2.00 | 17.50 | 2.70 | 6.50 | 17.6 | 340 |
| **AMCC 40** | 13.0 | 0.80 | 15.00 | 56.0 | 35.00 | 0.50 | 41.00 | 1.00 | 82.00 | 2.00 | 19.90 | 3.70 | 8.40 | 31.1 | 530 |
| **AMCC 25** | 13.0 | 0.80 | 15.00 | 56.0 | 25.00 | 0.50 | 41.00 | 1.00 | 82.00 | 2.00 | 19.60 | 2.70 | 8.40 | 22.7 | 380 |
| **AMCC 32** | 13.0 | 0.80 | 15.00 | 56.0 | 30.00 | 0.50 | 41.00 | 1.00 | 82.00 | 2.00 | 20.00 | 3.20 | 8.40 | 26.9 | 460 |
| **AMCC 50** | 16.0 | 1.00 | 20.00 | 70.0 | 25.00 | 0.50 | 52.00 | 1.00 | 102.0 | 3.00 | 24.90 | 3.30 | 14.0 | 46.2 | 590 |
| **AMCC 63** | 16.0 | 1.00 | 20.00 | 70.0 | 30.00 | 0.50 | 52.00 | 1.00 | 102.0 | 3.00 | 25.30 | 3.90 | 14.0 | 54.6 | 710 |
| **AMCC 80** | 16.0 | 1.00 | 20.00 | 70.0 | 40.00 | 1.00 | 52.00 | 1.00 | 102.0 | 3.00 | 25.40 | 5.20 | 14.0 | 72.8 | 950 |
| **AMCC 100** | 16.0 | 1.00 | 20.00 | 70.0 | 45.00 | 1.00 | 52.00 | 1.00 | 102.0 | 3.00 | 25.00 | 5.90 | 14.0 | 82.6 | 1,060 |
| **AMCC 160** | 19.0 | 1.00 | 25.00 | 83.0 | 40.00 | 1.00 | 63.00 | 1.00 | 121.0 | 3.00 | 28.50 | 6.50 | 20.8 | 135.2 | 1,330 |
| **AMCC 125** | 19.0 | 1.00 | 25.00 | 83.0 | 35.00 | 1.00 | 63.00 | 1.00 | 121.0 | 3.00 | 30.20 | 5.40 | 20.8 | 112.1 | 1,170 |
| **AMCC 250** | 19.0 | 1.00 | 25.00 | 90.0 | 60.00 | 1.00 | 63.00 | 1.00 | 128.0 | 3.00 | 31.40 | 9.30 | 22.5 | 209.3 | 2,100 |
| **AMCC 200** | 19.0 | 1.00 | 25.00 | 83.0 | 50.00 | 1.00 | 63.00 | 1.00 | 121.0 | 3.00 | 29.80 | 7.80 | 20.8 | 162.2 | 1,670 |
| **AMCC 168S** | 20.4 | 0.50 | 30.20 | 155.2 | 20.00 | 0.50 | 71.00 | 0.75 | 196.0 | 2.00 | 45.40 | 3.35 | 45.7 | 153.0 | 1,090 |
| **AMCC 320** | 22.0 | 1.00 | 35.00 | 85.0 | 50.00 | 1.00 | 79.00 | 1.00 | 129.0 | 4.00 | 32.50 | 9.00 | 29.8 | 267.8 | 2,170 |
| **AMCC 400** | 22.0 | 1.00 | 35.00 | 85.0 | 65.00 | 1.00 | 79.00 | 1.00 | 129.0 | 4.00 | 33.60 | 11.7 | 29.8 | 348.1 | 2,820 |
| **AMCC 500** | 25.0 | 1.00 | 40.00 | 85.0 | 55.00 | 1.00 | 90.00 | 1.00 | 135.0 | 4.00 | 35.60 | 11.3 | 34.0 | 384.2 | 2,900 |
| **AMCC 630** | 25.0 | 1.00 | 40.00 | 85.0 | 70.00 | 1.00 | 90.00 | 1.00 | 135.0 | 4.00 | 35.60 | 14.3 | 34.0 | 486.2 | 3,670 |
| **AMCC 800A** | 25.0 | 1.00 | 40.00 | 85.0 | 85.00 | 1.50 | 90.00 | 1.00 | 135.0 | 4.00 | 35.60 | 17.4 | 34.0 | 591.6 | 4,450 |
| **AMCC 367S** | 25.8 | 1.00 | 66.00 | 97.8 | 25.00 | 0.70 | 117.6 | 1.50 | 149.4 | 1.50 | 43.78 | 5.29 | 63.8 | 338.0 | 1,662 |
| **AMCC 800B** | 30.0 | 1.00 | 40.00 | 95.0 | 85.00 | 1.50 | 100.0 | 1.00 | 155.0 | 4.00 | 39.30 | 21.0 | 38.0 | 798.0 | 5,930 |
| **AMCC 1000** | 33.0 | 1.00 | 40.00 | 105.0 | 85.00 | 1.50 | 106.0 | 1.00 | 171.0 | 5.00 | 42.70 | 23.0 | 42.0 | 966.0 | 7,060 |

e-mail: metglas@metglas.com 1-800-581-7654

Bulletin PD-20766 rev. B 02/04

International
IOR Rectifier

# 8ETX06
# 8ETX06S
# 8ETX06-1
# 8ETX06FP

## Hyperfast Rectifier

**Features**

- Hyperfast Recovery Time
- Low Forward Voltage Drop
- Low Leakage Current
- 175°C Operating Junction Temperature
- UL E78996 approved

$t_{rr}$ = 15ns typ.
$I_{F(AV)}$ = 8Amp
$V_R$ = 600V

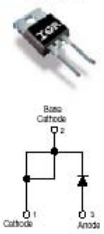
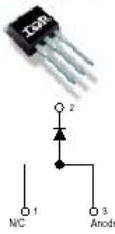
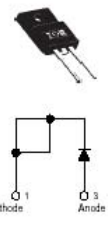
**Description/ Applications**

State of the art Hyperfast recovery rectifiers designed with optimized performance of forward voltage drop, Hyperfast recover time, and soft recovery.
The planar structure and the platinum doped life time control guarantee the best overall performance, ruggedness and reliability characteristics.
These devices are intended for use in PFC Boost stage in the AC-DC section of SMPS, inverters or as freewheeling diodes.
The IR extremely optimized stored charge and low recovery current minimize the switching losses and reduce over dissipation in the switching element and snubbers.

**Absolute Maximum Ratings**

| | Parameters | Max | Units |
|---|---|---|---|
| $V_{RRM}$ | Peak Repetitive Reverse Voltage | 600 | V |
| $I_{F(AV)}$ | Average Rectified Forward Current @ $T_C$ = 143°C<br>@ $T_C$ = 106°C (FULLPACK) | 8 | A |
| $I_{FSM}$ | Non Repetitive Peak Surge Current @ $T_J$ = 25°C | 110 | |
| $I_{FM}$ | Peak Repetitive Forward Current | 18 | |
| $T_J$, $T_{STG}$ | Operating Junction and Storage Temperatures | - 65 to 175 | °C |

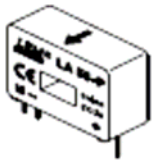
**Case Styles**

| 8ETX06 | 8ETX06S | 8ETX06-1 | 8ETX06FP |
|---|---|---|---|
|  |  |  |  |
|  |  |  |  |
| TO-220AC | D²PAK | TO-262 | TO-220 FULLPACK |

# Current Transducer LA 55-P/SP1

$I_{PN}$ = 50 A

For the electronic measurement of currents : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).



18024

## Electrical data

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $I_{PN}$ | Primary nominal r.m.s. current | | | 50 | | | A |
| $I_P$ | Primary current, measuring range | | | 0 .. ± 100 | | | A |
| $R_M$ | Measuring resistance @ | | $T_A$ = 70°C | | $T_A$ = 85°C | | |
| | | | $R_{M\,min}$ | $R_{M\,max}$ | $R_{M\,min}$ | $R_{M\,max}$ | |
| | with ± 12 V | @ ± 50 $A_{max}$ | 0 | 215 | 0 | 210 | Ω |
| | | @ ± 100 $A_{max}$ | 0 | 35 | 0 | 30 | Ω |
| | with ± 15 V | @ ± 50 $A_{max}$ | 0 | 335 | 30 | 330 | Ω |
| | | @ ± 100 $A_{max}$ | 0 | 95 | 30 | 90 | Ω |
| $I_{SN}$ | Secondary nominal r.m.s. current | | | 25 | | | mA |
| $K_N$ | Conversion ratio | | | 1 : 2000 | | | |
| $V_C$ | Supply voltage (± 5 %) | | | ± 12 .. 15 | | | V |
| $I_C$ | Current consumption | | | 10 (@ ± 15 V) + $I_S$ | | | mA |
| $V_d$ | R.m.s. voltage for AC isolation test, 50 Hz, 1 mn | | | 2.5 | | | kV |

## Accuracy - Dynamic performance data

| | | | | | |
|---|---|---|---|---|---|
| X | Accuracy @ $I_{PN}$, $T_A$ = 25°C | @ ± 15 V (± 5 %) | | ± 0.65 | % |
| | | @ ± 12 .. 15 V (± 5 %) | | ± 0.90 | % |
| $\varepsilon_L$ | Linearity error | | | < 0.15 | % |
| | | | Typ | Max | |
| $I_O$ | Offset current @ $I_P$ = 0, $T_A$ = 25°C | | | ± 0.10 | mA |
| $I_{OM}$ | Residual current [1] @ $I_P$ = 0, after an overload of 3 x $I_{PN}$ | | | ± 0.15 | mA |
| $I_{OT}$ | Thermal drift of $I_O$ | 0°C .. + 70°C | ± 0.05 | ± 0.25 | mA |
| | | - 25°C .. + 85°C | ± 0.05 | ± 0.30 | mA |
| $t_{ra}$ | Reaction time @ 10 % of $I_{PN}$ | | | < 500 | ns |
| $t_r$ | Response time [2] @ 90 % of $I_{PN}$ | | | < 1 | µs |
| di/dt | di/dt accurately followed | | | > 200 | A/µs |
| f | Frequency bandwidth (- 1 dB) | | | DC .. 200 | kHz |

## General data

| | | | | |
|---|---|---|---|---|
| $T_A$ | Ambient operating temperature | | - 25 .. + 85 | °C |
| $T_S$ | Ambient storage temperature | | - 40 .. + 90 | °C |
| $R_S$ | Secondary coil resistance @ | $T_A$ = 70°C | 146 | Ω |
| | | $T_A$ = 85°C | 160 | Ω |
| m | Mass | | 18 | g |
| | Standards | | EN 50178 : 1997 | |

Notes : [1] Result of the coercive field of the magnetic circuit
[2] With a di/dt of 100 A/µs.

### Features

- Closed loop (compensated) current transducer using the Hall effect
- Printed circuit board mounting
- Insulated plastic case recognized according to UL 94-V0.

### Special features

- $I_{PN}$ = 0 .. ± 100 A
- $K_N$ = 1 : 2000.

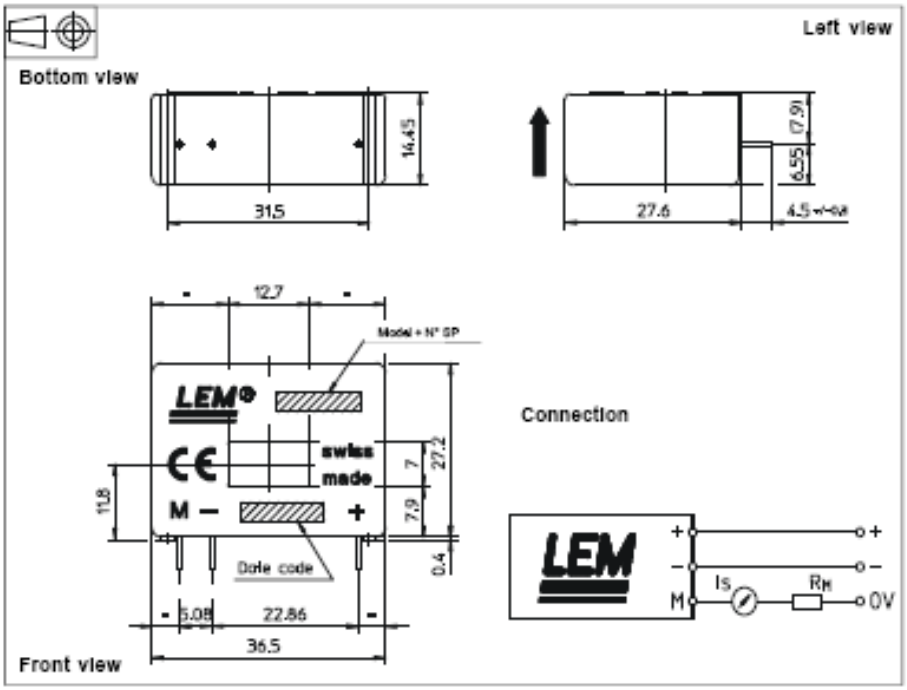
### Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

### Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

## Dimensions LA 55-P/SP1 (in mm. 1 mm = 0.0394 inch)




### Mechanical characteristics

| | |
|---|---|
| • General tolerance | ± 0.2 mm |
| • Primary through-hole | 12.7 x 7 mm |
| • Fastening & connection of secondary | 3 pins<br>0.63 x 0.56 mm |
| Recommended PCB hole | 0.9 mm |

### Remarks

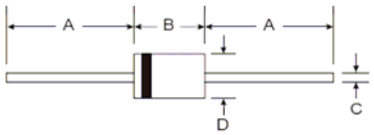
- $I_s$ is positive when $I_p$ flows in the direction of the arrow.
- Temperature of the primary conductor should not exceed 90°C.
- Dynamic performances (di/dt and response time) are best with a single bar completely filling the primary hole.
- In order to achieve the best magnetic coupling, the primary windings have to be wound over the top edge of the device.

# 1N4001/L - 1N4007/L

**1.0A RECTIFIER**

## Features

- Diffused Junction
- High Current Capability and Low Forward Voltage Drop
- Surge Overload Rating to 30A Peak
- Low Reverse Leakage Current
- Plastic Material: UL Flammability Classification Rating 94V-0




| | DO-41 Plastic | | A-405 | |
|---|---|---|---|---|
| **Dim** | **Min** | **Max** | **Min** | **Max** |
| A | 25.40 | — | 25.40 | — |
| B | 4.06 | 5.21 | 4.10 | 5.20 |
| C | 0.71 | 0.864 | 0.53 | 0.64 |
| D | 2.00 | 2.72 | 2.00 | 2.70 |
| **All Dimensions in mm** | | | | |

"L" Suffix Designates A-405 Package
No Suffix Designates DO-41 Package

## Mechanical Data

- Case: Molded Plastic
- Terminals: Plated Leads Solderable per MIL-STD-202, Method 208
- Polarity: Cathode Band
- Weight: DO-41 0.30 grams (approx)
  A-405 0.20 grams (approx)
- Mounting Position: Any
- Marking: Type Number

## Maximum Ratings and Electrical Characteristics

@ $T_A$ = 25°C unless otherwise specified

Single phase, half wave, 60Hz, resistive or inductive load.
For capacitive load, derate current by 20%.

| Characteristic | Symbol | 1N 4001/L | 1N 4002/L | 1N 4003/L | 1N 4004/L | 1N 4005/L | 1N 4006/L | 1N 4007/L | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Peak Repetitive Reverse Voltage<br>Working Peak Reverse Voltage<br>DC Blocking Voltage | $V_{RRM}$<br>$V_{RWM}$<br>$V_R$ | 50 | 100 | 200 | 400 | 600 | 800 | 1000 | V |
| RMS Reverse Voltage | $V_{R(RMS)}$ | 35 | 70 | 140 | 280 | 420 | 560 | 700 | V |
| Average Rectified Output Current (Note 1) @ $T_A$ = 75°C | $I_O$ | 1.0 | | | | | | | A |
| Non-Repetitive Peak Forward Surge Current 8.3ms single half sine-wave superimposed on rated load (JEDEC Method) | $I_{FSM}$ | 30 | | | | | | | A |
| Forward Voltage @ $I_F$ = 1.0A | $V_{FM}$ | 1.0 | | | | | | | V |
| Peak Reverse Current @ $T_A$ = 25°C<br>at Rated DC Blocking Voltage @ $T_A$ = 100°C | $I_{RM}$ | 5.0<br>50 | | | | | | | μA |
| Typical Junction Capacitance (Note 2) | $C_j$ | 15 | | | | 8 | | | pF |
| Typical Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | 100 | | | | | | | K/W |
| Maximum DC Blocking Voltage Temperature | $T_A$ | +150 | | | | | | | °C |
| Operating and Storage Temperature Range (Note 3) | $T_j$, $T_{STG}$ | -65 to +175 | | | | | | | °C |

Notes: 1. Leads maintained at ambient temperature at a distance of 9.5mm from the case.
2. Measured at 1. MHz and applied reverse voltage of 4.0V DC.
3. JEDEC Value

# 7. SILICON BRIDGE RECTIFIERS

T-23-01

The plastic material used in the bridges of 0.5 to 8 ampere rating carries U/L recognition 94V-O.

For Capacitance Load Derate Current by 20%.

Individual Technical Data Sheets Giving Rating and Characteristic Curves are Available

OPERATIONAL TEMPERATURE RANGE −55° to 125°C
STORAGE TEMPERATURE RANGE −55° to 150°C

| Type | PRV | Max Avg Rect Current @ Half-Wave Res Load 60Hz | | Max Fwd Peak Surge Current 1 ~ 60Hz Superimposed | Max Reverse Current @ PRV Voltage @ 25°C $T_A$ | Max Fwd Voltage @ 25°C $T_A$ | | Avalanche Breakdown Voltage | | Max Rev Recovery Time |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $I_O$ @ | $T_A$ | $I_{FM}$ (Surge) | $I_R$ | $I_{FM}$ | $V_{FM}$ | MIN | MAX | trr |
| | $V_{PK}$ | $A_{AV}$ | °C | $A_{PK}$ | μAdc | $A_{PK}$ | $V_{PK}$ | $V_{PK}$ | | ns |
| **7-1 1 TO 2 AMPERE/WB OUTLINE** | | | | | | | | | | |
| WB100 | 50 | 1.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB101 | 100 | 1.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB102 | 200 | 1.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB104 | 400 | 1.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB106 | 600 | 1.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB108 | 800 | 1.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB110 | 1000 | 1.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB150 | 50 | 1.5 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB151 | 100 | 1.5 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB152 | 200 | 1.5 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB154 | 400 | 1.5 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB156 | 600 | 1.5 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB158 | 800 | 1.5 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB1510 | 1000 | 1.5 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB200 | 50 | 2.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB201 | 100 | 2.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB202 | 200 | 2.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB204 | 400 | 2.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB206 | 600 | 2.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB208 | 800 | 2.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| WB210 | 1000 | 2.0 | 25 | 50 | 10 | 1.0 | 1.0 | | | |
| **7-2 1 TO 2 AMPERE/SB200 OUTLINE** | | | | | | | | | | |
| 3N246 | 50 | 1.0 | 75 | 30 | 10 | 3.14 | 1.3 | | | |
| 3N247 | 100 | 1.0 | 75 | 30 | 10 | 3.14 | 1.3 | | | |
| 3N248 | 200 | 1.0 | 75 | 30 | 10 | 3.14 | 1.3 | | | |
| 3N249 | 400 | 1.0 | 75 | 30 | 10 | 3.14 | 1.3 | | | |
| 3N250 | 600 | 1.0 | 75 | 30 | 10 | 3.14 | 1.3 | | | |
| 3N251 | 800 | 1.0 | 75 | 30 | 10 | 3.14 | 1.3 | | | |
| 3N252 | 1000 | 1.0 | 75 | 30 | 10 | 3.14 | 1.3 | | | |
| 3N253 | 50 | 2.0 | 55 | 60 | 10 | 3.14 | 1.1 | | | |
| 3N254 | 100 | 2.0 | 55 | 60 | 10 | 3.14 | 1.1 | | | |
| 3N255 | 200 | 2.0 | 55 | 60 | 10 | 3.14 | 1.1 | | | |
| 3N256 | 400 | 2.0 | 55 | 60 | 10 | 3.14 | 1.1 | | | |
| 3N257 | 600 | 2.0 | 55 | 60 | 10 | 3.14 | 1.1 | | | |
| 3N258 | 800 | 2.0 | 55 | 60 | 10 | 3.14 | 1.1 | | | |
| 3N259 | 1000 | 2.0 | 55 | 60 | 10 | 3.14 | 1.1 | | | |
| SB200 | 50 | 2.0 | 50 | 60 | 10 | 1.0 | 1.0 | | | |
| SB201 | 100 | 2.0 | 50 | 60 | 10 | 1.0 | 1.0 | | | |
| SB202 | 200 | 2.0 | 50 | 60 | 10 | 1.0 | 1.0 | | | |
| SB204 | 400 | 2.0 | 50 | 60 | 10 | 1.0 | 1.0 | | | |
| SB206 | 600 | 2.0 | 50 | 60 | 10 | 1.0 | 1.0 | | | |
| SB208 | 800 | 2.0 | 50 | 60 | 10 | 1.0 | 1.0 | | | |
| SB210 | 1000 | 2.0 | 50 | 60 | 10 | 1.0 | 1.0 | | | |
| **7-3 4 AMPERE/SB400 OUTLINE** | | | | | | | | | | |
| SB400 | 50 | 4 | 50 | 200 | 10 | 3.0 | 1.2 | | | |
| SB401 | 100 | 4 | 50 | 200 | 10 | 3.0 | 1.2 | | | |
| SB402 | 200 | 4 | 50 | 200 | 10 | 3.0 | 1.2 | | | |
| SB404 | 400 | 4 | 50 | 200 | 10 | 3.0 | 1.2 | | | |
| SB406 | 600 | 4 | 50 | 200 | 10 | 3.0 | 1.2 | | | |
| SB408 | 800 | 4 | 50 | 200 | 10 | 3.0 | 1.2 | | | |
| SB410 | 1000 | 4 | 50 | 200 | 10 | 3.0 | 1.2 | | | |

FAIRCHILD
SEMICONDUCTOR®

May 2006

# LM78XX/LM78XXA
# 3-Terminal 1A Positive Voltage Regulator

## Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

## General Description

The LM78XX series of three terminal positive regulators are available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

## Ordering Information

| Product Number | Output Voltage Tolerance | Package | Operating Temperature |
|---|---|---|---|
| LM7805CT | ±4% | TO-220 | -40°C to +125°C |
| LM7806CT | | | |
| LM7808CT | | | |
| LM7809CT | | | |
| LM7810CT | | | |
| LM7812CT | | | |
| LM7815CT | | | |
| LM7818CT | | | |
| LM7824CT | | | |
| LM7805ACT | ±2% | | 0°C to +125°C |
| LM7806ACT | | | |
| LM7808ACT | | | |
| LM7809ACT | | | |
| LM7810ACT | | | |
| LM7812ACT | | | |
| LM7815ACT | | | |
| LM7818ACT | | | |
| LM7824ACT | | | |

National Semiconductor

September 2001

# LM79XX Series
# 3-Terminal Negative Regulators

## General Description

The LM79XX series of 3-terminal regulators is available with fixed output voltages of −5V, −12V, and −15V. These devices need only one external component—a compensation capacitor at the output. The LM79XX series is packaged in the TO-220 power package and is capable of supplying 1.5A of output current.

These regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the LM79XX series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

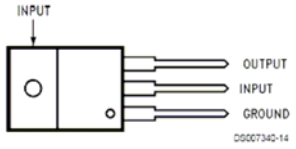
For applications requiring other voltages, see LM137 datasheet.

## Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5A output current
- 4% tolerance on preset output voltage

## Connection Diagrams

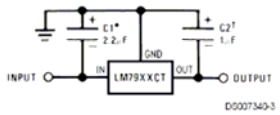
TO-220 Package




Front View
Order Number LM7905CT, LM7912CT or LM7915CT
See NS Package Number TO3B

## Typical Applications

Fixed Regulator




*Required if regulator is separated from filter capacitor by more than 3". For value given, capacitor must be solid tantalum. 25µF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25µF aluminum electrolytic may be substituted. Values given may be increased without limit.

For output capacitance in excess of 100µF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

FAIRCHILD SEMICONDUCTOR®

# RURG5060

**Data Sheet** **January 2002**

## 50A, 600V Ultrafast Diode

The RURG5060 is an ultrafast diode with soft recovery characteristics ($t_{rr}$ < 65ns). It has low forward voltage drop and is of silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of switching power supplies and other power switching applications. Its low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits, thus reducing power loss in the switching transistors.

Formerly developmental type TA09909.

## Ordering Information

| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| RURG5060 | TO-247 | RURG5060 |

NOTE: When ordering, use the entire part number.

## Symbol


## Features

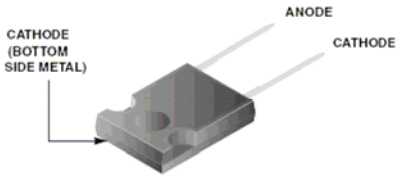
- Ultrafast with Soft Recovery . . . . . <65ns
- Operating Temperature . . . . . 175°C
- Reverse Voltage . . . . . 600V
- Avalanche Energy Rated
- Planar Construction

## Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

## Packaging

JEDEC STYLE 2 LEAD TO-247




## Absolute Maximum Ratings $T_C$ = 25°C, Unless Otherwise Specified

| | | RURG5060 | UNITS |
|---|---|---|---|
| Peak Repetitive Reverse Voltage | $V_{RRM}$ | 600 | V |
| Working Peak Reverse Voltage | $V_{RWM}$ | 600 | V |
| DC Blocking Voltage | $V_R$ | 600 | V |
| Average Rectified Forward Current ($T_C$ = 102°C) | $I_{F(AV)}$ | 50 | A |
| Repetitive Peak Surge Current (Square Wave, 20kHz) | $I_{FRM}$ | 100 | A |
| Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz) | $I_{FSM}$ | 500 | A |
| Maximum Power Dissipation | $P_D$ | 150 | W |
| Avalanche Energy (See Figures 7 and 8) | $E_{AVL}$ | 40 | mJ |
| Operating and Storage Temperature | $T_{STG}$, $T_J$ | -65 to 175 | °C |

**Electrical Specifications** $T_C = 25^oC$, Unless Otherwise Specified

| SYMBOL | TEST CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $V_F$ | $I_F = 50A$ | - | - | 1.6 | V |
| | $I_F = 50A$, $T_C = 150^oC$ | - | - | 1.4 | V |
| $I_R$ | $V_R = 600V$ | - | - | 250 | µA |
| | $V_R = 600V$, $T_C = 150^oC$ | - | - | 1.5 | mA |
| $t_{rr}$ | $I_F = 1A$, $dI_F/dt = 100A/\mu s$ | - | - | 65 | ns |
| | $I_F = 50A$, $dI_F/dt = 100A/\mu s$ | - | - | 75 | ns |
| $t_a$ | $I_F = 50A$, $dI_F/dt = 100A/\mu s$ | - | 30 | - | ns |
| $t_b$ | $I_F = 50A$, $dI_F/dt = 100A/\mu s$ | - | 20 | - | ns |
| $R_{\theta JC}$ | | - | - | 1 | $^oC/W$ |

DEFINITIONS

$V_F$ = Instantaneous forward voltage (pw = 300µs, D = 2%).

$I_R$ = Instantaneous reverse current.

$t_{rr}$ = Reverse recovery time at $dI_F/dt = 100A/\mu s$ (See Figure 6), summation of $t_a + t_b$.

$t_a$ = Time to reach peak reverse current at $dI_F/dt = 100A/\mu s$ (See Figure 6).

$t_b$ = Time from peak $I_{RM}$ to projected zero crossing of $I_{RM}$ based on a straight line from peak $I_{RM}$ through 25% of $I_{RM}$ (See Figure 6).

$R_{\theta JC}$ = Thermal resistance junction to case.

pw = Pulse width.

D = Duty cycle.

## *Typical Performance Curves*

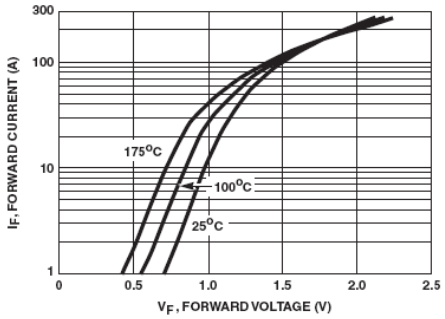



FIGURE 1. FORWARD CURRENT vs FORWARD VOLTAGE

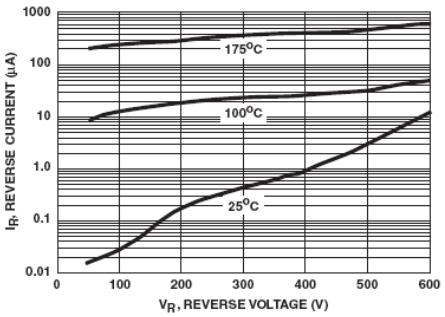


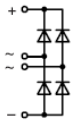

FIGURE 2. REVERSE CURRENT vs REVERSE VOLTAGE

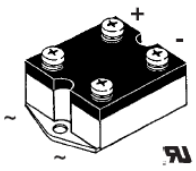
# Single Phase Rectifier Bridge

$I_{dAVM}$ = 35 A
$V_{RRM}$ = 1200-1800 V

| $V_{RSM}$ V | $V_{RRM}$ V | Type |
|---|---|---|
| 800 | 800 | VBO 30-08NO7 |
| 1200 | 1200 | VBO 30-12NO7 |
| 1400 | 1400 | VBO 30-14NO7 |
| 1600 | 1600 | VBO 30-16NO7 |
| 1800 | 1800 | VBO 30-18NO7* |

* delivery time on request





| Symbol | Conditions | | Maximum Ratings | |
|---|---|---|---|---|
| $I_{dAVM}$ | $T_C$ = 85°C, module | | 35 | A |
| $I_{FSM}$ | $T_{VJ}$ = 45°C; | t = 10 ms (50 Hz), sine | 400 | A |
| | $V_R$ = 0 | t = 8.3 ms (60 Hz), sine | 440 | A |
| | $T_{VJ}$ = $T_{VJM}$ | t = 10 ms (50 Hz), sine | 360 | A |
| | $V_R$ = 0 | t = 8.3 ms (60 Hz), sine | 400 | A |
| $I^2t$ | $T_{VJ}$ = 45°C | t = 10 ms (50 Hz), sine | 800 | $A^2s$ |
| | $V_R$ = 0 | t = 8.3 ms (60 Hz), sine | 810 | $A^2s$ |
| | $T_{VJ}$ = $T_{VJM}$ | t = 10 ms (50 Hz), sine | 650 | $A^2s$ |
| | $V_R$ = 0 | t = 8.3 ms (60 Hz), sine | 670 | $A^2s$ |
| $T_{VJ}$ | | | -40...+150 | °C |
| $T_{VJM}$ | | | 150 | °C |
| $T_{stg}$ | | | -40...+150 | °C |
| $V_{ISOL}$ | 50/60 Hz, RMS | t = 1 min | 2500 | V~ |
| | $I_{ISOL}$ ≤ 1 mA | t = 1 s | 3000 | V~ |
| $M_d$ | Mounting torque (M4) | | 1.5 ±15% | Nm |
| | | | 13 ±15% | lb.in. |
| | Terminal connection torque (M4) | | 1.5 ±15% | Nm |
| | | | 13 ±15% | lb.in. |
| Weight | typ. | | 135 | g |

| Symbol | Conditions | | Characteristic Values | | |
|---|---|---|---|---|---|
| $I_R$ | $V_R$ = $V_{RRM}$; | $T_{VJ}$ = 25°C | ≤ | 0.3 | mA |
| | $V_R$ = $V_{RRM}$; | $T_{VJ}$ = $T_{VJM}$ | ≤ | 5.0 | mA |
| $V_F$ | $I_F$ = 150 A; | $T_{VJ}$ = 25°C | ≤ | 2.2 | V |
| $V_{T0}$ | For power-loss calculations only | | | 0.85 | V |
| $r_T$ | $T_{VJ}$ = $T_{VJM}$ | | | 12 | mΩ |
| $R_{thJC}$ | per diode; DC current | | | 2.8 | K/W |
| | per module | | | 0.7 | K/W |
| $R_{thJK}$ | per diode; DC current | | | 3.4 | K/W |
| | per module | | | 0.85 | K/W |

Data according to IEC 60747 refer to a single diode unless otherwise stated.

### Features

- Package with screw terminals
- Isolation voltage 3000 V~
- Planar passivated chips
- Blocking voltage up to 1800 V
- Low forward voltage drop
- UL registered E 72873

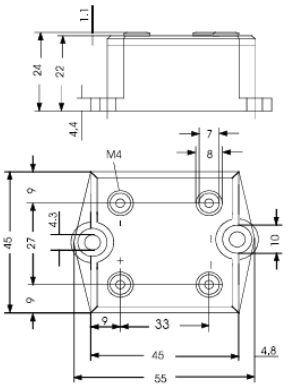
### Applications

- Supplies for DC power equipment
- Input rectifiers for PWM inverter
- Battery DC power supplies
- Field supply for DC motors

### Advantages

- Easy to mount with two screws
- Space and weight savings
- Improved temperature and power cycling

### Dimensions in mm (1 mm = 0.0394")




IXYS reserves the right to change limits, test conditions and dimensions.

FAIRCHILD SEMICONDUCTOR®

# HGTG20N60A4D, HGT4E20N60A4DS

**Data Sheet** **APRIL 2002**

## 600V, SMPS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode

This family of MOS gated high voltage switching devices combine the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C. The IGBT used is the development type TA49339. The diode used in anti-parallel is the development type TA49372.

These IGBT's are ideal for many high voltage switching applications operating at high frequencies where low conduction losses are essential. **These devices have been optimized for high frequency switch mode power supplies**.

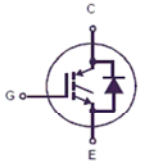
Formerly Developmental Type TA49341.

## Ordering Information

| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| HGTG20N60A4D | TO-247 | 20N60A4D |
| HGT4E20N60A4DS | TO-268 | 20N60A4DS |

NOTE: When ordering, use the entire part number.

## Symbol

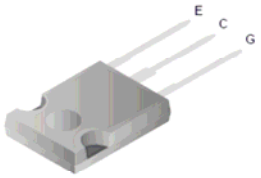



## Features

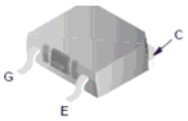
- >100kHz Operation At 390V, 20A
- 200kHz Operation At 390V, 12A
- 600V Switching SOA Capability
- Typical Fall Time . . . . . .55ns at $T_J$ = 125°C
- Low Conduction Loss
- *Temperature Compensating* SABER™ Model www.fairchildsemi.com

## Packaging

JEDEC STYLE TO-247




TO-268AA




FAIRCHILD SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 4,364,073 | 4,417,385 | 4,430,792 | 4,443,931 | 4,466,176 | 4,516,143 | 4,532,534 | 4,587,713 |
| 4,598,461 | 4,605,948 | 4,620,211 | 4,631,564 | 4,639,754 | 4,639,762 | 4,641,162 | 4,644,637 |
| 4,682,195 | 4,684,413 | 4,694,313 | 4,717,679 | 4,743,952 | 4,783,690 | 4,794,432 | 4,801,986 |
| 4,803,533 | 4,809,045 | 4,809,047 | 4,810,665 | 4,823,176 | 4,837,606 | 4,860,080 | 4,883,767 |
| 4,888,627 | 4,890,143 | 4,901,127 | 4,904,609 | 4,933,740 | 4,963,951 | 4,969,027 | |

## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | | HGTG20N60A4D, HGT4E20N60A4DS | UNITS |
|---|---|---|---|
| Collector to Emitter Voltage | $BV_{CES}$ | 600 | V |
| Collector Current Continuous | | | |
| At $T_C = 25^oC$ | $I_{C25}$ | 70 | A |
| At $T_C = 110^oC$ | $I_{C110}$ | 40 | A |
| Collector Current Pulsed (Note 1) | $I_{CM}$ | 280 | A |
| Gate to Emitter Voltage Continuous | $V_{GES}$ | ±20 | V |
| Gate to Emitter Voltage Pulsed | $V_{GEM}$ | ±30 | V |
| Switching Safe Operating Area at $T_J = 150^oC$ (Figure 2) | SSOA | 100A at 600V | |
| Power Dissipation Total at $T_C = 25^oC$ | $P_D$ | 290 | W |
| Power Dissipation Derating $T_C > 25^oC$ | | 2.32 | $W/^oC$ |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{STG}$ | -55 to 150 | $^oC$ |
| Maximum Lead Temperature for Soldering | $T_L$ | 260 | $^oC$ |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. Pulse width limited by maximum junction temperature.

## Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Collector to Emitter Breakdown Voltage | $BV_{CES}$ | $I_C = 250\mu A$, $V_{GE} = 0V$ | | 600 | - | - | V |
| Collector to Emitter Leakage Current | $I_{CES}$ | $V_{CE} = 600V$ | $T_J = 25^oC$ | - | - | 250 | μA |
| | | | $T_J = 125^oC$ | - | - | 3.0 | mA |
| Collector to Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C = 20A$, $V_{GE} = 15V$ | $T_J = 25^oC$ | - | 1.8 | 2.7 | V |
| | | | $T_J = 125^oC$ | - | 1.6 | 2.0 | V |
| Gate to Emitter Threshold Voltage | $V_{GE(TH)}$ | $I_C = 250\mu A$, $V_{CE} = 600V$ | | 4.5 | 5.5 | 7.0 | V |
| Gate to Emitter Leakage Current | $I_{GES}$ | $V_{GE} = ±20V$ | | - | - | ±250 | nA |
| Switching SOA | SSOA | $T_J = 150^oC$, $R_G = 3\Omega$, $V_{GE} = 15V$, $L = 100\mu H$, $V_{CE} = 600V$ | | 100 | - | - | A |
| Gate to Emitter Plateau Voltage | $V_{GEP}$ | $I_C = 20A$, $V_{CE} = 300V$ | | - | 8.6 | - | V |
| On-State Gate Charge | $Q_{g(ON)}$ | $I_C = 20A$, $V_{CE} = 300V$ | $V_{GE} = 15V$ | - | 142 | 162 | nC |
| | | | $V_{GE} = 20V$ | - | 182 | 210 | nC |
| Current Turn-On Delay Time | $t_{d(ON)I}$ | IGBT and Diode at $T_J = 25^oC$, $I_{CE} = 20A$, $V_{CE} = 390V$, $V_{GE} = 15V$, $R_G = 3\Omega$, $L = 500\mu H$, Test Circuit Figure 24 | | - | 15 | - | ns |
| Current Rise Time | $t_{rI}$ | | | - | 12 | - | ns |
| Current Turn-Off Delay Time | $t_{d(OFF)I}$ | | | - | 73 | - | ns |
| Current Fall Time | $t_{fI}$ | | | - | 32 | - | ns |
| Turn-On Energy (Note 3) | $E_{ON1}$ | | | - | 105 | - | μJ |
| Turn-On Energy (Note 3) | $E_{ON2}$ | | | - | 280 | 350 | μJ |
| Turn-Off Energy (Note 2) | $E_{OFF}$ | | | - | 150 | 200 | μJ |
| Current Turn-On Delay Time | $t_{d(ON)I}$ | IGBT and Diode at $T_J = 125^oC$, $I_{CE} = 20A$, $V_{CE} = 390V$, $V_{GE} = 15V$, $R_G = 3\Omega$, $L = 500\mu H$, Test Circuit Figure 24 | | - | 15 | 21 | ns |
| Current Rise Time | $t_{rI}$ | | | - | 13 | 18 | ns |
| Current Turn-Off Delay Time | $t_{d(OFF)I}$ | | | - | 105 | 135 | ns |
| Current Fall Time | $t_{fI}$ | | | - | 55 | 73 | ns |
| Turn-On Energy (Note 3) | $E_{ON1}$ | | | - | 115 | - | μJ |
| Turn-On Energy (Note 3) | $E_{ON2}$ | | | - | 510 | 600 | μJ |
| Turn-Off Energy (Note 2) | $E_{OFF}$ | | | - | 330 | 500 | μJ |

**Electrical Specifications** $T_J = 25^oC$, Unless Otherwise Specified **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Diode Forward Voltage | $V_{EC}$ | $I_{EC}$ = 20A | - | 2.3 | - | V |
| Diode Reverse Recovery Time | $t_{rr}$ | $I_{EC}$ = 20A, $dI_{EC}/dt$ = 200A/µs | - | 35 | - | ns |
| | | $I_{EC}$ = 1A, $dI_{EC}/dt$ = 200A/µs | - | 26 | - | ns |
| Thermal Resistance Junction To Case | $R_{\theta JC}$ | IGBT | - | - | 0.43 | $^oC/W$ |
| | | Diode | - | - | 1.9 | $^oC/W$ |

NOTE:

2. Turn-Off Energy Loss ($E_{OFF}$) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE}$ = 0A). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.
3. Values for two Turn-On loss conditions are shown for the convenience of the circuit designer. $E_{ON1}$ is the turn-on loss of the IGBT only. $E_{ON2}$ is the turn-on loss when a typical diode is used in the test circuit and the diode is at the same $T_J$ as the IGBT. The diode type is specified in Figure 20.

## *Typical Performance Curves* Unless Otherwise Specified

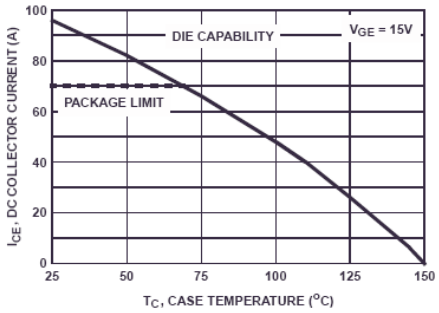



FIGURE 1. DC COLLECTOR CURRENT vs CASE TEMPERATURE

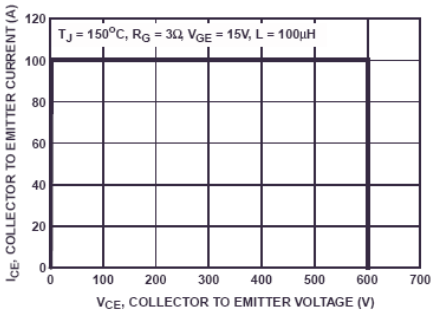



FIGURE 2. MINIMUM SWITCHING SAFE OPERATING AREA

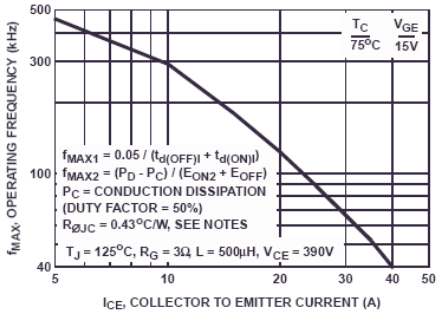



FIGURE 3. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT

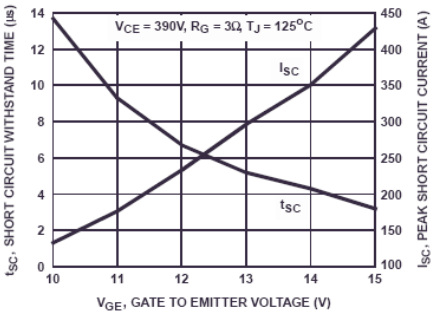



FIGURE 4. SHORT CIRCUIT WITHSTAND TIME

## Typical Performance Curves Unless Otherwise Specified (Continued)

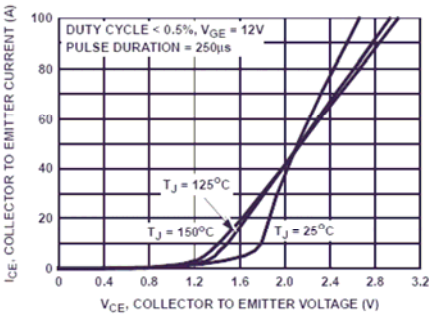



FIGURE 5. COLLECTOR TO EMITTER ON-STATE VOLTAGE

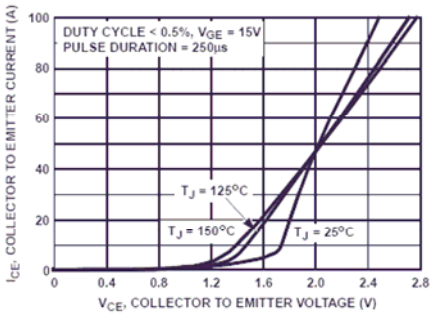



FIGURE 6. COLLECTOR TO EMITTER ON-STATE VOLTAGE

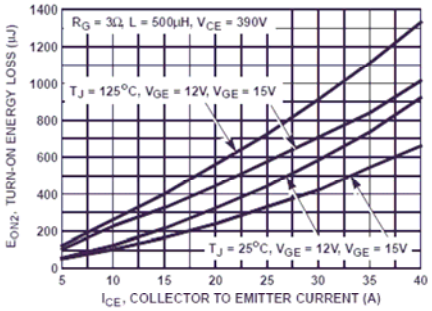



FIGURE 7. TURN-ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

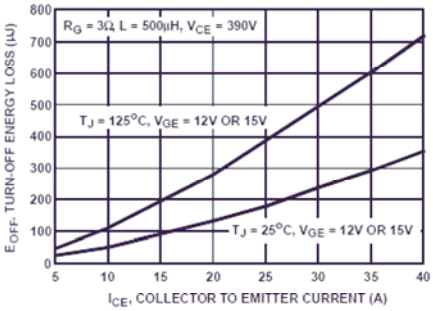



FIGURE 8. TURN-OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

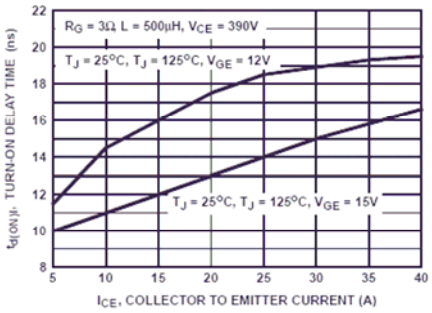



FIGURE 9. TURN-ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT

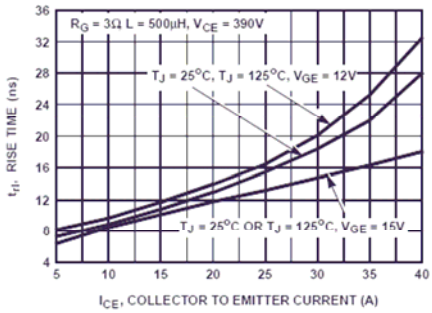



FIGURE 10. TURN-ON RISE TIME vs COLLECTOR TO EMITTER CURRENT

## Typical Performance Curves Unless Otherwise Specified (Continued)

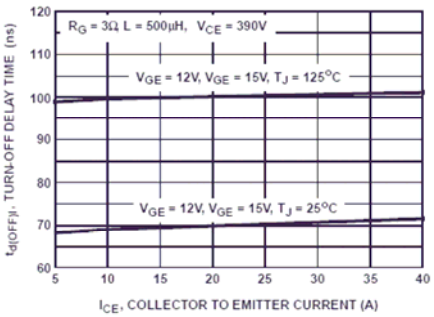



FIGURE 11. TURN-OFF DELAY TIME vs COLLECTOR TO EMITTER CURRENT

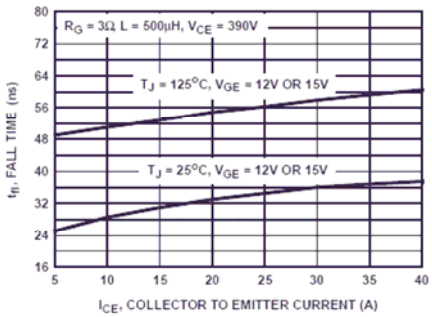



FIGURE 12. FALL TIME vs COLLECTOR TO EMITTER CURRENT

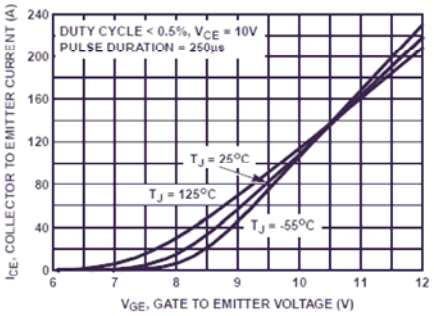



FIGURE 13. TRANSFER CHARACTERISTIC

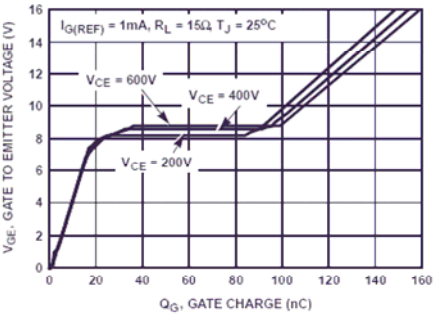



FIGURE 14. GATE CHARGE WAVEFORMS

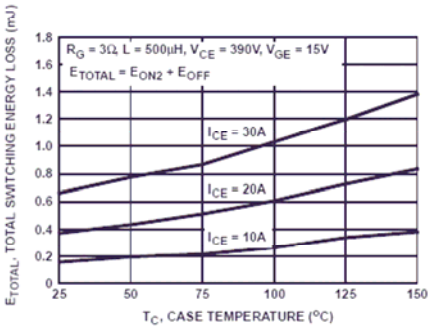



FIGURE 15. TOTAL SWITCHING LOSS vs CASE TEMPERATURE

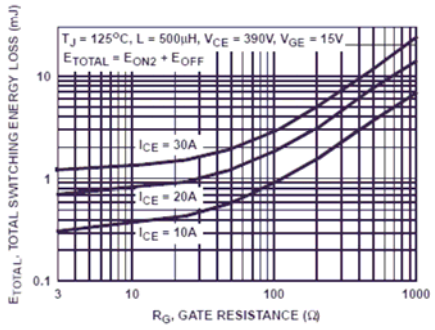



FIGURE 16. TOTAL SWITCHING LOSS vs GATE RESISTANCE

National Semiconductor

November 1994

# LM110/LM210/LM310 Voltage Follower

## General Description

The LM110 series are monolithic operational amplifiers internally connected as unity-gain non-inverting amplifiers. They use super-gain transistors in the input stage to get low bias current without sacrificing speed. Directly interchangeable with 101, 741 and 709 in voltage follower applications, these devices have internal frequency compensation and provision for offset balancing.

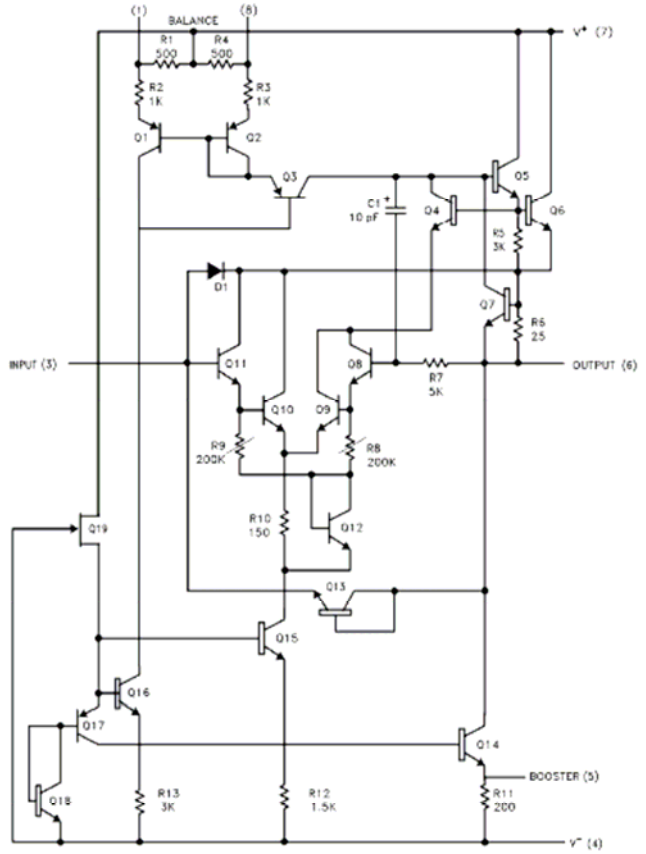
The LM110 series are useful in fast sample and hold circuits, active filters, or as general-purpose buffers. Further, the frequency response is sufficiently better than standard IC amplifiers that the followers can be included in the feedback loop without introducing instability. They are plug-in replacements for the LM102 series voltage followers, offering lower offset voltage, drift, bias current and noise in addition to higher speed and wider operating voltage range.

The LM110 is specified over a temperature range $-55°C \leq T_A \leq +125°C$, the LM210 from $-25°C \leq T_A \leq +85°C$ and the LM310 from $0°C \leq T_A \leq +70°C$.

## Features

| | |
|---|---|
| ■ Input current | 10 nA max over temperature |
| ■ Small signal bandwidth | 20 MHz |
| ■ Slew rate | 30 V/μs |
| ■ Supply voltage range | ±5V to ±18V |

## Schematic Diagram






RRD-B30M115/Printed in U. S. A.

## APPENDIX C: IGBT And Ultrafast Diode Selection Tables

| IGBT Code | $V_{CES}$ (min.) (V) | $I_C$ (in A at 25 $^0$C) | $I_C$ (in A at 110 $^0$C ) | $V_{CE}$ (sat.) V | Rise Time | Fall Time | Frequency | Digikey USD Price (Each/ 1000) |
|---|---|---|---|---|---|---|---|---|
| **IXSH30N60 B2D1** | 600 | 48 | 30 | 2.0 | $I_C$=24 A, $T_J$=25 $^0$C 30ns; $T_J$=125 $^0$C 50 ns | $I_C$ =24 A, $T_J$=25 $^0$C 140 ns typical, 300 ns max, $T_J$=125 $^0$C 234 ns typical | good up to 20 kHz | 3.29 |
| **IRG4PC50 UD** | 600 | 55 | 27 | 2.00 | $I_C$=27 A, $T_J$=25 $^0$C 25 ns, typical $T_J$ =150 $^0$C 27 ns | $I_C$ =27A, $T_J$=25 $^0$C 74 ns typical 110 ns max, $T_J$ =150 $^0$C 130 ns | Ultrafast 8-60 kHz | 7.01 |
| **IRGP50B 60PD** | 600 | 75 | 42 | 2.2 | $I_C$=33 A, $T_J$=25 $^0$C 26 ns typical 36 ns max, $T_J$=125 $^0$C 26 ns typical 36 ns max | $I_C$ =33A, $T_J$=25 $^0$C 43 ns typical 56ns max, $T_J$=125 $^0$C 50 ns typical 65 ns max | WARP 60-150 kHz | 7.54 |
| **IRGP50B60 PD1** | 600 | 75 | 45 | 2.35 | $I_C$=33 A $T_J$=25 $^0$C rise time=10 ns typical 15 ns max, $T_J$=125 $^0$C rise time 13 ns typical 20 ns max | $I_C$ =33 A $T_J$=25 $^0$C fall time=11 ns typical 15 ns, $T_J$=125 $^0$C fall time= 15 ns typical 20ns max | WARP 60-150 kHz | 6.20 |
| **IRG4PC50 W-ND** | 600 | 55 | 27 | 2.3 | $I_C$=27 A $T_J$=25 $^0$C rise time=33 ns typical, $T_J$ =150 $^0$C rise time 43ns typical | $I_C$ =27 A $T_J$=25 $^0$C fall time=57 ns typical 86 ns typical, $T_J$=125 $^0$C fall time 62 ns typical | WARP 60-150 kHz | 3.91 |
| **HGTG20N60 A4D** | 600 | 70 | 40 | $T_J$=25 $^0$C 2.7 V max; $T_J$=125 $^0$C 2.0 V max | $I_C$=20 A $T_J$=25 $^0$C rise time=12 ns typical; $T_J$=125 $^0$C rise time=13 ns typical 18 ns max | $I_C$ =20 A $T_J$=25 $^0$C fall time=32 ns typical, $T_J$=125 $^0$C fall time 55 ns typical 73 ns max | Ic=20 A max. at 100 kHz switching, 12 A max at 200 kHz switching | 2.93 |

**Table C.1** IGBT selection table.

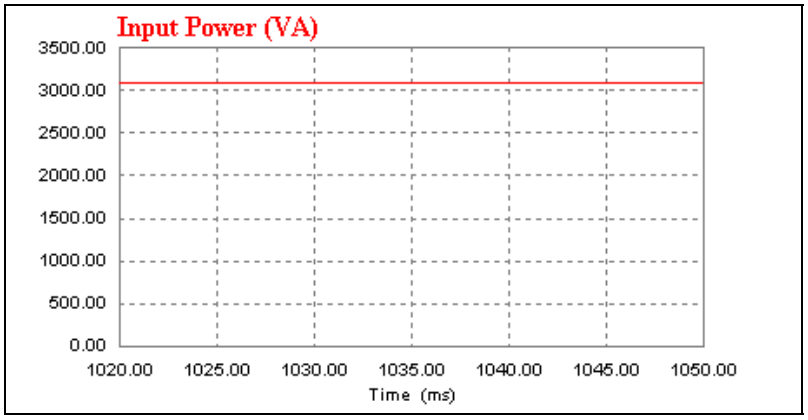
| Diode Code | $V_{RRM}$ Max (V) | $I_O$ (rec.) Max (A) at $T_J$ =125 $^0$C (nearly) | $I_{FSM}$ Max (A) | $V_{FM}$ Max (V) | $t_{rr}$ (ns) | Digikey USD Price (Each/ 1000) |
|---|---|---|---|---|---|---|
| **MUR3060PT** | 600 | 30 | 150 | $I_F$=15 A T=150 $^0$C 1.2V max, T=25 $^0$C 1.5 V max | $I_F$=1.0 A di/dt=50A/us 60 ns max | 1.40 |
| **MUR3060WT** | 600 | 30 | 150 | $I_F$ =15 A T=150 $^0$C 1.4 V max, T=25 $^0$C 1.7 V max | $I_F$=1.0 A di/dt=50A/us 60 ns max | 1.55 |
| **RURG3060** | 600 | 30 | 325 | $I_F$=30 A T=25 $^0$C 1.5 V max, T=150 $^0$C 1.3V max | $I_F$=1.0 A di/dt=100A/us 55 ns max, $I_F$=30 A di/dt=100A/us 60 ns max | 1.35 |
| **ISL9R3060P2** | 600 | 30 | 325 | 2.4 ($I_F$=30A T=25 $^0$C 2.1 V typical 2.4 V max, T=125 $^0$C 1.7 V typical 2.1 V max) | 35ns ($I_F$=30A T=25 $^0$C 36ns typical 110 ns max) | 1.58 |
| **RURP3060** | 600 | 30 | 325 | $I_F$ =30 A T=25 $^0$C 1.5 V max, T=150 $^0$C 1.3 V max | $I_F$=1A $dI_F/dt$=100A/us 55 ns max, $I_F$=30A dIF/dt=100A/us 60 ns max | 1.11 |
| **RHRG3060** | 600 | 30 | 325 | $I_F$ =30 A T=25 $^0$C 2.1 V max, T=150 $^0$C 1.7 V max | $I_F$=1A $dI_F/dt$=200A/us 40 ns max, $I_F$=30A $dI_F/dt$=200A/us 45 ns max | 1.45 |
| **30EPH06** | 600 | 30 | 325 A(60Hz) | 2.1 ($I_F$=30A, T=25 $^0$C 2.0 V typical, 2.6 V max and $I_F$=30A, T=150 $^0$C 1.34 V typical 1.75 V max) | 40 ns (T=25 $^0$C $I_F$=30 A, trr=31 ns typical and T=125 $^0$C $I_F$=30 A, trr=77 ns typical | 1.34 |
| **DSEI30-06A** | 600 | 37 | 260 | 1.4 ($I_F$ =37 A T=25 $^0$C 1.6V max, T=150 $^0$C 1.4V max) | $I_F$=1 A, di/dt=100A/us, $V_R$=30 V, $T_{VJ}$=25 $^0$C typical 35ns, Max 50 ns | 1.34 |
| **DSEK60-06A** | 600 | 2x30 | 260 | 1.4 ($I_F$=37 A T=25 $^0$C 1.6 V max, T=150 $^0$C 1.4 V max) | $I_F$=1 A, di/dt=100A/us , $V_R$=30 V, $T_{VJ}$=25 $^0$C typical 35ns, Max 50 ns | 2.99 |
| **DSEP30-06A/B/BR** | 600 | 30 | 250 | Version A 1.25 ($I_F$=30 A T=25 $^0$C 1.6V max, T=150 $^0$C 1.25V max), Version B 1.56 ($I_F$=30 T=25 $^0$C 2.51 V max, T=150 $^0$C 1.56 V max) | $I_F$=1 A, di/dt=100A/us , $V_R$=30 V, $T_{VJ}$=25 $^0$C Version A 35 ns max, Version B 30 ns max | 1.68 |

**Table C.2** Ultrafast diode selection table.

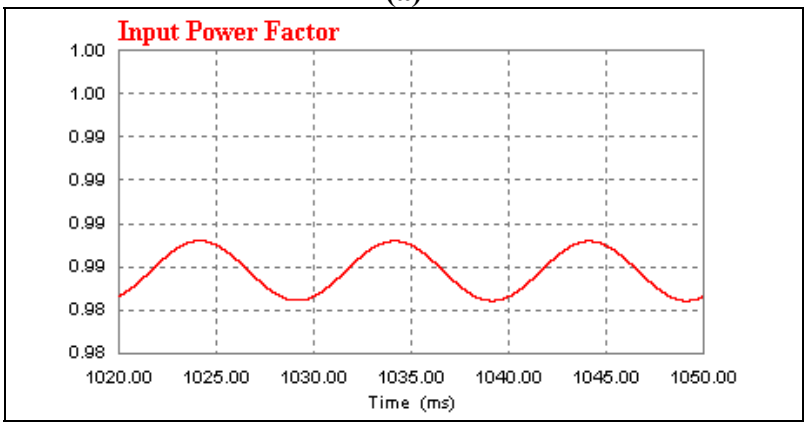
## APPENDIX D: Classical UPF Rectifier And Proposed Rectifier's Waveforms Obtained Via Simulations

### D.1 Waveforms of Classical Unity Power Factor Rectifier And Proposed Rectifier With 3 kW Purely Resistive Load

#### D.1.1 Waveforms of Classical Unity Power Factor Rectifier With 3 kW Purely Resistive Load

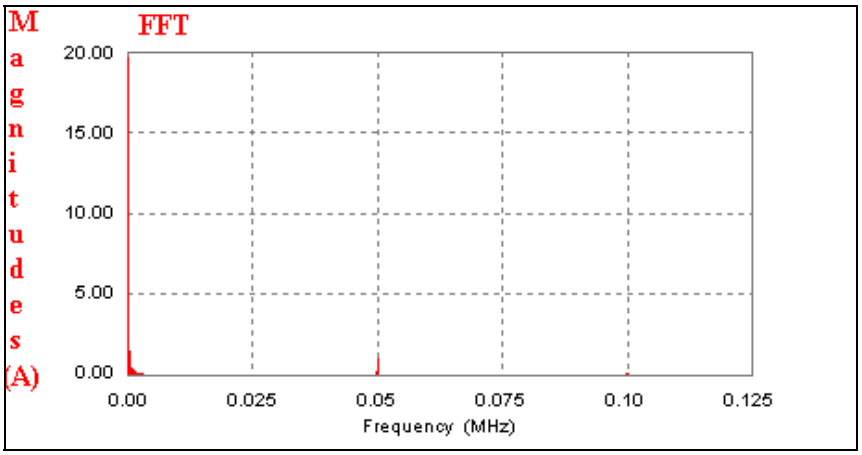



**(a)**

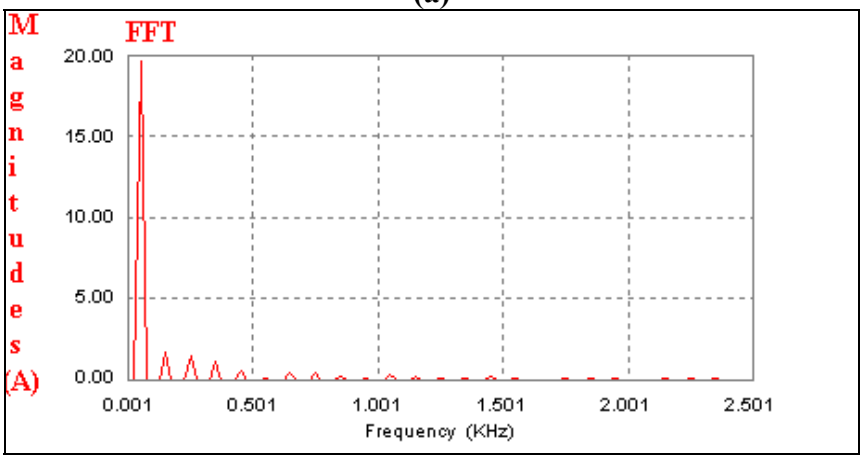



**(b)**

**Figure D.1** Classical unity power factor rectifier's input power and power factor at purely resistive 3 kW load, (a) its input power, (b) its power factor graph.




**(a)**




**(b)**

**Figure D.2** (a) FFT waveform of classical unity power factor rectifier's input current at 3 kW purely resistive load at steady state, (b) its zoomed version.

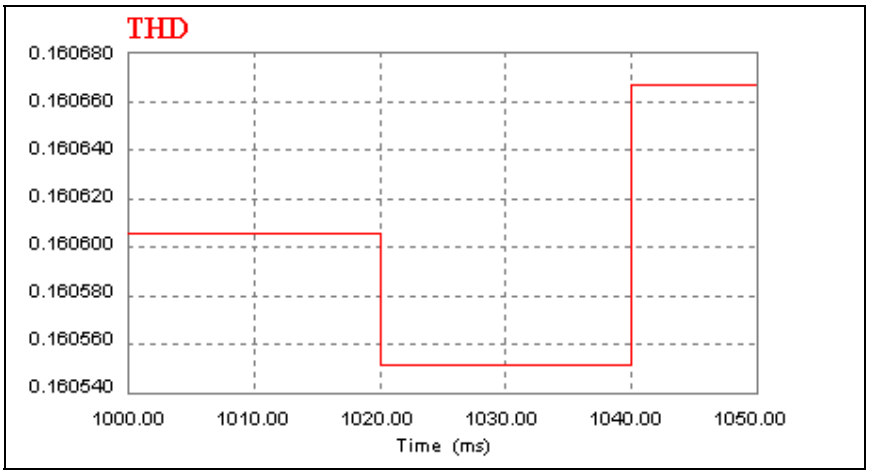
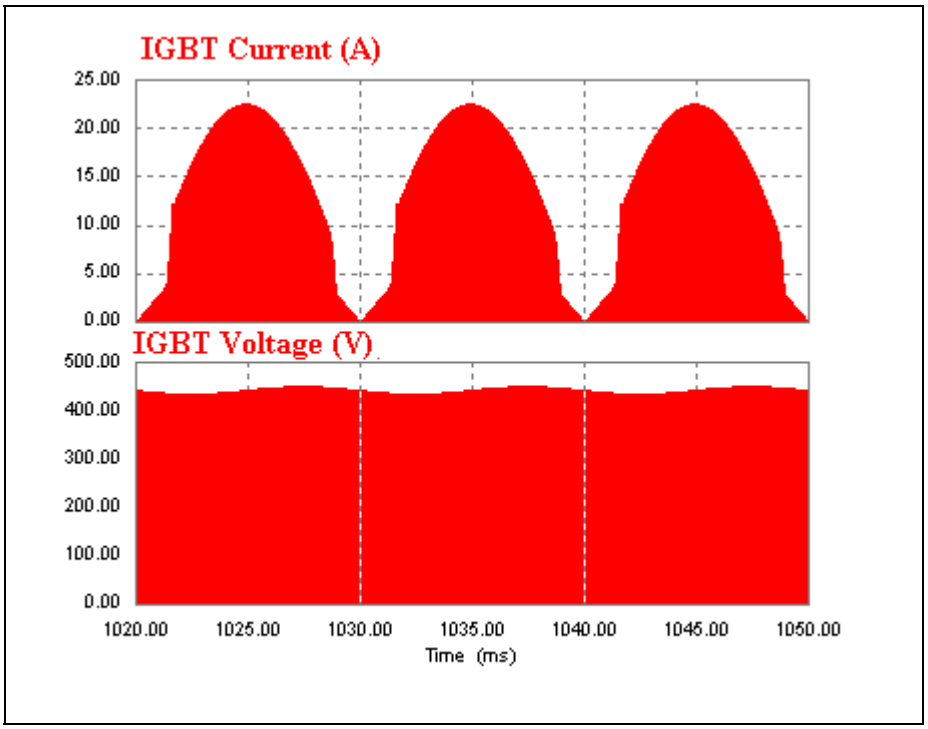
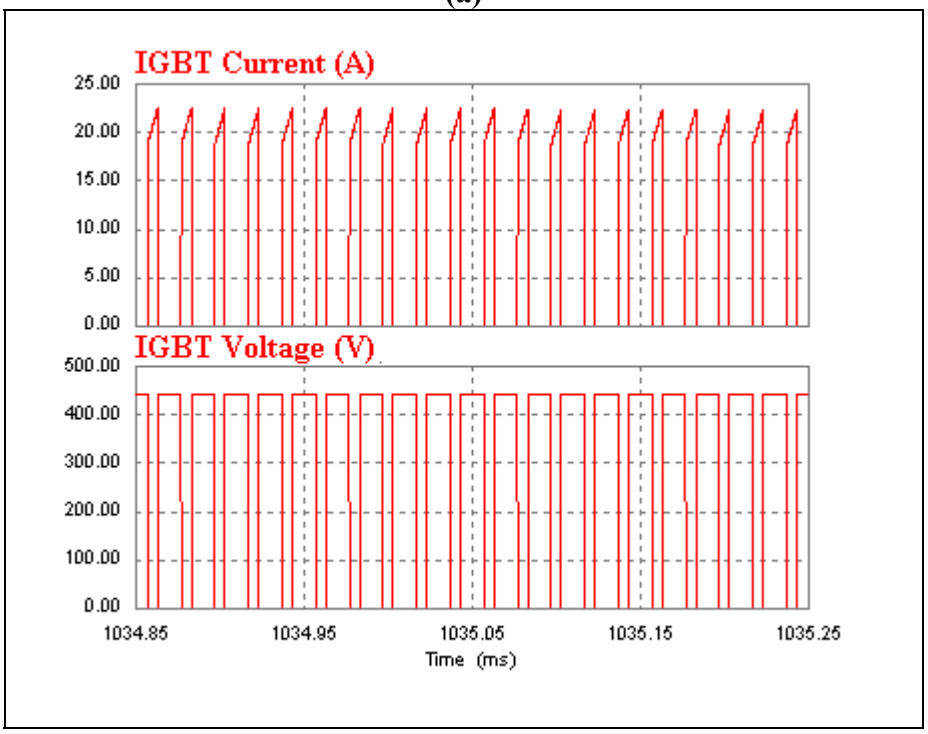



**Figure D.3** THD of classical UPF rectifier's input current at 3 kW purely resistive load at steady state.

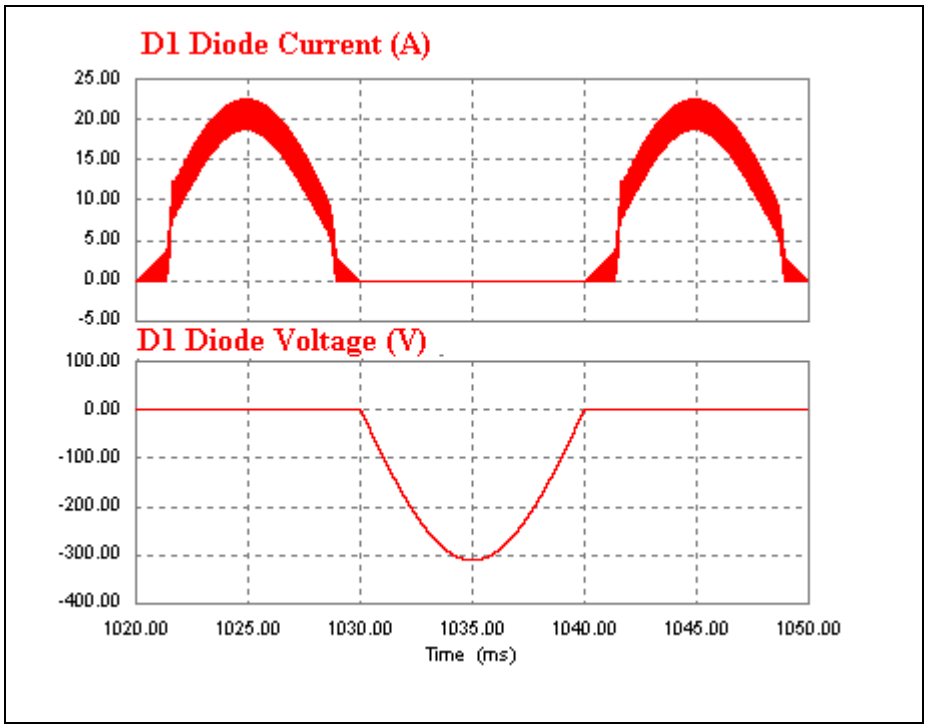



**(a)**

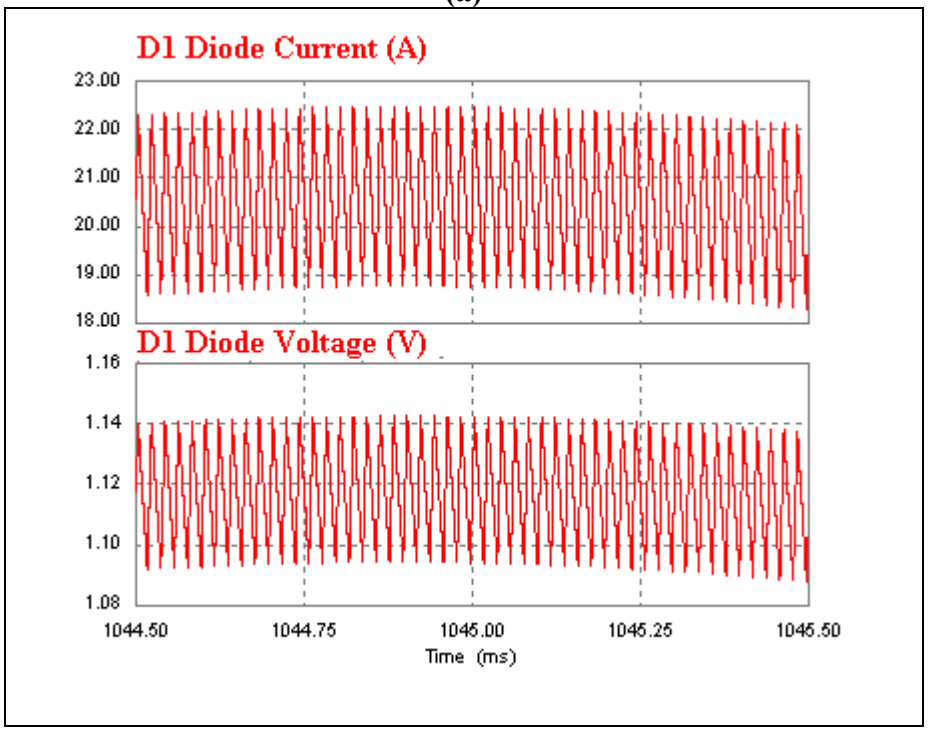



**(b)**

**Figure D.4** (a) IGBT's current and voltage waveform of classical UPF rectifier with 3 kW purely resistive load at steady state, (b) their zoomed version.

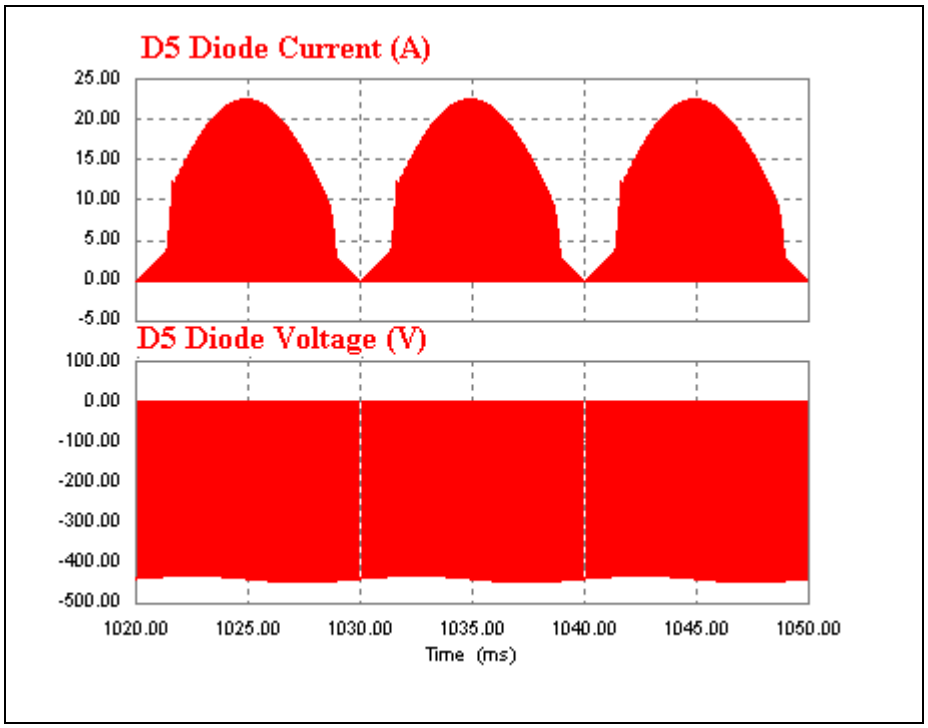



**(a)**

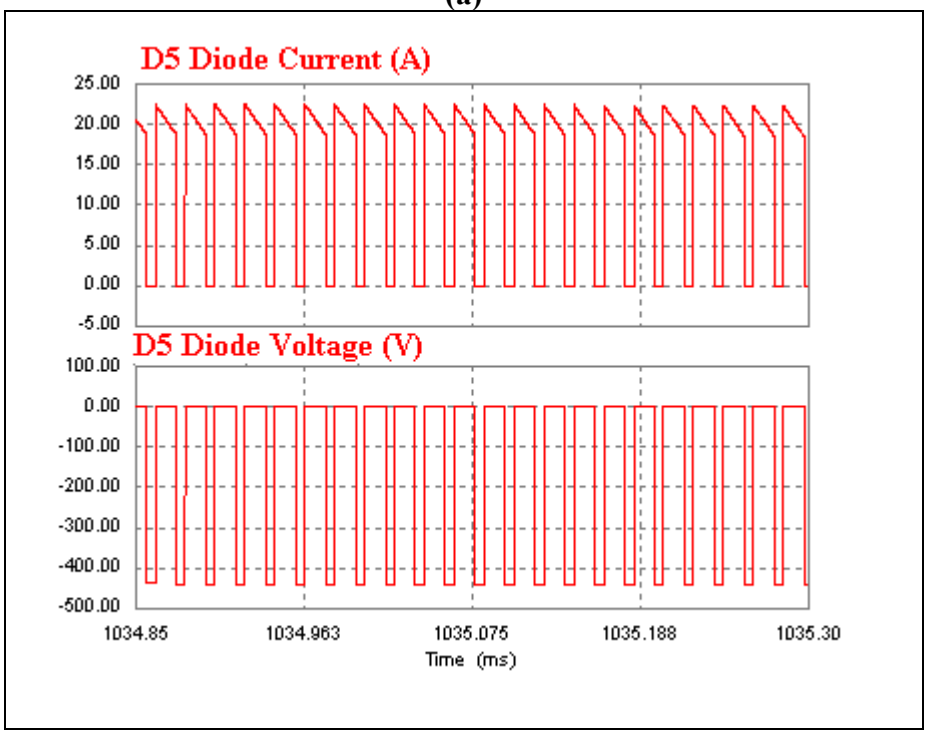



**(b)**

**Figure D.5** (a) One of the bridge diodes, D1's current and voltage waveform of classical UPF rectifier with 3 kW purely resistive load at steady state, (b) their zoomed version.



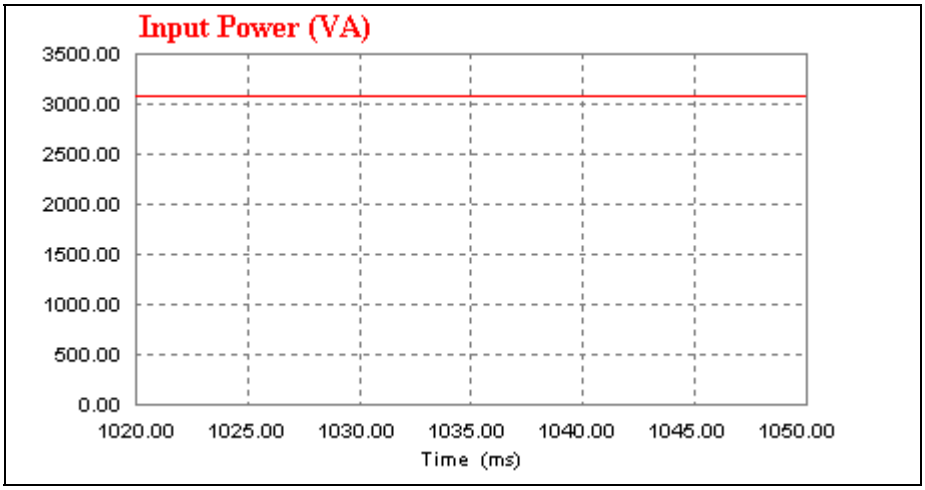

**(a)**



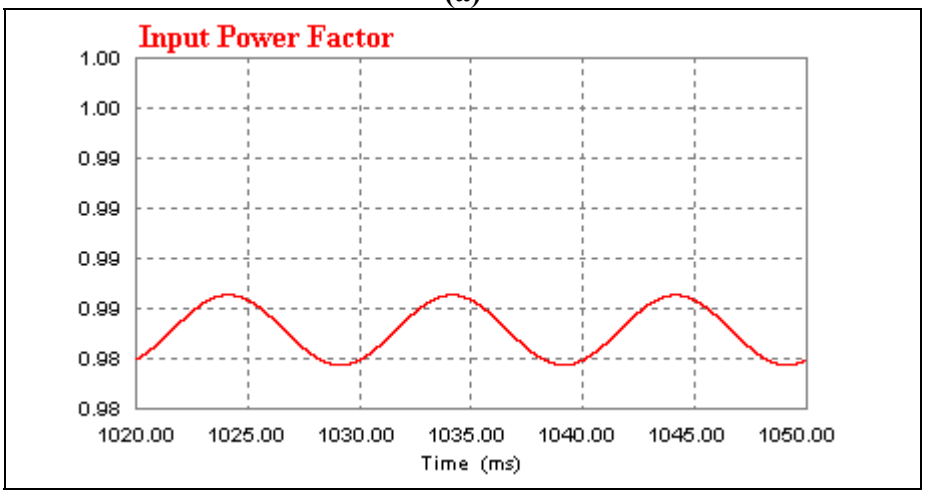

**(b)**

**Figure D.6** (a) Boost diode, D5's current and voltage waveform of classical UPF rectifier with 3 kW purely resistive load at steady state, (b) their zoomed version.

### D.1.2 Waveforms of Proposed Rectifier With 3 kW Purely Resistive Load

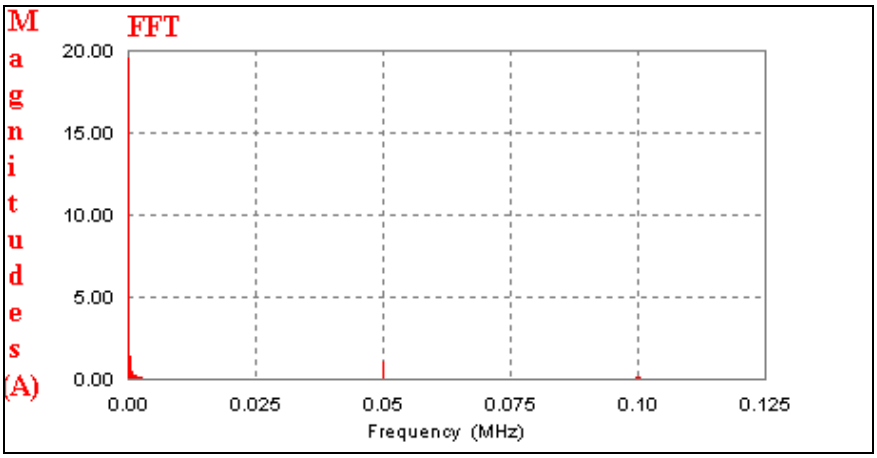



**(a)**

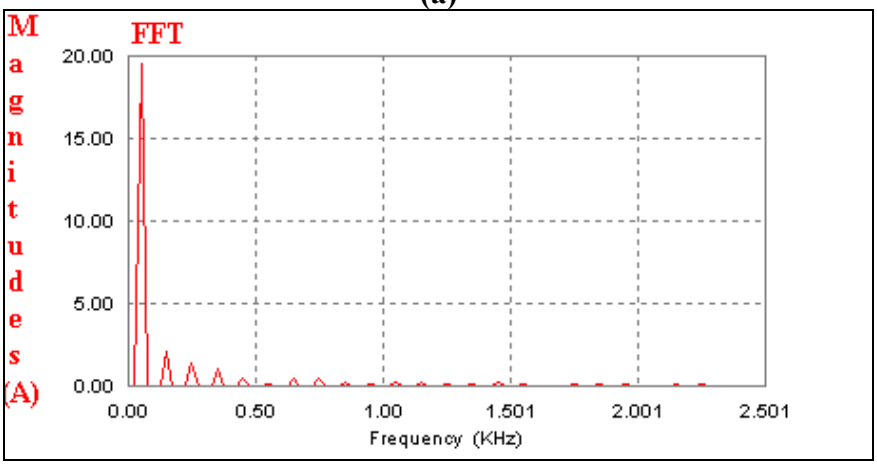



**(b)**

**Figure D.7** Proposed rectifier's input power and power factor graph at purely resistive 3 kW load, (a) its input power, (b) its power factor graph.




**(a)**




**(b)**

**Figure D.8** (a) FFT waveform of proposed rectifier's input current at 3 kW purely resistive load at steady state, (b) its zoomed version.

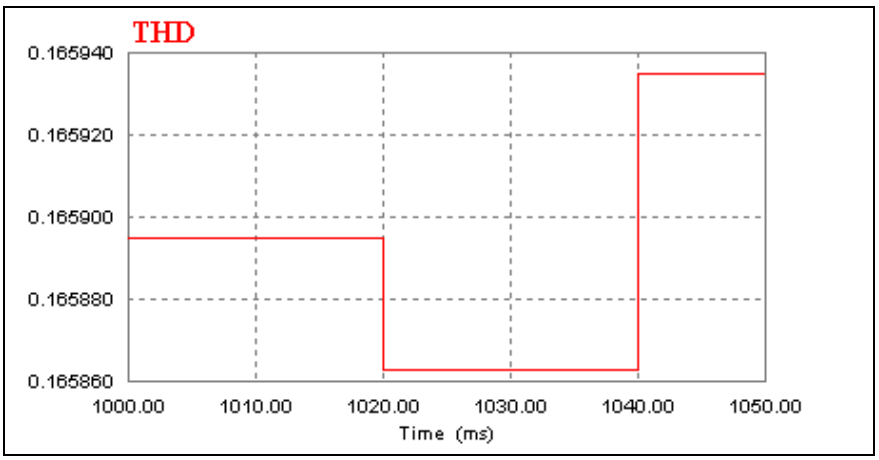
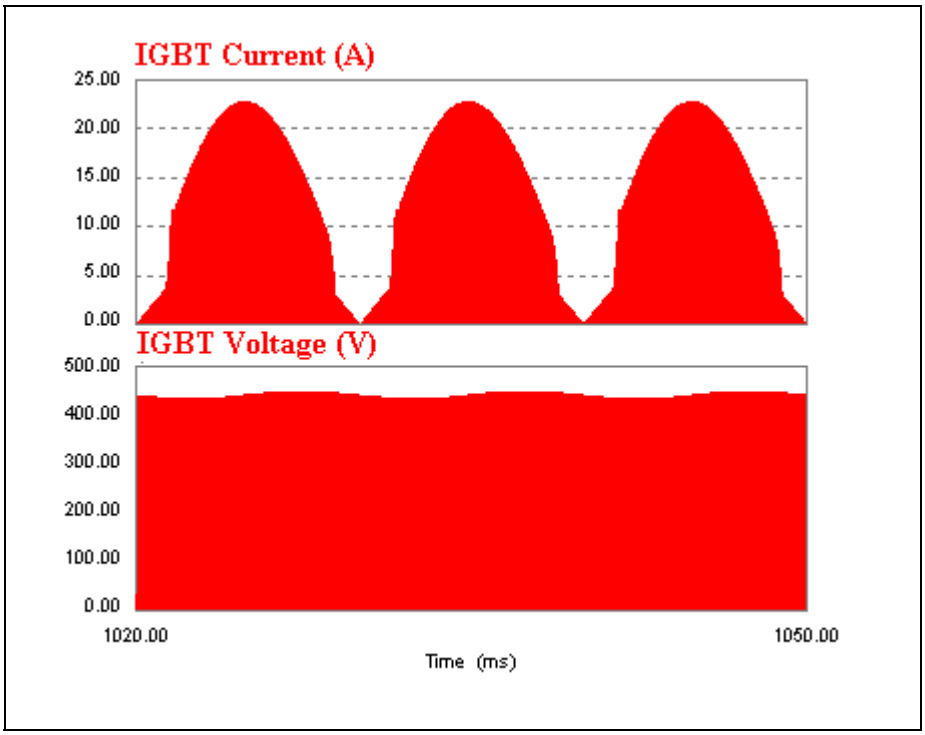
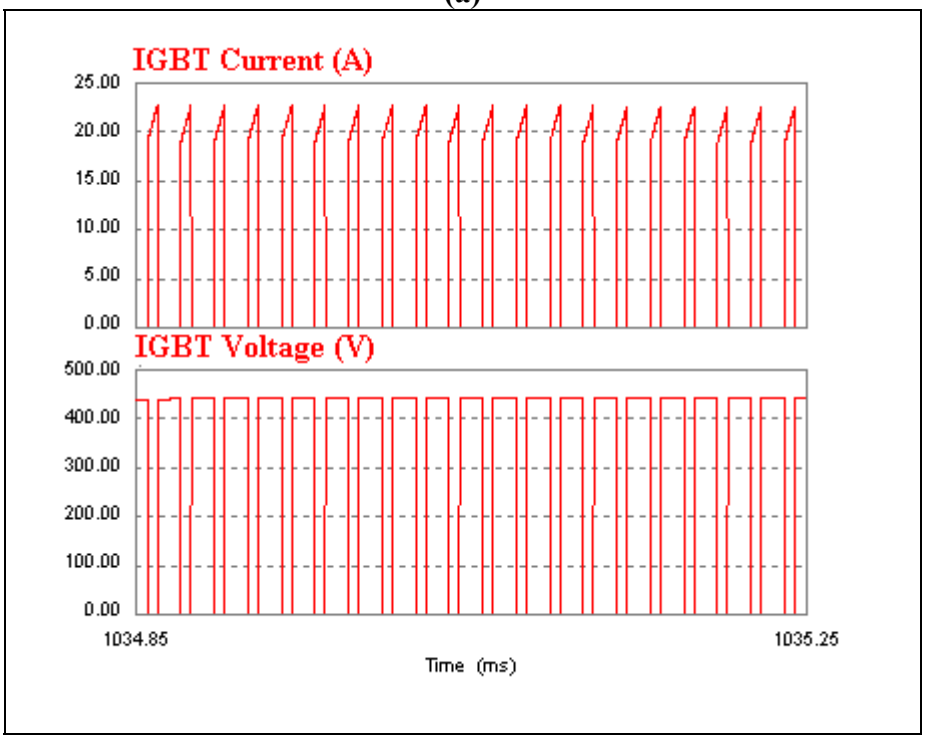



**Figure D.9** THD of proposed rectifier's input current at 3 kW purely resistive load at steady state.

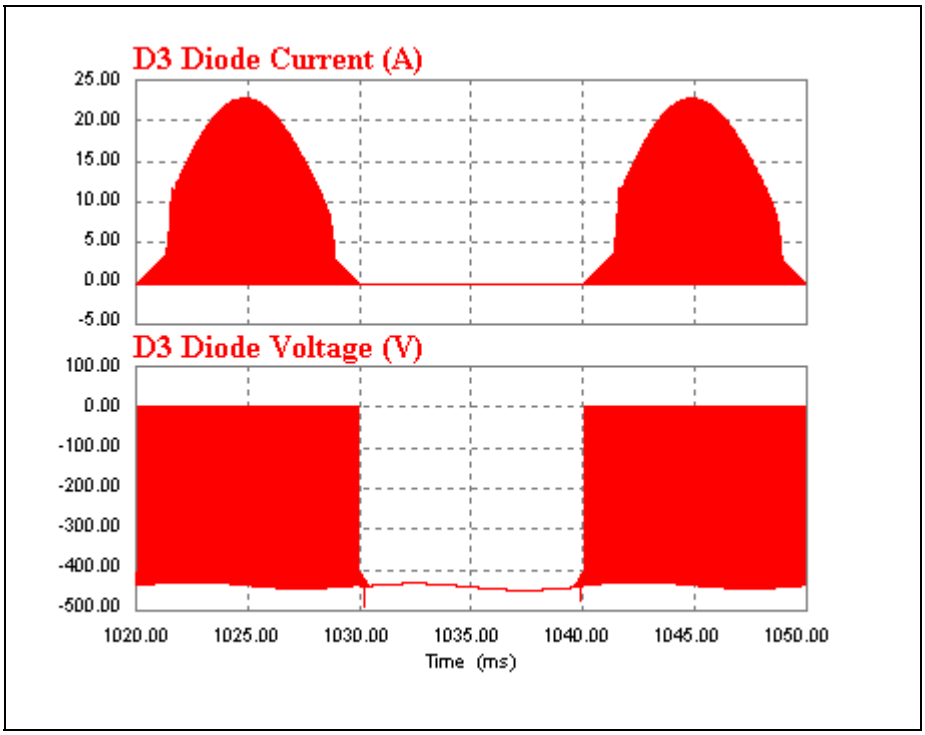



**(a)**

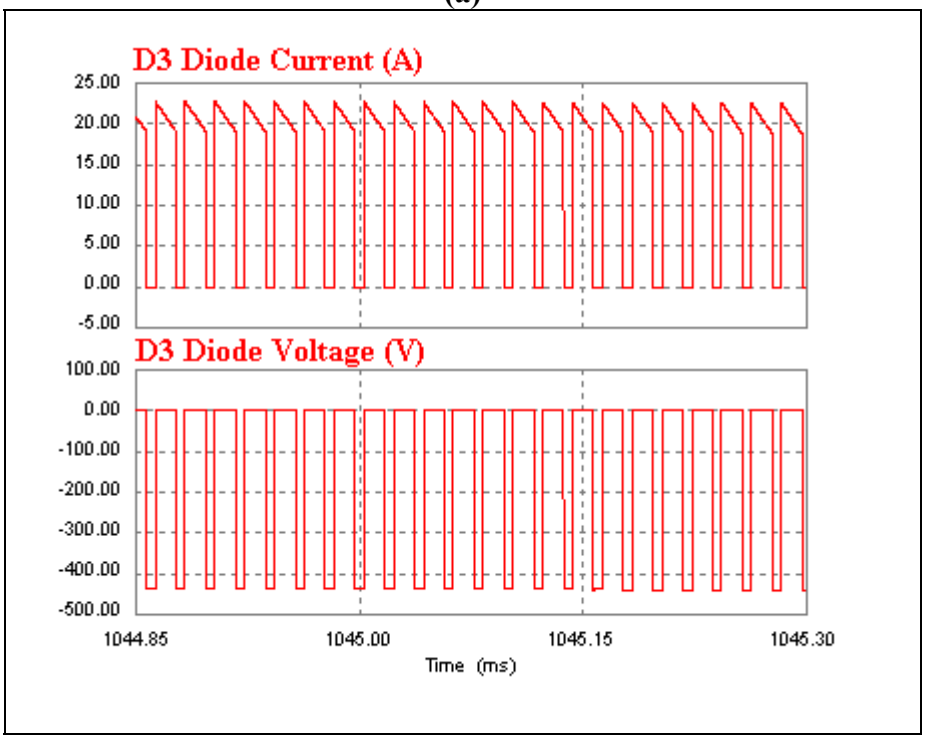



**(b)**

**Figure D.10** (a) IGBT's current and voltage waveform of proposed rectifier with 3 kW purely resistive load at steady state, (b) their zoomed versions.

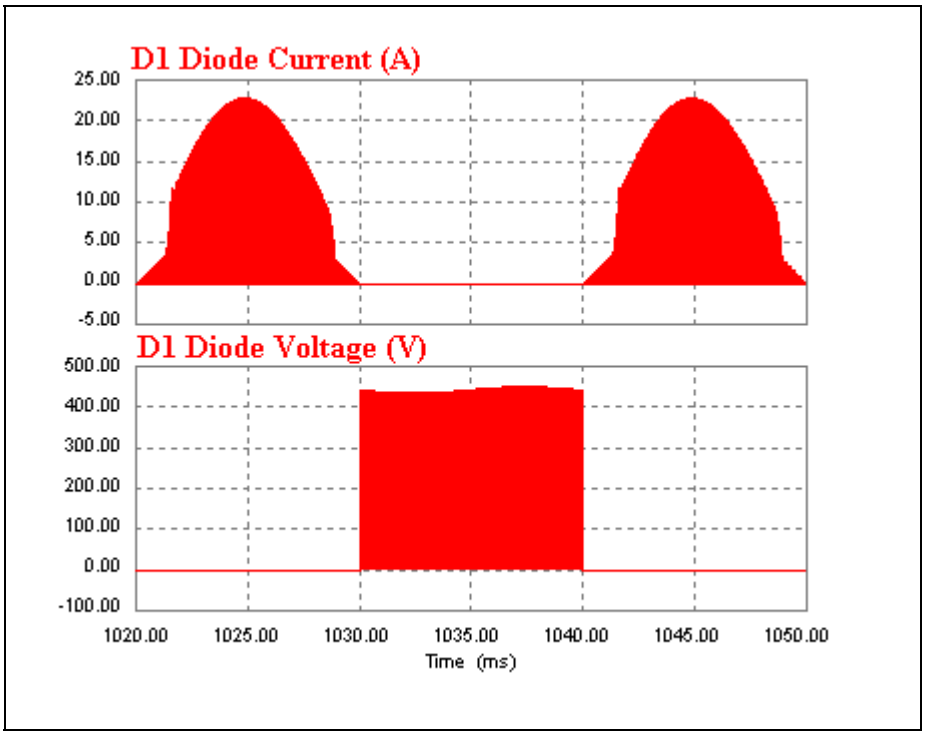



**(a)**

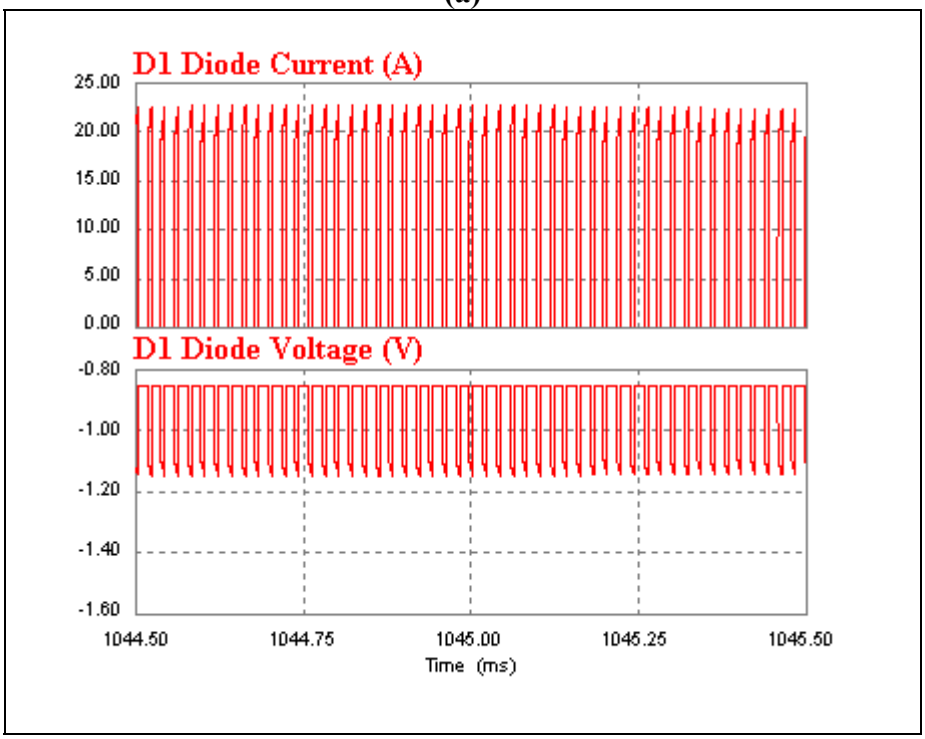



**(b)**

**Figure D.11** (a) One of the boost diodes, D3's current and voltage waveform of proposed UPF rectifier with 3 kW purely resistive load at steady state, (b) their zoomed versions.




**(a)**




**(b)**

**Figure D.12** (a) One of the bridge diodes, D1's current and voltage waveform of proposed UPF rectifier with 3 kW purely resistive load at steady state, (b) their zoomed versions.

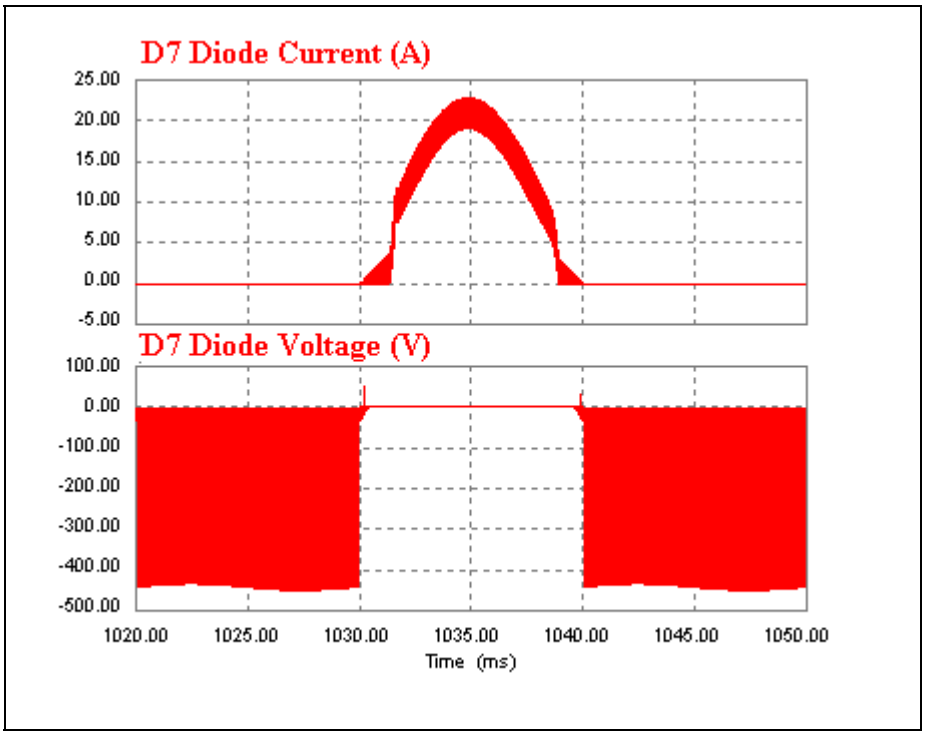
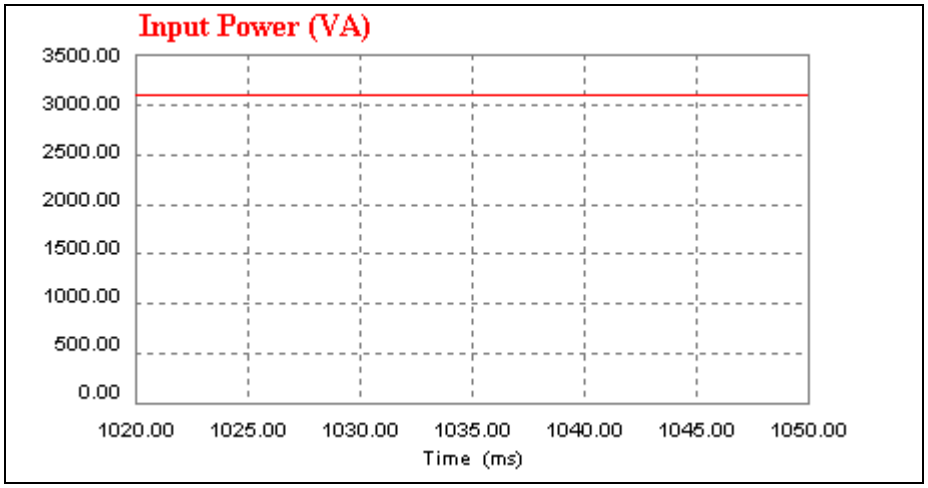



**Figure D.13** (a) One of the bridge diodes, D7's current and voltage waveform of proposed UPF rectifier with 3 kW purely resistive load at steady state, (b) their zoomed versions.

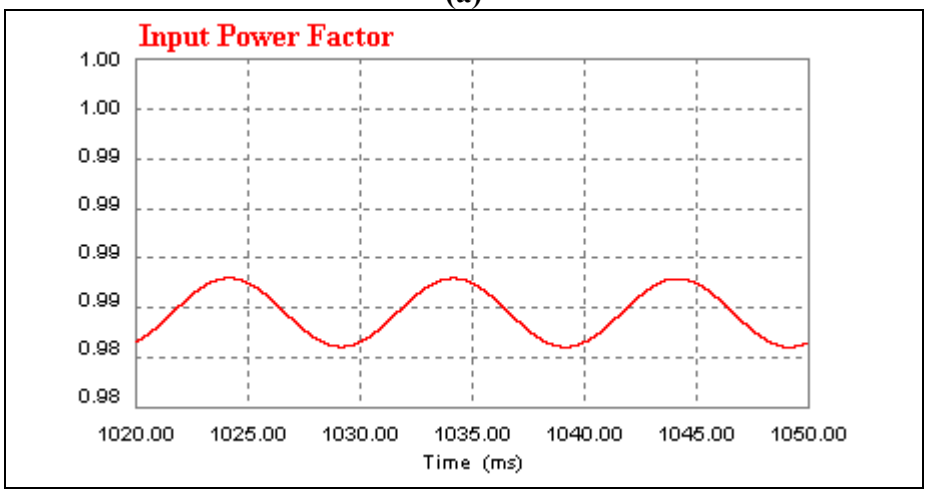
## D.2 Waveforms of Classical Unity Power Factor Rectifier And Proposed Rectifier With 3 kW Inductive-Resistive Load

### D.2.1 Waveforms of Classical Unity Power Factor Rectifier With 3 kW Inductive-Resistive Load

#### D.2.1.1 Waveforms of Classical Unity Power Factor Rectifier With 3 kW Inductive-Resistive Load (100 uH)




**(a)**




**(b)**

**Figure D.14** Classical unity power factor rectifier's input power and power factor at inductive-resistive 3 kW load (100 uH), (a) its input power, (b) its power factor.

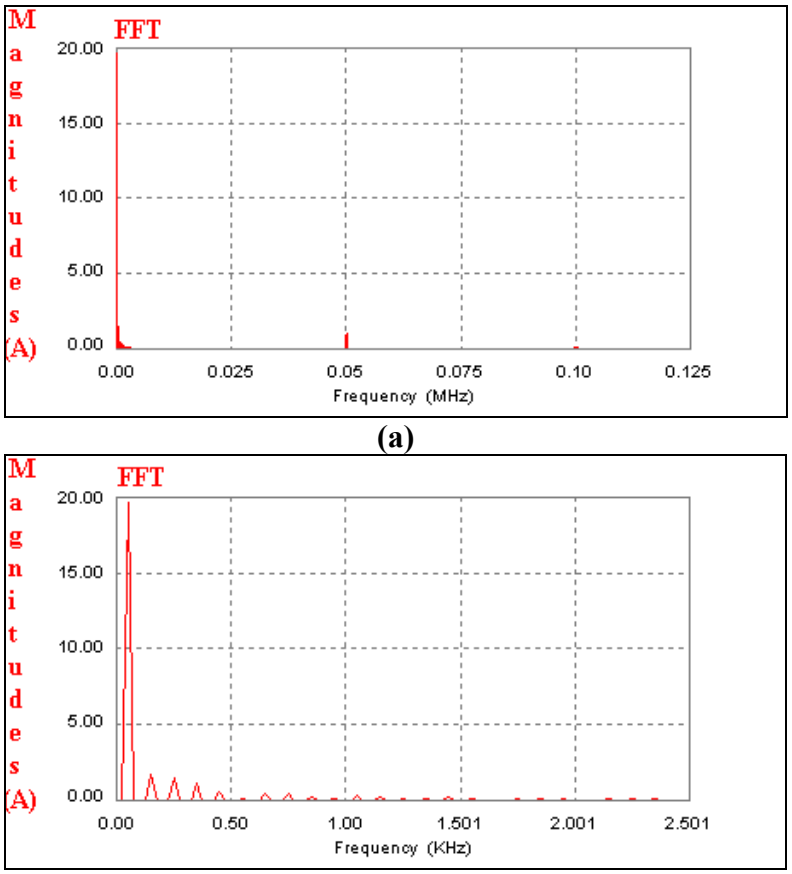



**Figure D.15** (a) FFT waveform of classical unity power factor rectifier's input current at 3 kW inductive-resistive load (100 uH) at steady state, (b) its zoomed version.

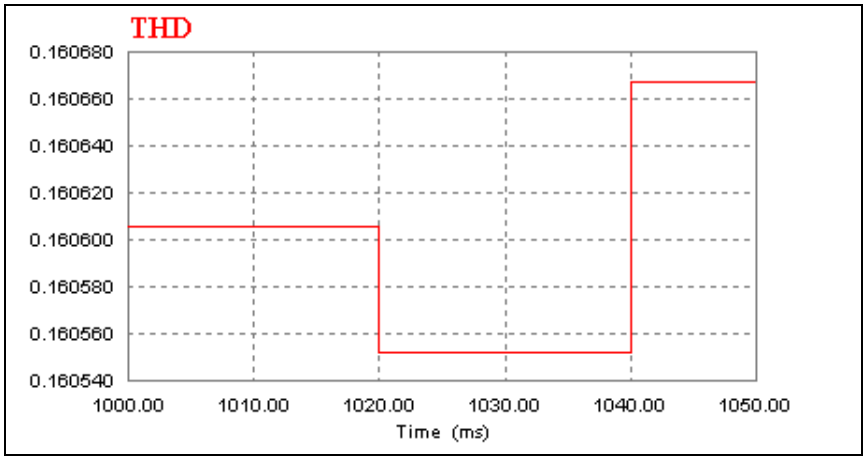
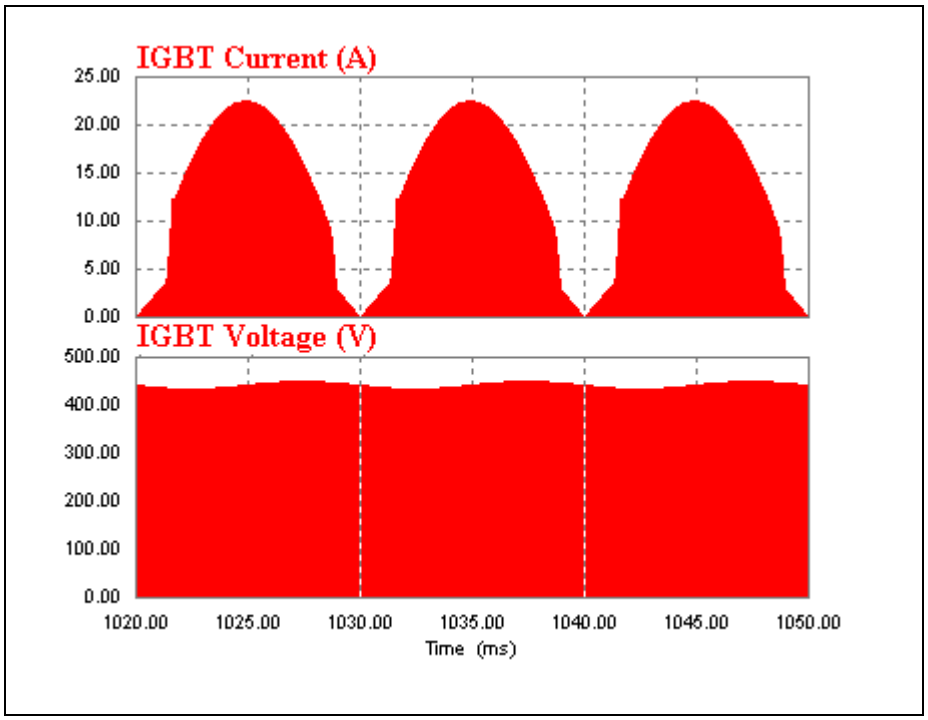
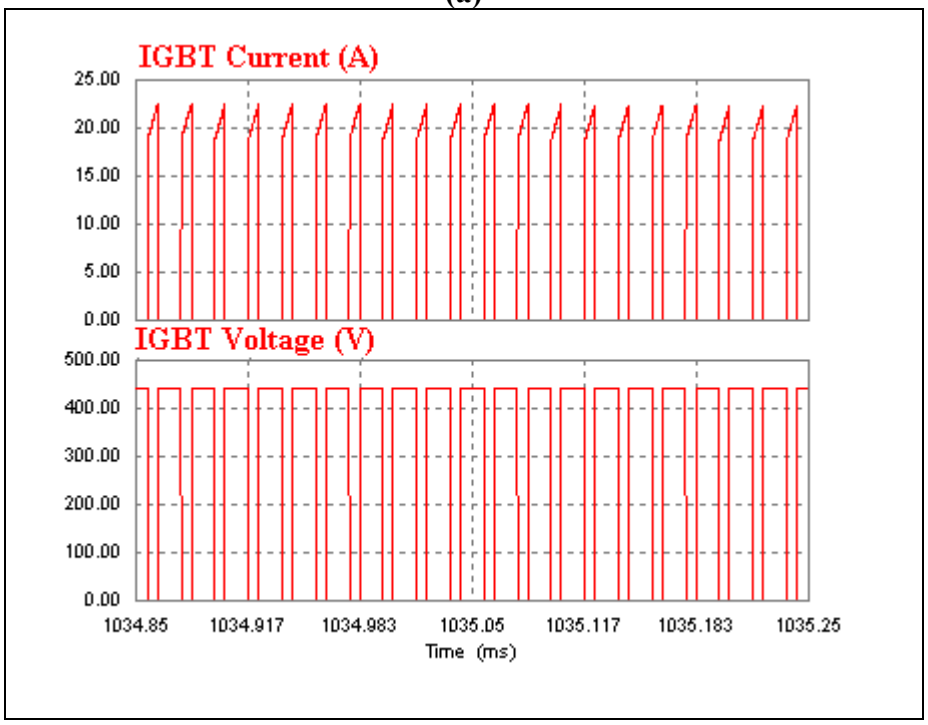



**Figure D.16** THD of classical UPF rectifier's input current at 3 kW inductive-resistive load (100 uH) at steady state.

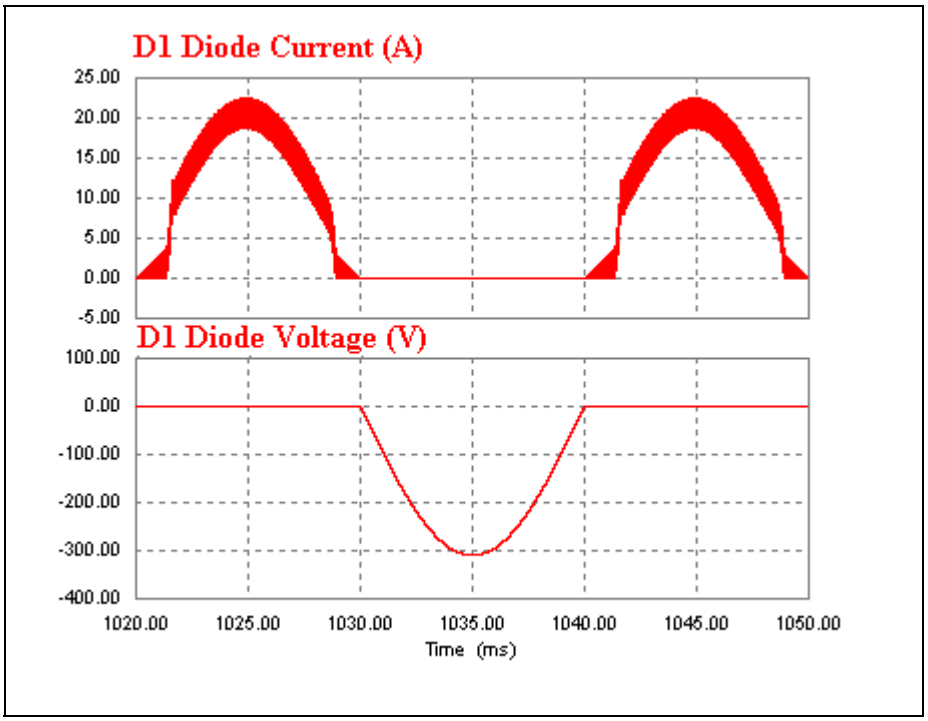



**(a)**

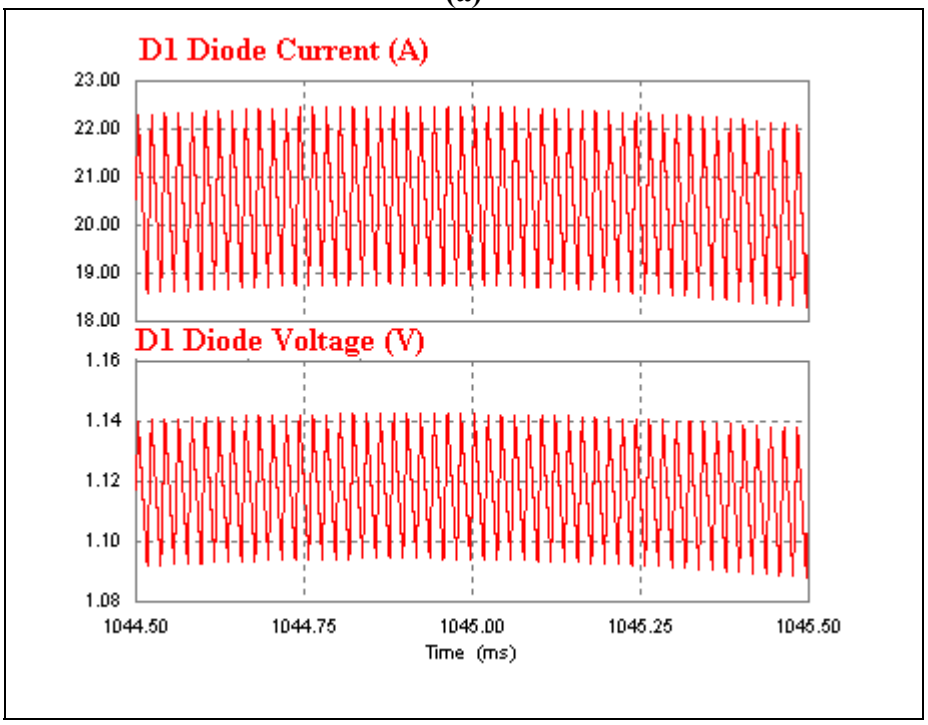



**(b)**

**Figure D.17** (a) IGBT's current and voltage waveform of classical UPF rectifier with 3 kW inductive-resistive load (100 uH) at steady state, (b) their zoomed version.

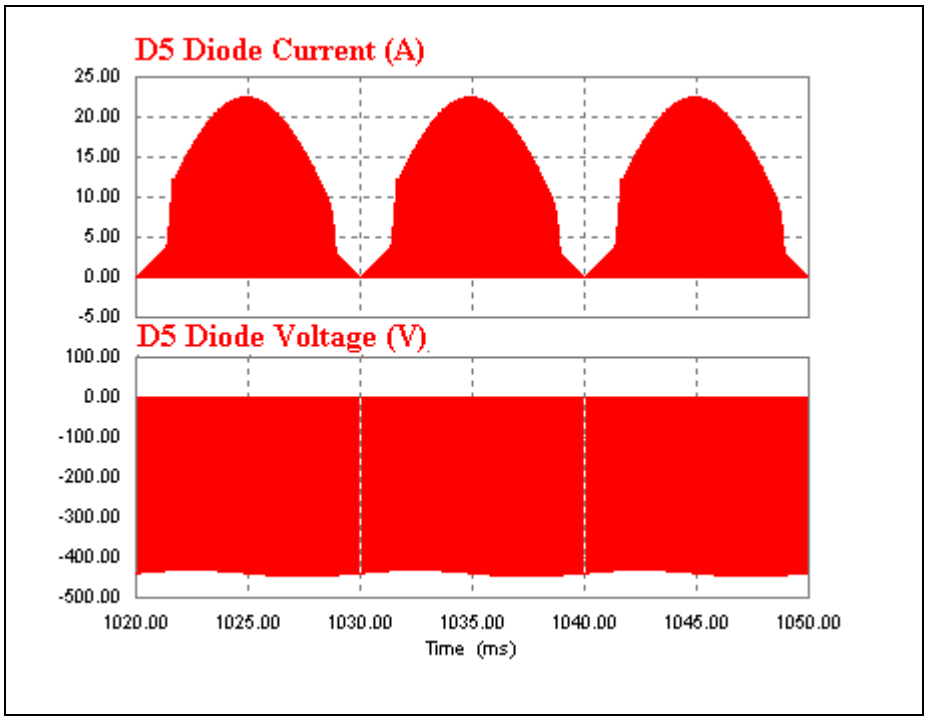



**(a)**

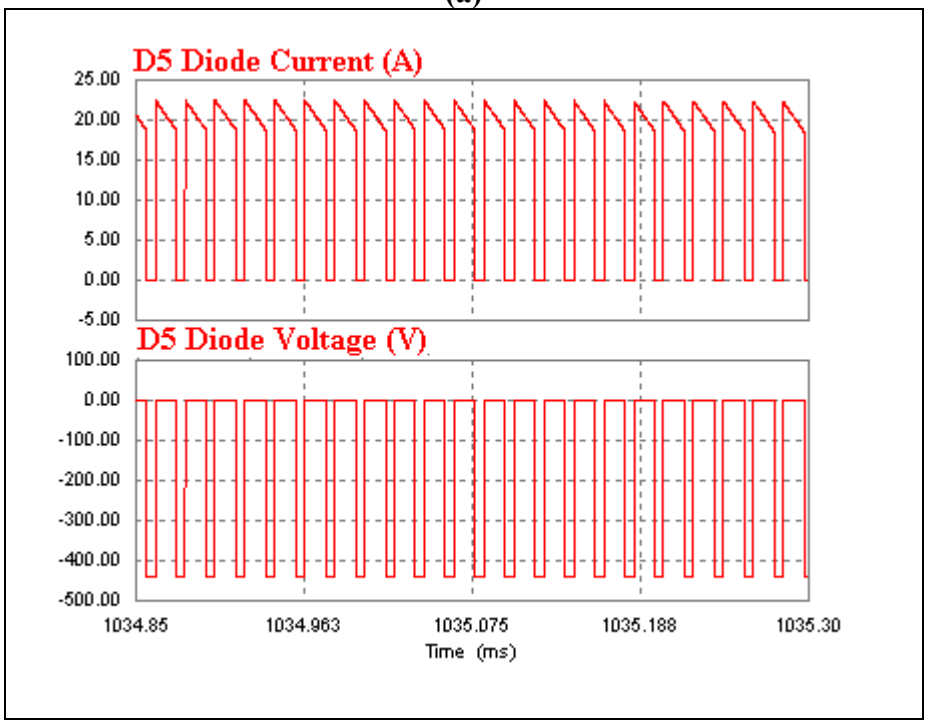



**(b)**

**Figure D.18** (a) One of the bridge diodes, D1's current and voltage waveform of classical UPF rectifier with 3 kW inductive-resistive load (100 uH) at steady state, (b) their zoomed version.



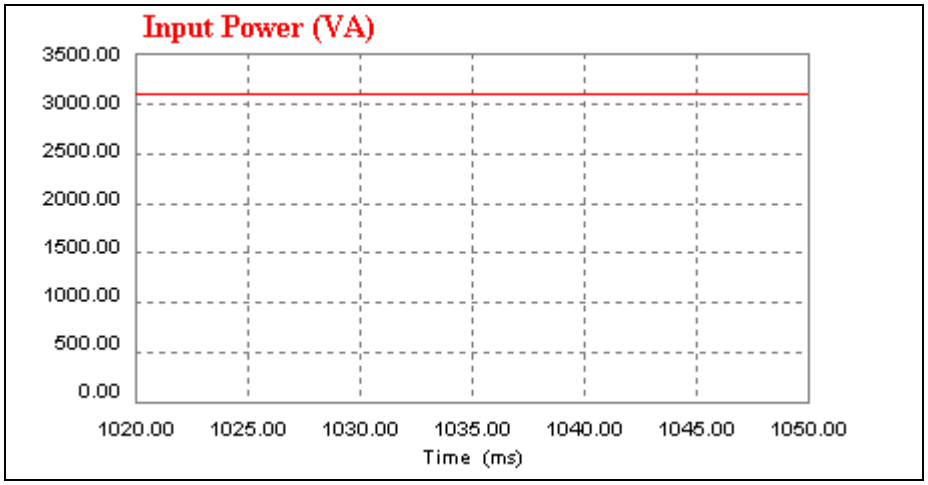

**(a)**



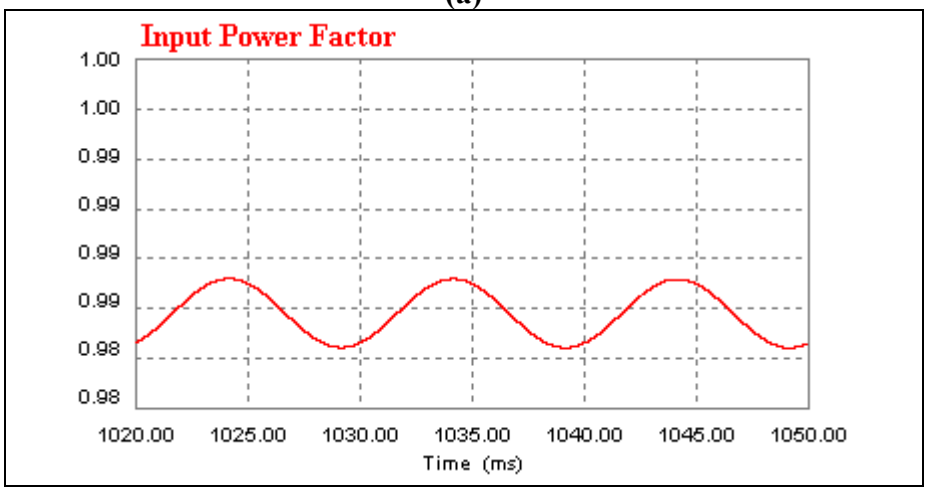

**(b)**

**Figure D.19** (a) Boost diode, D5's current and voltage waveform of classical UPF rectifier with 3 kW inductive-resistive load (100 uH) at steady state, (b) their zoomed version.

### D.2.1.2 Waveforms of Classical Unity Power Factor Rectifier With 3 kW Inductive-Resistive Load (10 uH)

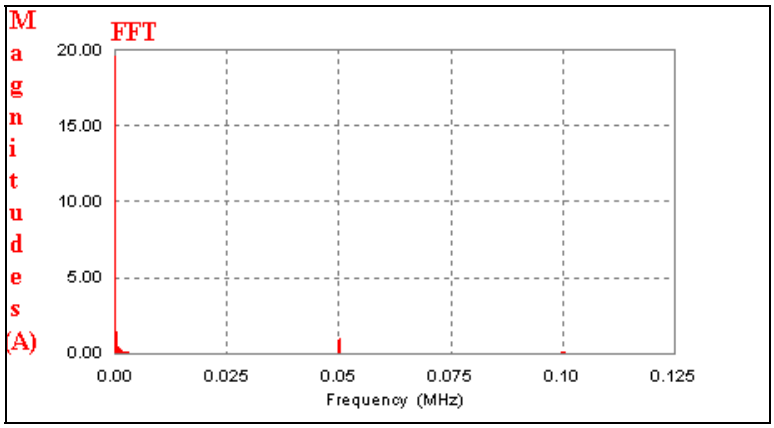



**(a)**

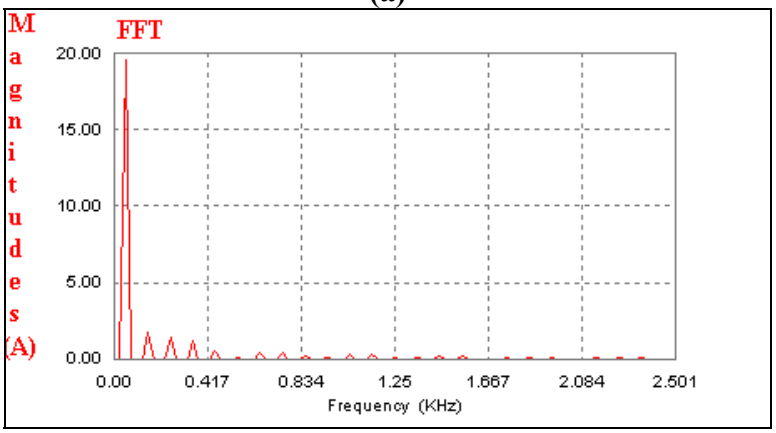



**(b)**

**Figure D.20** Classical unity power factor rectifier's input power and power factor at inductive-resistive 3 kW load (10 uH), (a) its input power, (b) its power factor.




**(a)**




**(b)**

**Figure D.21** (a) FFT waveform of classical unity power factor rectifier's input current at 3 kW inductive-resistive load (10 uH) at steady state, (b) its zoomed version.

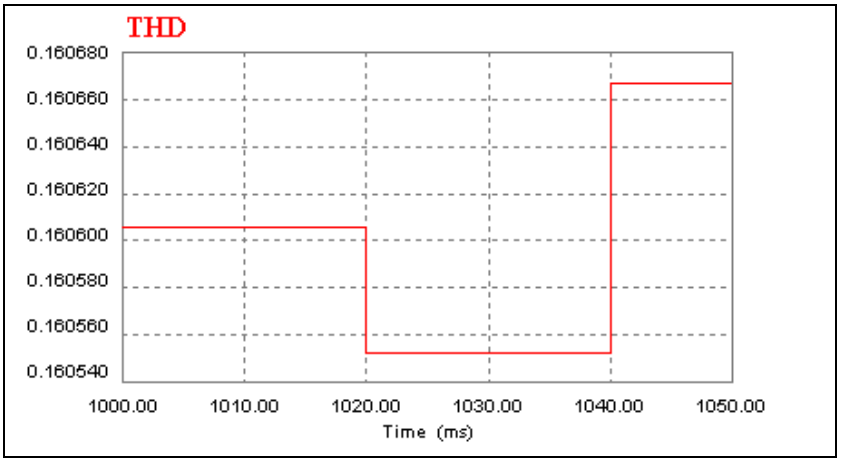
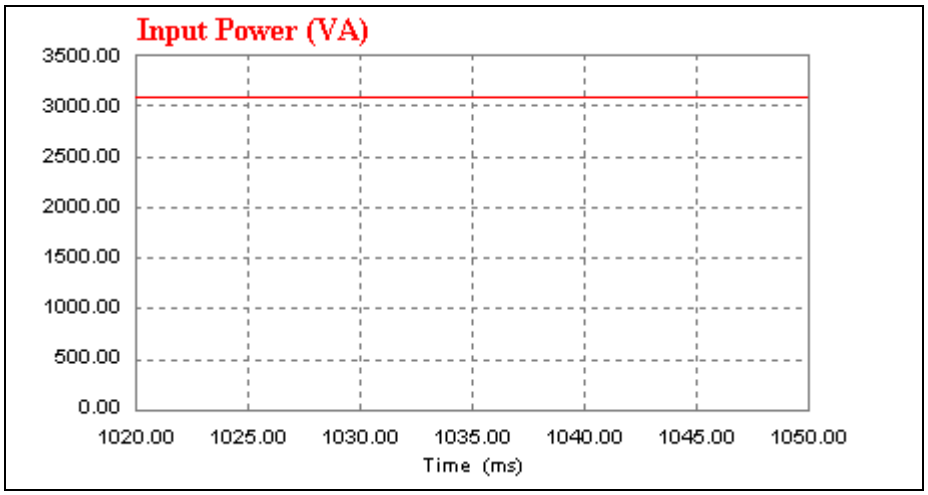


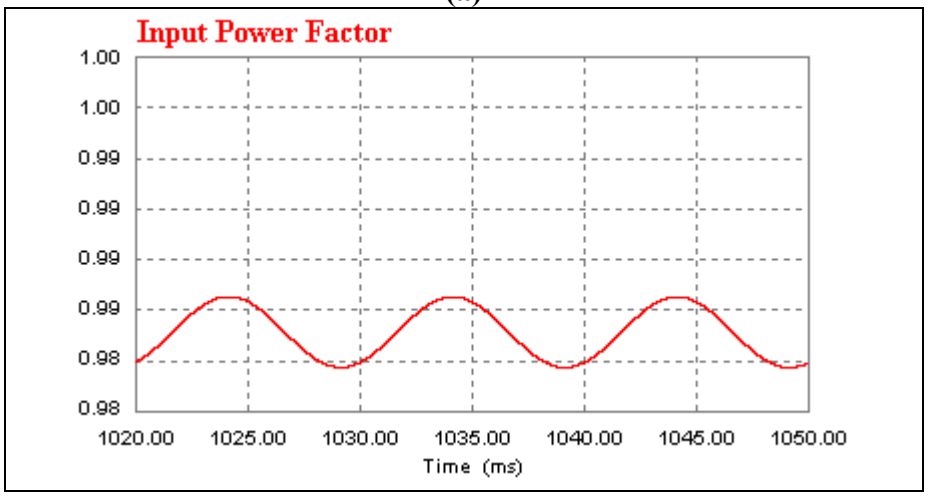

**Figure D.22** THD of classical UPF rectifier's input current at 3 kW inductive-resistive load (10 uH) at steady state.

### D.2.2 Waveforms of Proposed Rectifier With 3 kW Inductive-Resistive Load

#### D.2.2.1 Waveforms of Proposed Rectifier With 3 kW Inductive-Resistive Load (100 uH)

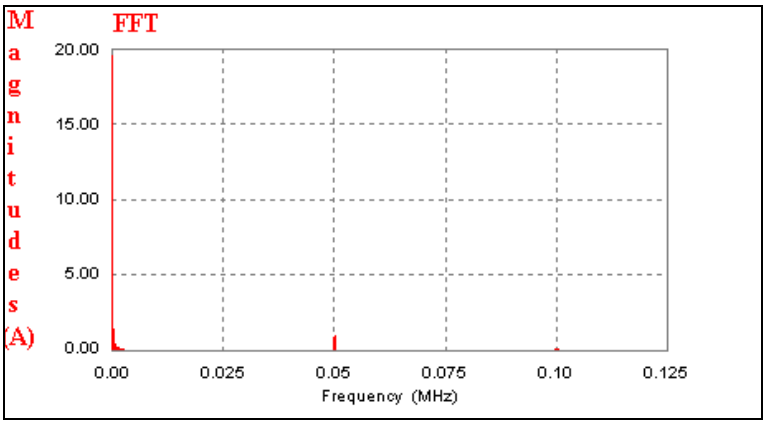



**(a)**

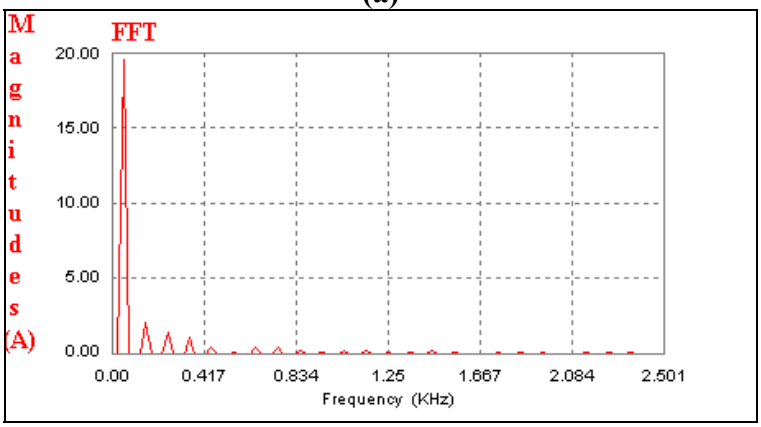



**(b)**

**Figure D.23** Proposed rectifier's input power and power factor at inductive-resistive 3 kW load (100 uH), (a) its input power, (b) its power factor.




**(a)**




**(b)**

**Figure D.24** (a) FFT waveform of proposed rectifier's input current at 3 kW inductive-resistive load (100 uH) at steady state, (b) its zoomed version.

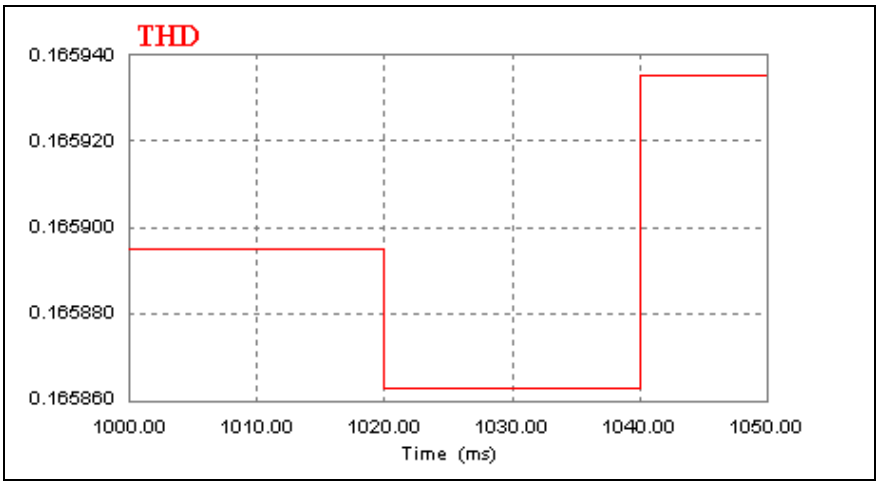
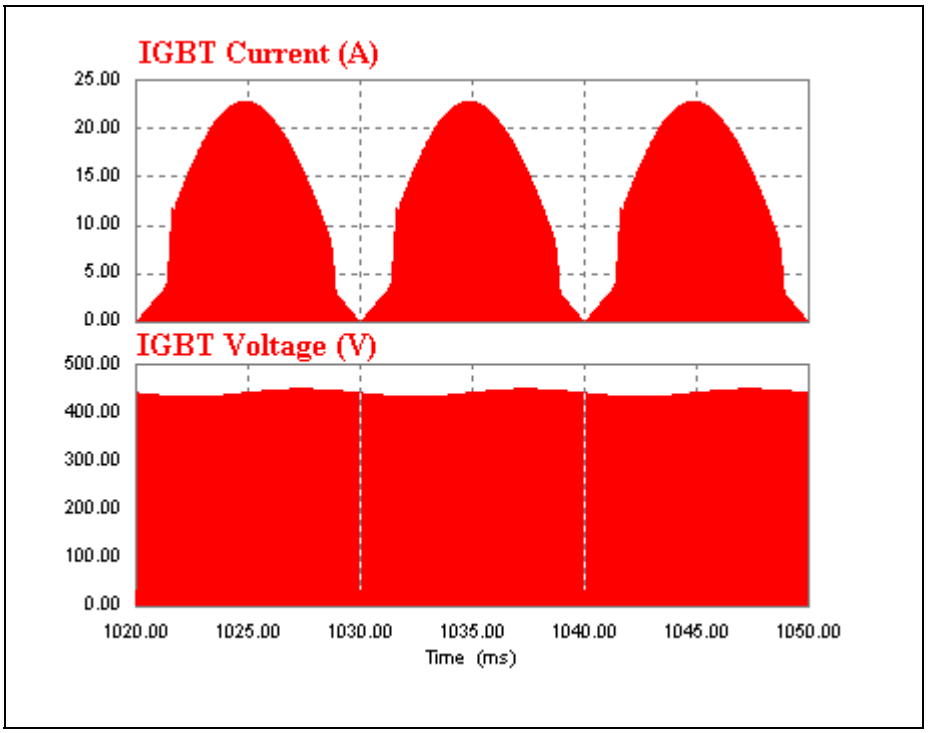
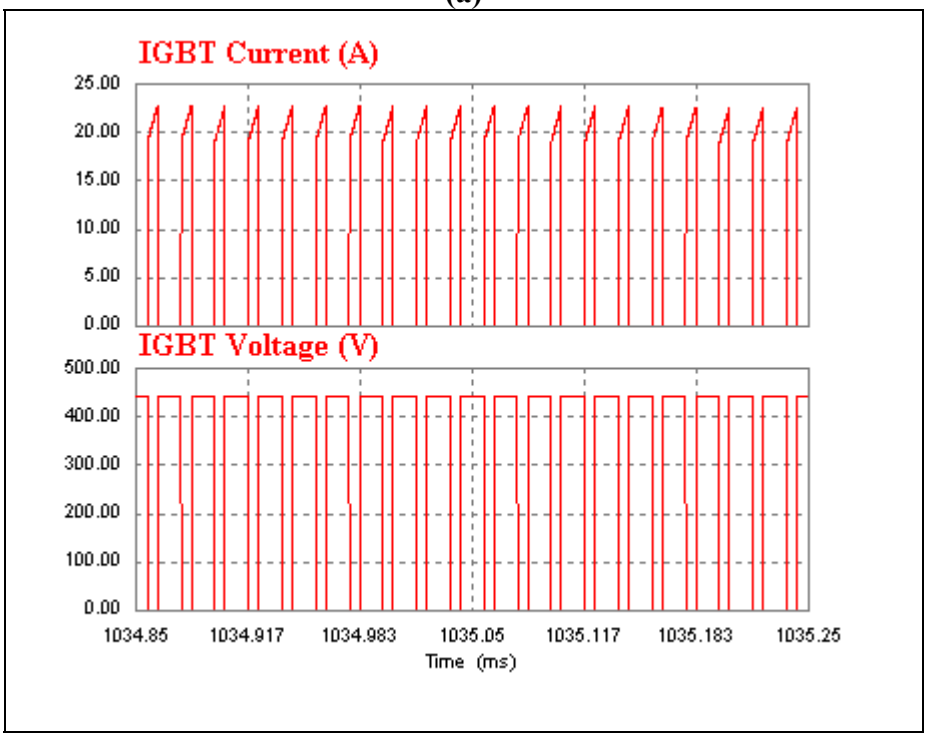



**Figure D.25** THD of proposed rectifier's input current at 3 kW inductive-resistive load (100 uH) at steady state.

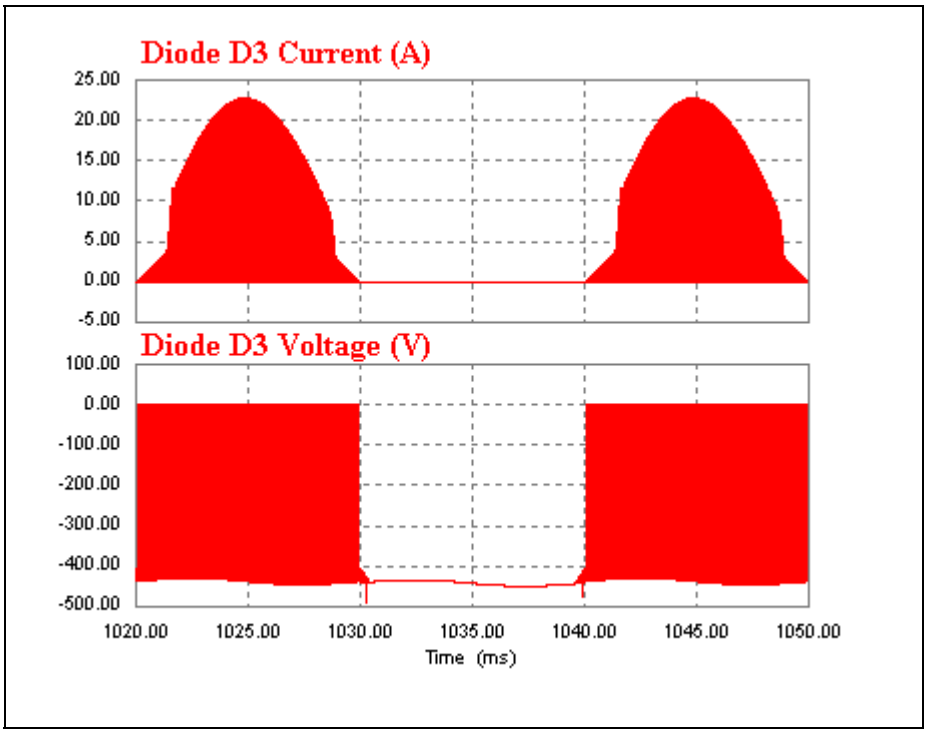



**(a)**

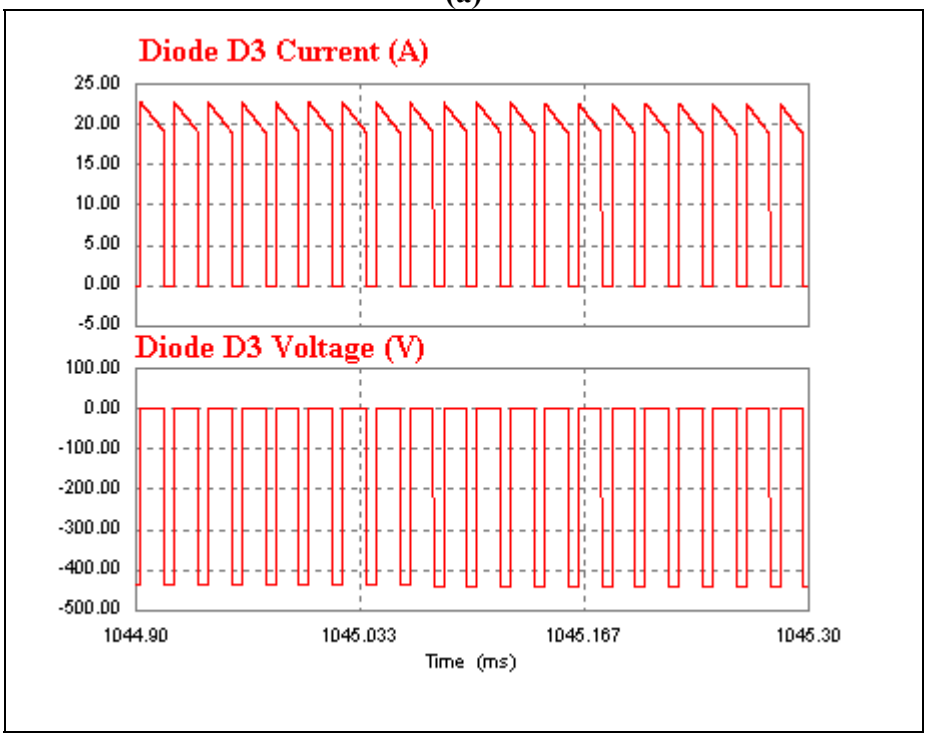



**(b)**

**Figure D.26** (a) IGBT's current and voltage waveform of proposed rectifier with 3 kW inductive-resistive load (100 uH) at steady state, (b) their zoomed versions.

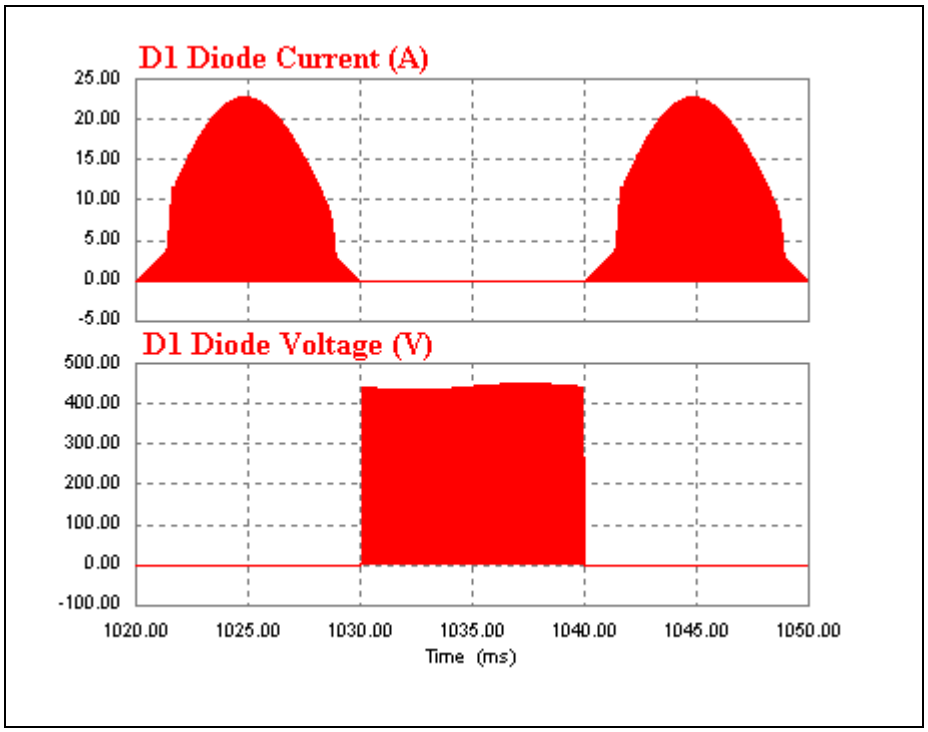



**(a)**

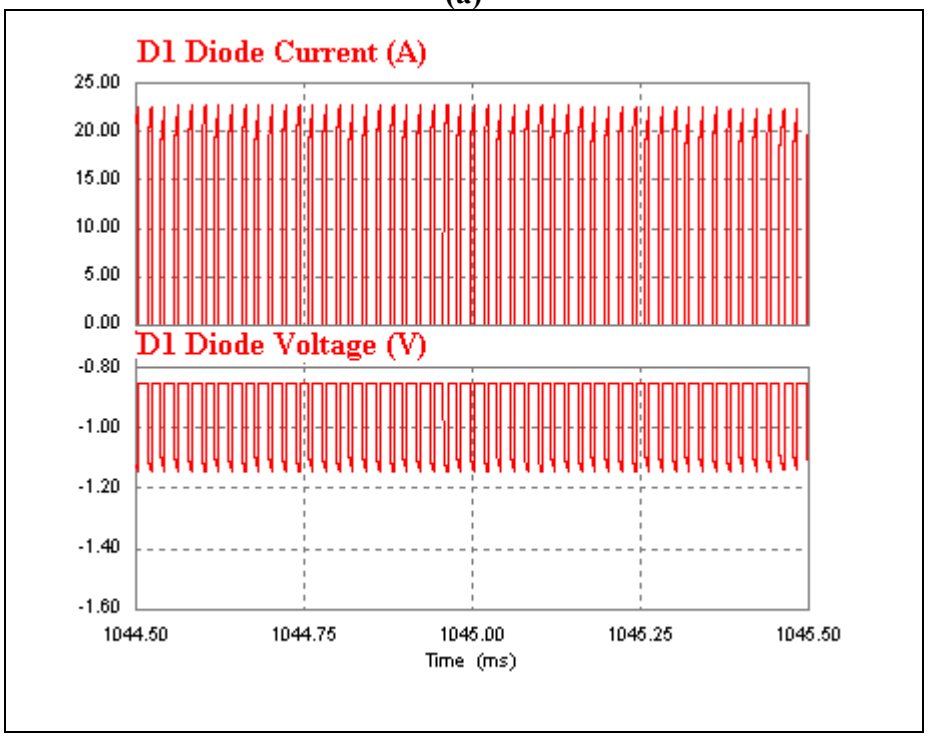



**(b)**

**Figure D.27** (a) One of the boost diodes, D3's current and voltage waveform of proposed UPF rectifier with 3 kW inductive-resistive load (100 uH) at steady state, (b) their zoomed versions.




**(a)**




**(b)**

**Figure D.28** (a) One of the bridge diodes, D1's current and voltage waveform of proposed UPF rectifier with 3 kW inductive-resistive load (100 uH) at steady state, (b) their zoomed versions.

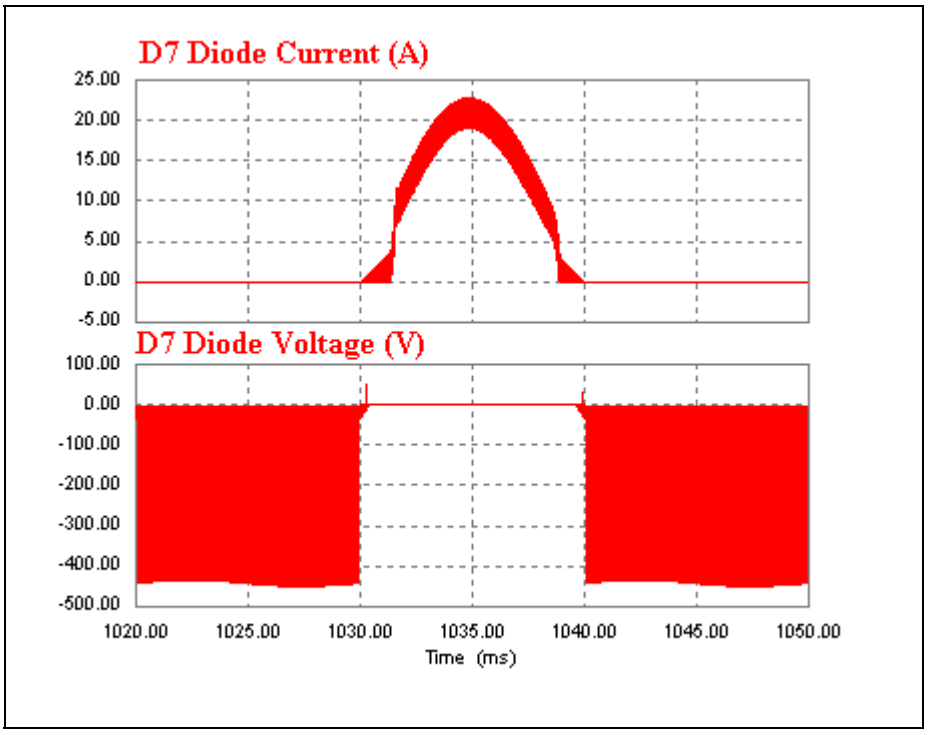
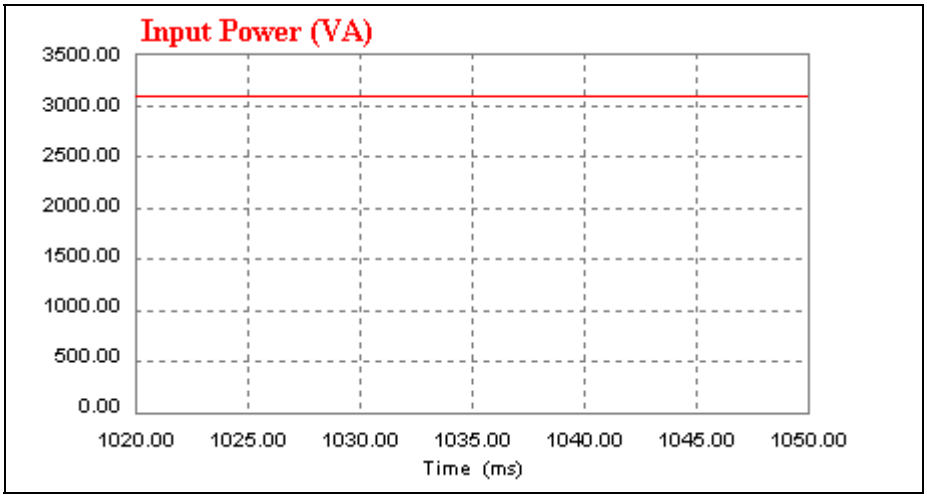
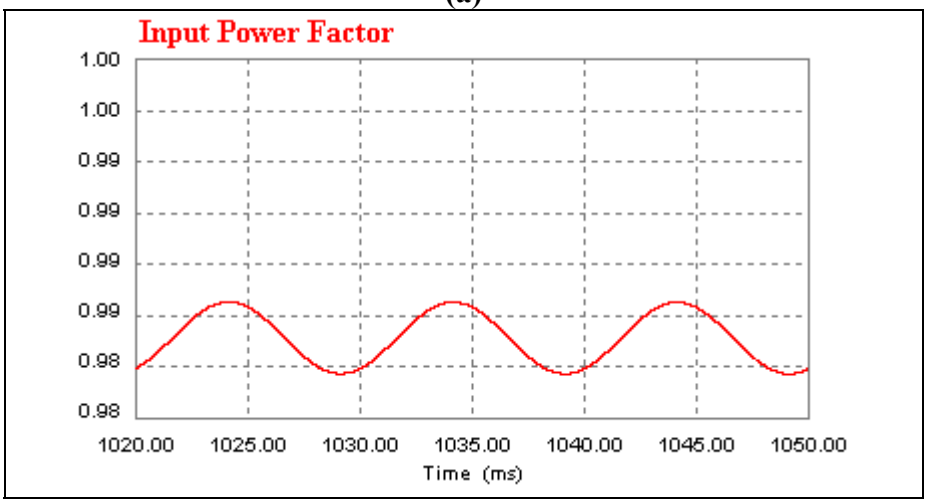



**Figure D.29** One of the bridge diodes, D7's current and voltage waveform of proposed UPF rectifier with 3 kW inductive-resistive load (100 uH) at steady state.

### D.2.2.2 Waveforms of Proposed Rectifier With 3 kW Inductive-Resistive Load (10 uH)

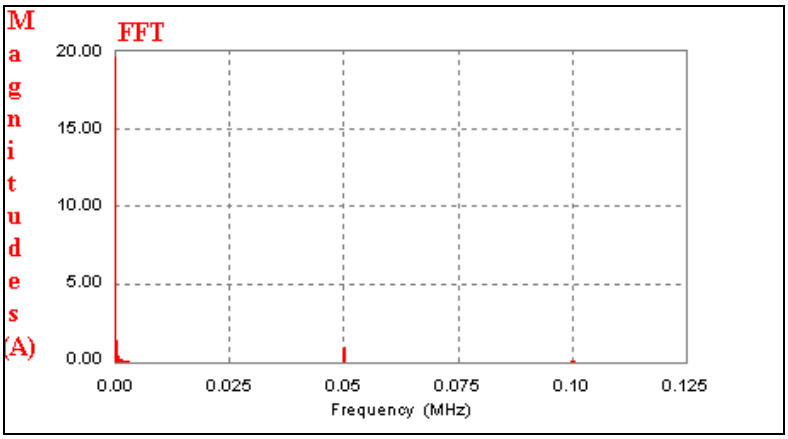



**(a)**

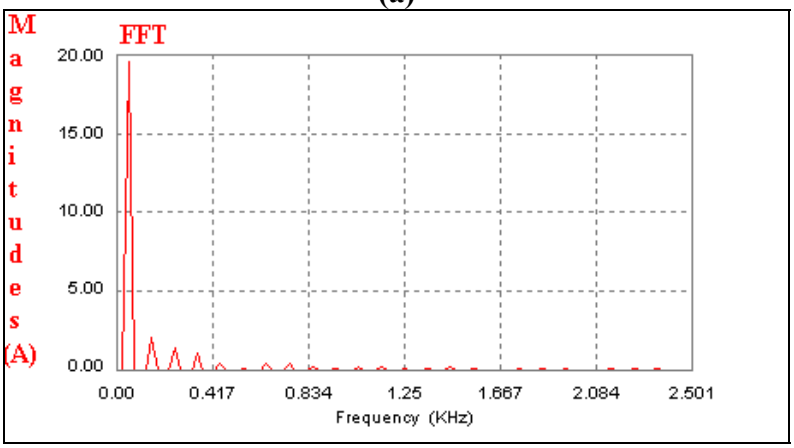



**(b)**

**Figure D.30** Proposed rectifier's input power and power factor at inductive-resistive 3 kW load (10 uH), (a) its input power, (b) its power factor.




**(a)**




**(b)**

**Figure D.31** (a) FFT waveform of proposed rectifier's input current at 3 kW inductive-resistive load (10 uH) at steady state, (b) its zoomed version.

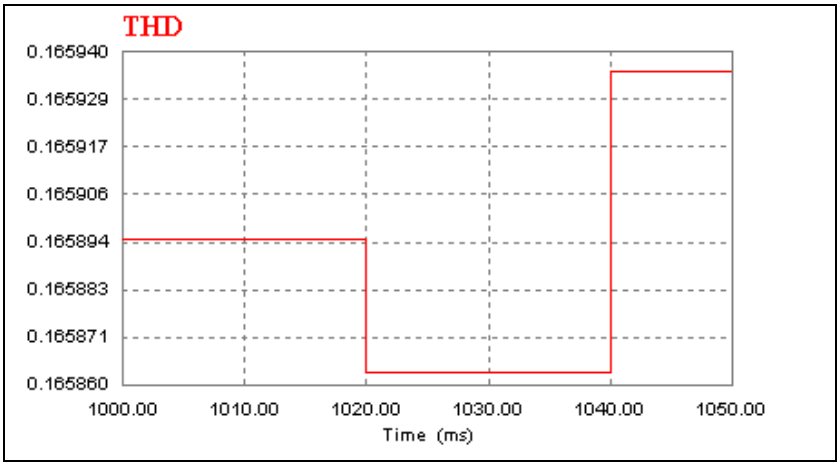
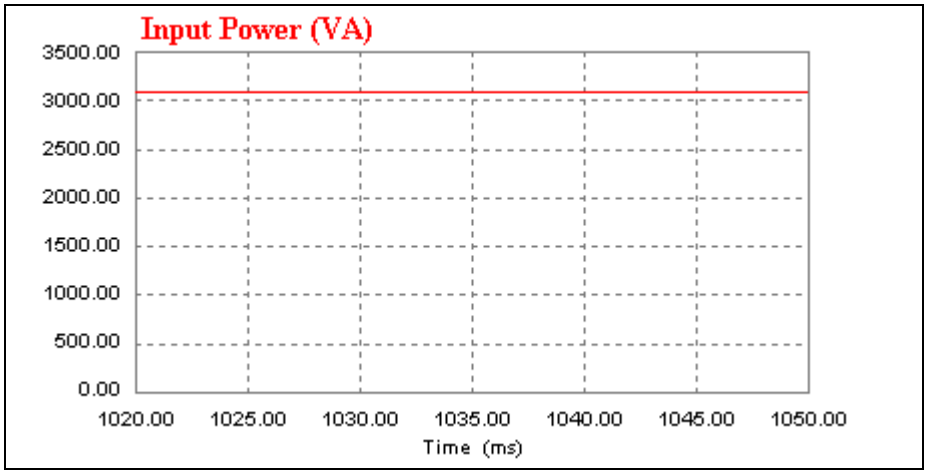
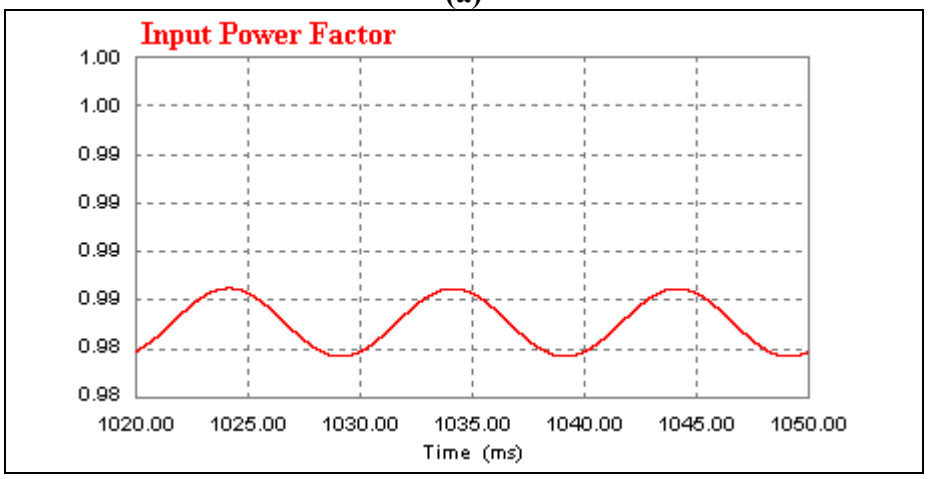



**Figure D.32** THD of proposed rectifier's input current at 3 kW inductive-resistive load (10 uH) at steady state.

**D.3 Waveforms of Classical Unity Power Factor Rectifier With 3 kW Inductive-Resistive Load By Taking Reference Voltage From A Transformer Connected To Mains Supply**

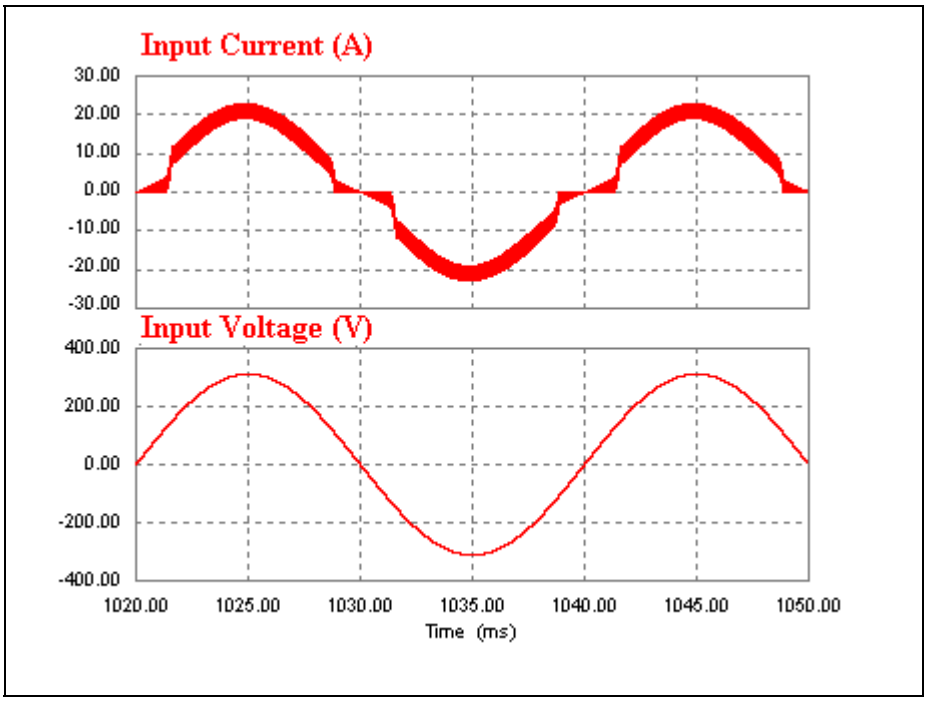



**(a)**

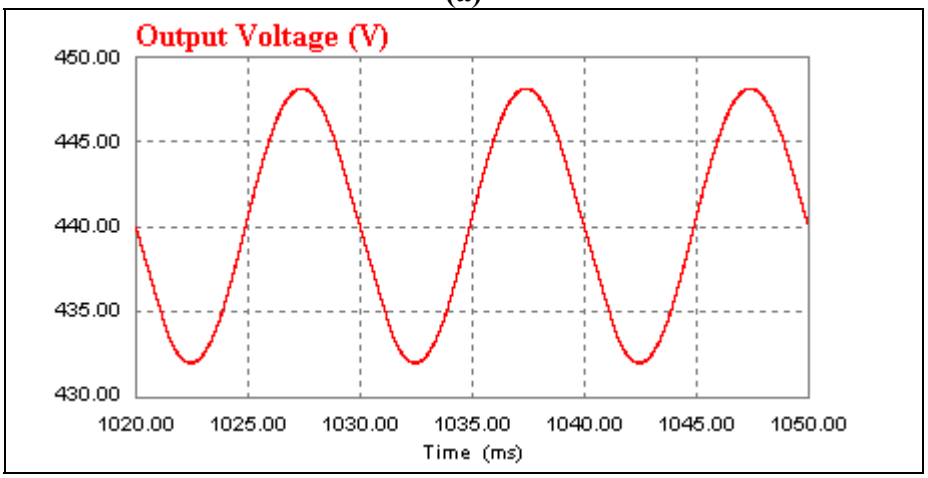



**(b)**

**Figure D.33** The classical unity power factor rectifier's input power and power factor with 3 kW purely resistive load by taking reference voltage from a transformer connected to mains supply, (a) the rectifier's input power (b) its power factor.

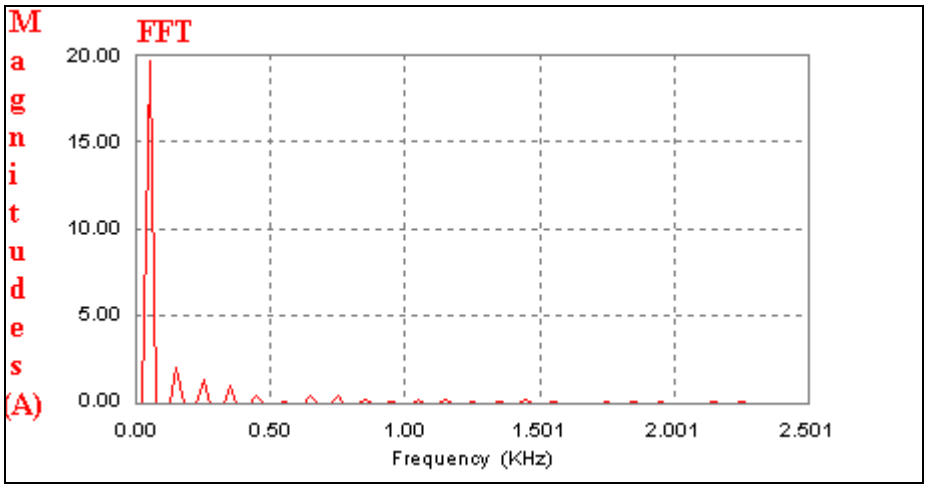



**(a)**

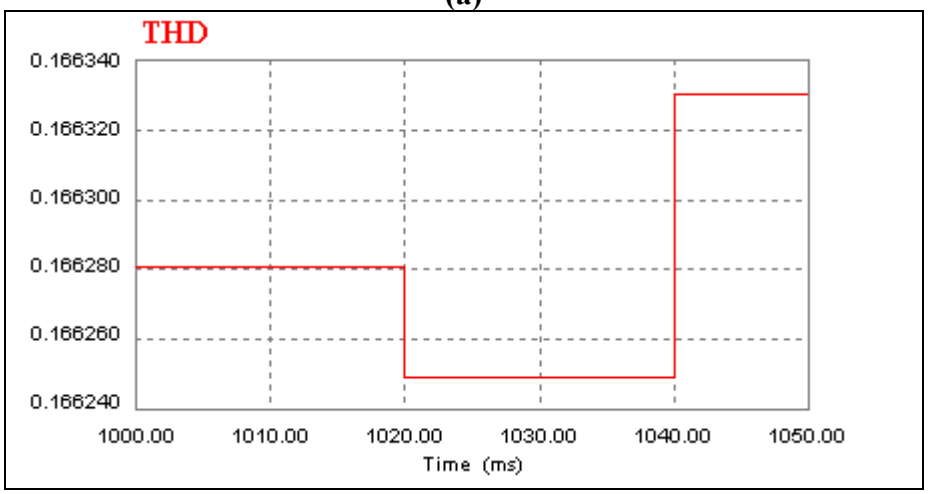



**(b)**

**Figure D.34** The classical unity power factor rectifier's input current and voltage waveform, and its output voltage waveform with 3 kW purely resistive load by taking reference voltage from a transformer connected to mains supply, (a) its input voltage and current waveform, (b) its output voltage.




**(a)**




**(b)**

**Figure D.35** The classical unity power factor rectifier's input current FFT and THD graph obtained with 3 kW purely resistive load by taking reference voltage from a transformer connected to mains supply, (a) its FFT waveform (b) its THD graph.

## APPENDIX E: Classical UPF Rectifier And Proposed Rectifier's PCB

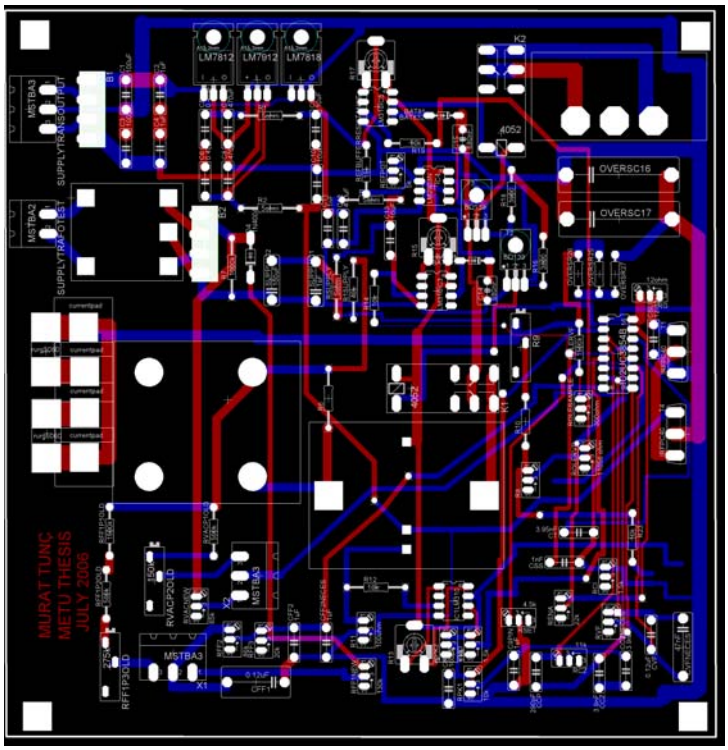



**Figure E.1** Classical unity power factor rectifier and proposed rectifier's printed circuit board.

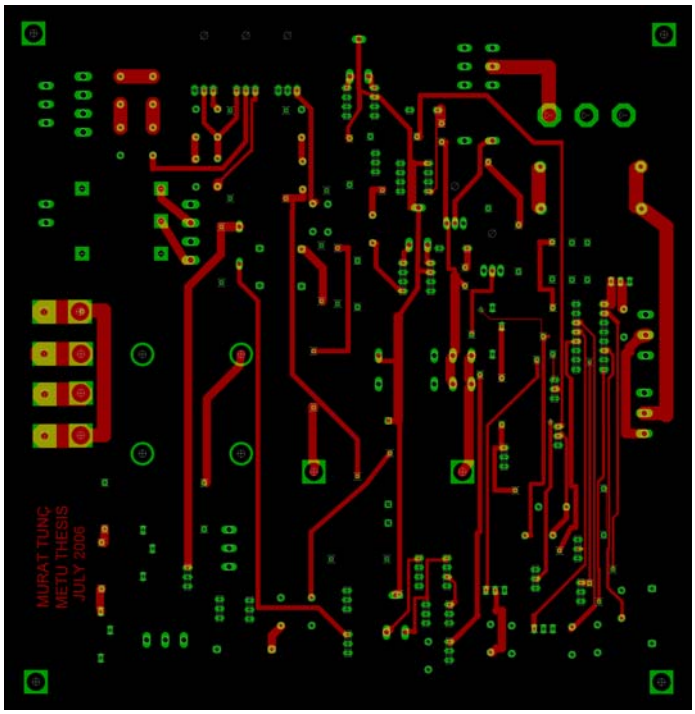



**Figure E.2** Classical unity power factor rectifier and proposed rectifier's printed circuit board's top layer.

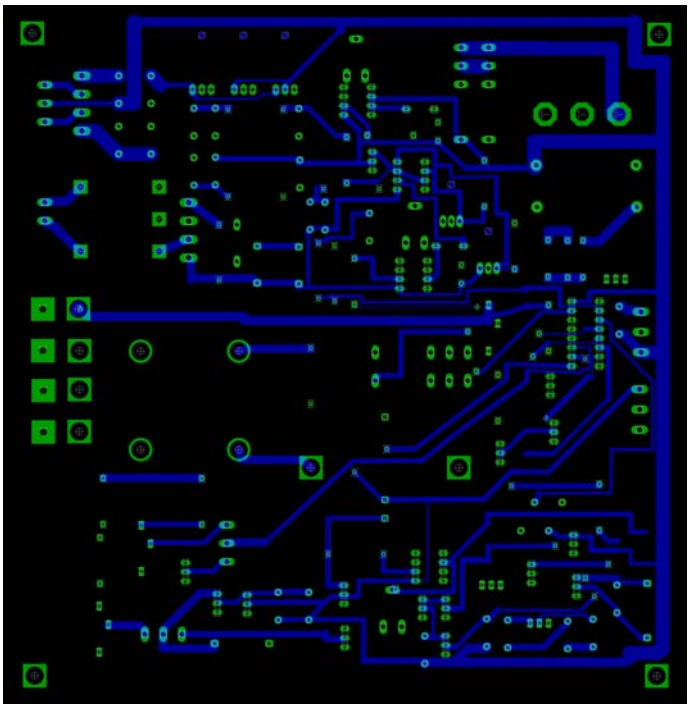


**Figure E.3** Classical unity power factor rectifier and proposed rectifier's printed circuit board's bottom layer.