DEEP-TRENCH RIE OPTIMIZATION
FOR
HIGH PERFORMANCE MEMS MICROSENSORS

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ABSTRACT

DEEP-TRENCH RIE OPTIMIZATION FOR HIGH PERFORMANCE MEMS MICROSENSORS

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This thesis presents the optimization of deep reactive ion etching process (DRIE) to achieve high precision 3-dimensional integrated micro electro mechanical systems (MEMS) sensors with high aspect ratio structures. Two optimization processes have been performed to achieve 20 µm depth for 1 µm opening for a dissolved wafer process (DWP) and to achieve 100 µm depth for 1 µm opening for silicon-on-glass (SOG) process. A number of parameters affecting the etch rate and profile angle are investigated, including the step times, etch step pressure, platen power, and electrode temperature.

Silicon etch samples are prepared and processed in METU-MET facilities to understand and optimize the DRIE process parameters that can be used for the production of MEMS gyroscopes and accelerometers. The etch samples for DWP are masked using a photoresist, Shipley S1813. After the optimization process, vertical trench profiles are achieved with minimum critical dimension loss for trench depths up to 20 μm. Since the selectivity of the resist is not sufficient for 100 μm-deep trench etch process, silicon dioxide (SiO_2) is used as the mask for this process. At the end of the optimization processes, more than 100 μm depth for 1 μm opening with almost vertical sidewalls are achieved. In summary, this study provides an extensive understanding of the DRIE process for successful implementations of integrated MEMS sensors.

Key words: Deep Reactive Ion Etching (DRIE), Micro Electro Mechanical Systems (MEMS), Anisotropic Dry Silicon Etching.

ÖZ

YÜKSEK PERFORMANSLI MEMS DUYARGALARI İÇİN DERİN-KUYU RIE OPTİMİZASYONU

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Bu tez yüksek boy-en oranına sahip 3 boyutlu MEMS duyargaları elde etmek için derin kuyu alındırma tekniğinin optimizasyon çalışmalarını sunmaktadır. 2 ayrı uygulama için optimizasyon yapılmıştır. Bunlar, aşındırılmış pul silisyum mikro işleme sürecinde kullanılmak üzere 1 mikrometre genişliğindeki kanalların 20 mikrometre derinliğe indirilmesi ve ileriki çalışmalarda kullanılmak üzere 1 mikrometre genişliğindeki kanallarda 100 mikrometre derinlik elde edilmesidir. Silikon aşındırma hızını ve kanal profil açısını etkileyen adım süreleri, aşındırma

adımı basıncı, uygulanan besleme gücü ve silicon pulun sıcaklığı incelenmiştir. MEMS dönüölçer ve ivme ölçer üretiminde kullanılabilecek derin kuyu aşındırma süreci parametrelerinin optimizasyon çalışmalarında kullanılan silicon pullar ODTÜ – MET tesislerinde hazırlanmış ve yine bu tesislerde başarı ile üretilmişlerdir. Aşındırılmış pul silicon mikro işleme için hazırlanan desen aşındırılacak silicon pullara fotoresist, S1813, kullanılarak tek maske ile aktarılmıştır. Fotoresistin seçiciliği 100 mikron denemesi için yeterli olmayacağından dolayı maske olarak silikondioksit, (SiO_2), kullanılmıştır. Bu çalışmada dike yakın yan duvarlar ile 100 mikrondan fazla derinliğe ulaşılmıştır. Özetle, bu çalışma entegre MEMS duyargaları için başarılı derin kuyu aşındırma süreci uygulamasını geniş bir çerçevede anlatmaktadır.

Anahtar Kelimeler: Derin kuyu aşındırma, mikro elektro mekanik sistemler (MEMS), Anizotropik kuru silikon aşındırma.

To My Family

and

To My Love, Ayşe Gül

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CHAPTER 1

INTRODUCTION

Micro Electro-Mechanical Systems combine electrical and mechanical systems together with the overall size and critical dimensions ranging from millimeter to sub-micrometer scales [1].

The rapid growth of the MEMS during the last decade is due to the achievement of high volume production with low unit cost. In addition to the economical benefits, distinctive capabilities can also be achieved such as sensors, actuators, and biomedical devices [2, 3]. The MEMS technology has a wide range of application areas in all aspects by means of automotive, defense, biomedical, and scientific applications. Accelerometers, gyroscopes, optical devices, pressure, and flow sensors are the examples of the MEMS devices. These devices are designed for sensing mechanical, thermal or optical variations and response is given on the macro scale [4]. Mostly, the electronic signal processing circuitry is also produced together with the sensor providing the benefits of fully integrated systems.

The development of the MEMS devices includes the techniques of integrated circuit (IC) fabrication technology including thin-film growth, doping, lithography, and etching processes [5]. One of the important MEMS process for etching is deep reactive ion etching (DRIE) process of silicon substrate and there is a need for optimization of this process to achieve high aspect ratio structures with smooth

sidewalls, high selectivity to masking material, and good profile control across the wafer.

This thesis presents the optimization studies for the DRIE process for obtaining deep trenches with vertical sidewalls and high aspect ratios. The system used for optimizing the process is from the Surface Technology Systems (STS) called as Advanced Silicon Etching (ASE) which is based on the standard Bosch process. Several parameters affecting the process are investigated, including the individual etch and passivation step times, etch step pressures, coil and platen power, and the electrode temperature. Silicon etch samples are produced in METU-MET facilities to understand and optimize the effects of DRIE process parameters that can be used for development of accelerometers and gyroscopes.

This study has allowed understanding and successful implementation of DRIE process at Middle East Technical University.

This chapter is organized as follows: Section 1.1 explains the MEMS fabrication techniques to give information about MEMS processing including wet and dry etching. Section 1.2 describes the etching process including, wet and dry etching. It underlines the DRIE process. Section 1.3 gives some examples of sensors that include the DRIE processing. Section 1.4 concludes this chapter with the research objectives and thesis organization.

1.1. MEMS Fabrication Techniques

MEMS fabrication techniques are mainly based on the techniques of IC fabrication technology [5]. The major steps are thin-film growth, doping, lithography, and

etching processes. In the following part, these techniques are briefly explained. Figure 1.1 shows the major steps of integrated circuit technology.

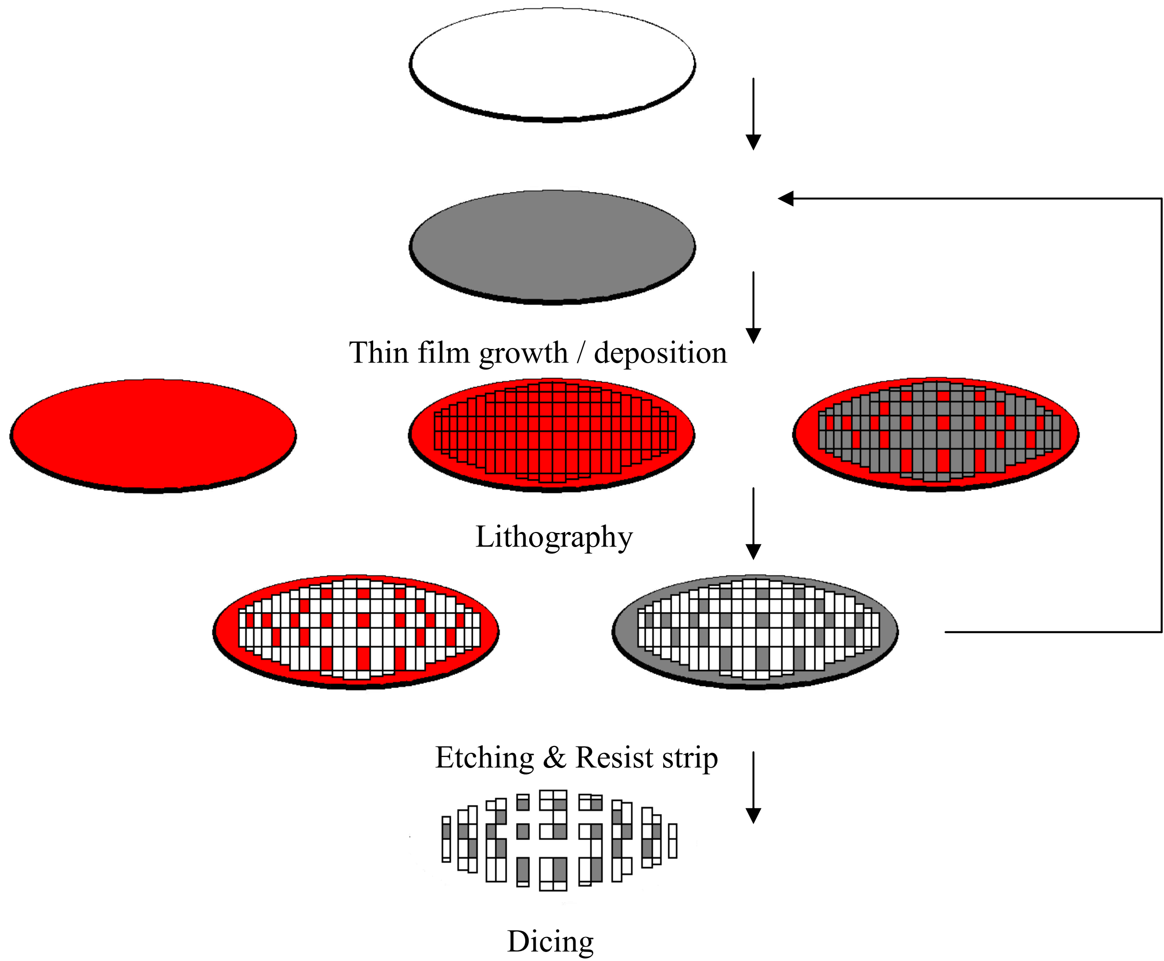


Figure 1.1: Major processing steps in integrated circuit fabrication.

1.1.1. Thin Film Growth

Thin film grown on a polished silicon wafer is a widely used technique for the MEMS technology. These growth films are used for providing conducting regions within the device, electrical insulation between metals, or protection from the environment [6].
Silicon dioxide (SiO_2), silicon nitride (Si_3N_4), polycrystalline silicon (polysilicon), and metals are the most widely used thin films. The most common deposition methods are atmospheric-pressure chemical vapor deposition (CVD), low-pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), and sputtering [7,8].

Silicon dioxide films are mostly used for passivating the silicon surface or as a masking material for diffusion, ion implantation, and etching or sometimes used as a sacrificial layer. Silicon nitride is used for passivating silicon devices, as a mask for selective oxidation, or as a sacrificial layer. Metal films are mostly used for generating interconnections, ohmic contacts, and rectifying metal-semiconductor contacts, deposited by evaporation, sputtering or electro plating [6].

1.1.2. Doping

Changing the electrical properties of the semiconductor is accomplished by introducing impurity atoms into the layer. This process is called doping and is accomplished by either thermal diffusion or ion implantation [9].

To make the silicon n-type, it is doped with an impurity atom of five valence electrons. Since silicon has four valence electrons, one of the electrons coming from the impurity atom will be free. As a result, the number of free charge carriers, i.e.,

electrons, will be increased. On the other hand, making silicon p-type is accomplished by doping it with an atom which has three valence electrons. This will increase the number of free charge carriers, holes. Figure 1.2 shows the illustration of p- and n-type doped silicon atoms.

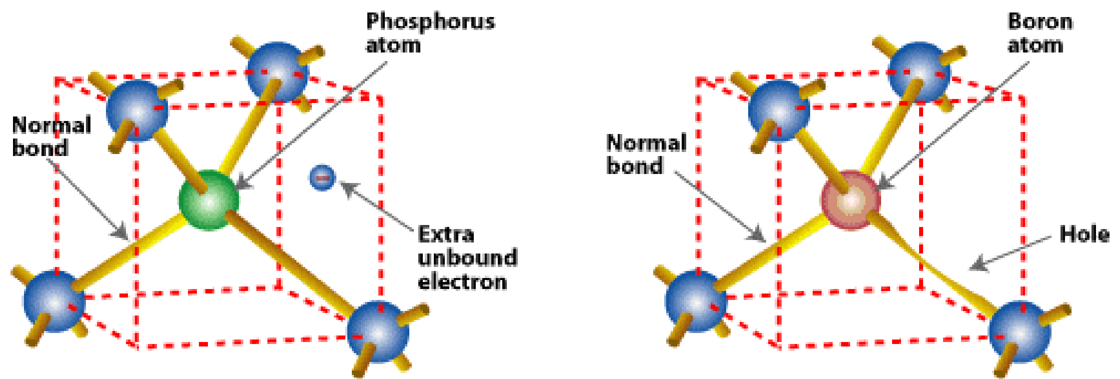


Figure 1.2: Illustration of p and n type doped silicon atoms [10].

1.1.3. Lithography

Lithography is the process of transferring the pattern on a mask to a growth film or a substrate surface by exposing a photosensitive polymer film through a mask [6].

Transferring the pattern starts with dehydration and priming of the substrate surface to improve the adhesion of the polymer. Then, the photosensitive polymer film is coated on the surface of the wafer. In order to reduce the retained solvent level and densify the film, it is softbaked. After that it is exposed to radiation through the mask. It is followed by the chemical development of the photosensitive film by which either the exposed or non-exposed parts removed depending on the type of the polymer. At this step the mask pattern is completely transferred to the photosensitive

film. Optionally, the polymer film can be hardbaked for further crosslinking of the polymer in order to further harden the photoresist and improve its adhesion to the surface. Figure 1.3 shows the illustration of transferring the pattern from mask to the positive photoresist by the photolithography technique.

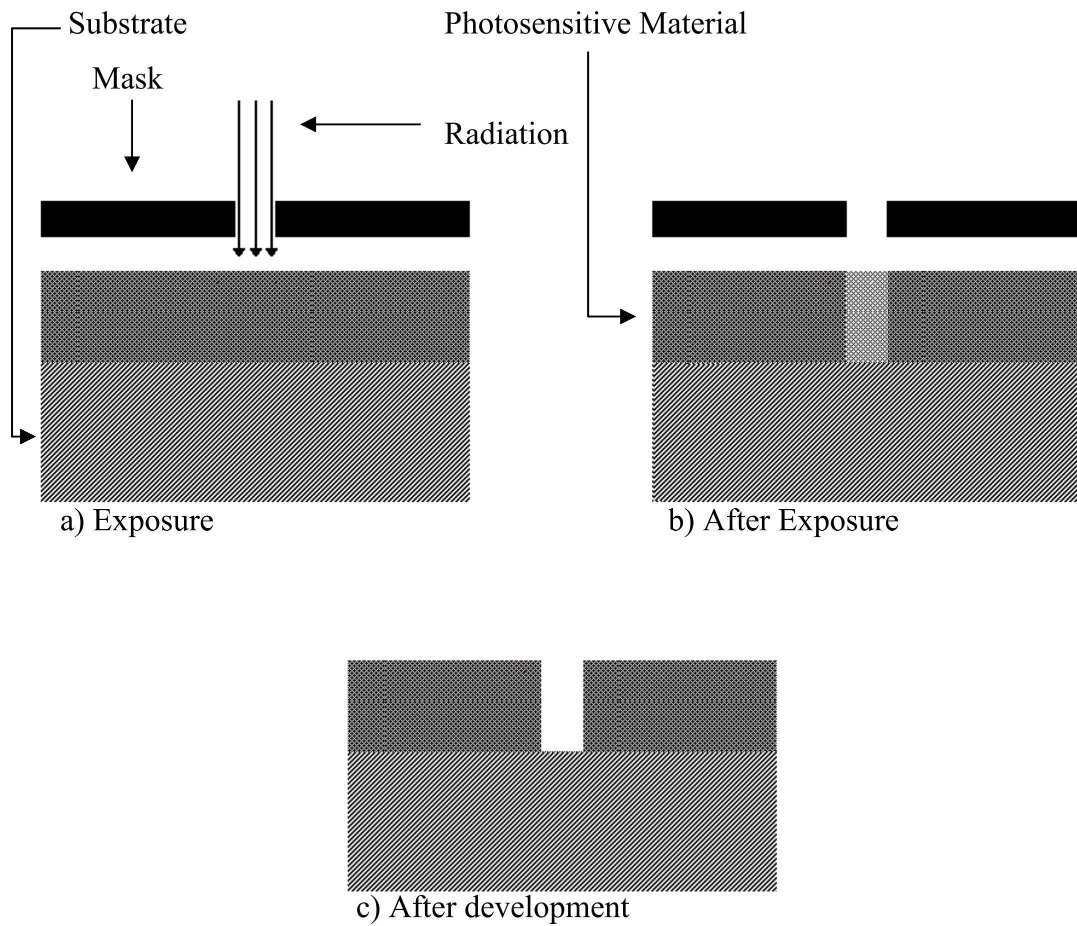


Figure 1.3: Illustration of transferring the pattern from mask to the positive photoresist by photolithography technique.

1.1.4. Etching

After transferring the mask pattern to the polymer, the underlying material can be etched through the openings on the patterned polymer mold [11]. Semiconductors, metals, and insulators can all be etched with the appropriate enchants. Etching can be categorized into two major groups, wet and dry etching.

In wet etching processes liquid chemicals are used to etch the desired material. It can also be etched by electrochemical process with a source of current, photochemical process with a source of light or photoelectrochemical processes a source of both current and light [12]. Generally, wet etching is an isotropical etching process, but depending on the crystallographic preferences of the chemical enchants, substrate can also be etched anisotropically.

In dry etching process the etchant is transferred into the gaseous or plasma phase. There are different types of dry etching processes, including sputter etching, plasma etching, reactive ion etching (RIE), and DRIE [6].

1.1.5. Surface and Bulk Micromachining

Surface micromachining is the fabrication of micromechanical structures from the deposited thin films. Substrate wafer is primarily used as a mechanical support on which multiple of structural and sacrificial layers are deposited and patterned to define mechanical, optical, physical, etc. properties of the structure [13]. Depositing and selectively removing the thin film allow building three-dimensional structures on a planar substrate.

In surface micromachined MEMS devices the patterned layers are used to produce electromechanical elements or as sacrificial layers to make the mechanical layers movable. Figure 1.4 shows an example of a surface micromachining process flow.

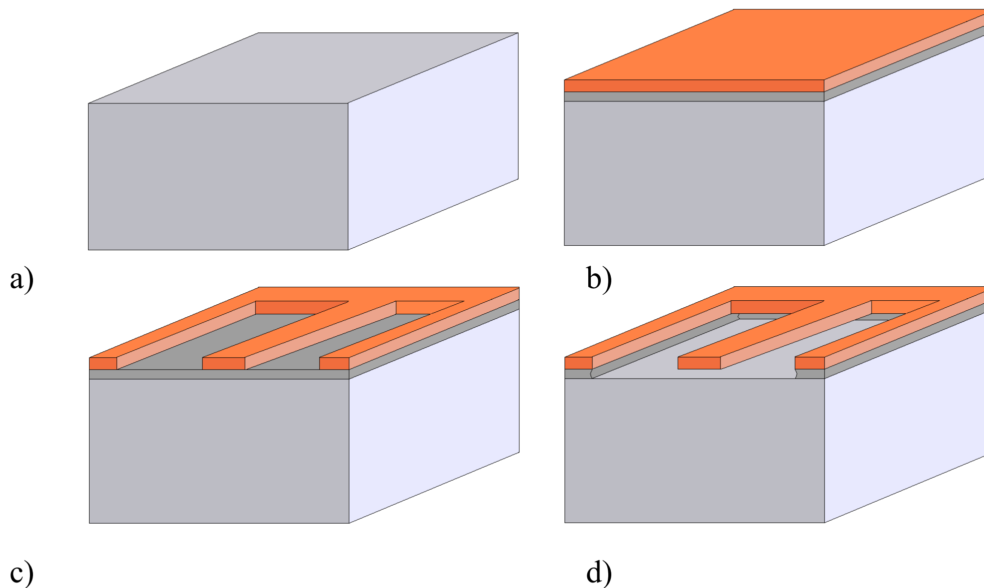


Figure 1.4: Schematic demonstration of surface micromachining. (a) Silicon substrate, (b) deposition of sacrificial layer and photoresist, (c) structural layer patterning, and (d) free-standing microstructure after etching.

Bulk micromachining is another widely used technique for the production of micromachined sensors, actuators, and structures by selectively removing the silicon from substrates [8]. It involves etching features directly into silicon or other substrates for the fabrication of 3D structures. Figure 1.5 shows an example of a bulk micromachined process flow.

For selectively removal of the substrate, different wet and dry etching methods are available, depending on the requirements such as anisotropy, selectivity, etch rate, and safety.

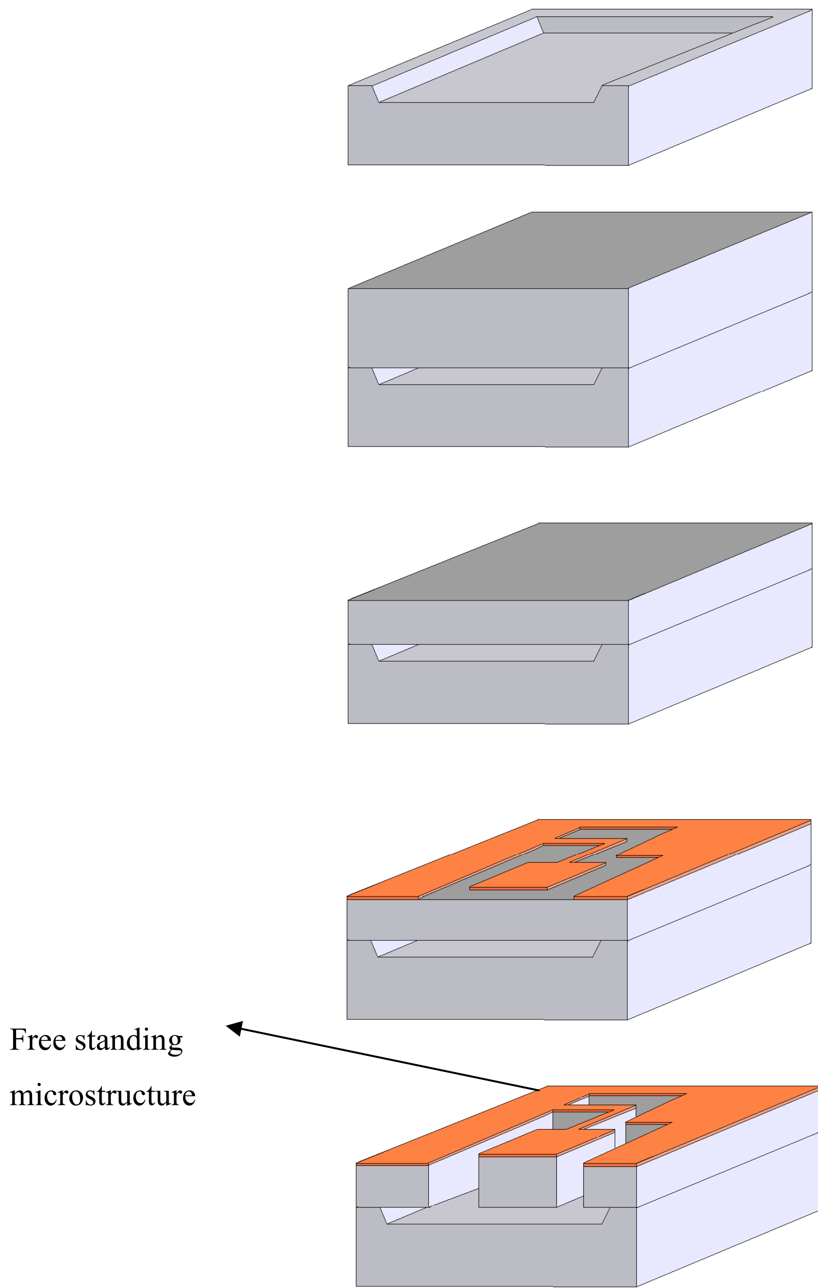


Figure 1.5: Schematic diagram of bulk micromachining.

Using silicon substrate as bulk allows production of larger and particularly deeper features than the ones fabricated in surface micromachining. This is an important consideration in MEMS where higher mechanical power or force levels are desired. Table 1.1 shows the comparison of the most common silicon etchants used in bulk micromachining.

Table 1.1: Comparison of the most common silicon etchants used in bulk micromachining [14].

	TMAH	**EDP**	**XeF_2**	**DRIE**	**KOH**
Etch Type	Wet	Wet	Dry	Dry	Wet
Si Etch Rate µm/min	0.02 - 1	≈ 1	1 - 3	> 1	1 – 2
Anisotropic?	Yes	Yes	No	Yes	Yes
p++ Etch Stop	Yes	Yes	No	No	Yes
Electrochemical Stop	Yes	Yes	No	No	Yes
Cost	Moderate	Moderate	Moderate	High	Low
Disposal	Difficult	Moderate	N/A	N/A	Easy
Safety	Low	High	Moderate	High	Moderate

Surface micromachining requires more fabrication steps than bulk micromachining, and hence is more expensive. However, with this technique, it is possible to create much more complicated. So surface micromachining is suitable for applications requiring more sophisticated mechanical elements [15].

However, surface micro-machining is typically limited to layers of thicknesses about several microns, which restricts the ability to create devices which can deliver significant mechanical forces or power levels or to define channels or cavities for fluidic, chemical or biological applications [16].

1.2. Etching

In order to give functionality to MEMS structure on a substrate, it is necessary to etch the patterned thin films or the substrate itself. In general, there are two classes of etching processes; wet etching where the material is dissolved when immersed in a chemical solution and dry etching where the material is sputtered or dissolved using reactive ions or a vapor phase etchant. In the following sections, wet and dry etching techniques and the differences of these techniques are briefly explained.

1.2.1. Wet Etching

In wet etching, liquid chemicals or etchants are used to remove the materials, defined by the photoresist mask on the wafer. Wet etching can be categorized into two groups according to their etching velocities in directions along different orientations; isotropic and anisotropic etching methods. Isotropic etchants attack the material being etched at the same rate in all directions. On the other hand, anisotropic etchants attack in a certain direction, depending on the crystallographic structures [12].

Advantages of wet etching are its low cost with respect to dry etching systems, its high reliability and excellent selectivity in most cases with respect to both mask and substrate materials. On the other hand, it has the disadvantages of limited resolution, higher safety risks due to the direct chemical exposure of the personnel, incomplete or non-uniform etching [17]. Figure 1.6 shows the illustrations of isotropical and anisotropical etching.

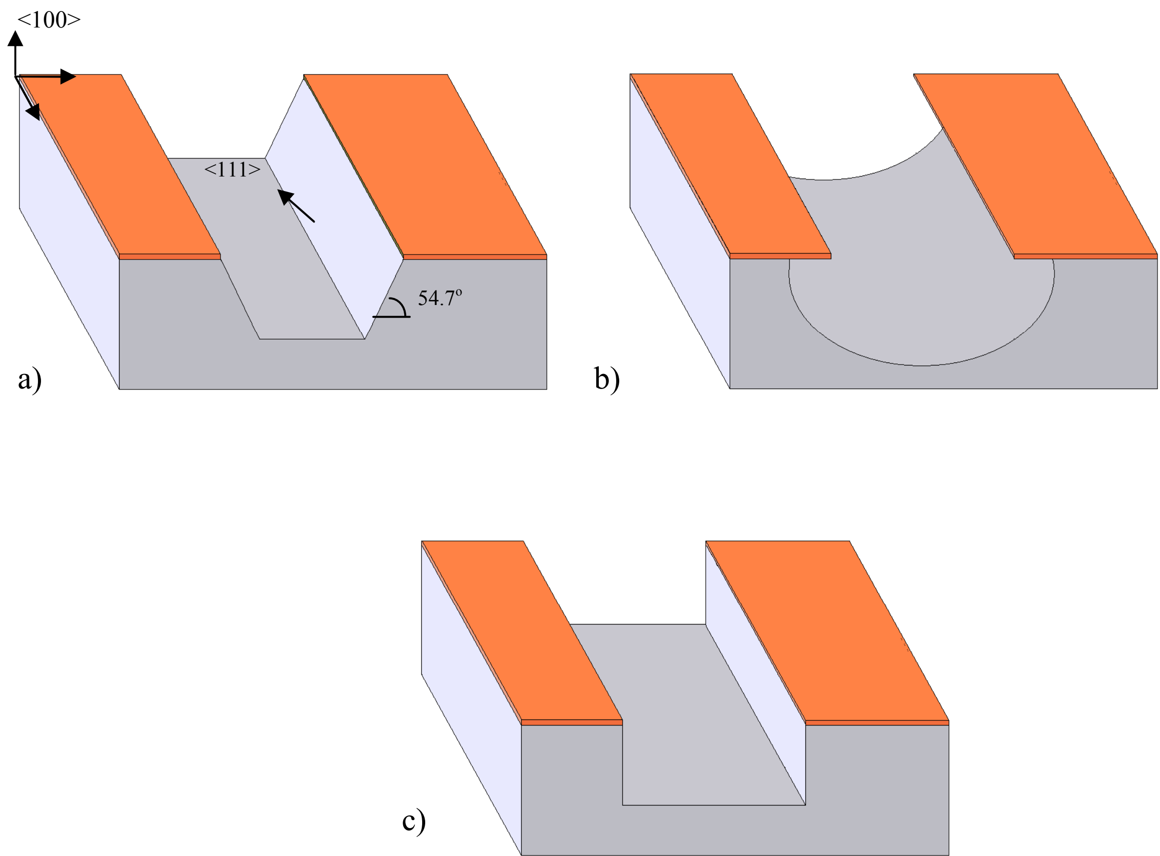


Figure 1.6: Illustrations of a) crystal orientation dependent anisotropic etching, b) isotropical etching, and c) anisotropical etching.

1.2.2. Dry Etching

Dry etching is a process that does not employ any liquid chemicals or etchants to remove materials from the wafer, generating only volatile byproducts in the process [18]. Dry etching may include chemical reactions that consume the material, using

chemically reactive gases or plasma, physical removal of the material, usually by ion bombardment or a combination of both physical removal and chemical reactions.
In general, the reactive species used in dry chemical etching must have high selectivity against the mask material over the layer being etched, high etch rate, and excellent etching uniformity.

Etching only along certain crystal planes, i.e., anisotropy, is another important issue. Unfortunately, most etching techniques do not exhibit high anisotropy. This is because chemical reactions can and do occur in all directions.

If maximum anisotropy is concerned, then dry etching techniques that employ physical removal of material must be considered. Sputter etching is an example of a purely physical etching process which involves bombardment of the substrate with highly energetic but chemically inert species or ions. These energetic ions collide with atoms of the material as they hit the material's surface and dislodge these atoms in the process. Unfortunately, such a purely physical process is also non-selective. On the other hand, physical sputtering and ion beam milling are the examples of purely physical dry etching techniques.

An example of a purely chemical dry etching technique is plasma etching. The highest anisotropy together with high selectivity can be achieved by using a combination of chemical and physical etching mechanism. Deep reactive ion etching is an example of dry etching that employs both physical and chemical etching technique.

1.2.2.1. Sputter Etching

Sputter etching is a process that etches the material by the transfer of mechanical momentum of the ions to the atoms or clusters of the material [12]. Sputter etching

systems are very similar in principle to sputtering deposition systems. The difference is that the material subject to ion bombardment is the substrate to be etched, instead of a source target [9].

1.2.2.2. Reactive Ion Etching

In a RIE system, RF power is applied to a combination of gases to break the gas molecules into ions. In the chemical part of the process, the ions and reactive radicals are accelerated towards the substrate to etch the surface of the material, resulting another gaseous material. The physical part is similar to sputter etching. If the ions have high enough energy, they can knock atoms out of the material to be etched without a chemical reaction. By changing the process parameters, it is possible to change the process into physical or chemical etching which will influence the anisotropy of the etching, since the chemical part is isotropic and the physical part highly anisotropic and the combination can form sidewalls that have shapes from rounded to vertical [12]. Cross sectional image of a standard RIE chamber is shown in the Figure 1.7.

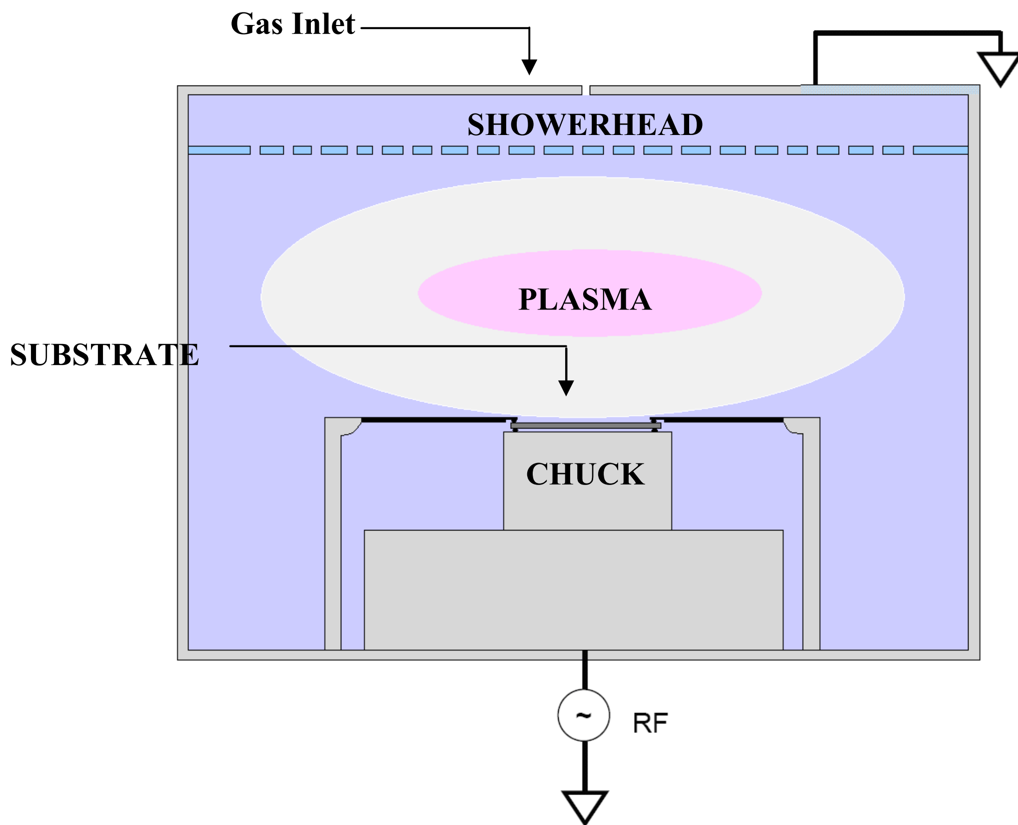


Figure 1.7: Cross sectional image of a standard RIE chamber.

1.2.2.3. Deep Reactive Ion Etching (DRIE)

Deep RIE is the special subclass of RIE process, and it become very popular in MEMS fabrication. It is an anisotropical etching process giving hundreds of microns of depth with almost vertical sidewalls. The primary technology is based on the so-called "Bosch process", named after the German company Robert Bosch GmbH developed, where two different steps are alternated in the reactor. In the first step, the substrate is deposited with the polymer including the sidewalls of the etched trench. At the beginning of the second step, polymer is sputtered away everywhere except the sidewalls. Then silicon is chemically etched at the bottom of the trench. Since

the polymer only dissolves very slowly in the chemical part of the etching, it builds up on the sidewalls and protects them from etching. As a result, high aspect ratio structures can be achieved. This process can also be used for through wafer etching with etch rates higher than that achieved by wet etching. Figure 1.8 shows the illustration of the DRIE process.

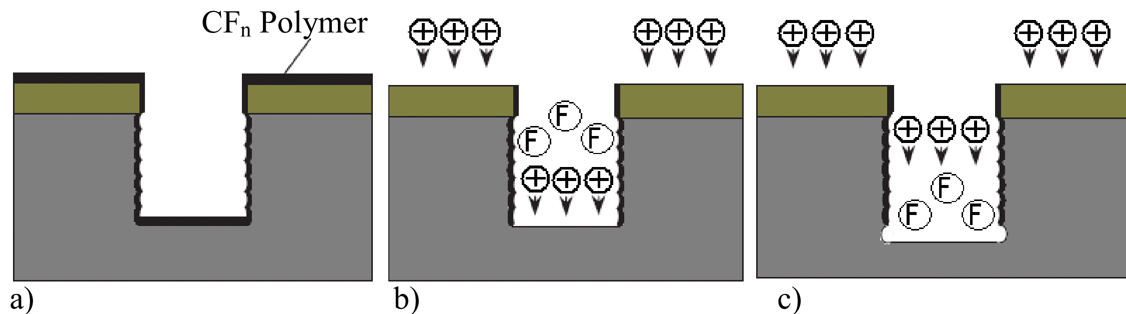


Figure 1.8: Illustration of the DRIE process: a) passivation deposition, b) removal of passivation layer from the bottom of the trench, c) chemical isotropic etching.

1.3. Applications of DRIE

The DRIE process is especially useful for devices that require complex mechanical structures. In such cases, it can be difficult to fabricate the required thick structural geometry using wet anisotropic etching due to the crystal plane dependence of wet etching. In addition, insufficient thickness of surface micromachined structures makes standard surface micromachining techniques inapplicable. Applications of the DRIE technology exist in all areas of traditional bulk micromachining: pressure sensors, fluidic microstructures, accelerometers, optical switches and more. Moreover, The DRIE process increases the silicon surface area with deeper vertical etching. Deeper grooves allow reducing the chip area, provide better control and

flexibility in silicon microsensor or microstructure fabrication since it is not restricted to structures.

One example that includes the DRIE process is the optical switches. They are widely used in telecommunication to switch signals in optical fibers or integrated optical circuits (IOCs) from one circuit to another [19].

MEMS fit well to optical switching technology due to the size of the transmission medium [4] and their better optical characteristics, such as lower cross talk and insertion loss (IL) [20].

The use of DRIE is a convenient method for producing vertical walls on silicon wafers [21]. The simply micromachined optical switch with only one vertical micromirror can realize the 2x2 optical add–drop switching using silicon DRIE process [5]. Figure 1.9 shows the operating principle 2x2 optical switch. This kind of switch has two pairs of tapered optical fibers aligned face to face. Therefore, the optical signals from input or add port propagate freely into output or drop port, respectively. When the micromirror is brought into the optical path, the optical signals are reflected and propagate into the other ports. Figure 1.10 shows the SEM image of fabricated micromirror and fiber groves.

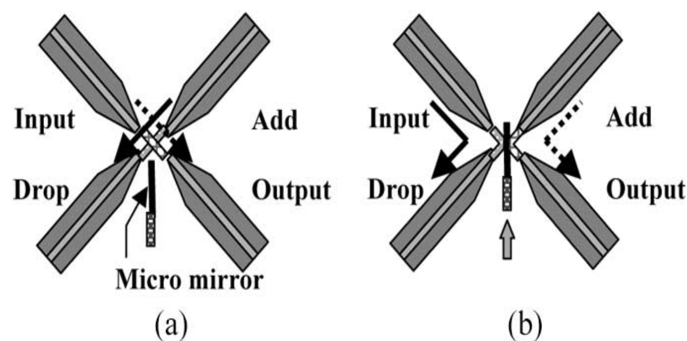


Figure 1.9: Operational principal of 2x2 optical switch a) OFF state and b) ON state [20].

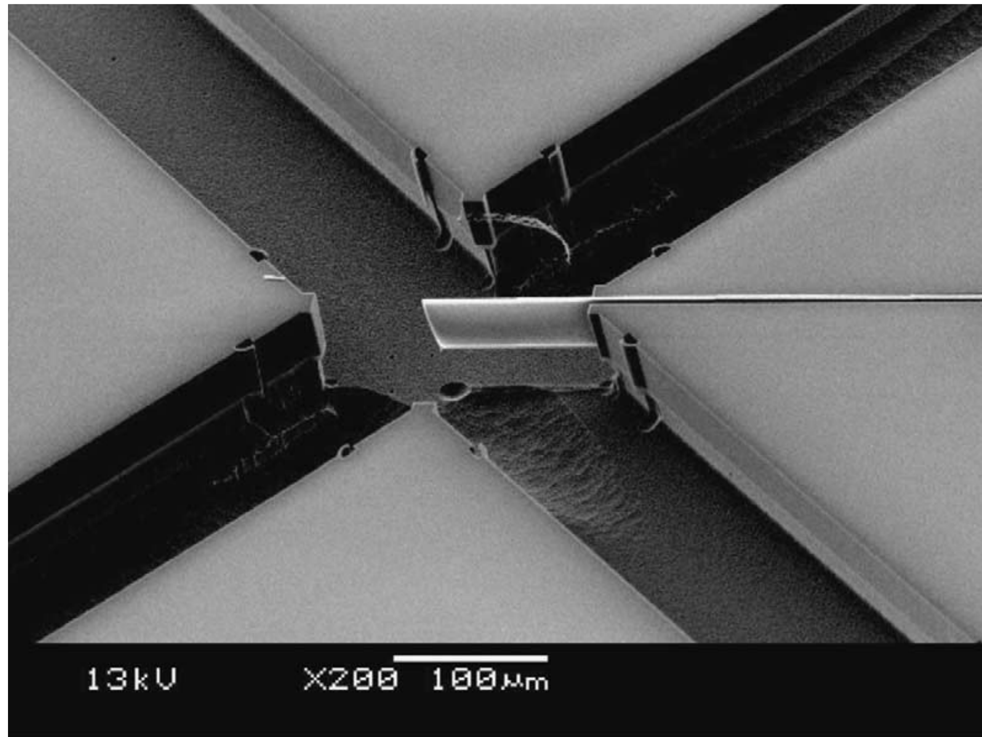


Figure 1.10: SEM image of a micromirror and fiber groves produced with the DRIE process [21].

Another application of DRIE is the fabrication of intracellular sensing probes in bio-MEMS to understand the physiology and processes of single living cells. Fabrication of sub micrometer needles is accomplished by a combination of DRIE process to form the pillars and a following RIE process to create the needles by sharpening them. The DRIE process can be used to create single needles [22, 23] or a whole array of needles. Figure 1.11 shows the individual needle-pillar with protection pillars.

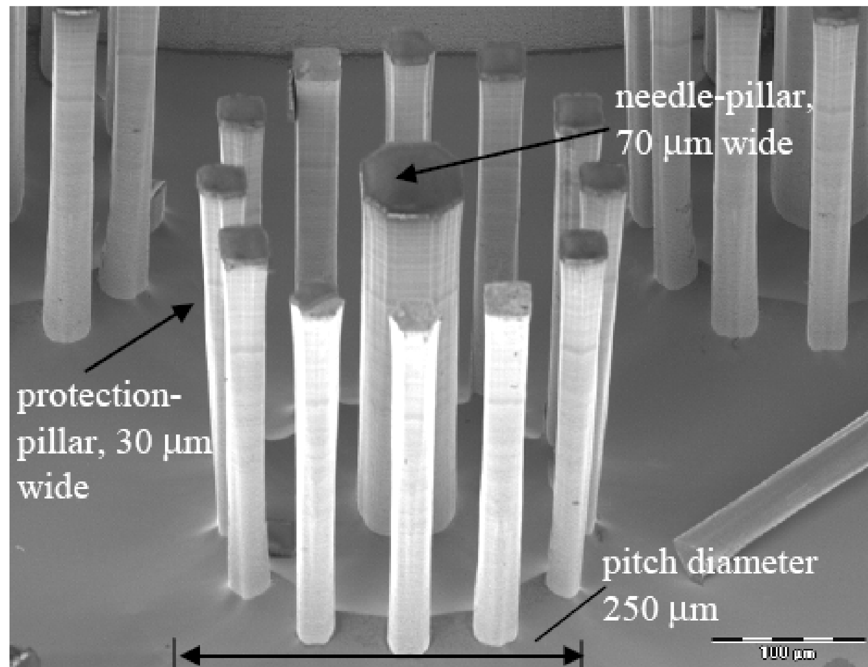


Figure 1.11: DRIE-etched pillars; pitch diameter 250 µm. The pillars are about 300 µm tall. The use of protection pillars ensures a straight profile for the needle pillar [22].

After the DRIE process for the fabrication of pillars, the wafer must be prepared for the RIE process by cleaning the masking photoresist and the DRIE polymer residues. The wafer is then subject to an RIE process to form the needles out of the 70 µm diameter pillars. This is a robust, self-sharpening process using SF6, which is optimized for obtaining long tips with high aspect ratio. During the RIE process, the 30 µm diameter protection-pillars are completely etched away leaving a ~230 µm tall single needle per pitch. Figure 1.12 shows a 230 µm tall single needle with a 200 nm wide tip.

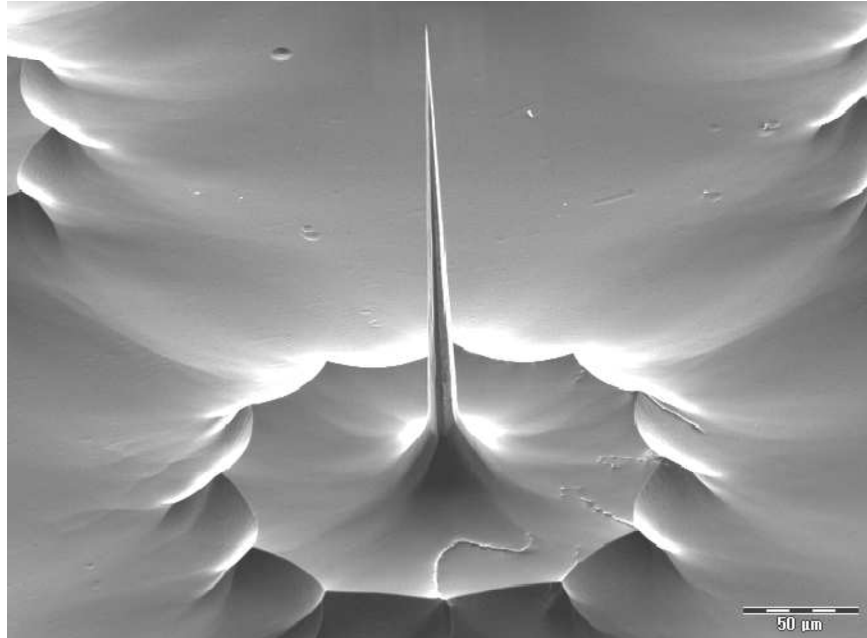


Figure 1.12: RIE-sharpened silicon needle. The needle is 230 µm tall and etched from the needle shown in Figure 1.10. The protecting pillars are eliminated during the sharpening process [22].

For intracellular recording, the fabricated silicon needles need to be covered with metal and silicon nitride to enhance the electrical properties of the needle electrolyte interface and to insulate the stump of the needle from electrical signals outside the cell [22, 23].

DRIE process is also used for the fabrication of phase Fresnel lenses (PFL) generaly used in astronomical observations since they can achieve higher sensitivity and angular resolution than the current generation of gamma and hard x-ray instruments. For ground tests of a PFL system, silicon lenses must be fabricated on the micro-scale with controlled profiles to enable high lens efficiency. Thus, two MEMS-based technologies, gray-scale lithography and deep reactive ion etching (DRIE), are extended to create multiple controlled step heights in silicon on the necessary scale.

The goal of gray-scale lithography is to only clear away a fraction of the photoresist thickness, leaving behind a series of *gray levels* that together form a 3D photoresist structure. The partial light transmission through the specially designed gray-scale optical mask coupled with time of exposure, time of development, and photoresist contrast, will determine these final intermediate *gray level* heights in photoresist [24].

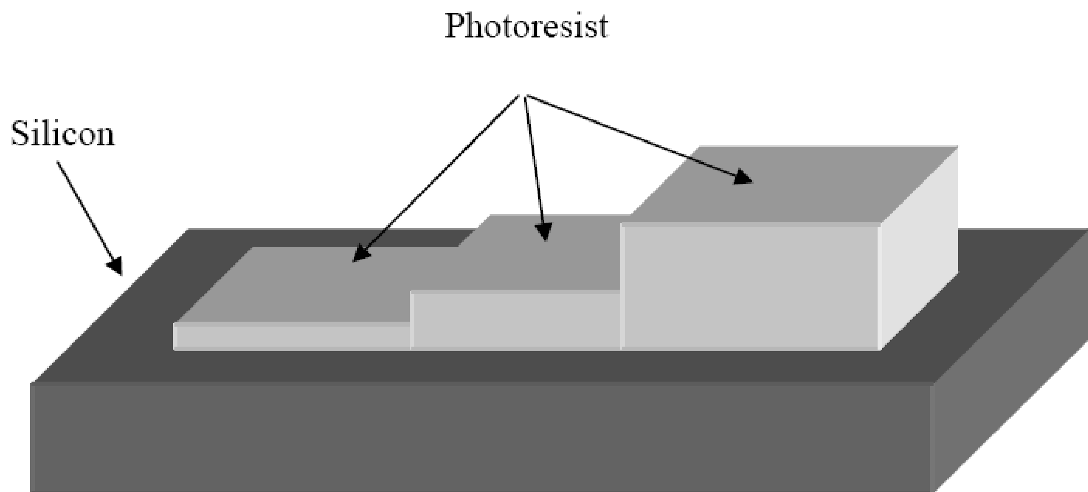


Figure 1.13: Photoresist gray levels after development, on a silicon substrate [24].

During the DRIE process, the masking material will be simultaneously etched along with the substrate. Just after removing the minimum thickness of resist, silicon will be etched and this will continue untill the maximum thickness of resist is removed. The transferred gray-scale structure retains its horizontal dimensions, however the vertical dimensions are amplified by the etch selectivity [24]. Figure 1.14 shows the phase Fresnel lens image after the DRIE process.

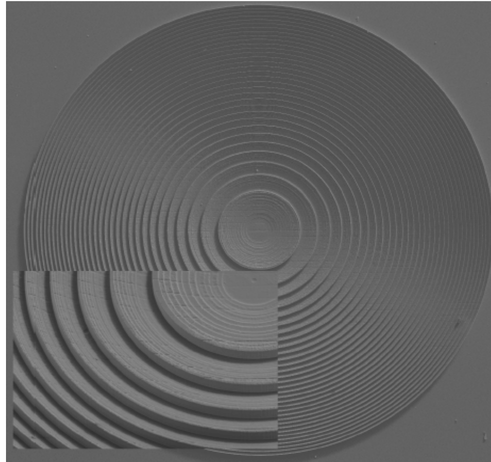
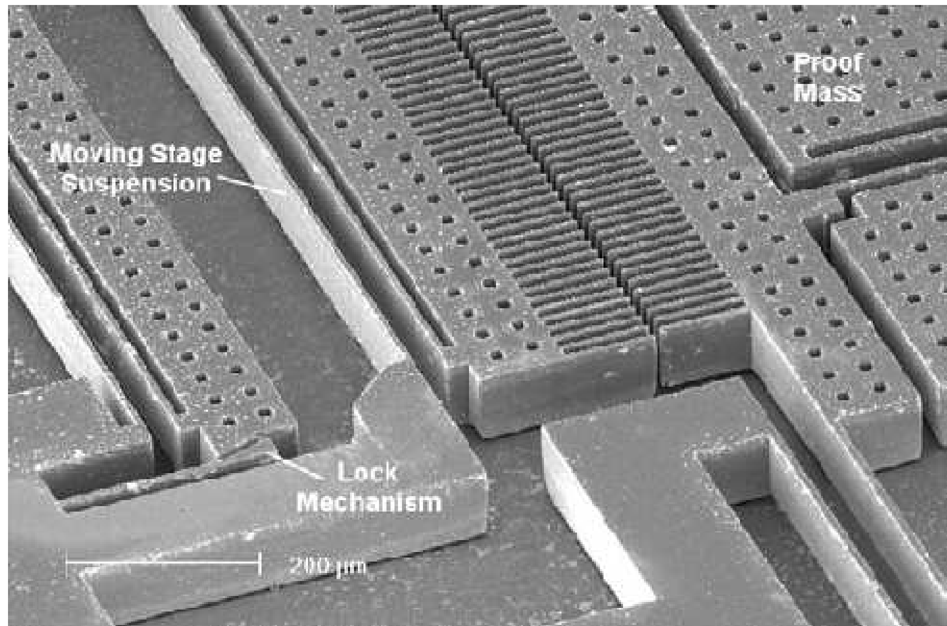


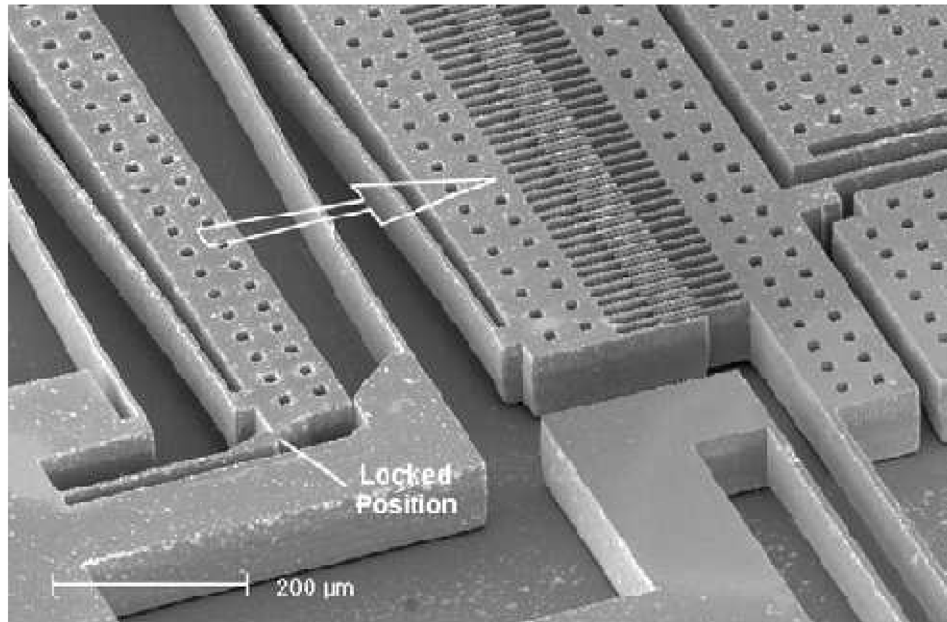
Figure 1.14: Phase Fresnel lens image after the DRIE process. The inset shows a zoom of the inner part of the Fresnel profile [25].

Another popular application of the DRIE process is the production of MEMS sensors with the increased surface area. The high aspect-ratio etching capability of DRIE allows the fabrication of large parallel plate capacitors, especially desired for capacitive sensors such as

Figure 1.15 and 1.16 show the SEM image of a gyroscope structure fabricated with the DRIE process. The operation principle of the micromachined vibratory gyroscopes relies on the generation of a sinusoidal Coriolis force due to the combination of vibration of a proof-mass and an angular-rate input. The proof mass is generally suspended above the substrate by a suspension system consisting of flexible beams. The overall dynamical system is typically a two degrees-of-freedom mass–spring–damper system, where the rotation induced Coriolis force causes energy transfer to the sense mode proportional to the angular rate input. The proof mass is driven into resonance in the drive direction by an external sinusoidal force. When the gyroscope is subjected to an angular rotation, the sinusoidal Coriolis force at the driving frequency is induced in the direction orthogonal to the drive-mode oscillation and the input angular rate [26].



a)



b)

Figure 1.15: SEM images of post-release positioning comb drives integrated in a micromachined gyroscope, (*a*) before and (*b*) after assembly [26].

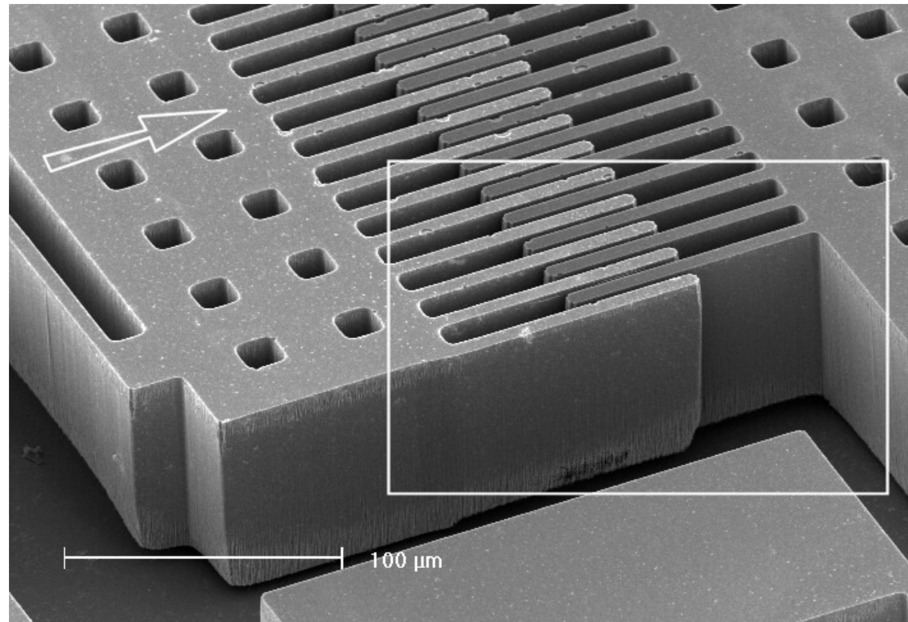


Figure 1.16: SEM images of post-release positioned comb drives integrated in a micromachined gyroscope [26]

1.3.1. Dissolved Wafer Process

Dissolved wafer process (DWP) is an illustrative example of using parallel plate capacitors. The DWP process has been widely used to fabricate micromechanical devices [27] since it can offer few masking steps, high throughput, and low production cost. The process is based on fabricating microstructures defined on a highly-doped silicon layer by using the DRIE process, silicon-glass anodic bonding, and wet etching of the undoped silicon wafer.

The process allows the fabrication of capacitive resonators, gyroscopes, accelerometers, etc., from a highly doped silicon structural layer of thickness up to more than 10 µm, a structural feature aspect ratio of 10 or more, and an insulating substrate layer for reduced parasitic capacitances.

The DWP process requires separate micromachining of the silicon and glass substrates prior to anodically bonding them to each other, and then dissolving the undoped volume of the silicon substrate leaving the highly doped-silicon sensors on glass substrate. The process requires only three masks, for pad metallization, anchor layer formation, and structural layer formation. The DRIE process is the most critical part, since it defines the minimum capacitive gaps that limits the overall performance of the sensor.

Figure 1.17 illustrates the DWP process flow. The process starts with deep boron diffusion on the polished surface of a standard silicon substrate while the back-side of the wafer is protected from the boron atoms by a growth silicon dioxide layer. Then the front-side of the silicon substrate is dry-etched to a depth of 20 μm using the DRIE process. The mask pattern contains the structural details of the silicon sensor, the beams, masses, comb electrodes, and anchor areas.

The glass substrate contains the anchor areas of sensor as well as the offset from the glass substrate to the movable structural silicon layer. After stripping the backside protection oxide layer the machined surfaces of the substrates are aligned and anodically bonded to each other.

The final step in the process is to dissolve the undoped silicon in ethylenediamine pyrocathecol (EDP) solution, until reaching the highly-doped structural silicon layer, at which the etch rate drops drastically. The suspended sensors are then cleaned with deionized water, rinsed in a standard acetone-isopropyl alcohol (IPA)-methanol bath, and dried on hotplate [28].

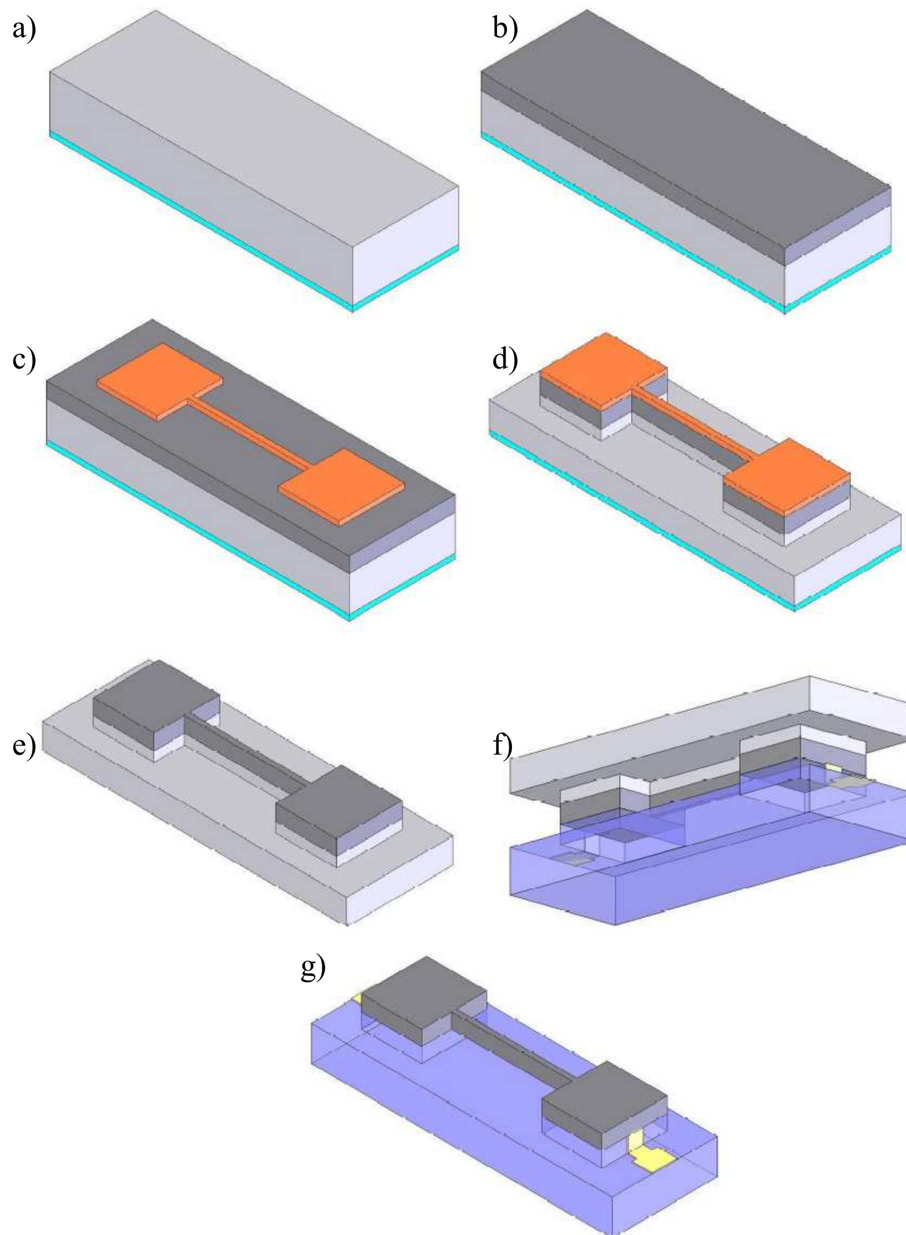


Figure 1.17: DWP process flow: a) Back-side oxidization for protection prior to doping, b) Deep boron diffusion on the front-side, c) Patterning the front-side with structural layer, d) DRIE of silicon to a depth larger than the Boron diffusion depth, e) Striping DRIE etch-mask and backside protection oxide, f) Anodic bonding of machined silicon and glass, f) Dissolve undoped silicon in EDP solution and release the structures [28].

Dissolved wafer process with the advantage of the DRIE process makes it easy to produce gyroscopes with high performance by offering few masking steps, high throughput, and low production cost. Figure 1.18 shows the suspended gyroscope structure using dissolved wafer process.

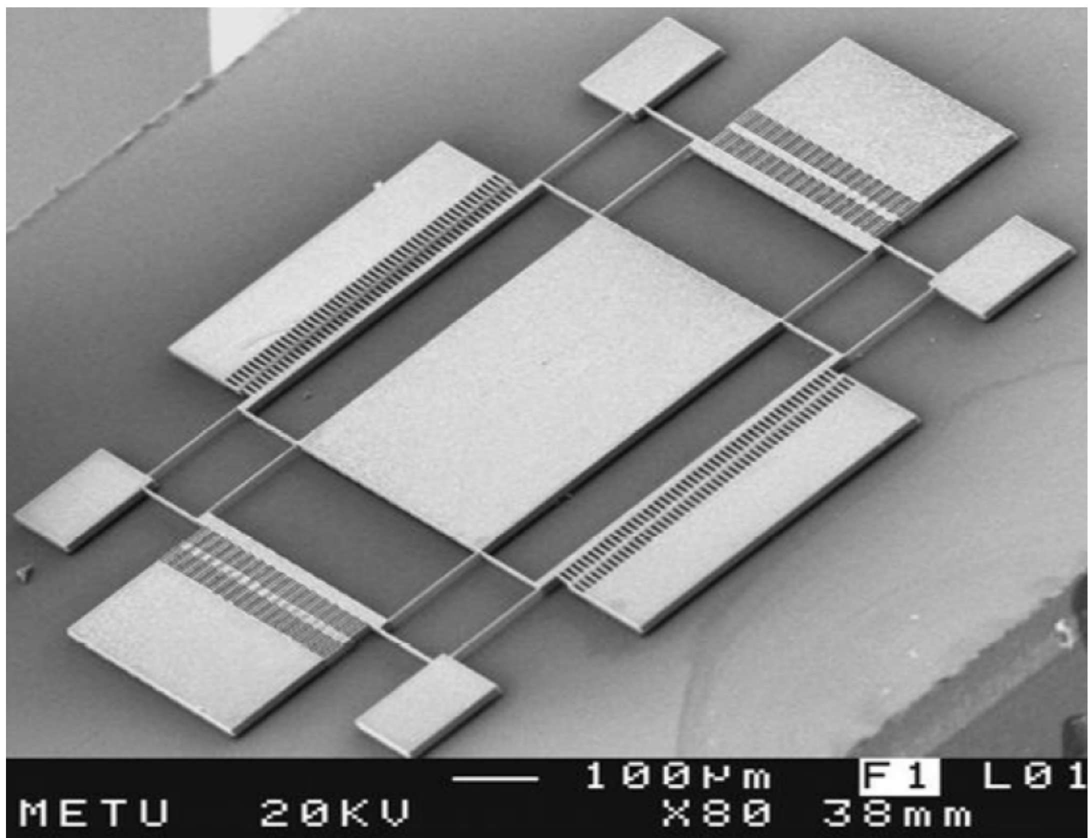


Figure 1.18: Suspended gyroscope structure using dissolved wafer process. Structural layer is p++ silicon.

1.4. Research Objectives and Thesis Organization

The goal of this thesis is to optimize the DRIE step of the dissolved wafer process for the production of gyroscopes capacitive sensors. It also aims to optimize the process parameters to obtain very high aspect ratio, 100:1, structures for silicon on glass (SOG) process. The specific objectives can be listed as follows:

- Optimizing the process conditions for opening a 1 µm wide 20 µm deep trench on silicon, with minimal loss of critical directions (1 µm). Extending this optimization to 100 µm deep trenches.

- Investigation of the effects of several parameters including step times, etch step pressure, platen power, and electrode temperature on the etch rate, profile angle, and surface roughness for 1 µm trench opening process on silicon wafers.

- Discussion on the results of the etching processes.

This thesis is organized as follows:

Chapter 2 presents the theories of deep reactive ion etching process. Detailed investigation about the process parameters is included in this chapter.

Chapter 3 explains the problems faced during deep reactive ion etching process arising from the cyclic nature of the process. The solutions to these problems are discussed in this chapter.

Chapter 4 includes the etch system configuration, wafer preparation and the optimization procedures. Results of these optimization processes are discussed at the end of each section separately.

Finally, Chapter 5 summarizes the achievements of this study, presents the conclusion of this research, and gives suggestions for future studies.

CHAPTER 2

THEORY OF DEEP REACTIVE ION ETCHING PROCESS

This chapter explains the theory of the deep reactive ion etching technique. Section 2.1 gives general information about the deep reactive ion etching process. Section 2.2 discusses two different anisotropic silicon etching processes i.e., the Bosch process and the Cryo process. Section 2.3 explains the inductively coupled plasma etching system and gives information about RF coil impedance and efficiencies. Section 2.4 explains the etch chemistry including the chemical reactions in the etching and passivation steps. Section 2.5 gives the details of process parameters and discusses the effects of each parameter on the etched structure. Finally, Section 2.6 concludes the chapter by summarizing the theory of deep reactive ion etching process.

2.1. Introduction

The deep reactive ion etching process, known as Bosch process, has been developed by Robert Bosch GmbH (Stuttgart, Germany) in 1994 [29, 30], to fabricate deep trenches in silicon substrates while maintaining smooth sidewalls, high selectivity to masking material and good profile control across a wafer

There are unique aspects of the DRIE process. Deep Reactive Ion Etching can be used to etch both shallow and deep trenches into the front side or backside of a silicon wafer. It can also be used for thorough etching of silicon wafer producing holes, diaphragms or suspended structures [31]. Deep RIE eliminates the need for costly and incompatible front side protection schemes during backside etching and provides significant reduction in chip area by increasing the sidewall angle to 90° (compared to ~53° in standard wet anisotropic silicon etch process) for devices that involve backside etching to produce or release the front side structures. With other etching techniques, it is difficult to get high aspect ratio structures with almost vertical sidewalls. For example, Figure 2.1 shows the SEM image of an aluminum layer after being etched with a reactive ion etching (RIE) system for which the sidewalls are angled.

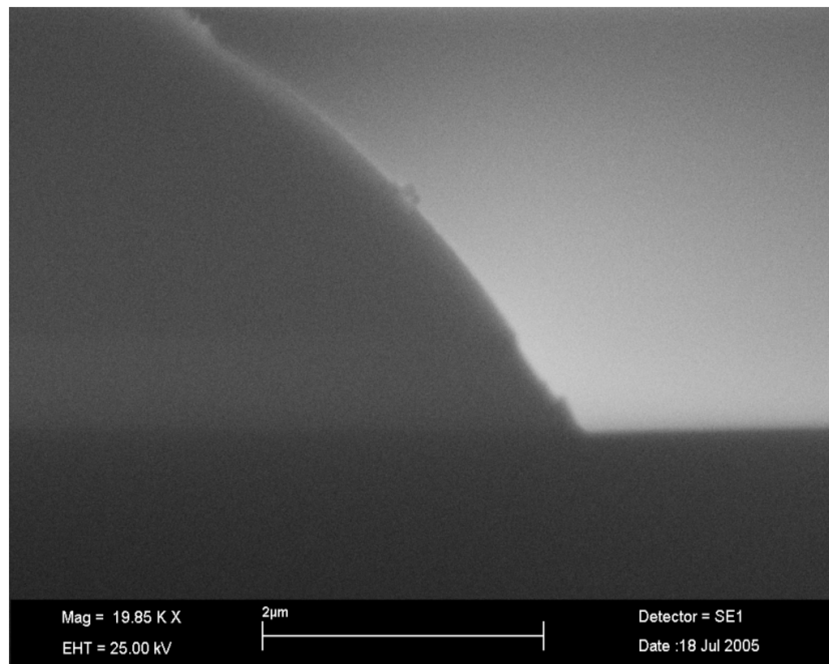


Figure 2.1: Scanning Electron Microscope (SEM) image of an aluminum layer etched with RIE system, showing limited anisotropy compared to that of DRIE.

Etch rate is another important consideration for the fabrication of MEMS structures. In deep silicon etching for Micro Electro Mechanical Systems, typical etch depths are in the range of 10 to 500 μm. Fluorine based chemistry is shown to achieve etch rates of several microns per minute, making deep silicon etching in plasma a viable alternative for KOH or TMAH based wet etching. With the high-density plasma generated in the inductively coupled plasma (ICP) reactor, it is possible to etch through the wafer as shown in Figure 2.2 [31, 32]. The etching is almost independent of the crystal orientation; it has excellent selectivity against masking oxide and photoresist layers and has a nearly vertical sidewall profile.

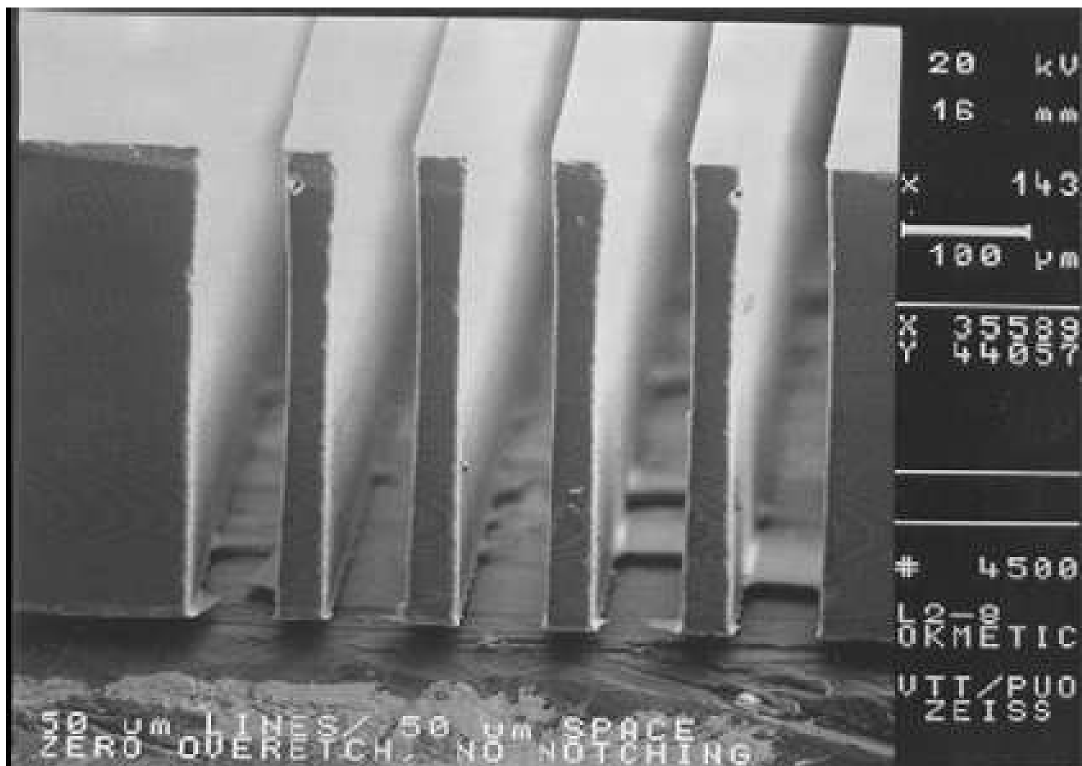


Figure 2.2: Through wafer etching with a DRIE process [31].

Masking the etch process may sometimes limit the process itself. The DRIE allows the use of a wide range of masking materials with satisfactory selectivities against silicon etch. Table 2.1 shows the selectivity of some materials that are commonly used as a masking material for DRIE process.

Table 2.1: Selectivity of various masking materials to silicon for the two ASE processes [33].

Masking material	**Selectivity to silicon (Deep process)**	**Selectivity to silicon (Shallow process)**
Thermal silicon oxide	333	172
PECVD silicon oxide	342	178
PECVD silicon nitride	28	9
LPCVD silicon nitride	106	63
Photoresist AZ6632	105	52
Chromium, evaporated	> 60 000	> 60 000

2.2. Deep Reactive Ion Etching

Deep anisotropic etching is essential for the fabrication of MEMS devices. In order to increase the capacitive electromechanical coupling, fabrication of narrow gaps in deep trenches with vertical deep gaps and with vertical sidewalls are necessary. Higher coupling results in a higher signal to noise ratio in sensors and lower equivalent motional impedance in electromechanical resonators [34]. Dry etching is a widely used technique in silicon etching since it provides better anisotropy than traditional wet etching techniques, which have etch rate dependency on crystal orientation.

Fluorine based dry etching is the most common technique for achieving high etch rate and selectivity during silicon etch. However, it is necessary to passivate the sidewalls of the etched trench for maintaining the directionality, since free fluorine radicals etch silicon isotropically [35]. The basic idea of the anisotropic reactive ion etching is to find a balance between trench sidewall passivation and trench vertical etching.

There are two main well known approaches for sidewalls protection, the Bosch process and the Cryo process. Although the Bosch process developed first, the Cryo process will be explained firstly in this part. Cryo process was introduced by Tachi et al. [36, 37] and is based on etching at cryogenic temperatures for low-bias fluorine based high-density plasmas. In this technique the sidewall protection is provided with a combination of formation of a blocking layer and reduction of the reaction probability of radicals at the silicon surface and the sidewall protection heavily depends on temperature [38], in particular in the cryogenic regime. Although initially not recognized by Tachi and his co-workers, the addition of O_2 gas to the plasma is required for deposition of SiO_xF_y as inhibitor layer to achieve directional etching [38].

The second method was developed by Laermer and Schilp [39] known as the "Bosch Process" in 1994, and is a room temperature process based on continuous cycling of subsequent passivation and etching steps, therewith achieving high aspect ratio microstructures with vertical sidewalls. Based on this generic approach, the company, Surface Technology Systems [40] has developed its advanced silicon etch (ASE) system.

2.2.1. Cryogenic Temperature Process

Tachi et al. exploit SF_6/O_2 high-density plasma chemistry to create directional etching. [38] Fluorine radicals for silicon etching are provided from SF_6 plasma and silicon is removed in the form of SiF_4 which is volatile.

The inhibitor layer is created by oxide and fluoride radicals via the formation of a SiO_xF_y deposit [41] and cryogenic temperature improves the protection of this layer from the fluorine radicals by reducing the chemical reactivity, which can be explained by a reduction in the volatility of reaction product SiF_4 [42, 43]. Ions like SF^+_5 are also produced during SF_6 decomposition that enhance etching of the SiO_xF_y layer locally as they strike the surface with relatively low kinetic energies. Since the bottom of the structure is exposed, etching can proceed there, leading to anisotropic features.

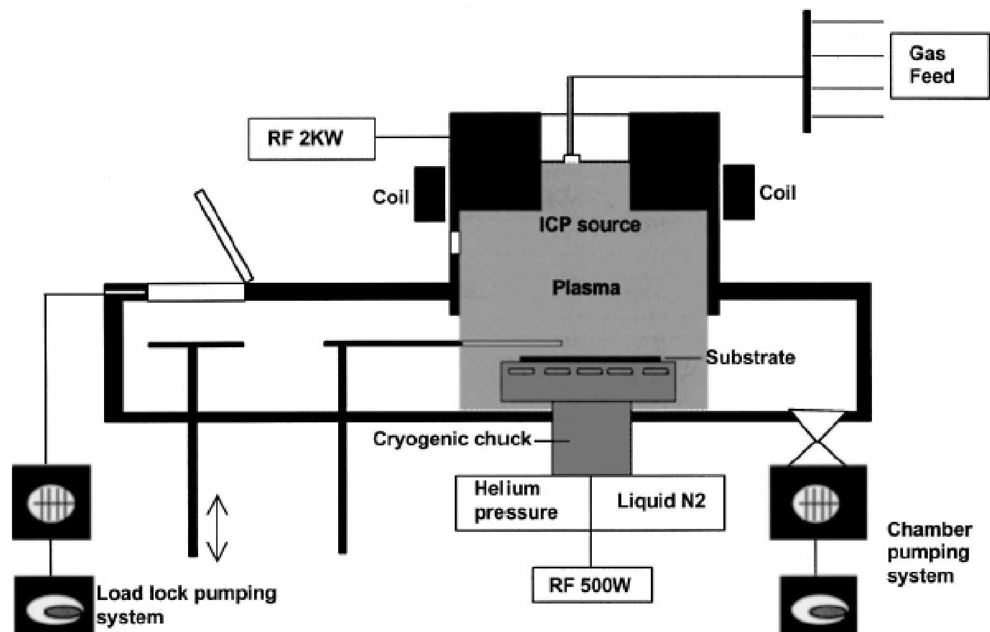


Figure 2.3: Schematic drawing of a cryogenic temperature DRIE chamber [44].

In a SF_6–O_2 plasma at a cryogenic temperature, the processes of formation of the passivation layer, its removal from the bottom of a trench, and the etching of silicon occur simultaneously [45].

The low temperature operation also increases the selectivity of the mask material, which is normally either photoresist or silicon dioxide. The attack on these materials by free radical fluorine is chemical in nature and is sensitive to temperature. On the other hand, the low temperature can have a adverse effect on some organic materials, causing cracking. Figure 2.4 shows the SEM image of a masking resist cracked at cryogenic temperature during the etch process. This effect becomes more severe for thicker photoresist. If a thicker layer is needed to achieve a very deep etch, then silicon dioxide should be used as the masking material, as it does not suffer from cracking problems [46].

Since temperature of the substrate is a very important parameter for profile control, it is not practical to use handle wafers for small pieces. These would significantly affect the thermal path from the sample being etched to the liquid nitrogen cooled stage, in a way that cannot easily be predicted. Another disadvantage of the cryogenic temperature process is that, it not compatible with many applications due to its low process temperature [46].

Figure 2.4: SEM image of a masking resist cracked at cryogenic temperature during the etch process [31].

2.2.2. Bosch Process

The Bosch, or time domain multiplex (TDM), process is a method where the etching and passivation mechanisms are separated in time and these mechanisms are continuously switched to keep the sidewalls perpendicular to the surface [47]. The Bosch process thus has an overall deep anisotropic profile, although each individual etch step may be more or less isotropic depending on the process conditions. This process is patented by Robert Bosch GmbH [29, 36] and licensed by several companies including STS, Alcatel, Oxford instruments, Unaxis [47].

Like the Cryo process, the Bosch process also uses a fluorine based plasma chemistry to etch the silicon, combined with a fluorocarbon plasma process to provide sidewall passivation and improve selectivity of the masking material [48].

In the etch step sulphur hexafluoride (SF_6) is used to provide the free radical fluorine for silicon etching and the passivation step is provided by octofluorocyclobutane (C_4F_8), a cyclic fluorocarbon that breaks open to produce CF_2. These readily deposit as fluorocarbon polymer on the samples being etched. The profile, etch rate and selectivity to the mask material are all controlled by adjusting the etch step efficiency, the deposition step efficiency or the ratio of times of the two steps.

The Bosch process includes several physical and chemical processes including rarified gas flow, gas ionization, ion bombardment, neutral diffusion which are physical and neutral-silicon and ion-silicon reactions which are chemical. It begins with an isotropic etch step, during which the exposed silicon is isotropically etched with SF_6 plasma. Then the passivation step starts in which thin fluorocarbon film is deposited on the surface of the wafer from C_4F_8 plasma. Although fluorocarbon film is deposited all the surface of the substrate, it is used for sidewall passivation. At the beginning of the next etch step, the fluorocarbon polymer is removed from the horizontal surfaces of the substrate by ion bombardment. Ions created in the bulk plasma are accelerated across the sheath, gain energy and used to remove polymer. Increasing ion energy in the vertical direction results in a much higher rate of removal of fluorocarbon polymer on horizontal surfaces than that on vertical surfaces. After polymer removal the horizontal silicon surface is exposed to reactive fluorine-based species. The silicon at the base of the trench is etched chemically during this period, whilst the vertical surfaces remain protected by the fluorocarbon polymer layer. Repeating the etching and passivation steps enable the silicon to be etched vertically. Figure 2.5 shows the cyclic nature of the process.

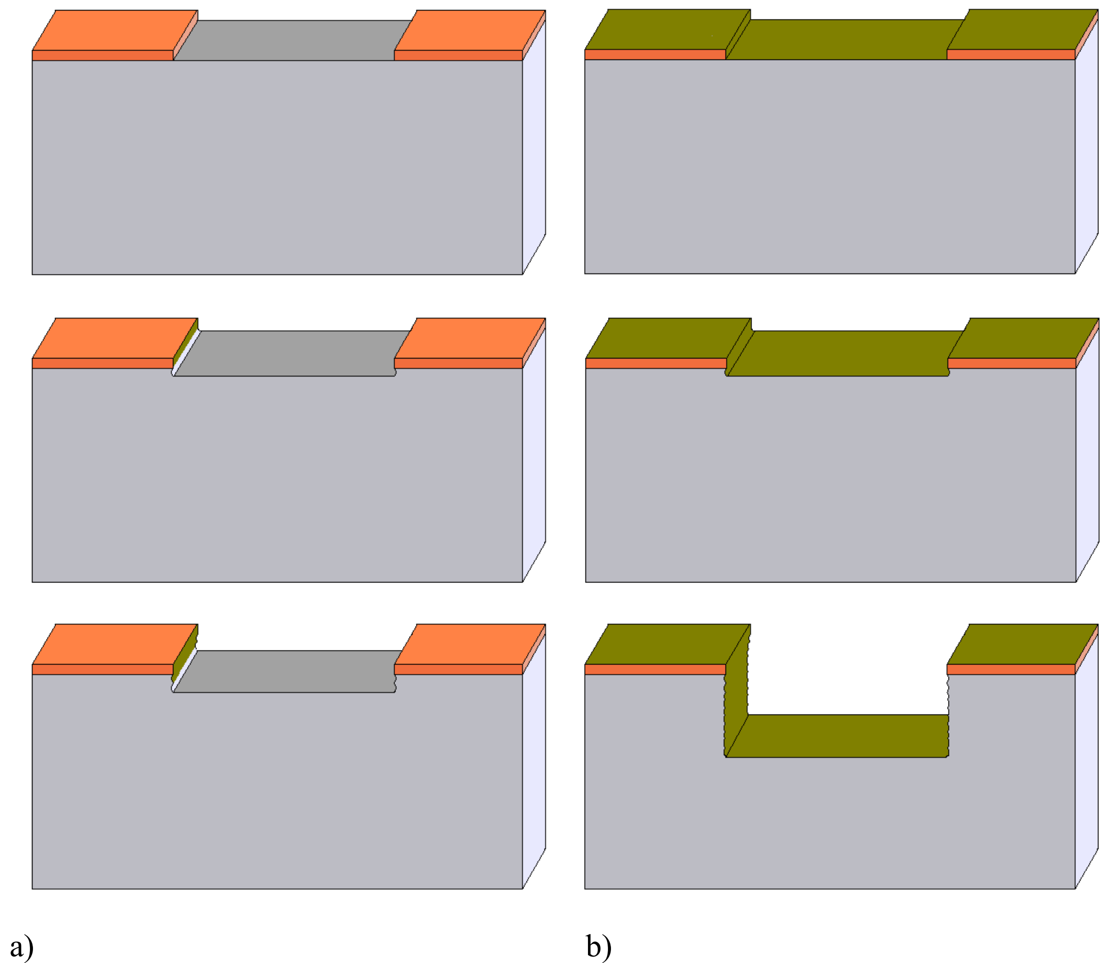


Figure 2.5: Deep silicon etching using the Bosch process: a) removal of passivation layer and isotropic etch step, b) passivation deposition.

Typical etching systems for the Bosch process include two RF generators. The first one, a high-power coil generator, operates at 13.56 MHz, is used for creating an intense inductively coupled plasma (ion concentration above 10^{11} cm^{-3}), and the second one, an independent RF power generator which can operate at both high frequency, 13.56 MHz, and low frequency, 380 kHz, is used for biasing the wafer electrode (platen). Despite high power and high plasma intensity, the bias voltage is

relatively low. The wafer is cooled during the process by helium backside flow. The wafer can be clamped to chuck mechanically or electrostatically to ensure thermal contact to the electrode which is cooled with a water flow. If thermal contact is lost or insufficient, the wafer temperature can rise too high for passivation deposition [49]. Figure 2.6 shows the schematic drawing of a typical DRIE – ICP chamber.

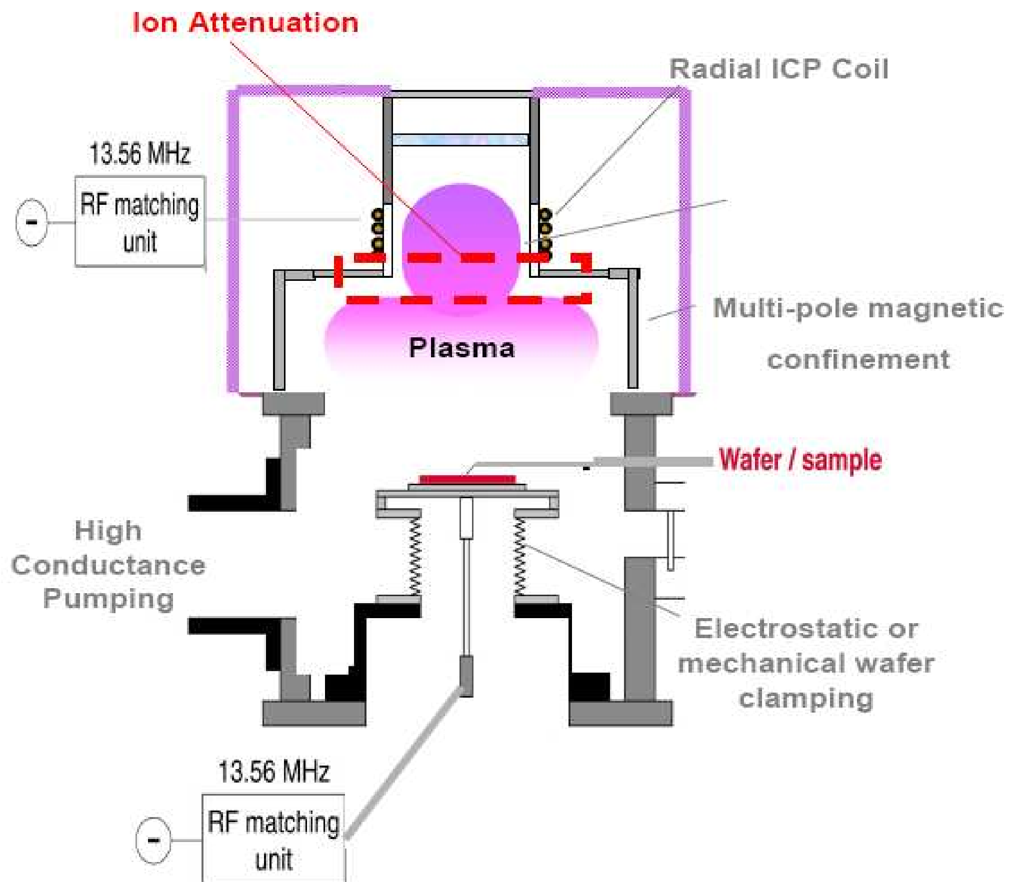


Figure 2.6: Schematic drawing of a typical ICP chamber [50].

Low frequency (380 kHz) also known as SOI, is an option developed by STS to prevent the notching effect while etching silicon to buried insulating layers. The SOI

option works under the following principle. A separate pulsed, low frequency power input is applied to the platen during the etching cycle. Low frequency allows the ions to escape more readily from deep trenches when the etching cycle is done than operating at high frequency. As a result, a decrease in over-etch sensitivity emerges, and the notching or "footing" of Silicon structures is minimized. It is also efficient for increasing the selectivity of the masking material. The result is the ability to produce high aspect ratio structures [49].

2.3. Inductively Coupled Plasma Etching

The requirements for DRIE processing plasma must include high density ions, electrons and radicals, excellent uniformity over a large diameter, low and controllable ion energies and negligible contamination from reactor sputtering at low pressures [51].

In conventional plasma etch systems, like RIE, plasma is typically generated by applying an RF electric field between two parallel plates. However, these systems cannot supply the plasma requirements of the DRIE processing. High plasma densities at low pressures have been achieved with electron cyclotron resonance (ECR) sources and magnetron systems [52, 53]. However, the presence of a strong magnetic field (850 G) leads to difficulties in achieving both good process uniformity and gate integrity [54]. One of the most commonly used method for generating high density plasma with a good uniformity is coupling electromagnetic energy from a coil surrounding the plasma chamber, called as inductively coupled plasma (ICP) [47]. RF coil surrounding the chamber generates a magnetic field inside the chamber. Secondly, the plasma will act as the secondary coil in a transformer. Since this RF magnetic flux density a time varying, it will induce a solenoidal electric field, according to Faraday's law given in Equation 2.1. This

induced electric field accelerates electrons and ion thereby causes collisions resulting more ion and electrons [51, 54]. Figure 2.7 shows the sketch of a helical ICP coil chamber.

$$\nabla \times E = -\partial B / \partial t \qquad 2.1$$

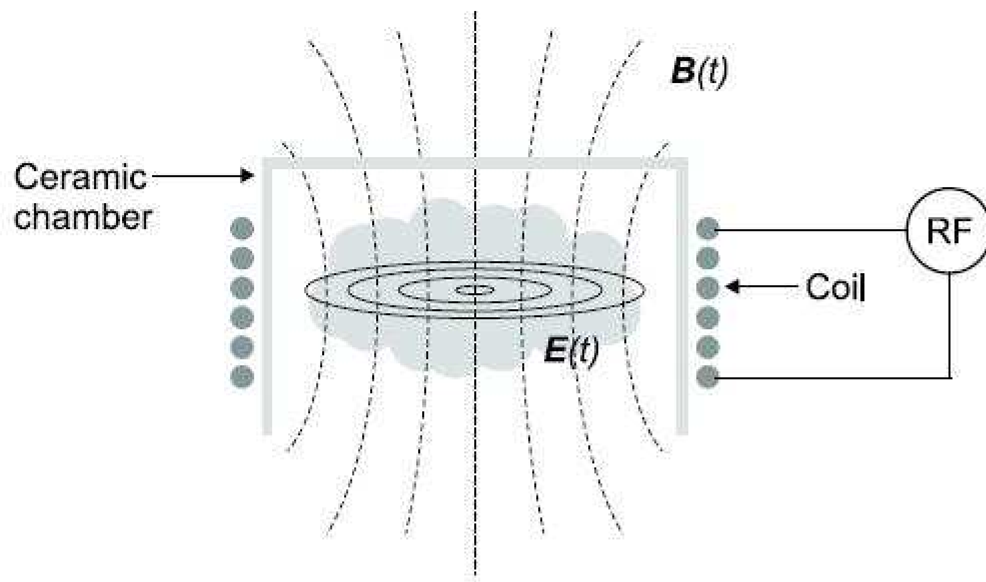


Figure 2.7: Sketch of a helical ICP coil chamber. The axial magnetic field induces an azimuthal electric field, which accelerates the charged particles [47].

Electrons and ions in the plasma will be accelerated with the presence of an induced electric field. Since the electron mass is much lighter than the ions', electrons will acquire a larger speed, and as a result they will leave the plasma. Therefore the plasma will become electrically positive compared to the surrounding. Then the ions in the plasma will be accelerated towards the chamber walls. An independent RF bias between plasma and wafer chuck can be used for ion bombardment of the wafer by

increasing the energy of the ions. Using RF frequencies prevents excessive charging of insulating substrates and enhances the efficiency of the ionization processes [47].

For capacitively coupled plasmas, the plasma efficiency is inversely proportional to the applied RF power since the plasma density is proportional to only the square root of the plasma power for the desired conditions where the sheath impedance dominates [54].

The efficiency of inductive plasmas, on the other hand, is high in the density region desired for single wafer plasma processing. The inductive coupling method allows producing a dense plasma with an electron density around 10^{12} cm^{-3} [47]. With the increasing density of the plasma, etch rate also increases, since the supply of the radicals is the limiting factor in the etch process.

Keeping the chamber pressure at low values, prevents the increased scattering, thus the directionality of the ion bombardment is maintained. With the combination of high density plasma and control on the ion bombardment high etch rates with high mask selectivities can be achieved [47].

2.3.1. RF Coil Impedance and Efficiency

By using the simple theory for the impedance of a transformer, the resistance of the plasma seen by the RF coil and the total resistance Re |Z1| are expressed as

$$R_{12} = k^2\omega^2 L_1 L_2 R_2 / Z^2 \qquad 2.2$$

$$Re|Z_1| = R_1 + R_{12} \qquad 2.3$$

where

$$Z^2 = (\omega L_2 + \omega L_e)^2 + R_2{}^2 \qquad 2.4$$

L_1 and L_2 are the RF and plasma coil inductances respectively, R_2 and L_e are the resistive and inductive effect of the electrons in the conductive skin of the plasma respectively, k is the coupling coefficient defined by geometrical parameters and R_1 is the RF coil resistance. Similarly, the inductive impedance respectively is

$$ImZ_1 = \omega L_1 - \omega^2 M^2 \omega L_{p1}/Z^2 \qquad 2.5$$

where $L_{p1} = L_2 + L_e$ is the plasma inductance and $M = k(L_1L_2)^{1/2}$ is the mutual inductance. From the conductivity and geometry the skin resistance is

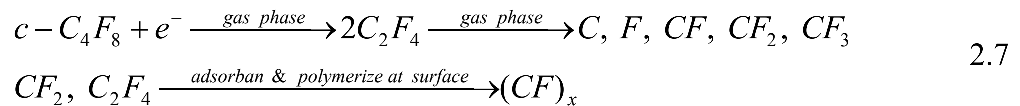
$$R_2 = \pi m \nu_{eff} /e^2 n_e d_s \qquad 2.6$$

for a planar system, where m and e are the mass and charge of the electron respectively, and n_e is the electron density per cubic meter.

The inductance L_e is given by Equation 2.6 divided by ν_{eff} . Except at low or high density ($n_e << 10^{17}$ or $10^{17} << n_e$), L_e and L_2 are of about the same magnitude [54].

2.4. Etch Chemistry

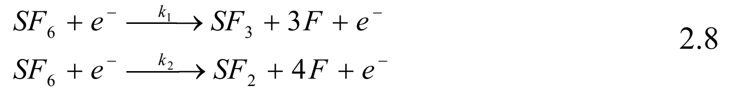
In the Bosch process, the deposition and etch steps are performed separately. During the deposition step, plasma breaks apart the strained cyclic hydrocarbon C_4F_8 into highly excited fragments. The individual fragments react one with another on the exposed surface and build up a more or less strongly cross-linked layer of polymer [55, 56]. This is called plasma polymerization. Although many neutral and ionic species are produced, the highest fluxes of species at the surface during deposition have been measured to be CF_2 and C_2F_4. The general chemical reactions are:



$$c-C_4F_8+e^- \xrightarrow{gas\ phase} 2C_2F_4 \xrightarrow{gas\ phase} C,\ F,\ CF,\ CF_2,\ CF_3$$
$$CF_2,\ C_2F_4 \xrightarrow{adsorban\ \&\ polymerize\ at\ surface} (CF)_x \qquad 2.7$$

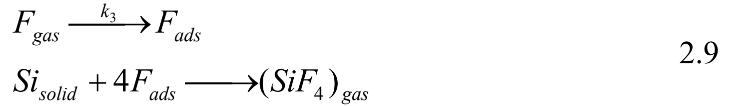
In the etch step SF_6 is used. The etch step includes two mechanisms. One of them is removal of the horizontal component of the polymer, by accelerating the ions in the plasma to the wafer surface, with an applied RF bias between the plasma and the wafer chuck. After the removal of the polymer, silicon is isotropically etched using atomic fluorine generated from SF_6 plasma.

The main chemical reactions in the gas phase of the SF_6 etch are:



$$SF_6 + e^- \xrightarrow{k_1} SF_3 + 3F + e^- \quad\quad 2.8$$
$$SF_6 + e^- \xrightarrow{k_2} SF_2 + 4F + e^-$$

At the wafer surface, Si is etched by the following reaction:



$$F_{gas} \xrightarrow{k_3} F_{ads} \quad\quad 2.9$$
$$Si_{solid} + 4F_{ads} \longrightarrow (SiF_4)_{gas}$$

Since ion fluxes at the wafer surface are relatively low compared to the F flux, SiF_6 is a primarily chemical etch producing an isotropic profile. Using continuity equations at the surface, an analytical expression for the etch rate can be obtained as follows.

$$\frac{\partial SF_6}{\partial t} = \frac{F_{SF_6}}{V} - \frac{SC_{SF_6}}{V} - k_1 n C_{SF_6} - k_2 n C_{SF_6} = 0 \quad\quad 2.10$$
$$\frac{\partial F}{\partial t} = \frac{SC_F}{V} + 3k_1 n C_{SF_6} + 4k_2 n C_{SF_6} = 0$$

Although there are many other reactions in the plasma, it has been reported that the one producing SF_3 accounts for about 2/3 and that producing SF_2 accounts for 1/3 of the released etching species F [57]. Solving for gas phase concentration of SF6 and F:

$$C_{SF_6} = \frac{\frac{F_{SF_6}}{V}}{\frac{S}{V} + k_1 n + k_2 n} \qquad 2.11$$

$$C_F = \frac{V}{S}\left[3k_1 n + 4k_2 n\right]C_{SF_6} = \frac{V}{S}\left[3k_1 n + 4k_2 n\right]\frac{\frac{F_{SF_6}}{V}}{\frac{S}{V} + k_1 n + k_2 n} \qquad 2.12$$

Therefore, the etch rate at the surface is can be expressed as,

$$Etch\ Rate = \frac{\Omega_{Si}}{4} k_3 C_F = \frac{\Omega_{Si}}{4} k_3 \frac{V}{S}\left[3k_1 n + 4k_2 n\right]\frac{\frac{F_{SF_6}}{V}}{\frac{S}{V} + k_1 n + k_2 n} \qquad 2.13$$

In spite of the rounded profiles, F chemistry is preferential to other etch chemistries due to the high volatility of SiF_4, the Si etch product [5, 9, 58]. This is necessary for deep features, as the presence of less volatile etch products in small feature sizes can inhibit etch rate [59].

The preferential etching of the bottom of the trench compared to its sidewalls can be modeled in several ways. Some literature suggests that the polymer is selectively deposited on the vertical sidewalls rather than on horizontal features [59, 60] as part of the dep/etch process balance. This would create a very thin polymer film on the bottom of the trench as compared to the sidewalls. Other sources indicate that polymer deposition is uniform, and that there is a third "breakthrough" etch step through the polymer from the bottom of the trench exposing Si to subsequent processing by the mostly chemical SiF_6 etch mechanism [47].

2.5. Process Parameters

There are several process parameter such as step times, gas flows, process pressure, platen and coil power and platen temperature effecting the process. The etch rate, profile angle of the trenches, uniformity, and selectivity are related to the pattern geometry and the process parameters such as individual step times of etching and passivation, process pressure, coil and platen power, process temperature gas flows and electrode temperature. The effects of these parameters are briefly discussed in the following sections.

2.5.1. Step Times

Step times are the individual etch and passivation times cycling during the process. They have a large influence on the profile and the etch rate [61]. If the ratio of the etch and passivation cycles is too large, then sidewalls will not be sufficiently protected and the etch will result in reentrant profiles. Contrarily, if the cycle ratio is too small then this leads to excess passivation on the base of the trench [62]. Moreover, if the deposition content of the etch step is too large then this can lead to the etch stopping altogether.

Generally the larger the step time for the etch step, the larger the scallops or increased roughness on the sidewall. Increasing the switching frequency of the plasma gases decreases the scallops' size and reduces the roughness of the sidewalls by decreasing the isotropic etch time at the bottom of the trench before the next passivation step protects the sidewall [34].

The optimum etch and passivation times and their ratio depend upon the application; for high aspect ratio structures the duration must be short whilst for deep etches of

large features etch time should be set to large value. It is important to realize that there is a fine balance between the step times.

Figure 2.8 and 2.9 shows the SEM pictures of the DRIE etched trenches with identical mask patterns and etch process parameters except the switching times. 2 seconds etch and 2 seconds passivation, 4 seconds etch and 4 seconds passivation respectively.

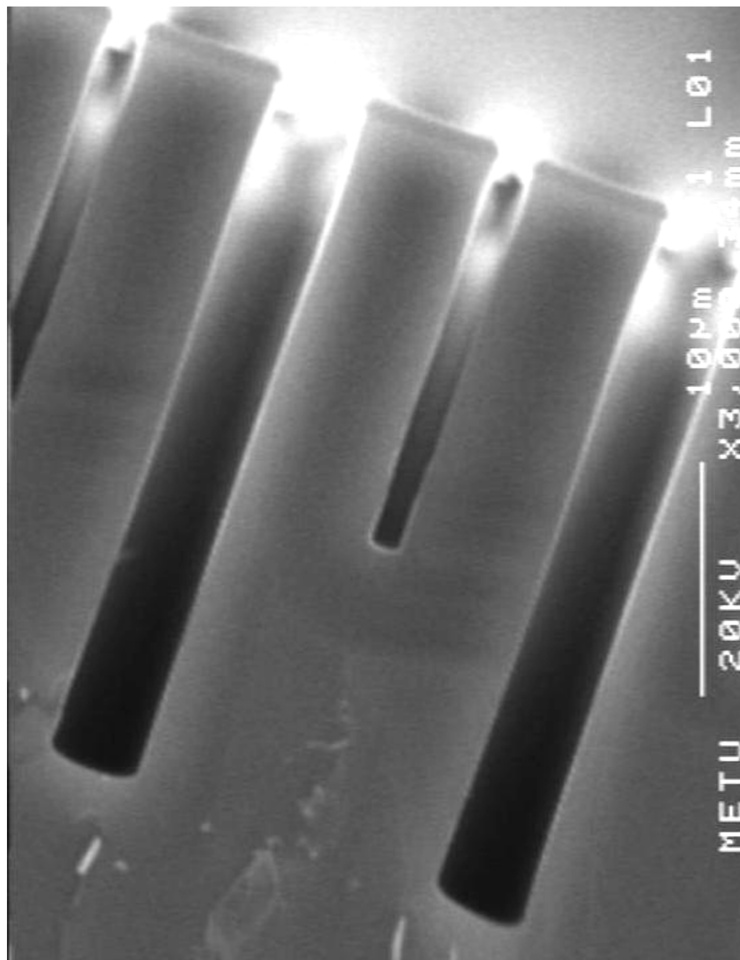


Figure 2.8: Effect of reducing step times to two seconds for the etch step and two seconds for the deposition step on the profile angle. Both profile angle gets positive and mask undercut increases.

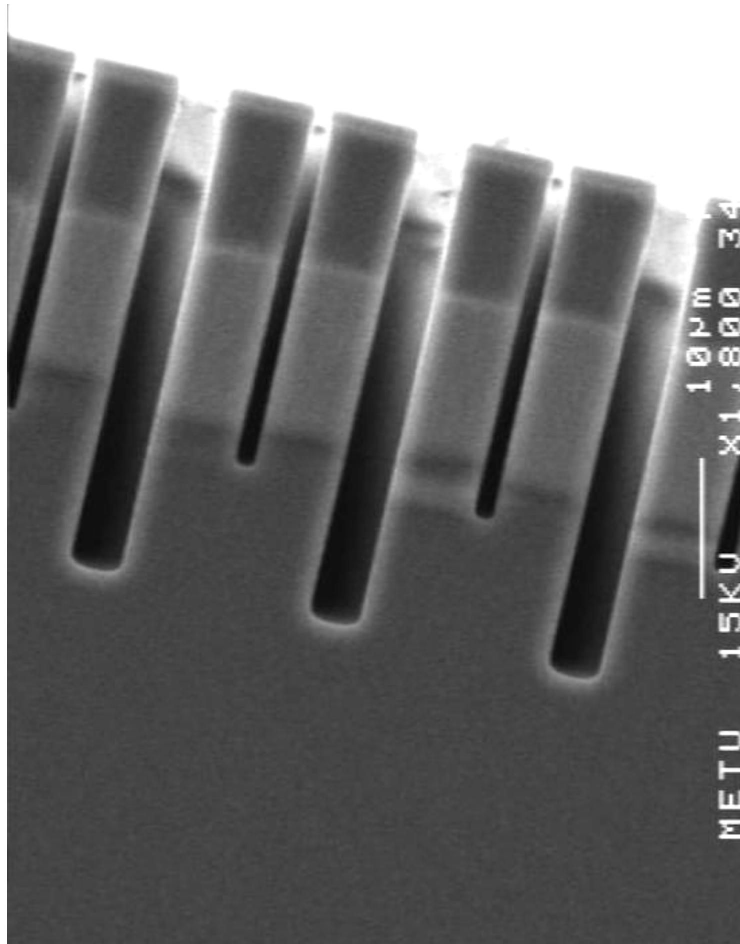


Figure 2.9: Effect of increasing step times to four seconds for the etch step and four seconds for the deposition step on the profile angle with a reduced mask undercut.

2.5.2. Gas Flow Dependence

Increasing the SF_6 flow during the etch step generally, increases the etch rate of the process. After a threshold, increase in etch rate will depend on the applied power. In other words, for a particular flow of SF_6 there is a point at which more power is required to ionize the SF_6 gas, and if this power is not supplied then the additional gas will not be ionized into reactive species resulting no change in etch rate. In the

same manner, thickness of the passivation layer will increase with increased C_4F_8 flow up to a certain limit.

2.5.3. Pressure Dependence

The process pressure has a great impact on the overall etch results [63], generally higher pressures in the etch step lead to higher etch rates resulting from the increased number of fluorine radicals available [64].

In addition, selectivity of the photoresist also increases with the increased process pressure. Increasing the pressure in the etch step, increases the availability of the free fluorine radicals for etching silicon chemically, resulting an increase in etch rate. Since increase in pressure also increases the collision ion/neutral scattering, ion energy and ion directionality will be reduced and this will reduce the etch rate of the photoresist [30, 45]. However, for high aspect ratio features this can cause a problem in term of profile control.

Processing high aspect ratio structures at high pressures causes the bowing and closing up towards the base of the trenches due to increased scattering of ions at higher pressures [64]. Keeping the process pressure low results in better profile angle. However, this will also reduce the selectivity of the masking material as a consequence of the increased ion energy. Pressure dependence of the profile angle is shown in Figure 2.10 and Figure 2.11.

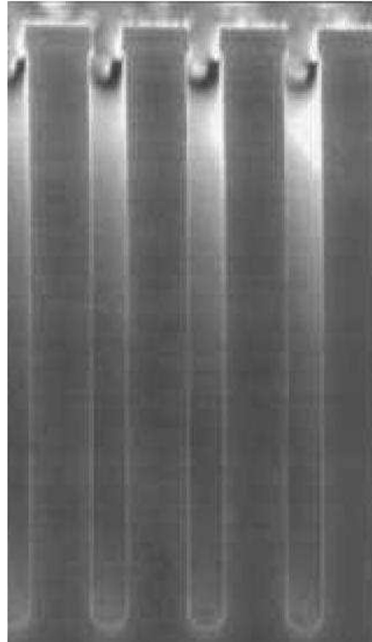


Figure 2.10: Effect of process pressure on profile angle at low pressure value, vertical sidewalls achieved [63].

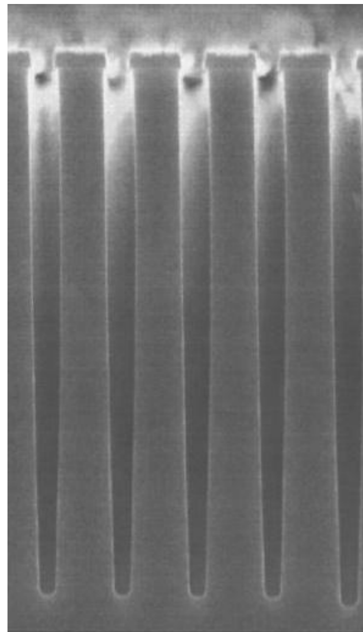


Figure 2.11: Effect of process pressure on profile angle at high pressure value, positive profile angles observed [63].

2.5.4. Platen & Coil Power Dependence

One of the radio frequency generator is the coil power. It is used for generating the plasma. Higher the power applied, more ions and free radicals will be generated.

Another radio frequency generator which is used to accelerate ions through the wafer is the platen power. It plays a major role in that once the ions are accelerated through a sufficiently high potential (to attain energies larger than 20eV) they remove the passivation from the base of the feature whilst leaving the sidewall passivation intact [64].

For higher aspect ratio features, the platen power plays an increasingly important role. Lack of bias during processing of high aspect ratio features can lead to closing up of the trenches toward the base [64].

There are both advantages and disadvantages of increasing platen power. Increasing the platen power improves the directionality of the plasma reactive particles. This will increase availability of plasma species at the bottom of a high aspect ratio trench. However, too much increase in platen power may cause both visible bowing in the trench profile [65] and increase in the etch rate of the masking material.

Figure 2.12 shows the relation of the photoresist etch rate with the platen and coil power.

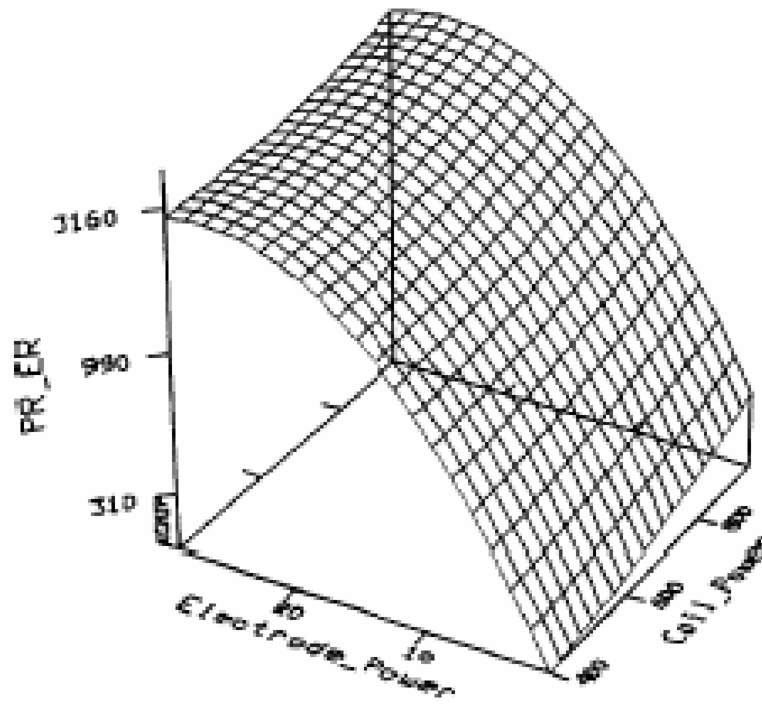


Figure 2.12: Platen and coil power dependence on photoresist etch rate [65].

2.5.5. Electrode Temperature

The passivation step strongly depends on the temperature of the substrate surface. During the process, temperature of the substrate is kept at a fixed temperature by cooling the chuck and temperature uniformity over the wafer is accomplished by helium flow at the back side of the wafer.

Increase in temperature, reduces the passivation rate, resulting in a decrease in the selectivity of the masking material.

2.5.6. Summary of the Parameter Effects

The effects of the increasing the process parameters on the etch rate, profile angle and selectivity are summarized in Table 2.2 from the given information in the previous sections.

Table 2.2: Summary of the parameter effects on the process.

Increasing Parameters	Etch Rate	Profile	Selectivity
SF_6 Flow	Increases	Negative	Increases
C_4F_8 Flow	Decreases	No effect	Increases
Etch:Dep Time Ratio	Increases	Negative	Increases
Pressure	Increases	Negative	Increases
Platen Power	Increases	Negative	Decreases
Coil Power in Etch	Increases	Negative	Increases
Coil Power in Dep	Decreases	Positive	Increases

2.6. Conclusion

The Deep Reactive Ion Etching or DRIE is a widely used etching method having applications in all areas of bulk micromachining, since it can give a high etch rate, good mask selectivity, high aspect ratio, and vertical anisotropic etching required by many of today's MEMS processes. However it has many parameters affecting the

etch process, and those parameters must be optimized for achieving specific etch profiles.

To complicate the matter even more, the optimal balance of process conditions differs for different mask layouts. Although the DRIE technology is continuously being improved, the optimization of the process for a special mask layout is still a time consuming affair and strongly depends on the skills and experience of the engineer.

This chapter explained the theory of the DRIE processing. Two different methods are examined, Bosch process and etching at cryogenic temperature. Effects of individual parameters including step times, gas flow rates, process pressure, platen and coil power and electrode temperature, are explained. In the last section, effect of each parameter are summarized. In the following chapter, mostly faced problems during the DRIE process are explained.

CHAPTER 3

CHALLENGES OF DRIE

This chapter explains the challenges ant the mostly faced problems during DRIE process. Section 3.1 provides an introduction of this chapter. Section 3.2 explains the aspect-ratio-dependent etch rate problem, together with its reasons and suggestions. Section 3.3 explains the loading effect, including a comparison with ARDE. Section 3.4 discusses the notching effect, appearing for SOI structures. Section 3.5 explains the scalloping and grassing problem. Finally, Section 3.6 concludes the chapter by summarizing the problems faced during deep reactive ion etching process.

3.1. Introduction

Deep reactive ion etching of silicon using Inductively Coupled Plasma (ICP) sources and Bosch etching processes have unleashed a wave of new high aspect ratio microdevices. However, in etching of high aspect ratio features, researchers have encountered several problems [66].

First problem is the aspect ratio dependent etch (ARDE) rate, which refers to the etch rate of narrower trenches or smaller diameter holes is slower than that of wider trenches or larger diameter holes [67]. This is caused by the depletion of etching ions and radicals or inhibiting neutrals during their trench passage [49].

Second problem that will be explained in this chapter is the loading effect, which refers to a local dependence of etch rate on pattern area density. The closer those patterns are packed or the greater the area to be etched in a given region, the slower the etch rate [66].

Another problem faced during silicon etching up to an insulator layer is the notching effect. When the etch depth reaches to the insulator layer, the positive charge is accumulated at the bottom of the etched trench and the incoming ions are deflected by Coulombic repulsion to the lower part of the sidewall, where the passivation layer is thinner than in the upper sidewall [49]. As a result, at the interface of the silicon and insulator layer, silicon is etched laterally, which is called notching.

The last problem discussed in this chapter is the scalloping and the grassing effect. Alternating nature of passivation and etching generates a periodical peak and valley [68] on the sidewalls and this periodical structure is called scalloping. Grassing occurs due to high rate of passivation or low rate of platen power. Summary of these effects are shown in Figure 3.1.

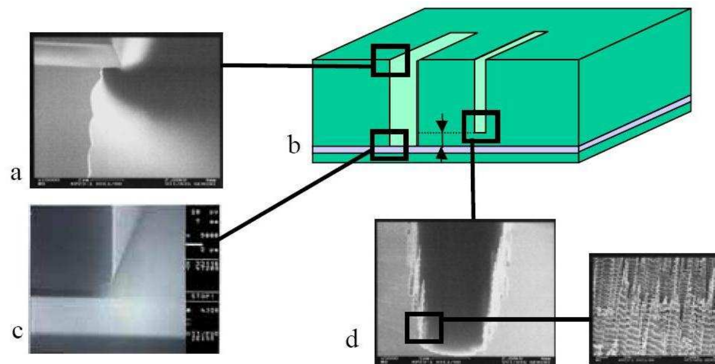


Figure 3.1: Typical features of the Bosch process: a) mask undercut and scallops, b) aspect ratio dependent etch rate, c) notching, and d) grassing [49].

3.2. Aspect Ratio Dependent Etch Rate

Decrease in etch rate for narrow trenches with increasing aspect ratio is called the aspect ratio dependent etching (ARDE) or RIE lag. The etch rate reduction is due to decreased transport of reactive species in the narrow and deeper features, and this results in a change of the chemical balance inside the feature [47].

The ARDE effect depends on the pattern geometry and process parameters, such as mask opening, step time at etching and passivation steps, coil power, gas pressure and gas flow according to analysis from experimental results. Figure 3.2 shows the SEM cross section image of an etched wafer containing the ARDE effect on different sized openings, starting from 0.8 µm to 4.4 µm with a step size of 0.2 µm.

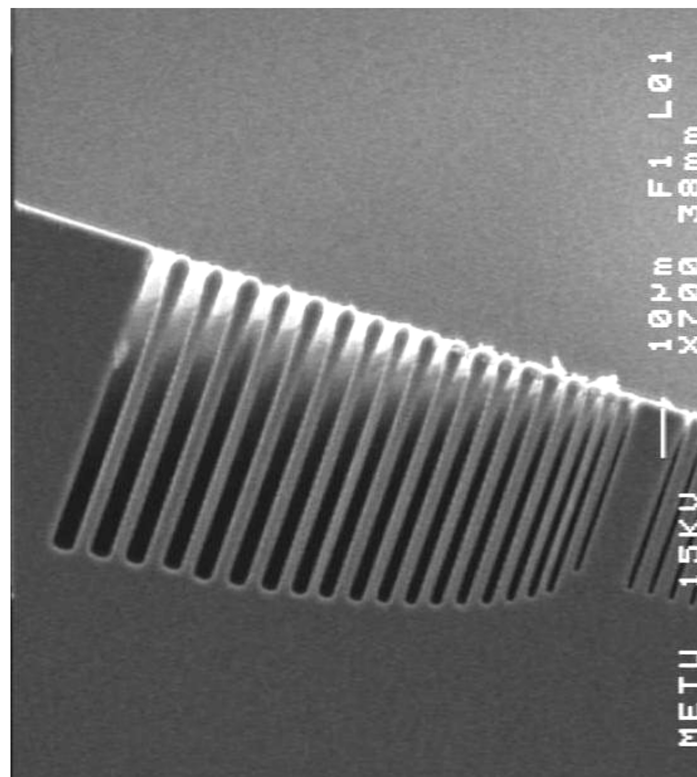


Figure 3.2: ARDE effect, etch rate differs with different sized opening.

The ARDE effect in plasma etching has been attributed to a wide range of physical mechanisms. The reasons of this effect are discussed widely, such as the Knudsen transport of neutrals, meaning that each reactant molecule reflects off a feature's sidewalls and can only react with a bottom of a feature [69, 70], ion shadowing, neutral shadowing and differential charging of insulating microstructure [49, 69, 71].

The main mechanisms for aspect ratio dependent etching were studied in the past and it is found that, differential charging of insulators, field curvature near conductors, image force deflection, ion shadowing with ion angular distribution, radical/inhibitor shadowing, molecular flow, bulk diffusion, and surface diffusion [49] are the main mechanisms for the ARDE effect [72].

Coburn and Winters [73] introduced a simple conductance model based on Knudsen transport of particles in etched trenches, where the molecular flow conductance limits the etching species arriving at the bottom of the feature. They derived the following equation for the ratio of the etch rate at the bottom of the feature R(A) to the etch rate at the top of the feature R(0):

$$R(A)/R(0) = K / (K + S - K \cdot S) \qquad 3.1$$

where S is the reaction probability on the bottom surface and K the molecular flow transmission probability for a given tube or trench. A is the aspect ratio: depth/diameter for a circular hole or depth/width for a long trench. Figure 3.3 shows the molecular behavior with Knudsen transport meaning that each reactant molecule reflects off a feature's sidewall and can only react with the bottom of a feature.

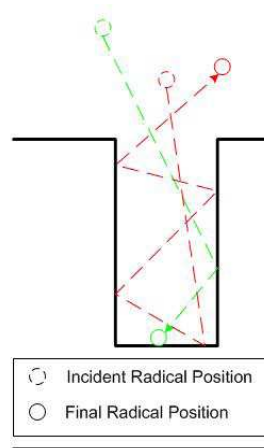


Figure 3.3: Illustration of molecular behavior with Knudsen transport [69].

3.3. Loading Effect

Decrease in the etch rate with increasing etchable area is called the loading effect, and it is an important source of etch depth nonuniformity. It is caused by the depletion of reactant species [49] and can be reduced by decreasing the etch rate, increasing the supply of reactants or by better control strategies [73, 74, 75].

A general model for the effect of loading on etch rate was developed by Mogab [74].

$$ER = (\beta\tau G) / (1+\beta\tau A_w d/V) \qquad 3.2$$

where β is the proportionality factor describing the affinity of the material being etched (silicon) to active species (fluorine), τ is mean lifetime, G is the generation rate of active species in plasma, d is a constant containing constants of chemical reactions and materials being etched, Aw is the etchable area, and V is the plasma

volume. It is known that time-domain multiplexed deep silicon etching suffers from serious loading effects typical to reactant transport-limited chemical etching.

Single wafer etch processes must be characterized for various pattern effects: macroloading, where etch rate depends on etchable area on the wafer scale and microloading, where etch rate depends on etchable area on a chip or feature scale. In the ion activated, surface reaction limited, regime etching is less prone to loading effects than in mass transport limited regime [69, 70]. The effect is extremely severe in high etch rate processes where chemical etching is the main etch mechanism. Especially the switched process with isotropic etching of silicon by fluorine is especially prone to the loading effect.

A macro scale loading effect is, because of the reactor geometry, that fluorine starvation is more severe at the center of the wafer than at the edges. This leads to non-uniformity of the etch rate at high etchable areas, and the edges are etched faster than central parts of the wafer [49].

Jensen and by Rickard and McNie [76] found that normal microloading behavior can be turned into inverse microloading by process conditions: with high fluorine flows it is possible to shift the etching to an ion-limited regime where fluorine starvation does not cause a loading effect [77].

Figure 3.4 shows another effect of the loading on small scale. The bottom of the etched feature is concave for narrow features and becomes convex for wider trenches. The convex bottom [78] is a result of local depletion of the etchant species at the center of the large area feature, while narrower features exhibit the normal ARDE behavior [49].

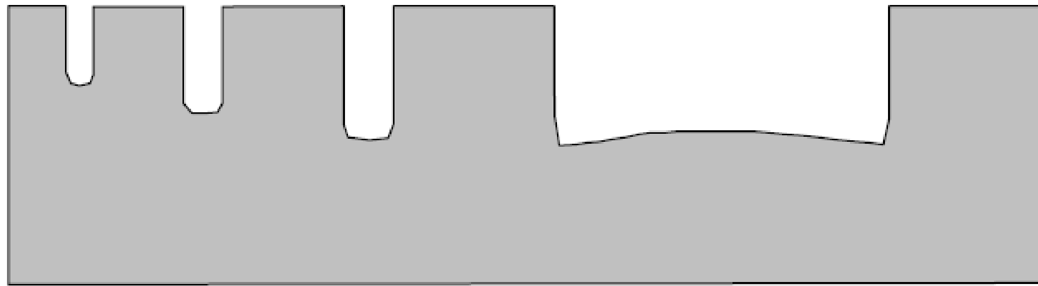


Figure 3.4 : Schematic presentation of appearance of the aspect ratio dependent etch rate and loading in a large feature [49].

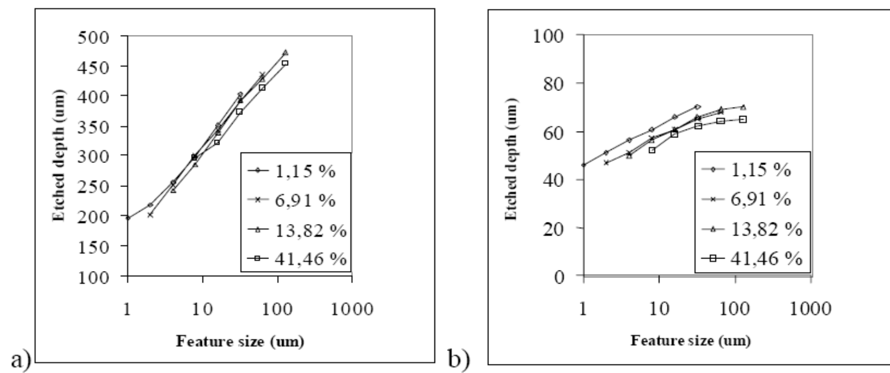


Figure 3.5: A comparison of the ARDE and the loading effect. a) Feature size effect dominates over loading, b) Microloading and feature size effect both affect etched depth [49].

The terms RIE-lag and microloading are often used interchangeably even though they are two are different phenomena. However, sometimes it is difficult to determine which effect is the dominant one [70]. A comparison of the ARDE and the loading effect is shown in Figure 3.5. For long etch times and high aspect ratio the ARDE has a stronger effect on etch depth non-uniformity than loading [49, 70].

3.4. Notching

During etching a conductive layer on an insulating layer, the accumulated charge is discharged until the insulator layer is reached. When the positive charge is accumulated on the bottom of the etched trench, the incoming ions are deflected by Coulombic repulsion to the lower part of the sidewall, where the passivation layer is thinner than in the upper sidewall, leading to silicon undercut at the interface [49].

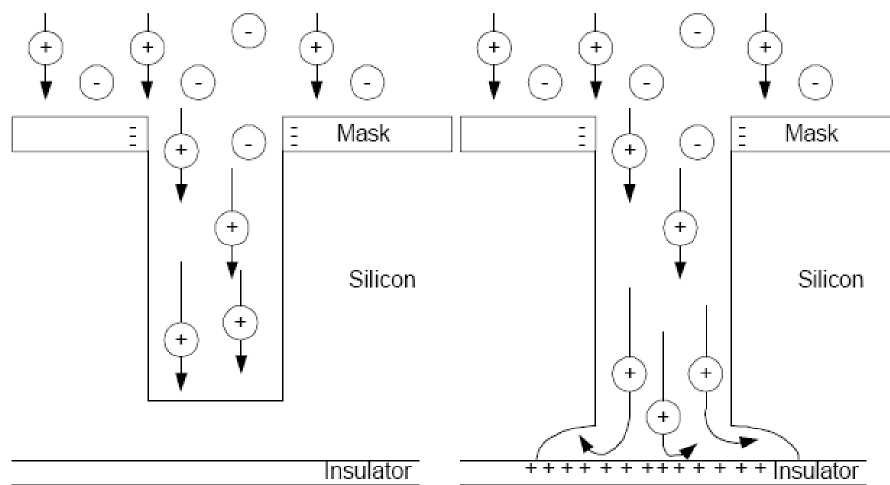


Figure 3.6: Charge distributions in deep trench and positive charge accumulation at Silicon- insulator interface resulting in lateral undercutting at trench foot (notching) [79]. Figure 3.7 shows the effect of notching for a SOI type wafer etching.

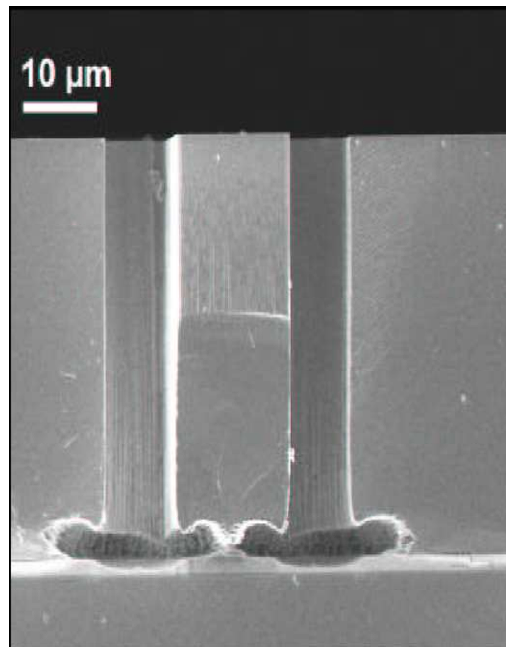


Figure 3.7: The effect of notching for a SOI type wafer etching [47].

The notching dependents on both the amount of charging and the over-etch time. There are two ways to avoid notching: either to prevent the charge accumulation during etching or to stop precisely at the time when the insulating layer is reached. Both of them are practically impossible. There is probably no way to totally eliminate charging in a plasma etching process, which relies on ions to etch the passivation layer and ion-assisted silicon etching. It is not likely that zero over-etch would be possible because of various etch rate non-uniformities. The remaining solutions are reduction of charging during the etching process and reduction of the etch rate non-uniformities by mask design rules.

A solution to minimize notching for SOI etching is to use a separate pulsed low frequency (LF) generator (380 kHz) for biasing the platen. This method is developed by STS [37]. On the STS tools, notching has been overcome by placing an additional low frequency power supply on the wafer chuck to let the substrate

discharge by allowing the ions to escape more easily from deep trenches when the etching cycle is done. As a result, the over-etch sensitivity decreases, and the notching or footing of silicon structures is minimized. . Figure 3.8 shows the reduced notching effect by using STS SOI feature.

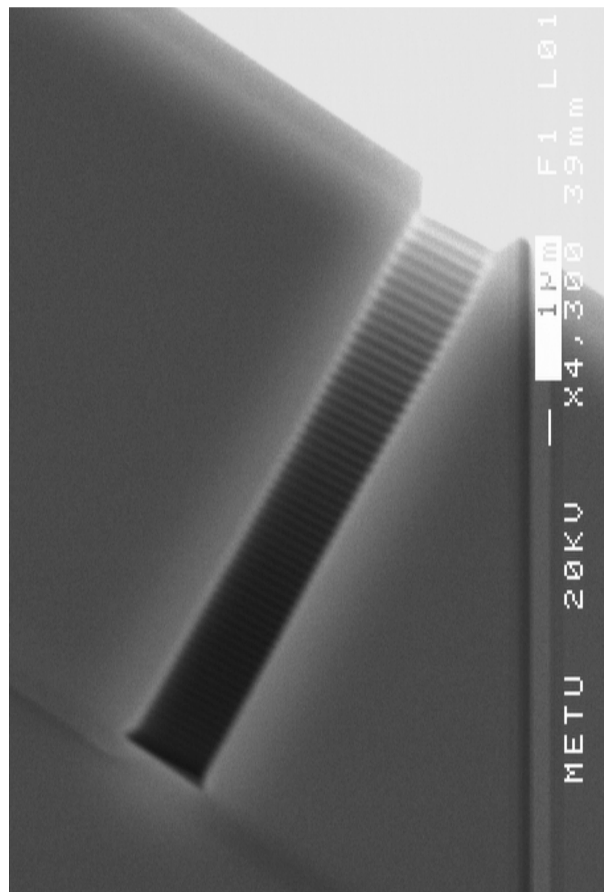


Figure 3.8: SEM image of an etched SOI wafer with STS SOI feature where the notching effect is reduced.

Another solution for preventing the notching in through wafer etching, where a handle wafer must be used both to protect the chuck from the incoming ions and to prevent the helium leak into the chamber, is to use aluminum stop layers, which have

been used successfully as they do not charge up and can be easily removed afterwards [79]. On the other hand, buried aluminum layers would not be feasible for electrostatic devices, unless they were subsequently oxidized, since they would cause short circuits throughout the substrate. An oxidation would also enhance the chemical strength of the layer. Alternatively, a silicon-aluminum-pyrex-aluminum configuration could be used, but both options would require some process optimization. Figure 3.9 shows the removed notching effect for through wafer etching by using aluminium layer at the back of the wafer [47].

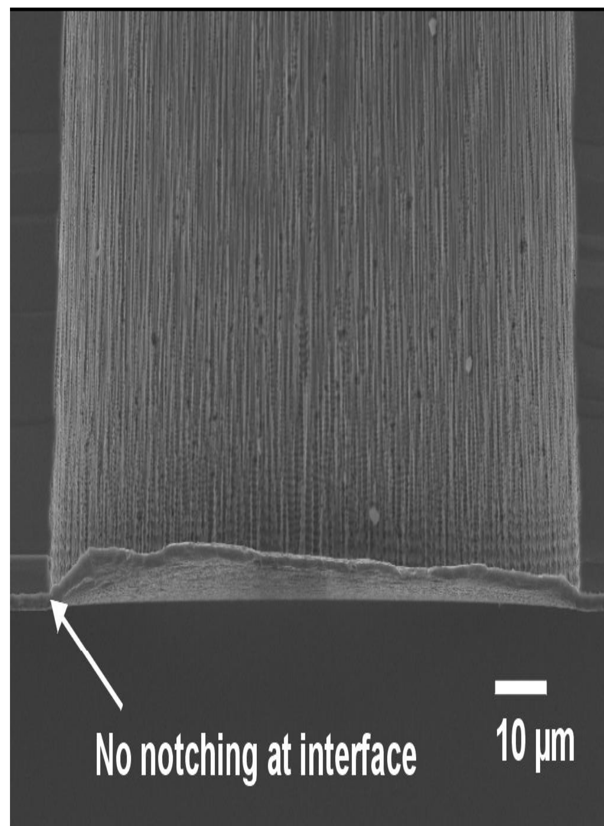


Figure 3.9: No notching at a silicon/aluminum interface [47].

3.5. Scalloping and Grassing

Nature of the Bosch process produces scallops on the sidewalls due to the alternating etch and passivation steps. Scallop size can be important for some applications where the surface roughness is critical or the trench size is comparable to the scallop size.

A straight forward method to decrease scalloping is reducing the etch step time, since scalloping comes from the cyclic etching of the silicon. Figure 3.10 shows the effect of scalloping on the sidewall of the opening and Figure 3.11 shows the close view of this effect.

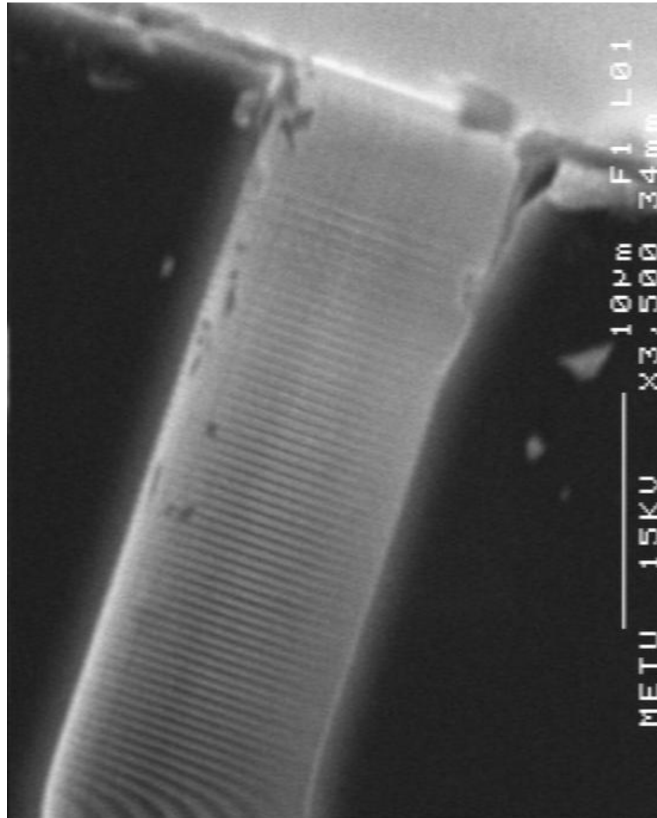


Figure 3.10: Scalloping effect on the sidewall of a trench due to nature of Bosch process.

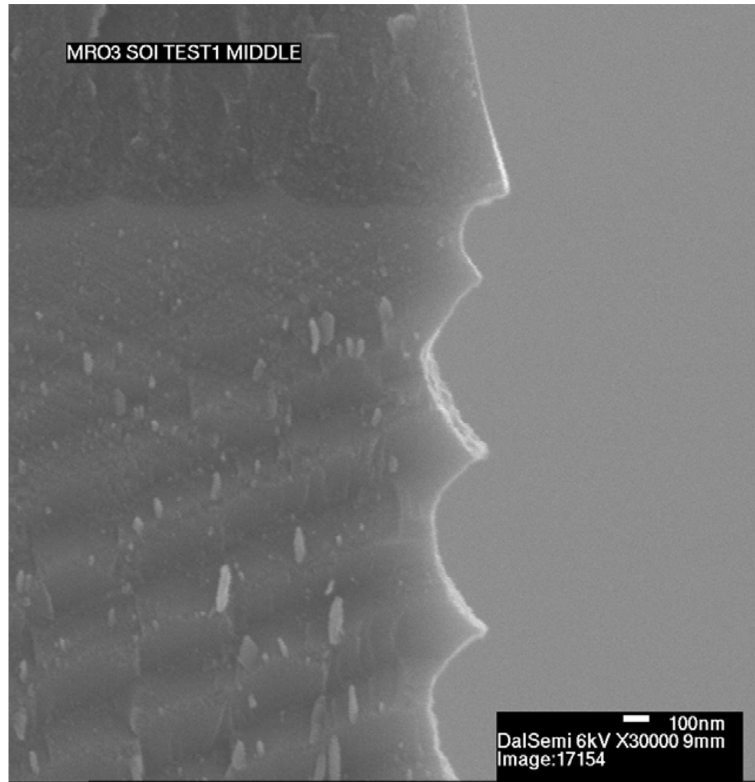


Figure 3.11: Close image of the scalloping effect on the side wall [50].

The grassing is another problem observed at the bottom of the larger trenches due to insufficient etching radicals in the etch step or too much passivation deposition in the passivation step as shown in Figure 3.12. Also micromasking, oxide or mask residues cause grassing. This problem can be reduced either by increasing the platen power, or reducing the passivation components.

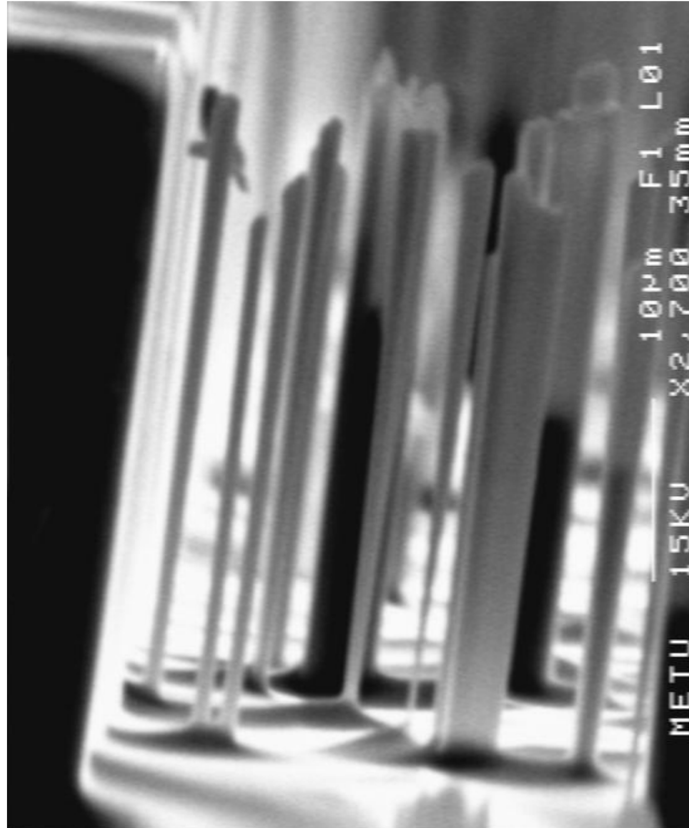


Figure 3.12**:** Grassing at the bottom of a trench due to insufficient platen power.

3.6. Conclusion

This chapter explained the most common problems faced during DRIE process. Some problems occur due to the cyclic nature of the Bosch process and some of them come with the nature of plasma etching.

The ARDE effect is one of the most commonly faced problem during etching a wafer with a layout containing different size of openings. Due to decreased transport of reactive species in the narrow and deeper features, etch rate differs.

Nonuniformity in the etch rate for large etchable area is called the loading effect. This problem occurs due to the depletion of reactant species in large areas and it can be reduced by decreasing the etch rate or increasing the supply of reactants.

The notching effect is another problem faced during etching silicon up an insulator layer. Due to positive charge accumulation on the insulator, incoming ion will be reflected to the bottom of the sidewall. As a result sidewall passivation at the bottom will be removed and silicon will be etched from the bottom of the sidewall. Some solutions to reduce the notching effect have been developed like the one developed by STS company. Using a low frequency RF bias, 380 kHz, will let the substrate discharge by allowing the ions to escape more easily from deep trenches and resulting reduced notching.

Scalloping and grassing are the last common problem explained in this chapter. Scalloping occurs due to the cyclic nature of Bosch process, since in the individual etch steps, silicon is etched isotropically. Reducing the etch step time, decreases the scallop size. And finally insufficient platen power or too much passivation causes grassing. Increasing the applied platen power or reducing the passivation prevents the grassing problem.

CHAPTER 4

OPTIMIZATION PROCESSES AND THE RESULTS

This chapter explains the procedures developed for the optimization of the processes to obtain 20 µm and 100 µm depths for 1 µm trenches. 4.1 is the introductory part of this chapter. Section 4.2 gives information about the etch system, STS-ASE^{HRM}, configuration. Section 4.3 briefly explains the wafer preparation procedure for dissolved wafer process before the etching is done. Individual parameter effects and the results of the processes for the 1 µm openings are discussed. Section 4.4 explains the wafer preparation procedure to obtain 100 µm depth for 1 µm opening. Effects of all parameters and results of the processes are also explained in this section. Finally, Section 4.5 concludes the chapter by summarizing the optimization processes and obtained results.

4.1. Introduction

The concerns of deep silicon etching mainly include the etch rate, side-wall profile or roughness, bottom roughness or uniformity and selectivity of the masking material. Those are influenced by process parameters such as coil power, platen power, process pressure, step time, gas flow rates, substrate temperature and distance from the source plasma. Therefore, a variety of parameters must be optimized to fulfill a specified etching requirement.

In the dissolved wafer process (DWP), the aim of the optimization is to obtain 20 μm depth for the minimum feature size, 1 μm, with a vertical sidewall and minimum undercut.

Second part of the optimization process is to obtain high aspect ratio structures, >100:1, with the same pattern used in the DWP. Figure 4.1 shows the drawing of the layout used for optimization of the processes and Figure 4.2 shows the pattern analyzed to see the effects of the parameters on the trenches.

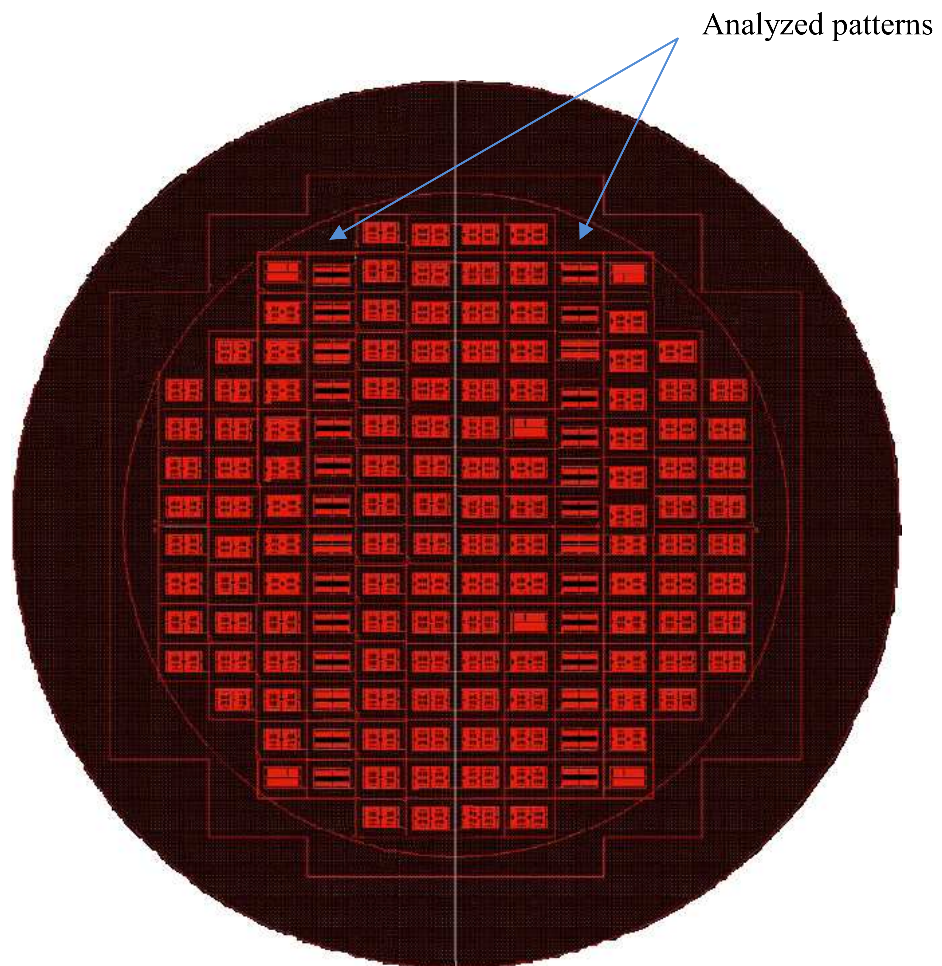


Figure 4.1: The layout used for optimization processes.

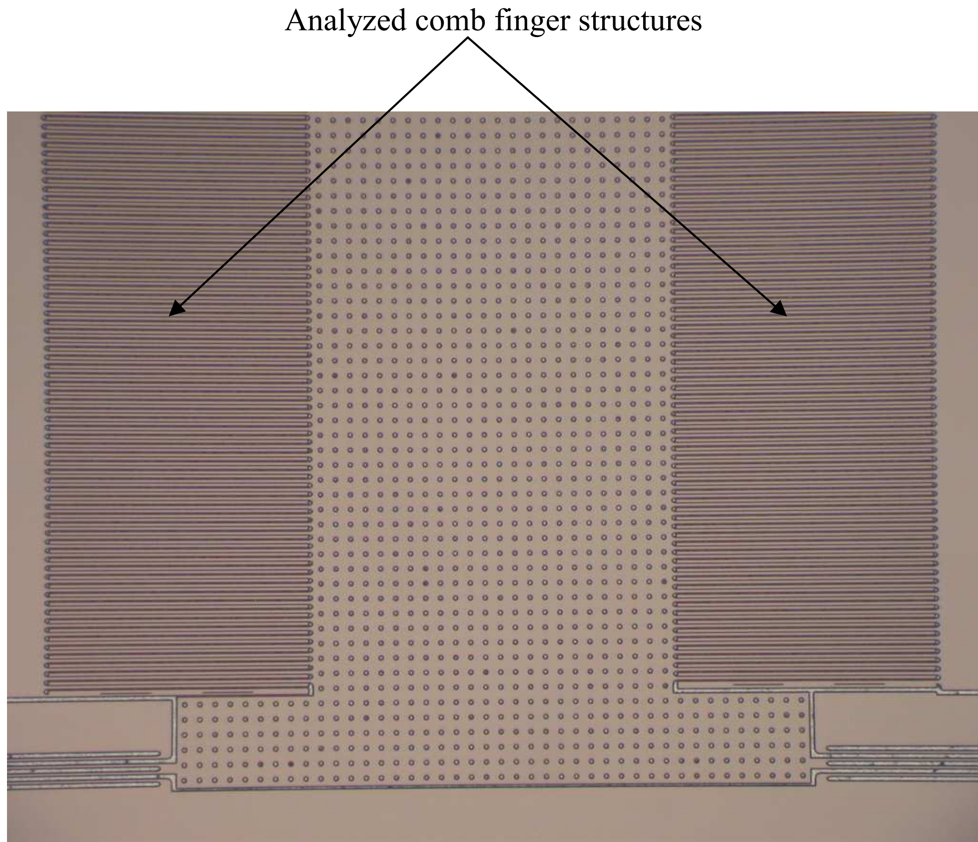


Figure 4.2: The pattern analyzed to see the effects of the parameters on the trenches.

In general, there are three ways to achieve high aspect-ratio trench. First of all reducing the step time of the plasma gases while keeping the step time ratio of etching to passivation constant will reduce the sidewall roughness by decreasing the isotropic etch time at the bottom of the trench before the next passivation step protects the sidewall.

Second, reducing the chamber pressure will increase the mean free path between the plasma ions and improve the directionality of energetic ions toward the target surface. However, reducing the chamber pressure below a certain point will also decrease the total number of plasma ions available in the chamber. The ions may recombine before they have a chance to reach the target, and no etching will occur.

Third, increasing the platen power will intensify the plasma ions density and energy, and improve the directionality of the plasma reactive particles. Moreover, this will also enhance the availability of plasma species at the bottom of a trench when the opening is too narrow for the plasma to get inside. However, too much increase in platen power will cause bowing in the trench profile [34] and also decrease in selectivity.

4.2. System configuration

The etch module, STS ASE^{HRM}, includes two independently controlled RF power sources, one for the inductive coupling coil (13.56 MHz) on the top of the etching chamber to create plasma; and the other power source connected to the wafer electrode to control the RF bias potential of the wafer with respect to the plasma, can be operated at a frequency of 13.56 MHz or 380 KHz. The electrode is kept at a fixed temperature and can be set any value between -20^oC to 20^oC to maintain a constant wafer temperature. Backside helium pressure is used to provide improved heat transfer between the wafer and the electrode. A set of eight alumina fingers clamped the wafer to the electrode to prevent the helium leak from backside of the wafer to chamber and to increase the contact area of the wafer to the electrode. The wall temperature is set to 120 °C. It is set at this level to enable good wafer to wafer repeatability by stabilizing the temperature of the system. The cartridge heaters are set to 130 and 150 °C for the confinement chamber and inserts. The chamber is pumped out to a low pressure, typically 10^{-7} Torr, by a turbomolecular pump, which is backed by a dry pump. The gas flow rates are regulated by mass flow controllers and the chamber pressure is controlled by an automatic pressure control valve which can be set to any value between 100% closed to 0% closed, independently in each step. SF_6 is employed with a flow rate in the range of 0–300 sccm in etch cycle. The

flow of C_4F_8 for passivation was varied between 0 and 160 sccm. Detailed configuration of the system is shown in Table 4.1.

Table 4.1: Specifications of the system used in optimization process.

Parameters	Ranges
Step Time (s)	0 to 30
SF_6 Flow (sccm)	0 to 600
C_4F_8 Flow (sccm)	0 to 300
Pressure (mTorr)	0 to 949
Coil Power (Watt)	0 to 3000
Platen Power (Watt)	0 to 300
Electromagnet (A)	0 to 10
Electrode Temperature (^oC)	-20 to 20
He Back Cooling(Torr)	5 to 19000

4.3. Wafer and Etch Mask Preparation for DWP

4-inch p-type silicon test wafers with resistivity ranging from 1 Ω - cm to 5 Ω - cm, 475-575 μm thick and (100) orientation were used in our study. The photoresist S1813 were coated at 4000 RPM (thickness ~1.3 μm) and softbaked at 115 ^oC for 60 seconds. Samples were exposed using mask aligner, EVG 620 Precision Alignment System, developed with MF319 for 1 minute before ICP etching was carried out.

Four variables were studied for the optimization process: Step times, automatic pressure control (APC) valve position, platen power, and electrode temperature on the original recipe given in Table 4.2.

Table 4.2: The recipe used for the starting point.

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	88.2% ≈ 40 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
Electromagnet (A)	Off	Off
Electrode Temperature (^oC)	10	
Process Height (cm)	22	
Process Time (min)	15	

4.3.1. Step Times

In this part, effects of step times without changing their ratio are investigated. Different step times are applied and the effects on the etch rate, scallop size and profile angle are investigated.

Step times of 2 seconds, 3 seconds and 4 seconds are used in the experiments with a etch/passivation cycle time ratio of one for all. 1 second step times are observed to yield unreliable pressure, platen power and coil power, since the mass flow controllers and RF generators cannot be adjusted in 1 second. So 1 second etching and 1 second passivation times are omitted. Figure 4.3, 4.4, 4.5 show SEM image of the process results and the effects of these step times on the etch rate and profile angle as an average are shown in Figure 4.6 and Figure 4.7 with the recipe given in Table 4.2 for 2x2, 3x3 and 4x4 step times.

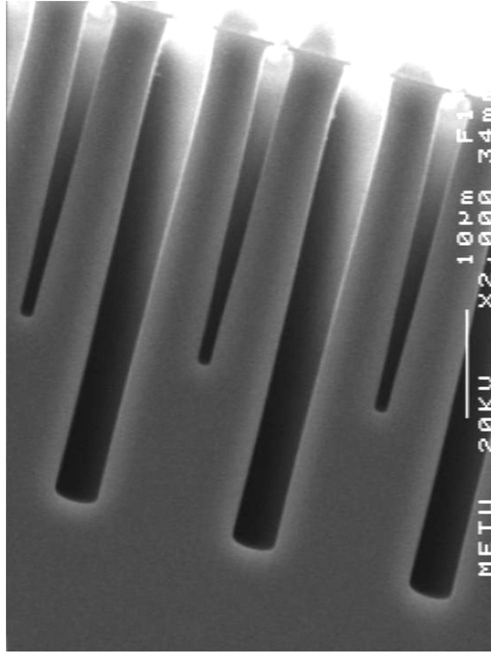


Figure 4.3: 2x2 step times, Mask undercut increases with the decreased passivation time. Recipe 1.4 given in Appendices A.

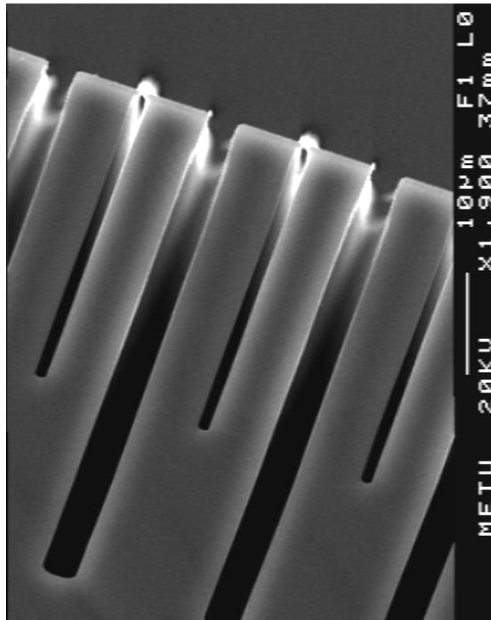


Figure 4.4: 3x3 step times, with the increased passivation time, sidewalls protected better. Recipe 2.4.

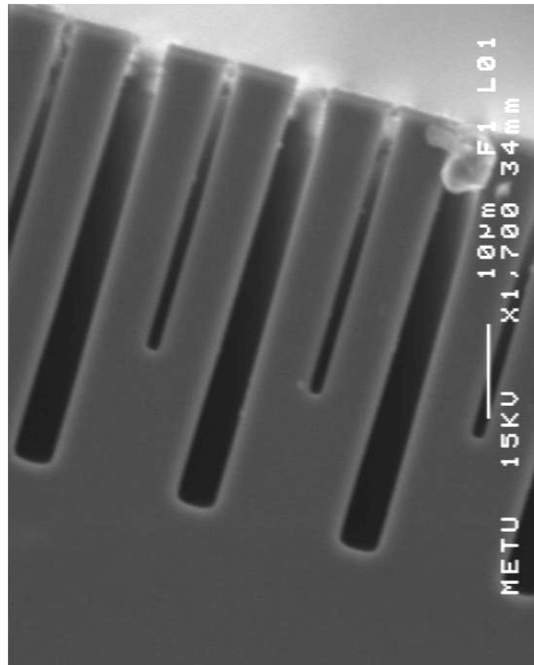


Figure 4.5: 4x4 step times, no mask undercut observed with the increased passivation time. Recipe 3.4.

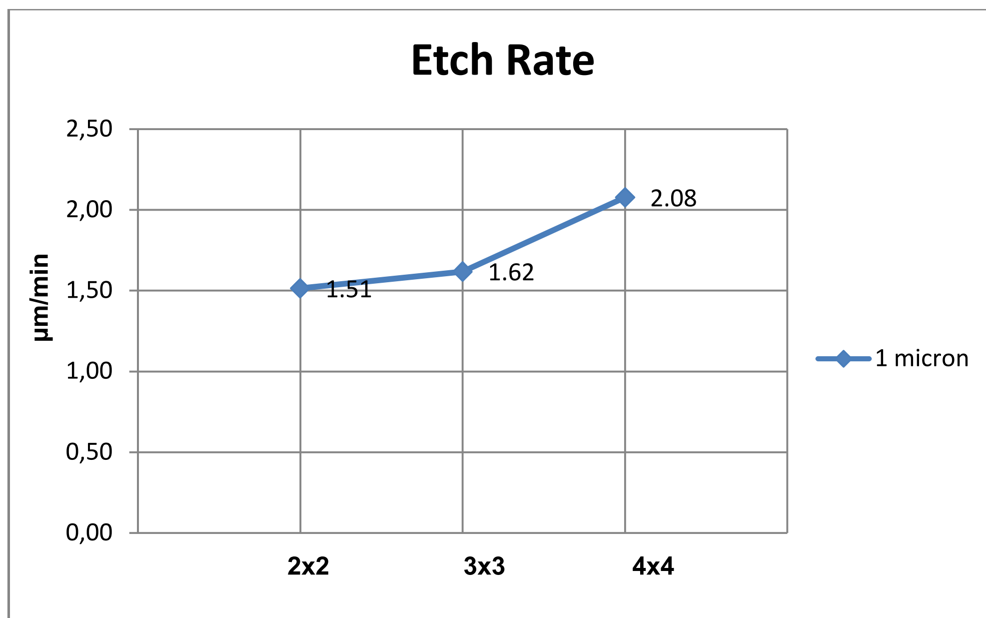


Figure 4.6: Etch rate dependence on the step time.

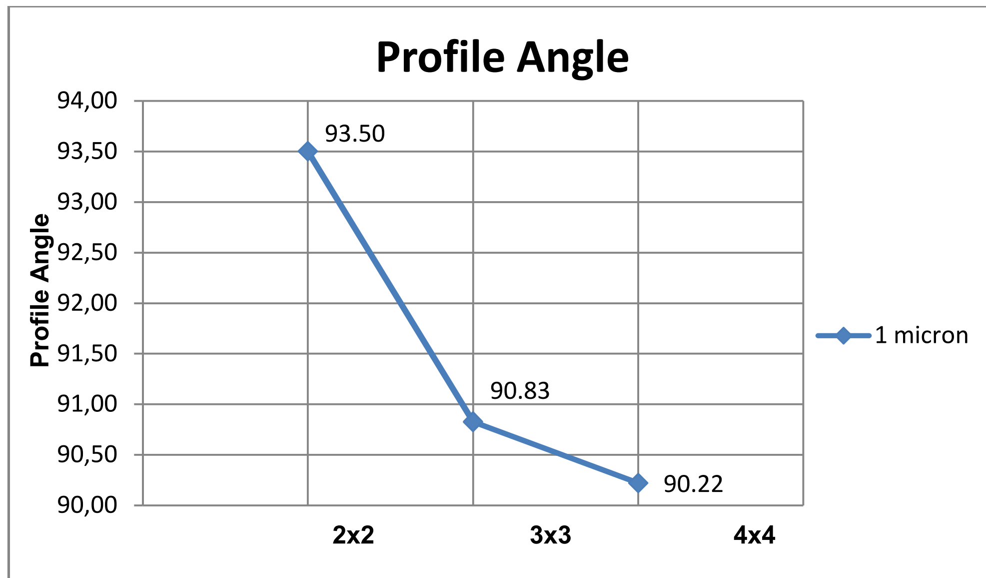


Figure 4.7: Profile angle dependence on the step time.

4.3.1.1. Comments:

Although reducing the etch step time reduces the scallop size, with the reduced passivation step time profile gets positive as shown in Figure 4.3. Since the passivation is not sufficient at low step times with the applied pressure, C_4F_8 flow and coil power, sidewalls are not protected well at the top of the openings. Because of insufficient passivation, trenches get larger and profile gets positive.

To overcome this problem either the passivation components must be increased such as step time, gas flow or coil power, or the etch step components must be reduced like platen power, coil power or gas flow. For the protection of the sidewalls more efficiently at the top of the openings for 2x2 process, C_4F_8 has been added to etch step. As a result mask undercut from one side of the 1 micron opening is reduced to 0.5 µm from 0.9 µm. New recipe is given in Table 4.3 and Figure 4.8 shows reduced mask undercut with the effect of the new recipe.

Table 4.3: The recipe developed to overcome the mask undercut problem for 2x2 process.

Parameters	Etch	Passivation
Step Time (s)	2	2
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	50 (-9 sccm / min)	80
Pressure (mTorr)	88.2% ≈ 40 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	10	
Process Time (min)	15	

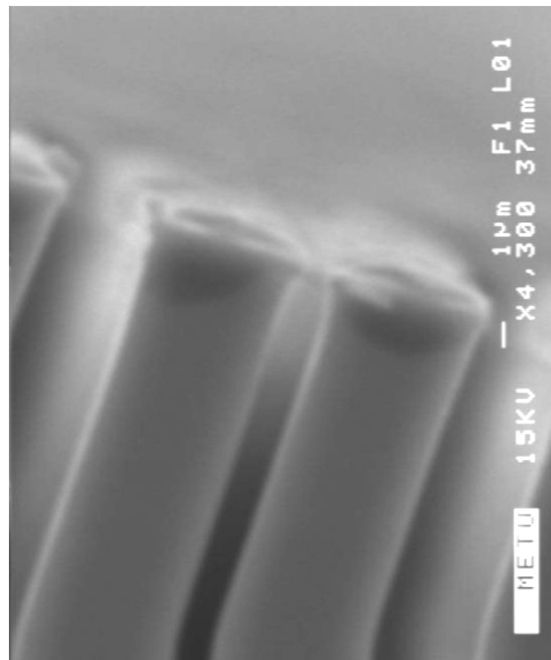


Figure 4.8: Improved results for the mask undercut problem with the addition of C_4F_8 in the etch step.

Step time also has a great effect on the etch rate as shown in the Figure 4.6. Increase in the etch step time also results in an increase in the etch rate. On the other hand, increase in the scallop size is observed when the etch step time gets higher. Since it is in the order of nanometers and not comparable with the minimum feature size, 1 μm, this problem is neglected in our optimization process.

4.3.2. Etch Step Pressure

In this part, effects of etch step pressure with different step times on the etch rate and profile angle are systematically explored. Although the process pressure of etch step depends on the APC value, SF6 gas flow rate and somewhat source power, only the APC value is used to change the pressure and the other values kept constant in this part of the optimization process.

In the experiment different APC values, pressures, for different step times are investigated. APC values 50%, 79.2%, 85.5%, 88.2%, 89.2% and the pressures respectively 12 mTorr, 20 mTorr, 30 mTorr, 40 mTorr and 50 mTorr for 2x2, 3x3 and 4x4 etch and passivation step times are explored. Since minimum pressure is 12 mTorr with the set gas flow, 400 sccm, 10 mTorr pressure cannot be achieved even with the decreased APC value.

The best results on the profile angle are obtained with the 4x4 step times. SEM images of 4x4 step times with different etch step pressure values are shown in Figure 4.9, 4.10, 4.11, 4.12, and 4.13 for 12, 20, 30, 40, and 50 mTorr and the effect of different etch step pressure with the individual step times on the etch rate and profile angle are shown on Figure 4.14 and 4.15 respectively.

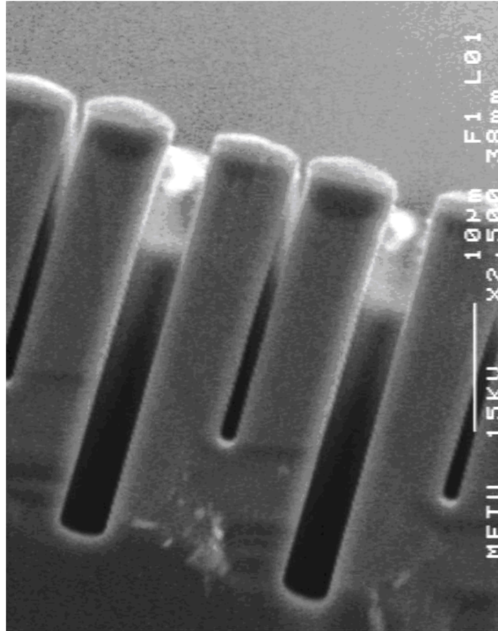


Figure 4.9: 12 mTorr etch step pressure, decrease in the etch rate with a good profile angle is observed at low etch step pressure. Recipe 3.1.

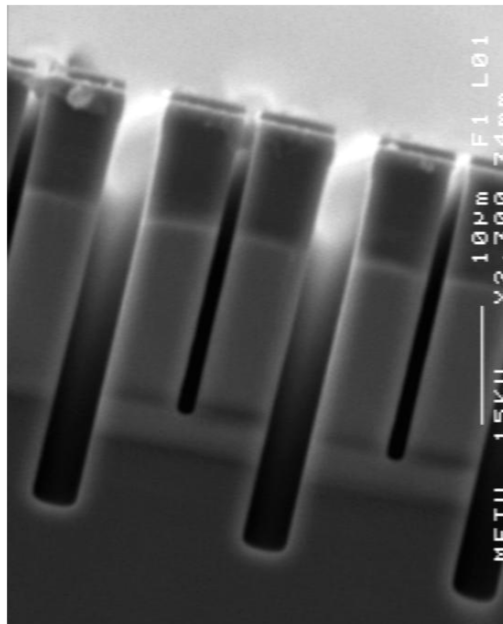


Figure 4.10: 20 mTorr etch step pressure. Recipe 3.2.

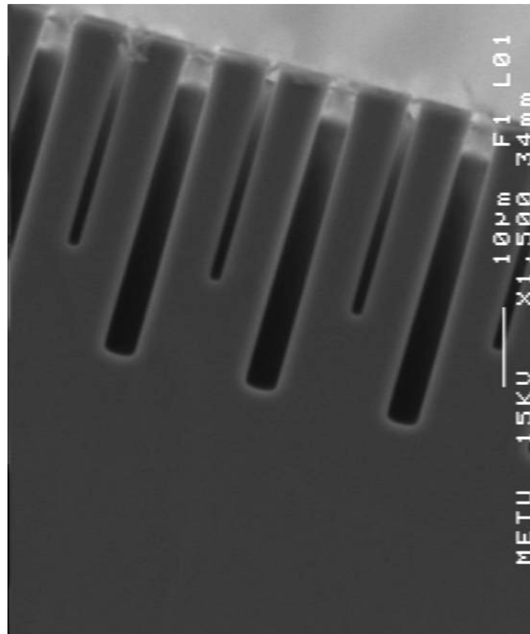


Figure 4.11: 30 mTorr etch step pressure. Recipe 3.3.

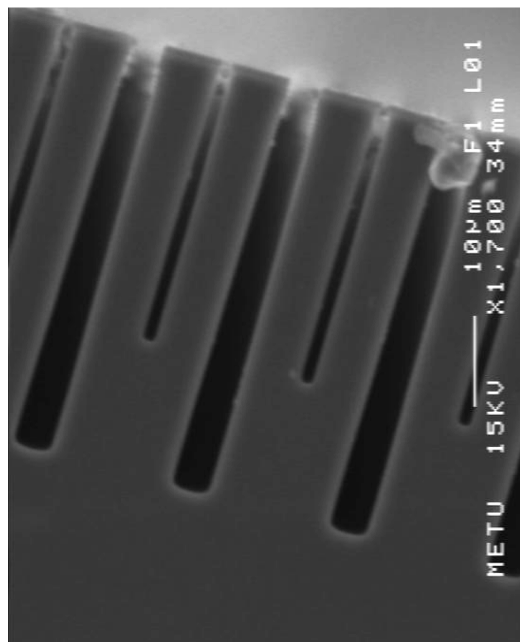


Figure 4.12: 40 mTorr etch step pressure, increase in the etch rate is observed at high etch step pressure. Recipe 3.4.

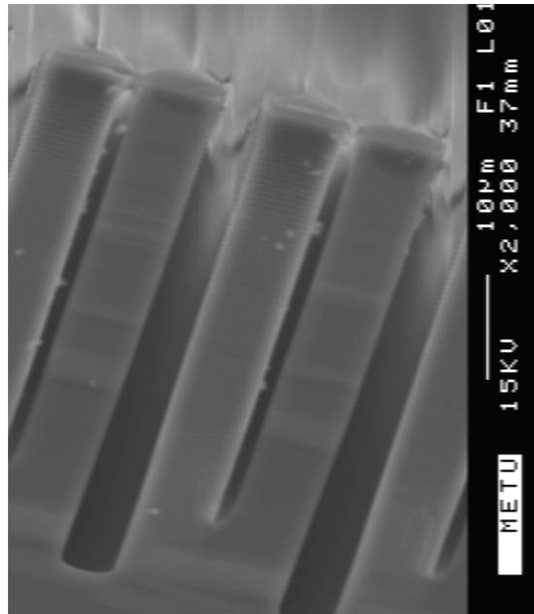


Figure 4.13: 50 mTorr etch step pressure, with the increased etch step pressure profile turns to positive values. Recipe 3.5.

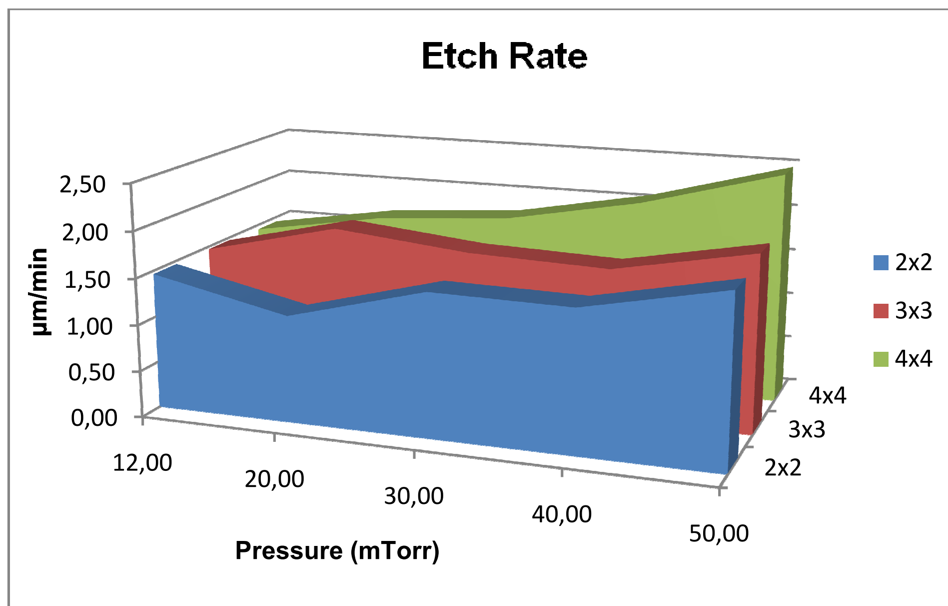


Figure 4.14: Effects of etch step pressure and step time on the etch rate for 1 µm opening.

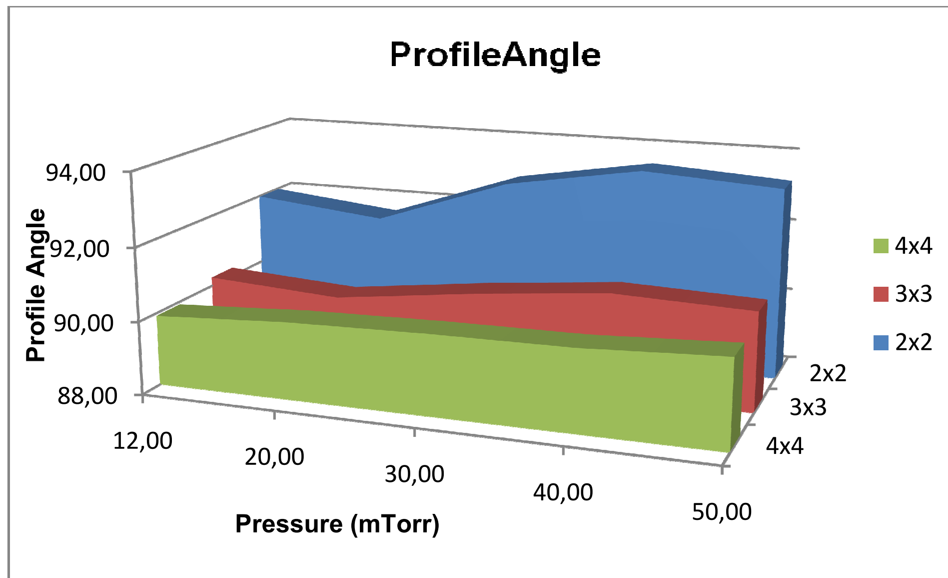


Figure 4.15: Effects of etch step pressure and step time on the profile angle of 1 μm opening.

4.3.2.1. Comments:

Since the available fluorine concentration increases with the increased pressure, etch rate also increases up to a point where the trench get deeper and collision of the ions becomes dominant. Figure 4.14 shows the relations of etch rate with step times and pressures. Pressure also has an important effect on the selectivity of the masking material. Since it is not so critical for this process, it is not investigated.

From the obtained results, it can be seen that profile angle also has a dependency on the etch step pressure. Increasing the pressure changes the profile in the positive direction. However this effect becomes more dominant when the etch and passivation times reduced. Figure 4.15 shows the relation of the profile angle with the step times and the pressure.

4.3.3. Platen Power

In this part, effects of platen power are investigated. Since the selectivity of the masking material is high at low frequency, platen power is used at low frequency, 380 KHz, and pulsed mode, 3ms pulse with 30% duty cycle. New recipe is chosen from the previous recipe given in Table 4.3 for 20 mTorr etch step pressure, given in Table 4.4.

20 watt, 45 watt 57.5 watt and 70 watt platen power in the etch step is applied with the recipe given below and the effects of these changes on the profile angle and etch rate are investigated. SEM images of the experiments are shown in Figure 4.16, 4.17, 4.18 and 4.19 for the given platen power values and Figure 4.20 and 4.21 show the platen power effect on the etch rate and profile angle respectively.

Table 4.4: New recipe to see the effect of platen power on the etch rate and profile angle.

Parameters	**Etch**	**Passivation**
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	10	
Process Height (cm)	22	
Process Time (min)	15	

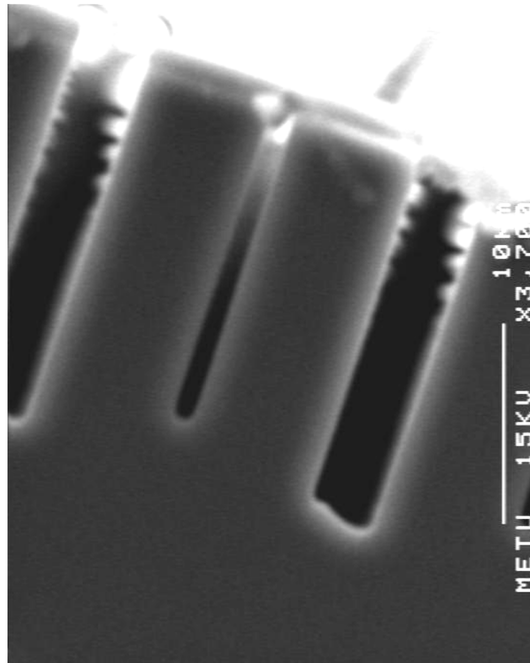


Figure 4.16: 20 watt platen power. Decreased etch rate due to low platen power. Recipe 4.1.

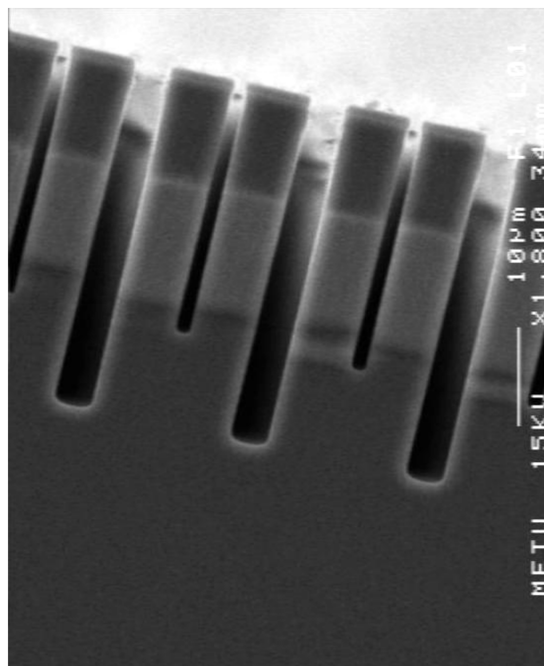


Figure 4.17: 45 watt platen power. Recipe 4.2.

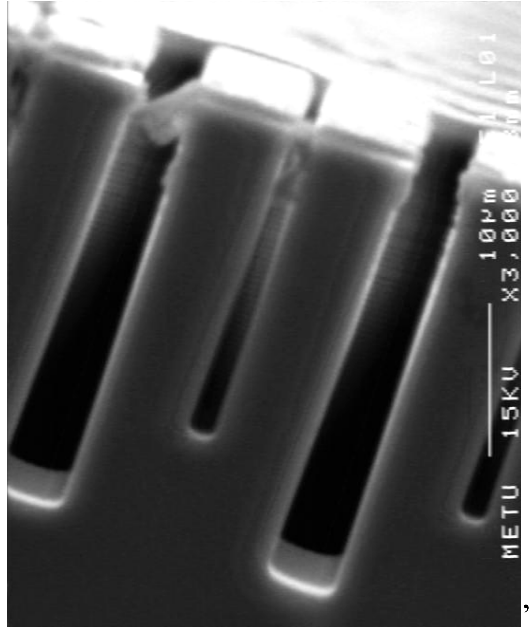


Figure 4.18: 57.5 watt platen power. Recipe 4.3.

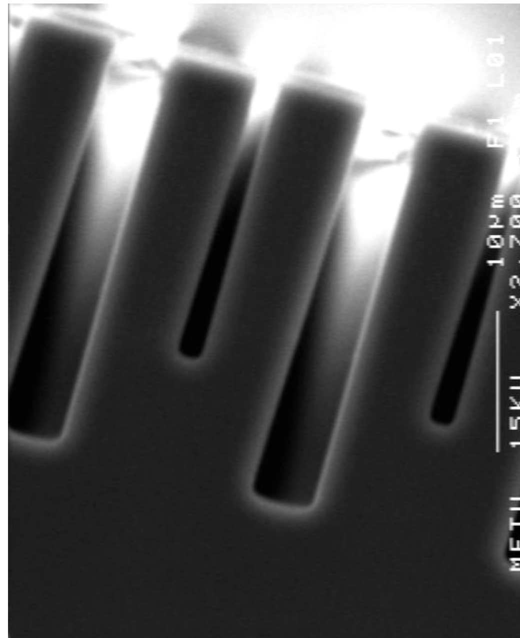


Figure 4.19 : 70 watt platen power. Trenches get larger through the bottom due to increased platen power. Recipe 4.4.

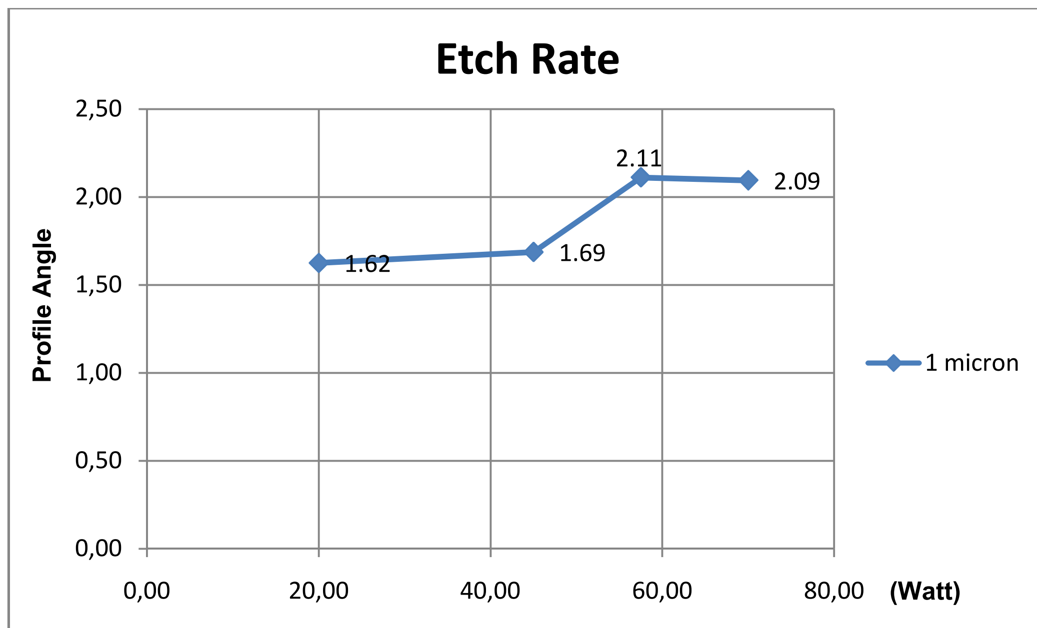


Figure 4.20: Effect of platen power on the etch rate.

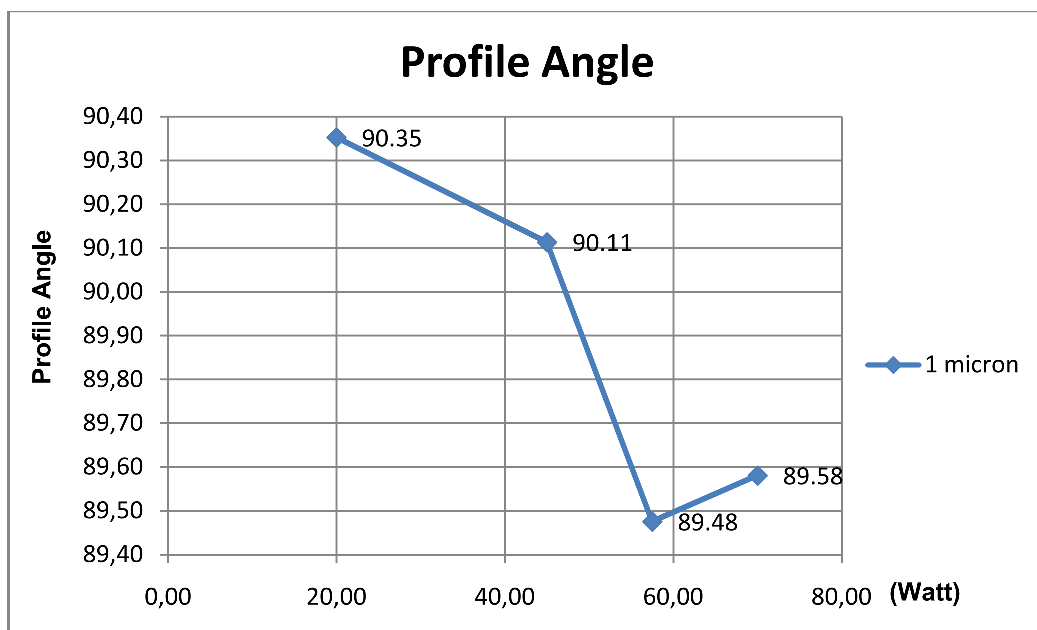


Figure 4.21: Effect of platen power on the profile angle.

4.3.3.1. Comments:

Table 4.20 shows that platen power has an important role on the etch rate, since it is used for removing the vertical component of the passivation. As the power increased, the time spent for removing the passivation is decreased and as a result, etch rate increases. Figure 4.20 shows the relation between the etch rate and the platen power. On the other hand, with the increased platen power, trenches get larger through the base of the opening.

In addition to my results, literature indicates that, although increasing the platen power increases the mask erosion due to increased ion energy and reduces the grassing at the bottom of the trenches [80].

4.3.4. Electrode Temperature

In the last part of the optimization process for dissolved wafer process, effects of electrode temperature are investigated. Starting from -20°C to 10°C with a step temperature 10 is applied to the recipe given in Table 4.5. Figure 4.22, 4.23, 4.24, and 4.25 show the SEM image of the processes and Figure 4.26 and 4.27 show the obtained results from these processes.

Table 4.5: The recipe used to see the effects of electrode temperature.

Parameters	**Etch**	**Passivation**
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-20 to +10	
Process Height (cm)	22	
Process Time (min)	15	

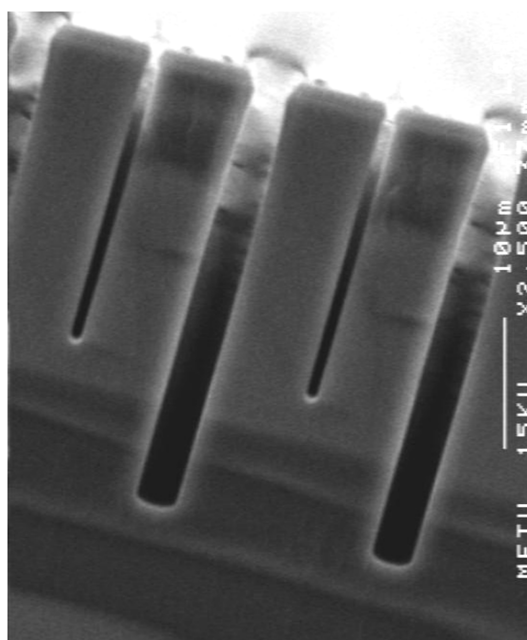


Figure 4.22: -20°C electrode temperature, decrease in the feature size is observed due to increased passivation at low temperature. Recipe 5.1.

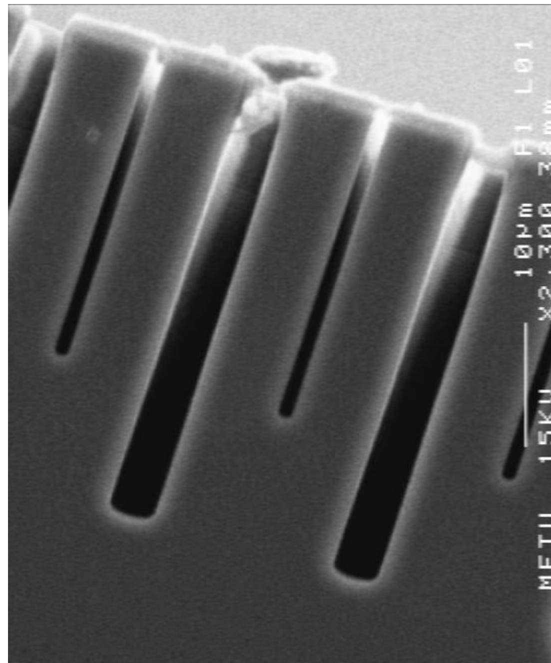


Figure 4.23: -10°C electrode temperature. Recipe 5.2.

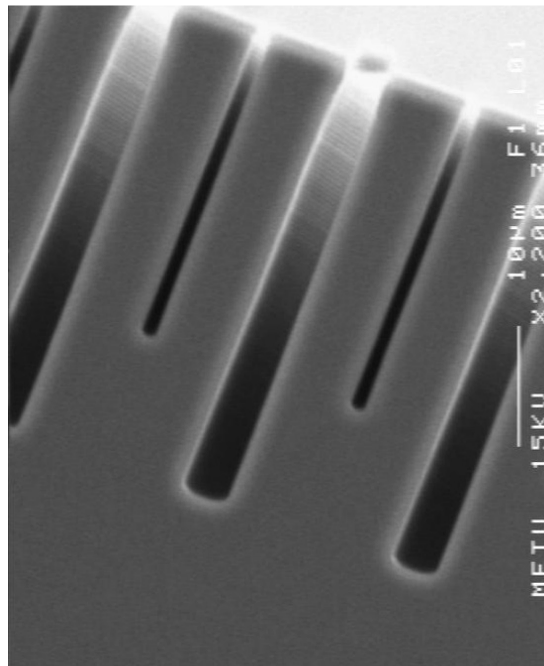


Figure 4.24: 0°C electrode temperature. Recipe 5.3.

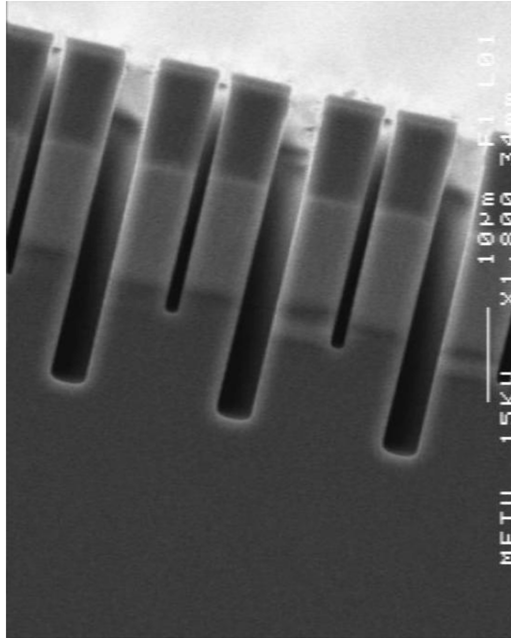


Figure 4.25: 10°C electrode temperature. No significant effect is observed on the etch rate within the range of -10 to 10°C electrode temperature. Recipe 5.4.

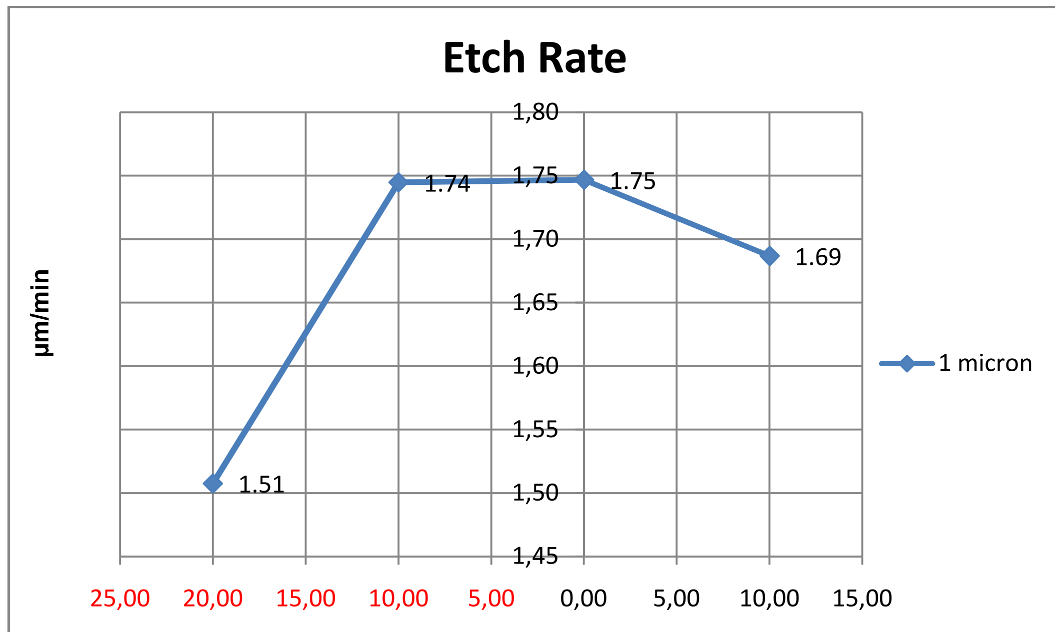


Figure 4.26: Etch rate dependence on the electrode temperature.

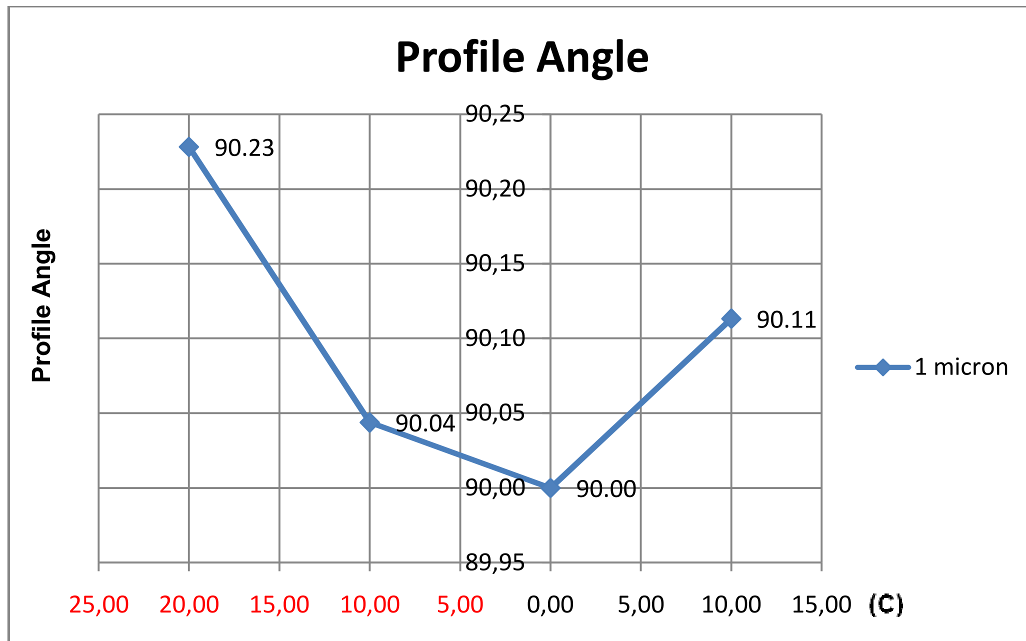


Figure 4.27: Profile angle dependence on the electrode temperature.

4.3.4.1. Comments:

Passivation rate increases with the decreased wafer temperature. At low temperatures, it is observed that the trenches get more tapered due to better sidewall passivation. On the other hand, ARDE effect becomes more dominant with the decreased temperature; etch rate decreases with respect to larger openings.

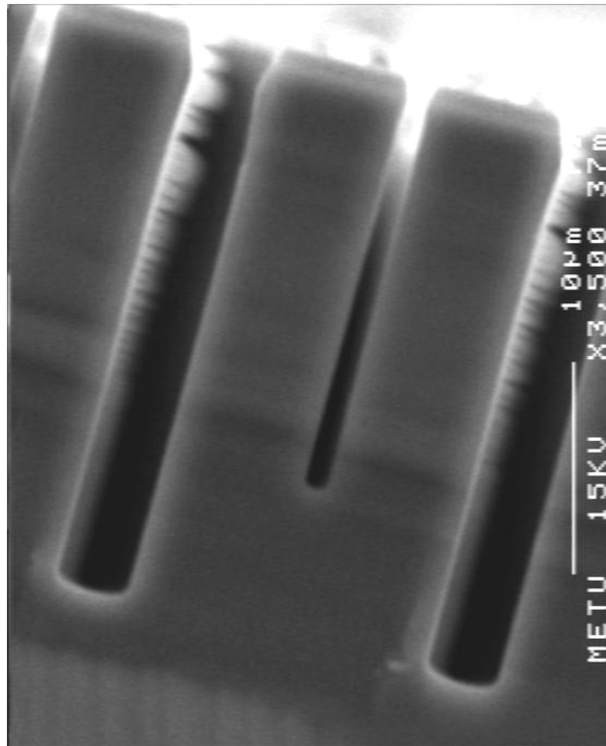
The recipe given below is applied to a wafer consisting of same structures with wide dicing streets to be etched. Wafer is prepared with the same manner of the DWP wafers and the layout, initial recipe, used for optimization, is given in Table 4.5.

Table 4.6: Starting recipe for the new mask having large openings.

Parameters	**Etch**	**Passivation**
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Height (cm)	22	
Process Time (min)	15	

Grassing is observed at the dicing streets. To solve this problem, platen power is increased. Starting from 45 watt to 60 watt with a step power 5 watt is applied.

SEM image of 45 watt and 60 watt platen power processes are shown in Figure 4.28 and 4.29. The effects of the processes on the etch rates and profile angle are shown in Figure 4.30 and 4.31.



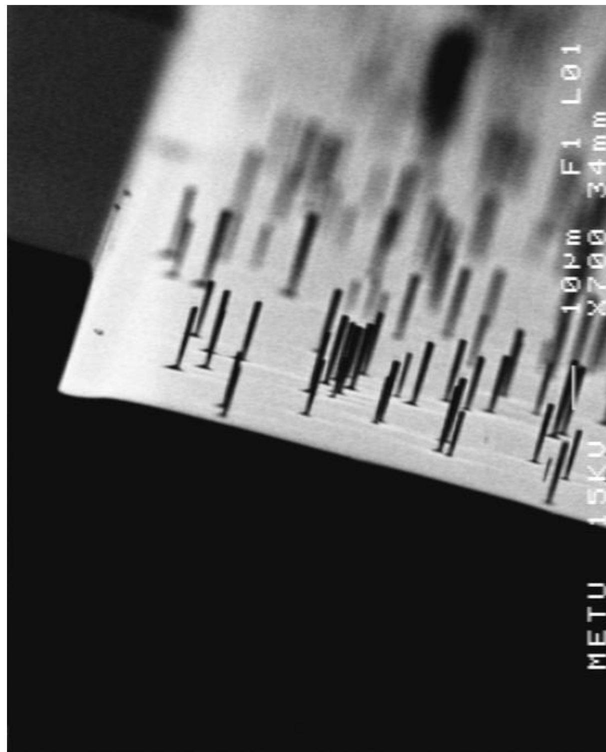
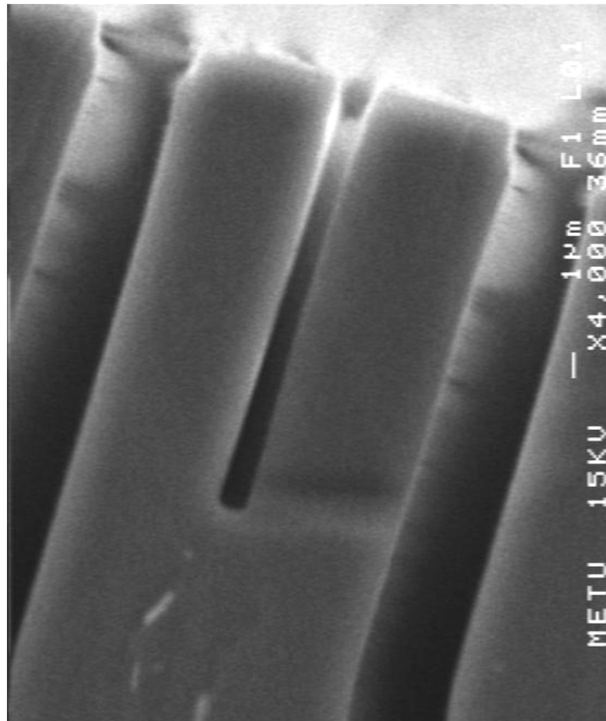


Figure 4.28: 45 watt platen power. Grassing at the dicing street due to insufficient platen power.



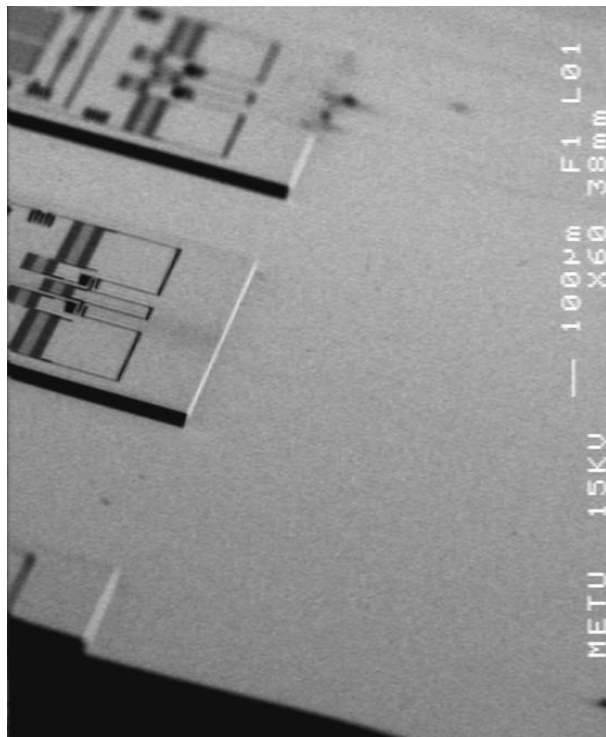


Figure 4.29: 60 watt platen power. With the increase platen power grassing problem solved without affecting the profile angle significantly.

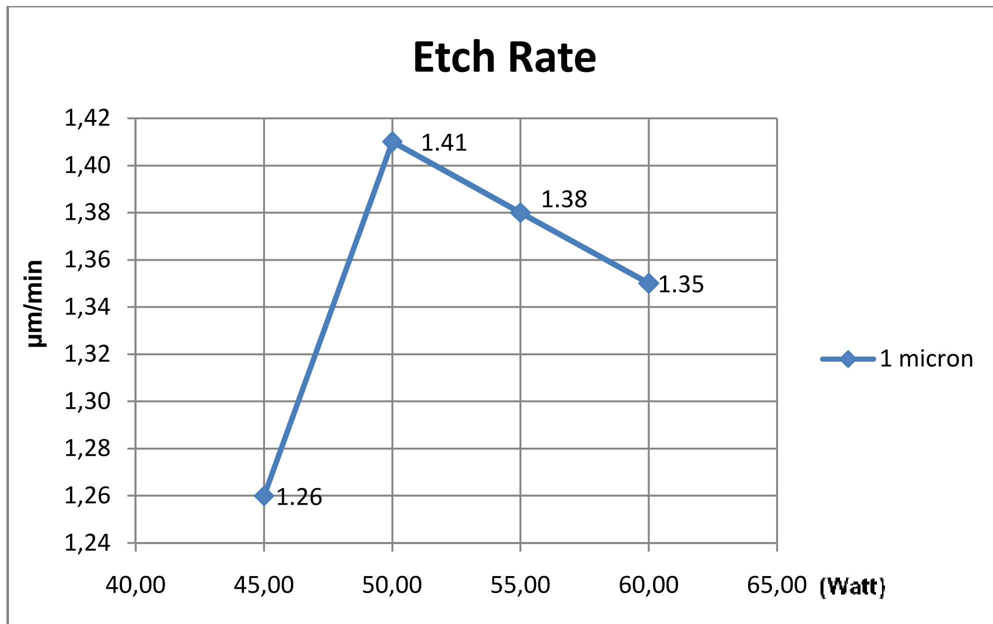


Figure 4.30: Etch rate dependence on the platen power.

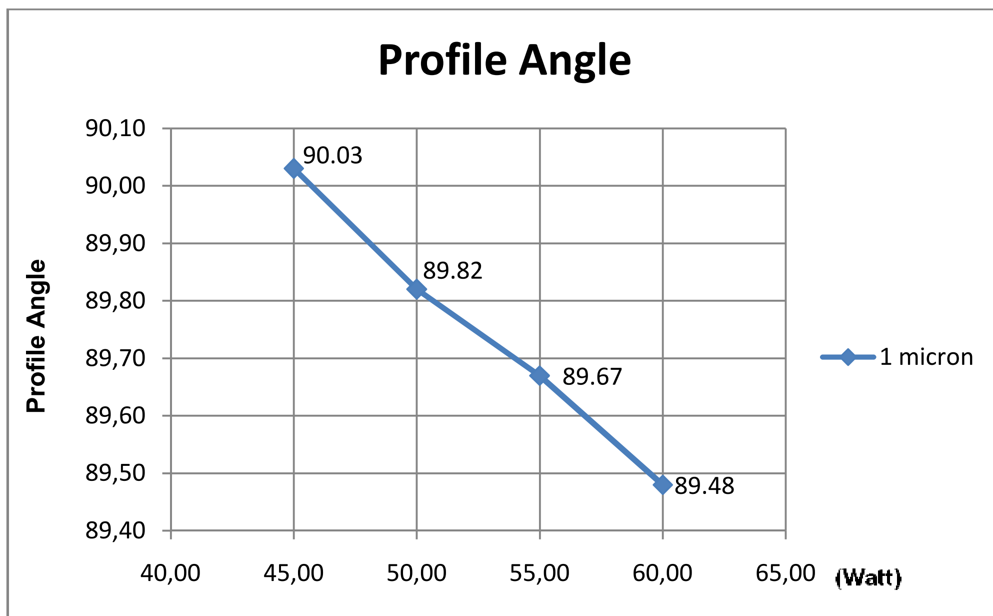


Figure 4.31: Profile angle dependence on the platen power.

4.3.5. Comments on the Optimization of DWP Results

For the optimization of DWP, effects of four parameters, step times, etch step pressure, platen power and electrode temperature, are investigated to obtain 20 µm depth for the minimum feature size, 1 µm, with a vertical sidewall and minimum undercut.

Step times have an important effect on the profile angle. For 2x2 step time, maximum mask undercut is observed due to insufficient passivation in 2 seconds among the other step time processes. The best sidewall passivation obtained with 3x3 and 4x4 step times. On the other hand, with the increased etch step time, increase in the etch step is observed.

Etch step pressure has a big effect on the etch rate. With the increased pressure, etch rate also increases. On the other hand, etch step pressure does not have a significant effect on the profile angle, except 2x2 step time, for the achieved depth of 1 µm trenches µm.

Since platen power is used for removing the passivation from the bottom of the opening, increasing the applied power, increased the etch rate by reducing the time spent for removing the passivation. However increasing the platen power also changes the profile angle to negative values.

Electrode temperature is the last parameter that is investigated for the DWP process. Since the passivation deposition rate directly related to the wafer temperature, reducing the electrode temperature increased the sidewall passivation. On the other hand, no significant effect on the etch rate is observed related to the electrode temperature. Table 4.7 shows the optimized recipe for DWP and Figure 4.32 shows cross sectional SEM image of the optimized trenches.

Table 4.7: Optimized recipe for DWP.

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Height (cm)	22	
Process Time (min)	15	

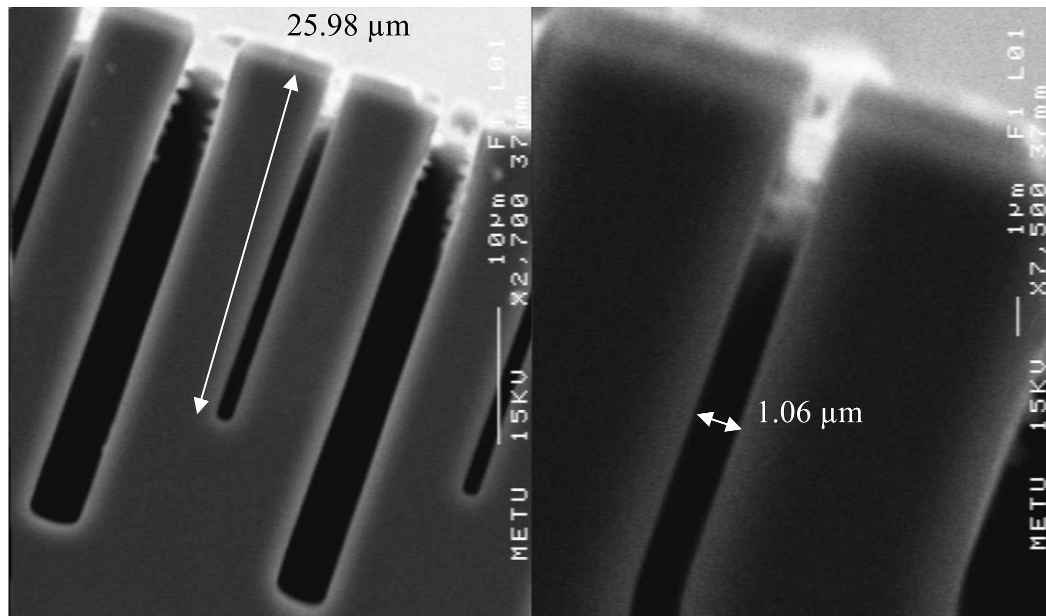


Figure 4.32: Cross sectional SEM image of the optimized trenches, without mask undercut and with a vertical sidewall.

4.4. Wafer Preparation for 100 micron Process

4-inch p-type silicon test wafers with resistivity ranging from 1 Ω - cm to 5 Ω - cm, 475-575 μm thick and (100) orientation were used in our study. Wafers are coated with 2.0 μm oxide, SiO_2, with STS PECVD system and Table 4.8 shows the recipe used for oxide mask. The photoresist 220-3 was coated at 2000 RPM (thickness ~4.0 μm, measured with Nanospec/AFT comprised film thickness measurement system) and softbaked at 115 ^{o}C for 90 seconds. Samples were exposed using mask aligner, EVG 620 Precision Alignment System, developed with MF24A for 1 minute before patterning the oxide layer with STS RIE system. Table 4.9 shows the recipe used for oxide etching.

The recipes to obtain 100:1 aspect ratio are chosen from the previous optimization processes giving the best results and satisfying given information to achieve high aspect ratio structures in section 4.1, for step time, pressure and platen power. Table 4.10 shows the recipe and for the etch step pressure 12, 20 and 40 mTorr etch step pressures are applied.

Table 4.8: PECVD recipe for SiO_2 deposition process.

Parameter	Value
SiH_4 flow rate	40 sccm
NH_3 flow rate	40 sccm
RF Power	20 W
Pressure	900 mTorr
Shower Temperature	250ºC
Platen Temperature	300ºC
Deposition Rate	350 Å/min.

Table 4.9: RIE SiO_2 etch recipe used for patterning the masking SiO_2.

Parameters	Value
CF_4 flow rate	12 sccm
CHF_3 flow rate	38 sccm
RF Power	300 W
Pressure	100 mTorr
Etch Rate	1400 Å/min.
Process Time	30 minute

Table 4.10: The recipe used for 100 µm etching process.

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	50% ≈ 12 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Height (cm)	22	
Process Time (min)	110	

Figure 4.33, 4.34 and 4.35 show the SEM image of the processes for 12, 20 and 40 mTorr etch step pressures and Figure 4.36, 4.37 and 4.38 show the result of the processes for etch rates, profile angle and achieved average depths from five different places of the wafer for 1 µm openings.

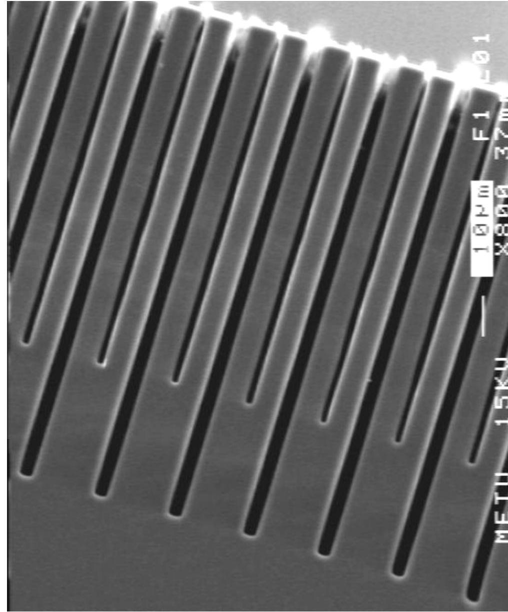


Figure 4.33: 12 mTorr etch step pressure. Average depth of 86.71 µm with vertical sidewalls and without any mask undercut is achieved. Recipe 6.1.

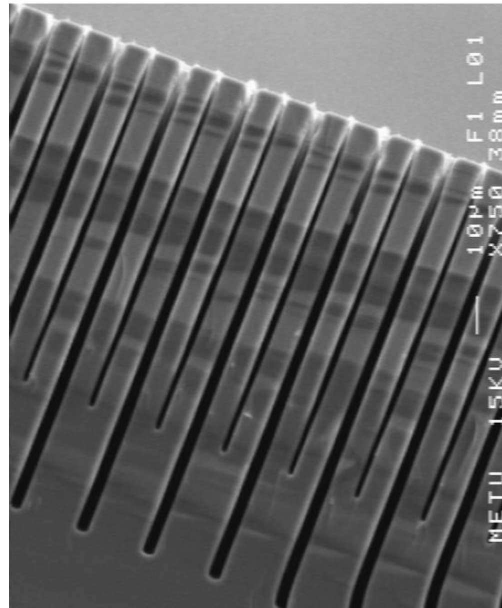


Figure 4.34: 20 mTorr etch step pressure. With the increased pressure, achieve average depth is increased to 94.93 µm. Recipe 6.2.

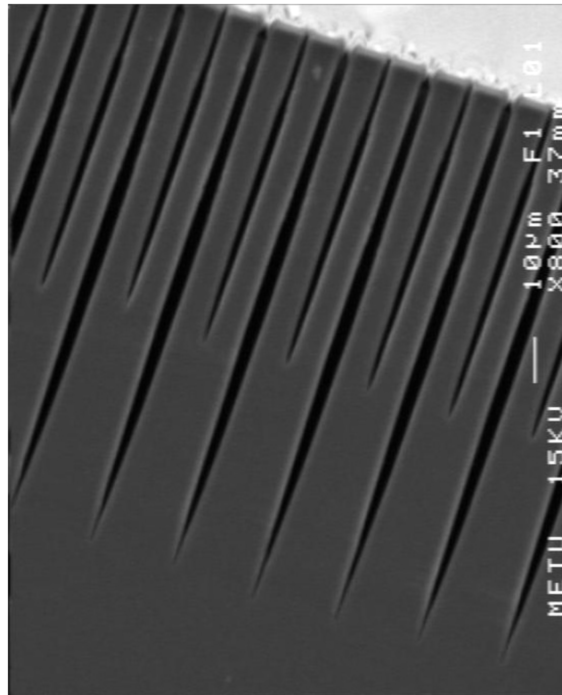


Figure 4.35: 40 mTorr etch step pressure. With the increased etch step pressure, closing up of the trenches through the bottom is observed. Recipe 6.3.

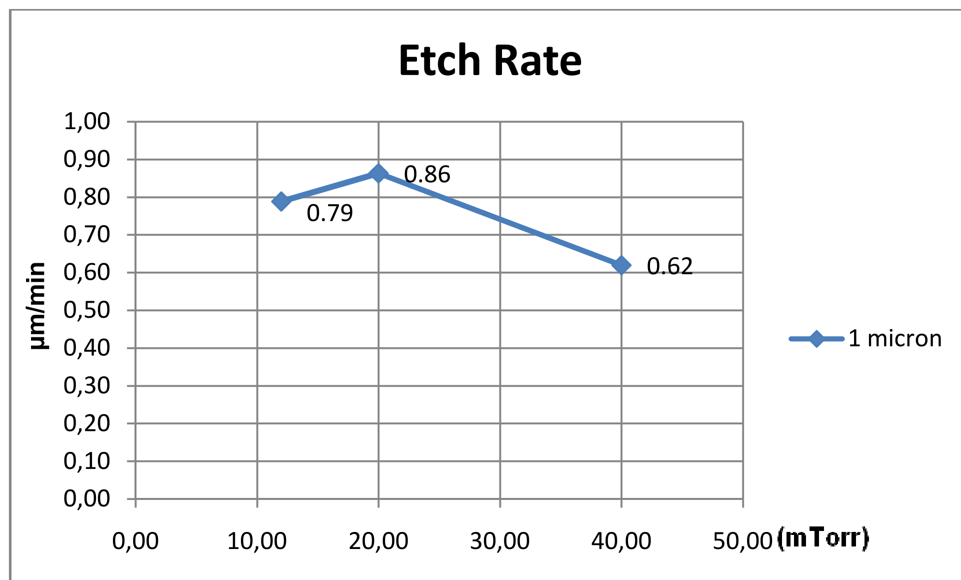


Figure 4.36: Etch rate dependence on the etch step pressure.

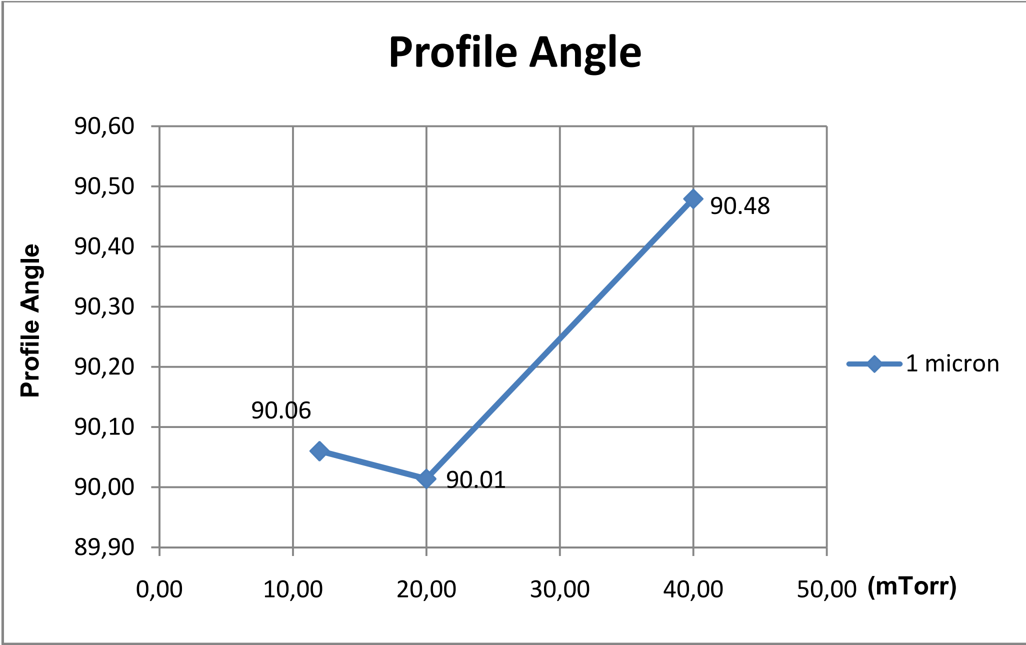


Figure 4.37: Profile angle dependence on the etch step pressure.

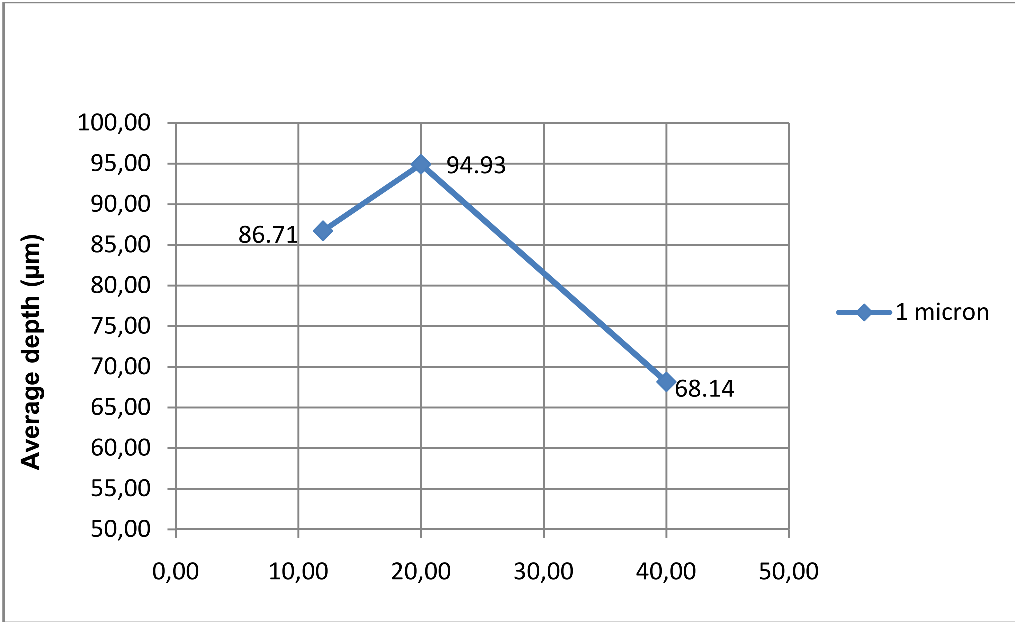


Figure 4.38: Average depth obtained for the different etch step pressure values.

At 40 mTorr etch step pressure, it is observed that both achieved depths are reduced and trenches are closed up towards the base. This problem can be explained considering two parameters in the recipe. First, the electrode temperature was set to -10°C, so deposition rate in the passivation step was high. Second, since the pressure was high in the etch step, mean free path of the ions were reduced. As a result, thick passivation layer couldn't be removed due to collisions of the ions at high pressure for such a deep trench and the silicon etching is completely stopped before the process has finished.

To increase the achieved depth to 100 μm for 1 μm openings, three more processes were done with the same recipe given in Table 4.10 for 12 mTorr and 20 mTorr and with 3x3 step time at 20 mTorr with the increased process time to 160 minutes for 4x4 processes and 150 minutes for 3x3 process. Same type of wafers were used for the process with an increased thickness of SiO_2 masking material to 4.5 μm, measured with Nanospec/AFT comprised film thickness measurement system, using the recipe given in Table 4.8 and with the same resist thickness of 4.0 μm. Samples were etched with RIE and Table 4.10 shows the recipe. SEM images of the processes results are shown in Figure 4.39, 4.40 and 4.41. Figure 4.42, 4.43 and 4.44 show the etch rate, profile angle and achieved depths for these processes.

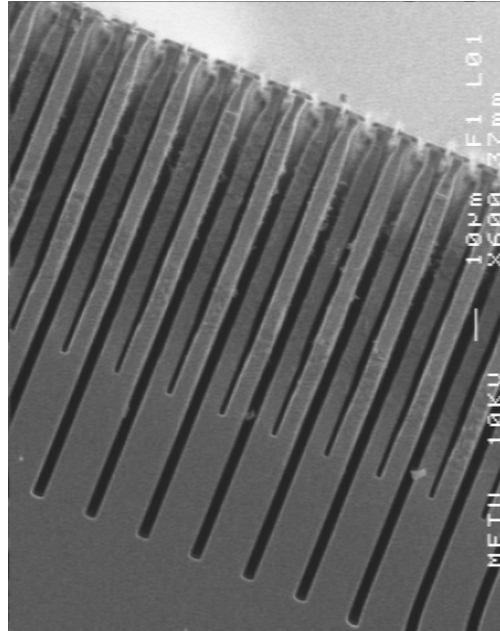


Figure 4.39: 3x3 step time at 20 mTorr etch step pressure. Mask undercut is observed due to decreased passivation time. Recipe 7.1.

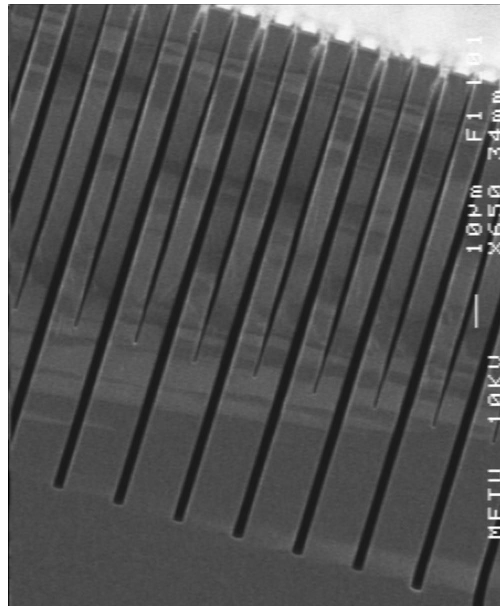


Figure 4.40: 4x4 step time at 12 mTorr etch step pressure. No mask undercut is observed. Recipe 7.2.

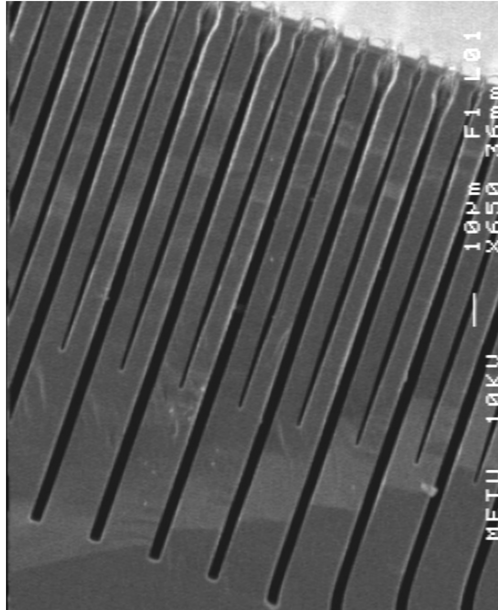


Figure 4.41: 4x4 step time at 20 mTorr etch step pressure. Better profile angle with a limited mask undercut is observed. Recipe 7.3.

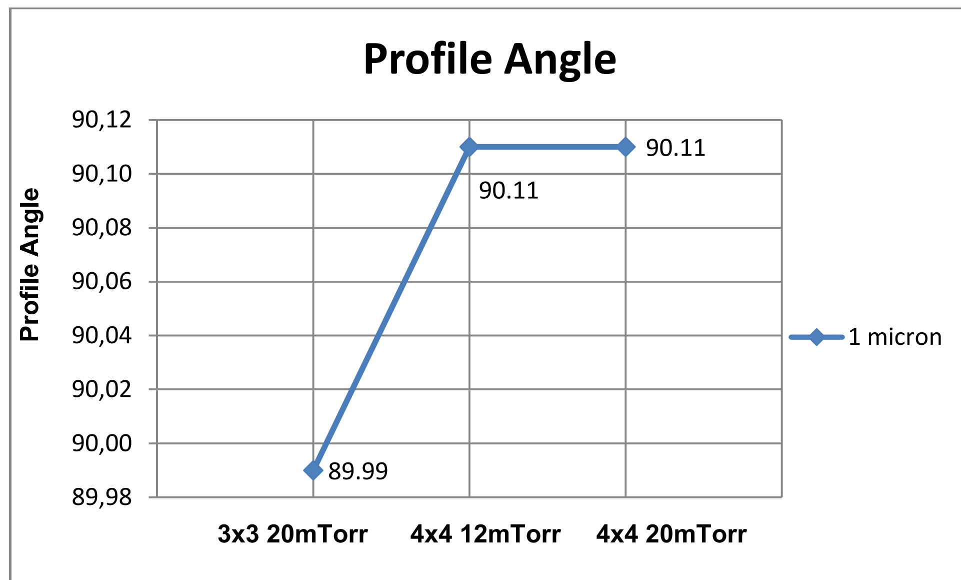


Figure 4.42: Profile angle dependence on step times and etch step pressures.

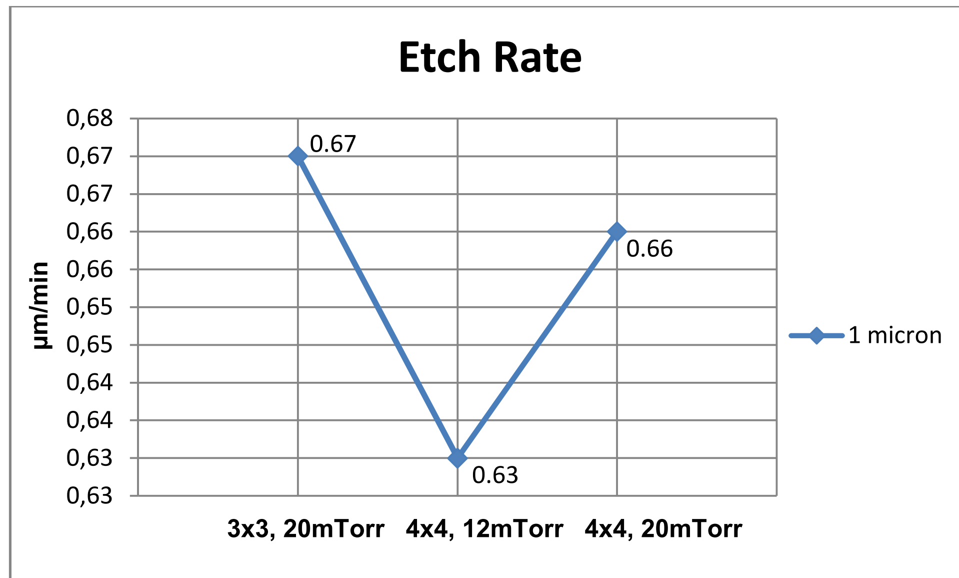


Figure 4.43: Graph of etch rate vs. different step times and etch step pressures.

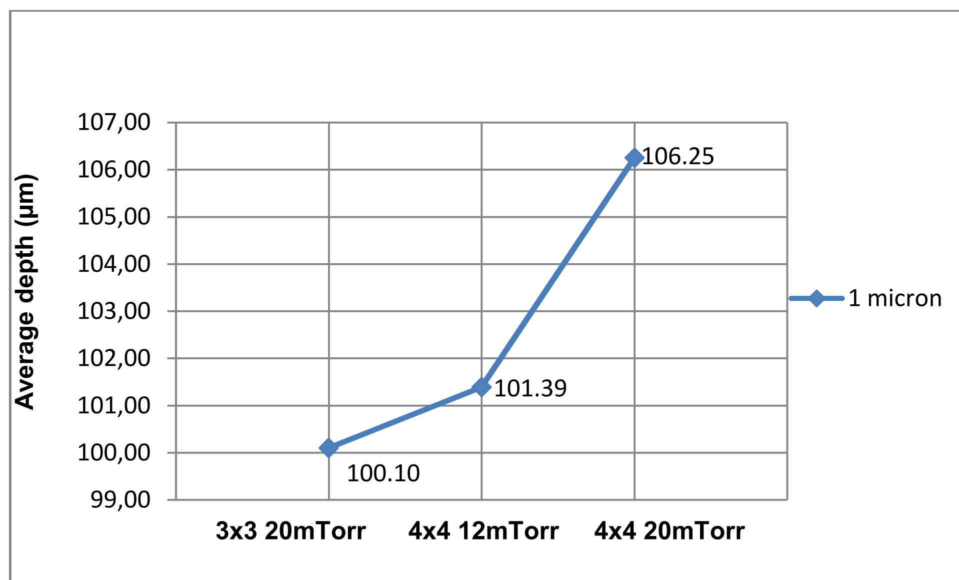


Figure 4.44: Average depth of 1.0 µm and 3.5 µm openings vs. different step times and etch step pressures.

4.4.1. Comments:

With the last recipes, Recipe 7.1, 7.2, 7.3, average depth of more than 100 µm is achieved. For the Recipe 7.2, 4x4 step time at 12 mTorr, it is observed that trenches close up through the base of the 1 µm openings and for the recipes 7.1 and 7.3 mask undercut is observed.

To make profile angle more vertical and to achieve more than 100 µm depth, a second step is inserted. Recipe 6.2 is used as the first step with a process time of 80 minutes. In the second step, ramping for the coil power in the passivation step is set to zero to prevent the closing up of the trenches and a ramping for the platen power is applied to remove the passivation from bottom of such deep openings. Moreover ramping the coil power in the etch step is also applied to improved the profile angle by increasing the amount of free radicals and ions in the plasma. The recipe for this two step processing is shown in Table 4.11 and 4.12 for the first and second step respectively and the SEM image of the obtained result is shown in Figure 4.45.

Table 4.11: Recipe A, 1st step used for two step process to increase the achieved depth for 1μm opening.

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Time (min)	80	

Table 4.12: Recipe A, 2nd step used for the two step process.

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400 (3.0 watt/min)	1000
Platen Power (Watt)	45 (0.3 watt/min)	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Time (min)	100	

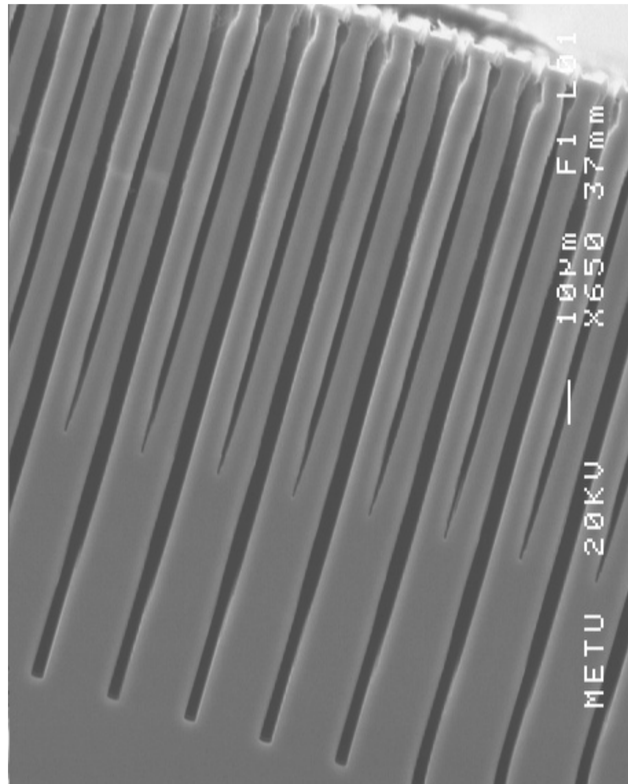


Figure 4.45: 2 steps process with new recipe. Mask undercut and closing up of the trenches through the base of the opening is observed. Recipe 8.

With the new recipe, it is observed that due to ramped platen and coil power in the second step, mask undercut is observed. Moreover, the developed recipe could not solve the profile angle problem. The last recipe, Recipe 9, is developed to solve the profile angle problem. The first step is kept as in the previous recipe. In the second step, ramp value for the coil power in the etch step is increased and the pressure value of the etch step is reduced to 12 mTorr to allow the ions to penetrate the deeper part of the openings.

Table 4.13 and Table 4.14 show the last developed recipe for two stepped process and Figure 4.46 shows the cross sectional SEM image of the 1 µm and 3.5 µm openings.

Table 4.13: Recipe B, 1st step used for two step process to prevent the closing up of the trenches through the base of the opening.

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Time (min)	80	

Table 4.14: Recipe B, 2nd step used for two step process to prevent the closing up of the trenches through the base of the opening.

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	50% ≈ 12	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400 (4.0 watt/min)	1000
Platen Power (Watt)	45 (0.3 watt/min)	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Time (min)	100	

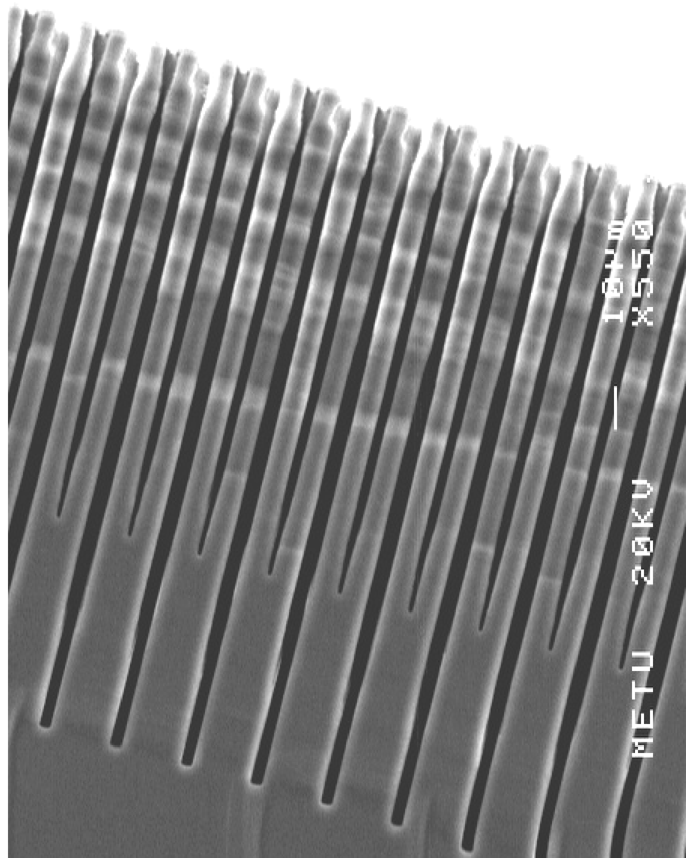


Figure 4.46: 2 steps process with last recipe. Closing up of the trenches through the base of the opening is reduced. Recipe 9.

With the applied Recipe B, average profile angle reduced to 90.40 from 90.80, achieved with the Recipe A and the etch rate increased to 0,62 from 0,58, achieved with the Recipe B.

Figure 4.47 shows the achieved depth results for the last two processes.

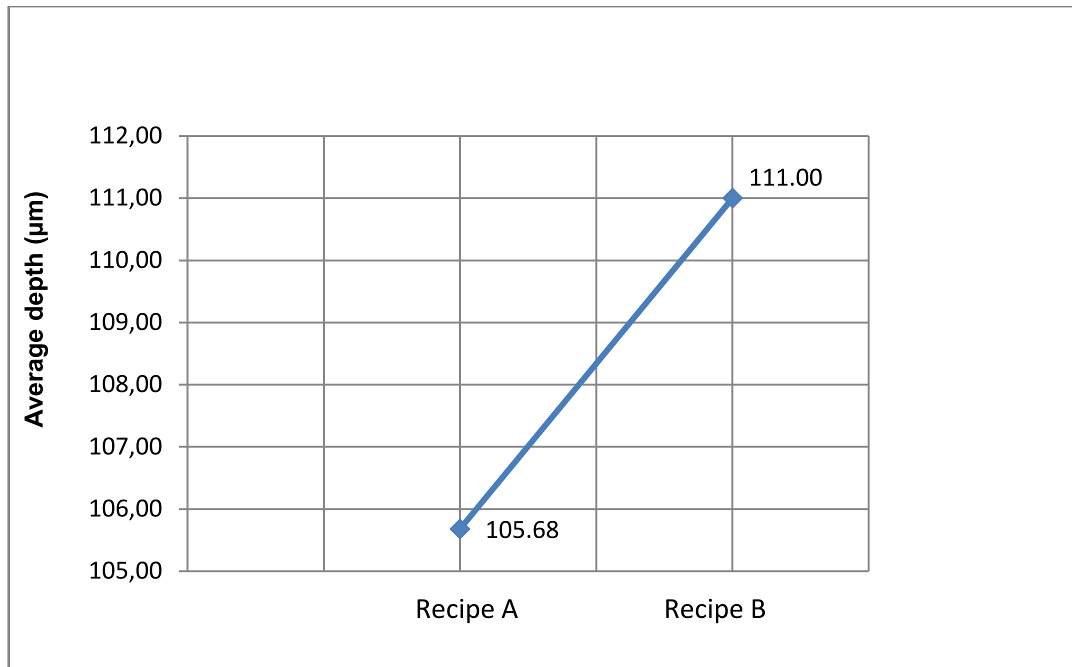


Figure 4.47: Average depth of 1.0 µm opening.

4.5. Conclusion

This chapter gives the experimental part of the optimization process. In the first part, process optimization for DWP is explained with the obtained result. Several parameters and their effects are investigated including step times, etch step pressure, platen power, and electrode temperature. The best result is obtained with the recipe given in Table 4.15.

Table 4.15: Optimized recipe for dissolved wafer process.

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Height (cm)	22	
Process Time (min)	15	

In the second part, parameters are optimized to obtain 100:1 aspect ratio. The information coming from the previous optimization processes are used. Considering the profile angle, etch rate and resist selectivity the new recipes are developed. Table 4.16 shows the applied recipe as the starting point. Two etch step pressure values are examined, 12 mTorr and 20 mTorr, in this processes.

Although the profile angle and selectivity of the masking material were sufficient, we could not succeed 100 µm depth with this recipe. Same recipe is applied with the increased process time from 110 minutes to 160 minutes for 3x3 step time at 20 mTorr, and 160 minutes for 4x4 step time at 12 and 20 mTorr to obtain 100 µm depths for 1 µm openings. Although 100 µm depth with a vertical sidewall obtained for 1 µm trenches with two of these recipes, Recipe 7.1, 7.3, with the increased process time, it is observed that profile angle turned to positive values for the 4x4 step time at 12 mTorr process, Recipe 7.2 and mask undercut is observed with the recipes 7.1 and 7.3. In order to solve profile angle problem and to increase the

achieved depths, another recipe, Table 4.11 and 4.12, is developed. In this recipe, process is divided into two parts. In the first step, the initial recipe is applied for 80 minutes. In the second step, to prevent the closing up of the trenches, ramping the coil power for the passivation step is stopped and a ramp for etch step platen power is applied. Moreover, the coil power in the etch step is also ramped in the second step to make plasma more dense. Although the achieved average depths are increased, ramping the coil and platen power did not solve the profile angle problem and the mask undercut is increased. As a final process, the last recipe, Table 4.13 and 4.14, is developed to solve the profile angle problem. With the last recipe better results with the average depth of 111 μm for 1 μm openings achieved.

Table 4.16: Initial recipe used for 100 μm etching.

Parameters	**Etch**	**Passivation**
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Height (cm)	22	
Process Time (min)	110	

CONCLUSION AND FUTURE WORK

The research performed in the concept of this thesis involves the optimization of DRIE process for integrated MEMS sensors. The theory of DRIE is explained in detail in this thesis. Process parameters of DRIE are investigated in order to obtain vertical sidewalls for two processes, DWP and 100 μm, and the results of experiments done with etch samples are included in this thesis.

The achievements carried out during this research can be summarized as follows:

1. Effects of step times on the etch rate, profile angle and mask undercut are investigated and it is found that, with the decreased step times, mask undercut problem becomes dominant due to the reduced sidewall passivation.

2. The effect of etch step pressure with different step times are investigated. Since the mask undercut problem observed in the step times could not be solved with the etch step pressure, 4x4 step times are chosen for the rest of the optimization processes.

3. The effect of electrode temperature and platen power on the etch rate and profile angle are examined. Although decreasing the electrode temperature increases the selectivity of the masking material and reduces the mask undercut problem by increasing the deposition rate, for larger openings it causes grassing problem. It is found that, increasing the platen power up to a point prevents grassing at the bottom of the larger openings without affecting the profile angle.

4. Since the etch step pressure is the key parameter to obtain high aspect ratio structures, for the optimization of the 100 μm process, 12, 20 and 40 mTorr etch step pressure values are examined. Because 40 mTorr is a quite high pressure, closing up of the trenches through the base of the openings is observed due to decreased mean free path of the plasma ions.

5. In the first optimization process, average depth of 100 μm depth could not be achieved due to the reduction in the etch rate with the increased aspect ratio. In the second recipe, process times were increased to 160 minutes for 4x4 processes and 150 minutes for 3x3 process to achieve 100 μm depth. Although more than 100 μm depth for 1 μm openings achieved, change in the profile angle to positive values observed.

6. In order to solve the problem faced in the second recipe of 100 μm process and to increase the achieved average depths for 1 μm openings, another recipe is developed. Since the trenches were closing up through the base of the openings, a second step with several changes were added. The initial recipe is applied for 80 minutes as the first step, since no problem observed up to that point and the second step for 100 minutes. The changes made in the second step can be explained as follows: a) Ramping the coil power in the passivation step is set to zero to reduce the passivation at the bottom of the trenches. b) A ramp value in the platen power is set to 0.3 watt per minute in order to increase the energy of the ions reaching the bottom of the opening. c) A ramp value in the coil power of the etch step is set to 3 watt per minute to make the plasma more dense by increasing the concentration of the ions and reactive radicals in the plasma. As a result achieved average depths are increased. On the other hand profile angle problem couldn't be solved with the developed recipe. To solve the problem a modification on the previous recipe is done. As a result, the last recipe is developed. In the last recipe, the ramp value in the coil power is increased to 4 Watt per minute and the

pressure is reduced to 12 mTorr. With the last recipe closing up of the trenches through the bottom is reduced with increased average depths. On the other hand, trenches got larger and mask undercut is observed with the increased process time and ramped powers.

This research gives above achievements on the optimization of two DRIE processes. However, there is still need to study further on some points which can be performed as future work:

1. For the smaller feature size, it is necessary to keep step times as low as possible. However for the 2x2 step times it is observed that, mask undercut and positive profile angle problems cannot be solved even with different pressure values. It is due to either too much etch components or too low passivation components. So optimization is required for 2x2 process.

2. Another parameter needed to be examined is the gas flow rates effect of which is not investigated in this research. The problem mentioned in the previous part can be solved by working on the gas flow rates by increasing the passivation or reducing the etching.

3. 100 μm process can be used for through wafer etching of 100 μm thickness wafer. However a handle wafer must be used in order to prevent both helium leak into the chamber and to protect the chuck from the incoming ions. Using handle wafer will affect the temperature of the process wafer and as a result the process will be affected. Attaching materials with good temperature conductivity must be investigated.

4. For 100 µm process optimization for the sidewall passivation is required to prevent the mask undercut due to the increased process time and ramped powers. This can be achieved by introducing an thermal oxidation process between the two steps in the DRIE process,

5. Since the process pressure depends on the gas flow rate and the position of the APC, effects of gas refreshment rates on the etch results can be analyzed. High gas refreshment rate means high gas flow rate with more opened APC valve and low gas refreshment rate means low gas flow rate with more closed APC valve position giving the same pressure.

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APPENDICES A

RECIPIES AND AVERAGE MEASUREMENT RESULTS

RECIPE 1 and Recipe 1.1:

Parameters	Etch	Passivation
Step Time (s)	2	2
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	50% ≈ 12 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	10	
Process Height (cm)	22	
Process Time (min)	15	

Recipe 1.2:

Step Time (s)	2	2
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr

Recipe 1.3:

Step Time (s)	2	2
Pressure (mTorr)	85.5% ≈ 30 mTorr	85.5% ≈ 8 mTorr

Recipe 1.4:

Step Time (s)	2	2
Pressure (mTorr)	88.2% ≈ 40 mTorr	85.5% ≈ 8 mTorr

Recipe 1.5:

Step Time (s)	2	2
Pressure (mTorr)	89.2% ≈ 50 mTorr	85.5% ≈ 8 mTorr

Recipe 2.1:

Step Time (s)	3	3
Pressure (mTorr)	50% ≈ 12 mTorr	85.5% ≈ 8 mTorr

Recipe 2.2:

Step Time (s)	3	3
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr

Recipe 2.3:

Step Time (s)	3	3
Pressure (mTorr)	85.5% ≈ 30 mTorr	85.5% ≈ 8 mTorr

Recipe 2.4:

Step Time (s)	3	3
Pressure (mTorr)	88.2% ≈ 40 mTorr	85.5% ≈ 8 mTorr

Recipe 2.5:

Step Time (s)	3	3
Pressure (mTorr)	89.2% ≈ 50 mTorr	85.5% ≈ 8 mTorr

Recipe 3.1:

Step Time (s)	4	4
Pressure (mTorr)	50% ≈ 12 mTorr	85.5% ≈ 8 mTorr

Recipe 3.2:

Step Time (s)	4	4
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr

Recipe 3.3:

Step Time (s)	4	4
Pressure (mTorr)	85.5% ≈ 30 mTorr	85.5% ≈ 8 mTorr

Recipe 3.4:

Step Time (s)	4	4
Pressure (mTorr)	88.2% ≈ 40 mTorr	85.5% ≈ 8 mTorr

Recipe 3.5:

Step Time (s)	4	4
Pressure (mTorr)	89.2% ≈ 50 mTorr	85.5% ≈ 8 mTorr

Recipe 4 and Recipe 4.1:

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	20	0
EM1	Off	Off
Electrode Temperature (^oC)	10	
Process Height (cm)	22	
Process Time (min)	15	

Recipe 4.2:

Platen Power (Watt)	45

Recipe 4.3:

Platen Power (Watt)	57.5

Recipe 4.4:

Platen Power (Watt)	70

Recipe 5 and Recipe 5.1:

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-20	
Process Height (cm)	22	
Process Time (min)	15	

Recipe 5.2:

Electrode Temperature (^oC)	-10	0

Recipe 5.3:

Electrode Temperature (^oC)	0	0

Recipe 5.4:

Electrode Temperature (^oC)	10	0

Recipe 6 and Recipe 6.1:

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	50% ≈ 12 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Height (cm)	22	
Process Time (min)	110	

Recipe 6.2:

Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr

Recipe 6.3:

Pressure (mTorr)	88.2% ≈ 40 mTorr	85.5% ≈ 8 mTorr

Recipe 7 and Recipe 7.1:

Parameters	Etch	Passivation
Step Time (s)	3	3
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Height (cm)	22	
Process Time (min)	150	

Recipe 7.2:

Step Time (s)	4	4
Pressure (mTorr)	50% ≈ 12 mTorr	85.5% ≈ 8 mTorr
Process Time (min)	160	

Recipe 7.3:

Step Time (s)	4	4
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr
Process Time (min)	160	

Recipe 8: Step 1

Parameters	**Etch**	**Passivation**
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Height (cm)	22	
Process Time (min)	80	

Step 2

Parameters	**Etch**	**Passivation**
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400 (+3 W/min)	1000
Platen Power (Watt)	45 (+0.3 W/min)	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Height (cm)	22	
Process Time (min)	100	

Recipe 9: Step 1

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	79.2% ≈ 20 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400	800 (+2.5 W/min)
Platen Power (Watt)	45	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Height (cm)	22	
Process Time (min)	80	

Step 2

Parameters	Etch	Passivation
Step Time (s)	4	4
SF_6 Flow (sccm)	400	0
C_4F_8 Flow (sccm)	0	80
Pressure (mTorr)	50% ≈ 12 mTorr	85.5% ≈ 8 mTorr
Coil Power (Watt)	2400 (+4 W/min)	1000
Platen Power (Watt)	45 (+0.3 W/min)	0
EM1	Off	Off
Electrode Temperature (^oC)	-10	
Process Height (cm)	22	
Process Time (min)	100	

RECIPE 1	1 µm Top	1 µm Bottom	1 µm Depth	3.5 µm top	3.5 µm Bottom	3.5 µm Depth	Etch Rate 1 µm	Etch Rate 3.5 µm	Profile Angle 1 µm	Profile Angle 3.5 µm
Recipe 1.1	2.50	1.74	21.94	4.53	4.41	29.34	1.46	1.96	91.98	90.23
Recipe 1.2	1.70	1.22	17.21	4.09	3.92	30.19	1.15	2.01	91.60	90.32
Recipe 1.3	2.46	1.30	23.06	4.40	4.13	33.30	1.54	2.22	92.88	90.46
Recipe 1.4	2.67	1.28	22.72	4.82	4.21	33.50	1.51	2.23	93.50	91.04
Recipe 1.5	3.05	1.49	27.37	5.12	4.28	37.30	1.82	2.49	93.26	91.29

RECIPE 2	1 µm Top	1 µm Bottom	1 µm Depth	3.5 µm top	3.5 µm Bottom	3.5 µm Depth	Etch Rate 1 µm	Etch Rate 3.5 µm	Profile Angle 1 µm	Profile Angle 3.5 µm
Recipe 2.1	1.35	1.26	22.02	3.53	3.86	30.87	1.47	2.06	90.23	89.39
Recipe 2.2	1.39	1.39	27.22	4.28	4.61	39.06	1.81	2.60	90.00	89.52
Recipe 2.3	1.69	1.49	25.00	3.66	4.09	34.44	1.67	2.30	90.46	89.28
Recipe 2.4	1.59	1.24	24.27	3.64	3.68	33.56	1.62	2.24	90.83	89.93
Recipe 2.5	1.45	1.10	28.58	3.33	3.65	40.99	1.91	2.73	90.70	89.55

RECIPE 3	1 µm Top	1 µm Bottom	1 µm Depth	3.5 µm top	3.5 µm Bottom	3.5 µm Depth	Etch Rate 1 µm	Etch Rate 3.5 µm	Profile Angle 1 µm	Profile Angle 3.5 µm
Recipe 3.1	1.00	1.03	21.67	3.66	3.49	31.25	1.44	2.08	89.92	90.31
Recipe 3.2	1.32	1.27	25.30	3.35	3.55	34.69	1.69	2.31	90.11	89.67
Recipe 3.3	1.34	1.25	26.92	3.60	3.70	39.23	1.79	2.62	90.19	89.85
Recipe 3.4	1.24	1.12	31.16	3.56	3.91	45.36	2.08	3.02	90.22	89.56
Recipe 3.5	1.22	0.96	37.26	4.07	4.66	46.70	2.48	3.11	90.40	89.28

RECIPE 4	1 µm Top	1 µm Bottom	1 µm Depth	3.5 µm top	3.5 µm Bottom	3.5 µm Depth	Etch Rate 1 µm	Etch Rate 3.5 µm	Profile Angle 1 µm	Profile Angle 3.5 µm
Recipe 4.1	1.17	1.02	24.37	3.67	3.22	28.44	1.62	1.90	90.35	90.91
Recipe 4.2	1.32	1.27	25.30	3.35	3.55	34.69	1.69	2.31	90.11	89.67
Recipe 4.3	1.21	1.50	31.67	3.70	4.17	42.58	2.11	2.84	89.48	89.37
Recipe 4.4	1.30	1.53	31.42	3.94	4.33	43.77	2.09	2.92	89.58	89.49

RECIPE 5	1 µm top	1 µm Bottom	1 µm Depth	3.5 µm top	3.5 µm Bottom	3.5 µm Depth	Etch Rate 1 µm	Etch Rate 3.5 µm	Profile Angle 1 µm	Profile Angle 3.5 µm
Recipe 5.1	0.83	0.74	22.61	3.13	3.01	33.15	1.51	2.21	90.23	90.21
Recipe 5.2	1.07	1.05	26.17	3.63	3.50	37.07	1.74	2.47	90.04	90.20
Recipe 5.3	1.11	1.11	26.20	3.69	3.75	37.10	1.75	2.47	90.00	89.91
Recipe 5.4	1.32	1.27	25.30	3.35	3.55	34.69	1.69	2.31	90.11	89.67

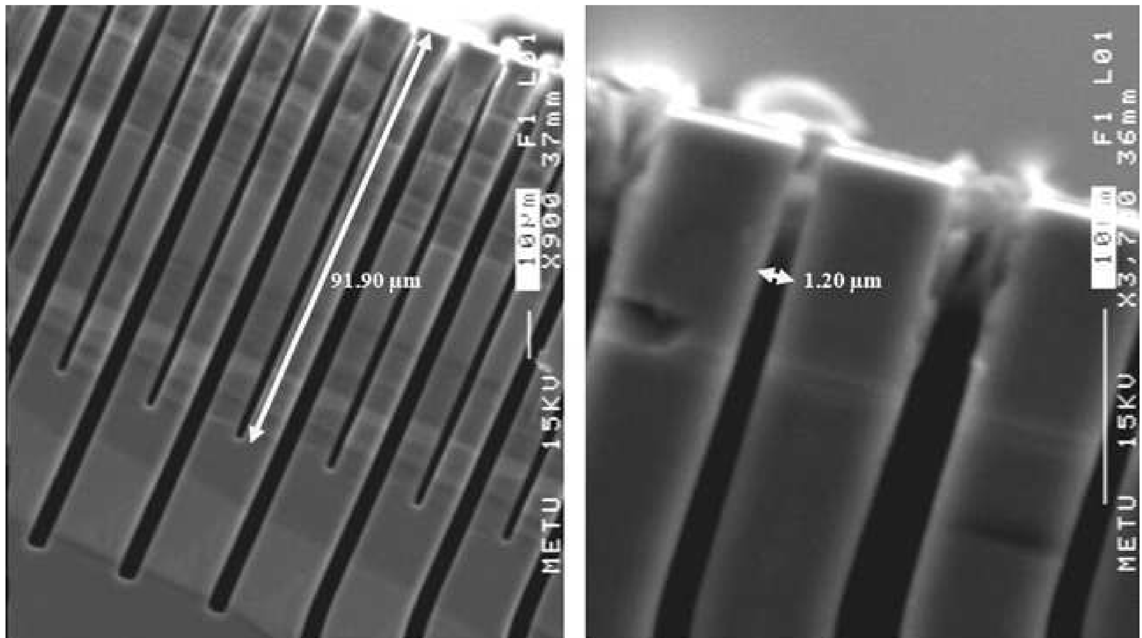
RECIPE 6	1 µm top	1 µm Bottom	1 µm Depth	3.5 µm top	3.5 µm Bottom	3.5 µm Depth	Etch Rate 1 µm	Etch Rate 3.5 µm	Profile Angle 1 µm	Profile Angle 3.5 µm
Recipe 6.1	1.04	0.95	86.71	2.34	2.67	120.31	0.79	1.09	90.06	89.84
Recipe 6.2	1.06	1.05	94.93	2.22	2.85	126.61	0.86	1.15	90.01	89.72
Recipe 6.3	1.27	0.70	68.14	2.18	0.90	115.93	0.62	1.05	90.48	90.63

RECIPE 7	1 µm Top	1 µm Bottom	1 µm Depth	3.5 µm top	3.5 µm Bottom	3.5 µm Depth	Etch Rate 1 µm	Etch Rate 3.5 µm	Profile Angle 1 µm	Profile Angle 3.5 µm
Recipe 7.1	1.68	1.69	100.10	3.86	3.49	141.92	0.67	0.95	89.99	90.15
Recipe 7.2	0.96	0.64	101.39	2.00	3.18	151.11	0.63	0.94	90.11	90.18
Recipe 7.3	1.19	0.98	106.25	2.52	3.20	152.92	0.66	0.96	90.11	89.64

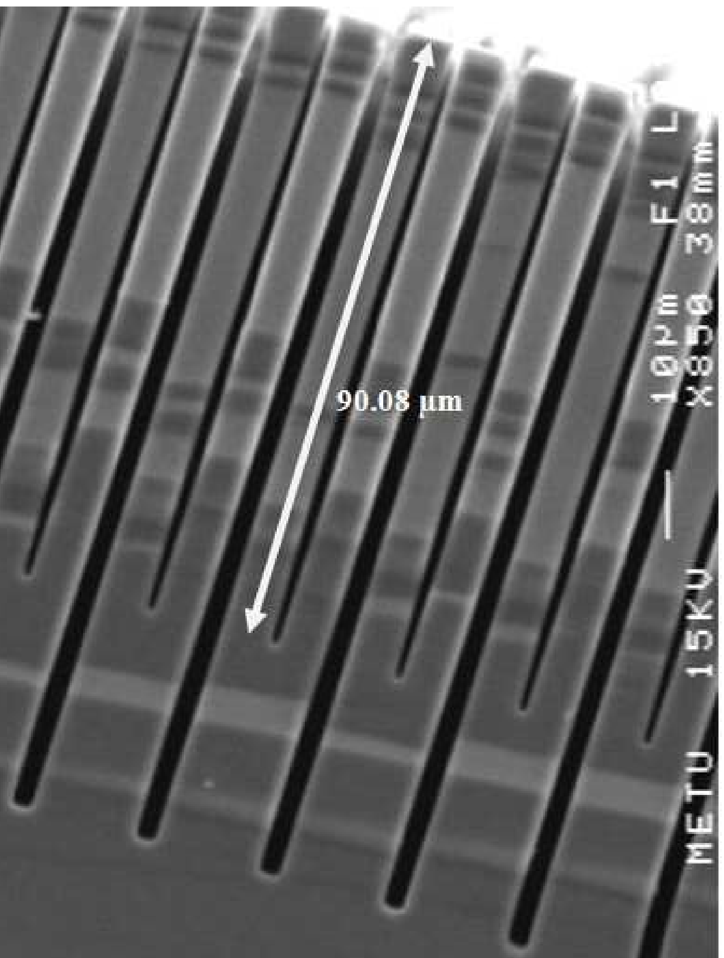
	1 µm Top	1 µm Bottom	1 µm Depth	3.5 µm top	3.5 µm Bottom	3.5 µm Depth	Etch Rate 1 µm	Etch Rate 3.5 µm	Profile Angle 1 µm	Profile Angle 3.5 µm
RECIPE 8	1.98	0.51	105.68	3.09	2.28	153.60	0.58	0.85	90.80	90.28
RECIPE 9	1.94	1.16	111.00	2.46	2.40	157.50	0.62	0.88	90.40	90.02

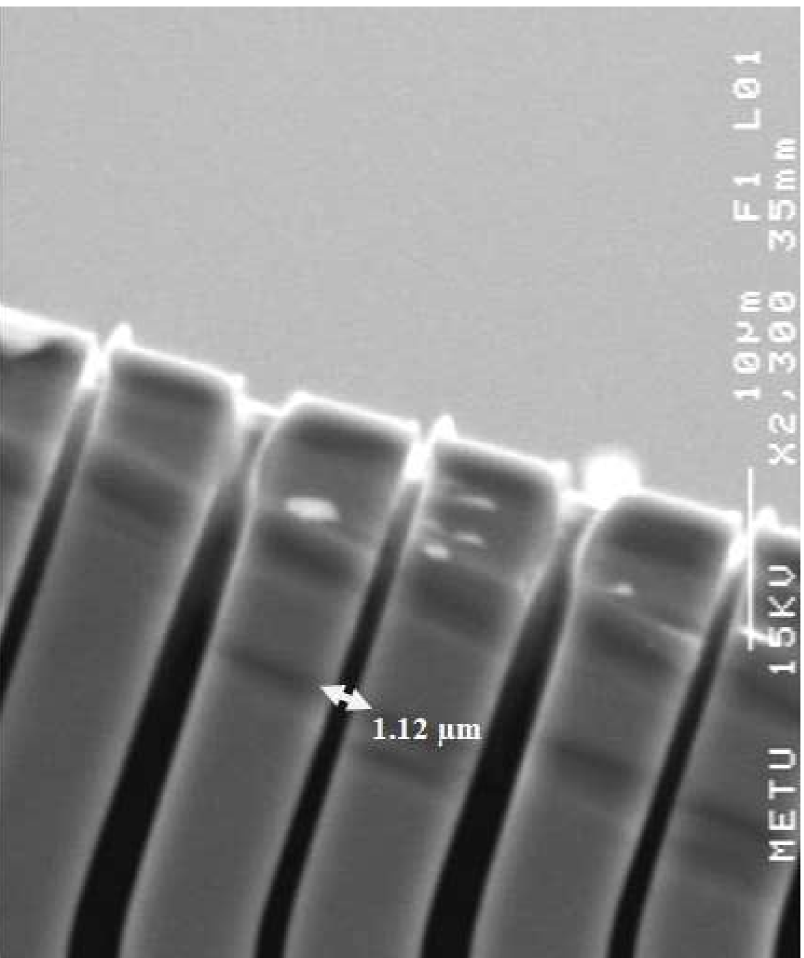
APPENDICES B

SEM IMAGES OF 100 MICRON PROCESSES

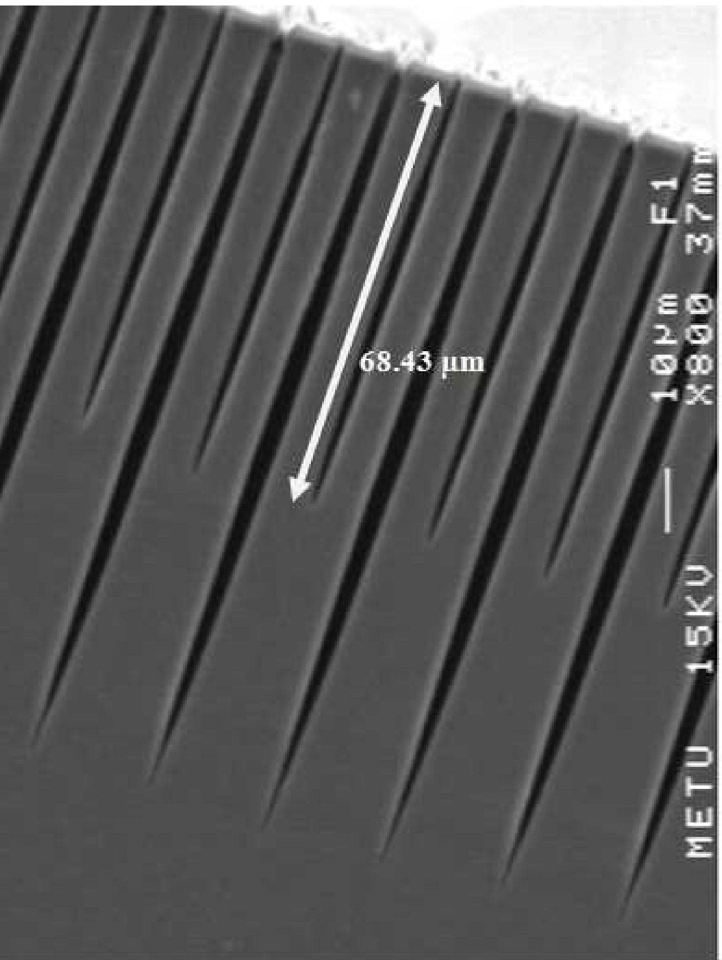


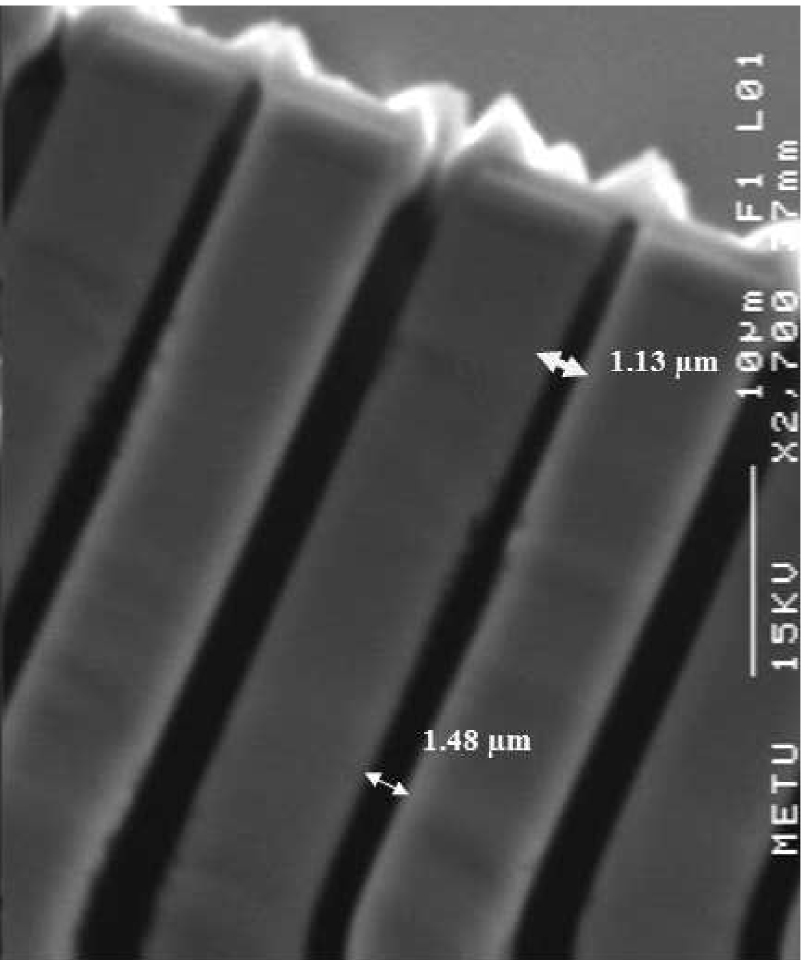
Recipe 6.1, 110min, 12mTorr, Aspect Ratio: 76.58



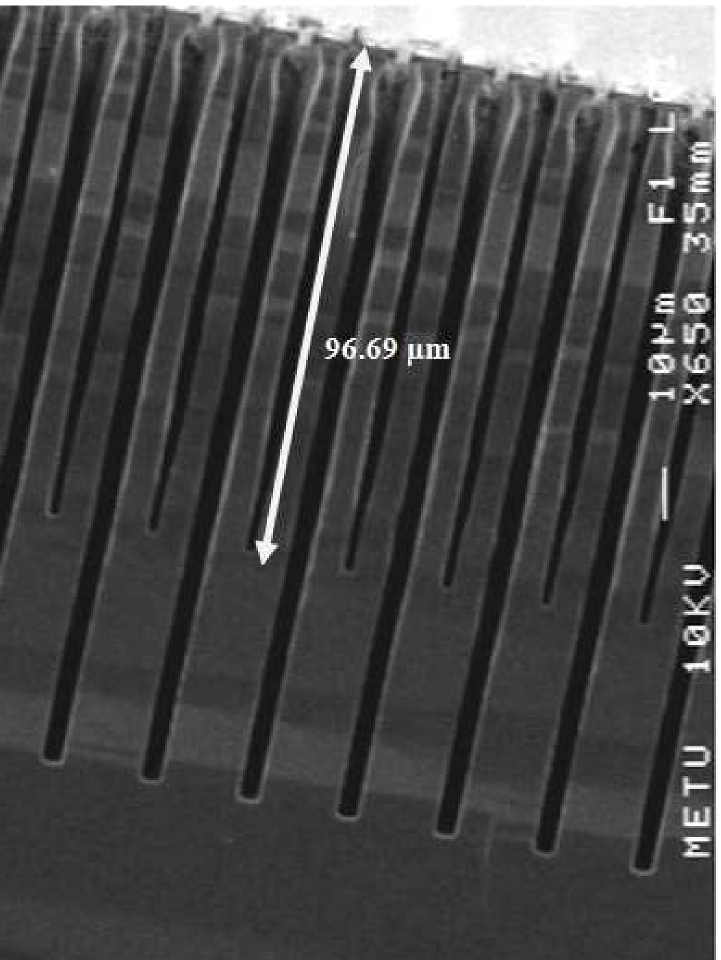


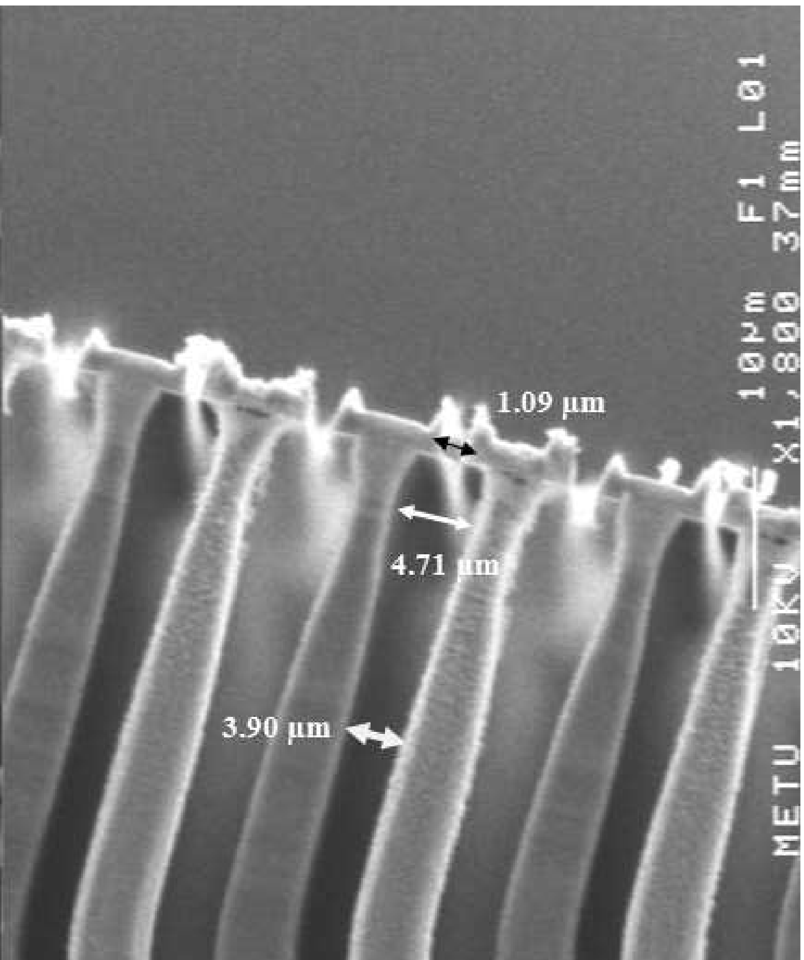
Recipe 6.2, 110min, 20mTorr, Aspect Ratio: 80.43



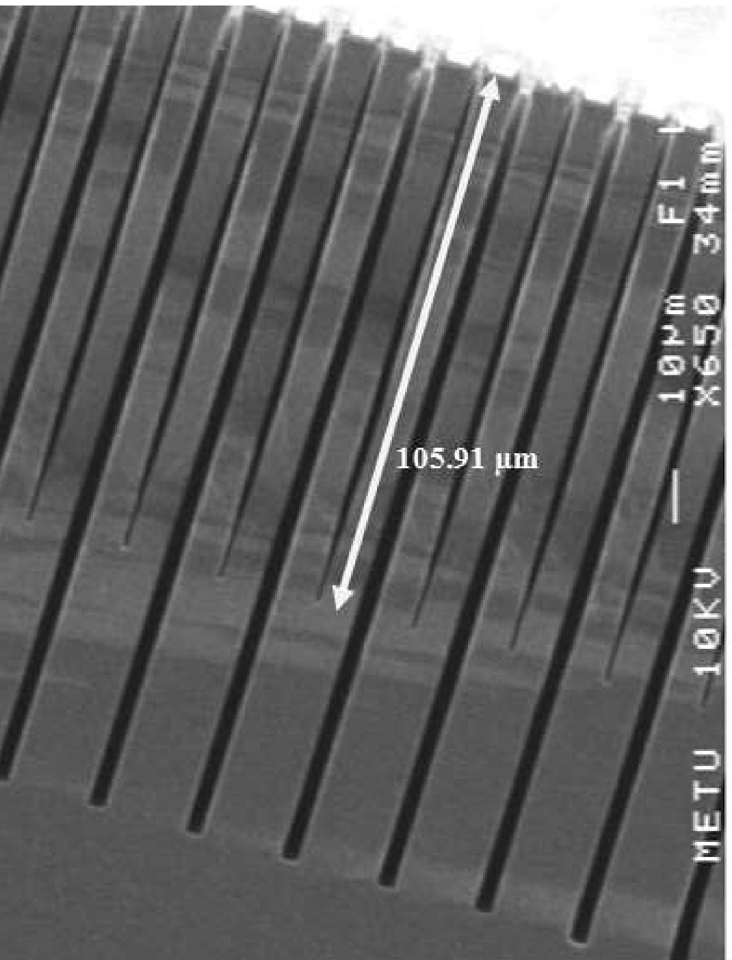


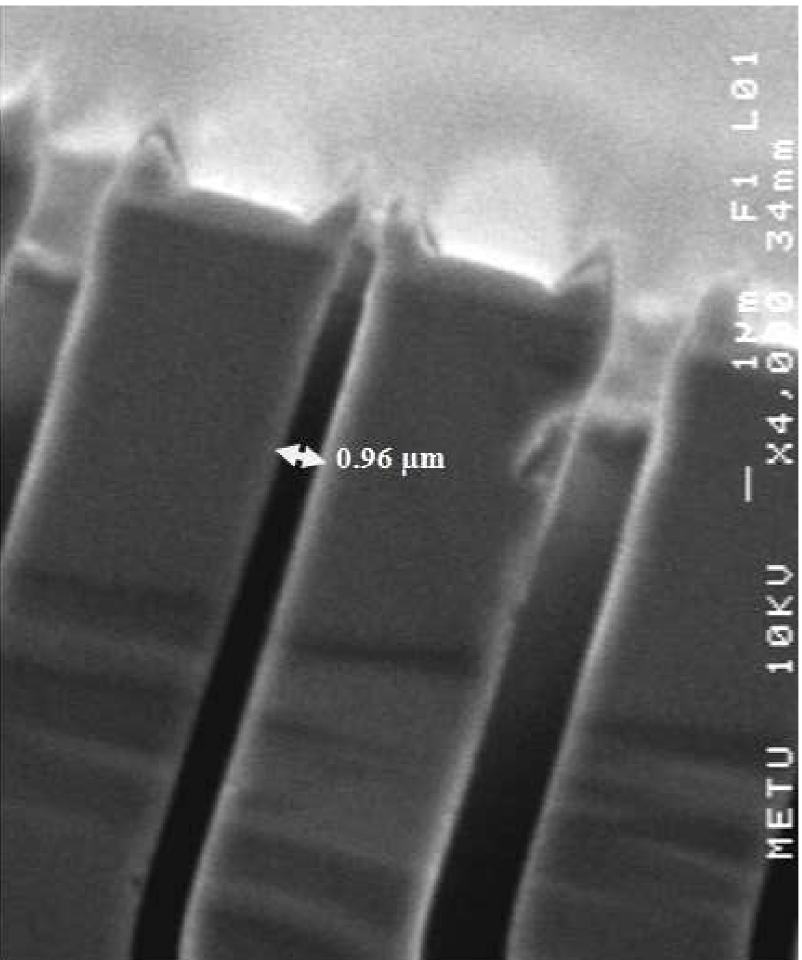
Recipe 6.3, 110min 40mTorr, Aspect Ratio: 60.56 for 1.13 µm opening



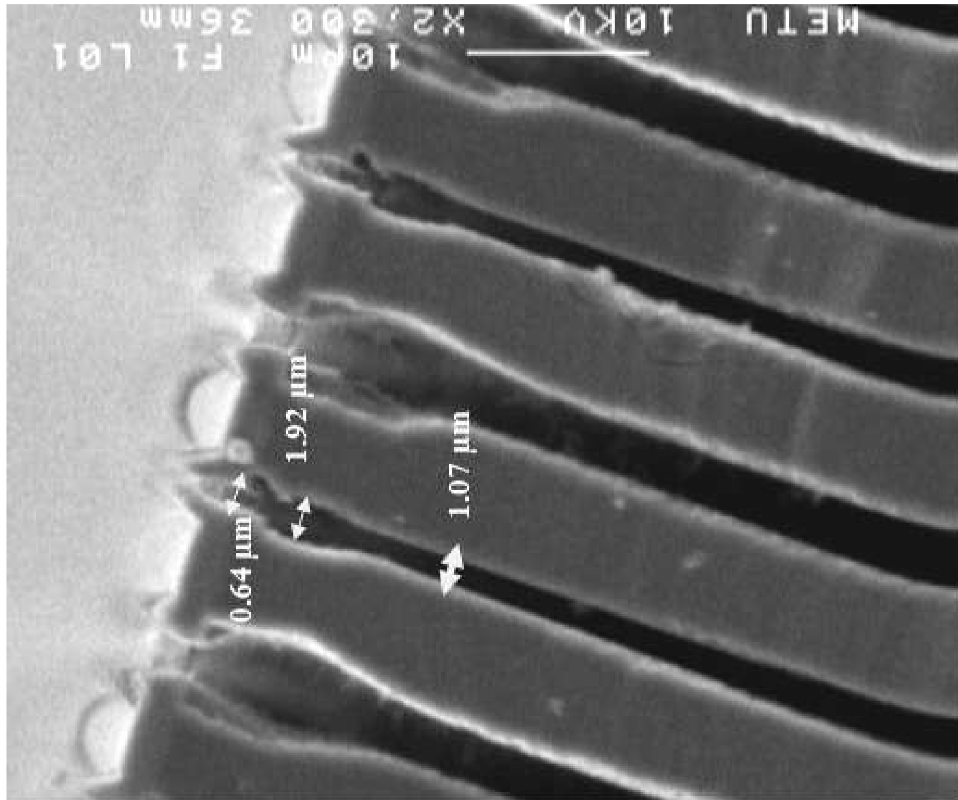


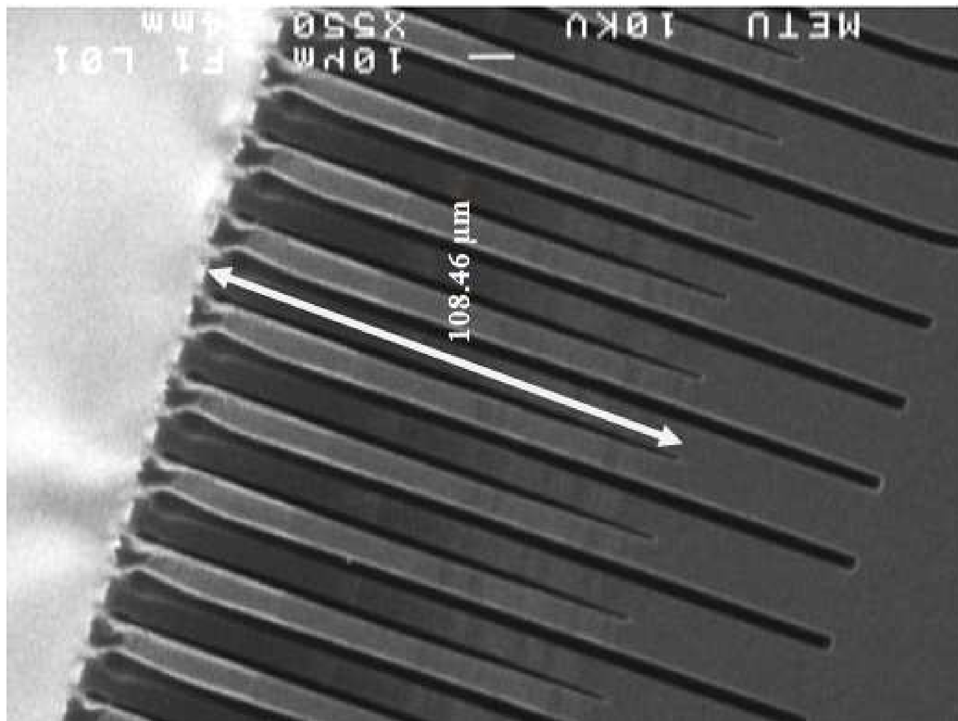
Recipe 7.1, 150min, 20mTorr, 3x3





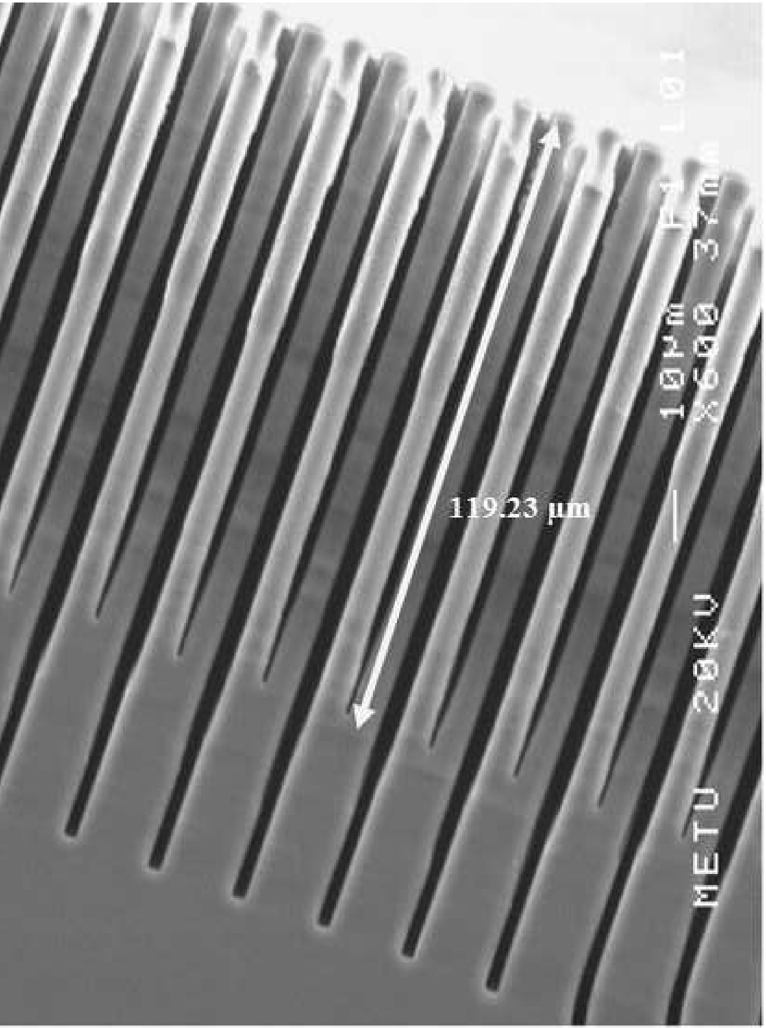
Recipe 7.2, 160min, 12mTorr, Aspect Ratio: 110.32

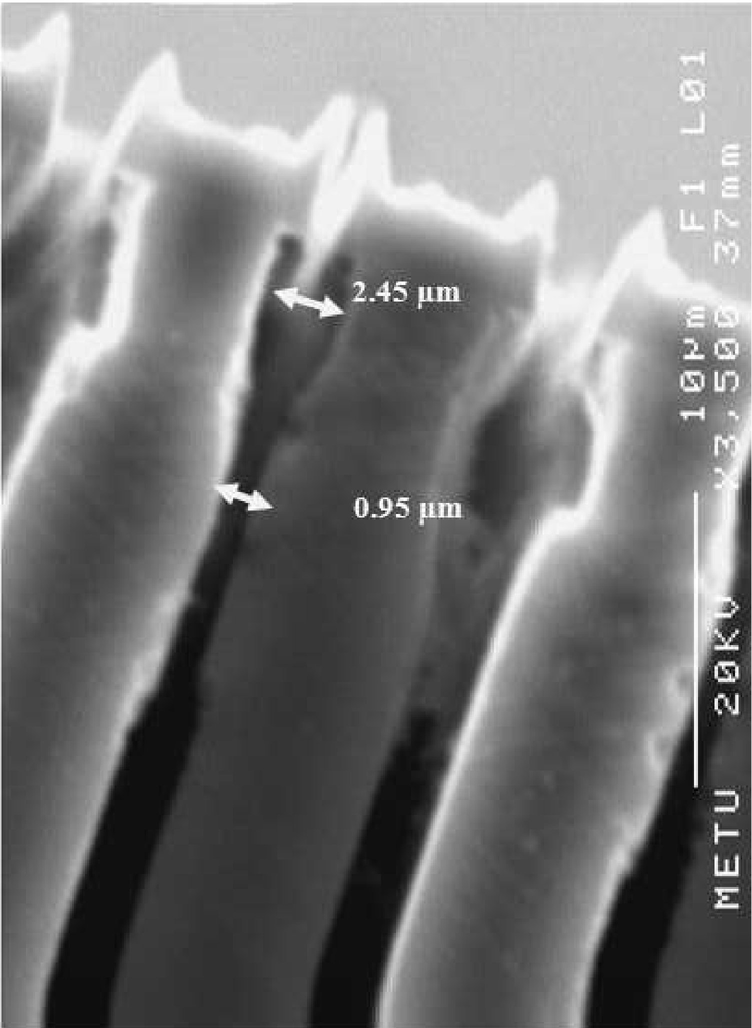




Recipe 7.3, 160min, 20mTorr

Recipe 8, 180min, (2 steps), Aspect Ratio: 105.77





Recipe 9, 180min, (2 steps), Aspect Ratio: 125.