

OPTIMIZING TRANSIENT AND FILTERING PERFORMANCE  
OF A C-TYPE 2<sup>ND</sup> HARMONIC POWER FILTER  
BY THE USE OF SOLID-STATE SWITCHES

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## ABSTRACT

OPTIMIZING TRANSIENT AND FILTERING PERFORMANCE  
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In this research work, the performance of a C-type, 2<sup>nd</sup> harmonic power filter is optimized by the use of a thyristor switched damping resistor. In the design of conventional C-type, 2<sup>nd</sup> harmonic filters; the resistance of permanently connected damping resistor is to be optimized for minimization of voltage stresses on filter elements arising from switchings in transient state and for maximization of filtering effectiveness in the steady-state. Transformer inrush current during energization of power transformers and connection of filter bank to the supply are the major causes of voltage stresses arising on filter elements in transient state. These can be minimized by designing a highly damped C-type filter (low damping resistor) at the expense of inadequate filtering performance and high losses in the steady-state. On the other hand, higher damping resistance (high quality factor) is to be chosen in the design of C-type filter for satisfactory filtering of 2<sup>nd</sup> harmonic current component at the expense of higher voltage rating for capacitor bank and hence a more costly filter bank design. This drawback of conventional C-type 2<sup>nd</sup> harmonic filter circuit can be

eliminated by subdividing damping resistor into two parallel parts; one is permanently connected while the other is connected to and disconnected from the circuit by back-to-back connected thyristor assemblies. The use of light triggered thyristors provides isolation between power stage and control circuit, and hence allows outdoor installation.

**Keywords:** C-type Harmonic Filter, Arc and Ladle Furnaces, Filter Capacitor Overvoltages, Harmonics and Interharmonics

## ÖZ

### C-TİPİ 2İNCİ HARMONİK GÜÇ FİLTRESİNİN GEÇİCİ REJİM VE FİLTRELEME PERFORMANSININ YARI-İLETKEN ANAHTARLAR KULLANILARAK OPTİMİZE EDİLMESİ

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Bu araştırma çalışmasında, C-tipi 2inci harmonik güç filtresinin performansı, tristör anahtarlama direnci kullanılarak optimize edilmiştir. C-tipi 2inci harmonik filtrelerin geleneksel tasarımında; filtre elemanları üzerinde, geçici rejimdeki anahtarlama sebebiyle oluşan gerilim baskılarını en aza indirmek ve durağan-durumda filtreleme etkinliğini azami dereceye çıkarmak için, sürekli olarak bağlı olan direncin değeri optimize edilmelidir. Güç transformatörlerinin enerjilendirme akımı ve filtre bankasının kaynağa bağlanması, geçici rejimde filtre elemanları üzerinde oluşan gerilim baskılarının iki ana nedenidir. Bu baskılar, yetersiz filtreleme performansı ve durağan-durumda yüksek kayıplar pahasına, yüksek sönümlendirmeli C-tipi filtre (düşük sönümlendirme direnci) tasarlanarak en aza indirilebilir. Öte yandan, C-tipi filtenin tasarımında, daha yüksek gerilim sınıflı kondansatör bankası, ve dolayısıyla daha pahalı bir filtre tasarımı pahasına; 2inci harmonik akımın yeterli oranda filtrelenmesi için, daha yüksek bir sönümlendirme

direnci (yüksek kalite faktörü) seçilmelidir. Geleneksel C-tipi 2inci harmonik filtre devresinin bu sakıncası, sönümlendirme direncini iki paralel kısma ayırıp birisini sürekli bağlı tutmak, diğerini anti-paralel bağlı tristörler yardımıyla devreye alıp çıkarmak suretiyle ortadan kaldırılabilir. Işık tetiklemeli tristörler güç katı ile kontrol devresi arasındaki izolasyonu sağlayıp açık hava kurulumuna olanak sağlar.

**Anahtar Kelimeler:** C-tipi Harmonik Filtre, Ark ve Pota Ocakları, Filtre Kondansatör Aşırı Gerilimleri, Harmonikler ve İnterharmonikler

*To My Family*



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## **CHAPTER 1**

### **INTRODUCTION**

#### **1.1. GENERAL**

In terms of power quality, the need for reactive power compensation and harmonic filtering is inevitable for most of the industrial applications. Iron and Steel Industry, which is one of these applications, has been growing increasingly in Turkey in the last decade. Today, its electricity demand is nearly one tenth of the installed generation capability of 40 GW of the country. Steel production in Turkey is based on extensive use of arc and ladle furnaces in most of the plants, which is the cause of power quality problems at those locations of the Turkish Electricity Transmission System [1].

A major cost to a steel manufacturing facility is the energy used in the arc and ladle furnaces for the melting and refining processes. Operation at low power factor results in additional voltage drop through the power system yielding a lower system voltage on the plant buses. Low system voltage increases melting (tap-to-tap) time and it will add to the overall plant operating costs per ton. Low power factor can also result in additional costs in the form of penalties from the electric utility company.

Furthermore, arc and ladle furnaces are known to be a source of low order harmonics. The harmonics produced by scrap metal and ladle furnaces in practice are continuously varying due to the variability of the arc length over the total heat period. The amount of harmonic generation is dependent upon the furnace type. Moreover, even harmonics are also present in the furnace power system because of

the erratic arcing behavior that yields unequal conduction of the current for the positive and negative half-cycles [2].

## **1.2. PROBLEM DEFINITION AND SCOPE OF THE THESIS**

Ereğli Iron and Steel Plant (ERDEMİR), which is located in Zonguldak-Ereğli, is one of the biggest steel manufacturers in Turkey. It produces flat steel products in compliance with national and international standards by using advanced technology, and adds considerable value to the economy. (The products of the plant are: Hot rolled coils and sheets, cold rolled coils and sheets, tinplate coils and sheets, and galvanized coils and sheets [3].) The plant owns an 18 MVA ladle furnace (LF) supplied from a 20 MVA, 13.8/0.327 kV furnace transformer. The power factor (*pf*) of the furnace is around 0.75-0.8 lagging. Moreover, it injects harmonic currents mainly of order 2, 3, 4, and 5 to the supply.

According to the regulations published by the Ministry of Energy and Natural Resources and The Energy Market Regulatory Authority in January 2007, the inductive reactive energy and capacitive reactive energy consumptions in the monthly electrical energy bills should not exceed respectively 20% and 15% of the associative active energy consumption. This necessitates keeping the average *pf* of the industrial plant on monthly basis between 0.98 lagging and 0.99 leading [4].

On the other hand, according to the recent harmonic standard (IEEE Std 519-1992 [5]), now there are stricter limits for individual voltage and current harmonics at the point of common coupling (PCC).

In order to provide the necessary fluctuating reactive power for the LF while eliminating the 2<sup>nd</sup> harmonic current, a Static VAr Compensation (SVC) System is to be installed within the scope of a contracted SVC project signed between TÜBİTAK-UZAY Institute-Power Electronics Group and ERDEMİR Authority.

This SVC project includes the installation of a 16 MVAR Thyristor Controlled Reactor (TCR), and a 14.2 MVAR C-type 2<sup>nd</sup> harmonic filter (HF) as the first phase. The second phase of the project includes the installation of another 16 MVAR TCR and a 16 MVAR single-tuned 3<sup>rd</sup> HF. This is because; ERDEMİR is planning to install a new LF which has the same specifications with the currently installed one. After the installation of 2<sup>nd</sup> LF, the second phase of the project will be implemented.

The author of this thesis has worked on the design and optimization of C-type 2<sup>nd</sup> HF for this project. The detailed analysis of the harmonic, interharmonic and flicker problems of the LF, together with the problems caused by the LF transformer energizations have given rise to a novel design of C-type 2<sup>nd</sup> HF. The author's claim is that a C-type HF with two different operation modes is necessary for the sake of filter performance optimization for steady and transient states, and filter safe operation. Due to the large amount of 2<sup>nd</sup> harmonic current injected to the 13.8 kV supply side by the LF transformer during energization, the C-type HF has to be operated in a highly-damped (no filtering) mode, whereas it should be operated in a low-damping (filtering) mode for normal LF operation. At first sight, the easiest solution seems to switch off the harmonic filter after the furnace transformer breaker is opened and to wait for the breaker to be closed before switching in the harmonic filter. This method prevents any transient current and voltage due to the magnetizing inrush current of the furnace transformer affecting the filter components. However, switching the filter itself is in fact a source of transient currents and voltages, thus this method will not be a feasible solution regarding the filter breaker life and the filter elements. Another solution is to design a highly damped filter by using a low resistance value. However, in this case, due to high damping, the losses will increase, the filtration characteristics will be severely affected and it will not be possible to filter out the harmonic current effectively. Therefore, a novel approach is required to achieve both good filtration and transient performance. This approach is mainly using a permanently connected high-value resistor in parallel with a temporarily connected low-value resistor switched in and out by semi-conductor devices, namely Light Triggered Thyristors. The organization of the thesis is as follows:

The second chapter discusses the characterization of arc and ladle furnaces as an electrical load and includes the real time field data analysis for the ERDEMİR LF. The problematic LF transformer energizations are also investigated.

The third chapter includes the solution methods for harmonic mitigation, reactive power and flicker compensation techniques especially for LF applications, discusses their advantages and disadvantages. The design of the optimized C-type 2<sup>nd</sup> HF is also discussed in this chapter. The simulation results for different damping values are compared and the harmonic and interharmonic mitigation performances are discussed together with the flicker issue.

The fourth chapter includes the implementation and installation work of the filter. The specifications of the equipment that will be used are given in this chapter. The control algorithm for the solid-state switching is also given and the designed electronic cards are described. Also the laboratory test results for solid-state switches, triggering unit and electronic cards are given. The installation photographs of the whole system are included in this chapter.

The final chapter summarizes the contributions of the thesis, provides the concluding remarks, and recommends future work.

## **CHAPTER 2**

### **CHARACTERIZATION OF ARC AND LADLE FURNACES AS A LOAD ON THE NETWORK**

#### **2.1. ARC AND LADLE FURNACES**

An AC Electrical Arc Furnace (EAF) is an unbalanced, nonlinear and time variant load that produces unbalance, harmonics and interharmonics related with flicker effect. For a power distributor, a modern steel plant represents a somewhat dubious customer. On the one hand, the plant may be the biggest paying consumer in the distribution system; on the other hand, the same consumer through the nature of his load disturbs power quality for the other consumers connected to the network [6, 7].

An EAF heavily consumes not only active power, but also reactive power. The physical process inside the furnace (electric melting) is erratic in its nature, with one or several electrodes striking electric arcs between furnace and scrap. As a consequence, the consumption especially of reactive power becomes strongly fluctuating in a stochastic way. The voltage drop caused by reactive power flowing through circuit reactances therefore becomes fluctuating in an erratic way, as well. This gives rise to voltage flicker and it is visualized most clearly in the flickering light of incandescent lamps fed from the polluted grid [8].

In a LF; flicker, reactive power, unbalance, and harmonic problems are not as severe as those of AC EAFs. If the short-circuit MVA rating of the bus bar to which the LF is connected is high enough, then only harmonic and reactive power compensation problems arise [9].

The arc is something of a white noise generator, superimposing a band of higher frequencies on the system, especially during times of extreme arc instability, such as in the early melting period. This means that the arc can generate frequencies that are directly in the highest amplification band of the filter circuit [10].

For an inductive feeding network, which is the most common, it is mathematically simple to show that setting the plant reactive power at a low value with small fluctuation in time, the network voltage quality will increase considerably even if the fluctuation in active power still exists.

It is important when designing steel plant power supply that the installation of an SVC should not be considered at the final stage when all other equipment has already been sized and ordered, but instead it should be a part of an optimization plan for a complete power supply system for a steel plant. This is valid both for brand-new green-field plants and for revamping and extensions of existing plants [7].

It is evident that the reactive power compensation of an arc or ladle furnace can not be made simply by harmonic filters alone. A parallel TCR should be also installed in order to compensate for the fluctuating reactive power. Otherwise, the furnace would be overcompensated in the capacitive region and the  $pf$  limits would be violated which leads to penalties.

The HFs for the LF should be designed based on the real time field data. The reactive power peak consumption, maximum and average harmonic current injection of the furnace should be well known before making the design. It is mentioned in the literature [9] that the ladle furnace harmonics are approximately as given in Table 2.1. This table includes real data gathered from İSDEMİR LF.

Table 2.1 shows that for a LF, the need for a 2<sup>nd</sup> HF alone is not so vital in fact. When a 3<sup>rd</sup> HF is installed, however, due to the parallel resonance with the supply, 2<sup>nd</sup> harmonic component increases. Moreover, a TCR injects 2<sup>nd</sup> harmonic current to the supply. These facts may give rise to the need for a 2<sup>nd</sup> HF because the harmonic



limits may be exceeded. The harmonic values given in Table 2 had been calculated with 50 Hz bandwidths. However, according to the recent standards, the harmonic measurements should have been made by using 5 Hz bandwidths and combining them. This issue is discussed in Section 3.1.7.

**Table 2.1 İSDEMİR Ladle Furnace Harmonic Currents**

Harmonic Order	İsdemir Ladle Furnace, %		İsdemir Ladle Furnace, % with 3 <sup>rd</sup> Harmonic Filter	
	The most expected	Maximum	The most expected	Maximum
2	2.0	6.0	3.0	8.0
3	5.5	8.5	3.5	7.0
4	1.5	3.5	1.0	3.0
5	2.5	4.5	2.0	3.5
6	0.8	2.5	0.5	1.5
7	1.4	1.8	1.0	1.5
8	0.6	1.2	0.5	1.0
9	0.7	1.0	0.5	0.8
10	0.5	0.8	0.4	0.8
11	0.5	0.8	0.3	0.8
12	0.4	0.6	0.2	0.6
13	0.5	0.7	0.3	0.7
<b>TDD</b>	<b>7.0</b>	<b>10.0</b>	<b>6.0</b>	<b>10.0</b>

Table 2.1 includes only the harmonic current components for steady state operation of the furnace. Any transient event such as switching of the harmonic filter or the initiation of the first arcing of the electrodes should be taken into consideration for the determining peak levels of the filter components' currents and voltages. Another harmonic current producing source is the energization of scrap metal and ladle furnace transformers. This is a case where the distinction between harmonics and transients becomes less clear [2].

## **2.2. TRANSFORMER INRUSH PHENOMENA**

### **2.2.1. General**

Transformers used in industrial facilities such as furnace installations are switched many times during a twenty-four-hour period. Each energization of the transformer will generate a transient inrush current rich in harmonics. This inrush current is dependent on several factors. In fact, the magnetizing inrush current may result from not only energization of the transformer but also may occur due to: [11]

- (a) Occurrence of an external fault,
- (b) Voltage recovery after clearing an external fault,
- (c) Change of the character of a fault (for example when a phase-to-ground fault evolves into a phase-to-phase-to-ground fault), and
- (d) Out-of-phase synchronizing of a connected generator.

In other words, magnetizing inrush current in transformers results from any abrupt change of the magnetizing voltage. However, in this thesis, only the energization case will be mentioned and taken into consideration from now on because it is the case for the LF transformer of ERDEMİR, which is under the investigation of this study and furthermore, energization of the transformer results in the worst case of all.

The transformer inrush current includes both even and odd harmonics which decay in time, until the transformer magnetizing current reaches a steady state [12]. The most predominant harmonics, during transformer energization, are the second, third, fourth, and fifth in descending order of magnitude. Some typical magnitudes of the energization inrush current harmonics are given in Table 2.2.

During energization, since the flux could reach three times that of its rated value, the inrush current could be extremely large (For example, 10 times that of the rated load current of the transformer). Inrush currents have a significant impact on the supply system and neighboring facilities. Some of the major consequences are listed below: [13]

**Table 2.2** Typical Magnitudes of the Transformer Energization Inrush Current Harmonics

Harmonic	Magnitude
2nd harmonic	21.6% of <b>X</b> .Full load current
3rd harmonic	7.2% of <b>X</b> .Full load current
4th harmonic	4.6% of <b>X</b> .Full load current
5th harmonic	2.8% of <b>X</b> .Full load current
Where <b>X</b> is a constant typically between 5 and 12	

i) A large inrush current causes voltage dips in the supply system, so customers connected to the system including manufacturing facilities of the generator owner will experience the disturbance. Such a disturbance could lead to mal-operation of sensitive electronics and interrupt the manufacturing process.

ii) A step-up transformer consists of three phases. When it is energized, the inrush current will be highly unbalanced among the three phases. Protective relays of motors are very sensitive to unbalanced three-phase currents. Therefore unbalance caused by inrush current could easily result in motor tripping.

iii) The waveform of an inrush current is far from sinusoidal. It contains a lot of low order harmonics. Such harmonics could excite resonance in the system, causing significant magnification of voltages or currents at various locations in the system. Sensitive electronic devices could respond and equipment could be damaged.

iv) The DC component of the inrush current can lead to oscillatory torques in motors, resulting to increase motor vibration and aging.

The extent to which power quality is degraded depends on short circuit MVA at the source bus, and the magnitude and decay time constant of the transient current.

### **2.2.2. Transformer Inrush due to Switching in [11]**

Vacuum switches (vacuum circuit breakers) are used extensively in power systems including arc and ladle furnaces, due to the operating characteristics of these installations and the maintenance requirements of the switches. Low maintenance, long operating life, and the absence of any exhaust make vacuum switches well suited for highly repetitive switching operations such as those found on arc and ladle furnace power systems [14]. These switches are intentionally used because, energizing of a furnace transformer 50-60 times a day is not unusual. A normal circuit breaker would fail much earlier than a vacuum circuit breaker for an operation like this.

Energization inrush currents occur when a system voltage is applied to a transformer at a specific time when the normal steady-state flux should be at a different value from that existing in the transformer core. For the worst-case energization, the flux in the core may reach a maximum of over twice the normal flux. For flux values much higher than normal, the core will be driven deep into saturation, causing very high-magnitude energization inrush current to flow. The magnitude of this current is dependent on i) the rated power of the transformer, ii) the impedance of the supply system from which the transformer is energized, iii) magnetic properties of the core material, iv) remanence in the core, v) the moment when the transformer is switched in, and vi) the way the transformer is switched in. This initial energization inrush current could reach values as high as 25 times full-load current and it will decay in time until a normal exciting current value is reached. Values of 8 to 12 times full-load current for transformers larger than 10 MVA with or without load tap changers had been reported in the literature. The decay of the inrush current may vary from times as short as 20 to 40 cycles to as long as minutes for highly inductive circuits [12]. The parameters that affect the inrush current magnitude are explained below:

#### **i) Rated power of the transformer**

The peak values of the magnetizing inrush current are higher for smaller transformers while the duration of this current is longer for larger transformers. The

time constant for the decaying current is in the range of 0.1 of a second for small transformers (100 kVA and below) and in the range of one second for larger units.

**ii) Impedance of the system from which the transformer is energized**

The inrush current is higher when the transformer is energized from a powerful system. Moreover, the total resistance seen from the equivalent source to the magnetizing branch contributes to the damping of the current. Therefore, transformers located closer to the generating plants display inrush currents lasting much longer than transformers installed electrically away from the generators.

**iii) Magnetic properties of the core material**

The magnetizing inrush is more severe when the saturation flux density of the core is low. Designers usually work with flux densities of 1.5 to 1.75 Tesla. Transformers operating closer to the latter value display lower inrush currents.

**iv) Remanence in the core**

Under the most unfavorable combination of the voltage phase and the sign of the remnant flux, higher remnant flux results in higher inrush currents. The residual flux densities may be as high as 1.3 to 1.7 Tesla. Since the flux cannot instantaneously rise to peak value, it starts from zero and reaches 1 p.u. after 1/4 cycle and continues to increase until it becomes approximately 2 p.u. (peak) half-cycle after switching. This phenomenon is commonly referred to as the flux doubling-effect. If there is any remnant flux present prior to switching, and its polarity is in the direction of flux build-up after switching, the maximum flux can even exceed 2 p.u.

**v) Moment when a transformer is switched in**

The highest values of the magnetizing current occur when the transformer is switched at the zero transition of the winding voltage, and when in addition, the new forced flux assumes the same direction as the flux left in the core. In general, however, the magnitude of the inrush current is a random factor and depends on the point of the voltage waveform at which the switchgear closes, as well as on the sign

and value of the residual flux. It is approximated that every 5<sup>th</sup> or 6<sup>th</sup> energizing of a power transformer results in considerably high values of the inrush current.

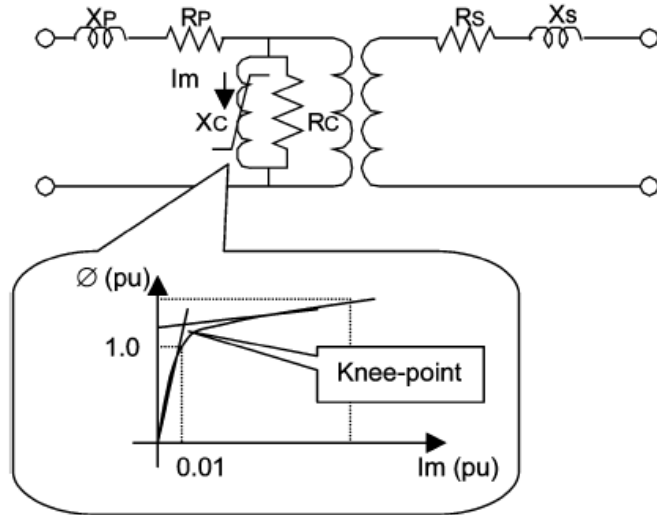
**vi) Way a transformer is switched in**

The maximum inrush current is influenced by the cross-sectional area between the core and the winding which is energized. Higher values of the inrush current are observed when the inner (having smaller diameter) winding is energized first. It is approximated, that for the transformers with oriented core steel, the inrush current may reach to a value 5-10 times the rated value when the outer winding is switched-in first, and 10-20 times the rated value when the inner winding is energized first. Due to the insulation considerations, the lower voltage winding is usually wound closer to the core, and therefore, energizing of the lower voltage winding generates higher inrush currents.

Some transformers may be equipped with a special switchgear which allows switching-in via a certain resistance. The resistance reduces the magnitude of inrush currents and substantially increases their damping.

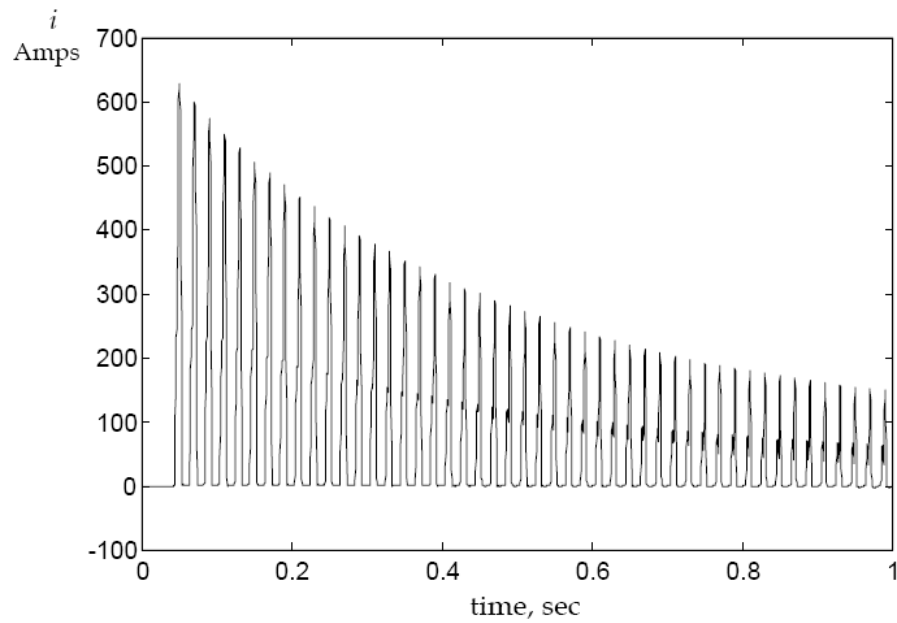
In contrast, when a transformer is equipped with an air-type switch, then arcing of the switch may result in successive half cycles of the magnetizing voltage of the same polarity. The consecutive same polarity peaks cumulate the residual flux and reflect in a more and more severe inrush current. This creates extreme conditions for transformer protection and jeopardizes the transformer itself.

The equivalent circuit model of a power transformer is given in Figure 2.1. In this figure,  $X_p$  and  $R_p$  represent the primary winding reactance and resistance respectively, whereas  $X_s$  and  $R_s$  represent the secondary winding reactance and resistance respectively. The magnetizing branch is thought as a saturated inductor in parallel with the core resistance.



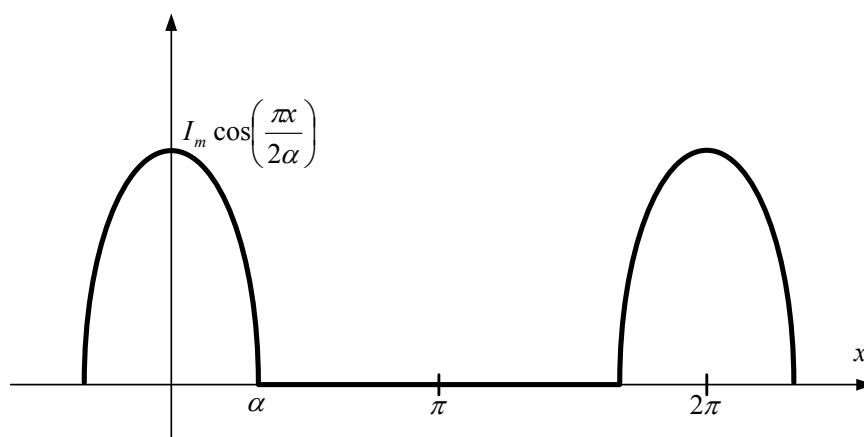
**Figure 2.1** Equivalent Circuit Model of a Power Transformer [15]

Analyzing the circuit in Figure 2.1, one can conclude that, the inrush current cannot exceed  $1/(X + X_p + X_c(\min))$  p.u., where  $X$  is the source reactance of the bus from which the transformer is energized. The minimum magnetizing reactance,  $X_c(\min)$ , represents the maximum possible flux build-up after the transformer energization. Although  $X_c(\min)$  can be estimated from the open circuit test and the hysteresis characteristic of the transformer iron core, it is not as readily available as the nameplate data. Since the transformer iron core behaves like an air core at such a high degree of saturation, the air core inductance is typically two times the short circuit impedance i.e.,  $X_c(\min)$  can be typically assumed as  $2(X_p + X_s)$  or  $2X_T$ .  $X_T$  is the sum of the primary and secondary leakage reactances, and it is available from the nameplate data. Substituting the typical value of  $X_c(\min)$ , the inrush current cannot exceed  $1/(X + X_p + 2X_T)$  p.u. Although the leakage reactances of individual windings are not available, in most practical studies they are assumed as equal, i.e.,  $X_p$  or  $X_s$  is equal to  $X_T/2$ . Thus, the maximum voltage sag can be estimated as  $X/(X + 2.5X_T)$  p.u.” [15] The time required for inrush current to decay depends on the resistance and reactance of the circuit, including the transformer’s magnetizing reactance.



**Figure 2.2** A Typical Transformer Inrush Current [11]

A typical transformer inrush current is given in Figure 2.2. By doing a simplified mathematical one-period analysis of this current waveform (Figure 2.3) harmonic content of the inrush current waveform can be calculated.



**Figure 2.3** One period of the Transformer Inrush Current Waveform



In Figure 2.3, the angle  $\alpha$  is assumed to be a parameter. The amplitude of the  $n^{\text{th}}$  harmonic of the current waveform is calculated as:

$$A_n = \frac{I_m}{\pi} \left[ \frac{1}{n+1} \sin((n+1)\alpha) + \frac{1}{n-1} \sin((n-1)\alpha) - 2 \cos\left(\frac{\alpha}{n}\right) \sin(n\alpha) \right] \quad (2.1)$$

The second harmonic always dominates because of a large dc component. However, the amount of the second harmonic may drop below 20%. The minimum content of the second harmonic depends mainly on the knee-point of the magnetizing characteristic of the core. The lower the saturation flux density, the higher the amount of the second harmonic becomes.

Modern transformers built with the improved magnetic materials have high knee-points, and therefore, their inrush currents display a comparatively lower amount of the second harmonic.

Another issue is that the inrush currents measured in separate phases of a three-phase transformer may differ considerably because of the following:

- The angles of the energizing voltages are different in different phases.
- When the delta-connected winding is switched-in, the line voltages are applied as the magnetizing voltages.
- In the later case, the line current in a given phase is a vector sum of two winding currents.
- Depending on the core type and other conditions, only some of the core legs may get saturated.

From a point of measurement view, the traditional method to measure high voltage currents in transformer substations is the use of inductive current transformers (CTs). In a transformer inrush event, due to the large and slowly-decaying dc component, the inrush current is likely to saturate the CTs even if the magnitude of the current is comparatively low. When saturated, a CT introduces certain distortions to its secondary current. Due to CT saturation during inrush conditions, the amount of the measured second harmonic may drop considerably which gives rise to measurement

errors and misinterpretations [11]. Care should be taken for this case, in order to properly evaluate the inrush current peak value and DC component especially.

### **2.3. ERDEMİR LADLE FURNACE FIELD DATA**

This part includes the field measurement data gathered on 16-17 May 2006 by TÜBİTAK-UZAY Institute Power Electronics Group ERDEMİR-SVC Project researchers, at the medium voltage side (13.8 kV) of the ladle furnace transformer in ERDEMİR. The measurement had been made for a continuous 19-hour period and the following equipments had been used:

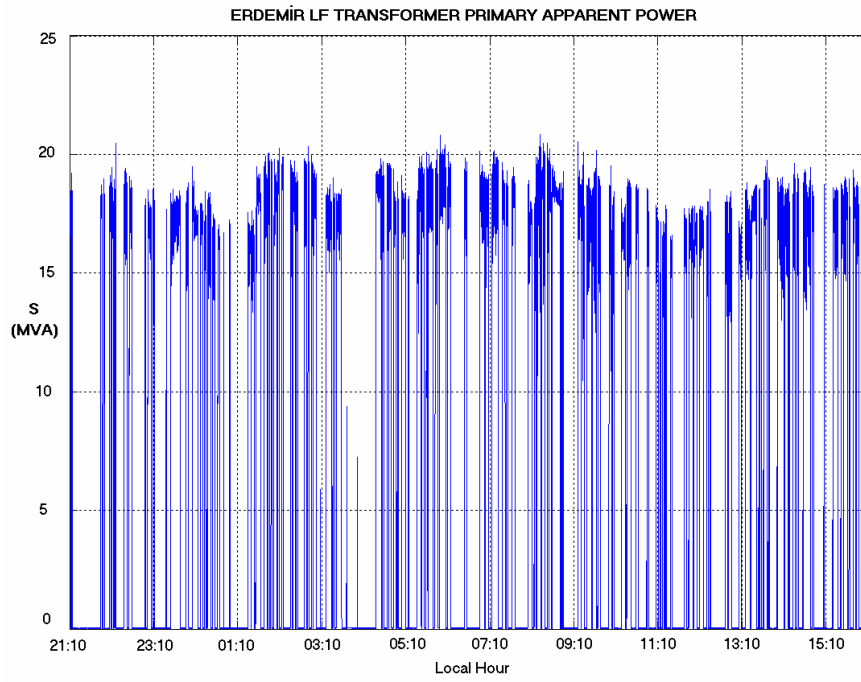
- National Instruments DAQ Card 6062E
- National Instruments SC-2040 S/H Card
- NI Labview Software
- Fluke 434 Power Quality Analyzer

3 line currents and 2 line-line voltages has been recorded with a sampling frequency of 3.2 kSample/second per channel. The turns ratio of the measurement transformers are given below:

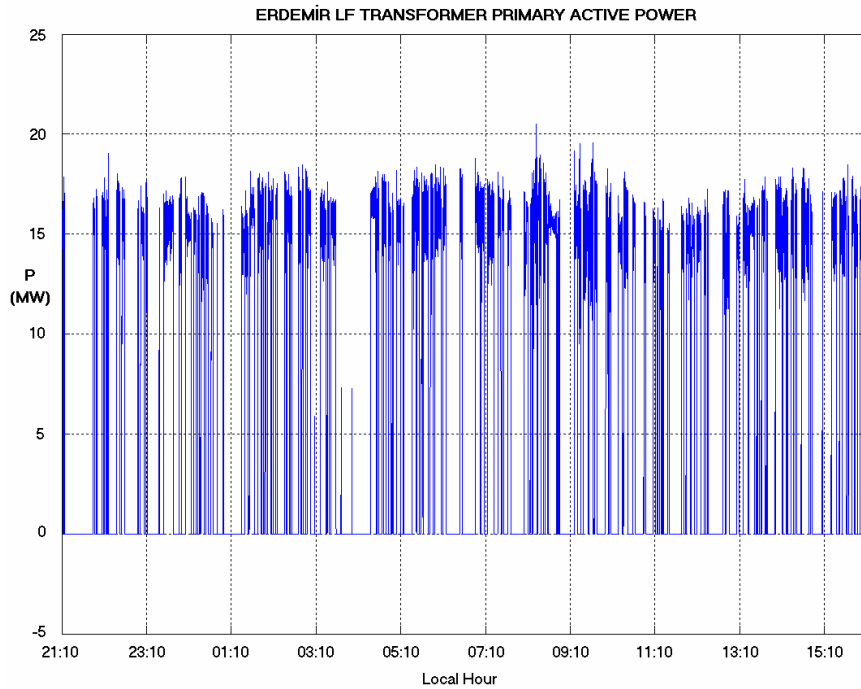
- Current Transformer Ratio: 1200/5 A
- Voltage Transformer Ratio: 13.8/0.1 kV

According to the measurements, the apparent power, real power and reactive power consumption of the LF are given in Figures 2.4, 2.5 and 2.6 respectively. The line-to-line bus voltage of the furnace transformer primary is given in Figure 2.7.

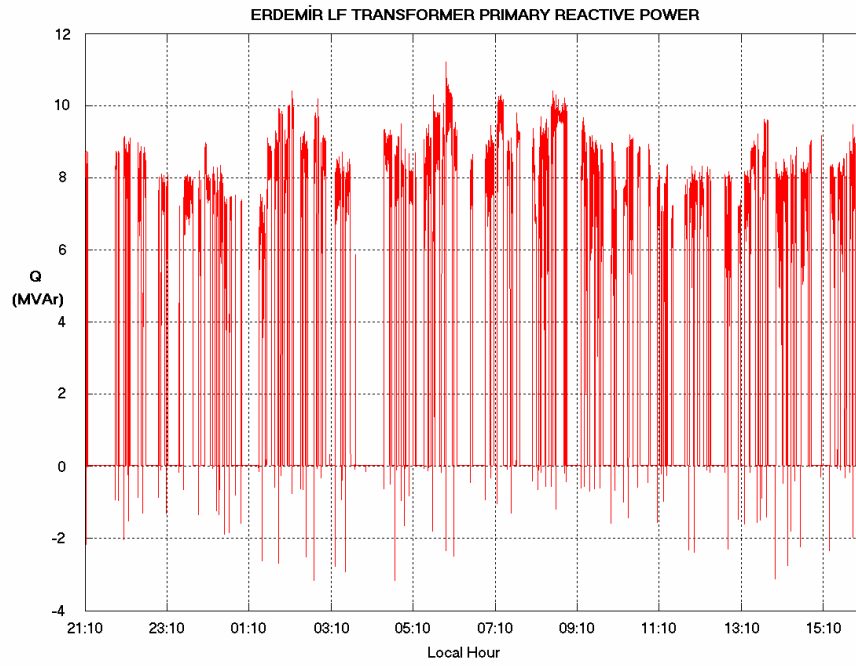
According to Figure 2.4 and 2.5, a simple calculation of  $pf = \frac{P}{S} \approx 0.8$  lagging can be made. It is seen that the LF operation is not continuous, but it lasts for 5-20 minute periods. What are not seen in these figures are the transformer energizations. A transformer energization case is given in Figure 2.8 and Figure 2.9.



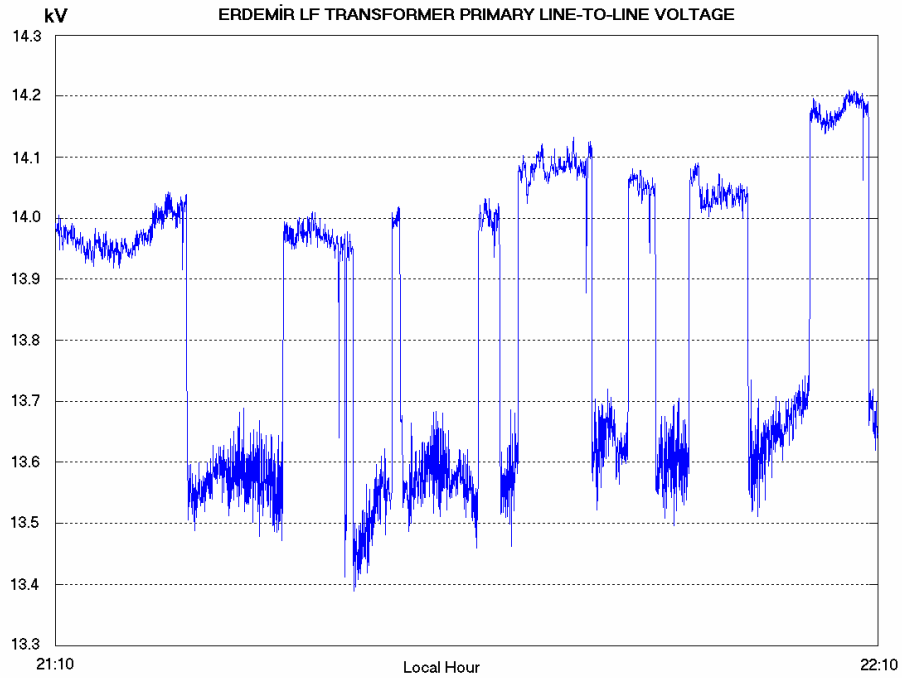
**Figure 2.4** ERDEMİR LF Transformer Measured Apparent Power



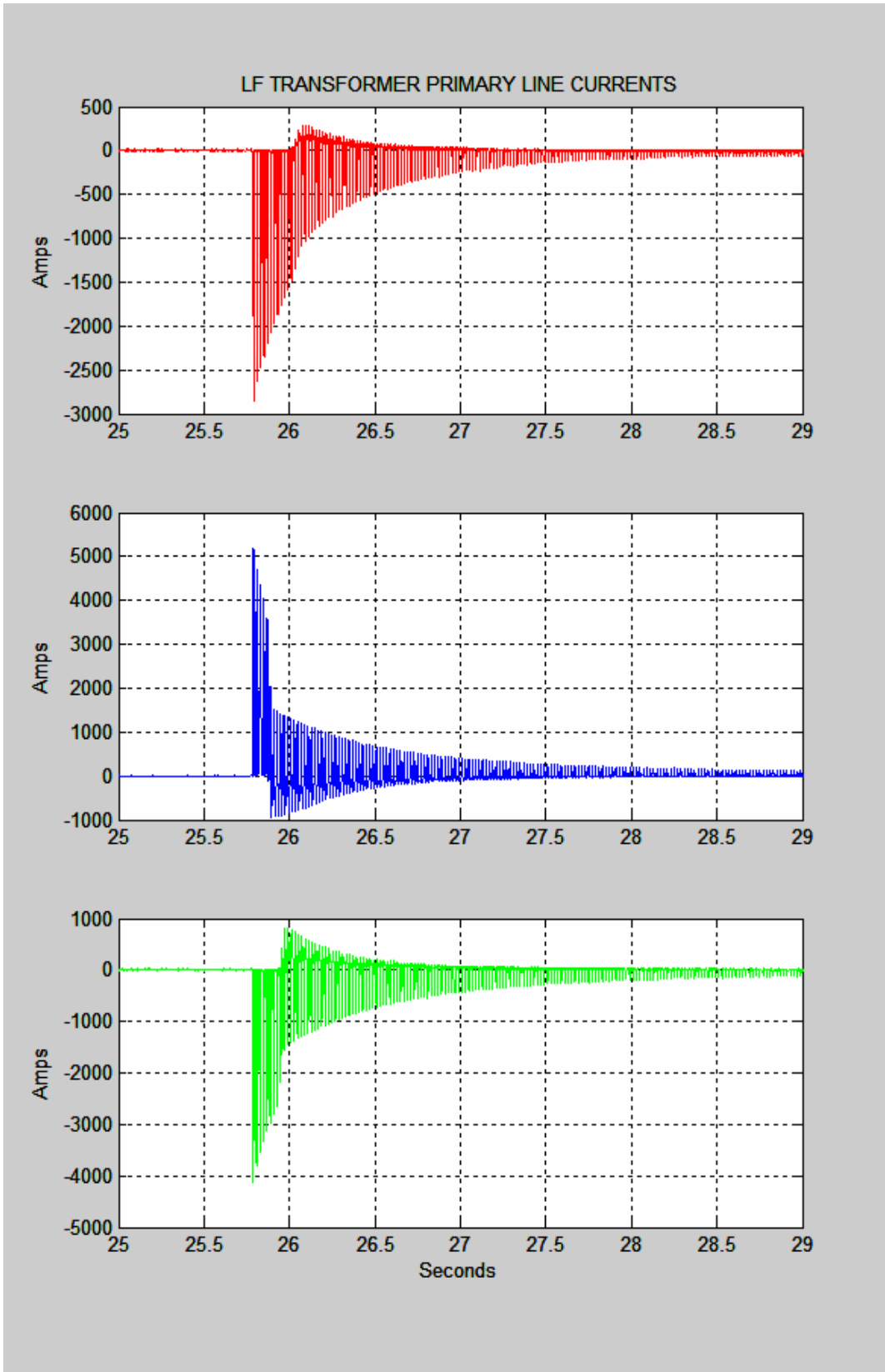
**Figure 2.5** ERDEMİR LF Transformer Measured Active Power



**Figure 2.6** ERDEMİR LF Transformer Measured Reactive Power

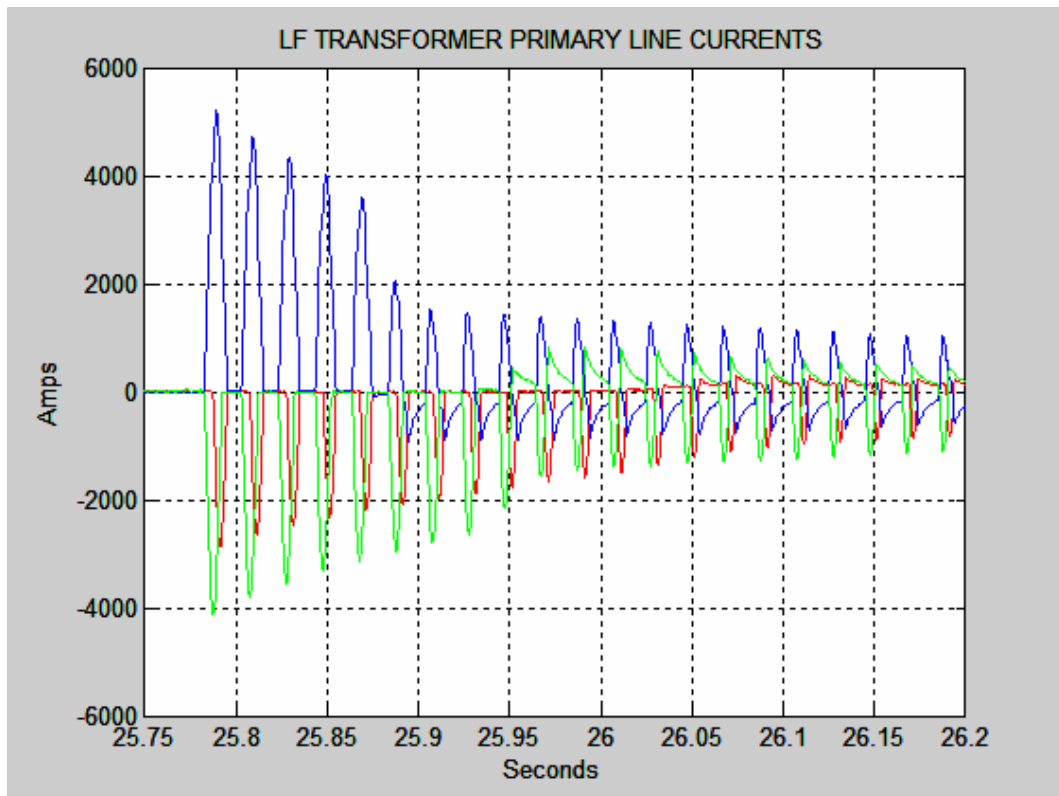


**Figure 2.7** ERDEMİR LF Transformer Measured Primary Line-to-Line Voltage



**Figure 2.8** LF Transformer Measured Primary Inrush Line Currents (4-Sec Period)

Figures 2.8 and 2.9 show the worst transformer inrush among the 19-hour measurement period. It is seen that the peak of the inrush current for one line is around 5.2 kA, whereas it is 4.0 kA and 2.5 kA for the other lines.

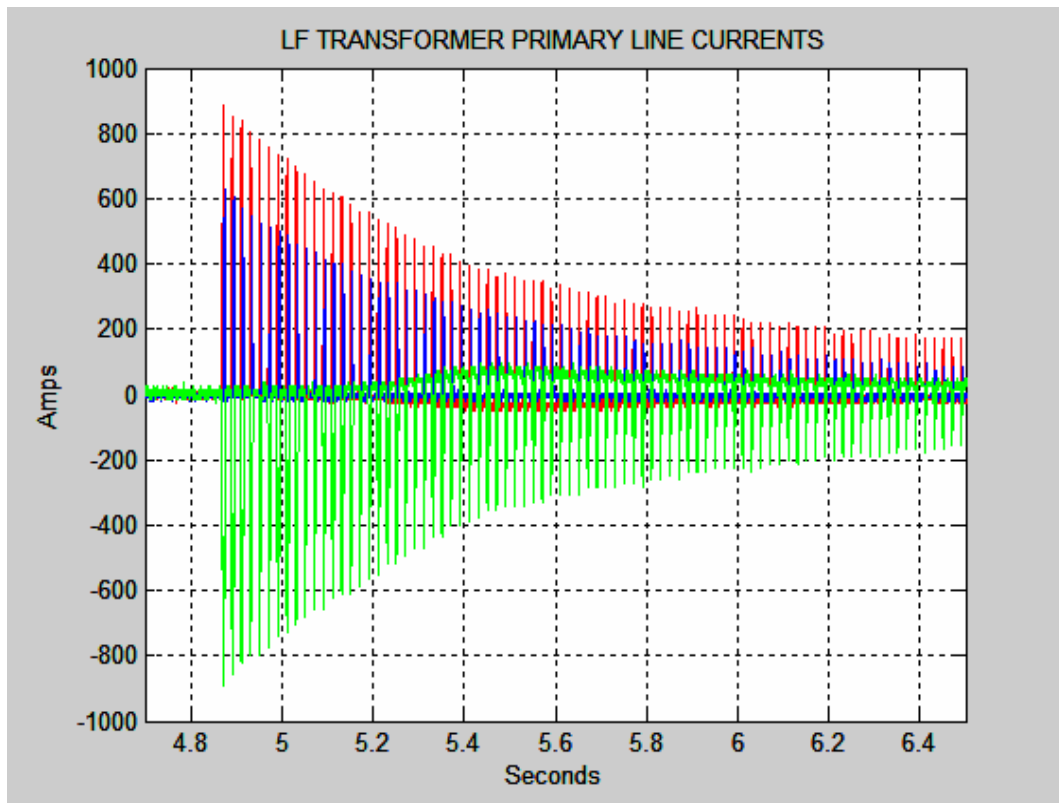


**Figure 2.9** LF Transformer Measured Primary Inrush Line Currents (0.5-Sec Period)

After examining the 19-hour period measurement, it has been seen that there exists approximately 3 transformer energizations per hour. It was also seen that not all of the transformer energizations resulted in high peak line currents as given in Figures 2.8 and 2.9, but current peaks of 2.5 kA were seen mostly. There were even inrushes with current magnitudes less than 1.0 kA. Figure 2.10 shows one of them.

Comparing Figures 2.8 and 2.9 with Figure 2.10, it is seen that the worst case inrush must be triggered by some other mechanisms. The big difference is in fact related to

the delays among the closing instants of the vacuum circuit breaker poles. A worst case combination of different closing instants of the poles may result in the biggest inrush current magnitude [16].

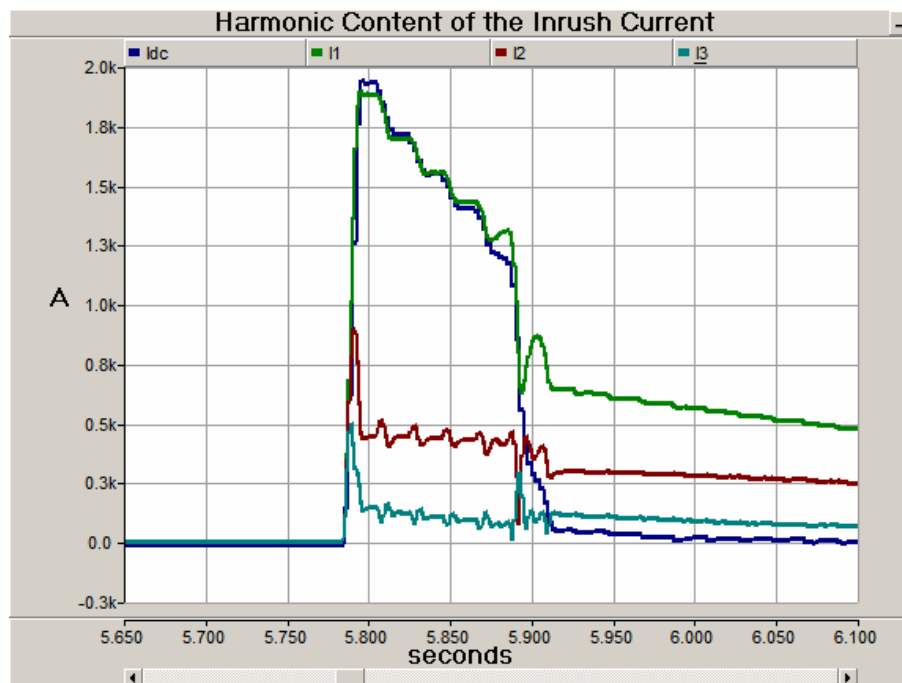


**Figure 2.10** Measured Inrush Currents Less Than 1 kA Peak

The harmonic content and the DC component of the inrush current of Figure 2.8 and 2.9 for one phase (the line with the maximum peak current) are given in Figure 2.11. In Figure 2.11, DC component is in dark blue, fundamental (50 Hz) component is in green, 2<sup>nd</sup> harmonic component is in red and the 3<sup>rd</sup> harmonic component is in light blue. It is seen that the maximum value of the 2<sup>nd</sup> harmonic reaches up to nearly 1 kA.

In Figure 2.11, it is seen that after approximately 100ms from the initiation of the inrush, the harmonic content values differ abruptly. This is because the CTs used in the current measurement go into saturation due to the high DC component of the current and they cannot measure correctly anymore.

During the normal operation of the LF, the current waveforms shown in Figure 2.12 and 2.13 are recorded. In fact, the characteristics of the current waveform evolve into a steadier and less distorted manner as the molten metal in the furnace gets homogeneous.



**Figure 2.11** The Measured Harmonic Content of the Worst Inrush Current

The harmonic content of the blue current given in Figures 2.12 and 2.13 is given in Figure 2.14. It is understood from Figure 2.14 that the 2<sup>nd</sup> harmonic component is very small and it may not cause a penalty problem. However, as mentioned before, it will increase when a 3<sup>rd</sup> HF and a TCR are installed.



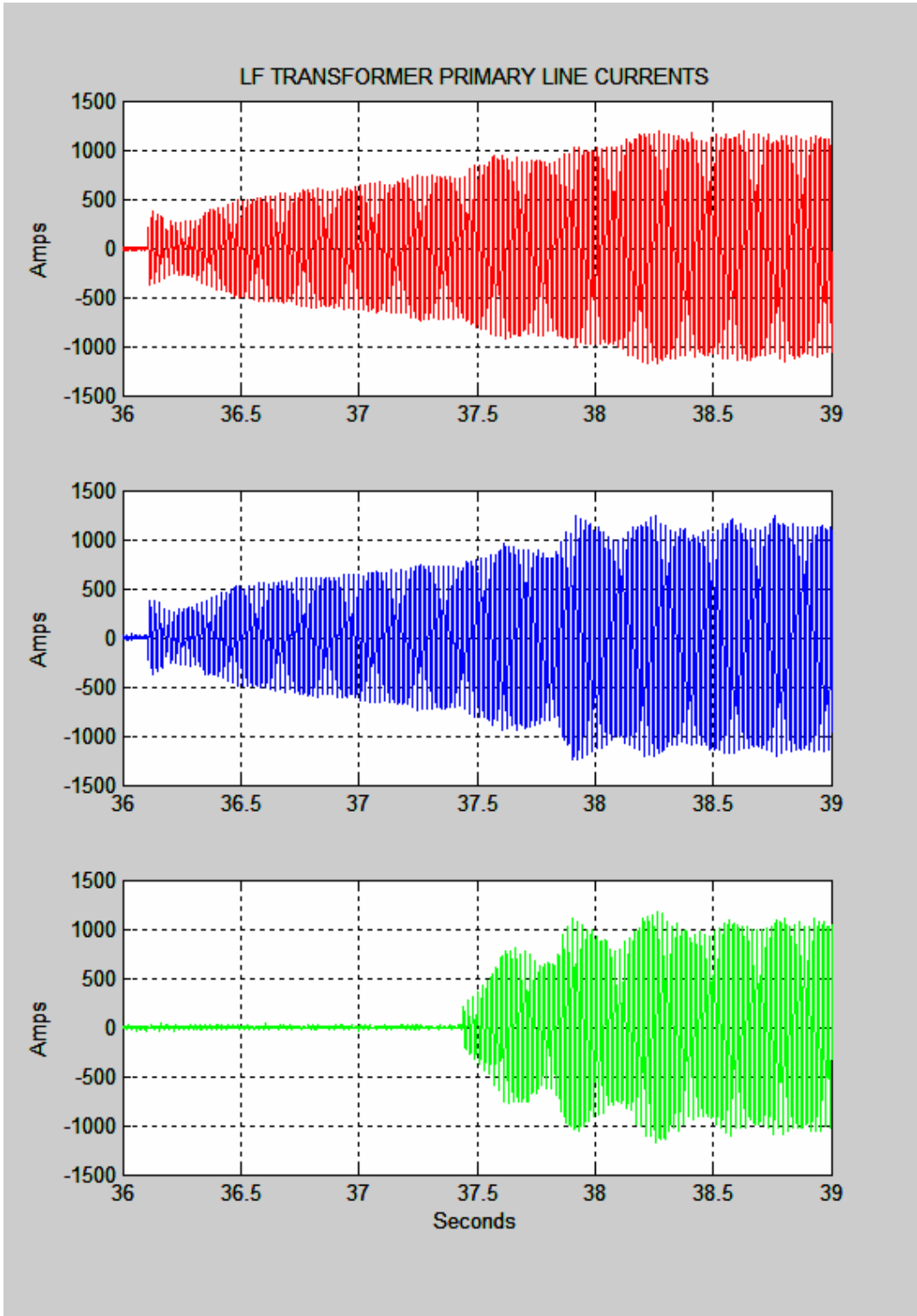
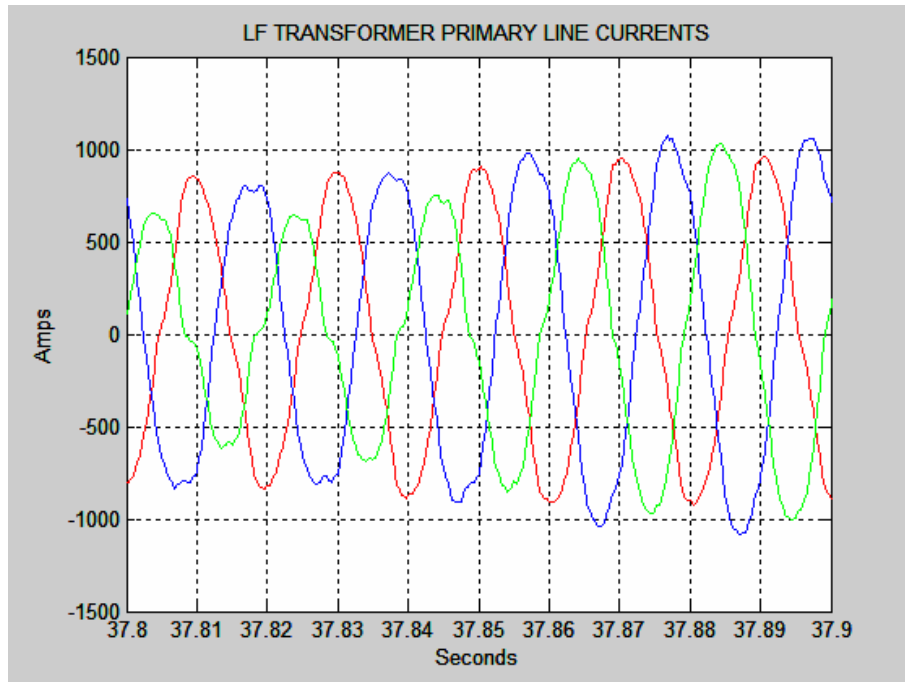
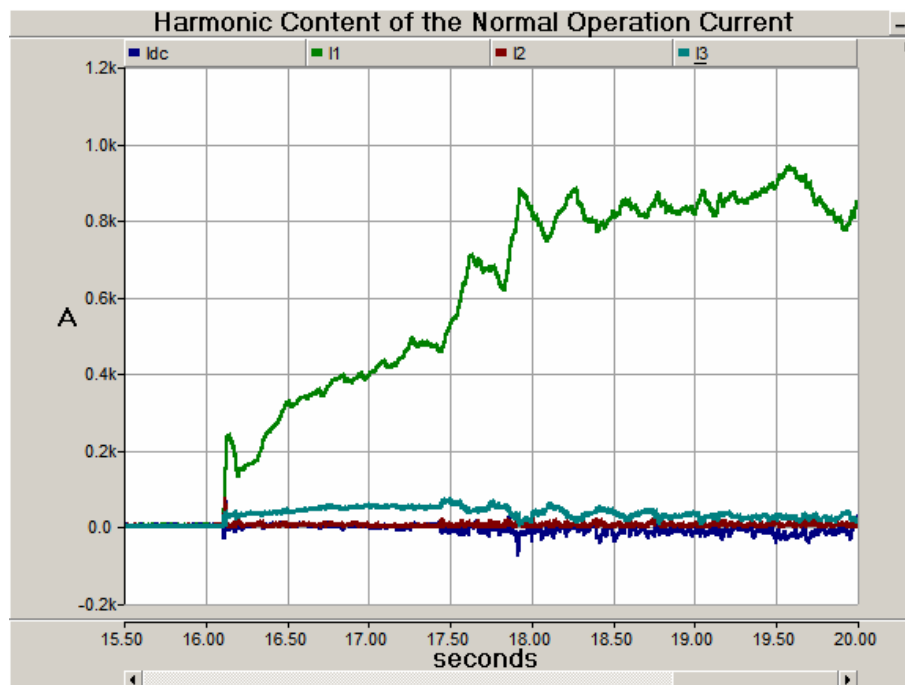


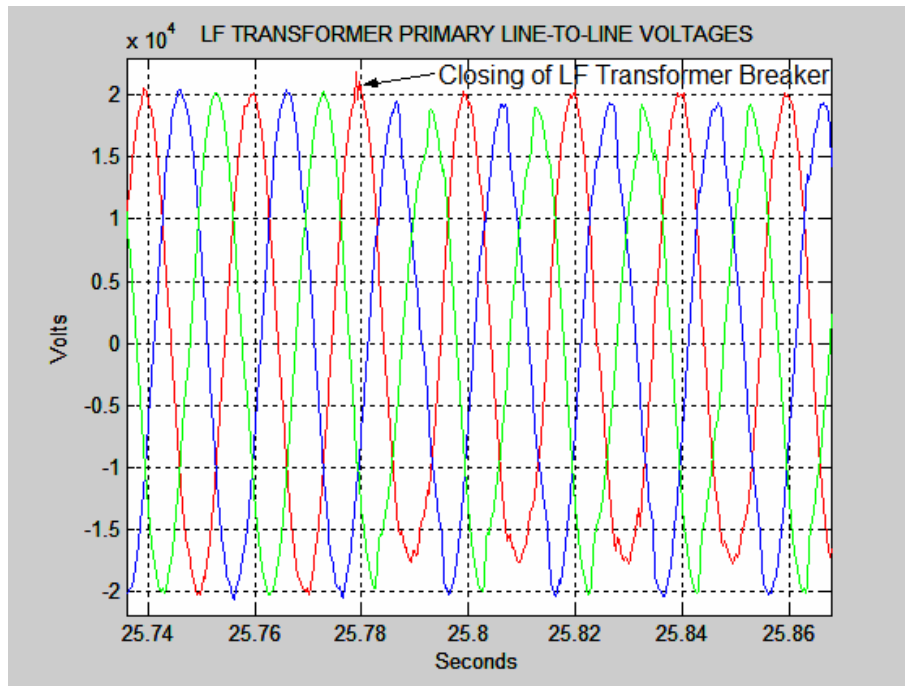
Figure 2.12 LF Transformer Measured Primary Line Currents during Normal Operation of the Furnace (4-sec period)



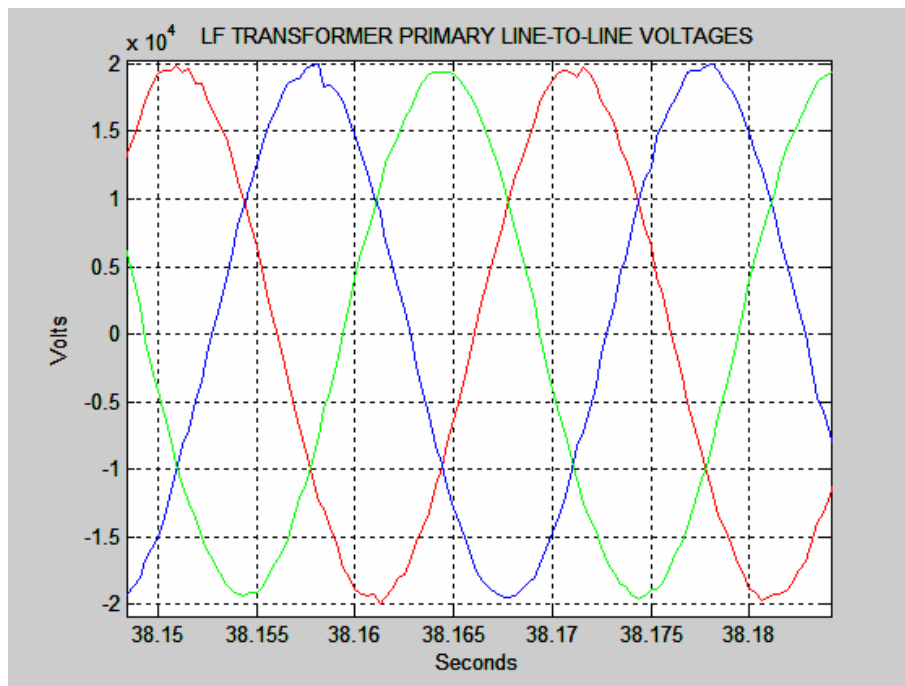
**Figure 2.13** LF Transformer Measured Primary Line Currents during Normal Operation of the Furnace (0.1-sec period)



**Figure 2.14** The Measured Harmonic Content of the Current during Normal Furnace Operation



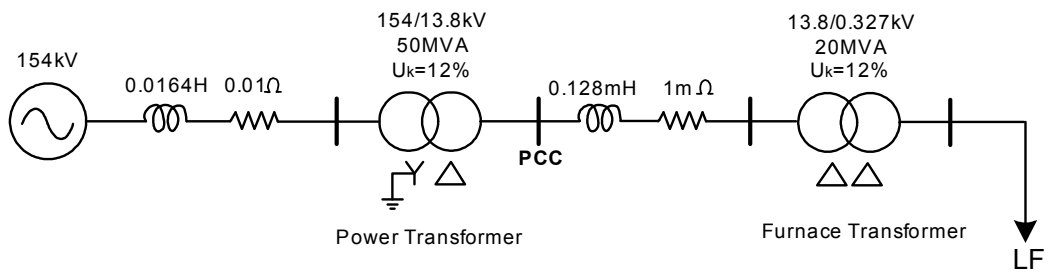
**Figure 2.15** Measured Line-to-Line Voltages at the Primary Terminals of the LF Transformer During LF Transformer Inrush



**Figure 2.16** Measured Line-to-Line Voltages at the Primary Terminals of the LF Transformer During Normal Operation of the Furnace

The line-to-line voltage at the primary terminals of the furnace transformer is given in Figure 2.15 for the transformer inrush case and given in Figure 2.16 for the normal operation of the furnace transformer.

For making the computer simulations, first the overall electrical network of the ERDEMİR LF should be modeled. Using the network data taken from ERDEMİR Management, the model given in Figure 2.17 is used in this study.



**Figure 2.17** Network Model of the System under Study

The data measured from the ERDEMİR LF transformer primary have been extensively used in PSCAD and MATLAB simulations for examining the filtering and transient state performance of the C-type 2<sup>nd</sup> HF. Chapter 3, firstly discusses the issues related to harmonics and interharmonics and then gives the detailed simulation results obtained using the field data given here.

## CHAPTER 3

### DESIGN OF THE OPTIMIZED C-TYPE 2<sup>ND</sup> HARMONIC FILTER

#### 3.1. HARMONICS

##### 3.1.1. General

The Institute of Electrical and Electronics Engineers Inc. (IEEE) defines a harmonic as a sinusoidal component of a periodic wave or quantity having a frequency which is an integral multiple of the fundamental frequency. The word harmonics originated in acoustics and describes a column of air that vibrates at frequencies that are integral multiples of the fundamental frequency. In acoustics, the fundamental frequency is the lowest frequency at which the musical instrument such as a guitar string will vibrate. The fundamental frequency of the string is determined by the length of the string.

Harmonic distortion is the mathematical representation of discontinuities in a pure sine waveform. It has been occurring since the first alternating current generator went on-line more than a hundred years ago. Harmonics generated from what was a simple electrical system were very minor and had no detrimental effects at all during that early period of time. Harmonics are not transients because harmonics have a steady state and occur cycle after cycle while transients occur at random or they are separated by a wide space of time [17].

In the Turkish Electricity System, the fundamental frequency is 50 Hz, which means that the 2<sup>nd</sup> harmonic component is located at 100 Hz, 3<sup>rd</sup> at 150 Hz, and so on.

### **3.1.2. Harmonic Sources [18]**

The main sources of harmonics before the appearance of power semiconductors were the electric arc furnaces. The other known sources were transformer magnetization nonlinearities (magnetizing inrush especially), and rotating machine harmonics. Today, with the widespread use of power electronic devices almost in every aspect of modern life, harmonic current injection is inevitable. The new harmonic generating sources are mainly:

- DC power supplies,
- Railway rectifiers,
- Three phase current and voltage source converters,
- Inverters,
- Static VAR compensators, etc.
- Cycloconverters

### **3.1.3. Effects of Harmonics**

#### **3.1.3.1. General Effects [17]**

Harmonics have been shown to have deleterious effects on equipment including transformers, rotating machines, switchgear, capacitor banks, fuses, and protective relays. Transformers, motors, and switchgear may experience increased losses and excessive heating. Induction motors may refuse to start (cogging) or run at subsynchronous speeds. Circuit breakers may fail to interrupt currents due to improper operation of blowout coils. Capacitors may prematurely fail from the increased dielectric stress and heating. The time-current characteristics of fuses can be altered, and protective relays may experience erratic behavior [19].

Additional losses due to harmonic voltages and current include; increased  $I^2R$  losses, increased stray motor losses, increased high frequency rotor and stator losses, and increased tooth pulsation losses. Harmonics can also produce torsional oscillations of the motor's shaft. Positive sequence harmonics are classified as harmonic numbers 1, 4, 7, 10, 13, etc., which produce magnetic fields and currents that rotate in the same

direction as the fundamental frequency harmonic. Harmonic numbers such as 2, 5, 8, 11, 14, etc., are classified as negative sequence harmonics which produce magnetic fields and currents rotating in the opposite direction to the positive sequence fields and currents. Zero sequence harmonics (numbers 3, 9, 15, 21 etc.) do not produce any usable torque or any adverse effects on a motor, but they develop heat and create a current in the neutral of a 3-phase 4-wire power distribution system.

In 3-phase, 4-wire circuits, the weakest link of the circuit is usually the connectors on the shared neutral conductor. Power factor correction capacitors in plants are susceptible to power systems containing large voltage or current harmonics. Because capacitive reactance is inversely proportional to frequency, capacitor banks can act like a sink to unfiltered harmonic currents and become overloaded. Another more serious cause of capacitor bank failure is harmonic resonance. When the capacitive and inductive reactances within an electrical system become equal, resonance occurs. Both series and parallel resonance can occur in a harmonic rich environment.

#### **3.1.3.2. Series Resonance**

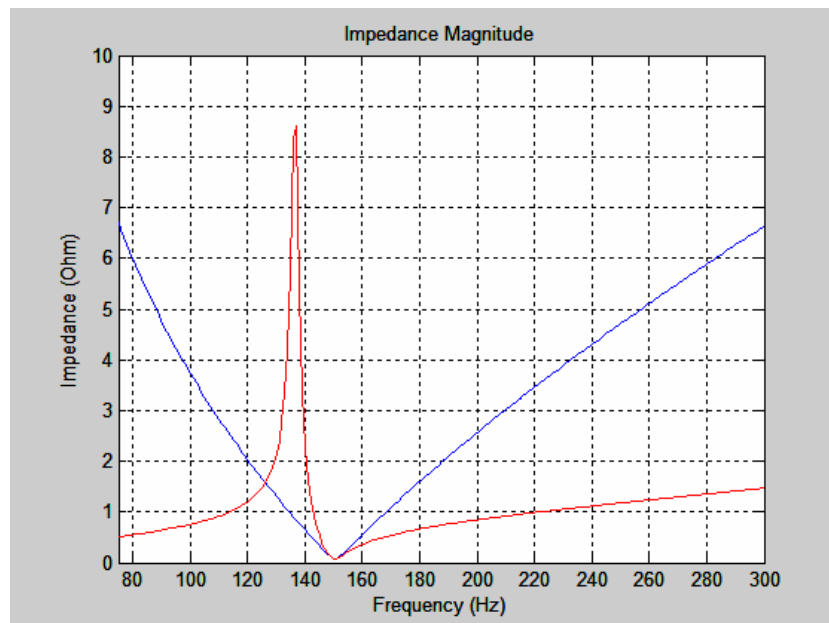
The total impedance at the resonant frequency reduces to the resistive component only. Therefore, the equivalent impedance seen by the harmonic current would be very low and a high current would flow at the resonant frequency [20]. This fact is commonly used for the harmonic current mitigation in a network. If harmonic problems exist in a system, the cheapest and simplest way to solve is to sink the harmonic currents into a relatively lower impedance path at that harmonic frequency. This is called passive shunt filtering and it will be the topic of Section 3.1.5.

#### **3.1.3.3. Parallel Resonance**

Parallel resonance occurs at a frequency when the shunt capacitance reactance becomes equal to the system equivalent shunt inductive reactance. The total impedance seen by harmonic current would be very high at the resonant frequency. A high current circulates in the capacitance-inductance loop [20]. This is often an

inevitable result of passive shunt filtering. Although the impedance of the filter for a specific frequency is very low, the filter impedance in parallel with the network impedance to a harmonic current source becomes very high at a frequency which is below the filtering frequency. This may cause serious voltage and current amplification problems in not only the HF, but also in the whole network.

A sample case including both the series and the parallel resonance is given in Figure 3.1. The filter is tuned to 150 Hz and sinks almost all of the harmonic current. However, around 135 Hz, which corresponds to the parallel resonant frequency, 1 A current injection from the harmonic source will generate 8.5 V amplification at the common connection point of the filter and the network.



**Figure 3.1** Series and Parallel Resonance Example  
(Blue: Filter Alone, Red: Filter and the Power System)

Since harmonic currents and voltages present a disturbing effect for the electrical network, there are some standards that limit the harmonic content for customers with different power and voltage ratings.



### 3.1.4. Harmonic Standards

When a harmonic current generating consumer connects to the electrical grid, a voltage drop on the impedance of the grid which is proportional to the harmonic current magnitude is created. Thereby, apart from just causing the circulation of excess current, this harmonic generating customer disturbs the power quality of the electrical grid. When other consumers connect to the same grid, due to the distorted voltage, their electronic control equipment may face serious problems. Thus, the electric utility defines limits for the harmonic contents of consumers in order to both protect both themselves and the other consumers at the point of common coupling (PCC). The most commonly used standards are the IEC 61000 series and the IEEE Std 519-1992. The adopted version of the latter one is also used in Turkey. According to IEEE Std-1992, the harmonic limits for the current at distribution level (between 1.0 and 34.5 kV) are given in Table 3.1.

**Table 3.1** IEEE Std 519-1992 Harmonic Current Limits

$I_{SC}/I_{L1}$	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	TDD (%)
<20	4	2	1.5	0.6	0.3	5
20-50	7	3.5	2.5	1	0.5	8
50-100	10	4.5	4	1.5	0.7	12
100-1000	12	5.5	5	2	1	15
>1000	15	7	6	2.5	1.4	20

The values in Table 3.1 are percentages of the fundamental (50 Hz) component; where  $h$  represents the harmonic order,  $I_{SC}$  is the short circuit current of the network, and  $I_{L1}$  is the rated current of the load. The values in Table 3.1 are true for the odd harmonics. For even harmonics, the limit is 0.25 of the odd harmonic following that even harmonic. The same standard also includes the voltage distortion limits as given in Table 3.2.

**Table 3.2** IEEE Std 519-1992 Voltage Distortion Limits

Bus voltage at PCC	individual component (%)	Maximum THD (%)
69kV and below	3	5
through 161kV	1.5	2.5
above	1	1.5

### 3.1.5. Harmonic Mitigation

Harmonic problems can be solved by two different approaches. The first and the most favorable approach is to utilize appropriate circuit topologies such that harmonic pollution is not created. The second approach involves filtering. Harmonic filtering techniques are generally utilized to reduce the current THD and filters based on these techniques are classified in three main categories:

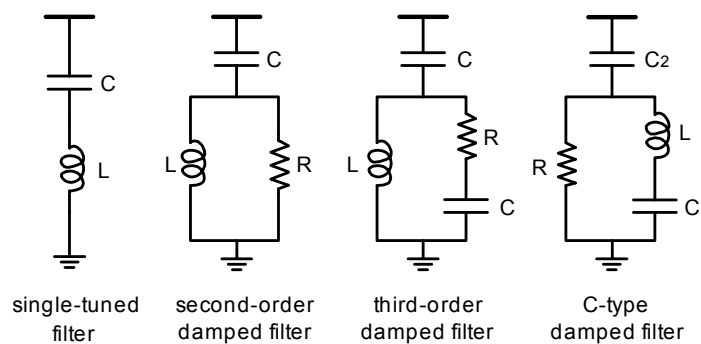
- Passive filters
- Active filters
- Hybrid filters

The traditional harmonic mitigation technique is the passive filtering technique. The basic principle of passive filtering is to prevent harmonic currents from flowing through the power system by either diverting them to a low impedance shunt filter path (parallel passive filter) or blocking them via a high series impedance (series passive filter) depending on the type of nonlinear load [21]. The C-type 2<sup>nd</sup> shunt power harmonic filter, which is the main discussion of this thesis, is also a passive filter.

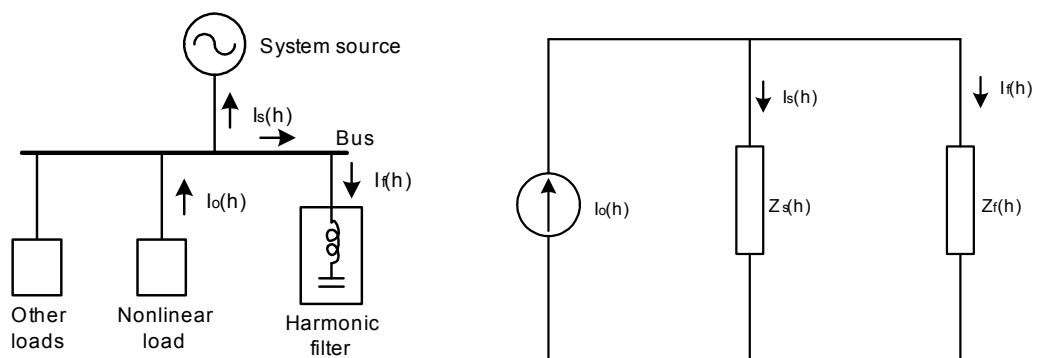
Series filters must carry full load current. In contrast, shunt filters carry only a fraction of the current that a series filter must carry. Given the higher cost of a series filter and the fact that shunt filters may supply reactive power at the fundamental frequency, the most practical approach usually is to use shunt filters [19].

The passive harmonics filters are composed of passive elements: resistor (R), inductor (L) and capacitor (C). The common types of passive harmonic filter include single-tuned and double-tuned filters, second-order, third-order, and C-type damped filters. The double-tuned filter is equivalent to two single-tuned filters connected in parallel with each other; so, only single-tuned filter and other three types of damped filters are presented here. The ideal circuits of the presented four types of filters are shown in Figure 3.2. Both third-order and C-type damped filters have two capacitors with one in series with resistor and inductor, respectively [22].

The connection of the HF to the network is made as given (load is not shown) in Figure 3.3.a. In Figure 3.3.b, the equivalent circuit for harmonic analysis is given.



**Figure 3.2** Passive Shunt Harmonic Filter Types



**Figure 3.3** (a) The connection of HF to the Network, (b) Equivalent Circuit for Harmonic Analysis

In Figure 3.3,

- $I_o(h)$  is the current source of  $h^{th}$  order harmonic produced by the nonlinear load,
- $I_s(h)$  is the  $h^{th}$  harmonic current to system source,
- $I_f(h)$  is the  $h^{th}$  harmonic current to harmonic filter,
- $V_s(h)$  is the  $h^{th}$  harmonic voltage at bus,
- $Z_s(h)$  is the equivalent  $h^{th}$  harmonic impedance of source system,
- $Z_f(h)$  is the equivalent  $h^{th}$  harmonic impedance of harmonic filter,
- $h$  is the harmonic number (multiple of harmonic frequency,  $f_h$  to fundamental frequency,  $f_b$ ) [22].

The damped filters' impedance approaches to the value of resistance at high frequency; so, they have a better performance of harmonic filtering at high frequency. As a result, the damped filters are suitable for reducing complex harmonics, i.e. many large harmonics distributed on wide frequency range.

The damped filters are usually used in cooperation with tuned filters for reducing investment and power loss, in which the tuned filters are used for filtering primary harmonics and the damped filters are used for filtering secondary harmonics [22].

The application of a filter bank results in a low impedance at the tuned frequency and a higher impedance at a lower parallel resonant frequency. The installation must be carefully engineered to place the parallel resonance at a point that does not result in harmonic overvoltages during energization of the furnace transformer or the steady-state operation of the furnace [10].

C-type damped filter are designed to yield series resonance at fundamental frequency for reducing the fundamental power loss. For those low harmonics to be reduced, C-type damped filters are suitable to use due to no fundamental power loss (in ideal case) and VAr derating.

### 3.1.6. Interharmonics and Flicker

Among the harmonics of the power frequency voltage and/or current, further frequencies can be observed which are not integer multiples of the fundamental. They can appear as discrete frequencies or a wideband spectrum [23]. Mathematically, it is customary to show this fact as follows:

Harmonic  $f = hf_1$  where  $h$  is an integer  $> 0$ ,

DC  $f = 0 \text{ Hz}$  ( $f = hf_1$  where  $h = 0$ ),

Interharmonic  $f \neq hf_1$  where  $h$  is an integer  $> 0$ ,

Sub-harmonic  $f > 0 \text{ Hz}$  and  $f < f_1$ ,

where  $f_1$  is the fundamental power system frequency.

Interharmonics can be observed in an increasing number of loads in addition to harmonics. These loads include static frequency converters, cycloconverters, subsynchronous converter cascades; adjustable speed drives for induction or synchronous motors, and all loads not pulsating synchronously with the fundamental power system frequency [24].

Another common source of interharmonic currents is an arcing load. This includes arc welders and arc furnaces. These types of loads are typically associated with low frequency voltage fluctuations and the resulting light flicker. These voltage fluctuations can be thought of as low frequency interharmonic components. In addition to these components, however, arcing loads also exhibit higher frequency interharmonic components across a wide frequency band.

It should be noted that most of these sources have interharmonic characteristics that vary in magnitude and frequency in time. This should be taken into account when characterizing sources [23].

The power industry is accustomed to dealing with harmonic distortion and special attention is often given to avoid resonances at a harmonic frequency, particularly an

odd harmonic. However, the power industry is unprepared for loads that can inject interharmonic frequency currents over a wide range of frequencies and it can excite whatever resonance exists. Power quality analyzers which are not designed to display interharmonics may give confusing readings. Significant utility and consulting manpower may be required to diagnose and solve the problem [25].

The relationship between flicker and interharmonics has been investigated previously and it has been shown that flicker and interharmonics are the causes of each other [1]. Light flicker occurs when the voltage amplitude fluctuates in time. Therefore, flicker can be modeled as an amplitude modulated (AM) signal whose carrier frequency is the 50 Hz supply frequency as given in IEC 61000-4-15.

$$y(t) = (A + M \cos(w_m t + \phi)) \sin(w_c t) \quad (3.1)$$

where  $M$  is the amplitude of flicker,  $w_m$  is the flicker frequency,  $w_c$  is the power system frequency and  $A$  is its amplitude.  $y(t)$  can also be expressed as:

$$y(t) = A \sin(w_c t) + \frac{M}{2} [\sin((w_c + w_m)t + \phi) + \sin((w_c - w_m)t + \phi)] \quad (3.2)$$

The fluctuation of the voltage amplitude given in (3.1) causes the interharmonic frequencies  $(w_c + w_m)$  and  $(w_c - w_m)$  to appear in the frequency spectrum of  $y(t)$  as shown in (3.2). In case of any harmonics existing in the power system, interharmonics also appear around the harmonics as shown in the example for a second harmonic in (3.3) and (3.4). For the sake of simplicity, it is assumed that the fundamental and the second harmonic are in-phase in (3.3) and (3.4).

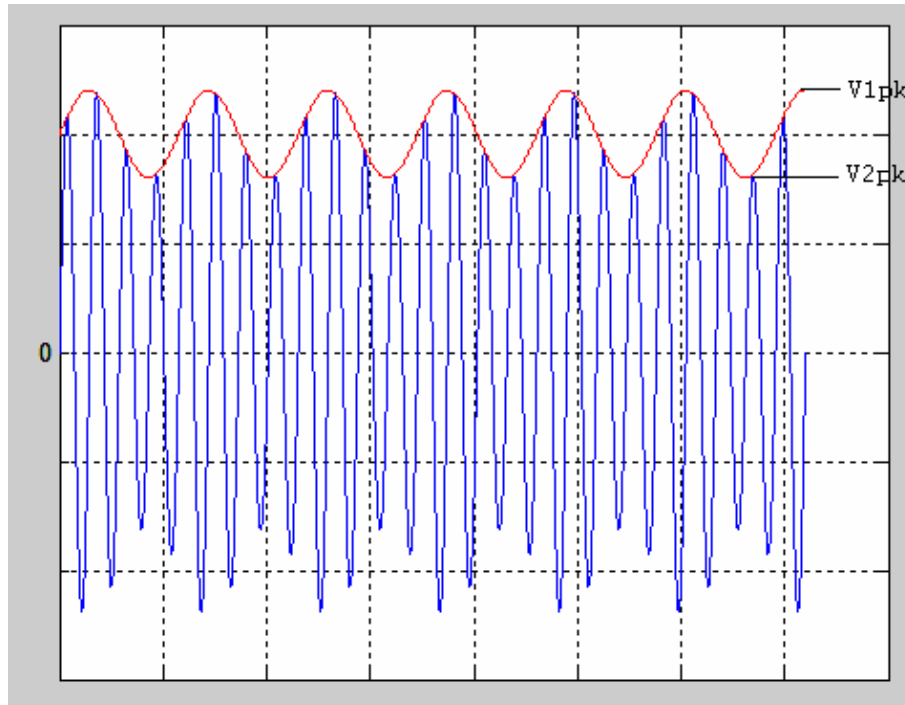
$$y(t) = (A + M \cos(w_m t + \phi)) [\sin(w_c t) + M_2 \sin(2w_c t)] \quad (3.3)$$

where  $AM_2$  product is the amplitude of the second harmonic component.  $y(t)$  can also be expressed as:

$$y(t) = A \sin(w_c t) + \frac{M}{2} [\sin((w_c + w_m)t + \phi) + \sin((w_c - w_m)t + \phi)] \\ + AM_2 \sin(2w_c t) + \frac{MM_2}{2} [\sin((2w_c + w_m)t + \phi) + \sin((2w_c - w_m)t + \phi)] \quad (3.4)$$

This shows any voltage fluctuation which can be approximated as an amplitude modulation, creates interharmonics around the fundamental and the harmonics, if they exist. The reverse is also true, i.e. if there are interharmonics close to the fundamental or the harmonics, they result in fluctuations in the signal amplitude. Interharmonics approximately 10 Hz apart from the fundamental and also from the harmonics give the highest contribution to the light flicker problem [1].

The flicker phenomena can be divided into two general categories: Cyclic flicker and non-cyclic flicker. Cyclic flicker results from periodic voltage fluctuations such as the ones caused by the operation of a reciprocating compressor. Non-cyclic flicker corresponds to occasional voltage fluctuations such as the ones caused by the starting of a large motor. The operation of a time-varying load, such as an electric arc furnace, may cause voltage flicker that can be categorized as a mixture of cyclic and non-cyclic flicker [10]. A simple calculation of flicker percentage is as follows:



**Figure 3.4** Example Voltage Waveform Causing Flicker

In Figure 3.4,

$$\Delta V = V_{1pk} - V_{2pk} \quad (3.5)$$

$$\text{Rms voltage of modulating wave} = \frac{\Delta V}{2\sqrt{2}} = \frac{V_{1pk} - V_{2pk}}{2\sqrt{2}} (A) \quad (3.6)$$

$$\text{Average rms voltage} = \frac{V_{1pk}/\sqrt{2}}{2} + \frac{V_{2pk}/\sqrt{2}}{2} = \frac{V_{1pk} + V_{2pk}}{2\sqrt{2}} (B) \quad (3.7)$$

$$\text{Percent (\%) voltage flicker} = \frac{(A)}{(B)} \times 100 = \frac{V_{1pk} - V_{2pk}}{V_{1pk} + V_{2pk}} \times 100 \quad (3.8)$$

It has been found in tests that the human eye is most sensitive to modulating frequencies in the range of 8-10 Hz, with voltage variations in the magnitude range of 0.3%-0.4% at these frequencies [10].

A variety of perceptible/limit curves are available in the published literature which can be used as general guidelines to verify whether the amount of flicker is a problem [10]. The IEC flicker meter is used to measure light flicker indirectly by simulating the response of an incandescent lamp and the human eye-brain response to visual stimuli [23].

Apart from the flicker issue,

- Interharmonics cause interharmonic voltage distortion according to the system impedance in the same manner as for harmonics and have similar impacts and concerns.
- Interharmonics can interfere with low frequency power line carrier control signals.
- Series tuned filters commonly applied on power systems to limit 5<sup>th</sup> through 13<sup>th</sup> harmonic voltage distortion cause parallel resonance (high impedance) at interharmonic frequencies (e.g. 210 Hz for a 5<sup>th</sup> harmonic filter). Filter designers expect this bandwidth to be clear of intentional signals. Interharmonic currents/voltages at these frequencies can be magnified. Filter failure and/or loss of equipment life can result [23].



### 3.1.7. Harmonic and Interharmonic Measurement Methods

In general, periodic signals can be analyzed with reference to a single time interval corresponding to one period. When interharmonic components are present, this period is different from the system fundamental period  $2\pi/\omega_1$ . From the “mathematical point of view”, the period of the signal containing interharmonics is equal to the ‘Fourier’s fundamental period’,  $2\pi/\omega_F$  where  $\omega_F$  is the greatest common divisor of all of the angular frequencies of all the signal components to be analyzed and combined [24].

From an “engineering point of view”, interharmonic component frequencies can be managed with the use of an “optimal” frequency resolution selected taking into account: the knowledge of the system under study, the computational burden needed for the analysis, the difficulties in storage, and presentation of the results and even adopting an opportune method to reduce the spectral leakage effects [24]. IEC 61000-4-7 [26] has established a well disciplined measurement method for harmonics. The reader is referred to the standard for details, but the key to the measurement of both harmonics and interharmonics in the standard is the utilization of a 10 (50 Hz systems) or 12 cycle (60 Hz systems) sample windows upon which to perform the Fourier transform. The result is a spectrum with 5 Hz resolution for both 50 Hz and 60 Hz systems. The standard further defines ways of combining individual 5 Hz bins to produce various groupings and components for which limits and guidelines can be referenced to [23]. According to this IEC Standard, the harmonic and interharmonic groups and subgroups are defined as follows:

#### i) Harmonic and interharmonic groups:

Harmonic group denoted by  $G_{g,n}$  is the square root of the sum of the squares of a harmonic and the spectral components adjacent to it within the time window, such that;

$$G_{g,n}^2 = \frac{C_{k-5}^2}{2} + \sum_{i=-4}^4 C_{k+i}^2 + \frac{C_{k+5}^2}{2} \quad (3.9)$$

for 50 Hz power systems, where  $C_k$  is the rms of amplitude of the  $(k)^{th}$  spectral component obtained from the Discrete Fourier Transform (DFT) for the  $(n = k/10)^{th}$  harmonic component. (Since the resolution is 5 Hz and the system frequency is 50 Hz, every 10<sup>th</sup> DFT sample corresponds to a harmonic, i.e. 10<sup>th</sup> is the fundamental, 20<sup>th</sup> is the 2<sup>nd</sup> harmonic and so on.)

Similarly, interharmonic group is defined as:

$$G_{ig,n}^2 = \sum_{i=1}^9 C_{k+i}^2 \quad (3.10)$$

for 50 Hz power system, where  $C_{k+i}$  is the  $(k+1)^{th}$  DFT sample, and they are the DFT samples between the  $(n)^{th}$  and the  $(n+1)^{th}$  harmonics (for example, 9 adjacent DFT samples between 55 Hz and 95 Hz for the interharmonics between 2<sup>nd</sup> and 3<sup>rd</sup> harmonics).

ii) Harmonic and interharmonic subgroups:

The harmonic grouping considers only the previous and the next DFT components around the harmonic component itself:

$$G_{sg,n}^2 = \sum_{i=-1}^1 C_{k+i}^2 \quad (3.11)$$

In the interharmonic subgroup case, the effects of fluctuations of harmonic amplitudes and phases are partially reduced by excluding the components immediately adjacent to the harmonic frequencies:

$$G_{isg,n}^2 = \sum_{i=2}^8 C_{k+i}^2 \quad (3.12)$$

iii) Single line harmonic frequency:

This is the single line measurement of the current or voltage frequency amplitude component obtained directly from the 5 Hz-resolution DFT samples according to IEC 61000-4-7.

The methods for measuring harmonics and interharmonics according to IEC 61000-4-7 can be summarized as given in Figure 3.5.

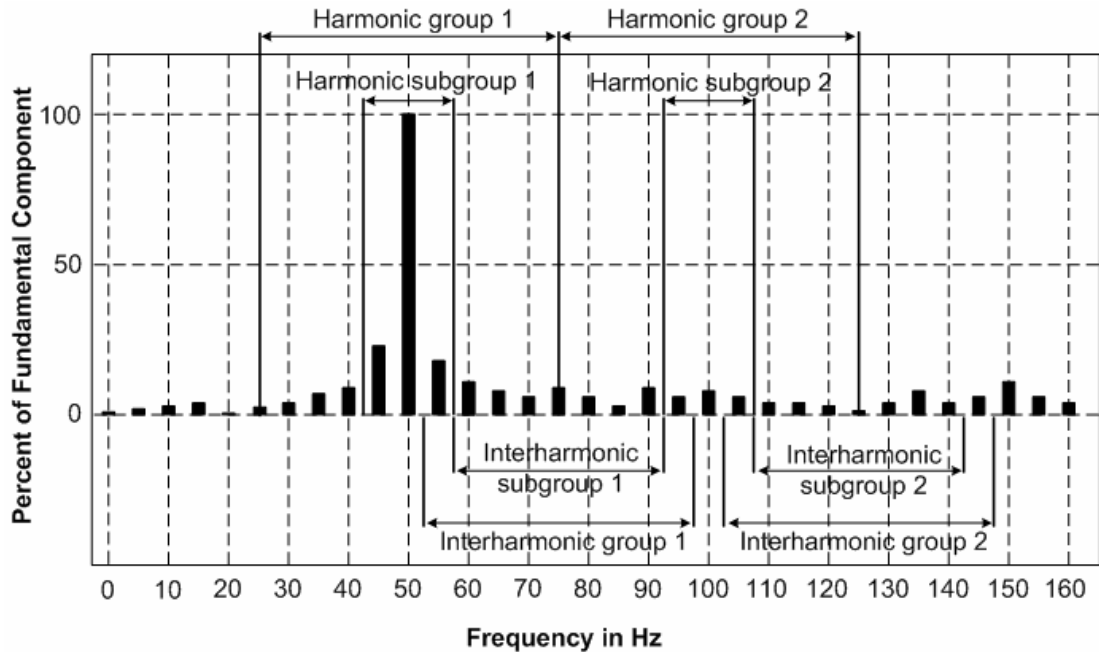
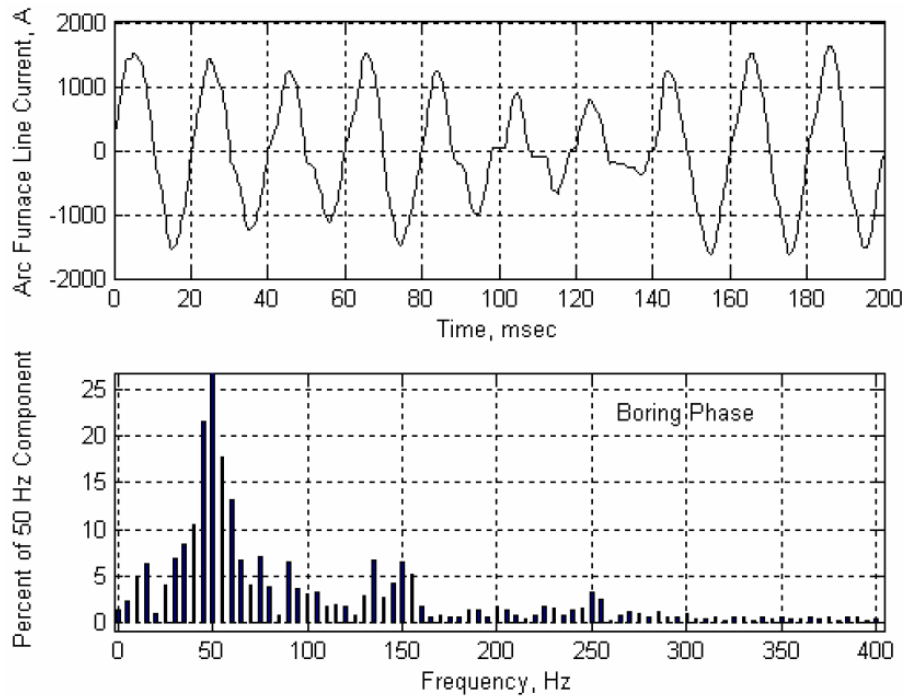


Figure 3.5 Measurement of Harmonics and Interharmonics as Given in IEC 61000-4-7

## 3.2. DESIGN OF THE HARMONIC FILTER

### 3.2.1. Optimized C-Type Harmonic Filter

The field data gathered from ERDEMİR LF transformer primary was given in Section 2.3. Before proceeding with the design of the C-type 2<sup>nd</sup> HF suitable for this LF, it will be more convenient to have a look at the performance of passive filters installed for EAFs and LFs in general. In Figure 3.6, the single phase current waveform of an EAF during the boring phase, together with its single line frequency harmonic components are given.

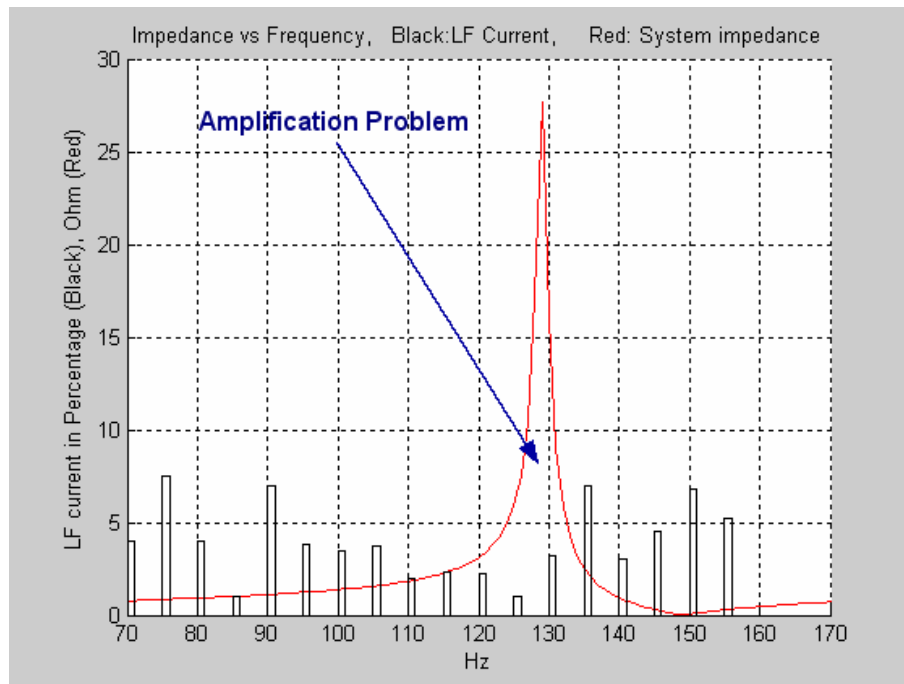


**Figure 3.6** Current Waveform and Harmonic Spectrum of an EAF during Boring Phase

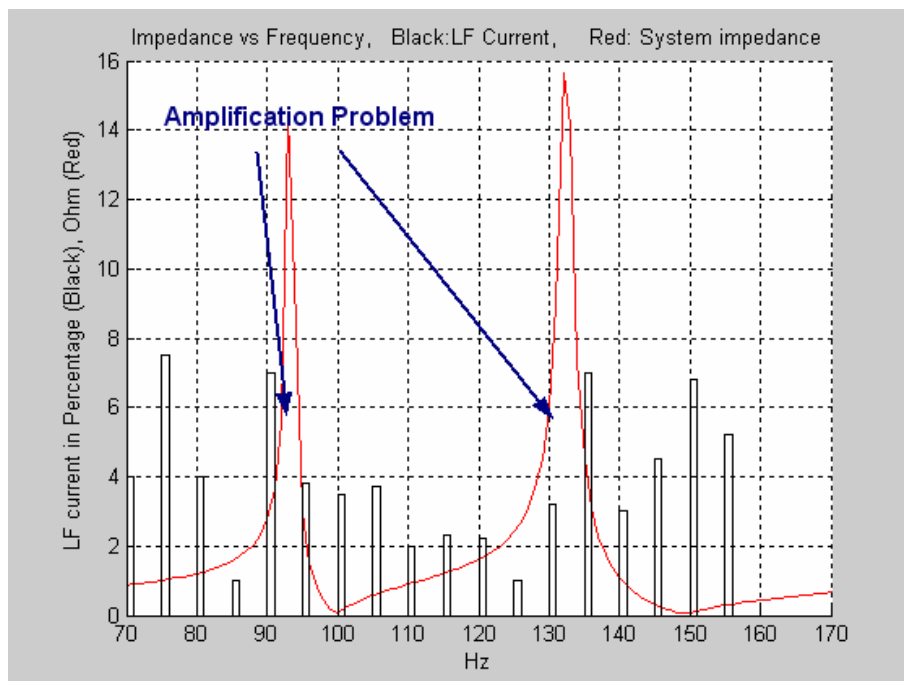
When the current harmonic spectrum given in Figure 3.6 is used together with a single-tuned 3<sup>rd</sup> HF, due to the single line frequencies existing almost everywhere, the result is an interharmonic amplification below 150 Hz as seen in Figure 3.7.

Similar to the case in Figure 3.7, when single-tuned 3<sup>rd</sup> HF is used together with a single-tuned 2<sup>nd</sup> HF, the result becomes worse as seen in Figure 3.8.

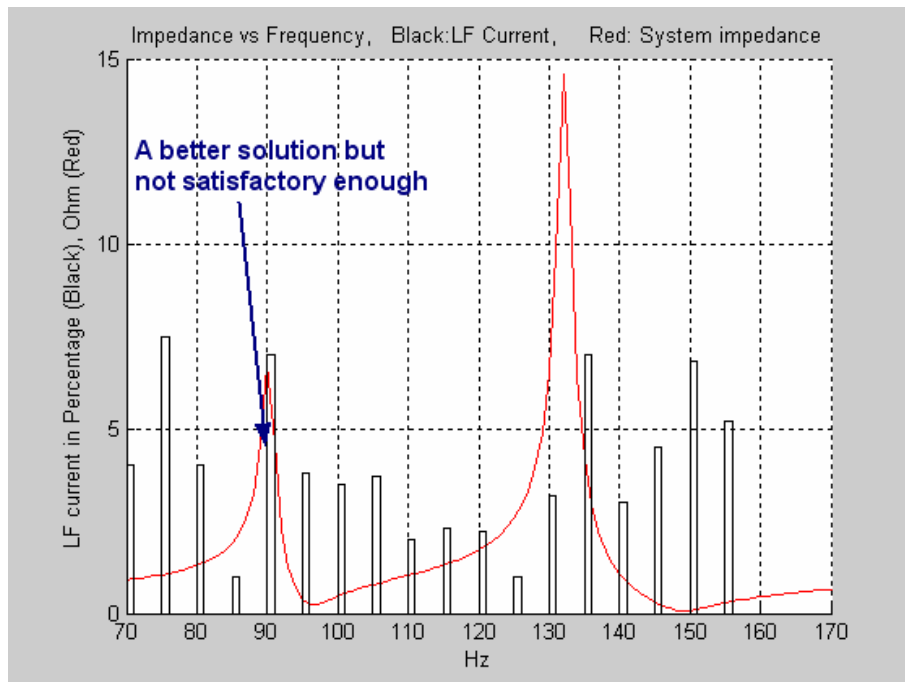
When the 2<sup>nd</sup> HF type is changed from single-tuned to C-type, it is seen in Figure 3.9 that the amplification factor becomes less compared to the case in Figure 3.8. The case for a highly damped C-type 2<sup>nd</sup> HF is given in Figure 3.10. The resistor values for the damping resistors were chosen to be 250 and 18  $\Omega$  for low damping and high damping cases, respectively. The reason for selecting these values will be clear in the proceeding sections of this chapter.



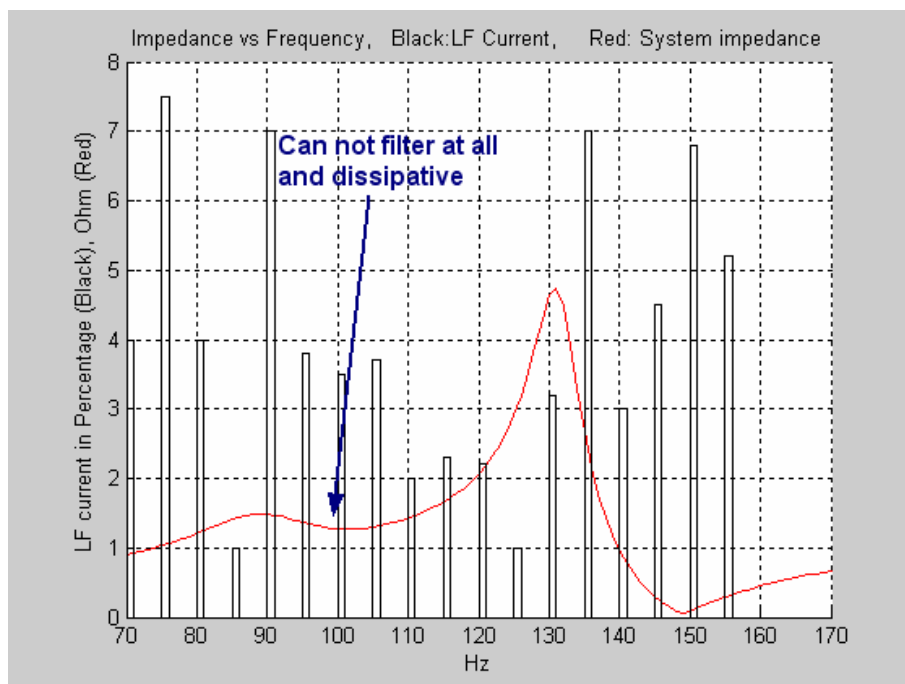
**Figure 3.7** Amplification Problem for a Single-Tuned 3<sup>rd</sup> HF Installed Alone



**Figure 3.8** Amplification Problem for a Single-Tuned 2<sup>nd</sup> HF and a Single-Tuned 3<sup>rd</sup> HF Installed Together



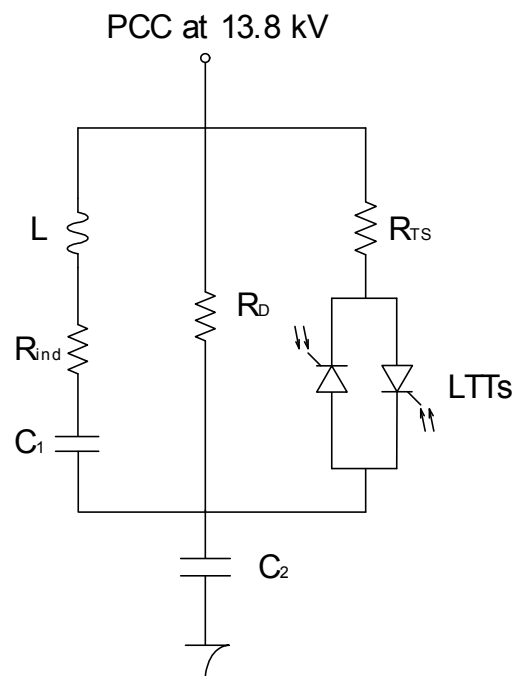
**Figure 3.9** Amplification Problem for a C-Type 2<sup>nd</sup> HF (Low-Damping) and a Single-Tuned 3<sup>rd</sup> HF Installed Together



**Figure 3.10** Amplification Problem for a C-Type 2<sup>nd</sup> HF (High-Damping) and a Single-Tuned 3<sup>rd</sup> HF Installed Together

Being one of the passive shunt filters, C-type filter has the advantage of having nearly no fundamental frequency loss because the resistor is in parallel with a serially connected branch whose impedance is tuned to zero at 50 Hz. In this study, addition of one more resistor in parallel is suggested and investigated in order to optimize the filter's transient state performance and maintain safe operation. This resistor is switched in and out by means of Light Triggered Thyristors (LTTs). The circuit schematic of the optimized C-Type HF is given in Figure 3.11.

This thesis is only involved in the optimization part of the filter, i.e. determination of the resistance values of permanently connected damping resistor ( $R_D$ ) and switched resistor ( $R_{TS}$ ), defining the solid-state switch parameters and implementing the switching control algorithm. The parameters of the inductor and capacitors had already been specified and they had been purchased before the author's studies started. The specifications of  $R_D$ ,  $R_{TS}$  and the solid-state switches had to be defined.



**Figure 3.11** The Circuit Schematic of the Optimized C-Type HF

As seen in Figure 3.11, the left hand side branch of the filter consists of an inductor ( $L$ ) and capacitor ( $C_1$ ) in series. ( $R_{ind}$  represents the internal resistance of the inductor). The values of  $L$ ,  $C_1$  and  $C_2$  had been selected in such a way that, the left hand side branch shows zero impedance at 50 Hz, and the filter is tuned to 100 Hz. The values are:

$$L = 14.25 \text{ mH}, \quad R_{ind} = 60 \text{ m}\Omega, \quad C_1 = 714 \text{ }\mu\text{F}, \text{ and } C_2 = 238 \text{ }\mu\text{F}.$$

The impedance of the left hand branch is:

$$\begin{aligned} Z_{left} &= j\omega L + \frac{1}{j\omega C_1} + R_{ind} \\ &= 0.06 + j0.0895f - \frac{j222.9}{f} \text{ }\Omega \end{aligned} \quad (3.13)$$

$$= 0.060 + j0.017 \text{ }\Omega \quad \text{at } f = 50 \text{ Hz} \quad (3.14)$$

Excluding  $R_{TS}$ , the total impedance of the filter is calculated as:

$$Z_{eq} = Z_{left} // R_D + \frac{1}{j\omega C_2} \quad (3.15)$$

$$= 0.060 - j13.36 \text{ }\Omega \text{ at } f = 50 \text{ Hz} \quad (3.16)$$

$$= 0.065 + j0.037 \text{ }\Omega \text{ at } f = 100 \text{ Hz} \quad (3.17)$$

The value of  $R_D$  does not affect the result of (3.16); however, (3.17) slightly differs by using different  $R_D$  values. Here, in (3.17),  $R_D = \infty$  is used. Different values of this resistor change the damping and quality factors of the HF and these cases will be examined in detail in Section 3.2.5.

Using (3.16), the reactive power compensation of the HF can be calculated for 50 Hz as follows:

$$S_{HF} = \frac{V_{bus}^2}{Z_{eq}^*} = \frac{13800^2}{0.06 + j13.36} = 0.06 - j14.25 \text{ MVA} \quad (3.18)$$

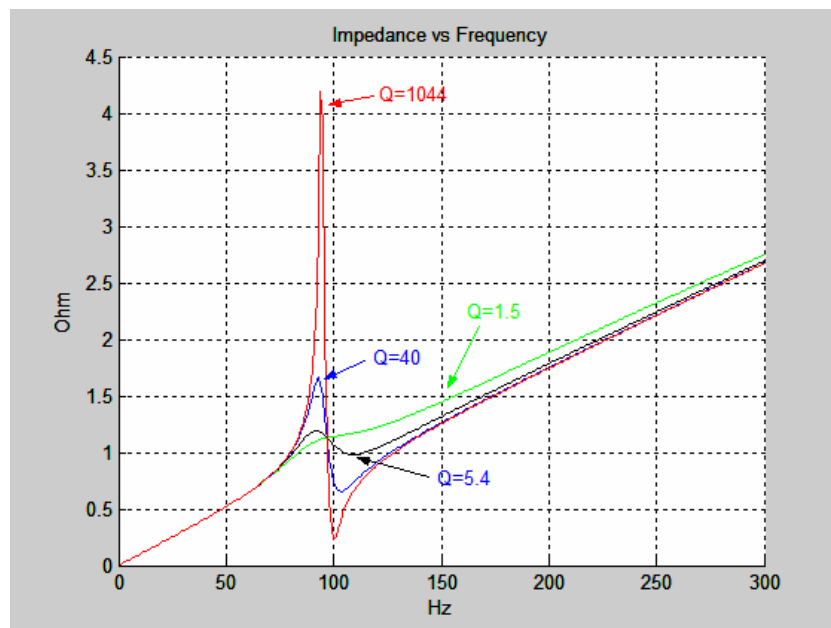


It is seen from (3.18) that  $Q_{HF} = -14.25$  MVAR.

One other important parameter for harmonic filters is the quality factor (Q). It represents the damping (or inversely filtering) performance of the filter. For a C-type

$$\text{filter } Q = \frac{R_D^2 C_2}{L} \quad [27].$$

Although it is mentioned in the literature that Q values between 0.5 – 2.0 are the commonly used ones, it is seen in Figure 3.12 that these values result in a very poor filtering performance. In Figure 3.12, the impedance versus frequency graphs for different Q values for the C-type filter are given.



**Figure 3.12** Impedance-Frequency Graph of C-Type Harmonic Filter and the Power System for Different Q Values

In Figure 3.12,  $Q = 1.5$  corresponds to  $R_D = 9.5\Omega$ ,

$Q = 5.4$  corresponds to  $R_D = 18\Omega$ ,

$Q = 40$  corresponds to  $R_D = 49\Omega$ , and

$Q = 1044$  corresponds to  $R_D = 250\Omega$ .

It is understood that  $Q$  values below 5.4 will result in no filtering at all.

### 3.2.2. Simulation Method

For the power system simulations and investigations of overvoltages resulting from the magnetizing inrush of the LF transformer of ERDEMİR, PSCAD/EMTDC v4.2 power systems simulation software is used throughout this study.

Since the furnace transformer of Figure 2.17 is energized approximately 60-70 times a day, a measure has to be taken against the overvoltages destroying any filter component. The worst case inrush current was given in Figure 2.8 and 2.9. According to the peak values and the decay time of this current, the LF transformer is modeled in PSCAD. Simulation work and the analysis are performed step by step as follows:

- i) Firstly, the LF transformer parameters in PSCAD are adjusted in such a way that the peak magnitude, harmonic content and the decay time of the inrush current are the same as those seen in the field data. When doing this, the instant when the LF transformer circuit breaker (CB) is closed and its poles' closing instants are adjusted in a way that the worst case inrush current is obtained.
- ii) Secondly, the overvoltages on the filter elements, namely the capacitors, are observed when there is no damping resistor ( $R_D$ ) or switched resistor ( $R_{TS}$ ) connected. (In this case, the C-type HF acts simply as a single-tuned filter.)
- iii) Thirdly, performances with different  $R_D$  and  $R_{TS}$  values are tested for both transformer inrush and filter energization conditions. The overvoltages on the capacitors and the filtering performances are investigated.

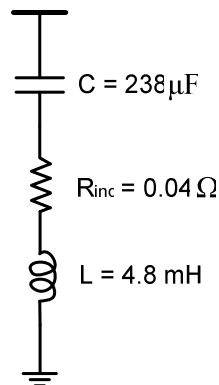
iv) For investigating the steady-state performance of the filter, the field data is directly transferred to PSCAD, and the harmonic group, subgroup and single line frequency analyses are made for different values of  $R_D$ .

v) Finally, the optimum values for  $R_{TS}$  and  $R_D$  are determined considering both the filtering (including interharmonics) performance during steady-state and power losses during the transformer inrushes.

Another event that causes the overvoltages on the harmonic filter capacitors is the closure of the filter circuit breaker. Although this case happens very rarely and it is not as common as the transformer inrush; it is also investigated and shown in this work.

This work is based on the first phase of ERDEMİR-SVC project. However, since the optimized C-type HF will also be in operation after the second phase of the project is finished, the simulations are made considering the second phase also. In other words, the effect of single-tuned 3<sup>rd</sup> HF on the performance of optimized C-type 2<sup>nd</sup> HF is also investigated and the study results are included.

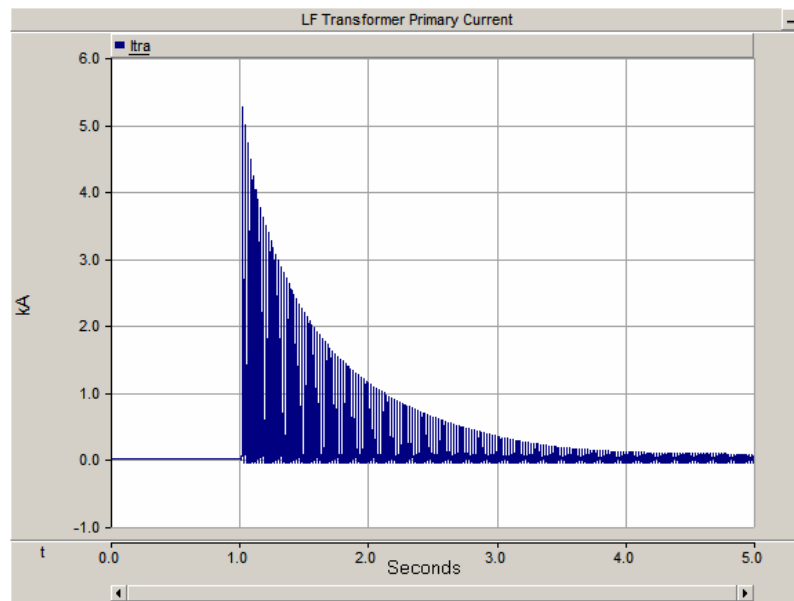
The one-line circuit diagram for the single-tuned 3<sup>rd</sup> HF of the second phase of the project is given in Figure 3.13.



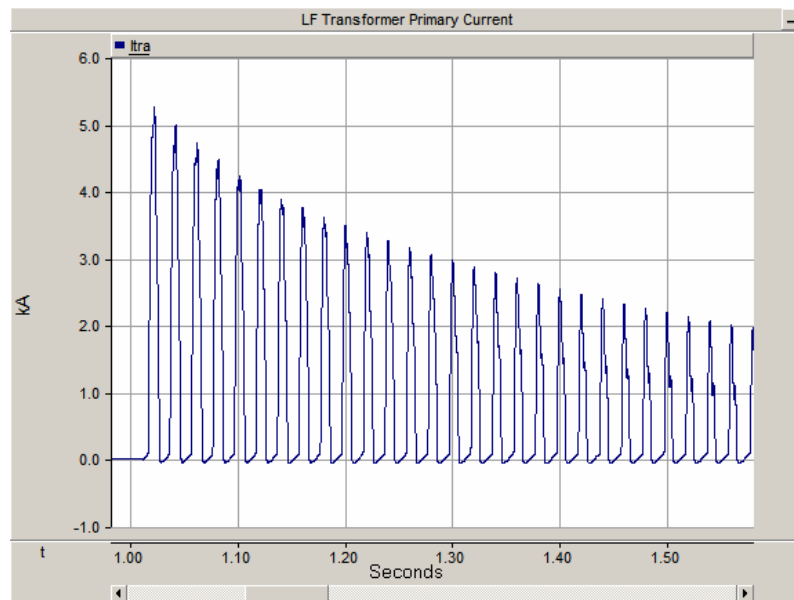
**Figure 3.13** 3<sup>rd</sup> HF of ERDEMİR-SVC Project's 2<sup>nd</sup> Phase

### 3.2.3. Transient and Steady-State Simulation Results with $R_D = \infty$

The worst case inrush current simulated in PSCAD is given in Figures 3.14.a and 3.14.b. It is concluded from Figure 3.14 that the peak magnitude and the decay duration of the current are in coincidence with the field data given in Figures 2.8 and 2.9.



(a)

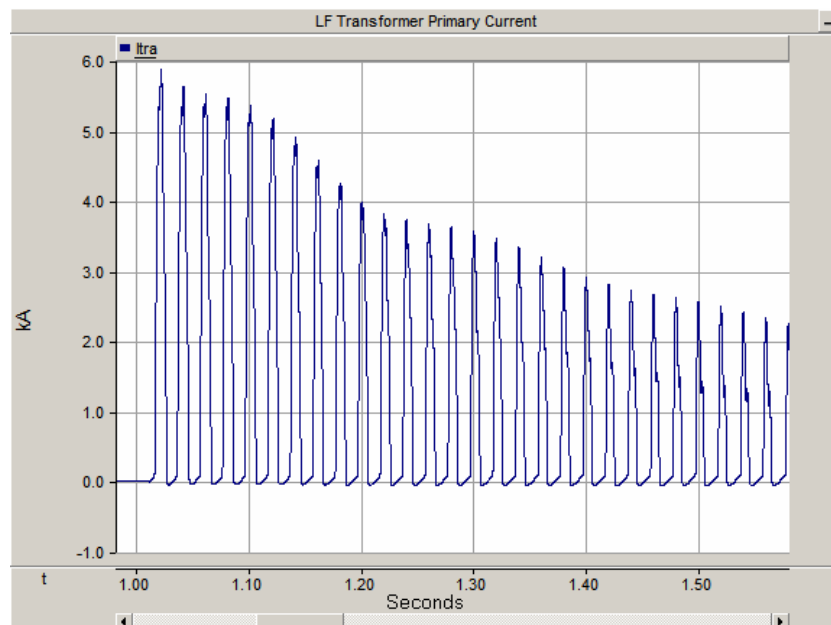


(b)

**Figure 3.14** LF Transformer Primary Current during Transformer Inrush Simulated in PSCAD

If the 2<sup>nd</sup> HF is added to the system, the peak magnitude of the inrush current is seen to be a bit larger as given in Figure 3.15. Under normal conditions, this inrush current does not cause problems. However, overvoltages may occur if the system is sharply tuned at one of the predominant harmonics produced by the inrush. The case is similar for the C-type 2<sup>nd</sup> harmonic filter here. The filter is tuned to 2<sup>nd</sup> harmonic component and it is designed to sink approximately 100 A at maximum. Since a peak 2<sup>nd</sup> harmonic current component with a peak of 1 kA at maximum is created by the furnace transformer during inrush, when this amount of current (in fact, a percentage of it) goes into the filter; the filter components, namely the capacitors, face overvoltage problems. The frequent switching of furnace transformers may result in thousands of overvoltage events in a year, leading to degradation of insulation systems [12].

The overvoltages seen on the capacitors are the same no matter the 3<sup>rd</sup> HF is included in the network or not. However, the transformer inrush also affects the 3<sup>rd</sup> HF components and overvoltages have also been observed on the 3<sup>rd</sup> HF capacitors also.



**Figure 3.15** Simulated LF Transformer Primary Current during Transformer Inrush with 2<sup>nd</sup> HF Included to the System

This should, in fact, be solved by a method which is similar to the one asserted in this study. However, this is out of the scope of this thesis; hence, the results will not be discussed here.

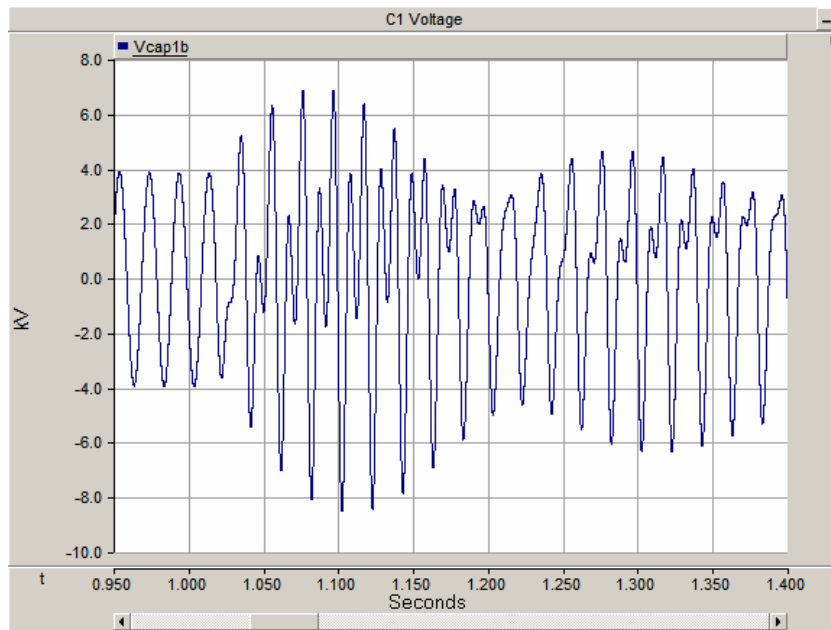
The voltages on  $C_1$  and  $C_2$  (for  $R_D = \infty$ ) during the worst transformer inrush are given in Figures 3.16 and 3.17, respectively. According to Figures 3.16 and 3.17, the peak voltages on the capacitors for the worst transformer inrush are as follows:

$$V_{C1_{peak}} = 8.50 \text{ kV}, \quad V_{C2_{peak}} = 25.55 \text{ kV}$$

However, the rms ratings of these capacitors are as follows:

$$V_{C1_{rms}} = 4.5 \text{ kV}, \quad V_{C2_{rms}} = 12.0 \text{ kV}$$

The simulated overvoltages seen on capacitors  $C_1$  and  $C_2$  during filter energization are given in Figures 3.18 and 3.19, respectively. It can be concluded that especially for the second capacitor ( $C_2$ ), a measure has to be taken against the overvoltages to prevent any flashover and/or life degradation of the capacitors.



**Figure 3.16** Voltage on  $C_1$  during Worst Transformer Inrush with  $R_D = \infty$

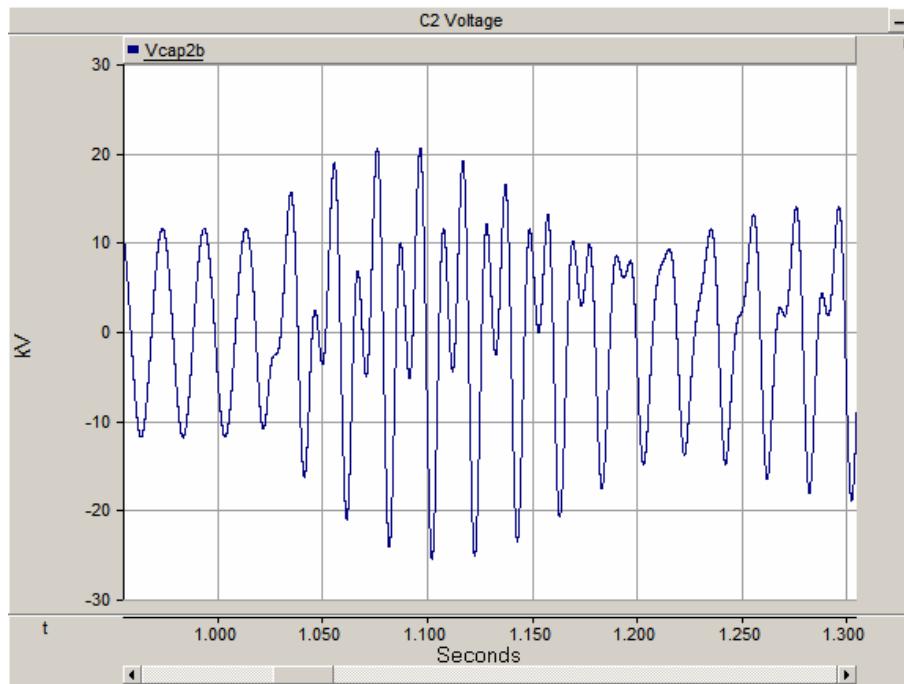


Figure 3.17 Voltage on  $C_2$  during Worst Transformer Inrush with  $R_D = \infty$

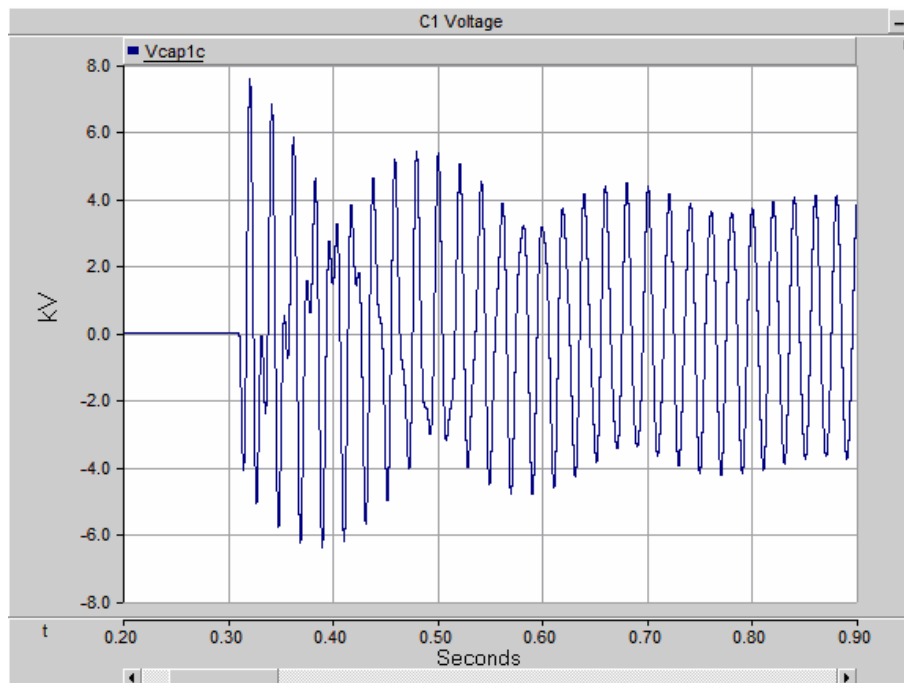
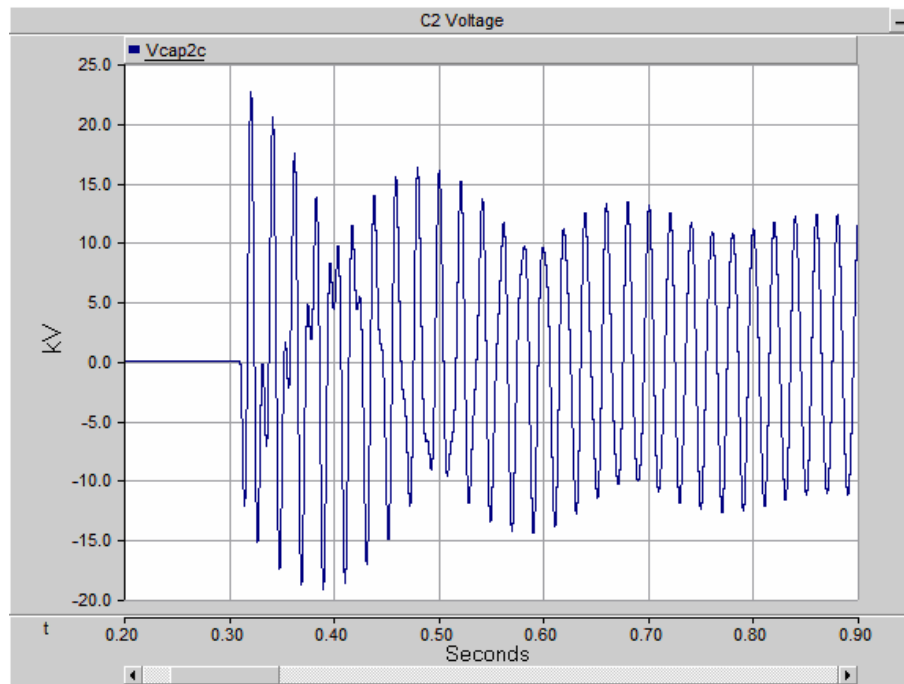


Figure 3.18 Voltage on  $C_1$  during Worst Filter Energization with  $R_D = \infty$



**Figure 3.19** Voltage on  $C_2$  during Worst Filter Energization with  $R_D = \infty$

An optimization would be made between the filtering performance and the transient performance only if the damping resistor ( $R_D$ ) existed.

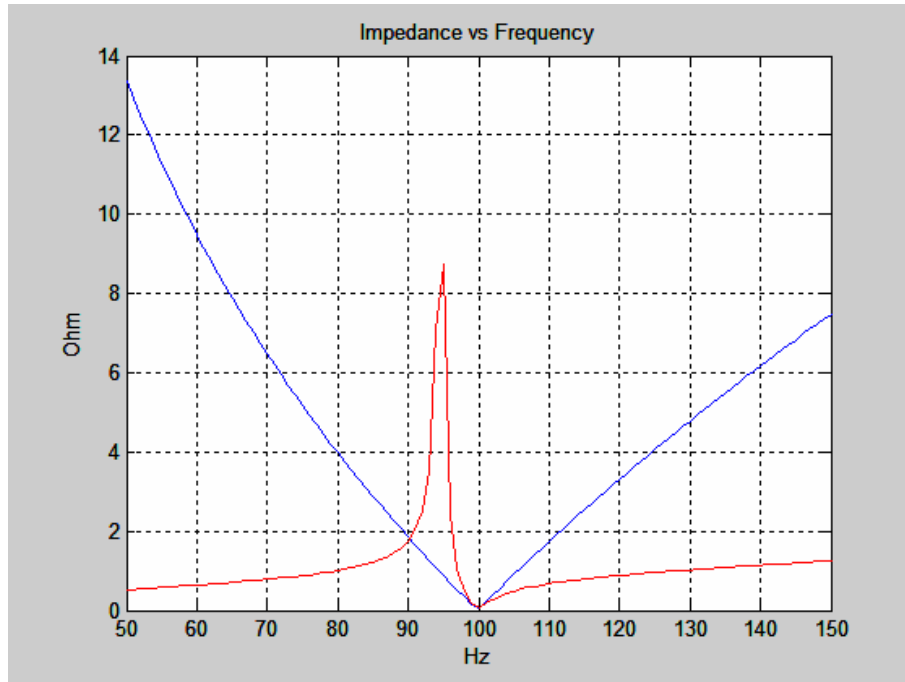
By using the switched resistor ( $R_{TS}$ ) in taking it into conduction during the transformer inrushes only, both the transient and the filtering performance of the filter can be made satisfactory. According to Figures 3.18 and 3.19, the peak voltages on the capacitors for the worst filter energization are as follows:

$$V_{C1_{peak}} = 7.55 \text{ kV}$$

$$V_{C2_{peak}} = 22.65 \text{ kV}$$

Although the transient performance of the filter is the worst, the filtering performance of it will be the best for  $R_D = \infty$ . The impedance-frequency graphs of filter alone (blue), and filter and the system together (red) for  $R_D = \infty$  are shown in Figure 3.20.





**Figure 3.20** Impedance-Frequency Graph of Filter Alone (Blue) and Filter and the Power System (Red) for  $R_D = \infty$

The steady-state performance of the filter is also investigated for  $R_D = \infty$  also. The measured data is directly transferred to PSCAD simulation. FFT blocks with 5 Hz bandwidth are used and the different computation methods given in Section 3.1.7 are applied. The results are given in Table 3.3. In Table 3.3, the effect of adding the 3<sup>rd</sup> HF is also shown. The bus current values ( $I_s(h)$ ) given in Table 3.3 are not the steady state values for the normal LF operation. They are the maximum values and not values of the same time instant necessarily.

It is seen in Table 3.3 that, for 2<sup>nd</sup> HF installed only, although the 100 Hz component (single-line frequency) is filtered from 42 A to 26 A, since 95 Hz component is amplified to 110 A from 38 A, harmonic group value is seen to be worse with the 2<sup>nd</sup> filter. This case is common for nearly all iron and steel plants due to the interharmonic creating nature of the furnaces and HFs designed by considering only harmonics, not interharmonics. It is seen that all of the  $G_{g,n}$  values have gone worse.

$R_D$  value should be taken to decrease these values (especially the harmonic subgroup) while also sustaining the power loss on  $R_D$  at a tolerable level.

**Table 3.3** Harmonic and Interharmonic Currents on the Bus for  $R_D = \infty$

LF Transformer Primary Harmonic Currents without the 2nd and 3rd HF				LF Transformer Primary Harmonic Currents with the 2nd HF connected ( $R_D = \infty$ )				LF Transformer Primary Harmonic Currents with the 2nd HF ( $R_D = \infty$ ) and 3rd HF connected			
Single Line Frequency	Amps	Gg,n	Amps	Single Line Frequency	Amps	Gg,n	Amps	Single Line Frequency	Amps	Gg,n	Amps
I (55 Hz)	125	<b>Gg,2 (Harmonic Group)</b>	106	I (55 Hz)	132	<b>Gg,2 (Harmonic Group)</b>	160	I (55 Hz)	138	<b>Gg,2 (Harmonic Group)</b>	191
I (60 Hz)	71			I (60 Hz)	74			I (60 Hz)	77		
I (65 Hz)	42			I (65 Hz)	43			I (65 Hz)	46		
I (70 Hz)	34			I (70 Hz)	36			I (70 Hz)	37		
I (75 Hz)	33			I (75 Hz)	34			I (75 Hz)	36		
I (80 Hz)	38	<b>Gsg,2 (Harmonic Subgroup)</b>	65	I (80 Hz)	44	<b>Gsg,2 (Harmonic Subgroup)</b>	116	I (80 Hz)	53	<b>Gsg,2 (Harmonic Subgroup)</b>	120
I (85 Hz)	39			I (85 Hz)	51			I (85 Hz)	61		
I (90 Hz)	41			I (90 Hz)	75			I (90 Hz)	112		
I (95 Hz)	38			I (95 Hz)	110			I (95 Hz)	111		
I (100 Hz)	42			I (100 Hz)	26			I (100 Hz)	35		
I (105 Hz)	32	<b>Gig,1 (Inter-harmonic Group)</b>	175	I (105 Hz)	25	<b>Gig,2 (Inter-harmonic Group)</b>	222	I (105 Hz)	27	<b>Gig,2 (Inter-harmonic Group)</b>	247
I (110 Hz)	25			I (110 Hz)	21			I (110 Hz)	28		
I (115 Hz)	24			I (115 Hz)	21			I (115 Hz)	24		
I (120 Hz)	22			I (120 Hz)	19			I (120 Hz)	29		
I (125 Hz)	21			I (125 Hz)	20			I (125 Hz)	34		
I (130 Hz)	20	<b>Gisg,1 (Inter-harmonic Subgroup)</b>	117	I (130 Hz)	21	<b>Gisg,2 (Inter-harmonic Subgroup)</b>	141	I (130 Hz)	35	<b>Gisg,2 (Inter-harmonic Subgroup)</b>	173
I (135 Hz)	21			I (135 Hz)	20			I (135 Hz)	32		
I (140 Hz)	26			I (140 Hz)	27			I (140 Hz)	29		
I (145 Hz)	34			I (145 Hz)	33			I (145 Hz)	27		

### 3.2.4. Capacitor Overvoltages in the Literature

In several cases, capacitors and reactors used in filter arrangements have subsequently experienced insulation failures during switching operations. For instance, investigation of a capacitor failure has revealed that the capacitors'

dielectric system was unfailed. The insulation failure was external with arcing damage to the capacitor cases. Reactors on the same banks also failed. Transient simulations have determined that complex switching transients occurred on all switching operations. Similar failures have occurred in filter systems designed by more than one designer [28].

Energizing a capacitor and inductor combined as a single tuned filter will also result in a voltage twice the voltage which normally appears across the capacitor.

Some of the types of switching events which cause transient and dynamic overvoltages and overcurrents in industrial filters are i) normal energizing of the banks, ii) energizing of transformers connected to the bus, iii) fault initiation and fault clearing on the bus, and iv) filter breaker restriking during breaker opening.

In evaluating the effect on the ratings of the equipment, it is important to account for the relative frequency of such occurring events. Filter bank and transformer energization may occur many times a day. Breaker restriking may not occur more than several times in the filter lifetime. What the tables in the standards do not show clearly is the duration of the transients.

When a transformer is energized, inrush current can be high in magnitude and harmonic content and of long duration (lasting several seconds). The harmonic content can excite resonances in the filter which extends the duration of the inrush and resonance. Although the peaks of this case are not as high as the other switching transients, the extended duration can result in severe stress on component insulation. Transformer energization can be a regular occurrence on an industrial bus.

The capacitor bank rating should be selected so that when the stresses of the components are per unitized on the rated voltage of the capacitor bank, the resulting per unit values are less than the maximum permissible voltage derived from the IEEE Standard. As long as this rule is followed, the capacitor bank internal and external

insulation will be properly coordinated with the stresses applied from the power system [28]. The allowable overload limits of capacitors based on standards are:

kVAr	135%
rms voltage	110%
sum of peak voltages	120%
rms current	180%

All of these parameters should be checked when applying capacitors to a harmonic environment, especially if the capacitors are parts of a filter [19].

On the other hand, there are no standards that directly apply to the application of shunt power capacitors in industrial environments containing extreme distortion due to the repetitive events such as furnace transformer energizations, producing high transients and harmonics. Two sections from the IEEE Std 18-1992 (IEEE Standard for Shunt Power Capacitors) [29] and CAN3-C155-M84 (Canadian Standards for Shunt Capacitors for AC Power Systems) [30], if applied in a general sense, can be used to obtain approximate transient and overvoltage limits for the operation of capacitors in severely distorted industrial environments [12].

The momentary power frequency overvoltage section found in both the IEEE and the Canadian standards for shunt power capacitors, IEEE Std 18-1992 and CAN3-C155-M84, respectively, states that “A capacitor may reasonably be expected to withstand, during normal service life, a combined total of 300 applications of power frequency terminal-to-terminal overvoltages without superimposed transients or harmonic content, of the magnitudes and durations listed in Table 3.4 and Table 3.5.” Since the standard does not consider harmonic content, it is difficult to determine how it applies to capacitors that are subject to transformer energizations. However, it should be noted that the 300 applications of power frequency terminal-to-terminal overvoltages could be exceeded in a time period of only one week due to a great number of furnace transformer energizations present at a steel manufacturing facility [12].

For a single-tuned filter case investigation given in [28], the transient capacitor overvoltages during different events are given in Table 3.6. This particular example shows the need for the second harmonic filter capacitors being rated higher than that required for steady-state harmonics. This is due to the dynamic overvoltage condition that occurs during transformer energization.

**Table 3.4** Maximum Permissible Power Frequency Capacitor Overvoltages

<b>Momentary Power Frequency Overvoltage</b>		
Duration	Maximum Permissible Voltage	
	RMS (p.u.)	Peak (p.u.) = $\sqrt{2}$ RMS (p.u.)
0.5 cycle	3.00	4.24
1.0 cycle	2.70	3.82
6.0 cycles	2.20	3.11
15.0 cycles	2.00	2.83
1.0 second	1.70	2.40
15.0 seconds	1.40	1.98
1.0 minute	1.30	1.84
30.0 minutes	1.25	1.77

**Table 3.5** Maximum Permissible Transient Capacitor Overvoltages

<b>Maximum Permissible Transient Overvoltage</b>	
Number of transients (half cycle) per year	Multiplication factor for maximum permissible peak voltage
4	5.0
40	4.0
400	3.4
4000	2.9

Using IEEE Std 18-1992 and CAN3-C155-M84, capacitor bank rating constraints may be summarized as given in Table 3.7.

**Table 3.6** Capacitor Overvoltages during Different Events for a Single-Tuned Filter Case Investigation

Case Description	13.8 kV bus peak voltage (kV)	Single-tuned filter capacitor peak voltage (kV)
energization of filter	18.6	45.6
initiation of 3 phase fault on bus	14.7	20.8
clearance of 3 phase fault on bus	16.0	34.1
restricking of filter breaker	22.5	64.0
energization of furnace transformer	12.7	42.5

**Table 3.7** Capacitor Bank Rating Constraints

System status	Capacitor bank voltage rating (VR-rms)
Steady state operation	$VR \geq \text{sum of fundamental and harmonic voltages}$
Inrush/Dynamic overvoltage (VD)	$VR \geq (VD/\sqrt{2})/1.4$
Energizing transient (VTE)	$VR \geq (VTE/\sqrt{2})/2.5$
Restrike condition (VTR)	$VR \geq (VTE/\sqrt{2})/2.5$

Possible solutions for preventing the overvoltages from damaging the capacitors may be listed as follows:

i) A control scheme can be installed to prevent furnace transformer energizations with the capacitor bank on-line. This would minimize the effects on the capacitors. In this scheme, the capacitor bank will have to be energized each time after the furnace transformer is energized. This will lead to an increased number of energizations and deenergizations of the capacitor bank and in fact, this also causes transient overvoltages. Moreover, the filter circuit breaker's life is reduced severely in this method.

ii) Pre-insertion devices such as resistors or reactors can be used with the transformer vacuum switch. This will dampen the high transients from the transformer energizations. This may lead to modification or replacement of the existing switch and it will not be feasible or economical for the case in ERDEMİR.

iii) Overtopping of the filter elements in order to remain in the safe operating region even during transformer inrushes. This means increasing the current rating and the rms voltage rating of the capacitors  $C_1$  and  $C_2$ ; however, this will not be economical.

iv) A novel solution method, which is examined in this work, is to use the harmonic filter in two operation modes. In one of these modes, the filter sinks the harmonic current component satisfactorily; in the other mode, which is used in transformer inrush, the filter characteristics are intentionally changed and it does not sink harmonic current any more. This is done by switching in  $R_{TS}$  by means of LTTs.

### 3.2.5. Transient Simulation Results with Different Values of $R_D$

Different values of the permanently connected damping resistor result in different filtering and transient performances of the optimized C-type 2<sup>nd</sup> HF. If the value of  $R_D$  is reduced, the filtering performance becomes worse, but the overvoltages on the capacitors during the transformer inrushes decrease.

The overvoltages on the capacitors, power loss and the filtering ratio of the HF for different  $R_D$  values are given in Table 3.8. In Table 3.8, the second column, which is the continuous power loss on  $R_D$  during normal LF operation, is calculated by using the following current values for the ladle furnace transformer primary:

Fundamental = 1.5 kA rms, 2<sup>nd</sup> harmonic = 225 A rms  
3<sup>rd</sup> harmonic = 300 A rms, 4<sup>th</sup> harmonic = 100 A rms  
5<sup>th</sup> harmonic = 150 A rms, 7<sup>th</sup> harmonic = 100 A rms

These values are used considering the worst case for LF and TCR harmonics and the amplification of 2<sup>nd</sup> harmonic due to the 3<sup>rd</sup> HF.

Third column of Table 3.8 is the instantaneous maximum power loss on  $R_D$  during transformer inrush. The fourth column of Table 3.8 is the instantaneous power loss on  $R_D$  after one second has passed over the initiation of transformer inrush.

**Table 3.8** Overvoltages on the Capacitors, Power Loss and the Filtering Ratio of the HF for Different  $R_D$  Values

Rd(ohm)	CONTINUOUS POWER LOSS DURING NORMAL LF OPERATION (kW)	INSTANTANEOUS PEAK POWER LOSS DURING TRANSFORMER INRUSH (kW)	INSTANTANEOUS POWER LOSS ONE SECOND AFTER TRANSFORMER ENERGIZATION (kW)	Vc1 peak (kV)	Vc2 peak (kV)	2nd Harmonic Filtering Ratio (%)
10	72.26	286	27.1	4.13	12.57	-13.58
14	61.00	340	25.3	4.18	12.99	-10.24
18	54.60	386	24.6	4.35	13.36	-6.29
20	52.31	405	24.4	4.43	13.55	-4.17
25	48.00	441	23.9	4.60	14.95	1.34
30	44.77	467	23.6	4.76	14.40	6.89
35	42.08	488	22.9	4.88	14.45	12.25
40	39.71	501	22.2	5.07	14.86	17.30
45	37.57	510	21.3	5.25	15.43	21.98
50	35.61	511	20.6	5.41	15.94	26.27
55	33.80	510	19.7	5.55	16.39	30.19
60	32.14	507	18.9	5.68	16.80	33.75
65	30.61	501	18.1	5.79	17.18	36.99
70	29.20	495	17.4	5.91	17.53	39.94
75	27.89	488	16.7	6.01	17.86	42.63
80	26.68	482	16.0	6.11	18.16	45.08
90	24.52	469	14.7	6.28	18.70	49.38
100	22.65	455	13.7	6.43	19.17	53.00
110	21.03	441	12.7	6.56	19.57	56.09
120	19.61	426	11.9	6.67	19.92	58.75
130	18.36	412	11.1	6.78	20.24	61.05
140	17.25	398	10.5	6.87	20.52	63.07
150	16.27	383	9.8	6.95	20.77	64.84
160	15.39	370	9.3	7.02	20.99	66.42
170	14.59	360	8.8	7.09	21.20	67.82
180	13.87	350	8.4	7.15	21.39	69.08
190	13.22	339	8.0	7.21	21.56	70.22
200	12.62	329	7.6	7.26	21.71	71.25
210	12.08	319	7.3	7.30	21.86	72.19
220	11.58	310	7.0	7.35	21.99	73.05
230	11.11	302	6.7	7.39	22.11	73.84
240	10.68	294	6.5	7.42	22.23	74.56
250	10.29	285	6.2	7.46	22.33	75.23
infinite	0	0	0	8.50	25.55	91.49



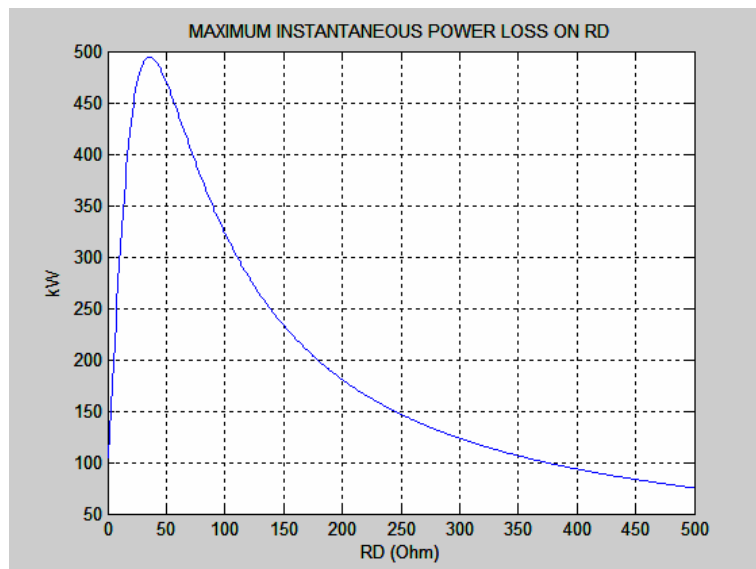
It is seen in Table 3.8 that in order to decrease the overvoltages on the capacitors, the value of  $R_D$  should be decreased. On the other hand, decreasing the value of  $R_D$  decreases the filtering ratio. Furthermore, it increases the power loss on it during normal operation of the LF.

One interesting point is that the power loss on  $R_D$  during transformer inrush is not inversely proportional to the power loss of it. There seems to be a value of  $R_D$  between 35 – 60  $\Omega$  that maximizes the power loss of it. This case is also investigated in MATLAB v6.5 by modeling the network and the peak transformer inrush current harmonic components. The code written in MATLAB is given in Appendix-A.

Figure 3.21 shows that the maximum power loss on  $R_D$  is seen for  $R_D \approx 40 \Omega$ . This calculation is made for a transformer inrush of harmonic components:

$$I_1 = 2000 \text{ A}, \quad I_2 = 950 \text{ A}, \quad I_3 = 300 \text{ A}, \quad I_4 = 100 \text{ A}, \quad I_5 = 80 \text{ A}.$$

(All values in rms)



**Figure 3.21** Maximum Instantaneous Power Losses of Different  $R_D$ s during Worst Transformer Inrush

In fact, most of the power loss is due to the 2<sup>nd</sup> harmonic as expected, since the filter is tuned to 100 Hz. In Table 3.8, the  $R_D$  value that causes the maximum power dissipation, and the according power loss value are a bit different from the ones concluded from Figure 3.21. This is because, in Figure 3.21, only the harmonic components are modeled, the interharmonic components are not included. In other words, 950 A rms 2<sup>nd</sup> harmonic current in MATLAB model represents a point-wise value, not a group with 5 Hz bandwidth. This results in the discrepancy between Table 3.8 and Figure 3.21. However, both results give the idea that choosing a resistor value around 40 – 50  $\Omega$  will be too lossy although it can not decrease the transient overvoltages very much.

### 3.2.6. Steady State Simulation Results with Different Values of $R_D$

The overvoltages seen on the capacitors for different values of  $R_D$  are given in Table 3.8. The last column of this table also represents the 2<sup>nd</sup> harmonic filtering ratio performance. However, the values represent only the 100 Hz component values with no dimension (they do not include a bandwidth of 5 Hz). Thus, it is not very informative. In order to investigate the filtering performance, the field data is used and the methods discussed in section 3.1.7 are applied.

The current harmonics and interharmonics have been measured by using 5 Hz sampled DFT with and without the filter for the system. While doing this, the instantaneous maximum values of the harmonics have been taken for simplicity. The average values are much less than these values.

The results for  $R_D = 500$  are seen in Table 3.9. It is inferred that adding the filter still makes the harmonics worse except for the single-line frequency at 100 Hz. The same is also true for  $R_D = 250$  and  $R_D = 150$  whose results are given in Tables 3.10 and 3.11 respectively.

**Table 3.9** Harmonic and Interharmonic Currents on the Bus for  $R_D = 500$

LF Transformer Primary Harmonic Currents without the 2nd and 3rd HF				LF Transformer Primary Harmonic Currents with the 2nd HF connected (RD=500)				LF Transformer Primary Harmonic Currents with the 2nd HF (RD=500) and 3rd HF connected			
Single Line Frequency	Amps	Gg,n	Amps	Single Line Frequency	Amps	Gg,n	Amps	Single Line Frequency	Amps	Gg,n	Amps
I (55 Hz)	125	<b>Gg,2 (Harmonic Group)</b>	106	I (55 Hz)	132	<b>Gg,2 (Harmonic Group)</b>	148	I (55 Hz)	138	<b>Gg,2 (Harmonic Group)</b>	180
I (60 Hz)	71			I (60 Hz)	75			I (60 Hz)	78		
I (65 Hz)	42			I (65 Hz)	43			I (65 Hz)	46		
I (70 Hz)	34			I (70 Hz)	36			I (70 Hz)	37		
I (75 Hz)	33			I (75 Hz)	34			I (75 Hz)	36		
I (80 Hz)	38	<b>Gsg,2 (Harmonic Subgroup)</b>	65	I (80 Hz)	43	<b>Gsg,2 (Harmonic Subgroup)</b>	101	I (80 Hz)	52	<b>Gsg,2 (Harmonic Subgroup)</b>	108
I (85 Hz)	39			I (85 Hz)	50			I (85 Hz)	60		
I (90 Hz)	41			I (90 Hz)	73			I (90 Hz)	106		
I (95 Hz)	38			I (95 Hz)	95			I (95 Hz)	99		
I (100 Hz)	42			I (100 Hz)	25			I (100 Hz)	32		
I (105 Hz)	32	<b>Gig,1 (Inter-harmonic Group)</b>	175	I (105 Hz)	25	<b>Gig,2 (Inter-harmonic Group)</b>	215	I (105 Hz)	27	<b>Gig,2 (Inter-harmonic Group)</b>	239
I (110 Hz)	25			I (110 Hz)	21			I (110 Hz)	28		
I (115 Hz)	24			I (115 Hz)	21			I (115 Hz)	24		
I (120 Hz)	22			I (120 Hz)	19			I (120 Hz)	29		
I (125 Hz)	21			I (125 Hz)	19			I (125 Hz)	34		
I (130 Hz)	20	<b>Gisg,1 (Inter-harmonic Subgroup)</b>	117	I (130 Hz)	21	<b>Gisg,2 (Inter-harmonic Subgroup)</b>	140	I (130 Hz)	39	<b>Gisg,2 (Inter-harmonic Subgroup)</b>	169
I (135 Hz)	21			I (135 Hz)	19			I (135 Hz)	31		
I (140 Hz)	26			I (140 Hz)	27			I (140 Hz)	28		
I (145 Hz)	34			I (145 Hz)	33			I (145 Hz)	27		

**Table 3.10** Harmonic and Interharmonic Currents on the Bus for  $R_D = 250$

LF Transformer Primary Harmonic Currents without the 2nd and 3rd HF				LF Transformer Primary Harmonic Currents with the 2nd HF connected (RD=250)				LF Transformer Primary Harmonic Currents with the 2nd HF (RD=250) and 3rd HF connected			
Single Line Frequency	Amps	Gg,n	Amps	Single Line Frequency	Amps	Gg,n	Amps	Single Line Frequency	Amps	Gg,n	Amps
I (55 Hz)	125	<b>Gg,2 (Harmonic Group)</b>	106	I (55 Hz)	132	<b>Gg,2 (Harmonic Group)</b>	140	I (55 Hz)	138	<b>Gg,2 (Harmonic Group)</b>	170
I (60 Hz)	71			I (60 Hz)	74			I (60 Hz)	78		
I (65 Hz)	42			I (65 Hz)	43			I (65 Hz)	46		
I (70 Hz)	34			I (70 Hz)	36			I (70 Hz)	38		
I (75 Hz)	33			I (75 Hz)	34			I (75 Hz)	36		
I (80 Hz)	38	<b>Gsg,2 (Harmonic Subgroup)</b>	65	I (80 Hz)	43	<b>Gsg,2 (Harmonic Subgroup)</b>	92	I (80 Hz)	51	<b>Gsg,2 (Harmonic Subgroup)</b>	99
I (85 Hz)	39			I (85 Hz)	49			I (85 Hz)	58		
I (90 Hz)	41			I (90 Hz)	71			I (90 Hz)	100		
I (95 Hz)	38			I (95 Hz)	84			I (95 Hz)	90		
I (100 Hz)	42			I (100 Hz)	27			I (100 Hz)	30		
I (105 Hz)	32	<b>Gig,1 (Inter-harmonic Group)</b>	175	I (105 Hz)	25	<b>Gig,2 (Inter-harmonic Group)</b>	209	I (105 Hz)	28	<b>Gig,2 (Inter-harmonic Group)</b>	232
I (110 Hz)	25			I (110 Hz)	21			I (110 Hz)	27		
I (115 Hz)	24			I (115 Hz)	21			I (115 Hz)	24		
I (120 Hz)	22			I (120 Hz)	19			I (120 Hz)	28		
I (125 Hz)	21			I (125 Hz)	20			I (125 Hz)	33		
I (130 Hz)	20	<b>Gisg,1 (Inter-harmonic Subgroup)</b>	117	I (130 Hz)	21	<b>Gisg,2 (Inter-harmonic Subgroup)</b>	138	I (130 Hz)	38	<b>Gisg,2 (Inter-harmonic Subgroup)</b>	164
I (135 Hz)	21			I (135 Hz)	19			I (135 Hz)	30		
I (140 Hz)	26			I (140 Hz)	24			I (140 Hz)	28		
I (145 Hz)	34			I (145 Hz)	33			I (145 Hz)	26		

**Table 3.11** Harmonic and Interharmonic Currents on the Bus for  $R_D = 150$

LF Tranformer Primary Harmonic Currents without the 2nd and 3rd HF				LF Tranformer Primary Harmonic Currents with the 2nd HF connected (RD=150)				LF Tranformer Primary Harmonic Currents with the 2nd HF (RD=150) and 3rd HFconnected			
Single Line Frequency	Amps	G <sub>g,n</sub>	Amps	Single Line Frequency	Amps	G <sub>g,n</sub>	Amps	Single Line Frequency	Amps	G <sub>g,n</sub>	Amps
I (55 Hz)	125	<b>G<sub>g,2</sub></b> <b>(Harmonic Group)</b>	106	I (55 Hz)	132	<b>G<sub>g,2</sub></b> <b>(Harmonic Group)</b>	133	I (55 Hz)	138	<b>G<sub>g,2</sub></b> <b>(Harmonic Group)</b>	162
I (60 Hz)	71			I (60 Hz)	74			I (60 Hz)	78		
I (65 Hz)	42			I (65 Hz)	43			I (65 Hz)	46		
I (70 Hz)	34			I (70 Hz)	35			I (70 Hz)	38		
I (75 Hz)	33			I (75 Hz)	34			I (75 Hz)	36		
I (80 Hz)	38	<b>G<sub>sg,2</sub></b> <b>(Harmonic Subgroup)</b>	65	I (80 Hz)	43	<b>G<sub>sg,2</sub></b> <b>(Harmonic Subgroup)</b>	82	I (80 Hz)	50	<b>G<sub>sg,2</sub></b> <b>(Harmonic Subgroup)</b>	92
I (85 Hz)	39			I (85 Hz)	48			I (85 Hz)	57		
I (90 Hz)	41			I (90 Hz)	68			I (90 Hz)	94		
I (95 Hz)	38			I (95 Hz)	73			I (95 Hz)	82		
I (100 Hz)	42			I (100 Hz)	29			I (100 Hz)	31		
I (105 Hz)	32	<b>G<sub>ig,1</sub></b> <b>(Inter-harmonic Group)</b>	175	I (105 Hz)	25	<b>G<sub>ig,2</sub></b> <b>(Inter-harmonic Group)</b>	203	I (105 Hz)	28	<b>G<sub>ig,2</sub></b> <b>(Inter-harmonic Group)</b>	227
I (110 Hz)	25			I (110 Hz)	21			I (110 Hz)	26		
I (115 Hz)	24			I (115 Hz)	21			I (115 Hz)	24		
I (120 Hz)	22			I (120 Hz)	19			I (120 Hz)	27		
I (125 Hz)	21			I (125 Hz)	20			I (125 Hz)	33		
I (130 Hz)	20	<b>G<sub>isg,1</sub></b> <b>(Inter-harmonic Subgroup)</b>	117	I (130 Hz)	20	<b>G<sub>isg,2</sub></b> <b>(Inter-harmonic Subgroup)</b>	136	I (130 Hz)	37	<b>G<sub>isg,2</sub></b> <b>(Inter-harmonic Subgroup)</b>	160
I (135 Hz)	21			I (135 Hz)	19			I (135 Hz)	29		
I (140 Hz)	26			I (140 Hz)	27			I (140 Hz)	27		
I (145 Hz)	34			I (145 Hz)	33			I (145 Hz)	25		

Decreasing the value of  $R_D$  further does not solve the problem because this time interharmonics of 90 and 95 Hz will not be amplified, but the 100 Hz component will not be filtered either. Moreover, as seen in Table 3.8, lower values of  $R_D$  are not feasible because of the high power loss during normal LF operation.

### 3.2.7. Optimizing the Value of $R_D$

Since decreasing the value of  $R_D$  does not solve the harmonic group and harmonic subgroup amplification problem, another measure must be taken. After making detailed simulations, the performance is seen to be very satisfactory if  $R_D = 250 \Omega$  is used when  $C_2$  value is also increased by an amount of 10%. The results for these values are seen in Table 3.12. Unfortunately, before this study has been carried out, the capacitors were purchased, so the values could not be changed. However, after the installation of the first phase of the project and obtaining field data, this fact will also be shown by practical results also and an increase in the value of  $C_2$  will be made afterwards. In summary, the value of  $R_D$  is chosen to be  $250 \Omega$  and the harmonic and interharmonic performance of the filter is satisfactory if  $C_2$  is increased by an amount 10%.

### 3.2.8. Optimizing the Value of $R_{TS}$

The value of  $R_D = 250 \Omega$  alone is shown to be inefficient for preventing the overvoltages on the filter capacitors as seen in Table 3.8. What has to be done is to take another parallel resistor into conduction during transient events. When the third and the fourth column data in Table 3.8 are considered and the parallel value of  $R_D = 250 \Omega$  and  $R_{TS}$  is used, it can be concluded that any  $R_{TS}$  value between 30 – 60 will cause the lossiest operation during transient states. The values larger than  $60 \Omega$  are shown to be ineffective for decreasing the overvoltages on the capacitors during transient events to an acceptable level. Thus, values lower than  $30 \Omega$  are used and simulations are made.

**Table 3.12** Harmonic and Interharmonic Currents on the Bus for  $R_D = 250$  and  $C_2$  Increased by an Amount of 10%

LF Transformer Primary Harmonic Currents without the 2nd and 3rd HF				LF Transformer Primary Harmonic Currents with the 2nd HF connected (RD=250) and C2 %10 increased				LF Transformer Primary Harmonic Currents with the 2nd HF (RD=250) and 3rd HF connected and C2 %10 increased			
Single Line Frequency	Amps	Gg,n	Amps	Single Line Frequency	Amps	Gg,n	Amps	Single Line Frequency	Amps	Gg,n	Amps
I (55 Hz)	125	<b>Gg,2 (Harmonic Group)</b>	106	I (55 Hz)	133	<b>Gg,2 (Harmonic Group)</b>	128	I (55 Hz)	139	<b>Gg,2 (Harmonic Group)</b>	151
I (60 Hz)	71			I (60 Hz)	75			I (60 Hz)	80		
I (65 Hz)	42			I (65 Hz)	45			I (65 Hz)	48		
I (70 Hz)	34			I (70 Hz)	35			I (70 Hz)	38		
I (75 Hz)	33			I (75 Hz)	35			I (75 Hz)	39		
I (80 Hz)	38	<b>Gsg,2 (Harmonic Subgroup)</b>	65	I (80 Hz)	44	<b>Gsg,2 (Harmonic Subgroup)</b>	50	I (80 Hz)	54	<b>Gsg,2 (Harmonic Subgroup)</b>	54
I (85 Hz)	39			I (85 Hz)	50			I (85 Hz)	67		
I (90 Hz)	41			I (90 Hz)	85			I (90 Hz)	95		
I (95 Hz)	38			I (95 Hz)	36			I (95 Hz)	38		
I (100 Hz)	42	<b>Gig,1 (Inter-harmonic Group)</b>	175	I (100 Hz)	25	<b>Gig,2 (Inter-harmonic Group)</b>	202	I (100 Hz)	27	<b>Gig,2 (Inter-harmonic Group)</b>	221
I (105 Hz)	32			I (105 Hz)	23			I (105 Hz)	27		
I (110 Hz)	25			I (110 Hz)	22			I (110 Hz)	26		
I (115 Hz)	24			I (115 Hz)	21			I (115 Hz)	26		
I (120 Hz)	22			I (120 Hz)	21			I (120 Hz)	27		
I (125 Hz)	21	<b>Gisg,1 (Inter-harmonic Subgroup)</b>	117	I (125 Hz)	20	<b>Gisg,2 (Inter-harmonic Subgroup)</b>	148	I (125 Hz)	33	<b>Gisg,2 (Inter-harmonic Subgroup)</b>	168
I (130 Hz)	20			I (130 Hz)	19			I (130 Hz)	39		
I (135 Hz)	21			I (135 Hz)	20			I (135 Hz)	30		
I (140 Hz)	26			I (140 Hz)	27			I (140 Hz)	26		
I (145 Hz)	34			I (145 Hz)	34			I (145 Hz)	25		

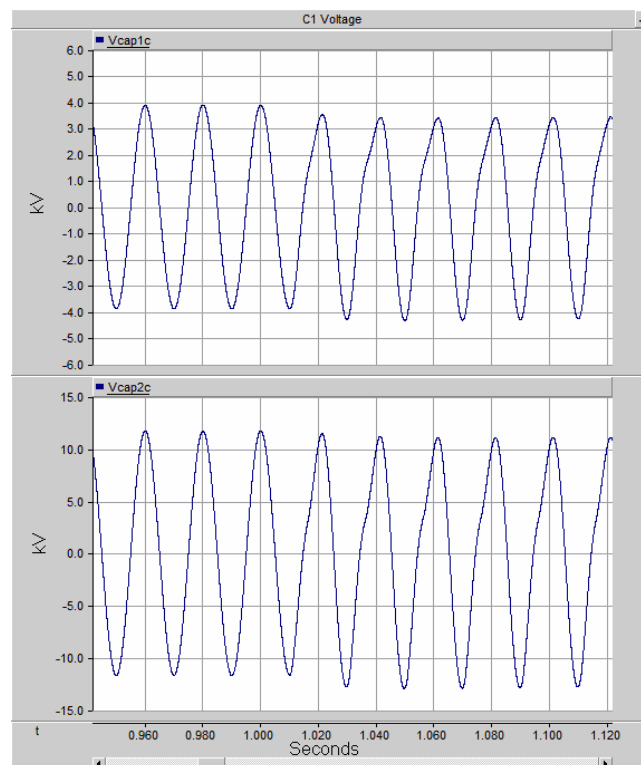
On the other hand, the value of  $R_{TS}$  is not decreased very much in order not to increase the power loss on it during normal operation of the LF. In fact, this loss calculation for  $R_{TS}$  is meaningless since it is not intended to be in conduction during normal operation of the furnace. However, as described in Section 4.4.1, due to the switching control algorithm,  $R_{TS}$  can be taken into conduction during a LF operation including heavy harmonics, thus the loss on it. If it stays in conduction by mistake, it should also be taken into account while deciding on the optimum  $R_{TS}$  value. Three main concerns when deciding on the value of  $R_{TS}$  are:

- i) The capacitor overvoltages during transformer inrush and filter energization: Reducing the values of  $R_{TS}$  decreases the capacitor overvoltages. It is aimed to keep the capacitor overvoltages within the limits of capacitor ratings.

ii) Power loss during normal LF operation (if taken into conduction for 3 seconds by mistake): Reducing the value of  $R_{TS}$  increases this steady-state loss. It is aimed that this power loss should be around 50 kW at maximum, for economical and dimensional reasons.

iii) Instantaneous maximum power loss during transformer inrush: It is shown that there is a power of maximum power loss for values or  $R_{TS}$  between 30 – 60 $\Omega$ . It is aimed that this power loss should be as low as possible in order to minimize the dimensions and avoid instant overheating of  $R_{TS}$ .

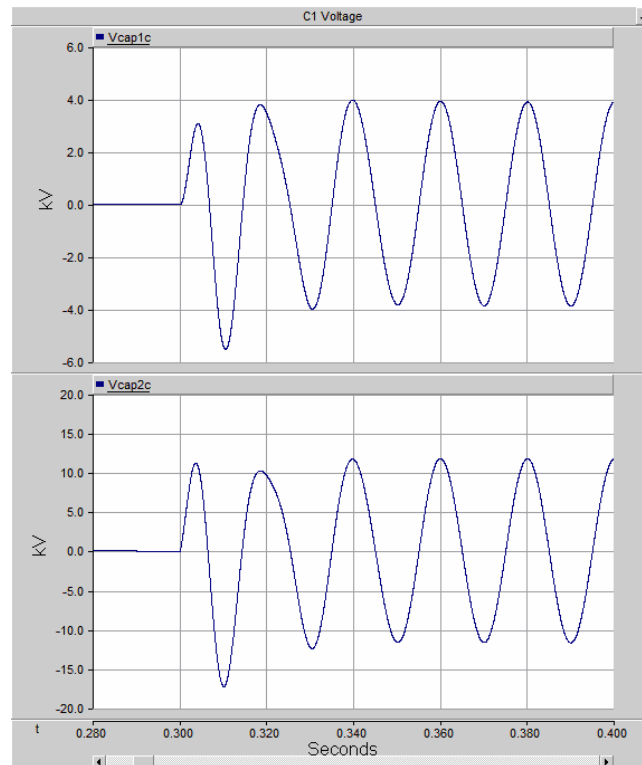
The optimum value of  $R_{TS}$  is decided to be 18  $\Omega$ . The capacitor overvoltages for  $R_{TS} = 18\Omega$  during the worst case transformer inrush and during the filter energization are given in Figure 3.22 and 3.23 respectively.



**Figure 3.22** The Overvoltages Seen on the Capacitors during Transformer Inrush when  $R_{TS} = 18\Omega$

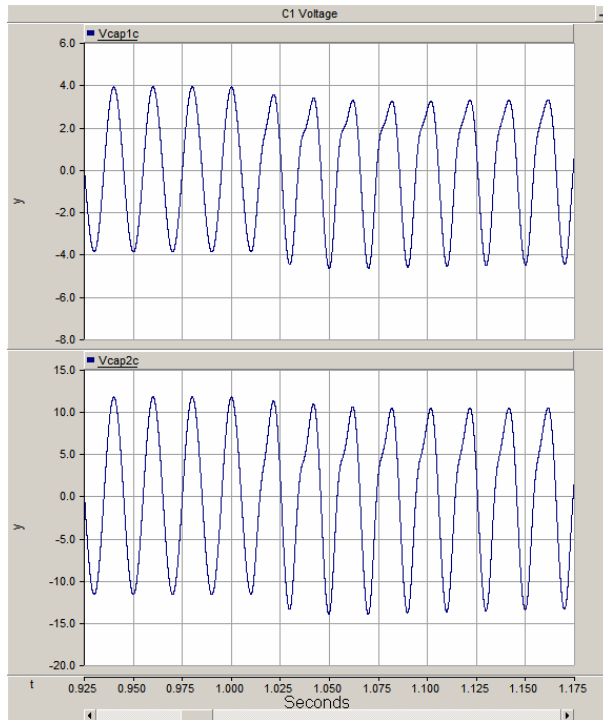


For comparison, the results in the case with  $R_{TS} = 30 \Omega$  are given in Figures 3.24 and 3.25. It is seen that, the overvoltages on the capacitors are a bit increased, there seems to be no difference at all, nevertheless, the maximum instantaneous power loss on  $R_{TS}$  is increase from 386 kW to 467 kW as given in Table 3.8.

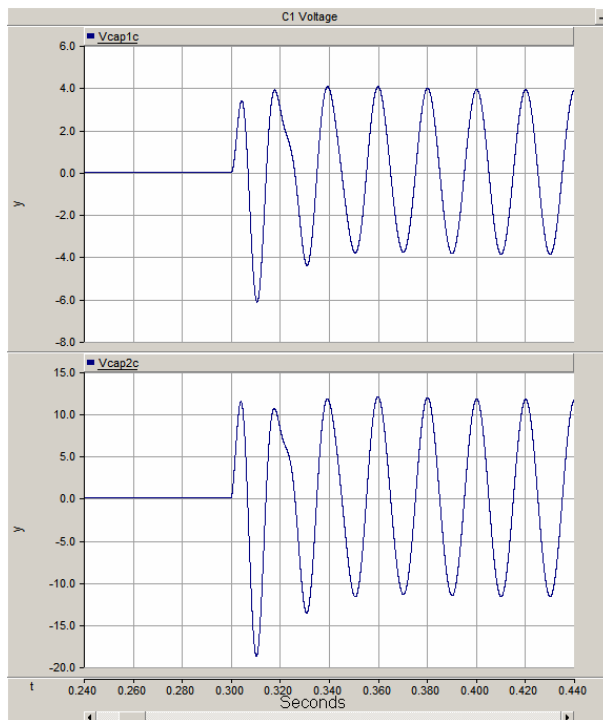


**Figure 3.23** The Overvoltages Seen on the Capacitors during Filter Energization when  $R_{TS} = 18 \Omega$

According to the simulation results obtained in this chapter, the specifications of the equipment that will be used, namely the damping resistors, solid-state switches and the control system can finally be determined. The detailed explanation is given in the following chapter, where the equipment and installation photographs are also included.



**Figure 3.24** The Overvoltages Seen on the Capacitors during Transformer Inrush when  $R_{TS} = 30 \Omega$



**Figure 3.25** The Overvoltages Seen on the Capacitors during Filter Energization when  $R_{TS} = 30 \Omega$

## CHAPTER 4

### IMPLEMENTATION OF THE OPTIMIZED C-TYPE 2<sup>ND</sup> HARMONIC FILTER

#### 4.1. GENERAL

According to the design whose details are given in the previous section, the specifications of i) the resistors, ii) the solid-state switches and iii) the control algorithm have to be defined. Apart from these, this section also includes the laboratory test results and the explained photographs of the work implemented at the site.

Since the harmonic inrush current decays to rated magnetizing branch current in approximately 3 seconds and the filter energization transients last much less this, the duration for which the resistor  $R_{TS}$  will be in conduction is set to be 3 seconds. This duration is very important while determining the resistor and the solid-state switch parameters, and implementing the switching control algorithm.

#### 4.2. SPECIFICATIONS OF THE RESISTORS $R_D$ AND $R_{TS}$

The optimum values for  $R_D$  and  $R_{TS}$  have been found in Section 3. Here, the detailed specifications of these resistors will be given.

Permanently connected damping resistance:  $R_D = 250 \Omega$

Thyristor switched damping resistance:  $R_{TS} = 18 \Omega$

Equivalent internal inductance of  
thyristor switched damping resistor:  $L_{TS} = 40 \mu\text{H}$

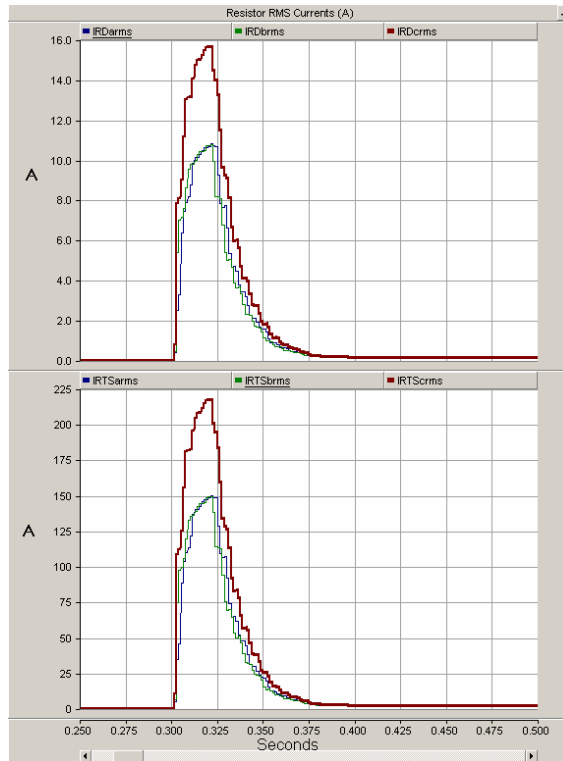
#### 4.2.1. Normal Operation Conditions

As mentioned before, the ladle furnace transformer is energized 70-80 times per day. During transformer energization, significant 2<sup>nd</sup> harmonic current component is produced. To protect the elements of the 2<sup>nd</sup> harmonic filter bank against undesirable effects of significant 2<sup>nd</sup> harmonic current,  $R_{TS}$  is connected to the circuit by triggering back-to-back connected thyristor strings.  $R_{TS}$  normally remains connected to the circuit at most for 3 seconds.

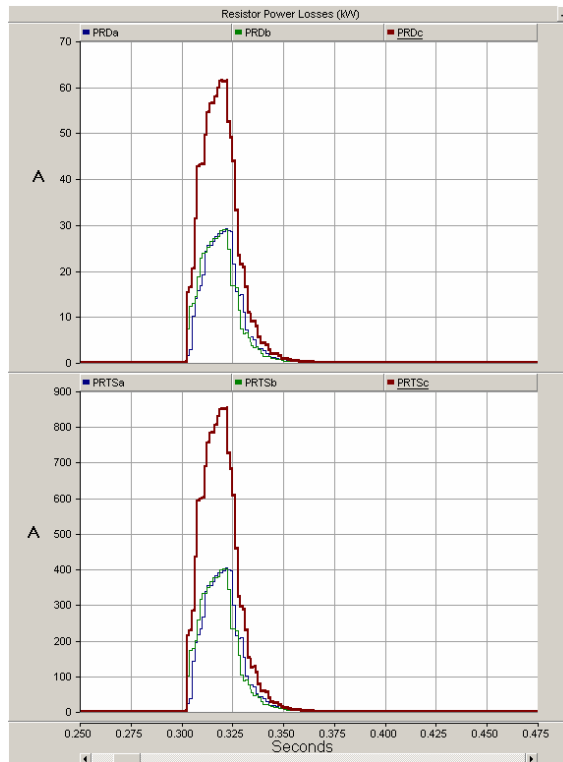
The 2<sup>nd</sup> harmonic filter is permanently connected to 13.8 kV bus and a similar operation will also take place for  $R_{TS}$  during connection of the 2<sup>nd</sup> harmonic filter bank to the circuit. Since the system is 3 $\Phi$ , three sets of single-phase damping resistors are needed.

Switching of a purely resistive load by thyristors is dangerous in a way that if the thyristors become conductive at the peak point of the voltage, the current will rise to the peak current immediately since no inductance exists in the circuit. In order to limit  $di/dt$  under the maximum value allowed for the thyristor, a series inductance with the resistor should be inserted externally, or the resistor itself should have an inductance. Hence,  $L_{TS}$  limits  $di/dt$  in thyristor strings to less than 300 A/ $\mu$ s during circuit-breaker and thyristor switchings.

During filter energization (between  $t = 0.3 - 0.4$ sec) and LF transformer energization cases (between  $t = 1.0 - 5.0$ sec), the currents through the resistors and the power losses on them are given in Figures 4.1 – 4.4. In Figure 4.1, the true rms currents through  $R_D$  and  $R_{TS}$  during the worst filter energization are seen. In Figure 4.2, the according power losses on the resistors are given. In Figure 4.3 and 4.4, the rms currents and the according power losses are given for the resistors respectively for the worst transformer inrush. It is seen in Figures 4.1 – 4.4 that the worst case results in the largest current and power loss in one of the phases, but not in all of them. However, the current and power specifications are determined based on the largest of all.



**Figure 4.1** Resistor True RMS Currents during Worst Filter Energization



**Figure 4.2** Resistor Power Losses during Worst Filter Energization

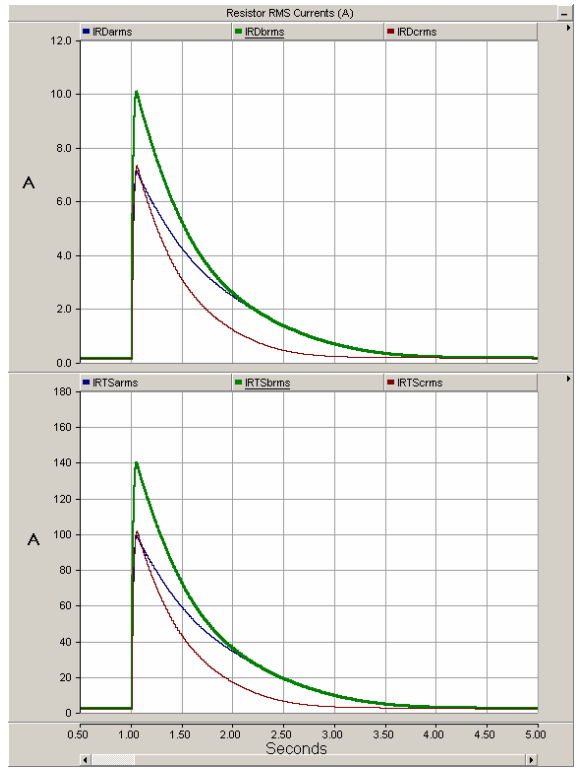


Figure 4.3 Resistor True RMS Currents during Worst Transformer Inrush

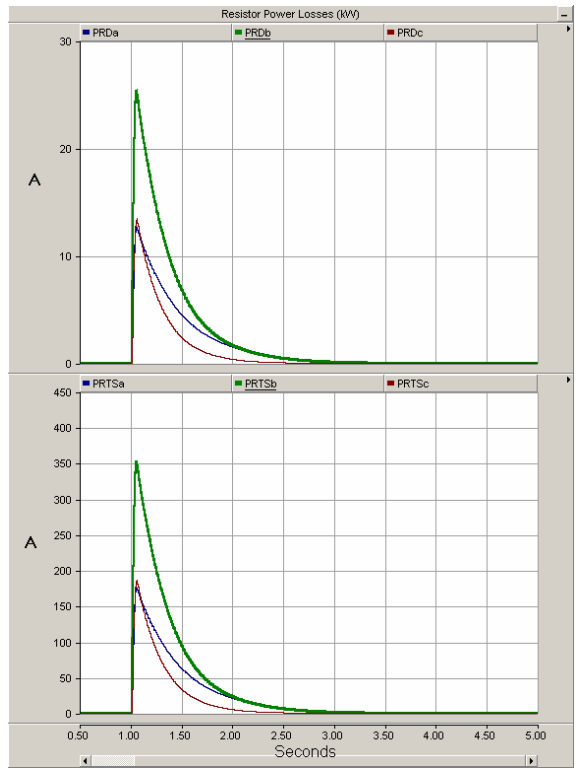


Figure 4.4 Resistor Power Losses during Worst Transformer Inrush

#### 4.2.2. Abnormal Operation Conditions

Apart from the intended operation of  $R_{TS}$ , the case which  $R_{TS}$  can not be taken into conduction due to any reason should be also considered for safe operation of the whole HF. In this case, the stress of filter energization and/or transformer inrush is totally on  $R_D$ , which is a case that is unwanted and the circuit-breaker (CB) of the filter should be opened. However,  $R_D$  must be capable of withstanding the inrush approximately for 100 msecs because this is the time duration for which the CB may respond in practice. For this case, the current through and power loss of  $R_D$  is given in Figure 4.5. The transformer is energized at  $t = 1.0$ sec by closing the transformer CB, and filter CB is opened at  $t = 1.1$ sec in order to protect the resistor  $R_D$  and the filter elements.

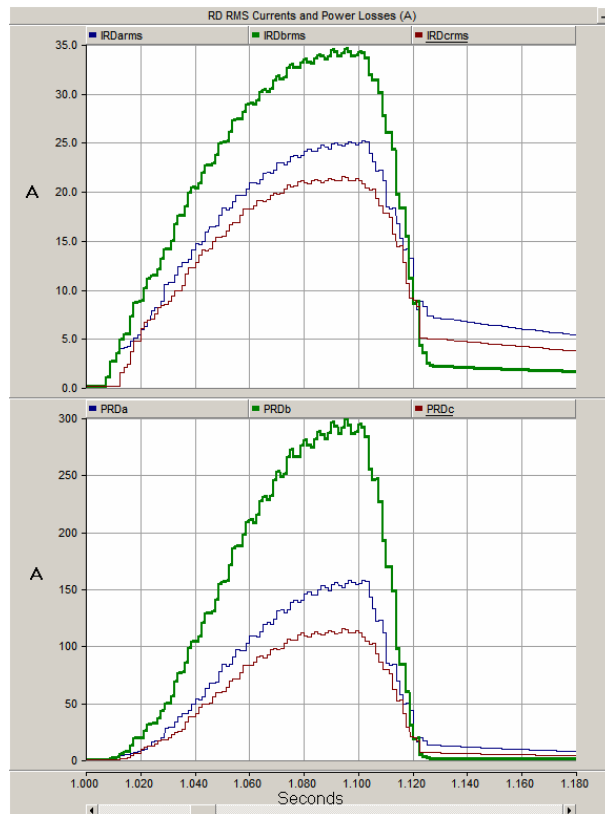


Figure 4.5 Currents Through and Power Losses of  $R_D$  during Worst Transformer Inrush when  $R_{TS}$  is not in Conduction

Another abnormal operation condition is that  $R_{TS}$  remains connected during normal LF operation to the circuit (this case also lasts 3 seconds)  $I_{R_{TS}} = 49.7$  A rms for this case, so the power loss of it =  $P_{R_{TS}} = 44.5$  kW for a period of 3 seconds.

### 4.2.3. Summary of Resistor Specifications

#### **For $R_{TS} (= 18\Omega)$ :**

During the transformer inrush case:

345 A peak	201 A rms	at $t = t_0$
117 A peak	86 A rms	at $t = t_0 + 0.5$ sec
88 A peak	40 A rms	at $t = t_0 + 1.0$ sec
58 A peak	20.4 A rms	at $t = t_0 + 1.5$ sec
35 A peak	10.6 A rms	at $t = t_0 + 2.0$ sec
18 A peak	5.8 A rms	at $t = t_0 + 2.5$ sec
8 A peak	3.9 A rms	at $t = t_0 + 3.0$ sec

On the other hand, during the rare filter energization case: (In the worst case, 10-minute period exists between the two consecutive filter energizations)

600 A peak	215 A rms	at $t = 0$
240 A peak	100 A rms	at $t = 20$ msec
87 A peak	50 A rms	at $t = 40$ msec
42 A peak	27 A rms	at $t = 60$ msec
27 A peak	16 A rms	at $t = 80$ msec
20 A peak	10.7 A rms	at $t = 100$ msec

#### **For $R_D (= 250\Omega)$ :**

During the transformer inrush case:

24.9 A peak	14.5 A rms	at $t = t_0$
9.5 A peak	6.22 A rms	at $t = t_0 + 0.5$ sec
6.4 A peak	2.89 A rms	at $t = t_0 + 1.0$ sec
4.2 A peak	1.47 A rms	at $t = t_0 + 1.5$ sec
2.5 A peak	0.76 A rms	at $t = t_0 + 2.0$ sec



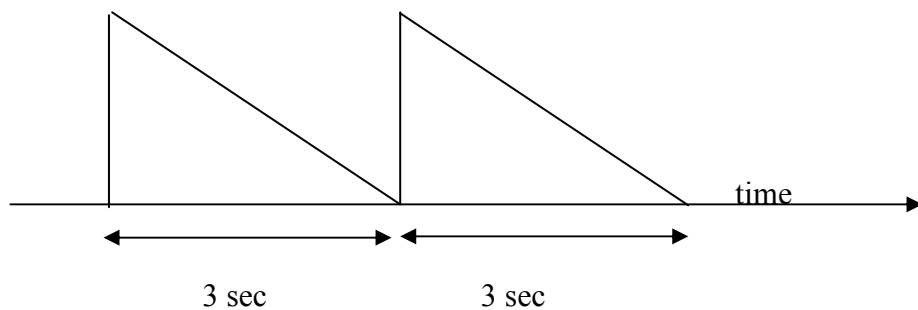
1.3 A peak	0.42 A rms	at $t = t_0 + 2.5$ sec
0.6 A peak	0.28 A rms	at $t = t_0 + 3.0$ sec

On the other hand, during the rare filter energization case: (In the worst case, 10-minute period exists between the two consecutive filter energizations)

48 A peak	23.2 A rms	at $t = 0$
38 A peak	17.7 A rms	at $t = 20$ msec
31 A peak	14.7 A rms	at $t = 40$ msec
25 A peak	13.3 A rms	at $t = 60$ msec
23 A peak	11.8 A rms	at $t = 80$ msec
20 A peak	9.2 A rms	at $t = 100$ msec
13.4 A peak	6.1 A rms	at $t = 150$ msec
9.0 A peak	4.3 A rms	at $t = 200$ msec

i) After the transformer inrush,  $18 \Omega$  resistor is switched out and only  $250 \Omega$  resistor stays in conduction, and this steady state normal filter operation loss of  $R_D$  is 10.2 kW per phase at maximum.

ii) In the case where  $R_{TS}$  accidentally remains energized during normal LF operation, the steady state loss of  $R_{TS}$  is 44.5 kWatts per phase. (This is expected to happen sometimes accidentally, maybe 1-2 times a day and last for again 3 seconds only due to the time-based control described in Section 4.4.1)



**Figure 4.6** Illustration of Two Consecutive Transformer Inrushes

iii) The thermal limit of the resistors should allow two consecutive transformer inrushes as the worst case as illustrated in the Figure 4.6 (2 times, 3 second inrushes).

iv) If during a transformer inrush, 18 Ω resistor can not be taken into conduction due to any reason, the current on the 250 Ω resistor will be much larger as given below.

61 A peak	41.6 A rms	at t = t <sub>0</sub>
20.7 A peak	12.0 A rms	at t = t <sub>0</sub> + 0.5 sec
10.0 A peak	5.3 A rms	at t = t <sub>0</sub> + 1.0 sec

Since this will cause too much power stress on the 250 Ω resistor, it must be avoided. Thus, when any current larger than 24.9 A peak (given in page 3) is measured on the 250 Ω resistor, the filter breaker will open, otherwise, the filter capacitors and the 250 Ω resistor will be damaged. However, assuming that the circuit breaker needs approximately 100msecs to open at maximum, the 250 Ω resistor should withstand the “61 A peak      41.6 A rms      at t = t<sub>0</sub>” for about 100msecs.

**Table 4.1** Resistor Current and Power Specifications

		<b>R<sub>D</sub> = 250 Ω</b>	<b>R<sub>TS</sub> = 18 Ω</b>
<b>1</b>	SS Losses (kWatts)	10.2	44.5 ( for 3 seconds )
<b>2</b>	Transformer Inrush max rms current (Amps)	10.1	140
<b>3</b>	Filter energization max rms current (Amps)	15.7	220

**Supply Conditions:**

Rated Voltage: 13.8 kV rms, line-to-line, ± 10% (7.97 kV rms, phase to ground, ± 10%)

Rated Frequency: 50 Hz ±1%

SCMVA: 380 MVA (at 13.8 kV bus)

**Service Conditions:**

Type: Outdoor

Temperature: -5 to +40 C<sup>0</sup>

Humidity: High

Pollution: Very heavily polluted

The resistors with these specifications were ordered from Schniewindt GmbH & Co. KG. The technical documentation is given in Appendix-B.

**4.3. SPECIFICATIONS OF THE SOLID-STATE SWITCHES****4.3.1. LTT Strings**

During transformer inrush and filter energization,  $R_{TS}$  is taken into conduction by means of solid-state switches. These switches are assemblies composed of back-to-back connected thyristor strings for each phase although the use of conventional Electronically Triggered Thyristors (ETTs), Light Triggered Thyristors (LTTs) has been preferred in this project due to their suitability for outdoor applications.

Direct Light-Triggered Thyristors have been well known since the 1960s. Because of the target market of High Voltage Direct Current transmission (HVDC), the LTTs are provided with overvoltage and  $dv/dt$  protection functions, both directly integrated into the thyristor. The thyristors are fabricated like electronically-triggered thyristors (ETTs) by well-established technologies. The only difference of production between ETTs and LTTs is the light sensitive gate area containing the integrated protection functions in the center of the thyristor [31]. Triggering of an LTT is achieved by a 40mW light pulse generated from a laser diode. The wavelength of the emitted light should be between 850 and 1000nm. Typical pulse durations are about 10 $\mu$ s. Some of the important properties of LTTs are as follows: [32]

i) The LTT has more or less the same case technology as the ETT. In contrast to the ETT, the ceramics of the LTT are not penetrated by a gate bushing. Instead, the light

pulse for triggering is applied directly to the center of the silicon wafer through the metal contact.

ii) The light pulse which triggers an LTT has a power of 40mW peak. This is equivalent to an electrical gate pulse of 50 A peak. In comparison, the gate pulse of electrically triggered thyristors typically has 3 A peak. Because of the improved turn-on performance, LTTs are much less vulnerable to high  $di/dt$  and to short-circuit currents.

iii) The LTT does not have internal gate contacts; in particular, it does not need a mechanical spring which may show fatigue after long years of operation. It is therefore inherently more reliable. Investigations of thyristor failures after more than ten years of operation have shown that in some cases, a deteriorated gate contact was the cause of the failure.

iv) The LTT does not need auxiliary energy or logic circuits at high potential. Therefore, the LTT does not need auxiliary energy for the firing circuits at thyristor potential, the duration of voltage reductions during AC system faults and of external faults (e.g. DC-trapped current) is of no importance. In addition, elimination of the gate drive unit at thyristor potential simplifies the wiring in the module, so there is less risk of accidental damage during maintenance. Elimination of the gate drive unit at thyristor potential also eliminates a potential source of partial discharges and electromagnetic interference (EMI) which gives an LTT valve an inherently higher reliability.

v) The entire individual thyristor protection is integrated in the LTT itself by means of a forward overvoltage protection firing (Break over diode-BOD). The internal overvoltage protection of the LTT has led to a significant improvement of the protection level. Even if the trigger signals to the thyristor are interrupted, the overvoltage protection feature remains fully operational, and this is especially important for thyristors connected in series.

vi) To fire all individual thyristors of each valve direction, only one light pulse is generated in the valve base electronics. It is transferred to high potential by a single fiber-optic cable.

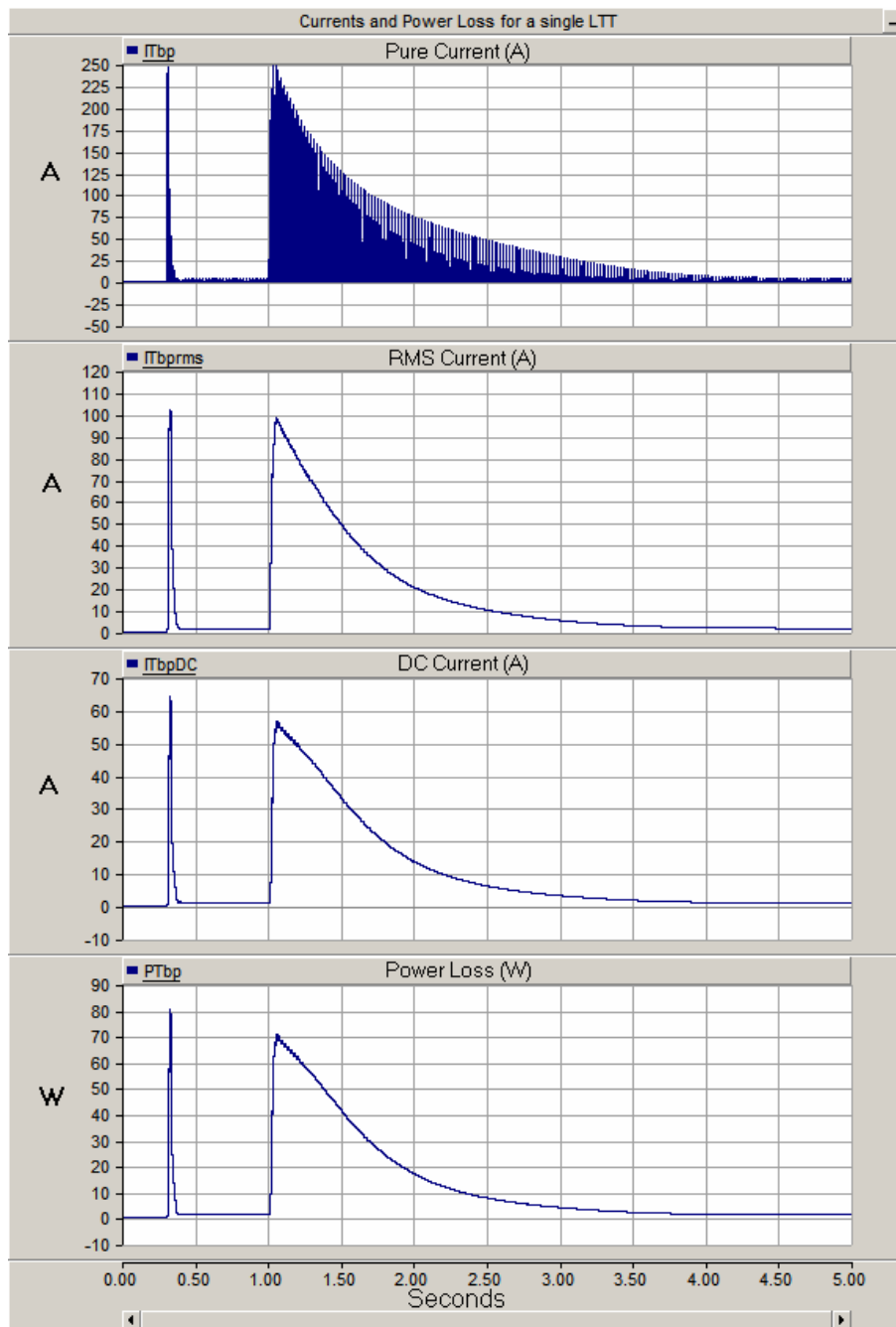
vii) All components in the light distribution system are standard components from the optical communication technology and commercially easily available.

The LTTs are manufactured only by EUPEC. The minimum current rating available for the LTTs is for T553N (see Appendix-C) and it is much larger than the operation current for the project. However, the current and power loss waveforms are included in this study.

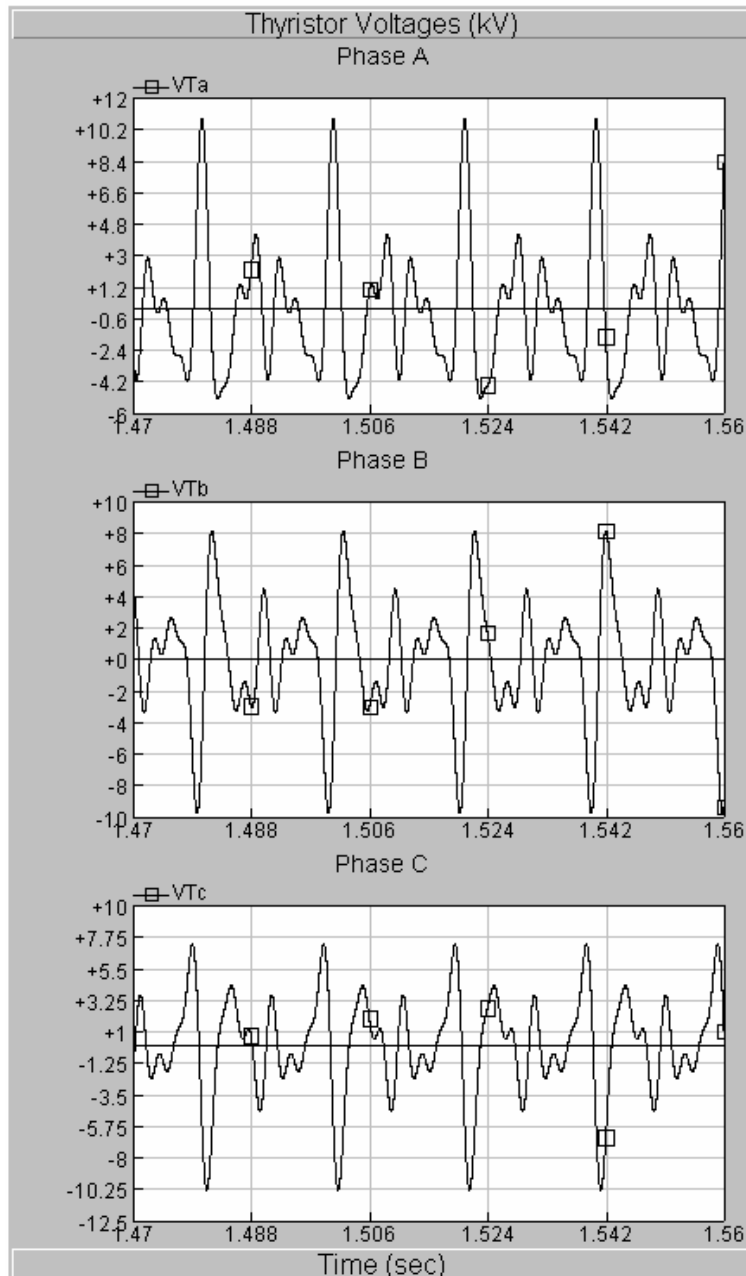
Current through and power loss of a single LTT during filter energization and transformer inrush cases are given in Figure 4.7. It is seen in Figure 4.7 that the mean current on a single LTT is less than 60 A at max and this value is much less than the rating of the LTT which is 550 A.

During normal operation of the filter,  $R_{TS}$  will be out of service, i.e., the thyristors will not be conducting. In this period, back-to-back thyristors are off and 11 kV peak voltages appear across the terminals of each thyristor string in both directions as given in Figure 4.8. However, 20 kV peak voltage appears across the thyristor string as the worst case, for the case that thyristors are not triggered into conduction or triggering operation is missed during energization of LF transformer.

In this outdoor application, light triggered thyristors are preferred by considering ease in packaging of back-to-back thyristor strings. EUPEC LTT / T 553N seems to be quite suitable by connecting four matched LTTs in series in each string as illustrated in Figure 4.9. Well designed static and dynamic equalizing circuits provide a good voltage sharing among LTTs even for the worst operating condition of  $V_{DRM} = V_{RRM} = 20$  kV peak.

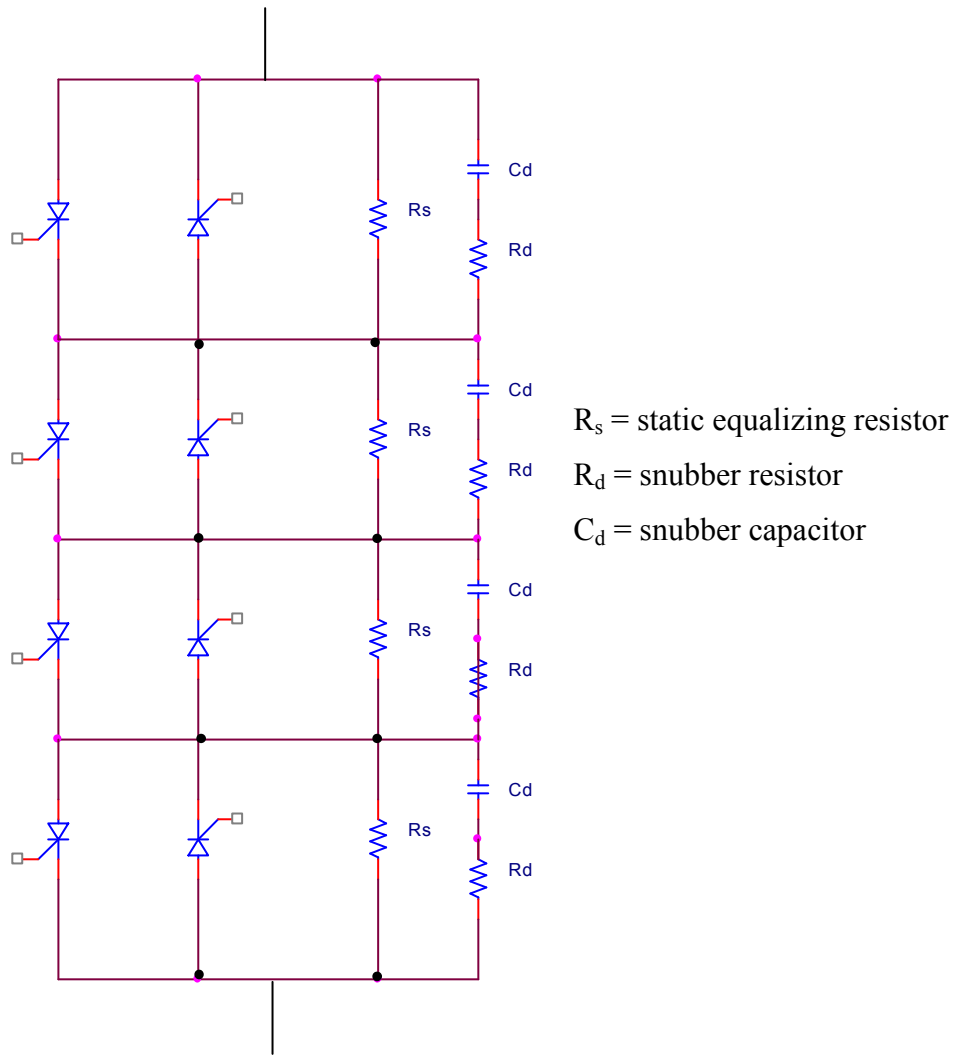


**Figure 4.7** Current Through and Power Loss of a Single LTT during Filter Energization and Transformer Inrush



**Figure 4.8** Thyristor String Voltage during Normal LF Operation

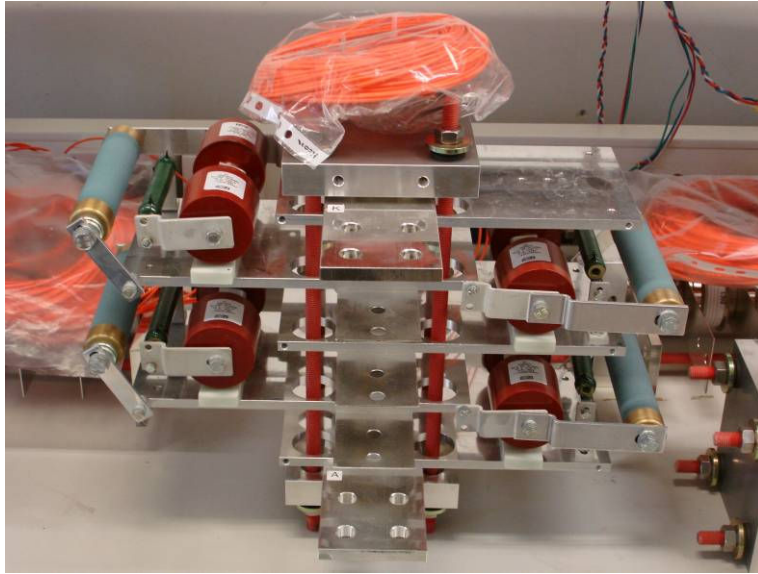
In view of the operation cycles, it seems that the rise in virtual junction temperature does not exceed 10 K. Therefore, it is decided that there is no need to use a cooling system for the thyristors. What is needed is five solid aluminum or copper bars (at the top and bottom and in between thyristors) in stack assembly in order to allow connection of active conductors, static and dynamic equalizing circuits.



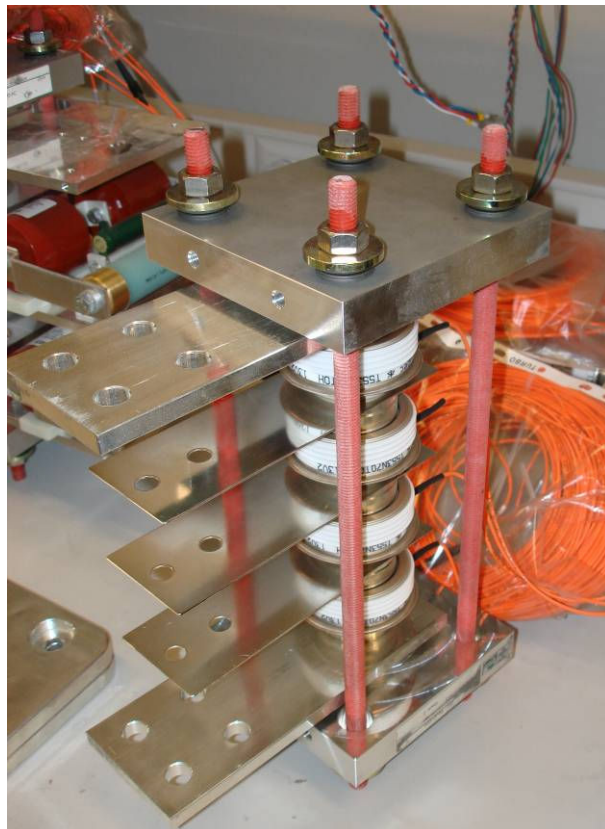
**Figure 4.9** An LTT Stack Consisting of Two Strings with 4 LTTs in Series for each Phase

The photograph of the LTT string with snubber is given in Figure 4.10, the one without the snubber is given in Figure 4.11 The technical documentation for the LTT stacks are given in Appendix-C.





**Figure 4.10** Photograph of the LTT String with Snubber



**Figure 4.11** Photograph of the LTT String without Snubber

### 4.3.2. LTT Triggering Units

The triggering of LTTs is achieved by means of light pulses. The triggering unit that sends the light pulses to the LTTs is named as Light Fired Thyristor Driver (LFTD).

There exists 8 thyristors for each LTT stack, so three LFTDs with laser outputs are required. The photograph of the LFTD is given in Figure 4.12. The technical documentation for the LFTD is given in Appendix-D.

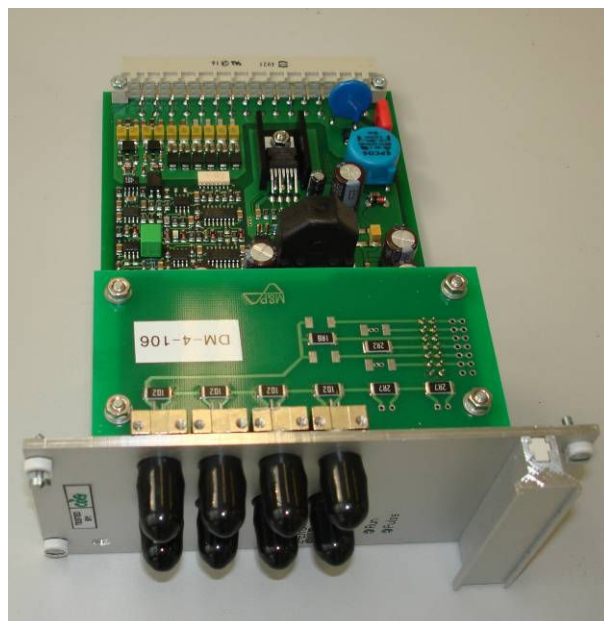


Figure 4.12 Photograph of the LFTD

## 4.4. SPECIFICATIONS OF THE CONTROL ALGORITHM

### 4.4.1. General

The control of the system is mainly taking  $R_{TS}$  into conduction when a filter energization and/or a transformer inrush is sensed.  $R_{TS}$  is taken into conduction by triggering the LTT stacks using LFTDs. The best way to sense filter energizations

and transformer inrushes is to follow the positions of filter and transformer CBs, respectively. When the position of CBs goes from OFF to ON, the LFTDs should trigger continuously for a period of 3 seconds. However, this was not put into practice in ERDEMİR, because the site at which the harmonic filter is installed is approximately 2 kms away from the LF transformer CB. Using a cable to carry the position signal of CB through such a distance seemed unpractical. Another solution may be using GPS signals, but this is also not reliable. Thus, another method was used.

The currents through the resistors  $R_D$  and  $R_{TS}$  are measured for all of the 3 phases. It is examined that for a transformer inrush that may be harmful for the capacitors, the peak current on  $R_D$  for at least one of the phases becomes larger than 10 A. Thus, the controller senses the transformer inrush when the current on at least one of  $R_D$ s becomes greater than 10 A peak, and it triggers  $R_{TS}$ s into conduction by means of LTTs. Apart from just sensing the correct triggering instant, the control algorithm has many other properties. Since the currents through the resistors  $R_D$  and  $R_{TS}$  in all phases are measured continuously, it can be decided on i) whether current passes through  $R_D$  in all phases during transformer inrush or not, ii) whether current passes through  $R_{TS}$  during transformer inrush or not, iii) whether the frequency of triggering is dangerously high or not, iv) whether current passes through  $R_{TS}$  or not, although no inrush is sensed, and v) whether there is a fault on the LFTDs or not. The check of these 5 conditions is made by the control algorithm apart from just triggering the LTTs into conduction.

#### **4.4.2. Control of LFTDs**

3 LFTDs are placed in the same rack together with an Auxiliary Card. The Auxiliary Card is used to send the input and reset pulses to the LFTDs and receive error signals from the LFTDs. The circuit schematic of the Auxiliary Card is given in Figure 4.13. The photograph of the card is given in Figure 4.14.

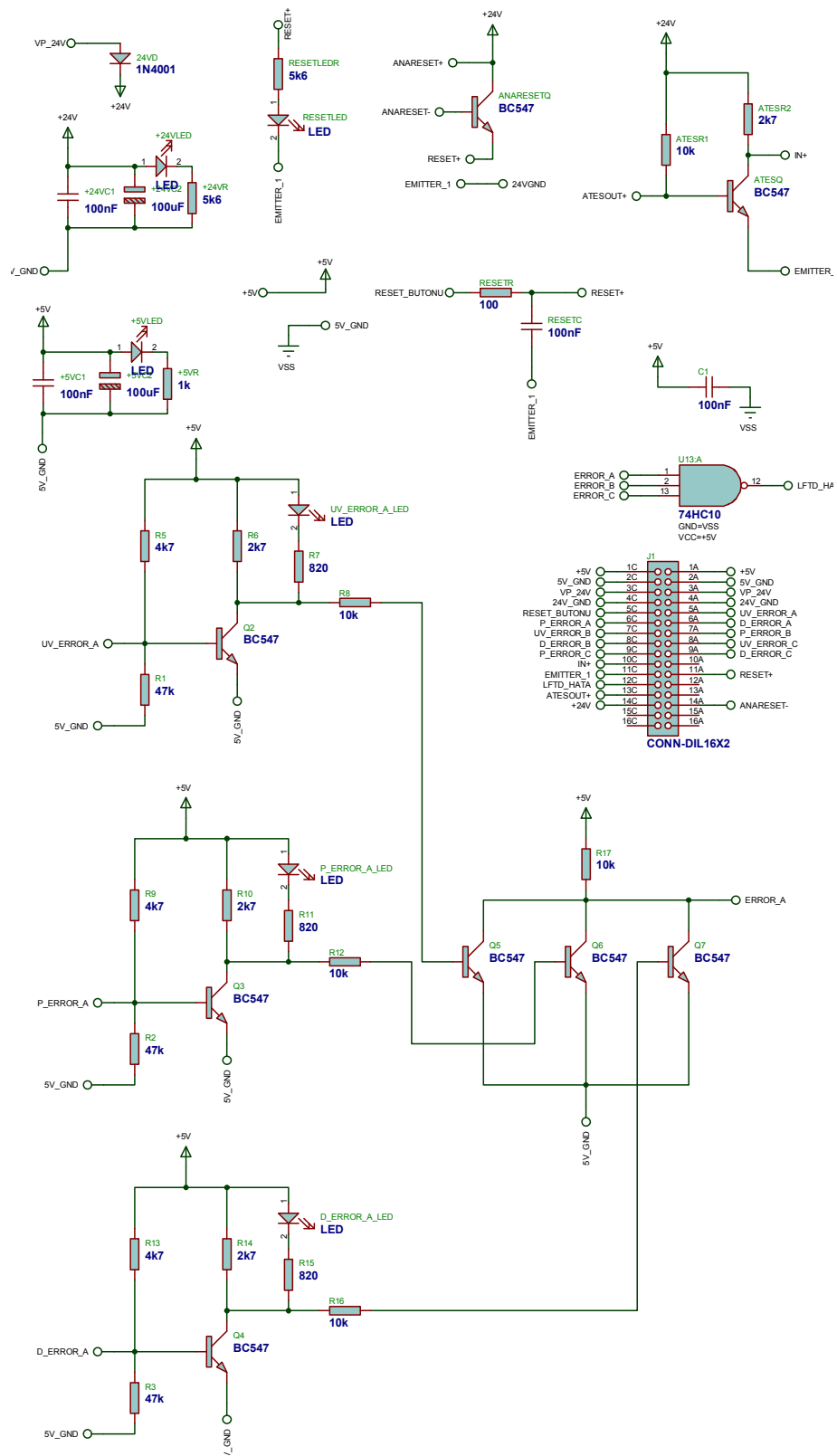
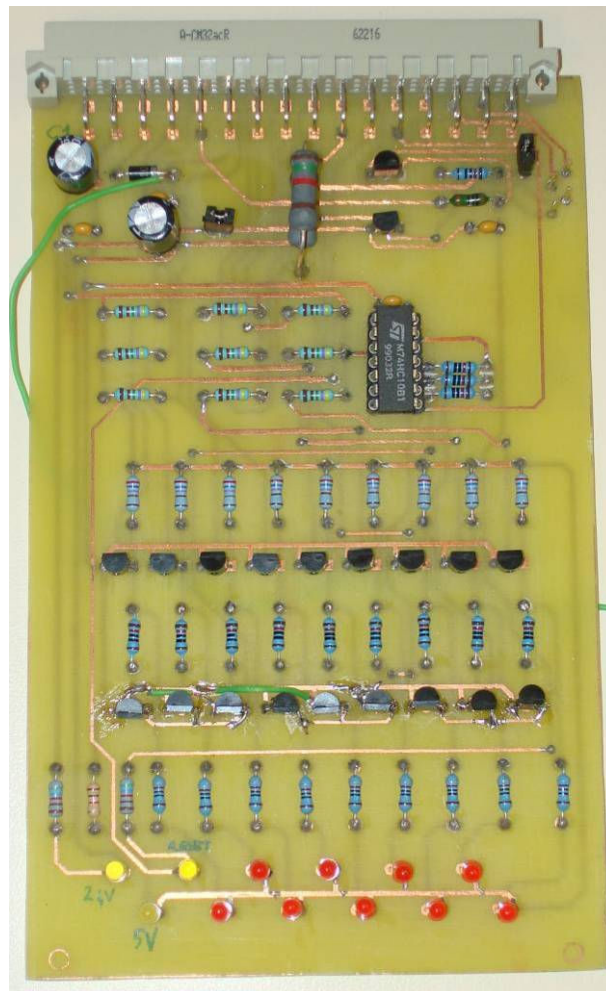


Figure 4.13 Circuit Schematic of the Auxiliary Card

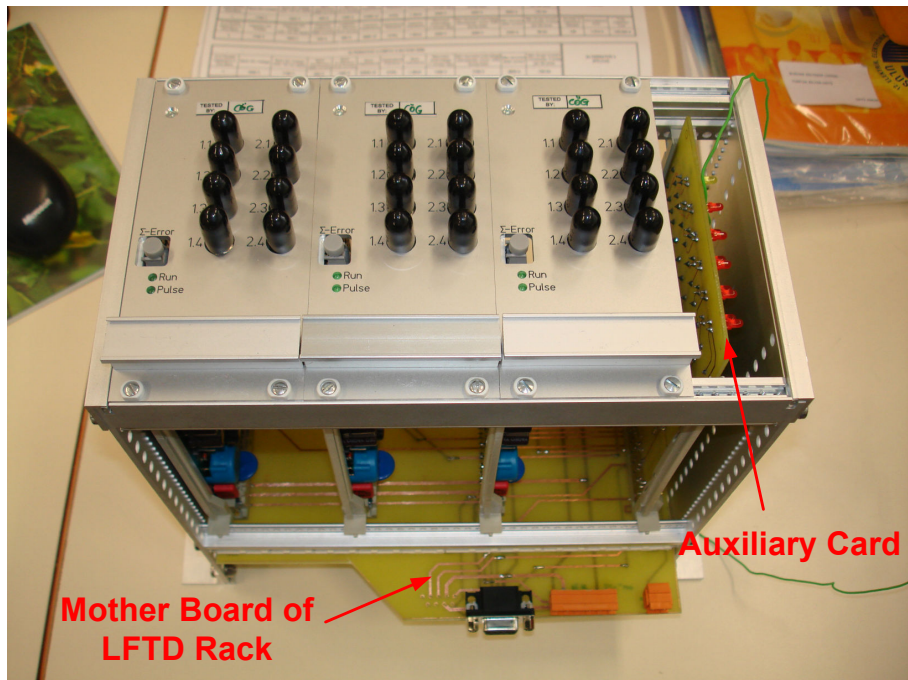
Pulse error, laser diode error and under-voltage error for any of the LFTDs are collected by the Auxiliary Card and the pin LFTD\_HATA sends the signal to the other control cards (Control Card 1 and Control Card 2). The manual reset of the LFTDs is made via a button connected to 24 V. The input trigger signal for LFTDs is sent through pin IN+ to the LFTDs.

The photograph of the rack including 3 LFTDs and the Auxiliary Card is given in Figures 4.15 and 4.16.

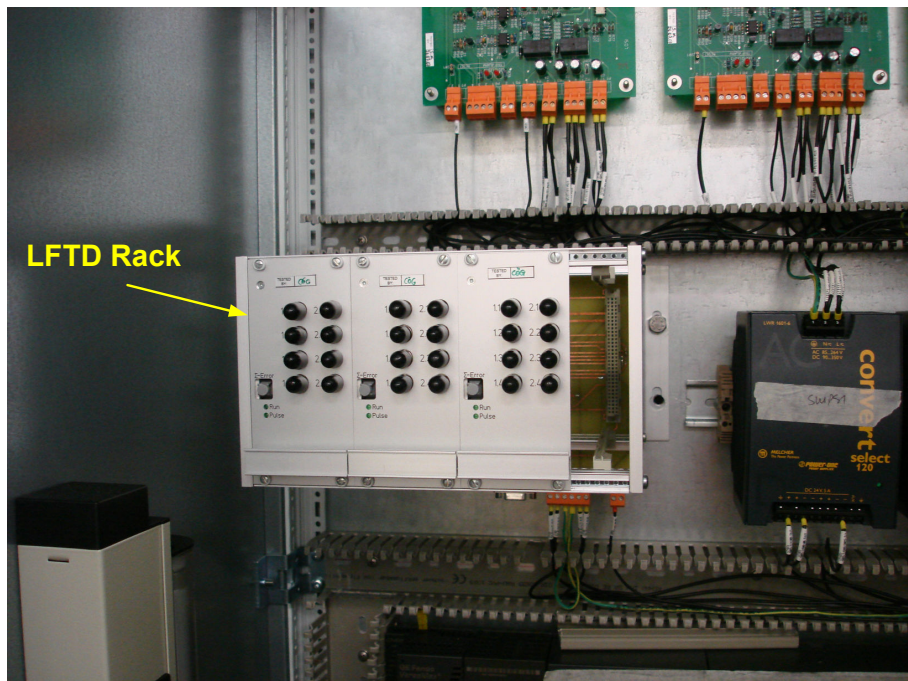


**Figure 4.14** Photograph of the Auxiliary Card





**Figure 4.15** Photograph of the Rack Including 3 LFTDs and the Auxiliary Card



**Figure 4.16** Photograph of the Rack Including 3 LFTDs and the Auxiliary Card (in the Control Panel)

#### 4.4.3. Current and Condition Control

The check for currents is made in Control Card 1 whose photograph is given in Figure 4.17. When the current thresholds are violated, Control Card 1 sends signals to Control Card 2. Control Card 2 has a micro-controller (PIC), 16F628A which makes the decisions and sends the triggering signals to the rack which LFTDs are mounted. It also sends signals to the main controller of TCR and the harmonic filter (PLC) in case of faults in order to take the harmonic filter out of operation to prevent any damage to equipment. The photograph of Control Card 2 is given in Figure 4.18. The controls that are made by these Control Cards are listed as follows:

- i) If any of the three phase currents through  $R_D$  s becomes larger than 10 A peak, it is sensed and triggering is started. (LTTs are fired for a period of 3 seconds.)
- ii) During the first 100msec of a transformer inrush that is sensed, for a duration of 40 msec, if any of the three phase currents through  $R_D$  becomes less than 3 A peak, it is sensed and it means that there is a fault in either  $R_D$  connection or  $R_D$  current sensing. A fault signal is sent to PLC and the harmonic filter CB is opened.
- iii) Although there is no triggering, if any of the currents through  $R_{TS}$  is above 10 A peak, this means that there is a false triggering or a short circuit. A fault signal is sent to PLC and the harmonic filter CB is opened.
- iv) During the first 100msec of a transformer inrush that is sensed, although the LTTs are triggered, if any of the currents through  $R_{TS}$  is below 3 A peak for a duration of 40 msec, this means that either there is a fault in  $R_{TS}$  connection or  $R_{TS}$  current sensing.
- v) The position of the harmonic filter CB is sensed. The position of the test button is also sensed. Test button is used to trigger the LTTs for a duration of 3 seconds manually. It is also used to clear a fault signal after the filter CB is made OFF, and

the maintenances are made. Then, the test button should be pressed manually in order to start the control system again before closing the filter CB.

vi) When there exists a fault in any of the LFTDs, it is sensed and a fault signal is sent to PLC and the harmonic filter CB is opened.

vii) If three consecutive triggerings (due to transformer inrush or filter energization) are made within a three-minute period, this is also sensed and a fault signal is sent to PLC and the harmonic filter CB is opened. This is because such frequent switching of LTTs will put  $R_{TS}$  and the LTTs themselves under stress due to frequent pulsed power loss, which violates their power capacities.

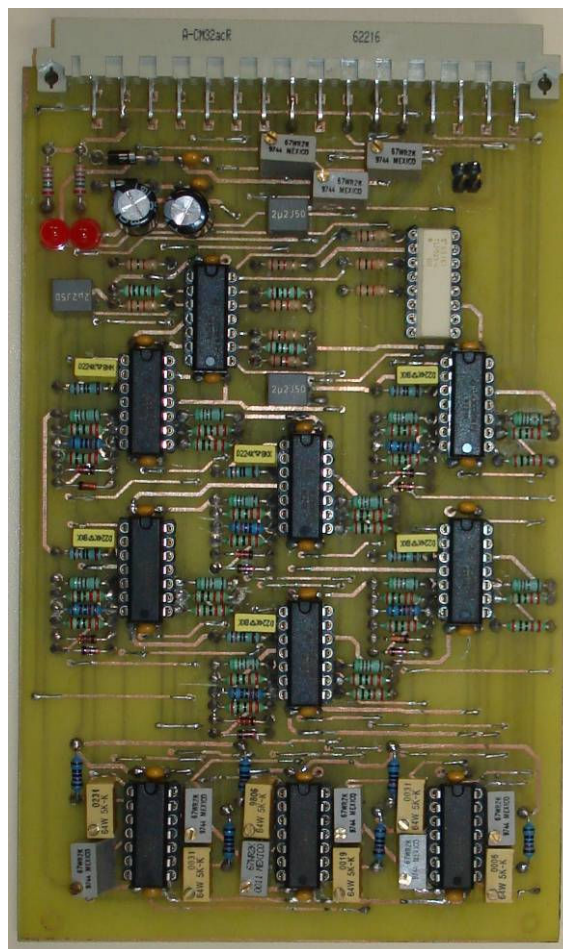
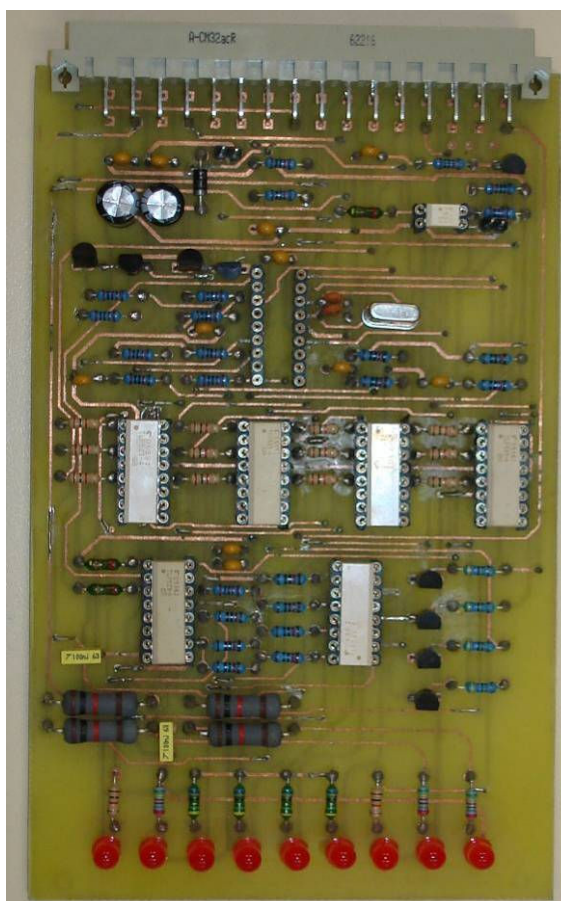


Figure 4.17 Photograph of Control Card 1





**Figure 4.18** Photograph of Control Card 2

The whole algorithm is implemented using C language by PIC-C CCS program. The code written for the PIC microcontroller in CCS is given in Appendix-E.

#### **4.5. LABORATORY TEST RESULTS**

Before installation to site, the LTTs, LFTDs and the control cards were tested in laboratory conditions. A single string consisting of 4 LTTs in series has been connected in series with a purely resistive load and this circuit has been energized from 300 V AC. The LFTDs were triggered manually. The observed voltage and current waveforms of the LTT string are given in Figure 4.19 and 4.20.

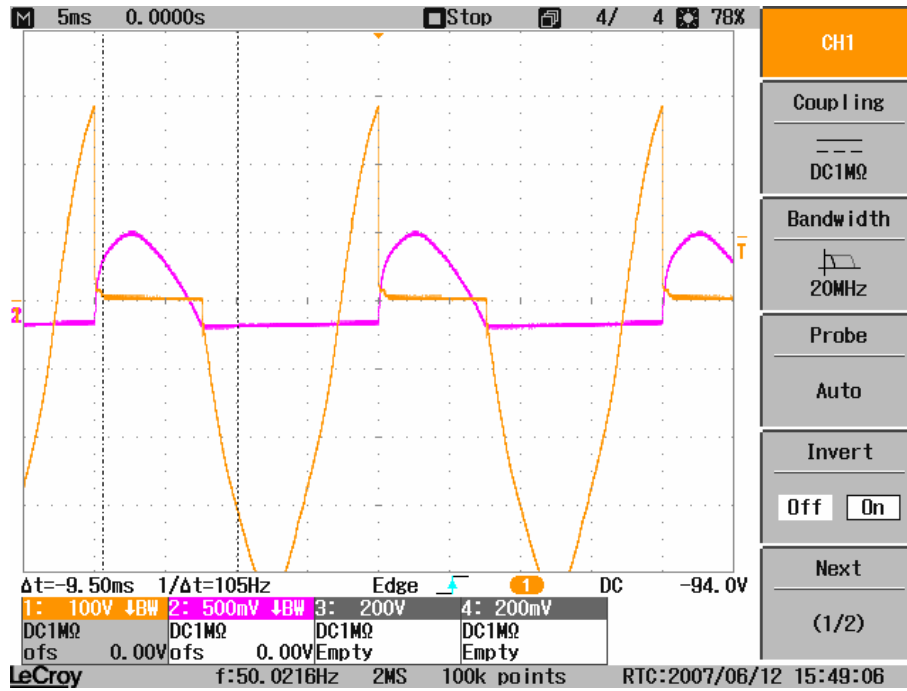


Figure 4.19 Voltage (Yellow) and Current (Pink) Waveforms of the LTT String under Purely Resistive Load

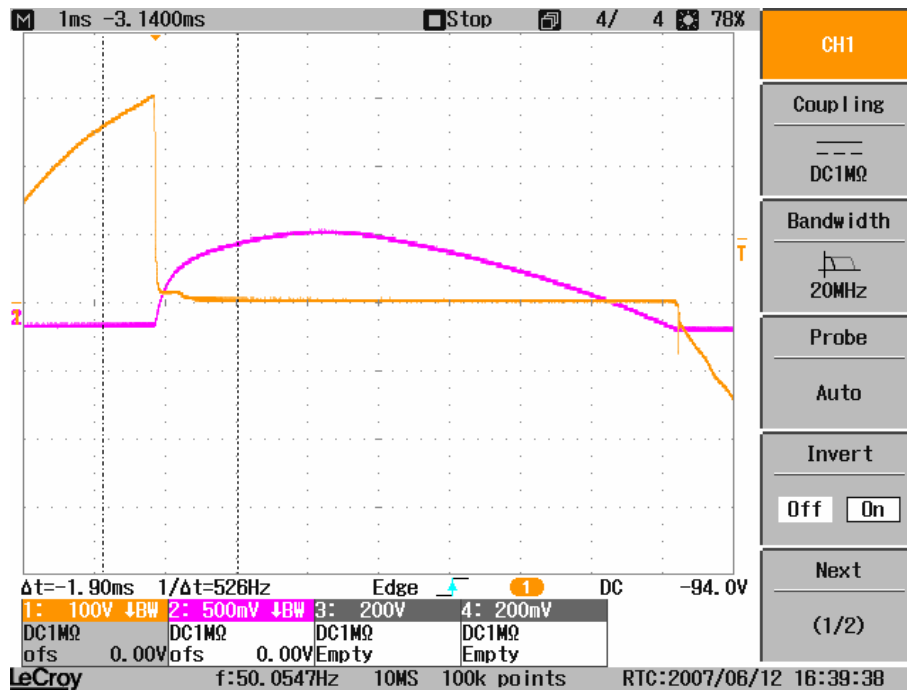


Figure 4.20 Voltage (Yellow) and Current (Pink) Waveforms of the LTT String during Turn-On

It is seen in Figure 4.19 that since only one string is in conduction, current passes through the LTTs during only the positive half cycle of the voltage. Another observation is that the current is seen to have a negative nonzero value during the negative half cycle of the voltage. This is in fact a measurement error and results from the DC saturation of the Rogowski coil used for current measurement. The current should stay at zero for the voltage negative half cycle.

From Figure 4.20, it is inferred that although the LTTs are triggered continuously, current starts to rise only after the string forward voltage reaches approximately 300 V. This issue has been discussed with the manufacturer and it has been learnt that a single thyristor needs a forward voltage of around approximately 75 Volts in order to be able to turn on. Since the actual voltage on an LTT string during normal operation will be around 10 kV, this will not be a problem. All of the LTT strings (6 of them, 3 with snubber, 3 without snubber) and LFTDs (3 of them) were tested one by one.

Apart from the laboratory tests made for LTTs and LFTDs, the control cards were also tested and the software programmed into the microcontroller chip was debugged based on the test results.

#### **4.6. INSTALLATION TO SITE**

2<sup>nd</sup> HF together with the TCR and the control systems have been installed to site by TÜBİTAK-UZAY Power Electronics Group recently. Although energization of the whole system is not made yet, the preparations are ready. Due to a power transformer allocation problem of ERDEMİR Management, the actual time of the system energization is not known yet. In this section, the installation photographs of the work made at site are given in Figures 4.21 – 4.28.

Apart from the uncertainty in time of energization, another important issue is that the measurement equipment for recording the capacitor voltages is not ready yet. As shown in Chapter 3, the most important parameter of concern for this study is the

overvoltages seen on the filter capacitors. When the filter is de-energized, remnant DC voltages are observed across the capacitors.

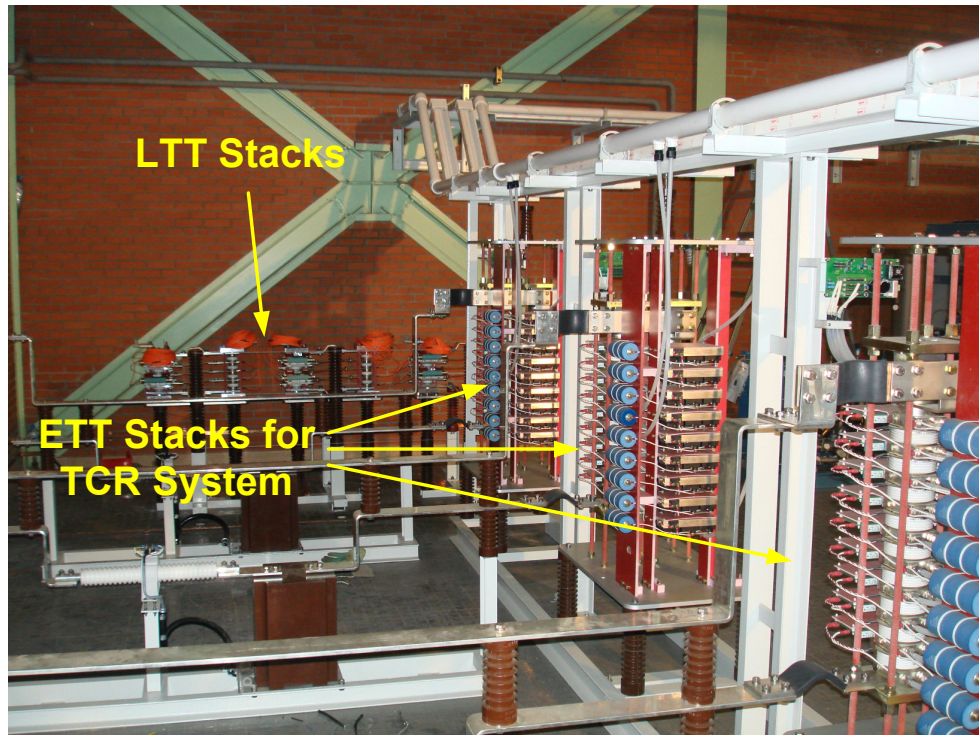


**Figure 4.21** Installation of LTT Stacks to Site



**Figure 4.22** Fiber Optic Cable Installation for LTTs

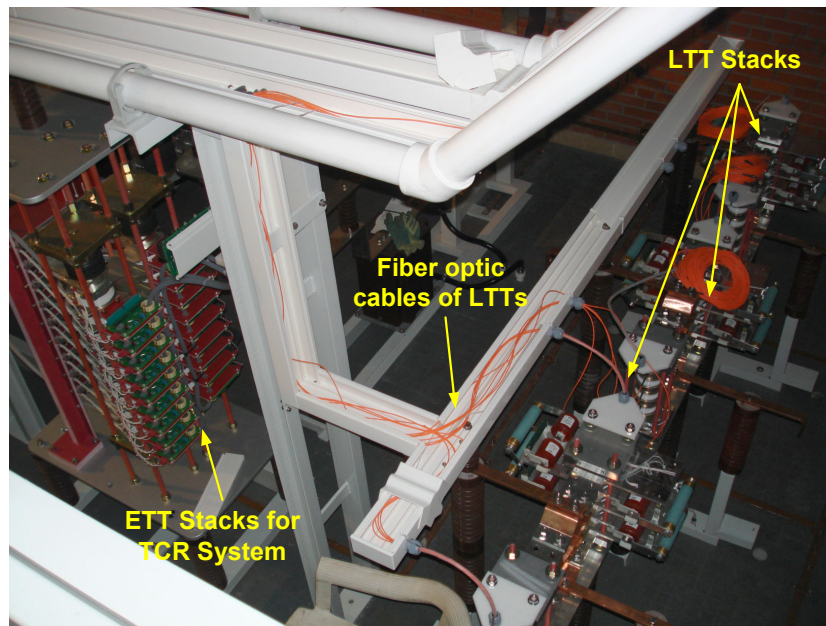
Conventional voltage transformers are not capable of measuring non-fundamental frequency components correctly. They can not measure DC values and moreover, they may be damaged. Thus, another method of capacitor voltage measurement has to be used.



**Figure 4.23** LTT Stacks and the Thyristor Assemblies of TCR System

Resistive-capacitive voltage transformers (RCVT) of TRENCH are suitable for capacitor voltage measurements that are investigated in this study and they have been ordered for different voltage levels in scope of the National Power Quality Project of Turkey seven months ago. However, they are not ready yet and they will arrive in Ankara in late October. Hence this study, unfortunately does not contain the field measurements after installation of the systems to site.





**Figure 4.24** LTT Stacks and Fiber Optic Cable Installation Seen from Top



**Figure 4.25** Water Cooling System of the ETT Stacks Used for TCR System



Figure 4.26 Installation of the TCR System

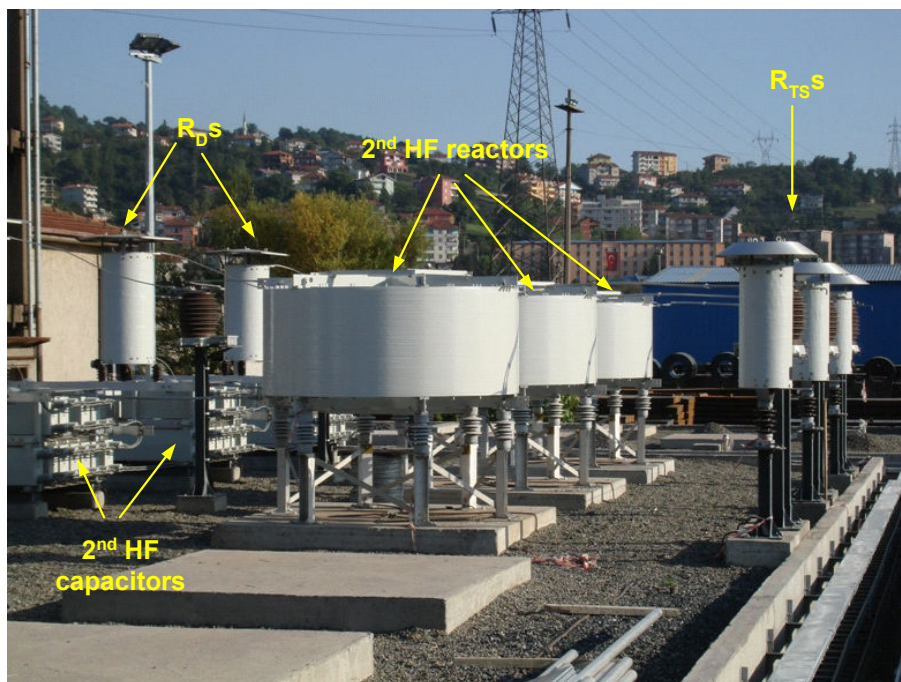


Figure 4.27 Installation of the 2<sup>nd</sup> HF

## CHAPTER 5

### CONCLUSION AND FUTURE WORK

#### 5.1. CONCLUSION

A C-Type 2<sup>nd</sup> Harmonic Power Filter as a part of the Static VAr Compensation System is installed in ERDEMİR Iron & Steel Plant for reactive power compensation of ladle furnaces (Project No: 7050503 signed between ERDEMİR Iron & Steel Plant Management and TÜBİTAK-UZAY Institute on 15/02/2006). Field data collected by mobile power quality measurement devices in iron & steel plants and within the scope of “National Power Quality Project of Türkiye” have shown that conventional TCR based SVC systems can not solve the power quality problems of iron & steel plants arising from electric arc furnace operation entirely. On this occasion, ERDEMİR LF Compensation Project has been considered as an opportunity to test the performance of new topologies for 2<sup>nd</sup> harmonic filter of TCR based SVCs. Thereby in the design phase, the C-Type 2<sup>nd</sup> Harmonic Power Filter mentioned above has been converted to a novel topology in order to comply with the current harmonics related issues of IEEE Std 519-1992 and IEC 61000-4-7 under the support of “National Power Quality Project of Türkiye” (Project No: 105G129). It is expected that the field test results of the novel C-Type 2<sup>nd</sup> Harmonic Filter could be a solution for the power quality problems of iron & steel plants arising mainly from arc furnaces. In this thesis work, the detailed analyses of the harmonic, interharmonic and flicker problems of the LF, together with the problems caused by the LF transformer inrushes and filter energizations, have been investigated.

It is concluded that a C-type HF with two different operation modes provides the best filter performance optimization for transient and steady-state cases, and filter safe



operation. During transformer inrushes and filter energizations, the C-type HF has to be operated in a high-damping mode in order to protect the filter capacitors from overvoltages caused by the large amount of 2<sup>nd</sup> harmonic current, whereas it should be operated in a low-damping mode for normal LF operation so as to provide efficient filtering characteristics. This approach is mainly based on using a permanently connected high-value resistor in parallel with a temporarily connected low-value resistor switched in and out by semi-conductor devices, namely Light Triggered Thyristors.

In this study, characterization of the LF in ERDEMİR as an electrical load has been made using the real time field data analyses. The problematic LF transformer inrushes have also been investigated and the voltage and current waveforms similar to the measured ones have been created in a power systems simulation tool, namely PSCAD, for further analysis. The capacitor overvoltages have been observed for different damping resistor values of the optimized C-type 2<sup>nd</sup> harmonic power filter, and the corresponding filtering performances have also been noted with these resistors. While interpreting the filtering performances, the latest harmonic, interharmonic and flicker measurement standards have been used. Transient and steady state performances with different resistor values have been compared and summarized, and then the optimum values for damping and switched resistors have been defined by using the simulation data.

The specifications of the equipment that will be used have been determined according to the simulation results. Parameters of the resistors and LTTs have been chosen and the relevant technical data have been given. The control algorithm for switching of LTTs has been discussed and the designed electronic cards have been described. After the controls and laboratory tests, the whole system has been installed to the site; the installation photographs have also been included.

Operation with two different modes for a C-type 2<sup>nd</sup> HF is the innovative side of this study. The unwanted effects during transient events, namely the transformer inrush and filter energization, are prevented from damaging the filter capacitors by means of

a novel method: Switching in a low-value resistor using LTTs. The value of the permanently connected resistor has been optimized regarding the filtering performance, interharmonic amplification and steady-state power losses. On the other hand, the value of the temporarily connected resistor is optimized regarding the capacitor overvoltages and the instantaneous power loss on it during the transformer inrush. It has been found out that there exists a critical point for the temporarily connected resistor value at which the instantaneous power loss during a transformer inrush becomes maximum ( $R_{TS} \approx 40 \Omega$ ). This is a novel inference of this study. Moreover, the filtering performance of the optimized C-type 2<sup>nd</sup> HF is investigated in 5 Hz frequency bands. This method is rather recent and has not been used for the SVC systems designed for arc and ladle furnaces in Turkey up to now. Therefore, the filtering performances of especially the conventional 2<sup>nd</sup> harmonic filters installed for arc and ladle furnaces in Turkey have been recorded to be unsatisfactory. This is because they had not been designed considering the interharmonic issues related to the nature of arc and ladle furnaces. This study shows that special attention should be given to the harmonic filter design for arc and ladle furnaces in order to prevent interharmonic and flicker amplification. Another conclusion is that harmonic subgroup elimination for 2<sup>nd</sup> harmonic (composed of 95 Hz, 100 Hz and 105 Hz single line frequencies) is usually not satisfactory enough for an arc or ladle furnace when passive harmonic filter configurations are used alone.

Although the simulation results show that the two mode operation of the optimized C-type 2<sup>nd</sup> harmonic power filter gives satisfactory results for both transient and steady-states, unfortunately, field measurements after installation to site could not be carried out due to the unexpected delay in energization of the system which is dependant upon ERDEMİR Management. Another factor for the absence of field measurements after installation to site is that the voltage measurement equipment capable of measuring non-fundamental frequency components correctly and withstanding DC voltages (RCVT) is not ready yet.

## 5.2. FUTURE WORK

The installation of the TCR and HF systems together with the control panels at ERDEMİR have been completed recently. However, the field measurements have not been started yet due to the unexpected delay in switchgear installation and energization of the system. In two or three months time, energizations will be made. Hence, the complete field measurements should be conducted by using RCVTS and the results should be compared with those obtained from the simulations and theoretical ones. The capacitor overvoltages and the harmonic subgroup filtering performance should be the main concerns while evaluating the measurement results. Then, the filter design change proposed in this study (10% increase in  $C_2$ ) need to be made. Afterwards, the field measurements should be repeated. The results may be again compared with the ones obtained from the simulations. The overall discussion can be the subject of a full paper to be sent to IEEE 43<sup>rd</sup> Annual IAS Meeting which will be held in Edmonton, Alberta, Canada on October 5-9, 2008.

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## APPENDIX – A

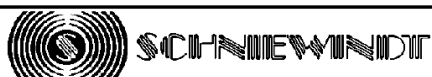
### MATLAB CODE FOR CALCULATION OF MAXIMUM POWER LOSS RESISTOR

```
1 - clear all;
2 - close all;
3 - clc;
4
5 - w=2*pi*50;
6 - Ls=1594/1000000;
7 - L1=14.25/1000;
8 - R1=0.08;
9 - C1=714/1000000;
10 - C2=238/1000000;
11
12
13 - I(1)=2000;
14 - I(2)=950;
15 - I(3)=300;
16 - I(4)=100;
17 - I(5)=80;
18
19 - for h=1:5,
20
21 -     for r=1:500,
22
23 -         Zeq(h,r)=r*(w*h*L1*j+R1-j/(w*h*C1))/(w*h*L1*j+R1-j/(w*h*C1)+r);
24 -         Zeq_mag(h,r)=abs(Zeq(h,r));
25 -         Zl(h,r)=Zeq(h,r)-j/(w*h*C2);
26 -         Zl_mag(h,r)=abs(Zl(h,r));
27 -         If(h,r)=I(h)*(w*h*Ls*j)/(w*h*Ls*j+Zl(h,r));
28 -         If_mag(h,r)=abs(If(h,r));
29 -         Ir(h,r)=If(h,r)*(w*h*L1*j+R1-j/(w*h*C1))/((w*h*L1*j+R1-j/(w*h*C1))+r);
30 -         Ir_mag(h,r)=abs(Ir(h,r));
31
32 -         P(h,r)=Ir_mag(h,r)*Ir_mag(h,r)*r/1000;
33
34 -     end
35
36 - end
37
38 - for r=1:500,
39
40 -     Ptot(r)=P(1,r)+P(2,r)+P(3,r)+P(4,r)+P(5,r);
41
42 - end
```

```
43  
44  
45  
46 - figure;  
47 - plot(Ptot(:))  
48 - grid on  
49 - title('MAXIMUM INSTANTANEOUS POWER LOSS ON RD')  
50 - xlabel('RD (Ohm)')  
51 - ylabel('kW')  
52
```

## APPENDIX – B

### RESISTOR TECHNICAL DOCUMENTS



<b>Document</b>	:	LD111329	
<b>Title</b>	:	List of Documents	
<b>Date</b>	:	2007-06-12	

<b>Object</b>	:	HV- Damping Resistor
<b>Project</b>	:	ERDEMIR – SVC 1432
<b>Type</b>	:	G-OI
<b>Manufacturing No.</b>	:	111329.1.1-3 (R <sub>D</sub> ) 111329.2.1-3 (R <sub>TS</sub> )
<b>Customer</b>	:	TÜBITAK-UZAY, Ankara, TURKEY
<b>Order No.</b>	:	B02.1.TBT.5.03.06.12-150-015

1. Technical Data Sheet		TD111329
2. Dimension Drawing		
2.1 item 1 (R <sub>D</sub> )		107046
2.2 item 2 (R <sub>TS</sub> )		107047
3. Transport Instruction		F9501_1.DOC
4. Storage Instruction		F9431_20.DOC
5. Table of Torques		F9431_19.DOC
6. Installation Instruction		II111329
7. Operation Instruction		F9443_2.DOC
8. Maintenance Instruction		F9536_2.DOC
9. Inspection Certificates		AP111329.1-2

		Issued by Dept.	QS / Schnabel	12.06.2007	Page : 1
		Design checked	T1 / M. Streit	12.06.2007	Cont. : -
No. of Revision / Modification	Date	Quality Management	Name	Date	

©: Dokumentations-Flussdiagramm V02 Typ 4 - Storage 111329 - 1PDE\_Engl\_Technik-Gen; Turkey LD111329.doc

**Document** : TD111329  
**Title** : Technical Data Sheet  
**Date** : 2007-06-12

## HV- Damping Resistor, single phase for outdoor use

### Item 1 (R<sub>D</sub>)

1.	Resistance	
	1.1 Resistance at nominal power	250 Ω
	1.1 Resistance at 20°C (no load)	223 Ω
	1.2 Resistance material	NiCrMo 25205
2.	Manufacturing tolerance	± 5 %
3.	Max. cont. current	6.4 A
4.	Max. cont. load	10.2 kW
5.	Inductance	max. 50 μH
6.	Insulation Level	95 kV <sub>BIL</sub>
7.	Ambient temperature range	-5°C....+40°C
8.	Protection Class	IP X3

			Issued by Dept.	QS / Schnabel	12.06.2007	Page : 1
			Design checked	T1 / M. Streit	12.06.2007	
						Cont. : 2
No. of Revision / Modification	Date	Quality Management	Name	Date		

**Document** : TD111329  
**Title** : Technical Data Sheet  
**Date** : 2007-06-12

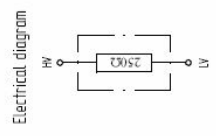
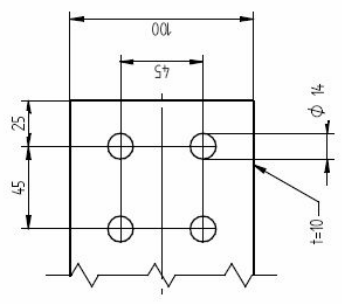
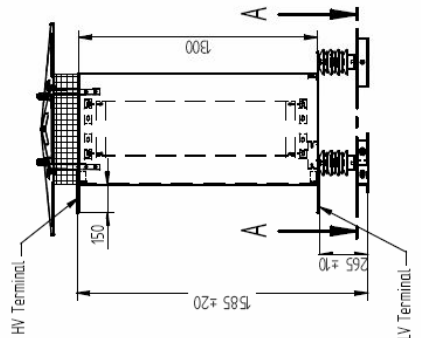
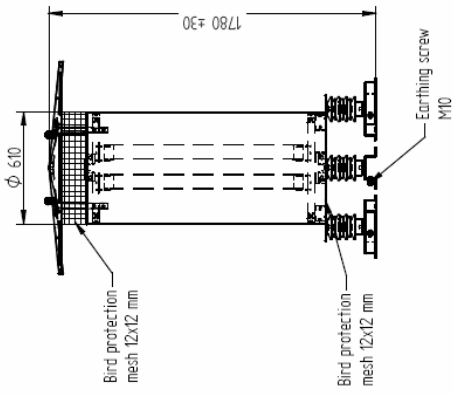
**Item 2 (R<sub>TS</sub>)**

- |  |                              |
|--|------------------------------|
| 1. Resistance  |                              |
| 1.1 Resistance at 20°C                                 | 18 Ω                         |
| 1.1 Resistance after short time load                   | 20.2 Ω                       |
| 1.2 Resistance material                                | NiCrMo 25205                 |
| 2. Manufacturing tolerance                             | ± 5 %                        |
| 3. Max. short time load                                | 44.5 kW for 3 s, twice a day |
| 4. Max. impulse energy on cold resistor                | 230 kJ                       |
| 5. Max. cooling down time between each short time load | 400 s                        |
| 6. Inductance  | max. 15 μH                   |
| 7. Insulation Level                                    | 95 kV <sub>BIL</sub>         |
| 8. Ambient temperature range                           | -5°C....+40°C                |
| 9. Protection Class                                    | IP X3                        |

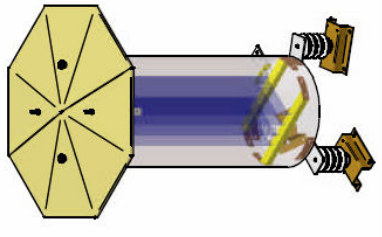
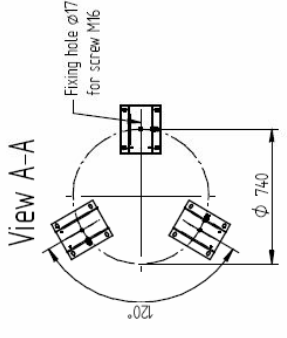
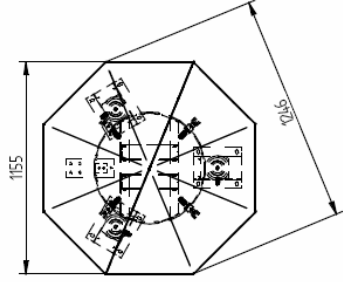
			Issued by Dept.	QS / Schnabel	12.06.2007	Page : 2
			Design checked	T1 / M. Streit	12.06.2007	
						Cont. : -
No. of Revision / Modification	Date	Quality Management	Name	Date		

H:\Dokumente\oscar\Fabrikdaten\td\FDZ Typ 4\_Scoreggi\111329\_1\FDZ\_Engl\_Tibink-Utay\_Turkey\TD111329.doc

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over to third parties.  
Carryover will be provided.

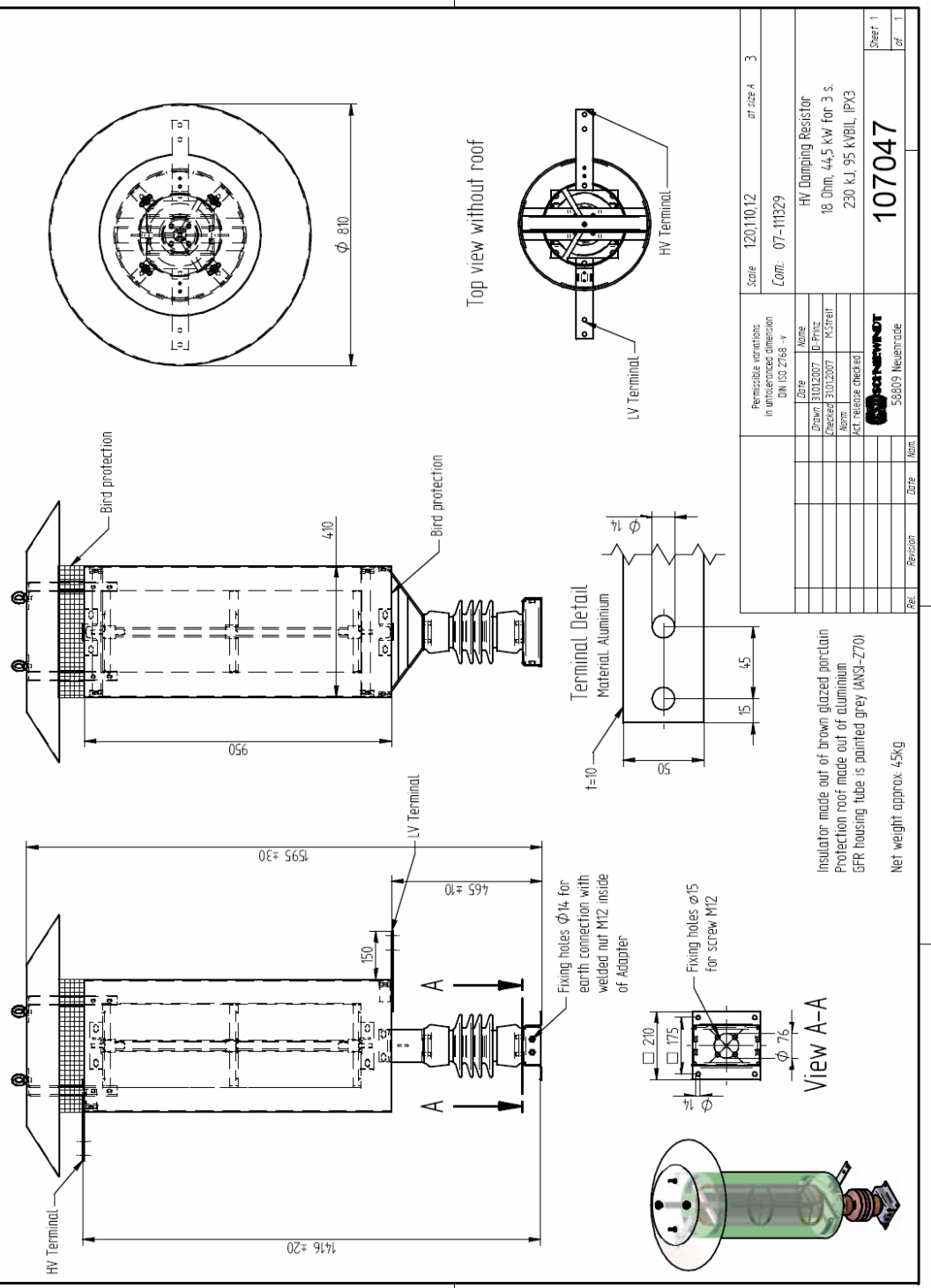


HV terminal is connected to the roof and bird protection grid



Permissible variations in dimensions (DIN ISO 2768-mS)	Scale	1:20; 1:10; 1:2	Sheet 1 of 1
Date	Com:	07-11329	
Drawn	Name	HV-Damping Resistor	
Checked	IP-Prüfung	250 ohm, 10.2kV, 95kVBL, IPX3	
Norm	ACT release checked		
Part	Revision	Date	Name
Steel parts are hot-dip galvanised, protection roof made out of stainless steel. (14301) Colour of tube:RAL7035 Grey Colour of support insulators: brown Max. terminal load: 500N Weight: approx. 75kg			
107046			

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Contribution will be protected.



Permissible variations in unbracketed dimension		Scale	120,110,12	at size A	3
DIN ISO 2768-1		Com.	07-111329		
Date	Name	HV Damping Resistor			
Drawn 31/01/2007	D-Prinz	18 Ohm, 44,5 kW for 3 S.			
Checked 31/01/2007	RS/Striel	230 kV, 95 KVBL, IPX3			
Norm					
ACT release checked					
 58809 Neuetrade		107047			
		Sheet	1		

**Abnahmeprüfzeugnis „3.1“ gemäß DIN EN 10 204**  
**Inspection Certificate „3.1“ according to DIN EN 10 204**

 Dateiname /  
 Filename: 111329.1-2  
 Seite / Page: 1 von / of 2

**Gerätebezeichnung** / Test Object: HV-Dämpfungswiderstand / HV-Damping Resistor  
**Auftrag-Nr.** / Order No.: 111329.1.1-3 / 111329.2.1-3  
**Kunde** / Customer: TÜBITAK-UZAY, Odtu Balgat Ankara, TURKEY  
**Ihre Auftrag-Nr.** / Your Order No.: B02.1.TBT.5.03.06.12-150-015, Date 10.01.2007  
  
**Technische Daten** / Technical Main Data: 111329.1.1-3 / 111329.2.1-3  
**Nominal-Widerstand (20°C)** / Rated Resistance (20 °C): 223 Ω ± 5 % / 18 Ω ± 5 %  
**Zeichnungs-Nr.** / Drawing No.: 107046 / 107047

**1 DC Widerstandsmessung / DC resistance measurement**

Serien-Nr.	Nominal-Widerstand in Ω bei 20 °C	Min. / Max. Widerstand in Ω	Gemessener Widerstand in Ω
Serial No.	Nominal Resistance in Ω at 20 °C	Min. / Max. Resistance / Ω	Measured Resistance / Ω
111329.1.1	223	211.85 / 234.15	222.9
111329.1.2	223	211.85 / 234.15	224.7
111329.1.3	223	211.85 / 234.15	224.0

*Fehlergrenze der Messeinrichtung:* 0,1 % (Fluke 8062)  
*Limit of error of the measuring equipment:* 0,1 % (Fluke 8062)

Serien-Nr.	Nominal-Widerstand in Ω bei 20 °C	Min. / Max. Widerstand in Ω	Gemessener Widerstand in Ω
Serial No.	Nominal Resistance in Ω at 20 °C	Min. / Max. Resistance / Ω	Measured Resistance / Ω
111329.2.1	18	17.1 / 18.9	17.9
111329.2.2	18	17.1 / 18.9	17.9
111329.2.3	18	17.1 / 18.9	17.9

*Fehlergrenze der Messeinrichtung:* 0,05 % (Fluke 187)  
*Limit of error of the measuring equipment:* 0,05 % (Fluke 187)

Seite 1 von 2

Version: 1 vom 10.07.2000

Dokument: FO 160021

FORMULAR



## APPENDIX – C

### LTT TECHNICAL DOCUMENTS

Technische Information / Technical Information																																																	
Lichtzündbarer Netzthyristor mit integriertem Überspannungsschutz  Light Triggered Phase Control Thyristor with integrated overvoltage protection	<b>T 553 N 70 TOH</b>	<b>N</b>																																															
<p><b>Features:</b></p> <table style="width: 100%; border: none;"> <tr> <td style="width: 50%; vertical-align: top; padding: 5px;"> <p><b>Lichtgezündeter Netz Thyristor mit integriertem. Überspannungsschutz</b></p> <p>Volle Sperrfähigkeit bei 120° mit 50 Hz</p> <p>Hohe Stoßströme und niedrige Wärme-widerstände durch NTV-Verbindung zwischen Silizium und Mo-Trägerscheibe.</p> <p>Elektroaktive Passivierung durch a - C:H</p> </td> <td style="width: 50%; vertical-align: top; padding: 5px;"> <p><b>Phase Control Thyristor, light triggered with integrated overvoltage protection</b></p> <p>Full blocking capability at 120°C with 50 Hz</p> <p>High surge currents and low thermal resistance by using low temperature-connection NTV between silicon wafer and molybdenum.</p> <p>Electroactive passivation by a - C:H</p> </td> </tr> </table>					<p><b>Lichtgezündeter Netz Thyristor mit integriertem. Überspannungsschutz</b></p> <p>Volle Sperrfähigkeit bei 120° mit 50 Hz</p> <p>Hohe Stoßströme und niedrige Wärme-widerstände durch NTV-Verbindung zwischen Silizium und Mo-Trägerscheibe.</p> <p>Elektroaktive Passivierung durch a - C:H</p>	<p><b>Phase Control Thyristor, light triggered with integrated overvoltage protection</b></p> <p>Full blocking capability at 120°C with 50 Hz</p> <p>High surge currents and low thermal resistance by using low temperature-connection NTV between silicon wafer and molybdenum.</p> <p>Electroactive passivation by a - C:H</p>																																											
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<p><b>Elektrische Eigenschaften / Electrical properties</b></p> <p>Höchstzulässige Werte / Maximum rated values</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width: 45%;"></th> <th style="width: 15%;"></th> <th style="width: 10%;"></th> <th style="width: 15%;"></th> <th style="width: 15%;"></th> </tr> </thead> <tbody> <tr> <td>Periodische Rückwärts-Sperrspannung repetitive peak reverse voltage</td> <td>F = 50 Hz</td> <td>V<sub>RRM</sub></td> <td>T<sub>vj min</sub> = -40°C 7000</td> <td>T<sub>vj min</sub> = 0°C 7200</td> </tr> <tr> <td>Durchlaßstrom-Grenzeffektivwert RMS forward current</td> <td></td> <td>I<sub>FRMSM</sub></td> <td></td> <td>1200 A</td> </tr> <tr> <td>Dauergrenzstrom mean forward current</td> <td>T<sub>C</sub> = 85°C, f = 50Hz T<sub>C</sub> = 60°C, f = 50Hz</td> <td>I<sub>FAVM</sub></td> <td></td> <td>550 A 765 A</td> </tr> <tr> <td>Stoßstrom-Grenzwert surge forward current</td> <td>T<sub>vj</sub> = 25°C, t<sub>p</sub> = 10ms T<sub>vj</sub> = T<sub>vj max</sub>, t<sub>p</sub> = 10ms</td> <td>I<sub>FSM</sub></td> <td></td> <td>12.1 kA 11.7 kA</td> </tr> <tr> <td>Grenzlastintegral I<sup>2</sup>t-value</td> <td>T<sub>vj</sub> = 25°C, t<sub>p</sub> = 10ms T<sub>vj</sub> = T<sub>vj max</sub>, t<sub>p</sub> = 10ms</td> <td>I<sup>2</sup>t</td> <td></td> <td>732 · 10<sup>3</sup> A<sup>2</sup>s 684 · 10<sup>3</sup> A<sup>2</sup>s</td> </tr> <tr> <td>Kritische Stromsteilheit, periodisch critical rate of rise of on-state current, periodical</td> <td>DIN IEC 747-6 V<sub>D</sub> ≤ V<sub>BO</sub>, f = 50Hz, P<sub>I</sub> = 40mW, t<sub>rise</sub> = 0,5µs</td> <td>(di/dt)<sub>cr</sub></td> <td></td> <td>300 A/µs</td> </tr> <tr> <td>Kritische Stromsteilheit, nicht-periodisch critical rate of rise of on-state current, non-periodical</td> <td>DIN IEC 747-6 V<sub>D</sub> ≤ V<sub>BO</sub>, P<sub>I</sub> = 40mW, t<sub>rise</sub> = 0,5µs</td> <td>(di/dt)<sub>cr</sub></td> <td></td> <td>1000 A/µs</td> </tr> <tr> <td>Kritische Spannungssteilheit critical rate of rise of off-state voltage</td> <td>T<sub>vj</sub> = T<sub>vj max</sub>, V<sub>DM</sub> = 4,3kV</td> <td>(dv/dt)<sub>cr</sub></td> <td></td> <td>2000 V/µs</td> </tr> </tbody> </table>										Periodische Rückwärts-Sperrspannung repetitive peak reverse voltage	F = 50 Hz	V <sub>RRM</sub>	T <sub>vj min</sub> = -40°C 7000	T <sub>vj min</sub> = 0°C 7200	Durchlaßstrom-Grenzeffektivwert RMS forward current		I <sub>FRMSM</sub>		1200 A	Dauergrenzstrom mean forward current	T <sub>C</sub> = 85°C, f = 50Hz T <sub>C</sub> = 60°C, f = 50Hz	I <sub>FAVM</sub>		550 A 765 A	Stoßstrom-Grenzwert surge forward current	T <sub>vj</sub> = 25°C, t <sub>p</sub> = 10ms T <sub>vj</sub> = T <sub>vj max</sub> , t <sub>p</sub> = 10ms	I <sub>FSM</sub>		12.1 kA 11.7 kA	Grenzlastintegral I <sup>2</sup> t-value	T <sub>vj</sub> = 25°C, t <sub>p</sub> = 10ms T <sub>vj</sub> = T <sub>vj max</sub> , t <sub>p</sub> = 10ms	I <sup>2</sup> t		732 · 10 <sup>3</sup> A <sup>2</sup> s 684 · 10 <sup>3</sup> A <sup>2</sup> s	Kritische Stromsteilheit, periodisch critical rate of rise of on-state current, periodical	DIN IEC 747-6 V <sub>D</sub> ≤ V <sub>BO</sub> , f = 50Hz, P <sub>I</sub> = 40mW, t <sub>rise</sub> = 0,5µs	(di/dt) <sub>cr</sub>		300 A/µs	Kritische Stromsteilheit, nicht-periodisch critical rate of rise of on-state current, non-periodical	DIN IEC 747-6 V <sub>D</sub> ≤ V <sub>BO</sub> , P <sub>I</sub> = 40mW, t <sub>rise</sub> = 0,5µs	(di/dt) <sub>cr</sub>		1000 A/µs	Kritische Spannungssteilheit critical rate of rise of off-state voltage	T <sub>vj</sub> = T <sub>vj max</sub> , V <sub>DM</sub> = 4,3kV	(dv/dt) <sub>cr</sub>		2000 V/µs
Periodische Rückwärts-Sperrspannung repetitive peak reverse voltage	F = 50 Hz	V <sub>RRM</sub>	T <sub>vj min</sub> = -40°C 7000	T <sub>vj min</sub> = 0°C 7200																																													
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BIP AC / SM PB, 2002-05-23, Przybilla J. / Keller <span style="float: right;">Release 6 <span style="margin-left: 100px;">Seite/page 1</span></span>																																																	

# Technische Information / Technical Information

**eupec**

Lichtzündbarer Netzthyristor  
mit integriertem Überspannungsschutz

**T 553 N 70 TOH**

Light Triggered Phase Control Thyristor  
with integrated overvoltage protection

**N**



## Charakteristische Werte / Characteristic values

Schutzzündspannung (statisch) protective break over voltage	$T_{vj} = 0^{\circ}\text{C} \dots T_{vj\text{max}}$	$V_{BO}$	min. 6500	V
Durchlaßspannung on-state voltage	$T_{vj} = T_{vj\text{max}}, I_T = 1\text{ kA}$	$V_T$	typ. 2,55 max. 2,65	V
Schleusenspannung / threshold voltage Ersatzwiderstand / slope resistance	$T_{vj} = T_{vj\text{max}}$	$V_{TO}$ $r_T$	typ. 1,25 max. 1,3 1,3 1,35	V mΩ
Durchlaßrechenkennlinie on-state characteristics for calculations $V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$	$T_{vj} = T_{vj\text{max}}$	A B C D	typ. -0,0927 max. -0,0921 0,000967 0,001 0,1815 0,1841 0,01334 0,0149	
erforderliche Zündlichtleistung required gate trigger light power	$T_{vj} = 25^{\circ}\text{C}, V_D = 100\text{V}$	$P_{LM}$	min 40	mW
Haltestrom holding current	$T_{vj} = 25^{\circ}\text{C}$	$I_H$	100	mA
Einraststrom latching current	$T_{vj} = 25^{\circ}\text{C}, V_D = 100\text{V},$ $P_{LM} = 40\text{mW}, t_{on} = 0,5\mu\text{s}$	$I_L$	1	A
Rückwärts-Sperstrom reverse current	$T_{vj} = T_{vj\text{max}}$ $V_R = 7000\text{V}$	$i_R$	200	mA
Zündverzug gate controlled delay time	$T_{vj} = 25^{\circ}\text{C}, V_D = 1000\text{V},$ $P_{LM} = 40\text{mW}, t_{on} = 0,5\mu\text{s}$	$t_{gd}$	typ. 5	μs
Freiwerdezeit circuit commutated turn-off time	$T_{vj} = T_{vj\text{max}}, I_{TM} = I_{TAVM}$ $V_{RM} = 100\text{V}, V_{DM} = 0,67 \cdot V_{DRM}$ $dV_D/dt = 20\text{V}/\mu\text{s}, -di_T/dt = 10\text{A}/\mu\text{s}$ 4. Kennbuchstabe / 4 <sup>th</sup> letter O	$t_q$	typ. 650	μs
Sperrverzögerungsladung recovered charge	$T_{vj} = T_{vj\text{max}}$ $I_{TM} = 1000\text{A}, di/dt = 10\text{A}/\mu\text{s}$ $V_R = 0,5 \cdot V_{RRM}, V_{RM} = 0,8 \cdot V_{RRM}$	$Q_r$	7,2	mAs
Rückstromspitze peak reverse recovery current	$T_{vj} = T_{vj\text{max}}$ $I_{TM} = 1000\text{A}, di/dt = 10\text{A}/\mu\text{s}$ $V_R = 0,5 \cdot V_{RRM}, V_{RM} = 0,8 \cdot V_{RRM}$	$I_{RM}$	210	A

# Technische Information / Technical Information

**eupec**

Lichtzündbarer Netzthyristor  
mit integriertem Überspannungsschutz

**T 553 N 70 TOH**

Light Triggered Phase Control Thyristor  
with integrated overvoltage protection

**N**



## Thermische Eigenschaften / Thermal properties

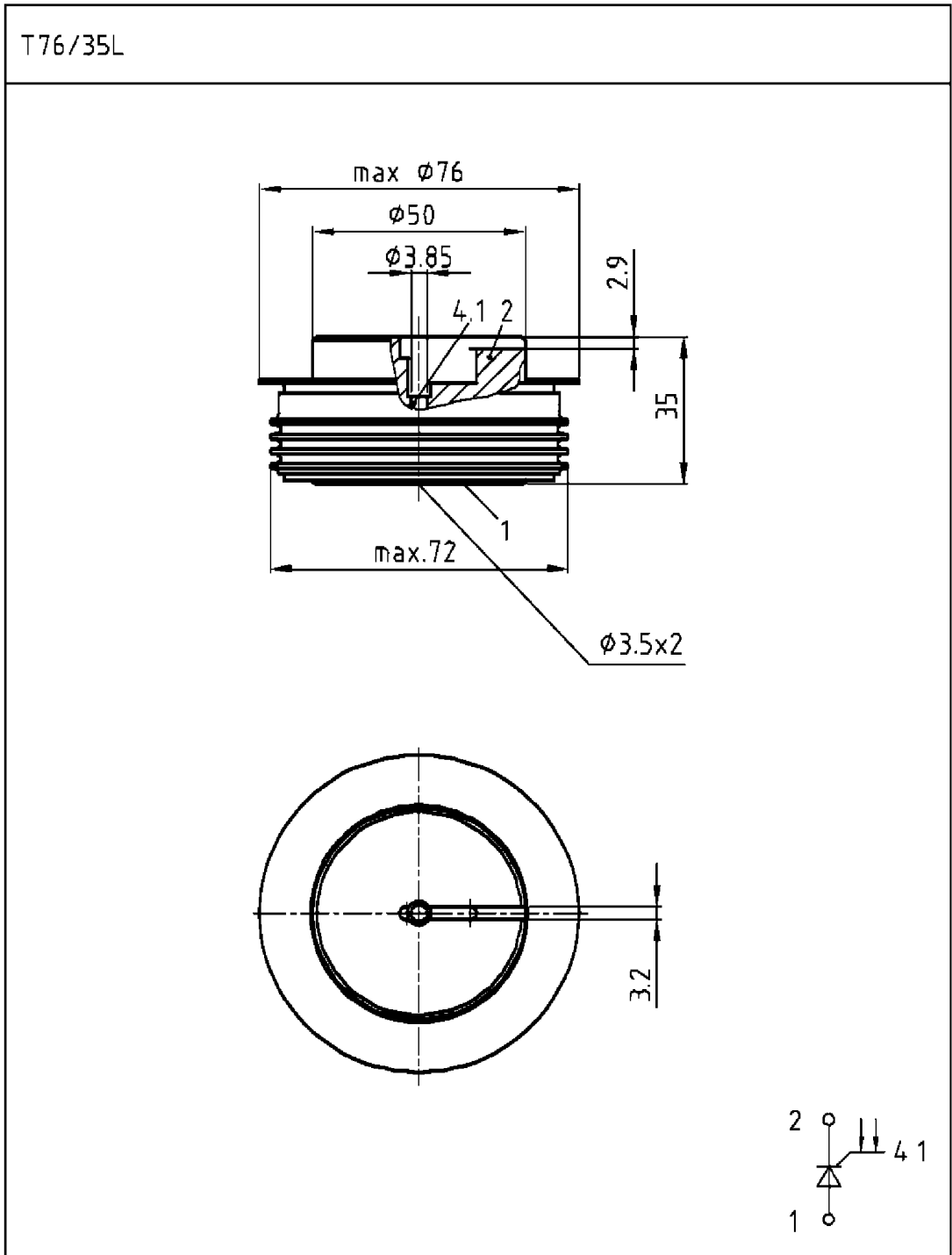
Innerer Wärmewiderstand thermal resistance, junction to case	beidseitig / two-sided, $\Theta = 180^\circ \sin$	$R_{thJC}$	0,0200	$^\circ\text{C/W}$
	beidseitig / two-sided, DC		0,0190	$^\circ\text{C/W}$
	Anode / anode DC		0,0305	$^\circ\text{C/W}$
	Kathode / cathode DC		0,0500	$^\circ\text{C/W}$
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	beidseitig / two-sided	$R_{thCH}$	0,005	$^\circ\text{C/W}$
	einseitig / single-sided		0,010	$^\circ\text{C/W}$
Höchstzulässige Sperrschichttemperatur max. junction temperature		$T_{vj \max}$	+120	$^\circ\text{C}$
Betriebstemperatur operating temperature		$T_{c \text{ op}}$	-40...+120	$^\circ\text{C}$
Lagertemperatur storage temperature		$T_{stg}$	-40...+150	$^\circ\text{C}$

## Mechanische Eigenschaften / Mechanical properties

Gehäuse, siehe Anlage case, see appendix			Seite 4	
Si-Element mit Druckkontakt, Lichtzündung Si-pellet with pressure contact, light triggered	Silizium Tablette silicon wafer		55LTN70	
Anpreßkraft clamp force		F	15...24	kN
Gewicht weight		G	typ 650	g
Kriechstrecke creepage distance			25	mm
Feuchteklasse humidity classification	DIN 40040		C	
Schwingfestigkeit vibration resistance	f = 50Hz		50	$\text{m/s}^2$

Mit dieser technischen Information werden Halbleiterbauelemente spezifiziert, jedoch keine Eigenschaften zugesichert. Sie gilt in Verbindung mit den zugehörigen technischen Erläuterungen.  
This technical information specifies semiconductor devices but promises no characteristics. It is valid in combination with the belonging technical notes.

# Maßbild / Outline



Lichtzündbarer Netzthyristor  
mit integriertem Überspannungsschutz

T 553 N 70 TOH

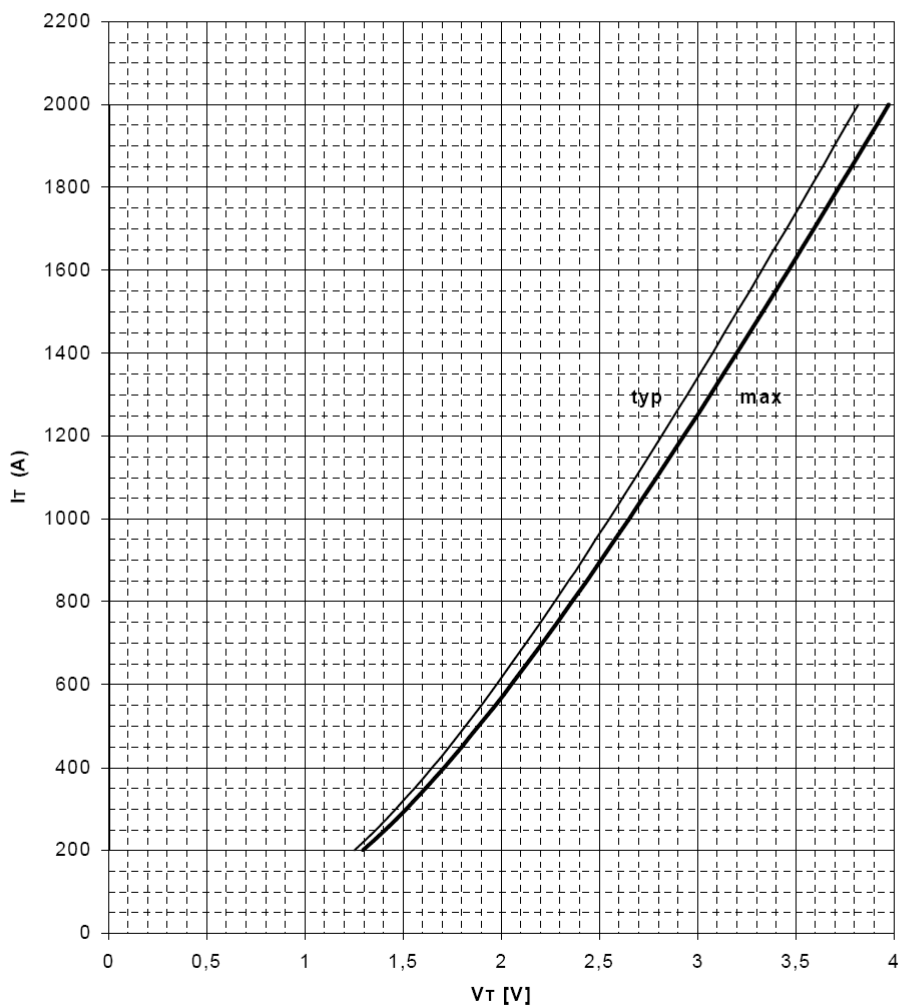
Light Triggered Phase Control Thyristor  
with integrated overvoltage protection

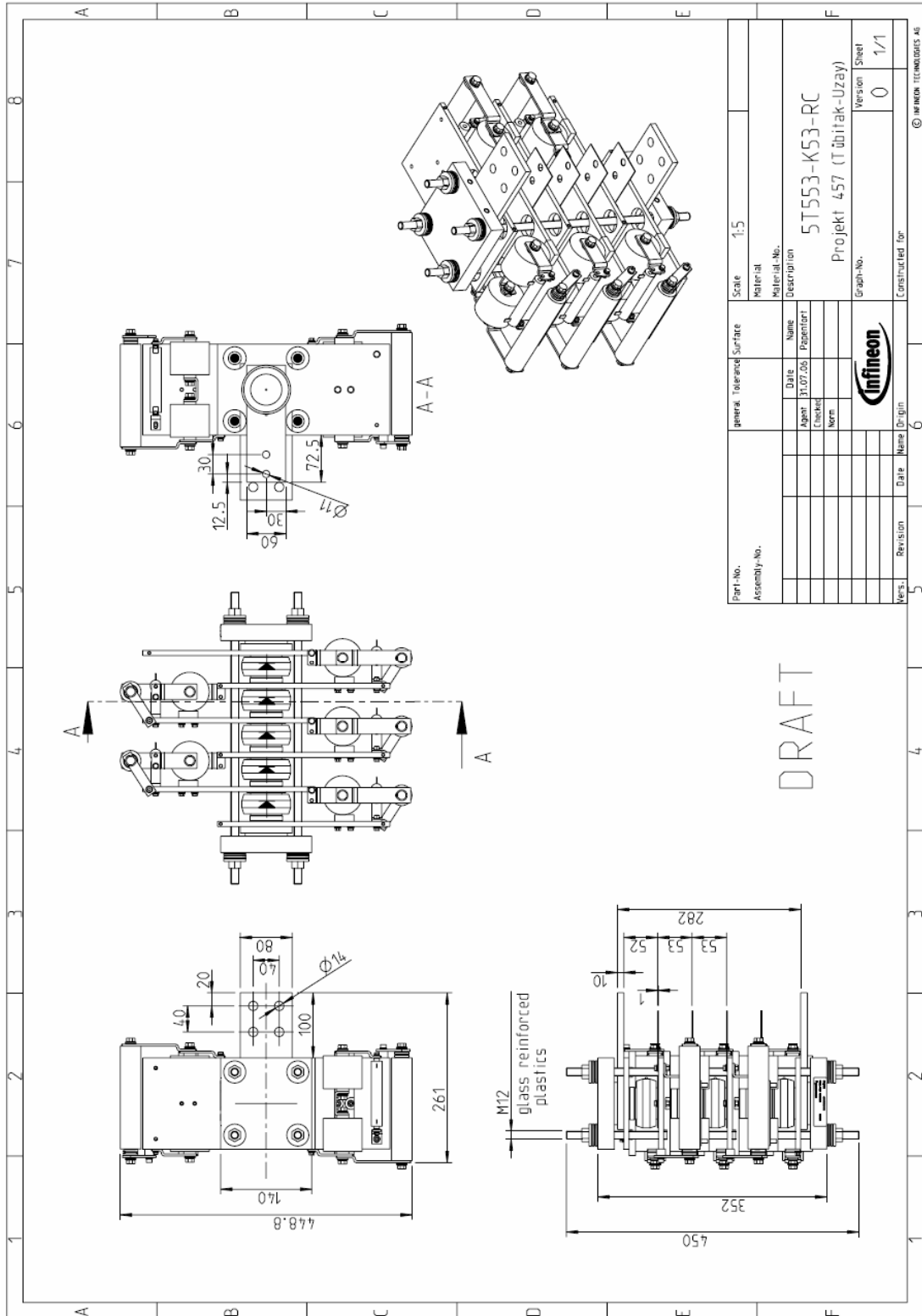
N



**Durchlaßkennlinien  $i_T = f(v_T)$**   
Limiting and typical on-state characteristic

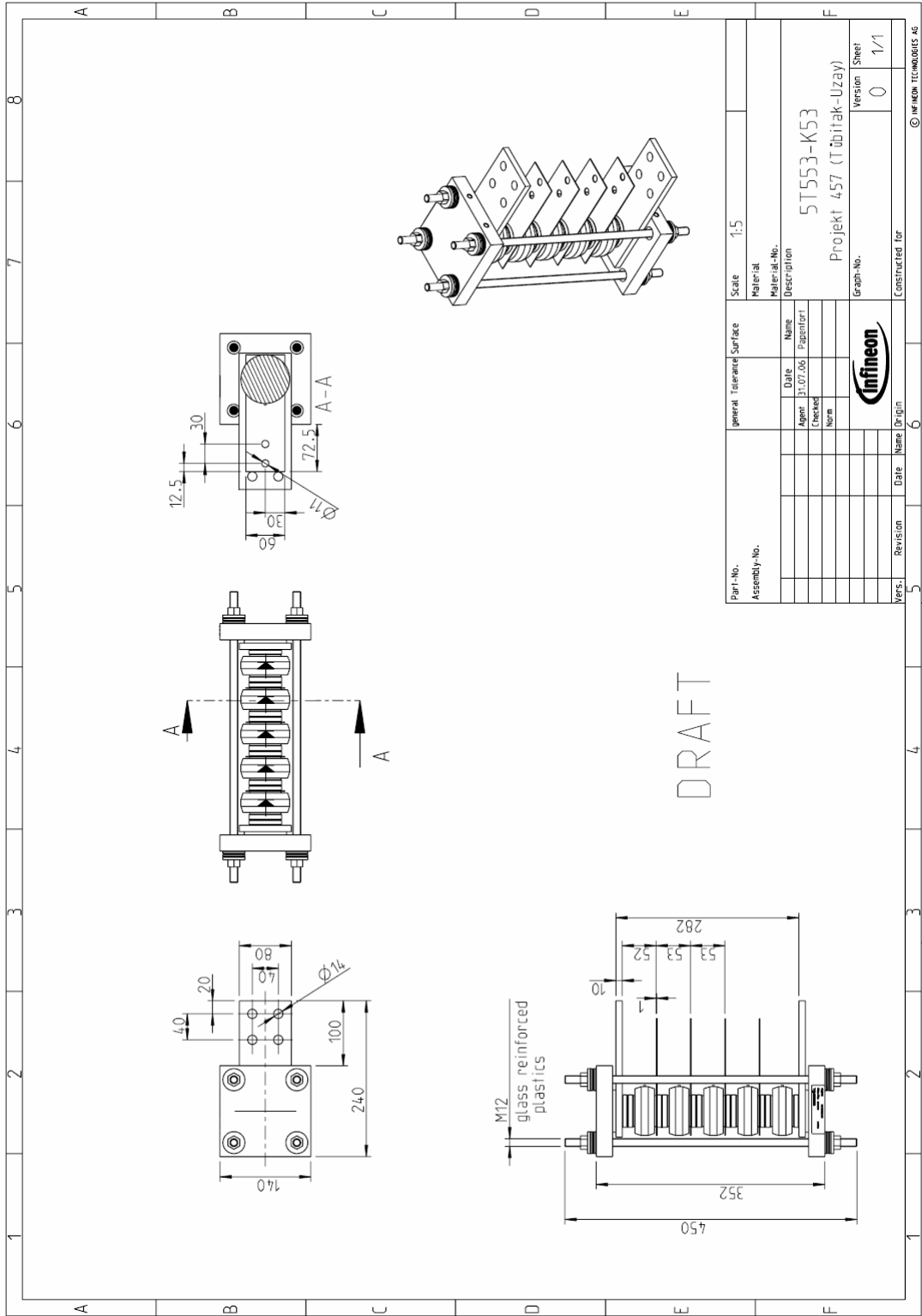
$T_{vj} = 120^\circ\text{C}$





Part-No. Assembly-No.	Scale	1:5
Material	Material-No.	5T553-K53-RC
Description	Description	Projekt 457 (Tübitak-Uzay)
Author	Date	31.07.05
Checked	Name	Papierfort
None	Version	0
None	Sheet	1/1
None	Graph-No.	
None	Constructed for	
None	Version	0
None	Date	
None	Name	
None	Origin	





## APPENDIX – D

### LFTD TECHNICAL DOCUMENTS



LFTD18P-LRM

#### 1 Safety precautions

### Caution!

Driver operates with class 4b laser! Laser light is invisible and has very high energy. Eye contact can cause serious, irreversible injuries.

!

Driver must only be installed from trained personnel.

!

Unused laser diodes must be covered. Rubber covers do not block the laser light completely.

!

Laser diodes not used during operation must be covered with metal cover. Proper covers can be supplied on request.

!

Remove diode cover only when connecting the fiber optic to the thyristor.

!

Correct transport, storage, installation and operation are important for proper function of the module.

!

Protect the module against shock and vibrations during transport. Water and extreme temperatures can damage the module.

!

Service and maintenance operations require proper ESD protection. At least the metal housing of the switch gear cabinet and the service personnel must be connected to ground potential by a ESD wrist band.

!

If the fiber optic is removed, the receiving diode must be protected with a cover in order to avoid uncontrolled triggering of the thyristor (e.g. camera flash light).





#### **4 General advice**

The technical documentation LFTD18P, project Padua contains the description of the module LFTD18P and all options and settings necessary for the operation of the module. It describes the function of the module. All explanations and descriptions are based on the circuit diagram revision date 25/11/2001.

This document replaces all previous documents describing the LFTD18P, project Padua.

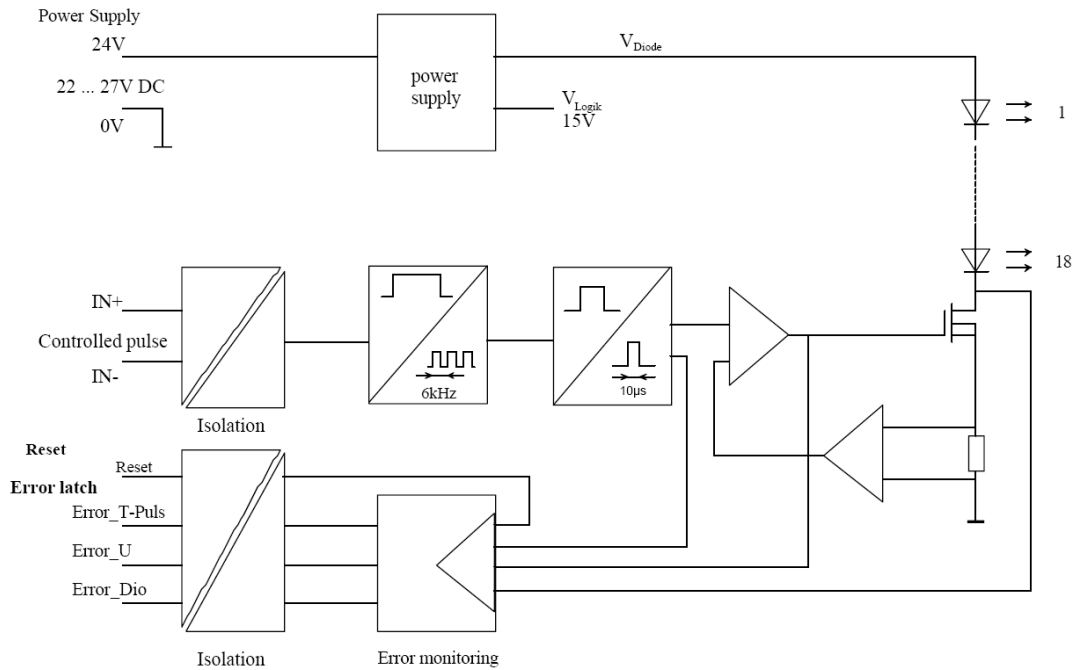
#### **5 Brief description of the module**

The module generates laser impulses for the control of light triggered thyristors. Applying a signal to the input generates a series of trigger impulses at the power outputs. The current flowing through the laser diode is controlled to 0.8 A by the power supply (power transistors with current control). Failure of the current control or the laser diode activates the error signal of the driver (see 7.7.1).

Supply voltage (15 V, 5 V) for the control unit and driver are provided by an internal switch mode power supply.

Up to 18 laser diodes (respectively 18 thyristors) can be triggered simultaneously. For the Padua project the modules are equipped with a varying number of laser diodes (n=4; 6; 8 and 12). The mother board contains 3 power transistors for driving the laser diodes and the receiving unit. Each power transistor has its own current control and all are triggered simultaneously. Diode modules plugged into the mother board contain the laser diodes. Each diode module contains a maximum of 6 laser diodes. Each diode module is controlled by a separate power transistor. Control errors (e.g. current value too small or too large) are displayed and memorized.

Operation of the module with control error will effect the expected lifetime of the module. The lifetime will be reduced significantly. Immediate shut-down of the system will be necessary. Application 1 shows the block diagram of the LFTD18P module.



Application 1: Block circuit diagram

## 6 Name and type code

	LFTD18P	-XXXX / XX
Light Fired Thyristor Driver	LFTD	
Max. number of thyristors (18)	18	
Stage of development	P -	
Fiber optic trigger input	L	
Opto-coupler trigger input	O	
External reset	R	
Auto reset	A	
Multi-impulse trigger	M	
Single-impulse trigger	S	
Fiber optic collective error message	S	
Number of laser diodes (e.g. 12)		/12



## 7 In- and output parameter

### 7.1 Supply voltage and current

Symbol	Unit	Value
$U_{in\_nenn}$	V	24 +/-5%
$I_{in\_nenn}$	A	0,5

**Table 1: Supply voltage and current**

The power supply must be capable to supply a current of 3 A immediately during turn-on.

Type	Terminal	Description
24V_in	VG32B A28, C28	24V-power supply +
0V	VG32B A30, C30	24V-power supply GND
PE	VG32B A32, C32	Safety contact

**Table 2: Terminal arrangement power supply of trigger module**

### 7.2 Input signal

The input requires a optical signal.

#### 7.2.1 Fiber optic input signal

For the fiber optic input the interface the coupler series type HFBRx528 are used (sender: HFBR1528, receiver: HFBR2528). Minimum required pulse width is 20  $\mu$ s. Controlling the module with fiber optic the specifications and recommendations of Fa. Agilent must be followed.



Symbol/ component	Unit	Value
Receiver		HFBR2528 (Agilent)
recommended sender		HFBR1528
$t_{on\_min}$	$\mu s$	20
$t_{delay}^{* 1)}$	$\mu s$	<2

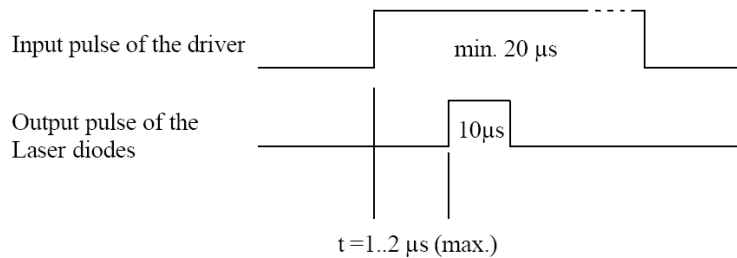
**Table 3: Data for input signal via fiber optic**

\* 1)  $t_{delay}$  : input signal trough receiver HFBR1528 (recommended Agilent circuit) until output of the laser light trigger impulse to the thyristor (Application 2).

### 7.3 Impulse processing

The LFTD18P-LRM converts the input impulse to a pulse packet. Delay time is in the order of 1 – 2  $\mu s$  (Application 2).

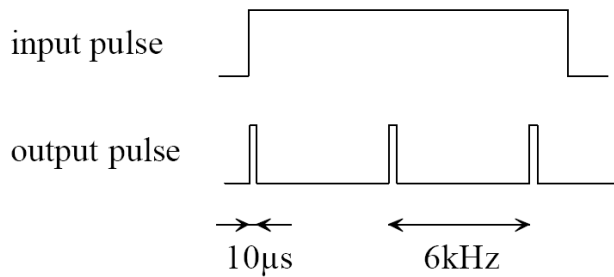
Time behaviour



#### Application 2: Delay time

##### 7.3.1 Pulse packet

The driver LFTD18P-LRM generates a pulse packet with the time length of the input signal. Repetition rate of the 10  $\mu s$  wide impulses is 6 kHz  $\pm$  5 %. If the pulse width of the input pulse is less then 1/6 kHz a single impulse is generated.



**Application 3: Pulse packet**

**7.4 Output signal**

For triggering the thyristor the laser diode transmits 10 µs wide light impulses with a wave length of 904 nm.

**Caution!**

Driver operates with class 4b laser! Laser light is invisible and has very high energy. Eye contact can cause serious, irreversible injuries.

Symbol/ component	Unit	Value
$T_{puls\_out}$	µs	10
$I_{puls}$	mA	800
Laser diode		SPL PL90 (Osram)
$n_{max\_Thyristor}$ *1)		18

**Table 4: Data of the output pulse**

\*1)  $n_{max\_Thyristor}$ : max. number of simultaneous triggered thyristors

**7.5 Temperature range**

0 ... 70 °C

**7.6 Dimensions of the trigger unit**

19" plug-in, 160 x 100 x T (length x width x depth)

The height of the module depends on the number of laser diodes used.



$n_{\text{Laserdiode}}$	T/mm
1..6	40
7..12	60
13..18	80

**Table 5: Height depending on number of laser diodes**

## 7.7 Error messages

Three error messages are generated and are available at the terminal. In addition a optic collective error message and a trigger signal for the thyristor are displayed on the front panel. All error messages are stored in a flip flop.

### 7.7.1 Error messages (under voltage, pulse error and diode error)

The connections at the terminal are the output of the output opto coupler (emitter and collector). They are connected with suppresser diodes and capacitors to the 0 V potential of the supplying 24 V power supply. Emitter and collector are connected separately and can be used for open-emitter or open-collector circuit. Pull-up and pull-down resistors are required. Activated the internal resistance of the error signal is approximately 110 Ohm. High currents trough the transistor can simulate an error for following units. Currents higher then 20 mA can destroy the output transistor. The output is not suitable for driving inductive loads.

#### 7.7.1.1 Under voltage error U\_error

Monitored are the supply voltage for the laser diodes and the internal supply voltage for the logic components. Failure of a voltage will cause the output to become high resistive, the transistor blocks.

All voltages correct: transistor is turned on

Voltage off limit: transistor is high resistive

The error message is activated without delay as soon as a voltage fails. No other event can activate the error message.

#### 7.7.1.2 Pulse error T\_Pulse\_error

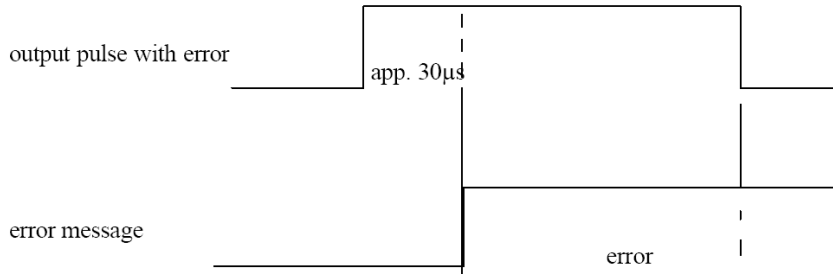
Monitored are the length of the control impulses of the diodes. If the output impulse is longer then 30  $\mu$ s the signal is activated and the output becomes high resistive.

Length of impulse correct: transistor is turned on

Impulse to long: transistor is high resistive



7.7.1.2.1 Time behaviour



**Application 4: Time behaviour of T\_Puls\_Error**

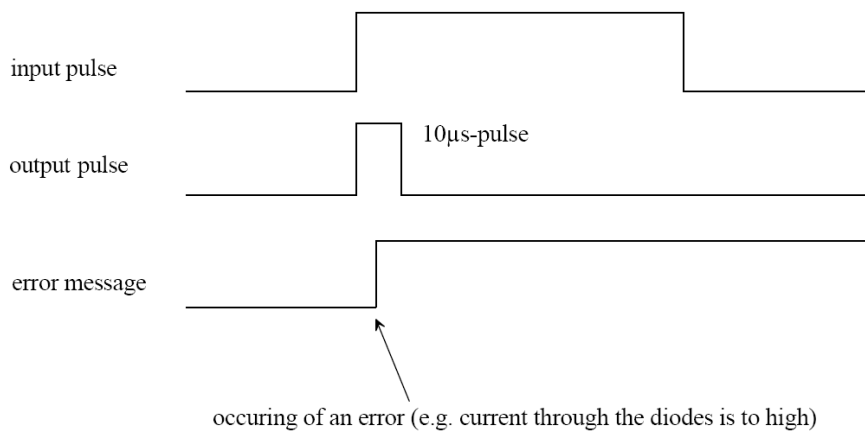
7.7.1.3 **Diode error Diode\_error**

Diode error monitors internal errors in the trigger unit. It is activated if the current control fails, the diode supply voltage is too high, a diode failed or the corresponding thyristor is turned on by the over voltage protection.

Error occurred: transistor is turned on

No error occurred: transistor is high resistive

7.7.1.3.1 Time behavior



**Application 5: Time behaviour Diode\_error**



**7.7.1.4 0V**

Reference potential for power supply. Output signals are protected by suppresser diodes against 0V.

**7.7.1.5 Terminal arrangement**

error type	description	terminal	description
U_Error	under voltage	VG32B C6	output opto coupler collector
U_Error_E		VG32B A6	output opto coupler emitter
Puls_Error	pulse error	VG32B C8	output opto coupler collector
Puls_Error		VG32B A8	output opto coupler emitter
Diode_Error	diode error	VG32B C10	output opto coupler collector
Diode_Error_E		VG32B A10	output opto coupler emitter
0V	24 V potential reference	VG32B A14, C14	

**Table 6: Terminal arrangement for error messages**

**7.7.1.6 Recommended output circuit for open collector circuit**

The output can be operated in open collector or open emitter circuit. Series connection of two 60 Ohm resistors protects the opto coupler. Reference for the output is always 0 V.

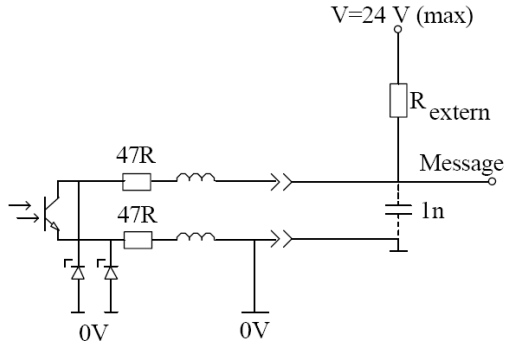
Maximum output current is 25 mA.

The low level of the output is 4 V at maximum message output current. It is recommended to rate to external resistor in achieve to the required low level voltage.

Calculations for a open emitter circuit are accordingly.



recommended output circuit:

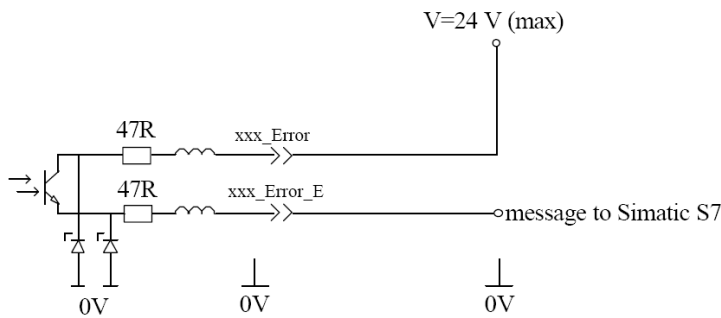


**Application 6: Recommended output circuit**

For noise suppression the capacitor can be used.

**7.7.1.7 Recommended output circuit for connection to PLC (SIMATIC S7 SM321)**

Typical value for the input current of the SIMATIC S7 SM321 is 7 mA. Current limitation is not required. Collector outputs are connected to 24 V and emitter outputs are connected directly to the SIMATIC S7.



**Application 7: Connecting to a PLC SIMATIC S7**

**7.7.2 Collective error**

In the event of an error the collective error is activated. It is displayed on the front panel of the module.

LED (green) illuminated                      no error

**7.7.3 Pulse LED**

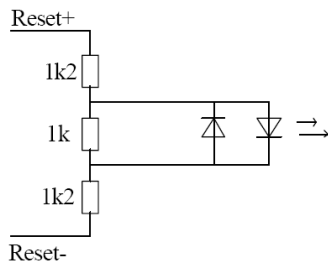
Next to the collective error LED is the pulse LED. It signals the trigger signal for the thyristor with a short flash. To visualize the trigger signal the trigger impulse duration is expanded. Because the thyristors are triggered with a pulse packet the length of the flash is equivalent to the input pulse of the LFTD18P-LRM/xx.

## 7.8 Error control and reset

All errors are memorized and displayed by the driver. Occurrence of an error does not block the thyristor driver. The error is only visualized and must be evaluated by the control system. After completion of the task the driver is deactivated. Contact the manufacturer if errors occur repeatedly.

### 7.8.1 Reset

The error memory can be reset with a electrical impulse trough the terminal (VG32B A4/C4). Application 8 illustrates the opto coupler of the reset input.



**Application 8: Circuit of reset input**

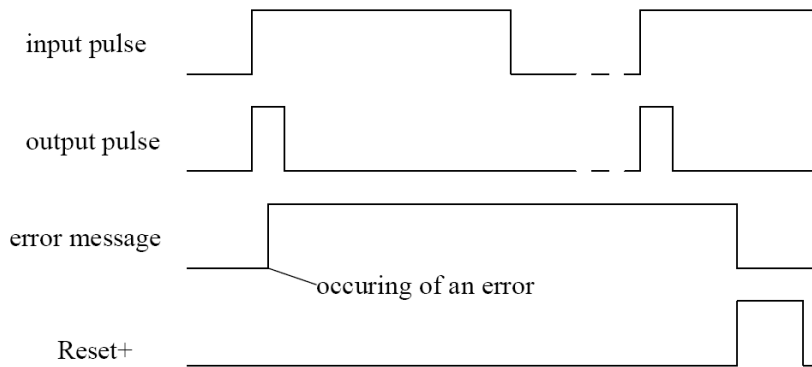
Description	Terminal	Remark
Reset+	VG32B C4	anode input opto coupler
Reset-	VG32B A4	cathode input opto coupler

**Table 7: Terminal arrangement for Reset**

### 7.8.2 Error message, reset trough terminal

If an error occurs it is displayed and memorized. The signal for the trigger diode is not disabled. Only a positive pulse on terminal VG32B C4 against A4 resets the memory. The output is not blocked.

*All errors displayed **do not** lead to deactivation of the module. They are only meant for monitoring. The decision about deactivation of the module is with the control system or instructed personnel. Deactivation is strictly recommended in case of an error. Occurrence of errors during operation requires inspection and/ or repair.*



Application 9: Error message and reset

## 8 Error and error correction

Error	cause	correction
Uok_out	supply voltage to low or off limit internal voltage supply defect	control 24 V supply voltage send module in for repair
Tpuls_out	internal pulse generator defect	send module in for repair
Error_out	input voltage to low laser diode or electronic part defect	control 24 V supply voltage send module in for repair
Pulse-LED does not lit up	clock voltage to low	increase voltage level
Pulse-LED is lit continuously	clock frequency to high for single impulse or continuous input signal	correct frequency check input pulse
driver signals error after turn on, but functions correct after reset	power of power supply to low	increase supply power
self configured driver signals error with input signal	error signal from unused channels is not suppressed	set jumper

Table 8: Possible errors

## APPENDIX – E

### PIC CODE WRITTEN IN CCS

```
1 #include<16F628A.h>
2 #include<stdio.h>
3
4 #FUSES NOWDT // No Watch Dog Timer
5 #FUSES HS // High speed Osc (> 4mhz)
6 #FUSES PUT // Power Up Timer
7 #FUSES NOPROTECT // Code not protected from reading
8 #FUSES NOBROWNOUT // No brownout reset
9 #FUSES NOMCLR // Master Clear pin used for I/O
10 #FUSES NOLVP // No low voltage prgming, B3(PIC16)or B5(PIC18)
11 // used for I/O
12 #FUSES NOCPD // No EE protection
13
14 #use delay(clock=2000000)
15
16 #define TRIGGEROUT2 PIN_A0
17 #define NTCOUT PIN_A1
18 #define TRIGGEROUT PIN_A2
19 #define CURRENTFAULTOUT PIN_A3
20 #define CT3UP PIN_A4
21 #define CT3DOWN PIN_A5
22 #define RESETER PIN_B0
23 #define BREAKER PIN_B1
24 #define LFTDOUT PIN_B2
25 #define CT2DOWN PIN_B3
26 #define TEST PIN_B4
27 #define NICTRIG PIN_B5
28 #define CT2UP PIN_B6
29 #define LFTDIN PIN_B7
30
31 int8 time1a=0; // Used for detection of timer overflow in "termination"
32 int8 time1b=0; // Used for detection of timer overflow in "termination"
33 int8 time2a=0; // Used for detection of timer overflow in "no_current2"
34 int8 time2b=0; // Used for detection of timer overflow in "no_current2"
35 int16 time2c=0; // Used for detection of 1.5msec duration in "high_current2"
36 int16 time2d=0; // Used for detection of 1.5msec duration in "high_current2"
37 int8 time3a=0; // Used for detection of timer overflow in "no_current3"
38 int8 time3b=0; // Used for detection of timer overflow in "no_current2"
39 int16 time3c=0; // Used for detection of 1.5msec duration in "high_current3"
40 int16 time3d=0; // Used for detection of 1.5msec duration in "high_current3"
41 int1 lan1=0; // Used for entering only once to triggering start part.
42 int16 counter1=0; // Used as a counter in "termination"
43 int16 counter2a=0; // Used as a counter in "no_current2"
44 int16 counter3a=0; // Used as a counter in "no_current3"
45
46 int16 sayac1=150; // Used as the counter limit in "termination"
```

```

47 int8 sayac2a=5; // Used as the counter limit in "no_current2"
48 int8 sayac3a=5; // Used as the counter limit in "no_current3"
49
50 int8 sayac4=59; // Used as a counter for detecting whether CT2UP, CT3UP
51 // and TEST pins stay LOW for a period of 1.5 msec.
52
53 int1 status=0; // Used for recalling the status of filter CB position.
54 // (ON = HIGH, OFF = LOW)
55 int1 ates=0; // Used for recalling whether there is a triggering
56 // or not at the moment.
57 // (HIGH = triggering exists, LOW = no triggering)
58
59 int1 hata=0; // Used for recalling whether there exists a fault.
60 // (HIGH = there is a fault, LOW = no fault)
61 int1 cok2=0; // Used for recalling the status of
62 // high current fault of current transformer 2. (RD)
63 int1 cok3=0; // Used for recalling the status of
64 // high current fault of current transformer 3. (RTS)
65
66 int1 say=0;
67 int8 ates_time1=0;
68 int8 ates_time2=0;
69 int16 ates_counter=0;
70 int16 ates1=0;
71 int16 ates2=0;
72 int16 ates3=0;
73 int16 ates_yok=0;
74 int8 adet=0;
75 int1 counter_tut=0;
76
77
78 void termination() // This function stops the triggering
79 // after 3 seconds have passed.
80 {
81     time1b=time1a;
82     time1a=get_timer0(); // The PIC timer is recorded.
83
84     if (time1b>time1a)
85     {
86         counter1=counter1+1; // The number of timer overflows are counted.
87     }
88
89     if (counter1==sayac1) // The triggering will be terminated
90     // iff 3 seconds have passed.
91     {
92         output_low(TRIGGEROUT2);
93         output_low(TRIGGEROUT);
94         counter1=0; // The counter is made ready for another termination.
95         ates=0; // The triggering status is set to No triggering.
96         cok2=0;
97         cok3=0;
98     }
99 }
100
101 void temperature_fault() // This function will be used in the future
102 // if a temperature sensor can be installed
103 // on either the LTTs or the resistors.
104 {
105     if (input(NTCTRIG))
106     {
107         output_high(NTCOUT); // The high temperature warning output signal
108 // will be sent, and the filter CB will be
109         hata=1; // opened by PLC. Fault status is set to HIGH.
110     }
111 }
112
113
114 void LFTD_fault() // This functions follows the state

```

```

115 // of the LFTDs. If LFTDIN pin is HIGH,
116 {
117     if (input(LFTDIN)) // that means there exists a fault in at least
118     { // one of the LFTDs.so LFTD fault output signal
119         output_high(LFTDOUT); // will be sent and the filter CB will be
120         hata=1; // opened by PLC. Fault status is set to HIGH.
121     }
122 }
123
124 void no_current2() // If during triggering, the current through
125 // at least one of RDs is below
126 { // the bottom threshold for a duration of
127 // at least 25 msec (CT2DOWN is LOW)
128     time2b=time2a; // this is a fault. (RD is not connected or
129 // the current can not be measured.)
130     time2a=get_timer0();
131
132     if (time2b>time2a) // Number of PIC timer overflows are counted.
133     {
134         if (input(CT2DOWN))
135         {
136             counter2a=counter2a+1;
137         }
138         else
139         {
140             counter2a=0;
141         }
142     }
143     if (counter2a==sayac2a) // If the counter limit is reached
144     {
145         output_high(CURRENTFAULTOUT); // CURRENTFAULTOUT fault output signal
146         // will be sent and the
147         hata=1; // filter CB will be opened by PLC.
148         // Fault status is set to HIGH.
149     }
150 }
151
152 void no_current3() // If during triggering, the current through
153 // at least one of RTSs is below the bottom
154 { // threshold for a duration of at least
155 // 25 msec (CT3DOWN is LOW)
156     time3b=time3a; // this is a fault. (RTS is not connected or
157 // the current can not be measured.)
158     time3a=get_timer0();
159
160     if (time3b>time3a) // Number of PIC timer overflows are counted.
161     {
162         if (input(CT3DOWN))
163         {
164             counter3a=counter3a+1;
165         }
166         else
167         {
168             counter3a=0;
169         }
170     }
171     if (counter3a==sayac3a) // If the counter limit is reached
172     {
173     {
174         output_high(CURRENTFAULTOUT); // CURRENTFAULTOUT fault output signal
175         // will be sent and the
176         hata=1; // filter CB will be opened by PLC.
177         // Fault status is set to HIGH.
178     }
179     }
180
181 void high_current2() // If 100msec has passed from the start of
182 // triggering and the current through
183 { // at least one of RDs is above the

```

```

184 // top threshold for at least 1.5 msec
185 // (CT2UP is LOW) this is a fault.
186 // (there may be a short-circuit).
187
188 if (cok2==0)
189 {
190     time2c=get_timer0();
191     time2d=get_timer0();
192     cok2=1;
193 }
194
195 if (input(CT2UP))
196 {
197     time2d=get_timer0();
198 }
199 else
200 {
201     cok2=0;
202 }
203
204 if (time2d<time2c)
205 {
206     time2d = time2d + 255; // care taken for PIC timer overflow.
207 }
208 if ((time2d-time2c)==sayac4) // if CT2UP is LOW for at least 1.5 msec
209 {
210     output_high(CURRENTFAULTOUT); // CURRENTFAULTOUT fault output signal
211 // will be sent and the
212     hata=1; // filter CB will be opened by PLC.
213 // Fault status is set to HIGH.
214 }
215 }
216
217
218 void high_current3() // If there is no triggering and the
219 // current through at least one of RDs
220 // is above the top threshold for at least
221 // 1.5 msec (CT3UP is LOW) this is a fault.
222 // (there may be a short-circuit).
223 {
224     if (cok3==0)
225     {
226         time3c=get_timer0();
227         time3d=get_timer0();
228         cok3=1;
229     }
230     if (input(CT3UP))
231     {
232         time3d=get_timer0();
233     }
234     else
235     {
236         cok3=0;
237     }
238
239     if (time3d<time3c)
240     {
241         time3d = time3c + 255; // care taken for PIC timer overflow.
242     }
243     if ((time3d-time3c)==sayac4) // if CT3UP is LOW for at least 1.5 msec
244     {
245         output_high(CURRENTFAULTOUT); // CURRENTFAULTOUT fault output signal
246 // will be sent and the
247         hata=1; // filter CB will be opened by PLC.
248 // Fault status is set to HIGH.
249     }
250 }
251
252

```

```

253 void too_frequent() // This function detects whether there exists
254 // 3 consecutive triggerings in a
255 { // 3-minute period. If such a thing occurs,
256 // NTCOUT fault signal is sent to PLC
257 ates_time2=ates_time1; // and it opens the filter CB, in order to
258 // prevent high power loss stress on
259 ates_time1=get_timer0(); // both the resistors and the LTTs.
260
261 if (ates==1 && say==1)
262 {
263     say=0;
264     adet=adet+1;
265     counter_tut=1;
266     if (adet==5) adet=4;
267 }
268
269
270 if (ates_time2>ates_time1)
271 {
272     ates_counter=ates_counter+1;
273 }
274
275 if (counter_tut==1)
276 {
277     if (adet==1)
278     {
279         ates1=ates_counter;
280     }
281     if (adet==2)
282     {
283         ates2=ates_counter;
284     }
285     if (adet==3)
286     {
287         ates3=ates_counter;
288     }
289
290     if (adet==4)
291     {
292         ates1=ates2;
293         ates2=ates3;
294         ates3=ates_counter;
295     }
296     counter_tut=0;
297 }
298
299 if (ates==1)
300 {
301     ates_yok=0;
302 }
303
304 if (ates==0 && ates_time2>ates_time1)
305 {
306     say=1;
307     ates_yok=ates_yok+1;
308 }
309
310 if (ates_yok==1526)
311 {
312     ates_yok=0;
313     ates_counter=0;
314     adet=0;
315 }
316
317 if (adet>2)
318 {
319     if ((ates3-ates1)<1526)
320     {
321         hata=1;

```



```

322         output_high(NTCOUT);
323         adet=0;
324     }
325 }
326
327 if (ates_counter==30000)
328 {
329     ates3=ates3-ates1;
330     ates2=ates2-ates1;
331     ates1=0;
332     ates_counter=ates3;
333 }
334 }
335
336
337 void main() // main program function
338 {
339     setup_timer_0 (RTCC_DIV_128|RTCC_INTERNAL|RTCC_8_BIT);
340
341     while(TRUE) //main program returns here
342     {
343
344         if (!input(BREAKER) && input(TEST)) // when the filter CB is OFF and
345                                             // the Test button is pressed
346         { // the faults are cleared and
347         // the PIC is ready for normal
348             hata=0; // operation again in order to
349                 // trigger again.
350
351             output_low(NTCOUT);
352             output_low(LFTDOUT);
353             output_low(CURRENTFAULTOUT);
354             adet=0;
355         }
356
357         if(input(BREAKER)) // the status bit recalls
358                             // the position of the filter CB
359         {
360             status=1;
361         }
362         else
363         {
364             status=0; // it is guaranteed that no
365                     // triggering is made while
366                     // the filter CB is OFF.
367         }
368
369         if(status==1 && hata==0) // if the breaker is ON and
370                                 // no fault exists
371         {
372             if ((input(TEST) || input(CT2UP)) && lan1==0) // if the test button is
373                                                         // pressed or, CT2UP pin
374                                                         // is HIGH
375             {
376                 set_timer0(0); // PIC timer is reset.
377                 lan1=1;
378             }
379
380             if ((input(TEST) || input(CT2UP)) && lan1==1)
381             {
382                 if(get_timer0(>sayac4) // if the condition lasts
383                                     // more than 1.5 msec
384                 {
385                     output_high(TRIGGEROUT2); // triggering is started.
386                     output_high(TRIGGEROUT);
387                     ates=1;
388                 }
389             }
390         }

```

```

391         lan1=0;
392     }
393
394     if (ates==1)                // if there is a triggering
395     {
396         termination();          // the "termination" function cares for
397                                 // stopping the trigger.
398     }
399 }
400
401 else
402 {
403     output_low(TRIGGEROUT2);    // If filter CB is OFF or there is a fault
404     output_low(TRIGGEROUT);    // no triggering shall be made.
405 }
406 if(status==1)
407 {
408     temperature_fault();       // if filter CB is on, "temperature_fault",
409     LFTD_fault();              // "LFTD_fault" and "too_frequent"
410                                 // functions are called.
411     too_frequent();
412
413     if (ates==1 && counter1<16)
414     {
415         no_current2();
416         no_current3();
417     }
418
419     if (ates==1 && counter1>16 && counter1<32)
420     {
421         high_current2();
422     }
423
424     if (ates==0)
425     {
426         high_current3();
427     }
428 }
429 }
430 }
431

```