A MONOLITHIC PHASED ARRAY USING RF MEMS TECHNOLOGY

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ABSTRACT

A MONOLITHIC PHASED ARRAY USING RF MEMS TECHNOLOGY

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This thesis presents a novel monolithic phased array implemented using the RF MEMS technology. The structure, which is designed at 15 GHz, consists of four linearly placed microstrip patch antennas, 3-bit distributed RF MEMS low-loss phase shifters, and a corporate feed network. The RF MEMS phase shifter employed in the system consists of three sections with a total of 28 unit cells, and it occupies an area of 22.4 mm × 2.1 mm. The performance of the phase shifters is improved using high-Q metal-air-metal capacitors in addition to MEMS switches as loading elements on a high-impedance coplanar waveguide transmission line. The phased array is

fabricated monolithically using an in-house surface micromachining process, where a 1.2-μm thick gold structural layer is placed on a 500-μm thick glass substrate with a capacitive gap of 2 μm. The fabrication process is simple, requires only 6 masks, and allows the implementation of various RF MEMS components on the same substrate, such as RF MEMS switches and phase shifters. The fabricated monolithic phased array occupies an area of only 6 cm × 5 cm. The measurement results show that the phase shifter can provide nearly 20°/50°/95° phase shifts and their eight combinations at the expense of 1.5 dB average insertion loss at 15 GHz. The phase shifters can be actuated with 16 V, while dissipating negligible power due to its capacitive operation. It is also shown by measurements that the main beam can be steered to 4° and 14° by suitable settings of the RF MEMS phase shifters.

Keywords: Phased arrays, RF MEMS, phase shifter, switch, loaded line, coplanar waveguide, micromachining.

ÖZ

RF MEMS TEKNOLOJİSİ KULLANILARAK TEK PARÇA FAZ DİZİLİ ANTEN

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Bu tezde, RF MEMS teknolojisi kullanılarak gerçekleştirilen yeni bir tek parça faz dizili anten sunulmaktadır. 15 GHz frekansında tasarlanan yapı, doğrusal olarak dizilmiş 4 adet mikroşerit yama anten, 3-bit dağıtılmış RF MEMS düşük kayıplı faz kaydırıcılar ve besleme ağından oluşmaktadır. Sistemde kullanılan RF MEMS faz kaydırıcılar toplamda 28 birim hücreyle 3 bölümden oluşmaktadır ve 22.4 mm × 2.1 mm'lik bir alanı kaplamaktadır. Faz kaydırıcının performansı, yüksek empedanslı eşdüzlemsel dalga klavuzu iletim hattını yükleyen MEMS anahtarlarla birlikte yüksek-Q metal-hava-metal sığalar kullanılarak geliştirilmiştir. Faz dizili anten, 1.2

µm kalınlığında yapısal altın katmanı ve 2 µm sığasal aralığın 500 µm kalınlığında cam taban üzerine koyulduğu yüzey mikroişleme süreci ile tek parça olarak üretilmiştir. Üretim süreci basittir, sadece 6 maske gerektirmektedir ve aynı taban üzerinde RF MEMS anahtar ve faz kaydırıcı gibi çeşitli RF MEMS devre elemanlarının üretilebilmesine izin vermektedir. Üretilen faz dizili anten yapısı sadece 6 cm × 5 cm'lik bir alanı kaplamaktadır. Faz kaydırıcı yapısının yaklaşık olarak 20°/50°/95° faz kaymalarını ve bunların sekiz kombinasyonunu, 15 GHz'de 1.5 dB ortalama araya girme kaybı ile sağlayabildiği ölçüm sonuçlarıyla gösterilmiştir. Faz kaydırıcılar, sığasal olarak çalıştıkları için ihmal edilebilecek bir güç tüketimiyle, 16 V ile hareketlendirilebilmektedir. RF MEMS faz kaydırıcıların uygun olarak ayarlanmasıyla ana hüzmenin 4° ve 14°'ye döndürülebildiği yine yapılan ölçümlerle gösterilmiştir.

Anahtar Kelimeler: Faz dizili antenler, RF MEMS, faz kaydırıcı, anahtar, yüklenmiş hat, eşdüzlemsel dalga kılavuzu, mikroişleme.

"What we do in life echoes in eternity."

To my family.

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CHAPTER I

INTRODUCTION

The Microsystems Technology Office of the United States DARPA (Defense Advanced Research Projects Agency) reports that "Micro-Electromechanical Systems (MEMS) is a way of making things." [1], [2]. These "things" merge the functions of sensing and actuation with computation and communication to control physical parameters at the microscale. Present markets of MEMS technology are mainly in pressure and inertial sensors, inkjet print heads, and high-resolution digital displays. Future and emerging applications include tire pressure sensing, fiber optical components, fluid management and processing devices for chemical microanalysis, medical diagnostics, and drug delivery, and RF and wireless electronics, namely RF MEMS.

The application of MEMS technology to RF systems enables production of components with low power consumption, high linearity, low insertion loss, and high isolation [3]. RF MEMS components are particularly attractive for researchers due to their tunable properties. This technology is used to implement many tunable circuits and systems in a miniaturized way that has never been implemented before using any other technology.

The first RF MEMS structure, which is MEMS relay for microwave applications, was produced in 1991 [4]. Although the device was not mature, it showed excellent performance compared to solid-state counterparts. More mature devices were demonstrated in 1995: a series switch for DC to 60 GHz by Rockwell Science Center and a shunt switch for 10 to 120 GHz by Texas Instruments [5], [6]. These devices took attention of many research groups to the subject of RF MEMS. To date, a bundle of components and devices have been presented in the literature including various type of switches [7]-[10], phase shifters [11]-[15], impedance matchers [16]-[18], filters [19]-[21], reconfigurable antennas [22]-[24], film bulk acoustic resonators (FBARs) [25], [26]. Although these components and devices show impressive performances, there are still only a few commercially available components and devices. For instance, FBAR produced by Agilent, which is the first commercially available component in the market, enables a 5 times size reduction with respect to its ceramic counterpart at comparable performance [27]. The other commercially available one is the switch produced by Radant MEMS [28]. They offer switches with an insertion loss of lower than 0.5 dB up to 38 GHz, an isolation of 20 dB at 10 GHz and 13 dB at 40 GHz, a return loss better than 20 dB up to 36 GHz with lifetime of more than 900 billion cycles.

Although RF MEMS components are not extensively placed on the shelves of the market, we should keep in mind that it took several decades for the previous revolution of the semiconductor based circuit technology to reach its full potential. Several problems of the RF MEMS technology particularly related with long-term reliability, packaging, and fabrication cost are currently being examined by many research groups and companies. It is expected that the solutions to these problems will be available in the forthcoming years leading to the placement of many components on the market.

One of the main advantages of RF MEMS technology is that it allows monolithic implementation of a number of components to achieve more functionality and better

performance in a small area. Today a number of researchers are trying to monolithically implement various RF MEMS components on a common substrate.

This thesis presents the development of one of the first monolithic phased arrays in the literature using the RF MEMS technology [29], [30]. RF MEMS phase shifters are used in a novel phased array structure to have better performance in terms of losses and size compared to arrays with conventional phase shifters. Phased arrays consist of multiple stationary radiating elements each of which are fed by tunable phase or time-delay control units to steer the beam [31], [32]. Phased arrays are generally implemented using separately produced components such as a feed network, phase shifters, and antennas, as shown in Figure 1.1. Hybrid connection of these components not only increases the system size, but also introduces parasitic effects, packaging cost, and losses. In order to eliminate these drawbacks, there is a need to produce these components on the same substrate, forming a monolithic phased array, which is possible with the enabling RF MEMS technology.

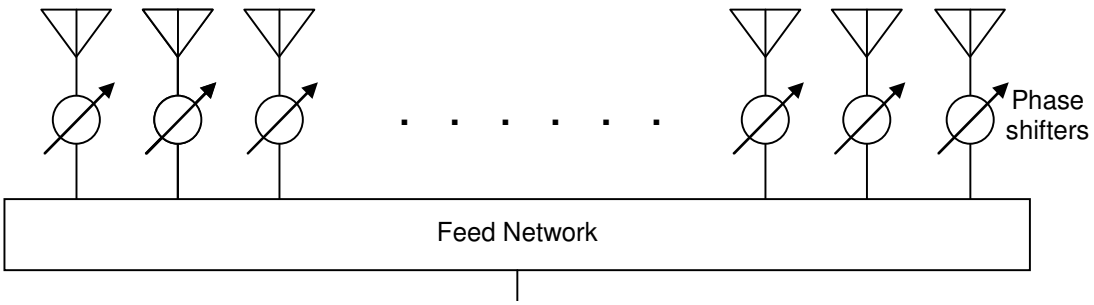


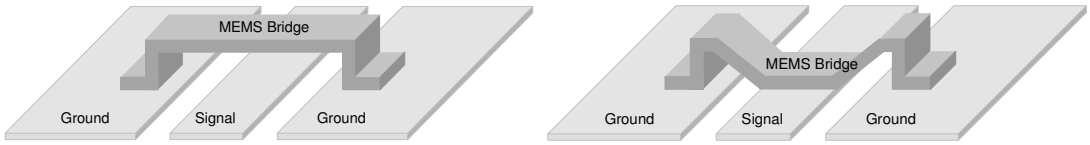
Figure 1.1 Basic phased array architecture: linear array with phase shifters for each antenna element.

This chapter introduces the RF MEMS components used in this thesis. Section 1.1 presents the RF MEMS switch, which is the key element of the technology. Section

1.2 presents an introduction about RF MEMS phase shifters. Then, Section 1.3 introduces the monolithic phased array developed in this thesis. Finally, Section 1.4 presents the research objectives and the organization of the thesis.

1.1. RF MEMS Switch: The Key Element of the Technology

RF MEMS switches have an important role since they are not only used as discrete components, but also used as a part of other components, such as phase shifters [11]-[15], impedance tuners [16]-[18], and filters [19]-[21]. There are two types of RF MEMS switches: shunt switch and series switch. Figure 1.2 and Figure 1.3 show how MEMS shunt and series switches operate, respectively. RF MEMS shunt switch is employed as the key element of the RF MEMS phase shifter of the monolithic phased array developed in this thesis. An RF MEMS shunt switch has two states: upstate and downstate. In the upstate, the bridge loads the transmission line capacitively and the RF power can be routed to the output port. In the downstate, a DC voltage is applied between the MEMS bridge and the transmission line resulting in an electrostatic force that causes the bridge to collapse on the DC isolation dielectric layer. The bridge forms a high capacitance with the signal line acting as very low impedance at the frequency of interest, and the bridge provides isolation between input and output. When the actuation voltage is removed, the MEMS bridge returns back to its original position due to the restoring spring forces. All the MEMS structures presented in this thesis are electrostatically actuated devices. There are also some other actuation mechanism such as magnetostatic, piezoelectric, and thermal actuation, which are beyond the scope of this work.



(a) (b)

Figure 1.2. Conceptual drawing of an RF MEMS shunt switch showing the two states: (a) upstate and (b) downstate.

(a) (b)

Figure 1.3. Conceptual drawing of an RF MEMS series switch showing the two states: (a) upstate and (b) downstate.

RF MEMS shunt switches are usually implemented on coplanar waveguide (CPW) topology considering the realizable bridge dimensions. A CPW-based topology has advantages over a microstrip topology, such as low radiation losses, less dispersion, easier in combining active devices, and the possibility of connecting shunt lumped components without the need of via holes through the substrate. There are also shunt switch designs on microstrip lines, but the shunt connection of MEMS bridge requires either radial stub behaving as a virtual ground or a via hole to ground metallization at the bottom of the substrate. The RF MEMS switches and the RF MEMS phase shifters designed in the frame of this thesis are implemented on conductor-backed CPW, where an additional ground plane exists at the bottom of the substrate. It is advantageous to have such a ground plane at the bottom when CPW

and microstrip structures are designed on the same substrate, which is the case for the monolithic phased array presented in this thesis. It should be noted here that, within this thesis, CPW implies conductor-backed CPW since all the designs include a ground at the bottom of the substrate.

1.2. RF MEMS Phase Shifters

Most phase shifters currently being used in microwave and millimeter wave systems are based on ferrite or semiconductor devices such as PIN diodes, or FET switches. Ferrite based phase shifters are generally used in arrays where low insertion loss is required (~1 dB) and slow-switching time (150 μs) is permissible [33], [34]. However, these phase shifters are not suitable for the implementation of low profile and low weight phased arrays. FET-based phase shifters consume very low power, but have a large amount of RF loss (4-6 dB at 12-18 GHz) [35]. PIN diode-based phase shifters consume more DC power and have slightly better performance compared to FET-based phase shifters [36], [37]. However, the semiconductor device-based phase shifters can not compete with the loss performance of the RF MEMS-based phase shifters, which has been shown with various designs [3]. MEMS phase shifters are designed using the switched line [11], [12] or the distributed loaded line [14]-[16], [38]-[40] approaches. The switched line phase shifters are implemented using MEMS switches on microstrip transmission lines. These phase shifter either require via holes for series switch configuration increasing the fabrication complexity [11] or radial stubs for shunt switch configuration limiting the bandwidth of the phase shifter [12]. Among the MEMS phase shifters, the ones designed using the distributed techniques, namely distributed MEMS transmission lines (DMTL), offer wide band and low-loss cascadable devices with a simple design and fabrication method on relatively low-permittivity substrates such as quartz ($\varepsilon_r = 3.8$) and glass ($\varepsilon_r = 4.6$). These low-permittivity substrates also allow the

implementation of the radiators monolithically integrated with the phase shifters. Therefore the monolithic phased array structure in this thesis employs a phase shifter structure designed using the distributed techniques.

The reason for low loss characteristics of a MEMS phase shifter is that the MEMS switches used in the implementation of a DMTL have a very low series resistance (0.1 to 0.3 Ω) as compared to the solid-state devices [39], [40]. The average loss of a 3-bit MEMS phase shifter is 1.2 dB at 13.6 GHz [39], which is a 3 to 4 dB improvement compared to designs using GaAs FET switches. This leads to an improvement of 6 to 8 dB in a radar system. Therefore one of the amplifier stages can be removed from the system reducing both DC power consumption and manufacturing costs of the system.

1.3. The Monolithic Phased Array Developed in This Thesis

The phased array system in this work is designed to operate at 15 GHz, and it employs 3-bit Distributed MEMS Transmission Line (DMTL) type phase shifters. These digital phase shifters are monolithically integrated with the feed network and four linearly placed microstrip patch antennas on the same substrate. Figure 1.4 shows the layout drawing of the monolithic phased array.

The use of MEMS phase shifters in a phased array offers some advantages. First, MEMS phase shifters have low-loss performance with nearly zero DC power consumption compared to semiconductor based counterparts. Moreover, MEMS phase shifters are also suitable for monolithic phased array designs with their reduced cost and volume compared to semiconductor and ferrite based counterparts. The phase shifters in the phased array presented in this work are used to obtain progressive phase shifts in the excitation of radiating elements to steer the beam. The

performance of the phase shifter is improved using high-Q MAM (Metal-Air-Metal) capacitors as the loading elements. This work is one of the first few electronically scanning phased array systems with RF MEMS phase shifters, reported in the literature [29], [30]. The other phased array structure has been presented by the University of Michigan [29], which is an array of eight linearly placed slot-coupled microstrip antennas at a design frequency of 38 GHz. The antenna elements are fed by a corporate feed network consisting of Wilkinson power dividers and eight analog type RF MEMS phase shifters. The feed network and RF MEMS phase shifters are fabricated monolithically and are laminated to a substrate containing the antennas using tile construction techniques. It is reported that the main beam of the phased array can be steered to 12° by suitable settings of the RF MEMS phase shifters.

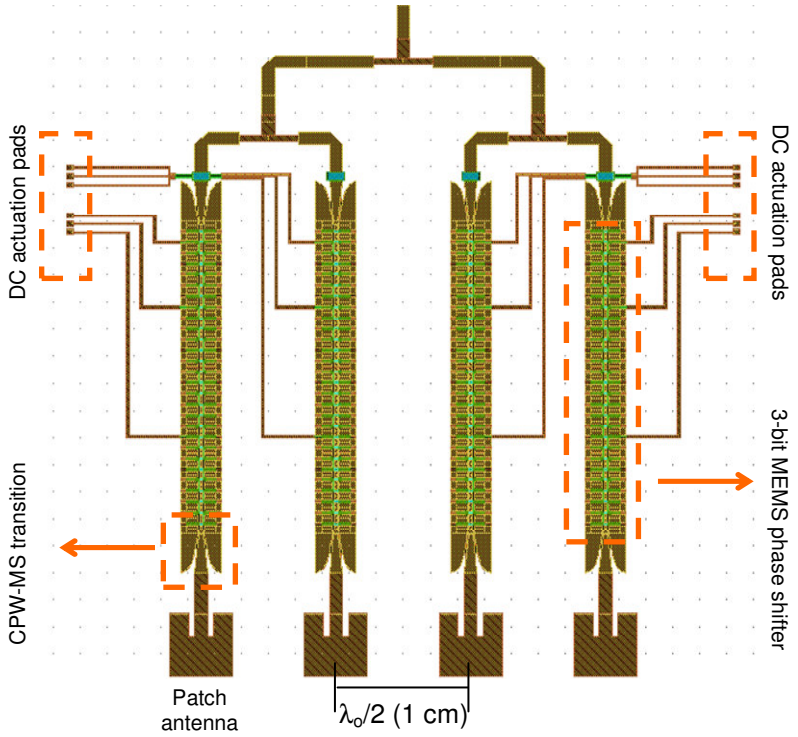


Figure 1.4. The layout drawing of the monolithically integrated phased array developed in this thesis.

1.4. Research Objectives and Organization of the Thesis

The goal of this thesis is to design, fabricate, and measure a novel monolithic phased array using the RF MEMS fabrication process developed at Middle East Technical University. The specific objectives in the frame of this thesis can be summarized as follows:

- The optimization of the in-house process for the fabrication of RF MEMS devices at the microelectronics facilities of METU.

- RF MEMS switch design and fabrication.

    - MEMS switch is used as a part of the MEMS phase shifter in the phased array. The switch should be designed to have a very low insertion loss and high isolation since many of these switches needs to be cascaded in the final design.

- Modeling of distributed structures.

    - The phase shifters of the array are designed using distributed techniques. A number of different distributed MEMS transmissions lines should be used to verify modeling and simulations. New modeling approaches should be developed if required.

- Modeling, design, and fabrication of MEMS phase shifters.

    - The phase shifter should provide the required phase shift steps at the operating frequency of the array. The device should have a low

insertion loss. Additional layers such as resistive bias lines should be added to the process if required.

- Design, fabrication, and measurement of the monolithic phased array.

    - The designed digital phase shifters should be monolithically integrated with the corporate feed network and the antennas. Test boards for the radiation pattern measurements should be prepared.

This thesis includes the results of the accomplishments up to date in the frame of the mentioned objectives in six chapters. After this introduction chapter, Chapter 2 gives the process flow followed throughout the fabrication of RF MEMS devices in this thesis.

Chapter 3 presents the design, modeling, and measurement results of RF MEMS shunt switches. The mechanical design and the electrostatic actuation principles of MEMS devices, CPW line formulations, and inductive tuning methods are also included in the chapter.

Chapter 4 gives the theoretical background of DMTL structures with different design aspects followed by the design and measurement results of the digital phase shifter used in the phased array.

Chapter 5 presents the measurement results for the monolithic phased array. This chapter also introduces the setup used for the radiation pattern measurements.

Chapter 6 concludes the thesis with a discussion on the future work requiring further research.

CHAPTER II

RF MEMS FABRICATION PROCESS DEVELOPED AT METU

2.1. Introduction

This chapter presents the fabrication process developed at METU Microelectronics Facility (METU-MET), which is used to realize the devices in the frame of this work[1]. The fabrication is composed of several steps such as layout drawing, processes in the cleanroom including many lithography, deposition and etching steps, dicing, and release of suspended MEMS structures. The following sections of the chapter give a brief overview of these steps.

[1] A number of other researchers were also involved in the development of this process, namely Mr. Hüseyin Sağkol, Mr. Mehmet Ünlü, Ms. İpek İstanbulloğlu, Mr. Engin Ufuk Temoçin, and Mr. Halil İbrahim Atasoy.

2.2. Required Layers and Materials for RF MEMS Technology

Figure 2.1 shows the cross-section of an RF MEMS switch illustrating the required layers to fabricate the fundamental structure. It is composed of a base metallization for CPW or microstrip line implementation, a suspended movable bridge, and an isolation layer on top of the base metallization to prevent DC short during the electrostatic actuation. The gap between the base metal and the bridge (structural) layer is offered by the use of a spacer layer coated before the deposition of the bridge layer. The spacer layer is removed at the end of the processes. Therefore, the spacer layer is commonly termed as "sacrificial layer". These layers can be used for the realization of many RF MEMS components and systems as shown in this thesis by only modifying the layout drawings. Although the fabrication gives the impression to be quite simple, it requires a sequence of good choices of materials and processes. Companies and even research laboratories do not give the details of the critical steps in their fabrication process. Therefore, the METU RF MEMS group had to develop its own solution for these hidden parts of the fabrication after many time consuming optimization experiments. It should be noted here that the success of MEMS fabrication in general is highly dependent on the material selection, the processing conditions, and the specific equipment used. The information about the material selection given below is the outcome of the mentioned experiments of the METU RF MEMS group and depends on the available equipment and the infrastructure at METU-MET.

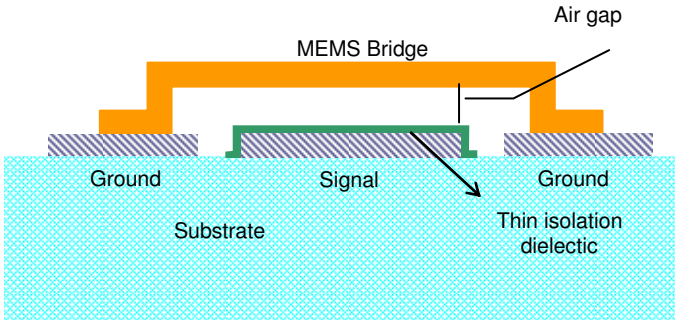


Figure 2.1 Cross-section of an RF MEMS device, which is composed of three major layers: Base metal, isolation dielectric, and structural bridge layers.

- **Substrate selection**: The substrate selection is important not only for the RF losses, but also for the system level integrity considering the other possible elements of the system such as antennas, active devices, and the cap wafers used in the packaging. Insulating or semi-insulating substrates are often necessary for RF MEMS devices to minimize the losses. High-resistivity (> 5000 Ω.cm) silicon (HRS) substrates offer acceptable performances when a polysilicon and silicon dioxide stabilizing layers between the substrate and base metal are employed. Semi-insulating gallium arsenide (GaAs) is also preferred substrate since GaAs is already in usage for MMIC for its high electron mobility. Insulators such as glass, quartz, and alumina are widely used substrates for RF MEMS processes since they have low-loss characteristics and compatibility with the most processes in a cleanroom. Glass substrates with a thickness of 500 µm are preferred in the METU RF MEMS processes as they are low-cost (< $30 per wafer), and suitability for more efficient antennas to be integrated with RF MEMS components due to its relatively low dielectric permittivity (ε_r = 4.6) compared to HRS substrate (ε_r = 11.9), and suitable for anodic bonding with a silicon cap, which is used for wafer-level packaging.

- **Base metal selection**: Base metals of RF MEMS devices are usually aluminum, gold, or copper as their conductivities are sufficiently high for lowering the losses due to conductor, while they are easily deposited with standard semiconductor process equipments. The base metallization is selected as gold in the METU RF MEMS process.

- **Isolation dielectric selection**: Thin isolation dielectric in RF MEMS devices are required to prevent DC short between the bridge and the base metal when the bridge collapses. The material should be able to withstand an electric field of about 100-150 MV/m in order to operate the RF MEMS devices without any breakdown during the electrostatic actuation. The common materials are silicon nitride and silicon dioxide that are widely used in many MEMS applications for insulating, protection, and diffusion barrier layers. It should be noted here that the dielectric constant of the isolation dielectric is also a concern to achieve high downstate capacitance in RF MEMS devices. Silicon nitride is often preferred with its high dielectric constant over silicon oxide, and therefore silicon nitride is used as the isolation dielectric in the METU RF MEMS process.

- **Sacrificial layer selection**: In order to have a mechanically movable structural layer in MEMS structures, a sacrificial layer is deposited underneath. This layer is etched at the end of the process releasing the structural layer free to move. There are several requirements during the selection of a sacrificial layer:

    1. It should be able to withstand chemical and thermal processes till the end of the process.
    2. It should be straightforwardly removed underneath the suspended bridges without damaging the other layers.

3. It should be deposited, grown, or spun on the wafer uniformly in order to sustain the designed capacitive gap for RF MEMS devices. Otherwise, the performances of the devices show variations along different locations of the wafer, which is detrimental in large-scale devices such as a phased array.

During the research at METU, three types of sacrificial layers are studied: photoresist, copper, and polyimide. Photoresist does not satisfy the first requirement in the list above as a sacrificial layer. The solvents in the photoresist outgas during deposition, cracking or even making bubbles on it during the structural layer growing. Moreover, photoresist, even if it is cured, is solved in acetone, which is widely used in the rest of the process after the deposition sacrificial layer. Copper is comparatively reliable material unless some solvents and etchants are avoided after the deposition of the copper sacrificial layer. It can be selectively and easily etched during the release of the suspended structures. However, the principal bottleneck for the copper sacrificial layer is its uniformity when it is grown by copper electroplating, which is inherently a non-uniform process. The non-uniformity for the copper sacrificial layer is about 50 %, i.e., the measured height of the layer is between 1 µm and 3 µm when a 2-µm thick sacrificial layer is targeted. Polyimide is an organic material which is spin-coated as photoresist. Spin-coating ensures the thickness uniformity with a deviation less then 10 % across the wafer. Polyimide is stable against standard acids and solvents. It does not outgas during the deposition of the structural layer if it is properly cured. Therefore, polyimide is selected as the sacrificial layer in the METU RF MEMS process. The METU RF MEMS group has developed two reliable removal processes for the polyimide sacrificial layer: i) wet removal using a special organic solvent and, ii) dry removal using reactive ion etching (RIE) equipment to form an oxygen plasma environment (O_2 mixed with CF_4), which is detailed in the next section.

- **Structural layer**: Together with the removal of the sacrificial layer, the structural layer formation is the most critical part of the RF MEMS process influencing the device performance significantly. The stress of the structural layer, which may results as buckling of the bridges, is the major concern about this layer. Gold layer deposited by sputtering technique is used as the structural layer in the current METU RF MEMS process. Sputtering parameters of the structural layer deposition are adjusted so that low-stress bridges are obtained after the removal of the sacrificial layer. There are some advantages of using gold as the structural layer. Gold is an inert metal that does not form any oxide that degrades the conductivity of the layer and imposes stress to the structural layer. Moreover, gold is not damaged during wet or dry etching of the sacrificial layer. The METU RF MEMS group has also used electroplated gold with copper sacrificial layer process. The current density, which is equal to the current divided by the mask opening area, is an important parameter controlling the stress of the structural layer. Therefore, gold electroplating process recipe depends on the mask set that is being used, and the recipe should be modified as the mask set is changed, which produces additional load to the fabrication optimization time. Hence, the use of sputtered gold with polyimide sacrificial layer is preferred over the use of electroplated gold with copper sacrificial layer.

2.3. Process Flow

This section presents the METU RF MEMS process flow. The process requires 6 masks. Some of the details are as follows:

- ***Wafer cleaning:*** Before processing, wafers are cleaned using Piranha solution against any organic/inorganic contaminants.

- ***Surface treatment:*** The surface roughness of the glass wafers are increased by means of buffered HF acid in order to enhance the adhesion of layers to substrate.

- ***Resistive bias line deposition and pattern:*** RF MEMS devices such as digital phase shifters require resistive bias lines which are realized with sputter deposition of 2000-Å thick Si-Cr. After the lithography for the *masking* of photoresist, Si-Cr layer is etched in buffered HF. These process steps are summarized in Figure 2.2 and Figure 2.3.

- ***Seed layer deposition and electroplating for thicker base metal:*** Base metallization is formed first depositing a seed layer of Ti/Au (300 Å/3000Å) via sputtering. Titanium is an adhesive metal which is deposited before gold without breaking the chamber pressure. Some regions, which are defined by the *masking* with photoresist, are electroplated in a cyanide based gold electroplating solution to obtain nearly a 3 µm-thick gold layer. These process steps are depicted in Figure 2.4 and Figure 2.5.

- ***Seed layer post-etching of base metal:*** The residuary Ti/Au seed layer is etched by means of wet etching with the selective titanium and gold etchants after the lithography for the *masking* of CPW line not to have damage on them. This process step is shown in Figure 2.6.

- ***Isolation dielectric deposition and pattern:*** The isolation dielectric, which is silicon nitride (SiN) with a thickness of 3000 Å, is deposited using plasma enhanced chemical vapor deposition (PECVD) equipment. After the lithography for the *masking* of the regions requiring isolation dielectric, the open regions are etched via reactive ion etching (RIE) equipment, which forms a plasma environment with a mixture of special gases. RIE equipment provides reliable dry etching of silicon nitride compared to wet etching,

which is a challenging task due to the damage of silicon nitride etchant (orthophosphoric acid) on the photoresist. Figure 2.7 shows the corresponding process step.

- ***Sacrificial layer formation:*** Photo-definable polyimide (PI2737 by HD Microsystems) is spun on the wafer and exposed with the anchor opening *mask* to construct the connection points between the base metal and the structural layer. After curing, the resulting thickness is 2 µm with a high-uniformity across the wafer. The process step is shown in Figure 2.8.

- ***Structural layer formation:*** 1.2-µm thick DC sputtered gold forms the structural layer of RF MEMS structures. The structural layer is connected to the base metal from the anchor openings. After the lithography for the *masking* of the bridge, the anchors and any other region requiring a second metallization such as a metal-insulator-metal (MIM) and a metal-air-metal (MAM) capacitor, the remaining structural layer is etched with the selective gold etchant. The *etch holes* enhancing the sacrificial layer removal process is also patterned on the bridges. Figure 2.9 summarizes the structural layer deposition and pattern process.

- ***Sacrificial layer etch and release of the suspended structures:*** The METU RF MEMS group developed two processes for the sacrificial layer etch: wet etch and dry etch. The former is the polyimide removal with SVC-175, which is a multi-purpose photoresist stripper, followed with the drying the samples or the wafer using critical point dryer equipment. Critical point dryer is used to avoid stiction, which occurs due to the surface tension of the liquids underneath the suspended structures pulling them down to the substrate during drying [41]. The latter is the dry etch of polyimide in RIE where two gases, namely O_2 and CF_4, are applied at the same time for an improved removal process of the polyimide compared to the simple O_2 plasma. The

structures are directly released without any need for drying. It should be noted here that both of the processes offer similar RF performances. However dry release with RIE equipment is advantageous over wet etching since the structures are directly ready for measurements after etching without any need for critical point drying. Figure 2.10 shows the finalized structure after the release process.

The process steps described above is applied for the implementation of components at METU such as switches, phase shifters, impedance matchers, and reconfigurable antennas. Figure 2.11 shows the SEM photographs of a frequency tunable antenna fabricated at METU MET, as an example to the implemented devices [22].

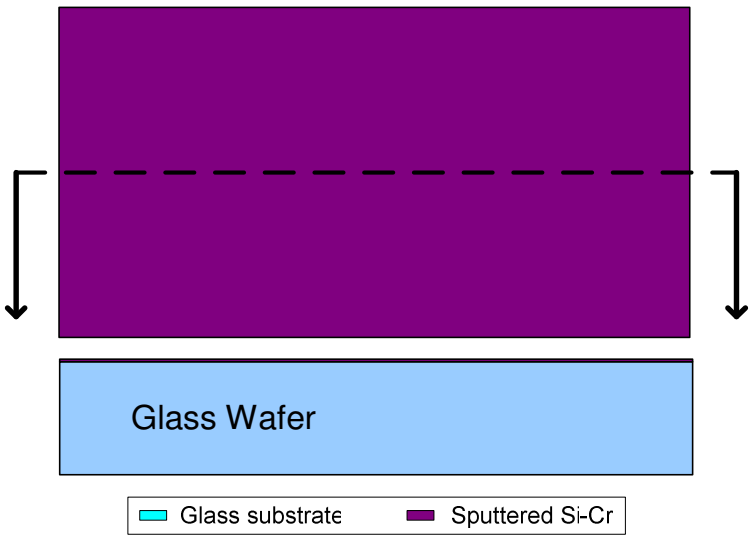


Figure 2.2 2000 Å-thick Si-Cr resistive layer deposition using RF sputtering.

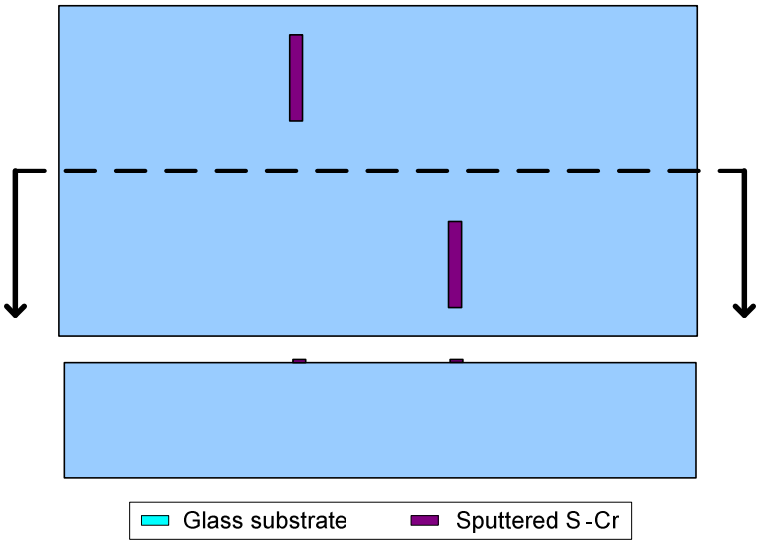


Figure 2.3 Etching of Si-Cr layer using buffered HF acid.

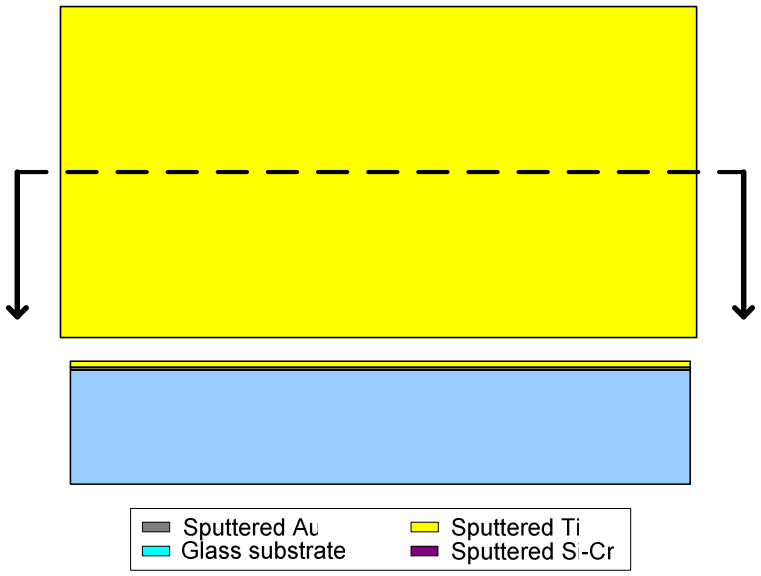


Figure 2.4 300 Å/3000 Å-thick Ti/Au seed layer deposition via sputtering.

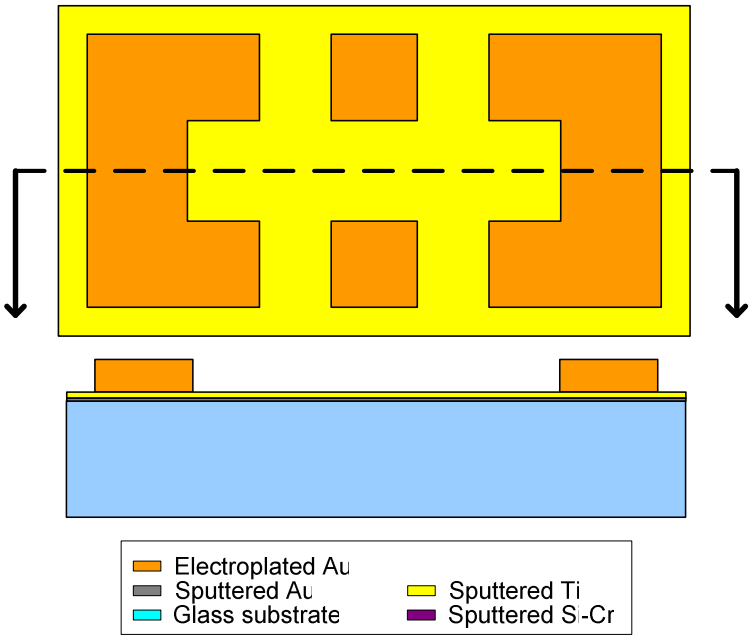


Figure 2.5 Electroplating of gold up to 3 µm for thick CPW metallization.

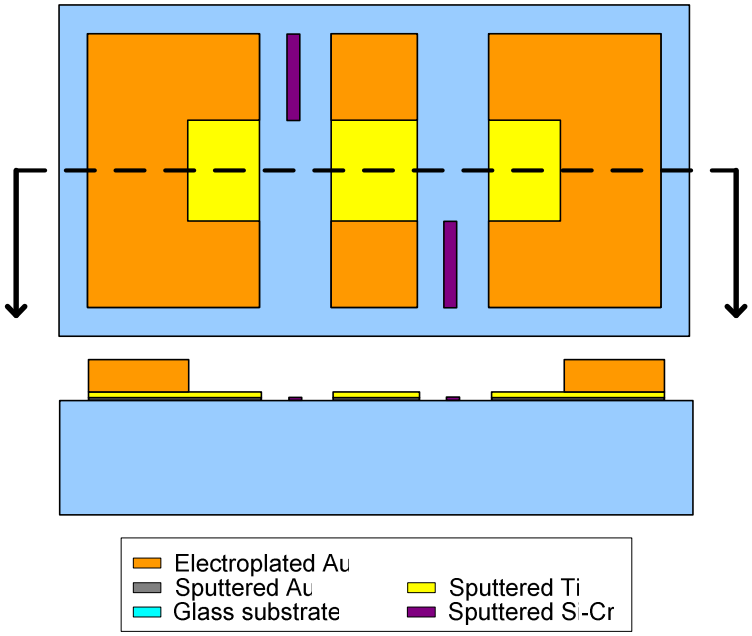


Figure 2.6 Ti/Au seed layer removal from residuary regions.

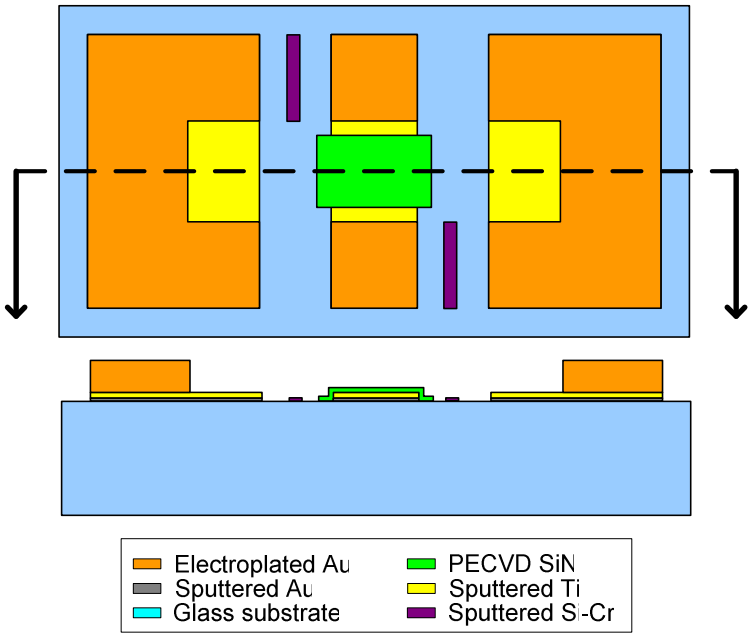


Figure 2.7 Deposition of 3000 Å-thick silicon nitride (SiN) using PECVD and pattern using RIE equipment.

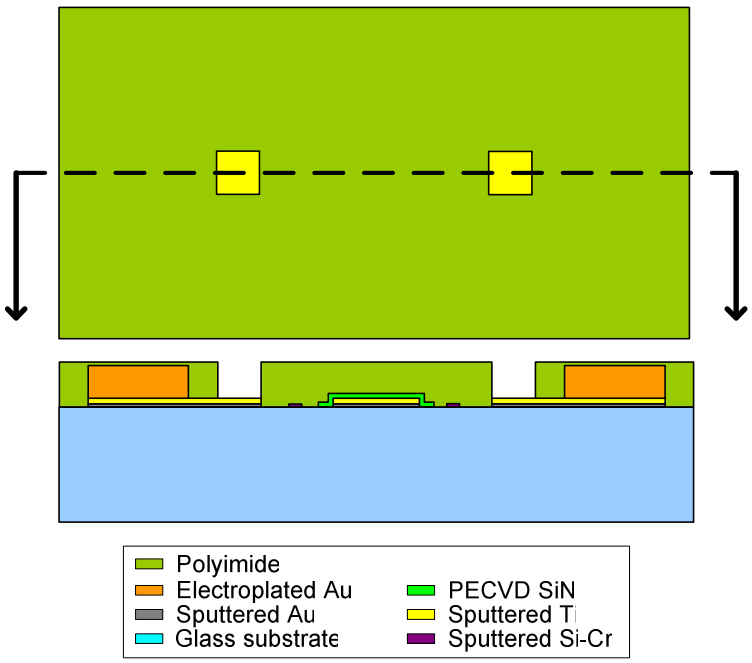


Figure 2.8 Spin-coating of polyimide as the sacrificial layer and pattern.

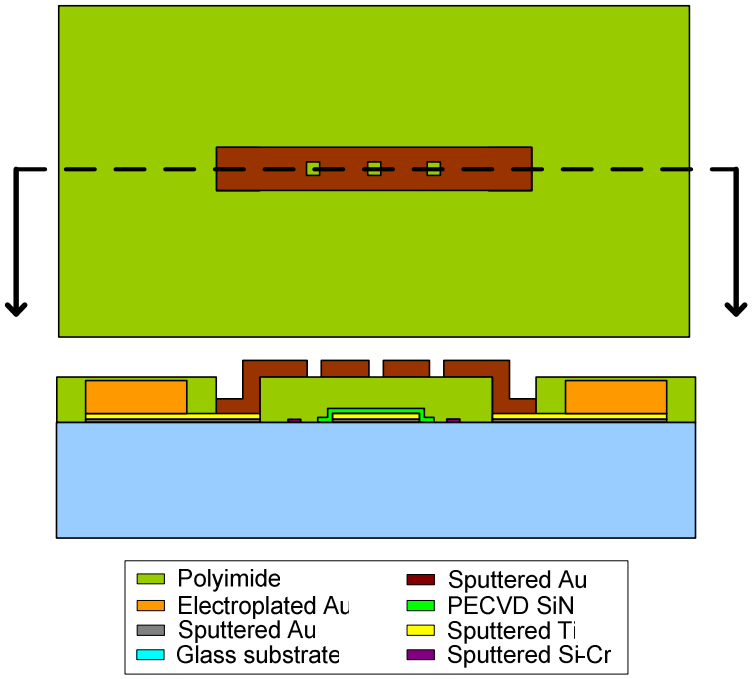


Figure 2.9 1.2-µm thick Au structural layer deposition and pattern.

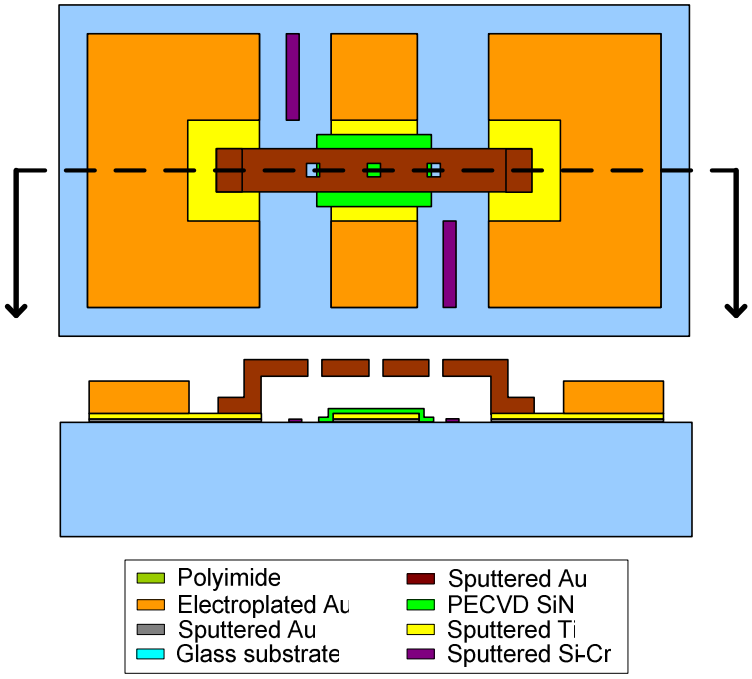
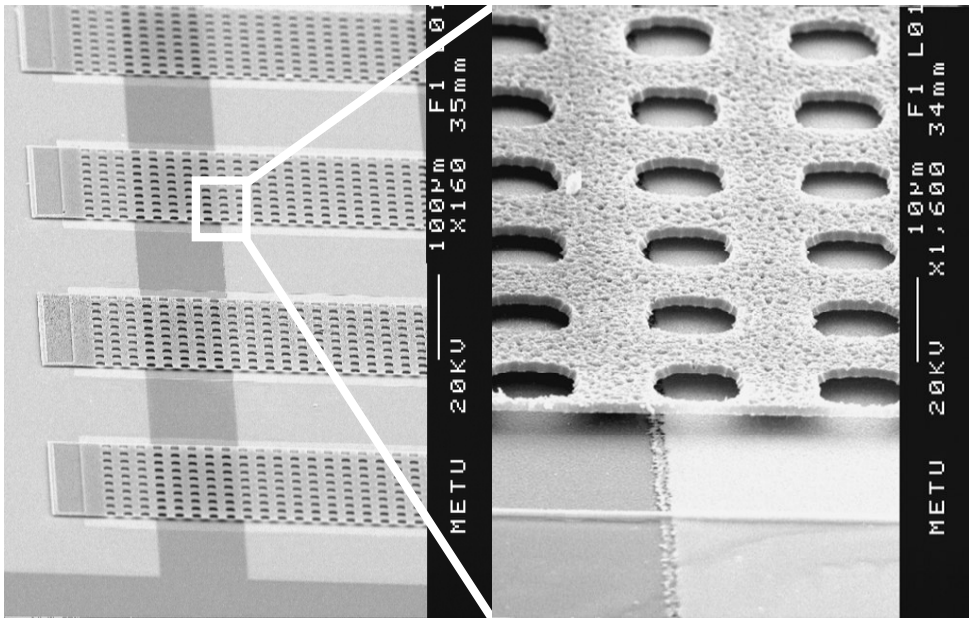


Figure 2.10 Sacrificial layer removal and release of suspended structures.



(a) (b)

Figure 2.11 SEM photographs of the fabricated frequency tunable antenna: (a) The loading section of the frequency tunable antenna and (b) The detailed view of the bridge region marked in (a).

CHAPTER III

DESIGN AND MODELING OF RF MEMS CAPACITIVE SHUNT SWITCHES

3.1. Introduction

This chapter deals with the design and modeling of RF MEMS shunt switches. The background introduced in this chapter is beneficial to construct the fundamentals about the phase shifters used in the phased array developed in this thesis. These fundamentals include the mechanical design equations, the actuation mechanism of RF MEMS structures, and the circuit modeling of the switches. The chapter does not concentrate on one switch geometry, but tries to give different design aspects such as inductive tuning methods of the RF MEMS shunt switches for *Ku*-band applications. This chapter also presents the measurement results of RF MEMS shunt switches that are designed and fabricated at METU in the frame of this thesis.

There are two basic switches used in microwave and millimeter-wave circuits design: the shunt switch and the series switch. Figure 3.1 gives the schematic view of the series and the shunt switch configurations. An ideal series switch results in an open circuit in the transmission line when no bias voltage is applied (upstate position), and it results in a short circuit in the transmission line when a bias voltage is applied

(downstate position). Ideal series switches have infinite isolation in the upstate position and have zero insertion loss in the downstate position. RF MEMS series switches are used extensively for 0.1 to 40 GHz applications. They offer high isolation at RF frequencies, around 50 dB to 60 dB at 1 GHz and rising to 20 to 30 dB at 20 GHz. In the downstate position, they result in very low insertion loss, around 0.1 to 0.2 dB at 0.1 to 40 GHz.

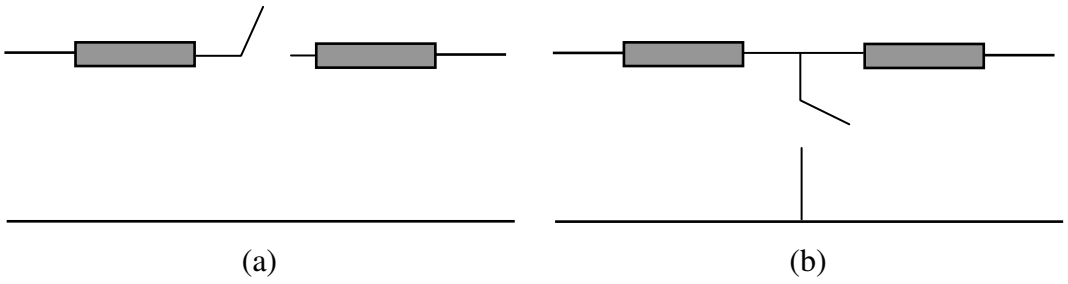
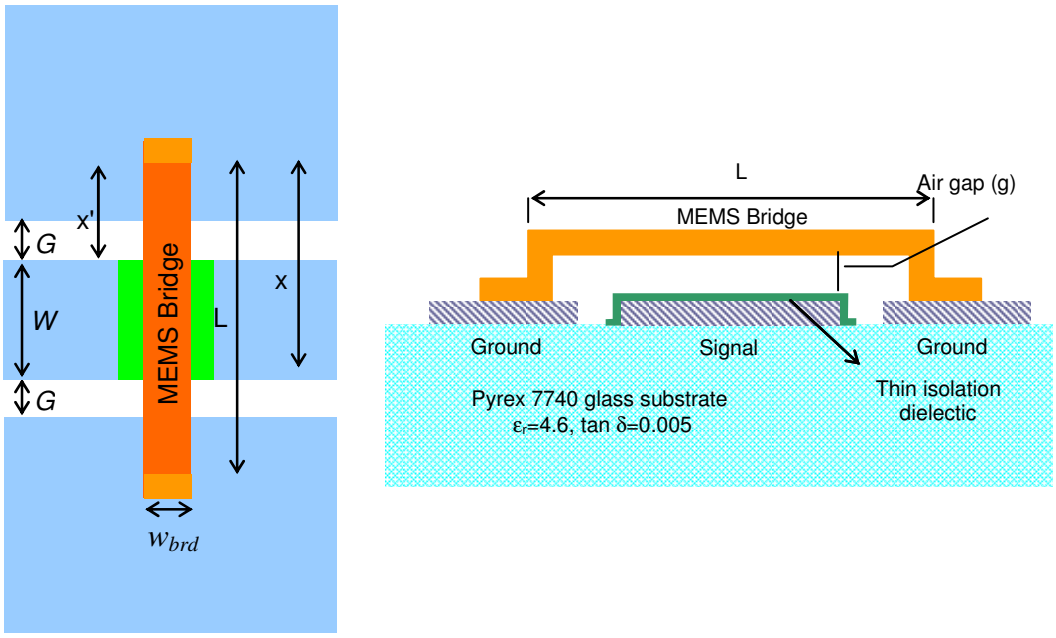


Figure 3.1 Configurations of RF MEMS switches: (a) Series and (b) Shunt.

The shunt switch is placed in shunt between the transmission line and ground; depending on the applied bias voltage, it either leaves the transmission line undisturbed or connects it to ground. Therefore, an ideal shunt switch results in zero insertion loss when no bias is applied (upstate) and infinite isolation when bias is applied (downstate). RF MEMS shunt switches are more suited for higher frequencies (5-100 GHz) since the connection between the transmission line and ground is provided through a capacitance behaving virtually as a short circuit at higher frequencies. A well-designed shunt capacitive switch results in low insertion loss (0.04 to 0.1 dB at 5-50 GHz) in the upstate position and acceptable isolation (better than 20 dB at 10-50 GHz) in the downstate position.



(a) (b)

Figure 3.2 RF MEMS capacitive shunt switch: (a) Top view and (b) Cross-sectional view.

3.2. Description of the MEMS Shunt Switches

Figure 3.2 shows the general schematic view of a shunt RF MEMS switch. The switch consists of a CPW transmission line and a metallic membrane suspended at a height h_o above the dielectric layer on a CPW transmission line. The dielectric layer having a thickness of t_d is used to prevent DC short when the bridge collapses.

Typical values of the switch geometry are a dielectric thickness, t_d, of 1000-1500 Å with a relative dielectric constant of 5.0-7.6 depending on the material used, a bridge height, h_o, of 1.5-5 µm, a length, L, around 250-400 µm, and a width, w, between 25 and 180 µm depending on the switch capacitance required. The length is rarely shorter than 200 µm due to the sharp increase of the actuation voltage with

decreasing bridge length. The width is practically limited to 200 µm to have a flat contact area between the MEMS bridge and transmission line for the downstate of the switch.

3.3. Mechanical Design of Shunt Switches

3.3.1. Spring Constant

The spring constant is composed of two components, one due to the stiffness of the material and one due to the biaxial stress within the beam because of the fabrication [3]. There are three common cases for applying the force in MEMS structures: evenly distributed on the entire beam, evenly distributed over a portion of the beam around the center, and evenly distributed near the ends of the beam. Figure 3.3 shows the case where the force is distributed over a portion of the beam around the center. Since the MEMS structures presented in this thesis mechanically belong to this group, only the formulations for this case are summarized below.

The first component of the spring constant is given by [42]:

$$k' = 32Ew\left(\frac{t}{L}\right)^3 \frac{1}{8\left(\frac{x}{L}\right)^3 - 20\left(\frac{x}{L}\right)^2 + 14\left(\frac{x}{L}\right) - 1} \tag{3.1}$$

where E is the Young's modulus, w is the width of the beam, t is the thickness, and L is the length. The second component which is due to the tensile residual stress is given by:

$$k'' = \frac{8\sigma(1-\nu)w\left(\frac{t}{L}\right)}{3-2\left(\frac{x}{L}\right)} \tag{3.2}$$

where σ is the residual stress, ν is the Poisson's ratio. The total spring constant in a fixed-fixed beam with uniformly distributed load and in the case of tensile stress is the sum of the two components [42]:

$$k_{Total} = k' + k'' \tag{3.3}$$

$$k_{Total} = 2Ew\left(\frac{t}{L}\right)^3 \frac{1}{8\left(\frac{x}{L}\right)^3 - 20\left(\frac{x}{L}\right)^2 + 14\left(\frac{x}{L}\right) - 1} + \frac{8\sigma(1-\nu)w\left(\frac{t}{L}\right)}{3-2\left(\frac{x}{L}\right)} \tag{3.4}$$

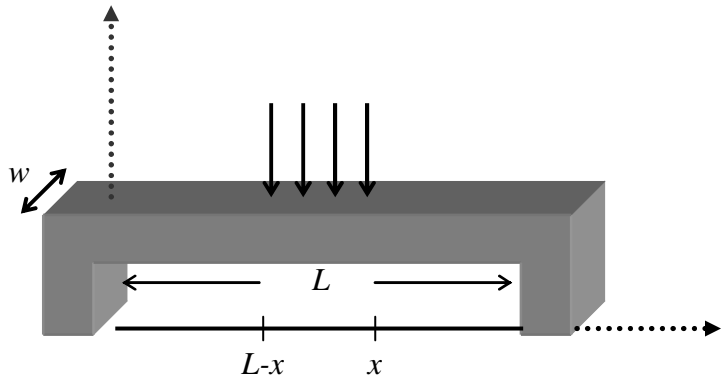


Figure 3.3 The diagram of a fixed-fixed beam with the force distributed uniformly around the center from *L-x* to *x*.

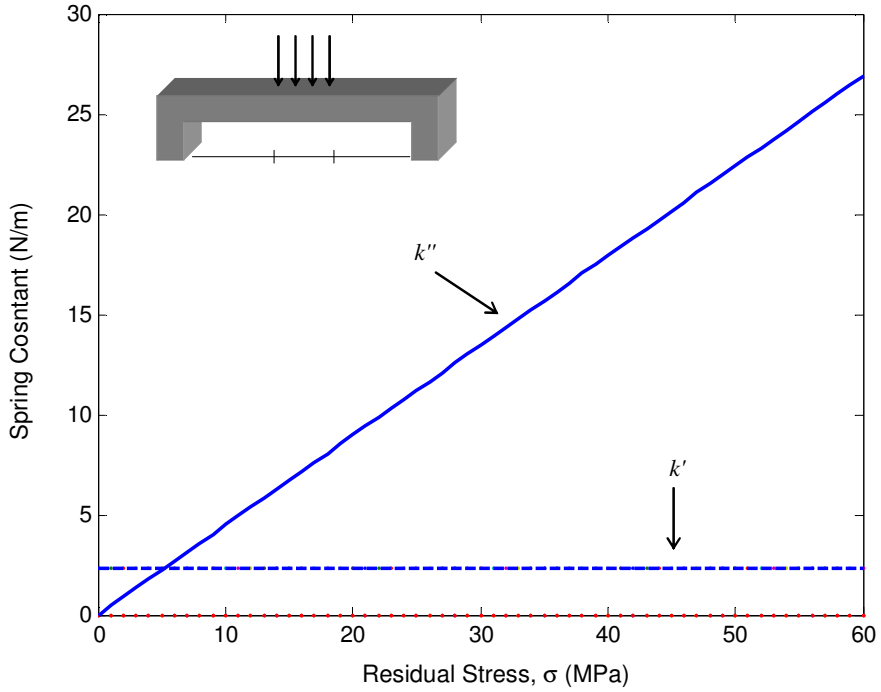


Figure 3.4 The variation of the spring constant components (k' and k'') with respect to the residual stress (σ) for a center-loaded fixed-fixed gold beam.

Figure 3.4 shows the variation of k' and k'' with respect to the residual stress for a beam with the force distributed around the center for $x = 2L/3$. The structure is selected to be a 300-μm long, 1-μm thick gold beam (E = 78 GPa). The spring constant component due to the stiffness of the beam, k', depends on Young's modulus, not on the residual stress. On the contrary, the other spring constant component, k'', changes linearly with respect to the residual stress. The k'' component dominates the k' component as the residual stress is larger than 15-20 MPa. The residual stress is absolutely related to the fabrication conditions of the beam and can be reduced by applying proper processing conditions.

3.3.2. Electrostatic Actuation

When a voltage is applied between the electrodes of a capacitor, an electrostatic force is exerted on the electrodes and they attract each other. For a MEMS capacitor, the beam, which is the only movable part of the system, is deflected towards the lower electrode. The restoring force due to the stiffness of the beam opposes this electrostatic force forming equilibrium. Figure 3.5 gives a schematic view of the forces on the beam under electrostatic actuation.

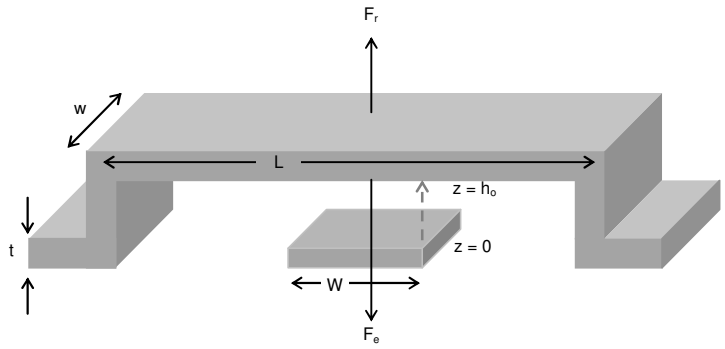


Figure 3.5 The forces on the beam under electrostatic actuation.

The electrostatic force, F_e, deflecting the beam to a height of h from the initial height of h_o increases the capacitance and hence the stored electrical energy. The electrostatic force, F_e, can be found by the taking the derivative of stored electrical energy since it is related with the change of the stored energy with respect to the beam height. The stored electrical energy can be expressed as:

$$W_e = \frac{1}{2}C(h)V^2 = \frac{1}{2}\frac{\varepsilon_o W w}{h}V^2 \qquad (3.5)$$

$$F_e = \frac{\partial W_e}{\partial h} = -\frac{1}{2}\frac{\varepsilon_o W w}{h^2}V^2 \tag{3.6}$$

The sign of resulting expression in (3.6) indicates the direction of electrostatic force. The restoring force, F_r, opposing to the movement due to the electrostatic force can be expressed as:

$$F_r = k(h_o - h) \tag{3.7}$$

The equilibrium condition is used to obtain a relationship between the beam height and the applied voltage as follows:

$$F_e + F_r = 0 \tag{3.8}$$

$$V = \sqrt{\frac{2kh^2}{\varepsilon_o W w}(h_o - h)} \tag{3.9}$$

Figure 3.6 shows a plot of gap vs. applied voltage extracted using (3.9) for a gold beam. There are two possible beam positions for every applied voltage. However the hachured region is the unstable portion for the height values. The beam position becomes unstable at $2h_o/3$ because of the positive feedback on the beam. As the voltage is increased, the gap height decreases, which, in turn, increases the capacitance and thus the charge and the electric field.

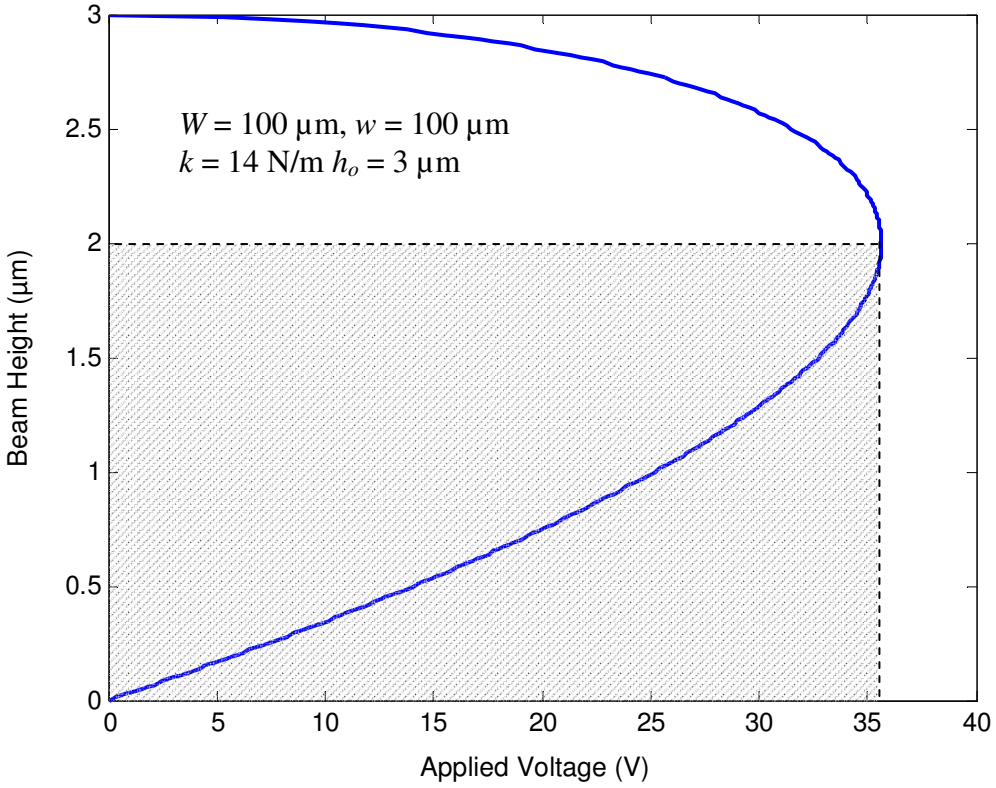


Figure 3.6 Beam height vs. applied voltage for a fixed-fixed beam. The hachured region indicates the portion for unstable gap height.

The unstable gap height can be found by taking the derivative of (3.9) with respect to h and equating it to zero, which is two-thirds the initial gap height. If this height is substituted into (3.9), the pull-in voltage is found to be:

$$V_p = \sqrt{\frac{8k}{27\varepsilon_o W w} h_o^{\,3}} \tag{3.10}$$

Figure 3.7 shows the pull-in voltages, which are calculated using (3.4) and (3.10) with different beam thicknesses, for aluminum and gold beams with residual stresses

of 0, 15, 30, 45, and 60 MPa. Aluminum and gold beams have similar spring constant and actuation voltages. The thickness of the beam should be selected around 1-1.5 µm to have a reasonable pull-in voltage. Figure 3.8 presents the pull-in voltage values for different gap heights. A gap height around 2 µm seems to be a good compromise to achieve both low upstate capacitance and low actuation voltage at the same time. Figure 3.9 shows the effect of residual stress on the actuation voltage when the beam thickness and height is selected as 1 µm and 2 µm, respectively. The residual stress should be kept lower than 20 MPa to have an actuation voltage lower than 20 V.

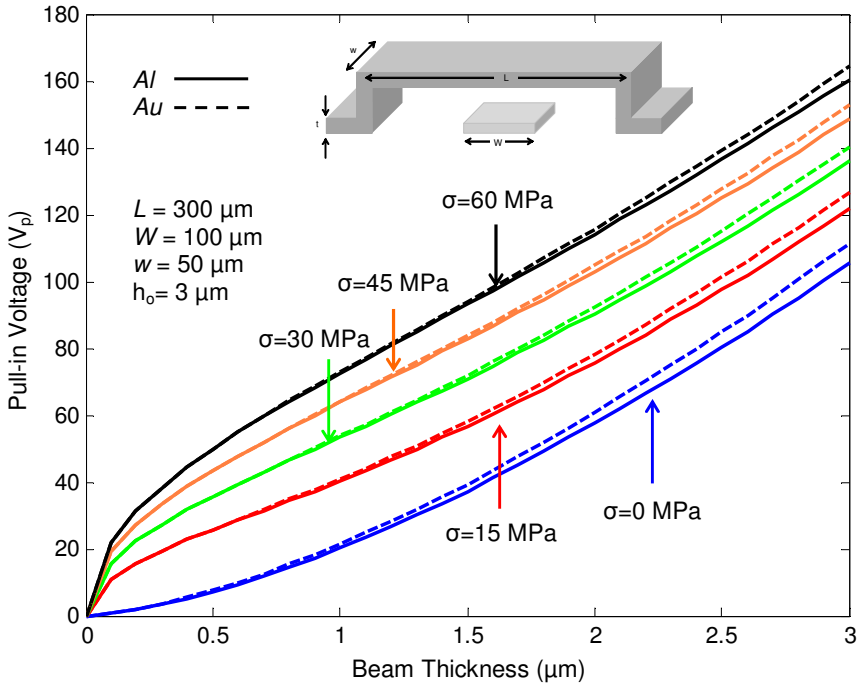


Figure 3.7 Pull-in voltage of beams versus beam thickness.

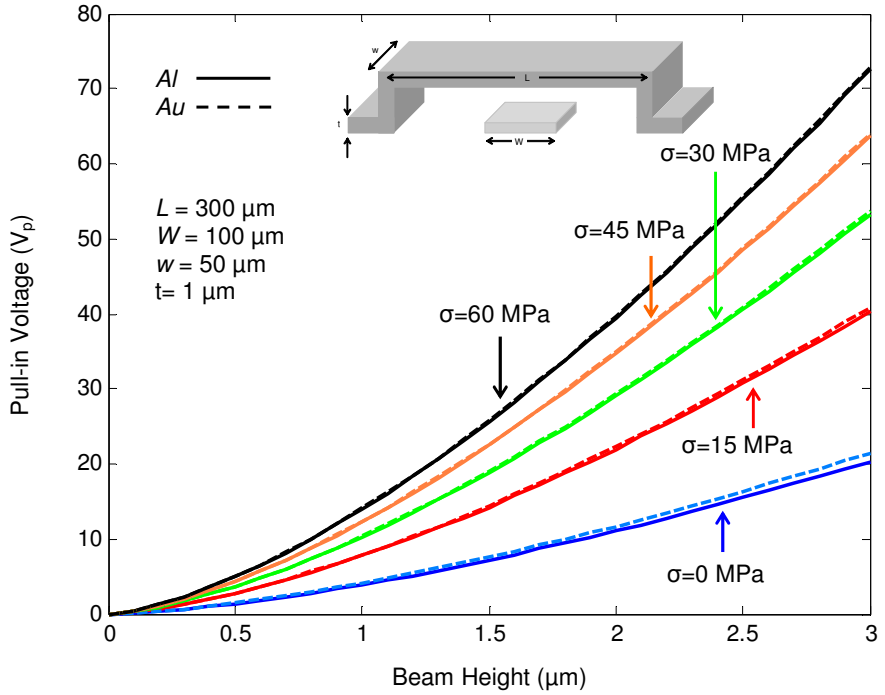


Figure 3.8 Pull-in voltage of the fixed-fixed beams vs. beam height.

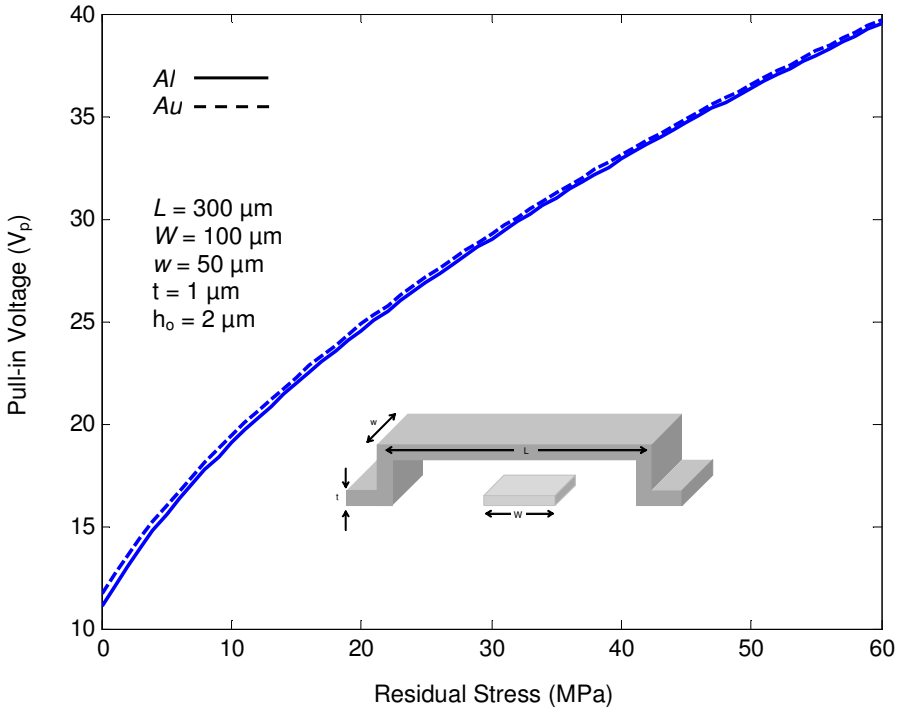


Figure 3.9 Pull-in voltage of the fixed-fixed beams vs. residual stress.

3.4. Circuit Model of MEMS Shunt Switches

Figure 3.10 shows the equivalent *CLR* circuit model [8] for the RF MEMS shunt switch. The MEMS switch is modeled by two short sections of transmission line and a lumped *CLR* model of the bridge with the capacitance having the upstate (C_{bu}) and downstate (C_{bd}) values. The name *CLR* is intentionally chosen since the dominant element in the shunt branch is the capacitance of the bridge. Typical values of the capacitance for mm-wave switches are 35 fF/2.8 pF, an inductance of 6-12 pH and a series resistance of 0.2-0.3 Ω. For X-band switches, the capacitance is 70 fF/5.6 pF with an inductance of 4-5 pH and a series resistance of 0.15 Ω.

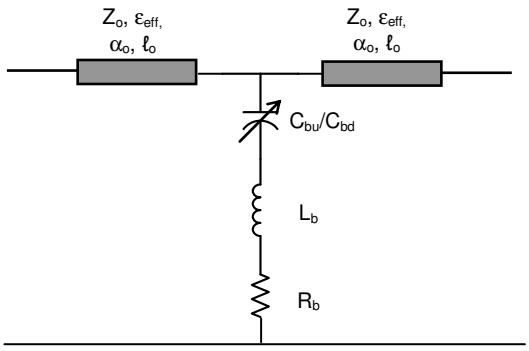


Figure 3.10 The equivalent *CLR* circuit model for the RF MEMS shunt switch.

3.4.1. CPW Transmission Line Design and Modeling

RF MEMS shunt switches are usually implemented on CPW since MEMS bridges are easier to fabricate on CPW lines, as mentioned before. Figure 3.11 shows the physical parameters of a conductor-backed CPW.

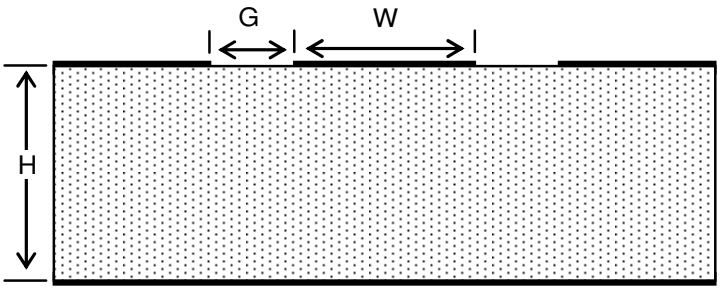


Figure 3.11 Conductor-backed CPW where *W* is the signal line width, *G* is the spacing between the signal line and *H* is the substrate thickness.

In order to design or accurately model a switch or any other MEMS component, the transmission line characteristic impedance, electrical length, and the attenuation constant should be determined. The equations given below provide the required information to design and model a CPW [43]:

$$\varepsilon_{eff} = 1 + q(\varepsilon_r - 1) \tag{3.11}$$

$$q = \frac{\frac{K(k_1)}{K(k_1')}}{\frac{K(k_1)}{K(k_1')} + \frac{K(k_2)}{K(k_2')}} \tag{3.12}$$

$$k_1 = \frac{\tanh(\pi W/4H)}{\tanh[\pi(W+2G)/4H]} \quad , \quad k_1' = \sqrt{1-k_1^2} \tag{3.13}$$

$$k_2 = \frac{W}{W+2G} \quad k_2' = \sqrt{1-k_2^2} \tag{3.14}$$

$$Z_o = \frac{60\pi}{\sqrt{\varepsilon_{eff}}} \frac{1}{\frac{K(k_1)}{K(k_1')} + \frac{K(k_2)}{K(k_2')}} \tag{3.15}$$

where *W*, *S*, and *H* are the physical dimensions of the structure given in Figure 3.11, and *K(k)* is the complete elliptic integral of the first kind.

The total CPW attenuation constant (α_o) is composed of the attenuation due to the dielectric losses (α_d) in the substrate and the attenuation due to the conductor losses (α_c) in the center conductor, ground planes and the bottom conductor.

$$\alpha_o = \alpha_c + \alpha_d \tag{3.16}$$

The attenuation due to the dielectric loss can be defined as:

$$\alpha_d = \frac{8.686\pi f}{c} \frac{\varepsilon_r}{\sqrt{\varepsilon_{eff}}} q' \tan\delta_e \tag{3.17}$$

where $\tan\delta_e$ is the loss tangent of the dielectric and q' is evaluated as

$$q' = \frac{K(k_3)}{2K(k_3')} \frac{K(k_2')}{K(k_2)} \tag{3.18}$$

$$k_3 = \frac{\sinh(\pi W/4H)}{\sinh[\pi(W+2G)/4H]} \ , \ k_3' = \sqrt{1-k_3^2} \tag{3.19}$$

The losses due to the conductors of CPW are expressed as follows:

$$\alpha_c = 8.686 \frac{R_C + R_G}{2Z_o} \text{ dB/m} \tag{3.20}$$

where R_C is the series resistance of the center conductor and R_G is the distributed series resistance of the ground planes in ohms per unit length. R_C and R_G can be found by:

$$R_C = \frac{R_s}{4W\left(1-k_2^{\,2}\right)K^2(k_2)}\left(\pi + \ln\left(\frac{4\pi W}{t}\right) - k_2 \ln\left(\frac{1+k_2}{1-k_2}\right)\right) \tag{3.21}$$

$$R_G = \frac{k_2 R_s}{4W\left(1-k_2^{\,2}\right)K^2(k_2)}\left(\pi + \ln\left(\frac{4\pi W}{t}\right) - \frac{1}{k_2} \ln\left(\frac{1+k_2}{1-k_2}\right)\right) \tag{3.22}$$

$$R_s = \frac{1}{\delta\sigma}\ ,\ \delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{3.23}$$

where t is the metallization thickness and R_s is the surface resistance, and σ is the conductivity of the metal.

The switch structures in this chapter are designed on *G/W/G* = 25 µm/170 µm/25 µm CPW on a glass substrate with ε_r = 4.6, $\tan\delta_e$ = 0.005, H = 500 µm. Ground-to-Ground spacing of CPW of the switch is selected as 220 µm considering the pitch spacing of the RF probes of the measurement setup. Using (3.11)-(3.23), the characteristic impedance, effective permittivity, and the total attenuation constant are found as 50.3 Ω, 2.8, 35.5 dB/m, respectively.

3.4.2. Modeling of the Switch in the Upstate

The bridge capacitance in the upstate, C_{bu}, including the fringe capacitance formed between the center conductor of the CPW line and the bridge can be calculated using the equation given below [44]:

$$C_{bu} = \varepsilon_0 \left[1.15\left(\frac{W.w}{h_{equ}}\right) + 2.8.(w+W)\left(\frac{t}{h_{equ}}\right)^{0.222} + 4.12.h_{equ}\left(\frac{t}{h_{equ}}\right)^{0.728} \right] \tag{3.24}$$

$$h_{equ} = g + \frac{t_d}{\varepsilon_r} \tag{3.25}$$

where t is the metallization thickness, t_d is the thickness of the isolation dielectric, ε_o is the free-space permittivity, and ε_r is the dielectric constant of the isolation dielectric.

The upstate capacitance is effective on the reflection coefficient of a switch:

$$S_{11} = \frac{-j\omega C_{bu} Z_o}{2 + j\omega C_{bu} Z_o} \tag{3.26}$$

and for $S_{11} \leq -10$ dB or $\omega C_{bu} Z_o << 2$ we have:

$$\left|S_{11}\right|^2 \cong \frac{\omega^2 {C_{bu}}^2 Z_o^2}{4} \tag{3.27}$$

Figure 3.12 shows the reflection characteristics plotted using (3.27) for bridge widths of 50 µm and 80 µm. The capacitance values are calculated using (3.24). The analysis shows that the increase in the loading capacitance results in the increase of

the reflected power. Hence, keeping the bridge width as low as possible is desirable to lower the return loss value. However, reducing the bridge width increases the actuation voltage and decreases the downstate capacitance, both of which are detrimental on the switch performance.

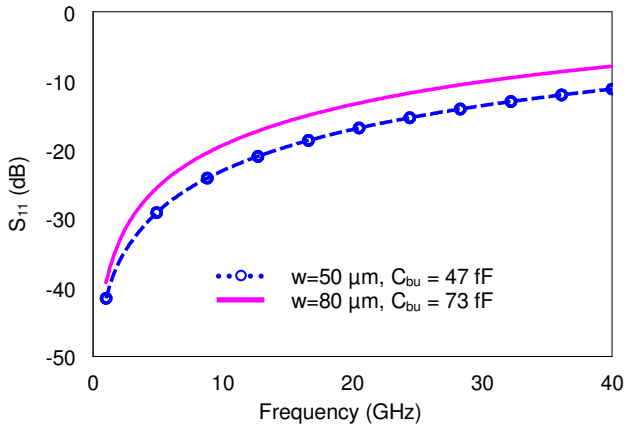
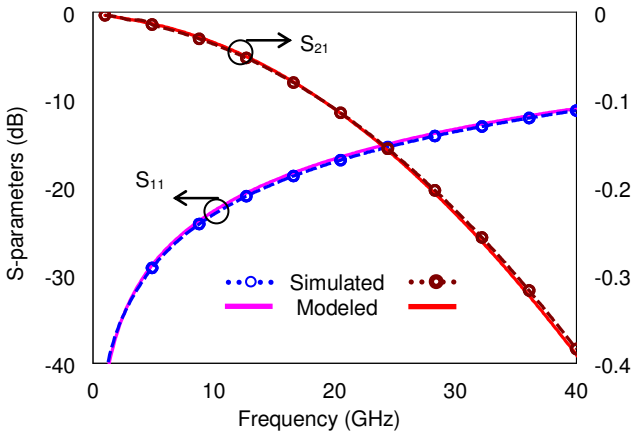
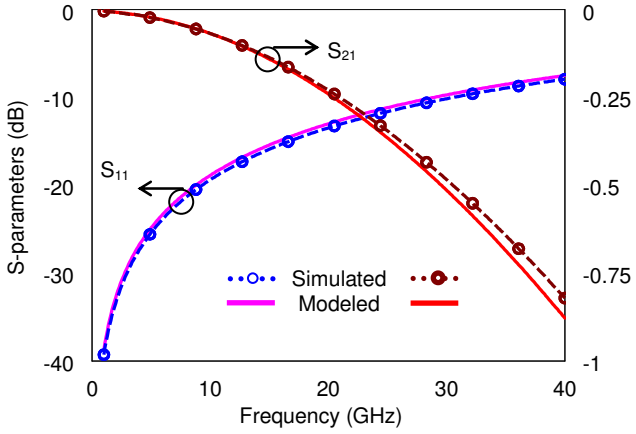


Figure 3.12 The effect of the bridge capacitance on the reflection coefficient of RF MEMS shunt switches in the upstate for bridge widths of 50 µm and 80 µm.

Ansoft HFSS simulations for the upstate of the switch show a good agreement with the CPW equations in Section 3.4.1 and upstate bridge capacitance formulation in (3.24). Figure 3.13 shows the S-parameter results of the circuit model and the simulations performed by Ansoft HFSS for 50 µm and 80 µm bridge widths. Table 3.1 gives the circuit parameters found from the mentioned equations. The bridge inductance and resistance are ignored since they have nearly no effect on the upstate performance of the switch.



(a)



(b)

Figure 3.13 Simulated and modeled S-parameters for a shunt switch in the upstate with bridge width of (a) 50 µm (b) 80 µm.

Table 3.1 The model parameters for the upstate of RF MEMS shunt switches with bridge widths of 50 µm and 80 µm.

Parameter	w=50 µm	w=80 µm
C_{bu}	47 fF	74 fF
Z_o	50 Ω	50 Ω
ε_{eff}	2.8	2.8
α_o @ 10 GHz	35 dB/m	35 dB/m

3.4.3. Modeling of the Switch in the Downstate

The MEMS bridge capacitance in the downstate can be easily calculated using the parallel plate formulation neglecting the fringe capacitance since the thickness of the dielectric, t_d, is so small.

$$C_{bd} = \frac{\varepsilon_r \varepsilon_o W w}{t_d} \tag{3.28}$$

The downstate capacitance of a shunt switch directly determines the isolation performance of the switch, which is evaluated from the transmission coefficient of a switch, S_{21}. The transmission coefficient of the switch, when the losses of the transmission line, the bridge inductance (L), and the resistance (R) are ignored, can be expressed as follows:

$$S_{21} = \frac{1}{1 + j\frac{\omega C Z_o}{2}} \tag{3.29}$$

$$\left|S_{21}\right|^2 = \frac{1}{1 + \frac{\omega^2 C_{bd}{}^2 Z_o{}^2}{4}} \tag{3.30}$$

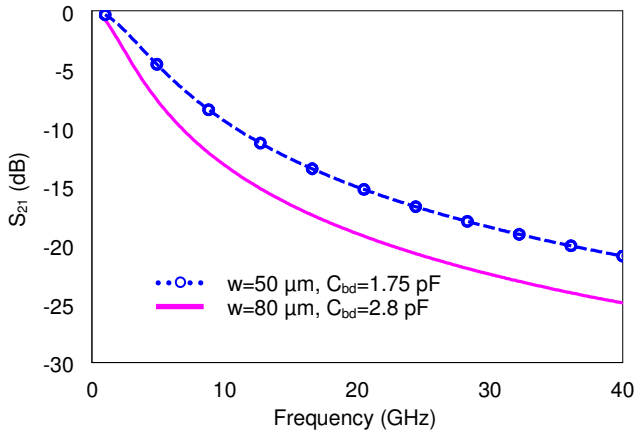


Figure 3.14 The effect of the bridge capacitance on the transmission coefficient of RF MEMS shunt switches in the upstate for bridge widths of 50 µm and 80 µm.

Figure 3.14 shows the isolation of an RF MEMS shunt switch plotted using (3.30) for bridge width of 50 µm and 80 µm. The bridge inductance shows its effect particularly for the frequencies greater than $f_o/2$ where f_o is the LC resonant frequency. Taking the inductance into account and neglecting the bridge resistance, the transmission coefficient of the switch can be expressed as:

$$S_{21} = \frac{1}{1 - j\dfrac{j\omega C_{bd} Z_o}{2\left(\omega^2 LC_{bd} - 1\right)}} = \frac{1}{1 - j\dfrac{j\omega C_{bd} Z_o}{2\left(\omega^2/\omega_o{}^2 - 1\right)}} \tag{3.31}$$

$$\left|S_{21}\right|^2 = \frac{1}{1 + \dfrac{\omega^2 C_{bd}{}^2 Z_o{}^2}{4\left(\omega^2/\omega_o{}^2 - 1\right)^2}} \tag{3.32}$$

where $\omega_o = 2\pi f_o$, the resonant frequency in radians/sec. The transmission coefficient given in (3.32) becomes zero for $\omega = \omega_o$ yielding infinite isolation at that frequency.

This knowledge on the improvement of isolation constitutes the basic idea of inductively tuned switches which will be further analyzed in the next sections.

The bridge resistance models the losses on the bridge. It can be evaluated from the value of transmission coefficient at resonance since the shunt branch reduces to the bridge resistance only at that frequency. A simulation or a measurement is required to extract the bridge resistance using the expression below:

$$S_{21}\big|_{\omega_o} = \frac{2R}{Z_o} \tag{3.33}$$

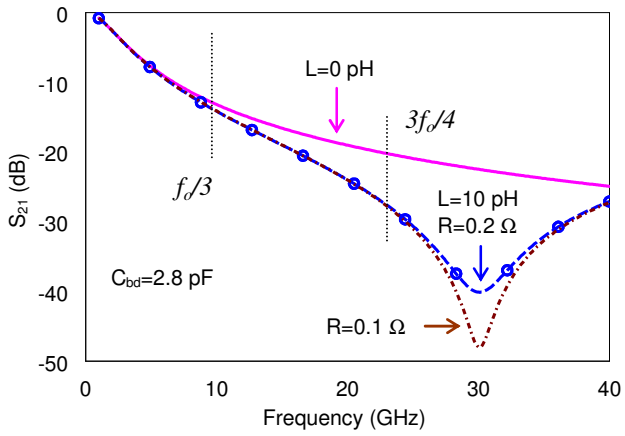


Figure 3.15 The effect of the bridge inductance on the isolation of the switch at downstate.

Figure 3.15 shows the effect of the bridge inductance and resistance on the isolation characteristics for C_{bd} = 2.8 pF. Comparing the responses for L = 0 pH and L = 10 pH, it can be noted that the capacitance controls the response up to ~$f_o/3$ (up to 10 GHz in this case). The inductance significantly affects the slope of S_{21} after $f_o/2$-$f_o/3$. The bridge resistance controls the deep amplitude and the sharpness of the

characteristics around resonant frequency. The amplitudes at the resonant frequency are -48 dB and -40 dB for bridge resistances of 0.1 Ω and 0.2 Ω, respectively. The bridge resistance has no effect on the isolation characteristics for $f < 3f_o/4$ and it can only be extracted using measurements around the resonant frequency. It should be noted here that in order to measure a resistance of 0.1 Ω, an excellent calibration is compulsory for measuring a transmission coefficient of about -50 dB.

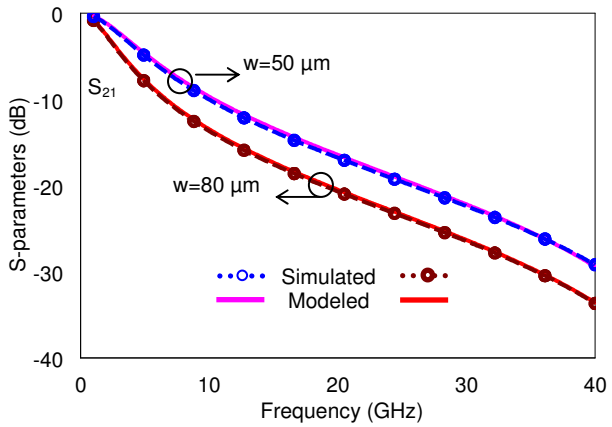


Figure 3.16 Ansoft HFSS simulation and circuit model results for RF MEMS shunt switches in the downstate with bridge widths of 50 µm and 80 µm.

Figure 3.16 shows the EM simulation by HFSS and circuit model results for the downstate of the switches with for bridge widths of 50 µm and 80 µm. The isolation of the switch with 80 µm bridge is better due to its increased downstate capacitance. Table 3.2 shows the circuit model parameters for these structures. The inductance and resistance are found by curve fitting to the simulations. The inductance of the structure with 80 µm bridge width is lower than that of the structure with 50 µm bridge width. The bridge inductance is mainly determined by the portion of the bridge over the CPW gaps and is not dependent on the portion of the bridge over the center conductor since the current distribution of CPW line is concentrated at the

edges of the signal and ground planes. Increasing the bridge width over the CPW gaps reduces the induced voltage on the bridge due to its reduced impedance. Hence, this induction can be modeled with a smaller inductance in the shunt branch. It should be noted here that the METU RF MEMS group have recently developed an empirical formulation for the evaluation of the bridge inductance [45]. These formulations will be presented in the following section.

Table 3.2 The calculated and extracted model parameters for the downstate of the RF MEMS shunt switches with bridge widths of 50 and 80 μm.

Parameter	w = 50 μm	w = 80 μm
C_{bd}	1.75 pF	2.8 pF
L_{bd}	5.7 pH	3.6 pH
R_{bd}	0.15 Ω	0.15 Ω
Z_o	50 Ω	50 Ω
ε_{eff}	2.8	2.8
α_o @ 10 GHz	35 dB/m	35 dB/m

3.5. Inductively Tuned Shunt Switches

This part of the chapter focuses on the inductively tuned RF MEMS shunt switches to achieve high-isolation in *Ku*-band. One of the most important performance criteria of a MEMS switch is the isolation of the switch and its bandwidth. The isolation characteristics of conventional MEMS shunt switches show an *LC* resonant behavior at the mm-wave frequency band. In order to achieve an isolation better than 20 dB at *X*- and *Ku*-band frequencies with these switches, one should increase either the bridge capacitance or the bridge inductance (or both at the same time). However the bridge capacitance is limited due to some reasons such as area miniaturization considerations, surface roughness of the used materials, and fabrication difficulties of

the suspended structures with large areas. The bridge inductance of a conventional MEMS switch is around 5-10 pH but it can be increased up to 60-70 pH by properly modifying the geometry, which is referred as the inductive tuning of a MEMS switch [9]. Therefore, increasing the bridge inductance is an appropriate way of tuning the isolation bandwidth of MEMS shunt switches to *X*- or *Ku*-band.

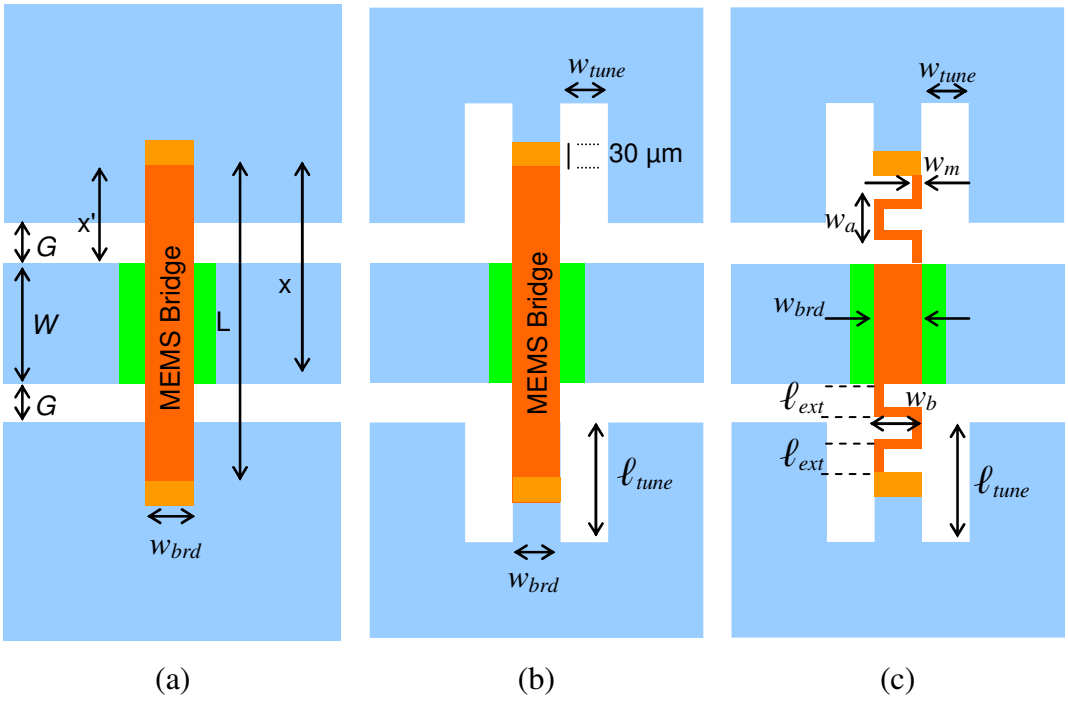


Figure 3.17 The schematic top view of the RF MEMS capacitive shunt switches (a) standard fixed-fixed beam (Type A) (b) inductively tuned switch with the recesses in the ground plane (Type B) (c) inductively tuned switch with both recessed ground plane and meanders supporting bridge (Type C).

3.5.1. Sample Inductively Tuned Switch Designs

Figure 3.17 and Table 3.3 show the top-view and dimensions of the switches, respectively. Type A group switches have standard fixed-fixed beams whereas Type

B group switches have recesses in the ground plane. Type B switches have bridge widths of 50 µm and 100 µm, recess widths of 40 and 60 µm with recess depths of 25, 50, and 100 µm. Type C switch group has bridges supported by meanders acting as an additional inductance to the bridge. The primary and secondary meander lengths are defined as w_a (60 µm for both C-1 and C-2) and w_b (100 µm for C-1 and 160 µm for C-2), respectively. The meanders have a width of w_m = 20 µm which is kept as small as possible to introduce the highest possible inductance. All switches are implemented on CPW with dimensions of *G/W/G* = 25/170/25 µm (50 Ω).

Table 3.3 Dimensions and simulated circuit parameters for the switches (Z_o = 50 Ω, ε_{eff} = 2.78, α_o = 35 dB/m, ℓ_o = 150 µm).

	w	L_{tune}	w_{tune}	$C_{u,sim}$	$C_{bd,sim}$	L_b	R	L_g
Type A-1	50 µm	-	-	47 fF	1.75 pF	5.7 pH	0.1 Ω	0
Type A-2	80 µm	-	-	73 fF	2.8 pF	3.6 pH	0.1 Ω	0
Type B-1	50 µm	100 µm	40 µm	47 fF	1.75 pF	18.8 pH	0.1 Ω	15 pH
Type B-2	50 µm	50 µm	40 µm	47 fF	1.75 pF	11.4 pH	0.1 Ω	12 pH
Type B-3	50 µm	25 µm	40 µm	47 fF	1.75 pF	8.3 pH	0.1 Ω	6 pH
Type B-4	100 µm	150 µm	40 µm	90 fF	3.5 pF	17.2 pH	0.08 Ω	25 pH
Type B-5	100 µm	150 µm	60 µm	90 fF	3.5 pF	20 pH	0.06 Ω	35 pH
Type C-1	100 µm	150 µm	60 µm	90 fF	3.5 pF	49.8 pH	0.2 Ω	35 pH
Type C-2	160 µm	150 µm	60 µm	142 fF	5.6 pF	61.7 pH	0.2 Ω	55 pH

3.5.2. Circuit Model for Inductively Tuned Switches

Figure 3.18 shows the circuit model for the RF MEMS switches proposed for the inductively tuned switches, which is quite similar to the one given in Section 3.4.

The model consists of two 50 Ω transmission lines, a shunt *CLR* impedance for the bridge and two series inductances. The bridge inductance in the shunt arm, L_b, is denoted as three different inductances for three types of switches. The series inductor, L_g, models the discontinuity associated with the recesses in the ground plane of Type B and C switches. This element of the model particularly provides accurate modeling of the upstate characteristics of Type B and C switches. Table 3.3 presents the parameters of the model where the parameters except the inductance, L_g, and bridge resistance, R_b are evaluated by means of the expressions given below. The inductance, L_g, and the bridge resistance, R_b, are found by curve fitting to the Ansoft HFSS simulations. The relationship between bridge inductance, L_b, and physical dimensions are extracted empirically with curve fitting to the EM simulation results. It should be noted here that it is the first attempt in literature, to express the bridge inductance analytically in terms of physical dimensions.

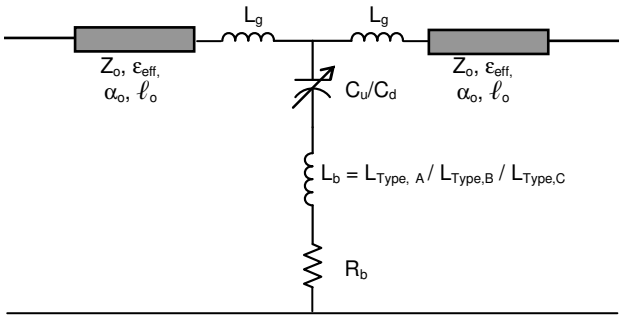


Figure 3.18 The modified *CLR* model for the switches with recessed ground.

The bridge inductance models the voltage induced on the bridge due to the current flowing to the ground planes. As mentioned before, the inductance is determined by the portion over the gaps of the CPW since the fields are concentrated at the gaps, and there is a canceling effect for the portions of the bridge over the CPW center conductor and ground planes [8]. The inductance of the bridge can be increased by

decreasing the width (w_{brd}) and increasing the length of the bridge (ℓ_{brd}) over the CPW gaps. The bridge inductance for Type A switches, L_A, is related to the physical dimensions as:

$$L_{Type,A} = L_1 = c_1 \frac{\ell_{brd}}{w_{brd}} \tag{3.34}$$

where c_1 is an empirical coefficient and determined to be 11.4 by curve fitting using the values in Table 3.3. It should be noted here that the length of the bridge (ℓ_{brd}) over the CPW gaps is directly equal to the gap (G) of the CPW for Type A switches.

The recesses on the ground plane of Type B switches contribute to the bridge inductance. This additional inductance increases with the depth (ℓ_{tune}) and width of the recess (w_{tune}). This inductance is also affected by the width of the bridge at the anchor. As the width of the bridge at the anchor increases, the inductance decreases. The additional inductance due to the recessed ground can be expressed as

$$L_2 = c_2\left(\ell_{tune} - c_3\right)\sqrt{\frac{w_{tune}}{w_{brd}}} \tag{3.35}$$

where c_2 and c_3 are empirical coefficients with values of 0.16 and 7.2, respectively. The bridge inductance for Type B switches, $L_{Type,\ B}$, is the sum of L_1 and L_2 as follows

$$L_{Type,B} = L_1 + L_2 = c_1 \frac{\ell_{brd}}{w_{brd}} + c_2\left(\ell_{tune} - c_3\right)\sqrt{\frac{w_{tune}}{w_{brd}}} \tag{3.36}$$

If the width of the bridge over the gap is reduced such as in case of Type C switches, the inductance can be increased significantly. In order to express the inductance due to the meanders, (3.34) is modified as

$$L_3 = c_4 \frac{w_A + 2(w_B - w_m)^p + \ell_{ext}}{w_m} \tag{3.37}$$

where c_4 and p are empirical coefficients with values of 0.19 and 1.42, respectively. It should be noted here that for $p = 1$ the numerator of the expression is equal to the total length of the meander [Figure 3.17 (c)]. The section of the meander denoted as w_B, is perpendicular to the net current direction flowing from the bridge plate to grounds and the effect of this section is emphasized with the exponent, p.

The inductance due to the recessed ground, L_4, can be calculated using (3.35) replacing the w_{brd} with w_m. This change is crucial since the effect of recessed ground plane depends on the anchor-bridge connection as mentioned before. The bridge inductance for Type C switch, $L_{Type,\,C}$, is the sum of L_3 and L_4 as follows

$$L_{Type,C} = L_3 + L_4 = c_4 \frac{w_A + 2(w_B - w_m)^p + \ell_{ext}}{w_m} + c_2(\ell_{tune} - c_3)\sqrt{\frac{w_{tune}}{w_m}} \tag{3.38}$$

3.5.3. The Bandwidth of a Shunt Switch

The bandwidth of a shunt switch is specified considering the isolation performance. The isolation of the switch is limited by the capacitance for the frequencies lower than LC resonant frequency, f_o, and by the inductance for the higher frequencies than f_o. Both the bridge inductance, L_b, and the downstate capacitance, C_d is effective in the vicinity of f_o and specifies two boundary frequencies around the deep of the S_{21} characteristics. The bridge resistance can be ignored in the bandwidth calculations of the switch. These boundary frequencies are denoted as f_L (or ω_L) and f_H (or ω_H) and can be solved for isolation better than 20 dB ($|S_{21}|<0.1$) as follows:

$$\left|S_{21}\right| = \left| \frac{\frac{2}{Z_o}}{\frac{2}{Z_o} + \frac{j\omega C_d}{\left(\omega^2 L_b C_d - 1\right)}} \right| \leq 0.1 \tag{3.39}$$

$$S_{21}\big|_{\omega_L} = 0.1,\ S_{21}\big|_{\omega_H} = 0.1 \tag{3.40}$$

$$\omega_L = \frac{\sqrt{99}}{198L_b}\left(\sqrt{\frac{1}{C_d}\left(396L_b + 625C_d\right)} - 25 \right) \tag{3.41}$$

$$\omega_H = \frac{\sqrt{99}}{198L_b}\left(\sqrt{\frac{1}{C_d}\left(396L_b + 625C_d\right)} + 25 \right) \tag{3.42}$$

The expressions in (3.41) and (3.42) can be written for other design specifications on the isolation with a more general approach as

$$\left|S_{21}\right| \leq \frac{1}{T},\ S_{21}\big|_{\omega_L} = \frac{1}{T},\ S_{21}\big|_{\omega_H} = \frac{1}{T} \tag{3.43}$$

$$\omega_L = \frac{1}{2L_b\sqrt{T^2 - 1}}\left(\sqrt{\frac{1}{C_d}\left(4L_b\left(T^2 - 1\right) + \frac{{Z_o}^2 C_d}{4} \right)} - \frac{Z_o}{2} \right) \tag{3.44}$$

$$\omega_H = \frac{1}{2L_b\sqrt{T^2 - 1}}\left(\sqrt{\frac{1}{C_d}\left(4L_b\left(T^2 - 1\right) + \frac{{Z_o}^2 C_d}{4} \right)} + \frac{Z_o}{2} \right) \tag{3.45}$$

$$BW = \omega_H - \omega_L = \frac{1}{2L_b\sqrt{T^2 - 1}}\left(Z_o\right) \tag{3.46}$$

It is observed from (3.46) that the bandwidth of the switch is independent of the downstate capacitance, which may degrade due to the roughness of the isolation dielectric layer and insufficient contact force. The degradation of the downstate capacitance shifts the boundary frequencies, ω_H and ω_L, from the desired locations. This shift can be compensated by the increase of bridge inductance using the approaches presented in this work. The inductive tuning approaches yield 10 times improvement in the inductance compared to conventional MEMS switches without any recesses or meanders.

The increase of bridge inductance reduces the boundary frequencies down to *Ku*- and *X*-band from mm-wave. Table 3.4 gives the resonant frequency, f_o, boundary f_L, and f_H values of the switches calculated using (3.41) and (3.42). The comparison of inductive tuning effects will be fair for the designs with equal downstate capacitance. For instance, the switches Type C-1 and Type B-5 have the same downstate capacitance, which is 3.5 pF in simulations, but different bridge inductances; 20 pH and 49.8 pH, respectively. The first conclusion is that the resonant frequency for Type C-1 is lower compared to Type B-5. The second conclusion can be drawn when the reduction of downstate capacitance in real life is taken into account. Table 3.5 shows the re-calculated resonant frequency, f_L, and f_H values for Type B-5 and Type C-1 switches with the capacitance values are assumed to 40% of the simulated ones. According to Table 3.5, Type B-5 switch can not provide 20 dB isolation below 26 GHz. However Type C-1 can operate between 18 GHz and 26.4 GHz with the aid of inductive tuning. The bandwidth for Type C-1 can even be extended to 12 GHz-40 GHz if 10 dB isolation is permissible depending on the application. These results show that inductive tuning can be used to reduce the effects of the capacitance degradation, which is unavoidable due to the non-idealities such as surface roughness and low contact forces.

Table 3.4 Resonant frequency (f_o) and boundary frequencies (f_L, and f_H) of the switches.

	f_o	f_L	f_H
Type A-1	50.1 GHz	26.1 GHz	96.7 GHz
Type A-2	49.9 GHz	19.3 GHz	131 GHz
Type B-1	27.6 GHz	18.7 GHz	40.3 GHz
Type B-2	35.6 GHz	21.6 GHz	57.3 GHz
Type B-3	42 GHz	24.1 GHz	73.1 GHz
Type B-4	20.4 GHz	11.7 GHz	35.9 GHz
Type B-5	19.1 GHz	11.3 GHz	32.6 GHz
Type C-1	12 GHz	8.6 GHz	16.7 GHz
Type C-2	8.4 GHz	5.8 GHz	12.4 GHz

Table 3.5 Re-calculated resonant frequency, f_o, boundary frequencies, f_L, and f_H values for the switches Type B-5 and C-1 for measured capacitance values

	f_o	f_L	f_H
Type B-5	34.7 GHz	26.2 GHz	42 GHz
Type C-1	22 GHz	18 GHz	26.4 GHz

3.5.4. Mechanical Considerations on the Meandered Bridges

The effective spring constant of a fixed-fixed beam (Type A and B), $k_{Type\text{-}A,B}$. with the force distributed at the center, from x to L-x on Figure 3.17, is given by (3.4). For 1-µm thick sputtered gold switch (E = 78 GPa, ν = 0.44) with L = 300 µm, x = 235

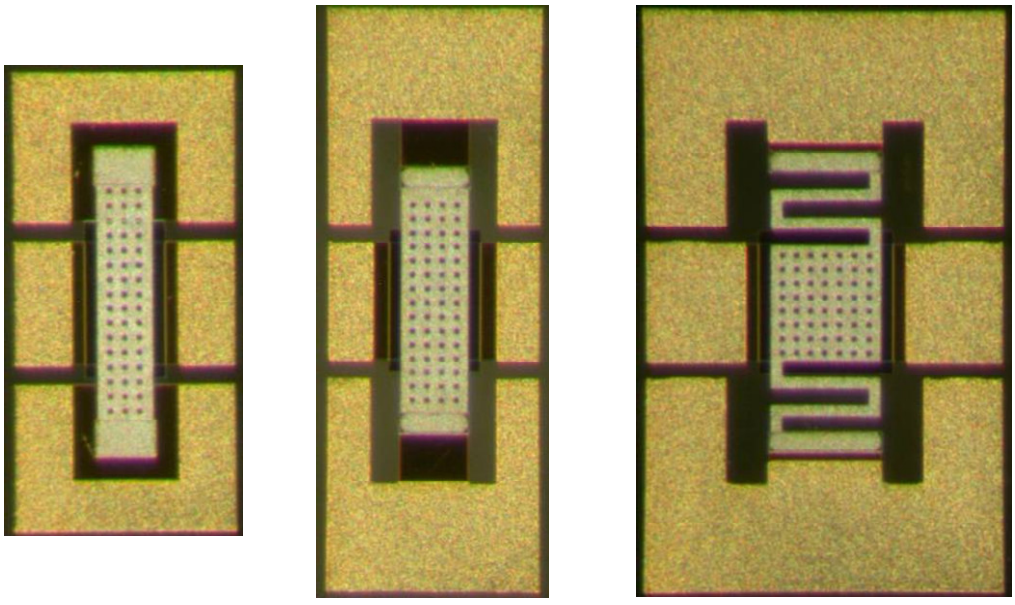
µm, g = 2.1 µm, w = 80 µm (Type A-2), and σ = 15 MPa, the spring constant value from (3.4) and the pull-in voltage value from (3.10) is found as 17.3 N/m and 19.8 V, respectively. Type C switches have lower spring constants which can be calculated as [46]:

$$k_{Type-C} = \frac{2Ew\left(\frac{t}{w_a}\right)^3}{1+\frac{w_b}{w_a}\left[\left(\frac{w_b}{w_a}\right)^2+\frac{12(1+\nu)}{1+\left(\frac{w_m}{t}\right)^2}\right]} \tag{3.47}$$

where w_a are the primary meander length, w_b is the secondary meander length, and w_m is the width of the meanders. The spring constant for the switch Type C-2, where w_a = 60 µm w_b = 160 µm, w_m = 20 µm, is equal to 0.72 N/m. Although the effect of the residual stress in low spring constant beams is not taken into account in (3.47), it can be deduced that $k_C < k_{A,B}$. The restoring force acting on the beam to come back to upstate after the DC bias is removed is also very low for low-k beams. Therefore Type C switches are more vulnerable to stiction due to dielectric charging and humidity. The fabrication results show that Type C switches can not come back to upstate after first actuation due to their low spring constant. The annealing process step added to fabrication process enhances the restoring capability of Type C switches. The annealing process step added to fabrication process enhances the restoring capability of Type C switches. The annealing can be done by placing the samples either on a hotplate at 200 °C for 3 minutes or in an oven at 200 °C for 15 minutes.

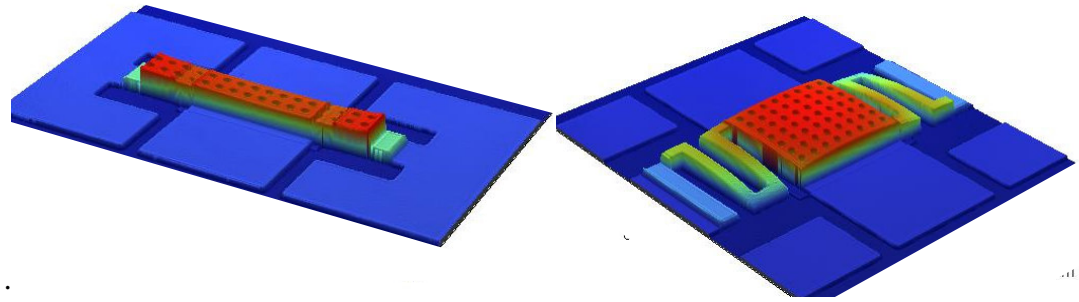
3.6. Measurement Results of Shunt Switches

This section of the chapter presents the measurement results of shunt switches with the physical dimension given in Section 3.5. Figure 3.19, Figure 3.20, Figure 3.21 shows the photographs, surface profiler images, and SEM views of the fabricated structures, respectively. The buckling of the switch with meanders is clearly illustrated in Figure 3.20 (b) which is due to the annealing step of the process. It should be noted here that this step does not affect the height fixed-fixed beam structures significantly as shown in Figure 3.20 (a). The annealing process step used to enhance the restoring capability of the switches can easily be integrated into a hermetically sealed packaging process, which requires temperatures around 200 ºC [47]-[49].



(a) (b) (c)

Figure 3.19 The photographs of the fabricated switches: (a) Type A-2 (b) Type B-5 (c) Type C-2.



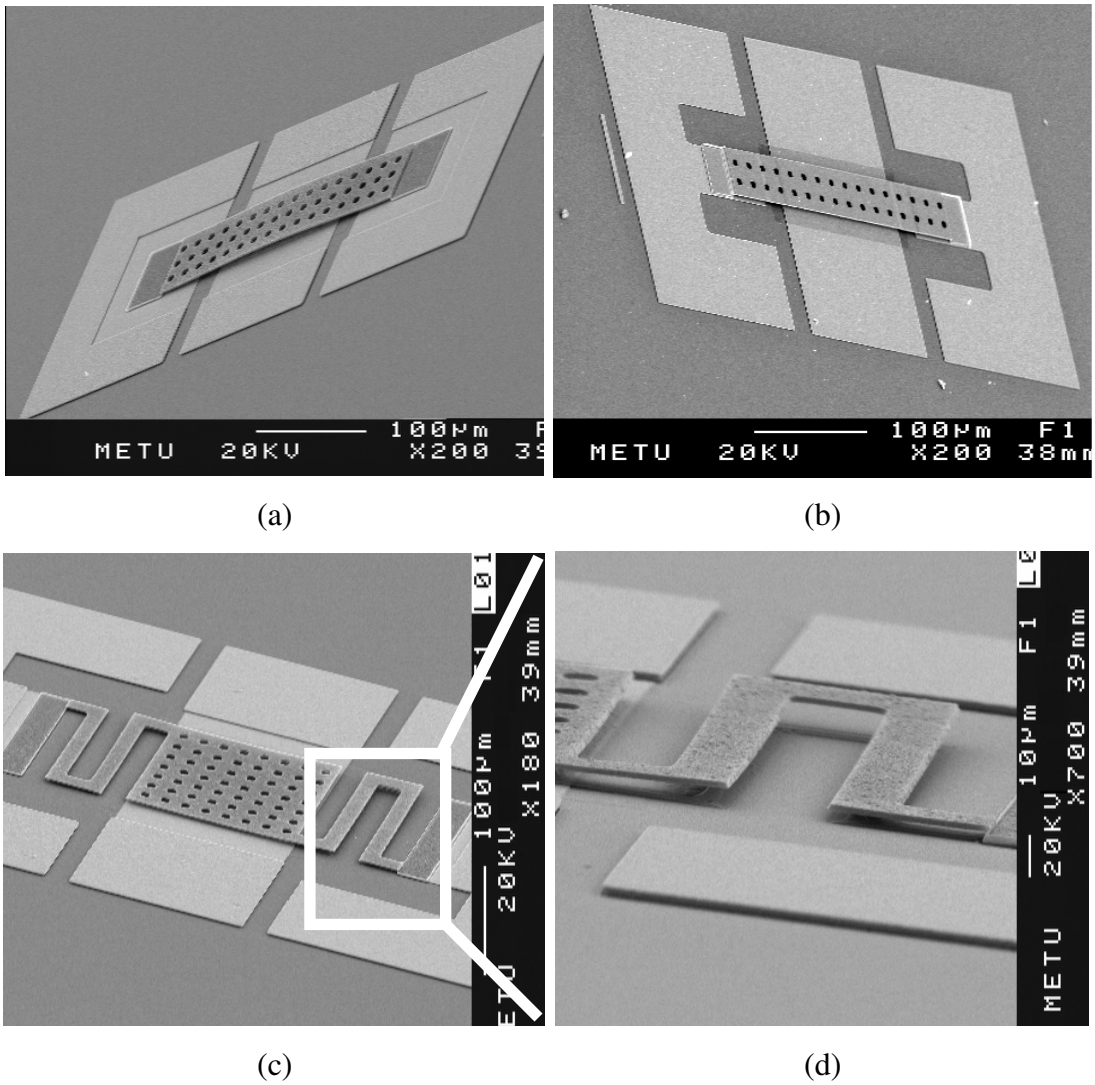
(a) (b)

Figure 3.20 The surface profiler images of the fabricated switches: (a) Type A-2 and (b) Type C-2.

The RF measurements of the switches are performed using the HP 8720 D vector network analyzer and Picoprobe 40-A-GSG-150P CPW probes with SOLT calibration [50], [51]. Picosecond 5542-230 bias-tee is used to apply the actuation voltage. Table 3.6 gives the measured bridge height and the upstate-downstate capacitance values of the switches. Type A and B group switches have bridge heights about 2-2.5 µm and a down/up capacitance ratio of about 15. The measured downstate capacitance is about 30-40 % of the simulated values.

Figure 3.22 and Figure 3.23 show the measured and modeled S-parameters for the switch Type A-2 and Type B-5. Type C group switches have increased bridge heights since they are quite sensitive to the annealing process due to the meanders. The increase in the bridge height also increases the down/up capacitance ratio. Type C-2 has the best down/up capacitance ratio, which is about 70. The upstate capacitance, which is reduced to 30 fF, is compensated with the discontinuity inductance (L_g) due to the recesses in the ground and as a consequence, the switch has a return loss better than 30 dB in 1-20 GHz band. Hence, the annealing step reduces the upstate capacitance and improves the overall performance of the switch in the upstate. Figure 3.24 gives the RF measurement results for the Type C-2 switch.

The switch has an isolation better than 20 dB between 11.1 GHz and 17.3 GHz covering nearly the whole *Ku*-band which is consistent with the formulation given in (3.41) and(3.42) for $C_{d,meas}$ = 2.08 pF, and L = 61.7 pH. The switch has an insertion loss lower than 0.4 dB up to 20 GHz.



(a) (b)

(c) (d)

Figure 3.21 SEM photographs of the fabricated structures: (a) Type A-2 (b) Type B-1 (c) Type C-2 (d) meandered section of Type C-2 switch.

The lifetime and performance of the capacitive MEMS switches are strongly affected by dielectric charging of the isolation dielectric in the downstate of the switch. Although the charging phenomenon is not well-understood yet, it is accelerated by the actuation voltage leading to two different failure modes: the stiction of the bridge and the screening of the bridge (the increase of the pull-in voltage). The lifetime of capacitive MEMS switches and dielectric charging have been investigated by various researchers [52]-[55]. It has been found that, together with the number of cycles, the amplitude of the applied voltage is one of the key parameters determining the lifetime of capacitive switches [55]. The outcomes of the dielectric charging, both screening and stiction, are also observed in our study. For the low spring constant structures (Type C switches), the stiction problem is encountered after first actuation if the samples are not annealed. The screening effect is common for all types of switches. The shift of the pull-in voltage increases if the applied voltage is increased due to the higher amount of charges injected in the dielectric. The screening problem is reduced if polarity of the actuation is altered after each actuation. The switch structures are tested in the life-time setup at METU up to 80×10^6 cycles with a bipolar actuation waveform. These tests were performed by Halil Ibrahim Atasoy in Milimeter-wave Laboratory at METU Department of Electrical and Electronics Engineering.

Table 3.6 Measured bridge height, measured up and downstate capacitance values of the switches.

	h	$C_{up,meas}$	$C_{d,meas}$	$C_{d,meas}/C_{d,sim}$	$C_{d,meas}/C_{up,meas}$
Type A-1	2.5 µm	38.5 fF	650 fF	0.37	16.8
Type A-2	2.1 µm	69.8 fF	926 fF	0.33	13.2
Type B-1	2.5 µm	38.5 fF	597 fF	0.34	15.5
Type B-2	2.5 µm	38.5 fF	597 fF	0.34	15.5
Type B-3	2.5 µm	38.5 fF	667 fF	0.38	17.3
Type B-4	2 µm	90 fF	1.17 pF	0.3	13
Type B-5	2 µm	90 fF	1.3 pF	0.27	14.4
Type C-1	5 µm	39 fF	1.1 pF	0.33	28.2
Type C-2	11 µm	30 fF	2.08 pF	0.38	69.3

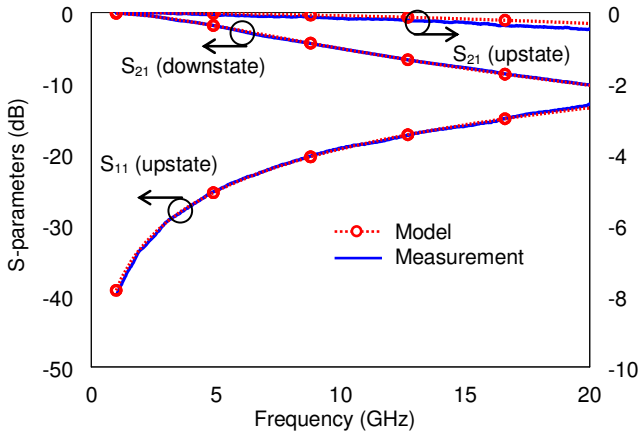


Figure 3.22 The measurement results for the switch denoted as Type A-2.

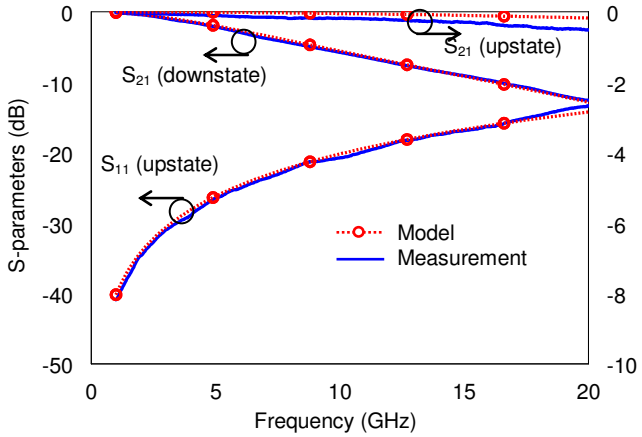


Figure 3.23 The measurement results for the switch denoted as Type B-5.

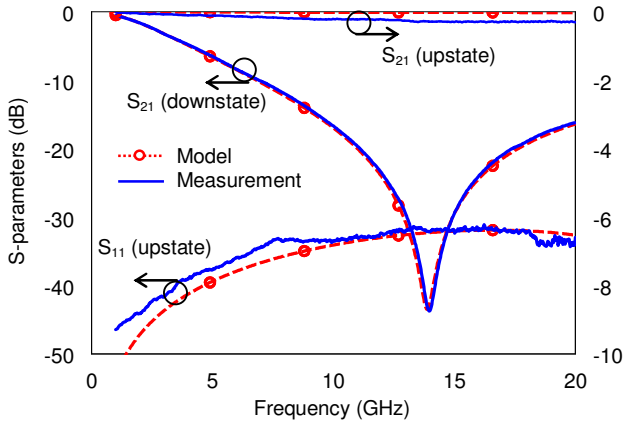


Figure 3.24 The measurement results for the switch denoted as Type C-2.

Figure 3.25 shows the change of the downstate capacitance with respect to the applied actuation voltage up to 80 V for the switch Type C-2, which has a pull-in voltage of 17 V. The capacitance values are extracted from the isolation measurements at different actuation voltage. The use of 40 V instead of 80 V as the actuation voltage seems to be the best compromise to reduce the dielectric charging effects since the capacitance value already reaches already to 80 % of the highest measured value (2.1 pF at 80 V) at 40 V (1.74 pF).

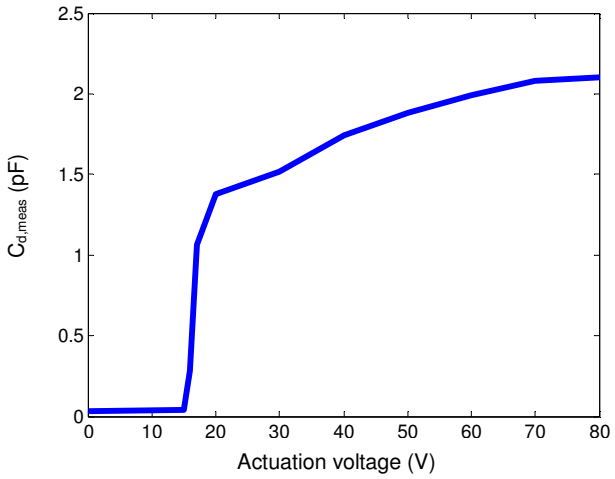


Figure 3.25 The characteristics of the downstate capacitance vs. actuation voltage for the switch Type C-2.

To summarize, increasing the bridge inductance of RF MEMS shunt switches is an appropriate way of tuning the isolation bandwidth of these switches to *X*- or *Ku*-band instead of increasing the capacitance or using additional shunt switches. The bridge inductance is increased by 10 times compared to conventional MEMS switch designs by the use of recesses and meanders at the same switch design. The relationship between the bridge inductance and physical dimensions are extracted empirically to obtain analytical expressions for the bridge inductance. The switches having meanders fabricated without annealing process can not come back to upstate after the DC bias is removed since they are vulnerable to stiction due to charging and humidity. This study also shows that the adverse effect of the meanders on the restoring force can be eliminated by adding an annealing step to the fabrication.

CHAPTER IV

THEORY AND DESIGN OF DISTRIBUTED MEMS TRANSMISSION LINE PHASE SHIFTERS

4.1. Introduction

Distributed MEMS Transmission Lines (DMTLs) are used in the implementation of phase shifters [39], [40], [56], [57], resonators [58], and filters [59], which are the key components in phased arrays, radars, wireless communication systems, and measurement instruments. The implementation of DMTLs employs the idea of periodically loading a high-impedance transmission line with reactive loading elements. Generally, the loading elements are tunable RF MEMS bridges, forming a transmission line with adjustable parameters [3].

Distributed MEMS structures are implemented on both CPW and microstrip lines. Figure 4.1 and Figure 4.2 show DMTL structures with CPW and microstrip topology, respectively. Due to ease of implementation, CPW is the most preferred transmission line. The phase shifter structure of the phased array in this work is also in CPW topology.

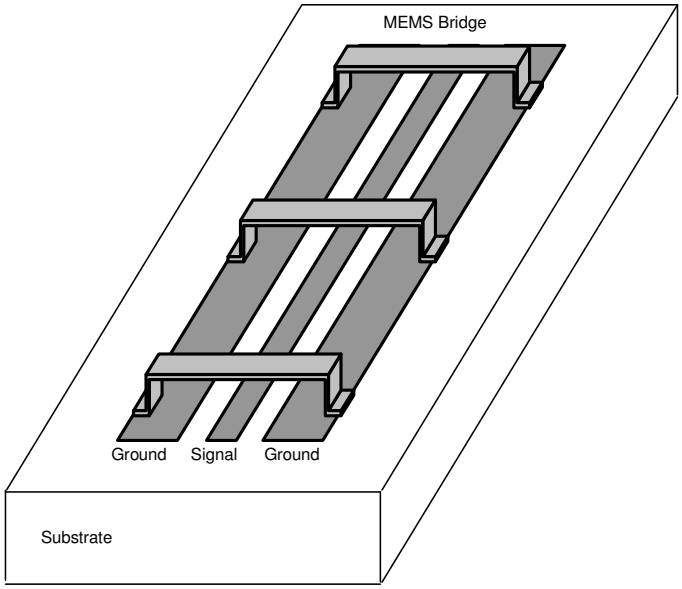


Figure 4.1 The DMTL structure with CPW topology.

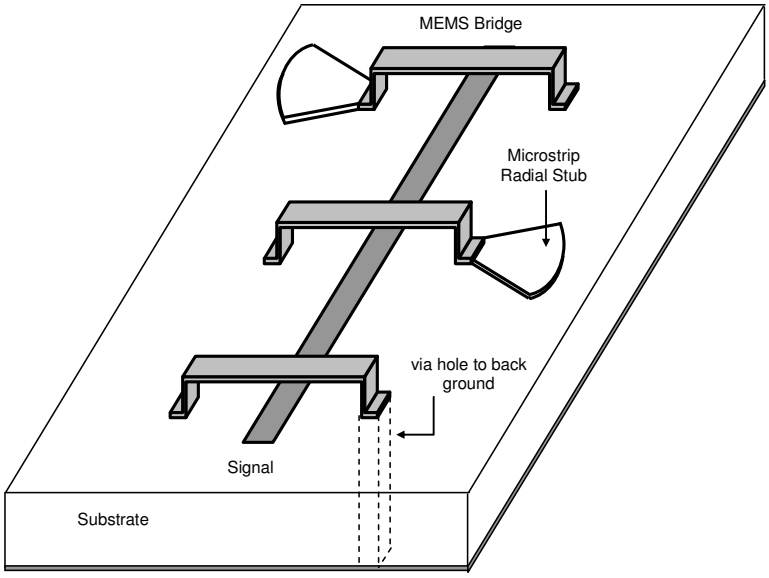


Figure 4.2 The DMTL structure with microstrip topology. The bridges are coupled to the ground either using an open circuited stub or via hole.

This chapter is composed of mainly two parts: Theoretical background required for the design of the phase shifter is given at the first part, which includes the definition of the propagation properties such as the characteristic impedance, the phase velocity, and the Bragg frequency of a loaded line structure followed by the closed-form design equations of the DMTL structure. The second part presents the digital phase shifter structure used in the phased array. Based on the background of the first part, the design equations are provided for the digital RF MEMS phase shifter. The measurement results and post-fabrication observations of the fabricated phase shifters are also given. The chapter is finalized with the comments about digital phase shifter designs on various substrates and scaling these designs to higher frequencies.

4.2. Loaded Transmission Line Parameters

Figure 4.3 shows the lumped equivalent circuit of a two-conductor transmission line with a length of dz, where R_t, L_t, C_t, and G_t are the per unit length resistance (due to the transmission line conductor losses), inductance (self inductance of the two conductors), capacitance (due to the proximity of the conductors), and conductance (due to the dielectric loss of the substrate where the transmission line is located), respectively. The characteristic impedance, Z_o, the attenuation constant, α, the phase constant, β, and the propagation velocity, υ_p, of a low-loss line is:

$$Z_o \cong \sqrt{\frac{L_t}{C_t}} \tag{4.1}$$

$$\alpha = \frac{R_t}{2Z_o} + \frac{G_t Z_o}{2} \tag{4.2}$$

$$\beta = \omega\sqrt{L_t C_t} \tag{4.3}$$

$$v_p = \frac{1}{\sqrt{L_t C_t}} \tag{4.4}$$

The equations (4.1)-(4.4) for the characteristic impedance, attenuation/phase constants, and propagation velocity serve the basic equations for the loaded transmission lines.

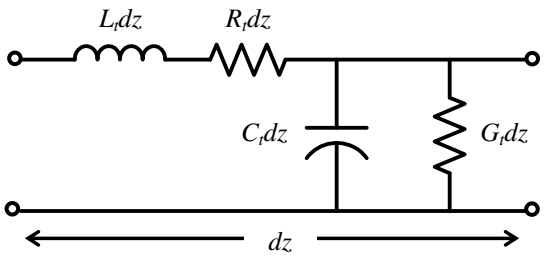


Figure 4.3 Lumped equivalent circuit model of the transmission line.

The expression for the propagation velocity in (4.4) shows that the wave can be slowed down by either increasing the capacitance per unit length or increasing the inductance per unit length (or both at the same time). Due to ease of implementation with diode varactors [60] or MEMS bridges [40], increasing the capacitance per unit length is preferred in the literature and also in this thesis. Figure 4.4 shows the DMTL unit cell where a variable MEMS capacitor is used as the loading element. The length of the unit cell, *s,* is a small fraction of the wavelength at the design frequency that enables the designer to use the given lumped element approximation of Figure 4.4 with a high accuracy [40]. The transmission line is assumed to be

lossless for simplicity at this stage. The analysis about the losses is given in the following sections.

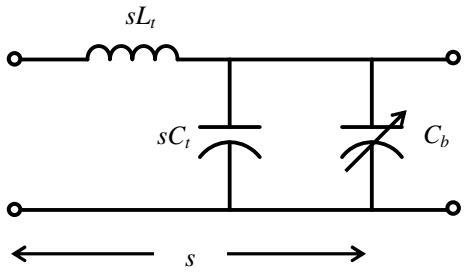


Figure 4.4 The lumped equivalent circuit model for the unit cell of a DMTL structure.

Using (4.1), the characteristic impedance, i.e., loaded line impedance, and propagation velocity for the loaded unit cell is:

$$Z_L = \sqrt{\frac{sL_t}{sC_t + C_b}} \tag{4.5}$$

$$\upsilon_p = \frac{1}{\sqrt{L_t\left(C_t + C_b/s\right)}} = \frac{s}{\sqrt{sL_t\left(sC_t + C_b\right)}} \tag{4.6}$$

where L_t and C_t are the per unit length inductance and capacitance of the unloaded transmission line, respectively. The variable capacitance has two extreme values for the upstate (C_{bu}) and downstate (C_{bd}). For a DMTL implementation with fixed-fixed beam capacitors shown in Figure 4.1, the downstate capacitance, C_{bd}, is the final value just before the pull-in of the MEMS bridge, not the actual downstate capacitance obtained after pull-in of the bridge. The characteristic impedance of the

loaded line, Z_L, can have two values, which are denoted as Z_{lu} and Z_{ld} for upstate and downstate loaded line impedances, respectively:

$$Z_{lu} = \sqrt{\frac{sL_t}{sC_t + C_{bu}}} \tag{4.7}$$

$$Z_{ld} = \sqrt{\frac{sL_t}{sC_t + C_{bd}}} \tag{4.8}$$

The MEMS bridge inductance is ignored in the model of Figure 4.4 since it has no nearly no effect on the DMTL characteristics below the Bragg frequency, which is explained below.

The characteristic impedance value of a loaded line approaches to zero as the frequency increases [61]. At a critical frequency, called as the Bragg frequency, the characteristic impedance becomes zero and no power will be delivered from one port of the loaded line to the other. The Bragg frequency is an important design parameter and can be calculated by:

$$\omega_B = \frac{2}{\sqrt{sL_t\left(sC_t + C_b\right)}} \tag{4.9}$$

Due to the Bragg phenomenon, the characteristic impedance of a loaded line structure is a frequency dependent parameter, which can be calculated as [40]:

$$Z = \sqrt{\frac{sL_t}{sC_t + C_b}}\sqrt{1 - \left(\frac{\omega}{\omega_B}\right)^2} \tag{4.10}$$

It should be noted here that the modeling the MEMS bridge with a capacitor only is not valid if the bridge width is larger than 50 μm. The METU RF MEMS group developed modeling approaches for these kind of DMTL structures which are presented in detail in [62]-[64].

4.3. Closed-Form Design Equations of DMTL Phase Shifters and Design Considerations

4.3.1. Selection of Loaded Line Impedances

In order to extract the closed-form design equations, one should specify the maximum return loss, RL_{max}, as the initial design constraint, of a DMTL structure. The return loss value at the input of a DMTL structure terminated with matched load (50 Ω) definitely depends on the frequency, hence β, and the length of the structure. The maximum return loss is defined as the return loss value when the input impedance is purely real, which is achieved when $\beta l = n\pi/2$ where n is an odd number (odd multiples of quarter-wave length transformer). For these βl values the input impedance for a DMTL with a loaded line impedance of Z_L is:

$$Z_{in} = \frac{Z_L^{\,2}}{50} \tag{4.11}$$

The reflection coefficient at the input, Γ_{in}, is related to RL_{max} and Z_{in} by:

$$\Gamma_{in} = \frac{Z_{in} - 50}{Z_{in} + 50} \tag{4.12}$$

$$20\log|\Gamma_{in}| \le RL_{\max} \tag{4.13}$$

Substituting (4.11) and (4.12) into (4.13) gives a range for the loaded line impedance, Z_L, due to the inequality in (4.13), where the boundary values of the inequality are the upstate (Z_{lu}) and downstate (Z_{ld}) loaded line impedances. These loaded line impedances are also called as optimal loaded line impedances for the specified maximum return loss value, RL_{max}.

Table 4.1 The optimal loaded line impedances for various maximum return loss values.

RL_{max}	Z_{lu} (Ω)	Z_{ld} (Ω)
-20 dB	55.3	45.2
-15 dB	59.8	41.8
-10 dB	69.4	36.0

4.3.2. Phase Shift Obtained From a Unit Cell

Having two values of loaded line impedances, a DMTL unit cell has two different phase velocities and phase constants:

$$\beta_u = \frac{\omega\sqrt{sL_t\left(sC_t + C_{bu}\right)}}{s} \quad \text{rad/m}$$
$$\beta_d = \frac{\omega\sqrt{sL_t\left(sC_t + C_{bd}\right)}}{s} \quad \text{rad/m} \tag{4.14}$$

The insertion phase between upstate and downstate of the unit cell of a DMTL phase shifter is calculated using the phase constants given in (4.14) as:

$$\Delta\phi = (\beta_u - \beta_d)s$$

$$\Delta\phi = 360 s f_o \frac{Z_o\sqrt{\varepsilon_{eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) \quad \text{degrees/section} \tag{4.15}$$

$$\Delta\phi = 360 f_o \frac{Z_o\sqrt{\varepsilon_{eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) \quad \text{degrees/m}$$

where f_o is the center frequency of operation for a DMTL phase shifter, c is the free-space velocity of light, Z_o is the characteristic impedance of the unloaded line, and ε_{eff} is the effective permittivity of the unloaded line.

4.3.3. The Loading Periodicity and the Selection of the Bragg Frequency

The Bragg frequency of a DMTL is specified in order to determine the loading periodicity, s, of the structure. Considering the expression in (4.9), the Bragg frequency gets smaller as the loading MEMS capacitance is increased. Therefore the worst case Bragg frequency of a DMTL occurs when the MEMS capacitance reaches to the value of C_{bd}. The Bragg frequency, f_B, of a DMTL can be related to downstate loaded line impedance (Z_{ld}) using (4.8) after some manipulations to obtain the periodicity:

$$s = \frac{Z_{ld}}{\pi f_B L_t} = \frac{Z_{ld} c}{\pi f_B Z_o \sqrt{\varepsilon_{eff}}} \tag{4.16}$$

Table 4.2 gives the unit cell length found using (4.16) for RL_{max} = -15 dB for different Bragg frequency choices. The phase shift per meter value of a loaded line structure is independent of the Bragg frequency as evident from (4.15). However the number of sections to obtain same phase shift from DMTL designs with different Bragg frequency change since the phase shift per unit section depends on the Bragg frequency choice due to the term 's' in the expression.

Table 4.2 The effect of the Bragg Frequency values on the unit cell length (s) for RL_{max} = -15 dB, which yields Z_{lu} = 59.8 Ω and Z_{ld} = 41.8 Ω. f_o and Z_o is selected as 10 GHz and 87.6 Ω, respectively (CPW dimensions: 70/80/70 on glass substrate).

Bragg Frequency	Unit Cell Length (μm)
$f_B = 1.5f_o$	1809
$f_B = 2.0f_o$	1357
$f_B = 3.0f_o$	904

The selection of the Bragg frequency is vital in terms of the bandwidth of the device. The expression in (4.10) serves the basis showing the frequency dependent behavior of the downstate and upstate loaded line impedances, Z_{ld} and Z_{lu}. Figure 4.5 shows the change of the loaded line impedances with frequency for DMTLs with different Bragg frequency choices. It can be deduced from this analysis that the structures with higher Bragg frequency values yield more stable loaded line impedances over a frequency band. A Bragg frequency larger than $2f_o$, where f_o is the center frequency of the design, is a proper selection for a wideband phase shifter design. The significance of the selection of the Bragg frequency becomes more obvious when the inserted phase shift characteristics is considered. Figure 4.6 shows the inserted phase shift per length (degree/cm) performance vs. frequency characteristics for different Bragg frequency choices. Due to the drift of the loaded line impedances as the frequency increases, the degree/cm characteristics shows a non-linear behavior preventing the structure to behave as a true-time delay. Considering the plot, a Bragg frequency larger than $2f_o$ yields a linear phase shift characteristics.

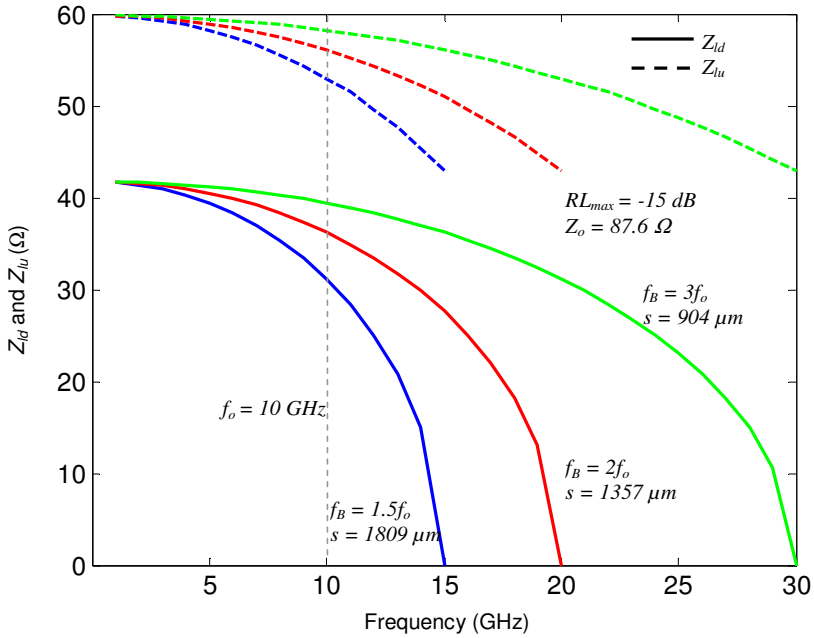


Figure 4.5. The optimal loaded line impedances vs. frequency characteristics for different Bragg frequencies. .

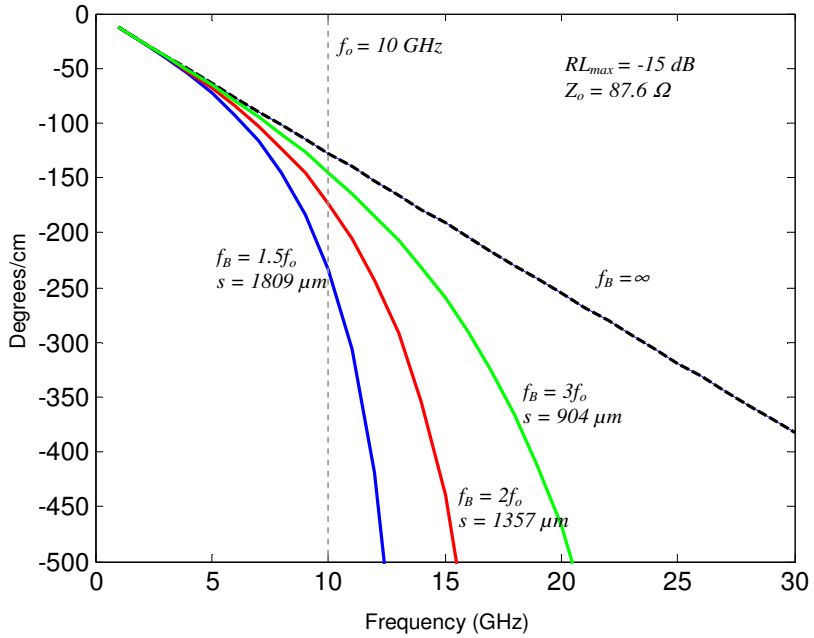


Figure 4.6. The effect of the Bragg frequency on the linearity of the degrees/cm characteristics. $f_B = \infty$ corresponds to the case Z_{lu} and Z_{ld} are independent of frequency.

4.3.4. The Calculation of the Required MEMS Bridge Capacitances

This section presents the calculation of the required MEMS bridge capacitances in order to realize the loaded line impedances. The upstate and downstate capacitances of the MEMS bridge can be extracted by substituting (4.16) into (4.7) and (4.8):

$$C_{bu} = \frac{Z_{ld}\left(Z_o^{\,2} - Z_{lu}^{\,2}\right)}{Z_{lu}^{\,2} Z_o^{\,2} \pi f_B} \tag{4.17}$$

$$C_{bd} = \frac{\left(Z_o^{\,2} - Z_{ld}^{\,2}\right)}{Z_{ld} Z_o^{\,2} \pi f_B} \tag{4.18}$$

$$C_r = \frac{C_{bd}}{C_{bu}} = \left(\frac{Z_{lu}}{Z_{ld}}\right)^2 \frac{Z_o^{\,2} - Z_{ld}^{\,2}}{Z_o^{\,2} - Z_{lu}^{\,2}} \tag{4.19}$$

The capacitance values are specified by the loaded line impedances which are controlled by the selection of RL_{max}. The characteristic impedance of the unloaded line, Z_o also plays a role in the design as an important parameter. The impact of Z_o in a DMTL design is evaluated in the next section where the losses in a DMTL structure are analyzed.

Figure 4.7 shows the downstate-upstate capacitance ratio (C_r) for different RL_{max} values. As the absolute value RL_{max} decreases, the capacitance ratio increases significantly due to increase in the range between Z_{lu} and Z_{ld}, as given in Table 4.1. The other issue that is raised by this plot is the stability of the designs over process variations. A DMTL structure designed to provide RL_{max} value of -10 dB may drift from the required loaded line impedance easily only with a few ohms of change in the unloaded line impedance, Z_o. The structures with -15 dB or -20 dB of RL_{max} are more stable against the variations of Z_o due to fabrication errors.

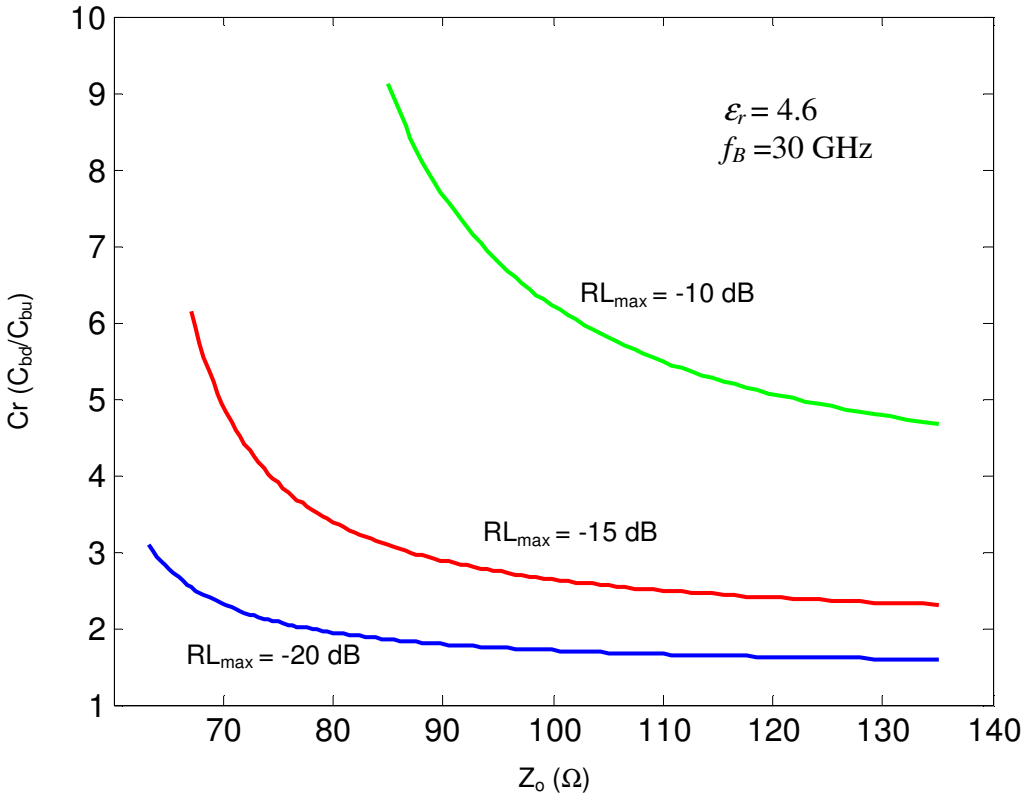


Figure 4.7. The capacitance ratio values vs. unloaded line characteristic impedance for different RL_{max} values.

4.3.5. The Losses in DMTL structures

There are two components of losses in a DMTL structures:

a) The loss due to the unloaded CPW line

b) The loss due to the bridge resistance

In order to include the loss component due the CPW line in the DMTL unit section, a resistance of sR_t, "*the series resistance per unit cell*" is inserted to the circuit model. Figure 4.8 shows the circuit model of the unit cell with a lossy CPW line. It should

be noted here that the dielectric losses of the unloaded CPW line is ignored since the dominant loss mechanism in a CPW is the conductor losses.

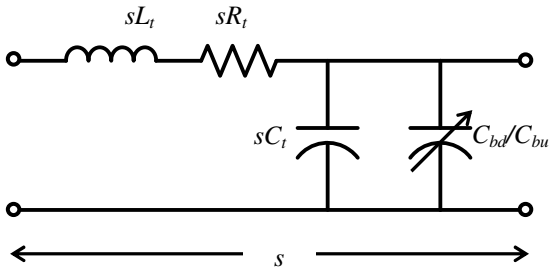


Figure 4.8. The circuit schematics of the unit cell of a DMTL where the conductor losses are modeled with a resistance of sR_t.

By considering the analogy between the models in Figure 4.3 and Figure 4.8, and using (4.2) with the dielectric loss ignored, the attenuation constant *per unit cell* of the loaded line can be expressed as:

$$\alpha_{ld} = \frac{sR_t}{Z_{ld}} \quad \text{Np/unit cell} \tag{4.20}$$

Attenuation constant of the loaded line, α_{ld}, is related to that of unloaded line using (4.2) and (4.20):

$$\alpha_{ld} = \alpha_o \frac{Z_o}{Z_{ld}} \quad \text{Np/m} \tag{4.21}$$

It should be noted here that the loss of a loaded line increases as the loaded line impedance decrease. Therefore, it is more reasonable to define the loss of a DMTL structure for the lowest loaded line impedance, which is the downstate loaded line

impedance, Z_{ld}. Figure 4.9 shows the attenuation constant of the unloaded and loaded lines vs. unloaded line characteristic impedance. The unloaded line loss, α_o, is calculated for a CPW with a ground-to-ground spacing of 220 µm at the frequency of 10 GHz. The center conductor width is swept as a parameter, keeping the ground-to-ground spacing constant, to control both the unloaded line loss and characteristic impedance. The loss and characteristic impedance values of the unloaded line and loaded line impedance for a given RL_{max} are used in (4.21) to find the loaded line loss.

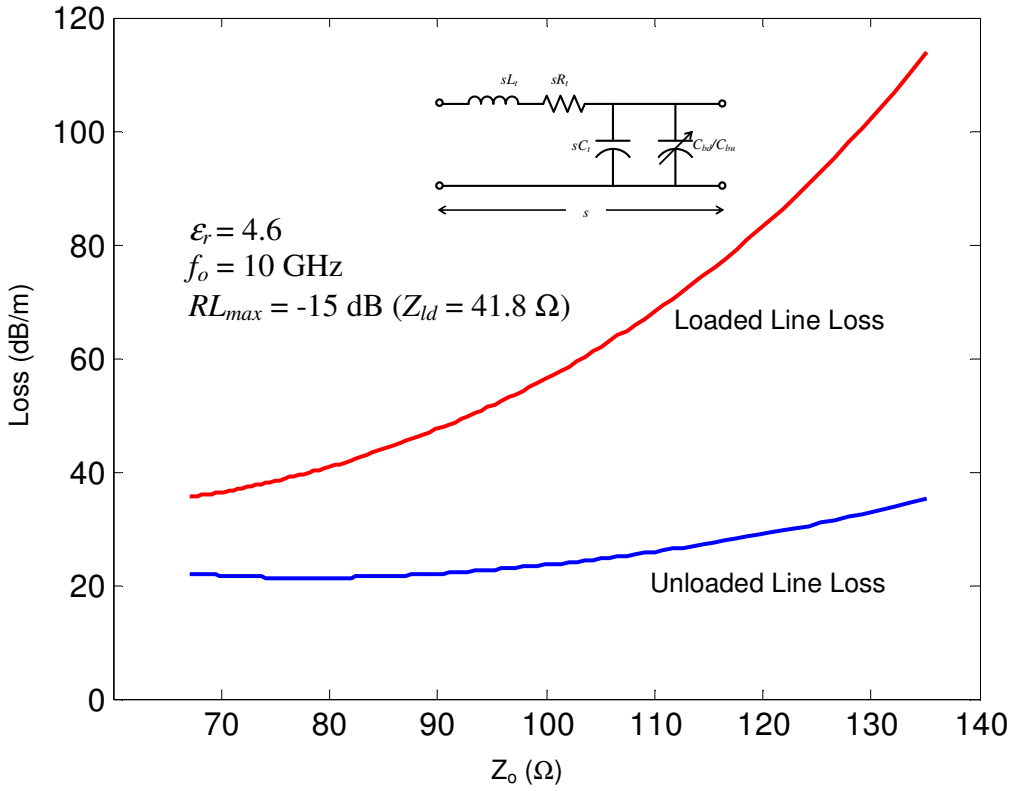


Figure 4.9. The loss of the unloaded line and loaded line vs. unloaded line characteristic impedance. The bridge loss is neglected for the analysis.

In order to extract the loss due to the bridge resistance, the circuit model given in Figure 4.10 is used, where the only loss contributor is the bridge resistance. If the wave equation for the unit cell is solved, one can obtain the attenuation and phase constants of the unit cell in Figure 4.10:

$$\gamma^2 = (\alpha + j\beta)^2 = \alpha^2 - \beta^2 + 2j\alpha\beta \tag{4.22}$$

$$\gamma^2 = j\omega sL_t\left(j\omega sC_t + \frac{j\omega C_b}{1 + j\omega C_b R_b}\right) = -\omega^2 s^2 L_t C_t - \frac{\omega^2 sL_t C_b}{1 + j\omega C_b R_b} \tag{4.23}$$

$$\beta = \omega\sqrt{sL_t(sC_t + C_b)} \quad \text{rad/unit cell} \tag{4.24}$$

$$\alpha_b = \frac{\omega^2 C_b{}^2 R_b Z_l}{2} \quad \text{Np/unit cell,} \tag{4.25}$$

where γ is the complex propagation constant, α_b is the attenuation constant per unit cell due to the bridge resistance, and β is the phase constant per unit cell, which is identical to that of the lossless loaded line presented in Section 4.2 It should be noted here that the expression for the attenuation constant due to the bridge resistance, α_b, does not include any subscripts since it is not clear from the expression which case should be interpreted as the worst case in terms of losses. To be more specific, although the loaded line impedance for upstate is higher than downstate case, the capacitances follow the reverse trend: the downstate capacitance is higher than the upstate capacitance. To clarify this point, the plot in Figure 4.11 might be helpful showing the attenuation constant due to the bridge resistance vs. the unloaded line characteristic impedance. It is evident that the loss due to the bridge is higher for the downstate of the bridge.

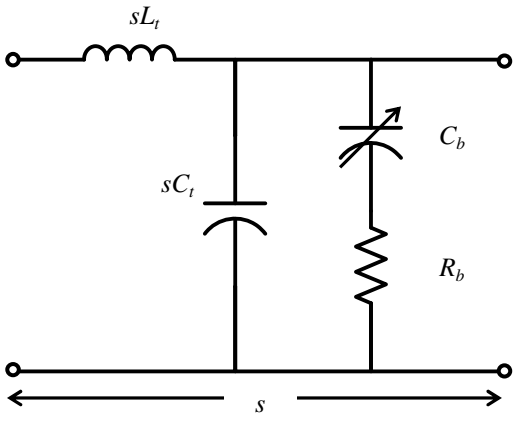


Figure 4.10. The circuit schematics of the unit cell of a DMTL where the losses due to bridge are modeled with a resistance of R_b in the shunt branch.

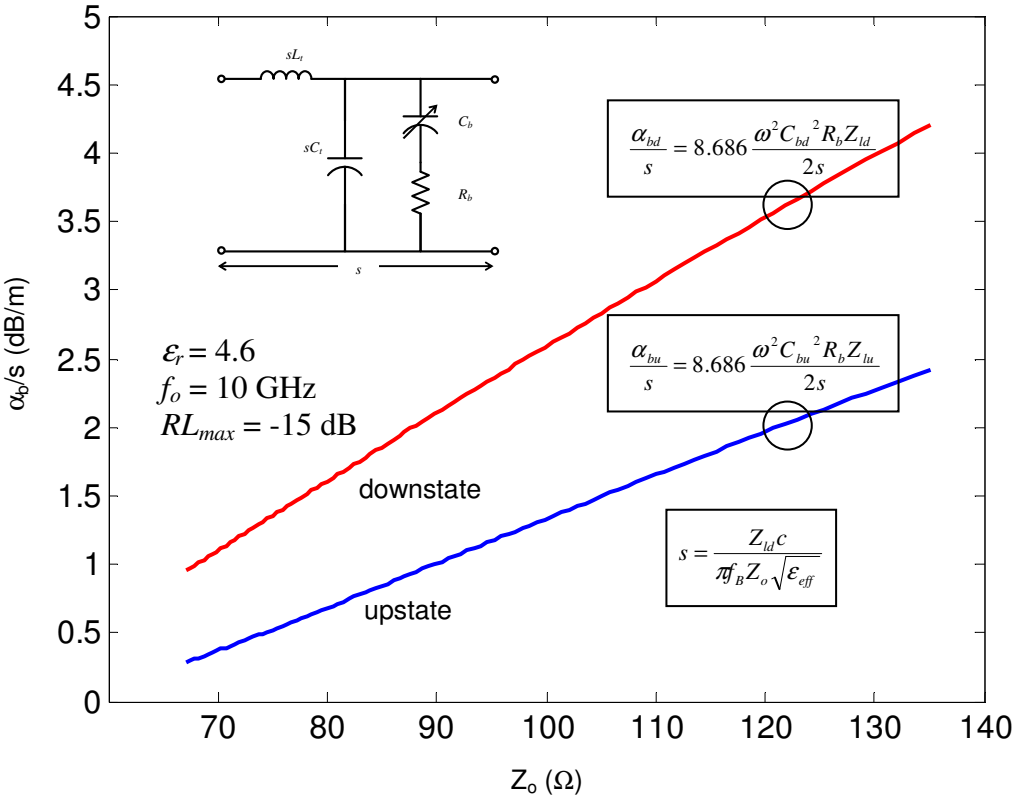


Figure 4.11. The loss *per unit length* due to the bridge resistance vs. unloaded line impedance. The unloaded line is assumed to be lossless during analysis.

The bridge loss divided by the unit cell length, α_o/s, enables us to handle the bridge loss in a distributed sense. By this approach, the loss due the bridge *per meter* can be added to the loss due to the unloaded line given in (4.21). The total loss *per meter*, in terms of dB/m, of the DMTL can be found as:

$$\alpha_{ld_total} = \alpha_{ld} + \alpha_{bd} \tag{4.26}$$

$$\alpha_{ld} = 8.686\left(\alpha_o \frac{Z_o}{Z_{ld}} + \frac{\omega^2 C_{bd}{}^2 R_b Z_{ld}}{2s} \right) \quad \text{dB/m} \tag{4.27}$$

Figure 4.12 shows the plot for the total loss vs. unloaded line characteristic impedance. The bridge loss has a negligible effect to the total loss. However, the bridge loss contributes to the total loss significantly when the bridge resistance increases or the quality factor of the loading capacitors decrease. The Q-factor point of view for the loss contribution of MEMS capacitors are beneficial when shunt bias resistors are connected to the MEMS capacitors. The effect of Q-factor of loading capacitors is detailed in the next sections for the calculation of losses of digital DMTL phase shifter design.

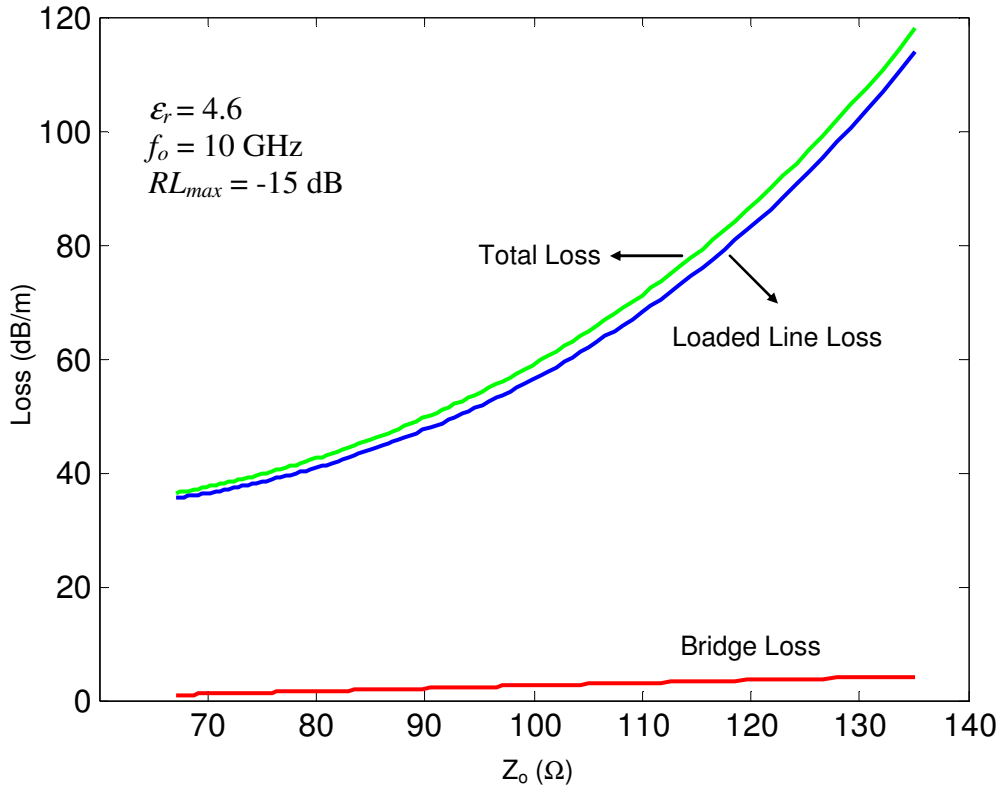


Figure 4.12. The loss due to the bridge resistance, CPW line loss, and total loss *per meter* of DMTL structures for different unloaded line characteristic impedances.

4.3.6. Degree/dB and Degree/cm performance analysis: The effect of substrate and CPW impedance

One of the most crucial performance criteria of a DMTL phase shifter is the ratio of the insertion phase to the loss, which is called as degree/dB performance. Using (4.15) for the *phase shift per meter* and using (4.27) for the *loss in dB per meter*, degree/dB performance can be evaluated. Figure 4.13 shows the degree/dB characteristics vs. unloaded line characteristic impedance values for DMTLs on different substrates. As can be seen, the characteristics increase as the unloaded line impedance is increased up to a value since the phase shift is directly proportional with the impedance of the line. However beyond a critical value, due to the increase

of the losses with decreasing CPW width, the performance starts degrading. As the dielectric permittivity increases, the peak of the degree/dB shifts towards lower unloaded line impedance values. The optimal unloaded line impedance for quartz, glass, and silicon substrates are around 90 Ω, 85 Ω, and 55 Ω, respectively. However for silicon substrates, 55 Ω unloaded line requires negative valued capacitances to achieve RL_{max} = - 15 dB with Z_{lu} = 59.8 Ω. Therefore, on silicon substrate, 65-70 Ω impedance for unloaded line seems to be more feasible with the expense of degradation in the performance. As a general rule, using low-permittivity substrate is more proper to realize a DMTL structure to achieve better performance.

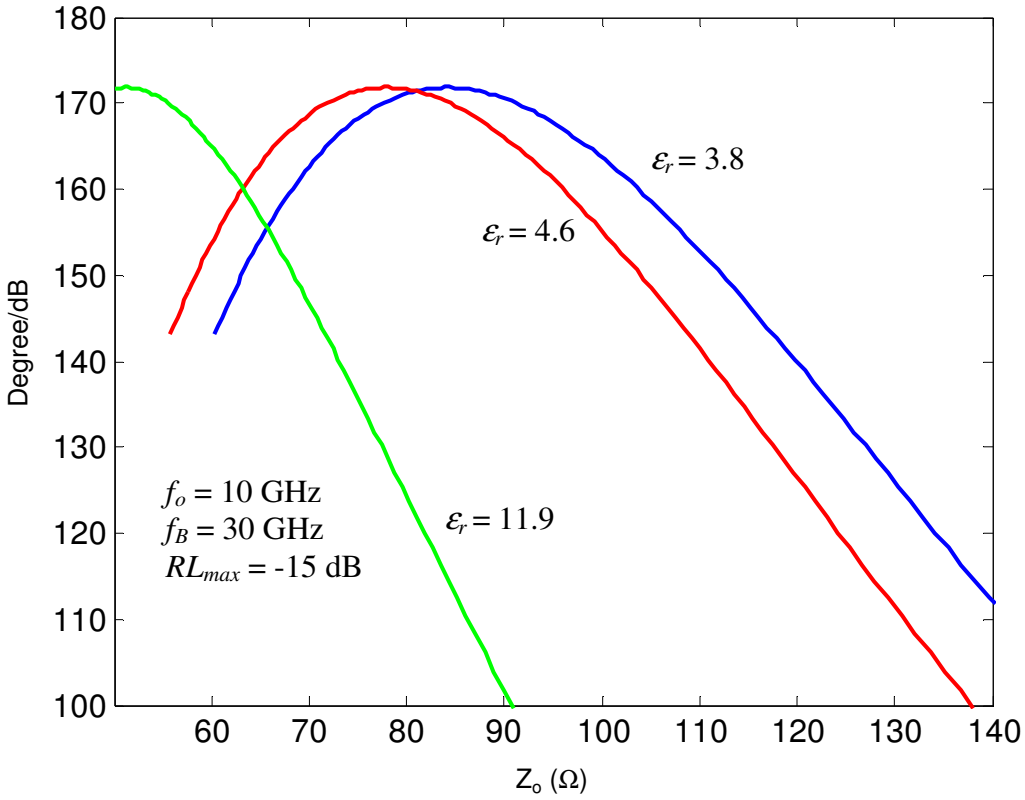


Figure 4.13. The degree/dB performance of DMTL structures implemented on different substrates with CPW ground-to-ground spacing of 220 µm.

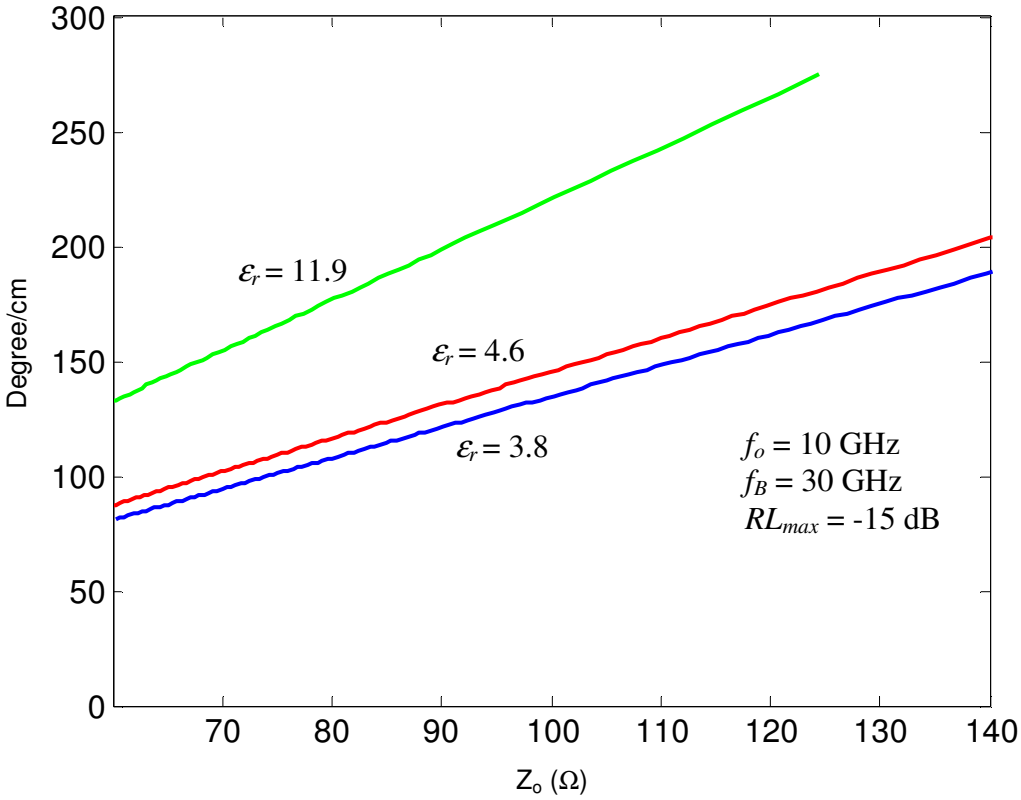


Figure 4.14. The degree/cm performance of DMTL structures implemented on different substrates.

The other important performance criteria of DMTL phase shifter is the *phase shift per centimeter* (degree/cm) characteristics. Figure 4.14 shows the degree/cm characteristics vs. unloaded line characteristic impedance values on different substrates. The degree/cm increases linearly with increasing Z_o. Therefore, high-permittivity substrates are suited for area miniaturization purposes since required phase shifts can be obtained in smaller areas.

4.4. Analog Phase Shifter versus Digital Phase Shifter

The DMTL design with only a fixed-fixed beam type capacitor in the shunt branch are called as analog DMTL phase shifter because the beam can reach to any position between z = h_o and z = $2h_o/3$ depending on the applied DC voltage [40]. The downstate to upstate capacitance ratio, C_r, can have any value between 0 and 1.5 that results infinite number of phase shift states obtainable between 0° and $\Delta\phi_{max.}$

An analog phase shifter, which has a C_r value to 1.5, can be operated around maximum return loss, RL_{max}, value of -20 dB as shown in Figure 4.7. Therefore, the *degree/cm* and the *degree/dB* performances of an analog phase shifter are limited by the C_r value. A DMTL phase shifter with a higher C_r value, for example around 2-3, gives higher *degree/cm* and *degree/dB* performances, due to the increased range between loaded line impedances, and sustains an RL_{max} value of around -15 dB at the same time, which can be achieved by a digital type DMTL structure.

Digital type DMTL phase shifters can provide higher C_r values, typically 2.5 [39]. It is obvious that the phase shifter have finite number of steps between 0° and $\Delta\phi_{max}$ because the term "digital" refers that the C_r value can be only 0 or 2.5. The main advantage of the digital design over analog is the reduction of the area of the device for the same amount of phase shift. The penalty paid for the gain in the area is the decreased resolution of phase steps obtained from the phase shifter.

The number of steps in a digital phase shifter structure, i.e. the number of bits, can be specified according to the requirements of the application. For example, for the monolithic phased array presented in this thesis, the number of bits is finalized as 3, because 8 states for the corresponding bits provide sufficient amount of resolution for progressive phase shifts between antenna elements. Higher number of bits will definitely offer higher sensitivity for beam steering however it will increase the biasing and fabrication complexity.

4.5. Digital DMTL Implementation using Metal-Air-Metal Capacitors

This section presents the design of the digital phase shifter structure used in the monolithic phased array. The phase shifter is composed of a periodically loaded high-impedance transmission line ($Z_o > 50\,\Omega$) with MEMS bridges in series with MAM capacitors forming a DMTL. Figure 4.15 shows general view of the phase shifter and its unit cell. Figure 4.16 gives the corresponding circuit model of the unit cell. When compared with the model in Figure 4.4, the circuit model uses transmission lines with the parameters of unloaded CPW, instead of using per unit length inductance and capacitance parameters modeling the unloaded CPW line. Both approach results very close results, however, in the modeling of phase shifters, using transmission lines simplify the circuit analysis in AWR Microwave Office v7.03 simulation environment. The unit cell has two states for the bridge: the up position and the down position. The total loading capacitance when the MEMS bridge is in the upstate position, is the series combination of two capacitors: C_{bu} and C_s. As the bridge is actuated by applying a DC bias voltage and collapsed on the DC isolation dielectric, the bridge capacitance increases by a factor of 60-70 and the resulting loading capacitance seen by the line is simply reduced to C_s. These two states in the loading capacitance yields two distinct loaded characteristics impedance of DMTL, namely, Z_{lu} (upstate loaded characteristic impedance: 58 Ω) and Z_{ld} (downstate loaded characteristic impedance: 44 Ω) where an acceptable return loss for both states can be achieved [39]. The phase shift per unit section can be controlled with the change of the phase velocity due to the change in the loaded characteristic impedance as given in (4.15). The periodicity along the DMTL structure, s, is optimized as 800 µm. The selection of f_B = 35 GHz as $f_B = 2.3f_o$ (f_o = 15 GHz) ensures the proper operation of the phase shifter as true-time delay at 15 GHz as shown in Figure 4.6. The following equations, which are the modified versions of the ones in Section 4.3.4, can be solved to define the required capacitance values and periodicity:

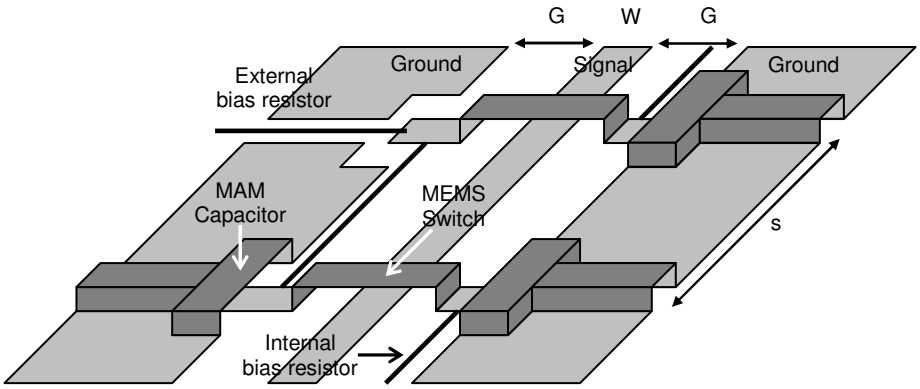
$$s = \frac{Z_{ld} c}{\pi f_B Z_o \sqrt{\varepsilon_{eff}}} \tag{4.28}$$

$$C_s = \frac{Z_o^{\,2} - Z_{ld}^{\,2}}{\pi f_B Z_o^{\,2} Z_{ld}} \tag{4.29}$$

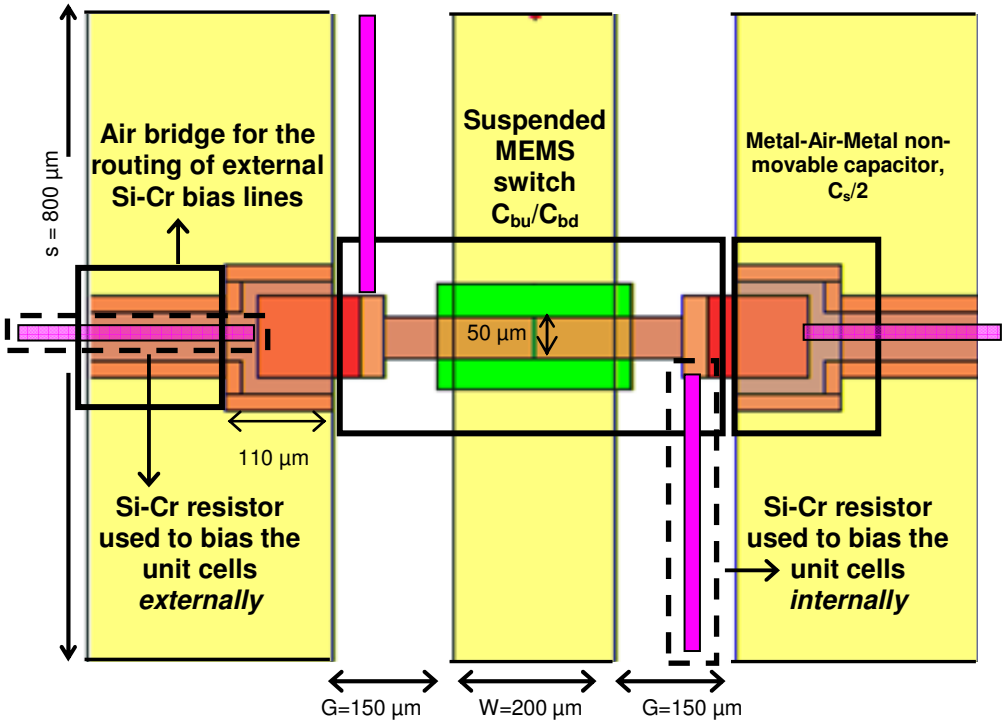
$$C_{bu} = C_s \frac{Z_{ld}^{\,2}\left(Z_o^{\,2} - Z_{lu}^{\,2}\right)}{Z_o^{\,2}\left(Z_{lu}^{\,2} - Z_{ld}^{\,2}\right)} \tag{4.30}$$

$$C_r = \frac{C_s}{\frac{C_{bu} C_s}{C_{bu} + C_s}} = \frac{C_{bu} + C_s}{C_{bu}} \tag{4.31}$$

The designed unit cell shown in Figure 4.3 (b) can provide nearly 11.5° at 15 GHz, which is verified with Ansoft HFSS simulations where C_{bu} (55 fF) and C_s (115 fF) are tuned to achieve the specified Z_{lu} and Z_{ld}. The non-movable static capacitor, C_s, is realized as a metal-air-metal (MAM) capacitor which has a high Q-factor (> 400 at 15 GHz) compared to a metal-insulator-metal (MIM) capacitor. The height of the membranes in the MAM capacitor and the switch is 2 µm. The characteristic impedance of the unloaded transmission line is selected to be Z_o = 77 Ω (CPW dimensions: W = 200 µm, G = 150 µm). The selection of Z_o = 77 Ω is reasonable choice considering the result of the *degree/dB* analysis in Section 4.3.6. The attenuation constant, α_o, and the effective dielectric constant, ε_{eff}, of the unloaded line is found to be 16 dB/m and 2.76 respectively with the given formulation in Section 3.4.1. Figure 4.17 presents the EM simulation and modeled S-parameters of a structure consisting of 8 unit cells.



(a)



(b)

Figure 4.15. The digital DMTL phase shifter: (a) General schematic view of the structure. The air bridge on the external resistor is removed in the drawing for better visualization. (b) The top view of the unit cell.

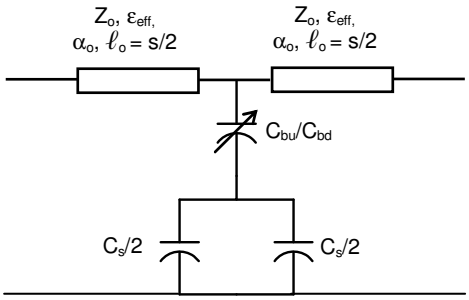
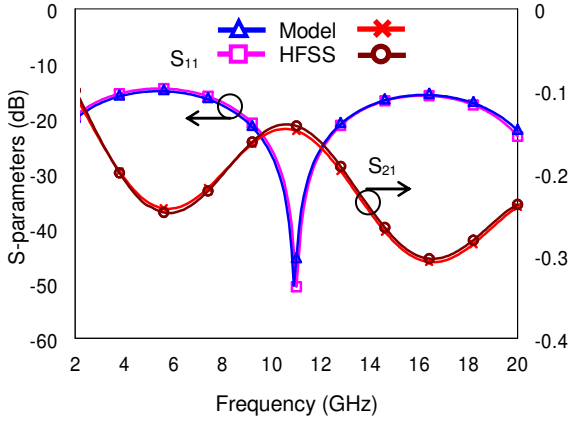
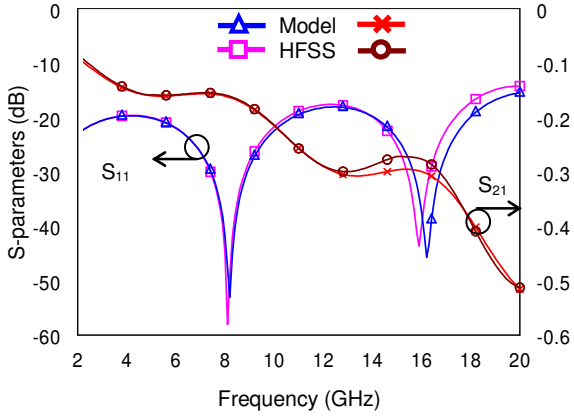


Figure 4.16. The circuit model of the unit cell of the phase shifter.



(a)



(b)

Figure 4.17. The simulation and circuit model results for the DMTL consisting of 8 unit cells: (a) MEMS bridges are in upstate (b) MEMS bridges are in downstate.

The overall 3-bit RF MEMS phase shifter employed in the system consists of there sections with a total of 28 unit cells within an area of 22.4 mm × 2.1 mm. Figure 4.18 shows the layout view of the 3-bit structure consisting of 28 unit cells. The first section has 4 cells and is designed to have a phase shift of $\Delta\phi$=46.9°. The second section has 8 cells providing 90.4°, and the next 16 cells forms the 3rd bit which is designed to give 182.6° at 15 GHz. Figure 4.19 shows the phase shifts obtained from the simulation for 8 states of the 3-bit structure. The structure can give phase shifts with 45° steps at 15 GHz as designed. Each bit is connected internally with internal bias resistors extending from one unit cell to the next cell shown in Figure 4.3 (b). There are also three external resistors for three bit to be actuated separately.

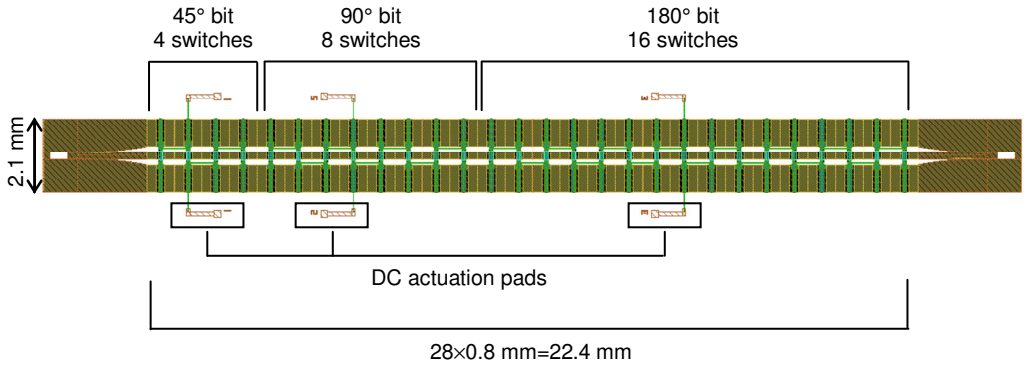


Figure 4.18. The layout drawing of the 3-bit DMTL phase shifter with a total of 28 unit cells.

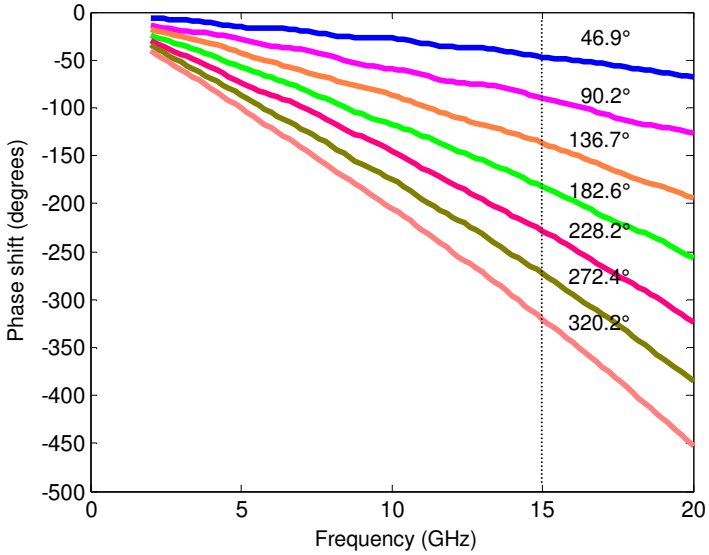


Figure 4.19. HFSS simulation results for phase shift vs. frequency for 8 states of the 3-bit RF MEMS phase shifter.

4.6. The Losses in the Digital Phase Shifter

The dominant loss mechanism of the phase shifter is the loss of the unloaded CPW. However, the series resistance of the bridge and Q-factor of C_s also play a significant role. The modified circuit model which includes the resistors modeling the effects of bridge losses and finite Q-factor losses of the MAM capacitors is given in Figure 4.20. The loss due to the MEMS bridge is modeled with a series resistance of R_{bu} = 1.5 Ω in the upstate and R_{bd} = 0.8 Ω in the downstate, which is found by curve fitting. The finite Q-factor of the MAM capacitor is also involved in the model with shunt resistors with the MAM capacitor. The next section gives the details about the calculations of the losses due to the bias resistors.

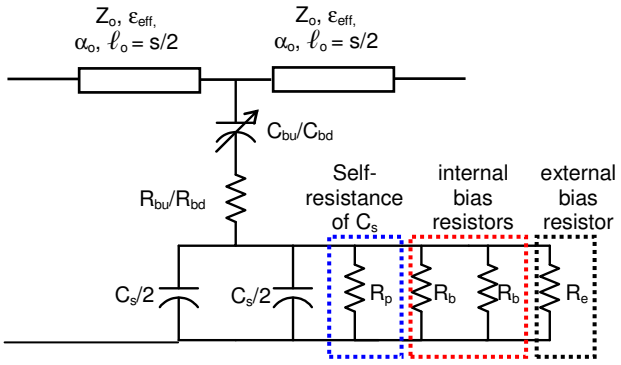


Figure 4.20. The complete circuit model of the unit cell with the effect of bias resistors included as shunt elements with the MAM capacitors.

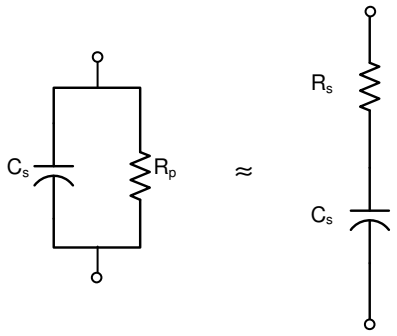


Figure 4.21. The equivalent representations of a lossy capacitor.

4.6.1. The Loss due to MAM Capacitors: Q-factor point of view

In order to evaluate losses due to the MAM capacitor, the approximation of the lossy capacitor model given in Figure 4.21 is used. This provides us to handle the shunt resistors as a series equivalent resistors resembling to the bridge resistance. Using

(4.25), the loss contribution of the finite Q-factor of the MAM capacitor *per section* can be expressed as:

$$\alpha_Q = 8.686 \frac{\omega C_s Z_{ld}}{2Q_o} \quad \text{dB/section} \tag{4.32}$$

where Q_o is the Q-factor of the capacitor defined at the center frequency ω_o. It should be noted here that Q-factor loss is expressed in the downstate since the losses in the downstate are higher than the upstate as explained in Section 4.3.5. The expression of (4.27) for loaded line loss and the bridge loss can be merged with the Q-factor loss in (4.32) to find the total loss per unit length of the structure:

$$\alpha_{ld_total} = \alpha_{ld} + \alpha_{bd} + \alpha_Q \tag{4.33}$$

$$\alpha_{ld} = 8.686 \left(\alpha_o \frac{Z_o}{Z_{ld}} + \frac{\omega^2 C_s{}^2 R_{bd} Z_{ld}}{2s} + \frac{\omega C_s Z_{ld}}{2Qs} \right) \quad \text{dB/m} \tag{4.34}$$

Figure 4.22 gives the *degree/dB* performance vs. frequency of the design in Section 4.5 showing the great influence of the Q-factor of the MAM capacitor on the performance of the phase shifter. During these analyses, the loss of the structure is calculated using (4.34). The bridge resistance, R_{bd}, is considered to be zero to simplify the analyses. The HFSS simulations show that the Q-factor of the static capacitor (C_s) is 433 ($R_p = 40$ kΩ) which results very high *degree/dB* performances. However the bias resistors have an adverse effect on the Q-factor of the MAM capacitors, which is examined in detail in the next section.

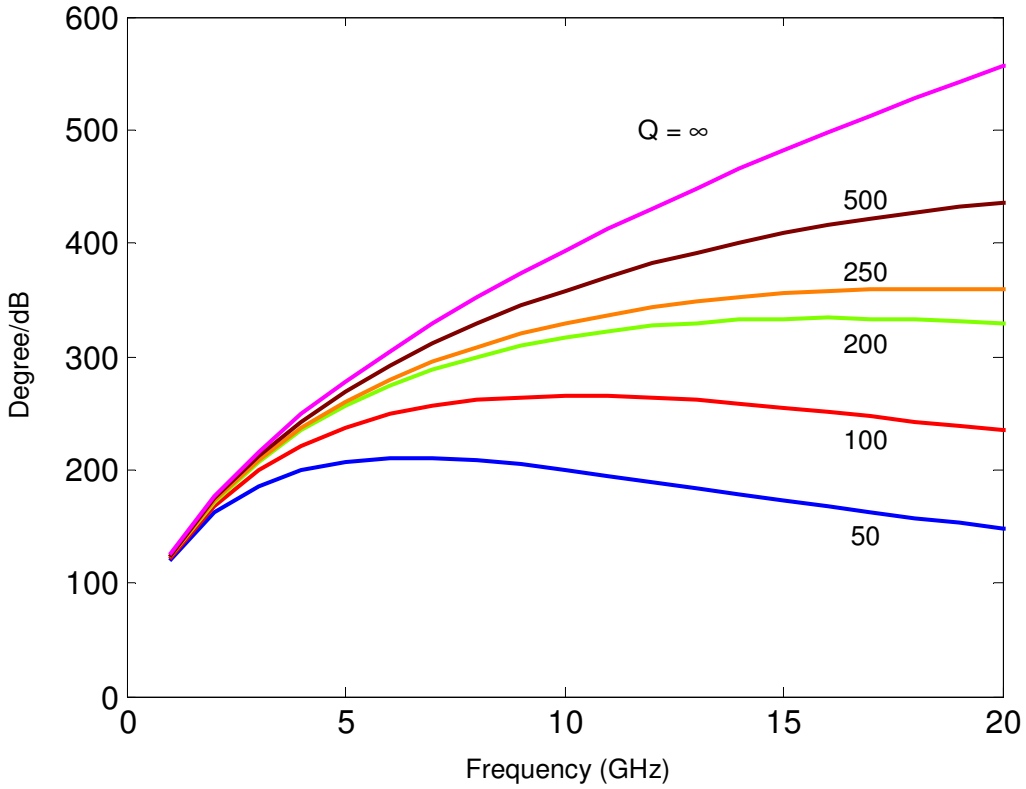


Figure 4.22. The effect of the Q-factor of the MAM capacitor on the degree/dB performance of the digital phase shifter design.

4.6.2. The Effect of the Bias Resistors

In order to DC bias the unit sections of the phase shifter, thin film resistors are employed both inside the gaps of CPW extending from one bridge to the other (internal resistors) and underneath the over-pass air bridges on the grounds of CPW (external resistors) as shown in Figure 4.3. These resistors are implemented using the resistive material of Si-Cr with a conductivity of 4300 S/m. The return loss of the structure is not significantly affected by the presence of the bias resistors since the return loss is determined by the loaded line impedances, Z_{ld} and Z_{lu}, which are only affected from the unloaded transmission line parameters and the loading capacitors,

C_{bu} and C_s. The designed phase shifter has an insertion loss of nearly 1.08 dB for the worst case (all switches are down) if no bias lines are present. The insertion loss is calculated directly from the S_{21} characteristics with the return loss removed by tuning the port impedance to 44 Ω in the simulations. The bias lines which are placed inside the gaps of the CPW have an adverse effect on the insertion loss due to the decrease of the Q-factor of the static capacitor, C_s. The internal Si-Cr bias lines shown in Figure 4.20 are shunt connected to the self resistance (R_p) of the static capacitor, C_s, reducing the Q-factor. Since there exists two bias lines seen by C_s, the equivalent resistance of the capacitor C_s reduces to $R_p//(R_b/2)$ from R_p (40 kΩ) where R_b (internal bias resistor) is equal to 20 kΩ ($\sigma_{Si\text{-}Cr}$ = 4300 S/m, length = 350 µm, width = 20 µm, thickness = 0.2 µm). The Q-factor reduces to 87 from 433, accordingly. The insertion loss of the whole structure, which is calculated as 1.08 dB, increases to 1.56 dB due to the reduced Q-factor of C_s. The external bias resistors, which are placed underneath the air bridges on the ground depicted in Figure 4.3, are used only for the 3 cells in order to actuate each bit separately. Due to the strong coupling between the ground plane and bias resistor underneath, the effective resistance seen by C_s, reduces to R_e = 1.45 kΩ (effective resistance of the external bias lines) and Q-factor to 13 for those 3 cells. The insertion loss of the structure is 1.91 dB where the Q-factor of 3 cells with external bias lines is 13 and the Q factor of the remaining 25 (out of 28) is 87. Figure 4.23 shows the effect of the bias lines using the simulation results of the insertion loss characteristics.

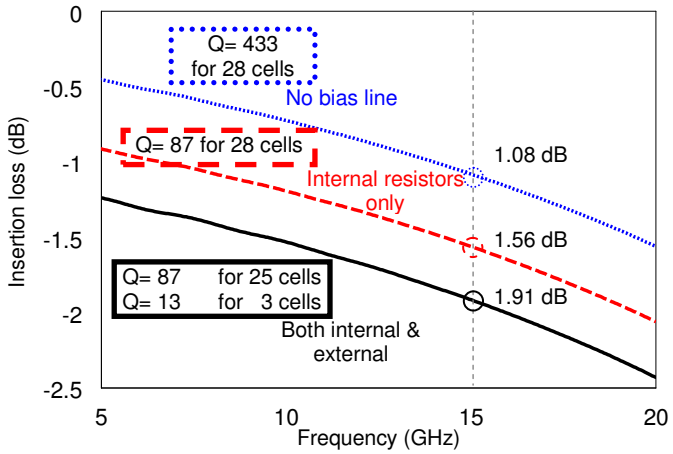


Figure 4.23. Simulated insertion loss of the phase shifter which is obtained from S_{21} when the ports of the structure are tuned as 44 Ω (Z_{ld}).

4.7. Phase Shifter Measurements

The phase shifters of the phased array are also fabricated separately on the same wafer and measured using TRL calibration with a port impedance of 77 Ω [64]. All of 8 states are measured by applying DC voltage with DC probes and bias tee. The actuation voltage of the phase shifters is found to be 16 V. All the states have a return loss better than 10 dB, with a worst case insertion loss of 2 dB at 15 GHz. The average insertion loss for 8 states is 1.5 dB. Figure 4.24 shows the photograph of the fabricated phase shifters. Figure 4.25 presents the SEM images of the unit cells of the phase shifter. Both external and internal resistors are illustrated on the images. The etch holes on the suspended regions are used to improve the removal of sacrificial layer underneath those regions. The measurements are performed with the HP8720D vector network analyzer and Cascade Microtech Summit 9000 manual probe station using Picoprobe 40-A-GSG-150P CPW probes [51]. The bias voltages are applied with the Picosecond 5542-230 bias tees. Figure 4.26 shows the measured and modeled S-parameters of the 3-bit DMTL phase shifter for 8 states. Table I shows the simulated and measured circuit parameters for the unit cell. The glitch around 15

GHz in the measurements is observed for all of the samples. Although the exact reasoning of the glitches is not identified yet, they occur most probably due to a possible design error in TRL calibration kit. Similar glitches around 15 GHz are also observed in the simple CPW line measurements with the same calibration kit.

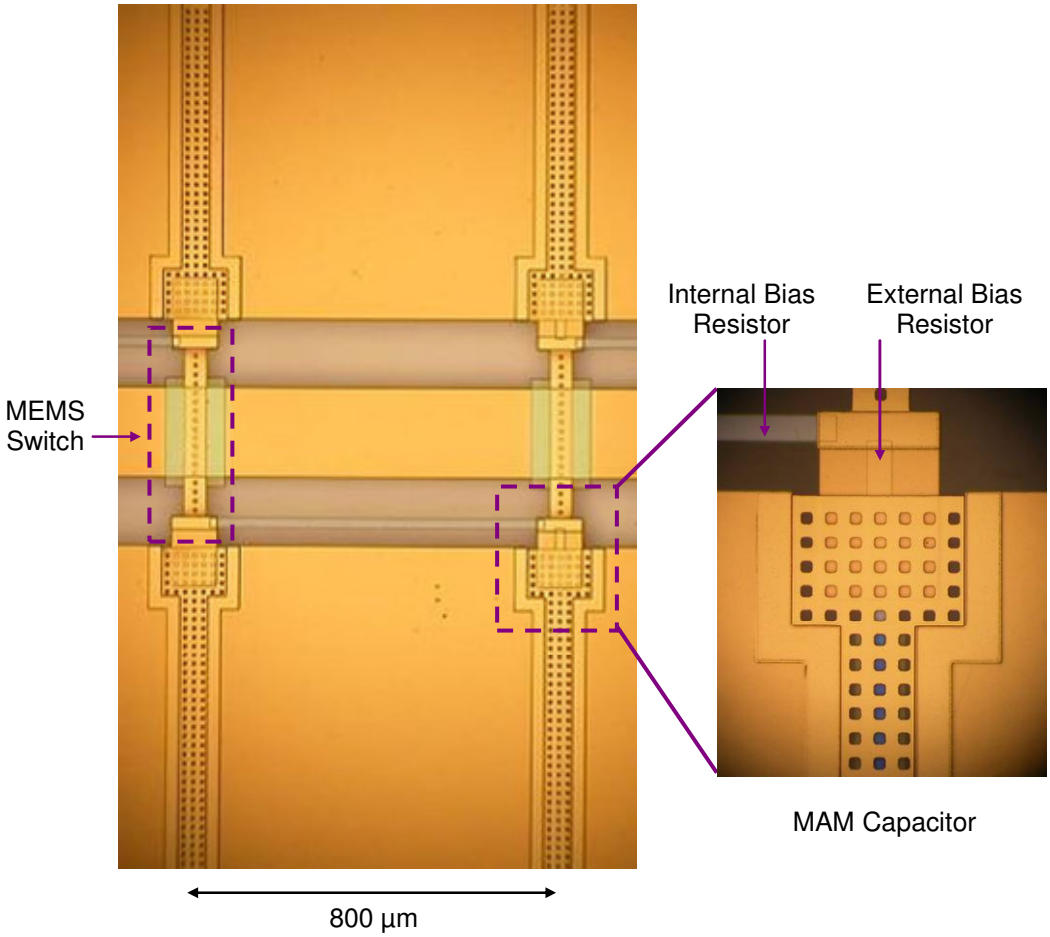
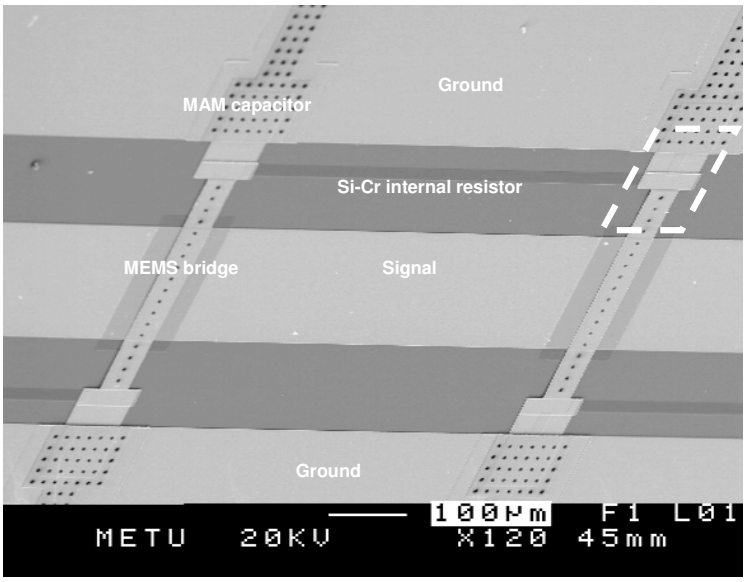
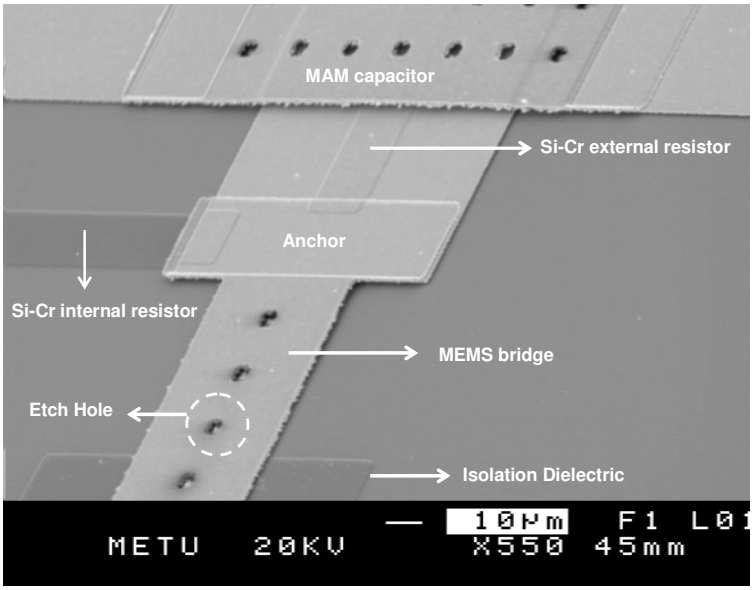


Figure 4.24. Photograph of the fabricated 3-bit DMTL RF MEMS phase shifter.

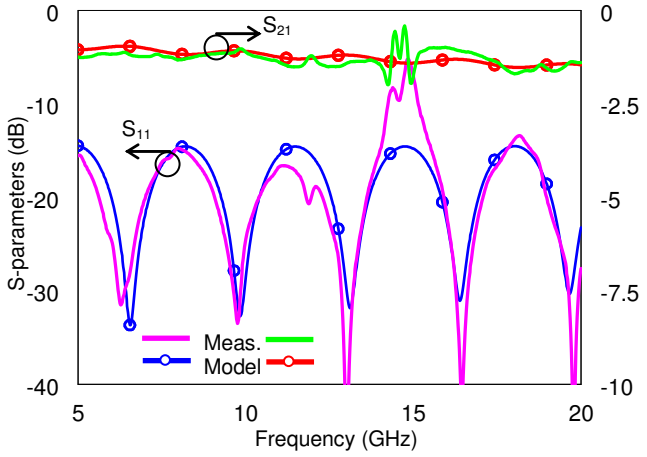


(a)

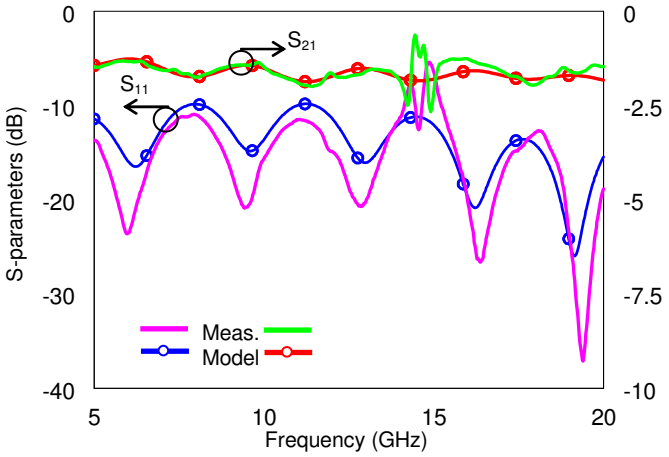


(b)

Figure 4.25. SEM photographs of the phase shifter structure. (a) Photograph of the two unit cells where Si-Cr internal resistors connecting the unit cells to carry DC signal can be seen. (b) A detailed view of the anchor region of the MEMS bridge.


S21
S11
Meas.
Model
S-parameters (dB)
Frequency (GHz)
0
-10
-20
-30
-40
-2.5
-5
-7.5
5
10
15
20

(a)


S21
S11
Meas.
Model
S-parameters (dB)
Frequency (GHz)
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-40
-2.5
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15
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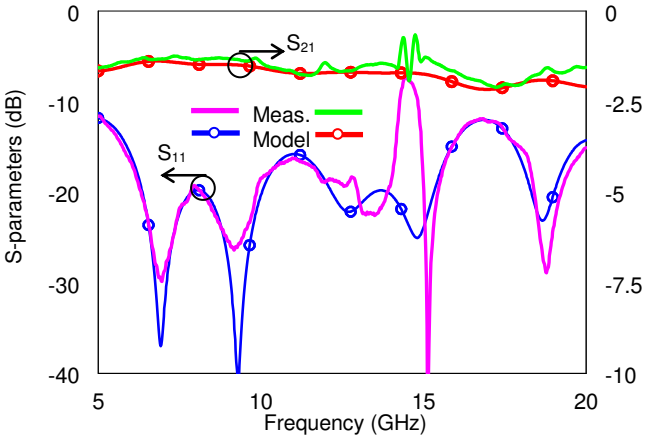
(b)


S21
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Meas.
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S-parameters (dB)
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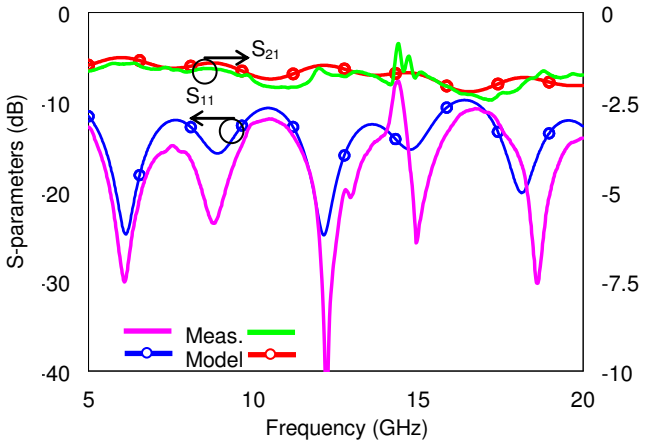
(c)


S21
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Meas.
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S-parameters (dB)
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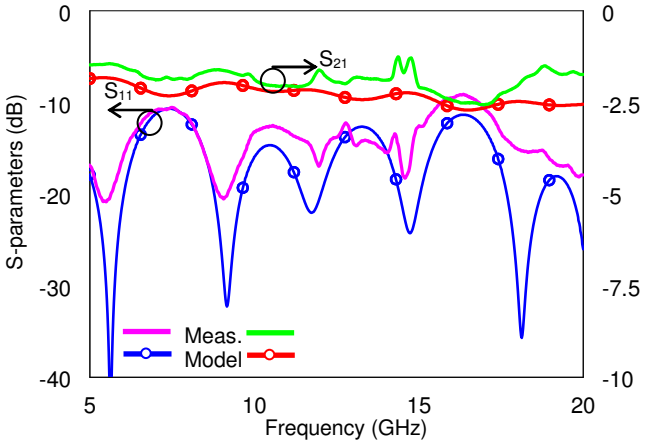
S21
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Meas.
Model
S-parameters (dB)
Frequency (GHz)
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10
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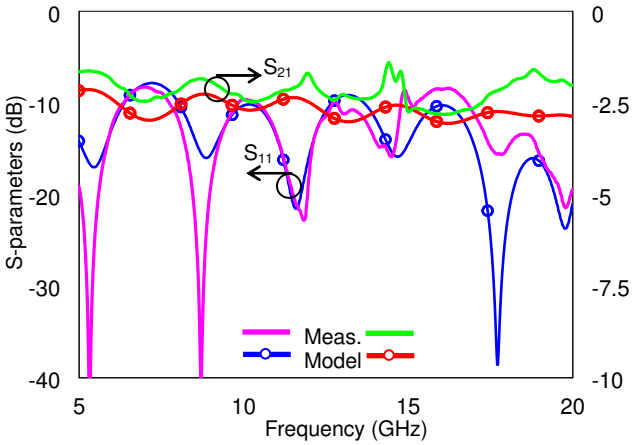
(e)


S21
S11
Meas.
Model
S-parameters (dB)
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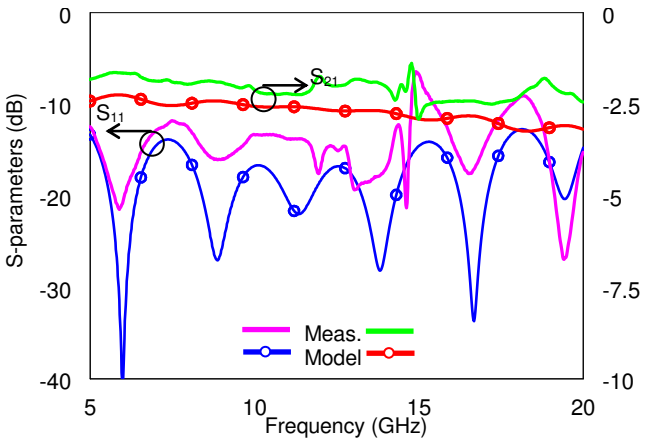
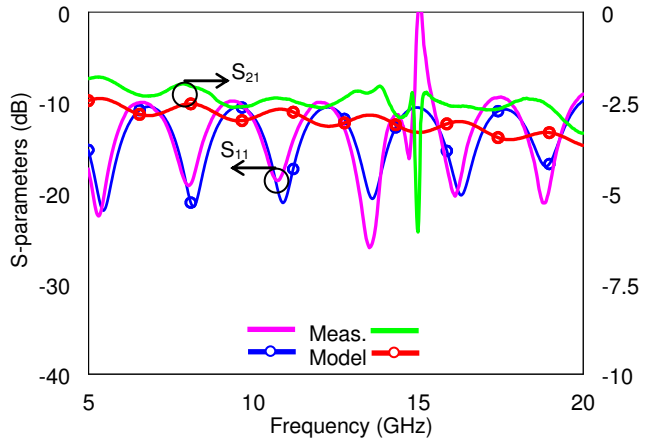


(g)



(h)

Figure 4.26. Measured and modeled S-parameters of the 3-bit phase shifter for different states (a) 000 state (b) 001 state (c) 010 state (d) 011 state (e) 100 state (f) 101 state (g) 110 state (h) 111 state.

Table 4.3 Simulated and measured circuit parameters for the unit cell of the DMTL phase shifter.

Parameter	Simulated	Measured
C_{bu}	55 fF	50 fF
C_s	115 fF	71 fF
R_{bd}/R_{bu}	0.8 Ω/1.5 Ω	0.8 Ω/1.5 Ω
Z_o	77 Ω	77 Ω
ε_{eff}	2.76	2.76
α_o @ 10 GHz	16 dB/m	23 dB/m
R_p	40 kΩ	40 kΩ
R_b	20 kΩ	20 kΩ
R_e	1.45 kΩ	1.45 kΩ
C_{bd}	3 pF	1 pF
Z_{lu}	58 Ω	62.8 Ω
Z_{ld}	44 Ω	52.9 Ω
°/unit cell @ 15 GHz	11°	6°
Insertion Loss	1.91 dB	2.03 dB

The bridge capacitance for the upstate, C_{bu}, can be fabricated very close to the designed value. However, the MAM capacitors, C_s, show a deviation compared to the simulated value. The measured downstate capacitance value is also degraded compared to simulated value due to the surface roughness. However the measured downstate capacitance is high enough to have a virtual short circuit through the bridge. The MAM capacitors have a different mechanical design and are fixed on three sides to have a rigid structure which might result in increase in the height due to the residual stress on the structural layer metal. Figure 4.27 shows 3-D plot of the surface profile data of the fabricated phase shifter obtained using a light-

interferometer microscope. The bridge height is around 2 µm and 2.6 µm for the central bridge and MAM capacitor, respectively. The decrease of the MAM capacitances shifts the loaded line impedances, Z_{lu} and Z_{ld}. The shift reduces *degree/unit cell* performance of the measured phase shifter to 6° according to (4.15), which is 11° for the designed phase shifter. Figure 4.28 shows the insertion phase characteristics for all the states of the phase shifter. The measured phase shifter provides approximately 20°/50°/95° phase shifts and their combinations at 15 GHz.

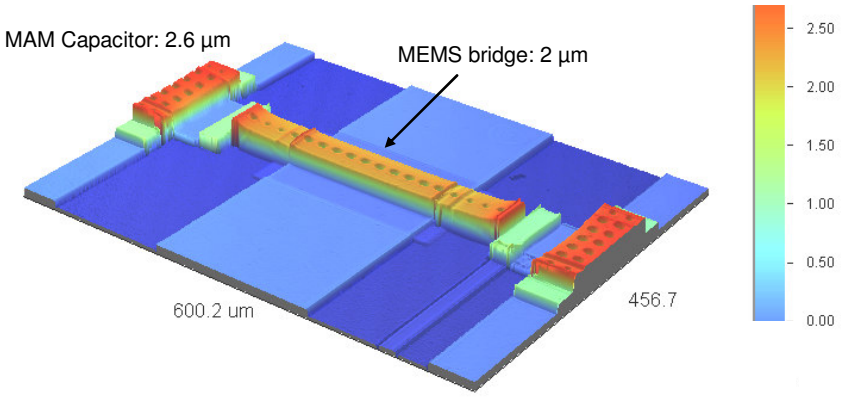


Figure 4.27. Surface profiler view of the unit cell of the phase shifter obtained using the interferometer microscope.

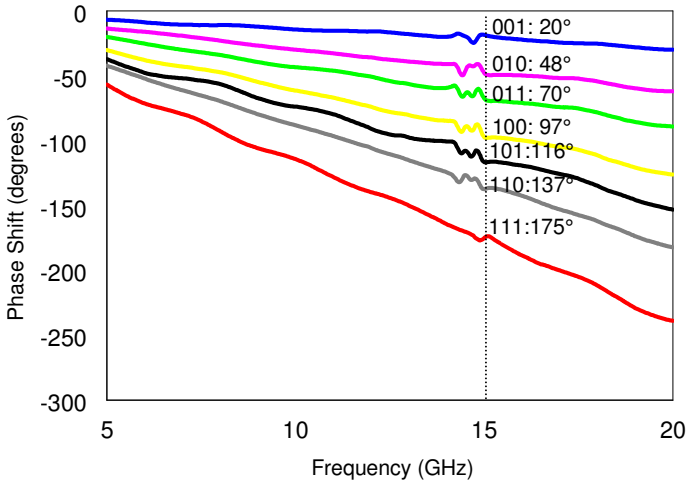


Figure 4.28. The measured phase shift vs. frequency characteristics of the phase shifter for different states.

Table 4.4 The simulated and measured loss components at 15 GHz. The loaded line loss is defined when $R_{bd} = 0\ \Omega$, $R_p = 40\ k\Omega$, $R_b = R_e \rightarrow \infty$.

Parameter	Simulated	Measured
Loaded Line Loss	0.63 dB	0.83 dB
Bridge Resistance (R_{bd}) Loss	0.45 dB	0.21 dB
25 cells Q-factor Loss	0.43 dB	0.51 dB
3 cells Q-factor Loss	0.40 dB	0.48 dB
Total Loss	1.91 dB	2.03 dB

Table 4.4 shows the simulated and measured loss components at 15 GHz. The loaded line loss, which is defined when $R_{bd} = 0\ \Omega$, $R_p = R_b = R_f \rightarrow \infty$, is directly related to the unloaded line loss, with a multiplicative factor of Z_o/Z_{ld} as mentioned in Chapter III. The loaded line loss is increased in the measurements due to the increase of the attenuation constant (α_o) of the unloaded line. The Q-factor losses are increased due to decrease of the quality factor and also the change of the loaded line impedance to

52.9 Ω from the designed value of 44 Ω. The Q-factor of the MAM capacitors with internal bias resistors reduces to 53 (simulated value: 87) due to the decrease of the capacitance value. The Q-factor of the MAM capacitors having both internal and external resistors is equal to 8 (simulated value: 13). Figure 4.23 shows the insertion loss analysis for the measured structure illustrating the effect of Q-factor values of MAM capacitors. These cases are Q = 433 (no bias line present) for 28 cells, Q = 53 for 28 cells, and Q = 53 (for 25 cells) and Q = 8 (for 3 cells). The analysis also shows that if a conductivity of 2500 S/m for Si-Cr layer is achieved, the worst case insertion loss can be reduced down to nearly 1.6 dB where Q-factors can be increased to 132 for 25 cells with internal bias resistors and 22 for 3 cells with both internal and external resistors. The average insertion loss of the phase shifter will be about 1.3 dB, which is quite close to the reported losses of these types of MEMS phase shifters [39]. The conductivity value of Si-Cr film depends on the chamber conditions of the sputter equipment and provided gas flow during processing.

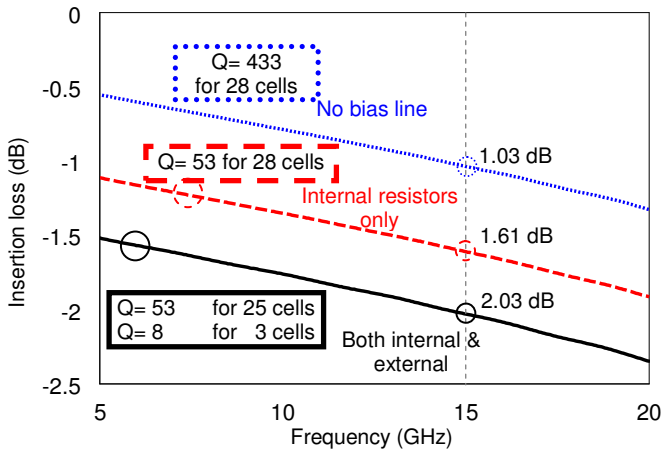


Figure 4.29. The insertion loss of the phase shifter (extracted from measurement results) which is obtained from S_{21} when the ports of the structure are tuned as 52.9 Ω (Z_{ld}).

4.8. Designs on Different Substrates

This section provides an approach in the design of digital type DMTL phase shifters on different substrates using the theoretical background given in this chapter. Moreover, a general guideline for the selection of CPW dimensions, i.e. ground-to-ground spacing, which is quite significant for layout considerations, is drawn in this section. The sample substrates are quartz, glass, and silicon with relative permittivities of 3.8, 4.6, and 11.9, respectively. Table 4.5 gives the parameters of the designs for RL_{max} = -15 dB at the center frequency, f_o, of 15 GHz with a Bragg frequency of $2.3f_o$.for the DMTL structure with physical parameters shown in Figure 4.3 (a). The following is the summary of the evaluation of the parameters in Table 4.5:

- **Unloaded line impedance, Z_o:** In Section 4.3.6, the effect of the unloaded line impedances on the *degree/dB* performance for quartz, glass and, silicon substrates are evaluated. It was deduced that the optimal unloaded line impedances for quartz, glass, and silicon are about 90 Ω, 85 Ω, and 55 Ω, respectively. However for silicon substrate, 55 Ω unloaded line requires negative valued capacitances. Therefore, on silicon substrate, 70 Ω impedance for unloaded line is an acceptable choice with the expense of degradation in the performance.

- **The length of the unit cell (s), required capacitances (C_{bu} and C_s) and down-up capacitance ratio (C_r):** These parameters can be evaluated using the expression in (4.28)-(4.31) with the given Bragg frequency of $f_B = 2.3f_o$ and the optimal loaded line impedances which are Z_{lu} = 59.8 Ω and Z_{ld} = 41.8 Ω. The length of the unit cell decreases as the dielectric constant of the substrate increases.

- **CPW dimensions:** The ground-to-ground spacing of a CPW of a DMTL structure, which is equal to $W+2G$, should be selected according to the substrate and center frequency. The substrate parameters affect the W/G ratio to realize the unloaded line characteristic impedance (first bullet) and hence the width of the bridges to obtain the required capacitance values (second bullet). Moreover, in order to reduce radiation losses, the ground-to-ground spacing of a CPW should be reduced as the frequency increases. As a general guideline the value of ground-to-ground spacing of a CPW can be approximately selected as:

$$W + 2G \approx \frac{c}{8 f_o \sqrt{\varepsilon_r}} \tag{4.35}$$

  where ε_r is the relative permittivity of the substrate. The ratio of W/G can be found for the required unloaded line impedance (first bullet) using the CPW equations in Section 3.4.1.

- **The length and number of unit cells for 180° phase shift:** The phase shift along a DMTL structure between two different loaded line impedances can be calculated using (4.15). The required length for 180° phase shift can be calculated directly from this expression. The required length gets shorter as the permittivity of the substrate is increased. The number of unit cells for 180° phase shift is independent of the substrate since the ratio of the required length for 180° phase shift to the length of the unit cell (s) cancels both the effect of Z_o and $\varepsilon_{eff.}$

- **Insertion losses:** The insertion losses for a length of structure for 180° phase shift (fourth bullet) with different Q-factors of MAM capacitors are calculated using (4.27). For simplicity, MEMS bridges are assumed to be lossless, i.e. $R_{bd} = 0\ \Omega$. The losses are strongly affected by the Q-factor of the

MAM capacitances and are almost independent of the substrate used. Table 4.5 gives the parameters of phase shifters on different substrates designed using the guidelines presented above.

Table 4.5 The parameters of the phase shifter designs on different substrates. RL_{max} = -15 dB, f_o = 15 GHz, $f_B = 2.3f_o$.

Parameter	Quartz	Glass	Silicon
Z_o (Ω)	90.7	84.4	69.4
s (μm)	810	808	652
C_{bu} (fF)	93.4	78.8	34.5
C_s (fF)	174	166	141
C_r	2.86	3.11	5.08
W/G (μm)	210/195	180/160	70/115
[W+2G] (μm)	600	500	300
Length for 180° (mm)	9.7	9.65	7.8
# of unit cells for 180°	12	12	12
Insertion Loss (dB) for Q = 50	0.97	0.98	1.11
Insertion Loss (dB) for Q = 200	0.44	0.48	0.68

4.9. Scaling the Designs to Other Frequencies

The design parameters in Table 4.5 can be scaled to other frequencies easily with minor modifications. As a case study, the center frequency is selected as f_o =15 GHz and f_o = 30 GHz on glass substrate. The unloaded line characteristic impedance are nearly around 85 Ω to achieve optimal performance. The periodicity along DMTL is scaled according to the change of f_o. The capacitance values are also scaled due to

the scaling of the unit cell length in order to achieve the same loaded line impedances. The number of unit cell to achieve 180° phase shift is independent of the frequency. However the length of DMTL for 180° phase shift is scaled according to the center frequency, f_o. The ground-to-ground spacing of CPW is modified and scaled to reduce the radiation as discussed in the previous section.

Table 4.6 The parameters of the phase shifter designs on glass substrate for different f_o selections with RL_{max} = -15 dB, $f_B = 2.3f_o$.

Parameter	f_o = 15 GHz	f_o = 30 GHz
Z_o (Ω)	84.4	84.9
s (μm)	808	405
C_{bu} (fF)	78.8	40.1
C_s (fF)	166	83.7
C_r	3.11	3.08
W/G (μm)	180/160	96/77
[W+2G] (μm)	500	250
Length for 180° (mm)	9.65	4.85
# of unit cells for 180°	12	12
Insertion Loss (dB) for Q = 50	0.98	1.07
Insertion Loss (dB) for Q = 200	0.48	0.55

CHAPTER V

MONOLITHIC PHASED ARRAY USING RF MEMS TECHNOLOGY

5.1. Introduction

This chapter presents the design and measurement results of the monolithic phased array structure employing RF MEMS digital phase shifters as the phase shifting elements, which are presented in the previous chapter. The design of the feed network and CPW-MS transition are also detailed. The effect of the number of elements of the phased array on the scan angle is also examined and presented. The chapter is finalized with the proposal of a alternative design approach for monolithic phased array implementation using slot-coupled antennas.

The phased array system in this thesis is designed at 15 GHz, and it employs 3-bit Distributed MEMS Transmission Line (DMTL) type phase shifters. These phase shifters are monolithically integrated with the feed network and four linearly placed microstrip patch antennas on the same substrate. The use of MEMS phase shifters in a phased array offers some advantages as mentioned in the previous chapter: To summarize, MEMS phase shifters have low-loss performance with nearly zero DC power consumption compared to the semiconductor based counterparts [36], [37].

Moreover, MEMS phase shifters are also suitable for monolithic phased array designs with their reduced cost and volume compared to the semiconductor and ferrite based counterparts. The phase shifters in the phased array presented in this work are used to obtain various combinations of progressive phase shift in the excitation of radiating elements to steer the beam. Furthermore, system losses and size are reduced by implementing RF MEMS phase shifters in a phased array monolithically manufactured by micromachining technology. This work is one of the first few electronically scanning phased array systems with RF MEMS phase shifters, reported in the literature [29], [30]. The next sections give the configuration of the array including the simulation results for the sub-blocks of the array and the measurement results.

5.2. The Configuration of the Phased Array

The phased array is composed of four microstrip patch antennas, a corporate feed network, and four RF MEMS phase shifters. The operation frequency is selected as 15 GHz to be able fit the whole system into a single 500-μm thick 4" glass substrate ($\varepsilon_r = 4.6$, $\tan\delta = 0.005$). The total size of the system is about 6 cm × 5 cm. Figure 5.1 gives the layout of the monolithically integrated phased array. Microstrip patch antennas having dimensions of 4.65 mm × 4.65 mm are equally spaced by $\lambda_o/2$ (1 cm) distance from each other's phase center. A corporate feed network, which is composed of 70 Ω ~$\lambda_o/4$ (2.2 mm) transformers, is optimized at around 15 GHz. The width of 50 Ω and 70 Ω lines are 0.95 mm and 0.43 mm. Tapered lines with low return loss are required for the transitions from microstrip lines to coplanar waveguide (CPW) since RF MEMS phase shifters are implemented on CPW. The transition is designed by Engin Ufuk Temoçin at the METU RF MEMS group [66]. Figure 5.2, Figure 5.3, and Figure 5.4 give the simulation results for the patch

antenna, the CPW-microstrip transition and the microstrip feed network, respectively.

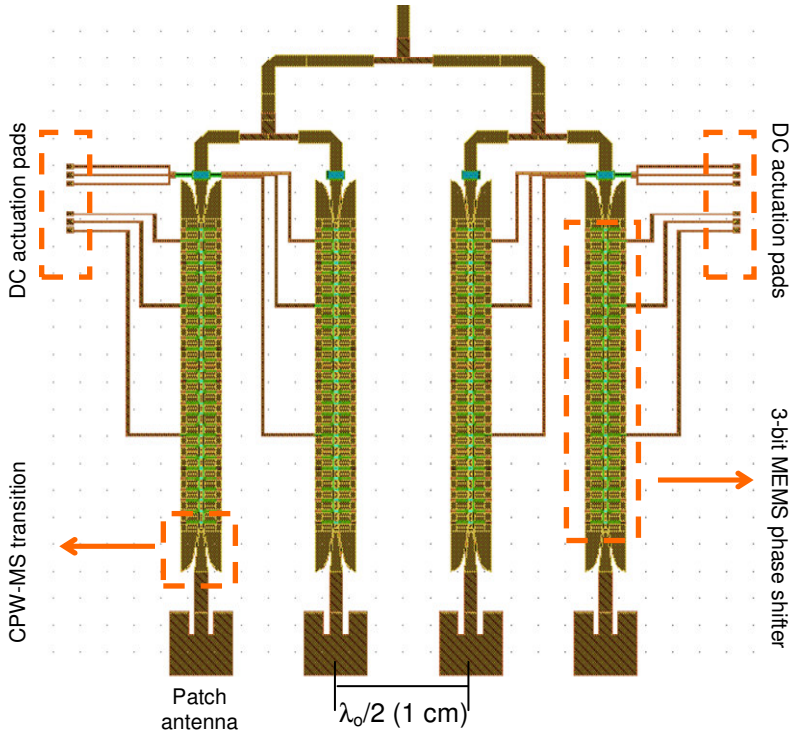


Figure 5.1. The layout drawing of the monolithically integrated phased array.

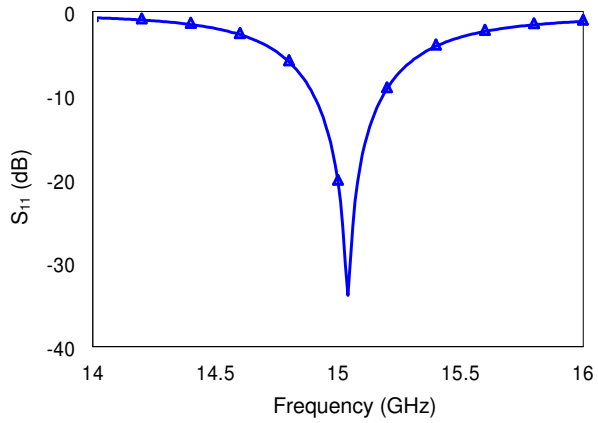


Figure 5.2. The reflection coefficient characteristics of the square microstrip patch antenna with dimensions 4.65 mm × 4.65 mm and inset feed depth 1.7 mm. The simulation is performed by Ansoft Ensemble.

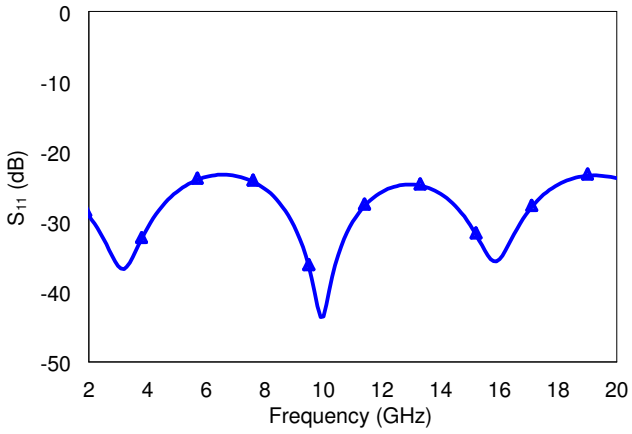


Figure 5.3. The reflection coefficient characteristics of the exponential type transition from CPW to microstrip lines. The simulation is performed by Ansoft HFSS v9.2.

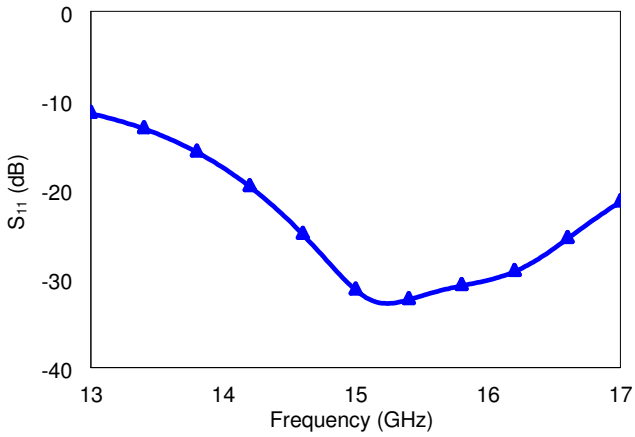


Figure 5.4. The reflection coefficient characteristics of the microstrip feed network. The simulation is performed using Ansoft Ensemble.

It has been shown in the previous chapter that the phase shifters of the array are designed to provide progressive phase shifts of 45°/90°/180° and their combinations at 15 GHz. Table 5.1 shows the calculated maximum directivities of an array consisting of 4 linearly placed patch antennas placed on a glass substrate for broadside configuration. The field pattern of a patch antenna is derived based on the cavity model assumption. When both array factor and element pattern are taken into account 3 dB beamwidth of the array is 30° and the main beam can be rotated to approximately 12° and 24° for progressive phase shifts of 45° and 90°, respectively. The finite number of elements in the array prevents the beam steering to the expected angles which are 15° and 30°, considering the array factor. Figure 5.5 shows the field magnitudes in H-plane for the element factor, the array factor, and the total field for a linear array of 4 patch antennas with a spacing and progressive phase shift between elements of $\lambda/2$ and 90°, respectively. Although the array factor maximum is at 30°, the total field maximum occurs at 24°. When the number of elements is increased to 8 patch antennas, the total field maximum occurs at 28°, which is illustrated in Figure 5.6. Progressive phase shift of 135° and 180° can also be provided by the

phase shifter; however due to the element pattern the main beam can not be steered to the corresponding scan angles.

Table 5.1 Calculated maximum directivities of the microstrip patch antenna and the phased array with $d = \lambda/2$ and $\beta = 0°$.

	Directivity (unitless)	Directivity (dB)
Microstrip patch	2.66	4.25
Phased Array	10	10

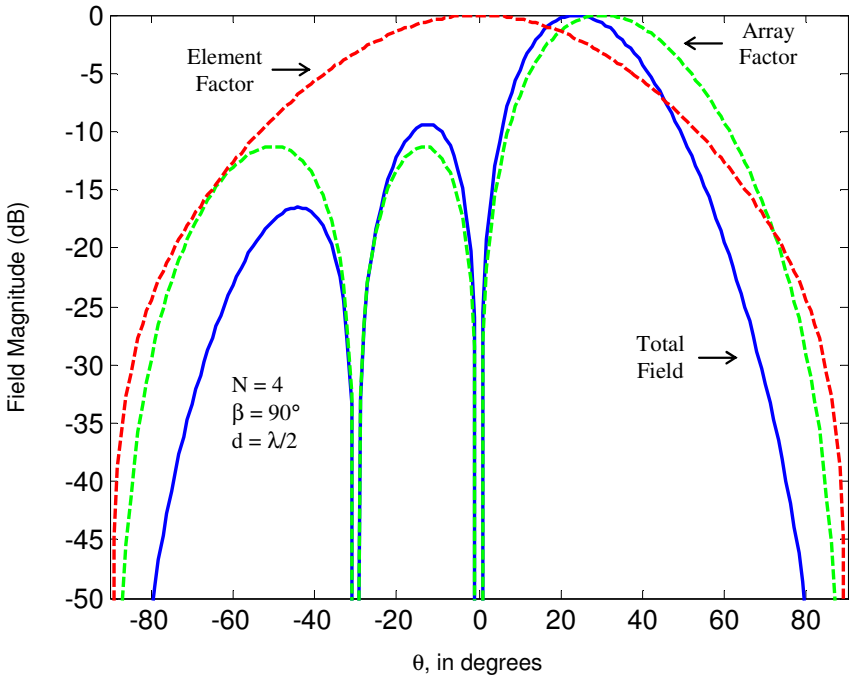


Figure 5.5. The field magnitudes in H-plane for the element factor, array factor, and total field for a linear array of 4 patch antennas with a spacing and progressive phase shift between elements of λ/2 and 90°.

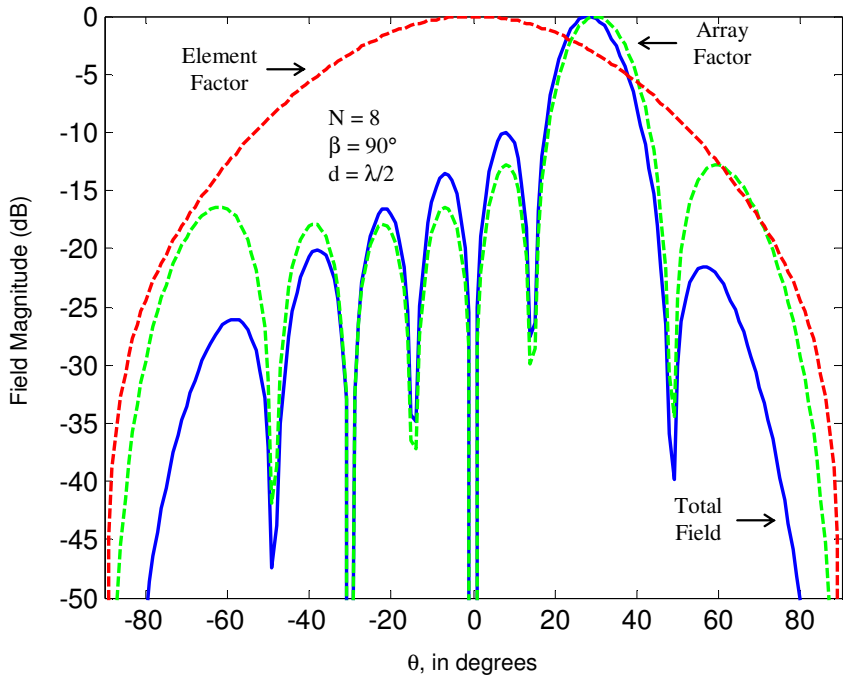


Figure 5.6. The field magnitudes in H-plane for the element factor, array factor, and total field for a linear array of 8 patch antennas with a spacing and progressive phase shift between elements of λ/2 and 90°.

5.3. The Radiation Pattern Measurements

Figure 5.7 shows the fabricated monolithic phased array. The fabricated device is attached a PCB card that is used to apply DC voltages to the phase shifters on which external mechanical switches are located. Figure 5.8 shows the constructed setup in the anechoic chamber for radiation pattern measurements. The mechanical switches are located at the back of the PCB card in order not to affect the radiation characteristics. The phased array is fixed to the card with the aid of white epoxy. The DC connections from the card to the phase shifter pads are provided by wire-bonds.

The PCB is gold coated on top of copper metallization in order to be able to implement wire-bonding. The SMA connector is attached the antenna feed line using conductive epoxy instead of soldering. If soldering is used for this connection, the circuit metallization is peeled off from the substrate since it is quite thin (1.5-2 μm) and can not withstand to soldering temperature. The detailed photograph of the SMA connector attachment is shown in Figure 5.9. Silver epoxy requires temperature curing to achieve high levels of conductivity. However the curing temperature should be kept as low as possible (around 70 °C) in order not to affect the suspended MEMS structures.

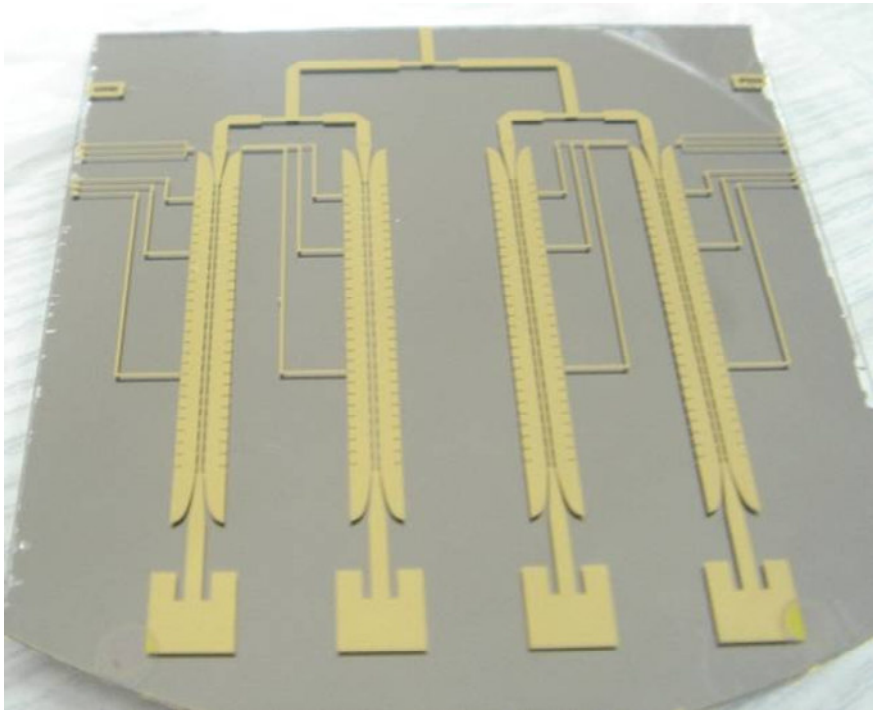


Figure 5.7. The photograph of the phased array fabricated using the surface micromachining process developed at METU. The total chip size is about 6 cm × 5 cm.

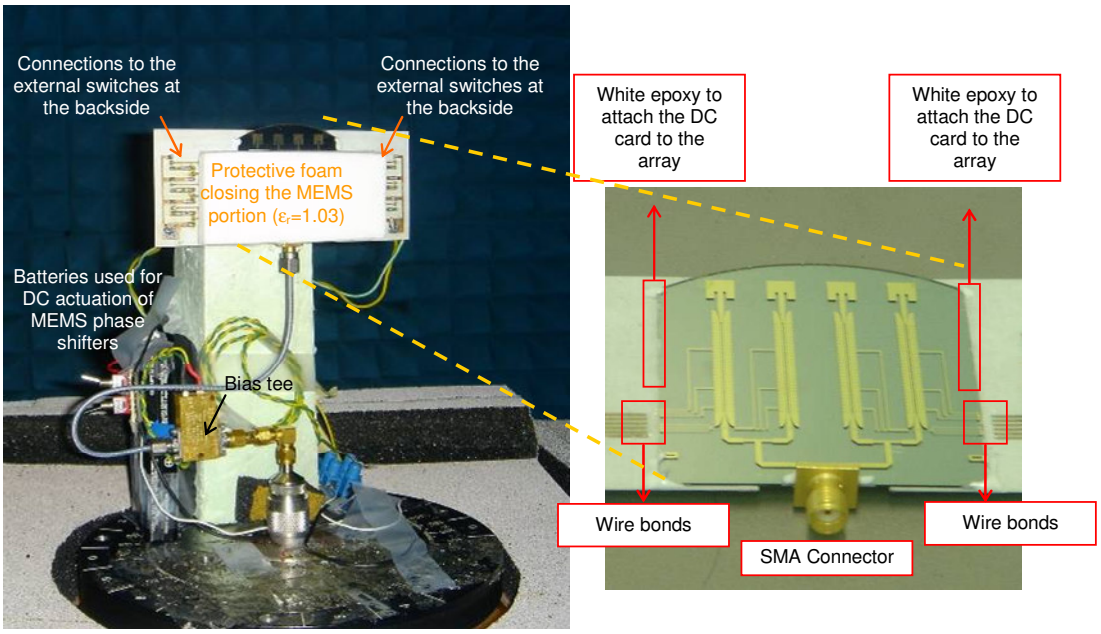


Figure 5.8. The setup used for the radiation pattern measurements of the phased array which is attached to a PCB card. The card includes external switches at the backside which are used to actuate the phase shifters with the desired combinations.

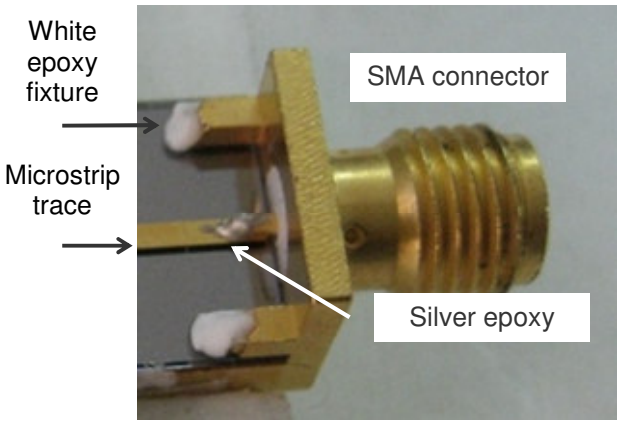


Figure 5.9. The detailed view of the attachment of SMA connector to microstrip trace using silver epoxy.

Figure 5.10 shows the reflection coefficient characteristics of the phased array. The resonant frequency of the system is at 14.62 GHz with a 10 dB bandwidth of 6 %. Figure 5.11 gives the radiation patterns of the phased array for different phase shifter settings. It is observed that, the beam can be tilted by 4° and 14° when the progressive phase shift is adjusted nearly 20° and 50°, respectively. These values are quite close to the expected amount of steering. The backradiation levels around -15 dB are acceptable considering edge diffraction effects, the PCB card, and the mechanical switches attached to this card for DC biasing of the RF MEMS phase shifters.

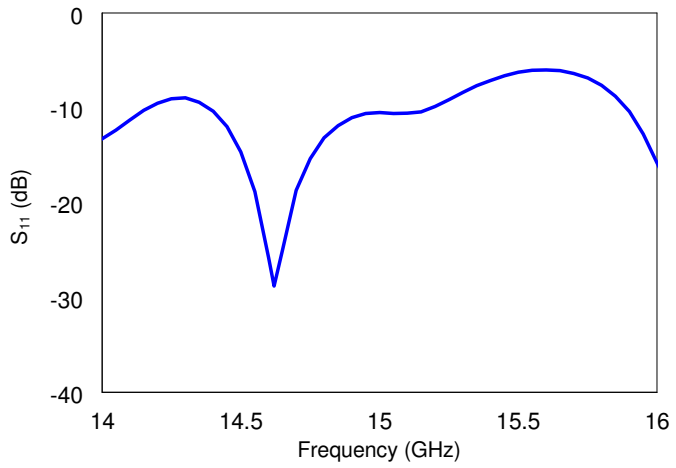


Figure 5.10. The measured return loss of the monolithic phased array. The resonant frequency of the system is at 14.62 GHz with a 10 dB bandwidth of 6 %.

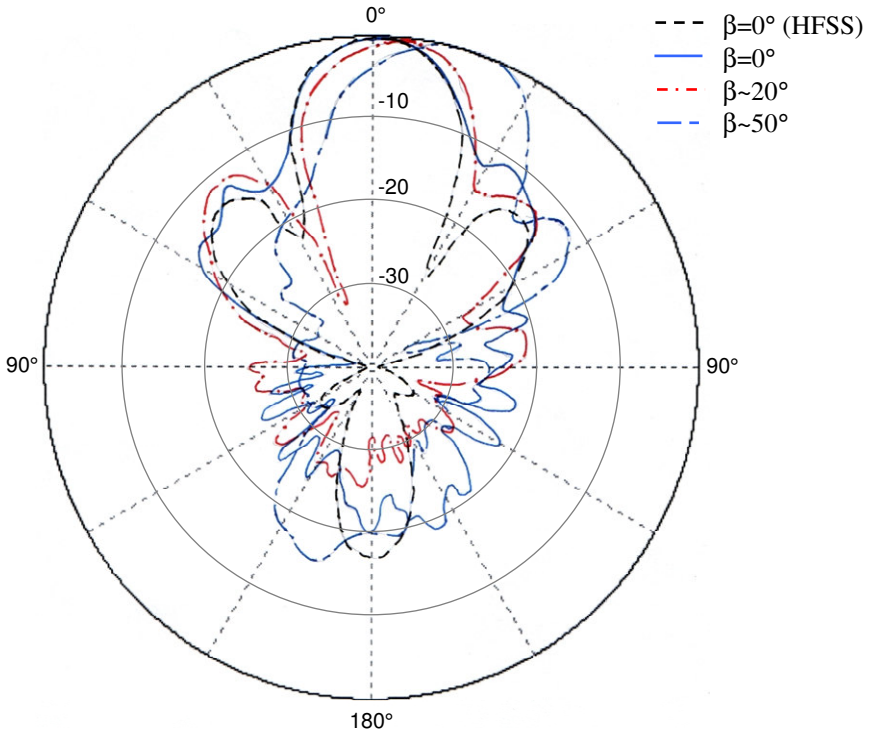


Figure 5.11. The radiation pattern of the phased array for different progressive phase shifts.

5.4. Design of a phased array with slot-coupled antenna configuration

The monolithic phased array can be alternatively designed and fabricated with slot (aperture)-coupled antenna configuration, where a metal ground planes is inserted between the radiating elements and the feed network to prevent the main beam from interfering with the feed network. Figure 5.12 shows the conceptual view of a phased array with slot-coupled patches. Figure 5.13 gives the layers of the phased array configuration where high-resistivity silicon (HRS) wafer with a thickness of 150 µm for MEMS devices and glass substrates with a thickness of 500 µm for patch

antennas are employed as the two substrates to be stacked. Eutectic bonding technique between the common ground metallization deposited on the glass substrate and bare silicon surface is a suitable solution to bond these substrates. Thin HRS substrates enable a designer to realize a switched line phase shifter on microstrip transmission line where series RF MEMS switches are utilized as the routing elements between different paths. Figure 5.14 and Figure 5.15 show the layout of the RF MEMS series switch and 2-bit RF MEMS switched line phase shifter, respectively. RF MEMS switches have a narrowed RF signal line at the recessed part to minimize the fringes and coupling between the ports when the bridge is in the upstate. The switch provides isolation better than 25 dB for the upstate; return loss better than 30 dB, and insertion loss lower than 0.1 dB for the downstate from DC to 40 GHz. This excellent performance, particularly the isolation performance, can not be sustained if the HRS substrate is altered with the glass substrate since the fringes at the recessed end of the transmission line of the switch implemented on a 150-µm thick HRS substrate are very low compared to that of the switch realized on a 500-µm thick glass substrate. The switched line phase shifter utilizing these series switches provides phase shifts of 35°/70° and their combinations depending on the selection of switches. The shortest path is Path 1-Path 3 (00 state, 0°) whereas the longest path is Path 2-Path 4 (11 state, 105°). In order to select a patch, the two switches on each path are actuated at the same time. Therefore, each state of the phase shifter requires the actuation of 4 switches at the same time. Figure 5.16 gives the RF simulation results of the phase shifter for different states. The designed phase shifter structure shows wideband operation with the aid of added inductive matching section at the tee-junctions.

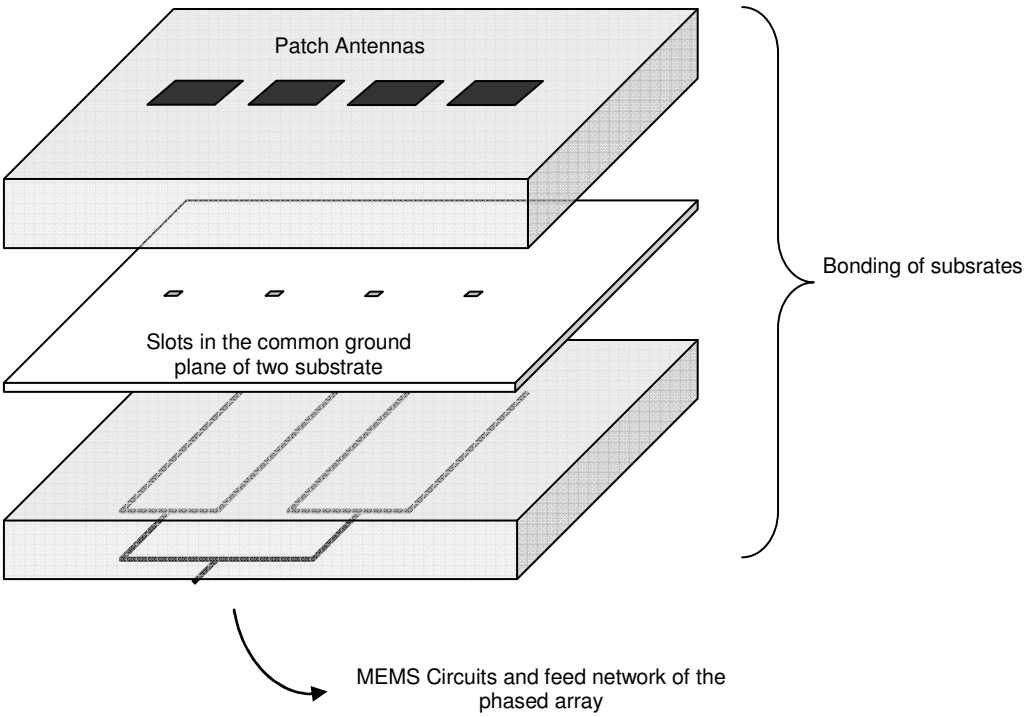


Figure 5.12 Conceptual design of a phased array with slot-coupled antennas.

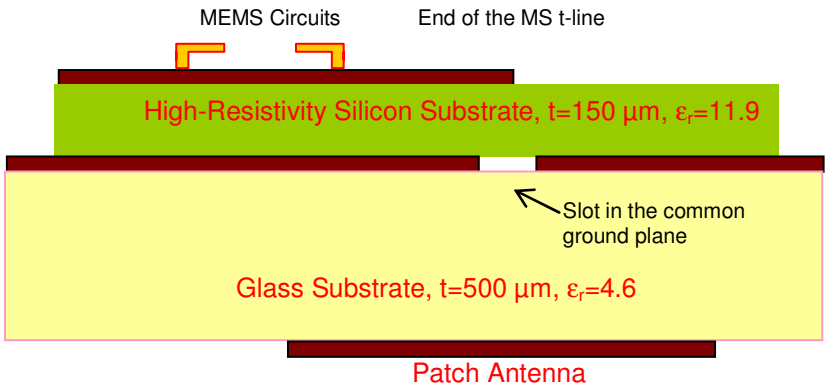


Figure 5.13 The layer configuration of the phased array with slot-coupled patch antennas.

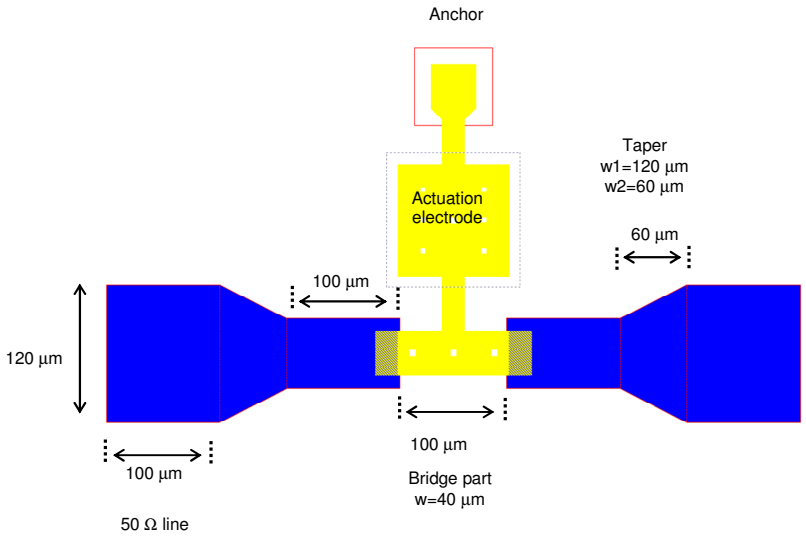


Figure 5.14 The layout of the series switch on a microstrip line on HRS substrate.

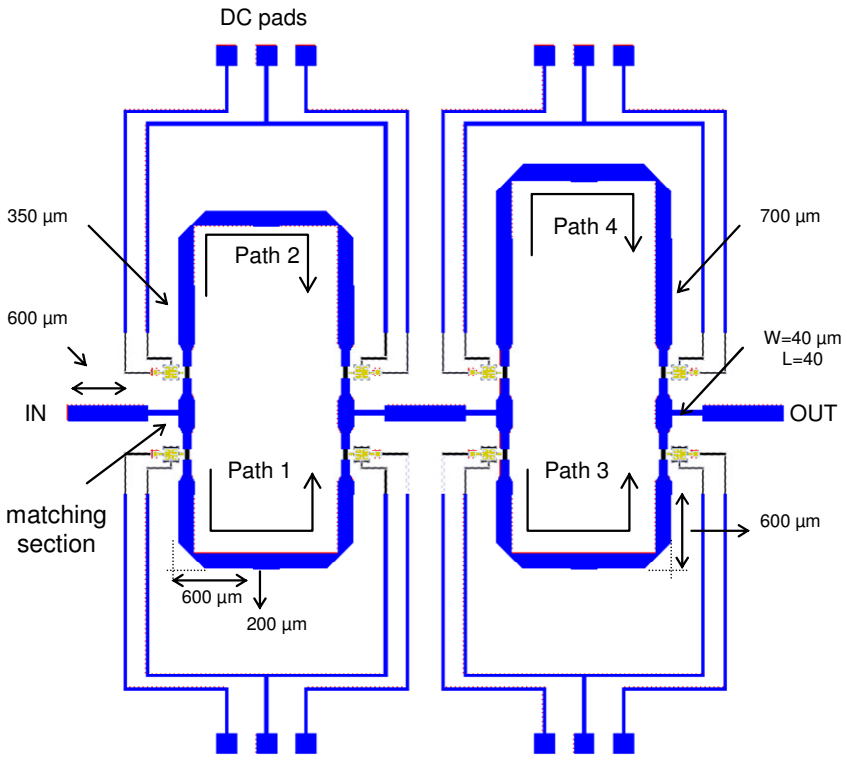


Figure 5.15 The layout of the switched line phase shifter on HRS substrate.

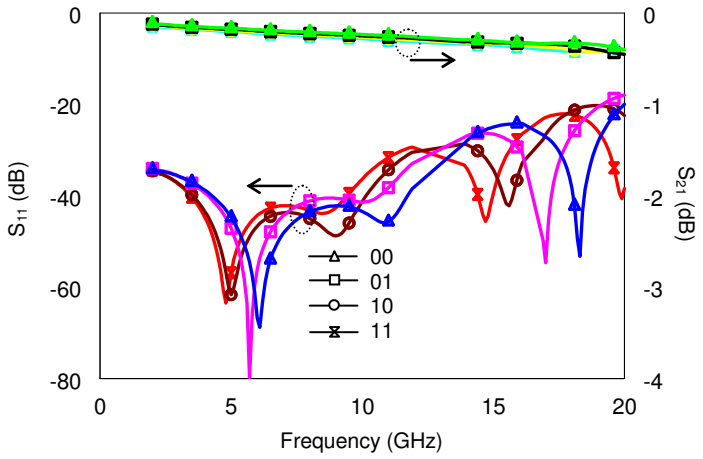


Figure 5.16 Simulation results of the RF MEMS switched line phase shifter for different states.

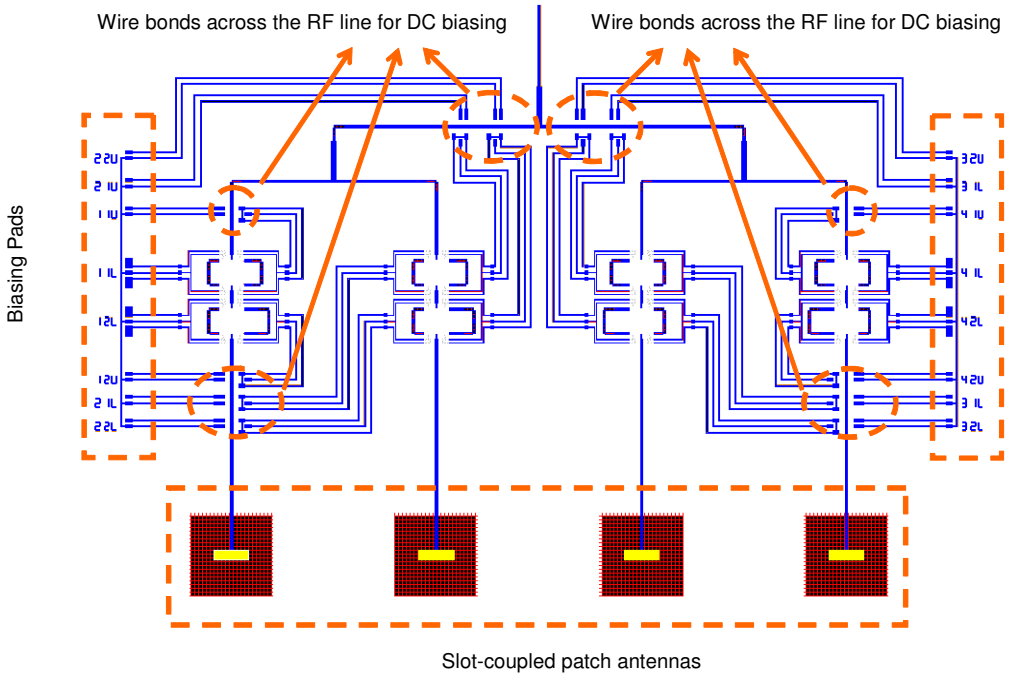


Figure 5.17 The layout of the phased array with switched line phase shifters and slot-coupled patch antennas.

Figure 5.17 gives the layout of the phased array with slot-coupled antennas and switched line phase shifters. The structure has a total of 32 series RF MEMS switches requiring a bundle of actuation pads and wire-bonds. Moreover, the DC actuation of the phase shifters at the inner portion of the array requires additional wire-bonds over the RF lines. Figure 5.18 and Figure 5.19 show the cross-sectional and top view of the conceptual designs of the setups to test the phased array structure. In order to construct these setups, the MEMS part of the array is first placed on a supporting substrate (substrate no: 1 in Figure 5.18) with adhesive white epoxy. This stacked structure, again using adhesive epoxy, is attached to the substrate where SMA launcher is connected (substrate no: 2 in Figure 5.18). The RF signal line and the ground vias of the attached substrate as well as the DC pads on the attached substrate are wire-bonded to the MEMS phased array. It should be noted here that the antenna radiation properties is affected from the supporting substrate above the patch. Therefore the antenna should be designed together with this layer. The other option is to create windows about a wavelength on the supporting substrate in order not to affect the radiation properties of the antenna.

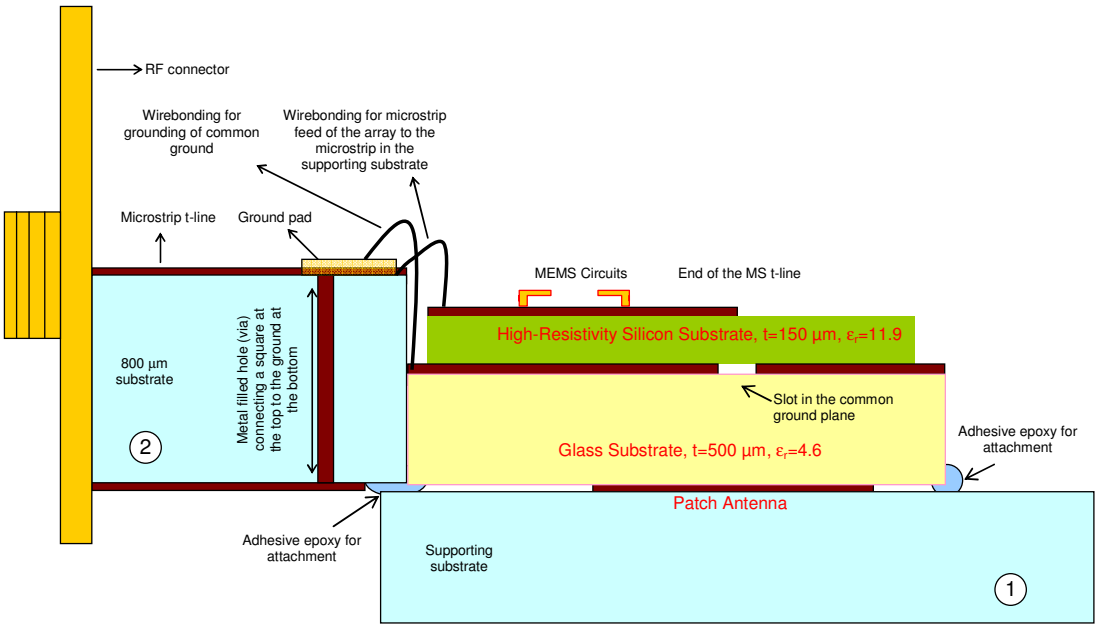


Figure 5.18 The cross-sectional view of the setup to test the phased array with slot-coupled patch antennas.

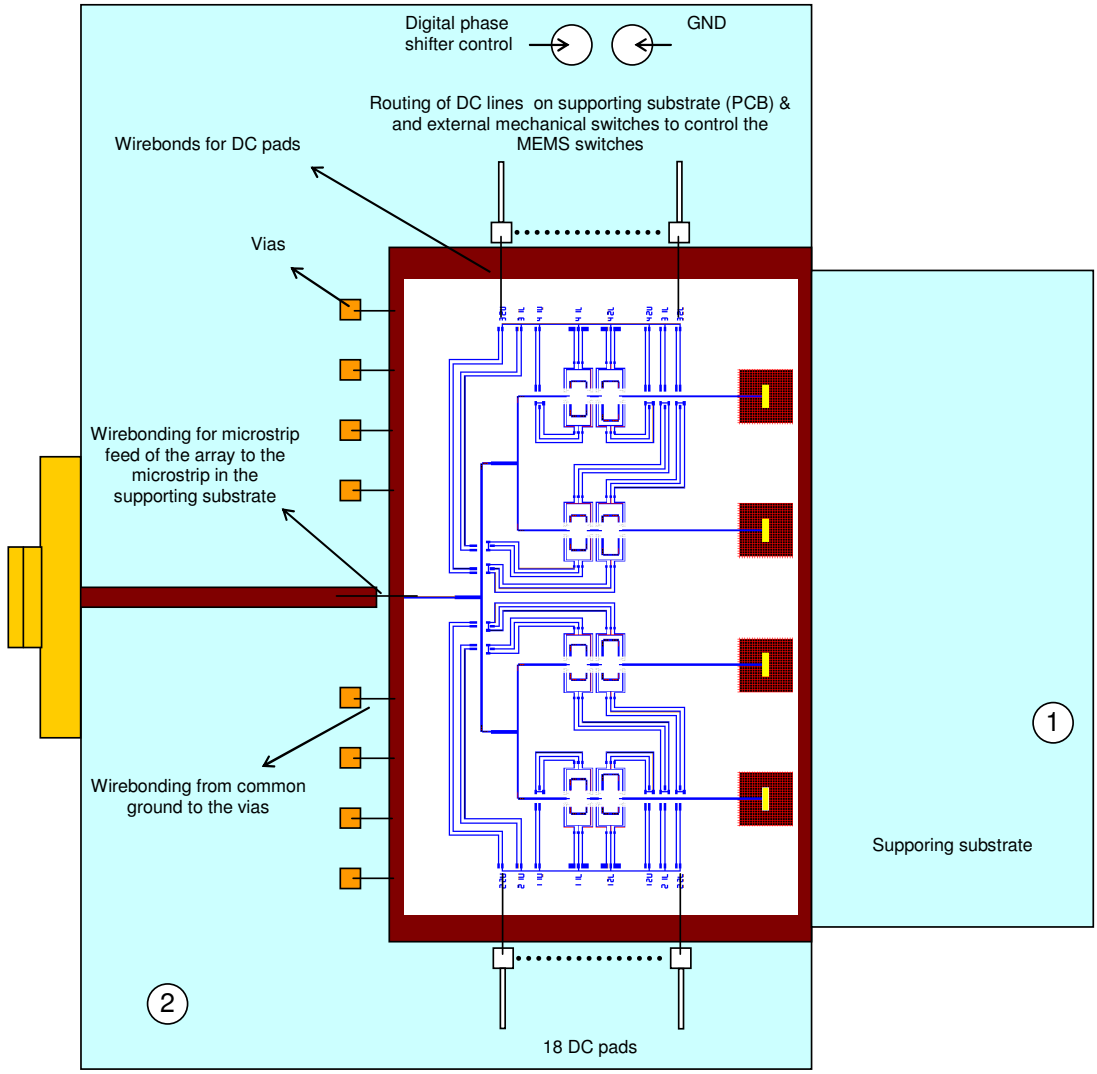


Figure 5.19 The top view of the setup to test the phased array with slot-coupled patch antennas.

CHAPTER VI

CONCLUSION AND FUTURE WORK

This thesis presents a novel phased array structure using RF MEMS technology. The phased array system is fabricated using the in-house surface micromachining process developed at METU. The system employs 3-bit DMTL type RF MEMS phase shifters which are composed of high-impedance transmission lines ($Z_o > 50\,\Omega$) loaded with MEMS bridges in series with MAM capacitors. The phase shifter can provide nearly 20°/50°/95° phase shifts and their combinations at the expense of 1.5 dB average insertion loss at 15 GHz, showing low-loss performance compared to semiconductor counterparts. The reduction of the losses in the phase shifting elements of a phased array can be used to eliminate one of the amplification stages both decreasing the system costs and DC power consumption. Radiation pattern measurements shows that the beam can be steered to the desired angles by the appropriate settings of MEMS phase shifters. This work shows that the use of RF MEMS phase shifters monolithically integrated with patch antennas and feed network can offer better performance phased arrays by reducing the DC power consumption, packaging costs and the size of the system compared to arrays with ferrite or semiconductor based phase shifters.

Based on the research in the frame of this thesis, the conclusions can be drawn as follows:

- RF MEMS phase shifter presented in this work shows low-loss characteristics compared to semiconductor based counterparts. This improvement may lead to an innovative design approach for phased arrays. In the current phased arrays, there is a power amplifier/low-noise amplifier chip at each antenna element in order to reduce the effects of the loss of the phase shifter. RF MEMS may eliminate the requirement reducing the number of active elements in a phased array, which leads to a decrease in the system level costs.

- The measured results for the DMTL structure with MAM capacitors provide a well-defined starting point for the design of other components employing similar loaded lines such as impedance matching networks and filters.

- Inductively tuning approaches developed for RF MEMS shunt switch structures is a solution for tuning the isolation bandwidth to *X*- and *Ku*-band.

- The monolithic phased array fabrication shows the capability and maturity of METU RF MEMS process which can be adopted to produce many other components.

The future works are summarized below:

- The loss of the phase shifter structure presented in this work can be further improved to about 1.3 dB at 15 GHz, by using higher resistivity bias lines, which can be achieved by using different materials or different deposition techniques. Moreover the reduction in the inserted phase shift performance of the phase shifter can be eliminated by changing the layout of the device for the static capacitor region according to the measured values.

- The monolithic phased array can be fabricated with slot-coupled stacked configuration, where metal ground planes are inserted between radiating elements and feed networks to prevent the main beam from interfering with feed network. The fabrication of such a system requires bonding of substrates and two sided alignments. The development of stacked substrate processing is a future work of the METU RF MEMS group for the production of antennas and antenna systems that do not interfere with the other elements of the circuits.

- Besides the control on the phase of the antennas, in order to reduce the side-lobe levels of the radiation pattern, amplitude control can also be applied. Vector modulator circuits using MEMS technology, which provides a control on both amplitude and phase of the input signal, has been proposed by the METU RF MEMS group and will be fabricated soon. Depending on the measurement results of vector modulator circuits using MEMS technology, the fabrication of array structures employing vector modulator circuits may be considered.

- The reliability of MEMS structures is a major concern for long term applications. The reliability of RF MEMS switches is currently a subject of the METU RF MEMS group and it will be investigated in more detail in the next years. The failure mechanism of RF MEMS devices such as mechanical failures and stiction due the charging should be clearly identified and possible solutions should be proposed in order to have the technology more mature.

- RF MEMS devices are very sensitive to humidity and must be packaged in hermetic or near-hermetic seals. Packaging is a critical and challenging part of the RF MEMS technology. It will be one of the research items of the group in the next years.

- The other important future work is the integration of MEMS devices with active elements, which fulfills the requirement to have a complete RF system. The integration techniques such as flip-chip, wire bonding should be studied in the frame of this research item.

As a result, it is believed that the design, fabrication, and measurement experience gained during the implementation of the novel monolithic array research period to present this thesis makes a significant contribution to the development of RF MEMS technology in our country. This experience can be adopted not only to build many similar devices to be commercialized but also to explore different research fields about future's wireless systems.

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APPENDIX

FABRICATION DETAILS

1.1. Definition of Some MEMS Fabrication Terms

Lithography: A process common in microfabrication for delineating a pattern image in a photosensitive polymer. The polymer, or photoresist, can then be used as a masking layer to transfer the pattern into the underlying substrate.

Photoresist: A light sensitive material that is spun-coated. When an area of the photoresist is exposed to UV light, it can be removed in an aqueous solution called "developer" rendering visible the hidden image (positive photoresist). There are also some types of photoresist which behave vice versa: the exposed regions do not dissolve in the developer (negative photoresist).

Developer: A chemical solution that selectively removes exposed or unexposed areas of photoresist, depending on the polarity of the resist.

Sputtering: A process to deposit a thin film on the surface of a substrate. It involves the removal of material from a target by ion bombardment and subsequent redeposition on the substrate.

Electroplating: It is an industrial method adopted to MEMS technology for the patterned deposition of metal films. Electroplated metals can take the shape of underlying substrate and a photoresist mold.

PECVD: Plasma enchanced chemical vapor deposition**.** A technique which is used to deposit dielectric films (silicon dioxide and silicon nitride) with gaseous mixtures in an RF plasma environment.

Wet etching: Process term used for the selective etching of a material from wafer surface by means of wet chemical agents.

Dry (RIE) etching: A method applied with reactive ion etching equipment where specific gaseous mixtures in RF plasma environment are used to selectively etch materials.

Sacrificial layer etching: A micromachining processing method in which an intermediate layer sandwiched between two layers of a different material is completely etched and selectively removed.

Critical Point Dryer (CPD): An equipment which is used for drying the wet released suspended structures without sticking due to surface tension. The system fills the chamber with liquid CO_2 removing the chemicals underneath the suspended structures. By heating and pressurizing the chamber, the critical point for CO_2, in which CO_2 exists as a liquid and a vapor state at the same time, is achieved. Then pressure is reduced, keeping CO_2 in vapor state and drying the samples.

Acetone: A solvent that is used to strip the photoresist off from the wafer surface.

IPA (isopropyl alcohol): A solvent that is used to remove the traces of acetone.
HF: Hydrofluoric acid.

BHF: Buffered Hydrofluoric acid. NH_4:HF 1:5

Piranha solution: A wafer cleaning solution. H_2SO_4:H_2O_2 1.2:1

DI: Deionized water used for rinsing the wafers in cleanroom.

N_2 Gun: A gun attached to a nozzle used for the accelerated drying of the wafers.

HMDS: A chemical that is spun on the wafer before photoresist to enhance its adhesion to the wafer.

1.2. Detailed Fabrication Flow

1.2.1. Wafer Cleaning

- Piranha cleaning of glass wafers using H_2SO_4:H_2O_2 1.2:1
- DI rinse ×2 (15 min each)
- Dry with N_2 gun
- Dehydration (120 °C 20 min)

1.2.2. Si-Cr Bias Resistor Layer

- RF sputter from Si-Cr target, 10×10^{-3} mbar, 100 W, 90 minutes, for a 2000-Å thick bias resistor deposition
- Dehydration (120 °C 20 min)
- Spin HMDS as adhesion layer
- Spin S1828 for 30 secs at 3750 rpm

- Softbake at 115 °C for 1 min 20 secs on the hotplate
- Align wafer and expose 8 secs at 15 mW/cm^2
- Develop in MF26 A for 1 min
- Hardbake at 120 °C for 10 min in the oven
- Descum: O_2 plasma, 0.3 mT, 300 W, 1 minute
- Etch Si-Cr in BHF for 4-5 minutes
- Strip photoresist-spray acetone and IPA
- O_2 plasma for 10 minutes

1.2.3. Base Metallization

[*] *Gold electroplating is not mandatory. Base metallization can directly be obtained by depositing thicker (300 Å/7000 Å) sputtered Ti/Au*

- Dehydration (120 °C 20 min)
- DC Sputter from Ti/Au target for base metal seed layer,
    - 2×10^{-3} mbar, 300 W, 100 secs, for a 300 Å-thick Ti
    - 2×10^{-3} mbar, 150 W, 600 secs, for a 3000 Å-thick Au
- Dehydration (120 °C 20 min)
- Spin AP140 as adhesion layer
- Spin SPR220-3 for 30 secs at 3750 rpm
- Softbake at 115 °C for 1 min 20 secs on the hotplate
- Align wafer and expose 16 secs at 18 mW/cm^2
- Relaxation period for 30 minutes in humidity environment
- Develop in MF24 A
- Hardbake at 120 °C for 10 min in the oven
- Descum: O_2 plasma, 0.3 mT, 300 W, 1 minute
- Gold electroplating for 10 min with 60 mA current
- Strip photoresist-spray acetone and IPA

- Dehydration (120 °C 20 min)
- Spin HMDS as adhesion layer
- Spin S1828 for 30 secs at 3750 rpm
- Softbake at 115 °C for 1 min 20 secs on the hotplate
- Align wafer and expose 8 secs at 15 mW/cm^2
- Develop in MF26 A for 1 min
- Hardbake at 120 °C for 10 min in the oven
- Descum: O_2 plasma, 0.3 mT, 300 W, 1 minute
- Etch Au and Ti
- Strip photoresist-spray acetone and IPA
- O_2 plasma 10 minutes

1.2.4. Backside Metallization

- Dehydration (120 °C 20 min)
- DC Sputter from Ti/Au/Ti target-backside metallization
    - 2×10^{-3} mbar, 300 W, 100 secs, for a 300 Å-thick Ti
    - 2×10^{-3} mbar, 150 W, 600 secs, for a 3000 Å-thick Au
    - 2×10^{-3} mbar, 300 W, 100 secs, for a 300 Å-thick Ti

1.2.5. Isolation Layer Deposition and Pattern

- PECVD nitride deposition-isolation layer deposition
- Dehydration (120 °C 20 min)
- Spin HMDS as adhesion layer
- Spin S1828 for 30 secs at 3750 rpm
- Softbake at 115 °C for 1 min 20 secs on the hotplate.
- Align wafer and expose 8 secs at 15 mW/cm^2

- Develop in MF26 A for 1 min
- Hardbake at 120 °C for 10 min in the oven
- Descum: O_2 plasma, 0.3 mT, 300 W, 1 minute
- RIE-Nitride etch
- Strip photoresist-spray acetone and IPA. SVC-175 stripper is required for the residues on top of silicon nitride.

1.2.6. Sacrificial Layer Formation

- Dehydration (120 °C 20 min)
- Spin PI2737 for .30 secs at 3000 rpm
- Softbake at 75 °C for 4 min 30 secs on the hotplate.
- Align wafer and expose 15 secs at 18 mW/cm2
- Develop in DE9040 for 1 min 20 secs
- Rinse in PA401R
- Hardbake: ramp from 50 °C -150 °C in 40 min, hold at 150 °C for 50 min, cool down to 50 °C in 20 min

1.2.7. Structural Layer Deposition and Pattern

- DC Sputter from Au target-structural layer formation
    - 10×10^{-3} mbar, 214 W, 300 secs ×4, for a 1.2-µm thick Au
- Skip Dehydration
- Spin HMDS as adhesion layer
- Spin MaN1420 for 30 secs at 7000 rpm
- Align wafer and expose .13 secs at 15 mW/cm^2
- Develop in MaD532S for 1 min 10 secs

- Hardbake (120 °C 10 min)
- Descum: O_2 plasma, 0.3 mT, 300 W, 1 minute
- Etch Au
- Etch Ti (backside protection)
- Wafer Dicing
- Release
    - RIE-Release (option 1)
        - O_2 and CF_4 plasma
    - Wet Release (option 2)
        - Soak the samples in SVC-175 overnight swirling the chemical
        - Rinse in acetone for 5-6 hours
        - Rinse in IPA for 15 minutes
        - Release in critical point dryer

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INTERNATIONAL CONFERENCE PUBLICATIONS

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