DESIGN AND IMPLEMENTATION OF A CURRENT SOURCE CONVERTER BASED STATCOM FOR REACTIVE POWER COMPENSATION

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Hazım Faruk BİLGİN

ABSTRACT

DESIGN AND IMPLEMENTATION OF
A CURRENT SOURCE CONVERTER BASED STATCOM
FOR REACTIVE POWER COMPENSATION

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This research work is devoted to the analysis, design and development of the first medium power Current-Source Converter (CSC) based distribution-type Static Synchronous Compensator (D-STATCOM) with simplest converter topology and coupling transformer connection. The developed CSC-D-STATCOM includes a +/-750kVAr full-bridge CSC employing Selective Harmonic Elimination Method (SHEM), a 250kVAr low-pass input filter at 1kV voltage level, and a Δ/Y connected coupling transformer for connection to medium-voltage load bus. The power stage of CSC is composed of series connection of natural air-cooled high-voltage IGCT switched at 500 Hz for the elimination of four lowest current harmonic components (5^{th}, 7^{th}, 11^{th}, 13^{th}), and optimized fast recovery high voltage diode in each leg. Reactive power control is achieved by applying the phase shift angle control at fixed modulation index, which is implemented digitally on a DSP microcontroller.

The developed system has been implemented for compensation of rapidly varying reactive power demand of coal mining excavators in Turkish Coal Enterprises. The field test results have shown that the proposed CSC D-STATCOM serves as a

technologically new full substitute of conventional Voltage-Source Converter based D-STATCOM having complex transformer connections in view of relatively fast response in reactive power compensation, very low total demand distortion factors, complying with the IEEE Std. 519-1992 even for the weakest power systems, and acceptable efficacy figures.

Keywords: power quality, reactive power compensation, current source converter, STATCOM, harmonic elimination

ÖZ

REAKTİF GÜÇ KOMPANZASYONU İÇİN
AKIM KAYNAKLI ÇEVİRGECE DAYALI STATKOM
TASARIMI VE UYGULAMASI

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Bu çalışma, orta güç seviyesinde basit çevirgeç yapısına ve transformatör bağlantısına sahip ilk Akım Kaynaklı Çevirgece (AKÇ) dayalı dağıtım tipi Statik Senkron Kompanzatörünün (D-STATKOM) analizi, tasarımı ve geliştirilmesine hasredilmektedir. Geliştirilen AKÇ-D-STATKOM, 1kV gerilim seviyesinde Seçici Harmonik Eliminasyon Metodunu (SHEM) kullanan +/-750kVAr gücündeki AKÇ'yi, 250kVAr gücündeki düşük geçirgen giriş filtresini ve orta gerilim yük barasına bağlantı için Δ/Y bağlı kuplaj transformatörünü içermektedir. AKÇ'nin güç devresi, en düşük dört akım harmonik bileşenin (5.,7.,11.,13.) eliminasyonu amacıyla 500Hz'de anahtarlanan doğal hava soğutmalı yüksek gerilim IGCT ile en uygun, hızlı yüksek gerilim diyodunun her çevirgeç bacağında seri bağlanmasından oluşmaktadır. DSP mikrodenetleyicisinde dijital olarak uygulanan, sabit kipleme endeksindeki faz kayma açması kontrolü ile reaktif güç kontrolü elde edilmektedir.

Geliştirilen sistem, Türkiye Kömür İşletmelerindeki elektrikli kömür kazı makinalarının hızlı değişen reaktif güç taleplerinin kompanzasyonu için uygulanmıştır. Reaktif güç kompanzasyonundaki hızlı tepkisi, IEEE 519-1992

standardındaki en zayıf güç sistemleri için bile uyumlu düşük toplam talep bozulum değeri ve kabul edilebilir verimlilik rakamlarından dolayı önerilen AKÇ D-STATKOM'un, karmaşık trafo bağlantılarına sahip geleneksel Gerilim Kaynaklı Çevirgece dayalı D-STATKOM yerine kullanılabilecek yeni teknolojik bir alternatif olduğunu saha test kayıtları göstermektedir.

Anahtar Kelimeler: güç kalitesi, reaktif güç kompanzasyonu, akım kaynaklı çevirgeç, STATKOM, harmonik eliminasyonu

To My Parents

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I would like to thank also the team of National Power Quality Project of TURKEY (Project No: 105G129) for the measurement facilities provided during the field tests. This research work provides bases for Medium Voltage Active Power Filter and Transmission STATCOM subprojects carried out within the scope of National Power Quality Project of TURKEY in view of the extensive industrial experience gained during the design and implementation phases of the CSC D-STATCOM.

I would like to thank to Dr. Alper Akdağ for his efforts in solving problems about the application and urgent delivery of IGCTs.

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ABBREVIATIONS

CSC ..... Current Source Converter
VSC ..... Voltage Source Converter
THD ..... Total Harmonic Distortion
TDD ..... Total Demand Distortion
PWM ..... Pulse Width Modulation
SPWM ..... Sinusoidal PWM
SVPWM ..... Space Vector PWM
MSPWM ..... Modified Sinusoidal PWM
SHEM..... Selective Harmonic Elimination Method
IGCT ..... Integrated Gate Commutated Thyristor
HV IGBT..... High Voltage Integrated Gate Bipolar Transistor
GTO ..... Gate Turn-Off Thyristor
SCR ..... Silicon Controlled Rectifier
FACTS ..... Flexible AC Transmission Systems
AC ..... Alternating Current
DC ..... Direct Current
FBSOA..... Forward Biased Safe Operating Area
RBSOA ..... Reverse Biased Safe Operating Area
STATCOM..... Static Synchronous Compensator
D-STATCOM ..... Distribution type STATCOM
TSC ..... Thyristor Switched Capacitor
TCR..... Thyristor Controlled Reactor
SVC..... Static VAR Compensator
DSP ..... Digital Signal Processor
VA..... Volt-Ampere
VAR (r) ..... Volt-Ampere Reactive

NOMENCLATURE

M ..... modulation index

θ ..... phase angle between line-to-line voltage and the other line current

ϕ..... phase shift angle defined as θ rads in inductive mode and (π-θ) rads in capacitive mode of operation of CSC STATCOM

f_s ..... switching frequency of power semiconductors

f_1 ..... fundamental frequency, which is also the frequency of power system (i.e., 50Hz)

$f_{carrier}$ .. frequency of carrier signal in PWM applications

f_c ..... corner frequency of low pass input filter

I_{dc} ..... mean value of dc-link current

L_{dc} ..... inductance of dc-link reactor in CSC STATCOM

R_{dc}..... internal resistance of dc-link reactor in CSC STATCOM

I_{R1} ..... magnitude of fundamental-frequency component of converter line current in phase R

I_{RM} ..... maximum reverse recovery current of reverse blocking diode

E_{off} ..... turn-off energy loss of power semiconductor during switching

E_{on}..... turn-on energy loss of power semiconductor during switching

E_{rec} ..... reverse recovery energy loss of reverse blocking diode or symmetrical device

di/dt ... rate of rise or decay in current

I_{TGQM}.. maximum controllable turn-off current

V_F ..... forward voltage drop of power semiconductor during conduction

CHAPTER 1

INTRODUCTION

Power systems are complicated networks with hundreds of generating stations and load centers being interconnected through power transmission lines. An electric power system can be separated into four stages: i) generation, ii) transmission iii) distribution and iv) utilization. The basic structure of a power system is as shown in Fig.1.1. It is composed of generating plants, a transmission system and distribution system. These subsystems are interconnected through transformers T_1, T_2 and T_3.

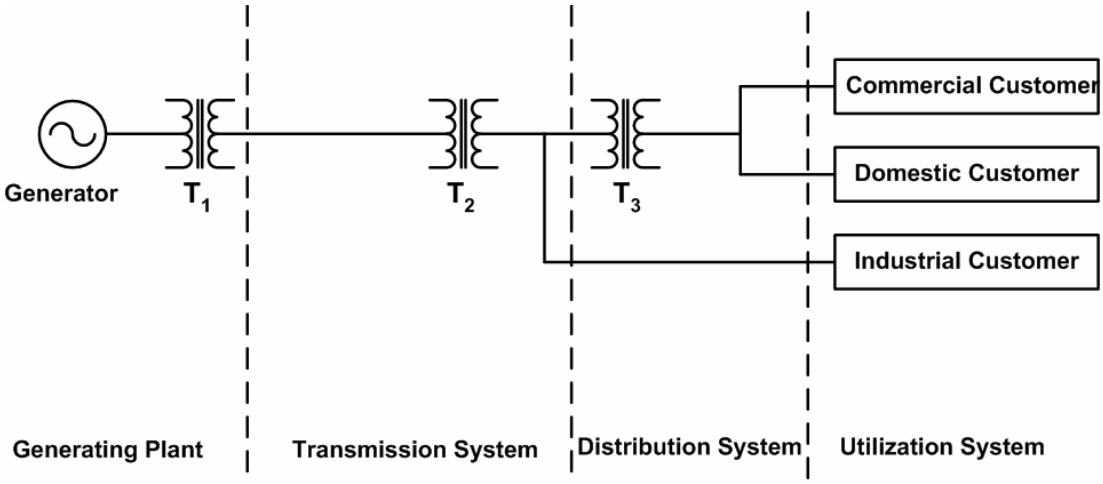


Figure 1.1 Typical power system

1.1 Power Quality Concept

Even a few years back, the main concern of consumers in power system was the reliability of supply which is defined as the continuity of electricity. It is

however not only the reliability that consumers want these days, quality of electricity supply is also very important for consumers. The term, electric power quality, broadly refers to maintaining a nearly sinusoidal bus voltage at rated magnitude and frequency in an uninterrupted manner from the reliability point of view. For a well-designed generating plant which generates voltages almost perfectly sinusoidal at rated magnitude and frequency, power quality problems start with transmission system and stay valid until end users in distribution system. In [1,2], the terms, characterizing the power quality in the power system have been defined and are summarized as follows:

- **Transients:** are defined as the change in a system variable that dissappears during transition from one steady-state operating condition to another and can be classified as impulsive transients and oscillatory transients. Impulse transients are mainly caused by the impact of lightining srikes to the power system. The typical causes of oscillatory transients are capacitor or transformer energization and converter switching. While impulsive transient is a sudden and has non-power frequency change in voltage and current with a fast rise and decaying time, oscillatory transient has one or more sinusoidal components with frequencies in the range from power frequency to 500kHz and decays in time.

- **Short Duration Voltage Variations:** are defined as the variations in the supply voltage for durations not exceeding one minute and caused by faults, energization of large loads that having large inrush currents or rapidly varying large reactive power demands of the loads. These are further classified as voltage sags, voltage swells and interruption.

- **Long Duration Voltage Variations:** are defined as the rms variations in the supply voltage at fundamental frequency for exceeding one minute, such as overvoltage, undervoltage and sustained interruption. The causes of overvoltage (or undervoltage)may be the switching off (or on) of a large load having poor power factor, or the energization of a large capacitor bank or reactors.

- **Voltage Unbalance:** is the condition in which three phase voltages of the supply are not equal in magnitude and may not be equally displaced in time. The primary cause is the single phase loads.
- **Waveform Distortion:** is defined as steady-state deviation in the voltage or current waveform from an ideal sinewave. These distortions are classified as dc-offset, harmonics and notching. The causes of dc-offsets in power systems are geomagnetic disturbances, especially at higher altitudes and half-wave rectifications. These may increase the peak value of the flux in the transformer, pushing it into saturation and resulting in heating in the transformer. Power electronics like UPS, adjustable speed drives cause harmonics in the power systems. Notching is a periodic voltage distortion due to the operation of power converters when current commutates from one phase to another.
- **Voltage Fluctuations:** are defined as the rapid, systematic and random variations in the supply voltage. These are known as "Voltage Flicker". These are caused by rapid and large variations in current magnitude of loads having poor power factor such as arcfurnaces. These large variations in load current causes severe dips in the supply voltage unless the supply bus is very stiff.
- **Power Frequency Variations:** are the variations that are caused by rapid changes in the load connected to the system, such as the operation of draglines connected to a comperatively low inertia system. Since the frequency is directly related to rotational speeds of the generators, large variations in power frequency may reduce the life span of turbine blades on the shaft connected to the generator.

Although these terms, above, are not new, customer awareness on power quality has increased. In recent times, power quality issues and custom solutions have generated tremendous amount of interest among power system authorities and engineers. International Electrotechnical Commission (IEC) and Institute of

Electrical and Electronics Engineers (IEEE) have proposed various standards on power quality [65, 93, 94]. This led to more stringent regulations and limits imposed by electricity authorities although they differ from one country to another in a limited extend. As an example, the progress in both reactive energy limits and distortion limits for the near future is recently imposed by the Energy Market Regulatory Authority of Turkey, as summarized in Table 1.1 and Table 1.2 for the customers directly connected to transmission system such as large industrial plants, electricity distribution companies, etc.

Although terms of power quality are valid for both transmission and distribution systems, their approach to power quality has different concerns. An engineer of transmission system deals with the control of active and reactive power flow in order to maximize both the loading capability and stability limits of the transmission system. On the other hand, an engineer of distribution system deals with load compensation (by means of individual or group compensation) in order to maintain power quality for each load in the distribution system, for example achieving nearly sinusoidal bus voltage at rated magnitude for every load. These interests on power quality have also brought the solution by utilizing power electronic based power conditioning devices.

Table 1.1 Reactive energy limits recently imposed by Energy Market Regulatory Authority of Turkey

Validity of the regulations	Energy Demand / Month		
	Active, %	Reactive, %	
		Inductive	Capacitive
currently in use	100	≤ 33	≤ 20
by the end of 2007	100	≤ 20	≤ 15

Table 1.2 Current limits for distribution and transmission systems imposed by Energy Market Regulatory Authority of Turkey

I_h: Harmonic component of load current at point of common coupling (3 sec avarage value)
I_k: Maximum short circuit current at point of common coupling
I_l: Fundamental component of maximum load current at point of common coupling (15 min avarage value)
(even harmonics are limited to 0.25 times the following odd harmonics)

Voltage Level		Medium Voltage $1<U_n<34.5$					High Voltage $34.5<U_n<154$				
Harmonic No		I_k/I_l					I_k/I_l				
		<20	20-50	50-100	100-1000	>1000	<20	20-50	50-100	100-1000	>1000
Odd harmonics (I_h/I_1) (%)	3≤h≤9	4	7	10	12	15	2	3.5	5	6	7.5
	11≤h≤15	2	3.5	4.5	5.5	7	1	1.8	2.3	2.8	3.5
	17≤h≤21	1.5	2.5	4	5	6	0.8	1.25	2	2.5	3
	23≤h≤33	0.6	1	1.5	2	2.5	0.3	0.5	0.75	1	1.25
	h>33	0.3	0.5	0.7	1	1.4	0.15	0.25	0.35	0.5	0.7
TDD (%)		5	8	12	15	20	2.5	4	6	7.5	10

1.2 FACTS Controllers

The IEEE Power Engineering Society (PES) Task Force of the FACTS Working Group has defined FACTS and FACTS Controller as given below [3].

Flexible AC Transmission System (FACTS): *Alternating current transmission systems incorporating power electronic-based and other static controllers to enhance controllability and increase power transfer capability*

FACTS Controller *A power electronic-based system and other static equipment that provide control of one or more AC transmission system parameters*

The general symbol for FACTS Controller is shown in Fig.1.2a. FACTS Controllers are divided into four categories [3]: i) Series FACTS Controllers, ii) Shunt FACTS Controllers, iii) Combined Series-Series FACTS Controllers, iv) Combined Series-Shunt FACTS Controllers.

i) Series FACTS Controllers: These FACTS Controllers could be a variable impedance such as capacitor, reactor or a power electronic based variable source, which in principle injects voltage in series with the line as illustrated in Fig.1.2b.

ii) Shunt FACTS Controllers: may be variable impedance such as capacitor, reactor or power electronic based variable source, which are shunt connected to the line in order to inject variable current, as shown in Fig.1.2c.

iii) Combined Series-Series FACTS Controllers: are the combination of seperate Series FACTS Controllers, which are controlled in a co-ordinated manner in a multiline transmission system, as illustrated in Fig.1.2d. This configuration provides independent series reactive power compensation for each line but also transfers real power among the lines via power link. The presence of power link between series controllers name this configuration as "Unified Series-Series Controller".

iv) Combined Series-Shunt FACTS Controllers: are combination of seperate shunt and series controller, which are controlled in a co-ordinated manner (Fig.1.2e) or a Unified Power Flow Controller with series and shunt elements (Fig.1.2f). When the Shunt and Series FACTS Controllers are unified, there can be a real power exchange between the series and shunt controllers via power link.

Although Series FACTS Controllers for a given MVA size is several times more powerful than Shunt FACTS Controllers, they have to be designed to ride through contingency and dynamic overloads, and ride through or by-pass short circuit currents [3]. Therefore, Shunt FACTS Controllers are more popular in order to control voltage at and around the point of connection through injection of reactive current (lagging or leading) or a combination of active and reactive current for a more effective voltage control and damping of voltage oscillations.

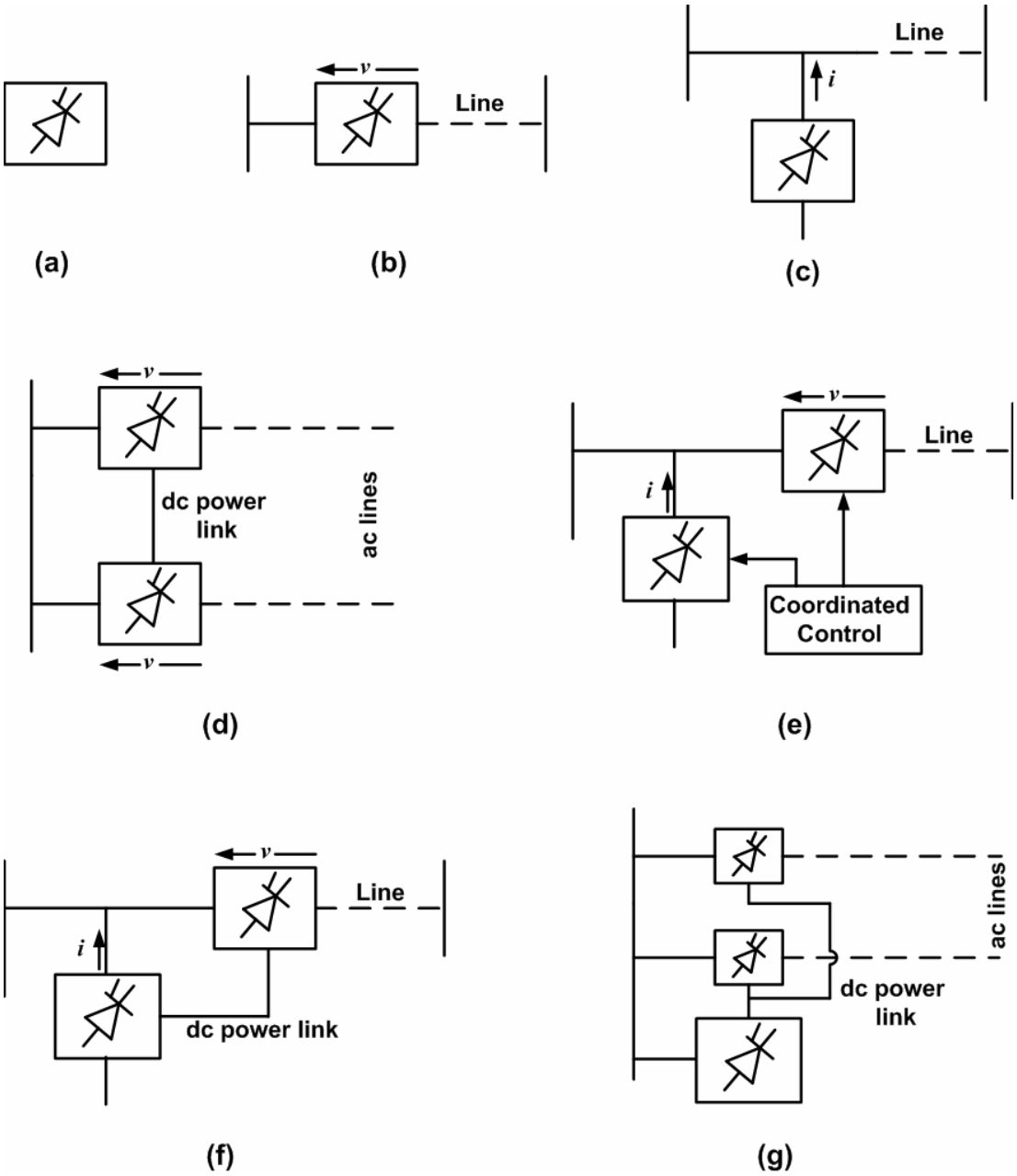


Figure 1.2 Basic types of FACTS Controllers [3]: (a) general symbol for FACTS Controller, (b) series FACTS Controller, (c) shunt FACTS Controller, (d) unified series-series FACTS Controller, (e) coordinted series and shunt Controller, (f) unified series-shunt Controller, (g) unified Controller for multiple lines

Due to the same reasons, Shunt connected FACTS Controllers have also found wide applications in the distribution systems for many years since they present simple, cost effective solutions in load compensation. The common Shunt connected FACTS Controllers are static shunt compensators: SVC and STATCOM.

1.3 Static Shunt Compensators: SVC AND STATCOM

Although static shunt compensators in both transmission systems and distribution systems have the same structure, their objectives are differents due to their concerns on the power quality issues.

The primary objectives of a shunt compensator in a distribution system are as follows:

- compensation of poor load power factor so that the current drawn from the source will have a nearly unity power factor
- suppression of harmonics in loads so that the current drawn from source is nearly sinusoidal
- voltage regulation for the loads that cause fluctuations in the supply voltage
- cancelation of the effect of unbalance loads so that the current drawn from the source is balanced (load balancing)

All of these objectives are not necessarily met for a typical shunt compensator. The required shunt compensator should be designed in view of the needs of load to be compensated since each of these functions has a certain cost to the compensator.

On the other hand, the objectives of these shunt compensator in a transmission system are as given below in order to increase the transmitted power in the transmission lines.

- Midpoint voltage regulation for Line Segmentation in order to increase transmittable power in the transmission system

- End of line voltage support to prevent voltage instability requires the compensation of load having poor factor. This increases the maximum power transmission capability of the transmission line while improving the voltage instability limits.
- Improvement of transient stability margin by increasing the maximum transmittable power in the transmission line.
- Power oscillation damping by exhanging active (real) power with power system so that oscillations in the machine angle due to any minor disturbance can be damped out rapidly.

1.3.1 Static VAr Compensators

According to definition of IEEE PES Task Force of FACTS Working Group:

Static VAr Compensator (SVC): *A shunt-connected static var generator or absorber whose output is adjusted to exchange capacitive or inductive current so as to maintain or control specific parameters of the electrical power system (typically bus voltage)*

This is a general term for a Thyristor Controlled Reactor (TCR) or Thyristor Switched Reactor (TCR) and/or Thyristor Switched Capacitor (TSC) (Fig.1.3). The term, “SVC” has been used for shunt connected compensators, which are based on thyristors without gate turn-off capability.

In a TSC, a capacitor is connected in series with two back-to-back connected thyristors. The control of TSC is obtained by cycle selection principle such that capacitor is totally connected to line by firing thyristors or disconnected by blocking thyristors. An important issue in TSC is to achieve transient free switching. This can only be achieved firing thyristors if the voltage across the capacitor is in either possitive peak or negative peak of the supply voltage.

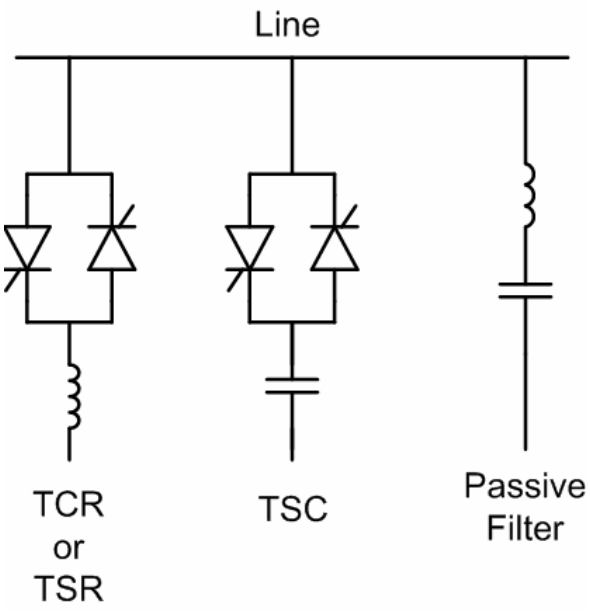


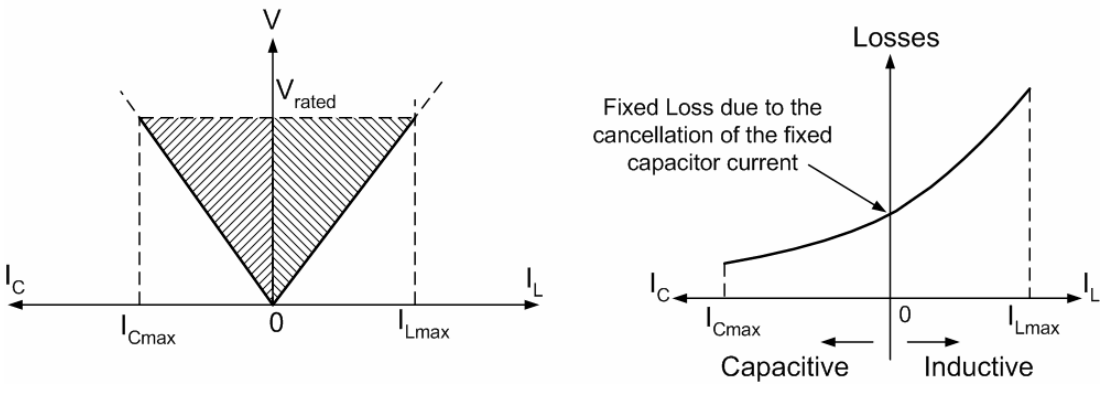
Figure 1.3 Static VAr Compensators: Thyristor Controlled Reactor (TCR) or Thyristor Switched Reactor (TSR), Thyristor Switched Capacitor (TSC), Passive Filter

In a TCR, a reactor is connected in series with back-to-back connected thyristors. By controlling the delay angle, which is defined as the angle between the zero-crossing of line voltage and firing signal of thyristors, it absorbs variable reactive (inductive) power.

For shunt compensation in both transmission and distribution systems, the SVC system can be realized by one of the following combinations:

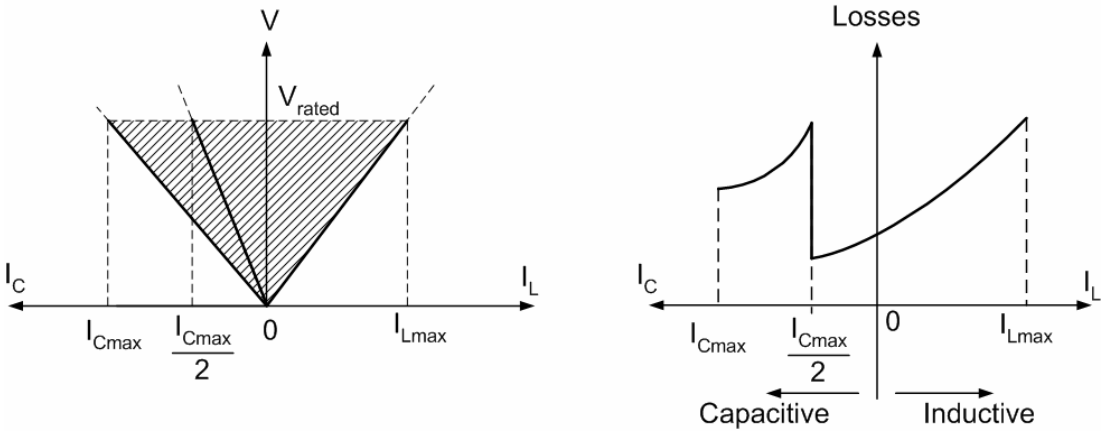
i) Fixed Capacitor and TCR (FC-TCR): In order to achieve variable capacitance and variable inductance, FC-TCR is generally used. The typical operating V-I area of FC-TCR is as given in Fig.1.4a. The fixed capacitor in practive is usually substituted fully or partially by a filter network that has the necessary capacitive impedance at the fundamental frequency to generate the reactive power. Not only this filter network filters out the characteristic low order harmonics of TCR but also the selected low order harmonics injected by the load [5].

ii) A combination of TCR and TSC: Typical loss versus VAr output characteristics of FC-TCR is given in Fig.1.4b. In order to decrease the losses in inductive operating region of FC-TCR and achieve increased operating flexibility, a combination of TCR-TSC with multiple TSC units can be used at the expense of decrease in dynamic response in capacitive region. Then typical operating V-I area and loss versus VAr output characteristics can be improved as shown in Fig.1.5.



(a) (b)

Figure 1.4 For FC-TCR: (a) operating V-I area (b) loss vs. output VAr characteristic [3]



(a) (b)

Figure 1.5 For TSC-TCR: (a) operating V-I area (b) loss vs. output VAr characteristic [3]

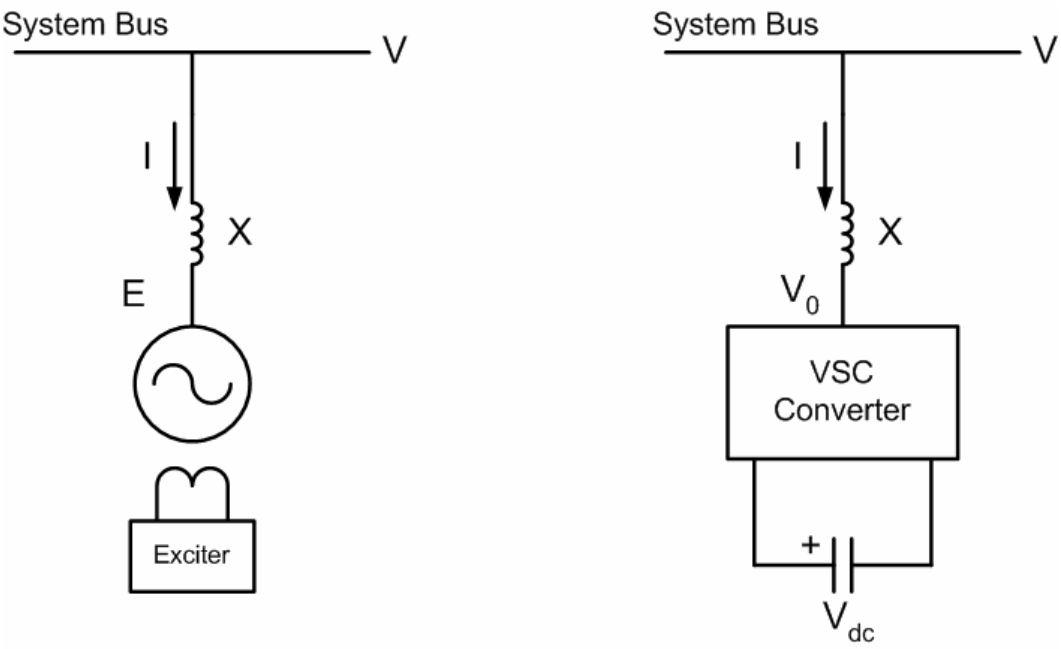
1.3.2 STATCOM

According to definition of IEEE PES Task Force of FACTS Working Group:

Static Synchronous Compensator (STATCOM): *A Static synchronous generator operates as a shunt-connected static var compensator whose capacitive or inductive output current can be controlled independent of the ac system voltage.*

The possibility of generating controllable reactive power directly, without the use of ac capacitors or reactors by various switching power converters was disclosed by Gyugi in 1976 [3]. Functionality, from the standpoint of reactive power generation, their operation is similar to that of an ideal synchronous machine whose reactive power output is varied by excitation control (Fig.1.6a). Like the mechanically powered machine these converters can also exchange real power with the ac system if supplied from an appropriate, usually dc energy source (Fig.1.6b). Because of these similarities with a rotating synchronous generator, they are termed Static Synchronous Generator (SSG). When SSG is operated without an energy source and with appropriate controls to function as shunt-connected reactive compensator, it is termed, analogously to the rotating synchronous compensator (condenser) a Static Synchronous Compensator (STATCOM) or Static Synchronous Condenser (STATCON).

Rotating synchronous condensers (Fig.1.6a) have been used in both distribution and transmission systems for 50 years. However, they are rarely used today because of their following drawbacks: i) require substantial foundations and a significant amount of starting and protective equipment, ii) contribute to the short circuit current, iii) can not be controlled fast enough to compensate for rapid load changes due to the large time constant of their field circuit, iv) have much higher losses as compared with STATCOM [90].



(a) (b)

Figure 1.6 Reactive power generation by (a) a rotating synchronous compensator, (b) voltage source converter based Static Synchronous Compensator (STATCOM)

For the generation of controllable reactive power by the converter can be a voltage source type (VSC) (Fig.1.7a) or a current source type (CSC) (1.7b). However, converters presently employed in FACTS Controllers are based on voltage source converter [3]. The major reasons for this preference are as follows:

i) Current source converters require power semiconductors with bi-directional voltage blocking capability. The available high power semiconductors with gate turn-off capability (GTOs, IGBTs) either can not block reverse voltage at all or can only do it with detrimental effort on other parameters (e.g., increased conduction losses)

ii) Dc-link reactor of CSC is practically more lossy than complementary dc-link capacitor of VSC.

iii) The CSC requires capacitors at its ac terminals while VSC requires reactors, which may be naturally provided by the leakage inductance of the coupling transformer.

Although they have the same structure, STATCOM systems are classified as Transmission STATCOM and Distribution STATCOM (DSTATCOM). While Transmission STATCOM having a larger MVAr rating is intended to inject a set of three balanced quasi-sinusoidal voltages for controlling reactive power flow in transmission system, DSTATCOM performs load compensation, i.e, power factor correction, harmonic filtering, load balancing in the distribution system. Therefore, DSTATCOM must be able to inject an unbalanced and harmonically distorted current to eliminate unbalance or distortions in the load current or the supply voltage [1,7].

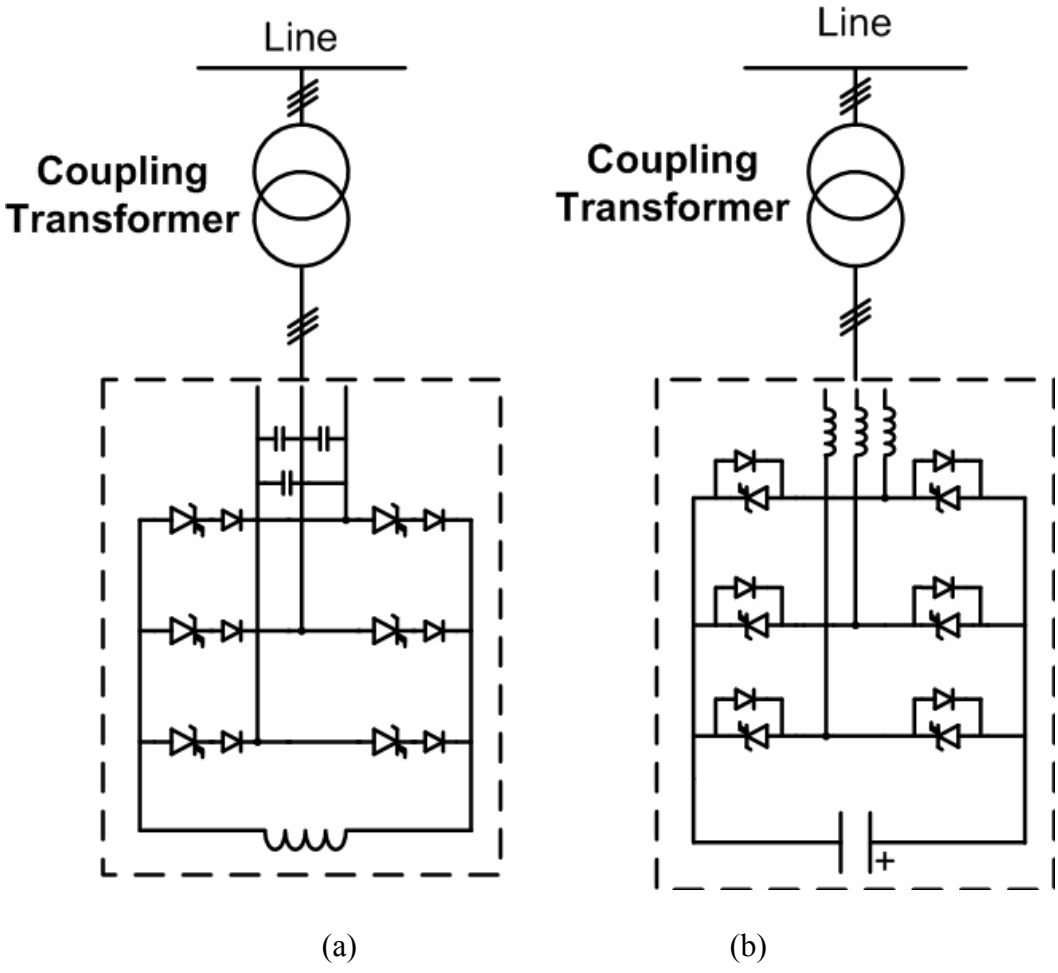


Figure 1.7 STATCOM based on (a) Current Source Converter (CSC) and (b) Voltage Source Converter (VSC)

The single line diagram of basic VSC based STATCOM is shown in Fig.1.6b. From a dc-voltage provided by dc-link capacitor, C, the converter produces a set of controllable three-phase output voltage with the frequency of ac power system. Each output voltage is in phase with and coupled to the corresponding phase of ac system via coupling reactor (including reactance of the coupling transformer). Then, reactive power per phase produced by the converter can be expressed as follows [3],

$$Q = \left(\frac{V - V_0}{X}\right)V = \frac{1 - \left(\frac{V_0}{V}\right)^2}{X}V^2$$

If the amplitude of output voltage (V_0) is increased above that of ac system voltage (V) the converter generates reactive (capacitive) power. If the amplitude of V_0 is reduced to a level below that of ac system voltage (V), then the converter absorbs the reactive (inductive) power.

All of the practical converters so far employed in actual STATCOM applications are composed of a number of elementary converters, shown in Fig.1.8. In transmission STATCOM systems, fully controllable power semiconductors such as GTO, GCT which are switched at supply frequency have been used. Then, harmonics produced by VSC have been eliminated by complex coupling transformer connections and multiphase converter topologies. With the advents in high voltage IGBT technology, DSTATCOMs have been applied to medium voltage distribution systems for harmonic filtering and load balancing in addition to reactive power compensation. These features of DSTATCOM make necessary generation of harmonic components superimposed on the fundamental voltage component at the ac side of VSC by turning on and off IGBTs at frequencies much higher than the supply frequency overlapping with switching frequencies, operation, and control strategies of low voltage shunt active power filters.

The operating V-I area of STATCOM is limited only by the maximum voltage and current ratings of the converter and system components as illustrated in Fig.1.9a. Typical loss versus VAr output characteristics of an actual 100MVA, 48-pulse VSC based STATCOM is shown in Fig.1.9b. [3,6]

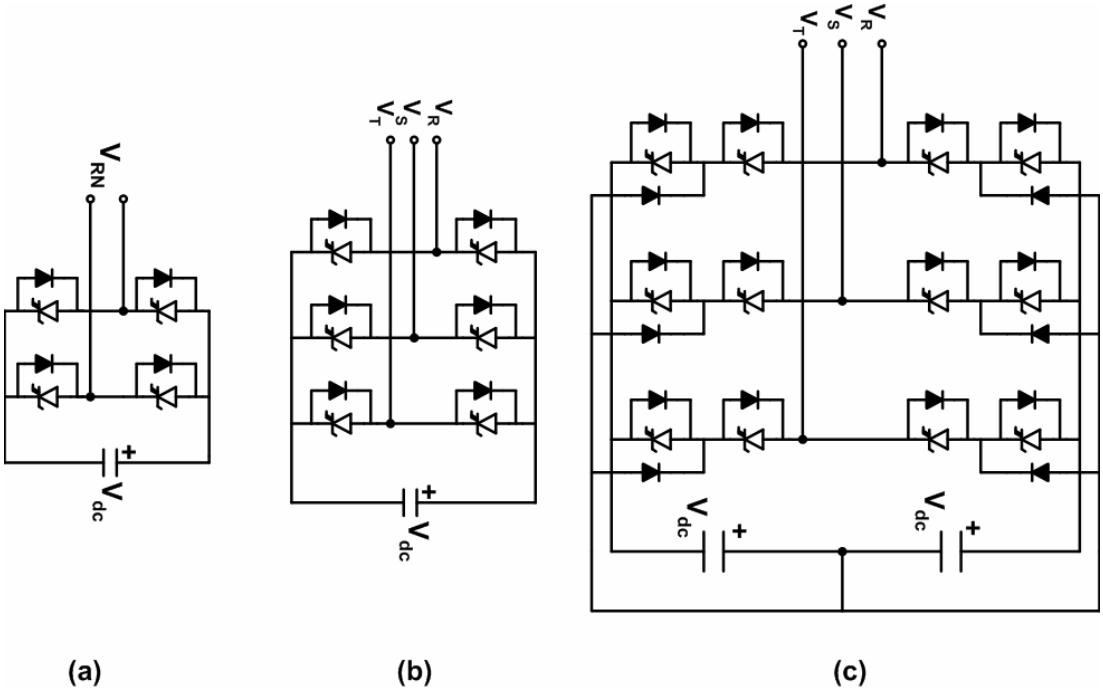


Figure 1.8 Basic converter schemes used for STATCOM [3]
(a) Single phase two-level H-converter
(b) Three-phase two-level 6-pulse converter
(c) Three-phase, three-level 12-pulse converter

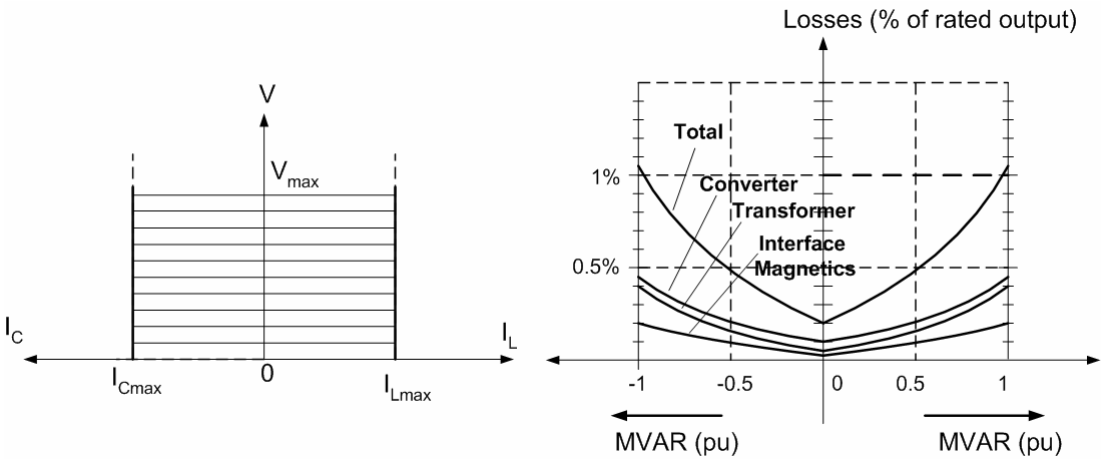


Figure 1.9 For STATCOM (a) operating V-I area (b) loss vs. output VAr characteristic [3]

A brief comparison between SVC and STATCOM can be made in terms of their operational and performance characteristics with the corresponding application benefits:

1) V-I Characteristics: Comparison of Fig.1.9a with Fig.1.7a shows that STATCOM can inject its full reactive current even at very low, typically about 0.2 pu system voltage level. This makes STATCOM superior to SVC in providing voltage support under large system disturbances. The capability of providing maximum compensating current at reduced system voltage enables STATCOM to perform the same dynamic compensation as an SVC of considerably higher rating. STATCOM may have an increased transient rating in both capacitive and inductive region while SVC has no mean to increase the VAr generation since the maximum current it can draw is strictly determined by the size of capacitor and inductors and the magnitude of system voltage.

2) Transient Stability: The ability of STATCOM to maintain full capacitive reactive current at low system voltage makes it more effective than SVC in improving the transient stability of transmission system.

3) Response Time: Attainable response time and bandwidth of the closed loop of STATCOM are also significantly better than those of SVC. This is due to the availability of fully controllable power semiconductors in STATCOM. The practical importance of wide frequency bandwidth can not be overstated for applications requiring fast response, but even in typical transmission STATCOMs which have fully controllable power semiconductor switches with a switching frequency at supply frequency can provide stable operation with respectable response over a much wide variation of the transmission network impedance than is possible with SVC.

4) Capability to Exchange Real Power: For applications requiring active (real) power compensation it is clear that the STATCOM in contrast to the SVC, can interface a suitable energy storage (large capacitor, battery

or super conducting magnetic storage, etc) with the ac system for real power exchange. This potential capability of STATCOM with the control of active and reactive power independently improves the stability limits and efficiency of the power system, enchances dynamic compensation and potentially prevents power outages.

5) Operation in Load Compensation: Although SVC systems have been successfully used in load compensation for harmonic filtering, unbalanced currents, bus voltage regulation, STATCOM having appropriate structure (i.e., by using single phase H bridge for each phase) and power semiconductor switches (such as IGBTs) with pulse width modulation presents more flexible, efficient load compensation. While typical SVC comprises harmonic filters generating reactive (capacitive) reactive power for filtering harmonic of load and its TCR part, STATCOM, namely DSTATCOM can cancel out the load harmonics without the need for bulky filters. Due to its better response time, STATCOM can also perform load balancing or voltage regulation for voltage flicker problem more rapidly.

6) Loss versus VAr output characteristics: Although loss contribution of power semiconductors and their related components, such as snubbers is higher for STATCOM than for SVC, on the avarage overall loss of STATCOM is comparable with that of SVC due to large inductors (i.e, reactors) of SVC.

7) Physical Size and Installation: Since the converter of STATCOM produces both controllable capacitive and inductive reactive power with a relatively small energy storage in the dc-link, the large capacitor and reactor banks with their associated switchgear and protection used in SVC are not needed. This results in a significant reduction in overall size (reported as 30-40% in [3]) as well as in installation labor and cost, furthermore improves the relocability of the system.

1.4 Current Source Converter

Although the possible use of CSCs for reactive power compensation has been known over a quarter of a century [3, 56], it has not been realized for many years due to reasons given in perivious section. In fact, the basic topology of current source converter has been known since the first application of line commutated rectifiers. Line commutated rectifiers have similar the topology as in Fig.1.7b except the ac capacitors since they do not need capacitors at their ac terminal due to their line commutated thyristors. In fundamental topology of CSC given in Fig.1.7b the converter is build up of forced commutated power semiconductors and hence the capacitors at ac terminal provide not only commutation path for the currents of power semiconductors but also low impedance for the high order harmonics injected by the converter.

The advents in power semiconductor and capacitor technology have made PWM voltage source converters popular in power electronics, leaving application of CSC as line commutated thyristorized front end rectifiers in DC drives, or load-commutated thyristorized inverters in MV synchronous motor drives. With the introduction of GTOs and GCTs, PWM CSC has found wide application in MV AC drives due to their simple converter topology, motor friendly waveforms and reliable inherent short circuit protection [4, 22]. PWM CSC has also been used in MV drives as an active front end rectifier [14, 27,31,51] and dc motor drive [53] instead of line commutated thyristor rectifiers, thus eliminating their inherent properties such as poor power factor, distorted line currents. The application of single phase CSC as a resonant inverter in induction heating has also been reported in [78].

The research work on CSC are generally based on its use as a rectifier or inverter. Its control strategies and modulation techniques have been proposed accordingly [11-55]. However, there are limited research on CSC based STATCOM as compared to VSC based STATCOM [56-64]. Among these research work, only [64], which has been the part of this study presents the first application of CSC based STATCOM for load compensation.

A reactive power compensation system which employs a three-phase PWM current source converter which is modulated by optimized PWM patterns stored in an EPROM is presented in [56]. This work also includes the methods of reactive power current control for optimizing the system response, input filter and dc-link reactor design, specification of power semiconductor ratings, and a method of closing reactive power demand loop by using phase angle control. The proposed methods were verified on a 117V, 1.1kVA power circuit. However, filter components and dc-link reactor are not so realistic that the results can not prove viability of CSC based STATCOM.

The research work in [57] is an experimental verification of CSC based STATCOM on a 120V, 500VA laboratory set-up by employing a different control approach: reactive power control by varying modulation index while maintaining constant dc-link current by phase shift angle control. However, the proposed control technique with Space Vector PWM (SVPWM) is not suitable for medium and high power applications.

In order to minimize the switching losses in CSC, [58] proposed a soft-switching scheme by integrating H-type soft switching module to three phase current source converter for static power compensation. By using trapezoidal PWM with a carrier frequency of 5kHz and only phase shift angle control for reactive power control, the proposed topology has been tested on a scaled prototype at 120V/2kVA. The results shows that proposed topology improves higher efficiency at the expense of higher circuit and control complexity.

The simultaneous control of modulation index and phase shift angle is proposed in [59] in order to eliminate oscillations due to poorly damped input filter while improving dynamic response of CSC based STATCOM. For this purpose, full state- feedback and integral controllers are employed by using the state space representation of CSC based STATCOM in dq frame. The proposed control method is compared with phase angle control employing conventional PI controller and the results are verified by 1kVA laboratory set-up.

Due to the non-linearity in state space representation of CSC based STATCOM, there is a difficulty in controller design for CSC based STATCOM. A

new approach for the linearization of state space representation has been proposed in [60]. This approach allows the design of a decoupled state feedback controller. CSC based STATCOM with the proposed controller and SVPWM modulation has been simulated in [60] in order to illustate the excellent current and voltage waveforms as well as very short response time at a relatively low switching frequency of 900Hz.

A comparison between VSC based STATCOM and CSC based STATCOM has been given in [61] in view of their device rating, dc-link energy storage requirement, ac-side waveform quality, start-up and cost. This comparison study shows that CSC based STATCOM has certain advantages over VSC based STATCOM in following points: CSC based STATCOM, i) does not need pre-charging or inrush current limiting scheme ii) can present better ac current waveforms at relatively lower switching frequency iii) does not inject harmonics in the "idle" state. The theoretical results are partly verified by laboratory tests.

The possible application of CSC based STATCOM for the compensation of induction generators has been presented in [62] in order to solve self-excitation and poor voltage regulation problems of induction generators used in renewable energy sources. The proposed application has been illustrated by simulation.

In [63] develepment of Symmetrical Emitter Turn-off Thyristor (ETO) is presented for possible use in CSC application. The novel multilevel CSC, named the parallel-cell multilevel CSC based STATCOM is also proposed in [63]. Its power stage design, modeling, control, and switching modulation scheme are analyzed and illustrated by simulations.

In summary, few researchers has focused on the analysis and design of CSC based STATCOM systems [56-64]. However, with the advents in high voltage, high power semiconductor technology (in IGCT and HV-IGBT technologies) CSC based STATCOM systems employing different VAr control methods and PWM techniques can be increasingly used in the near future as a FACTS Controller in industrial applications.

1.5 Scope of the Thesis

In this research work, it is aimed at developing the simplest CSC based STATCOM topology for medium voltage, medium power industrial applications. Its circuit diagram has already given in Fig.1.7b. It does not contain any complexity such as complex transformer connection, series or parallel connected semiconductors and multilevel converter arrangements. The capabilities, drawbacks, limitations and advantages have been investigated by simulations, laboratory and field tests by considering present high voltage, high power semiconductor technology and expected progress in the near future. Phase shift angle control in order to control generated VAr by STATCOM and Selective Harmonic Elimination to comply with harmonic standards [65] have been exercised for simplest CSC based STATCOM topology. In view of theoretical findings a prototype system has been designed and implemented. To verify theoretical results, the prototype system has been applied to reactive power compensation problem of coal mining excavators and its performance has been tested in the field.

The prototype STATCOM is composed of ±750kVAr CSC, +250kVAr low pass input filter developed at standard highest low voltage level of 1kV and 31.5/1kV, 800kVA, delta-wye connected coupling transformer for connection to the medium voltage bus. The low pass filter of the prototype system is tuned to 200Hz. An air-core reactor is chosen as the magnetic storage element in the dc-link in order to eliminate magnetic saturation risk. A switching element with reverse blocking capability has been formed by combining an asymmetric IGCT and fast soft-recovery high voltage diode. In order to avoid complexity in the control circuit, to minimize switching frequency of the power semiconductors and hence converter losses, phase shift angle control to vary generated reactive power and selective harmonic elimination method (SHEM) to comply with harmonic standards have been employed in the design and implementation. Elimination of only 5th, 7th, 11th and 13th harmonics by SHEM and minimization of higher order harmonics by low pass input filter are found quite satisfactory in complying with associated harmonic standards [65]. Although the simplest medium voltage, medium power CSC based

STATCOM topology has been used to improve reliability, the switching frequency of power semiconductors still remains at a relatively low value of 500Hz.

This research work makes following original contributions to CSC based STATCOM area:

- first design and development work of medium voltage, high power CSC based STATCOM in the world [64, 92],
- first application of CSC based STATCOM to an industrial problem, such as load compensation of coal mining excavators [64],
- presentation of qualititive design criteria based on analysis, simulation and experimental work for CSC based STATCOM,
- verification of designed system by field test results,
- first utilization of series connected asymmetric IGCT and fast recovery diode in CSC based STATCOM,
- application of Selective Harmonic Elimination Technique for eliminating 5th, 7th, 11th and 13th harmonics in order to inject nearly sinusoidal reactive currents while controlling reactive power of CSC based STATCOM

The outline of the thesis is given below:

In Chapter 2, system description and operating principles of CSC based STATCOM is described. After presenting the basic circuit configuration, the principles of reactive power control in CSC are described. After comparing the applicable modulation techniques for CSC, selective harmonic elimination method, which has been applied in this study has been explained. Reactive power control methods for CSC based STATCOM are also discussed. The commutation types in CSC are described in detail

In Chapter 3, the design principles of CSC based STATCOM are presented. First, design specifications of the prototype system are stated. Then, selection criteria for the right power semiconductor among the most candidate power semiconductors applicable to CSC based STATCOM, is given. At the same time, constraints on modulation techniques are discussed and parameters for the chosen modulation techniques are determined. Design criteria of input filter, dc-link reactor,

power stage layout and snubber circuits are also presented in view of simulation results. Protection circuits used in the implemented CSC based STATCOM is discussed. Design of control system including reactive power controller and electronic system are described. Factors increasing VAr generation capability of designed CSC based STATCOM has been discussed at the end of the chapter.

In Chapter 4, field results obtained from the application of developed system for group compensation of coal mining excavators are presented.

General conclusions are given in Chapter 5. Proposals for further work are also given in the same chapter.

In Appendix A, the list of implemented Transmission STATCOM systems in the world is given.

In Appendix B, the derivation of CSC based STATCOM model in dq stationary frame is presented.

In Appendix C, simulation model of CSC based STATCOM in PSCAD/EMTDC is posted.

Derating curves which are used in determination of switching frequency for IGCT is given in Appendix D.

The method for theoretical calculation of power semiconductor losses in current source converter is explained in Appendix E.

In Appendix F, simulation models for analysis of turn-off snubber in MATLAB/Simulink can be found.

In Appendix G, flowchart of implemented software for the reactive power control system is given.

CHAPTER 2

SYSTEM DESCRIPTION AND OPERATING PRINCIPLES OF CURRENT SOURCE CONVERTER BASED STATCOM

2.1 Introduction

In the most general case, a shunt connected compensator in a distribution system can also filter out load harmonics and balance the unbalanced load currents in addition to the correction of load power factor. Each additional capability obviously increases initial cost of the implemented system. However, for the balanced clean loads although their reactive power demand varies rapidly the shunt connected compensator is required only for power factor correction.

The three phase CSC based STATCOM is a shunt connected compensator, which injects nearly sinusoidal three phase balanced currents with adjustable magnitudes and leading or lagging the corresponding line voltages by nearly 90°. Therefore, the three phase CSC based STATCOM can compensate for the balanced loads having rapidly fluctuating reactive power demands of harmonicless loads, such as synchronous or asynchronous motors in Ward-Leonard drives.

In this chapter, the system description and operating principles of three phase Current Source Converter (CSC) based STATCOM will be presented in order to meet following objectives:

- harmonic content of the nearly sinusoidal current produced by STATCOM should comply with IEEE 512 Std 1992 and limits imposed by the Energy Market Regulatory Authority of Turkey,
- the magnitude of the reactive current component produced by STATCOM should be controllable between zero and pre-specified value,

- The STATCOM current can be made either lagging or leading corresponding supply voltage by 90° according to the reactive power demand of the load.

After defining basic circuit topology chosen for the CSC based STATCOM, its operating principles during reactive power control will be explained. Different modulation techniques which are commonly applied to CSC to create nearly sinusoidal currents in the supply lines will be compared and among these modulation techniques Selective Harmonic Elimination Method is going to be explained. Then, the control methods applicable to CSC based STATCOM for reactive power control will be presented. The equivalent circuit model in dq stationary frame will be given in the same section. The current commutations in CSC will also be defined. At the end of the chapter, brief conclusions will be posted.

2.2 Basic Circuit Configuration

The general circuit topology of the three phase Current Source Converter (CSC) based STATCOM is shown in Fig 2.1 [56,57,61-64]. It consists of six fully controllable power semiconductor switches (S_1, S_2, S_3, S_4, S_5, S_6) which have unidirectional current carrying and bipolar voltage blocking capabilities.

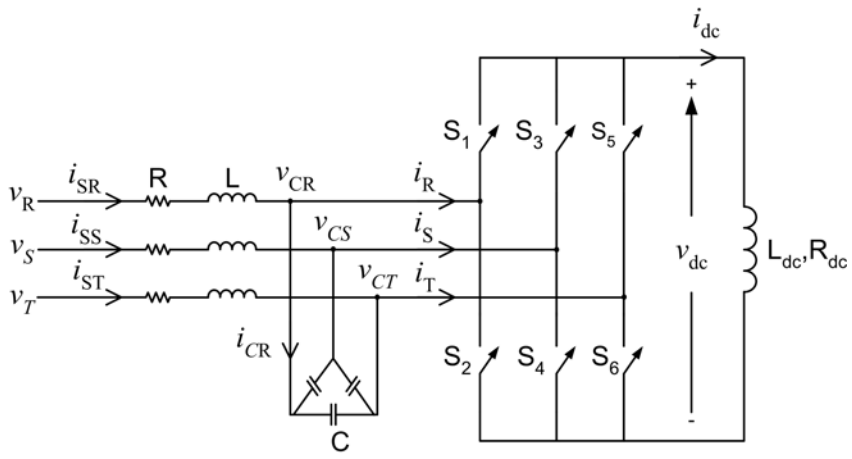


Figure 2.1 General circuit topology of Three Phase Current Source Converter

A dc-link reactor has been placed in dc-link as the energy storage element. The dc-link reactor has an electrical equivalent circuit which is composed of series connection of dc-link inductance L_{dc} and its internal resistance R_{dc}. Due to relatively high time constant of dc-link circuit, dc-link current, i_{dc} becomes nearly constant over a switching period.

Because of the switchings of the power semiconductors in accordance with a pre-specified pattern, the nearly constant dc-link current in the steady state is reflected to the ac lines of the CSC in the form of bidirectional current pulses. The converter line currents (i.e., i_R, i_S, and i_T in Fig.2.1) will therefore have harmonic spectra in addition to the fundamental component at supply frequency. In order to filter out these harmonic components, a three phase low pass input filter is to be used at the AC side of the converter. By this way, nearly sinusoidal supply line currents, (i.e., i_{SR}, i_{SS}, i_{ST}) which comply with the harmonic standards [65] can be obtained. Capacitors in the input filter are inherent to the Current Source Converters in order to provide a low impedance return path to the converter current pulses. Although the use of series reactor in the input filter is optional their use is beneficial for adjusting the corner frequency of the filter and thus lowering effectively the harmonic content of the injected currents to the supply by the STATCOM. Since the filter inductance is composed of leakage inductance of the coupling transformer, cable and bulbar inductances and the inductance of external reactor for medium voltage applications, fine tuning of the corner frequency can only be achieved by the use of an external reactor in each line as shown in Fig.2.1. The series resistance, R in Fig.2.1 takes account of internal resistances of coupling transformer, cables and bus bars and the external filter reactor. In the input filter electrical damping is provided only by R.

2.3 Principles of Reactive Power Control

Since reactive power control is achieved by controlling the reactive power generated by Current Source Converter (CSC), the steady-state input-output

relations in CSC will be defined ignoring the input filter as shown in Fig. 2.2. Following assumptions are made in the derivations:

- power semiconductor switches are lossless
- time constant of the dc-link circuit (L_{dc}/R_{dc}) is high enough for switching period in which the dc-link current is almost level with negligibly small ripple and its value is I_{dc}
- three phase balanced AC supply voltages are purely sinusoidal as in (2.1).

$$\left.\begin{aligned} v_R &= V\cos(\omega t) \\ v_S &= V\cos(\omega t - 2\pi/3) \\ v_T &= V\cos(\omega t - 4\pi/3) \end{aligned}\right\} \tag{2.1}$$

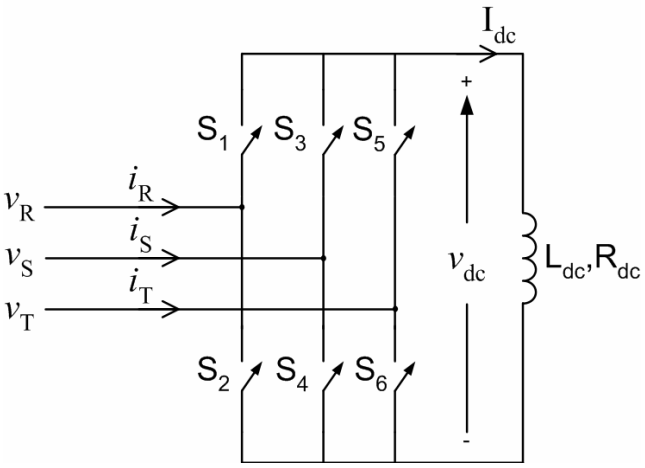


Figure 2.2 Circuit diagram of CSC without input filter

Depending on the modulation technique, which will be discussed in detail later in Chapter 2, fully controllable power semiconductor switches have switching signals, designated as m_{S1}, m_{S2}, m_{S3}, m_{S4}, m_{S5}, m_{S6}. Typical switching signals, m_{S1}, m_{S2} and corresponding converter line current, i_R are shown in Fig.2.3

The switching signals and the corresponding converter line currents are the same in shape in all three lines but they are shifted by $2\pi/3$ and $4\pi/3$ radians with respect to those of line R. Instantaneous values of converter line currents can then be expressed as in (2.2) [20].

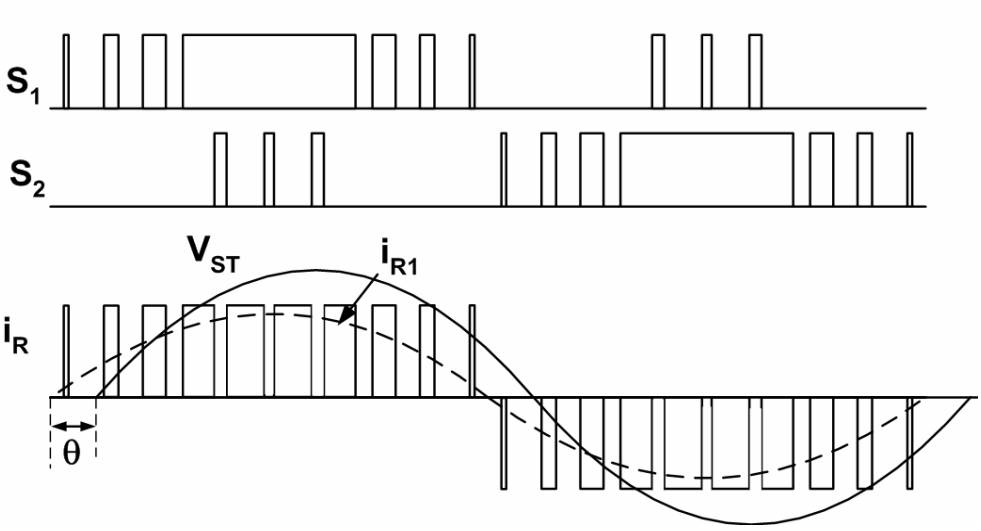


Figure 2.3 Switching signals of S1&S2, and the corresponding theoretical converter input current, i_R(t) and line-to-line voltage, v_{ST}(t) for inductive reactive power generation of CSC

$$\left.\begin{aligned} i_R(t) &= (m_{S1} - m_{S2})I_{dc} \\ i_S(t) &= (m_{S3} - m_{S4})I_{dc} \\ i_T(t) &= (m_{S5} - m_{S6})I_{dc} \end{aligned}\right\} \tag{2.2}$$

The fourier series expansion of converter line currents are as given in (2.3).

$$\left.\begin{aligned} i_R &= I_1 \sin(\omega t + \theta) + \sum_{h=2}^{\infty} I_h \sin(\omega_h t - \lambda_h) \\ i_S &= I_1 \sin(\omega t + \theta - 2\pi/3) + \sum_{h=2}^{\infty} I_h \sin(\omega_h t - \xi_h) \\ i_T &= I_1 \sin(\omega t + \theta - 4\pi/3) + \sum_{h=2}^{\infty} I_h \sin(\omega_h t - \psi_h) \end{aligned}\right\} \tag{2.3}$$

In literature [24,31], modulation index, M is defined as in (2.4).

$$M = \frac{I_1}{I_{dc}} \tag{2.4}$$

Since the CSC produces a dominant harmonic current component at fundamental frequency, harmonic components in (2.4) can be neglected. Under this assumption active and reactive power flows between the supply and the converter will take place only at supply frequency (fundamental component). Fundamental current components at the input of the converter can then be expressed in terms of

modulation index, M and dc-link current, I_{dc} as in (2.5) by using (2.2), (2.3) and (2.4).

$$\left.\begin{aligned} i_{R1} &= MI_{dc}\sin(\omega t+\theta) \\ i_{S1} &= MI_{dc}\sin(\omega t+\theta-2\pi/3) \\ i_{T1} &= MI_{dc}\sin(\omega t+\theta-4\pi/3) \end{aligned}\right\} \qquad (2.5)$$

The phasor diagrams for the quantities given in (2.1) and (2.5) are as shown in Fig. 2.4. It should be noted that converter line currents are either lagging the corresponding supply line voltages by an angle of ($\pi/2$-θ) radians or leading the corresponding line-to-line voltages by an angle of θ rads resulting in inductive reactive power generation of CSC. This is also defined in Fig.2.3. From now on, since line-to-line voltages are terminal quantities and therefore can be measured all the time, converter line currents will be defined with respect to zero crossings of associated line-to-line supply voltages. If CSC is intended to generate capacitive reactive power, switching signals must be shifted by nearly π radians with respect to inductive mode of operation in order to create converter line currents which lead the corresponding to line-to-line voltages by an angle θ as shown in Fig. 2.4b. The switching signals, associated converter input current and line-to-line voltage are as given in Fig.2.5 for capacitive reactive power generation of CSC.

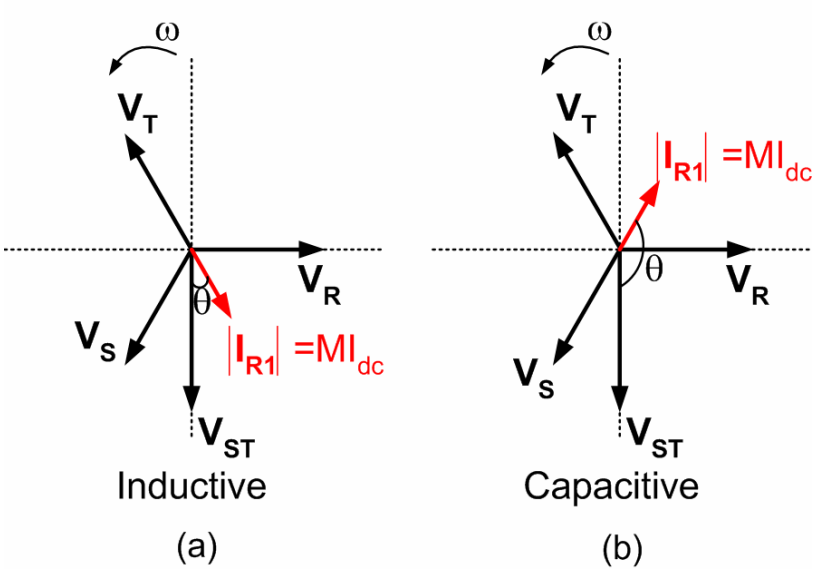


Figure 2.4 Principle phasor diagram of CSC in a steady-state (a) for inductive (b) capacitive reactive power generation

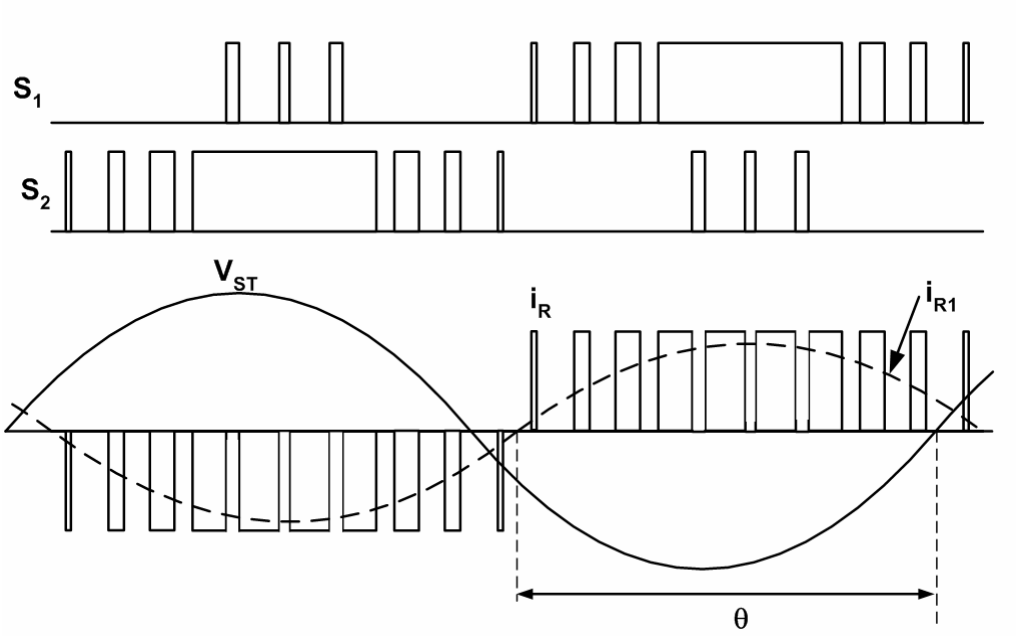


Figure 2.5 Switching signals of S1&S2, and the corresponding theoretical converter input current, i_R(t) and line-to-line voltage, v_{ST}(t) for capacitive reactive power generation of CSC

Using (2.1), (2.5) and Fig.2.4, the steady-state values of active and reactive power at the input terminals of CSC can be expressed as in (2.6) and (2.7).

$$P = \frac{3}{2} VMI_{dc} \sin\theta \tag{2.6}$$

$$Q = \frac{3}{2} VMI_{dc} \cos\theta \tag{2.7}$$

Since the power semiconductor switches have been assumed to be lossless, active power at the input terminals of CSC in (2.6) is equal to power loss in the DC-link reactor owing to its internal resistance, R_{dc}. The power loss in the DC-link is expressed in (2.8). By equating (2.6) to (2.8), steady-state expressions for DC-link voltage, V_{dc} and current, I_{dc} can be found as in (2.9) and (2.10).

$$P = V_{dc} I_{dc} = R_{dc} I_{dc}^2 \tag{2.8}$$

$$V_{dc} = \frac{3}{2} VM \sin\theta \tag{2.9}$$

$$I_{dc} = \frac{3}{2} \frac{VM \sin\theta}{R_{dc}} \tag{2.10}$$

The substitution of (2.10) into (2.6) and (2.7) yields alternative expressions in (2.11) and (2.12) respectively for active and reactive power components. These expressions are valid for θ only in the range of [0,π] because active power in (2.6) becomes negative beyond this range the meaning of which is that the CSC can not deliver active power in the steady-state.

$$P = \frac{9}{4}\frac{V^2 M^2}{R_{dc}}\sin^2\theta \tag{2.11}$$

$$Q = \frac{9}{8}\frac{V^2 M^2}{R_{dc}}\sin 2\theta \tag{2.12}$$

where $0 \le \theta \le \pi$

Using (2.11) and (2.12), the variations in active and reactive power against phase angle, θ are as given in Fig.2.6. It is worth noting the reactive power is increased in θ range from 0 to π/4, active power increases too. The same observation can be made for θ control range from 3π/4 to π. These operating ranges are marked by shaded areas in Fig.2.6. However, in the θ control range from π/4 to 3π/4, active power flowing from ac supply to the dc-link becomes dominant power component and hence CSC can act as an active power flow controller. It is also observed from Fig.2.6 that maximum value of active power is two times bigger than that of reactive power. These occur at different angles of π/4 and π/2 respectively. These features of CSC allow the controlled flow of both active and reactive power between two independent networks not necessarily operating at the same frequency. This can be achieved by connecting on independent network to the other through back-to-back connected CSC circuits. However, for the operation of CSC in STATCOM mode, the main power component which should be controlled is the reactive power. Active power flow much lower than reactive power is needed in the steady-state only for maintaining dc-link active by compensating power losses of STATCOM. However, in transient state much higher values of active power should be delivered to or extracted dc-link in order to be able to change the stored energy content of dc-link reactor in a short time.

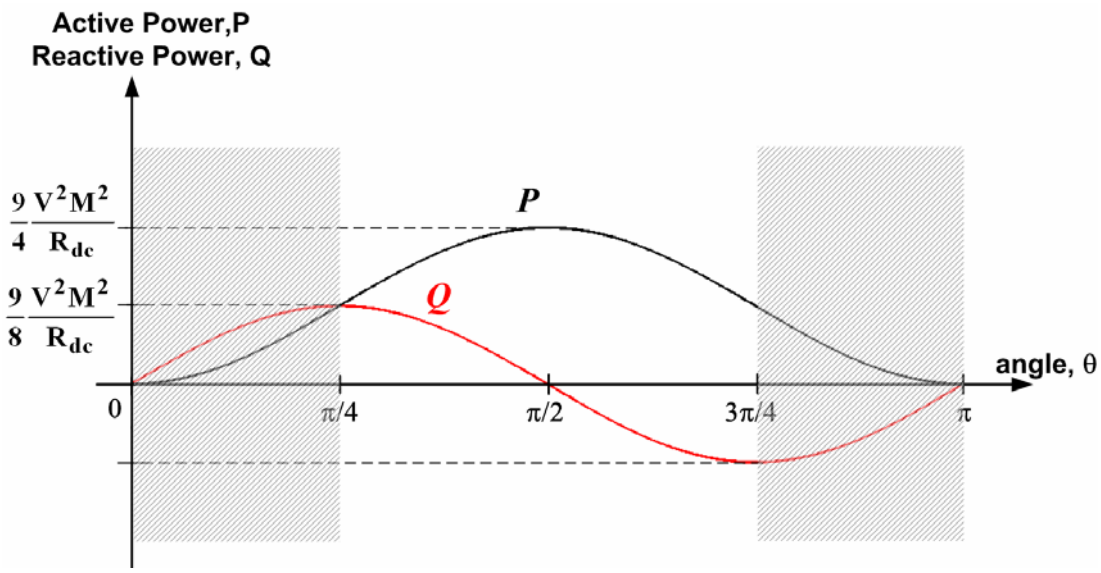


Figure 2.6 Theoretical active and reactive power variations of CSC STATCOM w.r.t. angle, θ at a fixed modulation index

In view of these discussions the values of θ will be very close to 0 in the inductive region and to π in the capacitive region for STATCOM operation in the steady-state. Since for small values of θ (θ<10°) sinθ ≅ θ and cos(π-θ) ≅ 1 then active and reactive power expressions in (2.6) and (2.7) can be approximated to (2.13) and (2.14).

$$P = \frac{3}{2} VMI_{dc}\,\phi \qquad \text{where } \phi = \begin{cases} \theta & \text{for inductive region} \\ \pi - \theta & \text{for capacitive region} \end{cases} \tag{2.13}$$

$$Q = \begin{cases} \dfrac{3}{2} VMI_{dc} & \text{for inductive region} \\ -\dfrac{3}{2} VMI_{dc} & \text{for capacitive region} \end{cases} \tag{2.14}$$

On the other hand ϕ=3° yields rated value of reactive power produced by the prototype STATCOM as will be described in Chapter 3. This fact strengthens the validity of the approximations given above.

It can therefore be concluded from (2.14) that reactive power generated by CSC can be controlled by varying either i) modulation index, M, ii) dc-link current, I_{dc}, or iii) both. For a fixed PWM pattern, modulation index can be varied by changing pulse widths of all pulses by the same factor. The magnitude of dc-link current can only be changed by delivering active power to or extracting from the dc-link. This can be achieved by varying phase shift angle ϕ in (2.13). This is also apparent from (2.15), which is obtained by equating (2.13) to (2.8).

$$I_{dc} = \frac{3}{2}\frac{VM}{R_{dc}}\phi \qquad \text{where } \phi = \begin{cases} \theta & \text{for inductive region} \\ \pi - \theta & \text{for capacitive region} \end{cases} \tag{2.15}$$

An important observation is that the reactive power does not depend on inductance of the magnetic energy storage element because the objective of the use of an energy storage element in the dc-link is to provide a constant level dc-link quantity (i.e., dc-link current in CSC or dc-link-voltage in VSC) without any active power consumption. That is the reason why STATCOM is known as "Static VAr Compensator with minimum energy storage element".

For a lossless CSC (i.e., all power semiconductors are ideal and R_{dc}=0), there won't be any active power flow to CSC in steady-state. This can be done making phase shift angle ϕ in (2.13) equal to zero. This makes equation (2.15) undefined since R_{dc} and ϕ are both equal to zero. In this situation, the magnitude of dc-link current can only be controlled by varying ϕ in transient-state in order to provide a power flow from/to CSC. This charges/discharges the dc-link reactor (i.e., energy storage element) to a defined value of dc-link current, as shown in Fig.2.7. The current phasors in quadrants II and III, correspond to discharging and those in I and IV to charging the dc link reactor. Since the system is totally lossless the dc-link current stays constant at this value forever. Then, the required reactive power can be adjusted by the control of modulation index, as illustrated in Fig.2.8.

For the CSC STATCOM developed within the scope of this study, the control range of phase shift angle (ϕ) is in the range from -15° to 15° in the transient state. However, operating value of phase shift angle is in the range from 0° to 3° in the steady state.

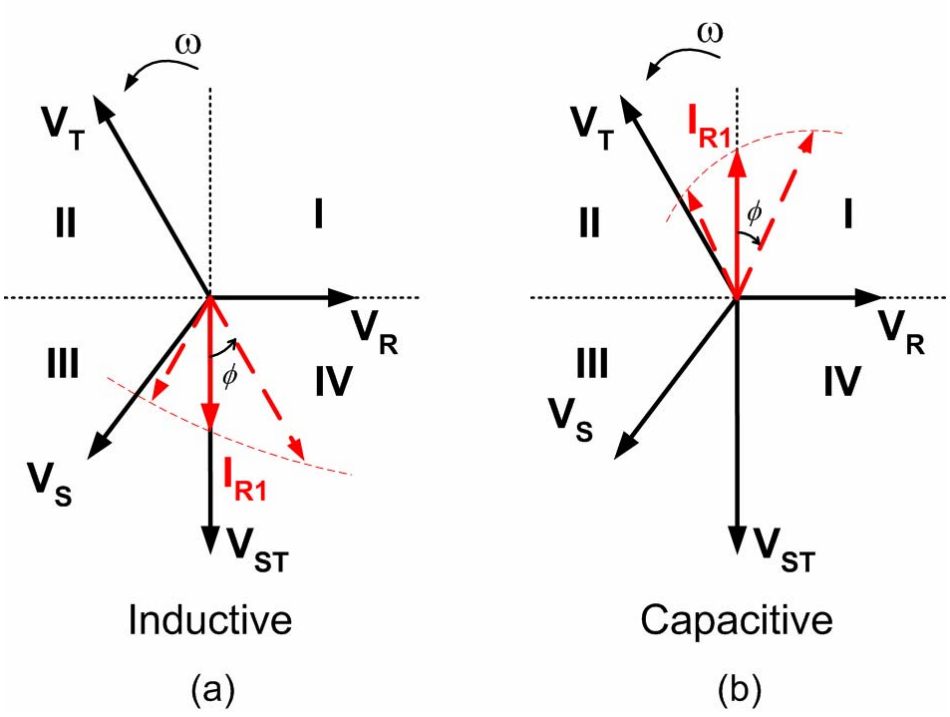


Figure 2.7 Phasor diagram of CSC in a lossless system (transient-state representation) (a) for inductive (b) capacitive reactive power generation

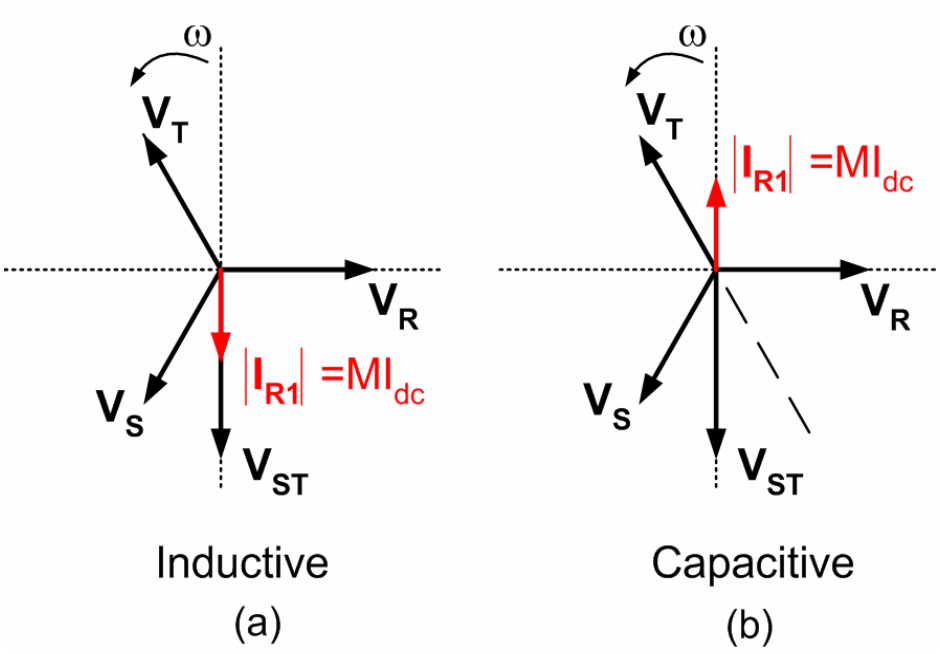


Figure 2.8 Phasor diagram of CSC in a lossless system (steady-state representation) (b) for inductive (b) capacitive reactive power generation

Simultaneous control of modulation index, M and phase shift angle result in a faster response for reactive power generation of CSC as shown in [59-60]. However, in some applications, control of modulation index is inapplicable, as to be discussed in Section 2.3. In such cases, the reactive power control can only be achieved by the control of dc-link current via phase shift angle (ϕ). This will be achieved by charging or discharging energy storage element (i.e., dc-link reactor). Due to the large time constant of dc-link reactor, dc-link current can not be changed instantaneously. It can therefore be concluded that the control of ϕ only yields a relatively slow response in comparison with simultaneous control of M and ϕ. A quantitative comparison on the bases of simulations and laboratory experiments is given in [59].

So far, the principles of reactive power generation by CSC have been described by Fig.2.2, in which the input filter has been ignored. However, in a practical system, input filter becomes an indispensable part of CSC in order to filter out the converter line current harmonics shown in Fig.2.3 and Fig.2.5. The input filter has some effects on the behaviour of CSC such as the voltage regulation just at the input terminals of CSC. Fig.2.9 shows the single diagram of CSC based STATCOM where supply voltage V_R is assumed to be constant. Phasor diagrams for CSC based STATCOM can be obtained from Fig.2.9 and sketched in Fig.2.10 for both inductive and capacitive mode of operation. The input voltage V_{CR} of the CSC is lower than V_R for inductive mode of operation as expected while higher values than V_R are obtained for capacitive mode. The variation in V_{CR} from full inductive load to full capacitive load depends only on the value of filter inductances. The matters related to CSC based STATCOM will be discussed in detail in Chapter 3 under the title of "input filter design".

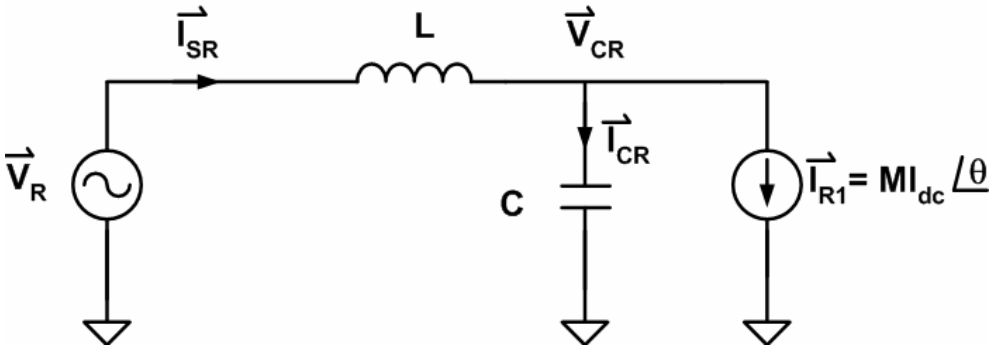


Figure 2.9 Equivalent single line diagram of CSC based STATCOM

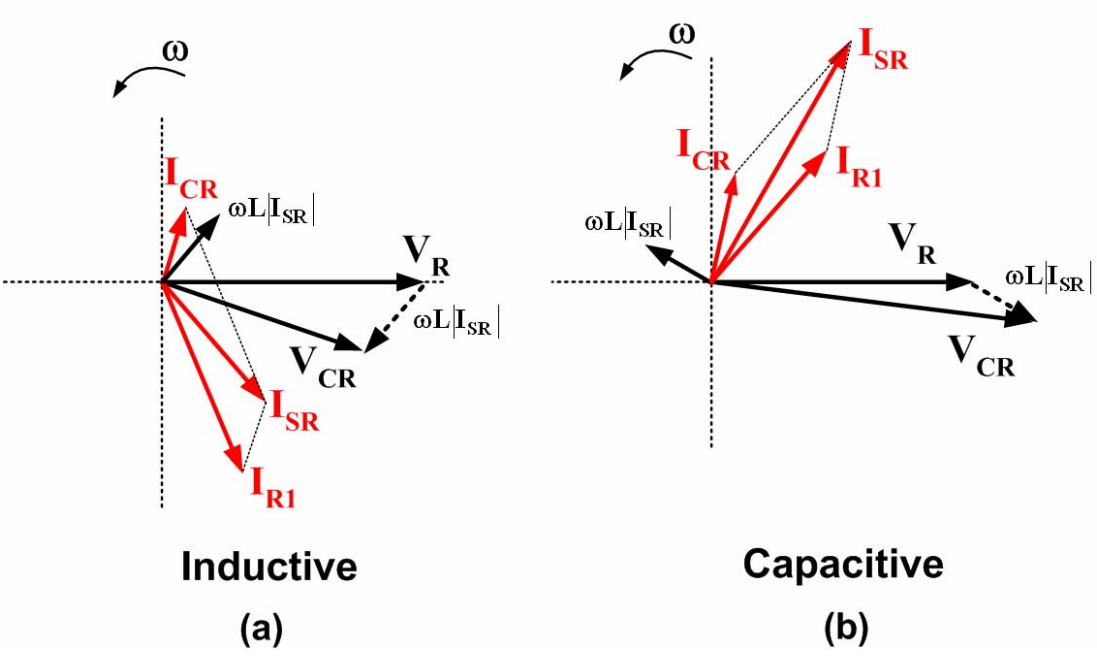


Figure 2.10 Illustration of variations in converter input voltage, V_{CR} with the generated reactive power of CSC

2.4 Pulse Width Modulation Techniques

The developments in fully controllable power semiconductors and high speed digital processors have made various pulse width modulation (PWM) techniques applicable to power converters [53]. PWM techniques present i)cost effective, efficient and more compact systems, ii) nearly sinusoidal input/output waveforms, iii) superior control characteristics [24].

In the application of PWM techniques to CSC given in Fig.2.1, the constraint in (2.16) must be guaranteed [12,20,53,64]. This constraint implies that there is always at least one switch from the upper half bridge (S1, S3, S5) and at least one switch from the lower half bridge (S2, S4, S6) should be in conduction in order to provide a circulating path for the dc-link current through the supply or the converter.

$$\begin{aligned} m_{S_1} + m_{S_3} + m_{S_5} &= 1 \\ m_{S_2} + m_{S_4} + m_{S_6} &= 1 \end{aligned} \tag{2.16}$$

Different PWM techniques have been studied for CSC [11-15,16,19,24,25,27,33,42,45,50]. Among these studies, following PWM techniques are mainly used: i) Modified Sinusoidal PWM (MSPWM) [12, 53], ii) Space Vector PWM (SVPWM) [4,17,19,25], and iii) Selective Harmonic Elimination Method (SHEM) [12,13,24,50].

Typical switching patterns and the corresponding converter line currents, defined in (2.2) are given in Fig.2.11, Fig. 2.12 and Fig 2.13 for different modulation techniques. These switching patterns, yield harmonic spectra of converter line currents as given in Fig. 2.14. Since the peak value of the pulses in converter line current waveforms is theoretically dc-link current (I_{dc}) the harmonic spectra in Fig. 2.14 are given as normalized form with respect to I_{dc}.

These modulation techniques are compared in Table 2.1. MSPWM is a modified version of the classical SPWM for CSC. It produces lower low order harmonics (such as 5^{th}, 7^{th}, 11^{th}, 13^{th}) in magnitude as the converter semiconductors are switched on and off at relatively higher frequencies than 2kHz in comparison with SVPWM. However, SVPWM is being the most common been widely used

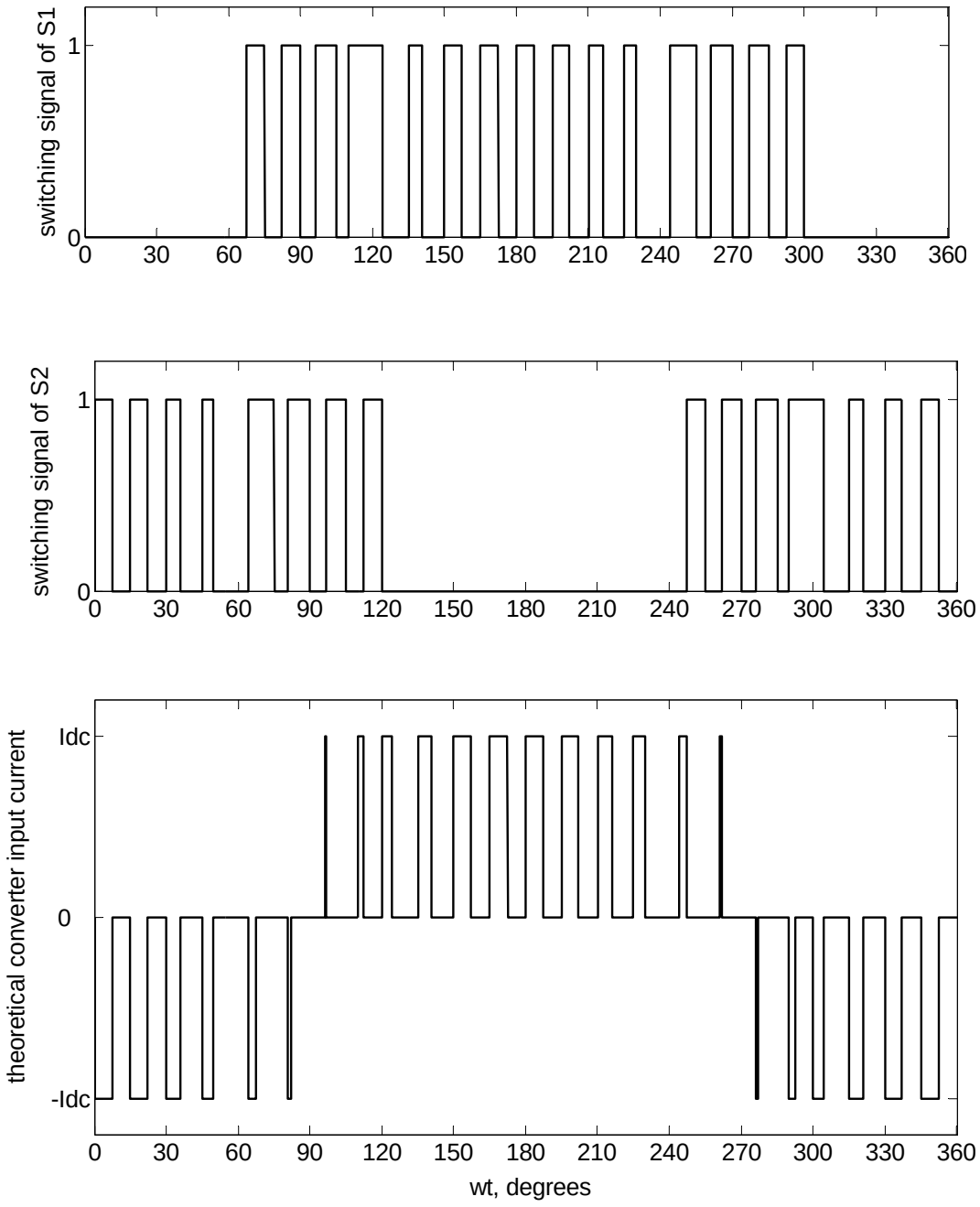


Figure 2.11 Typical switching patterns for MSPWM (M= 0.5, $f_{carrier}$= 1200Hz)

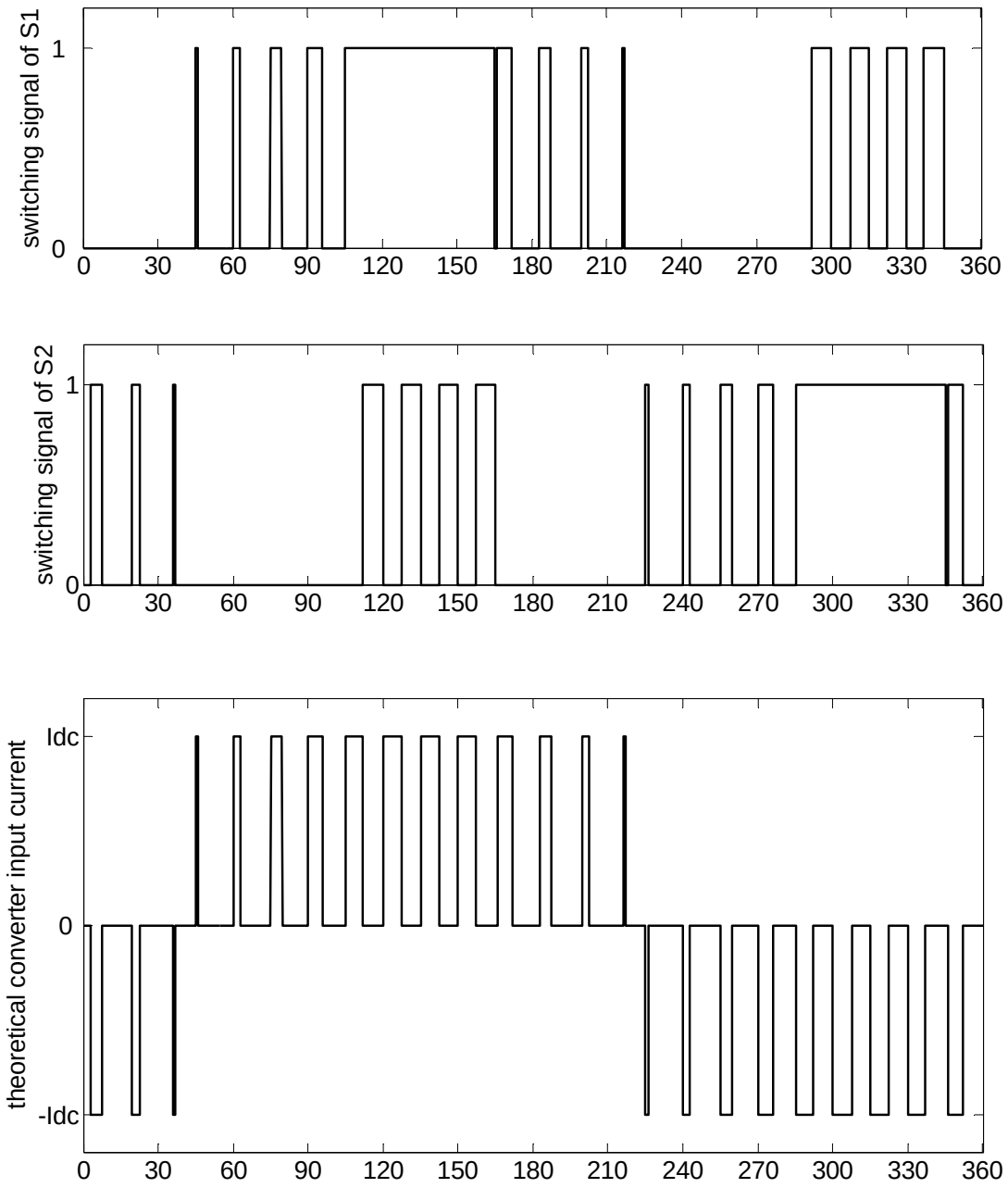


Figure 2.12 Typical switching patterns for SVPWM (M= 0.5, $f_{carrier}$= 1200Hz)

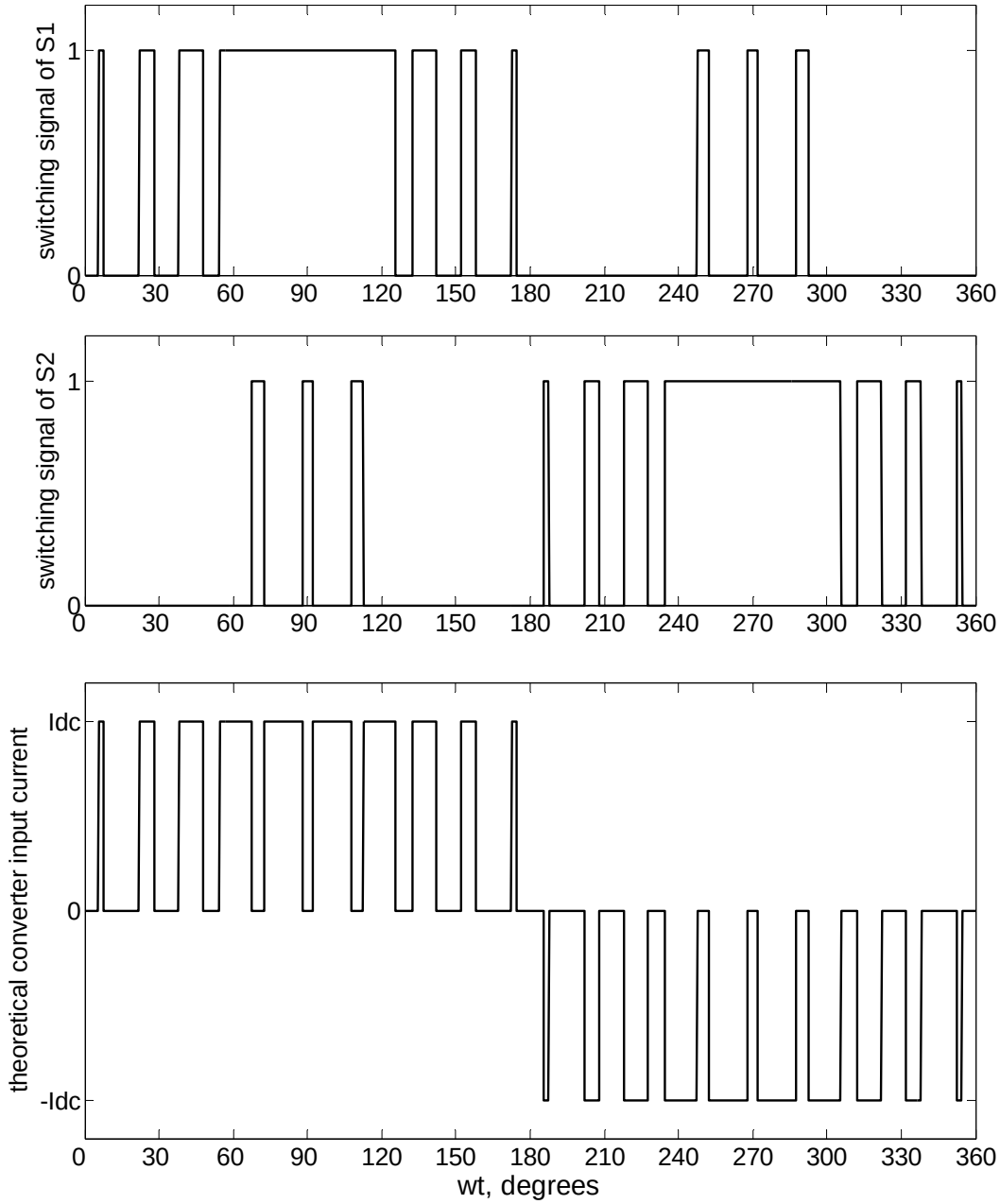
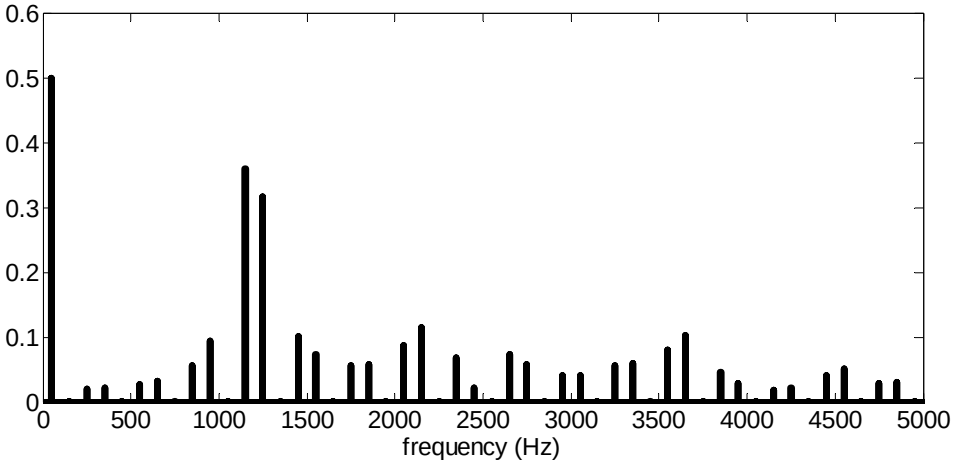
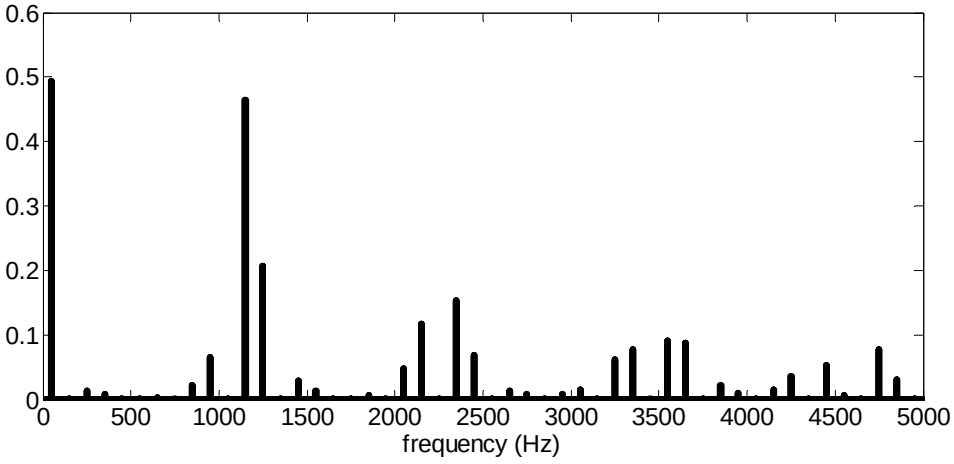


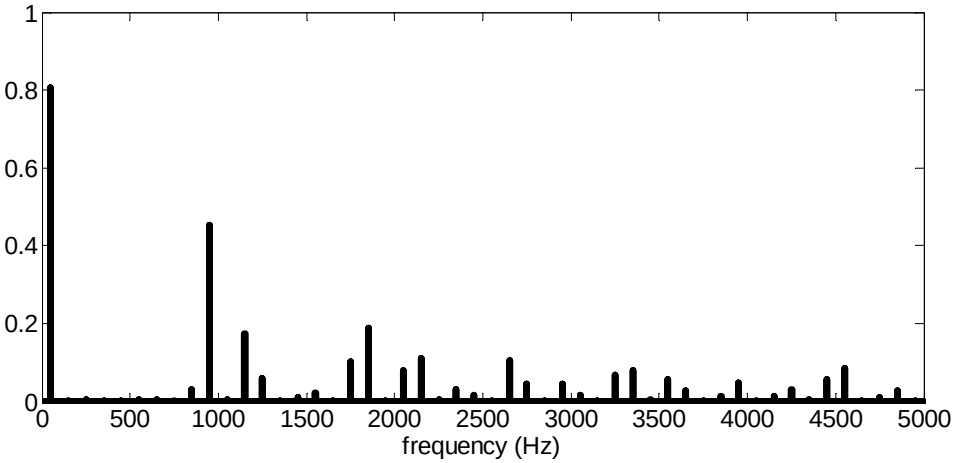
Figure 2.13 Typical switching patterns for SHEM
(elimination of 5th, 7th, 11th and 13th harmonics at M=0.8)



(a)



(b)



(c)

Figure 2.14 Normalized harmonic spectra of converter input current w.r.t. dc-link current (a) for MSPWM (b) for SVPWM (c) for SHEM

modulation technique due to its lower switching frequency for the same carrier frequency. The control range of modulation index for both MSPWM and SVPWM is the same. Therefore, MSPWM is suitable for low voltage medium power applications [53]. Although MSPWM and SVPWM offer continuous control of modulation index and phase shift angle simultaneously, resulting in faster dynamic response, SHEM has the harmonic spectra of converter line current superior to those of MSPWM and SVPWM, which usually contain low order harmonics, such as fifth and seventh at low switching frequencies. These low order harmonics may excite parallel resonance of the input filter in CSC [55]. This can be avoided with the use of passive damping [53] or active damping [42, 55]. Passive damping requires addition of an external damping resistor to input filter resulting in excessive power dissipation. On the other hand, active damping requires complicated control algorithm and can not provide continuous damping in the entire operating range [55].

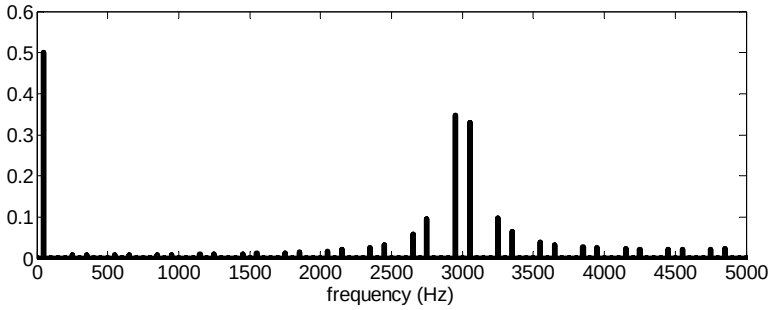
Table 2.1 Comparison of modulation techniques applicable to CSC

f_S – switching frequency K – number of harmonics to be eliminated
$f_{carrier}$ – carrier frequency f_1 – fundamental frequency

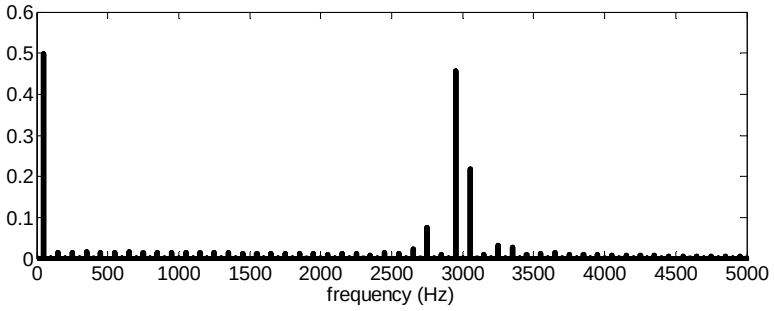
	Harmonic Spectra	**Modulation Index**	**Applications**
MSPWM	– smaller low order harmonics for $f_S > 2$ kHz – $f_S=(2/3)f_{carrier}$	– controllable – $0 \leq M \leq 1.0$	medium power IGBT or MOSFET based converters, where $f_S > 2$kHz
SVPWM	– smaller low order harmonics for $f_S < 2$ kHz – $f_S=(1/2)f_{carrier}$	– controllable – $0 \leq M \leq 1.0$	medium power IGBT or MOSFET based converters, where $f_S > 2$kHz
SHEM	– negligible low order harmonics – $f_s = \begin{cases} (2K+2)f_1 & \text{if } \frac{K}{2} \text{ is even} \\ (2K+3)f_1 & \text{if } \frac{K}{2} \text{ is odd} \end{cases}$	can only be controlled in discrete steps	Medium or high power IGBT or IGCT based converters where $f_S < 1$kHz

All modulation techniques used in CSC applications yield the same utilization factor for power semiconductors. The average value of the current through each power semiconductor is found to be one third of the dc-link current for all values of modulation index.

SHEM technique is based on pre-calculated switching patterns (i.e., off-line generated pattern) while MSPWM and SVPWM are based on on-line generated patterns [55]. Therefore, patterns of SHEM for each modulation index are to be calculated in such a way that the magnitudes of low order harmonics should be zero as shown in Fig.2.14c. Although the transient response of CSC STATCOM is slower in SHEM, it has been widely used in high power applications, for which switching frequency should be kept at low values, e.g., below 1kHz [31,36,55,64]. In the applications where the switching frequencies above 2kHz is permissible, the use of on-line generated PWM techniques become more feasible, as illustrated in Fig.2.15.



(a)



(b)

Figure 2.15 Normalized harmonic spectra of converter input current w.r.t. dc-link current (a) for MSPWM (b) for SVPWM when carrier frequency, $f_{carrier}$= 3kHz

Therefore, the most proper modulation technique is to be chosen according to the needs of the application. Within the scope of this thesis, SHEM has been chosen as the modulation technique for the implementation of IGCT based CSC STATCOM, which the switching frequency is set to 500Hz due to restrictions in the cooling system of the power semiconductors.

2.4.1 Selective Harmonic Elimination Method

Selective harmonic elimination method provides not only elimination of selected harmonics at moderate switching frequencies but also control of magnitude of the fundamental component in converter line currents. Since the harmonics, at any order, deteriorates the quality of power, they should be filtered out. As the order of harmonics to be filtered out increases, the use of smaller size and hence cheaper filters becomes allowable. Therefore, it is common to apply SHEM for elimination of low order harmonics in the converter line currents. The main problem in selective harmonic elimination techniques is that when the numbers of harmonics to be eliminated increases such techniques fail to provide an adequate solution [11,13]. Among the studies on SHEM for CSC [11,13,24,50], [24] presents a generalized technique for generating switching patterns of three phase CSC in order to eliminate only even number of low order selected harmonics in the converter line currents. Although [50] proposes an alternative approach, which enables elimination of both odd and even number of selected harmonics, the switching frequency of power semiconductors is higher than that proposed approach given in [24] for the same even number of harmonics to be eliminated. Therefore, the generalized technique for SHEM in [24] will be used in this thesis.

The relationship between the switching frequency and the number of harmonics to be eliminated in [24] is as given in (2.17).

$$f_s = \begin{cases} (2K+2)f_1 & if \ \dfrac{K}{2} \ is \ even \\ (2K+3)f_1 & if \ \dfrac{K}{2} \ is \ odd \end{cases} \tag{2.17}$$

where, f_s is the switching frequency, f_1 is the supply frequency and hence fundamental frequency, and K is the even number of harmonics to be eliminated.

Depending on the harmonics to be eliminated from the converter line currents, pulses in the switching patterns of the power semiconductor switches should be positioned properly within [0,π/3] interval as given in [24]. For this purpose, independent chopping angles are defined within [0, π/6] interval. Typical switching patterns with the independent chopping angles are given in Fig. 2.16 for 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic elimination. As it can be understood from Fig.2.16, the position of the switching patterns is defined in terms of these chopping angles, therefore they are called as "independent chopping angles". The number of independent chopping angles, E is defined as

$$E = K + 1 \tag{2.18}$$

Then, five chopping angles in Fig. 2.16 are defined in order to eliminate 5^{th}, 7^{th} , 11^{th} , and 13^{th} harmonic components of converter input current. Since the converter input current waveform is to be odd quarter wave [86], switching patterns for S1 and S2 are defined for [0,π/2] interval in Fig. 2.17. Complete switching pattern of S1 and S2, and corresponding converter input current are shown in Fig.2.3. The switching patterns of the remaining power semiconductors (S3, S4, S5, S6) and the corresponding converter input line current waveforms (i_S, i_T) are to be shifted with respect to first leg , respectively by 2π/3 and 4π/3 radians. The switching patterns of all power semiconductors are given in Fig.2.17 in conjunction with Fig.2.18, in which conduction paths are numbered and these numbers are marked under the waveforms in Fig.2.17 at appropriate places. From Fig.2.17 and Fig.2.18, it is clear that generated switching patterns validate the basic constraint in (2.16) for CSC. It should be noted that switching patterns described for [0,π/3] interval in Fig.2.16 are applied to all power semiconductor switches over a full cycle, i.e., from 0 to 2π.

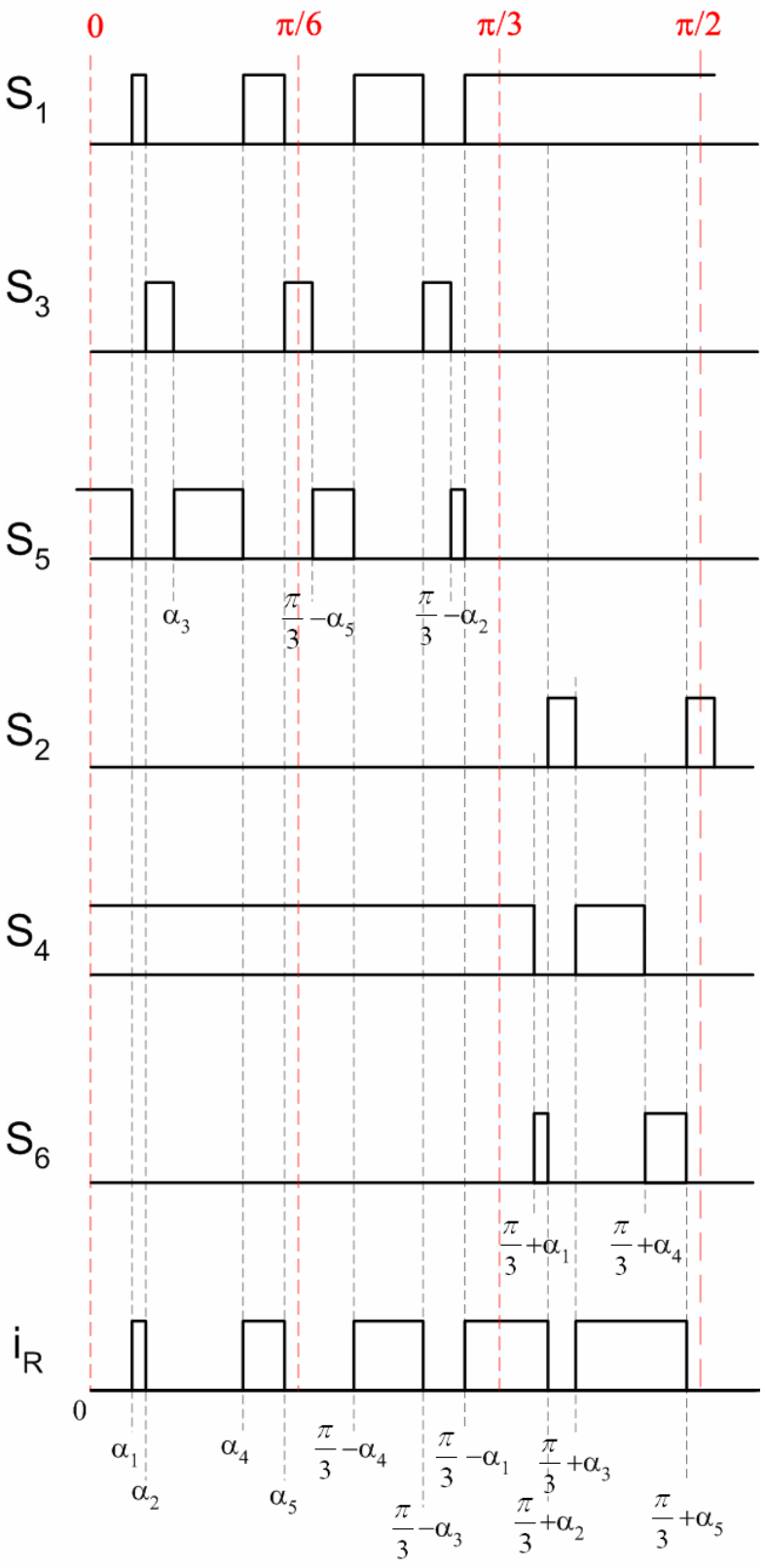


Figure 2.16 Definition of five independent chopping angles for 5th, 7th ,11th and 13th harmonic elimination

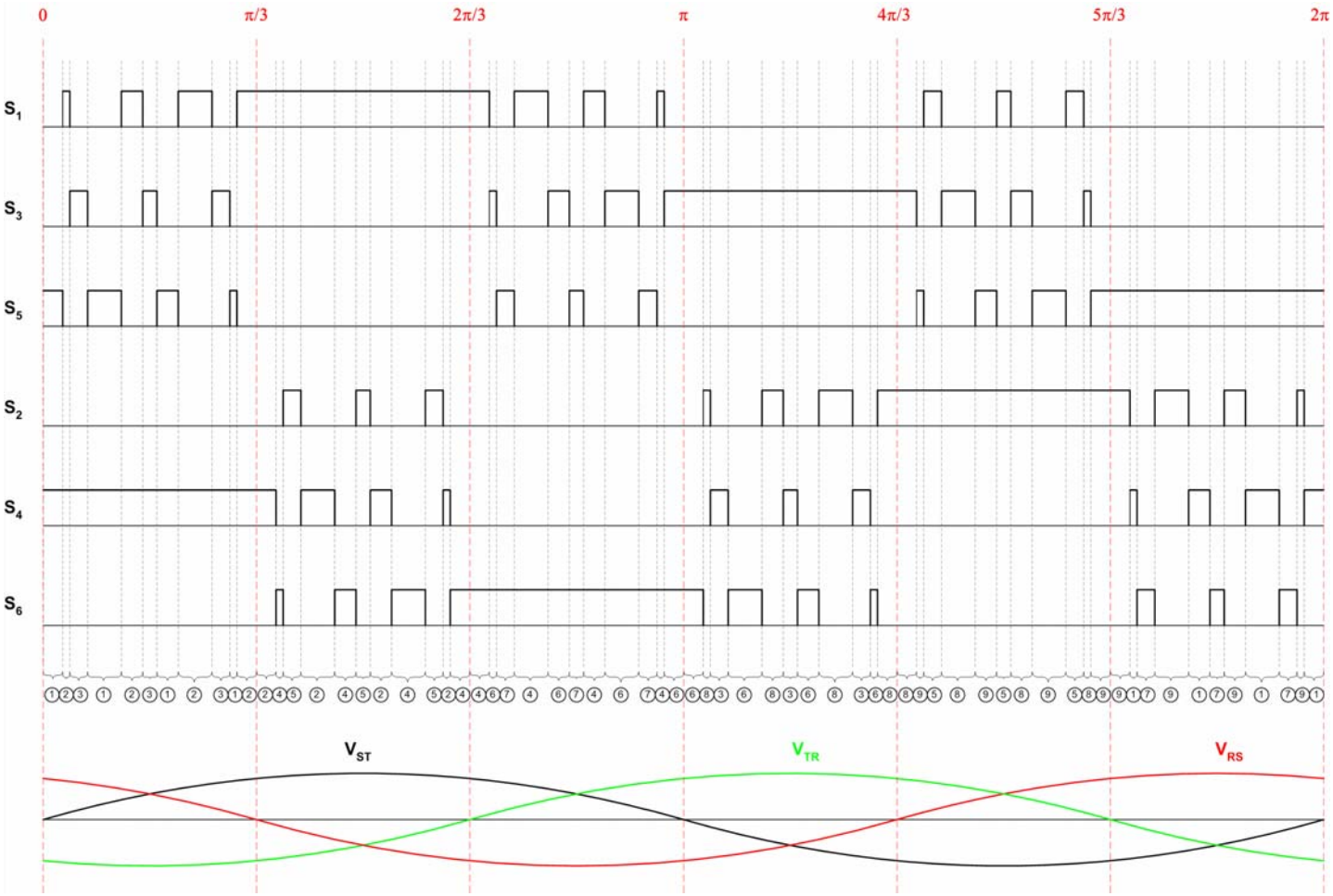


Figure 2.17 The switching patterns of all power semiconductor switches w.r.t. line to line voltages are defined for inductive reactive power generation of CSC STATCOM

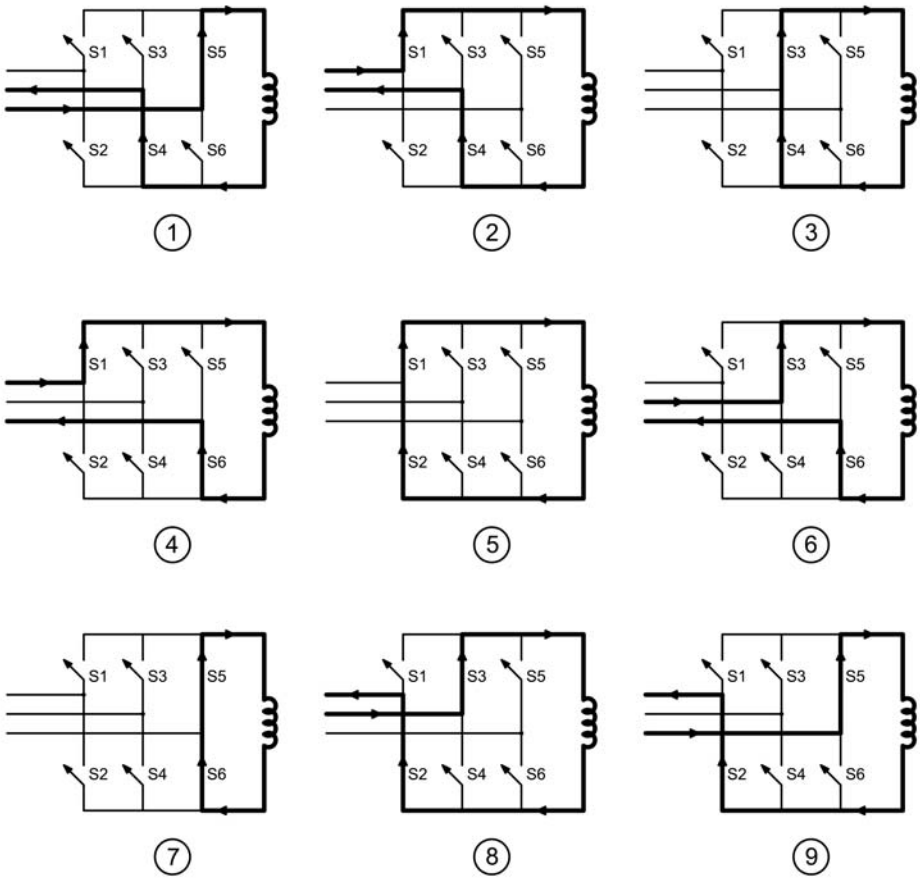


Figure 2.18 Conduction states of power semiconductor switches in CSC are labeled w.r.t. Fig.2.17

Since the converter input current waveform i_R in Fig.2.16 is an odd quarter wave, only the coefficients of sinusoidal terms (b_n) are to be evaluated over the quarter of a period and they are given in (2.19).

$$b_n = \frac{4I_{dc}}{n\pi}\left[\begin{array}{l} cos(n\alpha_1) - cos(n\alpha_2) + cos(n\alpha_4) - cos(n\alpha_5) \\ + cos\left(n(\frac{\pi}{3} - \alpha_4)\right) - cos\left(n(\frac{\pi}{3} - \alpha_3)\right) + cos\left(n(\frac{\pi}{3} - \alpha_1)\right) \\ - cos\left(n(\frac{\pi}{3} + \alpha_2)\right) + cos\left(n(\frac{\pi}{3} + \alpha_3)\right) - cos\left(n(\frac{\pi}{3} + \alpha_5)\right) \end{array}\right] \qquad (2.19)$$

The five independent angles (α_1, α_2... α_5) can be determined from (2.19) by equating b_5, b_7, b_{11} and b_{13} to zero, in turn. One more equation is needed in determining these five independent angles. The fifth equation relates peak value of

the fundamental current (b_1) to dc-link current (I_{dc}) in terms of modulation index, M as in (2.4).

In order to find five independent chopping angles by equating (2.19) to zero for n=5, 7, 11, 13 and (2.4) to the desired modulation index, M a proper optimization algorithm should be employed. In other words five nonlinear algebraic equations in five unknown are to be solved. Since the exact solution can not be reached for nonlinear equations, constrained nonlinear optimization methods should be used such as optimization tool of MATLAB. This employs constraints on the harmonic components to be eliminated in such a way that they are made as small as possible (i.e., less than 1%) while the cost function defined in (2.20) is being minimized in order to make the fundamental component as close as possible to the desired modulation index, M. This optimization problem is defined in (2.20) together with its constraint.

$$\text{Cost Function:} \quad \min_{\{\alpha_1,\alpha_2,\alpha_3,\alpha_4,\alpha_5\}} \left| b_1 - M \right| \tag{2.20}$$

with the linear inequality constraints:

$$-\alpha_1 \le -\frac{\pi}{720};\quad \alpha_2-\alpha_1 \le \frac{\pi}{720};\quad \alpha_3-\alpha_2 \le \frac{\pi}{720};\quad \alpha_4-\alpha_3 \le \frac{\pi}{720};\quad \alpha_5-\alpha_4 \le \frac{\pi}{720};\ \alpha_6 \le \frac{\pi}{6}$$

and with nonlinear inequality constraints:

$$\begin{aligned}
&\left|b_5(\alpha_1,\alpha_2,\alpha_3,\alpha_4,\alpha_5)\right| - 0.002 \le 0;\\
&\left|b_7(\alpha_1,\alpha_2,\alpha_3,\alpha_4,\alpha_5)\right| - 0.002 \le 0;\\
&\left|b_{11}(\alpha_1,\alpha_2,\alpha_3,\alpha_4,\alpha_5)\right| - 0.002 \le 0;\\
&\left|b_{13}(\alpha_1,\alpha_2,\alpha_3,\alpha_4,\alpha_5)\right| - 0.002 \le 0
\end{aligned}$$

Having defined the optimization problem, these five independent angles can be found by using “fmincon” solver in optimization toolbox of MATLAB. These independent angles are given in Fig. 2.19 for different modulation index values. In the application of SHEM technique, continuous control of modulation index may be achieved by storing switching patterns generated with these independent chopping angles at infinitely many value of modulation index in the range of [0,1] at the expense of very large digital memory storage device. Since this is not practical, control of modulation index can be done in discrete steps [55].

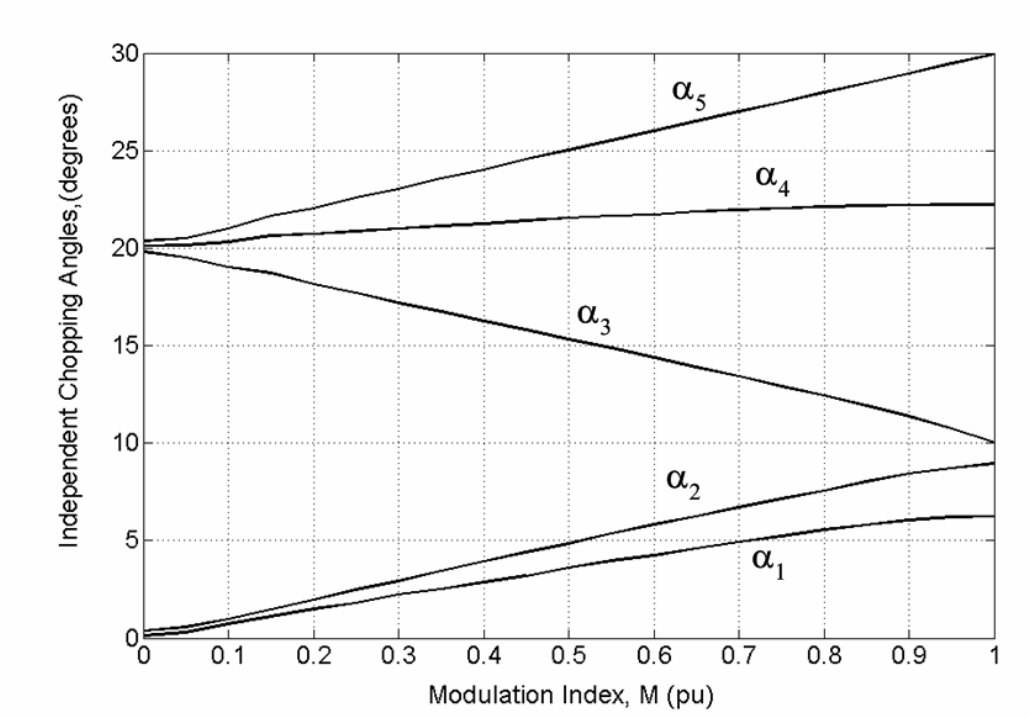


Figure 2.19 The variation independent chopping angles in degrees for the elimination of 5^{th}, 7^{th}, 11^{th}, 13^{th} harmonics in converter input current w.r.t. modulation index

The harmonic spectrum of the resultant converter line current for 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic elimination for a modulation index value of 0.8 has already been given in Fig.2.14c. As seen from Fig.2.17, the switching frequency is 500Hz as implied by (2.17).

It may be useful to repeat the analysis above for K=6 in order to illustrate the benefits of eliminating higher of number harmonics on TDD of converter line currents. Using the generalized technique in [24], the generation of switching patterns of power semiconductor switches for 5th, 7th, 11th, 13th, 17th, and 19th harmonic elimination can be determined as shown in Fig.2.20. The resultant switching patterns of all power semiconductors are given in Fig.2.21. The converter line current, shown in Fig.2.20 will have the harmonic spectrum as given in Fig.2.22. And, the variation of independent chopping angles with respect to modulation index is as shown in Fig.2.23.

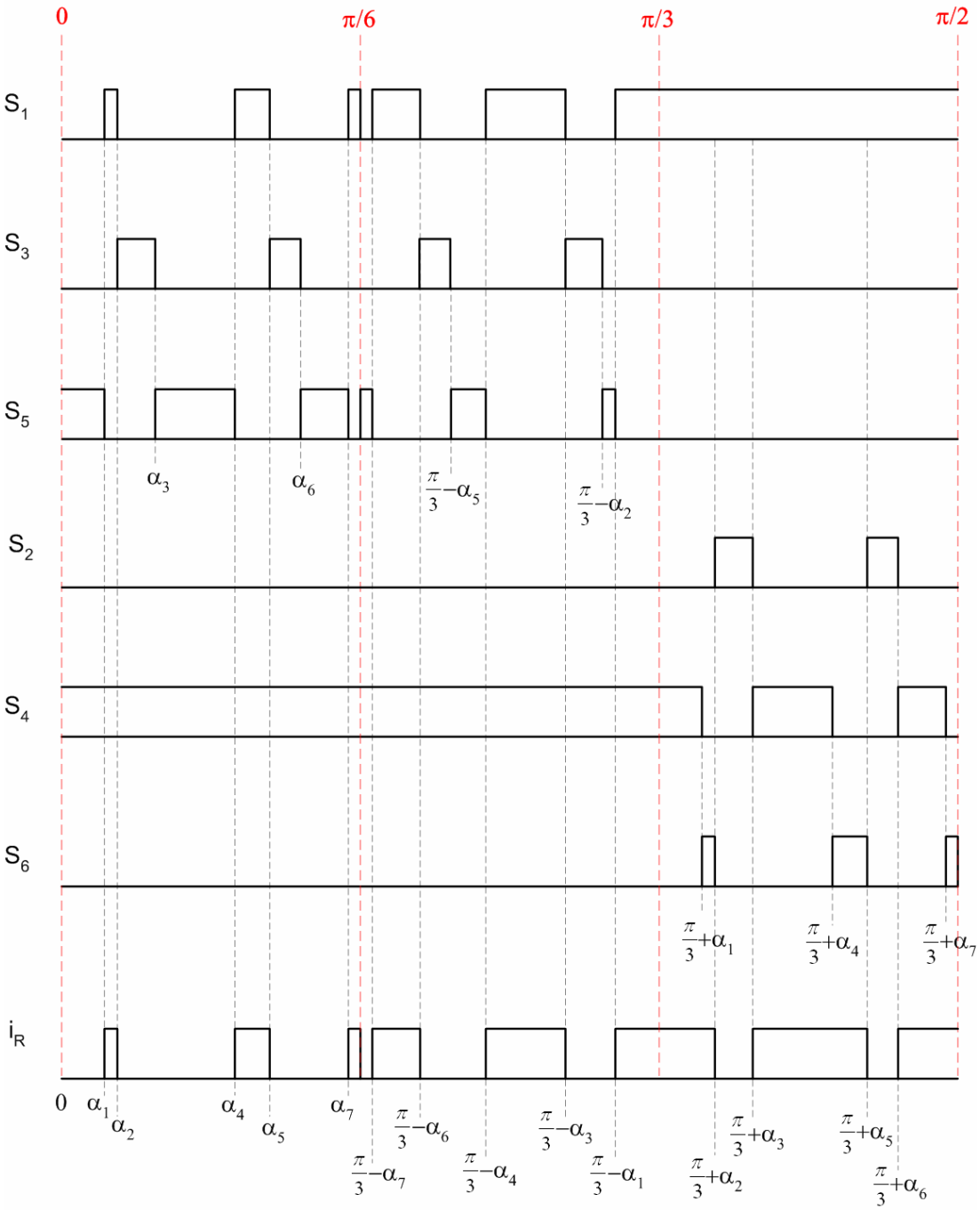


Figure 2.20 Definition of seven independent chopping angles for 5th, 7th ,11th, 13th, 17th and 19th harmonic elimination

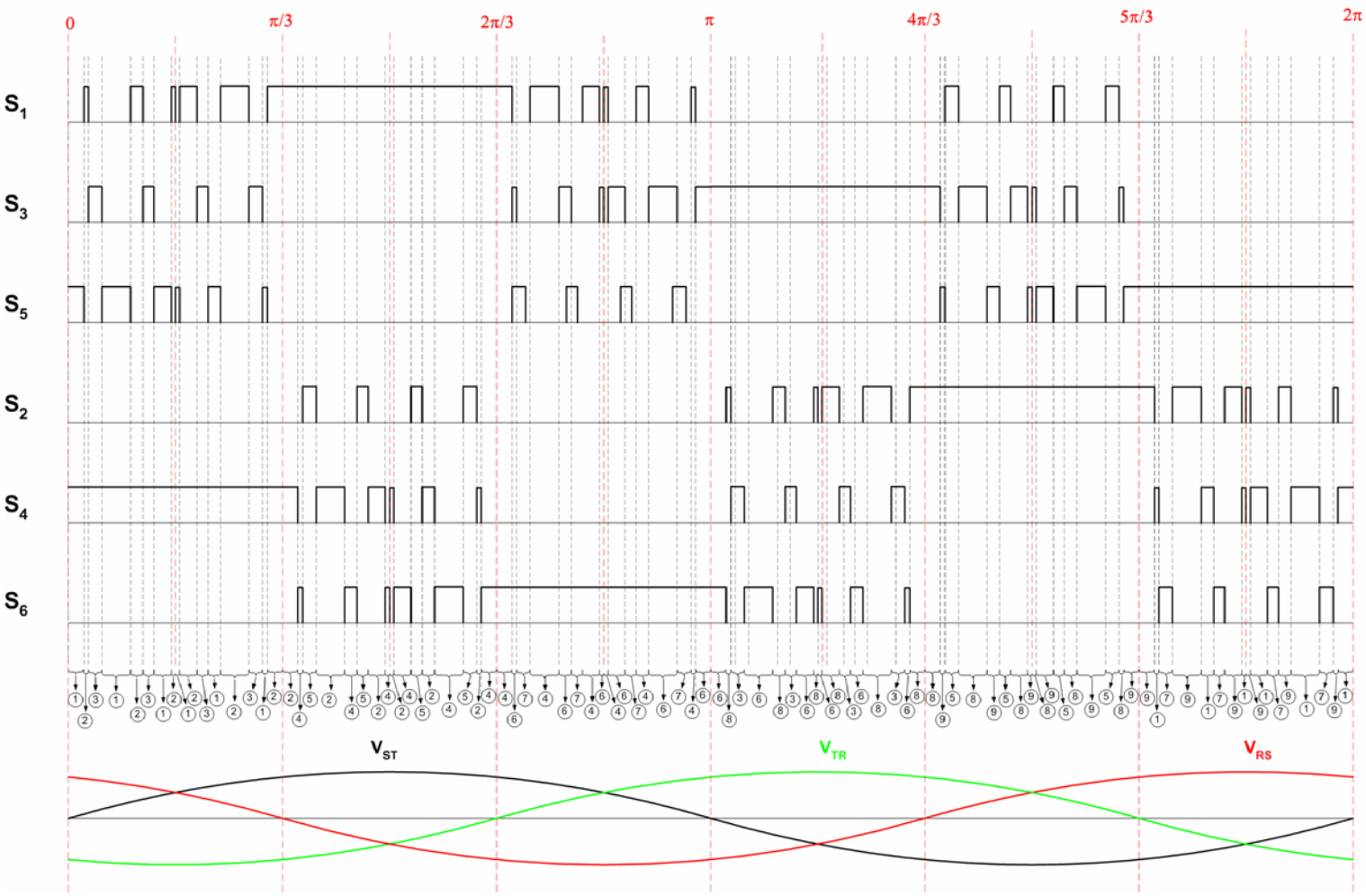


Figure 2.21 The switching patterns of all power semiconductor switches w.r.t. line to line voltages are defined for inductive reactive power generation of CSC STATCOM

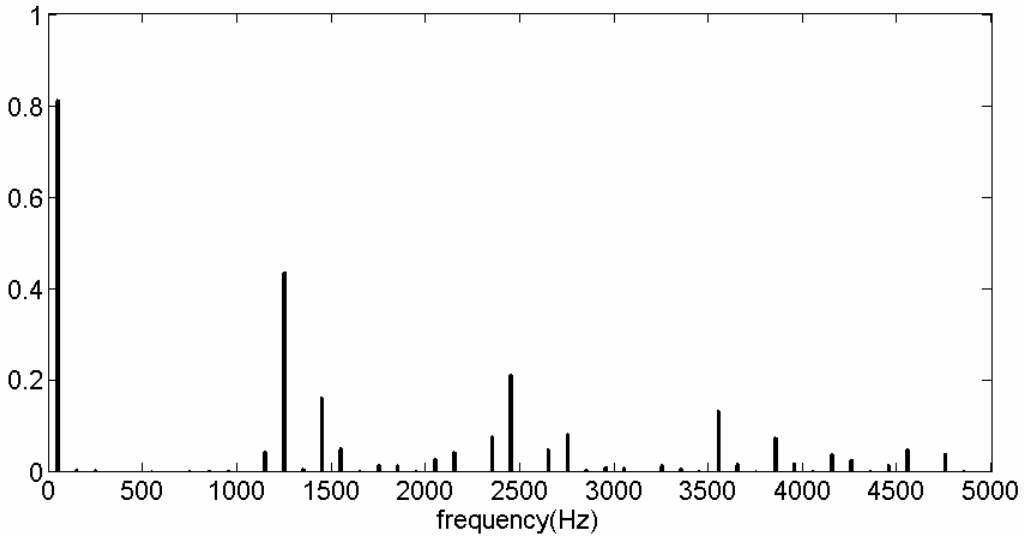


Figure 2.22 Normalized harmonic spectra of converter input current w.r.t. dc-link current for 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonic elimination of SHEM

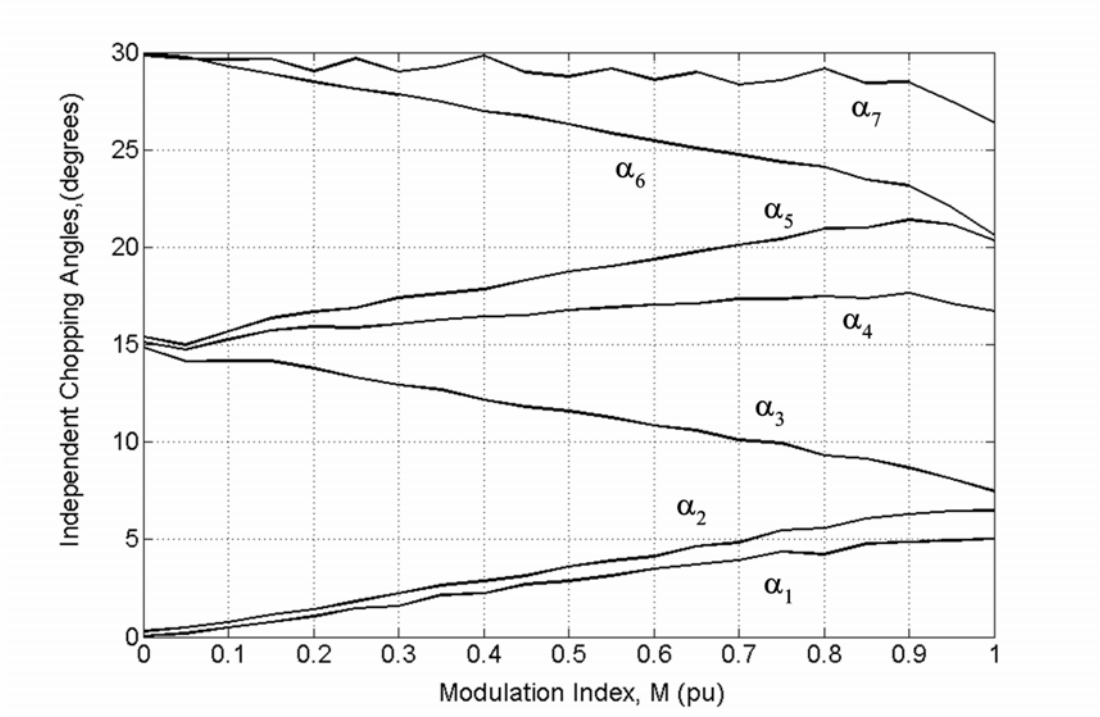


Figure 2.23 The variation independent chopping angles in degrees for the elimination of 5^{th}, 7^{th}, 11^{th}, 13^{th},17^{th} and 19^{th} harmonics in converter input current w.r.t. modulation index

TDD of supply side line currents are given in Fig.2.24 as a function of corner frequency for M=0.8 and two different cases, i.e., elimination of 4 and 6 low order harmonic components. Following conclusions can be drawn from these characteristics:

- Adjusting the corner frequency to a low value such as in the range from 200 to 250Hz allows bringing the number of harmonics eliminated to an absolute minimum, e.g., 4 harmonic elimination and hence minimizes the switching frequency such as 500Hz. However, this occurs at the expense of bulky and costly second order undamped LC input filter. Another drawback of this choice will be the asymmetrical operating characteristics for the STATCOM in inductive and capacitive operation modes and/or higher voltage regulation figures than usual which arise from the use of bulky input filter.
- If it is intended to use a small and hence cheap filter on the ac side then it is advantageous to choose SHEM with higher number of harmonics eliminated,e.g., 6 harmonic elimination, in complying with harmonic standards. This needs higher switching frequency and hence gives rise to higher switching losses.
- In order to comply with harmonic standards for a certain installation site, switching frequency can only be decreased by reducing the corner frequency by employing an input filter larger in size.

It is seen that a comprise is needed between the above factors affecting the design in accordance with the needs of application.

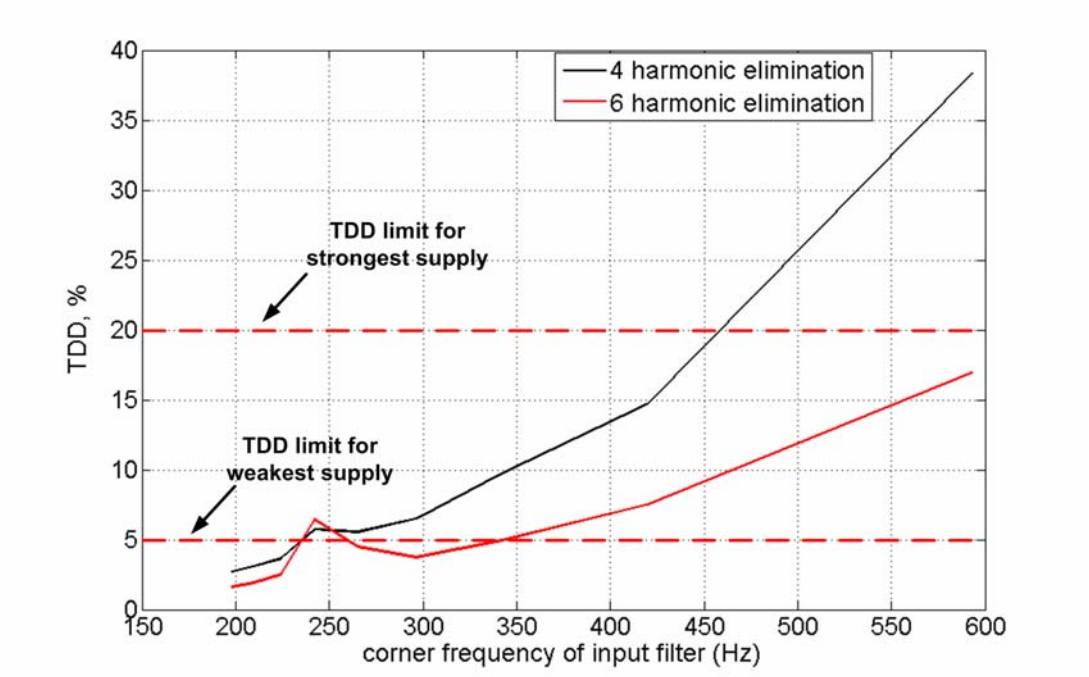


Figure 2.24 Variation of THD in supply current with the corner frequency of theoretical LC low pass input filter for 4 harmonic elimination case (black line) and 6 harmonic elimination (red line) case

2.5 Reactive Power Control Methods For Current Source Converter Based STATCOM

Various control methods are used in the control of reactive power produced by CSC based STATCOM. There is few research work on reactive power control methods in the literature, which can be classified as, i) conventional control methods based on PI-type linear controllers [56,57,59,61,64], ii) modern control methods based on state-space approach [59,60].

Although design and implementation of the conventional control methods are simple, they do not yield an optimal control system [87]. Moreover, they may result in high frequency oscillations in CSC based STATCOM with poorly damped input filter when high proportional gains are used in order to achieve fast transient response [59].

On the other hand, modern control methods based on state-space methods provide optimal control systems, which have desired closed loop poles, and hence improved transient response. Moreover, design and implementation of these methods in dq-stationary reference frame also present following advantages for CSC based STATCOM: i) independent control of active and reactive power, ii) inherent damping for the input filter of CSC, iii) faster transient response [38].

These control methods will be briefly explained in the following subsections.

2.5.1 Conventional Control Method based on PI Controller

As discussed in Section 2.3, the control variables in CSC based STATCOM are the modulation index (M) and phase shift angle (ϕ). The block diagram of the control system is as shown in Fig.2.25. With this control system, dc-link current is controlled via phase shift angle so that it stays constant at the prespecified value of $I_{dc(ref)}$ which is equal to the dc-link current at maximum controllable value of modulation index for the maximum VAr rating of CSC STATCOM. Then, required reactive power can be generated by controlling the modulation. This control approach results in faster response to the changes in reactive power reference. However, it may suffer from higher converter losses and dc reactor losses due to keeping dc-link current at its maximum value for all times. Therefore, the reference of dc-link current can also be controlled depending on the application. The modulation index and phase shift angle are then supplied to switching signal generator, which employs one of the modulation techniques as described in Section 2.4.

For the cases where the control of modulation index is not used, required reactive power is produced by controlling the magnitude of dc-link current via phase shift angle as shown in Fig.2.26.

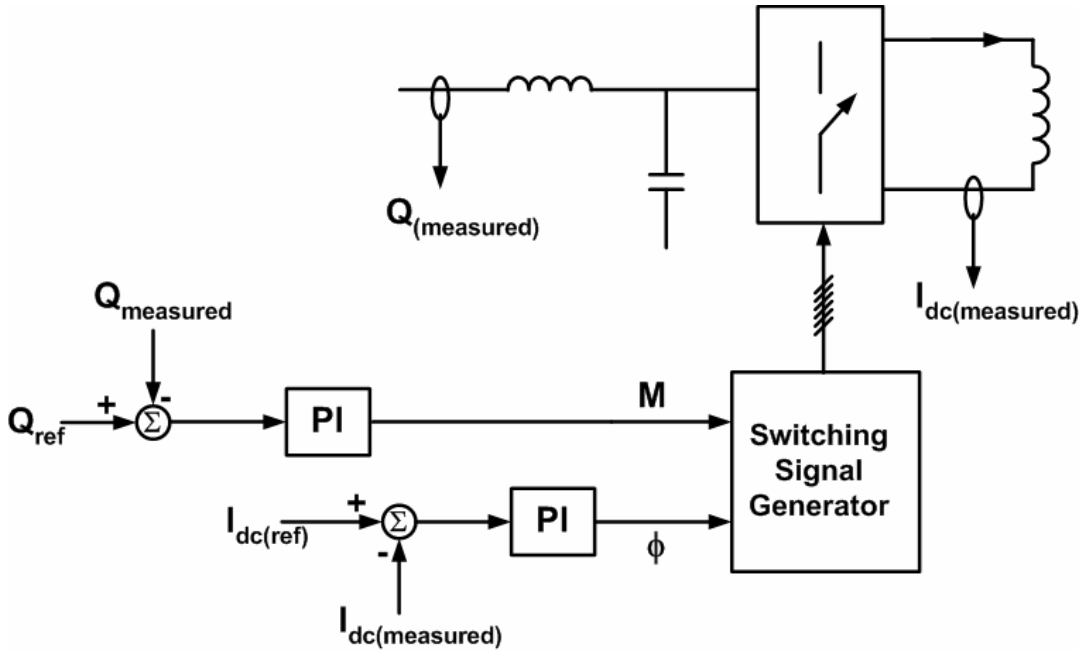


Figure 2.25 Control system based conventional PI controller

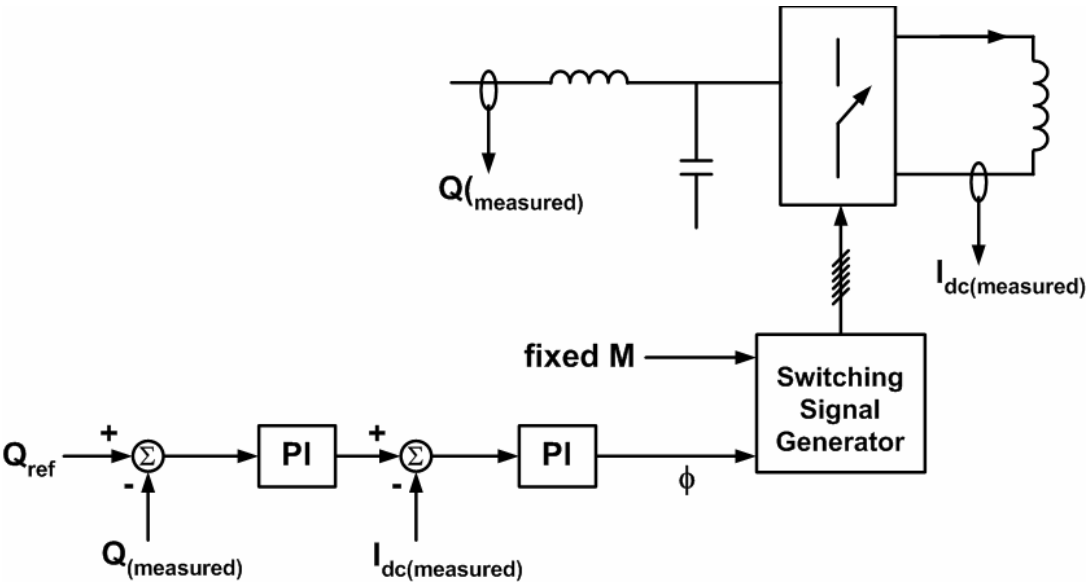


Figure 2.26 Control system based conventional PI controller for CSC based STATCOM, where modulation index control is not applicable

The design or selection of PI parameters in the given control system for optimum response requires the transfer function together with a variety of graphical techniques such as root-locus plots, Bode diagrams. However, these design techniques are applicable only to linear time invariant systems having a single input and single output [87]. Since CSC based STATCOM is non-linear (as will be described in the following subsection) and multi input and multi output, these design techniques are not applicable. Therefore, PI parameters can only be determined by PID tuning rules such as Second Method of Ziegler-Nichols Rules which have been widely used in process control systems [87]. This method can also be applied to the control system in Fig.2.26 in steps as shown in Fig.2.27. Firstly, optimum PI parameters of dc-link current controller are determined by applying a unit step input as shown in Fig.2.27a. Then, optimum parameters of reactive power controller are determined with the use of pre-determined parameters of dc-link current controller by applying a step input to the overall control system in Fig.2.27b.

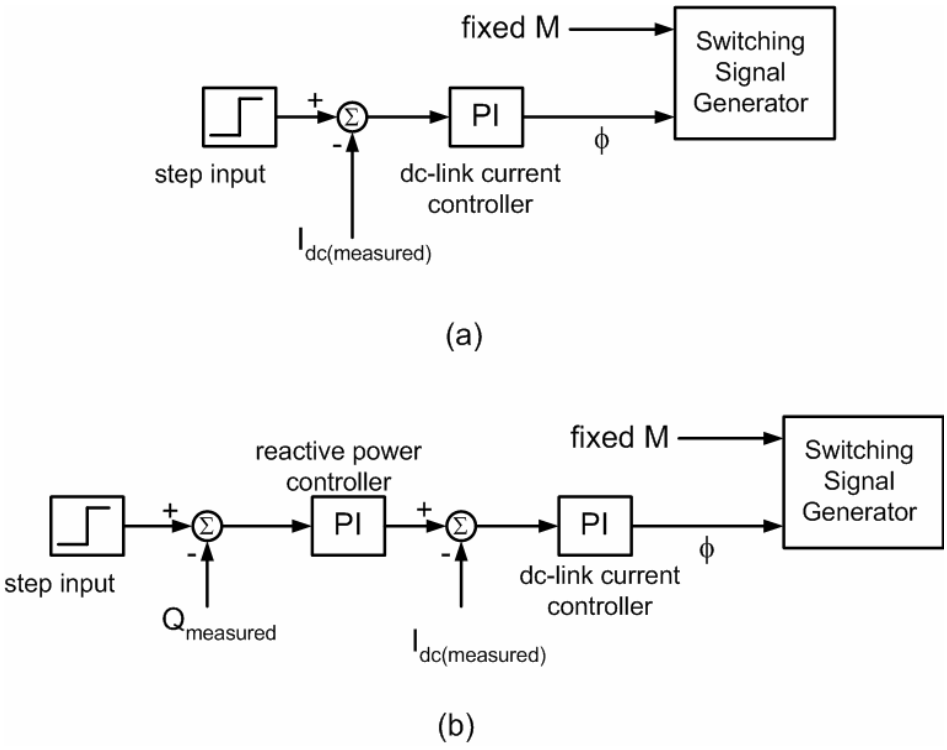


Figure 2.27 Steps applied in tuning PI parameters of CSC based STATCOM control system (a) for dc-link current controller, and (b) for reactive power controller

2.5.2 Modern Control Method based on State Feedback Controller

This control method requires the state-space representation of CSC based STATCOM. It is common to obtain the state-space representation in d-q stationary frame [38, 59-60] since it results in less number of state variables, which become dc quantities in steady-state. This makes both analysis and design of control system relatively easier. The state-space representation of CSC based STATCOM in Fig.2.28 is given in (2.21). Its derivation is included in Appendix B. The equivalent circuit of CSC based STATCOM in Fig.2.29 can be deduced from state-space representation in (2.21).

$$\frac{d}{dt}\begin{bmatrix} i_{sd} \\ i_{sq} \\ v_{cd} \\ v_{cq} \\ i_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega & -\frac{1}{L} & 0 & 0 \\ -\omega & -\frac{R}{L} & 0 & -\frac{1}{L} & 0 \\ \frac{1}{3C} & 0 & 0 & \omega & -\sqrt{\frac{3}{2}}\frac{M}{3C}\sin\theta \\ 0 & \frac{1}{3C} & -\omega & 0 & \sqrt{\frac{3}{2}}\frac{M}{3C}\cos\theta \\ 0 & 0 & \sqrt{\frac{3}{2}}\frac{M}{L_{dc}}\sin\theta & -\sqrt{\frac{3}{2}}\frac{M}{L_{dc}}\cos\theta & -\frac{R_{dc}}{L_{dc}} \end{bmatrix}\begin{bmatrix} i_{sd} \\ i_{sq} \\ v_{cd} \\ v_{cq} \\ i_{dc} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_d \\ v_q \end{bmatrix} \quad (2.21)$$

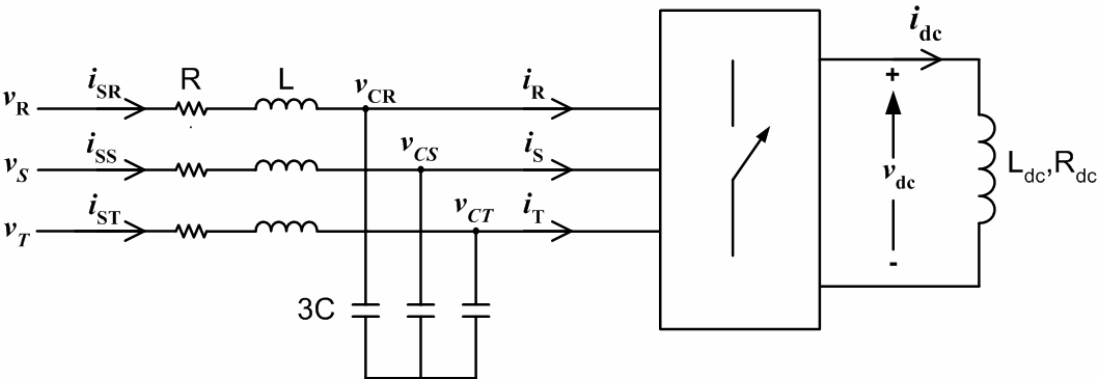
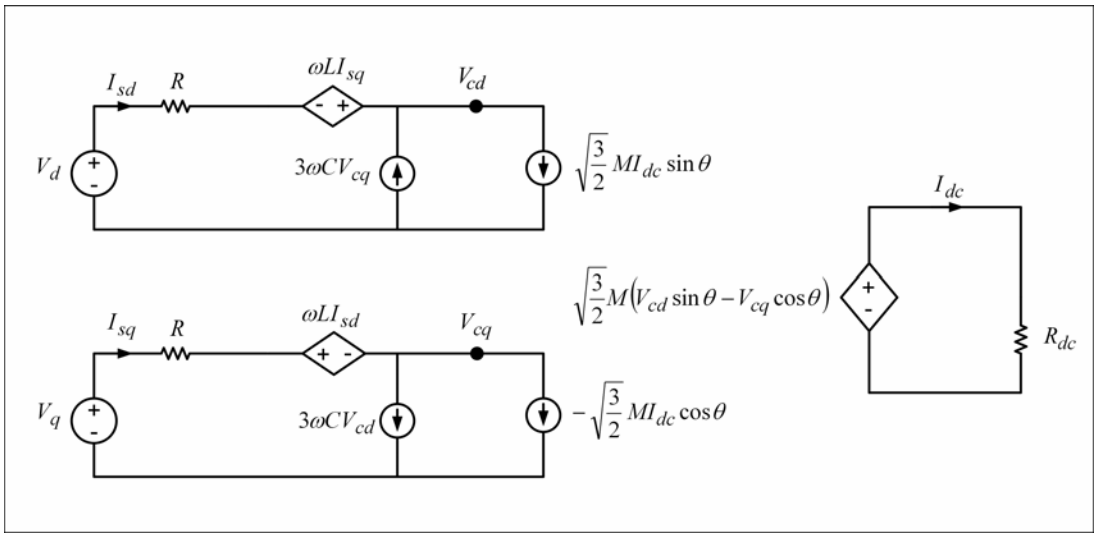
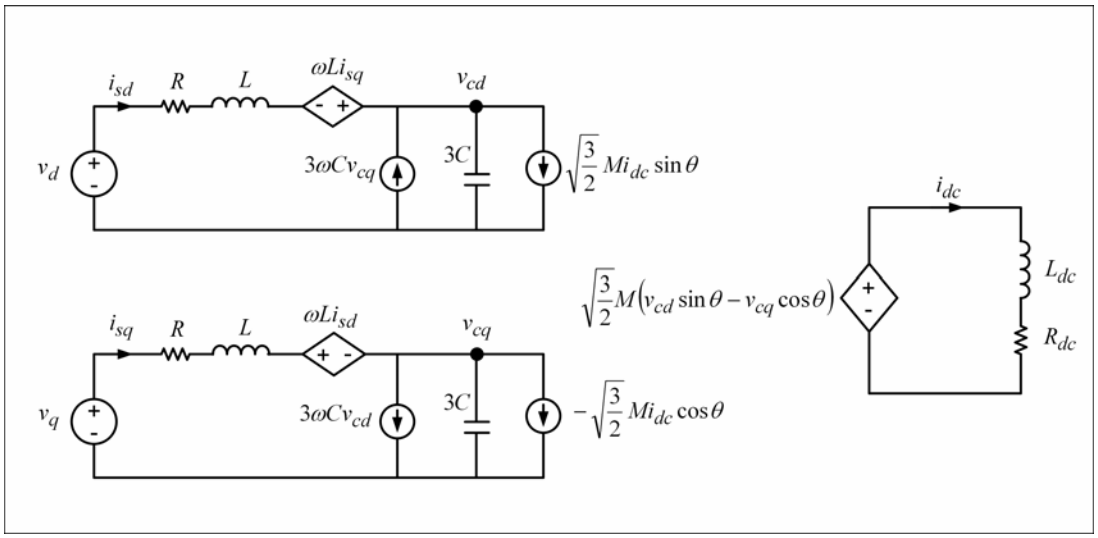


Figure 2.28 Equivalent circuit of CSC based STATCOM in abc-rotating frame



(a)



(b)

Figure 2.29 Equivalent circuit of CSC based STATCOM in dq-stationary frame
(a) for transient state, (b) for steady-state

The state-space representation in (2.21) is re-arranged in (2.22), where M_d and M_q are the controlled input variables and defined in (2.23).

$$\frac{d}{dt}x = \begin{bmatrix} -\frac{R}{L} & \omega & -\frac{1}{L} & 0 \\ -\omega & -\frac{R}{L} & 0 & -\frac{1}{L} \\ \frac{1}{3C} & 0 & 0 & \omega \\ 0 & \frac{1}{3C} & -\omega & 0 \end{bmatrix} x + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{3C} & 0 \\ 0 & \frac{1}{3C} \end{bmatrix} u + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} w \qquad (2.22)$$

$$y = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} x$$

$$\text{where} \quad x = \begin{bmatrix} i_{sd} \\ i_{sq} \\ v_{cd} \\ v_{cq} \end{bmatrix}, \quad u = \begin{bmatrix} M_d\, i_{dc} \\ M_q\, i_{dc} \end{bmatrix}, \quad w = \begin{bmatrix} v_d \\ v_q \end{bmatrix}$$

$$\begin{bmatrix} M_d \\ M_q \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{3}{2}} M \sin\theta \\ -\sqrt{\frac{3}{2}} M \cos\theta \end{bmatrix} \qquad (2.23)$$

Since the state-space representation in (2.22) contains multiplication of controlled input variables and state variables CSC based STATCOM is said to have non-linearity [38]. Moreover, there is a cross-coupling between the d and q axis components of the system, where dc-link current depends on both input variables [38]. These present problem in designing state feedback controller for CSC based STATCOM. Therefore, few work have been carried out in order to linearize and decouple the state-space model of CSC based STATCOM [38,59-60]. Using the linearized and decoupled state-space representation, state-space methods such as pole-placement method via state feedback have been applied to CSC based STATCOM for reactive power control [59-60,87]. The typical block diagram of the control system based on state-feedback controller [59] is given in Fig.2.30. The PI controller in the outer loop generates d-axis reference supply current from the reference and measured dc-link current. Then, reference d and q-axis reference supply currents (where q-axis reference supply current corresponds to the reactive current to be injected by STATCOM) are subtracted from their measured values. Error between them is integrated and then added to the state feedback to obtain the

required control input variables, M_d and M_q. These control variables can then be used by the switching signal generator, which employs one of modulation techniques given in Section 2.4. The gains K_I and K are determined by the pole-placement algorithm [59]. The design and implementation of this controller is beyond the scope of this thesis.

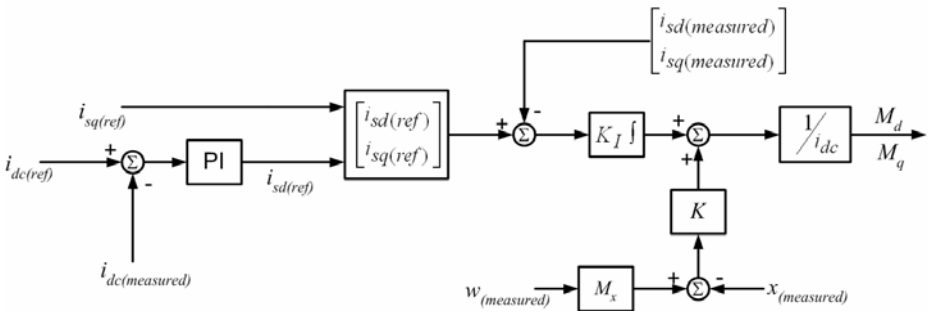
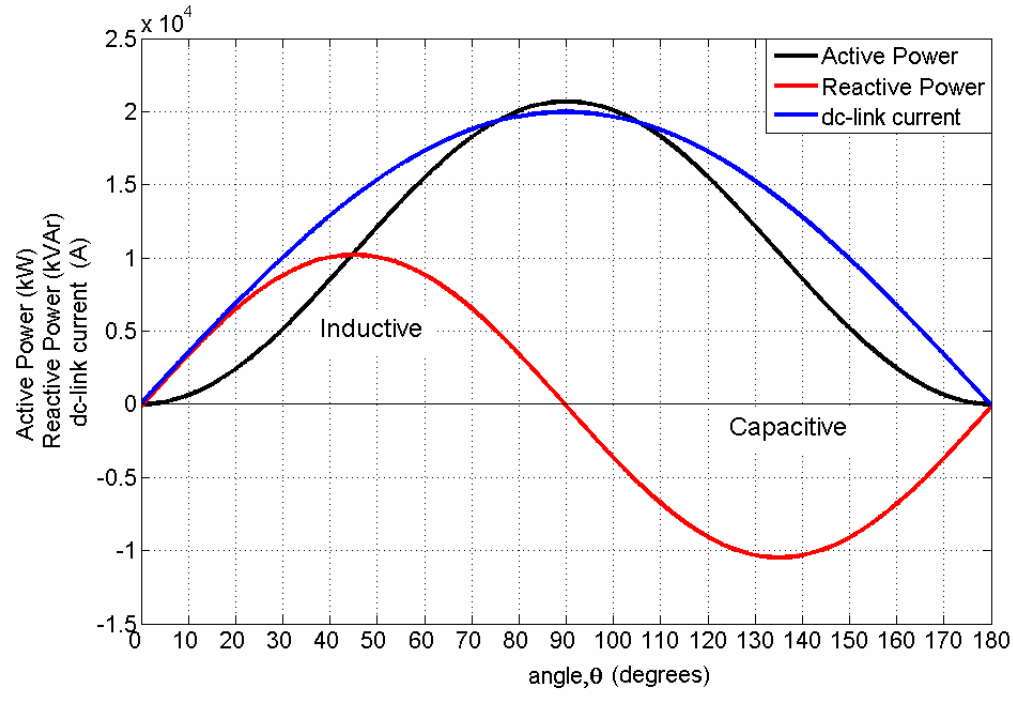


Figure 2.30 Typical block diagram of modern control method based on state feedback controller for CSC based STATCOM [59]

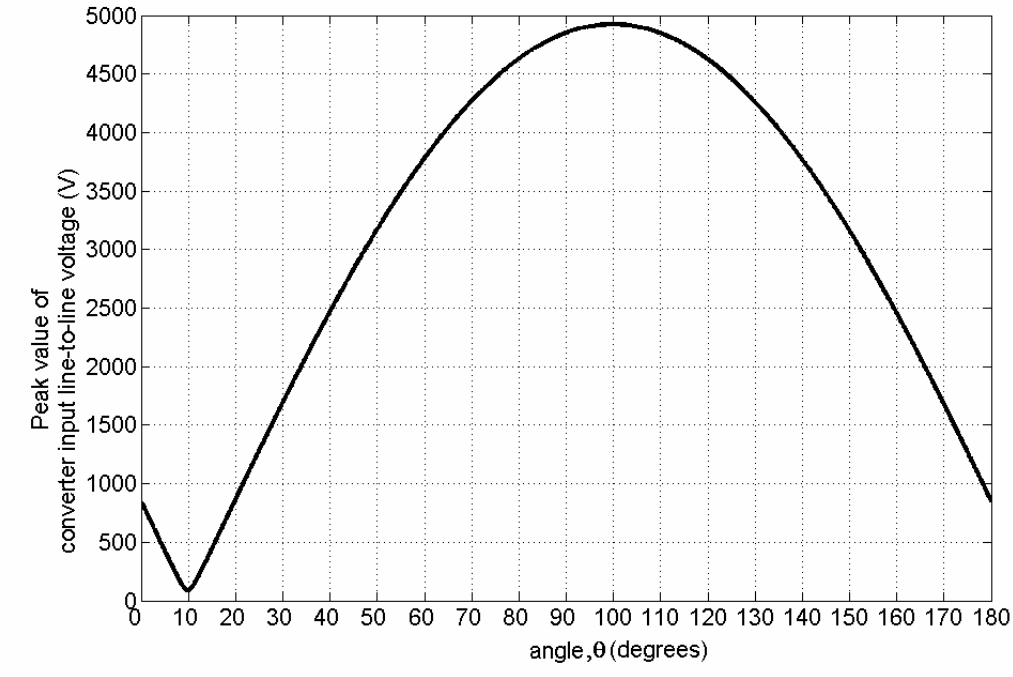
On the other hand, the equivalent model of CSC based STATCOM in d-q stationary frame (Fig.2.29a) is very useful since its steady-state equivalent can be easily derived as given in Fig.2.29b. Steady-state values of the state variables can be easily solved by the use of computer programmes for the given system parameters. As an example, for the given system parameters in Table.2.2, the variations of active and reactive power with angle, θ can be found as in Fig.2.31. It is also possible to find the variations of the other state variables such as converter input line voltage (v_{CR} shown in Fig.2.28) and dc-link current with respect θ as shown in Fig.2.31. These results are consistent with the theoretical results found under the assumptions made in Section 2.3.

Table 2.2 System parameters of a CSC STATCOM, determined in Chapter 3

R=20mΩ	L_{dc}=3mH	V (supply line to line voltage, rms)= 1000V
L=900μH	R_{dc}=30mΩ	ω (supply angular frequency)= 314 radian
C=240μF		



(a) Variations of active and reactive power, dc-link current

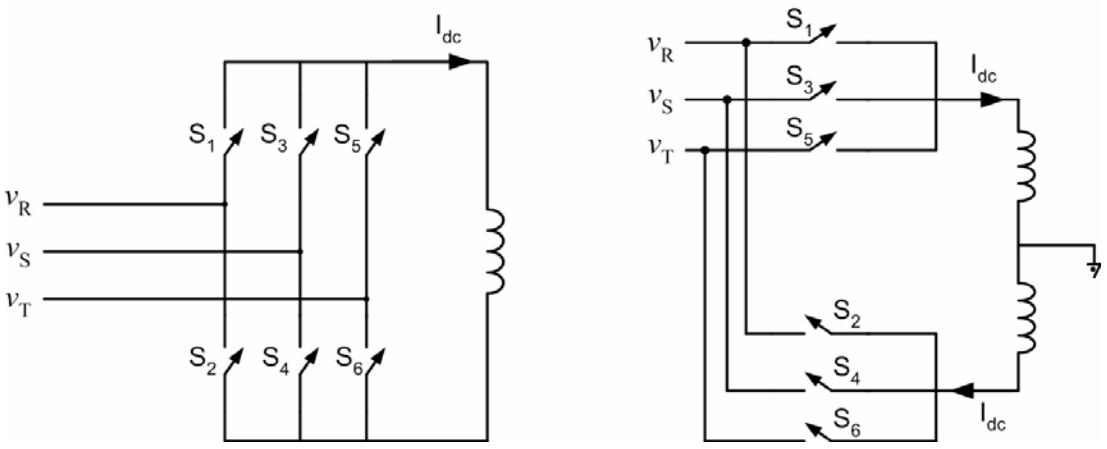


(b) Variation of peak value of converter input line-to-line voltage

Figure 2.31 Variations of steady-state variables of CSC based STATCOM with controlled input variable, angle θ (MATLAB/Simulink)

2.6 Commutation Types in Current Source Converter

In the analysis of three phase line commutated bridge converters, the circuit is usually separated into two three-phase half-wave circuits (midpoint circuits) [86]. This approach can provide us with some simplifications in the analysis of device commutated CSC. The circuit diagram of device commutated CSC in Fig.2.32a can be shown to be equivalent to the equivalent circuit in terms of forward and backward device commutated half wave circuits, shown in Fig.2.32b. The basic commutation types will be firstly described on Fig.2.33b and then the necessary test circuits (see Chapter 3.3) will be used from these findings.



(a) (b)

Figure 2.32 (a) three phase CSC topology, and (b) its equivalent circuit in terms of two three phase half-wave circuits

In the device commutated CSC in Fig.2.32, only two power semiconductors are in conduction at any time, one in the upper half-bridge and one in the lower half-bridge except the commutation period. In the commutation period which is less than 5-10 microseconds for self-commutated devices such as IGCTs and IGBTs, three semiconductors will be in conduction. Commutations which take place in CSC can be summarized as follows,

a) Commutation from one semiconductor to another in the upper half-bridge (among S1, S3, and S5)
b) Commutation from one semiconductor to another in the lower half-bridge (among S2, S4, and S6)
c) Two simultaneous commutations one in the upper half-bridge as in (a) and one in the lower half-bridge as in (b) only for transition from inductive region to capacitive region or vice versa.

Each commutation described above may be one of the following types [37,63,67,77]:

1) **Forced commutation (self commutation)**: The incoming device can be triggered into conduction from its reverse blocking state while the outgoing device is turned off to block positive voltage in the forward direction. Here, transfer of current from outgoing device to the incoming device is called as **forced commutation**, turn-off mechanism of the outgoing device is **forced turn-off** and turn-on mechanism of incoming device is **load turn-on**.

2) **Load commutation**: The incoming device can be triggered into conduction from its forward blocking state while the outgoing device is turned off to block negative voltage in the forward direction. Here, the transfer of current from outgoing device to the incoming device is called as **load commutation**, turn-off mechanism of the outgoing device is **load turn-off** and turn-on mechanism of incoming device is **device turn-on**.

Turn-on mechanism of power semiconductors in a CSC can be classified in two groups as will be described below:

i) **Device turn-on**: If a power semiconductor which is already forward biased receives a turn-on signal, it can turn on successfully. From now on, this kind of turn-on mechanism will be called as **device turn-on** in the thesis.

ii) **Load turn-on**: The power semiconductor receiving a triggering signal does not turn on if it is reverse-biased. However, a successful turn-off of another semiconductor in the same half-bridge may lead to appear a positive voltage in the forward direction across the power terminals of incoming device resulting in transfer of load current from outgoing device to incoming device. From now on, this kind of turn-on mechanism will be called as **load turn-on** in the thesis.

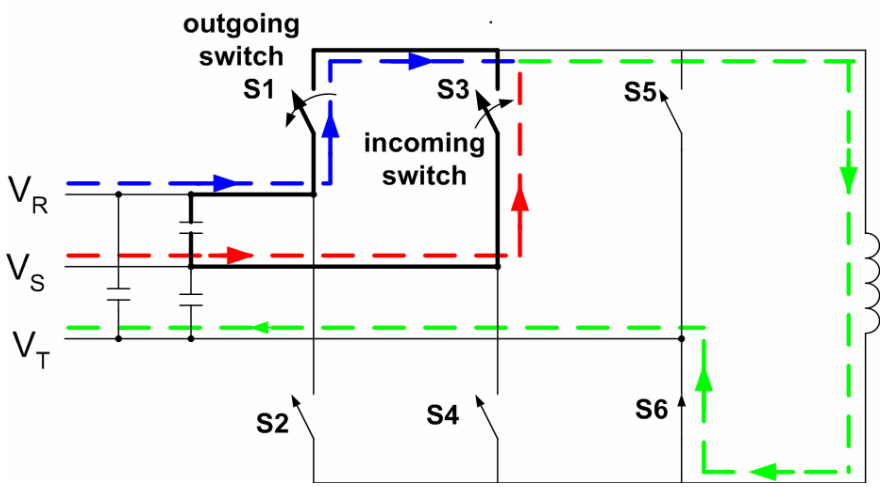
Turn-off mechanisms of power semiconductors in CSC can also be classified in two groups, as will be defined below:

i) **Forced turn-off**: The power semiconductor which is conducting the load current can be successfully turned off by applying a turn-off signal to its control terminal (gate driver). From now on, this kind of turn-off mechanism will be called as **forced turn-off**.

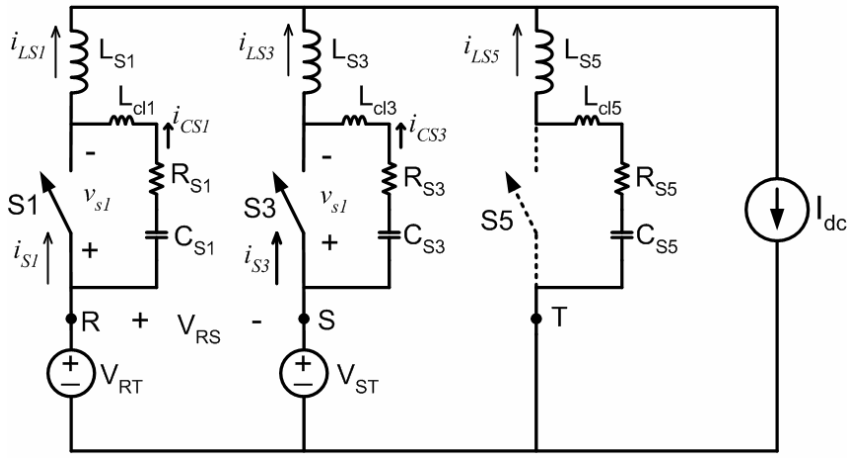
ii) **Load turn-off**: A power semiconductor which is conducting the load current and still receiving turn-on signal can be successfully turned off by turning on another semiconductor in the same circuit according to device turn-on mechanism. Since the load current will be transferred from the outgoing device to the incoming device as a result of device turn-on mechanism of the outgoing device will be called as **load turn-off** in the thesis.

It is worth noting that in the classification of commutation types given above, the name of the ***turn-off mechanism for the outgoing device defines the type of the commutation between incoming and outgoing devices***. Typical commutation process can be observed from Fig. 2.33a. Blue path shows the current flow before the commutation (i.e., S1 and S6 are ON). Red path shows the current flow after commutation (i.e., S3 and S6 are ON). Green path shows the path at which dc-link current flows before, during and after commutation (i.e., S6 is ON before, during and after commutation). For this particular commutation, commutation path is indicated with bold lines in Fig.2.33a. Stray inductance on this commutation path plays an important role, as to be discussed in the following subsections. The commutation paths for all possible commutations in CSC are illustrated in Fig.2.34.

Types of commutation will be described using the equivalent circuit in Fig.2.33b, where power semiconductors for CSC (S1, S3 and S5), stray inductances in the commutation paths (L_{S1}, L_{S3} and L_{S5}) and typical snubber components (L_{cl1}, R_{S1}, C_{S1}, L_{cl3}, R_{S3}, C_{S3}, L_{cl5}, R_{S5}, and C_{S5}) are shown [37, 63]. Since the commutation process takes place within a few microseconds due to fast power semiconductors, voltage across the filter capacitors stays almost constant. Therefore, they are modeled as constant voltage source in Fig.2.33b.



(a) typical commutation path



(b) equivalent circuit

Figure 2.33 Commutation in upper half-bridge of CSC

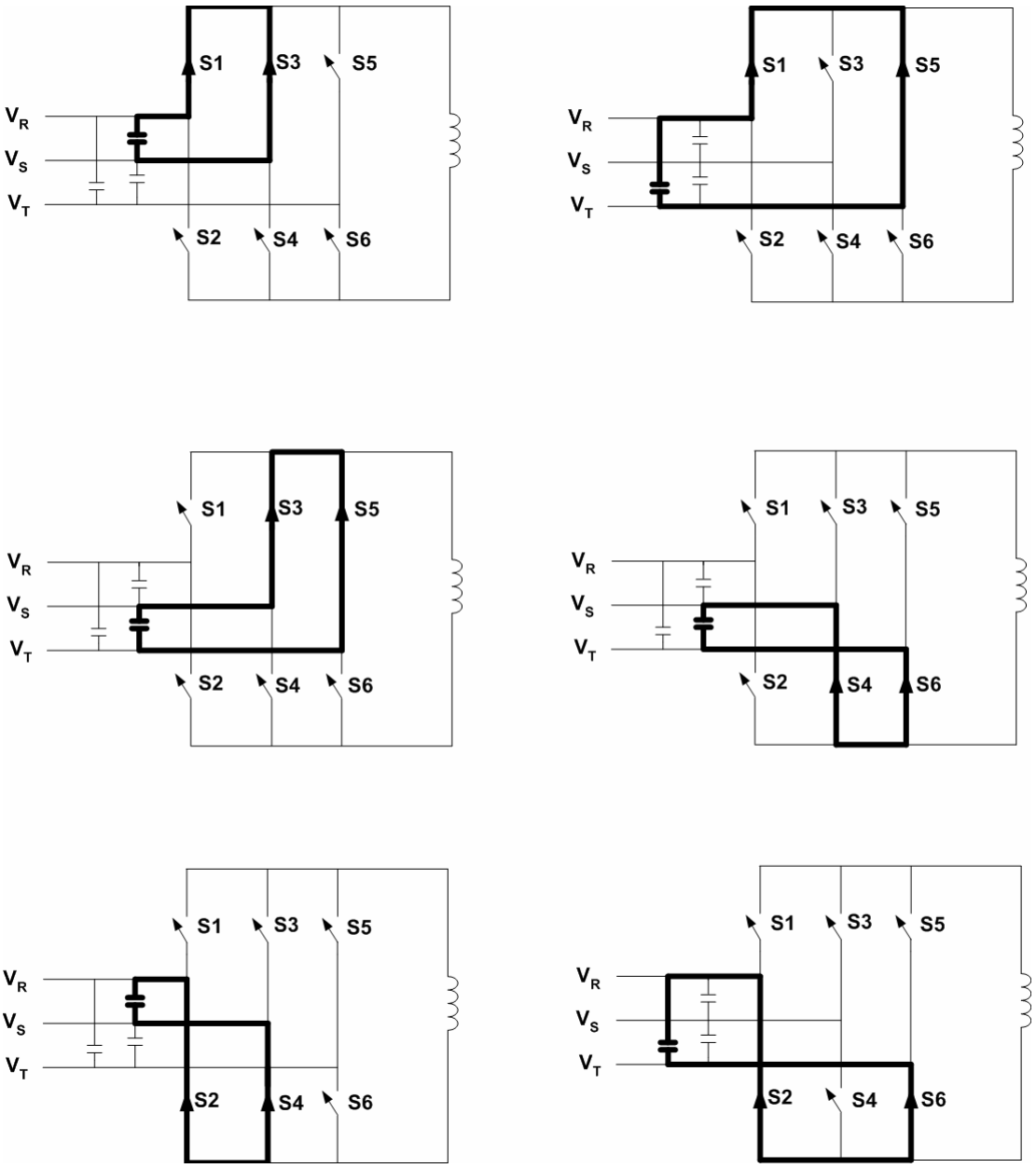


Figure 2.34 All Commutation paths in CSC

2.6.1 Forced Commutation

Referring to Fig.2.33a, if $V_R > V_S$ (i.e., $V_{RS} > 0$) during commutation, the commutation is said to be forced commutation. This particular commutation will be described by using the equivalent circuit in Fig.2.33b where S1 is outgoing and S3 is incoming switch. Theoretical voltage and current waveforms of incoming and outgoing switches are illustrated in Fig.2.35.

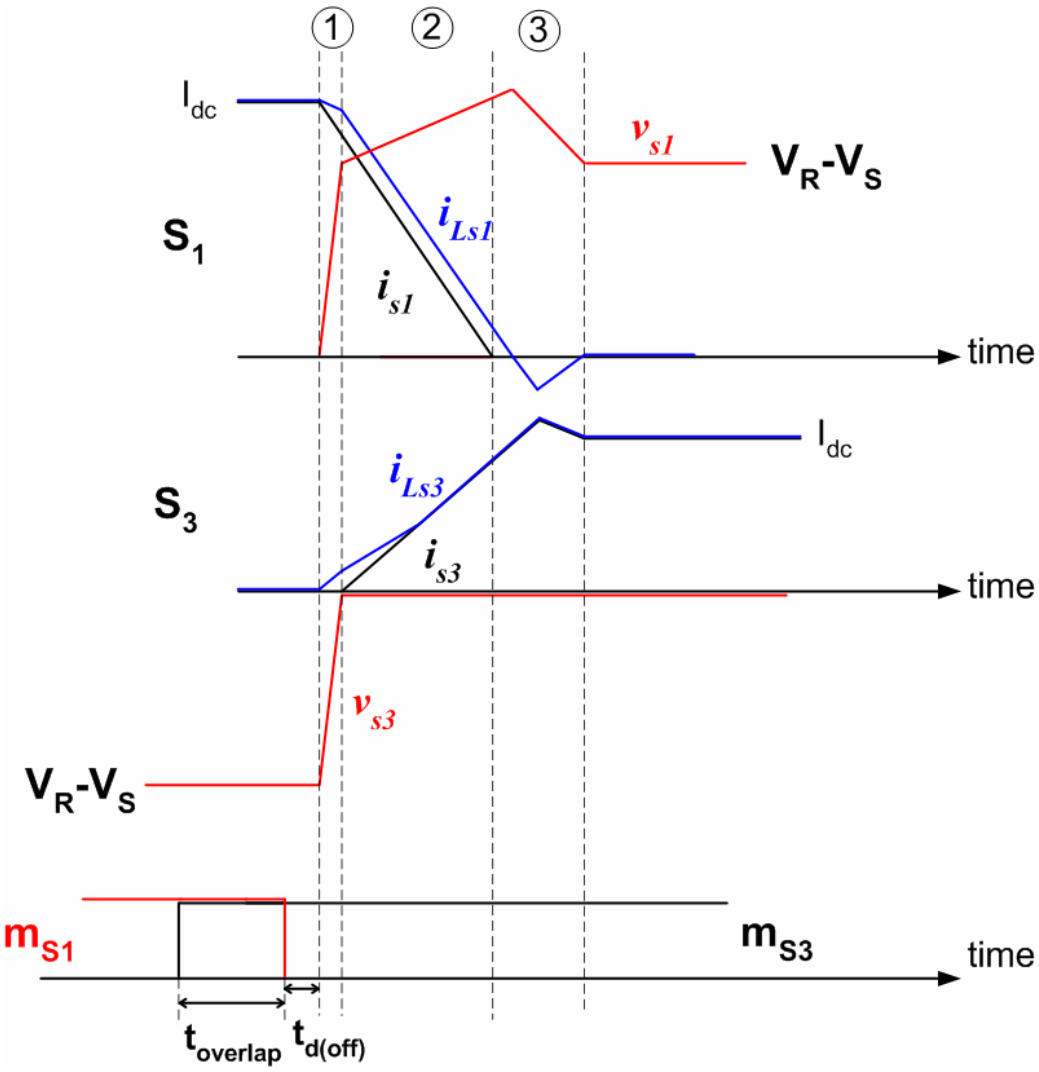


Figure 2.35 Theoretical current and voltage waveforms of power semiconductors S1 and S3 during force commutation where $V_R > V_S$

As seen in Fig.2.35, S3 blocks reverse voltage before the commutation. When the switching signal is applied to S3 for turn-on, the current through S3 can not increase since it is still reverse-biased. Only when the switching signal is applied to S1 for turn-off, the current starts to decay after a turn-off delay time, $t_{d(off)}$ at a di/dt dictated by the device characteristics of S1. In Fig.2.35, as the current through S1 decays, the current through stray inductance, L_{S1} stays nearly constant and the amount of decay in current through S1 flows through the snubber capacitors, C_{S1}, C_{S3} and C_{S5}. This will increase the voltage across S1 in forward direction by a certain dv/dt, which is dictated by its snubber components. At the same time, this will decrease the voltage across S3, as shown in Fig.2.35. For the interval ① indicated on Fig.2.35, state equations are as given in (2.24), referring to quantities given in Fig.2.33b.

$$\left.\begin{aligned} & i_{CS1} + i_{S1} = i_{LS1} \\ & i_{LS3} = i_{CS3} \\ & i_{LS5} = i_{CS5} \\ & i_{LS1} + i_{LS3} + i_{LS5} = I_{dc} \quad \Rightarrow i_{CS1} + i_{CS3} + i_{CS5} = I_{dc} - i_{S1} \end{aligned}\right\} \qquad (2.24)$$

As the voltage across S1 increases and tends to exceed V_{RS}, S3 becomes forward biased and current starts to increase through S3 as shown in Fig.2.35. The rate of increase in current through S3 is equal to the rate of decrease in current through S1 and this rate is dictated by the device characteristics of S1. While the current is commutating from S1 to S3 through a path including S1, L_{S1}, S3, and L_{S3}, there is an over-voltage across S1 due to the stray inductances, L_{S1} and L_{S3} since the current is changing at a rate (di/dt) dictated by S1. This over-voltage charges the snubber of S1 further. These can also be described in terms of state equations in (2.45). Typical voltage and current waveforms given in (2.25) are illustrated for interval ② in Fig.2.35.

$$\left.\begin{aligned} & i_{CS1} + i_{S1} = i_{LS1} \\ & i_{LS3} = i_{S3} \\ & i_{LS5} = i_{CS5} \\ & i_{LS1} + i_{LS3} + i_{LS5} = I_{dc} \quad \Rightarrow i_{CS1} + i_{S3} + i_{CS5} = I_{dc} - i_{S1} \\ & v_{S1} = V_{RS} - L_{s1}\left(\frac{di_{S1}}{dt} - \frac{di_{CS1}}{dt}\right) + L_{S3}\frac{di_{S3}}{dt} \end{aligned}\right\} \quad (2.25)$$

When the current through S1 becomes zero at the end of the interval ②, not only the current through S3 does not reach the value of dc-link current but also the current through L_{S1} does not become zero. Then, current starts flowing through L_{S1}, snubber of S1 and S3 until the current through L_{S1} becomes zero. This will further increase voltage across S1. After total current through L_{S1} is suddenly transferred to the snubber of S1, an extra over voltage across S1 is inevitable. This is expressed in (2.26) and illustrated in Fig.2.35-interval ③.

$$\left.\begin{aligned} & i_{CS1} = i_{LS1} \\ & i_{LS3} = i_{S3} \\ & i_{LS5} = i_{CS5} \\ & i_{LS1} + i_{LS3} + i_{LS5} = I_{dc} \quad \Rightarrow i_{S3} + i_{CS5} = I_{dc} - i_{CS1} \\ & v_{S1} = V_{RS} - L_{s1}\frac{di_{CS1}}{dt} + L_{S3}\frac{di_{S3}}{dt} \end{aligned}\right\} \quad (2.26)$$

Since the commutation is initiated by the turn-off switching signal of outgoing switch S1 and commutation is dictated by the device characteristics of S1, incoming device S3 should be switched on prior to switching off of S1 as shown in Fig.2.35. This overlap in switching signals of devices S1 and S3 shown in Fig.2.35 is not a must since turn-off delay time ($t_{d(off)}$) of power semiconductors such as IGCTs, IGBTs is always greater than their turn-on time ($t_{d(on)}$). However, it will be safer to choose the overlap time ($t_{overlap}$) as ($t_{d(off)}$-$t_{d(on)}$).

As seen from the theoretical waveforms in Fig.2.35, S3 does not experience any switching loss during forced commutation due to zero voltage turn-on. On the other hand, significant losses occur in S1, which is under forced turn off.

2.6.2 Load Commutation

Referring to Fig.2.33a, if $V_S > V_R$ (i.e., $V_{SR} < 0$) during commutation, the commutation is said to be load commutation. This particular commutation will be described by using the equivalent circuit in Fig.2.33b where S1 is outgoing and S3 is incoming switch. Theoretical voltage and current waveforms of incoming and outgoing switches are illustrated in Fig.2.36.

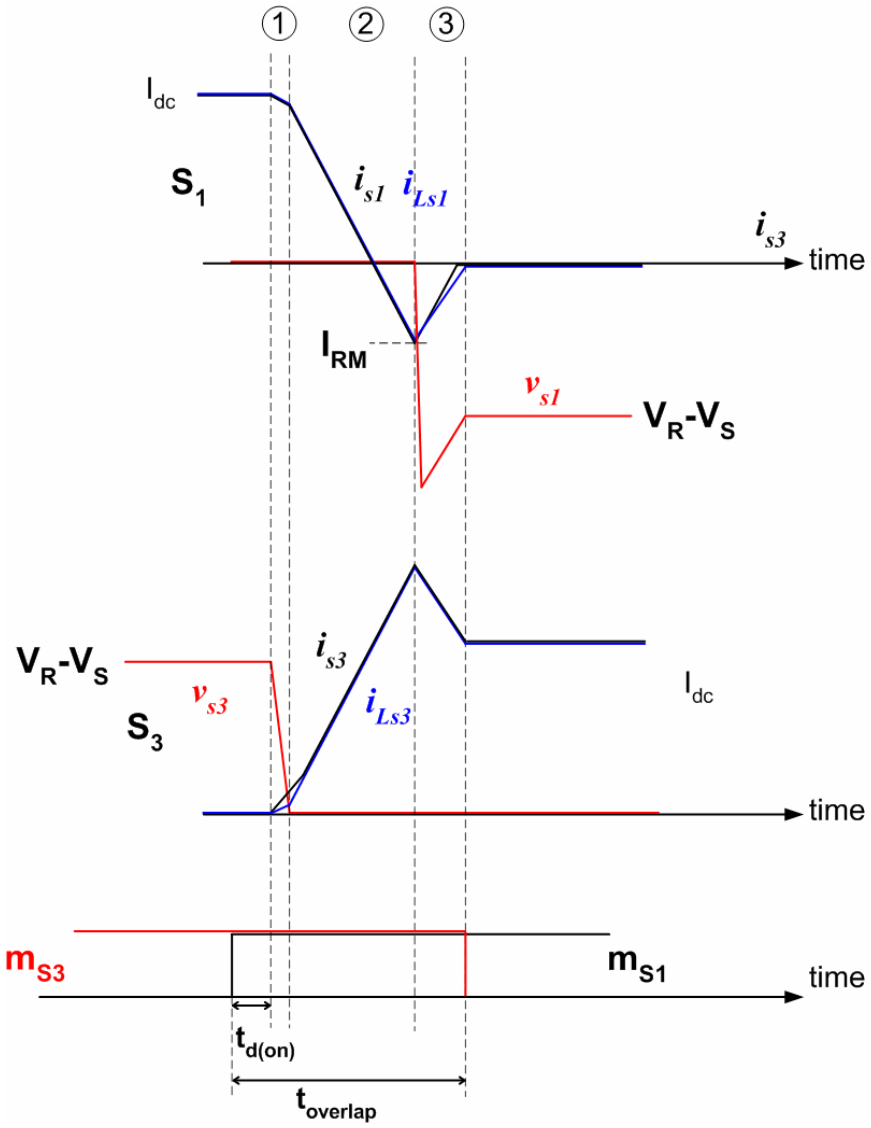


Figure 2.36 Theoretical current and voltage waveforms of power semiconductors S1 and S3 during load commutation where $V_R < V_S$

Before commutation, S3 blocks positive voltage. When S3 is switched on, the voltage across S3 starts to decrease after a turn-on delay time, $t_{d(on)}$. Voltage across S3 almost collapses to zero within one microsecond especially for thyristor based power semiconductors, such as IGCTs, GTOs. This can be observed from interval ① in Fig.2.36. During this interval, snubber capacitor, C_{S3} also discharges to zero through S3. The state equations are given in (2.27). Due to linear decrease in voltage across S3, the rate of decrease in current through S1 and increase through L_{S3} is relatively low, meanwhile the rate of increase in current through S3 is higher due to the discharge of snubber capacitor, C_{S3}. Due to diode of S3, snubber current i_{CS3} stays zero when it reaches to zero.

$$\left.\begin{aligned}
&i_{LS1} = i_{S1} \\
&i_{LS3} = i_{S3} + i_{CS3} \\
&i_{LS5} = i_{CS5} \\
&i_{LS1} + i_{LS3} + i_{LS5} = I_{dc} \quad \Rightarrow i_{S1} + i_{S3} + i_{CS3} + i_{CS5} = I_{dc} \\
&V_{RS} + v_{S3} = L_{S1}\frac{di_{S1}}{dt} - L_{S3}\frac{di_{LS3}}{dt} \\
&V_{RS} + v_{S3} = L_{cl3}\frac{di_{CS3}}{dt} + R_{S3}\,i_{CS3} + \frac{1}{C_{S3}}\int i_{CS3}dt \\
&-V_{RT} - L_{S1}\frac{di_{S1}}{dt} = \left(L_{S5} + L_{cl5}\right)\frac{di_{CS5}}{dt} + R_{S5}\,i_{CS5} + \frac{1}{C_{S5}}\int i_{CS5}dt
\end{aligned}\right\} \quad (2.27)$$

At the beginning of interval ②, snubber current i_{CS3} becomes zero and voltage across S3 reaches to zero. Since the current through S1 is still decaying, S1 is still conducting and its voltage is still zero until its current is equal to maximum reverse recovery current, I_{RM}. Then, state equations can then be written as in (2.28). Neglecting the snubber current of S5, i_{CS5} , rate of decay in S1 current and rate of increase in S3 current become equal and can be expressed as in (2.29). Since V_{RS} has assumed to be almost constant during commutation, rate of change in currents through S1 and S3 become linear. This is dictated by line to line voltage V_{RS}.

$$\left.\begin{aligned}
&i_{LS1} = i_{S1} \\
&i_{LS3} = i_{S3} \\
&i_{LS5} = i_{CS5} \\
&i_{LS1} + i_{LS3} + i_{LS5} = I_{dc} \quad \Rightarrow i_{S1} + i_{S3} + i_{CS5} = I_{dc} \\
&V_{RS} = L_{S1}\frac{di_{S1}}{dt} - L_{S3}\frac{di_{S3}}{dt} \\
&-V_{RT} - L_{S1}\frac{di_{S1}}{dt} = \left(L_{S5} + L_{cl5}\right)\frac{di_{CS5}}{dt} + R_{S5}\, i_{CS5} + \frac{1}{C_{S5}}\int i_{CS5}dt
\end{aligned}\right\} \quad (2.28)$$

$$V_{RS} = \left(L_{S1} + L_{S3}\right)\frac{di_{S1}}{dt} = -\left(L_{S1} + L_{S3}\right)\frac{di_{S3}}{dt} \quad (2.29)$$

After the current through S1, i_{S1} reaches maximum reverse recovery current, S1 starts to experience reverse recovery. Its current decays to zero at a di/dt which depends on its device characteristics. This behaviour can be observed from interval ③ in Fig.2.36. The state equations for interval ③ are given in (2.30). The rate of increase in current through L_{S1} and decrease in current through L_{S3} results in over-voltage beyond V_{RS} across diode of S1. Although this rate of change in current is dictated by the device characteristics of S1, the rate of change is softened by the presence of snubbers across S1 and partly snubber across S5. Therefore, the excessive over-voltage across S1 can be limited.

$$\left.\begin{aligned}
&i_{LS1} = i_{S1} + i_{CS1} \\
&i_{LS3} = i_{S3} \\
&i_{LS5} = i_{CS5} \\
&i_{LS1} + i_{LS3} + i_{LS5} = I_{dc} \quad \Rightarrow i_{S1} + i_{S3} + i_{CS1} + i_{CS5} = I_{dc} \\
&v_{S1} = V_{RS} - L_{S1}\frac{di_{LS1}}{dt} + L_{S3}\frac{di_{S3}}{dt} \\
&v_{S1} = L_{cl1}\frac{di_{CS1}}{dt} + R_{S1}i_{CS1} + \frac{1}{C_{S1}}\int i_{CS1}dt \\
&-V_{RT} - v_{S1} = -L_{S1}\frac{di_{LS1}}{dt} + \left(L_{S5} + L_{cl5}\right)\frac{di_{CS5}}{dt} + R_{S5}i_{CS5} + \frac{1}{C_{S5}}\int i_{CS5}dt
\end{aligned}\right\} \quad (2.30)$$

As seen from Fig.2.36, S3 experiences turn-on power loss, but this can be even further reduced by reducing di/dt due to nearly zero current turn-on. On the other hand, significant loss occurs in S1 during its reverse recovery phase. This reverse recovery loss is due to the magnitude of maximum reverse recovery current, I_{RM} and the overvoltage across it. Magnitude of maximum reverse recovery current can also be reduced by reducing the rate of decay in diode current (di/dt) in interval ② prior to reverse recovery loss. This di/dt can be reduced by increasing L_{S1} and L_{S3}. This can be easily observed from (2.31). Not only the overvoltage but also the rate of increase in voltage (dv/dt) across S1 can be reduced by increasing the snubber capacitance at the expense of higher snubber losses, as to be discussed in detail in Chapter 3.7.

The commutation is initiated with switching on S3. After the reverse recovery of S1, S1 is switched off. It is also possible to switch on S3 and switch off S1 simultaneously since turn-off delay of power semiconductors is always larger than their turn-on delay. However, in some cases where di/dt is so slow and initial current is high, S1 may be switched off before its reverse recovery. In that case, dc-link current can not be totally commutated to incoming switch S3 resulting in a dangerous overvoltage across all the power semiconductors due to large dc-link reactor. Therefore, it is better to apply an overlap of 5-10 microseconds.

2.7 Discussions

In this chapter, system description and operating principles of three phase CSC based STATCOM have been presented in order to satisfy following objectives:

- Nearly sinusoidal currents should be produced,
- Magnitude of these currents should be fully controlled,
- The phases of the produced current should be fully controlled with respect to supply voltages in order to permit the flow of desired amount of active and reactive powers in the desired direction.

It has been demonstrated that for reactive power control of CSC, there are two control variable: modulation index, M and phase shift angle, ϕ. By using ϕ, active power flow to/from CSC can be controlled, hence the magnitude of dc-link current

can be adjusted. The reactive power produced by CSC has been shown to be directly related to the modulation index, M and magnitude of dc-link current, I_{dc}. With simultaneous control of M and I_{dc}, a fast reactive power control can be obtained.

Among the available modulation techniques for CSC, common modulation techniques have been compared and classified as on-line techniques (such as MSPWM and SVPWM) and off-line techniques (SHEM). Although the continuous control of modulation index is impractical in SHEM, it presents superior harmonic spectra for the line current at ac terminals of CSC. This feature makes it the commonly applied technique in high power CSC applications, such as in MV drives. Then, SHEM has been explained in detail and the principles on generation of switching patterns have been given for two different cases: elimination of selected 4 harmonics and elimination of selected 6 harmonics. As the number of selected harmonics increases, the switching frequency also increases. The variation of independent angles with the modulation index has been also given for two cases and from these, it can be observed that as the number of selected harmonics increases, these angles become close to each other, resulting in smaller pulse widths. This may impose a significant constraint in practical application in selection of power semiconductors. However, it has been also illustrated that as the number of harmonics eliminated increases, distortion of line currents decreases. Not only this satisfies the objective of nearly sinusoidal current injection but also provides the use of smaller input filter having higher corner frequency.

Based on the basic control variables, possible control methods for reactive power control for CSC based STATCOM have been also presented. While conventional control methods based on linear controllers such as PI controller present simple, time-effective design solutions, modern control methods based on full state feedback controller results in faster response and inherent damping effect for oscillations in the input filter. Despite of the attractive performances, the use of modern control methods requires the linear model of CSC based STATCOM. The equivalent model of CSC in dq-stationary frame has been given in order to illustrate the non-linearity in CSC based STATCOM. Since linearization and design of the model for state feedback control is beyond the scope of this study, its principles has

been stated and typical block diagram has been given. The equivalent model of CSC based STATCOM in dq-stationary frame has been used in order to analyze the variations of state variables against angle (θ). Instead of modern control methods, design and implementation principles of a typical conventional control method based on PI controller has been proposed using Ziegler Nichols tuning rules for reactive power control of CSC based STATCOM.

Beside the principles of reactive control methods and modulation techniques, basic operation of CSC in terms of current commutations between the power semiconductors is very important for design and implementation of CSC based STATCOM. These commutation types have been defined and explained in detail.

In summary, system description and operating principles of three phase CSC based STATCOM has been given in this chapter so that design and implementation can be done accordingly in the next chapter.

CHAPTER 3

DESIGN OF CURRENT SOURCE CONVERTER BASED STATCOM

3.1 Introduction

The system description and operating principles of three phase Current Source Converter (CSC) based STATCOM have been presented in previous chapter. It has been illustrated that three phase CSC based STATCOM should meet following objectives

- Nearly sinusoidal currents should be produced,
- Magnitude of these currents should be fully controlled,
- The phases of the produced current should be fully controlled with respect to supply voltages in order to permit the flow of desired amount of active and reactive powers in the desired direction.

In this chapter, the design and implementation of a high power prototype for three phase CSC based STATCOM satisfying the above objectives will be presented. Design of the prototype system will be accomplished in view of reactive power compensation requirements of an actual sample application that is load compensation of coal mining excavators.

The design methodology used in this work is based on analysis, simulation and experimental work. The simulation of CSC based STATCOM has been carried out by using PSCAD/EMDTC simulation tool. The modulation techniques and control methods of the prototype system has been exercised with this model. The ratings of power semiconductors, input filter components, dc-link reactor, snubber components have all been determined by using this simulation model. The details of this simulation model can be found in Appendix C. Analysis such as the effects of

snubber components in snubber design has been carried out by MATLAB/Simulink. The optimization algorithms for calculating independent chopping angles for Selective Harmonic Elimination have been applied by using MATLAB/Optimization Toolbox. In some cases, where the use of simulation is not adequate or impractical, experimental work has been carried out in the laboratory, such as in determination of switching characteristics for power semiconductors or verification of snubber effects.

In this chapter, defining the load characteristics of sample application (load compensation of coal mining excavators) technical specifications of the prototype CSC based STATCOM will be determined first. Then, criteria on the selection of power semiconductors will be given by comparing different combinations of candidate power semiconductors and then the application of proper modulation technique will be discussed on the basis of selected power semiconductor. Next, a qualitative design criteria for input filter and dc-link reactor will be posted. The design of power stage for CSC based STATCOM will be presented in two different parts: design of CSC power stage layout and design of overall power stage for STATCOM system. The design criteria on selection of snubber type and its components will be given on the basis of power semiconductor switching waveforms and then verified by experimental results. The design of protection circuit used in prototype system will be discussed. The implementation of the control system including reactive power controller and switching signal generator will be presented. In the final section, discussion on maximum utilization of designed CSC based STATCOM will be posted.

3.2 Design Specifications of Protoype System

Within the scope of this thesis, the protoype of CSC based STATCOM has been designed and developed in order to compensate the reactive power demands of coal mining electric excavators in Tınaz Transformer Substation of South Eagen

Open Cast Lignite Mining Enterprise (GELI) connected to Turkish Coal Enterprises (TKI).

Electrical excavators, shown in Fig.3.1 are the key equipments in open cast coal mining applications. In addition to their intermittent character as a load on the network, they may be the sources of harmonics, and consumers of reactive power. The severity of power quality problems arising from electric motor drive technology: i)Ward Leonard drives, ii) dc motor drives based on phase-controlled thyristor rectifiers and, iii) variable frequency ac motor drives based on dc link converters [64]. Within the scope of this work, electric excavators are powered by Ward Leonard drives. As shown in Fig.3.1, there are two types of electric excavators in Tınaz Transformer Substation: i) dragline and ii) power shovel.

Figure 3.1 General view of open-cast lignite mining site (top: power shovels, bottom:dragline)

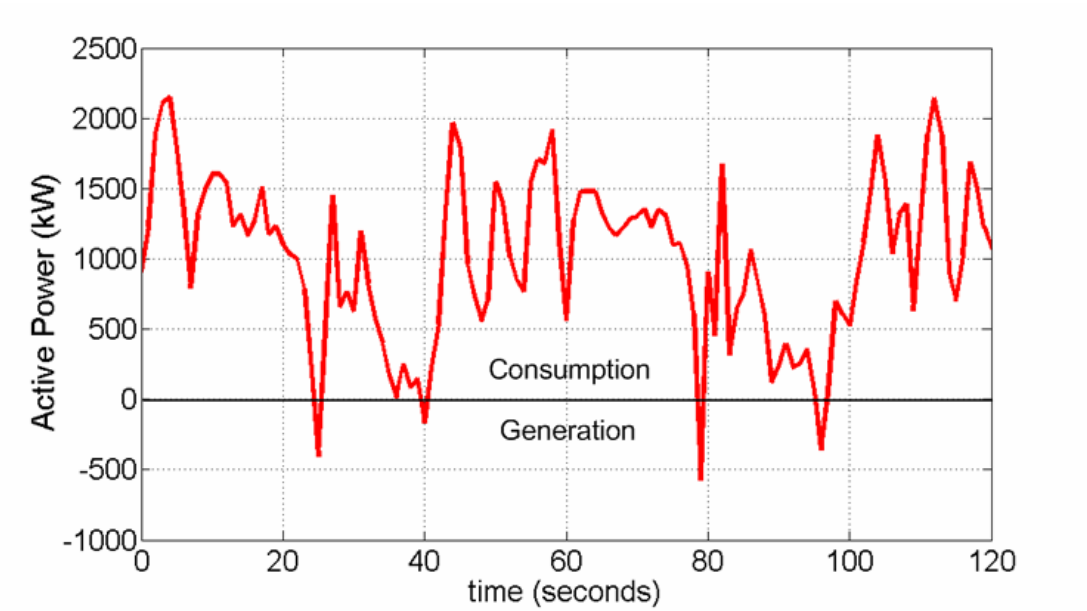
Dragline is the largest electric excavator, which is rated at 2000kW and 6.3kV. Its Ward-Leonard drive is powered by synchronous motors, which are operated in over-excited mode to maximize the electromechnical torque. Therefore, dragline behaves as a capacitive load. The typical active and reactive power variation of the dragline for a few operating cycle are as given in Fig.3.2.

Power shovel, the other type of electric excavators, is rated at 600kW, 6.3kV. Its Ward-Leonard drive is powered by an asynchronous motor, which always behaves as an inductive load. The typical active and reactive power variations of a power shovel for a few operating cycle are as given in Fig.3.3.

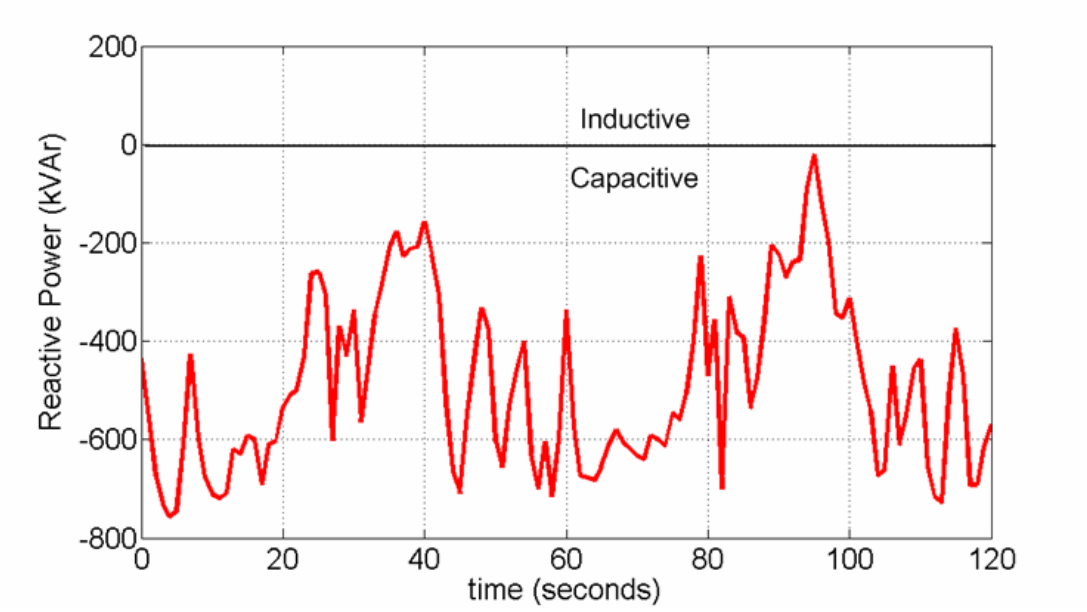
One dragline and one power shovel are connected to a common 6.3kV medium voltage bus as shown in Fig.3.4. Instead of solving reactive power compensation problem on each electric excavators individually, group compensation approach [5,64] is found to be more feasible and economical. For group compensation, CSC based STATCOM system is connected to 31.5kV medium voltage level as shown in Fig.3.4. Then, STATCOM compensates the reactive power demand of the transformer substation, where electric excavators are the main loads.

Considering the reactive power demands of the electric excavators and reactive energy penalty limits in Table 1.1, reactive power rating of CSC STATCOM has been specified to be in the range from 500kVAr capacitive (-500kVAr) to 500kVAr inductive (+500kVAr). CSC based STATCOM system is intended to meet the harmonic limits (TDD-Total Demand Distortion) specified to be 15% for PCC shown in Fig.3.4.

The voltage level at which CSC is designed has been specified as 1kV, because it is a standard low voltage level [66], thus permitting the use of standard components and switchgear devices. Moreover, this choice makes the CSC STATCOM specifications compatible with other TCR based SVCs in TKI [5,64]. This also provides the unification of SVC systems.

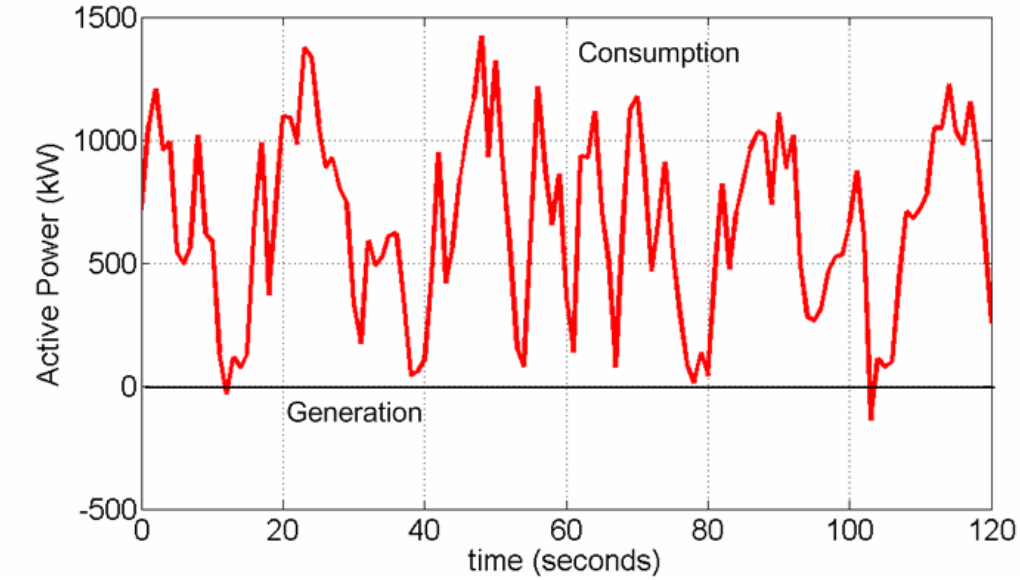


(a)

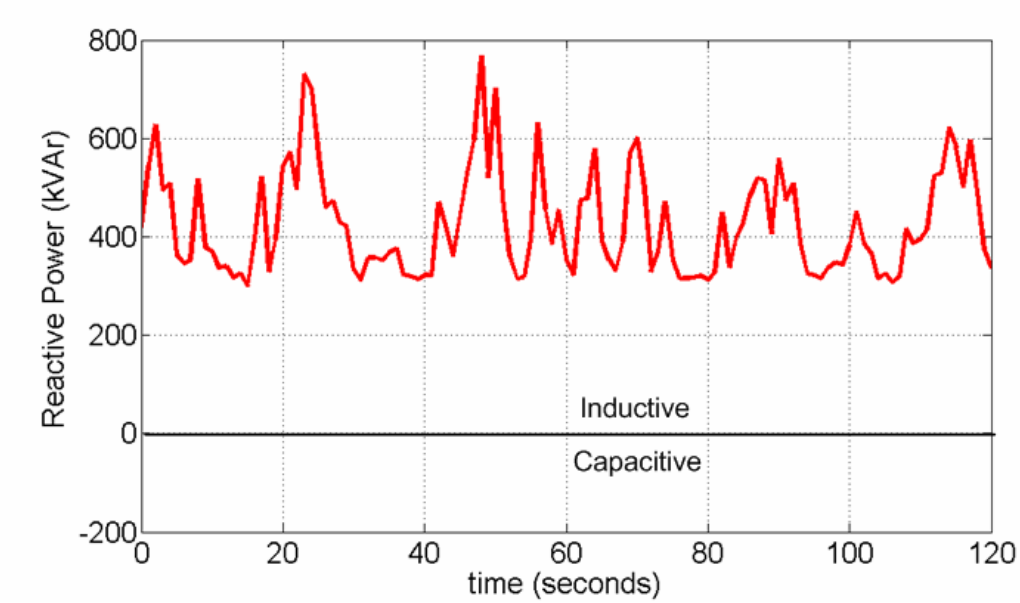


(b)

Figure 3.2 (a) Active (b) reactive power variation of dragline in Tınaz open cast mine of TKI



(a)



(b)

Figure 3.3 (a) Active (b) reactive power variation of power shovel in Tınaz open cast mine of TKI

Since transformer substation is a few tens of km far from the open cast coal mining site STATCOM should need minimum maintanance and monitoring. This imposes natural air cooling for the cooling in STATCOM. The sites of open cast coal mining sites are not stationary, and hence electric excavators should also be moved to the new site. Therefore, transformer substations in open cast mining are to be relocatable, hence STATCOM system should also be relocatable.

According to the constraints defined above, technical specifications of the prototpe system are listed in Table 3.1. The design of CSC based STATCOM system will be carried out in view of these technical specifications.

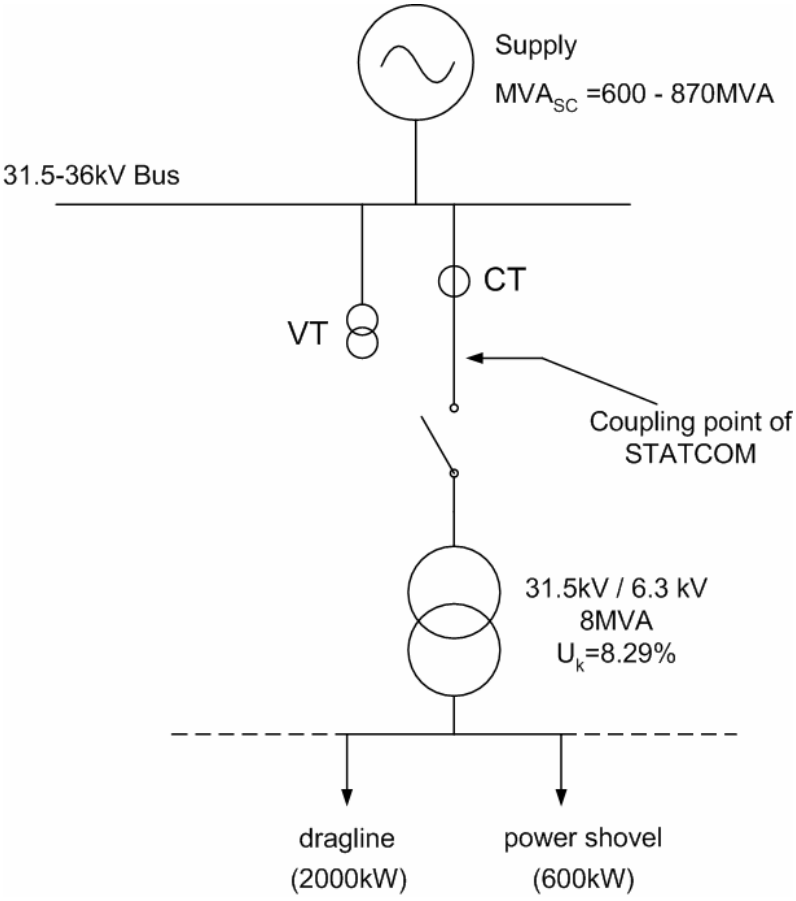


Figure 3.4 Illustration of transformer substation and the coupling point of STATCOM on a simple single line diagram of feeder

Table 3.1 Technical Specifications of the prototype system

Technical Specification	Ratings
Nominal Reactive Power Output Range	500kVAr Capacitive 500kVAr Inductive
Nominal Converter Voltage	1 kV±10% , line-to-line rms, 50Hz
Harmonic Distortion, (TDD)	< 15%
Efficacy (%)	< 10%
Cooling System	Natural Air Cooling for converter Air Ventilation for cabinets
Response Time to a step change in reactive power demand of load	<100msec
Maximum Overshoot in Reactive Power Output of STATCOM to a step change in reactive power demand of load	< 20%

3.3 Selection of Power Semiconductors

Since the voltage level of CSC is specified as 1 kV and minimum peak value of voltage across the power semiconductor should be taken as $\sqrt{2}$ x1.41x$V_{line\text{-}to\text{-}line,(rms)}$ +50% for safety, the voltage rating of power semiconductors in CSC must be 3300V or higher. The candidate fully controllable power semiconductor switches are GTO (Gate Turn-Off Thyristor), IGBT (Insulated Gate Bipolar Transistor) and IGCT (Integrated Gate Commutated Thyristor). However, due to its inherent drawbacks on switching perfomance such as low turn-on di/dt, turn-off dv/dt ratings, complex drive circuitry, GTO is eliminated for the use in CSC as compared with IGCT and IGBT. Although there are also other novel power semiconductor switches such as IEGT (Injetion Enhanced Gate Transistor) from Toshiba [85] and ETO (Emitter Turn-Off Thyristor) [63], they have not been commercialized yet.

As stated in Chapter 2, there are fully controllable power semiconductor switches in CSC. They have unidirectional current flow and bipolar voltage blocking capability. These power semiconductors are characterized as symmetrical devices

[74]. Symmetrical IGCT (SGCT) has been known and commercially available for a few years [41,47,63,77-79]. On the other hand, symmetrical High Voltage IGBT (HV-IGBT) has not been produced yet. HV-IGBTs are generally reverse-conducting devices, in which there is an antiparallel freewheeling diode in the same housing [74]. But, there are also some asymmetric HV-IGBTs [84], which do not have anti-parallel freewheeling diode and can not block reverse voltage. Beside the HV-IGBTs, there are also Asymmetric IGCTs and Reverse Conducting IGCT (RC-IGCT) [71,74]. Although the most candidate power semiconductor seems to be SGCT for CSC applications, it is also possible to use asymmetrical HV-IGBTs, reverse conducting HV-IGBTs, Asymmetric IGCTs in series with a matched Fast Recovery Diode for CSC based STATCOM.

HV-IGBTs are commercialized as standard modules with an integrated antiparallel freewheeling diode. Only a few manufacturer produce IGBTs in presspack housing, such as WESTCODE. WESTCODE also supplies asymmetrical IGBTs in presspack housing. In CSC applications, there is no need to use an extra antiparallel freewheeling diode across the asymmetrical power semiconductor switches (i.e., IGBT and IGCT) to carry the reverse-recovery current of seriesly connected fast recovery diode because asymmetrical power semiconductor switches can sustain current in reverse direction for short periods of time [74,77-79]. The key technical specifications of these candidate power semiconductor switches are given in Table 3.2 for the same operating conditions. For asymmetrical and reverse conducting IGBTs, series diodes are chosen as fast recovery type and compatible with the housing of the corresponding IGBT (i.e., for module IGBTs, module fast recovery diodes are used and for presspack IGBTs, presspack fast recovery diodes having the same pole-pitch diameter are used).

At first glance, the use of Asymmetric IGCT and fast recovery diode is found to be more advantageous against IGBT cases in terms of having: i) lower total forward voltage drop during conduction, ii) comparable switching energy loss, iii) presspack housing resulting in double side cooling and reliable explosion proof nature.

Table 3.2 Technical specification of the most candidate power semiconductor for CSC based STATCOM

Manurfacturer	Power Semiconductors	V_{DRM} (V)	I_{TGQM} (A)	V_F (V)	E_{on} (J)	E_{off} (J)	Erec (J)	$R_{th(j-h)}$ (K/kW)	T_{jmax} (°C)	di/dt (A/µsec)	$f_{switching}$ (Hz)
ABB	Asymmetric IGCT (5SHY35L4510)	4500	4000	1.4	0.3	2.57J		11.5	125°C	1000	< 1000
	Fast Recovery Diode (5SDF10H4520)	4500		1.9			3	13	140°C	-600	
WESTCODE	Asymmetric IGBT (T1200EA45E)	4500	2100	3.75	1.26	1.8J		9	125°C		
	Fast Recovery Diode (E1500VF450)	4500		2.15			5.4	13	150°C	-2000	
MITSUBISHI	Reverse Conducting IGBT (CM1200HC-66H)	3300	2400	3	1.25	1.36J		14.5	125°C		
	Fast Recovery Diode (RM1200HA-66S)	3300		2.7			0.5J	43	125°C	-2400	
DYNEX	Reverse Conducting IGBT (DIM800NSM33)	3300	1600	3	1.7	1.2J		20	150°C		
	Fast Recovery Diode (DFM800NXM33)	3300	1600	2.5			0.85	32	125°C	-3000	
ABB	Symmetric IGCT (5SHZ15H6000)	6000	1500	5.8	1.44	5.4J	3.87	16.5	140°C	+/-1300	< 750
MITSUBISHI	Symmetric IGCT (GCU15CA-130)	6500	1500	6	0.75	3J	2.7	14	125°C	+/-1000	< 1000

V_{DRM} – maximum repetitive voltage in forward direction
I_{TGQM} – maximum anode (collector) current that can be repetitively turned off
V_F – typical on-state voltage at 800A and 125°C
E_{on} – turn-on energy pulse, scaled for switching at 800A, 1800V
E_{off} – turn-off energy pulse, scaled for switching at 800A, 1800V
E_{rec} – reverse-recovery energy pulse, scaled for switching at 800A and specified -di/dt (for diode and symmetric devices)
$R_{th(j-h)}$ – steady-state thermal resistance from junction to heatsink
T_{jmax} – maximum operating junction temperature
di/dt – maximum permissible di/dt through the power semiconductor. (+ denotes for di/dt at turn-on, - denotes for di/dt at turn-off)
$f_{switching}$ – maximum switching frequency (limited by the gate driver unit for IGCTs, and maximum operating junction temperature of IGBT)

Inside the housing of commercially available SGCTs, there are discrete GCT (Gate Commutated Thyristor) and diode wafers, connected in series via molybdenum disk, and for the time being it has been found more feasible than symmetric processing of the silicon wafer due to the compromise between high switching losses and conduction losses[77,79]. In any way, since the natural air cooling has been specified for STATOM system in the previous section, the use of asymmetric IGCT and fast recovery diode meets this objective better than symmetric IGCTs. This is because total power dissipation of symmetric IGCTs will be transferred to the heatsink through a conduction area nearly half of that in case of asymmetric IGCT and fast recovery diode. Moreover, it is clear that while the switching losses are comparable, conduction losses for the case of asymmetric IGCT and fast recovery diode is much smaller than that for symmetric IGCTs.

As a result of these discussions, the use of asymmetric IGCT and fast recovery diode in CSC based STATCOM has been preferred. Having commercialized in 1997, IGCTs have found many applications such as in Medium Voltage Drives (MVD), Traction, Solid State Breakers (SSB), Flexible AC Transmission Systems (FACTS), Power Quality, Induction Heating [75, 81]. IGCT is composed of power semiconductor disc (GCT) part and gate drive unit. GCT, derived from basic GTO structure.

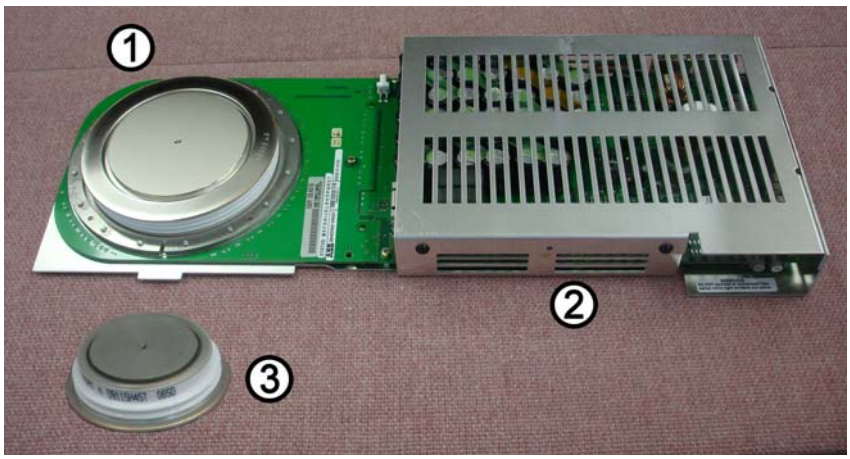
Integration of the gate driver unit through ultra low inductance to the gate of silicon wafer allows GCT to be turned off with unity gain via low voltage (20V) source so that IGCT can behave like IGBT at turn-off but like thyristor in conduction and at turn-on [80]. Unlike thyristors and GTOs, IGCT does not have dv/dt limit at turn-off, but it has di/dt limit at turn-on which is much more higher than thyristor. Due to homogenous current distribution throughout the switching, there is no need to restrict re-applied dv/dt, hence this permits snubberless operation of IGCTs [74]. Although IGBTs allow dv/dt control at turn-off and di/dt control at turn-on through its gate driver, these are pre-designed in manufacturing phase and standard for all IGCT types [80]. However, di/dt at turn-on can be controlled by external di/dt limiting reactor. Not only this significantly reduced turn-on losses but also provides the most pragmatic fault current limiting in the event of a short circuit

current. Furthermore, press-pack construction of the IGCT, combined with these di/dt limiting reactors, makes IGCT resistant to explosion, even when the device surge rating is exceed [75,80].

By carrier lifetime engineering of standard GCT silicon wafers, tailor made Asymmetric IGCT can be manufactured comprising low conduction losses for low switching losses. Among the available Asymmetric IGCTs, 5SHY35L4510 has been optimized conduction and switching losses [72,76]. Commercially available lowest voltage rating of Asymmetric IGCTs is 4500V, which meet the system voltage level specification of CSC based STATCOM. Therefore, 4500V/4000A rated 5SHY35L4510 has been chosen for CSC based STATCOM. Specified current rating of 4000A is the maximum peak current, I_{TGQM} that can be turned-off. If IGCT is operated at 500Hz, I_{TGQM} should be derated to 1500A due to power dissipation in the gate driver unit [70]. Derating curves of the chosen IGCT are given in Appendix D. Sample pictures of the chosen IGCT are as given in Fig.3.5.

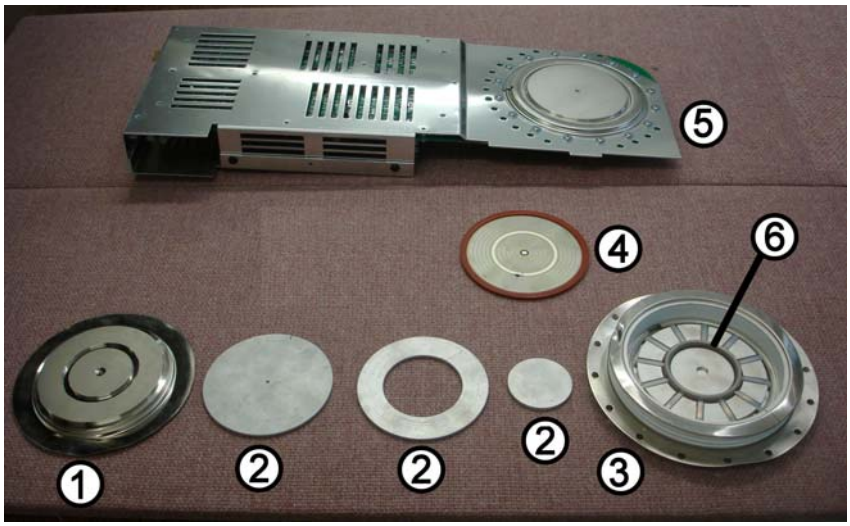
In perivious section, it is specified that STATCOM should comply with the harmonic limits even for the weakest power supply. This requires the use of appropriate PWM technique, which should be chosen according to type of the power semiconductor switches and power dissipation in the power semiconductors.

As discussed in Chapter 2, MSPWM and SVPWM provides continuous control of modulation index and phase angle control simultaneously at the expense of higher switching frequency. Otherwise, low order harmonics in the converter line current may cause resonance with the input filter. As specified in Table 3.2, IGCTs are optimized for switching frequencies below 1000Hz. According to I_{TGQM}, switching frequency of IGCTs is restricted by maximum allowable power dissipation in the gate driver unit. The switching frequency for the selected IGCT should be at most 750Hz in order to have dc-link current of 800A. In Chapter 2, it has been concluded that SHEM technique presents superior harmonic spectra for current line currents at switching frequencies less than 2kHz, therefore SHEM is chosen for the modulation of power semiconductors in CSC based STATCOM.



(a)

①-GCT part of IGCT (5SHY35L4510), ②- Gate Driver of IGCT,
③- Fast Recovery Reverse Blocking Diode (D911SH45)



(b)

①-Copper pole-piece of anode side of GCT , ②- Molybdenum discs, ③- Press pack Housing,
④- Silicon wafer of GCT ⑤- Complete IGCT (cathode side view),⑥- Gate Ring Electrode

(c)

cathode side of GCT silicon (on the left) and anode side of GCT (on the right)

Figure 3.5 Sample pictures of the chosen power semiconductors, 5SHY35L4510 and D911SH45

From (2.17), SHEM technique provides the elimination 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th} and 19^{th} harmonic components in the converter line current at a switching frequency of 750Hz. However, due to natural air cooling, switching frequency should be limited to 500Hz, which enables larger I_{TGQM} Then, 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic elimination in SHEM will be applied in this work. The generation of switching patterns has been explained in Chapter 2. Although modulation index control can be achieved in discrete steps, only phase angle control will be applied due to following reasons:

i. In applying IGCTs, minimum repetitive ON pulse duration (t_{on}), OFF pulse duration (t_{off}) and minimum switching period (t_{on}+ t_{off}) constraints must be satisfied [70,88]. For 5SHY35L3510, the manufacturer specifies the minimum ON and OFF pulse duration (t_{on}, t_{off}) as 10μsec. Minimum switching period (t_{on}+t_{off}) is specified as 60μsec. These values correspond to 0.2° and 1° at supply frequency of 50Hz. The durations of pulses in the switching pattern for 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic elimination are given in Table 3.3. Although all pulses seem to meet these constraints, it is wise to choose a safer value for minimum ON and OFF pulse durations as 1°. Then, applicable modulation index values become in the range between 0.35 and 0.95. This will introduce a non-linearity and complexity to the control system design.

ii. Since the electric excavators have Ward-Leonard systems powered by large synchronous and asynchronous motors, the variation in reactive power demand is much lower than supply frequency (50Hz) due to their large inertia. Therefore, using discrete control of modulation index in order to reduce the response time is unnecessary. Only phase angle control can easily provides required response time for the reactive power compensation of the electric excavators [59].

Table 3.3 Depending on the value of modulation index, durations of pulses in the switching pattern for 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic elimination

	Pulse Durations, degrees (1°≡55μsec at 50Hz)																			
Modulation index. M (pu)	Ton1	Toff1	Ton2	Toff2	Ton3	Toff3	Ton4	Toff4	Ton5	Toff5	Ton6	Toff6	Ton7	Toff7	Ton8	Toff8	Ton9	Toff9	Ton10	Toff10
0.05	0.3	19.6	0.4	19.3	0.6	19.2	60.6	19.2	0.6	19.3	0.4	19.6	0.3	60.9	19.0	1.0	19.0	1.0	19.0	60.9
0.10	0.3	19.3	0.7	18.7	1.3	18.3	61.5	18.3	1.3	18.7	0.7	19.3	0.3	61.7	18.0	2.0	18.0	2.0	18.0	61.7
0.15	0.4	19.2	1.0	17.7	1.9	17.6	62.2	17.6	1.9	17.7	1.0	19.2	0.4	62.6	17.2	2.9	16.7	2.9	17.2	62.6
0.20	0.5	18.7	1.3	17.2	2.6	16.7	63.0	16.7	2.6	17.2	1.3	18.7	0.5	63.5	16.2	3.9	15.9	3.9	16.2	63.5
0.25	0.7	18.4	1.7	16.6	3.2	15.9	63.6	15.9	3.2	16.6	1.7	18.4	0.7	64.3	15.2	4.9	14.8	4.9	15.2	64.3
0.30	0.7	18.1	2.1	16.0	3.8	15.0	64.4	15.0	3.8	16.0	2.1	18.1	0.7	65.1	14.3	5.8	13.9	5.8	14.3	65.1
0.35	1.0	17.7	2.4	15.3	4.4	14.2	65.0	14.2	4.4	15.3	2.4	17.7	1.0	65.9	13.3	6.8	12.9	6.8	13.3	65.9
0.40	1.1	17.3	2.8	14.7	5.0	13.4	65.7	13.4	5.0	14.7	2.8	17.3	1.1	66.8	12.3	7.8	12.0	7.8	12.3	66.8
0.45	1.2	17.0	3.2	14.0	5.6	12.6	66.4	12.6	5.6	14.0	3.2	17.0	1.2	67.6	11.4	8.8	10.9	8.8	11.4	67.6
0.50	1.2	16.7	3.5	13.4	6.2	11.7	67.2	11.7	6.2	13.4	3.5	16.7	1.2	68.4	10.5	9.7	10.0	9.7	10.5	68.4
0.55	1.4	16.3	3.9	12.8	6.8	10.9	67.9	10.9	6.8	12.8	3.9	16.3	1.4	69.3	9.5	10.6	9.0	10.6	9.5	69.3
0.60	1.6	15.9	4.3	12.3	7.3	10.1	68.5	10.1	7.3	12.3	4.3	15.9	1.6	70.1	8.6	11.6	8.0	11.6	8.6	70.1
0.65	1.6	15.6	4.6	11.6	8.0	9.3	69.2	9.3	8.0	11.6	4.6	15.6	1.6	70.8	7.6	12.6	7.0	12.6	7.6	70.8
0.70	1.8	15.3	5.0	11.1	8.5	8.5	69.9	8.5	8.5	11.1	5.0	15.3	1.8	71.6	6.7	13.6	6.0	13.6	6.7	71.6
0.75	1.9	14.9	5.4	10.5	9.1	7.7	70.5	7.7	9.1	10.5	5.4	14.9	1.9	72.4	5.8	14.6	5.0	14.6	5.8	72.4
0.80	2.0	14.5	5.9	9.9	9.7	6.9	71.1	6.9	9.7	9.9	5.9	14.5	2.0	73.1	4.9	15.6	4.0	15.6	4.9	73.1
0.85	2.2	14.1	6.3	9.4	10.2	6.1	71.6	6.1	10.2	9.4	6.3	14.1	2.2	73.8	3.9	16.5	3.1	16.5	3.9	73.8
0.90	2.4	13.8	6.7	8.9	10.8	5.3	72.1	5.3	10.8	8.9	6.7	13.8	2.4	74.5	2.9	17.6	2.1	17.6	2.9	74.5
0.95	2.5	13.5	7.2	8.3	11.5	4.5	72.4	4.5	11.5	8.3	7.2	13.5	2.5	74.9	2.0	18.7	1.1	18.7	2.0	74.9
1.00	2.7	13.3	7.7	7.9	12.2	3.8	72.5	3.8	12.2	7.9	7.7	13.3	2.7	75.2	1.1	19.9	0.1	19.9	1.1	75.2

not suitable recommended highly recommended

the one chosen

For phase angle control in SHEM, switching patterns are generated at a fixed value modulation index, M. An optimum value for modulation index should be chosen in view of the following constraints:

i. For safe operation of IGCTs chosen (5SHY35L4510), duration of each pulse should be larger than 10μsec. From Table 3.3, a safer value of $T_{on(min)}=T_{off(min)}=55\mu sec$ (corresponding to 1° for 50Hz system) has been chosen.

ii. For a pre-specified value of generated reactive power by CSC (2.7) and hence fundamental component of converter line current, as the modulation index is reduced, DC-link current, I_{dc} increases. Since the copper losses of DC-link reactor and conduction losses of power semiconductors increase with I_{dc}, it is therefore better to work at low I_{dc} values.

iii. For the simplicity in implementation of the control system, full control range of phase angle, θ should be as large as possible. This forces the use of low modulation index values.

The first constraint imposes an M value in the range from 0.8 to 0.9. This range is shaded with light gray in Table 3.3. The constraints on selection of M value are summarized are as illustrated in Fig. 3.6. Among these, M=0.8 is chosen for implementation by considering second and third constraints given above.

The diodes specified for fast switching GTO, GCT or IGBT applications, must feature not only low static and dynamic losses, but must also demonstrate exemplary recovery behaviour. In these applications, the critical need to minimise stray inductance between the switch and diode, encourages super-fast diode commutation.

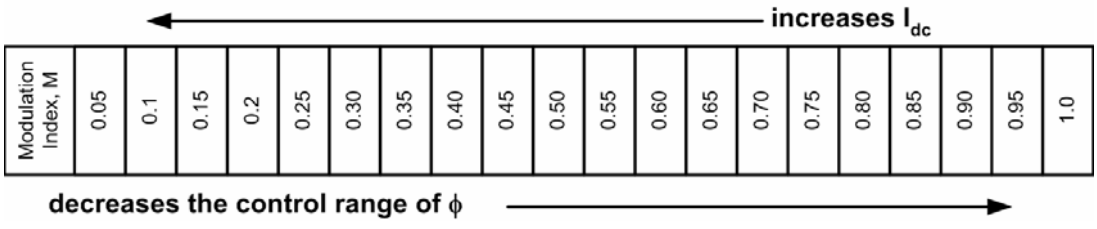


Figure 3.6 Constraints on selection of modulation index in SHEM for IGCT based CSC

Such commutation places a premium on low reverse peak current I_{RM}, and "soft recovery" performance [74]. Together with the growing trend to eliminate voltage snubbers on diodes, semiconductor manufacturers are developing new generation of diodes with different methods in order to achieve enhanced Safe Operating Areas (SOA) and controlled (soft) recovery at high di/dt and dv/dt levels. It has been reported that due to type of irradiation in manufacturing phase fast recovery diodes exhibit different reverse recovery characteristics depending on the application [82]. In Table 3.2, fast recovery diode, 5SDF10H4520 is chosen for connection in series with 5SHY35L4510. This is not only the best combination among the available fast recovery diodes in ABB product range but also provides the lowest conduction losses. However, critical *-di/dt* rating of this diode during reverse recovery phase is nearly half of the critical *di/dt* of chosen IGCT. As will be explained in the next section, *di/dt* value of IGCT is equal to *-di/dt* value of diode in magnitude during load commutation in CSC application. This restricts the value of *di/dt* during load commutation resulting a larger commutation reactor (i.e, *di/dt* limiting reactor). Larger commutation reactor presents a larger overvoltage across IGCT during self commutation and diode during load commutation. Another observation is that maximum reverse recovery current, I_{RM} of diode is mainly dependent on the *-di/dt* prior to reverse recovery phase. As the value of *-di/dt* increases, I_{RM} increases and presents a larger stress on the seriesly connected asymmetric IGCT in terms of its reverse current carrying capability. Moreover, not only overvoltage stress increases across the diode due to the commutation reactors but also reverse recovery losses increase. In view of these discussions, a compromise has been done on the selection of fast recovery diode and D911SH45 manufactured by EUPEC has been chosen for the final system in order to obtain lower reverse recovery losses and overvoltage during reverse recovery, higher *-di/dt* rating at the expense of higher conduction losses. Technical properties of D911SH45 and 5SDF10H4520 are compared in Table 3.4.

Using the input filter and dc-link reactor designed in the following sections, the simulated voltage and current waveforms of theoretical power semiconductor switches in CSC for 5th, 7h, 11th, 13th harmonic elimination with M=0.8, are given in Fig.3.7 and 3.8. Since dc-link current for 500kVAr inductive case is nearly two

times that of 500kVAr capacitive case, the power dissipation of power semiconductors is greater in 500kVAr inductive case. Therefore, using simulation results in Fig.3.7 and the values obtained from the datasheets, the most suitable candidate power semiconductors for CSC based STATCOM are compared in terms of their losses at 500kVAr inductive reactive power in Table 3.5. The method used for the calculation of power losses in each power semiconductor is explained in Appendix E.

Table 3.4 Comparision of the candidate fast recovery diodes which can be used in series with IGCT (5SHY35L4510) in CSC based STATCOM

Power Semiconductors	**V_{RRM} (V)**	**$I_{T(AV)M}$ (A)**	**V_F (V)**	**I_{RM} (A)**	**E_{rec} (J)**	**$R_{th(j-h)}$ (K/kW)**	**T_{jmax} (°C)**	**di/dt (A/μsec)**
ABB 5SDF10H4520	4500	1440	1.9	1250	3	13	140	-600
EUPEC D911SH45	4500	890	3	800	1.7	13	140	-1300

Table 3.5 Comparison of candidate power semiconductors for use in CSC based STATCOM

		5SHY35L4510 IGCT + D911SH45 Diode	CM1200HC-66H IGBT + RM1200HA-66S Diode	GCU15CA-130 SGCT*
Conduction Loss	Switch	390 W	707 W	1366 W
	Diode	732 W	610 W	
Turn-on Loss		26 W	172 W	34 W
Turn-off Loss		176 W	90 W	185 W
Reverse Recovery Loss		222 W	60 W	232 W
TOTAL LOSS		**1546 W**	**1639 W**	**1817 W**

* It is no longer commercially available

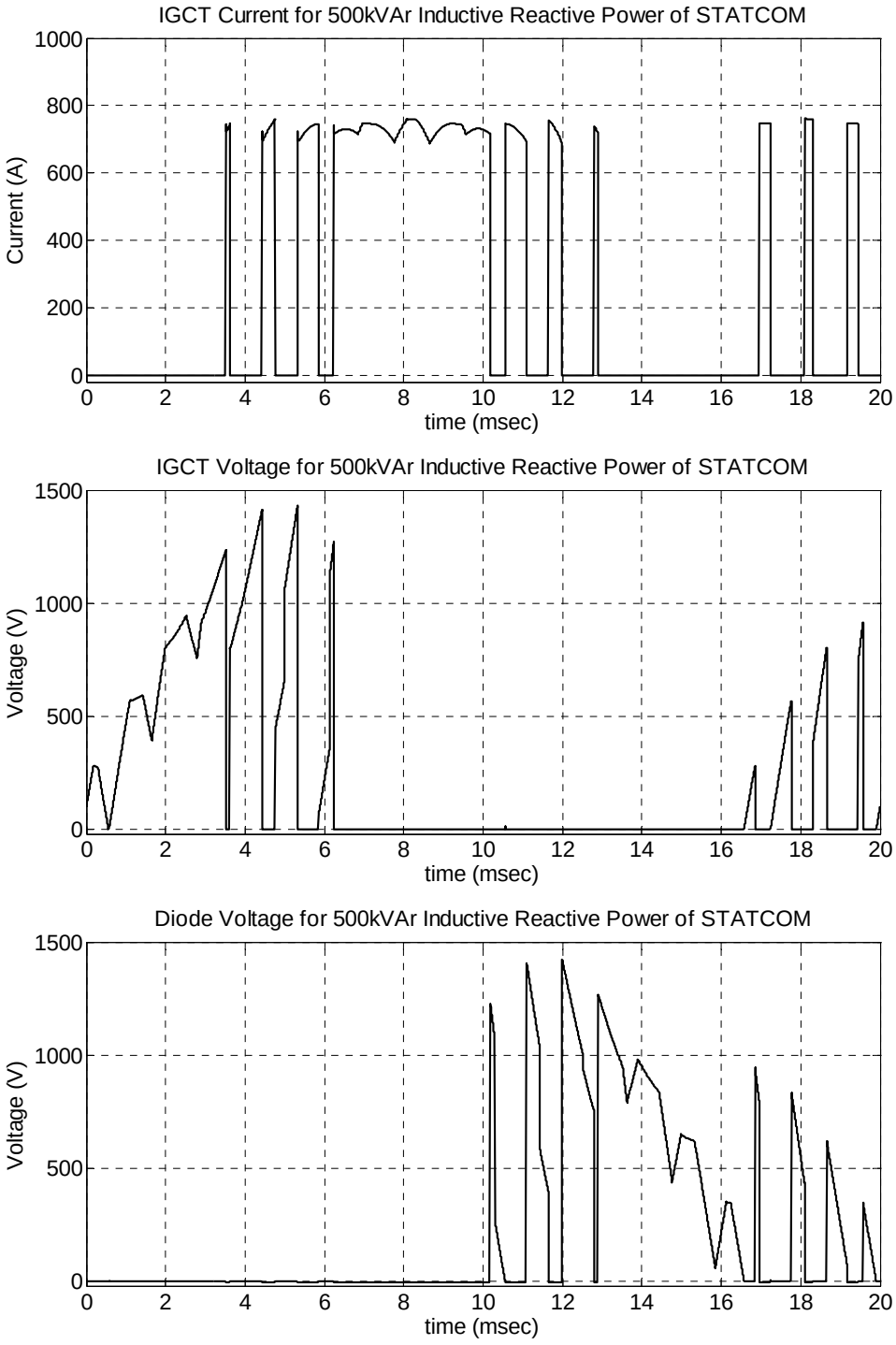


Figure 3.7 Theoretical voltage and current waveforms of IGCT and Diode for 500kVAr inductive reactive power generation of CSC based STATCOM(PSCAD/EMTDC)

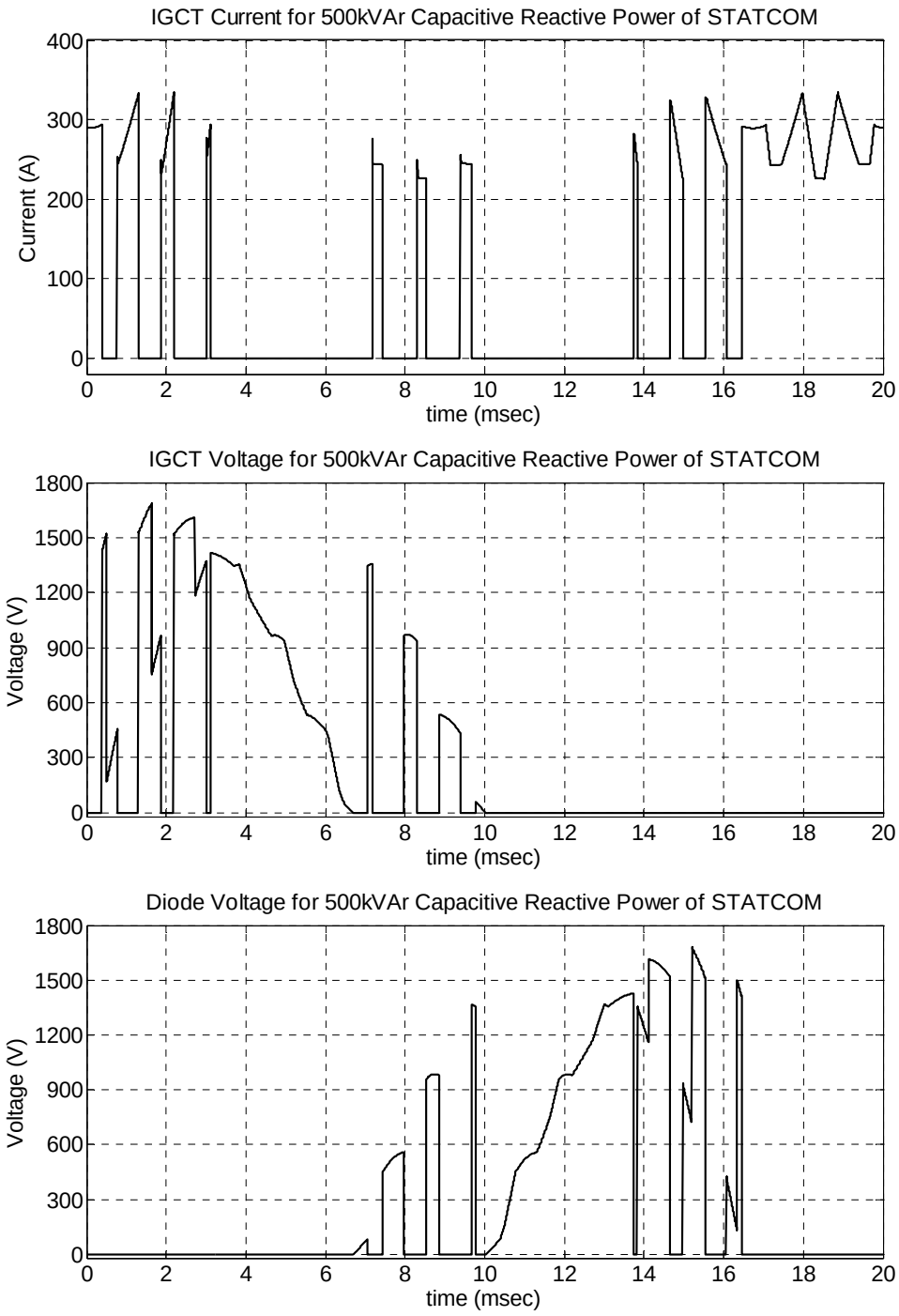


Figure 3.8 Theoretical voltage and current waveforms of IGCT and Diode for 500kVAr capacitive reactive power generation of CSC based STATCOM (PSCAD/EMTDC)

The use of asymmetric IGCT (5SHY35L4510) and fast recovery diode (D911SH45) has been compared with HV-IGBT (CM1200HC-66H) and fast recovery diode (RM1200HA-66S) for different commutation types in CSC-STATCOM (described in Chapter 2) by using test circuit in Fig.3.9. The switching waveforms of power semiconductors were recorded for three different current magnitude (200A, 600A, 1200A) at 600V in each commutation type. Since the switching characteristic of DUT2 during load turn-off were aimed to be observed, single fast recovery diode (without IGCT or HV-IGBT) in DUT2 was used. The commutation inductance which represents the overall stray inductances in commutation path is taken as 200nH for IGBT case and 2μH for IGCT case. The switching waveforms of power semiconductors were taken by the high voltage differential probe P5210 (for voltage) and Rogowski current transducer (for current), which are described in Chapter 4. These waveforms were recorded at a sampling rate of 25MS/sec with the use of Tektronix TDS5054 digital phosphor oscilloscope.

The switching waveforms of IGCT and HV-IGBT at device turn-on are as given in Fig.3.10. It is clear that IGCT has very low turn-on losses since voltage across IGCT collopses immeadiately while its current increases with relatively low di/dt (indicated as $\Delta I_1/\Delta t_1$ in Fig.3.10). On the other hand, HV-IGBT experiences the relatively high turn-on losses since the decrease in voltage and increase in current occur simultaneously. The voltage overhoot (indicated as ΔV in Fig.3.10b) in voltage waveforms of HV-IGBT during turn-on are due to stray inductance between the connection points of high voltage probe since reverse-recovery current of fast recovery diode (DUT2) has high di/dt and flows through HV-IGBT (indicated as ΔI in Fig.3.10). The overshoot in current waveforms of both IGCT and HV-IGBT are due to this reverse-recovery current. However, fast recovery diode for IGCT applications has softer reverse-recovery characteristics (lower di/dt or $\Delta I/\Delta t$ in reverse-recovery) since di/dt of DUT1 (indicated as $\Delta I_1/\Delta t_1$) is limited by the use of relatively higher L_{comm} in circuit.

Device turn-off mechanism can be observed from the switching waveforms obtained for IGCT and HV-IGBT in Fig.3.11. The turn-off of IGCT current is relatively longer than that of IGBT, resulting in lower -di/dt, hence higher turn-off

losses in IGCT case. It should also be noted that voltage overshoot (indicated as ΔV in Fig.3.11) in both IGCT and HV-IGBT although L_{comm} is ten times higher in value for IGCT case. This shows the ease in power stage assembly for IGCT applications where minimization of stray inductances in power stage is not as strict as in IGBT applications.

In order to observe the electrical stress on diode load turn-off of reverse blocking fast recovery diode, the switching waveforms of D911SH45 and RM1200HA-66S are compared in Fig.3.12 for IGCT and IGBT cases. Reverse-recovery of diode depends not only on the magnitude of forward current before turn-off but also on di/dt (indicated as $\Delta I/\Delta t$ in Fig.3.12). Since the magnitude of forward currents for IGBT and IGCT cases are the same, the reverse recovery of diodes are mainly dictated by $\Delta I/\Delta t$, which is higher in IGBT case due to the low commutation inductance (L_{comm}). This results in higher maximum reverse recovery current (I_{RM}).

Also for IGCT case, 5SDF10H4520 is replaced with D911SH45 in order to illustrate the use of optimized diode in series with IGCT for CSC applications. For the same magnitude of forward current before load turn-off and $\Delta I/\Delta t$ during load turn-off, I_{RM} for 5SDF10H4520 is higher than I_{RM} of D911SH45. Moreover, D911SH45 has more softer reverse-recovery characteristic due to lower $\Delta I_1/\Delta t_1$. This results in lower voltage overshoot across diode, as shown in Fig.3.12.

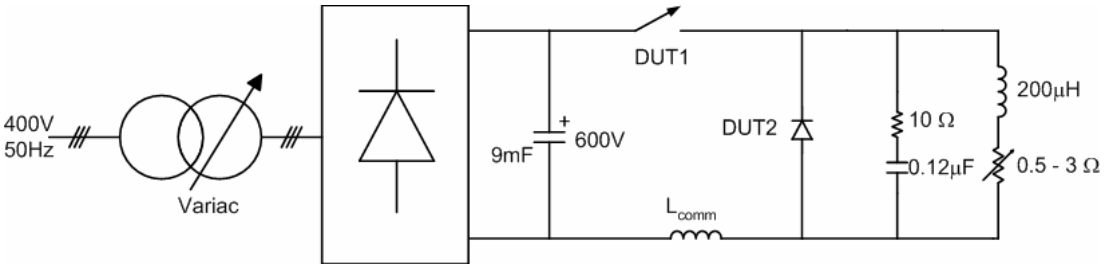
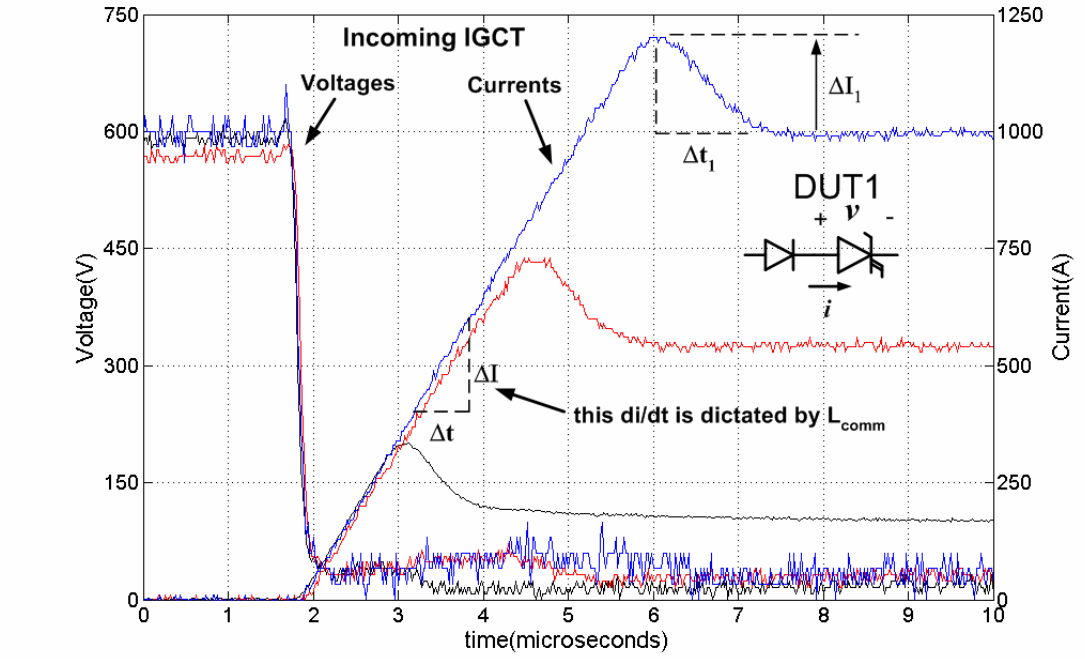
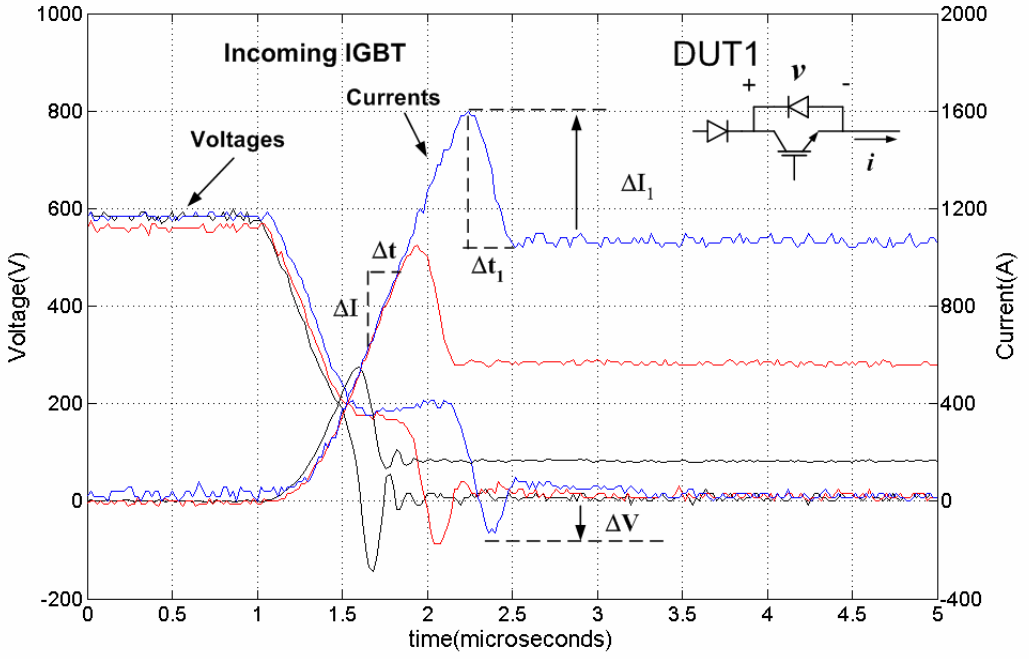


Figure 3.9 Test circuit for obtaining the switching characteristics of power semiconductors

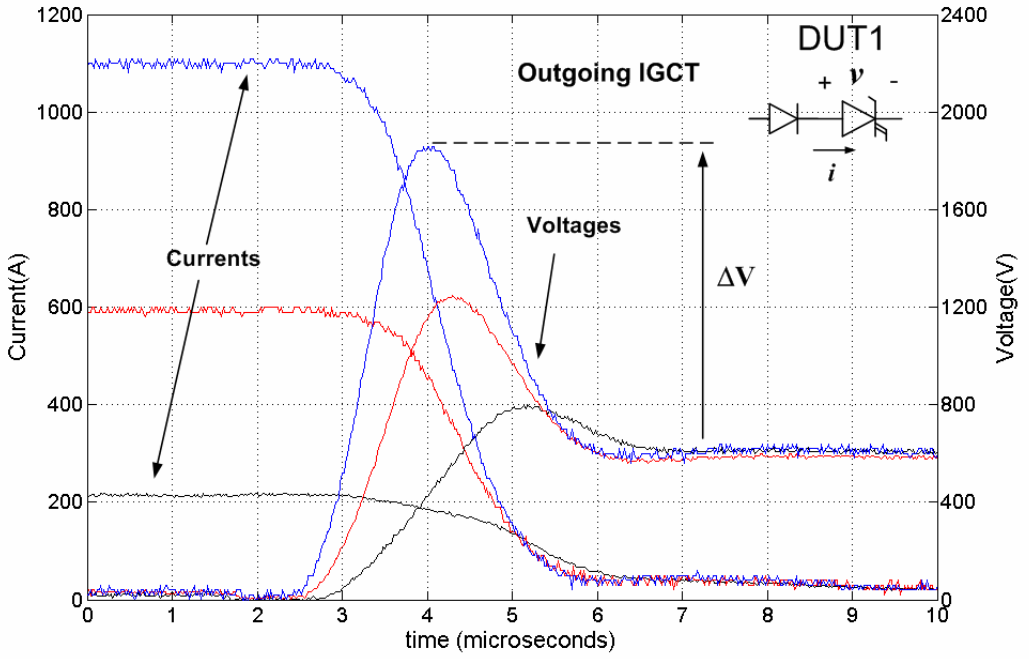


(a)

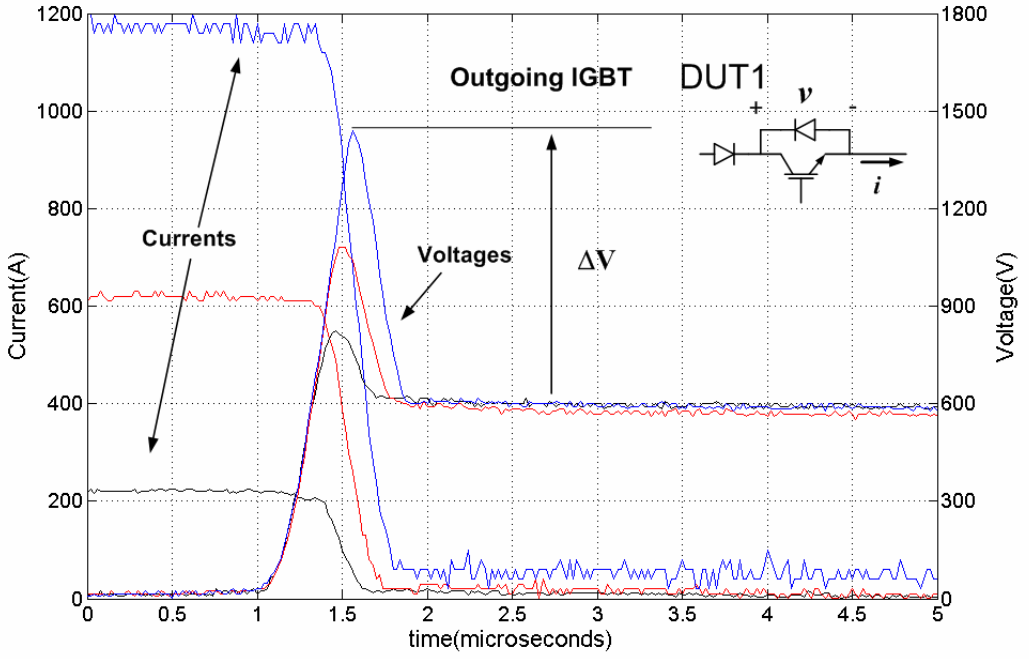


(b)

Figure 3.10 Device turn-on switching waveforms (a) IGCT (5SHY35L4510) voltage and current waveforms, (b) HV-IGBT (CM1200HC-66H) voltage and current waveforms at 600V, 1000A (blue lines), 600V,500A (red lines), 600V, 150A (black lines) (sampling rate: 50MS/sec)

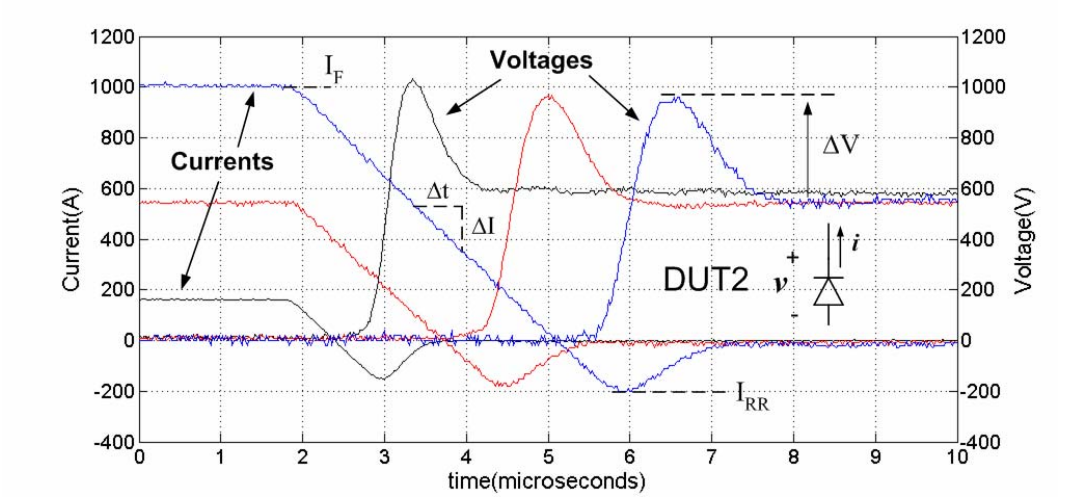


(a)

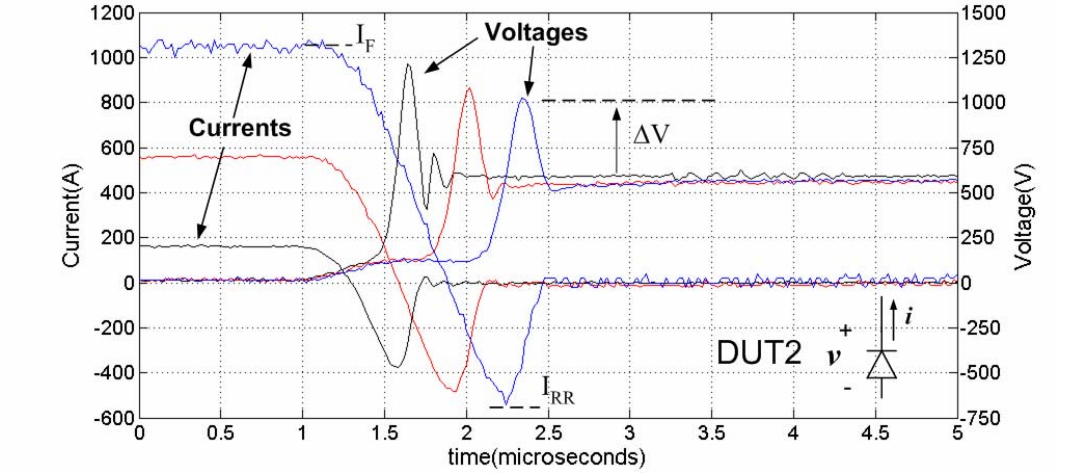


(b)

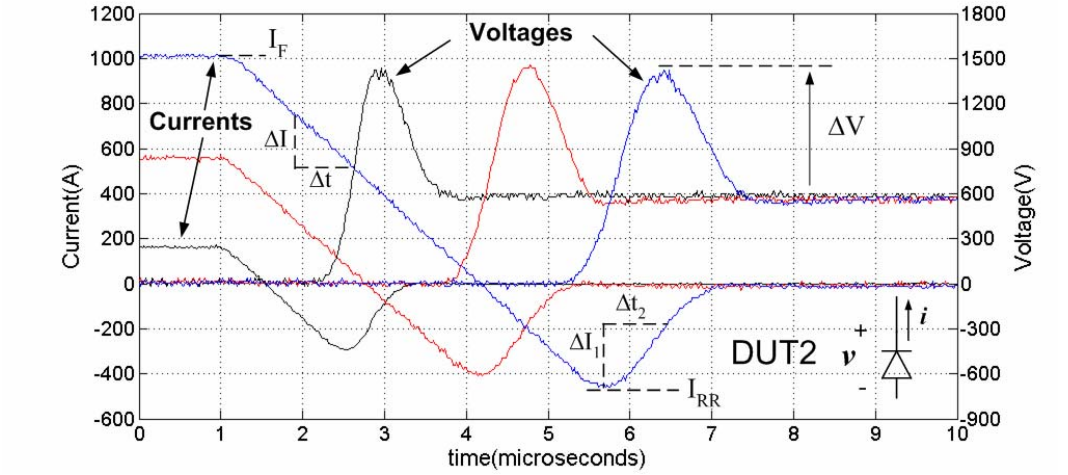
Figure 3.11 Forced turn-off switching waveforms (a) IGCT /5SHY35L4510) voltage and current waveforms (b) HV-IGBT (CM1200HC-66H) voltage and current waveforms at 600V, 1200A (blue lines), 600V,600A (red lines), 600V, 200A (black lines) (sampling rate: 50MS/sec)



(a)



(b)



(c)

Figure 3.12 Load turn-off switching waveforms (a) voltage and current waveforms of D911SH45 (b) voltage and current waveforms of RM1200HA-66S (c) voltage and current waveforms of 5SDF10H4520 at 600V, 1000A (blue lines), 600V,600A (red lines), 600V, 200A (black lines) (sampling rate: 50MS/sec)

3.4 Input Filter Design

As given in Fig.2.14c, converter line currents contain significant 17th, 19th, 23rd and higher order harmonics for the chosen in SHEM technique which eliminates 5th, 7th, 11th, 13th harmonics. These significant harmonics must be filtered out in order to meet the specified individual current harmonic components and TDD values given in Section 3.2. This is achieved by the use of a low pass input filter as shown in Fig.2.1.

The single line diagram of input filter, referred to 1kV-side is given in Fig.3.13. The leakage inductance and copper losses of coupling transformer are also included in Fig.3.13. Using the single line diagram, the filter parameters are chosen in view following constraint:

i. Filtering perfomance : Since it is a second order filter theoretical frequency response of input filter from converter line current i_R to supply current i_{SR} is as given in Fig.3.14. The undamped resonance frequency, f_c is expressed in (3.1). It should be placed between the supply frequency and the most significant harmonic components in the converter line current. It should be set to a value as close as the supply frequency to achieve better filtering perfomance so that these significant high order harmonic components are considerably attenuated.

$$f_c = \frac{1}{2\pi\sqrt{(L_{tr} + L)3C}} \tag{3.1}$$

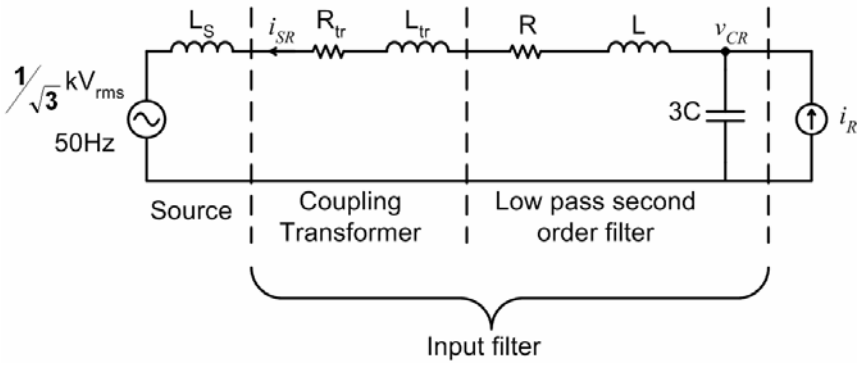


Figure 3.13 Single line diagram of the input filter

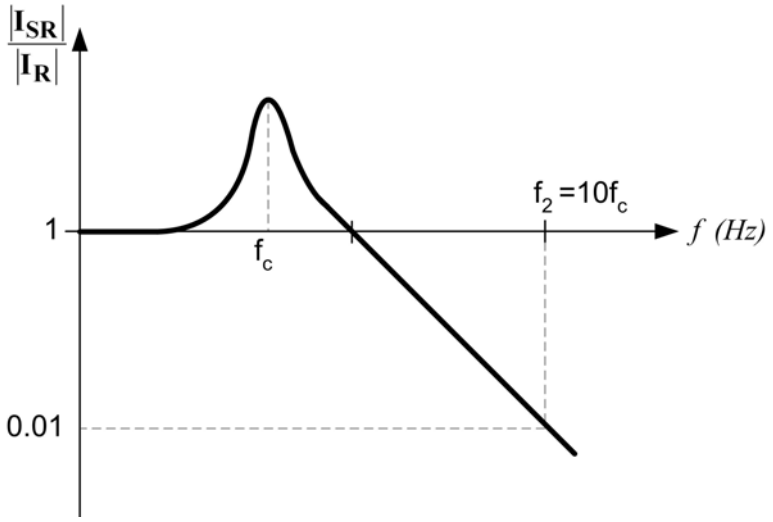


Figure 3.14 Theoretical frequency response of the input filter

ii. Size of the Filter Capacitor: Filter size at a certain corner frequency determines the total capacitive VAr produced by the input filter at rated voltage and frequency, as given in (3.2). In (3.2), f_1 denotes supply frequency and V is the rated line to line voltage in rms volts. It should be made as small as possible in order to achieve nearly symmetric VAr generation of CSC. However, this can be utilized for optimizing converter losses in some applications. For example, for the compensation of inductive loads filter size may not be a concern, but for capacitive loads it should be minimized in order to minimize converter losses.

$$Q = 3V^2(2\pi f_1)C \tag{3.2}$$

iii. Voltage regulation: Due to presence of transformer leakage inductance and the filter inductance, voltage at the input terminals of the converter V_{CR} varies with VAr generation of STATCOM, as discussed in Chapter 2.3. Voltage regulation can then be expressed as in (3.3).

$$\text{Voltage Regulation} = \frac{V_{CR,\max} - V_{CR,\min}}{V} \tag{3.3}$$

Especially, V_{CR} increases much beyond rated system voltage when STATCOM is generating capacitive reactive power. This is very crucial in choosing voltage ratings of filter capacitors and power semiconductors. The line to line voltage in rms, V_{CR} at the input terminals of CSC can be expressed roughly as (3.4), where Q is positive for capacitve reactive power and V is the source line-to-line voltage in rms. As illustrated in (3.4), transformer leakage inductance and filter inductance should be chosen in order to present any problem for the filter capacitors and power semiconductors in terms of their voltage ratings.

$$V_{CR} = V \pm \frac{Q}{V}(2\pi f_1)(L_{tr} + L) \tag{3.4}$$

iv. Transient response: Transient response of input filter determines the overall transient response of CSC based STATCOM [63]. Since the transfer function of input filter has a standard form of second order underdamped systems, some important parameters characterizing the transient response of the system can be defined as given in (3.5) and (3.6). As can be understood from (3.6), decreasing resonance frequency increases the settling time of the reactive power generated by STATCOM.

$$\text{damping factor, } \varsigma = \frac{R}{2}\sqrt{\frac{\mathrm{C}}{\mathrm{L} + \mathrm{L_{tr}}}} \tag{3.5}$$

$$\text{settling time, } t_s = \frac{4}{\varsigma(2\pi f_c)} \tag{3.6}$$

v. Damping factor: Damping factor, which has already defined in (3.5) determines the amplification factor of the input filter in its frequency response at resonance frequency as shown in Fig.3.14. Since harmonic elimination in SHEM technique can not be totally possible due to applied optimization techniques for finding the independent angles, power semiconductors for their non-ideal switching behaviour, etc, there may be harmonics around the resonance frequency of the input filter. Even though the magnitudes of these harmonics are less than

0.5%, they can be amplified by a factor of 60-100 resulting in non-compliance of the harmonic limits. Therefore, proper damping should be applied at the expense of longer settling time and higher losses in the overall STATCOM system performance.

In view of these constraints, filter capacitor and inductor has been decided to be 240μF/phase-delta and 700μH/phase-wye, respectively. Since the CSC based STATCOM has been rated to 500kVAr, a 31.5/1kV, 800kVA coupling transformer are designed and manufactured among standard ratings. Standard power transformers at this power rating have nearly 5% voltage drop value as U_k. Then, leakage inductance of the transformer, referred to 1kV side can be found as in (3.7). As the copper loss of typical power transformer is nearly 1% of its power rating, equivalent resistance of the transformer can be calculated from (3.8).

$$L_{tr} = \frac{V^2\ U_k}{S\ (2\pi f_1)} = \frac{(1kV)^2\ 0.05}{(0.8kVA)(2\pi 50)} = 200\mu H \qquad (3.7)$$

$$R_{tr} = \frac{V^2\ 0.01}{S} = \frac{(1kV)^2\ 0.01}{(0.8kVA)} = 12.5m\Omega \qquad (3.8)$$

With the selected parameters, the resonance frequency of the input filter is found as 197Hz. This resonance frequency has been especially chosen because it is below the characteristic harmonics of the converter (5^{th}, 7^{th}) and provides sufficient attenuation of higher order harmonics in the converter line current. Further reduction of resonance frequency has not been prefferred due to the larger filter size. Having nearly symmetrical reactive power generation of converter and equal converter losses filter size, defined above, becomes 225kVAr capacitive at 1kV. At the input terminals of the converter, the voltage regulation which is defined as the percentage of change in voltage from full capacitive to full inductive reactive power generation of STATCOM with respect to rated system voltage has been found as 28%.

Choosing internal resistance of filter inductor as 5% of its supply frequency impedance (R=10mΩ), the frequency response of the designed input filter is given in Fig.3.15. The attenuation and amplification factors at significant frequencies are also indicated in Fig.3.15. In order to damp the filter characteristics at resonance

frequency an extra resistor should be connected in series to filter inductance. For an amplification factor of nearly 10, this extra resistor should be 90mΩ. The frequency response of the input filter with an extra resistor of 90mΩ is also given in Fig.3.15. For 500kVAr STATCOM system, line current at 1kV is 290A rms. These extra resistors will introduce 22kW extra power dissipation at the expense of adequate damping.

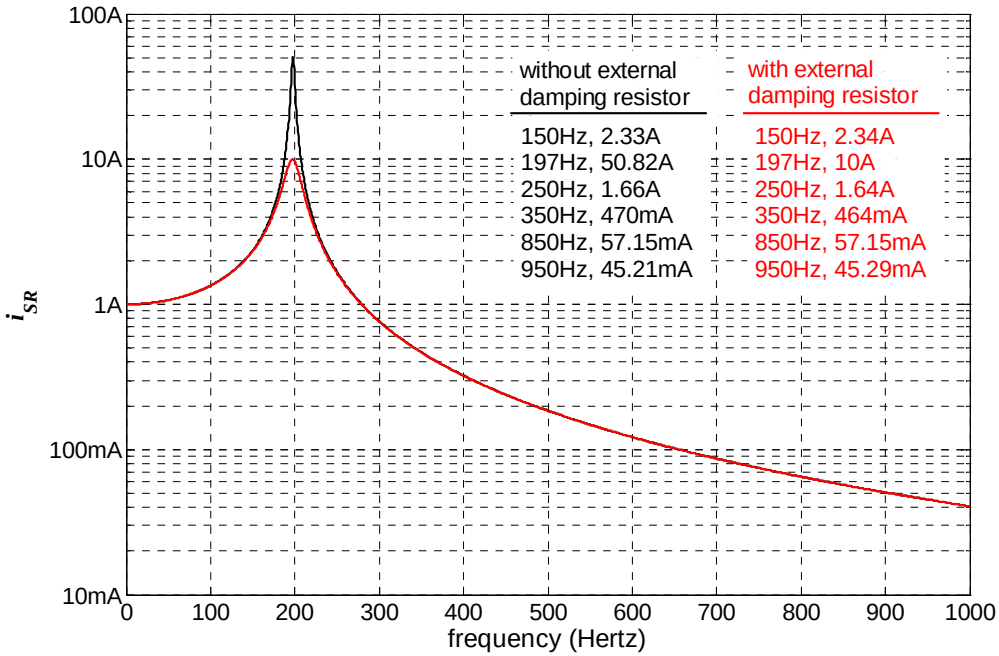
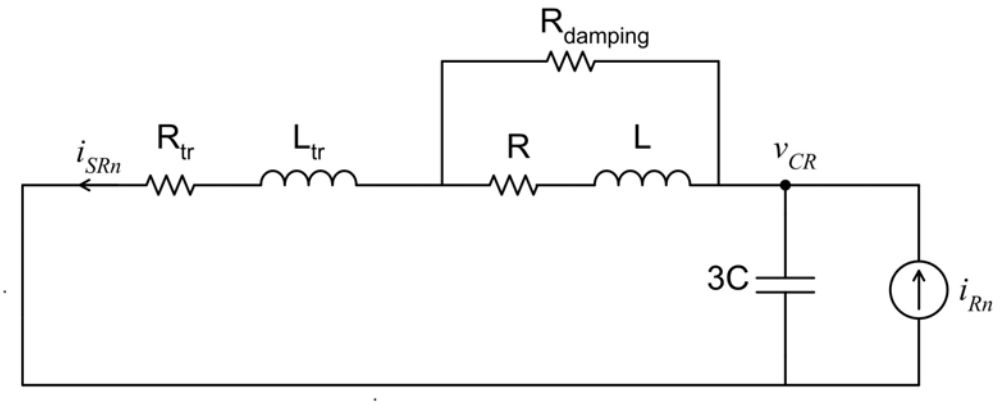


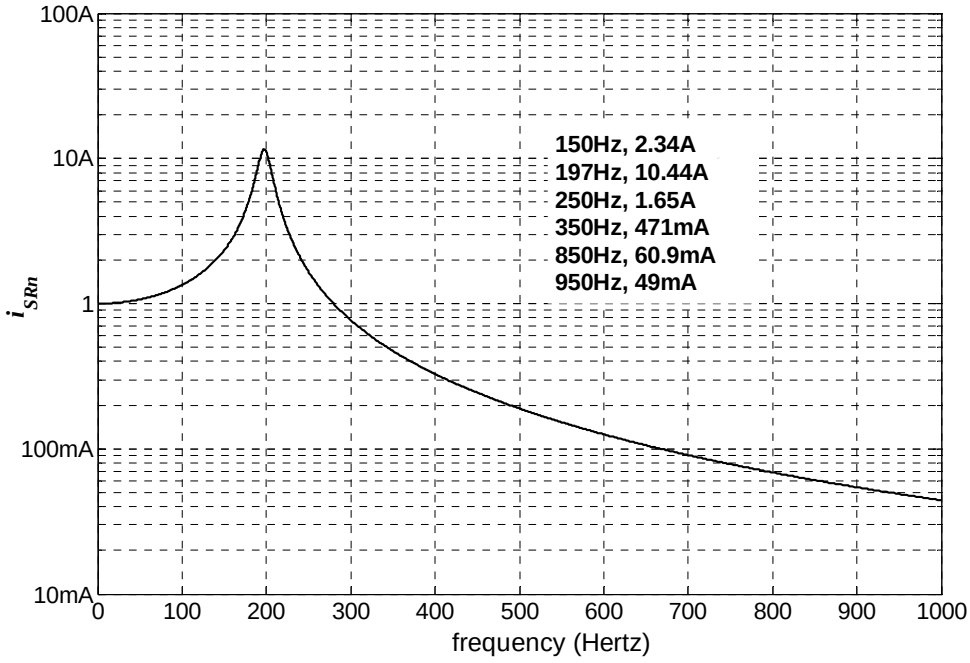
Figure 3.15 Frequency response of input filter having the selected reactor and capacitor with / without damping (Pspice)

Instead of this lossy passive damping approach, same damping factor can be achieved by connecting the extra resistors in parallel with the filter inductors as shown in Fig.3.16a. [29,53,64]. Since its transfer function has three poles, it is not possible to find simple expressions for characterization of its transient response. However, its undamped resonance frequency is same as one given in (3.1). By computer simulations, damping resistor is found to be 10Ω in order to achieve an

amplification factor of nearly 10. The resultant frequency response of the filter is given in Fig.3.16b. By computer simulations, it has been found that the total power dissipation in this damping resistor is only 2kW at worst case for 500kVAr STATCOM.



(a)



(b)

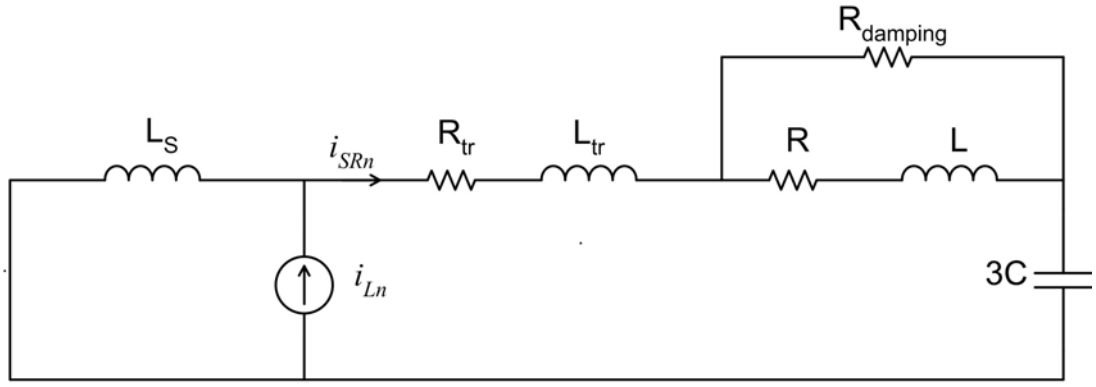
Figure 3.16. (a) Equivalent circuit of designed third-order input filter with passive damping (R_{tr}=12mΩ, L_{tr}=200μH, R=10mΩ, L=700μH, $R_{damping}$=10Ω), (b) frequency response of designed input filter in (a) (PSpice)

The frequency response in Fig.3.16b is obtained by injecting harmonic currents, which have 1A in magnitude at various frequencies from CSC side. For harmonics injected from load side, the frequency response of the input filter can be obtained as in Fig.3.17a by using the equivalent circuit in Fig.3.17b. The supply line impedance in Fig.3.12 can be calculated from the short circuit MVA of the power supply, given in Fig.3.4. It is evident that the designed input filter does not cause any resonance problems with the supply side harmonics.

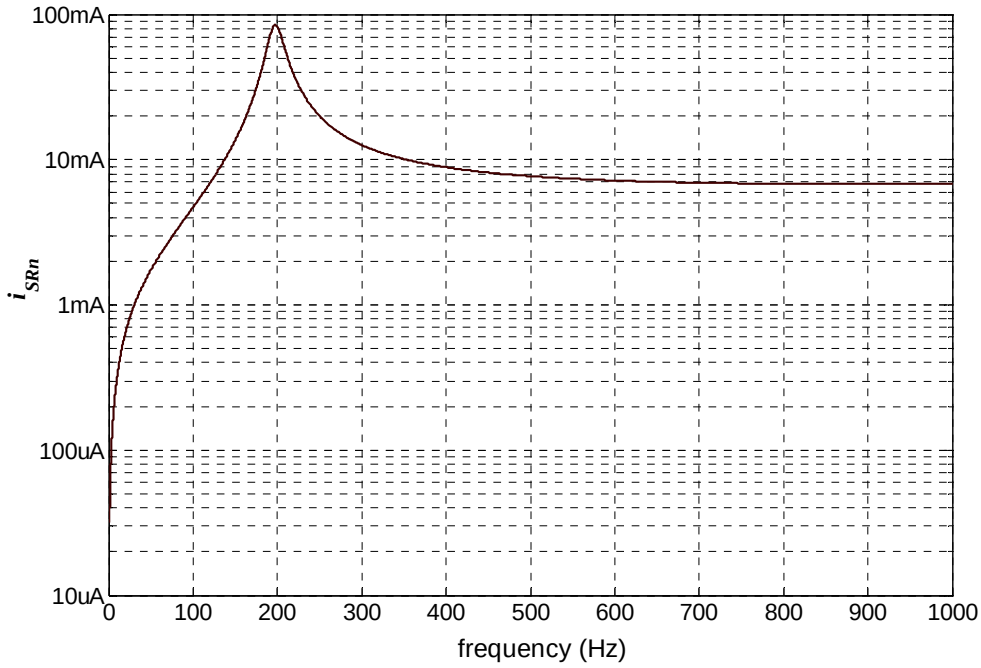
The circuit diagram of the designed input filter for CSC based STATCOM is given in Fig.3.18. The filter capacitors should be power electronics type. Capacitors for power electronics are used in applications, where extremely non-sinusoidals and pulsed currents are present [89]. Due to their low self inductance, their repetitive peak current rating is almost 100 times the rms current rating. In CSC based STATCOM, not only these capacitors are used for filtering higher order harmonics in the converter line current, but also provide a commutation path for the currents of power semiconductors in the converter. Among available power electronics capacitors, input filter capacitor has been chosen as general purpose AC power electronics capacitor which has high maximum rms and repetitive peak current ratings. The input filter capacitors are arranged in delta connected capacitor bank where the capacitance of 240μF per phase is formed by parallel connection of four 60μF capacitor units as shown in Fig.3.18.

The filter reactors are chosen as air core single phase reactor because air core reactors are especially used in outdoor applications and do not need any forced air cooling, therefore they are more robust and reliable as compared to the iron core reactors. They are arranged as single phase reactors, as shown in Fig.3.18. This has been chosen in order to avoid magnetic coupling between the phases. However, it is also possible to use them as magnetically coupled units such as mounting them top-to-top.

Damping resistors shown in Fig.3.18 are selected as each rated to 10Ω for outdoor use.



(a)



(b)

Figure 3.17. (a) Equivalent circuit for frequency response of input filter to the load harmonics (b) The frequency response of input filter to the load harmonics (Pspice)

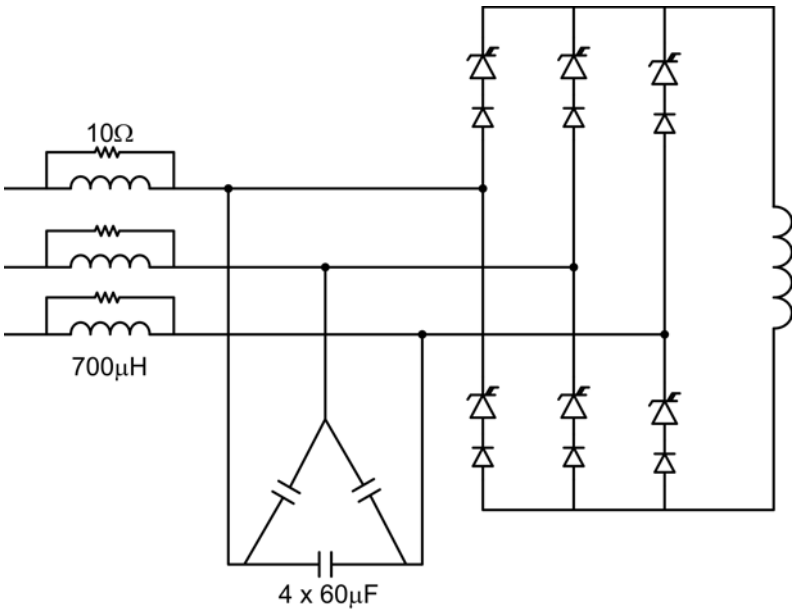


Figure 3.18 The circuit diagram of the designed input filter for CSC based STATCOM

3.5 Design of DC-Link Reactor

The dc-link reactor as a magnetic energy storage element of CSC based STATCOM should be chosen in view of transient response, harmonic distortion in converter line currents and power loss.

As mentioned in Chapter 2, after fixing modulation index, reactive power of CSC can be controlled by controlling dc-link current by phase shift angle. Therefore, faster reactive power control requires faster change in dc-link current. The equivalent circuit of CSC based STATCOM in dq stationary reference frame has been given for transient state in Fig.2.29. The dc-link current can be expressed as in (3.9). For a step change in phase shift angle, ϕ, dc-link current i_{dc} changes with a time constant of L_{dc}/R_{dc}. Although time required for setting dc-link current to a certain value is dependent on the value of dc-link reactor, it can be reduced by increasing shift angle ϕ. However, in some applications, where the control range of phase shift angle is limited, the value of dc-link reactor dictates the speed of

response for dc-link current control, hence reactive power control of CSC based STATCOM. That's why dc-link reactor should be made as small as possible for faster transient response.

$$\sqrt{\frac{3}{2}}M\left(v_{cd}\sin\theta + v_{cq}\cos\theta\right) = L_{dc}\frac{di_{dc}}{dt} + R_{dc}\,i_{dc} \tag{3.9}$$

From the viewpoint of distortion in converter line current waveforms at the input of CSC, better approximation of dc link current to a level current improves the TDD of the input current waveform. In order to minimize the peak-to-ripple in dc-link current (ΔI_{dc}), switching frequency (f_s) and/or inductance of dc-link reactor (L_{dc}) should be increased, as given in (3.10).

$$\Delta I_{dc} \propto \frac{V}{f_s\ L_{dc}} \tag{3.10}$$

Once the system voltage (V) and switching frequency are chosen, the inductance of dc-link reactor determines ΔI_{dc}. The general approach is to make the ΔI_{dc} is 10% of its rated mean value (I_{dc}) [61,63]. The expressions given in literature [61,63] for (3.10) results in unnecessarily large dc-link reactor. A large dc-link reactor means a huge and expensive system component. Therefore, the effect of inductance of dc reactor on the TDD should be investigated by the simulation. The variation of TDD vith the inductance of dc-link reactor for the chosen modulation technique in Section 3.3 is given in Fig.3.19. It is found that TDD increases as the inductance decreases. Since TDD limit is in the range from 5% to 15% for typical MV busses, L_{dc} value which is 1mH seems to be quite satisfactory. Then, this constraint should be considered for capacitive operating region of CSC based STATCOM.. Therefore, it is better to decide on the value of dc-link reactor from simulation results.

Internal resistance, R_{dc}, of the dc-link reactor should be kept at an implementable minimum value, thus reducing dc reactor losses. Operating the dc-link reactor at a higher voltage for the same system size could make a more significant contribution to reactor loss reduction problem, than R_{dc} reduction. Meanwhile, superconducting energy storage element (SMES) could also make a contribution to loss reduction at the expense of its much higher costs.

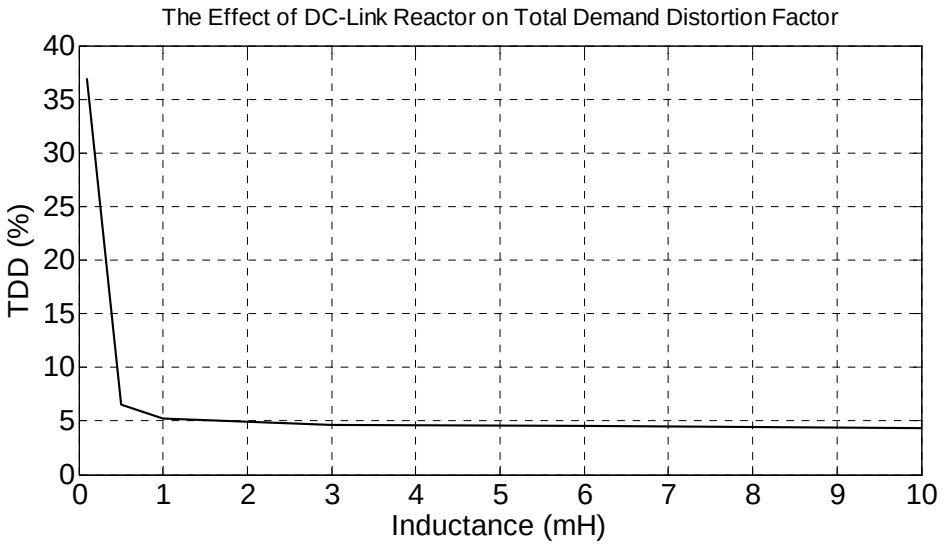


Figure 3.19 The variation of Total Demand Distortion factor with inductance of DC-link reactor in CSC based STATCOM at 500kVAr capacitive reactive power (PSCAD/EMTDC)

In view of above considerations and specification of CSC based STATCOM given so far, inductance, L_{dc} is found to be 3mH. In an air core reactor, the only power loss is due to the copper losses. Since air core reactor has the number of turns higher than that of an iron core reactor due its lower permeability, This results in higher losses than that of iron core reactor. Although from the view point of dc-link reactor losses iron-core reactor is better than air-core reactor, dc-link reactor has been chosen as air core reactor, which can be used at outdoor with natural air cooling.

3.6 Design of Power Stage Layout

The design of a power stage layout in CSC based STATCOM are subject to following constraints:

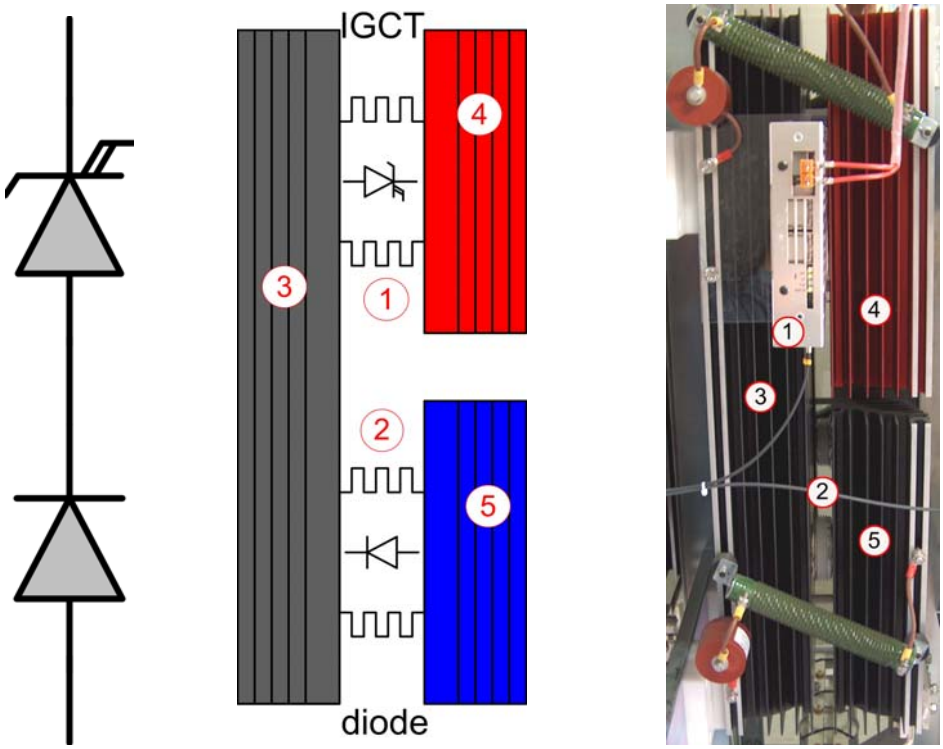
i. The type of semiconductor switches chosen and their switching characteristics during the fundamental commutation types of CSC

ii. Semiconductor cooling methods chosen, i.e., natural air cooling, forced air cooling or water cooling

As demonstrated in Section 3.3, the switching speed of IGBTs is faster than IGCTs. This results in high di/dt during switching transients in IGBT applications. Therefore, stray inductances in the power stage layout should be as small as possible (~ 100nH) in order to avoid excessive over-voltages across power semiconductors. However, in IGCT applications, this is not so strict due to slower switching speeds. Therefore, it is relatively easy to design the power stage layout of IGCT based CSC since an acceptable unclamped (i.e, without clamping snubber) stray inductance in the power stage is between 200 and 600nH. However, one can double this stray inductance at the expense of only 30% overshoot in voltage waveform of IGCT during turn-off and turn-off losses also increases by 30%. This feature should not encourage “sloppy wiring”, but it does facilitate the design and construction of large systems and highlights the IGCT’s robustness and user-friendliness. [80]

3.6.1 Power Stage of Current Source Converter

Fig. 3.20 shows the assembly of each power semiconductor switch. Each switch consists of an asymmetric IGCT and a reverse blocking diode. Thermal specifications of power switch assembly are as given in Table 3.6. Steady-state thermal model of each assembly is as given in Fig.3.21. By solving the algebraic equations corresponding to thermal equivalent circuit for thermal resistances of natural air cooled heatsinks, the maximum operating values of virtual junction temperature, T_{vj} are found to be 120°C for IGCT and revere blocking diode. It is seen that T_{vj} of IGCT is not in the safety limit. Then, air ventilation of the container has been utilized to provide an effect of 1m/sec forced air cooling for the heatsinks as shown in Fig.3.28. Using the thermal resistances of heatsinks for 1m/sec forced air cooling in Table 3.5, operating values of T_{vjmax} are found to be 93°C and 101°C for IGCT and reverse blocking diode, respectively. These values are lower than the design values of maximum operating junction temperatures (105°C for IGCT and 120°C for DIODE).



(a) (b) (c)

Figure 3.20 (a) Circuit diagram, (b) illustration (c) picture of each power semiconductor

Table 3.6 Thermal specifications of power switch assembly

Maximum Ambient Temperature= 40		
IGCT (ABB-5SHY35L4510)	T_{vjmax}	125
	safety limit in the design	20K
	$R_{j\text{-}c}$ (for double side cooling)	8.5 K/kW
	$R_{c\text{-}h}$ (for double side cooling)	3 K/kW
DIODE (EUPEC-911SH45)	T_{vjmax}	140
	safety limit in the design	20K
	$R_{j\text{-}c}$ (for double side cooling)	10 K/kW
	$R_{c\text{-}h}$ (for double side cooling)	3 K/kW
Heatsink (Fischer- SK144)	40 cm in length (R_{th1}) natural air cooling with 1m/sec forced air cooling	 160 K/kW 96 K/kW
	80 cm in length (R_{th2}) natural air cooling with 1m/sec forced air cooling	 140 K/kW 84 K/kW

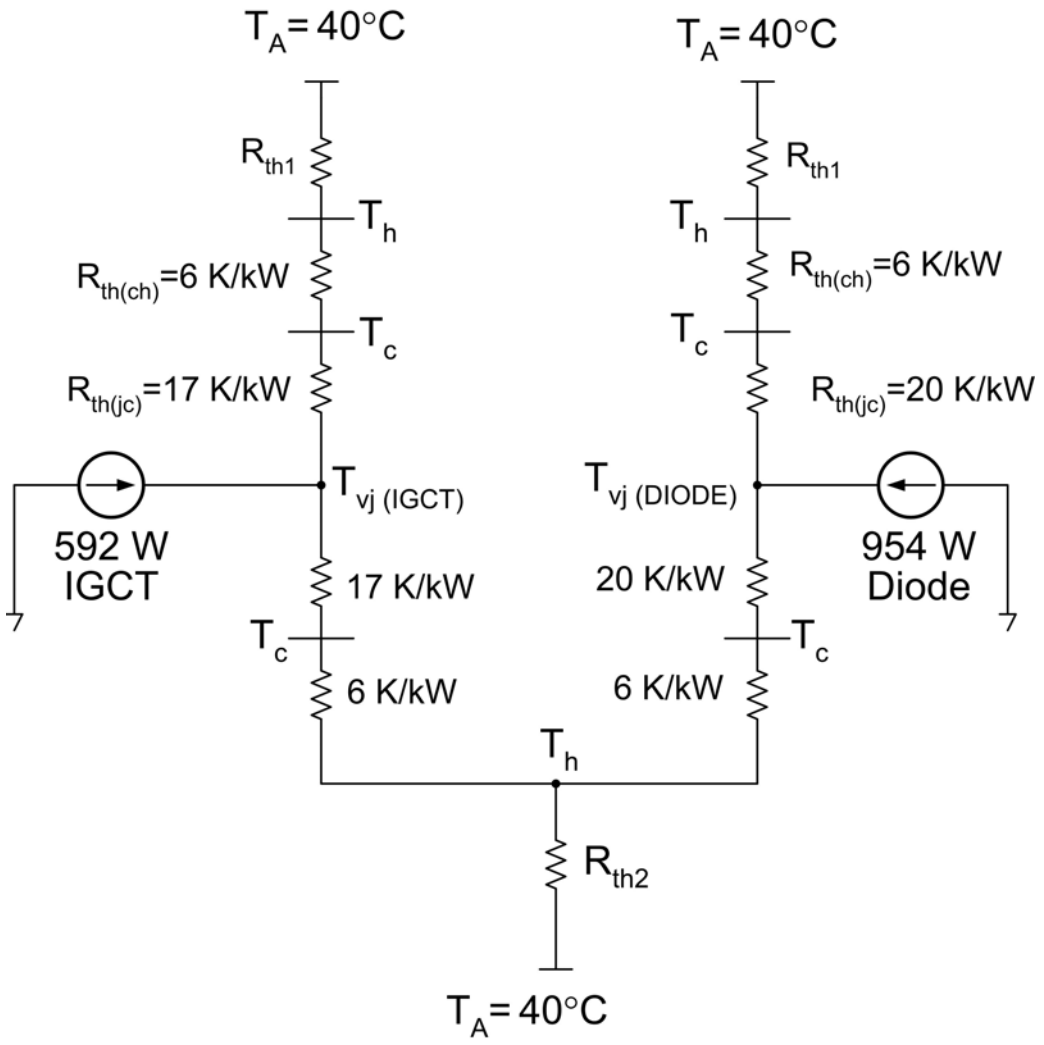


Figure 3.21 Steady-state thermal model of each power assembly

Since IGCT and DIODE have their own presspack housing their heatsinks have also been utilized as conductors to carry anode, cathode currents and terminals to make connections possible. Six power semiconductor assemblies are then connected together by the use of copper busbars to form the power stage of CSC as shown in Fig.3.22. Since the power stage with natural cooling occupies a large volume the upper half bridge and lower half bridge are to be placed into two seperate but side by side located cabinets as shown in Fig.3.23. The components in the power stage of CSC are illustrated in Fig.3.22 and can be matched with those in Fig.3.23.

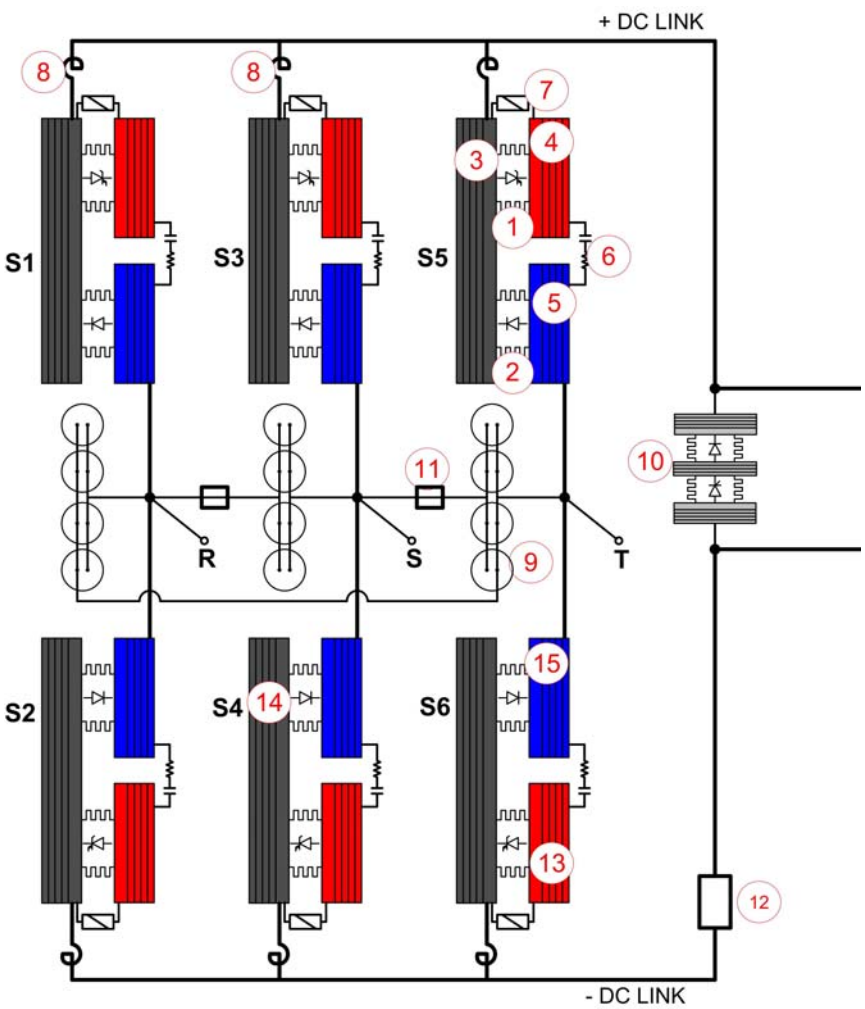
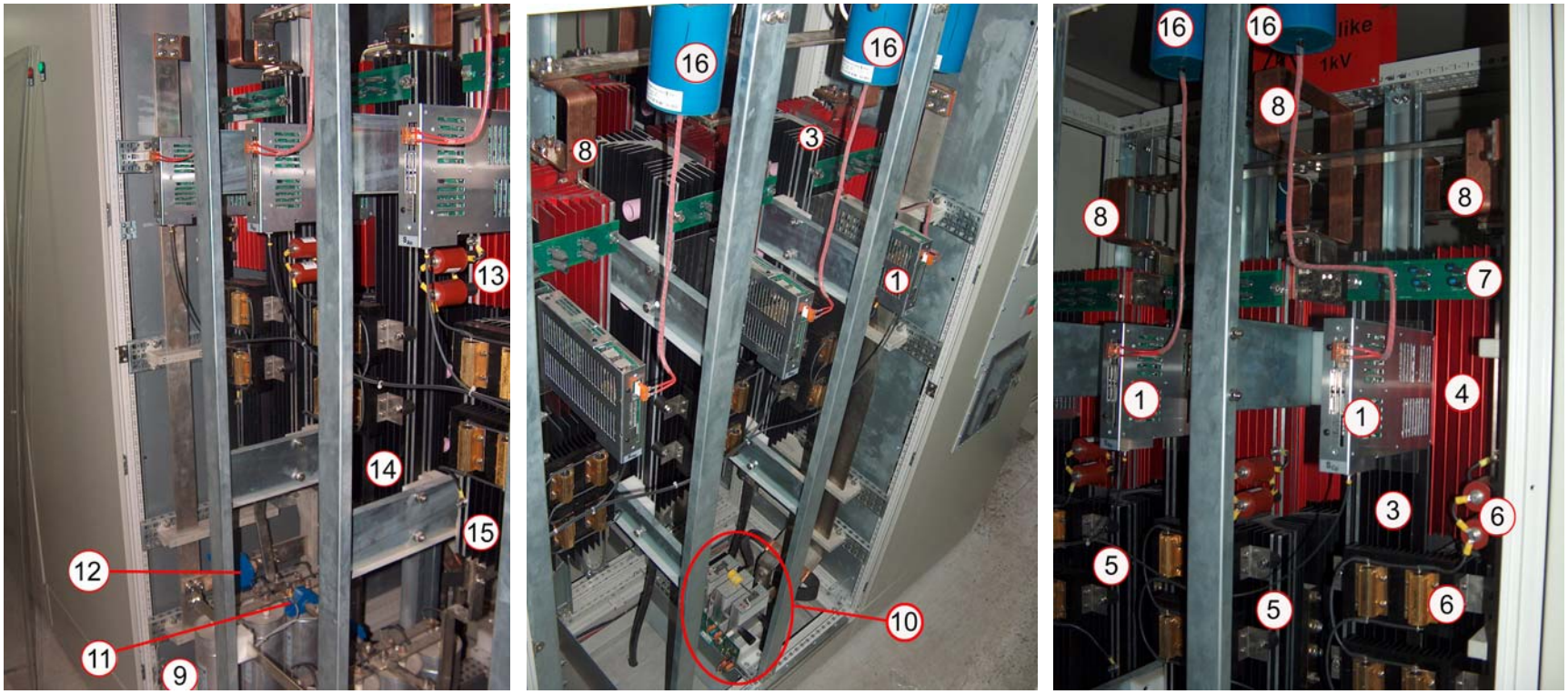


Figure 3.22. The illustration of power stage layout of CSC



(a) (b) (c)

Figure 3.23 View of power stage of developed CSC, (a) cabinet including upper half bridge of CSC, (b) cabinet including lower half bridge of CSC and filter capacitors, (c) cabinet including upper half bridge which also comprises AC-link and DC-link connections of CS

The stray inductances in the developed power stage for different commutation paths, shown in Fig.3.22 are measured in the range from 1.7 to 2.1 μH. These inductances can be utilized for di/dt limiting. The critical di/dt for IGCT at turn-on is 1000A/μsec and for the diode 1300A/μsec at turn-off. The worst case for di/dt of IGCT is during its for device turn-on and it depends on the maximum peak value of line-to-line voltage across the input filter capacitors and total inductance in the commutation path. Assuming the snubberless operation, maximum value of di/dt during load commutation can be found from (3.11). As a safer design criteria, V_{peak} is assumed to be 2000V and maximum permissible value of di/dt during load commutation is taken to be 800A/μsec for the worst case. Then, the required commutation inductance is found to be 2.5μH. This requires an additional inductances of 0.4-0.8μH besides the existing stray inductances in the commutation paths. These additional inductors, connected in series with IGCTs which are called di/dt limiting reactors are shown in Fig.3.22.

Although the switching signals are transferred to IGCT gate drivers via fiber optic interface, IGCT gate driver unit does not provide an on-board isolation. Therefore, an isolated power supply for each IGCT is required. This power supply should meet: i) isolation requirement of the nominal voltage of the converter, ii) maximum power rating of the gate driver unit at a given switching frequency and maximum controllable turn-off current of GCT, and iii) input voltage rating of the gate driver unit. In view of these constraints, specially designed IGCT power supply having an isolation level of 10kV and a nominal power rating of 100W has been used, as shown in Fig.3.23.

Typical RC snubber components as shown in Fig.3.22 are connected across each switch comprimising asymmetric IGCT and fast recovery diode for limiting overvoltages due to stray inductances and di/dt limiting reactors. The design of these RC snubbers will be given in the following section. The CSC is also equipped with a crowbar circuit. It is connected across the dc output terminals of the converter in order to provide a freewheeling path for a dc-link current against commutation failure among power semiconductors.

3.6.2 Layout of CSC based STATCOM

The CSC and its input filter which have been implemented at 1kV are shunt connected to 31.5kV bus through a coupling transformer and air insulated medium voltage switchgear equipment, as shown in Fig.3.24. Single line diagram of air-insulated medium-voltage switchgear system is as given in Fig.3.25. Fig. 3.26 and 3.27b shows the medium voltage container into which switchgear equipment are placed. The low voltage container in Fig.3.26 contains the power stage of CSC, its control system and the distribution cabinet shown in Fig.3.27a.

Outdoor system components such as coupling power transformer, air-core reactors and damping resistors are all mounted on a common concrete platform in the STATCOM yard (Fig.3.26). Footprint of the STATCOM yard is given in Fig.3.28. In Fig.3.25, basic system components are marked by encircled numbers which should be matched with those of Fig.3.24, Fig.3.26 -3.28.

Heat dissipation within the medium voltage and low voltage containers are transferred to ambient by ventilation. This is achieved by constant speed radial fans in medium voltage container and centrifugal fan controlled by variable-frequency drive in low voltage container. Inlet air provided by ventilation system of the low voltage container first passes through the IGCT cabinets in order to maintain enchanced natural cooling effect (resulting in nearly 1m/sec air flow through the heatsinks) as illustrated in Fig.3.29 for power stage of CSC.

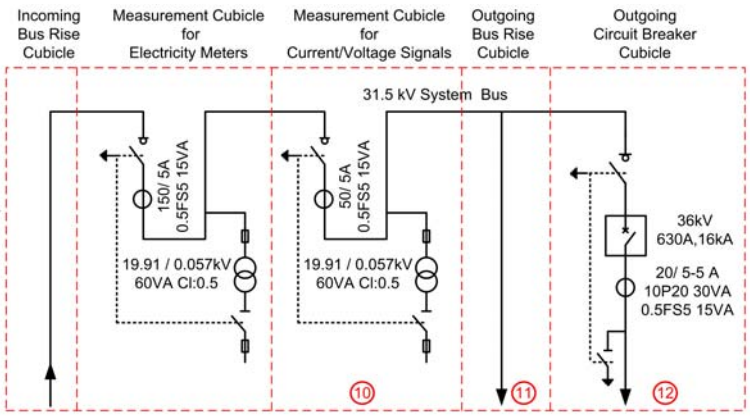


Figure 3.24 Circuit diagram of medium voltage switchgear systems

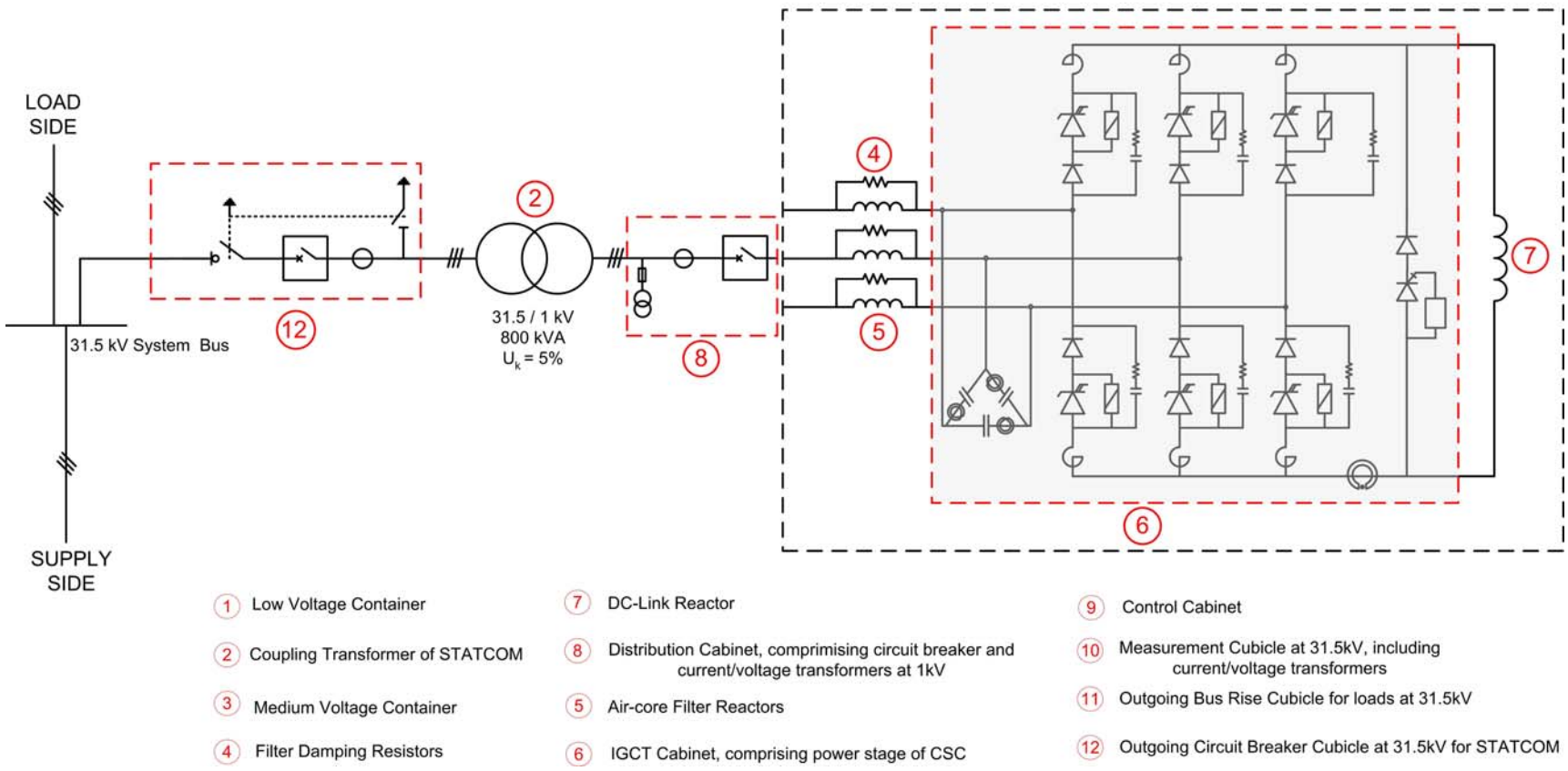
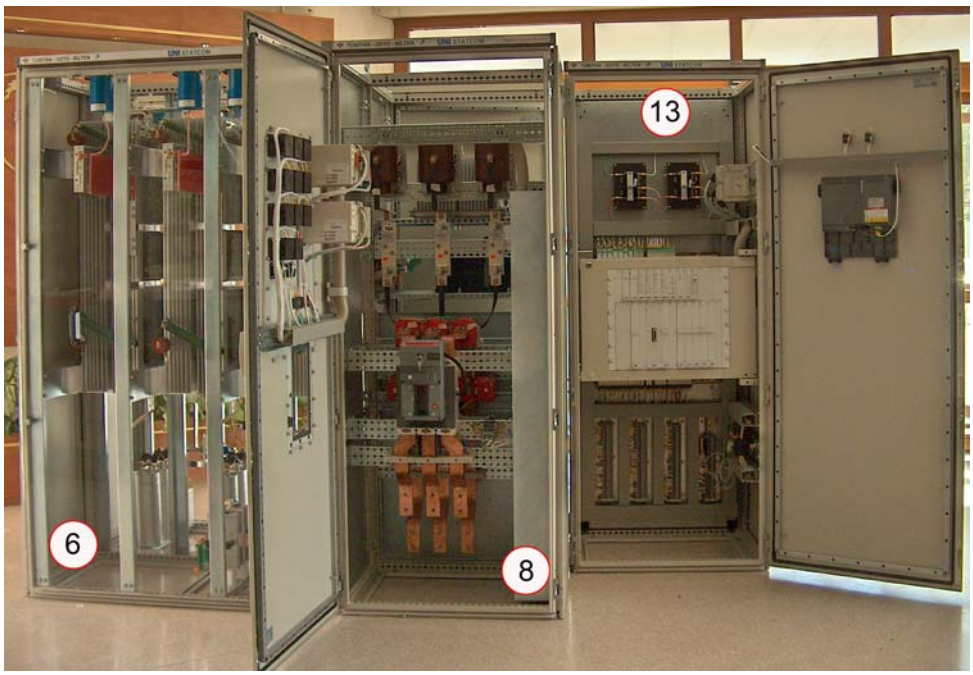


Figure 3.25. The circuit diagram of complete power stage for CSC based STATCOM,

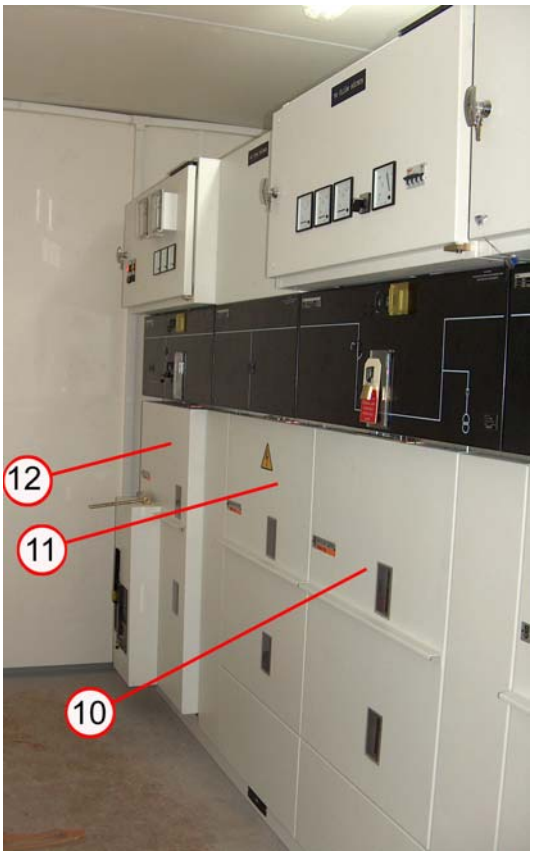
(a)

(b)

Figure 3.26 (a) CSC based STATCOM installed at (a) Tinaz Transformer Substation, (b) Sekkoy Transformer Substation of TKI



(a)



(b)

Figure 3.27 Photos of equipments inside (a) Low Voltage Container, (b) Medium Voltage Container

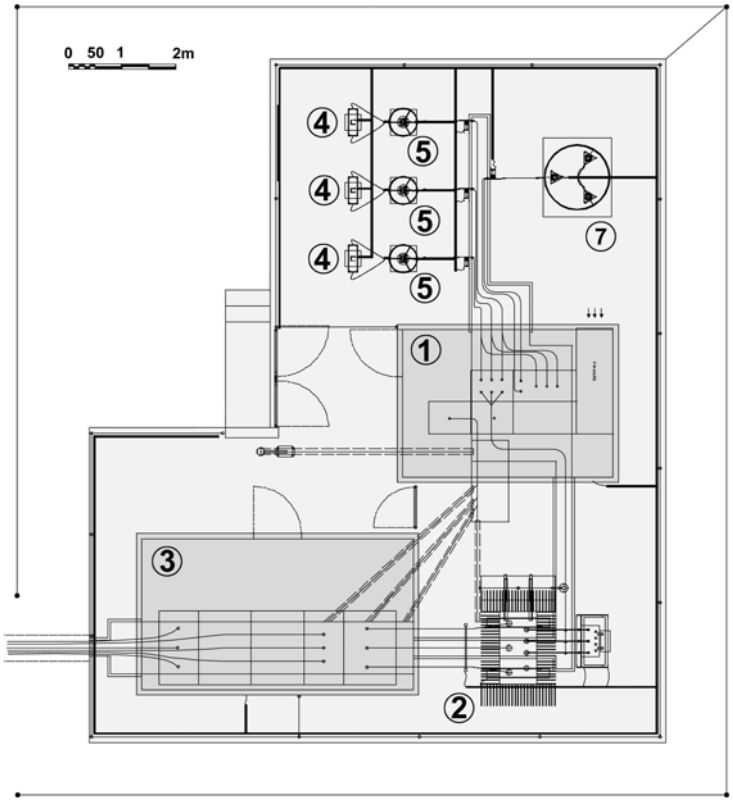


Figure 3.28 Footprint of CSC based STATCOM on a platform

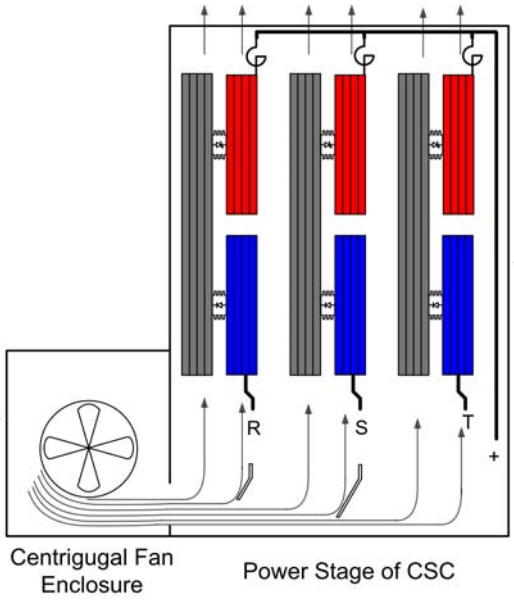


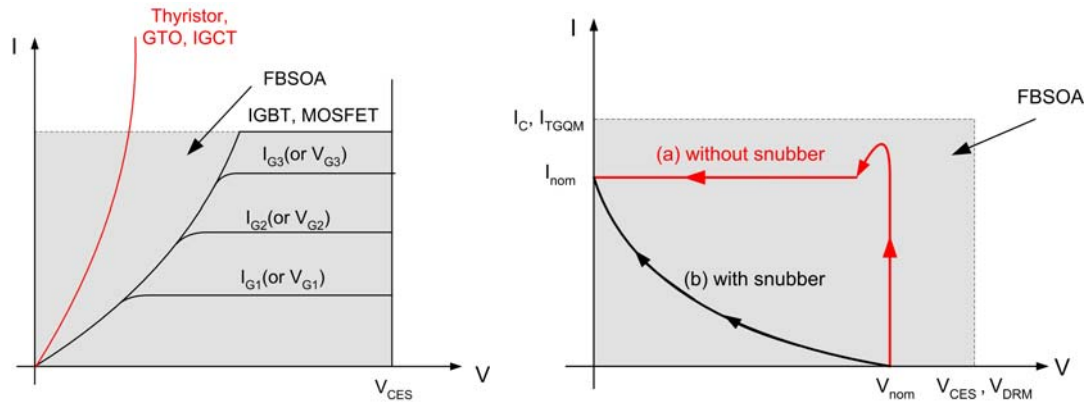
Figure 3.29 Utilization of ventilation for Low Voltage Container for cooling power stage of CSC

3.7 Design of Snubber Circuit

The function of snubber circuit is to reduce the electrical stress placed on a power semiconductor during switching by a power electronics converter to levels that are within the electrical ratings of the power semiconductors [86]. As described in Chapter 2.6, each switch in CSC, including Asymmetric IGCT and Fast Recovery Diode, experiences forced commutation or load commutation. Especially, during device turn-on and forced turn-off, IGCTs –and during load-commutated turn-off, diodes simultaneously undergo both high current and high voltage.

SCRs, GTOs, and IGCTs, unlike transistor based power semiconductors (such as IGBT, MOSFETs) have no self-current limiting capability, which is the ability for a switch to limit its maximum current regardless of the voltage applied, as shown in Fig.3.30a. For power semiconductors with good FBSOA (IGBTs, MOSFETs), the self-current limiting capability, the forced turn-on di/dt can be controlled through the gate. On the other hand, IGCTs do not have FBSOA (Forward Biased Safe Operation Area), the forced turn-on di/dt is uncontrollable and current crowding may happen in a localized area, which is particularly true for large area devices. Therefore, a snubberless forced turn-on is not possible for IGCTs, GTOs, SCRs. Having FBSOA or not, all controllable power semiconductor switches simultanuously undergo both high current and high voltage as illustrated by a switching trajectory in curve (a) of shown in Fig.3.30b. This trajectory presents an excessive switching loss not only for the power semiconductor under the forced turn-on but also diode of complementary switch under load-commutated turn-off in power converters. These switching losses can be reduced by reducing the rate of increase in device current (i.e, di/dt) under forced turn-on via a snubber for IGCTs, SCRs, GTOs or gate drive circuit for IGBTs, MOSFETs, as illustrated in curve (b) of Fig.3.30b [63].

During forced turn-off, a controllable power semiconductor switches simultaneuously undergo high current and high voltage as represented by curve (a) in Fig.3.31a, where the current stays nearly constant while its voltage increases rapidly to its nominal value. The voltage overshoot occurs due to the di/dt applied to the stray inductance in the commutation path.



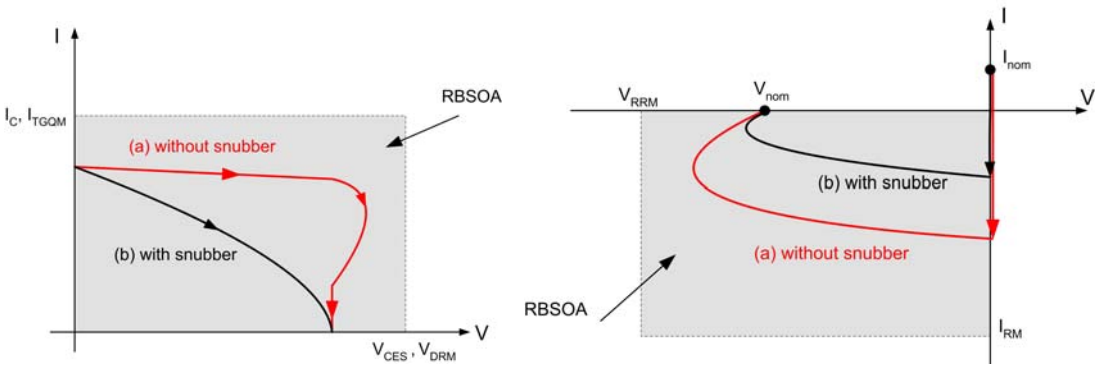
(a) (b)

Figure 3.30 (a) Forward I-V characteristic of power semiconductor switches with self-current limiting capability (black line) and without self-current limiting capability (red line), (b) I-V switching trajectory of a power semiconductor during forced turn-on [63]

Especially specified as snubberless turn-off power semiconductor switches such as MOSFETs, IGBTs, IGCTs, can trace the switching trajectory given in curve (a) in Fig.3.31a. On the other hand, GTO can not handle the switching trajectories similar to one given in curve (a) because during forced turn-off, such a dv/dt higher than the specified maximum rate of change in the increase in the anode-cathode voltage of GTO may cause retriggering of GTO back to into the on state [86]. Therefore, snubber circuit should be used in order to make the switching trajectory of GTO similar to one in curve (b) of Fig.3.31a, where the increase in device voltage (i.e, dv/dt) is slowed down by the snubber and the device current decreases before the device voltage increases to the nominal value.

During load-commutated turn-off of a switch in CSC, IGCT part of switch does not experience any electrical stress. On the other hand, its diode part experiences reverse-recovery as discussed in Chapter 2.6.2. During load-commutated turn-off, diode remains in forward conduction state untill its current reaches the value of maximum reverse recovery current. Once this value is reached, the diode starts reverse-recovery phase by making its negative current to zero exponentionally. The behaviour of the diode during reverse-recovery is defined with

its softness factor, which is defined in Fig.3.32. As the start of reverse recovery phase, the voltage across cathode-anode of diode increases to the nominal value quickly. The switching trajectory of diode during reverse recovery is illustrated in curve (a) of Fig.3.31b. The voltage overshoot occurs due to the stray inductance in the commutation path. As discussed in Section 3.3, fast recovery diode can not handle high dv/dt during reverse-recovery depeding on the application type [82]. Therefore, with the use of snubber circuit dv/dt in the cathode-anode voltage of diode during reverse-recovery can be decreased resulting in a switching trajectory in curve (b) of Fig.3.31b.



(a) (b)

Figure 3.31. (a) I-V switching trajectory and RBSOA of an IGCT during forced turn-off (b) I-V switching trajectory and RBSOA of a reverse blocking diode during load turn-off [63]

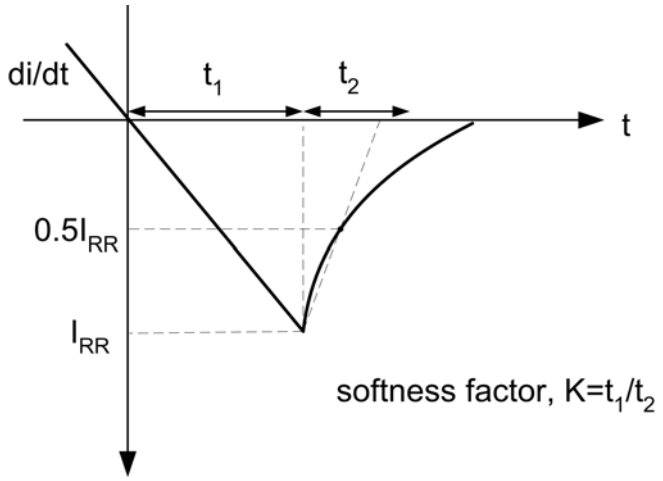


Figure 3.32 Characterization of reverse-recovery for fast recovery diode

Since the Reverse Biased Safe Operation Area (RBSOA) is defined as the maximum voltage and current boundary within which the device can turn off without destructive failure, all the possible turn-off switching trajectories should be within the RBSOA of the corresponding power semiconductor, such as given in Fig.3.31. A power semiconductor without sufficiently large RBSOA needs a snubber circuit to reduce the size of its turn-off switching trajectory in order to ensure safe turn-off operation [63].

Within the scope of this thesis, turn-on snubber has been applied in order to improve the switching characteristics of Asymmetric IGCT and fast recovery diode during load commutation, where IGCT undergoes forced turn-on and diode undergoes load turn-off. Since IGCT has no gate control, the rate of increase in its anode current (i.e, di/dt) can only be controlled by turn-on snubber circuit, which will be described in the following section.

3.7.1 Design of Turn-on Snubber

Turn-on snubber limits di/dt of IGCT current during device turn-on period and also at the same time –di/dt of reverse blocking diode of the complementary switch, which is going to be turned off simultaneously.

Since IGCTs do not have self-current limiting capability, absolute maximum di/dt rating of the selected IGCT, 5SHY35L4510 has been specified as 1000A/μsec at device turn-on by the manufacturer. As described in Chapter 2.6, the device turn-on of an IGCT cause load turn-off of a diode in the complementary switch in CSC applications. During this commutation process, limitation of di/dt is not only necessary for IGCT under forced turn-on but also fast recovery diode of the complementary switch under load-commutated turn-off. Because, both IGCT and fast recovery diode experience the same di/dt and the magnitude of maximum reverse-recovery current of fast recovery diode increases with di/dt. The critical value of di/dt for fast recovery diodes is also usually specified in their datasheets. For the selected fast recovery diode, D911SH45 it has not been specified, but from the figures for the maximum reverse recovery current, it should not be higher than

1200A/μsec. For this purpose, the common approach is the use of di/dt limiting reactors in series with IGCTs as a turn-on snubber [63,67,86]. These di/dt limiting reactors have been demonstrated in Section 3.6.1.

The value of di/dt limiting reactor can be calculated for the specified maximum peak value of line-to-line voltage across the input filter capacitor and maximum allowable di/dt by using (2.29). In designing di/dt limiting reactor as a turn-on snubber, following conditions should be considered:

i. There are two di/dt limiting reactors on any commutation path (i.e, L_{S1} and L_{S3} in Fig.2.33) in CSC. Beside these reactors, there may be significant total stray inductance on each commutation path. Hence, the expression in (3.11) should be used in calculating the required inductance of di/dt limiting reactors. Depending on the power stage layout, stray inductance on different commutation paths shown in Fig.2.34 may be different and this may result in different di/dt limiting reactors so that specified di/dt rating of all IGCTs can be fully and equally utilized.

$$\left(L_{S1} + L_{S3} + L_{stray}\right) = \frac{V_{RS}}{di/dt} \tag{3.11}$$

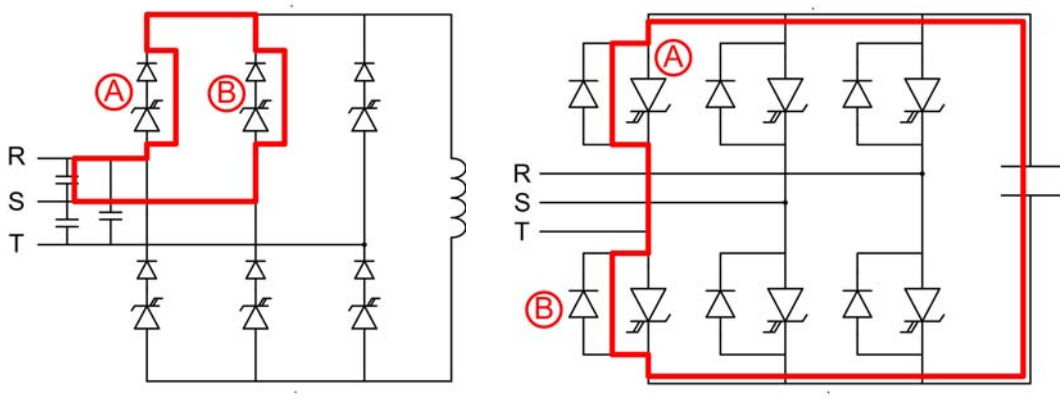
ii. The maximum peak value of line-to-line voltage should be taken into account by the use of results of simulation work for the maximum capacitive reactive power generation capability of CSC based STATCOM. Due to voltage regulation phenomena discussed previously, it may be much higher than the rated value of the system voltage. Although it is found from the simulation works that the maximum value of line-to-line voltage across the input filter capacitors during any load commutation is lower than the maximum peak value of that line-to-line voltage across the input filter capacitors for the same operating conditions, it is wise to take the maximum peak value for a safer design approach.

iii. Choosing design value of di/dt slightly lower than maximum permissible di/dt limit of IGCT and fast recovery diode (whichever is lower) may be a better design approach for reliability. On the other hand, the switching

losses and magnitude of maximum reverse recovery current of diode increases with di/dt and on the other di/dt may result in higher di/dt limiting reactors, which may result in excessive overshoot during forced turn-off of IGCTs or load commutated turn-off of fast recovery diodes. A compromise should be done according to results of switching tests by considering a good trade-off between the maximum allowable voltage overshoot at forced turn-off and swithing losses

iv. Since di/dt rating of IGCTs is relatively low in comparision with HV-IGBTs the stray inductance in the IGCT based power circuit of both voltage source and current source converters always presents some difficulties in the design and implementation of the corresponding circuits. Typical stray inductance paths during the current commutation from outgoing to incoming IGCT are marked.By designing the layout of power stage the stray inductance in both of these topologies can be brought to absolute minimum. For this case, IGCTs and DIODEs face with following problems:

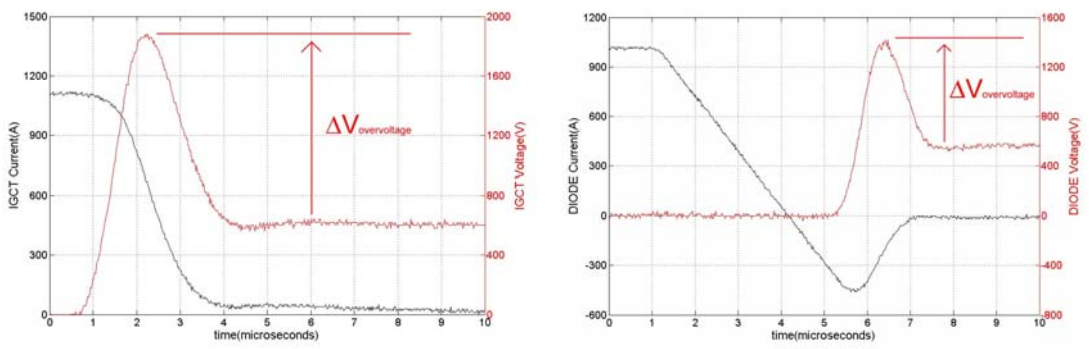
- In the device turn-on period, the rate of change in current may exceed maximum permissible value of di/dt for IGCT or maximum permissible value of –di/dt for DIODE of the complementary IGCT (whichever is smaller).



(a) (b)

Figure 3.33 Typical current commutation from device A to device B (a) for voltage source converter, where A is IGCT and B is DIODE, and (b) for current source

- During device and load turn-off periods –di/dt in excess of maximum permissible value leads to appear a dangerous overvoltage across the power terminals of outgoing IGCT or DIODE. This rvoltage overshoot is shown to be superimposed on dc-link voltage in VSC and on the instantaneuos value of the corresponding line-to-line voltage. A sample waveform obtained in laboratory is shown in Fig.3.34.



(a) (b)

Figure 3.34 Sample waveforms illustrating overvoltage (a)across outgoing IGCT due to –di/dt during forced turn-off (b) across outgoing DIODE due to –di/dt during load turn-off (sampling rate: 50MS/sec)

First problem can be eliminated by introducing external inductors (di/dt limiting inductors) into the commutation paths of CSC and VSC. Possible connections for these inductors are as illustrated in Fig.3.35. However, addition of di/dt limiting reactors to the circuit has the following drawbacks:

1) Utilization of IGCT forward voltage blocking or DIODE reverse voltage blocking capability is reduced. Optimum utilization occurs at the expense of higher reverse recovery current of its reverse blocking diode and its turn-on losses.

2) For a peak value of the line-to-line voltage in CSC and dc-link voltage in VSC higher than pre-specified value in the turn-off period, the peak

of the voltage overshoot may exceed forward voltage blocking capability of IGCT or reverse voltage blocking capability of DIODE at rated current. This problem can be entirely solved by using clamping snubber in VSC as shown in Fig.3.36a. However, this problem can be alleviated to a certain extent by using turn-off snubber across IGCT and its reverse blocking diode as shown in Fig.3.36b. Because the use of clamping snubbers one for each di/dt limitng reactor is not possible due to the bipolar voltage blocking capability of power semiconductors in CSC.

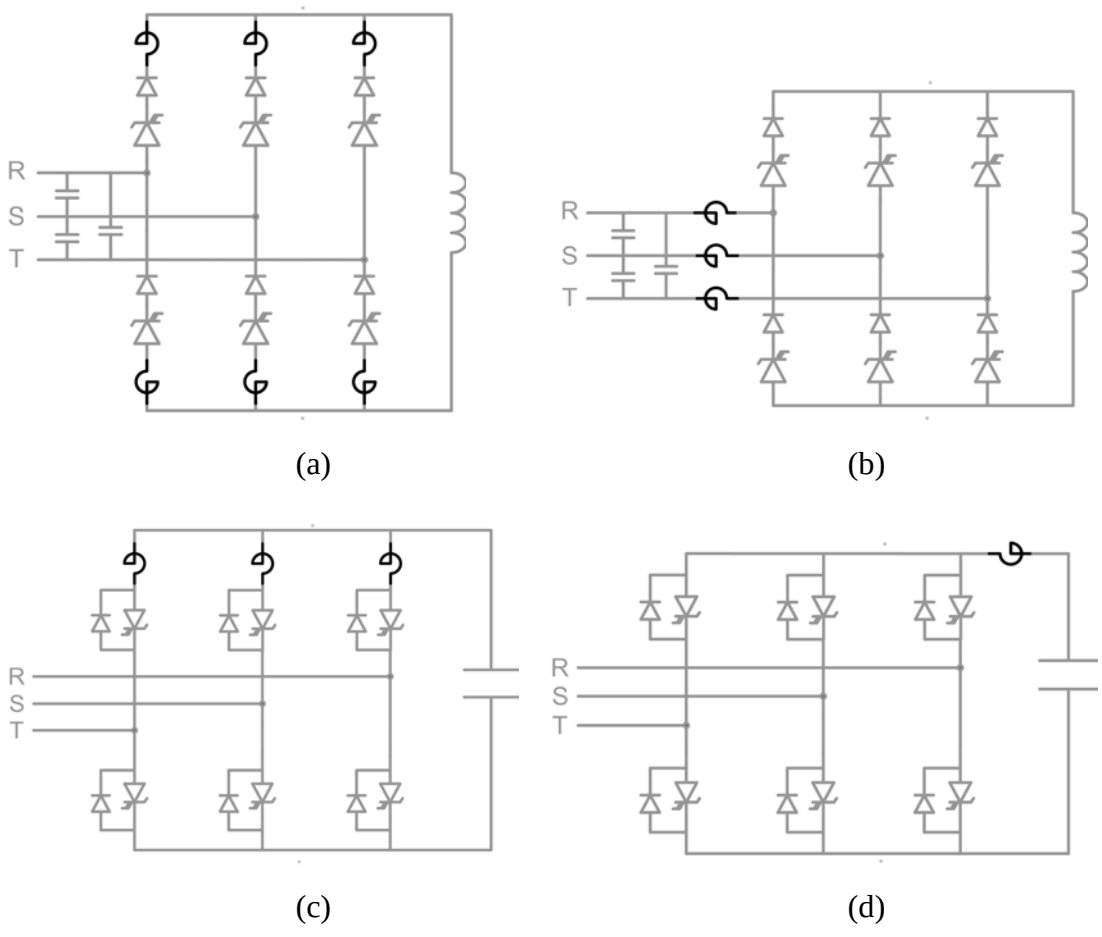
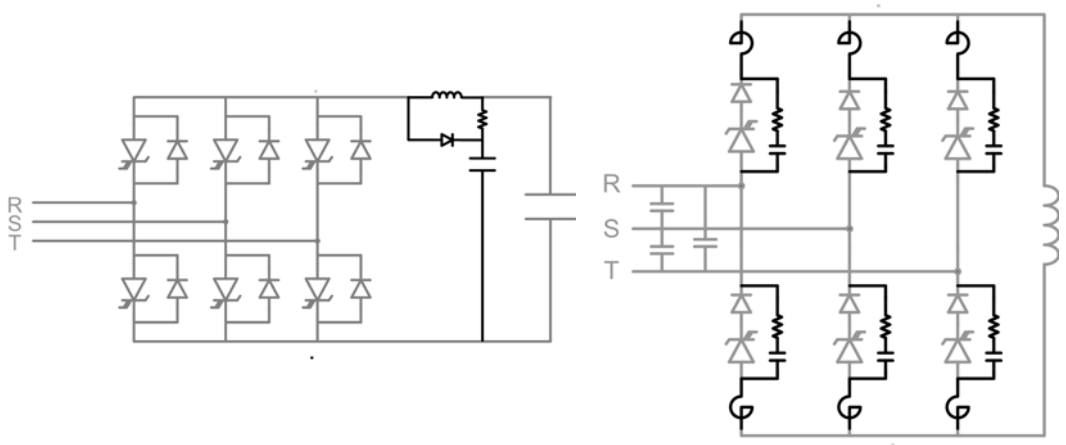


Figure 3.35 Possible connections of di/dt reactors for IGCT based converters (a) typical connection for CSC, (b) alternative connection for CSC, (c) inefficient connection for VSC, (d) common connection for VSC



(a) (b)

Figure 3.36 (a) Illustration of clamping snubber in VSC, and (b) Illustration of turn-off snubber in CSC

In view of these constraints, total inductance on any commutation path has been adjusted to 2.5μH while the maximum peak value of line-to-line voltage is specified as 2000V and maximum allowable di/dt as 800A/μsec. The stray inductance on different commutation path of the implemented power stage layout has been measured between 1.7 and 2.1 μH. Then, different di/dt limiting reactors has been designed in the range of 0.2 and 0.4 μH, as illustrated in Fig.3.22.

In literature, turn-on snubbers may be used as polarized L-R snubbers [86] where diode and resistor are connected across the di/dt limiting reactors in order to dissipate the energy stored in the reactor onto the resistor through the diode at forced turn-off so that overvoltage across IGCT can be avoided. Since it is polarized snubber, there is still overvoltage across the fast recovery diode during its load-commutated turn-off. Since the required di/dt limiting reactor for IGCT applications is much lower than that for GTO applications, this type of snubber may present unnecessarily complicated and expensive solution.

3.7.2 Design of Turn-off Snubber

Although the chosen asymmetric IGCT and fast recovery diode have the snubberless turn-off capability, turn-off snubber would improve their switching characteristics or trajectories, as discussed in Section 3.7. For GTO based CSC applications RCD snubbers, which clamp the voltages across GTO to safe levels and limit dv/dt during turn-off have been used [37,47,68,86]. Due to the presence of a and a need to a larger di/dt limiting reactor and maximum permissible value for dv/dt for GTO in contrary to IGCTs, RCD snubber becomes bulky and lossy. Therefore, optimization of RCD based turn-off snubber components for GTO based CSC applications becomes an important issue in the design[37]. Moreover, regenerative snubbers have also been studied in order to reduce snubber losses for high frequency GTO based PWM converter at the expense of further circuit complexity [30].

With the introduction of IGCTs, which have superior switching characteristics as compared with GTO, complex, expensive and bulky RCD snubbers are replaced with the simple RC snubbers for CSC applications [47,63,67,77-79,64]. The unpolarized RC snubbers have been widely used to protect diodes and thyristors not only for limiting dv/dt at reverse recovery but also the maximum voltage overshoot [47, 63]. Therefore, the design of RC snubber is well known for the three phase line-commutated CSC [69,86]. The design rules of RC snubber for CSC applications has been studied in [63].

When power semiconductors of the same type are going to be connected in series, it is a general rule to connect individual RC snubber to each power semiconductor for ensuring equal dynamic voltage sharing among them. However, in this application fast recovery diode is going to be connected in series with the main switching element an asymmetric IGCT in order to attain reverse blocking capability for the resulting power semiconductor switch. Here, IGCT part of the resulting switch blocks the forward voltage and diode part blocks the reverse voltage. Therefore, the use of a single RC snubber across the resulting switch is adequate to achieve the limitation of both dv/dt and overvoltage which appear across the IGCT in the forward direction and across the diode in the reverse direction.

In this study the design of RC snubber has been carried out by using equivalent circuit of CSC and actual turn-off characteristics of IGCT and reverse blocking diode. In the design of RC snubber some simplifying assumptions are also needed. In [63] some expressions the origin of which is not known are used in the calculations of R and C values. In the snubber design, the actual device characteristics are to be used. In [69] a methodology that can be used for phase recovery power diodes is proposed. This application note proposes the use of curve fitted to the actual diode characteristics instead of its semiconductor model in the design of RC snubber.

In this thesis, the equivalent circuit shown in Fig.3.37 is used. The behaviour of CSC during various commutation periods can be satisfactorily represented by this equivalent circuit. Beside the common snubber components R and C, stray inductance in the snubber circuit is also taken into account as L_{cl}. The typical stray inductance in the commutation path in the actual power stage of CSC is represented by L_{comm}. IGCT characteristic during forced turn-off is obtained experimentally on the actual device (5SHY35L4510) in the laboratory (Fig.3.9). Diode characteristic in reverse recovery phase during load commutation has also been obtained for the actual device (D911SH45) in the laboratory (Fig.3.9). These characteristics are then approximated respectively by hyperbolic secant and exponential functions as given in Fig. 3.38 and 3.39.

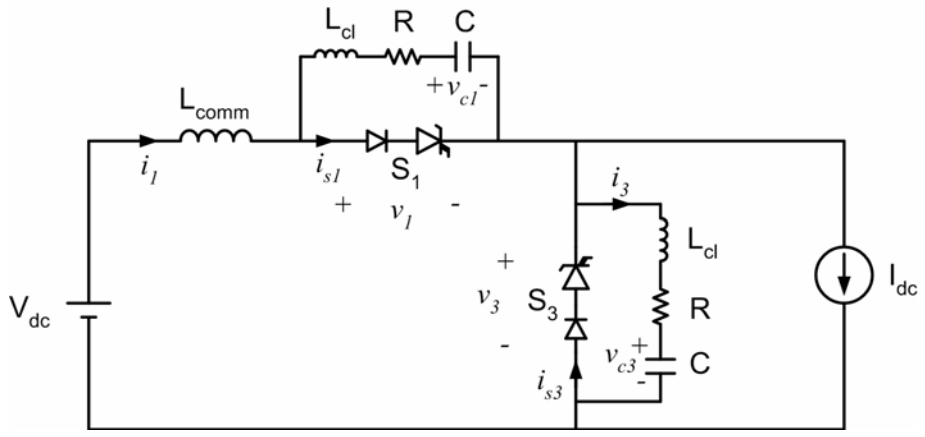


Figure 3.37. Equivalent circuit for snubber design for CSC

Another approximation in design is that the dc-link current I_{dc} is assumed to be level. In order to find out the response of the snubber circuit in Fig.3.37 against different snubber parameters (R,C and L_{cl}) first state-space representations of the circuit for the forced turn-off of IGCT and load turn-off of DIODE and then these mathematical models have been solved by using MATLAB Simulink.

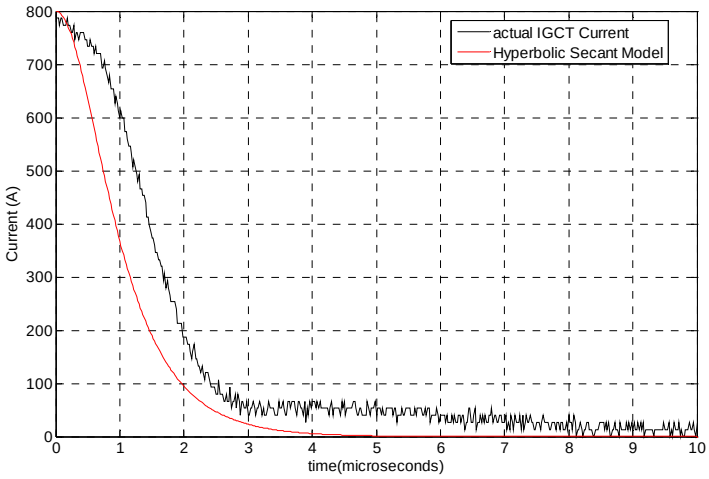


Figure 3.38 The hyperbolic secant model and the real IGCT current during forced turn-off

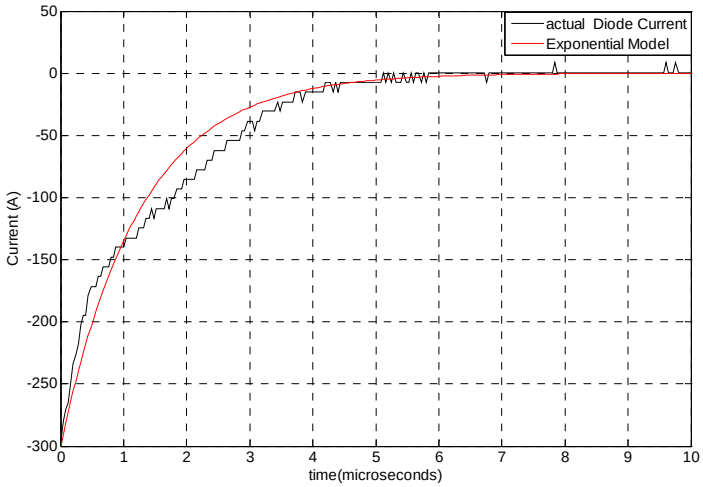


Figure 3.39 The exponential model and the real DIODE current during reverse-recovery

3.7.2.1 Snubber Performance during forced turn-off of IGCT

As discussed in Chapter 2.6.1, there are two phases during forced commutation in CSC, and hence in the equivalent circuit in Fig.3.37 : i) Turning off of S1, its current starts decreasing and its voltage starts increasing while S3 stays turned off since it is revesed biased due to the negative voltage across it, ii) when the voltage across S3 tends to be positive, S3 becomes forward biased and S3 becomes turned on.

For the first phase, the equivalent circuit is as given in Fig.3.40. The voltage across snubber capacitor of S1 is intially zero while the voltage across the snubber capacitor of S3 is V_{dc}. The current through commutation inductance, L_{comm} is initially I_{dc}. The current waveform of S1 is inherent to its characteristic during forced turn-off and it has been defined in terms of hyperbolic function, as illustrated in Fig.3.38. The definition of the hyperbolic secant function is also given in (3.12). Then, the state-space representation can be obtained as in (3.12) by applying the KCL and KVL to the equivalent circuit in Fig.3.40.

$$
\begin{aligned}
&(L_{comm} + 2L_{cl})\frac{di_1'}{dt} = -2Ri_1' - v_{c1} - v_{c3}' + Ri_{S1} + L_{cl}\frac{di_{S1}}{dt} - RI_{dc} \\
&C\frac{dv_{c1}}{dt} = i_1' - i_{S1} + I_{dc} \\
&C\frac{dv_{c3}'}{dt} = i_1' \qquad (3.12) \\
&i_{S1} = I_{dc}\sec h(t/\tau) \\
&\text{where } i_1 = I_{dc} + i_1' \quad \text{and} \quad v_{c3} = V_{dc} + v_{c3}',\ \tau = 0.68\mu\sec
\end{aligned}
$$

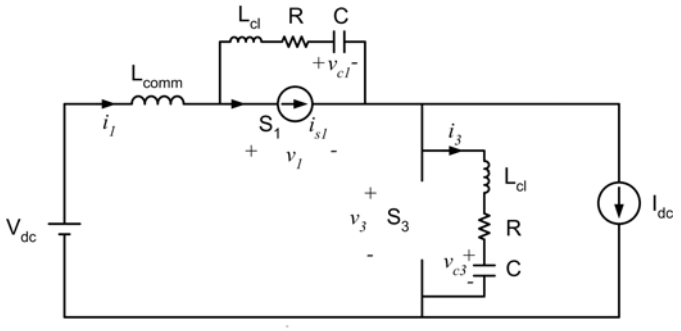


Figure 3.40 The equivalent circuit for the first condition during forced commutation

In the second phase, the equivalent circuit is as given in Fig.3.41. The initial conditions of the state variables, $v_{c1,}$ v_{c3}, i_1, i_3 and the input variable, i_{S1} can be determined for the condition for which v_3 is zero at t_0 in (3.12). Then, the differential equations can be derived as in (3.13) by using KCL and KVL so that one can define the state-space representation for the second phase.

$$
\begin{aligned}
&(L_{comm} + L_{cl})\frac{di_1'}{dt} = -Ri_1' - v_{c1}' + Ri_{S1} + L_{cl}\frac{di_{S1}}{dt} - RI_0 - V_0 + V_{dc} \\
&C\frac{dv_{c1}}{dt} = i_1' - i_{S1} + I_0 \\
&i_{S1} = I_{dc}\sec h((t - t_0)/\tau) \\
&\text{where } i_1 = I_0 + i_1' \quad \text{and} \quad v_{c1} = V_0 + v_{c1}',\ \tau = 0.68\mu\sec
\end{aligned}
\tag{3.13}
$$

The transient simulation model based on the state-space representations found from (3.12) and (3.13) is presented in Appendix F. Simulation model has been developed in order to investigate the effects of snubber components on the voltage across IGCT of S1 during forced turn-off. Taking commutation inductance (L_{comm}), maximum peak value of line-to-line voltage (V_{dc}) and dc-link current (I_{dc}) as 2.5μH, 2000V, and 800A, voltage waveforms across IGCT during forced turn-off are found from the simulation model for different value of the snubber components and are given in Fig.3.42.

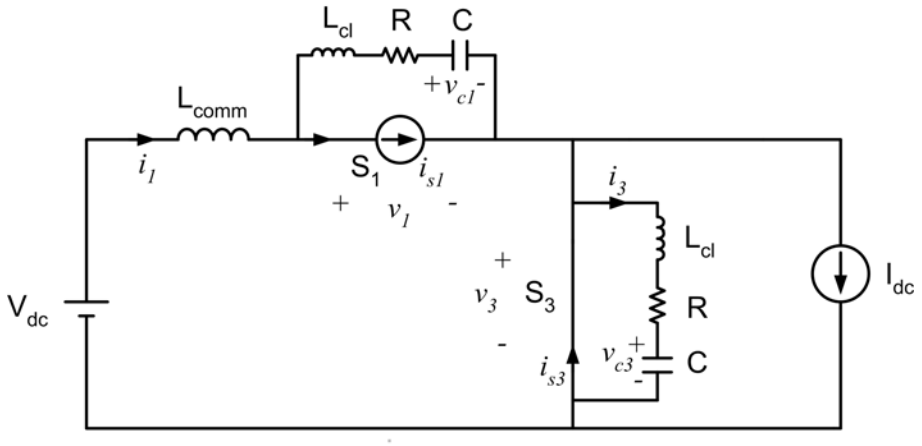
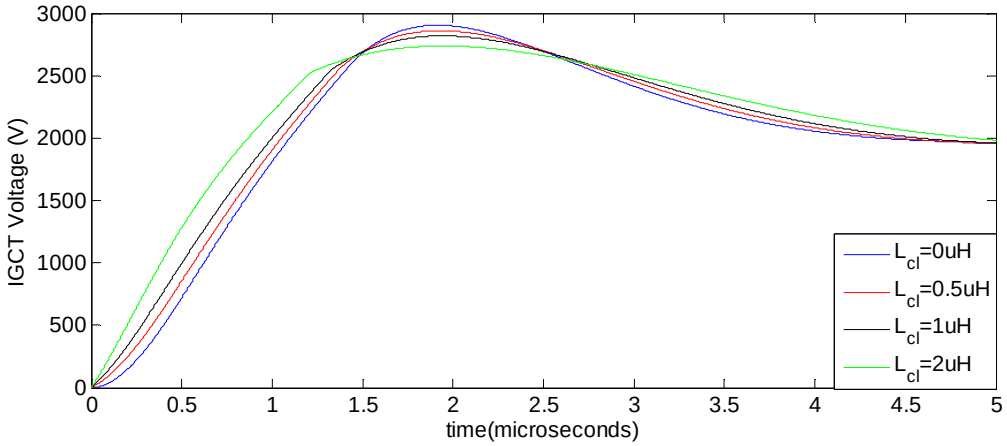
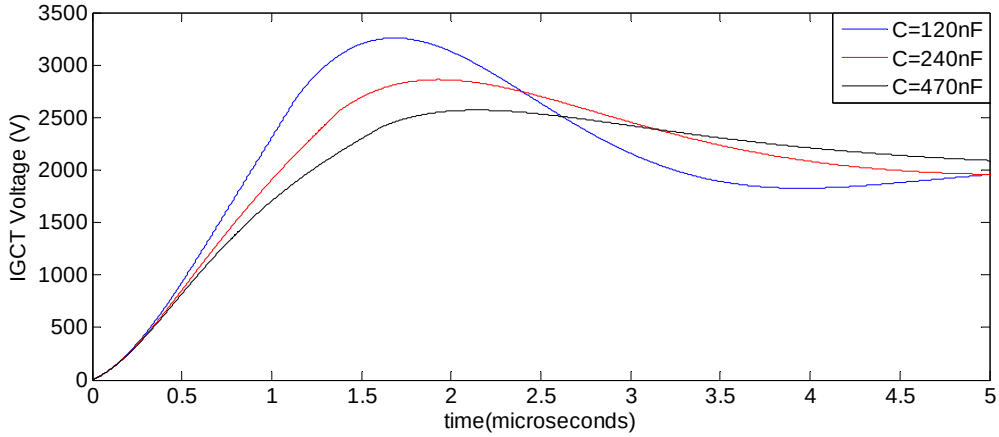


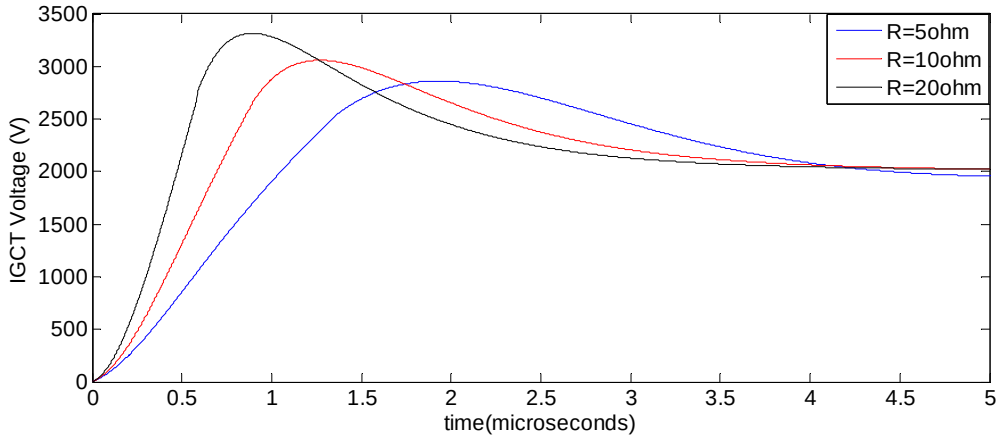
Figure 3.41 The equivalent circuit for the second phase during forced commutation



(a)



(b)



(c)

Figure 3.42 Snubber performance during froced turn-off of IGCT (MATLAB)
(a) effects of stray inductance R=5Ω, C=0.24μF (b) effects of snubber resistance L_{cl}=0, C=0.24μF ,
(c) effects of snubber capacitance L_{cl}=0, R=5Ω,

3.7.2.2 Snubber Performance during load turn-off of DIODE

In load commutation, turn-off snubber acts only during reverse recovery phase of reverse blocking diode of outgoing switch S3. Prior to reverse recovery phase both S1 and S3 are conducting. The reverse recovery current of reverse blocking diode of S3 is inherent to its characteristics and modeled as a current source which is an exponential function of time as illustrated in Fig.3.39. The equivalent circuit for the reverse recovery phase is as given in Fig.3.43. As the reverse recovery current of S3 goes to zero its voltage increases in the negative direction. Hence, this voltage appears across the reverse blocking diode of S3. During this phase, S1 is conducting and carrying the reverse recovery current of S3 together with dc-link current. Initial value of reverse recovery current is I_{RM} and the snubber capacitors of S1 and S3 are uncharged. Meanwhile, the current through commutation inductance (i_1) is initially $I_{dc}+I_{RM}$. Then, the differential equations for the equivalent circuit in Fig.3.43 can be derived as in (3.14).

$$\begin{aligned} &\left(L_{comm}+L_{cl}\right)\frac{di_3}{dt} = -Ri_3 - v_{c3} + + L_{comm}\frac{di_{S3}}{dt} + V_{dc} \\ &C\frac{dv_{c3}}{dt} = i_3 \\ &i_{S3} = -I_{RM}e^{-t/\tau} \text{ where } \tau = 1.25\mu sec \end{aligned} \tag{3.14}$$

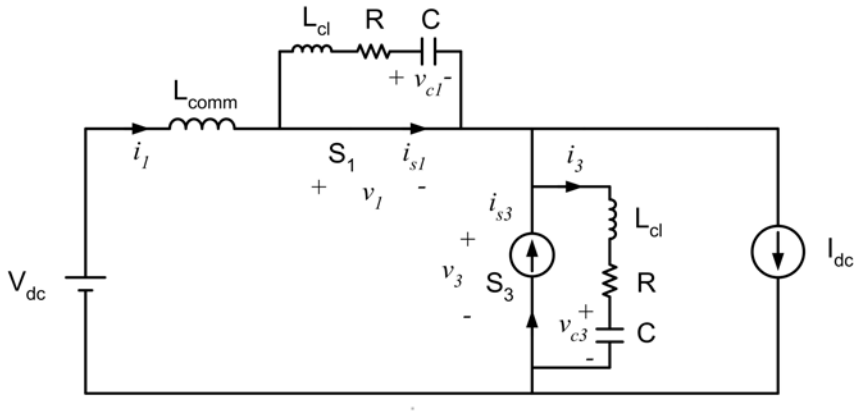
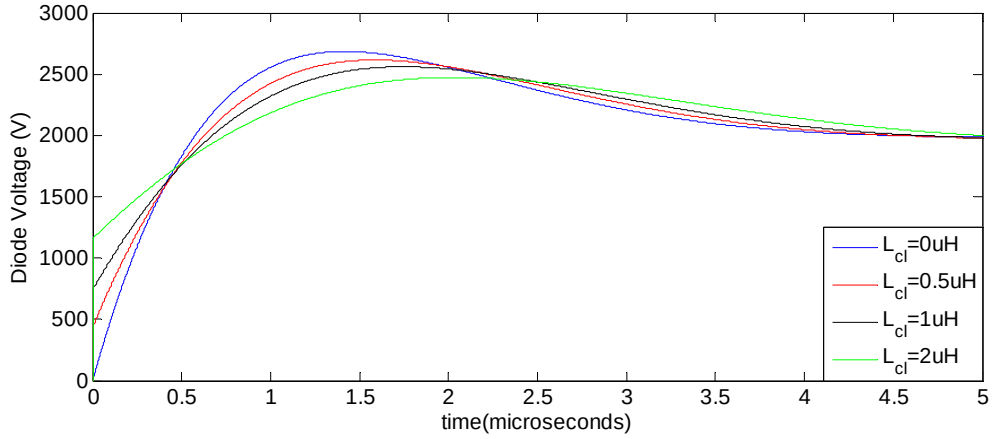


Figure 3.43 The equivalent circuit during load commutation where diode of S3 is in reverse recovery phase

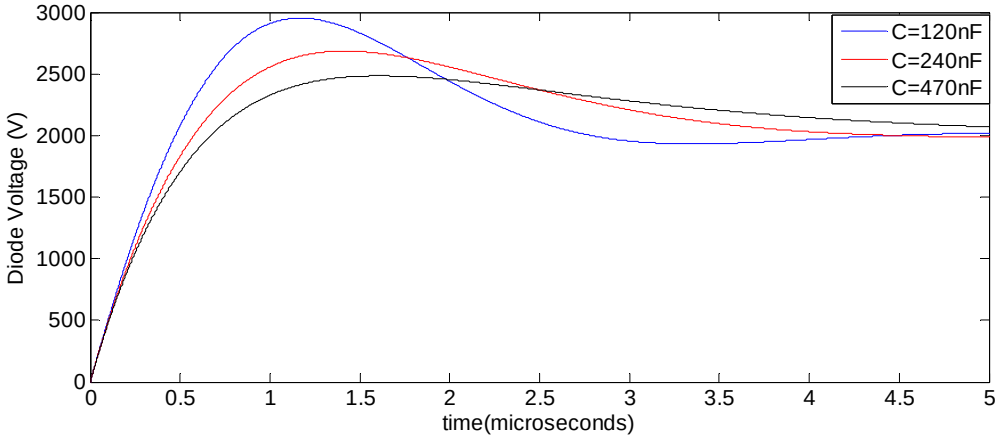
Using the state space representations in (3.14), another simulation model has been developed in order to investigate the effects of snubber components on the voltage across diode of S3 during reverse recovery phase in load commutation. This simulation model, which is also developed in MATLAB Simulink, is given in Appendix D. Taking commutation inductance (L_{comm}), maximum peak value of line-to-line voltage (V_{dc}), dc-link current (I_{dc}) and maximum reverse recovery current (I_{RM}) as 2.5μH, 2000V, 800A and 300A respectively, voltage waveforms across reverse blocking diode of S3 during reverse recovery phase are found from the simulation model for different value of the snubber components and are given in Fig.3.44.

3.7.2.3 Effects of Snubber Capacitance on Snubber Losses

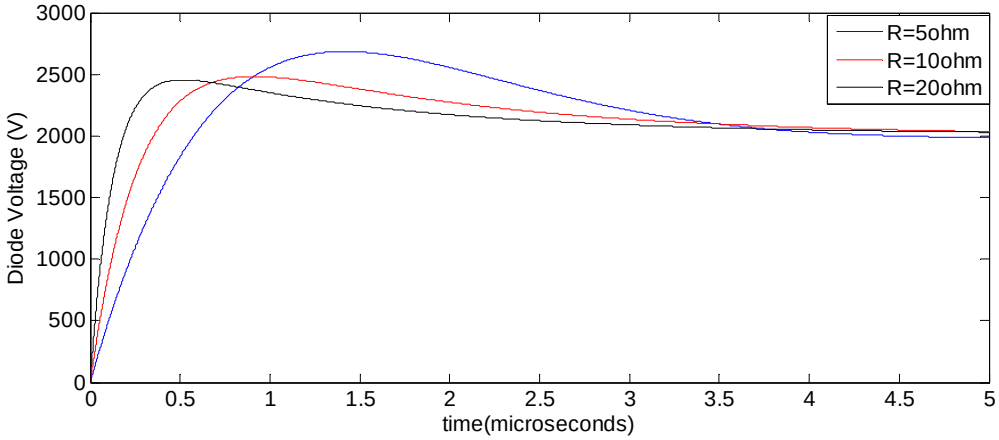
Beside the effects of snubber components on the switching waveforms of the power semiconductors, the power loss should also be considered. Simple expression can not be driven for the power loss in snubber circuit since the snubber capacitor does not only charge and discharge during switching of its power semiconductor but also switching of other semiconductors in CSC. As the snubber capacitor charges and discharges through the snubber resistor, the power dissipation on the resistor occurs and this depends on the value of snubber capacitor, swtiching frequency. From the simulation of CSC based STATCOM, the power dissipation on the snubber resistor for different values of snubber capacitor is found for the worst case and given in Fig.3.45.



(a)



(b)



(c)

Figure 3.44 Snubber performance during load turn-off of DIODE (MATLAB)
(a)) effects of stray inductance R=5Ω, C=0.24μF (b) effects of snubber resistance L_{cl}=0, C=0.24μF , (c) effects of snubber capacitance L_{cl}=0, R=5Ω,

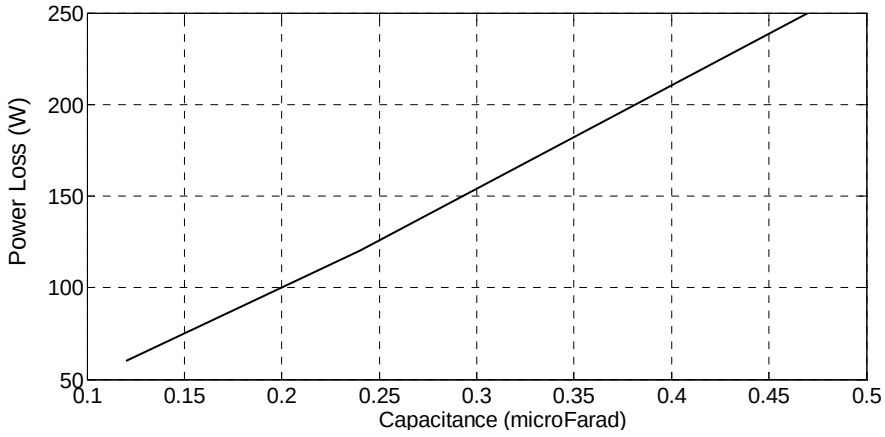


Figure 3.45 The simulated power dissipation of snubber circuit for different snubber capacitors (based on PSCAD/EMTDC)

3.7.2.4 Selection Criteria of Snubber Parameters

In three phase full bridge converters , similar to CSC in Fig.2.1, RC snubbers interact with each other at each turn-off. This can be observed from Chapter 2.6., where there exists current flow through all RC snubbers during commutations. This results in effective values of snubber components different than their actual values, as proposed in [67, 69]. The effective values of the snubber components in CSC can be approximated as in (3.15), where C_{eff} and R_{eff} are the effective values to be used in the equivalent circuit in Fig.3.37 and R and C are the actual values in CSC.

$$R_{eff} = \frac{3}{5}R \text{ and } C_{eff} = \frac{5}{3}C \qquad (3.15)$$

The turn-off snubber acts in two operation periods of CSC as described in Subsections 3.7.2.1-3.7.2.2. For each operation period an optimum set of snubber parameters R, C, and L_{cl} can be assigned. However, the chosen and the implemented snubber circuit is unique and should save all operation modes mentioned above. Therefore, a compromise is needed in order to ensure a satisfactory snubber performance during both IGCT forced turn-off and diode load turn-off.

Optimum parameters of the common snubber circuit are determined in view of the following facts and criteria.

i. An increase in the value of snubber capacitor leads to a reduction in dynamic overvoltage during forced and load turn-off at the expense of snubber losses (Fig.3.45)

ii. Switching losses of IGCT and reverse blocking diode are reduced effectively by keeping dv/dt at relatively low values. This is because at the beginning of turn-off period device current decays rapidly depending upon only the device characteristic while device voltage rises relatively slowly. This makes necessary the use of larger C and small R as can be understood from Fig.3.42 and 3.44.

iii. A larger stray inductance in the snubber circuit leads to a weaker damping effect in limiting dv/dt and dynamic overvoltage across power semiconductor. Therefore, it should be minimized in the selection of R and in the implementation of snubber circuit layout.

iv. It is not recommended to choose a snubber resistance larger than an optimum value because dv/dt and dynamic overvoltage increases considerably across the IGCT (Fig.3.42c) and less prominently across the diode (Fig.3.44c). On the other hand, a resistance value less than a critical minimum value is also not recommended because of poor damping effect of snubber circuit. Furhter than these, unnecessarily larger values of snubber resistance does not make any further contribution to dynamic overvoltage reduction across diode.

v. In the selection of snubber resistance and the implementation of stray inductance discharge period of snubber capacitor during first turn-on should also be taken into account. Discharge current closes its path through IGCT, reverse blocking diode combination. Although di/dt during the discharge period can be higher than di/dt limit of IGCT only for discharge current values considerably lower than device rating as specified by the manufacturer, di/dt can be adjusted to a safe value by stray inductance for larger discharge current of snubber circuit. On the other hand, peak value of the discharge current should not exceed maximum device ratings at turn-on. Peak current can be

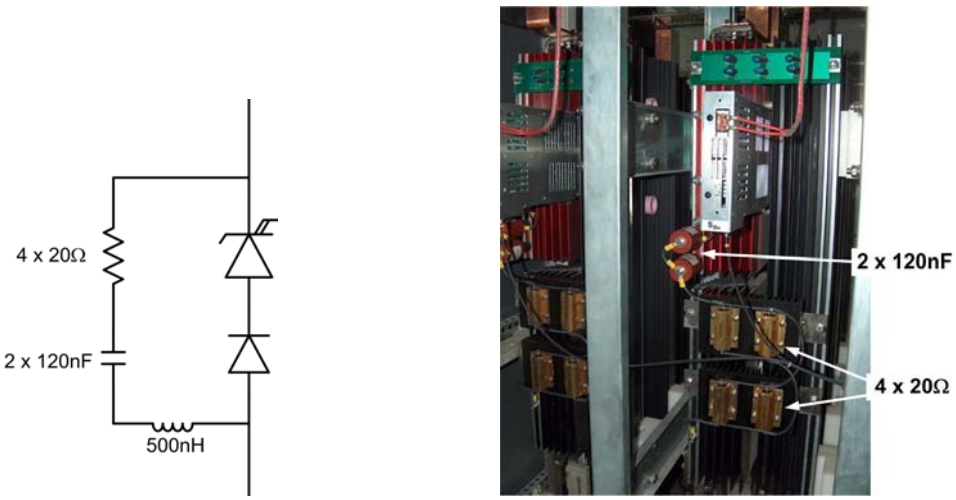
limited only by the snubber resistor therefore, its value should be chosen carefully.

vi. In the tail phase of IGCT turn-off, because of its carrier lifetime engineering, device current tends to cease sharply resulting in an extra overshoot in anode-cathode voltage waveform of IGCT owing to in the inductance commutation path (Fig.4.5), [79]. This overshoot can be limited to certain extent by transferring part of the extra energy in the commutation inductance to the snubber circuit. In order to act the snubber more rapidly, R and L values slightly lower than those chosen in view of iii-v and C value slightly higher than that chosen in view of i-ii.

In view of above discussions and by considering standard snubber resistance and capacitance values, snubber parameters are chosen to be C=240nF, R=5Ω and L=400nH.

3.7.2.5 Experimental Verification of Snubber Performance

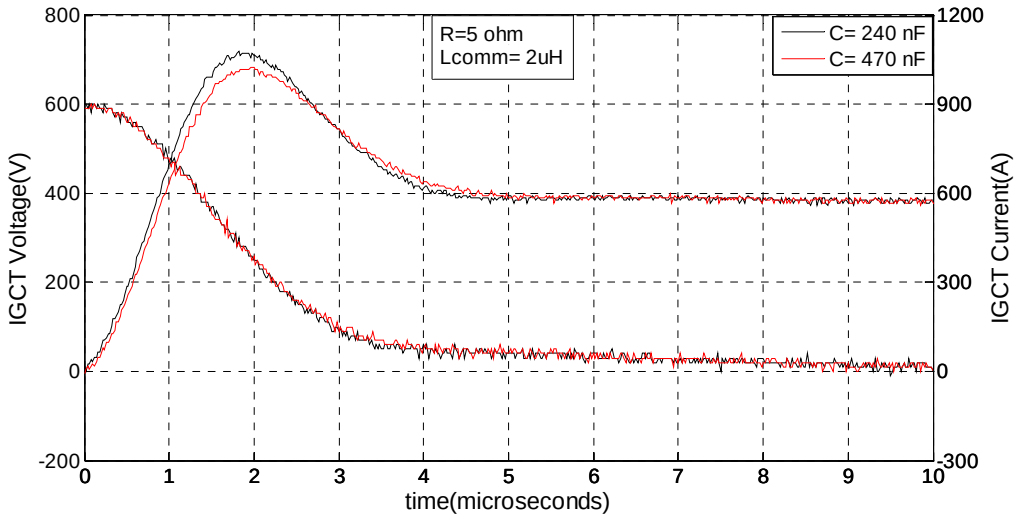
The implemented snubber circuit is as given in Fig.3.46. Its stray inductance L_{cl} is measured to be 500nH.



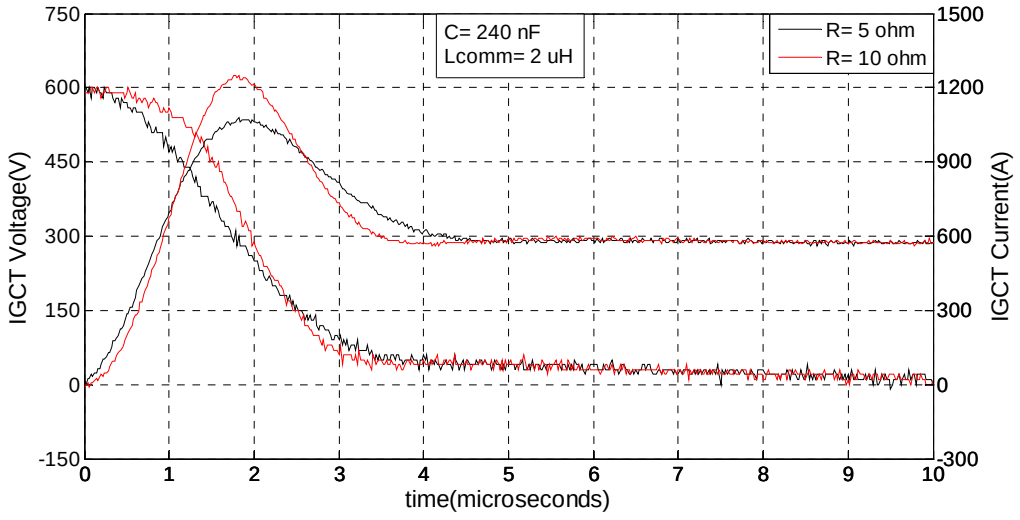
(a) (b)

Figure 3.46 View of implemented snubber circuit (a) its circuit diagram (b) picture

In order to verify the theoretical findings described in Subsections 3.7.2.1-3.7.2.2, the snubber performance has been tested in laboratory for two different values of snubber capacitor and snubber resistance by using the test setup in Fig.3.9. IGCT voltage during forced turn-off are given in Fig.3.47 and the diode voltage during load turn-off are given in Fig.3.48.

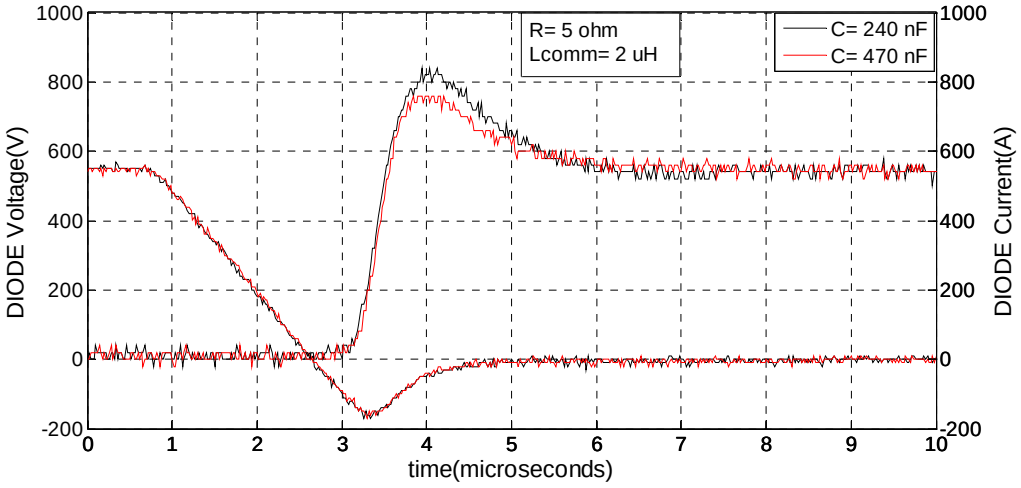


(a)

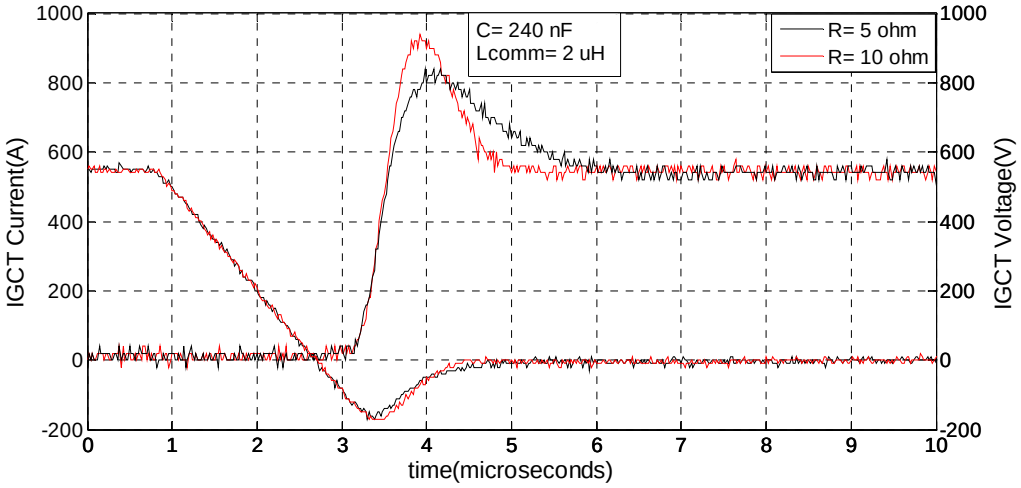


(b)

Figure 3.47 Experimental verification of snubber performance during forced turn-off of IGCT (sampling rate: 50MS/sec)
(a) effects of snubber capacitance L_{cl}=500nH, R=5Ω,
(b) effects of snubber resistance L_{cl}=500nH, C=0.24μF



(a)



(b)

Figure 3.48 Experimental verification of snubber performance during load turn-off of diode (sampling rate: 50MS/sec)
(a) effects of snubber capacitance L_{cl}=500nH, R=5Ω,
(b) effects of snubber resistance L_{cl}=500nH, C=0.24μF

A comparision between experimental and theoretical results shows that there are good correlation between them in verifying the design of the snubber circuit. The performance of the implemented snubber is obtained in the field for actual operating conditions and the resulting waveforms will be given in Chapter 4.

3.8 Design of Protection Circuits

CSC based STATCOM should be equipped with several protection circuits., Some of these protection circuits are characteristic to only CSC based STATCOM. The protection circuits are given on the circuit diagram of CSC based STATCOM in Fig.3.49 and will be briefly described in the subsequent sections.

3.8.1 Standard Protection Relays

The standard protection relays, which are common to other Static Var Compensators, are used in CSC based STATCOM. These relays are marked as ①-④ in Fig.3.49. The operating voltage is specified in the range (28.5kV – 36kV) for the 31.5kV bus [66] and 31.5kV bus voltage may exceed this range in the case of fault in the power system. For these situation, STATCOM system must be disconnected from the system. Otherwise, system components at 31.5kV may be destroyed in case of over voltage, or misoperation may occur in case of low voltage. Therefore, “Over / Low Voltage Protection Relay” has been used.

Due to any fault in 31.5kV system components, such as measurement transformers, cables, or coupling transformer, an over-current may flow through them. In order to protect them from these over-currents, STATCOM system has been equipped with “Over Current Protection Relay”. This relay acts for faults not only at 31.5kV side but also 1kV side. Both “Over / Low Voltage Protection Relays” and “Over Current Protection Relay” trip the circuit breaker at 31.5kV. As will be discussed later, these trip signals first stop CSC and then trip the circuit breaker at 1kV prior to tripping circuit breaker at 31.5kV.

When the power system voltage decreases, STATCOM may inject reactive current higher than its ratings in the case where the current limit does not act, or due to any fault in the system components at 1kV side an over-current may flow. In these cases, “OverLoad Protection Relay” trips the circuit breaker at 1kV side to disconnect the system from the suppy.

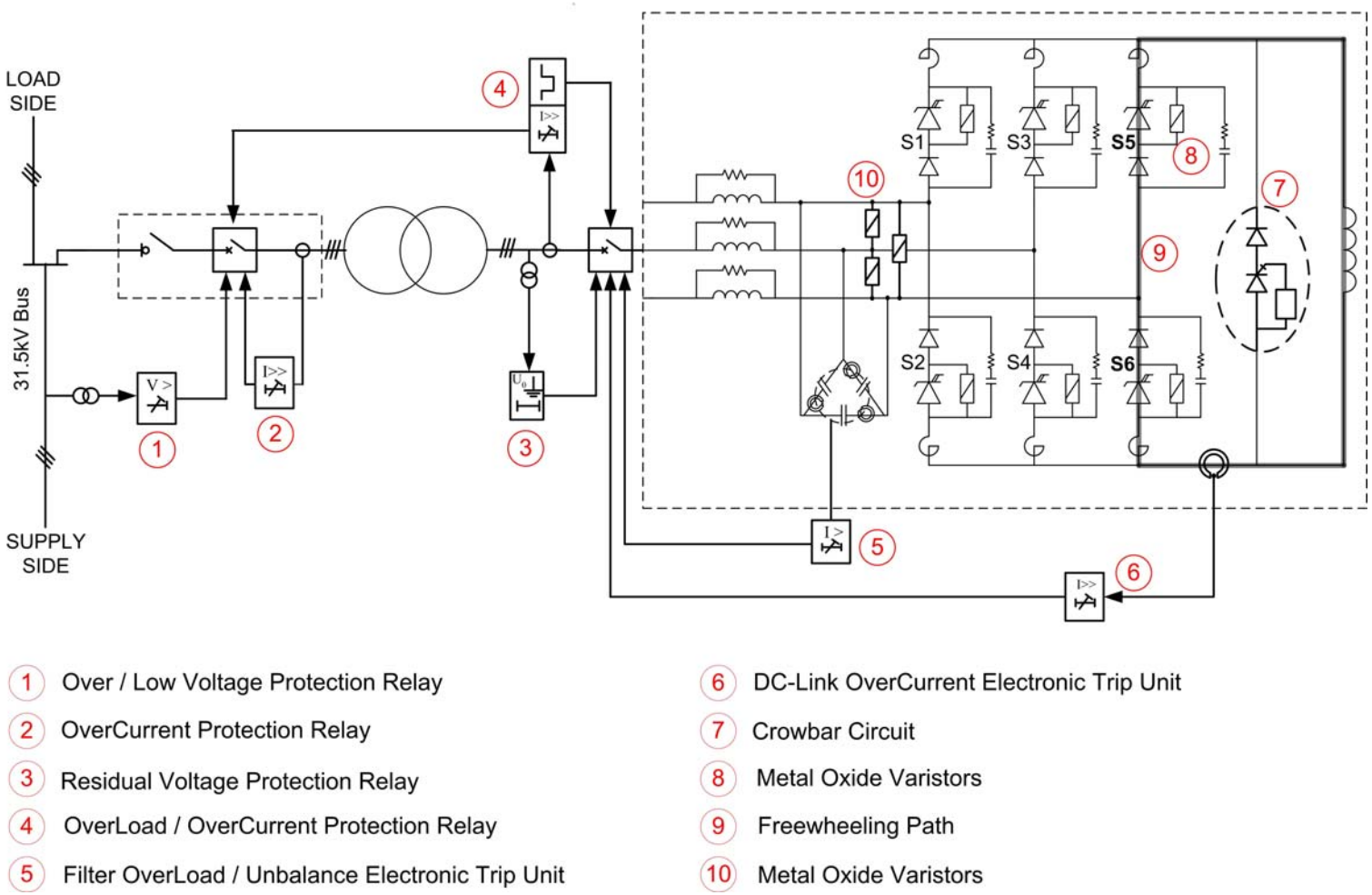


Figure 3.49 Block diagram of protection circuits in CSC based STATCOM

Since the neutral point of coupling transformer has been isolated from earth, earth fault can only be detected by the “Residual Voltage Protection Relay”. The “Residual Voltage Protection Relay” monitors the sum of phase voltages at 1kV and in case of any earth fault at 1kV, this sum deviates from zero. In this condition, it only trips the circuit breaker at 1kV.

3.8.2 Electronic Trip Units

The “Electronic Trip Units” are marked by ⑤ and ⑥ in Fig.3.49. These protection circuits are designed on PCB and located into the electronic control unit of CSC. Input filter capacitors are protected by an electronic protection circuit. Although standard protection relays are avaliable, they can be operated with a conventional voltage and current transformers, which have limited frequency bandwidth (i.e, below 1kHz). Since the currents through the capacitors have the significant harmonic components around and above 1kHz (i.e, significant 17^{th}, 19^{th} harmonics), these conventional current transformers are not suitable for the protection of these capacitors. Therefore, using hall effect current transformers in the capacitor banks as shown in Fig.3.49, an electronic circuit has been designed for monitoring the fundamental component and total rms value of the current through the capacitors. This electronic unit takes the sum of the waveforms of fundamental components of the currents in all phases in delta-connected capacitor bank. If this sum is greater than the tripping value for a few seconds, the circuit breaker at 1kV is tripped for “Filter Unbalance Protection”. Beside the fundamental components, total rms of each current in delta-connected capacitor banks is calculated and compared with the tripping value. As soon as any of the total rms value exceeds the tripping value, the circuit breaker at 1kV is tripped for “Filter Overload Protection”.

The other protection inserted into the electronic control system of CSC is “DC-Link Ove rCurrent Protection”. As given in Fig.2.31c, dc-link current may reach 20kA theoretically for the large phase angle. This value is far from the maximum controllable turn-off current rating of IGCTs. For this reason, dc-link current should be sensed accurately without any delay and saturation. This can only be done with Hall Effect Current Transducers, as shown in Fig.3.49. Due to the presence of dc-

link reactor, the rate of rise of dc-link current would not be instantaneous and it takes a few miliseconds to reach maximum short circuit current in dc-link under loss of control. Therefore, an over-current can be detected within tens of microseconds time by the use of a Hall Effect Current Transducer which has a fast response time and a custom fast acting electronic trip circuit. Since the rated current of CSC is 800A, the tripping value is adjusted to 1200A which is much smaller than rated IGCT current of 4kA. As soon as the tripping value is detected in the dc-link current, "DC-Link Over Current Electronic Trip Unit" stops the operation of CSC and trips the circuit breaker at 1kV.

3.8.3 Metal Oxide Varistors

The metal oxide varistors (MOVs) are known as fast acting transient over-voltage suppressors. They are connected across the IGCTs and across the filter capactiors. When there is an over-voltage across these MOVs, they behave like a short circuit absorbing the energy which otherwise would cause an over-voltage for a short time. Since they are cheaper than the filter capacitors and IGCTs, they are useful in transient over-voltage protection.

If the circuit breaker at 1kV is tripped before stopping CSC, the energy stored in dc-link reactor may charge the input capacitors beyond their voltage rating. Moreover, any surge voltage from the power network due to lightning, switching of circuit breakers, may result in over-charge of filter capacitors. In case of these fault conditions, MOVs rated at 1.1kVrms are connected across the filter capacitors.

IGCTs experience over-voltages during forced turn-off, as described in previous sections. Although these over-voltages are under control by the design of snubber circuits and control system, over-voltage protection circuits, including seriesly connected MOVs to achive 3600Vpeak, are connected across each IGCTs. This protection provides a life guard for IGCTS in a short time of period during a fault, such as dc-link overcurrent.

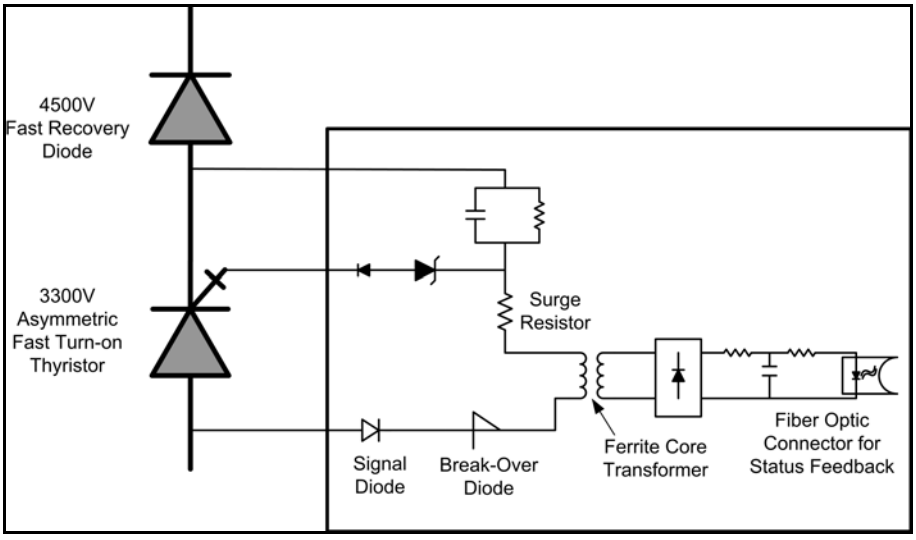
3.8.4 Crowbar Circuit

If a sudden interruption occurs in the dc-link current then dc-link voltage theoretically tends to go negative. Possible causes of dangerous voltage production are commutation failure in CSC, semiconductor/s failures, broken connections on the dc-side and lightining surges incident on the outdoor type air-core dc-link reactor.

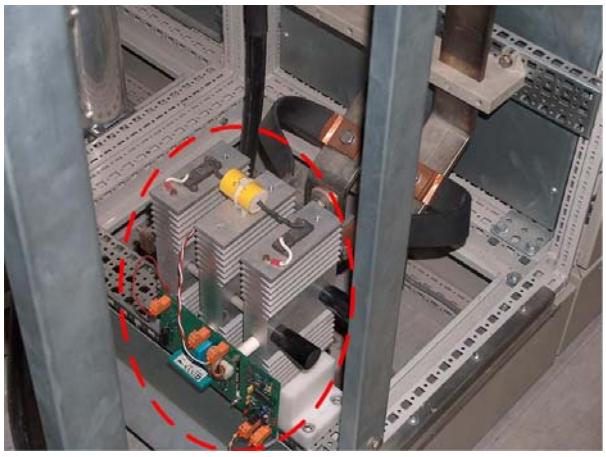
The overvoltage production can be eliminated or at least restricted by providing a closed return path to the dc-link current by the use of a rapidly acting auxilliary circuit. The most favorable circuit for medium voltage applications is known as the crowbar circuit in the literature. In this application, a proper crowbar circuit with unidirectional operating capability has been designed, implemented and connected across the output dc terminals of CSC. It is as shown in Fig.3.50. For higher dc-link voltage levels more than one seriesly connected crowbar semiconductors can be used. It is composed of a 3300V asymmetric fast turn-on thyristor (Dynex-ACR300SG33), 4500V fast recovery diode (Dynex-DSF8045SK) and a self-triggering mechanism. The threshold value for overvoltage protection is adjusted to 3000V by the use of IXYS BOD30 breakover diode. Since the crowbar circuit should act rapidly asymmetric thyristor/s should be used because of their superior dv/dt (3000V/μsec) and di/dt (2000A/μsec) ratings in comparison with conventional thyristors. Since the IGCTs used in this application can turn-on within a microsecond time the dv/dt across the dc-link and hence the crowbar circuit can be not more than 1000V/μsec. This would lead to misfiring if conventional thyristors are used in crowbar circuit. When the crowbar semiconductor is turned on di/dt of the semiconductor current becomes large thus restricting semiconductor types that can be used in crowbar circuits. Among candidate power semiconductors (asymmetric IGCT, HV-IGBT, asymmetric fast turn-on thyristor) the most favorable device is the asymmetric fast turn-on thyristor because it has inherent latching capability once triggered into conduction.

When the anode-cathode voltage of asymmetric thyristor tends to exceed the threshold value of 3000V, breakover diode turns on and self-triggering circuit sends

a firing pulse to asymmetric thyristor. The self-triggering circuit permits the application of a high triggering current (10A) to the gate of asymmetric thyristor to maintain triggering of thyristor at high di/dt. The status feedback circuit integrated into the self-triggereing circuit detects the operation of the crowbar and sends a signal to the control circuit via fiber optic cable. Upon the receipt of status feedback signal indicating crowbar operation control circuit blocks IGCT triggering pulses except those for freewheeling operation and at the same time sends a trip signal to 1kV circuit breaker.



(a)



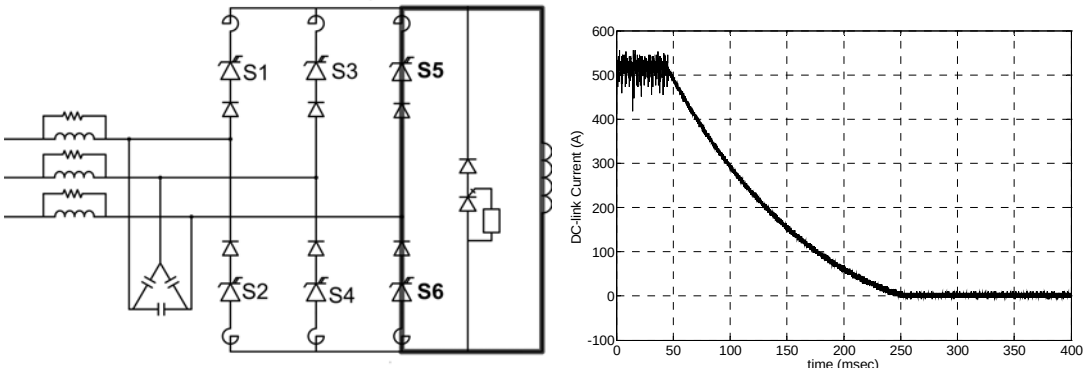
(b)

Figure 3.50 (a) Crowbar circuit diagram, (b) picture of implemented crowbar circuit, encircled by red dashed line

3.8.5 Non-Repetitive Freewheeling Operation

The Current Source Converter based STATCOM can be stopped successfully only by discharging entirely the dc-link reactor under normal or abnormal conditions. Upon the receipt of stop command the control circuit turns on S5 and S6 and blocks other switches. S5 and S6 provides a close return path to the dc-link current as illustrated in Fig.3.51a and kept in conduction for a period of 2sec.

Since the time constant of dc-link current is τ_{dc}=0.15sec, 1 seconds pre-programmed conduction time is quite enough to discharge to discharge dc-link reactor entirely as shown in Fig.3.51b.



(a) (b)

Figure 3.51 (a) illustration of freewheeling path (b) dc-link current waveform during freewheeling operation through freewheeling path (sampling rate: 250kS/sec)

3.9 Design of Control System

The control system of CSC based STATCOM includes the reactive power control, switching signal generator, fault monitoring circuit and protection circuit. Design of protection circuit has already been described in Section 3.8. Design of reactive power controller and switching signal generator will be presented in this section.

3.9.1 Design of Reactive Power Controller

Since SHEM will be used with fixed modulation index (Section 3.3), the reactive power control is achieved by controlling dc-link current via phase angle, which is the only control input variable. Instead of advanced controllers (e.g., fuzzy-logic, sliding mode controller) and modern complicated controllers (e.g., pole placement with state feedback controller or phase lead-lag compensators), more simple industry-standard PI controller based approach has been chosen in the reactive power control of CSC based STATCOM. As proposed in Chapter 2.4, the block diagram of control system based on converntional PI controllers is given in Fig.3.52. There are two control loops: the inner loop controls dc-link current while the outer loop controls reactive power.

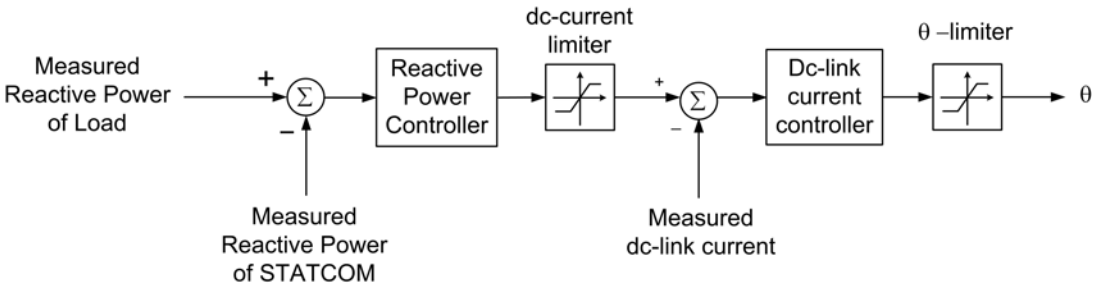


Figure 3.52 Block diagram of reactive power control loop for CSC based STATCOM

The reactive power generated by CSC is directly dependent on dc-link current as discussed in Chapter 2.3. Therefore, according to the difference between the calculated total reactive power demand and the total reactive power generated by STATCOM, power controller in the outer loop calculates a reference for dc-link current. Then, current controller in the inner loop generates the phase angle for switching signal according to the difference between the reference and the actual value of dc-link current.

Reactive power control can also be achieved without the use of inner dc-link current control loop. For this case, phase angle could be generated directly by the reactive power controller at the expense of uncontrolled current flow in the dc-link.

If the reactive power demand of loads increases then the reactive power controller tends to increase the phase angle, which may overloading not only the dc-link reactor but also IGCTs. In other words, against rapid changes in reactive power demand dc-link current could be increased rapidly and in an uncontrolled manner to meet this demand thus exceeding the current ratings time to time.

There are two limiters included in the control loop as shown in Fig.3.52. The reference for dc-link current should be limited according to considerations above. Then, the limiter for phase angle becomes redundant in theory. However, it is very useful in case of failure in hall-effect transducer of dc-link current at the expense of slightly longer transient response.

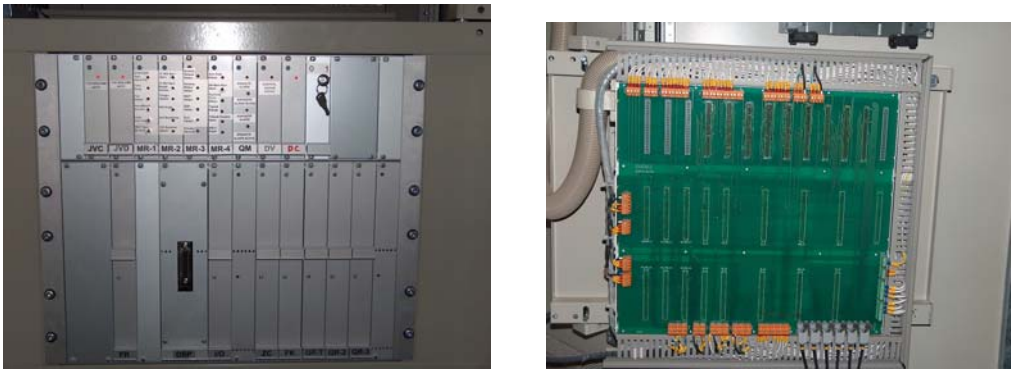
Determination of parameters for PI controllers for CSC based STATCOM is not very easy due to non-linearities in CSC as given in Chapter 2.4. Instead of these, it is more practical to use Ziegler-Nichols rules for tuning parameters of PI controllers [87].

As explained in Chapter 2, there is a discontinuity in transition from capacitive operation of CSC to inductive operation or vice versa. During this transition, dc-link current should be made zero in the perivious operation mode of CSC by setting the reference dc-link current to zero. This is also proposed in [59] for the reactive power control of CSC based STATCOM where phase angle is only the control variable. Although this seems to present a significant delay in the reactive power control, the regeneration capability of CSC provides fast discharge of dc-link current.

The reactive power control controller has been implemented on a TMS320LF2407A DSP microcontroller. The sampling period of both reactive power controller and dc-link current controller is approximately 3.33msec, which is determined by the zero-crosses of supply line-to-line voltages. The measured variables such as reactive power of load and STATCOM, and the dc-link current are also sampled and avaraged within the sampling period of the controllers. The flowchart for the reactive power control is given in Appendix E.

3.9.2 Design of Electronic System

The picture of electronic system is presented in Fig.3.53. Electronic system is composed of PCBs mounted on a common motherboard. The block diagram of the electronic system is given in Fig.3.54.



(a) (b)

Figure 3.53 Picture of electronic system for CSC based STATCOM
(a) front view (b) view of motherbard

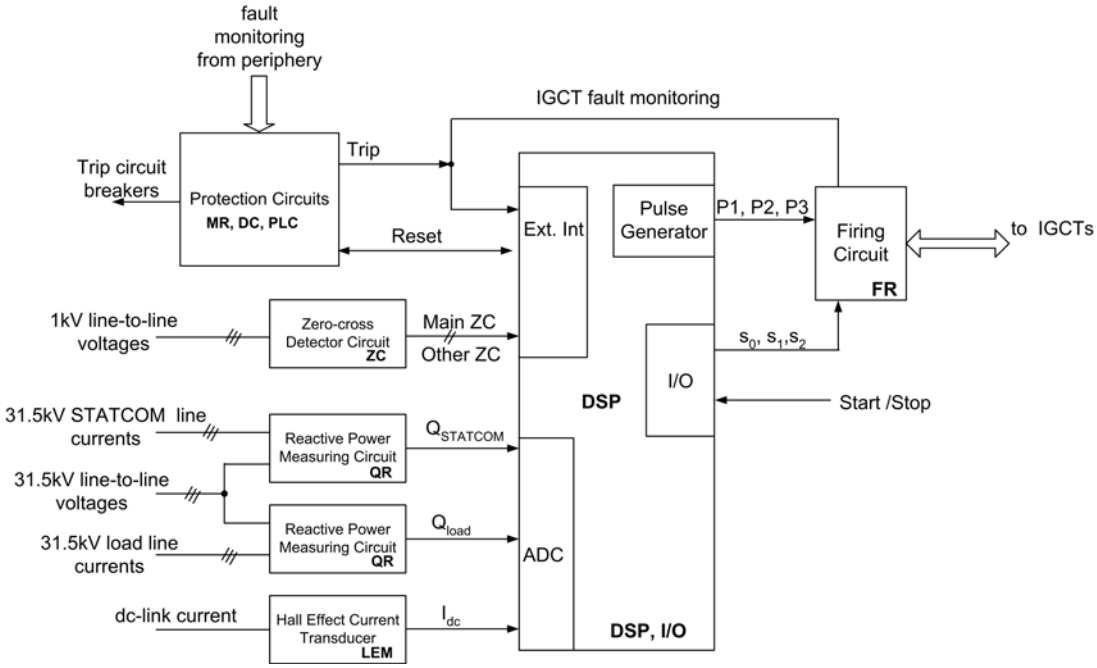


Figure 3.54 Block diagram of electronic system

Reactive power controller and switching signals are all implemented on TMS320LF2407A DSP microcontroller. For the sake of simplicity, evaluation board of TMS320LF2407A has been used and mounted on an interface PCB as shown in Fig.3.55. As described in Chapter 2.4.1, switching patterns in each [0,π/3] interval in Fig.2.16 are same with the other intervals in Fig.2.17, but are applied to different IGCTs according to the interval. These intervals are determined by the zero-crosses of line-to-line voltages. These common switching pulses are generated by DSP as P1, P2, P3. Then, the application of these pulses to IGCTs are determined by the signals, s_0, s_1, s_2. The multiplexer chips on the firing circuit distribute the pulses, P1, P2, P3 to the corresponding IGCTs according to the signals, s_0, s_1, s_2. The generation and distribution of switching pulses are described in Fig.3.56. The generation of pulses of P1, P2, P3 starts over at each zero-cross of line-to-line voltages. After the last pulse of P1, P2, and P3 is reached their last state is sustained until the next zero-cross. The counter is incremented by one at each zero-cross and reset to its initial value after receiving main zero-cross, as shown in Fig.3.56. The number in the counter describes the intervals in Fig.3.57. The counter outputs the number in binary format in terms of signals s_0, s_1, s_2.

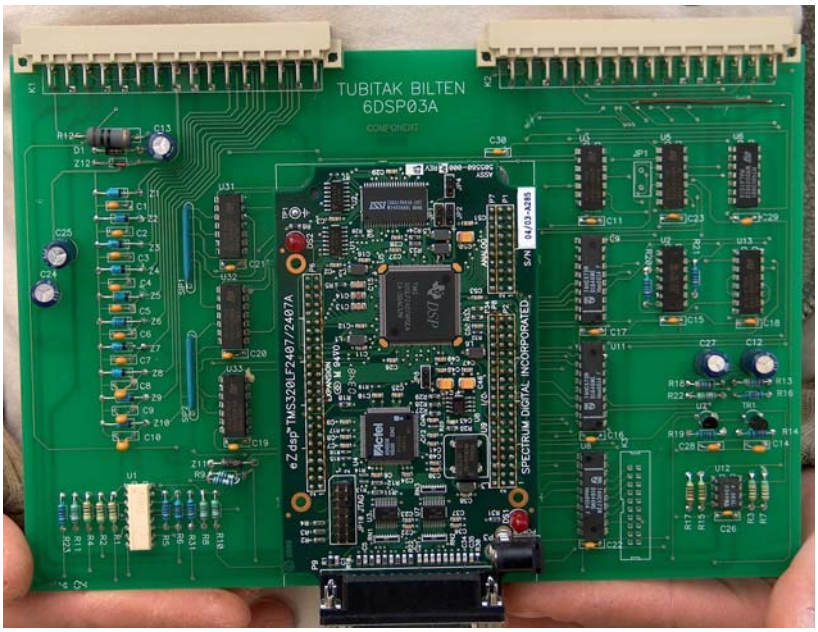


Figure 3.55 Picture of evaluation board of TMS320LF2407A with its interface PCB

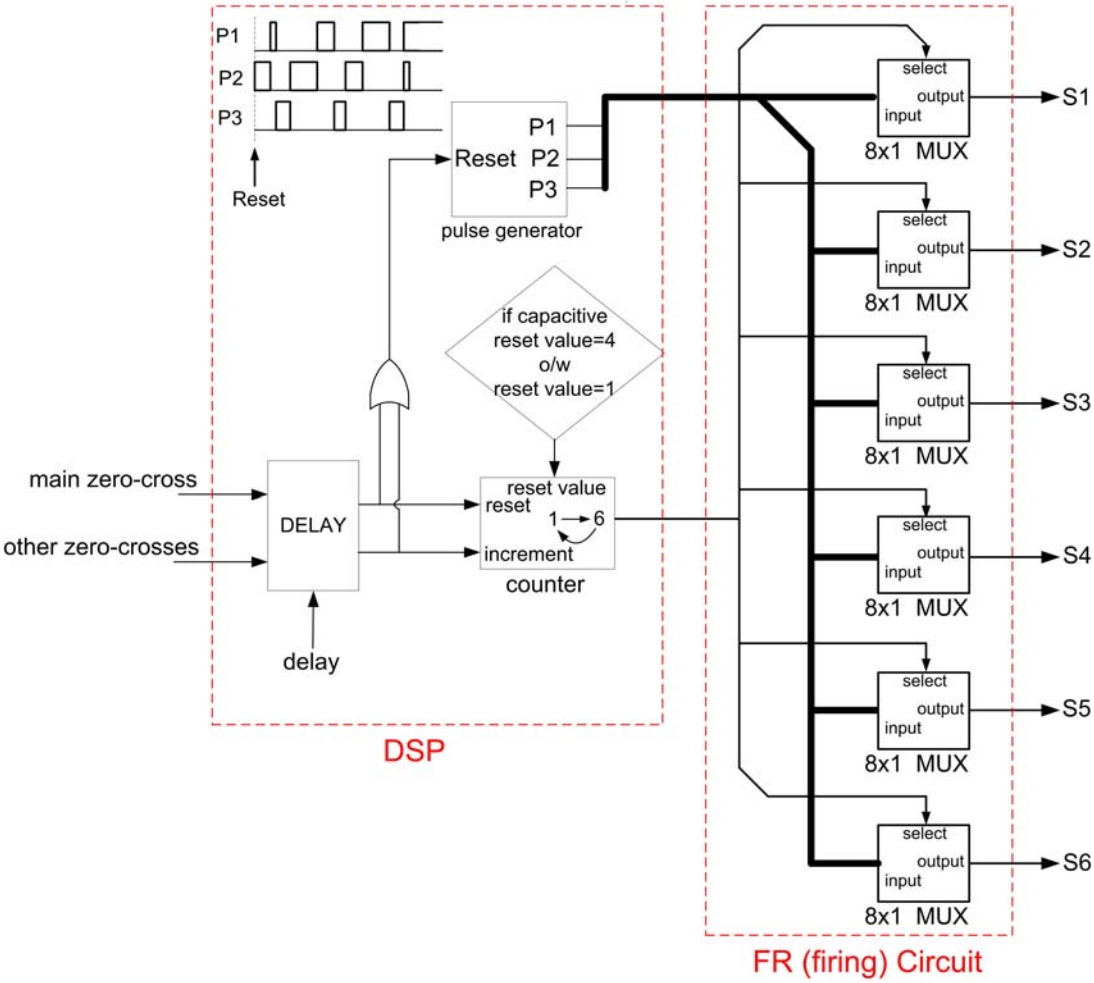


Figure 3.56 Block diagram for generation of switching signals

The control of phase angle can only be achieved by delaying the start of switching pulses, P1, P2, and P3 with respect to zero-crosses since pre-delay is not possible in real time processing. Therefore, the zero-crosses of line-to-line voltages are adjusted in advance to their actual zero-crosses as shown in Fig.3.57. As described in Chapter 2, continuous control of phase angle during switching from inductive reactive power generation to capacitive reactive power generation is not possible due to large amount of power flow to the dc-link. Therefore, a discontinuity is added to the counter, such that the initial value of the counter is 1 for the inductive operation of CSC and 4 for the capacitive operation of CSC.

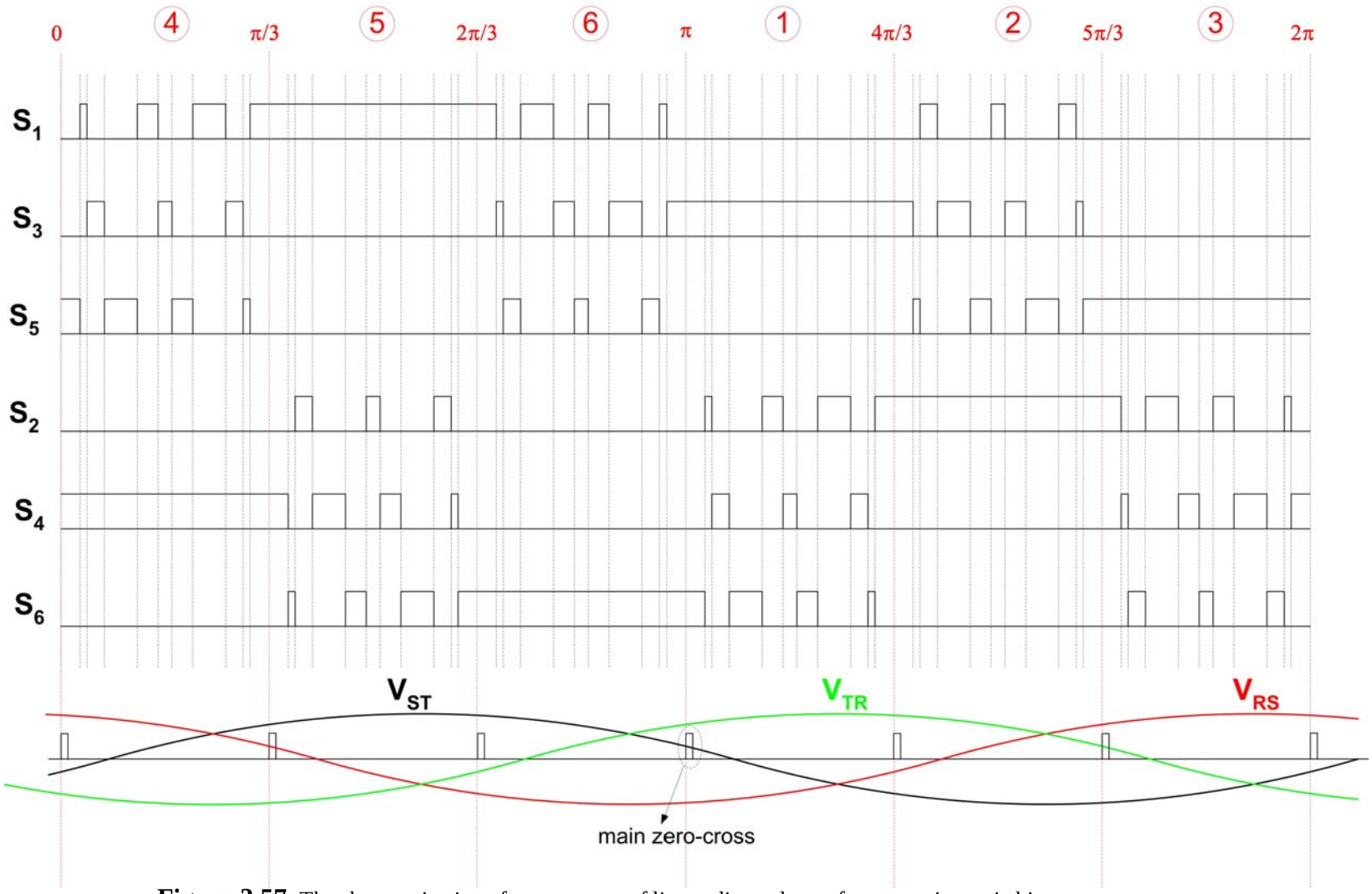


Figure 3.57 The characterization of zero-crosses of line-to-line voltages for generation switching patterns

As can be understood from Fig.2.3, delay is decreased in order to increase the phase angle and the magnitude of phase angle is limited with the difference between the adjusted and actual zero-crosses of line-to-line voltages for inductive operation of CSC. On the other hand, the delay should be increased from adjusted zero-cross beyond the actual zero-cross in order to increase phase angle, hence reactive power in capacitive operation of CSC. This can also be understood from Fig.2.5.

The switching pulses are sent to IGCTs via fiber optic cable. The fiber optic connectors are mounted on motherboard as shown in Fig.3.53b. The gate drive of each IGCT also sends a status feedback signal via fiber optic cable. These signals are evaluated for the monitoring any failure in IGCTs.

There are two identical reactive power measuring circuit, one for load and one for STATCOM. Reactive power measuring circuits calculates the required three phase total reactive power via analog circuits. For this purpose, there are three analog multipliers, each of which multiplies line-to-line voltage with current in the irrelevant line. Output of each multiplier is integrated over a half cycle of supply frequency. At the zero-crosses of the line-to-line voltages, output of the corresponding integrator is sampled and stored to a capacitor, then the integrator is reset. Then, the voltages across the capacitors are added to obtain three phase total reactive power. With this implementation, only the required reactive power component at supply frequency can be measured. It should be noted that the change in reactive power of either load or STATCOM can be measured with a delay of nearly 20msec.

Zero-cross detector circuit generates pulses 900μsec (i.e., corresponds to 16.2° at 50Hz supply frequency) before the zero-crosses of 1kV line-to-line voltages. With respect to these pulses DSP introduces a delay in starting of switching pulses as discussed above.

The rest of the circuits in the electronic system are used for protection and fault diagnosis. There is a Programmable Logic Controller (PLC) for coordination between the electronic system and the operator panel. It also carries out the temperature monitoring and speed control of variable frequency driven fan system in low voltage container.

3.10 Discussion on the Maximum Utilization of CSC based STATCOM

Although the design work has been carried out for 500kVAr CSC based STATCOM at 1kV, the power rating of the resultant system can be further increased to some extend by utilizing capabilities of system components. The maximum controllable turn-off current of IGCT is 1500A at 500Hz, which is imposed by the maximum power consumption of its gate driver. Then, mean value dc-link current can be increased to 1500A. Moreover, the modulation index value can be used as 0.9 in order to increase the magnitude of fundamental component of converter line current for the same dc-link current at the expense of reduction in the control range of phase shift angle. It is therefore found from the simulations that CSC can produce 2.6MVAr capacitive reactive power and 960kVAr inductive reactive power at system voltage level of 1kV. Meanwhile, the overall STATCOM system can produce 2MVAr capacitive reactive power and 1500kVAr inductive reactive power. It should be noted how the input filter design affects the reactive output capacity of CSC based STATCOM. This can also be understood from the simulation results which show that the rms value of line-to-line voltage at the input terminal of CSC is 1560V at 2.6MVAr capacitive -and 580V at 960kVAr inductive reactive power generation of CSC. This result is due to the effects of filter reactor, which causes poor voltage regulation at higher reactive power generation of STATCOM system.

While increasing the maximum controllable turn-off current of IGCT for maximum utilization of CSC, dynamic overvoltage across IGCT during forced turn-off should be checked whether it is above the maximum repetitive peak value turn-off voltage of IGCT (i.e, 4500V). For this purpose, the simulation model given in Section 3.7.2 is used with the maximum peak value of line-to-line voltage and dc-link current, 2500V and 1500A, respectively. It should also be noted that the most important parameter is the value of commutation inductance in designing turn-off snubber. In order to fully utilize the maximum di/dt capability of IGCT, commutation inductance is chosen 2.5μH for 2500V and 1000A/μsec. Then, it is found that the maximum IGCT voltage including the overshoot is around 3800V for the snubber components employed in the simulation model of turn-off snubber

(R=5ohm and C=0.7μF). Since the actual snubber parameters are set to 5/3 and 3/5 of the simulation values of R and C respectively, actual snubber components are set to R=10ohm and C=0.47μF as proposed in (3.15). This will result in nearly 400W power dissipation in each snubber circuit.

As the reactive power generation capacity of CSC is increased, the power dissipation of IGCT and diode increases significantly. It means that both natural air cooling and forced air cooling techniques become inadequate for cooling of the converter. The only solution is the water cooling. Typical power stage layout of CSC based on de-ionized water cooling is as shown in Fig.3.58.

(a) (b)

Figure 3.58 Typical power stage of CSC based on water cooling (a) close view of power stage, (b) view of power stage with deoinized water cooling unit

CHAPTER 4

FIELD TEST RESULTS

4.1 Introduction

Using the design principles given in Chapter 3, +/- 500kVAr CSC based STATCOM has been developed at 1kV. In order to verify theoretical results, implemented system has been applied to two different sites of Turkish Coal Enterprises in order to provide group compensation of coal mining excavators, which have the similar load characteristics as explained in Chapter 3.2.

The complete circuit diagram of the developed STATCOM system has already been given in Fig.3.25. The modulation technique of the developed system is SHEM with elimination of 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic at a fixed modulation index of 0.8. The reactive power control of the developed system has been achieved by the control of phase shift angle ϕ as explained in Chapter 3.9.

During the field tests, performance of the developed system has been tested at different operating conditions and various characteristics of CSC based STATCOM have been obtained. In this Chapter, these characteristics obtained from these field tests will be presented. Field test results include the records taken from the developed system for the worst operating cases and illustrations derived from the results of several records.

The records have been obtained by the measuring apparatus, which are listed in Table 4.1. Two different oscilloscopes have been used. Theses are 500MHz oscilloscope (TDS5054) from Tektronix and 300MHz oscilloscope (WaveJet 324) from Lecroy. The later one has the data acquisition capability of 500K samples whereas the former has 100K samples. High voltage measurements have been made by using differential high voltage probes such as DP100 from Pintek and P5210 from Tektronix. Since P5210 is an active probe which is supplied by TDS5054 it has

been used together with TDS5054. On the other hand, DP100 which is supplied by its isolated power supply from 220VAC has been used with WaveJet 324. Voltage signals smaller than 100V were recorded by signal probe (P5050) from Tektronix so that the signal can be measure accurately. Not only ac currents in the system but also the currents through power semiconductors were measured by Rogowski coils. Rogowski coil is an electrical device for measuring AC currents or high current pulses. Since a Rogowski coil has an air core unlike other types of current transformers, it does not saturate and can respond to fast-changing currents. Bandwidth of the Rogowski coils is approximately 16MHz. It is supplied either from a battery or a 220V ac power supply. Variations in active and reactive power have been measured with the use of data acquisition system. The current waveforms are acquired via current probe (80i-110S) from Fluke through associated current transformer and voltage waveforms are taken with the use of divider in terms of resistors. The data acquisition system samples voltage and current waveforms at a sampling rate of 3200kS/sec. Ferrite beads in different sizes have been used for the measuring devices supplied from power supply in order to suppress common mode noise in the measurements.

In this Chapter, first current and voltage waveforms of power semiconductors in steady –and transient-state will be given in order to verify the design criteria and demonstrate operating characteristics of CSC based STATCOM. Then, the compliance of the developed system with the corresponding standards will be shown both by the records obtained for the maximum operating conditions and the results obtained at various operating conditions. The efficacy figure of the developed system will then be defined on the basis of the variations in power loss against reactive power produced by the system. Typical records of state variables of CSC based STATCOM on both AC and DC sides will be presented at maximum operating conditions in order to verify the design work and show the operating principles of CSC based STATCOM. After that the performance of CSC based STATCOM in reactive power control will be evaluated by the records obtained from the transient –and steady-state responses to the different types of reactive power demands.

Table 4.1 List of measuring apparatus

– Tektronix TDS5054 Digital Phosphor Oscilloscope
– LeCroy WaveJet 324 Oscilloscope
– Pintek DP100 High Voltage Differential Probe (100MHz)
– Tektronix P5210 High Voltage Differential Probe (50MHz)
– Tektronix P5050 Passive Voltage Probe (500MHz)
– LEM LT 1005 S Hall-Effect Closed Loop Current Transducer
– Powertek, Rogowski Current Waveform Transducers: CWT 15B, 2mV/A, and CWT 6B, 5mV/A
– Data Acquisition System: National Instruments DAQ 6062 E Data Acquisition System National Instruments SC2040 Sample and Hold Card Fluke 80i-110S AC/DC Current Probe

4.2 Field Test Results

4.2.1 Current and Voltage Waveforms of Power Semiconductors

Current and voltage waveforms of IGCT and DIODE have been recorded by the use of Rogowski coils and DP100 high voltage differential probes in the field. Two sample records, one for 650kVAr capacitive and the other for 500kVAr inductive reactive power generation of overall STATCOM are given in Fig.4.1 and 4.2 respectively for one supply cycle (20msec).

Since the power semiconductors employed in CSC are self-commutated devices, switching patterns and semiconductor current waveforms are to be the same. A comparison between waveforms in Fig.2.17, Fig.3.7 and Fig.4.1-4.2 shows that the implemented CSC operates successfully. Different than Fig.2.17 and Fig.3.7 there are negative currents in IGCT current waveforms due to reverse recovery of its series diode.

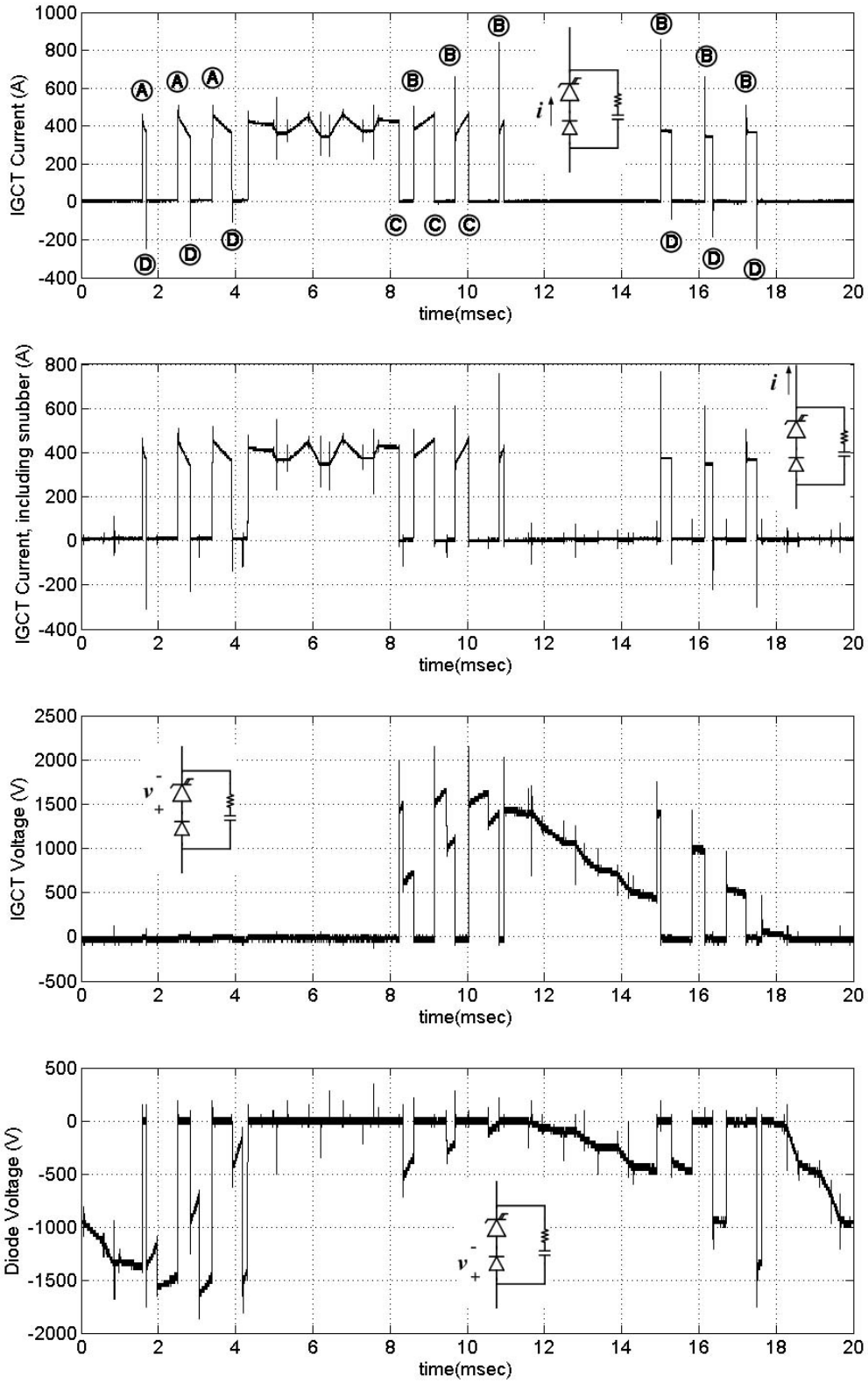


Figure 4.1 Typical voltage and current waveforms of IGCT and Diode, recorded for 650kVAr capacitive reactive power generation of STATCOM (sampling rate= 25MS/sec)

Ⓐ - load turn-on, Ⓑ - device turn-on, Ⓒ - forced turn-off, Ⓓ - load turn-off

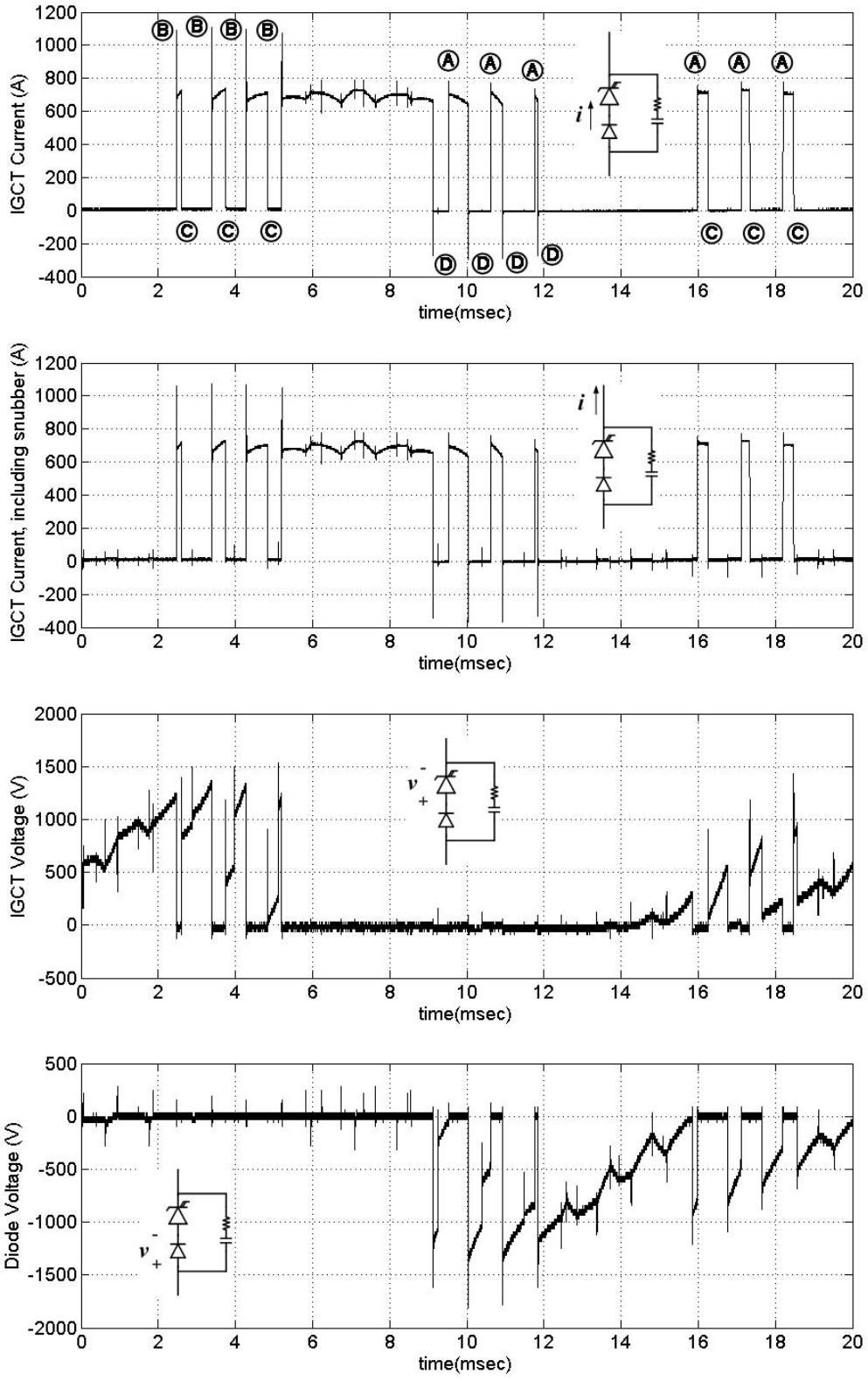


Figure 4.2 Typical voltage and current waveforms of IGCT and Diode for 500kVAr inductive reactive power generation of STATCOM (sampling rate= 25MS/sec)

Ⓐ - load turn-on, Ⓑ - device turn-on, Ⓒ - forced turn-off, Ⓓ - load turn-off

At the instants where the negative current flows through IGCT, there exists a load turn-off (marked by encircled “D” on IGCT current waveforms) and diode blocks the voltage. Current overshoots in IGCT current waveform are due to reverse recovery currents of the diodes on the other phases of CSC and discharge current of its own snubber together with the other snubbers. At the instants of current-overshoots, IGCT undergoes device turn-on (marked by encircled “B” on IGCT current waveforms). From the voltage waveforms of IGCT and DIODE, it is clear that DIODE blocks reverse voltages and IGCT blocks forward voltages. There are over-voltages in IGCT and DIODE voltage waveforms. At the instants where there is over-voltage at turn-off of IGCT it is said to be forced turn-off of IGCT (marked by encircled “C” on IGCT current waveforms). And similarly, at the instants where there is an overvoltage across diode together with negative current through IGCT diode undergoes load turn-off, or equivalently reverse-recovery. It is worth to note that records in Fig.4.2 and 4.3 show the effect of snubber. As stated in Section 3.7.2.4 which is devoted to the design of RC snubber, there is an interaction among the snubbers in CSC. It can be easily observed from the records of IGCT current including/excluding snubber current. While IGCT is in OFF state, there are high frequency ripples in its current waveform, including snubber current. This is due to the turn-off of power semiconductors in other phases, either IGCT under forced turn-off or DIDOE under load turn-off. An interesting observation would be that during ON state of IGCT, these high frequency snubber currents flow through it since same high frequency ripple exists both in pure IGCT current and IGCT current including snubber. There are also high frequency ripples in IGCT and DIODE voltage waveforms. These ripples are due to the flow of snubber current through the di/dt limiting reactors.

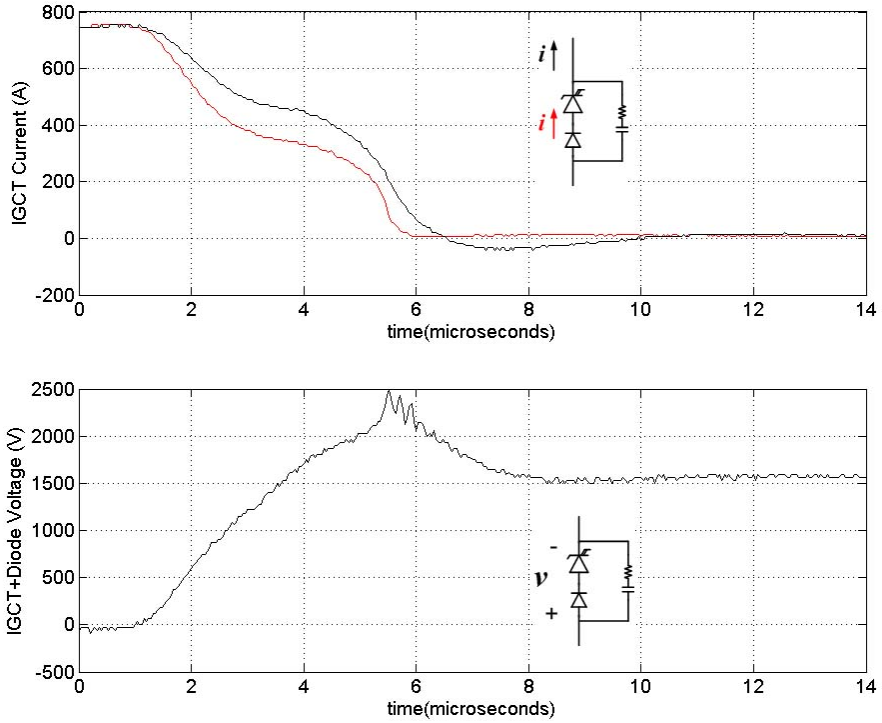
The voltage overshoots in IGCT and DIODE voltage waveforms during turn-off are much lower than their maximum peak repetitive blocking voltage rating, resulting in safe operation.

It is seen from IGCT current waveforms that reverse blocking diode undergoes reverse-recovery six times during one cycle of capacitive mode of operation and four times in inductive mode of operation among ten turn-off. In the remaining turn-off instant, forced turn-off of IGCT occurs.

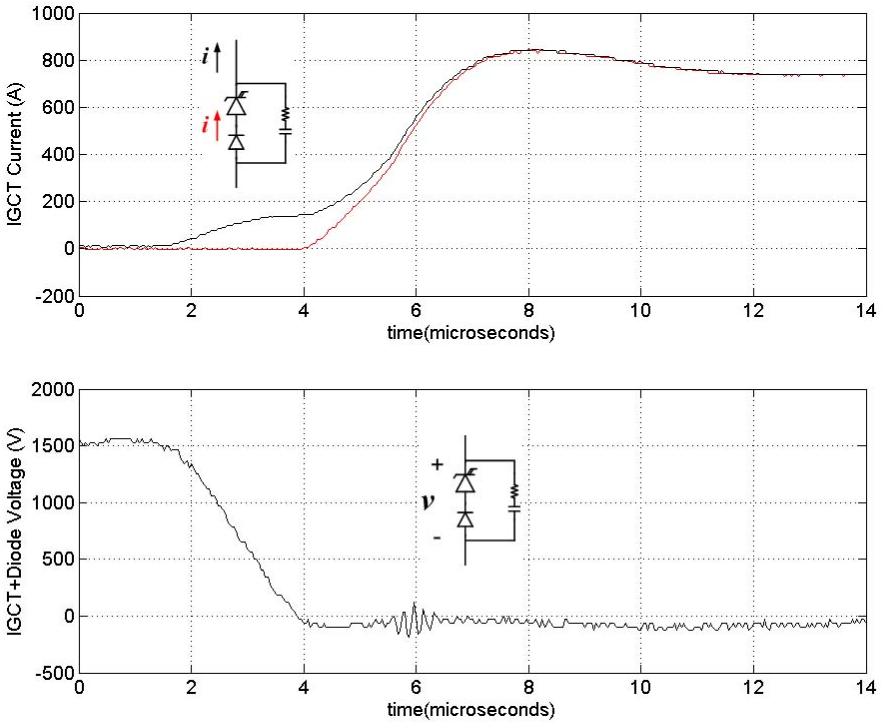
The typical switching waveforms recorded with the use of DP100 and Rogowski Coils during forced commutation and load commutation are given in Fig.4.3 and Fig.4.4 respectively. The waveforms are in consistent with the description of commutation types in Chapter 2.6.

The switching waveforms of outgoing and incoming devices during forced commutation are observed in Fig.4.3. The current of outgoing IGCT can not commutate to the incoming IGCT simultaneously at the beginning of the commutation because incoming device is reverse biased. While current through outgoing device is decreasing, the snubber across incoming device discharges to zero. When it becomes zero, the current starts to flow through incoming device. This results in nearly no power dissipation in IGCT and diode of incoming device. While the voltage across IGCT of outgoing device increases, its current decreases. Therefore, significant turn-off loss occurs in IGCT of outgoing device. There is a defined end in tail current of outgoing IGCT, which presents an extra over voltage. This extra over voltage is limited with the use of successfully designed turn-off snubber.

During load commutation in Fig.4.4, superior turn-on characteristic of IGCT can be observed since its voltage collapses to zero within one microsecond like an ideal switch. This results in relatively lower turn-on losses in IGCT of incoming device. Since di/dt during load commutation relatively is higher than that of forced commutation, forward recovery of diode of incoming device is expected to be observed in Fig.4.4. However, due to the stray inductance in the measuring circuit, it can not be recorded accurately. During load commutation, diode of outgoing device experiences reverse recovery loss because the voltage across the outgoing diode increases and its current decreases to zero, simultaneously. It can be observed from Fig.4.4a, the rate of decrease in current of outgoing diode during its reverse recovery is reduced with the use of turn-off snubber. Therefore, the voltage overshoot across it is limited. It is also observed from Fig.4.4b that the rate of rise in current through incoming IGCT is relatively larger at the beginning of the commutation due to discharge of its snubber. This relatively larger di/dt of current through incoming device is allowable for smaller magnitude of discharge current.

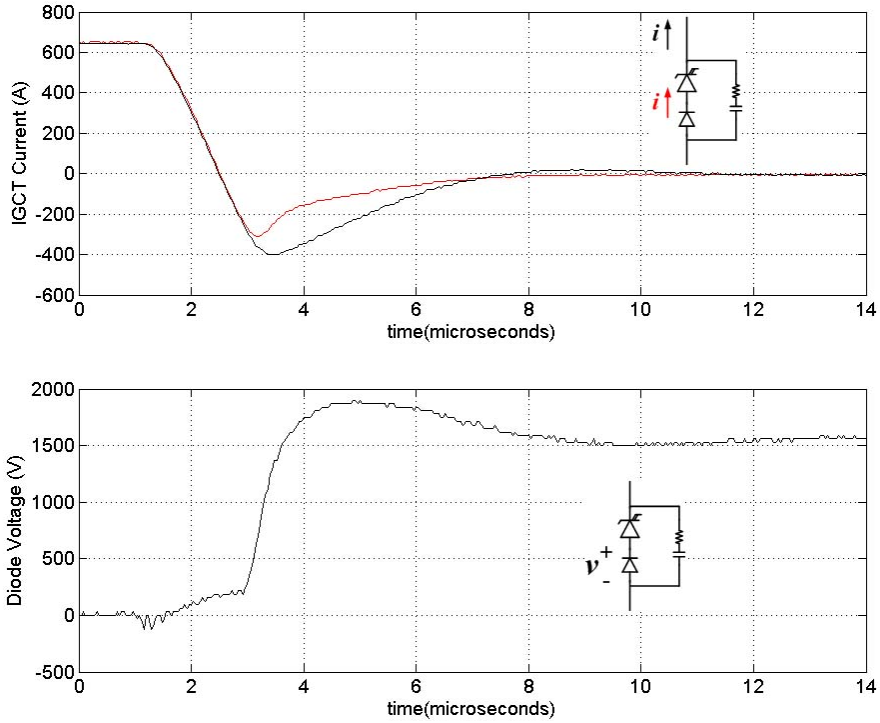


(a) current and voltage waveforms of outgoing device under forced turn-off

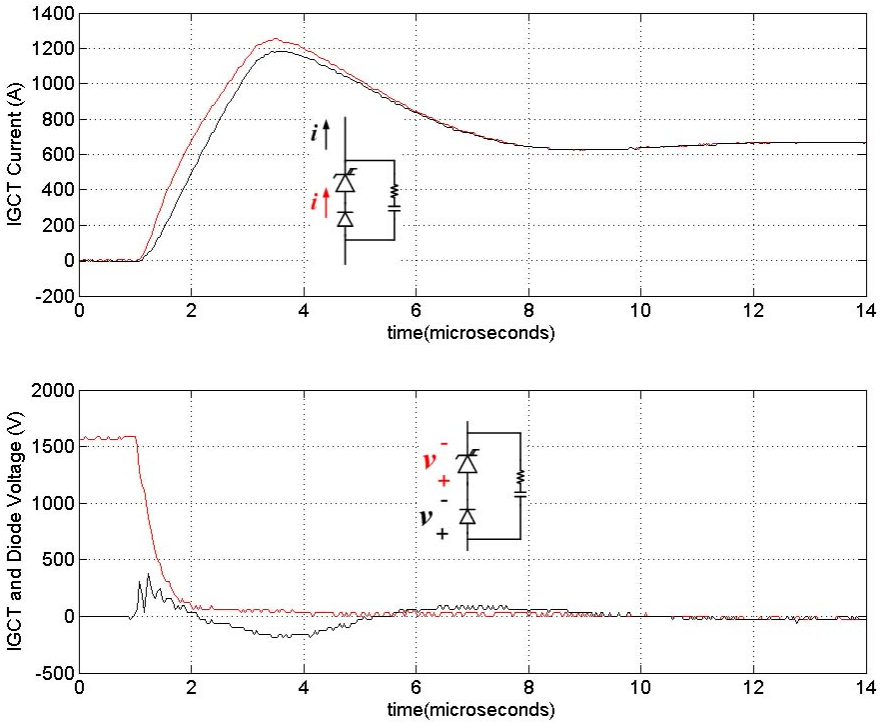


(b) current and voltage waveforms of incoming device under load turn-on

Figure 4.3 Typical voltage and current waveforms during forced commutation (sampling rate= 25MS/sec)



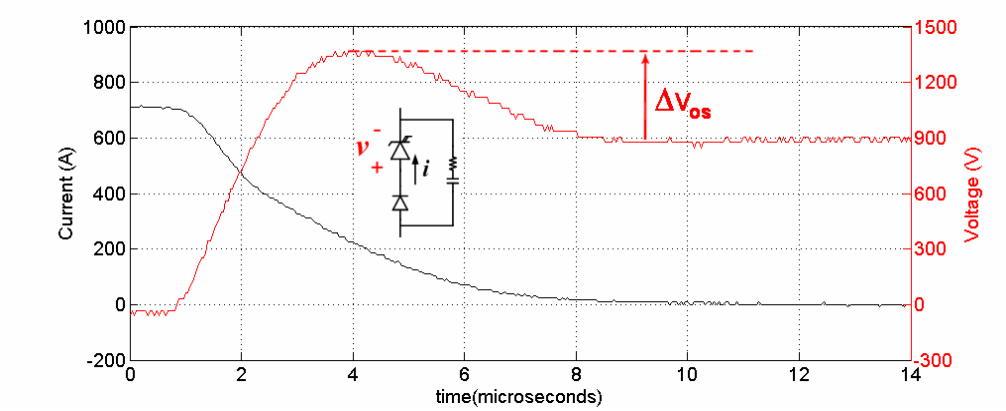
(a) current and voltage waveforms of outgoing device under load turn-off



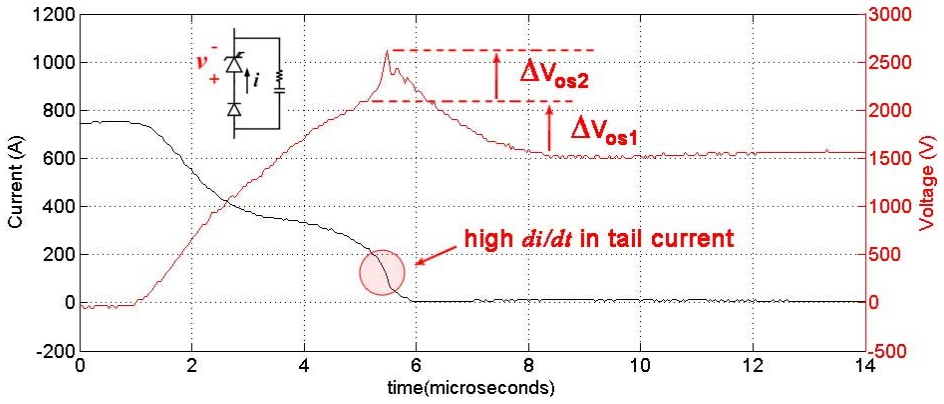
(b) current and voltage waveforms of incoming device under device turn-on

Figure 4.4 Typical voltage and current waveforms during load commutation (sampling rate= 25MS/sec)

As discussed in the design of turn-off snubber, IGCT has a defined end in their tail current during turn-off and this causes an extra voltage overshoot. This behavior can be observed from Fig.4.3a, where there is a decrease in IGCT current with a high/dt at the "tail" current (encircled on Fig.4.5b). This switching characteristic of IGCT is likely to occur in capacitive operating region, where IGCT is turned-off to block voltage higher than 1500V. This switching behavior is not observed in inductive operating region, where IGCT is always turned-off to block less than 1200V. This can be observed from the typical forced turn-off of IGCT in inductive operating region, given in Fig.4.5a. It is concluded that the turn-off and the turn-on snubbers are designed successfully.



(a)



(b)

Figure 4.5 Non-linear switching characteristics of IGCT (a) smooth forced turn-off of IGCT, (b) undesired forced turn-off of IGCT,where high di/dt exists in "tail" part of IGCT current (sampling rate= 25MS/sec)

In Fig.4.6 and 4.7, IGCT currents are given with respect to switching signals for load commutation and forced commutation, respectively. There is an overlap (marked as $t_{overlap}$ in Fig.4.6 and Fig.4.7) in switching signals such that IGCT of outgoing device is always gated off approximately 10μsec after gating on the incoming IGCT. In load commutation, incoming IGCT is turned on after it is gated on since it is forward biased. On the other hand, during forced commutation, incoming IGCT can not be turned on although it is gated on since its series diode is reverse-biased. It should wait until gating off of outgoing IGCT. It is observed from Fig.4.6 and 4.7 that turn-on delay ($t_{d(on)}$) is typically 3.5μsec in load commutation while the turn-off delay ($t_{d(off)}$) is typically 5μsec.

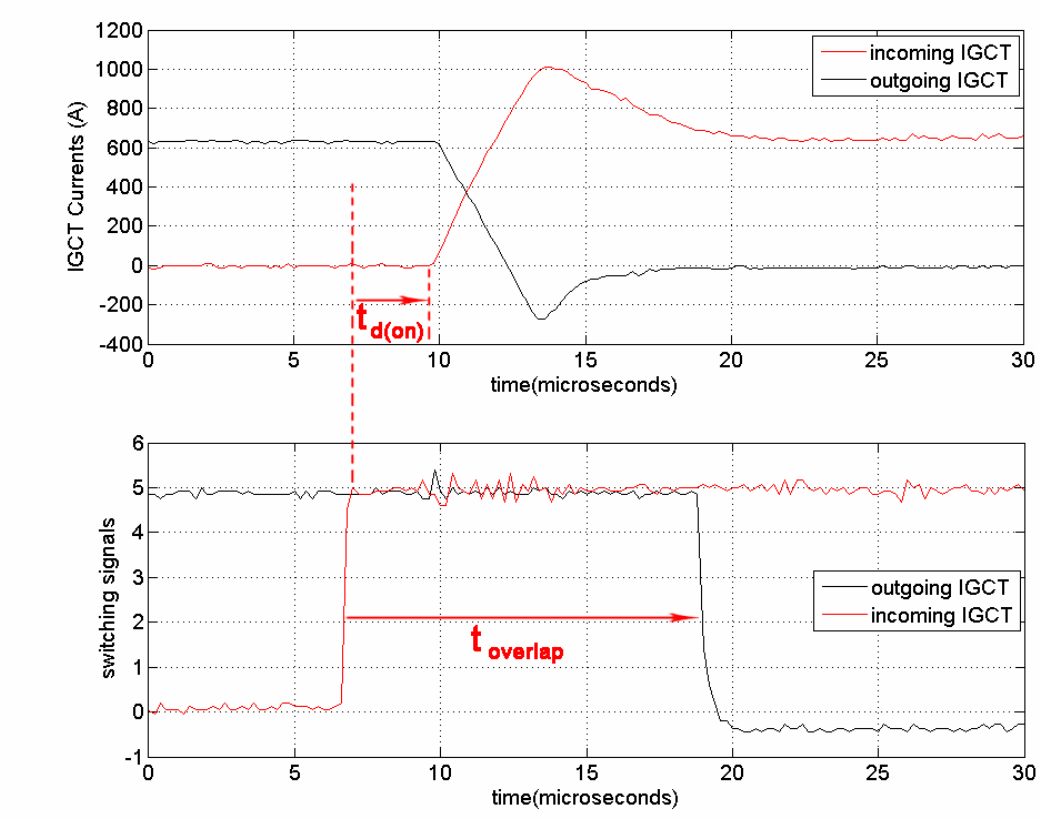


Figure 4.6 IGCT currents and their corresponding switching signals during load commutation (sampling rate= 2.5MS/sec)

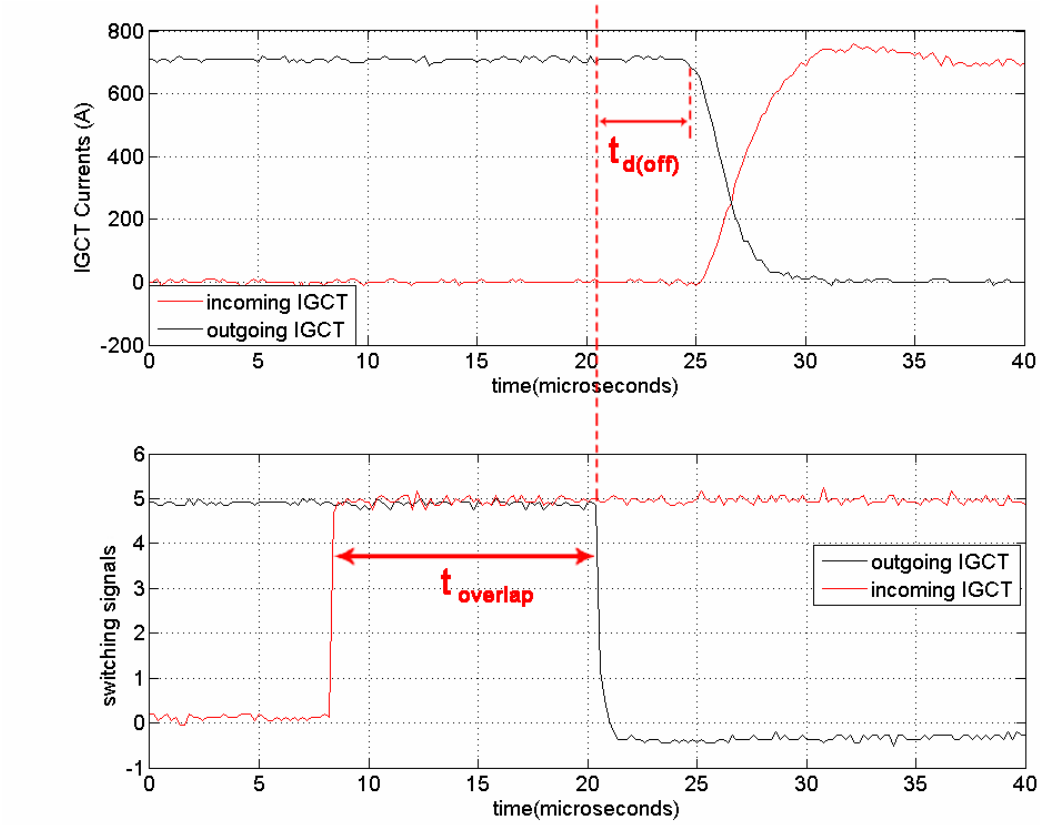


Figure 4.7 IGCT currents and their corresponding switching signals during forced commutation (sampling rate= 25MS/sec)

4.2.2 Harmonic Distortion

The performance of harmonic elimination technique is proven by field tests. The measured quantities are marked on the single-line diagram given in Fig.4.8. The variations in TDD of line current waveforms on medium voltage side (i_{MR}) against reactive power produced by CSC based STATCOM ($Q_{STATCOM}$) are given in Fig.4.9.

These experimental results are compared with simulation results in Table 4.2 for 500kVAr reactive power generation in inductive mode. Since the chopping angles are determined by optimization, the harmonic elimination technique used in this study does not yield an absolute elimination of all low order harmonics (e.g. 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics in the second column of Table 4.2 are not absolutely

zero). Moreover, non-ideal switching characteristics of IGCTs also affect the success of harmonic elimination. To quantify the effects of these non-idealities in the implemented system on CSC input line current, measured I_R values given in the fourth column of Table 4.2 can be compared with those in the second column obtained from simulation.

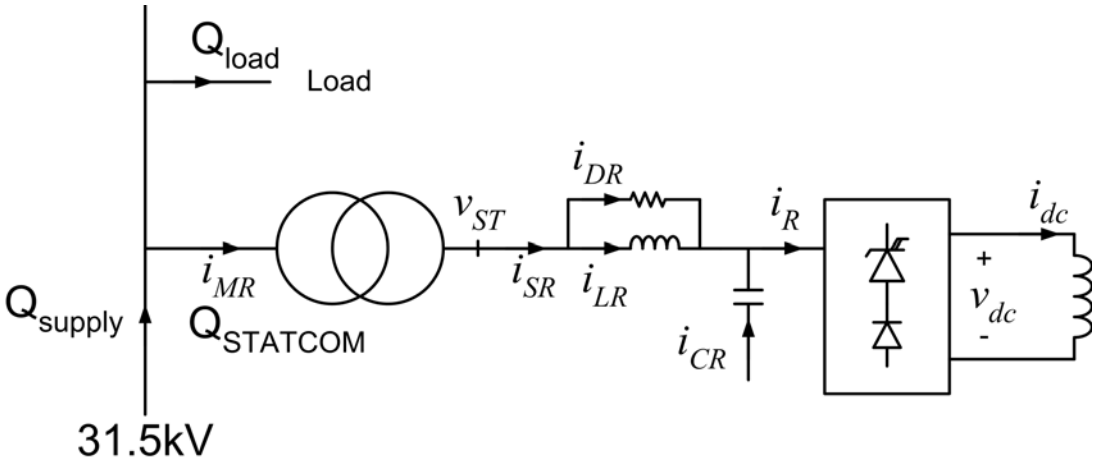


Figure 4.8 Illustration of measured variables on the single line diagram

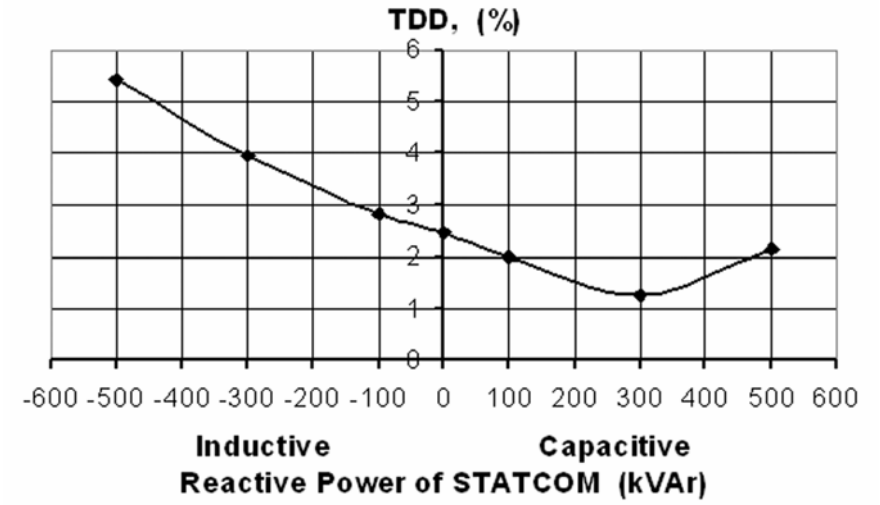
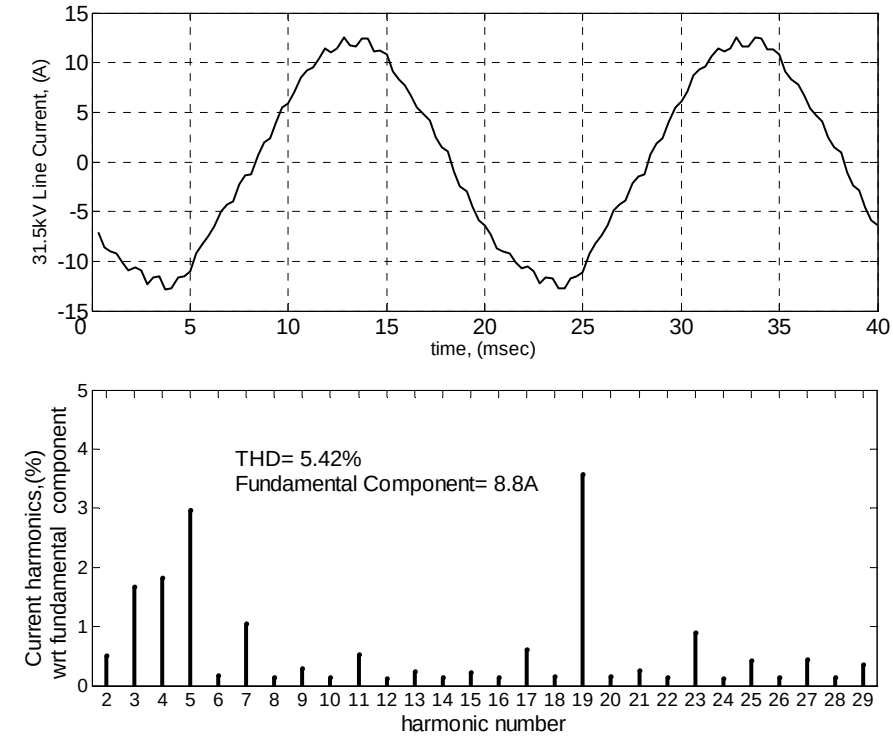


Figure 4.9 Variations in TDD of CSC based STATCOM line current on 31.5 kV side

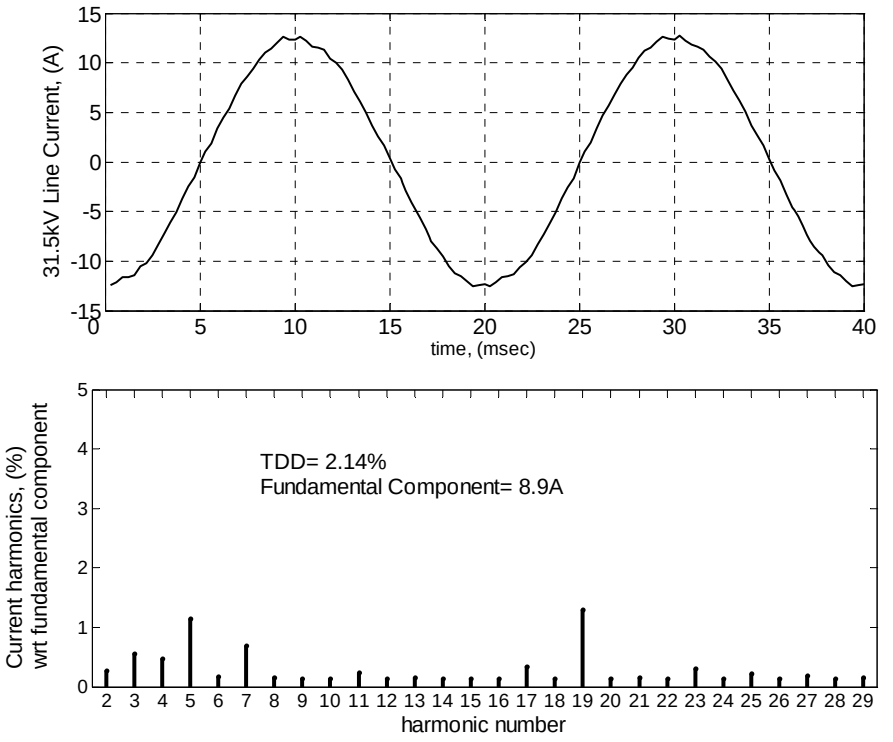
Table 4.2 Harmonic content of CSC input current, i_R and supply current, i_{SR}. on 1kV side (when CSC based STATCOM is generating 500kVAr inductive reactive power)

Harmonic Number, n	rms Current, Amps			
	Simulation		Field Test	
	I_R	I_{SR}	I_R	I_{SR}
1	407.8	297.9	400.7	283.7
3	0	0	1.4	3.9
5	0	0	4.6	9.9
7	2.1	1.0	4.3	2.1
11	7.1	1.1	9.9	1.4
13	3.5	0	5.0	0
17	19.9	0	26.2	1.4
19	227	9.9	221.3	9.9
23	92.2	1.63	82.3	2.5

Further than these, low-pass input filter causes magnification of 3rd, and 5th harmonic current components. 3rd, and 5th harmonics appearing in the line current waveform of CSC will then be amplified theoretically by the factors of 2.3 and 1.6, respectively. In practice however, owing to the component tolerances of low-pass input filter, these are magnified by 2.75 and 2.1, respectively, as can be determined from experimental values in last two columns of Table 4.2. In summary, TDD value of the implemented CSC based STATCOM can be 20% higher than theoretical value. Some sample line current waveforms of CSC based STATCOM on 31.5kV side and their harmonic spectra are shown in Fig.4.10. For the developed system, total harmonic distortion TDD, as well as the amplitudes of individual current harmonic components of line current waveforms at the common coupling point (31.5kV medium voltage distribution bus) are compared with limit values given in IEEE Std. 519-1992. This comparison is summarized in Table 4.3 for 500kVAr reactive power generation in inductive region. It is observed that all field test results comply with IEEE Std. 519-1992, over the entire operating range of CSC based STATCOM. In the last column of Table 4.3, the limit values for the worst case are also given. The worst case corresponds to weakest supplies, which are not usual at medium voltage buses. The CSC based STATCOM can comply even with the worst case limit values by seven harmonic elimination, and/or a more careful filter design.



(a)



(b)

Figure 4.10 31.5kV side line current waveforms of CSC based STATCOM and their harmonic spectra for (a) 500kVAr inductive, (b) 500kVAr capacitive (sampling rate= 25MS/sec)

Table 4.3 Harmonic distortion in line currents of CSC based STATCOM at the Common Coupling Point (31.5kV bus)

$^{\Psi}$ maximum demand STATCOM current (fundamental frequency component) at PCC is taken as 9.2A corresponding to 500kVAr reactive power generation of STATCOM at 31.5kV side of coupling transformer maximum short-circuit current at PCC is 2.4kA, therefore I_{SC}/I_1=260

Harmonic Number, n	Field Test Results	Limit recommended by IEEE Std. 519-1992$^{\Psi}$	
		$100<I_{sc}/I_L<1000$	$I_{sc}/I_L<20$
3	1.5%	12%	4%
5	3%	12%	4%
7	1%	12%	4%
11	0.5%	5.5%	2%
13	0%	5.5%	2%
17	0.5%	5%	1.5%
19	3.5%	5%	1.5%
23	1%	2%	0.6%
TDD	5.62%	15%	5%

4.2.3 AC Side Voltage and Current Waveforms

The current waveforms, $i_R(t)$, $i_{SR}(t)$, $i_{CR}(t)$ and $v_{ST}(t)$ which are already defined in Fig.4.8 are given in Fig.4.11 and 4.12 for two different cases. In both cases, converter line current waveforms, $i_R(t)$, contain pulses, which are filtered out by filter capacitors. These pulses can also be observed from the capacitor current waveforms. This also shows that filter capacitors provide the commutation path during commutation of dc-link current among the power semiconductor switches in CSC since the reverse recovery current flow through a path including capacitor as marked on Fig.4.11-4.12.

As can be understood from Fig.4.12, the suppy current, $i_{SR}(t)$ is nearly sinusoidal in capacitive operating region since CSC can only generate 250kVAr capacitive reactive power in addition to 250kVAr capacitive reactive power of input filter, hence the magnitude of harmonics injected by CSC is relatively low with respect to fundamental component of supply current. On the other hand, CSC generates 750kVAr inductive reactive power to overcome 250kVAr capacitive reactive power of input filter, resulting in injection of higher harmonics in magnitude by CSC.

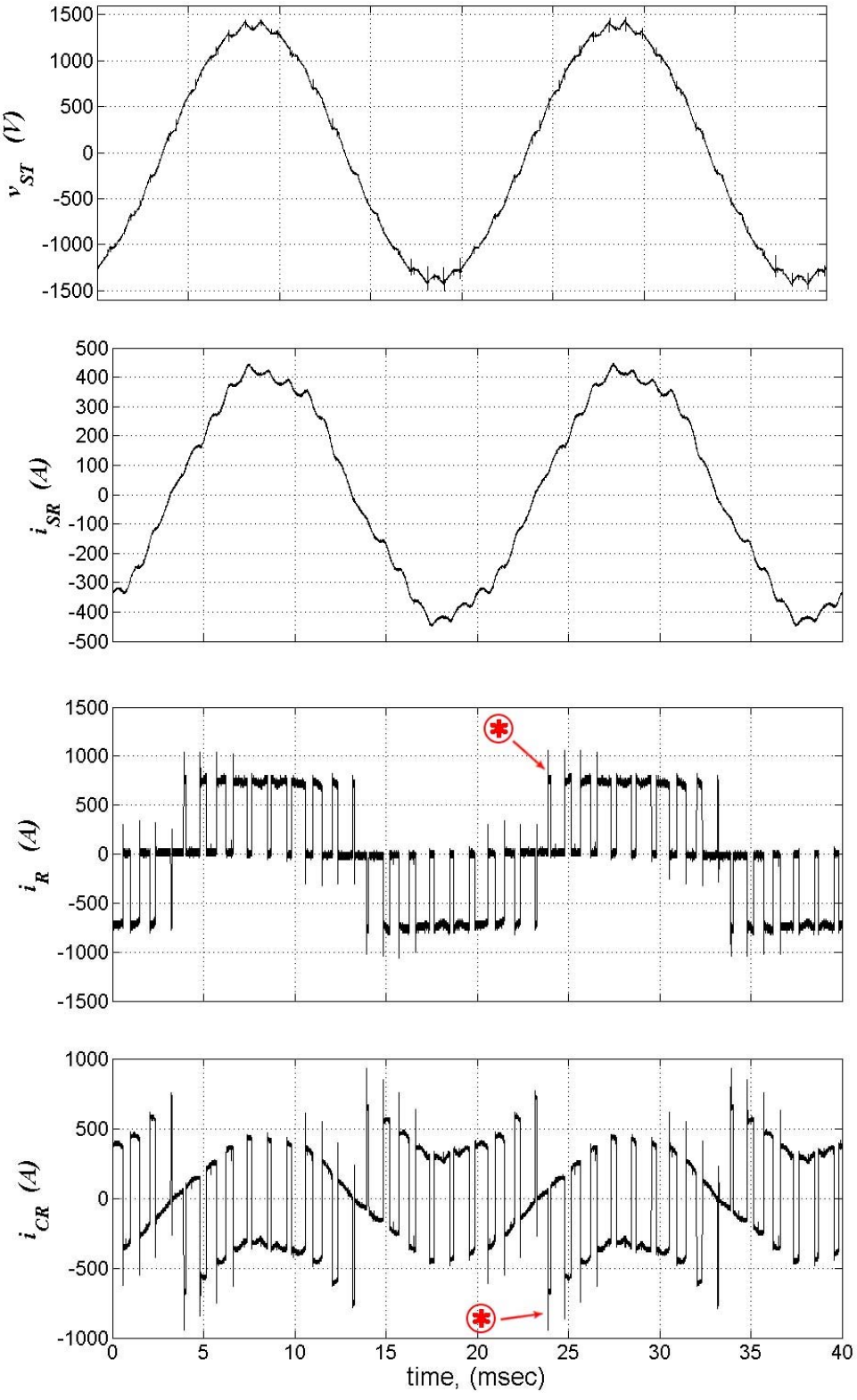


Figure 4.11 AC side waveforms of CSC based STATCOM at 1kV during 550kVAr inductive reactive power generation of STATCOM (* - reverse recovery current of diode under load turn-off through IGCT under device turn-on and capacitor) (sampling rate= 1MS/sec)

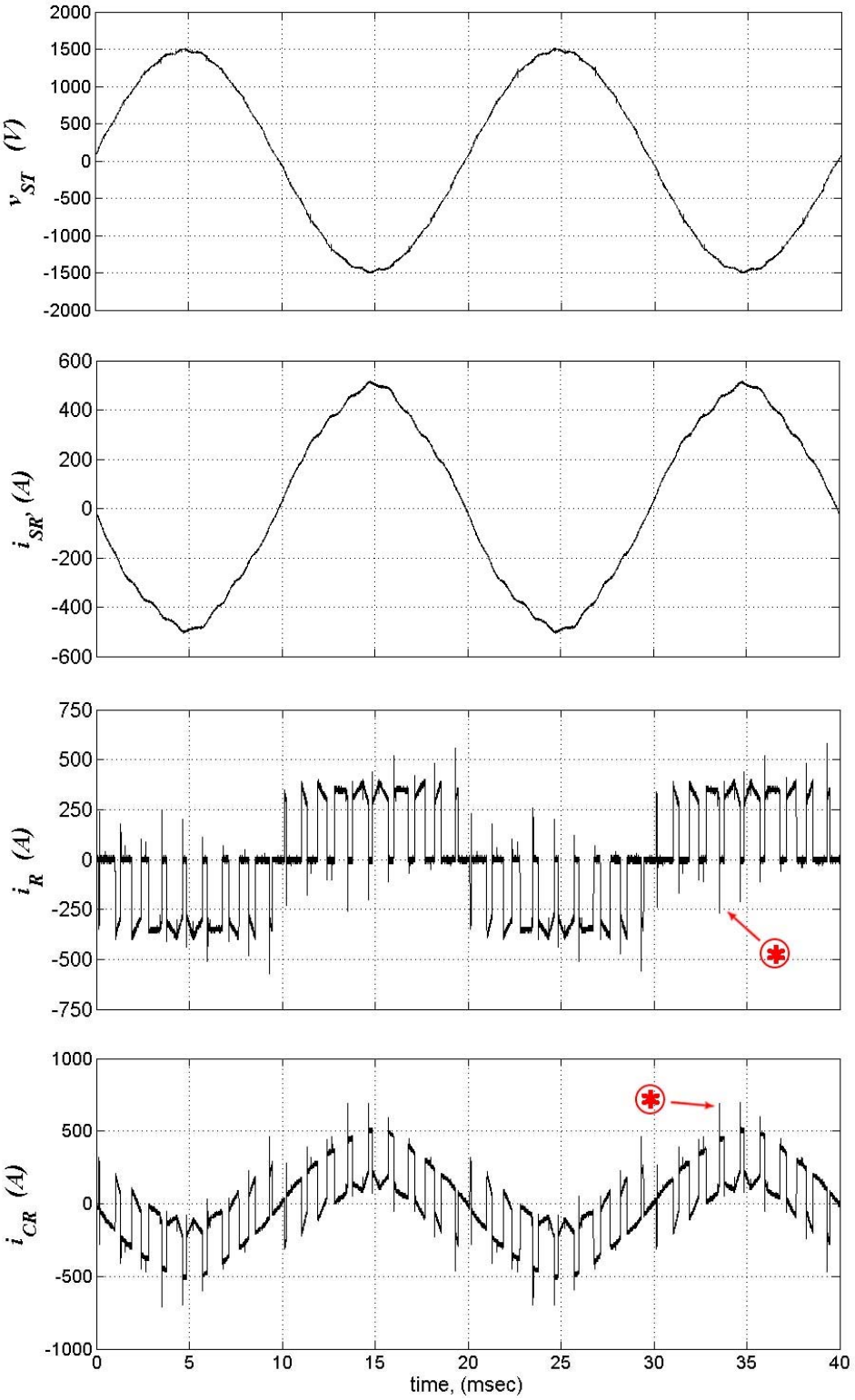


Figure 4.12 AC side waveforms of CSC based STATCOM at 1kV during 625kVAr capacitive reactive power generation of STATCOM(* - reverse recovery current of diode under load turn-off through IGCT under device turn-on and capacitor) (sampling rate= 1MS/sec)

Since the line-to-line voltage waveform, $v_{ST}(t)$ has been taken from the secondary side of the coupling transformer, harmonics in the supply current, $i_{SR}(t)$ cause small distortions in the voltage waveform due to significant leakage inductance of the transformer. However, these distortions can not be seen at the primary side of the coupling transformer due to relatively low line impedance of power system with respect to leakage inductance of the transfomer.

As discussed in design of input filter, the magnitude of line-to-line voltage at the input terminals of CSC from full capacitive to full inductive reactive power generation. This is also valid for the secondary side line-to-line voltage of coupling transformer, given in Fig.4.11 and 4.12. The current waveforms of filter reactor and filter damping resistor are presented in Fig.4.13 and 4.14 for capacitive and inductive operation of STATCOM, respectively. As the impedance of the filter reactor increases with frequency, higher order supply currents flow through filter resistors. On the other hand, fundamental component of supply current flow through the filter reactor, resulting low loss damping for the input filter.

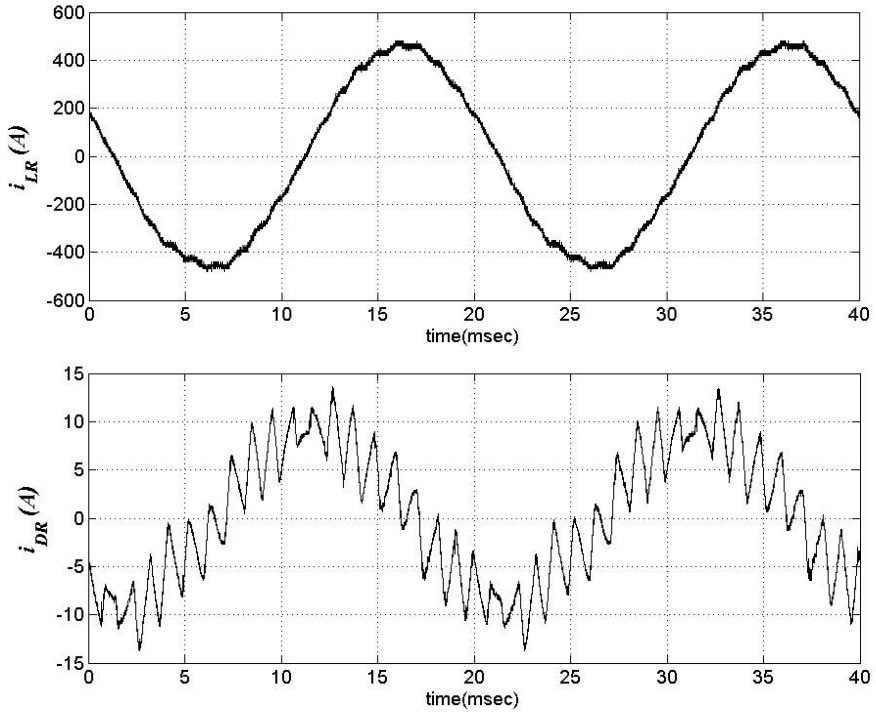


Figure 4.13 Filter Reactor and Filter Damping Resistor currents waveforms for 560kVAr capacitive case (sampling rate= 1MS/sec)

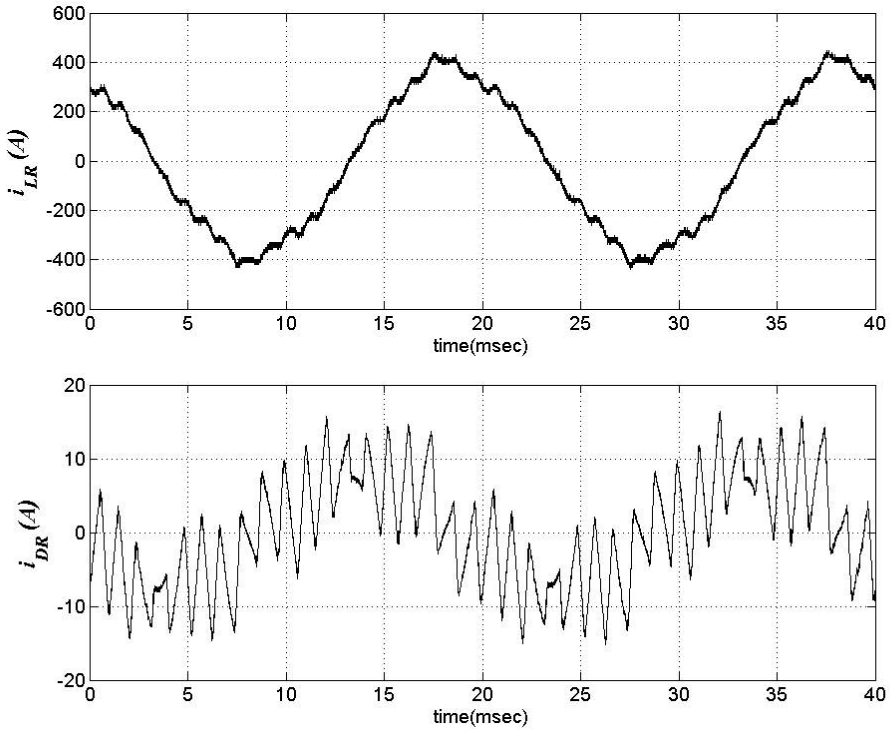
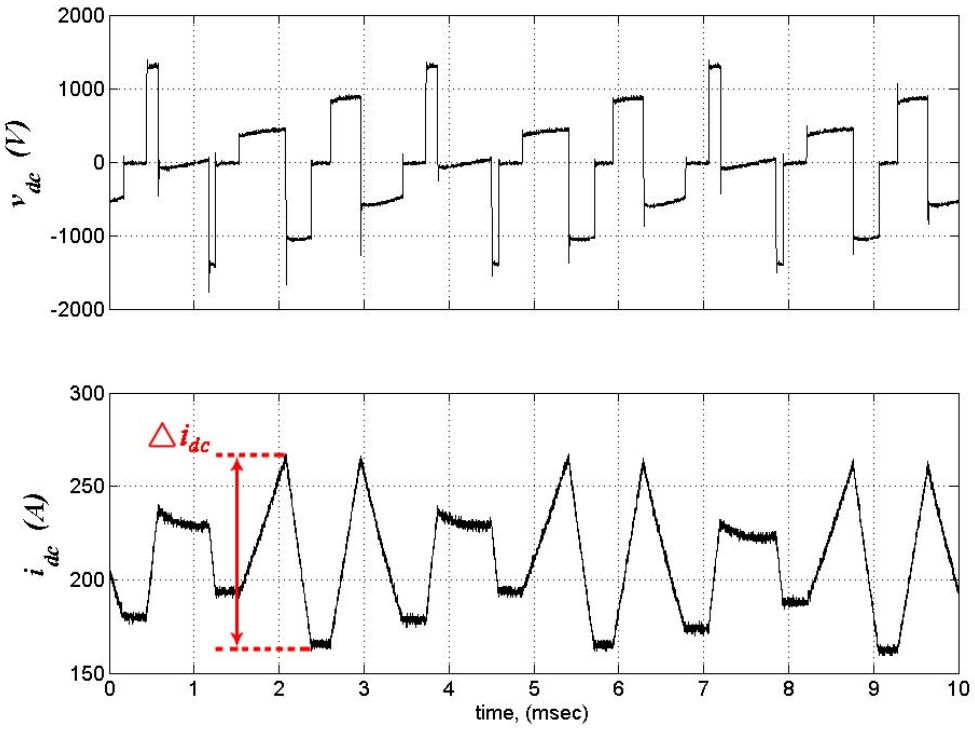


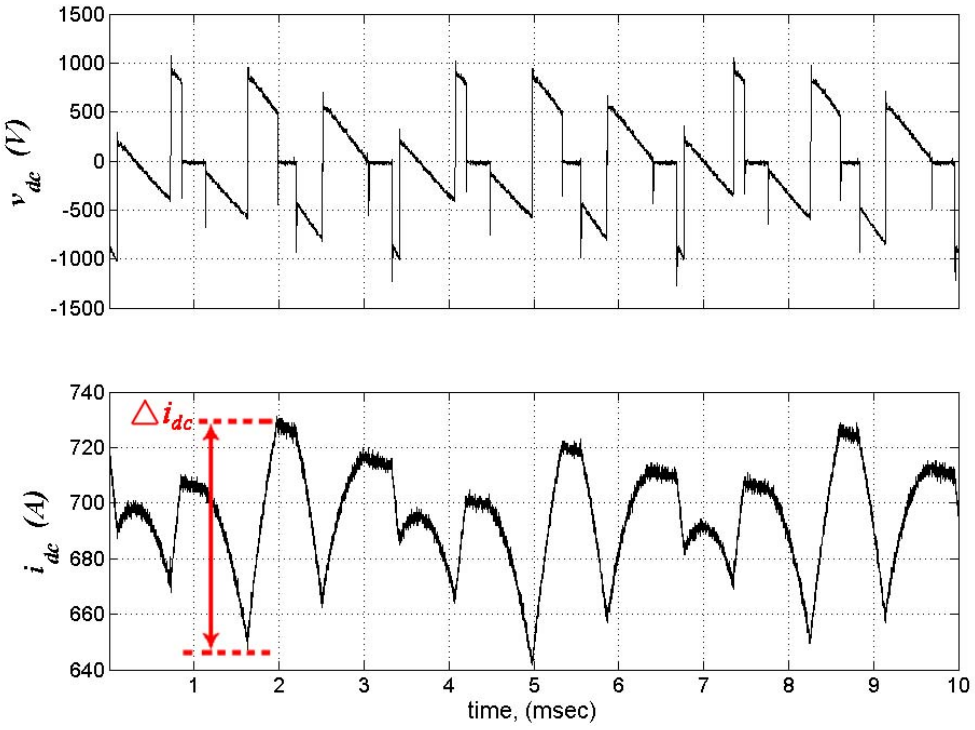
Figure 4.14 Filter Reactor and Filter Damping Resistor current waveforms for 500kVAr inductive case (sampling rate= 1MS/sec)

4.2.4 DC Side Voltage and Current Waveforms

Dc-link voltage and current waveforms are as given in Fig.4.15. Voltage waveform has been recorded by a high voltage differential probe,. Peak-to-peak ripple current has been measured by a Rogowski coil while mean value of the dc-link current has been deduced from hall-effect device measurements. The peak-to-peak ripple in dc-link current is 10% of its mean value at 500kVAr inductive reactive power generation of STATCOM. It is interesting to observe that the peak-to-peak ripple in dc-link current stays constant in magnitude although its mean value changes. There is 180° phase difference between the ripples in different operating regions, as observed from Fig.4.15. The over voltages in dc-link voltage in both operating region are lower than the over voltages across IGCTs during forced turn-off because high over voltages remain in the commutation path.



(a)



(b)

Figure 4.15 DC link waveforms of CSC for (a) 500kVAr capacitive and (b) 500kVAr inductive reactive power generation of STATCOM (sampling rate= 1MS/sec)

From Fig.4.15a, some of the pulses in dc-link voltage has the peak value of the line to line voltage resulting in increase in dc-link current. But, due to the inherent short circuit capability of CSC, this rate of rise is so slow that it can be easily detected by a hall-effect current transducer in case of loss of control and short circuit current in dc-link.

4.2.5 Characterization of Power Losses

During the field tests, forward voltage drop of IGCT was recorded by passive signal probe. Together with the forward voltage drop, voltage and current waveforms were also recorded by high voltage differential probe (DP100) and Rogowski coils so that switching and conduction losses of the power semiconductors can be calculated. The forward voltage drop of DIODE is taken from its datasheet as a typical voltage drop value for the operating junction temperature of 125°C. The reverse-recovery losses are calculated from the voltage and current waveforms. However, the forward-recovery losses of DIODE are neglected since the rate of rise in current during turn-on is slower as compared with the data in its datasheet, hence forward voltage drop during forward recovery can not be measured accurately due to the stray inductance in the measuring circuit. The results are presented in Table 4.4 for sample operating points. As compared with Table 3.4, field results show that turn-off loss of IGCT is higher than theoretically interpolated value while the reverse recovery loss of DIDOE is found to be less than the expected value. This is because there is an inevitable over voltage across the IGCT during turn off. This results higher turn-off losses. The over voltage across DIODE during reverse recovery is relatively small and the maximum reverse-recovery current is lower than expected value due to lower -di/dt. These can also be concluded from Fig.4.3 and 4.4. The turn-on loss of IGCT is also found to be less than the expected value due to the positive effect of turn-on snubber.

Table 4.4 Measured power loss components of IGCT and Diode at different operating conditions

	Conduction		Turn-on		Turn-off		Total	
	IGCT	DIODE	IGCT	DIODE	IGCT	DIODE	IGCT	DIODE
500kVAr Inductive	340W	775W	13W	-	295W	115W	648W	890W
200kVAr Inductive	165W	330W	13W	-	90W	131W	268W	461W
650kVAr Capacitive	175W	330W	13W	-	182W	50W	370W	380W

Since the use of snubber reduces the electrical stress on power semiconductors at the expense of their power loss, this should also be considered in the snubber design. The power loss in the snubber resistor has been measured to be 200W per snubber in the worst case. This is larger than the theoretical value obtained from the simulation work as given in Fig.3.45 due to the transient over voltages during commutation and these are not considered in the simulation work.

The internal dc resistor of the dc-link reactor has been measured to be 14.75mΩ. The power dissipation in dc-link reactor is based on copper loss since it is an air-core reactor. Similar to dc-link reactor, internal dc resistor of each filter reactor in input filter has been measured as 9.75mΩ. Then, power dissipation in dc-link reactor and each filter reactor can be calculated as 7.5kW and 880W for the maximum operating conditions. Beside the reactors and the damping resistors in the input filter result in extra power dissipation, which has been measured to be 500W per each resistor for the worst case.

Total losses of CSC based STATCOM including coupling transformer, cables, bus bars, semiconductors, dc-link reactor, and all others will vary as a function of reactive power generated by the overall system as given in Fig.4.16.

Total power loss of implemented CSC based STATCOM can be separated as 20% in coupling transformer, 30% in converter losses including snubber and IGCT power supply, 20% in dc-link reactor, 15% in low-pass input filter and 15% in other system elements at full load. The efficacy of the CSC based STATCOM (power dissipation/reactive power generated) is found to vary in the range from 2% to 7% over the entire operating range

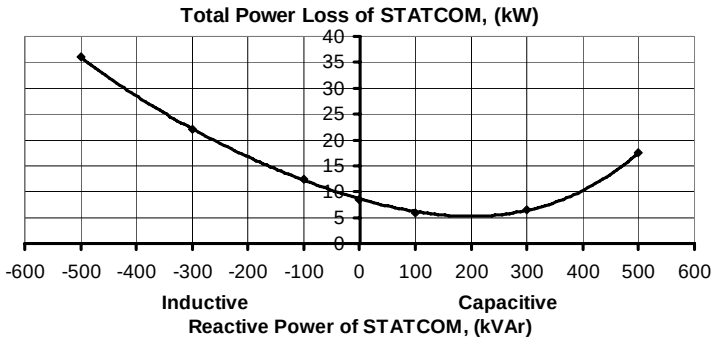
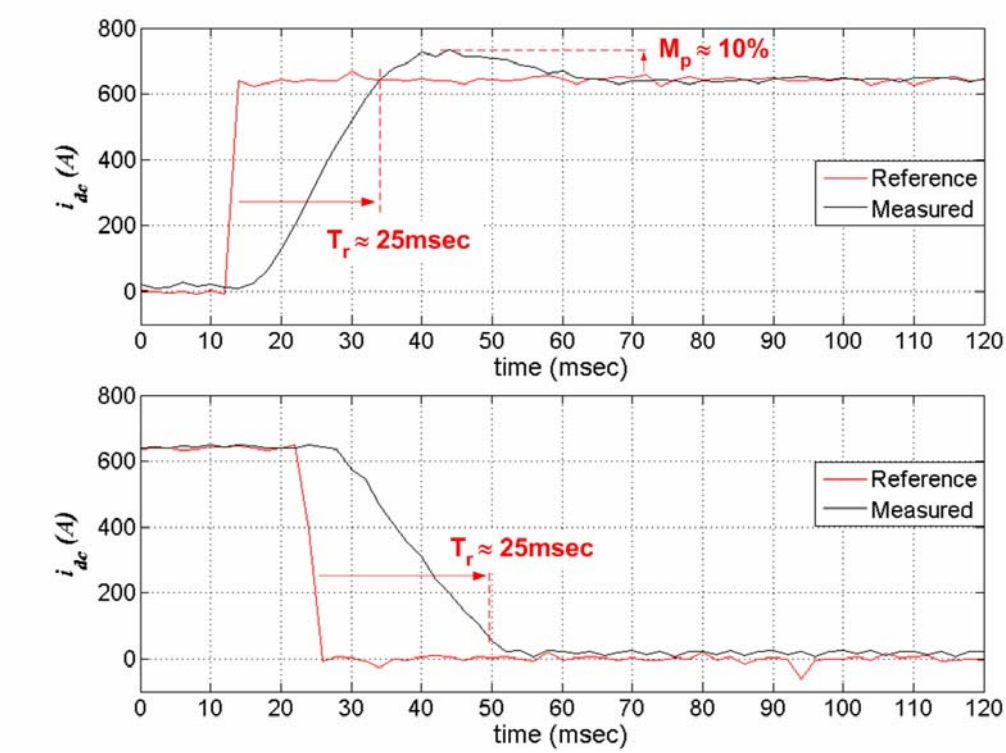


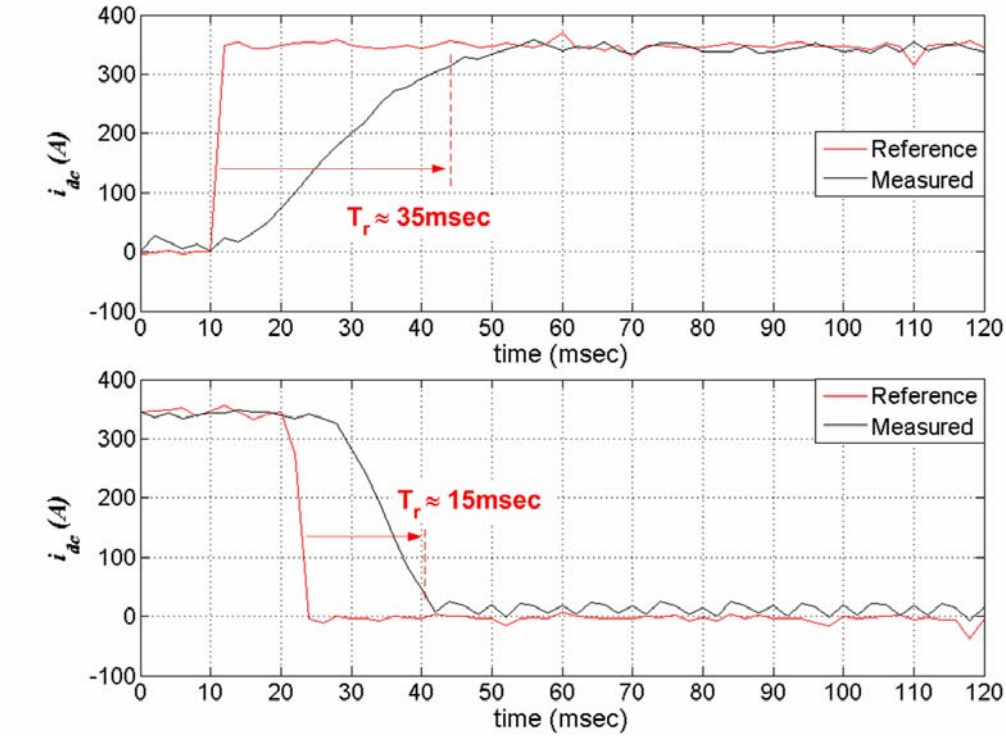
Figure 4.16 Total STATCOM losses against reactive power

4.2.6 Reactive Power Compensation Performance

Transient response of the implemented CSC based STATCOM was also recorded in the field. There are two control loops, one within the other as described in Chapter 3. In order to test current control loop, reactive power controller was decoupled through the software and the reference input for the current control loop was applied to Analog-to-Digital Converter (ADC) of DSP, as proposed in Chapter 2. Applying a step input to the ADC, the proportional and integral time constants of the current controller were tuned by using Ziegler Nichols rule. The transient response of the current control loop was verified by recording the step input and dc-link current simultaneously for the best case as given in Fig.4.17. Response time (T_r) is approximately 25msec and the maximum percentage of overshoot (M_p) in current is less than or equal to 10% for both capacitive and inductive operating mode of CSC. After tuning the parameters of current controller, reactive power controller was coupled to the software again and a step reference signal was applied to ADC of DSP. Again, the Ziegler-Nichols rule was applied in order to adjust the proportional and integral time constants of reactive power controller. Transient response of the reactive power control loop together with the current control loop was also recorded and given in Fig.4.18 for the best case. The reference step input was applied as from full capacitive to full inductive reactive power generation of STATCOM, and vice versa. The results meet the design specifications of the prototype system given in Chapter 3 since the response is always less than 100msec and M_p in the produced reactive power is less than 10%.

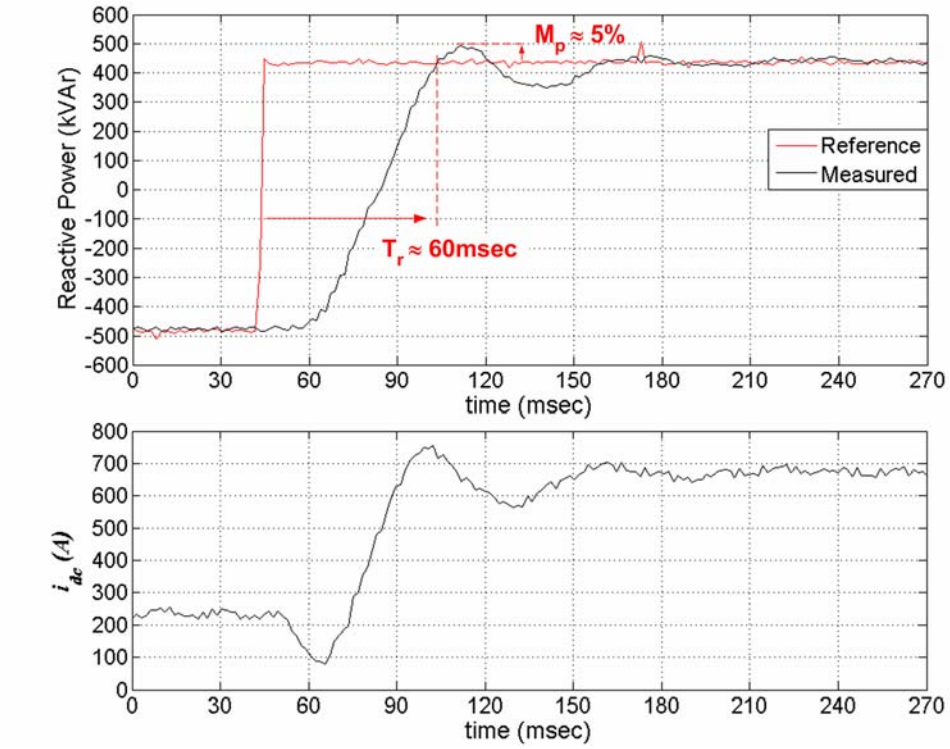


(a) during inductive reactive power generation of CSC

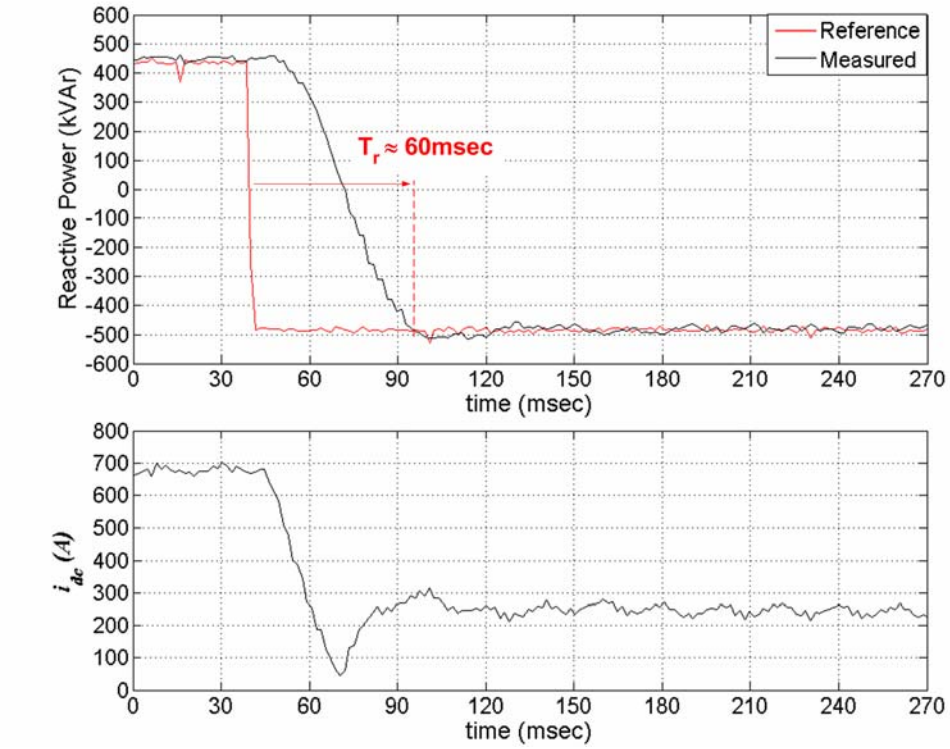


(b)) during capacitive reactive power generation of CSC

Figure 4.17 Transient response of current control loop to a step input (sampling rate= 2.5kS/sec and averaged at every 5 sample)



(a) from full capacitive to full inductive



(b) from full inductive to full capacitive reactive power reference

Figure 4.18 Transient response of overall control system to a step change in reference reactive power (sampling rate= 2.5kS/sec and averaged at every 4 sample)

Beside the transient response to a step change in reference reactive power, reactive power compensation performance of the developed STATCOM systems was also recorded on site by using data acquisition system. The variations in reactive power consumption of electric excavators (Dragline and Power Shovel), and reactive power generated by CSC based STATCOM are as given in Fig.4.19 for nearly two minutes operating period which corresponds nearly to two operating cycles of Dragline. The developed STATCOM (black colored curve in Fig.4.19) follows closely the rapid variations in reactive power demand of the load bus (red colored curve).

The records of reactive -and active powers for 24 hours are given in Fig.4.20 both for the excavators, and the STATCOM. Although the developed STATCOM having ±500kVAr reactive power generation capability does not provide full compensation (Fig. 4.20), this capacity can meet the reactive power compensation needs of the electric excavators to meet strict reactive penalty limits even in the future (Table 1.1), resulting in nearly unity pf. (1% inductive and 3% capacitive reactive energy of active energy demand of the load).

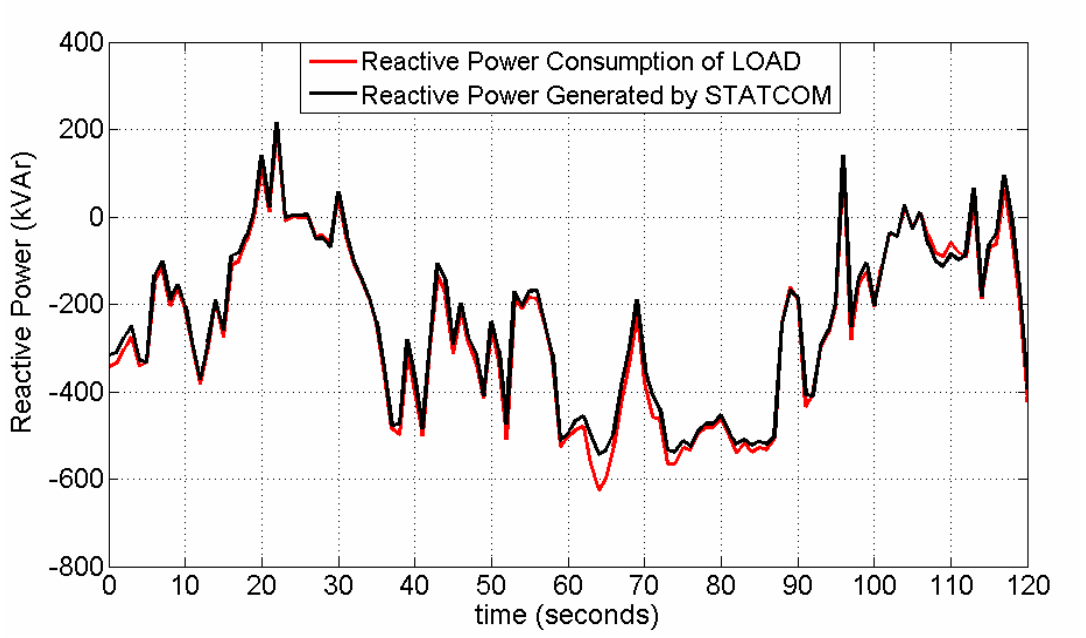
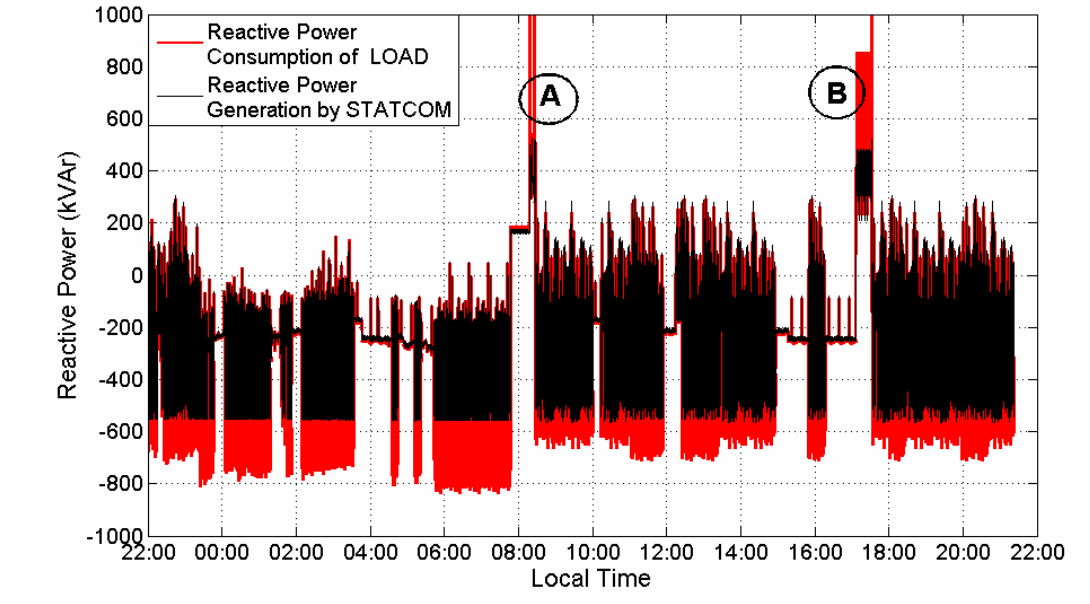
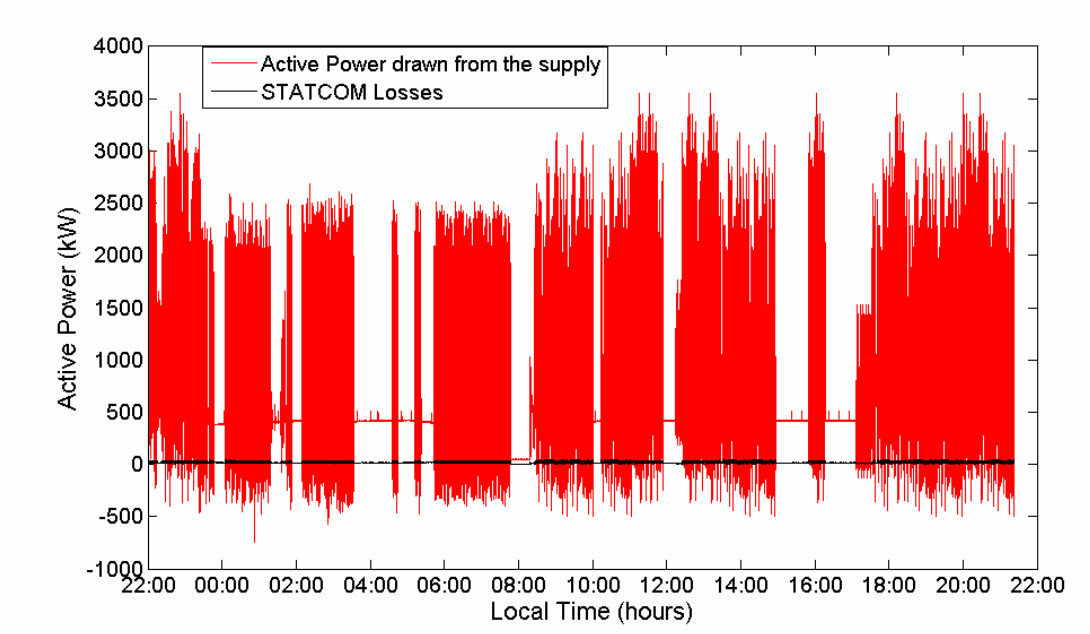


Figure 4.19 Reactive power consumed by load and generated by STATCOM (1sec averaged data)



(a)



(b)

Figure 4.20 Daily power variations (a) reactive, (b) active power variations (1 sec averaged data)

In Figs.4.19 and 4.20, one second averaged data are plotted. Positive kVAr consumption denotes lagging pf load, and positive reactive power generation for STATCOM denotes capacitive operation. Curve portion A in Fig.4.20b corresponds to consecutive startings of dragline and the power shovel. Dragline demands nearly 4.5 MVAr during a starting period of 30 seconds, while the power shovel 2 MVAr for a period of 20 seconds. On the curve portion B in Fig.4.20b, power shovel is excavating coal while the dragline is in the standby mode. In Fig.4.20b, negative active power drawn from the supply corresponds to regeneration of electric excavators. During regenerative braking period, electric excavator supplies the STATCOM losses. Since buy and sell tariff does not apply to this bus, only part of the STATCOM losses will be reflected to electricity bills.

CHAPTER 5

CONCLUSIONS

The design and implementation of a three phase single stage CSC based STATCOM prototype has been carried out in this research work. The prototype has been designed and developed according to the sample application such as load compensation of coal mining excavators.

The developed system is composed of a single full-bridge current-source converter with selective harmonic elimination and the simplest coupling transformer topology to serve as a full substitute for conventional voltage source converter based STATCOMs with complicated transformer connections and/or multiphase converters for harmonic elimination. The 5^{th}, 7^{th}, 11^{th} and 13^{th} current harmonics produced by CSC are shown to be eliminated by switching semiconductors at a moderate frequency of 500Hz. The series combination of an asymmetrical IGCT, and a reverse blocking diode meets the objective of natural air cooling for high reliability and unmanned operation. The line currents of CSC based STATCOM at the medium voltage common coupling bus comply with IEEE Std. 519-1992. Especially TDD of STATCOM line current can be reduced to an absolute minimum by applying six harmonic component elimination strategy at the expense of higher switching frequency, and designing the low-pass input filter more carefully. The resulting system follows the rapid changes in reactive power demand of electric excavators, thus improving the power factor of the overall system to nearly unity. The power loss versus reactive power output of the resultant CSC based STATCOM is nearly the same as that of practical SVC having same rating even though dissipative damped input filter with parallel connected resistors has been preferred in the implementation.

The developed prototype system has been applied to two different sites of Turkish Coal Enterprises for load compensation of coal mining excavators. These

applications have been presented as the first industrial application of CSC based STATCOM [64].

Following conclusions can be drawn from the results of theoretical and experimental work carried out within the scope of this research work:

- The technical feasibility and viability of an IGCT based CSC in D-STATCOM application have been proven.
- The current harmonic standards can be met even for the weakest power supplies by using CSC topology and the simplest transformer connection.
- Without using series or parallel operation of power semiconductors, CSC can be implementable in the form of a single unit with de-ionized water cooling for the operating range from 2.6 MVAr capative to 960 kVAr inductive reactive power.
- The CSC STATCOM topology is very flexible so that asymmetrical operating characteristics can be easily realized by using larger input filter capacitor banks and/or by connecting plain capacitor or tuned LC filters to the medium voltage side of coupling transformer. Increasing the VAr production capability of STATCOM improves significantly the harmonic content of STATCOM line currents. Thus allowing lower switching frequencies.
- SHEM in complying with harmonic standards and phase shift angle control in controlling the reactive power produced by STATCOM permit the use of relatively low switching frequencies in CSC based STATCOM in comparison with VSC based STATCOM because input low pass filter of CSC serves as second order filter for the current harmonics injected by CSC whereas the coupling reactor of VSC present a first order low pass filter for the voltage harmonics injected by VSC.
- In CSC based STATCOM, IGCT is more suitable candidate power semiconductor than HV-IGBT in accordance with SHEM and phase shift angle control.

- The developed system gives a satisfactory performance in both steady-state and transient state. A complete transition from maximum inductive VAr production to maximum capacitive VAr production or vice versa takes place in a time period less than 100msec. The use of smaller dc-link inductance and smaller input filter components will reduce response time significantly at the expense of higher switching frequency needed.
- The use of turn-on snubber circuit is a must in order to limit di/dt of IGCT and –di/dt of reverse blocking diode. However, this is not the case for turn-off snubber. The use of turn-off snubber is found to be useful not only in reducing the turn-off losses of IGCT and reverse blocking diode but also in limiting dynamic overvoltages across the terminals of power semiconductors, i.e., in forward direction for IGCT and reverse direction for reverse voltage blocking diode.
- The use of presspack IGCT as the main switching element of CSC based STATCOM simplifies the design and implementation of power stage layout and makes the layout more flexible as compared with other power semiconductors.
- The presence of external di/dt limiting reactors allows the possibility of making fine adjustments for the stray inductance between the semiconductors and input filter capacitors.

An important consequence of this study is that the application of CSC based STATCOM is not impractical and viable as believed previously. By applying critical compromises in the design of CSC based STATCOM, such as in power semiconductor selection, dc-link reactor design, input filter design, controller design better performance figures in terms of lower TDD values, efficacy values, and faster response time can be obtained as compared to conventional SVC systems. Considering inherent advantages of CSC over VSC, including

i) direct control of injected reactive current
ii) better distortion figures for the injected reactive current at relatively low switching frequencies

iii) implicit short circuit protection

iv) fast start-up (that is no need for additional pre-charging circuit)

the proposed CSC based STATCOM may constitute a viable alternative to conventional SVC and VSC-STATCOMs, offering a new technological solution for FACTS Controllers.

Based on these operating principles described in this work, not only qualitative but also quantative design criteria for developing a CSC based STATCOM have been given. These are summarized in Table 5.1.

Table 5.1 Effect of main system parameters on cost and performance

System Parameter	Advantages	Disadvantages
The use of larger filter capacitor	• low cost compensation of fixed part of the load VAR demand	• Higher cost • worse closed loop response • makes VAR characteristic asymmetric
The use of larger filter reactor	• for damping in parallel connected damping resistor based input filter • for adjusting corner frequency of input filter	• makes VAR characteristic asymmetric • presents poor voltage regulation • worse closed loop response
DC link reactor with minimum storage capacity	• faster closed loop response • lower cost • lower loss	• higher harmonic content in ac side current waveforms • the rate of rise in dc-link current increases during fault conditions
Higher switching frequency	• lower harmonic content in ac side current waveforms • smaller input filter components • smaller dc-link reactor	• Higher switching losses • More costly cooling system

Table 5.1 (cont'd) Effect of main system parameters on cost and performance

System Parameter	Advantages	Disadvantages
The use of separate diode and Asymmetric IGCT connected in series instead of Symmetrical GCT	• higher power dissipation capability • higher VAR generation capability	• higher number of component count, hence increase in circuit complexity • problem in finding the match diode • higher stray inductance between GCT and diode
The use of antiparallel diode across Asymmetric IGCT	–	• costly • may cause problem in GCT operation
The use of turn-off snubbers	• limits dynamic overvoltages • decreases switching losses	• Increases circuit complexity • Decreases system efficiency
The use of IGCT instead of HV-IGBT	• lower conduction losses • more robust • optimized gate driver • lower turn-on losses • presents double side cooling opportunity as compared with module wire-bound HV-IGBTs • simplifies power stage design because its lower force turn-off di/dt	• Requires relatively high power supply • higher cost • integrated gate driver is uneconomical • lower di/dt • turn-on and turn-off is beyond the control of designer • higher turn-off losses
The use of SHEM with phase shift angle control instead of on-line PWM techniques with simultaneous control of modulation index and phase shift angle	• allows optimized fixed PWM • allows lower switching frequencies • easier in implementation	• slower transient response • coupled active and reactive power control • lacks active damping for the input filter

With the use of modern control methods such as full state feedback controller, dynamic response of CSC based STATCOM can be greatly improved. Since it allows the damping for possible resonance between ac capacitors and ac system reactance, damping resistors can be eliminated. Moreover, input filter reactors can also be eliminated by utilizing the transformer leakage reactance. This would further

decrease voltage regulation across ac terminals of CSC, allowing maximum utilization of voltage ratings of power semiconductors and ac filter capacitors. Although this requires implementation of PWM techniques, such as Space Vector PWM at switching frequencies around 1kHz, advents in power semiconductor technology in near future will make it possible.

Beside the advances in power semiconductor technology, widely use of superconducting magnetic energy storage will probably make CSC a better choice than VSC in FACTS applications.

An application of SVPWM at low switching frequencies with modern control methods based on full state feedback controller, including active damping method, to the developed CSC STATCOM within the scope of this work will be one of the further work topic.

Although SHEM is generally known as off-line PWM technique with fixed modulation index, the modulation index can be varied in steps. Due to advantages of SHEM over on-line PWM techniques, feasibility of simultaneous control of phase shift angle and modulation index with the use of SHEM in CSC STATCOM application will be an interesting future work topic.

The trend in FACTS Controllers is the use of multi-level VSC topologies in order to increase power rating and voltage rating of the converter. The multi-level CSC is a new concept and there are limited studies on this. As this application shows that main converter loss is due to conduction losses, they can be reduced by using parallel connected multi CSC. Therefore, a future work might be the design and implementation of a multi-level CSC based STATCOM.

Since the developed CSC based STATCOM is designed for reactive power compensation of balanced loads, another further work may cover the modification of the developed system for reactive power compensation of unbalanced loads.

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APPENDIX A

IMPLEMENTED TRANSMISSION STATCOM SYSTEMS

Table A.1 List of implemented Transmission STATCOM Systems

Application	Place	Year	Ratings	Details
Inuyama STATCOM Project	Japan	1991	±80 MVA, 154kV	48-pulse VSC
TVA Sullivan STATCOM	Tennessee, USA	1995	±100 MVA,161kV	48-pulse VSC
A Transmission SVC for National Grid Company	London, England	1997	0-225 MVAr, 400kV	Multilevel VSC
AEP UPFC	USA	1997	2 x 160 MVAr / 138kV	Three level VSC
20MVA Static Synchronous Compensator	China	1999	±20 MVAr / 220kV	Four levelVSC
The Hagfors SVC Light	Hagfors, Sweden	1999	0 - 44 MVAr / 10.5kV	PWM based VSC
Shin-Shinano 3 Terminal Voltage Sourced Converter Back-to-Back System [VSC-BTB]	Shin-Shinano Substation, Nagano, Japan	1999	53 MVA / 275kV (terminal A), 66kV (terminal B&C)	4 Two level VSC are in parallel
The Moselstahlwerk SVC Light	Moselstahlwerk, Trier, Germany	2000	0 - 38 MVAr / 20kV	PWM based VSC
Eagle Pass / Piedras Negras BTB Light	Coahula, Mexico	2000	0 - 36 MVAr / 138kV	PWM based *Neutral Point Clamped* (NPC) VSC

Table A.1 (Cont'd) List of implemented Transmission STATCOM Systems

Application	Place	Year	Ratings	Details
Tornio Avesta Polarit	Finland	2001	0 - 164 MVAr	-
STATCOM Based Relocatable SVC Project	England	2001	±75 MVAr / 275 & 400kV	-
SDG&E Talega STATCOM/BTB FACTS Project	Talega Substation, San Clemente, California, USA	2003	±100 MVAr / 138kV-ac	8 Three level VSC are in parallel
STATCOM for Northeast Utilities	Stamford, Connecticut, England	2003	± 150MVAr / 115kV	VSC
Holly	USA	2003	± 100MVAr	-

APPENDIX B

MODELING OF CURRENT SOURCE CONVERTER BASED STATCOM IN DQ STATIONARY FRAME

CSC based STATCOM will be modeled in dq-stationary frame for balanced AC supply. For modeling, the equivalent circuit shown in Fig.B.1 will be used. In this circuit, three phase delta connected filter capacitor bank is connected in wye and equivalent capacitance of each capactior is taken as 3C. Following assumptions will be considered in the modeling:

- all the power semiconductor switches are lossless
- three phase balanced AC supply having harmonic-free line voltages, as defined in (B.1).

$$\left.\begin{aligned} v_R &= V\cos(\omega t) \\ v_S &= V\cos(\omega t - 2\pi/3) \\ v_T &= V\cos(\omega t - 4\pi/3) \end{aligned}\right\} \qquad \text{(B.1)}$$

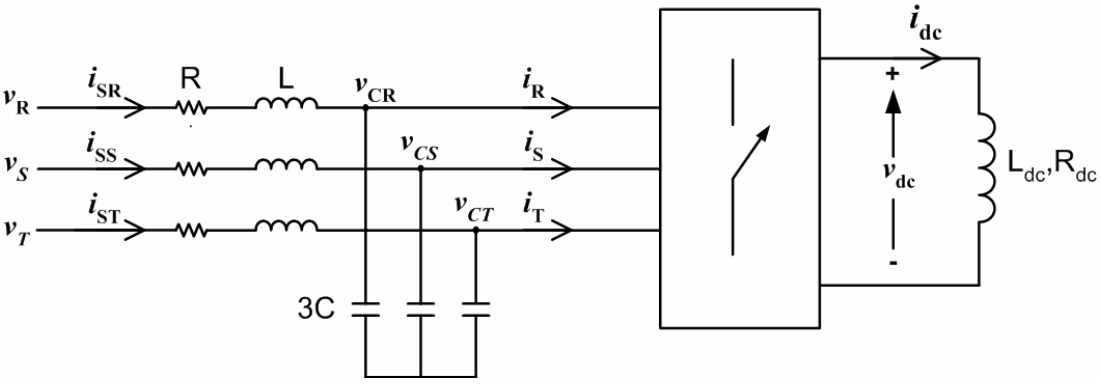


Figure B.1 Circuit diagram of CSC based STATCOM to be used for modeling

AC side differential equations are given in (B.2) for phase R. Same equations can be easily written for the other phases, S and T.

$$\left.\begin{aligned} v_R &= Ri_{SR} + L\frac{di_{SR}}{dt} + v_{CR} \\ i_{SR} &= 3C\frac{dv_{CR}}{dt} + i_R \end{aligned}\right\} \tag{B.2}$$

DC side differential equation of CSC based STATCOM is as follows

$$v_{dc} = L_{dc}\frac{di_{dc}}{dt} + R_{dc}i_{dc} \tag{B.3}$$

AC side and DC side quantities are coupled with switching functions as in (B.4).

$$\left.\begin{aligned} v_{dc} &= (m_1 - m_2)v_{CR} + (m_3 - m_4)v_{CS} + (m_5 - m_6)v_{CT} \\ i_R &= (m_1 - m_2)\, i_{dc} \\ i_S &= (m_3 - m_4)\, i_{dc} \\ i_T &= (m_5 - m_6)\, i_{dc} \end{aligned}\right\} \tag{B.4}$$

Using (2.2), (2.3) and (2.4), these switching functions can be expressed in terms of their Fourier components as in (B.5).

$$\left.\begin{aligned} m_1 - m_2 &= M\sin(\omega t + \theta) + b_h \sin(\omega_h t - \lambda) \\ m_3 - m_4 &= M\sin(\omega t + \theta - 2\pi/3) + b_h \sin(\omega_h t - \xi) \\ m_5 - m_6 &= M\sin(\omega t + \theta - 4\pi/3) + b_h \sin(\omega_h t - \psi) \end{aligned}\right\} \tag{B.5}$$

Switching functions do not linearly dependent on the control variables modulation index, *M* and phase angle, θ since they contain harmonic components, which do not depend on modulation index and phase angle explicitly.

In order to linearize the switching functions harmonic components should be neglected. This does not cause any problem in analyzing the system performance since harmonics do not contribute to active and reactive power flow. Then, switching functions can be approximated as in (B.6).

$$\left.\begin{aligned} m_1 - m_2 &= M\sin(\omega t + \theta) \\ m_3 - m_4 &= M\sin(\omega t + \theta - 2\pi/3) \\ m_5 - m_6 &= M\sin(\omega t + \theta - 4\pi/3) \end{aligned}\right\} \tag{B.6}$$

Before applying transformation from *abc*-rotating frame to *0dq*-stationary frame, (B.2) and (B.4) must be rearranged and put into appropriate matrix form as in (B.7), (B.8) and (B.9)

$$\begin{bmatrix} v_R \\ v_S \\ v_T \\ i_R \\ i_S \\ i_T \end{bmatrix} = \begin{bmatrix} Lp+R & 0 & 0 & 1 & 0 & 0 \\ 0 & Lp+R & 0 & 0 & 1 & 0 \\ 0 & 0 & Lp+R & 0 & 0 & 1 \\ 1 & 0 & 0 & -3Cp & 0 & 0 \\ 0 & 1 & 0 & 0 & -3Cp & 0 \\ 0 & 0 & 1 & 0 & 0 & -3Cp \end{bmatrix} \begin{bmatrix} i_{SR} \\ i_{SS} \\ i_{ST} \\ v_{CR} \\ v_{CS} \\ v_{CT} \end{bmatrix} \tag{B.7}$$

where $p=d/dt$

$$v_{dc} = \begin{bmatrix} M\sin(\omega t + \theta) & M\sin(\omega t + \theta - 120^\circ) & M\sin(\omega t + \theta - 240^\circ) \end{bmatrix} \begin{bmatrix} v_{CR} \\ v_{CS} \\ v_{CT} \end{bmatrix} \tag{B.8}$$

$$\begin{bmatrix} i_R \\ i_S \\ i_T \end{bmatrix} = \begin{bmatrix} M\sin(\omega t + \theta) \\ M\sin(\omega t + \theta - 120^\circ) \\ M\sin(\omega t + \theta - 240^\circ) \end{bmatrix} \begin{bmatrix} i_{dc} \end{bmatrix} \tag{B.9}$$

Transformation takes place first from abc-rotating frame to 0αβ-rotating frame, then to *0dq*-stationary frame. These are done by proper transformation matrices. These transformation matrices are derived referring to Fig.B.2 as in (B.10)-(B.13).

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = C_1 \begin{bmatrix} 0 \\ \alpha \\ \beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} 0 \\ \alpha \\ \beta \end{bmatrix} \tag{B.10}$$

$$\begin{bmatrix} 0 \\ \alpha \\ \beta \end{bmatrix} = C_2 \begin{bmatrix} 0 \\ d \\ q \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\omega t & -\sin\omega t \\ 0 & \sin\omega t & \cos\omega t \end{bmatrix} \begin{bmatrix} 0 \\ d \\ q \end{bmatrix} \tag{B.11}$$

$$C_1 = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \tag{B.12}$$

$$C_2 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\omega t & -\sin\omega t \\ 0 & \sin\omega t & \cos\omega t \end{bmatrix} \tag{B.13}$$

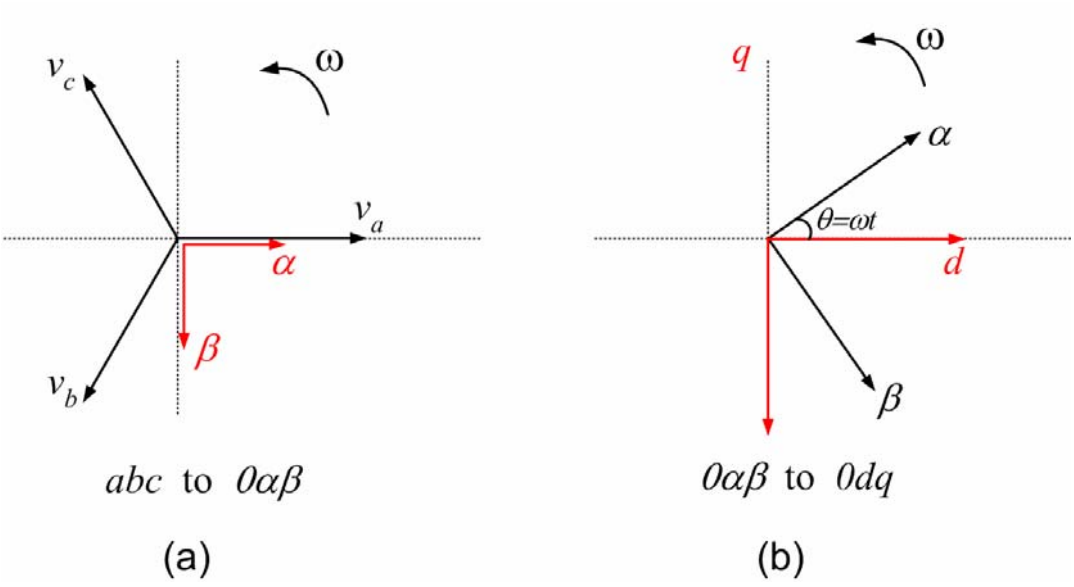


Figure B.2 Phasor diagrams used in deriving transformation matrices

Since transformation matrices are “orthogonal matrices”, such that they satisfy (B.14) and (B.15)

$$C_1^T C_1 = I \tag{B.14}$$

$$C_2^T C_2 = I \tag{B.15}$$

The transformation matrices are applied to both sides of (B.7) as in (B.16). These tranformation matrices are also applied to right-hand side of (B.8) and left-hand side of (B.9) as in (B.16) and (B.17), respectively.

$$C_1 C_2 \begin{bmatrix} v_0 \\ v_d \\ v_q \\ i_0 \\ i_d \\ i_q \end{bmatrix} = \begin{bmatrix} Lp+R & 0 & 0 & 1 & 0 & 0 \\ 0 & Lp+R & 0 & 0 & 1 & 0 \\ 0 & 0 & Lp+R & 0 & 0 & 1 \\ 1 & 0 & 0 & -3Cp & 0 & 0 \\ 0 & 1 & 0 & 0 & -3Cp & 0 \\ 0 & 0 & 1 & 0 & 0 & -3Cp \end{bmatrix} C_1\, C_2 \begin{bmatrix} i_{S0} \\ i_{Sd} \\ i_{Sq} \\ v_{C0} \\ v_{Cd} \\ v_{Cq} \end{bmatrix} \tag{B.16}$$

$$v_{dc} = \begin{bmatrix} M\sin(\omega t+\theta) & M\sin(\omega t+\theta-120^\circ) & M\sin(\omega t+\theta-240^\circ) \end{bmatrix} C_1 C_2 \begin{bmatrix} v_{C0} \\ v_{Cd} \\ v_{Cq} \end{bmatrix} \tag{B.17}$$

$$C_1 C_2 \begin{bmatrix} i_0 \\ i_d \\ i_q \end{bmatrix} = \begin{bmatrix} M\sin(\omega t+\theta) \\ M\sin(\omega t+\theta-120^\circ) \\ M\sin(\omega t+\theta-240^\circ) \end{bmatrix} \begin{bmatrix} i_{dc} \end{bmatrix} \tag{B.18}$$

Equations in (B.16) and (B.18) can be arranged as in (B.19) and (B.20) respectively.

$$\begin{bmatrix} v_0 \\ v_d \\ v_q \\ i_0 \\ i_d \\ i_q \end{bmatrix} = C_2^{-1} C_1^{-1} \begin{bmatrix} Lp+R & 0 & 0 & 1 & 0 & 0 \\ 0 & Lp+R & 0 & 0 & 1 & 0 \\ 0 & 0 & Lp+R & 0 & 0 & 1 \\ 1 & 0 & 0 & -3Cp & 0 & 0 \\ 0 & 1 & 0 & 0 & -3Cp & 0 \\ 0 & 0 & 1 & 0 & 0 & -3Cp \end{bmatrix} C_1\, C_2 \begin{bmatrix} i_{S0} \\ i_{Sd} \\ i_{Sq} \\ v_{C0} \\ v_{Cd} \\ v_{Cq} \end{bmatrix} \tag{B.19}$$

$$\begin{bmatrix} i_0 \\ i_d \\ i_q \end{bmatrix} = C_2^{-1} C_1^{-1} \begin{bmatrix} M\sin(\omega t+\theta) \\ M\sin(\omega t+\theta-120°) \\ M\sin(\omega t+\theta-240°) \end{bmatrix} [i_{dc}] \tag{B.20}$$

In applying transformation matrices, the effect of operator "*p*" should be noted as given in (B.21). After applying transformation matrices to (B.17), (B.19) and (B.20), expressions in 0dq-stationary frame are obtained and given in (B.22), (B.23) and (B.24).

$$(Lp+R)\cos\omega t = -\omega L\sin\omega t + \cos\omega t\,(Lp+R) \tag{B.21}$$

$$\begin{bmatrix} v_0 \\ v_d \\ v_q \\ i_0 \\ i_d \\ i_q \end{bmatrix} = \begin{bmatrix} Lp+R & 0 & 0 & 1 & 0 & 0 \\ 0 & Lp+R & -\omega L & 0 & 1 & 0 \\ 0 & \omega L & Lp+R & 0 & 0 & 1 \\ 1 & 0 & 0 & -3Cp & 0 & 0 \\ 0 & 1 & 0 & 0 & -3Cp & 3\omega C \\ 0 & 0 & 1 & 0 & -3\omega C & -3Cp \end{bmatrix} \begin{bmatrix} i_{S0} \\ i_{Sd} \\ i_{Sq} \\ v_{C0} \\ v_{Cd} \\ v_{Cq} \end{bmatrix} \tag{B.22}$$

$$\begin{bmatrix} i_0 \\ i_d \\ i_q \end{bmatrix} = \begin{bmatrix} 0 \\ \sqrt{\frac{3}{2}}M\sin\theta \\ -\sqrt{\frac{3}{2}}M\cos\theta \end{bmatrix} [i_{dc}] \tag{B.23}$$

$$v_{dc} = \begin{bmatrix} 0 & \sqrt{\frac{3}{2}}M\sin\theta & -\sqrt{\frac{3}{2}}M\cos\theta \end{bmatrix} \begin{bmatrix} v_{C0} \\ v_{Cd} \\ v_{Cq} \end{bmatrix} \tag{B.24}$$

So far, the differential equations in *abc*-rotating frame have been transformed into *0dq*-stationary frame. From these equations, state-space representation of CSC can be derived. In this derivation zero sequence components are ignored since balanced system has already been assumed. Using (B.22), (B.23) and (B.24) and choosing state variables as i_{sd}, i_{sq}, v_{cd}, v_{cq} and i_{dc} state-space equations of CSC can be found as in (B.25).

$$\frac{d}{dt}\begin{bmatrix} i_{sd} \\ i_{sq} \\ v_{cd} \\ v_{cq} \\ i_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\omega & -\frac{1}{L} & 0 & 0 \\ \omega & -\frac{R}{L} & 0 & -\frac{1}{L} & 0 \\ \frac{1}{3C} & 0 & 0 & -\omega & -\sqrt{\frac{3}{2}}\frac{M}{3C}\sin\theta \\ 0 & \frac{1}{3C} & \omega & 0 & -\sqrt{\frac{3}{2}}\frac{M}{3C}\cos\theta \\ 0 & 0 & \sqrt{\frac{3}{2}}\frac{M}{L_{dc}}\sin\theta & \sqrt{\frac{3}{2}}\frac{M}{L_{dc}}\cos\theta & -\frac{R_{dc}}{L_{dc}} \end{bmatrix}\begin{bmatrix} i_{sd} \\ i_{sq} \\ v_{cd} \\ v_{cq} \\ i_{dc} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_d \\ v_q \end{bmatrix} \quad \text{(B.25)}$$

From the state-space representation of CSC STATCOM in (B.25), equivalent circuit in dq-statioanry frame can be found as given in Fig.B.3. Advantage of the equivalent circuit in Fig.B.3 is that all quantities at supply frequency become dc-quantity in steady-state as shown in Fig.B.3b. This means that analysis of this circuit is algebraic rather than vectorial. Based on the transformation matrices and equivalent circuits, active and reactive power can be defined as in (B.26) and (B.27).

$$P = V_d\, I_{sd} + V_q\, I_{sq} \quad \text{(B.26)}$$

$$Q = -V_d\, I_{sq} + V_q\, I_{sd} \quad \text{(B.27)}$$

The state space representation of CSC based STATCOM in (B.25) has the standard form given in (B.26).

$$\dot{x} = Ax + Bu \quad \text{(B.26)}$$

where x is the state vector (5x1)
A is the constant matrix (5x5)
B is the constant matrix (5x2)
u is the input vector (2x1)

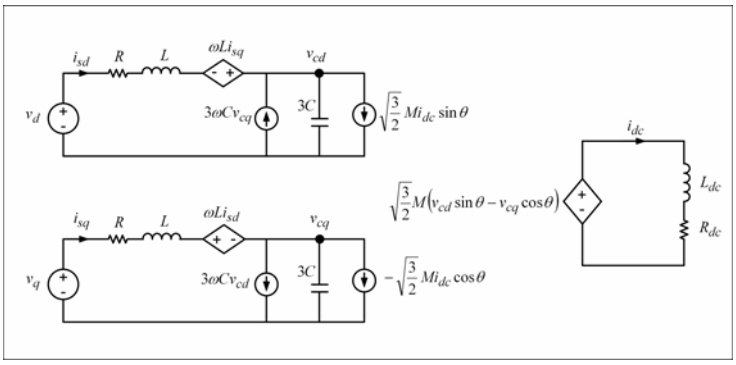
Supply voltages are given as in the form of input vector in (B.25). They have been defined for abc-rotating frame in (B.1). Applying transformation matrices to (B.1) yields the input vector u as in (B.27).

$$\begin{bmatrix} v_0 \\ v_d \\ v_q \end{bmatrix} = C_2^{-1} C_1^{-1} \begin{bmatrix} v_R \\ v_S \\ v_T \end{bmatrix} = \begin{bmatrix} 0 \\ \sqrt{\frac{3}{2}} V \\ 0 \end{bmatrix} \tag{B.27}$$

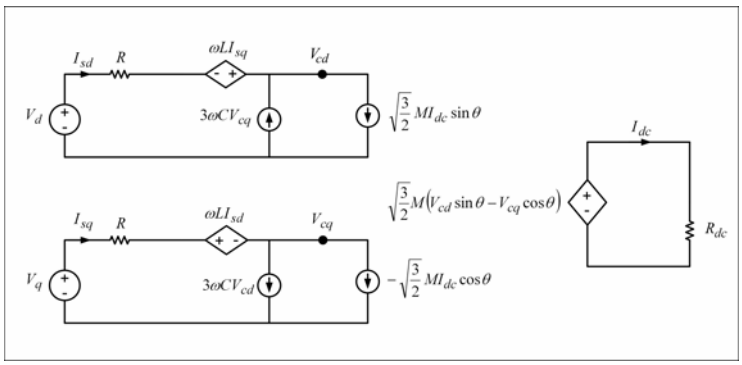
From the state space equations given in (B.25) and (B.26), steady-state expressions can be found by equating *dx/dt* =0 and solving for *x* as in (B.38).

$$x = A^{-1} B u \tag{B.38}$$

Although expressions for state variables can be derived by solving (B.38) after a very long elementary matrix operations, the result will be too complicated. Therefore, rather than deriving the expressions, numerical solution can be easily found for the given system parameters by using computer programmes, such as MATLAB.



(a) for transient state



(b) for steady-state

Figure B.3 Equivalent circuit of CSC based STATCOM in dq-stationary frame

APPENDIX C

SIMULATION MODEL OF CURRENT SOURCE CONVERTER BASED STATCOM IN PSCAD/EMTDC

The general view of simulation model is as shown in Fig.C.1. This simulation model is implemented in PSCAD/EMTDC V4.2.0. The simulation time step is taken as 1μsec and simulation duration is made to be 1sec.

In Fig.C.2, the details of “Power Stage” block is illustrated. Since the exact models for IGCT and fast recovery diode are not available, GTO and diode models of PSCAD has been used. Although their switching characteristics can not be modeled, their conduction voltages are specified. In order to realize asymmetric IGCT, an anti-parallel diode is connected across the GTO. Snubber components are used across the power semiconductors in order to find the snubber losses by simulation. The commutation inductances are also inserted into the model so that the effects of snubber can be observed.

In Fig.C.3, the details are given for the input filter which is shown as “Filter” block in Fig.C.1. Filter reactor and capacitors are modeled including their their stay resistor and inductance, which may affect the filtering performance of the input filter. The current ratings of each capacitor has been determined by the use of this model.

The reactive power control performance of the model has been achieved by giving step changes as reference reactive power from variable input to control system (Fig.C.1). The reactive power of STATCOM is measured with reactive power measuring block named as “QR Karti” in Fig.C.1. The details of “QR Karti” is given in Fig.C.4.

The control system is composed of “CONTROLLER”, “reactive_power_controller”, and “current_controller” blocks as shown in Fig.C.1. Each block contains a FORTRAN code, which is designed same as the actual code

in DSP of prototype system. Their flowchart are given in Fig.C.5-C.7. Calculations in these blocks are also made as “fixed-point” at certain sampling intervals, which are determined by zero-crosses of supply line-to-line voltages. PSCAD/EMTDC executes these block at each simulation time step of 1μsec. The code of these blocks are devised in such a way that each block can accept the output of preeceding block with a synchronizing signal. This realizes the control system embeded into DSP of developed prototype.

Switching patterns of power semiconductors are generated with the “STATCOM-Control” block shown in Fig.C.1. The details of “STATCOM_Control” block is given in Fig.C.8 and Fig.C.9. This block generates the switching patterns with respect to supply line-to-line voltages (v_{ca}, v_{ab}, v_{bc}) with the use of “mode” and “aci” signals, which are generated by “current_controller” as shown in Fig.C.1. Inside “STATCOM_Control” block, there is “Zero_Cross_Detector” block, which generates “main_ZC” and “other_ZC” signals for synchronization of switching signals. The details of “Zero_Cross_Detector” block is shown in Fig.C.10. This block generates zero-crosses, which are leading the actual zero-crosses of the line-to-line voltages at 1kV by 900μsec.

The “region_counter” block which is shown in Fig. C.8 contains a FORTRAN code and its flowchart is given in Fig.C11. The “pulse_generator” block generates P1, P2 and P3 signals defined in Chapter 3.9.2. This block also contains a FORTRAN code, which is explained by the flowchart in Fig.C.12. The generation of switching signals for each power semiconductor is shown in Fig.C.9. The “Delay” block in Fig.C.9 is used for overlapping the switching signals and its details is illustrated in Fig.C.13.

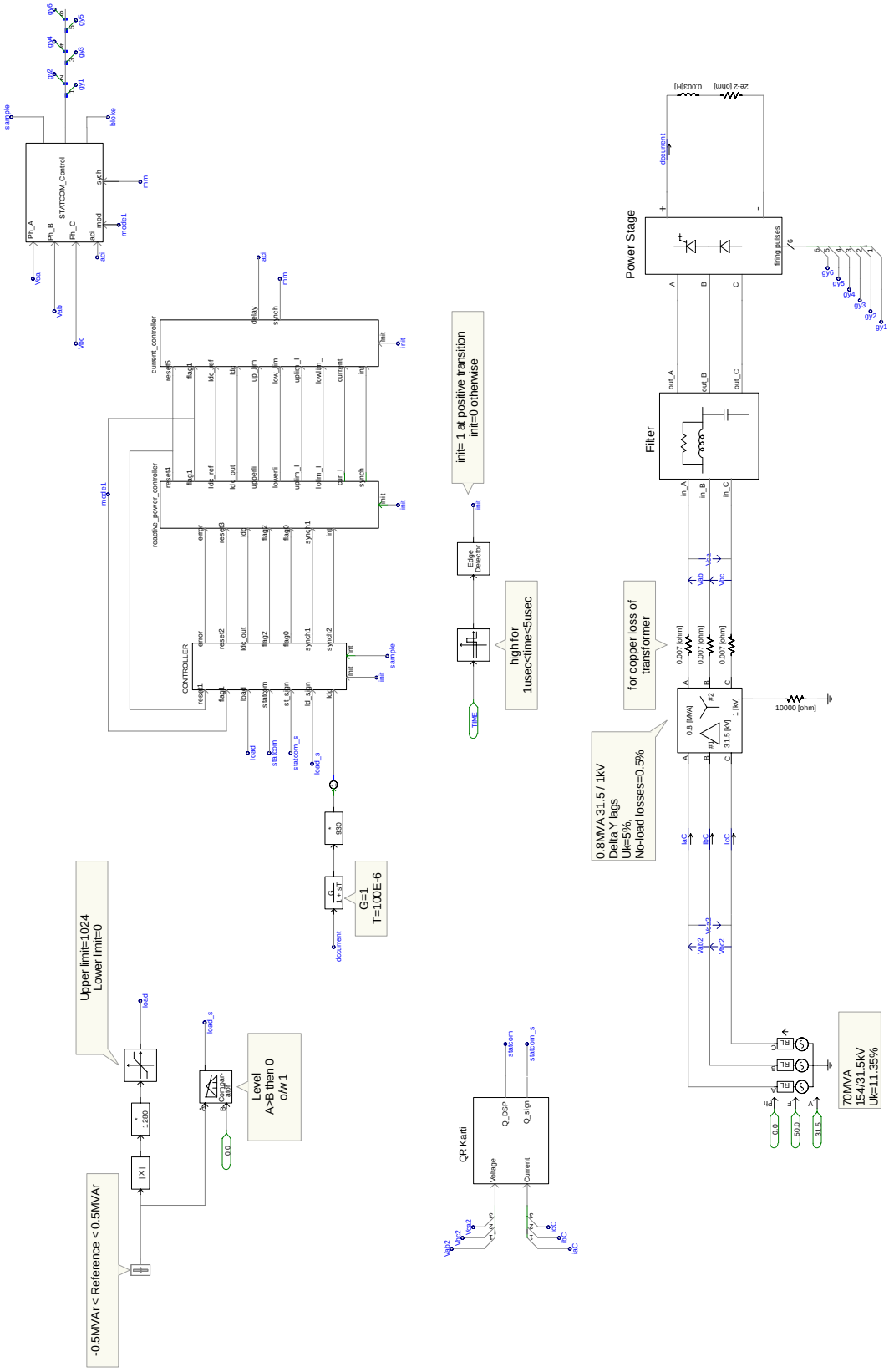


Figure C.1 General view of simulation model of CSC based STATCOM in PSCAD/EMTDC

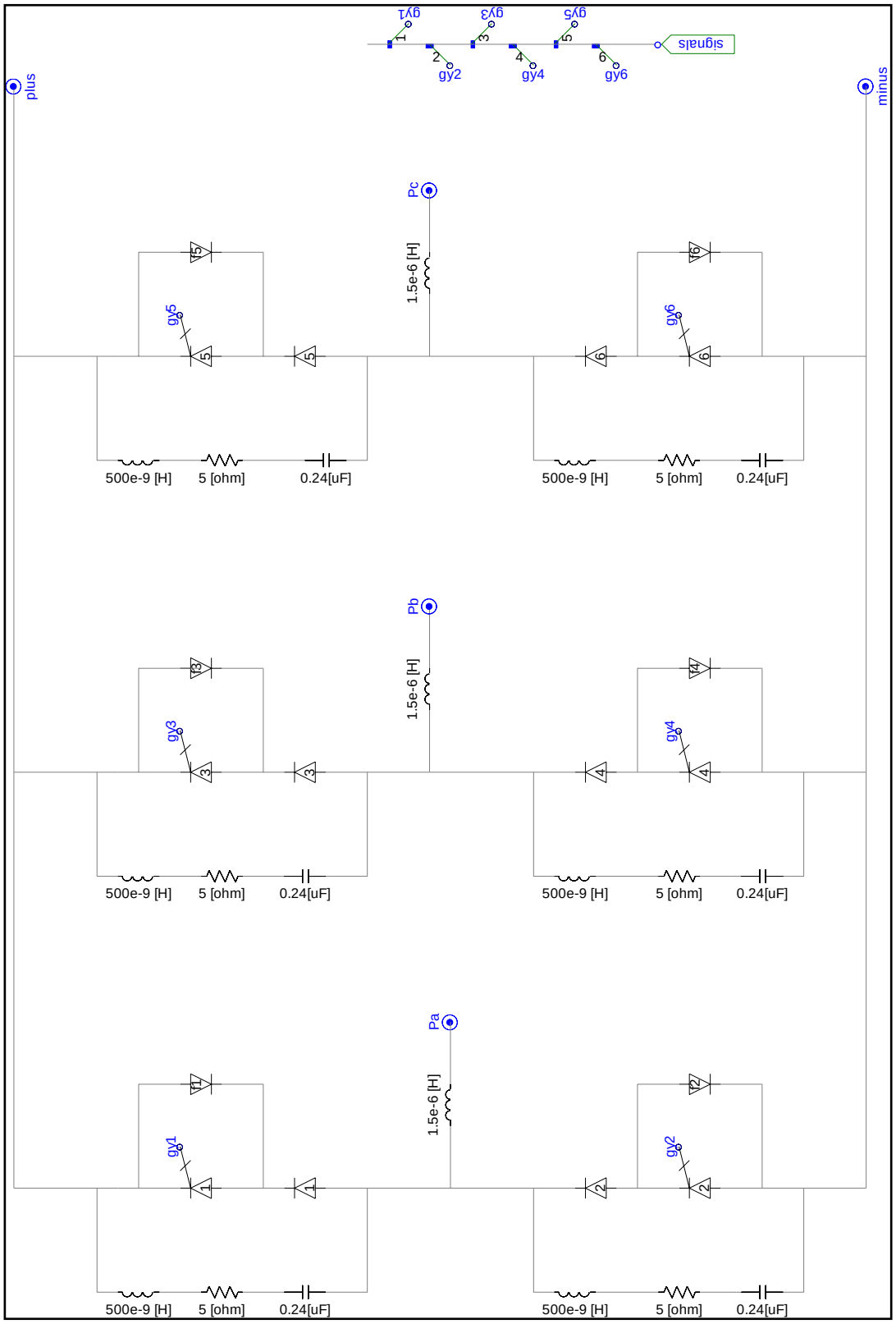
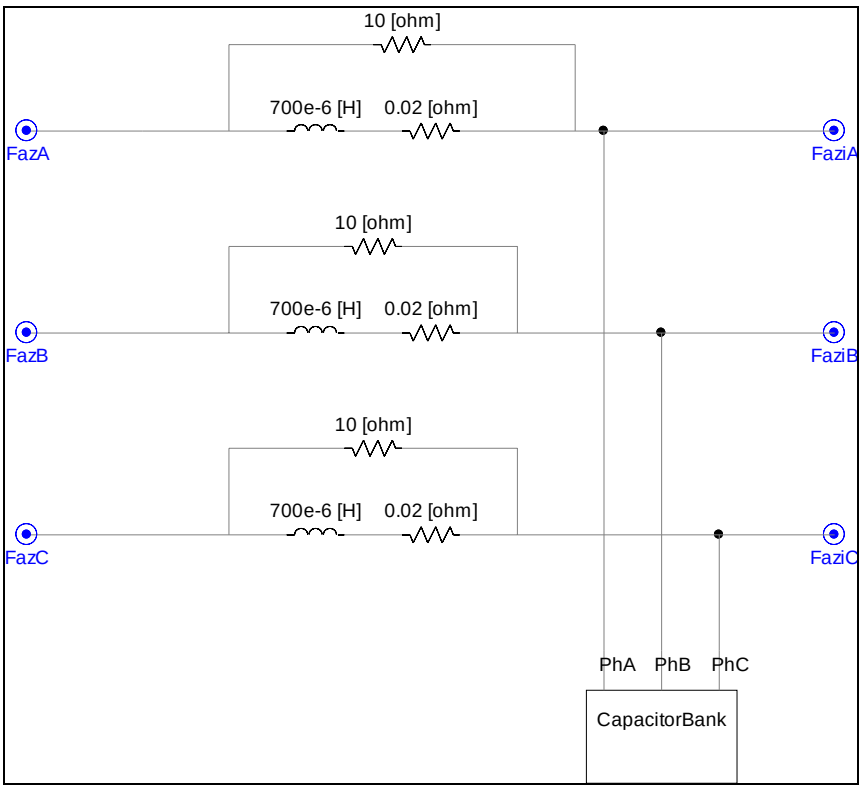
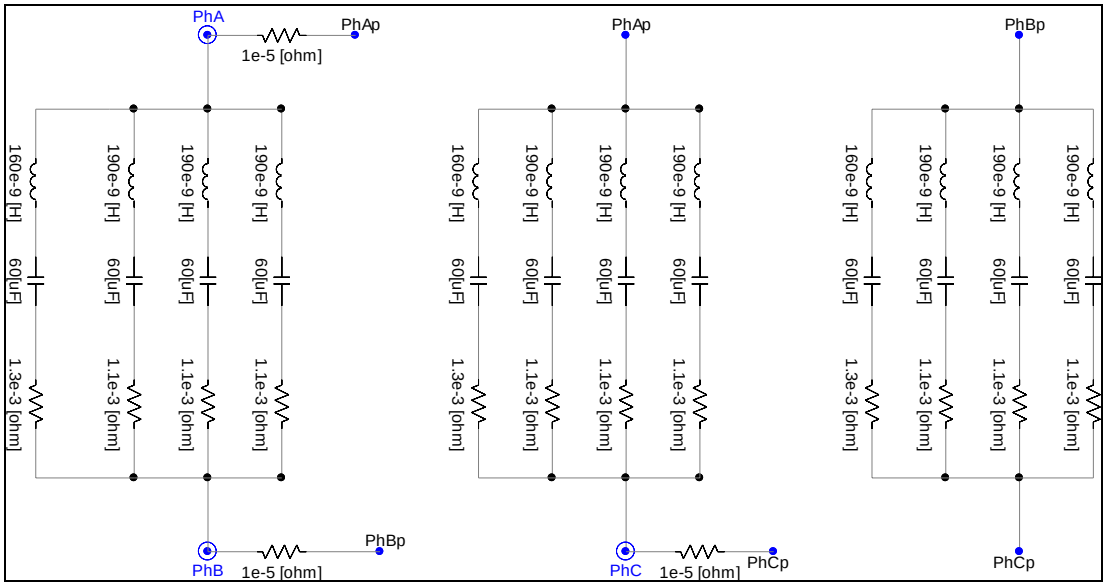


Figure C.2 The details of “Power Stage” block in Fig.C.1



(a)



(b)

Figure C.3 (a) The details of "Filter" block in Fig.C.1
(b) details of "Capacitor Bank" block

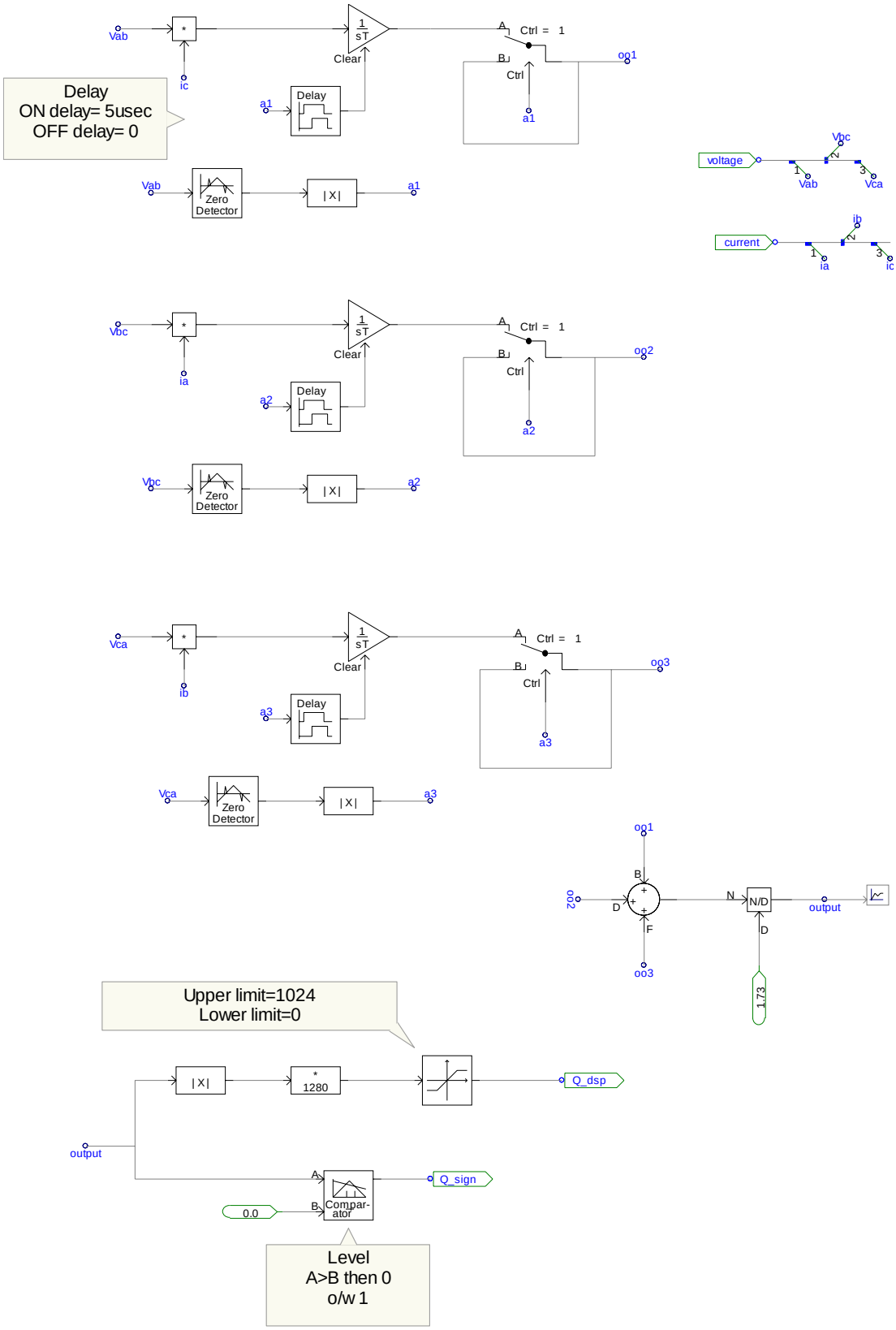


Figure C.4 The details of "QR Karti" block in Fig.C.1

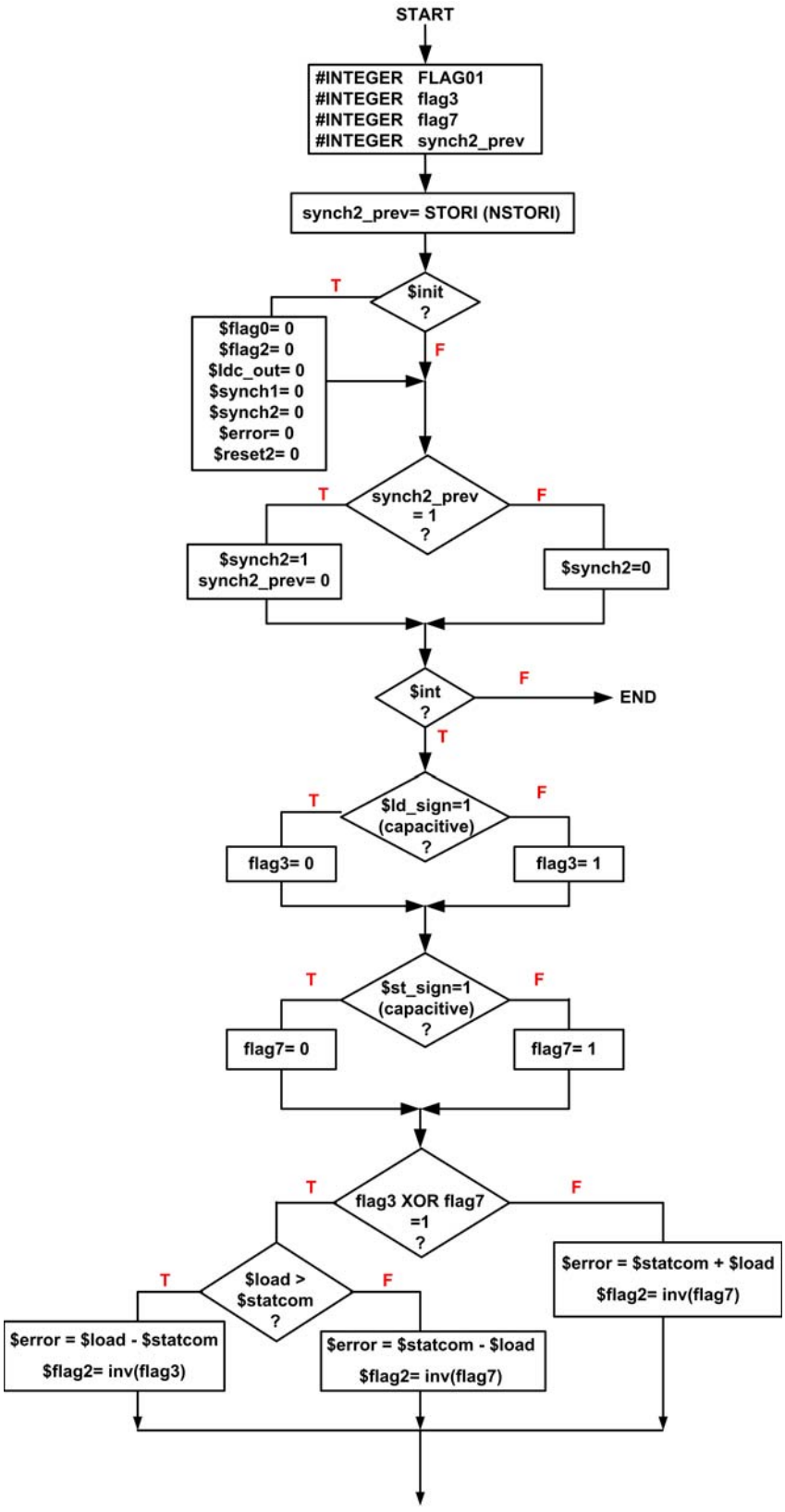


Figure C.5 Flowchart of "CONTROLLER" block in Fig.C.1

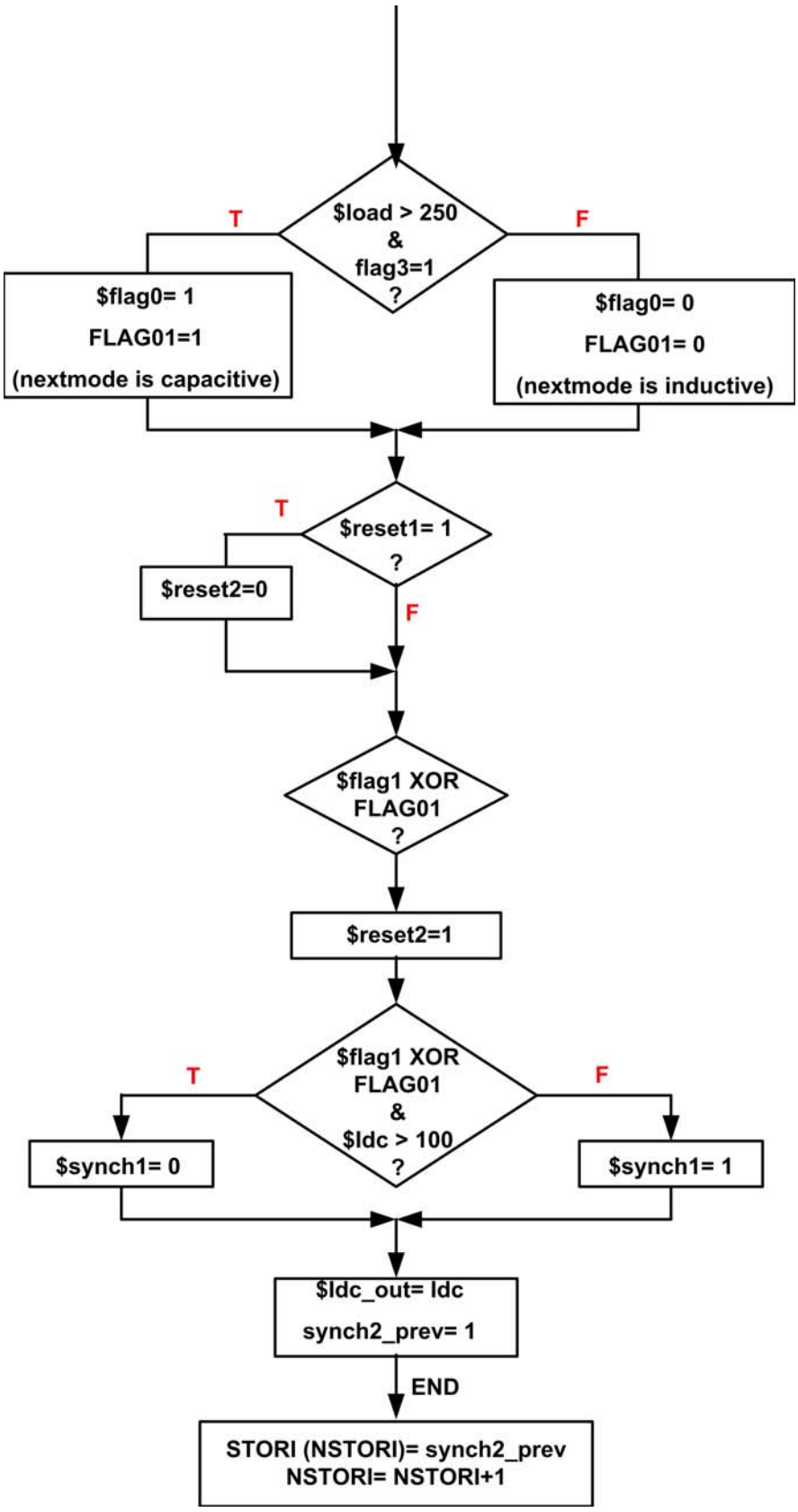


Figure C.5 (cont'd) Flowchart of "CONTROLLER" block in Fig.C.1

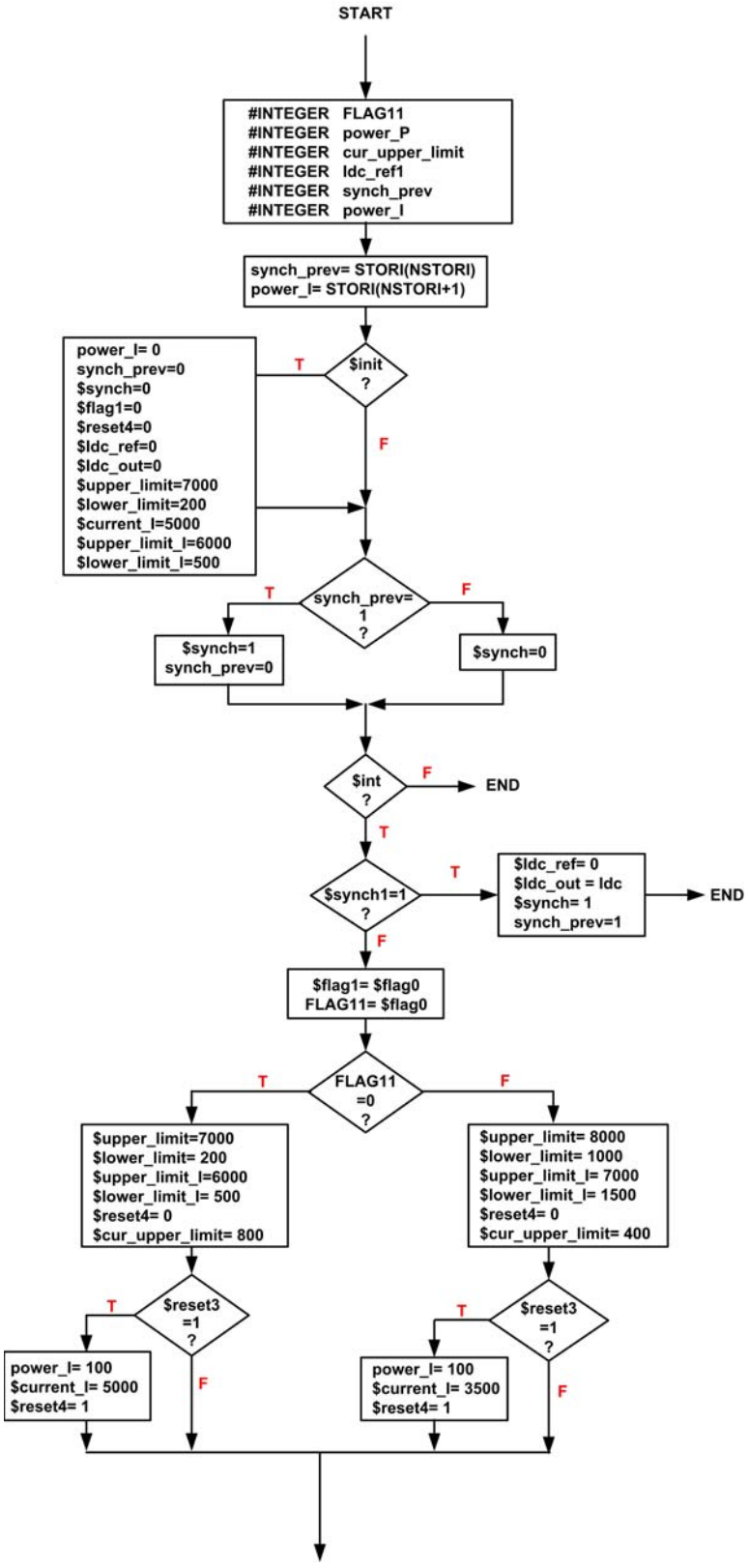


Figure C.6 Flowchart of "Reactive Power Controller" block in Fig.C.1

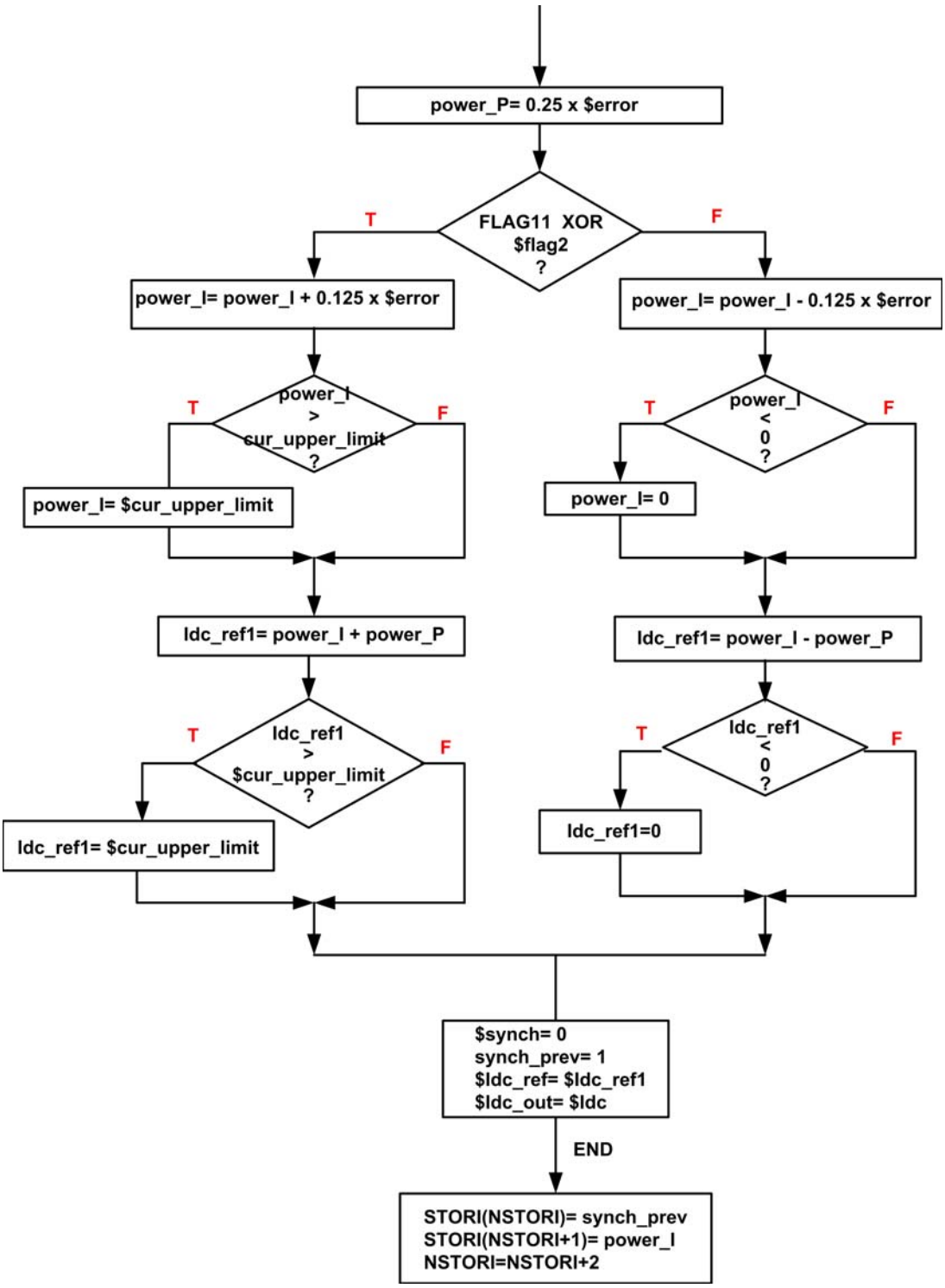


Figure C.6 (cont'd) Flowchart of "Reactive Power Controller" block in Fig.C.1

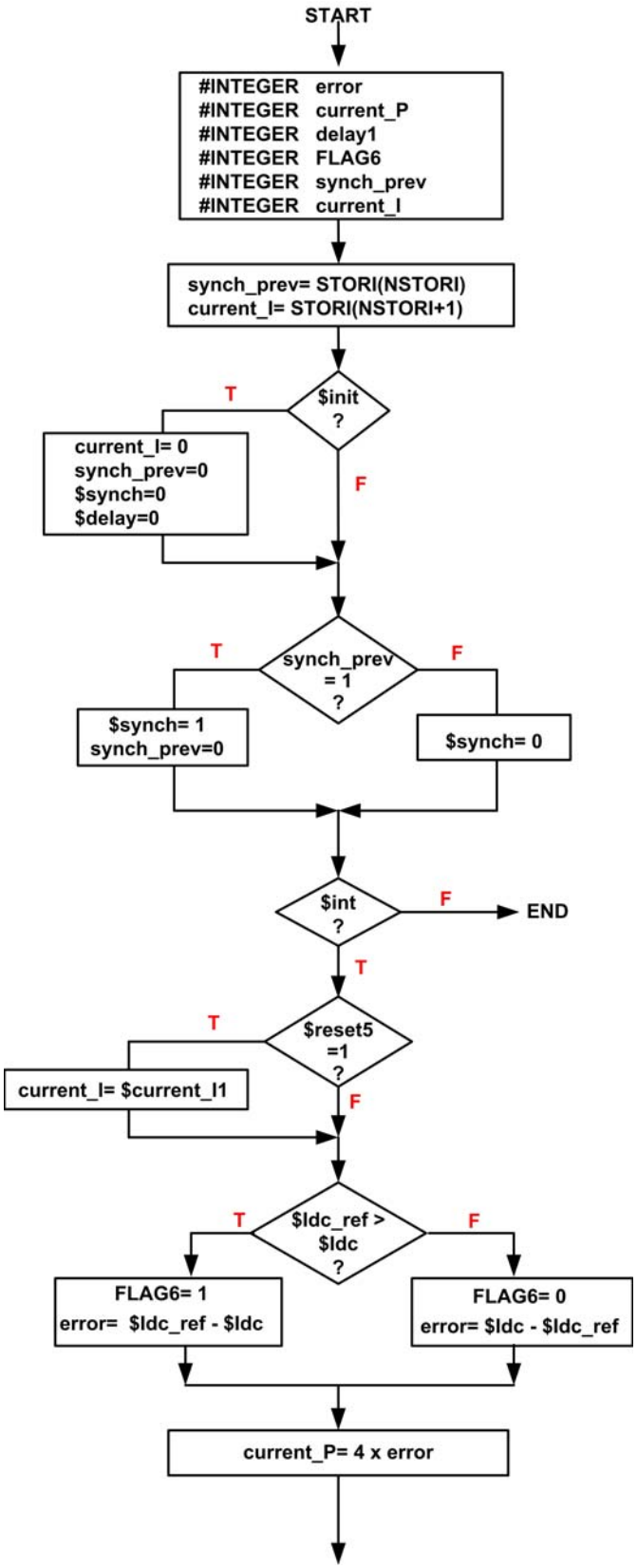


Figure C.7 Flowchart of "Current Controller" block in Fig.C.1

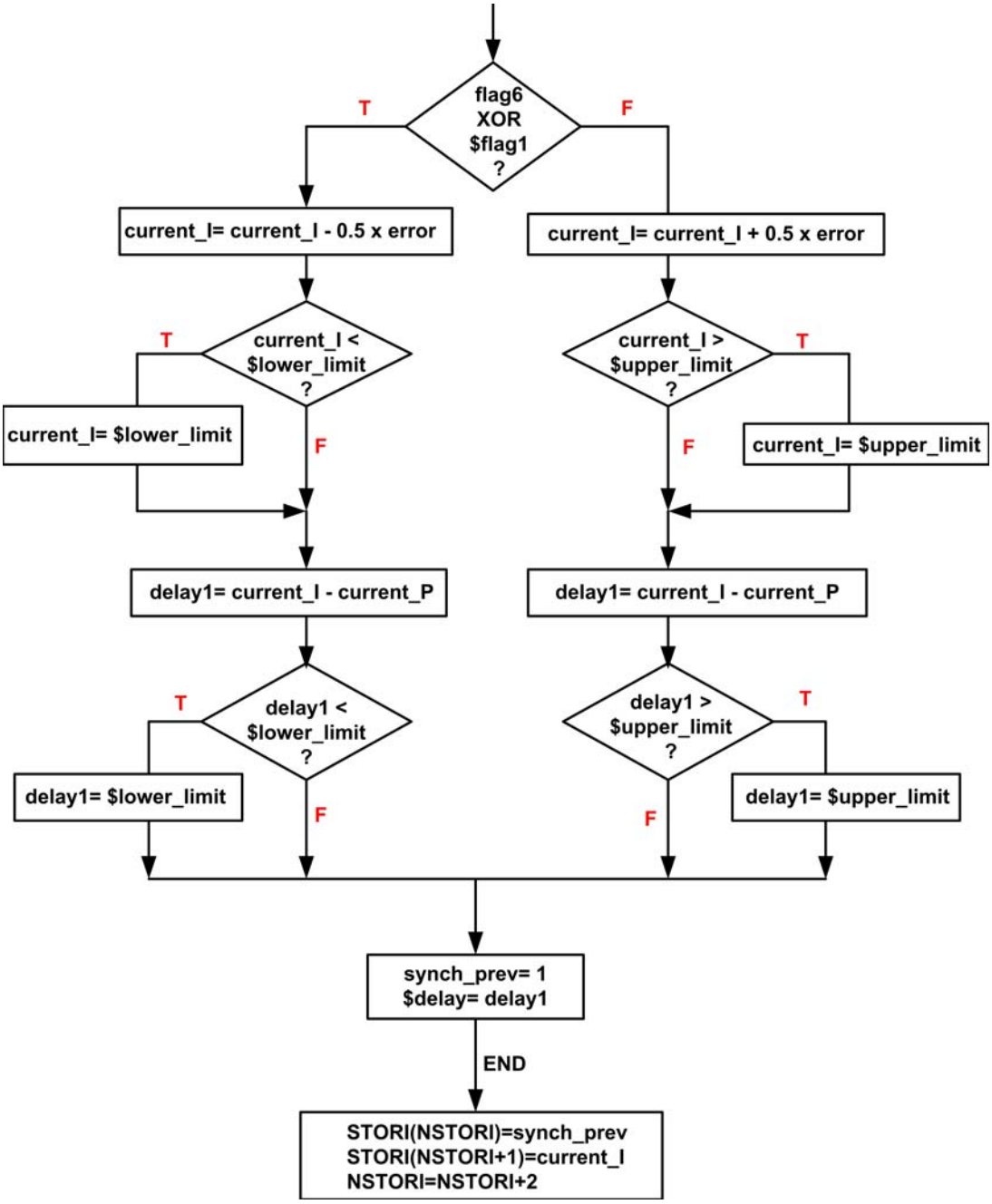


Figure C.7 (cont'd) Flowchart of "Current Controller" block in Fig.C.1

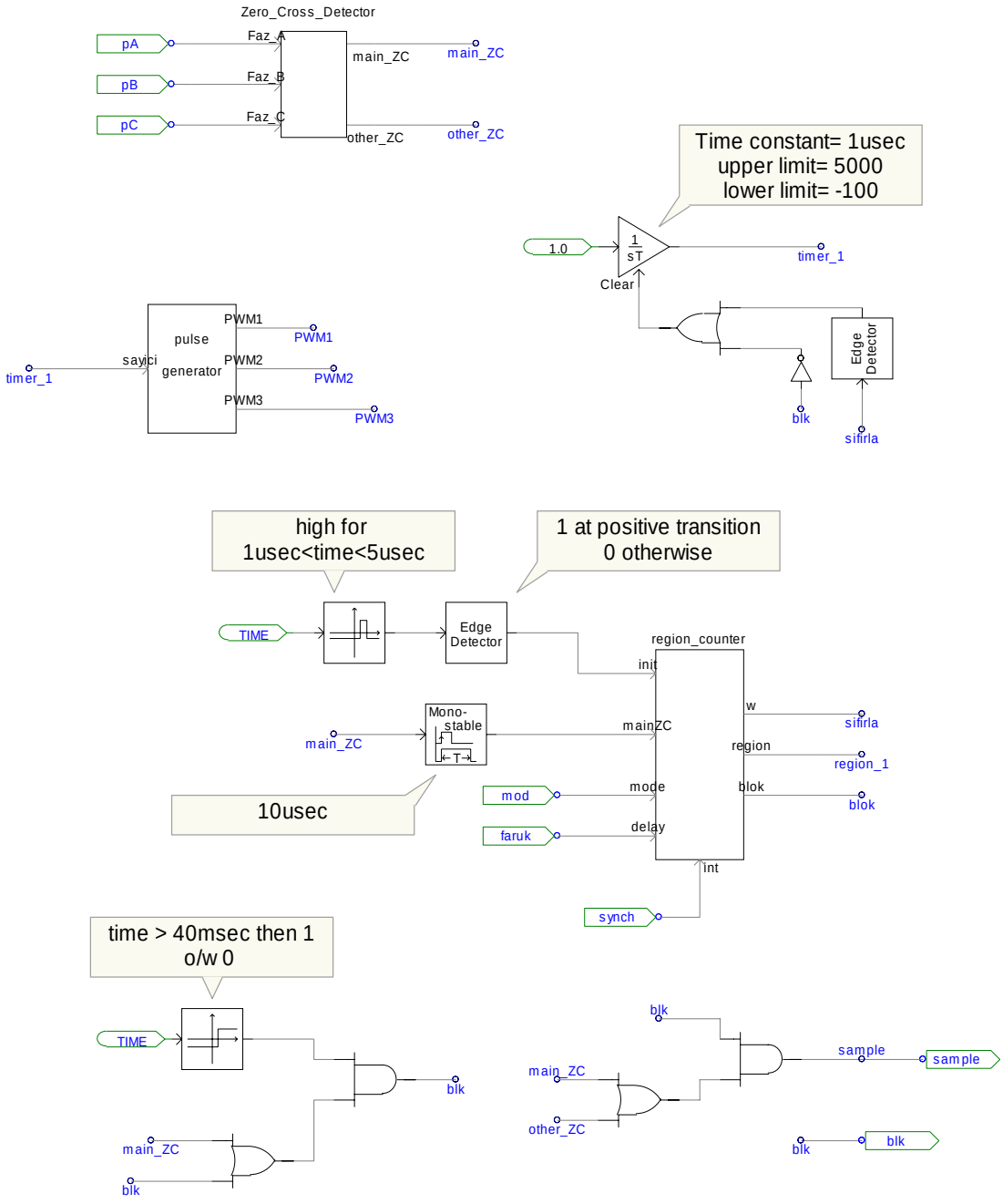


Figure C.8 Details of “STATCOM_Control” block shown in Fig.C.1

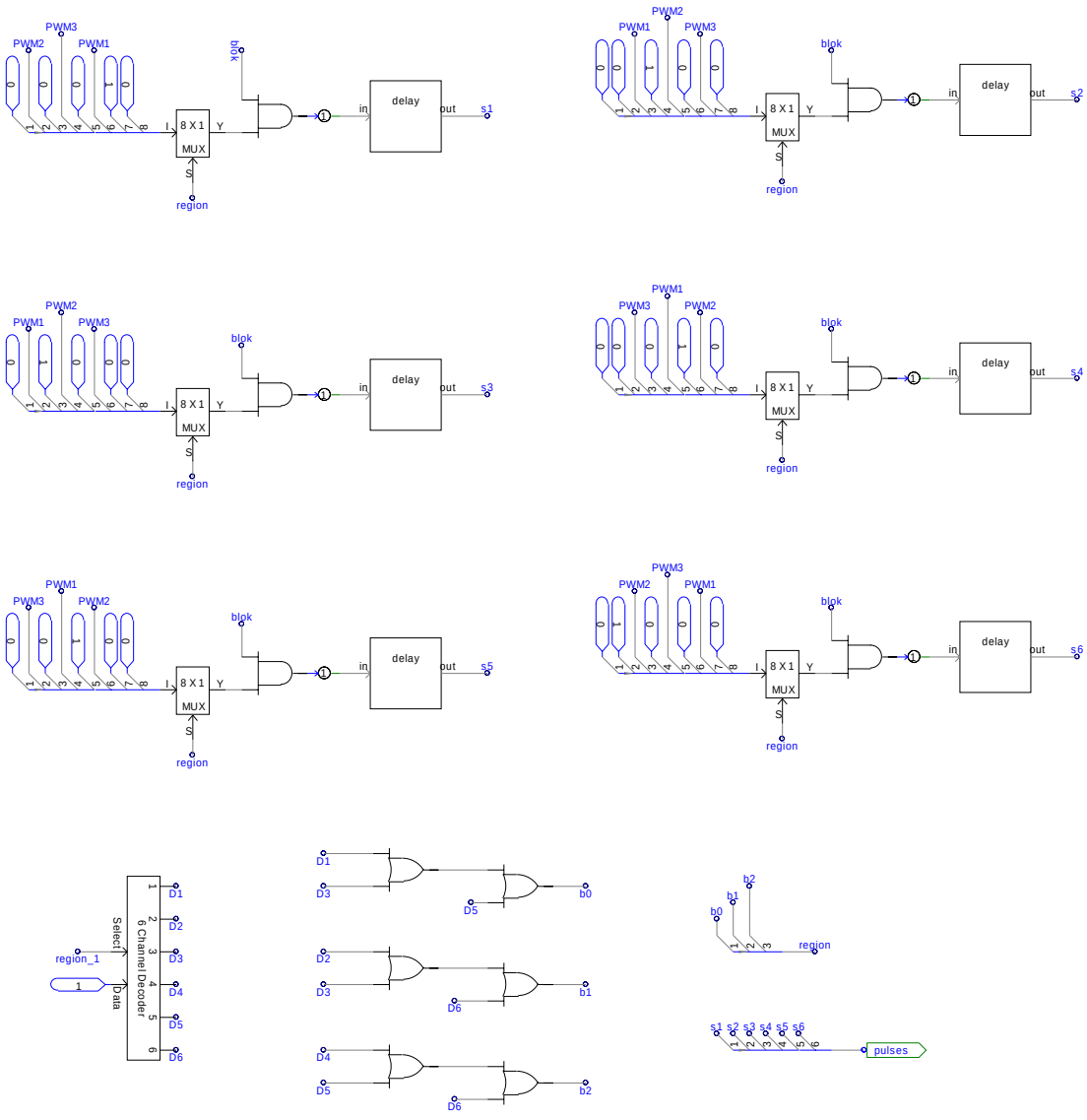


Figure C.8 (cont'd) Details of "STATCOM_Control" block shown in Fig.C.1

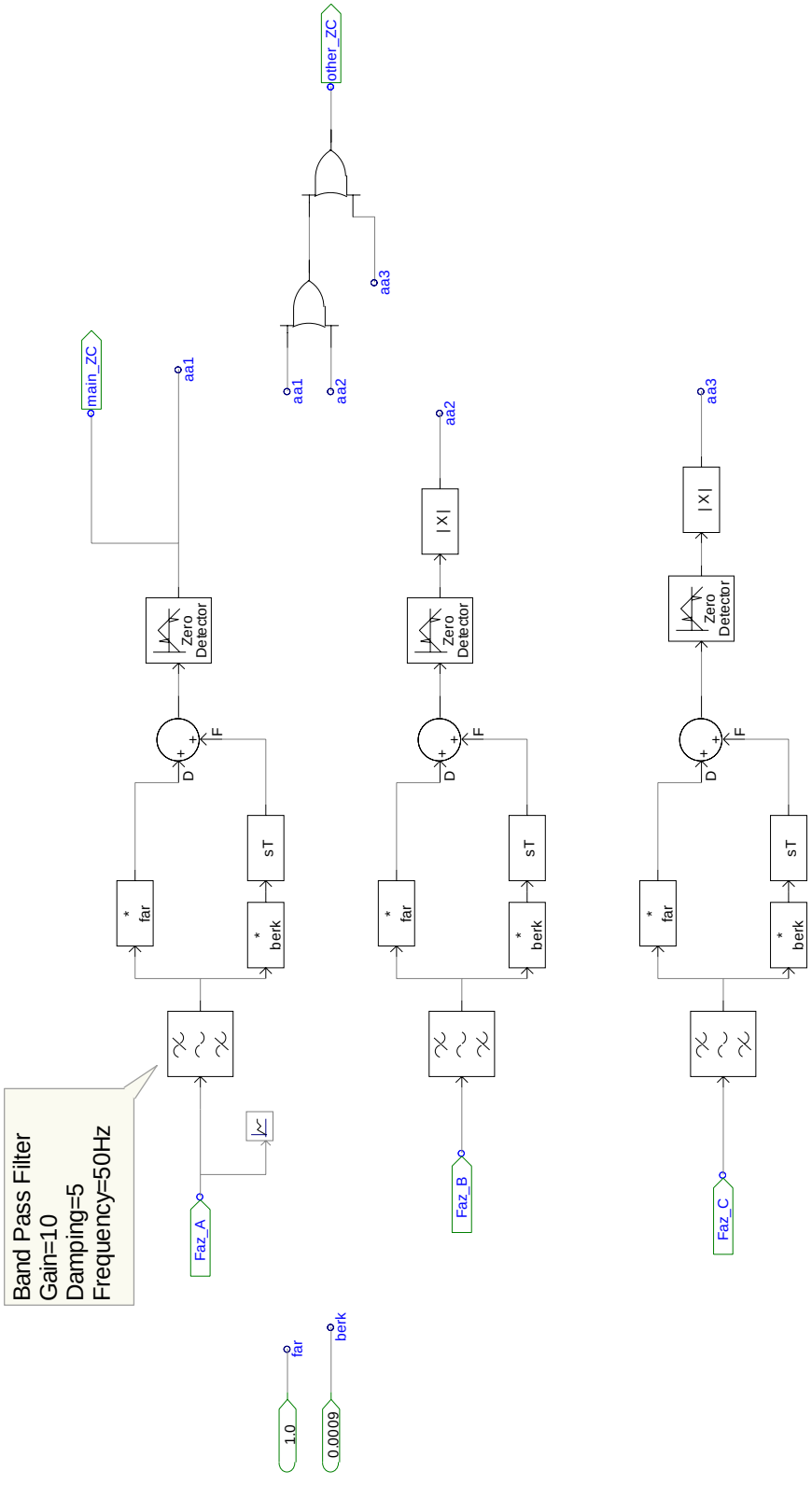


Figure C.9 Details of “Zero-Cross_Detector ” block in Fig.C.8

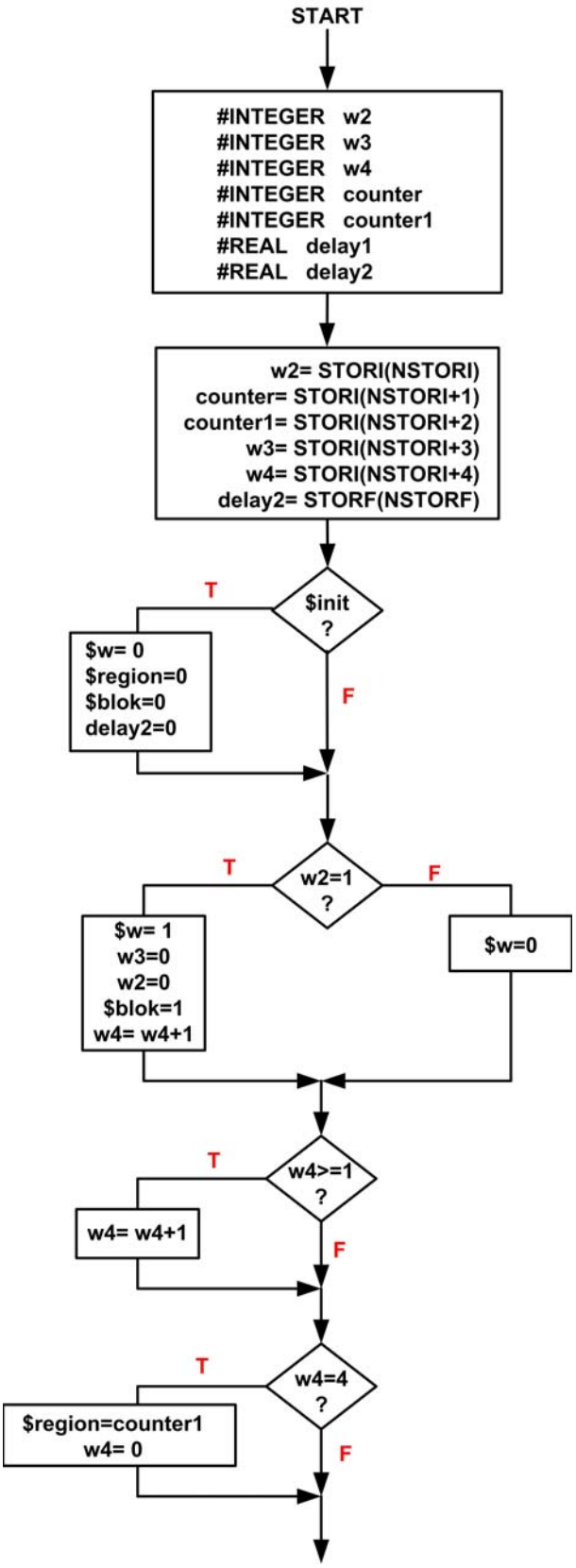


Figure C.10 Flowchart of “region_counter” block in Fig.C.8

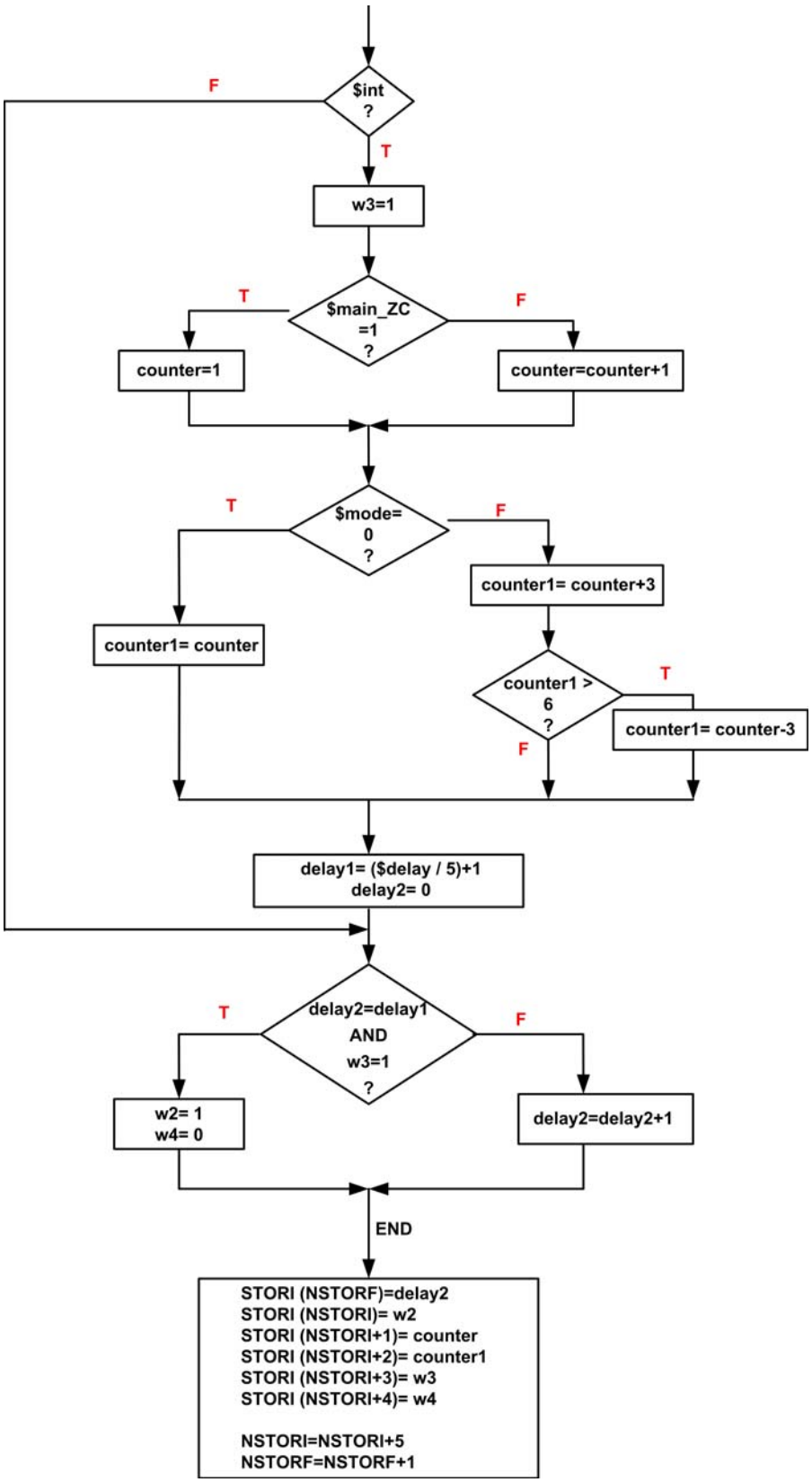


Figure C.10 (cont'd) Flowchart of "region_counter" block in Fig.C.8

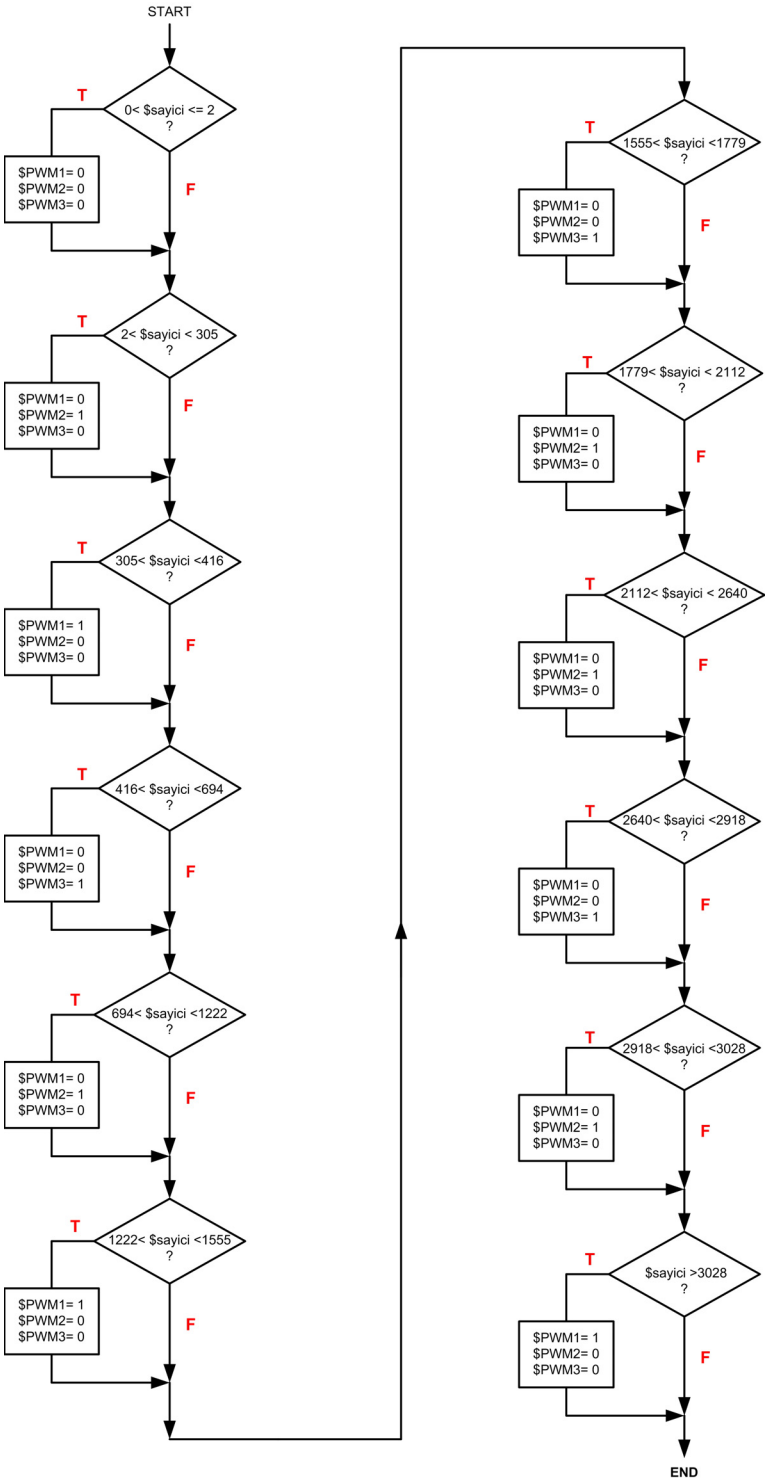


Figure C.11 Flowchart of "pulse_generator" block in Fig.C.8

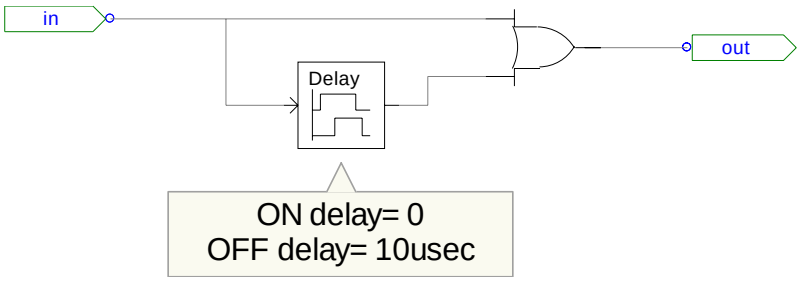


Figure C.12 Details of “delay” block in Fig.C.9

APPENDIX D

DERATING CURVES OF IGCT

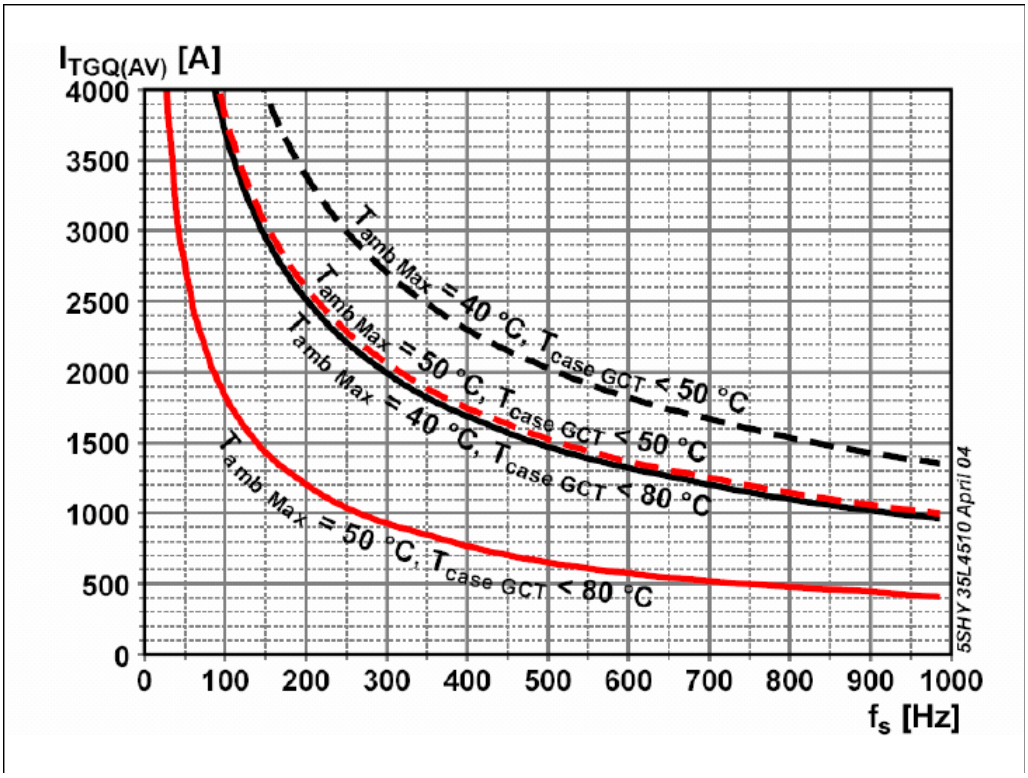


Figure D.1 Maximum turn-off current vs. frequency for lifetime operation of on-board capacitors 20 years

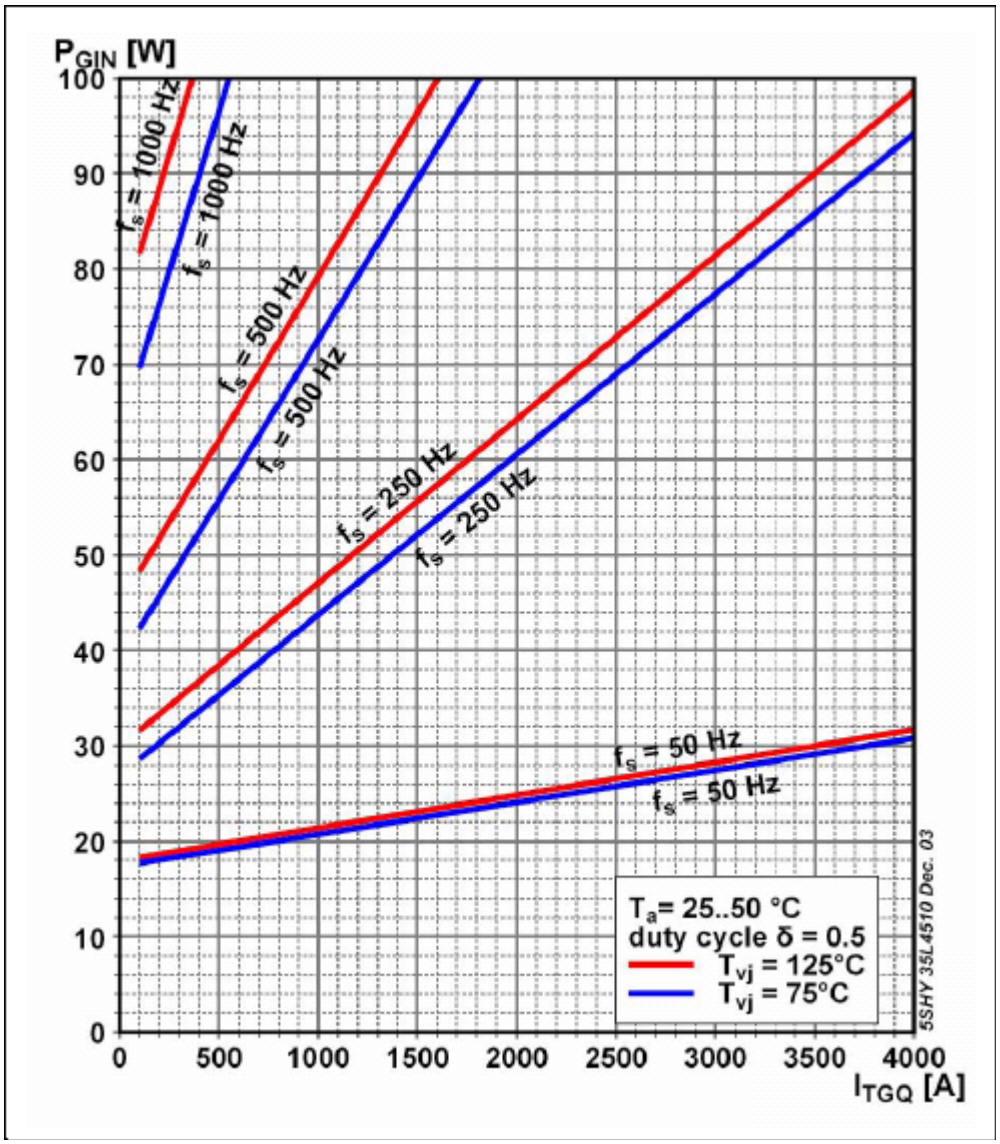


Figure D.2 Maximum Gate Unit input power vs. turn-off current of IGCT (specified to be 100W maximum for the chosen IGCT)

APPENDIX E

METHOD FOR THEORETICAL CALCULATION OF POWER SEMICONDUCTOR LOSSES IN CURRENT SOURCE CONVERTER

In Chapter 3, the most suitable candidate power semiconductors are compared in terms of their losses in Table 3.5. The results given in Table 3.5 are calculated by using the simulation result given in Fig.3.7 and the values in the datasheets of the correspoding power semiconductors. Here, the method used in calculating these power losses will be explained.

E.1. Conduction Loss

The conduction loss in power semiconductor occurs due to voltage drop across power semiconductor during conduction. For each power semiconductor, there exists an “on-state characteristic” curve, which illustrates voltage drop across the power semiconductor for the magnitude of the current carried by the power semiconductor. These curves are generally given for T_{vj}= 25°C and T_{vj}= 125°C. The curve for T_{vj}= 125°C should be considered.

In CSC based STATCOM, the magnitude of the current through power semiconductors are almost level and equal to the dc-link current (I_{dc}) as illustrated in Fig.3.7 due to the presence of relatively large dc-link reactor. The magnitude of current through each power semiconductor can be taken as nearly 700A during conduction from Fig.3.7. The maximum forward voltage drop (V_F) of the power semiconductors, obtained form their datasheet at 700A are given in Table E.1.

From the simulation results in Fig.3.7, mean value of current (I_{mean}) through each power semiconductor is found as 244A. Then, conduction loss of each power semiconductor can be calculated as

$$P_{conduction} = V_F \times 244 \qquad \text{(E.1)}$$

Table E.1. Maximum voltage drop across the power semiconductors at 700A and T_{vj}=125°C

	IGCT 5SHY35L4510	Diode D911SH45	IGBT CM1200HC-66H	Diode RM1200HA-66S	SGCT GCU15CA-130
V_F	1.6V	3V	2.9V	2.5V	5.6V

E.2. Turn-on Loss

There are two parts of turn-on loss in CSC based STATCOM: i) turn-on loss due to the switching of fully controllable power semiconductor (such as IGCT, IGBT or Mosfet), and ii) turn-on loss due to the forward recovery of seriesly connected diode.

Typical voltage and current waveforms across the diode during forward recovery are given in Fig.E.1. Forward recovery loss is dependent on forward recovery voltage (V_{FR}) and it increases with di_F/dt, hence turn-on loss of diode also increases. However, this characteristic is not defined for all diodes by the manufacturers. Since di_F/dt is less than 1000A/μsec in IGCT applications and V_{FR} is relatively small (less than 100V), forward recovery loss of diode during turn-on is not considered in comparison of candidate power semiconductors.

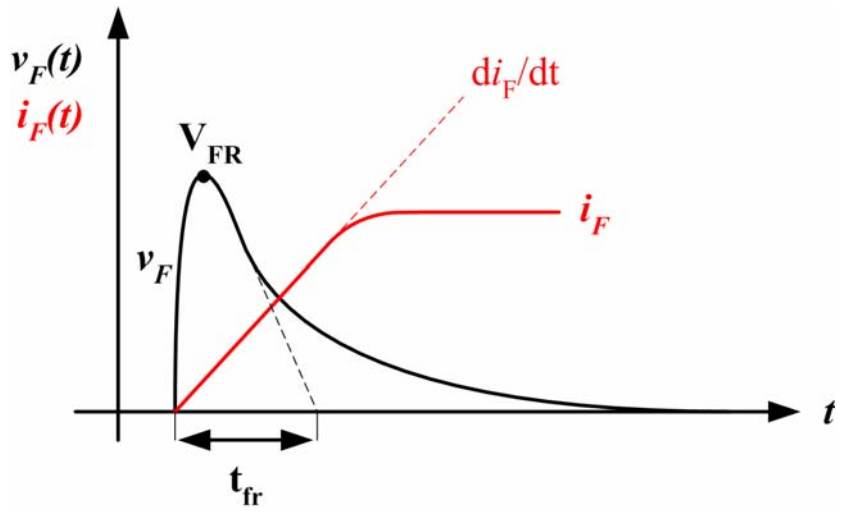


Figure E.1 Typical voltage and current waveforms of fast recovery diode during turn-on (not-to-scale) [91]

For fully controllable switches in CSC-STATCOM, turn-on losses occur only during device turn-on period, as explained in Chapter 2. Turn-on energy (E_{on}) is calculated at each device turn-on of power semiconductor. The instants at which power semiconductor undergoes device turn-on are defined by encircled B in Fig.4.1. and Fig.4.2. For this purpose, the magnitude of voltage (V_1) across the power semiconductor just before device turn-on and the magnitude of current (I_1) through the power semiconductor after device turn-on should be determined from the simulation results for device turn-on instants as illustrated in Fig.E.2. In datasheets, the value of E_{on} is generally given for certain switching conditions, such as V_0, I_0 and T_{vj}. Typical values of E_{on} for different power semiconductors can be found from their datasheets as given in Table E.2. From simulation results in Fig.3.7, the values of V_1 and I_1 are given in Table E.3 according to the current pulse in Fig.3.7. Then, using the values of E_{on} in Table E.2 and V_1, I_1 in Table E.3 turn-on loss of fully controllable power semiconductors are calculated as in (E.2).

$$P_{turn-on} = \frac{E_{on}}{V_0 I_0} \times (1230 \times 740 + 1410 \times 720 + 1420 \times 720 + 1275 \times 740) \times 50 \quad \text{(E.2)}$$

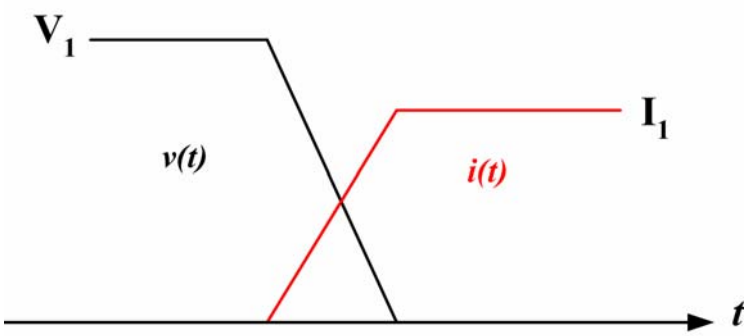


Figure E.2. Typical voltage and current waveforms of fully controllable power semiconductor during device turn-on in PSCAD/EMTDC (not-to-scale)

Table E.2 Turn-on energy loss of power semiconductors at T_{vj}=125°C for the corresponding switching conditions, given in their datasheets

	IGCT 5SHY35L4510	IGBT CM1200HC-66H	SGCT GCU15CA-130
E_{on}	1.5J	1.1J	0.42J
V_0	2800V	1650V	3000V
I_0	4000A	750A	800A

Table E.3 Voltage and current of fully controllable power semiconductor during device turn-on (obtained from Fig.3.7)

	Current Pulse 1	Current Pulse 2	Current Pulse 3	Current Pulse 4
V_1	1230V	1410V	1420V	1275V
I_1	740A	720A	720A	740A

E.3. Turn-Off Loss

Turn-off loss occurs during forced turn-off of fully controllable power semiconductor as explained in Chapter 2. Turn-off energy (E_{off}) is calculated at each forced turn-off of power semiconductor. The instants at which power semiconductor undergoes forced turn-off are defined by encircled C in Fig.4.1 and 4.2. For this purpose, the magnitude of voltage (V_2) across the power semiconductor after forced turn-off and the magnitude of current (I_2) through the power semiconductor just before forced turn-off are determined from the simulation results for forced turn-off instants as illustrated in Fig.E.3. In datasheets, the value of E_{off} is also given for certain switching conditions, such as V_0, I_0 and T_{vj}. Typical values of E_{off} for different power semiconductors can be found their datasheets as given in Table E.4. From simulations results in Fig.3.7, the values of V_2 and I_2 are given in Table E.5 according to the current pulse in Fig.3.7. Then, using the values of E_{off} in Table E.4 and V_2, I_2 in Table E.5, turn-off loss of fully controllable power semiconductors are calculated as in (E.3).

$$P_{turn-off} = \frac{E_{off}}{V_0 I_0} \times (800 \times 740 + 450 \times 760 + 60 \times 750 + 0 \times 730 + 400 \times 760 + 760 \times 750) \times 50 \quad \text{(E.3)}$$

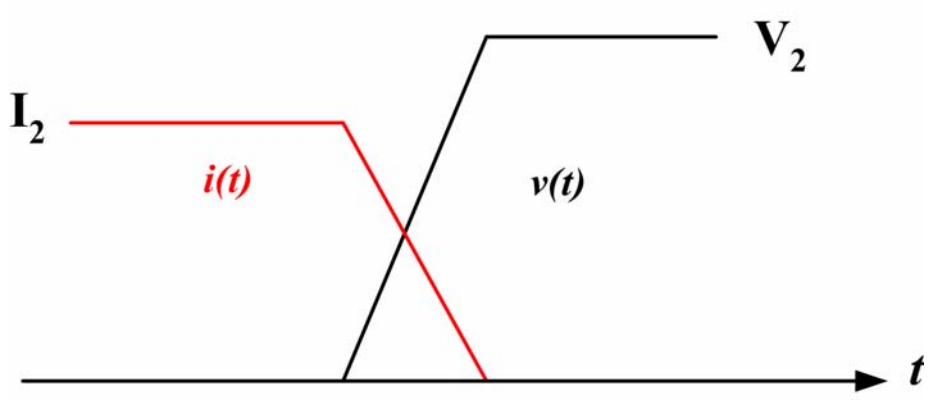


Figure E.3 Typical voltage and current waveforms of fully controllable power semiconductor during forced turn-off in PSCAD/EMTDC (not-to-scale)

Table E.4 Turn-off energy loss of power semiconductors at T_{vj}=125°C for the corresponding switching conditions, given in their datasheets

	IGCT 5SHY35L4510	IGBT CM1200HC-66H	SGCT GCU15CA-130
E_{off}	4J	1.2J	4.5J
V_0	2800V	1650V	3000V
I_0	750A	750A	750A

Table E.5 Voltage and current of fully controllable power semiconductor during device turn-on (obtained from Fig.3.7)

	Current Pulse 1	Current Pulse 2	Current Pulse 3	Current Pulse 8	Current Pulse 9	Current Pulse 10
V_2	800V	450V	60V	0V	400V	760V
I_2	740A	760A	750A	730A	760A	750A

E.4. Reverse Recovery Loss

Reverse recovery loss belongs to either fast recovery diode or diode part of symmetric power semiconductor. It occurs during reverse recovery phase in load commutation as explained in Chapter 2. Reverse recovery energy (E_{rec}) is calculated at each load turn-off of diode. The instants of load turn-off are defined by encircled D in Fig.4.1 and 4.2. For this purpose, the magnitude of voltage (V_3) across the power semiconductor during reverse-recovery and the magnitude of current (I_3) through the power semiconductor just before load turn-off are determined from the simulation results for load turn-off instants as illustrated in Fig.E.4. In datasheets, the value of E_{rec} is also given for switching conditions, such as V_0, I_0, -di/dt and T_{vj}. Typical values of E_{rec} for different power semiconductors can be found from their datasheets as given in Table E.6. The value of –di/dt is determined by the companion fully controllable power semiconductor. From simulations results in Fig.3.7, the values of V_3 and I_3 are given in Table E.7 according to the current pulse

in Fig.3.7. Then, using the values of E_{off} in Table E.6 and V_3, I_3 in Table E.7, reverse recovery loss of diodes or symmetric power semiconductors are calculated as in (E.4).

$$P_{rec} = \frac{E_{rec}}{V_0 I_0} \times (1225 \times 720 + 1400 \times 690 + 1425 \times 690 + 1260 \times 715) \times 50 \qquad \text{(E.4)}$$

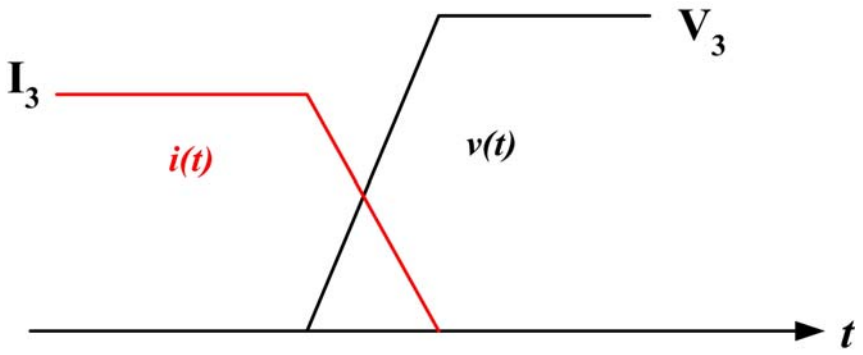


Figure E.4 Typical voltage and current waveforms of fully controllable power semiconductor during load turn-off in PSCAD/EMTDC (not-to-scale)

Table E.6 Reverse recovery energy loss of power semiconductors at T_{vj}=125°C for the corresponding switching conditions, given in their datasheets

	Diode D911SH45	Diode RM1200HA-66S	SGCT GCU15CA-130
E_{off}	2.5J	0.45J	2.8J
V_0	2800V	1650V	3000V
I_0	750A	750A	750A

Table E.7 Voltage and current of fully controllable power semiconductor during load turn-off (obtained from Fig.3.7)

	Current Pulse 4	Current Pulse 5	Current Pulse 6	Current Pulse 7
V_3	1225V	1400V	1425V	1260V
I_3	720A	690A	690A	715A

APPENDIX F

SIMULATION MODELS FOR ANALYSIS OF TURN-OFF SNUBBER IN MATLAB/SIMULINK

F.1 Simulation Model For Forced Turn-off of IGCT

This model is for turn-off snubber of S1 in Fig.3.37. There are two phase during forced turn-off of IGCT and these phases occur consecuently. These phases can also be observed from theoretical waveforms in Fig.2.35, where they are indicated as ① and ②. In phase ①, S3 is in off state untill v_3 becomes 0. When v_3 becomes 0, phase ② starts. In phase ②, S3 is conducting and v_3=0.

The model used in MATLAB/Simulink is as given in Fig.F.1. Inside the block "state-space", the state space representation of phase ① in (F.1), which is obtained from (3.17) is written. From the outputs of "state space" block, "Subsystem1" calculates v_3.. If it is less than zero, "mode" is -1, otherwise it is 1. "Subsystem2" calculates v_1 for phase ①. The details of "Subsystem1" and "Subsystem2" are shown Fig.F.2.

$$\frac{d}{dt}\begin{bmatrix} i_1' \\ v_{C1} \\ v_{C3}' \end{bmatrix} = \begin{bmatrix} \frac{-2R}{L_1+2L} & \frac{-1}{L_1+2L} & \frac{1}{L_1+2L} \\ \frac{1}{C} & 0 & 0 \\ 0 & 0 & \frac{1}{C} \end{bmatrix}\begin{bmatrix} i_1' \\ v_{C1} \\ v_{C3}' \end{bmatrix} + \begin{bmatrix} \frac{R}{L_1+2L} & \frac{L}{L_1+2L} & \frac{-R}{L_1+2L} & 0 \\ \frac{-1}{C} & 0 & \frac{1}{C} & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{S1} \\ \frac{di_{S1}}{dt} \\ I_{dc} \\ V_{dc} \end{bmatrix} \qquad \text{(F.1)}$$

$$y = \begin{bmatrix} R & 1 & 0 \\ 1 & 0 & 0 \\ R & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}\begin{bmatrix} i_1' \\ v_{C1} \\ v_{C3}' \end{bmatrix} + \begin{bmatrix} -R & -L & R & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{S1} \\ \frac{di_{S1}}{dt} \\ I_{dc} \\ V_{dc} \end{bmatrix}$$

In "state space1" block, the state-space representation of phase ② in (F.2) is written. During phase ①, "mode" is -1 and all the inputs for the "state space" block is zero. When the phase ① ends, "mode" becomes 1 and instantaneous values of i_1

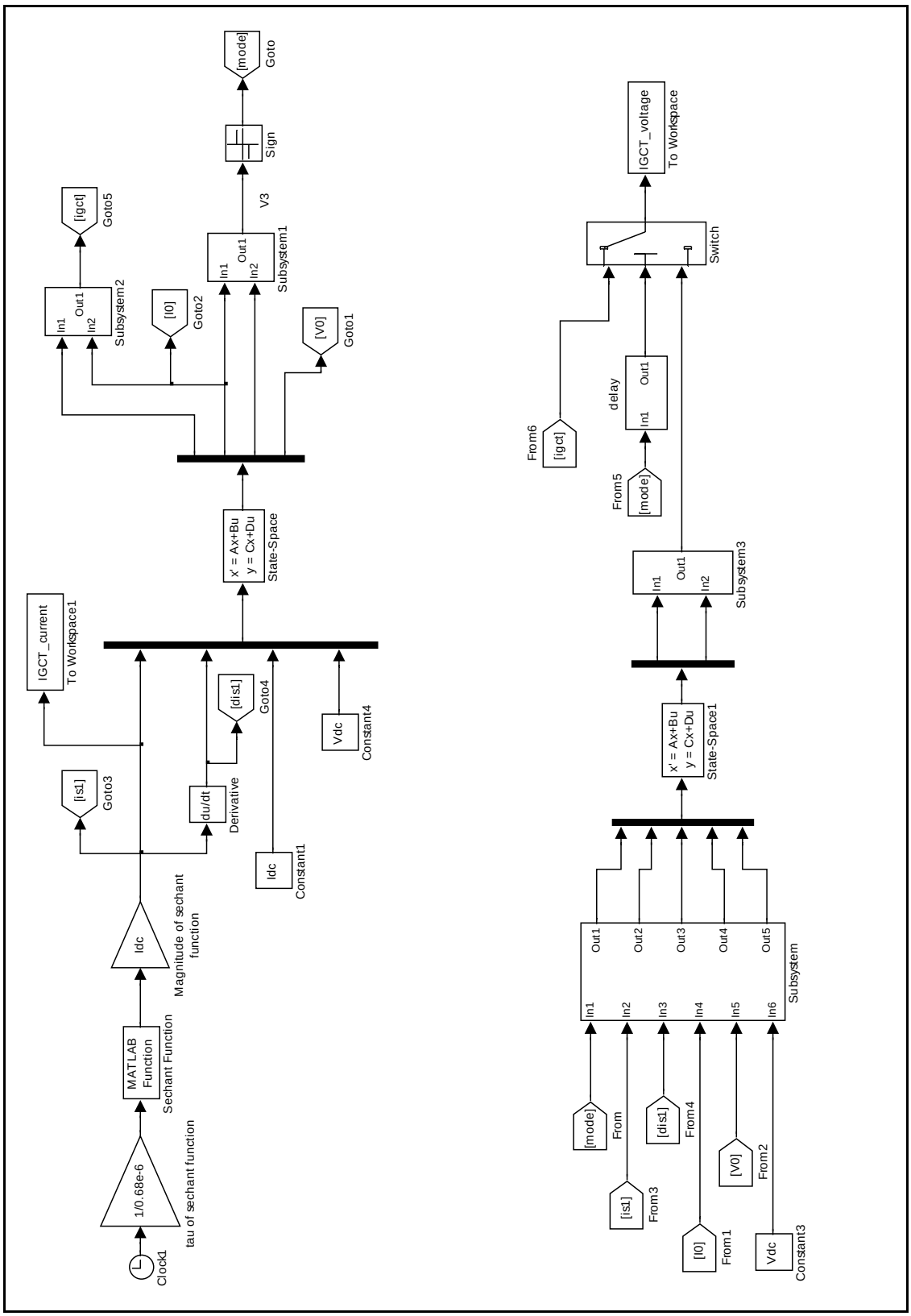
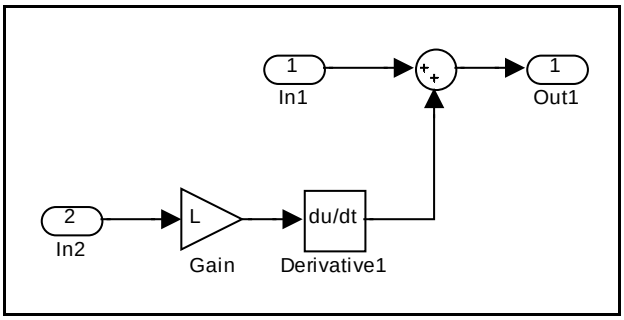


Figure F.1 Simulation model of forced turn-off for IGCT in MATLAB/Simulink

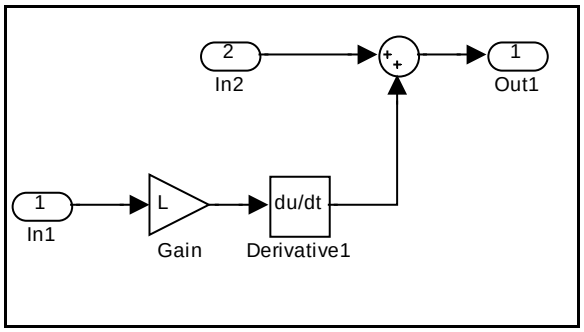
and v_{C1} are taken as snapshot as the initial value (I_0 and V_0) for "state space1". After then, with the use of switches in "Subsystem", S1 current and its derivative are then fed to "state space1". The details of "Subsystem" is shown in Fig.F.3a. "Subsystem3" calculates v_1 during phase ②. Its details are shown in Fig.F.3b. "Switch" combines the waveforms of IGCT (v_1) in phases ① and ②.

$$\frac{d}{dt}\begin{bmatrix} i_1 \\ v_1 \end{bmatrix} = \begin{bmatrix} \frac{-R}{L+L_1} & \frac{-1}{L+L_1} \\ \frac{1}{C} & 0 \end{bmatrix}\begin{bmatrix} i_1 \\ v_1 \end{bmatrix} + \begin{bmatrix} \frac{R}{L+L_1} & \frac{L}{L+L_1} & \frac{-R}{L+L_1} & \frac{-1}{L+L_1} & \frac{1}{L+L_1} \\ \frac{-1}{C} & 0 & \frac{1}{C} & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{S1} \\ \frac{di_{S1}}{dt} \\ I_0 \\ V_0 \\ V_{dc} \end{bmatrix} \quad \text{(F.2)}$$

$$y = \begin{bmatrix} 1 & 0 \\ R & 1 \end{bmatrix}\begin{bmatrix} i_1 \\ v_1 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ -R & -L & R & 1 & 0 \end{bmatrix}\begin{bmatrix} i_{S1} \\ \frac{di_{S1}}{dt} \\ I_0 \\ V_0 \\ V_{dc} \end{bmatrix}$$

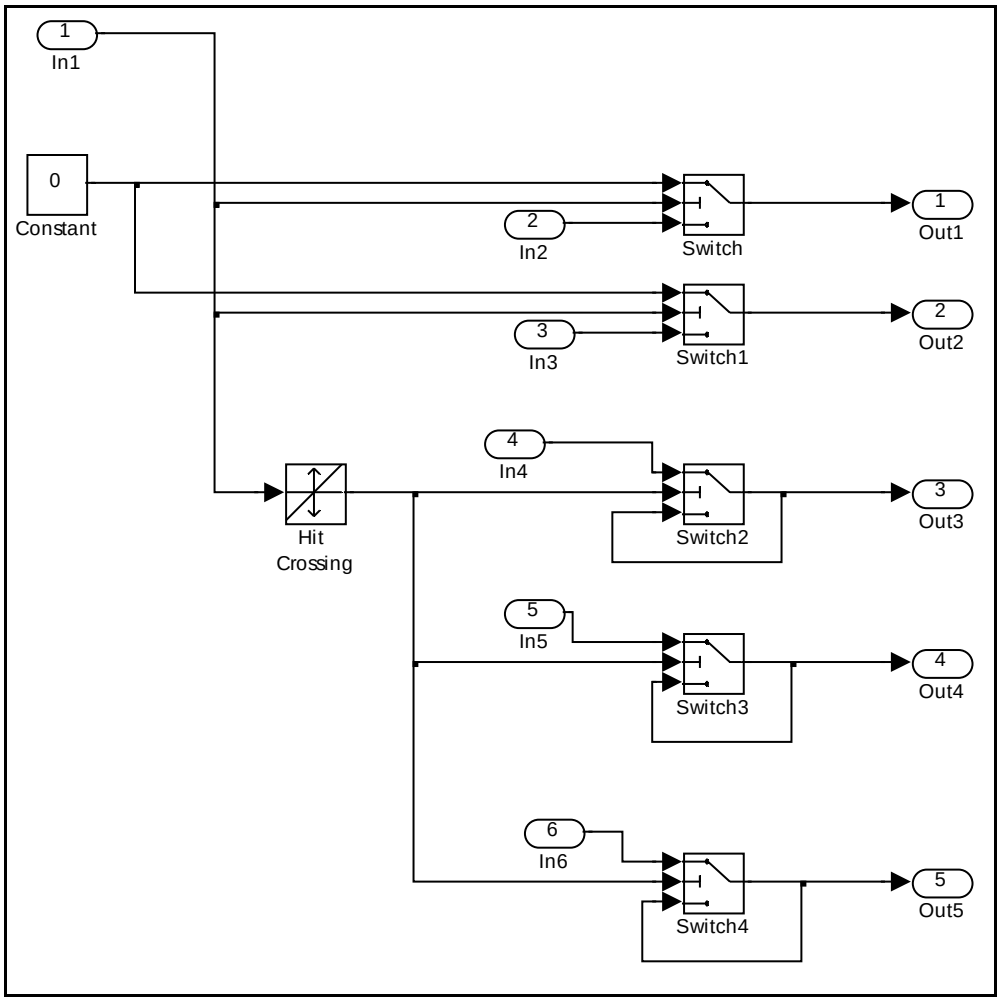


(a) Subsystem2

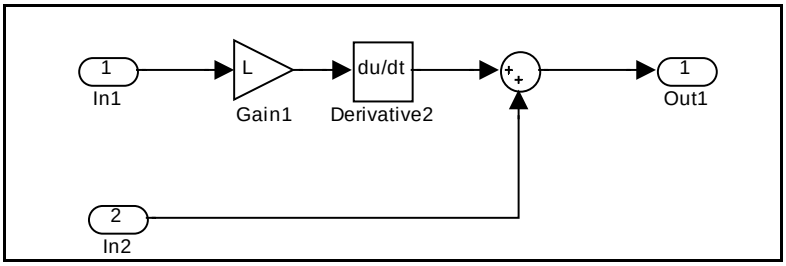


(b) Subsystem1

Figure F.2 Details of "Subsystem2" and "Subsystem1" in simulation model of turn-off snubber for IGCT forced turn-off



(a) Subsystem



(b) Subsystem3

Figure F.3 Details of “Subsystem ” and “Subsystem3” in simulation model of turn-off snubber for IGCT forced turn-off

F.2 Simulation Model for Load Turn-off of Diode

This model is for turn-off snubber of S3 in Fig.3.37. Unlike forced turn-off of IGCT, there is only one phase during load turn-off of diode. This phase can also be observed from theoretical waveforms in Fig.2.36, where it is indicated as ③. In this phase, S1 is conducting and S3 is under load turn-off.

The model used in MATLAB/Simulink is as given in Fig.F.4. In block "state-space", the state space representation in (F.3) which is obtained from (3.18) is written.

$$\frac{d}{dt}\begin{bmatrix} i_3 \\ v_{C3} \end{bmatrix} = \begin{bmatrix} \dfrac{-R}{L+L_1} & \dfrac{-1}{L+L_1} \\ \dfrac{1}{C} & 0 \end{bmatrix}\begin{bmatrix} i_3 \\ v_{C3} \end{bmatrix} + \begin{bmatrix} \dfrac{L_1}{L+L_1} & \dfrac{1}{L+L_1} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} \dfrac{di_{S3}}{dt} \\ V_{dc} \end{bmatrix} \qquad \text{(F.3)}$$

$$y = \begin{bmatrix} 1 & 0 \\ R & 1 \end{bmatrix}\begin{bmatrix} i_3 \\ v_{C3} \end{bmatrix}$$

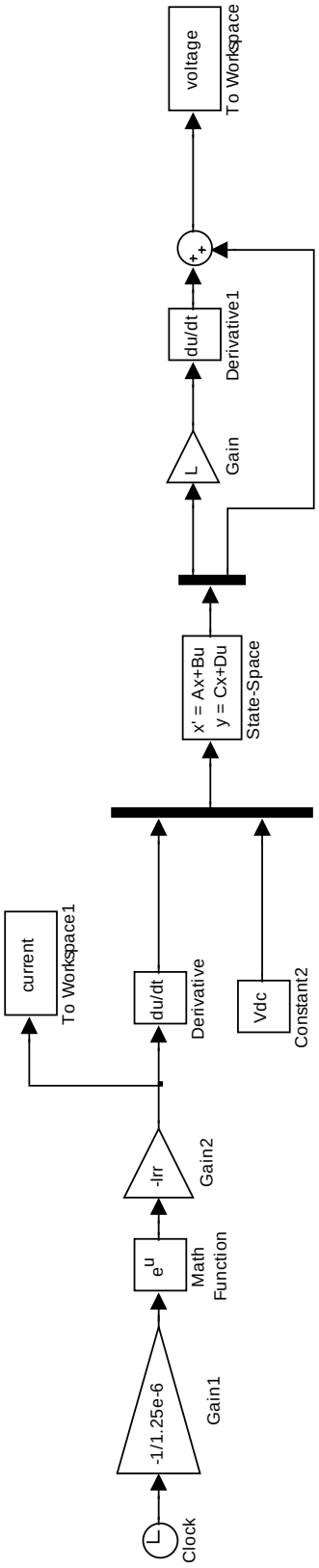


Figure F.4 Simulation model of load turn-off for diode in MATLAB/Simulink

APPENDIX G

FLOW CHART OF IMPLEMENTED REACTIVE POWER CONTROL SYSTEM

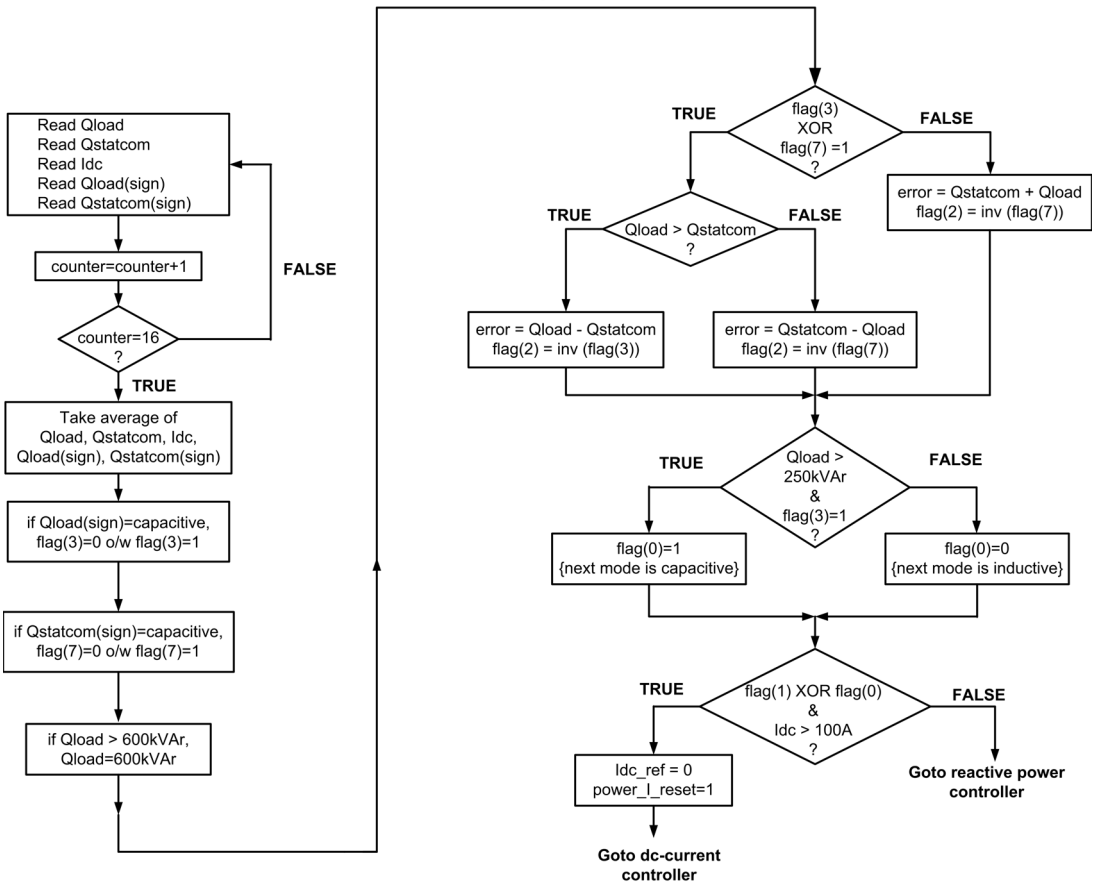


Figure G.1 Flowchart for root of the reactive power control system

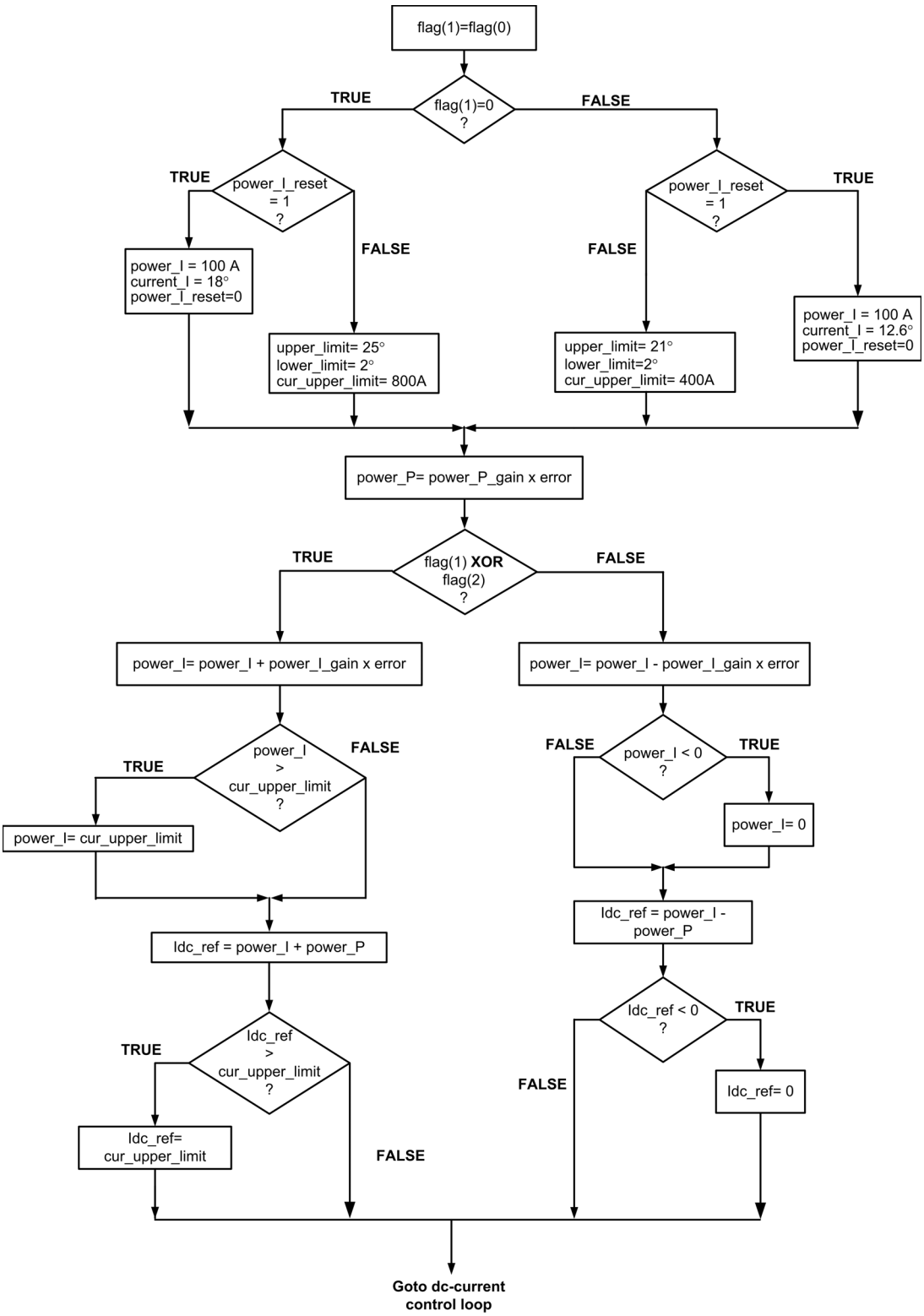


Figure G.2 Flowchart of the reactive power controller

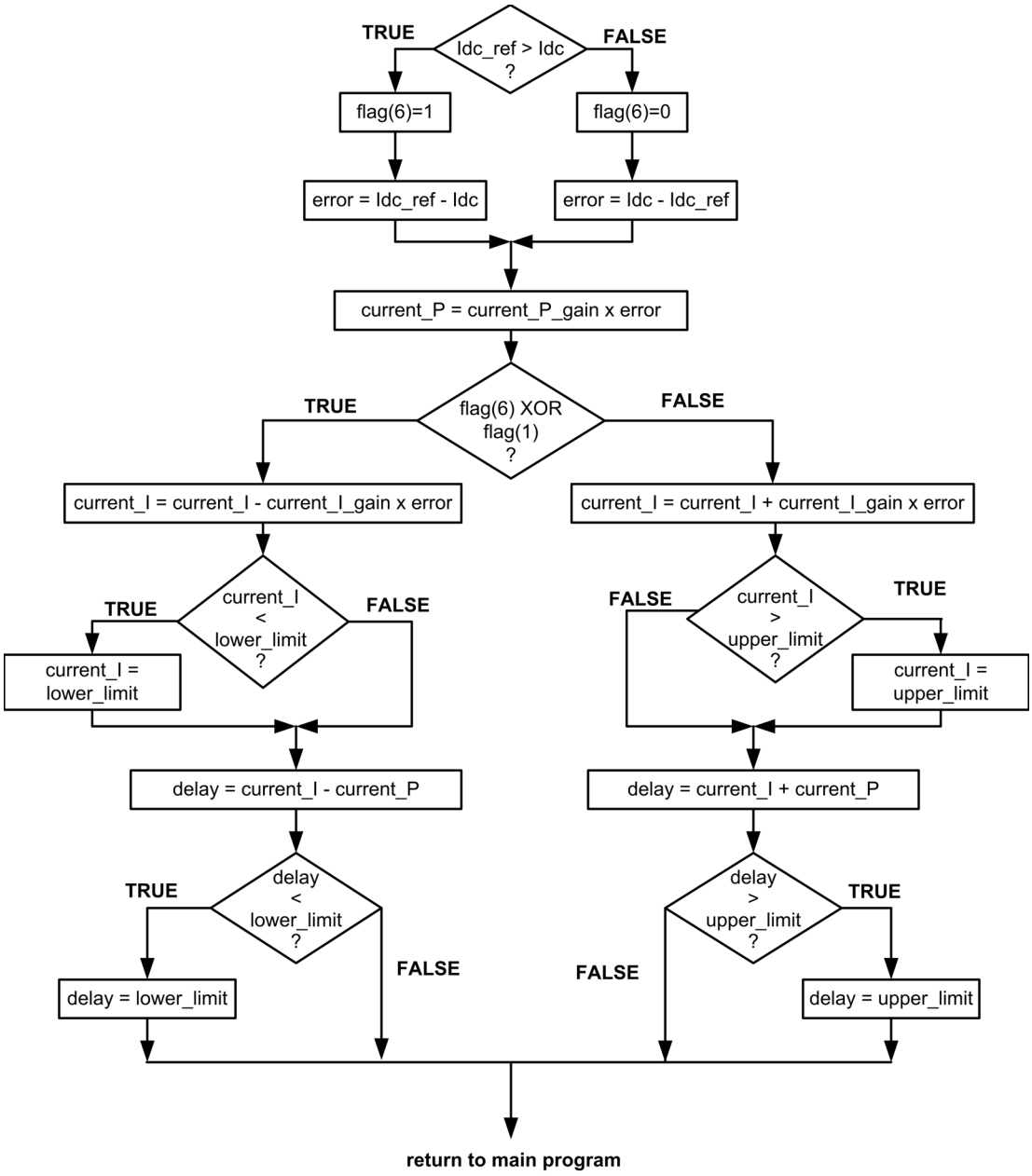


Figure G.3 Flowchart of the reactive dc-current controller

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PUBLICATIONS

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