CASCADED, REACTIVELY TERMINATED, SINGLE STAGE DISTRIBUTED 2-18 GHZ AMPLIFIER

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CASCADED, REACTIVELY TERMINATED, SINGLE STAGE DISTRIBUTED 2-18 GHZ AMPLIFIER

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ABSTRACT

CASCADED, REACTIVELY TERMINATED, SINGLE STAGE DISTRIBUTED 2-18 GHZ AMPLIFIER

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M.S., Department of Electrical and Electronics Engineering

Supervisor : Assoc. Prof. Dr. Şimşek DEMİR

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In this thesis work, a 3-stage ultra broadband amplifier operating in 2-18 GHz frequency band with gain 23 $\pm$ 1.5 dB is designed, simulated and fabricated. The amplifier is based on cascaded, reactively terminated single stage distributed amplifier (CRTSSDA) concept. The idea of including reactive terminations to achieve ultra broadband gain is investigated and simulated. The simulated design is fabricated and measurements of the fabricated amplifier are compared with simulation results. Also practical experience on working at high frequencies with surface mount components is presented in this thesis work.

Keywords: Broadband Amplifier, Distributed Amplifier, CRTSSDA, Reactive Termination

ÖZ

SERİ BAĞLI, REAKTİF SONLANDIRILAN TEK AŞAMADA DAĞITILMIŞ
2–18 GHZ YÜKSELTEÇ TASARIMI

EFE, Oğuzhan
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Temmuz 2008, 76 sayfa

Bu tez çalışmasında, 2–18 GHz bandında $23 \pm 1{,}5$ dB kazançlı 3 aşamalı çok geniş bant yükselteç tasarımı, benzetimleri ve üretimi yapılmıştır. Tasarlanan yükselteç, seri bağlı, reaktif sonlandırılan, tek aşamada dağıtılmış (SRSTADY) devre tasarımı tekniği kullanılarak tasarlanmıştır. Benzetim sonucu elde edilen tasarım gerçeklenmiştir. Gerçeklenen yükselteçte alınan ölçümler benzetim sonuçlarıyla kıyaslanmıştır. Ayrıca, bu tez çalışmasında yüksek frekanslarda yüzeye monte edilen elemanlarla çalışırken elde edilen pratik tecrübeler sunulmuştur.

Anahtar Kelimeler: Çok Geniş Bant Yükselteç, Dağıtılmış Yükselteç, SRSTADY, Reaktif Sonlandırma

To my fiancée Canan

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LIST OF ABBREVIATIONS

ADS	: Advanced Design System
CRTSSDA	: Cascaded, Reactively Terminated, Single Stage Distributed Amplifier
DPHEMT	: Double-Heterojunction Pseudomorphic High-Electron-Mobility Transistor
FET	: Field Effect Transistor
MESFET	: Metal-Semiconductor Field Effect Transistor
MMIC	: Monolithic Microwave Integrated Circuit
PHEMT	: Pseudomorphic High-Electron-Mobility Transistor
TWA	: Traveling Wave Amplifier
TWDA	: Traveling Wave Distributed Amplifier
VSWR	: Voltage Standing Wave Ratio

CHAPTER 1

INTRODUCTION

1.1 Microwave Amplifiers

Researches on amplifiers date back to A. G. Clavier [1] who established a radio link between England and France in 1931. His successful experiment motivated researches on amplifiers from 1930s to nowadays. Because of shortage of technology of that time, implemented amplifiers were narrow banded. Invention of distributed amplifier concept presented a new viewpoint to engineers and shed light on the design of wide band amplifiers. Invention of junction bipolar transistors, than FETs and MESFETs accelerated the researches on broadband amplifiers.

Today, microwave amplifiers are used in various fields of microwave engineering such as in electronic warfare systems, radars, satellite communications, optical communications, networks and instrumentation. An amplifier is used to amplify received signals from an antenna in order to be able to process it, to amplify a signal that is going to be transmitted from an antenna in a radar system or to maintain a robust communication with a satellite or in a network. In conclusion, amplifiers are one of the necessary components in microwave systems.

In order to meet today's technological requirements, researches are focused on widening the gain bandwidth of an amplifier. Several circuit techniques are developed to have stable, high gain and efficient broadband amplifiers. These amplifiers are realized in hybrid or monolithic forms which have advantages or disadvantages on each other for different constraints. For example, high output power and noise figure are always in a trade-off for a designer, or linearity is an expense of efficiency. The best design method should be chosen according to the requirements.

Concept of distributed amplifiers is one of the circuit techniques developed to widen operating frequency band. The amplifier designed in this thesis work is based on distributed amplifier concept. In order to have an insight of distributed amplifiers, the following section is given.

1.2 Distributed Amplifiers

The concept of distributed amplifiers dates back to the 1940s [2]. W. S. Percival [3] found that bandwidth of an amplifier is determined by the capacitance and transconductance of the conventional electronic valve. He separated capacitance of the valve from its transconductance and absorbed the separated capacitance into artificial transmission lines. Now the gain bandwidth of the valve is limited to the cut-off frequency of those artificial lines. Separating capacitance and absorbing it into artificial transmission lines is the first insight of distributed amplifiers.

Switching from electronic tube valve technology to junction bipolar transistors increased researches on distributed amplifiers. Publications about distributed amplifiers appeared on television broadcasting, radar and networking areas [4]. Between 1970 and 1980 GaAs FET and MESFET researches gave additional acceleration on distributed amplifiers [5-6]. Afterwards, the development of monolithic microwave integrated circuit technology (MMIC) improved the researches on distributed amplifiers.

Distributed amplifiers are advantageous because of eliminating the gain bandwidth limiting effect of transistor's gate and drain line capacitances. They give successful gain, matching and noise figure over a wide bandwidth. These attributes of distributed amplifier are used for the proposed amplifier of this thesis work, together with cascading transistors and including reactive terminations.

1.3 Cascaded, Reactively Terminated, Single Stage Distributed Amplifier

Conventional traveling wave amplifiers (TWA) are used for broadband amplification since the last 2 decades. Ayasli, et al. [7] presented a TWA which operates in 2-20 GHz band. Attenuation at gate and drain lines and mismatches in phase velocities of the successive stages in a TWA structure makes it difficult to obtain high gain in broad bandwidth. In order to overcome these deficiencies, cascaded, reactively terminated single stage distributed amplifier concept is developed.

A cascaded, reactively terminated, single stage amplifier (CRTSSDA) is firstly presented by Virdee [8]. Bandwidth of distributed amplifiers is limited to the cut-off frequencies of the artificial transmission lines, which are realized by inductors. In order to improve the bandwidth of the amplifier, which is limited to the cut-off frequencies of artificial lines, reactive terminations are included at the input of each stage of a CRTSSDA. Together with selecting resonance-free values for biasing components, reactive terminations provide broadband matching and gain flattening.

It is stated in [8] that a CRTSSDA exhibits a substantial gain and superior efficiency compared to a conventional traveling wave amplifier (TWA). A three-stage TWA can give 8-9 dB gain maximum, however Virdee [8] achieved more than 20 dB gain in 2-18 GHz frequency band with a three-stage CRTSSDA. Another advantage of CRTSSDA is that it is easier to design than designing a conventional TWA since there is no need for phase velocity equalization of gate and drain lines.

DPHEMT transistors are used in Virdee's [8] ultra broadband amplifier. The amplifier proposed in [8] is realized on alumina substrate which has a permittivity ε_r = 9.8 and height of 0.381 mm. In this thesis work, the designed amplifiers are fabricated on Rogers4350 and Rogers4003 substrates, having permittivities ε_r = 3.48 and ε_r = 3.38 respectively. DPHEMT transistors are used in the proposed amplifiers as in Virdee's work.

1.4 Description of the Thesis

In this thesis work, a 3-stage ultra broadband amplifier in 2-18 GHz frequency band, having gain of 23 $\pm$ 1.5 dB is designed, simulated and fabricated. The proposed amplifier is a cascaded, reactively terminated, single stage distributed amplifier (CRTSSDA). Two different amplifiers with the same topology are designed and presented in this thesis work. The first trial of the CRTSSDA is realized on Rogers4350 substrate. Having tunings and observations on the firstly fabricated amplifier inspirited a second design of CRTSSDA to achieve a better gain flatness and input and output match. The secondly designed ultra broadband amplifier is fabricated of Rogers4003 substrate. The theory of designing a broadband amplifier, simulations, analysis and measurements of the proposed amplifiers are given within this thesis study in detail in the next chapters. Experience gained during fabrication and measurements are also noted and comparisons between simulation results and measurements are presented.

1.5 Outline of the Thesis

This thesis is organized as follows: In Chapter 2, brief theoretical knowledge about designing broadband amplifiers is given. Comparisons between the circuit techniques are presented and an introduction to CRTSSDA topology is given.

In Chapter 3, designing a CRTSSDA is given step by step together with the designed amplifiers. Simulations regarding the theory of reactive terminations of a CRTSSDA and results of the designed amplifiers are also presented in Chapter 3.

In Chapter 4, fabrication and measurement techniques are given. Simulation results are compared to the measurements in this chapter. Experience about using surface mount components at high frequencies are also explained in this chapter.

Finally, conclusions about design and fabrication of an ultra broadband CRTSSDA are made in Chapter 5.

CHAPTER 2

BROADBAND AMPLIFIERS

Development in the fields of instrumentation, electronic warfare, optical communication and microwave motivated studies in multi octave amplifiers [4]. These researches resulted several circuit techniques to achieve broadband amplifiers. These different methods of designing broadband amplifiers have advantages and disadvantages compared to each other. Brief description about these topologies and comparisons between them are presented in this chapter.

2.1 Review of Broadband Amplifiers

Broadband amplifiers' power-added efficiencies are usually lower than narrowband amplifiers. There is a trade-off between achieving multi octave gain and efficiency. Broadband amplifiers' power-added efficiencies are generally in the range of 8% to19% [4]. High power-added efficiency is one of the strict requirements of broadband amplifiers. The other requirements for broadband amplifiers are high stability, high gain and acceptable output power. In order to meet these requirements several circuit techniques are developed.

Some of the circuit techniques developed for designing broadband amplifiers can be listed as follows [4]:

- Feedback circuit
- Reactively matched circuit
- Traveling wave distributed circuit
- Cascaded, reactively terminated single stage distributed circuit

Brief description about the circuit techniques listed above is given in the following sections. More emphasis is employed on traveling distributed amplifier (TWA) and cascaded, reactively terminated single stage distributed amplifier (CRTSSDA) circuits.

2.1.1 Feedback Amplifiers

In a feedback amplifier, shown in Figure 2.1 [4], broadband is achieved by a feedback path, comprising R_{fb}, L_{fb} and C_{fb}. The capacitor C_{fb} blocks the DC biasing of gate and drain lines, which should be resonant free in band with biasing inductors, L_1 and L_2. The inductor in the feedback path, L_{fb}, cuts the feedback path for high frequencies to adjust gain flatness and R_{fb} determines the gain and bandwidth of the amplifier. L_g and L_d are used to compensate intrinsic gate and drain capacitance respectively to achieve broadband gain.

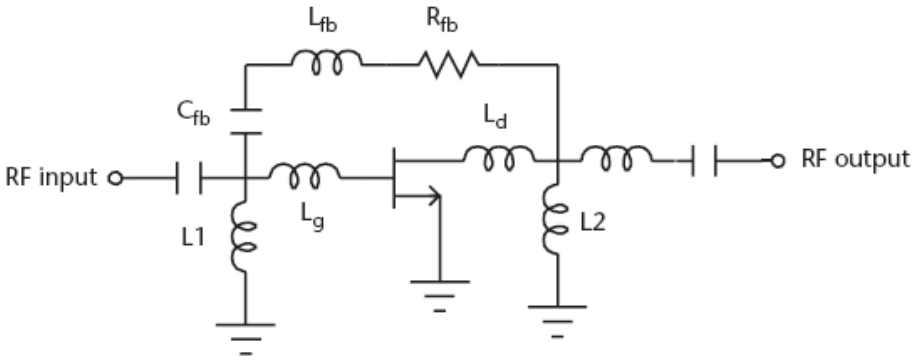

Figure 2.1 Feedback Amplifier [4]

Niclas, et al. [9] proposed a feedback amplifier that achieves multi octave band with one active device. Niclas achieved broadband gain by adjusting L_g, L_d and L_{fb} in Figure 2.1 [9].

Feedback amplifier circuit is not a complex configuration compared to traveling wave amplifier and CRTSSDA. Feedback amplifiers have good input and output

matching over a multi octave band. They also have excellent unconditional stability and a flat gain in broadband.

Disadvantages of feedback amplifiers are that they have very high noise figures because of including a resistor in the feedback path. They are also very sensitive to frequency, therefore realizing a feedback amplifier in a hybrid circuit is difficult to achieve. Feedback amplifiers are usually realized in MMIC circuits.

2.1.2 Reactively Matched Amplifiers

As the name implies, reactively matched amplifiers consist of input and output matching circuits which are composed of reactive components as shown in Figure 2.2 Reactively Matched Amplifier [4]. Input matching circuit provides a high gain and output matching circuit provides maximum output power which enhances power-added efficiency.

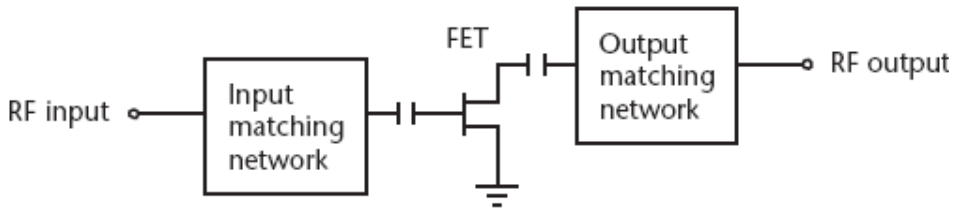

Figure 2.2 Reactively Matched Amplifier [4]

Tserng, et al. [10] presented a reactively matched amplifier operating in 2-18 GHz frequency band. The output power of Tserng's reactively matched amplifier is 23 dBm with efficiency 15%. Tserng used wideband impedance transformers to maintain input and output match; however, voltage standing wave ratio (VSWR) was poor in the band.

Palmer, et al. [11], realized the first reactively matched amplifier in MMIC circuit technology. Palmer's amplifier is operating in 6-18 GHz band, with output power of 27 dBm and efficiency of 19%. The amplifier is a two stage amplifier with driver

circuits at input and output, where he paralleled the active devices to decrease source inductance.

Multi octave matching of this type of broadband amplifier is not an easy task since the reactive matching circuits are dependent on frequency. One can design a matching circuit for a moderate band of frequencies; however, the performance of the matching circuit degrades with increasing bandwidth. Several methods are developed for improving broadband performance [10-11]; however, these methods increase the cost and size of the amplifier.

2.1.3 Traveling Wave Distributed Amplifiers

In a traveling wave distributed amplifier (TWDA), gate and drain capacitances are absorbed in artificial transmission lines by lumped inductors. The conventional schematic of a TWDA is given in Figure 2.3 [4].

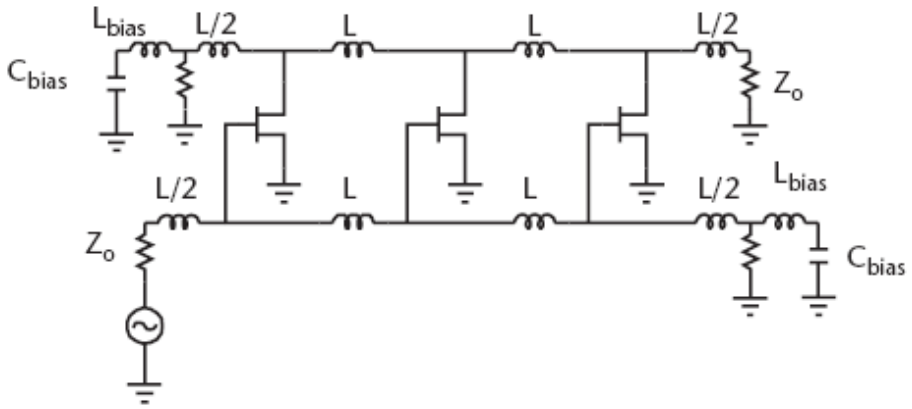

Figure 2.3 Traveling Wave Distributed Amplifier [4]

Each transistor is excited at their gates and transistors conduct the input signal to their drain ports through their transconductance. The amplified signals from each transistor are added in forward direction to the output. Equalizing phase velocities is the vital point in designing TWDA, since any mismatch of phase velocities will degrade the amount of signal transmitted to load. The reverse directed traveling

waves are absorbed in drain lines which are terminated to characteristic impedance by the inclusion of artificial transmission lines.

Since the artificial transmission lines are terminated with the characteristic impedance, a constant resistance at the input and output is observed. Constant input and output impedance provides a broadband matching. Cut-off frequency of the artificial line determines the highest operating frequency of the amplifier, which depends on the capacitance of the active devices and lumped inductors of the artificial line.

Gain expression of a TWDA is given by [12]:

$$G_{TWDA} = \frac{1}{4} g_m n^2 Z_0{}^2 \qquad \textbf{(2-1)}$$

where g_m is the transconductance of the transistors, n is the number of active components used and Z_0 is the characteristic impedance of the artificial lines.

Since the given gain expression for TWDA is independent of frequency, it is possible to have multi octave response by this circuit technique. The only limiting factor is the cut-off frequency of artificial transmission lines, hence gate and drain capacitance and lumped inductors.

In a lossless system, one can get higher gain by simply increasing the number of stages. However, gate and drain line attenuations will limit the gain that one can get from traveling wave amplifiers.

Traveling wave distributed amplifiers exhibit good matching since the artificial transmission lines are terminated to characteristic impedance. The only limiting factor of bandwidth is the cut-off frequencies of the gate and drain lines of the transistors. This characteristic of TWDAs also allows designers to cascade gain modules to get higher gained amplifiers. Constant resistance through the wide band also rivets stability when cascading gain modules and decrease tendency to oscillations.

Since the gain of a TWDA is the addition of in-phase currents from drain lines of each transistor, it is essential to equate the phase velocities of the forward directed signals from each active component. Any mismatch of phase velocities will cause degradation in gain. Also, if there is a failure in one stage, this failure will affect the whole response of the amplifier. Attenuation in gate lines decreases the available output power from the amplifier when the number of stages is increased. These deficiencies are solved by CRTSSDA topology which is explained in the next section.

2.1.4 Cascaded, Reactively Terminated Single Stage Distributed Amplifier (CRTSSDA)

In cascaded, reactively terminated single stage distributed amplifier (CRTSSDA), the transistors are cascaded unlike the conventional traveling wave amplifier. Since CRTSSDA is also a distributed amplifier, gain and drain capacitances are absorbed into artificial transmission lines. The schematic of a CRTSSDA is given in Figure 2.4 [4].

Since the cut-off frequency of the artificial transmission lines limits the upper frequency of operation of the amplifier, reactive terminations are included in the topology as seen in Figure 2.4.

Transistors have 6 dB/octave gain roll off because of their intrinsic properties. To achieve broadband response, this roll off must be eliminated. If the cut-off frequencies of the artificial transmission lines are selected higher than the upper operating frequency, reactive terminations can be used to widen the band by removing gain roll off.

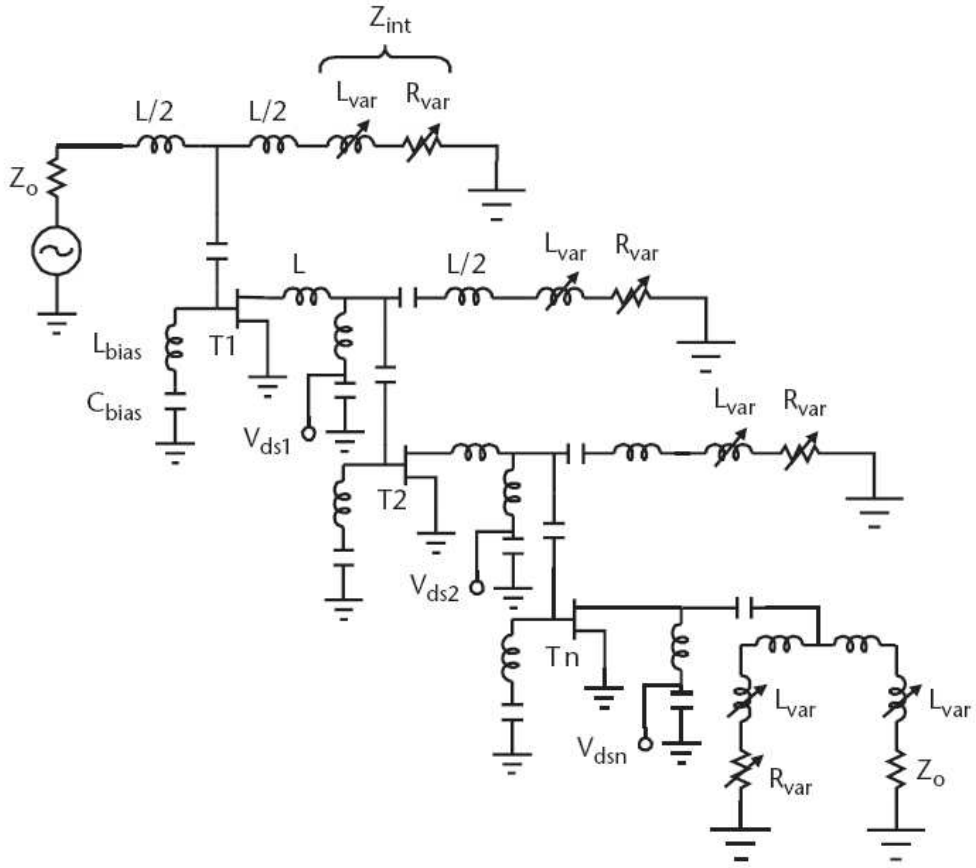

Figure 2.4 Cascaded Reactively Terminated Single Stage Distributed Amplifier [4]

Eliminating gain roll off is achieved by enhancing voltage swing at gate-to-source capacitance of each transistor. Resistors R_{var} and inductors L_{var} of Figure 2.4 form the reactive termination. Note that reactive terminations at gate terminals of each stage are responsible for voltage swing enhancement of the corresponding stage. Also, the reactive termination at the output helps for optimum match at the output for maximum power transfer to the load.

The impedance of reactive termination, labeled as Z_{int} in Figure 2.4 depends on frequency. Since the impedance of Z_{int} increases at higher frequencies because of the contribution of L_{var}, higher voltage will be coupled to the gate-to-source capacitance of the transistor. The coupled voltage than will be amplified through the transconductance of the active element and conducted to the next stage. After amplification through successive stages, a broadband gain is achieved at the output. Gain expression for an n-stage CRTSSDA is given as follows [4]:

$$G_{CRTSSDA} = \frac{1}{4} g_m{}^{2n} Z_{\text{int}}{}^{2(n-1)} Z_0{}^2 \quad \textbf{(2-2)}$$

where g_m is the transconductance of the transistor, Z_{int} is the impedance of the reactive termination and Z_0 is the characteristic impedance of the artificial transmission lines.

Gain of a CRTSSDA is an exponential function as seen from (2-2). This equation claims that the gain of a CRTSSDA is higher than the gain of TWDA given in (2-1) with equal number of stages.

Another advantage of CRTSSDA is that, it does not need any phase velocity equalization as in TWDA since the transistors are cascaded. The only constraint to achieve broadband is to design reactive terminations properly to adjust voltage swing at the gate of the stages. The number of stages is limited due to the gate and drain line attenuations in TWDA topology, however, there is not a limit for number of stages in CRTSSDA design.

Disadvantage of a CRTTSDA amplifier is that it is very sensitive to oscillation problems. Also biasing of each stage should be achieved individually and isolated from each other.

A 2-18 GHz broadband amplifier in CRTSSDA topology is designed and fabricated in this thesis study. Filtronic's FPD200, FPD6836 and FPD750 DPHEMT transistors are used in the design. Two trials of amplifiers are realized in Rogers4003 and Rogers4350 substrates and surface mount elements are used on fabrication. Details of the designed amplifiers are given in Chapter 3 where the fabrication and measurement sections are in Chapter 4.

CHAPTER 3

DESIGN OF THE BROADBAND AMPLIFIER

3.1 Introduction

Various design methods given in Chapter 2 are used to design broadband amplifiers recently. Among these circuit techniques, cascaded, reactively terminated, single stage distributed amplifier (CRTSSDA) design method [8] is used to design a 3-stage broadband amplifier, operating in 2-18 GHz band with gain 23 ± 1.5 dB.

In this chapter, principles of a CRTSSDA design are given in detail. Afterwards, the proposed amplifiers are explained with design steps. Simulations and their results regarding to the designed amplifiers are also given in this chapter.

3.2 Principles of CRTSSDA

In a CRTSSDA structure, the transistors that constitute the amplifier are cascaded as the name implies. Cascading transistors eliminates the need for equalizing phase velocities of the stages as in conventional traveling wave amplifiers (TWA). Theory of CRTSSDA is basically based on conveying the signal from preceding stage to next together with amplifying. In order to achieve broadband response, voltage swing enhancements are made on gate-to-source voltages by including reactive terminations at each stage. Necessary matching networks at input, output and between stages are also included in a CRTSSDA topology as the other types of broadband amplifiers have.

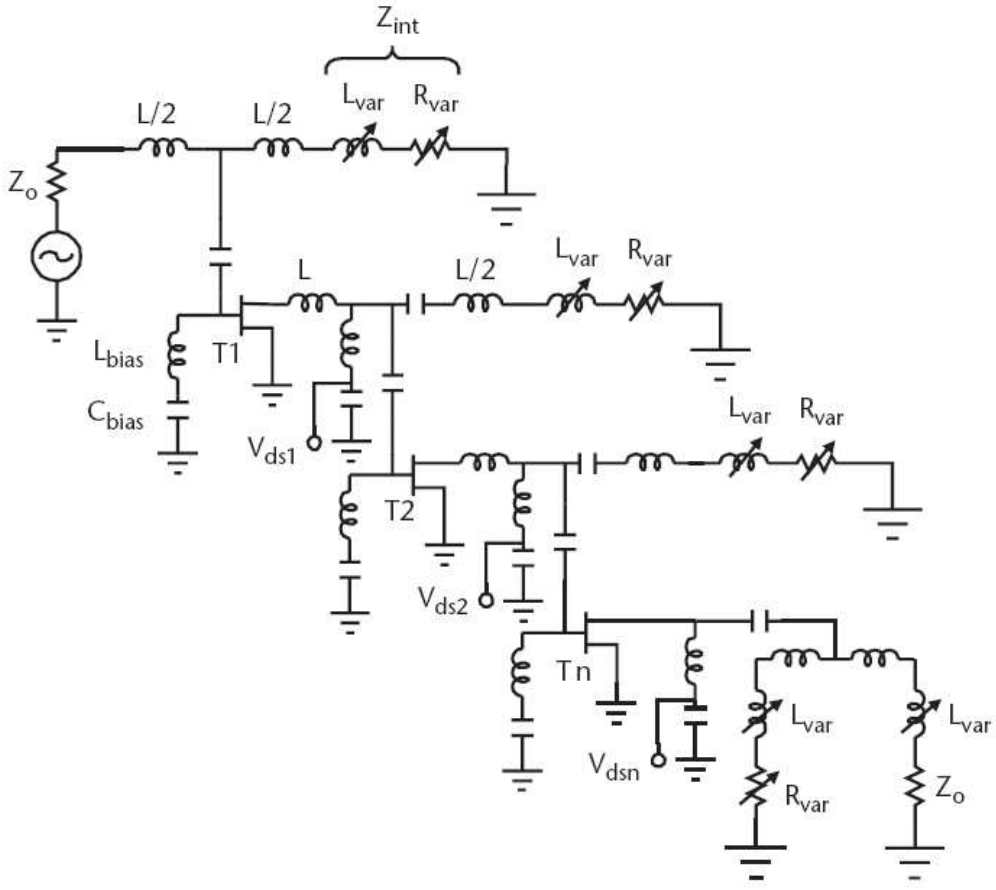

Figure 3.1 Block Diagram of a CRTSSDA [4]

Transistors have 6dB/octave gain roll off because of their intrinsic properties. The crucial point for a CRTSSDA design is to overcome the gain roll off of the transistors. For a 3-stage and 3 octaves amplifier, gain roll off totals 54dB decrease in gain at the upper operating frequency. In order to eliminate this roll off and get a flat gain across the band, reactive terminations are included in CRTSSDA design.

3.2.1 Theory of Reactive Terminations

Block diagram of a CRTSSDA given in Figure 2.4 is redrawn in Figure 3.1 for convenience. The components; resistor Rvar and inductor L_{var} in Figure 3.1 are the reactive terminations. The impedance of the reactive termination, $R_{var} + j\omega L_{var}$ is denoted as Z_{int} [8]:

$$Z_{\text{int}} = R_{\text{var}}(\omega) + j\omega L_{\text{var}}(\omega) \quad \textbf{(3-1)}$$

Reactive termination Z_{int} has higher values when the frequency increases as seen in (3-1) . This characteristic of reactive termination is used to adjust the voltage swing at the gate of transistors in a CRTSSDA. Having a frequency dependent voltage across the gate-to-source capacitance can be applied to compensate the intrinsic gain roll off. Analyzing a small signal model of a transistor with reactive termination helps to visualize the behavior of reactive termination. Figure 3.2 shows the small signal model of a single transistor with reactive terminations.

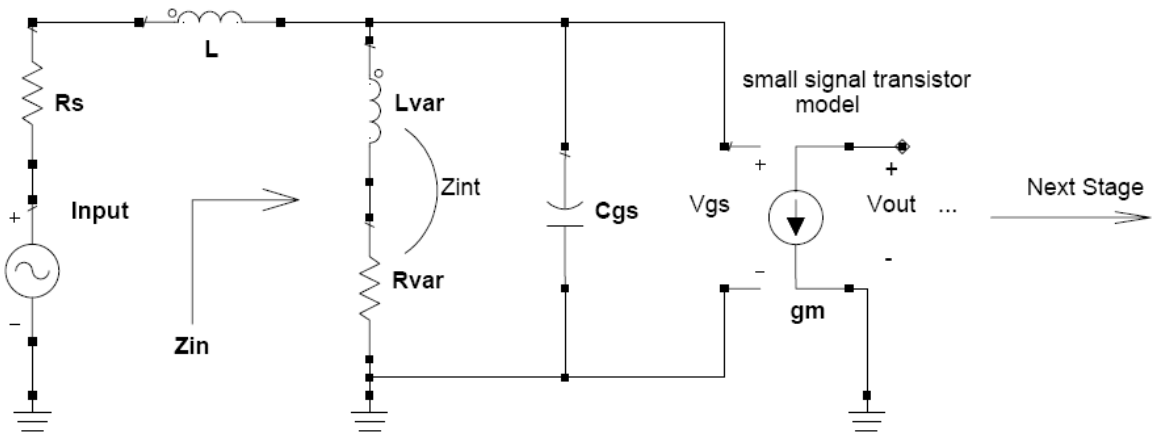

Figure 3.2 Small Signal Model of a Transistor with Reactive Terminations

The circuit given in Figure 3.2 shows the inclusion of reactive termination to enhance the voltage swing across gate-to-source capacitance C_{gs} for a single stage network. The transistor will amplify the voltage V_{gs} across C_{gs} by its transconductance g_m. Including reactive termination makes V_{gs} tend to be higher at higher frequencies than lower frequencies. It is suggested that, if the slope of V_{gs} is adjusted so as to equalize the roll off of the transistor, a flat gain will be achieved in broadband.

The output voltage $V_{out}(\omega)$ is given in (3-2). Transconductance, g_m, is assumed to be constant with frequency, therefore, manipulations on the gate voltage will be enough to have rigorous solutions.

$$V_{out}(\omega) = g_m \times V_{gs}(\omega) \quad \textbf{(3-2)}$$

Since reactive termination is the key point for a flat gain in broadband, its characteristics must be exposed clearly. From DC to 1 GHz, L_{var} has negligible effect on the value of Z_{int} whereas R_{var} is the dominant contributor. The impedance of the reactive termination Z_{int} in Figure 3.2 can be expressed as in (3-3) for frequencies ≤ 2 GHz.

$$Z_{\text{int}}(\omega) = R_{\text{var}} \quad \textbf{(3-3)}$$

On the other hand, the impedance of L_{var} will be effective on Z_{int} at higher frequencies (>2 GHz). R_{var} is negligible compared to the impedance of L_{var}. L_{var} is the component that determines the amount of voltage at the gate of the transistor in the whole frequency band. (3-3) is rewritten as in (3-4) for frequencies > 2 GHz.

$$Z_{\text{int}}(\omega) = j\omega L_{\text{var}}(\omega) \quad \textbf{(3-4)}$$

It is obvious from (3-4) that L_{var} is effective on the gain of the amplifier in the full range of the band. L_{var} should be chosen very carefully in order to adjust the amount of the voltage that is to be amplified by the transconductance of each transistor.

In order to see the effect of reactive termination in Figure 3.2, a simulation using a CAD program named Advanced Design System 2006A (ADS) is performed. The values of the components shown in Figure 3.2 are chosen same as the ones of the first stage of the designed CRTSSDA. Those values for the components are given in Table 3-1.

Table 3-1 Component Values of Figure 3.2

	Symbol	Value	Units
Source Impedance	R_s	50	Ω
Series inductor of artificial line	L	0.2	nH
Inductor of reactive termination	L_{var}	1	nH
Resistor of reactive termination	R_{var}	50	Ω
Gate-to-source capacitance	C_{gs}	0.2	pF
Transconductance of transistor	g_m	80	mS

The input signal has a power of 0 dBm in the frequency range of 2-18 GHz and the corresponding simulation result is given in Figure 3.3

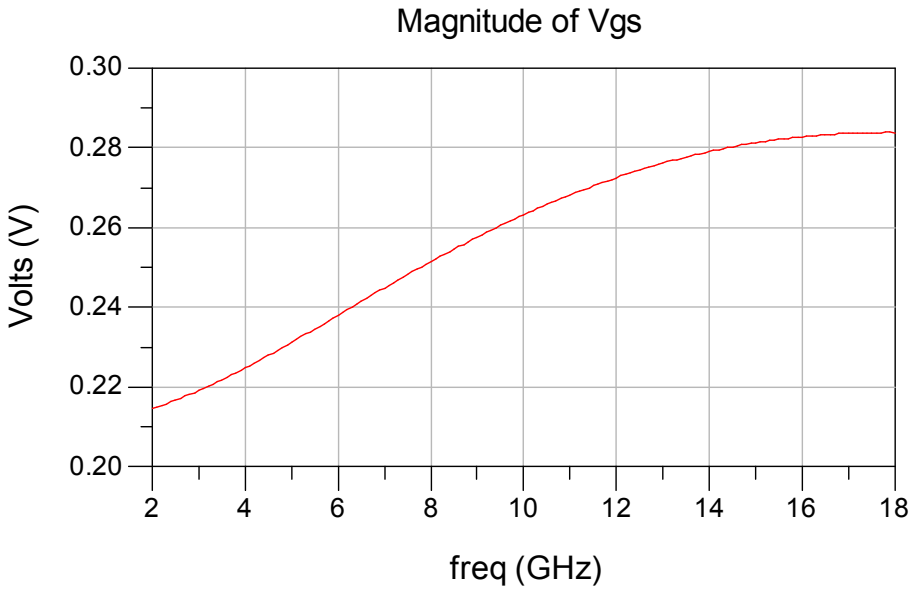

Figure 3.3 Enhancement of Voltage Swing Across C_{gs} With Reactive Terminations

Figure 3.3 shows that including reactive termination provides an increasing V_{gs} in the band. So the gain roll off of the transistors can be eliminated and gain flatness in broadband is provided.

3.3 Design of the Proposed CRTSSDA

Cascaded, reactively terminated, single stage distributed amplifier, having 2-18 GHz band with gain 23 $\pm$ 1.5 dB and VSWR<2 is designed in this thesis study. The transistors used in the design are Filtronic's FPD200, FPD6836 and FPD750 AlGaAs/InGaAs pseudomorphic high electron mobility (DPHEMT) transistors. The simulations during the design are performed on Advanced Design System 2006A (ADS). The schematic of the designed CRTSSDA is given in Figure 3.4

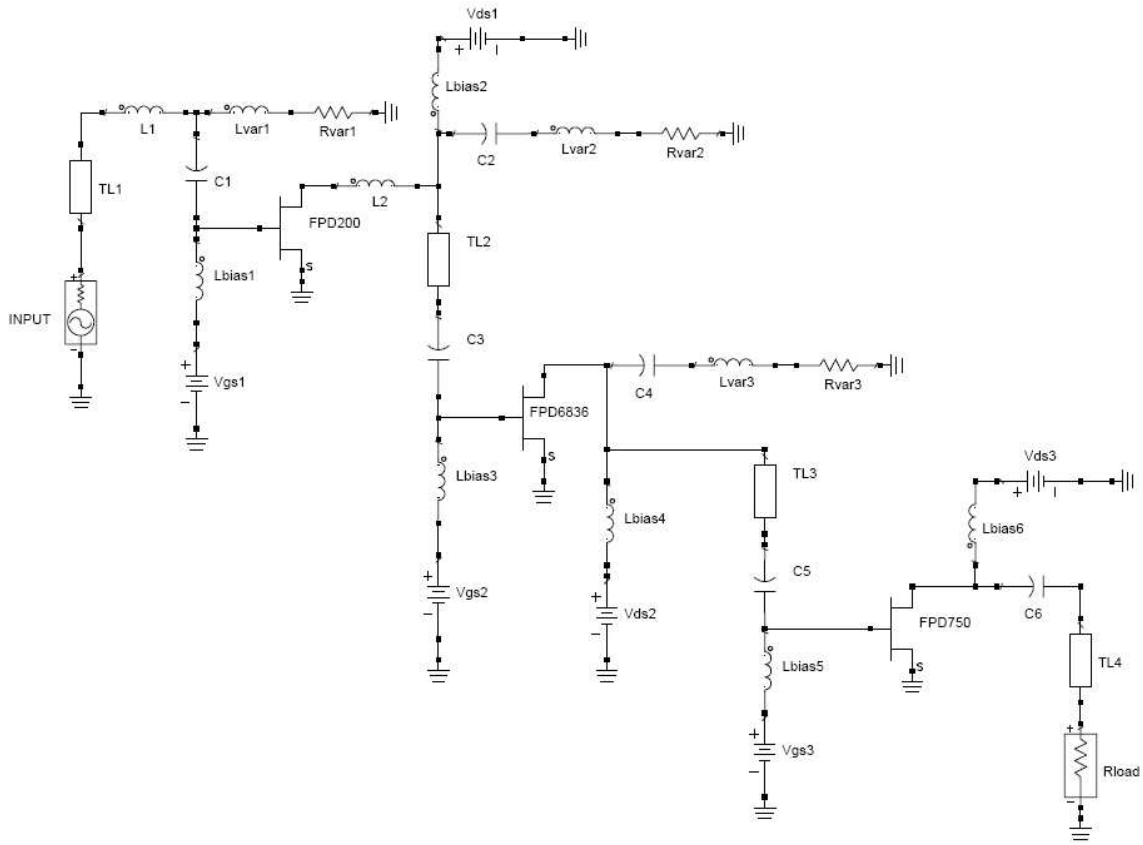

Figure 3.4 Schematic of the Proposed Amplifier

3.3.1 Brief description about the transistors used in the design:

FPD200

The FPD200 is an AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT), featuring a 0.25 μm by 200 μm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The recessed gate structure minimizes parasitic to optimize performance. The epitaxial structure and processing have been optimized for reliable medium-power applications [13].

FPD200 is used in die form to avoid package parasitic in the design. It is biased to -0.42 Volts at the gate and +5 Volts at the drain. The drain-to-source current (I_{ds}) is 30 mA. The transconductance of FPD200 is 80 mS. Electrical specifications of FPD200 are given in Table 3-2.

Table 3-2 Electrical Specifications of FPD200

	Min	Typ	Max	Units
Maximum Stable Gain	16	17		dB
Saturated Drain-Source Current	45	60	75	mA
Transconductance		80		mS
Power at 1dB Gain Compression	18	19		dBm
Power Gain at P1dB	10.5	12		dB
Gate-Source Breakdown Voltage	12	14		V
Gate-Drain Breakdown Voltage	14.5	16		V

FPD6836

The FPD6836 is an AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (PHEMT), featuring a 0.25 μm by 360 μm Schottky barrier gate, defined by high -resolution stepper-based photolithography. The recessed gate structure minimizes parasitic to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications [14].

FPD6836 is used same as FPD200 in die form to avoid package parasitic in the design. It is biased to -0.5 Volts at the gate and +5 Volts at the drain. The drain-to-source current (I_{ds}) is 32 mA. The transconductance of FPD6836 is 140 mS. Electrical specifications of FPD6836 are given in Table 3-3.

Table 3-3 Electrical Specifications of FPD6836

	Min	Typ	Max	Units
Maximum Stable Gain	15.5	16.5		dB
Saturated Drain-Source Current	90	110	135	mA
Transconductance		140		mS
Power at 1dB Gain Compression	24.5	25.5		dBm
Power Gain at P1dB	9	10		dB
Gate-Source Breakdown Voltage	12	14		V
Gate-Drain Breakdown Voltage	14.5	16		V

FPD750

The FPD750 is an AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (PHEMT), featuring a 0.25 μm by 750 μm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The recessed gate structure minimizes parasitic to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications. The FPD750 also features Si_3N_4 passivation [15].

FPD750 is used in die form like FPD200 and FPD6836 to avoid package parasitic in the design. It is biased to -0.55 Volts at the gate and +5 Volts at the drain. The drain-to-source current (I_{ds}) is 35 mA. The transconductance of FPD750 is 200 mS. Electrical specifications of FPD750 are given in Table 3-4.

Table 3-4 Electrical Specifications of FPD750

	Min	Typ	Max	Units
Maximum Stable Gain	13.5	14.5		dB
Saturated Drain-Source Current	185	230	280	mA
Transconductance		200		mS
Power at 1dB Gain Compression	26.5	27		dBm
Power Gain at P1dB	13.5	14.5		dB
Gate-Source Breakdown Voltage	12	14		V
Gate-Drain Breakdown Voltage	14.5	16		V

3.3.2 Design Procedure:

As mentioned in the previous section, reactive terminations are used to enhance the voltage swing at the gate of each transistor that will be amplified. Designing these reactive terminations is the vital point in design of the amplifier since the theory of CRTSSDA is based on this issue.

In Chapter 2, it is mentioned that gain of a CRTSSDA is higher than a conventional traveling wave amplifier (TWA) with the same number of stages [4]. Comparing the gains of CRTSSDA and TWA will give the constraint for Z_{int}.

Gain of an ideal lossless n-stage conventional TWA is given by [12]:

$$G_{TWA} = \frac{1}{4} g_m n^2 Z_0{}^2 \quad \textbf{(3-5)}$$

where n is the number of stages, Z_0 is the characteristic impedance of the system and g_m is the transconductance.

In CRTSSDA structure, transistors are cascaded and the preceding transistor's output is input for the next transistor. Gain expression for CRTSSDA is given by [16]

$$G_{CRTSSDA} = \frac{1}{4} g_m{}^{2n} Z_{\text{int}}{}^{2(n-1)} Z_0{}^2 \quad \textbf{(3-6)}$$

where Z_{int} is the internal characteristic impedance of the n-stage cascaded system and g_m and Z_0 are as before.

The following equation can be derived in order for the gain of CRTSSDA to be higher than the gain of TWA.

$$G_{CRTSSDA} \geq G_{TWA} \quad \textbf{(3-7)}$$

(3-5) and (3-6) are substituted in (3-7) and after the simplifications, an expression for Z_{int} can be derived for n>1.

$$Z_{\text{int}} \geq \frac{n^{\frac{1}{n-1}}}{g_m} \quad \textbf{(3-8)}$$

(3-8) shows that the impedance of reactive termination is dependent only on the number of stages, n, and the transconductance of the devices.

To estimate the value of Z_{int} for an amplifier including FPD200 transistors is done by substituting the value of transconductance of FPD200 into (3-8). If the designed amplifier is a 3-stage amplifier it will yield $Z_{int} > 21.65\ \Omega$.

Remember that (3-3) claims Z_{int} is equal to R_{var} at low frequencies. Therefore, since R_{var} is independent of frequency, one may choose R_{var} to be greater than 21.65 Ω. The final value of R_{var} is determined after the optimizations to meet a good VSWR. Another point that should be taken into account while choosing the values of R_{var} is that, in order to be able to fabricate the designed amplifier, it is required to choose standard resistor values. Thin-film resistors are used in fabrication of this thesis work; therefore, the values chosen for R_{var1}, R_{var2} and R_{var3} of Figure 3.4 are given in Table 3-5.

Table 3-5 Resistor Values of Reactive Terminations of the Designed Amplifier

	Symbol	Value	Units
Resistor of the 1st Reactive Termination	R_{var1}	50	Ω
Resistor of the 2nd Reactive Termination	R_{var2}	100	Ω
Resistor of the 3rd Reactive Termination	R_{var3}	50	Ω

Designing the reactive terminations will be completed after determination of L_{var}. (3-4) is used to determine the value of L_{var} at high frequencies (>2 GHz). Substituting (3-4) into (3-8) will give the expression for L_{var}.

$$L_{var} \geq \frac{n^{\frac{1}{n-1}}}{\omega g_m} \qquad \textbf{(3-9)}$$

(3-9) suggests that Lvar depends on the number of the stages of the amplifier, the transconductance of the devices used and also on frequency. L_{var} not only determines the amount of voltage at the gate of each transistor to be amplified, but also plays critical role in input and output return loss and matching between stages. Therefore, choosing the most proper value of L_{var} is important.

Unfortunately, (3-9) is not enough to choose the value of L_{var}. The most appropriate values of L_{var} in the reactive terminations of Figure 3.4 are determined during the optimizations. Estimated values of L_{var} in the proposed amplifier are listed in Table 3-6.

Table 3-6 Inductor Values of Reactive Terminations of the Designed Amplifier

	Symbol	Value	Units
Inductance of the 1st Reactive Termination	L_{var1}	0.6	nH
Inductance of the 2nd Reactive Termination	L_{var2}	2.4	nH
Inductance of the 3rd Reactive Termination	L_{var3}	1.5	nH

In a broadband amplifier design, it is required to include matching networks at input, output ports and between stages of the amplifier. Conventional schematic of a 2-stage amplifier with matching networks is given in Figure 3.5

Figure 3.5 The General Transistor Amplifier Circuit

Input matching circuit determines how much of the input power is coupled to the first stage. In order to have a reasonable VSWR, successful input matching is required. This is achieved by including a transmission line (TL_1) for impedance transformation, inductor L_1, capacitor C_1 and the reactive termination R_{var1} and L_{var1} in Figure 3.4.

Intermatching network between FPD200 and FPD6836 in Figure 3.4 is constructed by the transmission line TL_2, inductor L_2 and capacitor C_3. Capacitor C_3 not only

provides matching between the stages, but also isolates DC biasing of the transistors from each other. In addition, the combination of L_2, C_3 and TL_2 supports enhancement of voltage swing at the input of FPD6836 transistor with reactive termination R_{var2} and L_{var2}.

The second intermatching circuit is between the second and last stage, which are FPD6836 and FPD750 transistors. This matching circuit includes the capacitor C_5 and transmission line TL_3. These components also play a role on adjusting the voltage swing at the last stage with R_{var3} and L_{var3}.

Finally, an output matching circuit is included in the design of the proposed CRTSSDA. Output matching network is important because it determines the amount of power transmitted to the load and the output return loss. Inappropriate output matching can cause oscillations and also minimize the efficiency of the amplifier. As seen in Figure 3.4, transmission line TL_4 is used for impedance transformation between FPD750 and R_{load}, which is 50 Ω in the simulations.

3.4 Analysis and Simulation

The circuit given in Figure 3.4 is designed and analyzed using Advanced Design System 2006A. The components used in the circuit are ideal and lossless. TriQuint TOM3 Scalable Nonlinear FET Models [17] used to model FPD200, FPD6836 and FPD750 transistors in the simulations. TOM3 models for these transistors are given in Appendix A in detail.

There are two simulations performed for designing the proposed amplifier. In the first simulation, the components used are lossless and ideal and also, bond wires and other layout constraints applied on fabrication are not included in the simulation. These deficiencies cause unexpected results on fabricated amplifier measurements. In the second simulation, the experience gained throughout fabrication is used and more robust amplifier is designed considering experience on fabrication process. The layout constraints mentioned are the effect of pads left for mounting surface mount capacitors, thin-film resistors, bond wires that cause additional inductances and the

position of the components that are not included in simulations. These layout constraints and experience gained during fabrication will be explained detailed in the next chapter.

3.4.1 Simulation Results

3.4.1.1 1st Trial

In the first design, the proposed CRTSSDA is constructed with ideal and lossless components. TOM3 models are used to simulate the transistors. The schematic of the finalized design is given in Figure 3.6.

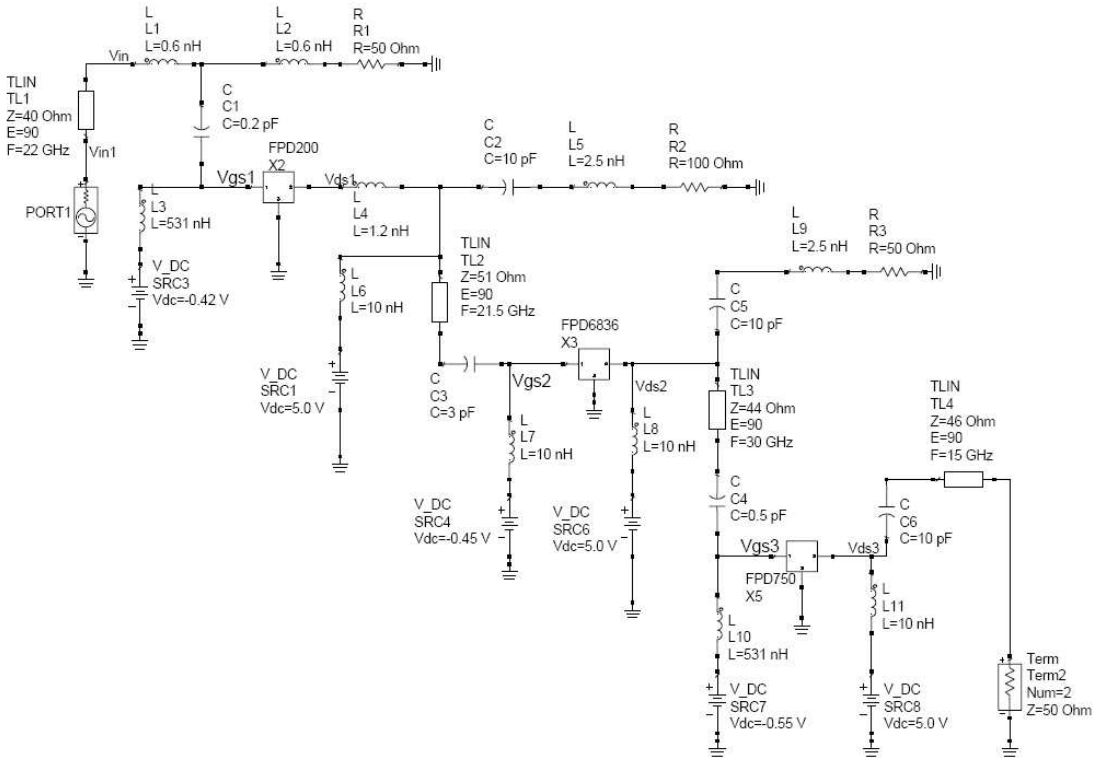

Figure 3.6 Schematic of the Firstly Designed CRTSSDA

Simulations of the circuit given in Figure 3.6 are performed by s-parameter analysis on ADS. Figure 3.7 and Figure 3.8 give S21, S11 and S22 plots of simulation results respectively.

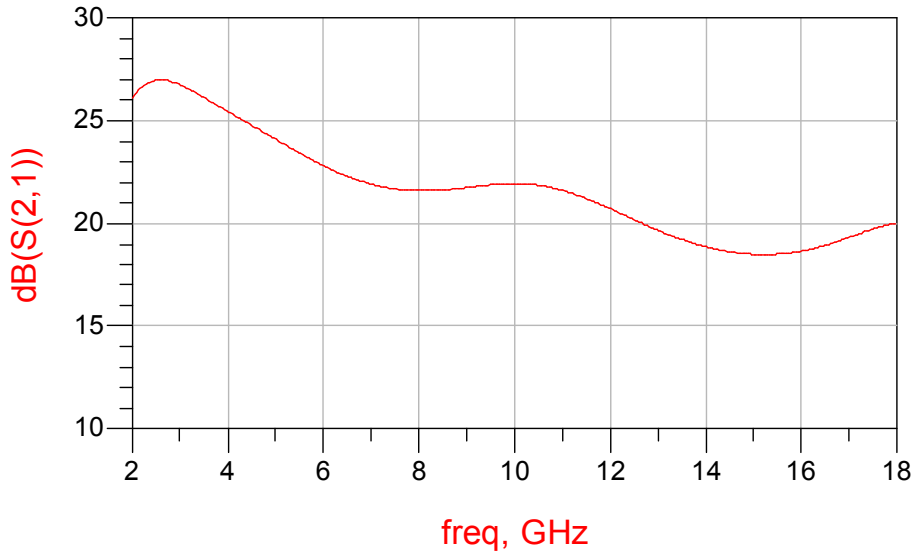

Figure 3.7 S21 Plot of The First CRTSSDA

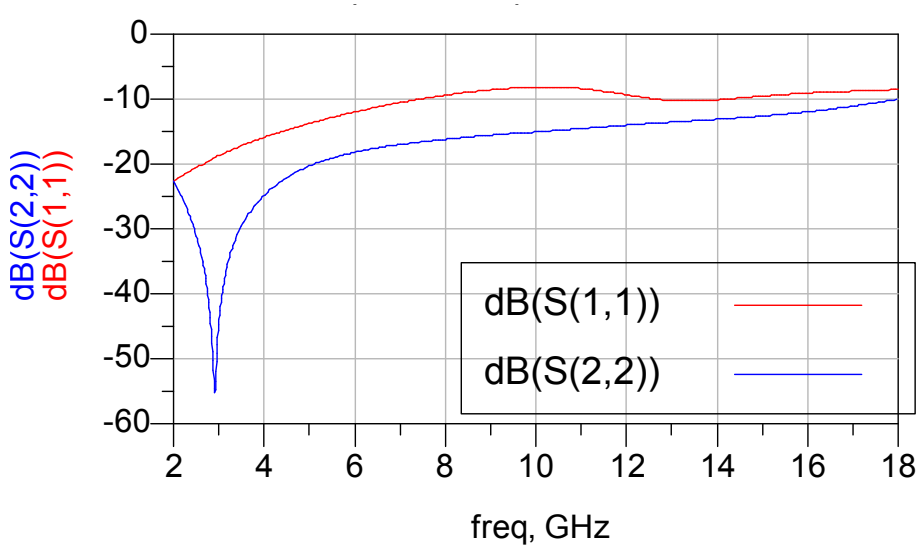

Figure 3.8 S11 and S22 Plots of The CRTSSDA

In order to see the enhancement of voltage swing provided by reactive terminations at the gate terminals of each transistor, harmonic balance simulation is ran on ADS. The nodes representing V_{gs} of each transistor are labeled in Figure 3.6. The following plots clearly show the aimed enhancements at these nodes.

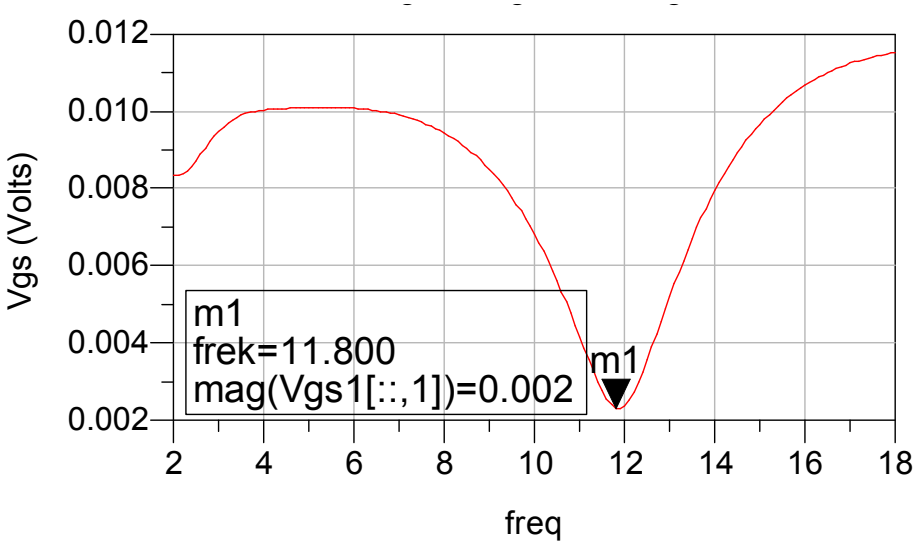

Figure 3.9 Voltage Swing Enhancement of The First Stage

Figure 3.9 gives the voltage across the gate of FPD200 at the first stage with respect to frequency. Reactive termination for the first stage seems to compensate the gain roll off of the transistor, however, there is a resonance at f = 11.8 GHz as seen from the marker on the plot. The source of the resonance is thought to be the combination of the inductor L_4 in Figure 3.6 and gate-to-source capacitance C_{gs1}. Simulations performed to see the reason of that resonance showed that changing the value of L_4 slides the frequency of resonance. However, despite of the resonance at 11.8 GHz, there is no resonance in the overall gain of the amplifier, because the voltage swing enhancements at the remaining stages compensate the notch of first stage at 11.8 GHz. This assertion is also proved by fabrication and measurement experience, where the existing oscillations are removed by tuning L_4, which is explained in the next chapter in detail.

Enhancements on voltage swing of the second and the third transistor gate voltages are given in Figure 3.10 and Figure 3.11 respectively.

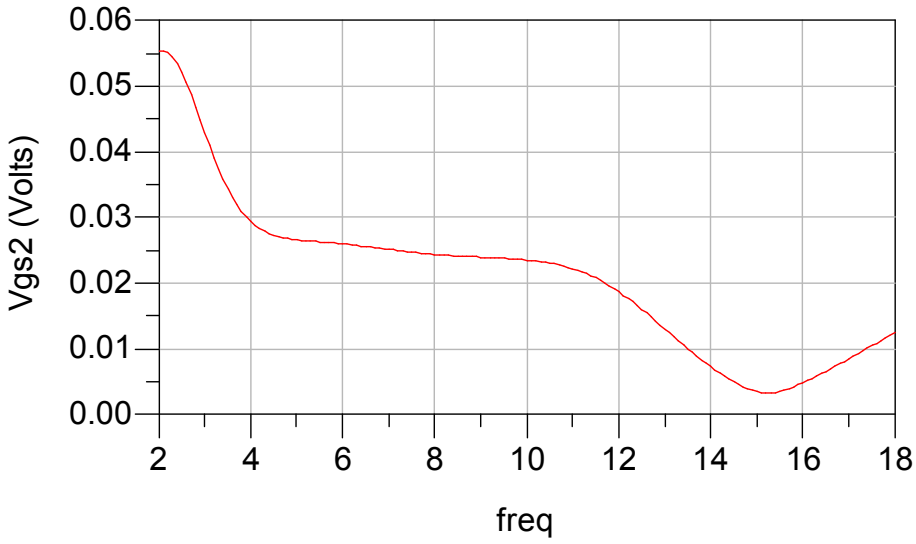

Figure 3.10 Voltage Swing Enhancement of The Second Stage

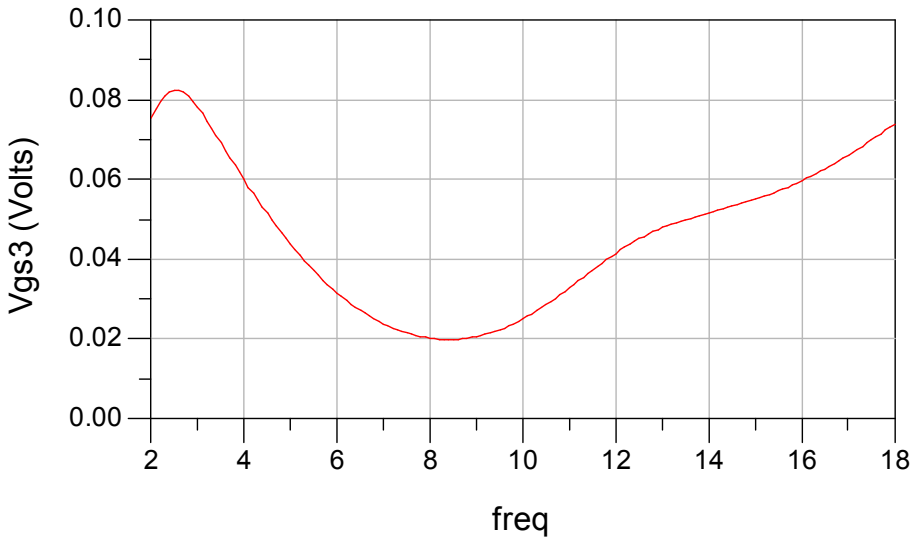

Figure 3.11 Voltage Swing Enhancement of The Third Stage

3.4.1.2 2nd Trial

In the first simulation, the gain obtained from CRTSSDA is 22 ± 4 dB as given in Figure 3.7. There is a dramatic decrease of gain between 2-7 GHz which has to be improved. These results are also observed during the measurements of the fabricated amplifier. Having the layout experience, which will be mentioned in the next chapter,

the reasons for these deficiencies are noted and a second simulation is performed to solve these problems.

Second simulation contains all the contributing effects to the response of the amplifier such as layout pads, parasitic of the transistors and possible additional inductances caused by wire bonding. The schematic of the second design is given in Figure 3.12.

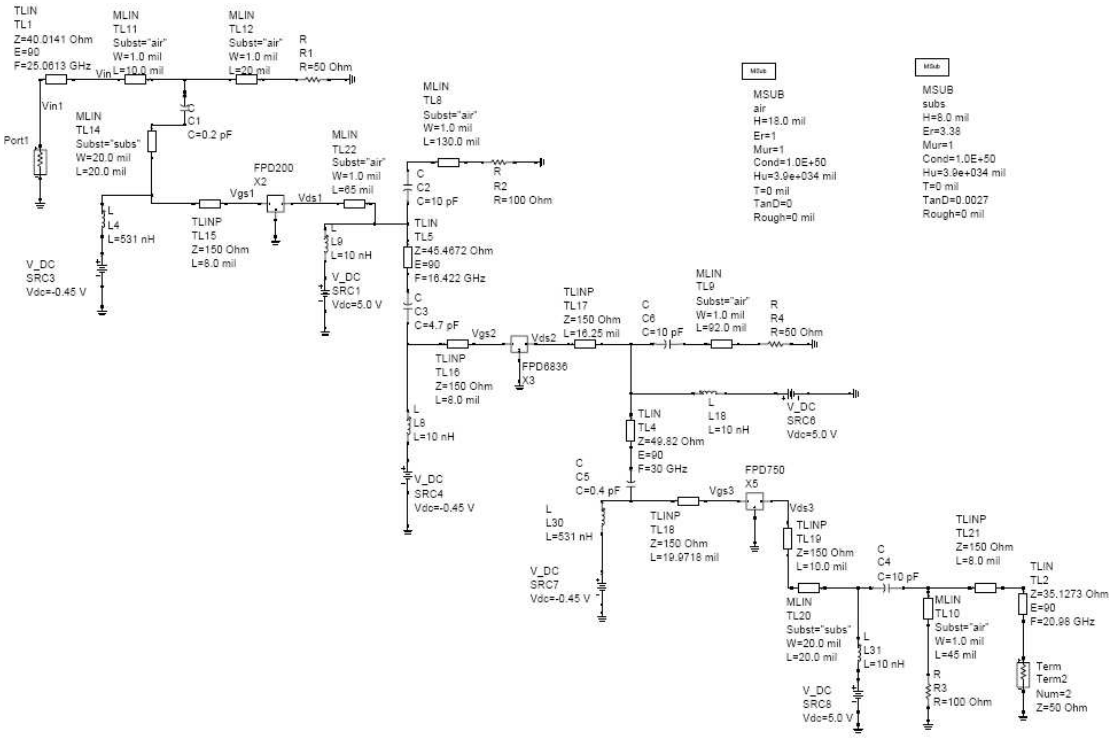

Figure 3.12 Schematic of The Second CRTSSDA

Note that the inductors except the choking coils in the first simulation are replaced with equivalent transmission lines, since these inductors are realized by wire bonding during fabrication. Replacing the inductors with transmission lines gives the ability to tune their values easily while making measurements on the fabricated amplifier. Transmission lines TL_{14} and TL_{20} of Figure 3.12 represent the pads left for mounting capacitors C_1 and C_4, which cause extra capacitance that is not taken into account for the first simulation. Results of the simulations are given by the following plots.

Figure 3.13 gives the s-parameter simulation result for the gain expression of the amplifier. Gain of this amplifier is 23 ± 1.5 dB which is more successful than the first design in terms of gain flatness.

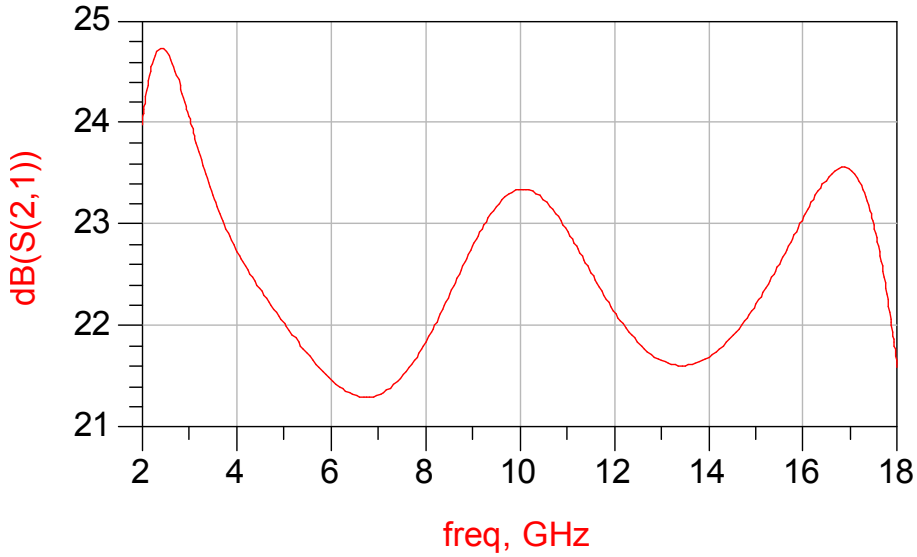

Figure 3.13 S21 Plot of The Second CRTSSDA

Input and output return loss for the second CRTSSDA is given in Figure 3.14.

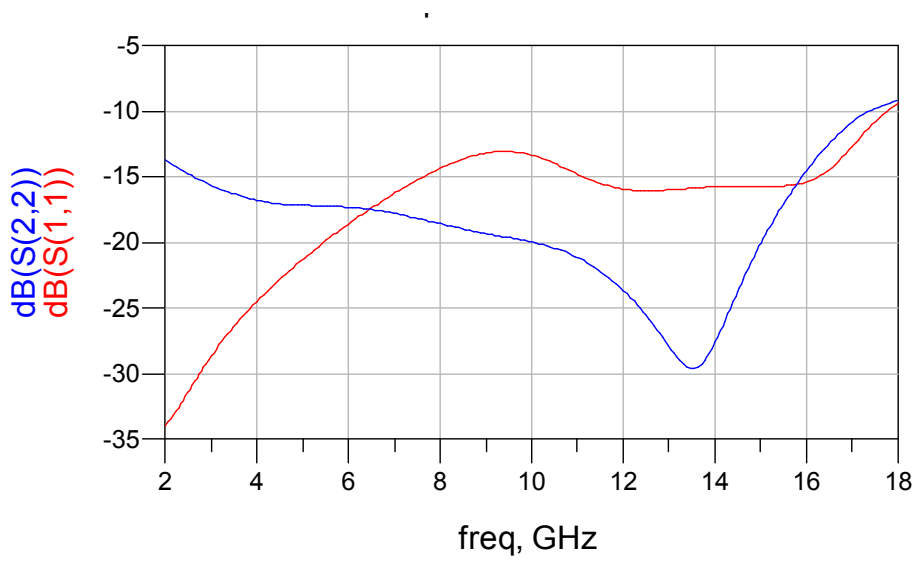

Figure 3.14 S11 and S22 Plots of Second CRTSSDA

The second trial of CRTSSDA is better than the first trial in terms of gain flatness and input and output return loss. Also experience gained during fabrication of the first amplifier is employed on simulations of the second amplifier to get similar responses of the simulation and measurement of the second amplifier.

CHAPTER 4

FABRICATION AND MEASUREMENT

Fabricating an operating broadband amplifier is as difficult as designing it. There are many contributors to the response of the amplifier that cannot be observed during simulations on CAD programs. The components used in simulations are usually ideal components. Unfortunately, non ideal models of components are not always successful to model components exactly. Parasitic of both active and passive devices add up with additional layout pads left for mounting components and wire bonds for connections and result in a deviation of expected response of the amplifier.

Two different CRTSSDA amplifiers are designed in this thesis work as mentioned in the previous chapter. The first design is simulated using ideal components. Package parasitic of transistors are included in TOM3 models, where they should not be included, since the transistors used are in die form in this design. When the designed amplifier is fabricated, unexpected results are observed during measurements. The differences between simulation results and measurements are observed carefully to identify the reasons of failures. After determining the factors of unexpected results, a second design is performed. The second design includes effects of bond wires used for connections, additional layout pads, and package parasitic are not included in TOM3 models.

4.1 Choosing the Appropriate Substrate

Apart from component models or parasitic, the choice of substrate used on fabrication is also one of the most important tasks that must be taken into consideration.

The substrate used in high frequency applications, i.e. $f \geq 2\,\text{GHz}$, should be chosen carefully. The attenuation of substrate plays one of the main roles in these applications. The width of the substrate and tangent loss are the other factors that affect the performance of the substrate.

In Virdee's CRTSSDA [8], alumina substrate with $\varepsilon_r = 9.8$ and height = 0.318 mm is used for the microstrip medium. On the other hand, the designed amplifiers of this thesis work are realized on Rogers4350 and Rogers4003 with permittivity $\varepsilon_r = 3.48$ and $\varepsilon_r = 3.38$ respectively. The substrate height for Rogers4350 is 0.254mm where the height of Rogers4003 is 0.2032 mm. Choosing lower height for dielectric thickness is important since the attenuation caused by the substrate increases proportionally with the height of dielectric. Dielectric loss affects the response of the amplifier in terms of a decrease in gain at higher frequencies.

Dielectric constant of a substrate varies with temperature. Amplifiers dissipate heat in a small area which causes high temperatures on board. If the substrate used on fabrication is very sensitive to temperature changes, it may result unpredictable results. Characteristic impedances of transmission lines evaluated in room temperature may change after a few minutes from power on. Change in characteristic impedance of transmission lines causes impedance mismatches that results decrease in gain and ruined input return loss. Rogers4350 substrate used in the first fabrication possesses a dielectric constant change by 0.8% between -50˚C to 150˚C. In the realization of the secondly designed amplifier, the substrate used is Rogers4003 and its dielectric constant changes 0.3% between -50˚C to 150˚C.

Another attribute of a substrate that affects the performance of the dielectric is the dissipation factor or tangent loss. Dissipation factor of Rogers 4350 is 0.037 where it is 0.027 for Rogers 4003.

4.2 Assembling the Components on PCB

The fabrication of the amplifier starts with the assembly of transistors on PCB. An appropriate amount of electrically conductive epoxy-adhesive is applied on the relevant points on PCB that the transistors lay on. After applying epoxy, the transistors are located on the epoxy-adhesive. The purpose of the epoxy-adhesive is to hold the components on PCB mechanically and to support heat and electrical conductivity. In order for epoxy to function properly, the PCB is kept in an oven at 80˚C for 1.5 hours. Keeping the circuit in the oven hardens the epoxy and makes it conductive.

Wire-bonds of the transistors from source pads to ground and from drain and gate to the relevant pads are applied by a ball bonder machine after taking the amplifier out of the oven. The connections of the transistors are realized by golden wire bonds of diameter 18 um. The other wire bonds applied on the circuit to connect capacitors or resistors are realized by golden wire bonds of diameter 25 um. The reason for using thinner wire bonds for transistors is that the pads on transistors are not large enough for 25 um wire bonds. Figure 4.1 shows the ball bonder machine Kulicke Soffa AG 4124 used in fabrication of the designed amplifiers.

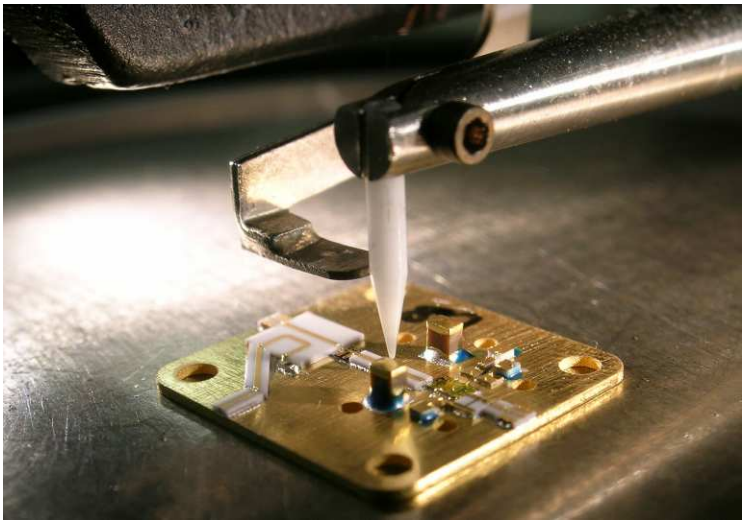

Figure 4.1 Ball Bonder Kulicke Soffa AG 4124

After assembling the transistors, remaining components are mounted on PCB. These remaining components are thin-film resistors, parallel plate capacitors and biasing coils. Thin-film resistors and parallel plate capacitors are laid on epoxy-adhesive like the transistors and then the PCB is kept in the oven at 80˚C for 1.5 hours for the second time.

After bonding the capacitors and thin-film resistors, the biasing coils are added in the circuit. The coil tips are Teflon-plated where Teflon is a non conductive material. In order to acquire conductance on the tips, the covered Teflon is removed by a lancet. Attention must be paid while shelling the coil in order not to harm the copper of the wire.

Figure 4.2 An Air Core Coil, A Shelled Tip, And Wedge Bonding On A Capacitor

The coils are connected by Unitex Equipment Wedge Bonder machine. Figure 4.2 shows an air core biasing coil of 10 nH, a coil tip that is shelled and a coil wedge bonded on a capacitor.

After mounting all the components on board, RF connectors are soldered. RF connector's ground must be in touch in an as large as area for a good input reflection loss. Capacitors used for filtering the bias sources are also soldered to source pads left on PCB design. Wire bonds can be applied only to the gold plated areas on PCB, therefore, solder used for mounting filtering capacitors or connectors must not spread over the gold plated areas.

4.3 Measurement Setup and DC Biasing of Transistors

Measurement of an amplifier consisting of die-form transistors is a challenge. The transistors are very sensitive to electrostatic discharge (ESD). Handling precautions should be taken during the measurements in order to prevent ESD problems. Another point that should be paid attention on is that biasing of the transistors should be done in the appropriate order.

Transistors FPD200, FPD6836 and FPD750 are n-channel transistors. Therefore, gate-to-source (V_{gs}) biasing voltages are negative for these transistors. Drain-to-source voltages (V_{ds}) are positive and should not be applied before V_{gs} is on. It is given in the datasheets of the transistors [13-15] that $0 > V_{gs} > -3V$. In order to prevent drain port to pull high currents, V_{gs} is hold at -3V at start up.

After switching V_{gs} on at -3V, V_{ds} is gradually increased from 0V to +5V. The required drain currents are approximately 30 mA at each transistor as designed and simulated. During these steps, the gate-to-source current should be 0 mA. If there is any current drawn from gate ports, there seems to be problem about the transistors. At the moment where $V_{gs} = -3V$ and $V_{ds} = 5V$, the expected drain current (I_{ds}) is 0 mA. Now, to make the channel of the transistor on, V_{gs} is gradually increased until $I_{ds} = 30mA$. The biasing voltages and corresponding currents are given in Table 4-1.

Table 4-1 Biasing Current and Voltage Values of Transistors

	1st Fabricated Amplifier			2nd Fabricated Amplifier		
Transistor	V_{gs} (V)	V_{ds} (V)	I_{ds} (mA)	V_{gs} (V)	V_{ds} (V)	I_{ds} (mA)
FPD200	-0.45	5	26	-0.42	5	25
FPD6836	-0.60	5	32	-0.60	5	30
FPD750	-0.66	5	37	-0.70	5	29

Limiting current that is drawn from DC supplies is an effective way to prevent transistors from burning out. DC power supplies are limited to 10mA at the terminals that supply gates of the transistors and to 50mA that supply drain ports.

Unfortunately, unexpected high currents do not always mean that there is a problem about the transistors. High current and unstable voltage values usually mean that the amplifier faces oscillation problems. It is usually hard to find the source of oscillations. During measurements, various oscillations are observed and how to remove these oscillations are explained in the next sections.

Measurements of the fabricated amplifiers are performed using Agilent Technologies E8364B PNA Network Analyzer, Agilent Technologies E3631A Triple Output DC Power Supplies and a microscope of Cambridge Instruments. The measurement setup is given in Figure 4.3.

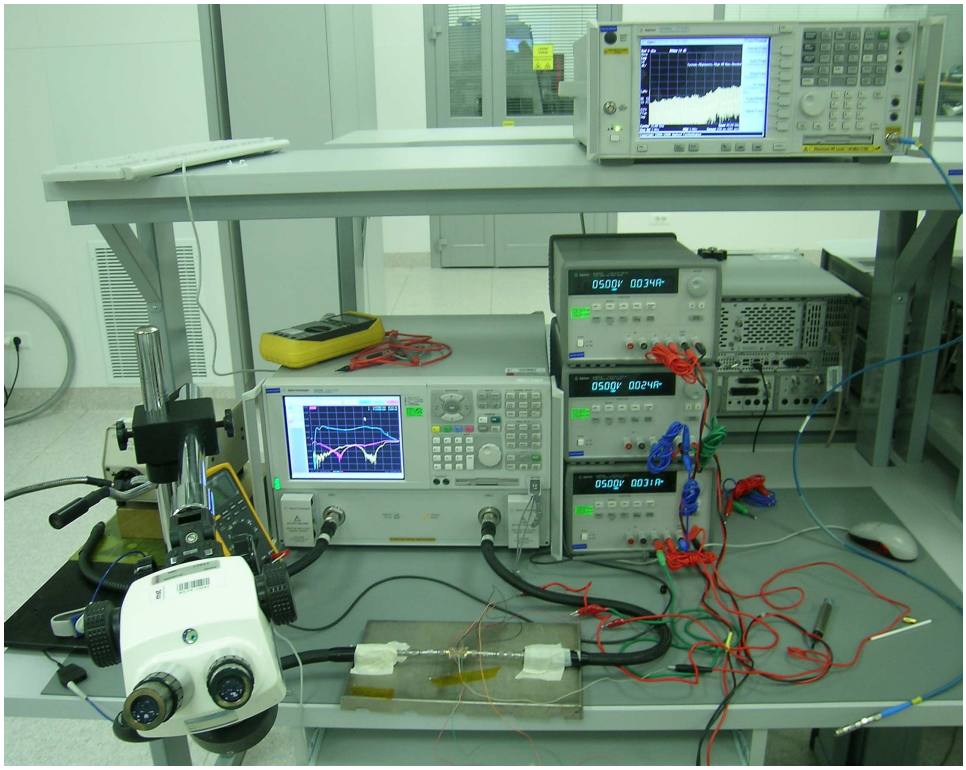

Figure 4.3 Measurement Setup

While measuring the fabricated amplifiers, attenuators of 10dB, operating between DC-40 GHz are included both at the input and output of the amplifiers. The reason of including attenuators is to prevent any damage to the measurement devices in case of any oscillation. The calibration applied on network analyzer before measurement consists of these attenuators.

Agilent Technologies 85052 B 3.5mm calibration kit is used to calibrate the network analyzer. A successful calibration is one of the important tasks that must be performed to have accurate results. Since the measured device is an amplifier, it has a high tendency to oscillate. In order not to damage PNA in case of any oscillation, port input power is adjusted to -40 dBm. The number of points of calibration is set to 1601 points in order to have a good resolution on the response.

4.4 Layout of the First Amplifier

Layout of the first designed amplifier is fabricated on Rogers 4350 substrate with height 0.254 mm and relative permittivity $\varepsilon_r = 3.48$. The first designed amplifier is given in Figure 3.6. Figure 3.6 is redrawn as Figure 4.4 below for convenience.

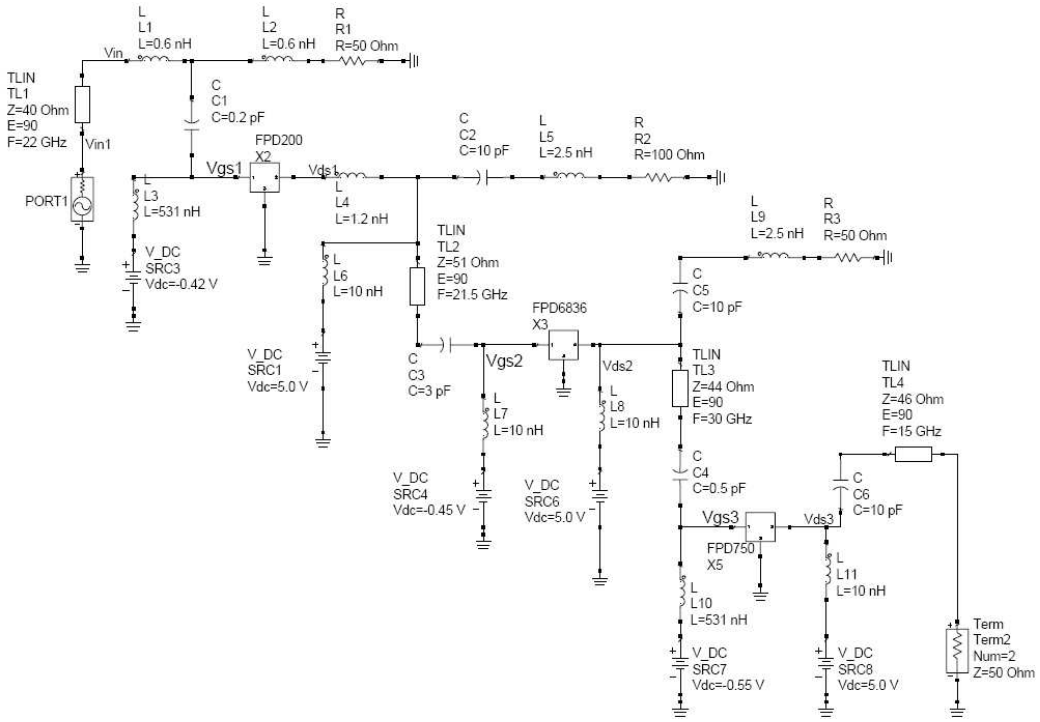

Figure 4.4 Schematic of the First Designed CRTSSDA

Inductors of Figure 4.4 are all packaged inductors except L_1 and L_2 at the input of the first stage. The packaged inductors are in 201 geometry, which are thought to operate at 18 GHz. L_1 and L_2 are realized by wire bonding during fabrication. It is observed from simulations that values of L_1 and L_2 affect the gain and VSWR in the whole band. Tuning L_1 and L_2 is done by changing the length of the bonds or bending to make far or near to the ground plane. Inductance of a wire bond is calculated as follows:

$$L(nH) = 2 \times l \times (\ln(l/d) + 0.5 + 0.22 \times 2 \times d/l)/10000 \qquad \textbf{(4-1)}$$

where L is the resultant inductance in nH; l is the length and d is the diameter of wirebond both in um.

Diameter of the wirebond used in fabrication is 25 um. In order to have 0.6 nH inductance for L_1 and L_2 in Figure 4.4, it is estimated that the required length of the wirebond is approximately 770 um from (4-1).

Capacitors C_1, C_2, C_3, C_4, C_5 and C_6 in Figure 4.4 are parallel-plate 254um x 254um surface mount capacitors. They are stick on the board by epoxy at one side and then held in oven for an hour at 80˚C. The other side of the capacitor is the area where the necessary wire bondings are applied.

FPD200, FPD6836 and FPD750 transistors are also mounted on board like capacitors. These transistors' source-pads are not grounded by default. Therefore, their source-pads are connected to ground plane of board via wire bonding. Wire bonding made from the transistors' source-pads must be as short as possible in order not to have additional inductance from source to ground. Any inductance from source-pad of a transistor to ground results loss in gain which is observed during simulations. The length of wire bonds from source pads of transistors to ground are a few micrometers length in the fabricated amplifiers of this thesis work.

Transmission lines seen in Figure 4.4 are realized as microstrip lines. The width of a microstrip line is determined by its impedance value, relative permittivity and height of the substrate used. The length of a microstrip line is determined by frequency and electrical length of the transmission line. The values of impedance and the frequency where the electrical length of the line is 90˚ are listed in Table 4-2.

Table 4-2 Estimated Dimensions For Transmission Lines in Figure 4.4

	Impedance(Ω)	Frequency @ E=90˚	Width(mm)	Length(mm)
TL_1	40	22 GHz	0.81	2
TL_2	51	21.5 GHz	0.56	2.01
TL_3	46	15 GHz	0.65	2.98

After determining the dimensions of the transmission lines, the task is now to locate the components on board carefully for connecting the components at minimum distance from each other. The length of wire bonds between components must be

minimized to avoid additional inductances. In order to be able to solder connectors, 50Ω microstrip lines with length 4mm is left at the input and output of the amplifier. Also as seen in Figure 4.5, the edged board is gold plated to be able to make wire bonds available.

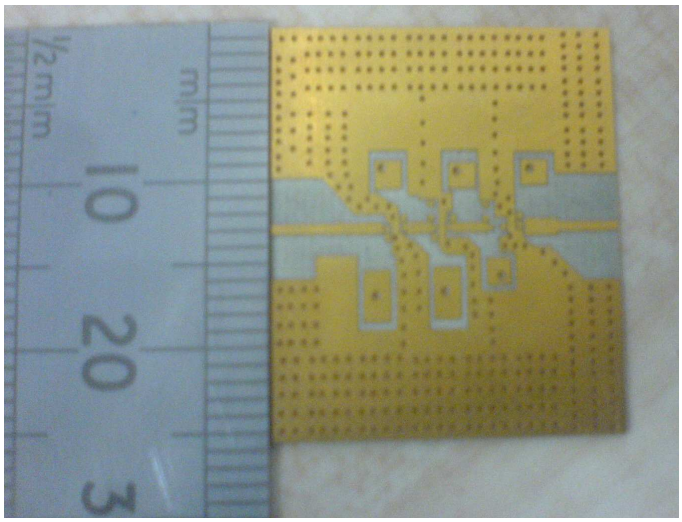

Figure 4.5 Layout of the First Designed CRTSSDA

The components are assembled on PCB in clean room facility of ASELSAN Inc. The fabricated amplifier is given in Figure 4.6.

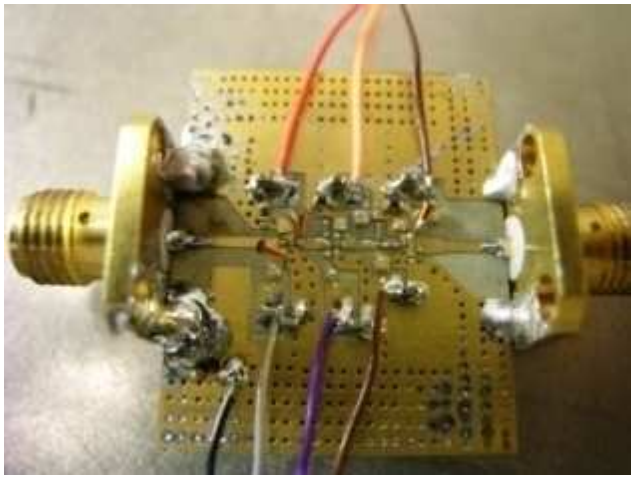

Figure 4.6 First Fabricated CRTSSDA

After the assembling of the amplifier, measurements are performed. These measurements are compared with the simulations of the first design.

4.5 Measurements of the First Amplifier

The amplifier given in Figure 4.6 is measured. In the first measurement of the amplifier, there are observed oscillations at f ≤200 MHz. These low frequency oscillations are seen because the matching of the transistors is valid for 2-18 GHz. Low frequency oscillations are removed by adding serial resistors to the gate biasing of the transistors. The values of resistors connected to the gate biasing are determined by the gate peripheries of the transistors. These values are listed in Table 4-3.

Table 4-3 Resistors Included to Prevent Low Frequency Oscillation

	Symbol	Value	Units
Resistor of the 1st Bias	R_{b1}	50	Ω
Resistor of the 2nd Bias	R_{b2}	30	Ω
Resistor of the 3rd Bias	R_{b3}	15	Ω

Therefore, the biasing circuit is applied as in Figure 4.7 for the first stage. Same biasing circuits with the values of the resistors in Table 4-3 are applied at each stage.

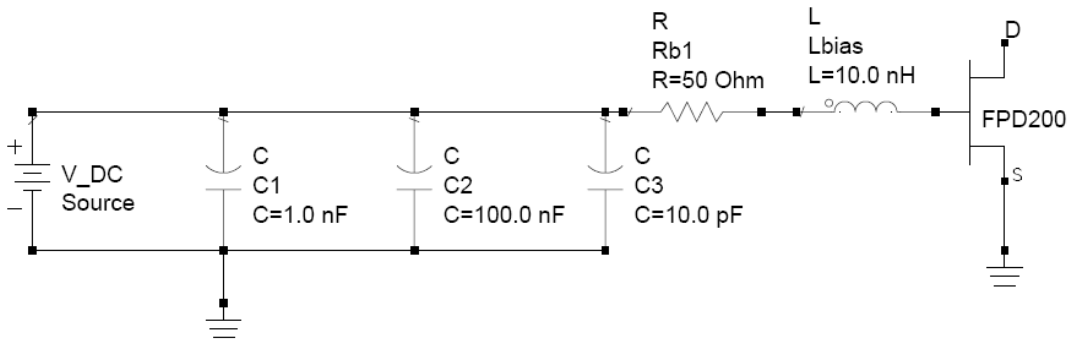

Figure 4.7 Gate Biasing of The First Stage

After eliminating low frequency oscillations by including series resistor as shown in Figure 4.7, s-parameter measurement is performed. In this measurement there appeared another oscillation at f = 2 GHz. Inductor L_{bias} of Figure 4.7 is an air cored inductor. During tunings on the amplifier, when the turnings of the inductor are loosened, the oscillation frequency shifts to 1.04 GHz. Shifting of oscillation frequency shows that the source of oscillation is the biasing coil. The oscillation can be observed in Figure 4.8.

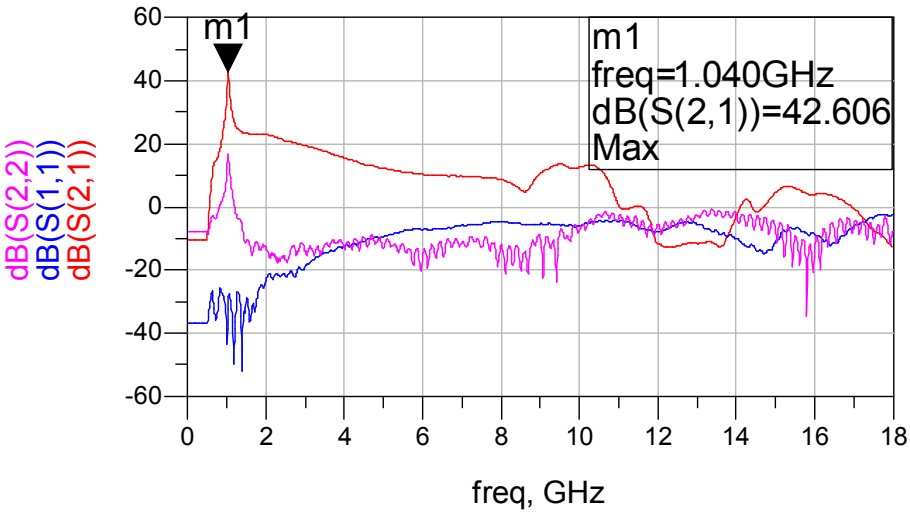

Figure 4.8 Oscillation Caused By Biasing Inductor

The oscillation seen in Figure 4.8 is eliminated by changing L_{bias} to a conical biasing inductor of value 531 nH as seen in Figure 4.4. The s-parameter result of the amplifier after eliminating oscillation is given in Figure 4.9.

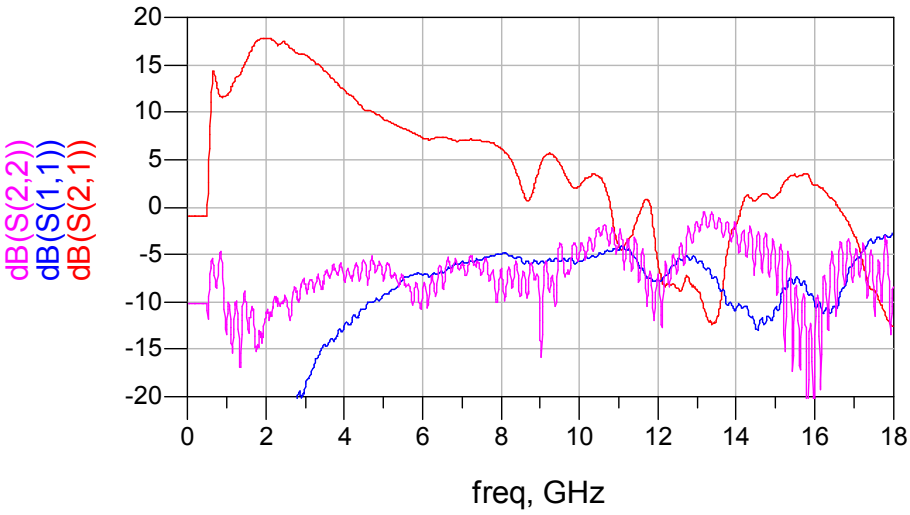

Figure 4.9 S-Parameters After Eliminating Oscillation

Despite that the oscillations are eliminated, the gain and input and output matching of the amplifier seem to be unsuccessful according to the simulation results given in

Figure 3.7 and Figure 3.8. Tunings and improvements are applied on the circuit to correct the response of the amplifier.

Grounding in high frequency applications is one of the important tasks that an engineer must pay attention. Via holes seen in Figure 4.5 are placed at 0.6 mm away from each other. Distance between vias should be λ/10 conventionally, where λ is the wavelength of the signal. The expression to calculate wavelength is given in (4-2)

$$\lambda = \frac{c}{f\sqrt{\varepsilon_r}} \tag{4-2}$$

Where c is the velocity of light in m/s; f is the frequency in Hertz and ε_r is the dielectric constant of the substrate.
Wavelength, λ, for f = 18 GHz is estimated to be 8.9 mm for Rogers 4350. Therefore, minimum distance between via holes should be 0.89 mm. 0.6 mm distance between via holes therefore seems to be acceptable.

However, a good grounding is not only related with the distance of via holes. The ground of connectors should be in touch with PCB's ground at the largest area it can. A copper plate is soldered to the ground area of the connector and the other end of the copper plate is soldered to the PCB in Figure 4.6. In order to see the effect of good grounding of the connectors the following measurement result is given in Figure 4.10

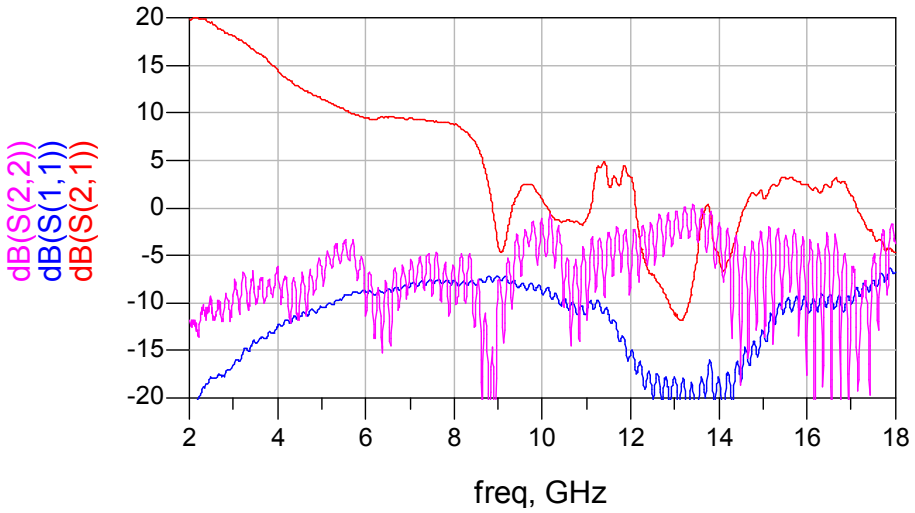

Figure 4.10 S-Parameters After Improved Grounding of Connectors

Input return losses, S(1,1) of Figure 4.9 and Figure 4.10 are redrawn in Figure 4.11 to see the effect of grounding:

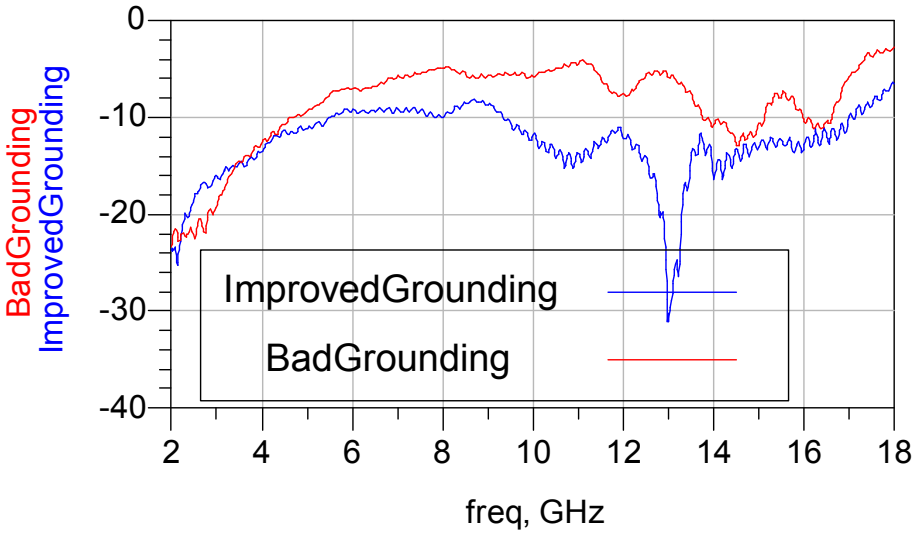

Figure 4.11 Input Return Loss After Improved Grounding of Connectors

Although the input return loss is improved it is still not acceptable for the designed amplifier. The aimed VSWR of the amplifier is less than 2.0, therefore it is required

to have a input return loss that is better than 9.5 dB. Gain and the output return loss also seem to be unsuccessful from Figure 4.10.

In order to have the expected response of the fabricated amplifier in Figure 4.6, tunings are performed on the components. It is observed from the tunings that biasing coils should be as near as to the gate and drains of the related transistors. In other words, the RF path to the biasing DC sources must be very short. In the first measurements given before, the biasing coils are wire bonded on the capacitors and then connected to the related port of the transistor via wire bonding. That wire bonds connecting biasing coils to the transistors behave like small valued inductors in a few nH values. These inductances demolish the input and inter stage matching. Therefore these extra inductances cause a decrease in gain and a bad VSWR.

In order to improve the gain and matching of the amplifier, the biasing coils are reconnected to the related terminals to shorten the RF paths toward DC sources. The improved circuit is measured and the following response is obtained.

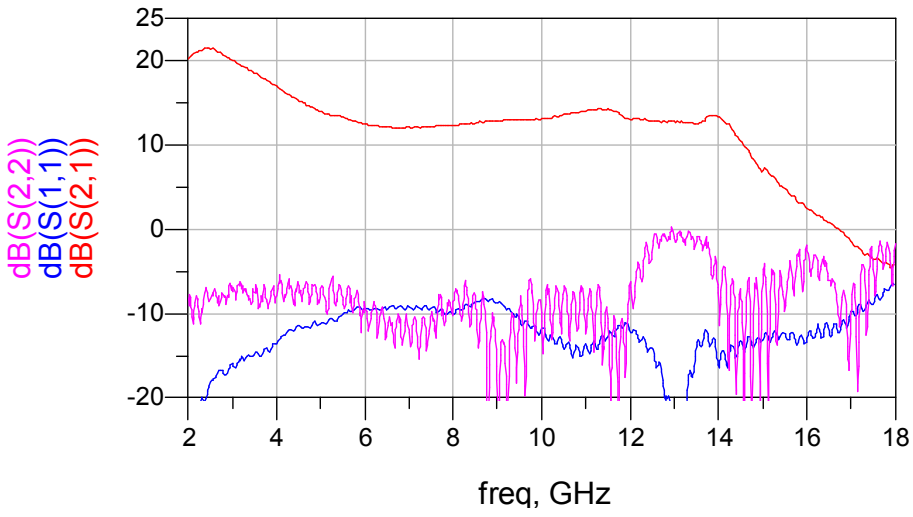

Figure 4.12 Final Response of the First Fabricated Amplifier

Figure 4.12 shows that the input return loss is improved to an acceptable level. Fabricated amplifier operates up to 14 GHz; however its gain is not as high as in the simulation results. Tunings on biasing coils and shortening the length of wire bonds

are not enough to improve the whole response. There are also extra pads left for mounting capacitors on the PCB. For example a square of 20milx20mil area is left for a 10milx10mil parallel plate capacitor. The pad area also exhibits as an additional capacitor that is not included in the simulation. Therefore, the expected result differs than the simulation results.

Another deficiency of the design is that, wire bonds are not included in simulations. Although the lengths of the wire bonds are minimized during tunings, they are still in existence and act like small valued inductors. A series inductor means loss in an amplifier circuit, and this loss becomes evident at high frequency. The gain roll off seen after 14 GHz in Figure 4.12 is caused by the wire bonds that are not included in simulations.

Another dramatic decrease in gain is between 2-6 GHz in Figure 4.12. However, this gain roll-off is not caused by deficiencies of inclusion of wire bonds or additional pads. This gain roll-off between 2-6 GHz is also observed on simulation results. That gain roll-off is caused by the inclusion of the parasitic of the transistors in TOM3 models. As mentioned in the previous sections, the transistors used in this thesis study are in die-form. In other words, package parasitic of transistors do not exist in this application.

Figure 4.13 below shows the simulation result and measurement gain plots on the same figure.

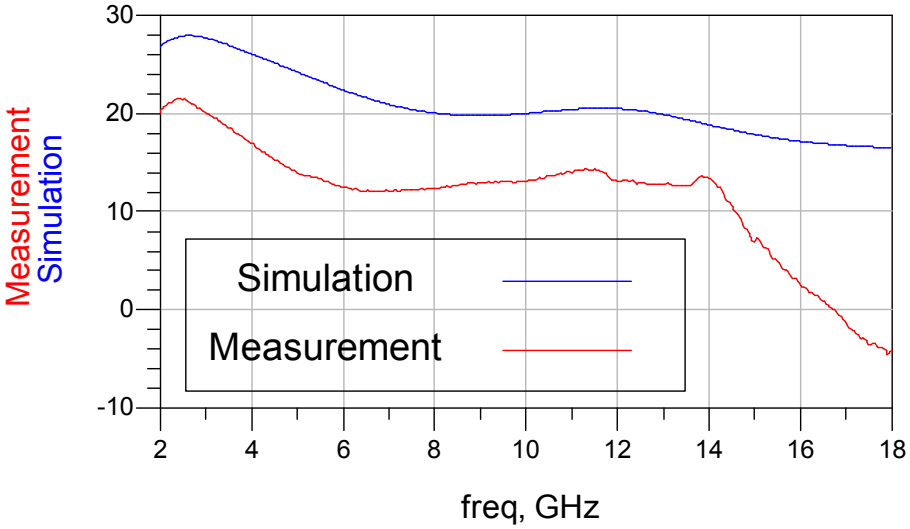

Figure 4.13 Comparison of Simulation and Measurement Gains

It is observed from Figure 4.13 that the measurement and simulated gains are in parallel up to 14 GHz. The fabricated amplifier's gain is approximately 8 dB lower than the simulated results. It is mentioned previously that the gain roll-off after 14 GHz is evident because of the wire bonds that are not included in the simulation. Now if the results are considered up to 14 GHz, it is obvious that the gains of both simulation and measurement have similar slopes. The difference of 8 dB between the simulated and measurement gains are thought to be because of the losses of dielectric material, the loss of the connectors that are not considered in simulation and additional inductances of the wire bondings on the RF path.

Having these experiences in fabrication and measurement of the first amplifier, a second simulation is done. The fabricated amplifier of the second design is measured and the results are given in the next sections in this chapter.

4.6 Layout of the Second Amplifier

Layout of the second amplifier is fabricated on Rogers 4003 substrate with height 0.2 mm and relative permittivity $\varepsilon_r = 3.38$. The secondly designed amplifier is given in Figure 3.12. Figure 3.12 is redrawn as Figure 4.14 below for convenience.

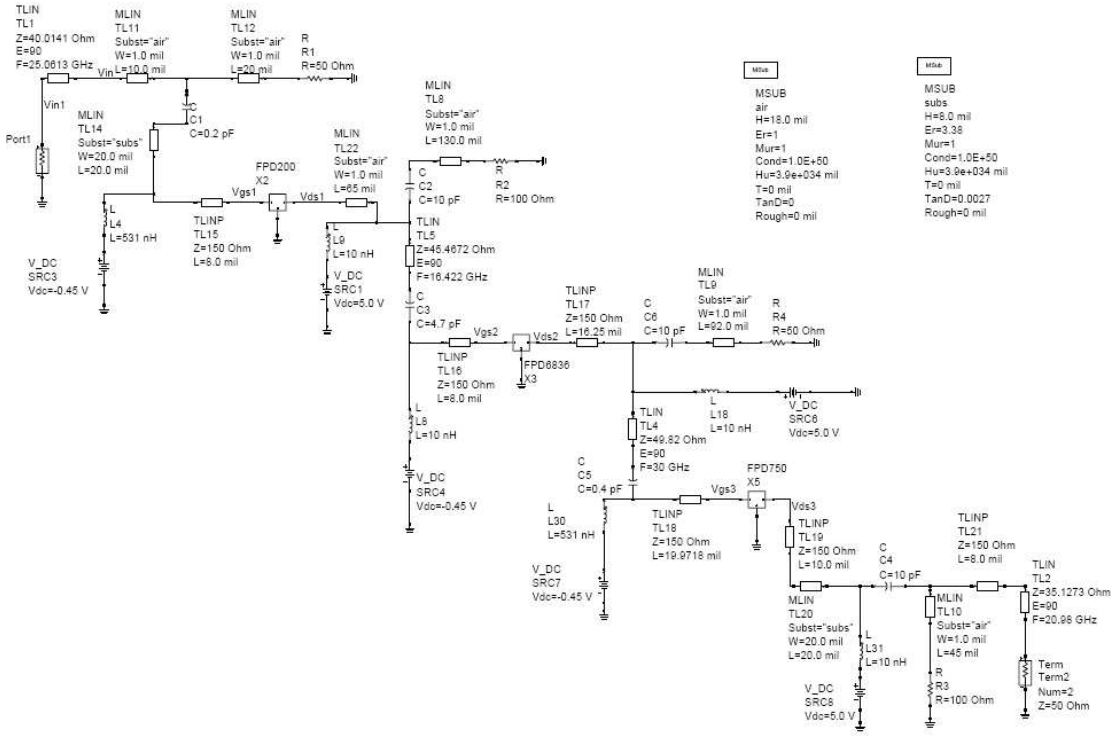

Figure 4.14 Schematic of The Second CRTSSDA

Inductors seen in Figure 4.14 are realized by wire bonds. The required lengths of the bonds are estimated using (4-1). The wire bonds representing the inductors are simulated as transmission lines in the simulations. The values and their corresponding wire lengths of the transmission lines representing the inductors of Figure 4.14 are given in Table 4-4.

Table 4-4 Transmission Lines Representing Inductors and Corresponding Bond Wire Lengths

Transmission Line	Value (nH)	Length (mm)
TL_8	2.6	3.3
TL_9	1.84	2.3
TL_{10}	0.9	1.14
TL_{11}	0.2	0.25
TL_{12}	0.4	0.5

The capacitors used in the second fabrication are parallel plate capacitors of surface area 254um x 254 um as in the first fabrication.

The transmission lines included for matching circuits are realized as microstrip lines as in the first fabrication. Their dimensions are calculated on Ansoft Designer. The calculated dimensions of the microstrip lines are given in Table 4-5

Table 4-5 Estimated Dimensions For Transmission Lines in Figure 4.4

	Impedance(Ω)	Frequency @ E=90°	Width(mm)	Length(mm)
TL_1	40.01	22.06 GHz	0.635	1.8
TL_2	35.12	20.98 GHz	0.776	2.13
TL_4	49.82	30.00 GHz	0.46	1.52
TL_5	45.47	16.42 GHz	0.52	2.78

Layout of the second amplifier is designed considering the wire bond lengths representing the necessary inductors, the pads left for mounting capacitors and microstrip lines. The positions of the biasing coils are also considered to minimize the RF path to the DC biasing sources. The layout is formed and the PCB is fabricated. Via holes on PCB are spread so as to achieve good grounding especially at high frequencies. After the PCB is fabricated, it is plated with gold in order to allow wire bonding in clean room. The fabricated PCB is given in Figure 4.15

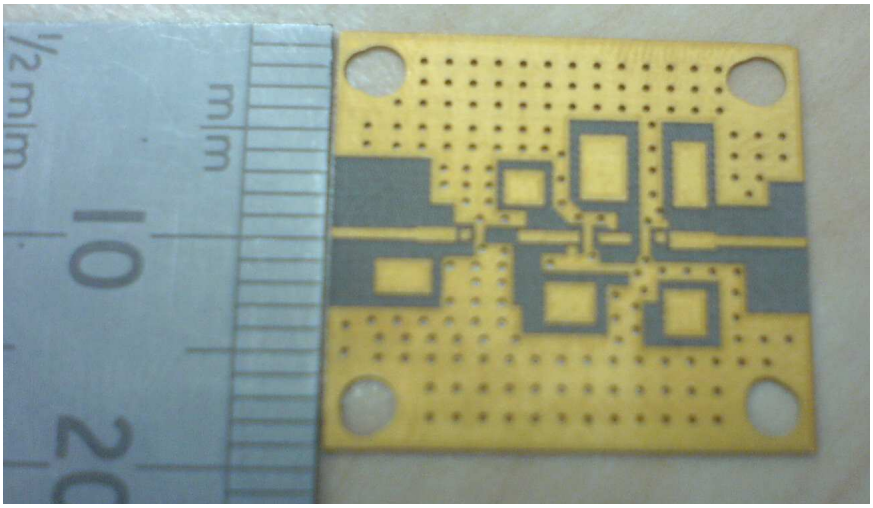

Figure 4.15 Layout of The Second CRTSSDA

The components are assembled on PCB in accordance of the fabrication techniques mentioned in the previous sections. The fabricated circuit is given in Figure 4.16

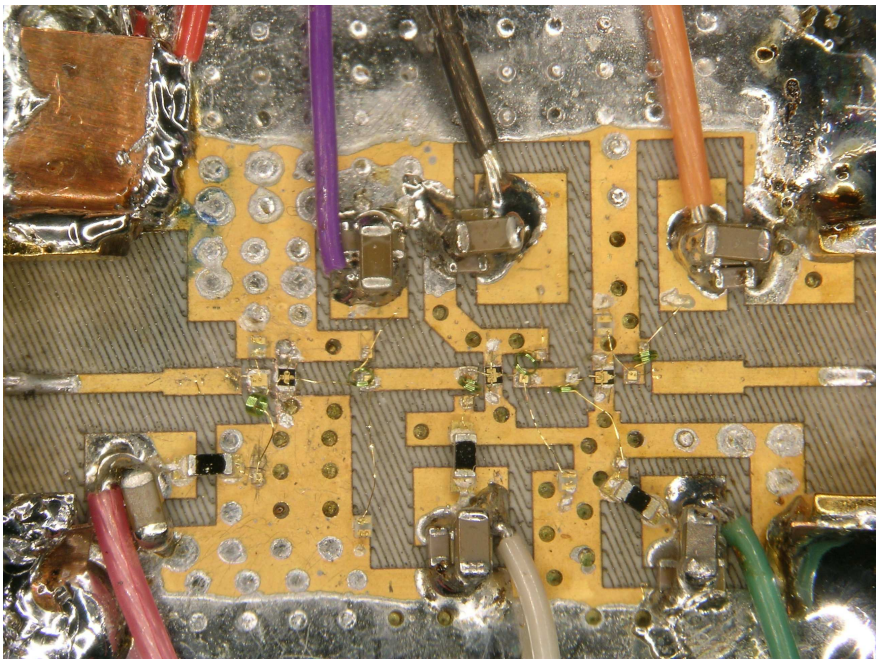

Figure 4.16 Fabricated Circuit of The Second CRTSSDA

4.7 Measurements of the Second Amplifier

The fabricated amplifier given in Figure 4.16 is measured. As in the measurement of the first amplifier, there are observed low frequency oscillations. In addition to the oscillations that exist for f < 200MHz there is also an oscillation at f = 340 MHz in the second amplifier. In order to eliminate the oscillations, 402 packaged resistors are included as in the first trial. The same values of resistors are included in the bias circuits of the transistors. Those values were given in Table 4-3. Applying the resistors and the bias circuit given in Figure 4.7 eliminated the oscillations for f<200 MHz; however, the oscillation at f = 340 MHz was still alive. In order to eliminate this oscillation, a 4.7 uF capacitor is added to the biasing circuit given in Figure 4.7. Addition of this capacitor eliminated the remaining oscillation. The final biasing circuit for the gate of the first stage is given in Figure 4.17

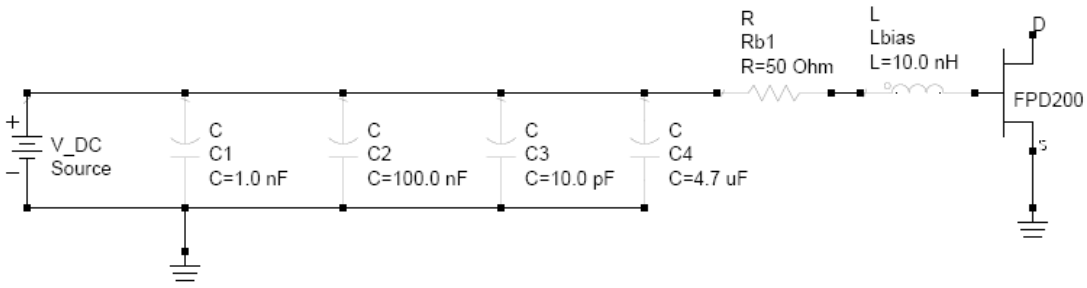

Figure 4.17 Gate Biasing of the First Stage of the 2nd CRTSSDA

Gate biasing of the remaining stages are the same of the first stage except the value of R_{b1} of Figure 4.17. The values of R_{b1} change for each stage according to Table 4-3.

There are not observed any in-band oscillations as in the first amplifier. Therefore, biasing inductors L_{bias} of Figure 4.17 are all 10 nH for each stage. Biasing sources must be isolated from RF path. In order to isolate DC sources from RF path biasing coils are used. The electrical length from RF path to the body of the biasing coil must

be minimized since the RF signal should see an open circuit right on the RF path through the bias path.

The transistors are biased with the appropriate order as mentioned in section 4.3. The biasing voltage and current values of each transistor are given in Table 4-1. The result of s-parameter measurements of the second amplifier is given in Figure 4.18.

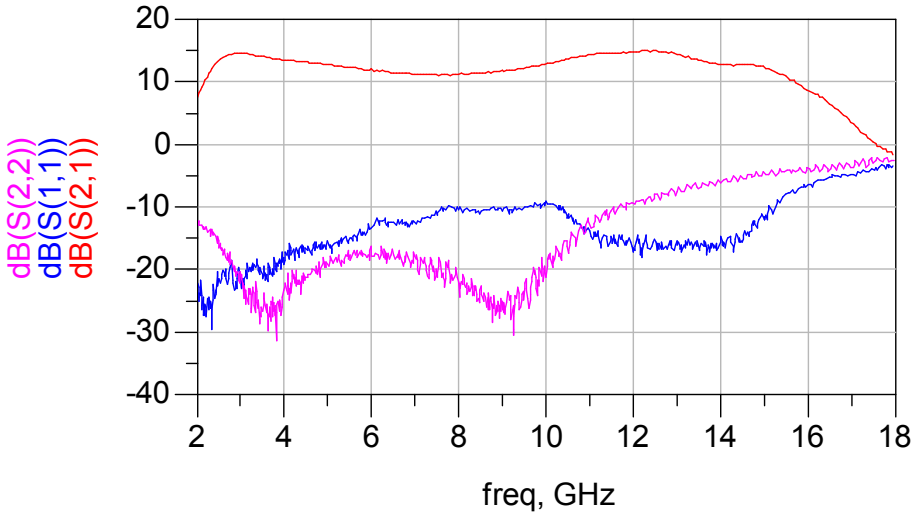

Figure 4.18 S-Parameters of the 2nd CRTSSDA Before Tunings

Figure 4.18 show that the secondly fabricated amplifier needs tunings to improve input return loss and gain flatness. The input return loss in Figure 4.18 is not acceptable for f > 15 GHz. The simulated amplifier has a gain of 23 ± 1.5 dB; however, the gain of the fabricated amplifier is 11.5 ± 3 dB from Figure 4.18 for $2 < f < 16$ GHz.

During measurements of the firstly fabricated amplifier, it is observed that soldering a copper plate between the RF connector's ground and PCB's ground improves input return loss. Based on this experience, four pieces of copper plates soldered to the RF connectors and the PCB. The red circles in Figure 4.19 show the soldered copper plates to improve grounding.

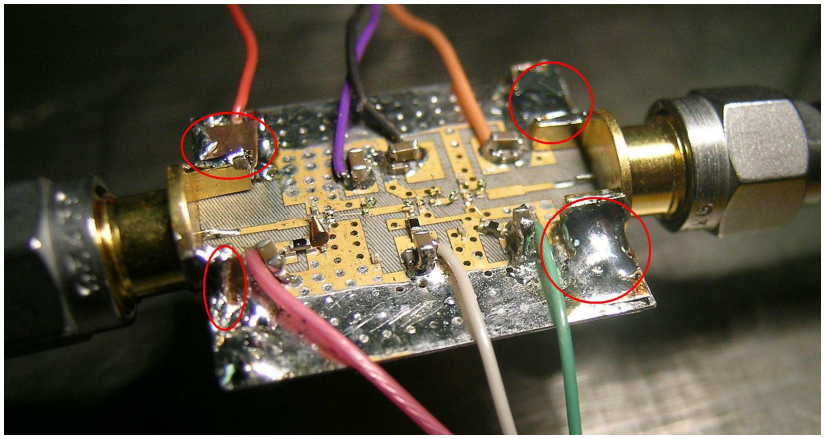

Figure 4.19 Copper Plates Soldered to Improve Grounding

The effect of including copper plates is shown in Figure 4.20. Additional tunings are applied to the inductors realized by wire bonds at the input. These two wire bonds are shown in Figure 4.14 as TL_{11} and TL_{12}. Comparison of the gains of the first measurement and the measurement after tuning is given in Figure 4.21.

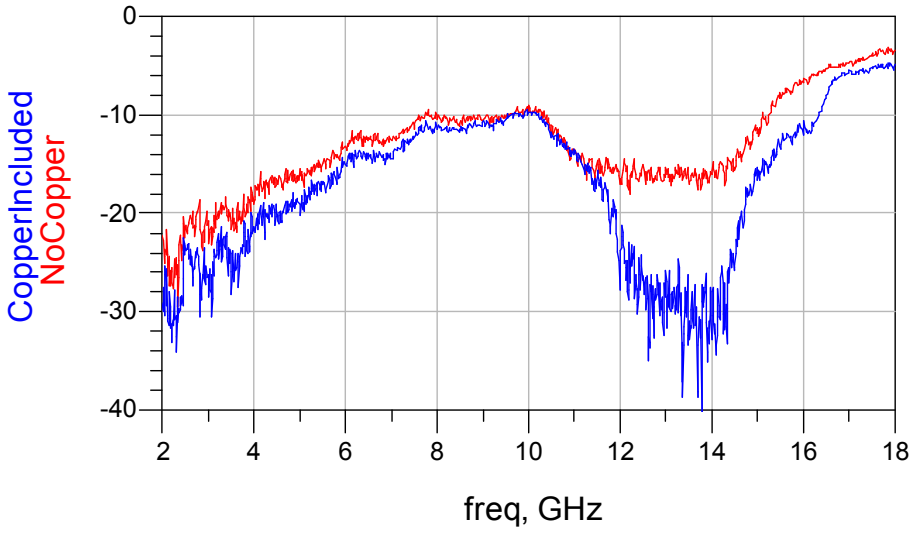

Figure 4.20 Effects of Including Copper Paltes on Input Return Loss

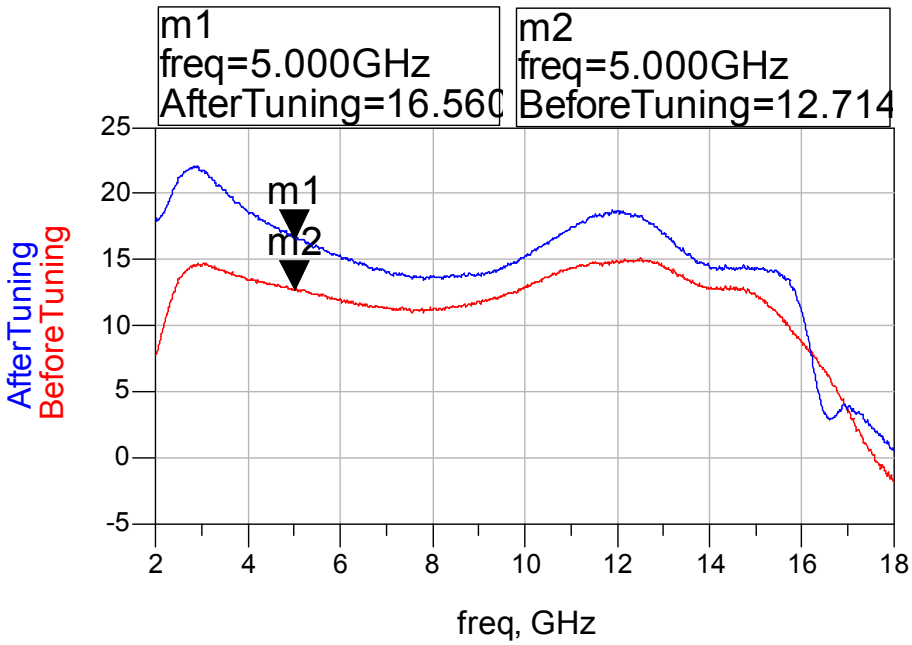

Figure 4.21 Gain of the Second CRTSSDA Before and After First Tuning

Tunings on TL_{11} and TL_{12} of Figure 4.14 results an increase in gain of 3.8 dB at f = 5 GHz. However, although the gain after tuning is higher than the first measurement, gain flatness of the tuned amplifier is worse than the flatness of the first measurement. In addition, the amplifier still does not operate in 2-18 GHz frequency band.

Tuning on the wire bonds at the input is not enough to provide the expected response. Therefore, additional tunings are carried on the remaining wire bonds representing the inductors. These tunings are performed to achieve a better gain flatness across the operating band, to widen the upper operating frequency from 16 GHz to 18 GHz and to achieve a VSWR < 2.00.

Tunings are performed by bending the wire bonds or changing their lengths. Bending wire bonds is achieved by a probe with a needle attached at front end. Electrostatic discharge precautions are held to prevent any damage to the transistors during tunings. Since the diameter of the wire bonds is 25 um, an intense attention must be

paid while bending the bonds, in order not to break off them. The final response of the amplifier after tunings is given in Figure 4.22.

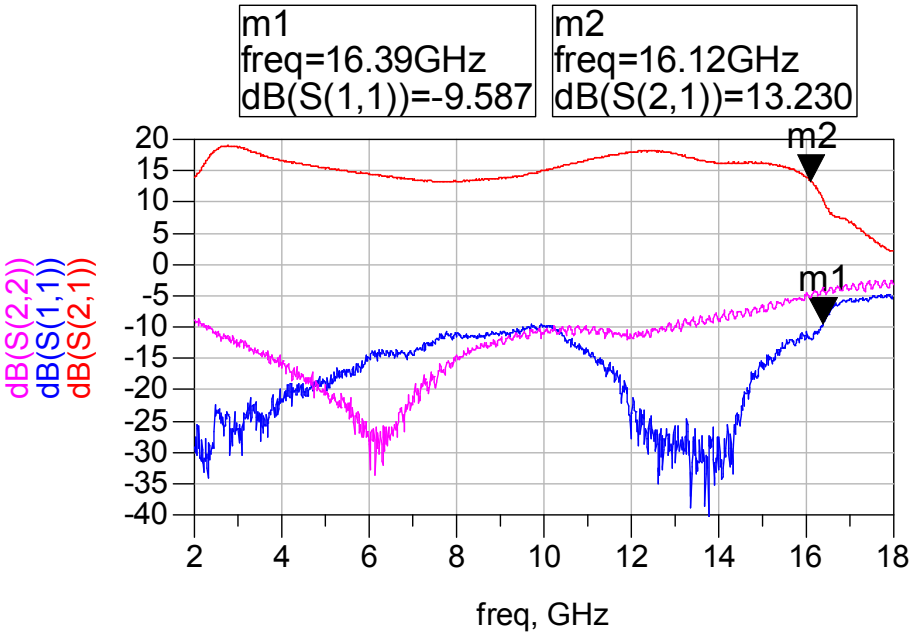

Figure 4.22 Final Response of the Second CRTSSDA After All Tunings

Figure 4.22 shows that VSWR < 2.0 is achieved up to 16.12 GHz. Input return loss for 16.12 < f < 18 GHz is worse than the simulated results.

Gain of the measured amplifier is 15.5 ± 3.5 dB as seen in Figure 4.22. However, the aimed gain is 23 ± 1.5 dB as seen in Figure 3.13. Tunings on the fabricated amplifier increased the gain form 11.5 dB to 15.5 dB. However, the fabricated amplifier still does not match with the simulated amplifier.

The comparisons of responses between the simulated and fabricated amplifiers of second trial are given in Figure 4.23 and Figure 4.24.

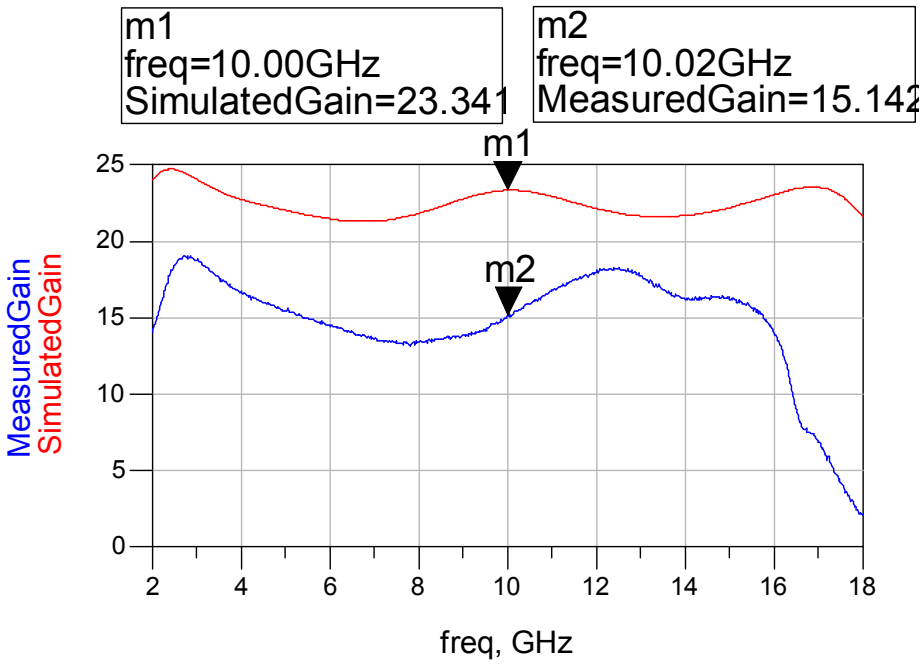

Figure 4.23 Comparison of Gains Between Simulated And Measured Amplifier

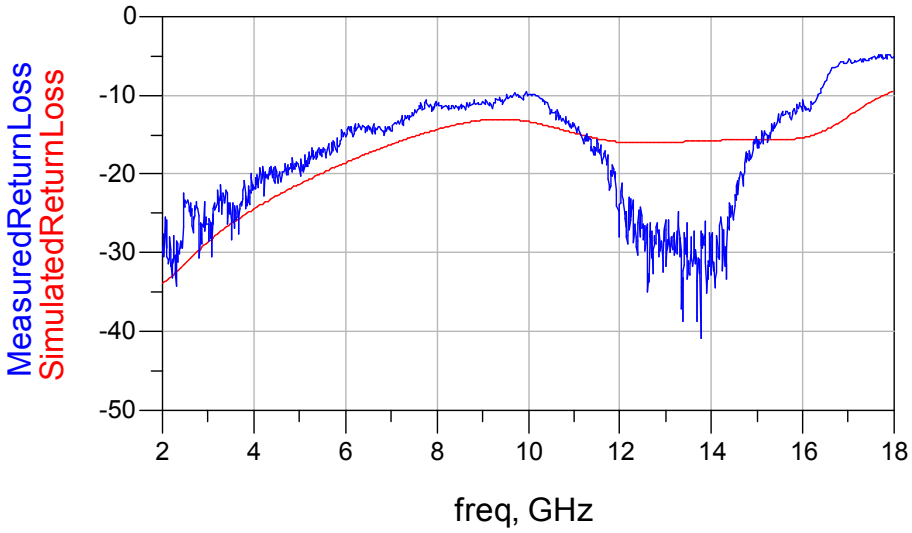

Figure 4.24 Comparison of Input Return Loss Between Simulated And Measured Amplifier

4.8 Comparisons between the Fabricated Amplifiers

In this thesis work, two amplifiers both in CRTSSDA topology are designed and fabricated. The first amplifier is fabricated on Roger4350 where the second amplifier is fabricated on Rogers4003 substrate. Layout and measurement experience of the first amplifier is used on the second trial.

Figure 4.25 and Figure 4.26 show the comparisons between first and second trial in terms of gain and input return losses.

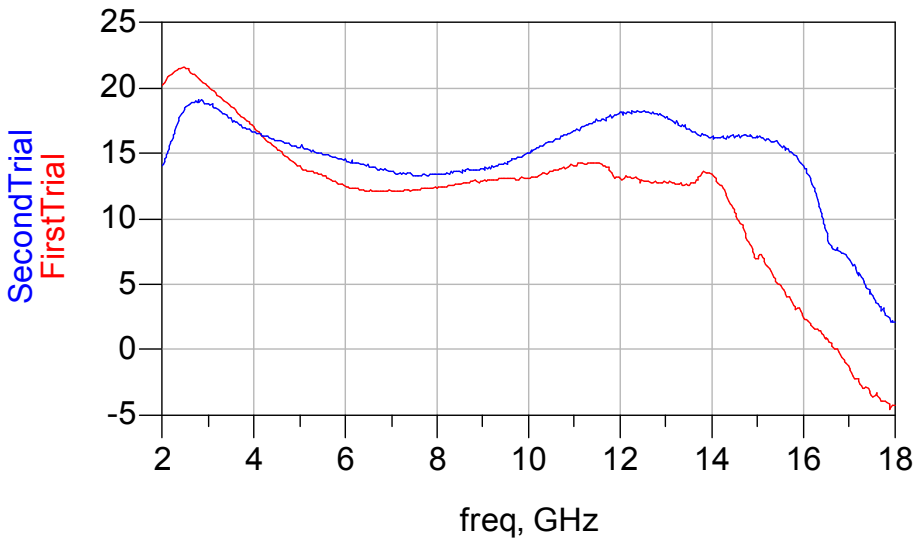

Figure 4.25 Comparison of Gains of First and Second Fabrications

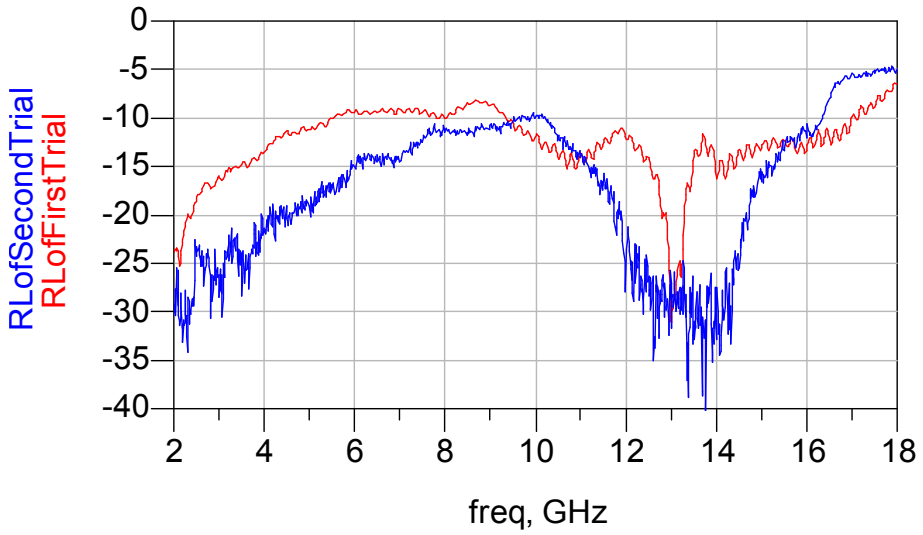

Figure 4.26 Comparison of Input Return Losses of First and Second Fabrications

It is observed from Figure 4.25 that, operating frequency band of the second amplifier is wider than the first trial. The first amplifier operates up to 14 GHz where the second amplifier operates to 16 GHz.

It is also observed from Figure 4.25 that the decrease in gain between 2-6 GHz of the first amplifier is eliminated in the second trial. Eliminating the gain roll off for 2-6 GHz is achieved by including additional layout constraints and effects of the wire bonds in the second simulation which are not taken into consideration in the first trial. Therefore, gain flatness of the second amplifier is better than the first.

The input return losses of the amplifiers are compared in Figure 4.26. The input return loss of the second amplifier is better than the first amplifier for $2 < f < 16$ GHz. In the range of $2 < f < 16$ GHz VSWR of the second amplifier is better than 2.0. However, for $16 < f < 18$ GHz, the first amplifier possess a better input return loss than the second amplifier.

CHAPTER 5

CONCLUSIONS

In this thesis work, cascaded, reactively terminated, single stage distributed amplifier (CRTSSDA) operating in 2-18 GHz frequency band with 23 $\pm$ 1.5 dB gain is designed, simulated and fabricated. The designed amplifier is a 3-stage CRTSSDA comprising of FPD200, FPD6836 and FPD750 DPHEMT transistors. Reactive terminations are included to achieve broadband gain and matching in the circuit.

CRTSSDA circuit technique is superior to traveling wave distributed amplifiers because of its higher gain with equal number of stages. In a TWA design, it is essential to equate the phase velocities of gate and drain lines. Any mismatch of phase velocities in gate or drain will result a decrease in gain. Also, attenuations caused by gate and drain lines restrict high gains from TWAs. CRTSSDA circuit technique overcomes these deficiencies by cascading the transistors. Cascading transistors removes the requirement for equating phase velocities in any stage; therefore it is easier to design a CRTSSDA. Gain of a CRTSSDA is substantially higher than TWA since gate and drain line attenuations are minimized by cascading transistors.

Unfortunately, a transistor's 6dB/octave gain roll-off caused by its intrinsic properties is added at each stage which results a 54dB gain roll-off for a three octave three stage CRTSSDA amplifier. This gain roll-off is the major problem for a CRTSSDA to be solved. As the name implies, a CRTSSDA amplifier includes reactive terminations. The reason for including reactive terminations is to overcome the mentioned gain roll-off. Reactive terminations are constructed by a series resistor and an inductor with appropriate values which is parallel to the gate-to-source capacitance of the transistor. Reactive termination enhances the voltage swing across the gate-to-source capacitance of the transistor. Therefore, gain roll-off is eliminated

by adjusting voltage swing across the gate-to-source capacitance of the transistor by the reactive terminations.

In addition, reactive terminations help broadband matching. In a distributed amplifier concept, gate and drain capacitances and inductances are absorbed in artificial transmission lines. Together with the artificial lines and biasing components, reactive terminations provide broadband matching by their frequency dependent impedances.

Realization of an amplifier is as crucial as designing it on a robust theory. In the fabrication process of a broadband amplifier, there are several constraints that should be taken into consideration. These constraints may be listed as the fabrication method, type of the substrate used, the components' non ideal behaviors and additional layout effects that are not included in simulations.

The designed amplifier is fabricated in ASELSAN Inc. facilities. Circuits operating at high frequencies are usually realized in MMIC technology; however, the components used in this thesis are surface mount components. The aim of fabricating the designed amplifier in this thesis work is not only to realize the theory of a CRTSSDA but also to prove that high frequency applications can be implemented by surface mount components in hybrid circuits. The fabrication process of this thesis shows that not only the theory must be robust, but also the success of fabrication technique and assembling experience is important.

Since the amplifier is designed to work up to 18 GHz, the substrate used for microstrip medium must be suitable for high frequency applications. Another restrictive factor for selecting the type of the substrate is the technology used in fabrication. The designed amplifiers are realized on Rogers 4003 and Rogers 4350 substrates in this thesis work. These two dielectrics can be used up to 18 GHz because of their low attenuations at high frequencies. Their other advantage is that the dielectric constants of these two substrates do not change dramatically with increasing temperature.

The higher height of the substrate means the higher attenuation at high frequencies. The dielectric height of Rogers 4350 used in the first fabrication is 0.254 mm where Rogers 4003 used in the second trial is 0.2 mm in height. Via holes on the board are drilled at a distance from each other that is less than the one tent of the wavelength. Via holes are copper plated for providing successful grounding at every single point on the board. After edging the patterns of the designed amplifier, the board is plated with gold to make wire bonding available.

Components used in the simulations are usually ideal. Unfortunately, in spite of using non-ideal components in simulations, the responses usually do not match with the measurement results exactly. Additional layout pads or wire bonds that are not noticed at simulations affect the responses dramatically. The secondly designed amplifier of this thesis study is based on the experience gained throughout the first fabrication. A wider band for gain is obtained in the second measurement by taking layout constraints into attention.

The gain measured is 8 dB less than the simulated gain in both of the designs. Connectors assembled on the fabricated amplifiers add extra losses which are not included in simulations. One connector at input and the other at the output increases the loss especially at high frequencies. The effects of wire bonds are included as inductances in the simulations. Wire bonds included in the circuit also cause mismatches which degrade gain. The substrates used have low attenuations but they also cause loss in the expected gain.

To sum up, CRTSSDA circuit technique is successful in designing broadband amplifiers, having higher gain than conventional TWAs. Circuits can be realized with surface mount components at higher frequencies if the fabrication technique is well established.

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APPENDIX A

A.1 TriQuint TOM3 Scalable Nonlinear FET Model

Filtronic's DPHEMT transistors FPD200, FPD750 and FPD6836 are modeled by TOM3 models in ADS. TOM3 models used in ADS are charge-based models. The parameters that belong to the transistors are substituted in the model parameters. The following sections give the parameters of the transistors used in the design with schematic of each transistor including parasitic.

In order to have an insight of the model, description of TOM3 model parameters are given in Table A-1, Table A-2 and Table A-3 [18].

Table A-1 TOM3 Model Parameters [18]

Name	Description	Units	Default
NFET	N-channel type		YES
PFET	P-channel type		NO
Tnom	model temperature at which all parameters were derived	deg C	25
Ugw	gate width to which model parameters are normalized	m	1.0e-6
Ngf	number of gate fingers to which model parameters are normalized		1
Vto†	threshold voltage	V	-2.0
Alpha†	saturation parameter in Ids equation	1/V	3.0
Beta†, †††	transconductance parameter in Ids equation	A/V^Q	0.05
Lambda	channel length modulation / output conductance	1/V	0
Gamma†	coefficient for pinch-off change with respect to Vds		0.1
Q	power generalizing the square-law for Ids current		2.0
K	knee function power law coefficient		3.0
Vst†	subthreshold slope voltage	V	0.05
Mst†	parameter for subthreshold slope voltage dependence on Vds	1/V	0
Ilk†††	reverse leakage saturation current - diode models	A	0.1e-6

† Parameter value varies with temperature based on model Tnom and device Temp.
†† Parameter value scales inversely with area.
††† Parameter value scales with area.
‡ Total gate resistance is Rg + Rgmet.

Table A-2 TOM3 Model Parameters-Continued [18]

Name	Description	Units	Default
Plk	reverse leakage reference voltage - diode models	V	2.25
Kgamma	feedback coefficient for the internal VCVS		0.33
Taugd	series Ctau-Rtau time constant (implicit definition of Rtau)	sec	1.0e-9
Ctau	dispersion model capacitance	F	1.0e-15
Qgql†††	low-power gate charge nonlinear term coefficient	C	0.2e-12
Qgqh†††	high-power gate charge nonlinear term coefficient	C	0.1e-12
Qgi0†††	reference current in high-power gate charge nonlinear Ids term	A	0.1e-3
Qgag	low-power gate charge nonlinear term exponential coefficient	1/V	0.75
Qgad	low-power gate charge nonlinear term exponential Vds coefficient	1/V	0.65
Qggb††	transition coefficient for combined low-high power charge	1/W	3.0
Qgcl†††	low-power gate charge linear terms coefficient	F	0.1e-12
Qgsh†††	high-power gate charge linear Vgsi term coefficient	F	0.2e-12
Qgdh†††	high-power gate charge linear Vgdi term coefficient	F	0.1e-12
Qgg0†††	combined low-high power additional linear terms coefficient	F	0
Capmod	capacitance model: 1 – bias-dependent capacitances, 2 – charge		2
Cds†††	drain-source capacitance	F	0
Tau	transit time under gate	sec	0
Rd†, ††	drain ohmic resistance	ohm	0
Rdtc	temperature linear coefficient for Rd	1/deg C	0
Rg‡	gate resistance	ohm	0
Rgmet‡	gate metal resistance	ohm	0
Rs†, ††	source ohmic resistance	ohm	0
Rstc	temperature linear coefficient for Rs	1/deg C	0
Is†, †††	saturation current in forward gate current diode models	A	1.0e-12

† Parameter value varies with temperature based on model Tnom and device Temp.
†† Parameter value scales inversely with area.
††† Parameter value scales with area.
‡ Total gate resistance is Rg + Rgmet.

Table A-3 TOM3 Model Parameters-Continued [18]

Name	Description	Units	Default
Eta	emission coefficient for gate diode models		1.25
Alphatce	temperature exponential coefficient for Alpha	1/deg C	0
Gammatc	temperature linear coefficient for Gamma	1/deg C	0
Msttc	temperature linear coefficient for Mst	1/(V deg C)	0
Vsttc	temperature linear coefficient for Vst	V/deg C	0
Vtotc	temperature linear coefficient for Vto	V/deg C	0
Betatce	temperature exponential coefficient for Beta	1/deg C	0
Xti	temperature exponent for saturation current		2.5
Eg	energy gap for temperature effect on Is	eV	1.11
Imax	explosion current	A	1.6
Fnc	flicker noise corner frequency	Hz	0
R	gate noise coefficient		0.5
P	drain noise coefficient		1.0
C	gate-drain noise correlation coefficient		0.9
Kf	flicker noise coefficient		0
Af	flicker noise exponent		1
Ffe	flicker noise frequency exponent		1
wVgfwd	gate junction forward bias warning	V	
wBvgs	gate-source reverse breakdown voltage warning	V	
wBvgd	gate-drain reverse breakdown voltage warning	V	
wBvds	drain-source breakdown voltage warning	V	
wIdsmax	maximum drain-source current warning	A	
wPmax	maximum power dissipation warning	W	
AllParams	DataAccessComponent for file-based model parameter values		

† Parameter value varies with temperature based on model Tnom and device Temp.
†† Parameter value scales inversely with area.
††† Parameter value scales with area.
‡ Total gate resistance is Rg + Rgmet.

A.2 TOM3 Model of FPD200

The schematic of the TOM3 model with external parasitic of FPD200 is shown in Figure A.1.

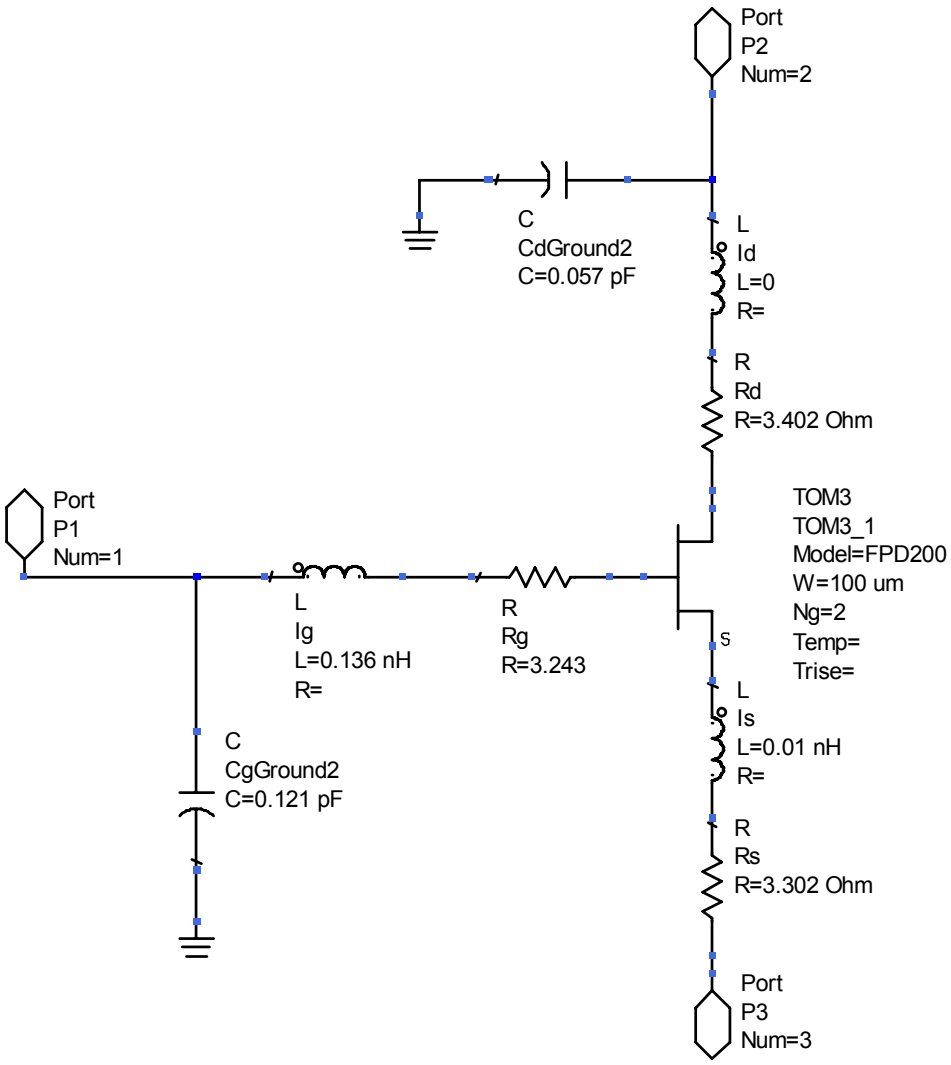

Figure A.1 TOM3 Model with External Parasitic of FPD200

The components included in the schematic of TOM3 model of FPD200 are the parasitic elements of the transistor in die form.

TOM3 parameters are extracted to model the device over a wide range of operating conditions. The TOM3 parameters of FPD200 are given in Table A-4 [19].

Table A-4 TOM3 Model Parameters of FPD200 [19]

VTO	-0.6471 V	QGG0	1.227E-16
ALPHA	3.053	CDS	0.000234
BETA	0.000682	IS	1E-11 mA
LAMBDA	-0.02432	EG	0.8 V
GAMMA	0.03358	N	1
Q	0.9352	XTI	2
K	4.279	TAU	0.001 ns
VST	0.05677	VBI	1 V
MST	0.2041	TAU_GD	1000 ns
ILK	1.8E-6 mA	KGAMMA	0.01194
PLK	1.5 V	RG	*0.01*Ω
QGQH	7.349E-16	RGSH	0Ω
QGSH	8.451E-16	RD	0.01Ω
QGDH	2.073E-17	RS	0.01Ω
QGIO	2.002E-6	LS	0 nH
QGQL	8.58E-16	LG	0 nH
QGAG	2.21	LD	0 nH
QGAD	2.241	NG	2
QGCL	7.715E-17	W	100
QGGB	144.55		

A.3 TOM3 Model of FPD6836

The schematic of the TOM3 model with external parasitic of FPD6836 is shown in Figure A.2.

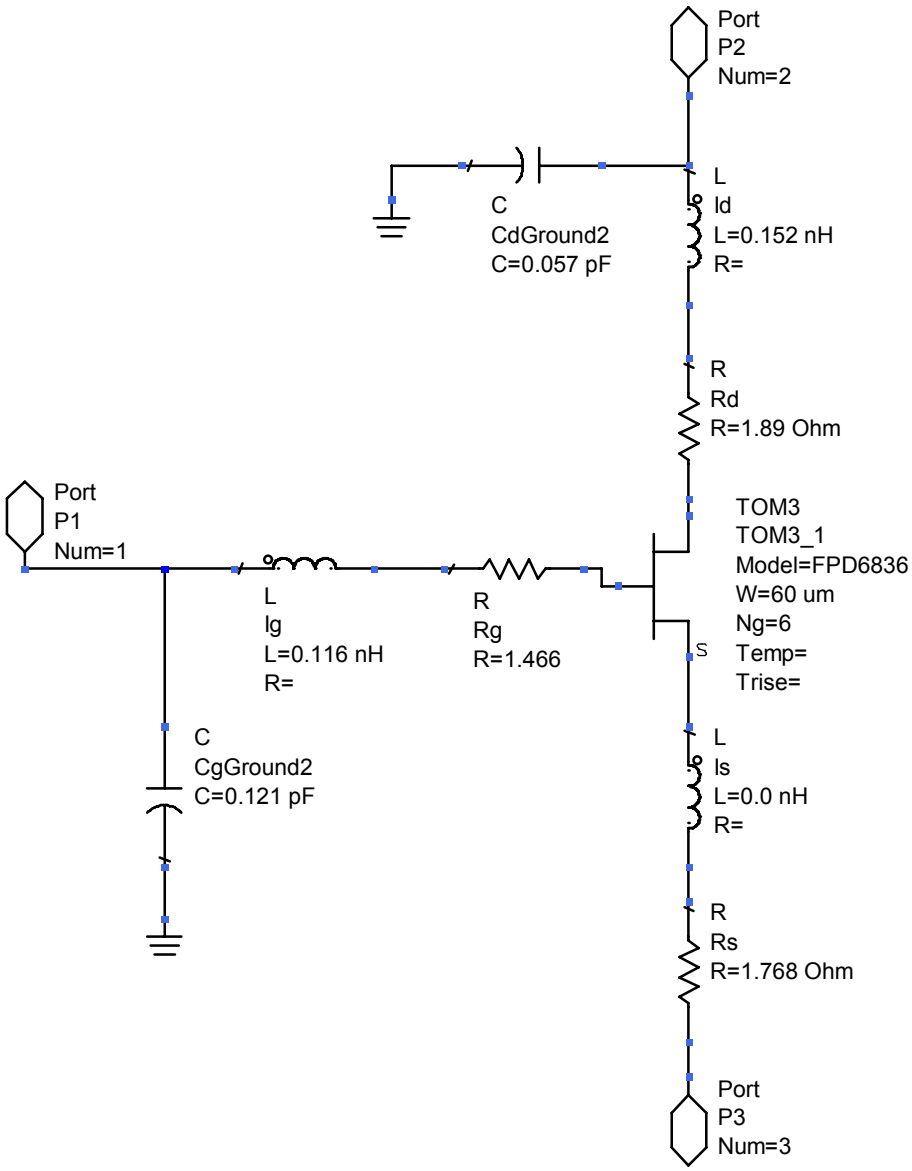

Figure A.2 TOM3 Model with External Parasitic of FPD6836

The TOM3 parameters of FPD6836 are given in Table A-5 [20].

Table A-5 TOM3 Model Parameters of FPD6836 [20]

VTO	-0.6448 V	QGG0	1.50476E-16
ALPHA	1.83566	CDS	0.000276 pF
BETA	0.0005841	IS	1E-11 mA
LAMBDA	-0.01603	EG	0.8 V
GAMMA	0.03528	N	1
Q	0.788782	XTI	2
K	4.15391	TAU	0.001 ns
VST	0.03797	VBI	1 V
MST	0.212655	TAU_GD	1000 ns
ILK	1.8E-6 mA	KGAMMA	0.01364
PLK	1.5 V	RG	*0.01*Ω
QGQH	8.9603E-16	RGSH	0Ω
QGSH	8.2027E-16	RD	0.01Ω
QGDH	1.0396E-17	RS	0.01Ω
QGIO	2.00161E-6	LS	0 nH
QGQL	9.1063E-16	LG	0 nH
QGAG	2.30006	LD	0 nH
QGAD	2.11351	NG	6
QGCL	7.9467E-17	W	60
QGGB	144.459		

A.4 TOM3 Model of FPD750

The schematic of the TOM3 model with external parasitic of FPD750 is shown in Figure A.3.

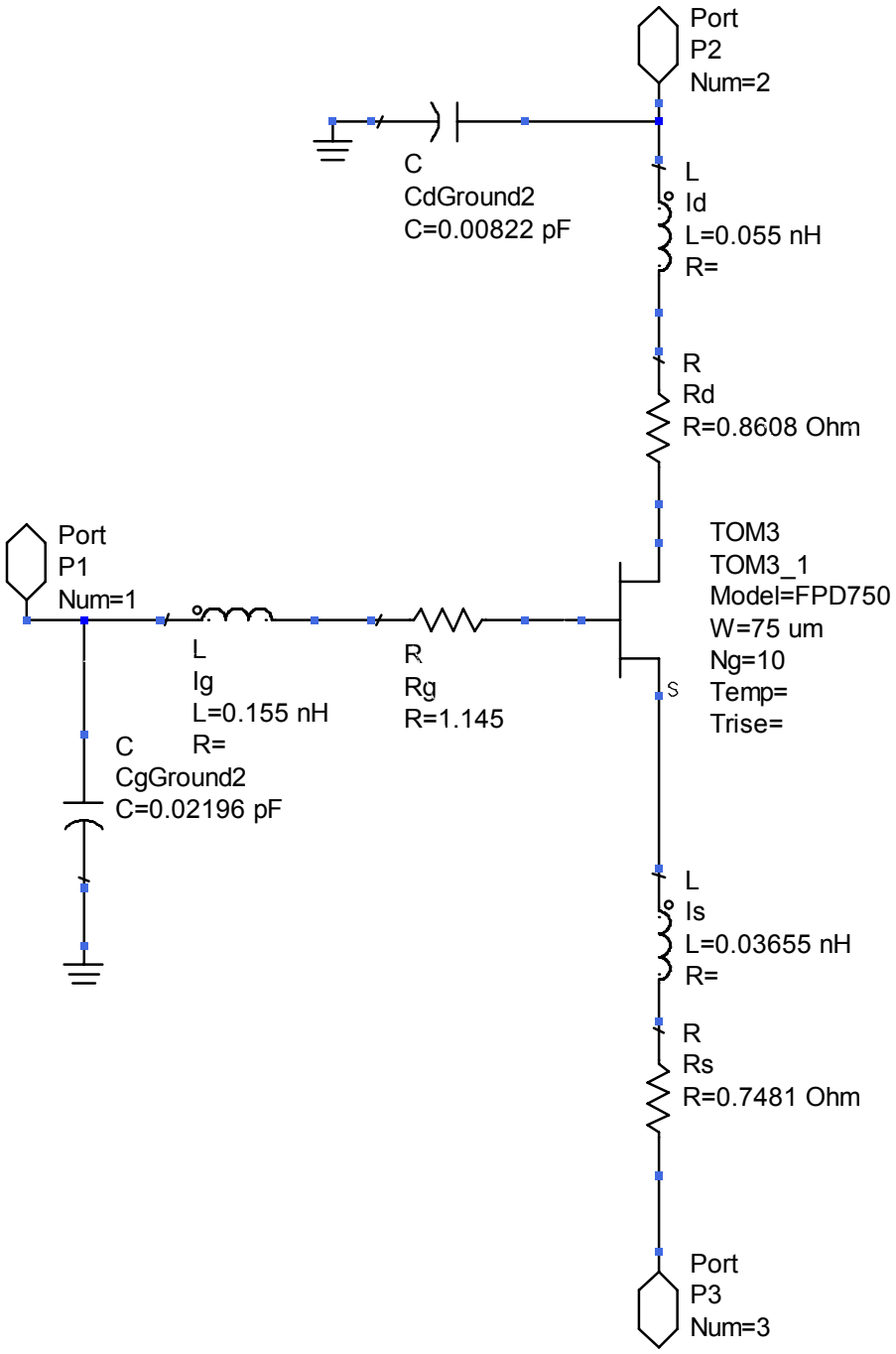

Figure A.3 TOM3 Model with External Parasitic of FPD750

The TOM3 parameters of FPD750 are given in Table A-6 [21].

Table A-6 TOM3 Model Parameters of FPD750 [21]

VTO	-0.85 V	QGG0	1.936E-16
ALPHA	5.5	CDS	0.000234 pF
BETA	0.00062	IS	1E-11 mA
LAMBDA	-0.051	EG	0.8 V
GAMMA	0.064	N	1
Q	1.09	XTI	2
K	3.178	TAU	0.00117 ns
VST	0.02	VBI	1 V
MST	0.01	TAU_GD	1000 ns
ILK	1.8E-6 mA	KGAMMA	0.023
PLK	1.5 V	RG	0.01 Ω
QGQH	4.001E-16	RGSH	0 Ω
QGSH	4.785E-17	RD	0.01 Ω
QGDH	1.143E-16	RS	0.01 Ω
QGIO	1.075E-6	LS	0 nH
QGQL	1.929E-15	LG	0 nH
QGAG	1.264	LD	0 nH
QGAD	1.512	NG	10
QGCL	2.359E-17	W	75
QGGB	470.044		