# A SWITCH MODE POWER SUPPLY FOR PRODUCING HALF WAVE SINE OUTPUT

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**A SWITCH MODE POWER SUPPLY FOR PRODUCING HALF WAVE SINE OUTPUT**

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# ABSTRACT

## A SWITCH MODE POWER SUPPLY FOR PRODUCING HALF WAVE SINE OUTPUT

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In this thesis; analysis, design and implementation of a DC-DC converter with active clamp forward topology is presented. The main objective of this thesis is generating a rectified sinusoidal voltage at the output of the converter. This is accomplished by changing the reference signal of the converter. The converter output is applied to an inverter circuit in order to obtain sinusoidal waveform. The zero crossing points of the converter is detected and the inverter drive signals are generated in order to obtain sinusoidal waveform from the output of the converter. Next, the operation of the DC-DC converter and sinusoidal output inverter coupled performance is investigated with resistive and inductive loads to find out how the proposed topology performs. The design is implemented with an experimental set-up and steady state and dynamic performance of the designed power supply is tested. Finally an evaluation of how better performance can be obtained from this kind of arrangement to obtain a sinusoidal output inverted is thoroughly discussed.

Keywords: Pure Sinusoidal voltage waveform, active clamp forward converter, rectified DC-link.

# ÖZ

## DOĞRUTULMUŞ YARI DALGA SİNÜS ÇIKIŞ ÜRETEN ANAHTARLAMALI GÜÇ KAYNAĞI

Kaya, İbrahim
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Bu tez çalışmasında “active clamp forwad converter” topolojisinde bir anahtarlamalı güç kaynağı tasarlanarak, laboratuar ortamında çalıştırılmıştır. Tezin temel amacı, tasarlanan çeviricinin çıkışında doğrultulmuş sinusoidal dalga şekli elde etmektir. Bu dalga şekli çeviricinin referans sinyali değiştirilerek elde edilmiştir. Çevirici çıkışına, evirici devresi eklenerek doğrultulmuş sinus dalgasından tam bir sinus dalgası elde edilmiştir. Ardından, önerilen topolojinin performansını görmek amacıyla, çevirici ve evirici katları doğrusal ve indüktif yükler ile çalıştırılarak deneyler yapılmıştır. Son olarak, benzer bir yapının kullanımı ile elde edilebilinecek sinüs çıkışlı evirici topolojisinin performansının iyileştirilmesi için neler yapılabileceği tartışılmıştır. Bu kapsamda yeni bir güç kaynağı topolojisi önerilmiştir.

Anahtar Kelimeler: Saf sinüs dalga şekli, active clamp forward DC-DC çevirici, Doğrultulmuş Doğru Akım Barası.

To My Wife

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I would like to express my deepest gratitude to my supervisor Prof. Dr. H. Bülent ERTAN for his guidance, advice, criticism, encouragements and insight throughout the research.

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| | |
|---|---|
| SMPS | : Switch Mode Power Supply |
| $V_{IN}$ | : Input Voltage of the Converter |
| $V_{IN}$ | : Output Voltage of the Converter |
| Np | : Primary Turns Number |
| Np | : Secondary Turns Number |
| D | : Duty Ratio |
| $V_{DS}$ | : Drain to Source Voltage |
| $V_{CE}$ | : Collector to Emitter Voltage |
| RCD | : Resistor Capacitor Diode |
| $V_{INMIN}$ | : Minimum Input Voltage |
| $V_{INMAX}$ | : Maximum Input Voltage |
| EMI | : Electromagnetic Interference |
| RFI | : Radio Frequency Interference |
| $I_{PR}$ | : Primary Current |
| $I_{SC}$ | : Secondary Current |
| $V_{CR}$ | : Clamp Voltage |
| $C_{CR}$ | : Clamp capacitor |
| $C_{IN}$ | : Input Capacitor |
| $C_{OUT}$ | : Output Capacitor |
| Lo | : Output Inductor |
| $L_{MAG}$ | : Magnetizing Inductor |
| $A_C$ | : Magnetic Cross-section Area of the Core |
| Wa | : Window Area |
| $\phi$ | : Magnetic Flux |
| B | : Magnetic Flux Density |
| H | : Magnetic Field Density |
| Ts | : Switching Period |
| fs | : Switching Frequency |
| $\Delta B$ | : Flux Density Swing |
| $I_{RMS}$ | : RMS Current |
| Ipeak | : Peak Current |
| Jrms | : RMS Current Density |

$A_{CU}$ : Copper Cross Sectional Area

Ku : Window Utilization Factor

$P_{IN}$ : Input Power

$P_{OUT}$ : Output power

AL : Inductance Factor

$I_D$ : Drain Current

$I_C$ : Collector Current

$I_L$ : Load Current

$I_{MAG}$ : Magnetizing Current

UPF : Unity Power Factor

# CHAPTER 1

# INTRODUCTION

## 1.1 Purpose

In variable-speed ac drives which utilize voltage-fed inverters, control of the voltage and frequency output of the inverter feeding the ac motor is essential for torque and speed control of the motor. Similarly, in ac power supplies, which utilize uninterruptible power supplies, again control of the output voltage and frequency of the supply feeding the load is essential for supplying regulated voltage to the load without any distortion. Various PWM strategies have been introduced for controlling inverters. The common principle in all these strategies is to introduce notches in the basic square-wave pole voltage, such that the resulting periodic waveform has the desired fundamental frequency and amplitude. In the PWM techniques, some drawbacks occur with the increasing frequency levels. The switches in the inverter are rapidly switched and are either turned hard ON or OFF with no in between state. The result is that the sine wave current is generated if the load is inductive by using pulse width modulated switching. However, the voltage wave form is a series of pulses in the output of the inverter, and the voltage transitions are very rapid. This rapid switching causes a voltage waveform with a very high dv/dt (rate of change in voltage). This high dv/dt causes high EMI problems, reduced life expectancy of the motor and additional losses.

In reference [1], a novel approach for generating power level sinusoidal waveforms is proposed. The basic structure is a DC-DC converter that produces a rectified DC-link at its output and an H-bridge inverter that inverts the rectified sinusoids to form a sinusoidal voltage (see Figure 1.1). Main advantages of the circuit are that the H-bridge inverter switches have no switching stresses, they are switched at low frequency so the reliability is increased.

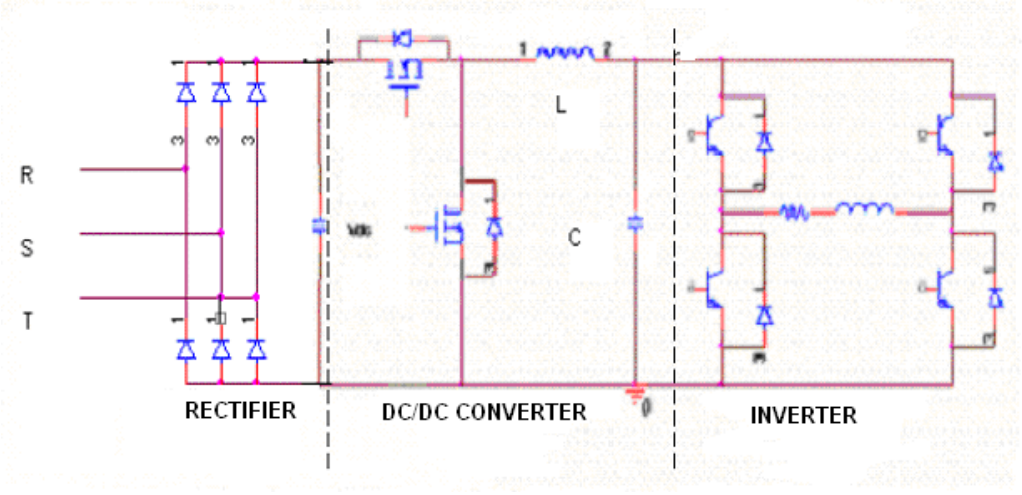



**Figure 1.1: Inverter Topology Proposed in [1]**

The drawbacks of the topology proposed in [1] are its lack of isolation and having non-sinusoidal input current. In this thesis, an alternative isolated DC to DC converter with half wave rectified sinusoidal output voltage will be investigated. Main specification of this converter is given in Table 1.1. At this stage, only operation with resistive load will be considered.

**Table 1.1: Main Specifications of the SMPS**

| Specification | Minimum | Maximum |
|---|---|---|
| Input Voltage Range | 200 VAC rms | 240 VAC rms |
| Input Voltage Frequency | 50 Hz | |
| Output Voltage Range | 0 | 240 VAC rms |
| Output Frequency Range | 10 Hz | 100 Hz |
| Output Power | 0 | 1500 Watts |

Block diagram of the SMPS topology is given in Figure 1.2 It has three power stages: a bridge rectifier, a DC to DC converter and an inverter. Bridge rectifier stage rectifies AC input voltage, DC-DC converter generates rectified sinusoidal voltage waveform and inverter converts the rectified sinusoidal voltage to AC voltage. In this topology, the most challenging stage is the DC converter stage. Output regulation and dynamic response of the overall SMPS is performed by this stage. Also, isolation between input and output stages is achieved by this stage.

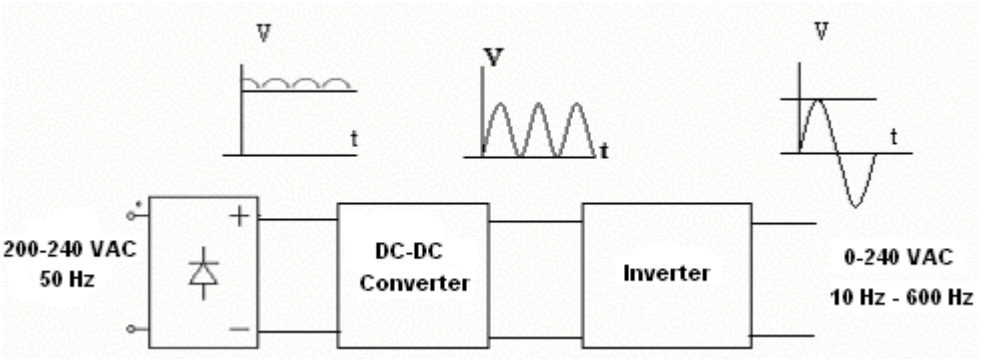



**Figure 1.2: SMPS Topology**

## 1.2 Topology Selection

In this section, different isolated DC-DC converter topologies will be investigated. Investigated topologies will be compared. The comparison criteria is lower cost. Here, with low cost we mean lower power device ratings, small transformer and capacitor sizes. There are four common configurations for isolated DC-DC converters.

### 1.2.1 Flyback Converter

In flyback converter (see Figure1.3), transformer acts as an energy storage device during the converter operating cycle. First energy is stored in the transformer, then transferred to the output over diode D1.

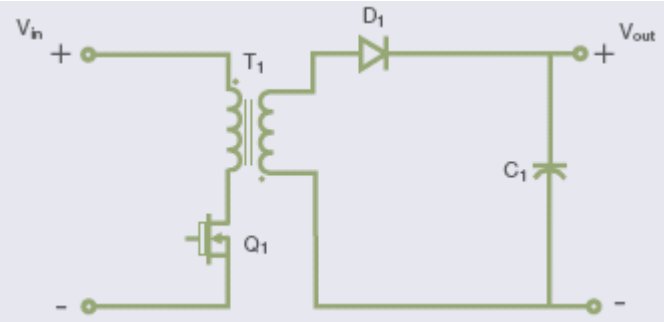



**Figure 1.3: Flyback Converter**

In Flyback converter, output voltage expression is given in Equation 9.1 [3]. Ns and Np are primary and seconsary turn numbers. D is the duty cycle.

$$V_{OUT} = V_{IN} \cdot \frac{Ns}{Np} \cdot \frac{D}{1-D} \qquad (1.1)$$

Voltage stress of the transistor is given in Equation 1.2 [3].

$$V_{CE} = V_{IN} + \frac{Np}{Ns} \cdot V_{OUT} \tag{1.2}$$

We can merge Equations 1.1 and 1.2 into the following equation:

$$V_{CE} = \frac{V_{IN}}{1 - D} \tag{1.3}$$

For D=0.5 then transistor voltage stress is $V_{CE}=2V_{IN}$.

Voltage stress of the fast diode is given in Equation 1.4 [3].

$$V_D = V_{OUT} + V_{IN} \cdot \frac{Ns}{Np} \tag{1.4}$$

By combining equation 1.1 and 1.4 we can obtain the diode voltage stress:

$$V_D = \frac{V_{OUT}}{D} \tag{1.5}$$

For D=0.5 then transistor voltage stress is $V_D=2V_{OUT}$.

Peak transistor current is given in Equation 1.6.

$$I_{peak} = \frac{2}{D} \cdot \frac{P_{IN}}{V_{IN}} \tag{1.6}$$

In reference [9], power transfer capacity coefficient of the flyback transformer is given as TC=0.62 where TC=1 is the power transfer capacity coefficient of the push pull converter. This means, by using the same core, a flyback transformer transfers 0.62W energy while a push-pull type transformer transfers 1W energy. We can define the core size coefficient as 1/TC where TC is the energy transfer capacity coefficient. Then core size coefficient of the flyback transformer is 1.62.

As core size increases, its cost increases. Then this core size coefficient can be seen as relative cost of the transformer core. Most flyback converters are designed for applications of less than 100 W [4]. Device ratings and relative transformer size criteria are given in the comparison Table 1.2. By applying a half wave rectified sinusoidal reference signal, it is possible with flyback converter to obtain a half wave rectified sinusoidal output voltage.

### 1.2.2 Forward Converter

The simplest form of the forward converter is shown in Figure 1.4. It is a direct converter, so the energy from the input to output is transferred during the on time of the switch device. During this time, secondary diode D2 is reverse biased and current flows to the load through the secondary inductor. During the switch off time, the transformer primary voltage reverses polarity due to the change in primary current. This forces the transformer secondary to also reverse polarity. Secondary diode D2 becomes forward biased, and conducts current through the load driven by the stored energy in the output filter inductor. The simple topology shown in the diagram is not practical for power levels above 200 W [3]. Device ratings and relative transformer size criteria are given in the comparison Table 1.2. By applying a half wave rectified sinusoidal reference signal, it is possible with forward converter to obtain a half wave rectified sinusoidal output voltage.

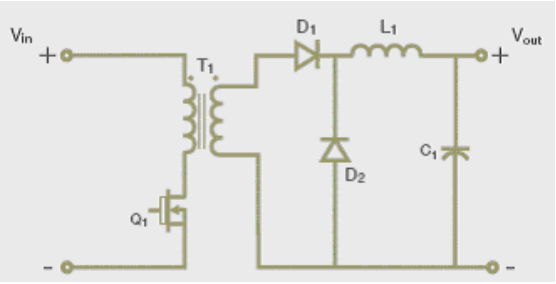



**Figure 1.4: Forward Converter**

### 1.2.3 Half-Bridge Converter

Half bridge topology is given in Figure 1.5. A voltage level of half the input voltage is generated by the two stacked capacitors on the input. The transformer primary is alternatively switched from this voltage to either input voltage or input return, so that the transformer primary voltage is half of the input voltage. Maximum voltage stresses of the transistors are equal to the input voltage. Expression for the output voltage is given in Equation (1.7).

$$V_{OUT} = V_{IN} \cdot \frac{Ns}{Np} \cdot D \qquad (1.7)$$

Peak transistor current can be given as

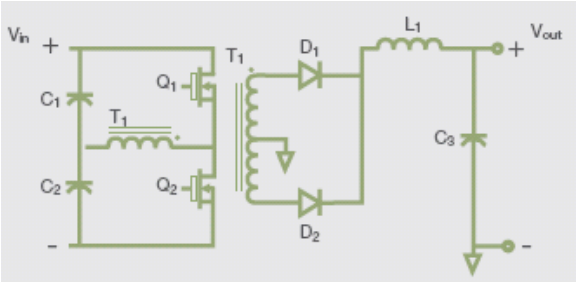



**Figure 1.5: Half Bridge Converter**

$$I_{peak} = \frac{1}{D} \cdot \frac{P_{IN}}{V_{IN}} \qquad (1.8)$$

Voltage stress of the fast diode is obtained form the following equation:

$$V_D = V_{IN} \cdot \frac{Ns}{Np} \qquad (1.9)$$

Equation 9.9 can be rewritten by using Equation 1.7:

$$V_D = \frac{V_{OUT}}{D} \qquad (1.10)$$

Device ratings and relative transformer size criteria are given in the comparison Table 1.2. By applying a half wave rectified sinusoidal reference signal, it is possible with half bridge converter to obtain a half wave rectified sinusoidal output voltage.

### 1.2.4 Full-Bridge Converter

The full bridge topology is given in Figure 1.6. In this topology, diagonally opposite switches are simultaneously turned on and input voltage is applied to the transformer primary side. Voltage stresses of the transistors are equal to the input voltage. Expression for the output voltage is given in Equation (1.11) [7].

$$V_{OUT} = 2 \cdot V_{IN} \cdot \frac{Ns}{Np} \cdot D \qquad (1.11)$$

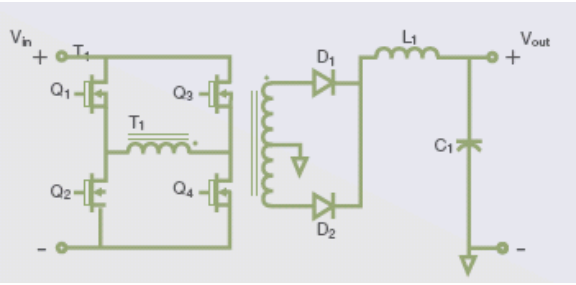



**Figure 1.6: Full Bridge Converter**

Peak transistor current is given in Equation 1.12. [7]

$$I_{peak} = \frac{1}{2 \cdot D} \cdot \frac{P_{IN}}{V_{IN}} \tag{1.12}$$

Voltage stress of the fast diode is obtained form the following equation:

$$V_D = 2 \cdot V_{IN} \cdot \frac{Ns}{Np} \tag{1.13}$$

Equation 9.13 can be rewritten by using Equation 1.11 [7]:

$$V_D = \frac{V_{OUT}}{D} \tag{1.14}$$

At a given power level, the primary current and switch current is half that of the half bridge due to the higher primary voltage. This makes the full bridge suitable for higher power levels. It is perhaps the most common topology for converters in the 400 to 2000 W power ranges [2]. Device ratings and relative transformer size criteria are given in the comparison Table 1.2. By applying a half wave rectified sinusoidal reference signal, it is possible with full bridge converter to obtain a half wave rectified sinusoidal output voltage.

### 1.2.5 Comparison of the Converter Topologies

In Table 1.2, device ratings and relative transformer sizes of the investigated topologies are given. Note that, we have defined lower cost as lower devices ratings and lower transformer size. According to this definition and Table 1.2, it is seen that full bridge converter topology is the lowest cost topology.

**Table 1.2: Topology Comparison**

| **Parameters** | **Flyback** | **Forward** | **Half Bridge** | **Full Bridge** |
|---|---|---|---|---|
| Transistor Voltage Rating for D=0.5 | 2 x $V_{IN}$ | 2 x $V_{IN}$ | $V_{IN}$ | $V_{IN}$ |
| Transistor Peak Current for D=0.5 | 4 x $P_{IN}$ / $V_{IN}$ | 2x $P_{IN}$ / $V_{IN}$ | 2x $P_{IN}$ / $V_{IN}$ | $P_{IN}$ / $V_{IN}$ |
| Diode Voltage Rating for D=0.5 | 2 x $V_{OUT}$ | 2 x $V_{OUT}$ | 2 x $V_{OUT}$ | 2 x $V_{OUT}$ |
| Transformer Relative Core Size | 1.62 | 1.40 | 1.00 | 1.00 |
| Power Limit | 100 W | 200W | 500W | 2000W |
| Half Wave Rectified Sinus Output | Possible | Possible | Possible | Possible |

In this thesis, forward converter topology is selected. In chapter 2, analysis of the forward converter topology is presented. Expressions used in the design are derived.

In chapter 3, design of the converter stage is presented. In this chapter, a forward converter with half wave rectified sinusoidal output voltage is designed. The designed converter is simulated to verify the design. Then implementation of the converter is explained. Finally, tests of the implemented converter are presented.

In chapter 4, operation of the converter with inverter stage is investigated. Simulations are performed in order to investigate the operation of the power supply with resistive, inductive and capacitive loads. Implementation of the inverter stage is also explained in this chapter.

In chapter 5, the results of the experiments are given. Experiments are performed for resistive and inductive loads. Problems observed in the experiments are discussed in this chapter.

In chapter 6, alternative topologies are investigated in order to solve the problems of the implemented topology. An alternative topology is proposed in this chapter. Implemented and proposed SMPS topologies are compared with the conventional PWM inverter topologies. Finally, conclusion of the thesis is presented in this chapter.

# CHAPTER 2

# ANALYSIS OF THE FORWARD CONVERTER

## 2.1 Introduction

The purpose of this chapter is deriving the main design expressions of the forward converter topology. The derived expressions will be used in the next chapter.

## 2.2 Basic Forward Converter Operation

Basic operation theory of the forward converter was given in the previous chapter in section 1.2.2. Input output voltage relationship of the forward converter is given by equation (2.1). [4]

$$V_{OUT} = V_{IN} \cdot \frac{N_S}{N_P} \cdot D \qquad (2.1)$$

Here, $V_{IN}$ is the input; $V_{OUT}$ is the output voltage of the converter. $N_P$ and $N_S$ are the number of primary and secondary turns of the transformer, respectively. D is the duty ratio of the main switch.

The problem with the operation of the circuit in Figure 1.4 is that, only positive voltage is applied across the core, thus flux can only increase with the application of the input voltage. The flux will increase until the core saturates when the magnetizing current increases significantly and circuit failure occurs. The transformer can only sustain operation when there is no significant DC

component to the input voltage. While the switch is ON there is positive voltage across the core and the flux increases. When the switch turns OFF, we need to reset the core flux. Following reset methods can be used for this purpose:

- Reset Winding Method
- RCD Type Reset Method
- Active Clamp Method

### 2.2.1 Reset Winding Method

Forward converter with reset winding is given in Figure 2.1. A separate "reset" winding was incorporated in the main transformer to provide a convenient route for clamping the reset voltage amplitude to the input supply source. Almost all the magnetization energy that was stored in the transformer during the switch on time freewheels into the input capacitor through the reset winding when the switch turns off. Reset winding would guarantee proper operation and reset over all line and load conditions. However, a penalty is incurred due entirely to the limited maximum duty cycle. A lower transformer turns ratio results, which translates into a higher primary current than otherwise necessary .Designing for operation over a wide input voltage range exaggerates the difficulty with this approach. Very narrow duty cycles are necessary at higher input voltage to meet the 50% maximum duty cycle clamping at lower input voltage conditions. Operation over a worldwide input voltage span hardly results in an efficient power supply design at any set of line and load conditions since numerous compromises must be considered. It does, however, recycle the energy stored in the transformer's magnetizing inductance back to the primary side input capacitor.[4]

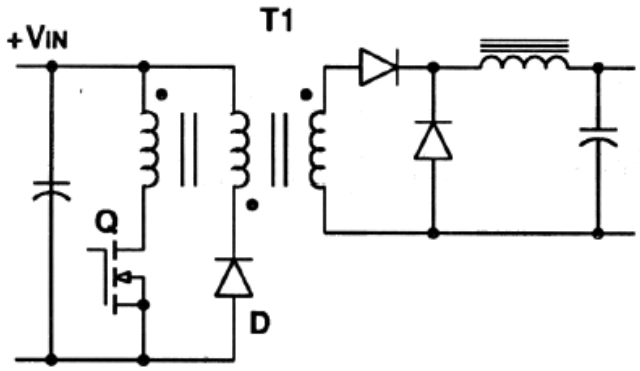



**Figure 2.1: Forward Converter with Reset Winding**

The reset winding usually has the same number of turns as the primary winding and is sometimes eve wound bifilar with it for good coupling. Then, maximum voltage stress of the switch is two times the input voltage.

$$V_{DS} = 2 \cdot V_{IN} \qquad (2.2)$$

In this Equation, VDS is the drain-source voltage of the switching transistor when in is OFF. For MOSFET VDS; for IGBT VCE is used for the voltage stress expression.

### 2.2.2 RCD Type Reset Method

Forward converter with RCD reset circuit is given in Figure 2.2. In the RCD circuit, resistor, capacitor and diode components are used to develop a varying clamp voltage into which the magnetizing energy is dissuasively discharged. Using a high clamp voltage with an amplitude greater than twice the input supply will facilitate maximum duty cycles which can stretch beyond the 50% milestone, particularly useful in wide range input supply designs. There are two penalties to be paid with this adaptation: high voltage stress on the semiconductors and power losses from the resistor in the clamp circuit. Generally, the RCD is the

preferred choice for wide input ranges, especially low voltage input designs where a higher clamp/reset voltage still yields manageable low voltage semiconductors. Transistor voltage stress in RCD reset method is given in Equation 2.3. [4]

$$V_{DS} = V_{IN} + \frac{V_{INMIN} \cdot D_{\max}}{1 - D_{\max}} \qquad (2.3)$$

In this Equation, $V_{DS}$ is the drain-source voltage of the switching transistor when in is OFF. $V_{INMIN}$ is the minimum input voltage. $D_{max}$ is the maximum duty ratio of the switching transistor.

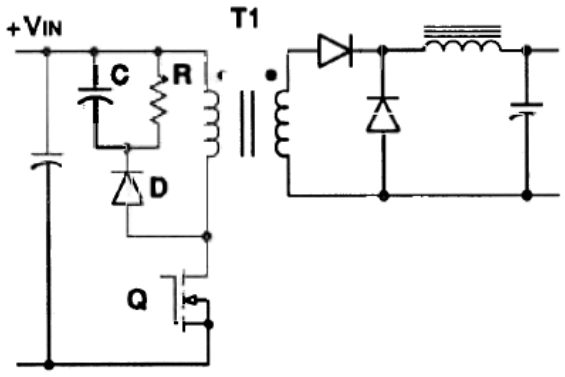



**Figure 2.2: Forward Converter with RCD Type Reset**

### 2.2.3 Active Clamp Method

Forward converter with active clamp is given in Figure 2.3. The diode in the RCD reset circuit given in Figure 2.2 is replaced with an active MOSFET switch. Its first purpose is to clamp the primary to the reset capacitor, just as diode would. A second function, which a standard rectifier is unable to provide, is to allow a controlled (switched) transfer of energy back from the reset capacitor to

the primary side power stage of the converter. Current in the MOSFET switch "channel" is bidirectional during part of its active interval, but is zero during the remainder of the switching cycle. Note that the active clamp and RCD reset techniques are inactive during the normal power transfer portion of the switching cycle, and only operate during the main switch's off-time. For the most part, conventional square wave power conversion waveforms apply to system voltages and currents during the on-time of the main switch. However, significant improvements and differences take place during the low loss clamp, reset and soft alignment of the power switch. Two pivotal benefits are obtained with this new approach: higher efficiency and zero voltage "soft" switching transitions.

In Figure 2.3, two types of active clamp circuit are given: high side and low side clamp. The difference is the clamp capacitor voltage stresses and type of the clamp switches. In high side active clamp, N type MOSFET is used whereas in low type active clamp P type MOSFET is used. In high side clamp, voltage stress on the clamp capacitor is lower [4].

Benefits of the active clamp method are listed below [4]:

- "recycles" transformer magnetizing energy instead of dissipating it in a resistor
- facilitates Zero Voltage Transition of the main switch for higher efficiency
- uses lower voltage MOSFET and diodes compared to the RCD
- reduced EMI/RFI via soft switching
- duty cycles beyond 50% max are obtainable
- actively resets main transformer to third quadrant of BH curve

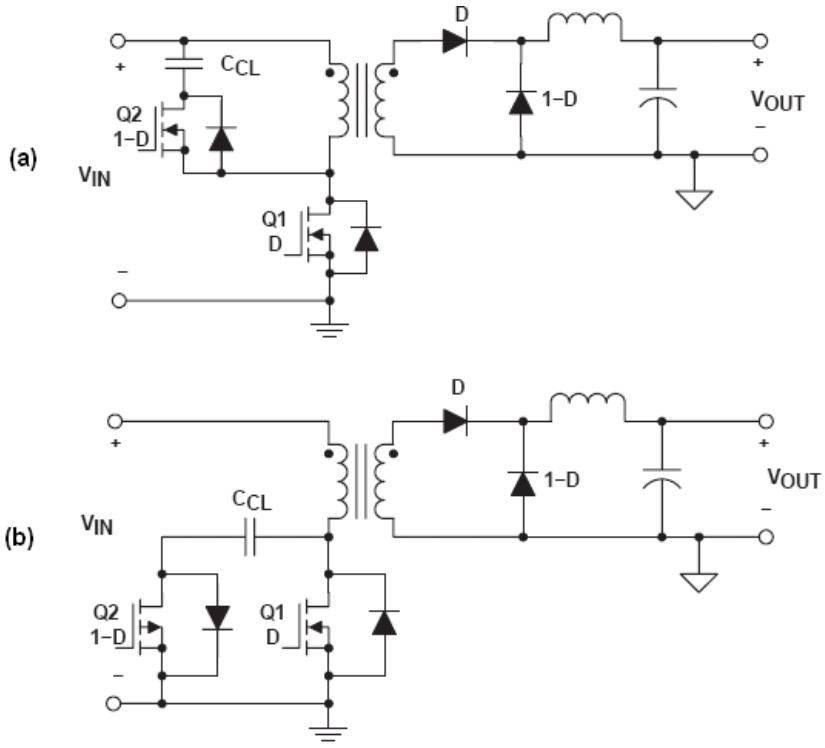



**Figure 2.3: Forward Converter with Active Clamp (a): High Side Clamp (b): Low Side Clamp**

In active clamp forward converter, expression for the transistor voltage stress is given in Equation 2.4 .

$$V_{DS} = \frac{V_{IN}}{1-D} \qquad (2.4)$$

In this Equation, $V_{DS}$ is the drain-source voltage of the switching transistor when in is OFF. $V_{IN}$ is the input voltage. D is the duty ratio of the switching transistor.

One area, which is significantly different between the active clamp method and other methods, is found in the transformer's B-H curve operation. In reset winding and RCD method, the transformer is driven in the first quadrant where both H (ampere- ampere- turns) and B (flux density) are positive. On the other

hand, in active clamp method, since the magnetizing current becomes both positive and negative in a switching cycle, first and third quadrants of the B-H curve are used (see figure 2.4). At lower frequencies or with better core materials where core loss is not the dominant factor, the active reset technique offers the benefit of higher flux density swings. By the operating characteristic just described, the core can now be used at double its first quadrant ability as the total flux density swing encompasses both first and third quadrant operation. Nevertheless, this mode of operation allows reducing the number of turns in each winding by half [4] .

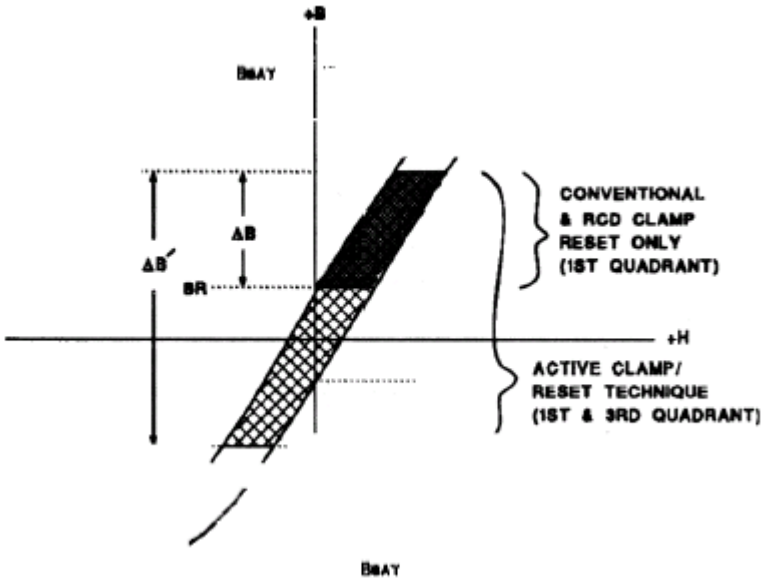



**Figure 2.4: B-H Curve Difference between Active Clamp Method and Other Methods**

### 2.2.4 Selecting the Transformer Reset Method

In reset method selection, the main criterion is the voltage stress of the switch. Since our maximum input voltage is 240 VAC rms, 240x$\sqrt{2}$ =340Vpeak, voltage stress of the switch is very important in transistor selection. If the voltage stress is above 600V level, a 1200V switch would be selected. There are a few choices between 600V and 1200V. In order to reduce the transistor cost, our first objective is obtaining a voltage stress value lower then 600V level.

In reset winding method, according to Equation 2.1, transistor voltage stress is $V_{DS} = 2 \cdot V_{IN}$. In our case, maximum transistor voltage stress will be 680V for maximum input voltage 340V peak. With this method, obtaining a transistor voltage stress lower then 600V level is not possible for our application. Then, reset winding method is eliminated.

In RCD type reset method and active clamp reset method maximum transistor voltage stress is reduced by choosing maximum duty ratio lower then 0.5 (see Equation 2.2 and 2.4). With these methods, obtaining a transistor voltage stress lower then 600V level is possible. Then, we have two choices: RCD reset and active clamp reset method.

RCD clamp method is simpler since it does not need an extra driver circuit. On the other hand, the magnetizing energy dissipated in the resistor decreases the efficiency of the converter. Moreover, with this method only first quadrant of the BH curve of the transformer is used. This results in inefficient use of the transformer. Regarding the converter efficiency and transformer utilization active clamp method is more advantageous. As a result, active clamp reset method is selected in this thesis.

There are two types of active clamp: high side and low side, as mentioned in Appendix A.1. Low side active clamp has advantage of simple transistor driver requirements since the source of the clamp switch is connected to ground.

However, in low side clamp circuit P channel MOSFET switch is used. In out application for voltage levels, such as 600V, there are a few choices for P channel MOSFET. For this reason high side active clamp topology is selected.

Operation theory of active clamp forward converter is given in Appendix A.1

### 2.2.5 Transformer Design

The functions of the power transformer in forward converter are: to transfer power efficiently and instantaneously from input supply to the load, to step down or step up the voltage, and to provide voltage isolation between input supply and the load. In this section transformer design expressions are derived.

First step in transformer design is determining the turns ratio. By rewriting Equation 2.1, we can obtain the following equation which gives the turns ratio expression.

$$N = \frac{N_S}{N_P} = \frac{V_{OUT}}{V_{IN} \cdot D} \qquad (2.5)$$

Next step in transformer design is selecting the core material, geometry and size. E/ETD, EFD and RM/PM cores made of ferrite materials are recommended for forward converter transformer [9]. We need some guidance in making an initial estimate of the appropriate core size One widely used method, with many variations, is based on the core Area Product, obtained by multiplying the core magnetic cross-section area ($A_c$) by the window area ($W_a$) available for the winding. We can derive the area product expression for the forward converter transformer by using Faraday's law of induction [6]:

$$V = N_p \frac{d\phi}{dt} = N_p A_c \frac{dB}{dt} \qquad (2.6)$$

$N_p$ is the turns number of the primary winding. $\phi$ is the magnetic flux, B is the flux density, $A_c$ is the cross sectional area of the core. By integrating Equation (2.6) we have,

$$V \cdot T_{on} = N_p \cdot A_c \cdot \Delta B \qquad (2.7)$$

In this equation, $\Delta$B is the flux density swing; $T_{on}$ is the time duration when the main switch is ON. We can write $T_{on}$ as:

$$T_{on} = \frac{D}{f_s} \qquad (2.8)$$

D is the duty ratio, $f_s$ is the switching frequency of the switch. By using Equation (2.8), we can rewrite equation (2.7) such that:

$$A_c = \frac{V_{IN} \cdot D}{N_p \cdot \Delta B \cdot f_s} \qquad (2.9)$$

Since the input current waveform of the forward converter is square wave its rms value ($I_{in\_rms}$) is written as:

$$I_{in\_rms} = \frac{I_{in\_dc}}{\sqrt{D}} \qquad (2.10)$$

$I_{in\_dc}$ is the average input current, and it can be written as:

$$I_{in\_dc} = \frac{P_{in}}{V_{IN}} \qquad (2.11)$$

Rearranging equations (2.10) and (2.11) gives:

$$I_{in\_rms} = \frac{P_{IN}}{V_{IN} \cdot \sqrt{D}} \qquad (2.12)$$

Input rms current is related to the current density J such that:

$$J = \frac{I_{in\_rms}}{A_{CU}} \tag{2.13}$$

$A_{CU}$ is the cross sectional area of the copper wire used in the primary windings. It is related to the window utilizations factor $K_{u.}$ Window utilization factor is the ratio of the total copper area core window area $W_a$.

$$K_u = \frac{N_p \cdot A_{CU}}{W_a} \tag{2.14}$$

Rearranging equations (2.13) and (2.14) gives:

$$\begin{aligned} Np &= \frac{W_a \cdot K_u}{A_{CU}} \\ &= \frac{W_a \cdot K_u \cdot J}{I_{in\_rms}} \end{aligned} \tag{2.15}$$

In this equation, replacing $I_{in\_rms}$ with equation (2.12) gives:

$$\begin{aligned} N_p &= \frac{W_a \cdot K_u \cdot J}{I_{in\_rms}} \\ N_p &= \frac{W_a \cdot K_u \cdot J \cdot V_{IN} \cdot \sqrt{D}}{P_{IN}} \end{aligned} \tag{2.16}$$

In equation (2.9), replacing $N_p$ with the term in equation (2.16) gives:

$$\begin{aligned} A_c &= \frac{V_{IN} \cdot D}{N_p \cdot \Delta B \cdot f_s} \\ A_c &= \frac{V_{IN} \cdot D}{\Delta B \cdot f_s} \cdot \frac{P_{IN}}{W_a \cdot K_u \cdot J \cdot V_{IN} \cdot \sqrt{D}} \end{aligned} \tag{2.17}$$

Finally, from equation (2.17), we can write the area product expression

$$A_c \cdot W_a = \frac{P_{IN} \cdot \sqrt{D}}{\Delta B \cdot f_s \cdot J \cdot K_u} \qquad (2.18)$$

This equation will be used in the following chapter in order to determine the core size. In equation (2.18):

- $A_c \cdot W_a$ is the area product value in $m^4$.
- $P_{IN}$ is the input power of the converter, in Watts.
- D is the duty ratio of the converter.
- $f_s$ is the switching frequency of the converter, in Hertz.
- J is the rms current density of the winding conductor, in $A/m^2$.
- $K_u$ is the window utilization of the core for primary windings.
- $\Delta B$ is the flux density swing of the core, in Tesla.

Number of primary turns can be calculated from Equation 2.19. This equation is obtained by rewriting equation (2.9).

$$N_p = \frac{V_{IN} \cdot D}{Ac \cdot \Delta B \cdot f_s} \qquad (2.19)$$

As mentioned Appendix A.1, in active camp forward converter transformer, first and third quadrant of the B-H curve. Then, theoretically the maximum value of the flux density swing can be $\Delta B$ = 2x$B_{sat}$, where $B_{sat}$ is the flux density of the core at saturation level. Higher $\Delta B$ value results in lower turns numbers and lower copper losses. However, higher $\Delta B$ value increases core losses. In transformer design an optimization work in $\Delta B$ selection is necessary.

After calculating the number of primary turns, number of secondary turns is calculated from Equation (2.5).

Magnetizing inductance is calculated form the following equation. AL is the inductance factor and given in core datasheet.

$$L_{MAG} = AL \cdot N_p^{\,2} \qquad (2.20)$$

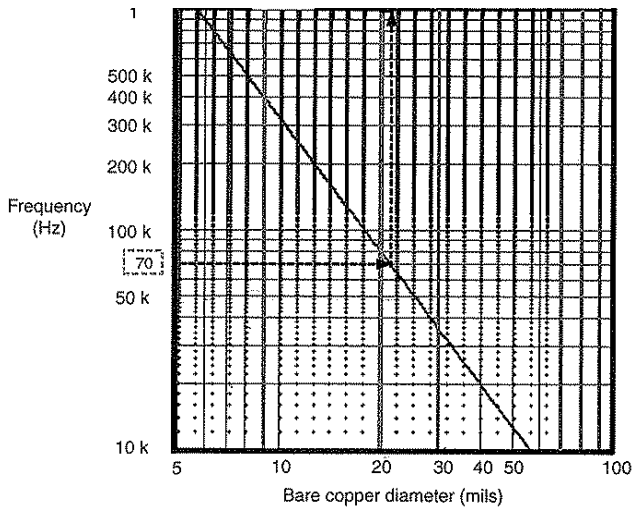



**Figure 2.5: Quick Estimate of Diameter at Different Frequencies**

Next step in transformer design is determining the maximum conductor cross section according to the skin affect. Skin effect is the tendency of an alternating electric current to distribute itself within a conductor so that the current density near the surface of the conductor is greater than that at its core. That is, the electric current tends to flow at the "skin" of the conductor. The skin effect causes the effective resistance of the conductor to increase with the frequency of the current. In order to minimize the conductor resistance at high frequencies, thin conductors should be used. In Figure 2.5, recommended cross sections of the conductors at different frequencies are given. Detail calculations about skin depth can be found in reference [6].

After determining the maximum conductor cross section, numbers of parallel conductors that will carry the rms winding currents are calculated in order to satisfy the current density value used in area product calculations.

### 2.2.6 Main Transistor

In transistor selection, current, voltage and power stresses are main factors that must be considered. In section, voltage stress, peak and rms current expressions of the main transistor are derived. Moreover, expressions for conduction and switching losses will be derived. These equations will be used in the following converter design chapter.

From Figure 2.6, , it can be seen that voltage stress of the main switch is the sum of input voltage and clamp capacitor voltage, that is:

$$V_{CE(QA)} = V_{IN} + V_{CR} \tag{2.21}$$

Clamp capacitor voltage can be found by using the volt seconds law. That is, in square wave power conversion, we always apply a certain voltage to the transformer during the switch ON time, then we automatically get a constant voltage (of opposite sign) during the off time [6]:

$$V_{ON} = L_{MAG} \cdot \frac{\Delta I_{MAG(ON)}}{t_{ON}} \tag{2.22}$$

$$V_{OFF} = L_{MAG} \cdot \frac{\Delta I_{MAG(OFF)}}{t_{OFF}} \tag{2.23}$$

From Figure A.6, it can be seen that $\Delta I_{MAG(ON)} = \Delta I_{MAG(OFF)}$. Also, during the main switch is ON, transformer voltage is $V_{ON}$ = $V_{IN}$ ; during the main switch is OFF, transformer voltage is $V_{OFF}$ = -$V_{CR}$. Then, from equations (2.22) and (2.23), we can write the volts seconds equation:

$$V_{IN} \cdot t_{ON} = V_{CR} \cdot t_{OFF} \quad (2.24)$$

Time interval $t_{ON}$ and $t_{OFF}$ can be written as:

$$t_{ON} = D \cdot T \quad (2.25)$$

$$t_{OFF} = (1 - D) \cdot T \quad (2.26)$$

Where T is the switching period and D is the duty cycle. From Equations (2.24), (2.25) and (2.26), clamp capacitor voltage is obtained:

$$V_{CR} = \frac{D}{1 - D} V_{IN} \quad (2.27)$$

Form equations (2.21) and (2.27) voltage stress of the main switch is obtained as:

$$V_{CE(QA)} = \frac{V_{IN}}{1 - D} \quad (2.28)$$

In order to find the main transistors current stress, we need to consider Figure A.3 and the first mode of operation. That is power transfer mode (Mode-1) given in Appendix-A1. As mentioned, primary current is the sum of reflected output load current, reflected output inductor charging current and primary magnetizing current. It can be seen from Figure A.3, drain current waveform of the main transistor $I_DQ_A$. If we capture main transistor current $I_{D(QA)}$ waveform during the transistor is ON, we obtain the following figure.

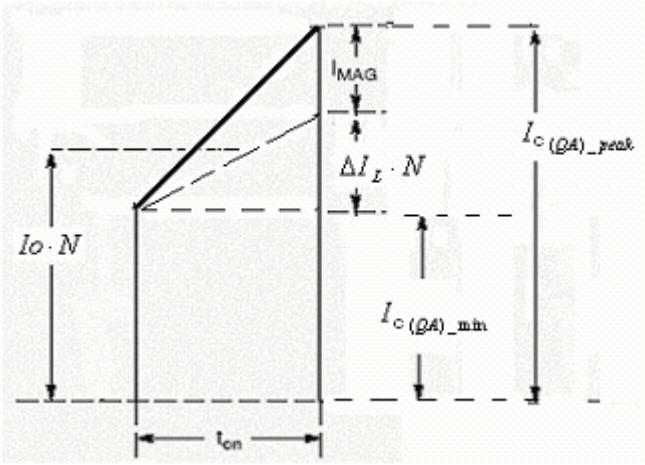



**Figure 2.6: Current Waveform for The main Transistor (Captured From Figure A.6)**

Then, peak transistor current can be expressed by the following equation:

$$I_{C\,(QA)\_\,peak} = Io \cdot N + \frac{\Delta I_L}{2} \cdot N + I_{MAG} \qquad (2.29)$$

In this equation, $Io$ is the output current, N is the turns ratio of the transformer, then $Io \cdot N$ is the reflected output load current. $\Delta I_L$ is the peak to peak current ripple in the output inductor, it will be derived in the following sections. $I_{MAG}$ is the magnetizing current. It can be derived from the following equation.

$$V = L_{MAG} \frac{dI_{MAG}}{dt} \qquad (2.30)$$

This equation leads to:

$$V_{ON} \cdot t_{on} = L_{MAG} \cdot \Delta I_{MAG} \qquad (2.31)$$

Since $V_{ON}$= $V_{IN}$ , and $t_{on} = DT = \frac{D}{f_s}$,

$$\Delta I_{MAG} = \frac{V_{IN} \cdot D}{L_{MAG} \cdot f_s} \tag{2.32}$$

Magnetizing current swings between $-I_R$ value to $I_{MAG}$ value as seen in Figure A.3. Assuming $I_R \cong I_{MAG}$ gives:

$$I_{MAG} = \frac{\Delta I_{MAG}}{2} \cdot \tag{2.33}$$

We can calculate rms value of the piecewise linear waveform given in Figure 2.6. Its expression is given in equation 2.34. [6]

$$I_{C(QA)\_RMS} = \sqrt{(I_{C(QA)\_peak}{}^2 + I_{C(QA)\_\min}{}^2 - I_{C(QA)\_peak} \cdot I_{C(QA)\_\min}) \cdot \frac{D}{3}} \tag{2.34}$$

$I_{C(QA)\_peak}$ is calculated from the Equation (2.29). $I_{C(QA)\_\min}$ is the lowest value of the transistor current ad can be obtained from Figure 2.6:

$$I_{C(QA)\_\min} = (I_o - \frac{\Delta I_L}{2}) \cdot N \tag{2.35}$$

Expressions of conduction losses for MOSFET and IGBT switches are given in Equations (2.36) and (2.37), respectively. $R_{DS(on)}$ is the on state resistance of the MOSFET, and $V_{CE(on)}$ is the on state collector emitter voltage of the IGBT.

$$P_{con\_MOSFET} = I_{D(QA)\_RMS}{}^2 \cdot R_{DS(on)} \tag{2.36}$$

$$P_{con\_IGBT} = I_{C(QA)\_RMS} \cdot V_{CE(on)} \tag{2.37}$$

Expressions of turn on switching losses for MOSFET and IGBT switches are given in Equations 2.38 and 2.39, respectively. $t_{sw(on)}$ is the turn on time of the MOSFET and $E_{ON}$ is the turn on energy of the IGBT.

$$P_{SW\_ON\_MOSFET} = \frac{V_{DS} \cdot I_{D(QA)\_\min} \cdot t_{sw(on)} \cdot f_s}{6} \quad (2.38)$$

$$P_{SW\_ON\_IGBT} = E_{ON} \cdot f_s \quad (2.39)$$

Expressions of turn off switching losses for MOSFET and IGBT switches are given in Equations 2.40 and 2.41, respectively. $t_{sw(off)}$ is the turn off time of the MOSFET and $E_{OFF}$ is the turn off energy of the IGBT.

$$P_{SW\_OFF\_MOSFET} = \frac{V_{DS} \cdot I_{D(QA)\_peak} \cdot t_{sw(off)} \cdot f_s}{6} \quad (2.40)$$

$$P_{SW\_OFF\_IGBT} = E_{OFF} \cdot f_s \quad (2.41)$$

### 2.2.7 Active Clamp Stage

Active clamp stage contains a clamp capacitor, Cr and an N channel MOSFET switch, Qc. Voltage stress of the clamp capacitor is derived in the previous section and it is given by Equation 2.27. From Figure 1.12, it can be seen that voltage stress of the clamp switch is the same as the voltage stress of the main switch. Then, Equation 2.28 is also valid for the clamp switch voltage stress. Current stress of the clamp switch is equal to the magnetizing current. This can be seen from Figure A.3. Then, Equation 2.33 gives peak current stress of the clamp switch.

Clamp capacitor and magnetizing inductance of the transformer performs a resonant circuit. The resonant frequency of this circuit is given in equation [5].

$$f_{r(clamp)} = \frac{1}{2\pi \cdot \sqrt{L_{MAG} \cdot C_R}} \quad (2.42)$$

The resonant frequency must be lower then the switching frequency of the main switch in order to maintain a constant $V_{DS}$ voltage while the main switch is off [5]. Minimum required clamp capacitance can be found from this criterion:

$$f_{r(clamp)} < f_s \tag{2.43}$$

### 2.2.8 Fast Diodes

In this section voltage stress expression of fast diodes are derived. These equations will be used in the following chapter in order to calculate the voltage stress od diodes.

In Figure A.1, diodes D1 and D2 operates alternatively in order to maintain constant inductor current. When the main switch is ON, D1 conducts the inductor current and D2 is reversed biased. Voltage stress of D2 is equal to the transformer secondary winding voltage. When the main switch is OFF, D2 is forward biased and D1 is reversed biased. Voltage stress of D1 is again equal to the transformer secondary winding voltage.

From Figure A.3, when the main switch is ON, voltage across the primary winding is $V_{IN}$, then voltage stress of D2 is:

$$V_{D2} = V_{IN} \cdot N \tag{2.44}$$

When the main switch is OFF, voltage across the primary winding is $V_{CR}$, and then voltage stress of D1 is:

$$V_{D1} = V_{CR} \cdot N \tag{2.45}$$

By combining equation 2.45 and 2.46 gives:

$$V_{D1} = N\frac{D}{1-D}V_{IN} \qquad (2.46)$$

### 2.2.9 Output Inductor

Selection of output inductor is critical since it affects the operation of the converter circuit. Depending on the inductor current waveform, the operation of the forward converter can be examined in 2 different modes. These are:

- Continuous Conduction Mode
- Discontinuous Conduction Mode

These modes are explained in Appendix A.3 .From Equations A.13 and A.22, it can be seen that continuous mode of operation is more desirable for forward converter because in this mode of operation output voltage is linearly related to the duty cycle. In order to guarantee continuous mode operation for even light loads, output inductor must be selected as high as possible. This is analyzed in the following section.

#### 2.2.9.1 Determining Inductor Value

Inductor selection is critical in converter design since it affects the operation mode of the converter. In equation (2.47), expression of inductor current ripple is given for continuous mode of operation. This equation is derived form Equation (A.19)

$$\Delta I_L = \frac{Vo \cdot (1-D)}{L \cdot f_s} \qquad (2.47)$$

In order to maintain the continuous mode of operation, inductor current must be nonzero within a switching cycle. Then for continuous mode of operation:

$$Io - \frac{\Delta I_L}{2} \geq 0 \qquad (2.48)$$

$$Io \geq \frac{\Delta I_L}{2} \tag{2.49}$$

Then, condition for discontinuous mode of operation is:

$$Io < \frac{\Delta I_L}{2} \tag{2.50}$$

When output current is decreased under $\Delta I_L / 2$ level, converter operates in discontinuous conduction mode. In order to maintain continuous mode of operation for wide range of output current, i.e. for light load conditions, output ripple $\Delta I_L$ must be minimized.

In order to minimize the current ripple, inductor value must be increased according to Equation 2.47. On the other hand, to increase inductor value, a core with large size must be used. Increasing core size also increase the cost of the converter. Moreover, in some cases a bigger core may not be available in market. Then, in inductor selection, needed core size must be calculated.

In determining the core size, area product method is used. Area Product, obtained by multiplying the core magnetic cross-section area ($A_c$) by the window area ($W_a$) available for the winding must equal to or greater then the area product given in Equation (2.51). The derivation of this equation can be found in reference [1].

$$AP = \frac{L \cdot I_{L\,peak} \cdot I_{L\,rms}}{J \cdot Ku \cdot B_{peak}} \tag{2.51}$$

L is the inductor value. $I_{L\,peak}$ is the peak inductor current, in A. $I_{L\,rms}$ is the rms inductor current in A. Ku is the window utilization factor. $B_{peak}$ is the peak flux density of the core material.

For continuous mode of operation, $I_{L\,rms}$ is calculated by using the piecewise linear waveform of inductor current given in Figure A.9 [6]. When the main switch is ON, D1 diode carries the inductor current, for this interval its rms value is:

$$I_{D1\,rms} = \sqrt{(I_{L\,peak}{}^2 + I_{L\min}{}^2 - I_{L\,peak} \cdot I_{L\min}) \cdot \frac{D}{3}} \qquad (2.52)$$

When the main switch is OFF, D2 diode carries the inductor current, its rms value is:

$$I_{D2\,rms} = \sqrt{(I_{L\,peak}{}^2 + I_{L\min}{}^2 - I_{L\,peak} \cdot I_{L\min}) \cdot \frac{D-1}{3}} \qquad (2.53)$$

RMS value of rms diode currents gives rms of inductor current $I_{L\,rms}$.

$$I_{L\,rms} = \sqrt{I_{D1\,rms}{}^2 + I_{D2\,rms}{}^2} \qquad (2.54)$$

In equation 2.52 and 2.53, $I_{L\min}$ is the minimum inductor current. $I_{L\min}$ and $I_{L\,peak}$ can be calculated with following Equations.

$$I_{L\min} = Io - \frac{\Delta I_L}{2} \qquad (2.55)$$

$$I_{L\,peak} = Io + \frac{\Delta I_L}{2} \qquad (2.56)$$

After selecting the core size by using area product method, number of turns is calculated. Its expression is derived form faraday's law of induction equation:

$$V = L\frac{di}{dt} = N\frac{d\phi}{dt} = NA_c\frac{dB}{dt} \qquad (2.57)$$

$$L\frac{\Delta i_L}{\Delta t} = NA_c\frac{\Delta B}{\Delta t} \tag{2.58}$$

$$N = \frac{L \cdot \Delta i_L}{Ac \cdot \Delta B} \tag{2.59}$$

For soft ferrites and most other magnetic materials used in power conversion there is almost no field remaining in the core if the current in windings goes to zero [6]. Therefore, since flux density is zero when current is zero we can write as:

$$N = \frac{L \cdot i_{L\,peak}}{Ac \cdot B_{peak}} \tag{2.60}$$

The air gap length ($l_g$) that will achieve the required inductance is calculated from the following equation [10].

$$\sum l_g = \mu_0 \cdot N^2 \cdot \frac{Ae}{L} \cdot (1 + \frac{\sum l_g}{D_{cp}})^2 \cdot 10^4 \tag{2.61}$$

$\sum l_g$ is the total air gap length in cm.

$\mu_0$ is the permeability of free space. $\mu_0 = 4\pi \cdot 10^{-7}$

$N$ is the number of turns.

$A_e$ is the effective area the core in cm

$L$ is the inductance in μH.

$D_{cp}$ is the dimension of center pole of the core in cm.

Expressions derived in this section will be used in the following design chapter in order to determine the size of the inductor core and calculate the turns number and air gap.

### 2.2.10 Output Capacitor

The minimum output capacitance required to maintain the output voltage ripple below the design target of $V_{out(rip)}$ is obtained by using the following Equation. This equation will be used in the following chapter in order to calculate the output capacitor value [1].

$$C_{out} = \frac{\Delta I}{8 \cdot f_s \cdot V_{out(rip)}} \tag{2.62}$$

### 2.2.11 Controller Selection

Control techniques in DC-DC converters are given in Appendix A.2. In this study, voltage mode control technique is selected because of its simplicity. In order to eliminate its line regulation drawback, a controller with feed forward feature is selected. National Semiconductor's LM5025A type numbered Active Clamp Voltage Mode PWM Controller is selected as the controller.

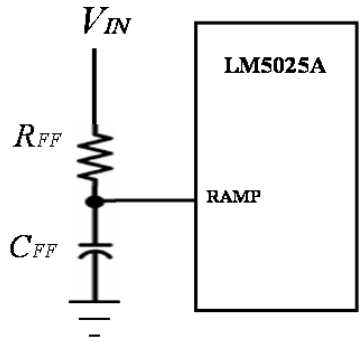



**Figure 2.7: Feed Forward In LM5025A Controller**

LM5025A controller has feed forward feature in order to achieve better line regulation than the conventional voltage mode control technique. In the controller, saw tooth signal is generated at the RAMP pin by the charging of the external $C_{FF}$ capacitor over $R_{FF}$ resistor from $V_{IN}$ voltage (see Figure 2.7). When the signal at RAMP pin reaches 2.5 Volts level, it is terminated by an internal circuit. Since the capacitor charging time is constant and determined by the $R_{FF}C_{FF}$ time constant, slope of the charging waveform, PWM saw tooth, is dependent to the $V_{IN}$ voltage. As a result, input voltage determines the slope of the saw tooth signal and input voltage variations directly affect the duty ratio.

# CHAPTER 3

# DESIGN, IMPLEMENTATION AND TEST OF THE SWITCH MODE POWER SUPPLY

## 3.1 Introduction

In the previous chapter, most of the design equations are derived. In this chapter, the main goal is to design a switch mode power supply (SMPS) that generates a rectified sinusoidal output voltage. Here, we will used the design equations derived in the previous chapter. Main specifications of the power supply is given in Table 3.1

**Table 3.1: Main Specifications of the SMPS**

| **Specification** | **Minimum** | **Maximum** |
|---|---|---|
| Input Voltage Range | 200 VAC rms | 240 VAC rms |
| Input Voltage Frequency | 50 Hz | |
| Output Voltage Range | 0 | 240 VAC rms |
| Output Frequency Range | 10 Hz | 100 Hz |
| Output Power | 0 | 1500 Watts |

In this chapter, components of the DC-DC converter will be selected in order to operate for all line and load conditions. These conditions are:

1. For 240 VAC rms input voltage, output of the DC-DC converter should be adjustable between 0 and 350 VDC. Converter should give 1500 Watts output power at 350 VDC output voltage. All components ratings should satisfy this condition.

2. For 200 VAC rms input voltage, output of the DC-DC converter should be adjustable between 0 and 350 VDC. Converter should give 1500 Watts output power at 350 VDC output voltage. All components ratings should satisfy this condition.

After design phase, simulations will be achieved in order to verify the designed SMPS. At the end of the chapter, implementation and test of the designed SMPS is presented.

## 3.2 Switching Frequency and Duty Ratio Selection

In DC-DC converters, switching frequency can be up to 1000 kHz. As frequency increases component sizes and output ripple decreases. However, switching losses increase as frequency increases. In determining the switching frequency, there is a trade-off between component sizes and efficiency. At high switching frequencies, due to the noise coupling problems, PCB layout design has a critical importance. Switching at high frequencies is a challenging requirement for layout design. In this thesis, switching frequency is selected to be 25 kHz in order to limit the switching losses and EMC problems. Furthermore, the power load is rather high and the switching element is likely to be an IGBT rather then a MOSFET.

In DC-DC converters output voltage is regulated via duty ratio control. Duty cycle ratio is dependent to the input voltage range. By rewriting Equation 2.1 and the output voltage expression is obtained as given in Equation (3-1). $D$ is the duty ratio, $V_{IN}$ is the input voltage, and $N$ is the transformer turns ratio

$$V_{OUT} = V_{IN} \cdot D \cdot N \qquad (3\text{-}1)$$

For a constant turn's ratio *N*, $V_{IN} \cdot D$ product must be constant. Maximum duty cycle $D_{max}$ is selected for the minimum input voltage $V_{INmin.}$ If we assume that the input voltage ripple is 10%, then minimum input voltage of the converter is approximately $V_{INmin} = 200 \times \sqrt{2} \times 0.9 =$ 255 VDC. Maximum input voltage of the converter is approximately $V_{INmax} = 240 \times \sqrt{2}$ =340 VDC.

Selection of the maximum duty cycle effects voltage ratings of the main transistor and rectifier diodes. This selection must be optimized regarding the voltage stress of these devices.

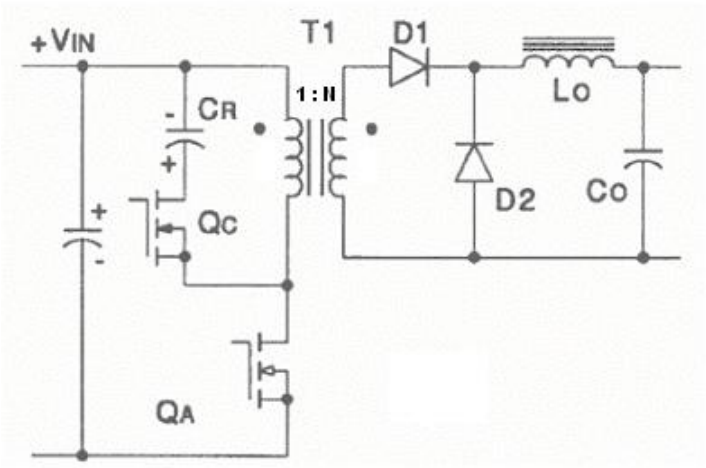



**Figure 3.1: Active Clamp Forward Converter**

In the previous section, voltage stresses of the main transistor $Q_A$ and the diodes $D_1$ and $D_2$ are derived. By using Equation (3.1) transformer turns ratio N is calculated for different $D_{max}$ values and 255 VDC minimum input voltage. Output voltage is taken to be 350V. The resultant curve is given in Figure 3.2

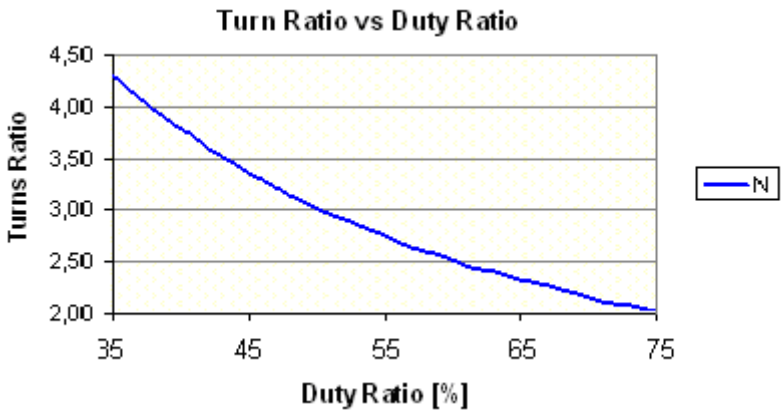



**Figure 3.2: Turns Ratio vs Duty Ratio for $V_{IN}$=255V, $V_{OUT}$=350V**

By using Equations (2.25), (2.39) and (2.41), maximum voltage stress of the main switch and diodes are calculated. Equation (2.39) is used with lowest input voltage $V_{IN}$=255V, Equations (2.25) and (2.41) are used with highest input voltage $V_{IN}$=340V. The results of the calculations are given in Figure 3.3.

In order to minimize primary side current stress and transformer copper losses, turns ratio should be selected as minimum. In duty ratio selection, the goal is to obtain minimize the turns ratio and voltage stress. For transistor selection, the goal is to obtain a voltage stress value that is lower then 600V level ($V_{CE}$ < 600V). For diode selection, goal is obtain a voltage stress value that is lower then 1200V level ($V_{D1}$<1200V and $V_{D2}$ < 1200V).

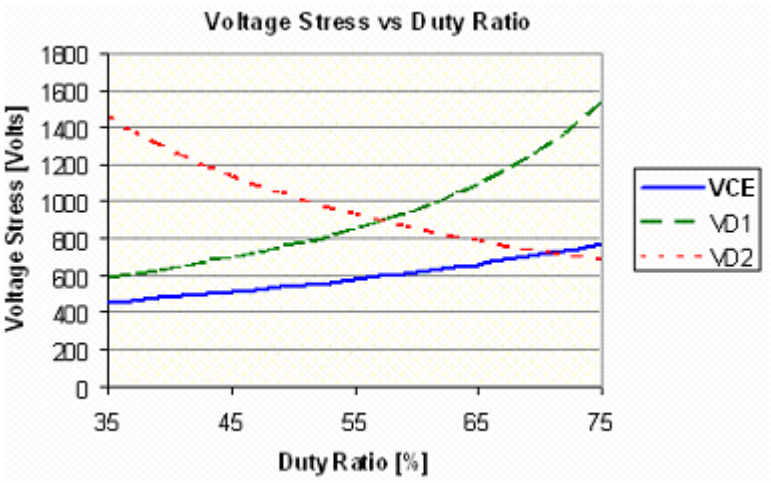



**Figure 3.3: Voltage Stress vs Maximum Duty Ratio**

From figure 3-3, duty ratio value is selected to be 51% regarding the 600V level for $V_{DS}$ and 1200V level for $V_{D1}$ and $V_{D2}$. Note that, this duty cycle value is valid for the lowest input voltage, $V_{IN}$ = 255 VDC. Converter must operate with the input voltage range 255 to 340VDC. Then for 340VDC highest input voltage, minimum duty ratio is obtained as 38%.

Maximum voltage stress for D1 diode occurs at lowest input voltage, it is $V_{D1}$= 786V For this condition, transistor stress is 530V; voltage stress of diode D2 is 795 V.

Maximum voltage stress for transistor and D2 diode occurs at the highest input voltage, 340V. They are $V_{CE}$=550V and $V_{D2}$=1000V, respectively. Voltage stress of diode D1 is 630V.

Transformer design is performed by applying the design procedure developed for this thesis. It is given in Figure 3.4.

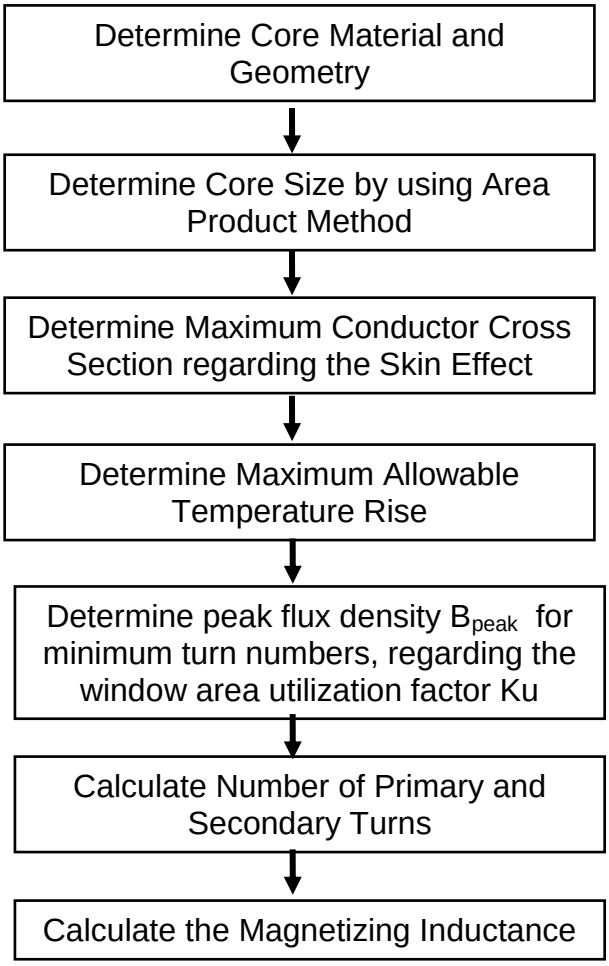



**Figure 3.4: Design Procedure for the Transformer**

Transformer core is selected from EPCOS catalog. E/ETD, RM/PM core geometries with N27, N87 and N49 ferrite materials are recommended for forward converter topology in the manufacturer's application note [5]. E core is selected due to its relatively low cost and better heat dissipation property [6].

### 3.2.1 Area Product Calculation

In order to determine the core size, area product method is used. Area product equation is derived in the previous section. It is given in Equation 3.2.

$$A_c \cdot W_a = \frac{P_{IN} \cdot \sqrt{D}}{\Delta B \cdot f_s \cdot J \cdot K_u} \qquad (3.2)$$

Where,

- $A_c \cdot W_a$ is the area product value in $m^4$.
- $P_{IN}$ is the input power of the converter, in Watts. $P_{IN}$= 1500 W
- D is the duty ratio of the converter. D = 0.51
- $f_s$ is the switching frequency of the converter, in Hertz. $f_s$ = 25000 Hz.
- J is the rms current density of the winding conductor, in $A/m^2$. J = $250x10^4$ $A/m^2$
- $K_u$ is the window utilization of the core for primary windings. For $K_u$=0.35, overall window utilization factor and turns ratio N=3, window utilization factor for primary windings is calculated as $K_u$= 0.0875.
- $\Delta B$ is the flux density swing of the core, in Tesla. Peak flux density is taken to be $B_{peak}$ = 0.35 Tesla, then $\Delta B$ =0.7 Tesla.

$$AP = \frac{1500 \cdot (0.51)^{1/2}}{0.0875 \cdot 250 \cdot 10^4 \cdot 0.7 \cdot 25000} = 2.77x10^{-7}\ m^4 = 27.7\ cm^4$$

E80/58/20 core size is selected according to its 30.84 $cm^4$ AP value. Its shape and dimensions are given in Figure 3.5.

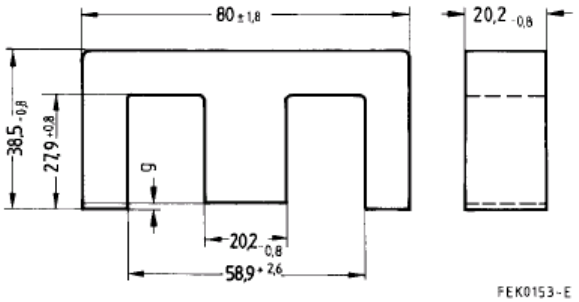



**Figure 3.5: Dimensions of the Selected Core E80/58/20**

Properties of the selected core are given in Table-3.2 [8].

**Table 3.2: Properties of the Selected Core**

| | |
|---|---|
| Core Geometry and Size | E80/58/20 |
| Core Material | Ferrite, N87 |
| Effective Volume ($V_e$) | 71800 $mm^3$ |
| Effective Length ($l_e$) | 184 mm |
| Effective Area ($A_e$) | 390 $mm^2$ |
| Window Area ($W_a$) | 791 $mm^2$ |
| Area Product ( $W_aA_c$ ) | 30.84 $cm^4$ |
| Inductance Factor ($A_L$) | 4500 nH |

## 3.2.2 Conductor Selection

Switching frequency is 25 kHz. According to Figure 2.1, recommended maximum copper diameter at this frequency is about 36 mils= 0.91 mm. Then, 0.8 mm conductor is selected. Its cross sectional area is 0.5 $mm^2$.

Number of the parallel conductors is determined by the average primary and secondary currents. For 1500 Watt output power and 270 VDC input voltage (average input voltage for 200VAC rms and 10% ripple: 200x $\sqrt{2}$ x0.95), average primary current is found as $I_{P\_avg}$= 5.56 A. For N=3 turns ratio average secondary current is $I_{S\_avg}$ =1.85 A. Current carrying capacity of the 0.8 mm (0.5 $mm^2$) copper conductor for J = 2.5 A/$mm^2$ current density is 1.25A. Then, number of parallel conductors for primary windings is 5.56/1.25≅ 5. Number of parallel conductors for secondary windings is 3.57/1.25≅ 3.

### 3.2.3 Thermal Analysis

As core temperature rises, core losses can rise and the maximum saturation flux density decreases. Thermal runaway can occur causing the core to heat up to its Curie temperature resulting in a loss of all magnetic properties and catastrophic failure [9]. For 30 $^oC$ ambient temperature, and 100 $^oC$ maximum allowable core temperature, maximum allowable temperature rise is 70 $^oC$. In the manufacturer's application document thermal resistance of the selected core E80/38/20 is given as 7 $^oC/W$ [9]. For 70 $^oC$ temperature rise, 10 W total power loss is tolerable at the transformer. In the following sections, the core flux density and wire size selection will be made so that the total loss remain below the defined level assuring accepted temperature rise.

### 3.2.4 Peak Flux Density ($B_{peak}$ ) Selection

In this section, maximum allowable peak flux density $B_{peak}$ will be selected according to the temperature rise. For different Bpeak values, temperature rise is calculated. While selecting the maximum $B_{peak}$ value, window utilization factor must be kept about 35%. In order to obtain the relation between temperature rise and peak flux density, the calculations given in Figure 3.6 are done.

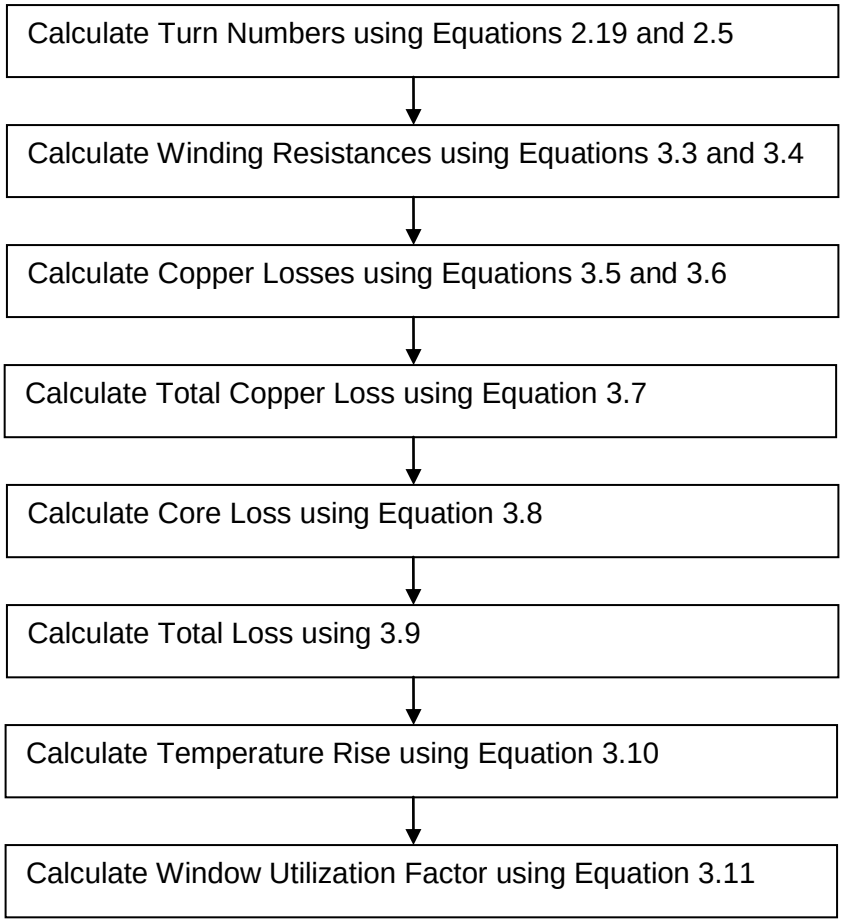



**Figure 3.6 Calculation Order to Obtain Area Product**

Primary turn number is calculated by using Equation 2.19 for $V_{IN}$= 255V, D=0.51 duty cycle, and fs=25000 Hz switching frequency.

$R_{pr}$ and $R_{\sec}$ are the winding resistances of primary and secondary turns. These resistance values are calculated by using following equations:

$$R_{pr} = Np \cdot l_{turn} \cdot \frac{R_{con}}{n_{pr\_con}} \qquad (3.3)$$

$$R_{\sec} = Ns \cdot l_{turn} \cdot \frac{R_{con}}{n_{\sec\_con}} \quad (3.4)$$

In these equations, NP and Ns are the primary and secondary turn numbers, respectively. $l_{turn}$ is the average length of 1 turn. . In reference [9], it is given as $l_{turn}$=165 mm for the selected core size. $R_{con}$ is the dc resistance of the 0.8mm copper, it is 34 mΩ /m [4]. $n_{pr\_con}$ and $n_{\sec\_con}$ are number of parallel conductors used in primary and secondary windings, respectively. $n_{pr\_con}$=5 and $n_{\sec\_con}$ = 3. Note that, $Np \cdot l_{turn}$ and $Ns \cdot l_{turn}$ product gives total length of primary and secondary windings, respectively.

$P_{cu\_pr}$ and $P_{cu\_\sec}$ are copper losses of the primary and secondary windings, respectively. These losses are calculated from the following equations:

$$P_{cu\_pr} = I_{pr}^{\ 2} \cdot R_{pr} \quad (3.5)$$

$$P_{cu\_\sec} = I_{\sec}^{\ 2} \cdot R_{\sec} \quad (3.6)$$

Here, $I_{pr}$ and $I_{\sec}$ are primary and secondary rms currents, respectively. Relation between rms and average current for pulsed current waveform is $I_{rms} = \frac{I_{avg}}{\sqrt{D}}$ [4].

Then $I_{pr}$ = $\frac{5.56}{\sqrt{0.51}}$ =7.8A and $I_{\sec}$ = $\frac{1.85}{\sqrt{0.51}}$ =2.6A.

Total transformer copper loss $P_{CU}$ is calculated from the following equation.

$$P_{CU} = P_{cu\_pr} + P_{cu\_\sec} \quad (3.7)$$

Core loss is calculated by using manufacturer's core loss curves. For 25 kHz switching frequency, core loss curve for N87 material is given in Figure 3.7 [12]. From the curves, core loss per unit volume ($P_S$, specific loss) is obtained. Total

core loss, $P_{core}$ is calculated by using the Equation (3.8). $V_e$ is the effective volume of the core, and given in Table 3.2.

$$P_{core} = P_S \cdot V_e \tag{3.8}$$

Total transformer loss is calculated from the following equations .

$$P_{loss} = P_{core} + P_{cu} \tag{3.9}$$

The temperature rise is directly dependent to the total power dissipation as given in the following Equation:

$$\Delta T = R_{th} \cdot P_{loss} \tag{3.10}$$

Here, Rth is the thermal resistance of the core, $P_{loss}$ is the total power loss of the transformer and ΔT is the temperature rise.

Window utilization factor Ku is the ratio of copper area $A_{cu}$ to the core window area $W_a$, as given in the following equation:

$$Ku = \frac{Copper\,Area\ (A_{cu})}{WindowArea(Wa)} \tag{3.11}$$

Window area of the selected core is given in Table-2.1. It is 791 $mm^2$. Copper area is the sum of total primary and secondary copper cross sections. In the primary windings and secondary windings 0.64 $mm^2$ copper wire is used. Then, expression for the copper area is:

$$A_{cu} = (n_{pr\_con} \cdot N_p + n_{sec\_con} \cdot N_s) \cdot 0.64 \text{ mm}^2 \tag{3.12}$$

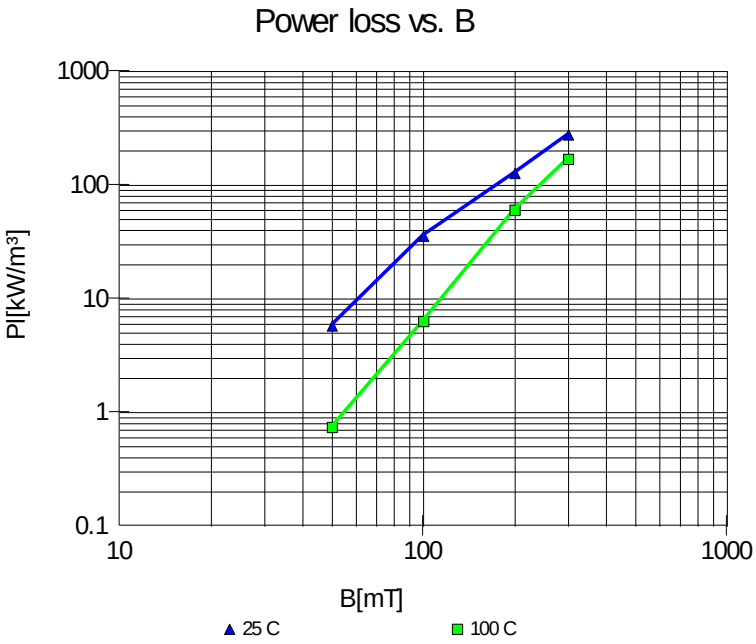



**Figure 3.7: Core Loss Curve for N87 Material at 25 kHz for 25°C and 100°C**

By using equations (3-3) to (3-12), core losses, copper losses, total losses and temperature rise are calculated at 0.15, 0.20, 0.25 and 0.3 Tesla $B_{peak}$ values. Core loss is calculated for 100°C core temperature. Calculation results are given in Table 3.3, Table 3.4 and Figure 3.8.

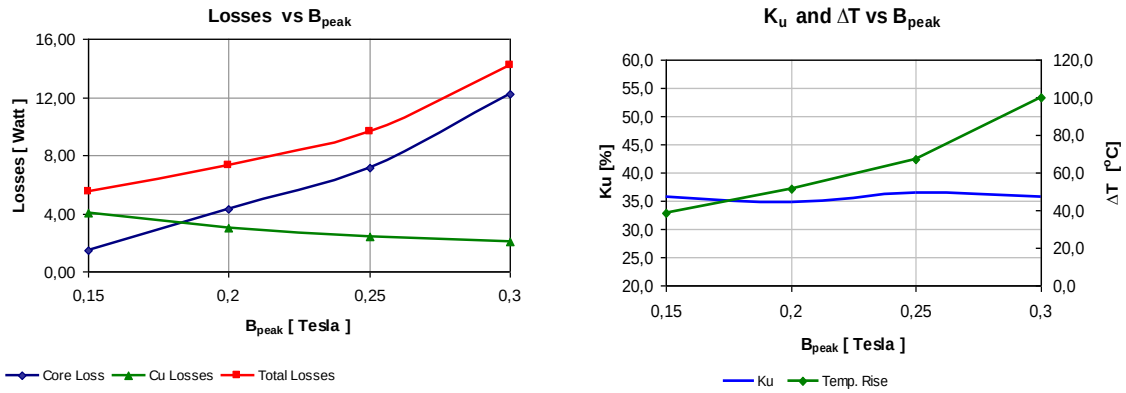
**Table 3.3: Copper Loss For Different $B_{peak}$ Values**

| $B_{peak}$ (T) | Np | Ns | Primary Copper Resistance (Ω) | Primary Copper Loss (W) | Secondary Copper Resistance (Ω) | Secondary Copper Loss (W) | Total Copper Loss (W) |
|---|---|---|---|---|---|---|---|
| 0.15 | 45 | 134 | 0.05 | 3.04 | 0.15 | 1.01 | 4.05 |
| 0.20 | 33 | 100 | 0.04 | 2.28 | 0.11 | 0.76 | 3.04 |
| 0.25 | 27 | 80 | 0.03 | 1.82 | 0.09 | 0.61 | 2.43 |
| 0.30 | 22 | 67 | 0.02 | 1.52 | 0.07 | 0.51 | 2.03 |

**Table 3.4: Transformer Loss and Temperature Rise For Different $B_{peak}$**

| Bpeak (T) | Ps (kW/m3) | Core Loss (W) | Copper Loss (W) | Total Loss (W) | Temperature Rise (C) | Copper Area mm2 | Window Utilization Factor |
|---|---|---|---|---|---|---|---|
| 0.15 | 20 | 1.44 | 4.05 | 5.49 | 38.4 | 282 | 35.7 |
| 0.20 | 60 | 4.31 | 3.04 | 7.35 | 51.4 | 275 | 34.8 |
| 0.25 | 100 | 7.18 | 2.43 | 9.61 | 67.2 | 288 | 36.4 |
| 0.30 | 170 | 1.21 | 2.03 | 14.24 | 99.6 | 282 | 35.7 |

From Figure (3-8), it is seen that maximum peak flux density value for $\Delta T < 70\ ^{o}C$ is $B_{peak}$ =0.25 Tesla. Then 0.25 T peak flux density is selected. Then for $K_u$=36.4%, $n_{pr\_con} = 5$ and $n_{sec\_con} = 4$.




(a) (b)

**Figure 3.8: (a)Transformer Losses versus $B_{peak}$ (b) Window Utilization Factor $K_u$ and Temperature Rise $\Delta T$ versus $B_{peak}$**

Number of primary turns is calculated as $N_p$= 27 turns by using Equation (2.19) for $B_{peak}$=0.25T. Then magnetizing inductance is obtained from Equation (2.20). $A_L$ is the inductance factor of the selected core, it is given in Table 3-2 as $A_L$=4500 nH. For $A_L$=4500 nH and $N_p$=27 turns, $L_{MAG}$ = 3.28 mH.

Properties of the designed transformer are summarized in Table 3.5.

**Table 3.5: Properties of the Transformer**

| | |
|---|---|
| Core Geometry & Material | E80/38/20 & Ferrite, N87 |
| Primary Turns | 27 turns 5 x 0.64 $mm^2$ |
| Secondary Turns | 81 turns 4 x 0.64 $mm^2$ |
| Window Utilization Factor (Ku) | 36.4 % |
| Peak Flux Density ($B_{peak}$) | 0.25 Tesla |
| Core Losses ($P_{core}$) | 7.18 W |
| Copper Losses ($P_{CU}$) | 2.03 W |
| Total Losses & Efficinecy | 9.61 W & 99.3% |
| Temperature Rise ($\Delta T$) | 67.2$^oC$ |
| Magnetizing Inductance ( $L_{MAG}$ ) | 3.28 mH |

As given in Table 3.5, efficiency of the designed transformer is 99.3%. This is a very good efficiency value.

## 3.3 Main Transistor Selection

Current, voltage and power stresses are the main factors considered in main transistor selection. In section 3.1, maximum voltage stress of the main transistor is calculated as 550 Volts.

RMS current of the main switch is calculated from Equation 2.34. First, we must calculate the magnetizing current, the peak and lowest value of the transistor current by using equations derived in Section 2.2.3.

Magnetizing current is calculated from equations 2.32 and 2.33. We can rewrite these equations as:

$$I_{MAG} = \frac{V_{IN} \cdot D}{2L_{MAG} \cdot f_s} \qquad (3.13)$$

For $V_{IN}$=255V, D=0.51, $L_{MAG}$= 3.28 mH and fs=25000 Hz, magnetizing current is calculated as

$$I_{MAG} = 0.8A$$

Peak transistor current is calculated Equation 2.26. For Io=6.8A, ΔI=6.8A, $I_{MAG}$ =0.8A, and N=3, peak transistor current is calculated as

$$I_{C(QA)\_peak} = 6.8 \cdot 3 + \frac{6.8}{2} \cdot 3 + 0.8$$

$$I_{C(QA)\_peak} = 31.4 \text{ A.}$$

By using Equation 2.35, lowest value of the transistor current is calculated. For Io=6.8A, ΔI=6.8A, and N=3 it is

$$I_{C(QA)\_\min} = (6.8 - \frac{6.8}{2}) \cdot 3$$

$$I_{C(QA)\_\min} = 10.2 \text{ A.}$$

By using peak and lowest value of the transistor current, we can now calculate the its RMS value by using Equation 2.34. The worst case is for the highest duty ratio 51%, then the RMS current is calculated as:

$$I_{C(QA)\_RMS} = \sqrt{(31.4^2 + 10.2^2 - 31.4 \cdot 10.2) \cdot \frac{0.51}{3}}$$

$$I_{C(QA)\_RMS} = 9.77 \text{ A}$$

IXYS RGP4062DPbF IGBT is selected as the main transistor. Its properties are given in Table 3-6.

**Table 3.6: IGBT Specification Data**

| | |
|---|---|
| Manufacturer | IRF |
| Model | IRGP4062DPbF |
| VCES | 600 V |
| IC | 24 A |
| $VCE_{ON}$ | 1.9V for 175C, 20A |
| $E_{ON}$ | 0.2 mJ for 15A |
| $E_{OFF}$ | 0.6 mJ for 20A |

Conduction loss of the transistor is calculated by using Equation 2.37. For 9.77A rms current and $V_{CE(on)}$ =1.9V, conduction loss is

$$P_{con} = 9.77 \cdot 1.9$$

$$P_{con} = 18.6W$$

Turn on switching loss is calculated by using Equation 2.39. For 25kHz switching frequency, and $E_{ON}$ = 0.2 mJ, it is

$$P_{SW\_ON} = 0.2 \cdot 10^{-3} \cdot 25000$$

$$P_{SW\_ON} = 5W$$

Turn off switching loss is calculated by using Equation 2.41. For 25kHz switching frequency, and $E_{OFF}$ = 0.6 mJ, it is

$$P_{SW\_OFF} = 0.6 \cdot 10^{-3} \cdot 25000$$

$$P_{SW\_OFF} = 15W$$

Then total losses of the transistor are 38.6 W. Heatsink analysis is given in the following sections.

## 3.4 Fast Diode Selection

In section 3.1, maximum voltage stress of the rectifier diodes are calculated as $V_{D1}$=786 V and $V_{D2}$=1000V. The average current of these diodes are average secondary current is $I_{S\_avg}$= 3.57A as calculated in section 3.1. IXYS's DSEP12-30A type number fast diodes are selected for this application. Specifications of the selected diode are given in Table 3.7.

Total losses on the rectifier diode can be calculated form the following equation.

$$P_{tot} = P_{con} + E_{off} f_{sw} + P_{off} \quad (3.14)$$

In this Equation, $P_{con}$ is the conduction, $E_{off} f_{sw}$ is the turn off and $P_{off}$ is the blocking loss of the diode. The expressions for these loss terms are given in the following Equations.

$$P_{on} = V_{TO} I_{F(AV)} + r_T I^2_{F(RMS)} \quad (3.15)$$

$$E_{off} = 0{,}5 I_{RRM} V_{off} t_B \quad (3.16)$$

$$P_{off} = I_R V_R D \quad (3.17)$$

In these equations, $I_{F(AV)}$ is the average and $I_{F(RMS)}$ is the rms value of diode's forward current. Expression for $I_{F(AV)}$ and $I_{F(RMS)}$ is given in Equation 3.18 and 3.19. $V_{off}$ is the voltage stress of the diode while it is off. D is the duty ratio of the converter, D=0.51. $V_{RRM}$, $V_{TO}$, $r_T$, $t_{rr,}$ $I_{RRM}$ and $I_R$ parameters for the selected diode is given in Table 3.7. $V_{RRM}$ and $t_{rr}/2$ values are used for $V_R$ and $t_B$, respectively.

$$I_{F(AV)} = \frac{I_{peak} \cdot D}{2} \quad (3.18)$$

$$I_{F(RMS)} = \frac{I_{peak} \cdot \sqrt{D}}{\sqrt{3}} \quad (3.19)$$

**Table 3.7: Fast Diode Specification Data**

| | |
|---|---|
| Manufacturer | IXYS |
| Model | DSEP 12-12A |
| $V_{RRM}$ | 1200 V |
| $I_{RRM}$ | 4.5 A |
| $V_{TO}$ | 1.25 V |
| $r_T$ | 0.03 Ω |
| $t_{rr}$ | 40 ns |
| $I_R$ | 0.5 mA for $T_{Vj}$=150 $^oC$ |

In Equations 3.18 and 3.19, D is the duty cycle of each diode. Since diode D1 conducted during the main transistor is ON, duty cycle of D1 is 0.51, the highest duty cycle of the main transistor. Diode D2 is conducted during the main transistor is off, then duty cycle of D2 is 1-0.51=0.49. $I_{peak}$ is the peak current of the output inductor and it is $I_{peak}$ = 2x$I_{S_avg}$. Average secondary current is calculated in section 3.2.2, it is $I_{S\_avg}$= 3.57A. Average and rms current of D1 and D2 is obtained as $I_{F(AV)\_D1}$ = 1.82 A , $I_{F(RMS)\_D1}$ = 2.94A, $I_{F(AV)\_D2}$ = 1.75 A and $I_{F(RMS)\_D2}$ = 2.88A.

By using Equations (3.14) to (3.17), power losses for diodes D1 and D2 is calculated for 25 kHz switching frequency .Results are given in Table 3.8.

**Table 3.8: Fast Diode Power Losses**

| | | **D1** | **D2** |
|---|---|---|---|
| Conduction Losses, $P_{con}$ | (Watt) | 2.53 | 2.43 |
| Turn off Losses, $E_{off}\, f_{sw}$ | (Watt) | 0.88 | 1.25 |
| Blocking Losses, $P_{off}$ | (Watt) | 0.31 | 0.30 |
| **Total Losses** | **(Watt)** | **3.72** | **3.98** |

## 3.5 Output Inductor Selection

According to the manufacturer document [9], the biggest core among EE cores is E80/38/20. Inductor value is determined regarding the area product of this core. Area product expression given in Equation 2.51 is used. In this expression, peak and RMS inductor current values are dependent to the inductor current ripple, $\Delta I_L$. Then for different $\Delta I_L$ values, first peak and RMS current values are calculated, then area product is calculated. $I_O$ is the average output current. The calculations given in Figure 3.8 are done for different inductor ripple ratios, from $\Delta I_L/I_O$ = 0.1 to 1. for Ku=0.35 Calculation results are given in Table 3-9. In the calculations, $K_u$=0.35, $J_{rms}$=300A/cm$^2$, $B_{peak}$=0.3T, Io=6.8A, Vo=350V, D=0.38, and fs=25000 Hz are used.

**Table 3.9: Area Product Calculations For Different Inductor Ripple Ratios**

| $\Delta I_L$/Io | L [mH] | $I_{Lpeak}$ [A] | $I_{Lmin}$ [A] | $I_{rms}$[A] | AP[cm4] |
|---|---|---|---|---|---|
| 0,10 | 12,76 | 7,14 | 6,46 | 6,80 | 196,83 |
| 0,20 | 6,38 | 7,48 | 6,12 | 6,81 | 103,23 |
| 0,30 | 4,25 | 7,82 | 5,78 | 6,83 | 72,10 |
| 0,40 | 3,19 | 8,16 | 5,44 | 6,85 | 56,59 |
| 0,50 | 2,55 | 8,50 | 5,10 | 6,87 | 47,33 |
| 0,60 | 2,13 | 8,84 | 4,76 | 6,90 | 41,20 |
| 0,70 | 1,82 | 9,18 | 4,42 | 6,94 | 36,87 |
| 0,80 | 1,60 | 9,52 | 4,08 | 6,98 | 33,65 |
| 0,90 | 1,42 | 9,86 | 3,74 | 7,03 | 31,19 |
| 1,00 | 1,28 | 10,20 | 3,40 | 7,08 | 29,25 |

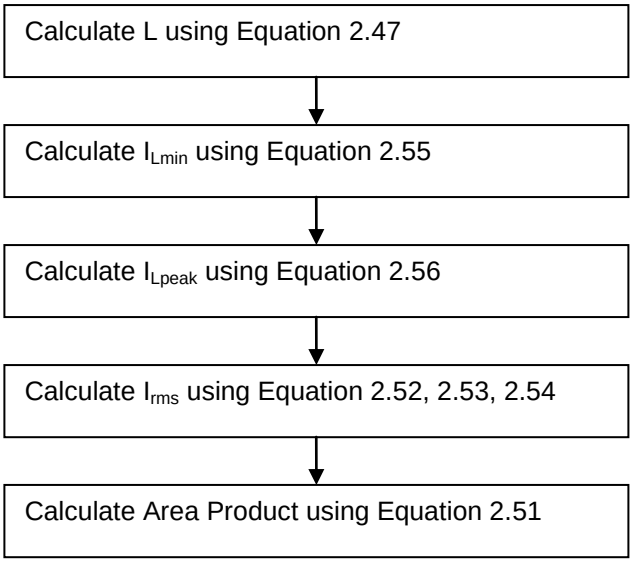



**Figure 3.9: Calculation Order to Obtain Area Product**

In order to minimize the current stresses of semiconductors, minimum current ripple ratio is aimed. For this purpose, largest inductor value is out target. The largest inductor value satisfying the area product of the E80/38/20 core is selected. As given in Table Table-3.2, the area product of this core is 30.84 $cm^4$. Then, according to the calculation results given in Table 3.6, maximum inductor value that can be obtained with this core is L=1.28mH.

Number of turns is calculated from the Equation 2.60 for $A_e$= 3.9 $cm^2$., $B_{peak}$=0.3T, $I_{peak}$=10.2 A, L=1.28mH.

$$N = \frac{L \cdot I_{peak}}{B_{peak} \cdot A_e} = \frac{1.28 \cdot 10^{-3} \cdot 10.2}{0.3 \cdot 3.9 \cdot 10^{-4}} = 112 \text{ turns}$$

In core loss calculations ac flux density $B_{AC}$ must be used. Its expression is given in Equation 3.20.It is calculated as $B_{AC}$=0.1T.

$$B_{AC} = \frac{I_{peak} - I_o}{I_{peak}} B_{peak} \quad (3.20)$$

From core loss curve given in Figure 3-7, loss per unit volume is $P_s$= 35 kW/m$^3$ at 25 kHz and 25$^o$C core temperature. For $V_e$=71800 mm$^3$ , core loss is $P_{core}$ = 2.52 W.

The conductor cross section area is selected by using Equation 3.21, for current density $J_{rms}$=3 A/mm$^2$, and $I_{rms}$=7.08A.

$$A_{cu} = \frac{I_{rms}}{J_{rms}} \quad (3.21)$$

$$A_{cu} = \frac{7.08}{3} = 2.36 mm^2$$

For Acu=2.36 mm$^2$ cross section area, the copper diameter is Φ1.7mm.

Copper losses are calculated by using Equation 3.22.

$$P_{CU} = I_o^{\,2} \cdot (N_p \cdot l_{turn} \cdot R_{con}) \quad (3.22)$$

$l_{turn}$ is the average length of 1 turn. $l_{turn}$ =0.165 m. $R_{con}$ is the dc resistance of the 1.7 mm copper, it is 7.75 mΩ /m [4]. For 6.8A output current and 112 turns, copper losses are calculated as $P_{CU}$ = 6.62 W.

Total inductor loss is $P_{core}$ + $P_{CU}$ = 9.14 Watt. For 7 $^o$C/W thermal resistance, temperature rise will be 64 $^o$C.

The air gap length ($l_g$) that will achieve the required inductance is calculated from the Equation 2.61.

$$\sum l_g = \mu_0 \cdot N^2 \cdot \frac{Ae}{L} \cdot (1 + \frac{\sum l_g}{D_{cp}})^2 \cdot 10^4$$

$\sum l_g$ is the total air gap length in cm.

$\mu_0$ is the permeability of free space. $\mu_0 = 4\pi \cdot 10^{-7}$

$N$ is the number of turns. $N$ = 112.

$A_e$ is the effective area the core. $A_e$ = 3.9 cm$^2$

$L$ is the inductance in μH. $L$ = 1280 μH

$D_{cp}$ is the diameter of center pole of the core. $D_{cp}$ ≈ 2 cm

$$\sum l_g = 4\pi \cdot 10^{-7} \cdot 112^2 \cdot \frac{3.9}{1280} \cdot (1 + \frac{\sum l_g}{2})^2 \cdot 10^4$$
$$\sum l_g = 0.48 \cdot (1 + \frac{\sum l_g}{2})^2 \qquad (3.23)$$

In order to find the air gap value, equation 3.23 is solved. Total airgap value is find as $\sum l_g$ =1.33 cm. As the air-gap at the center leg of the E-shaped inductor is twice in width of the gaps at the side legs, the center gap will be thought as two gaps. Thus, in calculations it is assumed that the inductor has four air-gaps. Then the length of a single air gap is found as:

$$l_g = \frac{\sum l_g}{4} = \frac{1.33}{4} = 0.33cm$$

Properties of output inductor are summarized in Table 3.10.

**Table 3.10: Properties of the Output Inductor**

| | |
|---|---|
| Core Geometry & Material | E80/38/20 & Ferrite, N87 |
| Inductance (L) | 1.28 mH |
| Number Turns | 112 turns Φ1.7mm |
| Peak Flux Density ($B_{peak}$) | 0.3 Tesla |
| Core Losses ($P_{core}$) | 2.52 W |
| Copper Losses ($P_{CU}$) | 6.62 W |
| Total Losses | 9.14 W |
| Temperature Rise (ΔT) | 64°C |
| Air-gap | 3.3 mm |

## 3.6 Output Capacitor Selection

The minimum output capacitance required to maintain the output voltage ripple below the design target of $V_{out(rip)}$ is obtained by using the Equation 2.62. For 3% output ripple, $V_{out(rip)}$ = 350 x 0.03 = 10.5V and 6.8A inductor current ripple, output capacitor value is calculated as :

$$C_{out} = \frac{6.8}{8 \cdot 25000 \cdot 10.5} = 3.2\mu H$$

In our specific application, value of output capacitor directly affects the half wave rectified output voltage. Here, we obtained an initial capacitor value. The exact value of the capacitor will be determined in the following chapters.

## 3.7 Active Clamp Stage

As explained in section 2.2.7, voltage stress of the clamp switch is the same as the voltage stress of the main switch. Then maximum voltage stress of the clamp switch is 550V as calculated in section 3.5. Current stress of the clamp transistor is equal to the magnetizing current and it is calculated in section 3.4

as 0.8A. Since the current stress is very low, a power MOSFET with high on state resistance can be used as clamp transistor. IRFPC40 is used in the design. Its specifications are given in Table 3.11.

**Table 3.11: Specifications of Clamp Transistor**

| | |
|---|---|
| Manufacturer | IRF |
| Model | IRFPC40 |
| VDSS | 600 V |
| $I_D$ | 6.8 A |
| $R_{DSON}$ | 1.2 Ω |
| Qg | 60 nC |

Value of the active clamp capacitor is selected according to equation 2.42 and 2.43. To satisfy the condition given in equation 2.43, minimum clamp capacitor value is calculated for fs=25000Hz and $L_{MAG}$= 3.28 mH.

$$\frac{1}{2\pi \cdot \sqrt{L_{MAG} \cdot C_R}} < f_s$$

$$C_R > \frac{1}{4\pi^2 \cdot f_s^{\,2} \cdot L_{MAG}}$$

$$C_R > 12nF$$

In the design Cr =1μF is used. Capacitor voltage stress is calculated from equation 2.27. VIN$\cdot D$ product is constant, according to the equation the worst case voltage stress is obtained for the maximum duty ratio D=0.51. For this case $V_{IN}$=255V. Capacitor voltage stress is obtained as:

$$V_{CR} = \frac{0.51}{1-0.51} \cdot 255 \qquad V_{CR} = 265V$$

In the design, voltage rating of the used clamp capacitor is 400V.

## 3.8 Bridge Rectifier Selection

A bridge rectifier is required in order to rectify the AC input voltage. Voltage stress of the bridge rectifier is peak input voltage, 340V. For 1500W output power and 90% converter efficiency, RMS input current will be 8.33 A (1500/0.9/200). Here, minimum input voltage is used in order to calculate the worst case. Peak current of bridge rectifier will be $8.33 \cdot \sqrt{2} = 11.8$ A. Single-phase bridge rectifier with 30A rated current is selected. Its part number is VBO36. It is manufactured by IXYS. Datasheet is given in Appendix D.

RMS and average current of each diode is $I_{peak} \cdot 0.635$ and $I_{peak} \cdot 0.318$ [4]. Then RMS diode current is $11.8 \cdot 0.635$=7.5A and average diode current is $11.8 \cdot 0.318$=3.75A. From Equation 3.15, loss of each diode is calculated. From datasheet, $V_{TO}$=0.8V $r_T$=5.8mΩ, then power loss will be

$$P_{loss} = 0.8 \cdot 3.75 + 5.8 \cdot 10^{-3} \cdot 7.5^2$$

$$P_{loss} = 3.4W$$

In bridge rectifier, two diodes are always operating, then power loss of the bridge rectifier will be 2x3.4=6.8W.

## 3.9 Efficiency Analysis

Converter losses are summarized given in Table 3.12. Total converter loss is calculated as 81.6W. For 1500W output voltage efficiency of the converter is estimated to be 90.5%.

**Table 3.12: Converter Losses**

| | |
|---|---|
| Transformer losses from section 3.2 | 9.6 W |
| Transistor losses from section 3.3 | 38.6 W |
| Fast Diode losses from section 3.4 | 7.7 W |
| Inductor Losses form section 3.5 | 9.2 W |
| Bridge Rectifier Loses from section 3.8 | 6.8 W |
| Snubber Losses from Simulations | 75 W |
| Other losses, (power consumption of control circuit) | 10 W |
| Total Losses | 156.8 W |

## 3.10 Heatsink Analysis

Transistors, diodes and snubber resistors are placed on a single heat sink. The dimensions of the heat sink are 20 x 20 x 10 cm. Case to air thermal resistance of heat sink can be calculated from Equation 3.24 [12].

$$R = (\frac{0.8}{Volume})^{0.68} \quad ^{o}C/W \tag{3.24}$$

Form dimensions heatsink volume is calculated as 4 liters. Then, form equation 3.24, case to air thermal resistance is calculated as 0.33 $^{o}$C/W.

The equivalent thermal model of the heatsink with semiconductor devices is given in Figure 3.10. TO247 transistor package is used for semiconductor devices. R(J-C) is junction of case thermal resistance of the TO-247 package, it is given as 0.5 $^{o}$C/W in datasheets (see Appendix D). R(C-A) is the case to ambient thermal resistance of the heat sink. The devices are connected to the heatsink with thermal pads. The connection resistances of the pads are ignored in the model.

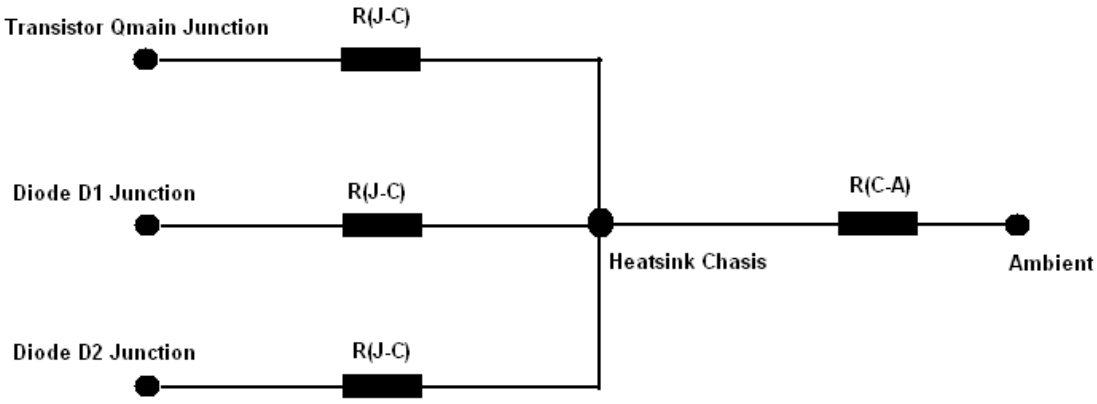



**Figure 3.10: Equivalent Thermal Model of Heatsink and Semiconductor Devices**

Total power dissipation of the heatsink can be obtained from Table 3.12. It is 75W+38.6W+7.7W=121.3 W. Since the case to ambient thermal resistance of the heatsink is R(C-A)= 0.33 $^{o}$C/W, its temperature rise for 121.3W is 40$^{o}$C. For 30$^{o}$C ambient temperature, heatsink temperature will be 40$^{o}$C.

Among the semiconductor devices, power dissipation of the main transistor is the highest one. For this reason, here we will calculate the junction temperature of this device only. We can say that junction temperature of diodes will be lower. Power dissipation of main transistor is obtained as 38.6 W in section 3.3. Since the junction to case thermal resistance is R(J-C)=0.5 $^{o}$C/W. For 38.6W, temperature difference between case and junction will be 19.6 $^{o}$C. Since heatsink temperature is calculated as 70$^{o}$C, then transistor junction temperature will be 89.6 $^{o}$C. Its less then 125 $^{o}$C, maximum operating junction temperature.

## 3.11 Small Signal Analysis

Converter regulates the output voltage by adjusting the duty ratio using a negative feedback loop. If the loop is not stable, converter oscillates. In order to

ensure that the converter is stable, and has an adequate transient response, the closed loop response should have a minimum phase margin of $45^{o}$ under all line and load conditions [11]. This is accomplished by shaping the open loop response using a compensator circuit. In order to obtain the open loop response of the converter, small signal model of the converter is used.

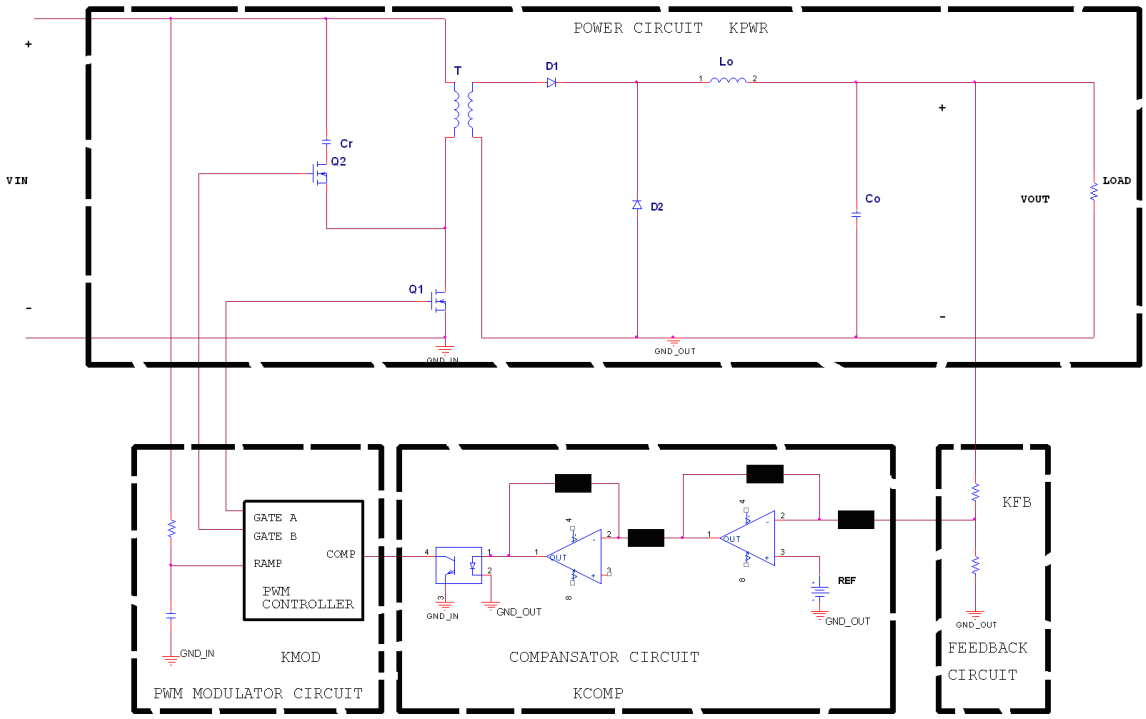



**Figure 3.11: Hardware Implementation of Transfer Functions**

Converter with control circuits is given in Figure 3.11. This circuit contains following transfer functions:

$K_{PWR}$ : Transfer function of the converter's power stage

$K_{FB}$ : Transfer function of feedback circuit

$K_{COMP}$ : Transfer function of the compensator circuit

$K_{MOD}$ : Transfer function of PWM modulator

Small signal model of of the system is given in Figure 3.12.

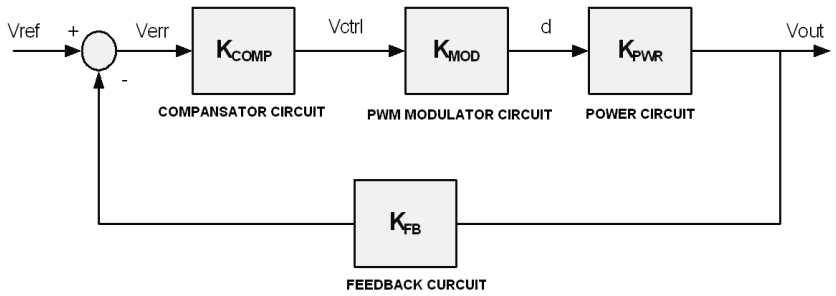



**Figure 3.12: Small Signal Model of A Voltage Controlled Converter**

In the following section, transfer functions of the power stage $K_{PWR}$, feedback circuit $K_{FB}$ and modulator circuit $K_{MOD}$ is derived. In the following sections, these transfer functions are derived.

### 3.11.1 Transfer Function of the Power Stage

Transfer function of the power stage ($K_{PWR}$) is obtained by averaging and linearizing the power circuit of the converter. In reference [14], transfer function of a buck converter is derived with this method. Here we derive transfer function of forward converter by the same way.

The concept of averaging is applied when the switching rate is fast with respect to the rate of change of any other parameters of interest. The accuracy of the approximations is excellent up to one-tenth of the switching frequency. The process of averaging the operation of the circuit is given in Figure 3.13. In Figure 3.12(a), the condition when the main switch ON is given. N is the turns ratio of

the power transformer used in the power circuit. d is the duty cycle of the converter. Load current is supplied by input voltage source over the power transformer.

The condition when the main switch is OFF is given in Figure 3.13(b). Load current is supplied by the energy stored in output inductance. The relationship between these two conditions is the duty cycle. Effect of the duty cycle to the output voltage is modeled with a hypothetical DC transformer (shown in Figure 3.13(c)). Note that, the transformer is not the isolation transformer used in actual circuit. Here, the DC transformer is a conceptual transformer, it is used for obtaining a continuous model of the converter.

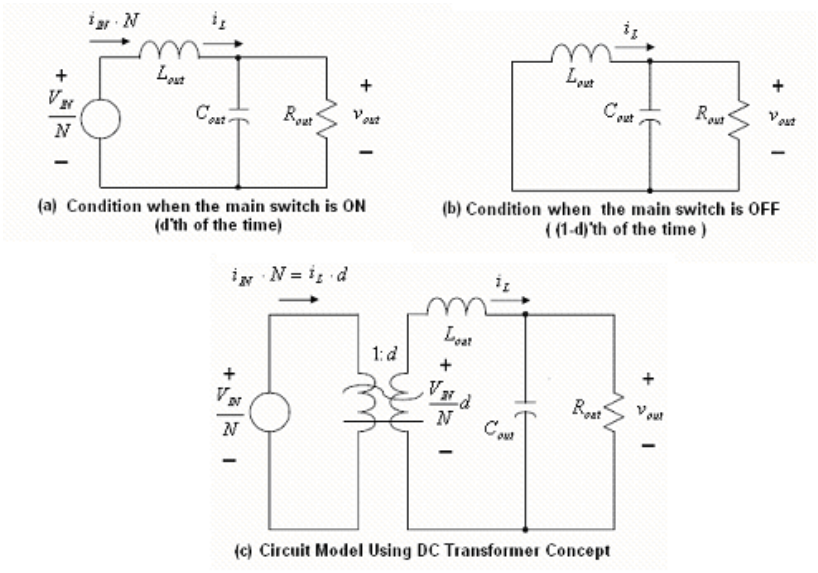



**Figure 3.13: Averaged Forward Converter**

The averaged system is now a nonlinear continuous system. The nonlinearity of the system comes from the DC transformer's turns ratio d. It is the control variable of the system, and is not constant.

After obtaining the averaged continuous model of the converter, linearizing this model is the next step. In order to linearize the model, small signal parameters is defined based on a large signal operating point. The linearization process involves separating each variable into its DC and signal frequency, AC, components. In the following equations, DC components are shown in capitals while AC components are shown with caps symbol. Product of two ac components is neglected in calculations.

$$i_L = I_L + \hat{i}_L \tag{3.25}$$

$$d = D + \hat{d} \tag{3.26}$$

$$\begin{aligned} V_{IN} \cdot d &= V_{IN} \cdot (D + \hat{d}) \\ &= V_{IN} \cdot D + V_{IN} \cdot \hat{d} + \hat{v}_{IN} \cdot \hat{d} \\ &= V_{IN} \cdot D + V_{IN} \cdot \hat{d} \end{aligned} \tag{3.27}$$

$$\begin{aligned} i_L \cdot d &= (I_{IN} + \hat{i}_L) \cdot (D + \hat{d}) \\ &= i_L \cdot D + I_L \cdot \hat{d} + \hat{i}_L \cdot \hat{d} \\ &= i_L \cdot D + I_L \cdot \hat{d} \end{aligned} \tag{3.28}$$

From Figure 3.13(c) and Equations (3.27) and (3.28), linearized (small signal) model of the converter is obtained as given in Figure 3.14.

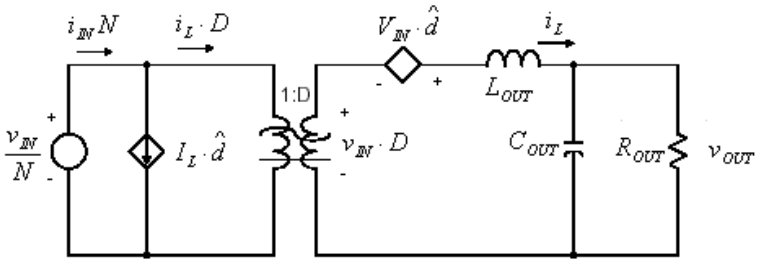



**Figure 3.14: Linearized Forward Converter**

In Figure 3.14, from the secondary side of the DC transformer, we can write the following two equations:

$$\frac{V_{IN}}{N} \cdot \hat{d} = L_{OUT} \cdot \frac{di_L}{dt} + v_{OUT} \tag{3.29}$$

$$i_L = C_{OUT} \cdot \frac{dv_{OUT}}{dt} + \frac{v_{OUT}}{R_{OUT}} \tag{3.30}$$

By combining Equation 3.29 and 3.30 we obtain following equation:

$$\frac{V_{IN}}{N} \hat{d} = L_{OUT} \cdot C_{OUT} \cdot \frac{d^2 v_{OUT}}{dt^2} + \frac{L_{OUT}}{R_{OUT}} \cdot \frac{dv_{OUT}}{dt} + v_{OUT} \tag{3.31}$$

By writing Equation (3.31) in s-domain, transfer function $K_{PWR}$ is obtained as given in Equation (3.32).

$$K_{PWR} = \frac{v_{OUT}}{\hat{d}} = \frac{V_{IN} / N}{L_{OUT} \cdot C_{OUT} \cdot s^2 + \frac{L_{OUT}}{R_{OUT}} \cdot s + 1} \tag{3.32}$$

Here, $V_{IN}$ is the input voltage, $L_{out}$ is the output inductor, $C_{out}$ is the output capacitor, N is the turns ratio of the isolation transformer and $R_{out}$ is the load resistance.

### 3.11.2 Transfer Function of the Feedback Circuit

Transfer function of the feedback circuit $K_{FB}$ is dependent to the reference voltage level as given in Equation (3.33).

$$K_{FB} = \frac{V_{REF}}{V_{OUT}} \tag{3.33}$$

Here, Vref is the reference voltage applied to the compensator circuit, and $V_{OUT}$ is the output voltage.

### 3.11.3 Transfer Function of the Modulator Circuit

Conventional PWM modulators compare the control signal $V_C$ with fixed amplitude saw tooth signal and generates the switching signal, as given in Figure 3.15. Transfer function of a conventional PWM modulator is given in Equation (3.34). $V_S$ is the amplitude of the saw-tooth signal.

$$\frac{d}{V_C} = \frac{1}{V_S} \tag{3.34}$$

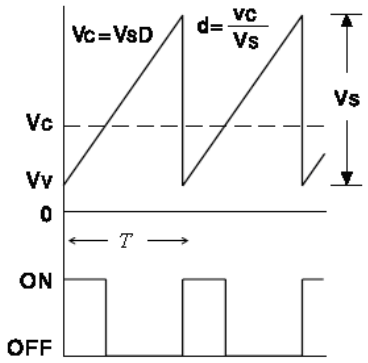



**Figure 3.15: Conventional PWM Waveforms**

In this thesis, feed forward is used with PWM modulator, so transfer function of the modulator is different from conventional PWM modulator. In order to derive the transfer function KMOD, operation of the PWM controller, LM5025A is investigated. In this controller, ramp (sawtooth) signal is generated by the charging of the external $C_{FF}$ capacitor over $R_{FF}$ resistor from the voltage $V_I$ (see Figure 3.16). Since the maximum voltage of the controller can be 90V, input voltage is not directly applied to the converter. A $V_I$ voltage is obtained from the input voltage $V_{IN}$, and applied to the PWM controller's input voltage pin. When the signal at the ramp pin reaches 2.5 Volts, it is internally terminated by the controller. Charging cycle is restarted within every switching period. The slope of the ramp signal is dependent to the input voltage.

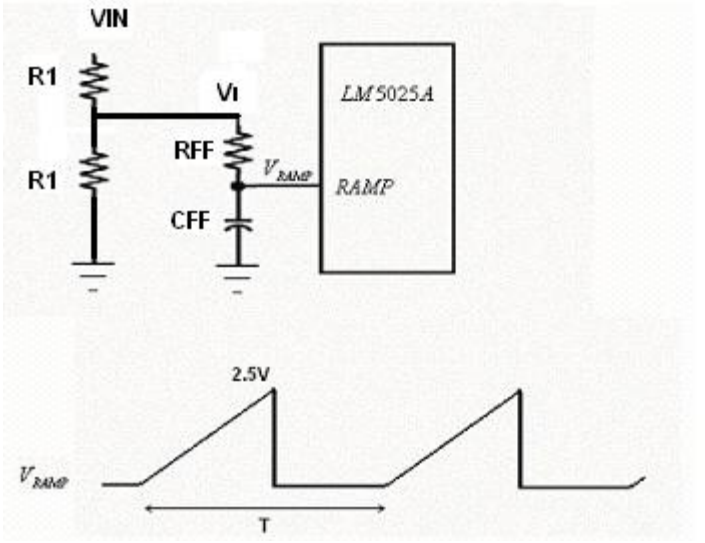



**Figure 3.16: Generation of Ramp Signal in the LM5025A Controller**

While the capacitor $C_{FF}$ is charging, ramp voltage is expressed with the Equation (3.35), where $\tau$ is the time constant $\tau = R_{FF}C_{FF}$ .

$$V_{RAMP} = V_I (1 - e^{-t/\tau}) \tag{3.35}$$

For $t << \tau$ , it can be rewritten as:

$$V_{RAMP} = V_I \frac{t}{\tau} \tag{3.36}$$

In Figure 3-17, the ramp signal is given. From this figure duty cycle *d* can be written as given in the following equation:

$$d = \frac{t_{ON}}{T} = \frac{V_C}{V_P} \tag{3.37}$$

$V_C$ is the control voltage, output of the compensator circuit. $V_S$ is the ramp voltage for t=T. Actually, ramp signal is terminated by the controller when it reaches 2.5V level. $V_S$ voltage is used in order to calculate the transfer function of the modulator circuit. From Equation (3-36), Vs voltage is obtained as:

$$V_S = V_I \frac{T}{\tau} \tag{3.38}$$

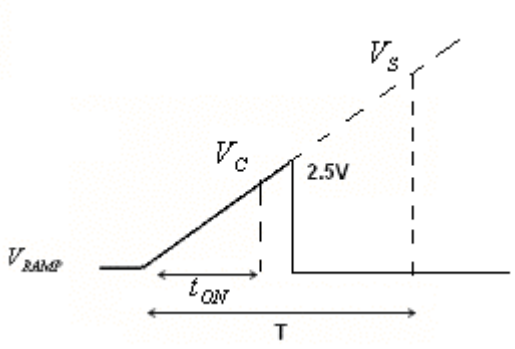



**Figure 3.17: PWM Ramp Signal**

From Equations (3.38) and (3.39), transfer function of the modulator circuit $K_{MOD}$ is written as:

$$K_{MOD} = \frac{d}{V_C} = \frac{1}{V_S} = \frac{\tau}{V_I \cdot T} \tag{3.39}$$

Transfer function of the PWM modulator is dependent to the input voltage due to the feed forward mechanism used with the modulator.

### 3.11.4 Uncompensated Open Loop Transfer Function

The open loop transfer function is defined as the product of the transfer functions around the entire feedback loop, whether the loop is actually open or closed [11]. In this thesis, we define open loop transfer function without compensator stage as uncompensated open loop transfer function, $T_{UC}$. Then its expression is obtained with the product of power, feedback and modulator stage as given in Equation (3.40).

$$T_{UC} = K_{PWR} \cdot K_{FB} \cdot K_{MOD} \tag{3.40}$$

By wiritng the transfer functions obtained in previous chapters, uncompensated open loop transfer function $T_{UC}$ is obtained as given in Equation (3.41).

$$T_{UC} = K_{PWR} \cdot K_{FB} \cdot K_{MOD}$$

$$T_{UC} = \frac{V_{IN} / N}{L_{OUT} \cdot C_{OUT} \cdot s^2 + \frac{L_{OUT}}{R_{OUT}} \cdot s + 1} \cdot \frac{V_{REF}}{V_{OUT}} \cdot \frac{\tau}{V_I \cdot T} \tag{3.41}$$

- $V_{OUT}$ is the output voltage, $V_{OUT}$= 350 V
- $V_{REF}$ is the reference voltage of the feedback circuit, $V_{REF}$= 6 V
- T is the switching period of the converter, T=40μs, (for 25 kHz)

- N is the turns ratio of the transformer, N=3.
- $L_{OUT}$ is the output inductor of the converter circuit, $L_{OUT}$= 1.28 mH.
- $C_{OUT}$ is the output capacitor of the converter circuit, $C_{OUT}$= 3.2 µF.
- $R_{OUT}$ is the load resistance, for %20 LOAD $R_{OUT}$=200Ω.
- $\tau$ is the time constant of he feed forward circuit, $\tau = R_{FF}C_{FF}$.
- $V_I$ is the voltage applied input pin of the controller. $V_I$= 26V

Time constant of the feed forward circuit is determined by investigating the volt-second clamp feature of the LM5025A controller. Since the volt-second comparator terminates the ramp voltage at 2.5V level, then maximum turn on time is determined by the time constant of the feed forward circuit as given in Equation (3.42).

$$\tau = \frac{V_{IN} \cdot t_{ON(MAX)}}{2.5} \qquad (3.42)$$

Since $t_{ON(MAX)} = \frac{D_{MAX}}{f_S}$, where $D_{MAX}$ is the maximum duty ratio and $f_S$ is the switching frequency, Equation (3.42) can be rewritten:

$$\tau = \frac{V_I \cdot D_{MAX}}{2.5 \cdot f_S} \qquad (3.43)$$

Maximum duty ratio is set to 0.51. For $D_{MAX}$=0.51, $V_I$=26V and $f_S$ =25 kHZ, time constant of the feed forward circuit is calculated as $\tau$ = 228 µs.

From Equation (3.41), uncompensated open loop transfer function is calculated as given in Equation 3.34.

$$T_{UC} = \frac{V_{IN}/N}{L_{OUT}\cdot C_{OUT}\cdot s^2 + \frac{L_{OUT}}{R_{OUT}}\cdot s + 1}\cdot\frac{V_{REF}}{V_{OUT}}\cdot\frac{\tau}{V_I\cdot T}$$

$$T_{UC} = \frac{300/3}{1.28\cdot10^{-3}\cdot3.2\cdot10^{-6}s^2 + \frac{1.28\cdot10^{-3}}{200}\cdot s + 1}\cdot\frac{6}{350}\cdot\frac{228\cdot10^{-6}}{26\cdot40\cdot10^{-6}}$$

$$T_{UC} = \frac{0.388}{4.096\cdot10^{-9}s^2 + 6.4\cdot10^{-6}\cdot s + 1} \qquad (3.44)$$

Bode diagram of the transfer function $T_{UC}$ is given in Figure 3.18. It has a resonance frequency at about 2.36 kHz. Its gain is below 0 dB. According to the Nyquist Stability Criteria, if the open-loop gain crosses 1 (0 dB) only once, the system is stable if the phase lag at the crossover frequency, is less than 180°. If the phase lag at the cut off frequency is only a few degrees less than $180^o$, then the system is stable, but will exhibit considerable overshoot and ringing. A phase margin of $45^o$ provides for good response with a little overshoot [11]. Then, in our design, compensator stage should be used in order to increase the gain and adjust the phase margin. Out target is obtaining a phase margin of about $45^o$ in order to guarantee the stability of design.

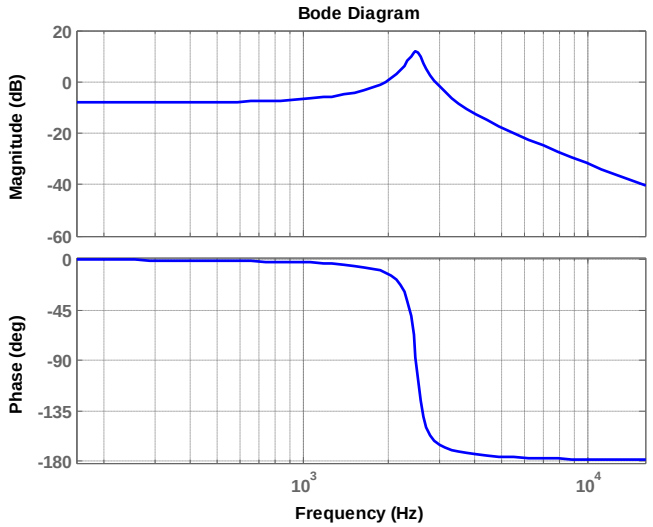



**Figure 3.18: Bode Diagram of the Uncompansated Open Loop Transfer Function**

### 3.11.5 Compensator Design

In the previous sections, it is concluded that a compensator stage is needed in order to increase the gain and adjust the phase margin to $45^{o}$ for stability. In this section, transfer function of the compensator stage will be obtained.

Cut off frequency ($f_C$) of the compensated open loop must be determined. As a rule of thumb, it is said hat open loop function must have attenuation at switching frequency large signal stability [14]. So, cut-off frequency must be sufficiently smaller than the switching frequency ($f_C$<25 kHz). Moreover, in order to obtain fast dynamic response cut off frequency must be greater then the resonant frequency of the converter., $f_C$ >2.36 kHz. Then, cut-off frequency of the compensated open loop is selected to be $f_C$ = 5 kHz.

In order to increase the phase margin at the cut-off frequency, a zero is required at $f_C$=5kHz. Open loop transfer function must have a high gain at low frequencies to suppress the low frequency components at the input voltage. So, compensator must have a pole at origin and a zero at low frequencies. Pole at

the origin is achieved by integrator component, then compensator must have a integrator component. The low frequency zero is placed at $f_C/10$, 500 Hz. Gain of the uncompensated open loop at 5 kHz is -18 dB (see Figure 3.18). Then the gain of the error amplifier at 5 kHz must be 18 dB, in order to have a unity gain at the cut-off frequency of the compensated open loop transfer function.

Design of the compensator stage is summarized below:

I. Compensator has a zero at $f_C$ = 5 kHz.

II. Compensator has a zero at $f_C$ /10 =500 Hz.

III. Compensator has an integrator component.

IV. Compensator has a 18 dB gain at 5 kHz. Then $\left|K_{COMP}\right| = 7.95$

Transfer function having two zeros at 500 HZ and 5000 Hz with a pole at the origin is given in Equation 3.45 [14]. It satisfies the first three requirements given above.

$$K_{COMP}(s) = \frac{A \cdot (1 + \frac{s}{2\pi \cdot 500})(1 + \frac{s}{2\pi \cdot 5000})}{s} \qquad (3.45)$$

In order to satisfy the fourth condition, the constant A must be obtained. It is calculated from the condition given in equation 3.46.

$$\left|K_{COMP}(s)\right| = 7.95 \quad for \quad s = 2 \cdot \pi \cdot 5000 \qquad (3.46)$$

$$\frac{A \cdot \left|1 + \frac{2\pi \cdot 5000 \cdot j}{2\pi \cdot 500}\right| \cdot \left|1 + \frac{2\pi \cdot 5000 \cdot j}{2\pi \cdot 5000}\right|}{2\pi \cdot 5000} = 7.95$$

$$A = 17700$$

In hardware implementation, compensator circuits have an extra pole at high frequencies [11]. As a first approximation, this pole is assumed to at 100 kHz, sufficiently bigger then the cut off frequency. With this high frequency pole, transfer function of the compensator stage is rewritten as given in Equation (3.47).

$$K_{COMP}(s) = \frac{17700 \cdot (1 + \frac{s}{2\pi \cdot 500}) \cdot (1 + \frac{s}{2\pi \cdot 5000})}{s \cdot (1 + \frac{s}{2\pi \cdot 100000})} \qquad (3.47)$$

$$K_{COMP}(s) = \frac{1.79 \cdot 10^{-4} \cdot s^2 + 6.197s + 17700}{1.592 \cdot 10^{-6} \cdot s^2 + s} \qquad (3.48)$$

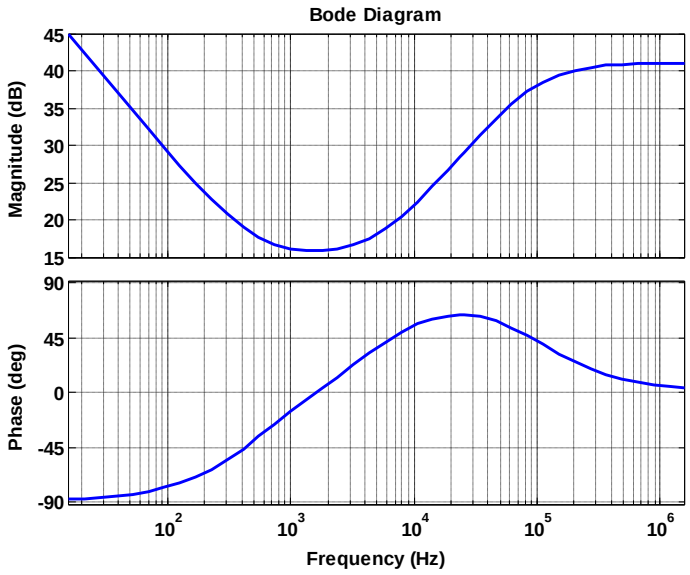



**Figure 3.19: Bode Diagram of the Compensator (Error Amplifier)**

Bode diagram of the compensator in equation 3.47 is given in figure 3.19. As desired, compensator have two zeros, at 500 Hz and 5 kHz and two poles, at

the origin and at 100 kHz. Gain of the compensator at 5 kHz is 18 dB. Phase response of the compensator at 25 kHz is 45 degrees, due to the zero placed at this frequency.

WE can now calculate the compensated open loop function to examine the presence of stability condition. As given in Equation 3.49, compensated open loop transfer function is the product of uncompensated open loop transfer function with compensator transfer function. Compensated open loop transfer function is given in Equation 3.50. Its bode diagram is given in Figure 3.20, with the bode diagram of uncompensated open loop and compensator transfer functions.

$$T_C = T_{UC} \cdot K_{COMP} \tag{3.49}$$

$$T_C = \frac{6.95 \cdot 10^{-5} \cdot s^2 + 2.407 \cdot s + 6874}{6.5 \cdot 10^{-15} \cdot s^4 + 4.10 \cdot 10^{-9} \cdot s^3 + 7.99 \cdot 10^{-6} \cdot s^2 + s} \tag{3.50}$$

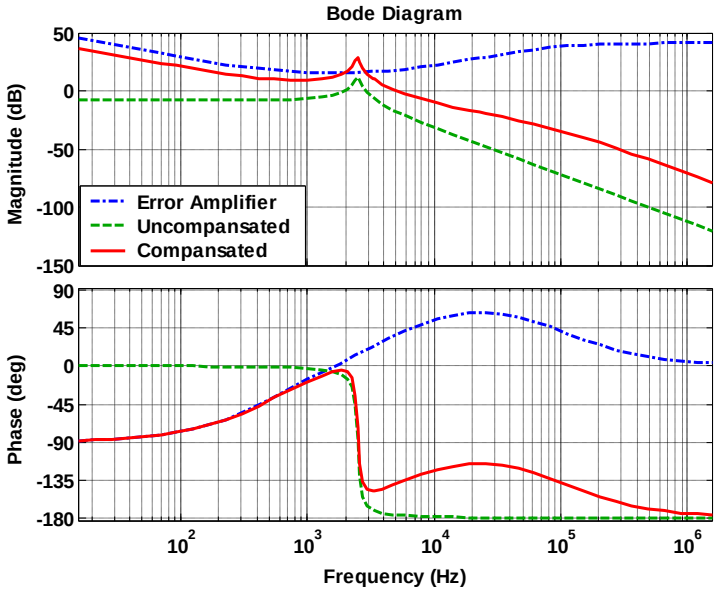



**Figure 3.20: Bode Diagrams of Uncompensated and Compensated Open Loop and Error Amplifier**

According to Figure 3.20, compensated open loop transfer function has cut-off frequency at 5 kHz. We need a phase margin about 45 at this point in order to guarantee the stability. From figure phase margin is obtained as approximately 45 degrees. Moreover, we need gain at low frequencies in order to suppress the low frequency components on the input voltage. From figure, it can be observed that compensated open loop gain is increased at low frequencies.

### 3.11.6 Compensator Circuit Design

In the previous sections, transfer function of the compensator stage is obtained. In this section, circuit design of the compensator stage is presented. In Figure 3.21, a conventional voltage error amplifier circuit, its bode plot and equations are given [11].

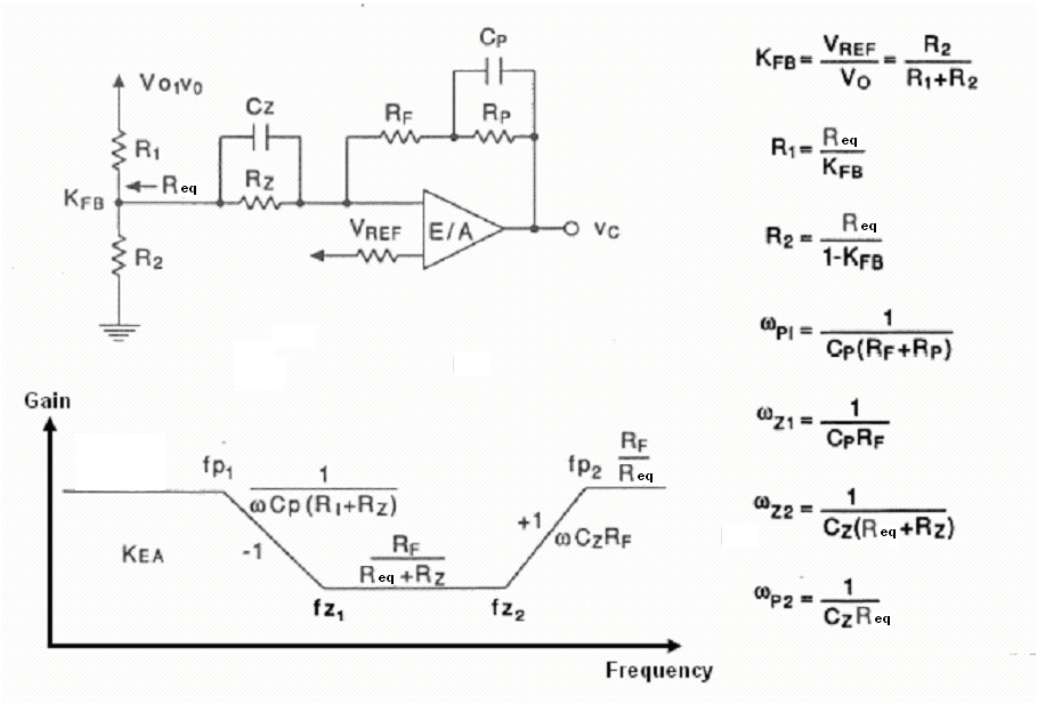



**Figure 3.21: A Conventional Voltage Error Amplifier (EA) Circuit with Bode Plot and Equations**

In error amplifier circuit given in figure 3.21, capacitor $C_P$ and resistor $R_F$ determines the first zero of the compensator circuit. Second zero is obtained form $C_Z$, $R_I$ and $R_Z$. R1 and R2 perform the feedback circuit. Resistors $R_F$, Req and $R_Z$ determine the compensator gain at zero frequencies.

Error amplifier circuit must have a zero at 500 Hz. Then $f_{z1}$=500 Hz. Values of $C_P$ and $R_F$ are calculated from Equation 3.51.

$$f_{z1} = \frac{1}{2\pi \cdot C_P \cdot R_F} = 500 \tag{3.51}$$

For $C_P$=10 nF, $R_F$= 31.8 kΩ

From the feedback circuit transfer function $K_{FB}$, values of $R_1$ and $R_2$ resistors are calculated as given in Equation 3.52:

$$K_{FB} = \frac{V_{REF}}{V_{OUT}} = \frac{R_2}{R_2 + R_1} \tag{3.52}$$

$$R_{eq} = \frac{R_1 \cdot R_2}{R_1 + R_2} \tag{3.53}$$

For $V_{REF}$=6, $V_{OUT}$=350V and $R_2$=1.7 kΩ, $R_1$ is calculated as $R_1$=97.4 kΩ. Then from Equation (3.53) $R_{eq}$, the equivalent resistance of the feedback circuit, is calculated as $R_{eq}$= 1.67 kΩ.

In the previous section, gain of the compensator ($V_{ctrl}/V_{err}$) at zero frequencies is obtained as 18dB, thus 7.95. Then $R_F$ is calculated from Equation 3.54.

$$\frac{R_F}{R_{\text{eq}} + R_Z} = 7.95 \tag{3.54}$$

For $R_F$=31.8 kΩ and $R_{eqI}$=1.67 kΩ, $R_Z$ is calculated as $R_Z$=2.33 kΩ.

Error amplifier circuit has a zero at 5 kHz. Then $C_Z$ is calculated from Equation 3.55.

$$f_{z1} = \frac{1}{2\pi \cdot C_z \cdot (R_{eq} + R_F)} = 5000 \qquad (3.55)$$

For $R_{eq}$=1.67 kΩ, $R_Z$=2.33 kΩ, $C_Z$ is calculated as $C_Z$ = 8 nF.

Since error amplifier has a pole at the origin, then $f_{p1}$=0. According to Equation 3.56, this is accomplished by the infinity value of the resistor $R_P$; it is open circuit.

$$f_{p1} = \frac{1}{2\pi \cdot C_P \cdot (R_P + R_F)} \qquad (3.56)$$

In the error amplifier circuit, *National Semiconductor's LM258* type number operational amplifier is used. Its unity gain bandwidth is 1 MHz. Compensator circuit is given in Figure 3.22.

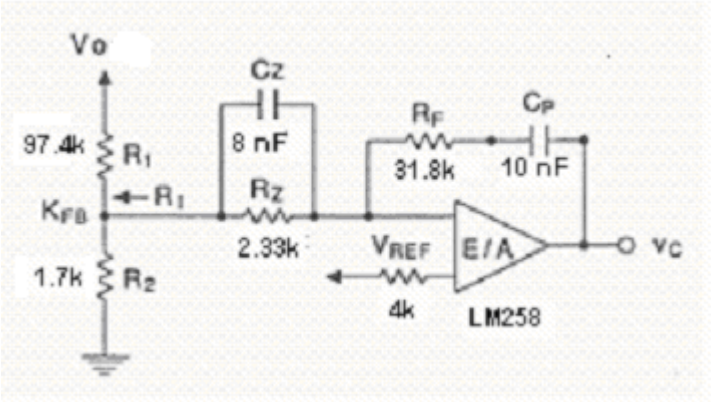



**Figure 3.22: Compensator Circuit**

## 3.12 Simulation of the Designed Circuit

In this section, our goal is verifying the designed SMPS. We will investigate the device stresses with PSPICE simulations. ORCAD version 15.7 is used for this purpose. In the simulations real model of the selected diodes and transistors are used. E80/38/20, 3C90 core model is used for the transformer (3C90 material is the cross reference of N87). In simulations, a rectified sinusoidal reference voltage is applied to the error amplifier circuit. The model of the PWM stage of the controller (LM5025A) is generated and used in simulations. Reference signal is obtained from a ideal sinusoidal voltage source. Absolute value of the sinusoidal signal is used for the half wave sine rectified reference signal. Here, ideal simulation model is used for reference signal. Implementation of the reference signal is explained in the following sections.

Simulation models used in this section are given in Appendix-B. Simulation Settings are given in Appendix-C.

According to equations 2.28, 2.44 and 2.46, device stresses of the power semiconductors are dependent to the input voltage and duty ratio. The stresses appear in the lowest and highest input voltages. For this reason, simulations are performed at these conditions at full load in order to investigate the device stresses. In the design phase, device stresses are calculated for steady state conditions. Here in simulation section, we will investigate device stresses at both steady state and start-up conditions. First, circuit is simulated at the lowest input voltage, 200VAC. Then, input voltage is increased to its highest value, 240VAC.

### 3.12.1 Simulations at the Lowest Input Voltage

200 VAC rms input voltage is applied to the bridge rectifier. 1500W linear load is connected to the output. A full wave rectified sinusoidal reference signal at 100Hz is applied to the error amplifier stage. A full wave rectified output voltage waveform is obtained at the output of the converter. As is given in Figure 3.23.

The waveform contains start-up and steady state conditions. Start-up is the transient operation time during the output capacitor and inductor settles their steady state voltages and currents. In the first half cycle, converter is starting up at t=0. Some distortions at the output voltage is seen at start up interval until t=2ms. After start up interval distortions disappear. Amplitude of the output voltage is 350V. Its frequency is 100 Hz. Note that, frequency of this voltage will be 50 Hz after inverted at the final stage. Investigation of operation of the converter with the inverter will be performed in the next chapter.

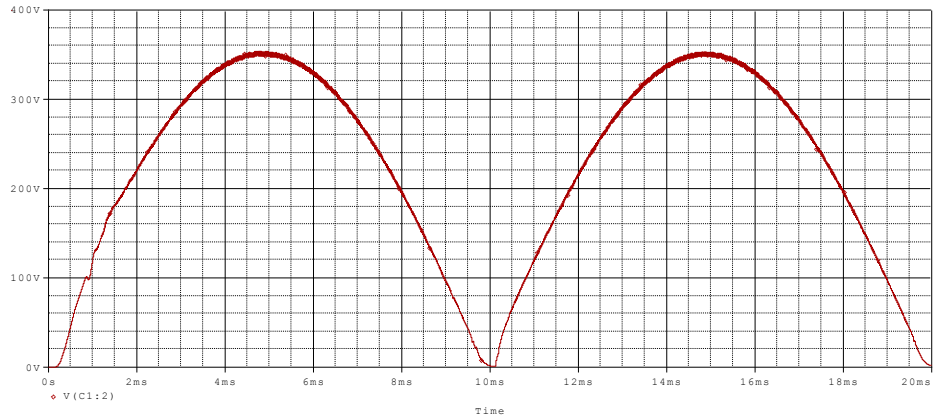



**Figure 3.23: Output Voltage at the Lowest Input Voltage**

In the design section, voltage stress for the main transistor at the lowest input voltage is calculated as 530V for steady state conditions. Voltage stress of the main transistor is given in Figure 3.24. It is seen that maximum voltage stress of the transistor is obtained in the first half cycle during start-up; it is 550V. In the next half cycle maximum transistor, in steady state, voltage stress reduces to 530V level, as calculated. At the lowest input voltage, both start-up and steady state voltage stresses of the main transistor are below 600V; therefore, the rated voltage of the selected transistor appears to be correct.

In the output voltage, there is a ripple component. It is converter's output ripple in switching frequency. This ripple affects the total harmonic distortion (THD) of the output voltage. In this section, THD is not investigated.

Voltage stress of the diode D1 is given in Figure 3.26. During steady state voltage, stress is maximum 1000V; it is below 1200V, incompliance with the rating of the selected diode. Note that this value is calculated as 795V in the design section. The reason of the difference is the voltage spikes. As given in Figure 3.26, voltage spikes occur in each rising edge of the diode voltage. The reason of theses spikes are the resonance of the diodes parasitic capacitances with transformer leakage inductance. These spikes are limited by to the case given in Figure 3.26 by using RC snubber circuit. Values of the snubber elements are determined by simulations. As given in the circuit model in Appendix-C, snubber values are R=1kΩ and C=1nF. Snubber circuits limit the voltage spike to an acceptable value, however these circuits causes 75 W total power loss.

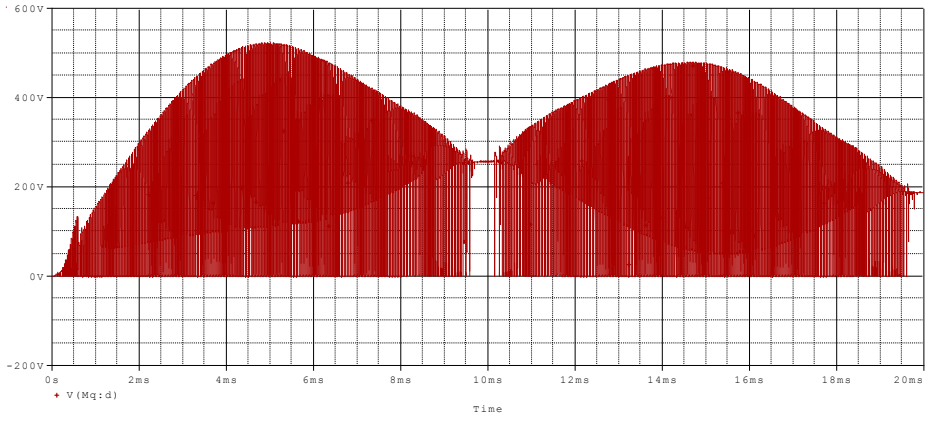



**Figure 3.24: Transistor Voltage Stress at the Lowest Input Voltage**

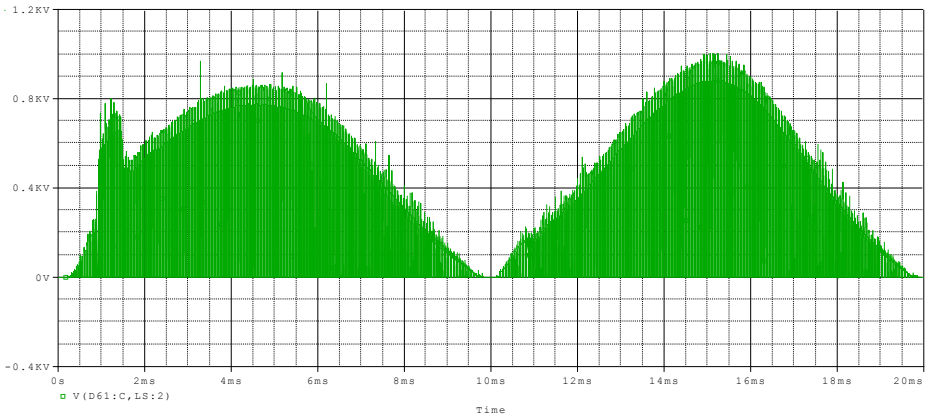



**Figure 3.25: Voltage Stress of Diode D1 at the Lowest Input Voltage**

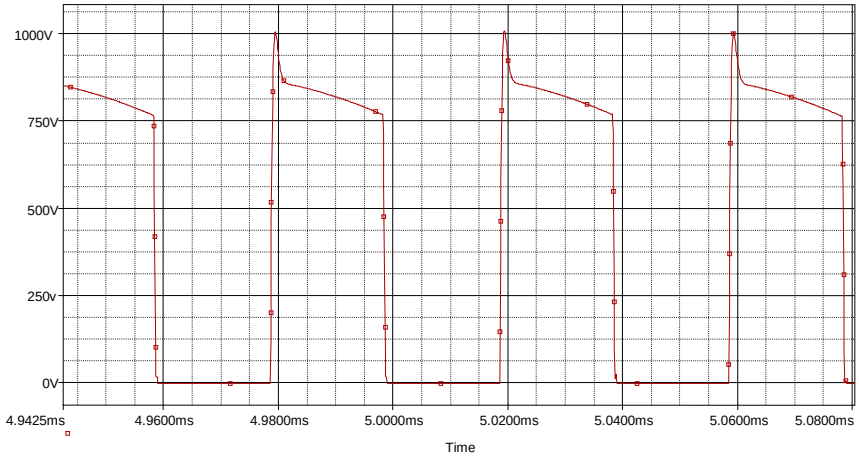



**Figure 3.26: Voltage Stress of Diode D1 in Large Scale**

Voltage stress of the diode D2 is given in Figure 3.27. During steady state voltage, stress is maximum 800V, it is below 1200V; therefore the rated voltage of the selected diode appears to be correct. Diode D2 voltage stress is calculated as 795V in the design section.

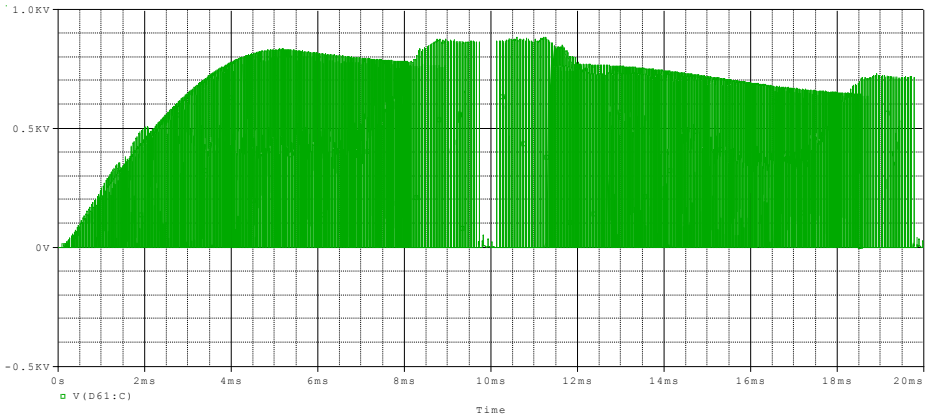



**Figure 3.27: Diode D2 Voltage Stress at the Lowest Input Voltage**

### 3.12.2 Simulations at the Highest Input Voltage

240 VAC rms input voltage is applied to the bridge rectifier. 1500W linear load is connected to the output. A full wave rectified sinusoidal reference signal at 100Hz is applied to the error amplifier stage. A full wave rectified output voltage waveform is obtained at the output of the converter. It is given in Figure 3.28. The waveform contains start-up and steady state conditions. In the first half cycle, converter is starting up at t=0. Some distortions at the output voltage is seen at start up interval until t=2ms. After start up interval distortions disappear. Amplitude of the output voltage is 350V. Its frequency is 100 Hz.

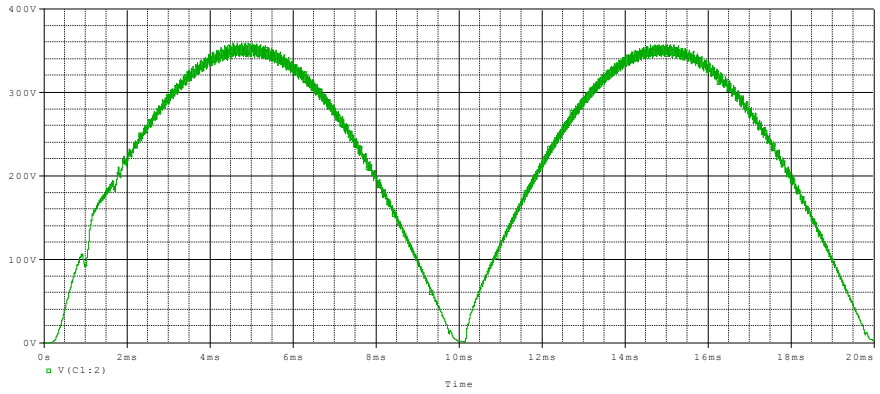



**Figure 3.28: Output Voltage at the Highest Input Voltage**

Voltage stress of the main transistor is given in Figure 3.29. Maximum voltage stress of the transistor is 550V, as calculated in the design section. It is below 600V the voltage rating of the selected transistor.

Ripple component of the output voltage is increased because for highest input voltage, minimum duty cycle D is obtained. According to Equations 2.28 and 2.44, voltage ripple is proportional to 1-D. Decrease in duty cycle D causes increase in the output voltage ripple.

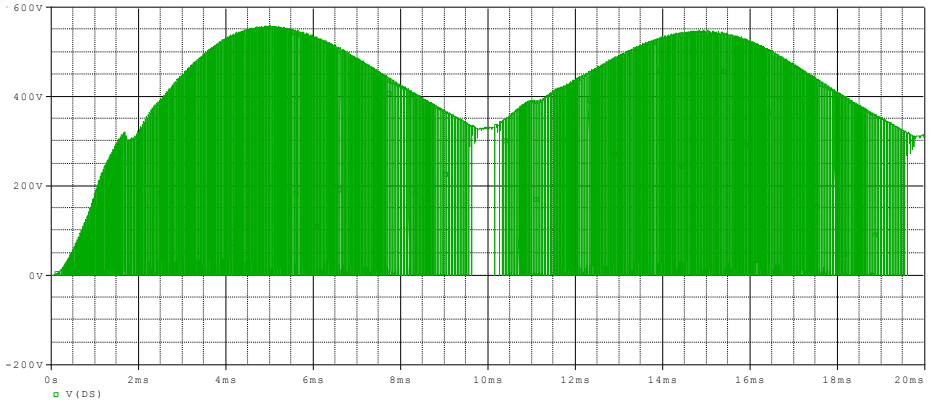



**Figure 3.29: Transistor Voltage Stress at the Highest Input Voltage**

Voltage stress of the diode D1 is given in Figure 3.30. Maximum voltage stress of the diode D1 is 800V. It is calculated as 660V in the design section. As explained in the previous section the reason of the difference is the voltage spikes. Voltage stress of the diode D2 is given in Figure 3.31. Maximum voltage stress of the diode D2 is 1000V, as calculated in the design section. Voltage stresses of both diodes D1 and D2 are below 1200V, the rating of the selected transistor.

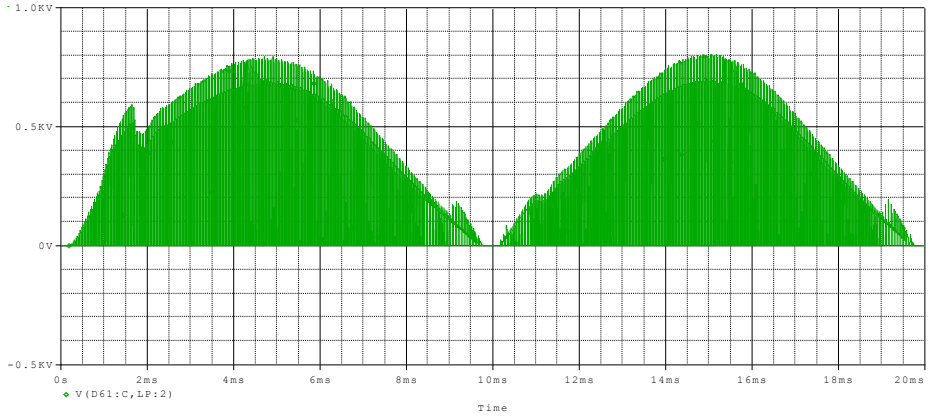



**Figure 3.30: Diode D1 Voltage Stress at the Highest Input Voltage Simulation**

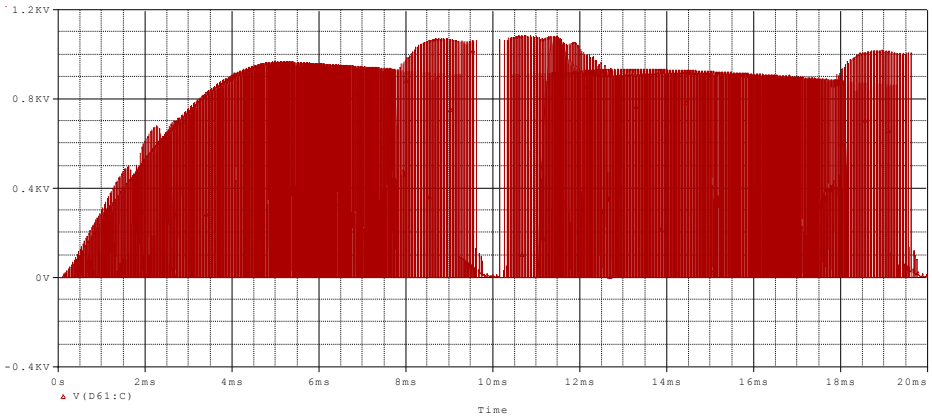



**Figure 3.31: Diode D2 Voltage Stress at the Highest Input Voltage Simulation**

## 3.13 Implementation of the Designed SMPS

In this section, implementation of the designed SMPS is explained. General view of the implemented SMPS is given in Figure 3.32. A power PCB (printed circuit board) is designed for implementation of the converter. Reference signal is generated in a microcontroller board and applied to the converter with a digital to analog converter (DAC). In order to guarantee the start-up of the converter at the starting of a half wave sine, start-up board is used.

In the following sections first, generation of the reference signal is presented. Then, start-up of the converter is given. Finally, design of the PCB is explained.

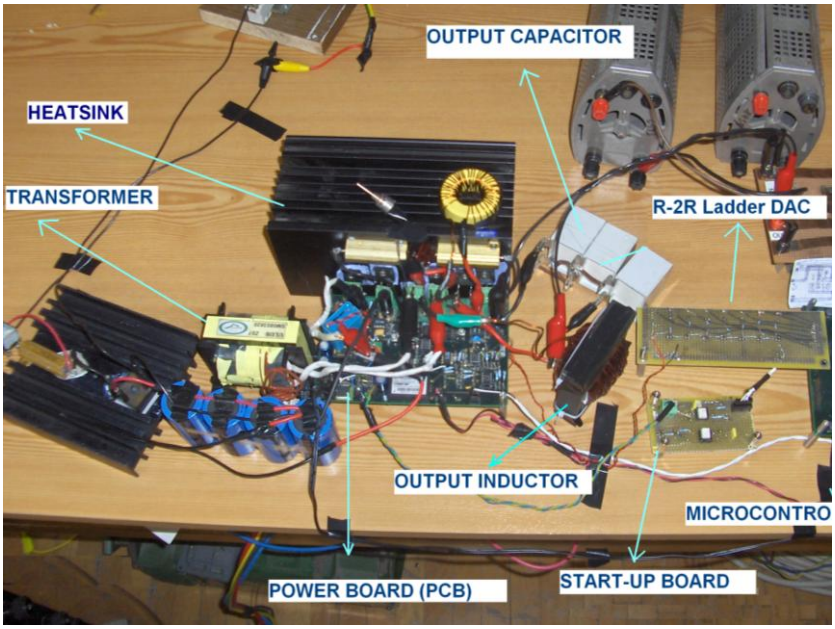



**Figure 3.32: General View of the Implemented SMPS**

### 3.13.1 Generation of the Reference Signal

A rectified sinusoidal reference signal is needed in order to obtain rectified sinusoidal output voltage. A microcontroller board used in order to generate the reference signal. Microcontroller board contains Microchip's 8 bit PIC18F458 controller IC. Specifications of the IC are given in Appendix-D. Micro controller board is given in Figure 3.33. It was designed by ASELSAN.

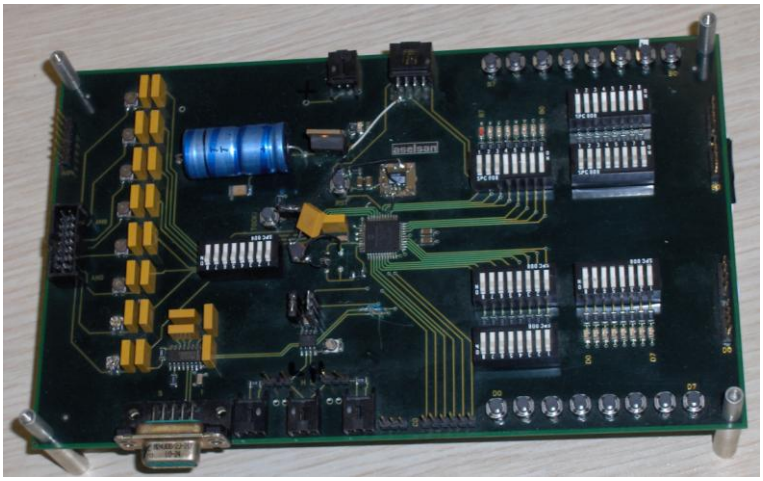


**Figure 3.33: Microcontroller Board Used in this Thesis**

In order to generate reference signal, 8 bit digital output of the controller is used. Waveform is defined as a look up table. Reference signal for one cycle is given in Figure 3.34. One half cycle is divided into 100 equal time pulses. Pulses are generated by using Timer0 interrupt sub routine. Duration of each pulse is the sum of interrupt delay and Timer0 delay. Interrupt delay is the delay time that is needed for the execution of one interrupt loop. It is dependent to the operations defined in the interrupt loop. Timer0 delay is the delay time of the Timer0 module. Timer0 delay is used in order to adjust frequency of the reference

signal. In order to obtain maximum frequency, Timer0 delay must be kept minimum. Interrupt delay limits the minimum pulse duration and so maximum frequency of the reference signal. Amplitude of the reference signal is adjusted by amplitude factor. When it is equal to 1, maximum value of the digital signal is $2^8$-1=255. Amplitude of the reference signal can be adjusted between Vout/5 , amplitude of digital reference signal is 21, and Vout, amplitude of digital reference signal is 21. Vout/5 can be obtained for 10 Hz, and Vout can becan be obtained for 50 Hz and above freqıencies.Output frequency can be adjusted between 10Hz and 100 Hz, with 0.6 Hz resolution. Flowchart and source code of the software is given in Appendix-E.

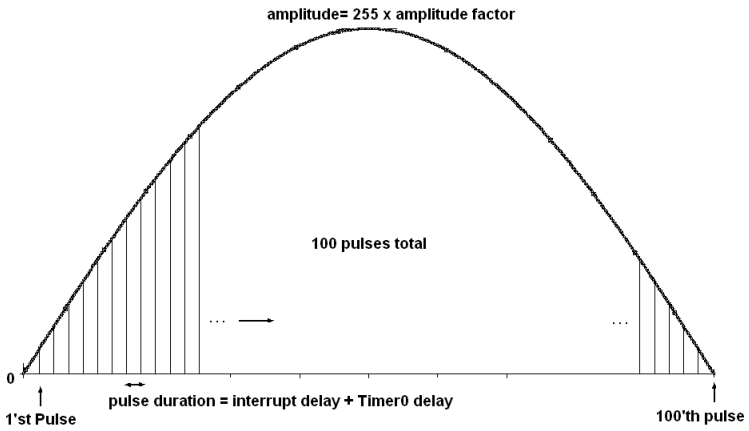



**Figure 3.34: Reference Signal for One Cycle**

8 bit digital signal generated by the controller is applied to a basic R-2R ladder type digital to analog converter (DAC) circuit in order to generate the analog reference signal. The DAC circuit is given in Figure 3.35.

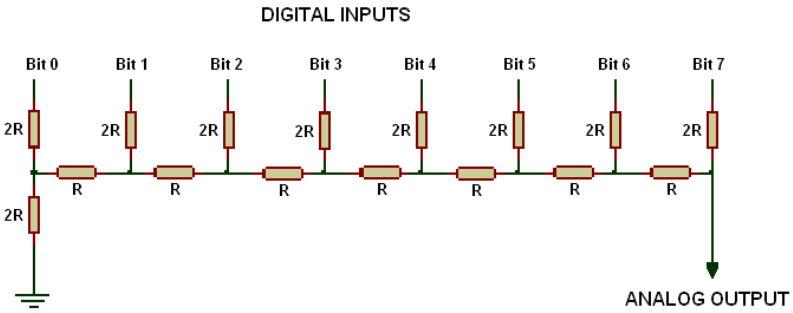



**Figure 3.35: R-2R Ladder Type DAC Circuit (R=10kΩ)**

## 3.13.2 Start-Up of the Converter

Start-up signals control the start-up of the converter. Start-up sequence is given in Figure 3.36.

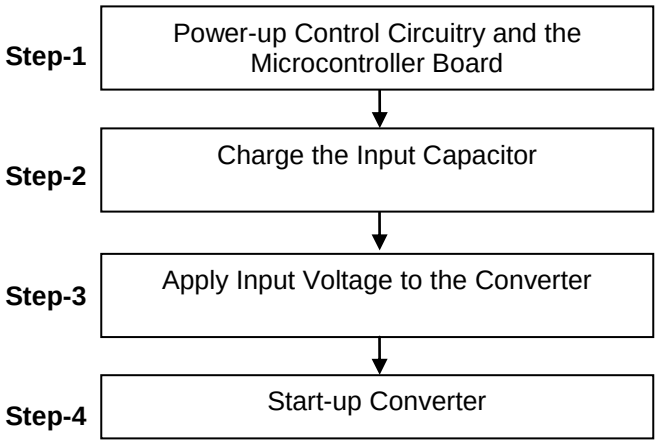



**Figure 3.36: Start-up Sequence of the Power Supply**

At Step-1, control circuit and microcontroller board is powered with a mains transformer. This step is done manually by putting the ac adaptor into the mains

socket. Then, voltage is manually applied to the input capacitor via a circuit breaker and 50 ohm resistor. This resistor prevents high charging (inrush) current levels. After the capacitor is charged, input voltage is applied to the converter at Step-3 via a hard switch. Converter does not start-up because the Under Voltage Lock Out (UVLO) pin of the PWM controller is pulled down. It must be greater then 2.5V level to start up the converter. Then converter waits for the start-up signal.

At Step-4, start-up signal comes from the microcontroller board at the next zero crossing of the reference signal. The interface between the converter and microcontroller boards is performed by the starter board. This board carries input available signal to from converter to the microcontroller. When signal is received by the microcontroller, start-up command is generated by the microcontroller. It is generated at the next zero crossing of the generating this signal. Input available and start-up signals are carried between primary and secondary grounds by means of optocouplers. With start-up signal, UVLO pin is released and converter starts up. Afterwards, the start-up action is controlled by the PWM controller with its soft start feature.

The softstart feature of the controller LM50a25A allows the power converter to gradually reach the initial steady state operating point, in order to reduce start-up stresses. A 20μA current is sourced out of the softstart pin (SS) into an external capacitor by the controller. The soft start capacitor voltage will ramp up slowly and will limit the COMP pin voltage and therefore the PWM duty cycle.

### 3.13.3 Design of the Printed Circuit Board (PCB)

The designed switch mode power supply is implemented with a PCB. The PCB contains the circuits listed below:

- Power circuit
- Error Amplifier circuit

- PWM Controller circuit
- Gate Driver circuits
- Power Supply Circuits

PCB power circuit contains only transistor and diodes. Schematic of power circuit is given in Figure 3.37. Power circuit has two isolated ground levels: primary and secondary ground. In the primary ground main and clamp transistors are placed. In the secondary one, secondary side diodes are placed. Other power components such as diode bridge rectifier, input, output and clamp capacitors, transformer and inductor is implemented outside the PCB circuit. PCB has connection terminals in order to connect these components.

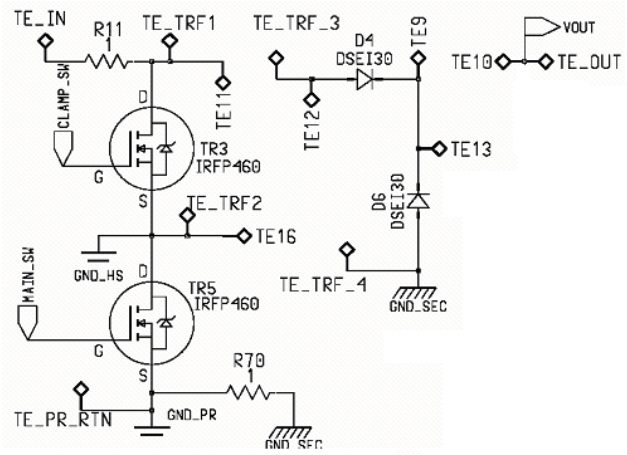



**Figure 3.37: PCB Schematic of the Power Circuit**

Error amplifier circuit is given in Figure 3.38. Error amplifier circuit is referenced to the secondary side ground, GND_SEC. DIP8 package operational amplifiers are used in the schematic. Op-amps are supplied with on-board ±12V voltages, VP12 and VN12 (see section 3.12.3.1 ). Reference signal of the error amplifier is

generated on a microcontroller board outside the PCB. Connections terminals are placed for the reference signal. In error amplifier, circuit 1206 package (3.2 x 1.6 x 1.1 mm) ceramic capacitors are used. 0.6W rating metal film resistors are used.

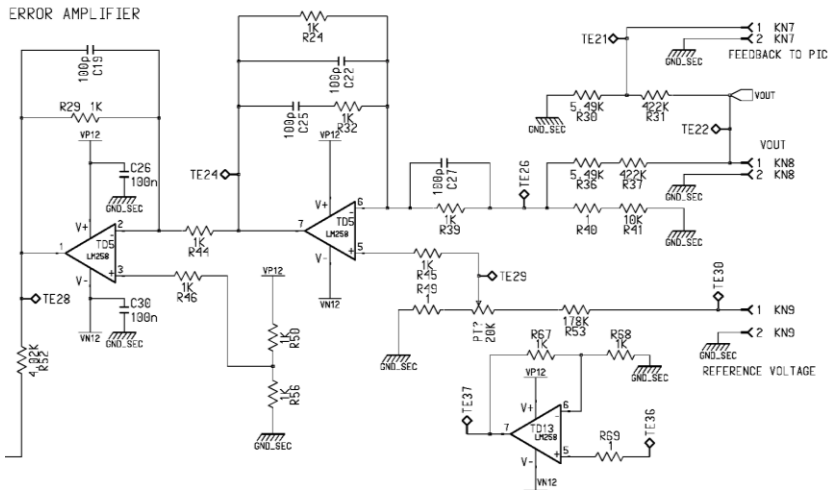



**Figure 3.38: PCB Schematic of Error Amplifier Circuit**

PWM controller circuit is given in Figure 3.39. It is referenced to the primary side ground, GND_PR. Output of the error amplifier circuit is over an optocoupler. Isolation between primary and secondary side grounds are achieved with this optocopuler. LM5025A controller and 4N38A optocoupler are used.

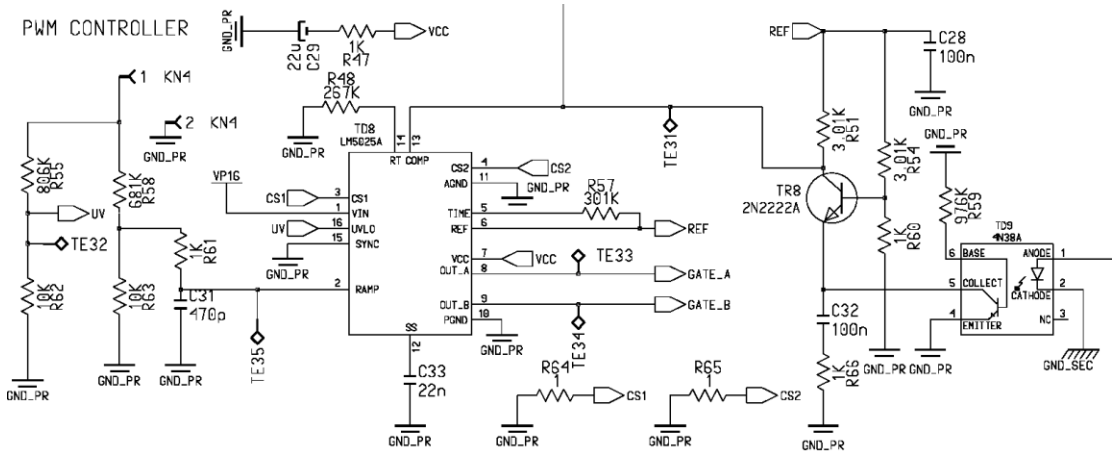



**Figure 3.39: PCB Schematic of PWM Controller Circuit**

Gate drive circuits are given in Figure 3.40. IR2121 is used as gate driver IC. Main transistor driver circuit is referenced to the primary side ground, GND_PR (see Figure 3.40 (a) ). Main switch driver is supplied with 16V voltage, VP16. Clamp transistor driver is referenced to the high side ground level GND_HS. Clamp switch driver is supplied with 15V voltage, VP15. Both drivers are driven by the gate signals generated by the PWM controller circuit. The isolation between primary side ground and high side grounds is achieved by the optocoupler, 4N38A.

PWM controller circuit is given in Figure 3.39. It is referenced to the primary side ground, GND_PR. Output of the error amplifier circuit is over an optocoupler. Isolation between primary and secondary side grounds are achieved with this optocopuler. LM5025A controller and 4N38A optocoupler are used.

(a)

(b)

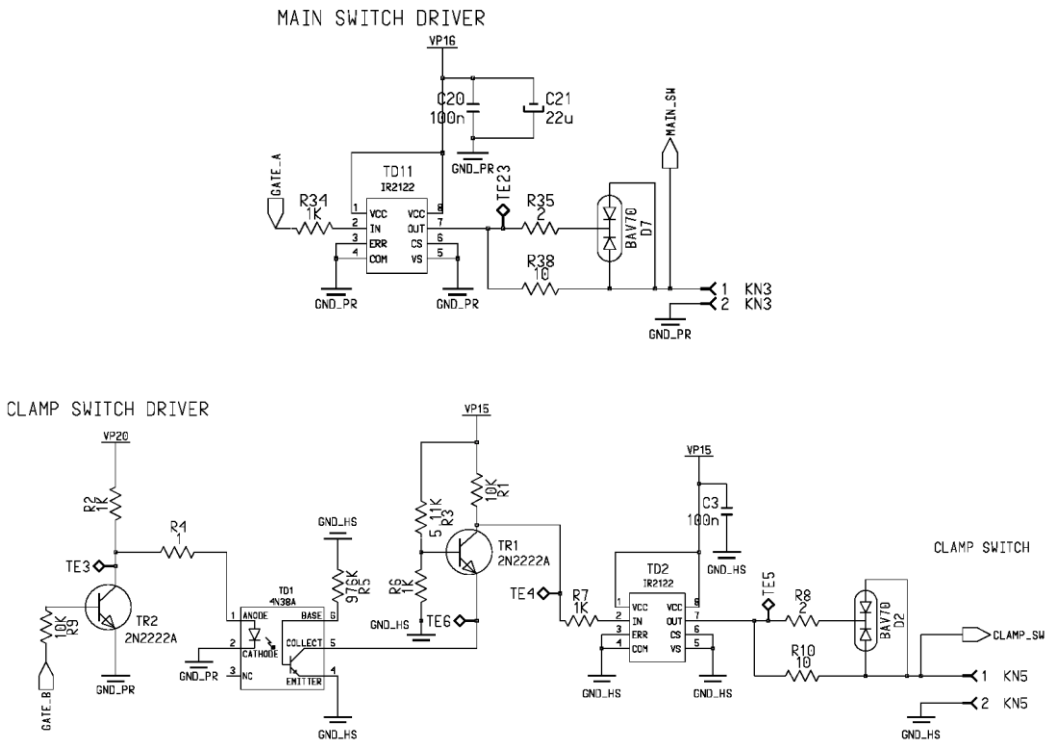



**Figure 3.40: PCB Schematic of Gate Driver Circuits**

### 3.13.3.1 Power Supplies of the PCB

Power supply circuits generates the supply voltages of error amplifier, PWM controller and gate deriver circuits. Schematics of these circuits are given in Figure 3.41. There are 4 different bias voltage levels in the PCB: VP20, VP16, VP12 and VN12.

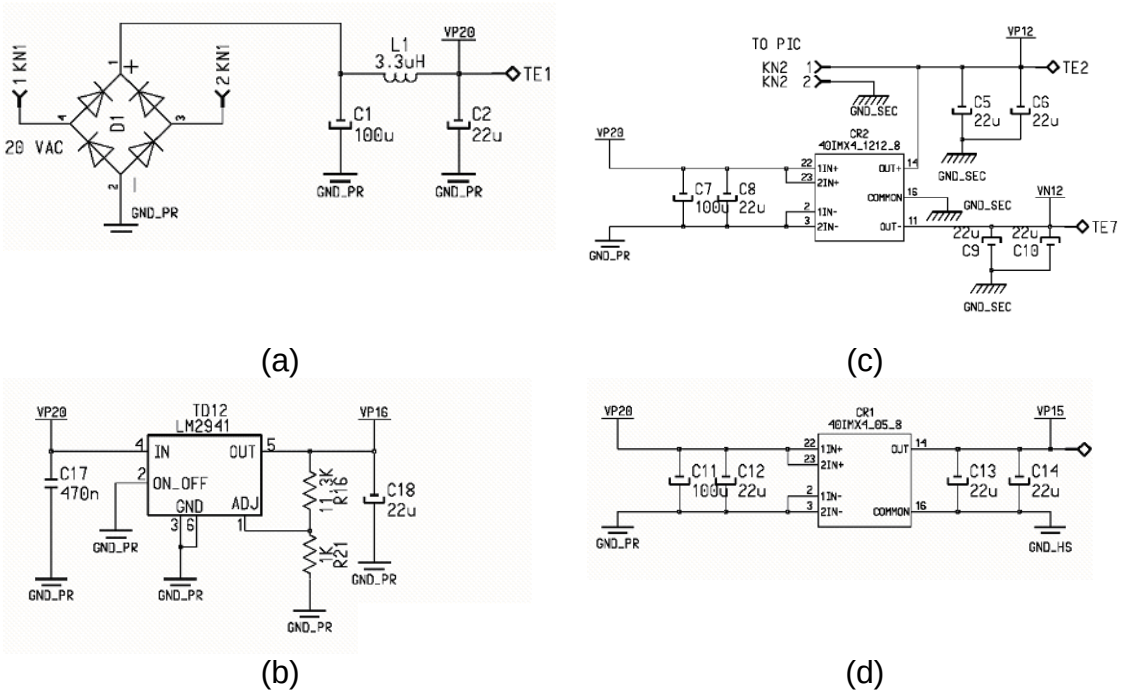



**Figure 3.41: Schematics of Bias Power Supply Circuits**

a) VP20 (20V): First VP20 voltage (20V) is generated. An AC voltage with 20V amplitude is generated by a 15W mains transformer outside the PCB. This AC voltage is rectified and VP20 voltage is obtained in the PCB (see Figure 3.41(a)). This voltage is referenced to primary ground, GND_PR.

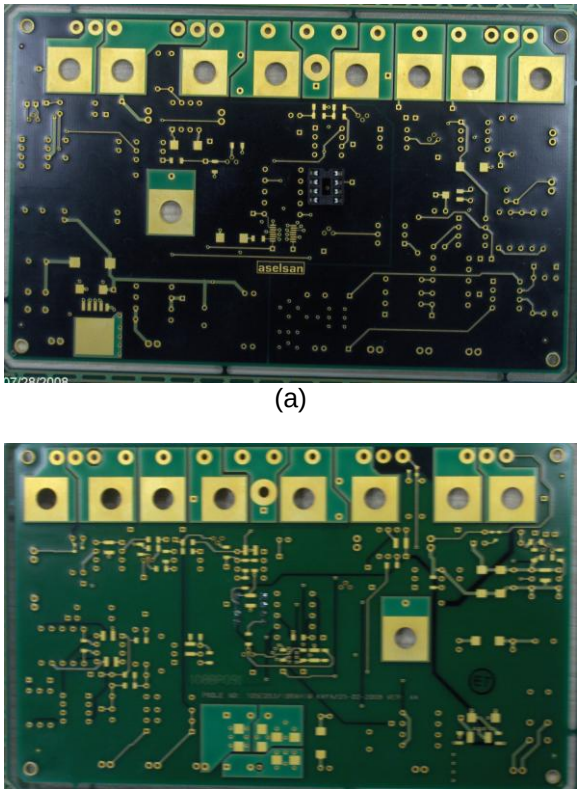
b) VP16 (16V): It is obtained from VP20 by a linear voltage regulator LM2941 (see Figure 3.37(b)). VP16 is used by the PWM controller and main transistor driver circuits.

c) VP12 and VN12 (±12V): In order to supply error amplifier circuit, VP12 (+12V) and VN12 (-12V) voltages are obtained from VP20 with an isolated DC/DC converter module (see Figure 3.37(c)).Type number of the converter module is 40IMX41212. It is 4W rated and manufactured by

Power-One. Input of this converter is referenced to the primary ground and output is referenced to secondary ground.

d) VN15 (15V): VP15 voltage is used by clamp transistor gate driver circuit. It is referenced to the high side ground, GND_HS. It is obtained from VP20 with an isolated DC/DC converter module (see Figure 3.37(d)). Type number of the converter module is 40IMX415. It is 4W rated, and manufactured by Power-One.

After schematic design, PCB circuit is designed with Mentor Design Architect design environment. PCB is designed with four layers: component (top) side, solder (bottom) side, one ground layer and one signal layer. Most of the components are placed in the component side. Surface mount capacitors are placed at the bottom side. Ground levels GND_PR, GND_SEC and GND_HS are placed on a ground layer. Signal layer is used for signal connections. The designed PCB is produced in ASELSAN facilities. It is given in Figure 3.42. Its dimensions are 160 x 100 mm.




(a)

(b)

**Figure 3.42: Photos of the Designed PCB( a: Component Side, b: Solder Side )**

## 3.14 Test of the Designed SMPS

The implemented SMPS is tested. In this section, our aim is to obtain rectified sinusoidal output voltage. Output voltage will be examined for this purpose. We will investigate the operation of the converter with resistive load. We will examine semiconductor device stresses in order verify the rated voltages of selected devices.

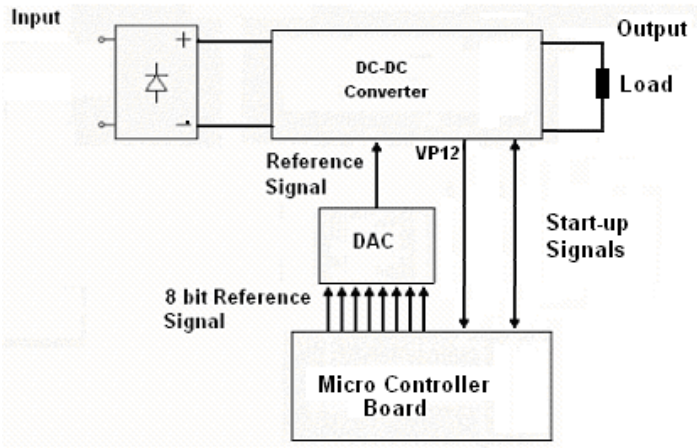



**Figure 3.43: Converter Test Set-Up**

Test set-up illustrated in Figure 3.43 is used. The microcontroller board is powered from the VP12 bias voltage of the converter. In order to start the converter, start-up steps given in the previous section are performed. First, input capacitor is charged over a resistor by turning on the circuit breaker. Then, power is applied to the converter with a hard switch. This switch also bypasses the resistor, which is used to charge the input capacitor.

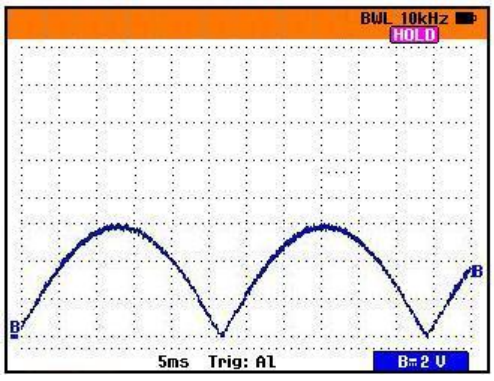



**Figure 3.44: Reference Signal Applied to the SMPS**

Analog reference signal given in Figure 3.44 is generated in the micro controller and DAC boards and applied to the converter. Its frequency is 100 Hz.

Nominal input voltage 50Hz 220VAC voltage is applied to the input. 80Ω resistive load is connected to the output of the converter. Converter is operated at 600W output power. Output voltage waveform is given in Figure 3.45. A half wave sinusoidal output voltage with 310V amplitude is obtained at the output of the converter. Frequency of the output voltage is 100 Hz.

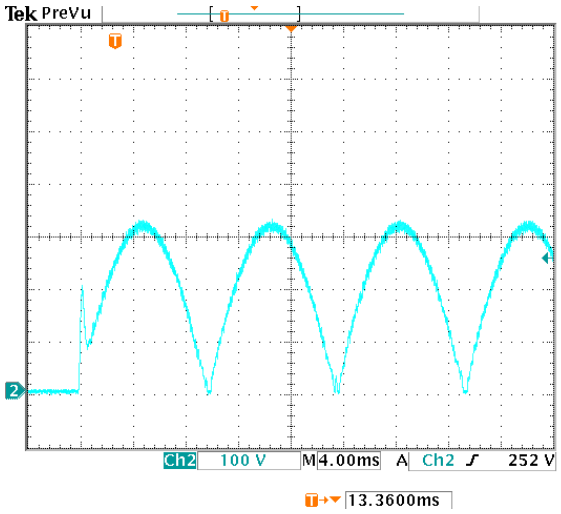



**Figure 3.45: Output Voltage of the SMPS**

Voltage stress of the transistor is given in Figure 3.46. Its maximum value is 480V, below the voltage rating of the used transistor.

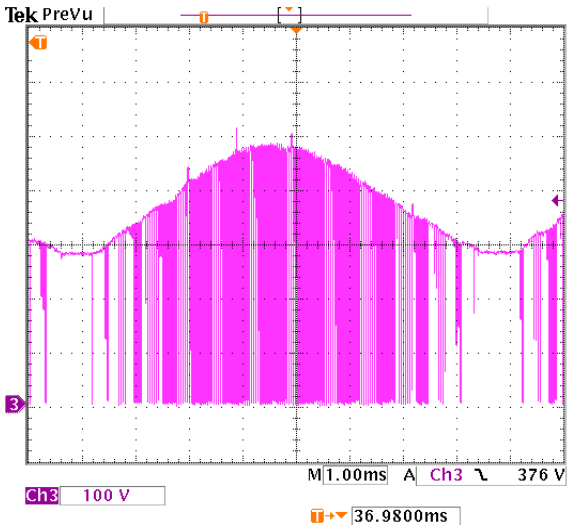



**Figure 3.46: Voltage Stress Waveform of the Transistor**

Voltage waveforms of the diodes D1 and D2 are given in Figure 3.47 and 3.48 respectively. Maximum voltage stress of the diode D1 is 650 Volts. Maximum voltage stress of the diode D2 is 900 Volts. Both voltages are below the rating of the used diodes.

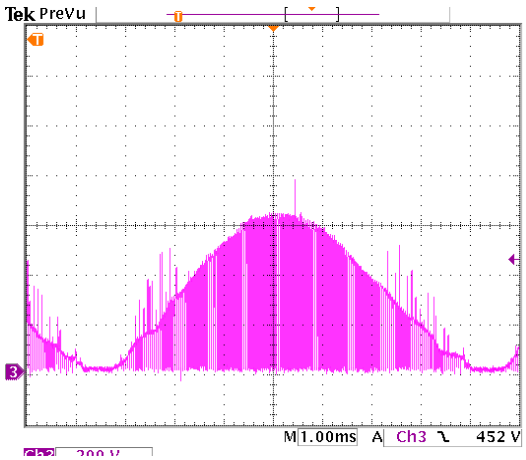



**Figure 3.47: Voltage Stress Waveform of the Diode D1**

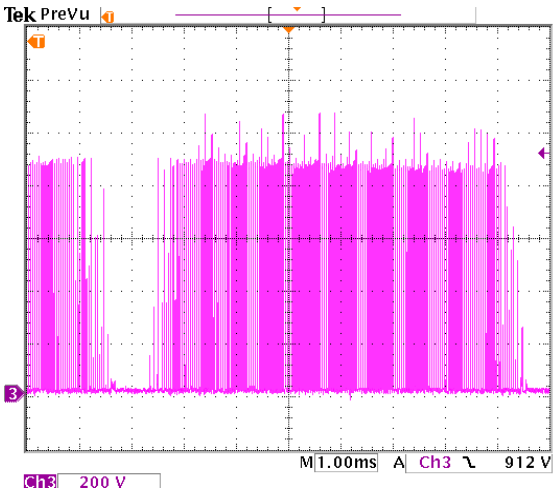



**Figure 3.48: Voltage Stress Waveform of the Diode D2**

## 3.15 Conclusion

In this chapter, switch mode power supply is designed by using the expressions derived in the previous chapter. The developed AC to half wave rectified power supply is simulated in order to verify the design. Devices stresses obtained with simulations are compared to the calculated values in the design section. Same values are obtained in the results of simulations, so design is verified. Then implementation of the design is explained. Finally, implemented design is tested in order to verify the device ratings. A half wave sinusoidal output voltage is obtained in the tests. In addition, it is seen that device stresses are below their ratings. It can be concluded that the switch mode power supply generating half have sine output is ready for experiments with inverter stage.

# CHAPTER - 4

# INVESTIGATION OF THE DESIGNED CONVERTER WITH THE OUTPUT INVERTER STAGE

## 4.1 Introduction

In this chapter, first operation of the converter together with inverter stage is investigated by means of PSPICE simulations. Then, at the end of this chapter, implementation of the inverter stage is explained.

In Figure 4.1, the inverter circuit is given. Main goal of this thesis is operate the converter and inverter stage at resistive loads. However, operation with inductive loads will be examined in order to have an idea about future research needs.

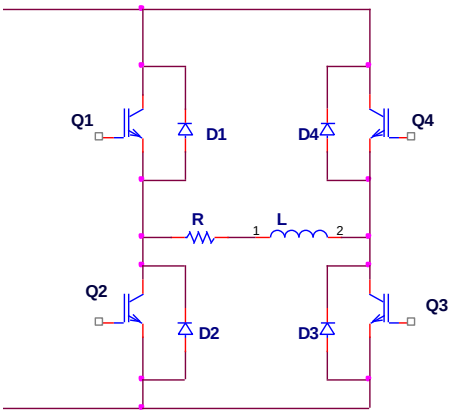



**Figure 4.1: Inverter Circuit**

## 4.2 Operation of Converter with Inverter Stage

Power circuit that will be analyzed in this chapter is given in Figure 4.2. This circuit contains rectifier circuit, active clamp forward converter circuit and inverter circuit. ORCAD version 15.7. PSIPCE simulation program is used in order to analyze the operation. Simulations are first achieved for resistive loads. Then inductive loads are simulated. Total harmonic distortion (THD) value of the output voltage is accepted as performance criteria.

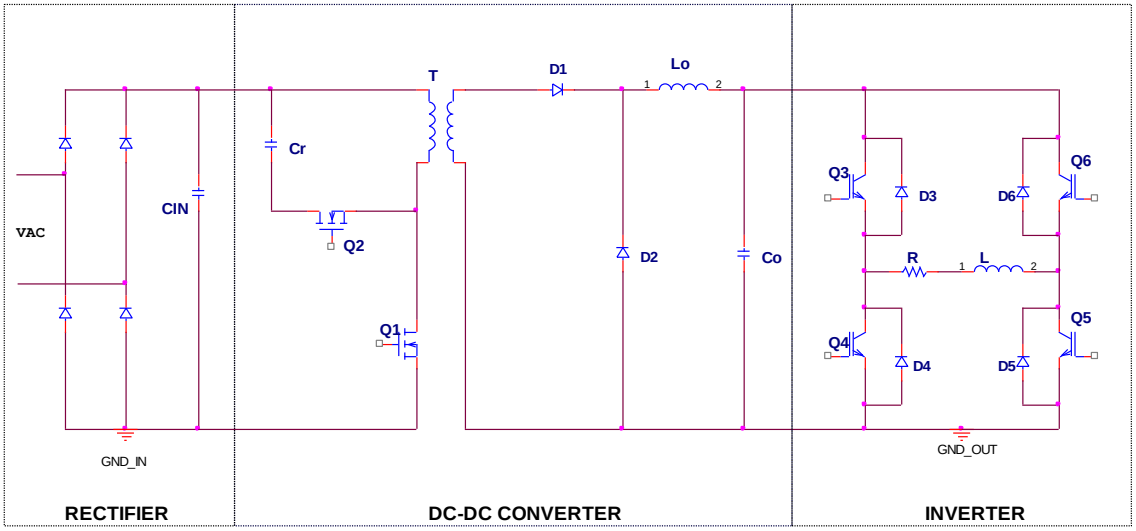



**Figure 4.2: Converter Circuit with Output Inductor Stage**

ORCAD Circuit schematics used in this section are given in Appendix B. Simulation settings are given in Appendix C. Inverter output voltage is set at 250Vrms,350V peak. For 1500VA output power, load impedance is set at 40Ω. In order to calculate the total harmonic distortion value of the output voltage, Fourier analysis is performed for first 50 harmonics of 50Hz, in PSPICE. In

simulations, gate pulses of the inverter switches are generated by using voltage sources. Frequencies of the pulses are adjusted to 50 Hz.

### 4.2.1 Operation with Resistive Loads

In resistive load analysis first load resistance is set to $R_L$=40Ω and analysis is performed for full load. Then load resistance is increased to 200Ω in order to analyze the light load performance. 20% of the full load is assumed as light loads condition. Simulation results are plotted between 10ms and 30ms.

Inverter Output voltage and load current waveforms for full load are given in Figure 4.3. It is seen that output voltage and current are in phase as expercted, thus, power factor is unity. However, in zero crossings, a distortion is seen. Pspice calculates THD value as 3.34%. In order to investigate the reason of the distortion, output voltage waveforms of the converter and main switch gate voltage is given in Figure 4.4.

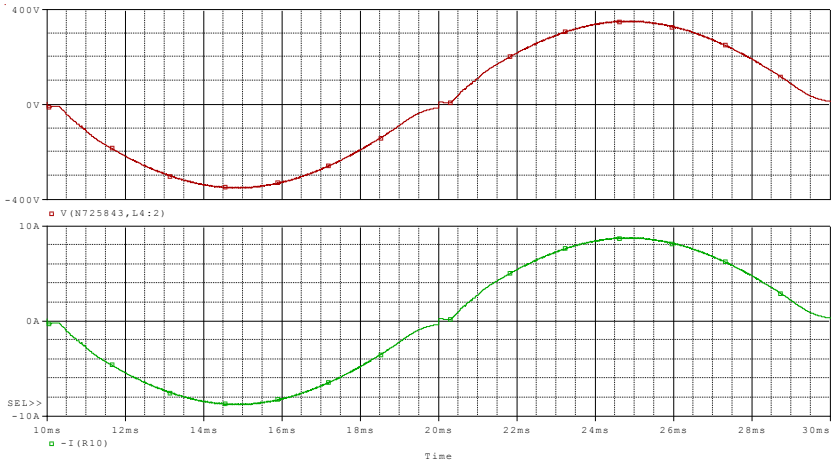



**Figure 4.3: For Resistive Load, Inverter Output Voltage (upper) and Current (bottom) Waveforms**

In Figure 4.4 it is seen that, output voltage can not decreases to zero level. Although the control circuit turns off the main switch in order to adjust the output voltage, output voltage remains nonzero due to the charge of the output capacitor. This causes distortion in inverter voltage output.

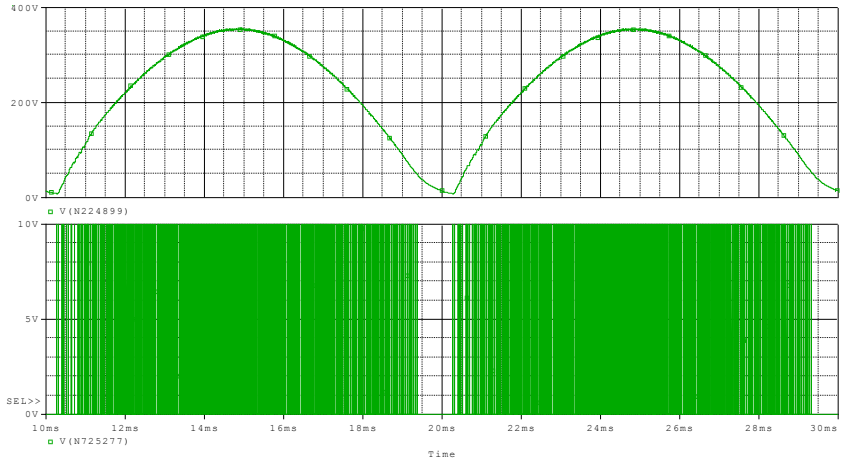



**Figure 4.4: For Resistive Load, DC Link Voltage with Main switch Gate-Source Voltage**

In Figure 4.5, output voltage and current waveforms are given for the light load case. It is seen that the distortion around the zero crossing is increased in light load. PSpice calculates THD value as 7.20%. The reason for this is the same as full load case, output capacitor can not be fully discharged. In light load case, since the load current is smaller, capacitor voltage remains in higher values then the full load case. Then, THD has its worst value in light loads case.

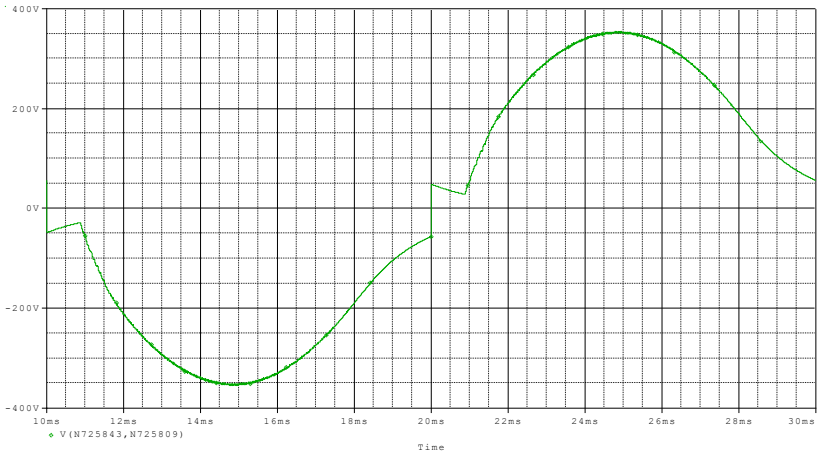



**Figure 4.5: Inverter Output Voltage For Light Resistive Load**

Note that, as mentioned above, in simulations gate drive signals are periodically generated by ideal voltage pulse sources. However, in the implementation, inverter gate drive signals are generated by microcontroller at zero crossings of the converter output voltage. Then for light load case, since the output voltage of the converter never decreases to zero level, gate drive signals can not be generated. Then, output of the converter stage will be as given in Figure 4.6.

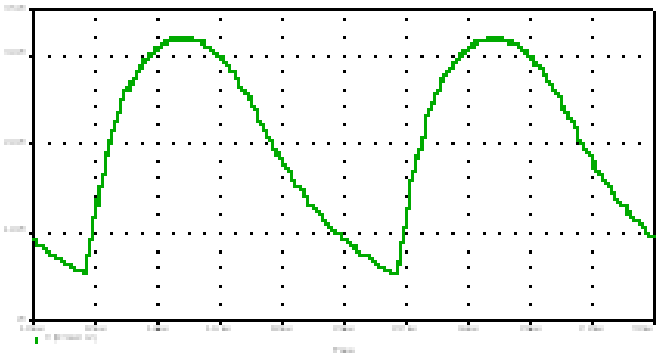


**Figure 4.6: Converter Output Voltage For Light Resistive Load**

### 4.2.2 Analysis with Inductive Load

Simulation for inductive load analysis is performed for 0.8 power factor. Load resistance is set to $R_L$=32Ω and load inductance is se to 76.4mH. Simulation results are plotted between 20ms and 40ms.

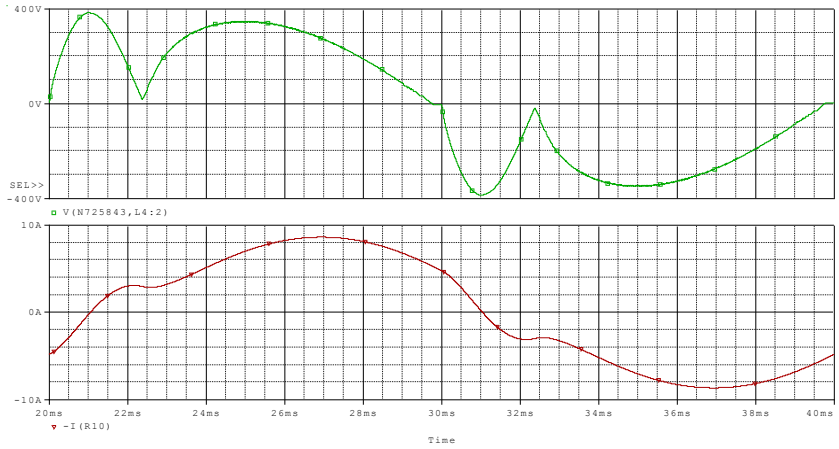



**Figure 4.7: For Inductive Load, Inverter Output Voltage (upper) and Current (bottom) Waveforms**

In Figure 4.7, inverter output voltage and current waveforms are given. It is seen that, output voltage is seriously distorted in the beginning of each half cycle. In order to examine this problem in detail, current waveforms for inverter switch Q3, diode D6 and converter output capacitor Co (see figure 4.2) are given in Figure 4.9. When inverter switch Q3 is turned off after zero crossing of the output voltage, diode D6 begins to carry the output current. This reactive current turns back to the converter output over diode D6 and begins to increase the output voltage by overcharging the output capacitor. This causes the distortion given in Figure 4.6. PSpice calculates THD value as 38.4%.

As mentioned in the previous chapter when driving inductive loads, converter must have the ability to sink current from load. However, conventional forward converter does not have this property. Then, reactive current overcharges output capacitor and distorts output voltage. Increasing output capacitor will reduce the

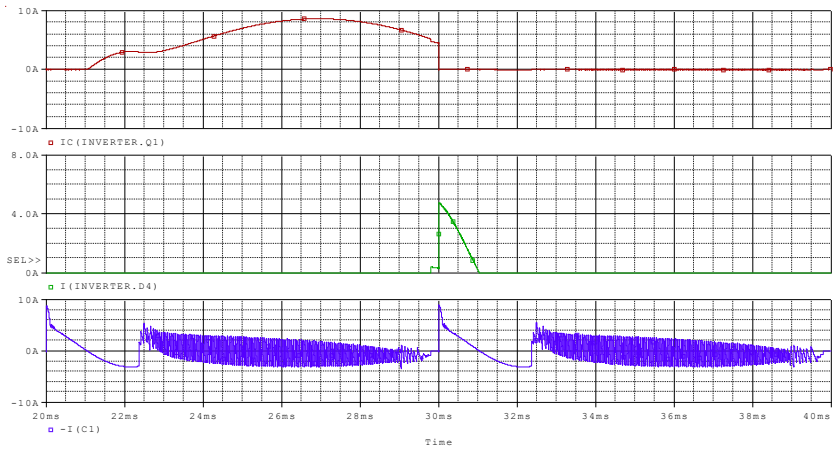



**Figure 4.8: Current Waveforms for Q3, D6 and Co ( See Figure 4.2)**

voltage distortion a bit for inductive load. However, increasing value of the output capacitor results in voltage distortion for resistive loads.

### 4.2.3 Modified Converter Topology

During the investigation in previous sections, we faced with two problems, which increase THD value. First, in resistive loads, output capacitor can not be fully discharged and output voltage does not reduce to zero. Second, in inductive loads reactive energy coming from the inductive load overcharges the output capacitor to high voltage values. Both problems are related to the output capacitor charge. Then circuit topology is modified in order to solve these problems. The purpose is creating a return path for the reactive current turning back to the converter. Modified topology is given in Figure 4.9.

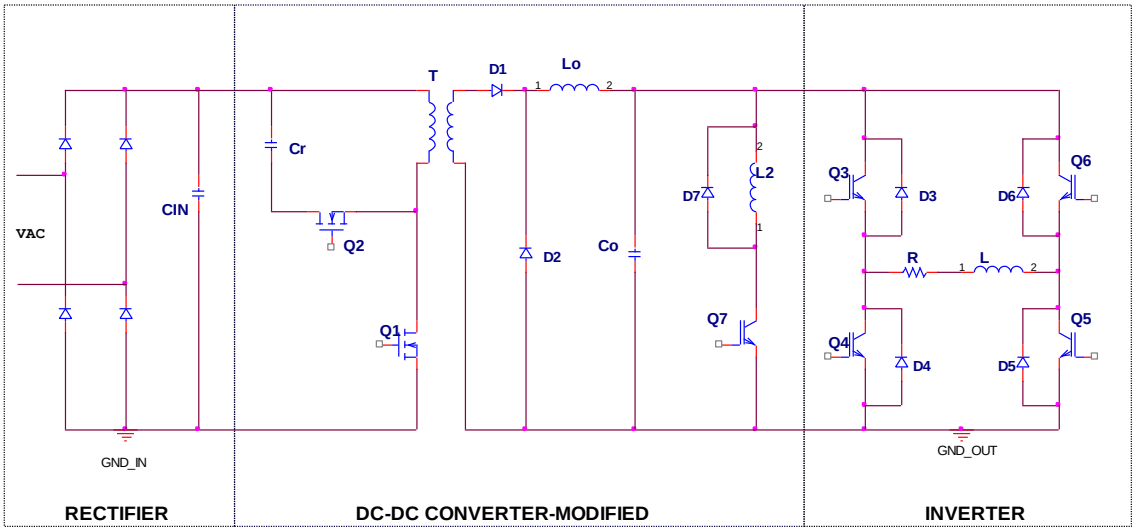



**Figure 4.9: Modified Converter Topology**

### 4.2.3.1 The Modification

In the modified topology given in Figure 4.9, a switch (Q7), a diode (D7) and an inductor (L2) is added to the circuit. The transistor Q7 is called secondary side switch in the following sections. Function of the switch is adjusting the output voltage with switching operation. For resistive load operation, switch will discharge the output capacitor during zero crossings. In inductive load operation this switch will carry the reactive current back to the load. Function of the inductor L2 is limiting the switch current to the reasonable values. Without this inductor, switch current will have very high values due to the short circuiting of the capacitor Co. Function of the diode D7 is carrying the inductor current when the switch is OFF. If this diode is not used, switch will have very high voltage stresses.

### 4.2.3.2 Control of The Secondary Side Switch Q7

Control of the switch will be archived with a secondary side control circuit. It is given in Appendix-B. Control circuit monitors the control voltage of the PWM

controller and fires the secondary side switch when the output voltage is higher then the reference value. In conventional operation, error amplifier circuit generates the control voltage by comparing the output voltage with reference voltage. PWM controller generates gate drive voltage for main and clamp switch according to value of the control voltage. When output voltage is higher then reference value, control voltage is reduced by the error amplifier circuit and then PWM controller reduces the duty cycle in order to adjust the output voltage. PWM controller has a threshold value at 1V level. When the control voltage is below 1V, PWM controller sets duty ratio to zero. This means, output voltage is much higher then reference voltage. Secondary side control circuit compares the control voltage with a constant value of 0.5V. When the control voltage is below 0.5, secondary side switch is fired.

### 4.2.4 Analyzing the Performance of the Modified Converter Topology

In this section, performance of the modified converter topology is analyzed with simulations. First steady state analysis is performed. The value of the output capacitor is reanalyzed. Simulations for different output capacitor values are performed. In these simulations, output voltage THD value, losses of secondary switch and diode is compared. According to the simulation results, an optimum capacitor value is selected. After capacitor selection, value of the L2 inductor is analyzed by means of simulations. Current of the secondary side switch and diode are the main considerations in inductor selection.

**Table 4.1: Simulation Results for Different Capacitor Values**

| Simulation Conditions | | THD | Switch Q7 Losses | Diode D7 Losses |
|---|---|---|---|---|
| Resistive, 1500W Full Load, p.f.=1 | Co=8 μF | 2.91 % | 0.05 W | 0.1 W |
| | Co=15 μF | 3.14 % | 0.1 W | 0.5 W |
| | Co=22 μF | 3.24 % | 0.5 W | 2 W |
| Resistive, 300W Light Load, p.f.=1 | Co=8 μF | 3.06 % | 0.8 W | 3.4W |
| | Co=15 μF | 3.32 % | 6 W | 15W |
| | Co=22 μF | 3.42 % | 13 W | 40W |
| Inductive, 1500VA Full Load, p.f.=0.8 | Co=8 μF | 6.19 % | 100 W | 150 W |
| | Co=15 μF | 3.85 % | 2 W | 9 W |
| | Co=22 μF | 2.75 % | 1 W | 4 W |
| Capacitive, 1500VA Full Load, p.f.=0.8 | Co=8 μF | 6.02 % | 104 W | 157 W |
| | Co=15 μF | 3.88 % | 1.8 W | 8.4 W |
| | Co=22 μF | 2.69 % | 1 W | 3.9 W |

Performance of the modified topology is analyzed in steady state conditions for output capacitor values of Co=8uF, 15uF and 22uF. Value of the inductor L2 is set to 200uH. PSpice simulations are performed for resistive, inductive loads and capacitive loads. In resistive load analysis, full load (1500W) and light load (300W) are applied to the inverter output. IRF740 MOSFET model is used as the secondary switch. Circuits used in simulations are given in Appendix B. Output voltage THD value, losses of the secondary switch, Q7, and diode D7 are obtained for each simulation (see Figure 4.9). Light load for inductive and capacitive cases are not analyzed since full load is the worst case for these types of loads. Simulation results are given in Table 4.1.

From Table 4.1 it is seen that simulation results for inductive and capacitive loads are similar as expected. In resistive load case, it is seen that the worst case is light load case. Simulations results for resistive light load and inductive

full load cases are summarized in Figure 4.10 and 4.11. In Figure 4.10 total losses of Q7 and D7 versus output capacitor are presented. In Figure 4.11, THD of the output voltage vs output capacitor is presented.

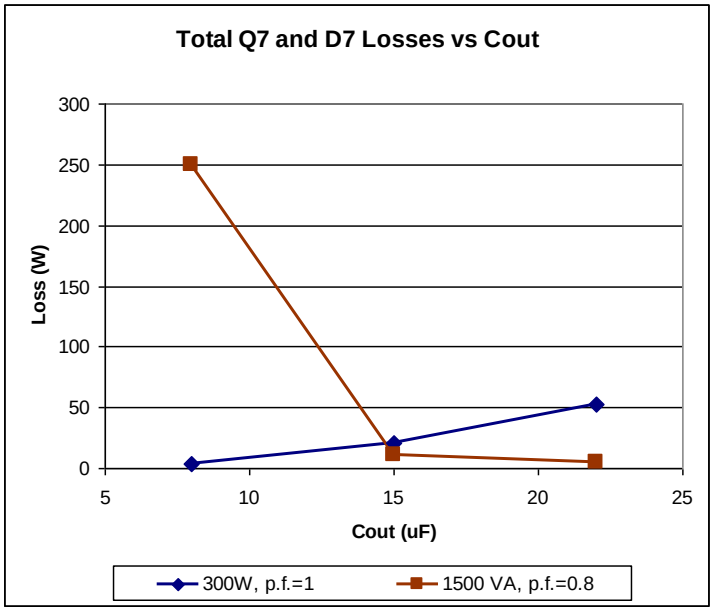



**Figure 4.10: Total Losses of Q7 and D7 vs Output Capacitor**

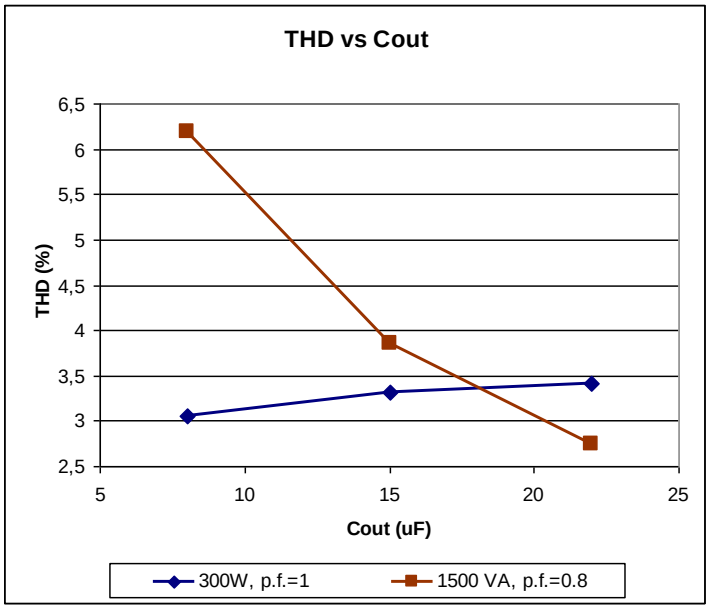



**Figure 4.11: THD vs Output Capacitor**

According to the simulations results given in Figure 4.10 and 4.11, for resistive loads, increasing capacitor value also increases THD and losses. On the other hand, for inductive loads, capacitor value must be increased in order to obtain low THD and losses. It seems that Co=15 μF is a reasonable value for both resistive and inductive loads. Then value of the output capacitor is selected to be 15 μF.

After determination of the output capacitor, value of the inductor L2 shown in Figure 4.7 is analyzed with simulations. Simulations are performed for different inductor values at resistive light load condition. Since switch and diode losses are at the highest level, light load condition is analyzed for inductor selection.

Peak Inductor current $I_{L2\_peak}$, output voltage THD value, losses of the secondary switch, Q7, and diode D7 and inductor are obtained for each simulation (see Figure 4.7). Simulation results are given in Table 4.2.

**Table 4.2: Simulation Results for Different $L_2$ Inductor Values**

| $L_2$ | $I_{L2\_peak}$ | THD | Switch Q7 Losses | Diode D7 Losses |
|---|---|---|---|---|
| 50 uH | 32 A | 3.65 % | 6 W | 16 W |
| 100 uH | 30 A | 3.55 % | 6 W | 16 W |
| 200 uH | 26 A | 3.32 % | 6 W | 16 W |
| 300 uH | 25 A | 3.31 % | 6 W | 16 W |
| 400 uH | 23 A | 3.30% | 5 W | 17W |

In Figure 4.12, peak inductor current $I_{L2\_peak}$ and THD of output voltage versus inductor L2 value is given. Since, total power loss is nearly same for all L2 values; this is not shown in Figure 4.12.

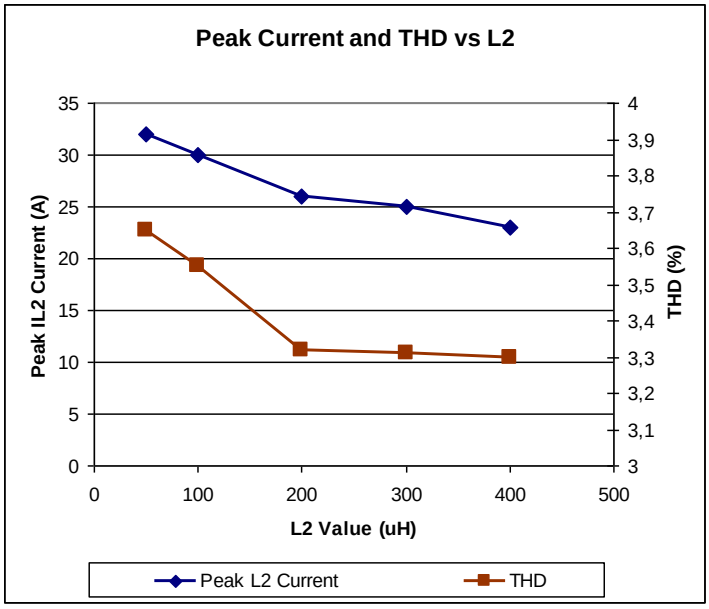



**Figure 4.12: Peak $I_{L2}$ currnet and THD vs $L_2$Inductor**

According to Figure 4.12, increasing inductor value above 200uH slightly reduces THD value. Inductors larger then 200uH cause small changes in THD value and peak inductor current. Note that losses are nearly same for all cases. Then it can be concluded that an inductance value about 200uH is appropriate for $L_2$ inductor.

Efficiency analysis of the converter is performed for modified and unmodified topologies. Simulations are done for 220 VAC 50 Hz input voltage. 220VAC 50 Hz output voltage is obtained. Resistive loads are used in the simulations. Results are given in Table 4.3 and Figure 4.13.

**Table 4.3: Efficiency Values with and without Modification**

| Output Power | Efficiency without Modification | Efficiency with Modification |
|---|---|---|
| **100 W** | 70.8 % | 63.3 % |
| **300 W** | 85.3 % | 81.2 % |
| **600 W** | 88.5 % | 87.8 % |
| **1500 W** | 89.7 % | 89.3 % |

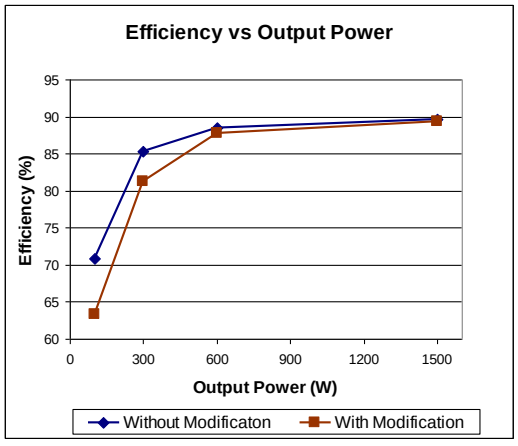



**Figure 4.13: Efficiency vs Output Power**

From figure 4.13, it is observed that, the modification decreases the efficiency of the power supply. For lower power levels, efficiency difference is higher. In other words, modification causes higher losses at the switch Q7 at light loads. This result is expected form the Figures 4.11 and 4.12. For light loads, the energy stored in the output capacitor is discharged by the switch Q7, this causes efficiency decrease for light loads. Although efficiency of the power supply is reduced after modification, it can be concluded that, efficiency of the modified topology is very good.

## 4.3 Implementation of the Inverter Stage

Inverter stage is implemented by using two boards: power board and control board.

Power board contains the circuit given in Figure 4.1. It has four switching transistors. In the inverter stage the voltage stress of the transistors are equal to the converter output voltage, 350V. IRF's IRGB4062 IBGTs are used as inverter transistors, which has voltage rating of 600V. Transistors are placed on a heatsink. Then inverter board that contains interconnections is placed onto the transistors. Copper sheets are used for the interconnections on the power board. Photo of the power board is given in Figure 4.14.

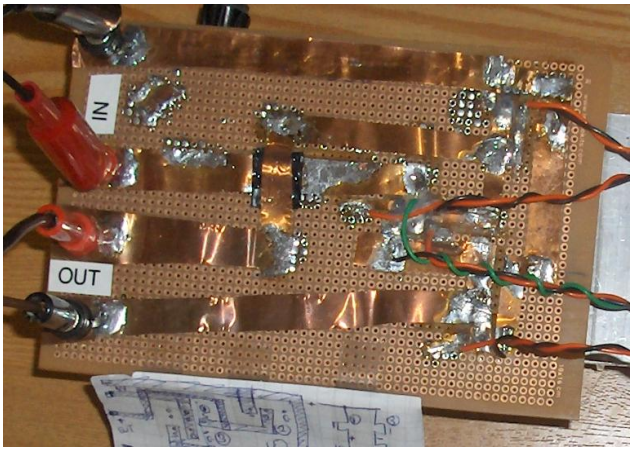



**Figure 4.14: Power Board of the Inverter**

Inverter control board contains IGBT drivers. Fuji Electric's EXB840 IGBT driver is used in the control board. Drivers are powered by isolated power supplies. Photo of the inverter control board is given in Figure 4.15

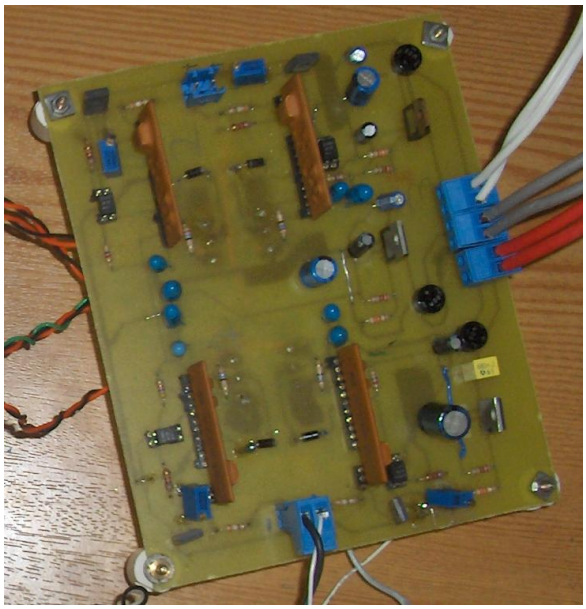


**Figure 4.15: Control Board of the Inverter**

Inverter transistor drive signals are generated by microcontroller board. These drive signals are applied to the drivers in the control board. Zero crossing points of the output voltage is sensed by the microcontroller and then inverter drive signals are generated. Converter output voltage is scaled to 5V level with resistor voltage divider. The scaled signal is given to the microcontroller. Microcontroller converts this analog signal to 10 bit digital signal by using its internal ADC module. Gate signals are generated at zero crossing points of this digital signal. Microcontroller generates two dual drive signal. Each signal drives the diagonal transistor pairs (see Figure 4.1). In order to prevent a short circuit of the DC link, 4μs dead time is used between dual signals. The source code and flowchart of the software is given at Appendix-E.

## 4.4 Conclusion

In this chapter, first the designed converter is investigated with output inverter stage by means of simulations. Secondly, implementation of the inverter stage is explained.

Since the main objective of this thesis is resistive load operation, resistive load simulations are performed first. It is seen that converter successfully operates with full resistive load. However, with light resistive loads output voltage distortion increases. In the next chapter, resistive load operation will be achieved with the implemented experimental circuit.

After resistive load simulations, inductive load operation will be investigated. Here, our goal is to gather information about inductive load operation for future development.

It is seen that, converter topology used in this thesis has a critical drawback with inductive loads. While driving inductive load, the reactive energy returning to supply overcharges the output capacitor and distorts the output voltage. The presence of diodes D1 and D2 (see Figure 4.9) and high frequency transformer

blocks the return path of the reactive energy to the supply. In fact, this is the main problem of the forward converter topology. In order to solve the problems observed in light resistive, inductive and capacitive loads, a modified topology is proposed and simulated. However, since this modified topology is a lossy topology, it is not, in fact, an ultimate solution to the problem. We will test and discuss the operation of the modified topology in the implemented power supply circuit and in the next chapter.

# CHAPTER 5

# EXPERIMENTS

## 5.1 Introduction

In this chapter, experimental studies performed with the modified SMPS circuit are explained. Purposes of the experimental tests are:

a) To observe the device stresses of the modified circuit

b) To measure the efficiency of the power supply

c) To measure the output voltage THD of the power supply

d) To understand the reliability of simulations by comparing the experiment simulation results.

The purposes listed above are achieved by the experiment done with resistive and inductive loads. First resistive load experiments is performed for steady state and dynamic conditions. Here, changing output frequency and changing the loads in and out suddenly is defined as dynamic conditions. Secondly, experiments with inductive loads are performed. Although capacitive load experiments are aimed, it is not performed because of the observed problems in inductive load experiments.

Block diagram of the experimental set-up is given in Figure 5.1. Photos of the set-up is given are given in Appendix-F.

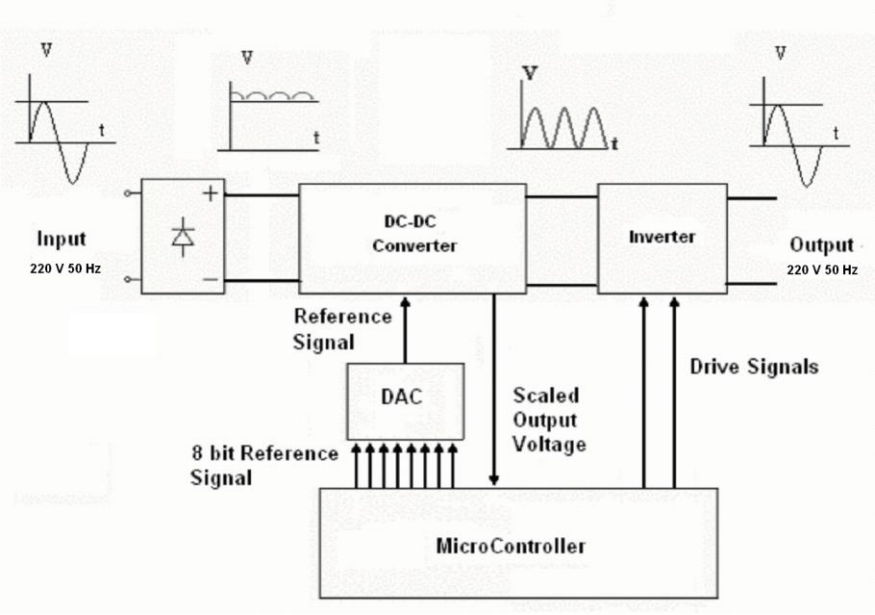



**Figure 5.1: Block Diagram of the Experimental Setup**

In the set-up, reference signal is generated by the microcontroller and digital to analog converter (DAC) boards. Generation of the reference signal is explained in Chapter 3. Gate drive signals of the inverter stage are also generated by the microcontroller board (see Chapter 4).

The experiments performed with 220VAC 50Hz mains input voltage. Converter is operated in 25 kHz switching frequency. 220VAC 50Hz output voltage is obtained for steady state resistive and inductive experiments. Frequency of the reference signal is adjusted to 50 Hz. Steady state resistive experiments are done for 300W and 600W resistive loads. Inductive load experiments are performed for 0.8 power factor, 300VA and 600VA loads.

### 5.2.1 Experiments with Resistive Load

Experiments with resistive load are performed for steady state and dynamic conditions.

### 5.1.1 Steady State Experiments with Resistive Load

In resistive load experiments, the designed power supply is operated for 300W and 600W resistive loads at 220VAC 50Hz output voltage. Although, the power supply is designed for 1500W, it is not operated in this output power. At 300W experiments, efficiency and THD of the output voltage are measured. At 600W experiments, efficiency, THD of the output voltage and device stresses are measured. At the end of this section, results of resistive experiments are evaluated.

#### 5.1.1.1 300W Resistive Load Experiments

In order to obtain 300W output power, 160Ω load resistance is used. At 300W output power, output voltage and current waveform of the inverter is obtained as given in Figure 5.2. Harmonic spectrum of the output voltage is given in Figure 5.3. RMS value of the Input current is measured with clamp meter. It is 1.66A. For 220VAC input voltage, input power is obtained as $220 \cdot 1.66 = 365W$. From Figure 5.2, peak output current is about 1.9A. Its RMS value is 1.34A. Then output power is exactly 295 W. Efficiency is 80.8%.

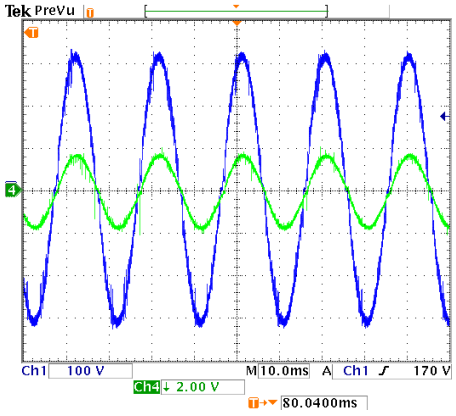



**Figure 5.2: Output Voltage and Current at 300W Resistive Load (2A Scale)**

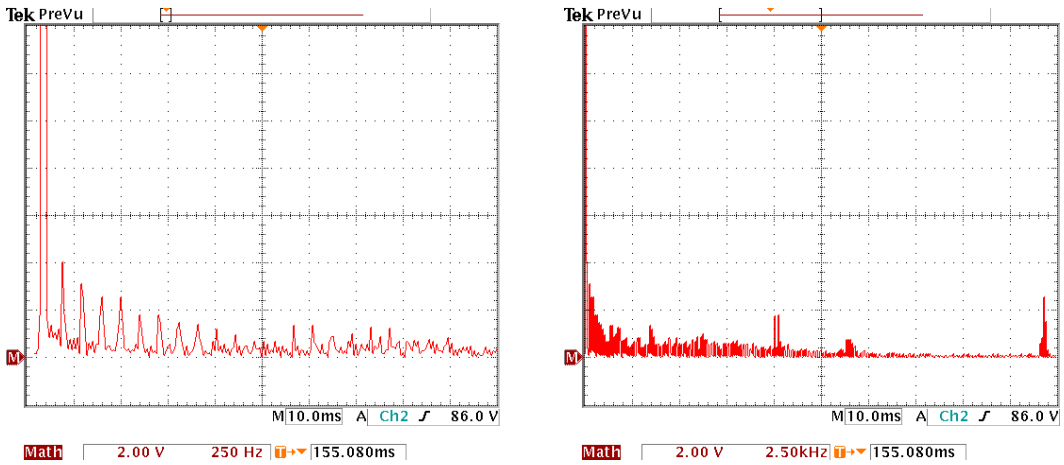



**Figure 5.3: Harmonic Spectrum of the Output Voltage at 300W Output Power**

Harmonics of the output voltage and their amplitudes are given in Table 5.1. THD value of the output voltage is calculated as 3.72%. In table 5.1, multiplies of the fundamental component 50 Hz, between 150Hz and 3150 Hz, causes 3.53% distortion. Other harmonics near switching frequency (24.9 kHz and 25 kHz in Table 5.1) causes 0.19% increase in the THD value.

**Table 5.1: Harmonics of the Output Voltage at 300W Output Power**

| Harmonic Frequency (Hz) | % of Fundamental | Harmonic Frequency (Hz) | % of Fundamental |
|---|---|---|---|
| 50 | 100% | 1050 | 0.41% |
| 150 | 1.84% | 1450 | 0.65% |
| 250 | 1.29% | 1550 | 0.69% |
| 350 | 1.06% | 1850 | 0.65% |
| 450 | 1.06% | 1950 | 0.69% |
| 550 | 0.78% | 3000 | 0.65% |
| 650 | 0.78% | 3050 | 0.46% |
| 750 | 0.69% | 3150 | 0.41% |
| 850 | 0.69% | 24900 | 0.46% |
| 950 | 0.46% | 25000 | 1.10% |

### 5.1.1.2 600W Resistive Load Experiments

In order to obtain 600W output power, 80Ω load resistance is used. At 600W output power, output voltage and current waveform of the inverter is obtained as given in Figure 5.4. Input current is given in Figure 5.5. Harmonic spectrum of the output voltage is given in Figure 5.6. RMS value of the Input current is measured as 3.2 A. Then, input power is $220 \cdot 3.14 = 704W$. From Figure 5.4, peak output current is about 3.9A. Its RMS value is 2.76 A. Then output power is exactly 607 W. Efficiency is 86.2%.

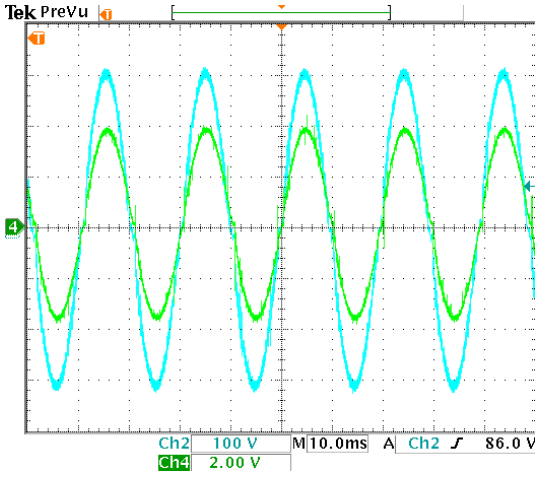



**Figure 5.4: Output Voltage and Current at 600W Resistive Load (2A scale)**

From Figure 5.5, it is seen that shape of the input current is not sinusoidal. Its peak value is 9A, RMS value is calculated as 3.2A. Peak to RMS ratio, which is called crest factor, is 2.82. For sinusoidal current, this value is 1.41 ($\sqrt{2}$). We can say that peak value of the obtained input current is two times higher then a sinusoidal wave shape. In order to obtain sinusoidal input current, the topology needs a power factor correction (PFC) stage.

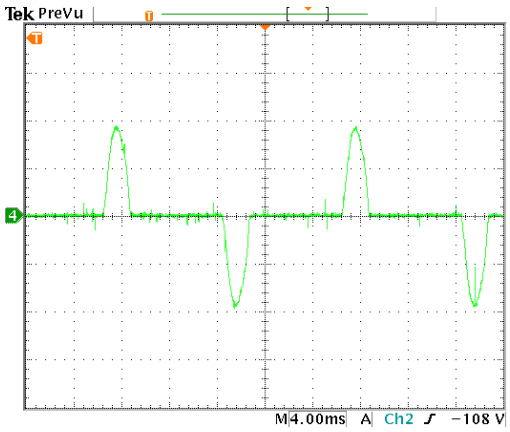



**Figure 5.5: Input Current at 600W Resistive Load (5A scale)**

Harmonics of the output voltage and their amplitudes are given in Table 5.3.

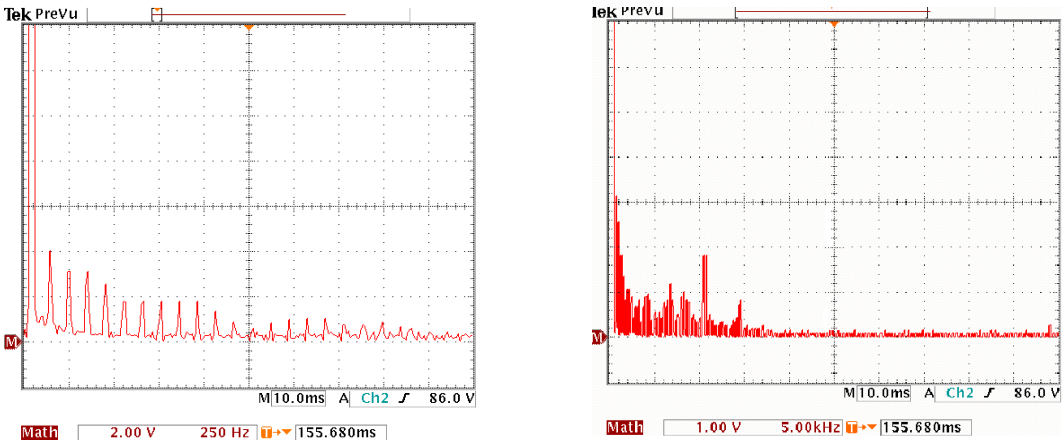



**Figure 5.6: Harmonic Spectrum of the Output Voltage at 600W Output Power**

**Table 5.2: Harmonics of the Output Voltage at 600W Output Power**

| Harmonic Frequency (Hz) | % of Fundamental | Harmonic Frequency (Hz) | % of Fundamental |
|---|---|---|---|
| 50 | 100% | 2500 | 0.36% |
| 150 | 1.81% | 2600 | 0.64% |
| 250 | 1.36% | 2700 | 0.64% |
| 350 | 1.36% | 7500 | 0.41% |
| 450 | 1.09% | 7600 | 0.50% |
| 550 | 0.91% | 9800 | 0.68% |
| 650 | 0.91% | 10000 | 0.73% |
| 750 | 0.91% | 10250 | 0.73% |
| 850 | 0.91% | 14000 | 0.36% |
| 950 | 0.77% | 25000 | 0.14% |

THD value of the output voltage is at 600W is calculated as 3.90%. In Table 5.2, multiplies of the fundamental component 50 Hz, between 150Hz and 2700 Hz, causes 3.62% distortion. Harmonics near switching frequency and the harmonics about 10kHz causes 0.28% increase in the THD value.

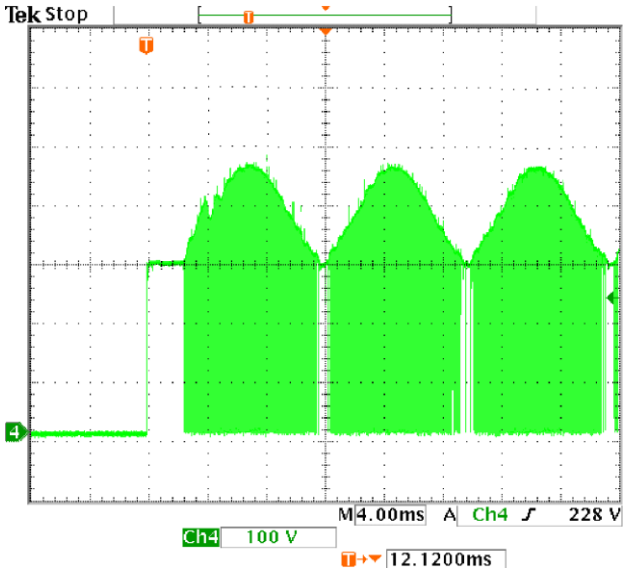



**Figure 5.7: Voltage Stress Waveform of the Transistor**

Waveform of the transistor voltage stress is given in Figure 5.7. Voltage waveforms of the diodes D1 and D2 are given in Figure 5.8 and 5.9, respectively.

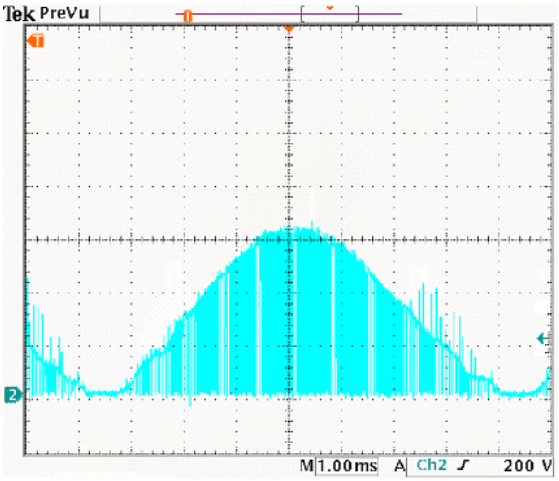



**Figure 5.8: Voltage Stress Waveform of the Diode D1**

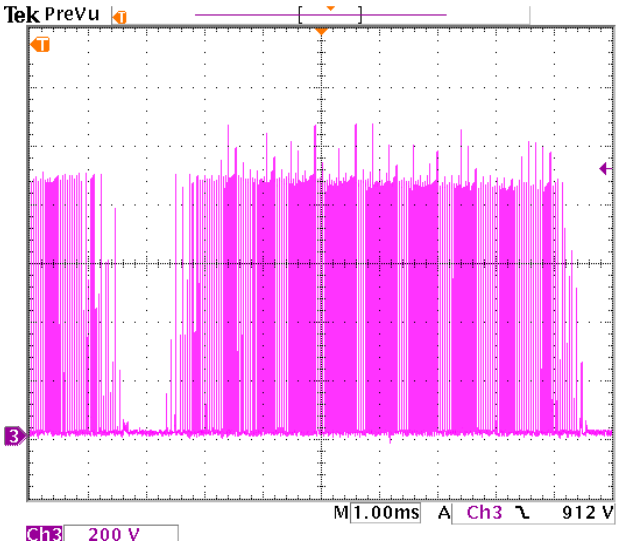



**Figure 5.9: Voltage Stress Waveform of the Diode D1**

#### 5.1.1.3 Evaluation of Steady State Resistive Experiment Results

Experiment results for resistive load are summarized in Table 5.3. In addition, simulation results for the modified and unmodified topology are given in the same table. In the table, Po is the output power, $\eta$ is the efficiency of the converter. THD is the total harmonic distortion value of the output voltage. Q1, D1 and D2 are the semiconductor devices given in Figure F.2. Simulation results are obtained for experiment conditions, 220VAC 50Hz input voltage and for 220VAC 50 Hz output voltage. According to experiment results:

According to the results given in Table 5.3,

a) In the experiments, maximum voltage stress of the transistor is obtained as 460 Volts. It is below 600V, the rated voltage of the transistor. Maximum voltage stress of the diode D1 and D2 is 650 and 1000 Volts, respectively. They are below 1200V, the rated voltage of the transistor. We can conclude that the device ratings of the modified topology are within the safe range. From simulations results, it is seen that device voltage stresses are not dependent to the output power.

b) In the experiments, at 300W output power efficiency is 6% lower then 600W case. The reason is, for lower loads, load cannot fully recharge the output capacitor of the converter. Then, it is recharged by the modified circuit's additional transistor Q7 in Figure 4.9 in order to obtain rectified half wave sine output voltage. The affect of Q7 can be observed from the efficiency values of modified and unmodified topology simulation results. Efficiency of the modified topology is reduced with respect to the unmodified topology. The amount of decrease in efficiency increases for lower loads. At 100W efficiency, difference between modified and unmodified topology is 6.7% whereas at 1500W the difference is only

0.4%. For light loads, amount of energy dissipated in Q7 increases because at lower loads can not discharge the output capacitor, then Q7 does this in a dissipative way. From simulation results, we can say that, efficiency of the implemented convert will increase for 1500W output power.

**Table 5.3: Experiment and Simulation Results for Resistive Loads**

| Po (W) | Simulation Results (Unmodified Topology) | | | | | Simulation Results (Modified Topology) | | | | | Experiment Results | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Device Stresses (V) | | | $\eta$ % | THD % | Device Stresses | | | $\eta$ % | THD % | Device Stresses | | | $\eta$ % | THD % |
| | Q1 | D1 | D2 | | | Q1 | D1 | D2 | | | Q1 | D1 | D2 | | |
| **100** | 450 | 640 | 960 | 70.8 | 9.75 | 450 | 640 | 960 | 63.3 | 2.85 | - | - | - | - | - |
| **300** | 450 | 640 | 960 | 85.3 | 3.53 | 450 | 640 | 960 | 81.2 | 2.90 | - | - | - | 80.8 | 3.72 |
| **600** | 450 | 640 | 960 | 88.5 | 2.29 | 450 | 640 | 960 | 87.8 | 3.05 | 460 | 650 | 1000 | 86.2 | 3.90 |
| **1500** | 450 | 640 | 960 | 89.7 | 1.80 | 450 | 640 | 960 | 89.3 | 3.12 | - | - | - | - | - |

c) THD of the output voltage is measured as 3.72% and 3.90 % for 300W and 600W output power levels. As mentioned in the previous section, most of the distortion occurs at the multiplies of 50Hz, output frequency. Distortion is switching frequency is For this reason, we can say that output voltage can not exactly follow the reference signal. This causes these harmonics at multiplies of 50 Hz. Distortion is switching frequency is very low. Note that, according to the power quality standard EN 50160 (*Voltage Characteristics in Public Distribution Systems*), permissible voltage THD for industry is 8%. Measured values are below the limit value of the standard.

d) Experiment results are similar to the simulation results. From table 5.3, it is seen that device stresses obtained in the experiments are similar to the simulation results. Furthermore, in simulation results, efficiency of the modified converter reduces for light loads. Same tendency can be seen in the experiment results. There is a slight difference between THD values of modified converter simulation results and experiment results. As mentioned in the previous paragraph, in experiments output voltage can not exactly follows the reference signal and this increases THD value slightly in the experiments. It can be concluded that simulation results are reliable.

e) In figure 5.5, input current of the converter is given. It is not sinusoidal current. As mentioned in the previous chapter, it has higher two times peak values then a sinusoidal waveform. In order to obtain sinusoidal input current, the topology needs a power factor correction (PFC) stage. This is discussed in the next chapter

### 5.1.2 Resistive Load Experiments at Dynamic Conditions

In order to test the dynamic response of the designed power supply, experiments are done with dynamic conditions. As defined in the introduction section with dynamic response we mean switching the load in and out; and changing the output frequency suddenly.

First, dynamic response for load change is tested. While the power supply is operating at 300W output power, load is increased to 600W suddenly. The response of the power supply is given in Figure 5.10. Secondly, load is reduced from 600W to 300W level and response of the power supply is given in Figure 5.11.

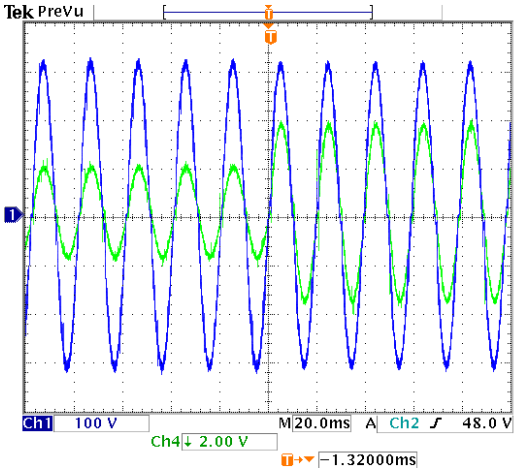



**Figure 5.10: Response of the Power Supply at 300W to 600W Transient (1 V=1A)**

According to the Figures 5.10 and 5.11, it is seen that, the output voltage is not affected from the load changes.

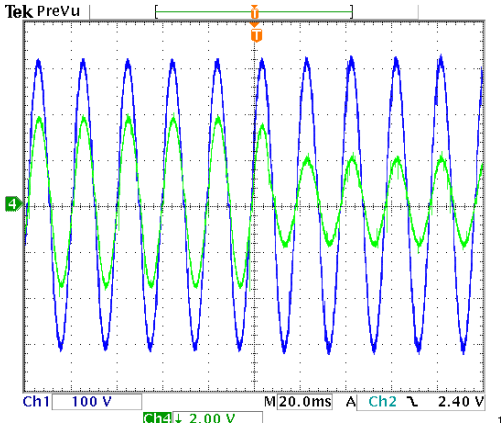



**Figure 5.11: Response of the Power Supply at 600W to 300W Transient (1 V=1A)**

In order to see the response of the power supply to the frequency changes, frequency of the reference signal is changed from 40Hz to 60 Hz and vice versa. The response of the converter is given in Figure 5.12 and Figure 5.13. Form the figures, it can be concluded that output power supply operated successfully after

a sudden change in output frequency. Note that, the amplitude of the output voltage for 40Hz is reduced to 250V level in order to keep voltage/frequency ratio constant.

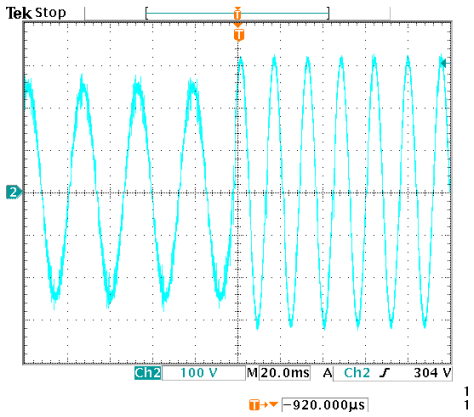



**Figure 5.12: Response of the Power Supply at Frequency Change from 40Hz to 60 Hz.**

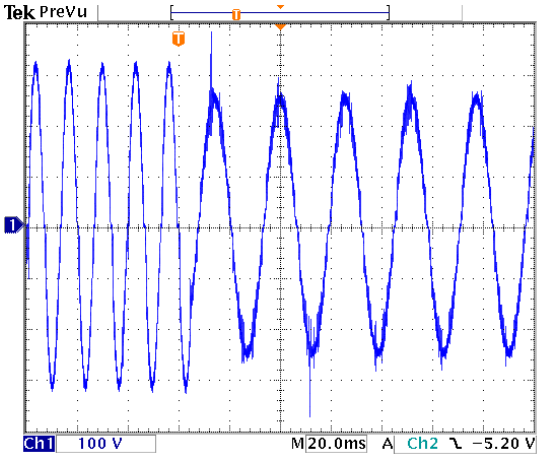



**Figure 5.13: Response of the Power Supply at Frequency Change from 60Hz to 40 Hz.**

## 5.2 Experiments with Inductive Loads

Inductive load experiments are done at 300VA and 600VA output power for 0.8 power factor. 220VAC 50Hz input voltage is applied to the power supply and 220VAC 50 Hz voltage is obtained at the output. Results of inductive experiments are evaluated in the evaluation section. In this section, THD values obtained in the experiments will be examined. Experiments with dynamic conditions are not performed with inductive loads due to the problems occurred. At the end of this section, the reason of the problems will be discussed in the discussion section.

### 5.2.1 300VA Inductive Load Experiments

In order to obtain 0.8 power factor 300 VA output power, 132Ω resistance and 305 mH inductor is connected in serial to the output of the power supply. Output voltage is given in Figure 5.14. Harmonics of the output voltage and their amplitudes in % of fundamental component are given in Table 5.4. Voltage THD is calculated as 4.25%. In Table 5.4, multiplies of the fundamental component 50 Hz, between 150Hz and 1250 Hz, causes 3.72% distortion. Harmonics near 10 kHz causes 0.53% increase in the THD value. Note that, contribution of the switching frequency harmonicas to THD is negligible.

**Table 5.4: Harmonics of the Output Voltage at 300VA Inductive Load**

| Harmonic Frequency (Hz) | % of Fundamental | Harmonic Frequency (Hz) | % of Fundamental |
|---|---|---|---|
| 50 | 100% | 1000 | 0.50% |
| 150 | 2.00% | 1050 | 0.50% |
| 250 | 1.50% | 1100 | 0.50% |
| 350 | 1.50% | 1200 | 0.80% |
| 450 | 1.00% | 1250 | 0.80% |
| 550 | 1.00% | 11500 | 0.90% |
| 650 | 0.70% | 12500 | 0.90% |
| 750 | 0.70% | 12700 | 1.00% |
| 850 | 0.60% | 13100 | 1.00% |
| 950 | 0.50% | 25000 | 0.50% |

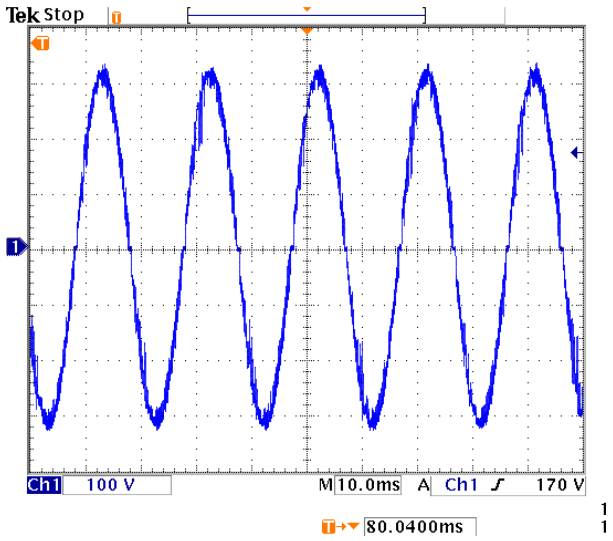



**Figure 5.14: Output Voltage Waveform at 300VA 0.8 pf Inductive Load**

## 5.2.2 600VA Inductive Load Experiments

In order to obtain 0.8 power factor 600 VA output power, 64Ω resistance and 153 mH inductor is connected in serial to the output of the power supply. Output voltage is given in Figure 5.15. Harmonics of the output voltage and their amplitudes in % of fundamental component are given in Table 5.5. Voltage THD

is calculated as 8.16%. In Table 5.5, multiplies of the fundamental component 50 Hz, between 150Hz and 950 Hz, causes 3.71% distortion. Harmonics about 10kHz frequency 4.45% increase in the THD value. The reason of this increase will be discussed in the following evaluation section.

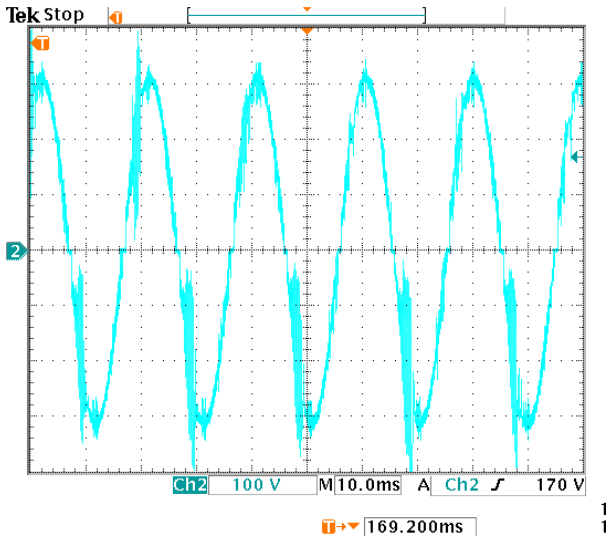



**Figure 5.15: Output Voltage Waveform at 600VA 0.8 pf Inductive Load**

**Table 5.5: Harmonics of the Output Voltage at 600VA Inductive Load**

| Harmonic Frequency (Hz) | % of Fundamental | Harmonic Frequency (Hz) | % of Fundamental |
|---|---|---|---|
| 50 | 100% | 10000 | 2.60% |
| 150 | 2.10% | 11000 | 2.50% |
| 250 | 1.70% | 11500 | 2.60% |
| 350 | 1.60% | 11700 | 2.40% |
| 450 | 1.10% | 11850 | 2.20% |
| 550 | 0.90% | 12020 | 2.30% |
| 650 | 0.80% | 12250 | 2.30% |
| 750 | 0.50% | 12350 | 2.40% |
| 850 | 0.50% | 13600 | 2.40% |
| 950 | 0.50% | 25000 | 0.50% |

### 5.2.3 Evaluation of Inductive Experiment Results

Experiment results for resistive load are summarized in Table 5.6. In addition, simulation results for the modified topology are given in the same table. In the table, Po is the output power of the converter; THD is the total harmonic distortion value of the output voltage. Simulation results are obtained for experiment conditions, 220VAC 50Hz input voltage and for 220VAC 50 Hz output voltage. Power factor of the loads are adjusted to 0.8.

**Table 5.6: Simulation and Experiment Results for Inductive Load**

| Po (VA) | Modified Topology Simulation Results THD % | Experiment Results THD % |
|---|---|---|
| **100** | 2.85 | - |
| **300** | 3.15 | 4.45 |
| **600** | 4.58 | 8.16 |
| **1500** | 6.78 | - |

According to experiment and simulation results:

a) When driving inductive loads, overcharge of the output capacitor is prevented by the modified circuit. However, the switching action of the switch Q7 increases voltage THD. This is explained in detail in the following paragraph.

b) At 300VA inductive load, THD of the output voltage is more then THD of 300W resistive load. From Table 5.3, the harmonic components about 10 kHz causes the difference. The reason for these harmonics is the inductive energy returning to the supply in the beginning of each half cycle. This is discussed in the following discussion section. The switch Q7 is switched when the reactive energy overcharges the output capacitor. The switching action of this switching causes distortion at

about 10 kHz. This means that, switching frequency of Q7 bis about 10 kHz. Note that, this frequency is not adjustable. Secondary side control circuit explained in the previous chapter determines the switching action of Q7. As mentioned, it is switched autonomously when the output capacitor is overcharged by the inductive energy. Its switching period is not adjustable.

c) The effect of inductive energy on voltage distortion increases at higher power levels. Voltage THD for 600VA inductive load is obtained as 8.16%. From Table 5.4, harmonic components about 10 kHz cause more 4.45% increase in THD. As explained in the previous paragraph the reason is the switching action of the switch Q7. For 600V level, this switch causes more THD.

d) According to the simulation results obtained from the modified circuit, THD values increases as output power increases. The same tendency can be seen in experiment results. Dorm these points of view, simulations seem to be reliable.

### 5.2.4 Discussion

The reason of the problem in driving inductive load is the reactive current coming from the output stage overcharges the output capacitor of the converter. In order to avoid the overcharge event, conventional forward converter topology is modified. As explained in previous chapter, an additional transistor and diode with an inductor is added to the topology. Operation of the power supply for inductive loads is illustrated in Figure 5.16 with two modes.

In Mode-1, transistors Q3 and Q5 are conducting the load current. When these transistors are turned off at zero crossing of the output voltage, the current in the load inductor turns back to the output of the converter stage in Mode -2. This reactive current causes problems. In a conventional forward converter, this

current overcharges the output capacitor of the converter and causes high voltage levels. In order to prevent this overcharge, we added a transistor and diode with an inductor to create a return path as given in Figure 5.16, Mode-2. Modified converter topology prevented the overcharge of the capacitor. However, for higher output powers the distortion of the output voltage increases. In inductive load experiments, for 300VA output power output voltage THD is % 4.2. This value increased to 8.1% at 600VA output power.

Although the capacitor overcharge is prevented, the reactive energy dissipated in the added components decreases the efficiency of the power supply. Moreover, it seems that for higher power levels and lower power factors, the increase in THD will become a more serious problem. The modified forward converter topology is based on the idea of dissipation of the inductive energy. Ideally, the inductive energy must be recycled to the large input capacitor $C_{in}$. Any transformerless recycle path from secondary side to the input capacitor cannot be used since it will break the isolation feature of the converter. The possible solutions for this inductive load problem will be discussed in the next chapter.

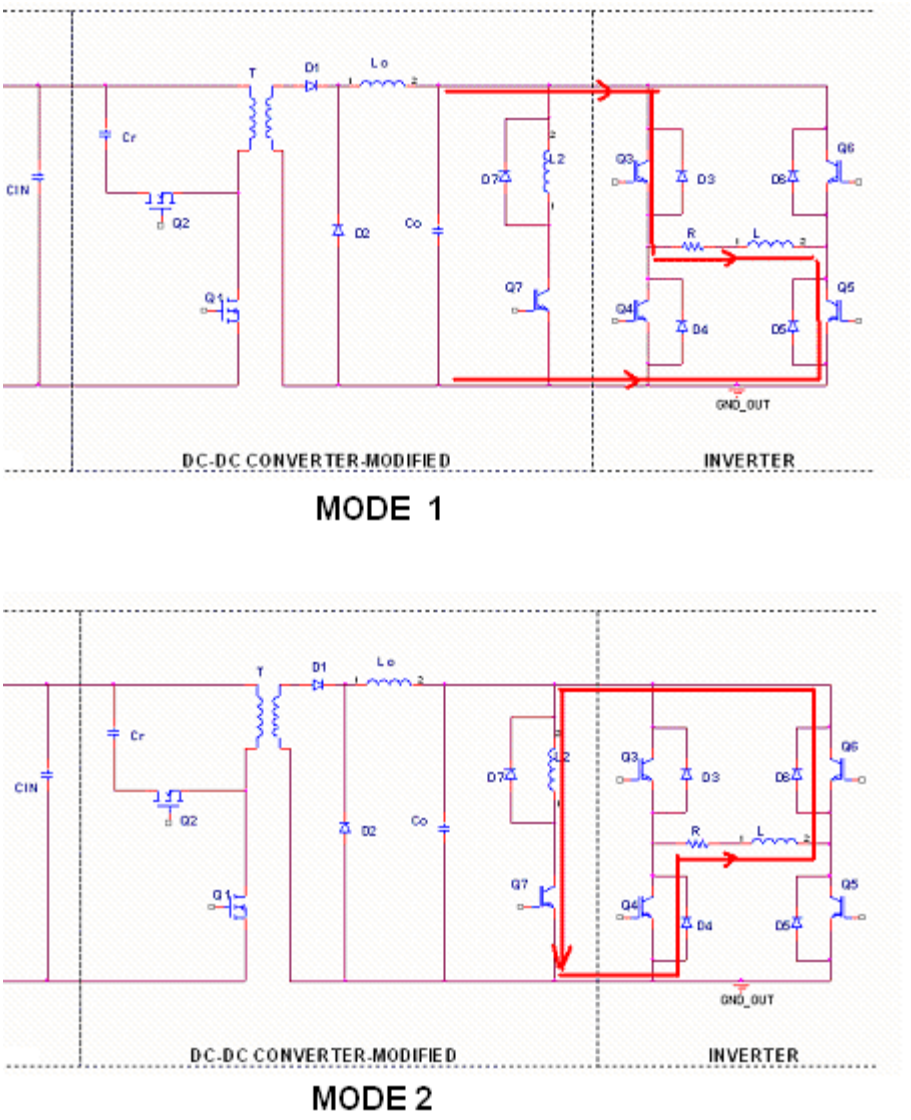



**Figure 5.16: Operation of the Power Supply with Inductive Load**

## 5.3 Conclusion

Implemented supply is operated at resistive and inductive loads. The voltage stresses of the semiconductor components are obtained as expected. The stresses are below the ratings of the selected components. The resultant waveforms are similar with the simulations results.

Efficiency of the power supply is obtained as 86.2% at 600W resistive load. Efficiency decreases at lower loads. THD values of 3.72% and 3.90% are obtained at the output voltage in operation with resistive loads. The implemented power supply operated successfully with linear loads. However, input current of the power supply is not sinusoidal. It has higher peak values. Power supply requires a PFC stage in order to obtain sinusoidal input current. PFC stage is discussed in the following chapter.

Converter has problems with inductive loads. In inductive load operations, THD of the output voltage increases as output power increases. %8.2 THD is obtained at 600VA level for 0.8 power factor. Solution of inductive load operation is discussed in the following chapter.

# CHAPTER 6

# CONCLUSION AND FUTURE WORK

## 6.1 Introduction

In the previous chapter, experiments are performed with the implemented power supply topology. From the results of these experiments, following conclusions are extracted:

a) By using the modified forward converter topology given in Figure 4.9, a pure sinusoidal output voltage is obtained for resistive loads. The obtained output voltage does not have switching pulses. Its THD is very low, about 3-4%, so there is no need to use external filters. We can conclude that the implemented power supply topology is operating successfully for resistive loads.

b) In industry, loads are not purely resistive. Electric motors, which are widely used in industry, are inductive loads. In experiments, implemented power supply is also tested for inductive loads in order to observe the performance for this type of loads. In the experiments, we have seen that problems occurred while driving inductive loads. The reason of the problems is that, reactive energy caused by the inductive load can not be transferred to a big capacitance. In other words, the energy returning to the supply while driving loads causes the problems. Then, we concluded that the modified forward converter topology is not appropriate for inductive load operations.

c) Input current of the implemented power supply is given in Chapter 5. It is not a sinusoidal input current. It has high peak values. Crest factor, peak to RMS ratio, of the input current is calculated as 2.83. This is two times higher then the crest factor of a sinusoidal current, which is 1.41. This high crest factor causes problems for higher load levels. In industrial facilities, many motor drivers are used. Drivers with high crest factors cause higher distortions at the electric distribution system. For this reason, the need of industry is drivers having sinusoidal input currents. Sinusoidal input current can be obtained for low power levels, however it is still a challenging work for high power levels. Furthermore, isolated motor drivers are needed in order to reduce EMI (Electromagnetic Interference) problems and satisfy some safety regulations.

Main objective of this chapter is to discuss the converter topologies in order to obtain a topology that clears the drawbacks given in the above paragraphs (b) and (c). In other words, we are going to investigate converter topologies to change the current topology with the one that drives inductive loads; has isolation and sinusoidal input current.

In discussion section, Implemented and proposed converter topologies are compared with the conventional PWM inverter topology.

## 6.2 Single Stage Converter Topologies

Commonly used single stage DC/DC converter topologies are flyback, half bridge and full bride converters. Their basic operation theory and device ratings are presented in the first chapter. In this section, their operations with inductive load and feasibility for having sinusoidal input current will be examined.

Flyback converter topology given in Figure 1.3 is derived from boost converter. The inductor in the conventional buck boost converter is replaced with flyback transformer. In basic PFC pre-regulator stages, generally boost converter type

topologies are used. Since the flyback converter is a boost derived topology, it is possible to obtain sinusoidal input current by using a power factor correction controller IC. However, in driving an inductive load, flyback converter has the same problem as forward converter has: reactive energy can not be recycled because of the rectifier diode D1 in figure 1.3. Therefore, flyback converter is not the appropriate topology in inductive load driving.

Half and full bridge converter topologies given in Figure 1.5 and 1.6 are buck derived converters. With these topologies, sinusoidal input current can not be obtained because their inductors are in the secondary side. PFC preregulator topologies need an inductor in the primary or input side in order to shape the input current. The output stages of these converters are similar to the forward converter. Then half and full bridge converter topologies have the same inductive load driving problem. Therefore, these two topologies are not the appropriate topology in our application.

As a result, commonly used isolated single stage DC/DC converter topologies, flyback, forward, half bridge and full bridge, can not solve the inductive load driving problem. Then we must examine two stage topologies in order to find a solution for the problem.

## 6.3 Two Stage Converter Topologies

In this section, DC-DC converter stage is examined in two stages. The converter requirements are satisfied by different stages. These stages are PFC (Power Factor Correction) stage and DC/DC converter stage as given in Figure 6.1. PFC stage can be a boost derived PFC regulator topology. DC-DC converter stage can be an isolated or non-isolated converter topology. Functions of the overall topology are obtaining sinusoidal input current, isolation, inductive load driving and generating half wave rectified sinusoidal waveform .These functions are separated to two topologies.

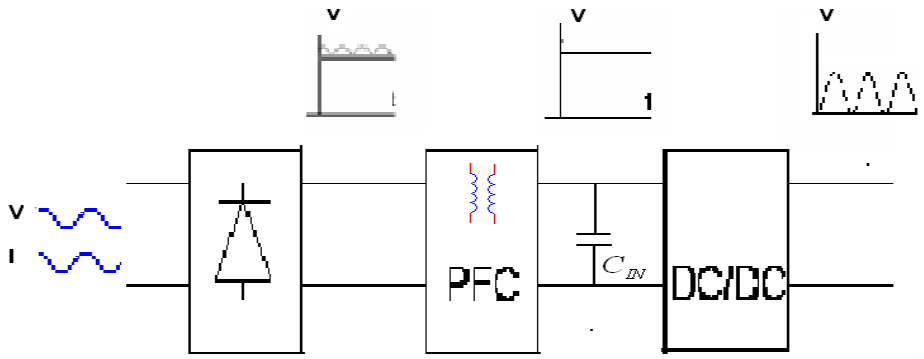



**Figure 6.1: Two Stage Converter Topology**

First, we must determine the functions of these two topologies. Generating half wave rectified sinusoidal output and driving inductive loads are related to the load side so DC-DC converter stage must satisfy these functions. Obtaining sinusoidal input current is related to the power factor correction concept, then PFC stage must handle this requirement. Isolation function determines the resulting topology. DC-DC converter topology needs to recycle reactive energy to the input capacitor $C_{IN}$ in Figure 6.1. in order to handle inductive load driving successfully. In this thesis, while considering energy recovery to the mains, we see that high frequency isolation transformer blockades any possible recycle path to the mains. Then, we can conclude that, if DC-DC converter stage has isolation, then there are problems in inductive load driving, especially in reactive energy recovery.

In reference [9], synchronous buck converter stage is used in reactive energy recovery. It is given in Figure 6.2. The diode of the conventional buck converter is replaced with a transistor, T2 in Figure 6.2. This topology is appropriate for our DC-DC converter stage.

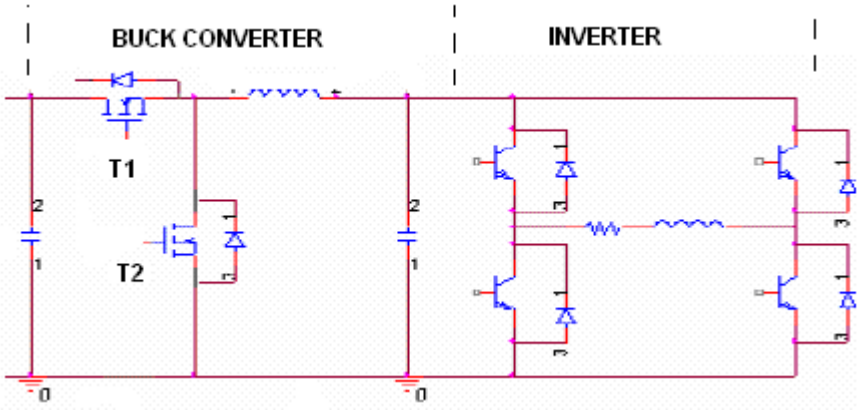



**Figure 6.2: Synchronous Buck Converter as DC-DC Converter Stage**

Operation of the synchronous buck converter with inductive load is illustrated in Figure 6.3. In mode 1, load current flows through the inverter transistors. When these transistors are turned off at the zero crossing of the output voltage, the current of the load inductor begins flowing through the diodes to the converter side and Mode-2 begins. In mode 2 (a), the reactive current flows though the low side transistor, and reactive energy is stored in the output inductor. Then, in Mode 2b, low side transistor is turned off, and energy stored in the output inductor is transferred to the input capacitor Cin. Note that, during Mode-2, buck converter operates as a boost converter and recycles the reactive energy to the load side. This process can not be achieved in the forward converter due to its high frequency isolation transformer. Lack of isolation seems to be the disadvantage of the synchronous buck, on the other hand its non-isolated structure enables the reactive energy recovery.

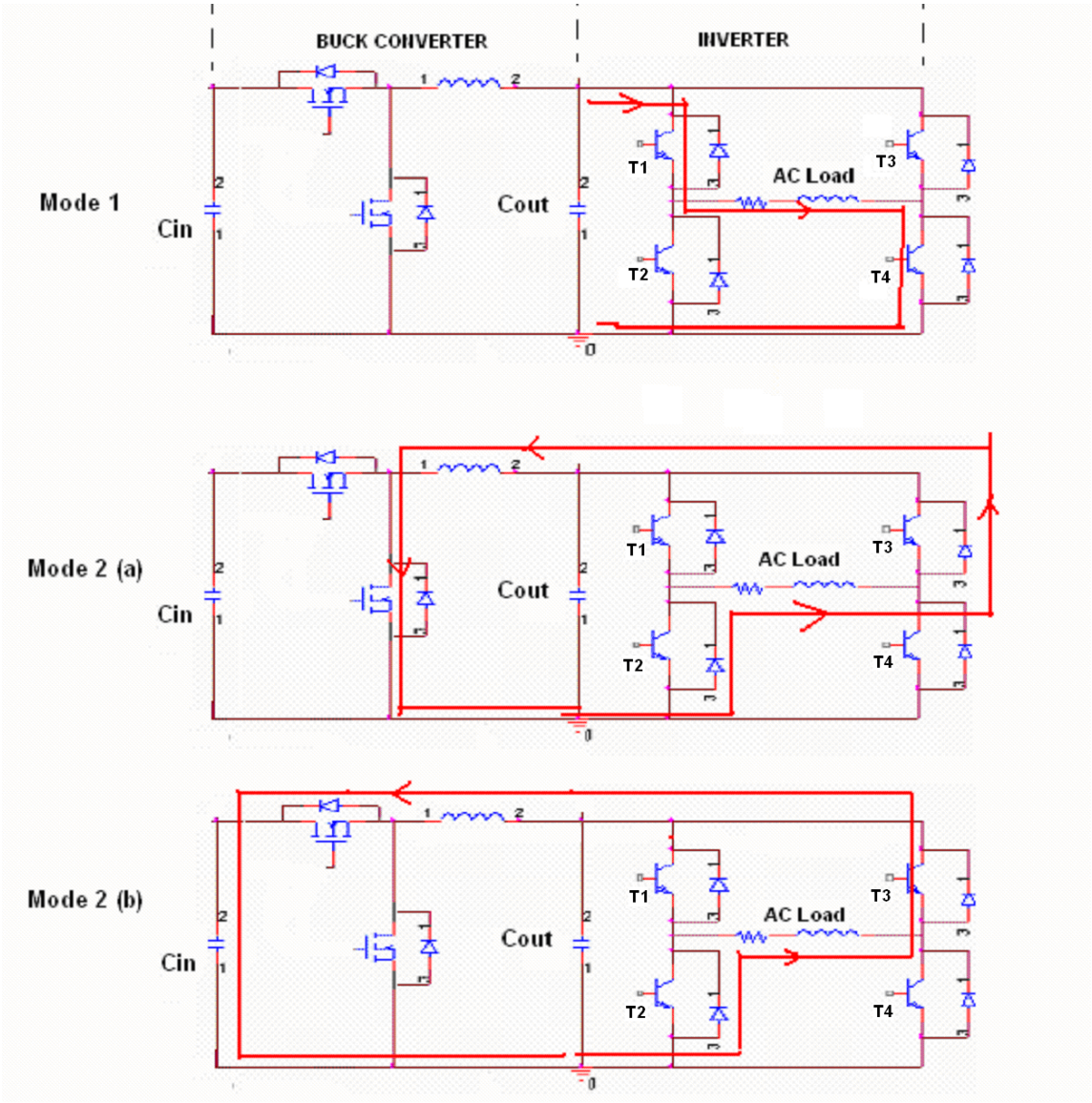



**Figure 6.3: Operation of the Synchronous Buck Converter with Inductive Load**

The operation given in Figure 6.3 is also valid for capacitive loads. In capacitive loads reactive energy returns back to the supply in the second quadrant of each half cycle, where as in inductive reactive energy transfer occurs in the first quadrant of each half cycle.

Reactive energy transferred to the input capacitor of the buck converter causes capacitor voltage to increase. This voltage rise is important since it can cause problems in the operation of the PFC stage. We must investigate the value of the voltage rise on the input capacitor of the buck converter.

The amount of voltage rise can be calculated for a specific output power and power factor. From energy equations, we can obtain expression of the capacitor voltage rise. Note that, the base of the following calculation is energy transfer concept. Equation for reactive power is given is equation 6.1.

$$Q = S \cdot \sin(\Phi) \qquad (6.1)$$

Here Q is the reactive power, S is the apparent power and $\Phi$ is the phase angle. Amount of reactive energy transferred in one-half cycle can be found from the following equation.

$$E = \frac{Q}{2} \cdot T \cdot \frac{\Phi}{2\pi} \qquad (6.2)$$

Here, E is the reactive energy of the load in once half cycle; T is the period of the output voltage, it is 20ms for 50 Hz output voltage. Here, $T \cdot \frac{\Phi}{2\pi}$ product gives us the reactive energy transfer duration in one half cycle.

If we assume that this energy is transferred to the input capacitor with 80% efficiency, then voltage rise in the input capacitor can be calculated with the following equation.

$$0.8 \cdot E = \frac{1}{2} \cdot C_{in} \cdot \Delta V^2 \qquad (6.3)$$

Here, $C_{in}$ is the input capacitor of the buck converter; $\Delta V$ is the voltage rise of this capacitor due to reactive energy transfer.

By combining equations 6.1, 6.2 and 6.3 we can obtain the following equation that gives the voltage rise equation of the input capacitor.

$$\frac{1}{2}\cdot C_{in}\cdot \Delta V^{2} = 0.8\cdot \frac{S\cdot \sin(\Phi)}{2}\cdot T\cdot \frac{\Phi}{2\pi}$$

$$\Delta V^{2} = 0.8\cdot S\cdot \sin(\Phi)\cdot T\cdot \frac{\Phi}{2\pi}\cdot \frac{1}{\cdot C_{in}}$$

$$\Delta V = \sqrt{\frac{0.127\cdot S\cdot \sin(\Phi)\cdot T\cdot \Phi}{C_{in}}} \qquad (6.4)$$

Note that the input capacitor of buck converter is also the output capacitor of the SEPIC converter. 2mF is capacitor value is used in calculations. Capacitor voltage rise is calculated for S=1KVA, 3KVA and 5KVA apparent power with cos(Φ)=0.1, 0.3, 0.5 and 0.8 power factor values. Calculation results are given in Figure 6.4.

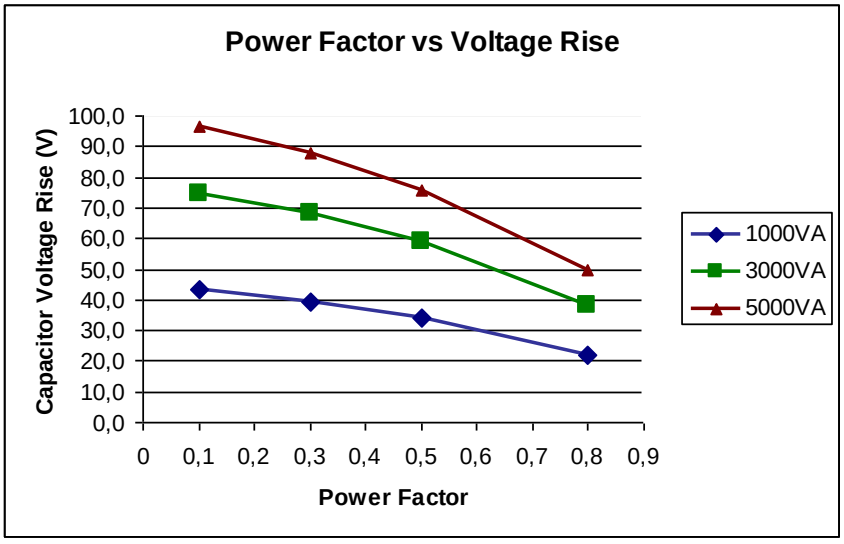



**Figure 6.4. Capacitor Voltage Rise vs Power Factor**

Note that, power factor of the electric motors are minimum 0.5, this is obtained for no load operation. For 0.5 power factor case, since the load is very low, voltage rise of the capacitor will not be problem. In other words, power factor ranges below 0.8 is not applicable for high power levels. From digure 6.4, maximum voltage rise at 0.8 power factor is 50V. We can say that this voltage rise for 2mF capacitor is acceptable for 310V output voltage. Furthermore, voltage rise can be reduced by increasing the capacitor value.

PFC stage must provide the Isolation of the overall converter. There are different isolated PFC stages. These are flyback converter, SEPIC converter and Cuk converter. In this section, SEPIC converter is selected in order to analyze the converter performance.

### 6.3.1 SEPIC With Synchronous Buck Converter

In this two-stage converter solution, as mentioned in the previous chapter, SEPIC converter has isolation and the power factor correction. On the other hand, synchronous buck converter generates the half wave rectified sinusoidal output voltage and manages to drive inductive loads. SEPIC with Buck Synchronous Converter is given in Figure 6.5.

SEPIC converter is used in order to obtain 500VDC output. UCC2817 controller is used in the simulation model. Performance of this topology is analyzed with PSIM circuit simulations. Its switching frequency is 20 kHz. For different output powers (1kVA, 3kVA and 5 kVA) and power factors (0.1, 0.5 and 1), total harmonic distortion of the output voltage is obtained at the result of simulations. Simulation results are given in Figure 6.6. These results are obtained in 50Hz operation. PSIM Version-7 simulation program is used for the simulations. Circuits used in simulations are given in Appendix B. Simulation parameters are given in Appendix C.

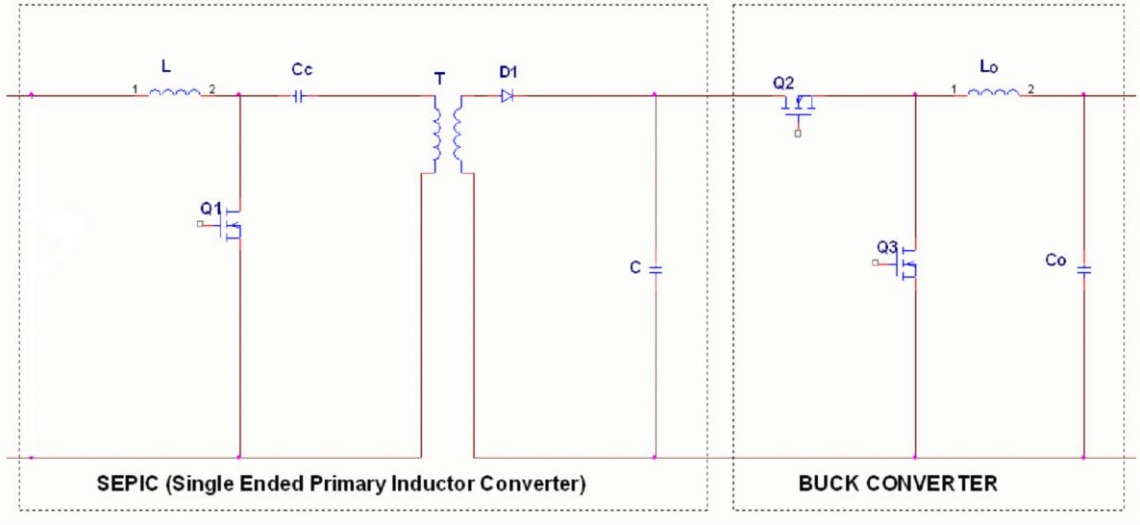



**Figure 6.5: SEPIC with Buck Synchronous Converter**

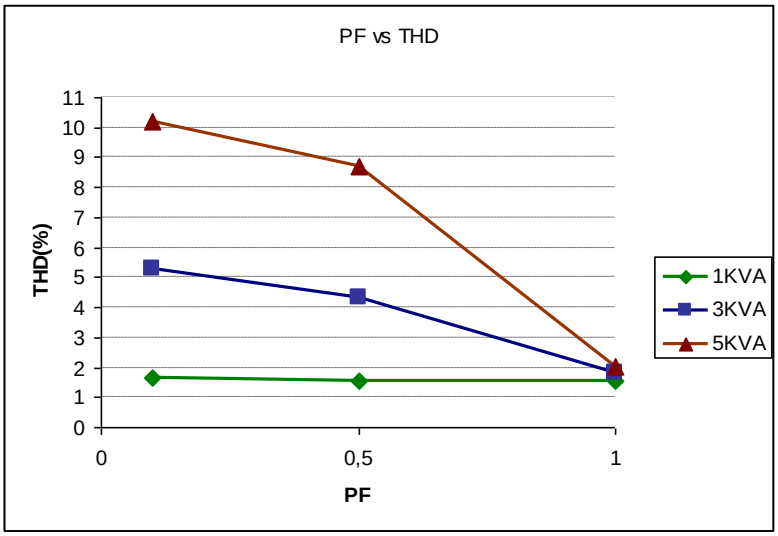



**Figure 6.6: Simulation Results- Power Factor vs THD For Diffent Power Levels**

In the simulation results, it is seen that as output power increases, lower power factors causes harmonic distortion in the output voltage In order to find out the

reason of this higher THD values at high powers , we can examine the output voltage waveform for 5 KVA and 0.1 power factor case given in Figure 6.7. The voltage waveform is distorted at the beginning of each half cycle. In order to understand the reason of this distortion, we must analyze the operation of the synchronous buck converter given in Figure 6.3. In mode 2, when the inductive current is turned back to the output capacitor, current flows through the output inductor, Lo. This operation has no problem in low power levels. However, for high power levels and for higher reactive powers (lower power factors), inductor causes a delay to the reactive current flow. Then during this delay duration, reactive current overcharges the output capacitor for a moment and causes voltage distortion as given in Figure 6.7.

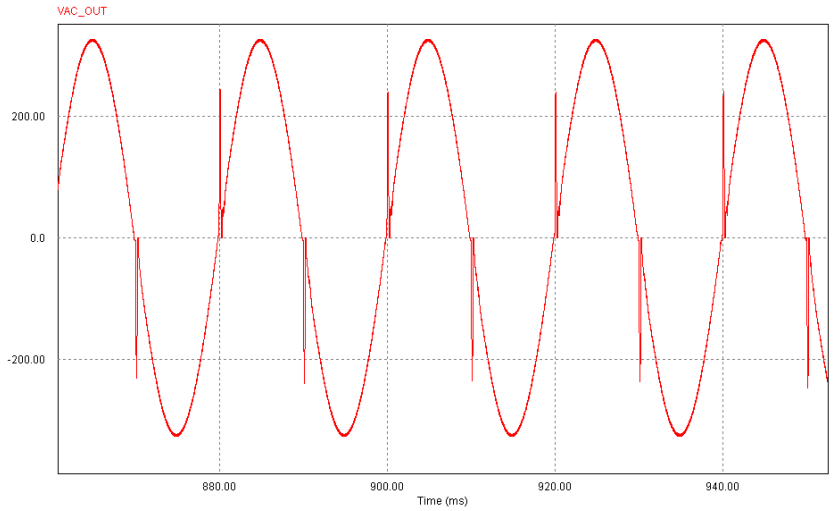
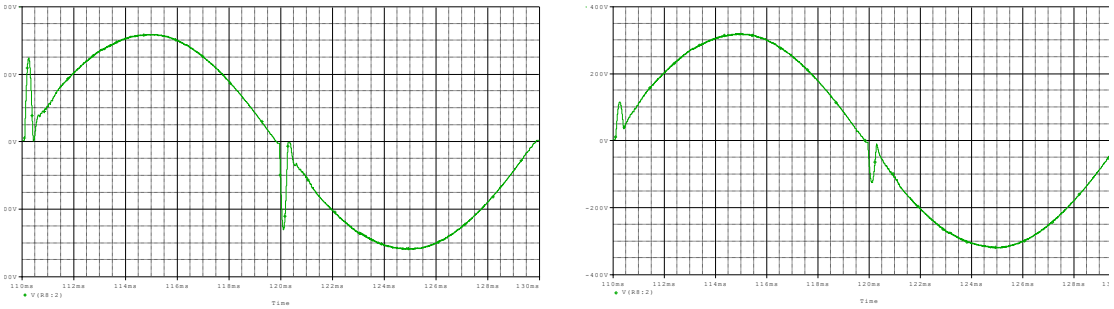



**Figure 6.7: Simulation Result- Output Voltage of the Inverter for 5KVA and PF=0.1**

In order to reduce the THD of the output voltage for high reactive power levels, output value of the output inductor (Lo in Figure 6.5) can be reduced and capacitor (Co in Figure 6.5) value can be increased. In Figure 6.8, output

voltages for 5KVA and 0.5 power factor is given. In Figure 6.8 (a), 500μH inductor and 20μF capacitor values are used in the buck converter. On the other hand, in Figure 6.8 (b), 250μH inductor and 40μF capacitor values are used. Voltage THD of the waveform given in Figure 6.8 (a) is 11.4%, whereas THD of the waveform given in Figure 6.8 (b) is 4.65%. It can be concluded that the voltage distortion decrease for lower inductor and bigger capacitor case.



(a) (b)

**Figure 6.8: Output Voltage at 5KVA, cosΦ=0.5 with Co=20μF and Lo=500μH (a) and Co=40μF and Lo=250μH (b)**

On the other hand, according to the power quality standard EN 50160 (*Voltage Characteristics in Public Distribution Systems*), permissible voltage THD for industry is 8%. From Figure 6.6, for 5KVA apparent power and power factor lower then 0.5, proposed topology does not satisfies the standard. However, for a 5KW induction machine, which will use this power supply, in practice 0.5 power factor is not feasible at full power. We can assume that power factor can not be less then 0.8 at full load. From this point of view, proposed power supply satisfies the THD value dictated by the standard.

Although, the proposed topology satisfies our requirements, the design of the converters, especially SEPIC is challenging. High voltage stress is obtained for

the transistor Q1 in Figure 6.5 due to the leakage inductance of the transformer. In order to reduce the voltage stress, additional snubber circuits can be used. However, these circuits reduce the efficiency of the converter. Different circuits can be used to overcome the voltage stress problem [15].

## 6.4 Discussion

In this section, implemented and proposed topologies are compared with conventional inverter topology. Firstly, implemented SMPS is compared with conventional PWM inverter topology. Afterwards, the proposed topology, SEPIC with synchronous buck converter, is compared with conventional unity power factor (UPF) PWM inverter topology.

### 6.4.1 Comparison of Implemented SMPS and Conventional PWM Inverter Topology

In the implemented topology, the target is isolating load from the source ground and obtaining a pure unpulsed sinusoidal output voltage. In the following paragraphs, this topology is compared with conventional PWM inverter topology.

About a 3 kW single phase inverter is taken as reference. The main cost of an inverter is its active elements, inductive components, capacitive components, and the heatsinks. The rest of the cost is electronics cost and is about the same for both topologies but a relatively small portion of the total. The frame is not considered in the evaluation. In evaluation of the volume, the same components are taken into consideration. Cost and volume of the conventional topology is taken as the base. The proposed topology cost is expressed as a percentage of that basis.

Implemented SMPS topology is given in Figure 6.9, conventional PWM inverter topology is given in Figure 6.10. Implemented topology contains a rectifier stage to rectify the sinusoidal input, a DC/DC converter stage to produce half wave

sine output and an inverter stage to obtain sinusoidal signal from the half wave sinusoidal signal. On the other hand, conventional topology contains rectifier stage rectify and an PWM inverter stage. The output of this PWM inverter contains pulses; a low pass filter is needed to obtain sinusoidal output voltage. Note that, both topologies do not contain power factor correction stages.

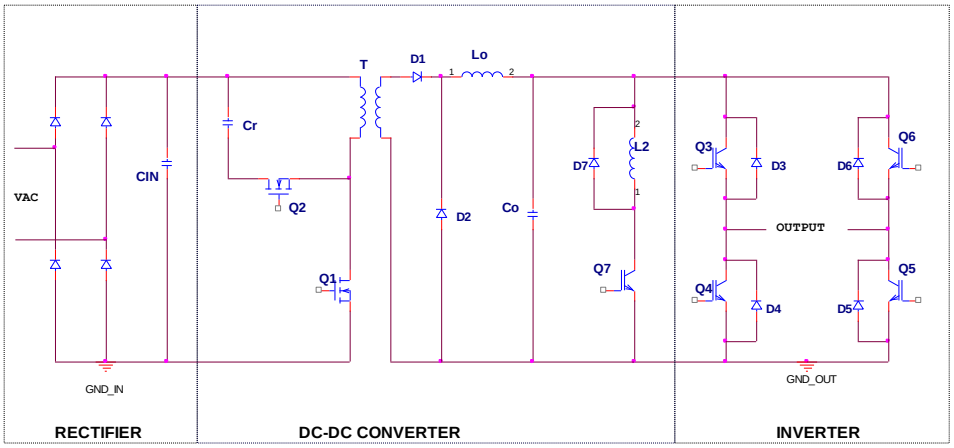



**Figure 6.9: Implemented SMPS Topology**

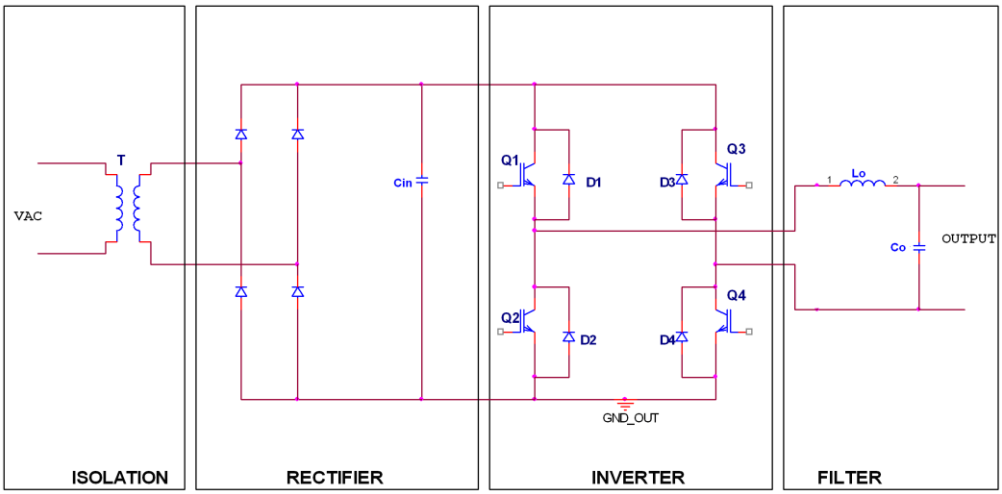



**Figure 6.10: Conventional PWM Inverter Topology**

Comparison of transistor costs is given in Table 6.1. In the conventional topology, output voltage is modulated by using the transistors Q1, Q2, Q3 and Q4 (see Figure 6.10). Fast switching transistors are required. While comparing transistor costs, IGBT's with 30A rated current and 600V rated voltage (IXGR40N60C2D1) are used. We take its cost as 1 pu (per unit). In the implemented circuit, transistor Q1 is used as the main transistor of the converter (see Figure 6.9). According to experiments, its voltage stress is below 600V. Since then main switch must be fast switching type, the same IGBT in the conventional inverter stage is used in comparison table. Also, transistor Q7 of implemented converter has same requirements as Q1. Then cost of Q7 is taken same as Q1. The active clamp transistor Q2 (see Figure 6.9) of the implemented converter has current stress about 1A. A low cost MOSFET switch can be used. In the comparison table, relative cost of the IRFPFC 40 transistor is used for Q2 transistor. In the inverter stage of the implemented circuit, low speed transistors can be used since their switching frequency is 50 Hz. In the comparison table, a low cost IGBT (IRG4PC40S) with 30A rated current and 1 KHz operating frequency is used for Q3, Q4, Q5 and Q6 (see Figure 6.9).

**Table 6.1: Comparison of the Transistor Costs**

| Transistor | Specifications | Transistor Cost | |
|---|---|---|---|
| | | Conventional | Implemented |
| Q1 to Q4 in Figure 6.10 | 4x IGBT, 30A, 600V, 25kHz | 4 x 1 pu = 4 pu | - |
| Q1 in Figure 6.9 | 1x IGBT, 30A, 600V, 25kHz | - | 1 pu |
| Q2 in Figure 6.9 | 1x MOSFET, 2A, 600V, 25kHz | - | 0.3 pu |
| Q7 in Figure 6.9 | 1x IGBT, 30A, 600V, 25kHz | - | 1 pu |
| Q3 to Q6 in Figure 6.9 | 4x IGBT, 30A, 600V, 50Hz | - | 4 x 0.4 pu = 1.6 pu |
| **Total Cost** | | **4 pu** | **3.9 pu** |

Beside transistor costs, heat sink volumes of both topologies are compared. It is assumed that volume of the heatsink is proportional to transistor losses. Then transistors losses are compared in order to obtain heat sink comparison. In Table 6.2, transistor losses of implemented and conventional topologies are compared. In the conventional topology, transistors modulating output voltage has switching and conduction losses. Conduction and switching losses of the transistors Q1 to Q4 in conventional topology (See Figure 6.9) are assumed to 1 pu (per unit). In the implemented topology main transistor, Q1 has also switching and conduction losses. Then, its losses are taken the same 2pu. Since the current rating of active clamp transistor is very low (1A), its total loss is taken as 0.1 pu. The transistor Q7 operates only at light loads, its losses are not included in heatsink calculations. Inverter transistors of the implemented topology have only conductions losses. These transistors are switched at zero crossings of the output voltage and have no switching losses.

**Table 6.2: Comparison of the Transistor Losses**

| Transistor | Condition | Transistor Losses | |
|---|---|---|---|
| | | Conventional | Implemented |
| Q1,Q2, Q3 and Q4 in Figure 6.10 | Conduction at 10A + switching at 10A 25 kHz | 4 x 2 pu = 8 pu | - |
| Q1 in Figure 6.9 | Conduction at 10A + switching at 10A 25 kHz | - | 2 pu |
| Q2 in Figure 6.9 | Conduction at 1A + switching at 1A 25 kHz | - | 0.1 pu |
| Q7 in Figure 6.9 | No losses at full load. | - | - |
| Q3, Q4, Q5 and Q6 in Figure 6.9 | Conduction at 10A | - | 4 x 1 pu |
| **Total Loss** | | **8 pu** | **6.1 pu** |

Transformers are compared by using the relationship of transformer area product and power handling capability. Its expression is given in Equation 6.5 [16].

$$Ap = \left(\frac{P \cdot 10^4}{K \cdot B_m \cdot f \cdot Ku \cdot K_j}\right)^{1.16} \quad [\text{cm}^4] \qquad (6.5)$$

This expression can be used for both topologies. In this equation,

- $A_p$ is the area product of the transformer core. It gives the product of core area and window area of the required core.

- P is apparent power, total of primary and secondary side power. In other words, total of input and output power of the transformer. For 50 Hz transformer of the conventional topology, it is P=2xPin where Pin the input power of the transformer [16]. For 3000W output power and 0.9 supply efficiency Pin= 3330W. Then P=6660W for conventional topology. For SMPS transformer apparent power is defined as P= $\sqrt{2}(Pin + Po)$ [16]. Pout the output power Po=3000W, Pin is the input power Pin=3330W. Then for the implemented topology, P=8883W.

- K is the waveform coefficient, for square wave K=4 (implemented topology ), for sine wave K=4.44 (conventional topology)

- $B_m$ is the flux density, for implemented topology it is $B_m$=0.3T (ferrite core is assumed), for conventional topology $B_m$=1.7T.

- f is the frequency, for implemented topology f=25000 Hz, for conventional topology f=50 Hz.

- Ku is the window utilization factor, Ku=0.4 is taken for both topologies.

- $K_j$ is the current density coefficient, it is given as $K_j$=468 for C type core (implemented topology) and (conventional topology) Kj=534 for lamination core [16].

Core of the high frequency transformer in implemented topology is a C-type core. Core of the conventional 50Hz isolation transformer is assumed to be a laminated core.

The relation between area product and transformer volume is given in equation 6.6 [16].

$$vol = Kv \cdot Ap^{0.75} \qquad [cm^3] \qquad (6.6)$$

In this equation, $K_v$ is the constant related to the core type. It is given for laminated core as $K_v$= 19.7 (conventional topology); for C-type core (implemented topology) as $K_v$= 17.9 [16].

By using equations 6.5 and 6.6, area products and volumes of the transformers are calculated. Results are given in Table 6.3. In the comparison, Volume of the transformer of implemented topology is taken as 1 pu (per unit).

**Table 6.3: Comparison of the Transformers**

| Condition | Area Product | Volume | Relative Volume | |
|---|---|---|---|---|
| | | | Conventional | Implemented |
| f=25 kHz and B=0.3 T | 24.5 $cm^4$ | 196 $cm^3$ | - | 1 pu |
| f=50Hz and B = 1.7 T | 2420 $cm^4$ | 6797 $cm^3$ | 34 pu | - |

Beside transformers, both topologies have filter inductors. Current of the filter inductor of the implemented topology (Lo in Figure 6.9) has DC component.

Equation 6.7 is used in order to obtain area product of the implemented converter's filter inductor [16].

$$Ap = \left(\frac{L \cdot I^2 \cdot 10^4}{B_m \cdot Ku \cdot K_j}\right)^{1.16} \quad [cm^4] \qquad (6.7)$$

In this expression:

- L is the inductance value. In our case it is 1.5 mH.
- I is the DC component of the inductor current. For 3000W output power and 310V output voltage, it is 9.68A.
- $B_m$ is the flux density, it is $B_m$=0.3T.
- Ku is the window utilization factor, Ku=0.4..
- $K_j$ is the current density coefficient, it is given as $K_j$=468 for C type core.

On the other hand, filter inductor of the conventional topology (Lo in Figure 6.10) has no DC component. The area product of this AC inductor is calculated by using the equation 6.8 [16].

$$Ap = \left(\frac{P \cdot 10^4}{4.44 \cdot B_m \cdot f \cdot Ku \cdot K_j}\right)^{1.14} \quad [cm^4] \qquad (6.8)$$

In this expression:

- P is the apparent power of the inductor, it is 3000VA.
- $B_m$ is the flux density, it is $B_m$=1.7T.
- f is the operating frequency of the AC current, it is 50 Hz.
- Ku is the window utilization factor, Ku=0.4.

- $K_j$ is the current density coefficient. Kj=534 for lamination core

By using equations, 6.7 and 6.8, areap products of inductors are calculated. After area product calculations, volumes are obtained by using Equation 6.6. Results are compared in Table 6.4. In the comparison, Volume of the inductor of implemented topology is taken as 1 pu (per unit).

**Table 6.4: Comparison of the Filter Inductors**

| Condition | Area Product | Volume | Relative Volume | |
|---|---|---|---|---|
| | | | Conventional | Implemented |
| L=1.5 mH and B=0.3 T | 41.8 $cm^4$ | 294 $cm^3$ | - | 1 pu |
| f=50Hz and B = 1.7 T | 852 $cm^4$ | 3106 $cm^3$ | 10.6 pu | - |

**Table 6.5: Comparison of the Capacitors**

| Capacitor | Type and Voltage | Relative Cost | |
|---|---|---|---|
| | | Conventional | Implemented |
| $C_{IN}$ = 2.2 mF in Figure 6.9 | Electrolytic capacitor, 450Vdc | - | 1 pu |
| Cr = 1 uF in Figure 6.9 | Low ESR, metallised polyester capacitor, 450Vdc | - | 0.05 pu |
| Co= 15 uF in Figure 6.9 | Low ESR, metallised polyester capacitor, 450Vdc | - | 0.15 pu |
| $C_{IN}$=2.2 mF in Figure 6.10 | Electrolytic capacitor, 450Vdc | 1 pu | - |
| Co =15 uF in Figure 6.10 | Low ESR, metallised polyester capacitor, 450Vdc | 0.15 pu | |
| **Total Cost** | | **1.15 pu** | **1.20 pu** |

In Table 6.5, a capacitors cost of two topology is compared. In the conventional topology, an input capacitor is used after rectifier and a filter capacitor is used at the output filter. In the implemented topology, same two capacitors are used. In addition, a clamp capacitor is used in the active clamp stage.

In table 6.6, costs of the topologies are compared. In this table, heatsink cost is obtained form transistor losses. In addition, cost of the transformers and inductors are obtained form their volumes by assuming that each per unit volume costs 1 pu. All results are normalized to conventional topology results.

**Table 6.6: Cost Comparison of the Conventional and Implemented Topologies**

| Parameter | Conventional (Fig. 6.10) | | Implemented (Fig. 6.9) | |
|---|---|---|---|---|
| | Per Unit | % | Per Unit | % |
| **Transistor Cost** | 4 pu | 100 % | 3.9 pu | 97.5% |
| **Capacitor Cost** | 1.15 pu | 100 % | 1.2 pu | 104 % |
| **Heat sink Cost** | 8 pu | 100 % | 6.1 pu | 76.2% |
| **Transformer Cost** | 34 pu | 100 % | 1 pu | 2.94 % |
| **Inductor Cost** | 10.6 pu | 100 % | 1 pu | 9.43 % |

From Table 6.6, it is seen that, transistor and capacitor costs of two topologies are nearly the same. With implemented topology, heat sink cost is reduced by 24%. With implemented topology, transformer cost is significantly reduced; it is only 2.94% of the conventional topology. In addition, inductor cost of the implemented typology is only 9.43 % of the conventional topology.

Beside cost, volume of the power supplies is also important. From Table 6.3 and 6.4, volumes of the magnetic elements are reduced with the implemented topology. We can say that, transformer volume is decreased by % 98 and inductor volume is decreased by % 90 with the implemented topology, giving a great volume advantage.

### 6.4.2 Comparison of the Proposed UPF SMPS and Conventional UPF PWM Inverter Topology

The topologies compared in the previous section do not have sinusoidal input current. On the other hand, as mentioned in previous sections, industry needs unity power factor (UPF) power supplies and motor drivers.

In this thesis a UPF SMPS topology is proposed. It is given in Figure 6.11. On the other hand, UPF can be obtained by the conventional UPF PWM inverter topology is given in Figure 6.12. In this section comparison of these two topologies are presented.

Proposed topology contains a rectifier stage to rectify the sinusoidal input, a SEPIC converter to DC voltage and provide PFC, a buck converter to produce half wave sine voltage and inverter stage to obtain sinusoidal signal from the half wave sinusoidal signal. On the other hand, conventional UPF topology contains rectifier stage rectify, a PFC stage, a PWM inverter stage and a filter stage.

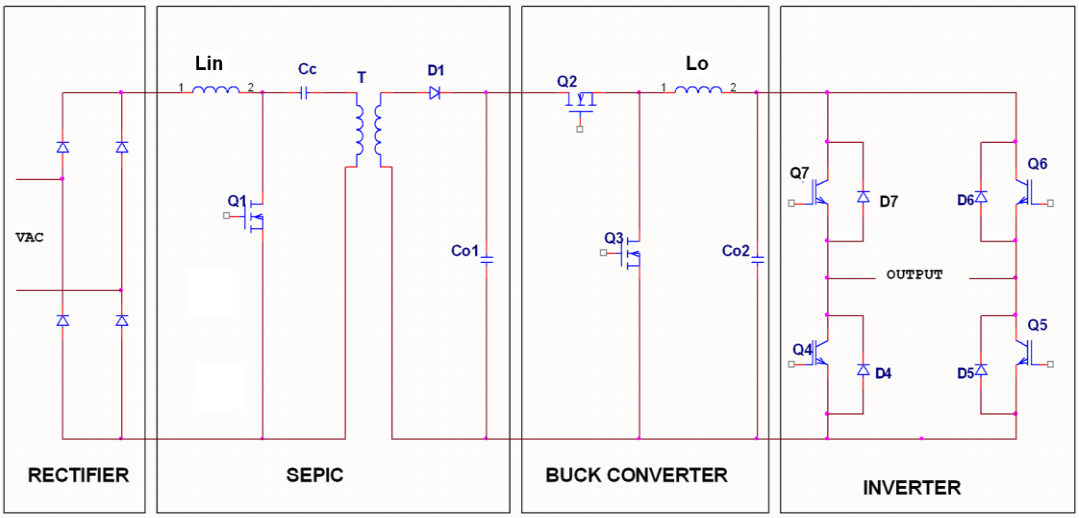



**Figure 6.11: Propesed UPF SMPS Topology**

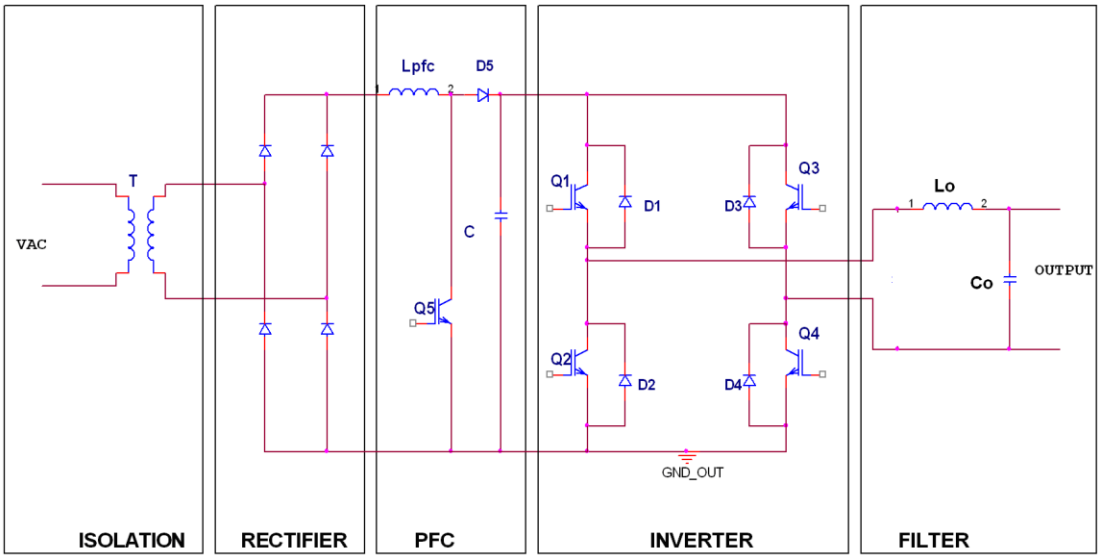



**Figure 6.12: Conventional UPF PWM Inverter Topology**

Comparison of transistor costs is given in Table 6.7. In conventional UPF inverter topology, 5 fast switching transistors are required. While comparing transistor costs, IGBT's with 30A rated current and 600V rated voltage (IXGR40N60C2D1) are used for these transistors. We take its cost as 1 pu (per unit). In the proposed circuit, transistor Q1 is the transistor of the SEPIC converter (see Figure 6.11). A fast switching transistor with 1200V rated voltage is required. Relative price of IRGP30B120KD is used in comparison table. In the inverter stage of the implemented circuit, low speed transistors can be used since their switching frequency is 50 Hz. In the comparison table, a low cost IGBT (IRG4PC40S) with 30A rated current and 1 KHz operating frequency is used for Q4, Q5, Q6 and Q7 (see Figure 6.11).

**Table 6.7: Comparison of the Transistor Costs for UPF Topologies**

| Transistor | Specifications | Transistor Costs | |
|---|---|---|---|
| | | Conventional UPF | Proposed UPF |
| Q1,Q2, Q3 and Q4, Q5 in Figure 6.12 | 5x IGBT, 30A, 600V, 25kHz | 5 x 1 pu = 5 pu | - |
| Q1 in Figure 6.11 | 1x IGBT, 30A, 1200V, 25kHz | | 1.5 pu |
| Q2 and Q3 in Figure 6.11 | 2x IGBT, 30A, 600V, 25kHz | - | 2 x 1 pu = 2 pu |
| Q4, Q5, Q6 and Q7 in Figure 6.11 | 4x IGBT, 30A, 600V, 50Hz | - | 4 x 0.4 pu = 1.6 pu |
| **Total Cost** | | **5 pu** | **5.1 pu** |

Transistors losses of the UPF topologies are compared in Table 6.8. In the conventional UPF topology, all transistors have both conduction and switching losses. Each loss is assumed to 1 pu (per unit). In the proposed, transistors used in SEPIC and Buck converter have both switching and conduction losses. Inverter transistors of the proposed topology (Q4 to Q7 in Figure 6.11) have only conductions losses.

**Table 6.8: Comparison of the Transistor Losses for UPF Topologies**

| Transistor | Condition | Transistor Losses | |
|---|---|---|---|
| | | Conventional UPF | Proposed UPF |
| Q1,Q2, Q3 and Q4, Q5 in Figure 6.12 | Conduction at 10A + switching at 10A 25 kHz | 5 x 2 pu = 10 pu | - |
| Q1,Q2 and Q3 in Figure 6.11 | Conduction at 10A + switching at 10A 25 kHz | - | 3 x 2 pu = 6 pu |
| Q4, Q5, Q6 and Q7 in Figure 6.11 | Conduction at 10A | - | 4 x 1 pu |
| **Total Loss** | | **10 pu** | **10 pu** |

Transformers properties are the same as given in the previous section. Transformer area product and volume calculations given in the previous section is also valid for this section. In addition, filter inductor calculations and volumes given in Table 6.4 are the valid for this section.

Both topologies have PFC inductors. If we assume that the operating frequencies of the PFC stages are the same, then sizes, volumes and costs of PFC inductors are the same.

In Table 6.9, capacitors of the conventional and proposed UPF topologies are compared. In the conventional topology, a input capacitor is the PFC stage and a filter capacitor is used at the output filter. In the proposed UPF topology, in SEPIC converter a charge balance capacitor Cc and an output capacitor $C_{o1}$ is used. In addition, an output filter capacitor ($C_{o2}$)is used in Buck converter. In Table 6.9, capacitor types and voltages are presented.

**Table 6.9: Comparison of the Capacitors**

| Capacitor | Type and Voltage | Relative Cost | |
|---|---|---|---|
| | | Conventional UPF | Proposed UPF |
| $C_{o1}$ = 2.2 mF in Figure 6.11 | Electrolytic capacitor, 450Vdc | - | 1 pu |
| Cc = 4 uF in Figure 6.11 | Low ESR, metallised polyester capacitor, 450Vdc | - | 0.1 pu |
| Co= 15 uF in Figure 6.9 | Low ESR, metallised polyester capacitor, 450Vdc | - | 0.15 pu |
| $C_{IN}$=2.2 mF in Figure 6.12 | Electrolytic capacitor, 450Vdc | 1 pu | - |
| Co =15 uF in Figure 6.12 | Low ESR, metallised polyester capacitor, 450Vdc | 0.15 pu | |
| **Total Cost** | | **1.15 pu** | **1.25 pu** |

In Table 6.10, costs of the UPF topologies are compared. In this table, heatsink cost is obtained form transistor losses. In addition, cost of the transformers and filter inductors are obtained from the previous section. All results are normalized to conventional topology results.

**Table 6.10: Cost Comparison of the Conventional and Proposed UPF Topologies**

| Parameter | Conventional (Fig. 6.12) | | Implemented (Fig. 6.11) | |
|---|---|---|---|---|
| | Per Unit | % | Per Unit | % |
| **Transistor Cost** | 5 pu | 100 % | 5.1 pu | 102 % |
| **Capacitor Cost** | 1.15 pu | 100 % | 1.25 pu | 109 % |
| **Heat sink Cost** | 10 pu | 100 % | 10 pu | 100 % |
| **PFC Inductor Cost** | 1 pu | 100 % | 1 pu | 100 % |
| **Transformer Cost** | 34 pu | 100 % | 1 pu | 2.94 % |
| **Filter Inductor Cost** | 10.6 pu | 100 % | 1 pu | 9.43 % |

From Table 6.10, it is seen that, transistor, capacitor, PFC inductor and heatsink costs of two topologies are nearly the same. On the other hand, transformer cost is significantly reduced with the proposed topology; it is 2.94% of the conventional. In addition, cost of the filter inductors is reduced to 9.43% of conventional. As a result, we can conclude the proposed topology offers significantly reduced transformer and filter costs.

In addition to the costs, the proposed topology offers significantly reduced transformer and filter volumes. The volume of the transformer and inductor are decreased by 97% and 90%, respectively.

## 6.5 Conclusion

In this thesis, a switch mode power supply producing half wave sine output is designed and implemented. The designed power supply is used with an inverter stage in order to generate sinusoidal signal. Active clamp forward converter topology is selected for the converter stage. The converter is designed for 1500W output power.

Circuit simulations are performed for resistive loads. At full resistive load, a pure sinusoidal output voltage is obtained with 3% voltage THD. However, it is observed that voltage THD begins to increase for light resistive loads. It is concluded that lower load levels can not fully recharge the output capacitor of the converter and causes distortion. A similar problem occurred with inductive and capacitive load simulations. For capacitive and inductive loads the reactive energy returning to the supply overcharges the output capacitor and causes serious voltage distortions. In order to solve the problem, active clamp converter topology is modified: an additional switch, inductor and diode are used in order to recharge the capacitor and create a return path for the reactive energy. Simulations are performed with the modified topology.

In resistive load simulations, it is observed that, for light loads, the modification manages to recharge the output capacitor and prevents voltage distortion. However, efficiency of the power supply is significantly reduced for light loads due to the power dissipated in the additional transistor. On the other hand, at full resistive load, the effect of the modification to the efficiency is negligible; efficiency of the converter at full resistive load is high. In inductive and capacitive load simulations, the modification prevents overcharge of the output capacitor but the switching action of the additional switch causes voltage distortion. The mount of the distortion increases for higher output power levels.

After simulations, designed power supply is implemented as an experimental set-up. Experiments are performed with this set-up for resistive and inductive

loads. In resistive load experiments, power supply is operated for steady state and dynamic conditions. It is observed that for resistive load experiments power supply operates successfully. A nearly pure sinusoidal output voltage with 4% THD is obtained at resistive load experiments. As output power increase, THD value slightly increases for resistive loads. On the other hand, for inductive loads THD value seriously increases as output power increases. Then, it is concluded that the modified active clamp forward converter topology is not appropriate for inductive and capacitive loads.

Implemented topology is compared with conventional WPM inverter topology. It is concluded that, implemented topology significantly reduces both cost and volume of the transformer, filter inductor and heat sink.

Proposed topology is compared with conventional UPF inverter topology. It can be stated that, cost and volume of the transformer and filter inductor significantly reduces with the proposed topology.

In order to solve the drawback of the implemented topology, other topologies are examined. An isolated SEPIC with synchronous buck converter topology is proposed.

To sum up:

a) The implemented power supply operates successfully with resistive loads.

b) The implemented topology reduces volume of isolation transformer, heat sink and filter inductor.

c) The implemented power supply has problems with inductive and capacitive load. These type loads cause distortion at the output voltage.

d) Input current of the power supply is not sinusoidal. A PFC stage is required.

e) In order to solve inductive and capacitive load driving problems and provide sinusoidal input current, an isolated SEPIC with synchronous buck converter topology is proposed. Such a configuration appears to offer cost and volume advantages in implementing one phase variable frequency variably voltage inverters or uninterruptible power supplies.

# REFERENCES


[1] ŞEDELE, Serkan, “A Novel Approach For Synthesizing Sinus Waveforms At Power Level “ METU M. Sc. Thesis, 2004.

[2] Ericsson Power Modules, The Powerbook, 4th Edition, 2003. http://www.ericsson.com/powermodules

[3] RASHID, Muhammed H., “Power Electronics, Circuits,Devices and Applications”, Prentice Hall, 3rd Edition, 2003.

[4] BROWN, Marty, “Power Supply Cookbook”, Newnes, 2nd Edition, 2001.

[5] ANDREYCAK, Bill, “Active Clamp and Reset Technique Enhances Forward Converter Performance”, Texas Instruments Application Note, 2001.

[6] MANIKTALA, Sanjaya, “Switching Power Supply Design & Optimization”, McGraww-Hill Professional Engineering, 2004.

[7] MAPPUS, Steve, “Active Clamp Transformer Reset: High Side or Low Side?”, Texas Instruments Application Note, 2004.

[8] AÇIK Adnan, ÇADIRCI Işık, “Active Clamped ZVS Forward Converter With Soft-Switched Synchronous Rectifier” Turkish Journal of Electrical Engineering and Computer Sciences, 2002, Vol. 10, pp. 473-491.

[9] EPCOS, “Ferrites and accessories”, Application Notes, 2006.

[10] Texas Instruments, “Inductor and Flyback Transformer Design” Application Note, 2001.

[11] DIXON Loyd H., Control Loop Cookbook, Texas Instruments Application Note, 2002.

[12] Epcos, Ferrite Magnetic Design Tool, Version 4.0, 2003. www.epcos.com

[13] http://ludens.cl/Electron/Thermal.html

[14] MITCHELL Dan, MAMMANO Bob, “Designing Stable Control Loops”, Texas Instruments Application Note, 2002.

[15] ATHALYE Praneet, MAKSIMOVIC, Dragan, ERICKSON Robert, “ High-Performance Front-End Converter for Avionics Applications ” IEEE Transactions On Aerospace and Electronic Systems, 2003, Vol. 39, pp. 462-470.

[16] MCLAYMAN Colonel William T., “Transformer and Inductor Design Handbook”, Marcel Dekker Inc.,1978.

# APPENDIX A

# THEORETICAL INFORMATION

## A. 1 Active Clamp Forward Converter Theory of Operation

In this section, operation modes of the active clamp forward converter are analyzed by using Figure A.1. Here, $C_A$ and $D_A$ are the output capacitance and body diode of the main switch $Q_A$; $C_C$ and $D_C$ are the output capacitance and body diode of the clamp switch, $Q_C$, respectively. $V_{IN}$ is the input capacitor voltage; $V_{CR}$ is initial voltage of the clamp capacitor.

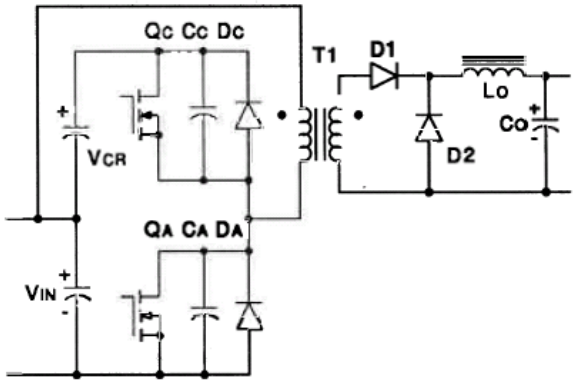



**Figure A.1: Active Clamp Forward Converter**

Waveforms of the active clamp forward converter are presented in Figure A.6 . VgsQA and VgsQC are the gate drive voltages of the main and clamp switches,

respectively. $V_{PR}T1$ and $I_{PR}T1$ are the voltage and current of the primary side, respectively. $I_{MAG}$ is the magnetizing current of the transformer. $V_{DS}Q_A$ and $V_{DS}Q_C$ are the Drain-Source voltages of the main and clamp switches, respectively. $I_DQ_A$ and $I_DQ_C$ are drain currents of the main switch and clamp switch, respectively. $I_{D1}$ and $I_{D2}$ are currents diode D1 and D2, respectively

In this section, one complete switching period is divided into eight individual time intervals (modes). Active clamp forward converter circuits for Mode-1 to Mode-4 are given in Figure A.2; circuits for Mode-5 to Mode-8 are given in Figure A.3.

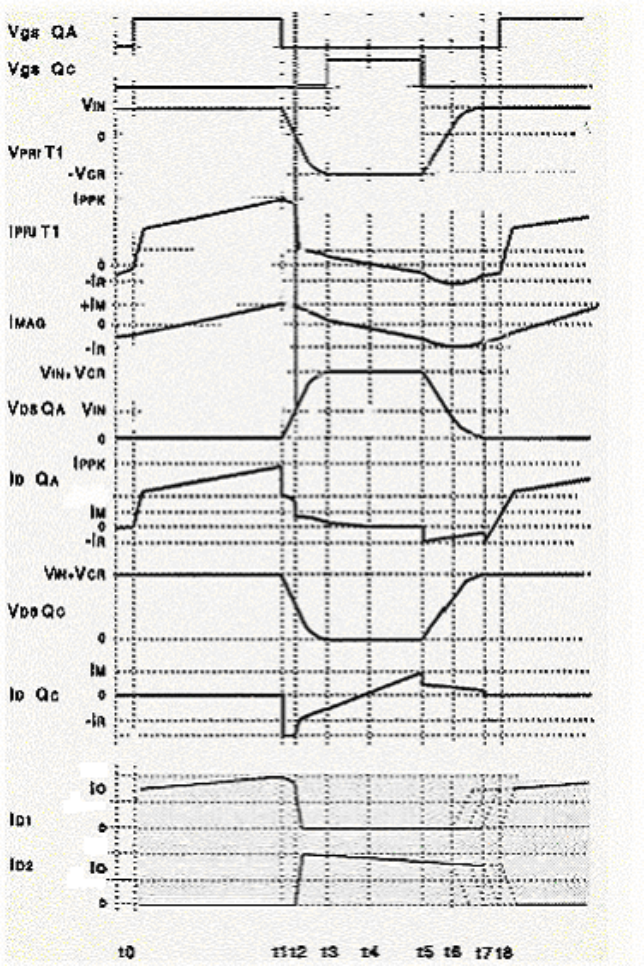



**Figure A.2: Active Clamp Forward Converter Waveforms**

Mode-1 (t0 to t1): Power Transfer Mode

This mode starts at time t0 when the main switch $Q_A$ is turned ON. Power is transferred from the primary to the secondary via the transformer. Then, this mode is called power transfer mode. The transformer primary current ($I_{PR}T1$) will build to the reflected load current (Iout x N where $N=N_S/N_P$) at the rate of input voltage $V_{IN}$ divided by the transformers leakage inductance. The current in the transformer secondary also rises, forward biasing diode D1. Current previously flowing in diode D2 is decreasing by the same amount rising in D1 such that sum of two equals the full load current. Primary current is the sum of three individual currents, the reflected output load current, the reflected output inductor charging current and also the primary magnetizing current.

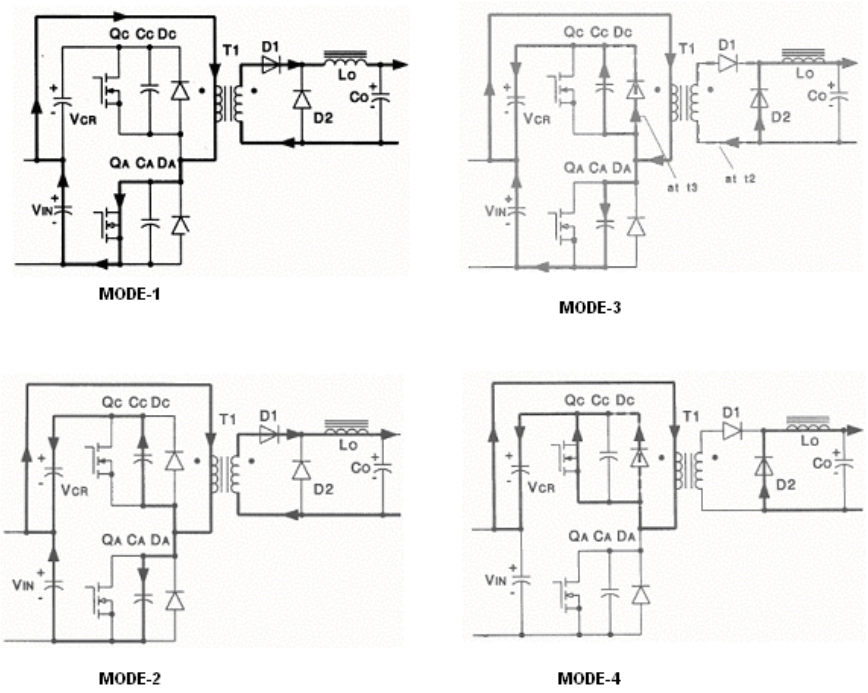



**Figure A.3: Active Clamp Forward Converter: Mode-1 to Mode- 4**

Mode-2: Linear Transition Mode (t1 to t2)

This mode begins at time t1 when $Q_A$ is turned OFF. Instantly, the current in the MOSFET device is diverted from its channel ($Q_A$) to its output capacitance, $C_A$. $C_A$ charges very quickly with the reflected load current flowing in the primary. The voltage across the main MOSFET ($Q_A$) rises linearly while the voltage across the clamp MOSFET ($Q_C$) decreases linearly. Then, this mode is called linear transition mode. This activity continues until time t2 when $C_A$ is fully charged to the input voltage ($V_{IN}$) and the voltage across $C_C$ has decayed from its initial value of Vcr to (Vcr -$V_{IN}$). This mode ends at time t2 when the transformer's primary voltage reaches zero. On the secondary side, it assumed that the entire load current continues to flow only through diode D1 during this interval. As the transformer voltage collapses to zero at t2, this situation could change depending on the design, magnetic coupling and placement of the leakage inductances in the physical transformer.

Mode-3: Resonant Transition Mode (t2 to t3)

This mode begins at time t2 when the transformer primary voltage has reached zero. It is also reflected to its secondary .This causes the full load current to transfer from diode D1 to D2 at a rate determined primarily by the secondary leakage inductance, but is all flowing in D2 at time t2. The transformer voltage continues its reversal from zero on towards the clamp voltage, Vcr. This transition is a resonant one because the previous catalyst of reflected load current is now gone with D2 conducting. Reverse biasing of D1 also allows the reversal of transformer’s voltage Current in the clamp switch $Q_C$ is negative during this interval as the output capacitance is discharging. This mode ends at time t3 when transformer voltage reaches the clamp reset voltage, -Vcr.

Mode-4: Passive Reset Mode (t3 to t4)

This mode begins at time t3 when the transformer primary voltage reaches the clamp voltage, -Vcr. Also at time t3 the clamp switch $Q_C$ is turned ON which

allows the reset current to transfer from the device's body diode to its channel, generally providing a lower impedance path. This mode is called passive reset mode because from time t3 until t4, the energy stored in the transformer's magnetizing inductance is transferred to the clamp capacitor. Mode-4 ends at time t4 when the primary current reaches zero. Note that, the main goal of turning the reset switch on is, in the next mode, to provide a path for current to flow from the clamp capacitor reservoir to the transformer primary to facilitate the Zero Voltage Transition.

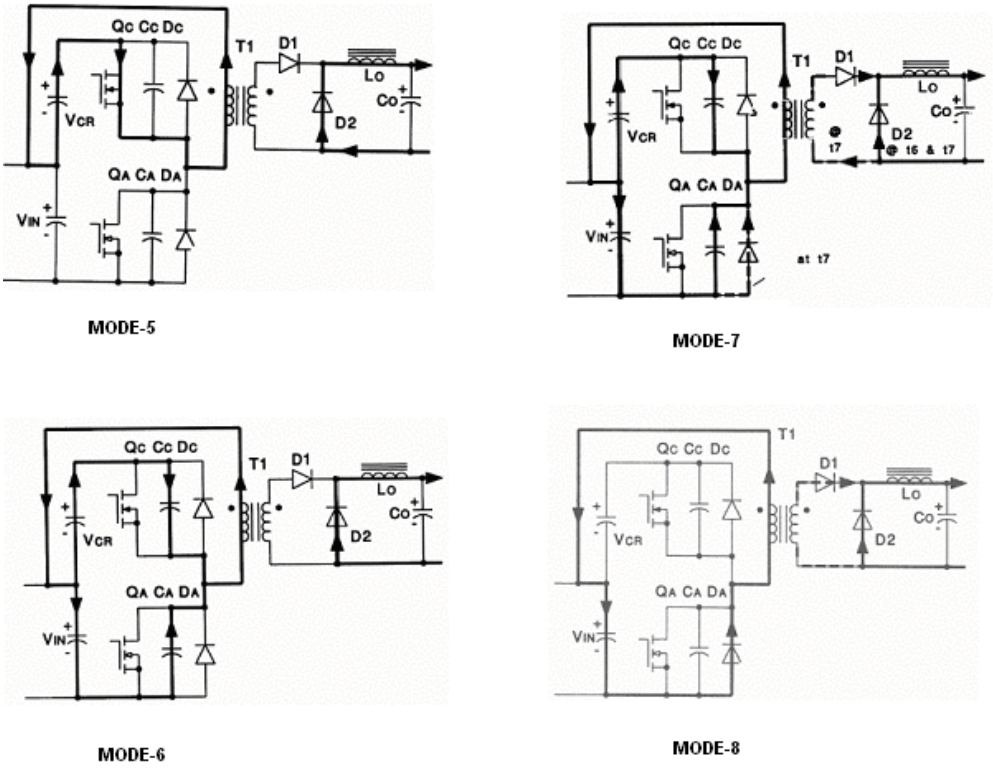



**Figure A.4 : Active Clamp Forward Converter: Mode-5 to Mode- 8**

Mode-5: Active Reset Mode (t4 to t5)

This mode begins at time t4 when the primary current reaches zero. The transformer is actively reset by switch $Q_C$ to the clamp voltage, Vcr. The magnetizing current is driven negative by the clamp circuit, storing energy in the magnetizing inductance. This will be used later to facilitate the Zero Voltage Transition. Primary current initially rises at the rate determined by the clamp voltage divided by the magnetizing inductance (Vcr/Lmag). This mode ends at time t5 when the clamp switch is turned OFF.

Mode-6: Resonant Transition Mode (t5 to t6)

This mode begins at time t5 when the clamp switch is turned OFF. This causes the primary current to divert from the device's channel ($Q_C$) to its output capacitance ($C_C$). The voltage across the clamp switch begins to increase. The transformer primary voltage similarly begins to collapse, but note that the magnetizing current is still increasing from its level at time t5. Even though the voltage across the magnetizing inductance is decreasing, there is still voltage across it until time t6 causing the current to increase, but at a reduced rate. Note also that a change has occurred in the drain current of the main switch, $Q_A$. No current was flowing in the device during the previous interval timing, but it does begin at time t5. The drain of $Q_A$ was held at the clamp voltage (Vcr) while the clamp switch $Q_C$ was ON until 15. Once turned off, the primary current simultaneous charges the clamp switch output capacitor ($C_C$) and discharges the main switch output capacitance $C_A$. $Q_A$ instantly sees some of the primary current to discharge its output capacitance which continues through this, and the next timing interval. On the secondary side, output inductor is still discharging its stored energy, diode D2 is commutating this current to the load, and D1 is off and reversed biased. This mode ends at time t6 when the voltage across the transformer is zero and the primary current has reached its lowest negative value (Ir) for the switching cycle.

Mode-7: Resonant Transition Mode (t6 to t7)

This mode begins when the voltage across the transformer is zero. The resonant transition established in the previous timing interval continues through this mode, but with a few minor differences. The primary current has reversed its slope, and decreases towards zero. The transformer voltage reverses to the input voltage $V_{IN}$. This resonant mode is supplied by the energy stored in the magnetizing inductance from the active reset mode (mode-5). Enough inductive energy must have been stored to overcome the opposing capacitive energy requirements of the two MOSFET switches, $Q_A$ and $Q_C$. When time t7 is reached, the main switch $Q_A$ is positioned with zero volts across it due to the active reset technique and resonant circuit elements. The active clamp switch is positioned to its highest amplitude with the full input and clamp voltage across its drain to source terminals. Current flowing is very low and is used to maintain the switches clamped in this position. Depending on the secondary circuit inductance and coupling to the primary winding, the load current could transfer from D2 to D1 during this mode. This mode ends at time t7 when the drain source voltage of the main switch is zero.

In order to zero switch the main transistor QA under zero voltage condition, ın enough inductive energy must be stored in the leakage and magnetizing inductances to overcome the opposing capacitive energy demands of the transistor output capacitances. This condition can expressed as given in Equation A.1.

$$\frac{1}{2} L_{mag} \cdot {I_m}^2 + \frac{1}{2} L_{lkg} \cdot {I_{pri}}^2 > \frac{1}{2} \cdot Cr \cdot (V_{IN} + V_{CR})^2 \qquad \text{(A.1)}$$

In this equation, $L_{mag}$ is the magnetizing inductance of the transformer; $I_m$ is the magnetizing current;, $L_{lkg}$ is the primary leakage inductance of the transformer; $I_{pri}$ is the primary current; $C_R$ is the total resonant capacitance, the parallel

combination of the two MOSFET output capacitors in parallel with the transformer primary capacitance; $V_{IN}$ is the input voltage and $V_{CR}$ is the clamp capacitor voltage.

Mode-8: Circulation Mode (t7 to t8)

This mode begins at time t7 when the drain source voltage of the main switch is zero. This interval is used to accommodate all resonant circuit tolerances, ranges of input voltage and magnetizing current. This brief mode ends when the main switch is turned ON at time t8 or t0 of the switching cycle.

## A. 2 Control Techniques in DC-DC Converters

Switching power supplies use closed-loop feedback to achieve design objectives for line and load regulation and dynamic response. Output voltage is controlled with duty cycle control. There are three control techniques in DC/DC converters:

- Voltage Mode Control Technique
- Peak Current Mode Control Technique
- Average Current Mode Control Technique

### A.2.1 Voltage Mode Control Technique

Voltage mode control technique is the oldest and simplest control technique. In voltage mode control, a pulse width modulator controls the duty cycle of the main switch. A basic voltage control loop is given in Figure A.5.

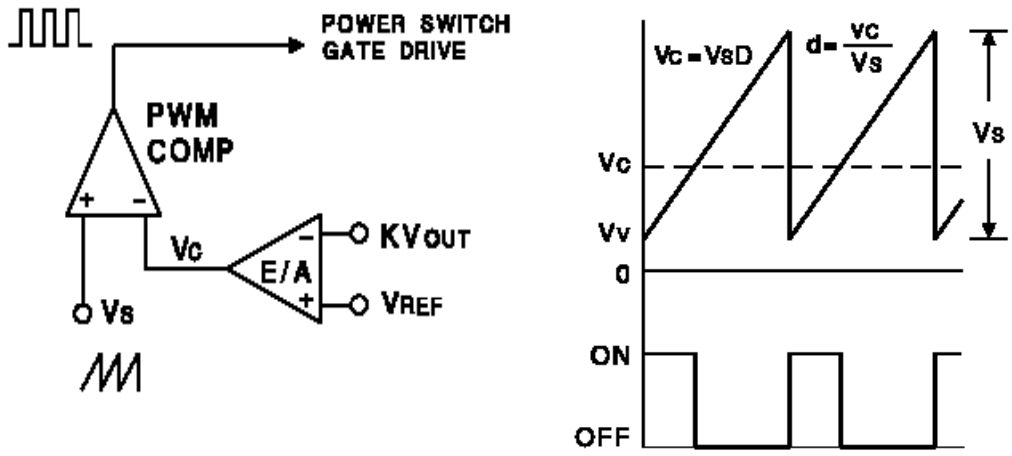



**Figure A.5: Voltage Mode Control Scheme and Waveforms**

The output voltage ($V_{OUT}$) of the converter is compared with a reference voltage $V_{REF}$ and the error amplifier E/A generates a control voltage $V_C$. PWM comparator compares the control voltage with a fix frequency saw tooth signal and generates the gated drive voltage. The frequency of the saw tooth signal is the switching frequency of the converter. Duty cycle D is controlled by the control voltage Vc according o the relationship in the following equation:

$$D = \frac{V_C}{V_S} \qquad \text{(A.2)}$$

where $V_S$ is the amplitude of the saw tooth signal.

The disadvantages of voltage mode control technique are its poor line regulation and poor dynamic response. There is no voltage feed forward to anticipate the affects of input voltage changes. Converter has a slow response to sudden input changes. Moreover, control changes must propagate through the output filter poles to make the desired output correction. This results in poor dynamic response. The advantage of the voltage mode control technique is its simplicity.

### A.2.2 Peak Current Mode Control Technique

Peak current mode control (CMC) technique is similar to voltage mode control technique. The difference is the saw tooth signal in peak CMC is not derived from a ramp generator as with VCM. In peak CMC the ramps is actually the inductor ripple current, as it rises while the switch is on, translated into a voltage by a current sense resistor. This ramp is compared with the control voltage by the PWM comparator. The main switch is tuned off when the current rises to the level of the control voltage. The control voltage determines the peak inductor current. The inner current loop directly controls the duty ratio and outer voltage loop controls the inductor current. In Figure A.6, a peak current mode controlled forward converter and its waveforms are given. Since the primary current is equal to the inductor current divided by turn's ratio, the controller circuit is on the primary side.

The advantage of peak CMC is its better line regulation. Since peak CMC has inherit voltage feed forward, it responds instantaneously to the input voltage changes. The disadvantage of this control technique is, it controls peak current instead of average current. The peak-to-average error is quite large, especially at light loads and the correction is done by the outer voltage loop with a poor dynamic response. Moreover, this method is extremely susceptible to noise. The current ramp is usually quite small compared to the control voltage level. When the main switch is turned on, noise is generated. This noise can couple at the comparator input and turn off the switch. A compensating ramp, with slope equal to the inductor current down slope, is required to the comparator input to eliminate the instability.

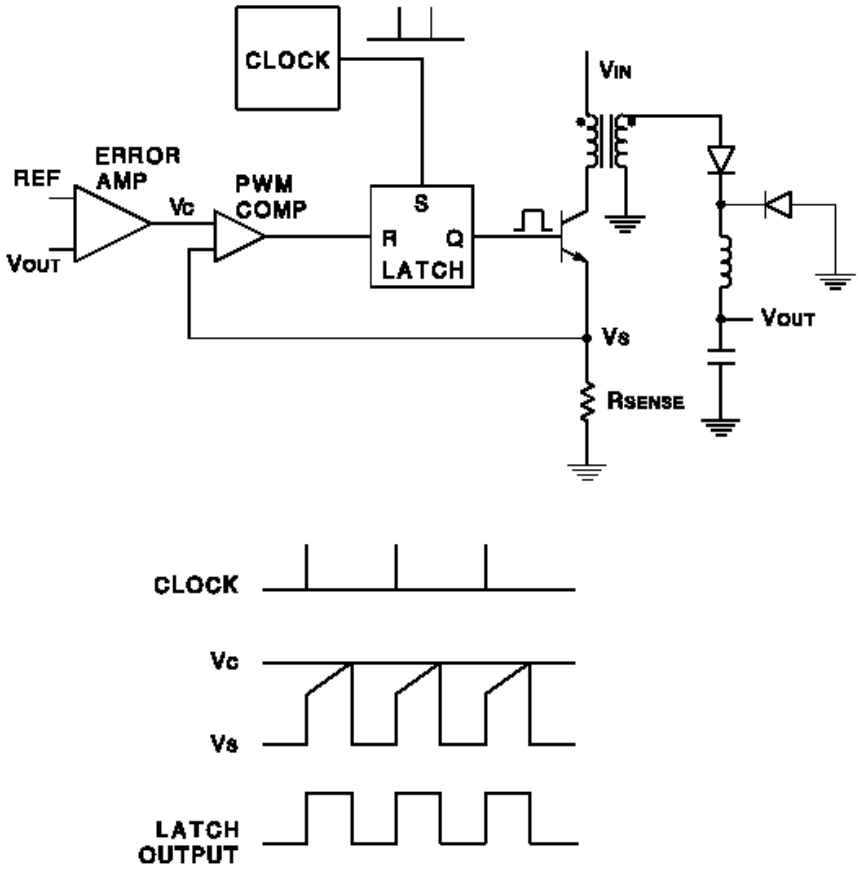



**Figure A.6: Peak Current Mode Controlled Forward Converter**

## A.2.3 Average Current Mode Control Technique

The drawbacks of the peak current mode control technique are related to its low internal current loop gain. Average CMC technique solves this problem by adding an error amplifier to the internal to the current loop.

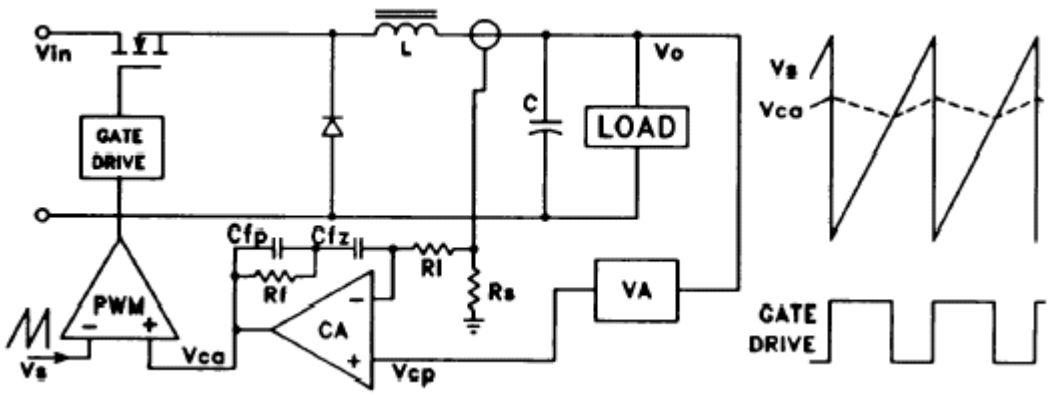



**Figure A.7: Average Current Mode Control Circuit and Its Waveforms**

In Figure A.7, average current mode control circuit and its waveforms are given. Inductor current is sensed through a resistor. The sensed voltage is compared with voltage $V_{CP}$ which sets the desired inductor current. The differential, representing the current error, is amplified by the current amplifier (CA). Output of the CA is compared to a saw tooth ramp to determine the duty cycle.

## A.3 Continuous and Discontinuous Conduction Mode in Forward Converter

### A.3.1 Continuous Conduction Mode

When circuit operated in continuous conduction mode, inductor current is non-zero. For continuous conduction mode of operation, regarding the operation in secondary side of the converter, there are two circuit states: State-1 main switch is ON, State-2 the main switch is OFF (see Figure A.8). In Figure A.9 inductor voltage and current waveforms are given.

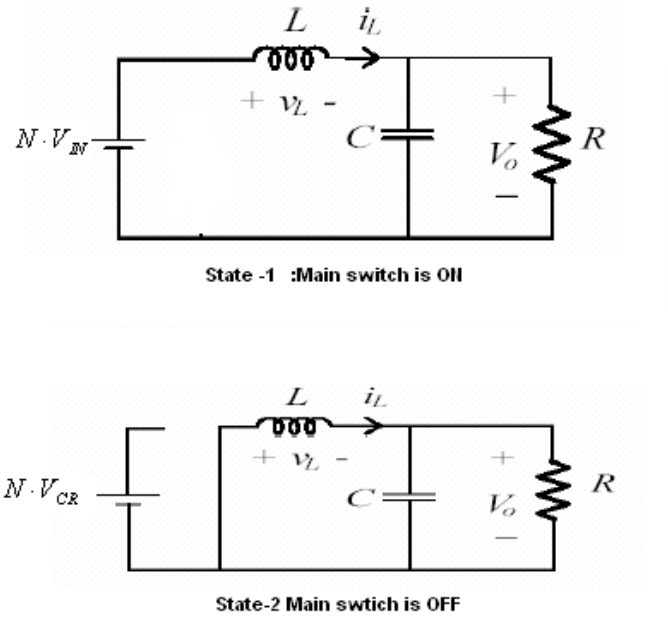



**Figure A.8: Two Circuit States in Continuous Conduction Mode**

During State-1,

$$v_L(t) = N \cdot V_{IN} - Vo \tag{A.3}$$

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{A.4}$$

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{N \cdot V_{IN} - Vo}{L} \tag{A.5}$$

$$\frac{\Delta I_L}{t_{on}} = \frac{N \cdot V_{IN} - Vo}{L} \tag{A.6}$$

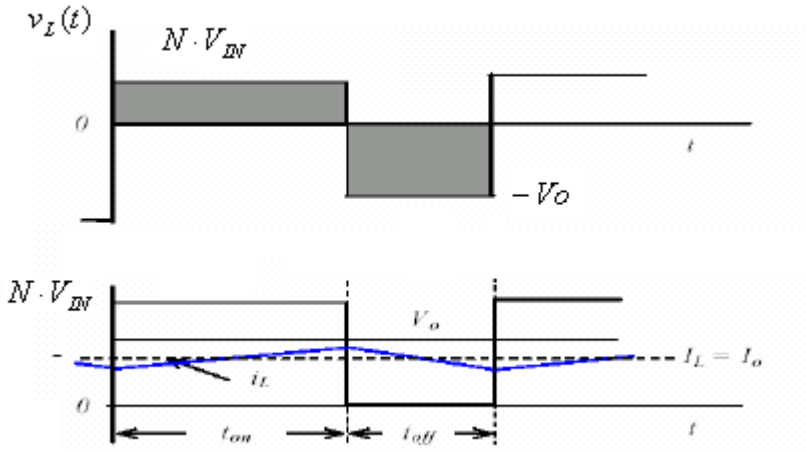



**Figure A.9: Inductor Voltage and Current Waveforms in Continuous Conduction Mode**

During State-2,

$$v_L(t) = -Vo \tag{A.7}$$

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{-Vo}{L} \tag{A.8}$$

$$\frac{\Delta I_L}{t_{off}} = \frac{-Vo}{L} \tag{A.9}$$

From figure A.10, it is seen that:

$$\Delta I_L \mid_{ton} = -\Delta I_L \mid_{toff} \tag{A.10}$$

From equations A.6 and A.9, input-output voltage relationship can be obtained:

$$\frac{N \cdot V_{IN} - Vo}{L} \cdot t_{on} = \frac{Vo}{L} \cdot t_{off} \tag{A.11}$$

$$(N \cdot V_{IN} - Vo) \cdot D = Vo \cdot (1 - D) \tag{A.12}$$

$$Vo = N \cdot D \cdot V_{IN} \qquad \text{(A.13)}$$

Form equation A.16, it is seen that, in continuous conduction mode, there is a linear relation between duty ratio and output voltage.

## A.4.2 Discontinuous Conduction Mode

When circuit operated in discontinuous conduction mode, inductor current is becomes zero in a switching cycle. For discontinuous conduction mode of operation, regarding the operation in secondary side of the converter, there are three circuit states: State-1: main switch is ON; State-2: the main switch is OFF and inductor current is non-zero: State-3: the main switch is OFF and inductor current is zero. In figure A.10, these states are given with inductor voltage and current waveforms.

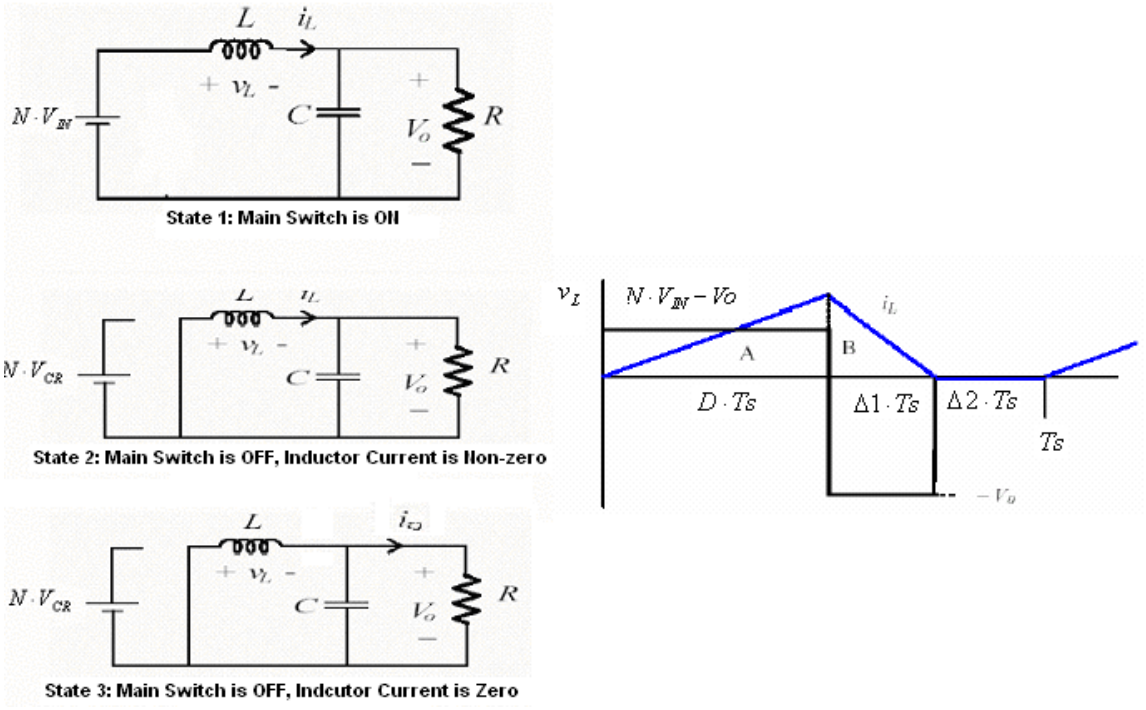



**Figure A.10: Three Circuit States and Indcutor voltage and Currnet Waveforms in Discontinuous Conduction Mode**

In steady state, the average inductor voltage for one cycle is zero. Then from figure A.10,

$$(N \cdot V_{IN} - Vo) \cdot D \cdot Ts - Vo \cdot \Delta 1 \cdot Ts = 0 \qquad \text{(A.14)}$$

From equations A.14 input-output voltage relationship is:

$$\frac{Vo}{V_{IN}} = \frac{N \cdot D}{D + \Delta 1} \qquad \text{(A.15)}$$

Peak inductor currnet can be written as:

$$i_{L\,peak} = \frac{Vo}{L} \cdot \Delta 1 \cdot Ts \qquad \text{(A.16)}$$

Since output current is the average value of the inductor current, it is written as:

$$Io = \frac{i_{L\,peak} \cdot \frac{D \cdot Ts}{2} + i_{L\,peak} \cdot \frac{\Delta 1 \cdot Ts}{2}}{Ts} = i_{L\,peak} \cdot \frac{D + \Delta 1}{2} \qquad \text{(A.17)}$$

Using Equation A.16 gives:

$$Io = \frac{Vo}{L} \cdot \Delta 1 \cdot Ts \cdot \frac{D + \Delta 1}{2} \qquad \text{(A.18)}$$

Using Equation A.15 gives:

$$Io = \frac{V_{IN} \cdot N \cdot D}{D + \Delta 1} \cdot \frac{1}{L} \cdot \Delta 1 \cdot Ts \cdot \frac{D + \Delta 1}{2} \qquad \text{(A.19)}$$

$$Io = \frac{V_{IN}}{2 \cdot L} \cdot N \cdot D \cdot \Delta 1 \cdot Ts \qquad \text{(A.20)}$$

$$\Delta 1 = \frac{2 \cdot L \cdot Io}{V_{IN} \cdot N \cdot D \cdot Ts} \qquad \text{(A.21)}$$

From equation A.15, input output relationship is

$$\frac{Vo}{V_{IN}} = \frac{N \cdot D}{D + \frac{2 \cdot L \cdot Io}{V_{IN} \cdot N \cdot D \cdot Ts}} \qquad \text{(A.22)}$$

From equation A.22, in discontinuous conduction mode, input-output relationship of the forward converter is dependent to load current and input voltage; there is not a linear relationship with duty cycle D.

# APPENDIX B

# CIRCUITS USED IN SIMULATIONS

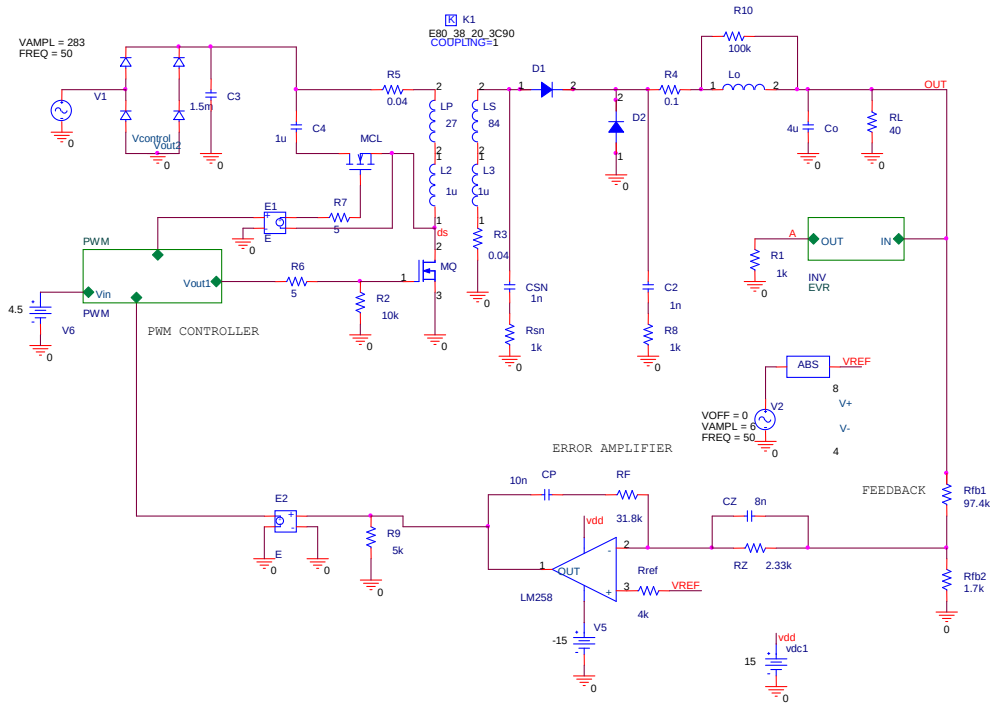



**Figure B.1: Simulation Circuit Used in Chapter 3.**

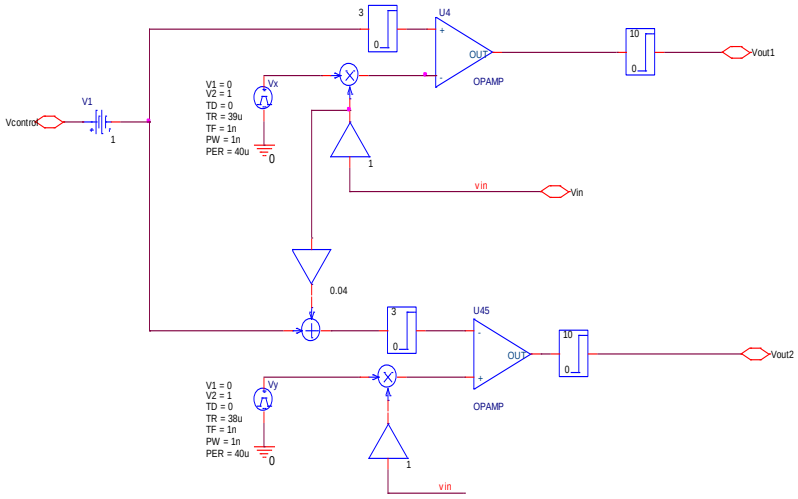



**Figure B.2: PWM Modulator Model Used in figure B.1**

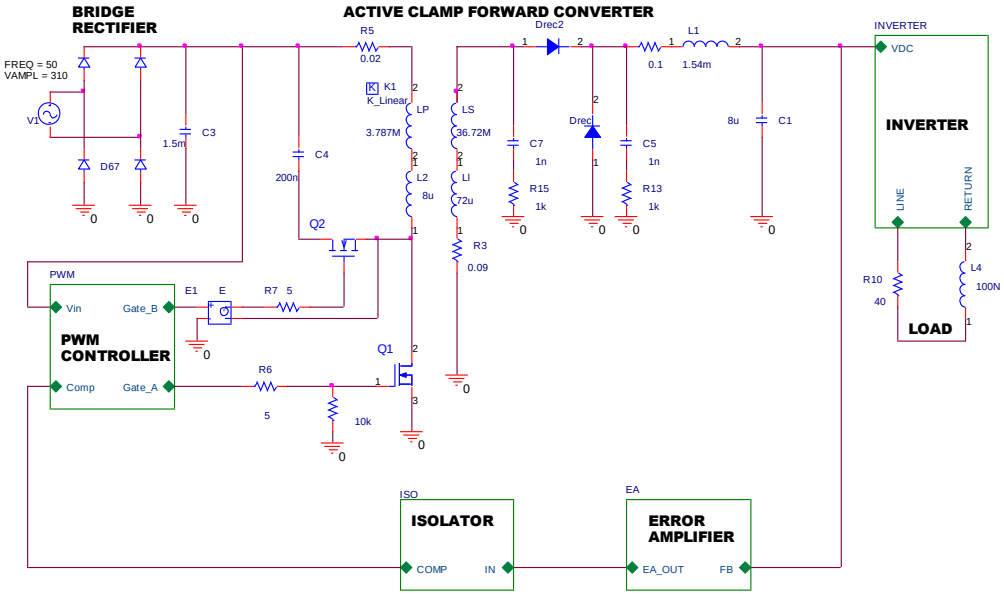



**Figure B.3: Simulation Circuit Used in Chapter 4.**

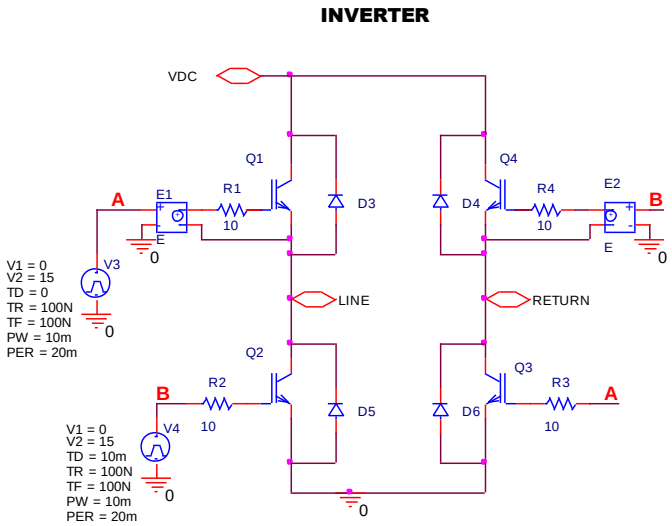



**Figure B.4: Simulation Circuit Used in Figure B.3.**

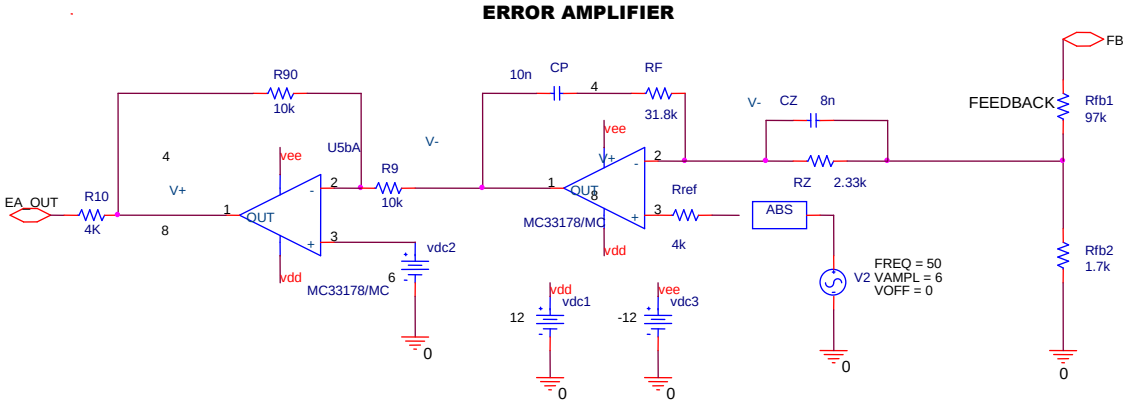



**Figure B.5: Error Amplifier Model Used in Figure B.3.**

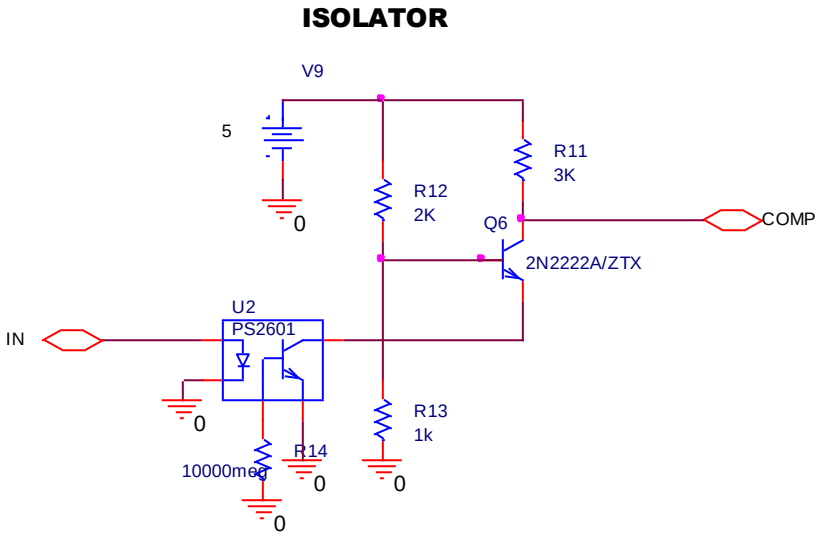



**Figure B.6: Isolator Circuit Model Used in Figure B.3.**

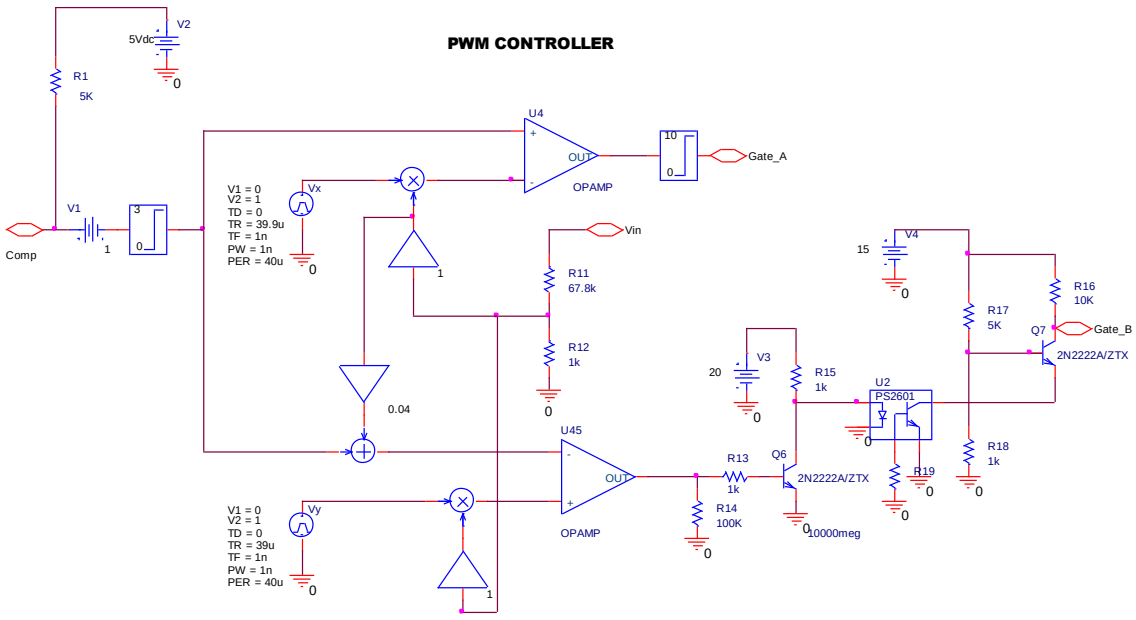



**Figure B.7: PWM Controller Model Used in Figure B.3.**

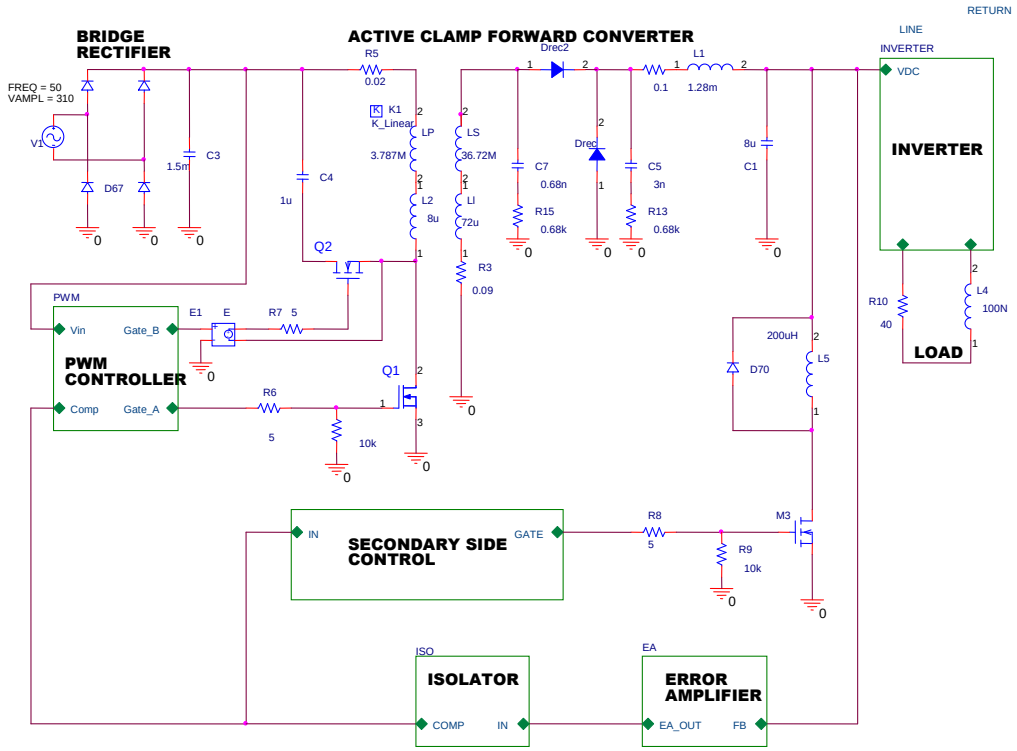



**Figure B.8: Simulation Circuit of the Modified Topology Used in Chapter 4**

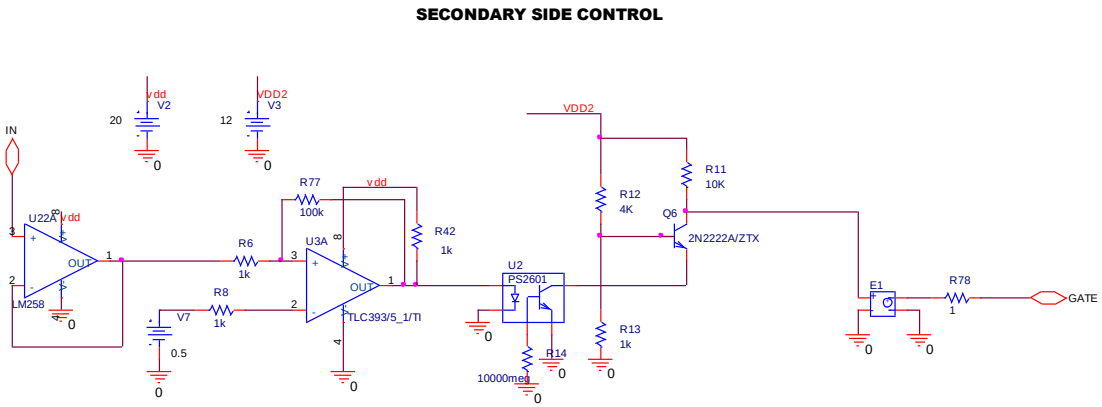



**Figure B.9: Secondary Side Control Circuit Model Used in Figure B.8**

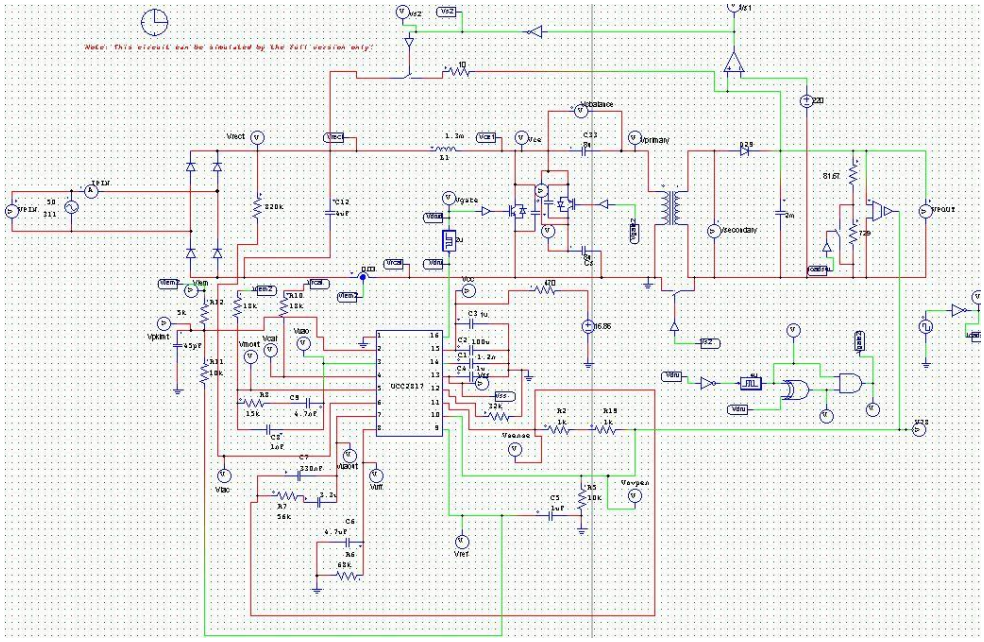


**Figure B.10: Simulation Circuit Used in Chapter 6**

# APPENDIX C

## SIMULATION SETTINGS

| Simulations Settings Used in Simulations | |
|---|---|
| Analysis Type | Transient (Time Domain) |
| Run to Time (TSTOP) | 30ms |
| Maximum Step Size | 250ns |
| Category | Analog Simulation |
| RELTOL | 0.01 |
| VNTOL | 10u |
| ABSTOL | 10p |
| CHGTOL | 0.01p |
| GMIN | 1E-10 |
| ITL1 | 150 |
| ITL2 | 200 |
| ITL4 | 500 |

# APPENDIX D

# DATASHEETS OF THE COMPONENTS

MICROCHIP

# PIC18FXX8

## 28/40-Pin High-Performance, Enhanced Flash Microcontrollers with CAN

### High-Performance RISC CPU:

- Linear program memory addressing up to 2 Mbytes
- Linear data memory addressing to 4 Kbytes
- Up to 10 MIPS operation
- DC – 40 MHz clock input
- 4 MHz-10 MHz oscillator/clock input with PLL active
- 16-bit wide instructions, 8-bit wide data path
- Priority levels for interrupts
- 8 x 8 Single-Cycle Hardware Multiplier

### Peripheral Features:

- High current sink/source 25 mA/25 mA
- Three external interrupt pins
- Timer0 module: 8-bit/16-bit timer/counter with 8-bit programmable prescaler
- Timer1 module: 16-bit timer/counter
- Timer2 module: 8-bit timer/counter with 8-bit period register (time base for PWM)
- Timer3 module: 16-bit timer/counter
- Secondary oscillator clock option – Timer1/Timer3
- Capture/Compare/PWM (CCP) modules; CCP pins can be configured as:
  - Capture input: 16-bit, max resolution 6.25 ns
  - Compare: 16-bit, max resolution 100 ns (TCY)
  - PWM output: PWM resolution is 1 to 10-bit Max. PWM freq. @:8-bit resolution = 156 kHz 10-bit resolution = 39 kHz
- Enhanced CCP module which has all the features of the standard CCP module, but also has the following features for advanced motor control:
  - 1, 2 or 4 PWM outputs
  - Selectable PWM polarity
  - Programmable PWM dead time
- Master Synchronous Serial Port (MSSP) with two modes of operation:
  - 3-wire SPI™ (Supports all 4 SPI modes)
  - $I^2C$™ Master and Slave mode
- Addressable USART module:
  - Supports interrupt-on-address bit

### Advanced Analog Features:

- 10-bit, up to 8-channel Analog-to-Digital Converter module (A/D) with:
  - Conversion available during Sleep
  - Up to 8 channels available
- Analog Comparator module:
  - Programmable input and output multiplexing
- Comparator Voltage Reference module
- Programmable Low-Voltage Detection (LVD) module:
  - Supports interrupt-on-Low-Voltage Detection
- Programmable Brown-out Reset (BOR)

### CAN bus Module Features:

- Complies with ISO CAN Conformance Test
- Message bit rates up to 1 Mbps
- Conforms to CAN 2.0B Active Spec with:
  - 29-bit Identifier Fields
  - 8-byte message length
  - 3 Transmit Message Buffers with prioritization
  - 2 Receive Message Buffers
  - 6 full, 29-bit Acceptance Filters
  - Prioritization of Acceptance Filters
  - Multiple Receive Buffers for High Priority Messages to prevent loss due to overflow
  - Advanced Error Management Features

### Special Microcontroller Features:

- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator
- Programmable code protection
- Power-saving Sleep mode
- Selectable oscillator options, including:
  - 4x Phase Lock Loop (PLL) of primary oscillator
  - Secondary Oscillator (32 kHz) clock input
- In-Circuit Serial Programming™ (ICSP™) via two pins

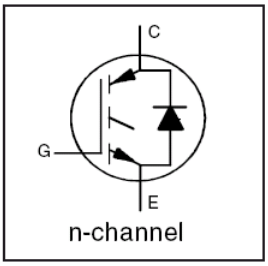
### Flash Technology:

- Low-power, high-speed Enhanced Flash technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Industrial and Extended temperature ranges

International
IOR Rectifier

# IRGB4062DPbF
# IRGP4062DPbF

***INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE***




$V_{CES}$ = 600V

$I_C$ = 24A, $T_C$ = 100°C

$t_{SC}$ ≥ 5µs, $T_{J(max)}$ = 175°C

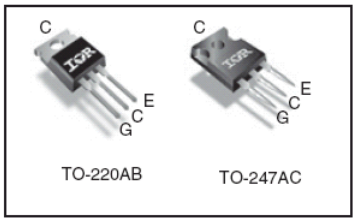
$V_{CE(on)}$ typ. = 1.65V

### Features

- Low $V_{CE\ (ON)}$ Trench IGBT Technology
- Low switching losses
- Maximum Junction temperature 175 °C
- 5 µS short circuit SOA
- Square RBSOA
- 100% of the parts tested for 4X rated current ($I_{LM}$)
- Positive $V_{CE\ (ON)}$ Temperature co-efficient
- Ultra fast soft Recovery Co-Pak Diode
- Tight parameter distribution
- Lead Free Package

### Benefits

- High Efficiency in a wide range of applications
- Suitable for a wide range of switching frequencies due to Low $V_{CE\ (ON)}$ and Low Switching losses
- Rugged transient Performance for increased reliability
- Excellent Current sharing in parallel operation
- Low EMI




| G | C | E |
|---|---|---|
| Gate | Collector | Emitter |

### Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $V_{CES}$ | Collector-to-Emitter Voltage | 600 | V |
| $I_C$ @ $T_C$ = 25°C | Continuous Collector Current | 48 | A |
| $I_C$ @ $T_C$ = 100°C | Continuous Collector Current | 24 | |
| $I_{CM}$ | Pulse Collector Current | 96 | |
| $I_{LM}$ | Clamped Inductive Load Current ① | 96 | |
| $I_F$ @ $T_C$ = 25°C | Diode Continous Forward Current | 48 | |
| $I_F$ @ $T_C$ = 100°C | Diode Continous Forward Current | 24 | |
| $I_{FM}$ | Diode Maximum Forward Current ③ | 96 | |
| $V_{GE}$ | Continuous Gate-to-Emitter Voltage | ±20 | V |
| | Transient Gate-to-Emitter Voltage | ±30 | |
| $P_D$ @ $T_C$ = 25°C | Maximum Power Dissipation | 250 | W |
| $P_D$ @ $T_C$ = 100°C | Maximum Power Dissipation | 125 | |
| $T_J$ | Operating Junction and | -55 to +175 | °C |
| $T_{STG}$ | Storage Temperature Range | | |
| | Soldering Temperature, for 10 sec. | 300 (0.063 in. (1.6mm) from case) | |
| | Mounting Torque, 6-32 or M3 Screw | 10 lbf·in (1.1 N·m) | |

### Thermal Resistance

| | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $R_{\theta JC}$ (IGBT) | Thermal Resistance Junction-to-Case-(each IGBT) TO-220AB | — | — | 0.60 | °C/W |
| $R_{\theta JC}$ (Diode) | Thermal Resistance Junction-to-Case-(each Diode) TO-220AB | — | — | 1.53 | |
| $R_{\theta JC}$ (IGBT) | Thermal Resistance Junction-to-Case-(each IGBT) TO-247AC | — | — | 0.65 | |
| $R_{\theta JC}$ (Diode) | Thermal Resistance Junction-to-Case-(each Diode) TO-247AC | — | — | 1.62 | |
| $R_{\theta CS}$ | Thermal Resistance, Case-to-Sink (flat, greased surface) | — | 0.50 | — | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (typical socket mount) | — | 80 | — | |

**Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)**

| | Parameter | Min. | Typ. | Max. | Units | Conditions | Ref.Fig |
|---|---|---|---|---|---|---|---|
| $V_{(BR)CES}$ | Collector-to-Emitter Breakdown Voltage | 600 | — | — | V | $V_{GE}$ = 0V, $I_C$ = 100µA ④ | CT6 |
| $\Delta V_{(BR)CES}/\Delta T_J$ | Temperature Coeff. of Breakdown Voltage | — | 0.30 | — | V/°C | $V_{GE}$ = 0V, $I_C$ = 1mA (25°C-175°C) | CT6 |
| $V_{CE(on)}$ | Collector-to-Emitter Saturation Voltage | — | 1.60 | 1.95 | V | $I_C$ = 24A, $V_{GE}$ = 15V, $T_J$ = 25°C | 5,6,7 |
| | | — | 2.03 | — | | $I_C$ = 24A, $V_{GE}$ = 15V, $T_J$ = 150°C | 9,10,11 |
| | | — | 2.04 | — | | $I_C$ = 24A, $V_{GE}$ = 15V, $T_J$ = 175°C | |
| $V_{GE(th)}$ | Gate Threshold Voltage | 4.0 | — | 6.5 | V | $V_{CE}$ = $V_{GE}$, $I_C$ = 700µA | 9, 10, |
| $\Delta V_{GE(th)}/\Delta TJ$ | Threshold Voltage temp. coefficient | — | -18 | — | mV/°C | $V_{CE}$ = $V_{GE}$, $I_C$ = 1.0mA (25°C - 175°C) | 11, 12 |
| gfe | Forward Transconductance | — | 17 | — | S | $V_{CE}$ = 50V, $I_C$ = 24A, PW = 80µs | |
| $I_{CES}$ | Collector-to-Emitter Leakage Current | — | 2.0 | 25 | µA | $V_{GE}$ = 0V, $V_{CE}$ = 600V | |
| | | — | 775 | — | | $V_{GE}$ = 0V, $V_{CE}$ = 600V, $T_J$ = 175°C | |
| $V_{FM}$ | Diode Forward Voltage Drop | — | 1.80 | 2.6 | V | $I_F$ = 24A | 8 |
| | | — | 1.28 | — | | $I_F$ = 24A, $T_J$ = 175°C | |
| $I_{GES}$ | Gate-to-Emitter Leakage Current | — | — | ±100 | nA | $V_{GE}$ = ±20V | |

**Switching Characteristics @ $T_J$ = 25°C (unless otherwise specified)**

| | Parameter | Min. | Typ. | Max. | Units | Conditions | Ref.Fig |
|---|---|---|---|---|---|---|---|
| $Q_g$ | Total Gate Charge (turn-on) | — | 50 | 75 | nC | $I_C$ = 24A | 24 |
| $Q_{ge}$ | Gate-to-Emitter Charge (turn-on) | — | 13 | 20 | | $V_{GE}$ = 15V | CT1 |
| $Q_{gc}$ | Gate-to-Collector Charge (turn-on) | — | 21 | 31 | | $V_{CC}$ = 400V | |
| $E_{on}$ | Turn-On Switching Loss | — | 115 | 201 | µJ | $I_C$ = 24A, $V_{CC}$ = 400V, $V_{GE}$ = 15V | CT4 |
| $E_{off}$ | Turn-Off Switching Loss | — | 600 | 700 | | $R_G$ = 10Ω, L = 200µH, $L_S$ = 150nH, $T_J$ = 25°C | |
| $E_{total}$ | Total Switching Loss | — | 715 | 901 | | Energy losses include tail & diode reverse recovery | |
| $t_{d(on)}$ | Turn-On delay time | — | 41 | 53 | ns | $I_C$ = 24A, $V_{CC}$ = 400V, $V_{GE}$ = 15V | CT4 |
| $t_r$ | Rise time | — | 22 | 31 | | $R_G$ = 10Ω, L = 200µH, $L_S$ = 150nH, $T_J$ = 25°C | |
| $t_{d(off)}$ | Turn-Off delay time | — | 104 | 115 | | | |
| $t_f$ | Fall time | — | 29 | 41 | | | |
| $E_{on}$ | Turn-On Switching Loss | — | 420 | — | µJ | $I_C$ = 24A, $V_{CC}$ = 400V, $V_{GE}$=15V | 13, 15 |
| $E_{off}$ | Turn-Off Switching Loss | — | 840 | — | | $R_G$=10Ω, L=100µH, $L_S$=150nH, $T_J$ = 175°C ④ | CT4 |
| $E_{total}$ | Total Switching Loss | — | 1260 | — | | Energy losses include tail & diode reverse recovery | WF1, WF2 |
| $t_{d(on)}$ | Turn-On delay time | — | 40 | — | ns | $I_C$ = 24A, $V_{CC}$ = 400V, $V_{GE}$ = 15V | 14, 16 |
| $t_r$ | Rise time | — | 24 | — | | $R_G$ = 10Ω, L = 200µH, $L_S$ = 150nH | CT4 |
| $t_{d(off)}$ | Turn-Off delay time | — | 125 | — | | $T_J$ = 175°C | WF1 |
| $t_f$ | Fall time | — | 39 | — | | | WF2 |
| $C_{ies}$ | Input Capacitance | — | 1490 | — | pF | $V_{GE}$ = 0V | 23 |
| $C_{oes}$ | Output Capacitance | — | 129 | — | | $V_{CC}$ = 30V | |
| $C_{res}$ | Reverse Transfer Capacitance | — | 45 | — | | f = 1.0Mhz | |
| RBSOA | Reverse Bias Safe Operating Area | FULL SQUARE | | | | $T_J$ = 175°C, $I_C$ = 96A<br>$V_{CC}$ = 480V, Vp =600V<br>Rg = 10Ω, $V_{GE}$ = +15V to 0V | 4<br>CT2 |
| SCSOA | Short Circuit Safe Operating Area | 5 | — | — | µs | $V_{CC}$ = 400V, Vp =600V<br>Rg = 10Ω, $V_{GE}$ = +15V to 0V | 22, CT3<br>WF4 |
| Erec | Reverse Recovery Energy of the Diode | — | 621 | — | µJ | $T_J$ = 175°C | 17, 18, 19 |
| $t_{rr}$ | Diode Reverse Recovery Time | — | 89 | — | ns | $V_{CC}$ = 400V, $I_F$ = 24A | 20, 21 |
| $I_{rr}$ | Peak Reverse Recovery Current | — | 37 | — | A | $V_{GE}$ = 15V, Rg = 10Ω, L =200µH, $L_s$ = 150nH | WF3 |

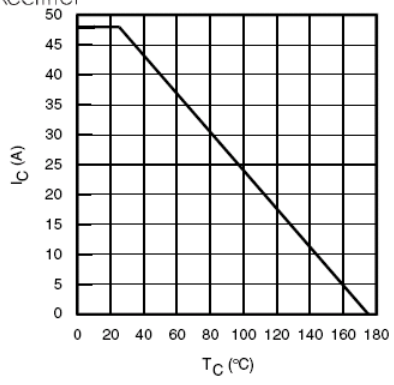



**Fig. 1** - Maximum DC Collector Current vs. Case Temperature

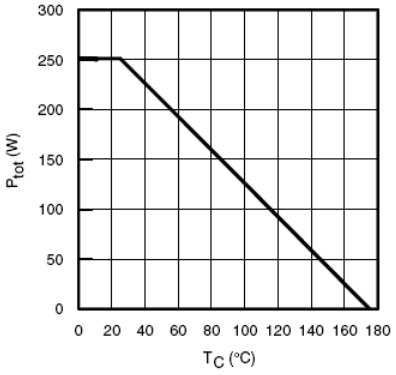



**Fig. 2** - Power Dissipation vs. Case Temperature

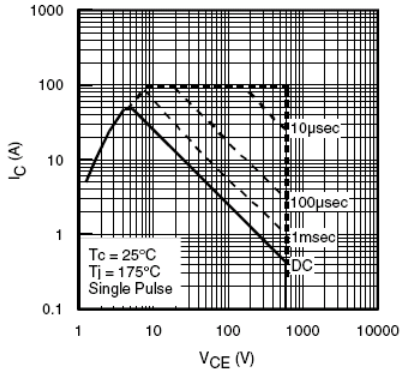



**Fig. 3** - Forward SOA
$T_C$ = 25°C, $T_J \leq$ 175°C; $V_{GE}$ =15V

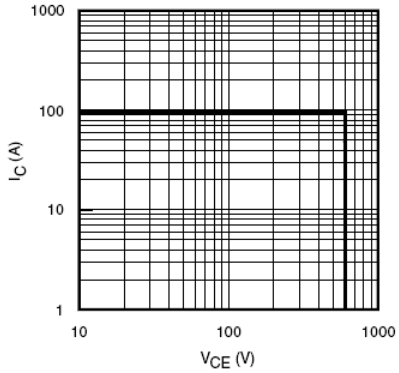



**Fig. 4** - Reverse Bias SOA
$T_J$ = 175°C; $V_{GE}$ =15V

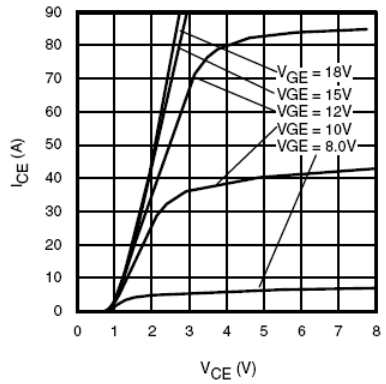



**Fig. 5** - Typ. IGBT Output Characteristics
$T_J$ = -40°C; tp = 80µs

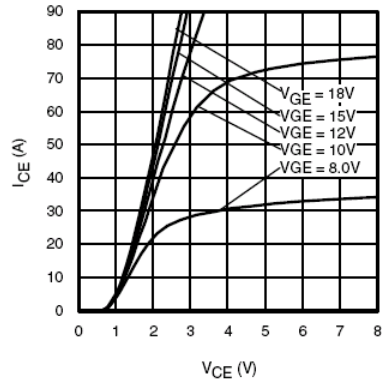
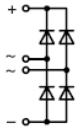


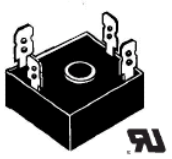

**Fig. 6** - Typ. IGBT Output Characteristics
$T_J$ = 25°C; tp = 80µs

# Single Phase Rectifier Bridge

$I_{dAVM}$ = 30 A
$V_{RRM}$ = 1200-1800 V

| $V_{RSM}$ V | $V_{RRM}$ V | Type |
|---|---|---|
| 1200 | 1200 | VBO 36-12NO8 |
| 1400 | 1400 | VBO 36-14NO8 |
| 1600 | 1600 | VBO 36-16NO8 |
| 1800 | 1800 | VBO 36-18NO8 |





| Symbol | Conditions | | Maximum Ratings | |
|---|---|---|---|---|
| $I_{dAV}$ | $T_C$ = 85°C, module | | 23 | A |
| $I_{dAVM}$ | $T_C$ = 62°C, module | | 30 | A |
| $I_{FSM}$ | $T_{VJ}$ = 45°C; | t = 10 ms (50 Hz), sine | 550 | A |
| | $V_R$ = 0 | t = 8.3 ms (60 Hz), sine | 600 | A |
| | $T_{VJ}$ = $T_{VJM}$ | t = 10 ms (50 Hz), sine | 500 | A |
| | $V_R$ = 0 | t = 8.3 ms (60 Hz), sine | 550 | A |
| $I^2t$ | $T_{VJ}$ = 45°C | t = 10 ms (50 Hz), sine | 1520 | $A^2s$ |
| | $V_R$ = 0 | t = 8.3 ms (60 Hz), sine | 1520 | $A^2s$ |
| | $T_{VJ}$ = $T_{VJM}$ | t = 10 ms (50 Hz), sine | 1250 | $A^2s$ |
| | $V_R$ = 0 | t = 8.3 ms (60 Hz), sine | 1250 | $A^2s$ |
| $T_{VJ}$ | | | -40...+150 | °C |
| $T_{VJM}$ | | | 150 | °C |
| $T_{stg}$ | | | -40...+150 | °C |
| $V_{ISOL}$ | 50/60 Hz, RMS | t = 1 min | 2500 | V~ |
| | $I_{ISOL} \leq$ 1 mA | t = 1 s | 3000 | V~ |
| $M_d$ | Mounting torque | (M5) | 2 ±10% | Nm |
| | | (10-32 UNF) | 18 ±10% | lb.in. |
| Weight | typ. | | 22 | g |

| Symbol | Conditions | | Characteristic Values | |
|---|---|---|---|---|
| $I_R$ | $T_{VJ}$ = 25°C; | $V_R$ = $V_{RRM}$ | ≤ 0.3 | mA |
| | $T_{VJ}$ = $T_{VJM}$; | $V_R$ = $V_{RRM}$ | ≤ 2.0 | mA |
| $V_F$ | $I_F$ = 150 A; | $T_{VJ}$ = 25°C | ≤ 1.7 | V |
| $V_{T0}$ | For power-loss calculations only | | 0.8 | V |
| $r_T$ | | | 5.8 | mΩ |
| $R_{thJC}$ | per diode; DC current | | 6.2 | K/W |
| | per module | | 1.55 | K/W |
| $R_{thJK}$ | per diode; DC current | | 7.4 | K/W |
| | per module | | 1.85 | K/W |
| $d_S$ | Creeping distance on surface | | 12.7 | mm |
| $d_A$ | Creepage distance in air | | 9.4 | mm |
| a | Max. allowable acceleration | | 50 | $m/s^2$ |

Data according to IEC 60747 and refer to a single diode unless otherwise stated.

IXYS reserves the right to change limits, test conditions and dimensions.

### Features

- Package with ¼" fast-on terminals
- Isolation voltage 3000 V~
- Planar passivated chips
- Blocking voltage up to 1800 V
- Low forward voltage drop
- UL registered E 72873

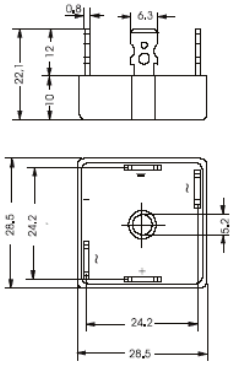
### Applications

- Supplies for DC power equipment
- Input rectifiers for PWM inverter
- Battery DC power supplies
- Field supply for DC motors

### Advantages

- Easy to mount with one screw
- Space and weight savings
- Improved temperature and power cycling

### Dimensions in mm (1 mm = 0.0394")




327

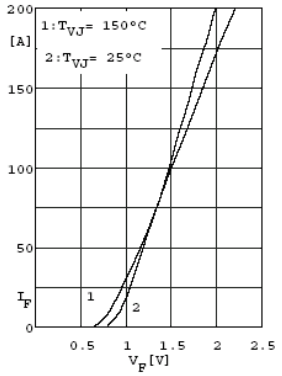



Fig. 1 Forward current versus voltage drop per diode

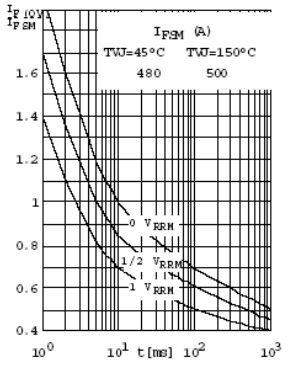



Fig. 2 Surge overload current per diode
$I_{FSM}$: Crest value. t: duration

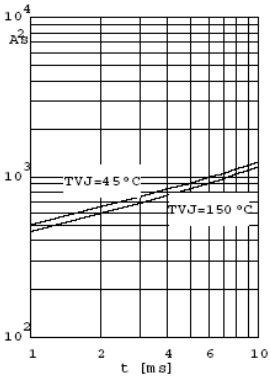



Fig. 3 $\int i^2dt$ versus time (1-10ms) per diode or thyristor

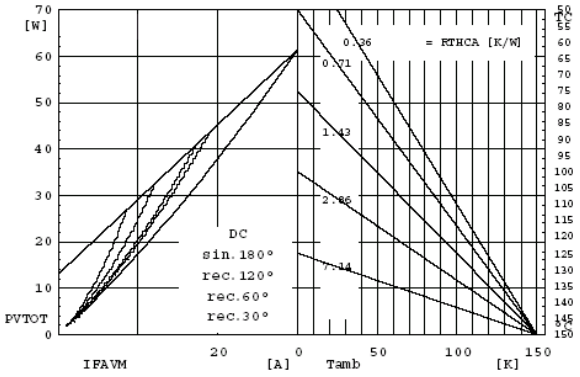



Fig. 4 Power dissipation versus direct output current and ambient temperature

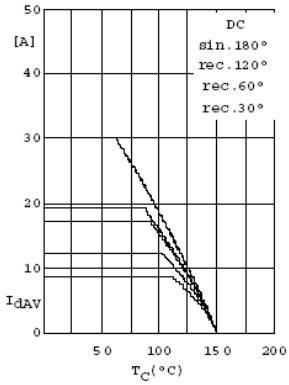



Fig.5 Maximum forward current at case temperature

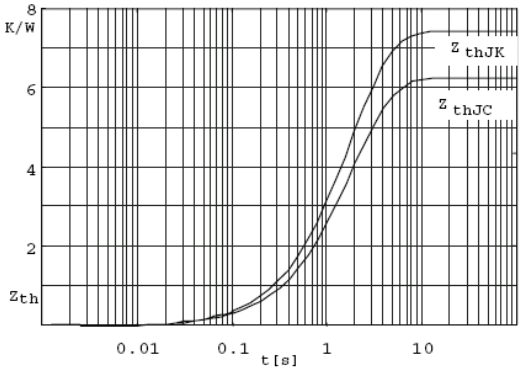


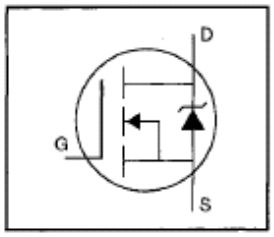

Fig. 6 Transient thermal impedance per diode or thyristor, calculated

# International IOR Rectifier

# IRFPC40

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements




$V_{DSS}$ = 600V

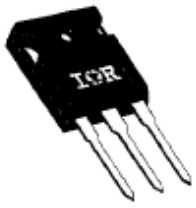
$R_{DS(on)}$ = 1.2Ω

$I_D$ = 6.8A

## Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial–industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.




TO-247AC

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10 V | 6.8 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10 V | 4.3 | |
| $I_{DM}$ | Pulsed Drain Current ① | 27 | |
| $P_D$ @ $T_C$ = 25°C | Power Dissipation | 150 | W |
| | Linear Derating Factor | 1.2 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 410 | mJ |
| $I_{AR}$ | Avalanche Current ① | 6.8 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 15 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 3.0 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to +150 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| | Mounting Torque, 6-32 or M3 screw | 10 lbf•in (1.1 N•m) | |

## Thermal Resistance

| | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | — | — | 0.83 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface | — | 0.24 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | — | 40 | |

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 600 | — | — | V | $V_{GS}$=0V, $I_D$= 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.70 | — | V/°C | Reference to 25°C, $I_D$= 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 1.2 | Ω | $V_{GS}$=10V, $I_D$=4.1A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$=$V_{GS}$, $I_D$= 250µA |
| $g_{fs}$ | Forward Transconductance | 4.9 | — | — | S | $V_{DS}$=100V, $I_D$=4.1A ④ |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 100 | µA | $V_{DS}$=600V, $V_{GS}$=0V |
| | | — | — | 500 | | $V_{DS}$=480V, $V_{GS}$=0V, $T_J$=125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$=20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$=-20V |
| $Q_g$ | Total Gate Charge | — | — | 60 | nC | $I_D$=6.2A |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 8.3 | | $V_{DS}$=360V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | — | 30 | | $V_{GS}$=10V See Fig. 6 and 13 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 13 | — | ns | $V_{DD}$=300V |
| $t_r$ | Rise Time | — | 18 | — | | $I_D$=6.2A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 55 | — | | $R_G$=9.1Ω |
| $t_f$ | Fall Time | — | 20 | — | | $R_D$=47Ω See Figure 10 ④ |
| $L_D$ | Internal Drain Inductance | — | 5.0 | — | nH | Between lead, 6 mm (0.25in.) from package and center of die contact |
| $L_S$ | Internal Source Inductance | — | 13 | — | | |
| $C_{iss}$ | Input Capacitance | — | 1300 | — | pF | $V_{GS}$=0V |
| $C_{oss}$ | Output Capacitance | — | 160 | — | | $V_{DS}$=25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 30 | — | | $f$=1.0MHz See Figure 5 |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 6.8 | A | MOSFET symbol showing the |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | — | — | 27 | | integral reverse p-n junction diode. |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.5 | V | $T_J$=25°C, $I_S$=6.8A, $V_{GS}$=0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | 450 | 940 | ns | $T_J$=25°C, $I_F$=6.2A |
| $Q_{rr}$ | Reverse Recovery Charge | — | 3.8 | 7.9 | µC | di/dt=100A/µs ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is neglegible (turn-on is dominated by $L_S$+$L_D$) | | | | |

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② $V_{DD}$=50V, starting $T_J$=25°C, L=16mH $R_G$=25Ω, $I_{AS}$=6.8A (See Figure 12)

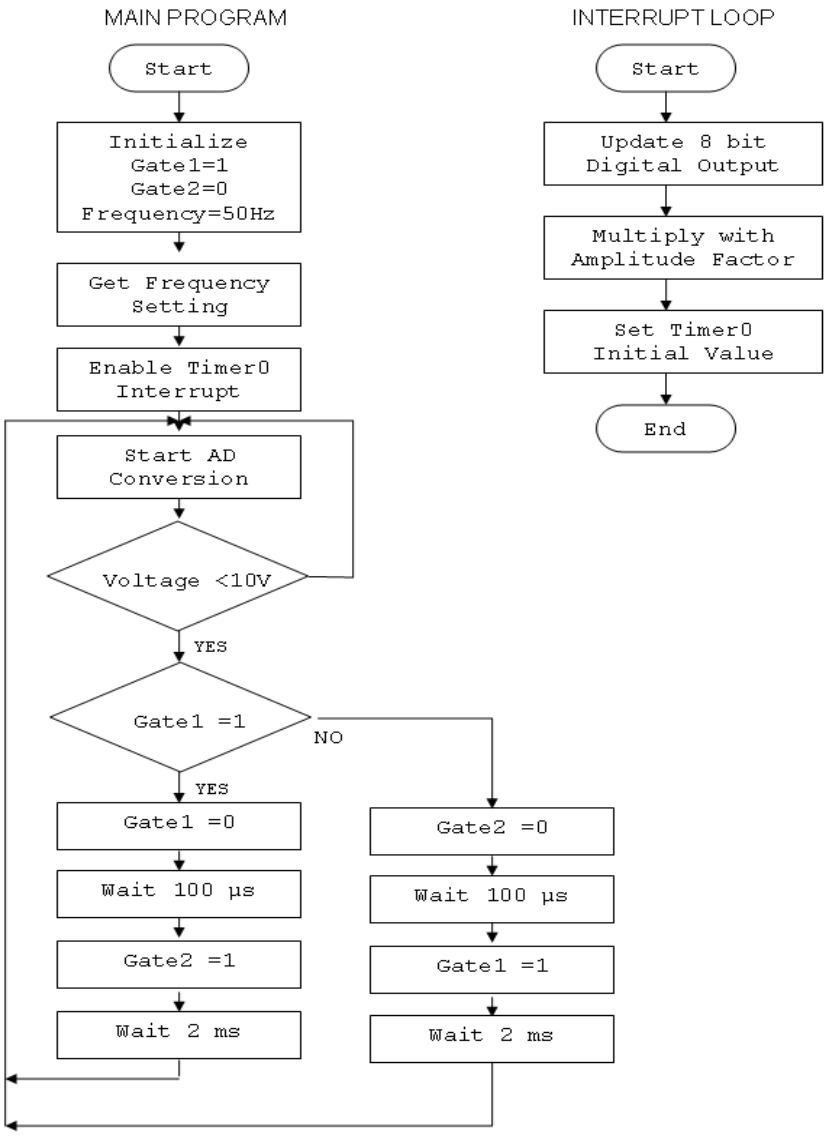
③ $I_{SD}$≤6.8A, di/dt≤80A/µs, $V_{DD}$≤$V_{(BR)DSS}$, $T_J$≤150°C

④ Pulse width ≤ 300 µs; duty cycle ≤2%.

# APPENDIX E

# FLOWCHART AND SOURCE CODE OF THE SOFTWARE

## E.1 FLOWCHART



## E.2 SOURCE CODE

```
#include <p18f458.h>
#include <timers.h>
#include <delays.h>

void timer_isr (void);

static char i;
static char t = 0;
unsigned int        voltage_ad;


static int
vref[100]={8,16,24,32,40,48,56,63,71,79,86,94,101,109,116,123,130,137,143,150,156,163,169,175,180,1
86,

191,196,201,206,211,215,219,223,227,231,234,237,240,243,245,247,249,250,252,253,254,254,255,255,

255,254,254,253,252,250,249,247,245,243,240,237,234,231,227,223,219,215,211,206,201,196,191,186,

180,175,169,163,156,150,143,137,130,123,116,109,101,94,86,79,71,63,56,48,40,32,24,16,8,0};


static unsigned char frq[7]={185,224,238,243,248,251,253};
static char amp[7]={1,2,3,4,5,5,5};


void SMPS_Startup(void)
{
        if(PORTCbits.RC0==0 && t==75)
                PORTCbits.RC1=0;
        if(PORTCbits.RC0)
                PORTCbits.RC1=1;
}

void adconversion(void)
{
        Delay10TCYx(4);                                                                 //Delay
of 40 micros to power up ADC module
        ADCON0bits.GO_DONE = 1;                         //Start the A/D conversion
        while(ADCON0bits.GO_DONE);              //Wait until A/D conversion is over

        voltage_ad = ADRESH*256 + ADRESL;       //Save 10 bit result in voltage_ad
        //voltage_ad = voltage_ad & 1008 ;      //Discard the left 4 bits   ?????


        if(i==6)
                if(voltage_ad<0x002E )                  //  1E=30.(30/1024)*350 = 10V.
                {
                        if(!PORTCbits.RC2)
                        {
```

```
                    PORTCbits.RC3=0;
                    Delay10TCYx(7);
                    PORTCbits.RC2=1;
                }
                else
                {
                    PORTCbits.RC2=0;
                    Delay10TCYx(7);
                    PORTCbits.RC3=1;
                }
                Delay10TCYx(450);
                //Delay of micros. long time delay to prevent adjacent gate signals
    }

if(i==5)
        if(voltage_ad<0x001E )
        {
                if(!PORTCbits.RC2)
                {
                    PORTCbits.RC3=0;
                    Delay10TCYx(25);
                    PORTCbits.RC2=1;
                }
                else
                {
                    PORTCbits.RC2=0;
                    Delay10TCYx(25);
                    PORTCbits.RC3=1;
                }
                Delay10TCYx(700);


    }

if(i==4)
        if(voltage_ad<0x001E )
        {
                    if(!PORTCbits.RC2)
                {
                    PORTCbits.RC3=0;
                    Delay10TCYx(40);
                    PORTCbits.RC2=1;
                }
                else
                {
                    PORTCbits.RC2=0;
                    Delay10TCYx(40);
                    PORTCbits.RC3=1;
                }
                Delay10TCYx(1200);

    }

if(i==3)
```

```
        if(voltage_ad<0x0017 )
        {
                        if(!PORTCbits.RC2)
                {
                        PORTCbits.RC3=0;
                        Delay10TCYx(40);
                        PORTCbits.RC2=1;
                }
                else
                {
                        PORTCbits.RC2=0;
                        Delay10TCYx(40);
                        PORTCbits.RC3=1;
                }
                Delay10TCYx(1700);



   }
if(i==2)
        if(voltage_ad<0x0017 )
        {
                if(!PORTCbits.RC2)
                {
                        PORTCbits.RC3=0;
                        Delay10TCYx(50);
                        PORTCbits.RC2=1;
                }
                else
                {
                        PORTCbits.RC2=0;
                        Delay10TCYx(40);
                        PORTCbits.RC3=1;
                }
                Delay10TCYx(2000);

   }

 if(i==1)
        if(voltage_ad<0x0005 )
        {
                if(!PORTCbits.RC2)
                {
                        PORTCbits.RC3=0;
                        Delay10TCYx(40);
                        PORTCbits.RC2=1;
                }
                else
                {
                        PORTCbits.RC2=0;
                        Delay10TCYx(40);
                        PORTCbits.RC3=1;
                }
                Delay10TCYx(3000);
```

```
            }
          if(i==0)
                    if(voltage_ad<0x000A )
                    {
                              if(!PORTCbits.RC2)
                        {
                              PORTCbits.RC3=0;
                              Delay10TCYx(40);
                              PORTCbits.RC2=1;
                        }
                        else
                        {
                              PORTCbits.RC2=0;
                              Delay10TCYx(40);
                              PORTCbits.RC3=1;
                        }
                        Delay10TCYx(3500);


            }

 }

#pragma code low_vector=0x18
void low_interrupt (void)
{
   _asm GOTO timer_isr _endasm
}

#pragma code

#pragma interruptlow timer_isr
#pragma config WDT = OFF

void
timer_isr (void)
{
   INTCONbits.TMR0IF = 0;
          PORTD = vref[t++]*amp[i]/5;
          if(t==100)
                    t=0;
          TMR0L=frq[i];
          if(i==8)
                    PORTD=160;
 }

void
main (void)
{
 char input=4;//default 50 Hz
 char k=0;
```

```
 TRISA=0b00000001;//RAO input.
 TRISD = 0;
 TRISC = 0x01;
 TRISB = 0xFF;
 CMCON = 0x07;
 PORTD = 0xFF;

 PORTCbits.RC1=1;   // SMPS INHIBITED

 PORTCbits.RC2=0;
 PORTCbits.RC3=1;

          //ADC registers
 ADCON1 = 0b11001110;                                          //Right
justified,Fosc/64,ANO Analog
 ADCON0 = 0b10000001;                                          //Select ANO, power up
ADC

OpenTimer0( TIMER_INT_ON & T0_8BIT & T0_SOURCE_INT & T0_PS_1_64 );


 INTCONbits.GIE = 1;  // enable all interrupts

 while (1)
  {
            adconversion();
                  SMPS_Startup();

                                    if(!PORTBbits.RB0)
                                    {
                                              input=8;
                                              k=0;
                                              //while(!PORTBbits.RB0);
                                    }

                        if(!PORTBbits.RB1)
                                    {
                                              input=0;
                                              k=0;
                                              //while(!PORTBbits.RB1);
                                    }

                                    if(!PORTBbits.RB2)
                                    {
                                              input=1;
                                              k=0;
                                              //while(!PORTBbits.RB2);
                                    }

                                    if(!PORTBbits.RB3)
                                    {
                                              input=2;
                                              k=0;
                                    //        while(!PORTBbits.RB3);
```

```
                                        }

                        if(!PORTBbits.RB4)
                                        {
                                                input=3;
                                                k=0;
                                                //while(!PORTBbits.RB4);
                                        }

                                        if(!PORTBbits.RB5)
                                        {
                                                input=4;
                                                k=0;
                                                //while(!PORTBbits.RB5);
                                        }

                                        if(!PORTBbits.RB6)
                                        {
                                                input=5;
                                                k=0;
                                                //while(!PORTBbits.RB6);
                                        }

                                        if(!PORTBbits.RB7)
                                        {
                                                input=6;
                                                k=0;
                                                //while(!PORTBbits.RB7);
                                        }

                i=input;
                }


}
```

# APPENDIX F

# PHOTOS OF THE EXPERIMENT SETUP

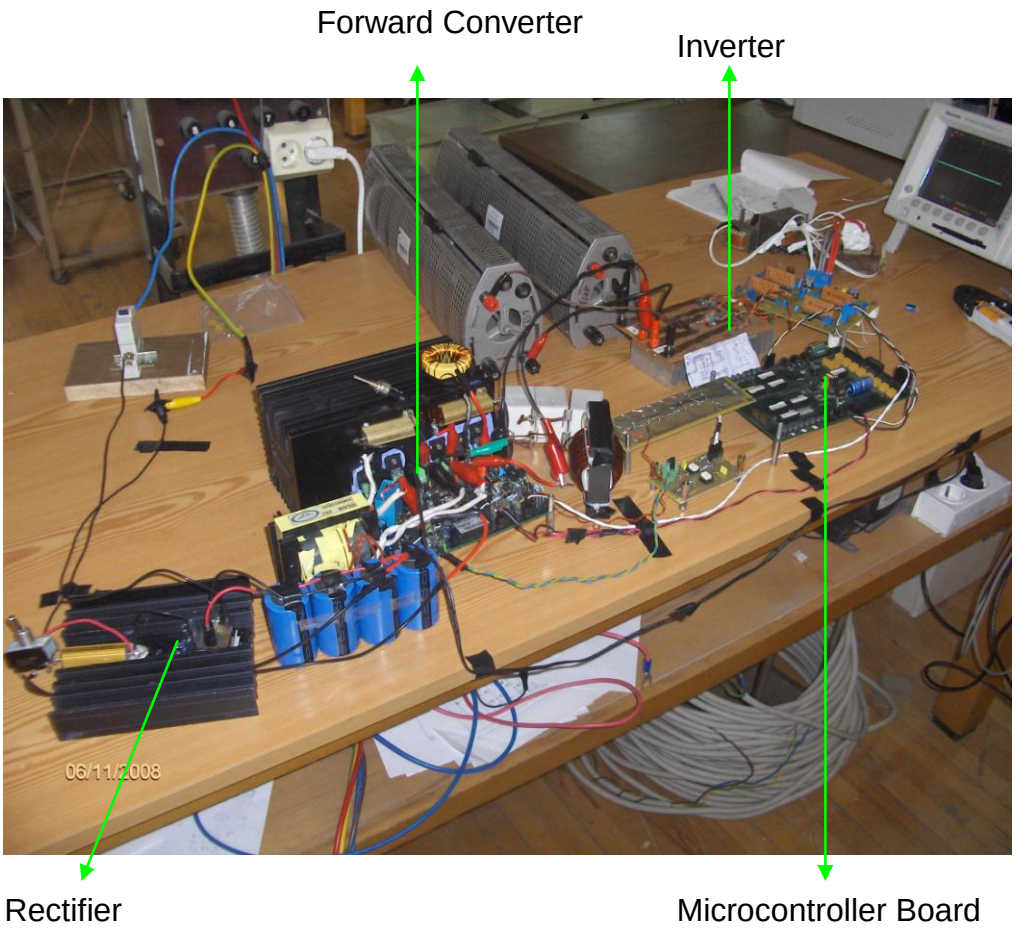



**Figure F.1: General View from the Set-Up**

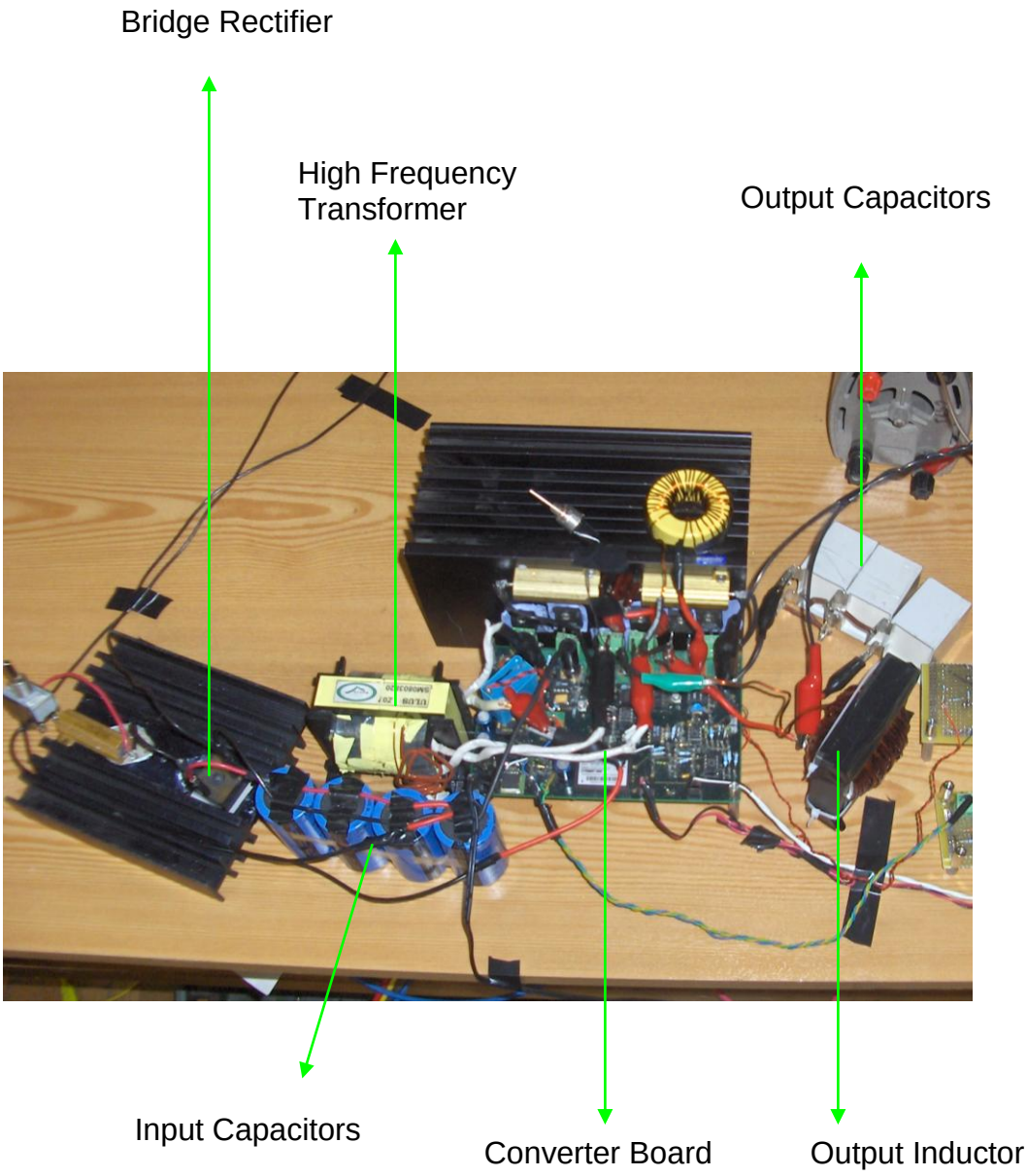



**Figure F.2: Converter Stage**

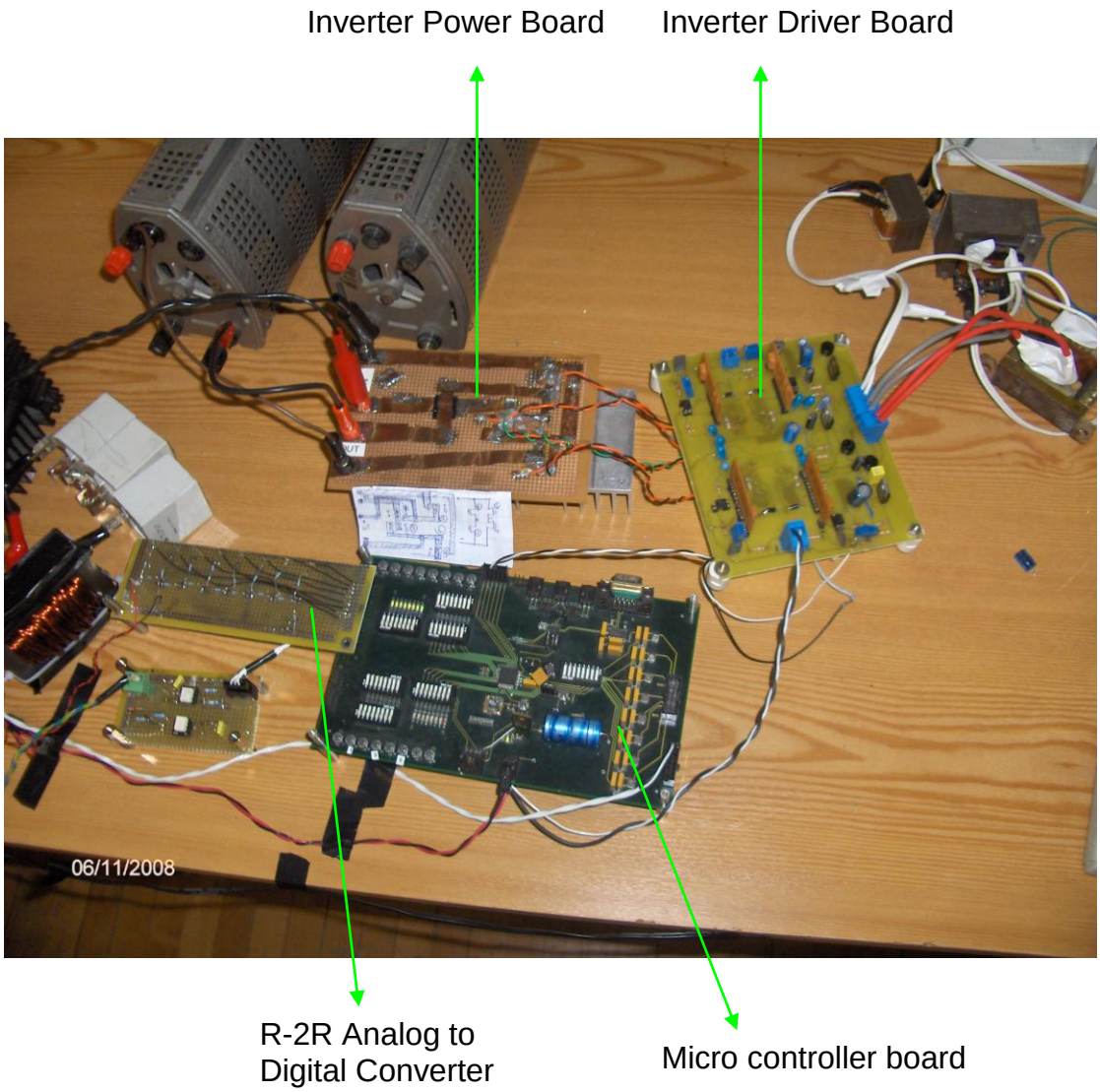



**Figure F.3: Inverter and Microcontroller Stages**