NOVEL IMPEDANCE TUNER, PHASE SHIFTER, AND VECTOR MODULATORS USING RF MEMS TECHNOLOGY

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

MEHMET ÜNLÜ

IN PARTIAL FULFILMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF DOCTOR OF PHILOSOPHY
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

MARCH 2009

Approval of the thesis:

NOVEL IMPEDANCE TUNER, PHASE SHIFTER, AND VECTOR MODULATORS USING RF MEMS TECHNOLOGY

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ABSTRACT

NOVEL IMPEDANCE TUNER, PHASE SHIFTER, AND VECTOR MODULATORS USING RF MEMS TECHNOLOGY

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March 2009, 268 pages

This thesis presents the theory, design, fabrication, and measurement results of novel reconfigurable impedance tuner, phase shifter, and vector modulators using the RF MEMS technology. The presented circuits are based on triple stub topology, and it is shown both theoretically and experimentally in this thesis that it is possible to control the insertion phase and amplitude of the input signal simultaneously using this topology. The presented circuits are implemented using an in-house, surface micromachining fabrication process developed at METU, namely METU RF MEMS Fabrication Process, which is implemented using six masks on quartz substrates. The RF MEMS impedance tuner is designed to operate in 6-20 GHz frequency band, and it covers the Smith Chart with 1331 impedance points. The measurement results of 729 impedance points of the fabricated impedance tuner show that a wide Smith Chart coverage is obtained in the entire band.

The RF MEMS phase shifter is designed to cover 0-360° range 10° steps at 15 GHz center frequency. The measurement results of the fabricated phase shifter show that the average phase error is 1.7°, the average insertion loss is -3.1 dB, and the average return loss is -19.3 dB for the measured 21 phase states. The phase shifter can also work up to 30 GHz and 40 GHz with average insertion losses of -5 dB and -8 dB, respectively. The designed RF MEMS vector modulator operates in 22.5-27.5 GHz band, and it has 3 amplitude and 8 phase states. The measurement results of the fabricated vector modulator show that the amplitude error is 0.5 dB, the phase error is 4°, and the return loss is -15 dB on average among the 24 measured states at each of 22.5, 25, and 27.5 GHz frequencies.

The results presented in this thesis show once more that the METU RF MEMS Fabrication Process is mature and successful on implementing complicated RF MEMS structures.

Keywords: RF MEMS, reconfigurable impedance tuner, phase shifter, vector modulator, MEMS switch.

ÖZ

RF MEMS TEKNOLOJİSİ İLE YENİ EMPEDANS AYARLAYICI, FAZ KAYDIRICI VE VEKTÖR KİPLEYİCİLER

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Mart 2009, 268 sayfa

Bu tezde, RF MEMS teknolojisi kullanılarak gerçekleştirilen yeni ayarlanabilir empedans ayarlayıcı, faz kaydırıcı ve vektör kipleyicilerin teorisi, tasarımı, üretimi ve ölçüm sonuçları sunulmaktadır. Sunulan devreler üç saplamali bir topoloji kullanılarak tasarlanmış, ayrıca bu topoloji ile gelen işaretin genliğinin ve fazının aynı anda değiştirilebildiği bu tez kapsamında kuramsal ve deneysel olarak gösterilmiştir. Sunulan devrelerin tamamı, ODTÜ'de geliştirilen, altı maske ile kuvars taban üzerinde gerçekleştirilen ve ODTÜ RF MEMS Üretim Süreci olarak adlandırılan bir yüzey mikroişleme süreci ile üretilmiştir. Bahsi geçen RF MEMS empedans ayarlayıcı 6-20 GHz frekans bandında çalışmak üzere tasarlanmış ve Smith Abağı'nı 1331 empedans noktası ile tarayabilmektedir. Yapının ölçülen 729 empedans noktası göstermektedir ki, bu yapı ile Smith Abağı'nın çok büyük bir bölümü bahsi geçen bandın tamamında kapsanabilmektedir.

RF MEMS faz kaydırıcı 15 GHz frekansında 0-360° faz aralığını 10°'lik adımlarla tarayabilecek şekilde tasarlanmıştır. Üretilmiş olan faz kaydırıcının ölçümü yapılan 21 durumundaki ortalama faz hatası 1.7°, araya girme kaybı -3.1 dB ve geriye dönüş kaybı -19.3 dB olarak elde edilmiştir. Ayrıca bu yapı; 30 GHz frekansına kadar ortalama -5 dB, 40 GHz frekansına kadar da ortalama -8 dB araya girme kaybı ile çalışabilmektedir. RF MEMS vektör kipleyici, 22.5-27.5 GHz frekans bandında, 3 adet genlik ve 8 adet faz durumu verebilecek şekilde tasarlanmıştır. Üretilmiş olan vektör kipleyicinin, 22.5, 25 ve 27.5 GHz frekanslarında yapılan 24'er durum ölçümünde ortalama, 0.5 dB genlik hatası, 4° faz hatası ve -15 dB geriye dönüş kaybı ile çalıştığı görülmüştür.

Bu tezde sunulan sonuçlar bir kez daha göstermektedir ki, ODTÜ RF MEMS Üretim Süreci olgundur ve karmaşık RF MEMS yapıların üretiminde başarıyla kullanılabilmektedir.

Anahtar Kelimeler: RF MEMS, empedans ayarlayıcı, faz kaydırıcı, vektör kipleyici, MEMS anahtar.

To My Family

ACKNOWLEDGMENTS

First, I would like to express my sincere appreciation and thanks to both of my supervisors Prof. Şimşek Demir and Prof. Tayfun Akın. I would like to thank Prof. Şimşek Demir for following, attending, and supporting each step of my research wherever possible, and also caring for me more than I do for myself, not only in the academic sense, but also in all the remaining parts of life. I would like to thank Prof. Tayfun Akın for giving me the opportunity to join his group, providing this extraordinary research environment in my country, and introducing me the invaluable people in his group. He was so kind and patient to listen to me for hours whenever I need at the hard times of all parts of my life.

I would like to thank Prof. Sencer Koç for taking the time to solve the points that I had stuck and supporting for being on my committee. I also would like to thank Prof. Hayrettin Köymen for taking time to serve on my committee, and also for his innovative solutions. I am indebted to Prof. Altunkan Hızal for taking time to attend to all of my committee meetings even though he was not a member, providing the millimeterwave laboratory environment, and encouraging me during the whole thesis study. I would like to acknowledge Prof. Özlem Aydın Çivi for her help and support during this Ph. D. study.

Words fail me when I try to express my gratefulness to Dr. Kağan Topallı after 13 years. He gave me priceless support during this Ph. D. study, and a shoulder that I can hold on at all the hard times of my life. I would like to thank the members of the METU RF MEMS Group, especially Hüseyin Sağkol (TU Delft), Halil İbrahim Atasoy, and Çağrı Çetintepe for their support and friendship. I also would like to acknowledge İpek İstanbulluoğlu Turhan, Engin Ufuk Temoçin, Ömer Bayraktar, İlker

Comart, Ozan Doğan Gürbüz, Caner Güçlü, Ahmet Hayrattin Yüzer for their help and friendship.

There are many people who helped me along the way in numerous ways. I would like thank the former and present members of the METU MEMS and BIOMEMS Groups. I would specially like to thank Murat Tepegöz. He is much more than a friend for me, and I owe much to him. I also would like to thank Dr. Mustafa Seçmen, Dr. Mahmud Yusuf Tanrıkulu, and Dr. Said Emre Alper in all sincerity for their nice accompany during the past 8 years. I would like to acknowledge Dr. Özge Zorlu for his friendship and help.

This research would not have been possible without the support of a special person, Orhan Akar. I am deeply indebted to him for his help, never-ending support, and friendship. I also would like to thank all of the personnel both inside and outside the cleanroom at METU MEMS Center fabrication facilities for their support.

I would specially like to thank my parents, Mustafa Ünlü and Kübra Ünlü, for their everlasting love, encouragement, and support throughout my whole life. I would not have been here without them, and I understand their priceless value more on every passing day of my life. I also would like to thank my grandfather Kenan Kul, who is my first mentor, my uncle Emre Kul, and all the elder and younger members of my family, who supported me with their prayers.

Last but not the least, I would like to express my deepest gratitude for my wife Nuriye for her everlasting love, patience, encouragement, and support. This achievement is as much hers as it is mine. I also would like to thank my son Ahmet Selim for being joy of my family.

Finally, I would like to thank TÜBİTAK BİDEB for the scholarship during my Ph. D. study.

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INTRODUCTION

The way of making things smaller always attracted scientists' attention, especially after a high number of technological inventions were achieved in the twentieth century. Dr. Richard Feynman's famous talk, "There's Plenty of Room at the Bottom" [1] was maybe one of the best foresights about what the technology will become in today's world. Micro-Electro-Mechanical systems, namely MEMS, are one of exciting and emerging technologies that Dr. Feynman had foreseen its potential. MEMS technology is the way of doing things in the "micro" world that are used to be done in the "macro" world. The advantage brought is more than just reducing the size; MEMS are employed as miniature embedded systems that also use the advantages brought by the microelectronics. They enable higher level functions, they integrate a number of functions in one single package, and they decrease the costs using the benefits of the batch fabrication technology.

MEMS have been developed starting from 1970s, and today, they are becoming one of the mature fields of electronics with a high number of manufacturers and research institutes, and the demand on MEMS is increasing day by day. The MEMS market value is reported to be 7.1 billion USD in 2007, and it is expected to be 14 billion USD by 2012 [2]. The MEMS products include inkjet printer heads, pressure sensors, accelerometers, gyroscopes, microdisplays, microbolometers, Si microphones, MOEMS, microfluidics, micro probes, micro fuel cells, and RF MEMS. Figure 1.1 shows the MEMS market forecast for the 2007-2012 period [2].

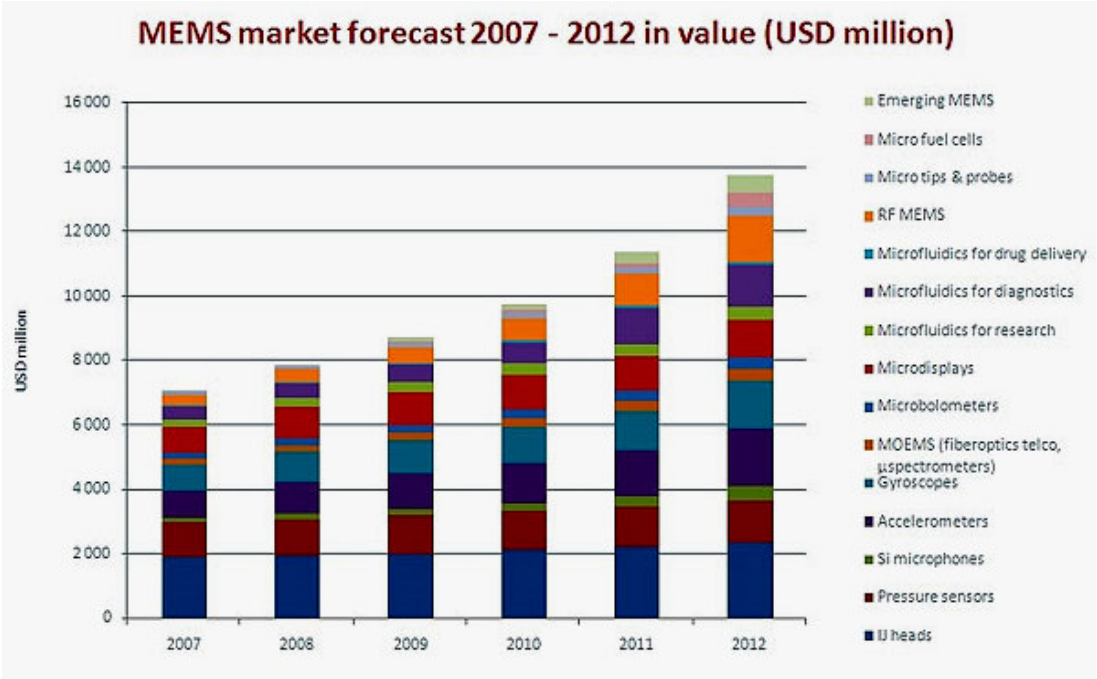

Figure 1.1: The MEMS market forecast for the 2007-2012 period [2].

One of the highly emerging fields of MEMS is the MEMS for radio frequency applications, shortly RF MEMS. Although the research on RF MEMS started much later than the other fields of MEMS, they gained a huge popularity. The first RF MEMS structure was demonstrated by Larson et al. in 1991 [3], which was a mechanical switch specifically designed for microwave applications. This work was followed by two outstanding switches in 1995, which were the metal-to-metal contact type Rockwell switch [4] and the capacitive type Texas Instruments switch [5] suitable for DC-60 GHz and 10-120 GHz applications, respectively. These works gave rise to the RF MEMS research all around the world with several universities and companies, which include the giant electronics manufacturers such as Motorola, Analog Devices, Samsung, Omron, NEC, and ST-Microelectronics. Today, RF MEMS technology is on the way to become one of the mature fields of microwave electronics, and the RF MEMS market is growing gradually day-by-day. Figure 1.2 presents the market forecast for the RF MEMS switches for the 2006-2011 period [6].

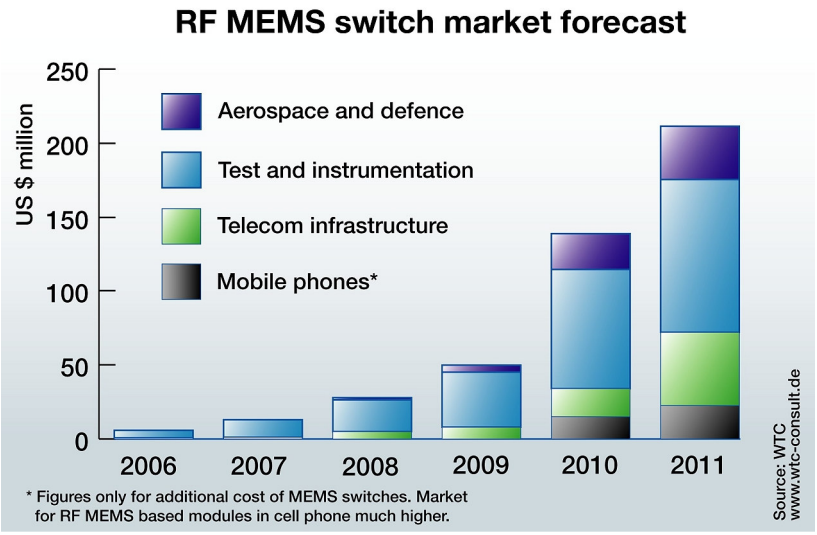

Figure 1.2: The MEMS market forecast for the 2007-2012 period [6].

RF MEMS offer important advantages in the switching devices technology with respect to their semiconductor rivals [7]. The most important one is the cut-off frequency, which is about 40 THz, and this value is 20 times of its closest rival by 2001. The other important advantages brought by RF MEMS technology is high linearity, low insertion loss, high isolation, and low power consumption.

A number of RF MEMS components and systems have been developed all around the world using RF MEMS technology. These are mainly concentrated on the switches ([7]-[15]), the varactors ([7], [16], [17]) and monolithic and hybrid components and systems that use RF MEMS switches such as phase shifters ([7], [18]-[30]), reconfigurable impedance matching networks ([31]-[37]), reconfigurable filters ([7], [38]-[42]), and reconfigurable antennas ([43]-[52]). There are also components other than the switches and switch based structures that are outcomes of this technology. Research on static micromachined components such as inductors, transmission lines, high-Q resonators, filters, and antennas; thin film bulk acoustic resonators (FBAR) and filters; and micromechanical resonators and filters

are carried out by universities and companies all around the world [53]-[55]. Among all of the RF MEMS components, FBARs are the first commercial ones [56].

The advantages brought by RF MEMS technology make these components strong candidates for a high number of applications in the microwave world, which are summarized in Table 1.1. Although the performances demonstrated by RF MEMS components are promising for these applications, these components should be ready for batch fabrication, which means that the problems of RF MEMS components should be solved. The main problems of RF MEMS components are high actuation voltage requirements, relatively low speed, reliability, power handling, packaging, and cost. The high actuation voltage requirement is solved by means of voltage upconverter circuits with the price of additional cost. There are already a high number of application areas for the RF MEMS switches with their current switching speeds, which are about 1-100 μs. To solve the remaining problems, the research on RF MEMS was directed to these issues all around the world. Today, it is reported that metal-to-metal contact switch of RadantMEMS [14], which is commercially available by now, worked for 900 billion cycles at +20 dBm RF power (cold-switched) without any failure [57]. This switch was hermetically packaged using glass frit, which means that the packaging problem was also solved. Another switch from RadantMEMS was demonstrated to work for 13 billion cycles at 40 dBm (again cold-switched), which was fabricated using a modified process for higher power handling operation. In [58], it is reported that a capacitive, shunt RF MEMS switch worked for more than 100 billion cycles +20 dBm RF power (hot-switched) without any failure. This switch was also packaged using wafer-level micro-encapsulation [59]. The cost is not a major issue for defense and aerospace applications; however, the cost including the packaging is still a problem for the cost-driven commercial applications. These developments show that RF MEMS is on the way for becoming a mature technology, and more companies will be providing RF MEMS components from batch fabrication soon [60].

Table 1.1: The application areas of RF MEMS switches, varactors, and inductors [7].

Area	System	Number of Cycles (Billions)	Years
Phased arrays	Communication systems (ground)	1–10	2–10
	(space)	10–100	2–10
	(airborne)	10–100	2–10
Phased arrays	Radar systems (ground)	10–100	5–10
	(space)	10–100	5–10
	(missile)	0.2–10	1–5
	(airborne)	1–100	5–10
	(automotive)	1–10	5–10
Switching and reconfigurable networks	Wireless communication (portable)	0.01–4	2–3
	(base station)	0.1–100	5–10
	Satellite (communication and radar)	0.1–1	2–10
	Airborne (communication and radar)	0.1–10	2–10
	Instrumentation	10–100	10
Low-power oscillators and amplifiers (varactors, inductors)	Wireless communication (portable)	0.1	2–3
	Satellite (communication and radar)	0.1–1	2–10
	Airborne (communication and radar)	0.1–10	2–10

RF MEMS Elements:	Switch, Varactor, Inductor
Subsystems:	Switching networks[a]
	Transmit/receive switches
	Very high isolation switches (instrumentation)
	Programmable attenuators
	Phase shifters (digital and analog)
	Reconfigurable antennas
	Reconfigurable matching (or impedance) networks
	Reconfigurable Butler matrices for multibeam systems
	Tunable filters
	Switched filter banks
	Miniature microwave filters
	Switched diversity antennas, oscillators, amplifiers
	Low phase-noise oscillators (fixed and tunable)
	High-efficiency networks (low-power systems)

[a]SPST, SPDT, DPDT, SPNT, $N \times N$, absorptive and reflective designs

The opportunities brought by RF MEMS technology today not only increase the component and the system performances, but also offer new aspects to build some new structures that cannot be implemented due to the performance limitations of

the components of the current state of the art semiconductor technology. For example, the idea of cascading many switching elements is not feasible since the insertion loss will increase rapidly and become intolerable. However, RF MEMS is an "enabling" technology, and it is possible to design totally reconfigurable structures and even control the whole physical layout of a distributed structure by means of RF MEMS switches [61], thanks to their very low insertion losses and high isolation. Even though this is limited to some special cases, the idea of changing the electrical length of a transmission line with small steps is achieved easily, which, in fact, is sufficient to implement structures with quasi-continuous control of performance using digital RF MEMS switches.

This thesis presents the theory, design, and implementation of reconfigurable circuits that are based on triple stub topology. The idea is to change the electrical lengths of the stubs precisely by means of RF MEMS switches or RF MEMS bi-state capacitors so that the performance of the circuit is controlled in a quasi-continuous manner. The triple stub topology is mostly used as an impedance matching network in the literature. However, it is theoretically and experimentally shown in this thesis that it is possible to control the phase and amplitude of the input signal simultaneously while the input return loss is exactly zero using the triple stub topology. In this thesis, the RF MEMS implementation of a novel impedance tuner, a novel phase shifter, and a novel vector modulator are presented using the triple stub topology.

The following parts of this chapter give the previous works on RF MEMS impedance tuners, RF MEMS phase shifters, and vector modulators. The chapter concludes with the organization of the thesis and the research objectives.

1.1. RF MEMS Impedance Tuners and Matching Networks

One of the applications that employ the advantages brought by RF MEMS technology is the impedance tuners or impedance matching networks. A low-loss, reconfigurable impedance tuner or impedance matching network with wide impedance coverage can be very useful for tomorrow's reconfigurable and intelligent systems. The possible applications of the RF MEMS impedance matching networks and impedance tuners include the impedance matching between a power amplifier and a radiating element; and noise or load-pull measurements, respectively.

Impedance tuners that are used in the noise or load-pull measurements are mostly mechanical devices with either coaxial or waveguide structures, and they use motors for reconfigurability. RF diodes and transistors are also used for impedance tuners; however, these designs introduce high insertion losses, and/or the impedance coverage is limited [62]-[66].

The first study on RF MEMS impedance matching networks was reported by Chiao et al. [67]. The authors use the idea of single stub matching, and the length of the transmission lines are adjusted by a sliding backshort plate on top of a transmission line. The position of the sliding short is changed by MEMS voltage controlled actuators.

The second RF MEMS impedance tuner was reported by Kim et al [68]. In this work, the authors presented two types of RF MEMS impedance tuners. The first one was an analog impedance tuner, which uses two shunt resonant cells connected in parallel to a transmission line. The resonant cells are operated near resonance frequency which allows the authors to obtain a large impedance variation. With this design, they obtained a voltage standing-wave ratio (VSWR) of 21.2 in Ka-band. The second design was a digital RF-MEMS impedance tuner which employs RF

MEMS switches to change the lengths of the two stubs of a double-stub network. The authors report a maximum VSWR of 32.3 with this second design.

The idea of using the triple stub topology on RF MEMS impedance matching networks is presented in [69] by Unlu et al.; however, the fabrication process was not mature at that time. So, measurement results were not presented.

A hybrid implementation of a reconfigurable double-stub impedance tuner was presented by Papapolymerou et al. [70]. The stubs were reconfigured using a digital capacitor bank in which the capacitors were selected using RF MEMS switches in order to obtain different load impedances. The microstrip parts of the design were implemented using standard lithography techniques on alumina substrate whereas the MEMS parts were implemented using surface micromachining on high resistivity Si substrate. The authors report that the structure can match loads with real parts between 1.5 Ω and 109 Ω and imaginary parts between -107 Ω and 48 Ω at 20 GHz.

A monolithic design on microstrip lines using ohmic contact MEMS switches was presented in [71]. The design has a double stub structure where the end of each stub is connected to a radial stub via MEMS switches forming a "3-bit, 3-bit" network. The aim of the design was efficiency optimization for a Class-E amplifier in X-band. The reported impedance range at 10 GHz is 0.63 Ω to 57 Ω in real part and -7.5 Ω to 51.8 Ω in the imaginary part.

Vähä-Heikkilä and Rebeiz presented the most mature reconfigurable impedance tuners, which employ the DMTLs. A 4-18 GHz design was implemented using a DMTL directly as an impedance tuner [72]. The authors also presented single stub topology for 20-50 GHz band [74], and double and triple stub [77] topologies to obtain wider impedance coverage. In all of these studies, the stubs and the interconnection lines are implemented using a few DMTL unit sections.

Qiao et al. [73] presented an intelligently controlled RF power amplifier with a reconfigurable RF MEMS varactor tuner for output matching. A double stub tuner is used for the output impedance tuner which employs MEMS switches and varactors. The gain and efficiency of the power amplifier is dynamically optimized by controlling the MEMS switches and the MEMS varactor control voltage for some known and unknown frequencies in 8-12 GHz band.

Another double stub design using shunt capacitive RF MEMS switches was demonstrated by Lu et al. [75]. Here, RF MEMS switches were used to change capacitance, and hence, the electrical length of the stubs. The two matching networks were used as input and output matching networks of a class AB amplifier to optimize gain and efficiency.

A tunable "double-slug" impedance matching network was demonstrated by Shen and Barker [76] which employs distributed MEMS transmission lines (DMTL). The design is composed of two 90° DMTL lines, which determine the operation frequency, and two other DMTL sections with electrical lengths θ_1 and θ_2 which determine the load value to be matched. Each switch of the DMTL structure is actuated separately resulting with adjustable θ_1 and θ_2.

Finally, an RF MEMS triple stub impedance matching network was presented by Unlu et al. [78], where the electrical lengths of the stubs were precisely reconfigured using a high number of RF MEMS switches.

In all of the above mentioned stub based studies except [69] and [78], only a small number of RF MEMS switches are employed on each stub. As a result, the electrical lengths of the stubs are digitally controlled with large steps, and the whole Smith Chart coverage could not be achieved because of the electrical length resolution of the stubs. Moreover, only a limited number of measured impedance points are presented.

The RF MEMS triple stub impedance tuner presented in this thesis employs 10 RF MEMS switches per stub, which is equivalently changing the length of the stub by $\lambda/20$ steps. This results with the coverage of the almost whole Smith Chart at the center frequency. The impedance coverage is better than all of the works in the literature, and a wide coverage is also obtained for the remaining frequencies of the design band. 729 out of 1331 measured impedance points are presented, which is limited by the packaging. This number is the highest presented number in the literature up to now.

1.2. RF MEMS Phase Shifters

Phase shifters are important crucial components for a number of applications in microwave and millimeterwave electronics. The phase shifters can be categorized in terms of design requirements, which are constant and linear phase versus frequency. The applications that require constant phase design are radar applications, communication systems, and components (SSB mixers, vector modulators, balanced amplifiers, etc.), and high precision instrumentation systems. The linear phase designs are mostly employed in phased array applications as true-time-delay networks.

The phase shifters are basically designed in two types, which are analog and digital controlled versions. The analog phase shifters, as the name refers, are used to control the insertion phase within 0-360° by means of varactors. The digital phase shifters are used to produce discrete phase delays, which are selected by means of switches.

There are three main technologies for the implementation of phase shifters, which are ferrite phase shifters, FET based phase shifters, and PIN based shifters. Ferrite phase shifters have low insertion loss, good phase accuracy, and they can handle

high power. However, they are bulky, they require a large amount of DC power, and they are slow compared to their rivals [79]-[81]. FET based [82]-[84], PIN based [85]-[87], and varactor diode based [88] phase shifters are the semiconductor alternatives for phase shifter. They propose low cost, low weight, and planar solutions to phased array systems. PIN based phase shifters provide lower loss compared to the FET based ones; however, they consume more DC power.

The phase shifters are implemented in several different topologies [7]. These include reflection-type [85], switched-line [84], loaded-line [86], varactor/switched-capacitor bank [88], and switched network [82] topologies. In all of these digital topologies (except varactor based one), the switching components are FETs or PIN diodes. Since the insertion losses of these components are high, the overall insertion losses of the phase shifters are also high. The reported insertion losses are about 4-6 dB at 12-18 GHz and 7-10 dB at 30-100 GHz [7].

The switches provided by emerging RF MEMS technology offer very low insertion losses, almost zero DC consumption, and very high linearity compared to these semiconductor components. As a result, RF MEMS phase shifters become strong alternatives for semiconductor based phase shifters, provided that the application area is limited to relatively low scanning arrays. A number of phase shifters are demonstrated that employ RF MEMS switches [7]. These include reflect-line [18], switched-line [19], [21], and 1:N switched-line [20] topologies. The reported average insertion losses of these designs vary between -1 and -2.2 dB, which are much lower than that of the semiconductor based designs.

One other alternative topology for the implementation of phase shifters is the distributed structures, which are used to obtain very wide-band circuits. The idea of distributed structures is to load a transmission line periodically with active or passive elements so that the parasitics brought by these elements are included as a

part of the transmission line model. Distributed amplifiers, oscillators, mixers, multipliers, and pulse shaping circuits were presented using this technique. Distributed phase shifters that employ Schottky-diode varactors were presented in [89] and [90], which are analog phase shifters and show good performance up to 20 GHz. Distributed phase shifters that employ RF MEMS varactors have also been presented in [22] and [23] for applications up to 110 GHz. The distributed RF MEMS phase shifters, or using the authors' labeling distributed MEMS transmission lines (DMTL), offer lower insertion loss than the semiconductor varactor based phase shifters. However, the tuning range of the standard MEMS varactors are about 1.3 practically, so the phase range of the analog DMTL phase shifters are lower than that of the semiconductor varactor based ones. It is possible to obtain higher capacitance ratio using a modified DMTL topology, in which the RF MEMS switch is used to select or unselect a static capacitance that is much larger than the upstate capacitance of the RF MEMS switch. Using this topology, a digital phase shifter design is attained with higher capacitance ratio and more reliable operation. Examples of the phase shifters using this topology are presented in [24]-[28], and the reported insertion loss is about at most -2.5 dB up to 60 GHz [7].

The RF MEMS phase shifter presented in this thesis uses on a novel topology, which is based on a triple stub network. The electrical lengths of the stubs and the interconnection lines are adjusted by means of DMTLs. The presented phase shifter is a linear phase design; however, the center frequency can be adjusted between 15 GHz and 40 GHz. This phase shifter design requires a high number of cascaded DMTL unit sections, which makes it possible to implement only using the "enabling" RF MEMS technology. To the author's knowledge, this phase shifter topology and its RF MEMS implementation are the first demonstrations in the literature.

1.3. Vector Modulators

The concept of the direct (or homodyne) modulation of the carrier signal has been found to be attractive in the last two decades, which is removing the IF stage from a conventional heterodyne transmitter [91]-[94]. The removal of the IF stage means to eliminate the set of IF modulators, filters, and amplifiers that are unavoidable once a conventional mixer is employed. The resulting system has much lower complexity and cost, which makes the direct modulation concept very attractive for the low-cost transmitters. The application areas include phased arrays, electronic warfare, automotive radars, measurement systems, and digital communications, which is maybe one of the most rapidly growing fields.

Direct modulators or in other words vector modulators play an important role in the implementation of the direct modulation systems. The vector modulators are used in the realization of amplitude-shift keying (ASK), binary phase-shift keying (BPSK), and more likely in quaternary (or quadrature) phase-shift keying (QPSK) and quadrature amplitude modulation (QAM).

The vector modulators are generally designed in two types, which are the cascaded (or α-ϕ) modulator and the I-Q modulator. The α-ϕ modulator consists of a cascade connection of an attenuator and a phase shifter, which can be seen in Figure 1.3-(a). The I-Q modulator divides the input power into two orthogonal vectors so that any vector can be obtained by applying phase and amplitude control on these vectors and finally by combining them. The block diagram of the I-Q modulator is given in Figure 1.3-(b). This topology is more popular compared to the former one, and it is implemented with many variations. The inphase combiner is common in most of the variations, but the divider at the input can be replaced by couplers, hybrids, splitters, etc. The more critical part is the phase and amplitude control part on each arm. Reflective type phase shifters with variable terminations, mixers, and high

pass/low pass structures are some of the alternatives that are used for the phase and amplitude control in vector modulators.

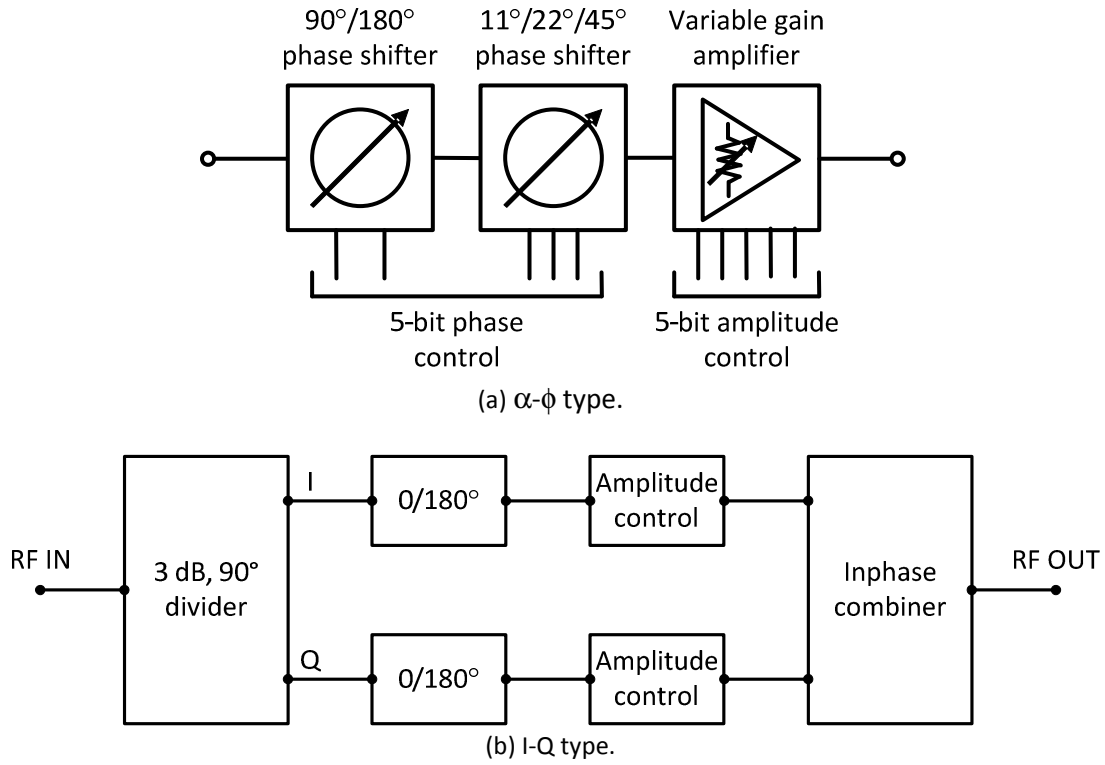

Figure 1.3: The block diagrams of the vector modulator topologies.

The research on vector modulators were started in 1980s, and mature vector modulators started to show up at the end of this decade. The α-ϕ vector modulators were first presented by Norris et al. [95], and these works were followed by other researches [96]-[98]. Devlin et al. [99] presented the first I-Q type vector modulator. This design employs quadrature power splitters with reflective FET terminations as variable resistances, which is actually a modified bi-phase modulator. An improved approach for reflective terminations was followed by Lo et al. [100], in which switching low noise amplifiers (LNAs) are implemented for BPSK. In this work, balanced reflective terminations were employed, and the parasitics inserted by reflective terminations are naturally

cancelled since two reflective terminations were used in a balanced manner. Ashtiani et al. [101] presented once of the fundamental publications of this topology following the above mentioned work. Ashtiani and his co-authors presented the successful usage of balanced reflective terminations on multiple-QAM (M-QAM) applications at 38 and 60 GHz using cold-pseudomorphic high electron mobility transistor (cold-pHEMT) technology. Ashtiani's approach was very attractive, and it is followed by many publications that use different technologies and work at different frequencies, only a limited part of which is referred here [102]-[105]. Although this approach was improved to be simpler and occupy less area by the same group [106], the former version is still more popular in the recent years, and it was implemented using different technologies such as HBT ([107],[110]), CMOS ([108], [109], [111]), and pHEMT ([112], [113]).

Another popular approach for the I-Q vector modulators is to use mixers. In this approach, the LO is divided into two orthogonal components. These components are modulated by means of two mixers, and finally, they are combined by means of combiners, amplifiers, couplers, etc. This approach was first presented by Pyndiah et al. ([114], [115]), and this work is followed by Telliez et al. [116]. Pyndiah et al. presented a QPSK modulator with double balanced mixers where Telliez et al. a 64-QAM modulator/demodulator with single balanced mixers. These works are followed by a number of publications [117]-[124], which include the implementations with the new solid-state technologies such as HBT [123], SiGe [124], and CMOS [122]. In these entire works, double balanced mixer topology is employed, which supplies better suppression of even-order distortion compared to a single balanced topology.

Modified versions of the I-Q modulators have also been presented. Primerose et al. [125] used a high pass/low pass topology for the phase (BPSK) modulators in the I-Q modulator topology. Burnsed et al. [126] obtained the four necessary quadrature vectors using high pass/low pass filter instead of couplers or dividers, and obtained

the desired vector by switching and changing the amplitudes of these vectors. Grajal et al. [127], who is followed by Ellinger et al. [128], used three base vectors separated by 120° instead of four quadrature base vectors in order to decrease the complexity. A similar approach is also presented by Altuntaş [129], where a four port 120° phase shifter is implemented. Wu et al. demonstrated two different methods that employ vector summation with the commercial CMOS processes ([130], [131]).

Alternative topologies are also presented for the direct modulators. Goldfarb et al. [132] used the SPDT switching for the implementation of a bi-phase modulator. Philibert et al. [133] employed anti parallel diode pairs as mixers monolithically, which is also applied in [134], where the diode pair is hybrid mounted on a multilayer thin-film multichip module. Another hybrid version that uses diode pair is presented on low-cost RF substrate [135]. In [136], a hybrid vector modulator is presented on ceramic substrate that utilizes FET transistors; and in [137], FET transistors are also utilized for a BPSK modulator on a microstrip based circuit.

Riza et al. proposed the photonic approach for vector modulation [138], and this work is followed by Jemison et al. [139], who used this approach in a vector modulator. The RF MEMS technology is applied for direct modulation circuits only in two examples. The first one is a BPSK modulator reported by Barker and Rebeiz, which is actually a 0/180° phase shifter [140]. The second one is also a BPSK modulator where an RF MEMS SPDT switch is employed [141].

The RF MEMS vector modulator presented in this thesis employ a novel topology, which is based on a triple stub network. This is the same topology that is also used in the RF MEMS phase shifter, where the electrical lengths of the stubs and the interconnection lines are adjusted by means of DMTLs. The vector modulator design only uses low-loss loaded transmission lines, i.e., DMTLs, and the amplitude modulation is obtained by using the resonating structure of open-circuit terminated

stubs. The presented vector modulator is a linear phase design; however, the center frequency can be adjusted between 22.5 GHz and 27.5 GHz. This design requires a high number cascaded DMTL unit sections, which makes it possible to implement only using the "enabling" RF MEMS technology. To the author's knowledge, the idea of amplitude modulation using low-loss transmission lines, the designed vector modulator topology and its RF MEMS implementation is first presented in the frame of this thesis.

1.4. Research Objectives and Organization of the Thesis

The goal of this thesis is to investigate the theory of triple stub topology, to design novel impedance tuner, phase shifter, and vector modulator circuits based on this topology, to fabricate the designed circuits using METU RF MEMS Fabrication Process, and to measure the performance of the fabricated circuits. The specific objectives that are used to achieve this goal are given as follows:

- *Improvement of the METU RF MEMS Fabrication Process.* The current fabrication process should be improved for more reliable and higher performance operation of the fabricated RF MEMS structures.

- *Design, modeling, fabrication, and measurement of the RF MEMS triple stub impedance tuner.* A reconfigurable, wide impedance coverage impedance tuner should be designed and fabricated, which demonstrates the possibilities that cannot be provided with other technologies.

- *Investigation of the theory of triple stub topology.* The theory of triple stub topology should be investigated in detail for ideal and non-ideal cases. Possible applications of this topology should be demonstrated both theoretically and experimentally.

- *Design, modeling, fabrication, and measurement of the novel RF MEMS phase shifter.* The novel triple stub topology based phase shifter should be designed, fabricated, and its performance and advantages should be demonstrated.

- *Design, modeling, fabrication, and measurement of the novel RF MEMS vector modulator.* The novel triple stub topology based vector modulator should be designed, fabricated, and its performance and advantages should be demonstrated.

This thesis is composed of seven chapters. Following this introductory chapter, Chapter 2 describes the METU RF MEMS Fabrication process, and also gives the optimization studies that are made for the improvement of the current fabrication process.

Chapter 3 gives the design, modeling, fabrication, and measurement results of the RF MEMS impedance tuner. This chapter also includes the design, implementation, and the usage of the Multi-pin MEMS Automated Measurement Setup.

Chapter 4 investigates the theory of the triple stub topology. In this chapter, theoretical and numerical analysis of the triple stub topology is presented for both ideal and lossy transmission line cases. Following that, the possible novel configurations such as phase shifter, vector modulator, power divider, etc. are explored, and design methodologies are proposed.

Chapter 5 starts with the application of the triple stub theory on the implementation of the novel RF MEMS phase shifter. It continues with the design, modeling, and the fabrication results. The chapter concludes with the discussion of the measurement results of the RF MEMS phase shifter.

Similar to Chapter 5, Chapter 6 presents the application of the triple stub theory on the implementation of the novel RF MEMS vector modulator. It gives the design, modeling, the fabrication results, and the discussion of the performance of the designed RF MEMS vector modulator.

Finally, Chapter 7 concludes the thesis where it summarizes the achievements of this thesis, and discusses the future research possibilities.

CHAPTER 2

METU RF MEMS FABRICATION PROCESS AND ITS IMPROVEMENT

2.1. Introduction

The fabrication of the RF MEMS structures is one of the most critical parts of this thesis. For this purpose, a surface micromachining fabrication process has been developed at METU-MEMS Center fabrication facilities in the past 9 years with efforts of several researchers[1]. With its current form, the fabrication process developed at METU, namely "METU RF MEMS Fabrication Process", is mature. It is demonstrated in the frame of this thesis and in the former work of METU RF MEMS Group that it is possible to implement complicated structures that employ many RF MEMS switches [142]. Nevertheless, the development phase is still continuing, and the fabrication process is always open for further development. The next section of this chapter gives the details of the METU RF MEMS fabrication process. This is followed by the optimization of some process steps that is developed in the frame of this thesis in order to improve the performance and the reliability of the RF MEMS components.

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[1] The current METU RF MEMS fabrication process is mainly developed together with Dr. Kağan Topallı. Mr. Hüseyin Sağkol, who is the first researcher of the METU RF MEMS Group, and Mr. Halil İbrahim Atasoy also contributed to the development of former or present versions. Mr. Engin Ufuk Temoçin, Mrs. İpek İstanbulluoğlu Turhan, Mr. Ömer Bayraktar, Mr. İlker Comart, and Mr. Çağrı Çetintepe has also involved and contributed to the application of the fabrication process in the past years. The optimization of the process development that is given at the end of this chapter is developed only by the author, and the other researchers have involved and contributed to the application of the fabrication steps.

2.2. METU RF MEMS Fabrication Process

2.2.1. Process Layers and Material Selection

The METU RF MEMS process is mainly composed of two metal, one isolation, and one resistive layer. A sacrificial layer is also used to supply the separation between the two metal layers. The first metal layer is used to define the coplanar waveguides (CPW) for the RF signal propagation as well as the DC lines for the actuation of the RF MEMS switches. The second metal layer is used to form the MEMS bridges, which are the mechanically movable parts of the structure. The isolation layer is used to prevent the DC short between the first and the second metal layers, which is necessary for the operation of the RF MEMS switches. In addition to that, it also forms the dielectric layer of the metal-insulator-metal (MIM) capacitance in both RF MEMS switches and other components. The resistive layer is used to form resistances that are used to isolate the RF lines from the DC lines. This is also necessary for the proper operation of the RF MEMS switches.

The METU RF MEMS fabrication process, with its current form, is implemented on 500 µm-thick, 4", low-loss quartz substrates. These substrates have relative dielectric constant of ε_r = 3.8, and their loss tangent can be better than 0.001 up to 60 GHz [143]. The electric fused quartz substrates [143] are chosen for the METU RF MEMS fabrication process considering antenna and millimeterwave applications. The METU process was formerly done on glass substrates, which have measured loss tangent of $tan\ \delta$ = 0.015-0.020. These substrates were left due to increasing loss performance of CPW lines, which will be explained quantitatively in the following parts of this chapter.

The METU RF MEMS fabrication process is composed of 7 layers and 6 lithography steps. The selection of the materials for each layer is quite important both from the

performance and the fabrication point of views. The material selection is a hard task as the deposition and the definition of each layer should not disturb any of the remaining layers. The selection should also be considered to preserve the RF performance since material properties may the limit the performance of the designs. Several materials and approaches have been tried for a properly working, reliable RF MEMS fabrication process in the past experience, which are explained in [144] and [145]. The current version is the 4th generation fabrication process that is developed at METU. The seven layers that are used in the fabrication process are summarized in Table 2.1.

Table 2.1: The materials used in the METU RF MEMS fabrication process.

Layer Name	Material	Abbreviation	Deposition Met.
Resistive layer	Silicon chromium	SiCr	RF sputtering
Adhesion layer	Titanium	Ti	DC sputtering
First metal layer	Gold	Au	DC sputtering
Isolation layer	Silicon nitride	SiN	PECVD
Sacrificial layer	Polyimide	PI	Spin coating
Strengthening layer	Gold	Au	Electroplating
Structural layer	Gold	Au	DC sputtering

The physical properties such as electrical conductivity, mechanical stress, thermal conductivity, etc. of the selected materials play an important role on the performance of the fabricated structures. The properties of the selected materials are very sensitive to deposition conditions, and they are usually not equal to the bulk material properties. The following properties of the materials are important, and the below mentioned consequences may occur due to the changes in the physical properties of the selected materials:

- *Resistive layer:* The electrical conductivity of this layer is important, and it determines the isolation level between the RF and the DC lines.

- *Adhesion layer:* This layer is used as an adhesion layer between the substrate and the first metal layer. The electrical conductivity of the adhesion layer affects the insertion loss of the RF MEMS structures.

- *First metal layer:* The electrical conductivity of the first metal layer is extremely important, and it dominantly determines the insertion loss of the RF MEMS structures. The roughness of this layer also affects the downstate performance of the capacitive RF MEMS switches.

- *Isolation layer:* The relative dielectric constant and the surface roughness of the isolation layer directly affect the downstate performance of the capacitive RF MEMS switches. These properties cause a strong degradation in the capacitance level if the layer is not deposited properly.

- *Sacrificial layer:* The mechanical stress of the sacrificial layer is important. This is because the sacrificial layer is a thick layer, and coated on more than 99% of the whole wafer area. If the stress level of this layer is high, it may buckle the wafer; moreover, it may also affect the stress level of the above layers.

- *Strengthening layer:* The layer is used to strengthen the anchor points of the RF MEMS switches so that they are resistant to the buckling. The mechanical stress of the strengthening layer is important since it affects the stress level of the structural layer. The electrical conductivity of this layer is also important, and it affects the insertion losses of the RF MEMS structures.

- *Structural layer:* The mechanical stress of this layer is vitally important, and it should have almost zero residual stress and controlled stress gradient. If the stress level of this layer is not very low, the MEMS bridges are buckled upwards or downwards depending on the situation, which directly disturbs

the RF performance, the insertion losses, actuation voltages, and lifetime of the RF MEMS switches.

Table 2.2 gives the thicknesses of the layers and the measured physical parameters of the materials that are used in the fabrication process. The electrical conductivities have been measured with four-point probe measurement method using Magnetron Model M-700 four point probe system. The residual stresses have been measured with the wafer buckling method using the Veeco Dektak 8 surface profiler.

Table 2.2: The measured physical properties of the METU RF MEMS fabrication process materials.

Material	Thickness (Å)	Electrical Cond. (S/m)	Residual Stress (MPa)	Relative permittivity
SiCr	1000	10000	Not measured	Not measured
Ti	200	Not measured	-740	NA
Au	9000	3×10^7	Not measured	NA
SiN	3000	NA	42	7
PI	15k-20k	NA	18[1]	2.9[1]
Au	20k-30k	1×10^7	Not measured	NA
Au	11k	~2×10^7	26	NA

[1] These values are provided by the manufacturer [146].

2.2.2. Process Flow

The METU RF MEMS fabrication process flow can be visualized as in Figure 2.1 and summarized as follows:

i) The process starts with the organic cleaning of the quartz wafers using piranha solution.

ii) The wafers are dipped into buffered HF for increasing the surface roughness of the wafers, which aims to increase the first metal layer adhesion.

iii) SiCr resistive layer is deposited using RF sputtering and patterned using wet etching (Figure 2.1-(a), Mask 1).

iv) Ti/Au first metal layer is deposited using DC sputtering and patterned using wet etching (Figure 2.1-(b), Mask 2). Ti layer is used as adhesion layer between the quartz substrate and Au layer.

v) SiN isolation layer is deposited using plasma enhanced chemical vapor deposition (PECVD) and patterned using the reactive ion etching (RIE) ((Figure 2.1-(c), Mask 3).

vi) Polyimide sacrificial layer is deposited using spin coating, patterned using lithography, and cured (Figure 2.1-(d), Mask 4).

vii) Au structural layer is deposited using DC sputtering (Figure 2.1-(e)).

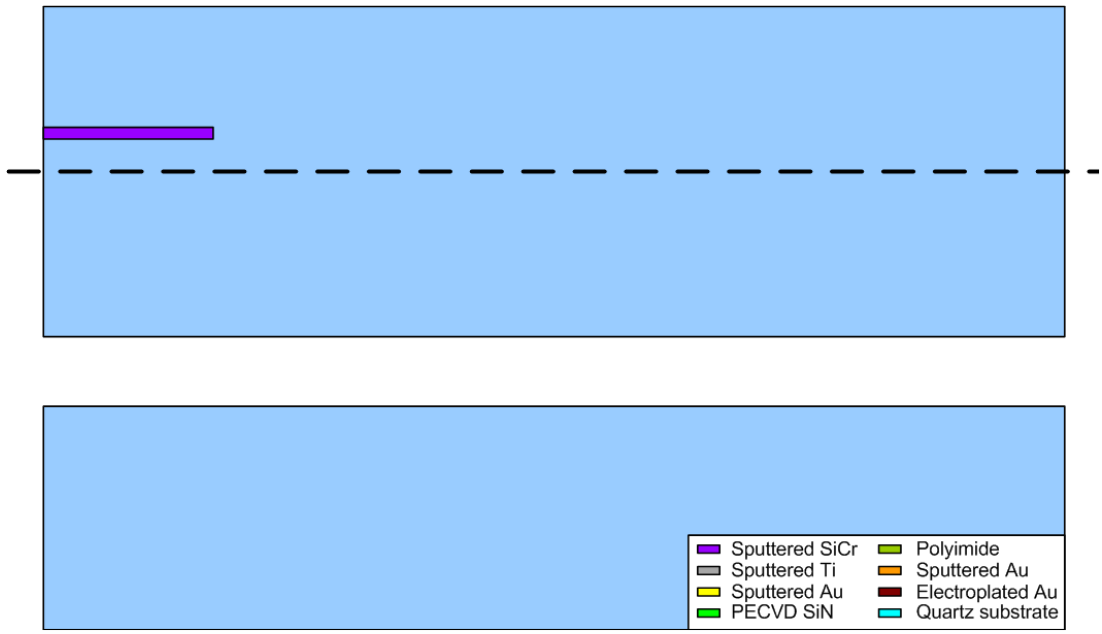
viii) Au strengthening layer is selectively deposited on the anchor point of the RF MEMS switches (Figure 2.1-(f), Mask 5).

ix) Au structural layer is patterned using wet etching (Figure 2.1-(g), Mask 6).

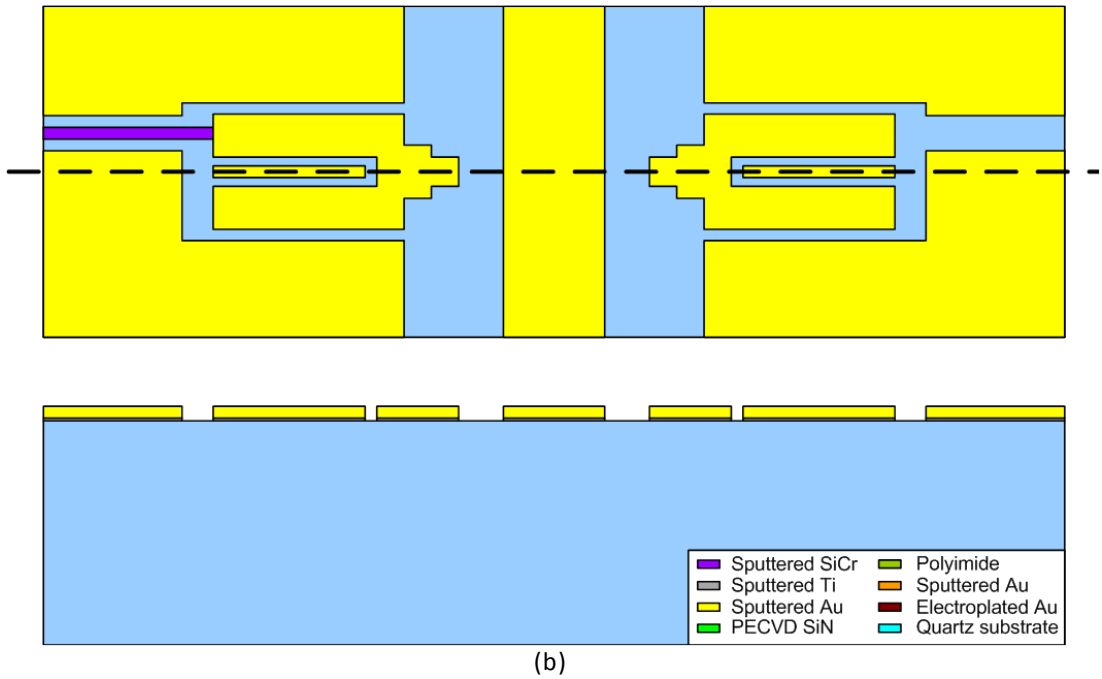
x) The sacrificial layer is wet etched, and the structures are released using critical point drying system (Figure 2.1-(h)).

The METU RF MEMS fabrication process is optimized for the implementation of the capacitive contact RF MEMS switches. It was also demonstrated that it is possible to implement metal contact RF MEMS switches successfully using this process [147]; however, the lifetime of the switches needs to be improved. This can easily be achieved by some modification without changing the process flow significantly.

The details of the METU RF MEMS fabrication process flow are given in Appendix.


Sputtered SiCr
Sputtered Ti
Sputtered Au
PECVD SiN
Polyimide
Sputtered Au
Electroplated Au
Quartz substrate

(a)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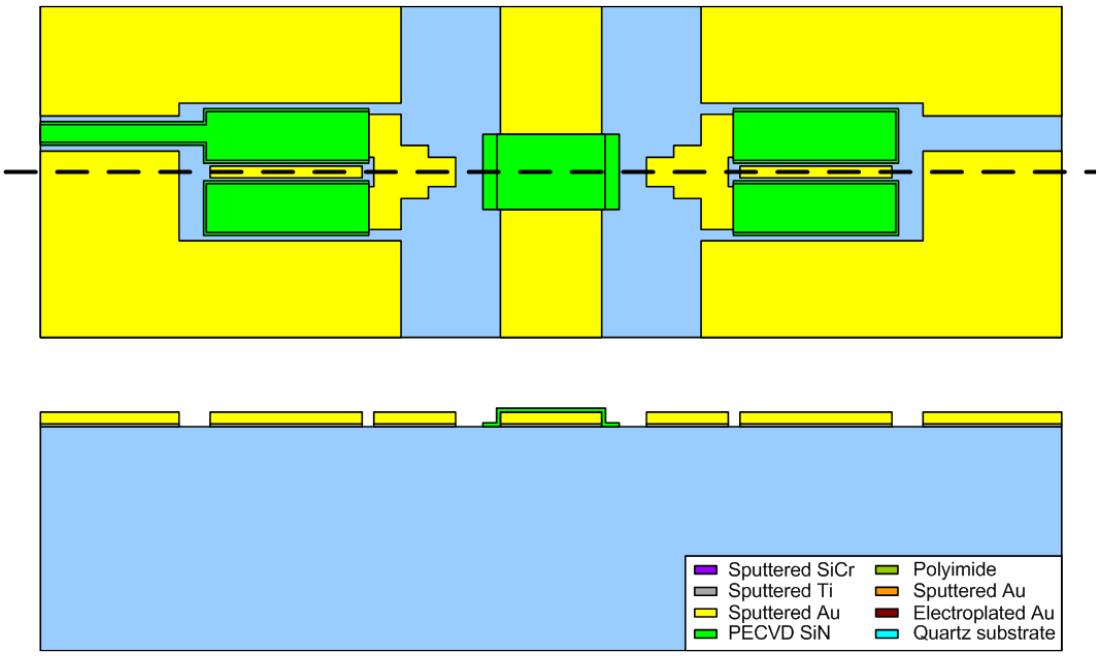
PECVD SiN
Polyimide
Sputtered Au
Electroplated Au
Quartz substrate

(b)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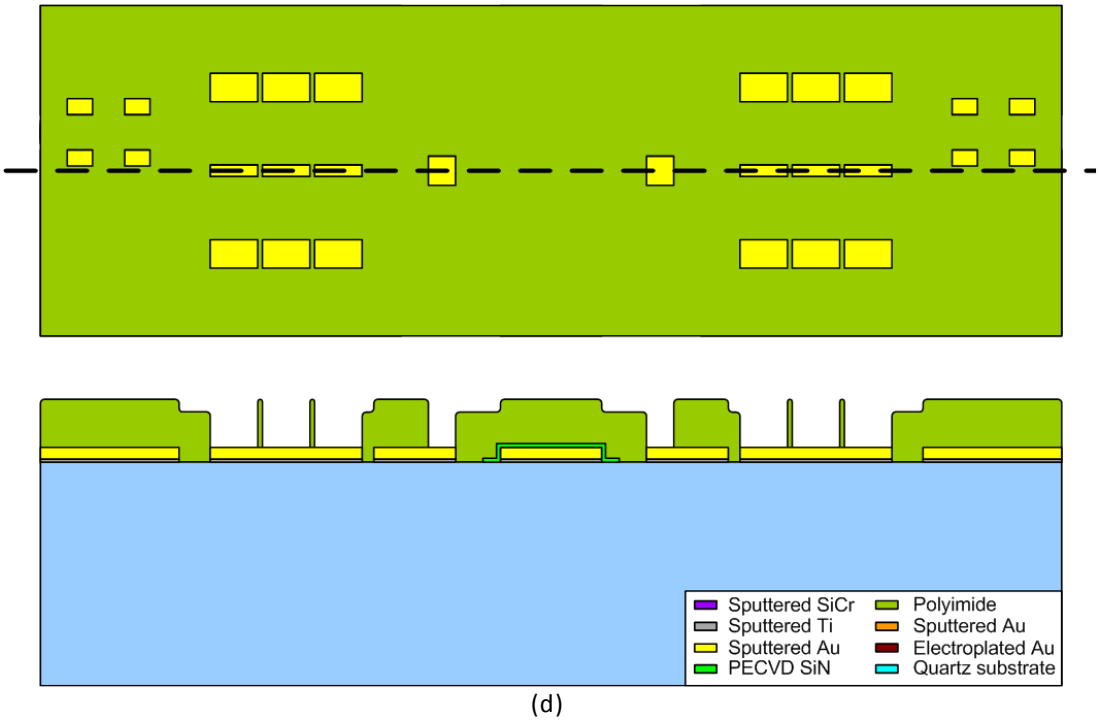
Polyimide
Sputtered Au
Electroplated Au
Quartz substrate

(c)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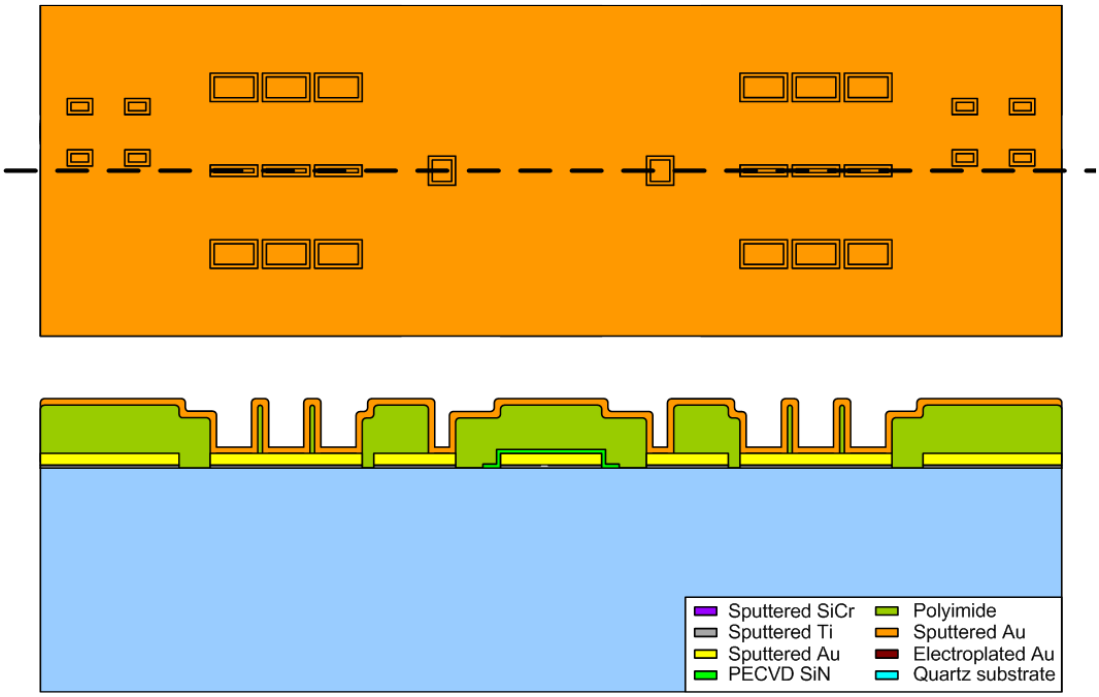
Sputtered Au
PECVD SiN
Polyimide
Sputtered Au
Electroplated Au
Quartz substrate

(d)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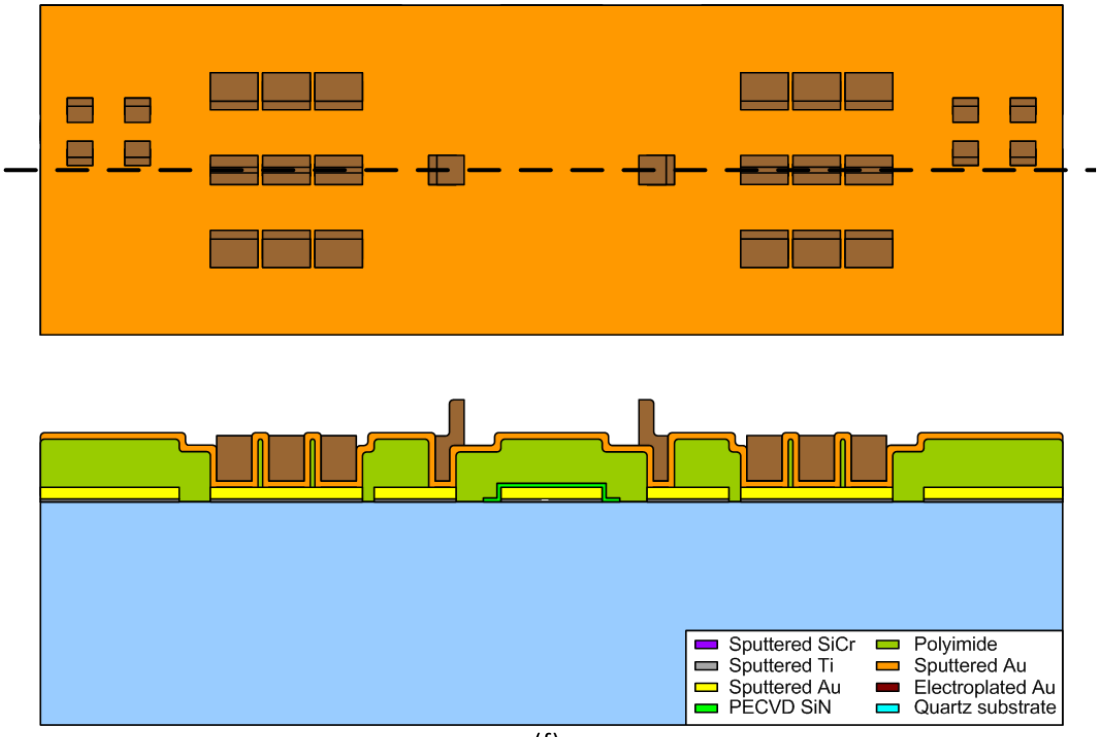
Sputtered Ti
Sputtered Au
PECVD SiN
Polyimide
Sputtered Au
Electroplated Au
Quartz substrate

(e)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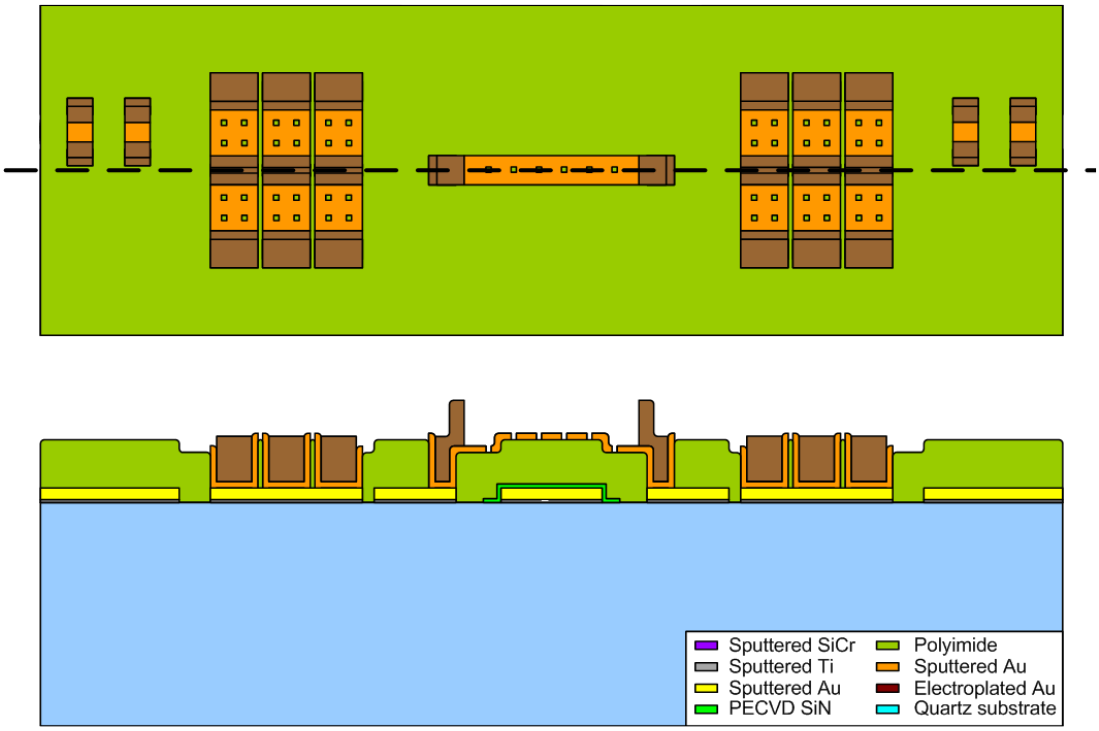
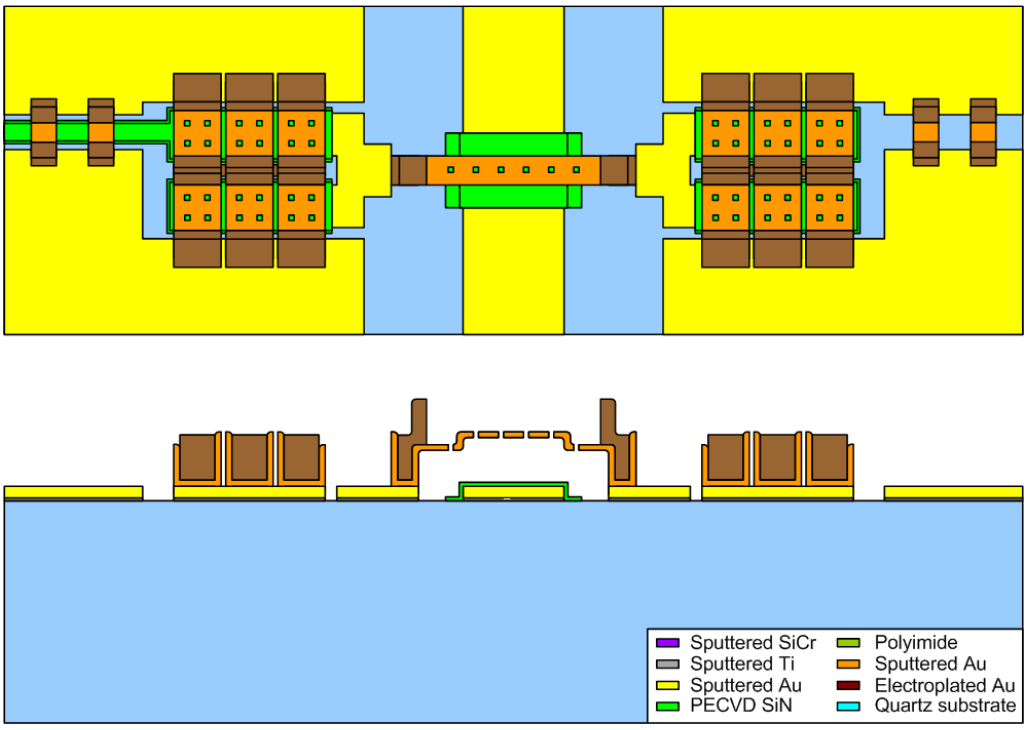
Sputtered Ti
Sputtered Au
PECVD SiN
Polyimide
Sputtered Au
Electroplated Au
Quartz substrate

(f)



(g)



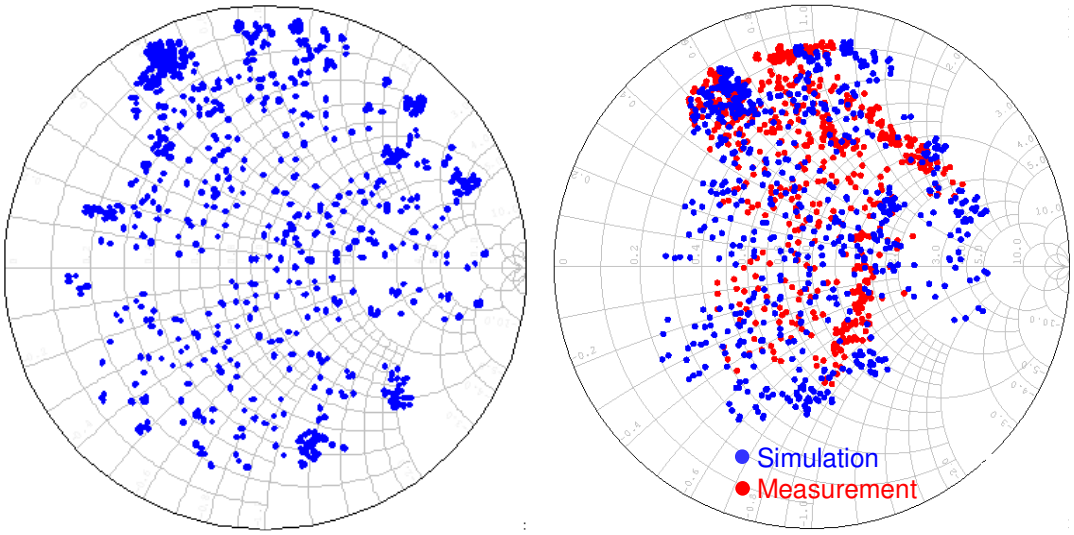
(h)

Figure 2.1: (a) The flow of the METU RF MEMS fabrication process.

2.3. The Optimization of METU RF MEMS Fabrication Process

A number of successful studies have been demonstrated that are implemented using the METU RF MEMS fabrication process ([142], [144], [145], [147]-[150]). However, two problems have always been observed in the measurement results of the fabricated RF MEMS structures in all of these studies. The first problem is that the insertion losses of the measured structures are much higher than the simulation results. The measured insertion losses are also higher than the results presented in the literature. The dominant loss mechanism for the RF MEMS structures is usually the loss of the first metal layer, and the conductivity of the gold layer is the primary responsible that determines the amount of the loss. Two examples are demonstrated in the following figures. Figure 2.2 shows the simulated impedance coverage of a triple stub RF MEMS impedance tuner compared with the measurement results. The right hand side figure shows that the increasing loss significantly reduces the impedance coverage. The second example is the degradation of the return loss of an RF MEMS frequency tunable antenna [49], which is given in Figure 2.3. It is clearly observed from the figure that the antenna return loss is also low even at the frequencies that it does not radiate, which means that the antenna dissipates the input power.

The second problem is the height of the MEMS bridges. In all of the above mentioned studies, it is observed that the MEMS bridge heights differ from the expected values due to the buckling of the MEMS bridges. The buckling can be upwards or downwards, and the residual stress and/or stress gradient of the structural gold layer is the primary responsible that determines the amount of the buckling. The examples for both cases are demonstrated in Figure 2.4. The change in the MEMS bridge height seriously affects the performance of the RF MEMS structures. This is because MEMS is generally used as tunable loading capacitances, and the change of these capacitances may distort the design performance, shift the design frequency, increase the losses, etc.



(a) α_{unl} = 70 dB/m (b) α_{unl} = 110 dB/m

Figure 2.2: The comparison of the simulated and the measured impedance coverage of an RF MEMS impedance tuner for different unloaded line loss values.

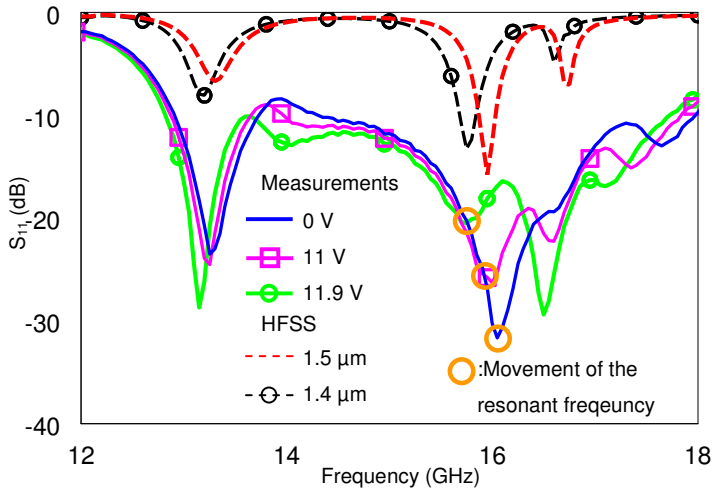
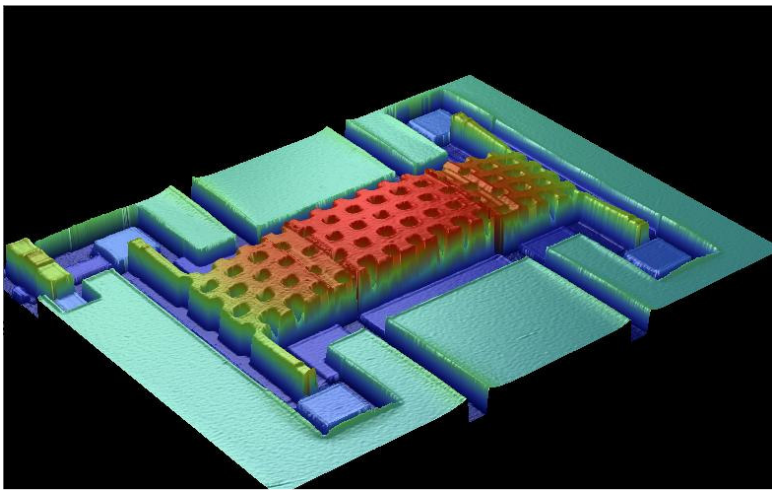
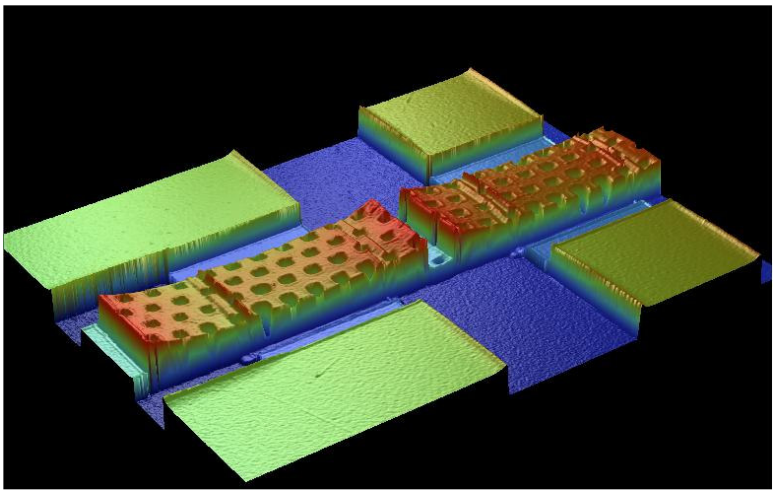


Figure 2.3: The comparison of the measured and simulated return loss performance of a tunable RF MEMS antenna [49].



(a)



(b)

Figure 2.4: Examples of the RF MEMS structures from previous runs that suffer from buckling due to residual stress (a) Compressive stress level (b) Tensile stress level.

To overcome the problems of the current fabrication process, separate optimization studies have been made to obtain a high-conductivity Au first metal layer and a low-stress Au structural layer. These studies will be explained in the following subsections.

2.3.1. Optimization of the Conductivity of the Ti/Au First Metal Layer

The first metal layer of the METU RF MEMS fabrication process is composed of Ti and Au layers, both of which are deposited using sputtering. Sputtering is a physical vapor deposition (PVD) method, and in this method, the deposition conditions such as type of sputtering setup, ion energy, substrate bias, gas type and pressure, atomic mass of gas and target atom, substrate temperature, angle of deposition and emission, and target are some of the important parameters that control the properties of the deposited films [151]. These properties control a number of film properties namely residual film stress, thickness, density, porosity, film morphology, elastic modulus, hardness, electrical conductivity, TCR, chemical etch rate, optical reflectance, color, etc.

For the first metal layer of the METU RF MEMS fabrication process, the important film parameters are the electrical conductivity, optical reflectivity, which is directly related with surface roughness, and residual stress. The electrical conductivity is the vitally important for the performance of the fabricated RF MEMS structures. For this purpose, an optimization study is made in order to obtain highest possible electrical conductivity with acceptable surface roughness and residual stress.

There are a high number of publications on the characterization of the thin films that are deposited with sputtering. The theoretical and experimental studies present the correlation of the deposition conditions with the film properties. The PVD theory says that the deposited film microstructure is modeled with zones that are determined due to the ion energy and the substrate temperature with respect to the melting temperature of the deposited material [152]. It is stated that the *zone T* is the most suitable region for device fabrication since the films in this zone yields refractory coating at relatively low temperatures. Moreover, the grains are small, dense, and formed in columnar forms [153]-[155], and the resulting film density is high [156]. Since high density films are necessary for obtaining high

conductivity, the films in this zone are feasible for the first metal layer of the METU RF MEMS fabrication process.

At the METU-MEMS Fabrication Facility, the tool used for the first metal layer deposition is Bestec planar magnetron DC sputtering tool [157]. Using this tool, the power (or DC bias), which is actually ion energy, gas pressure, substrate temperature, and the distance are the deposition conditions that can be controlled by the user. Ar is used as the inert gas for sputtering. Considering the above discussion and the controls of the sputtering tool at the facility, a number of deposition trials are made, in which the major target is to maximize the Au conductivity. The process conditions of the trials are given in Table 2.3.

During the trials, the target is to obtain proper grain formation, and hence, increase the conductivity by increasing the film density as explained above. For this purpose, the substrate temperature is elevated, and the deposition rate is lowered by decreasing the applied power and increasing Ar pressure. The surface resistances of the deposited films are measured using the four-point probing technique, the thicknesses are measured using Veeco Dektak 8 surface profiler, and the conductivity values are extracted using the standard formulation. In the final recipe, which is Trial No 6, an electrical conductivity of 3×10^7 S/m is achieved. This is almost three times of the former conductivity value, which was not measured directly, but extracted from the RF measurements. This is 73% of the bulk conductivity of gold, which is 4.1×10^7 S/m. However, the measured conductivity of the metals that are deposited with sputtering can be different than their bulk conductivities [158], and the obtained value is close to the maximum values reported in the literature to the author's knowledge.

Table 2.3: The summary of the sputtering process parameters that are used for the electrical conductivity optimization of the first metal layer.

Trial No	Power (W)	Pressure ($\times 10^{-3}$mBar)	Temp. (°C)	Thickness (Å)	End Point (Å/s)	Rate (Å/s)	Sheet Resistance (Ω/□)		Conductivity (S/m)
							min	max	
1	150	2	RT	3100	1500	2.1	0.123	0.154	1.92×10^{7}
2	150	3	150	4600	2000	2.3	0.088	0.091	2.08×10^{7}
3	300	3	150	4800	2000	4.4	0.091	0.096	1.94×10^{7}
4	100	1.5	150	4600	2000	1.5	0.075	0.08	2.27×10^{7}
5	100	13	150	5500	2000	1.4	0.053	0.055	2.77×10^{7}
6	100	20	150	6200	2000	1.2	0.045	0.045	3.03×10^{7}

Another important parameter for the losses of the first metal layer is the substrate loss tangent. The METU RF MEMS fabrication process is used to be implemented on Pyrex glass substrates, which has $\varepsilon_r = 4.6$ and $tan\ \delta = 0.005$. These values are the values reported by the manufacturer at low frequencies [159]. However, at the microwave and millimeterwave frequencies, it is reported that the loss tangent can go up to 0.015-0.020, and it may change from wafer to wafer [28]. In order to reduce also the dielectric losses, quartz substrates are used for the METU RF MEMS fabrication process. The quartz substrates have $\varepsilon_r = 3.8$ and better than $tan\ \delta = 0.001$ up to 60 GHz [143].

For the verification of the obtained recipe and the performance of the quartz substrates, a CPW test structure with gap / signal / gap dimensions G / W / G = 25 µm / 170 µm / 25 µm are fabricated on glass and quartz substrates with first metal layer that is deposited both the optimized recipe and the old recipe. The measurement results of the fabricated CPW test structures are given in Figure 2.5. Table 2.4 gives the summary of the extracted material properties and the CPW losses. The results presented in the table also verify the DC measurements of the optimized first metal layer process and the expected tangent losses of both substrates.

Table 2.4: The extracted material properties and losses for the optimized and old Au sputtering processes on quartz and glass substrates.

Wafer Mat.	Metal. Process	Metal. Thickness (µm)	Sim. Loss[1] (dB/m)	Ext. Loss[1] (dB/m)	Extracted σ (S/m)	Extracted tan δ
Quartz	Optimized	1.2	63.3	66.6	3×10^7	0.001
Glass	Optimized	1.2	103	99.7	3×10^7	0.015
Glass	Old	0.6	188	172	1×10^7	0.020

[1]*The loss values are calculated and extracted at 20 GHz.*

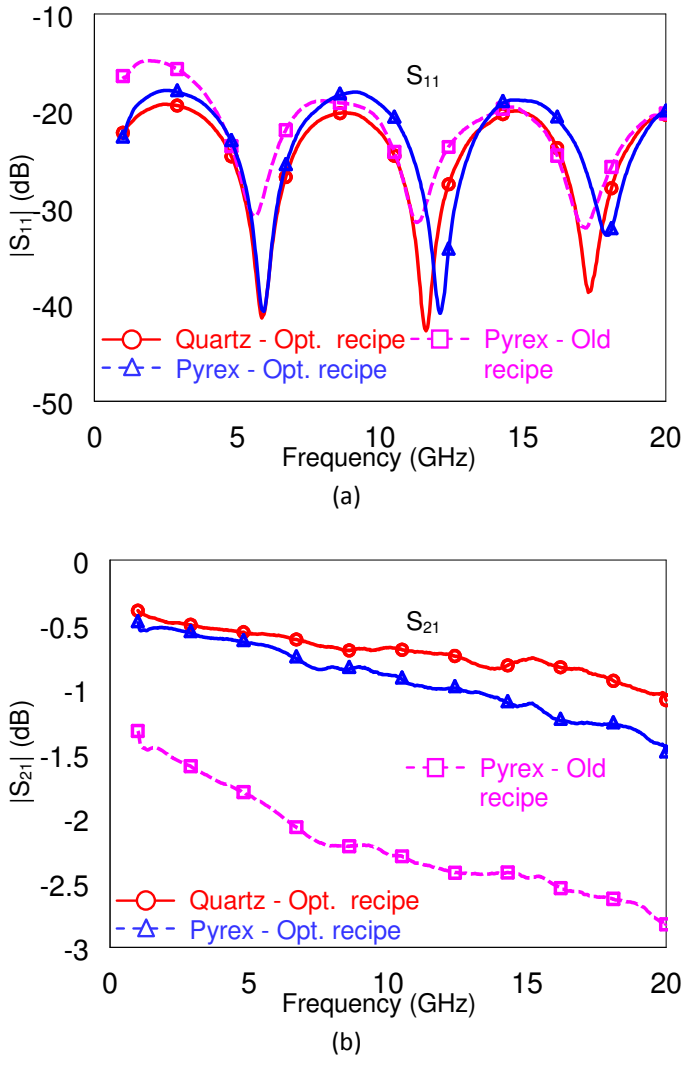


Figure 2.5: The measurement results of the CPW test structures that are fabricated on glass and quartz substrates with optimized and old first metal layer recipes (a) $|S_{11}|$ (b) $|S_{21}|$.

An optimization study is also conducted that aims to increase the conductivity of the strengthening layer, which is deposited using electroplating. The Au electroplating solution is a cyanide-based solution. This process was previously used to increase the thickness of the first metal layer. However, the process was quitted since the conductivity of this layer was too low. In the optimization study, the current density and the plating waveform is tuned in order to increase the conductivity of the electroplated Au layer. The conductivity of the deposited films is again measured from using four-point probing technique. Table 2.5 shows the measured material properties, which shows that the conductivity of the electroplated Au can be increased at most up to 1×10^7 S/m with this solution. This value is very low, and it is limited with the solution, which was not designed for microelectronic applications.

Table 2.5: The measured material properties for the Au electroplating optimization trial processes.

Trial No	Material	Current (mA)	Area (cm^2)	Time (min)	Temp. (°C)	Duty Cycle (%)	Thickness (µm)		Resistance (Ω/□)		Conductivity (S/m)	
							min	max	min	max	min	max
1	Au	228	57	20.00	32	50	1.55	1.73	$80x10^{-3}$	$86x10^{-3}$	0.71×10^7	0.69×10^7
2	Au	114	57	16.00	32	50	0.96	1.14	$93x10^{-3}$	$96x10^{-3}$	1.02×10^7	0.89×10^7
3	Au	114	57	16.00	32	10	1.04	1.32	$89x10^{-3}$	$95x10^{-3}$	0.97×10^7	0.91×10^7
4	Au	340	57	8.00	32	50	1.68	2.3	$77x10^{-3}$	$84x10^{-3}$	0.70×10^7	0.58×10^7
5	Au	114	57	16.00	32	50	0.96	1.13	$98x10^{-3}$	$103x10^{-3}$	0.96×10^7	0.75×10^7

Gold salt added to the electroplating solution as refreshment on the 5th trial.

2.3.2. Optimization of the Stress of the Au Structural Layer

The structural layer of the METU RF MEMS fabrication process is Au, and it is deposited also by sputtering. This layer should have minimum residual stress and stress gradient. As explained in the previous subsection, the sputtered film properties depend upon many deposition conditions. There are several publications in the literature that explain the formation of the stress and investigate

the effects of deposition conditions on the stress behavior. These publications are first demonstrated and leaded by Thornton and Hoffman [160]-[164], and followed by other researchers [165]. It is stated in these publications that the residual stress is predominantly compressive. The stress is formed because of the bombardment of the growing film surface by the energetic atoms arriving to the surface, which is the caused by the basic mechanism of sputtering. This leads to the generation of excess "interstitials" on the surface. The amount of interstitial formation is reported to be dependent upon incident atom energy and the sputtering gas pressure.

It is observed by the authors that the stress is compressive for low gas pressures and low deposition rates, where the incident atom energy is high. There also occurs a compressive-to-tensile transition for the deposited material. This point is mostly dependent upon the deposition conditions such as power and gas pressure that affect the incident atom energy. This behavior is explained by "atomic peening" model, which states that damage is induced at the growing film surface during either the bombardment of the highly energetic atoms or the atomic recoil. The atomic peening is also states that the amount of damage, i.e., the formed stress is correlated with the atomic mass of the deposited material, and it is shown that the materials with larger masses have more compressive stresses.

The effects of many deposition parameters on the film stress are explained in [164]. However, the sputtering tool used in METU-MEMS Fabrication Facility allows only a limited number of process parameters to be changed due to its nature. So, several trials are made in order to obtain low-stress Au films. During the trials, the applied power, the Ar pressure, and the substrate temperature are used as the optimization parameters, which are actually the main determinants of the stress. The stress level is targeted to be slightly tensile due to reasons that will be explained later. The temperature is also elevated in order to increase the adatom mobility, i.e., the mobility of the adsorbed atoms, so that the stress level is reduced [166].

The stress in thin films has been measured experimentally using different methods [166]-[168]. In this thesis work, the stress levels are extracted from the wafer curvature using Stoney formula [166]. The stress levels are measured using Veeco Dektak 8 surface profiler. Table 2.6 summarizes the process conditions and the measured stress levels of the structural layer optimization trials.

Table 2.6: The process conditions and the measured stress levels of the recipes that are measured on blank wafers for the structural layer stress optimization.

Rec. No	Wafer No	Mat.	Power (W)	Pressure ($\times 10^{-3}$mBar)	Temp. (°C)	Thickness (Å)	Rate (Å)	Stress (MPa)			
								tensile		compressive	
								avg	max	avg	max
1	-	Al	172	10	120	7000	-	81	365	-	-
2	-	Al	300	14	120	8200	-	47	70	-	-
3	-	Au	213	10	RT	6300	2.7	27	32	-	-
4	RD#11	Ti	300	2	150	~200	1.2				
		Au	100	6.6	150	5100	1.6	18	1.2	-6	-16
5	RD#12	Ti	300	2	150	~200	1.2				
		Au	100	9.3	150	5400	1.6	72	83	0	0
6	RD#13	Ti	300	2	150	~200	1.2				
		Au	100	12	150	5800	1.5	81	88	0	0
7	RD#14	Ti	300	2	150	~200	1.2				
		Au	100	14.7	150	6300	1.4	99	112	0	0
8	RD#15	Ti	300	2	150	~200	1.2				
		Au	100	4	150	4900	1.7	52	57	0	0
9	RD#17	Ti	100	9.3	150	-	0.2				
		Au	100	12.7	150	5800	1.5	0	0	-22	-25
10	RD#18	Ti	100	9.3	150	-	0.2				
		Au	100	12.7	150	5600	3.2	0	0	-29	-34
11	RD#22	Ti	100	9.3	150	1960	0.2	134	168	0	0
12	RD#23	Ti	300	2	150	2400	1.2	0	0	-726	-740

The results given in Table 2.6 include the stress levels of sputtered Au films as well as the stress levels of sputtered Ti and Al films. Sputtered Ti is used as the adhesion layer for sputtered Au, and it is also very effective although it is much thinner when

compared to Au. The stress level of the sputtered Al is investigated since it is used to be used as the structural layer of the METU RF MEMS fabrication process.

During the trials, the power level is first fixed to the level of the maximum conductivity process, and the Ar pressure is swept in a large range in order to find the compressive-to-tensile transition point (zero transition). The stress level increase in tensile direction with increasing Ar pressure as stated by the theory. Then, the deposition conditions of the Ti adhesion layer are changed without changing the deposition conditions of the Au layer. The residual stress of the Ti layer is also measured separately as explained above, and it is found out that the stress level is changing in an extremely wide range from -740 to +168 MPa (Recipe 11 and 12). The effect of Ti is easily observed on the results given in Table 2.6 (Recipe 6 and 10). Finally, two solution points are found, which are Recipe 3 and Recipe 4. The main difference between these recipes is the substrate temperature. One other point is that Recipe 3 is slightly tensile, and it is preferred due to the reasons that will be explained in the following parts of this chapter.

In order to verify the optimized recipes, they are applied as the structural layer of METU RF MEMS fabrication process. For the verification, the structural layer is implemented only together with the sacrificial layer on blank or Ti/Au coated glass substrates, and no other layers are deposited. Then, the sacrificial layer is etched, and the buckling amount is measured from the released MEMS test structures. Table 2.7 presents the summary of the optimization trials on MEMS test structures. The buckling amount is measured on a MEMS clamped-clamped beam, which is 300 µm-long and 80 µm-wide, using Veeco Wyko NT 1100 optical profiler.

Table 2.7: The process conditions and the measured buckling levels of the recipes that are measured on released MEMS bridge for the structural layer stress optimization.

Trial No	Wafer No	Mat.	Power (W)	Pressure ($\times 10^{-3}$ mBar)	Temp. (°C)	Thick. (Å)	Sacr. layer height (µm)		Sacr. spin spd (rpm)	Meas. stress (Mpa)	Meas. buckling
							min	max			
1	R#7	Au	213	10	RT	10000	2.5	2.76	3500	26	-1.5
2	RD#6	Ti	300	2	RT	200	2.24	2.36	4000	-740	-1.4
		Au	213	10	RT	10000				26	
3	RD#7	Ti	300	2	150	200	2.37	2.73	4000	-740	-1.3
		Au	100	20	150	10000				> 100	
4	RD#15	Ti	300	2	150	200	2.5	2.93	3000	-740	-1.2
		Au	100	6.6	150	11000				~0	
5	RD#15-2	Ti	300	2	150	200	2.5	2.93	3000	-740	-1.1
		Au	100	6.6	150	11000				~0	
6	RD#16	Ti	100	9.3	RT	200	2.61	2.75	3000	170	<-2.5
		Au	213	12.7	RT	10000				-	
7	RD#19	Ti	300	2	RT	2000	2.4	2.56	3750	-740	-1.4
		Au	213	10	RT	10000				26	
8	RD#20	Ti	300	2	RT	600	2.42	3.11	3750	-740	-1.4
		Au	213	10	RT	10000				26	
10	R#3	Au	213	10	RT	10000	2.54	2.98	3750	26	-1.4
11	RD#22	Au	213	10	RT	10000				26	+0.9
		Ti	300	2	RT	600	2.35	2.93	3750	-740	
12	RD#23	Au	213	10	RT	10000	2.27	2.9	3750	26	~0

Notes:

1) *The measured stress of the Au layer in Trial 1 and Trial 10 is 32 MPa (Table 2.6 Recipe 3).*
2) *The measured stress of composite Ti/Au layer in Trial 4 is ~0 MPa (Table 2.6 Recipe 4).*
3) *Trial 5 is the same as Trial 4 except the released structures are annealed 1 hour @ 200 ℃.*
4) *The measured stress of composite Ti/Au layer in Trial 6 is -25 MPa (Table 2.6 Recipe 9).*
5) *Ti is deposited upon Au layer in Trial 11.*
6) *The strengthening layer is added to the process (anchor filling).*

Recipe 3 is employed in Trial 1 where the MEMS clamped-clamped beam is buckled 1.4 µm downwards. At this point, this result was not expected, and it is concluded that the residual stress of the structural layer changes due to the thermal processes. Then, different recipes for Au are investigated; moreover, a different method is also applied, which is controlling the beam stress by using a bilayer structure [169]. In this case, the stresses coming from different layers compensate each other so that a buckling-free beam is obtained. For this purpose, Ti adhesion layer is added with different thicknesses (Trial 2, 7, and 8), Ti adhesion layer with tensile stress level is employed (Trial 6), other Au recipes are used (Trial 3 and Trial 4), annealing is used

(Trial 5), and finally Ti layer is deposited on top of Au layer (Trial 10). However, the resultant buckling was always downwards with different amounts. Only in Trial 10, the MEMS bridge is buckled 0.9 µm upwards, which opens the way to control buckling amount by means of Ti layer thickness.

The last result proves that this method can be used to obtain buckling free MEMS structures by changing the thickness of Ti layer; however, it is important to understand the reason behind the buckling of the beams in previous trials. To enlighten the situation, the beam theory is investigated using both analytical and numerical methods[1]. For the investigation, only residual stress is assumed, and no stress gradient is applied. The test structure is again the MEMS clamped-clamped beam, which is fabricated and measured for the optimization trials.

The beam theory states that if the residual stress is compressive, the beam can be buckled to upwards, downwards, higher order modes (sinusoidal for example), or no buckling is observed. This is because the anchor points are mechanically grounded, and the analytical solution of the problem results that these points are mathematically instable. As a result, all of the above mentioned cases may occur for a uniform beam. However, if there is an imbalance due to, for example a fabrication defect, it is expected to determine the state of the beam. If the residual stress in tensile, the beam theory states that there should be no buckling.

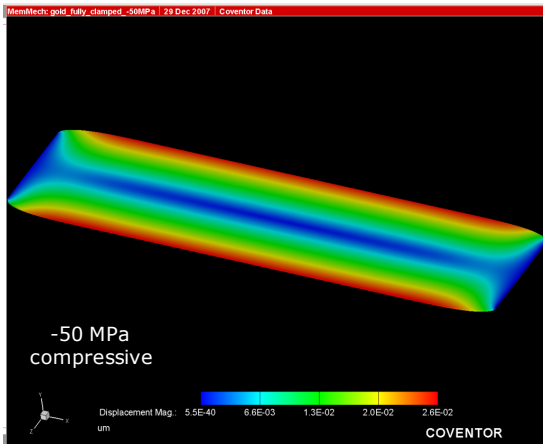
This phenomena is also verified with Coventorware [170] and SUGAR [171] simulations. Figure 2.6-(a) and (b) show that the beam is not buckled in the longitudinal direction from when it is fixed under -50 MPa compressive stress. However, if an imbalance is placed by thinning the beam at a position, the beam is buckled downwards as in Figure 2.6-(c) and (d). The beam is buckled 5.5 µm in this

[1] The theoretical analysis and Coventorware simulations are carried out by Korhan Şahin. The SUGAR simulations and other necessary Matlab simulations are carried out by Çağrı Çetintepe.

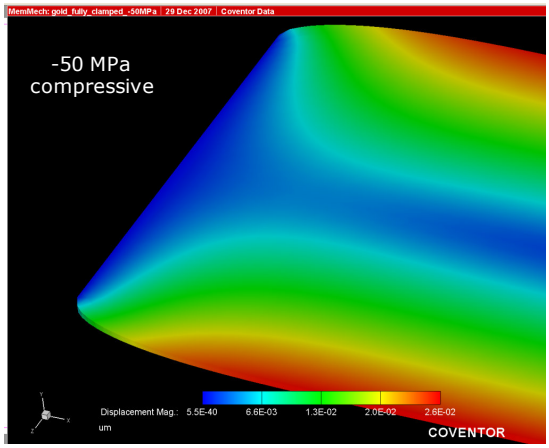
case, which is a significant result. The beam is not buckled under 50 MPa tensile stress as expected, which is shown in Figure 2.6-(e) and (f).

The fabricated MEMS structures do not have ideal mechanical grounds; instead, they are nominally clamped at the anchor points and connected to the substrate by only short beams of same thickness with the original beam. The anchor points in this case behave as imbalance points, and they change the beam shape under the presence of residual stress. For example, the beam buckles sinusoidally under -100 MPa compressive stress as in Figure 2.6-(g) and (h). The most important result is obtained when 50 MPa tensile stress is applied to the nominally clamped beam. The Coventorware simulations show that the beam is buckled downwards as in Figure 2.6-(i) and (j). This is the result observed also from the measurements. However, the amount of buckling is less than what is expected. SUGAR simulations also show similar response, and they give a better estimation of the buckling amount, which is about 1.4 μm.

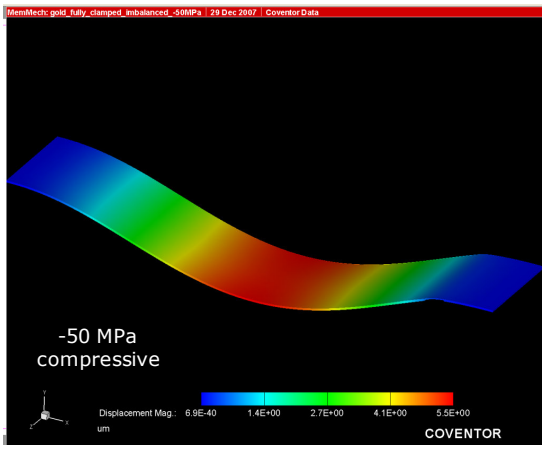
The above analysis clearly demonstrates that the buckling is not due to the amount of the residual stress, but it is because of the nonideal clamping of the MEMS beams. As a solution to this problem, the anchor points of the MEMS beams are filled in order to strengthen the clamping at these points. For this purpose, the strengthening layer is added to the process, which is used to fill the anchor points of the MEMS beams by Au electroplating. The measurement results of Trial 11 show that MEMS beams without any buckling are achieved. Figure 2.7 shows the measured 3D views and the beam shapes of the MEMS test beams from Trial 11, and comparison with the previous trials results, Trial 2 and Trial 10. The measurement results are obtained using Veeco Wyko NT 1100 optical profiler measurements. Figure 2.7 also includes the SEM picture of the MEMS test beam without any buckling.



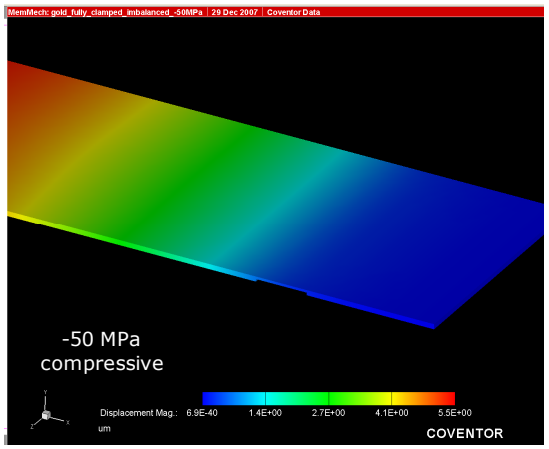
(a) Ideal clamping, compressive - No buckling.



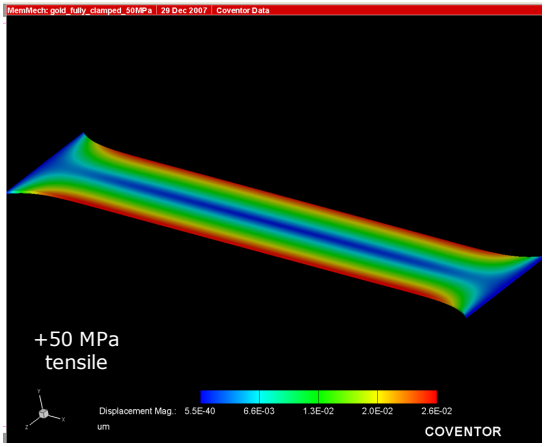
(b) Closer view of (a) at the anchor point.



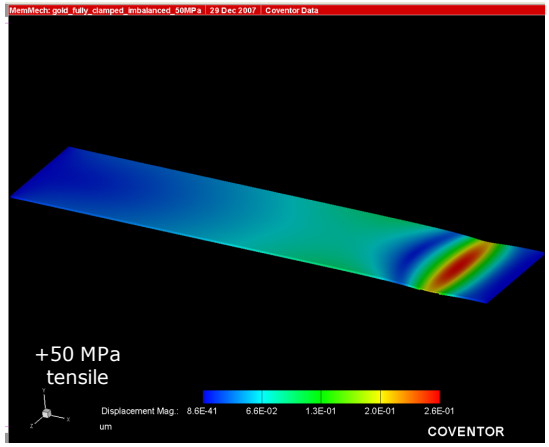
(c) Ideal clamping with imbalance, compressive - Downwards buckling.



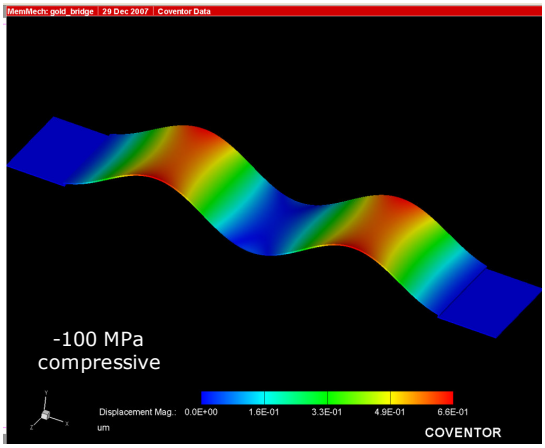
(d) Closer view of (c) near the imbalance point.



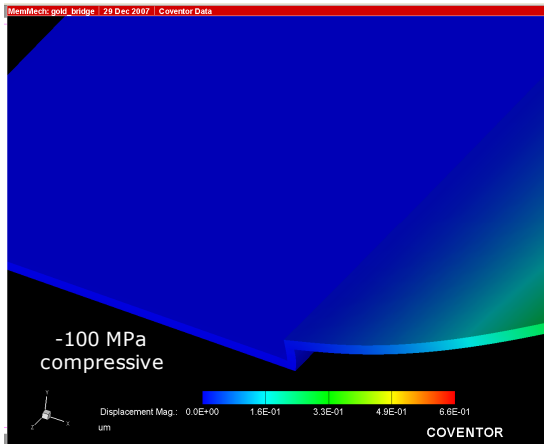
(e) Ideal clamping, tensile - No buckling.



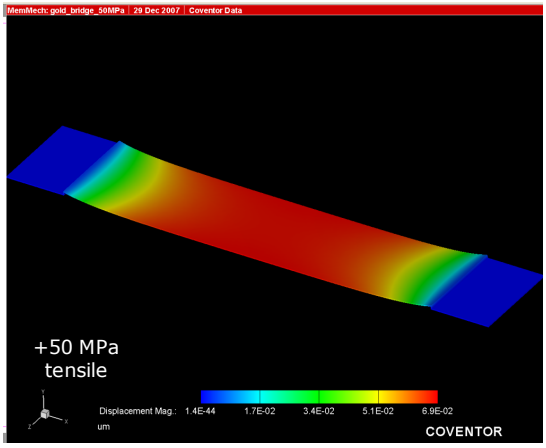
(f) Ideal clamping with imbalance, tensile - No buckling.



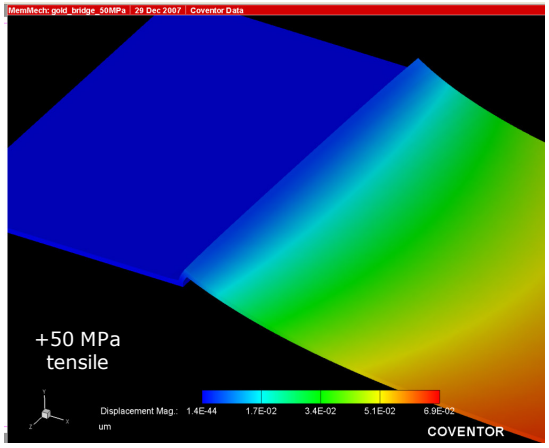
(g) Nominal clamping, compressive - Sinusoidal buckling.



(h) Closer view of (g) at the anchor point.

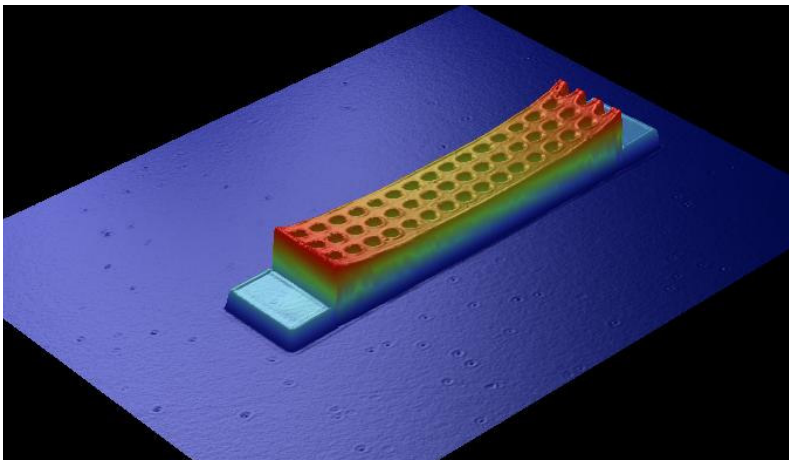


(i) Nominal clamping, tensile - Downwards buckling.

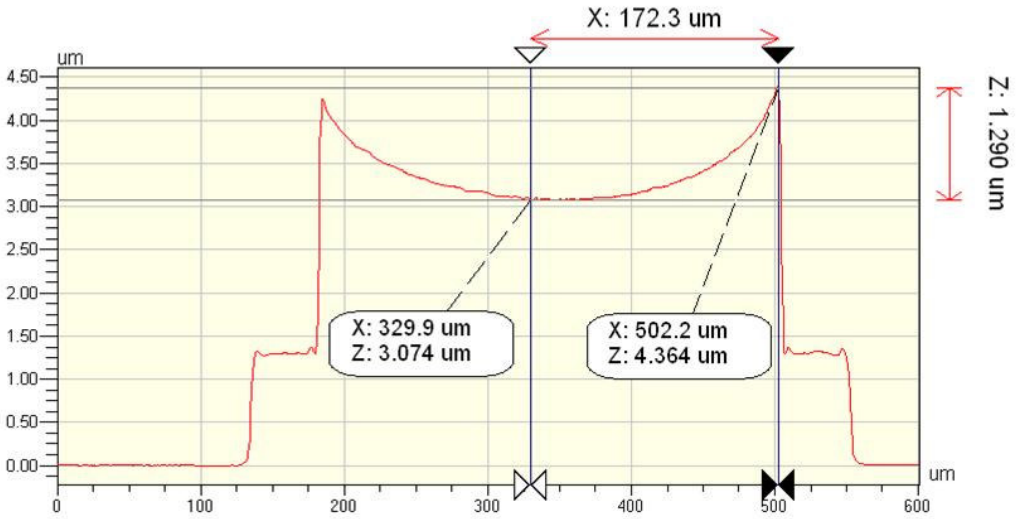


(j) Closer view of (i) at the anchor point.

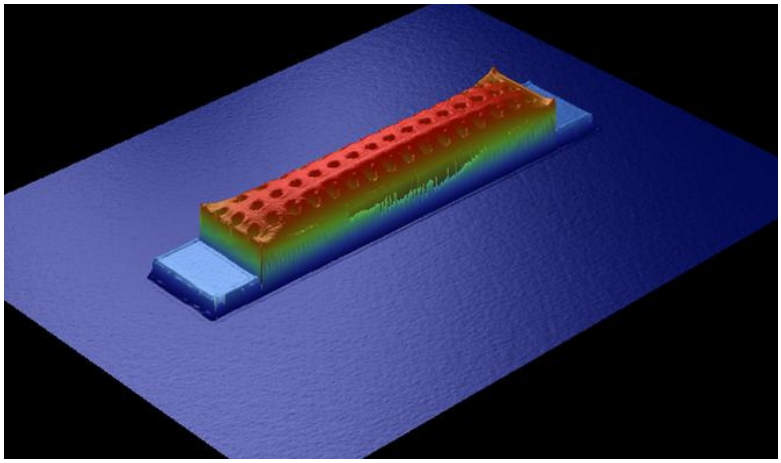
Figure 2.6: The snapshots of the MEMS beams simulated using Coventorware.



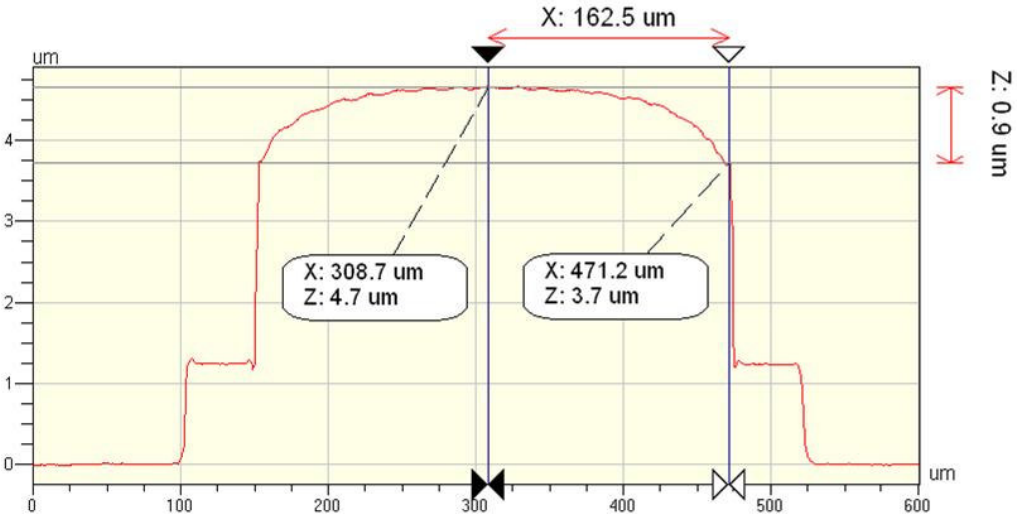
(a) Measured 3D view optical profiler view of the MEMS test beam from Trial 2 (RD#6).



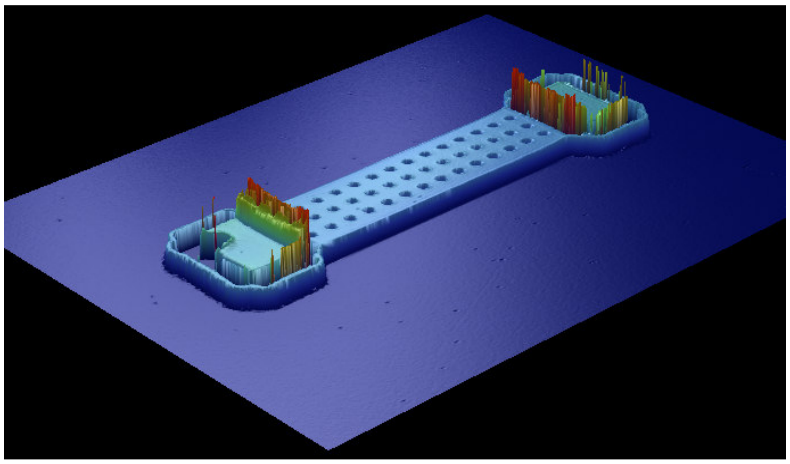
(b) Measured beam height variation of the MEMS test beam from Trial 2 (RD#6).



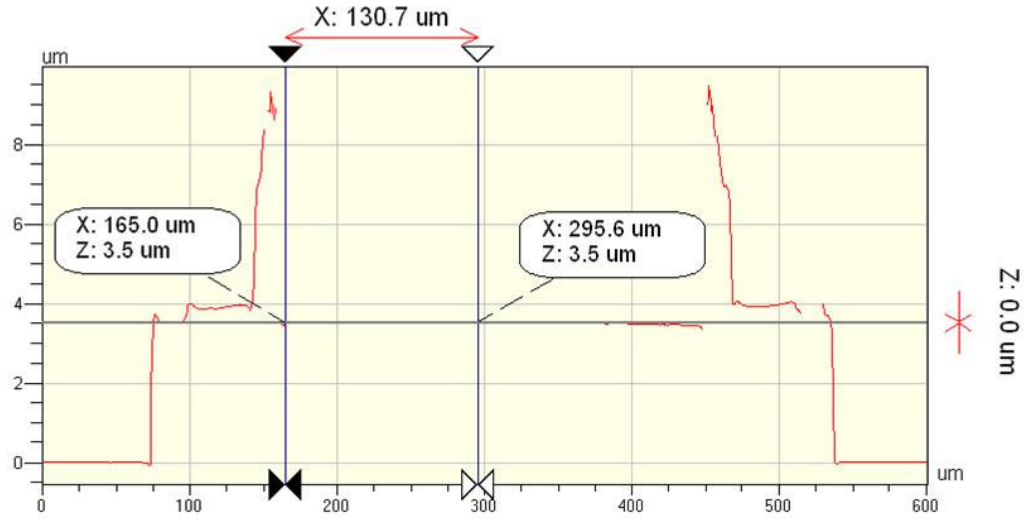
(c) Measured 3D view optical profiler view of the MEMS test beam from Trial 10 (RD#22).



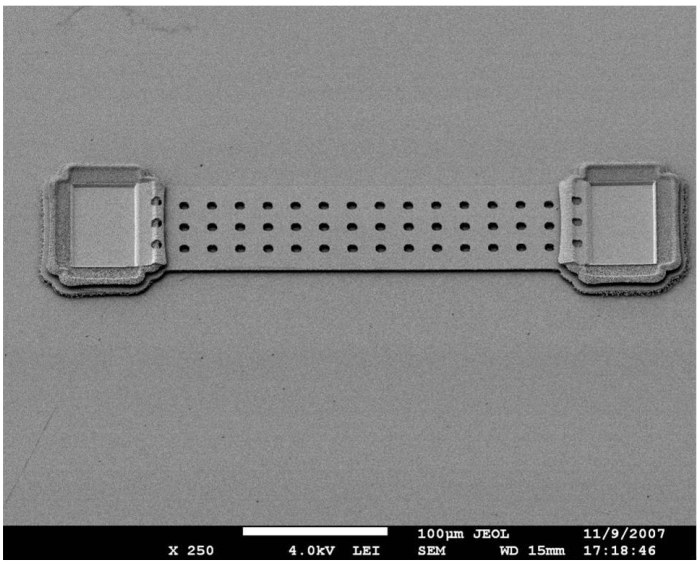
(d) Measured beam height variation of the MEMS test beam from Trial 10 (RD#22).



(c) Measured 3D view optical profiler view of the MEMS test beam from Trial 11 (RD#23).



(d) Measured beam height variation of the MEMS test beam from Trial 11 (RD#23).

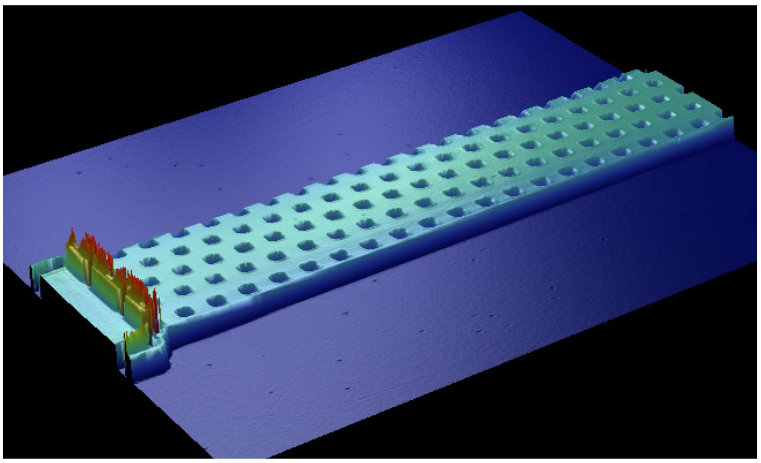


(f) SEM photograph of the MEMS test beam from Trial 11 (RD#23).

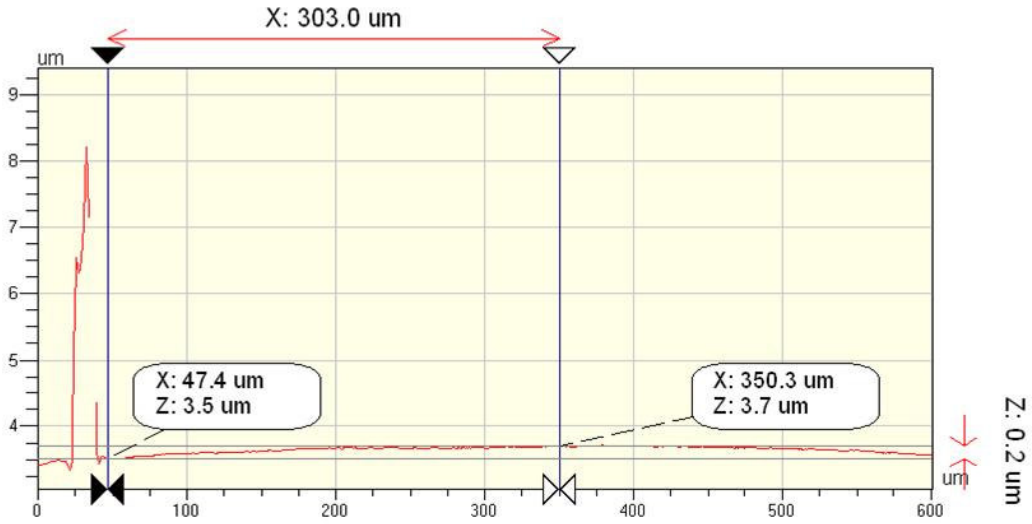
Figure 2.7: The optical profiler measurements and SEM pictures of the MEMS test beams.

Trial 11 also shows good results in other of MEMS structures that have different geometries. Figure 2.8 shows the measured 3D views and the beam shapes of two example structures. The first structure is a 600 µm-long MEMS clamped-clamped beam, and it is buckled by only 0.2 µm throughout the whole beam. The previous fabrication results showed that this beam buckles by about 2 µm downwards. Another example is a beam that is anchored at 4 points on the sides and at 2 points along the beam. This structure is buckled by 0.2 µm at maximum. The previous fabrication results showed that this beam buckles by about 1.8 µm upwards.

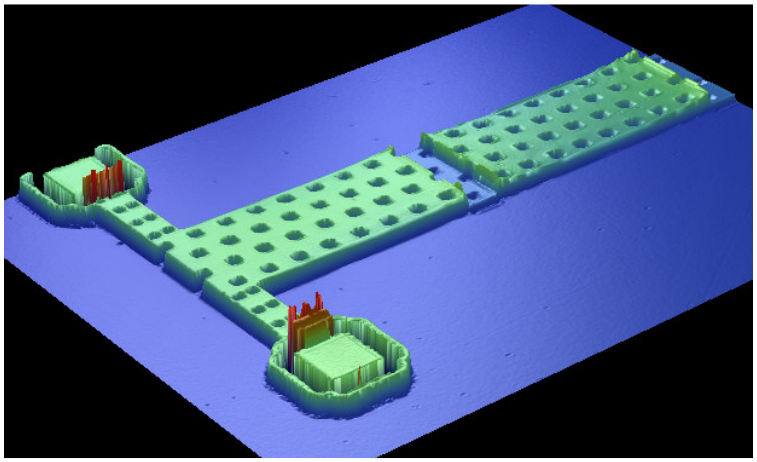
An interesting behavior is observed in the second example structure of Figure 2.8. This structure has 4 small anchors that hold the long beam by means of short cantilevers, and 2 wider anchors along the beam that are intended to prevent the buckling in the previous designs. The shape of this beam given in Figure 2.8-(d) starts with upward buckling, which is the characteristic shape of this structure, and this behavior was observed in the previously fabricated structures. However, the beam changes shape and bends downwards as it approaches the wide anchor. The beam has a similar shape with Figure 2.7-(b) in between the two wide anchors. The two wide anchors are not filled with electroplated Au; they are nominally clamped; so, they are “weak” compared to the ones that are filled with electroplated Au. The center part of the beam tries to get shorter due to tensile residual stress, and it stretches the weak anchors from both sides. This measurement shows that the anchor points or any other discontinuities through the longitudinal direction may totally change the beam shape in equilibrium once these anchors or discontinuities nominally clamped.



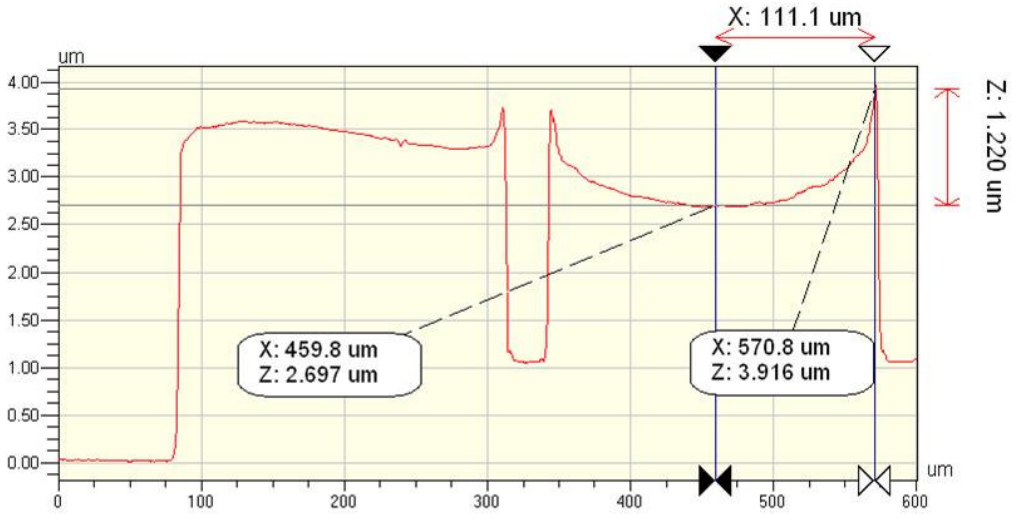
(a) Measured 3D view optical profiler view of a 600 µm-long MEMS beam.



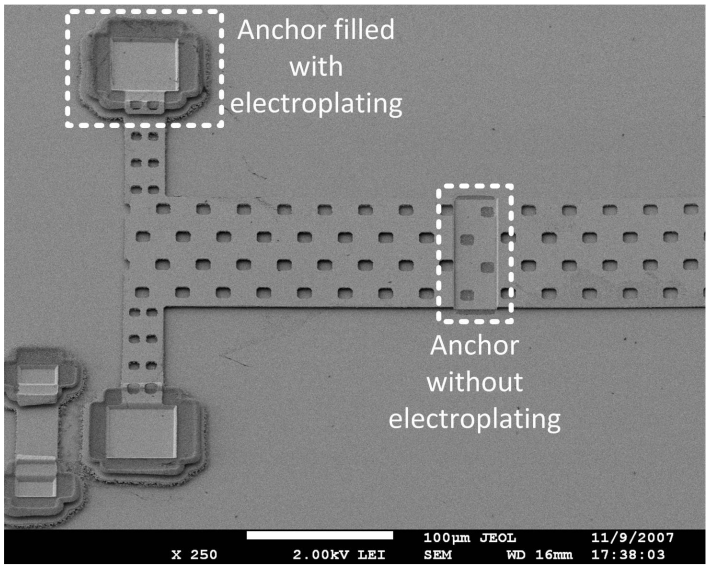
(b) Measured beam height variation of a 600 µm-long MEMS beam.



(c) Measured 3D view optical profiler view of the MEMS structure with 4 + 2 anchors.



(d) Measured beam height variation of the MEMS structure with 4 + 2 anchors.



(e) SEM picture of the MEMS structure with 4 + 2 anchors.

Figure 2.8: The optical profiler measurements and SEM pictures of other MEMS structures.

2.4. Conclusion

This chapter presents the details of the fabrication process, namely METU RF MEMS fabrication process, which is used to implement the RF MEMS structures in the frame of this thesis. The materials used and their deposition methods are introduced, and the process flow is presented. Also, the bottlenecks of the process

are identified, and solutions are proposed. In this frame, the conductivity of the first metal layer is increased up to 3×10^7 S/m by a detailed investigation of the effects of the process parameters. The obtained result is also verified with DC resistivity measurements, and parameters extracted from RF measurements. The residual stress of the structural layer is also minimized, and the possible solutions that prevent the buckling are investigated both theoretically and experimentally. Two solution methods are proposed for this purpose, and a process recipe is developed that result with MEMS test structures without any buckling.

CHAPTER 3

A RECONFIGURABLE RF MEMS TRIPLE STUB IMPEDANCE TUNER FOR 6-20 GHZ APPLICATIONS

3.1. Introduction

One of the applications that use the advantage of realizing reconfigurable circuits with the RF MEMS technology is impedance tuners and impedance matching networks. RF MEMS impedance tuners (IT) and impedance matching networks (IMN) propose a new aspect to some important problems in RF engineering such as noise parameter (NP) measurement, load-pull analysis, low-noise amplifier (LNA) and power amplifier (PA) matching, and antenna matching.

ITs and IMNs are generally implemented by transmission line based structures such as single stub, double stub, triple stub [172], and double slug [174] topologies at microwave and millimeter-wave frequencies. The idea of reconfigurable RF MEMS ITs and IMNs is to change the electrical lengths of the transmission lines in these structures by means of RF MEMS switches or RF MEMS varactors so that the tuned or matched impedances can be adjusted [67]-[78]. The use of RF MEMS components in the design of ITs or IMNs is due to the fact that these components have very low-loss with respect to their rivals. In this case, it becomes possible to implement structures by cascading a number of RF MEMS components, which brings an unaffordable amount of loss in case of using other microwave components. As a result, reconfigurable ITs or IMNs can be designed that have a

high number of RF MEMS components, which results with a high number of impedance states or wide impedance coverage.

The aim in this part of the thesis is to design and implement a universal tuner that can cover the whole Smith Chart in an ultra-wide band. The following subsections of this chapter explain the details of the design, the fabrication, and the measurement results of the triple stub RF MEMS impedance tuner.

3.2. RF MEMS Impedance Tuner Design

Figure 3.1 shows the block diagram of the impedance tuner (IT). The tuner is composed of three adjustable stubs, two interconnection lines, and three T-junctions that are used to connect the stubs to the interconnection lines. The electrical lengths of the stubs are adjusted by means of RF MEMS switches.

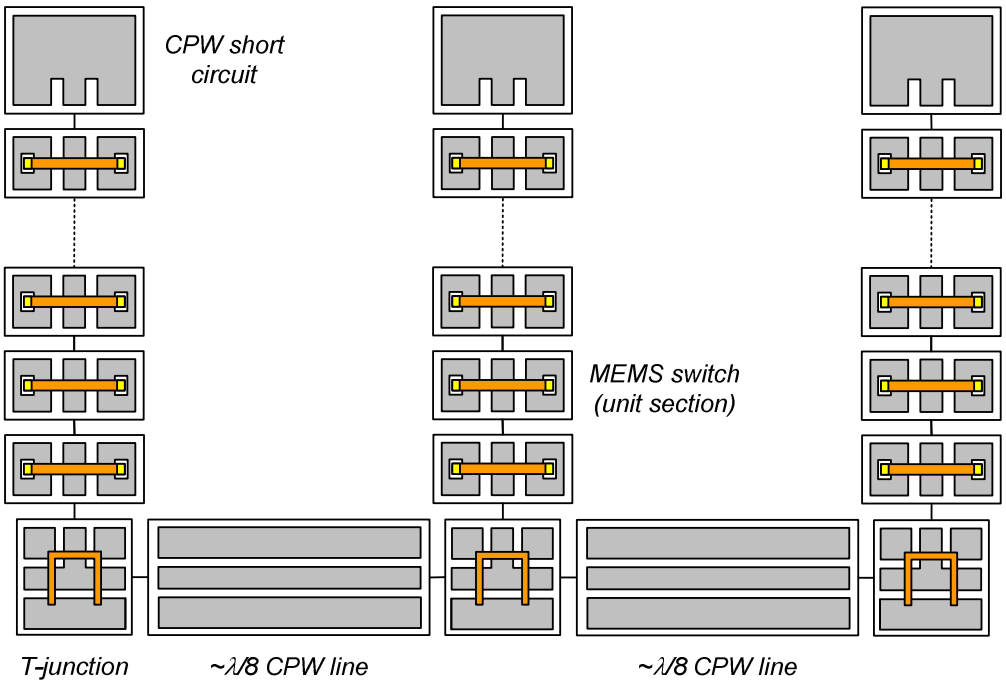


Figure 3.1: The block diagram of the triple stub impedance tuner.

The triple stub topology has been selected for the impedance tuner since the entire Smith Chart can be covered theoretically as the impedance range using this topology. Coplanar waveguides (CPW) are used as the transmission lines of the IT since both the signal and the ground lines are on the same plane. In this case, it is easy to implement shunt RF MEMS switches, and thru wafer via are not necessary. The CPW interconnection lines between the stubs have an electrical length of approximately $\lambda_g/8$ which was chosen in order to obtain uniform impedance distribution on the Smith Chart.

The center design frequency is selected as 18 GHz. The aim of the design is to cover the whole Smith Chart by a maximum number of impedance combinations at the center design frequency; in addition to that, the design is also targeted to cover as much area as possible on the Smith Chart in an ultra-wide frequency band. For this purpose, 10 RF MEMS switches have been uniformly placed on each stub so that there are $11^3 = 1331$ impedance states to cover the whole Smith Chart. All the three stubs are identical, and the electrical lengths of the stubs are greater than $\lambda/2$ at 18 GHz. Having a stub electrical length greater than $\lambda/2$ is necessary to be able to provide susceptances theoretically in $(-\infty, +\infty)$ range, which is required to reach each impedance value on the Smith Chart. However, since the positions of the RF MEMS switches are fixed, the $\lambda/2$ length is divided into 10 discrete steps, and the design targeted to cover the Smith Chart uniformly with discrete impedance points.

3.2.1. RF MEMS Switch (Unit Section) Design

The working principle of the reconfigurable triple stub IT in this thesis is to change the lengths of the stubs by actuating the RF MEMS switch closest to the required stub lengths. In this way, short or open circuited terminations can be obtained with discrete separations, and for this purpose, capacitive shunt RF MEMS switches are used. Because there are 10 RF MEMS switches on a stub and each of them must be

actuated independently, a standard capacitive, shunt RF MEMS switch, where the actuation signal is applied between the CPW signal and the CPW grounds, cannot be used. Hence, a special switch design is necessary, which has capacitive coupling from MEMS bridge to CPW ground. The 3D and the top views of the designed RF MEMS switch can be seen in Figure 3.2.

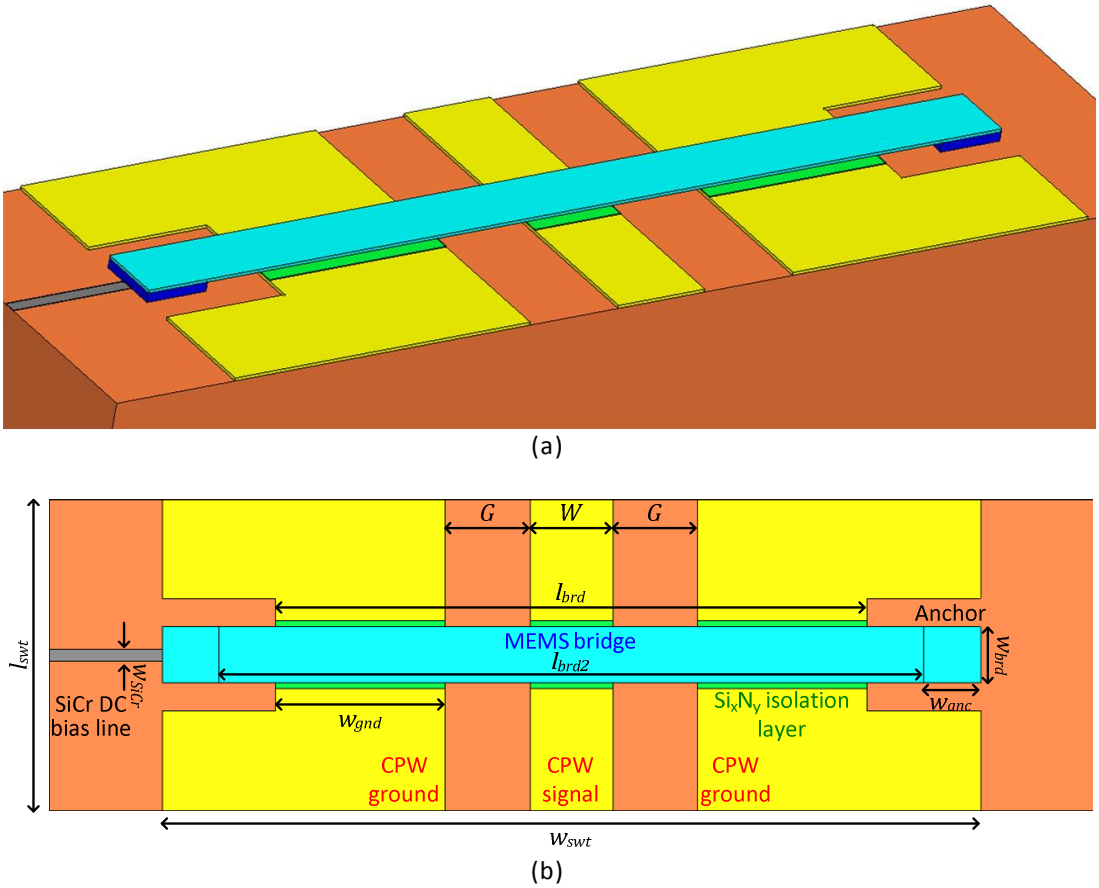


Figure 3.2: (a) 3D view of the RF MEMS switch of the triple stub IT (z-dimension exaggerated) (b) Top view of the RF MEMS switch of the triple stub IT.

The MEMS switch is designed first in Microwave Office v6.5 (MWO) [175] using the circuit model given in Figure 3.3. In the circuit model, all the capacitances have two states. C_{sbu} and C_{sbd} stand for the capacitance between the signal line of the CPW and the MEMS bridge for upstate and downstate, respectively, and C_{bgu} and C_{bgd} stand for the capacitance between the MEMS bridge and the ground of the CPW for upstate and downstate, respectively. In this step of the design, the design goal is to obtain such a switch design that the 1331 impedance states of the designed IT is distributed uniformly on the Smith Chart.

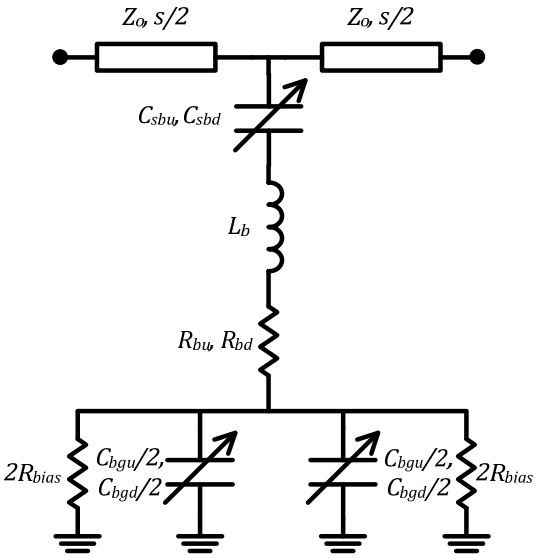


Figure 3.3: The circuit model of the MEMS switch that is used for the design of the triple stub IT.

The most critical parameters for the design are the characteristic impedance of the unloaded line, Z_o, the periodicity, s, and the upstate and downstate capacitances, C_{sbu}, C_{sbd}, C_{bgu} and C_{bgd}. The upstate capacitances are calculated from the physical dimensions using [177]:

$$C_{sbu} = \varepsilon_0 \left[1.15 \frac{W w_{brd}}{h_{equ}} + 2.8(W + w_{brd}) \left(\frac{t}{h_{equ}} \right)^{0.222} + 4.12 h_{equ} \left(\frac{t}{h_{equ}} \right)^{0.728} \right] \quad (3.1)$$

$$C_{bgu} = \varepsilon_0 \left[1.15 \frac{w_{gnd} w_{brd}}{h_{equ}} + 2.8(w_{gnd} + w_{brd}) \left(\frac{t}{h_{equ}} \right)^{0.222} + 4.12 h_{equ} \left(\frac{t}{h_{equ}} \right)^{0.728} \right] \quad (3.2)$$

$$h_{equ} = g + \frac{t_d}{\varepsilon_r} \quad (3.3)$$

where t stands for the first metal layer thickness, t_d stands for the dielectric layer thickness, ε_0 is the free-space permittivity, and ε_r is the relative dielectric constant. The above formulation includes the effects of the fringe capacitances, and it is successful in guessing the capacitance of the MEMS switch generally with less than 10% error when compared to the capacitance that are extracted from full wave EM simulations. So, this formula is very handy for having a good starting point for the design. The downstate capacitances are calculated using:

$$C_{sbd} = \varepsilon_r \varepsilon_0 \frac{W w_{brd}}{t_d} \quad (3.4)$$

$$C_{bgd} = \varepsilon_r \varepsilon_0 \frac{w_{gnd} w_{brd}}{t_d} \quad (3.5)$$

The selection of CPW dimensions is important on the design in several ways. First, the total ground-to-ground spacing should be less than:

$$W + 2G < \frac{c}{8 f_0 \sqrt{\varepsilon_{r,subs}}} \quad (3.6)$$

where $\varepsilon_{r,subs}$ is the relative dielectric constant of the substrate and f_o is the maximum operation frequency, in order to minimize radiation losses [22]. The total ground-to-ground spacing is selected as high as possible in order to reduce the unloaded CPW line losses. Having minimum unloaded CPW line loss is another

criteria, and it occurs when W is selected as equal to G, in which case the unloaded line Z_o becomes around 95 Ω. Also, the center conductor dimension, W, is directly effective on the capacitances in both upstate and downstate, and the actuation voltage of the RF MEMS switch. Considering the design requirements and all the criteria pointed out above, a set of circuit model parameters and their corresponding physical dimensions are determined.

Once the circuit model parameters of the switch are found, the switch is simulated and optimized by tuning the physical dimensions in the full-wave EM simulation environment, which is HFSS v9.2 [176]. The final dimensions of the RF MEMS switch design are given in Table 3.1. The comparison of the HFSS simulations of the RF MEMS switch with that of the circuit model simulations are given in Figure 3.4. The figures show that the HFSS simulations can successfully be modeled with the circuit model. The circuit model parameters that are extracted from the HFSS simulations are given in Table 3.2.

Table 3.1: The physical design parameters of the RF MEMS switch.

Parameter	Value
w_{swt}	550 µm
l_{swt}	1446 µm
W	146 µm
G	150 µm
l_{brd}	1046 µm
l_{brd2}	1246 µm
w_{brd}	100 µm
w_{anc}	100 µm
w_{gnd}	300 µm
w_{SiCr}	20 µm

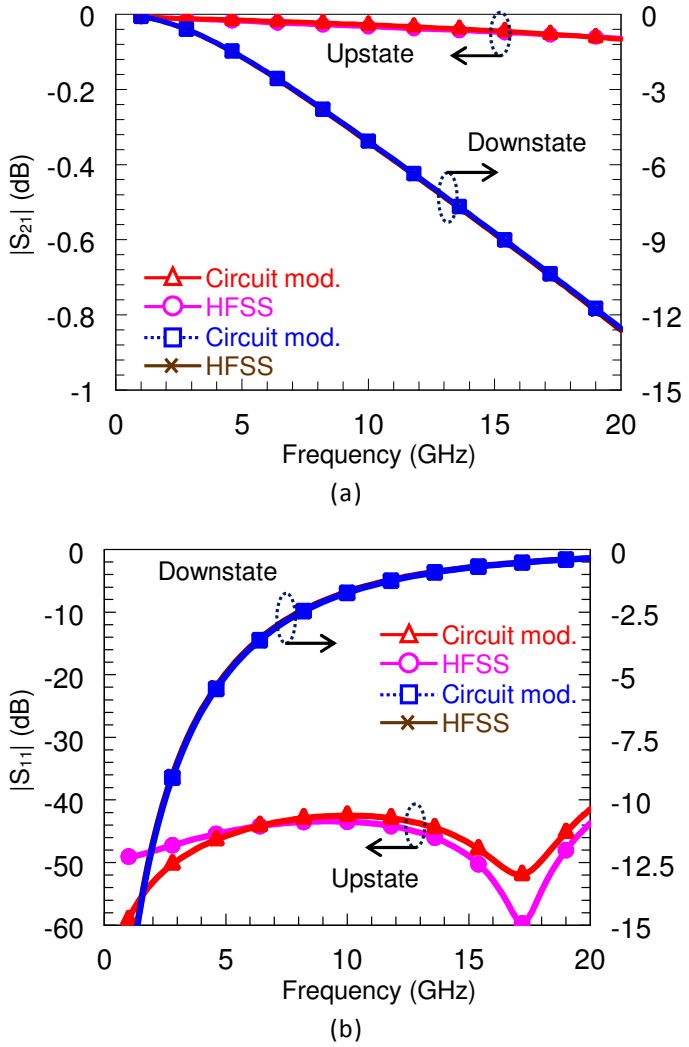


Figure 3.4: The comparison of HFSS simulations with that of the circuit model of the RF MEMS switch that is used for the design of the triple stub IT.

Table 3.2: The circuit design parameters of the RF MEMS switch design.

Circuit Model Parameters Extracted from HFSS			
Z_o	97.5 Ω	C_{sbd}	1.15 pF
$\varepsilon_{r,eff}$	2.32	C_{bgd}	4.73 pF
α	33 dB/m @20 GHz	L_b	18.3 pH
s	550 µm	R_{bu}/R_{bd}	2 / 0.18 Ω
C_{sbu}	91.2 fF	C_U/C_D	74.2 fF/ 926.3 fF
C_{bgu}	370 fF	R_{bias}	4000 Ω
Interconnection line parameters			
Z_o = 53.5 Ω, $\varepsilon_{r,eff}$ = 2.375, α = 71 dB/m, l = 994 µm			

For the HFSS simulations, the relative dielectric constant of the silicon nitride dielectric layer is used as $0.37 \times 7 = 2.59$. This change is made in order to include the degradation in the down state capacitance of the RF MEMS switches. From the previous measurement experience, it was observed that the extracted capacitance values are about 37% of the ideal parallel plate capacitance values. The decrease in the downstate capacitance is due to the surface roughness of the isolation layer and first metal layer, and insufficient contact force. This amount of degradation is not only observed in the METU RF MEMS fabrication process, and it is close to the ones that are observed in the literature ([34], [37]).

3.2.2. T-Junction Design

The T-junctions are quite important for the performance of the triple stub impedance tuner, and they should be designed carefully. Otherwise, the junction point adds additional inductance and capacitance that affect the lengths of the stubs and the CPW lines between the stubs. Suspended air bridges were used on all ports of the junction to prevent unwanted modes. The signal line of the CPW lines were narrowed to cancel the capacitance of the air bridges; and hence, to improve matching at the junction point. The T-junction was designed using Microwave Office v6.5 (MWO) [175] EM simulator and the designs were verified with HFSS v9.2 [176]. A more detailed analysis will be presented in Chapter 5.2.1. The top view of the designed T-junction can be seen in Figure 3.5, and its dimensions are given in Table 3.3.

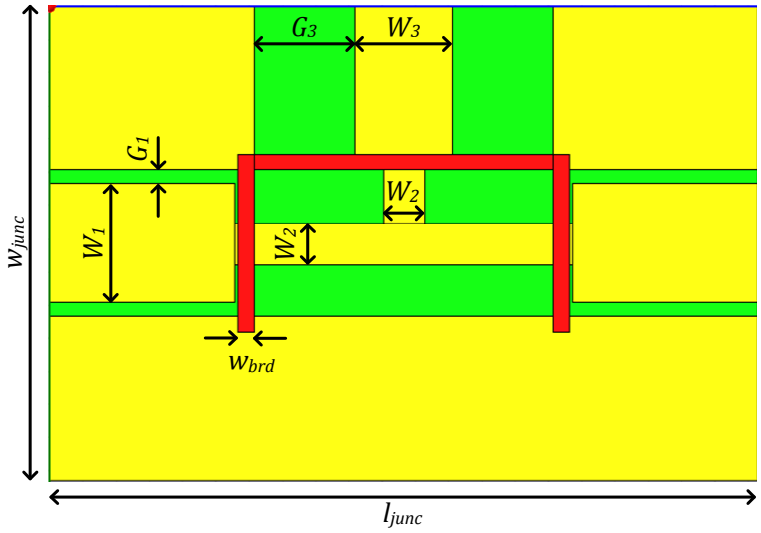


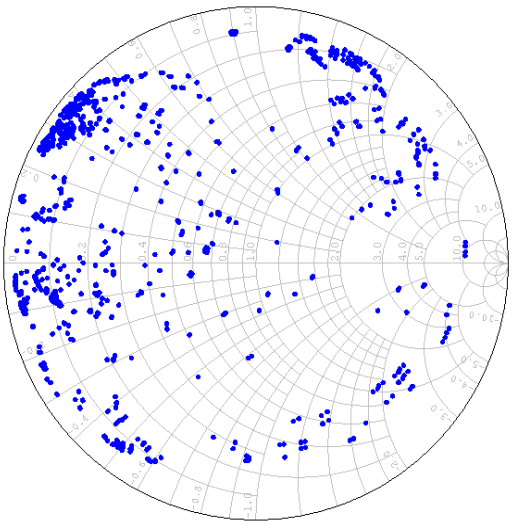
Figure 3.5: The layout of the T-junction that is used in the design of the triple stub IT.

Table 3.3: The physical design parameters of the T-junction design.

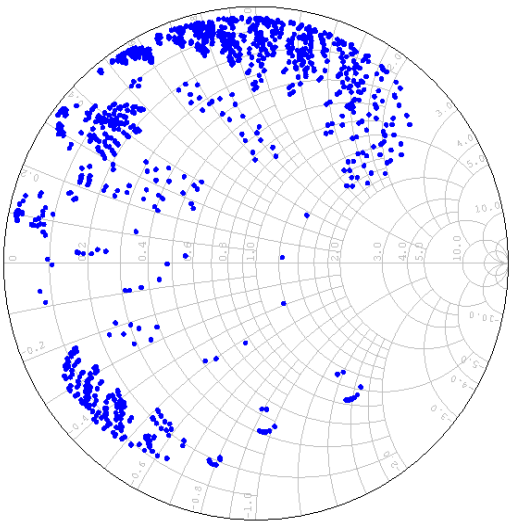
Parameter	Value
W_1	178 µm
G_1	21 µm
W_2	62 µm
W_3	146 µm
G_3	150 µm
l_{junc}	1064 µm
w_{junc}	714 µm
w_{brd}	24 µm

3.2.3. The Simulations of the Triple Stub Impedance Tuner

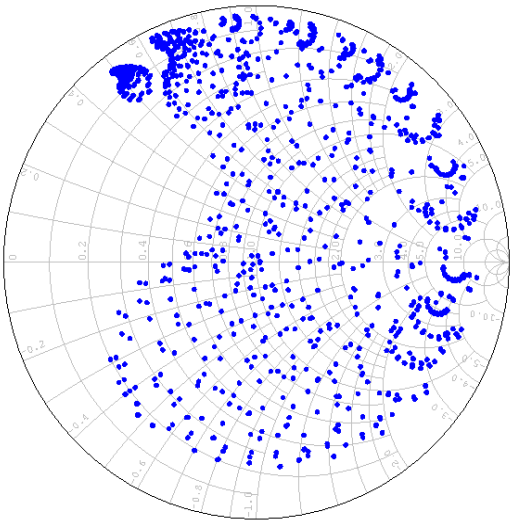
The simulations of the RF MEMS triple stub IT is made using MWO v6.5. The S-parameters of the RF MEMS switches, T-junctions, and CPW interconnection lines are cascaded, and the overall performance of the IT is investigated. The Smith Chart coverage of the designed IT for 6-20 GHz band is given in Figure 3.6. Each figure includes 11^3 impedance states. The center frequency of the design is 18 GHz. The area of the final IT design measures 8.6×8.6 mm^2. The interconnection line CPW parameters are Z_o = 53.5 Ω, $\varepsilon_{r,eff}$ = 2.375, α = 71 dB/m, and l = 994 µm.



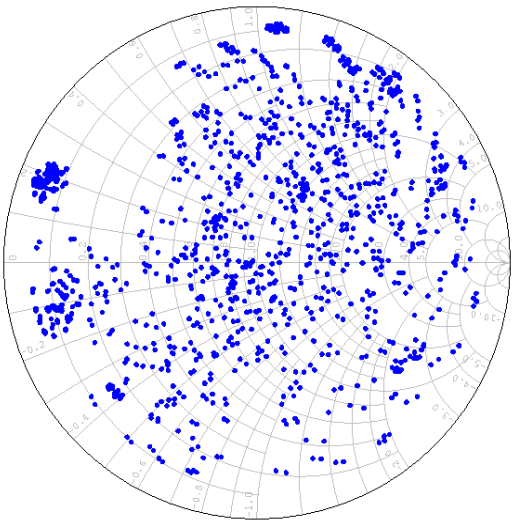
(a) 6 GHz



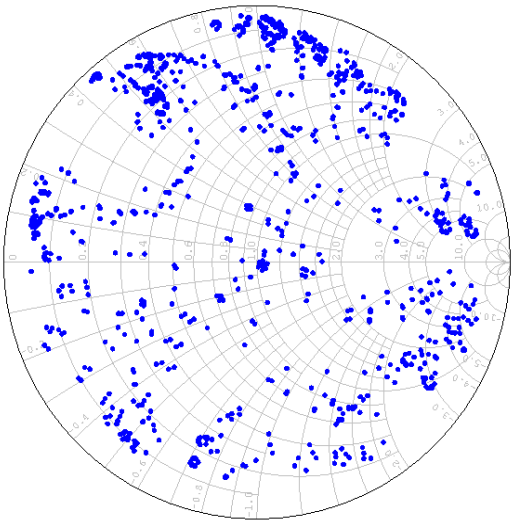
(b) 8 GHz



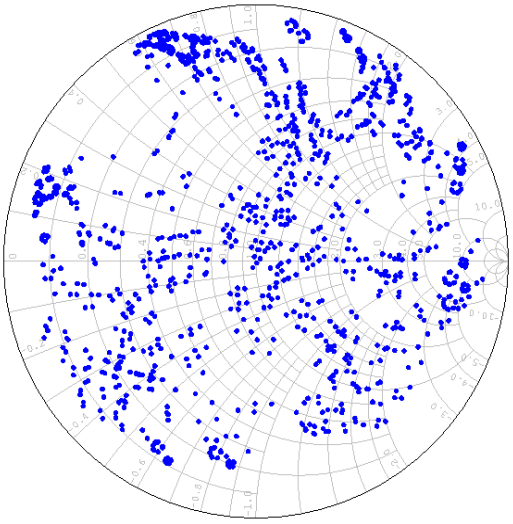
(c) 10 GHz



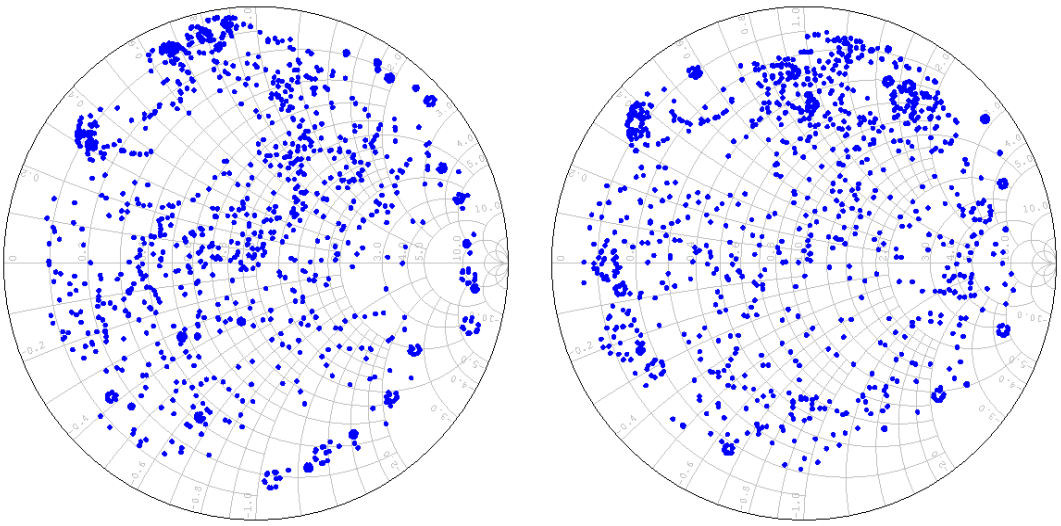
(d) 12 GHz



(c) 14 GHz



(d) 16 GHz



(e) 18 GHz (f) 20 GHz

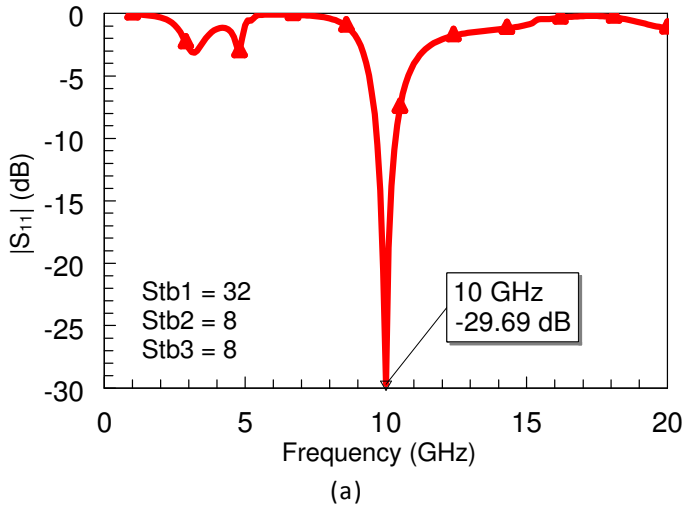
Figure 3.6: The Smith Chart coverage of the designed IT in 6-20 GHz band for 1331 impedance points.

The above figures show that the design is successful in covering almost entire Smith Chart in 6-20 GHz band. 20 GHz is actually not a limit for the operation of the design; however, due to the limitations in the measurement setup, the design and modeling is limited to this frequency.

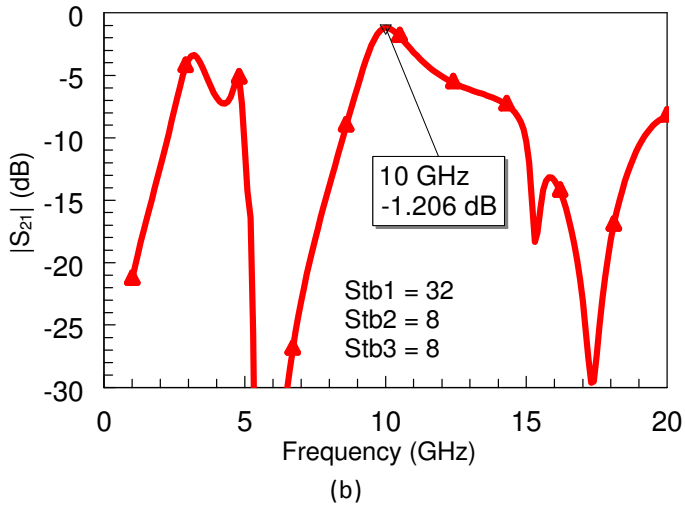
3.2.4. Case Studies

To demonstrate the operation of the IT, some sample impedance transformations are presented. Figure 3.7 shows the performance of the IT when it is adjusted to transform 50 Ω to 250 Ω at 10 GHz. Here, the reference impedance of the first port is 250 Ω, and S_{11} is defined with respect to this port. The insertion loss of the IT for this transformation case is -1.2 dB. The loss performance of the IT is also given for this impedance state in Figure 3.7-(c), where the loss of the IT is defined as:

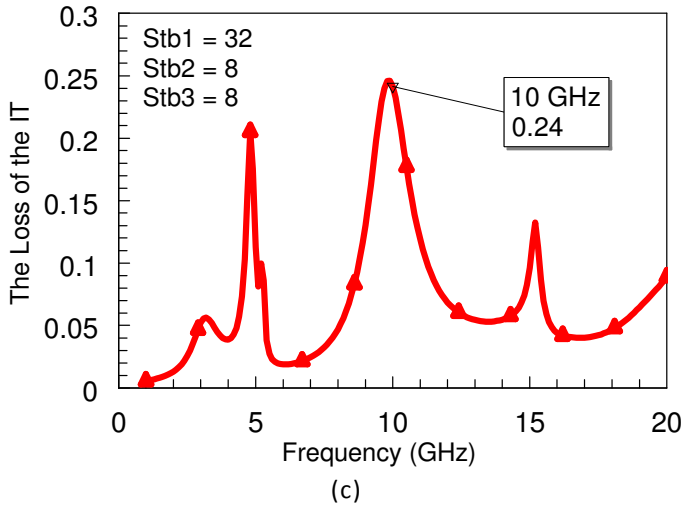
$$L = 1 - |S_{11}|^2 - |S_{21}|^2 \tag{3.7}$$



(a)



(b)



(c)

Figure 3.7: The performance of the triple stub IT for 50 Ω-to-250 Ω impedance transformation at 10 GHz (a) $|S_{11}|$ (b) $|S_{21}|$(c) The loss of the tuner at this state.

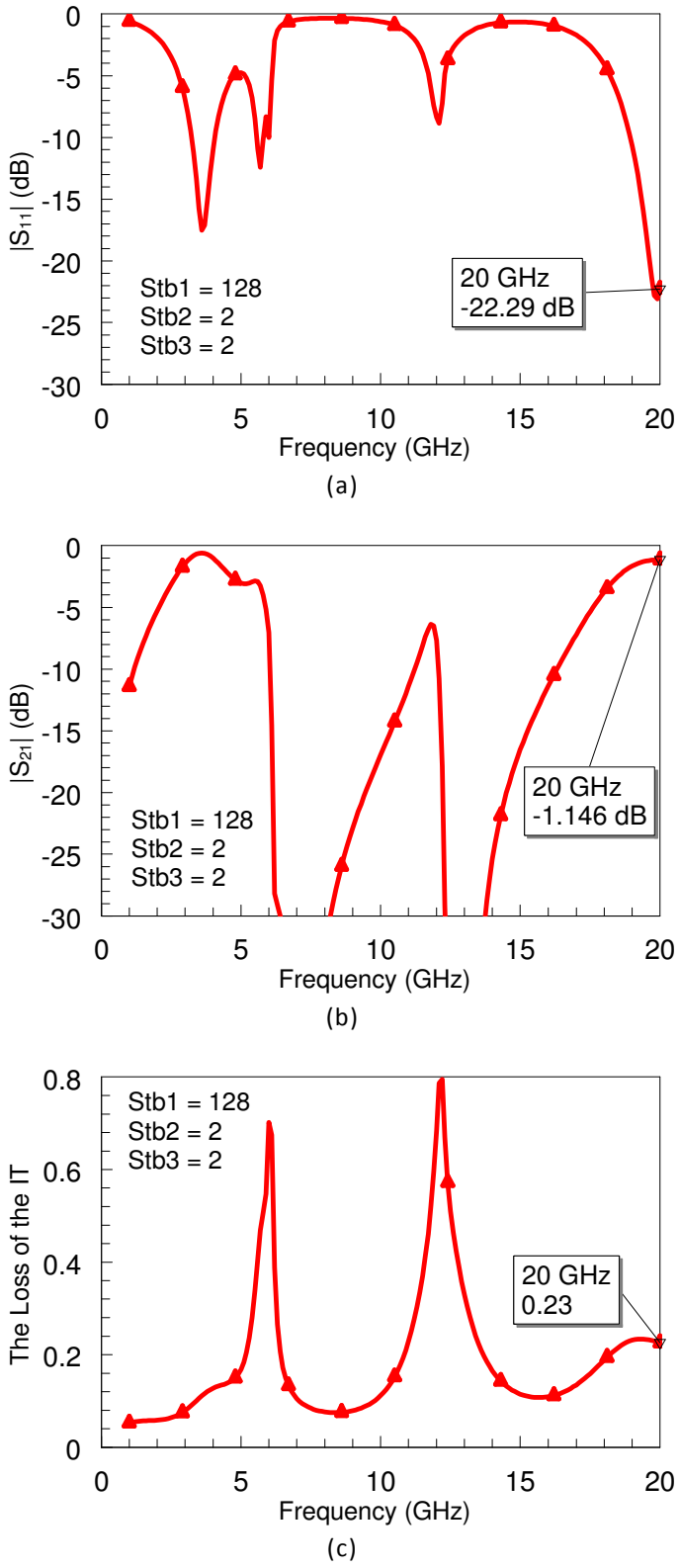


Figure 3.8: The performance of the triple stub IT for 50 Ω-to-20 Ω impedance transformation at 20 GHz (a) $|S_{11}|$ (b) $|S_{21}|$(c) The loss of the tuner at this state.

Another example is presented in Figure 3.8, where the IT is adjusted to transform 50 Ω to 20 Ω at 20 GHz. The insertion loss in this case is again -1.2 dB. The stub state numbers in the figures of the decimal equivalent of the states of the switches in each stub. For example, Stb1 = 32 means Stb1 = 0000100000, which means that the sixth switch on stub1 is in the downstate.

3.3. The Fabrication and the Measurement Results

The triple stub RF MEMS impedance tuner is implemented using the METU RF MEMS fabrication process, which was explained in Chapter 2 in detail. 350 µm-thick, 4" quartz substrates were used in the fabrication. The tangent loss of the substrate is $tan\ \delta = 0.001$ in all the band of interest. The photographs and the SEM pictures of the fabricated RF MEMS IT are given in Figure 3.9 and Figure 3.10, respectively.

3.3.1. The Packaging of the Impedance Tuner

The RF MEMS impedance tuner needs to be packaged before they are measured as there are many DC connections for the biasing of the RF MEMS switches. For this purpose, ceramic IC packages are used. The area of the triple stub IT measures 8.6×8.6 mm^2, so it was hard to find a package with this window size. Two different packages are selected for the IT from Spectrum-Semi Company, which are 24-pin, alumina based package (HYB02413) with a window of 10.9 x 26.7 mm^2 and 40-pin, ceramic based package (CSB04046) with a window of 8.9 x 11.4 mm^2. The IT is first fastened on the package by using white epoxy, and then the pads are connected to the package by aluminum wire bonds. Figure 3.11 shows the photographs of the packaged RF MEMS IT, which is placed on the daughter board for the measurements. The bonding diagram of the IT for HYB02413 alumina package is given in Figure 3.12.

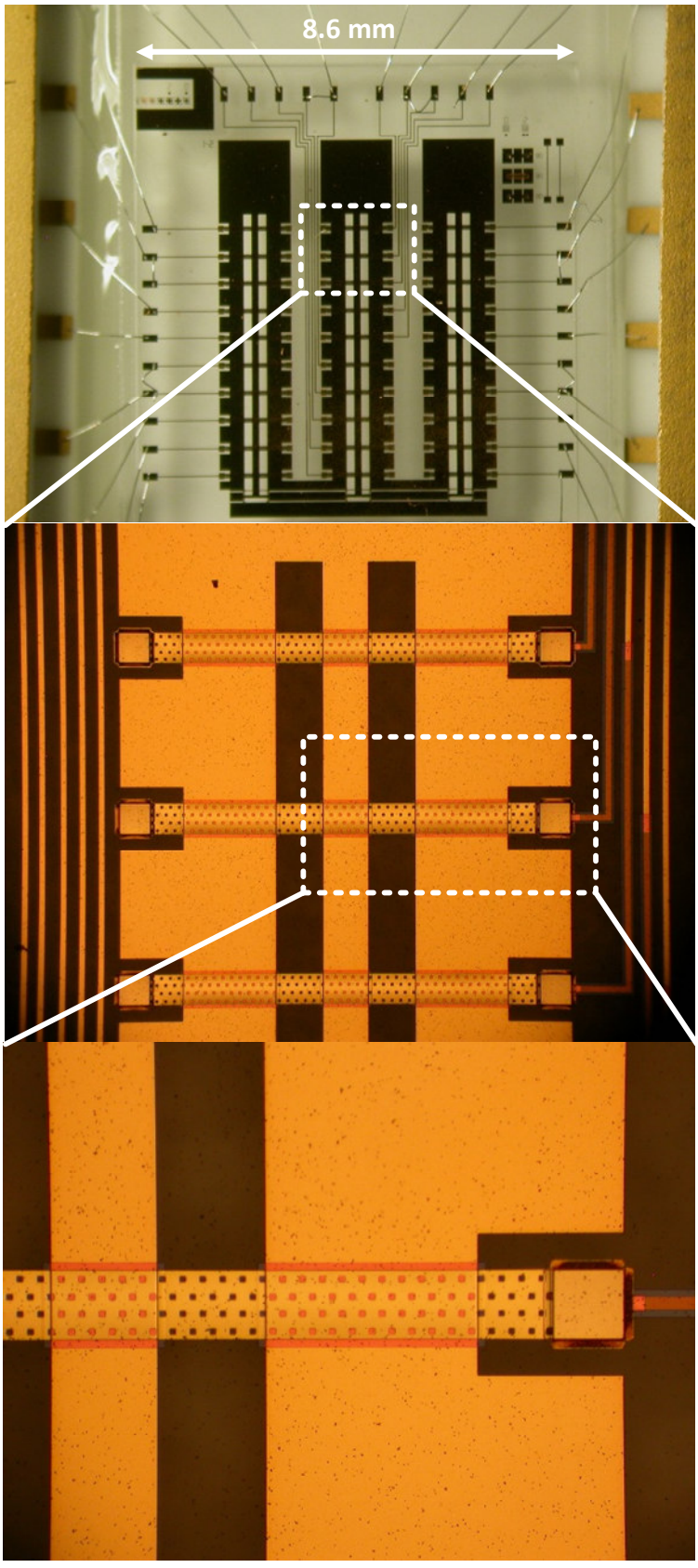
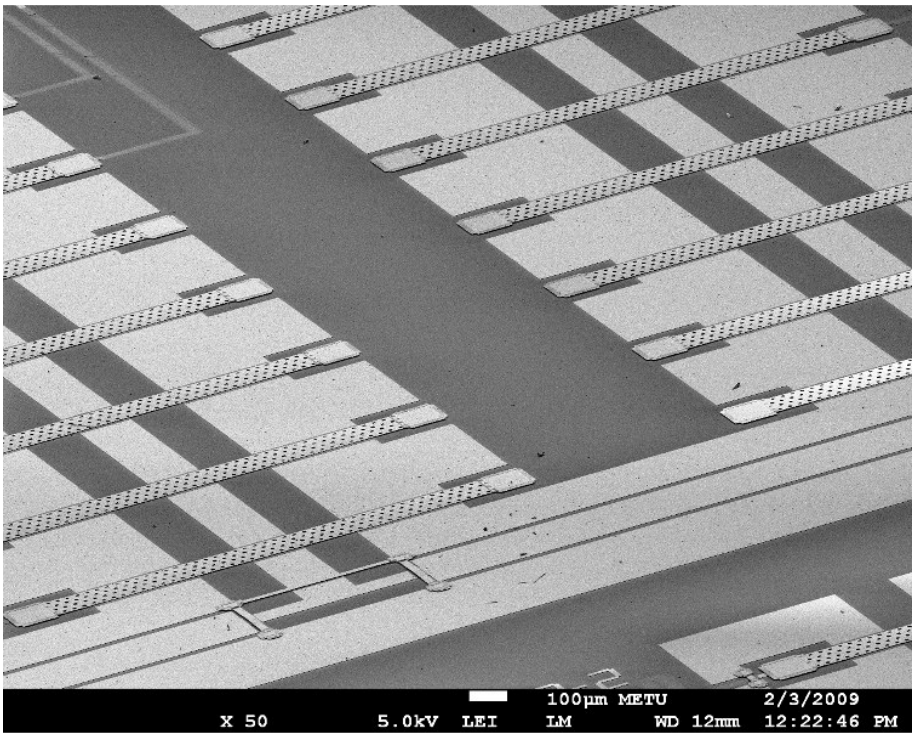
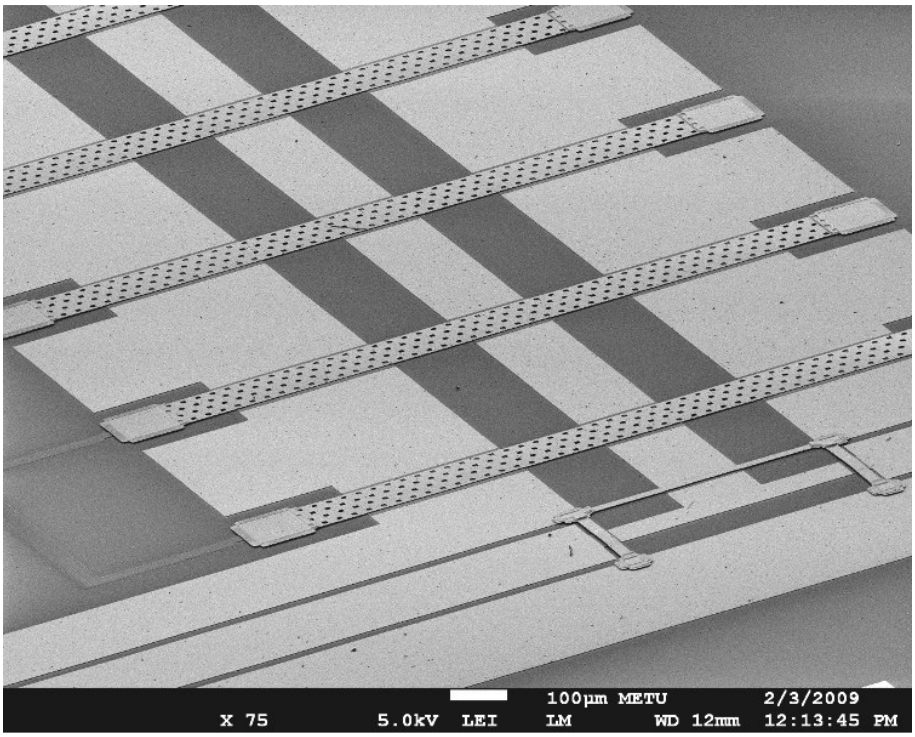


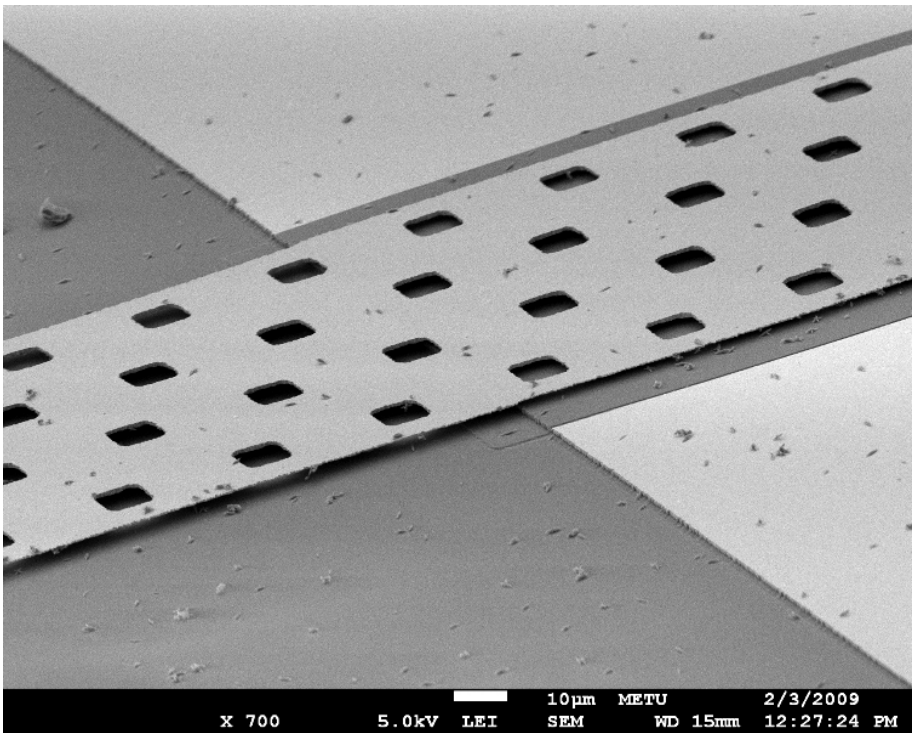
Figure 3.9: The photographs of the fabricated IT.



(a) Wide view of two of the stubs and the T-junction.

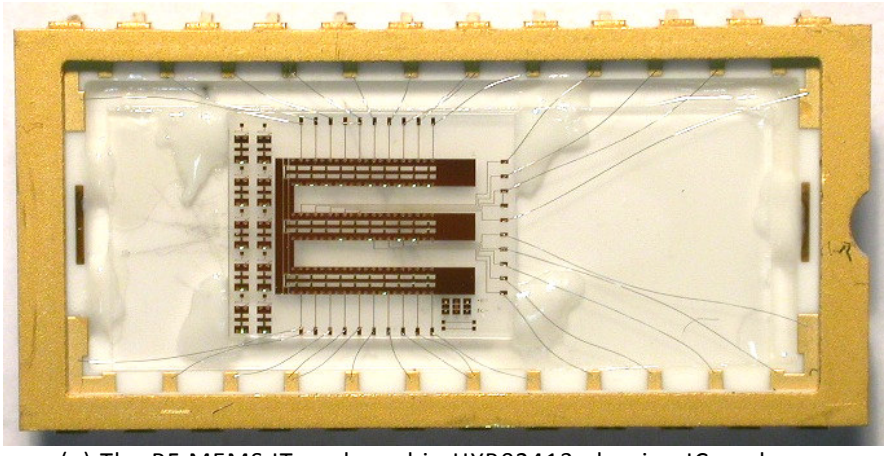


(b) The closer view of one of the stubs.

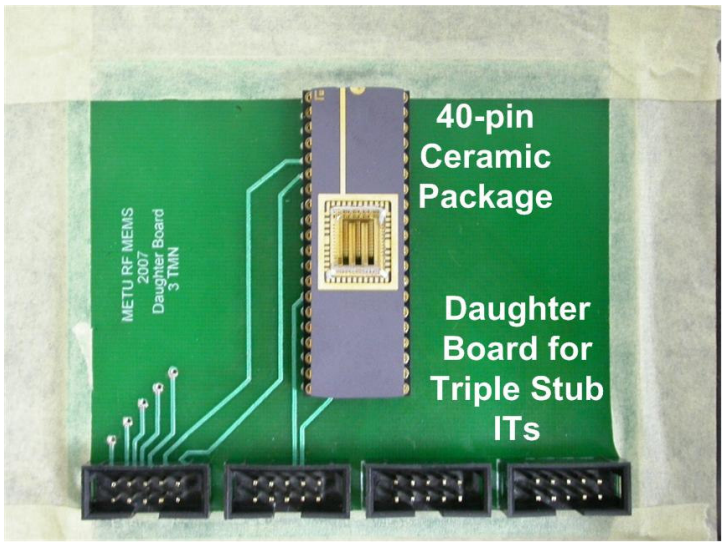


(c) The closer view of the MEMS switch.

Figure 3.10: The SEM pictures of the fabricated RF MEMS IT.



(a) The RF MEMS IT packaged in HYB02413 alumina IC package.



(b) The RF MEMS IT packaged in CSB04046 ceramic IC package and placed on the daughter board.

Figure 3.11: The photographs of the packaged RF MEMS IT.

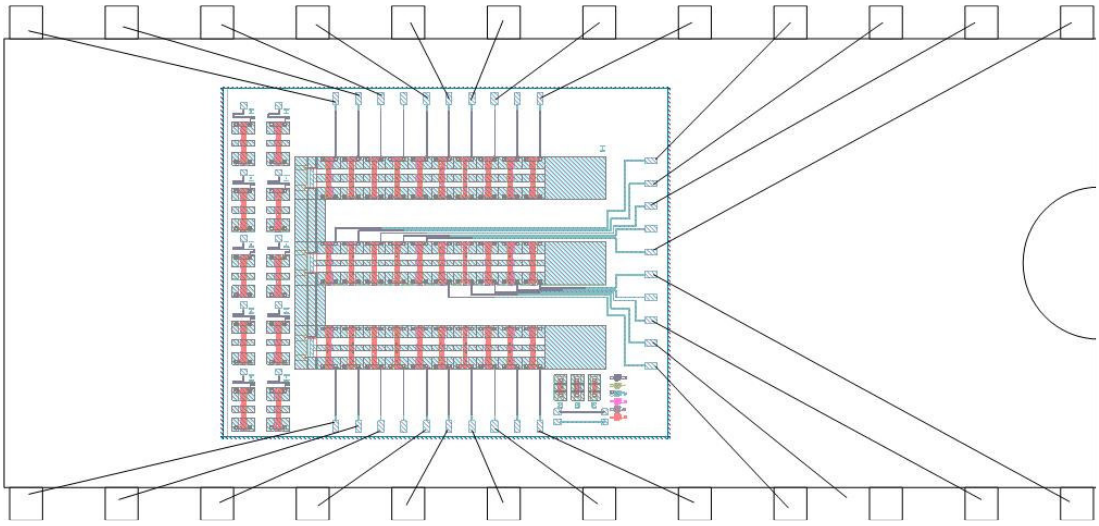


Figure 3.12: The bonding diagram of the RF MEMS IT for HYB02413 package.

3.3.2. The Design and the Implementation of the Multi-Pin MEMS Automated Measurement Setup (MAMS)

An automated measurement setup is needed for the measurements of the fabricated impedance tuner since there are 30 control pins, and all of the pins

should be controlled simultaneously. This is necessary for the measurement of all possible states of the impedance tuner, which has more than 1000 possible states. For this purpose, an automated measurement setup is designed and implemented. Figure 3.13 shows the block diagram of the setup. The setup consists of six main parts, which are;

i) the network analyzer to measure the S-parameters (Agilent E8361A),
ii) the probe station to contact the MEMS device (Summit 9000),
iii) the MEMS biasing waveform generator card to produce the biasing waveform,
iv) the biasing waveform distribution card to direct the biasing waveform to the MEMS switches on the correct time and order,
v) the computer controlled DC supply to bias the distribution card (HP 3631A),
vi) and the computer to control the network analyzer, DC supply, and save the data.

The most important parts of the setup are the "MEMS Biasing Waveform Generator Card[1]" and the "Biasing Distribution System[2]". The generator card is used to produce the waveform that is applied to the MEMS switches as the actuation voltage. With this generator card, it is possible to produce a number of different waveforms, which can be seen in Figure 3.14. For the all of the waveforms, the important parameter is not the voltage levels or the frequency of the waveform, but it is the transition time between the states. The transition time between any states of the waveform must be short enough that the RF MEMS switch should stay in down state. Since the rise or fall time of the MEMS switches are around a few microseconds, a transition time that is less than 1 μs should be enough.

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[1] The MEMS Biasing Waveform Generator Card is designed and the implemented by Halil İbrahim Atasoy.
[2] The Biasing Distribution System is designed and the implemented by Halil İbrahim Atasoy, the author has accompanied him during most of the steps.

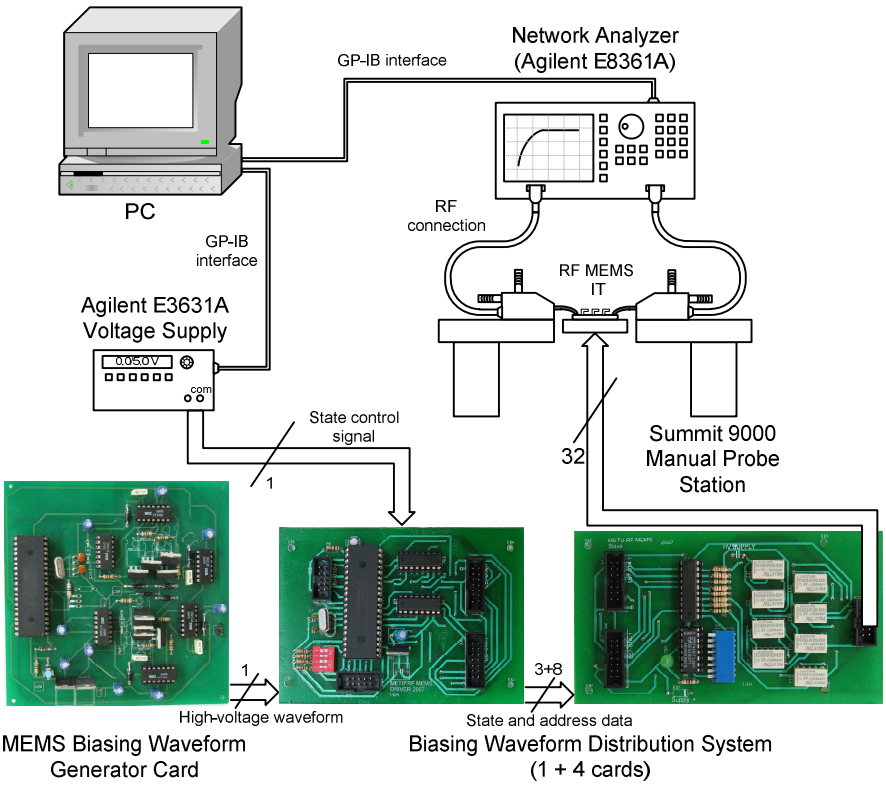


Figure 3.13: The block diagram of the multi-pin MEMS automated measurement setup.

The generator card is designed to produce different types of waveforms, which are unipolar, bilevel unipolar, bipolar, and bilevel bipolar waveforms. There are two types of bipolar waveforms for the actuation of the RF MEMS switches. In the first one, the actuation voltage is applied in different polarities in two consecutive actuations. In the second one, the actuation voltage is applied in positive and negative polarities and switching between them very quickly so that the switch cannot respond in a single actuation. By this method, the dielectric charging can be reduced. The bilevel bipolar waveform has two levels, which are the actuation and hold down voltages. In this waveform, first, the actuation voltage is applied in both polarities and the switch is pulled down, and then, the hold down voltage is applied in both polarities continuously to hold the switch in downstate. Since the hold down voltage is less than the actuation voltage, the dielectric charging can be reduced further.

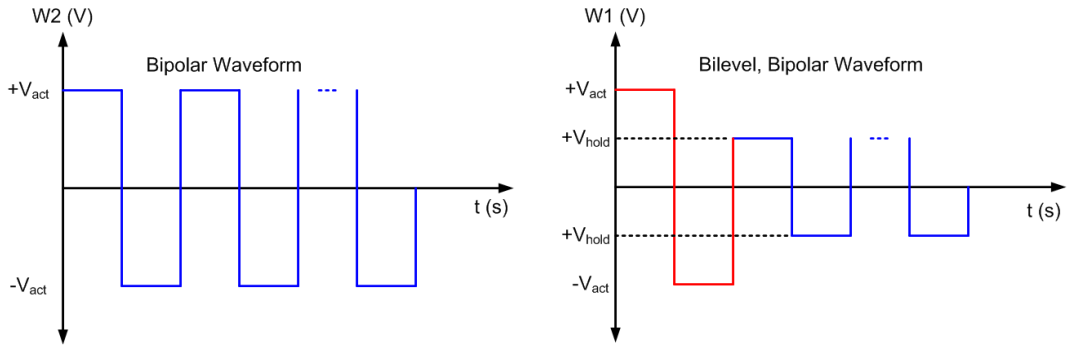


Figure 3.14: Some of the possible waveforms that can be produced by the "Waveform Generator Card".

Figure 3.15 shows the generator card photograph and the card block diagram. The card consists of 8 high voltage and high speed transistors (IRF 630), standard (IR 2113) and optocoupled (not shown in the figure) gate drivers for biasing the transistors, and a microcontroller (PIC 16F877) that organizes the time and duration of on/off states of the transistors. Figure 3.16 demonstrates the schematic of the generator card. There are 8 high voltage transistors in the circuit, which are grouped in 4, and they are driven by 4 gate driver ICs. The color coding of the transistors in Figure 3.16 shows which gate driver are connected to which transistor. The red transistors in the figure are driven by optocoupled gate drivers because of practical reasons.

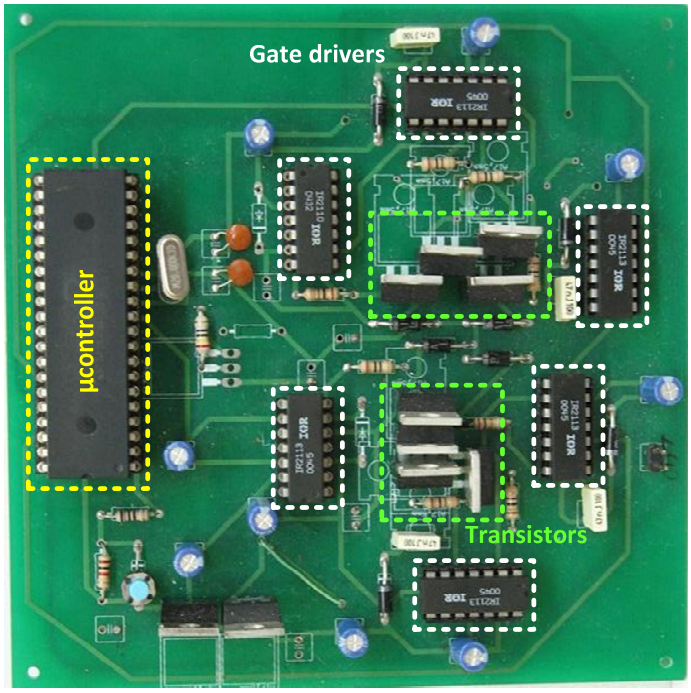


Figure 3.15: The photograph of the waveform generator card and its block diagram.

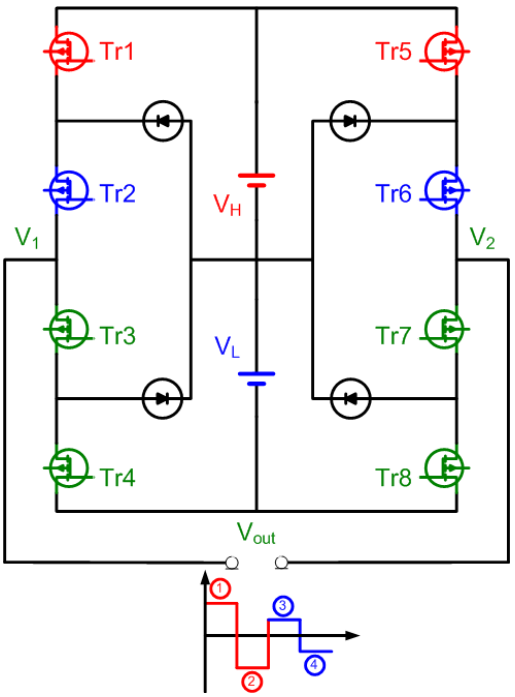
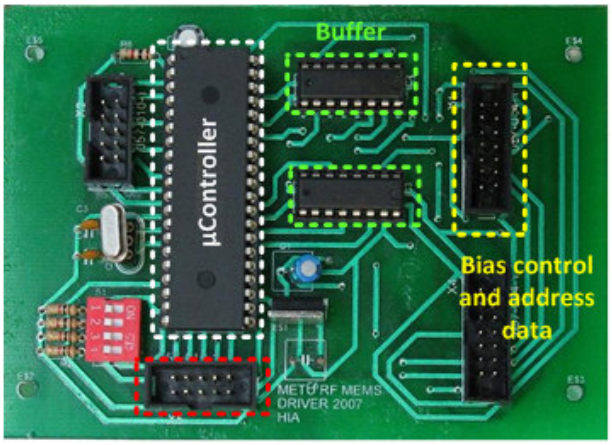


Figure 3.16: The basic schematic of the waveform generator card.

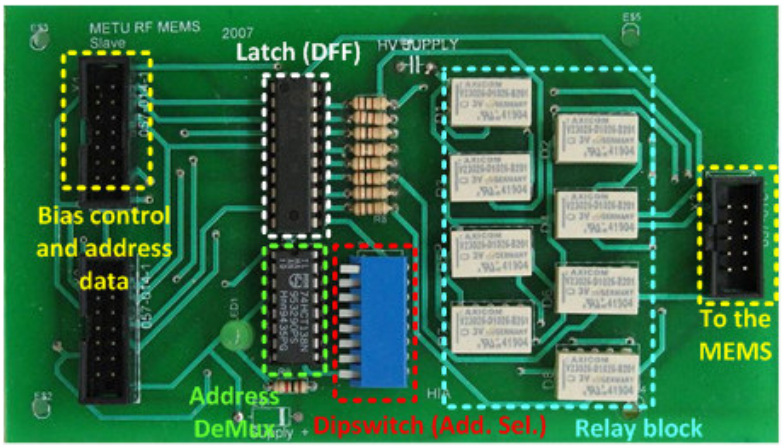
The generator card works differentially by between the outputs of the two arms, which are composed of 4 transistors. The card operates as follows:

- State 1: Tr1 and Tr2 are open on V_1 side so that $V_1 = V_H + V_L$. Tr7 and Tr8 are open on V_2 side so that $V_2 = 0$. Since the output is taken differentially, $V_{out} = V_H + V_L$.
- State 2: Tr5 and Tr6 are open on V_2 side so that $V_2 = V_H + V_L$. Tr3 and Tr4 are open on V_1 side so that $V_1 = 0$. Since the output is taken differentially, $V_{out} = -(V_H + V_L)$.
- State 3: Tr2 and Tr3 are open on V_1 side so that $V_1 = V_L$. Tr7 and Tr8 are open on V_2 side so that $V_2 = 0$. Since the output is taken differentially, $V_{out} = V_L$.
- State 3: Tr6 and Tr7 are open on V_2 side so that $V_2 = V_L$. Tr3 and Tr4 are open on V_2 side so that $V_1 = 0$. Since the output is taken differentially, $V_{out} = -V_L$.

The biasing waveform distribution system is designed to distribute the waveform produced by the generator card to the MEMS switches. The design and implementation of the distribution system has been accomplished by Halil Ibrahim Atasoy and the author has accompanied him during most of the steps. The distribution system is designed as two types of cards, which are the microcontroller and the relay driver cards, so that they can be used modularly. Figure 3.17 illustrates the two cards. The modular approach is feasible for this case since the number of relay driver cards depends upon how many MEMS switches we will drive. The microcontroller card can control 8 relay driver cards where each driver card can control 8 MEMS switches simultaneously. During the measurement of the RF MEMS IT, three or four distribution cards are used since there are a total of 30 MEMS switches to be controlled.



(a)



(b)

Figure 3.17: The waveform distribution system cards photograph and the block diagram. (a) Microcontroller card. (b) The relay driver card.

The microcontroller card is composed of a microcontroller (PIC16F877) and two buffers (74HC367). The microcontroller is triggered by the Agilent E3631A DC supply, which is controlled by the HPVEE program on the computer using GPIB interface. The microcontroller produces the 8-bit control data to control the relays and 3-bit address data to select the relay control cards. Each relay control card is composed of a latch (74HC574) to hold the control data coming from the microcontroller, a demultiplexer (74HC138) to convert the address data, a dipswitch to set the card address, and 8 relays (V23026) to switch the biasing waveform. The relays are used as single pole double throw (SPDT) switches, which select either one

or the other terminal of the generator card output. But since one of the terminals is connected to the ground of the relay control card, it behaves as the ground. The photographs of the all cards attached and the whole measurement setup can be seen in Figure 3.18.

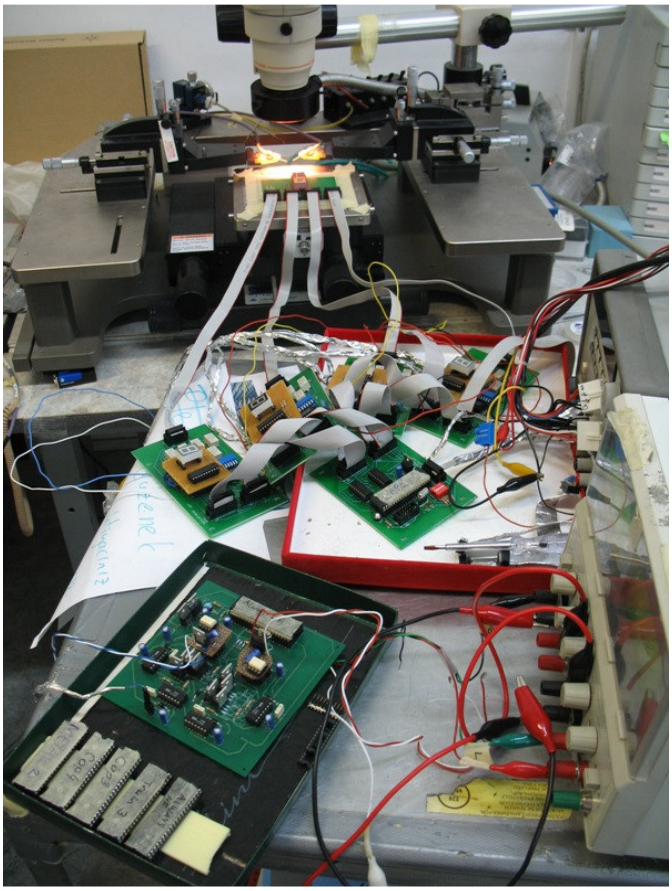


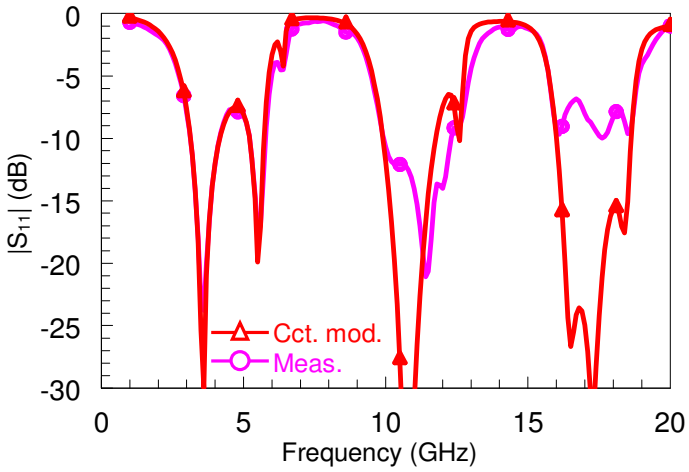
Figure 3.18: The photograph of the multi-pin MEMS automated measurement setup.

3.3.3. The Measurement Results of the RF MEMS Impedance Tuner

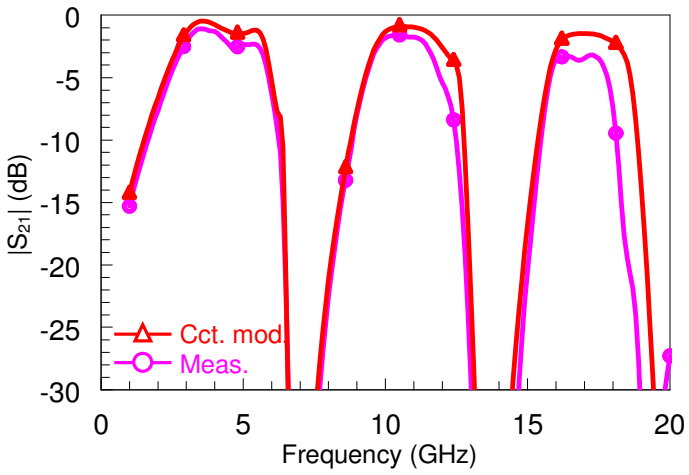
The MAMS is used for the measurements of the RF MEMS IT. The IT is measured in 1-20 GHz band using SOLT calibration technique, and Cascade ACP-GSG-150 coplanar probes are used during the measurements.

The IT is mounted on 24-pin, alumina based HYB02413 package instead of 40-pin, ceramic based CSB04046 package although the former has not enough number of pins. This is because some problems occurred during the measurements of the IT sample mounted on 40-pin, ceramic based CSB04046 package. Since HYB02413 package has 24 pins and there are no alumina based packages with a higher number of pins, 30 control pins of the IT are connected to the 24 pins of this package. This is done by shorting the fourth and fifth, and eighth and ninth pins of each stub, which reduces the total number of control pins of the IT to 24. The pins to be shorted are selected to obtain minimum reduction of the impedance coverage of the IT on the Smith Chart. As a result, a total of $(8 + 1)^3 = 729$ impedance states of the IT are measured. 1-20 GHz band is measured in 401-points using SOLT calibration since increasing the number of points also increase the data transfer time to the PC, and the total measurement time increase significantly. This situation affects the measurement reliability since the RF MEMS switches start to be affected from the dielectric charging as the total downstate time of the switches increase.

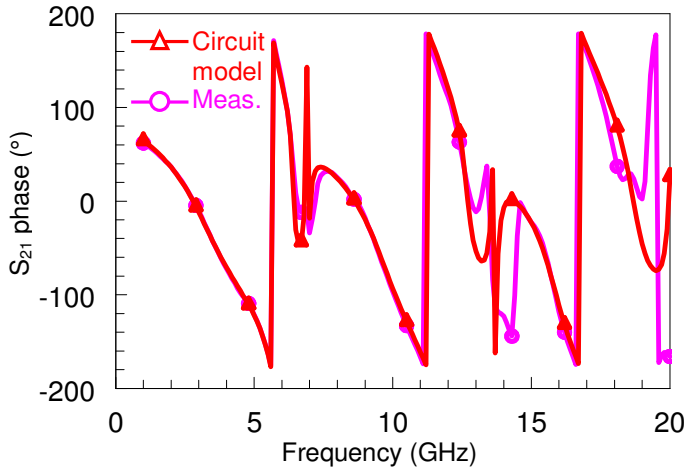
Figure 3.19 shows the measured upstate performance of the fabricated RF MEMS IT compared with the simulations. Figure 3.20 and Figure 3.21 show the measured performance of the RF MEMS IT for same sample impedance states compared with the simulations. The figures show that the measurements are in agreement with the simulations. The values of the circuit model parameters that are extracted from the measurements are given in Table 3.4. Most of these parameters simulations are the close to the ones given in Table 3.2. However, the upstate capacitances are increased significantly. This is because of the decrease in the bridge heights of the MEMS switches. Although the bridge is almost flat in between the anchors, they do not follow the changes on the substrate, and the bridge heights do not increase at the areas where the first metal layer is present. As a results, the height between the first metal layer and the MEMS bridge decrease significantly, which results the increase in the upstate capacitances. This behavior was explained in more detail in Chapter 5.



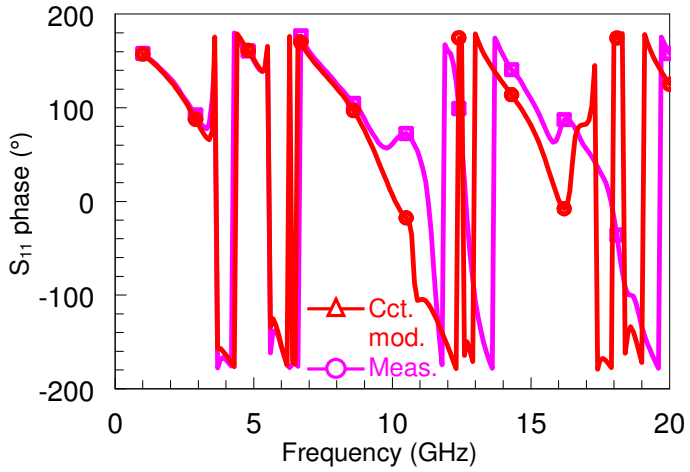
(a) $|S_{11}|$.



(b) $|S_{21}|$.



(c) $\angle S_{21}$.

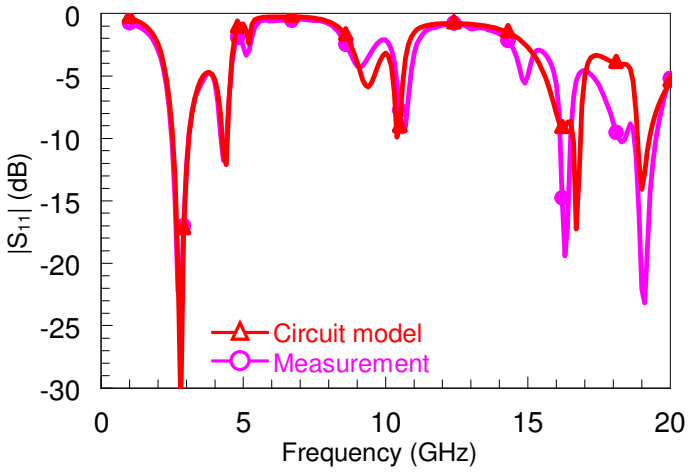


(d) $\angle S_{11}$.

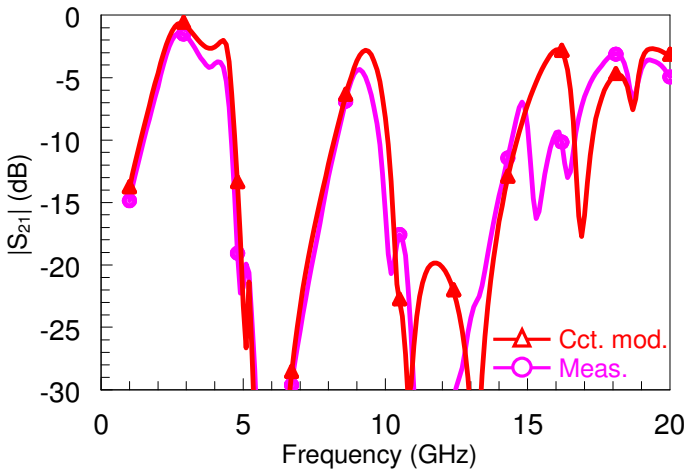
Figure 3.19: The measured upstate performance of the RF MEMS IT compared with the simulations (Stb1 = 0, Stb2 = 0, Stb3 =0) (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$ (d) $\angle S_{11}$.

Table 3.4: The circuit model parameters that are extracted from the measurements of the RF MEMS IT.

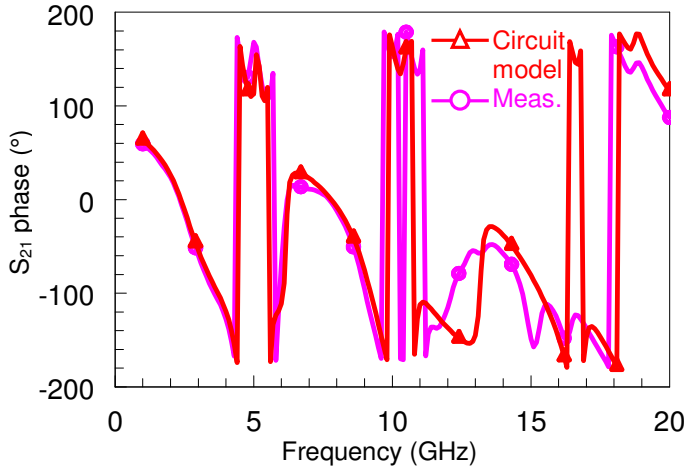
Circuit Model Parameters Extracted from Measurements			
Z_o	97.5 Ω	C_{sbd}	1.085 pF
$\varepsilon_{r,eff}$	2.45	C_{bgd}	4.46 pF
α	33 dB/m @20 GHz	L_b	10 pH
s	550 µm	R_{bu}/R_{bd}	0.5 / 0.5 Ω
C_{sbu}	193.9 fF	C_U/C_D	155.7 fF/ 872.9 fF
C_{bgu}	791.1 fF	R_{bias}	4000 Ω
Interconnection line parameters			
Z_o = 51.2 Ω, $\varepsilon_{r,eff}$ = 2.44, α = 71 dB/m, l = 994 µm			



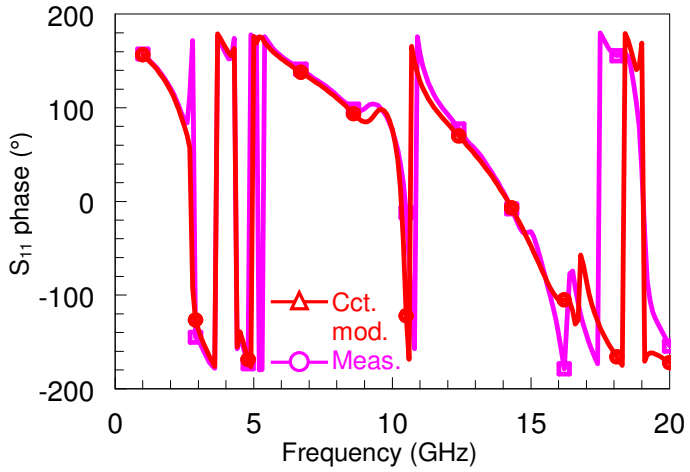
(a) $|S_{11}|$.



(b) $|S_{21}|$.

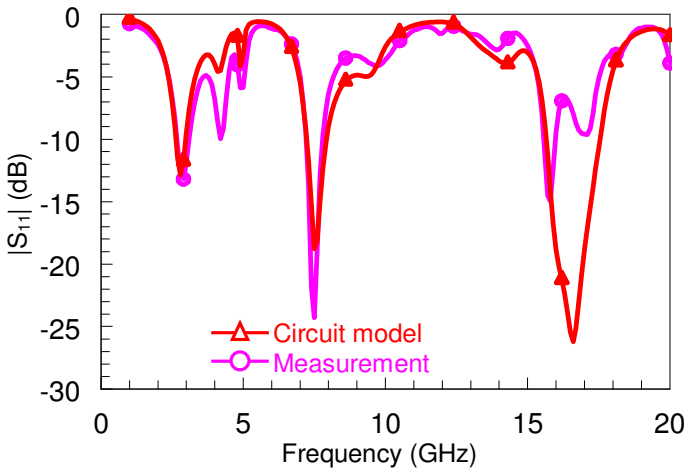


(c) $\angle S_{21}$.

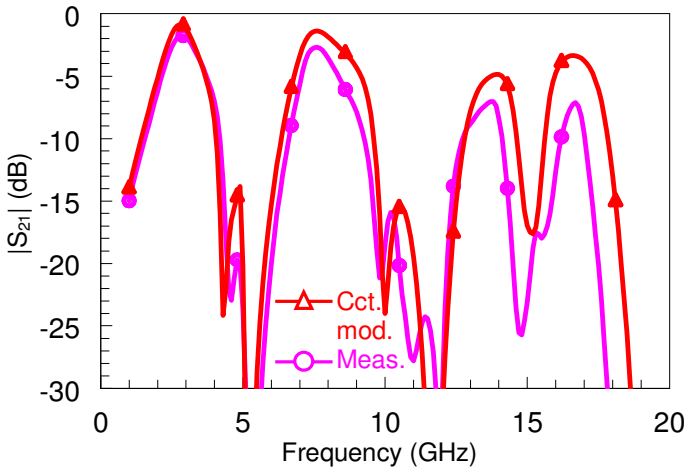


(D) $\angle S_{11}$.

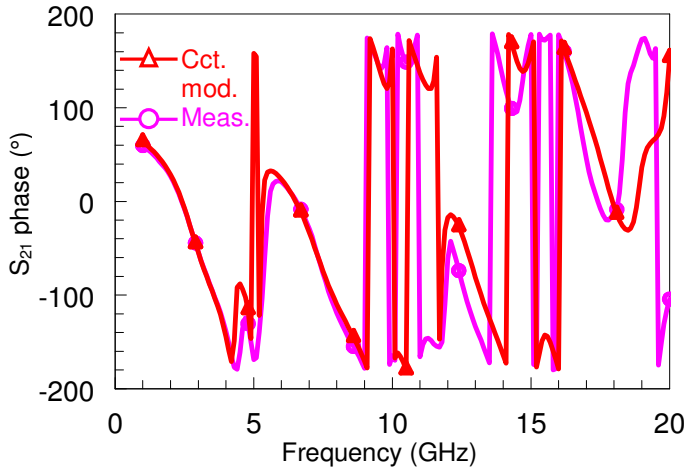
Figure 3.20: The measured performance of the RF MEMS IT compared with the simulations (Stb1 = 4, Stb2 = 2, Stb3 =32) (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$ (d) $\angle S_{11}$.



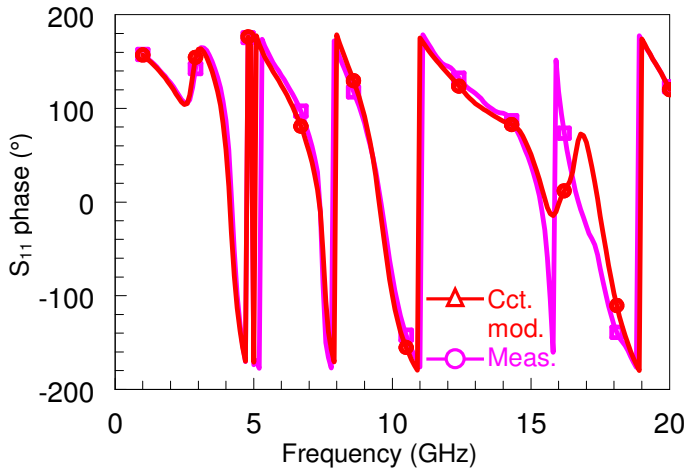
(a) $|S_{11}|$.



(b) $|S_{21}|$.



(c) $\angle S_{21}$.

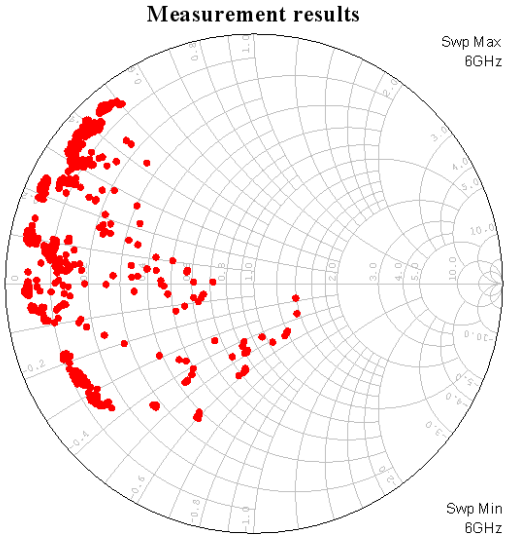


(c) $\angle S_{11}$.

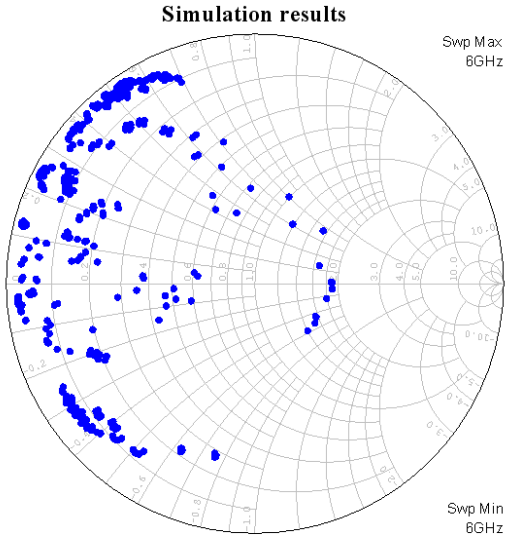
Figure 3.21: The measured performance of the RF MEMS IT compared with the simulations (Stb1 = 64, Stb2 = 384, Stb3 =24) (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$ (d) $\angle S_{11}$.

Figure 3.22 shows the impedance coverage of the fabricated RF MEMS IT. The left-hand side figures show the measurement results for $9^3 = 729$ impedance states, and the right-hand side ones show the corresponding simulations of those states. These figures show that the simulated Smith Chart coverage is almost achieved from the measurements. It should be mentioned here that the circuit model parameters given in Table 3.4 are used for the simulations, which account the changes in the upstate capacitances. R_{bu}, R_{bd}, and L_b are also differed from their values given in Table 3.2. These modified values are used in the simulations since

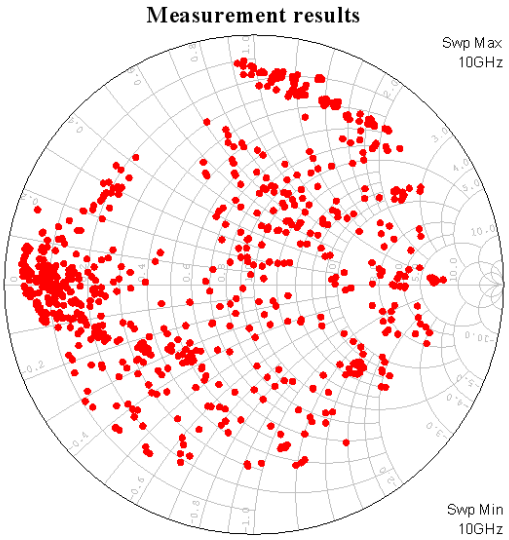
the simulations using these modified values give a better Smith Chart coverage when compared with the measurements. The change in L_b is because of the modified performance of the T-junctions. Since the MEMS bridge heights are changed, the performance of the T-junction, which is directly effective and optimized for the best the Smith Chart coverage, are also affected. The change in L_b compensates the consequences of the change in the performance of the T-junctions. The discussion about the changes in R_{bu} and R_{bd}, will be given in detail in Chapter 5.3.



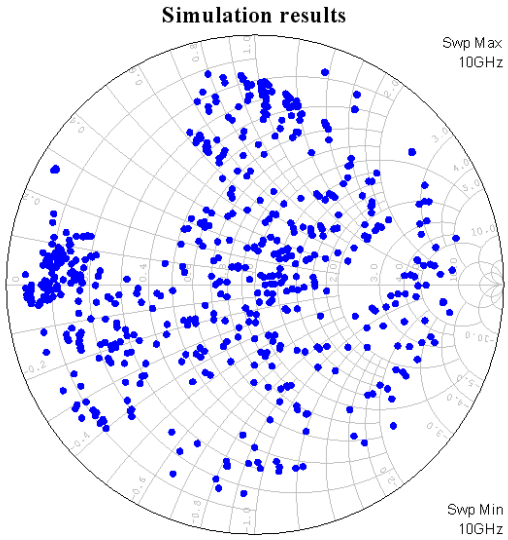
(a) 6 GHz measurements



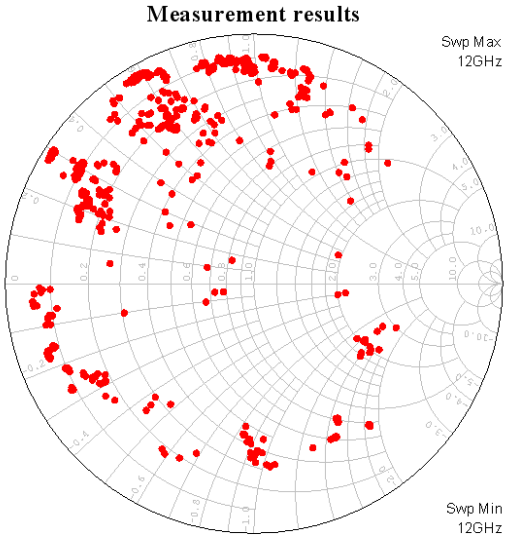
(b) 6 GHz simulations



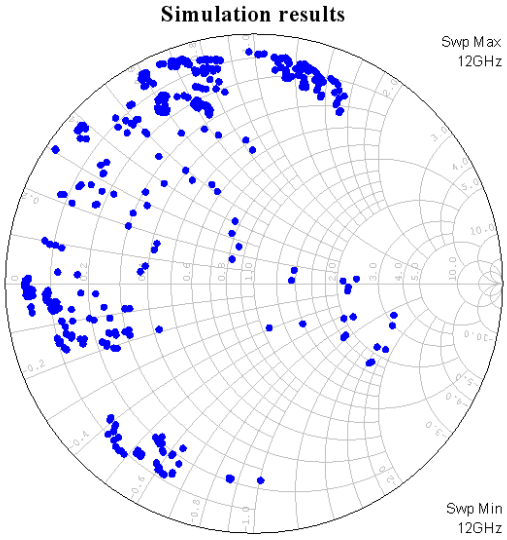
(c) 10 GHz measurements



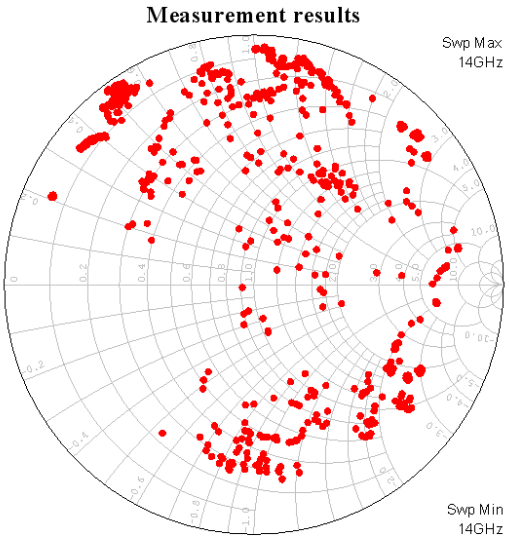
(d) 10 GHz simulations



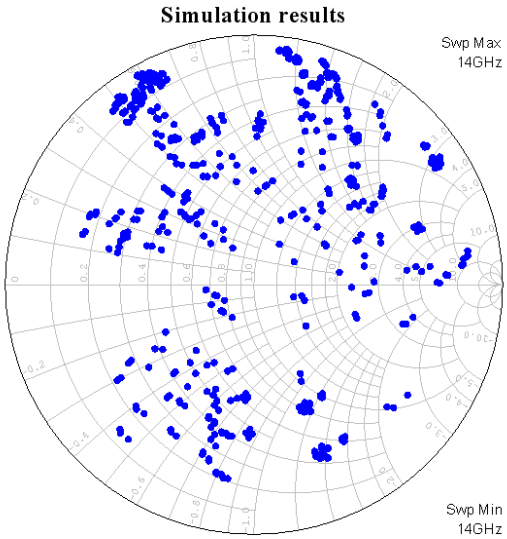
(c) 12 GHz measurements



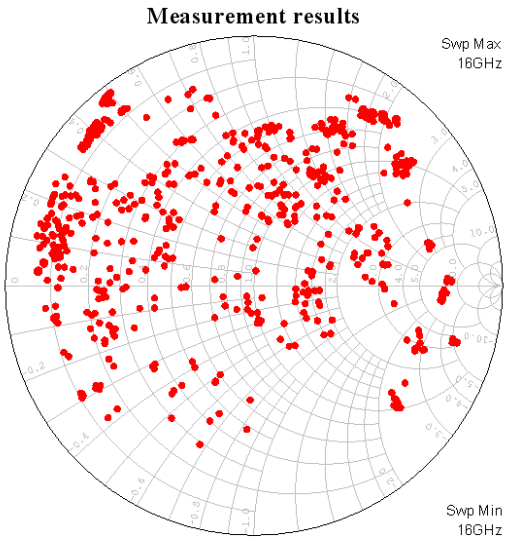
(d) 12 GHz simulations



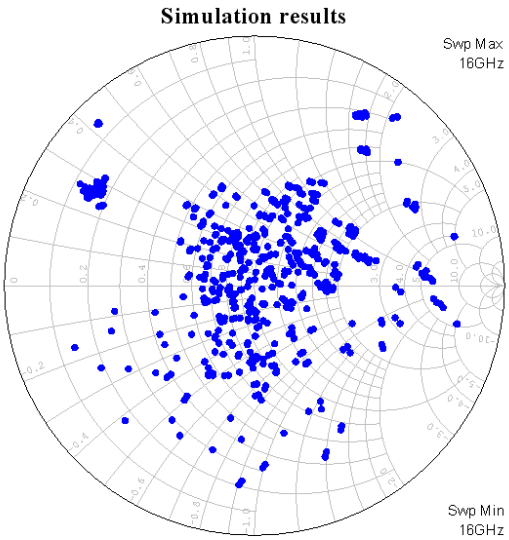
(e) 14 GHz measurements



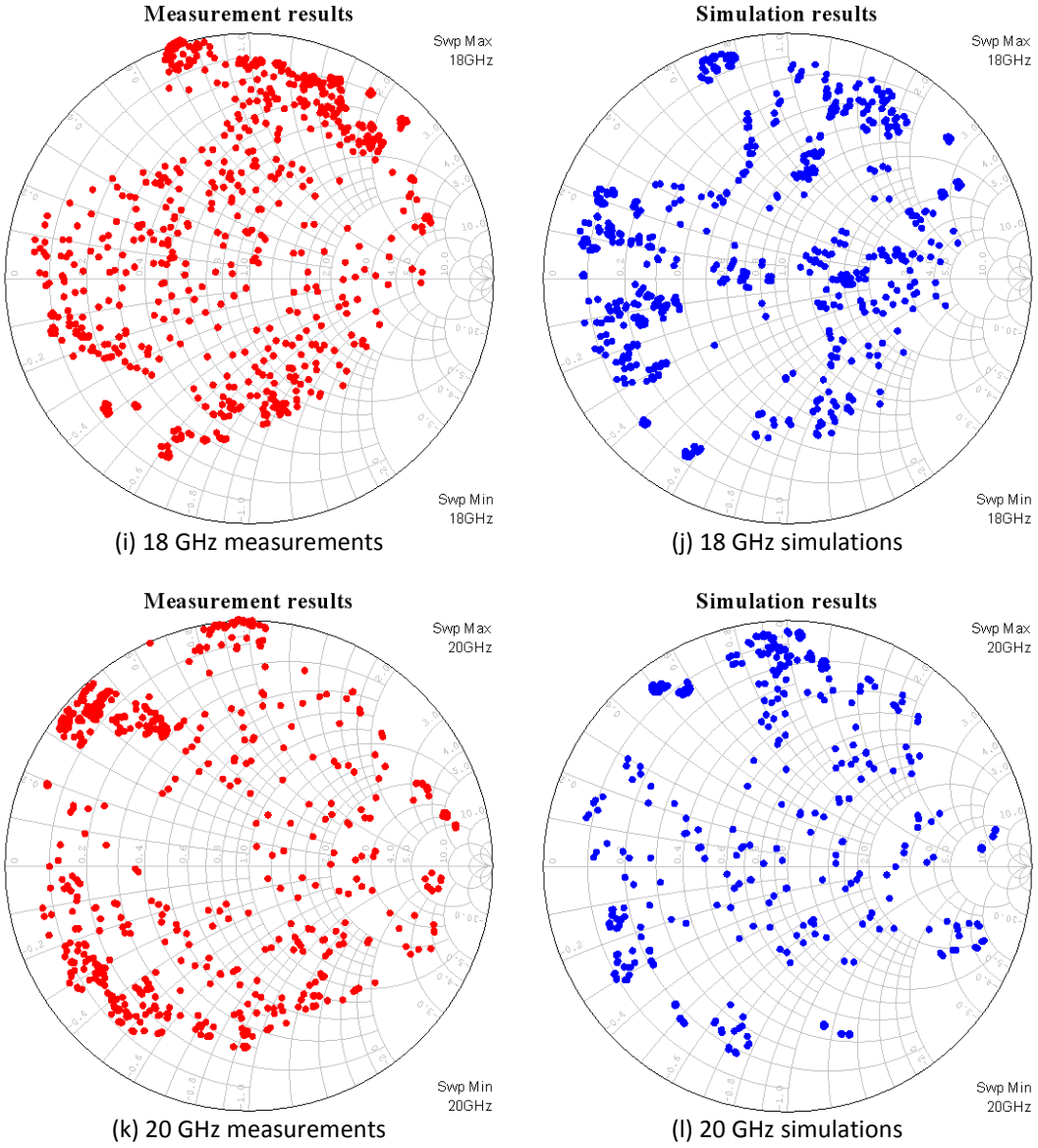
(f) 14 GHz simulations



(g) 16 GHz measurements



(h) 16 GHz simulations



(i) 18 GHz measurements (j) 18 GHz simulations

(k) 20 GHz measurements (l) 20 GHz simulations

Figure 3.22: The measured and simulated Smith Chart coverage of the RF MEMS IT in 6-20 GHz band.

Figure 3.22 shows the "exact" points that can be covered with the fabricated IT. However, -10 dB return loss is acceptable for many applications. So, considering a impedance mismatch level of 10 dB, the one-to-one correspondence between each measured-simulated impedance point pair is investigated. Table 3.5 summarizes the criteria for the comparison and the number of points that satisfy each criterion.

Table 3.5: The summary one-to-one correspondence between the measured and the simulated impedance point of the IT.

# of points	10 GHz	20 GHz	Amp. Margin	Phase Margin
n_{10dB}	267	182	r_{10dB}	ϕ_{10dB}
$n_{\phi 1}$	286	329	r_{10dB}	20°
$n_{\phi 2}$	345	363	r_{10dB}	30°
$n_{\phi 3}$	402	412	r_{10dB}	50°
n_{amp}	553	472	r_{10dB}	NA

r_{10dB}	Radius of 10 dB constant impedance mismatch circle (variable for each impedance point)
ϕ_{10dB}	The maximum phase deviation within 10 dB constant impedance mismatch circle (variable for each impedance point)
n_{10dB}	# of simulation points that fall into 10 dB circle of its corresponding measurement point
$n_{\phi i}$	# of simulation points that has $\|\Gamma_{sim}\| = \|\Gamma_{meas} \pm r_{10dB}\|$ and maximum phase deviation of ϕ_i degrees
n_{amp}	# of simulation points that has $\|\Gamma_{sim}\| = \|\Gamma_{meas} \pm r_{10dB}\|$

For the comparison of the measured and simulated point pairs, different criteria are used. The first one is the "constant impedance mismatch circle (CIMC)", which is used in the design of two-port network that is not matched at both of its ports. The CIMC determines the points that will have 10 dB return loss when connected to the original points. These points fall onto a circle for each impedance point on the Smith Chart, as its name already implies. The center, $\Gamma_{sM,}$ and the radius, $r_{sM,}$ of the CIMC can be calculated as in [172] using (3.8) and (3.9), respectively, where (3.10)-(3.11) give the impedance mismatch factor, M_1. (3.10) is the general form of M_1, and (3.11) is the reduced form that is used to calculate Γ_{sM} and r_{sM}.

$$\Gamma_{sM} = \frac{M_1(\Gamma_{in})^*}{1-(1-M_1)|\Gamma_{in}|^2} \tag{3.8}$$

$$\mathrm{r}_{sM} = \frac{\sqrt{1-M_1}(1-|\Gamma_{in}|^2)}{1-(1-M_1)|\Gamma_{in}|^2} \tag{3.9}$$

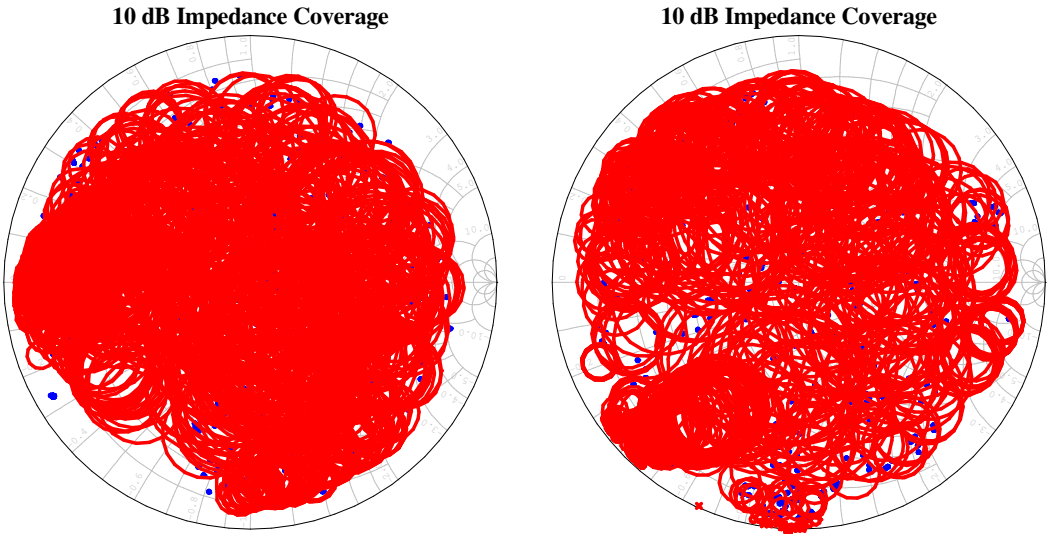
$$M_1 = \frac{(1-|\Gamma_{in}|^2)(1-|\Gamma_s|^2)}{|1-\Gamma_{in}\Gamma_s|^2} \tag{3.10}$$

$$M_1 = 1-\rho^2 \; and \; \rho = \frac{VSWR_{req}-1}{VSWR_{req}+1} \tag{3.11}$$

Table 3.5 shows that only 267 and 182 out of 729 simulation points fall into CIMC of their corresponding measured impedance points. However, this is mostly due to the phase errors occur in the phase of S_{11}. The phase of S_{11} generally changes rapidly in the triple stub IT topology, which cause the target impedance point to shift. This behavior can also be observed from Figure 3.19 to Figure 3.21. To prove this, the phase margin is loosed to three constant levels, which are namely 20°, 30°, and 50°, while keeping the amplitude margin as r_{10dB}. In this case, it is observed that the number of points that fall into to the margin of its corresponding point increases. Finally, if only the amplitude margin is used, which is again r_{10dB}, and the phase margin is removed, 553 and 472 out of 729 simulation points fall into the margin of its corresponding measured impedance point.

One point should also be mentioned before concluding the impedance coverage discussion, which is related with the limitations of the measurement setup. Since 729 impedance points have been measured continuously, some of the RF MEMS switches stay in downstate for a “long time”. Long time here refers the time that the switch performance starts degrading due to the dielectric charging. The phase response of the tuner shifts some degrees even the performance of a single RF MEMS switch drifts from its original upstate response. One proof of this statement is that the IT upstate response is “shifted” when it is measured after the measurement of 729 states. The “new” upstate response can be modeled by increasing the upstate capacitance, which proves the statement. As a result, it is expected that the IT may have better performance in terms of number of matching impedance pairs once it is measured considering this situation.

Finally, if the 10 dB impedance coverage of the all 729 measured impedance points is investigated, it is seen that this range covers almost 100% of the simulated impedance points. This means that the targeted impedance range that is defined by the simulations is covered by the measured impedance points with a worst case impedance mismatch of 10 dB. Figure 3.23 shows the mentioned comparison at two sample frequencies, which are namely 10 GHz and 20 GHz. The red regions show the area that is covered by the 10 dB circles of the measured 729 impedance points, and the blue points show the 729 simulated impedance points. In this figure, the conjugates of the simulated and measured points are used due to the definition of impedance mismatch.



(a) 10 GHz (b) 20 GHz

Figure 3.23: The 10 dB impedance coverage of the measured impedance points that can be matched by the fabricated RF MEMS IT (a) 10 GHz (b) 20 GHz. The impedance points in this figure are the conjugates of the ones given in Figure 3.22.

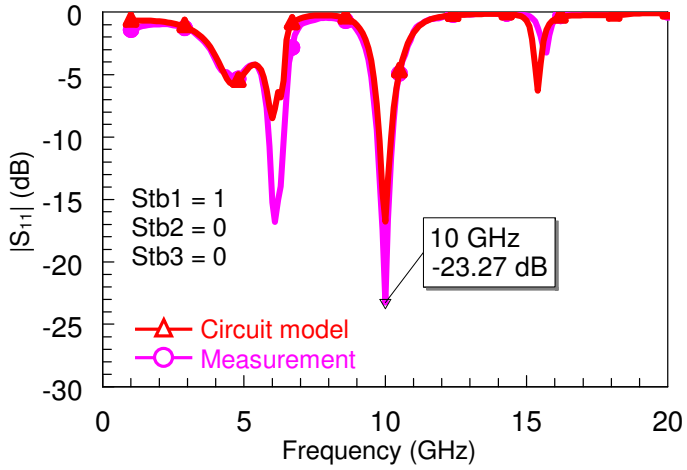
Finally, some example impedance transformations using the fabricated IT are presented. Figure 3.24 the measured performance of the IT when it is adjusted to transform 50 Ω to 5 Ω at 10 GHz compared with the simulations. Another example is presented in Figure 3.25 where the measured performance of the IT is given

compared with the simulations. In the figure, the IT is adjusted to transform 50 Ω to 150 Ω at 20 GHz, and the losses are calculated using (3.7).

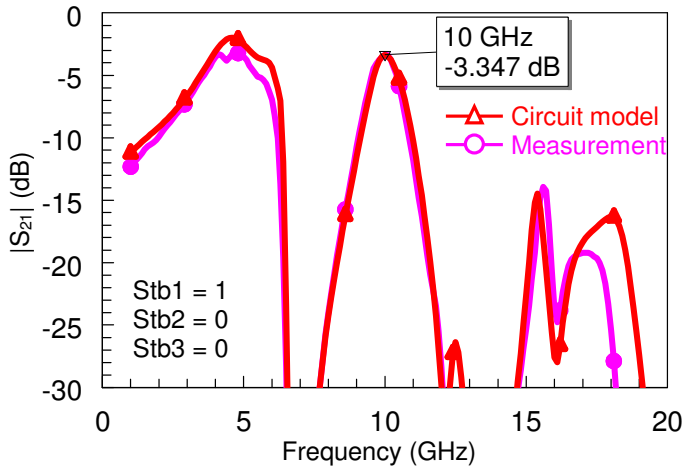
The measured insertion losses are about -3.3 dB for both cases. Although the loss behavior is similar to the simulations that use the extracted circuit model parameters, the measured losses are higher than that of the original design values. The reason for this case is the reduced MEMS bridge height. The reduced height increases the upstate capacitances, and the increase in the loss is actually expected as can be seen from the formula of the calculation of the loss of a DMTL. The formula is given in (3.12), and it is expected from the formula that the losses will increase as the upstate capacitance increases. Since the IT structure is composed of 30 MEMS switches that are as used as unit sections, and only 3 of them are hold in downstate at each impedance state, the amount of the loss increase is reasonable.

$$\alpha_{ld} = \frac{R_t}{2Z_{ld}} + \frac{R_b Z_{ld} \omega^2 C_U^2}{2} \; dB/unit\ section \tag{3.12}$$

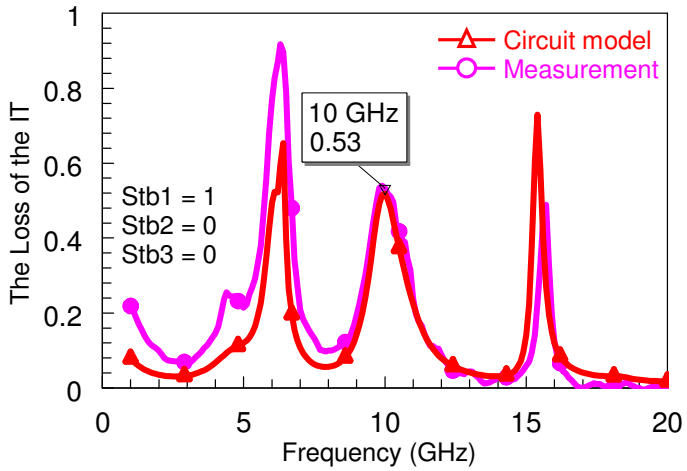
If the loss is calculated using the extracted circuit model parameters, the loss per unit section increases from 0.044 dB/unit section to 0.078 dB/unit section. This is obtained by only increasing the upstate capacitance from the original simulation values to the extracted values. So, this much change per unit section (switch) in the upstate also supports the above reasoning.



(a) $|S_{11}|$.

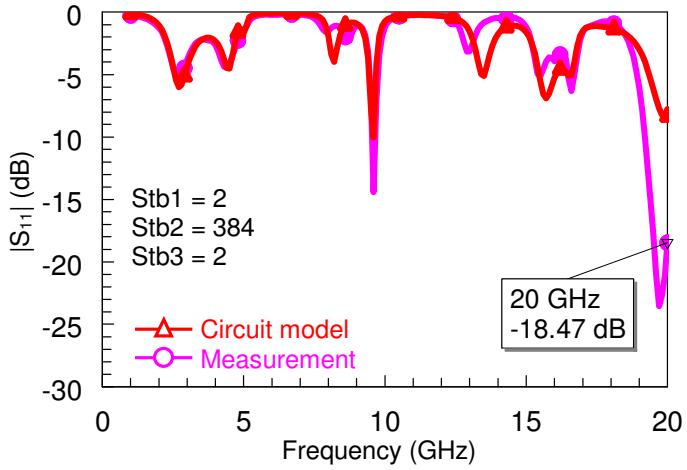


(b) $|S_{21}|$.

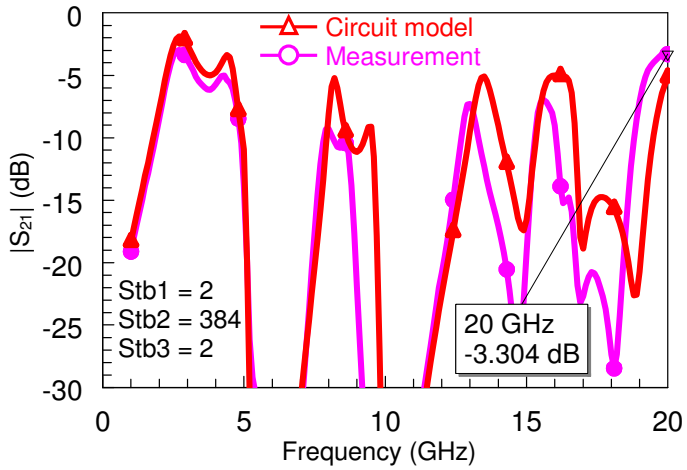


(c) The loss of the IT.

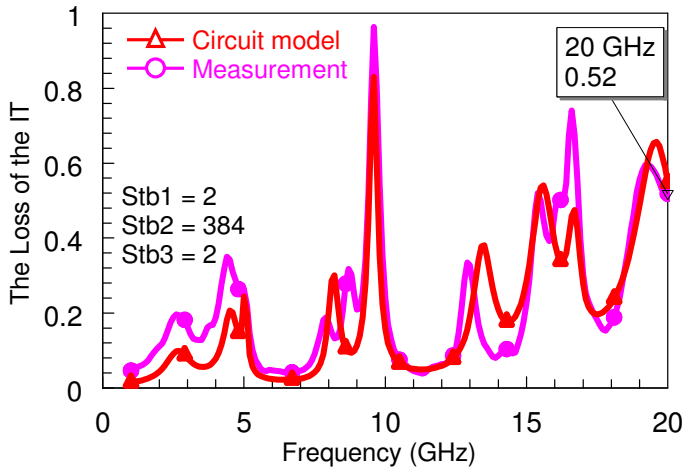
Figure 3.24: The measured performance of the triple stub IT for 50 Ω-to-5 Ω impedance transformation at 10 GHz compared with the simulations (a) $|S_{11}|$ (b) $|S_{21}|$(c) The loss of the tuner at this state.



(a) $|S_{11}|$.



(b) $|S_{21}|$.



(c) The loss of the IT.

Figure 3.25: The measured performance of the triple stub IT for 50 Ω-to-150 Ω impedance transformation at 20 GHz compared with the simulations (a) $|S_{11}|$ (b) $|S_{21}|$ (c) The loss of the tuner at this state.

3.4. Conclusion

In this chapter, the design and the implementation of a reconfigurable RF MEMS triple stub impedance tuner is presented for 6-20 GHz applications. The aim is to design and implement a reconfigurable impedance tuner that covers as much area as possible on the Smith Chart in this frequency band. A multi-pin MEMS automated measurement setup is also designed and implemented for the measurements of the designed RF MEMS IT. The measurement results of the IT show good agreement with the simulations. Although the fabricated device suffers from the reduced MEMS bridge height, it still shows a good Smith Chart coverage within the band of interest. One-to-one correspondence of the measured and the simulated impedance points is also investigated, and it is observed that the phase error of S_{11} mainly determines the deviations in the one-to-one correspondence. In any case, it is shown that the measured impedance points almost totally cover the area that includes all of the targeted impedance points with 10 dB impedance mismatch.

CHAPTER 4

THE THEORY OF PHASE AND AMPLITUDE CONTROL USING TRIPLE STUB TOPOLOGY

4.1. Introduction

The impedance matching using the stub based networks is a very well known and frequently applied way of solving impedance mismatch problems [172], [173]. Single, double, and triple stub impedance matching networks are the most commonly used topologies, and the easiest way to implement these networks is to use transmission lines. The triple stub topology is actually an extension of the double stub topology. The third stub is generally used to "move" the load impedance point out of the "forbidden region" of the double stub topology on the Smith Chart [172]. The triple stub topology comes up with infinitely many solutions for the lengths of the three stubs. Some of these solutions can be selected so that some other parameters other than the reflection coefficient can be tuned while keeping the input impedance unchanged.

This chapter shows that the triple stub (TST) topology can be used to control the insertion phase and the amplitude of the input signal simultaneously while the input impedance matching is preserved, using low-loss transmission lines. The TST is arranged to make a 50 Ω-to-50 Ω impedance transformation, which is actually an all pass network, and the lengths of the three stubs are selected so that the insertion phase and the insertion loss can be tuned from 0° to 360° and -0.8 dB to more than -20 dB, respectively. The control mechanisms for the insertion phase

and the insertion loss are investigated and identified. The idea is also verified experimentally using coplanar waveguides (CPW) on quartz substrates.

4.2. The Theory of Phase Control Using Triple Stub Topology

4.2.1. Lossless Case

The theory of phase control using triple stub IMN is based on the infinitely many solutions for Z_o-to-Z_o transformation. This all-pass network may be used to control the phase of output voltage signal as an all-matched phase shifter.

In an ideal phase shifter, the phase of S_{21} is controlled while its amplitude is kept at 1. This means that all the power is transferred to the output and its S_{11} is equal to 0. So, there are two complex equations and three real unknowns, which are the susceptances of the three stubs. The S_{21} equation can be separated into its real and imaginary parts, which actually means that there are four real equations and three real unknowns, and the system of equations has infinitely many solutions. The S_{21} and S_{11} of a two-port network can be represented in terms of its ABCD parameters as in (4.1) and (4.2). In (4.1), a and b are used to represent the real and imaginary parts of a unity magnitude complex number with arbitrary phase.

$$S_{21} = \frac{2}{A + B + C + D} = \frac{a + jb}{\sqrt{a^2 + b^2}} \tag{4.1}$$

$$S_{11} = \frac{A + B - C - D}{A + B + C + D} = 0 \tag{4.2}$$

(4.1) and (4.2) can be reduced to

$$A + B = \frac{a - jb}{\sqrt{a^2 + b^2}} \tag{4.3}$$

$$A + B = C + D \tag{4.4}$$

which are the final form of the two complex equations.

The schematic of the TST is given in Figure 4.1. The network consists of lossless transmission lines with characteristic impedance $Z_o = 50\,\Omega$, relative dielectric constant $\varepsilon_{r,eff} = 1$, and lengths x, y, z, and t. X, Y, and Z stand for the normalized susceptances of the three stubs. During the calculation normalized values will be used; therefore, Z_o is equal to 1. The ABCD parameters of the TST are found using (4.5) and (4.6).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{TST,lossless} = \begin{bmatrix} 1 & 0 \\ jX & 1 \end{bmatrix} \begin{bmatrix} U & jT \\ jT & U \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jY & 1 \end{bmatrix} \begin{bmatrix} U & jT \\ jT & U \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jZ & 1 \end{bmatrix} \tag{4.5}$$

$$X = \tan(\beta x), Y = \tan(\beta y), Z = \tan(\beta z), T = \sin(\beta t), U = \cos(\beta t) \tag{4.6}$$

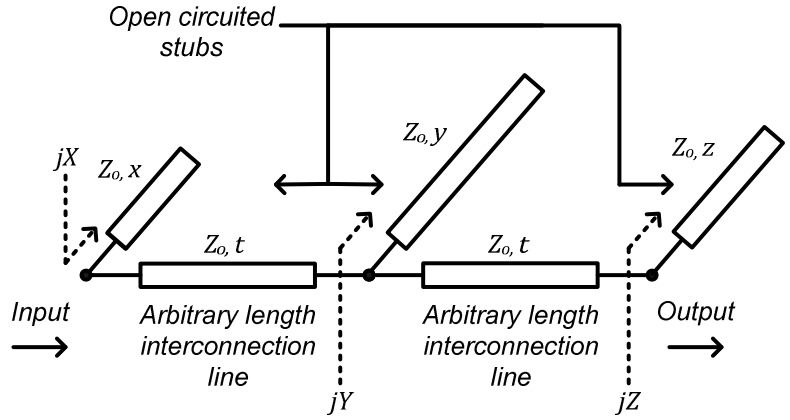


Figure 4.1: The schematic of the triple stub topology that is used for phase and amplitude control.

For the solution of the stub susceptances, (4.3) is separated into its real and imaginary parts, and solved for Y and Z, which results with:

$$Y = \frac{1}{T^2}\frac{b + 2TU\sqrt{a^2+b^2}}{\sqrt{a^2+b^2}} \tag{4.7}$$

$$Z = \frac{1}{bT}\left(T\sqrt{a^2+b^2} + aT + bU\right) \tag{4.8}$$

(4.4) can also be separated into its real and imaginary parts. Inserting (4.7) and (4.8) into the real part of (4.4), the conservation of power is verified, which is expected. Inserting (4.7) and (4.8) into the imaginary part of (4.4), X is found as:

$$X = \frac{1}{abT}\left(T^3(2-T^2)(a^2+b^2) - b^2T + aT\sqrt{a^2+b^2} + abU + TU^4(a^2+b^2)\right) \tag{4.9}$$

The equations (4.7)-(4.9) are the solutions for arbitrary interconnection line lengths and they are functions of only a, b, T and U. The lengths of the stubs are found using the inverse of the tangent function as:

$$x = \frac{\lambda}{2\pi}arctan(X), y = \frac{\lambda}{2\pi}arctan(Y), z = \frac{\lambda}{2\pi}arctan(Z) \tag{4.10}$$

The analytical solution presented for the lossless case is for the phase shifter solution with Z_o-to-Z_o transformation, which was intended to preserve the input impedance matching. However, there might be some cases where the input impedance is not required as to be Z_o, but rather, kZ_o. The analytical solution for this case is also investigated. By changing the conditions case given in (4.1) and (4.2) as

$$S_{21} = \frac{2}{A+B+C+D} = \frac{a+jb}{\sqrt{k}\sqrt{a^2+b^2}}, k \in \mathbb{R}\ and\ k > 1 \tag{4.11}$$

$$S_{11} = \frac{A + B - C - D}{A + B + C + D} = 0 \tag{4.12}$$

and following the same solution method, the solution is found for the Z_o-to-kZ_o transformation case where k is a real number. The solution for the susceptances in this case is given in (4.13)-(4.15).

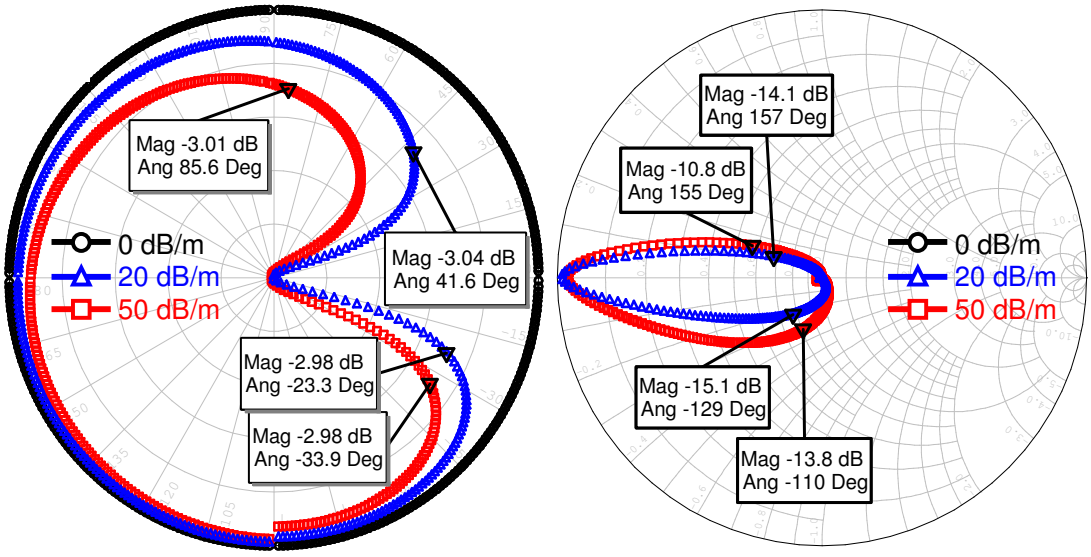
$$Y = \frac{1}{\sqrt{k}T^2} \frac{b + 2\sqrt{k}TU\sqrt{a^2 + b^2}}{\sqrt{a^2 + b^2}} \tag{4.13}$$

$$Z = \frac{1}{bT}\left(\sqrt{k}T\sqrt{a^2 + b^2} + aT + bU\right) \tag{4.14}$$

$$\begin{aligned} X = {} & \frac{1}{abT}\left(kT^3(2 - T^2)(a^2 + b^2) - b^2T + \sqrt{k}aT\sqrt{a^2 + b^2} + abU\right) \\ & + \frac{1}{abT}\left(kaTU^4(a^2 + b^2)\right) \end{aligned} \tag{4.15}$$

4.2.2. Lossy Case: Example Case Study: $t = \lambda/8$

To verify the formulation, a special case for an interconnection line length of $t = \lambda/8$, which is the most commonly used interconnection line length for TSTs, is studied. This TST is simulated in MWO for the whole phase range of 0-360° with 1° steps, where the lengths of the stubs of the IMN are calculated using (4.7)-(4.10), and the interconnection line lengths are fixed as $\lambda/8$. The simulation frequency is selected as 15 GHz, and transmission lines with $\varepsilon_{r,eff} = 1$ are used in the simulations. Figure 4.2-(a) shows that the formulation works well for 0-360° for the ideal (lossless) case (black line with circles in Figure 4.2-(a)). Figure 4.2-(b) verifies that the input matching is preserved since all the S_{11} point lie at the origin of the Smith Chart.



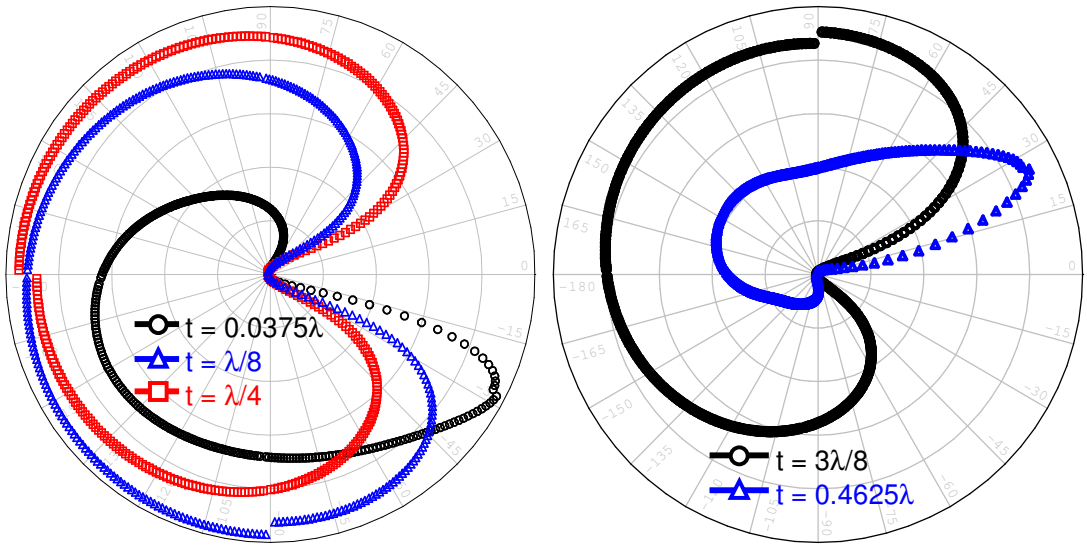
(a) (b)

Figure 4.2: The insertion phase, the insertion loss, and the return loss performances of the TST based phase shifter for different transmission line losses (a) S_{21} (b) S_{11}.

After verifying that the formulation is valid for the lossless case, the TST is simulated by adding a non-zero loss factor to the transmission lines and without changing any other parameters, i.e., keeping the stub and the interconnection line lengths the same. The simulation results for $\alpha = 20$ dB/m and 50 dB/m are also given in Figure 4.2. Examining the simulation results in the figure, it is seen that the formulation starts to deviate from the expected insertion phase and input return loss performance. Considering a worst case -3 dB range in the S_{21} magnitude, the phase shifter works for the 42-337° range for $\alpha = 20$ dB/m, and for the 86-326° range for $\alpha = 50$ dB/m. Out of these ranges, the phase shifter suffers from the increasing insertion loss, and the corresponding return losses also become worse than about -12 dB.

The above analysis show that the TST based phase shifter has a limited insertion phase range for a given value of the interconnection line, *t*. This is true for any value of *t*; but, the insertion phase range shifts as *t* changes. In other words, phase

shifter has limited insertion phase range for a specific value of *t*; however, whole 0-360° range can be covered by changing this interconnection line length. Since the solution exists for the stub lengths for each value of *t,* we can find one *t* value, for which the required insertion phase can be obtained. Figure 4.3 shows the performance of the phase shifter for different interconnection line lengths. For the cases in the graphs, S_{11} characteristics are also as good as $t = \lambda/8$ case for the possible phase range of each case. The reason of the discontinuities in the traces in Figure 4.3 is that the lengths of the stubs were increased by $\lambda/2$ in order to get rid of the negative line lengths coming from the mathematical formulation for some insertion phase values.

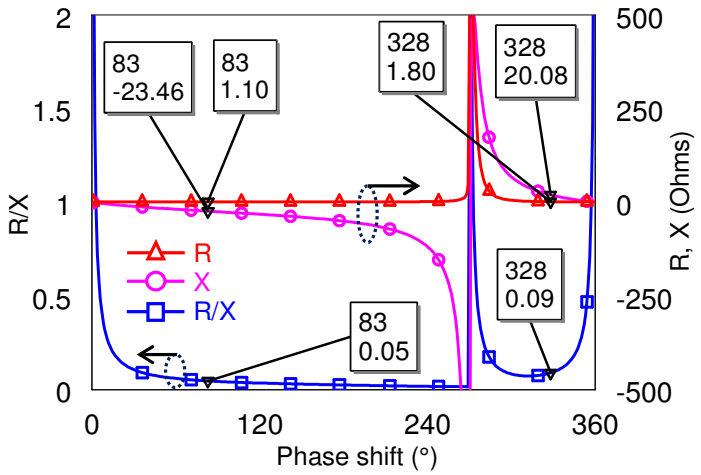


(a) (b)

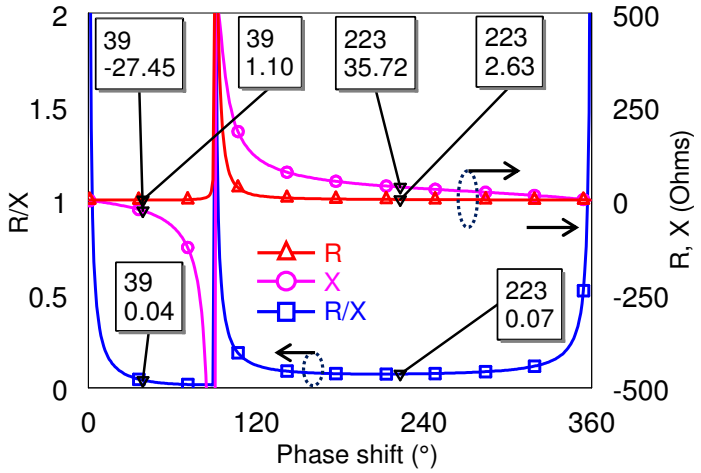
Figure 4.3: The performance of the TST based phase shifter for different interconnection line lengths (a) $t = 0.0375\lambda$, $t = \lambda/8$, $t = \lambda/4$ (b) $t = 3\lambda/8$, $t = 0.4625\lambda$.

The reason of the distortion in the insertion phase characteristics is understood better by examining the real and imaginary parts of the impedances of the stubs in detail. Figure 4.4 shows the real, R, and the imaginary, X, parts of the impedances

of the first and the third stubs, and their ratio, R/X for two sample interconnection line lengths. The first and the third stubs have the same length for all cases, which is a result of the analytical formulation. The imaginary parts of the impedance of the stubs get smaller as the desired insertion phase approaches to either 0° or 360°. Once the ratio of the real part to the imaginary part of the first and the third stub impedances increase significantly (0.05 as the insertion phase approaches 0° and 0.1 as the insertion phase approaches 360°; the difference between the ratios is the added $\lambda/2$ line because of the negative line lengths as explained above), the required reactance to be realized by the stub is suppressed by its resistance. As a result, the desired impedance transformations are not achieved, and the insertion and the return losses increase. The insertion phase also starts to deviate from the desired values. The real part of the input impedance of the second stub also becomes effective at some range; however, the real parts of the impedances of the first and the third stubs are the ones that distort the performance first.



(a) t = λ/8 @ 15 GHz.



(b) t = 3λ/8 @ 15 GHz.

Figure 4.4: The real and imaginary parts of the input impedance of the first stub and their ratio

4.3. The Phase / Amplitude Control Using the Triple Stub Topology

The results of the previous section show that 0-360° insertion phase range can be covered using the formulation for the lossless case and changing the length, t, of the interconnection line. It is observed on Figure 4.3 that the graphs are actually the shifted versions of each other, and there is always a low-loss region which can be tuned to the desired insertion phase value by changing t. At the other regions where the insertion loss increases significantly, the insertion phase and the input return loss is preserved up to some point. This result came up with the fact that the amplitude of the output signal can also be controlled.

It should be pointed out here that the aim is to achieve the above mentioned goal by only using low-loss transmission lines. The transmission lines used in the frame of this work have 50 dB/m loss at 20 GHz with characteristic impedance, Z_o = 50 Ω, and relative dielectric constant, $\varepsilon_{r,eff}$ = 1. The $R/\omega L$ is equal to 0.033 for these transmission lines at 15 GHz, where R and L are the per unit length parameters of the transmission line. This means that the transmission lines that are used in this work are low-loss transmission lines.

Several analytical solution methods are utilized to find the solution with lossy transmission lines; but, the problem results with four complex, transcendental equations that include complex hyperbolic functions. Instead, it is shown that the problem has solutions using two methods, (i) optimization and (ii) direct search of the whole solution space. In the first method, the Simplex optimization tool of the MWO is used, in which x, y, z, and t, are used as optimization variables. The optimization goals are setting:

i) $\angle S_{21}$ to any desired insertion phase value,
ii) $|S_{21}| = 1$, and
iii) $|S_{11}| = 0$.

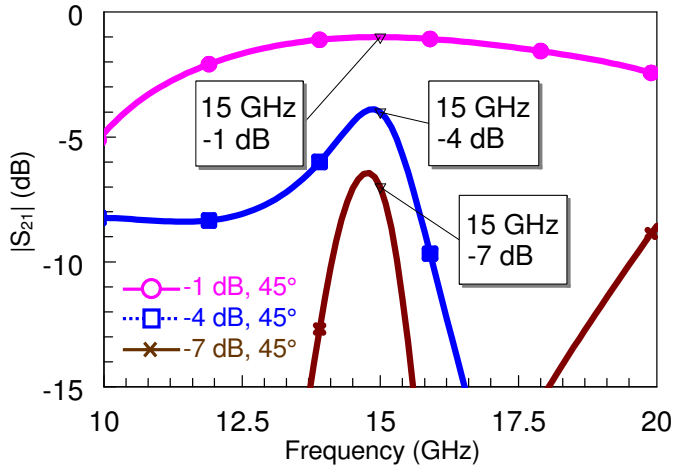
Using this method, the solutions are found for any magnitude value of the S_{21} from -0.8 dB to -20 dB and for any phase value of the S_{21} from 0° to 360° where $|S_{11}|$ is less than -250 dB for all cases. The solution took at most 30 s, and the cost of the optimization is always less than 10^{-26}. -20 dB for the S_{21} magnitude is not actually a limit; however, the insertion phase and the input return loss deviates from the desired values as the S_{21} magnitude becomes less than this value.

The second method is to sweep all the combinations of the line lengths from 0 to $\lambda/2$ with the smallest step size possible. A Matlab code has been developed for this purpose which can sweep the line length variables with $\lambda/80$ step size. The code can calculate $40^4 = 2.56$M combinations by searching the solution in 0 to $\lambda/2$ range for each variable in 300 seconds using multidimensional matrix operations supported by Matlab. Please note that a direct calculation of $12^4 = 20736$ combinations take about the same time, and the total simulation time grows exponentially as the step size decreases linearly. Using the developed code, it is observed that the same solutions can be found with the optimization method for any desired value of the phase and magnitude of the S_{21} where $|S_{11}|$ is less

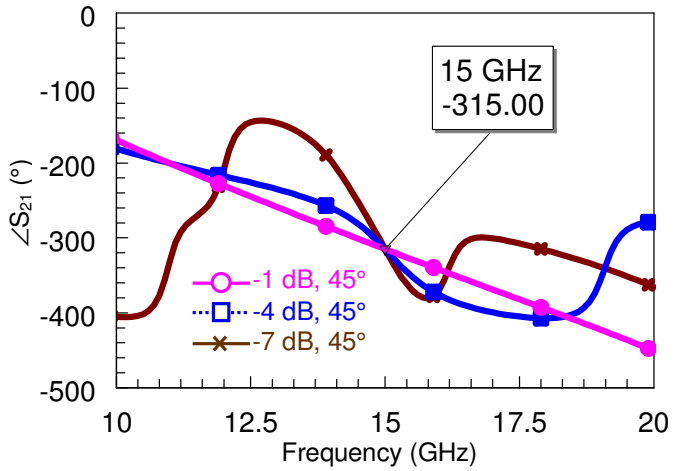
than -30 dB for all cases. The solutions found using this method, of course, has some errors because of the fact that the lengths are discreet variables.

The results of the two methods show that the TST can be used to control the insertion phase and the amplitude of the input signal at once while the input kept as exactly matched. This means that the TST can be used as a "vector modulator" circuit.

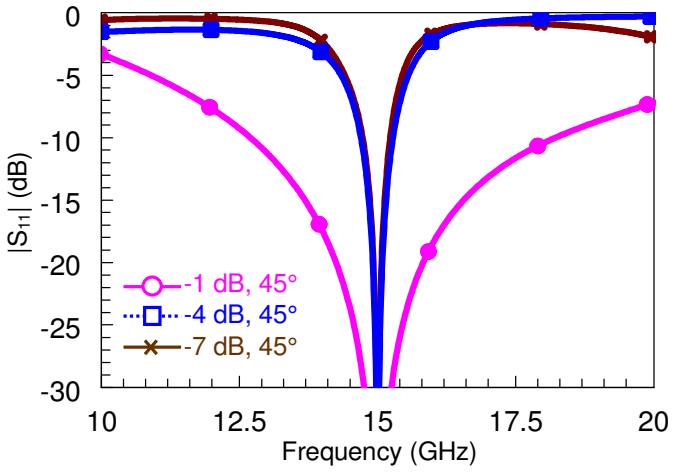
The frequency response of the TST is presented in Figure 4.5, where the vector modulator is set to different insertion phase/amplitude states. The circuit is naturally a narrowband circuit as it is based on transmission lines. However, the instantaneous bandwidth of the TST is large enough when the TST is used as a phase shifter. The bandwidth (BW) for -1 dB/45°, as an example, is about 3 GHz considering flat insertion loss (±0.2 dB for -1 dB) and acceptable return loss characteristics (better than -15 dB), and linear phase response. 2.6 GHz BW is equivalent to 17.3% bandwidth at 15 GHz, and it is limited by the return loss performance. The BW of the TST gets narrower as the required amplitude decreases. The BW for -7 dB/45° is 260 MHz (1.73%), and it is limited by return loss response (better than -15 dB). The amplitude remains within ±1 dB range in the BW determined by the return loss response. The insertion phase response is again linear within the return loss BW, and gives flat response when taken differentially with respect to the 0° state.



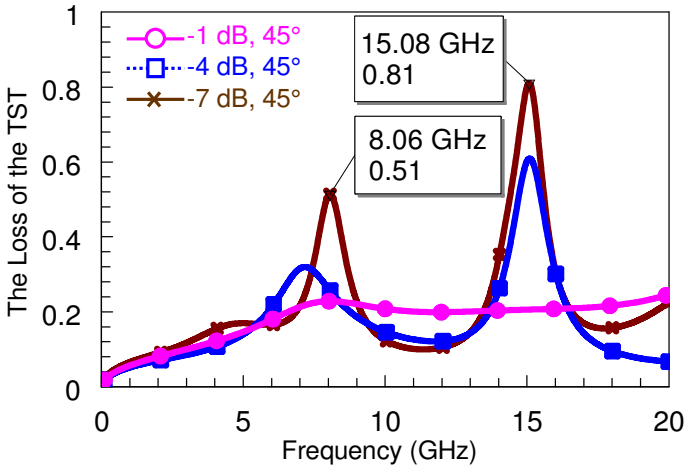
(a) $|S_{21}|$.



(b) $\angle S_{21}$ (unwrapped).



(c) $|S_{11}|$.



(d) The loss of the TST.

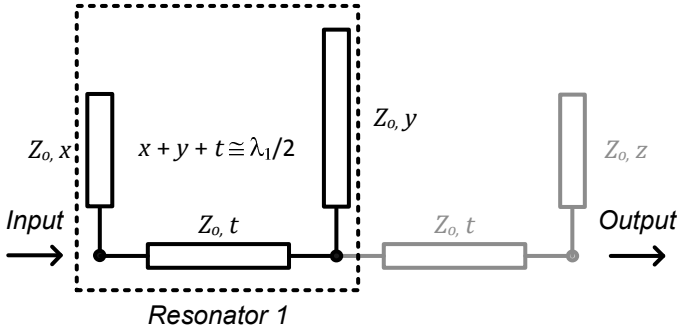
Figure 4.5: The performance of the TST when it is set to three sample insertion phase/amplitude states at 15 GHz (a) $|S_{21}|$ (b) $\angle S_{21}$ (c) $|S_{11}|$ (d) The loss of the TST.

4.3.1. Investigation of the Loss Behavior

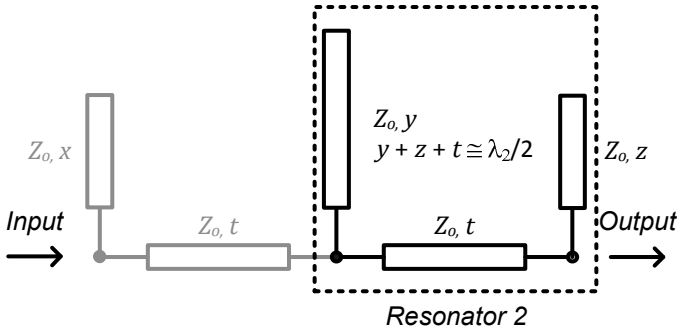
It is shown in the previous subsections that the TST can be used to control the amplitude of the input signal. It is possible to obtain amplitude levels as low as 0.1, which is equivalent to -20 dB insertion loss. Since the return loss is approximately 0 for all cases, having such small amplitudes means that most of the input power is attenuated in the circuit. It is interesting to have such a case since the circuit only consists of low-loss transmission lines.

The physical reasoning behind the losses, which can be defined as in (3.7) for a two-port network, is the resonating behavior of the TST. If the circuit is examined in detail, it is seen that there are three open-circuited terminations at the ends of the three stubs. The paths between any two of these open circuited ends behave as a $\lambda/2$ resonator, and the insertion loss of the TST increases significantly at any of the frequencies where the total length between the open-circuited terminations, i.e., $x + y + t$, $y + z + t$, and $x + z + 2t$, is equal to $n\lambda/2$. The resonators can be visualized in Figure 4.6.

One example of the above mentioned loss behavior can be seen Figure 4.5-(d). The loss of the TST that was set to (-7 dB, 45°) has peaks at 8.06 GHz and 15.08 GHz. The $x + y + t$, $y + z + t$, and $x + z + 2t$ totals are equal to 20042 µm, 20646 µm, 31415 µm, which are λ/2 at 7.48 GHz, 7.26 GHz, and 4.77 GHz, respectively. So, the peaks are due to the first resonator, and the loss peaks occur at frequencies that are very close to the first (7.48 GHz) and second (14.96 GHz) multiple of the λ/2 resonances. The difference between the simulated frequencies of the resonance points and the natural resonance frequencies of the λ/2 resonators is due to the fact that the real parts of the lossy transmission line distort the impedance transformation in and between the stubs.



(a)



(b)

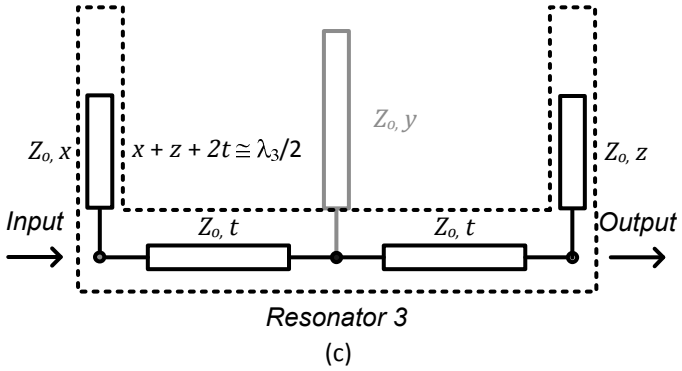


Figure 4.6: The open-circuited resonators of the TST.

Controlling the amplitude of the input signal using the $\lambda_o/2$ resonators is explained by approaching the problem from the quality factor point of view. Let us consider the circuits given in Figure 4.7. The circuit (1) is a $\lambda_o/2$ open-circuited transmission line resonator, which behaves like a shunt resonant circuit around $f = f_o$. The unloaded quality factor of circuit (1), Q, is given in (4.16) [173] as:

$$Q = \frac{\beta}{2\alpha} = \frac{R}{\omega_o L} \tag{4.16}$$

where α and β are the real and imaginary parts of the propagation constant of the transmission line, and R and L are the parameters of the equivalent parallel resonant circuit. R and L are given in (4.17).

$$R = \frac{Z_o}{\alpha l}, L = \frac{2Z_o}{\pi\omega_o}, and\ l = \frac{\lambda_o}{2} \tag{4.17}$$

Once this resonator is excited from any point between 0 and $\lambda_o/2$ as in circuit (2), it is loaded by the Z_o of the port 1, which is 50 Ω for this case. As a result, Q remains the same where the loaded quality factor, Q_L, decreases significantly since the external quality factor, Q_e, is much lower than Q. Q_e and Q_L are given in (4.18) and (4.19), respectively.

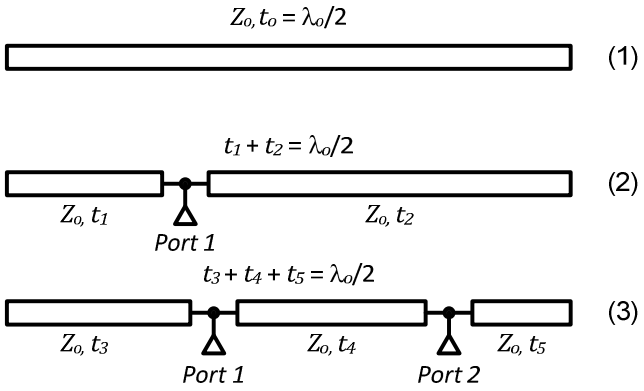
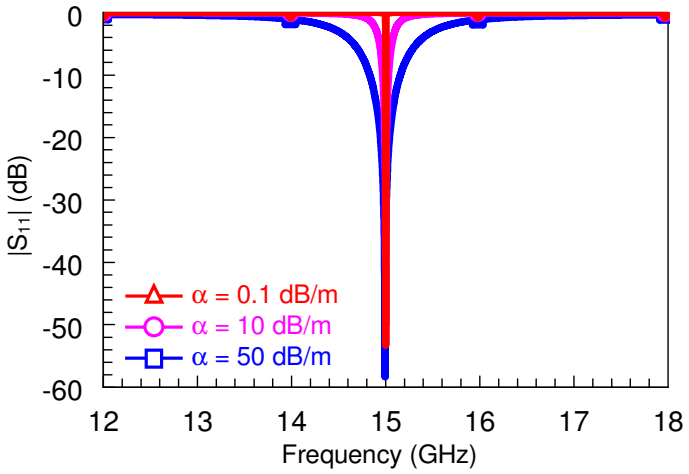


Figure 4.7: The schematic of λ/2 resonator with 0, 1, and 2 input/output ports.

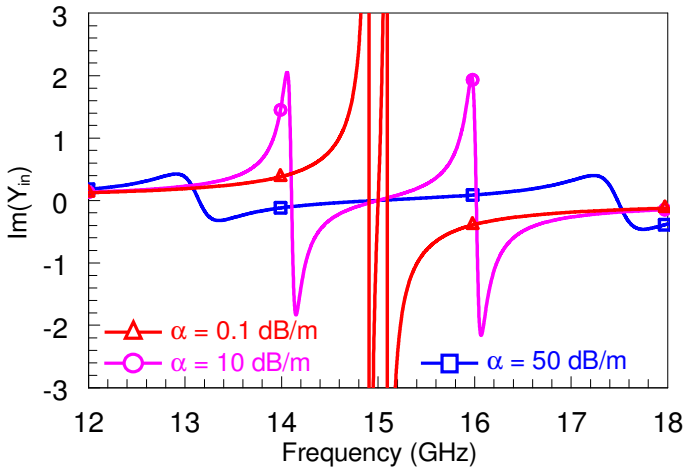
$$Q_e = \frac{Z_o}{\omega_o L} \tag{4.18}$$

$$\frac{1}{Q_L} = \frac{1}{Q} + \frac{1}{Q_e} \tag{4.19}$$

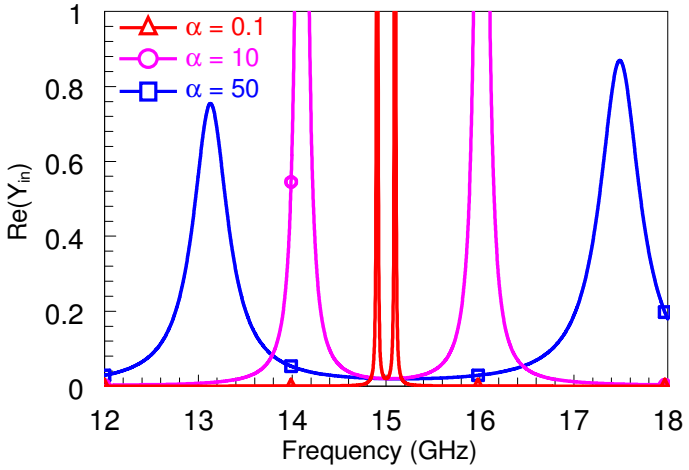
The input admittance at port 1 is purely real because the imaginary parts of the admittances looking towards each direction cancel each other since $t_1 + t_2 = \lambda_o/2$. So, the input admittance is purely real, and by changing the position of the port within the resonator, the real part of the input admittance at port 1 can be set to $Y_o = 1/Z_o$. This situation is true for any value of transmission line attenuation constant, α, which is greater than 0. This can be visualized in Figure 4.8. If t_1 and t_2 are selected around $\lambda_o/4$, there always exists a point where the sum of the real parts of the admittances looking towards each direction is equal to Y_o. The values of t_1 and t_2 that satisfy the condition for different values of α are given in Table 4.1. This, as a result, means that the maximum power transfer to the circuit (2) is obtained.



(a) $|S_{11}|$ of the resonator circuit (2).



(b) Imaginary part of the input admittance of the resonator circuits (2).



(c) Real part of the input admittance of the resonator circuits (2).

Figure 4.8: The $|S_{11}|$ and the input admittance of the resonator circuit (2) where the input admittance is equal to Y_o.

Table 4.1: The lengths used in the circuit (2) where the input admittance is equal to Y_o for different values of transmission line attenuation constants.

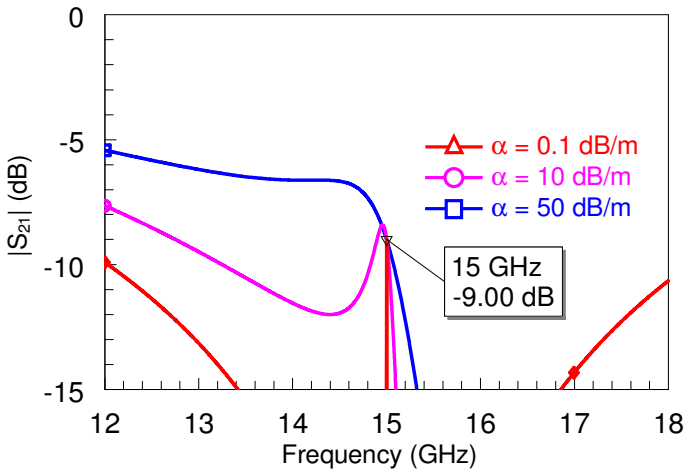
α (dB/m)	t_1 (μm)	t_2 (μm)
0.01	4986	5007
0.1	4965	5028
1	4896	5097
10	4679	5314
50	4285	5708

If one more port is added to the circuit as in circuit (3), the power that will be output power from the circuit can be adjusted. This can be achieved by arranging the positions of the two ports within the $\lambda_o/2$ resonator, and the S_{11} magnitude at port 1 can still be kept approximately equal to zero. This means that the maximum power transfer is still possible provided that the position of the port 1 in circuit (3) will be different than that of in circuit (2) because of the loading of Z_o of the port 2. An example case for circuit (3) is presented in Figure 4.9, where t_3, t_4 and t_5 are adjusted to have $|S_{21}|$ to be -9 dB for different values of transmission line attenuation constant, α. The values of t_3, t_4 and t_5 that are used in the simulations given in Figure 4.9 are presented in Table 4.2.

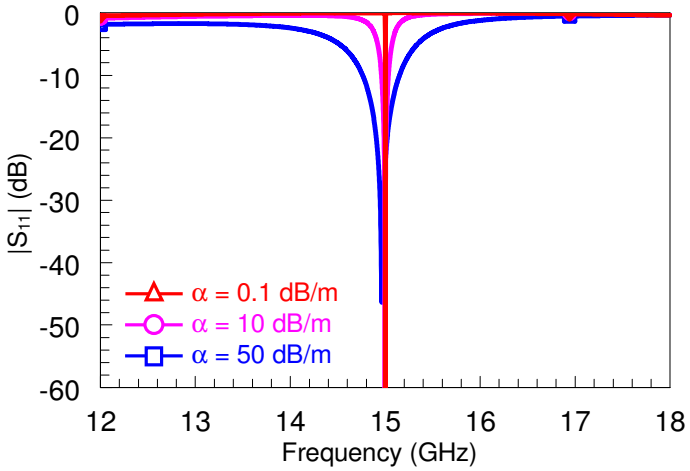
The idea behind controlling the output power is changing the value of Q_e. Arranging the positions of the ports is actually changing Q_e of the circuit by changing the ratio of Y_o to the real part of the input admittances at the port points. As a result, Q_L can be adjusted, which means that the amount of the power that will be dissipated in the circuit can also be adjusted. The same behavior, that is controlling the amount of the output power while keeping S_{11} magnitude equal to zero, can be obtained by changing the port impedances for given fixed positions of port 1 and port 2. In this case, it is clear that the Q_e of the circuit (3) is adjusted, and the output power control is obtained by changing Q_e of the circuit (3).

Table 4.2: The lengths of the parts of the circuit (3) for different values of transmission line attenuation constants.

α (dB/m)	t_3 (μm)	t_4 (μm)	t_5 (μm)
0.01	4986	4993	14.6
0.1	4963	4984	46
1	4889	4958	146
10	4658	4876	459
50	4249	4730	1015



(a) $|S_{11}|$ of the resonator circuit (3).



(b) $|S_{21}|$ of the resonator circuit (3).

Figure 4.9: The $|S_{21}|$ and $|S_{11}|$ of the resonator circuit (3).

4.3.2. Design Methodology in the Presence of the Losses

The design of the phase/amplitude control using the TST requires the analytical solution of the previously solved problem with lossy transmission lines. But, the analytical solution of the problem does not give explicit equations as explained in the previous subsections. Therefore, a design procedure that is based on the formulation for the lossless case is developed.

Observations on the solutions of the problem with lossy transmission lines using optimization and search of the whole solution space can be summarized as follows:

i) There is always an interconnection line length, t, that the analytical solution for the lossless case gives approximate results.
ii) The lengths of the first and the third stubs were equal in the analytical solution of the lossless case. The lengths of these stubs are not equal but close to each other for the lossy case.
iii) The second and the third stubs were enough to obtain the insertion phase/amplitude control, and the third stub was used to obtain the input matching in the lossless case. This is still true for the lossy case.
iv) The loss performance of the TST shows peaks in the vicinity of the frequencies where the lengths of the open-circuited resonators of the TST are equal to $n\lambda/2$.

Based on the observations above, the following method is developed for the design of the insertion phase/amplitude controlling using the TST:

i) Find the initial points for the stub lengths for the desired insertion phase value using the formulation for the lossless case given in (4.7) to (4.10).

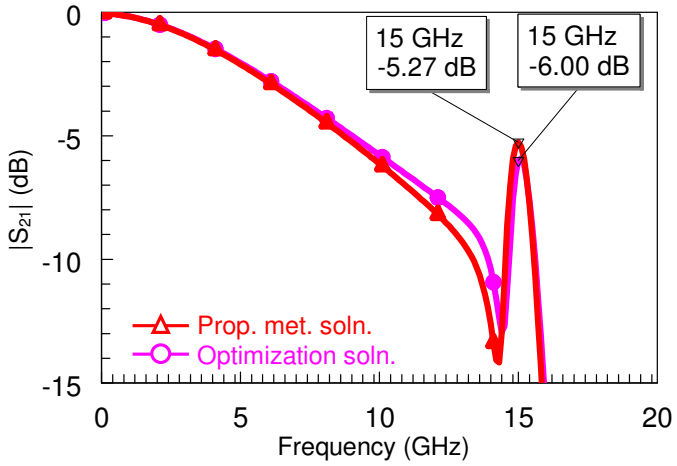
ii) Tune the interconnection line length, t, so that $x + y + t$, i.e., total length of the one of the shorter open-circuited resonators, is equal to $\lambda/2$ at the design frequency. $y + z + t$ or $x + z + 2t$ may also be used in some cases.

iii) Tune the lengths of the first and the third stubs in opposite directions; more clearly, tune z as $z \pm \Delta l$, meanwhile, tune x as $x \mp \Delta l$ as the S_{11} magnitude gets as small as possible.

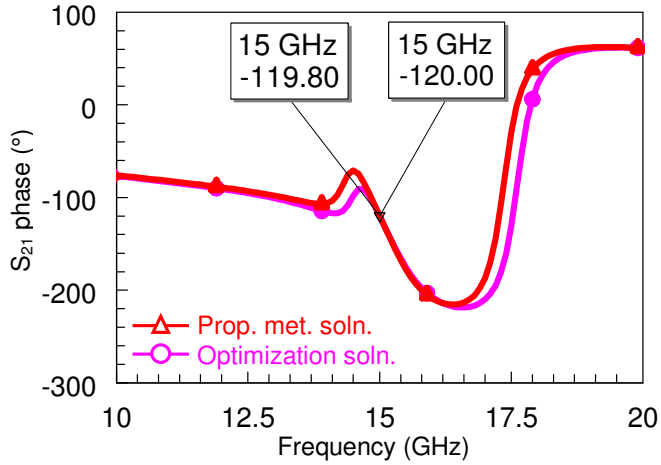
For the demonstration of the proposed method, a sample problem is presented. In the sample problem, S_{21} is targeted as (-6 dB, -120°). The problem is solved first with the optimization method, and then, with the proposed method. The performance comparison of the optimization solution with the proposed solution method is given in Figure 4.10. The line lengths obtained for both solutions are given in Table 4.3. The figures show that the proposed method can approximately guess the solution. The insertion phase is very close to the target value, and the return loss is acceptable. However, the amplitude response has some error. There is a trade-off between the insertion phase and the amplitude errors that come up with this method, and the designer can minimize the error in either the insertion phase or the amplitude of the input signal.

Table 4.3: The line lengths used in the TST circuit model that are obtained from the optimization solution and the proposed solution method.

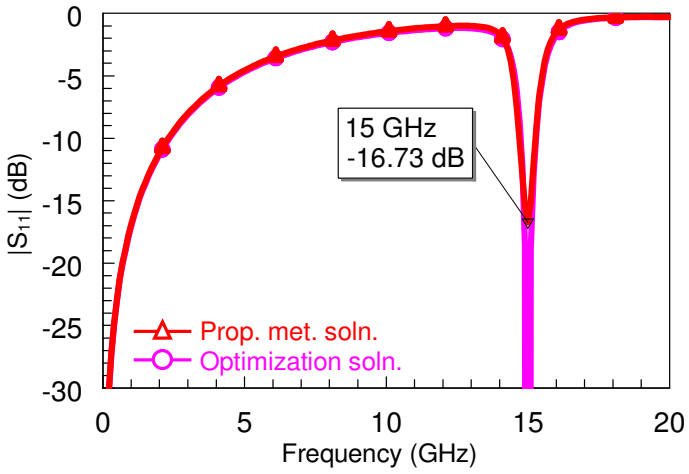
	Opt. Soln.	**Prop. Soln. Met.**
$x\ (\mu m)$	4241	4305
$y\ (\mu m)$	5169	5227
$z\ (\mu m)$	4267	4329
$t\ (\mu m)$	674.4	605.7
$\Delta l\ (\mu m)$	-	12.1
Loss peak (GHz)	14.83	14.79



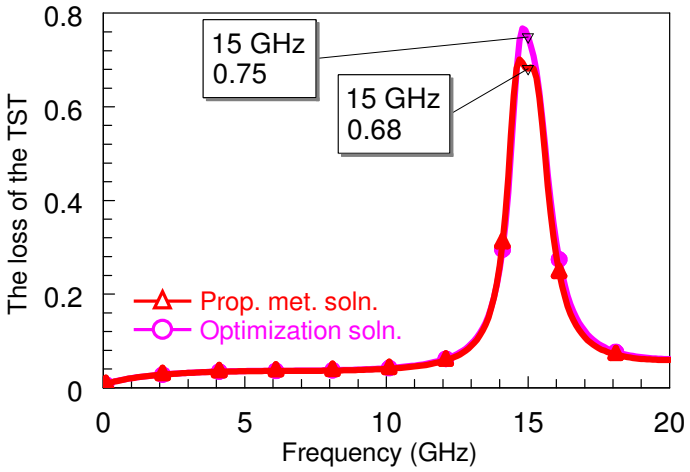
(a) $|S_{21}|$.



(b) $\angle S_{21}$ (unwrapped).



(c) $|S_{11}|$.



(d) The loss of the TST.

Figure 4.10: The performance of the proposed solution method for the insertion phase/amplitude control using the TST for (-6 dB/120°) state in the presence of transmission line losses (a) $|S_{21}|$ (b) $\angle S_{21}$ (c) $|S_{11}|$ (d) The loss of the TST.

4.4. Experimental Verification

4.4.1. The Design of the Single Metal Layer Triple Stub Topology Circuits

The experimental verification of the insertion phase/amplitude control using the TST concept is done by the implementation and the measurements of some sample TST based insertion phase/amplitude control circuits. The circuits include 14 sample insertion phase/amplitude states that are reconfigured as phase shifter, vector modulator, attenuator, and wider band design versions of these circuits.

For the design of the circuits, 50 Ω CPW lines have been used as the transmission lines. The dimensions of the CPW lines are G / W / G = 36 µm / 378 µm / 36 µm. The parameters of the CPWs are calculated using the formulation given in [172]. The CPW parameters that are used in the designs are Z_o = 50 Ω, $\varepsilon_{r,eff}$ = 2.36, α = 60 dB/m @ 20 GHz. The formulation given in [172] calculated the attenuation constant as α = 42 dB/m @ 20 GHz; however, α = 60 dB/m @ 20 GHz used in the

designs depending on the previous measurement experience. The circuits are implemented using CPW lines on quartz substrate with 0.8 µm-thick single metal layer, which is nothing but the first metal layer of the METU RF MEMS process that is detailed in Chapter 2.

T-junctions are used in each design at three points where the stubs are connected to the interconnection lines and the input/output ports. A special CPW T-junction is designed for this application. This special T-junction design is very important and definitely necessary for the proper operation of the designed circuits. If the T-junction design is not proper, the connection points would not behave as sections of transmission lines, which results with distortion from the expected performance of the circuit.

Figure 4.11 shows the layout of the T-junction, which is designed and simulated in HFSS v9.2. In the design, the grounds of the CPW lines are connected by wirebonds because the circuits are implemented using a single metal layer process, and it is not possible to use air-bridges in this process. The wirebond are modeled with a metallic strip that has 25 µm $\times$ 25 µm cross section area, which are used to simulate aluminum wirebonds with 25 µm diameter. The details about the design and the modeling of CPW T-junctions will be given in Chapter 5.2.1. The lengths of the transmission lines that are used to model the effects introduced by the T-junction are $x = 498.8$ µm and $y = 229.8$ µm, and the maximum error between the S-parameters of the circuits with and without T-junctions is 0.0003 in 1-20 GHz band.

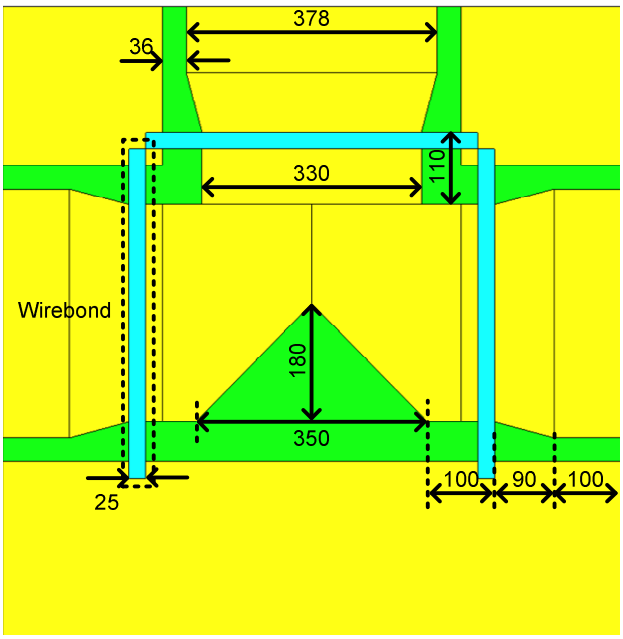


Figure 4.11: The layout of the T-junction that is designed for the single metal layer TST based insertion phase/amplitude control circuit. The dimensions are given in µm.

The circuits have been designed using the optimization method where the four optimization variables are the lengths of the three stubs and the interconnection line. The design procedure was explained previously in this chapter. There are 14 designs that are used to demonstrate some sample states of phase shifter, vector modulator, attenuator, and wider band versions of some of these designs. Table 4.4 shows the target insertion phase/amplitude values, the simulation results, the lengths of the stubs and the interconnection line, and the measurement results for each design. Figure 4.12 shows the layout of (-1 dB, 90°) state as an example.

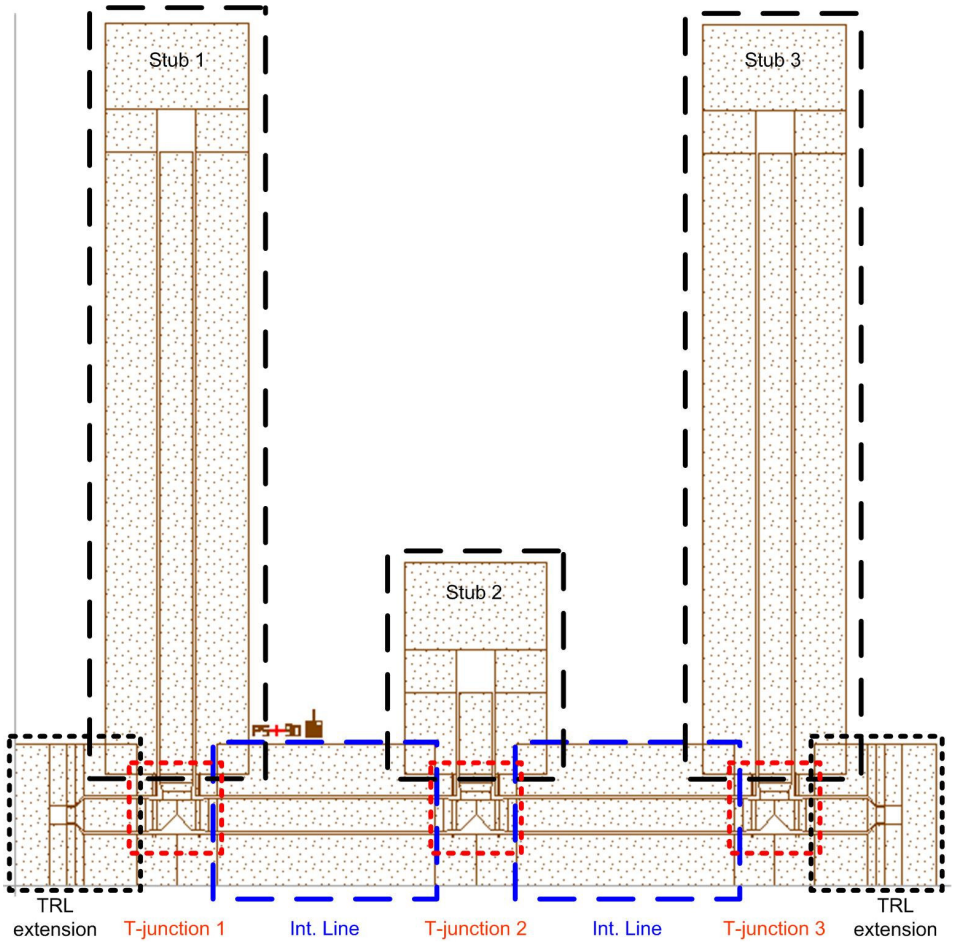


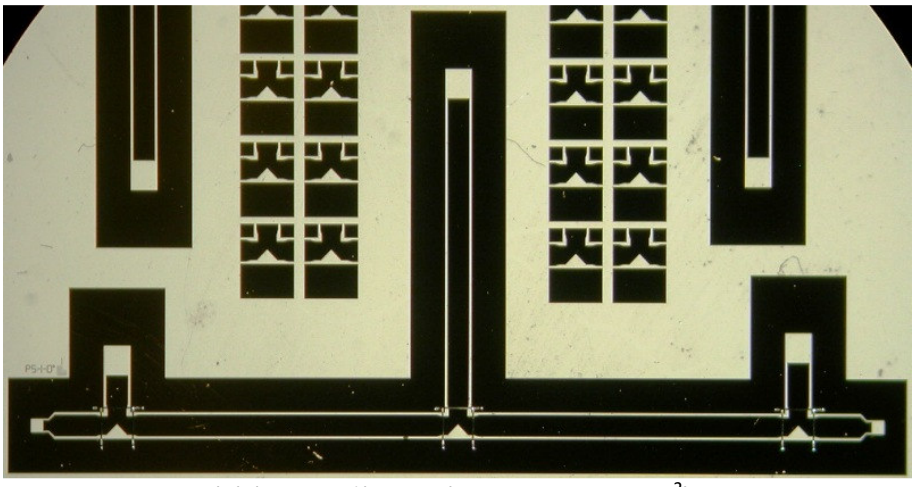
Figure 4.12: The layout of the single metal layer TST based insertion phase/amplitude control circuit, which is set for (-1 dB, 90°) state.

4.4.2. The Measurements of the Single Metal Layer Triple Stub Topology Circuits

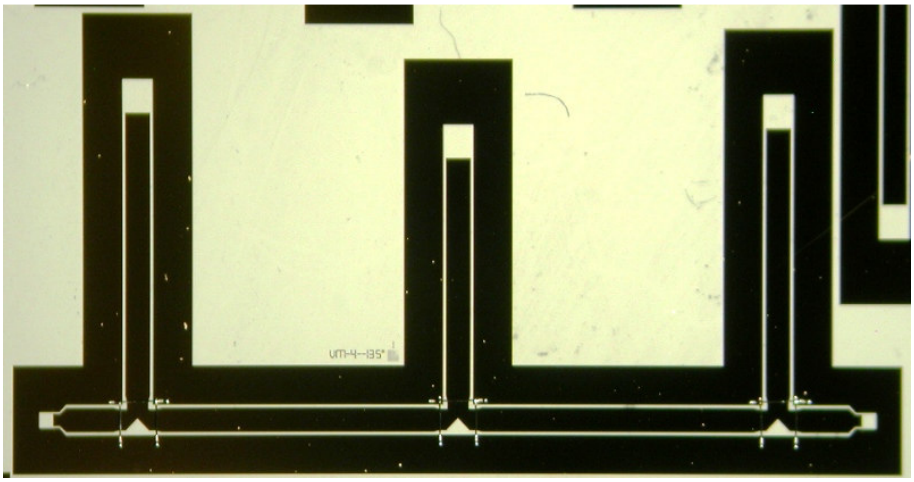
The designed TSTs are fabricated on 4" quartz substrate with single metal layer process. The metallization used is 0.8 µm-thick gold layer. The ground connections of the T-junctions of the TSTs are the aluminum wire bonds that are made with wedge bonding. The photographs of the fabricated single metal layer TST based phase/amplitude control circuits are given in Figure 4.13 for some example states.

Table 4.4: The summary of the simulation and measurement results of the TST insertion phase/amplitude control circuit designs that are implemented using single metal layer process.

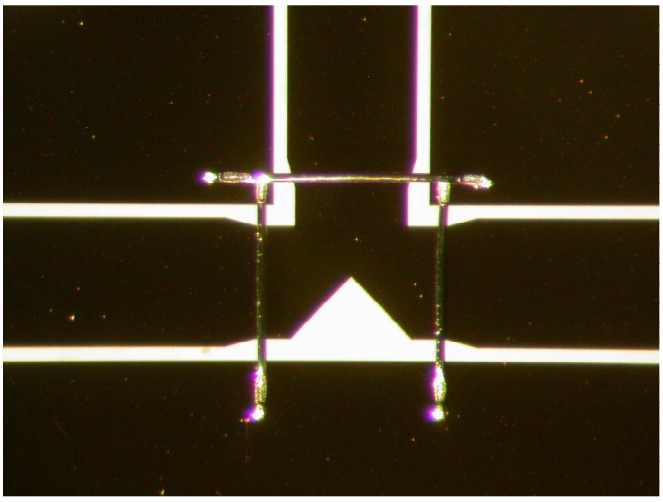
Target		Simulation							Measurement				
Mag (dB)	Ang (°)	S11	S21		Stb1	Stb2	Stb3	Int. Line	S11	S21		Freq.	Design No
		Mag (dB)	Mag (dB)	Ang (°)	LA2 (um)	LB2 (um)	LC2 (um)	mL (um)	Mag (dB)	Mag (dB)	Ang (°)	(GHz)	
PHASE SHIFTER													
-1	0	-287	-1	0	398.4	5170	636.7	4928	-15.3	-1.6	0	14.44	1
-1	45	-281	-1	45	5738	281.3	5666	4348	-28.2	-1.2	45	14.79	2
-1	90	-280	-1	90	7192	944.1	7173	2520	-28.4	-1.1	90	14.6	3
-1	180	-281	-1	180	7413	1476	7836	602.7	-24.8	-0.9	-179.9	14.55	4
VECTOR MODULATOR													
-6	90	-275	-6	90	8431	2618	8553	6906	-20.9	-5.6	90	14.64	5
-4	-135	-284	-4	-135	4169	3495	3939	3906	-24	-4.3	-135	14.43	6
-3	-90	-291	-3	-90	8101	3793	8064	6210	-12.7	-3.7	-90	14.69	7
-7	135	-275	-7	135	8468	9184	8356	6659	-29	-5.2	128.2	14.7	8
ATTENUATOR													
-9	0	-272	-9	0	1691	3963	2730	4487	-18.8	-10.5	0	14.46	9
-20	0	-278	-20	0	3742	9367	2641	4940	-12.7	-16	-7.9	14.43	10
WIDER BAND PS and VM (14.75-15.25 GHz)													
-1	90	-22	-1	90	0	237	0	3120	-29	-0.7	90	14.44	11
-1	0	-26.6	-1	0	6227	6341	6141	4981	-19.7	-1.3	1.8	14.75	12
-3	90	-15	-3	90	4350	7669	3963	4615	-25.3	-2.8	90.1	14.47	13
WIDER BAND ATTENUATOR (14.5-15.5 GHz)													
NA	-3	-16	-3	-	19110	5845	6177	15970	-33.9	-3.3	NA	14.84	14



(a) (-1 dB, 0°) state (Area: 15.4×8 mm^2).



(b) (-4 dB, -135°) state (Area: 13.4×7 mm^2).



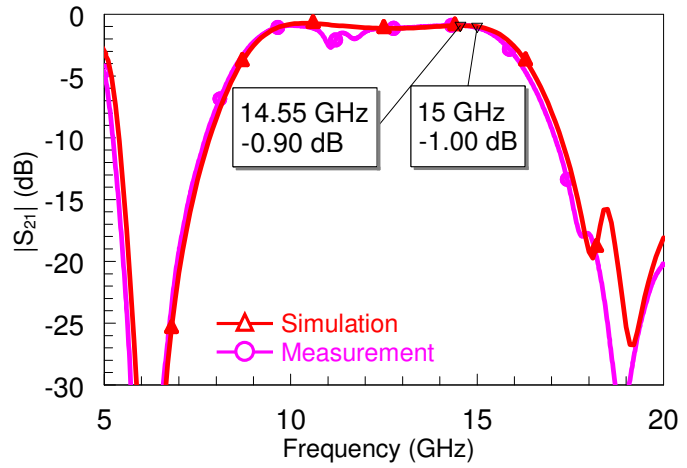
(c) The closer view of the T-junction and the wire bonded CPW ground connections.

Figure 4.13: The photographs of examples of the fabricated single metal layer TST based insertion phase/amplitude control circuits.

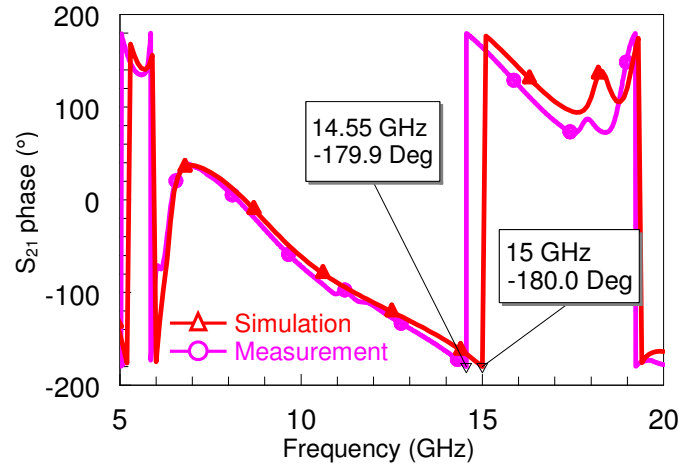
The fabricated samples are measured using Agilent 8361A network analyzer and Cascade Summit 9000 manual probe station. Cascade ACP-GSG-150 coplanar probes are used during the measurements. TRL calibration technique is applied for the measurements, and the measurements are made in 5-20 GHz frequency band.

The parameters of the 50 Ω CPW lines are extracted from the measurements of the CPWs that are fabricated on the same wafer with the TSTs. The extracted parameters for the line are Z_o = 50.4 Ω, $\varepsilon_{r,eff}$ = 2.43, and α = 58 dB/m @ 20 GHz. The characteristic impedance and the attenuation constant of the CPW lines are almost same as the calculated values, which are Z_o = 50 Ω and α = 60 dB/m @ 20 GHz; however, the effective permittivity is slightly higher than the design value, which was calculated as $\varepsilon_{r,eff}$ = 2.36.

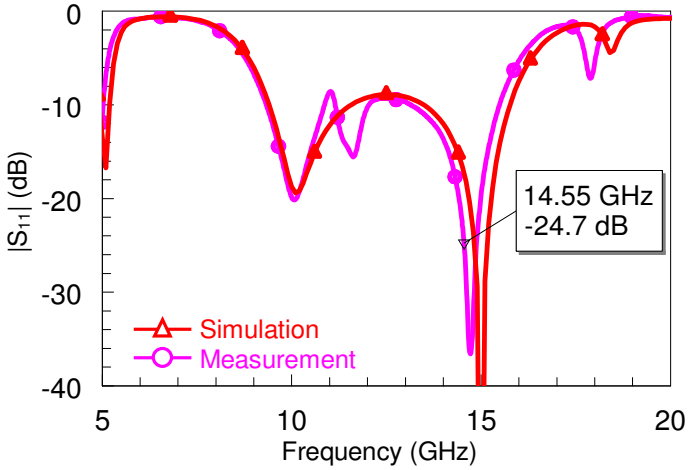
Figure 4.14, Figure 4.15, Figure 4.16, and Figure 4.17 show the measurement results of the fabricated TSTs. The figures prove that the desired performances are achieved from the circuits. Table 4.4 also shows the performance of all of the designed TST circuits.



(a) $|S_{21}|$.

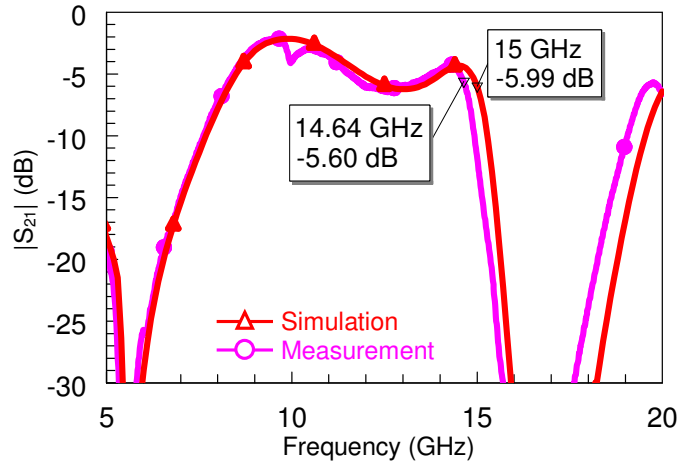


(b) $\angle S_{21}$.

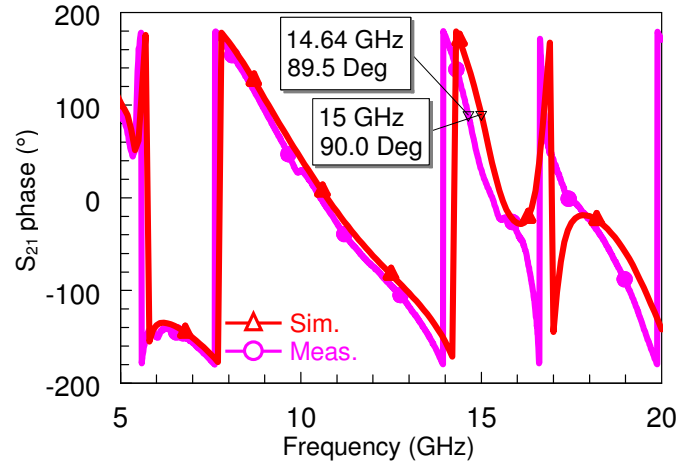


(c) $|S_{11}|$.

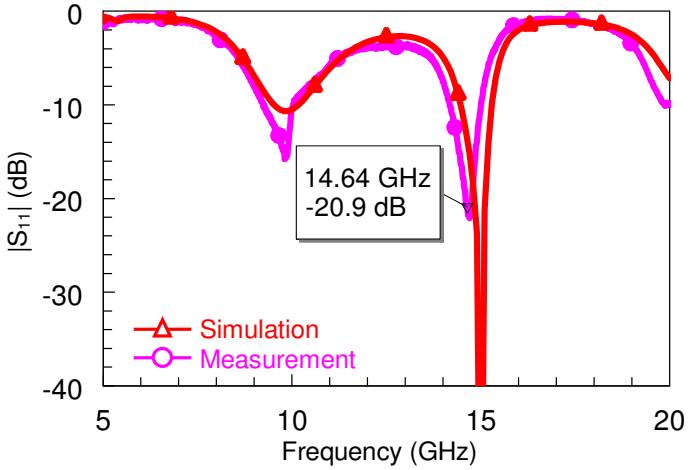
Figure 4.14: The measurement results of the TST based single metal layer PS for (-1 dB, 180°) state compared with the simulations (a) $|S_{21}|$ (b) $\angle S_{21}$ (c) $|S_{11}|$.



(a) $|S_{21}|$.

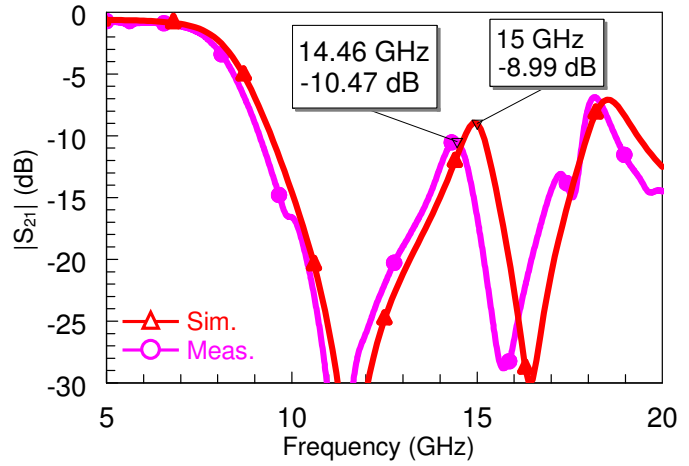


(b) $\angle S_{21}$.

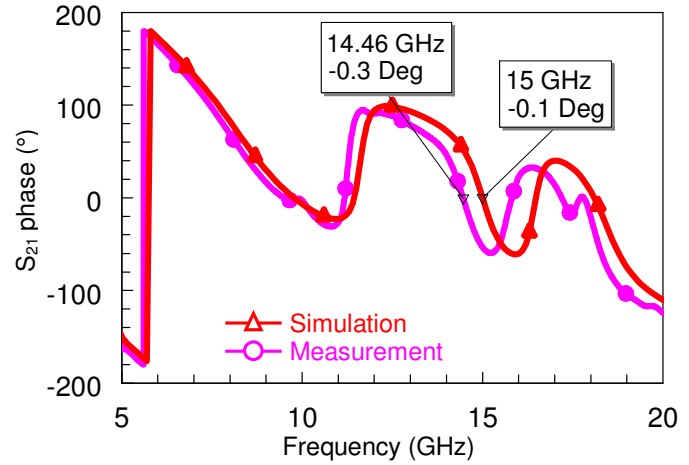


(c) $|S_{11}|$.

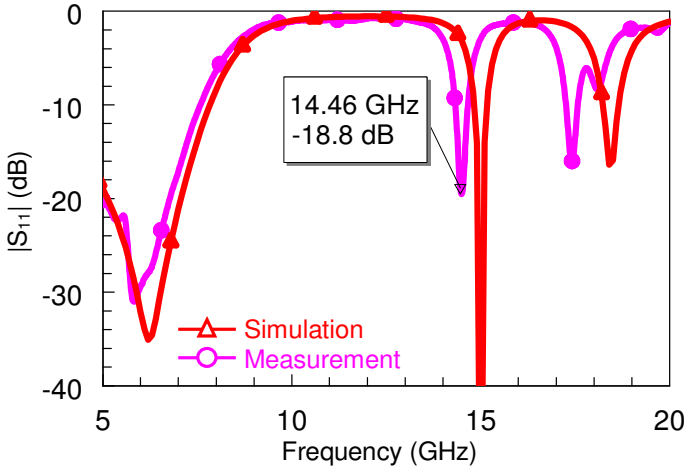
Figure 4.15: The measurement results of the TST based single metal layer VM for (-6 dB, 90°) state compared with the simulations (a) $|S_{21}|$ (b) $\angle S_{21}$ (c) $|S_{11}|$.



(a) $|S_{21}|$.

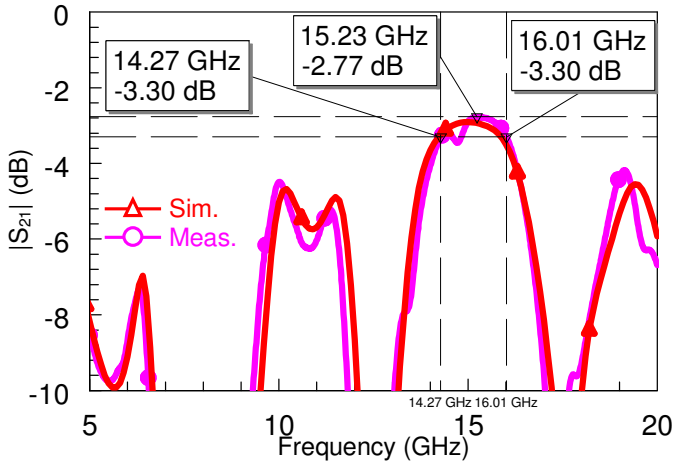


(b) $\angle S_{21}$.

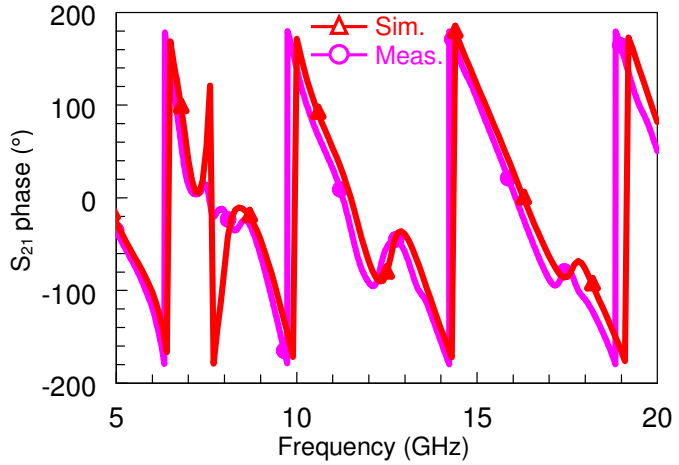


(c) $|S_{11}|$.

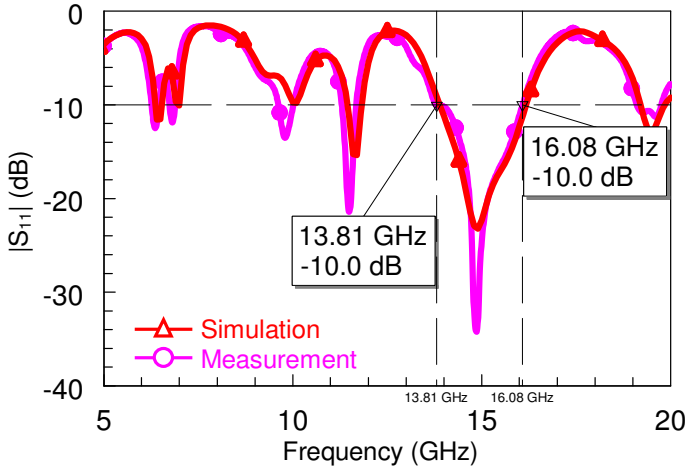
Figure 4.16: The measurement results of the TST based single metal layer attenuator without phase offset for (-9 dB, 0°) state compared with the simulations (a) $|S_{21}|$ (b) $\angle S_{21}$ (c) $|S_{11}|$.



(a) $|S_{21}|$.



(b) $\angle S_{21}$.



(c) $|S_{11}|$.

Figure 4.17: The measurement results of the TST based single metal layer wider band attenuator for (-3 dB) state compared with the simulations (a) $|S_{21}|$ (b) $\angle S_{21}$ (c) $|S_{11}|$.

Considering the performances that are given in the figures, some shift is observed in the frequency response of all of the circuits, and the desired performance is achieved at different frequencies for all circuits. These frequencies are slightly less than the center design frequency, which is 15 GHz. This situation has two reasons. The first one is that the effective relative dielectric constant used in the designs, 2.36, is lower than the measured one, 2.43. Therefore, all the CPW lines are electrically longer than the simulated ones, and the desired performance shifts to the lower frequencies. The second reason is the repeatability of the wirebonds. There are 3 wirebonds in each T-junction, which makes a total of $3 \times 3 = 9$ wire bonds for each circuit. These wirebonds are placed in a narrow area at the edge points of the CPW ground, and it is hard to repeat the positions and the heights of the wirebonds even from bond to bond. So, the changes in the positions and the heights of these bonds change the parasitic capacitance in each junction point; hence, the center frequency of each circuit slightly shifts in different amounts with respect to the design frequency.

4.5. Other Possible Application Areas

It is shown in the previous subsections that insertion phase and amplitude control is possible using TST while keeping the input impedance of the circuit equal to exactly Z_o. This allows us to use the idea to implement fixed phase shifter or vector modulators using one TST. However, the usage of the idea is not limited to this. It is shown in the second subsection of this chapter that it is also theoretically possible to control the insertion phase of the input signal while making Z_o-to-kZ_o impedance transformation, i.e., having different real input impedance. This is useful for designing some other useful circuits using the TST.

The concepts that are presented from this point on will depend only on the results of the lossless formulation for insertion phase control with Z_o-to-kZ_o

transformation. It was shown previously in this chapter that a solution can be found in the presence transmission line loss for all times even though the lossless formulation starts to fail at some insertion phase ranges. The formulation of the insertion phase control with Z_o-to-kZ_o transformation is very similar to that of with Z_o-to-Z_o transformation. As a result, it is believed that solutions can also be found for the insertion phase control with Z_o-to-kZ_o transformation in the presence of the transmission line losses, and it is unnecessary to show it one more time.

The circuits that are given next are for presentation of further applications of the proposed idea, and the details are not included here.

4.5.1. IQ Divider

Figure 4.18 shows the block diagram of the proposed "IQ divider" topology that uses TSTs. Two TSTs are used in the proposed topology, which are used to transform Z_o-to-$2Z_o$ while the insertion phases of the two arms are set as 0° and 90°. In this case, the impedance at the input port is equal to Z_o, and the power is divided equally as the input impedances at the two arms are real and equal to each other. Since the insertion phases of the two arms are set as 0° and 90°, one of the arms will be the inphase signal where the other will be the quadrature signal.

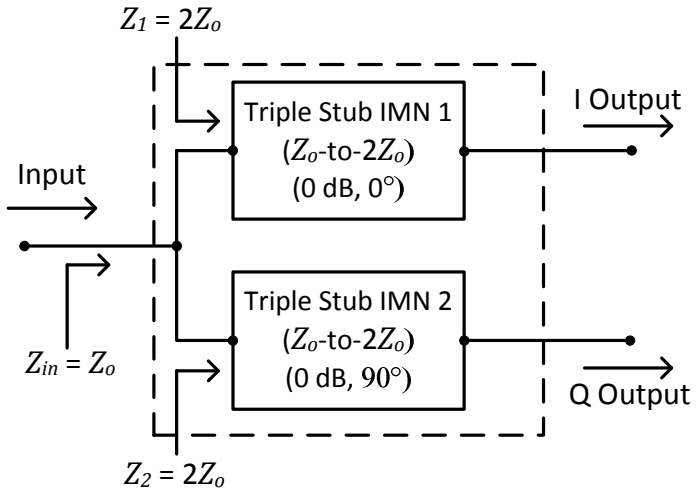


Figure 4.18: The block diagram of the proposed "IQ Divider" topology that uses TSTs.

4.5.2. 1:*k* Power Divider

Figure 4.19 shows the block diagram of the proposed "1:k Power Divider" topology that uses TSTs. Two TSTs are used in the proposed topology, which are used to transform the input admittance of the two arms as Y_o-to-G_1 and Y_o-to-G_2. The sum of G_1 and G_2 should be equal to Y_o for the input matching as given in (4.20), and the power will be divided proportionally with the ratio of the real parts of the input admittances of the two arms as given in (4.21). Solving these two equations, it is found that G_1 and G_2 should be selected as given in (4.22). The insertion phases are not important for this case; they can either be set both to 0° for inphase operation at the two arms, or they can be set free to any insertion phase values, ϕ_1° and ϕ_2°.

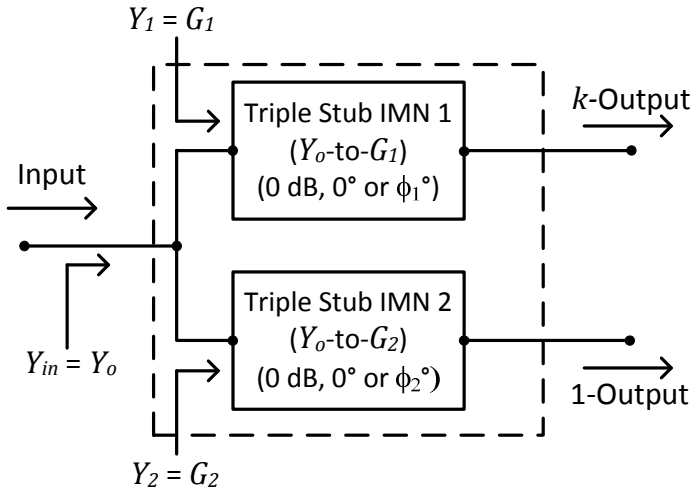


Figure 4.19: The block diagram of the proposed "1:k Power Divider" topology that uses TSTs.

$$Y_{in} = G_1 + G_2 = Y_0 \tag{4.20}$$

$$Power\ ratio = \frac{G_1}{G_2} = k \tag{4.21}$$

$$G_1 = \frac{k}{k+1} Y_0, G_2 = \frac{1}{k+1} Y_0 \tag{4.22}$$

4.5.3. Vector Modulator Type I

Figure 4.20 shows the block diagram of the proposed "Vector Modulator Type I" topology that uses TSTs. Two TSTs are also used in the proposed topology, which are used to transform the input admittance of the two arms as Y_o-to-G_1 and Y_o-to-G_2. The G_1 and G_2 should be selected as in the 1:k power divider topology. The insertion phases should be set as either 0° or 180° and either 90° or 270° for the upper and the lower arms, respectively. This is necessary for the vector modulator to cover all four quadrants of the polar space.

Setting the arms as explained above, the input signal will be divided into two arms orthogonally with the desired ratio while the impedance at the input port will be equal to Z_o. And finally, combining these two signals with an inphase combiner, the vector modulator operation can be achieved.

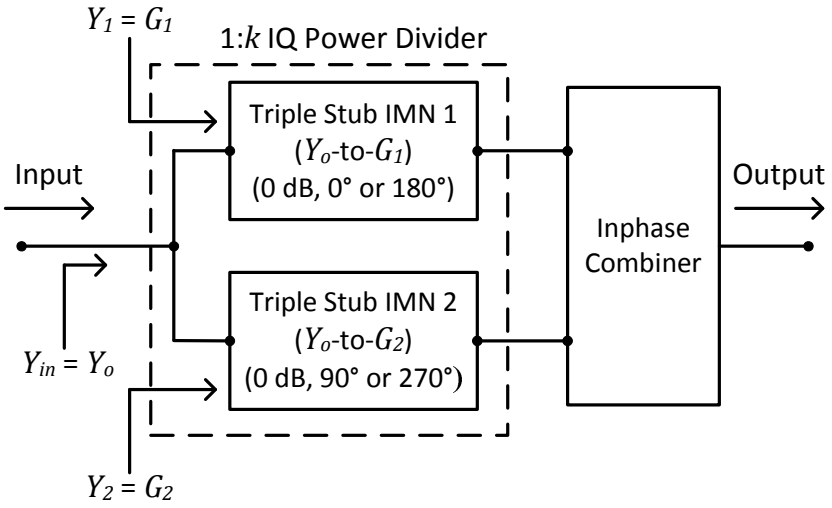


Figure 4.20: The block diagram of the proposed "Vector Modulator Topology I" that uses TSTs.

4.5.4. Vector Modulator Type II

Figure 4.21 shows the block diagram of the proposed "Vector Modulator Type II" topology that uses TSTs. Two TSTs are again used in the proposed topology, which are used to transform the input admittance of the two arms as Y_o-to-G_1 and Y_o-to-G_2. The G_1 and G_2 should be also selected as in the 1:k power divider topology in this case. The insertion phase at the output arm should be set to the required insertion phase, ϕ_{req}, and the insertion phase at the termination arm should be set to any values, ϕ_3°.

Setting the arms as explained above, the input signal will be divided into two arms with the desired ratio. This will result with transferring the necessary amount of

power to the upper arm. The upper arm will be the output arm, and it will be used to control the insertion phase of the output signal. The lower arm is used to terminate the amount of power that is left from the upper arm.

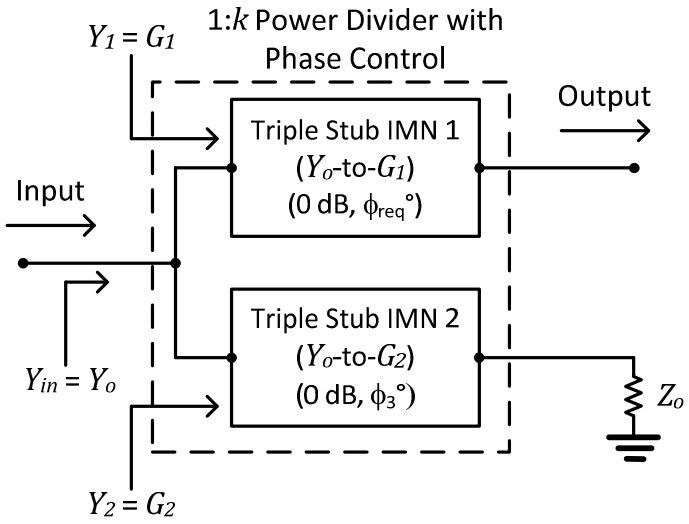


Figure 4.21: The block diagram of the proposed "Vector Modulator Topology II" that uses TSTs.

4.6. Conclusion

In this chapter, it is shown that it is possible to control the insertion phase and the amplitude of an input signal while keeping the input impedance equal to any desired real impedance using the TST. The analytical solutions for both phase and amplitude control are examined, and the solution for the insertion phase control for the lossless case is presented. The solution for the lossy case, which is actually the amplitude control case, does not give explicit equations; however, a design methodology is developed in the presence of losses. The reasons of the losses are discussed in detail. For the experimental verification, phase shifters, vector modulators, and attenuators are designed for a single metal layer process. The

measurement results of the fabricated structures verified the proposed idea. Finally, other possible application areas of the proposed idea are presented.

CHAPTER 5

RF MEMS PHASE SHIFTER USING TRIPLE STUB TOPOLOGY

5.1. Introduction

The idea of using triple stub topology as insertion phase and amplitude control circuit brings the opportunity to implement novel reconfigurable phase shifters that have a large insertion phase range with fine phase resolution. Achieving these specifications requires precise control of electrical lengths of the transmissions lines, which necessitates many switching components. At this point, MEMS technology is the best alternative since the MEMS technology offers low-loss, high-performance capacitive switches ([5], [8]-[15]), and therefore, using a high number of switches do not increase the insertion loss considerably.

In this chapter, a novel RF MEMS phase shifter that uses the TST is presented. In this topology, the electrical lengths of the stubs of the TST and the interconnection lines between the stubs are adjusted by means of distributed MEMS transmission lines (DMTL) [22]-[28]. By this way, insertion phase can be adjusted as explained in the previous chapter. In the following parts of this chapter the details of the design are explained and the details of the fabrication are given together with the measurement results, and finally, the measurement results are examined.

5.2. The Design of the RF MEMS Phase Shifter

Figure 5.1 gives the block diagram of the RF MEMS phase shifter (PS). This PS is composed of three main building blocks; (i) DMTL interconnection lines, (ii) DMTL stubs, and (iii) the connecting T-junctions. All of these components are very critical and directly affects the performance of the PS; so, each component is designed separately. Then, the component performance is verified as a part of the PS by cascading the S-parameters of all of the components in a circuit simulator, which is, in this case, Microwave Office (MWO) [175].

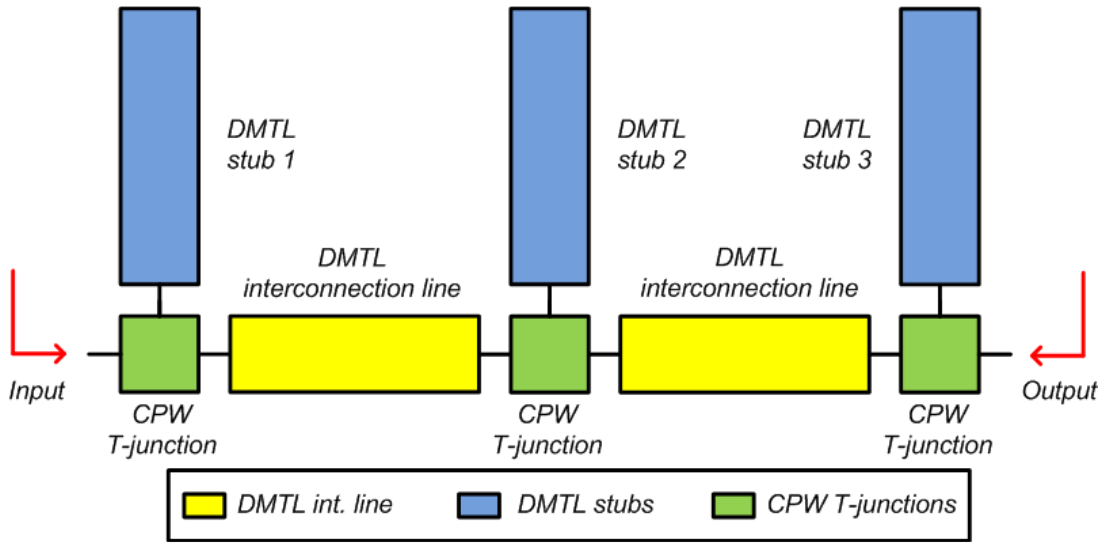


Figure 5.1: The block diagram of the RF MEMS phase shifter.

The PS is controlled digitally because all of the unit sections of the DMTLs are either in *on* or in *off* states. In the DMTL stubs, all of the unit sections are controlled independently, and these unit sections are used to obtain the required reflection coefficient at input of the corresponding stub. On the other hand, the unit sections of DMTL interconnection lines are controlled in groups because the overall impedance of these lines should not be altered significantly while adjusting the electrical lengths, i.e., the insertion phase, precisely. The importance of keeping the

characteristic impedance in the same level was explained in the previous chapter. It should also be emphasized at this point that, the DMTL interconnection in the PS design is *used to change the electrical length, i.e., the insertion phase*, and hence, it is not used as a *differential phase shifter*.

Transmission lines are implemented as coplanar waveguides (CPW) because it is easier to implement DMTL using CPWs. 15 GHz is chosen as the center frequency, and *0-360° phase range coverage with 10° resolution is aimed*, which requires at least *5-bit digital control*. The resolution can be increased without altering the structure. The limiting point in resolution is the phase error which is an *absolute value*. It should be mentioned here that the phase shifter operation is not limited to center design frequency, 15 GHz. Since the electrical lengths of the DMTL interconnection lines and DMTL stubs are reconfigurable, it is also showed in this thesis that the phase shifter can work up to 40 GHz. In the following subsections, the design of each part is explained in detail.

5.2.1. The T-Junction Design

The discontinuity at the connection points of planar transmission lines are subject to mode conversion. The mode conversion may result with unexpected increase in the insertion and return losses at the junction point ([178], [179]). Moreover, T-junctions may affect the electrical lengths of the stubs and the interconnection lines between the stubs, which should be precisely adjusted to achieve the desired insertion phase from the PS. As a result, the T-junction design is a critical part of the PS design.

A number of methods have been used in order to reduce the mode conversion in CPW T-junctions [179], and one of the most commonly used methods is using air bridges. Connecting the grounds of the CPW in the vicinity of the junction by air

bridges decreases the unwanted parasitic modes. The air bridges can easily be implemented using the RF MEMS process, and hence, is chosen for the T-junctions of the PS design.

A special CPW T-junction is designed for the connection points between the DMTL stubs and the DMTL interconnection lines, the layout of which can be seen in Figure 5.2. MEMS air bridges are used to connect the grounds of the CPW and the CPW center conductor is narrowed. Moreover, a notch is opened at the connection point on the thru line direction. This layout minimizes the effects of the parasitics that occur at the junction point.

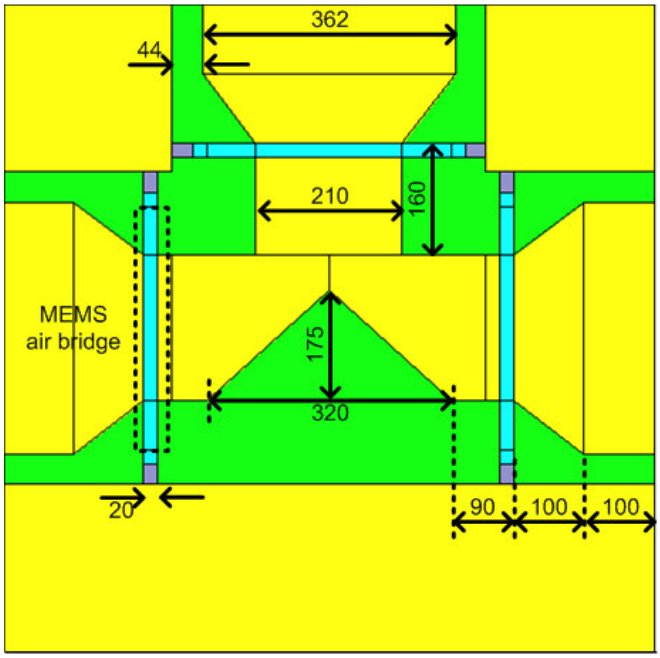


Figure 5.2: The layout of the designed T-junction. The dimensions are given in µm.

The reason of using air bridges was explained above. The reason of using narrower lines and the notch can be understood better by examining the electrical model of the T-junction, which is given in Figure 5.3 [179]. In the model, $C_{air\text{-}bridge}$ is used to model the parasitic capacitances brought by the air bridges, $C_{junction}$ is used to model

the fringe capacitance occurring at the junction point, and the L_1 and L_3 are used to model the change in the current densities at the junction point. The T-junction is a strong discontinuity and it affects the PS performance significantly, therefore a fundamental solution is to design the T-junction such that it only behaves as connection of three 50 Ω transmission lines. With this solution, the equivalent electrical lengths of the T-junction arms are subtracted from the required electrical lengths of the interconnection lines and the stubs. For this purpose, a notch is used at the junction point in order to reduce $C_{junction}$ as much as possible, and the center conductors of the CPWs are narrowed to change L_1 and L_3 so that these inductances compensates the $C_{air\text{-}bridge}$ and the $C_{junction}$.

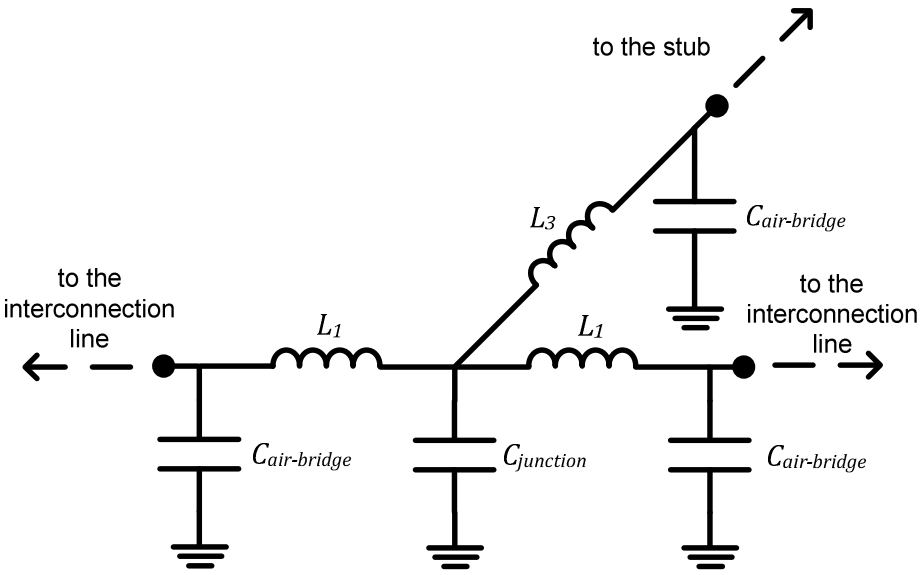


Figure 5.3: The electrical model of the T-junction discontinuity.

The T-junction is designed using HFSS v9.2 [176]. The design parameters are the width and the position of the MEMS air bridge, the width and the depth of the notch, and the width of the narrowed CPW center conductor. An iterative design method is followed. The T-junction simulation results are substituted into the PS design, and the simulation results with and without T-junctions are compared. The

circuits that are used to evaluate the performance of the T-junctions are given in Figure 5.4.

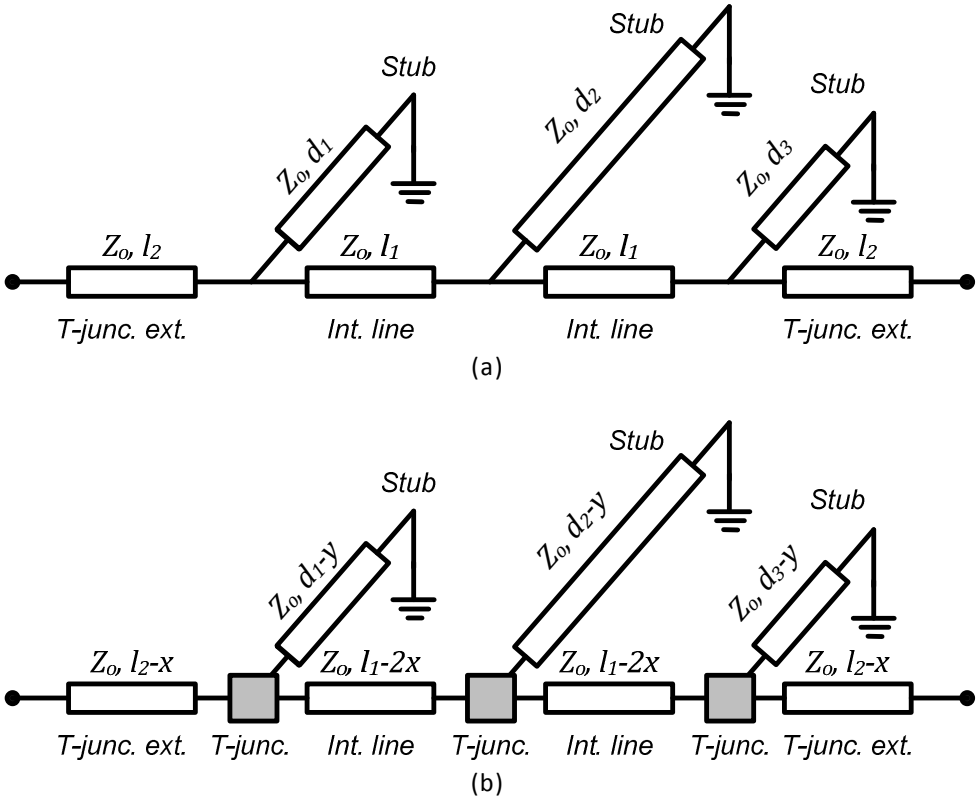


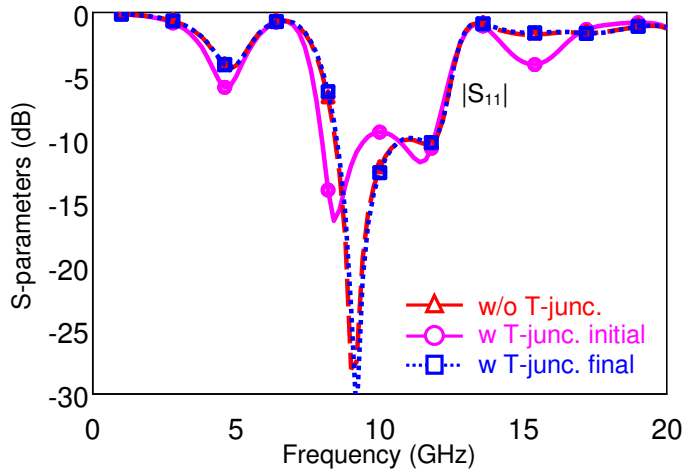
Figure 5.4: The PS models that are used to compare the effects of the T-junction: (a) The PS without T-junction (b) The PS with T-junction.

The T-junction design method is as follows: the PS is simulated using the circuit model given in Figure 5.4-(a) in MWO, where l_1, l_2, d_1, d_2, and d_3 are fixed to some predefined lengths. Then, the EM, HFSS v9.2, simulation results are inserted in the PS circuit model as shown in Figure 5.4-(b). Following this step, the error between the S-parameters of the two circuits, which is defined as the "average *squared* magnitude of the difference between each element of the S-parameter matrix" in this case, is minimized by optimization. The optimization is made using the Simplex Optimization tool of the MWO [175], and the optimization parameters are x and y

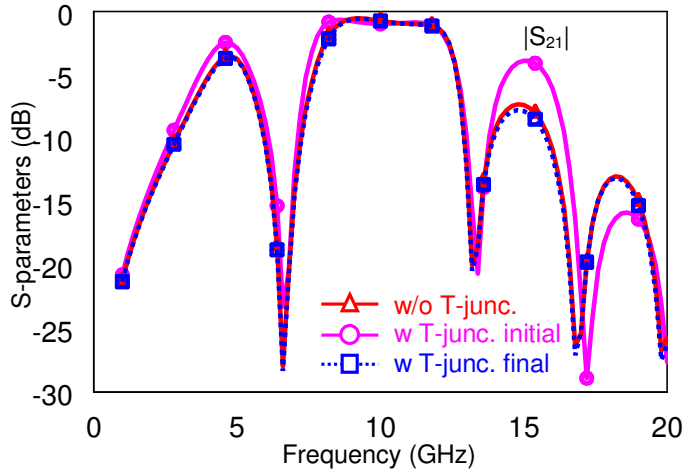
in Figure 5.4-(b), i.e., the lengths of the extra 50 Ω transmission lines that are subtracted from the original line lengths in order to compensate the presence of the T-junction.

In order to demonstrate the necessity of such a complicated design for the T-junction, the simulation results of the T-junction with MEMS air bridges only, which is the initial design, is compared with that of the final design, the layout of which was given in Figure 5.2. Figure 5.5 shows the S-parameters and the error between S-parameters of the PS for the cases without any T-junction, with the initial T-junction design, and the final T-junction design. The line lengths are given in Table 5.1. As can be seen in the figure, the error between the S-parameters for the initial design case, which is seen on the right axis, is much bigger than that of the final design case. The difference can also be easily observed on the S-parameters. It should be pointed out here that l_1, l_2, d_1, d_2, and d_3 set was selected randomly; in spite of this, the T-junction still works for *any* set of these variables, and the error does not change considerably.

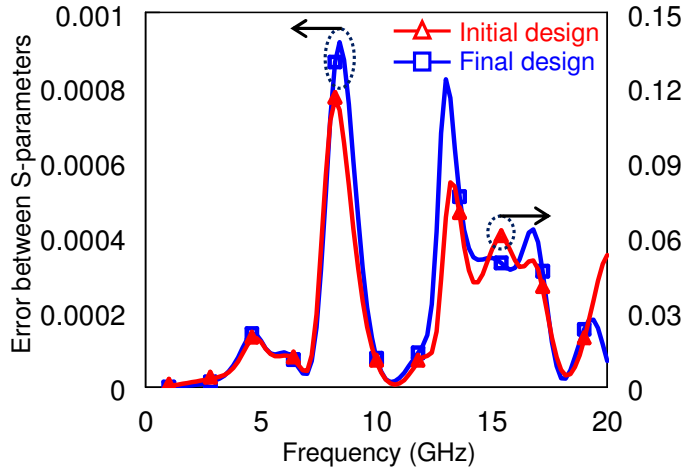
Considering the performance of the final design, this T-junction is selected to be used in the RF MEMS PS design.



(a) $|S_{11}|$.



(b) $|S_{21}|$.



(c) The error between the S-parameters.

Figure 5.5: The comparison of the S-parameters of the PS for with and without T-junction cases: (a) $|S_{11}|$ (b) $|S_{21}|$ (c) The error between the S-parameter of the two cases.

Table 5.1: The line lengths used in the PS model for the comparison of with and without T-junction cases. All the parameters are given in μm.

	Initial Design	Final Design
d_1	14500	14500
d_2	5700	5700
d_3	3700	3700
l_1	2500	2500
l_2	1000	1000
x	731.7	694.9
y	367.6	356.1

5.2.2. The DMTL Interconnection Line Design

DMTLs are one of the most widely used MEMS components. Although the most popular application area is the phase shifters, DMTLs are also demonstrated in resonators, filters, and impedance matching networks, the examples of which were given in Chapter 1. The main application areas of the DMTLs are phased arrays, radars, wireless communication systems, and measurement instruments in a very large frequency band starting from X-band up to W-band.

Operation principle of the DMTL is based on the theory of periodic structures ([172], [180]), which is actually means loading a transmission line periodically with reactive elements so that by changing the reactance of the loading elements, the phase velocity of the wave travelling inside the structure can be adjusted. The reactive element in the DMTL is the MEMS switch. Using MEMS switches as tunable capacitors, in which case the capacitance of the switch is tuned by changing the applied voltage, the phase velocity of the travelling wave can be controlled in an *analog* manner [22]-[23]. However, the maximum phase shift that can be obtained from this structure is limited by the capacitance tuning range of the MEMS switches, which is theoretically limited to 1.5 for standard switches caused by the mechanical instability of the MEMS switches [23]. On the other hand, *digital* type DMTL structure have also been presented in the literature ([24], [25], [27], [28]), in

which the MEMS switch is serially connected to another static MEMS capacitor and is used to select one of the two equivalent capacitance levels by holding the switch either in on or off states. In this case, the capacitance tuning range can be increased to 2.5 [27], which means that more phase shift can be obtained from one DMTL unit section. This also means that the degree per dB, shortly °/dB, performance of the structure is better in the digital case ([181], [142]). Moreover, the digital type structure shows stronger resistance to electrical and mechanical noise coming from the analog control of the MEMS structure [182]. Considering the performance of the digital type MEMS phase shifters, it is also selected as to change the electrical length, i.e., the insertion phase, of the interconnection line of the RF MEMS PS designed in this thesis.

Figure 5.6 shows the basic circuit model of a unit section of a digital type DMTL. In the model, sR_t, sL_t, and sC_t are the per unit length parameters of the unloaded transmission line, which is the CPW in this case. The unloaded transmission line is loaded by two MEMS capacitors, which are C_b and C_s. C_b represents the capacitance of the MEMS switch whereas C_s represents the capacitance of the static MEMS capacitance, which is, in this case metal-air-metal (MAM) capacitors. Since the unloaded CPW is *loaded* by two capacitances that are connected in series, the parameters of the equivalent structure are modified forming a new distributed transmission line structure. The loaded impedance and the phase velocity of a loaded transmission line are given in (5.1) and (5.2), respectively.

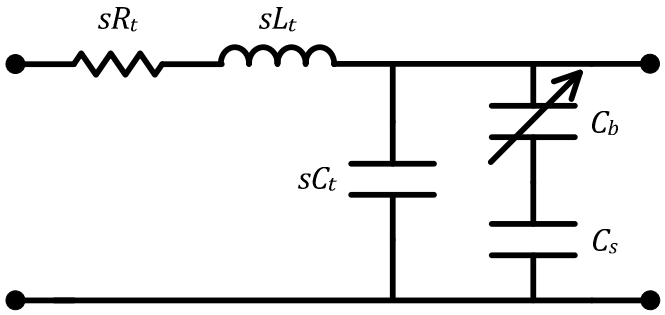


Figure 5.6: The circuit model of a unit section of a digital type DMTL.

$$Z_l = \sqrt{\frac{sL_t}{sC_t + \frac{C_b C_s}{C_b + C_s}}} \tag{5.1}$$

$$v_p = \frac{s}{\sqrt{sL_t\left(sC_t + \frac{C_b C_s}{C_b + C_s}\right)}} \tag{5.2}$$

The standard design methodology of the digital type DMTL starts with the selection of the Bragg frequency, which is given in (5.3), since it is the upper limit for the periodic structure [180]. The safe way is to select Bragg frequency as more than twice the center frequency of the DMTL. The upstate and the downstate characteristic impedances, Z_{lu} and Z_{ld}, are also selected as to stay in an acceptable return loss level, which is usually selected as -15 dB. The calculated impedance levels for upstate and downstate are 60 Ω and 42 Ω, respectively [27]. Then, the phase shift per unit section of the DMTL can be found using (5.4).

$$f_B = \frac{1}{\pi\sqrt{sL_t\left(sC_t + \frac{C_b C_s}{C_b + C_s}\right)}} \tag{5.3}$$

$$\Delta\phi = \frac{s2\pi f_0 Z_0\sqrt{\varepsilon_{eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) rad/section \tag{5.4}$$

The design parameters such as the periodicity, the static MAM capacitance, C_s, and the MEMS switch capacitance, C_{bu}, can be found using (5.5)-(5.7). The reader is encouraged to see [142] for an extensive analysis and a good example of the DMTL design.

$$s = \frac{Z_{ld} c}{\pi f_B Z_0 \sqrt{\varepsilon_{eff}}} \tag{5.5}$$

$$C_s = \frac{Z_0^2 - Z_{ld}^2}{\pi f_B Z_0^2 Z_{ld}} \tag{5.6}$$

$$C_{bu} = C_s \frac{Z_{ld}^2 \left(Z_0^2 - Z_{lu}^2\right)}{Z_0^2 (Z_{lu}^2 - Z_{ld}^2)} \tag{5.7}$$

Although the standard design methodology explained above is well-suited and proven for the DMTL design, a different method has been followed during the design of the DMTL section that is used in the RF MEMS PS design. This is because the RF MEMS PS DMTL interconnection line sections have different design requirements and limitations.

First of all, the RF MEMS PS design requires a specific *insertion phase* between the stub connection points for a predefined phase shift value of the whole structure. Hence, the important parameter for the DMTL interconnection line is *not only the differential phase shift, but also the upstate insertion phase* of the DMTL interconnection line.

Secondly, a high phase resolution is required for the DMTL interconnection line since the phase performance of the PS is very sensitive to small changes in this parameter. It is required by (4.7) to (4.10) that in order to obtain the targeted insertion phase range of the designed PS, i.e., 0-360° range with 10° resolution, the electrical length of the interconnection line should be changed between 0 and λ/2

with minimum λ/100 steps. This is requirement is valid when the minimum insertion loss point is targeted for each phase state of the PS. This means that the DMTL interconnection line should have (λ/2) / (λ/100) = 50 unit sections, which has 180°/50 = 3.6° phase resolution. Let us assume that 6.125° resolution, which is equivalent to 6-bit controlled phase shifter, is enough instead of 3.6°. Applying the above DMTL formulation for a 60 Ω-40 Ω design at 15 GHz with a Bragg frequency of 35 GHz results with periodicity of s = 740 μm. This results with a total DMTL interconnection line length of 32 x 740 = 23690 μm. Taking into account that two of these DMTLs will be used in the design, this approach is inapplicable in the sense that the design becomes infeasible to fabricate; moreover, the insertion loss will increase significantly.

Other than the above mentioned facts, there are also other limitations that are related with the measurement and packaging of the PS, which should be taken into account during the design. The PS has many DC control connections that are used to actuate the MEMS switches, and these connections should be somehow connected to the outer world for the measurements. This can be done in two ways, (i) using a probe card in the probe station and (ii) connecting the fabricated design into an integrated circuit (IC) package that allows the connection of many DC controls. Using a probe card is not feasible since each design necessitates a different probe card. The multi-pin MEMS automated measurement system (MAMS), which was explained in Chapter 3.3.2, will be used for the measurement of the designed PS. The MAMS allows 32 DC control pins simultaneously; so, this is also a design constraint for the PS. Additionally, the packages that the PS will be mounted have standard window sizes excluding the custom packages, and the maximum available window sizes limit the area of the PS design.

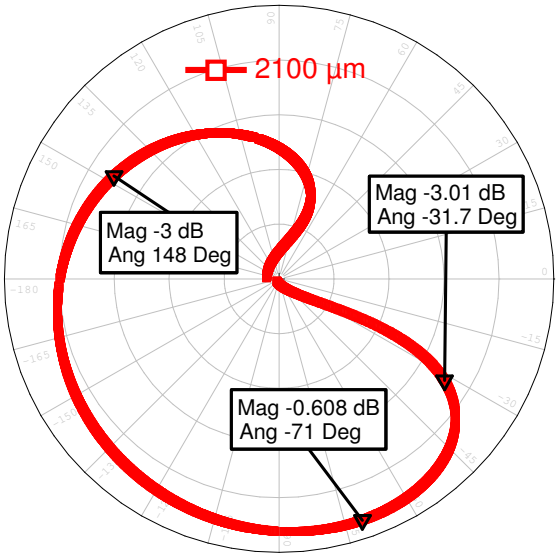
The design constraints explained above makes the usage of a standard digital type phase shifter impossible for the DMTL interconnection line, which means that an alternative approach is needed. For this purpose, a DMTL that has a lower insertion

phase range and a smaller area is designed. The design has a total of 8 unit sections, which are controlled by 5 pins. It uses two types of DMTL unit sections that are designed to give 5° and 10° differential phase shifts per unit section, respectively. The designed DMTL interconnection line gives an insertion phase of -115° and -178° when all the MEMS switches are in upstate and downstate, respectively.

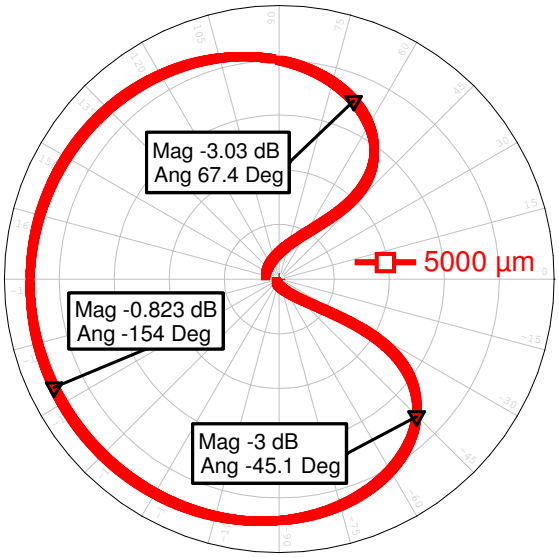
The reason behind selecting the aforementioned insertion phase range and the number of unit sections is understood better if the phase shifter theory, which was given in the previous chapter, is investigated in more detail. It is theoretically known that the interconnection line length should be changed between 0 to $\lambda/2$ in order to obtain 0-360° insertion phase range. However, the interconnection line length that is necessary in order to obtain one specific insertion phase value with minimum insertion loss also works for the neighboring insertion phase values. In other words, once the electrical length of the interconnection line length is fixed to some value, a range of insertion phase can be realized with the PS. But, this range is not constant and depends on the interconnection line length. The range is maximum when the interconnection line length is about $\lambda/4$, and it decreases as it goes towards either 0 or $\lambda/2$, which can be seen in Figure 5.7. The range becomes so small near 0 or $\lambda/2$ that the electrical length of the interconnection line should be exactly what is required by the formulation in order to obtain the desired insertion phase. So, during the interconnection line design, the electrical length is targeted to stay in 0-to-0.1λ and 0.4λ-to-0.5λ, which is equivalently about from -145° to -215°, and this range is covered by 5° steps to be able to cover the range accurately.

The electrical length of the interconnection line is determined by the length of the DMTL interconnection line and the extensions of the T-junctions at each stub connection point. The additional transmission lines that come from both sides of

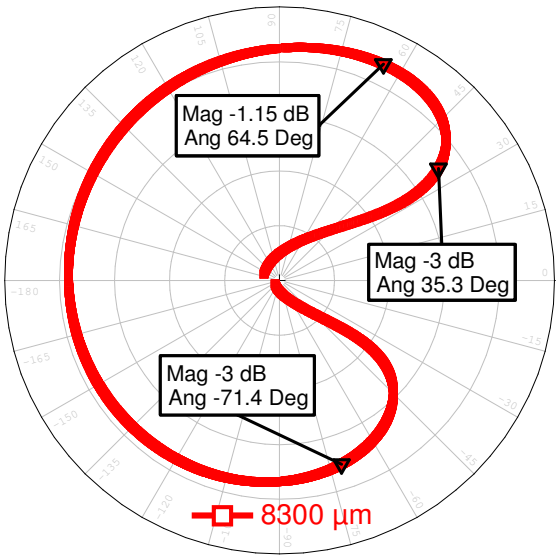
the T-junction add 2 x -20 = -40°. Adding the value to the insertion phase coming from the extensions, the interconnection line has a total insertion phase between -115 - 40 = -155° and -178 - 40 = -218°.



(a) 0.105λ = 2100 µm.



(b) 0.25λ = 5000 µm.



(c) 0.415λ = 8300 µm.

Figure 5.7: The S_{21} of the ideal TST based PS with different interconnection lines lengths. The figures show two insertion phase values when the insertion loss is minimum and when the insertion loss is equal to -3 dB.

Having identified the design requirements and targets, the next step is to design the DMTL unit sections. Two types of unit sections, which are named as *DMTL Unit Section Type I* and *Type II*, are designed for the DMTL interconnection line that give 5° and 10° differential phase shift per unit section, respectively. DMTL Unit Section Type I (UST-I) is used to decrease the size of the phase steps, and two unit sections of UST-I are used. All of the other remaining six unit sections are DMTL Unit Sections of Type II (UST-II).

The design of the DMTL unit sections begins using the formulation (5.1)-(5.7), which is followed by verifying the results using the circuit model that is given in Figure 5.8. Some key points should be considered here. First, the Bragg frequency should be adjusted so that the upstate insertion phase is not lower than -14° in order not to exceed -115°. Secondly, the differential phase shift should be 5° and 10° for UST-I and UST-II, respectively. And finally, the MEMS bridge widths should be less than 80 µm if possible for proper operation of the CLR model.

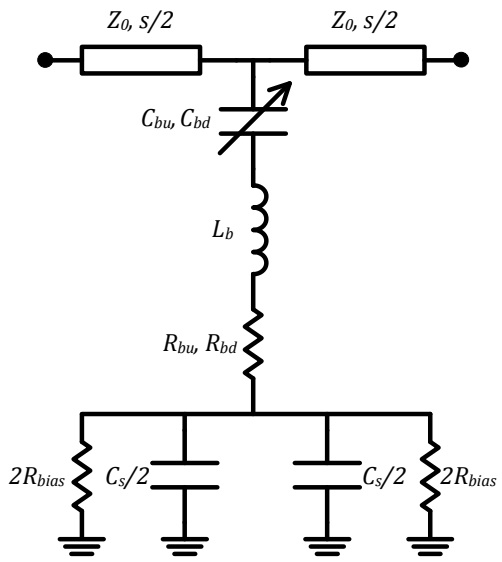


Figure 5.8: The circuit model of the DMTL unit section that is used for the design of the DMTL interconnection line.

Using (5.1)-(5.7), the parameters that are given in the first and the third columns of Table 5.2 are calculated as a starting point for the design for UST-I and UST-II, respectively. The impedance, effective relative dielectric constant, and the total loss of the CPW are calculated using the formulation in [172], and verified with the measurement results of the previously fabricated single metal layer TST based phase shifters, which were explained in Chapter 4. The impedance of the unloaded transmission line is selected as 96 Ω, and the CPW unloaded line loss is minimum around this impedance level. The CPW losses become minimum when the center conductor width is selected the same as the spacing between the signal and the ground. After determining the capacitance values and the periodicity, the physical dimensions of the unit section are extracted using capacitance formulation (3.1) to (3.3) given in Chapter 3. Here, C_{bu} and C_s values had to be modified as the parallel plate down state capacitance, C_{bd}, should be multiplied with 0.37 as explained in Chapter 3, which, indeed, causes the MEMS bridge to affect not only the upstate capacitance, but also the down state capacitance. Then, the unit sections are simulated using the model given in Figure 5.8 in MWO to adjust the capacitances, where the effects of the L_b, R_{bu}, R_{bd}, and R_{bias} are not included.

Table 5.2: The circuit design parameters of the DMTL UST-I and DMTL UST-II.

	DMTL UST-I		DMTL UST-II	
	DMTL Formulation	**Circuit Model HFSS Sim.**	**DMTL Formulation**	**Circuit Model HFSS Sim.**
Z_o	96 Ω	96 Ω	96 Ω	96 Ω
$\varepsilon_{r,eff}$	2.36	2.36	2.36	2.36
α	40 dB/m @20 GHz	40 dB/m @20 GHz	40 dB/m @20 GHz	40 dB/m @20 GHz
f_{Bragg}	90 GHz	73 GHz	69 GHz	59 GHz
s	302 µm	300 µm	300 µm	300 µm
Z_{lu}	58 Ω	55.9 Ω	54 Ω	52.9 Ω
Z_{ld}	42 Ω	40.9 Ω	32 Ω	34.5 Ω
ϕ_{up}	-13.8°	-14.1°	-14.8°	-15°
ϕ_{down}	-19.1°	-20°	-24.9°	-24°
$\Delta\phi$	5.3°	5.9°	10.1°	9.1°
C_{bu}	47.7 fF	46.4 fF	47.4 fF	46.7 fF
C_{bd}	458.4 fF	469.2 fF	458.4 fF	469.2 fF
C_s	68.1 fF	89.5 fF	128.1 fF	147.6 fF
L_b	-	30 pH	-	30 pH
R_{bu}/R_{bd}	-	1.6/0.15 Ω	-	1.6/0.15 Ω
C_U/C_D	28.1 fF/59.3 fF	30.6 fF/ 75.2 fF	34.6 fF/100.1 fF	35.5 fF/112.3 fF
Q_U/Q_D	-	27/12	-	60/27
R_{bias}	-	1400 Ω	-	1542 Ω
$R_{bias,DC}$	-	20.25 kΩ	-	18.375 kΩ

Table 5.3: The physical design parameters of the final designs of the DMTL UST-I and UST-II.

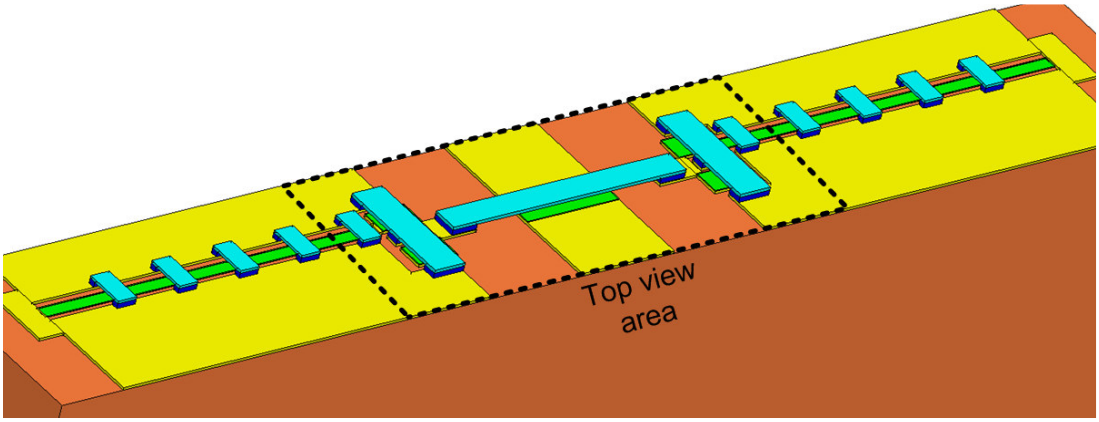
Parameter	**UST-I**	**UST-II**
W	150 µm	150 µm
G	150 µm	150 µm
l_{brd}	300 µm	300 µm
w_{brd}	38 µm	38 µm
w_{gnd}	40 µm	40 µm
$l_{brd\text{-}g}$	138 µm	138 µm
$w_{brd\text{-}g}$	49 µm	2 x 44 µm
w_{go}	30 µm	30 µm
l_{go}	40 µm	40 µm
w_{SiCr}	20 µm	20 µm

The unit sections designed in MWO are also simulated and optimized in HFSS v9.2 in order to obtain the required capacitance values. The 3D and the top views of the UST-I are given in Figure 5.9. The dimensions used for the final design for DMTL UST-I and UST-II are given in Table 5.3. During the simulations and optimization using HFSS v9.2, the following points have been taken into account:

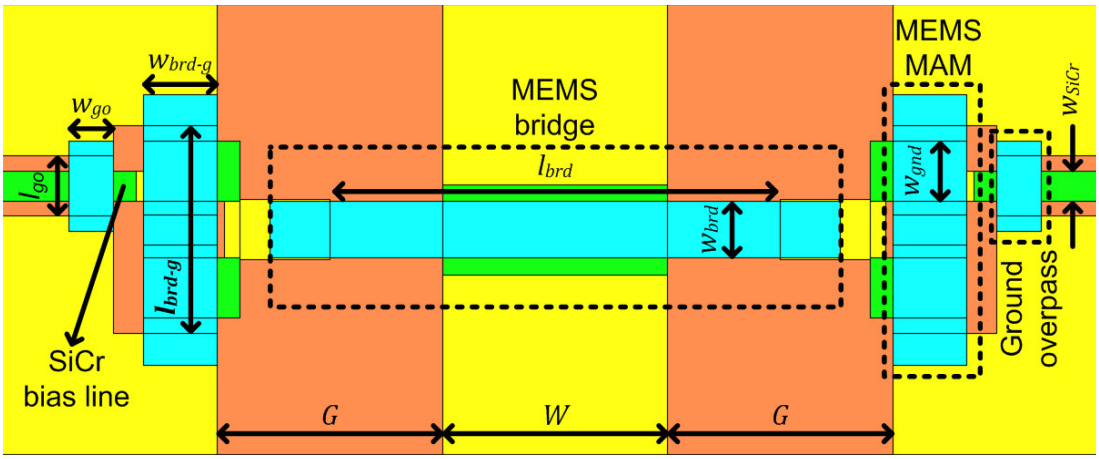
- The quartz substrate with parameters ε_r = 3.8 and $tan\ \delta$ = 0.001 are used. The conductivity of gold is used as σ_{Au} = 3 x 10^7 S/m.
- During the downstate simulations, the relative permittivity of silicon nitride is used as ε_r = 2.53 instead of 7 in order to include the 0.37 factor.
- The conductivity of the SiCr bias lines is taken as σ_{SiCr} = 12500 S/m, which is extracted from the measurement results of the previous runs.
- The dimensions of the CPW was selected as $G\ /\ W\ /\ G$ = 150 / 150 /150 µm. Although selecting the CPW dimensions as high as possible reduces the losses, there is an upper limit to provide higher order mode-free operation [183]. Considering the center design frequency, which is 15 GHz in this case, this selection is a good compromise considering both the line losses, and the actuation voltage of the MEMS bridge as it directly depends on the CPW signal width.
- MEMS bridge was fixed to w_{brd} = 38 µm in width and l_{brd} = 300 µm for both unit section types. The reason behind this selection is to prevent different mechanical buckling behavior of the MEMS bridges for different types of unit sections, and hence, to prevent different MEMS bridge capacitances. The MEMS bridges with wider and longer dimension are observed to buckle more easily in case of any residual stress. Moreover, w_{brd} was tried to be fixed around 50 µm in order the CLR model to work properly [184].
- The MAM capacitances in the DMTL structures have shown to be “buckled” more than the standard fixed-fixed MEMS bridge because of the residual stress since the area of these capacitors become large so as to achieve large capacitance value. To prevent this behavior, a modified MAM capacitance is

used in the DMTL unit sections in this thesis. First, the MAM is fixed from two sides instead of three to attain a mechanically balanced structure. Secondly, an additional anchor is used in the longitudinal dimension to avoid buckling. And finally, for the MAMs with more than 50 µm width, the MAM is divided into strips, whose width is about 50 µm and gap is 6 µm, as to prevent the buckling in the lateral dimension.

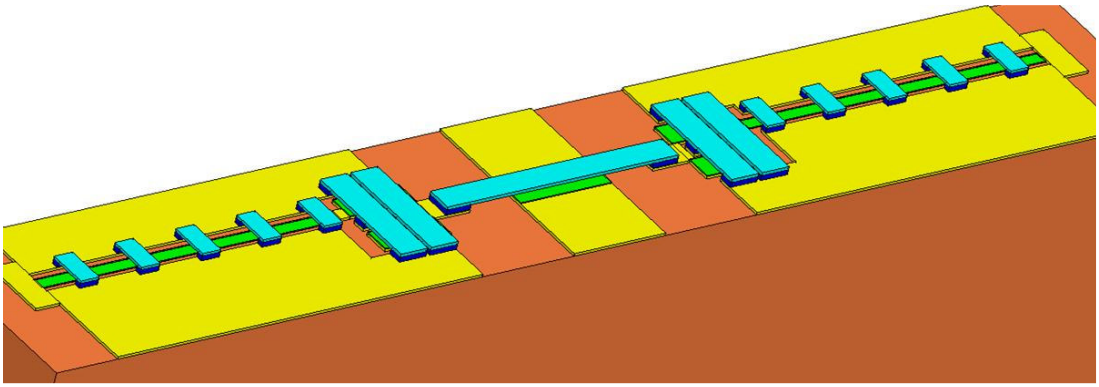
- The SiCr bias lines were shorted to the CPW grounds on both sides with the aim of modeling the connection to biasing network.



(a)



(b)



(c)

Figure 5.9: (a) 3D view of the DMTL UST-I (z-dimension exaggerated) (b) Top view of the DMTL UST-I (c) 3D view of the DMTL UST-II (z-dimension exaggerated).

During the design in HFSS, all the parameters are extracted by dedicated and separate simulations. In order to extract the MEMS bridge parameters in the upstate, C_{bu} and R_{bu}, the unit sections are simulated using an HFSS model *in which only the MEMS bridge is present, and it is connected to the CPW grounds without any MAM capacitances*. Then, these parameters are extracted by cascading the S-parameters of 16 unit sections that are simulated in HFSS and fitting the overall S-parameters with that of the circuit model. The MEMS bridge parameters in the downstate, C_{bd}, R_{bu}, and L_b, are extracted in a similar manner, *where the same HFSS model is used except the MEMS bridge is simulated in downstate*. The MAM capacitance parameters, C_s and R_{bias}, are extracted with an HFSS model *where only the MAM capacitance exists, and the center conductor of the CPW is directly connected the lower plate of the MAM capacitance*. In the model, the parasitic capacitances, and the loss factors due to the SiCr biasing resistors and the CPW ground overpasses are also included. Then, all the components, i.e., the capacitances, bias lines, and overpasses, are combined, and the HFSS simulations are repeated for both upstate and downstate to verify and optimize the model. To get the desired capacitance values, the dimensions of the MAM capacitance are tuned, and the MEMS bridge dimensions are not changed.

The results of the HFSS simulations yielded the parameters presented in the second and the fourth columns of Table 5.2. Here, L_b represents the inductance of the MEMS bridge. The change in the Bragg frequency is because of the effects of the added inductance to the model [7]. R_{bu} and R_{bd} model the resistance of the MEMS bridge in the upstate and downstate, respectively. R_{bias} models the losses coming from Q-factor of the MAM capacitor ([181], [142]). These losses include the ohmic losses of the capacitor itself and the additional losses coming from the SiCr bias lines. The SiCr bias line passes through the CPW ground planes, and the ground planes are patched up by small air bridges due to the discontinuities caused by the bias lines. Due to the distributed nature of the resistor and the coupling between this resistor, the CPW ground, and the air bridges, the equivalent value of R_{bias} is about a few kΩ, although it has a DC value of about 20 kΩ. Because of this fact, the latter factor is the dominant loss contributor.

A lossy capacitor can be modeled as in Figure 5.10, and the quality factor, Q, of the capacitor can be calculated as in (5.8) where R_s can be written as in (5.9). Here, R_p is the total resistance representing both the SiCr bias lines and the ohmic losses of the MAM capacitor. It was stated in [181] and [142] that the resistance of the MEMS bridge, R_b, does not contribute significantly to the losses. However, R_{bias} is quite effective on the losses since it causes a considerable decrease in the Q-factor of the MAM capacitance as explained above. Since the phase shifter design requires a resistive bias line in almost all unit sections of the designed DMTLs, it was decided to calculate the overall Q-factor, Q_D, of the equivalent shunt capacitor, C_D, and to see the total loss contribution of the overall Q-factor. Here, the subscript "D" states that the calculations were made for the downstate, where the losses are higher. The calculations can be repeated for the upstate in a similar manner. To find the overall Q-factor, the total series resistance is calculated using (5.10), where the equivalent series resistance of the MAM capacitor is given in (5.9). The overall Q can be found using (5.11), and the total loss contribution per unit section is given in (5.12).

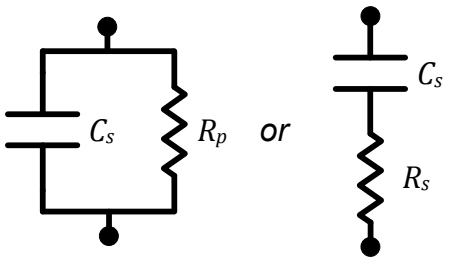


Figure 5.10: The circuit model of the DMTL unit section that is used for the design of the DMTL interconnection line.

$$Q = \omega C_s R_p = \frac{1}{\omega C_s R_s} \tag{5.8}$$

$$R_s = \frac{1}{\omega^2 C_s^2 R_p} \tag{5.9}$$

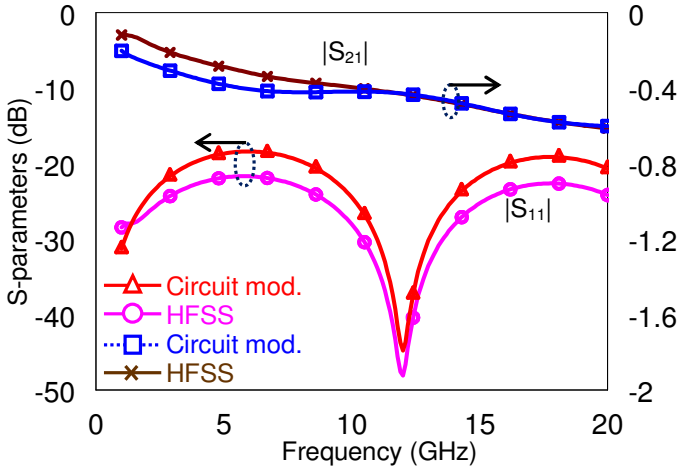
$$R_q = R_{bd} + \frac{1}{\omega Q C} \tag{5.10}$$

$$Q_D = \frac{1}{\omega C_D R_q} \tag{5.11}$$

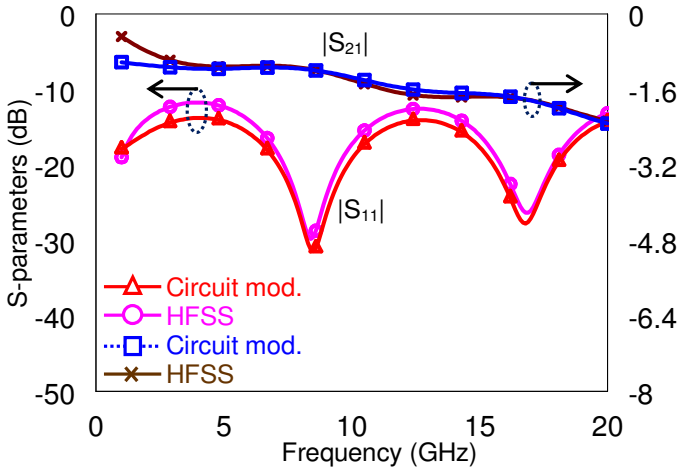
$$\alpha_{ld} = \frac{R_t}{2Z_{ld}} + \frac{R_q Z_{ld} \omega^2 C_D^2}{2}\ dB/unit\ section \tag{5.12}$$

Figure 5.11 gives the comparison of the HFSS simulations with the proposed circuit model simulations. In the simulations, S-parameters of a unit section that is simulated in HFSS is cascaded in MWO, and the result is compared with the results of the circuit model, which is also obtained by cascading 16 unit sections of the circuit model. The circuit model parameters that are used in the simulation are the ones in the second and the fourth column of Table 5.2. Considering the simulation results, it is seen that the circuit model is successful in predicting the EM full-wave simulations. The model can predict the phase response very accurately, and the insertion loss is also well predicted. The absolute difference between the S_{11} responses in the upstate is small. The error, which is defined previously in

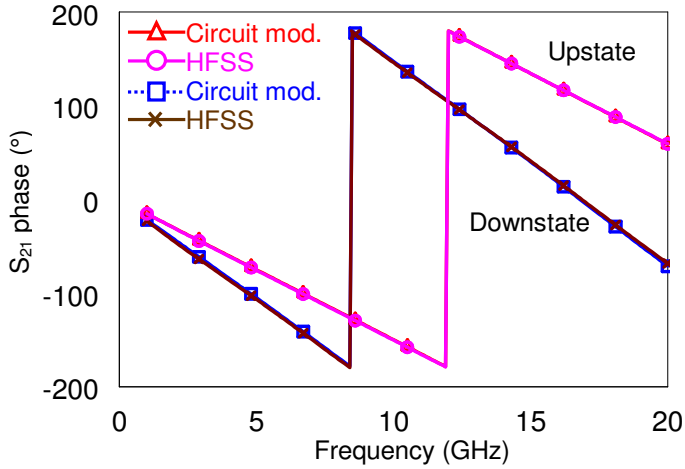
Section 5.2.1 between the S-parameters for all cases, which is given in Figure 5.11-(e), verifies that the modeling is successful.



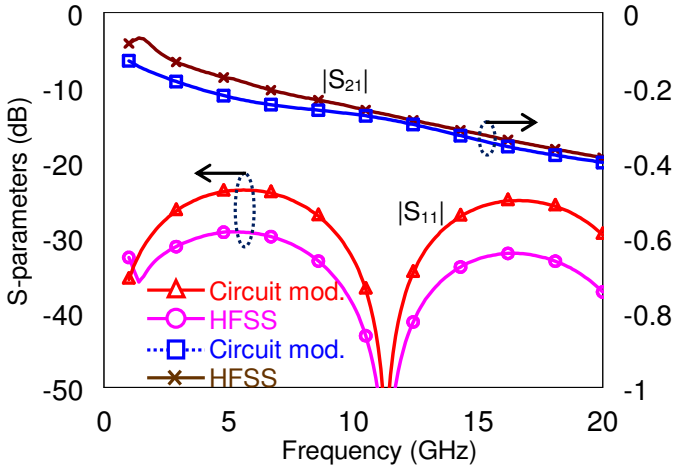
(a) $|S_{11}|$ and $|S_{21}|$ of DMTL UST-I in upstate (16 unit sections cascaded).



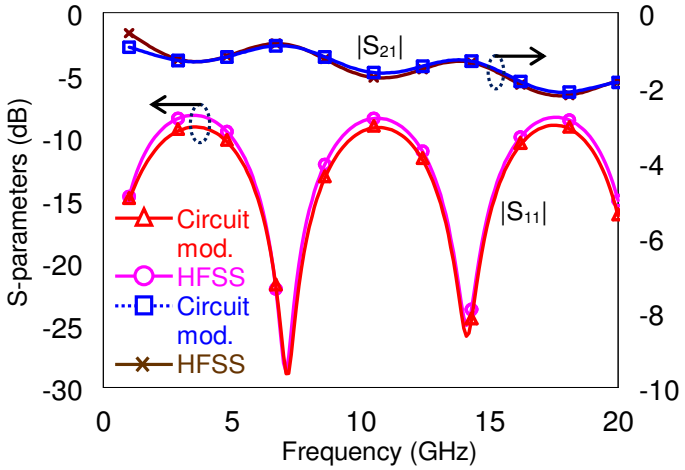
(b) $|S_{11}|$ and $|S_{21}|$ of DMTL UST-I in downstate (16 unit sections cascaded).



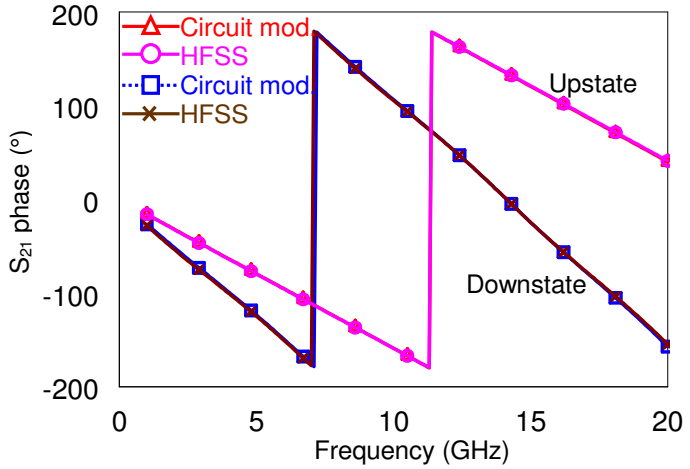
(c) $\angle S_{21}$ of DMTL UST-I in both states (16 unit sections cascaded).



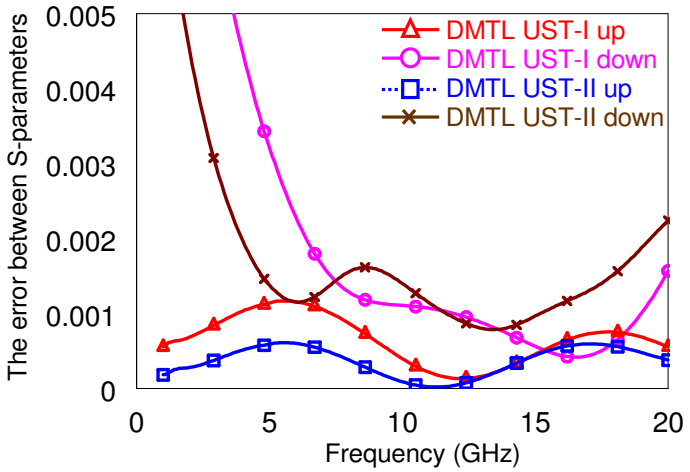
(d) $|S_{11}|$ and $|S_{21}|$ of DMTL UST-II in upstate (16 unit sections cascaded).



(e) $|S_{11}|$ and $|S_{21}|$ of DMTL UST-II in downstate (16 unit sections cascaded).



(f) $\angle S_{21}$ of DMTL UST-II in both states (16 unit sections cascaded).



(g) The error between the S-parameters of the circuit model and the HFSS simulations of DMTL UST-I and DMTL UST-II for all cases.

Figure 5.11: The comparison of the S-parameters of the circuit model and HFSS simulations for the DMTL UST-I and DMTL UST-II. The graphs are the results of cascaded 16 unit sections both for the circuit model and the HFSS simulation results (a)-(c) DMTL UST-I (d)-(f) DMTL UST-II (g) The error between the S-parameters of the circuit model and the HFSS simulations of both unit sections for all cases.

The loss of the DMTL unit sections is represented by two resistive components in the circuit, which are the resistance of the MEMS bridge, R_b, and the *effective* resistance of the MAM capacitor and the SiCr bias line, R_{bias}. The values presented in Table 5.2, especially R_{bu}, might be seen unphysical regarding the reported resistor values, which vary between 0.1-0.6 Ω. ([183], [185]). In these works, however, the value of R_b is extracted from the downstate measurements, and the same value is

also used in the upstate simulations, where the loss discrepancies in the upstate are explained by the changes in the unloaded line losses. In the design of the DMTL unit sections in this thesis, similar values are also obtained from the downstate simulations that are used to extract the circuit parameters. For example, from the HFSS simulations with only the MEMS bridge at downstate, i.e., without any MAM capacitors and biasing resistors, R_{bd} is extracted as 0.15 Ω. However, R_{bu} is extracted as 1.6 Ω from the HFSS simulations with only the MEMS bridge at upstate. This value results with a lower error between the S-parameters of the HFSS simulation and the circuit model. It should be also noted here that similar values are also reported previously for R_{bu}.

It is interesting to note here that the error between the S-parameters of the circuit model and the HFSS simulation can be reduced further for a different set of R_{bu}, R_{bd}, and R_{bias} values. Figure 5.12 shows the errors between the S-parameters for all cases for the values of R_{bu}, R_{bd}, and R_{bias} that are given in Table 5.4. It is clear that the error in Figure 5.12 is better that what is given Figure 5.11-(e). In the former case, R_{bu} and R_{bd} are fixed during the optimization, and R_{bias} is used as an optimization variable. In the latter case, all three parameters are used as optimization variables during the optimization. The optimization is made in 5-20 GHz band for both cases.

Table 5.4: The values of the resistances that are used for the first and the second modeling method for DMTL UST-I and UST-II.

	UST-I		**UST-II**	
	1st method	**2nd method**	**1st method**	**2nd method**
R_{bu}	1.6 Ω	2.1 Ω	1.6 Ω	0.97 Ω
R_{bd}	0.15 Ω	3.5 Ω	0.15 Ω	1.33 Ω
R_{bias}	1400 Ω	2411 Ω	1542 Ω	2462 Ω

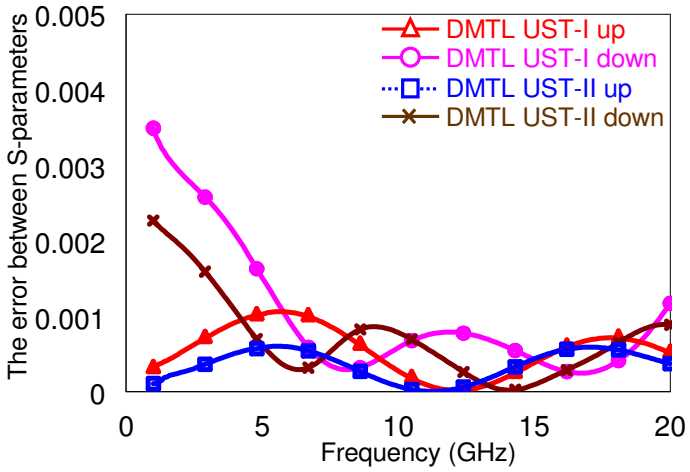


Figure 5.12: The error between the S-parameters of the circuit model and the HFSS simulation of both unit sections for the latter case, where the MEMS bridge resistance is extracted from "MEMS bridge only" HFSS simulations.

The change in R_{bu} and R_{bd} in the latter case is due to the way of using the SiCr bias lines. In standard DMTL phase shifter designs, the SiCr bias lines that penetrate through the CPW grounds are used only one for each bit, and these lines are modeled with additional shunt resistors. The unit sections with such type of biasing resistors are known as having the highest loss per unit section ([181], [142]). The designs in the frame of this thesis have such biasing lines in each unit section, and these lines are included in the HFSS simulations at all times. The change in R_{bu}, R_{bd}, and R_{bias} values are related according to using small C_s values in the design, which are comparable with C_b. In this case, the current distribution on the EM structure is different than that of a standard DMTL unit section where C_s is much bigger than C_b. Moreover, as the C_s is small, the fringe capacitances from to the bias lines to the ground overpasses become rationally larger, and these low-Q capacitances become more effective on the overall loss performance.

The quality factors in the upstate and downstate of UST-II is higher than that of UST-I. This is due to the increasing value of C_s. Moreover, R_{bias} also increase, which means the losses due to the biasing resistor has decreased, which is the dominant

loss mechanism of the DMTL unit sections of this type. This idea is also supported by the circuit model parameters of UST-III, which is the unit section type that is used in the DMTL stub design.

Figure 5.13 shows the layout of the final design of the DMTL interconnection line, which is composed by cascading two UST-Is and six UST-IIs. The DMTL interconnection line has five control pins, which results with 32 insertion phase states. The simulation results of the final design are given Figure 5.14, which conclude the design of the DMTL interconnection line.

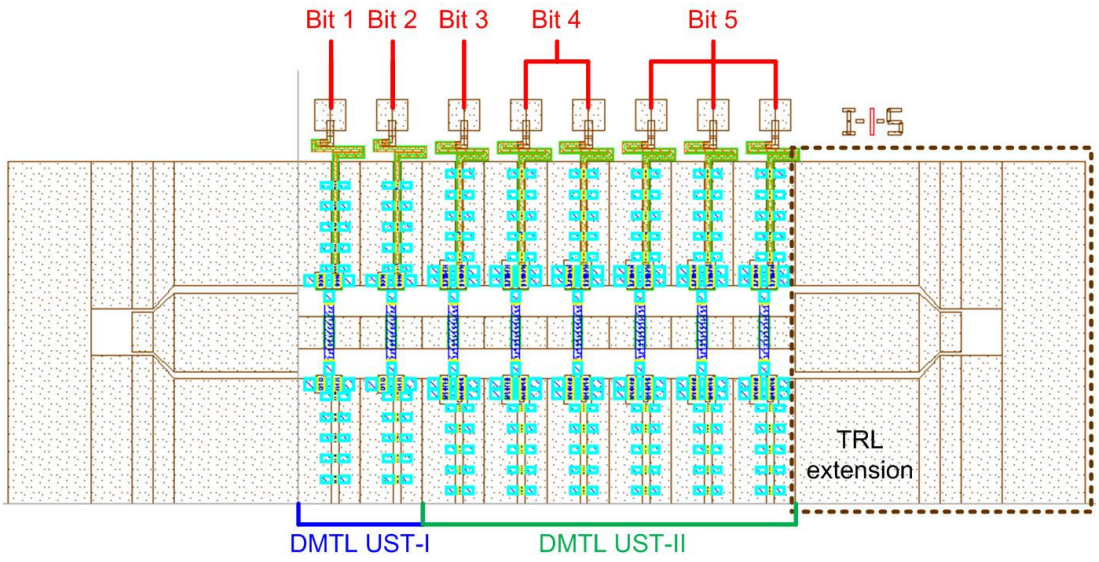
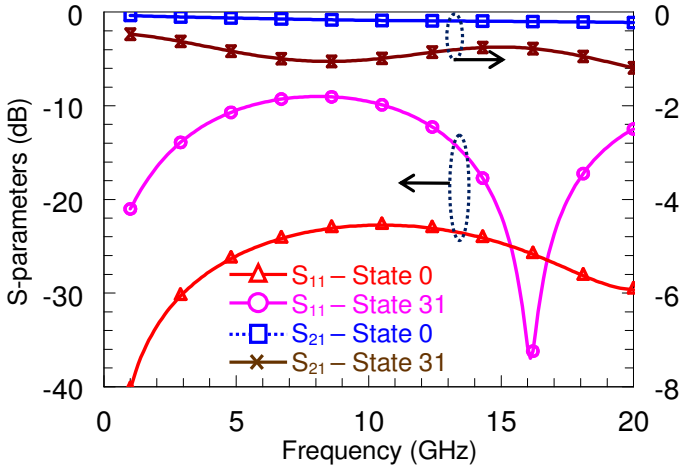
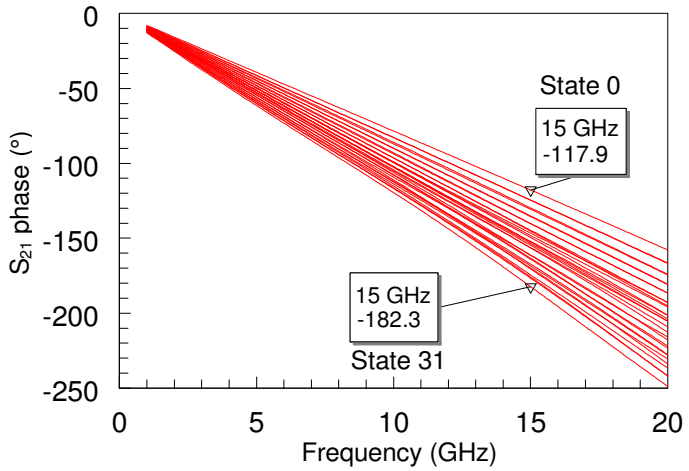


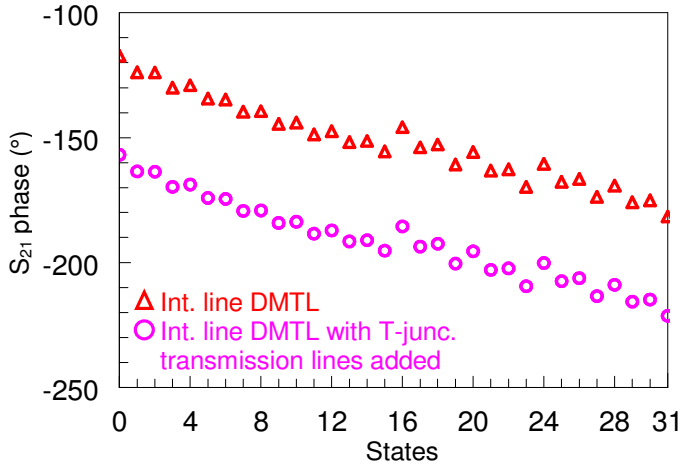
Figure 5.13: The layout of the DMTL interconnection line.



(a) $|S_{11}|$ and $|S_{21}|$ of DMTL interconnection line for states 0 and 31.



(b) $\angle S_{21}$ of DMTL interconnection line for all states.



(c) $\angle S_{21}$ (@ 15 GHz) of DMTL interconnection line.

Figure 5.14: The simulation results of the DMTL interconnection line (a) $|S_{11}|$ and $|S_{21}|$for all the switches are in upstate (State 0) and downstate (State 31) (b) $\angle S_{21}$ for all states (c) The change $\angle S_{21}$ with respect to the changes in the states.

5.2.3. The DMTL Stub Design

The electrical lengths of the stubs of the RF MEMS PS are also controlled by using DMTL unit sections. However, the design requirements of the DMTL stubs are yet different than that of the DMTL interconnection line. This is because the stubs are one port networks and the only design requirement is the phase of the input reflection coefficient. As a result, the loaded impedance of the DMTL is not required to be 50 Ω. Nevertheless, the DMTL should have minimal losses.

The design requirements of the DMTL stubs are determined by the theory of the TST based phase shifter, which was given in Chapter 4. It is required by (4.7) to (4.10) that in order to obtain the targeted insertion phase coverage of the designed PS, i.e., 0-360° range with 10° resolution, the phase of the reflection coefficients of the stubs should be changed between 0-360°. This is requirement is valid when the interconnection line lengths is not limited, and minimum insertion loss point is targeted for each phase state of the PS. But, once the interconnection line length is limited to the design constraints of the DMTL interconnection line, which is 0 to 0.1λ and 0.4λ to 0.5λ, the required values of the DMTL stubs are also changed. Using (4.7) to (4.10) one more time, it is shown that the phase of the reflection coefficients of Stub 1 and Stub 3 should be changed between -118° and 145°, the phase of the reflection coefficients of Stub 2 should be changed between -152° and 164° when the interconnection line length is in 0 to 0.1λ and 0.4λ to 0.5λ range.

The design requirements determined by the theory should also be verified by the circuit simulations once the interconnection line is replaced by the final DMTL interconnection line design. For this purpose, the circuit, whose block diagram was given in Figure 5.1, is used to find the necessary phase of the reflection coefficients for the stubs after the DMTL interconnection line is inserted to the circuit model. During the simulations, the stubs are modeled by lossy transmission lines, and the DMTL interconnection line and the T-junctions are used in their final design forms.

Using the Simplex Optimization tool of the MWO, the phase of the reflection coefficient should be changed between -110° and 119° for Stub 1 and Stub 3, and the phase of the reflection coefficient of Stub 2 should be changed between -143° and 120°. In order not to complicate the design, the maximum and minimum values of all the necessary phase of the reflection coefficient are chosen consequently, which are -143° and 120°, and a single DMTL stub design is made.

The DMTL stubs have 9 DMTL Unit Sections of Type III (UST-III). The number of unit sections is determined by the limitations related with the packaging and the measurement setup, which were explained previously in this chapter. The design of the UST-III again starts with using equations (5.1)-(5.11). Here, the unit section is designed using the equations in Matlab, and to check whether the electrical length of the stub is enough to cover the specified range, 9 UST-IIIs are cascaded with the T-junction extension, and the phase of S_{11} is checked. The parameters that are obtained using the equations are given in the first column of Table 5.5.

Following to same method that is used during the design of the UST-I and UST-II, the dimensions that are necessary for the physical implementation are extracted using the above mentioned capacitance formulation (3.1) to (3.3) given in Chapter 3. The structure is then simulated and optimized in HFSS v9.2. The 3D view and the physical dimensions of the final design of the DMTL UST-III are given in Figure 5.15 and Table 5.6, respectively.

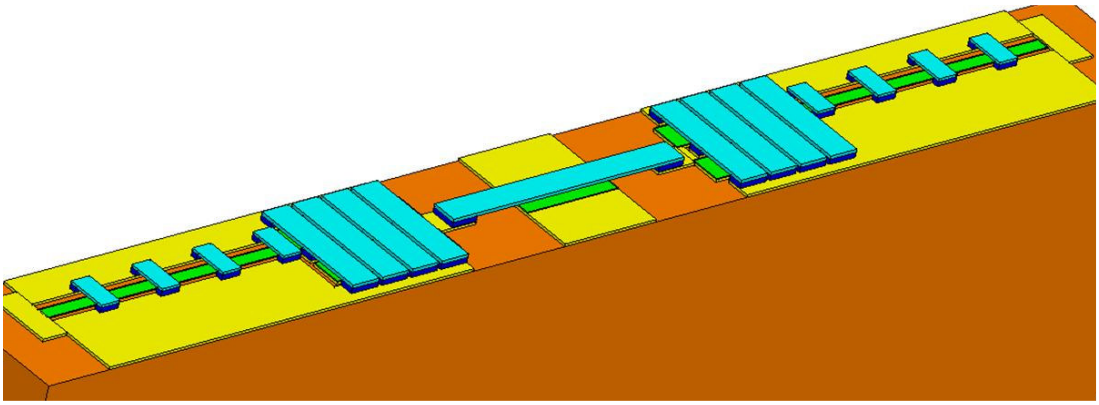


Figure 5.15: 3D view of the DMTL UST-III (z-dimension exaggerated).

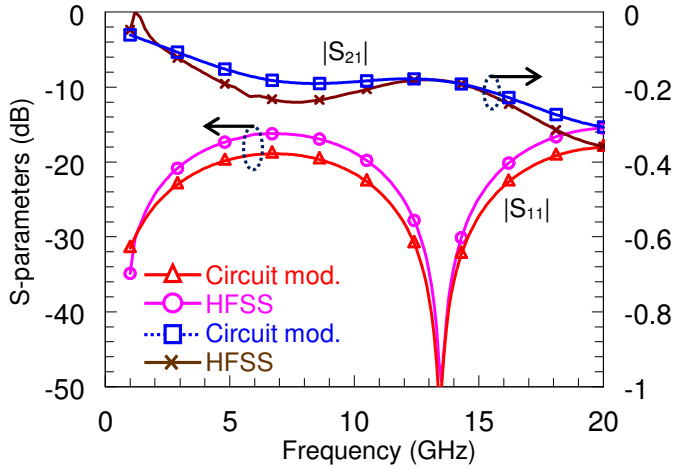
Table 5.5: The circuit design parameters of the DMTL UST-III.

	DMTL Formulation	**Circuit Model HFSS Sim.**
Z_o	96 Ω	96 Ω
$\varepsilon_{r,eff}$	2.36	2.36
α	40 dB/m @20 GHz	40 dB/m @20 GHz
f_{Bragg}	66 GHz	50 GHz
s	216 µm	210 µm
Z_{lu}	46 Ω	44.1 Ω
Z_{ld}	22 Ω	23.7 Ω
ϕ_{up}	-12.5°	-12.6°
ϕ_{down}	-26°	-25.4°
$\Delta\phi$	13.6°	12.8°
C_{bu}	47.5 fF	46.3 fF
C_{bd}	458.4 fF	469.2 fF
C_s	207 fF	296.7 fF
L_b	-	30 pH
R_{bu}/R_{bd}	-	0.46 Ω/0.45 Ω
C_U/C_D	38.6 fF/142 fF	40.1 fF/181.8 fF
Q_U/Q_D	-	114/67
R_{bias}	-	1784 Ω
$R_{bias,DC}$	-	15 kΩ

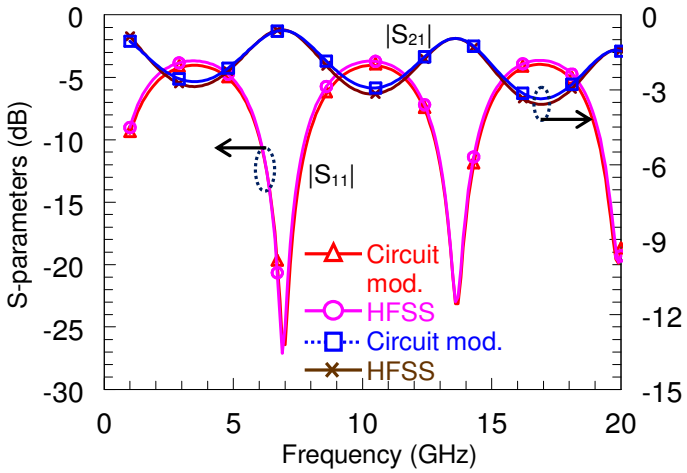
Table 5.6: The physical design parameters of the final design of the DMTL UST-III.

Parameter	UST-III
W	150 µm
G	150 µm
l_{brd}	300 µm
w_{brd}	38 µm
w_{gnd}	46 µm
$l_{brd\text{-}g}$	138 µm
$w_{brd\text{-}g}$	4 x 43 µm
w_{go}	30 µm
l_{go}	40 µm
w_{SiCr}	20 µm

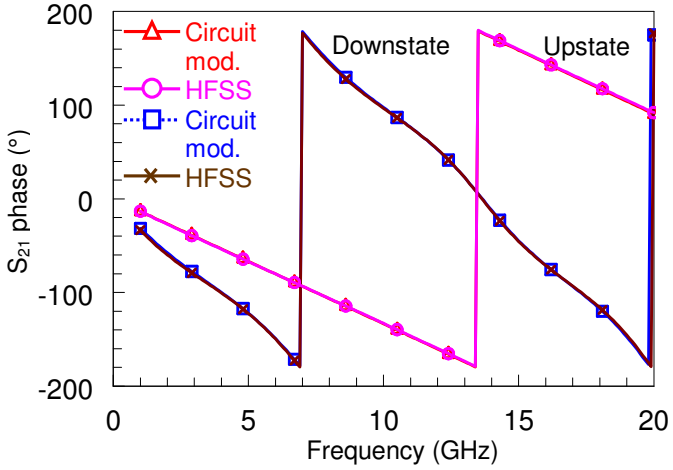
Figure 5.16 gives the comparison of the HFSS and the proposed circuit model simulations. The simulations are compared as in the design of UST-I and UST-II. The circuit model parameters that are extracted from the HFSS simulations are given in the second column of Table 5.5. The simulation results again show that the model is successful in predicting the EM full-wave simulations, which is also quantitatively given in Figure 5.16-(d). Lastly, Figure 5.17 shows the S_{11} characteristics of the final DMTL stub design for all possible states, $2^9 = 512$, in which 9 UST-IIIs are cascaded and terminated with an open circuit. The simulation circuit also includes the transmission line that models the T-junction extension. The simulation results show that the circuit satisfies the design requirements, which concludes the DMTL stub design.



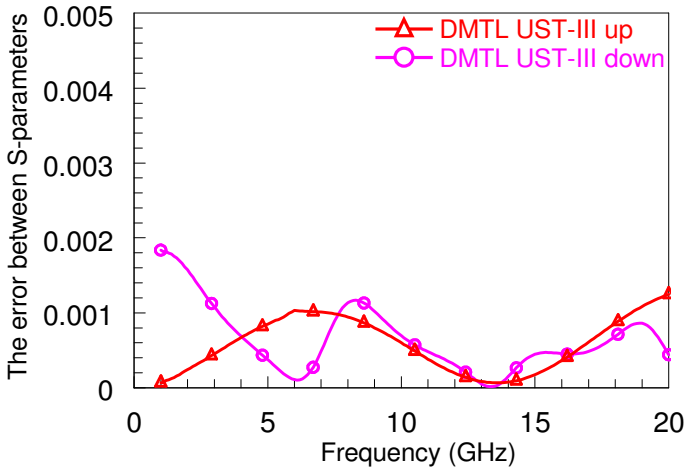
(a) $|S_{11}|$ and $|S_{21}|$ of DMTL UST-III in upstate (16 unit sections cascaded).



(b) $|S_{11}|$ and $|S_{21}|$ of DMTL UST-III in downstate (16 unit sections cascaded).



(c) $\angle S_{21}$ of DMTL UST-III in both states (16 unit sections cascaded).



(d) The error between the S-parameters of the circuit model and the HFSS simulations of DMTL UST-III for all cases.

Figure 5.16: The comparison of the S-parameters of the circuit model and HFSS simulations for the DMTL UST-III. The graphs are the results of cascaded 16 unit sections both for the circuit model and the HFSS simulation results (a)-(c) Magnitudes and phases of the S-parameters (d) The error between the S-parameters of the circuit model and the HFSS simulations for all cases.

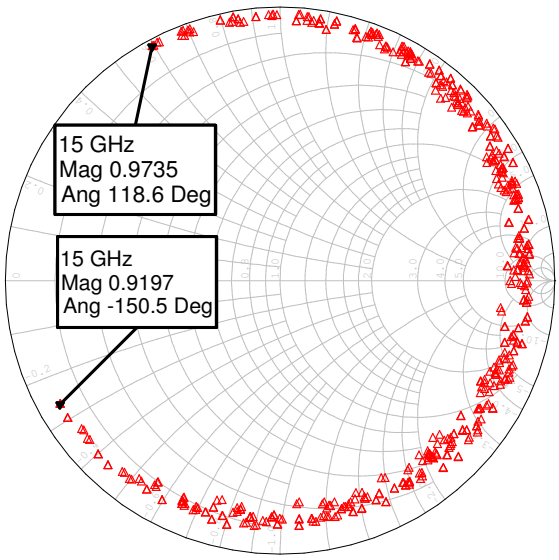


Figure 5.17: The S_{11} characteristics of the DMTL stub design for all possible 512 states.

5.2.4. The Overall RF MEMS Phase Shifter Design

The final step in the design of the RF MEMS PS is the connection of all the separately designed components, and to make final simulations in order to verify its operation. Figure 5.18 shows the layout of the final design of the RF MEMS PS. The design has 3×9 control pins the stubs and 5 control pins that control both DMTL interconnection lines, which make a total of 32 control pins. Each DMTL stub has $2^9 = 512$ different states and DMTL interconnection lines have $2^5 = 32$ states, which are controlled by the same 5 control pins. The layout of the design measures 10750 µm $\times$ 5915 µm, which includes the TRL extensions.

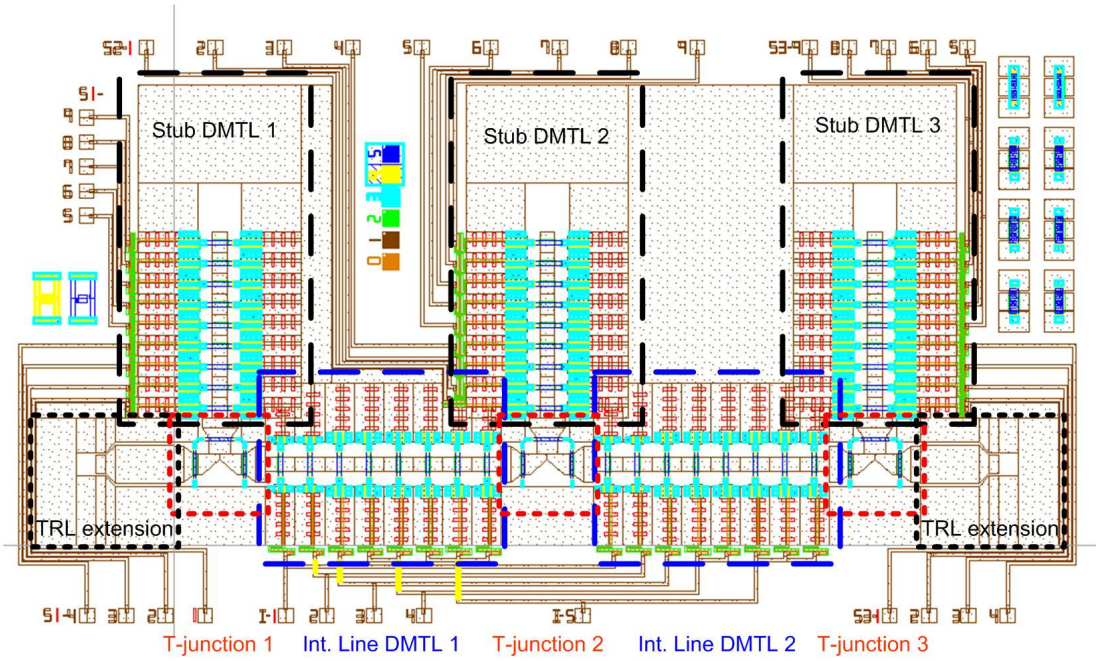


Figure 5.18: The layout of the final RF MEMS PS design.

For the final simulations of the RF MEMS PS, the ABCD parameters of the separately designed blocks, which are the T-junction, the DMTL interconnection line, and the DMTL stubs, are cascaded in MWO. For each insertion phase state, the required electrical lengths of the DMTL inter connection lines and the DMTL stubs are found

using the method explained in the previous section, and the states that give the closest electrical lengths to the required value is selected for that insertion phase state. Alternatively, the states for the DMTL stubs and the DMTL interconnection lines are found using the optimization tools of MWO. In the optimization, three state variables for the DMTL stubs and one state variable for the DMTL interconnection lines are used, which make a total of four variables. Optimization gives a state set among the 2^{32} state sets where the insertion loss and the input return loss performance are better for most of the insertion phase states.

The simulations results of the RF MEMS PS are shown in Figure 5.19, and the corresponding data is given in Table 5.7. In the final simulations, 0-360° insertion phase range is obtained with 10° steps. *The average phase error is 0.64°, the average insertion loss is -2 dB, and the average return loss is better than -24 dB among the 36 insertion phase states.* The maximum phase error is 4.8°, and there are a total of only 4 out of 36 that have phase errors worse than 1°. The worst case insertion loss is -3.9 dB, and there are a total of only 4 out of 36 states that have insertion losses worse than -3 dB. The worst case return loss is -10.9 dB, and there are a total of only 7 out of 36 states that have return losses worse than -20 dB. The performance parameters, i.e., the phase error, the insertion loss, and the return loss, degrade around some specific phase states, namely 110° and -40°. The reason of having low performance peaks at those specific points is due to the selection of the electrical length of the interconnection lines. These phase states are actually the transition regions, i.e., the maximum and minimum acceptable phase states allowed with the maximum and minimum states of the DMTL interconnection line. There are some differences between the theoretically required electrical length of the interconnection line and the electrical length of the final DMTL interconnection line design. Since the PS performance is very sensitive to the changes in the electrical length of the interconnection line, the performance of the PS degrade in a few insertion phase states around these transition regions.

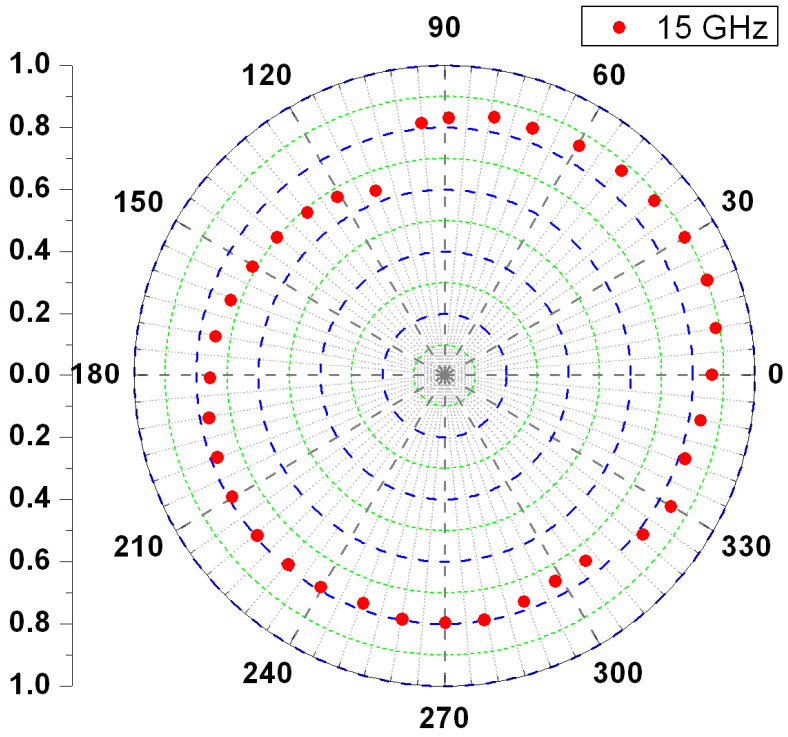


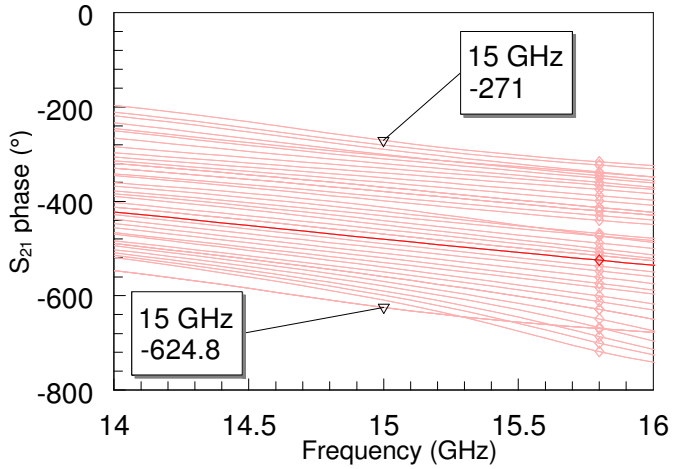
Figure 5.19: The S_{21} performance of the designed RF MEMS PS for all 36 phase states.

It should be also pointed out here that 10° phase resolution is not the lower limit for the design. The designed RF MEMS PS can be used with a resolution of 1° with ±1° maximum phase error at more than 90% of the 0-360° range.

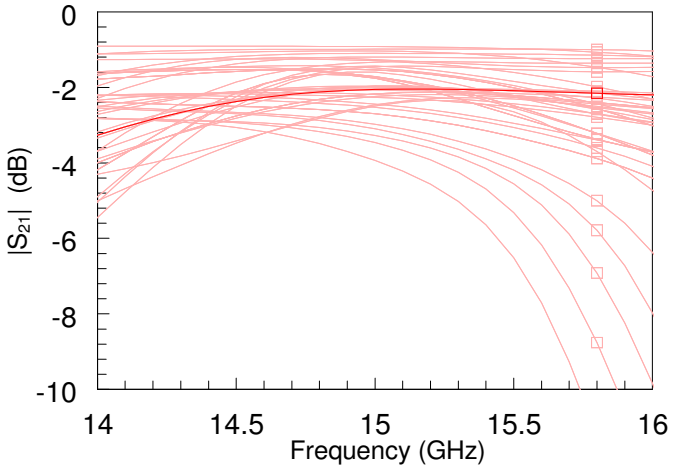
The frequency response is very important, and it deserves detailed investigation. Since the designed PS is a distributed structure, it has a comparably narrow instantaneous bandwidth; however, the design is completely reconfigurable, and the center frequency can be changed while preserving the instantaneous bandwidth. For 0-360° insertion phase coverage, center frequency should be higher than the initial design frequency. Figure 5.20 shows that the performance of the designed PS is acceptable in 1 GHz bandwidth around the center frequency, which is 15 GHz. The performance in higher frequencies is investigated in the following subsections where the measurements results are given.

Table 5.7: The final simulation results of the RF MEMS PS design for 0-360° range with 10° steps.

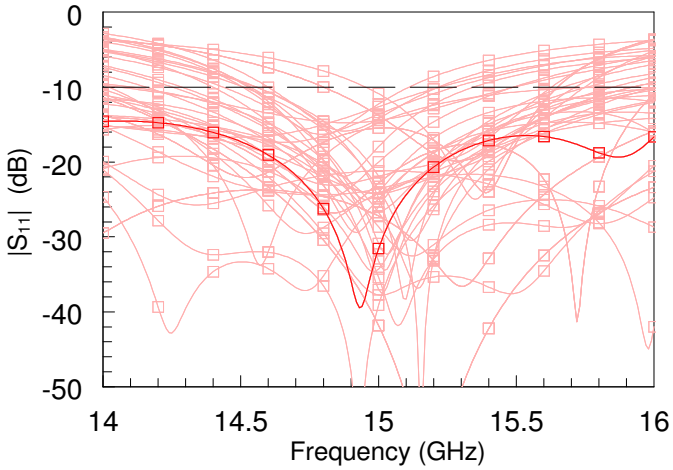
Target Phase	S_{11}	S_{21}		Phase Error (°)	Stub1 State	Stub2 State	Stub3 State	Int. Line State
	Mag (dB)	Mag (dB)	Ang (°)					
0	-24.08	-1.29	0.05	0.05	352	121	250	1
10	-26.76	-1.04	9.97	0.03	354	224	452	0
20	-27.20	-0.91	20.03	0.03	360	484	224	0
30	-21.19	-0.98	29.94	0.06	304	450	80	0
40	-24.16	-1.10	39.82	0.18	60	489	40	0
50	-23.32	-1.18	49.17	0.83	40	257	20	0
60	-25.97	-1.33	59.62	0.38	20	227	8	0
70	-24.02	-1.45	70.39	0.39	14	341	4	0
80	-17.94	-1.43	79.10	0.90	8	496	0	0
90	-14.21	-1.60	88.99	1.01	0	25	0	0
100	-12.26	-1.76	95.20	4.80	0	0	0	0
110	-15.47	-3.93	110.40	0.40	419	503	491	31
120	-21.90	-3.46	120.90	0.90	419	503	483	31
130	-24.22	-3.27	130.00	0.00	501	487	419	31
140	-22.81	-3.10	140.40	0.40	505	507	499	31
150	-31.55	-2.97	150.40	0.40	425	375	499	31
160	-26.71	-2.70	160.50	0.50	373	499	501	31
170	-34.29	-2.53	170.20	0.20	481	501	501	31
-180	-24.90	-2.44	-179.30	0.70	393	485	355	30
-170	-39.09	-2.26	-169.60	0.40	417	357	457	31
-160	-23.58	-2.18	-160.10	0.10	417	357	457	29
-150	-41.84	-2.07	-150.20	0.20	353	357	481	30
-140	-37.75	-2.01	-139.40	0.60	322	481	417	29
-130	-28.67	-2.04	-129.50	0.50	504	481	193	30
-120	-37.03	-2.05	-120.30	0.30	496	481	456	29
-110	-23.62	-2.17	-109.60	0.40	352	433	480	29
-100	-35.43	-1.97	-99.80	0.20	185	448	505	22
-90	-30.88	-1.98	-89.80	0.20	320	492	371	20
-80	-24.80	-1.96	-80.75	0.75	96	505	481	20
-70	-21.90	-2.24	-70.58	0.58	48	417	481	19
-60	-13.80	-2.46	-61.70	1.70	16	481	417	19
-50	-10.89	-2.49	-52.67	2.67	240	499	80	8
-40	-13.63	-1.72	-38.70	1.30	256	481	393	4
-30	-14.45	-1.48	-30.10	0.10	112	482	481	4
-20	-20.00	-1.71	-19.18	0.82	496	192	485	2
-10	-33.24	-1.53	-10.08	0.08	73	204	497	2
Avr.	-24.82	-2.02		0.64				
Std. dev.	7.95	0.72		0.89				



(a) $\angle S_{21}$ (unwrapped) of RF MEMS PS for all 36 phase states.



(b) $|S_{21}|$ of RF MEMS PS for all 36 phase states.



(c) $|S_{11}|$ of RF MEMS PS for all 36 phase states.

Figure 5.20: The performance of the designed RF MEMS PS for all 36 phase states (a) $\angle S_{21}$ (unwrapped) (b) $|S_{21}|$ (c) $|S_{11}|$.

5.3. The Fabrication and the Measurement Results

The designed RF MEMS phase shifter is fabricated using the METU RF MEMS Fabrication Process, the details of which were given in Chapter 2. The photographs and the SEM pictures of the fabricated PS are given in Figure 5.21 and Figure 5.22, respectively. The area of the fabricated PS measured 10.8×5.9 mm^2.

The fabricated phase shifters packaged using ceramic IC package with the same method given in Chapter 3. The package size of CSB03228 is 1.6×0.595 in^2. Figure 5.23 shows the photograph of the packaged RF MEMS PS. The packaged phase shifters are measured using Agilent 8361A network analyzer and Cascade Summit 9000 manual probe station. Cascade ACP-GSG-150 coplanar probes are used. The PS is measured using both TRL and SOLT calibration techniques. The TRL calibration kit is designed for the 5-20 GHz frequency range, and it is also fabricated on the same wafer with the PS. For the SOLT calibration, the impedance standard substrate of Cascade probes (101-190) is used, and the calibration frequency range is 10-40 GHz. Special PS samples are fabricated for SOLT and TRL calibrations separately. For these measurements, 50 Ω-50 Ω transitions are needed on both sides of the PS since the pitch spacing of the CPW probes are not compatible with that of the PS design. For this purpose, 50 μm-long 50 Ω-50 Ω transition is designed and added to the layout of the PS.

The same MEMS switch is used in all of the unit sections of the PS, and it is characterized by measurements. The actuation voltage of that switch is measured to be 8 V; nevertheless, all the MEMS structures are measured with 20 V-peak bipolar waveform as explained in Chapter 3. The reason for using a higher peak waveform is to guarantee the contact between the MEMS bridge and the dielectric layer. Each DMTL type is also fabricated separately to extract each parameter in different DMTL circuit models. The next subsection gives the details of the DMTL parameter extraction.

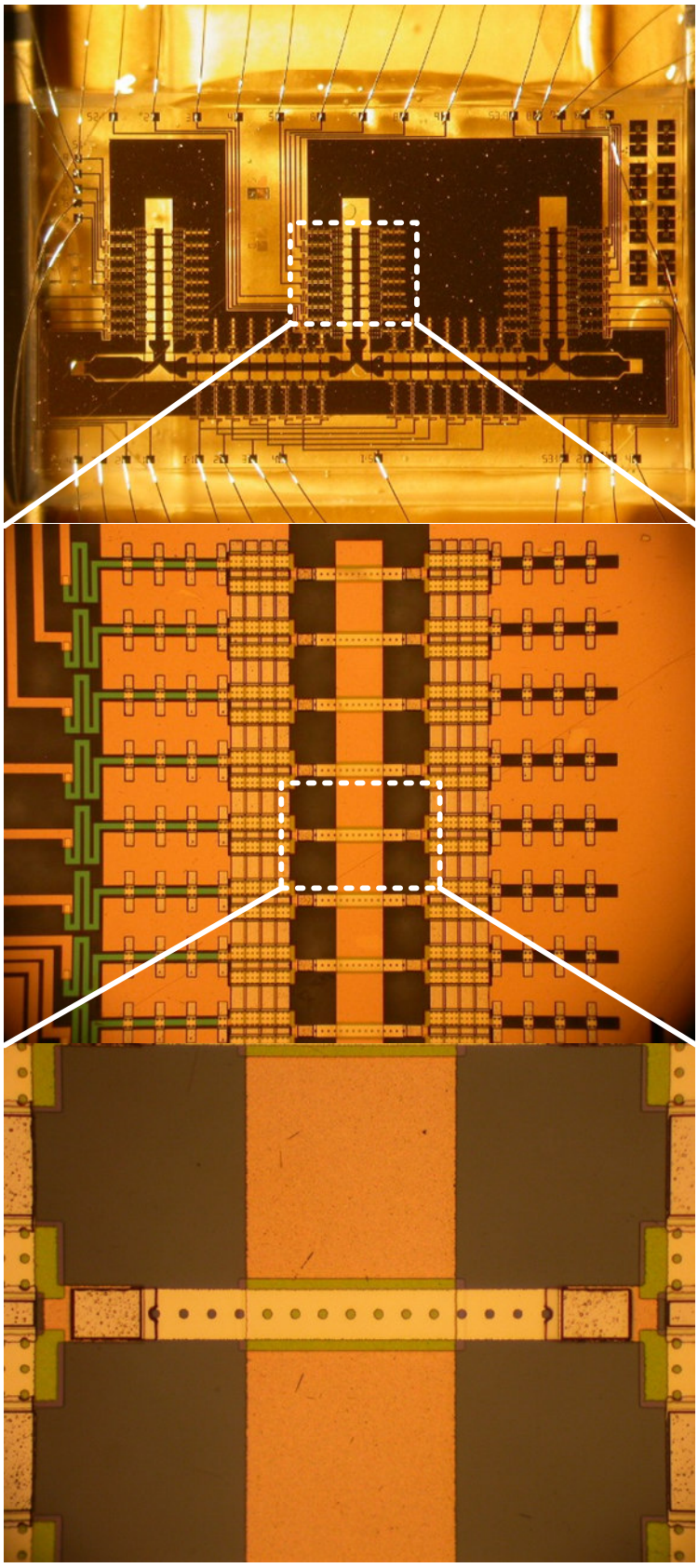
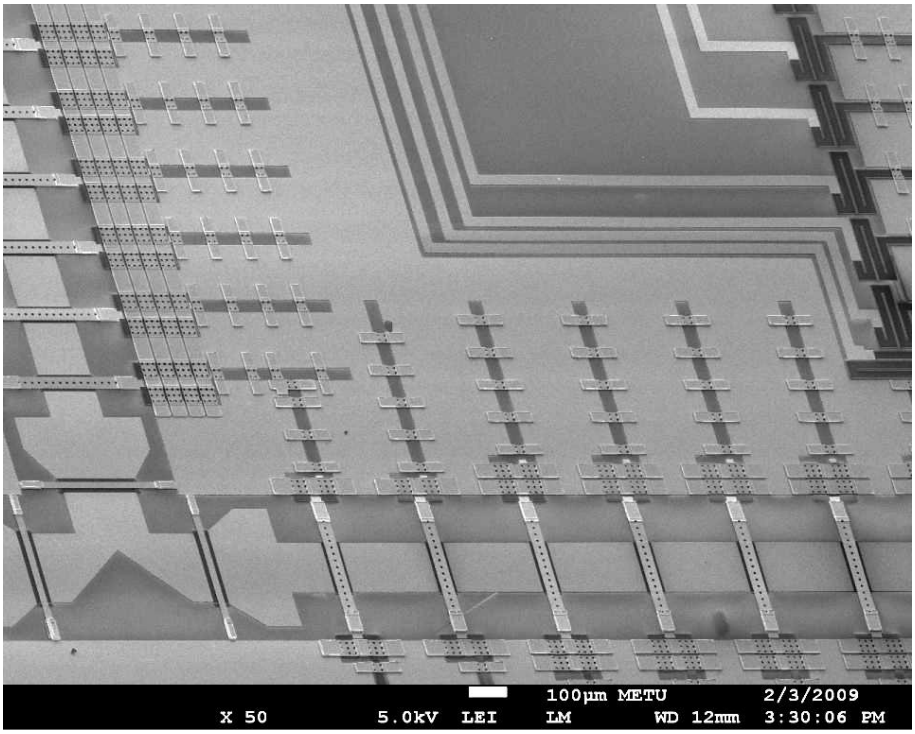
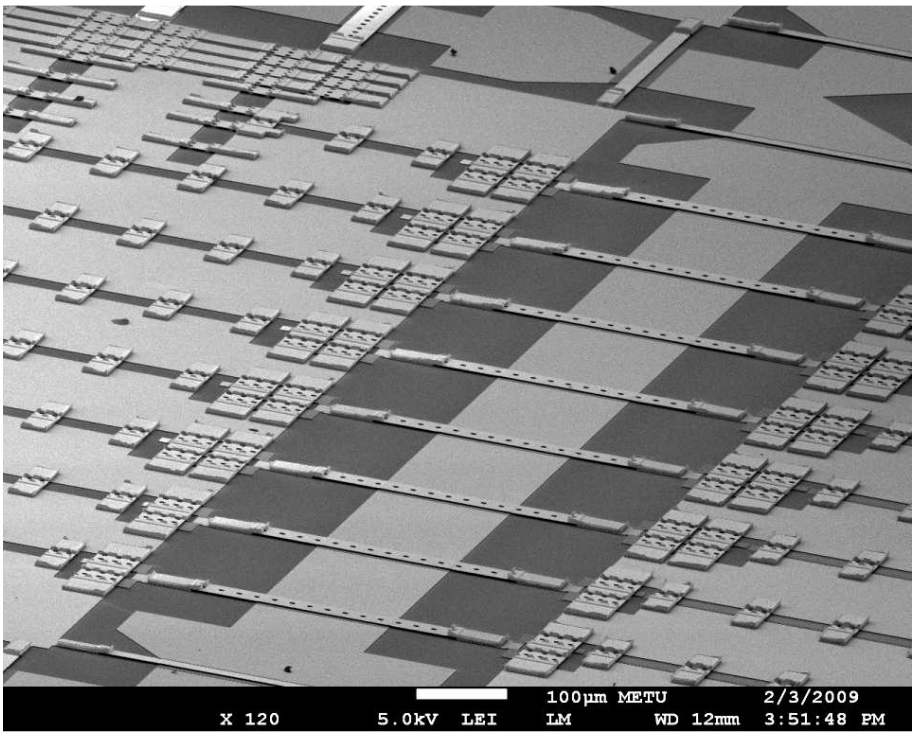


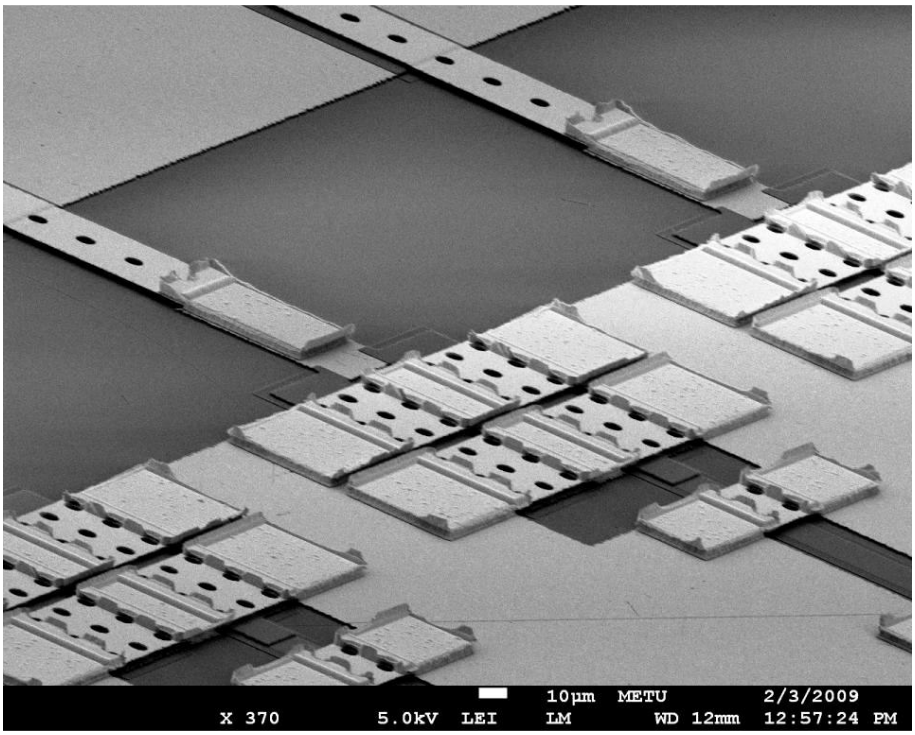
Figure 5.21: The photographs of the fabricated RF MEMS PS.



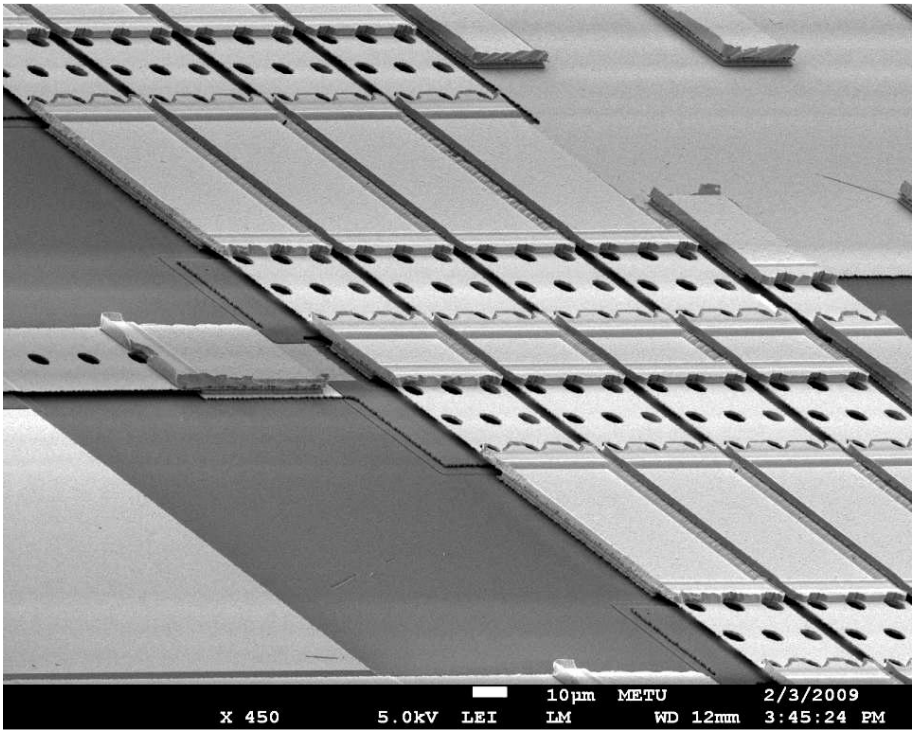
(a) Wide view of the DMTL interconnection line and the DMTL stub.



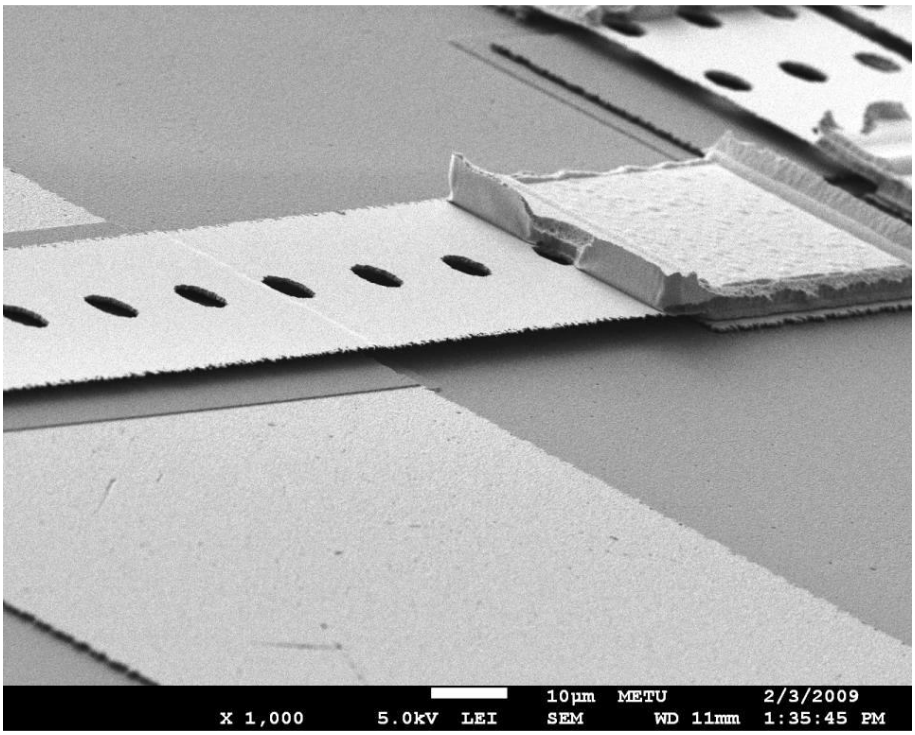
(b) The view of the of the DMTL interconnection line (UST I and II).



(c) The closer view of the of the MAM capacitor (UST II).



(d) The closer view of the of the MAM capacitor (UST III).



(e) The closer view of the of the MEMS bridge

Figure 5.22: The SEM pictures of the fabricated RF MEMS PS.

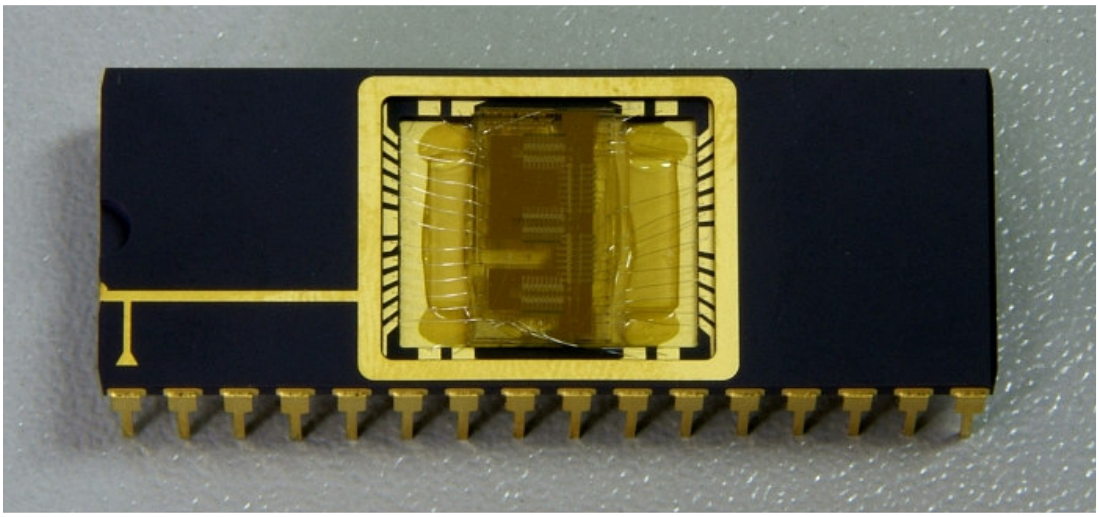


Figure 5.23: The photograph of the packaged RF MEMS PS (Package size: 1.6×0.595 in^2).

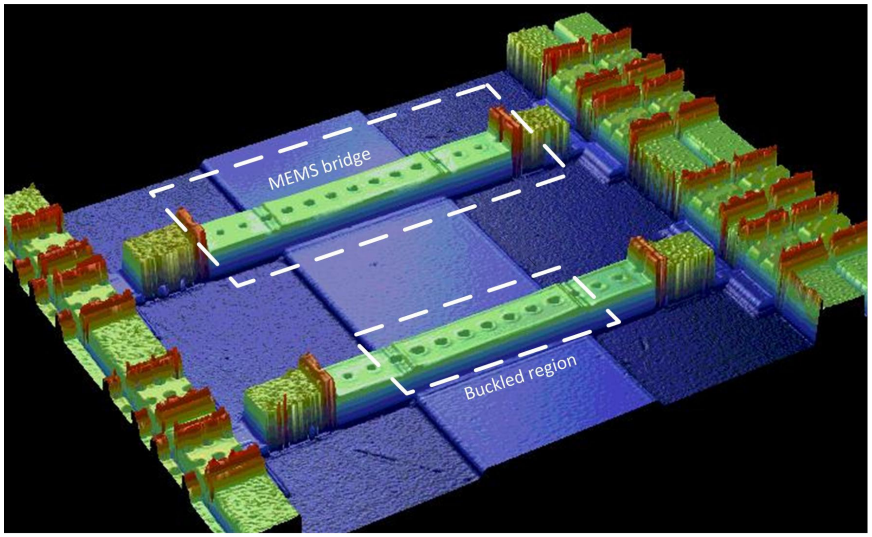
5.3.1. The DMTL Parameter Extraction

There are several parameters in the DMTL circuit model and specific structures are designed to extract each parameter of the fabricated RF MEMS PS. For the transmission line parameters, an unloaded CPW line is fabricated, and from the measurements of this line, the characteristic impedance, the relative dielectric constant, Z_o, $\varepsilon_{r,eff}$, and α are extracted. For the parameters of the MEMS bridge, a DMTL which only includes the MEMS bridge without any MAM capacitors is fabricated and measured. From the upstate measurements, C_{bu} and R_{bu}, and from the downstate measurements, C_{bd}, L_b, and R_{bd} are extracted. For the extraction of C_s, DMTLs that only include the MAM capacitors without any MEMS bridges are fabricated for each unit section type. From the measurements of these DMTLs, which only have the upstate, C_s is extracted for each unit section type. Finally, DMTLs that only include a single unit section type are fabricated and measured. From the upstate and downstate measurements of these structures, C_{bu} and C_s are tuned to fit the measurement results of the final DMTL of each type (UST-Type I, II, and III); in addition to that, R_{bias} is extracted. The extracted parameters for all types of unit sections are given in Table 5.8.

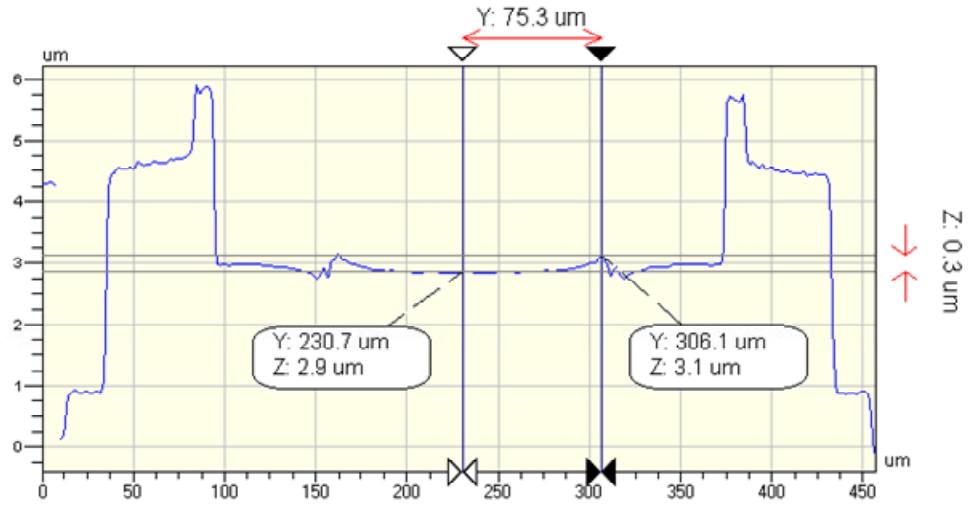
Considering the values given in the table above, most of the extracted values are close to the simulated values. The most important change is in the upstate capacitance of the MEMS bridge. This change is due to the change in the bridge height of the MEMS bridge on top of the CPW center conductor. The MEMS bridge is buckled downwards only on the center conductor of the CPW, and the remaining part of the MEMS bridge is totally flat. This can be observed from optical profiler measurements that are given in Figure 5.24-(a). The graphs and the views in Figure 5.24 are obtained from the measurements using Wyko NT 1100 optical profiler.

Table 5.8: The circuit model parameters of the DMTL UST-I, II, and III that are extracted from the measurements.

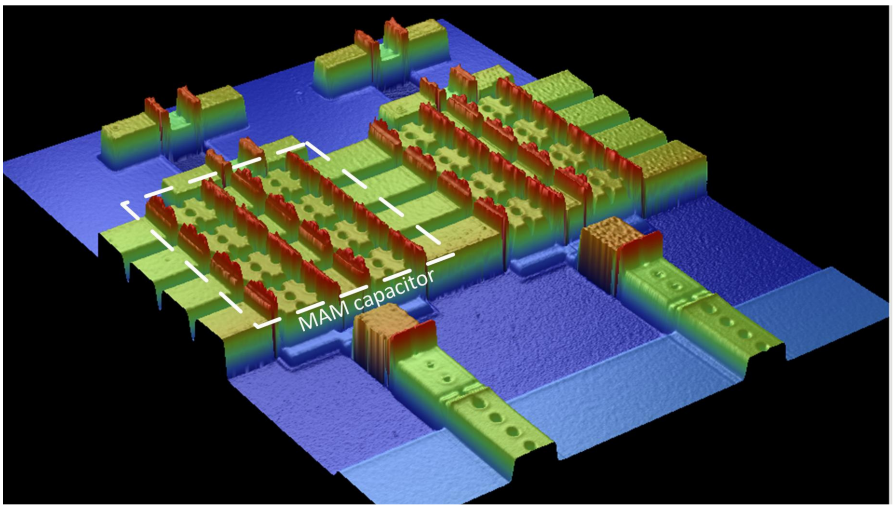
	DMTL UST-I		DMTL UST-II		DMTL UST-III	
	Sim.	**Meas.**	**Sim.**	**Meas.**	**Sim.**	**Meas.**
$Z_o\,(\Omega)$	96	96	96	96	96	96
$\varepsilon_{r,eff}$	2.36	2.43	2.36	2.43	2.36	2.43
$\alpha\,(dB/m)$	40 @20 GHz	38 @20 GHz	40 @20 GHz	38 @20 GHz	40 @20 GHz	38 @20 GHz
$f_{Bragg}\,(GHz)$	73	77	59	62	50	54
$s\,(\mu m)$	300	300	300	300	210	210
$Z_{lu}\,(\Omega)$	55.9	54.2	52.9	51.6	44.1	39.7
$Z_{ld}\,(\Omega)$	40.9	42.3	34.5	35.2	23.7	22.3
$\phi_{up}\,(^\circ)$	-14.1	-14.8	-15	-16	-12.6	-13.9
$\phi_{down}(^\circ)$	-20	-18.7	-24	-22.9	-25.4	-23.5
$\Delta\phi$	5.9	3.9	9.1	6.9	12.8	9.6
$C_{bu}\,(fF)$	46.4	61.5	46.7	62.3	46.3	67.7
$C_{bd}\,(fF)$	469.2	439.8	469.2	439.8	469.2	439.8
$C_s\,(fF)$	89.5	74.8	147.6	128.6	296.7	232.2
$L_b\,(pH)$	30	29.79	30	29.79	30	29.79
$R_{bu}/R_{bd}\,(\Omega)$	1.6 / 0.15	2 / 0.38	1.6 / 0.15	2 / 0.38	1.6 / 0.15	2 / 0.38
$C_U/C_D\,(fF)$	30.6 / 75.2	33.8 / 63.9	35.5 / 112.3	42 / 99.5	40.1 / 181.8	52.4 / 152
Q_U/Q_D	27 / 12	33 / 21	60 / 27	49 / 30	114 / 67	56 / 35
$R_{bias}\,(\Omega)$	1400	2718	1542	2120	1784	1300



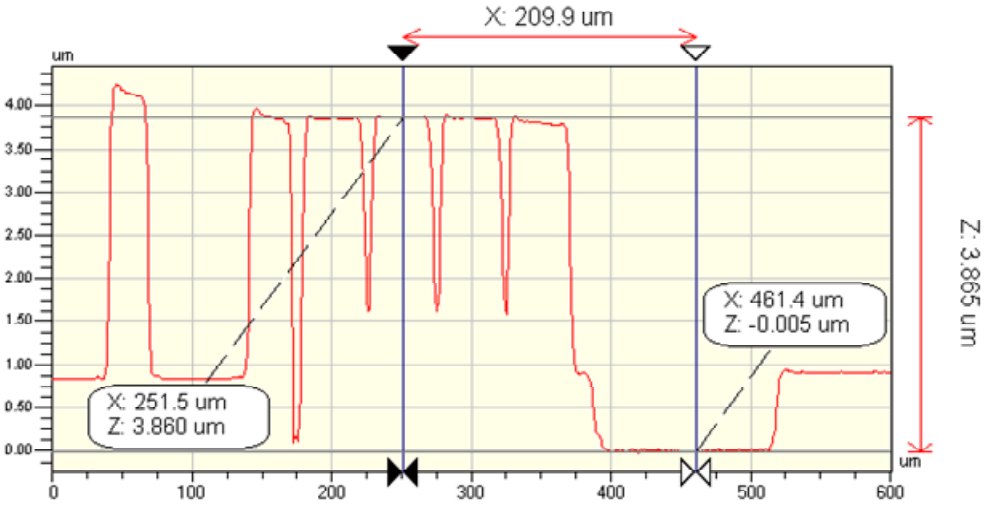
(a) Measured 3D view optical profiler view of the center MEMS bridge of the RF MEMS PS.



(b) Measured beam height variation of the center MEMS bridge of the RF MEMS PS.



(c) Measured 3D view optical profiler view of the MAM capacitor of the RF MEMS PS.



(d) Measured beam height variation of the MAM capacitor of the RF MEMS PS.

Figure 5.24: The optical profiler measurements of the fabricated RF MEMS phase shifter.

The measured thickness is of the first metal layer that forms the CPW lines is 0.9 µm, and the measured thickness of the structural layer is 1.1 µm. Once the MEMS bridge passes over the CPW center conductor, the MEMS bridge height is also expected to increase by 0.9 µm, and its top point is expected to be at 0.9 (first metal layer) + 1.1 (structural layer) + 1.8 (sacrificial layer) = 3.8 µm. However, the top point is measured to be at 2.9 µm, which means that the MEMS bridge is buckled downwards by 0.9 µm (Figure 5.24-(b)).

The reason of the buckling is the weak anchoring at the CPW metal step height point as explained in Chapter 2 in detail. Since the surface topology sharply increases due to the 0.9 µm-thick first metal layer, a secondary MEMS bridge occurs on top of the CPW center conductor, which is higher than the original bridge. However, this secondary bridge buckles downwards due to the tensile residual stress since the anchor points are not filled by strengthening layer, and they are nominally clamped. This is the behavior that was also observed in Chapter 2. The final MEMS bridge height is 2.9 - (0.9 + 1.1) = 0.9 µm, where the 0.9 µm and 1.1 µm are the thicknesses of the first metal layer and the structural layer, respectively. This result is also verified with the simulation results where the center MEMS bridge is modeled at 0.9 µm.

No buckling is observed on the MAM capacitances since there are no first metal layer step changes under these capacitances (Figure 5.24-(c)). The measured bridge height is exactly as expected, which is 3.8 - (0.9 + 1.1) = 1.8 µm as presented in Figure 5.24-(d). This result is also verified with the simulation results where the MAM capacitances are modeled at 1.8 µm.

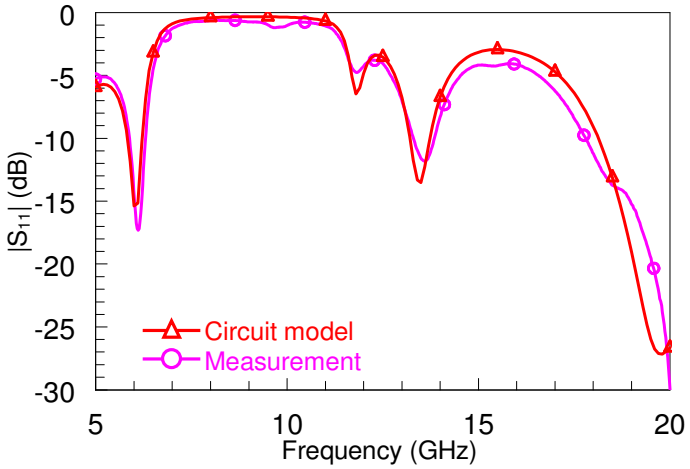
The change in the bridge height of the MEMS bridges increases C_{bu} significantly, which causes the up-down capacitance ratio to reduce significantly. This also results with a lower phase difference between upstate and downstate. The consequences of these changes are explained in the next subsection.

5.3.2. The RF MEMS Phase Shifter Measurements

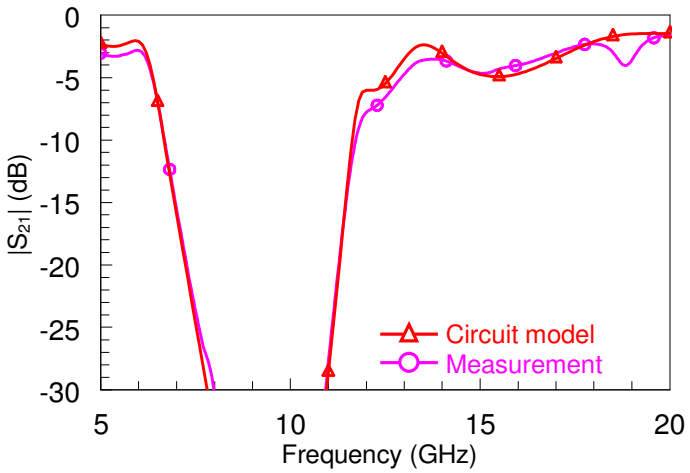
Having extracted the values of the circuit model parameters for each unit section type, the whole RF MEMS phase shifter is measured in 5-20 GHz and 10-30 or 10-40 GHz frequency bands with on-wafer TRL and SOLT calibration techniques, respectively. Since the circuit measured with SOLT calibration has additional 50 Ω-50 Ω CPW transitions on both sides, each measurement result is compared with its corresponding circuit.

For the measurement of the whole phase shifter, the multi-pin MEMS automated measurement setup (MAMS), which was explained in Chapter 3, is used since the RF MEMS PS has 32 control pins that should be controlled simultaneously. The applied actuation voltage is 20 V-peak bipolar waveform, which is supplied by the waveform generator card.

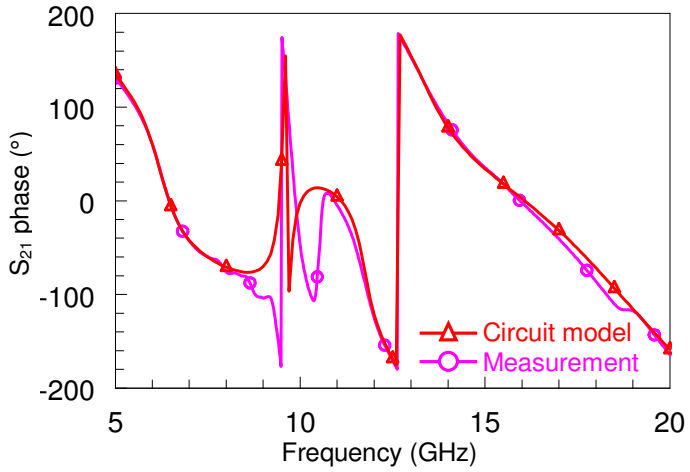
Figure 5.25 and Figure 5.26 show the upstate measurements of the PS with TRL and SOLT calibrations, respectively. The measurements with TRL calibration show good agreement with the simulations, whereas the measurements with SOLT calibration show good agreement with the simulations up to 30 GHz. After 30 GHz, the measurements still follow the simulations with some acceptable shift in both amplitude and phase responses. The circuit parameters used in the simulations are extracted from the measurements of corresponding type of DMTL structures as explained in the previous subsection.



(a) $|S_{11}|$ of measured RF MEMS PS compared with the simulations.

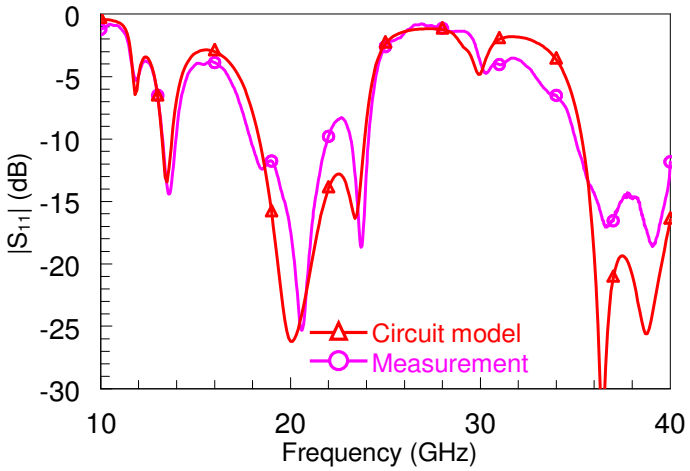


(b) $|S_{21}|$ of measured RF MEMS PS compared with the simulations.

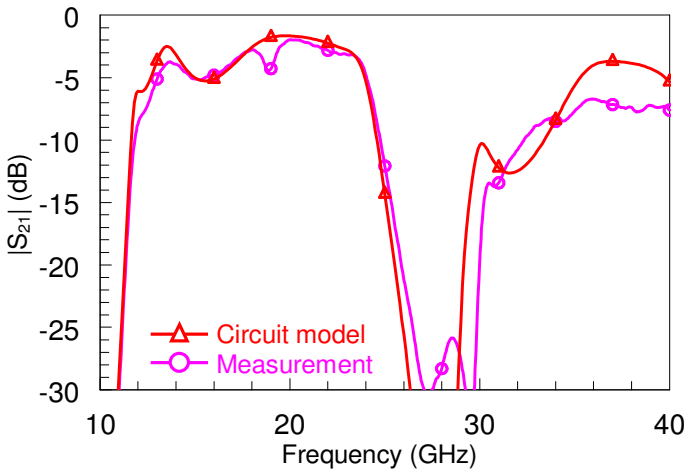


(c) $\angle S_{21}$ of measured RF MEMS PS compared with the simulations.

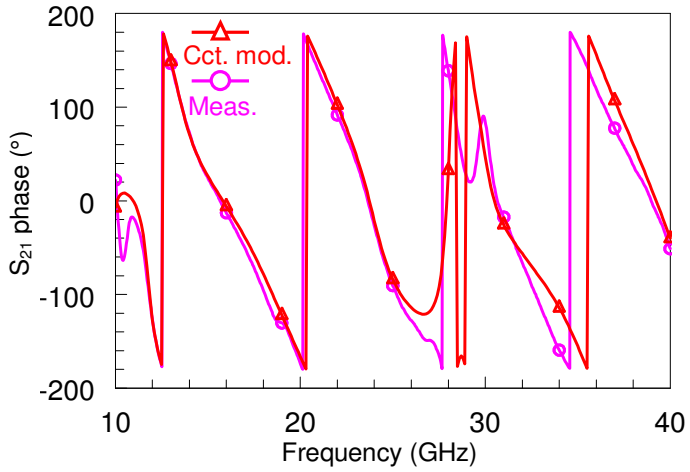
Figure 5.25: The measured upstate performance of the RF MEMS PS (TRL calibration used) compared with the simulations (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$.



(a) $|S_{11}|$ of measured RF MEMS PS compared with the simulations.



(b) $|S_{21}|$ of measured RF MEMS PS compared with the simulations.



(c) $\angle S_{21}$ of measured RF MEMS PS compared with the simulations.

Figure 5.26: The measured upstate performance of the RF MEMS PS (SOLT calibration used) compared with the simulations (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$.

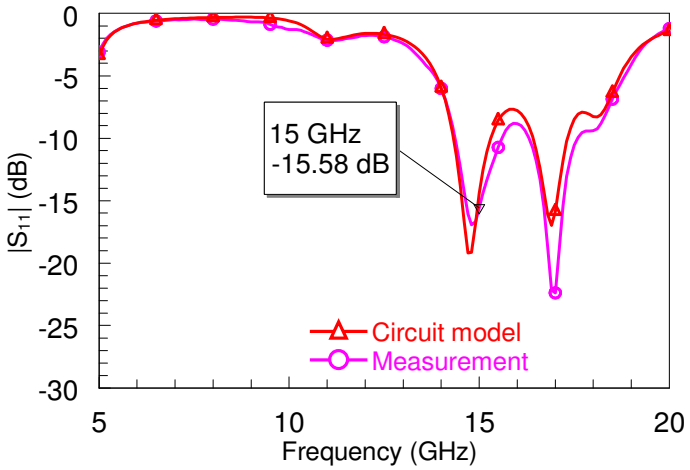
Figure 5.27 shows the performance of the PS configured for a sample phase state at the design center frequency, which is 15 GHz. The state numbers of the three stubs and the interconnection line are given in decimal form, and the ones in the corresponding binary equivalents indicate the unit sections in downstate. It is observed from the figure that the measurements are in good agreement with the simulations. The phase response is linear around the targeted frequency for at least ±1 GHz band. At 15 GHz, return loss is better than -15 dB, the insertion loss is about -3 dB, and both of them stay in acceptable levels in ±0.5 GHz. Figure 5.29, Figure 5.30, and Figure 5.31 show that the performance is similar for some other phase states even though they are not optimized specifically.

Figure 5.28 shows the performance of the PS for all possible phase states. From the figure, it is observed that the phase shift performance of the PS is limited to 160-360° range. *The average phase error among these 21 states (160-360°) is 1.7°. The average insertion loss and the return loss of the measured 21 states are -3.1 dB and -19.3 dB with standard deviations of 0.6 dB and 6 dB, respectively.*

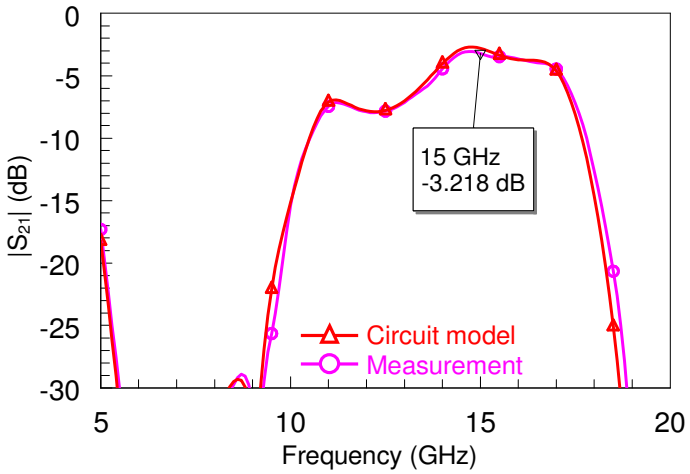
It should be emphasized once more here that the 10° phase resolution is only a demonstrator, and the performance is not limited to this value. The figure clearly demonstrates that 5° resolution is possible, and special effort is not spent to obtain measured the phase values for the gaps in the figure. The author truly believes that the whole insertion range of the PS can be covered with about 2° or 3° steps with a careful search among all possible states using optimization tools.

The reason of having a reduced insertion phase range is the change in the MEMS bridge heights, which resulted in a significant increase in C_{bu}, and hence significant changes in ϕ_{up} and $\Delta\phi$. The change in ϕ_{up} increases the minimum insertion phase of the DMTL interconnection lines and the DMTL stubs where the insertion phase is a vital parameter for the phase shift performance as explained previously in this chapter. The reduction in $\Delta\phi$ reduces the maximum insertion phase that can be

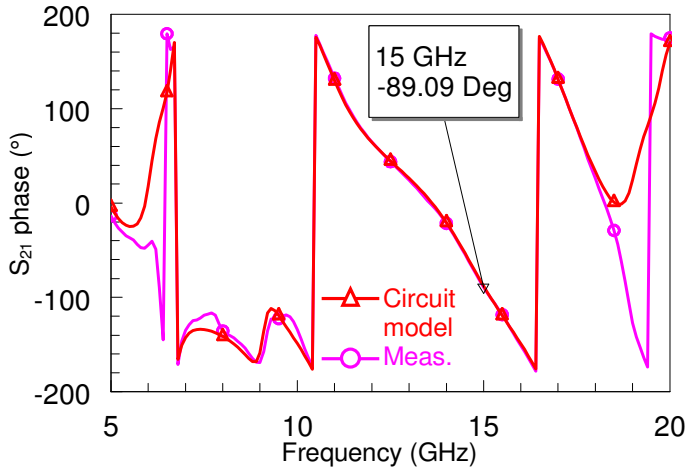
provided by the DMTL interconnection lines and the DMTL stubs, which is the second important parameter for the insertion phase performance of the PS. As a result of these changes, the electrical lengths that are necessary to obtain some insertion phase states of the phase shifter cannot be provided from the interconnection line and stubs DMTLs, which results with a reduced insertion phase range.



(a) $|S_{11}|$ of measured RF MEMS PS compared with the simulations.



(b) $|S_{21}|$ of measured RF MEMS PS compared with the simulations.



(c) $\angle S_{21}$ of measured RF MEMS PS compared with the simulations.

Figure 5.27: The measured performance of the RF MEMS PS (TRL calibration used) that is reconfigured to -90° @ 15 GHz compared with the simulations (Stb1 = 5, Stb2 = 235, Stb3 = 501, IntLine = 19) (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$.

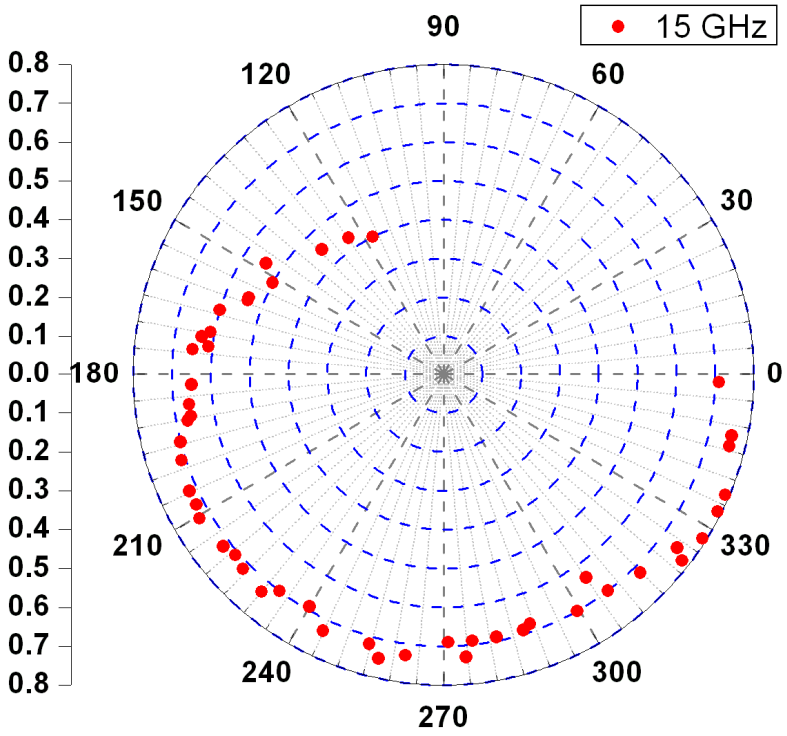
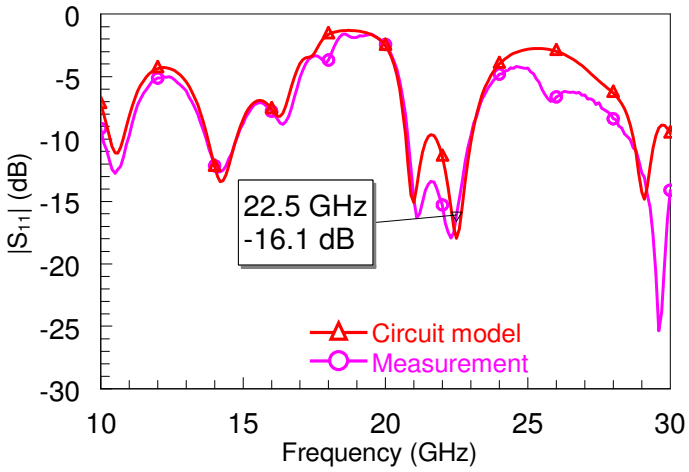


Figure 5.28: The S_{21} performance of the designed RF MEMS PS for all 36 phase states.

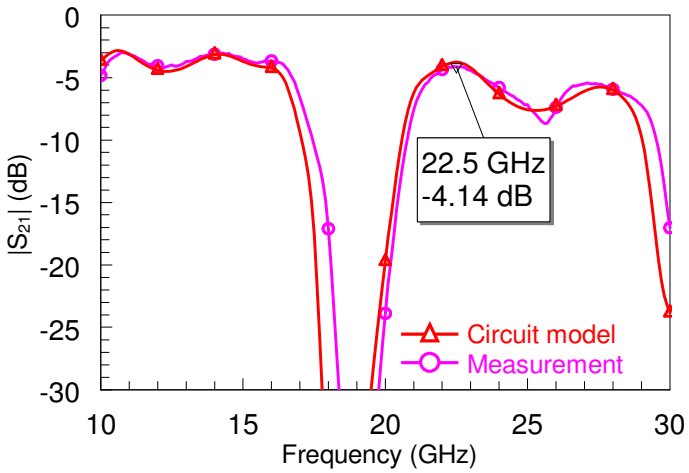
Although the insertion loss performance of the PS can be estimated once the circuit model parameters are extracted from the dedicated measurements, there occurred some difference between the initial design simulations and the measurements. The insertion loss of the PS was calculated as -2 dB in average among all 36 states during the design; however, the insertion loss is measured as -3.1 dB in average among the measured 21 states. This increase in the insertion loss is mainly due to the differences in the overall quality factor of MEMS and MAM capacitors between the simulations and measurements. These differences depend upon three main reasons. The first one is the EM simulation environment. It was observed in several different cases that HFSS underestimates the conductor losses in microstrip or CPW based structures, which results in a lower simulated insertion loss. This can easily be observed from the R_{bu} and R_{bd} values given in Table 5.8 that are extracted from the HFSS simulations and the measurements. During the extraction of R_{bu} and R_{bd}, a DMTL structure that is composed of only MEMS bridges at the center without any MAM capacitances as explained above; hence, the following effects, which will be explained next, are excluded. The second reason is due to the changes in the bridge heights of the MEMS switches and MAM capacitors. The variations in the bridge heights totally change the RF current distributions. These changes directly affect the coupling to the bias line, and hence, the values of R_{bias} resistors, which is the dominant mechanism of losses in the DMTL unit sections in this thesis. The final reason is the increase in R_{bu} and R_{bd} because of the material properties in the fabrication process. The conductivity of the second metal layer which is used to implement MEMS bridges has a lower conductivity than the first (CPW) metal layer. This is because the second metal layer has to have very low residual stress, and the deposition conditions were optimized to reduce the residual stress as much as possible. The conductivity of this layer decreases as a consequence, which, in return, results with increase in R_{bu} and R_{bd}. Moreover, the conductivity of the electroplated gold layer that is used to fill the anchors of the MEMS and MAM capacitances is much lower than that of the sputtered gold layer that is used for the first metal layer, which is another reason for the increase in R_{bu} and R_{bd}.

One point that should be added to the loss is discussion is that the loss contributions of the T-junctions and the 50 Ω-to-50 Ω CPW transitions, which are only composed of gold metal layers. These losses are also underestimated in the EM simulations. Considering that there are three T-junctions and two transitions (SOLT version) in the PS, small differences between the measured and the simulated values are multiplied by a factor of 3 and 2, respectively.

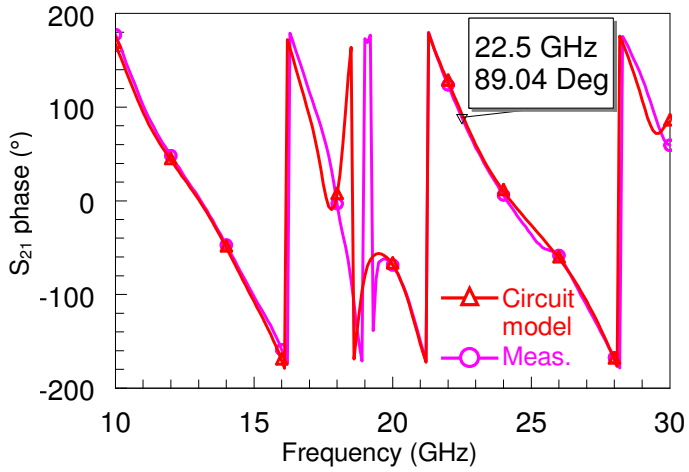
Although the phase shifter is designed at a center frequency of 15 GHz and modeled for 5-20 GHz band, it is also possible to operate the PS at higher frequencies. It was already shown in Figure 5.26 that the upstate performance of the PS was in good agreement up to 30 GHz and acceptable up to 40 GHz. Figure 5.29 and Figure 5.30 also show that the performance is quite good and in agreement with the simulations at 22.5 GHz and 30 GHz, respectively. These two frequencies are selected for demonstrative purpose, and the PS can work *at any center frequency* between 15 GHz and 30 GHz; and, the phase ranges and the insertion losses increase gradually from their corresponding levels at 15 GHz to their corresponding levels at 30 GHz.



(a) $|S_{11}|$ of measured RF MEMS PS compared with the simulations.

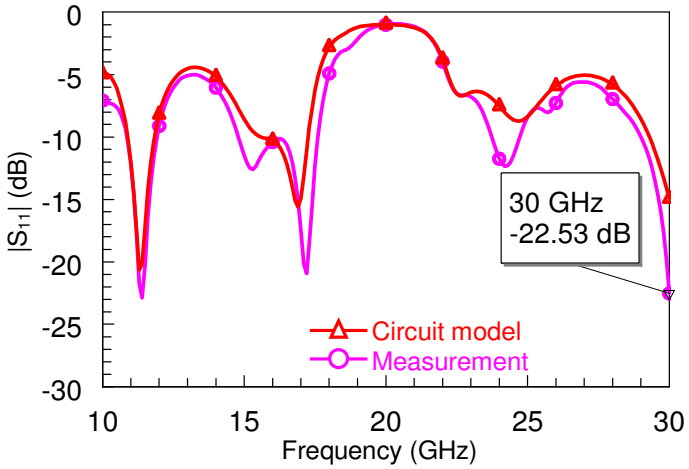


(b) $|S_{21}|$ of measured RF MEMS PS compared with the simulations.

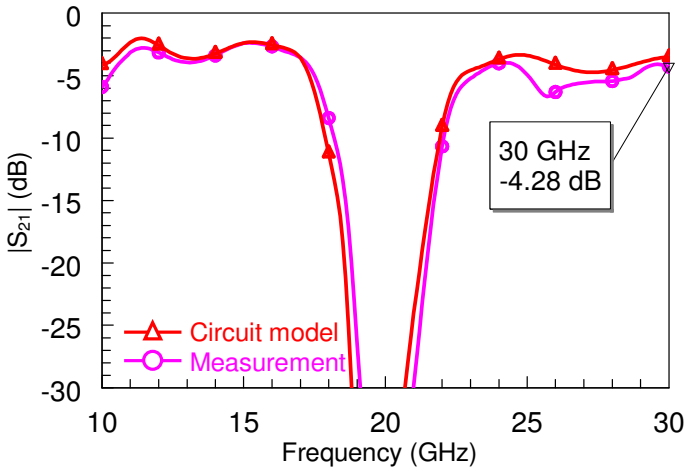


(c) $\angle S_{21}$ of measured RF MEMS PS compared with the simulations.

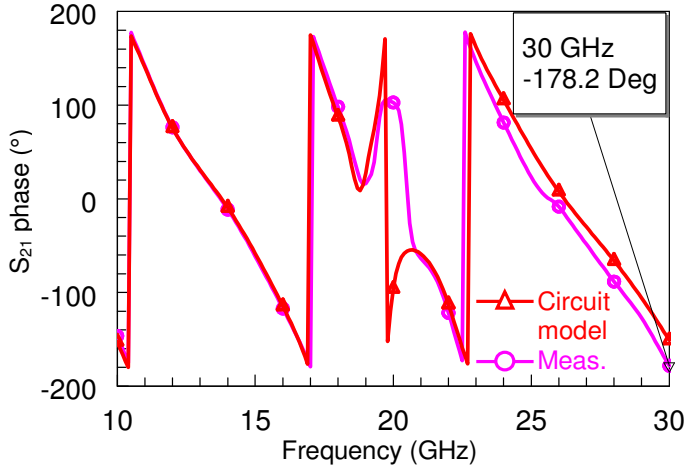
Figure 5.29: The measured performance of the RF MEMS PS (SOLT calibration used) that is reconfigured to 90° @ 22.5 GHz compared with the simulations (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$.



(a) $|S_{11}|$ of measured RF MEMS PS compared with the simulations.



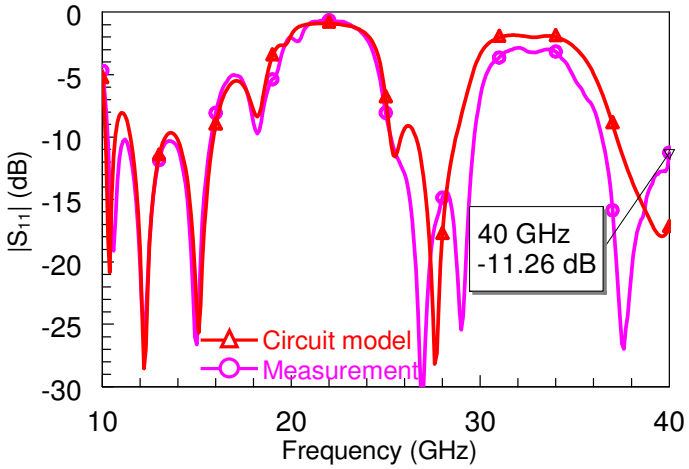
(b) $|S_{21}|$ of measured RF MEMS PS compared with the simulations.



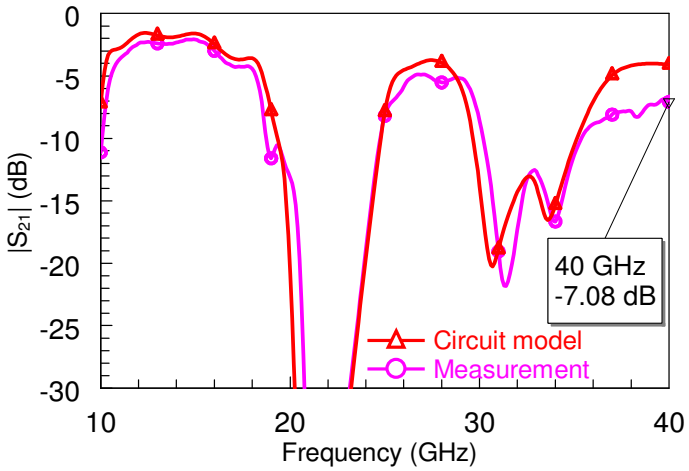
(c) $\angle S_{21}$ of measured RF MEMS PS compared with the simulations.

Figure 5.30: The measured performance of the RF MEMS PS (SOLT calibration used) that is reconfigured to 180° @ 30 GHz compared with the simulations (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$.

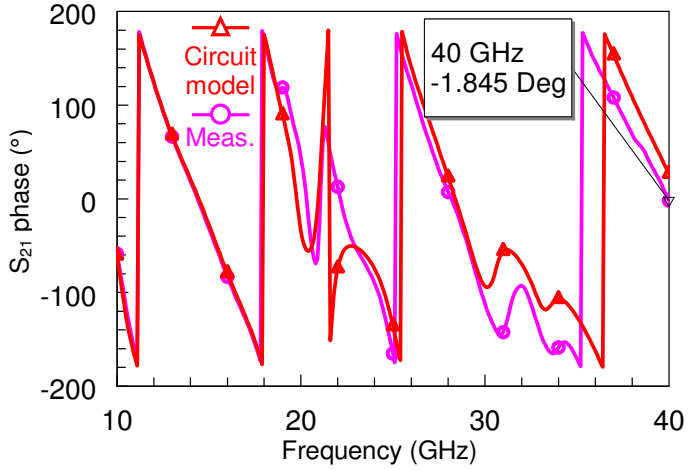
Figure 5.31 also shows the PS performance that is reconfigured for a specific phase state at 40 GHz. Here in this range, the return loss levels stay in an acceptable range around -10 dB; however, the insertion loss starts to deviate from the extracted simulations whereas the insertion phase performance shows an almost constant offset at each frequency. Nonetheless, it is possible to use the PS between 30 GHz up to 40 GHz using the reconfigurability of the design in spite of the shifted performance. Here, as the offset for each frequency is almost constant, the desired insertion phase value is obtained by reconfiguring the design to the desired insertion phase value plus the phase offset at that frequency. Figure 5.32 shows the measured S_{21} performance of the RF MEMS PS at 22.5 GHz, 25 GHz, 27.5 GHz, 30 GHz, 35 GHz, and 40 GHz frequencies. Again, these frequencies are selected as some sample points for demonstrative purposes to show that the PS can work on each frequency in the band of interest. As can be seen from the graphs in Figure 5.32, the insertion phase range gradually increases up to 25 GHz, which is expected since the electrical lengths of the DMTL stubs increase as the frequency increases. The insertion phase range is covered with maximum 5° steps, which also means that the phase resolution is still not lost. However, the insertion phase range ceases to increase and stays about the same level up to 30 GHz while some gaps within some parts of the insertion phase range starts to occur. Finally, the insertion phase range starts to decrease after 30 GHz, and the gaps become more evident. The average insertion losses increase gradually up to 30 GHz; moreover, they increase more rapidly after 30 GHz as expected. The performance of the RF MEMS PS for the higher frequency operation is summarized in Table 5.9.



(a) $|S_{11}|$ of measured RF MEMS PS compared with the simulations.

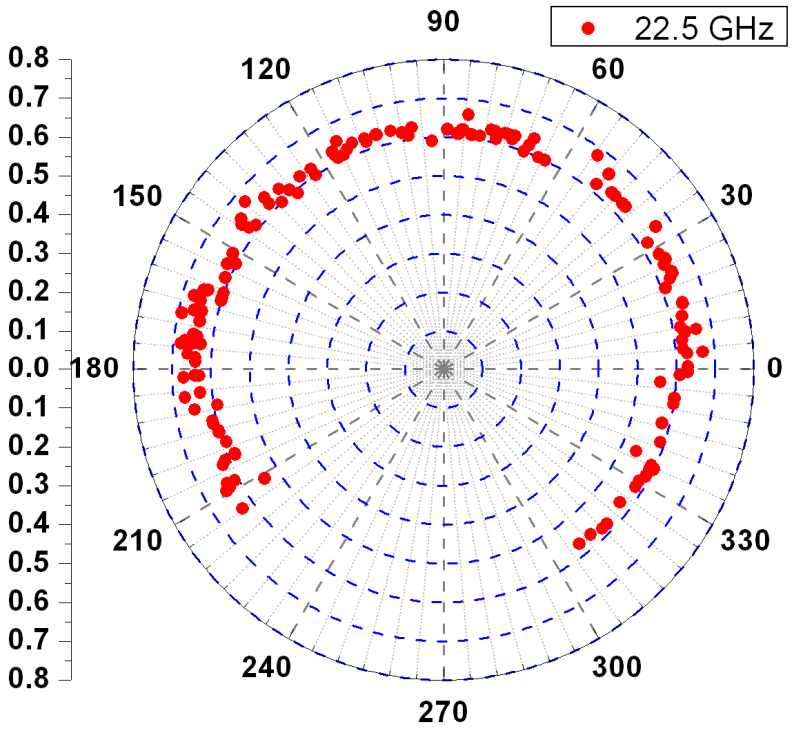


(b) $|S_{21}|$ of measured RF MEMS PS compared with the simulations.

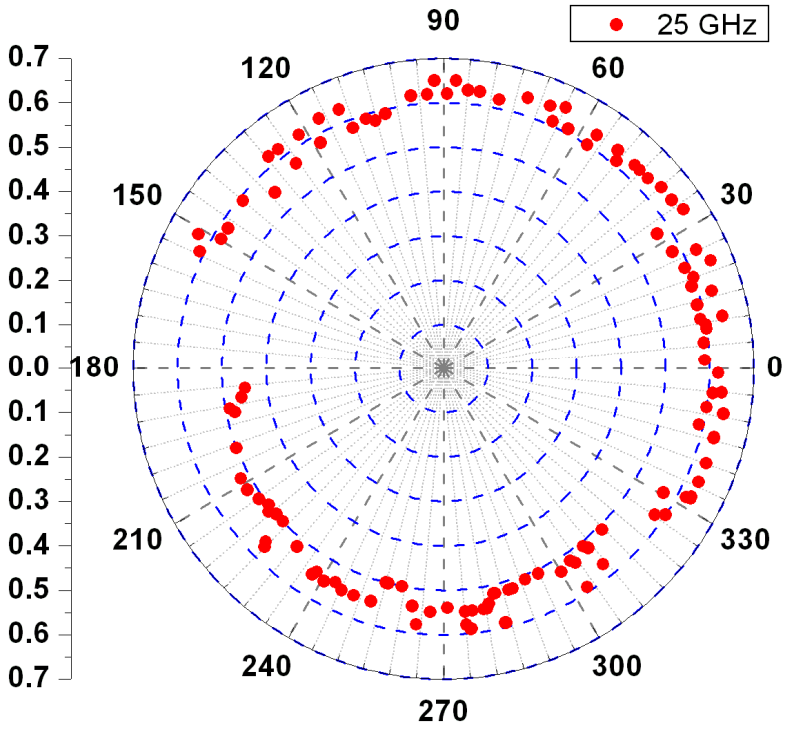


(c) $\angle S_{21}$ of measured RF MEMS PS compared with the simulations.

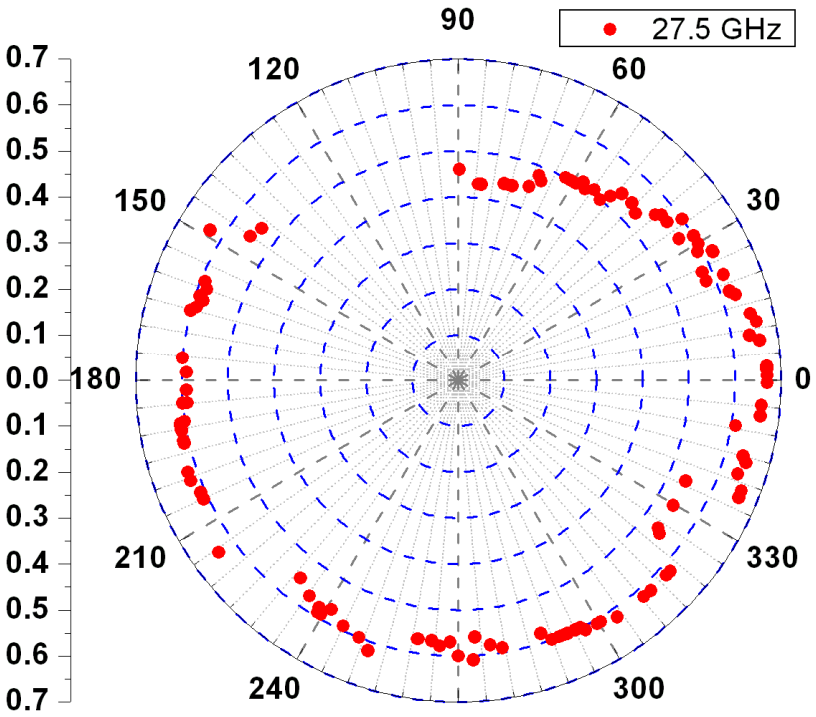
Figure 5.31: The measured performance of the RF MEMS PS (SOLT calibration used) that is reconfigured to 0° @ 40 GHz compared with the simulations (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$.



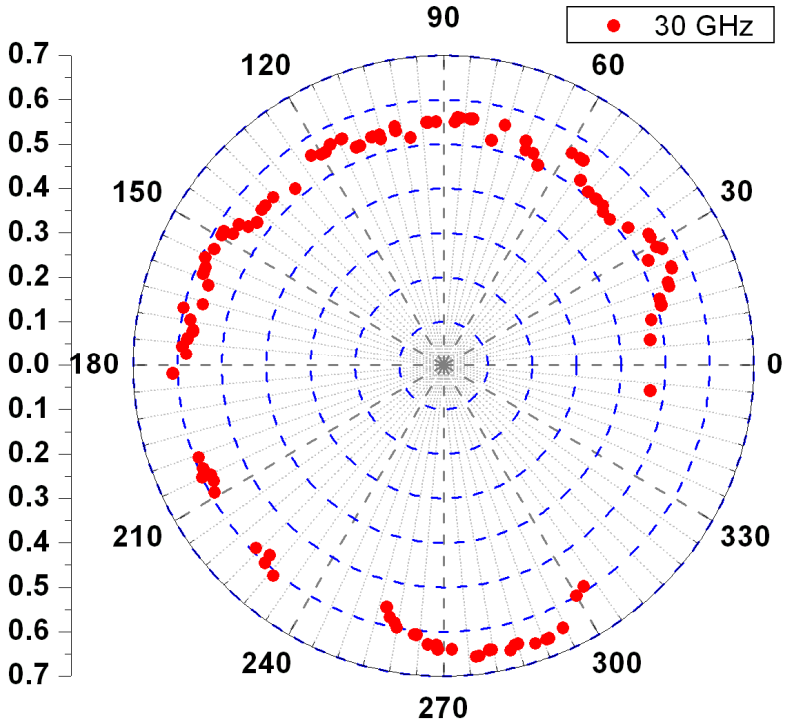
(a) 22.5 GHz.



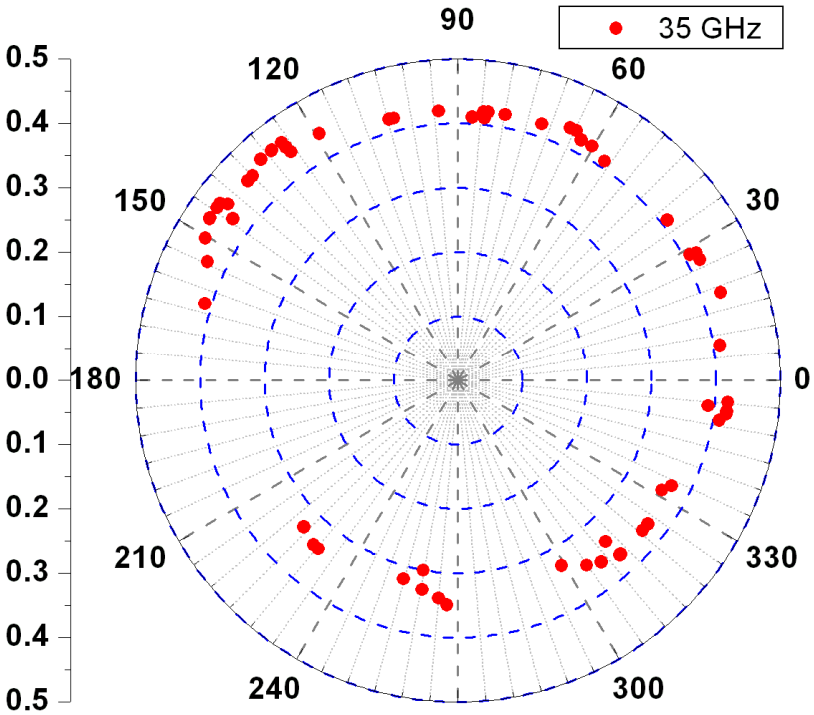
(b) 25 GHz.



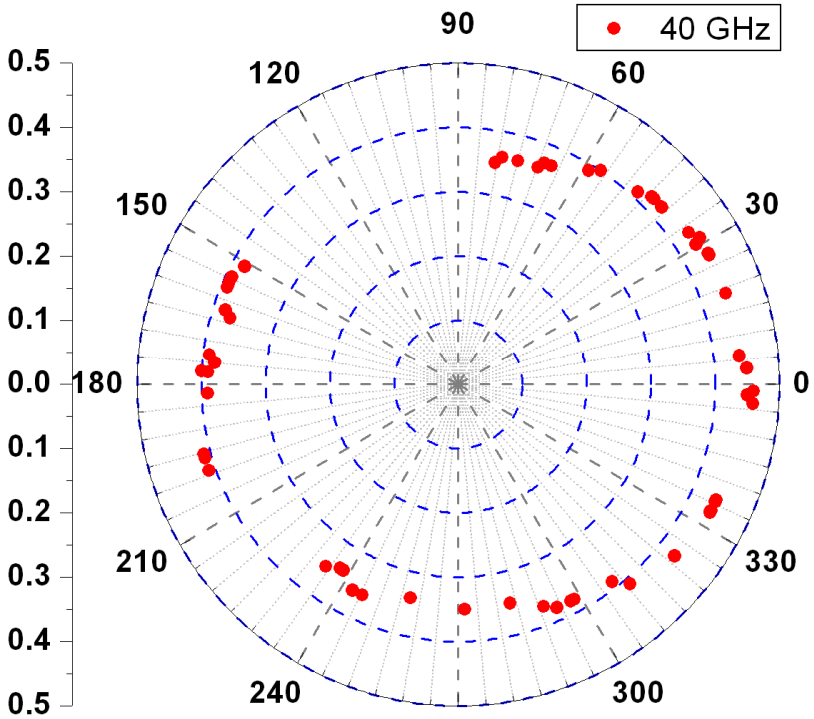
(c) 27.5 GHz.



(d) 30 GHz.



(e) 35 GHz.



(f) 40 GHz.

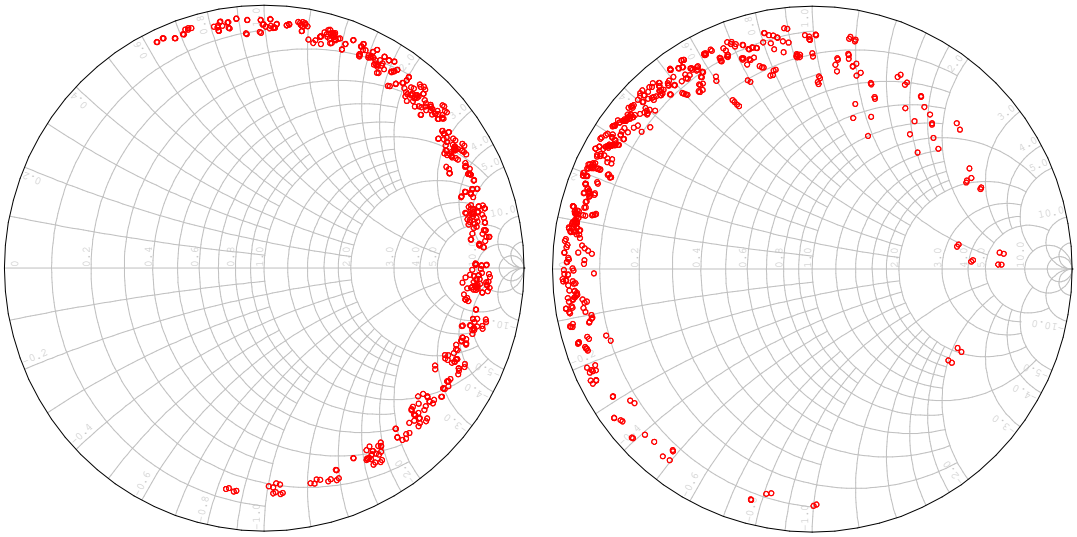
Figure 5.32: The measured S_{21} performance of the RF MEMS PS (SOLT calibration used) (a) 22.5 GHz (b) 25 GHz (c) 27.5 GHz (d) 30 GHz (e) 35 GHz (f) 40 GHz.

Table 5.9: The summary of measured performance of the RF MEMS phase shifter.

	Return Loss (dB)		Insertion Loss (dB)		Insertion Phase Range	Max. Phase Shift
	Mean	Std. Dev.	Mean	Std. Dev.		
15 GHz	-19.3	6.20	-3.1	0.65	160-360°	200°
22.5 GHz	-18.7	6.26	-4.1	0.38	0-215° ∪ 305-360°	270°
25 GHz	-18.2	4.00	-4.8	0.72	0-155° ∪ 185-360°	330°
27.5 GHz	-16.9	4.63	-4.7	0.90	0-090° ∪ 145-360°	305°
30 GHz	-15.3	3.58	-5.0	0.70	5-305° ∪ 355-360°	305°
35 GHz	-14.6	3.72	-7.8	0.95	0-165° ∪ 225-360°	300°
40 GHz	-13.9	3.47	-8.0	0.76	0-80° ∪ 150-360°	290°

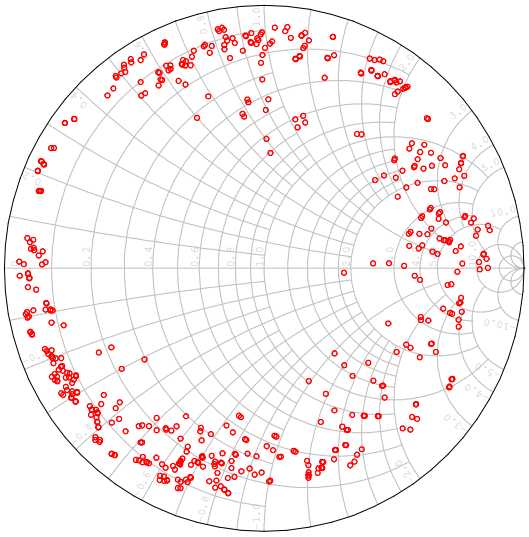
The reduction in the phase shifter performance is understood better if the performance of the DMTL stubs is investigated in more detail in the band of interest. Figure 5.33 shows the simulated S_{11} performance of the DMTL stub using the circuit parameters that are extracted from the dedicated measurements as explained previously. It is observed in Figure 5.33-(a) that the S_{11} of the DMTL stub goes very close to the Smith Chart periphery, which is required for the proper phase shifter operation. However, as the frequency increases, the S_{11} points commence not only to move away from the periphery, which, in case, means that a considerable real part is added to the DMTL stub reflection coefficient, but also the phase difference between the points commence to increase. This situation becomes even more dramatic as the frequency is greater than 30 GHz, which can be seen in Figure 5.33-(c) and (d). As a result, the DMTL stubs cannot provide the necessary reflection coefficient; and hence, the insertion losses increase significantly, and some insertion phase values cannot be obtained. The distortion in the S_{11} performance of the DMTL stub because the losses increase notably as the operation frequency increases, and more importantly, the operation frequency gets closer to the Bragg frequency of DMTL UST-III, which was extracted as 54 GHz. It should be pointed out here that for a proper DMTL operation, the Bragg frequency is usually selected at least more than two times of the design frequency. In this

case, the operation frequency becomes only 1.8 and 1.35 times of the Bragg frequency for 30 GHz and 40 GHz, respectively.

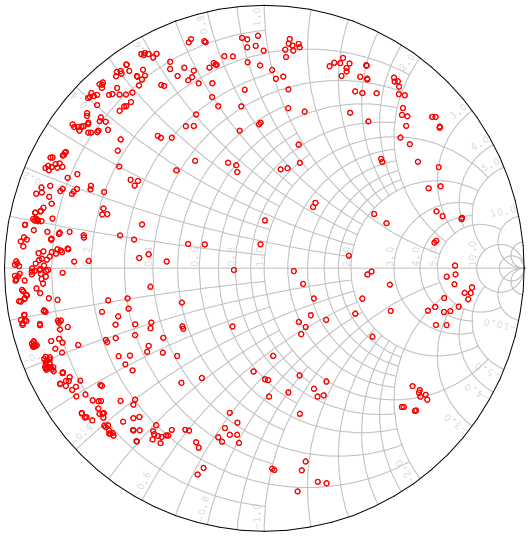


(a) 15 GHz

(b) 25 GHz



(c) 30 GHz



(d) 40 GHz

Figure 5.33: The simulated S_{11} characteristics of the DMTL stub design for all possible 512 states with the extracted circuit model parameters at some measurement frequencies (a) 15 GHz (b) 25 GHz (c) 30 GHz (d) 40 GHz.

5.4. Conclusion

In this chapter, the design, the fabrication, and the measurement results of the RF MEMS phase shifter that is based on the TST. The measurement results show good agreement with the simulations. The PS has good phase error, insertion loss, and return loss performance at the center design frequency, 15 GHz; however, the insertion phase range decreased due to reduced MEMS bridge height. The PS can also work frequencies up to 40 GHz with gradually increasing insertion phase ranges and insertion losses using the reconfigurability of the design. The phase errors that occur at any insertion phase state can be easily overcome using again the reconfigurability of the design for the frequencies up to 40 GHz.

CHAPTER 6

RF MEMS VECTOR MODULATOR USING TRIPLE STUB TOPOLOGY

6.1. Introduction

This chapter presents a novel RF MEMS vector modulator that is based on triple stub topology (TST). The vector modulator (VM) is uses the same idea with the RF MEMS phase shifter that was presented in the previous chapter; moreover, the amplitude of the input signal is also controlled with the VM. The theory of simultaneous phase and amplitude control was explained in Chapter 4. As explained previously, the theoretical approach results with a range of interconnection line lengths instead of a unique solution for a given insertion phase value. In addition to the phase control, the amplitude of the signal is controlled by selecting the interconnection line length such that the structure shows a resonating behavior between its open-circuited terminations at the end of the stubs. By tuning the interconnection line length and changing the "distance" to the resonance point, the amplitude of the input signal can be controlled simultaneously with the insertion phase while the input return loss is theoretically kept as 0.

In this chapter, first, the design of the RF MEMS vector modulator is presented that explains the design of each part of the circuit. Following the design, the results of the fabrication process of the designed VM are presented. Then, the measurement results of the VM are given. Finally, the measurement results and the performance of the VM are discussed, which is followed by the chapter conclusion.

6.2. The Design of the RF MEMS Vector Modulator

The VM design basically uses the same topology that was presented in Figure 5.2. The electrical lengths of the stubs and the interconnection lines are adjusted by means of the DMTLs. The methodology followed for the design of the VM is the same of that of the PS.

The VM design targets to cover *0-360° phase range with 45° resolution and to have three amplitude states, which are -2 dB, -5 dB, and -8 dB states*; this means that the VM design targets a total of 24 insertion phase/amplitude states. The -2 dB is the average insertion loss of the VM at 15 GHz; so, the minimum amplitude states are set to this value in order to minimize error between the design and the measurements.

The VM design has again three types of parts, which are the T-junction, the DMTL interconnection lines, and the DMTL stubs. The T-junctions in the VM are the ones that are used in the PS design since the T-junction that is used in the PS design is a general purpose design, and it also satisfies the requirements of the VM design.

For the DMTL interconnection line, the same DMTL design that is used in the PS is used. The reason for the design constraints was explained in Chapter 5.2.2. It should be kept in mind that the VM is also a 0-360° phase shifter in the minimum insertion loss states, and the current DMTL interconnection line satisfies the requirement of the phase shifter design. This DMTL interconnection line can also be used for the VM design. The reasoning is explained as follows: The current DMTL interconnection line is designed to cover 0 to 0.1λ and 0.4λ to 0.5λ electrical length range, which was necessary for the phase shifter to be able to cover $\pm$40° insertion phase range. For the remaining phase range, either 0.1λ or 0.4λ electrical length states of the DMTL interconnection line is used (please see Figure 5.7), where the insertion loss for the remaining states are more than their minimum values in this

case. Once the DMTL interconnection line length goes from 0.1λ to 0 or 0.4λ to 0.5λ, the insertion losses in the remaining insertion phase states increase, which means that the amplitude can also be controlled for these states. As the electrical length of the DMTL interconnection line changes in small steps in 0 to 0.1λ and 0.4λ to 0.5λ range, the amplitude of the remaining insertion phase states can also be controlled precisely.

The requirements of the DMTL stubs are, however, totally different from that of the PS, and the DMTL stub is designed considering the specific requirements of the VM design as explained in the following subsection.

6.2.1. The DMTL stub Design

The design of the DMTL stub of the VM is very similar to that of the PS, which is targeted to obtain a one port circuit with constant amplitude and varying phase of its reflection coefficient. The reader is referred to Chapter 5.2.3 for the details of the design constraints and the methodology followed during the design.

The design targets of the DMTL stub of the VM are found by optimization since the analytical solution does not give explicit equations for the lossy case as explained in Chapter 4. However, the initial points for the optimization are found using (4.7) to (4.10), which is critical to find the solution. According to the results of the optimization, the phases of reflection coefficients should be in ranges -120° to 150°, -173° to 180°, and -137° to 139° for Stub1, Stub2, and Stub3, respectively. After this step, the DMTL interconnection and the T-junctions are inserted to the circuit, and the optimization is repeated to see whether the requirements are still the same. It was found out that some ranges are not necessary for all three stubs. The only common unnecessary range is 0° to 70° for all of the stubs. In order to simplify the VM structure, a single DMTL stub has been

designed that uses only one type of DMTL unit section, which is DMTL UST-IV. So, the design target for the phase range of the reflection coefficient is selected as 70° to 360° for the DMTL stub.

To obtain the required phase range, DMTL Unit Section Type IV is designed using (5.1)-(5.11) in Matlab, and to check if the electrical length of the stub is enough to cover the specified range, 9 UST-IVs are cascaded with the T-junction extension, and the phase of the reflection coefficient is checked. The maximum number of DMTL unit sections that can be controlled independently is 9 as explained in the previous section. Since the phase range cannot be covered easily with 9 DMTL unit sections, 4 additional DMTL unit sections are added in order to shift the points with minimum and maximum reflection coefficient phases. The final DMTL stub has 13 unit sections of UST-IV, the first four of which is held only in the upstate.

The DMTL UST-IV designed in Matlab is also simulated in HFSS v9.2 to verify and optimize the design. During the simulations, the same physical dimensions are used for the CPWs, and the physical parameters of the MEMS center capacitance, C_b, and the MAM capacitances, C_s, are extracted using capacitance formulation (3.1) to (3.3) given in Chapter 3 as explained previously. The values of the parameters used in the initial design with DMTL formulation are given in the first column of Table 6.1. The 3D view of the final DMTL UST-III design and its physical dimensions are given in Figure 6.1 and Table 6.2, respectively.

Table 6.1: The circuit design parameters of the DMTL UST-IV.

	DMTL Formulation	**Circuit Model HFSS Sim.**
Z_o	96 Ω	96 Ω
$\varepsilon_{r,eff}$	2.36	2.36
α	40 dB/m @20 GHz	40 dB/m @20 GHz
f_{Bragg}	60 GHz	44 GHz
s	216 µm	210 µm
Z_{lu}	44.5 Ω	43.1 Ω
Z_{ld}	20 Ω	20.3 Ω
ϕ_{up}	-12.9°	-12.9°
ϕ_{down}	-28.6°	-28.3°
$\Delta\phi$	15.7°	15.4°
C_{bu}	50.4 fF	46.9 fF
C_{bd}	458.4 fF	469.2 fF
C_s	253.8 fF	471.5 fF
L_b	-	30 pH
R_{bu}/R_{bd}	-	1.6 Ω/0.15 Ω
C_U/C_D	42.1 fF/163.4 fF	42.7 fF/235.1 fF
Q_U/Q_D	-	131/99
R_{bias}	-	1665 Ω
$R_{bias,DC}$	-	10.125 kΩ

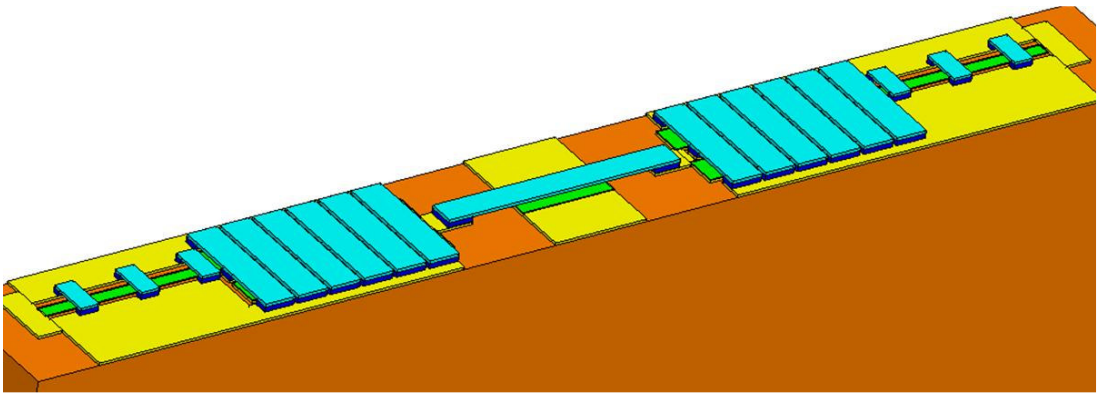
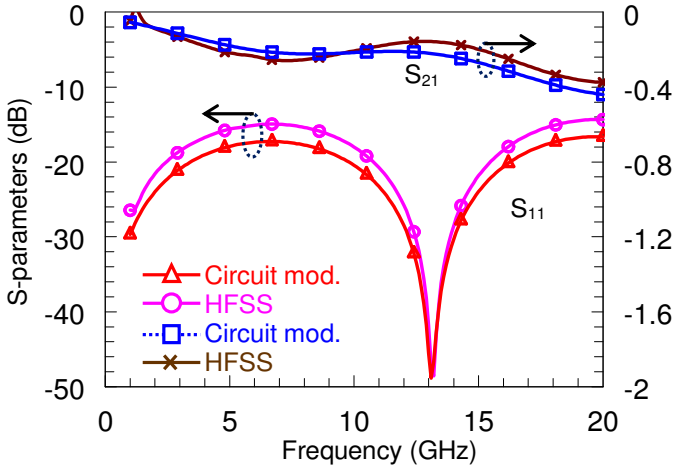


Figure 6.1: 3D view of the DMTL UST-IV (z-dimension exaggerated).

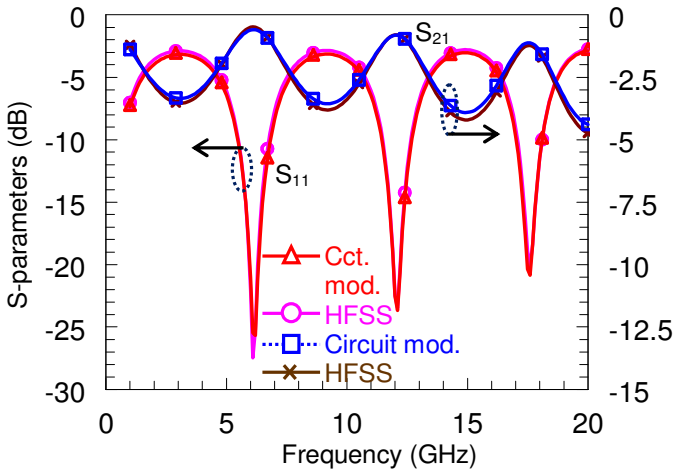
Table 6.2: The physical design parameters of the final design of the DMTL UST-IV.

Parameter	UST-IV
W	150 µm
G	150 µm
l_{brd}	300 µm
w_{brd}	38 µm
w_{gnd}	46 µm
$l_{brd\text{-}g}$	138 µm
$w_{brd\text{-}g}$	6 x 48 µm
w_{go}	30 µm
l_{go}	40 µm
w_{SiCr}	20 µm

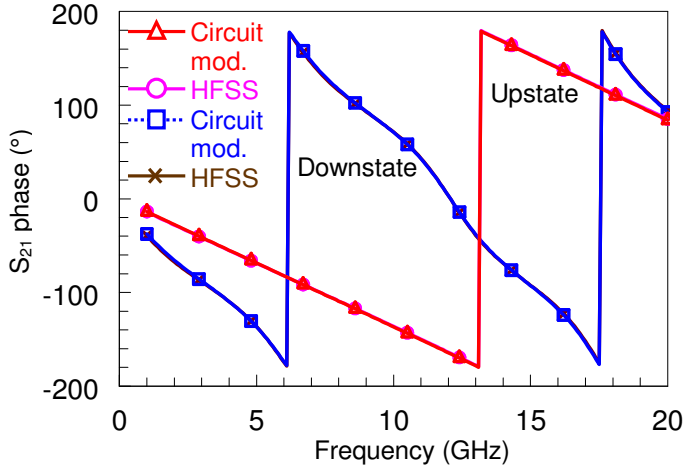
Figure 6.2 gives the comparison of the HFSS simulations with the proposed circuit model simulations. For the comparison of the HFSS simulations and the circuit model, 16 unit section of UST-IV are cascaded and compared with the results of the 16 cascaded simulation results of the HFSS model. The circuit model parameters that are extracted from the HFSS simulations are given in the second column of Table 6.1. The simulation results again show that the model is successful in predicting the EM full-wave simulations, which is also quantitatively given in Figure 6.2-(d). Lastly, Figure 6.3 shows the S_{11} characteristics of the final DMTL stub design for all possible $2^9 = 512$ possible states, in which 4 + 9 UST-IVs are cascaded and terminated with an open circuit. The first 4 UST-IVs are only used in the upstate, so the number of the states of the DMTL stub does not change. The circuit that is used for the simulation of the DMTL stub also includes the transmission line that models the T-junction extension. The simulation results show that the circuit satisfies the design requirements of the RF MEMS vector modulator.



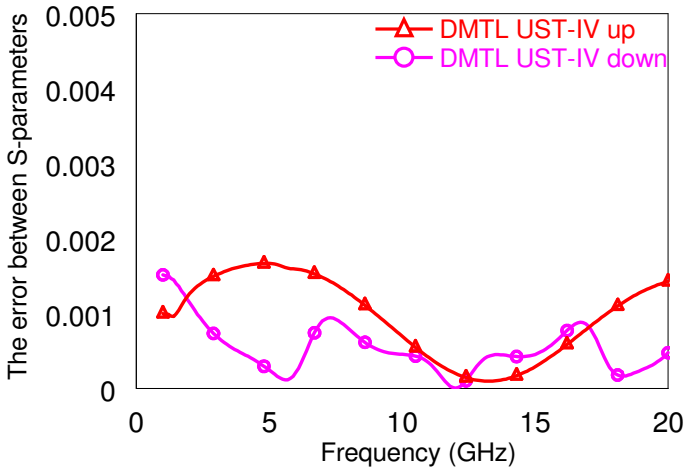
(a) $|S_{11}|$ and $|S_{21}|$ of DMTL UST-IV in upstate (16 unit sections cascaded).



(b) $|S_{11}|$ and $|S_{21}|$ of DMTL UST-IV in downstate (16 unit sections cascaded).



(c) $\angle S_{21}$ of DMTL UST-IV in both states (16 unit sections cascaded).



(d) The error between the S-parameters of the circuit model and the HFSS simulations of DMTL UST-IV for all cases.

Figure 6.2: The comparison of the S-parameters of the circuit model and HFSS simulations for the DMTL UST-IV. The graphs are the results of cascaded 16 unit sections both for the circuit model and the HFSS simulation results (a)-(c) Magnitudes and phases of the S-parameters (d) The error between the S-parameters of the circuit model and the HFSS simulations for all cases.

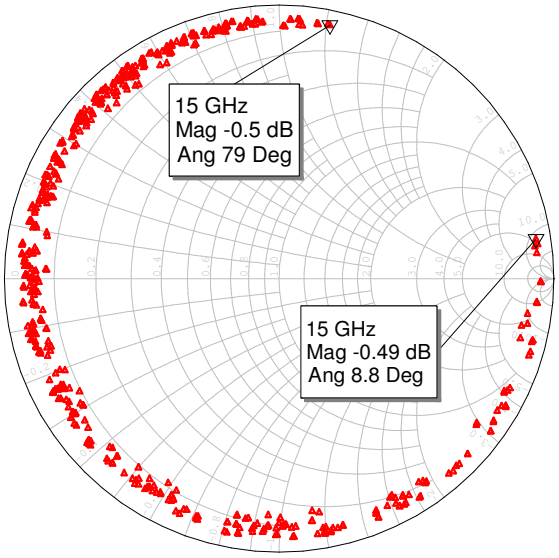


Figure 6.3: The S_{11} characteristics of the DMTL stub design that is composed of 4 + 9 DMTL UST-IVs for all possible 512 states.

6.2.2. The Overall RF MEMS Vector Modulator Design

Figure 6.4 shows the layout of the RF MEMS vector modulator. The design has 32 control pins, which has the same pin diagram with the RF MEMS PS. Each stub has 9 control pins, and two interconnection lines are controlled by 5 control pins. The layout of the design measures 9850 μm × 6755 μm^2, including the 50 Ω-50 Ω transitions. These transitions are necessary in order to decrease the CPW pitch spacing as explained in Chapter 5.3.

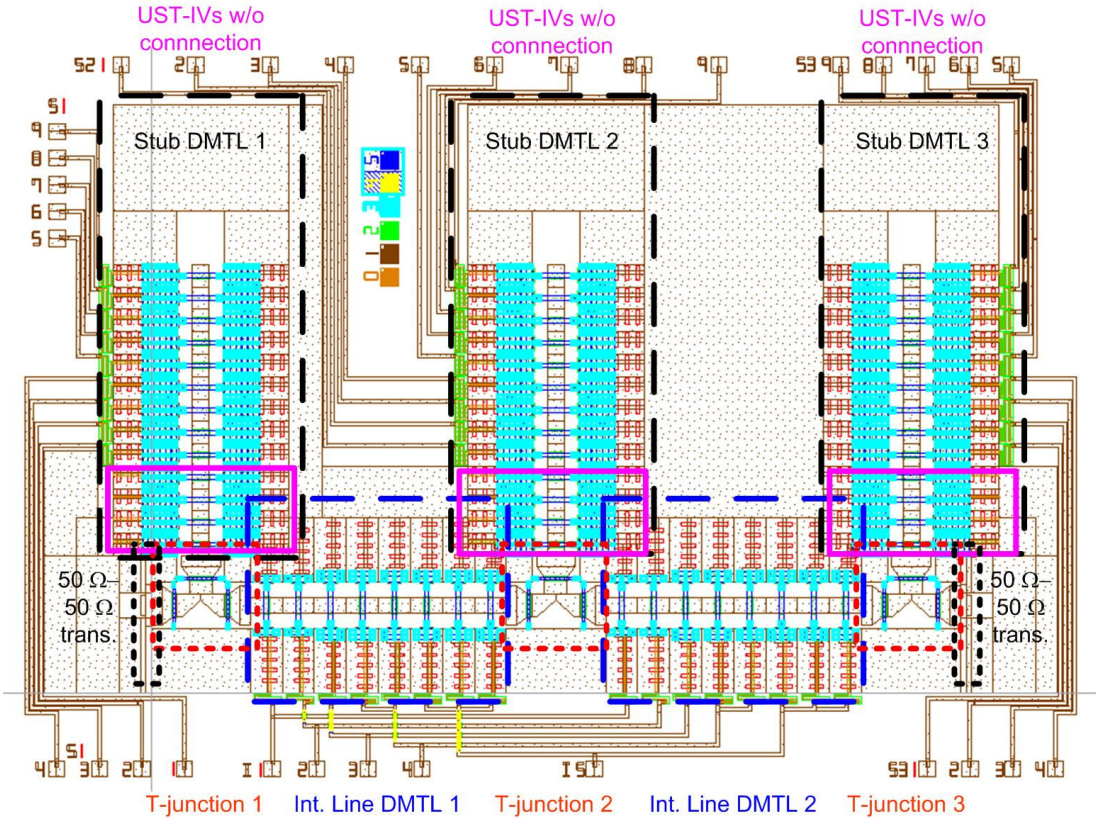


Figure 6.4: The layout of the final RF MEMS VM design.

For the final simulation of the RF MEMS VM, the same methodology that is used during the design of the PS is followed. The method is based on cascading the ABCD parameter of the separately designed subparts, and the details were explained in

Chapter 5. The states of the stubs and the interconnection lines for each insertion phase/amplitude state are found in two ways. The first one is to select the states that give the closest electrical lengths to the required value determined by the method explained in Chapter 4. The second way is to use the optimization method in which the states of the three stubs and the interconnection lines are used as the optimization variables.

The simulations results of the RF MEMS VM are shown in Figure 6.5, and the corresponding data is given in Table 6.3. The design targets of the VM are to cover 0-360° range with 45° steps and to have three amplitude states, which are -2 dB, -5 dB, and -8 dB. The design center frequency is 15 GHz. *The average phase errors is 1.31°, the average amplitude error is 0.08 dB, and the average return loss is -17.6 dB with standard deviations of 1°, 0.2 dB, and 5.1 dB, respectively for all 24 states.* The return loss is better than -10.6 dB for all 24 states. The amplitude error performance of the VM becomes worse only around -2 dB / 135° and -2 dB / 180° states, which is due to the selection of the interconnection line electrical length as explained in Chapter 5.

It should be also pointed out here that 45° phase and 3 dB amplitude resolutions are definitely not the lower limits for the VM design. The designed RF MEMS VM can easily be reconfigured to have a phase resolution of 5° with ±3° maximum phase error at the 0-360° range and an amplitude resolution of 0.2 dB with ±0.1 dB maximum amplitude error at -0.8 to -8 dB amplitude range and more than 80% of the 0-360° range. The amplitude range with minimum value less than -8 dB is also possible; however, the instantaneous bandwidth of the design drops rapidly as the minimum amplitude level is decreased.

Table 6.3: The final simulation results of the RF MEMS VM design for 0-360° range with 45° steps and -2 to -8 dB amplitude range with 3 dB steps.

Target		S_{11}	S_{21}		Amp.	Phase	Stub1	Stub2	Stub3	Int. Line
Mag (dB)	Ang (°)	Mag (dB)	Mag (dB)	Ang (°)	Err. (dB)	Error (°)	State	State	State	State
-2	0	-18.6	-2.03	-1	0.03	1	319	27	0	2
-2	45	-12.5	-2.09	44.3	0.09	0.7	231	320	327	1
-2	90	-17.8	-1.98	89	0.02	1	459	463	451	0
-2	135	-23.2	-2.89	136.4	0.89	1.4	200	244	320	31
-2	180	-31.1	-2.29	178.7	0.29	1.3	48	384	400	27
-2	-135	-19.5	-1.98	-134.7	0.02	0.3	62	232	44	14
-2	-90	-19.1	-2	-89.9	0	0.1	2	511	100	21
-2	-45	-10.6	-2.07	-46.8	0.07	1.8	0	0	19	4
	Avr.	-19.05	-2.17		0.18	0.95				

Target		S_{11}	S_{21}		Amp.	Phase	Stub1	Stub2	Stub3	Int. Line
Mag (dB)	Ang (°)	Mag (dB)	Mag (dB)	Ang (°)	Err. (dB)	Error (°)	State	State	State	State
-5	0	-13.4	-4.97	-1.4	0.03	1.4	37	506	154	0
-5	45	-21.4	-5	45.7	0	0.7	111	242	175	1
-5	90	-23.1	-5	90.1	0	0.1	127	264	275	1
-5	135	-19.8	-5.12	135.3	0.12	0.3	7	86	35	31
-5	180	-12.6	-4.97	178.2	0.03	1.8	164	43	1	26
-5	-135	-22.6	-4.98	-135.2	0.02	0.2	65	442	376	11
-5	-90	-16.2	-5.01	-87.22	0.01	2.78	64	78	254	11
-5	-45	-12.2	-4.99	-41.5	0.01	3.5	387	81	336	3
	Avr.	-17.66	-5.01		0.03	1.35				

Target		S_{11}	S_{21}		Amp.	Phase	Stub1	Stub2	Stub3	Int. Line
Mag (dB)	Ang (°)	Mag (dB)	Mag (dB)	Ang (°)	Err. (dB)	Error (°)	State	State	State	State
-8	0	-16.8	-8.06	-0.7	0.06	0.7	22	476	220	0
-8	45	-13.5	-7.89	44.2	0.11	0.8	444	504	445	0
-8	90	-15.1	-7.98	93.2	0.02	3.2	271	499	190	1
-8	135	-11.5	-7.95	137.3	0.05	2.3	511	89	210	29
-8	180	-17.2	-8.03	-178.7	0.03	1.3	256	154	388	18
-8	-135	-22.5	-8.03	-136.6	0.03	1.6	54	403	388	16
-8	-90	-22	-7.98	-89.6	0.02	0.4	415	312	425	30
-8	-45	-11.1	-7.98	-47.7	0.02	2.7	444	43	203	17
	Avr.	-16.21	-7.99		0.04	1.63				

Total avr.	-17.64	0.08	1.31
Total std. dev.	5.07	0.18	0.99

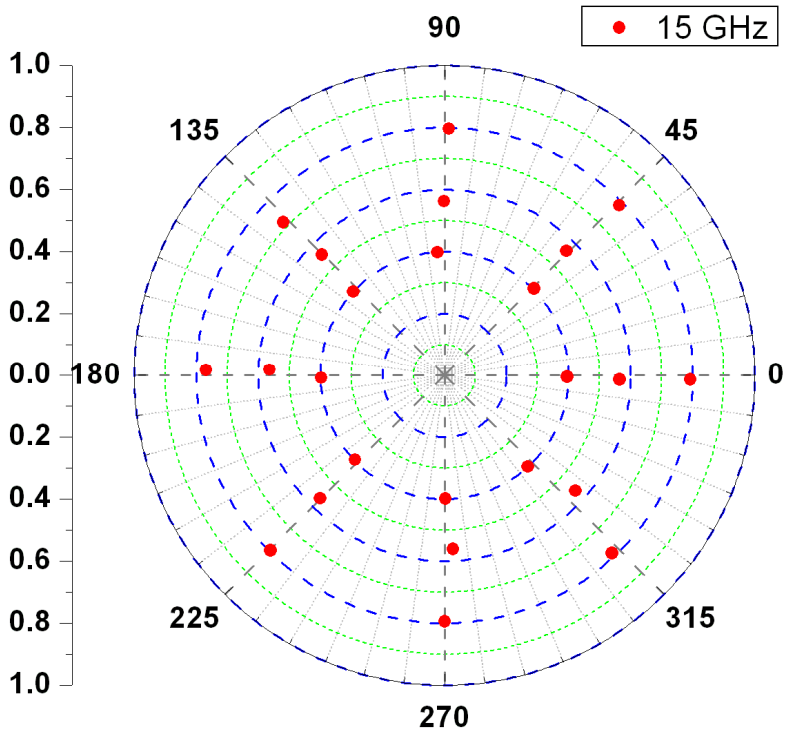
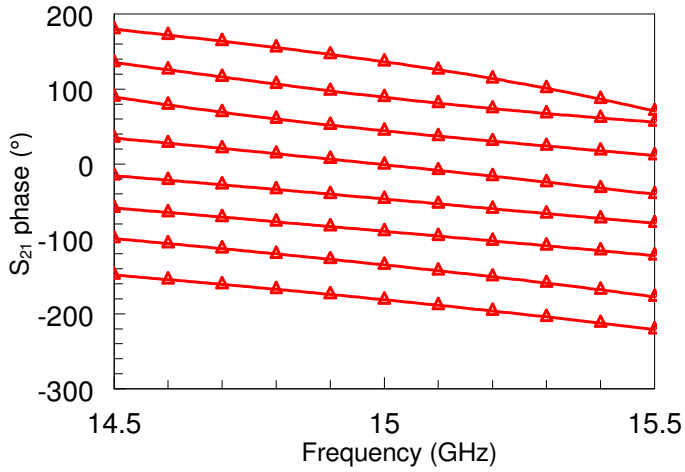
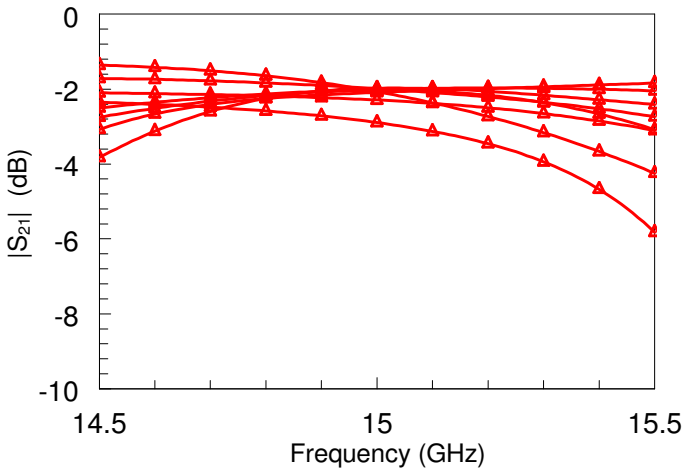


Figure 6.5: The S_{21} performance of the designed RF MEMS VM for all 24 insertion phase/amplitude states.

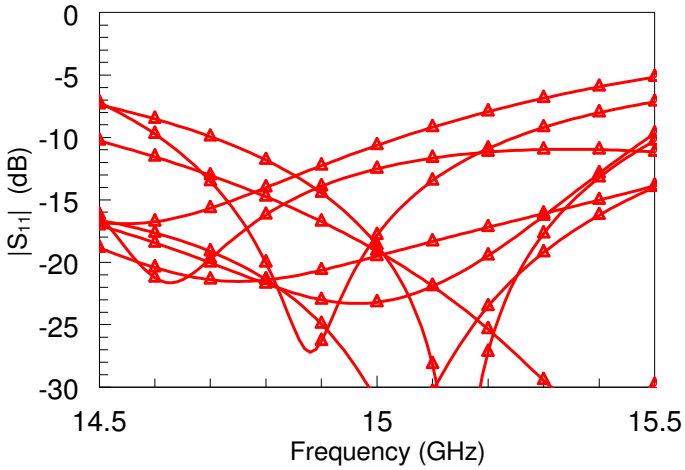
The frequency response of the designed VM is given in Figure 6.6. The design has a narrow instantaneous bandwidth since it is based on distributed structures. It has a bandwidth of about 400 MHz for the highest amplitude states, which is -2 dB, for ±0.5 dB amplitude error, and the performance is not limited by the phase, but the amplitude response. The bandwidth of the lowest amplitude states, which is -8 dB, is about 100 MHz for ±1 dB amplitude error. The reason behind having such narrow bandwidths with the decreasing amplitude is due to the resonating behavior of the design. As the amplitude decreases, the design is operated more closely to the λ/2 resonance point where the losses are maximum and the slope of the amplitude change very fast. *However, it should be kept in mind that the design is completely reconfigurable, the center frequency can be shifted to any frequency that is higher than the initial design frequency, where the instantaneous bandwidth is preserved.*



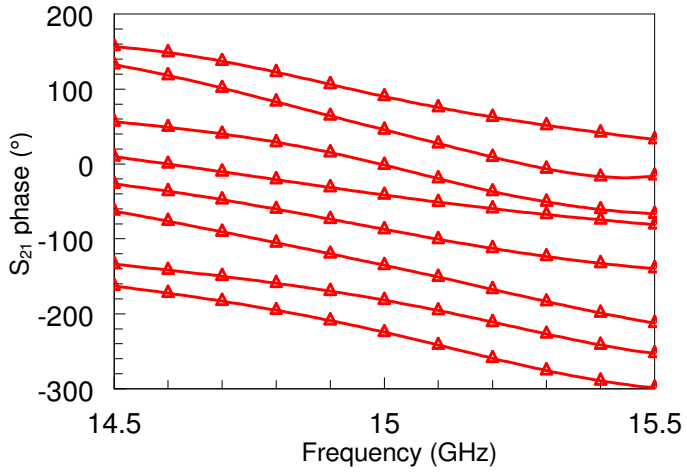
(a) $\angle S_{21}$ of RF MEMS VM for all -2 dB amplitude states.



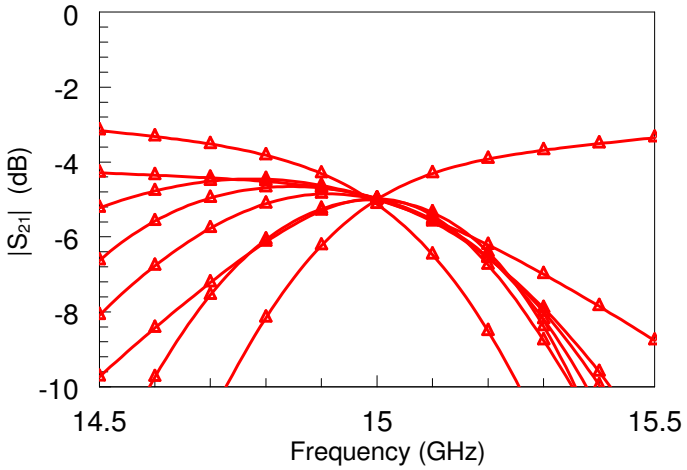
(b) $|S_{21}|$ of RF MEMS VM for all -2 dB amplitude states.



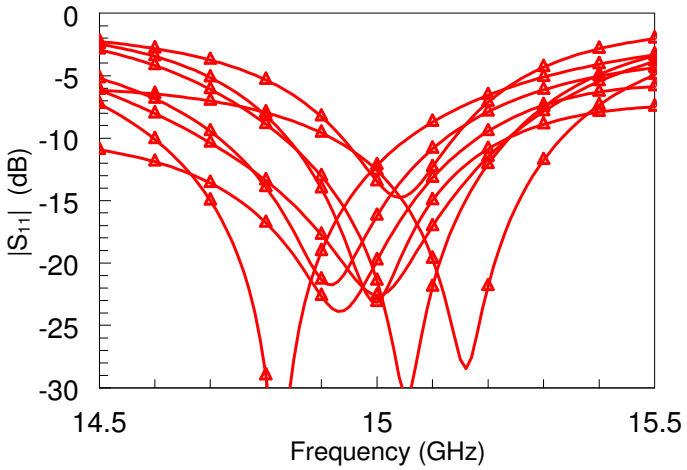
(c) $|S_{11}|$ of RF MEMS VM for all -2 dB amplitude states.



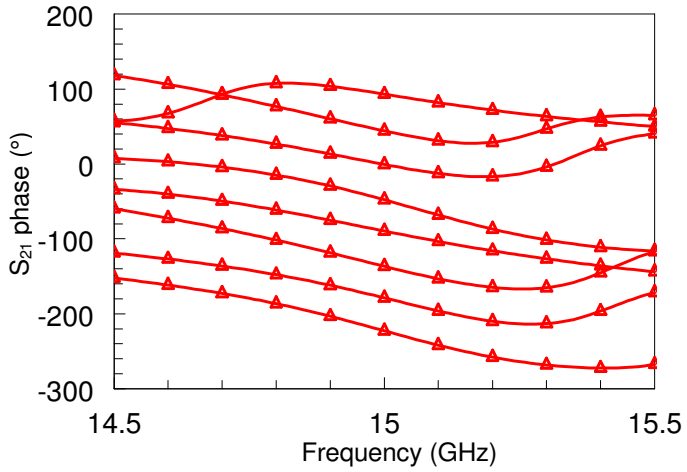
(d) $\angle S_{21}$ of RF MEMS VM for all -5 dB amplitude states.



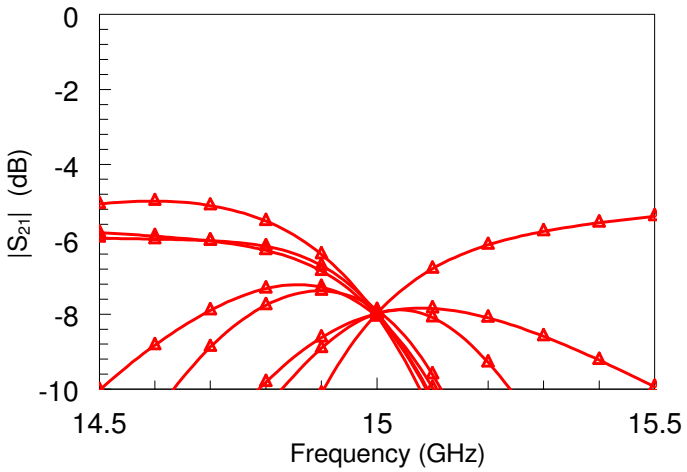
(e) $|S_{21}|$ of RF MEMS VM for all -5 dB amplitude states.



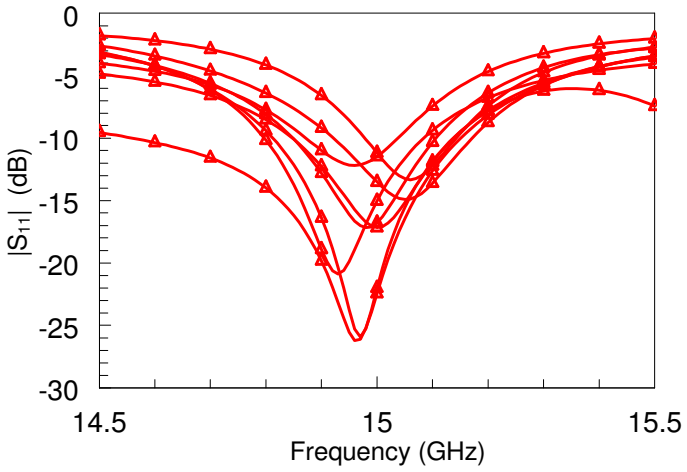
(f) $|S_{11}|$ of RF MEMS VM for all -5 dB amplitude states.



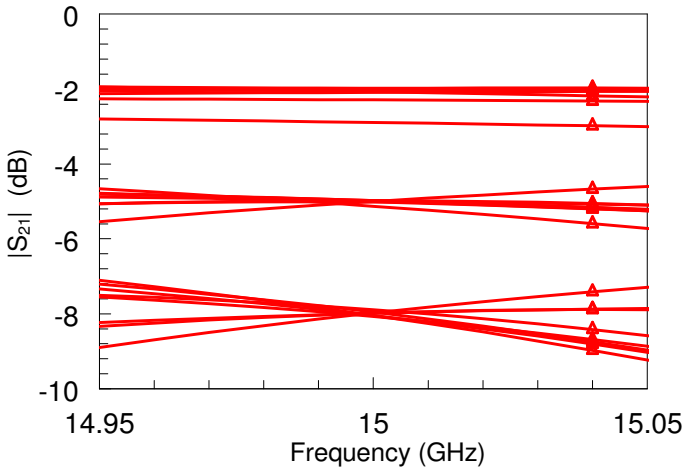
(g) $\angle S_{21}$ of RF MEMS VM for all -8 dB amplitude states.



(h) $|S_{21}|$ of RF MEMS VM for all -8 dB amplitude states.



(i) $|S_{11}|$ of RF MEMS VM for all -8 dB amplitude states.



(j) $|S_{21}|$ of RF MEMS VM for all 24 phase/amplitude states.

Figure 6.6: The performance of the designed RF MEMS VM. The performance for all (a)-(b)-(c) -2 dB (d)-(e)-(f) -5 dB (g)-(h)-(i) -8 dB amplitude states. (j) Amplitude linearity for all 24 states.

6.3. The Fabrication and the Measurement Results

The designed RF MEMS vector modulator is fabricated using the METU RF MEMS fabrication process, the details of which were given in Chapter 2. The photographs and the SEM pictures of the fabricated RF MEMS VM are given in Figure 6.7 and Figure 6.8, respectively. The RF MEMS VM measures 9850 μm × 6755 μm^2.

The fabricated vector modulator is mounted on CSB03228 ceramic IC package with the same method given in Chapter 3. The package dimensions of CSB03228 are 1.6 in × 0.595 in. Figure 6.9 shows the photograph of the packaged RF MEMS VM. The fabricated vector modulator is then measured using the MAMS setup explained in Chapter 5.3. SOLT calibration technique is used for the measurements of the RF MEMS vector modulator in 10-30 GHz frequency bands. Additional 50 Ω-50 Ω CPW transitions are also used for the SOLT measurements on both sides the VM as explained in Chapter 5.3.

The same MEMS switches are used in all types of DMTL unit sections; hence, the same actuation voltage is used in the test of the VM and all the other DMTL test structures. The actuation voltage of the MEMS switch is measured as 8 V, and all the MEMS structures are measured with 20 V bipolar waveform.

The DMTL UST-I and II, the T-junctions, and the transitions were characterized in the measurements of the RF MEMS phase shifter. So, the only remaining part in the measurement and characterization of the VM is the modeling and parameter extraction of the DMTL UST-IV, which is explained in the following subsection.

6.3.1. The DMTL Parameter Extraction

The characterization and the parameter extraction of DMTL UST-IV are made using the method applied during the measurements of the RF MEMS PS. In this method, dedicated DMTL structures are used for the extraction of DMTL circuit model parameters in groups. The dedicated DMTL structures are measured using the TRL calibration technique in 5-20 GHz frequency band. The details of the circuit model parameter extraction can be found in Chapter 5. The extracted circuit model parameters are given in Table 6.4, and the parameters are also compared with the simulated values within this table. Comparison of the measurement results of the DMTL, which is composed of 9 UST-IVs, with the circuit model simulations are given in Figure 6.10.

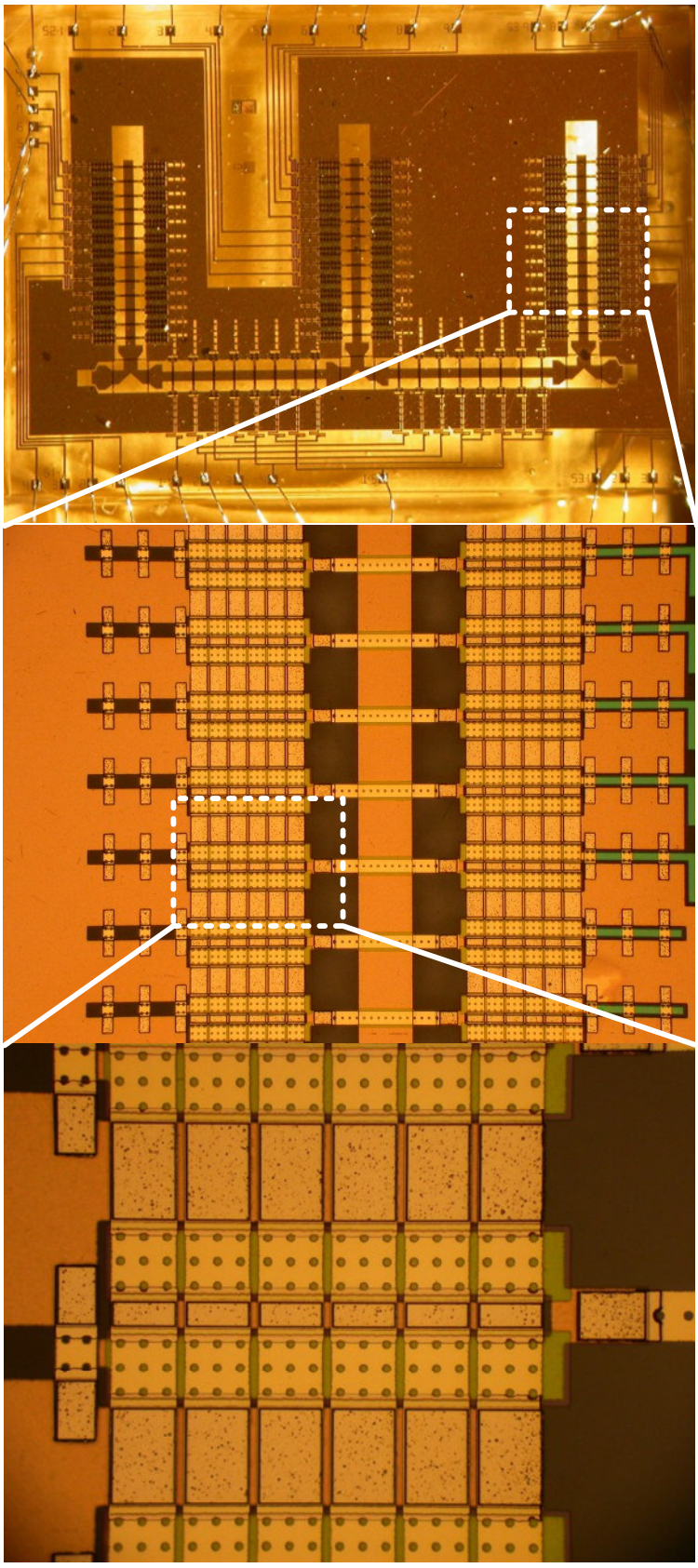
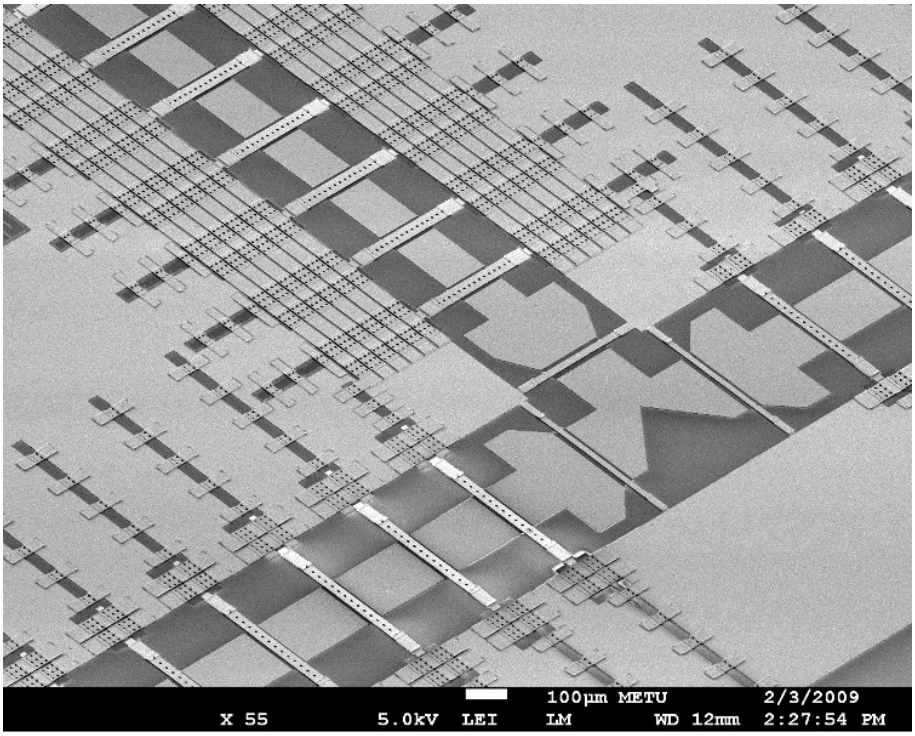
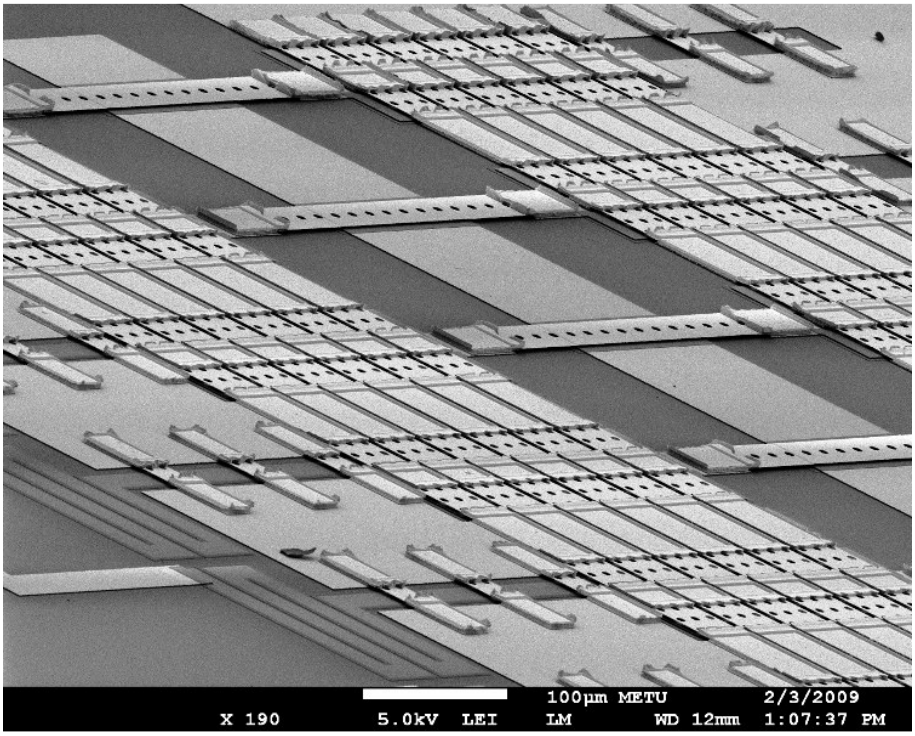


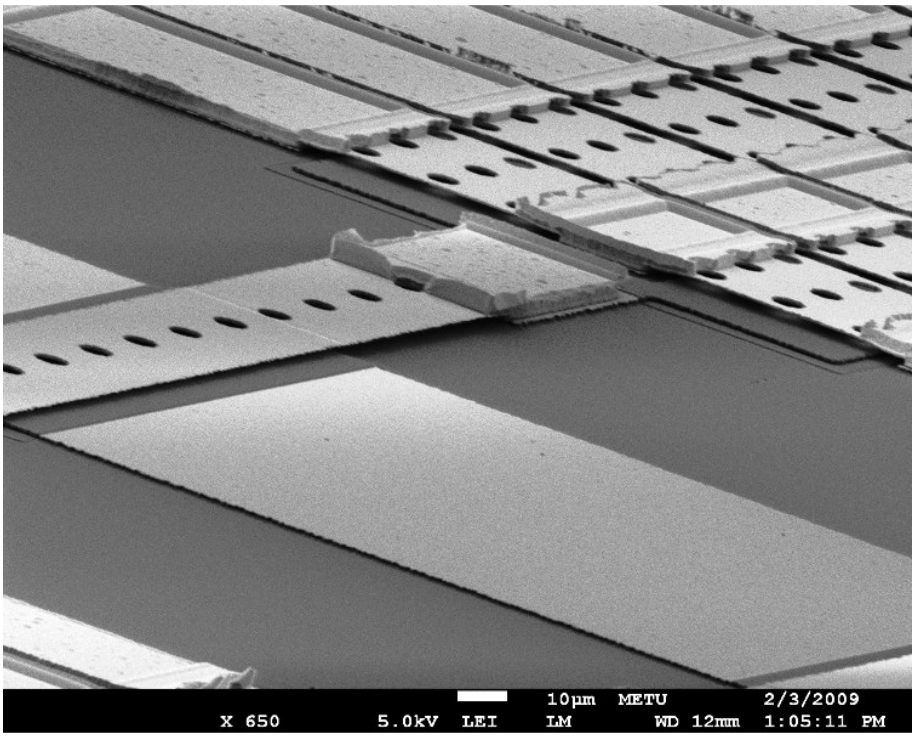
Figure 6.7: The photographs of the fabricated RF MEMS VM.



(a) Wide view of the DMTL interconnection line and the DMTL stub (UST-IV).



(b) The view of the of the DMTL stub (UST-IV).



(c) The closer view of the of the MEMS bridge and the MAM capacitor (UST-IV).

Figure 6.8: The SEM pictures of the fabricated RF MEMS VM.

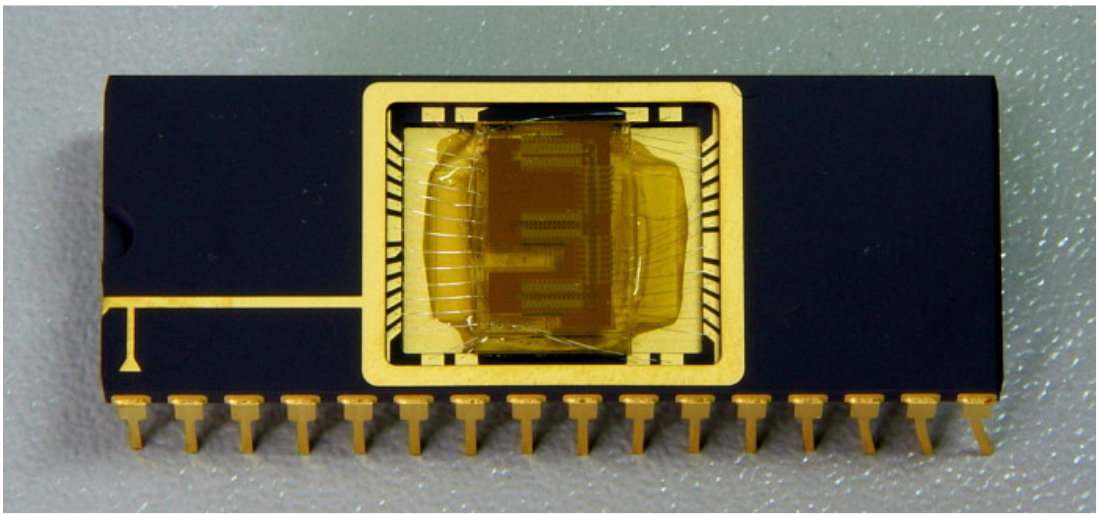
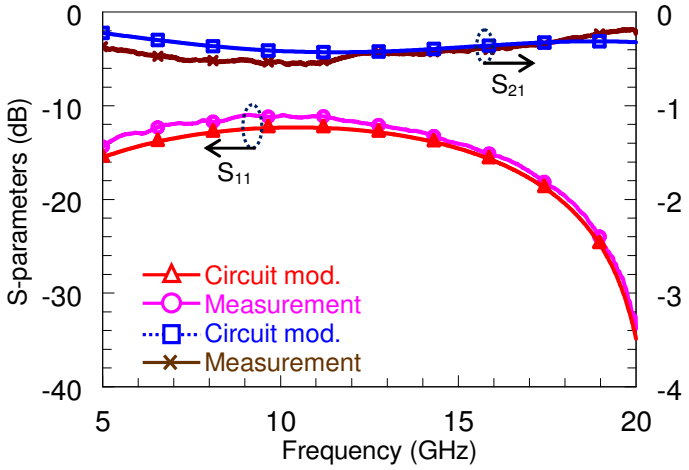


Figure 6.9: The photograph of the packaged RF MEMS VM.

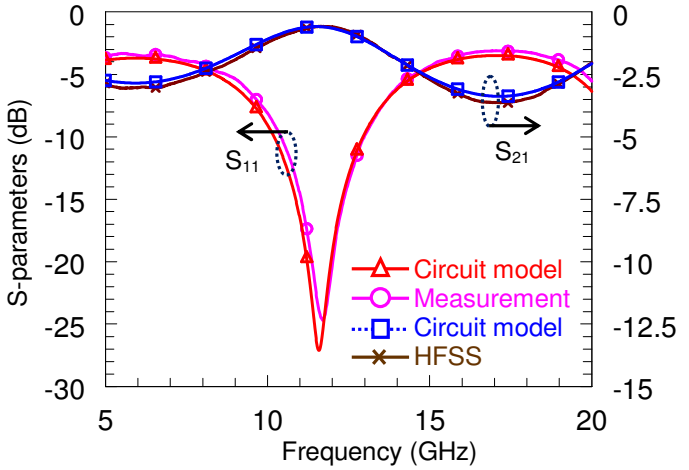
Table 6.4: The circuit model parameters of the DMTL UST-IV that are extracted from the measurements.

	DMTL UST-IV	
	Sim.	**Meas.**
$Z_o\,(\Omega)$	96	96
$\varepsilon_{r,eff}$	2.36	2.43
$\alpha\,(dB/m)$	40 @20 GHz	38 @20 GHz
$f_{Bragg}\,(GHz)$	44	47.5
$s\,(\mu m)$	210	210
$Z_{lu}\,(\Omega)$	43.1	37.4
$Z_{ld}\,(\Omega)$	20.3	21
$\phi_{up}\,(^\circ)$	-12.9	-14.5
$\phi_{down}\,(^\circ)$	-28.3	-27.2
$\Delta\phi$	15.4	12.7
$C_{bu}\,(fF)$	46.9	67.7
$C_{bd}\,(fF)$	469.2	439.8
$C_s\,(fF)$	471.5	363
$L_b\,(pH)$	30	29.79
$R_{bu}/R_{bd}\,(\Omega)$	1.6/0.15	2/0.38
$C_U/C_D\,(fF)$	42.7/235.1	57.1/198.9
Q_U/Q_D	131/99	69/49
$R_{bias}\,(\Omega)$	1665	1215

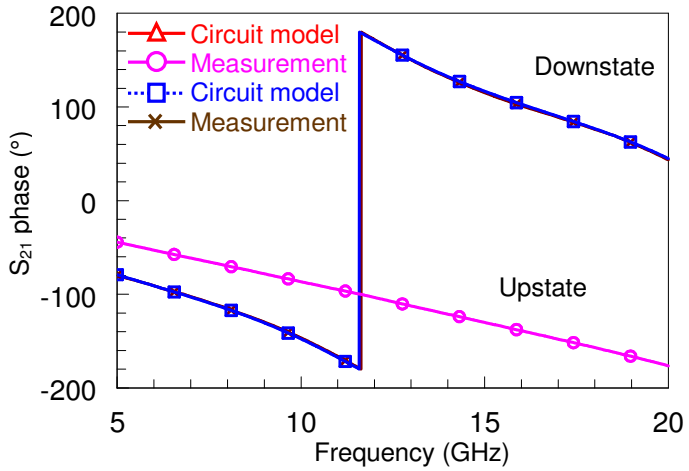
Considering the values given in the table above, most of the extracted values are close to the simulated values. The most import changes are the changes in the upstate capacitance of the MEMS bridge and MAM capacitance, C_{bu} and C_s, and the reasons behind this behavior was explained in detail in Chapter 5.3. The optical surface profiler measurements of the RF MEMS vector modulator is given in Figure 6.11. The figure shows that the bridge height of the MAM capacitances is 1.8 µm, which is the same as that of the MAM capacitances used in the RF MEMS phase shifter.



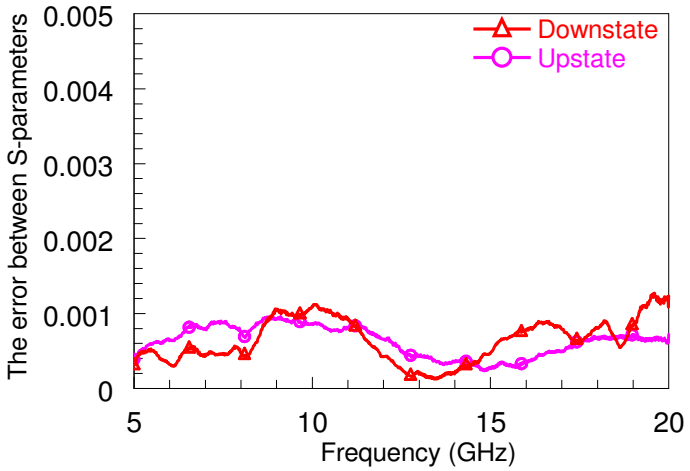
(a) $|S_{11}|$ and $|S_{21}|$ of DMTL UST-IV in upstate (9 unit sections cascaded).



(b) $|S_{11}|$ and $|S_{21}|$ of DMTL UST-IV in downstate (9 unit sections cascaded).



(c) $\angle S_{21}$ of DMTL UST-IV in both states (9 unit sections cascaded).

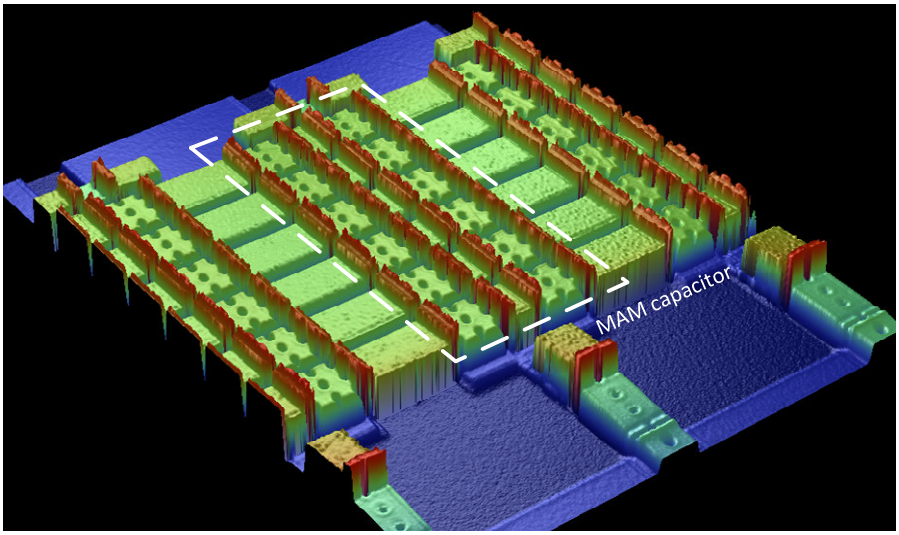


(d) The error between the S-parameters of the circuit model and measurements of DMTL UST-IV for all cases (9 unit sections cascaded).

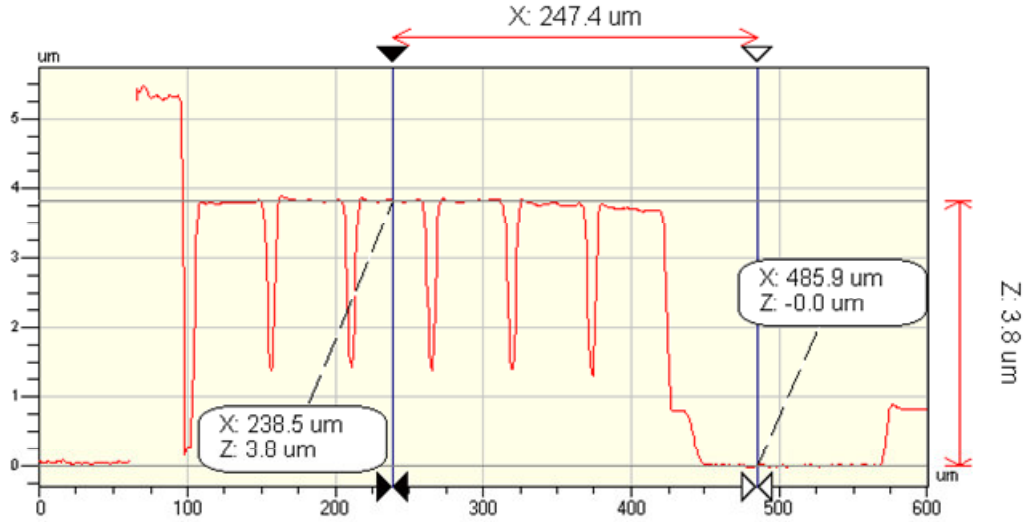
Figure 6.10: The comparison of the measured S-parameters and the circuit model simulations for the 9 cascaded UST-IVs. (a) Magnitudes of the S-parameters in the upstate (b) Magnitudes of the S-parameters in the downstate (c) The phases of the S-parameters for both states (d) The error between the S-parameters of the measurements and the circuit model for both states.

6.3.2. The RF MEMS Vector Modulator Measurements

The RF MEMS vector modulator is measured using SOLT calibration techniques 10-30 GHz frequency band. Since the VM that is used for the SOLT measurements has additional 50 Ω-50 Ω CPW transitions on both sides, the effects of these transitions are also included in the simulations. The multi-pin MEMS automated measurement setup (MAMS), which was explained in Chapter 3, is used for the measurements as the RF MEMS VM has 32 control pins that should be controlled simultaneously. The applied actuation voltage is 20 V bipolar waveform, which is supplied by the waveform generator card.



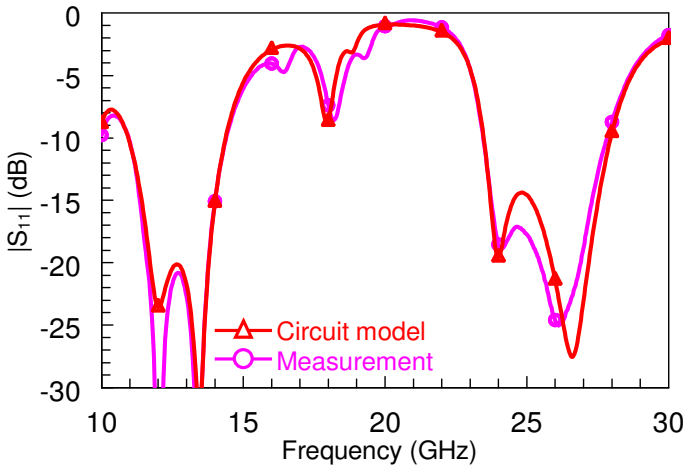
(a) Measured 3D view optical profiler view of the MAM capacitor of the UST-IV.



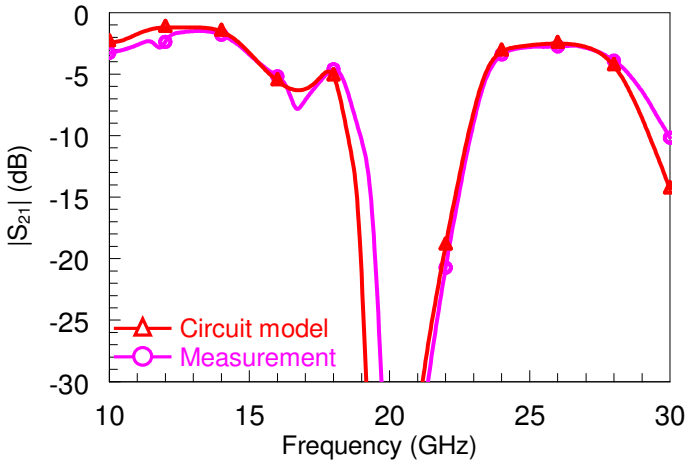
(b) Measured beam height variation of the MAM capacitor of UST-IV.

Figure 6.11: The optical profiler measurements of the fabricated RF MEMS vector modulator.

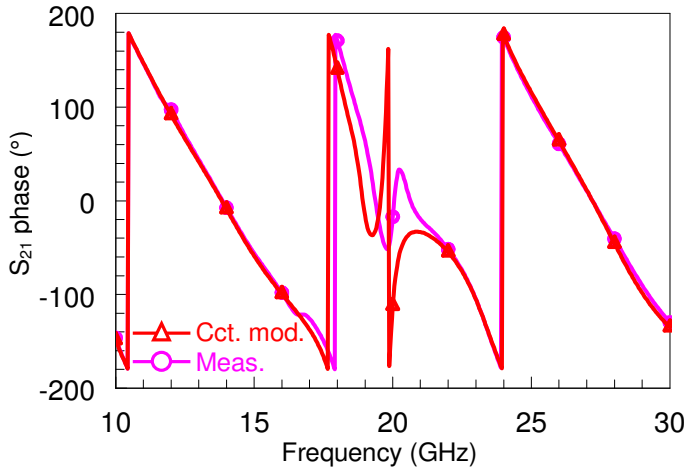
Figure 6.12 shows the upstate measurement of the RF MEMS VM that is measured using SOLT calibration technique. The measurements are in good agreement with the simulations up to the vicinity of 30 GHz, where the measured response starts to deviate from the simulations. The circuit parameters that are used in the simulations are extracted from the measurements of each type of DMTL structures, which were given previously in Table 5.8 and Table 6.4.



(a) $|S_{11}|$ of measured RF MEMS PS compared with the simulations.



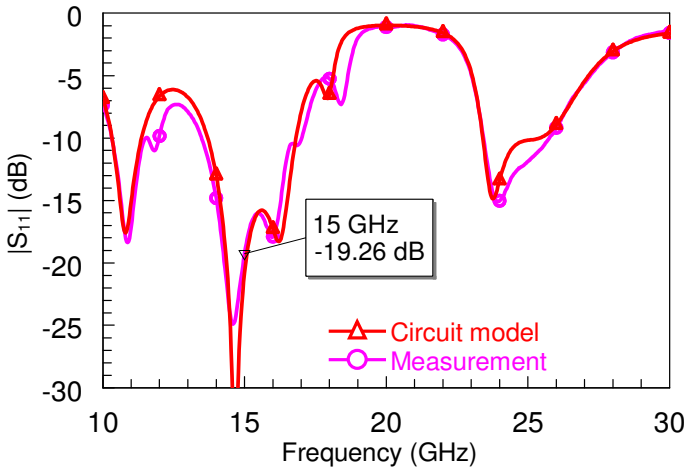
(b) $|S_{21}|$ of measured RF MEMS PS compared with the simulations.



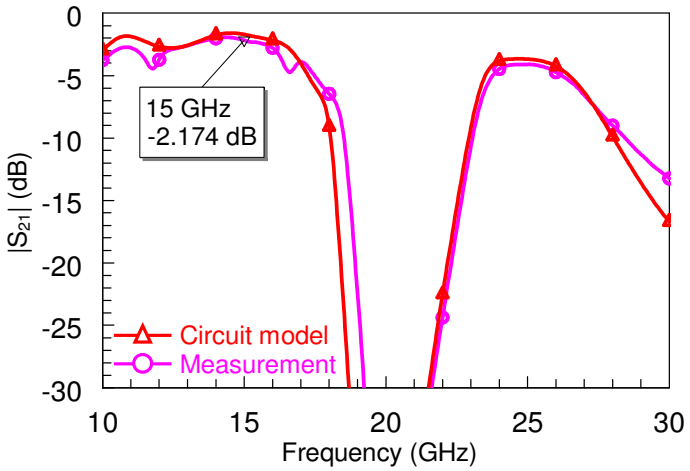
(c) $\angle S_{21}$ of measured RF MEMS PS compared with the simulations.

Figure 6.12: The measured upstate performance of the RF MEMS VM (SOLT calibration used) compared with the simulations (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$.

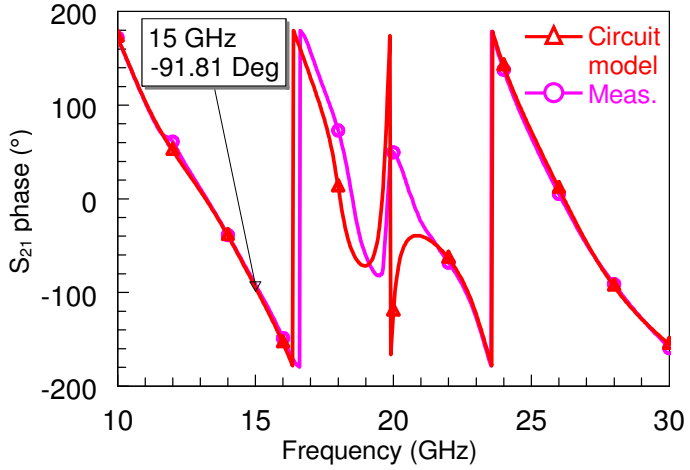
Figure 6.13, Figure 6.14, Figure 6.15, and Figure 6.16 show the measured performance of the VM for some sample insertion phase/amplitude states at 15 GHz, 22.5 GHz, 25 GHz, and 27.5 GHz, respectively. The state numbers of the three stubs and the interconnection line are given in decimal form, and the ones in the binary equivalent of each state number show that those unit sections are in downstate. The figures show that the measurements are in good agreement with the simulations when the VM is reconfigured at the frequencies mentioned above. The phase response is linear around the targeted frequencies for minimum ±1 GHz band. The return losses are better than -11 dB, and they stay in acceptable levels in 1 GHz band around the targeted frequencies. The insertion losses can also be guessed by the simulations by using the resistance values extracted from the specific DMTL measurements. The amplitude response is the bottleneck for the bandwidth of the RF MEMS VM, and the instantaneous bandwidth can go down to 150 MHz around the center reconfiguration frequency for some low amplitude states. However, since the VM is completely reconfigurable, the frequency of operation can be easily tuned to the desired value so that the center of the instantaneous bandwidth is centered to the frequency of operation.



(a) $|S_{11}|$ of measured RF MEMS PS compared with the simulations.

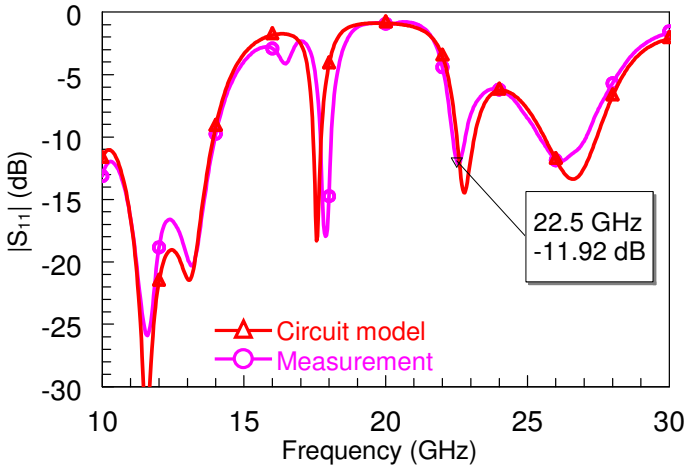


(b) $|S_{21}|$ of measured RF MEMS PS compared with the simulations.

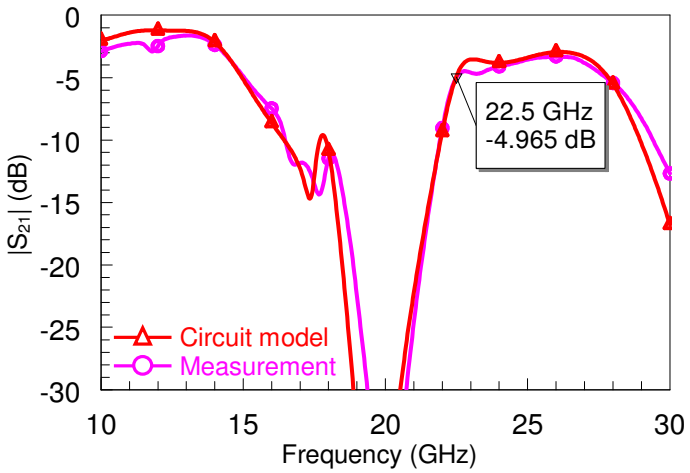


(c) $\angle S_{21}$ of measured RF MEMS PS compared with the simulations.

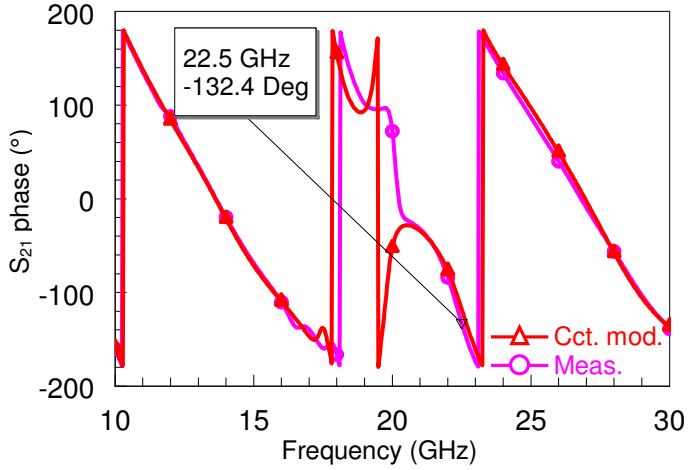
Figure 6.13: The measured performance of the RF MEMS VM (SOLT calibration used) that is reconfigured to (-2 dB, -90°) @ 15 GHz compared with the simulations (Stb1 = 0, Stb2 = 0, Stb3 = 0, IntLine = 8) (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$.



(a) $|S_{11}|$ of measured RF MEMS PS compared with the simulations.

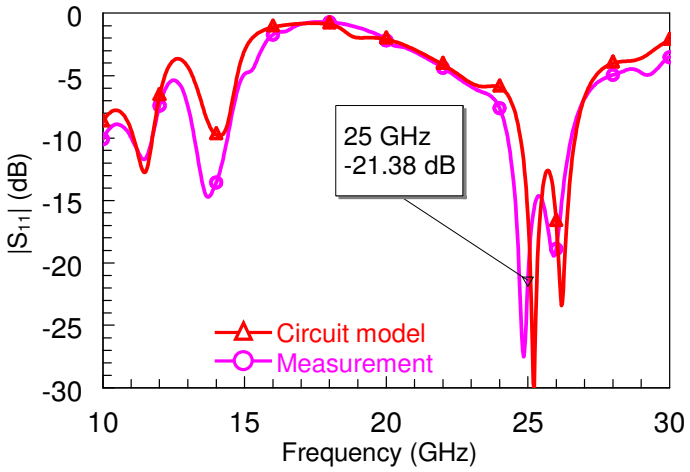


(b) $|S_{21}|$ of measured RF MEMS PS compared with the simulations.

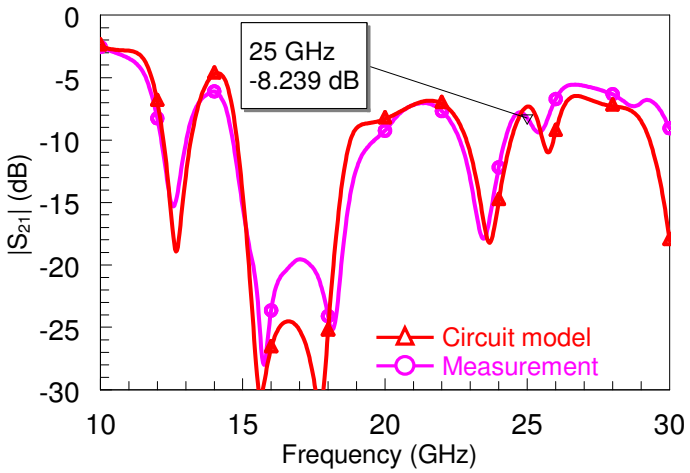


(c) $\angle S_{21}$ of measured RF MEMS PS compared with the simulations.

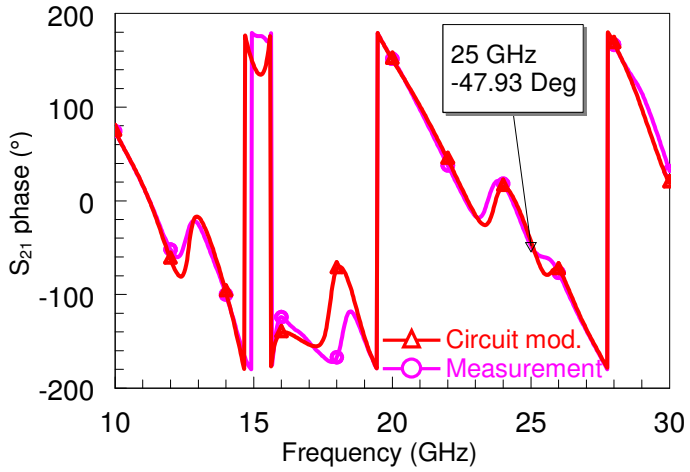
Figure 6.14: The measured performance of the RF MEMS VM (SOLT calibration used) that is reconfigured to (-5 dB, -135°) @ 22.5 GHz compared with the simulations (Stb1 = 32, Stb2 = 1, Stb3 = 0, IntLine = 0) (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$.



(a) $|S_{11}|$ of measured RF MEMS PS compared with the simulations.

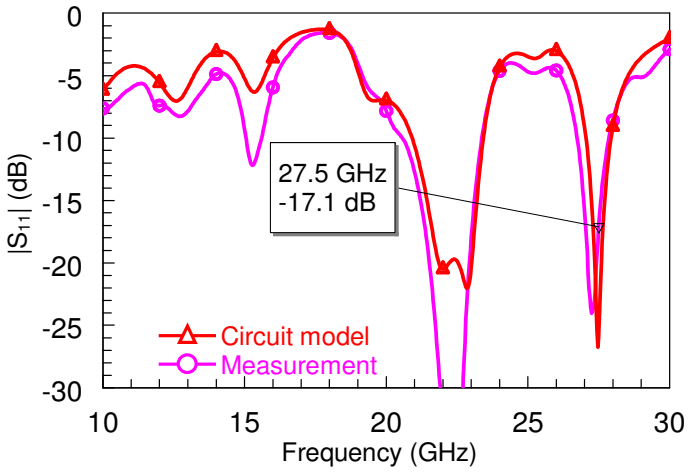


(b) $|S_{21}|$ of measured RF MEMS PS compared with the simulations.

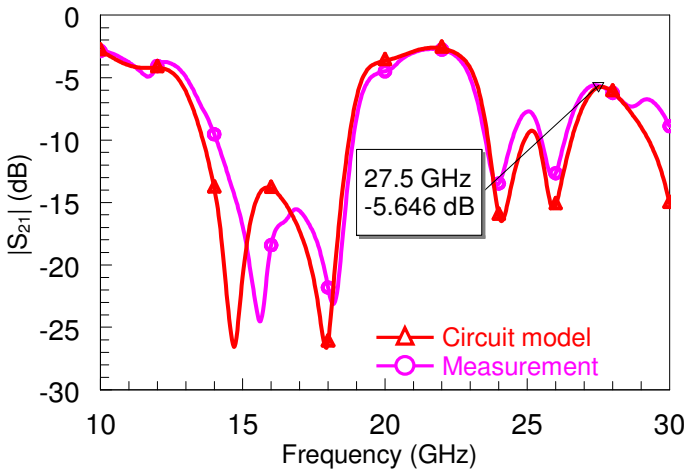


(c) $\angle S_{21}$ of measured RF MEMS PS compared with the simulations.

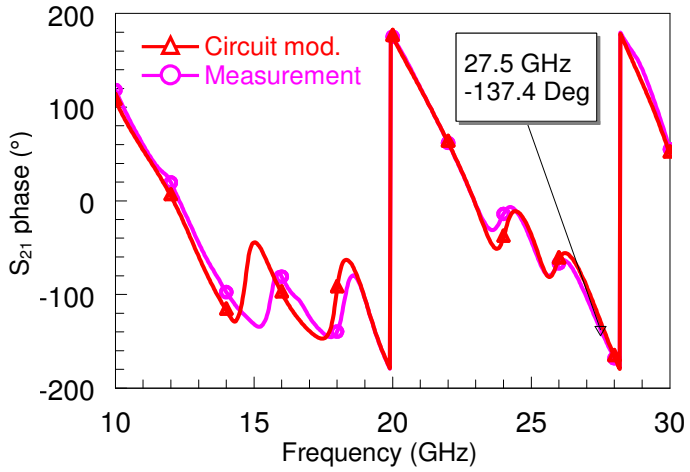
Figure 6.15: The measured performance of the RF MEMS VM (SOLT calibration used) that is reconfigured to (-8 dB, -45°) @ 25 GHz compared with the simulations (Stb1 = 192, Stb2 = 463, Stb3 = 59, IntLine = 24) (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$.



(a) $|S_{11}|$ of measured RF MEMS PS compared with the simulations.



(b) $|S_{21}|$ of measured RF MEMS PS compared with the simulations.



(c) $\angle S_{21}$ of measured RF MEMS PS compared with the simulations.

Figure 6.16: The measured performance of the RF MEMS VM (SOLT calibration used) that is reconfigured to (-6 dB, -135°) @ 27.5 GHz compared with the simulations (Stb1 = 2, Stb2 = 119, Stb3 = 401, IntLine = 18) (a) $|S_{11}|$ (b) $|S_{21}|$ (c) $\angle S_{21}$.

Table 6.5: The summary of measured performance of the RF MEMS VM.

	Amplitude States	Avr. / Std. Dev.	S_{11}	S_{21}		Amp. Error	Amp. Error	Phase Error
			dB	dB	Lin	dB	Lin	(°)
22.5 GHz	State Set 1	Avr.	-18.69	-3.10	0.70	0.70	0.06	4.03
	-3.10 dB / 45° steps	Std. Dev.	9.87	0.91	0.07	0.52	0.04	5.56
	State Set 2	Avr.	-16.36	-5.17	0.55	0.16	0.01	2.92
	-5.19 dB / 45° steps	Std. Dev.	7.26	0.21	0.01	0.11	0.01	4.39
	State Set 3	Avr.	-13.53	-7.56	0.42	0.71	0.03	4.94
	-7.96 dB / 45° steps	Std. Dev.	6.41	0.84	0.04	0.55	0.03	4.16
	Overall 24 states	Avr.	-16.19	-5.27	0.56	0.52	0.03	3.96
		Std. Dev.	7.93	1.99	0.13	0.50	0.03	4.61
25 GHz	State Set 1	Avr.	-20.37	-3.45	0.67	0.52	0.04	3.24
	-3.10 dB / 45° steps	Std. Dev.	5.67	0.73	0.05	0.61	0.04	3.62
	State Set 2	Avr.	-18.14	-5.17	0.55	0.18	0.01	3.83
	-5.19 dB / 45° steps	Std. Dev.	6.19	0.23	0.01	0.12	0.01	3.54
	State Set 3	Avr.	-17.18	-7.71	0.41	0.54	0.03	5.00
	-7.96 dB / 45° steps	Std. Dev.	5.04	0.65	0.03	0.40	0.02	3.91
	Overall 24 states	Avr.	-18.56	-5.44	0.55	0.41	0.03	4.02
		Std. Dev.	5.57	1.87	0.11	0.44	0.03	3.61
27.5 GHz	State Set 1	Avr.	-16.87	-3.90	0.64	0.35	0.03	4.69
	-3.74 dB / 45° steps	Std. Dev.	5.99	0.52	0.04	0.39	0.03	4.51
	State Set 2	Avr.	-16.44	-6.06	0.50	0.31	0.02	3.17
	-6.02 dB / 45° steps	Std. Dev.	2.96	0.35	0.02	0.11	0.01	2.29
	State Set 3	Avr.	-12.26	-9.09	0.35	0.57	0.02	2.79
	-9.12 dB / 45° steps	Std. Dev.	4.90	0.68	0.03	0.31	0.01	2.61
	Overall 24 states	Avr.	-15.19	-6.35	0.50	0.41	0.02	3.55
		Std. Dev.	5.04	2.23	0.12	0.31	0.02	3.25

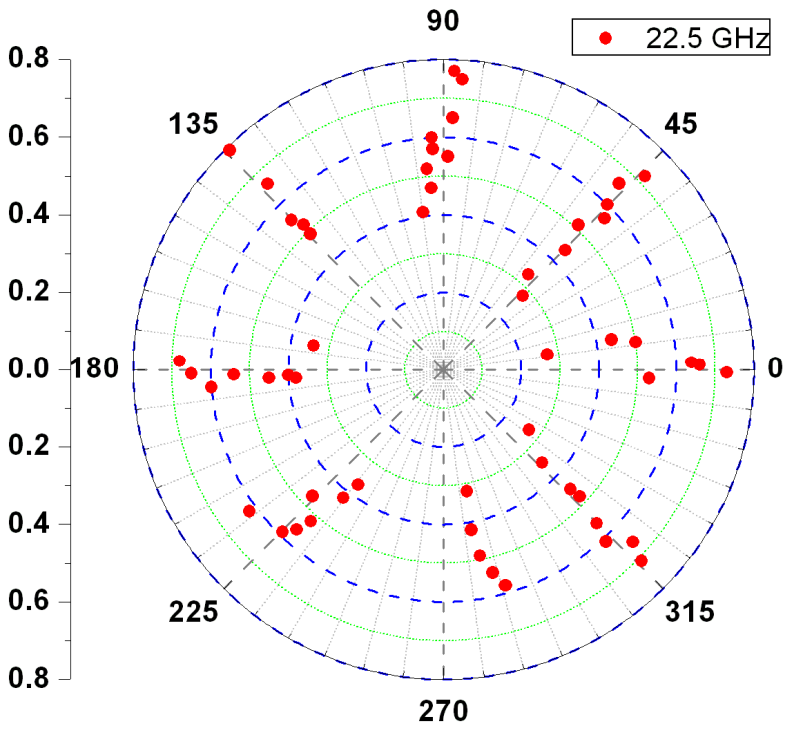
Table 6.5 shows the summary of the measured data for RF MEMS VM for 22.5 GHz, 25 GHz, and 27.5 GHz frequencies. The RF MEMS VM is reconfigured to 8 insertion phase states for each of the tabulated 3 amplitude states, which make a total of 24 states at each frequency, to demonstrate the wide operation frequency range of the RF MEMS VM. The insertion phase states are apart by 45°. The targeted amplitude states have $|S_{21}|$ values of 0.7, 0.55, and 0.4 for 22.5 GHz and 25 GHz, and 0.65, 0.5, and 0.35 for 27.5 GHz. The dB equivalents of the states are given in the table. *The average phase errors among the measured 24 states are 3.96°, 4.02°, and 3.55° for 22.5 GHz, 25 GHz, and 27.5 GHz frequencies, respectively. The average amplitude errors are 0.52 dB, 0.41 dB, and 0.41 dB for 22.5 GHz, 25 GHz, and 27.5 GHz frequencies, respectively. The average return losses of the measured*

24 states are -16.2 dB, -18.6 dB, and -15.2 dB for 22.5 GHz, 25 GHz, and 27.5 GHz frequencies, respectively. The standard deviations of all the mentioned measurements are also given in Table 6.5.

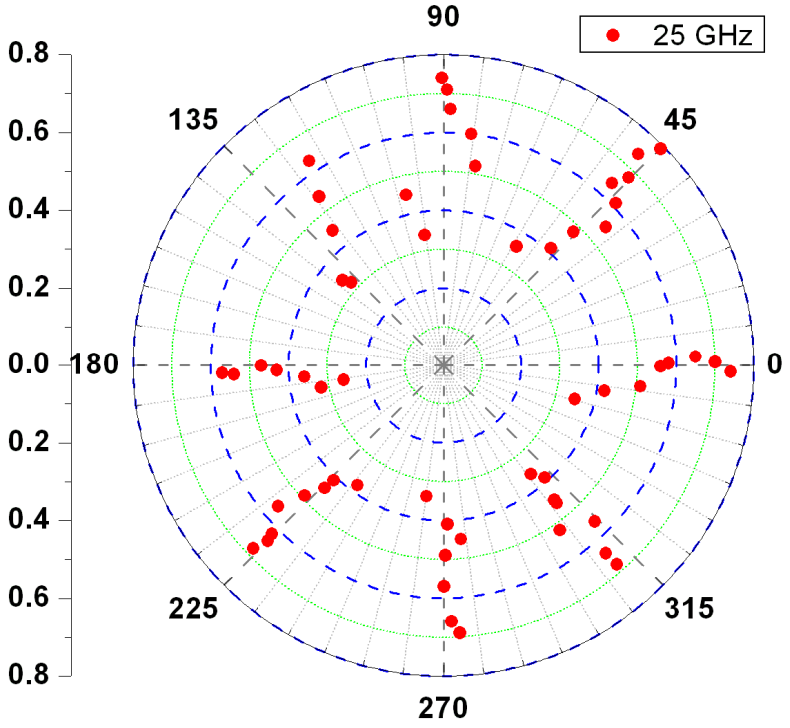
Figure 6.17 shows the measurement results of the VM for 22.5 GHz, 25 GHz, and 27.5 GHz frequencies. The graphs show samples of insertion phase/amplitude states that can be covered at those frequencies. The graphs also include the selected 24 states, the data of which were given in Table 6.5. The measurement results in the graphs show that the design and the fabrication are both successful, and RF MEMS VM can provide 24 insertion phase/amplitude states between 22.5 GHz and 27.5 GHz.

It should be emphasized once more here that the 45° phase resolution and the -2 dB amplitude resolution are targeted for proof of concept purposes, and the performance is definitely not limited to these values. The figures clearly demonstrate that it is easily possible to have insertion phase steps with lower than 10° phase and 1 dB amplitude resolutions with average errors less than 5° and 0.5 dB, respectively. The author believes that the RF MEMS VM can be reconfigured to any frequency between 22.5 and 27.5 GHz frequencies.

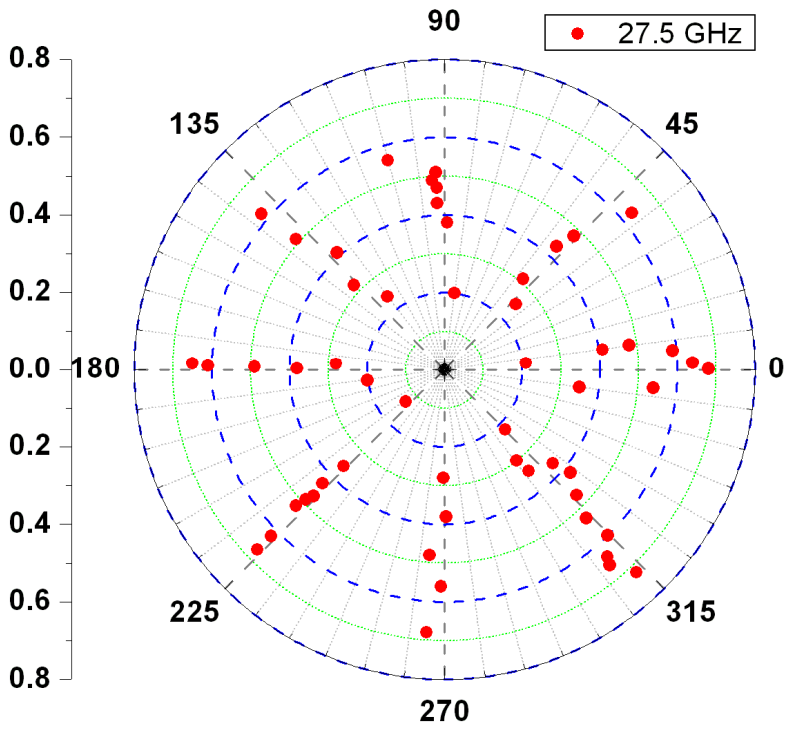
The measurements that are reconfigured at 15 GHz are not given here since the performance is seriously affected from the change in the capacitance values, especially the increase in C_{bu}. The reason behind this behavior is the decrease in the electrical lengths of the stubs and the interconnection line. The range of the interconnection line is severely reduced, which is critical for the proper operation of the VM. The discussion about the changes in the capacitances in the circuit model was discussed earlier in Chapter 5.3, and it will be not repeated here.



(a) 22.5 GHz.



(b) 25 GHz.



(c) 27.5 GHz.

Figure 6.17: The measured S_{21} performance of the RF MEMS VM (SOLT calibration used) for some sets of sample phase/amplitude pairs (a) 22.5 GHz (b) 25 GHz (c) 27.5 GHz.

The insertion loss performance of the RF MEMS VM is measured higher than the initial simulations results, which was expected from the experience obtained from the RF MEMS PS measurements. The initial design amplitude levels were -2 dB, -4.5 dB, and -8 dB where the targeted values are -3.1 dB, -5.2 dB, and -8 dB. The reasons of the increasing insertion losses were explained in Chapter 5 in detail. It is interesting to note here that even at 22.5 GHz, which is 1.5 times the initial design center frequency, there exist some states with about -2 dB insertion loss. This is because -2 dB is not maximum amplitude that the initial design could provide. The -2 dB level was selected to obtain the targeted amplitude value at each phase states so that the amplitude error remains small.

Another observation is that the instantaneous bandwidth is larger than that of the initial design, especially for the lower amplitude states. This is due to the fact that to obtain low amplitude levels with the presence of low insertion losses, the VM

circuit has to operate in the vicinity of the resonance points where the amplitude response changes very rapidly. However, as the insertion losses increase both due to the differences between the simulated and the measured response and due to the increasing frequency, the quality factor of the resonating VM circuit decreases. This results with peak points with less sharpness around the resonance point. Hence, the amplitude response of the circuit changes more slowly, which means a larger instantaneous bandwidth.

6.4. Conclusion

In this chapter, the design, the fabrication, and the measurement results of the RF MEMS vector modulator that is based on the triple stub topology are presented. The measurement results show good agreement with the simulations in 15 GHz to 30 GHz frequency range. The VM has good phase error, amplitude error, and return loss performance at the range starting from 22.5 GHz up to 27.5 GHz. The wideband operation and the performance within this frequency range show that the RF MEMS VM is completely reconfigurable. However, the VM performance is severely affected from the changes in the MEMS bridge heights, and the performance is limited to only some specific states at the center design frequency of 15 GHz. In any case, the proof of concept of RF MEMS VM is demonstrated; in addition to that, the fabricated VM is ready to use in the 22.5 GHz-27.5 GHz frequency range.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

This thesis presented the theory, the design, and the implementation of novel reconfigurable RF MEMS circuits that are based on triple stub topology. These circuits include an impedance tuner, a phase shifter, and a vector modulator. The RF MEMS circuits are fabricated using in-house METU RF MEMS Fabrication Process, and the measurements of all of the circuits are accomplished successfully.

The fabricated RF MEMS impedance tuner is measured for 729 out of 1331 impedance points, and the measurements are in agreement with the simulations. It is demonstrated that the tuner covers the most of the Smith Chart area in 6-20 GHz band, especially between 10 GHz and 20 GHz, when the 10 dB impedance mismatch level is considered. The insertion loss of the tuner is measured to be -3.3 dB at both 10 GHz and 20 GHz. The tuner is also capable of covering the Smith Chart with 2^{30} impedance points when more than one switch is actuated at once on each stub.

The performance of the fabricated RF MEMS phase shifter is investigated between 15 GHz and 40 GHz. The measurement results show that the phase shifter can cover 160-360° insertion phase range with 10° resolution with an average phase error of 1.7° at 15 GHz. The average insertion loss and the average return loss is measured to be -3.1 dB and -19.3 dB, respectively. It is also showed that the designed phase shifter can work up to 40 GHz with a insertion phase range about 300° starting from 22.5 GHz. The price paid is the gradually increasing insertion loss.

The performance of the fabricated RF MEMS vector modulator is examined in 10-30 GHz band. The vector modulator performance is demonstrated between 22.5 GHz and 27.5 GHz. The vector modulator is reconfigured to 8 phase states for each of the 3 amplitude states, which make a total of 24 states at each frequency. The phase state separation in 45°, and the targeted amplitude states have $|S_{21}|$ values of 0.7, 0.55, and 0.4 for 22.5 GHz and 25 GHz, and 0.65, 0.5, and 0.35 for 27.5 GHz. The average phase errors among the measured 24 states are 3.96°, 4.02°, and 3.55° for 22.5 GHz, 25 GHz, and 27.5 GHz frequencies, respectively. The average amplitude errors are 0.52 dB, 0.41 dB, and 0.41 dB again for 22.5 GHz, 25 GHz, and 27.5 GHz frequencies, respectively.

Considering the measurement results that are summarized above, the following conclusions can be deduced:

- METU RF MEMS Fabrication Process is used successfully to implement complicated RF MEMS structures, which include a high number of RF MEMS components in a small wafer area. Significant increase is observed in the performance of the fabricated structures by the change of the substrate, the improvement of the first metal layer, and the improvement of the structural layer.

- The RF MEMS impedance tuner that has wide impedance coverage is implemented successfully in a very wide band with advantages brought by RF MEMS technology. The multi-pin MEMS automated measurement setup, which enables the measurement and characterization of RF MEMS structures with a high number of control pins, is developed for the measurements. The number of measured impedance points is the highest reported in the literature, which allows a complete characterization of the design.

- The theory of the triple stub topology is investigated in detail. It has been shown both analytically and experimentally that this topology is capable of providing insertion phase and amplitude control of the input signal simultaneously using only low-loss transmission lines. The mechanism of obtaining high insertion losses without any reflection is explained. It is also illustrated that maximum power transfer is possible to the transmission line-based resonators by means of direct connection instead of capacitive coupling.

- A wide band, reconfigurable RF MEMS phase shifter is demonstrated using the results extracted from the theory of triple stub topology. It is shown that the insertion phase can be controlled in a quasi-continuous manner by the presented RF MEMS phase shifter.

- A wide band, reconfigurable RF MEMS vector modulator is presented, which is again based on the results of the theory of triple stub topology. It is shown that the insertion phase can be controlled simultaneously with the amplitude in a quasi-continuous manner by using only low-loss distributed structures with the presented RF MEMS vector modulator.

Although the targets of this thesis are achieved successfully, there is always room for improvements. The following items can be investigated as future work:

- The fabrication of the entire RF MEMS designs can be fabricated again with a thinner first metal layer only in the areas underneath the MEMS bridges. This will prevent the formation of weak boundaries on the bridge, which will cease the buckling of the structures. A study has just been completed by METU RF MEMS Group, in which it is shown that the buckling is prevented with this method. Having MEMS bridge without any buckling will result with better agreement with the predicted performance, and the insertion losses

are expected to decrease. Using a high-quality gold electroplating solution, which can provide a gold layer with higher conductivity, will also decrease the losses.

- The multi-pin MEMS automated measurement setup (MAMS) should be redesigned for application specific integrated circuit (ASIC) fabrication. Then, the RF MEMS structures and the setup should be placed in a hybrid package.

- The presented RF MEMS triple stub impedance tuner should be used for the implementation of real-time, autonomous impedance matching of an unknown load. The current MAMS needs a few hundred milliseconds to switch the tuner to a desired state. If the MAMS is redesigned as an ASIC as explained above, the interstate switching time will be reduced. In this case, computer or microcontroller based algorithm can be employed in order to obtain impedance matching of an unknown load. The presented RF MEMS impedance tuner allows this as the RF MEMS switches are placed uniformly on all of the stubs.

- The SiCr bias lines in the RF MEMS phase shifter and RF MEMS vector modulator should be redesigned, and the CPW ground penetrations should be avoided as much as possible. The modified designs with such bias lines are expected to have much lower insertion loss.

- The RF MEMS phase shifter and vector modulator should be investigated whether a predefined operation, for example a 4-bit phase shifter or a two amplitude state vector modulator, can be provided with less number of pins. In the current designs, the provided phase and amplitude ranges are covered in a continuous manner, so the present number of pins is necessary.

- The other alternative topologies for vector modulator, which are also based on the triple stub topology, should be implemented. The bandwidth of the simultaneous insertion phase/amplitude control is expected to increase significantly with these structures.

- The theory of triple stub topology should be investigated in more detail for the lossy case. Alternative analytical and graphical methods should be investigated for the exact solution of this problem.

- It has been shown that the set of switch states that are obtained from the optimization for a given insertion phase/amplitude can give better performance for RF MEMS phase shifter and vector modulator. An optimization method should be developed in order to find the best solution fast from the whole solution space, which currently includes 2^{32} states.

- The RF MEMS phase shifter or the RF MEMS vector modulator can be employed in adaptive millimeterwave phase arrays. However, these structures should be redesigned with a reduced number of controls as mentioned above.

- The lifetime of the RF MEMS switches should be investigated, and a packaging solution should be proposed for the RF MEMS structures presented in this thesis. These problems are not expected to prevent the application of these circuits; however, they should be addressed carefully, and the limits should be determined before the application. Dedicated works that address both of these issues are currently investigated by METU RF MEMS Group.

Considering the summarized achievements of this thesis, it is shown that RF MEMS in an enabling technology, and it is possible to design and implement novel structures using this technology. The successful implementation of the above mentioned circuits shows that METU RF MEMS Fabrication Process, which is the only example of its kind in Türkiye, is mature. Using this fabrication process, it is possible to implement RF MEMS structures reliably and repeatedly. This result is very important in the sense that this is a national technology, and it should be used in the implementation of high performance defense applications.

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APPENDIX

DETAILED FABRICATION PROCESS FLOW

This appendix presents the detailed fabrication flow of the METU RF MEMS Fabrication process. The entire fabrication process is done at the fabrication facilities of the METU MEMS center on 4" quartz substrate.

STEP NO	PROCESS	SPECIFICATION
1	**WAFER CLEANING**	1. Soak in piranha solution (H_2SO_4:H_2O_2 1:1.2), Duration: 2×15 min. 2. DI-water rinse (min. 3×10 min cycles in automated rinser). 3. Dry by N_2.
2	**SURFACE FORMATION**	1. Soak in BHF, Duration: 30 s. 2. DI-water rinse (min. 3×30 s cycles in automated rinser). 3. Dry by N_2.
3	**SiCr SPUTTERING** Resistive layer deposition	Dehydration, N_2, 110°C, 30 min. Power: 100 W, Rate: 0.05/0.1 Å/s. Pressure: 10×10^{-3} mBar, Flow: 12.6 sccm Ar. Temperature: 120 °C, Distance: 130 mm. Time: 4000 s, Endpoint: 200 Å. Measured thickness: 1000 Å.
4	**LITHOGRAPHY** MASK #1 for **SiCr Etch**	1. Dehydration, N_2, 110°C, 10 min. 2. Spin Primer (HMDS), 500 rpm 7 sec. + 4000 rpm 30 sec. 3. Spin S1813 PR, 500 rpm 7 sec. + 4000 rpm, 30 sec. 4. Softbake 115°C, 70 s, hotplate. 5. EBR @ 2000 rpm. 6. Align & Expose, 4.2 sec @ 13 mW/cm^2 (Constant intensity). 7. Develop, MF-319, 60 s. 8. DI-water rinse, 1:30 min + 1:30 min. 9. Dry by N_2. 10. Inspect alignment marks. 11. Hardbake @ 110°C, 10 min, N_2, oven. 12. O_2 plasma @ 300 W, 0.4 Torr, 30 s.
5	**SiCr ETCH** Resistive layer patterning	1. Etch in BHF, (Duration depends on the layer, ~3-6 min). 2. DI-water rinse (min. 3×30 s cycles in automated rinser). 3. Dry by N_2

		4. Inspection (Check the metals on the anchors)
6	**PHOTORESIST STRIP**	1. Soak in ACE (10 min) or wash the wafer with ACE. 2. Soak in IPA (5 min) or wash the wafer with IPA. 3. Soak in SVC-175 baths @ 80°C, Duration: 2×10 min. 4. DI-water rinse (min. 5×10 min cycles in automated rinser). 5. Dry by N_2. 6. Inspection.
7a	**Ti SPUTTERING** First metal layer deposition	Dehydration, N_2, 110°C, 30 min. Power: 300 W, Rate: 1.1 Å/s. Pressure: 2×10^{-3} mBar, Flow: 2.1 sccm Ar. Temperature: 150 °C, Distance: 130 mm. Time: 75 s, Endpoint: 80 Å. Measured thickness: 200 Å.
7b	**Au SPUTTERING** First metal layer deposition	Power: 100 W, Rate: 1.1 Å/s. Pressure: 20×10^{-3} mBar, Flow: 25 sccm Ar. Temperature: 150 °C, Distance: 130 mm. Time: 2000 s, Endpoint: 2500 Å. Measured thickness: 9000 Å.
8	**LITHOGRAPHY** MASK #2 for **Ti/Au Etch**	1. Dehydration, N_2, 110°C, 10 min. 2. Spin Primer(HMDS), 500 rpm 7 sec. + 4000 rpm 30 sec. 3. Spin SPR220-3 PR, 500 rpm 7 sec. + 4000 rpm, 30 sec. 4. Softbake 115°C, 90 s, hotplate. 5. EBR @ 2000 rpm. 6. Align & Expose, 12.5 sec @ 13 mW/cm^2 (Constant intensity). 7. Develop, MF-24A, 90 s. 8. DI-water rinse, 1:30 min + 1:30 min. 9. Dry by N_2. 10. Inspect alignment marks. 11. Hardbake @ 110°C, 10 min, N_2, oven. 12. O_2 plasma @ 300 W, 0.4 Torr, 30 s.
9a	**Au ETCH** First metal layer patterning	1. Etch in Au Etchant, Duration: ~2 min. 2. DI-water rinse (min. 3×30 s cycles in automated rinser). 3. Dry by N_2. 4. Inspection.
9b	**Ti ETCH** First metal layer patterning	1. Etch in Ti Etchant ($HF:H_2O_2$:DI 1:1:640), Duration: ~1 min. 2. DI-water rinse (min. 3×30 s cycles in automated rinser). 3. Dry by N_2. 4. Inspection.
10	**PHOTORESIST STRIP**	1. Soak in ACE (10 min) or wash the wafer with ACE. 2. Soak in IPA (5 min) or wash the wafer with IPA. 3. Soak in SVC-175 baths @ 80°C, Duration: 2×10 min. 4. DI-water rinse (min. 5×10 min cycles in automated rinser). 5. Dry by N_2. 6. Inspection.
11a	**Ti SPUTTERING** Backside metal deposition	Dehydration, N_2, 110°C, 30 min. Power: 300 W, Rate: 1.1 Å/s. Pressure: 2×10^{-3} mBar, Flow: 2.1 sccm Ar. Temperature: RT, Distance: 130 mm. Time: 75 s, Endpoint: 80 Å.

		Measured thickness: 200 Å.
11b	**Au SPUTTERING** Backside metal deposition	Power: 300 W, Rate: 4 Å/s. Pressure: 20×10^{-3} mBar, Flow: 25 sccm Ar. Temperature: 150 °C, Distance: 130 mm. Time: 150 s, Endpoint: 600 Å. Measured thickness: 2000 Å.
12	**PECVD SiN DEPOSITION**	Dehydration, N_2, 120°C 30 min. MF, stress free recipe @ 300 °C, Duration: 23 min. Meas. thickness: 2900 Å
13	**LITHOGRAPHY** MASK #3 for **SiN RIE**	1. Dehydration, N_2, 110°C, 10 min. 2. Spin Primer(HMDS), 500 rpm 7 sec. + 4000 rpm 30 sec. 3. Spin SPR220-3 PR, 500 rpm 12.5 sec. + 4000 rpm, 30 sec. 4. Softbake 115°C, 90 s, hotplate. 5. EBR @ 2000 rpm. 6. Align & Expose, 12.5 sec @ 13 mW/cm^2 (Constant intensity). 7. Develop, MF-24A, 90 s. 8. DI-water rinse, 1:30 min + 1:30 min. 9. Dry by N_2. 10. Inspect alignment marks. 11. Hardbake @ 110°C, 10 min, N_2, oven. 12. O_2 plasma @ 300 W, 0.4 Torr, 30 s.
14	**SiN RIE** Isolation layer patterning	Pressure: 70 mTorr, Power: 250 W. Flow: 60 sccm CF_4, 22 sccm CHF_3, 10 sccm O_2. Recipe: 1_SiN, Duration: 60 s.
15	**PHOTORESIST STRIP**	1. Soak in ACE (10 min) or wash the wafer with ACE (Mandatory). 2. Soak in IPA (5 min) or wash the wafer with IPA (Mandatory). 3. Soak in SVC-175 baths @ 80°C, Duration: 2×10 min. 4. DI-water rinse (min. 5×10 min cycles in automated rinser). 5. Dry by N_2. 6. Inspection.
16	**LITHOGRAPHY** MASK #4 for **Sacrificial Layer Formation**	1. Dehydration, N_2, 110°C, 10 min. 2. Spin PI2737 polyimide, 500 rpm 7 sec. + 4500 rpm, 30 sec. 3. Softbake 75°C, 4:30 min hotplate. 4. Align & Expose, 20 sec @ 13 mW/cm^2 (Constant intensity). 5. Develop in DE9040, 2:30 min. 6. Rinse in PA401R, 30 s. 7. Dry by N_2. 8. Inspect alignment marks. 9. Skip O_2 plasma. 10. Curing: Ramp 50-to-220 °C, hold @ 220°C for 115 min, Cool down to 50° C in 20 min.
17	**Au SPUTTERING** Structural metal layer deposition	Dehydration, N_2, 110°C, 10 min. Power: 213 W, Rate: 2.7 Å/s. Pressure: 10×10^{-3} mBar, Flow: 22 sccm Ar. Temperature: RT, Distance: 130 mm. Time: 4×300 s, Endpoint: 4000 Å. Measured thickness: 11000 Å.
18	**LITHOGRAPHY** MASK #5 for **Anchor Fill**	1. Dehydration, N_2, 110°C, 10 min. 2. Spin Primer(HMDS), 500 rpm 7 sec. + 2000 rpm 30 sec.

	Electroplating	3. Spin SPR220-7 PR, 500 rpm 7 sec. + 2000 rpm, 30 sec. 4. Softbake 115°C, 90 s, hotplate. 5. EBR @ 2000 rpm. 6. Align & Expose, 55 sec @ 13 mW/cm^2 (Constant intensity). 7. Develop, MF-24A, 2 min. 8. DI-water rinse, 1:30 min + 1:30 min. 9. Dry by N_2. 10. Inspect alignment marks. 11. Hardbake @ 110°C, 10 min, N_2, oven. 12. O_2 plasma @ 300 W, 0.4 Torr, 30 s.
19	**Au ELECTROPLATING** Strengthening layer selective deposition	Average current: 6 mA DC, Plating area: 2.53 cm^2. Duty cycle: 2 ms ON/98 ms OFF. Pump: ON, Reciprocator: OFF, Temperature: 32 °C. Duration: 20 min.
20	**PHOTORESIST STRIP**	1. Soak in ACE (10 min) or wash the wafer with ACE. 2. Soak in IPA (5 min) or wash the wafer with IPA. 3. DI-water rinse (min. 3×10 min cycles in automated rinser). 4. Dry by N_2. 5. Inspection.
21	**LITHOGRAPHY** MASK #6 for **Structural Layer Etch**	1. Dehydration, N_2, 110°C, 10 min. 2. Spin Primer(HMDS), 500 rpm 7 sec. + 2000 rpm 30 sec. 3. Spin SPR220-7 PR, 500 rpm 7 sec. + 2000 rpm, 30 sec. 4. Softbake 115°C, 90 s, hotplate. 5. EBR @ 2000 rpm. 6. Align & Expose, 55 sec @ 13 mW/cm^2 (Constant intensity). 7. Develop, MF-24A, 2 min. 8. DI-water rinse, 1:30 min + 1:30 min. 9. Dry by N_2. 10. Inspect alignment marks. 11. Hardbake @ 110°C, 10 min, N_2, oven. 12. O_2 plasma @ 300 W, 0.4 Torr, 30 s.
22	**Au ETCH** Structural layer patterning	1. Etch in Au Etchant, Duration: ~2:30 min. 2. DI-water rinse (min. 3×30 s cycles in automated rinser). 3. Dry by N_2. 4. Inspection.
23	**Ti ETCH** Backside metal stripping	1. Etch in Ti Etchant ($HF:H_2O_2$:DI 1:1:640), Duration: ~1 min. 2. DI-water rinse (min. 3×30 s cycles in automated rinser). 3. Dry by N_2. 4. Inspection.
24	**DICING**	Separating the samples by dicing.
25	**SACRIFICAL LAYER ETCH**	1. Sacrificial layer wet etching in EKC-265 @ 50 °C Stirrer @ 250 rpm, Duration: 16 h. 2. DI-water rinse (min. 2×30 min). 3. IPA rinse (min. 2×15 min).
26	**CRITICAL POINT DRYING**	1. Release the structures using critical point drying. 2. Inspection both by optical microscope and optical profiler.

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International Journal Publications

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