STRUCTURAL AND ELECTRICAL PROPERTIES OF FLASH
MEMORY CELLS WITH HfO$_2$ TUNNEL OXIDE AND
WITH/WITHOUT NANOCRYSTALS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

DÖNDÜ ŞAHİN

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
PHYSICS

JULY 2009

Approval of the thesis:

STRUCTURAL AND ELECTRICAL PROPERTIES OF FLASH MEMORY CELLS WITH HfO$_2$ TUNNEL OXIDE AND WITH/WITHOUT NANOCRYSTALS

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ABSTRACT

STRUCTURAL AND ELECTRICAL PROPERTIES OF FLASH MEMORY
CELLS WITH HfO$_2$ TUNNEL OXIDE AND WITH/WITHOUT
NANOCRYSTALS

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July 2009, 96 pages

In this study, flash memory cells with high-k dielectric HfO$_2$ as tunnel oxide and group IV (Si, Ge) nanocrystals were fabricated and tested. The device structure was grown by magnetron sputtering deposition method and analyzed by various diagnostic techniques such as X-ray Photoelectron Spectroscopy (XPS) and Raman spectroscopy. The use of HfO$_2$ tunnel oxide dielectric with high permittivity constant was one of the main purposes of this study. The ultimate aim was to investigate the use of Si and Ge nanocrystals together with HfO$_2$ tunnel oxide in the memory elements. Interface structure of the fabricated devices was studied by XPS spectroscopy. A depth profile analysis was performed with XPS. Nanocrystal formations were verified using Raman spectroscopy technique. The final part of the study includes electrical characterization of memory devices fabricated using Si and Ge floating gate. C-V (Capacitance-Voltage) and G-V (Conductance-Voltage) measurements and charge storage behaviour based on C-V measurements were performed. For

comparison, structure of Si and Ge layers either in thin film or in the nanocrystal form were studied. A comparison of the C-V characteristics of these two structures revealed that the memory device with thin films do not confine charge carriers under the gate electrode as should be expected for a continuous film. On the other hand, the device with nanocrystals exhibited better memory behavior as a result of better confinement in the isolated nanocrystals. Trace amount of oxygen was found to be enough to oxidize Ge nanocrystals as confirmed by the Raman measurements. The charge storage capability is weakened in these samples as a result of Ge oxidation. In general, this work has demonstrated that high-k dielectric HfO_2 and group IV nanocrystals can be used in the new generation MOS based memory elements. The operation of the memory elements are highly dependent on the material and device structures, which are determined by the process conditions.

ÖZ

NANOKRİSTAL İÇEREN/İÇERMEYEN HfO$_2$ TÜNEL OKSİTİNDEN OLUŞAN BELLEK ELEMANLARININ YAPISAL VE ELEKTRİKSEL ÖZELLİKLERİ

Şahin, Döndü

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Temmuz 2009, 96 sayfa

Bu çalışmada, tünel oksiti olarak yüksek yalıtkanlı malzeme olan HfO$_2$ ile IV. grup elemanlarını içeren (Si, Ge) nanokristaller kullanarak flaş bellek hücreleri üretildi ve test edildi. Aygıt yapısı mıknatıslı saçtırma yöntemi ile üretildi ve tanı tekniklerinden X-ışını fotoelektron spektroskopisi (XPS) ile Raman spektroskopisi kullanılarak analizleri yapıldı. Bu çalışmanın esas amaçlarından birisi yüksek elektriksel geçirgenlikli HfO$_2$ tünel oksitinin kullanımıdır. Nihai amaç ise bellek elemanlarında HfO$_2$ tünel oksiti ile birlikte Si ve Ge nanokristallerinin kullanımını araştırmaktır. Üretilen aygıtların ara yüzleri XPS spektroskopi tekniği ile incelendi. XPS ile birlikte derinlik profili analizi yapıldı. Nanokristal oluşumları Raman spektroskopi tekniği ile doğrulandı. Bu çalışmanın son bölümü ise Si ve Ge yardımcı kapı kullanılarak üretilen bellek elemanlarının karakterizasyonunu içermektedir. C-V (Kapasitans-Voltaj) ve G-V (iletkenlik-voltaj) ölçümleri ile C-V ölçümleri temel alınarak yük depolama

özelliği incelenmiştir. Karşılaştırma yapabilmek için, Si ve Ge yapıları ya ince film içerisinde ya da nanokristal formda çalışıldı. Bu iki yapının C-V karakteristiklerinin karşılaştırması gösterdi ki, ince film içeren bellek elemanları yükleri hücre kapısı altında boyutsal sınırlamamaktadır. Diğer taraftan, nanokristal içeren aygıtlar izole olmuş nanokristallerin boyutsal sınırlama yapabilirliği olduğu için daha iyi bellek özelliği göstermektedirler. Düşük miktardaki oksijen varlığının Ge nanokristallerini oksitlemeye yeterli olduğu Raman ölçümlerinde de doğrulanmıştır ve oksitlenme sonucu bu örneklerde yük depolama özelliğinin azaldığı gözlemlenmiştir. Genel olarak, bu çalışma yüksek yalıtkanlığı olan HfO_2 ile IV. grup nanokristallerinin yeni nesil MOS tabanlı bellek elemanlarında kullanılabileceğini göstermiştir. Bellek elemanlarının çalışması kullanılan malzemeye ve yöntem şartları ile belirlenen aygıt yapısına son derece bağlı olduğu görülmüştür.

Anahtar Kelimeler: Mıknatıslı Saçtırma, C-V, Yuksek Gecirgenlik Sabiti, Flash Bellek, XPS, Yapı Analizi, Raman, Ge, Si.

to my lovely family...

ACKNOWLEDGEMENTS

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LIST OF SYMBOLS

A: Area

AFM: Atomic Force Microscopy

BTB Tunneling: Band to Band Tunneling

C: Capacitance

C_{OX}: Oxide capacitance

C-V: Capacitance-Voltage

CMOS: Complementary Metal Oxide Semiconductor

E_F: Fermi energy level

E_G: Energy gap

E_i: Intrinsic energy level

FG: Floating gate

FN: Fowler-Nordheim

G: Conductance

G-V: Conductance-Voltage

J: Current

k: dielectric constant of material

k_B: Boltzmann constant

MNOS: Metal-Nitride-Oxide-Semiconductor

MOS: Metal Oxide Semiconductor

MOS-C: Metal Oxide Semiconductor Capacitor

MOSFET: Metal Oxide Semiconductor Field Effect Transistors

n_i: Intrinsic charge concentration

N_S: Substrate concentration

P/E: Program/ Erase

PL: Photoluminescence

Q_i: Interface charge density

RTA: Rapid Thermal Annealing

SSD: Solid State Disc

SPM: Scanning Probe Microscopes

T_t: Transmission probability

TAT: Trap Assisted Tunneling

V_{FB}: Flatband voltage

V_G: Gate voltage

V_{TH}: Threshold voltage

W/E: Write/ Erase

X: Thickness

XPS: X-Ray Photoelectron Spectroscopy

ε: Dielectric Constant

ε_n: Discrete energy state

ρ: Charge density

$\hbar$: Planck's constant

χ_e: Electron affinity

Φ_M: Metal work function

Φ_{SC}: Semiconductor work function

CHAPTER 1

INTRODUCTION TO FLASH MEMORIES

1.1 Introduction and Motivation

From the talk given by Feynman in 1959, which is titled as "There is plenty of room at the bottom" [1] to now, there is a continuous improvement in technology and there are remarkable research on solid state field of physics. Every two years, number of transistors in a chip and concurrently performance doubles as stated in Moore's Law by empirical observation [2] and given in figure 1.1. Memory elements such as non-volatile flash memories also constitute an important position in these technological improvements.

Non-volatile flash memories are categorized in CMOS technology. Floating gate concept as a non-volatile element was first proposed in MOS technology to avoid intrinsic volatility problem in 1967 [3]. At the same time, Metal-Nitride-Oxide-Semiconductor (MNOS) concept was introduced to overcome the same problem. Then, in a short time in 1971, first 1 Kbit product of floating gate device was put into the market. Then, Fujio Masuoka invented the first flash memory in 1984 while he was working in Intel [4]. This development continues with the invention of NOR-type memory in 1988 and NAND type memory in 1989 by Intel and Toshiba, respectively. Currently, 256 GB SSD discs have been available in market [5].

CMOS technology is in a trend of getting smaller and smaller each year. As the dimension decreases, quantum mechanical phenomena such as Coulomb blockade and quantum confinement effects start to play important roles in device operations. For example, quantum size effect manifests itself as quantization of

energy levels in reduced dimensions like quantum wells, or quantum dots and this quantization may lead to useful or undesirable behaviors in the device.

Due to the demands towards faster, smaller and more reliable electronic and optical components in market, some novel structures such as nanocrystals, nanorods, nanotubes and nanoneedles have been investigated [6-9]. Among these, quantum dot structures have attracted great interest. Charge confinement occurs in 3-dimension in quantum dots (such as nanocrystals) and this confinement effect brings new and novel properties that can be utilized in devices to import with better performance and/or new functionalities.

One of the promising applications of nanocrystals has been proposed for nonvolatile memory devices, where they replace the conventional floating gate which is the storage medium in these devices. This type of memory structure has been studied to improve the existing flash memory technology due to promising results reported in literature [10-15]. The challenge is to retain compatibility with current technology, maximize reproducibility, and continue shrinking and power preserving, namely decreasing applied voltage for write/erase operations. Power is the most critical issue because high power also creates excess temperature during operation and device reliability depends on working conditions.
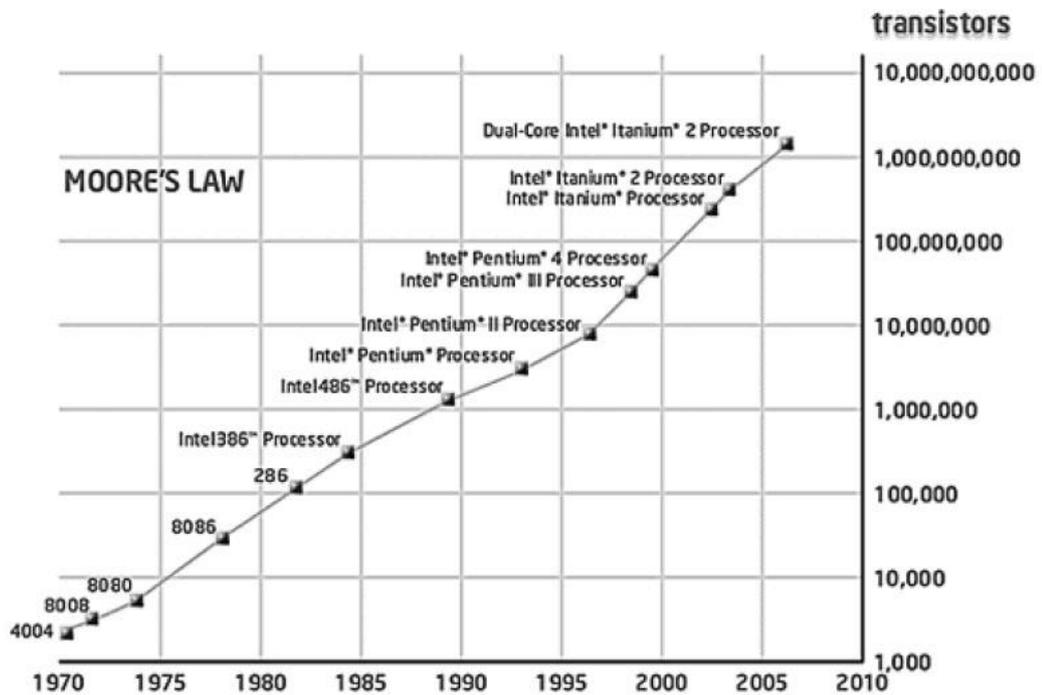
Figure 1.1: Transistor count according to Moore's Law- scaling issue and increase number of transistor per chip [24]

Nanocrystal memories have great potential due to their high performance, low power consumption, high program/erase speed [16-23]. The general aim of the reported studies has been to utilize this potential for higher capacity and longer data storage time. However, various aspects of fabrication and characterization of memory cells with nanocrystals need to be studied and understood before putting them into a mass production line. Thus, quantum dots made of nanocrystals and their usage in memory cells constitutes a popular and interdisciplinary research area including material science, physics and electronics.

Semiconductor nanocrystals with the size of 2-25 nm [25] show different properties as compared to their bulk form. Coulomb blockade, charge confinement and tunneling are the ones that need to be considered for

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write/erase/retention operations in memory devices [26]. Coulomb blockade and charge confinement effects are summarized schematically in figure 1.2 and figure 1.3, respectively. Quantum effects can be beneficial or harmful depending on the application. For memory devices, for example, tunneling is a beneficial quantum-mechanical event if it is not in excess at retention mode.
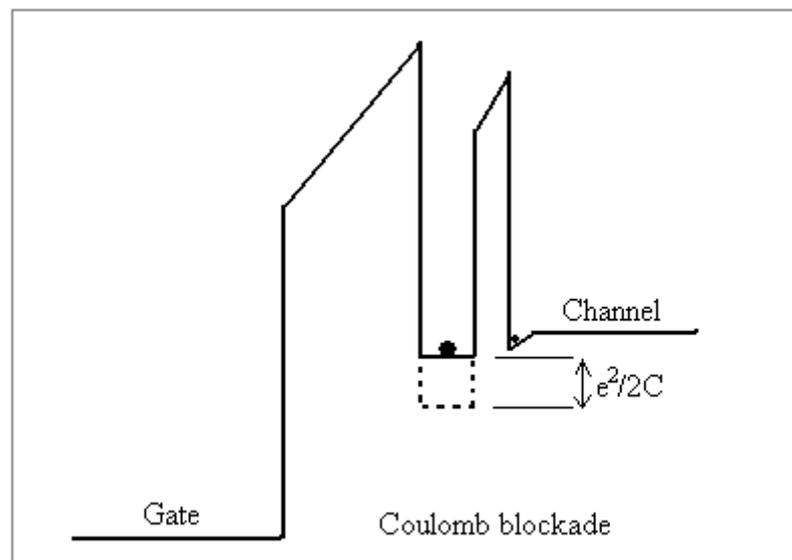
Figure 1.2: Representation of Coulomb blockade effect. After an electron is injected into quantum dot, it shifts energy level by $e^2/2C$ and blocks the other electrons to be injected. [27]
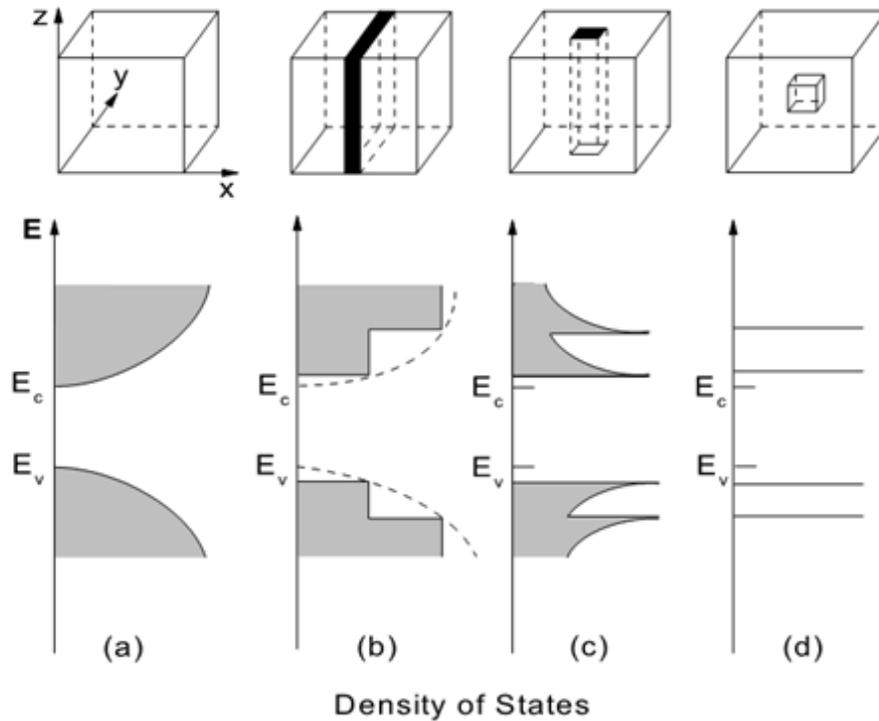
Figure 1.3: Density of states for (a) bulk material, (b) quantum well, (c) quantum wire and (d) quantum dot. [28]

Extensive research about flash memories has been carried out [29-35]. In this thesis, both continuous and nanocrystal floating gate flash memory cell structures with high-k tunnel barrier are fabricated and characterized. After a brief introduction to flash memories and concepts required for a better understanding, in chapter 2 discussions on new materials to replace silicon dioxide (SiO_2) for better memory cells are done. Experimental techniques used for fabrication and characterization of material and devices are explained in chapter 3. Then, in chapter 4, a study on structural and chemical properties of multilayer SiO_2/Germanium (Ge)/Hafnium dioxide (HfO_2)/Silicon (Si) structure and the effect of high temperature treatment is given. Chapter 5 deals with electrical characterization of memory cells with high-k tunnel oxide. Then, a short conclusion is given in chapter 6.

1.2 Introduction to Flash Memories

1.2.1 Frequently Used Terms in Flash Memory Characterization

Reliability is perhaps the most important issue in memory cells. It depends on "endurance" and "retention time" of the cell. However, the basis of these reliability issues bases on "degradation" effect. These concepts are clarified below.

Degradation: Degradation occurs under program/erase cycles. It is a kind of deformation in dielectric after injection and as a result a semi-conductive path is formed. Degradation effect is the main reason of reduced endurance and retention time, and reliability failure. When oxide deterioration is turned after charge injection or write/erase process, the cell faces degradation and finally results in breakdown. Breakdown occurs when tunnel oxide is totally degraded [26].

Endurance to Program/Erase (P/E) operation cycles: This parameter determines the life-time of the memory cell under operation. Endurance to P/E cycles determines the degradation occurring at threshold voltage with operation cycles. Since the flash memories are reprogrammed frequently and at each write/erase (or program/erase –P/E-) operation, some damages are introduced, lifetime of a memory cell is limited on a finite number of P/E cycles.

Nanocrystal memory cells are studied due to several promising and predicted advantages. One of them is the insignificant narrowing of the memory window [16, 21-22] after write/erase operation cycles ($>10^5$). The other one is that instead of using continuous floating gate layer, charge centers (quantum dots) are separated from each other and so data loss elimination is foreseen. With both of these advantages, endurance time extension is expected. In literature, it is stated that memory window closing results from hole trapping, in the opposite side memory window opening is due to electron trapping [3].

Charge Retention Time: It is different from endurance in the way of determining life-time of memory device under non-operation, namely the time determining the ability of holding information without performing any operation. With retention measurements, the reliability of the device to preserve data after loading is tested. In commercial memory cells, expected retention time is about 10 years. If the memory cell loses the information loaded, it is no longer non-volatile, meaning that it does not have the ability to preserve data without consuming any power. One of the aims of studies on nanocrystal based devices is to reach the retention time of the current technology and even increase it further.

Degradation directly effects the retention time because the damage in cell structure enhances the loss of data. With increasing number of P/E cycles, retention time decreases. This means that, after re-programming the cell many times, it does not meet its retention limit defined at the beginning. For charge trapping devices, retention is an intrinsic problem since trapping carriers as well as nitride layer in trap centers promotes the back injection.

Retention time measurements are done to test the reliability of the device and usually extrapolated after nearly 10^4-10^5 s up to 10^8 s (ten year is ~3.2×10^8 sec). It is the time sufficient for commercial flash-memory applications. In addition, the experiments are carried out at high temperatures (up to 250 °C) [21-22, 36-39] to observe the performance of memory cell, in a short time.

1.2.2   Commercially Available Flash Memories

Commercially available flash memories can be divided into two sub categories according to charge storage locations in MOS structure. One is "Floating gate" and the other is "Charge trap". Floating gate devices could have metal or semiconductor charge storage layers. In charge-trapping devices, charge is stored in an insulator layer consisting of silicon nitride (Si_3N_4), which is

intrinsically consisting of large number of trap sites. The most successful dielectric tunnel oxide used in this type is SiO_2. Other used dielectrics such as Al_2O_3 or Ta_2O_5 have also been suggested, but their material quality does not meet requirements for the memory cell technology.

Memories are divided into two sub-categories according to the retention behavior of data. One is volatile and the other is non-volatile. Volatile memories lose data when the power is off, whereas non-volatile memories retain the stored information even if the power is off. RAM (Random Access Memory) is the most widely used volatile memory today. DRAM (Dynamic- Random Access Memory) and SRAM (Static- Random Access Memory) are the examples for volatile RAMs. However, flash memories; such as AND, NAND and NOR are non-volatile type memories that are electrically erasable and programmable. Non-volatile memories are more expensive than volatile RAMs. Therefore, they are mainly used as secondary storage. The studies are towards to overcome this handicap. Beside, researchers are trying to improve the write/erase time of these non-volatile memories. Typically, achieved millisecond write/erase time for non-volatile memory cell operation is not suitable for communication with a CPU during program execution. Retention, endurance, degradation, reliability, reproducibility are important parameters and concepts defining the characteristics of non-volatile memory [27, 3].

1.2.3 Flash Memory Cells from Continuous Layer to Nanocrystal Floating Layer

Floating gate is the today's commercial technology for flash memories. The critical problem with this commercial device is to lose whole data instantly when a conductive path is occurred in the oxide. If the electrons or holes, trapped in the poly-Si floating gate is tunneled back to substrate or to the gate through a conductive path, all stored carriers are lost. The schematic of poly-Si floating

gate memory is shown in figure 1.3 (a). When positive voltage, in other words forward bias, is applied to the metal gate, electrons are stored in the floating gate layer. The electrons are injected through the tunnel oxide by the applied bias. This charging mechanism is the same for nanocrystal floating gate memories. The main difference is the "floating gate" structures, which are discrete charging trap sites for nanocrystal floating gate structure. Commercial ones are fabricated with poly-Si or nitride charge trap sites and these are continuous film layers.

As explained in previous sections, nanocrystal memory devices are promising for long time data endurance and more reliable due to charge separation nodes. As shown in figure 1.4 (a), when degradation occurs in floating gate layer, for continuous layer floating gate, all data is lost from this short circuit path created in channel. However, when one or a few of the nanocrystals are affected by this degradation effect, only the information hold by these nanocrystals is lost while the others remain (figure 1.4 (b)).

Replacing continuous film layer by nanocrystals brings a number of new physical research topics to the attention, such as confinement effects, Coulomb blockade, band engineering. Nanocrystal layer floating gate structure is schematically shown in figure 1.4 (b). This structure is the representation of sample by post annealing of thin layers (as in figure 1.4 (a) with 3-10 nm in thickness) at high temperatures in an inert gas ambient or vacuum ambient.
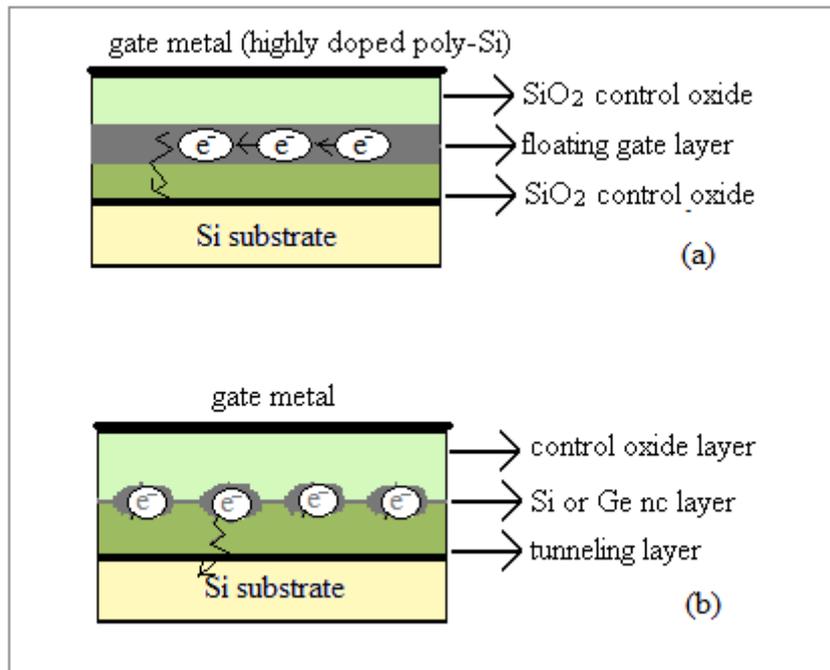
Figure 1.4: Schematic representation of Flash memory with (a) continuous floating gate (FG) layer and (b) Si/Ge nanocrystal FG layer. For FG layer any weak spot will result in complete loss of charge because the FG is a conductive film. For nanocrystal cell, weak spot will only result in a loss of a fraction of charge.

1.3   Basic Structures of Flash Memories

1.3.1   Metal Oxide Semiconductor Capacitor (MOS-C)

Metal-oxide-semiconductor (MOS) capacitor is the basic part of the Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs) and the memory cell structures used in technology as other electronic circuitry. MOS is a sandwich like structure consisting of a metal/oxide (insulator)/semiconductor layers as shown in figure 1.5. Since it is a capacitor in principle, it is highly charge sensitive. Due to this property, it can be used to investigate the electrical properties of the oxide layer and the interface.

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The most widely known MOS structure is the famous trinity, Aluminum (Al)/SiO$_2$/Si. Si is the substrate material and also it stands for "semiconductor" part in Metal-Oxide-Semiconductor. Then, SiO$_2$ is present on Si substrate and it is the dielectric layer, also called as oxide layer required for the MOS device. Finally, the metal gate, namely Al is formed as the gate electrode to have a conducting layer and accumulate charges on it. The capacitance of a MOS device is not constant as a function of the applied voltage. Therefore, it is not suitable to use static capacitance. Instead, differential capacitance should be considered. The differential capacitance is,

$$C_d = \frac{dQ_g}{dV_g}$$
eqn 1.1

where dQ$_g$ is the change of the charge on gate electrode and dV$_g$ is the applied voltage with AC (alternating current) amplitude superimposed on a DC (direct current) signal.

For an ideal MOS structure, the metal work function (Φ_M) should be equal to the work function of the semiconductor (Φ_{SC}). In addition, there should not be local charges in the oxide and the interface charges at Si/SiO$_2$ interface. However, in reality $\Phi_M > \Phi_{SC}$ or $\Phi_M < \Phi_{SC}$ and it is possible that charges can be accumulated in both oxide and at the interface.

Depending on the applied voltage, a MOS-Capacitor (MOS-C) has three different working regimes. It will be explained over p-type substrate below. First regime is accumulation of holes when the gate voltage V$_g$ is smaller than flatband voltage (V$_{FB}$) which is equal to zero for an ideal device. However, in reality, V$_{FB}$ is not zero due to the deviation from the ideality. Second regime is called depletion regime which occurs when V$_g$ is larger than V$_{FB}$ and smaller

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than the voltage to invert the interface and the third one is the inversion regime which is the case when V_g is large enough to collect the electrons in p-type doped Si.

If V_g < V_{FB}, then accumulation occurs: As seen from figure 1.5 (a), accumulation occurs with the help of the applied gate voltage (V_G). Electric field ($\mathbf{E}_f$) below the gate provides the driving force for the charge collection.

Capacitance of the system is due to the insulator so it results from the oxide capacitance.

$$C_{ox} = \frac{\varepsilon A_{ox}}{X_{ox}} \qquad\qquad \text{eqn 1.2}$$

A_{ox} is the oxide area and X_{ox} is the oxide thickness. Since A and X does not change with applied voltage, the capacitance is constant in accumulation region.

If V_g > V_{FB}, depletion region is created: As seen in figure 1.5 (b), when positive gate bias is applied to the gate metal, the region below the gate oxide is depleted from the free carriers (holes) by the electric field generated by the applied voltage. Consequently, the negative ions remain in this region, called depleted region. This results in the creation of a new capacitive contribution to the total capacitance of the device. Since the capacitance is proportional to the amount of charge in the depletion region, it is dependent on the magnitude of the voltage applied to the device. The total measured capacitance is then a function of the applied voltage.
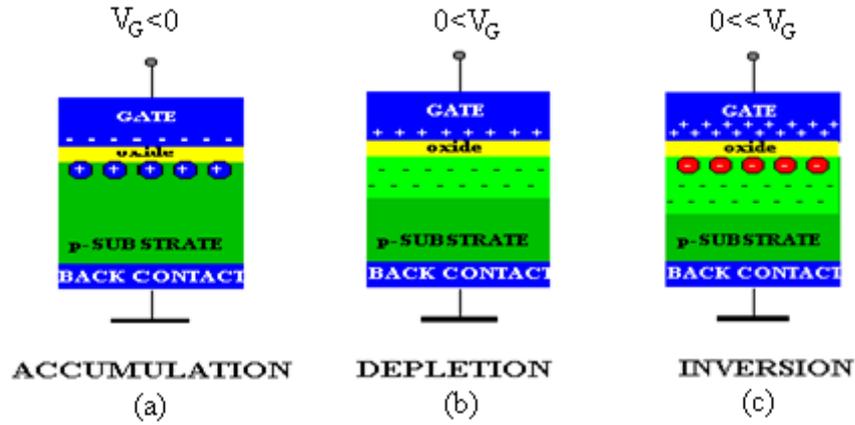
Figure 1.5: Working regimes of MOS-C as a) Accumulation b) Depletion and c) Inversion [40]

The relation (1.3) between gate voltage and depleted thickness can be written as;

$$X_d = function\left(V_g\right) \qquad \text{eqn 1.3}$$

Then, equivalent capacitance of a MOS device can be modeled as the total capacitance of two serially connected parallel plate capacitors that is shown in figure 1.6. C_{ox} and C_d are capacitors associated with the oxide layer and the depletion layer, respectively and R_s is the serial resistance of substrate. Then, the total capacitance of the system can be written as,

$$C_{eq}^{-1} = C_{ox}^{-1} + C_d^{-1} \qquad \text{eqn 1.4}$$

where

$$C_d = \frac{\chi_d}{\varepsilon_s} \quad \text{and} \quad \chi_d = \sqrt{\frac{2\varepsilon_s \Phi_s}{qN_a}} \qquad \text{eqn 1.5}$$

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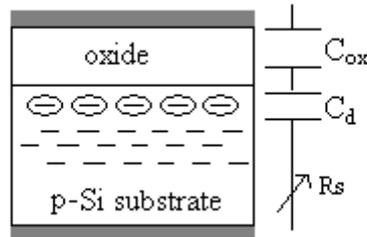
Figure 1.6: Modeling of depletion region total capacitance connected in series. C_{ox} and C_d stand for oxide and depleted region capacitances, respectively. In addition Rs represents serial resistance.

If electrons cannot be supplied to device at high voltages, inversion region does not form. This is called deep depletion. The deep depletion occurrence can easily be understood from a Capacitance-Voltage (C-V) curve, which shows continuous decrease in capacitance with increasing voltage. It will be clarified at the end of this section.

If $V_g \gg V_{FB}$, then inversion occurs: For this condition, electrons in the p-type Si are included in the process because the gate voltage is large enough to collect the minority carriers (electrons) at the SiO_2/Si interface. Free electrons inside Si are collected up the interface as shown in figure 1.5 (c). In inversion, change in the amount of the ions and free electrons due to the change in the applied AC voltage are independently formed. Inversion capacitance is not influenced by gate voltage anymore. This means that if the frequency is high, electrons in the inversion layer cannot follow the signal and the capacitance is the sum of the oxide and depletion layer capacitance. On the other hand, if the frequency is lowered, the electrons in the inversion layer can take part in the process and equivalent capacitance increases. The equivalent capacitance can reach the value measured in accumulation region.

Inversion condition occurs when the surface potential is higher than a certain threshold value. This threshold value is satisfied when,

$$\psi_s = 2\,\Phi_F \;\; \text{with} \;\; \Phi_F = \frac{\pm(E_i - E_F)}{e} = \frac{k_B T}{e} \ln\left(\frac{N_s}{n_i}\right)$$

eqn 1.6

where Φ_F is the Fermi potential, $_+$ and $_-$ corresponds to p- and n-type substrate, respectively. E_i and E_F are Fermi energy levels of intrinsic and aligned, respectively, k_B Boltzman constant, N_s substrate carrier concentration and n_i intrinsic carrier concentration. Then, maximum depletion layer thickness is;

$$X_{dep,max} = \left[\frac{4\varepsilon_s k_B T ln\left(\frac{N_s}{n_i}\right)}{e^2 N_s}\right]^{1/2}$$

eqn 1.7

As explained above, there are two possible capacitance conditions depending on the frequency in the inversion region. Firstly, if frequency is low, capacitance value approaches to oxide capacitance as described in eqn 1.2. This means that the electrons in the inversion layer follow the applied gate voltage bias. However, if frequency is high then the depletion region is affected and capacitance is calculated using eqn 1.4.

An ideal C-V curve is roughly shown in figure 1.7. V_{FB} and V_{TH} voltages correspond to flatband and threshold voltage, respectively.
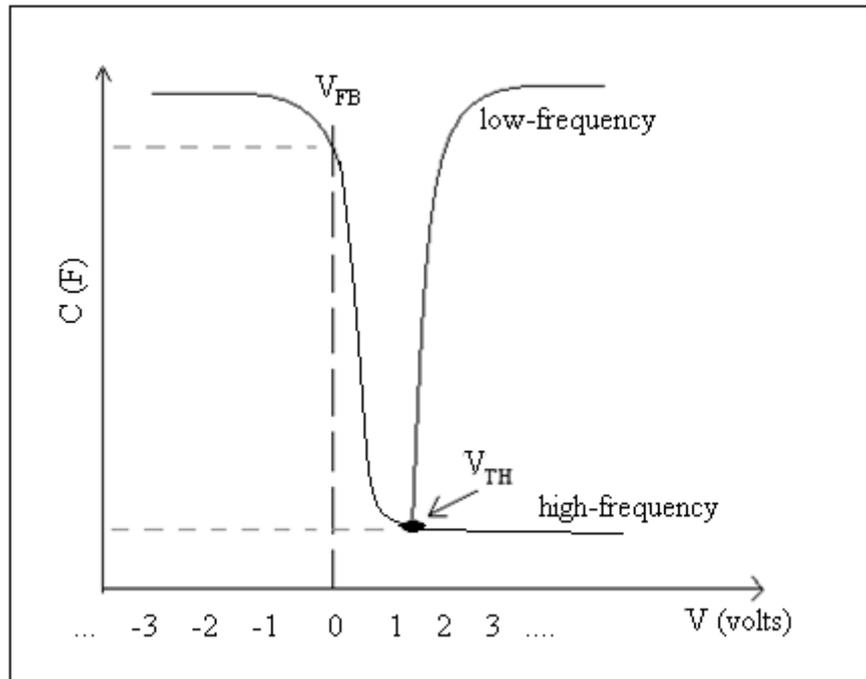
Figure 1.7: Ideal C-V curve under high-frequency and low frequency measurement.

However, in reality, C-V curve is affected by various factors like work function difference and oxide charges. Thus, the shape and the characteristics of the CV curve deviate from ideality depending on the charge concentration distribution, interface charges, oxide charges (as mentioned in more detail in previous section), work function difference between gate metal and semiconductor. Fixed charges make the curve shift in parallel to original curve, while dynamic charges affect the curve depending on the applied voltage. To visualize, this is shown schematically figure in figure 1.8, 1st line shift is due to fixed charges and 2nd line results from the dynamic charges and 3rd one represents the deep depletion. Deep depletion occurs if minority charges could not be collected at the interface.

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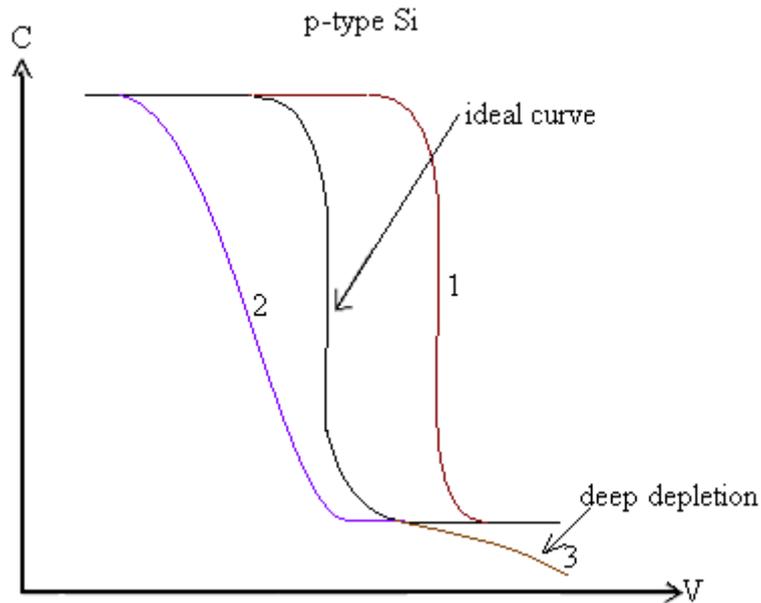
Figure 1.8: Shift from ideal C-V curve. Curve 1 stands for fixed oxide charges, 2 stands for mobile charges and 3 results from that minority carriers are not being able to collected in inversion region.

1.3.2 Basic parameters of MOS-Capacitor

Fixed oxide charges: Positive charges due to structural defects are classified under this group. The origin of these charges is oxidation process, temperature, ambient, cooling condition and substrate orientation. This type of charges affects the device performance.

Oxide trap charges: These charges can be positive or negative and formed during tunneling, injection or erasing mechanisms. They are usually located close to the interface.

Mobile oxide charges: These are generally resulting from ionic impurities such as Sodium (Na^+), Potassium (K^+), Lithium (Li^+) and hydrogen (H^+). Since these are mobile ions, they show time dependent behavior.

Interface trapped charges: These charges can be both positive and negative depending on the defect sites and/or impurities. They are located at the interface of any two different materials. Interface trap charges can be charged or discharged depending on the gate potential polarity. If they are dynamic states, additional path is created and this may result in discharging of the stored data. These charges generate electrostatic effects because of the interaction with the stored charges and affect the voltage drop (or electric field) on dielectric. Interface charges are mostly neutralized in hydrogen or deuterium ambient at low temperatures.

Flatband Voltage: Flatband voltage (V_{FB}) is the voltage that must be applied to obtain the flat band condition as shown in figure 1.9 which shows $Al/SiO_2/Si$ MOS-C structure. Flatband voltage in ideal conditions is required be zero under no applied voltage bias. However, if work function difference exists between semiconductor and metal, then one needs to provide the energy equal to the amount of the work-function difference to get flat band condition.

Work function (Φ) is the energy necessary to extract an electron from Fermi level to the vacuum level. It is $\Phi_M = 4.1$ eV for aluminum. The term work function is called as electron affinity (χ_e), if one is talking about work function of semiconductor. It is the energy required for an electron to jump into vacuum level from conduction band level. Electron affinity of the silicon dioxide is $\chi_{ox} = 0.9$ eV and silicon is $\chi_{Si} = 4.05$ eV. The work function difference between Si and Al is 0.05 eV. In addition, if there are also oxide charges, interface charges and/or charge inhomogenity in the structure, flatband condition is different than the work function difference.
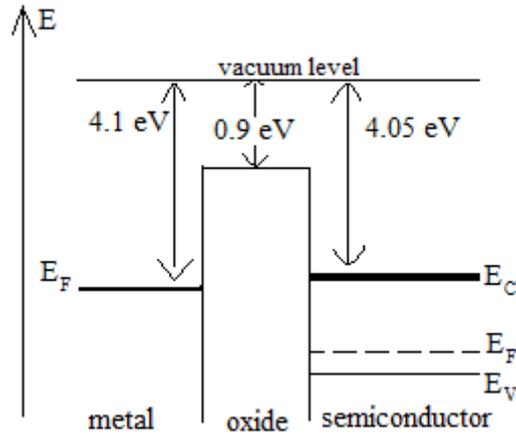
Figure 1.9: Ideal Metal-Oxide-Semiconductor structure band diagram explained over Al/SiO$_2$/Si (p-type) [41]

The flatband voltage in ideal condition is equal to work function difference between metal and semiconductor (It is the first term, Φ_{M-SC}, in eqn 1.8). However, band structure might be affected by the applied voltage falling across the oxide, resulting from fixed charges in the oxide and also charge distribution at the interface. Thus, the formulation turns into a little complex form [41]. All these effects and parameters can be combined in a single expression given by eqn. 1.8. This relation gets more complicated if moving charges are considered.

$$V_{FB} = \Phi_{M-SC} - \frac{Q_i}{C_{ox}} - \frac{1}{\varepsilon_{ox}} \int_0^{t_{ox}} \rho(x)dx \qquad\qquad \text{eqn 1.8}$$

where Q_i is interface charge density, C_{ox} is oxide capacitance, ε_{ox} is permittivity of oxide and $\rho(x)$ is the charge density in oxide.

Φ_{M-SC} depends on the doping density (N_d), intrinsic carrier density (n_i), energy gap (E_g), metal work function (Φ_M) and electron affinity (χ). In eqn 1.9 there is a logarithmic relation of metal-semiconductor work function with doping density and intrinsic carrier density.

$$\Phi_{M\_SC} = \Phi_M - \Phi_{SC} = \Phi_M - \chi - \frac{Eg}{2q} + V_t ln\left(\frac{Nd}{ni}\right) \qquad \text{eqn 1.9}$$

Threshold voltage: Threshold voltage is the value of gate voltage at which electrons are accumulated (for p-type Si) at the interface of semiconductor and tunnel oxide (inversion regime). Threshold voltage is a critical value that is necessary to form a conducting channel between source and drain of MOSFET creating a low resistance path for carriers. By applying a gate voltage simultaneously, carriers are collected at the available sites inside the oxide such as at defect states or in semiconductors inside the nanocrystals, in our case. When voltage is above the threshold voltage, transistor is said to be ON. If the gate voltage exceeds the threshold voltage limit significantly, this condition is called strong inversion.

1.4   Tunneling Mechanisms During Programming and Erasing (Write/Erase) Processes

There are various tunneling mechanisms used to explain programming and erasing conditions, such as direct band to band tunneling, trap-assisted tunneling, Fowler-Nordheim tunneling, modified Fowler-Nordheim tunneling, band to trap tunneling and trap to band tunneling. First three of these mechanisms will be explained in the following sections. More information on the transport mechanisms is available elsewhere [39].

The electron propagation through a potential barrier is called tunneling. Tunneling is a quantum mechanical phenomenon according to which the wave function does not vanish immediately in the barrier region; it decays exponentially into barrier material and leaves it on the other side if the barrier is thin enough. It depends on the barrier height, applied field and availability of the states in both sides of the barrier.

Some details of the different tunneling mechanisms are given below.

1.4.1 Fowler-Nordheim Tunneling (FN): In the presence of high electric field (E_{field}), band barrier is bent as shown in figure 1.10 (a) and current increases in the device, due to electron injection through a triangular shaped barrier [33]. Current density of FN tunneling is given by eqn 1.10 [3];

$$J_{FN} = a\ |E|^2\ exp(-b/|E|) \qquad\qquad \text{eqn 1.10}$$

where a and b are fitting parameters and E is the electric field falling on oxide.

1.4.2 Direct Band to Band Tunneling (BTB): It is called direct tunneling because the process occurs directly from a band to the other. High field in oxide promotes the Fowler-Nordheim tunneling. This can be explained using equation $E = \frac{V}{d} > \Phi_B$ where Φ_B is the barrier height while lower electric field is the direct tunneling ($E = \frac{V}{d} < \Phi_B$) [42]. Direct tunneling is shown in figure 1.10 (b), and no other sites such as trap sites take role in this mechanism. This increases the power consumption of large scale integrated circuits. Reducing tunnel layer thickness increases the probability of direct tunneling. This type of

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tunneling occurs without thermal activation. Meanwhile, it is the high-speed mechanisms to write information.

The main difference of direct tunneling mechanism from Fowler-Nordheim tunneling is the dependence on the temperature (T). It comes in current derivation as second order factor.

$$J_{BTB} = A^* T^2 \exp(-\beta \emptyset_b) \exp\left(\frac{-q\emptyset_s}{kT}\right)\left[\exp\left(\frac{qV_G}{kT}\right) - 1\right]$$ eqn 1.11

where A* is the Richardson constant, exp(-βϕ$_b$) is the tunneling probability, φs is the Schottky barrier between the gate and the semiconductor [41].

The transmission probability (T$_t$) for a charge carrier is given by [3],

$$T_t = \left[1 + \frac{E_0^2 sinh^2 \beta W}{4E\ (E_0 - E)}\right]^{-1}$$ eqn 1.12

with $\beta \equiv \sqrt{\frac{2m(E_0 - E)}{\hbar^2}}$ eqn 1.13

where E is the energy of the carrier, E$_0$ is the barrier height and W is the thickness. With decreasing thickness, predominant injection form direct tunneling of carriers.

1.4.3 Trap-Assisted Tunneling (TAT): Tunneling does not occur directly, instead tunneling mechanism requires a trap host site, and process arises more than one step. This mechanism is shown figure 1.10 (c). This tunneling type is observed after write/erase operation cycles even though it is not present at the beginning. The main reason is degradation of dielectric after operations such as Fowler-Nordheim and direct tunneling.
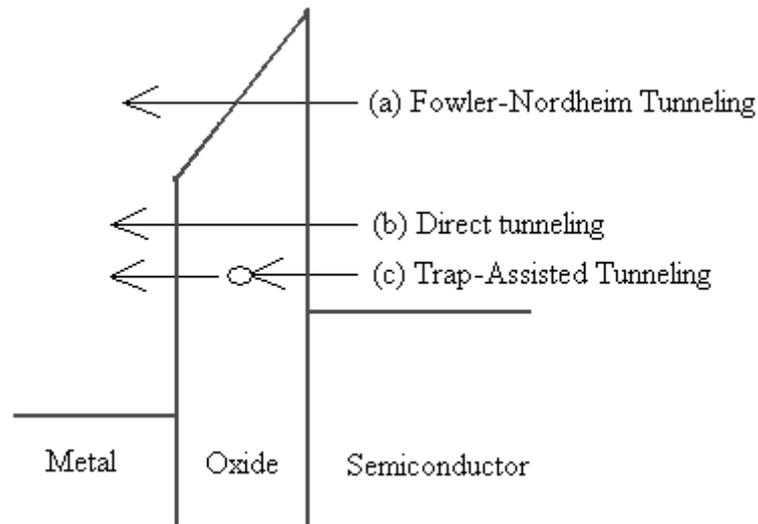
Figure 1.10: Emission of charge by Fowler-Nordheim (a), direct (b) and trap-assisted tunneling (c) mechanisms.

1.5 Charge Density Calculations

Charging calculations for continuous layer floating gate memory cell devices and nanocrystal floating gate devices are given in eqn 1.14 and eqn 1.16, respectively. Accumulation capacitance obtained with continuous floating gate memory cell is equal to the capacitance of control oxide as given in eqn 1.14.

$$n = \frac{C_{eff}\, \Delta V}{q} \qquad\qquad \text{eqn 1.14}$$

where C_{eff} is the effective oxide capacitance, ΔV is the shift in voltage with charge accumulation and q is the electric charge. Charge density is calculated per area to eliminate the gate area contribution. Thus, effective capacitance is divided by gate area of the device.

Charge density calculation differs for nanocrystal floating gate memories. The reason is that capacitance measured with C-V response is reflecting the effect of the stored charges in confined nanocrystals. Charges injected into nanocrystals can be accepted as the screening of the gate charges. This effect decreases the conduction in inversion regime. Due to reduction in conduction, threshold voltage shifts and this shift in threshold voltage is calculated by,

$$\Delta V_T = \frac{q n_{nc}}{\varepsilon_{ox}} \left(t_{cntl} + \frac{1}{2} \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\, t_{nc} \right) \qquad\qquad \text{eqn 1.15}$$

If n_{nc} needs to be calculated then this relation becomes,

$$n_{nc} = \frac{\Delta V_T\, \varepsilon_{ox}}{q} \frac{1}{\left(t_{cntl} + \frac{1}{2} \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\, t_{nc} \right)} \qquad\qquad \text{eqn 1.16}$$

where ε_{ox} and ε_{Si} are the permittivity values of oxide and Si substrate, t_{cntl} is the thickness of control oxide, and t_{nc} is the linear dimension of nanocrystals and ΔV_{TH} is voltage shift in threshold [43].

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CHAPTER 2

NOVEL DIELECTRIC MATERIALS FOR SiO$_2$ REPLACEMENT

2.1   Introduction

Scaling issue of microelectronics circuitry and increasing need of overcoming power consumption problem force scientists and technologist to look for new materials to overcome these difficulties arising from the limiting conditions at reduced size. In figure 2.1, it is shown that SiO$_2$ has reached its 90 nm scaling node and even it further decreases below 90 nm [44-46]. Intel announced its Hafnium-based 45 nm process technology in 2007 [47].

Below a certain thickness (~8 nm) of SiO$_2$, tunneling current increases rapidly [48] due to the quantum tunnel effect. The current flow through the oxide creates defects during operation, limitations start and reliability of these devices becomes additional problem. To overcome the problem, replacement of SiO$_2$ with another dielectric which can be grown physically thicker can be one of the solutions. Thus, integrated circuit technology is looking for potential dielectric materials to replace SiO$_2$. This is required to suppress the increase in degradation of oxide as a scaling issue. SiO$_2$ continues to shrink every two years according to Moore's Law and as a result degradation of oxide increases. When it exceeds the current limit, it takes away the advantage of low power, simultaneously [49].

Alternative high-k materials with high permittivity constant ($\varepsilon=\varepsilon_0 k$ where k is the dielectric constant of material and ε_0 is the electric constant of free space) having potential to replace SiO$_2$ have been investigated. Thus, moderately high-

k and high-k materials with k values ranging from 4<k<10 (moderately high-k) and 10<k<100 (high-k) have been studied widely [50-52].
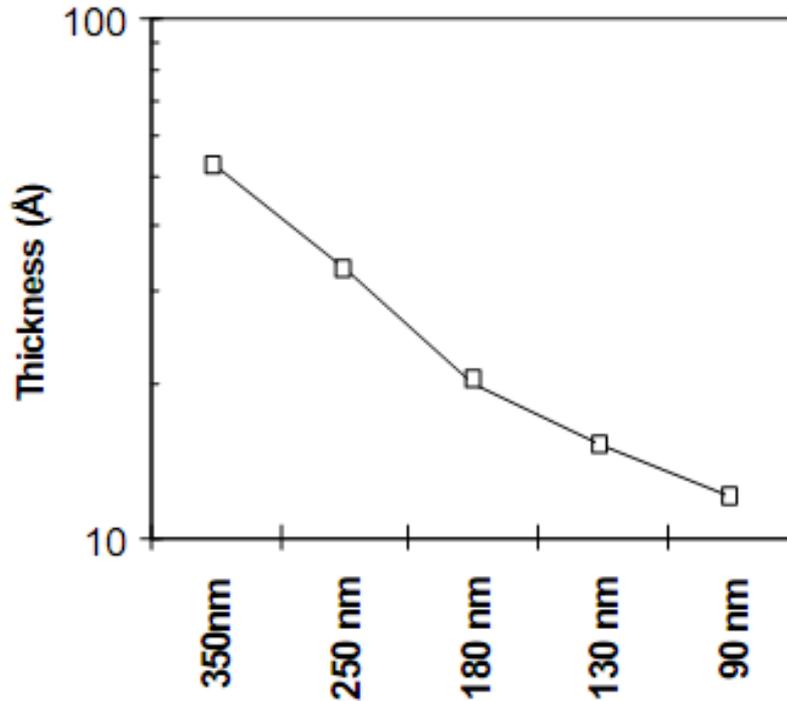
Figure 2.1: Scaling issue of SiO_2. Further scaling requires alternative materials to compensate leakage current, tunneling effect and etc. [53]

Silicon nitride (Si_3N_4) and aluminum oxide (Al_2O_3) have relatively low-k values that are k~7.5 and k~10, respectively. Si_3N_4 has an excellent interface with Si but its relatively low-k value limits its widespread use [54]. Thus, it is not ideal for 'long-term' scaling replacement.

Compared with Si_3N_4, Al_2O_3 has higher dielectric constant and larger band offset but due to interfacial charges formed between Si and Al_2O_3 during fabrication, it shows poor carrier mobility [55].

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With the stringent requirements of flash memory technology, search for better dielectric materials are continuing. Some of the candidates with the requirements are discussed below.

2.2   Requirements for High-k Dielectric Materials

The major advantage of using material with high permittivity (ε_k) is the requirements to suppress leakage current by increasing physical oxide thickness that is corresponding to the same capacitance value obtained by a physically thinner SiO_2. This is explained using a concept that is called equivalent oxide thickness (EOT). EOT represents the electrical thickness (not physical one) which corresponds to the same capacitance value with a thinner SiO_2 dielectric layer. As it is stated in chapter 1 (eqn 1.2), capacitance is given by the formula,

$$C_{ox} = \frac{\varepsilon_k \, A_{ox}}{X_{ox}} \qquad\qquad \text{eqn 2.1}$$

From this equation, we see that the capacitance decreases with the reduced device area. In order to maintain the same capacitance value with decreasing device area the thickness of the dielectric oxide layer should be reduced. However, after a certain thickness, it will not be permitted to decrease physical thickness further because device does not work as required due to the increased tunneling current. Alternatively, a new dielectric material with high dielectric constant can be used to accommodate the areal reduction in lateral dimension.

If dielectric constant is doubled by using a new high-k material, it is balanced with doubled-thickness of this high-k (X_{k-ox}) material keeping the EOT constant (eqn 2.2). Thus, high-k materials such as hafnium dioxide (HfO_2), beryllium

oxide (BeO), zirconium dioxide (ZrO_2), aluminum oxide (Al_2O_3), titanium dioxide (TiO_2) and tantalum oxide (Ta_2O_5) meet expectations in this way.

$$C_{ox} = \frac{\varepsilon\, A_{ox}}{X_{ox}} = \frac{\varepsilon_k\, A_{k-ox}}{X_{k-ox}} \qquad\qquad \text{eqn.2.2}$$

where ε_k is the permittivity and A_{k-ox} is the area of high-k material.

In a study reported previously [56], formation of metal oxide and silicate/silicide were calculated using Gibbs free energy approach. It was shown that thermodynamically most stable high-k materials are BeO, ZrO_2 and HfO_2, compared to Al_2O_3, TiO_2 and Ta_2O_5 [57].

The majority of investigated high-k materials are Zr-based and Hf-based dielectrics [58-62] and they almost have the same physical and chemical properties [53-57]. Their lattice constants are nearly same, ~0.78Å and 0.79 Å for HfO_2 and ZrO_2, respectively and their band offsets are relatively higher than other dielectric materials as given in figure 2.2. This figure explains the suitability of HfO_2 and ZrO_2 for Si in memory applications. Since there is an inverse relation between the dielectric constant and band offset between the oxide and the semiconductor [57], which is given in figure 2.3, optimum parameters should be chosen.

ZrO_2 and HfO_2 are the best alternatives for SiO_2 in device fabrication technology when figure 2.2 and figure 2.3 are considered together. In figure 2.3, there is an inverse relation between energy gap and dielectric constant. The reason is that high-k materials are from the transition metals of periodic table with d shell orbital which are not filled completely. This incompleteness introduces energy levels in energy gap with high density of states. This effect results in a relatively small energy gap.
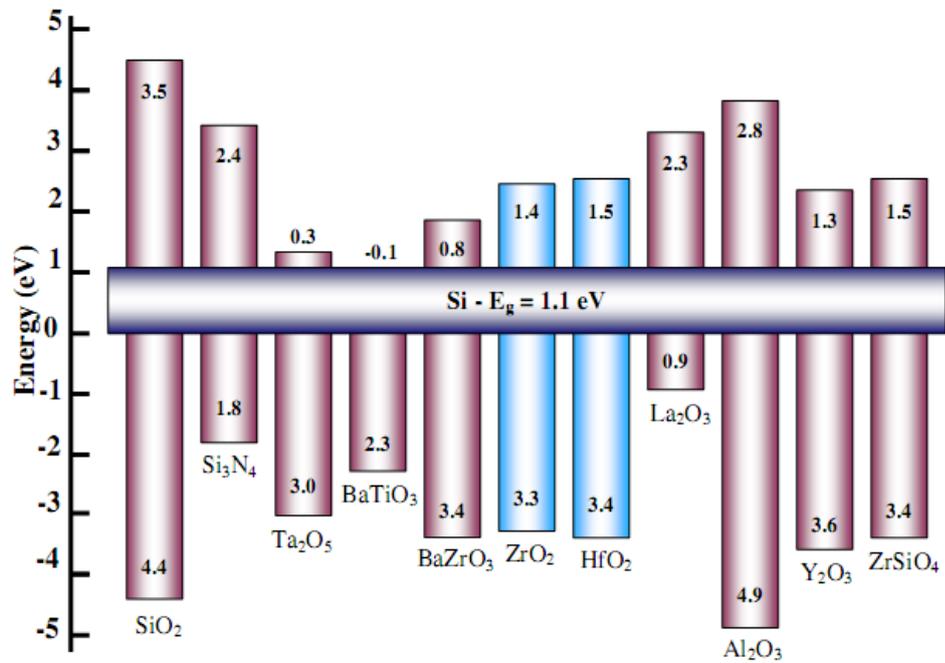
Figure 2.2: Band gaps and band offsets of various high-k materials. Since high-k engineering requires not only wide band gap but also large band offset, HfO_2 and ZrO_2 are better as their dielectric constants are considered also after SiO_2. [57].
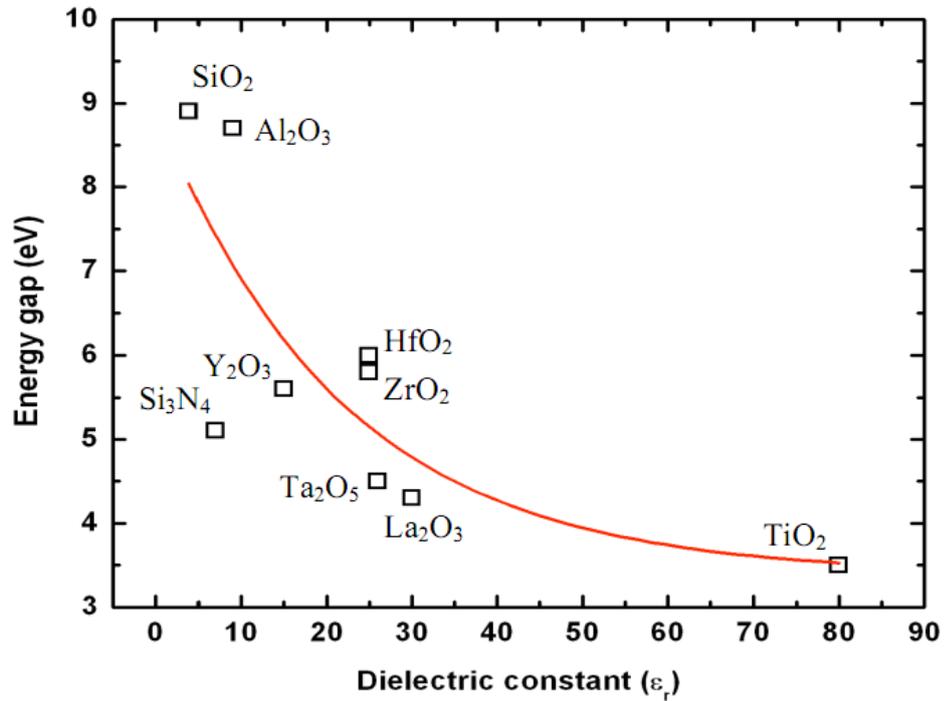
Figure 2.3: Inverse relation between energy gap and dielectric constant for different oxides [57]

2.3 HfO₂ as a High-k Dielectric in Flash Memory Technology and Replacement Challenges

HfO_2 is a promising material to replace SiO_2 due to its achievable equivalent oxide thickness and relatively higher band gap. Besides, HfO_2 is a high-k dielectric and it can be grown physically thicker to obtain a capacitance value equal to that of lower dielectric materials. Due to its larger physical thickness, high-k dielectric could decrease the tunneling or degradation effects. In addition, HfO_2 has asymmetric band-configuration for electron and hole barrier as shown in figure 2.4. This configuration makes the probability of electron and hole injection different. In this figure, there is a difference between work function of Al and activation energy of HfO_2 so there is an energy shift of 0.3 eV.
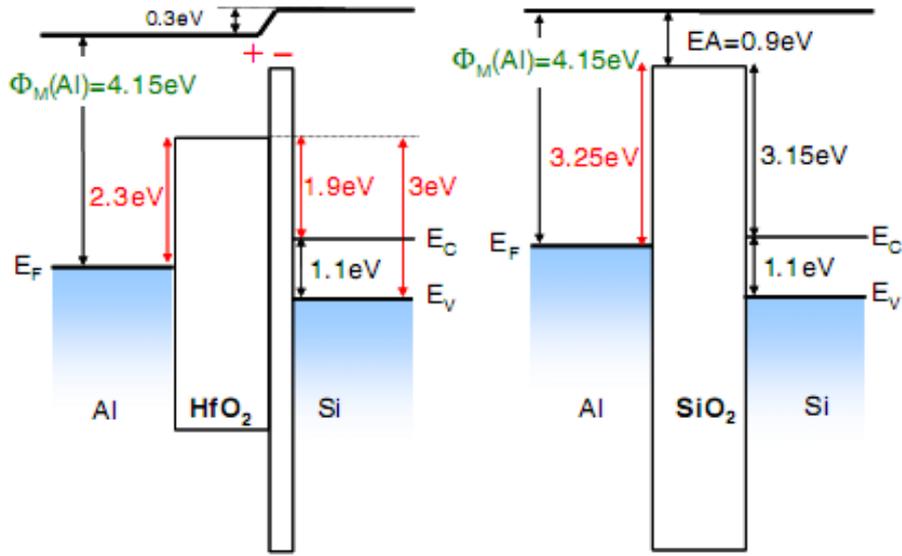
Figure 2.4: Band structure of HfO_2 with Si and SiO_2 compared with dielectric SiO_2 [63]. In the first figure intermediate band between Si substrate and HfO_2 corresponds to SiO_2.

Asymmetric band offset increases the retention time of an electron. Thus, HfO_2 as a high-k dielectric is foreseen to improve the memory device performance in the future. Due to these promising properties, HfO_2 seems more suitable for further downscaling of CMOS technology. One of the problems with HfO_2 fabrication is the undesirable interface formations with lower-k dielectric during growth and annealing processes. This interface formation degrades the memory cell performance. There are various studies to optimize and avoid the interface layer formation, such as using a buffer layer or surface passivation techniques. If substrate is Si and high-k dielectric is grown on this substrate, as a buffer layer, a thin Hf layer is used to suppress formation of intermediate SiO_2 [64]. In another case, if the interface is formed with Ge and HfO_2, and a hafnium oxide layer is grown on Ge, it is followed by either NH_3 annealing [65] or SiH_4 annealing [66] for the passivation of the surface. The band structure of this

arrangement is given in figure 2.5 comparing with Si case. It has advantageous because hole barrier of device structure for Ge increases more than Si floating gate case.
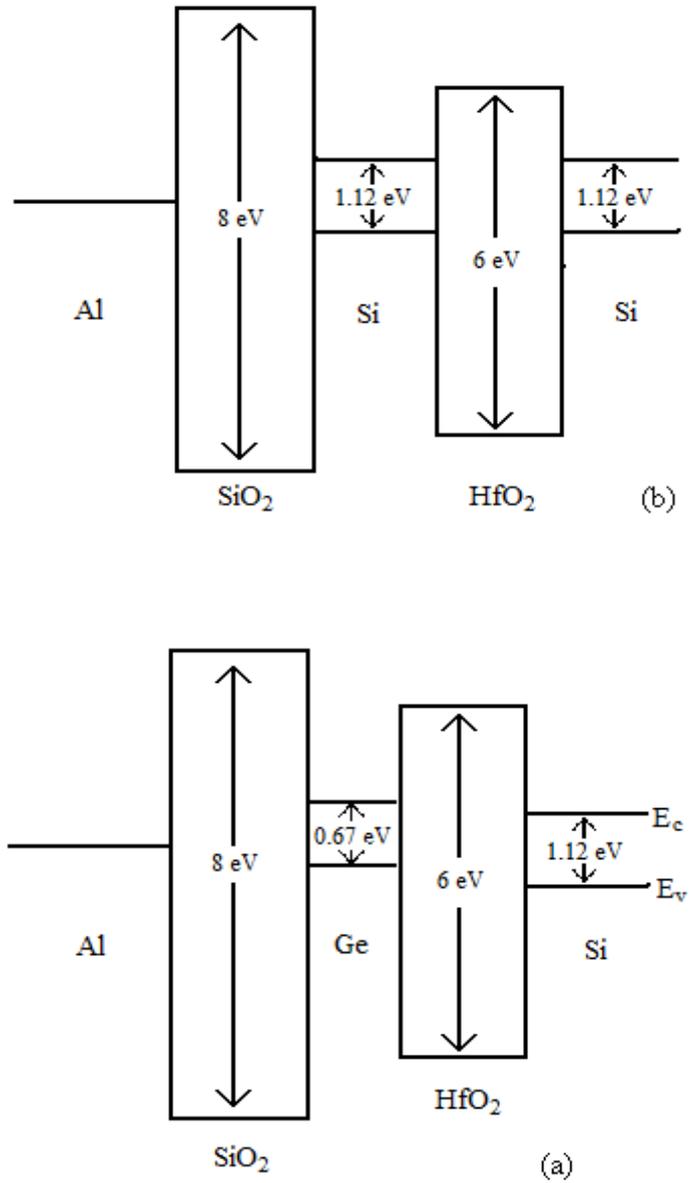
Figure 2.5: Electron energy band diagrams of Al/SiO$_2$/Si/HfO$_2$/Si structure (a) and Al/SiO$_2$/Ge/HfO$_2$/Si structure (b).

SiO$_2$ is the native oxide of Si and as given in table 2.1 there is no interfacial mismatch between Si and SiO$_2$. Nevertheless, it is not the case for high-k dielectric stacks. The basic problems to replace commercial MOS structure of Poly-Si/SiO$_2$/Si substrate are incompatibility of poly-Si/high-k dielectric stack due to Fermi level pinning and mobility degradation. To overcome these problems, an alternative metal gate is replaced with poly-Si gate. Appropriate metal choice is done for high-k dielectric replacement case according to metal work function. Being used in CMOS technology both for n-MOS and p-MOS, the metal work functions that are mid-gap or nearly mid-gap of high-k materials are studied in literature.

HfO$_2$ is the widely studied high-k material since its dielectric constant is more than 5 times larger than that of SiO$_2$ (table 5.1). Although band gap is relatively smaller than SiO$_2$, band offset inequality overlaps that negative effect and increase data retention. As it is the case for other high-k dielectrics, interfacial mismatch causes intermediate formations. However, there are various solutions proposed and attempted to overcome this negative effect. The material properties of HfO$_2$ are summarized in table 5.1 in comparison with SiO$_2$.

Table 2.1: Comparison of HfO_2 with SiO_2, the native oxide form of Si, in various aspects

Material Properties	SiO_2	HfO_2
Dielectric Constant (ε_r)	3.9	~25
Band gap (eV)	9	6.0
Conduction band offset (eV)	3.5	1.5
Valance ban offset (eV)	4.4	3.4
Density (g/cm3)	2.27	9.68
Lattice constant (Å)	5.43	5.12
Lattice mismatch with Si	-	~5.7 %
Reactive index	1.46	2.2

In this study, we have performed careful analysis of the interface by diagnostic techniques such as X-ray photoelectron spectroscopy (XPS) and Raman spectroscopy. In order to understand the device behavior, the interface structure should be clearly understood as it plays a crucial role in the operation of our devices. Samples used in this study were prepared by magnetron sputtering deposition technique. Compared to the atomic layer deposition (ALD) and chemical vapor deposition (CVD) methods, sputtering technique is more detrimental for structure but to eliminate this effect sputtering power is reduced. In spite of the intermixing problem between two materials, this method is compatible for mass production. Therefore, we investigated a memory cell type structure fabricated by magnetron sputtering structure of SiO_2/Ge(Si) on HfO_2/Si stack layer.

CHAPTER 3

NANOCRYSTAL MEMORY CELL FABRICATION AND CHARACTERIZATION METHODS

3.1   Instrumentations for Fabrication

3.1.1 Magnetron Sputtering Deposition Technique: Sputtering is a physical deposition and a high vacuum technique, and its mechanism bases on the energy and momentum transfer from ionized sputtering gas to the target. Under a low pressure inert sputtering gas (Ar in this study) and a high voltage across anode and cathode, plasma is created. Under glow discharge condition, cathode material is bombarded with Ar ions and specimen on anode is coated by the knocked of material.

In this study, all depositions except for HfO_2 tunnel layer were produced by Nano D100, a multi target sputtering system produced by VAKSIS Ltd. A picture of sputtering system is given in figure 3.1. It is a planar magnetron sputtering and a capacitively-coupled system. In addition, an RF supply is available in the system which allows for the deposition of semiconductor materials as well as metals. 3 inch targets are used as source materials. It is also possible to heat the substrate from backside with an infrared heater. Thickness of film layer can be measured during deposition by quartz thickness monitor attached to the system. Installed turbo molecular pump drops base pressure down to 10^{-7} Torr.
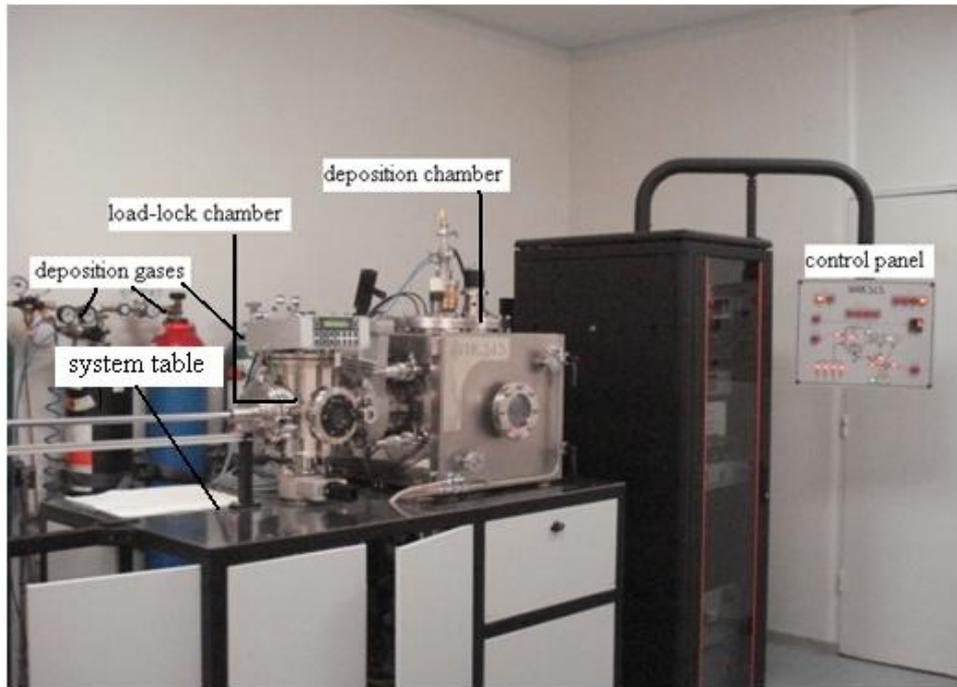
Figure 3.1: Picture of NANO-D 100

3.1.2 Thermal Evaporation Technique: In this study, metal electrodes were formed using thermal evaporation technique. Aluminum was used for metal electrodes. Contact area of gate electrode was fixed to 5.03×10^{-3} cm^2 for all samples using a shadow mask. Vacuum chamber of evaporation system was pumped by diffusion pump by which base pressure could be dropped down to 10^{-6} Torr in about 3.5 hours. Cooling was provided by both circulating water system connected to chiller pump and liquid nitrogen. Schematic representation of evaporation system is given in figure 3.2.
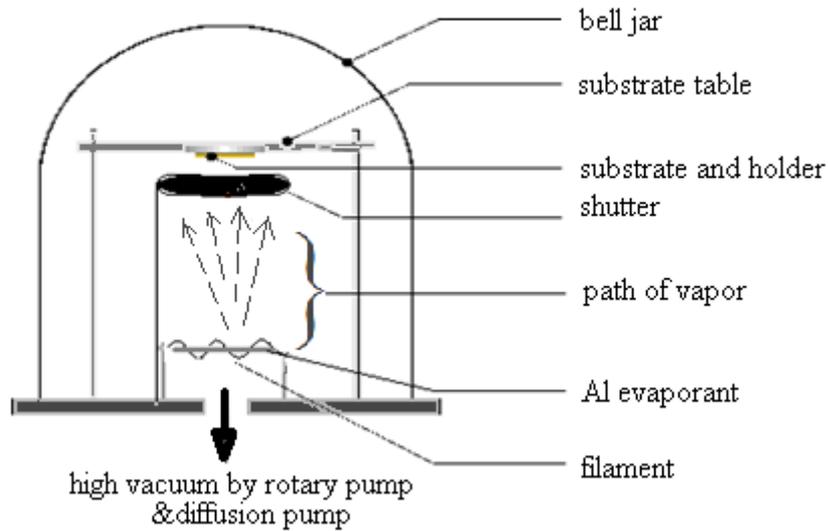
Figure 3.2: Schematic diagram of thermal evaporation system

3.1.3 Annealing in healing gas ambient:

Annealing is categorized in two parts according to the time of process. First one is annealing in nitrogen ambient, which will be referred as "annealing" and performed before the deposition of metal contact, i.e. before finalization of the fabrication. Annealing performed before device fabrication aims to heal the device structure and to form nanocrystals in structure. Annealing was performed at a range of 600-1100 °C.

The second one is annealing in hydrogen and nitrogen gas mixture and will be referred as "hydrogenation or metallization" and generally performed following deposition of metal contacts. Hydrogenation is a kind of healing process to fill dangling bonds and traps.

In this study, nitrogen annealing was performed in clean-room conditions under spectrum N_2 gas ambient. If not mentioned otherwise, all post-annealing processes were performed at 400 °C with 30% H_2+70% N_2 ambient for 20 minutes.

The detailed information on annealing conditions will be given during experimental parts on device fabrication in chapter 4 and chapter 5 because annealing temperature and is determined upon the desired device structure and functionality.

3.2   Instruments for Characterization

3.2.1   Structural Characterization

3.2.1.1 X-ray Photoelectron Spectroscopy (XPS): This non-destructive method is used for various purposes such as determining chemical states, composition and thickness of the oxide films, the transition layers and the empirical formula of the deposited thin films. Thus, ultra high vacuum condition is crucial for XPS measurements. XPS spectroscopy is also called as ESCA, which is the acronym for Electron Spectroscopy for Chemical Analysis.

This is a surface sensitive characterization technique. Probability of photoelectron collection exponentially decreases with an increase in thickness through a solid and it is given by the eqn.3.1 [67]. According to this equation, as the distance from the surface of desired layer on specimen surface increases, the photoelectron signal probability obtained from this layer decreases. Therefore, it is a useful measurement technique especially for investigating thin film coatings and it is considered to be especially useful for characterization of the top surface, from 1 to 10 nm thickness.

$$P(d) = exp\ (-d/l) \hspace{4cm} \text{eqn 3.1}$$

where l is inelastic mean free path of electrons in a solid and d is the distance of electron from surface.

Peak position of a photoelectron collected by an analyzer can be calculated using eqn.3.2 [67]. According to figure 3.3, electron is ejected from core level of atoms and by overcoming a work function specific to the solid, it becomes a free electron. Photon energy of X-ray source, $h\nu$, electronic charge, q, surface potential, ϕ, and work function of spectrometer, ϕ_S, are known parameters in this equation. Therefore, by measuring the kinetic energy of detached electron, binding energy (E_B) could be calculated from the formula as,

$$E_K = h\nu - E_B - \phi_S - q\phi \qquad \text{eqn 3.2}$$

By looking at this equation, it could be said that each element has a characteristic set of peak positions due to kinetic energy of ejected electron and its position in energy state. For Ge 2p peak position (E_B) is obtained about 1217.0 eV and 3d peak position is about 29.4 eV with instrument used for experiment in this work. Photoelectrons ejected from Ge 2p line are less energetic since they are inner core electrons and bonded more strictly. Therefore, their corresponding binding energies collected at higher energy side from eqn.3.2.

XPS technique gives a quantitative data for a thin surface analysis. For ultra thin samples, this is preferable but to analyze thicker samples it is a limiting factor. Due to this limitation, depth profiling characterization technique is added to the systems. Combining this property with XPS, it gains functionality and could be able to analyze thin films with any thickness. It only requires extensive amount of time.

This technique can be used for samples with intermediate layer formations. As discussed before, in our flash memory devices, it is important to control interfaces and their effects on device performance like flash memories. The

procedure of depth profiling technique is based on removing the film surface by sputtering technique and then continuing to collect data from the remaining part of the film. Thus, it is a destructive technique and used for samples that will not be used later.
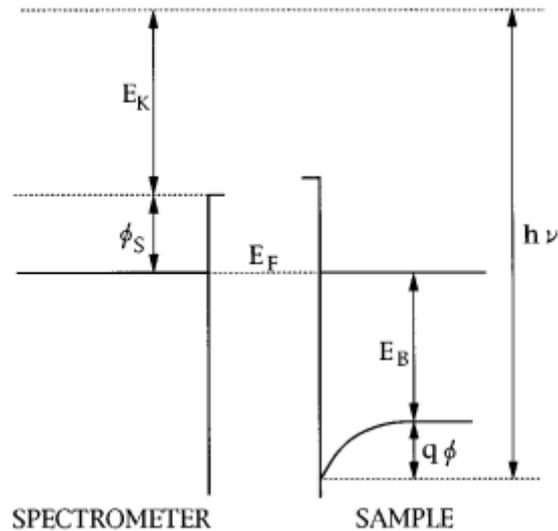
Figure 3.3: Energy band diagram for non-metal samples that is used to calculate peak position in XPS measurements [68].

With orbital angular momentum greater than zero, electrons could get two different angular momentum values. Peak position of these electrons with angular momentum greater than zero usually split into two separate positions. This is a result of spin-orbit coupling, which is the result of interaction between spin and orbital angular momentum. [69]

The main structural characterization technique used in this study was XPS. This method is fundamentally used to determine chemical composition and stoichiometry of transition layers (SiO_x, GeO_x) of film by the help of depth

profiling analysis. XPS measurements were done with SPECS EA-200 system, which is available in METU Central Laboratory, using an Al Kα x-ray source (hγ=1486.6 eV).

To determine chemical structure, background subtraction and peak fitting are required. PeakFit[TM] 4.12 and XPSPEAK41 are used to deconvolute each peak position in this study. Shirley method is used for background subtraction and to deconvolute peaks a combination of Lorenzian and Gaussian curve, which is called Voigt, is used. Detailed information on instrument and general view could be found elsewhere. [70-71]

3.2.1.2 Raman Spectroscopy: Photons directed onto a material does mostly not interact with the material. Most portion of the light is reflected back, some is transmitted and remaining part is absorbed and/or scattered, either elastically or inelastically. After elastic scattering, or Rayleigh scattering, photon leaves the sample without any interaction. However, a small number of photons (e.g. one photon in million) interacts inelastically with vibrating phonon modes. Photon frequency is subject to a change as a result of energy or momentum transfer in between photon and the lattice atom. This is called Raman Effect, named after the discovery of the effect by Indian physicist C. V. Raman in 1928. Change in energy either in higher energy direction, gaining energy which is Stokes shift or in lower energy direction, losing energy which is called Anti-Stokes shift. These scattering scenarios are shown in the schematic diagram in figure 3.4. Energy and momentum conservation rules given by eqn. 3.3 and eqn. 3.4 [72] are explaining the scattering processes.

$$\omega_s = \omega_i \pm \Omega \qquad\qquad\qquad\qquad \text{eqn 3.3}$$

$$q_s = q_i \pm \Lambda \qquad\qquad\qquad\qquad \text{eqn 3.4}$$

where ω_s and ω_i are the scattered and incoming photon frequencies and q_s and q_i are the wave-vectors of scattered and incoming photon, respectively. + sign and – sign are for Anti-stokes and Stokes shift, respectively.

Raman scattering gives information about polarization behavior of the material, lattice structure, impurities and free carriers in a semiconductor. For example; intensity of the peak can be used to have information about the crystallinity (the more crystallinity, the less disordered structure and so the less damping). First order Raman backscattering from crystal for certain direction gives only certain modes. In a crystal with diamond structure and in <100> direction, only longitudinal optic (LO) mode appears, transversal optical (TO) mode in <110> direction and both LO and TO modes appears in <111> direction.

Raman spectroscopy is a non-destructive and quantitative analysis. Light interacts with optical phonons and without damaging material structure, electron polarizability is observed in Raman Effect. Change in orbit after movement of nucleus in 10^{-14} s^{-1}, results with polarizability change. Since there is no relation of angle of detector with photon frequency and polarizability, it is fixed in configuration.
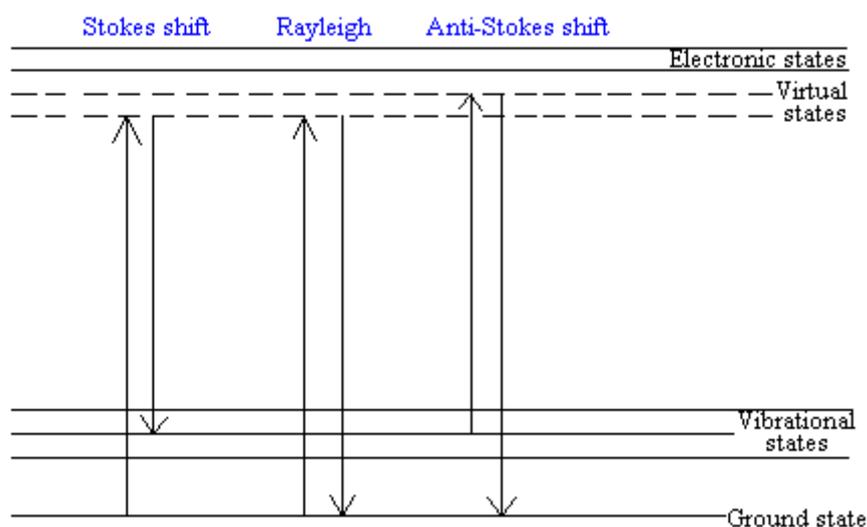
Figure 3.4: Schematic diagram representing scattering types, namely elastic (Rayleigh) scattering and inelastic (Stokes and Anti-Stokes) scattering.

Raman data are plotted as Raman intensity versus Raman shift, which is actually so called wave number. Energy difference of a photon is dependent on the wave number with the relation,

$$\Delta E = h\,\nu = h\,\frac{c}{\lambda} \qquad\qquad\qquad \text{eqn 3.5}$$

$$\overline{\nu} = \frac{\nu}{c} = \frac{c/\lambda}{c} = \frac{1}{\lambda}\ cm^{-1} \qquad\qquad\qquad \text{eqn 3.6}$$

$$\Delta E = hc\,\overline{\nu} \qquad\qquad\qquad \text{eqn 3.7}$$

where E is the photon energy, h is the Planck constant, λ is the wavelength of outgoing photon, $\overline{\nu}$ is the wave number and c is the velocity of light. When eqn 3.5 is inserted into eqn 3.6, final equation is obtained (eqn 3.7). It shows that there is a direct relation between energy and wave number. When h and c are

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inserted in this equation for one Raman shift, energy difference is calculated as 2.24×10^{-4} eV/molecule [73].

In this dissertation, Raman spectroscopy was used to analyze the crystalline structure of Ge floating layer in our memory devices. All measurements were conducted at room temperature in backscattering geometry using 632.8 nm light source of a conformal micro-Raman (HR800, Jobin Yvon) system. Raman system is located in the Department of Chemistry at METU, attached with Olympus microanalysis unit and a liquid-nitrogen-cooled CDD camera providing a resolution of ~1 cm^{-1}.

3.2.2 Electrical Characterization Instrument

3.2.2.1 Capacitance-Voltage (C-V) meter: In this dissertation for electrical characterization, Hewlett-Packard (HP) 4192A LF impedance analyzer (figure 3.5) is used to measure capacitance and conductance of MOS-type memory cells. This testing instrument is fully automatic and wide range in measurement techniques. Besides impedance parameters, gain, phase and group delay measurements are allowed to be done. Direct read-out can be provided by display units according to the selected measurement type. However, during experiments read out is done by computer control unit by using LabView codes. In this program, we are allowed to determine the voltage range and sweep voltage. In addition, frequency and oscillation level can also be controlled manually.

Equivalent circuit modes are served in three options; auto, series and parallel. Impedance, resistance and reactance are measured in series mode since they affect the circuit in serial mode. Admittance, conductance and susceptance are measured in parallel mode since they most generally affects the circuitry in parallel mode. More detailed information on testing instrument can be found elsewhere [74].

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Characterization of the memory devices was mostly done by capacitance measurements. Each data obtained with sweep range is plotted and analyzed according to the regions: accumulation, depletion and inversion, each of which were discussed in detail in chapter 1.3.

Device contact area was determined by evaporation to be 5.03×10^{-3} cm^2. Sharp gold probes were used during measurements in order to be sure that applied voltage was totally falling over the measured cell.

C-V characteristics of memory cells were investigated for five different sets of devices. By these measurements, charge density and equivalent oxide thickness (EOT) calculations were done.

The schematic of our set-up is as follows;
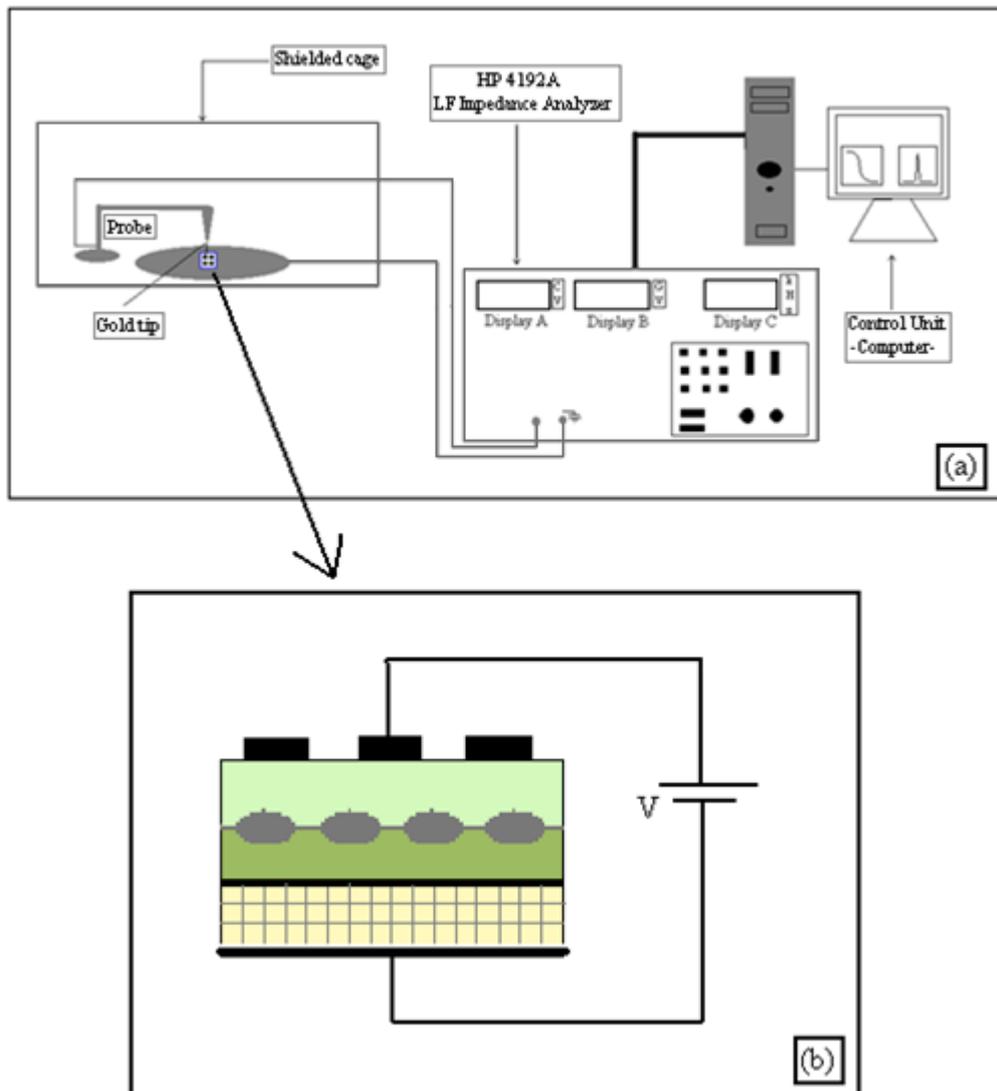
Figure 3.5: Schematic representation of HP 4192A impedance analyzer and measurement set-up (a) and a closer look at the device configuration and connection to the measurement set-up with nanocrystal floating gate in measurement system (b).

The front panel and block diagram of the LabView code control unit used for these measurements are given in figure 3.6 (a) and (b), respectively. Front panel shows two different graph charts. These show C-V and conductance-voltage graphs from left to right. The shown page of block diagram is the main cycle where data is processed, by reading output from characterization set-up and written into the graph and sending it to save in a file.
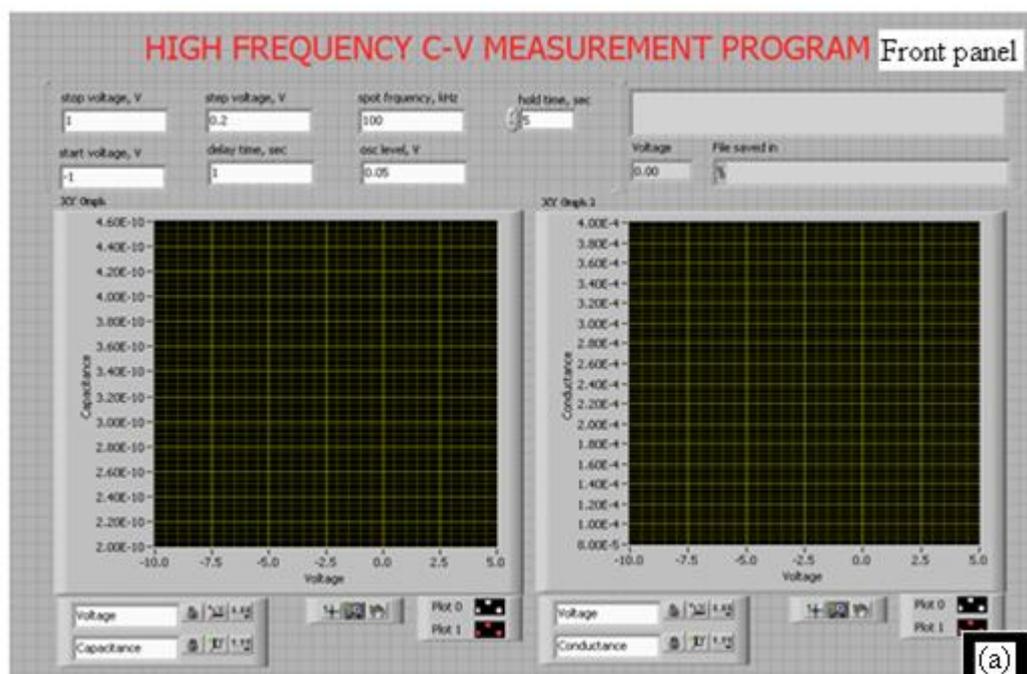
Figure 3.6: High frequency C-V measurement program; (a) front panel and (b) block diagram of LabView code used for C-V measurement.
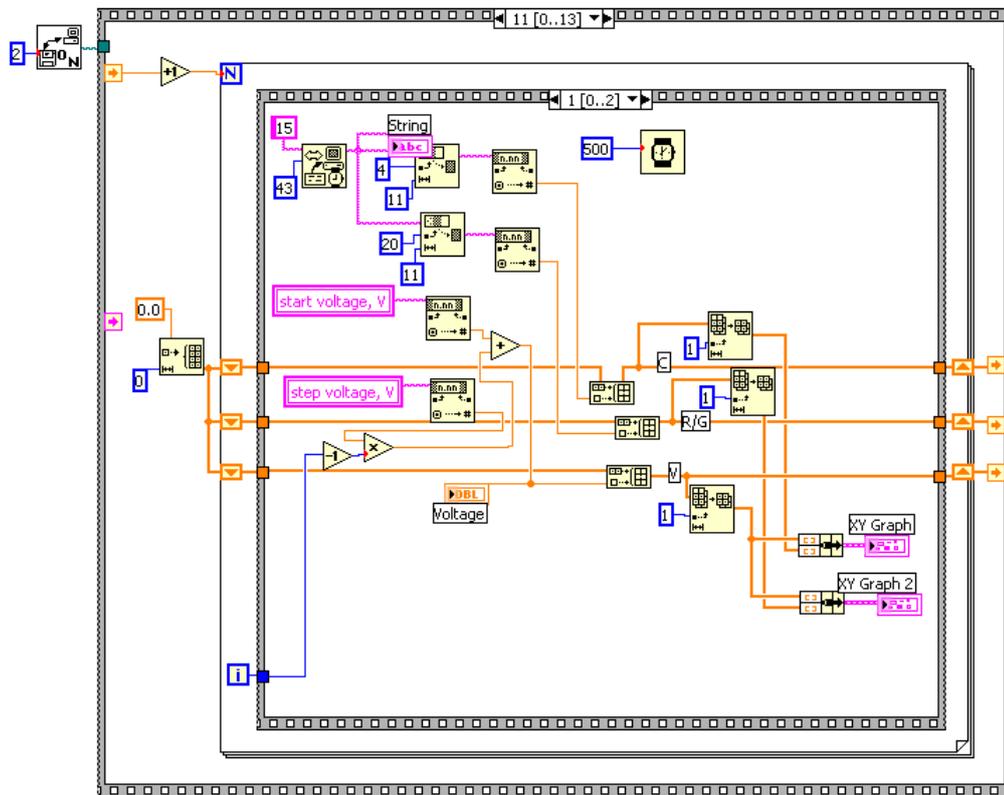
Figure 3.6: High frequency C-V measurement program; (a) front panel and (b) block diagram of LabView code used for C-V measurement (continued).

CHAPTER 4

EVOLUTION OF SiO$_2$/Ge/HfO$_2$/Si MULTILAYER STRUCTURE UNDER HIGH TEMPERATURE ANNEALING

4.1   INTRODUCTION

In this part of the study, SiO$_2$/Ge/HfO$_2$/Si multi-stack structure was studied to characterize chemical and structural properties of memory devices by spectroscopy techniques. Detailed analyses of the layers and their interfaces with each other were carried out by XPS in detail. In the following sections, first intended structure of the samples and their preparation methods are explained. Then, the results obtained from XPS depth profiling and Raman spectroscopy will be presented and discussed. Part of this chapter has been submitted to Thin Solid Film for publication [75].

4.2   SAMPLE PREPARATION

For this part of the study, five different sets of specimens were prepared as listed in table 4.1. Labels in table 4.1 has the following meanings: "a" represents the 1st set of prepared samples of wafer number 5, 2 or 21 while "b" represents the 2nd set of samples prepared from the same wafers. Different numbers in these labels (5, 2, 21) corresponds to different thickness of HfO$_2$. Sample 5 has ~10 nm thickness of HfO$_2$, sample 2 has ~15 nm and sample 21 has ~10 nm HfO$_2$ thicknesses, which were measured in MC2 laboratories at Chalmers University of Technology in Sweden using an ellipsometer.

Table 4.1: Thickness values of the HfO_2, Ge, Si and SiO_2 layers. Thickness of HfO_2 layer is measured by ellipsometry; Ge, Si and SiO_2 layers are measured by thickness monitor attached to the sputter system during deposition.

			Parameters					
Sample: Name		Sputter Layers in METU	Nitrogen annealing (°C/min)			RTA annealing (°C/min)		
Si	a5Si	8nmSi+15nmSiO₂	900 /30	1000 /30	1000 /60	900/5		1000/5
	b5Si	12nmSi+15nmSiO₂	900 /30	1000 /30	1000 /60	900/5		1000/5
Ge	a5Ge	8nmGe+15nmSiO₂	700 /30	800 /30	900 /30	700 /1	800 /1	900 /1
	b5Ge	12nmGe+15nmSiO₂	700 /30	800 /30	900 /30	700 /1	800 /1	900 /1
	a2Ge	2nmGe+15nmSiO₂	600 /30	700 /30	800 /30	600 /1	700 /1	800 /1

4.2.1 Fabrication of the Samples

Sample 5:

Sample 5 is a p-type Si <100> substrate grown by Czochralski process with a resistivity value of 1-10 ohm-cm and a doping density of 10^{15}-10^{16} cm^{-3}. Before the deposition of consequent layers, RCA cleaning was performed and it was followed by native oxide removal process using dilute HF solution.

SiO_2/Ge/HfO_2 stack layers were fabricated on p-type Si <100> substrates by sputter deposition technique. In this multilayer structure HfO_2 acts as the high-k dielectric tunnel oxide for the memory cell. HfO_2 film layer was grown by using sputtering technique in UHV conditions in MC2 laboratories at Chalmers University. Then, to fabricate MOS-type cell structure, floating gate and gate oxide productions were performed in Semiconductor Materials and Devices (SMD) group laboratories at METU by magnetron sputtering technique. This technique and the system were explained in detail in chapter 3.1.1. Ge/Si and SiO_2 layers were grown on HfO_2 films by magnetron sputtering at room temperature as floating gate and control dielectric, respectively.

SiO_2 was deposited as control oxide. During the fabrication of floating gate and the control oxide layers, substrates were not taken outside the deposition system. The structure of the Si/HfO_2/Ge/SiO_2 multi stack structure is schematically shown in figure 4.1.

Thickness measurements are summarized in table 4.2 for each stack of the structure. The thickness of the Ge and Si layers were measured to be ~8 nm for samples labeled with "a", and ~12 nm for samples labeled with "b". They all have the same thickness of SiO_2 as the control oxide and it was measured to be ~15 nm.

Base pressure of sputtering system before growth process was about 2x10^{-6} Torr for all set of samples. During the deposition the pressure raised to 7 mTorr and 3

mTorr with 50 W DC power with 20 sccm Ar flow for Si and Ge deposition, respectively. SiO_2 growth was conducted at 175 W RF power with 3 mTorr growth pressure and 20 sccm Ar flow. Fabrication processes were performed at room temperature. These parameters were kept constant for the other sets of the samples used in this part of the study.
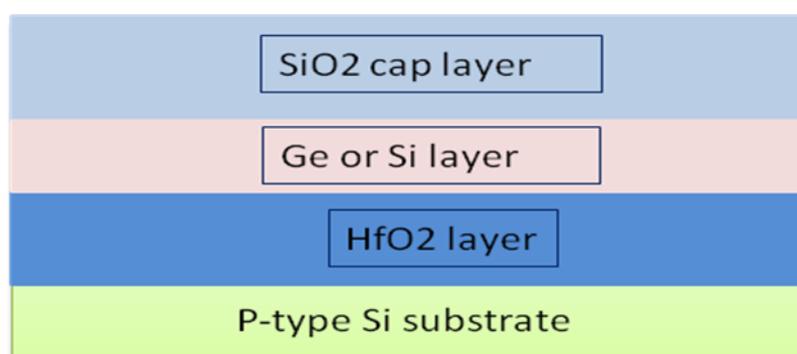
Figure 4.1: Schematic representation of SiO2/Ge(Si)/HfO2/Si multi layer structure.

Chemical structure and interfacial properties of a5Ge set were studied in detail by using XPS technique before and after heat treatment at 800 °C in N_2 ambient for 30 min in cleanroom conditions. For the depth profiling during the XPS measurements, more than 60 layers were sputtered for both as-sputtered and annealed samples with Ar ion gun, operating at 2500 eV. There was no detectable carbon contamination in the films following the removal of the first layer by Ar sputtering. Depth profiling was started after the removal of this layer. The XPS data were processed after background elimination, called Shirley background elimination technique, by using both PeakFit[TM] and XPSPEAK programs.

Sample 2:

$SiO_2/Ge/HfO_2$ structures with 15 nm HfO_2 high-k dielectric was fabricated on p-type Si <100> substrate with a doping density of 10^{15}-10^{16} cm^{-3} by sputtering technique under the same condition as sample 5. The only difference is the Ge layer thickness which was measured to be ~2-3 nm using thickness monitor of sputtering system. This set was also examined by Raman spectroscopy technique to see whether Ge-Ge bonds were formed. Electrical measurements performed on this sample set will be presented in the next chapter.

Table 4.2: HfO_2, Si (or Ge), SiO_2 control oxide layer thicknesses measured by ellipsometry (for HfO_2) and the thickness monitor (the rest).

Number of wafer	Name of samples	HfO_2 thickness (nm)	Ge or Si thickness (nm)	SiO_2 thickness (nm)
2	a2Ge	15	2-3 (Ge)	15
5	a5Ge	10	8 (Ge)	15
	b5Ge	10	12 (Ge)	15
	a5Si	10	8 (Si)	15
	b5Si	10	12 (Si)	15

4.3   CHARACTERIZATION

4.3.1   X-ray Photoemission Spectroscopy

Sample a5Ge with SiO_2/Ge/HfO_2/p-Si multilayer structure was analyzed using XPS depth profiling technique in more than 60 sputtering steps. Each sputtering step corresponds approximately to the removal of ~3-4 nm layers. The actual values vary for different materials and their micro structures. Figure 4.2 shows representative XPS spectra and deconvoluted peaks of Si, Ge and Hf and their chemical states at two different locations for the sample annealed at 800 °C in nitrogen ambient.

In figure 4.2 (a), the upper curve belongs to the Si 2p signal that is obtained from the Si substrate reached after 50 cycles of sputtering, whereas the lower curve is received from the top SiO_2 layer. These two signals measured at 99.2 eV and 103.7 eV corresponds to the typical Si and SiO_2 peak positions, respectively. There are no significant shifts observed at peak positions of Si and SiO_2. The small peak of lower curve seen at around 94 eV is the satellite peak of Si originated from ionization of X-ray photons with slightly higher energies.

Ge 3d signal displayed in figure 4.2 (b), exhibiting double peak features, is resulting from the pure Ge and the GeO_x state. After 20 sputtering cycles, Ge 3d peak is dominated by the pure Ge signal located at 29.3 eV and there is some signal coming from GeO_x at 31.6 eV. GeO_2 signal (at 33.7 eV) is detectable as approached to Ge/HfO_2 interface and when we approach further towards the Ge/HfO_2 interface, the binding energy peak corresponding to GeO_2 signal dominates over the pure Ge signal.
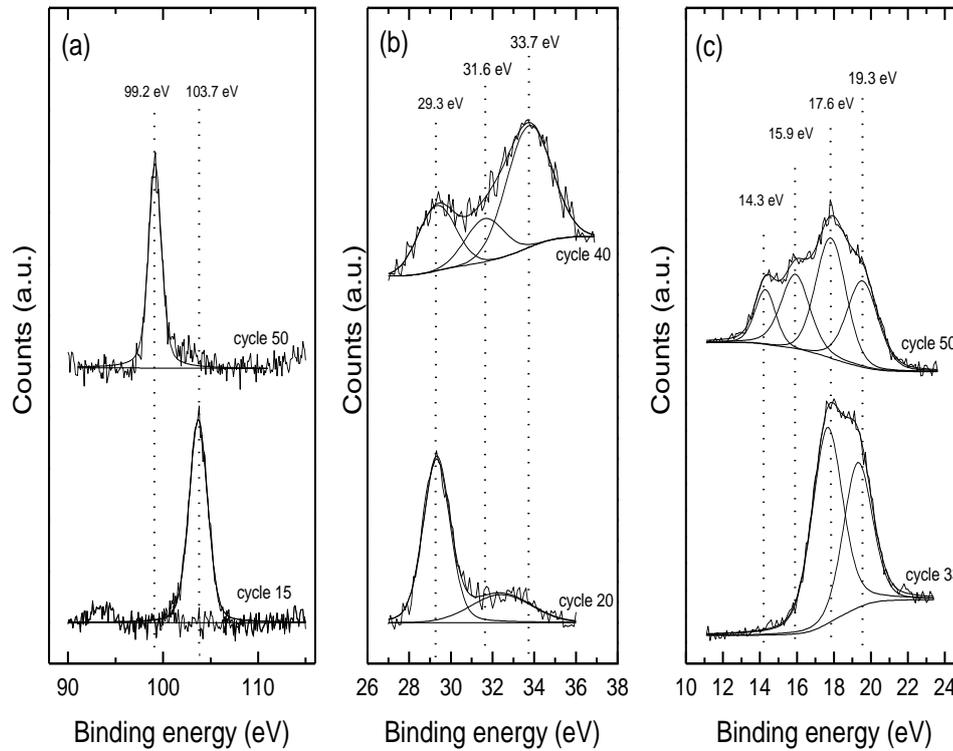
Figure 4.2: Representation of deconvolution process of XPS spectra of Si (a), Ge (b) and Hf (c) after annealing at 800 °C in N_2 ambient for ½ hour.

Hf 4f peaks are shown in figure 4.2 (c) in a similar way for two different layers with different chemical form of Hf molecule. Hf 4f signal is typically composed of two main peaks ($4f_{5/2}$ and $4f_{7/2}$), which is splitted due to spin-orbit interaction. After 26th sputtering cycle, Hf peaks corresponding to these spin states were measured with binding energies of 17.6 eV and 19.3 eV that can be assigned to the peak position of HfO_2 [76]. When we approach to the interface with the Si substrate, two additional peaks emerges at 15.9 eV and 14.3 eV (upper curve of figure 4.2 (c)). These two peaks appearing at the HfO_2/Si interface are resulted from HfSi/$HfSiO_x$ and Hf with low oxygen content. It should be mentioned that the presence of pure Hf metal, which might be in the form of local nanocluster,

or HfSi regions without any oxygen content since this cannot be excluded from the XPS signal alone as the peak position of these formation is hardly distinguishable [77-80].

Behavior of Ge at the interface of SiO_2/Ge and Ge/HfO_2 is of great interest because the electronic properties of these interface states, which play crucial role in the device operation, are mainly determined by the chemical formations in the structure. A complete analysis of Ge 3d peak across the multilayer structure is displayed with three dimensional graphs in figure 4.3 and figure 4.4, before and after the annealing processes, respectively. Presence of pure and oxidized Ge is clearly distinguishable in both figures. While GeO_x is observed only at the HfO_2/Ge interface of as fabricated sample, it is also seen at Ge/SiO_2 interface after annealing in nitrogen ambient at 800 °C. It appears that Ge atoms close to the Hf interface are oxidized during the deposition. It is likely that Ge atoms extract O atoms from the underlying HfO_2 film. The charge carrier should tunnel through the Ge/HfO_2 interface during the write/erase operation in a flash memory element and the presence of GeO_x influences the electronic barrier determining the tunneling process at the interface. Thus, formation of Ge oxide at the HfO_2/Ge interface should be taken into the account during the device design and analysis.
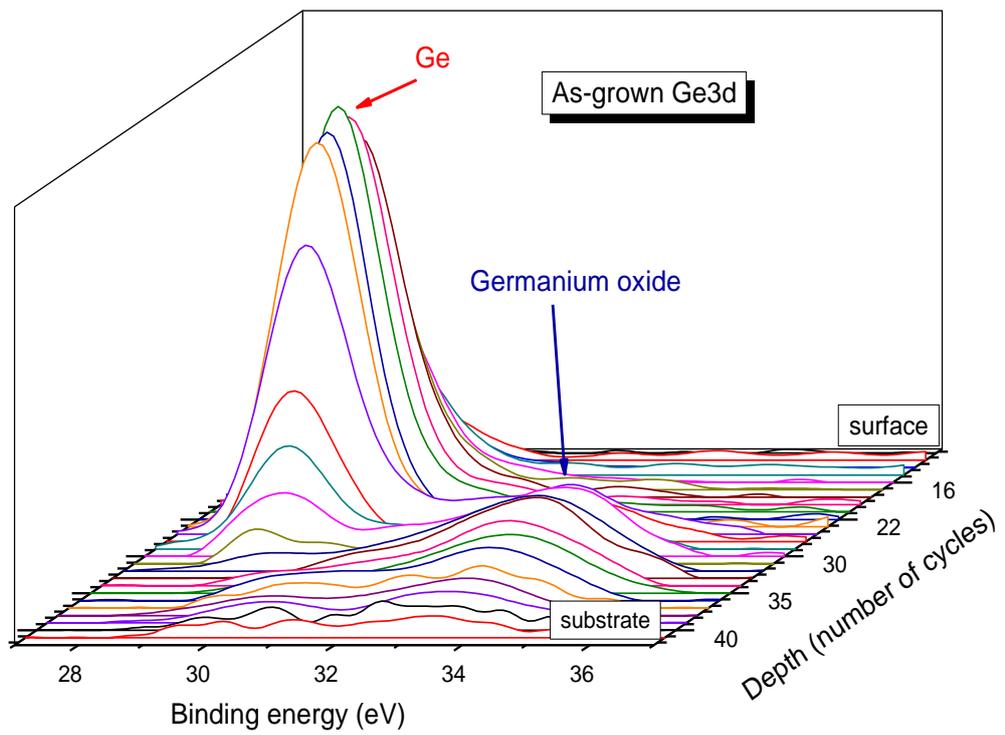
Figure 4.3: Smoothed data obtained from as-grown sample. Ge 3d peak positions beginning from cycle 12 to cycle 51. In this graph, Ge signal are started to collect after cycle 12 to cycle 40.
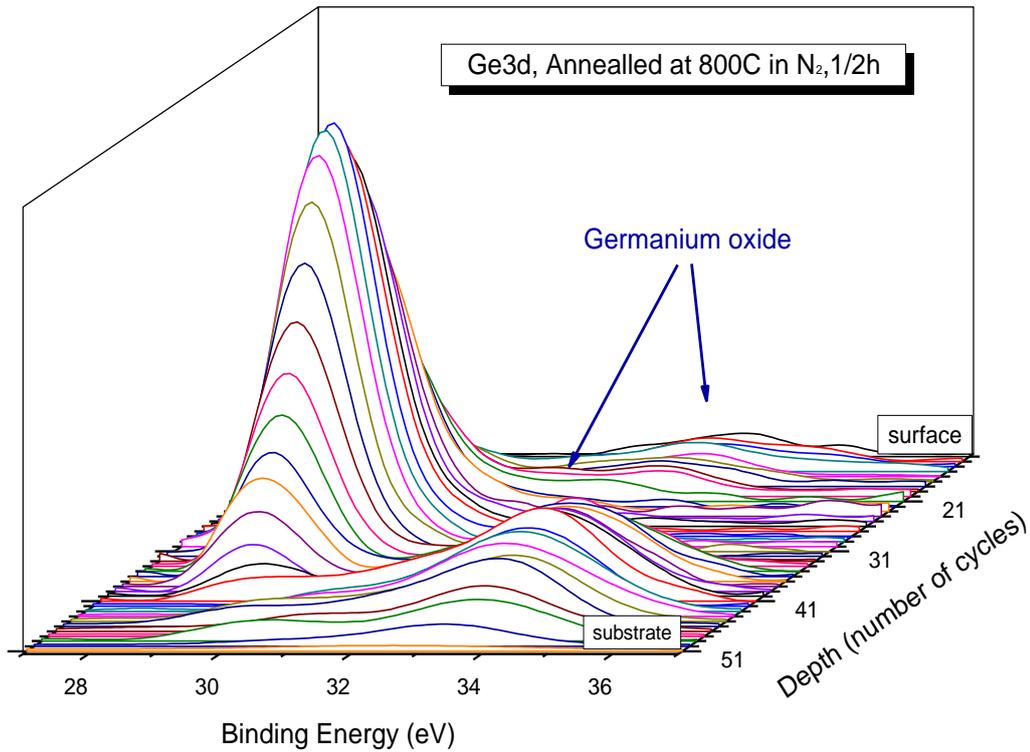
Figure 4.4: Smoothed data obtained from 800°C annealed Ge 3d peak positions in the same range of as fabricated sample.

Depth profiling of all elements across the stacked multilayer structure before and after annealing is shown in figure 4.5. Interfaces separated into 4 fundamental regions that are indicated in the figure. We see that the top SiO_2 layer formed by magnetron sputtering is almost stoichiometric and pure. Carbon contamination is observed at the very beginning surface layers only. HfO_2 film is seen to contain large amount of Ge before annealing. It seems that while Ge atoms penetrated into the underlying HfO_2 layer during the sputtering process, the annealing process greatly reduced the Ge amount in the HfO_2 film. The stoichiometry of the HfO_2 film is then healed by out diffusion of Ge atoms. The segregation of Ge from SiO_2 is a commonly observed phenomenon [81-82]. Similar behavior was

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also reported for Ge in the Al_2O_3 matrix [83]. We saw that Ge atoms behave in a similar way in HfO_2. This effect is apparently related to low solubility of Ge in the oxide materials.
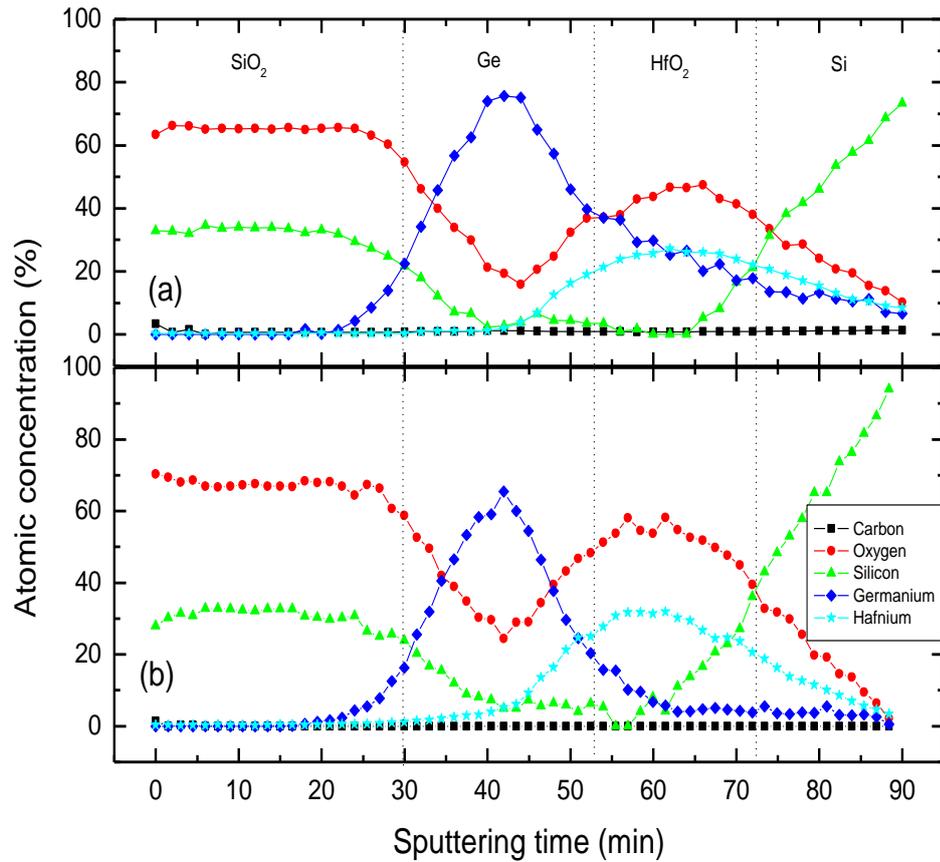
Figure 4.5: Depth profile spectra of $SiO_2/Ge/HfO_2/Si$ specimen for (a) as grown and (b) annealed in 800°C in highly pure nitrogen ambient.

In order to analyze the chemical state of constituting elements across the $SiO_2/Ge/HfO_2/Si$ stacked structure, binding energy values of Ge 3d and Hf 4f

were extracted by a careful deconvolution process, and given in figure 4.6. We also see from this figure how these chemical states changed during the annealing. In figure 4.6 (a) and (b), peak positions of Ge 3d and Hf 4f are shown, respectively. Binding energy values of Ge 3d peak positions were 29.3, 31.6 and 33.7 eV corresponding to Ge, GeO_x and GeO_2. The peak assigned to GeO_x could not be resolved any further due to the weak signal intensity. We see from figure 4.6 (a) that Ge was oxidized at the interface of HfO_2 even before the annealing process. It seems that Ge atoms oxidized with the oxygen atoms provided by the underlying HfO_2 layer during the sputtering. Upon annealing at 800 ^{o}C, the other side of the Ge film with SiO_2 interface oxidized, too. This oxidation took place due to oxygen atoms available in trace amounts in the annealing ambient even though the annealing was carried out in high purity nitrogen gas ambient under clean room conditions. We see however from figure 4.3, figure 4.4 and figure 4.6 (a) that a significant amount of pure Ge remained intact even after the annealing process at 800 ^{o}C.

The situation is more complicated for Hf, due to the presence of different phases and the spin splitting of the peaks. By using the deconvolution process described above, we were able to determine the chemical states shown in figure 4.6 (b) with some uncertainty. Figure 4.6 (b) suggests that even HfO_2 layer is mostly in the oxide form before annealing, some un-oxidized Hf atoms are detectable at HfO_2/Si interface. The peak measured at 17.6 eV corresponds to the fully stoichiometric HfO_2 $4f_{7/2}$ signal ($4f_{5/2}$ is 1.6eV larger than this value) while the slightly shifted value around 16 eV can be attributed to either HfSi or $HfSiO_x$. Previous publications on HfO_2/Si systems suggest the presence of both phases [80, 84]. As we measure a strong oxygen signal from the same region (not shown here), it is more likely that this part of the structure is composed of $HfSiO_x$ rather than HfSi. The relative intensities of HfO_2, HfSi/$HfSiO_x$, and Hf obtained after peak fit show that this region is highly dominated by HfO_2; although other chemical formations are present.
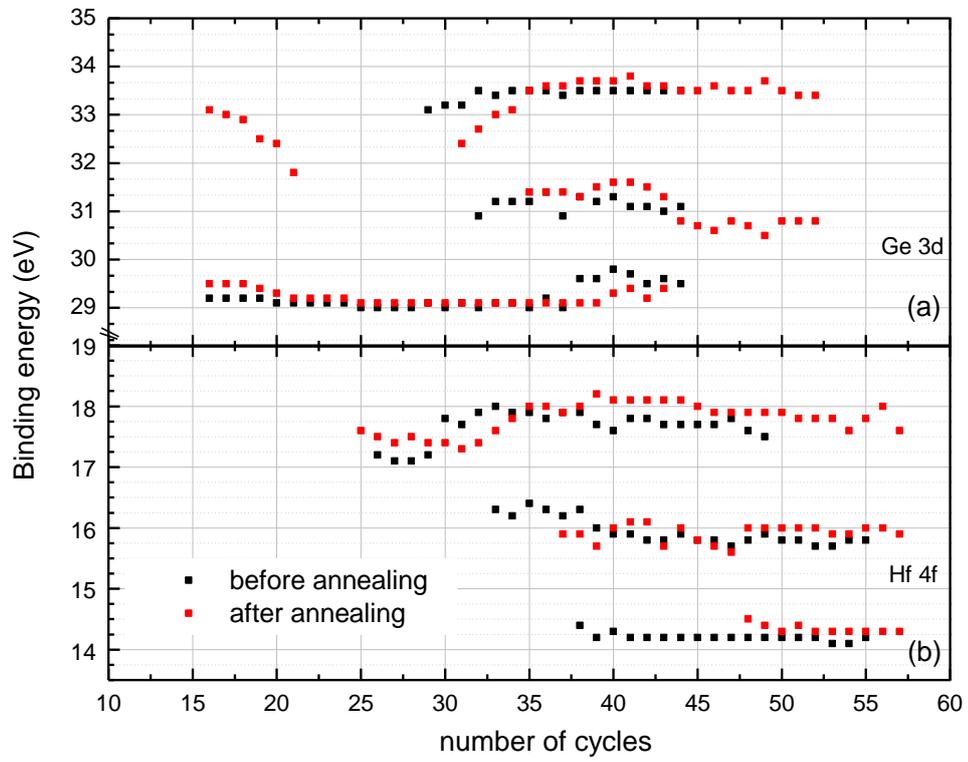
Figure 4.6: Peak positions of Ge (a) and Hf (b) before and after annealing processes.

4.3.2 Raman Spectroscopy

Being a complementary technique to XPS, we performed Raman spectroscopy measurements to identify the presence of Ge-Ge bonds and their evolution with the annealing for the sample called as "a5Ge". Figure 4.7 shows the Raman spectra for the as grown (control) and annealed samples. Annealing was conducted at various temperatures in N_2 ambient using 3 zone oven and in Ar ambient using rapid thermal annealing (RTA) technique.

As expected Ge-Ge peak located at 299.6 cm^{-1} emerged in the spectra after annealing at a variety of temperatures. It was observed that in N_2 ambient annealing, the peak intensity was its utmost value for the samples annealed at 700 °C, and decreases with increasing temperature. This is clearly a result of the increase in Ge oxidation with temperature. This result agrees very well with the XPS results (figure 4.3 and figure 4.4) for the 800 °C annealed samples where partial oxidation of Ge atoms is observed. However, as the annealing condition is changed from nitrogen oven to RTA system, since the annealing time decreases from 30 min to 1 min, signal coming from Ge-Ge bonding increases with temperature. In addition, RTA annealing for 1 min in Ar ambient enhanced the signal. This indicates that the crystallization takes time so high temperature treatment is required for a complete crystallization.

Another feature observed in the Raman spectra is the shoulder appeared at lower wave number side of the main peak of the annealed sample at 700 °C in nitrogen ambient for 30 min. A shift in the Raman peak towards the low wave numbers has been attributed to quantum size effect. The presence of such a shoulder can be assigned to nano-sized structures. In another study published from our group, it was showed that the size of Ge nanocrystals can be estimated from the asymmetric Ge peak [85]. The annealing temperature of 700 °C is lower end of the temperature range in which Ge crystallization occurs. Thus, it is expected that some regions of the film have been partially crystallized and film also have

nanocrystals rather than a continuous film. Consistently, we see that the shoulder disappear when the sample is annealed at higher temperatures. In addition, Ge signal disappears at 900 °C in N_2 ambient due to precipitation as well as oxidation at this temperature.

Figure 4.7: Raman spectra of as growth and annealed samples labeled as a5Ge at various temperatures in nitrogen ambient for 30 min and in RTA oven for 1 min.

In addition to this sample, Raman spectroscopic measurements were performed for the samples including thicker Ge layer denominated as b5Ge. The characteristic of the Ge-Ge bonding is almost same as plotted in figure 4.8. In nitrogen ambient, with increasing annealing temperature, signal obtained from

Ge atoms decreased as in the previous sample. However, at 800 °C there is an increase in signal. That can be attributed to that even oxidation of Ge occurs since this sample is thicker than the previous one, crystallization of Ge layer is highly observable. In addition, RTA annealing for 1 min in Ar ambient enhanced the Raman signal.
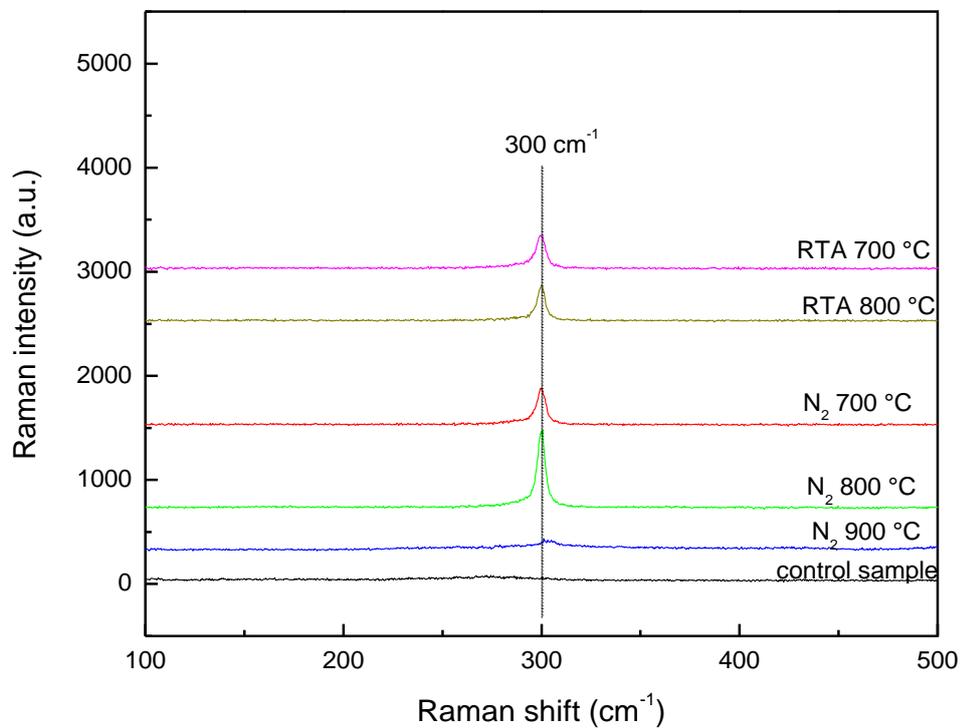
Figure 4.8: Raman spectra of as grown and annealed samples labeled as b5Ge at various temperatures in nitrogen ambient for 30 min and in RTA oven for 1 min.

In order to form nanocrystals instead of a continuous Ge film, we prepared a new sample set with thinner Ge film. This set is called as a2Ge and was grown with only difference of estimated thickness of Ge that is about 2-3 nm in

thickness. Raman results obtained from this sample are shown in figure 4.9. The peak located about 521 cm^{-1} is generated by the Si substrate and the peak seen at 300 cm^{-1} is by the Ge layer [86-87]. When compared with the signal obtained in previous samples, we see that the intensity decreased significantly. This is a result of less Ge content of the structure. More importantly we see a shoulder at the lower wave number side of the Ge signal, indicating the quantum size effect. This is a strong sign of the nanocrystal formation at the interface.

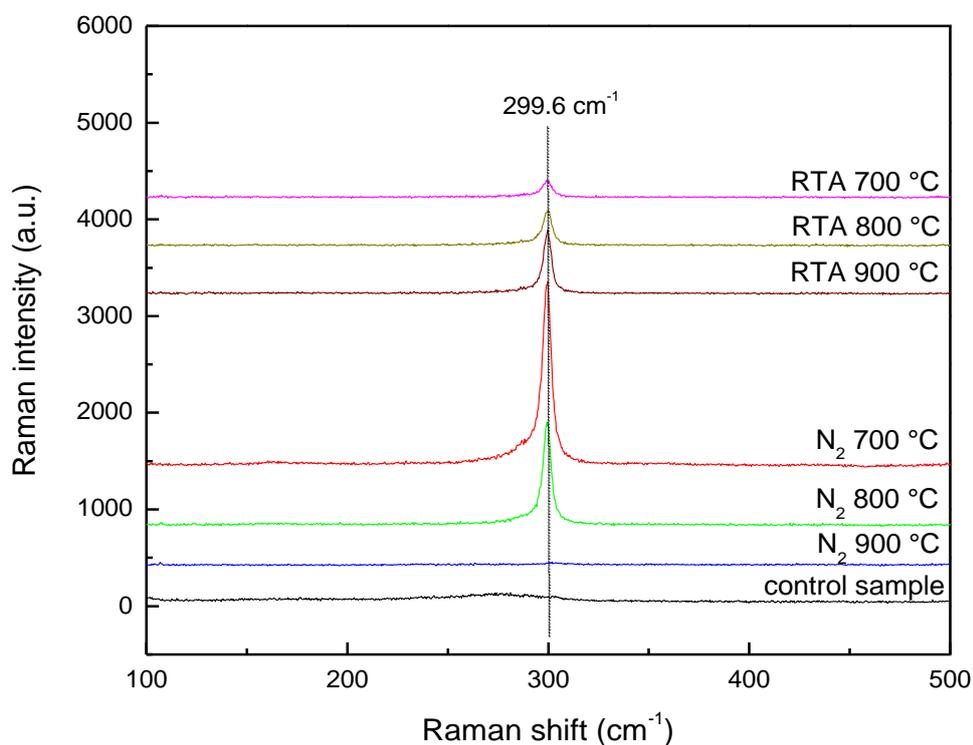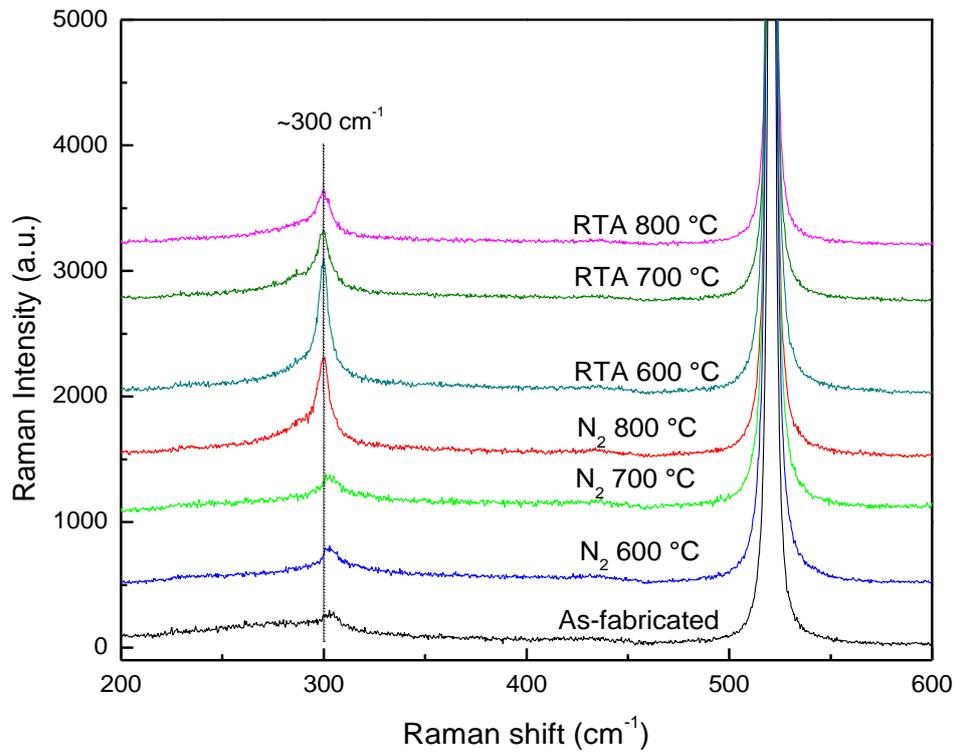
Figure 4.9: Raman spectra of as grown and annealed samples labeled as a2Ge at various temperatures in nitrogen ambient for 30 min and in RTA oven for 1 min.

CHAPTER 5

FABRICATION AND ELECTRICAL CHARACTERIZATION OF TRILAYER MEMORY CELLS WITH HfO$_2$ AS TUNNEL OXIDE

5.1   Introduction

In this chapter, electrical characterization of MOS devices made of SiO$_2$/Ge(Si)/HfO$_2$/Si stacked layers have been presented. Results obtained both from Si based and Ge based devices are discussed with a perspective towards flash memory applications. As described in the introduction chapters, flash memory cells are traditionally fabricated by using poly-Si floating gate embedded in SiO$_2$. In this work, we have studied two major modifications to this traditional structure; first one is the use of high-k dielectric tunnel oxide instead of SiO$_2$, the second one is the use of Ge nanocrystals instead of poly floating gate. These new structures have been fabricated and their memory behaviors have been measured. Continuous layer memory structures were not compatible with the state of the art memory devices. However, our results were promising for nanocrystal floating gate memory structures.

5.2   Sample Preparation

Samples were prepared on both p-type and n-type substrate using magnetron sputtering deposition technique. Both p-type and n-type Si <100> substrates were grown by Czochralski process with a resistivity value of 1-10 ohm-cm. Doping density of p-type and n-type substrates were in the range of 10^{15}-10^{16} cm^{-3} and $3x10^{14}$-$5x10^{15}$ cm^{-3}, respectively. Growth parameters such as thickness of tunnel oxides, floating gates and top oxides are given in table 5.1. For all

sample sets, control samples with as-grown layers were prepared to compare the effect of process parameters such as annealing and metallization. Samples with number 1, 2, 5 and 13 have been analyzed. Samples of 1, 2a and 13 have very thin SiO_2 layer at the interface of HfO_2 tunnel oxide and Si floating gate thin film. For samples 2b and 5, different types of floating gate were used, Ge, as well as removing SiO_2 interspaced layer. Ge including samples on sample 5 was analyzed also by XPS in detail.

Table 5.1: Prepared set of samples for electrical characterization

Name	Structure (nm)	Annealing temperatures/Ambient and time (°C/ min)		
1	25nm HfO_2 +3nm SiO_2 +5nm Si +20nm SiO_2	950/ In N_2 60 min	1000/ In N_2 60min	1100/ In N_2 60 min
2a	15nm HfO_2 +3nm SiO_2 +5nm Si +20nm SiO_2	---	---	1100/ In N_2 60 min
2b	15nm HfO_2 +2.5nm Ge+ 15nm SiO_2	600/ In N_2 30 min In Ar 1 min	700/ In N_2 30min In Ar 1 min	800/ In N_2 30 min In Ar 1 min
a5Ge	10nm HfO_2 +8nm Ge+ 15nm SiO_2	700/ In N_2 30 min In Ar 1 min	800/ In N_2 30min In Ar 1 min	900/ In N_2 30 min In Ar 1 min
13	25nm HfO_2 +3nm SiO_2 +5nm Si +20nm SiO_2	950/ In N_2 60 min	1000/ In N_2 60min	1100/ In N_2 60 min

C-V characteristics of samples have been presented in this chapter. They are categorized according to the variation on the multilayer structures. First, C-V analysis of SiO_2/Si/SiO_2/HfO_2/Si-substrate multilayer structure is explained.

Secondly, results on $SiO_2/Ge/HfO_2/Si$ structure with thick Ge floating gate are reported. Finally, studies on $SiO_2/Ge/HfO_2/Si$ with nanocrystal Ge floating gate are presented and discussed.

5.3   Capacitance-Voltage Characterization

5.3.1   Electrical Performance of MOS Structure with $SiO_2/Si/SiO_2/HfO_2/Si$ Multilayer

The structure of the device studied in this part is shown in figure 5.1. It should be noted that a thin SiO_2 layer is used above the HfO_2 layer to improve the device performance. This layer is measured to be ~3 nm using thickness monitor of the deposition system. In this group of samples, substrates numbered as 1, 2 and 13 have been used. Samples called as 1 and 2 have been grown on p-type Si substrate while sample 13 is grown on n-type substrate.
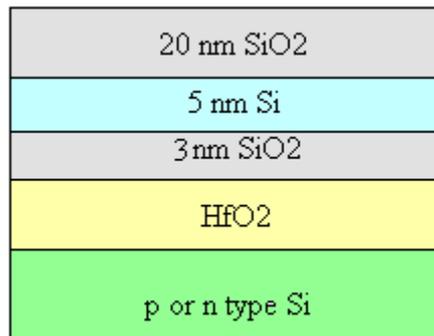
Figure   5.1:   Schematic   representation   of   MOS   structure   with $SiO_2/Si/HfO_2/SiO_2/Si$ multilayer. HfO_2 thickness is 25 nm for samples with number 1 and 13 and 15 nm for sample with number 2.

Growth parameters are the same for the samples used into this part. RF power of SiO$_2$ growth is 175 watt and DC power of Si is 50 W. Plasma is formed using Ar gas with growth pressures listed in table 5.2.

Table 5.2: Sputter growth parameters for samples of SiO$_2$/Si/SiO$_2$/HfO$_2$/Si

Material deposited	Power	Atmosphere	Growth Pressure
SiO$_2$	175 W RF	Ar	3 mTorr
Si	50 W DC	Ar	7 mTorr

A control sample with only HfO$_2$ tunnel oxide is prepared to test the quality of HfO$_2$ tunnel oxide and to obtain a basis for the comparison in the subsequent measurements. The C-V characteristics of sample 1 are plotted in figure 5.2. We see that before the fabrication of memory cell structure, Si/HfO$_2$ sample shows a clockwise-hysteresis and flat-band voltage is nearly at zero voltage at 500 kHz. Thus, the hysteresis occurs most probably due to mobile charges at the interface. After fabrication of memory cell structure, there has been about 2.7 V shift towards positive voltage. This indicates accumulation of negative charges in the dielectric. Counter-clockwise hysteresis has been observed as well, due to electron charging. In this memory construction, capacitance characteristic is improved after the construction of memory element fully. Hysteresis about 1.9 V has been measured before annealing. After annealing in nitrogen ambient for 1 hour at 1100 °C, device structural characteristic as well as charging capacity has been improved. Amount of stored electronic charge extracted from the C-V curve is calculated as 1.3×10^{11} cm^{-2} and 4.0×10^{11} cm^{-2} before and after the annealing, respectively.

Figure 5.2: High frequency (500 kHz) characteristics of sample set 1, control sample before memory device production (a), control sample after fabrication of memory structure (b) and annealing at 1100 °C (c).

For sample 2, control sample with only 15 nm HfO_2 tunnel oxide was prepared. HfO_2 thickness of sample 2 is thinner than sample 1 but leakage current has not been observed for this sample, too. We have observed strong effect of hydrogen annealing in this sample set. It is generally known that there are dangling bonds in such structures and these can be improved by hydrogen annealing. As can be seen from figure 5.3, both control sample and the sample with memory structure exhibit unexpected C–V behavior. In the depletion region of these samples, C-V curve starts showing typical behavior at voltages close to the flat band values. However, for higher voltages, C-V tends to saturate unexpectedly at capacitance

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values higher than the expected values. This is indication of very high interface state density which pins the Fermi level in the band gap. Hydrogen annealing resulted in release of Fermi level from the trap states and brought the C-V curve to their normal behavior by passivating the trap states by bindings of hydrogen bonds. We also observed expected hysteresis in the C-V curves after hydrogen annealing. However, in this case, we observed the hysteresis and charge trapping in both structures with and without nanocrystals. This is an indication of high interface trap density even in the sample with HfO_2 only. The effect of dynamic interface traps can easily be seen from asymmetric shape of the shift in the C-V curve of this sample. On the other hand the sample with memory structure after annealing exhibit a parallel shift as it should be in the case of normal memory operation. Effective charge density after hydrogenation is calculated to be n= $1.3x10^{11}$ cm^{-2} in this memory structure.
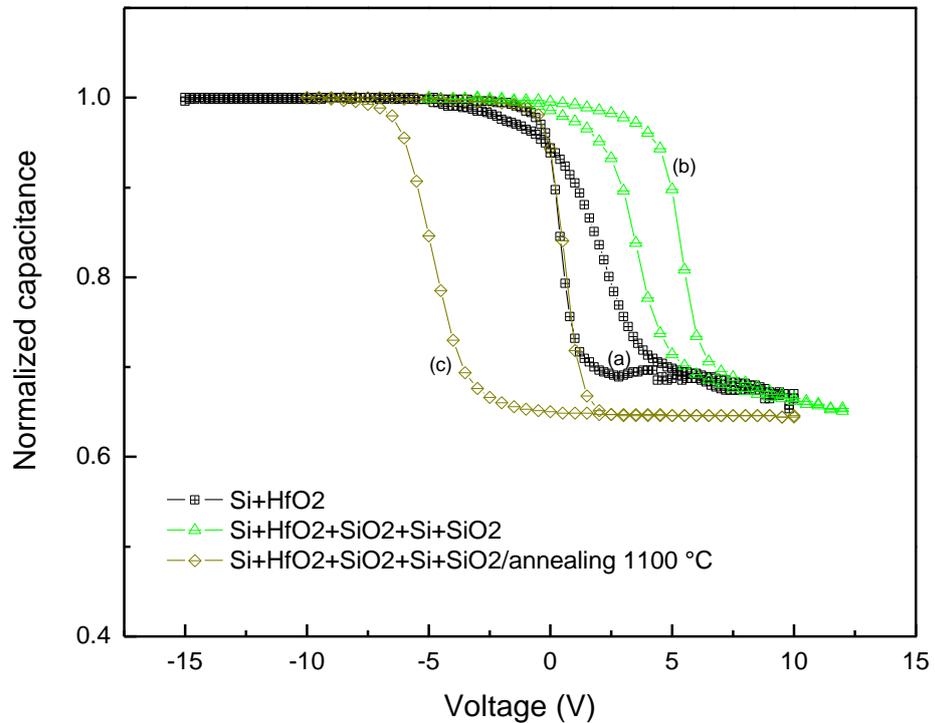
Figure 5.3: High frequency (1MHz) characteristics of sample set 2, control sample before memory device production (a), control sample with hydrogen annealing (b), memory structure fabricated and annealed at 1100 °C (c) and hydrogenated in %30 H_2 and %70 N_2 ambient 1100 °C (d).

In addition to p-type substrate based memory cell structures, memory elements were fabricated on n-type substrate with 25 nm HfO_2 tunnel oxide thickness. These samples were studied with C-V measurements and compared with sample 1 with the same HfO_2 thickness. It is observed that the sample without memory structure has large amount of oxide charges which caused a large shift in the negative direction (see figure 5.4 a). It is interesting to note that we observe no hysteresis in this sample. The absence of hysteresis indicates that charge/discharge process does not take place in this sample. Or if it does, it is

not observable due to the presence of huge positive charges present in the oxide, which caused the observed shift shown in figure 5.4 (b). Upon annealing under hydrogen atmosphere, the C-V curve shifts to its expected position, indicating that hydrogen annealing repaired the sample by passivating the trap states (figure 5.4 (b)). In addition, we observe a hysteresis after the hydrogen annealing. This hysteresis is a result of charging/discharging of charge trap states. It is likely that this behavior has become observable only after removing other sites by hydrogen annealing. After $HfO_2/SiO_2/Si/SiO_2$ multi structure is grown, capacitance shows a clockwise hysteresis with 1.5 V voltage shift as shown in figure 5.4 (c). This curve is showing typical memory behavior with a parallel shift in the C-V curve. In addition, the inversion region capacitance has been lowered to the expected values, showing that the device quality has improved after the fabrication of memory structure. This sample is further annealed in N_2 at 1100 °C for 1 h. In contrast to the p-type samples, C-V characteristic is totally destroyed after this high temperature annealing. It is likely that such a high temperature annealing has induced some unwanted reactions and/or mixing at the interface. This might be due to the dopant (phosphorous) in the n-type substrate. This explains why we have not see any such effect in the p-type samples.
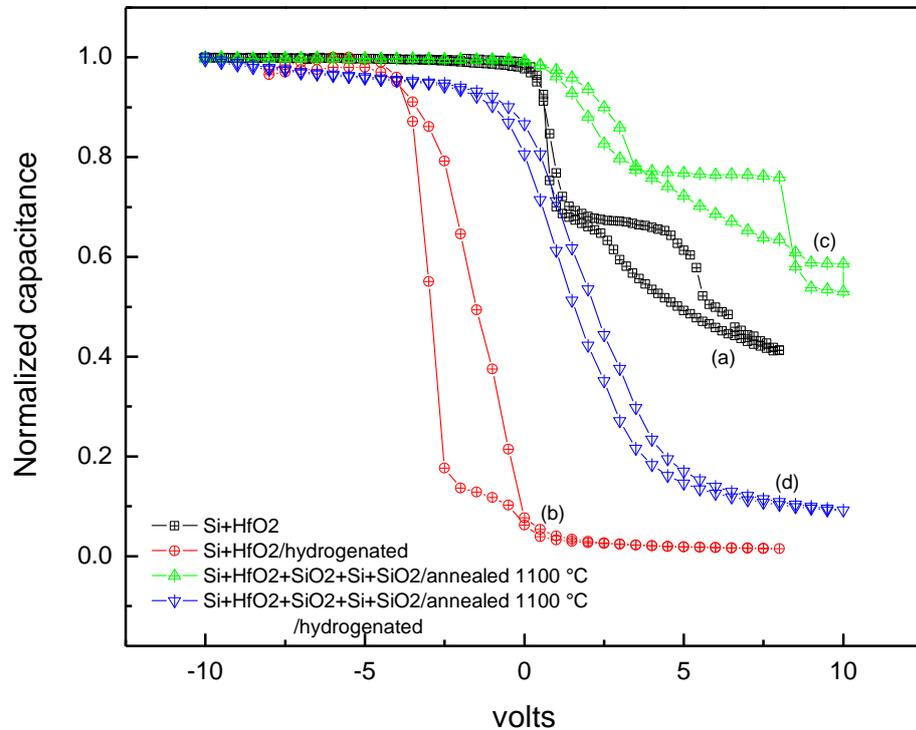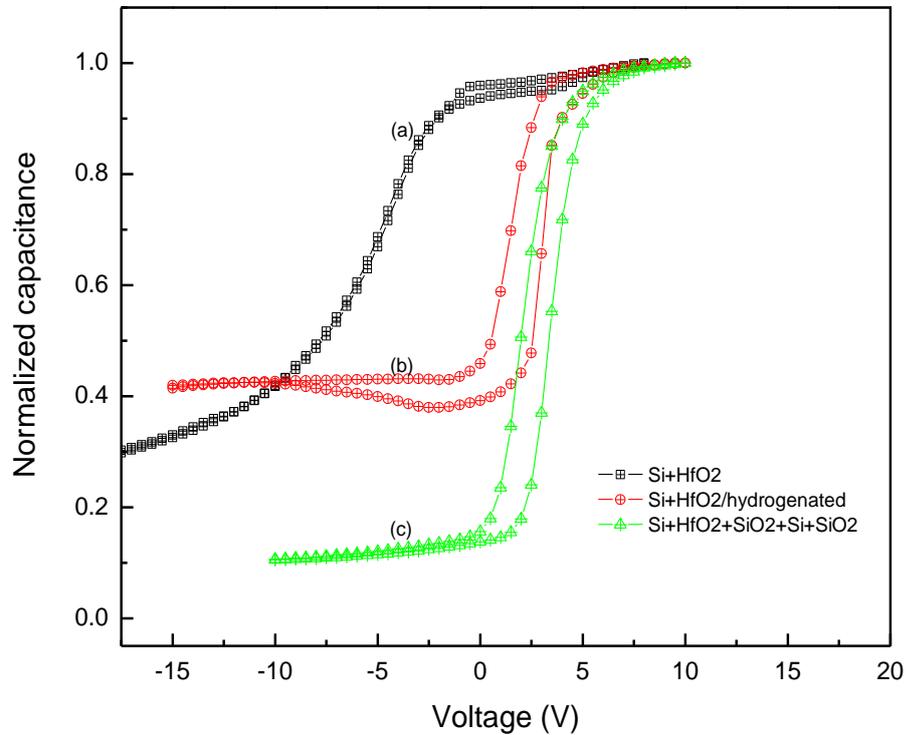
Figure 5.4: High frequency (1MHz) characteristics of sample set 13 (n-type), control sample before memory device production (a), hydrogenated control sample before memory cell production (b), control sample after fabrication of memory structure (c).

The effect of illumination in visible range on the C-V behavior is also studied with a regular light to see if there is any light induced effect in the memory operation. 100 kHz frequency response under illumination of sample 13 is plotted in figure 5.5 and it is observed that the depletion region of the C-V curve is not affected by the illumination. So the memory element remains intact during charging and discharging operation. The only effect of light illumination is seen in the inversion part of the C-V as an increase in the number of minority charges leading to higher capacitance values.
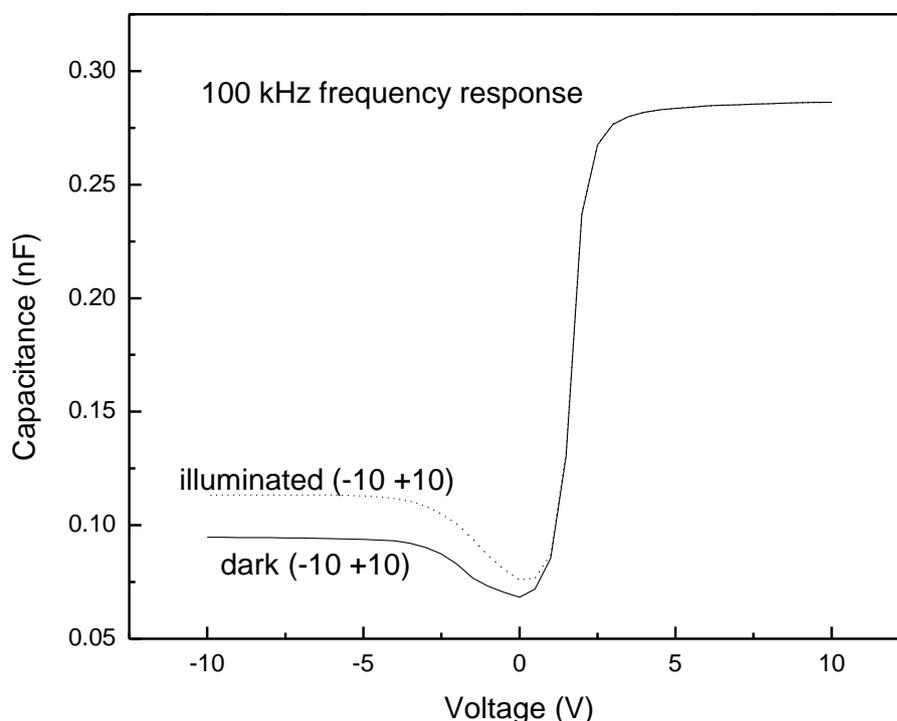
Figure 5.5: Effect of illumination on memory cell response.

Since the sample 1 has shown best memory behavior, we have further investigated this sample. Figure 5.6 shows the frequency dependence of sample 1. We see that the low frequency (10 kHz) behaviour is different than high frequency behaviour. Hysteresis is in clockwise direction for all cases due to electron injection. At lower frequencies, we have observed larger flat band shift due to the larger charge storage than high frequency cases. It seems that electron injection to the floating gate is more effective at low frequencies. Charge density calculated from C-V graph is at 10 kHz and 1 MHz as 3.4×10^{11} cm^{-2} and 1.5×10^{11} cm^{-2}, respectively. This is due to the fact that electrons are minority carriers in p-type samples and they cannot follow the signal at high frequency régime.
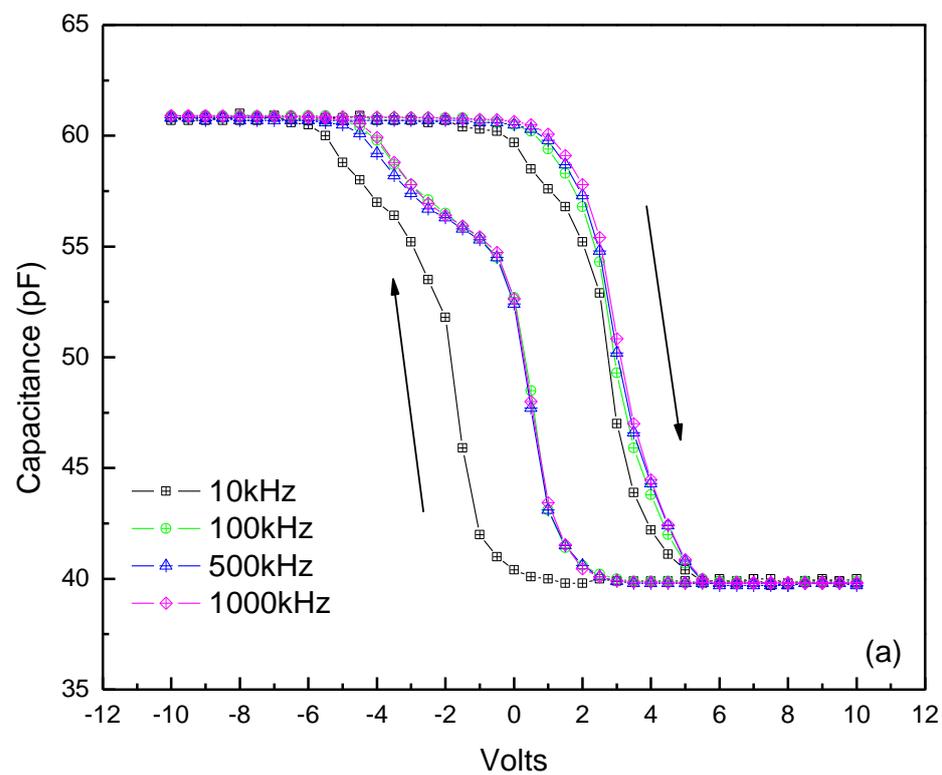
Figure 5.6: Capacitance (a) and conductance (b) plots of sample 1, annealed in nitrogen ambient for 1 hour at 1000 °C.
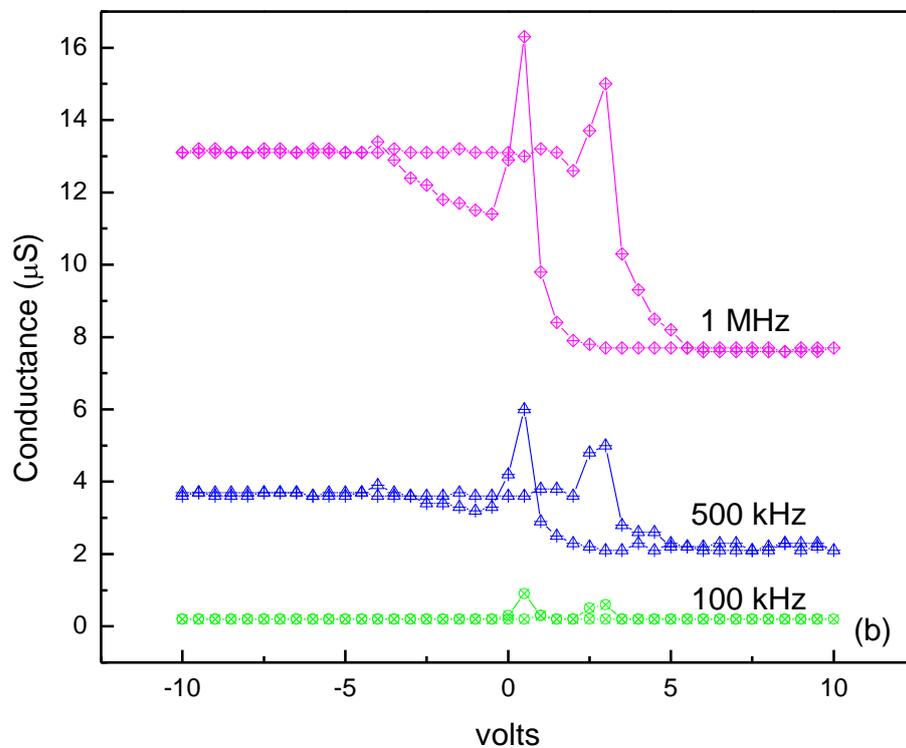
Figure 5.6: Capacitance (a) and conductance (b) plots of sample 1 annealed in nitrogen ambient for 1 hour at 1000 °C (continued).

After hydrogen annealing at 400 °C in %30 H_2 + %70 N_2 atmosphere for 10 minutes, clockwise hysteresis curve is improved as shown in figure 5.7 at 100 kHz. This shows that, hysteresis is not mainly resulting from interface states instead it is resulted from the charge carriers injected into the floating gate. The density of charge is calculated to be 2.5×10^{11} cm^{-2}.
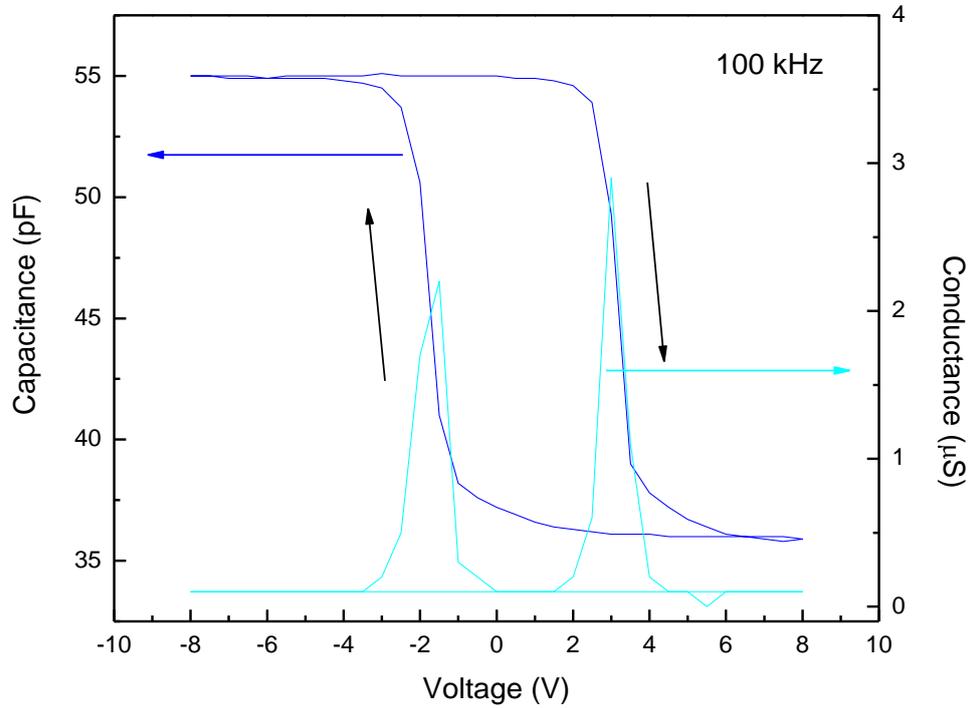
Figure 5.7: C-V curve of sample 1 annealed at 1000 °C for 1 h in N_2 ambient and then hydrogen annealing performed at 400 °C for 10 min in %30 H_2+%70 N_2 ambient.

5.3.2 Electrical Performance of Ge Floating Gate in SiO_2/Ge/HfO_2/Si Structure

In this section the result of memory structures with Ge is presented. The structure of the device used in this part of the study is shown in figure 5.8. The sample a5Ge has 10 nm HfO_2 tunnel oxides and 15 nm SiO_2 top oxide. In between, Ge semiconductor thin layers are fabricated. It was measured to be ~8 nm with thickness monitor installed in sputtering system. Although the intension has been to create a nanocrystalline layer, it appears from various measurements that this sample has a continuous Ge thin film layer. Such a structure is valuable

form of the memory application point of view. It corresponds to traditional structure with Ge floating gate and HfO$_2$ high-k dielectric.

| 15 nm SiO2 |
| 8 nm Ge |
| 10 nm HfO2 |
| p type Si |
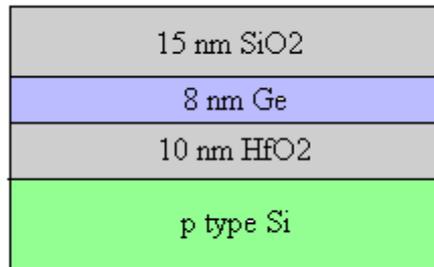
Figure 5.8: Schematic representation of MOS structure with SiO$_2$/Ge/HfO$_2$/ Si multilayer structure.

The C-V curves of the sample called a5Ge, which is annealed in RTA oven at 700 °C and 800 °C, are plotted in figure 5.9. We see very small hysteresis in both cases indicating that it does not have the ability to hold charges. This can be easily understood when we consider the structure of the device. It has been shown in the previous chapter that this sample has a continuous Ge layer instead of discrete nanocrystals. A continuous layer which is extending from one side of the sample to the other side cannot hold the charge pocket under the gate electrode. Instead, carriers are spread across the wafer if they are not injected back to the substrate at some leaky point. However, at 800 °C, the charge storage is improved due to the repair of the defect states, causing back injection of the carriers. This can be resulted from the oxidation of Ge because of the decrease in Ge thickness. As we will see in the next section charge storage will be improved by using nanostructures instead of continuous film.

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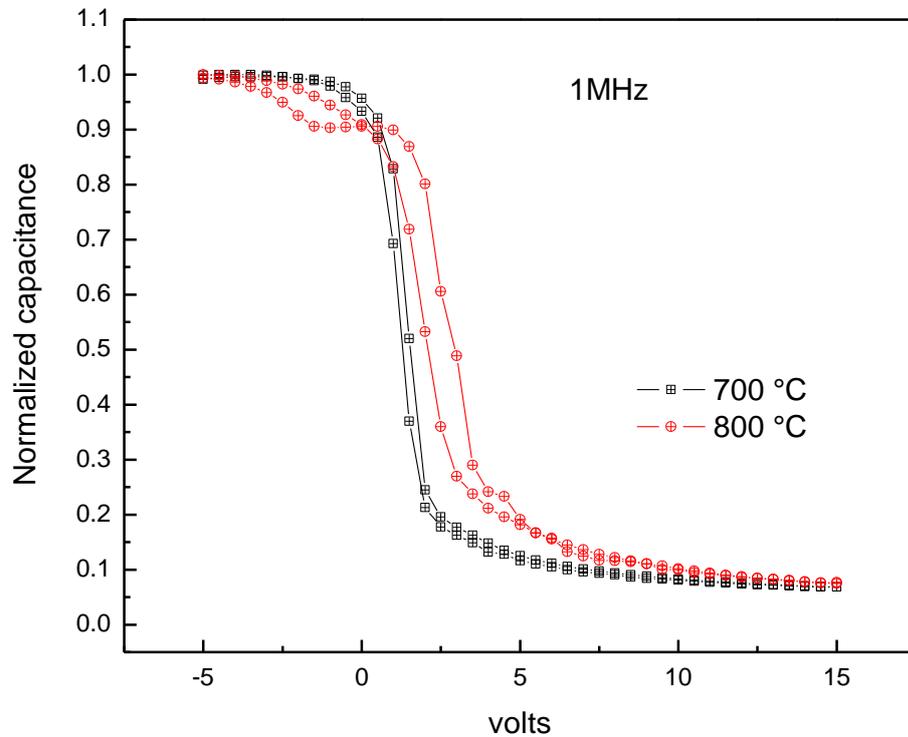
Figure 5.9: High frequency response of sample denominated as a5Ge at two different temperatures.

5.3.3 Electrical Performance of Ge nanocrystals embedded in HfO$_2$ Tunnel Oxide and SiO$_2$ Control Oxide

In the third group samples (called 2b) we have introduced a Ge layer which is thin enough to create Ge nanocrystals. Schematic of the device in this group is shown in figure 5.10. Initial Ge layer thickness was measured to be ~2.5 nm for sample 2b. The results of C-V are given in figure 5.11. Capacitance response is measured with 1 MHz frequency. In this figure, we have seen that the charge storage improves gradually with annealing. We have obtained the best storage in the sample annealed at 800 °C with RTA.
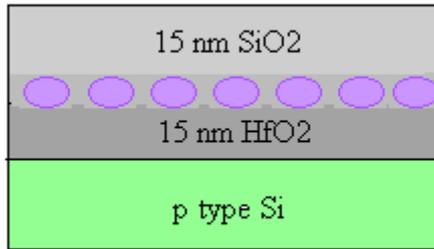
Figure 5.10: Schematic representation of MOS type structure with SiO_2/nc-Ge/HfO_2/Si multilayer structure.

Charge density is calculated as $n=2.93 \times 10^{12}$ cm^{-2} and EOT is as $d_{EOT}= 74.82$ nm from the plot for this sample that is annealed for 1 min by RTA at 800 °C.

Another interesting effect is observed when we annealed the same sample under N_2 atmosphere. We see that N_2 annealing has yielded very weak memory hysteresis. We know from our earlier experiment that Ge is very sensitive to oxygen in the structure and can be easily oxidized at the interface. We know also that although N_2 gas is spectrum, it contains some trace amount of O_2 gas which causes some oxidation. The oxidation of Ge layer prevents any nanocrystal formation and charge storage medium. Oxidation of Ge nanocrystals was confirmed by Raman measurements (as presented in chapter 4, in figure 4.9).
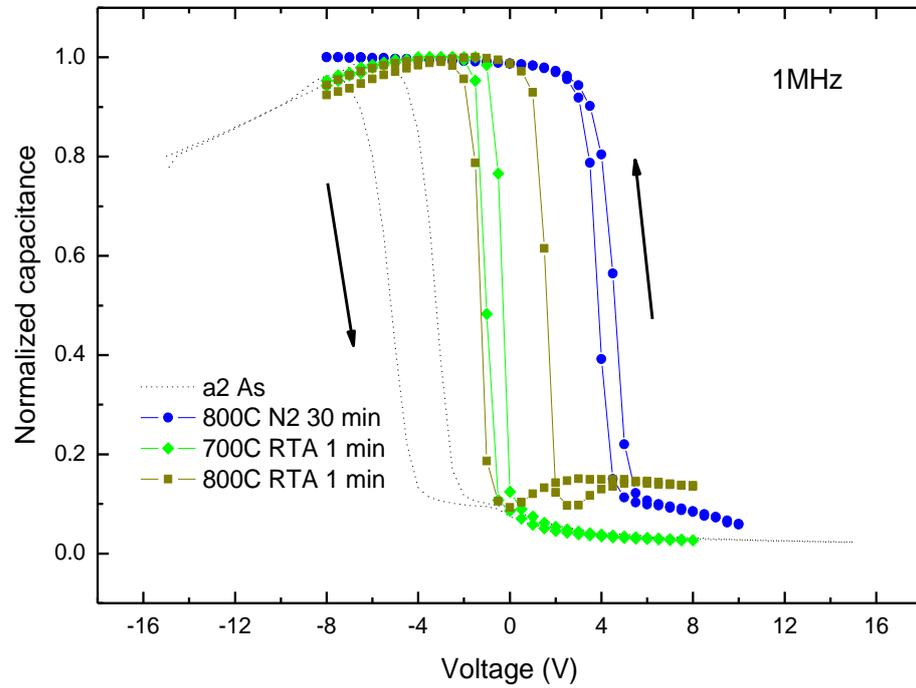
Figure 5.11: Capacitance-voltage characteristic of Si(p-type)/HfO$_2$/Ge/SiO$_2$ structure under high frequency.

Hysteresis is in counter-clockwise direction. It can be explained that, electrons are injected into structure in reverse sweep. Possible electron injection mechanism for this device structure is illustrated in figure 5.12 schematically.
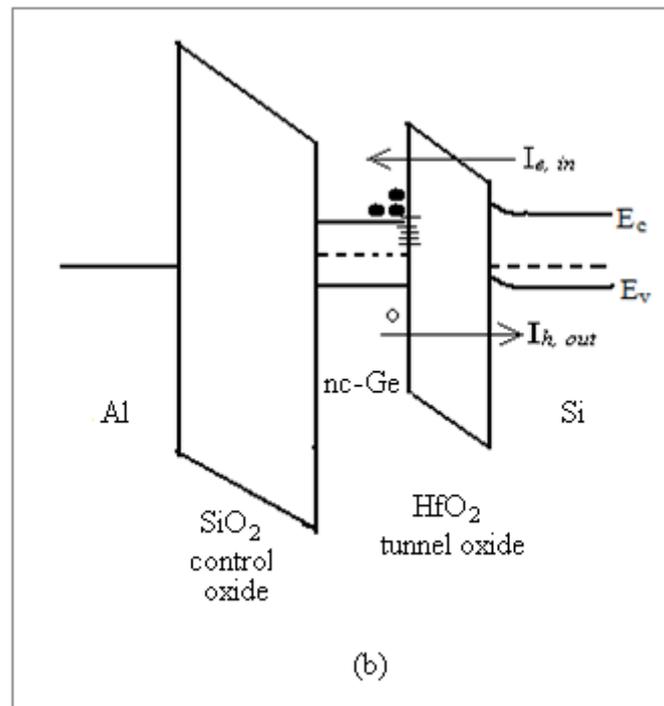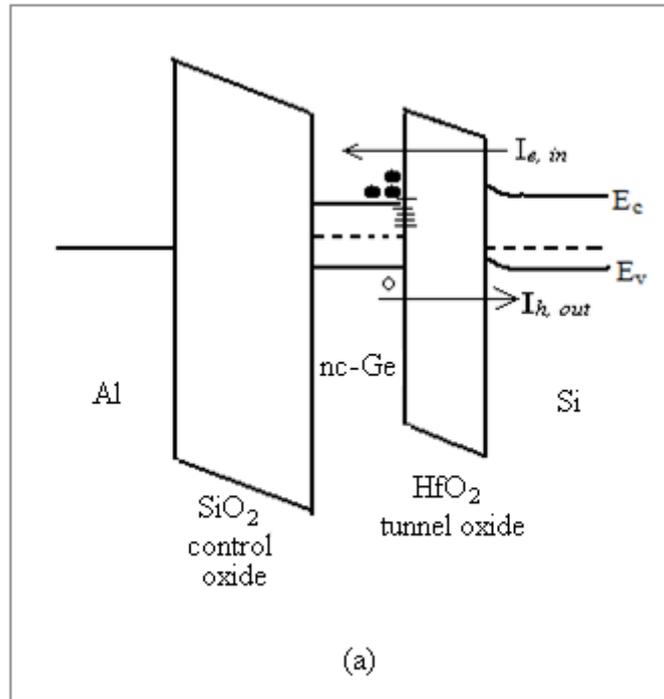
Figure 5.12: Energy band diagram of the Al/SiO$_2$/Ge/HfO$_2$/p-Si device structure at low (a) and high (b) electric field. Electrons and holes are represented by solid and open circles, respectively. (Traps in nc-Ge are not taken into account)

$I_{e,in}$ and $I_{h,out}$ represent the injection current tunneling through the tunnel oxide and hole current from nanocrystal to substrate, respectively. Band offset of conduction band is smaller than valance band thus electron injection is also possible at high field with enough energy to overcome energy barrier.

As it is explained in chapter 2.2 in detail, EOT gives the electrical thickness of the structures. Using accumulation capacitance, the values were extracted for the samples after hydrogen annealing. EOT of Al gated capacitors were given in table 5.3. They are not at the desired level but giving an idea about the nanocrystal based structures.

Table 5.3: EOT calculations for different types of samples

Sample	EOT (nm)	Control oxide (nm)	Tunnel oxide (nm)
2a	296	20	15
2b	74.8	15	15
a5Ge	155	15	10
13	153	20	25

There is a wide range of deflection in thickness. Actually, some is resulting from oxide thicknesses but the main effect could be attributed to possible parasitic parallel capacitances and resistances resulting from trilayer structure and the interfaces. It is more observable when SiO_2 is grown on HfO_2 as a tunnel oxide. The more interface means the more parasitic contribution. In sample 2b with nanocrystal Ge floating gate, since charge is confined and not spread inside floating gate, better equivalent thickness is obtained.

Equivalent circuit diagram for two types of structures are given in figure 5.13 for $SiO_2/Si/SiO_2/HfO_2/Si$ and $SiO_2/Ge/HfO_2/Si$-substrate multilayer structures.
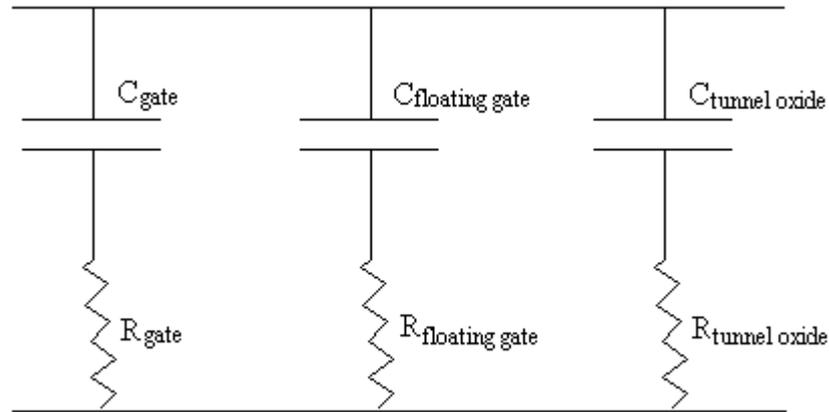
Figure 5.13: Schematic representation of equivalent circuit of the structures ($SiO_2/Si/SiO_2/HfO_2/Si$ and $SiO_2/Ge/HfO_2/Si$)

As structural analysis has indicated when we introduce thin Ge layer on HfO_2, Ge nanocrystals are formed at the interface and they confine the charge package in them. The thickness of the initial Ge layer has been found to be critical in obtaining memory devices with Ge nanocrystals. Another important result of this investigation is that N_2 annealing has caused the reduction in the charge storage due to the oxidation of nanocrystals.

CHAPTER 6

CONCLUSIONS

In this study, flash memory structures containing Ge and Si semiconductor floating gates were fabricated on Si substrate with various HfO_2 tunnel oxide thicknesses by magnetron sputtering deposition technique. Structures with both nanocrystal floating gate and continuous floating gate were fabricated. XPS depth profiling and Raman spectroscopy techniques and electrical characterization technique were employed for structural, chemical and electrical characterization. Following conclusions were drawn from these studies.

The chemical structure and interfacial properties of $SiO_2/Ge/HfO_2/Si$ multi layer structure were studied using ex-situ XPS depth profiling spectroscopy technique. Formation of low-k dielectric at HfO_2 layer and Si substrate interface was detected. XPS also provided clear evidence of different phases of Ge at the interfaces. Formation of Ge layer and nanocrystals were also confirmed by Raman spectroscopy. It was observed by XPS that after annealing at 800 °C in N_2 ambient for half an hour, Ge segregated out from HfO_2 and oxidized at SiO_2 interface. In addition, Hf and $HfSi/HfSiO_x$ formations were observed at HfO_2/Si interface. These form potential problems for the device operations. Some methods such as use of Hf buffer layer or nitridation to retard chemical reaction are proposed in literature to eliminate interfacial metal or silicide/silicate formations [46, 54, 63]. Moreover, after annealing process, germanium oxide formation was observed at SiO_2 interface.

C-V characteristics of the memory cells with Al as gate electrode were measured. In addition, the effect of H_2 annealing on memory cells was studied. Samples showed typical MOS characteristics with expected accumulation-

depletion-inversion regimes. We observed very small hysteresis for devices without any memory structure. This can be assigned to minor trapping at the oxide layer and interface charges. $SiO_2/Si/SiO_2/HfO_2/Si$ structure was studied in detail for different samples. Memory cell grown on p-type substrate with 25 nm HfO_2 and annealed at 1000 °C in nitrogen ambient and then at 400 °C in %30 H_2+%70 N_2 ambient showed better performance among continuous layer floating gate memory structures.

The samples with thicker Ge floating gate let to a continuous Ge layer formation as the charge storage medium while structures with thinner Ge layer resulted with nanocrystal floating gate formation. It can be concluded that formation of nanocrystals depends critically on the thickness of the initial Ge layer. Continuous layer floating gate devices with multi layer formation showed weak charge storage properties. However, $SiO_2/Ge/HfO_2/Si$ structure with nanocrystal floating gate was found to be the most promising one among all. Charge density and EOT values were calculated to be 2.93×10^{12} cm^{-2} and d_{EOT}= 74.82 nm, respectively. EOT value was better than the other cells grown in this study and charge density calculations were comparable with results announced in literature [17, 88-89]. Then, nanocrystal based multi-stack structure devices with HfO_2 tunnel oxide could be understood from the memory operation of the MOS structure.

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