RADAR EMITTER EMULATION FOR RESEARCH AND EXPERIMENTAL PURPOSES

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ABSTRACT

RADAR EMITTER EMULATION FOR RESEARCH AND EXPERIMENTAL PURPOSES

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The scope of this thesis is to implement radar emitter emulator in a low cost, portable hardware for operational and educational purposes. The model enables pulse train generation in real environment belonging to radar emitters for military exercises. The motivation comes from another research area which is to design effective algorithms for deinterleaving mixed pulse sequences in a suitable hardware and this thesis, covers the work done for implementing a hardware that generates mixed pulse sequences. First of all, a basic radar emitter model is built up using laboratory instruments by considering basic radar emitter models. Technical specs of these instruments have to be known well to find out how many emitters can be emulated simultaneously and what the limits of these emulations are. After giving emulation results, trigging signal generator externally to obtain complex mixed pulse sequences is mentioned. In the following section related schematics are given about implementing radar emitters. Cost efficient way of emitter emulation is mentioned by using wideband RF synthesizer/VCO with integrated RF mixers and some microwave components in the following section. A board is designed including all required components to implement radar emitter emulation. Tests are implemented in laboratory environment. Finally test results and technical specifications of the design are given. Also cost calculations of the implemented designs are done in the final section and some examples related to the use of emulators in environmental scenarios are given. Future work is also explained again in this final section.

Keywords: Electronic Warfare, Radar Emitter, RF Design, Emulation

ÖZ

ARAŞTIRMA VE DENEYSEL AMAÇLI RADAR VERİCİSİ ÖYKÜNÜMÜ

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Bu tezin kapsamı düşük maliyetle, taşınabilir donanımlar yardımıyla tatbikat ve eğitimsel amaçlarla radar emiter benzetimini gerçekleştirmektir. Model, gerçek ortamda askeri tatbikatlar için radar emiterlerine ait darbe üretimini mümkün kılmaktadır. Motivasyon, başka bir araştırma alanı olan karmaşık darbe dizilerinin etkin ayrıştırma yöntemleri ile uygun donanımda tasarlanmasıdır ve bu tez darbe dizilerini üreten donanımı uygulamak için gerekli çalışmaları kapsamaktadır. Öncelikle, radar emiter modelleri üzerinde durularak temel bir radar emiter modeli, laboratuvar enstrümanları yardımıyla gerçeklenmiştir. Ayrıca bu enstrümanların teknik özellikleri, aynı anda kaç emiterin benzetilebileceği ve benzetimlerin limitlerinin bilinmesi açısından çok önemlidir. Tasarıma ait benzetim sonuçları üzerine örnekler verildikten sonra sinyal üretecini karmaşık darbe dizisini elde edebilmek için harici olarak tetiklemekten bahsedilecektir. Sonrasında radar emiterlerini gerçeklemek için ilgili şematikler verilmiştir. Emiter benzetiminin geniş bantlı RF sentezleyici/VCO ile tümleşik RF karıştırıcılar ve mikrodalga elemanlar kullanılarak düşük maliyetli tasarımından bahsedilmiştir. Sonrasında radar emiter benzetimini gerçeklemek için gerekli tüm elemanları içeren kart tasarlanmıştır. Testler laboratuvar ortamında gerçeklenmiştir. Son kısımda test sonuçları ve tasarımın teknik özellikleri verilmiştir. Yapılan tasarıma ait maliyet hesaplamaları sonuç kısmında yapılmış ve benzetimlerin çevresel senaryolarda kullanımına yönelik bazı örneklere yer verilmiştir. Gelecekte yapılması gereken çalışmalar ise yine bu bölümde anlatılmıştır.

Anahtar Kelimeler: Elektronik Harp, Radar Vericisi, RF Tasarım, Öykünüm

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LIST OF SYMBOLS

AOA	Angle Of Arrival
ASP	Antenna Scan Period
AST	Antenna Scan Type
BW	Beam Width
CW	Continuos Wave
DC	Direct Current
dBm	decibel milli
ECCM	Electronic Counter Counter Measures
ECM	Electronic Countermeasures
ELINT	ELectronic INTelligence
ESM	Electronic Support Measures
EW	Electronic Warfare
FPGA	Field Programmable Gate Array
Hz	Hertz
I/O	Input/Output
IC	Integrated Circuit
IF	Intermediate Frequency
LO	Local Oscillator
MOP	Modulation On Pulse
MTI	Moving Target Indicator
NF	Noise Figure
PA	Pulse Amplitude
PC	Personal Computer
PLL	Phase Locked Loop
PRF	Pulse Repetition Frequency
PRI	Pulse Repetition Interval
PW	Pulse Width
RAM	Random Access Memory
RF	Radio Frequency
SNR	Signal to Noise Ratio
SRAM	Static Random Access Memory
VCO	Voltage Controlled Oscillator
VHDL	VHSIC Hardware Description Language

CHAPTER 1

INTRODUCTION

Emitters are one of the most important and fundamental devices that take place in part of many electronic equipment in use today. There are various uses of emitters and one of them is the radar, which is used to see what is going on in&out of the range of our eyes can see by using electromagnetic waves. Some of the implementations of radars are weather forecasting by remote sensing, flight arrangements and air traffic control in airports, cruise control and navigation for ship safety, space investigation and some other commercial and military uses. All of these radars that are embedded inside high technology equipment, are used for military purposes and form the backbone for most of the electronic military systems. Radars used for military purposes are set up on different platforms such as ship, plane, aircraft and land platforms. Friend and enemy vehicles can be seen from long distances and required precautions can be taken by using this technology. Military personnel have to be well educated to take required precautions in the shortest possible period of time. Radars are being well-known not only to see but also not to be seen. For instance, if someone tries to see the enemy, the enemy will try not to be seen. In this game the winner is the one who has the most knowledge and practice about the radars. Regular military trials must be arranged to train military personnel for real situations. For instance battle ship, combat plane, submarine etc. have to take their positions and there are at least two parties to attack and defend at the same time in these trials. The attacks can be seen by tracking each other through their radars and other party can use ECM techniques to break those tracks on them. Also one party tries to hide by considering radar coverage of the other party and make movements in this way. Many errors may occur from the mistakes of personnel to the errors which may occur in the hardware of these military equipment. Trials are very important to prevent errors that may occur in a possible real-life situation.

1.1 Motivation

Radars embedded inside high technology equipment are used for military purposes and form the backbone for most of the electronic military systems. Since radars have high technology equipment, those radars are expensive. Not only the radars are expensive, but also organizing such military trials to train military personnel calls for a great effort and cost. Because, in trials, all of the platforms have to be activated and it is costly. The primary motivation behind this work is the lack of commercially available cost effective emitter emulators that would have all the emitter modules or components on it. Hereby, the definition of emulator becomes important. Where any part of the actual system is present, the emulation approach is used. Emulation involves the generation of real signals to be received by a receiving system, or by some part of that system [1]. Therefore, having a portable and single board emitter emulator simplifies the design and reduces the need for using several different platforms for performing military trials. This board may be used as a platform for teaching and learning embedded emitter systems. Reducing the cost of the design as much as possible is one of the main design objectives. The target user groups for this design are the students, researchers in various universities and research labs and military personnel too. The other design objectives are robustness, reliability and functionality of the design which can simulate most of the emitters used today. The major uses of this design can be summarized as follows:

- The design would be used as a teaching tool in radar courses.
- Military personnel would use this design during the military trials to train.
- The sensitivity tests will be performed for ESM systems which are wideband receivers used for intercepting electromagnetic emissions.
- Besides, there is a database used for ESM systems to match the signals they detect and map these signals to known radars. Various ESM systems have different sensitivities and ESM systems may not be calibrated well. This design can be used to generate signals to be detected by ESM systems and as a result errors may be detected in those ESM systems by this way.
- The design will provide sufficient resources for the researchers and developers to build applications on top of it by interfacing different technologies with it.

1.2 Organization of the Thesis

The thesis has been organized into different sections to describe subject step by step. Chapter 2 of the thesis provides detail into the understanding of the emitter emulation, specifications and functionalities that were required for the emulators and radar emitter block diagram to be used in the design. The entire design rests on the initial specifications set for the project. All throughout the design project, these specifications and required functionalities were followed and kept in mind. Chapter 3 of the thesis provides the details and specifications of the instruments used for the emulator design. The instrument details such as triggering signal generator externally and connecting all of the components together have been discussed in this chapter. Also in this chapter, thesis provides the details of the hardware used for the emitter emulation. The hardware detail of each board used in the design is given and discussed briefly in this chapter. The design details of each circuit, including the schematic design, have been discussed in this chapter. In Chapter 4, which is the core of thesis, a single board is designed to perform the similar functionalities that are implemented in the previous chapters by using number of commercially available boards and laboratory instruments. Chapter 5 of the thesis provides detailed results about testing of the board. Testing forms a very important part of the project. In this chapter, some problems are determined in the board and solutions for those components are generated. Chapter 6 of the thesis summarizes and concludes the work done in this project and discusses the future work needed on this project.

CHAPTER 2

RADAR EMITTER EMULATION

In this chapter, radar emitters are examined as in their signal parameters. Since the aim of this thesis is to emulate radar emitters, transmitted signals from different types of radars are examined in this section. Receiving part of the radars are not covered in the scope of this thesis. In the following section, the signal processing units are considered. Radar signals are classified upon their properties and detailed information is given about each of these signal types. The reasons about why these signal processes required are discussed with examples also in this section. In the following section, the signals generated by different types of radars covered in details considering how to generate those signals using proper hardware. Hardware units are connections between world and algorithms. Signals cannot be transmitted as they are produced. There are many steps such as mixing the baseband signal with a local oscillator and amplifying the signal before transmitting through antenna to the world outside. All of these steps have the same purpose which is to generate required signal at the output of the transmitter in the area of radar's usage or depending on its application. Radars are classified upon their applications and each of those applications are covered in details to understand it better. Block diagram of each radar types is given as an example also in this section.

2.1 Signal Processing Point of View

First of all, radars basically transmit pulses and then analyze the reflected or scattered pulses from the objects to find their ranges, sizes or velocities. Ranging operation is performed by using time difference between the transmitted pulse from radar and scattered (received) pulse from object. Also the velocity of the object can be determined from frequency shifting, occurs on pulse. Moreover, from the amplitude of received pulses, the size of the object can be estimated. Basically, received power from object

and radar range equation can be given as in (2.1) [2].

$$P_{rec} = \frac{P_t G_T G_R \lambda^2 \sigma_b}{(4\pi)^3 R^4} = S_{min} \tag{2.1}$$

P_{rec} and P_t is received and transmitted power, respectively. G_R and G_T are receiving and transmitting gain of radar antenna, respectively. R is the distance between object and antenna. λ is operating wavelength and σ is radar cross section. Minimum receive power of the radar defined the range of radar. In this case received power is S_{min}. Basically, radar range equation becomes as in (2.2).

$$R_{max} = \left(\frac{P_t G_T G_R \lambda^2 \sigma_b}{(4\pi)^3 S_{min}} \right)^{\frac{1}{4}} \tag{2.2}$$

There are various types of radars and by the improvement of technology, these radar emitters have new capabilities to cover wider range or decrease the probability of their interception from other military devices. Since the main purpose of this thesis is to emulate radar signals, one needs to know more about radar signals. Therefore, parameters concerning radar signals are described below.

Frequency: Radar systems have been operated at frequencies as low as 2MHz and as high as 220GHz; laser radars operate at frequencies on the order of 10^{12} to 10^{15}Hz. However, most radars operate in the microwave frequency region of about 200MHz to about 95GHz, with corresponding to wavelengths on the order of 0.67m to 3.16mm [2]. Radars transmit pulses at a specific frequency depending on its application. Table 2.1 gives information about radar frequency bands with their applications [2]. Pulses are transmitted with a proper frequency and radars usually change their frequency to raise difficulty of being detected and being jammed. The change in frequency can be random or deterministic. Frequency changes may occur from pulse to pulse or pulse group to pulse group.

Pulse Width: Pulse width of the radar determines radar's energy. Radars rarely change their pulse width to take precaution to be detected. But radars can change their pulse width in accordance with the PRI parameter to improve their search capability. Pulse width measurement accuracy depends on the amplitude of pulse and sensitivity of the receiver. For small pulse amplitudes the pulse width measurement may be incorrect due to low Signal to Noise Ratio (SNR).

Pulse Amplitude: Majority of radars uses directive antennas making a mechanical rotation, hence the pulse amplitude received from a receiver changes in time. The pulse amplitude will be high whenever the main beam of radar is directed to the receiving

Table 2.1: Radar Frequency Bands

Band	Frequency	Description
HF	3-30 MHz	Over the horizon (OTH) radars.
P	$<$ 300 MHz	'P' for 'previous', applied in early radars.
VHF	30-330 MHz	Very long surveillance and ground penetrating radars.
UHF	300-1000 MHz	Very long surveillance, ground penetrating radars.
L	1-2 GHz	Long range surveillance, air traffic control radars.
S	2-4 GHz	Terminal air traffic control, long-range weather, marine radars.
C	4-8 GHz	Moderate range surveillance, terminal traffic control.
X	8-12 GHz	Short range tracking, missile guidance, marine radar, weather, medium resolution mapping and ground surveillance radars.
Ku	12-18 GHz	High resolution mapping, satellite altimetry.
K	18-24 GHz	Limited use due to absorption by water vapor and K-band is used for detecting clouds and for detecting speeding motorists.
Ka	24-40 GHz	Mapping, airport surveillance. Photo radar, used to trigger cameras which take pictures of license plates of cars.
mm	40-300 GHz	The frequency ranges depend on waveguide size.
Q	40-60 GHz	Used for Military communication.
V	50-75 GHz	Very strongly absorbed by the atmosphere.
E	60-90 GHz	
W	75-110 GHz	Used as a visual sensor for experimental autonomous vehicles, high-resolution meteorological observation, and imaging.
UWB	1.6-0.5 GHz	Used for through the wall radar and imaging systems.

system. When pulses from side or back lobe of radar are being received, pulses may not be detectable or the pulse amplitude may be very low. Detection of a pulse is directly related to the sensitivity of the receiver. Pulse amplitude is one of the parameters determining range of radar. Hence, high amplitude pulses make the radars seen, which is not desired.

PRI: Time difference between consecutive transmitted pulses is called PRI. The PRI value of radar can either be stable or vary from pulse to pulse. PRI values of radars

varies from microseconds to milliseconds which also plays role in range of radar.

PRI Type: PRI values can be stable, staggered, jittered or dwell & switch. Jittered PRI has large variations in PRI up to %30 randomly of its mean. This sort of variations used for ECCM. Staggered PRI means use of two or more PRI values in a fixed sequence and PRI value changes from pulse to pulse. The use of staggered PRI resolves blind speeds generally in Moving Target Indicator (MTI) systems. One another PRI type is Dwell & Switch. This type of radar uses several different PRI values and radar transmits pulses at a constant PRI for a dwell time and switches it's PRI for the next dwell time. This technique is used to resolve range ambiguities in pulse Doppler radars. Sliding and sinusoidal PRI types are both subsets of staggered PRI. Sliding PRI is characterized by monotonically increasing or decreasing PRI followed by a rapid jump to one extreme limit when the other extreme limit is reached. A sinusoidal variation in PRI can also improve radar's functionality. Sliding and sinusoidal PRI types eliminate blind ranges. One last type of PRI is pulse group which consists of closely spaced pulses separated by longer time intervals. This type of variation is used to resolve range and velocity ambiguity together.

Antenna Pattern: Antenna pattern gives information about transmit and receive properties of the antenna in space. Antennas may have different sensitivities from different angles. Also receiving and transmitting patterns of an antenna may change. Depending on the application, different scan pattern may be chosen. In most of the military radar applications, narrow beam antennas are chosen and back and side lobes are not desired. So the radar wants to receive the scattered pulses from its main lobe. Different types of antennas have different scan patterns and one example for antenna radiation pattern can be given in Figure 2.1. **Scan Type:** The rotation pattern of the antenna defines scan type. If antenna rotates circularly, this type of scan is known as circular scan. Also there are some other types of scans such as spiral, helical or conical. All of the names of these scan types give information about the rotation of antenna. Scan type gives information about the threat from the ESM receiver point of view. For instance, if scan type is locked, which means an antenna is locked on a target and transmit high amplitude pulses, a guided missile is being launched to the target. One more example can be given for circular scan, in which pulses from the radar is being received from ESM receiver periodically.

Scan Period: Scan period is the time during which a radar antenna completes one rotation around itself for circular scan. Scan period can be determined for other scan

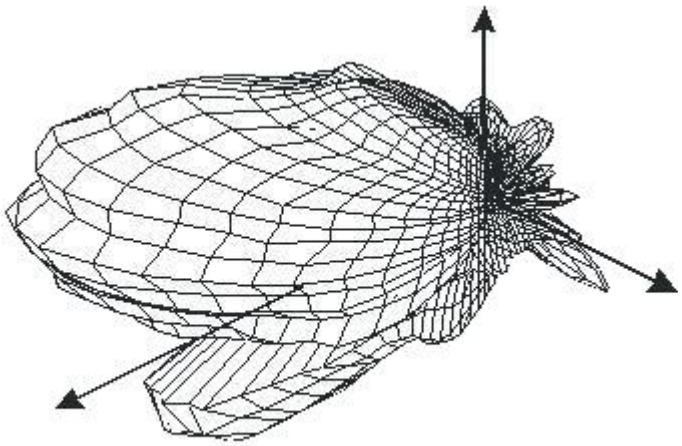

Figure 2.1: Antenna Radiation Pattern

types. The definition can be generalized as the time spent to complete a radar's one rotation pattern. Radars can change their scan period too. Double antenna radiation may be used. One more example can be given. If number of threats increase in the environment, radar antenna may rotate faster to track all of the threats.

Beam Width: Mostly used as 3 dB beam width which is about the aperture of the antenna in degrees where the signal power decreases 3 dB below its maximum value. For most of the radar applications, narrow beam antennas are desired.

Modulation: Pulses transmitted from radar modulated such as frequency modulation (chirp) or barker coded pulses to improve radars effectiveness. More type of modulations can be defined for radars such as amplitude modulation on pulse (AMOP), phase modulation on pulse (PMOP) and frequency modulated continuous waves (FMCW).

Information about what sort of parameters needs to be known to simulate radar signals is given above. Till the end of the thesis these basic parameters are combined together to obtain radar pulse trains of different types.

2.2 Classification of Radar Systems

In this section, classification of radar systems are briefly given to make a general description for radars. Moreover, each of the radar types are examined from signal processing point of view. Some research is done for the ways of emulating different type of radar signals in this section. Types of radars are classified in Figure 2.2 [3] and brief descriptions are given about those types. Depending on the desired information, radar

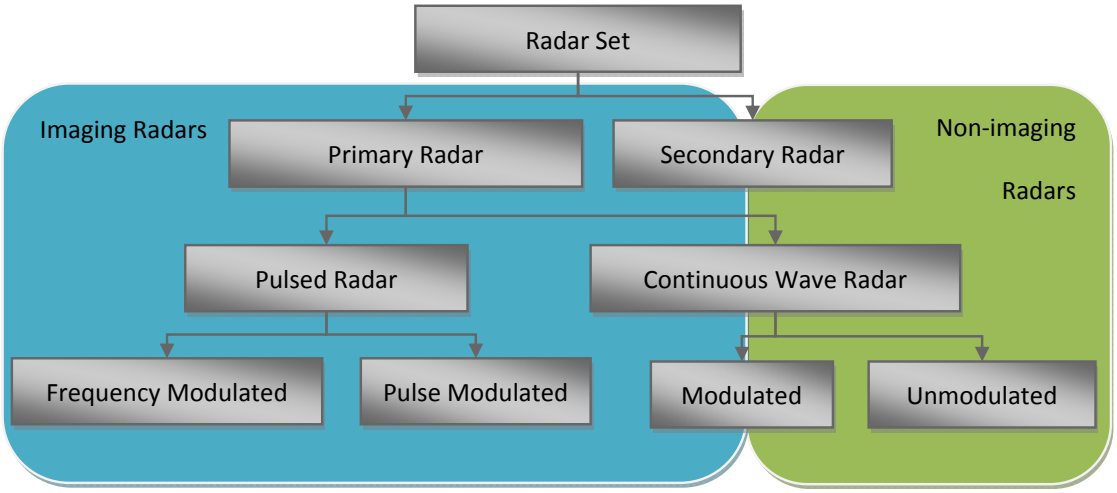

Figure 2.2: Classification of Radar Systems

sets must have different qualities and technologies, and those radar sets are described below.

Imaging Radar / Non-Imaging Radar: Imaging radars form picture of the observed object or area. Generally uses of an imaging radar form a map of the earth and other planets. Also these kind of radars categorize targets for military systems.

A non-imaging radar system is used for traffic control and radar altimeters. These are also called scatterometers. Because these radars measure the scattering properties of an object or region that is being observed. Non-imaging Secondary Radar applications are immobilizer systems in some recent private cars.

Primary Radar: Primary radar transmits high frequency signals which are scattered from targets. The echoes are then received and processed. Unlike secondary radar sets, a primary radar unit receives its own emitted signals as an echo.

Secondary Radar: Secondary radar sets have a transponder (transmitting responder) on board and this transponder respond to interrogation by transmitting a coded reply signal. For instance, secondary radar on an airplane has a transmitter and responses can contain much more information than a primary radar unit that is able to acquire. Secondary radar set in an airplane can give information about altitude, identification code or also any technical problems on board such as a radio contact loss.

Pulsed Radars: Pulsed radar sets transmit high frequency pulses of high power. After this pulse, a longer break follows in which the echoes can be received, before a new transmitted signal is sent out. Direction, distance, size and altitude of the target can

be determined from the antenna position and time of arrival of the echoes.

Continuous Wave Radar: CW radar sets transmit a high frequency signal continuously. The echo signal is received and processed. In continuous wave radar sets, transmitter and receiver does not have to be mounted at the same place. Every company's civil radio transmitter can work as a radar transmitter at the same time, if a remote receiver compares the propagation times of the direct signal with the reflected one. This is the concept of passive radar and one can determine the correct location of an airplane from the evaluation of the echo signals of three different television stations.

Unmodulated CW-Radar: The transmitted signal of this equipment is generally constant in amplitude and frequency. This equipment is specialized in speed measuring and traffic control. Distances cannot be measured. For instance unmodulated CW radars are used as speed gauges.

Modulated CW Radar: In this kind of radar, the transmitted signal is constant in the amplitude but modulated in frequency domain generally. Measurements are performed without reception break and the results are available continuously in modulated CW radars. These radar sets are used where the measuring distance is not too large and it is necessary for continuous measuring. For instance an altitude measuring in airplanes is continuous for safety. A similar principle is also used by radar sets whose transmitting pulse is too long to get a good range resolution. In this case frequency modulation is performed on pulse. Therefore, range resolution within the pulse is obtained by using pulse compression techniques.

2.3 Radar Emitter Emulator

The classification of radar systems and essential parameters which makes radar signals identical, are given in the previous sections. In this section, requirements for generating radar signals are explained and basic block diagram of a radar is given in Figure 2.3. Different radar sets transmit identical signals depending on its application. These types of signals are mentioned in this section to make decision about determining the required hardware to generate these signals in the following chapters.

Basically, a radar transmits high amplitude pulses at a frequency and evaluates the scattered pulses from environment. Therefore, a radar emulator have to synthesize the required frequency. If these transmitted pulses have PRI and PW, switching of the synthesized frequency is important. High power pulses can be obtained by amplifying

the generated pulses by using a power amplifier which is essential to transmit those pulses in a desired range. Duplexer is one of the important stage in conventional radar

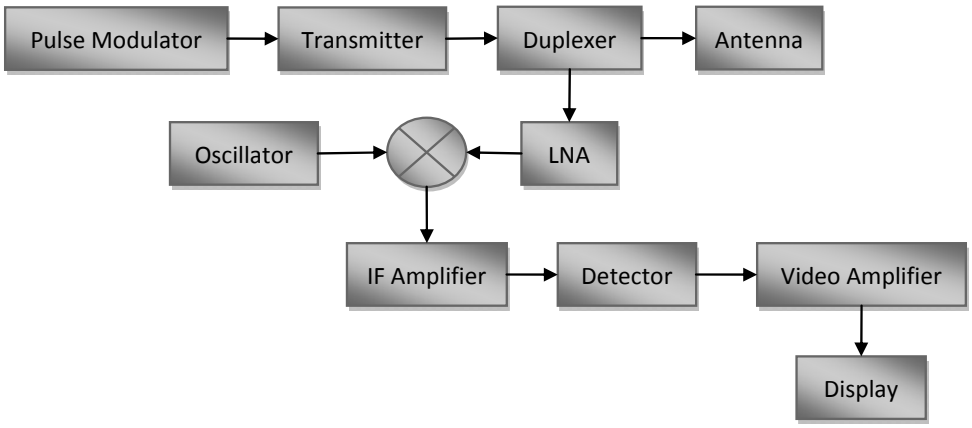

Figure 2.3: Basic Radar Block Diagram

sets which is used to switch antenna between transmitter and receiver as seen from Figure 2.3, so that only one antenna needs to be used. Switching is necessary because the high power pulses of the transmitter would destroy the receiver if energy were allowed to enter the receiver. Duplexer is used to protect receiver during the transmission and channel the received signal to the receiver during the reception. Since the transmission and reception take place at different times, the isolation of the transmitting and the receiving channels can be as high as required by using a single antenna. In this thesis, receiver side of radar is not covered. So it is not required to use a duplexer stage in this design.

From Figure 2.3, local oscillator and mixer are commonly used blocks for a conventional radar sets. Mixer is used for mixing frequency of the signals from its inputs and mixed signal is given to its output. Usually local oscillator signal is an input to a mixer to mix the scattered signal in radar system. Local oscillator signal is used with mixer to mix signal to downconvert to IF frequencies or upconvert to the RF frequencies.

The IF amplifier makes the receiver very sensitive for the weak echo signals. IF stage generates a signal at IF frequency. This signal is mixed with a stable signal having local oscillator frequency. IF amplifier stage is a low noise amplifier stage which usually comes after mixer stage as in Figure 2.3. IF amplifier usually used in the receiving side of a radar system. The need of an IF amplifier will be discussed in the following chapters.

Antenna is one of the most important components of radar, because of the need of sending/receiving the signal to/from environment. The antenna transfers the transmitter energy to signals in space with the required distribution and efficiency as seen from Figure 2.3. This process is identical during reception. It does not matter how well one produces the radar signal if it can not be sent to the media outside. Antennas have different properties such as radiation pattern, beam width and scan patterns. Depending on the uses of an antenna, these parameters vary. From radar application point of view, there should be a narrow beam width of the main lobe and side lobes must be suppressed as best as it could. To make a radar emulator, different kind of radar antennas are required to be imitated. Because different radar antennas have different transmit/receive patterns and beam widths. In this thesis, different antenna designs are not covered, only the radar signals are generated. It is decided to use commercially available antennas to be connected at the end of the final stage of design.

Basic radar signals can be generated by the procedure above. Since the military radars are not simple devices, these radars use different signal processing techniques not to be seen or increase their effectiveness as mentioned in the previous sections. This kind of radar is called frequency diversity radar. In order to overcome some of the target size fluctuations, many radars use two or more illumination frequencies. Frequency diversity may use two transmitters operating in tandem to illuminate the target with two separate frequencies. This brings another requirement for radar emulators to make it possible to generate different frequencies. Therefore, synthesizer to be used in the design must generate different frequencies. To generate pulses in different frequencies, two different solutions can be offered. In frequency diversity radar sets a time controlled switch which is controlled passively or actively may be used to switch signals from different frequencies from the input to the output. One synthesizer can be used to synthesize different frequencies in consecutive pulses. The time spent between the consecutive pulses must be longer from the time for the synthesizer to synthesize another frequency. Another solution may be used such as two or more synthesizers can be used to generate signals in different frequencies. Different frequencies can be generated at the output by switching the signal at the output of the synthesizers. Moreover, frequency may change within the duration of a single pulse (frequency diversity) and combinations of the several methods mentioned above may be used also such as transmitting pulses in different frequencies by using pulse compression techniques. In this case the synthesizer that will be able to generate chirp type compressed pulses and may be more than one

synthesizer is required to generate signals in different carriers simultaneously. This processes are implemented by pulse modulator and transmitter blocks of a radar as given in Figure 2.3.

Multiple frequency usage is advantageous which brings high jamming immunity to the radar. The further processing of the single received signals has a contribution to that. The work with two transmitters of different frequencies is often looked at falsely only for reasons of the redundancy. However, if one transmitter fails, other transmitter continues to transmit pulses. In this case, maximum range of the radar unit reduces but it works.

Some other important stages used in conventional frequency diversity radars are frequency selector, delay stage, summation circuit, multiplier, synchronizer and signal processing units. Frequency selector is used to separating received echo signals in the different frequencies to be processed. Delay stage is used to increase effectiveness of radar by delaying the echo signals to be processed together. Synchronizer supplies synchronizer signals at the times that radar transmits pulses for the indicator, and other associated circuits. Signal processor stage evaluates echo signals and processes those signals in separate channels. There are several processing procedures used to accumulate and compare signals with a threshold value. Though, radar effectiveness is increased. These stages, which are not required in radar signal emulation, are not covered.

CW radar sets transmit high frequency signal continuously. In these kind of radars, speed is measured by the Doppler procedure. If range information is required, the time measurement can be realized by a frequency modulation or phase keying of the transmitted power. A CW radar transmitting unmodulated power can measure the speed only by using Doppler effect. A run time measurement is not necessary for speed measurements, because the actual range of the object does not have a consequence in traffic applications. The value of the Doppler frequency depends on the wavelength. Therefore these radar sets use a very high frequency band. Emulation of unmodulated CW radar is similar to the basic radar signal emulation. In this case the synthesized frequency is not switched for pulse modulation.

Another kind of CW radar is FMCW radar. CW radars cannot measure distance, because CW radars do not transmit pulses. In order to measure the distance, frequency shifting methods can be used. In the frequency shifting method, a signal that constantly changes in a frequency around a fixed reference is used to detect stationary objects.

From the frequency of received signal, range can be calculated in a way similar to pulsed radar. FMCW radars usually use smoothly varying frequencies up and down. This brings another requirement to design which is the synthesized continuous wave signal must vary in frequency up and down smoothly. The synthesizer must allow frequency variations.

FMCW radars are frequently used as radar altimeter. Radar altimeter measures the exact height during the landing of aircraft. Radar altimeters are also used as terrain avoidance warning systems, telling the pilot that the aircraft is flying too low or that terrain is rising to meet the aircraft.

Finally the specifications of the radars are covered and types of the signals that radars generate are mentioned in this section. From those specifications, requirements for a radar emitter emulator is determined and in the following sections different ways of radar emitter emulations are described.

CHAPTER 3

RESEARCH ON DIFFERENT WAYS OF EMITTER EMULATION

In this chapter, different ways of generating radar pulse trains are covered. Therefore, some of the radar pulse trains can be generated by using laboratory instruments and commercially available boards. Previous chapters with this chapter will point to radar emitter emulator board design. Hence, there are not detailed tests and complete system is designed by the ways mentioned in this chapter to generate radar signals.

3.1 Emitter Emulation by Using Instruments

Till this point an introduction is given about various types of radars and parameters forming pulse trains of those radars. Most of the radar pulses can be generated by using a signal generator depending on their specifications [4]. Signal generators specified on generating different types of signals in a wide frequency band from continuous wave to modulated pulse trains. These devices are mostly used for testing and experimental purposes. In this part of the thesis radar pulse trains are generated by using instruments. Use of laboratory instruments is not the proper way to generate radar signals because these devices are expensive and once the system is designed it is hard to carry setup to any place that the radar signals will be generated. Nevertheless, it is shown that it is possible to generate those signals by using laboratory instruments. Table 3.1 gives a list of instruments that are used for this section. A signal generator is an electronic device that generates repeating or non-repeating electronic signals in either the analog or digital domains. These devices are generally used in designing, testing, troubleshooting, and repairing electronic devices. It is possible to generate radar signals and basic block diagram for this can be given in Figure 3.1. Use of PC while controlling instruments is not necessary. PC uses in this system bring to set required parameters remotely and

Table 3.1: List of Instruments

Instrument	Model
Signal Generator	Agilent (E8241A, E8244A)
Spectrum Analyzer	Agilent (E4448A)
Oscilloscope	RDS (2002)
Arbitrary Waveform Generator	Agilent (33120A)
Power Supply	Agilent (E3631A)

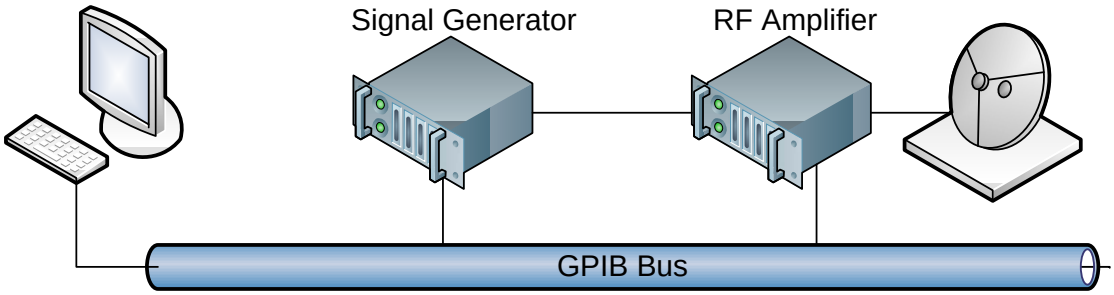

Figure 3.1: Radar Emitter Emulator Using Instruments

quickly. Characteristics of the radar pulse train is limited with the specifications of the signal generator. Pulse trains can be set by configuring pulse modulation capability. Pulse modulation can be initialized by the steps as follows;

- Set output frequency
- Set RF output amplitude
- Set pulse period (PRI)
- Set pulse width
- Activate pulse modulation
- Activate RF output

The following procedure is valid for E8244A model signal generator. By this way a basic radar emitter can be simulated because frequency, PRI and pulse width values are set in that procedure. Characteristics of the pulse train can be given with its ranges as below. These are the limits of signal generator in its pulse modulation output.

- Frequency may vary from 500MHz to 40GHz

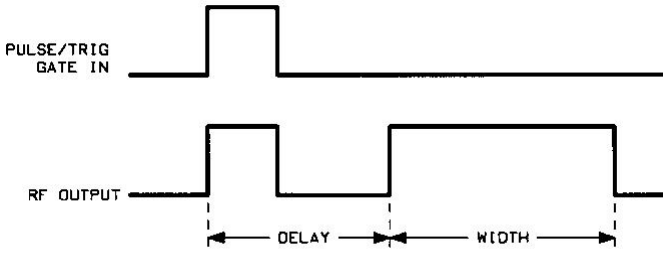

Figure 3.2: Pulse Modulation By Using Internal Doublet

- Minimum pulse width is 20ns.
- Maximum PRF value is 10MHz.

Configurations given above enables the generation of a simple stable pulse trains at a fixed frequency, amplitude and pulse width. To enhance the generation of different pulse trains, pulse sources can be used and by use of an internal pulse generator, pulse modulation parameters change as below.

- Modes are free-run, triggered, triggered with delay, doublet or gated. Triggered with delay, doublet or gated modes require an external trigger source to trig generation of pulses.
- PRI changes from 70ns to 42 s which means PRF varies between 0.024Hz-14.28MHz.
- Pulse width changes from 10ns to 42s.
- In free-run mode delay changes between values of 0 to ±42s. In triggered with delay and doublet modes this value becomes 75ns to 42 s with ± 10ns jitter.
- Resolution is 10ns and RF delay is smaller than 20ns.

The following list summarizes the different sources available for pulse modulation.

- External Pulse modulates by following an external pulse signal connected to the signal generator's pulse/trigger gate input connector.
- Internal Doublet produces two pulses at the RF output connector for each trigger event at the trigger in connector. The first pulse will follow the external trigger signal. The second pulse will have predefined delay and width parameters as seen in Figure 3.2.

- Internal Free-Run produces internal, free-run, pulse modulation with defined period, width and delay.

- Internal Gated produces an internal, gated, pulse modulation. When a valid gate signal is applied to the trigger in connector, a pulse with predefined parameters will be generated at the RF output connector. Pulse width and PRI parameters are set by way of the front panel or by programming the device. When the falling edge of the gate signal is sensed at trigger in connector, the pulse train will cease. If the falling edge of the gate signal occurs in the middle of a pulse at the RF OUTPUT connector, the generation of last pulse will be completed before the pulse train ceases. Once the falling edge of the gate signal is sensed, a time interval equal to the pulse repetition interval must elapse before another rising edge at the Trigger In connector will be valid as seen in Figure 3.3.

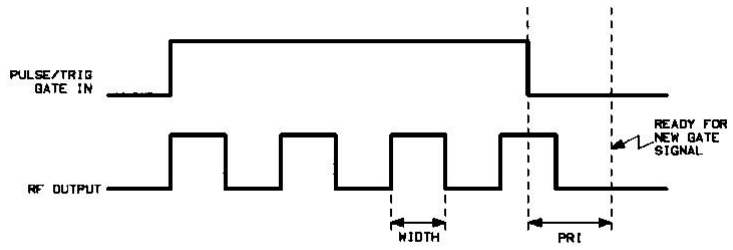

Figure 3.3: Pulse Modulation By Using Internal Gated

- Internal Trigger produces an internal, triggered, pulse modulation. An RF pulse with predefined width and delay parameters will occur at the RF output connector whenever a valid trigger signal occurs at the trigger in connector as in Figure 3.4. The RF pulse will have pulse width and delay as set by way of the front panel or by programming device.

- Internal Square produces internal, square, pulse modulation. This is a form of internal free-run pulse with a 50% duty cycle. The period is determined by rate.

The representation of pulse modulation can be summarized as in Figure 3.5. Pulse/Trigger Gate Input connector accepts an externally supplied TTL-compatible signal for use as a pulse or trigger input. The explanations above about generating radar pulse trains are not enough. Because some parameters such as frequency, amplitude and pulse width

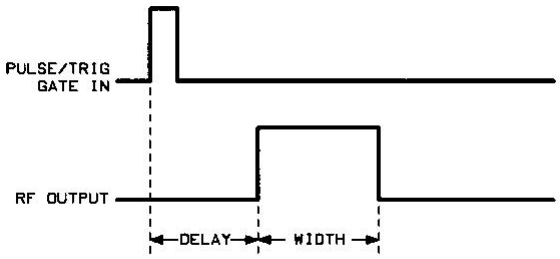

Figure 3.4: Pulse Modulation By Using Internal Triggered

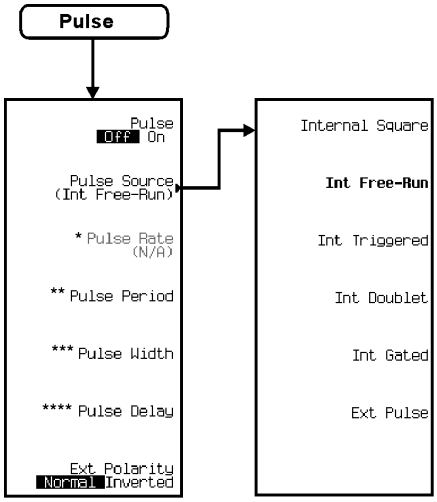

Figure 3.5: Pulse Modulation Selection

may change from pulse to pulse. One way to achieve this is to set parameters of a pulse after transmitting a pulse. Signal generator can be configured over GPIB bus or Ethernet. So after transmitting a pulse, parameters of the following pulse can be configured. When considering radar pulse trains, variations between consecutive pulses may occur before the time delay to configure signal generator to that pulse. GPIB and Ethernet delay the configuration of signal generator. In this case sweep mode of the signal generator can be used. Sweep list of signal generator triggered by using the ways explained in pulse sources. Sweep list configures parameters of signal generator. So by this way generating complex pulse trains will be possible. Signal generator has two sweep modes.

Step sweep allows to enter RF output start and stop frequencies and amplitudes, a number of equally spaced points (steps) to dwell upon, and the amount of dwell time at each point. When a step sweep is activated, the signal generator will sweep the RF output based on the values entered for the frequency and amplitude parameters. The

frequency, amplitude, or frequency and amplitude of the RF output will sweep from the start amplitude/frequency to the stop amplitude/frequency, dwelling at equally spaced intervals defined by the number of points softkey value for the configured step dwell time. Step sweep provides a linear progression through the start-to-stop frequency and/or amplitude values. The direction of the sweep can be toggled up or down.

The other sweep mode, which is list sweep, allows creating a list of arbitrary frequency, amplitude and dwell time values. RF output is swept based on the entries in the List Mode Values table. Unlike a step sweep that contains linear ascending/descending frequency and amplitude values spaced at equal intervals throughout the sweep, list sweep frequencies and amplitudes can be entered at unequal intervals and nonlinear ascending/descending or random order. Each step sweep point's associated frequency, amplitude and dwell time values are entered into a row in the List Mode Values table. To configure single step sweep following directions must be followed.

- Open sweep mode.
- Set sweep repeat single continuous.
- Set frequency start/stop values.
- Set amplitude start/stop values.
- Configure number of sweep points.
- Configure step dwell time at each point.
- Enable RF transmission.

In a continuous sweep mode, a continuous repetition of the frequencies and amplitudes configured in the step sweep are available at the RF output. List sweep mode using step sweep data must be used in generation of complex pulse trains. In this procedure, step sweep information is changed by editing several points in the list mode values table. To configure list sweep mode, following steps must be considered.

- Open sweep mode.
- Set sweep type list.
- Configure list sweep.
- Turn sweep on.

- Set sweep trigger.
- Enable RF transmission.

In the configuration above, external pulse trigger sources can be used to activate next step in the list. In this case, it is important to trigger the signal generator externally to obtain desired pulse trains. By using an FPGA board, signal generator can be trigged in required sequence. Once the list of pulses are configured in the signal generator, by choosing external trigger mode device can be triggered with the desired pattern.

Finally, pulse generation by using instruments is covered in this section. Pulse trains are generated in a desired pattern. Signal output of the signal generator can be connected to an RF amplifier module to increase range. Different antenna uses brings to generate different radiation patterns depending on the generated radar pulses. Variation of the amplitude of signal brings the capability about emulation of scan patterns and periods.

3.2 Emitter Emulation by Using Boards

In this section, radar emitters are tried to be generated by using commercially available evaluation boards. Most of the companies produce test boards for their products such as PLLs, mixers, amplifiers and switches. Customers can buy those components to try those boards to see if those components meet their requirements or not. From the requirements given in the previous chapter, a frequency synthesizer, power amplifier, mixer and switch modules are required. Only the PLL and amplifier modules are supplied and the trials are carried out depending on these two evaluation boards. The aim of this section is not to generate all of the radar signals, it is just to show the possibility of generating those signals.

Switch and mixer evaluation boards are not supplied during thesis. Therefore, complete radar signal generation could not performed. Only continuous wave signals are generated by using PLL and amplifier modules. These modules are supplied from RFMD company and evaluation board of power amplifier SZA-2044(Z) and evaluation board of PLL RF2051 are used for application.

The PLL chosen for this application has 30 MHz to 2.5 GHz frequency range. RF2051 has integrated PLL and VCO modules to synthesize desired frequency. Moreover RF2051 have integrated mixers and a serial bus to configure the output frequency

characteristics. Detailed functional block diagram of RF2051 is given in Figure 3.6.

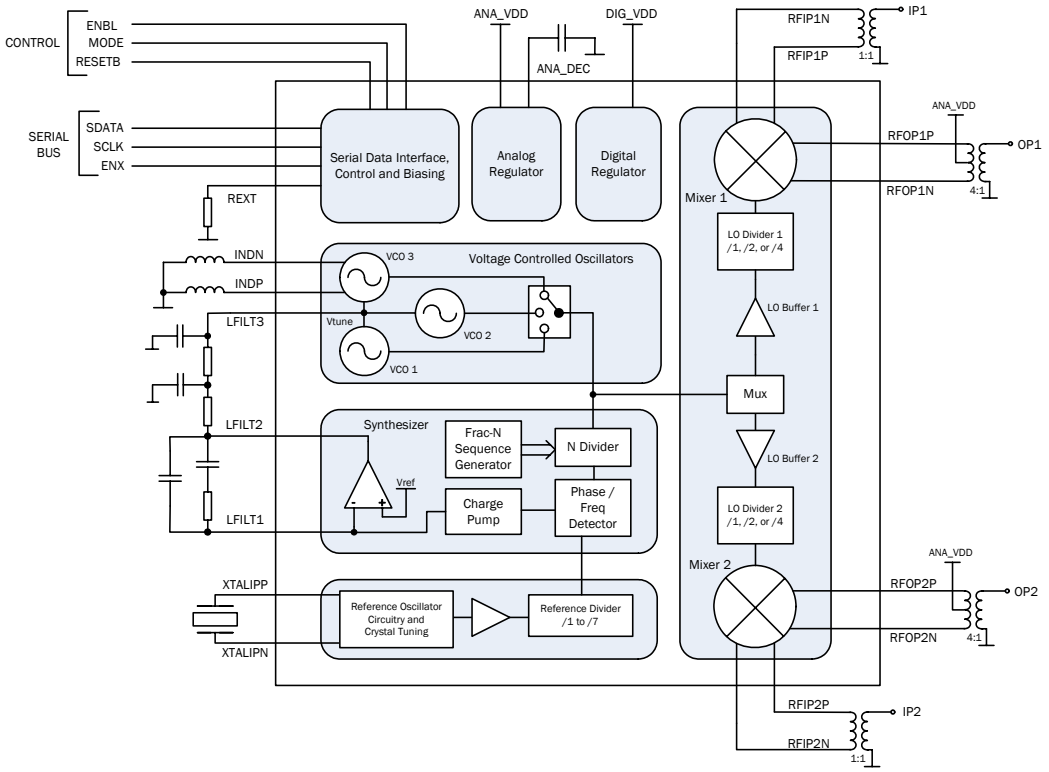

Figure 3.6: RF2051 Detailed Functional Block Diagram

The power amplifier module used for design operates between 1.9 - 2.7GHz and gives 22 dBm output power at 2.4GHz. P_{1dB} value is 29.5 dBm and small signal gain varies between 23.5dB to 27.5dB. Evaluation board schematic for SZA-2044 is given in Figure 3.7.

SMA output of the RF2051 is connected to SMA input of SZA-2044 and the output of the amplifier is attenuated to measure resulting signal at spectrum analyzer. By doing as such, continuous wave signals can be generated because there is not any switching stage exist in this design. Some other trials are performed by connecting a RF splitter in reverse to combine output of two RF2051 to obtain mixed signal at the input of power amplifier. By doing as such, two frequencies can be seen at the spectrum analyzer. RF/IF frequency range of integrated mixer is 30MHz to 2500MHz. If the IF port of the mixer was able operate from DC to 2500MHz, switching will be possible by switching a DC voltage as an input to IF port. When switch is closed DC voltage is transferred

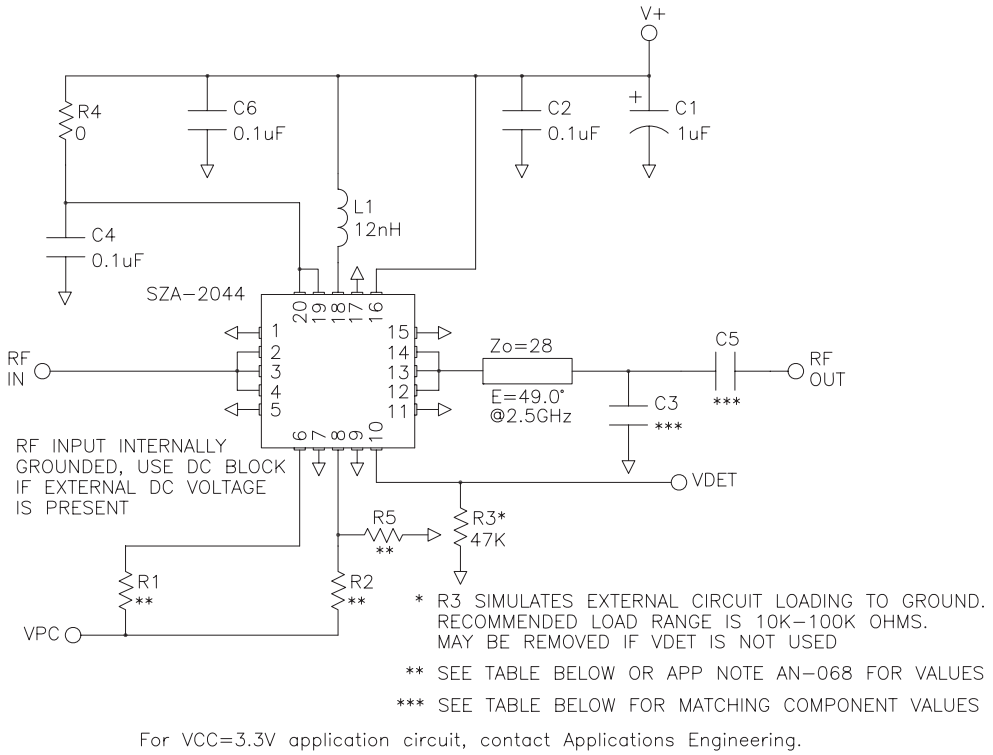

Figure 3.7: SZA-2044 2.0 to 2.7 GHz Evaluation Board Schematic

to IF port of mixer and then mixed with the frequency to obtain a pulse. If switch is opened, there will not be a DC voltage at the IF input of the mixer and RF signal will be mixed with 0 voltage. Therefore, no signal will be seen at the output of the mixer.

Detailed measurements and tests are not performed in this structure. Because the aim of this thesis is to generate radar signals. Without any pulse modulation, radar signal generation could not be performed at all. The importance of this section is the idea that is brought from these evaluation boards. In the next chapter, a single board is designed including synthesizer, mixer, switch and amplifier.

CHAPTER 4

RADAR EMITTER EMULATOR DESIGN

RF board design is different than other circuit designs. There are many constraints and trade-offs that must be considered during design. Moreover, RF signals are being exposed to unwanted distortion at the output of every component. Since these components are cascaded to each other those distortions become more of an issue. Undesired effects must be considered such as RF signal at the output of one component have to be proper for the input of the other component which is connected in the cascade. Design decisions determines the RF signal at the output of the transmitter and requirements have to be considered when making those decisions. Consequently, high frequency components have to be selected carefully.

In the previous chapters, most of the radar emitters are covered and different ways of emulating these emitters are presented by using instruments or commercially available boards. In this chapter, the design of a basic radar emitter emulator hardware is described. From the given requirements in the previous sections, frequency synthesizer is required to synthesize frequency; switch is required to modulate RF frequency with the mentioned specifications. Furthermore, modulation of the synthesized signal is possible by using a mixer allowing signals from DC up to 1 GHz to it's IF port.

First of all system must be designed by generally a set of functional blocks, and their specifications, that will interact in a manner that produces the required system performance. Therefore, characteristics of individual blocks must be clearly understood on how they affect the performance of the system. By this process, existing blocks can be combined with new blocks, using the specifications of the former and creating specifications for the latter in a manner that will achieve the system requirements [5]. During this chapter, every design step is examined. Before going into details, block diagram of a radar emitter emulator is described and followed by the section describing how to

choose components correctly. System diagram is built in AWR Microwave Office which is a program to design and simulate microwave circuits, by using selected components. Results of simulations are discussed in the following section. Other than the system design, PCB layout of the circuit is created in Altium Designer which is a PCB design program. PCB design section is about fabrication process. Designed layout is printed and components are placed. Finally tests are performed and results about the designed board is given at the end of this chapter.

4.1 Radar Emitter Emulator System Design

Radar emitter emulator is being expected to emulate most of the emitters operating within the required frequency band. Accordingly, parameters must be considered to imitate emitters in the final design. Therefore, design constraints are itemized and requirements are given in details as follows.

Frequency: Synthesizing different frequencies is important to emulate different emitters. For most applications, PLL is used for synthesizing different frequencies. In this thesis, the 3 - 4 GHz frequency band is chosen. Therefore desired frequency at the output can be synthesizer by a PLL operating in this band. 1 MHz is chosen to be frequency synthesizing resolution between 3 - 4 GHz band. This resolution is configuration dependent and 1 MHz resolution is enough for this application. Chirp type signals can be generated depending on the capabilities of the chosen PLL. Noise level, harmonics and intercept points are considered later.

Pulse Repetition Interval: PRI is one of the most distinctive parameters of radars. Because, these values are identical for most of the radars. Different PRI values and types at the output of the PLL can be generated by switching or mixing the signal. PRI value of radars vary from several microseconds to several milliseconds. Moreover, stable, staggered and jittered PRI types are handled. Many other subbranches of these types can also be generated. PRI modulation types such as sinusoidal, saw tooth, ramp-up, ramp-down and dwell&switch are also covered.

Pulse Width: PW value can be controlled by switch, which controls PRI. Transmit duration of a pulse is pulse width which is, in other words, time spent by switch in closed mode. So, the switch that will be used must be controlled digitally. Pulse width may vary from nanoseconds to microseconds for radars and this brings another requirement that switching speed must be at least several nanoseconds.

Scan Type: Radar antennas are interesting not only that they have narrow beams, but the beams move in ways tells a lot about the type of radar and its operating mode. The movement of the antenna is called antenna scan. The real interest in here is how the threat antenna looks to an EW receiver as it is moved [1]. The behavior of a circular scan over a receiver appears when receiver is illuminated and this behavior depends on the distance between radar and receiver. If that distance is far enough, receiver is being illuminated by only the pulses from the main lobe of radar. But, if radar and receiver are close enough, radar illuminates the receiver with pulses from its main lobe, side lobes and maybe back lobe. By choosing a narrow beam antenna and biasing the gain of power amplifier, emulation of scan types becomes possible. Scan types can be circular, sectoral, conical, helical and more types can be taken into account. In the scope of this thesis only most common scan types are simulated such as circular, conical and stable. Scan type is simulated by biasing amplitude of pulse train digitally or some sort of buffer circuit can be designed behind the switch to tune the amplitude of the DC signal.

Scan Period: Once the scan pattern of an antenna is known, the repetition period of this pattern can be arranged by changing the biasing speed of amplitude of the signal at the input of switch or amplifier.

From the requirements listed above, needed components can be listed as PLL for synthesizing frequency, switch for forming pulse train envelope, power amplifier for amplifying pulses, mixer to mix the signal and FPGA to control these components. Therefore, the system diagram of a radar emitter emulator can be given in Figure 4.1.

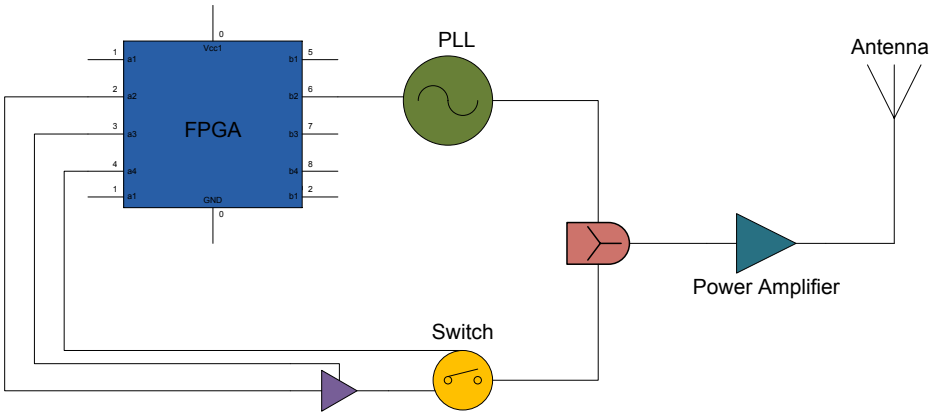

Figure 4.1: Basic Radar Emitter Emulator Block Diagram

From Figure 4.1, the design has digital and RF parts. Digital parts are used to control components such as PLL, switch and amplifier. RF parts are analog parts which the radar signals are generated. In the following section, these components are chosen by searching catalogs of various producers in the market by considering design requirements.

4.2 Choosing Components for Design

Figure 4.1 shows that, switch, PLL, mixer, power amplifier and antenna are the main components of the system. Antenna can be connected later to the output of the board but other components have to be chosen. FPGA is chosen to be used to design digital circuits to configure these components.

Emitters operating in 3 - 4 GHz band region are considered and the starting point to search these components must be their operating frequency. All of the other requirements will be considered in detail such as IP3, SFDR, harmonics, noise and gain in the following sections. Choices are made by considering the components that can be supplied at first. Purchasing of all of these components is another process. Because many vendors do not sell components for small quantities. Another problem is that, these components have to be in their stocks. Consequently, in other words, choices are limited. In the following sections, important points for choosing these components are explained. Some definitions which are important for component selection are given. Finally the specifications for the selected components are described.

4.2.1 Phase Locked Loop

The first element that is considered is PLL, which synthesizes frequency. Basic diagram of PLL is shown in Figure 4.2.

Basically the way that PLL works is there is a fixed crystal frequency, f_{osc}, which is divided to obtain a comparison frequency, f_{comp}. Phase detector compares f_{comp} to f_n, which is obtained after the output frequency divided by n. If the frequency of both signals are same, phase detector puts out only very small corrections. If $f_n > f_{comp}$, it sinks current. If $f_n < f_{comp}$, it sources current. The loop filter is a low pass filter that converts these current corrections into a voltage. Then, VCO converts this voltage to a frequency. This output frequency, f_{out} is divided down by the N counter and compared to f_{comp}. So, the PLL basically steers the voltage to VCO such that $f_n = f_{comp}$.

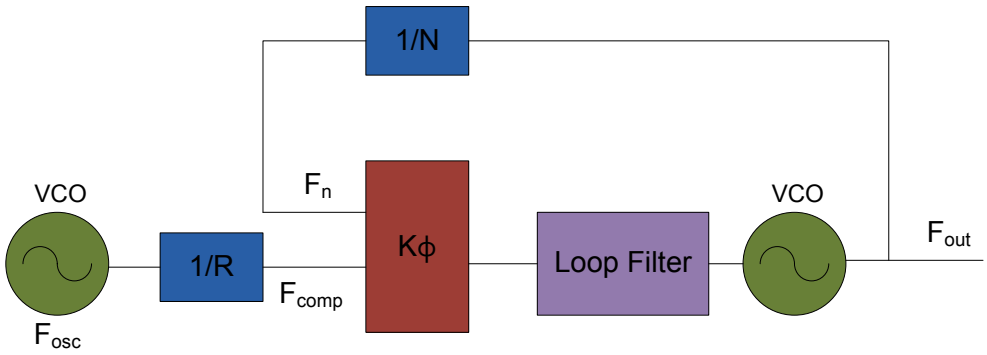

Figure 4.2: Basic PLL Block Diagram

The reason that VCO cannot be simply driven by a DAC is that VCO's have wide process variations and the output frequency cannot be accurately determined by the input voltage. Typically, the crystal frequency, f_{osc}, is very stable, but is limited to much lower frequencies [6]. PLL also provides very important advantage that the N counter can be changed by programming it to different values. This allows the PLL to be able to synthesize many different frequencies from a fixed frequency. On the other hand, designing wideband radar emulator is the aim of this chapter. Therefore, details of how PLL works and types are not covered. So, ADF4350 wideband synthesizer with integrated VCO is chosen to be used in this thesis. The ADF4350 allows implementation of fractional-N or integer-N PLL frequency synthesizers if used with an external loop filter and external reference frequency. Functional block diagram of ADF4350 is shown in Figure 4.3. Schematic of the ADF4350 is shown in Figure 4.4. ADISimPLL program report, frequency domain and time domain characteristics are indicated in APPENDIX C.

ADF4350 frequency range varies from 137.5 MHz to 4400 MHz which satisfies 3 - 4 GHz band coverage for design. 3 - 4 GHz band is supplied by integrated VCO with a fundamental frequency ranging from 2200MHz to 4400MHz. In addition, divide-by-1/2/4/8 or 16 circuits allows generating RF output frequencies as low as 137.5 MHz. Those output frequencies can be programmed by a reference oscillator and writing correct bits to registers of PLL. From the basic PLL operation f_{out} is divided by N to obtain f_{comp}. In ADF4350 N-divider allows division ratio in the PLL feedback path. This division ratio is determined by INT, FRACT and MOD values, which build up this divider. f_{out} can be calculated as in (4.1) [7]. f_{pfs} is the term that is presented by

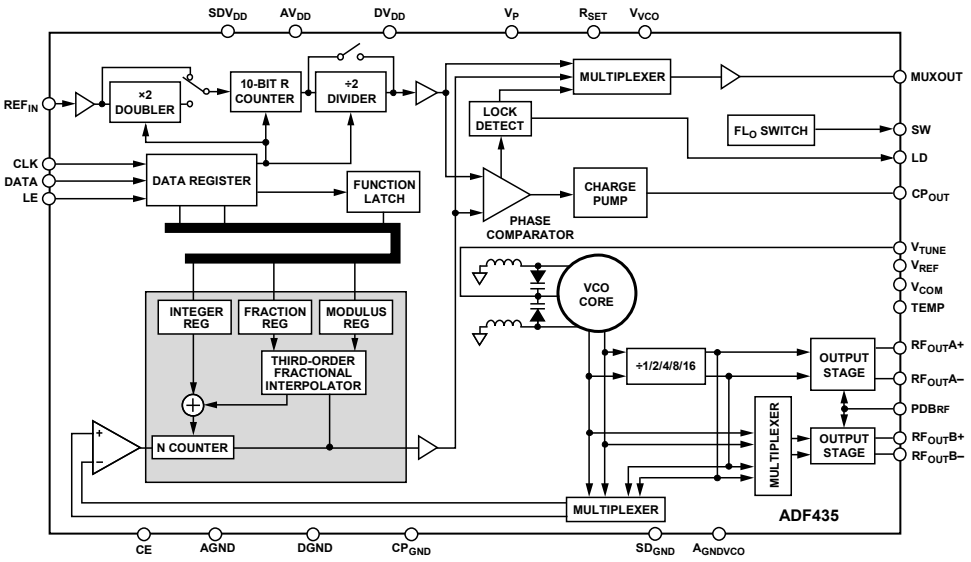

Figure 4.3: Functional Block Diagram of ADF4350

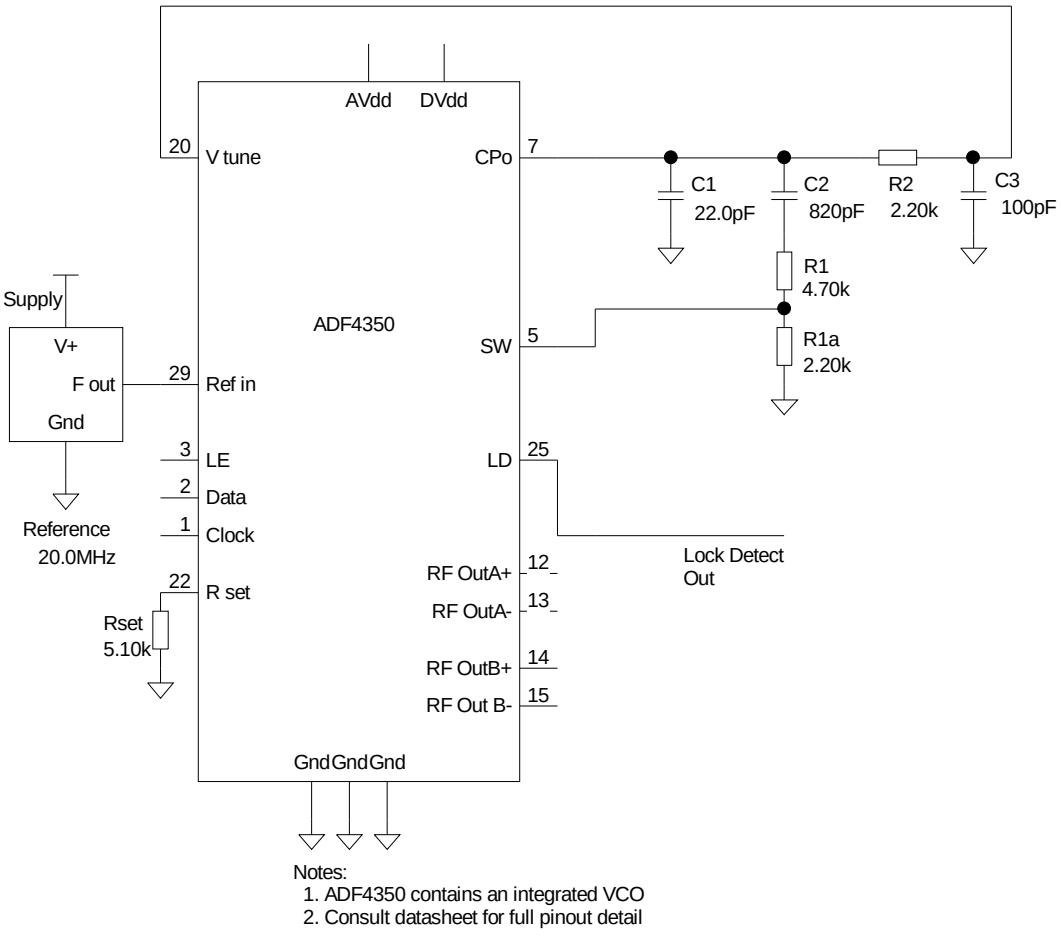

Figure 4.4: Designed Schematic of ADF4350

ADF4350 and is equal to the f_n in the previous representation.

$$f_{out} = f_{pfd}.(INT + \frac{FRACT}{MOD}) \tag{4.1}$$

f_{out} is the output frequency of external VCO. INT is the preset divide ratio of the binary 16-bit counter. MOD is the preset fractional modulus. FRACT is the numerator of the fractional division 0 to MOD-1.

$$f_{pfd} = f_{osc}\frac{1+D}{R(1+T)} \tag{4.2}$$

f_{osc} is the reference input frequency. D is the f_{osc} doubler bit. T is f_{osc} divide by 2 bit (0 or 1). R is the preset divide ratio of the binary 10 bit programmable reference counter (1 to 1023). Our requirement is to obtain frequencies between 3 and 4 GHz. 1 MHz steps are chosen which means that one thousand different frequencies can be synthesized. By using 20 MHz crystal as f_{osc} and 1 MHZ as f_{res}, f_{pfd} can be calculated. From (4.2) f_{pfd} is equal to 20 MHz.

$$MOD = \frac{f_{osc}}{f_{res}} \tag{4.3}$$

MOD value is chosen 20, INT value varies from 150 to 200 and FRACT value varies from 0 to 19. These values can be changed by writing correct bits to the registers of ADF4350. These design issues are simulated by using ADIsimPLL. This program is basic software for PLL products of AnalogDevices. Basically the model and the other requirements are chosen through ADIsimPLL and by choosing the desired configuration. The output of the program presents frequency and time domain characteristics of PLL design at final stage. Furthermore, these characteristics can be summarized as PLL that is being used has to produce a range of equal spaced output frequencies. All channels have to be checked that those channels can be generated. 1 MHz channel spacing is sufficient for design and by using ADIsimPLL, phase detector frequency will be determined automatically. 20 MHz reference oscillator is used as input to PLL [8]. Lock detect will be an open drain type.

Noise characteristics from data sheet give idea for our final signal at the output of PLL. Those characteristics are given in Table 4.1.

PLL is being used in this thesis in a closed loop application. Hence, noise characteristics of PLL in a closed loop application must be considered. Moreover, these characteristics affect performance of system. Figure 4.5, Figure 4.6 and Figure 4.7 gives

Table 4.1: VCO Phase Noise Performance

Typical Value	Unit	Condition
-89	dBc/Hz	10 kHz offset from 2.2 GHz carrier
-114	dBc/Hz	100 kHz offset from 2.2 GHz carrier
-134	dBc/Hz	1 MHz offset from 2.2 GHz carrier
-148	dBc/Hz	5 MHz offset from 2.2 GHz carrier
-86	dBc/Hz	10 kHz offset from 3.3 GHz carrier
-111	dBc/Hz	100 kHz offset from 3.3 GHz carrier
-134	dBc/Hz	1 MHz offset from 3.3 GHz carrier
-145	dBc/Hz	5 MHz offset from 3.3 GHz carrier
-83	dBc/Hz	10 kHz offset from 4.4 GHz carrier
-110	dBc/Hz	100 kHz offset from 4.4 GHz carrier
-132	dBc/Hz	1 MHz offset from 4.4 GHz carrier
-145	dBc/Hz	5 MHz offset from 4.4 GHz carrier

information about noise characteristics from datasheet of PLL in a closed loop application in 2.2 GHz, 3.3 GHz and 4.4 GHz respectively. More detailed information is available in [7].

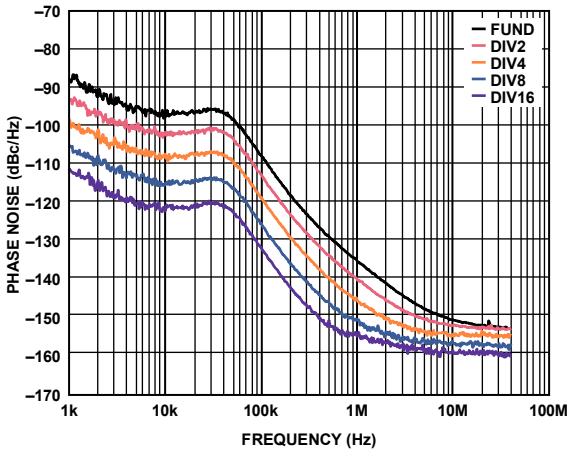

Figure 4.5: Closed-Loop Phase Noise, Fundamental VCO and Dividers, VCO = 2.2 GHz, PFD = 25 MHZ, Loop Bandwidth = 40kHz

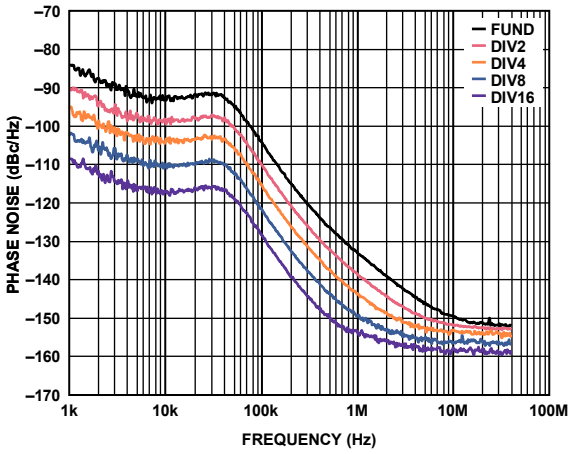

Figure 4.6: Closed-Loop Phase Noise, Fundamental VCO and Dividers, VCO = 3.3 GHz, PFD = 25 MHz, Loop Bandwidth = 40kHz

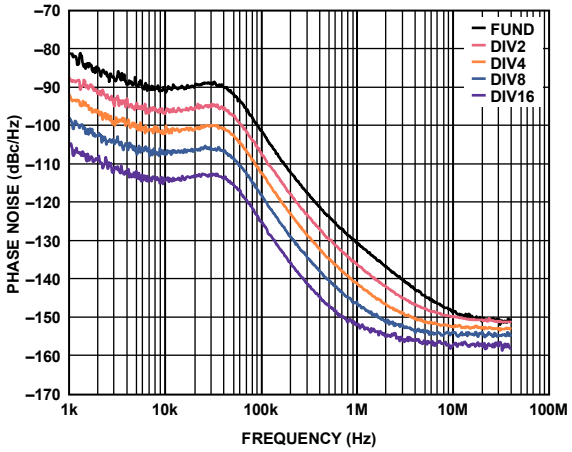

Figure 4.7: Closed-Loop Phase Noise, Fundamental VCO and Dividers, VCO = 4.4 GHz, PFD = 25 MHz, Loop Bandwidth = 40kHz

Furthermore, some other parameters such as frequency lock time, output phase error, frequency error and lock detect output characteristics of PLL can be plotted after simulations performed in ADIsimPLL. Use of different loop filter affects performance of PLL. Likewise, during simulations optimizations can be performed and the resulting PLL's time domain and frequency domain characteristics are summarized in Figure 4.8, Figure 4.9, Figure 4.10 and Figure 4.11.

Harmonics is also another issue when using fundamental VCO output. Second harmonic values are -19 dBc and third harmonic content is -13 dBc. RF output ranges from -4 dBm to 5 dBm which is programmable with 3 dB steps. Output power variation

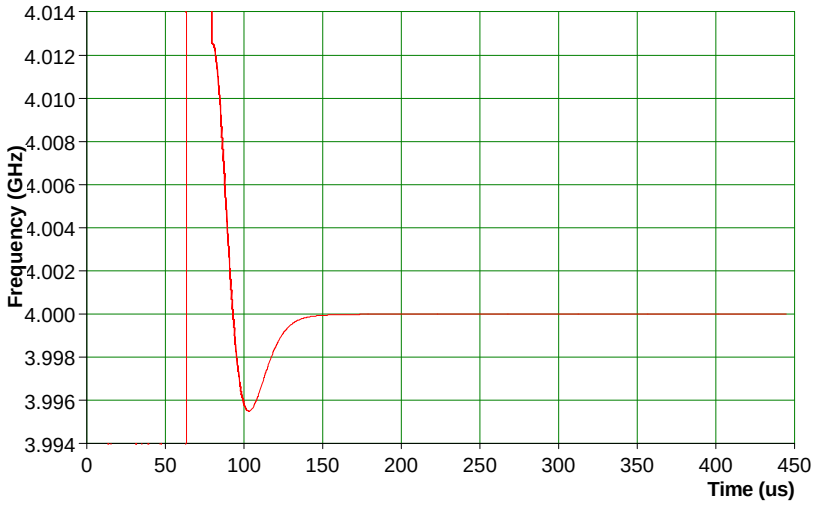

Figure 4.8: Frequency Lock Time

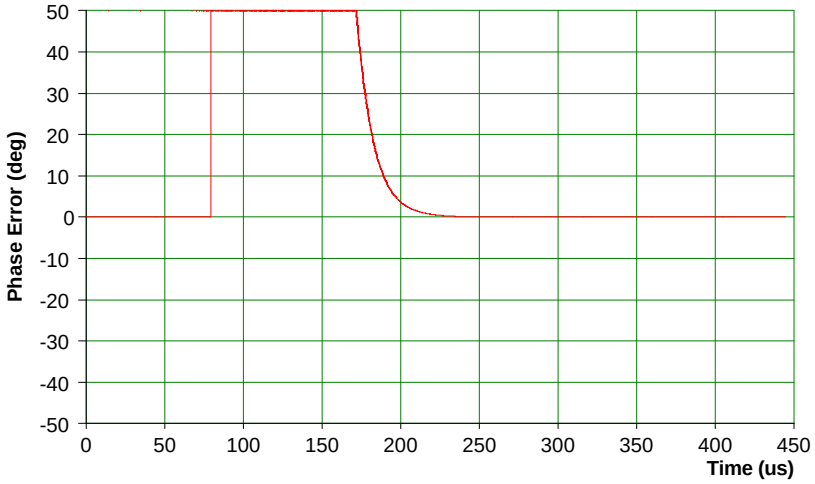

Figure 4.9: Output Phase Error

is $\pm$ 1 dB. Differential outputs can be used single without combining these outputs after shifting phases. It is possible to have the signal at the output at 10 dBm level when combining these outputs with a transformer. In this case unused outputs must be muted by finalizing them in a proper way. For applications that require isolation, when PLL is not in use, RF output stage can be muted. Mute function is both pin and software controllable. There are auxiliary RF outputs, which can be powered down if not in use. In order to test carrier frequencies, these outputs are finalized with SMA connectors. Besides, all of these characteristics of PLL are useful for system simulations which will be performed in AWR Microwave office.

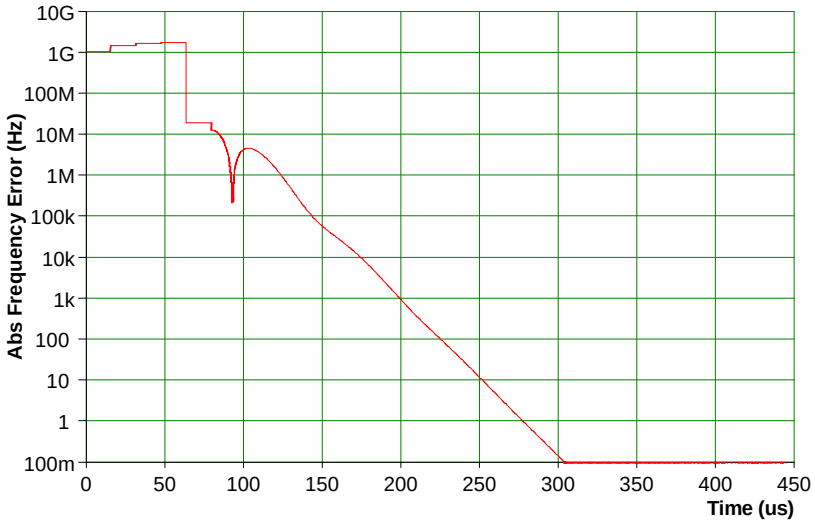

Figure 4.10: Frequency Error

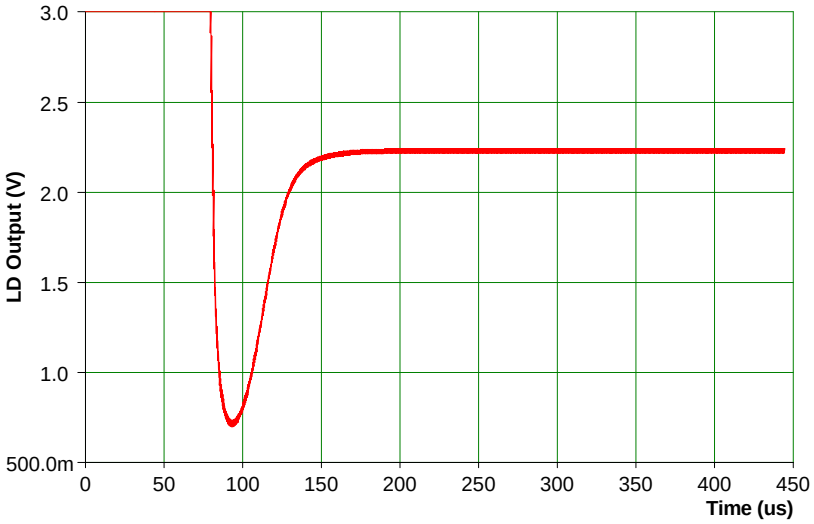

Figure 4.11: Lock Detect Output

4.2.2 Mixer

Mixers are frequency translation devices which convert signals between a high frequency (RF) and a lower Intermediate Frequency (IF) or baseband. In communications systems RF is the transmission frequency, which is converted to an IF to allow improved selectivity (filtering) and an easier implementation of low noise and high gain amplification [5]. The basic mixer design entails injecting the signals to be mixed and extracting the desired mixing product whilst maximizing the efficiency of the conversion. In this thesis, mixer is used to multiply video signal and RF signal as seen from Figure 4.1

to obtain desired pulse train at the output. Behaviors of mixers can cause problems if its characteristics are not understood. On the other hand, if specifications of mixer is known well, possible problems, which may happen, can be anticipated previously. One significant problem with mixers is that in addition to the wanted product, there are also numerous unwanted spurious products, often referred to as spurs. Figure 4.12 shows an example of a mixer's spectral output.

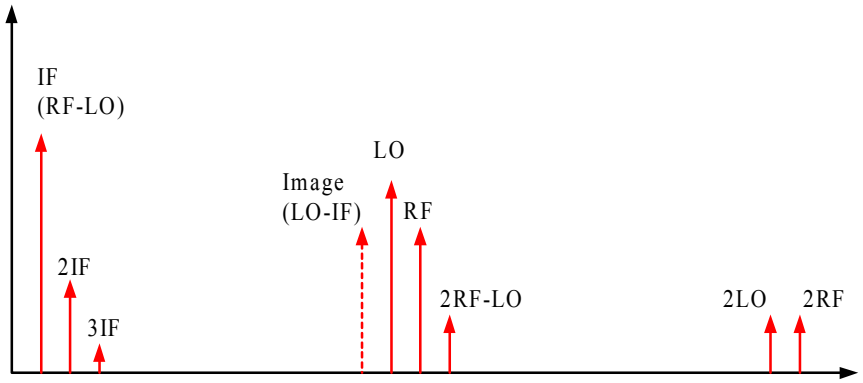

Figure 4.12: Mixer Spectral Output

As seen from the Figure 4.12, LO is mixed with the wanted RF signal to produce a copy of the RF signal at the difference frequency (IF). In general, mixer will generate outputs at a range of frequencies given by $mRF \pm nLO$. The spectrum shown in Figure 4.12 has an LO frequency below the IF, this is known as low side injection. One frequency of particular importance is the image frequency. This is $2IF$ away from RF and will be converted directly to the same IF frequency as RF. Noise and unwanted signals present at this frequency can severely degrade the system performance. Filtering and/or image reject mixers are normally incorporated to address this problem. In the case of upconverting mixers the input signal is IF and the desired output signal is either the product or difference of LO and IF frequencies, depending whether high side or low side injection is being used. If wanted output is ($LO+IF$), the difference product ($LO-IF$) is termed as the unwanted sideband, or image and must be rejected by filtering or the use of an image reject mixer. Most mixers incorporate some form of filtering which helps to reduce the levels of the unwanted spurious output. Another commonly used technique, which helps to reduce spurious output, is the use of balanced mixers. Without going into details about types of mixers, the definitions of some important

parameters to be considered in this design are given. The mixer that is used in this thesis is HMC615LP4E from Hittite Microwave. HMC615LP4E have an integrated amplifier. Some of the important characteristics are listed in Table 4.2. Specifications of this mixer is explained in the definitions below. More detailed information about HMZ615LP4 can be found in [9].

Table 4.2: Electrical Specifications of HMC615LP4E

Parameters	Value	Units
Frequency Range, RF, LO	2.3-4.0	GHz
Frequency Range, IF	DC-1	GHz
Conversion Loss	10	dB
Noise Figure (SSB)	10	dB
LO to RF Isolation	15	dB
LO to IF Isolation	10	dB
IP3 (Input)	35	dBm
1 dB Compression (Input)	21	dBm
LO Drive Input Level (Typical)	-2 to +6	dBm

Conversion Loss: The ratio of the wanted output signal level to the input, normally expressed in dB. Conversion loss is a measure of the efficiency of the mixer in providing frequency translation between the input RF signal and the output IF signal if mixer is operating in downconversion mode. In upconversion mode input is IF signal and output is RF signal. For a given frequency translation, two equal output signals are produced which are lower sideband and upper sideband signal. Since only one sideband is generally of value, the specifications given in here are for a single sideband output. If two sidebands are useful, then the conversion loss is 3 dB lower than in the single sideband case. Conversion gain of HMC615LP4E specifications can be given versus temperature and LO drive in Figure 4.13 and Figure 4.14 respectively.

Noise Figure: In practice, detection of signals is limited by the amount of noise that accompanies the signal at the receiver relative to the strength of the signal. Thermal noise in circuits is caused by the heating of electrons. Electrical current flow can be

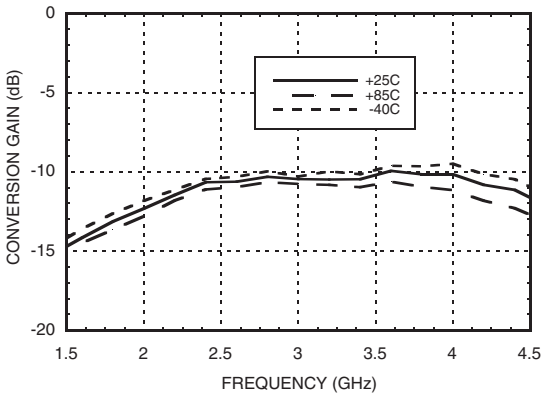

Figure 4.13: Mixer Conversion Gain vs. Temperature (LO = 4dBm)

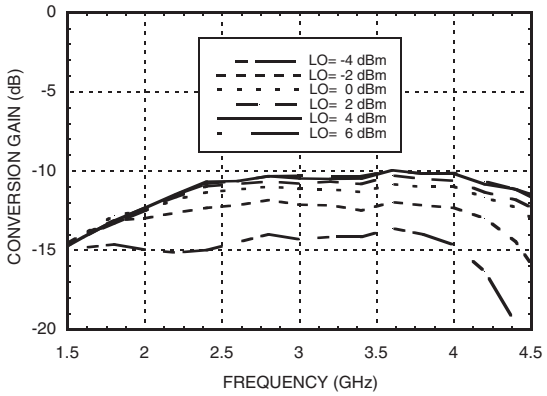

Figure 4.14: Conversion Gain vs. LO Drive

thought of as controlling the direction of this random motion in one direction or another. The actual motion of electrons can only be determined statistically, however, and the random motion of these electrons causes noise. Ideal electronic components are only an engineering approximation. Every capacitor, inductor and semiconductor has an associated resistance. It is within this resistance that the noise generation occurs. Each circuit generates thermal noise, some of which is added to signal. When all of these noise sources have their effects reflected to the signal input stage, the noise figure results, denoted by F. The noise can be summarized in the equivalent system noise, N, given by (4.4).

$$N = kTBF \tag{4.4}$$

k is Boltzman's constant, $k = 1.38x10^{-23}$ joules per degree Kelvin, T is the absolute temperature measured in degrees Kelvin. B is the noise bandwidth in Hertz and F is the system noise figure with no units [10]. Noise factor is the signal to noise ratio at the input of a module or cascade divided by the signal to noise ratio at its output. Noise figure (NF) which is expression of noise factor in dB and is a measure of degradation

of the signal to noise ratio (SNR), caused by components in the RF signal chain [5]. The noise figure is the ratio of the output noise power of a device to the thermal noise in the input termination at standard noise temperature T_0 (usually 290°K). The noise figure is thus the ratio of actual output noise to that figure which would remain if the device itself did not introduce noise. It is a number by which the performance of a radio receiver can be specified. The ratio of SNR at the input can be compared to the SNR at the output and can be formalized as in (4.5).

$$NF = \frac{SNR_{in}}{SNR_{out}} \tag{4.5}$$

Alternatively, noise figure can be defined in terms of dB units as in (4.6).

$$NF_{dB} = 10log(\frac{SNR_{in}}{SNR_{out}}) = SNR_{in,dB} - SNR_{out,dB} \tag{4.6}$$

The equation given in (4.6) is only valid when the input termination is at standard noise temperature T_0. These definitions are equivalent, differing only in the use of dB units. The first definition is sometimes referred to as noise factor to distinguish it from the dB form. Two types of NF can be defined as follows;

- Double Sideband (DSB) Noise Figure: Includes noise and signal contributions at both the RF and the image frequencies.
- Single Sideband (SSB) Noise Figure: No image signal is included although image noise is included. Single sideband gain of a mixer is measured by taking only one sideband of the output signal [5]. SSB noise factor is equal to twice the DSB noise factor.

Second and Third Order Intercept Point: Intercept points are figures of merit to give an indication of mixer's signal handling capability [5]. Third order intercept point is a theoretical point on the RF input versus IF output curve where the desired input signal and third order products become equal in amplitude as RF input is raised. In particular, this rise provides an indication of the levels of third order products of a mixer, which is likely to produce under multi-tone excitation. Intercept points are measured by applying two closely spaced input tones at frequencies F_1 and F_2. Second order terms are calculated as in (4.7) and (4.8).

$$F_{IP_21} = F_1 - F_2 \tag{4.7}$$

$$F_{IP_22} = F_2 - F_1 \tag{4.8}$$

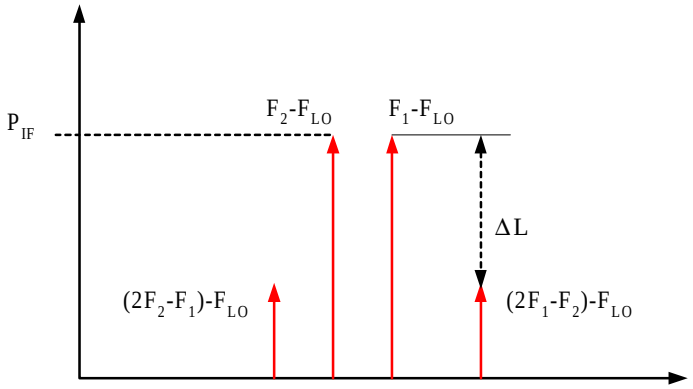

Figure 4.15: IF Spectrum for Mixer Third Order Intercept Point Measurement

Third order terms can be calculated as in (4.9) and (4.10).

$$F_{IP_31} = 2F_1 - F_2 \tag{4.9}$$

$$F_{IP_32} = 2F_2 - F_1 \tag{4.10}$$

Third order products from mixing of these tones with the LO (at frequency F_{LO}) occur at frequencies given by (4.11) and (4.12).

$$F_{IP_3Mixer1} = (2F_1 \pm F_2) \pm F_{LO} \tag{4.11}$$

$$F_{IP_3Mixer2} = (2F_2 \pm F_1) \pm F_{LO} \tag{4.12}$$

In the case of a downconvert mixer, as seen from equation (4.11) and (4.12), third order products of most interest are $(2F_1 - F_2) - F_{LO}$ and $(2F_2 - F_1) - F_{LO}$, which are given in Figure 4.15, as they fall in, or close to the IF band. So, instead of harmonics, IP3 value is important because it is in or close to the operating frequency band. Figure 4.15 depicts the IF output spectrum of a downconvert mixer under two-tone excitation. The third order intercept point itself is an entirely imaginary point, at which the third order product becomes as large as the direct downconverted product. Assume that F_1 and F_2 signals have equal power P and power of the products F_{IP_21} and F_{IP_22} is P'. The value of IP2 and IP3 can be calculated as (4.14) and (4.15).

$$\triangle L = P - P' \tag{4.13}$$

$$IP2 = P + \triangle L \tag{4.14}$$

$$IP3 = P + \frac{\triangle L}{2} \tag{4.15}$$

The level of the third order products rises at three times the rate of increase of the input signal level and fundamental output level. The mixer's output referred to as third

order intercept point ($IP3$) is given by equation (4.15), all values are in dB and it is the dB value of $\triangle L$ which is divided by 2. A convenient way to describe intermodulation products relative to input signal level is to state the relative difference between the two in dB; for example, a mixer may be specified as 60 dB down for two -20 dBm input signals. This means the mixer, with two -20 dBm signals at its input, will suppress third order products by 60 dB. If the input level is reduced by an additional 10 dB, the third order product level would decrease by a factor of three, or 30 dB. The difference between the two would be 20 dB and thus, the mixer would offer 80 dB suppression with two -30 dBm signals at its input. With another 10 dB drop in signal level, third-order products would drop another 30 dB with a difference of 20 dB between the two. Thus, two -40 dBm signals would produce third order products suppressed by 100 dB. The original input levels were -20 dBm and thus, the third-order products were 60 dB lower, or -80 dBm. Furthermore, if the input is raised by 30 dB to +10 dBm, the third order products would be increased by a factor of three or 90 dB; a 90 dB increase added to the original -80 dBm is +10 dBm, thus establishing equal amplitude for the desired and distorted signals. Graphically, the intercept point is obtained by linearly extending the desired signal curve past the compression point until it intersects the third order curve.

Conversion Compression: Conversion compression is a measure of the maximum RF input signal for which the mixer will provide linear operation. Each dB increase in signal level results in a dB increase in the output signal level for small input signal levels. As the input signal level continues to increase; conversion loss of the mixer will eventually start to increase. 1 dB compression point is the input signal level at which the conversion loss has increased by 1 dB. Mixers should be avoided to be used in 1 dB compression region because of its addition to distortion of the wanted signal. Consequently, operation at or close to 1 dB compression point would give rise to significant increases in the levels of the spurious outputs. Normally, IF output signal level is equal to a constant ratio of RF input signal level. However, when RF signal level is within 10 dB of the drive level, the constant ratio between IF and RF levels will exhibit a change of about 0.1 dB. As the RF level increases further, there will be a greater change in the constant ratio. The conversion loss will increase as the RF input level increases. The IF output level does not exactly follow the increase in RF input level. The criterium used to describe the deviation from linearity between the RF input level and the IF output level is a fixed amount of compression. Naturally, if a higher compression point were selected, the corresponding RF input level would be higher. Conversion compression provides an

indication of the mixer with two tone performances. The compression point is useful when selecting a mixer for maximum linear operation. The compression point will change as a function of LO drive level. Therefore, it is meaningful to specify the actual LO drive level when discussing the compression point. Conversion loss desensitization is a measure of the non-linearity caused by an unwanted RF signal at the mixer input. When the undesired RF input level causes the mixer conversion loss to increase by 1 dB, for the desired low level RF input signal, then the 1 dB desensitization level is reached and the maximum undesired RF input level is defined. Therefore, 1 dB compression point can be defined as in (4.16), which is another rule of thumb and widely used. P_{IP3} in the equation is input third order intercept point. This equation is not valid in a lot of cases where nonlinearity is high.[11]. HMC615LP4E mixer is a high IP3 component where its IP2 and IP3 characteristics are given in Figure 4.16 and Figure 4.17, respectively.

$$P_{1dB} = P_{IP3} - 9.6 \tag{4.16}$$

Dynamic Range: The power range over which a mixer provides useful operation is

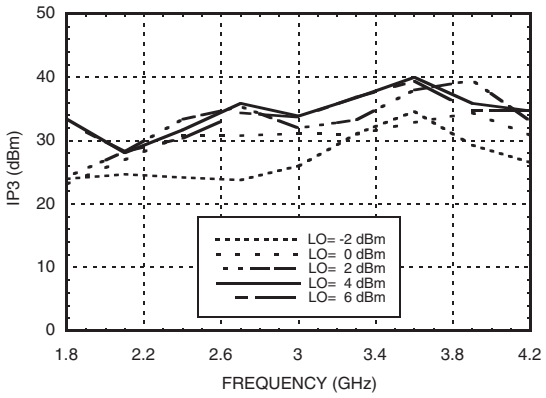

Figure 4.16: Input IP3 vs. LO Drive

called dynamic range. Upper limit of the dynamic range is limited by the conversion compression point. The lower limit of the dynamic range is limited by the noise figure of the mixer. Since the mixer noise figure is only about 0.5 dB higher than its conversion loss, the lowest conversion loss is desirable to obtain the largest dynamic range. In other words, dynamic range is also called spurious free dynamic range (SFDR) which characterizes the ratio between the fundamental signal and the highest spurious in the

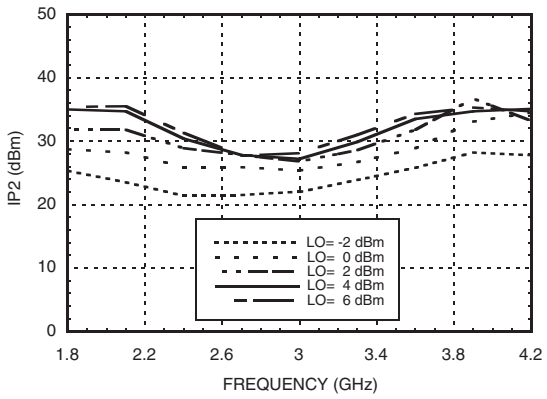

Figure 4.17: Input IP2 vs. LO Drive

spectrum.

$$SFDR = 20log\frac{P_{fundamental}}{P_{HighestSpurious}} \tag{4.17}$$

SFDR can be calculated as in (4.17). Sometimes harmonics are included in SFDR calculation and in this case, the highest spurious product will be power of harmonics.

Another important parameter is isolation. Because, mixers have signals in different frequencies flowing through its different pins. Therefore, if those signals are not isolated well, obvious degradation may occur. HMC615LP4E isolation and return loss specifications are given in Figure 4.18 and Figure 4.19, respectively. More detailed information is available in [9].

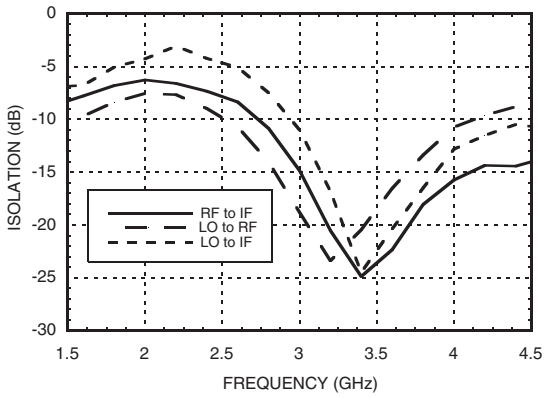

Figure 4.18: Isolation (LO = 4dBm)

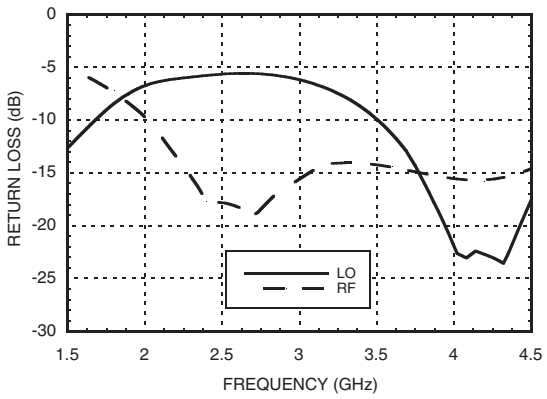

Figure 4.19: Return Loss (LO = 4dBm)

4.2.3 Amplifier

Main characteristics of an amplifier are linearity, efficiency, output power and signal gain. In general, there is a trade off between these characteristics. For example, improving amplifier's linearity will degrade its efficiency. Therefore, knowing the importance of each of these characteristics leads one to make correct design. For instance, high output power amplifier is used in the transmitter side of a transceiver, whereas high linear amplifier is used in the receiver side. Power amplifier of RFMD company is chosen for thesis which is SZP-3026ZDS with maximum output power of 2 Watts; because, not only this amplifier has 3 - 4 GHz operating frequency, but also it has high output power. Some specifications of SZP-3026ZDS are given in Table 4.3 [12]. More detailed specifications of the amplifier are given together with definitions about power amplifier.

High frequency amplifiers are usually made of one or more transistor steps. Those transistors operate linearly until one point. Linear operating region depends on base current and collector/emitter voltage. Base current has an importance, because it affects noise characteristics of an amplifier. If it is assumed that transistors, which the amplifier is made of, are not linear and if high amplitude signals are performed on the input of that amplifier, those transistors will distort the shape of signal by producing undesired signals. This is called Inter Modulation Distortion (IMD). Once IP3 and IP2 characteristics of an amplifier are known, IMD can be calculated. Detailed explanations about IP3 and IP2 are given in the previous sections. For amplifiers, IP2 and IP3 values are a measure of handling capacity with high amplitude input signals. In datasheets of amplifiers, OIP (Output Intercept Point) values are specified sometimes instead of IP3.

Table 4.3: SZ3026ZDS Specifications

Parameter	Specification	Unit	Condition
Frequency Operation	3000 - 3800	MHz	
Output Power at 1dB Compression	33.2	dBm	3.5 GHz
Small Signal Gain	10.5 - 12.0	dB	3.5 GHz
TOI (Pout=23dBm per tone)	-43 - -40	dBc	3.5 GHz
Noise Figure	5.1	dB	3.5 GHz
Input Return Loss (Worst Case)	14 - 18	dB	3.4 - 3.6 GHz
Output Return Loss (Worst Case)	7 - 10	dB	3.4 - 3.6 GHz
V_{out}; P_{out} = 10dBm to 33 dBm	0.9 - 2.2	V	
Quiescent Current (Vcc = 5V)	347 - 385 - 424	mA	
Power Up Control Current (Vpc = 5V)	2.3	mA	
V_{cc} Leakage Current (Vcc = 5V, Vpc = 0V)	max. 100	μA	

OIP, which is measured at the output of an amplifier, is different than IP3. The value of OIP can be confusing. Because, gain of an amplifier is taken into account which gives higher values than IP3 when calculating OIP. Figure 4.20 and Figure 4.21 are specifications which are about SZP3026ZDS's intermodulation and gain, respectively.

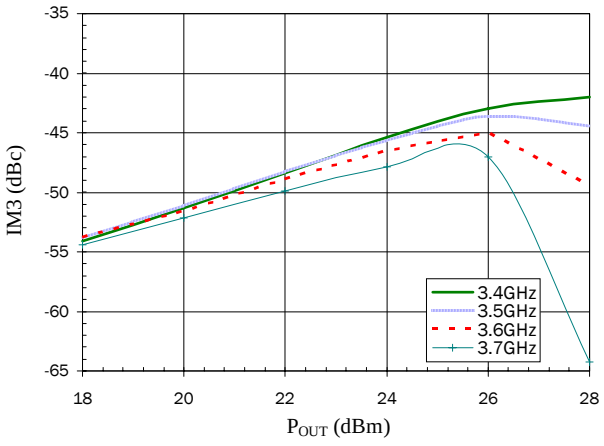

Figure 4.20: IM3 vs. P_{out} (2 Tone Avg.), $T = 25°C$ Tone Spacing = 1 MHz

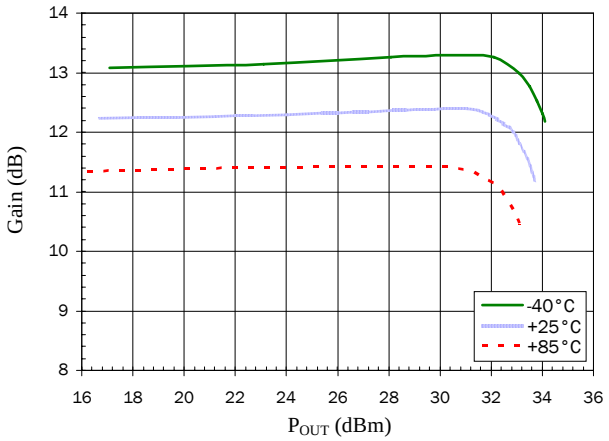

Figure 4.21: Typical Gain versus P_{OUT}, F=3.4 GHz

In practice, IP3 is important because this value quickly improves and distorts the output as given in the previous sections. After calculating IP3, compression point of an amplifier is 9.6 dB below from IP_3 point as given in (4.16) which means, if amplitude of input signal of an amplifier is increased by 1 dB from IP3 value, the signal at the output is attenuated by 1 dB. Therefore, amplifier produces second and third order harmonics. Much higher IP2 and IP3 points are desired in amplifiers. Besides, it is not possible in practice. Because base current must be increased to obtain high IP2 and IP3 values. If base current increases, noise characteristics of an amplifier increase too, which means there is a trade off between noise and IP3. In this case, design requirements must be considered. Low noise ratio and medium level IP2 and IP3 values are usually chosen for TV and Radio receivers. In high signal environments such as cable TV systems, linearity is important for amplifiers. Therefore, noise level is higher than its normal value. Figure 4.22 gives specifications of SZP3026ZDS about noise figure versus frequency.

An amplifier is said to be linear if it preserves the details of the signal waveform as in equation (4.18) where, V_i and V_o are the input and output signals, respectively, and A is a constant gain representing the amplifier gain.

$$V_o(t) = A.V_i(t) \tag{4.18}$$

But, if the relationship between V_i and V_o contains higher powers of V_i, then the amplifier produces nonlinear distortion. Efficiency of amplifier is a measure of its ability to convert the DC power of the supply into the signal power delivered to the load. The definition

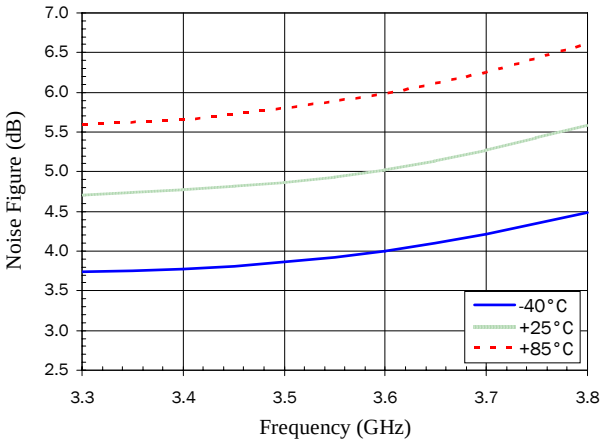

Figure 4.22: Noise Figure vs. Frequency

of the efficiency can be represented in (4.19).

$$\eta = \frac{Signal\ Power\ Delivered\ To\ Load}{DC\ Power\ Supplied\ To\ Output} \tag{4.19}$$

For an ideal amplifier, efficiency equals to one. Thus, power delivered to load is equal to power taken from DC supply. In this case, no power would be consumed in the amplifier. In practice, this is not possible, especially in high frequency implementation of RF circuits. Output and driver stage of an amplifier consumes power in the amplification process in many high frequency systems. The gain of an amplifier (G) is equal to the magnitude of the output signal (X_o) over the magnitude of the input signal (X_i) as shown in the equation.

$$G = \frac{X_o}{X_i} \tag{4.20}$$

Only some of the important characteristics about power amplifier are given. More detailed information is available in [12].

4.2.4 Switch

In this section, choice of the right switch is made by explaining types of switches and their specifications. Some of the switch terms, which are common in many components, were explained in the previous sections. There are some abbreviations for types of switches such as SPST (Single Push Single Throw) or SPDT (Single Push Dual Throw) which means, for SPST, switch has one input and one output and, for SPDT, switch has one input and two outputs. Isolation is the attenuation of the signal between input and output ports of the switch when the switch is in OFF state. VSWR indicates

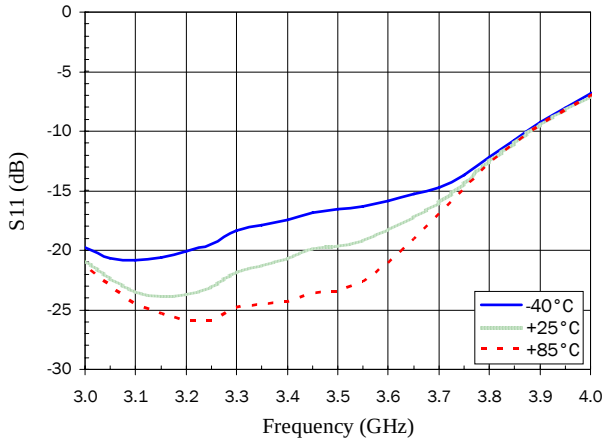

Figure 4.23: Narrowband S11 - Input Return Loss

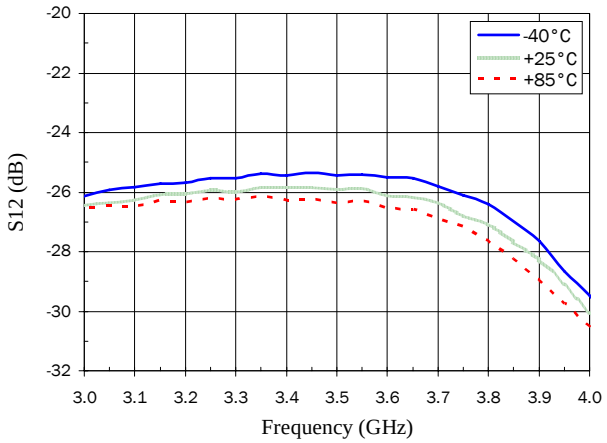

Figure 4.24: Narrowband S12 - Reverse Isolation

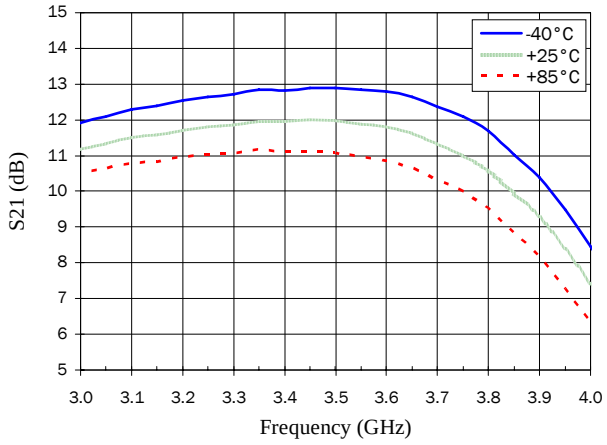

Figure 4.25: Narrowband S21 - Forward Gain

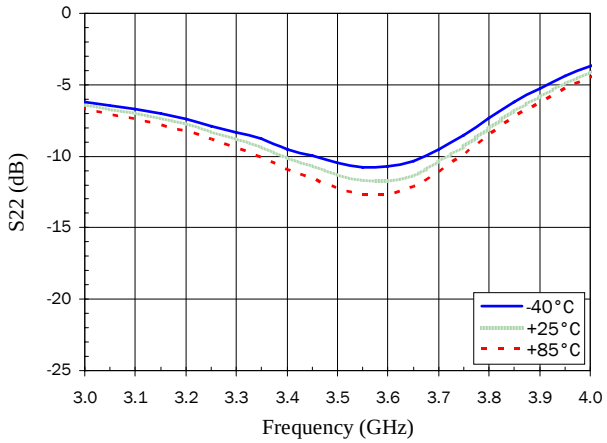

Figure 4.26: Narrowband S22 - Output Return Loss

the degree of impedance match present at the RF ports of the switch. In most cases, measuring return loss is chosen and VSWR can be calculated. Transients are defined as video transients, which occur during switching process, disturb RF components that connected to the switch. If lower transients are critical during the switching period, slower transition rate must be used between control states. Noise figure and 1 dB compression point definitions are made in the previous sections. However, for switches, it can be said that noise figure can be considered as equal to insertion loss of switch. 1dB compression point is the RF input power level at which the switch insertion loss increases by 1dB over low level value.

Moreover, use of switch brings to form two parameters of the pulse train in this design. These parameters, which are identical for radars, are pulse width and PRI. Switch must be driven by FPGA and must have short switching times to meet the requirements of radar pulse trains. Switch will be used as a pulse modulator. Therefore, isolation is important in this application. When switch is opened, high isolation between input and output ports of switch must be provided. Because, the signal at the RF input of mixer will be mixed with the signal at the output of the switch. Furthermore, if the leakage is not negligible, RF signal can be mixed at the output of the mixer with leakage voltage from the IF input of mixer when switch is opened. This causes generation of signal at the output of the amplifier. Moreover, even a more important characteristic for a switch is switching speed. Switching speed consists of rise time, fall time, on time and off time for the switch. These values determine the shape of pulse which is generated at the output of the amplifier.

Two types of switches are commonly used. These switches are PIN diode and GaAs switches. These RF switches can be generally driven with TTL drivers. There are some differences between PIN diode switches and GaAs switches. A PIN diode switch uses the PIN diode as the nonlinear element. So, PIN diode switches have low impedance and current in one direction, but high impedance and current in the opposite direction. Generally, PIN diode switches respond to the polarity of RF signal slowly at frequencies above approximately 10MHz. Therefore, the diode appears as a fixed impedance as low impedance for positive DC control current, high impedance for zero current or negative DC control voltage. The GaAs switch uses a GaAs FET as the nonlinear element, which is advantageous. Because, the transistor is in the fully "on" or fully "off" state depending upon bias conditions. A PIN diode switch is more tolerant of high peak power when using pulsed RF input, being limited mainly by average dissipation. However, power rating of a GaAs switch is determined more by internal peak voltage and current ratings. On the other hand, GaAs switches are faster, when switching. It takes few nanoseconds compared with microseconds for PIN switches. Moreover, GaAs switches have RF response extending down to DC, whereas in PIN switches there is a practical lower limit to the frequency range in which the diodes behave as linear resistors. The terms absorptive or reflective defines characteristics of switch. Absorptive switch brings good VSWR looking into the port that is not switched to the common port. Reflective switch is preferred, when high OFF port VSWR does not matter and when the switch has some other desired performance feature. In most cases, an absorptive switch can be preferred instead of reflective, but not vice versa. It will depend on the individual switch. Switch can be used as a modulator. So the highest modulating frequency can be calculated. The highest modulating frequency is given approximately in (4.21) [13].

$$f_{max} = \frac{1}{(T_{ON} + T_{OFF})} \tag{4.21}$$

In this thesis, SW90-0001 absorptive RF switch, which operates from DC up to 4GHz, is chosen. Switch is SPST type and can be driven with a TLL driver which allows driving switch through FPGA. Insertion loss is 0.85 dB maximum and isolation is 25dB minimum. VSWR of the switch in on or off state is 1.5:1. Input IP_3 of switch is 40dBm at 50MHz when two tone inputs are up to 5dBm. Rise time is 7ns from 10% to 90% and fall time is 2ns 90% to 10%. T_{ON} is 32ns which is time from 50% of the control pulse to 90% of the "on" level. T_{OFF} is 20ns which is time from 50% of the control pulse to 10% of the "on" level [14].

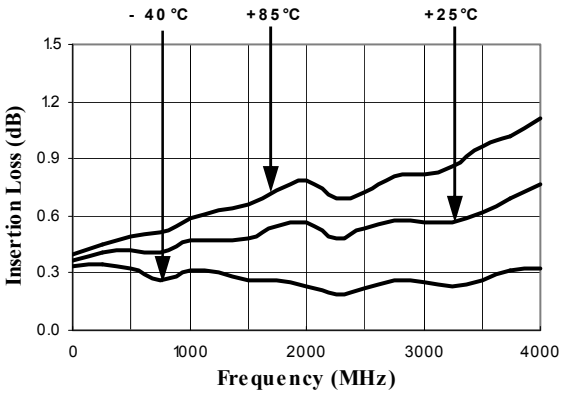

Figure 4.27: Insertion Loss vs. Frequency

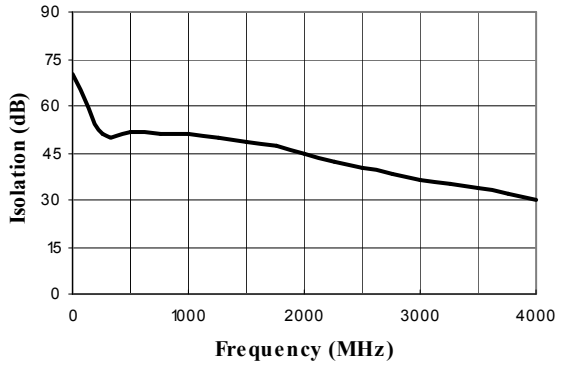

Figure 4.28: Isolation vs. Frequency

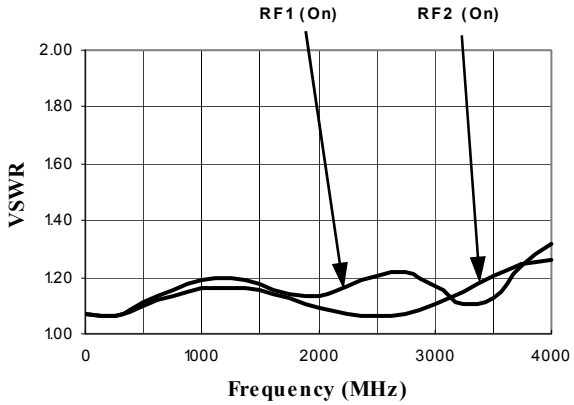

Figure 4.29: On VSWR vs. Frequency

4.2.5 FPGA

Xilinx Spartan 3E board is used to control all components such as PLL, switch and amplifier. Since the aim of this thesis is to emulate radar pulse trains, RF related parts of the design are mostly concerned. Hence, digital parts are not covered in details. The

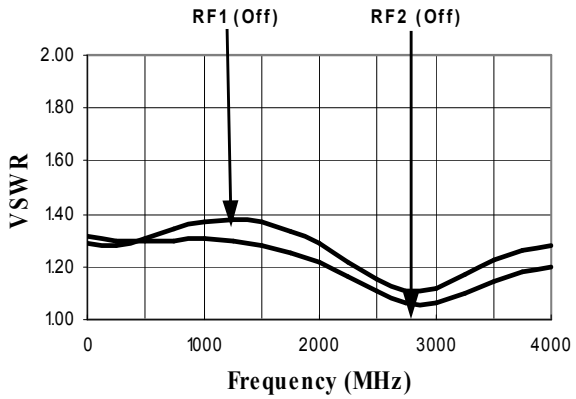

Figure 4.30: VSWR(Terminations) vs. Frequency

most important part in FPGA is generating the signal controlling envelope of pulse train which determines PRI and PW of the radar emitter to be emulated. Also the pattern for radar emitter is given to FPGA by using a PC. From Figure 4.1, the role of FPGA board can easily be understood. The picture of used board is given in Figure 4.31 and more detailed information about Spartan 3E is available in [15].

4.3 System Simulations

In the previous section, design requirements are covered and detailed explanations of those requirements are given. Moreover, important parameters to be considered in design are mentioned. Choosing all of the components is not enough to begin design of the circuit. Simulations must be performed to see possible missing design issues. Vendors of these components sometimes offer detailed behavior of their products. This information lets designers implement system design simulations. The program that is used for system simulations is AWR Microwave Office. In this section, the components are simulated through AWR. All of the specifications of components that are available must be entered to the program to get almost real simulation results. Graphical results are presented at the end of this section.

The block diagram of the system is given in Figure 4.1. A similar system is designed by using AWR as in Figure 4.32. AWR is a microwave simulation program which helps to simulate systems, schematics or electromagnetic structures of related designs. Simulations can be performed to know how the final system will behave. Some problems can be solved by this way and precautions can be taken. First of all, simulation of design

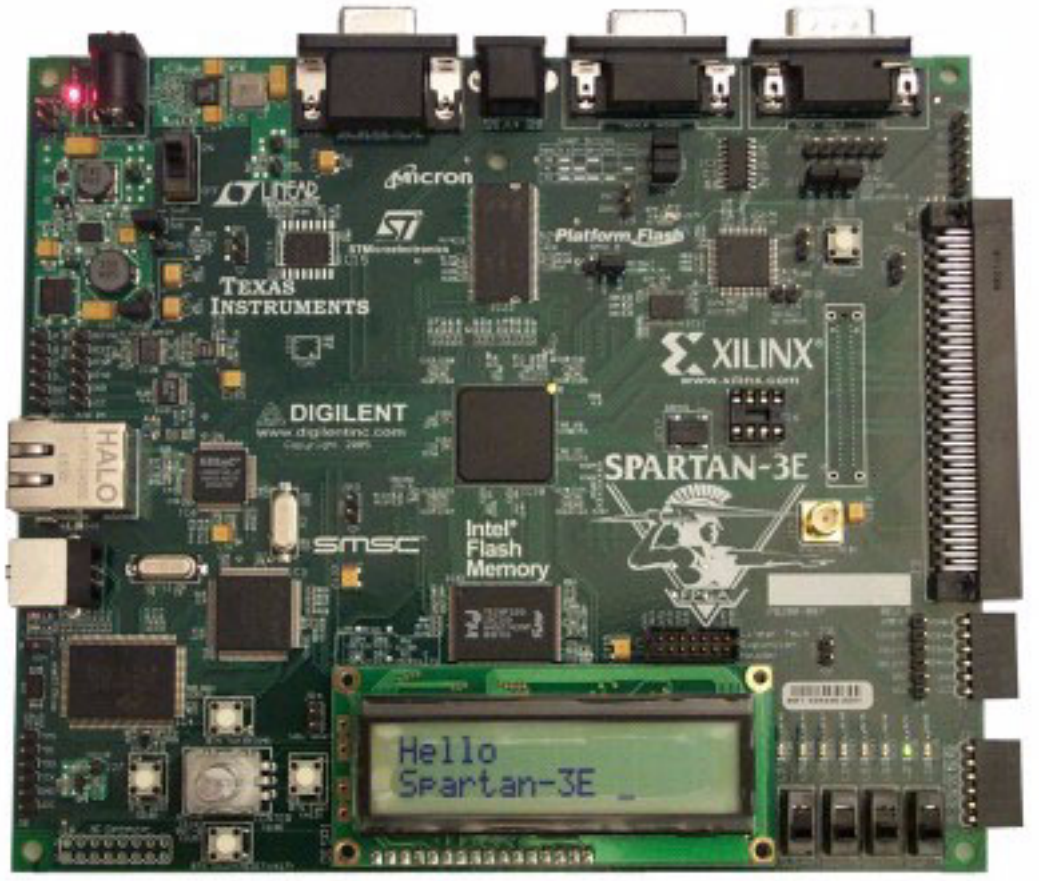

Figure 4.31: Spartan 3E FPGA Board

is required in system level. In order to achieve this, components of AWR are configured as the components in design. Data sheets of components give information about how to simulate those components. After building the system by blocks, simulation results will give information about RF output of design.

During simulations, there were some assumptions made when modeling components because it is impossible to find exact model of all components chosen for design. These simulations give information about the general behavior of the final system. It is not possible to obtain practical behavior of the system because there will be more effects that must be considered after circuit design and PCB design such as coupling, impedance matching and interference etc.

From Figure 4.32, the envelope of the signal is generated through a tone generator. This signal is carried to the IF input of the mixer. Duration of the pulse (PW) or time difference between consecutive pulses (PRI) can be set either by controlling the switch by on-off keying or by controlling the signal received from FPGA. Tone generator has

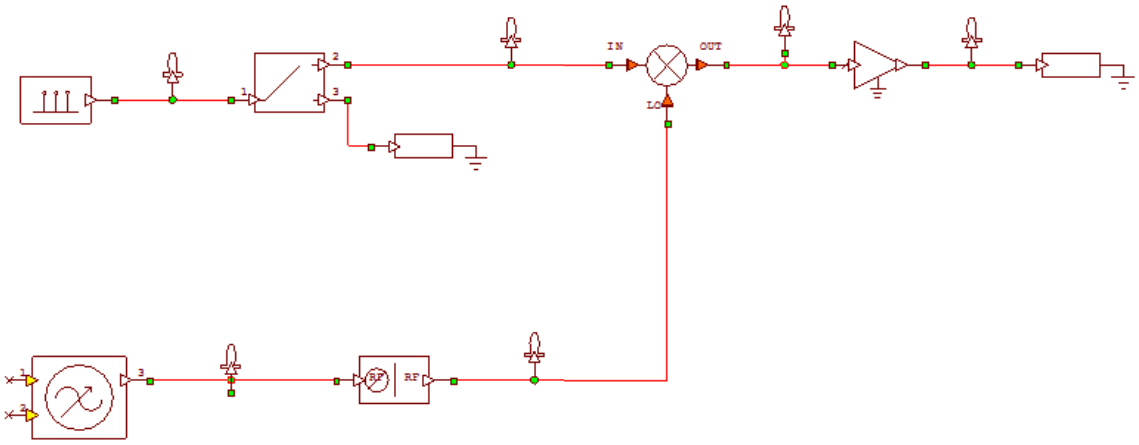

Figure 4.32: MWO System Diagram

to transmit Fourier transform of the pulse train which will be a sinc type function. The proper way is to implement all effects of the RF signal by generating a sinc type function of the desired pulse train and then adding the effects of the model of switch to that signal. Therefore, single frequency is generated through tone generator.

The other point is generating RF signal between 3 - 4 GHz. VCO model is used in order to simulate effects of the PLL. Because the PLL that is being used is a chip and has many capabilities to be modeled which is complex. The component that synthesizes frequency at the final stage inside PLL is VCO. So, VCO model is proper to be used during PLL modeling. Region of interest during these simulations is the output signal at the output of PLL. For the scope of this thesis, details of the PLL chip are not covered. Moreover, characteristics of the output signal are modeled by using specifications of PLL. Therefore, more detailed information about the output signal is counted, which is obtained from ADIsimPLL program.

After adding effects of mixer, resulting signal at the RF node is obtained. Spur table of mixer is configured in AWR while modeling. Other parameters such as conversion gain, 1 dB compression point, third order intercept point, local oscillator port power and noise figure of mixer are taken into account. Local oscillator port power uses determine higher order spur suppressions. Noise is modeled for both RF budget analysis and time domain simulations. Resulting signal at the mixer output can be seen from Figure 4.33. The obtained power levels at the output of the mixer are expected. Harmonic suppression levels from mixer specifications are almost same.

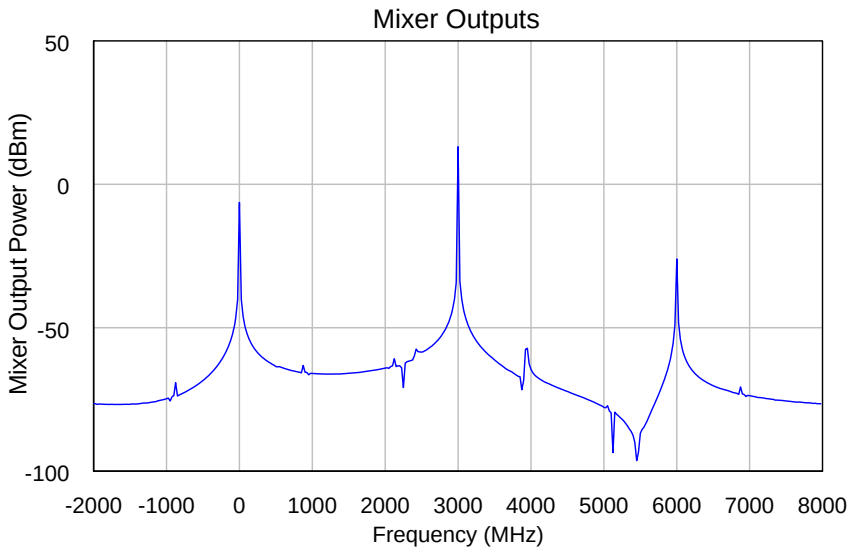

Figure 4.33: Mixer Output

The final stage in this design must be antenna to transmit signals. However, antennas are not covered for the scope of this thesis. Therefore, board has SMA connectors at the RF output. So, any kind of antenna can be used. The final stage is power amplifier and many effects such as IM products or spurs occur according to power amplifier. These effects are modeled in AWR. These parameters are gain, 1 dB compression point, third order intercept point, output power saturation level and noise figure. After configuring those parameters from data sheet of power amplifier, signal at the output can be given in Figure 4.34. Resulting IP3 value, which is seen from amplifier output, can be calculated from equation (4.22) about cascaded IP3 calculation [16].

$$\frac{1}{OIP3} = \frac{1}{OIP3_1 G_2 G_3} + \frac{1}{OIP3_2 G_3} + \frac{1}{OIP3_3} \tag{4.22}$$

From the equation (4.22), the first stage in our design is PLL which is followed by mixer. The third stage is the amplifier stage. After writing the gain and IP3 values of these components in the formula, resulting IP3 value of the system can be given as 35.8 dBm.

Finally, simulations give basic information about design. Because, these simulations are in system level. There have to be more detailed system simulations performed to obtain better results. However, in this case, transistor level models of those components must be obtained. Since most of the components are purchased from the market, there is no such detailed information given about those components. Therefore, simulations formed by using the specifications of components, that are going to be used in design,

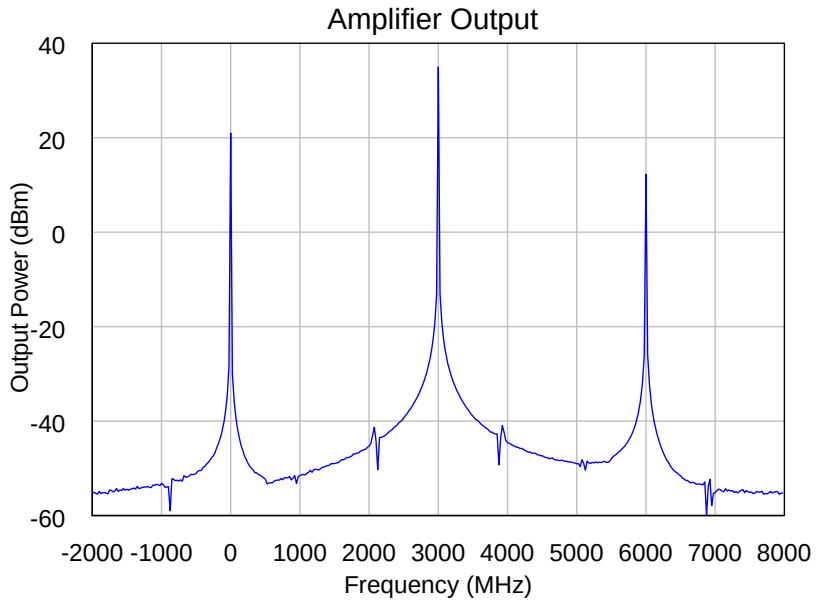

Figure 4.34: Amplifier Output

have been found satisfactory for the purpose of this thesis. In the next section, detailed board design is discussed.

4.4 PCB Design

PCB design is an important part of this thesis. There are many basic rules to follow during PCB design process [17]. Because, the aim is to design an RF circuit and to make all of the decisions that made affect the system performance. Any mistake during the design may fail the results such as line impedances mismatches. Moreover, any mistake about impedance calculation may burn up the circuit.

Altium Designer, which is an advanced PCB design program, is used in this thesis. Radar emitter emulator board is designed by following the steps below.

First of all, schematics library must be created. Schematics library includes all of the components in the project. In the library, components are represented as boxes. Input and output pins are drawn and named. Order of the pins does not have to be the same. Similar pins, such as not connected (NC) pins can be collected together for easy representation. For instance, SW90-0001 is designed as a box in schematics library by naming and numbering its pins as given in Figure 4.35.

Secondly, schematic of the whole design is created on a schematics sheet. Capacitors,

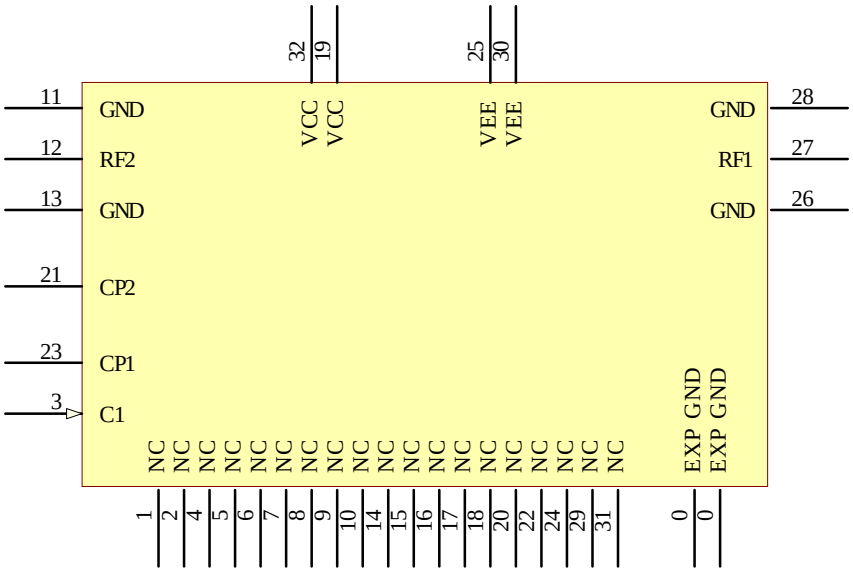

Figure 4.35: SW90-0001 Schematic Description

inductors and resistors are connected to those components. Component to component connections are also indicated including I/O ports of the board on the schematics sheet. An example of a schematic connection can be seen in Figure 4.36. As seen from APPENDIX B, comments about design can be stated about the points that are important. Comments may include some PCB placement issues such as the fact that a capacitor should be placed closely to another component or about some design issues to be careful such as current consumed by component. RF and power schematics of the whole design are indicated in APPENDIX B.

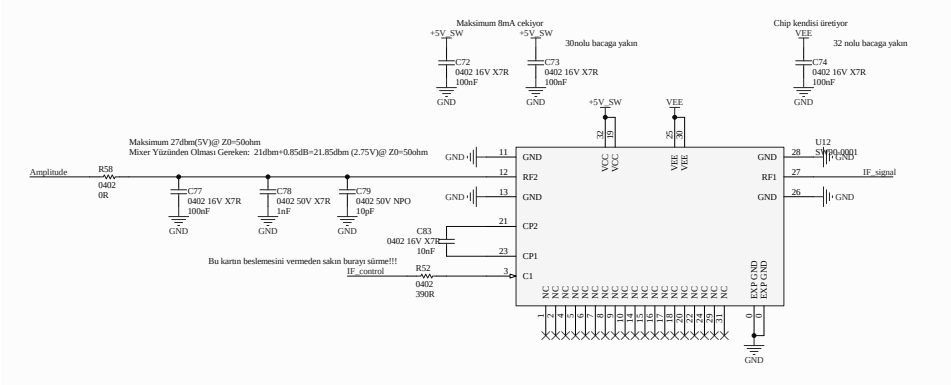

Figure 4.36: SW90-0001 Schematic Connections

Moreover, RF and supply units of the board are separated because supply circuits inject noise and affects system negatively. Therefore, two different schematic sheets are prepared. After completing schematic design, footprints of the components such as resistors, capacitors, inductors and chips are drawn. Furthermore, PCB library, which is a library of footprints, is created. An example of a footprint for switch can be seen from Figure 4.37. Footprints have to be the same as the components. If any mistake is made, the components cannot be soldered on the printed board. Furthermore, printing PCBs is costly and may result thousands of the printed boards to be waste, if any serious mistake is made in the mass production state of the PCB.

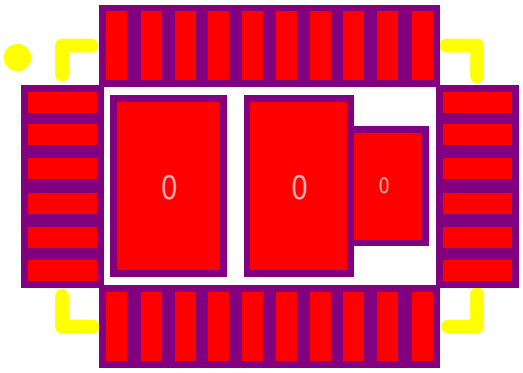

Figure 4.37: SW90-0001 Footprint

Compiling the schematic files to create a PCB is the next step. All of the components are created on the predefined PCB board. Then, those components are placed on PCB in a feasible manner by considering the connections among them. If there exists any evaluation boards for the components, those boards may give ideas how to make placements. Evaluation boards are used as a basis for the layout. Also, there are many key instructions written in datasheets and these instructions must be read carefully. In Figure 4.38, PCB placement of the regulator is given. U2 is the regulator in the figure and other components such as capacitors and resistors are placed around U2. Compiling the schematic files to create a PCB is the next step. All of the components are created on the predefined PCB board. Then, those components are placed on PCB in a feasible manner by considering the connections among them. If there exists any evaluation boards for the components, those boards may give ideas how to make placements. Evaluation boards are used as a basis for the layout. Also, there are many

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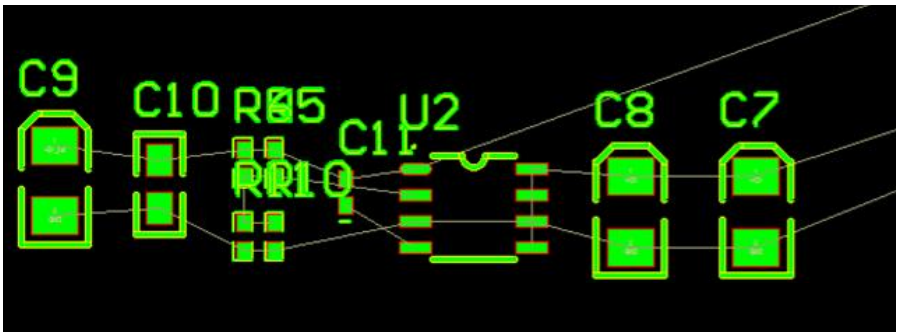

Figure 4.38: Placement of components to PCB

Routing is the final step after placement of components. Width of conducting lines varies from its specifications. RF components have to be connected with 50 ohm impedance microstrips. Microstrip is a type of electrical transmission line which can be fabricated using printed circuit board technology and is used to convey microwave-frequency signals. It consists of a conducting strip separated from a ground plane by a dielectric layer known as the substrate. For lowest cost, microstrip devices may be built on an ordinary FR4 (standard PCB) substrate. However, it is often found that the dielectric losses in FR4 are too high at microwave frequencies and that the dielectric constant is not tightly controlled. For these reasons, an alumina substrate is commonly used. The electromagnetic wave carried by a microstrip line exists partly in the dielectric substrate and partly in the air above it. In general, the dielectric constant of the substrate will be greater than that of the air, so that the wave is traveling in an heterogeneous medium. In consequence, the propagation velocity is somewhere between the speed of radio waves in the substrate, and the speed of radio waves in air. This behavior is commonly described by stating the effective dielectric constant (or effective relative permittivity) of the microstrip; this being the dielectric constant of an equivalent homogeneous medium (i.e. one resulting in the same propagation velocity).

A closed-form approximate expression for the quasi-static characteristic impedance of a microstrip line was developed by Wheeler in (4.23).

$$z = \frac{z_0}{2\pi\sqrt{2(1+\varepsilon_r)}} ln\left(1 + \frac{4h}{\omega_{eff}}\left(\frac{14+\frac{8}{\varepsilon_r}}{11}\frac{4h}{\omega_{eff}} + \sqrt{\left(\frac{14+\frac{8}{\varepsilon_r}}{11}\frac{4h}{\omega_{eff}}\right)^2 + \pi^2\frac{1+\varepsilon_r^{-1}}{2}}\right)\right) \tag{4.23}$$

ω_{eff} is the effective width, which is the actual width of the strip, plus a correction to account for the non-zero thickness of the metallization. Effective width is given in (4.24)

$$\omega_{eff} = \omega + t\frac{1+\varepsilon_r}{2\pi} ln\left(\frac{4e}{\sqrt{\left(\frac{t}{h}\right)^2 + \left(\frac{1}{pi}\frac{1}{\frac{w}{t}+\frac{11}{10}}\right)^2}}\right) \tag{4.24}$$

z_0 : impedance of free space

ε_r : dielectric constant of substrate

w : width of strip

h : thickness of substrate

t : thickness of strip metallization

FR4 material can be used up to 4 GHz. There are some other materials used for high frequency bands which are more suitable for those bands. In this thesis, RO4350 material is used as substrate. Line width for 50 ohm impedance matching is 550 μm for RO4350. Some other materials can be used in 3 - 4 GHz range, but the components that are used in this thesis do not have enough space between its pins. As for RO4003 material, line width for 50 ohm impedance matching will be approximately 1.2 mm, which will make routing of RF lines of PLL impossible. Because, distance between pins of PLL is 500 μm.

A multi layer PCB is much more expensive and difficult to manufacture than a single or double sided board. However, it is advantageous, because it makes possible to route complex power and signal tracks. By doing as such, more compact boards can be designed by placing components more tightly. Multi layer boards come in even number of layers such as 4, 6, and 8 layers which are the most common. With a multi layer design, one layer is completely dedicated to a ground plane and another to power usually. Power layers and ground layer are almost always in the middle of the board. Generally, ground layers are closer to the top layer [17]. 4 layered PCB is used to obtain isolation between supply and RF layers as mentioned before. Top layer of PCB is designed for RF components and lines. PLL, mixer, amplifier and RF microstrips are all in this layer. RO4350 material is used as substrate below RF signal lines. Next layer

is signal layer followed by ground layer. Between this signal layer and ground layer, FR4 material is used. Bottom layer is again signal layer and regulators and related components are placed on this layer. Again, substrate used between this signal layer and ground layer is FR4. I/O and supply ports are placed on PCB to communicate with components and transmit signals.

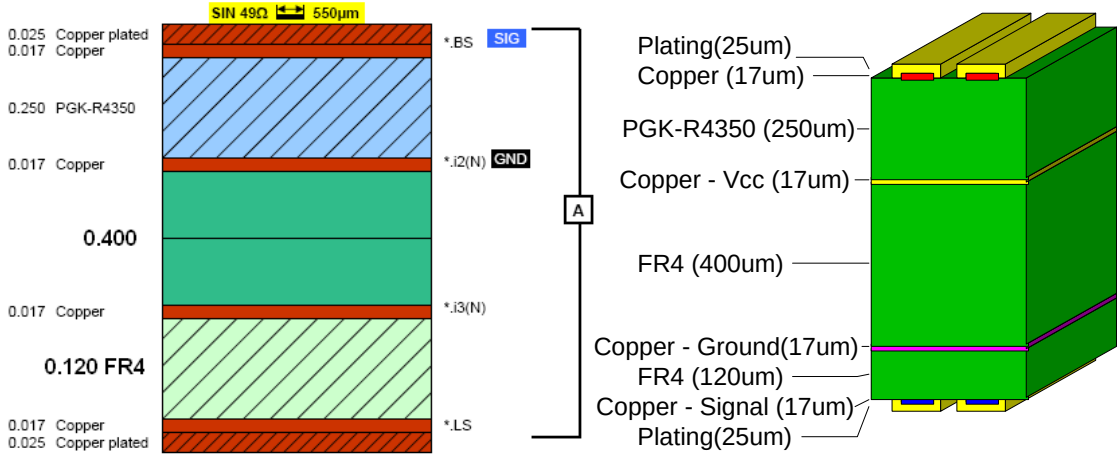

Figure 4.39: Stack-up Comparison

The required impedance is 50 ohms and PCB producer company's suggestion for proper line width when RO4350 substrate is used, was 550μm. PCB layers are built in Hyperlynx software, which is used for impedance calculations, to check the line width for 50 ohms impedance matching. In Figure 4.39, the figure in the left side is the configuration of the stack up that is given to PCB company and the line width for 49 ohm impedance is given as 550μm. The stack-up at the right hand side is Hyperlynx output of the designed stack-up. After calculating the line width for 50 ohms, the obtained results can be given in Figure 4.40.

These values can also be proven from (4.24) with the values given as below. The calculated impedance is 51.3720 ohms, which is approximately true. The effect of the plating is not considered in this case.

$z_0 = 376.730313$

$\varepsilon_r = 3.48$

	Layer Name	Usage	Thickness um	Er	Target Z0 ohm	Width um	Gap um
1		Plating	25	<Auto>			
2	Copper (17um)	Signal	17	<Auto>	49	552.071	
3	PGK-R4350 (250um)	Substrate	250	3.48			
4	Copper - Vcc (17um)	Plane	17	<Auto>	50	432.52	
5	FR4 (400um)	Substrate	400	4.3			
6	Copper - Ground (17u	Plane	17	<Auto>	50	437.516	
7	FR4 (120um)	Substrate	120	4.3			
8	Copper - Signal (17u	Signal	17	<Auto>	50	205.485	
9		Plating	25	<Auto>			

Figure 4.40: HyperLynxs Output

$w = 550\mu$m

$h = 250\mu$m

$t = 17\mu$m

Finally, a Gerber file, which is a standard file type for PCB designs, is generated to print PCB with a computer aided printing machine. In this thesis some components have 402 packaging and some of the components are surface mounted components. So, it is not possible to solder these components by hand. Resulting PCB is sent to soldering process with components used in design. Final view of the designed board in Altium designer is given in Figure 4.41 and Figure 4.42. The picture of RF and digital layers and a view of the resulting design is shown in APPENDIX A.

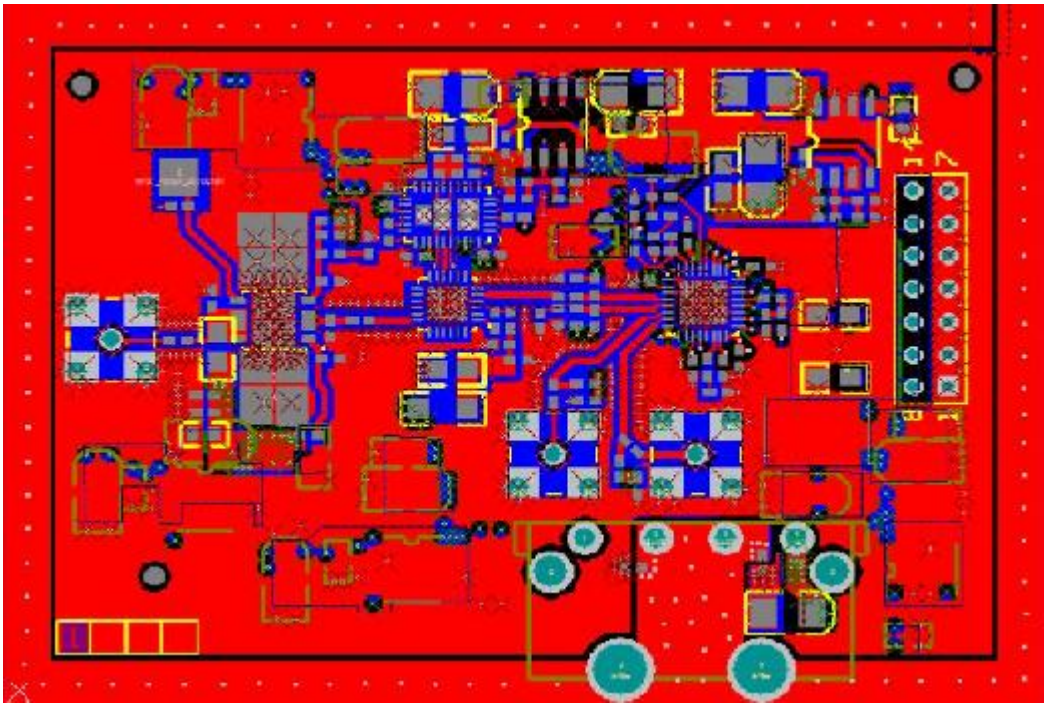

Figure 4.41: RF Layer of Resulting PCB

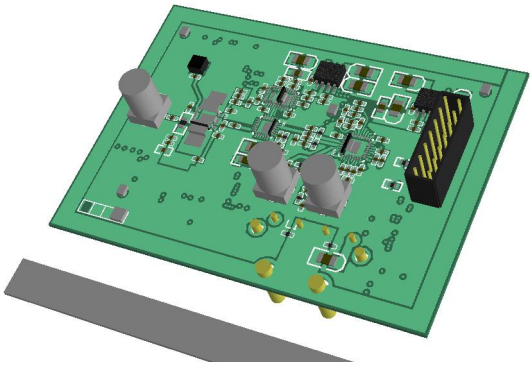

Figure 4.42: 3D View of Board

CHAPTER 5

RESULTS AND DISCUSSION

In this chapter, designed board is tested and some problems are covered during the tests. In the first few trials, board could not be operated. Problems are defined and solutions are suggested to solve these problems. Finally, board is operated and basic radar pulse trains are generated.

First of all, when supplies are connected to the board, as expected from many other electronic designs, it did not work. Therefore, temperatures of the components are controlled initially. Temperature of amplifier and regulator, which feed the amplifier increased rapidly. In the design, the board was thought to be supplied with 12V. Because the regulators allow to supply with 20V maximum. The output of regulators was biased to 5V. Therefore, it is enough to supply the board with 7.5V. This is applied to solve temperature problem because linear regulator converts excessive energy to heat. The board is operated with 7.5V to solve temperature problem. The temperature of the amplifier and the regulator were still increasing. Voltages of the input pin of power amplifier are controlled and from the data sheet of power amplifier those voltages are checked. V_{PC} voltage defines how the power amplifier will operate. The amplifier can work with 5V or 6V V_{PC} voltages. However, one of the voltage value must be chosen. Because, required resistors to be connected to the V_{PC} pin is different for both cases. The problem was that V_{PC} is chosen to be 6V, but the resistor values were set for 5V V_{PC}. Furthermore, in 6V application, the amplifier consumes 326mA and 385mA for 5V application. The problem was that the regulator tried to consume more current and the temperature of the regulator increased rapidly. After soldering correct resistors, temperature problem was disappeared. Soldered resistor, which is at the left of white supply connector in digital layer of the board, can be seen from APPENDIX A .

Moreover, voltage divider resistor values of one regulator were incorrect. The output voltage was required to be 3.3V but the measured value was different. Therefore, the

resistors for biasing the output voltage are checked that the voltage was 5.1V instead of required 3.3V. Resistor values at voltage divider of the regulator are checked and it was found that 2K2 Ω is soldered instead of 47K Ω.

After errors are corrected, one more time board is supplied and configured. When spectrum analyzer is controlled, signal at the desired frequency could not be seen. Spectrum is searched with a full span and signal at -56dBm level is detected at 4.378GHz. It was thought that PLL is not configured very well. Because the led connected to the lock detect output of PLL, which gives voltage when PLL is locked to a frequency, was not turned on. It was found from the datasheet of ADF4350 that PLL selects the desired frequency band coarsely by waiting (10PFD cycles x band select clock divider value). The clock divider value is set to 1 which gives less time to VCO to find the frequency band coarsely. After setting this 8 bit value to its maximum of 255, the signal at the output at 3.5GHz appears.

There was still one more problem. Desired frequencies could be seen at the spectrum analyzer but the signal level was -10dBm. If the 15dB attenuator value, which is connected to the output of the amplifier, is added to this value, the signal level is still 5dBm. The expected output signal level was 26dBm. Mixer output was controlled from the V_{DET} test point. V_{DET} is one of the pins of power amplifier that samples the output power of the mixer. So, the LO and IF inputs of the mixer are controlled. There was not any test point to measure the signal level at the LO input of the mixer. However, the auxiliary outputs of the mixer (RF_{OUTB+} and RF_{OUTB-}), which gives the same signals to the output if the PLL is configured to enable AUX outputs, were connected to SMA connector to make measurements and leaved for future applications. After enabling AUX outputs of the mixer, signal level at the AUX outputs was measured correctly. Therefore, IF input of the mixer is controlled by closing the switch to apply voltage to the IF input of the mixer. The voltage at the input of the switch was 2.6V. However, the voltage measured at the output of the switch was 0.8V. There was a problem with switch that the amplitude of the switching signal is attenuated at the output of the switch. When the datasheet of the switch is reviewed, the connections are described as from RF1 to RF2, but it was not indicated that RF1 is input and RF2 is output. During the design, it was thought that switch is operating from RF1 to RF2 and vice versa. Input and output ports of the switch were then changed, but the voltage at the output of the switch did not change. After applying 2.6V at the input of the mixer IF port directly, the signal level became 8dBm at spectrum analyzer, which means that the actual level

is 23dBm after adding 15dB attenuator value. 5 cards designed for testing and switch is disassembled from one of them to give switching signal from FPGA directly. Instead of switching regulator voltage, FPGA can generate switched signal as an input to the mixer. This idea was thought while designing the board. However, FPGA voltage is noisy, and FPGA board is not close to the IF input of the mixer. Regulator was the best choice because of its ability to generate clear DC voltage. Mixer input is driven by FPGA to solve problem but in this case the required output voltage of the switch still could not be achieved. The reason for this is thought that the sink and source currents of FPGA board is maximum of 20mA. By connecting transistors, the problem can be solved but the rest of the simulations are performed with lower power levels. Furthermore, it is thought that this current is not enough for mixer IF input.

Finally, board was tested with different frequencies and the results are given and explained in the next section.

5.1 Emulation Results

Radar pulse trains are generated at the end of thesis. The aim was to generate radar pulse trains between 3 - 4GHz with different kinds of PRI modulation. Therefore, carrier signal can be controlled if it could be generated first of all. Connecting one of the AUX output of the PLL to the spectrum analyzer will give information about the signal generated. The signal power at the output of PLL is programmable from -4dBm up to 5dBm. The output power is measured at 3GHz from the AUX output of PLL when the output power level is set to 5dBm. The measured value was -12dBm. 15dB attenuator was connected at the input of the AUX out and the signal at the output of the mixer was 3dBm.

First of all, 3.5GHz signal is synthesized and the signal is tested from the amplifier output and auxiliary outputs.

Output power levels are measured versus frequency and peak powers can be given in Figure 5.1.

From the figure, output power decreases when frequency is increased after 3.5GHz. Normally the power amplifier is suggested to run from 3GHz up to 3.8GHz. This is the reason for this attenuation on the signal.

Moreover, frequency domain representation of a rectangular pulse is a sinc function. The frequency difference between the peak and the first null of sinc function is the

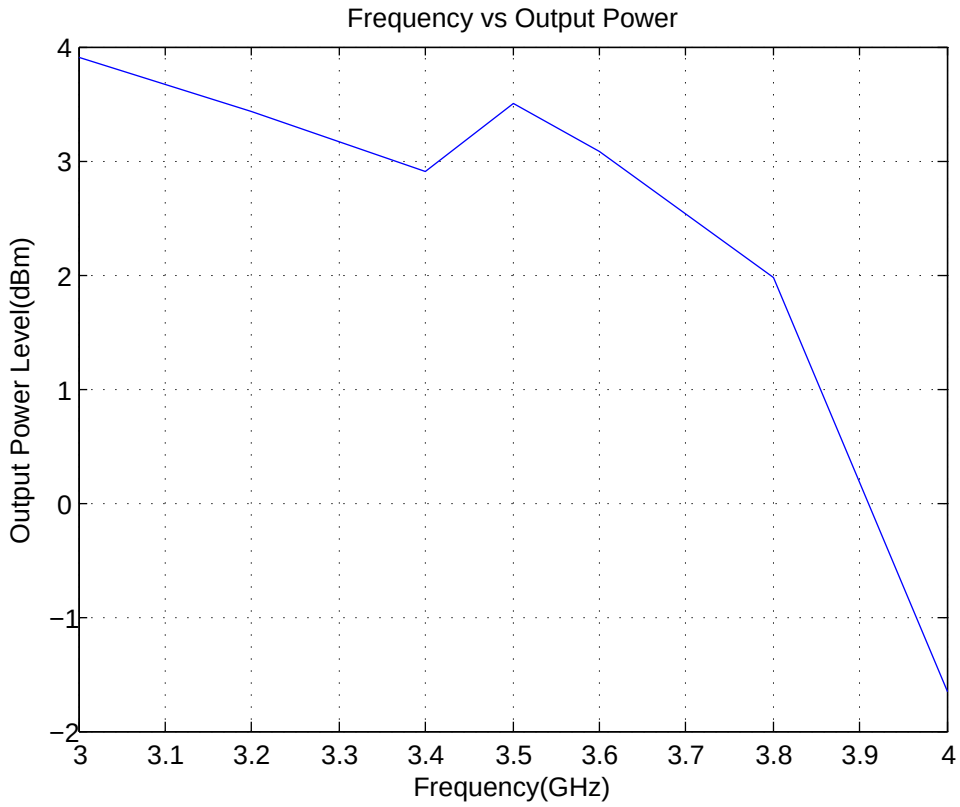

Figure 5.1: Output Power vs. Frequency

division of pulse with one. Therefore, pulse train with 100μs PRI is generated and pulse width is chosen to be 5μs. From the measurements taken from the spectrum analyzer, waveform is given in Figure 5.2.

Furthermore, the first null of the sinc function is expected to be 200kHz away from the main lobe or center frequency. Second and third nulls are expected to pass from 400kHz and 600kHz respectively. Therefore, sinc function is observed from spectrum analyzer. Span was chosen as 1MHz and screen was divided with 10 equally spaced lines. The first null of the signal was passing through second division from the center value. So, the distance is 200kHz, which means that the pulse is generated with desired pulse width. Figure 5.3, Figure 5.4 and Figure 5.5 indicate these null points with delta markers.

The difference level of the main lobe and the first side lobe of the sinc function has to be 13dBc. This value is measured by placing delta markers. Figure 5.6 depicts this difference.

The harmonic values are measured in different frequencies and can be given in

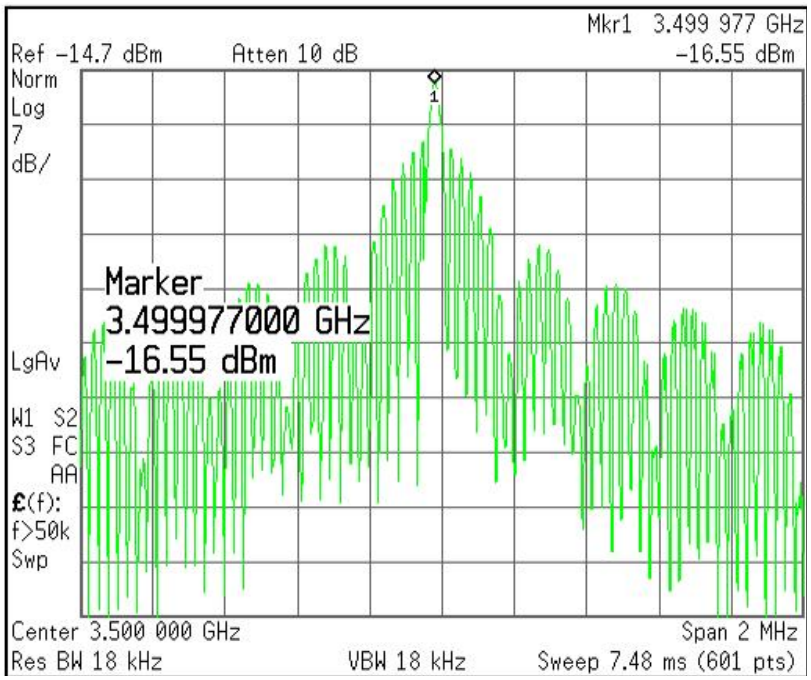

Figure 5.2: Frequency Domain Representation of the Pulse Train

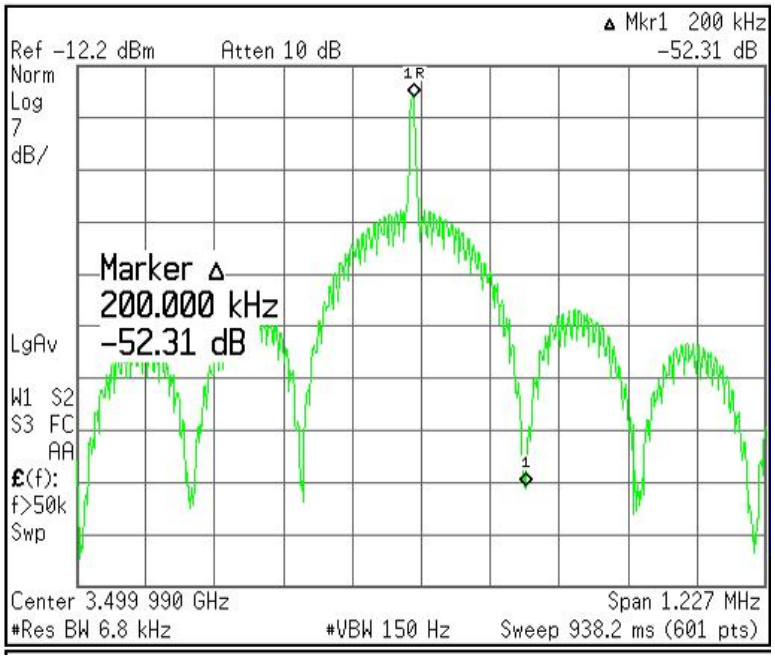

Figure 5.3: Distance Between Main Lobe and First Null of Sinc Function

Table 5.1.

Rise and fall times of the pulses can be calculated from spectrum analyzer by following the procedure below [21].

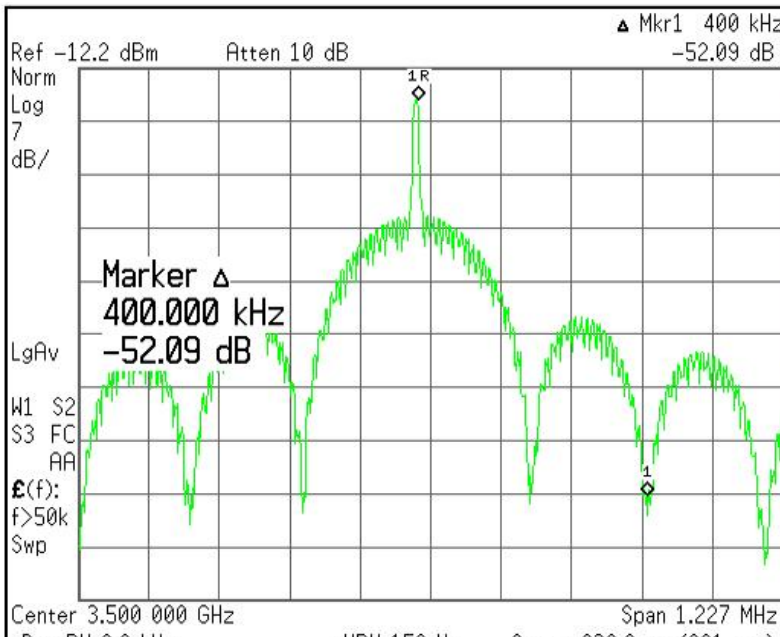

Figure 5.4: Distance Between Main Lobe and Second Null of Sinc Function

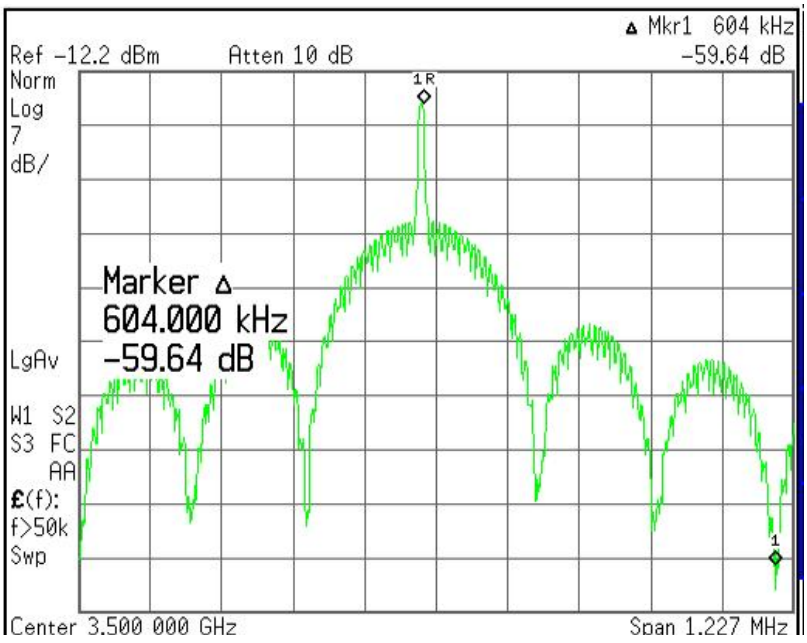

Figure 5.5: Distance Between Main Lobe and Third Null of Sinc Function

- Set the center frequency to the carrier frequency.
- Increase resolution BW and video BW to the maximum values.
- Set span to zero span.
- Decrease sweep time till pulses occur on the display.

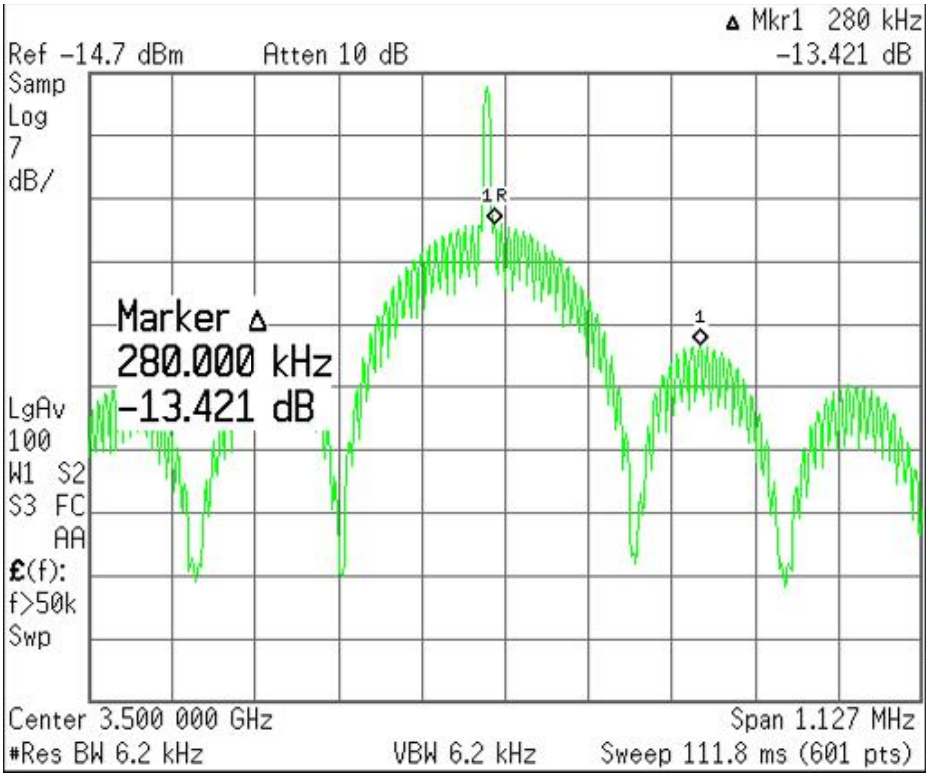

Figure 5.6: Difference Level Main Lobe Peak & First Side Lobe Peak

Table 5.1: Harmonic Terms

Frequency	2nd Harmonic	3rd Harmonic	4th Harmonic	5th Harmonic
3.2 GHz	-53.32dBc	-59.07dBc	-64.71dBc	-67.46dBc
3.5 GHz	-50.16dBc	-53.32dBc	-58.92dBc	-65.31dBc
3.8 GHz	-49.27dBc	-50.14dBc	-55.42dBc	-60.79dBc

- Set trigger in video mode and adjust to see stable pulses from the display.

However, rise time and fall time of the generated pulses could not be measured because of the deformation at the center frequency. Therefore, as seen from the frequency domain representation of the resulting signal, there is a distortion at the center frequency. It is known that switch is not working properly and switch is not isolating the signal well, when it is in off state. The resulting signal at the RF output is not the desired pulse train. The resulting signal is a sine wave, which is amplified during pulse and which is not amplified between consecutive pulses. When switch is off, sine wave is transmitted to the amplifier, which is leaked during PRI. Therefore, the spectral component at center frequency occurs. Because, the resulting signal is combination of

sine wave and pulse train.

Finally, some of the electrical specifications of the board are summarized. The board consumes 590mA at 7.5V, while both AUX and RF outputs are transmitting. When AUX output is muted, the consumed current decreases to 560mA. The heat of circuit increases to $70°C - 75°C$ after operating for a couple of minutes. Most of the heat is radiated because of power amplifier. Use of coolant with a mounted fan will solve this problem.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

Finally, different ways of emulating radar emitters are covered in this thesis. First of all, specifications and functionalities that were required to emulate radar are given. Two different ways of emulating emitters by using instruments and by using commercially available boards were covered briefly at first glance. Radar pulse trains with variety of frequencies and PRI values are generated by designing a simple trigger circuit while generating radar pulse trains. Signal generator's pulse modulation input gate feature is prerequisite for generating pulse trains. Next step was to emulate emitters by using commercially available boards. At the end, radar emitter emulator board was designed. As a result, tests were performed to define specifications of designed board.

Furthermore, since radars are embedded inside high technology equipment, some of those radars have military purposes. In order to use radars effectively, the information has to be detailed about them. At the end of this thesis, cost-effective way of radar emitter emulation is presented. Moreover, by this way, organizing military trials to train military personnel will be inexpensive. The primary motivation for this work was the lack of commercially available cost effective emitter simulators which is designed at the end of this thesis. Hence, portable and single board emitters reduce the need for using several different platforms while performing such military trials.

Moreover, the board will be used as a platform for teaching and learning embedded emitter systems. The target user groups for this design are students, researchers in various universities and research labs and military personnel, too.

Consequently, designed board can be used for the following purposes. Some of the listed items below can be enhanced by adding new features to design which are mentioned in the future work section.

- The design can be used as a teaching tool in radar courses.
- Military personnel may use this design during the military trials to train.
- The sensitivity tests can be performed for ESM systems which are wideband receivers used for listening electromagnetic emissions.
- The design will provide sufficient resources for the researchers and developers to build applications on top of it by interfacing different technologies with it.

6.2 Futurework

A basic radar emitter emulator is designed and implemented at the end of thesis. Basically a simple radar pulse train at a fixed frequency with any kind of PRI modulation can be generated. Hence, the design can be improved by developing software to control its capabilities. This can be performed by writing the required information to RAM through PC to set the parameters of the pulse train that is going to be generated. After then parameters of PLL or other components can be set through FPGA.

Antennas with different characteristics can be placed at the output of power amplifier. Therefore, desired pulse train can be transmitted through the air, by this way. System can be tested in this case by including the effects of the antenna. ESM systems generates digital words and passes it to a digital processor usually include five quantities which are, frequency, pulse amplitude, pulse width, time of arrival and angle of arrival [18]. Therefore, this board can trick other ESM systems or generate signals to test ESM systems after the required corrections are performed which are mentioned in the previous chapter. Because the designed board can generate the signals that an ESM system requires. External power amplifier can be used to transmit pulse trains with higher powers to improve the range. In this case, more linear amplifier can be chosen at the output of the board.

The aim of this thesis was to implement basic radar schematic. Therefore mixer is one important component of a radar design. This is the reason why mixer is used in the design. The use of mixer may be unnecessary to generate pulse trains. Instead of using a mixer, switch can be connected directly to the output of PLL. Therefore, by switching the synthesized frequency, pulse trains with different PRI types and modulations at a single frequency can be generated. The switch that is used can be a high isolation switch in order to obtain pulse train. So, when the switch is opened, there will be

less leakage from PLL to the amplifier. Mixer can be used to obtain pulse trains with frequency modulation. In this case, switch will be connected to the RF output of mixer and IF input of the mixer will have signal with changing frequency. There are also two differential outputs of the PLL. By switching these two outputs, B-PSK modulated pulses can be generated. However, all of these different designs can be implemented on a single board in order to compare the performance of different approaches on pulse train generation. Furthermore, phase, amplitude and frequency modulation will be possible by using IQ modulators. Any king of waveform can be generated by use of IQ modulators. So, the board that is going to be designed in future should include IQ modulator in the design.

In this thesis only the radars between 3 - 4 GHz frequency band is covered. To enhance the coverage of the design, similar structure can be used in different frequency bands. Therefore, more detailed simulations can be performed. Instead of using the blocks similar to the blocks of design, new blocks can be generated to get better simulation results.

Moreover, the generation of jamming signals cause information damage to radar if the ratio of interference power in the radar receiver to the power of the reflected signal is equal to or exceed a threshold level [19]. Therefore, if this board is supposed to be connected to cooperate with an ESM system, generating the received pulse trains which are received from environment will be possible. Consequently, jamming the radars which are identified by an ESM system will be possible by taking arrival time of the pulses into account.

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APPENDIX A
PICTURES OF FINAL DESIGN

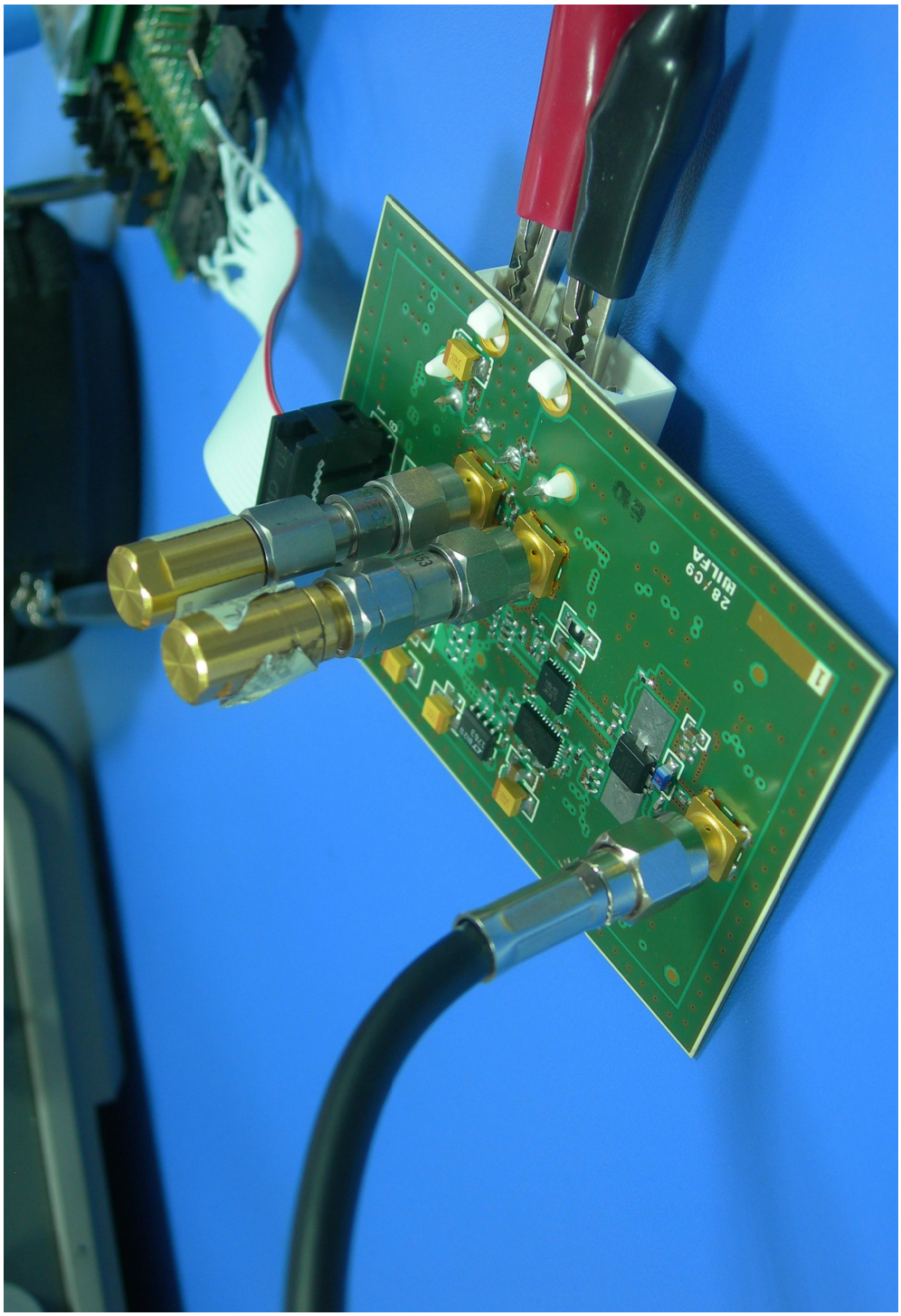

Figure 6.1: A View of the Final Design

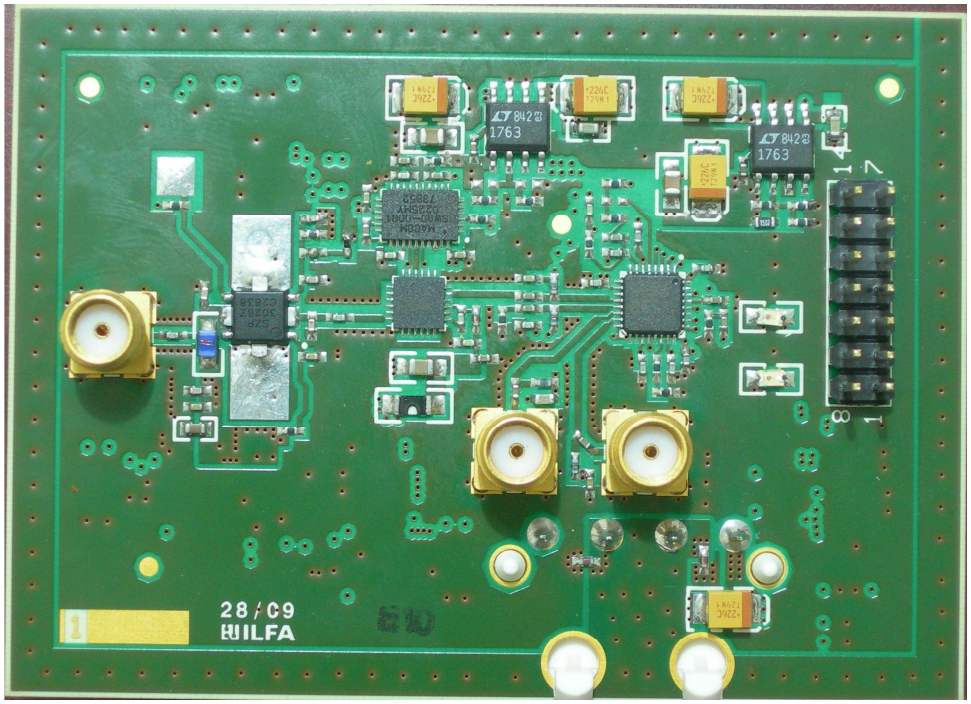

Figure 6.2: RF Layer of the Final Design

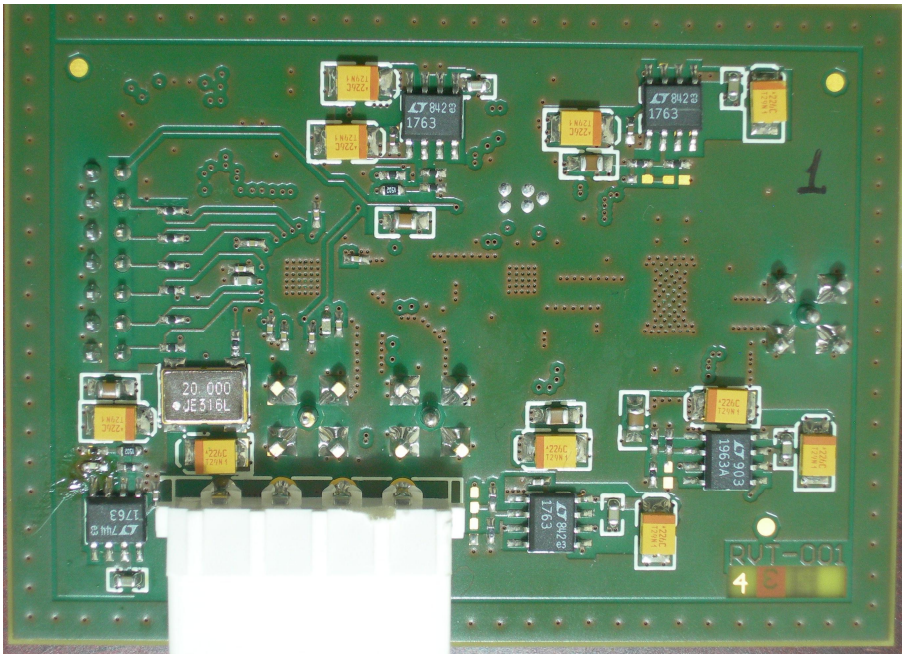

Figure 6.3: Digital Layer of the Final Design

APPENDIX B
SCHEMATICS OF DESIGN

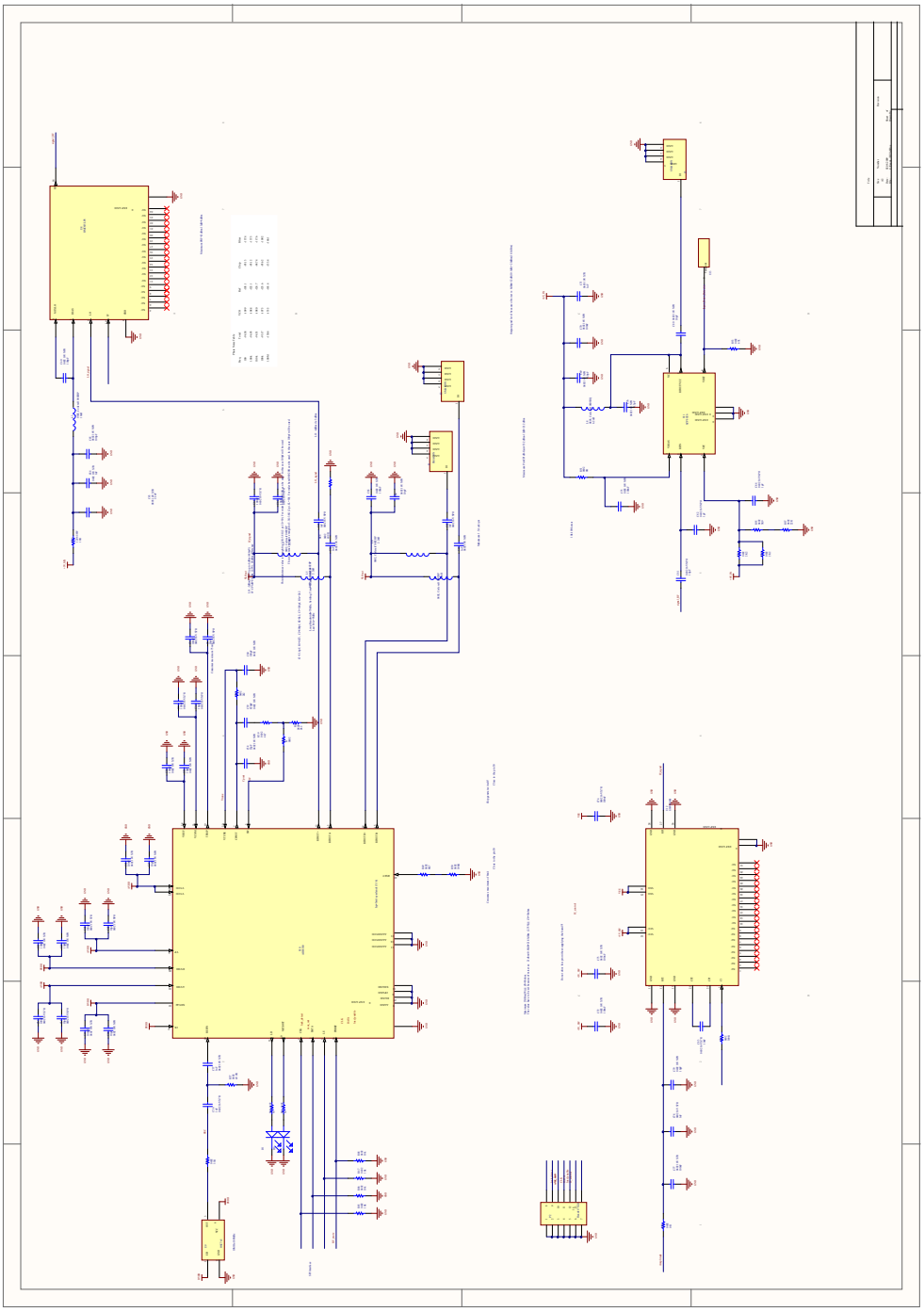

Figure 6.4: RF Schematics of the Final Design

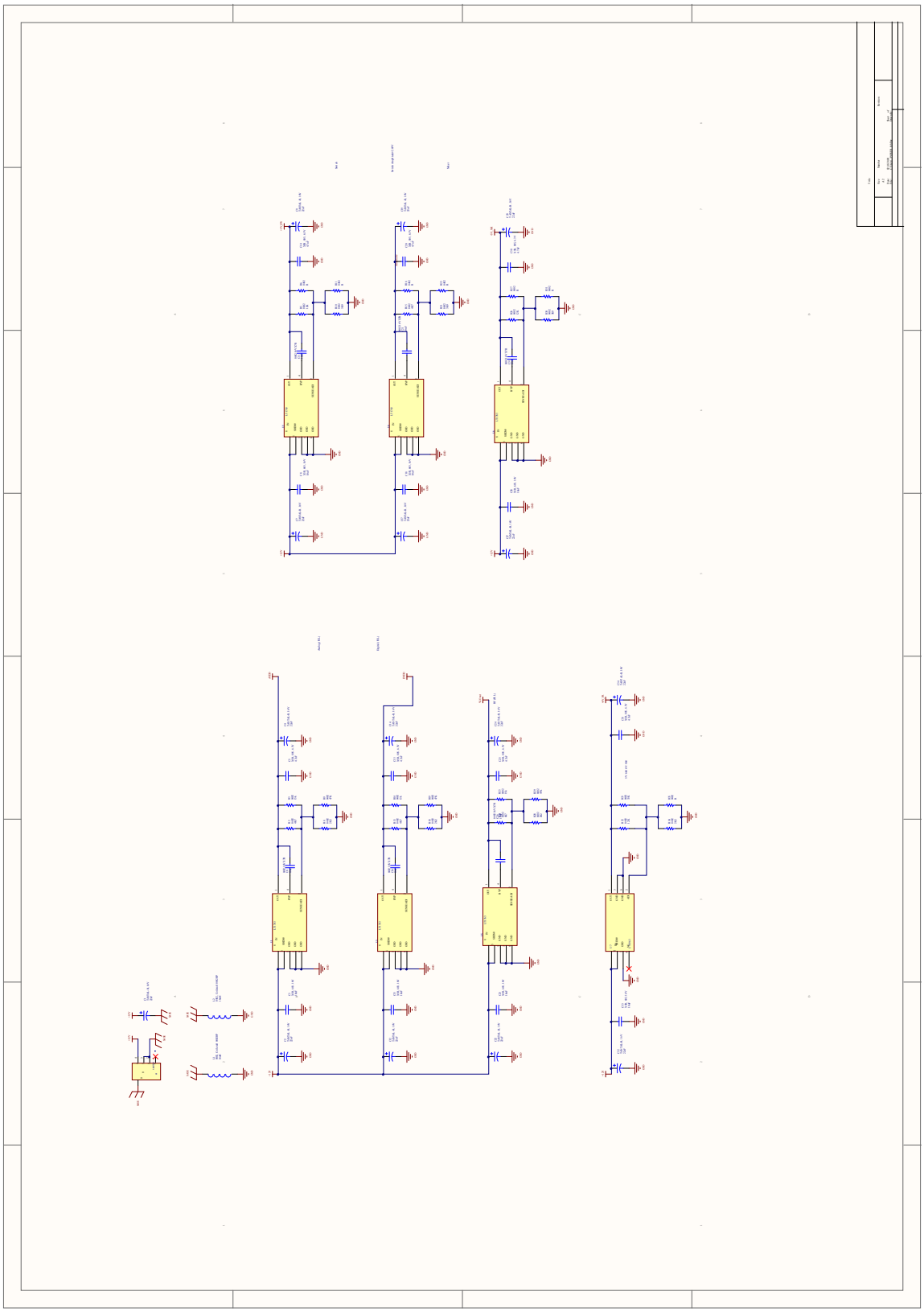

Figure 6.5: Power Schematics of the Final Design

APPENDIX C
ADF4350 ADISimPLL Simulation Results

ADISimADF4350METUThesis.pll analysed at 08/02/09 20:56:06
PLL Chip is ADF4350
VCO is ADF4350
Reference is custom
VCO Divider Inside Loop: division ratio = 1
Frequency Domain Analysis of PLL
Analysis at PLL output frequency of 3.464GHz
Phase Noise Table

Freq	Total	VCO	Ref	Chip	Filter
100	-95.10	-110.7	--	-95.22	-157.4
1.00k	-95.05	-109.4	--	-95.21	-137.4
10.0k	-94.63	-108.4	--	-94.84	-117.6
100k	-94.87	-107.7	--	-95.29	-108.8
1.00M	-130.1	-133.6	--	-132.8	-145.5

Reference Spurious
Noise and Jitter Calculations include the first 10 ref spurs
First three spurs: -300 dBc -300 dBc -300 dBc
Fractional-N Spur Estimate (worst case)
Phase Detector mode is Dither OFF

Freq (Hz)	Spur Level (dBc)
500k	-70.5
1.00M	-82.6
1.50M	-89.9

Phase jitter using brick wall filter
from 10.0kHz to 100kHz
Phase Jitter **0.55 degrees rms**
ACP - Channel 1
Channel 1 is centred 25.0kHz from carrier with bandwidth 15.0kHz
Power in channel = **-51.5dBc**
Transient Analysis of PLL
Frequency change from 3GHz to 4GHz
Simulation run for 161us
Frequency Locking
Time to lock to 1.00kHz is 113us
Time to lock to 10.0 Hz is 126us
Phase Locking (VCO Output Phase)
Time to lock to 10.0 deg is 103us
Time to lock to 1.00 deg is 112us
Lock Detect Threshold
Time to lock detect exceeds 2.50 V is 159us

Figure 6.6: ADISimPLL Report of Designed PLL

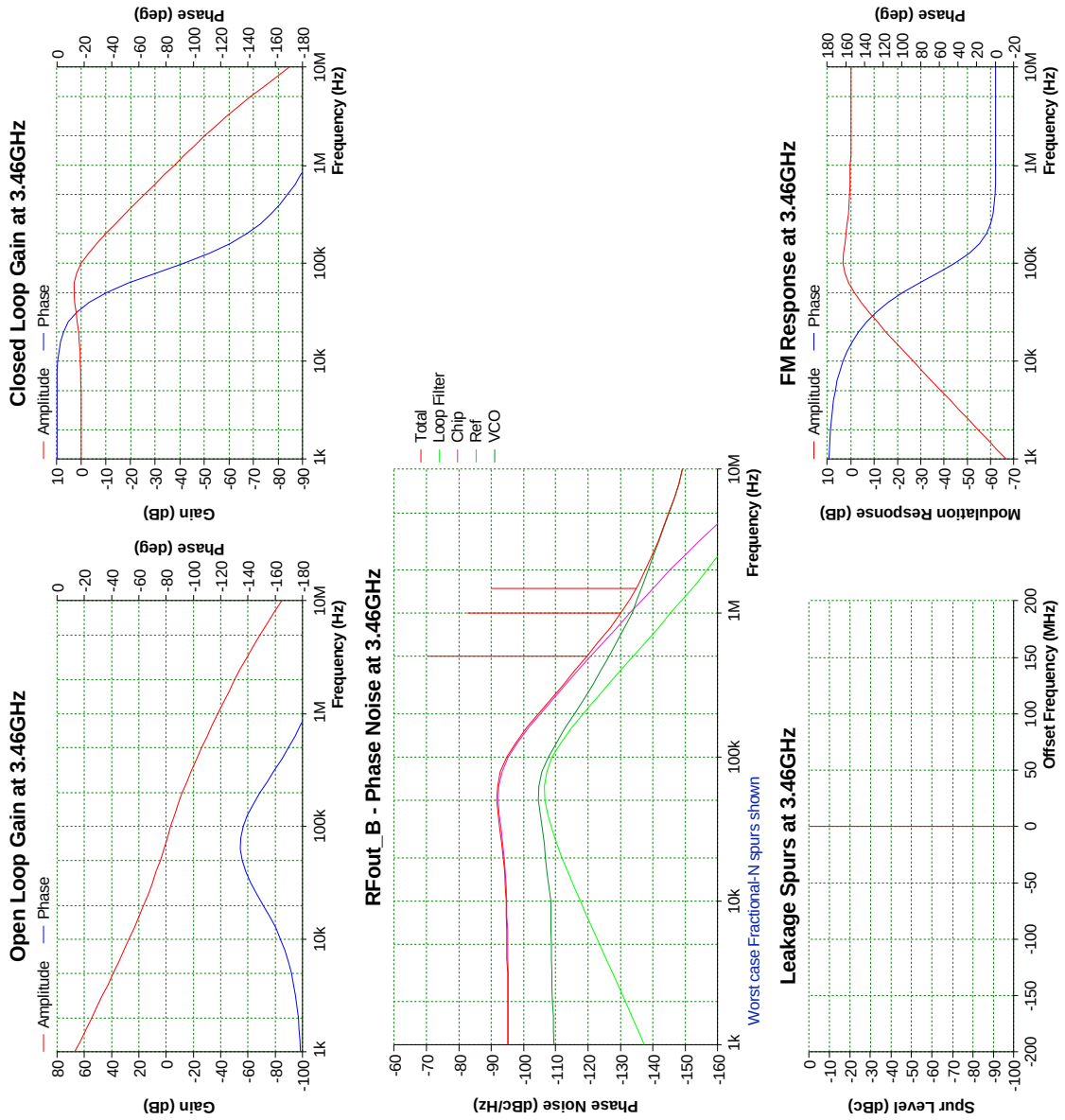

Figure 6.7: Frequency Domain Characteristics of the Designed PLL

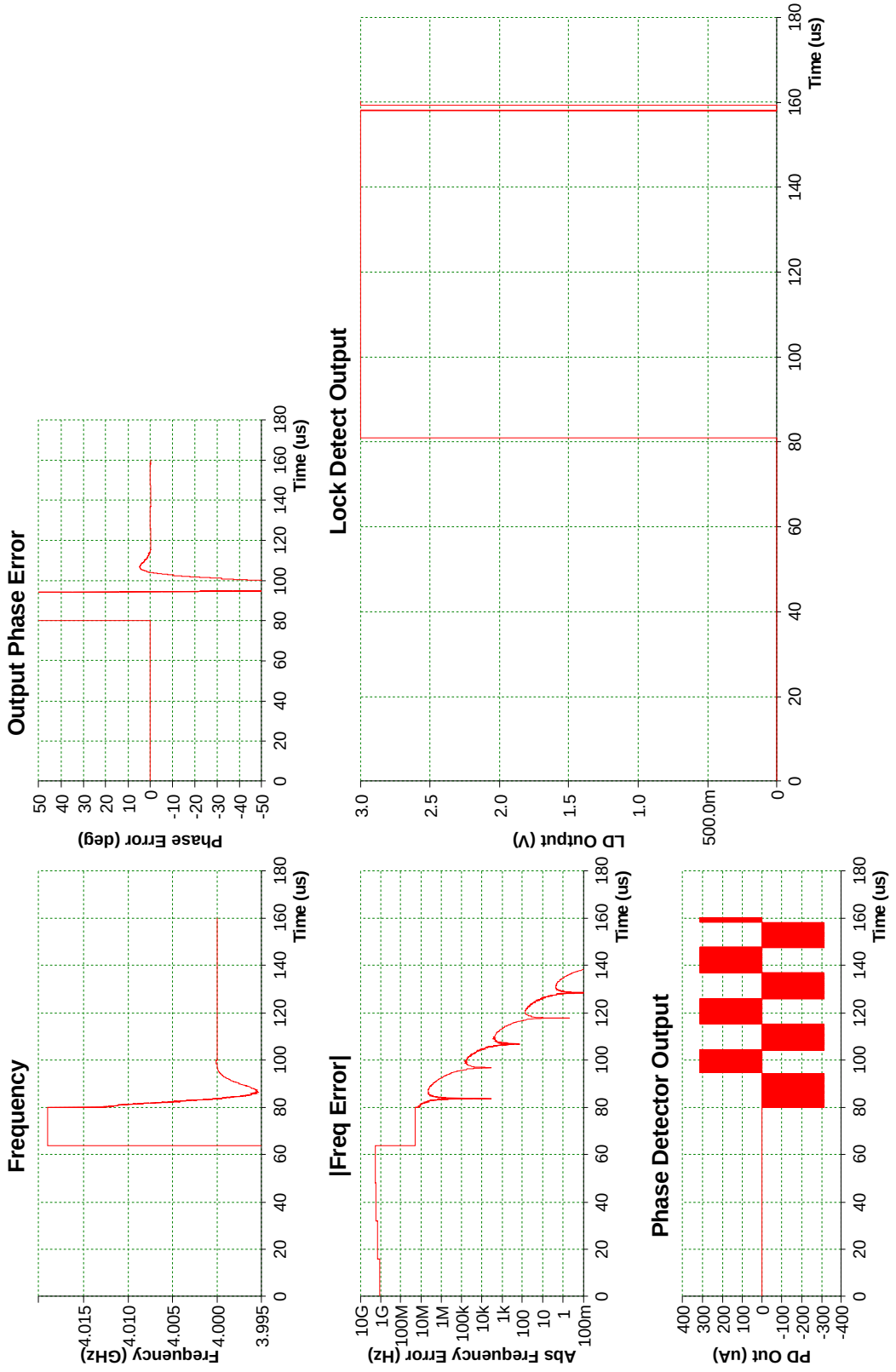

Figure 6.8: Time Domain Characteristics of the Designed PLL

VITA

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