INVESTIGATION OF MULTILEVEL INVERTERS FOR D-STATCOM APPLICATIONS

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ABSTRACT

INVESTIGATION OF MULTILEVEL INVERTERS FOR D-STATCOM APPLICATIONS

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The most important advantages of Multilevel Inverters are the absence of a coupling transformer for medium voltage applications and low harmonic current content. In this way, relocatable and economical STATCOM systems can be realized. Complex control algorithms and the isolation problems of measurement devices and power supplies are the main challenging parts of this type of application. In this study, the design, realization, and the performance of a Voltage Source Type Cascaded Multilevel Converter Based STATCOM will be investigated in terms of digital computation, control hardware and the semiconductors devices commercially available in the market. This research work is fully supported by the Public Research Grant Committee (KAMAG) of TUBİTAK within the scope of National Power Quality Project of Turkey with the project No: 105G129.

Keywords: multilevel inverter, STATCOM, power quality, reactive power compensation

ÖZ

D-STATCOM UYGULAMALARI İÇİN ÇOK SEVİYELİ ÇEVİRGEÇLERİN İNCELENMESİ

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Çok seviyeli çevirgeçlerin en önemli avantajları akımının düşük harmonik içermesi ve orta gerilim uygulamaları için bağlantı transformatörüne gerek duymamasıdır. Bu sayede kolay taşınabilir ve ekonomik STATKOM sistemleri gerçekleştirilebilir. Karışık kontrol algoritmaları, ölçümde ve beslemede elektriksel izolasyon problemleri bu tür bir uygulamanın en zorlayıcı kısımlarıdır. Bu araştırma kapsamında piyasadaki mevcut güç yarı iletkenleri, sayısal hesaplama ve kontrol donanımları açısından Gerilim Kaynaklı Seri Bağlı Çok Seviyeli Çevirgeç Tabanlı STATKOM un tasarlanabilirliği, gerçekleştirebilirliği ve performansı incelenmiştir. Bu araştırma, 105G129 Nolu Güç Kalitesi Milli Projesi kapsamında TÜBİTAK Kamu Araştırma Projeleri Destekleme Programı (KAMAG) tarafından desteklenmektedir.

Anahtar Kelimeler: çok seviyeli çevirgeç, STATKOM, güç kalitesi, reaktif güç kompanzasyonu

To My Family

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TABLE OF CONTENTS

LIST OF FIGURES

FIGURES

LIST OF TABLES

TABLES

CHAPTER 1

INTRODUCTION

1.1. Multilevel Inverters for STATCOM Applications

Multilevel inverters are gaining interest in medium voltage (<36kV) power converters for power quality applications [1-5]. When phase to neutral voltage of a converter has at least three voltage levels, the converter can be classified as a multilevel inverter [2]. In classical approach, six pulse two level converters are used for relatively low power (up to 1 MVA) and low voltage (up to 1kV). Operating voltage range of such a converter is limited to a few kV level due to switching device voltage ratings. Therefore, coupling transformers are being used to connect the inverter to the medium voltage load or the utility. Transformers are expensive and heavy component in the system. Therefore transformers increase the cost and decrease the mobility of the system. Six pulse inverters can generate higher voltages if switching devices are connected in series. However, this leads to complicated busbar designs to decrease busbar inductance, and requires nearly identical switching devices in a string. Un-identical devices in a series string leads to unequal voltage sharing between switching devices at transients and switching devices fail from high voltage. Furthermore, for series operation, press-pack switches (IGBT or IGCT) are required, which are produced by limited number of companies (Westcode, ABB and Toshiba). Therefore, semiconductor switch prices are not competitive. Conventional (wire-bond) IGBTs are price competitive and have higher market availability with respect to press-pack devices. Consequently, generation of medium voltages can be realized easily with Multilevel Inverters using wire-bond modules.

Previously built distribution type STATCOMs have low voltage converter (1kV) which are connected to medium voltage busbar via a coupling transformer. Voltage Source type [12] and Current Source type [11] STATCOMs based on 6-pulse 2-level converters have been investigated and designed. With existing wire-bond IGBTs (3300V, 1200A HV IGBT), maximum STATCOM power can reach approximately ±1.5MVAr [12].

There are three types of multilevel inverters reported in the literature [1,2]:

1. The Diode Clamped Multilevel Inverter (DCMI)
2. The Flying Capacitor Multilevel Inverter (FCMI)
3. The Cascade Multilevel Inverter (CMI)

Multilevel converters have more switching devices with respect to 6-pulse converters. Depending on the number of voltage level, number of switching device can be greater than hundreds. In addition, since the switching devices are not connected in parallel or series, all of the devices have their unique switching signal which complicates the control algorithms. In order to cope with the high number of switching signals, FPGAs (Field Programmable Gate Array) can be used as a switch controller [14]. Selective harmonic elimination or PWM methods have been used for switching waveform generation [5]. Instantaneous voltage and current signals can be processed digitally using a powerful DSP controller. A combination of DSP and FPGA circuits has been used for multilevel inverter control [6].

“Synchronous Static Condenser” or “Synchronous Static Compensator” is the static counterpart of synchronous motor used for reactive power compensation. STATCOM is advantageous from synchronous motor in these respects;

- STATCOM reacts faster
- Each phase of STATCOM can be controlled individually
- STATCOM is maintenance free
- STATCOM has less active loss

STATCOM can be used as reactive power compensator or voltage regulator. By adjusting the reactive power injected to the utility, bus voltage can be adjusted.

STATCOM can generate $\pm Q_{rated}$ reactive power. However the Static VAr Compensator (SVC), which has been used conventionally for static reactive power compensation, needs $2Q_{rated}$ rated thyristor banks and $-Q_{rated}$ harmonic filter banks to generate $\pm Q_{rated}$. In terms of prices, SVC and STATCOM systems produced by Tübitak UZAY Power Electronics Group have similar costs at same power level. In these respects, STATCOM constitutes a promising solution to correct the power quality problems of transmission and distribution systems. STATCOM systems are more expensive than the equivalent SVC systems, and this is the main disadvantage of STATCOM as compared to SVC.

For higher power and voltage level, either multipulse or multilevel converters have been proposed in the literature [2]. Series connection of zig-zag transformers driven by 2 level 6 pulse converters constitutes multipulse converters [18]. Almost all of the implemented medium voltage level STATCOMs are multipulse based, but it can be seen in the literature that multilevel converter based STATCOMs are more and more replacing the multipulse based ones [2]. Among multilevel inverter based STATCOMs as reported in the literature, cascade converter topology turns out to be the most preferred scheme due to its modularity, and least number of components [3] as explained in detail in Chapter 2.

1.2. Scope of the Thesis

Within the scope of the thesis, various multilevel inverter topologies have been investigated for use in STATCOM applications, and the 7-level Cascade Multilevel Inverter topology has been selected for the design and implementation of a 400V ±100kVAr laboratory prototype. First EMTDC/PSCAD simulations of the designed 7-level Cascade Multilevel Inverter based STATCOM have been carried out to verify the converter operation principles. Then the corresponding power stage design has been finalized. The control strategy and the controller parameters of the Cascade Multilevel Inverter based STATCOM have been selected according to the simulation results. A dedicated DSP and FPGA based controller has been developed for the associated multilevel converter control. Multilevel Converter output voltages are obtained. The reactive power response and the harmonic content of the waveforms are discussed.

CHAPTER 2

MULTILEVEL INVERTERS

There are three multilevel inverter topologies, The Diode Clamped Multilevel Inverter (DCMI), The Flying Capacitor Multilevel Inverter (FCMI), and The Cascade Multilevel Inverter (CMI) [1] which can be used in the implementation of of the multilevel inverter based D-STATCOM.

2.1. The Diode Clamped Multilevel Inverter (DCMI)

DCMI consists of a series and interconnected switches, diodes and capacitors. If DCMI is 3 level, then it can be called the Neutral Point Clamped Multilevel Inverter. In Figure 2.1, a 3-level DCMI is drawn. For different switch combinations, phase output voltage with respect to neutral point is given in Table 2-1.

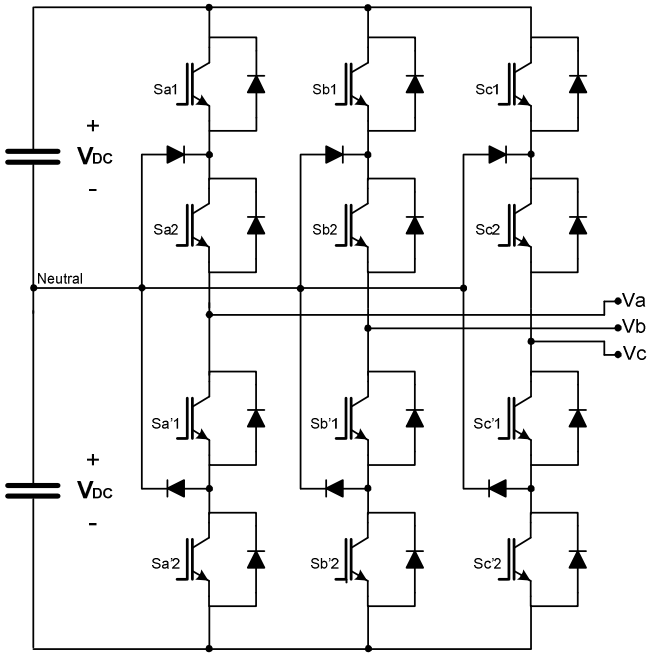

Figure 2.1 3-Level Diode Clamped Multilevel Inverter

Table 2-1 Line to Neutral Levels and Switch States for a 3-Level DCMI

Output Va	Switch State			
	S_{a1}	S_{a2}	S_{a1}'	S_{a2}'
V_{DC}	1	1	0	0
0	0	1	1	0
$-V_{DC}$	0	0	1	1

3-level ±20kVAr DCMI based STATCOM connected to 400V bus is simulated in EMTDC/PSCAD. Converter output voltage waveforms are in Figure 2.2. "Va" is line to neutral voltage measured between "Va" and "neutral" point (Figure 2.1), "Vab" represents Va-Vb.

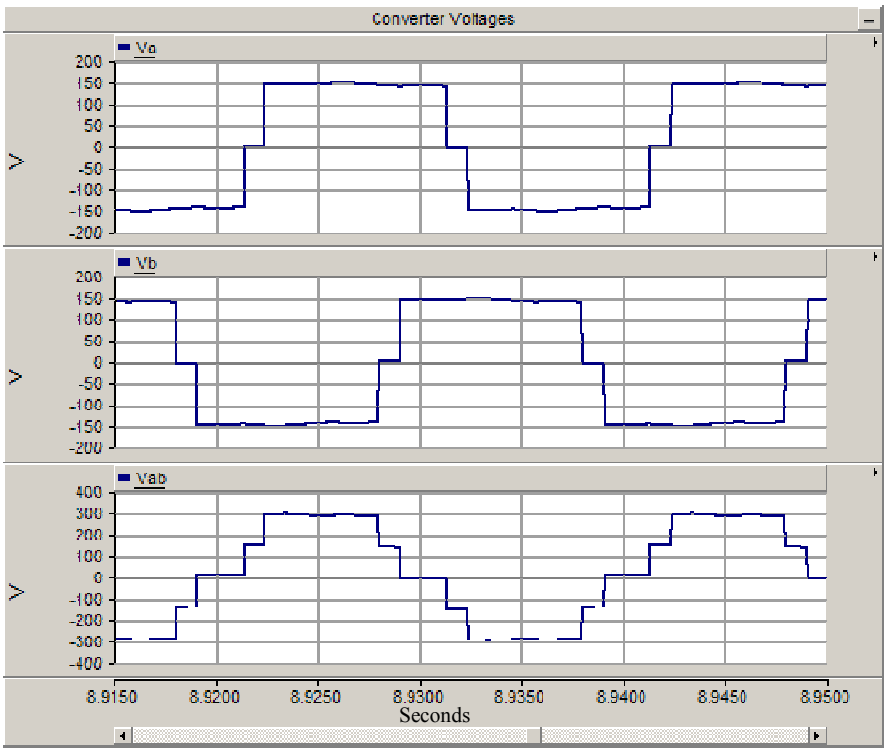

Figure 2.2 Simulation Results, Line to Neutral Voltage (V_a, V_b) and Line to Line Voltage (V_{ab}) of 3-level DCMI (5ms/div)

In Figure 2.3, a 5-Level DCMI is seen. There are six diodes. D_{ca2} diode blocks voltage of three DC capacitors. If clamping diode rating is same with the switching device rating, then D_{ca2} should be replaced by three series connected diodes with voltage rating equal to the switching device. Similarly, D_{ca3} and D_{ca4} should be replaced by two diodes connected in series and D_{ca5} is replaced by three diodes. Total number of diodes increase from 2 to 12 while the voltage level increases from 3 to 5.

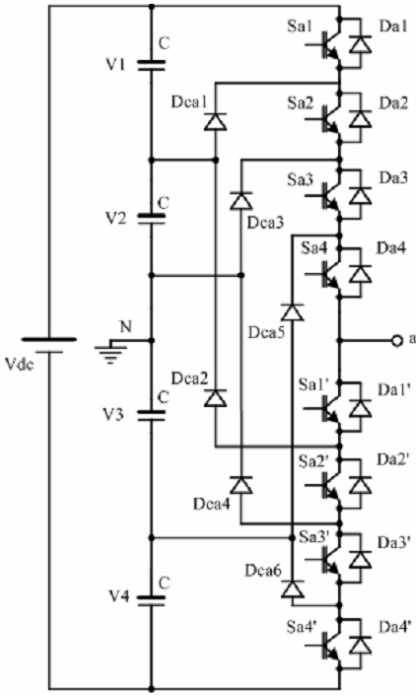

Figure 2.3 One Phase of a 5-Level Diode Clamped Multilevel Inverter [1]

Number of devices can be calculated systematically. Let n_l be the number of levels, n_c be the number of capacitors, n_s be the number of switches and n_{cd} be the number of clamping diodes. Then;

$$n_l = n_c + 1 \tag{2.1}$$

$$n_s = 2(n_l - 1) \tag{2.2}$$

$$n_{cd} = (n_l - 2)(n_l - 1) \ [1] \tag{2.3}$$

Main disadvantage of DCMI is easily seen from the equations. Number of diodes increase with the square of level number. In order to decrease the harmonic content of the converter output voltage waveform, and to increase the converter output voltage magnitude, number of levels should be increased. Beyond 5-level DCMI, clamping diode number and the connection complexity makes the converter nearly impossible to implement. Therefore a different topology is needed.

2.2. The Flying Capacitor Multilevel Inverter (FCMI)

FCMI generates multilevel voltage waveforms like DCMI. Instead of diodes, capacitors clamp the output voltage (Figure 2.4).

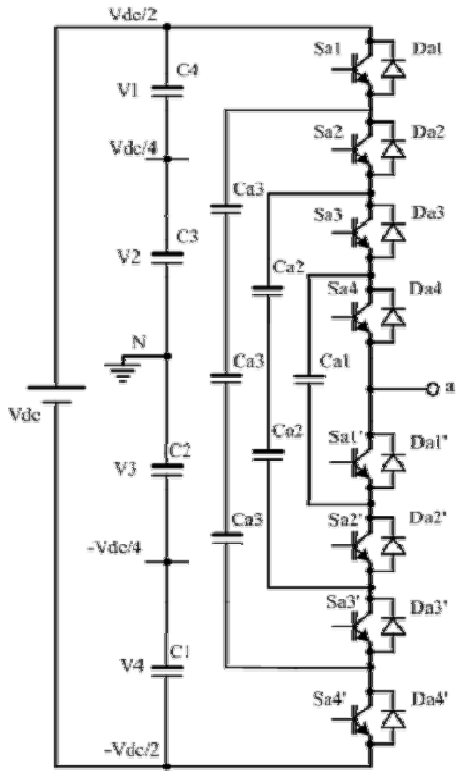

Figure 2.4 A 5-Level Flying Capacitor Multilevel Inverter [1]

In Table 2-2, switch states for different voltage levels are tabulated.

Table 2-2 Line to Neutral Levels and Switch States for a 5-Level FCMI [2]

Output Va	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a4}'	S_{a3}'	S_{a2}'	S_{a1}'
$V_{DC}/2$	1	1	1	1	0	0	0	0
$V_{DC}/4$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$-V_{DC}/4$	1	0	0	0	1	1	1	0
$-V_{DC}/2$	0	0	0	0	1	1	1	1

Equations for number of devices can be written as:

$$n_l = n_c + 1 \tag{2.4}$$

$$n_s = 2(n_l - 1) \tag{2.5}$$

$$n_{cc} = (n_l - 2)(n_l - 1)/2 \text{ [1]} \tag{2.6}$$

where n_l is the number of levels, n_s is the number of switching devices and n_{cc} is the number of clamping capacitors. Equation 2.6 clarifies that FCMI suffers from high number of clamping capacitors, as the level number increases.

2.3. Cascade Multilevel Inverter (CMI)

H-Bridge in Figure 2.5 can generate $+V_{DC}$ when S_1 & S_3 are on, and $-V_{DC}$ when S_2 & S_4 are on. By connecting H-Bridges serially, a Y connected CMI can be realized as shown in Figure 2.6.

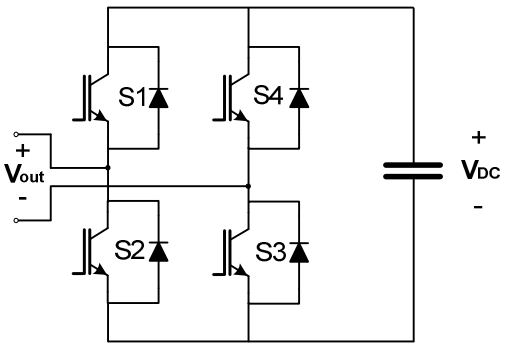

Figure 2.5 H-Bridge

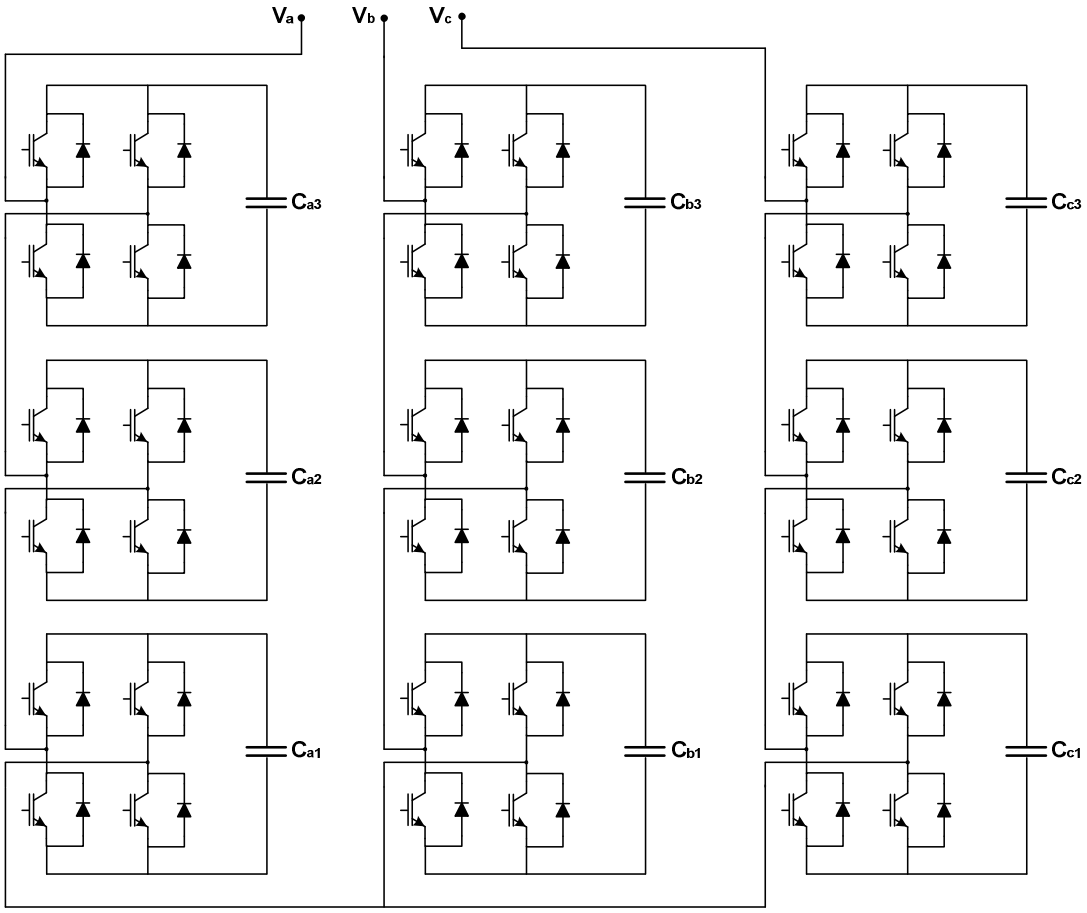

Figure 2.6 A 7-Level Cascade Multilevel Inverter with IGBT Switches

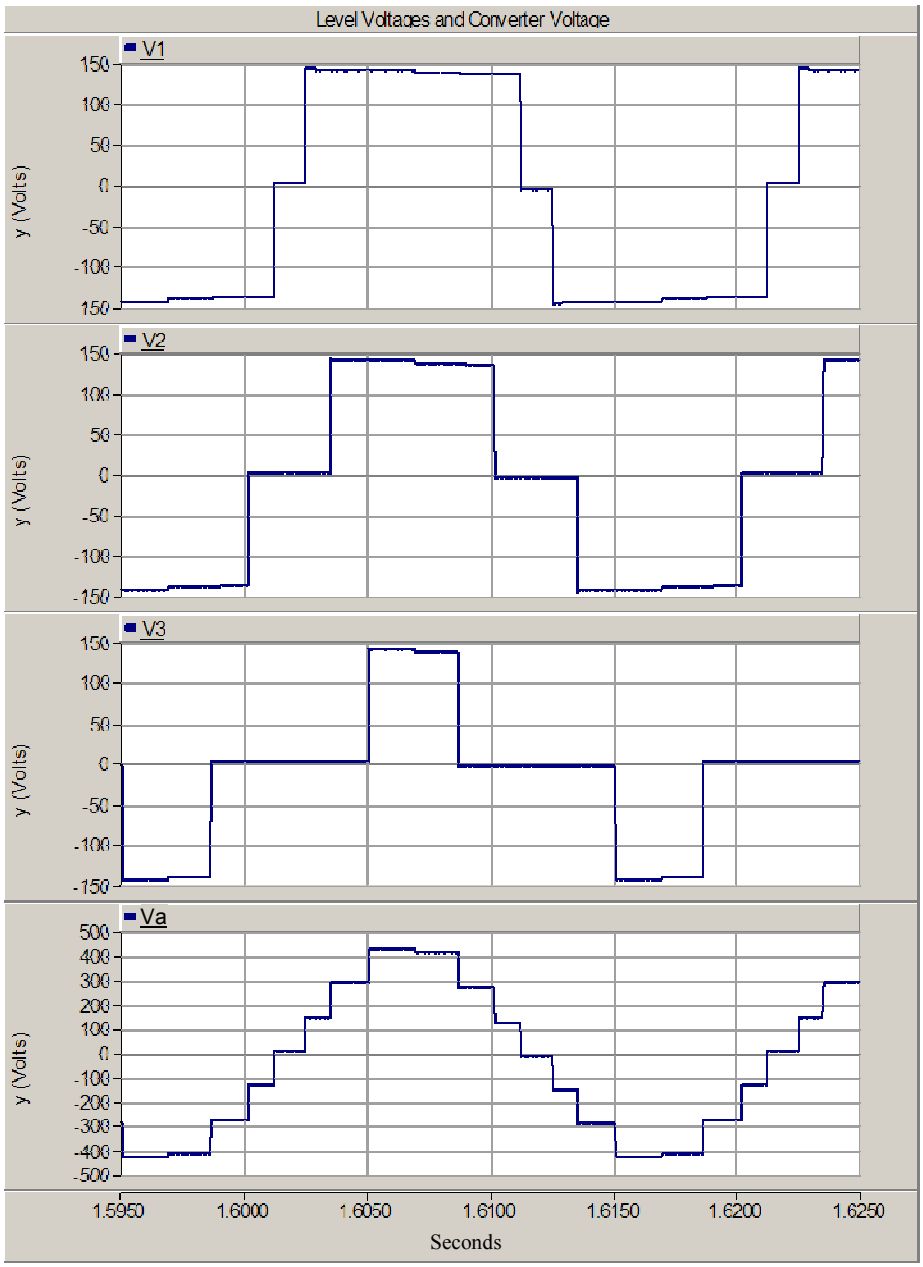

Figure 2.7 Simulation Results, H-Bridge Output Voltages and Sum of Them: Converter Line to Neutral Voltage (5ms/div)

Since H-Bridges are connected serially, their output voltages are summed and CMI line to neutral voltage is obtained (Figure 2.7). Selective harmonic elimination (SHEM) is used to find the switching angles in Figure 2.7.

Let n_c be the number of H-Bridges, n_l is the number of levels and n_s is the number of switches with anti parallel diodes.

$$n_l = 2n_c + 1 \tag{2.7}$$

$$n_s = 2(n_l - 1)\ [1] \tag{2.8}$$

2.4. Comparison of Multilevel Inverters

Multilevel Inverters are compared in terms of number of components in Table 2-3 to Table 2-6. In these tables, number of devices used in CMI are defined as follows:

n_s : Number of switching devices.
n_c : Number of DC-Link capacitors.
n_{cc} : Number of clamping capacitors.
n_{cd} : Number of clamping diodes.

Table 2-3 Number of Components per Phase for 5-Level Converter

Topology	n_s	n_c	n_{cc}	n_{cd}
DCMI	8	4	-	12
FCMI	8	4	6	-
CMI	8	2	-	-

Table 2-4 Number of Components per Phase for 7-Level Converter

Topology	n_s	n_c	n_{cc}	n_{cd}
DCMI	12	6	-	30
FCMI	12	6	15	-
CMI	12	3	-	-

Table 2-5 Number of Components per Phase for 11-Level Converter

Topology	n_s	n_c	n_{cc}	n_{cd}
DCMI	20	10	-	**90**
FCMI	20	10	**45**	-
CMI	20	5	-	-

Table 2-6 Number of Components per Phase for 15-Level Converter

Topology	n_s	n_c	n_{cc}	n_{cd}
DCMI	28	14	-	**182**
FCMI	28	14	**91**	-
CMI	28	7	-	-

In CMI, number of devices increases linearly. Therefore CMI is preferable to DCMI and FCMI at medium voltage applications, where high number of levels is needed.

As number of levels increase, converter voltage increases. With enough number of levels, connection to medium voltage buses without a coupling transformer can be implemented. 6500V IGBTs, which are the highest voltage switches commercially available, can operate at 4500V DC-Link voltages [13]. Peak line to neutral voltage of a multilevel converter built with 6500V IGBTs can be found by multiplying 4500V with the number of dc link capacitors. By this way, Table 2-7 is generated. In Table 2-7, applicability of the indicated number of levels to medium voltage buses in Turkey is investigated.

Table 2-7 Line to Line Medium Voltage Levels in Turkey and Applicability of Multilevel Inverters (built with 6500V IGBTs) in terms of Level Number

CMI Line to Neutral Voltage Level:	Maximum Achievable Line to Line Voltage:	6.3kV	10.5kV	15kV	31.5kV	33kV	34.5kV
5-level	11kV	✔	✔	-	-	-	-
7-level	16,5kV	✔	✔	✔	-	-	-
11-level	27kV	✔	✔	✔	-	-	-
13-level	33kV	✔	✔	✔	✔	✔	-
15-level	38kV	✔	✔	✔	✔	✔	✔

CHAPTER 3

CASCADE MULTILEVEL INVERTER BASED STATCOM

In this chapter, basic operating principles of voltage source converter (VSC) based STATCOM are discussed and simulation results concerning a 7-level CMI based STATCOM operation are given both in the steady-state and transient state. Voltage equalization problem of CMI based STATCOM and the performance of the proposed selective swapping method has been assessed.

3.1. Statcom Operating Principles

A single phase STATCOM model is given in Figure 3.1 [12]. Electrical parameters can be defined as follows:

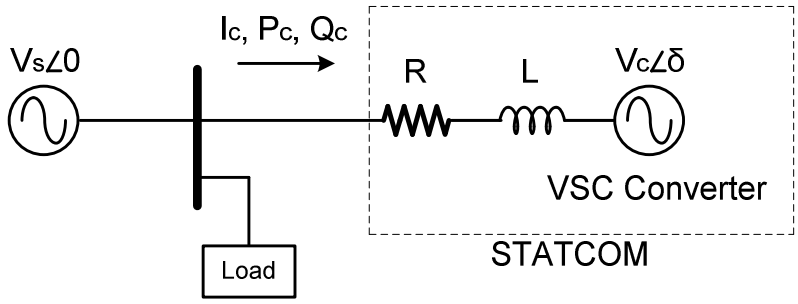

Figure 3.1 Simple STATCOM Model

Vs : RMS line to neutral source voltage

Vc : RMS line to neutral converter voltage

Ic : RMS STATCOM current

Qc : STATCOM reactive power

Pc : STATCOM active power

δ : Phase difference between source and converter

R : Resistor representing total loss of converter and coupling equipments

L : Inductor representing total inductance of coupling reactor and coupling transformer.

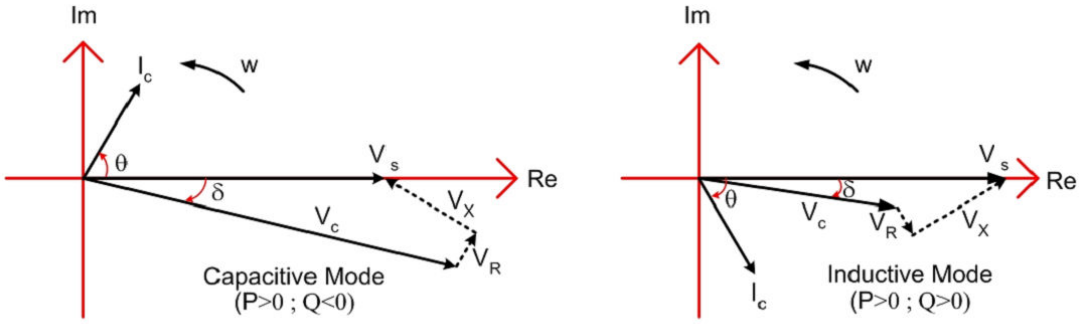

Figure 3.2 Phasor Diagrams for Lossy STATCOM [12]

By using the phasor diagrams in Figure 3.2, source voltage can be written as :

$$\overrightarrow{V_s} = \overrightarrow{V_c} + \overrightarrow{V_R} + \overrightarrow{V_X} \tag{3.1}$$

$$\overrightarrow{V_X} = jXI_c \tag{3.2}$$

$$\overrightarrow{V_R} = RI_c \tag{3.3}$$

Where $X = 2\pi fL$,

$$V_s - V_c \cos\delta = I_c(Rcos\theta + Xsin\theta) \tag{3.4}$$

$$V_c sin\delta = I_c(Xcos\theta - Rsin\theta) \tag{3.5}$$

Reactive and active power of STATCOM can be written as:

$$P_c = V_s I_c cos\theta \tag{3.6}$$

$$Q_c = V_s I_c cos\theta \tag{3.7}$$

In terms of X & R, STATCOM reactive power can be written as:

$$Q_c = V_s \frac{V_s - V_c cos\delta}{Rcos\theta + Xsin\theta} sin\theta \tag{3.8}$$

As R becomes zero, STATCOM become lossless and STATCOM reactive power can be written as in (3.9). Phasor diagram of lossless STATCOM is given in Figure 3.3 .

$$Q_c = V_s \frac{V_s - V_c}{X} \tag{3.9}$$

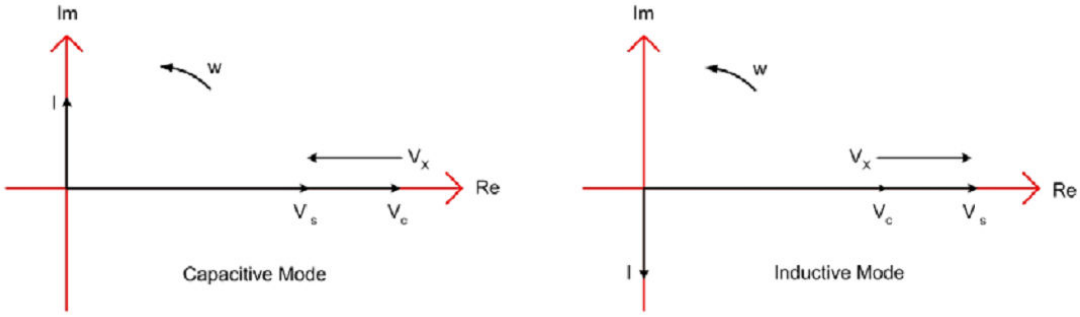

Figure 3.3 Phasor Diagrams for Lossless STATCOM [12]

STATCOM reactive power can be adjusted by varying V_c. Three methods can be used to vary V_c:

i. Varying modulation index (m),
ii. Varying DC-Link voltage,
iii. Using both (i) and (ii).

3.2. Switching and Control Algorithm

It has been mentioned in the literature that, among the multilevel inverter topologies used for STATCOM applications, the cascaded multilevel topology is the most advantageous and economical one [1-5]. On the other hand, the main problem of this topology comes out to be the difficulty of sustaining the DC capacitors' mean voltages. This issue is very important for obtaining an output voltage with low total harmonic distortion (THD) and having equal device stresses. In this work, a new DC voltage balancing method (Selective-Swapping Algorithm) for cascaded multilevel inverter based STATCOM applications is investigated and the results are given. Moreover, these results are compared with the ones obtained for the other DC voltage equalization methods given in the literature.

One of the main control difficulties in the CMI based STATCOMs is to balance the DC capacitor voltages, in order to maintain low THD in inverter output voltage, equal stresses on the switches and correct elimination of the unwanted low order harmonics such as the 5th, 7th, etc. For this reason, the DC link voltages of every H-Bridge (HB) should be equal, which means that a reliable capacitor voltage equalization algorithm should be used. In this work, a new approach (Selective-Swapping Algorithm) based on the use of switch combination redundancies for equalization of DC capacitor voltages has been proposed and the results have been compared with those given in the literature [4, 5].

The schematic of the 7-level VSC-based CMI is given in Figure 3.4. The phases of this topology consist of HBs connected in series. For a CMI with 3 H-Bridge per phase, there exists three DC capacitors for each phase (n_c=3). Selective harmonic elimination technique is used in this study. This means that the number of inverter line to neutral output voltage levels is given by $n_l = 2n_c + 1 = 7$ whereas; it is $n_{l3\emptyset} = 4n_c + 1 = 13$ for the inverter line to line output voltage. As the number of HBs used increases, the number of harmonics that can be eliminated from the output voltage increases. Thus, the output voltage converges to a sinusoidal waveform and the THD decreases.

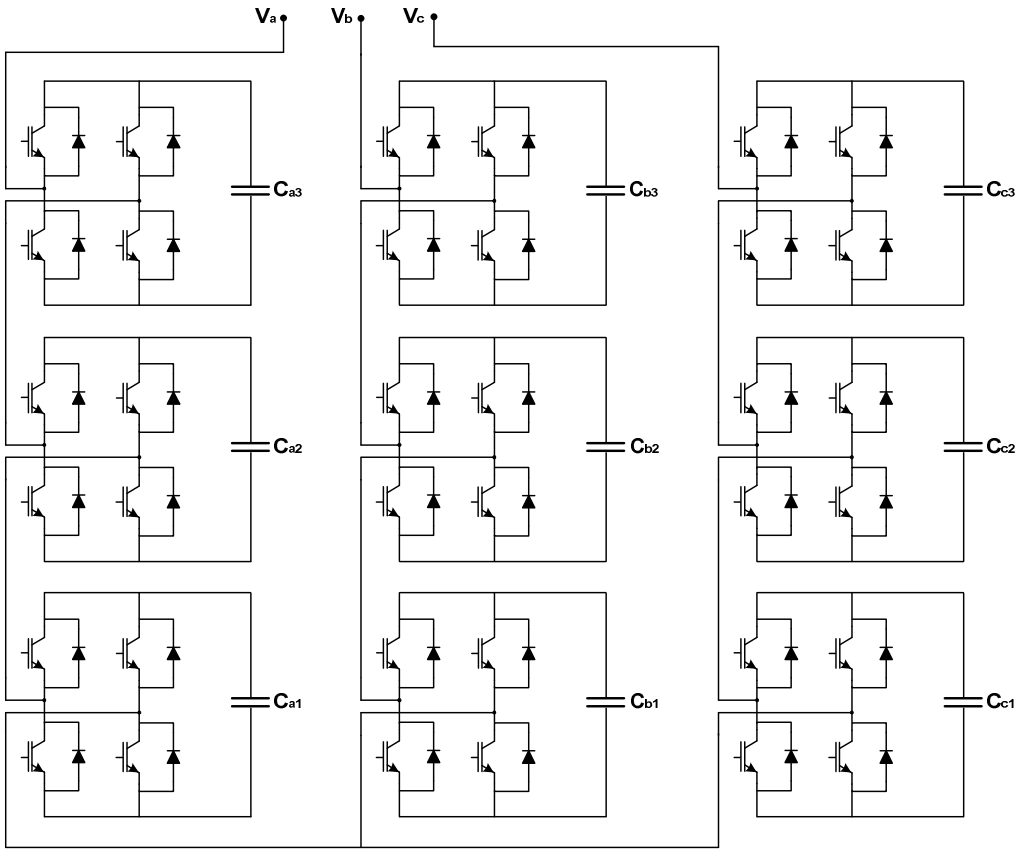

Figure 3.4 A 7-Level Cascade Multilevel Inverter with IGBT Switches

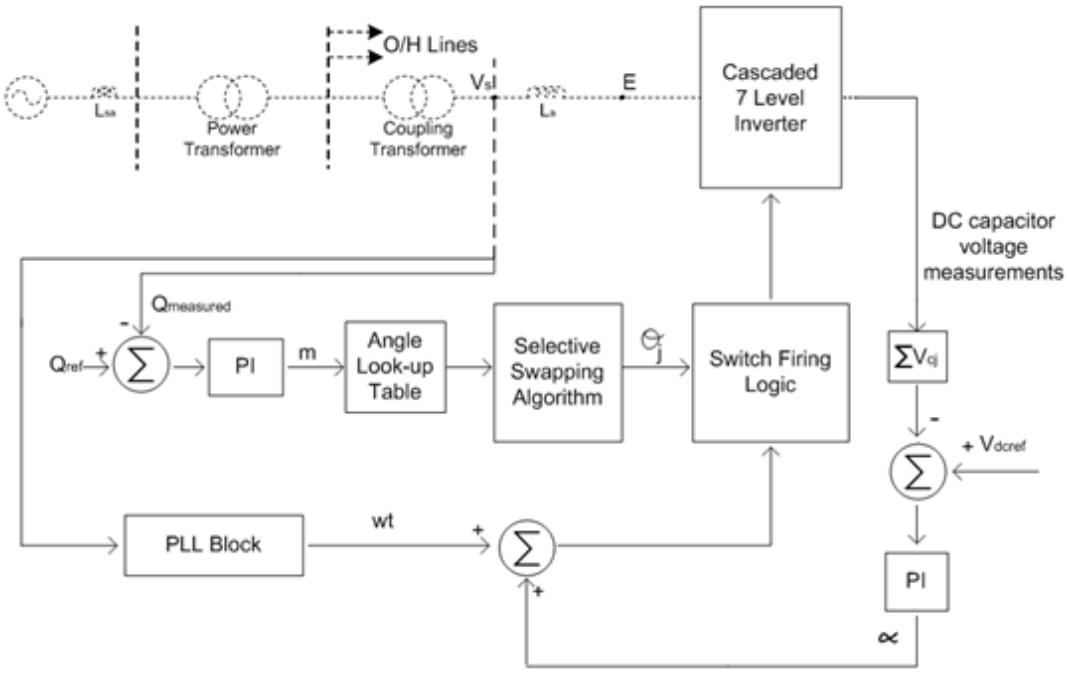

Figure 3.5 Block Diagram of the Cascaded 7-Level Inverter Prototype

Since there are three H-Bridges per phase, 2 harmonics can be eliminated in the output voltage waveform [3]. Switching angles are found by running genetic algorithms to solve the equations below:

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = m \tag{3.10}$$

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \tag{3.11}$$

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0 \text{ [10]} \tag{3.12}$$

"m" is the modulation index. Since 3rd harmonic is absent in a balanced system with no neutral wire, 5th and 7th harmonics are the most important ones to be eliminated.

3.2.1. Voltage Equalization Problem of DC Link Capacitors

In STATCOM operation, the CMI is intended to produce reactive power only, but due to the losses existing in the overall system, some real power is lost, resulting in the variation of mean capacitor voltages.

The real power flow into and out of the capacitors is controlled by adjusting phase difference α (in Figure 3.2 α is represented as δ) between the system and inverter output voltages. In order to equalize the capacitor voltages in each string, one of the conventional methods adopted is to control the total DC capacitor voltage per phase by adjusting α, and individual DC capacitor voltages by shifting switching angles of each HB by an amount of ±Δα [3]. However, this method may give unsatisfactory results as seen in Figure 3.6 for some operating points (reactive power outputs), and cause oscillations or divergence of the capacitors' mean voltages, because the corresponding PI parameters used to determine α and Δα may be time-consuming, and difficult to find. Moreover, the PI controls of α and Δα may interact with each other, resulting in instability. Another conventional method is to use α control only, and to swap the switching angles for HBs in every half-cycle. However, this method causes even more oscillations in the capacitor mean voltages, and is not stable for every reactive power reference (Q_{ref}) as seen from Figure 3.7.

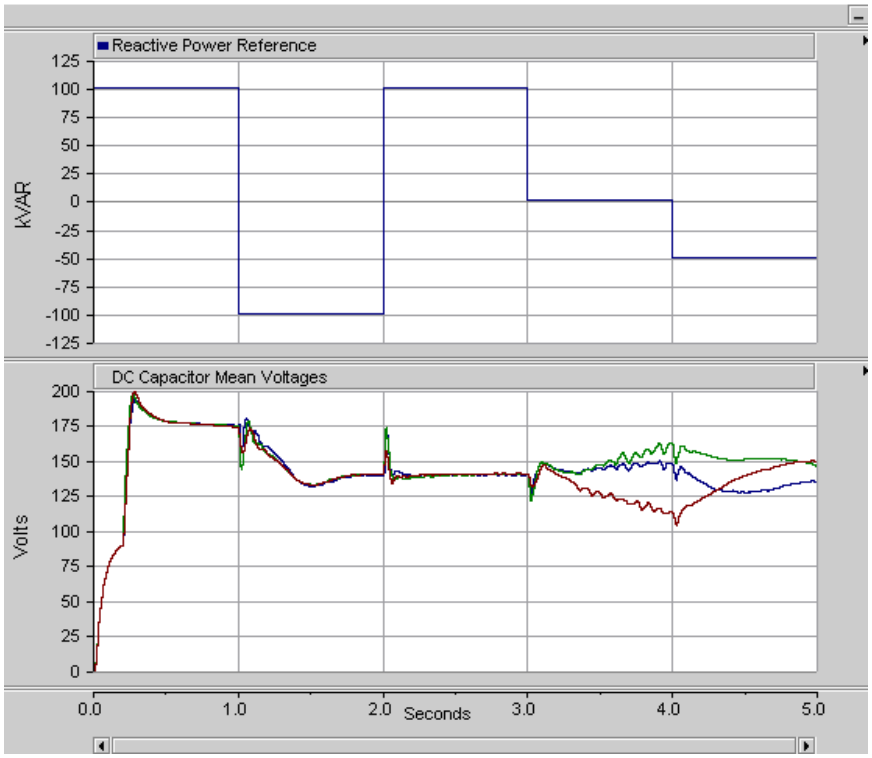

Figure 3.6 Single Phase Capacitor Mean Voltage Variations for α Control and Rotational Swapping

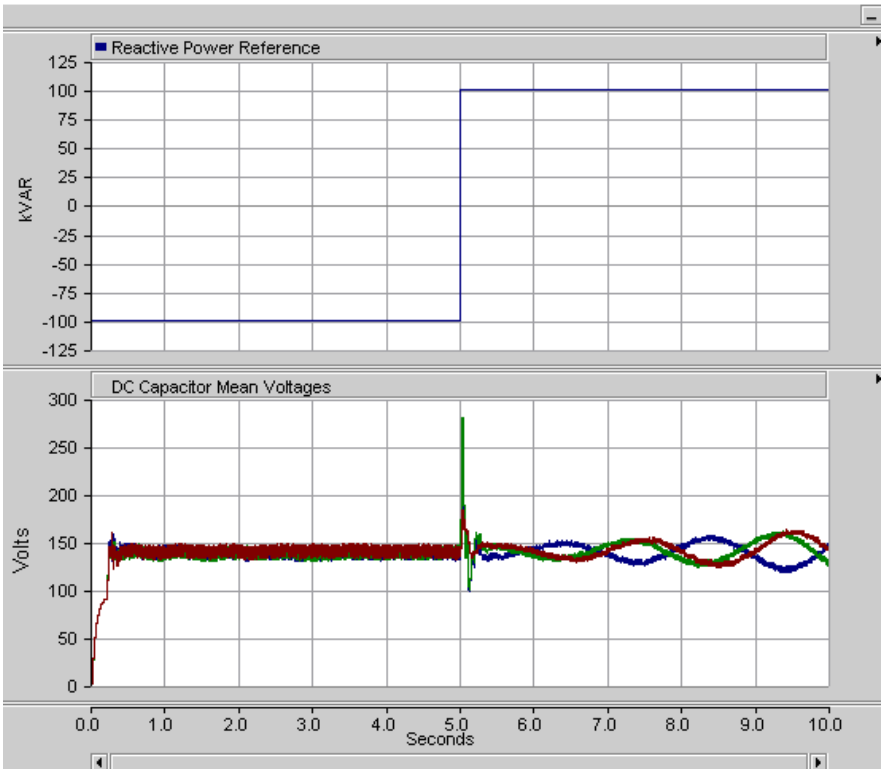

Figure 3.7 Single Phase Capacitor Mean Voltage Variations for α & Δα Control

Equalizing performance of both rotation method and α & Δα method is low. If disturbing forces which makes capacitor voltages unequal is greater than the equalizing capability, then capacitor voltages become divergent.

On the other hand; the method proposed in [6] uses different switch combinations at the instants of level changes. This method becomes unsatisfactory for high power applications with low DC capacitor voltage value. Performance of the method in [6] is discussed in Table 3.1. In order to improve this method based on the switch combination redundancies, a new algorithm is developed.

3.2.2. Proposed Selective Swapping Method for Voltage Equalization of DC Link Capacitors

In order to solve the unbalance problem in capacitor DC voltages, selective swapping of switching angles, which makes use of switch redundancy combinations of HBs, is applied multiple times during mid-levels, if necessary. To show the effectiveness of the method proposed herein, a 3-phase, 7-level inverter based STATCOM has been investigated (Figure 3.8). A typical 7- level inverter output voltage waveform has levels $+3V_{dc}$, $+2\ V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$, and $-3V_{dc}$ (Figure 3.8).

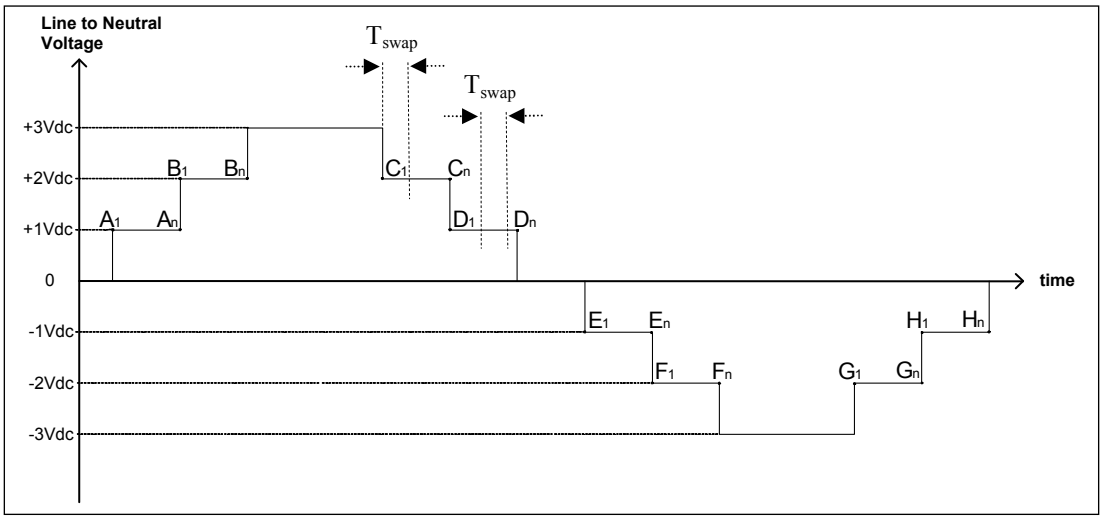

Figure 3.8 Typical Output Phase Voltage of the Inverter

Instead of swapping the angles every half cycle, a logical combination of HBs that will be in conduction is determined at mid-levels +2 V_{dc}, +V_{dc}, -V_{dc}, and -2V_{dc}. Each capacitor voltages are measured in each phase, and they are sorted with respect to their instantaneous values. Also, monitoring the direction of current, the algorithm determines whether the inverter is in charging mode or discharging mode. The aim is to charge the capacitor with the lowest voltage when the inverter is in charging mode, therefore the HB(s) with the lowest capacitor voltage(s) is (are) taken into conduction. On the other hand, when the inverter is in discharging mode, the HB(s) with the highest capacitor voltage(s) is (are) taken into conduction. This operation can be applied at the instant of level changes only corresponding to points A_1, B_1,…,H_1 in Figure 3.8. However, it is needed to apply selective swapping more frequently, when the ripple factor, $(Q_{rated}/V_{rated}.V_{dcset}.C)$ is high, where Q_{rated} is the maximum reactive power output, V_{rated} is the rated output AC voltage, and C is the capacitance of every capacitor.

To solve the problem of changing mean capacitor voltages, as a new approach proposed in this work, selective swapping of switching pulses can be applied several times additionally at critical points between $A_1 - A_n$, $B_1 - B_n$, …, $H_1 - H_n$ during all the mid-levels seen in Figure 3.8. Thresholds are defined for capacitor voltages in

order to decide whether another swapping is needed or not. As a result, the number of swappings for each mid-level may be different. However, the minimum duration between two consecutive swappings (T_{swap}) can be optimized. It is obvious that the switching losses of the inverter will increase for the proposed method, so a compromise should be made, considering between capacitance values and switching loss.

3.3. Simulation Results

A 400V, ±100kVAr 3-phase 7-level STATCOM prototype given in Figure 3.5 with the parameters L_a= 1.6mH, and C = 22mF/HB has been simulated. Selection procedure of these values is further discussed in 4.1.2 and 4.3.1. Overall schematics of the simulated CMI based STATCOM in PSCAD/EMTDC are given in Appendix-A. The prototype responds to reactive power demand by changing the modulation index (m) [7]. There are two PI controllers, one is used for reactive power control (proportional parameter is K_{PQ} and integral parameter is K_{IQ}) and the other one is used for active power control (proportional parameter is $K_{P\alpha}$ and integral parameter is $K_{I\alpha}$). By using Ziegler-Nichols method, PI parameters are optimized.

Table 3-1 Simulation Parameters

	Value
Coupling Inductor	L_a= 1.6mH
DC-Link Capacitor	C = 22mF/HB
K_{PQ}	6
K_{IQ}	40
$K_{P\alpha}$	5
$K_{I\alpha}$	0.007

3.3.1. Simulation Results of Selective Swapping Method

The capacitors' mean voltage waveforms are given in Figure 3.9 for the proposed method. Comparison results for different values of T_{swap} are given in Table 3.1.

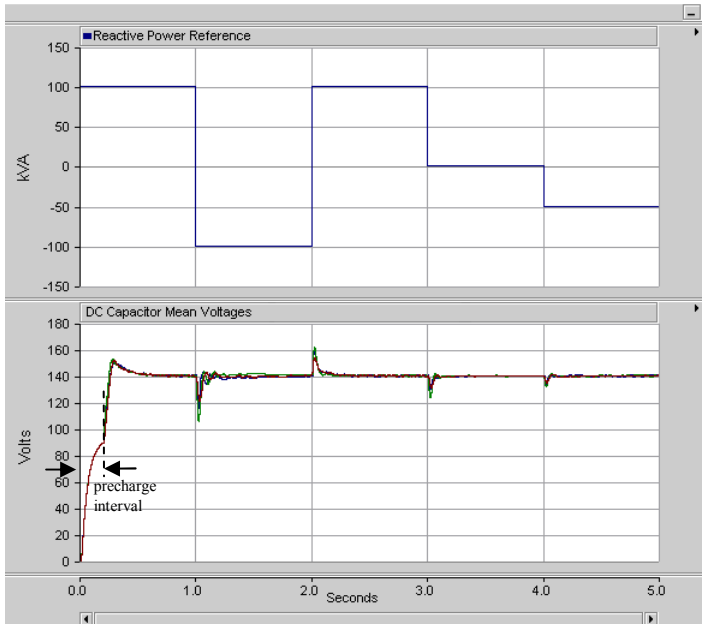

Figure 3.9 Capacitors' Mean Voltage Variations

Conventional methods for equalization of DC capacitor mean voltages do not give satisfactory results for all operating points of CMI based voltage source STATCOM applications. The proposed method based on a selective-swapping algorithm has shown better performance in balancing the DC link voltages than conventional methods, especially for low capacitor voltage, high power applications. The EMTDC/PSCAD simulations carried out on a 3-phase, 7-level CMI based STATCOM have shown the success of the proposed method for all operating points. The method can be optimized by changing the minimum period between two consecutive swappings (T_{swap}) in order to minimize the ripple factor and the THD of inverter output voltage. A compromise should be made between switching loss and value of capacitance (and/or THD).

Table 3.2 Comparison of the System Performances for Different T_{swap} Values

Case No	Parameters	Q rise time	Q fall time	Q rise peak	Q fall peak	Q ripple (+100kVAr)	Q ripple (-100kVAr)	Capacitor DC Voltage Ripple (+100 kVAr)	Capacitor DC Voltage Ripple (-100 kVAr)	Capacitor AC Voltage Ripple (+100 kVAr)	Capacitor AC Voltage Ripple (-100 kVAr)	Maximum Capacitor Voltage
1	Tswap=200µS	133ms	107ms	103.5kVA	113.2kVA	0.41%	0.72%	0.30%	0.54%	3.39%	10.3%	177.97Volts
2	Tswap=400µS	133ms	107ms	103.5kVA	113.2kVA	0.40%	0.66%	0.33%	0.92%	3.71%	10.5%	179.60Volts
3	Tswap=800µS	133ms	107ms	103.4kVA	113.0kVA	0.35%	0.71%	1.29%	1.04%	5.40%	11.4%	180.56Volts

3.3.2. Simulation Results of CMI based STATCOM Operation

In this section, the operation of CMI based STATCOM is simulated in EMTDC/PSCAD to obtain the reactive power response, and the performance of the associated control system using the general block diagram given in Figure 3.5. The corresponding schematics of the simulation circuit is given in Appendix-A.

In Figure 3.10, for a custom reactive power reference scenario (+100kVAr, -100kVAr, +100kVAr, 0VAr, -50kVAr), reactive power and modulation index response is obtained. Settling time of reactive power is around 200ms.

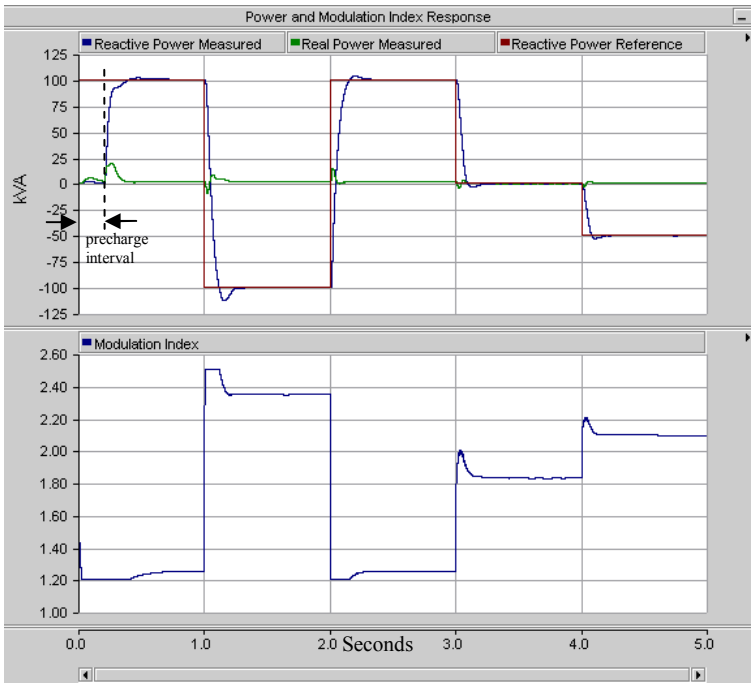

Figure 3.10 Reactive Power Response

Ziegler Nichols method is used to adjust the PI parameters of the reactive power controller in Figure 3.5. Transient response can be improved if PI parameters of the controller are fine tuned. Feed-forward control can be added to the control loop to improve the transient response further.

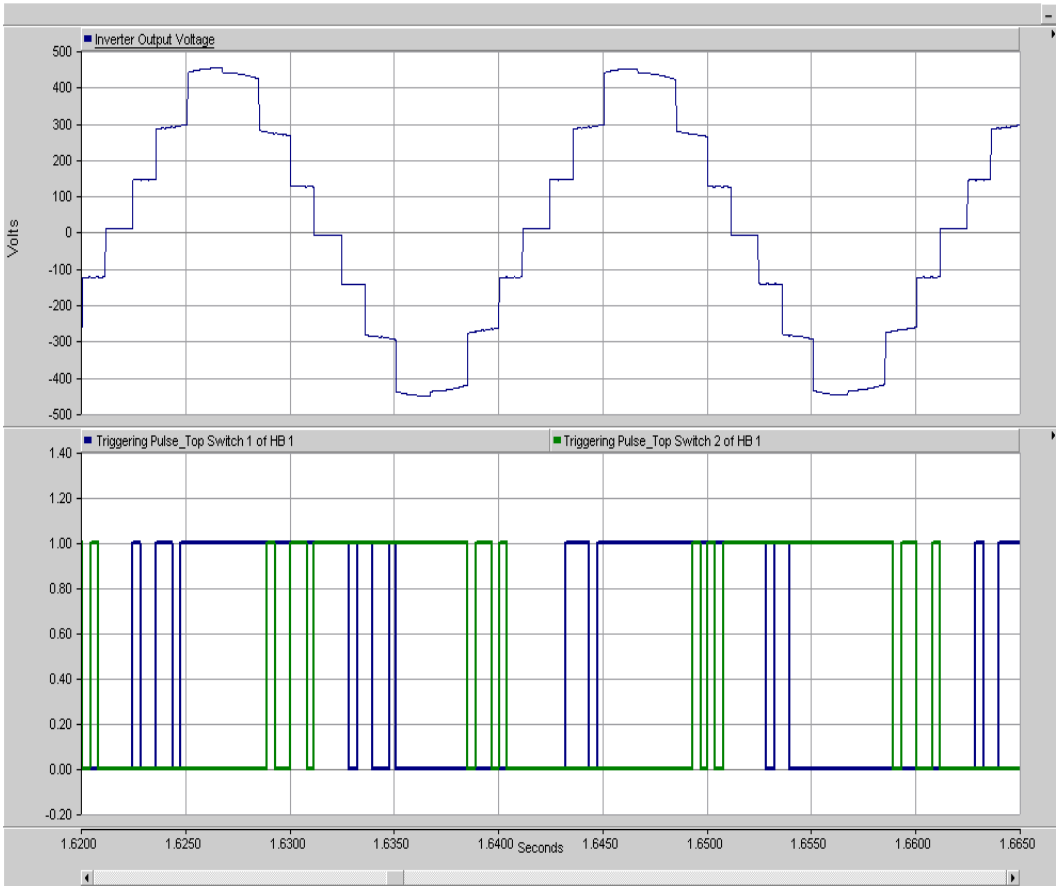

Figure 3.11 Practical Switching Signals for the Upper two Devices of a HB

The proposed voltage equalization method is applied with T_{swap} = 400µsecs. A practical switching frequency for any semiconductor is around 250-300 Hz at maximum as seen in Figure 3.11 and Figure 3.12, since there is no need for swapping operation for levels $+3V_{dc}$, 0, and $-3V_{dc}$ and, the swapping operation for mid - levels is applied every 400µsecs, if it is needed.

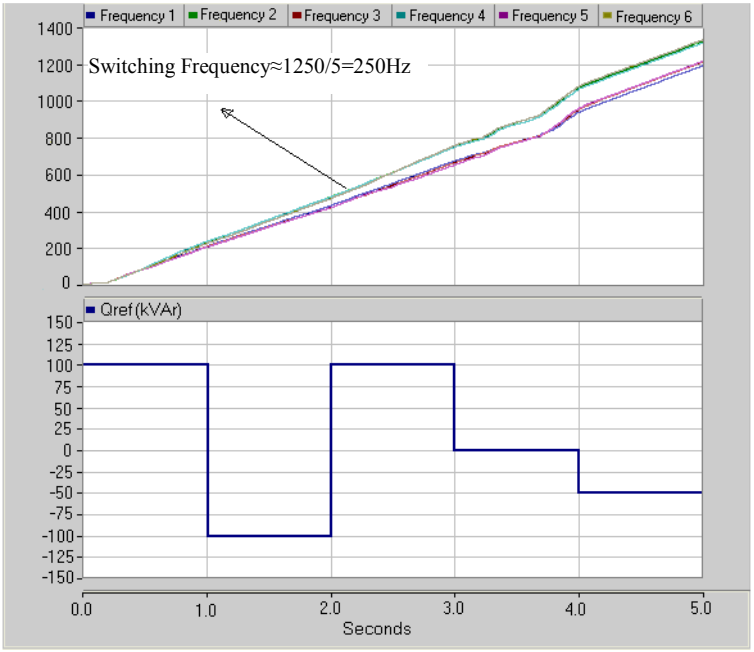

Figure 3.12 Total Number of Switching for the Upper Devices of a Phase for Duration of 5 Seconds

CHAPTER 4

DESIGN AND IMPLEMENTATION OF 7 LEVEL CASCADED MULTILEVEL INVERTER BASED STATCOM

The 7-level CMI based STATCOM is designed and implemented within the scope of the thesis. The circuit diagram of the implemented CMI including the coupling and protection circuits is given in Figure 4.1.

4.1. H-Bridge Design of CMI

4.1.1. Switching Device

For a 400V line-to-line, 100kVAr laboratory prototype, RMS current is calculated in (4.1).

$$I = \frac{100000}{V_{ll}.\sqrt{3}} = 144\text{A} \tag{4.1}$$

Peak current is 204A. At switching instants, the switch current can reach 300A. Therefore, a 400A switch is selected. Intelligent Power Modules (IPM) have IGBT and gate driver in one package. Since IPMs are easy to use and compact, they are used in the implementation. PM400DSA60 [17] has an IGBT leg which consists of two IGBTs. Hence, two IPMs are sufficient to construct the H-Bridge given in Figure 2.5.

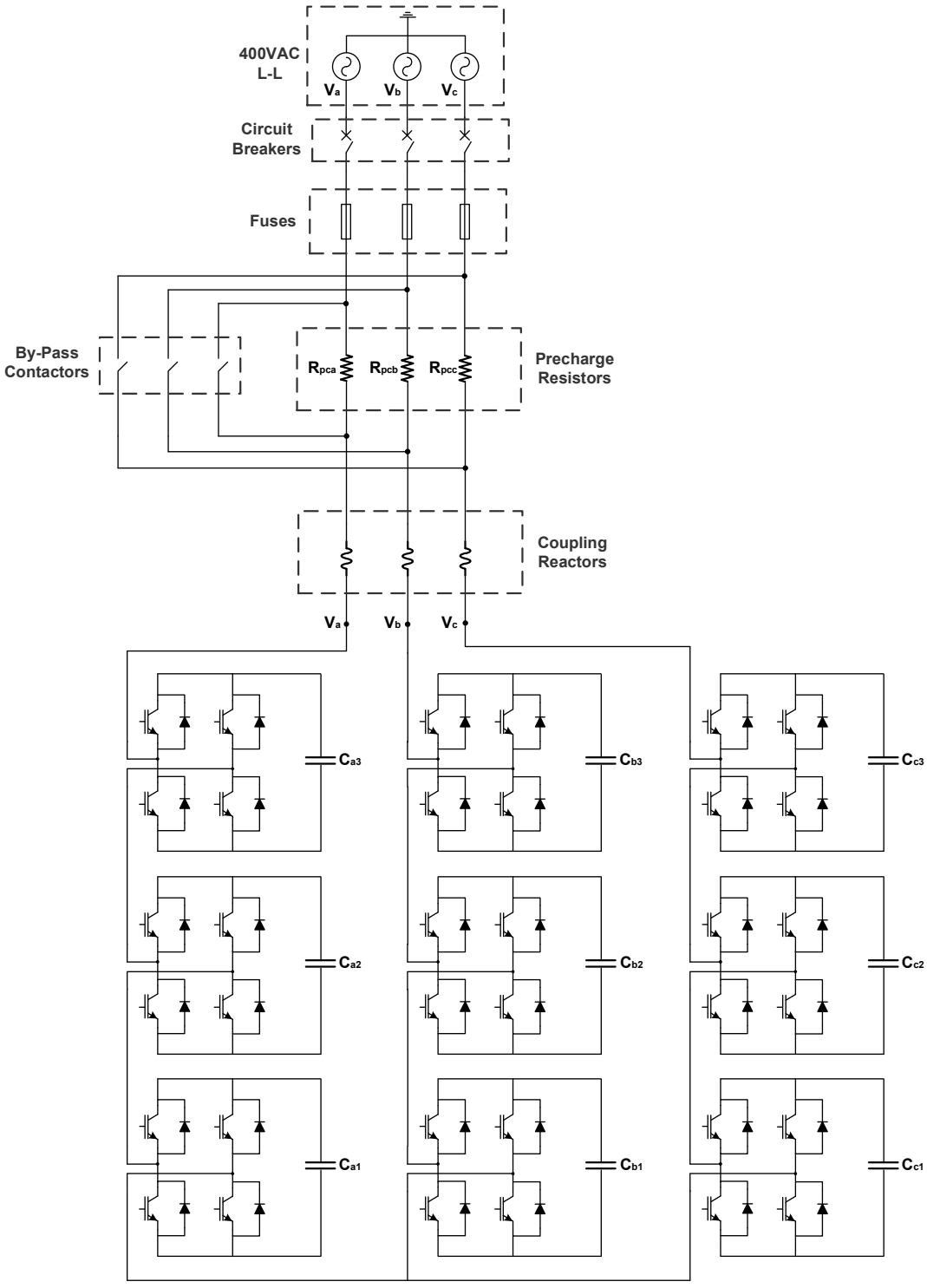

Figure 4.1 7 Level CMI based STATCOM

4.1.2. DC-Link Capacitor

DC link voltage of H-Bridge is set to 140V. If DC-Link voltage is decreased, then modulation index of the converter should be increased to maintain same converter output voltage. The converter output voltage has low harmonic distortion for a specified modulation index range. In order to use the low harmonic distortion range, 140V DC Link voltage is selected. At full capacitive power, RMS current of DC Link capacitors reach 80A (Figure 4.2). Therefore four capacitors with rated RMS current of 25A are connected in parallel. In order to keep capacitor voltage ripple less than 10%, capacitance of each capacitor is selected as 6800µF from simulations carried out using the selective swapping algorithm explained in section 3.2.

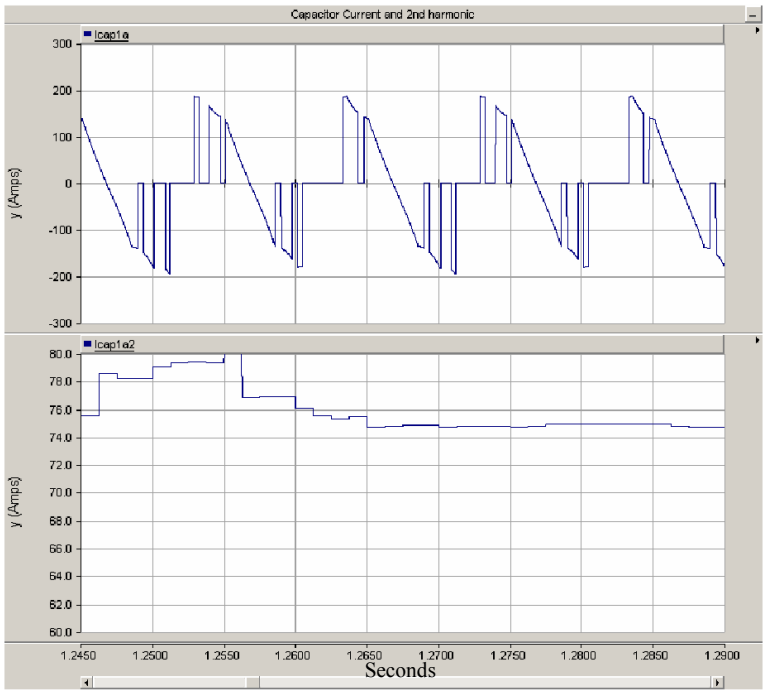

Figure 4.2 Capacitor Current Waveform and RMS Current

4.1.3. Busbar

Busbar inductance is tested with the circuit in Figure 4.3. Test setup is seen in Figure 4.4.

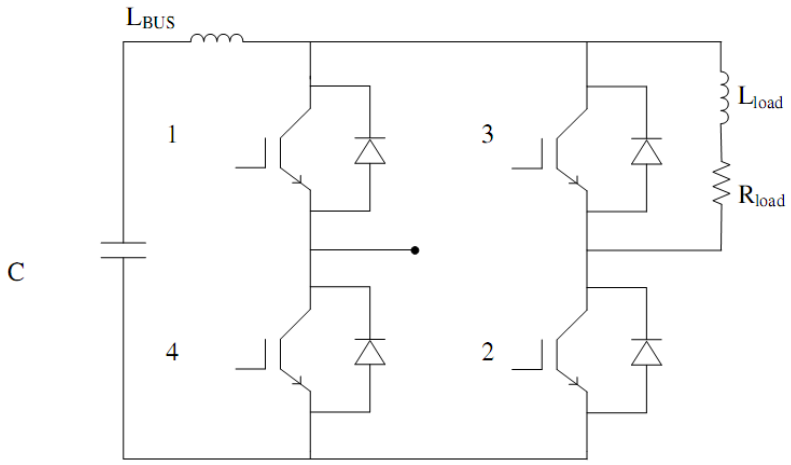

Figure 4.3 Switching Test Circuit

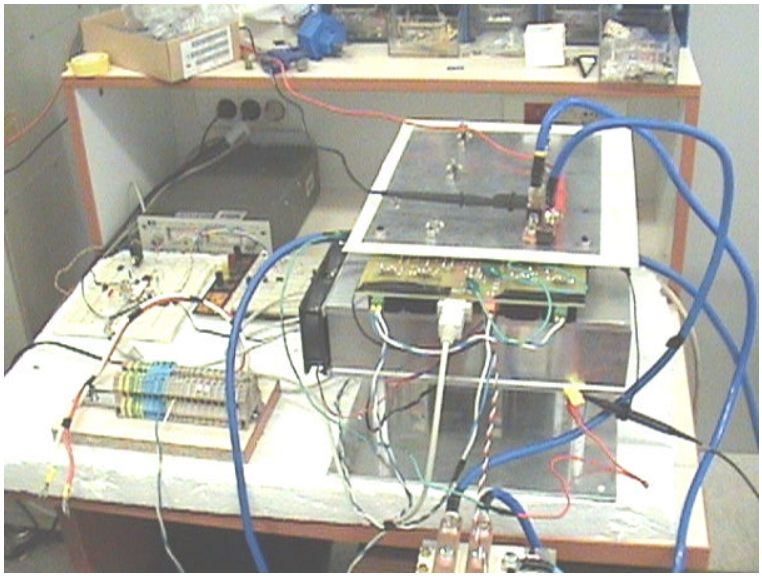

Figure 4.4 The Setup to Test the Busbar Inductance

First, DC-Link capacitors are charged to 125V. Then IGBT 2 is switched on. When load current reaches the test current (≈150A), IGBT 2 is turned off to investigate the turn off operation. All other IGBTs are kept in off state during the test.

Technical specifications of the components used in the test are given in Table 4-1. First, tests are carried out without 3µF snubber capacitor connected in parallel to the DC-Link. Finally, tests are repeated with the snubber capacitor connected.

Table 4-1 Switching Test Setup Component Technical Specifications

Component	**Specifications**
IPM	600V, 400A Dual Pack
L_{Load}	400V, 1.6mH, 150A
R_{Load}	25kW, 0-2,5Ω
C	415V, 4×6800µF

Following points are calculated from measurements taken during the tests:

- Busbar inductance value
- IPM collector current fall time
- Maximum di/dt value the collector current

Furthermore, the necessity of using snubber capacitors has been investigated.

While collector current of IGBT 2 is 162.5A and DC-Link voltage is 125V, IGBT 2 is switched off and the waveform in Figure 4.5 is acquired. The results obtained from the waveform are given in Table 4-2.

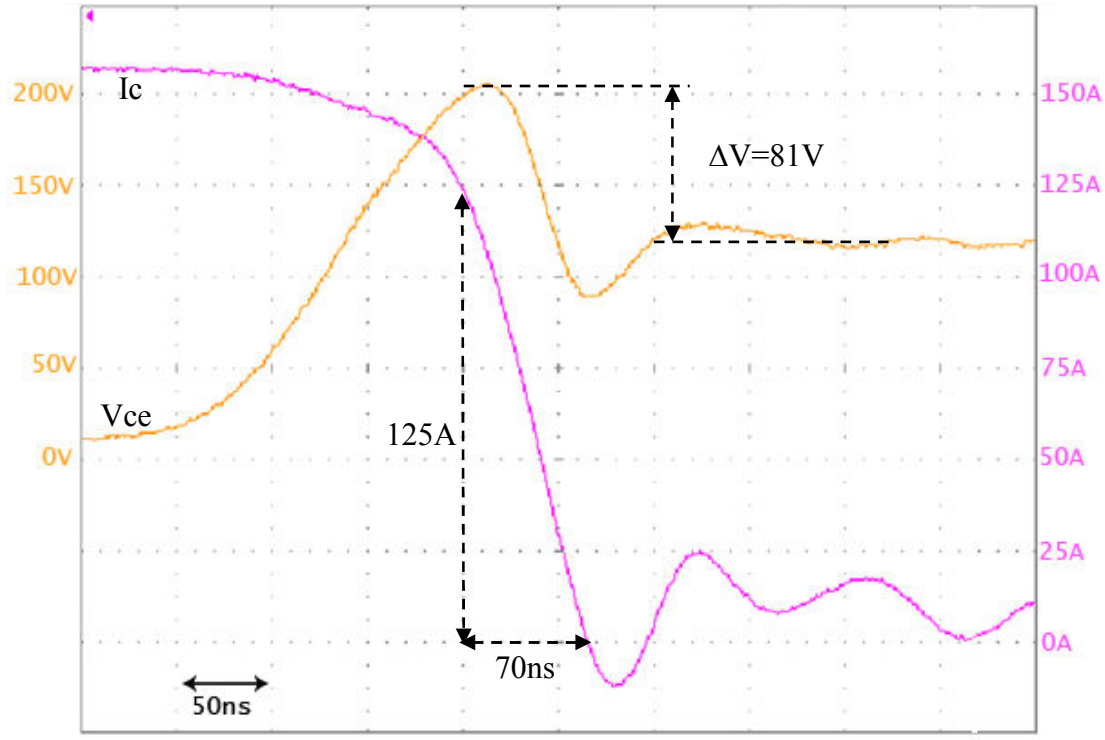

Figure 4.5 IGBT Turn-Off Graph, (I_c : pink, 25A/div), (V_{ce} : orange, 50V/div)

Table 4-2 Turn-Off Test Results

Parameter	**Value**
V_{peak}	206V
V_{DC}	125V
ΔV	81V
t_{fall}	70ns
di/dt (max)	125A/70ns=1,78A/ns
L_{Busbar}	81/1,78=45nH

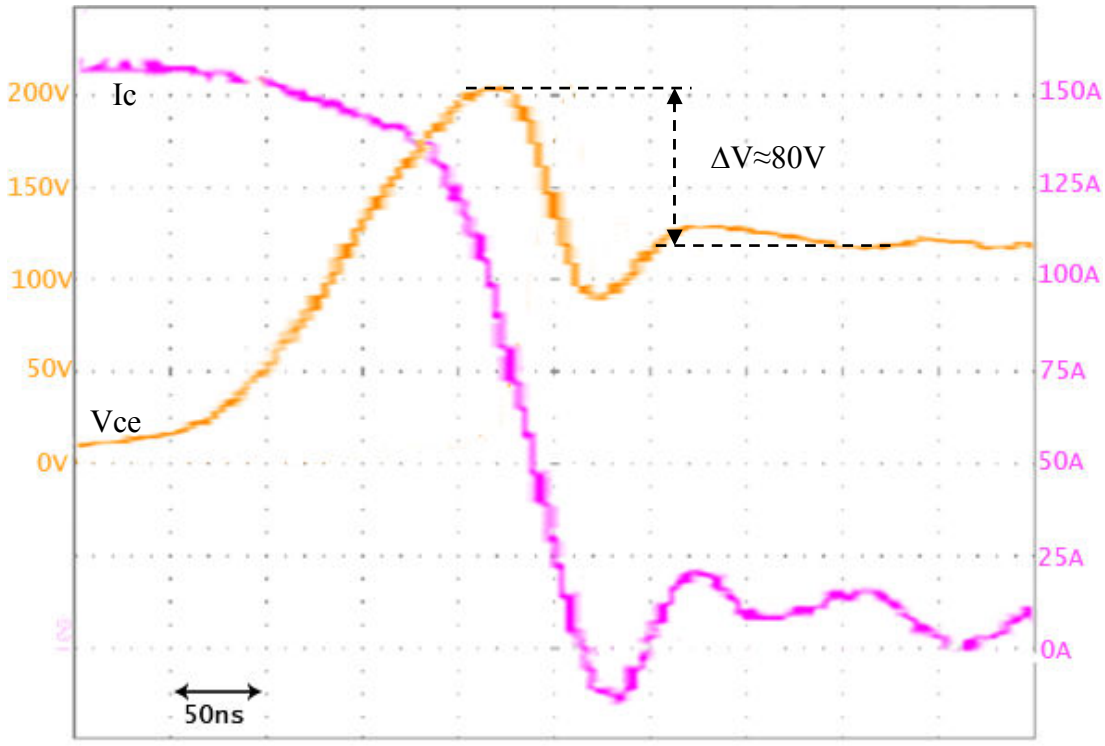

Figure 4.6 IGBT Turn-Off Graph with Snubber, (I_c : pink, 25A/div), (V_{ce} : orange, 50V/div)

Snubber is used to reduce the peak voltage when IGBT is turned off. For low voltage, and high current IPMs, snubber capacitor value should be 1µF per 100A [9]. 2×3µF 1000V KP-3C model snubber capacitors produced by Alcon are connected in parallel to the DC-Link. Waveforms in Figure 4.6 are obtained with snubber capacitors. Peak voltage level is 206V, which is the same as the snubberless operation value. Peak voltage level is not decreased because busbar inductance is already very low (45nH).

4.1.4. Cooling

4.1.4.1. Cooling Design

In order to cool IPMs, aluminum heatsink is used. Power losses are calculated with Melcosim program which is supplied by the manufacturer of the IPM. Power loss of PM400DSA60 IPM is 175W for 250Hz switching frequency, 140V bus voltage and 144A RMS current (Figure 4.7).

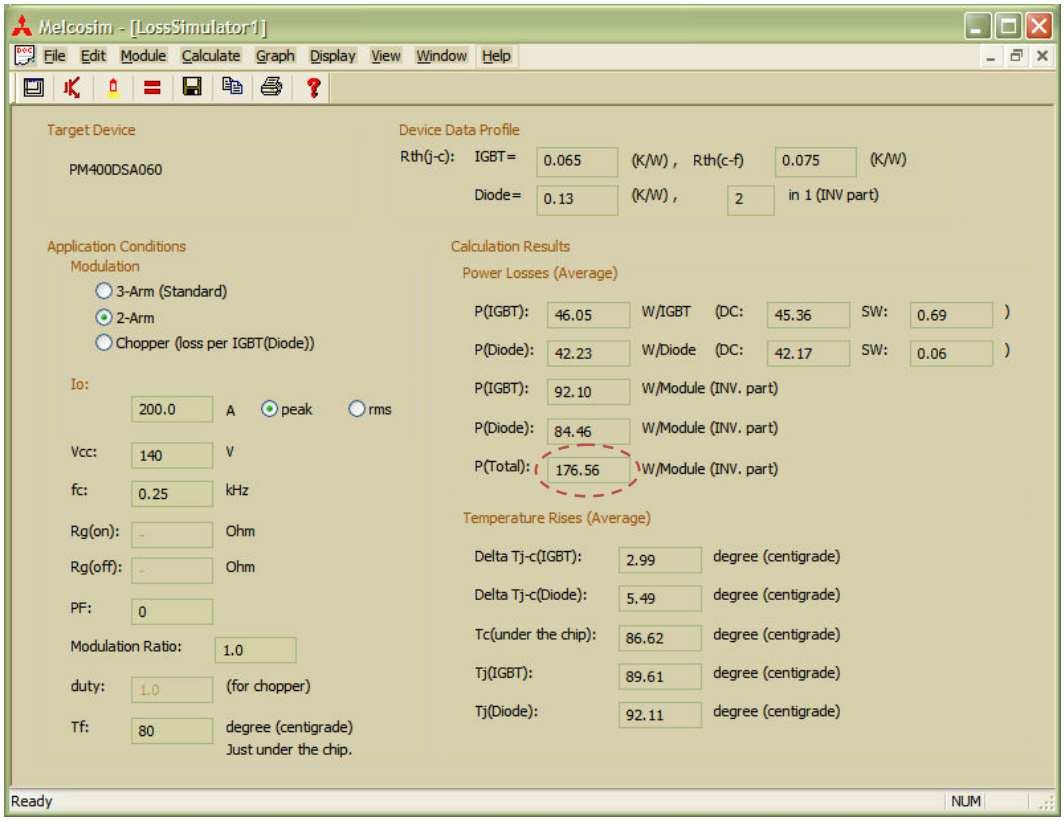

Figure 4.7 Losses for PM400DSA60 IPM

Since there will be two IPMs on the heatsink, cooling power should be 350W. Maximum junction temperature is 125°C. In order to be on safe side, 85°C maximum heatsink temperature is selected. If $T_{ambient}$ is assumed to be 45°C, then maximum heatsink thermal resistance can be calculated as;

$$R_{heat\sin k-air} = \frac{T_{heat\sin k} - T_{ambient}}{P_{\max}} = \frac{85-45}{350} = 0.114C°/W \tag{4.2}$$

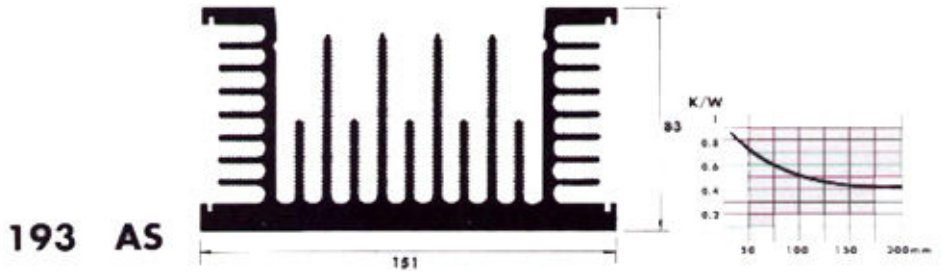

Figure 4.8 Heatsink Cross Section

193 AS model heatsink is selected for easy installation (Figure 4.8). For 300mm heatsink, thermal resistance is found as 0.4C°/W from the graph. The resistance value is for natural air convection.

2 fans are fixed to the heatsink. Fans are 80mm×80mm, 12V, 3200 rpm, 40CFM (Appendix-B). Because of static pressure, air flow is expected to decrease to 35CFM. Total air flow with two fans is 70CFM (33000 cm^3/sec). Air velocity can be calculated as:

$$v = \frac{33000cm^3/s}{80cm^2} = 412cm/s = 4.12m/s \tag{4.3}$$

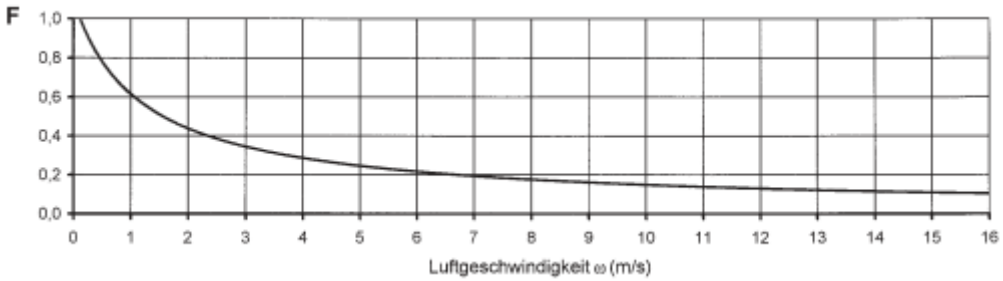

Figure 4.9 Thermal Resistance Multiplier vs Air Velocity

With forced air cooling, thermal resistance decreases to 27% for air velocity of 4.12m/s. Thermal resistance with forced air cooling is:

$$R_{heatsink\text{-}ambient,forced}=0.4\times0.27=0.108C°/W \quad (4.4)$$

This value is below the maximum acceptable thermal resistance (0.114C°/W).

4.1.4.2. Verification of Cooling Design

DC-Link of the H-Bridge module is charged to 140VDC via 100VAC supply and diode bridge rectifier (Figure 4.10, Figure 4.11). In order to simulate the thermal conditions at maximum power (Q=100kVar, I=144A), R & L values are adjusted.

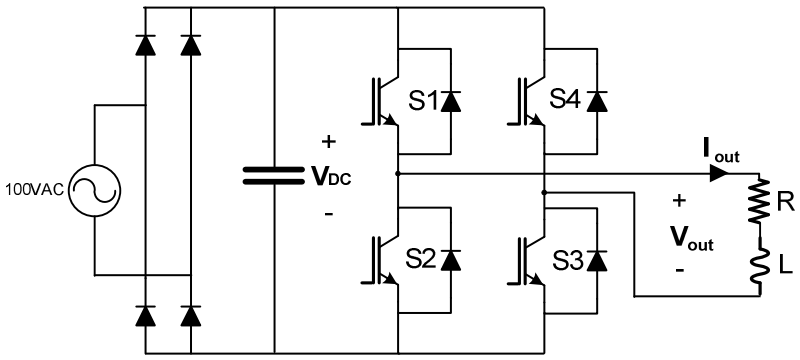

Figure 4.10 Cooling Test Circuit

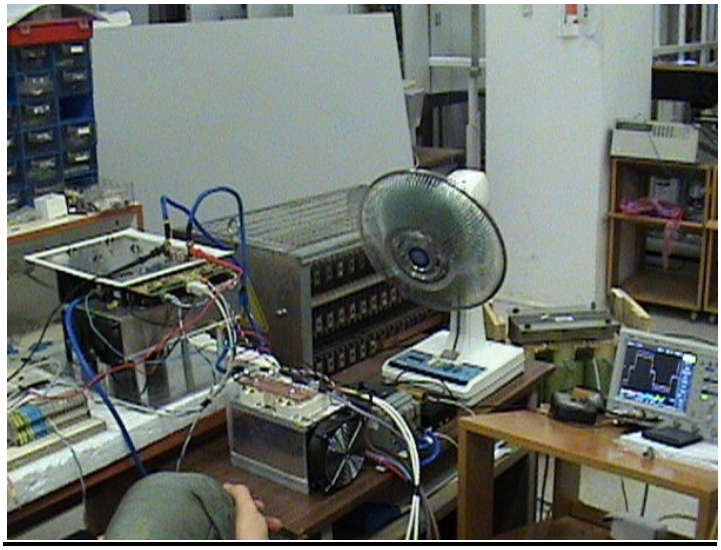

Figure 4.11 Thermal Test Setup

A quasi-square wave at expected switching frequency (250Hz) is generated with the H-Bridge and applied to the load (Figure 4.12).

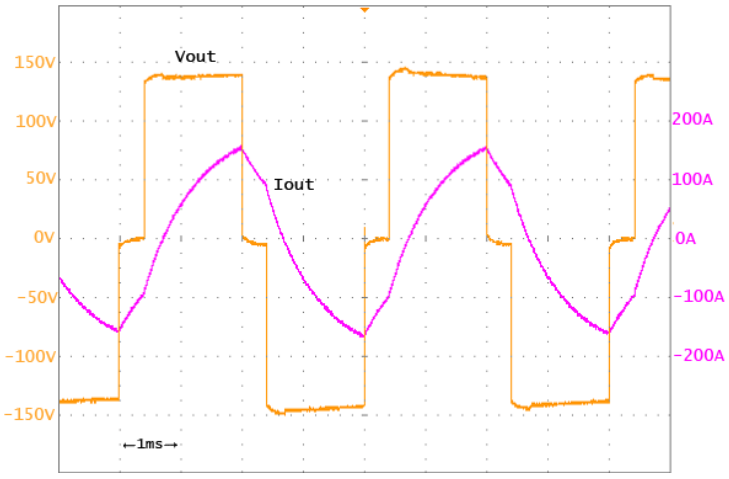

Figure 4.12 H-Bridge Module Output Voltage and Current for Thermal Test

Temperature of the heatsink is measured and recorded in 1 second intervals and the graph in Figure 4.13 is obtained. Fan speed is adjusted to maximum during the test. Ambient temperature is measured as 25 °C. From the graph, steady state heatsink temperature is found to be 55 °C. Then, temperature difference between heatsink and ambient is 30°C. At design stage, $T_{ambient}$ = 45°C and $T_{heatsink}$ =85°C are selected. Expected temperature difference between heatsink and ambient was 40°C, and during tests, 30°C is obtained. Heatsink cooling performance is %25 better than expected. Consequently, heatsink design is verified.

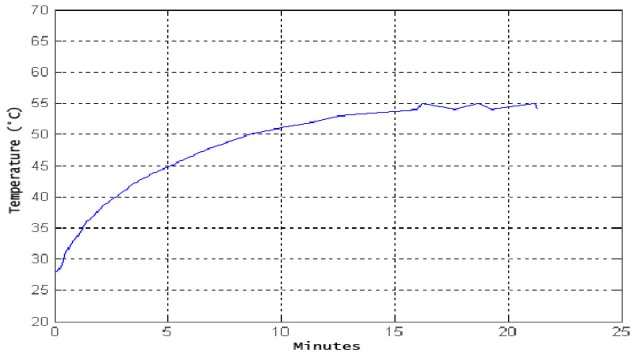

Figure 4.13 Temperature Variation at Full Load Current and Full Fan Speed

4.1.5. IPM Interface Card

In order to supply IPMs and interface the IPMs with controller, IPM Interface Card is designed. Transformer output voltage is rectified with diodes and regulated with a linear regulator (Figure 4.14). Regulated voltage is supplied to IPMs.

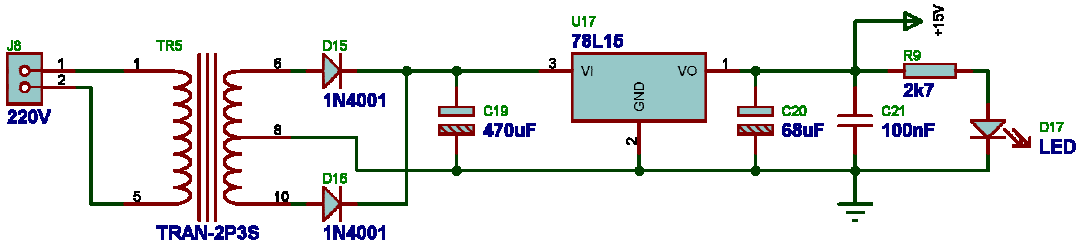

Figure 4.14 IPM Supply Stage

Optocouplers are used to interface and isolate drive and fault signals between converter side and control side (Figure 4.15).

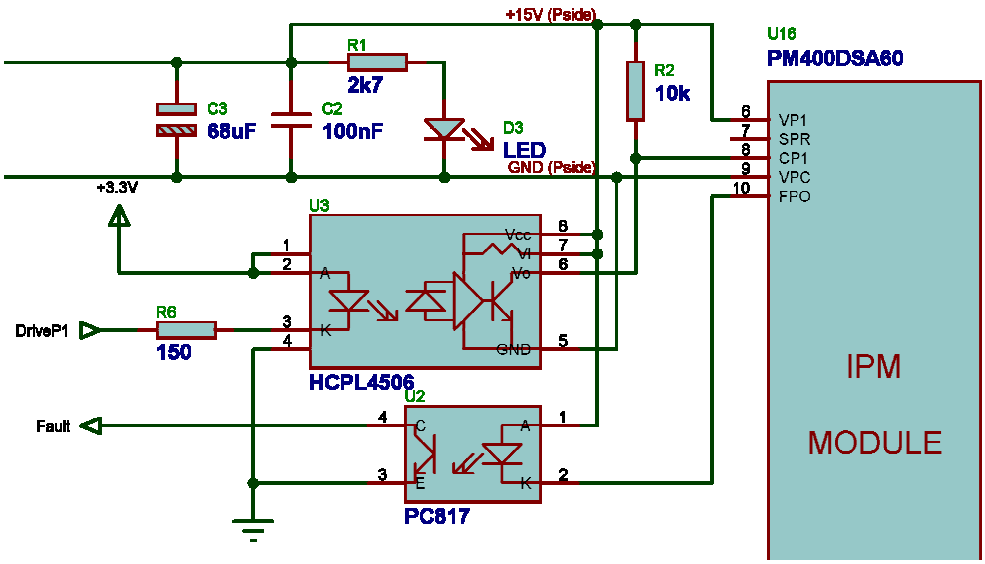

Figure 4.15 Optocoupler Isolation

Also there is a microcontroller on the PCB which measures the heatsink temperature with NTC and adjusts the speed of the fans by PWM method (Figure 4.16). If temperature of the heatsink exceeds critical level, then fault signal is generated.

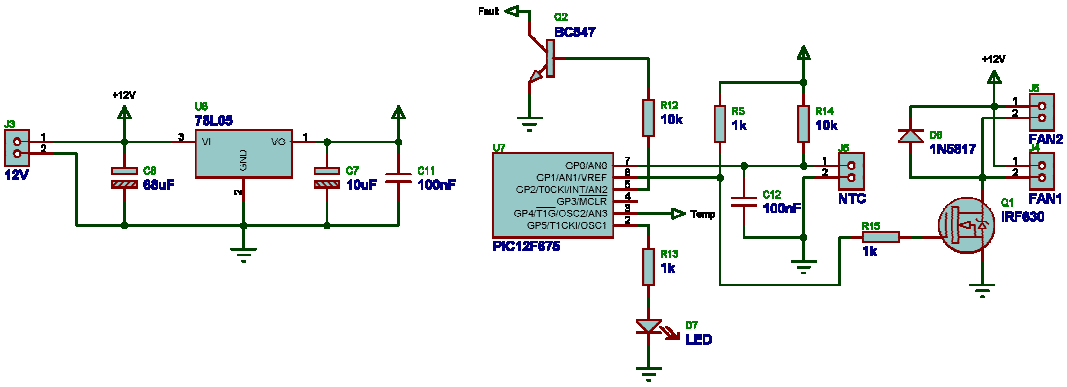

Figure 4.16 Fan Speed Control Circuit

Overall IPM Interface Card circuitry is presented in Figure 4.17. Printed circuit board and final circuit card are in Figure 4.18.

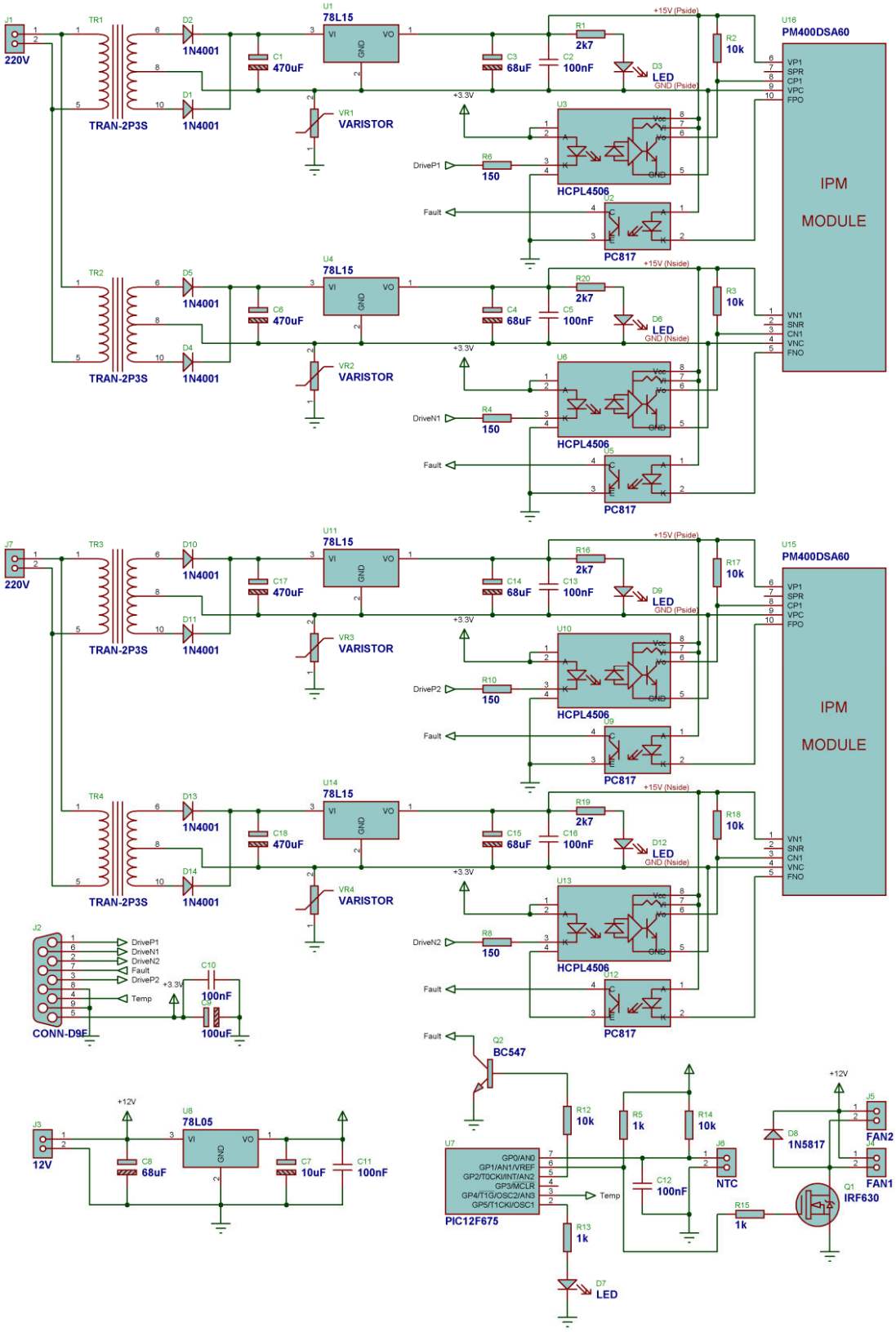

Figure 4.17 IPMs, IPM Supply, Interface Circuitry and Fan Control Circuit

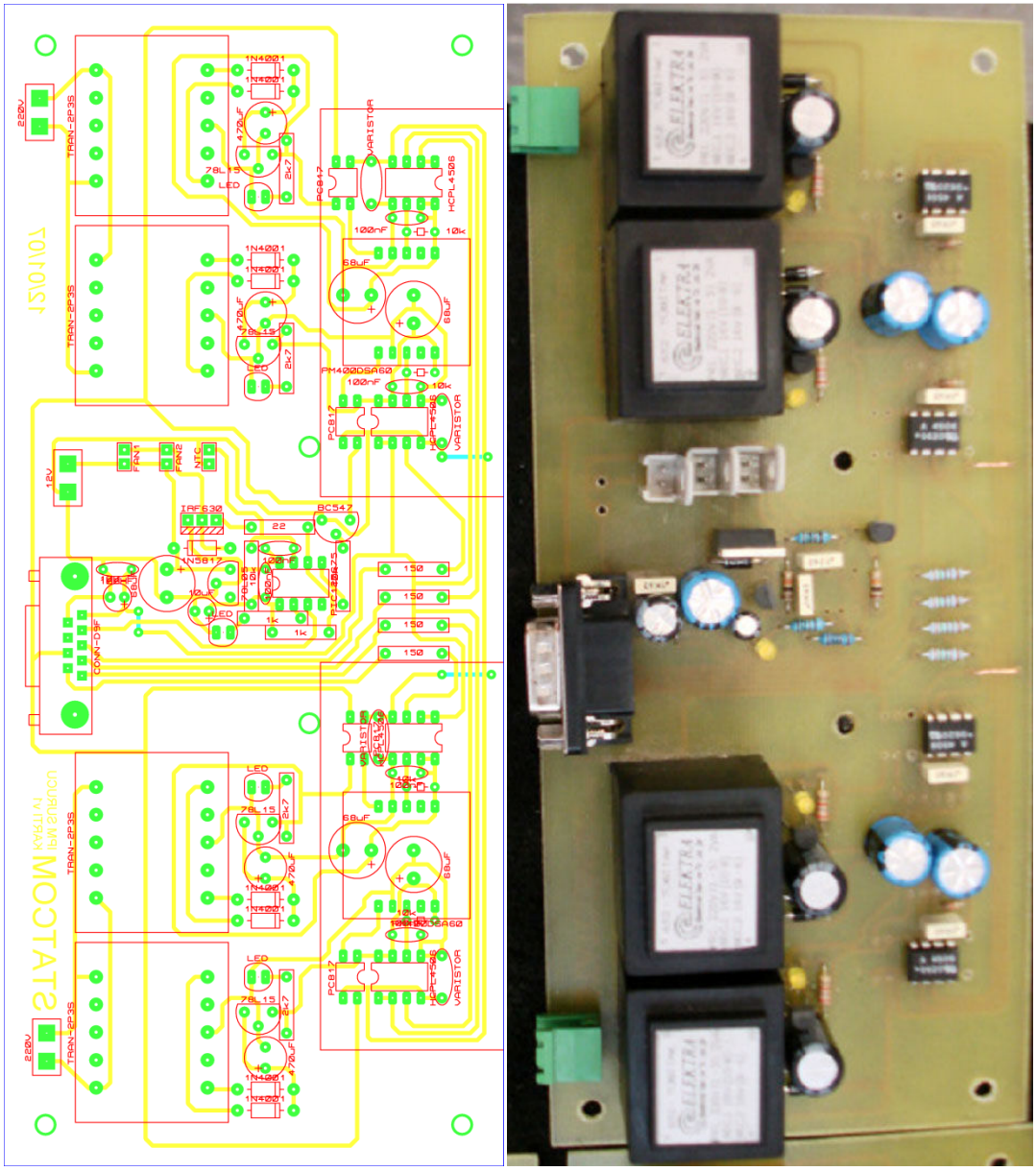

Figure 4.18 IPM Interface Card

Finally, the power and interface circuit are integrated to obtain the final H-Bridge module, as illustrated in Figure 4.19. The corresponding implemented circuit is given in Figure 4.20.

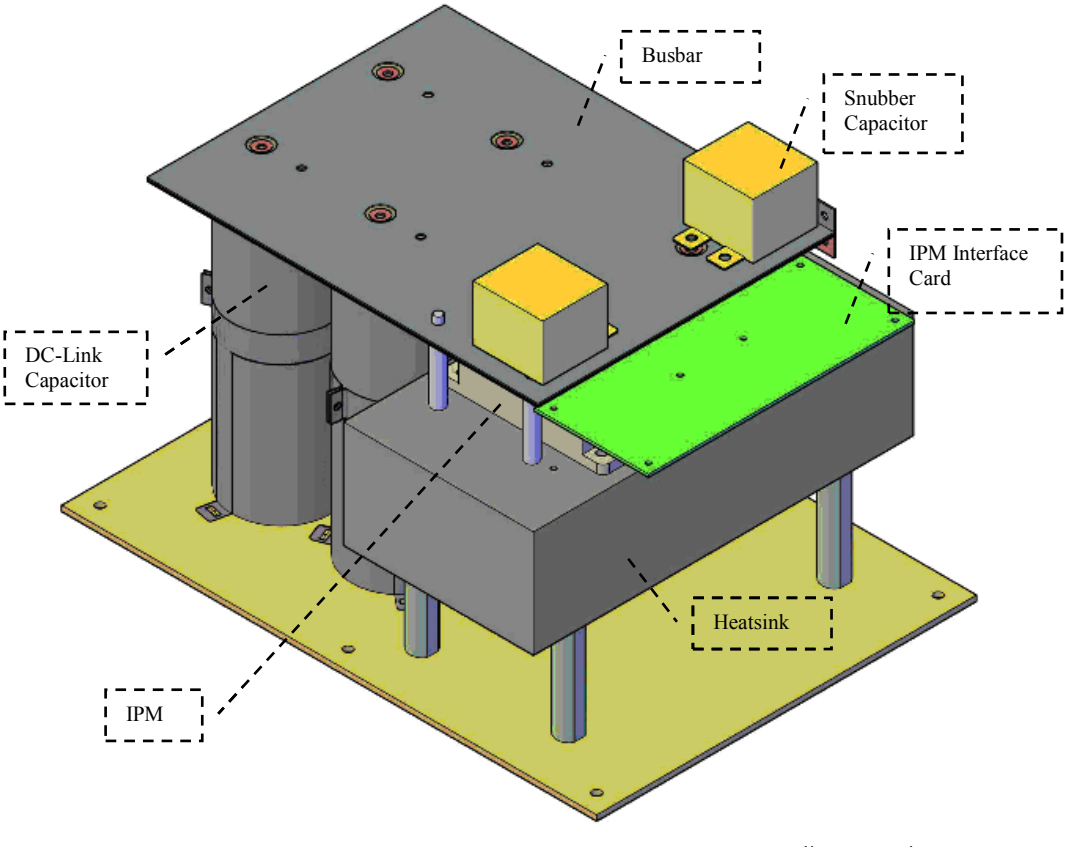

Figure 4.19 H-Bridge 3D Drawing

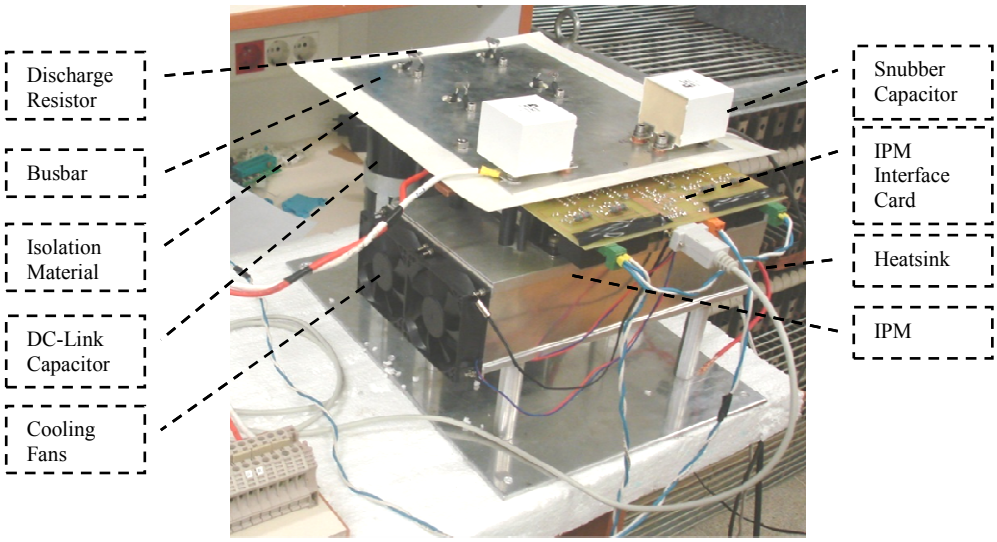

Figure 4.20 Produced H-Bridge

4.2. Controller Design

4.2.1. FPGA Stage

FPGA (Field Programmable Gate Array) is used to control the switches. There are 36 switches in the converter. Every switch has a custom control signal in μs resolution. DSP or microcontroller based controllers cannot handle that much operation precisely. Therefore parallel computing is required. FPGA;

- Communicates with DSP over SPI protocol and receives modulation index, shifting angle, PLL and capacitor voltage data, sends error data,
- Stores switching angle data corresponding to modulation index values,
- Generates firing pulses by considering PLL, switching angles, shifting angles, capacitor voltages and deadband,
- Stops switching if any IPM generates error signal.

Software flow diagram can be seen in Figure 4.21. FPGA board is given in Figure 4.23, where each DB-9 connector carries signals between FPGA and H-Bridges.

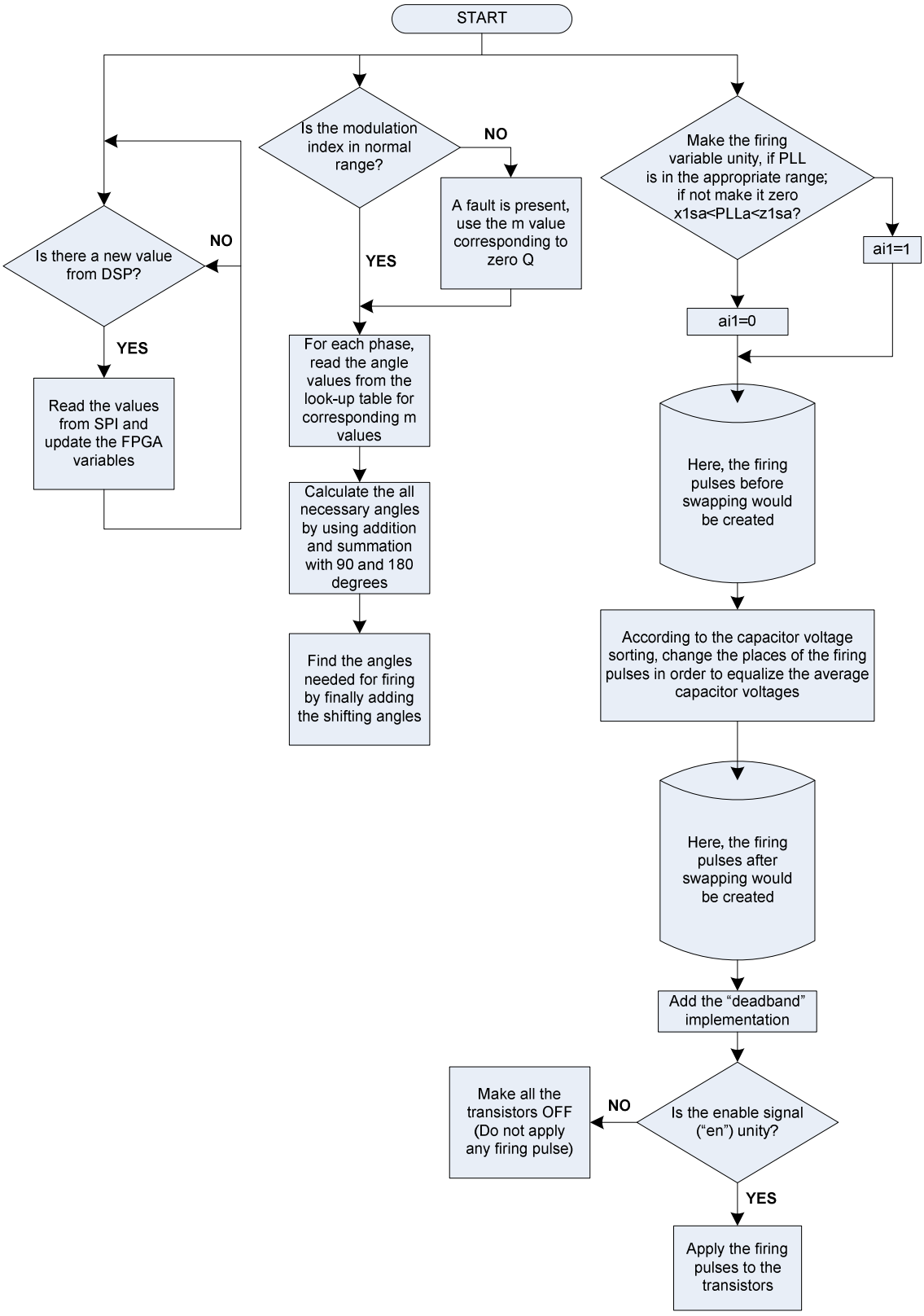

Figure 4.21 FPGA Software Flow Diagram

In Figure 4.22, generated firing pulses for all the transistors are available. In the figure, “a11” means 1st transistor of a1 H-Bridge module (there are 9 H-Bridge modules).

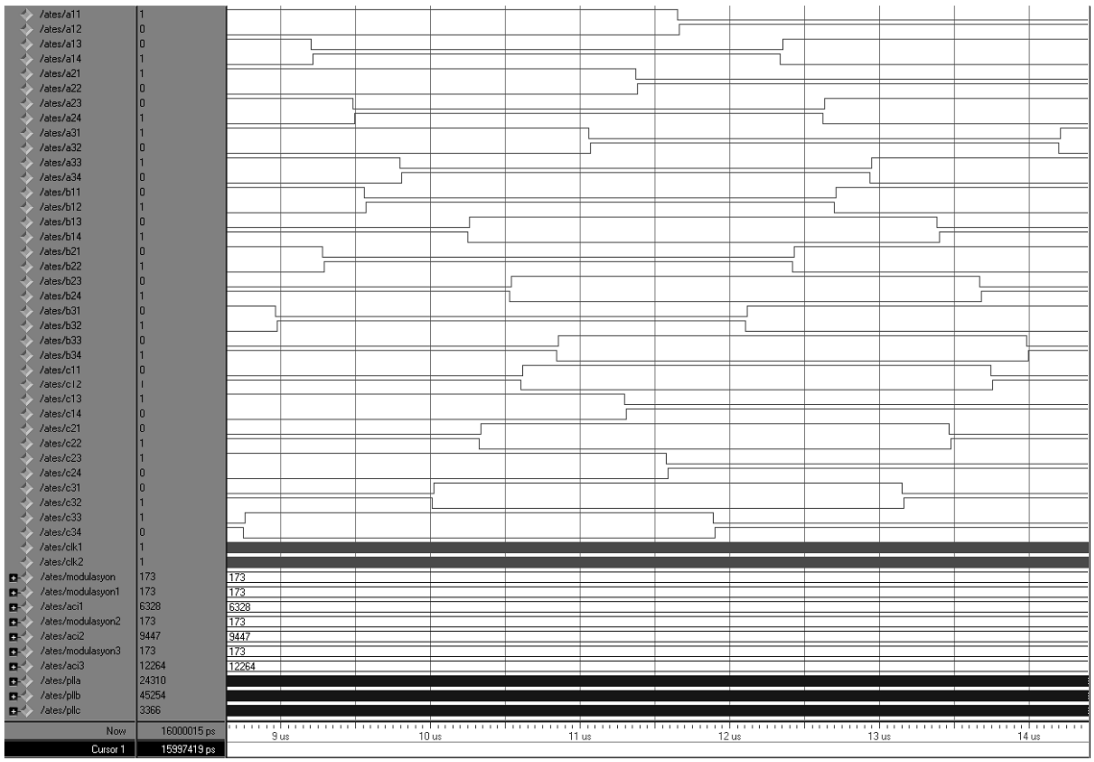

Figure 4.22 Sample Switching Signals for all Switches

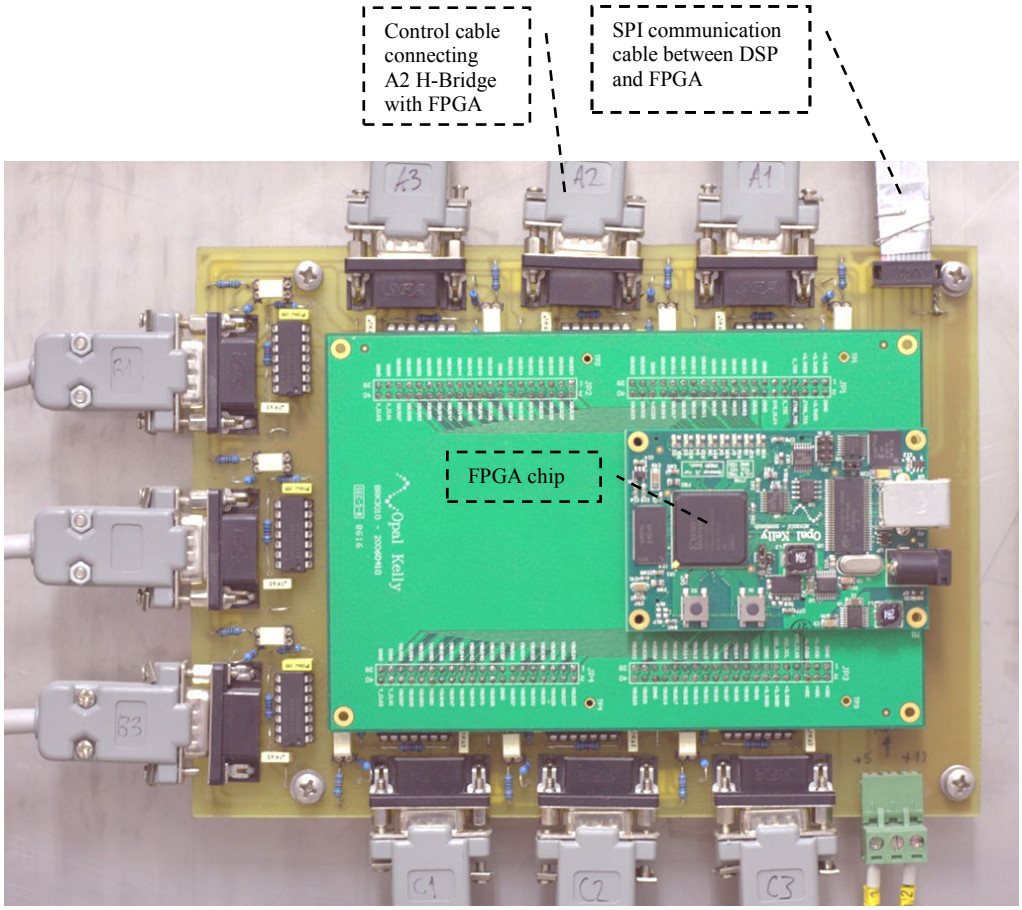

Figure 4.23 FPGA Board

4.2.2. DSP Stage

A DSP Stage, which is designed previously for the National Power Quality Project is used. DSP;

- Generates PLL signals, and sends to FPGA over SPI Communication Link,
- Measures line currents and controls the amount of reactive power injected,
- Converts capacitors voltages to digital and sends them to FPGA,
- In case of a fault, disconnects the converter from utility via a contactor,
- Controls contactor and relays.

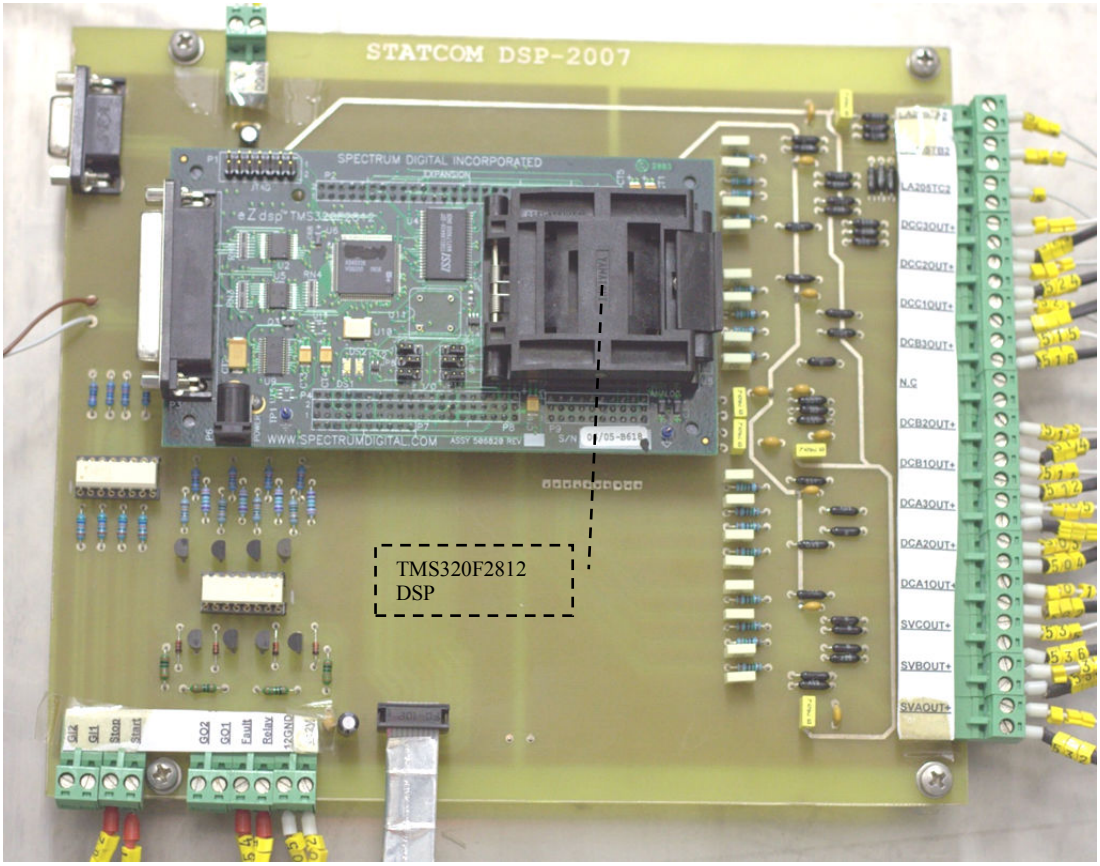

Figure 4.24 DSP Board

4.3. Auxiliary Components

4.3.1. Coupling Inductor

The inverter can generate low harmonic voltage waveforms in a specified modulation index range. Let V_{max} be the maximum inverter voltage and V_{min} is the minimum inverter voltage for low harmonic operation. Then,

$$(V_{max} - V_{min})/X_L = 2I_{max} \quad (4.5)$$

I_{max} is 144A, V_{max} - V_{min} is around 150V, then coupling inductance can be found as 1,6mH. The photograph of implemented coupling inductor is given in Figure 4.25.

Figure 4.25 Coupling Inductor

4.3.2. Circuit Breaker

In order to prevent excessive currents at fault conditions, a 400V 160A circuit breaker (Figure 4.26) is installed to system at the source side.

Figure 4.26 Circuit Breaker

4.3.3. Precharge Resistors

Precharge resistors are needed to limit the precharge current. Three 330Ω 100W resistors (Figure 4.27) (1 resistor for each phase) are taken into conduction while charging the capacitors.

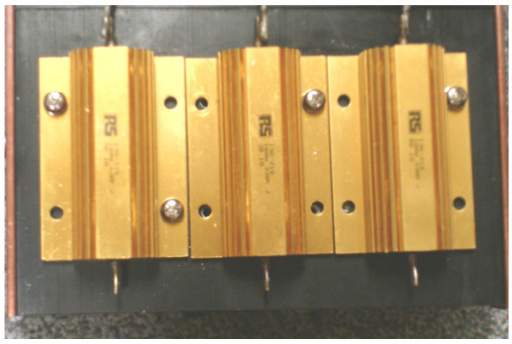

Figure 4.27 Precharge Resistors fixed to Heatsink

4.3.4. Bypass Contactor

When precharge is over, a 400V 185A contactor (Figure 4.28) bypasses the precharge resistors, and the STATCOM begins to inject reactive power to the grid.

Figure 4.28 Contactor

4.3.5. Voltage and Current Sensors

Hall Effect voltage sensors (LV25-P) are used to measure capacitor voltages. Therefore electrical isolation between the converter and the control stages is maintained. In Figure 4.29 sensors and voltage division resistors are mounted on the PCB.

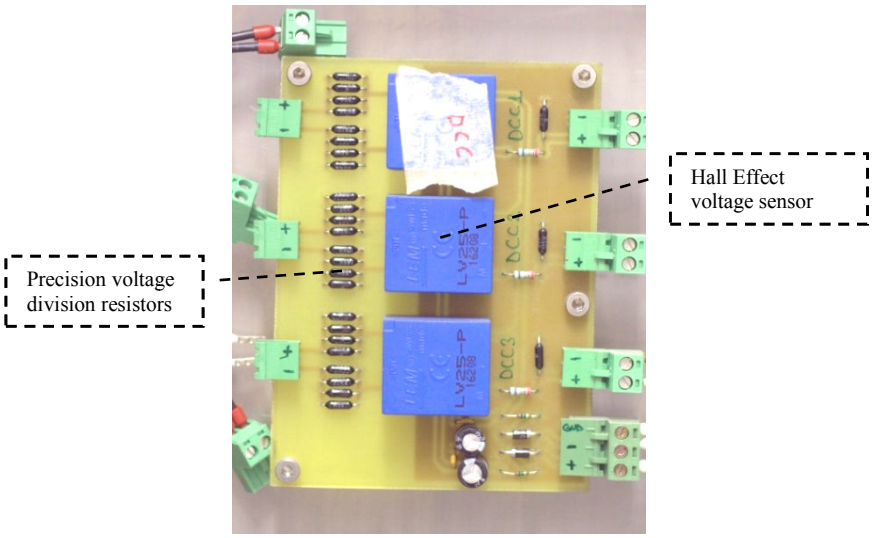

Figure 4.29 Hall Effect Voltage Sensors on PCB

Line currents are measured by Hall Effect current sensors (Figure 4.30).

Figure 4.30 Hall Effect Current Sensor (LA 205-T)

4.3.6. Voltage Transformer

Source voltage should be measured to generate PLL signals. Voltage transformers are used for this purpose (Figure 4.31).

Figure 4.31 0.5P Class Voltage Transformer

4.4. Enclosure Works

Power stage and controller stage are installed in a 120×200×60cm (w×h×d) enclosure as shown in Figure 4.32 and Figure 4.33.

Figure 4.32 Side View of Enclosure, CMI Converter Stage and Control Stage

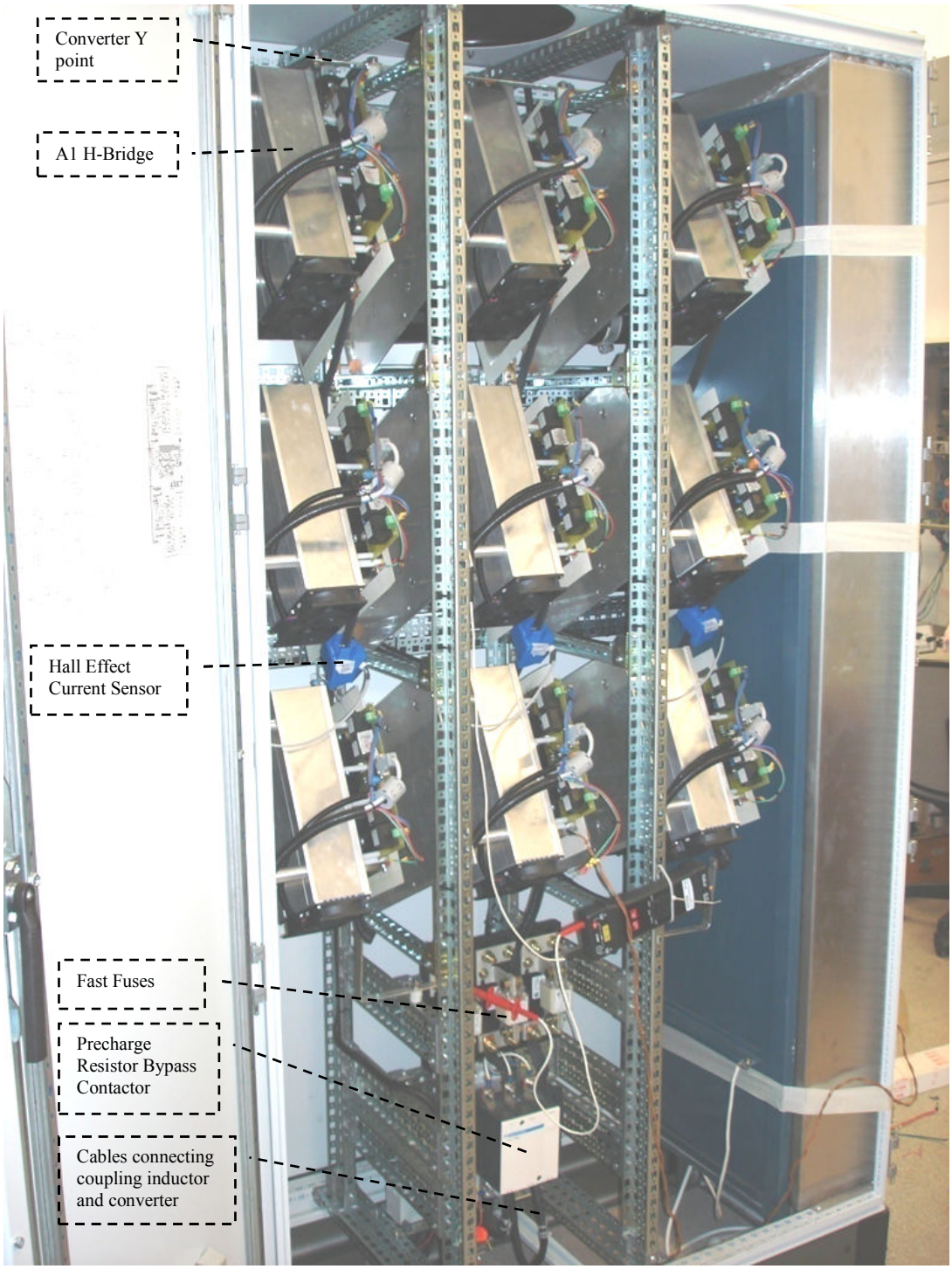

Figure 4.33 Front View of Enclosure, ±100kVAr CMI Converter Stage

CHAPTER 5

EXPERIMENTAL RESULTS

Experimental tests are carried out on the developed prototype system, to assess the performance of the CMI based STATCOM.

5.1 DC Capacitor Voltages

To verify the success of the proposed capacitor voltage balancing method, voltages of three capacitors at the same phase are measured for different reactive powers. It is apparently seen from Figure 5.1 through Figure 5.7 that the method is successful. Spikes on the voltage waveforms are due to noise coupled to the voltage probes. The DC-Link capacitors' voltage ripple remains within a 14% band as seen from table Table 5-1. In table Table 5-1, positive reactive power corresponds to inductive mode STATCOM operation, negative reactive power corresponds to capacitive mode STATCOM operation.

Table 5-1 DC-Link Capacitor Voltage Ripple for Various Reactive Powers

Power Level (kVAr)	Peak-to-Peak Voltage Ripple, %
99	6
66	4
33	3
0	0
-33	4
-66	10
-99	14

As STATCOM reactive power becomes capacitive, the CMI output voltage increases and $+3V_{dc}$ region becomes wider (Figure 5.43). At $+3V_{dc}$ level, all of the three H-Bridges in a phase should be taken into conduction, and no selective swapping can be applied. Therefore the capacitor voltages diverge and the voltage ripple increases.

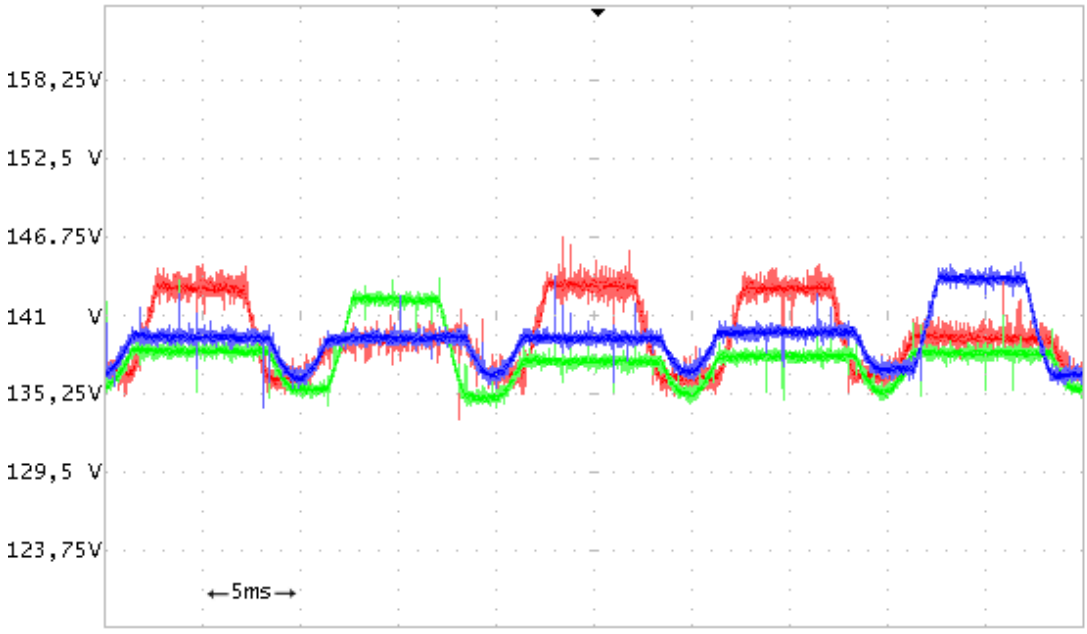

Figure 5.1 Capacitor Voltages of one phase at 99kVAr Inductive Reactive Power, 5.75V/div, +141V DC offset

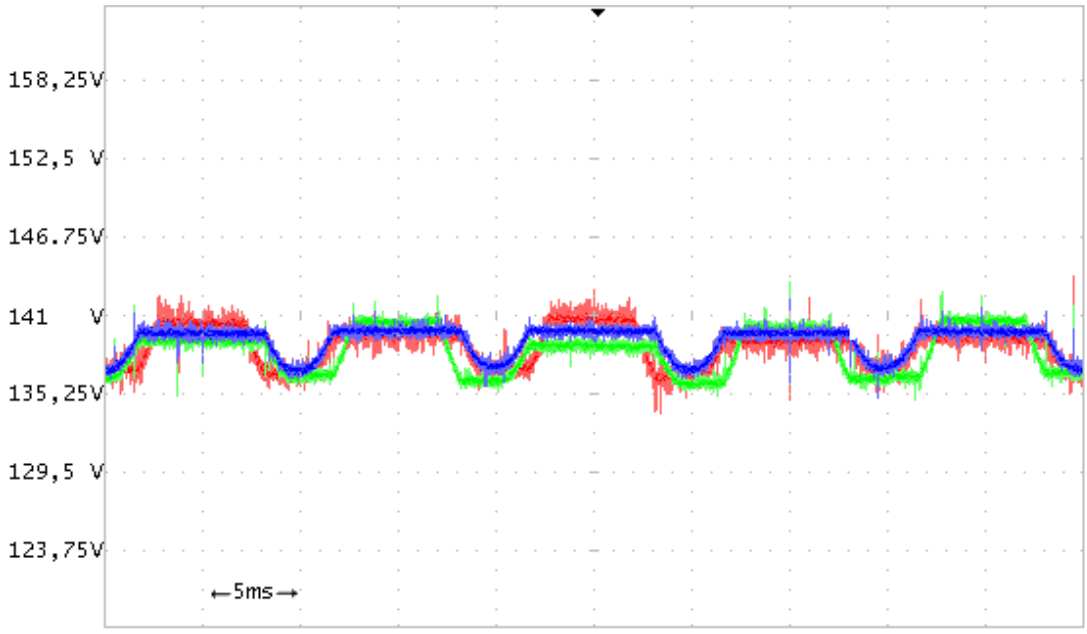

Figure 5.2 Capacitor Voltages of one phase at 66kVAr Inductive Reactive Power, 5.75V/div, +141V DC offset

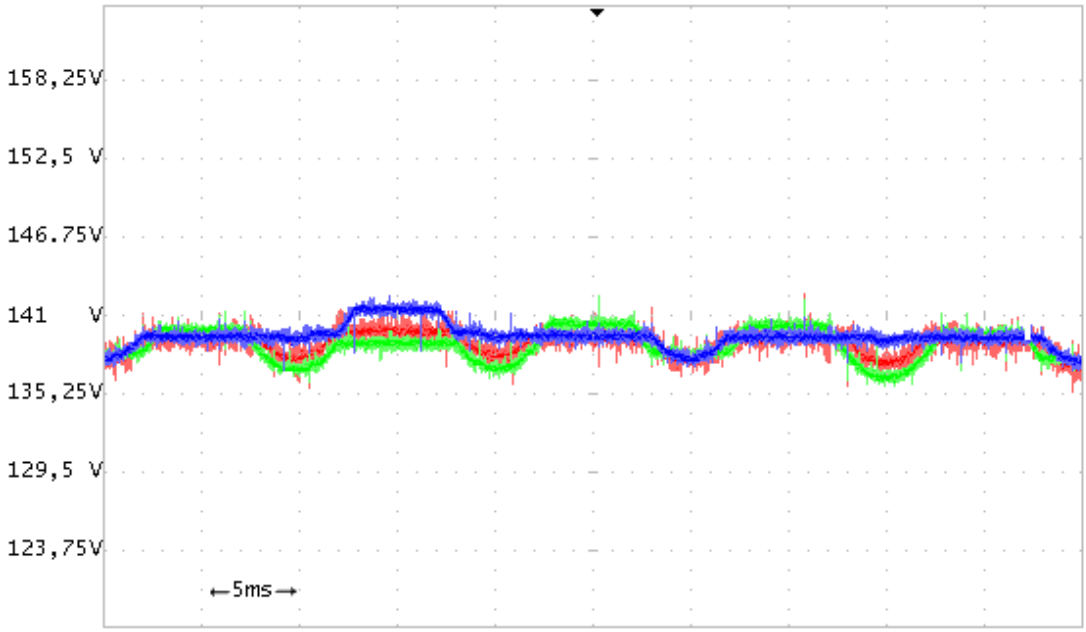

Figure 5.3 Capacitor Voltages of one phase at 33kVAr Inductive Reactive Power, 5.75V/div, +141V DC offset

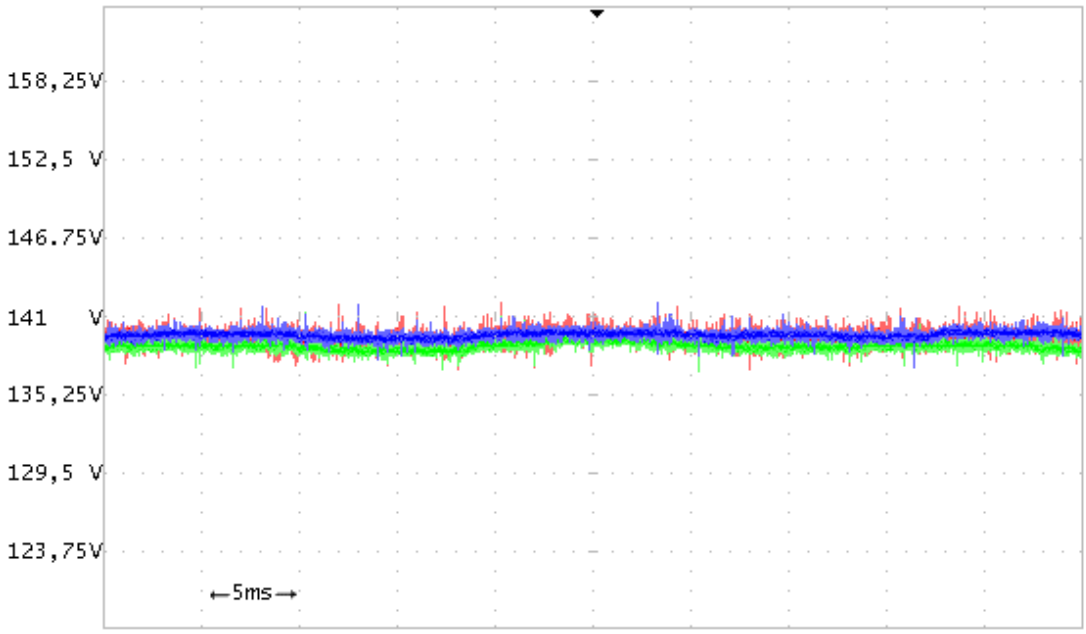

Figure 5.4 Capacitor Voltages of one phase at 0VAr Reactive Power, 5.75V/div, +141V DC offset

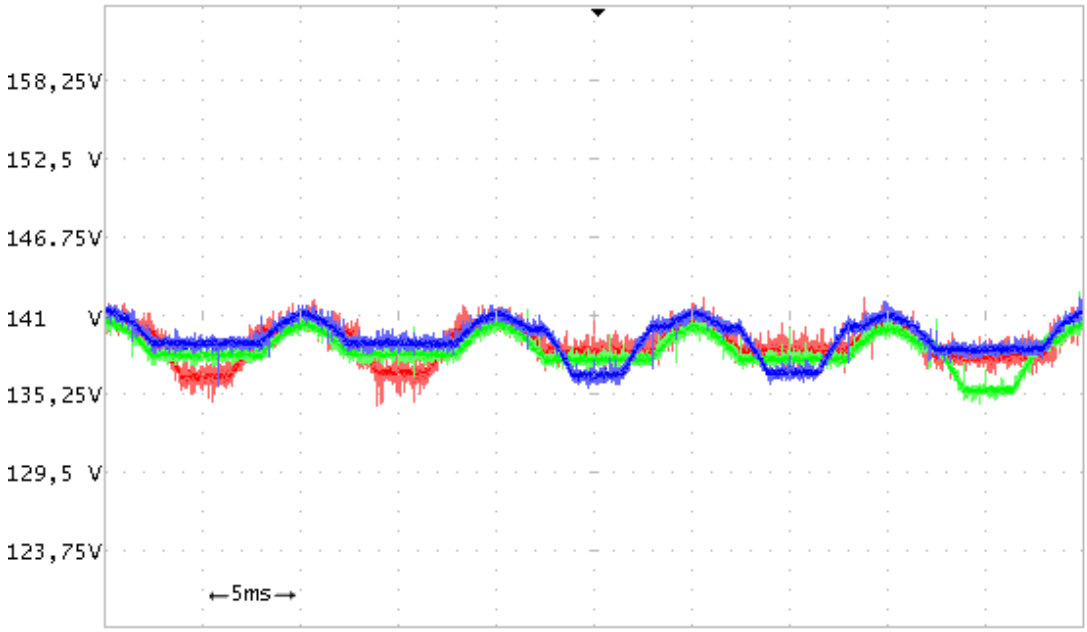

Figure 5.5 Capacitor Voltages of one phase at 33kVAr Capacitive Reactive Power, 5.75V/div, +141V DC offset

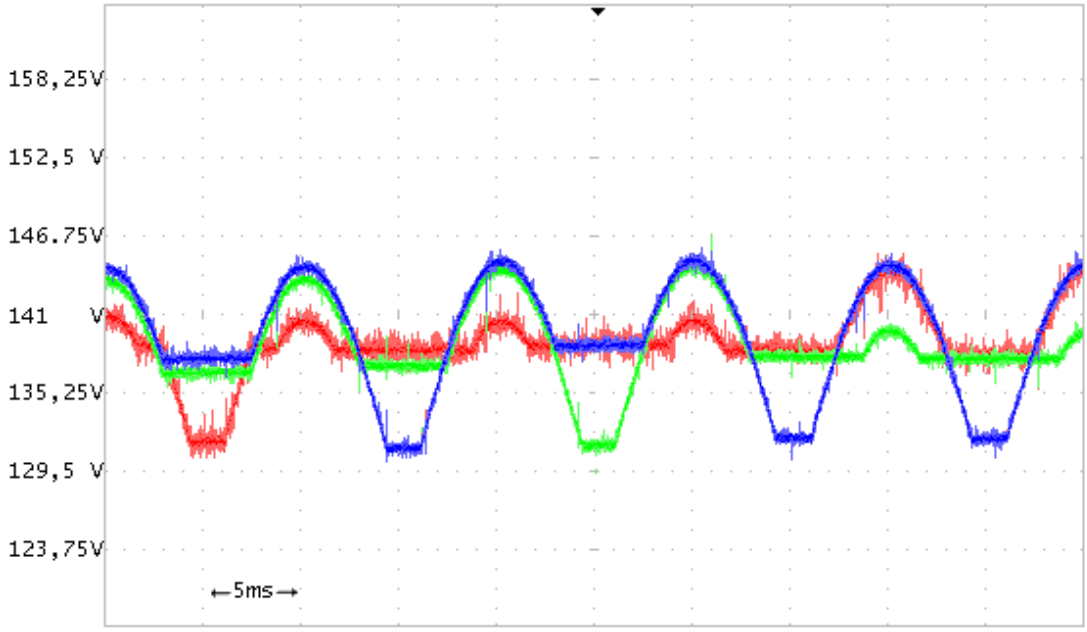

Figure 5.6 Capacitor Voltages of one phase at 66kVAr Capacitive Reactive Power, 5.75V/div, +141V DC offset

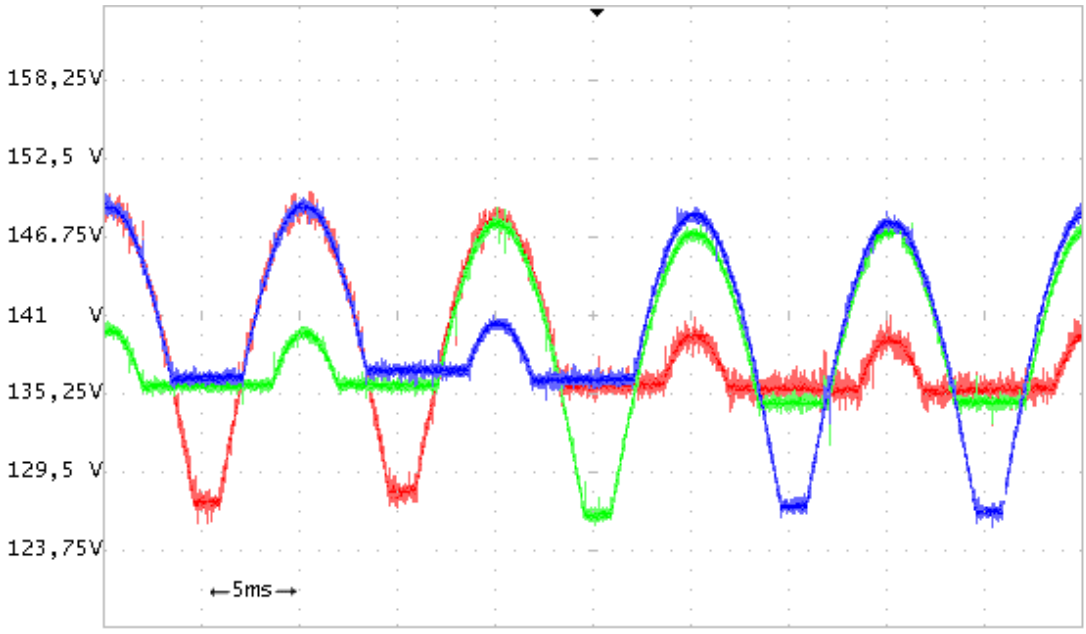

Figure 5.7 Capacitor Voltages of one phase at 99kVAr Capacitive Reactive Power, 5.75V/div, +141V DC offset

5.2 Line to Line Voltage Waveforms and Harmonics

Line to line converter output voltages and their harmonic contents are given in Figure 5.8 to Figure 5.21.

There are voltage spikes at transitions from one level to another. When changing the voltage level, a transistor in a leg of H-Bridge is turned off, and a time period equal to deadband passes before turning on the other transistor in the leg. During deadband time (5μs), both transistors are switched off, therefore current flows from one of the diodes in the leg. Thus, the H-Bridge generates unexpected voltage during deadband time.

Since each phase has three H-Bridges, two harmonics can be eliminated [3]. 3rd harmonic voltage is not present in such a balanced 3-phase system due to the neutral wire being absent. Therefore 5^{th} and 7^{th} harmonics are eliminated with the switching angles. Inverter is expected to generate harmonics of 11^{th}, 13^{th}, 17^{th}, 19^{th}... Results obtained from Figure 5.8 to Figure 5.21 are quite consistent with the expectation.

As a further observation, due to the changing modulation index value with reactive power level, harmonic content of line to line voltage waveforms varies to a certain extent for different reactive power levels. Since switching angles are generated by genetic algorithms, each modulation index value can have different harmonics as expected.

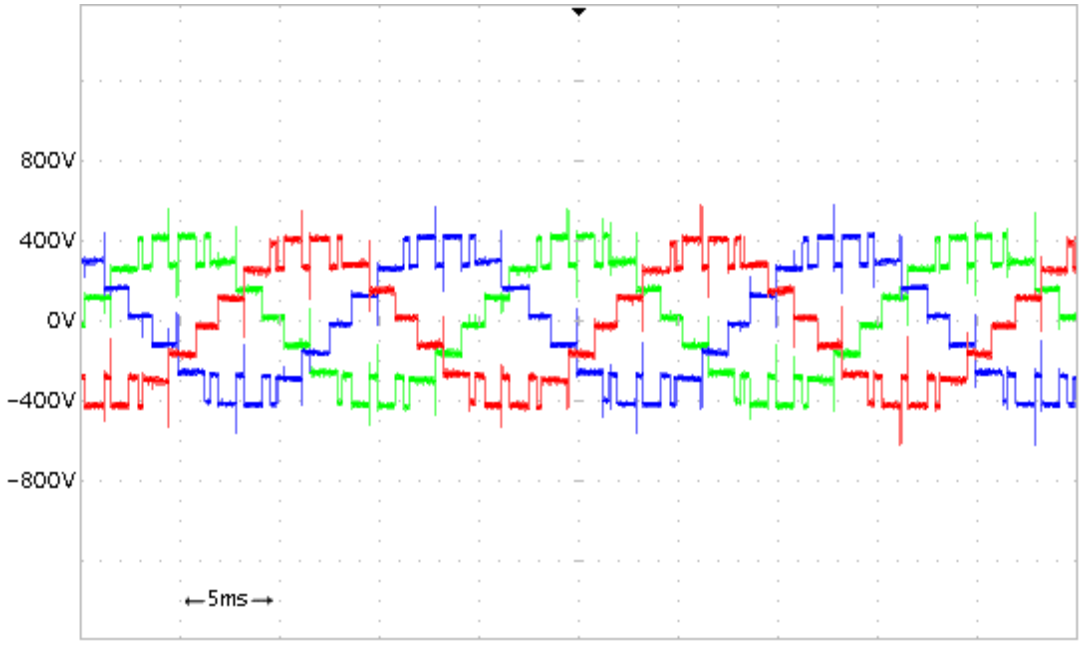

Figure 5.8 Line to Line Voltages at 99kVAr Inductive Reactive Power, 400V/div

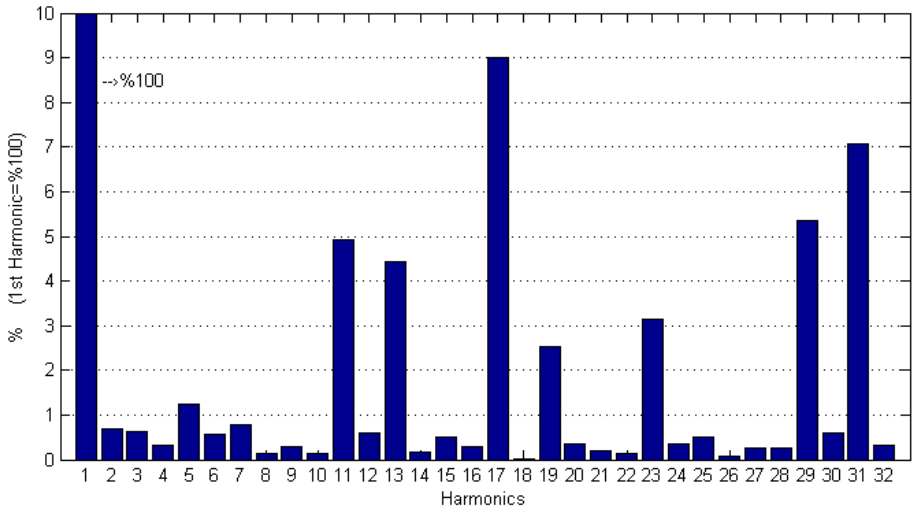

Figure 5.9 Line to Line Voltage Harmonics at 99kVAr Inductive Reactive Power

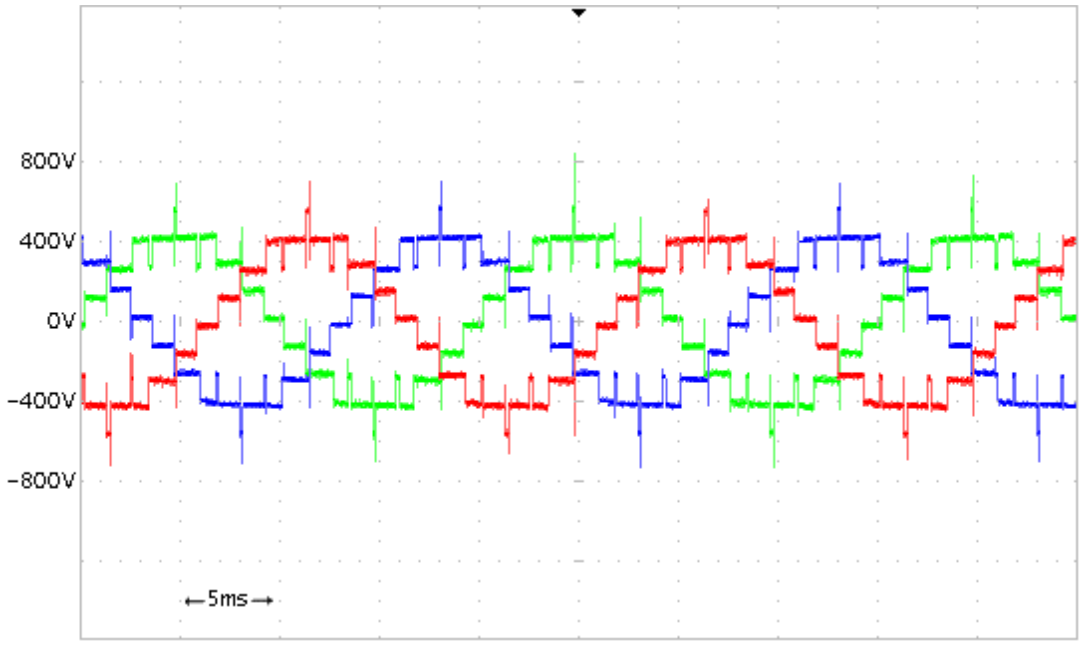

Figure 5.10 Line to Line Voltages at 66kVAr Inductive Reactive Power, 400V/div

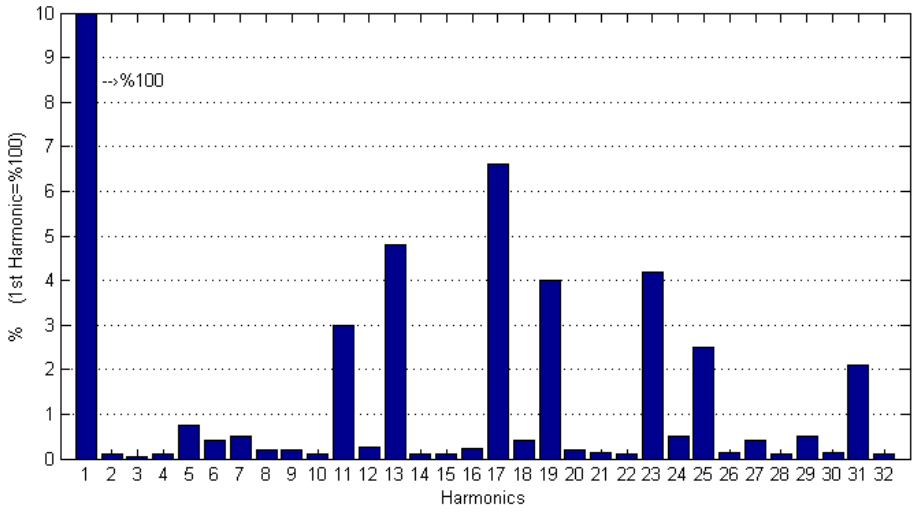

Figure 5.11 Line to Line Voltage Harmonics at 66kVAr Inductive Reactive Power

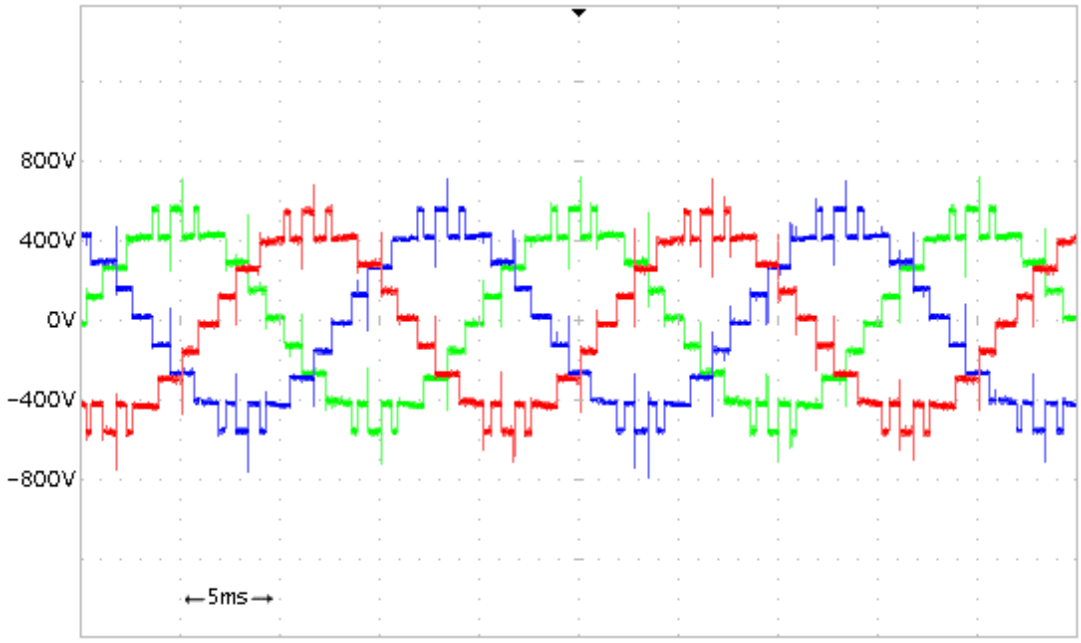

Figure 5.12 Line to Line Voltages at 33kVAr Inductive Reactive Power, 400V/div

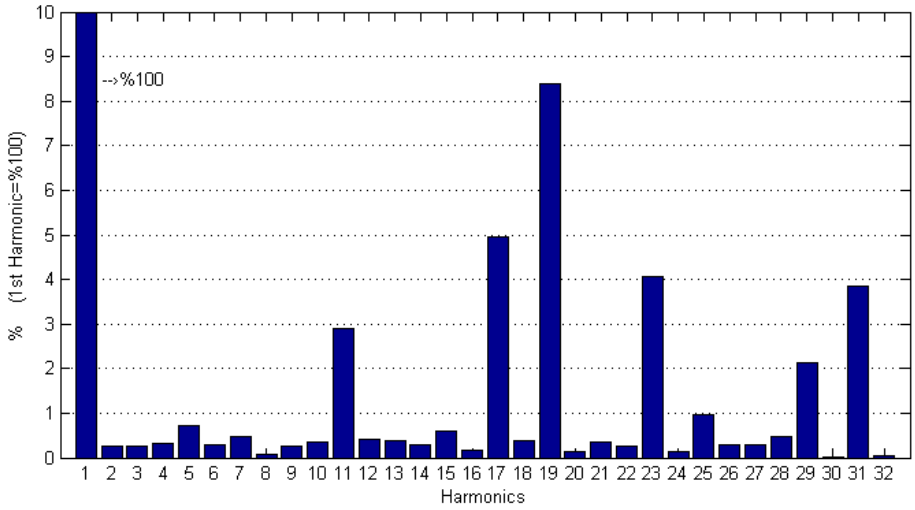

Figure 5.13 Line to Line Voltage Harmonics at 33kVAr Inductive Reactive Power

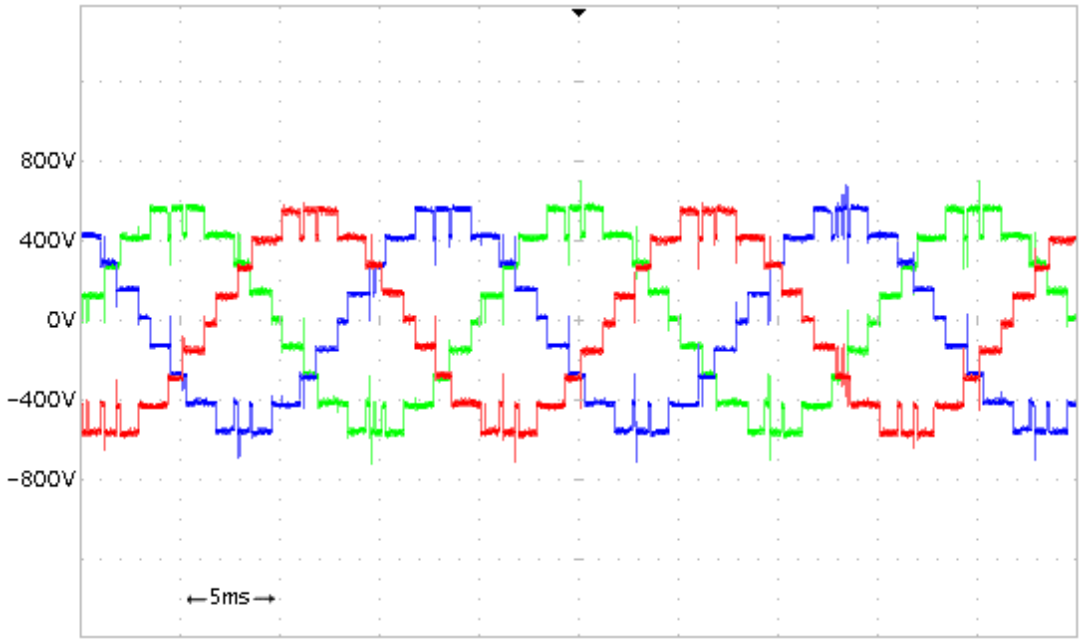

Figure 5.14 Line to Line Voltages at 0VAr Reactive Power, 400V/div

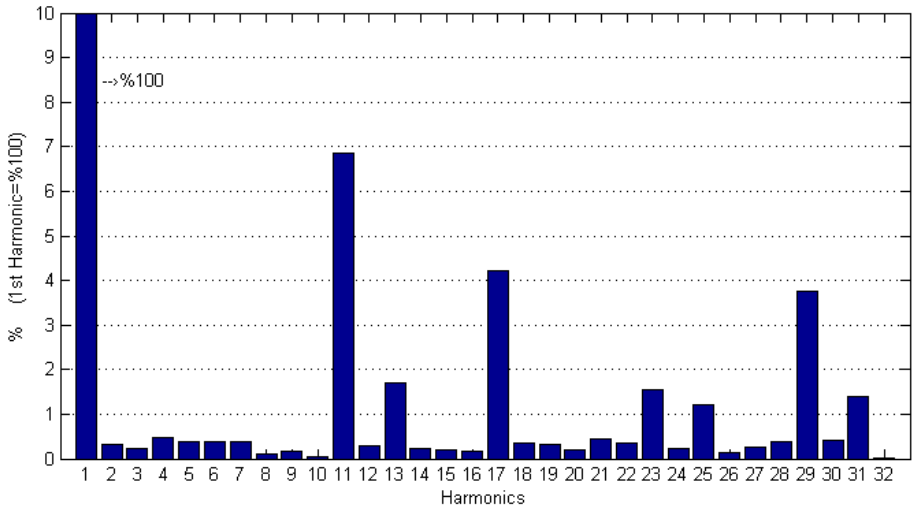

Figure 5.15 Line to Line Voltage Harmonics at 0VAr Reactive Power

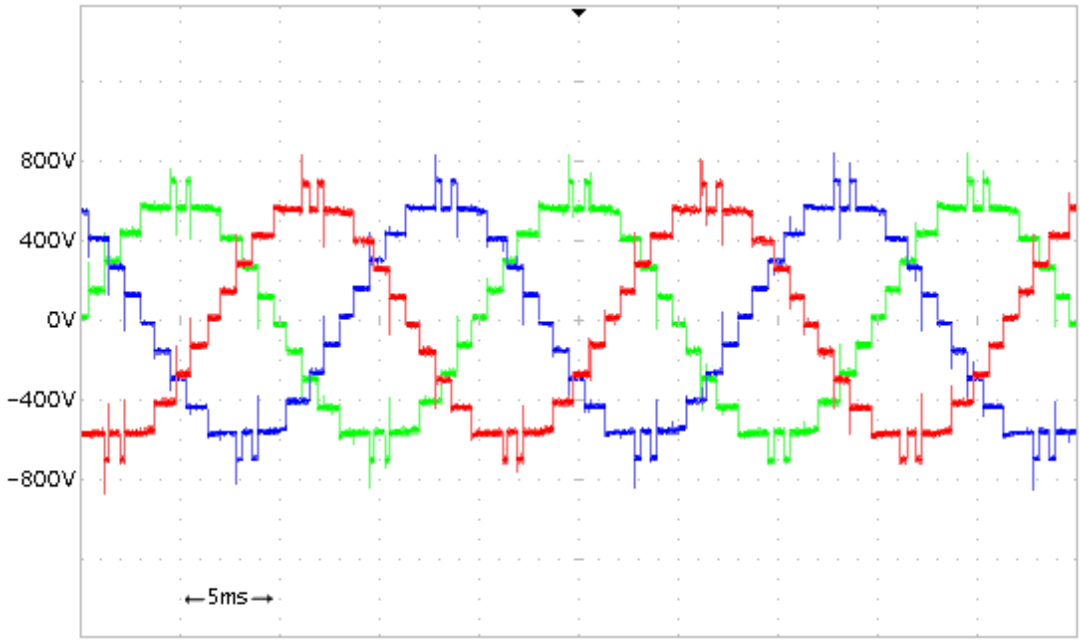

Figure 5.16 Line to Line Voltages at 33kVAr Capacitive Reactive Power, 400V/div

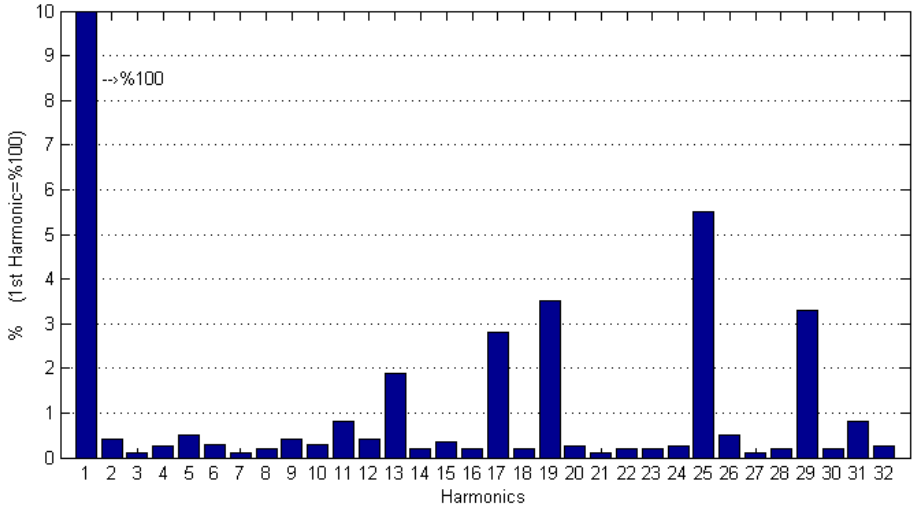

Figure 5.17 Line to Line Voltage Harmonics at 33kVAr Capacitive Reactive Power

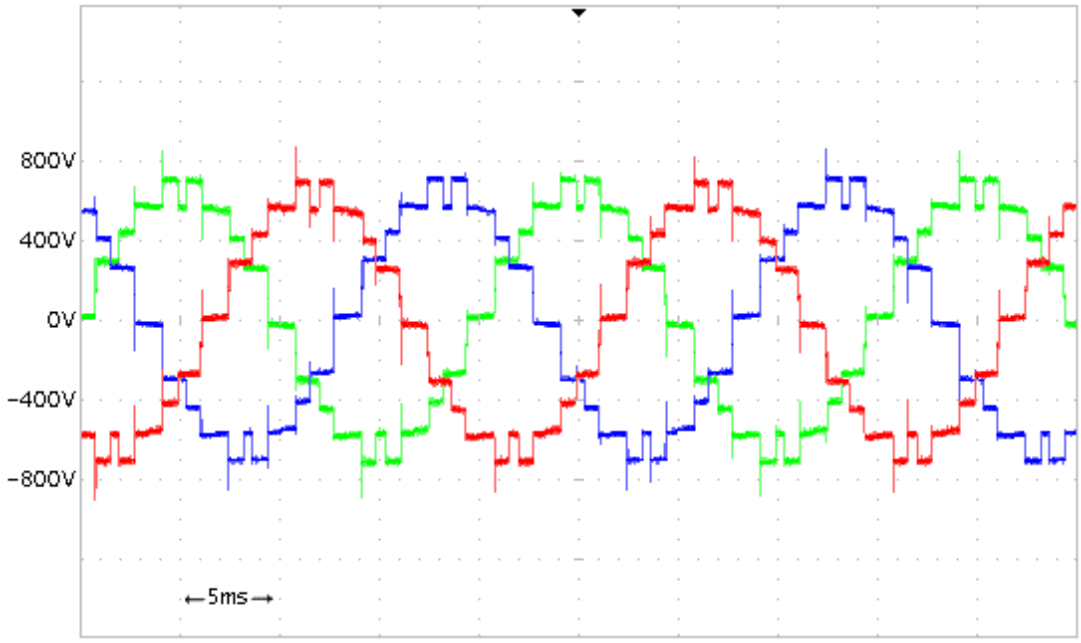

Figure 5.18 Line to Line Voltages at 66kVAr Capacitive Reactive Power, 400V/div

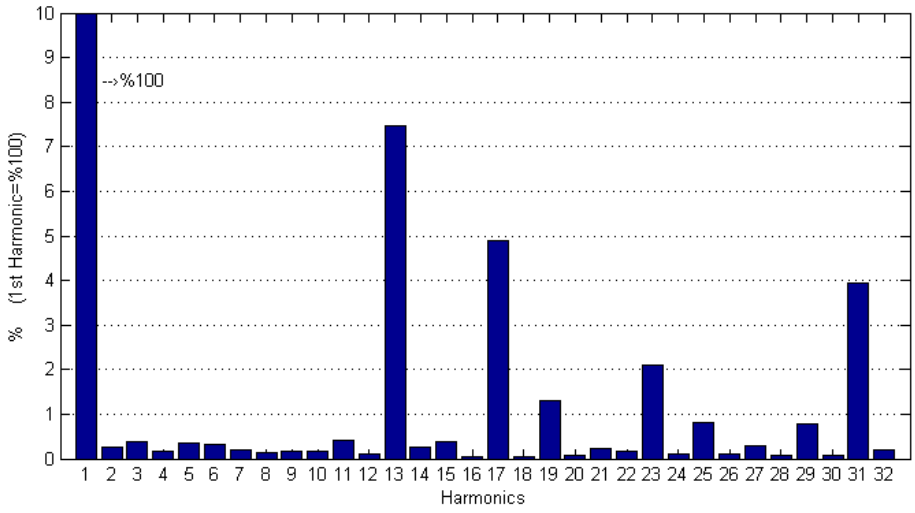

Figure 5.19 Line to Line Voltage Harmonics at 66kVAr Capacitive Reactive Power

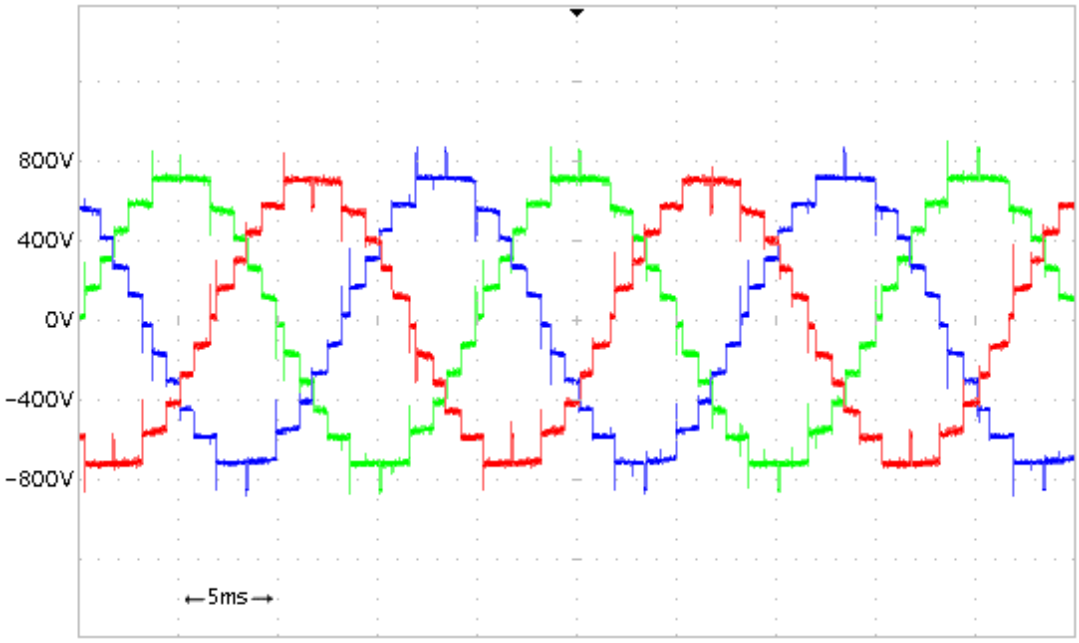

Figure 5.20 Line to Line Voltages at 99kVAr Capacitive Reactive Power, 400V/div

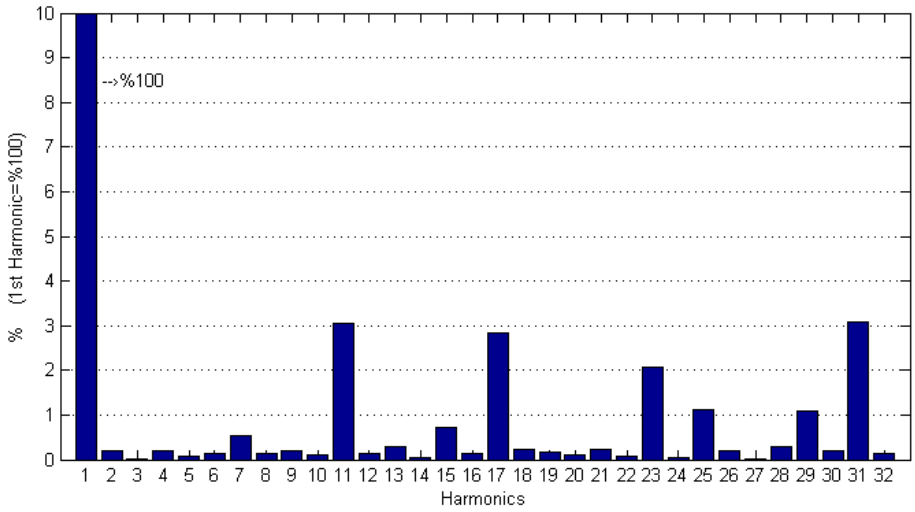

Figure 5.21 Line to Line Voltage Harmonics at 99kVAr Capacitive Reactive Power

5.3 Current Waveforms and Harmonics

Line current waveforms and their harmonic contents are presented in Figure 5.22 to Figure 5.36 for different reactive power outputs. As seen from the graphs, according to IEEE Std. 519-1992 [15], the STATCOM can meet harmonic current standards, if connected to a bus with a short circuit current ratio, I_{sc}/I_{load} given as, $100<I_{sc}/I_{load}<1000$.

Because of harmonic current components greater than 17^{th}, the STATCOM cannot meet harmonic standards of weak buses (i.e. $20<I_{sc}/I_{load}<50$). Simply by adding small filter components to the input of the STATCOM, high frequency harmonics can be filtered and the STATCOM can be supplied from weak buses, without violating the harmonic current limits specified in standards.

Although line to line converter output voltage does not include 3^{rd} harmonics, line currents do. Because:

- Unbalances in the source voltage or PLL can lead to 3^{rd} harmonics.
- STATCOM is a voltage source connected to grid, it can sink the harmonic currents generated by nearby loads.

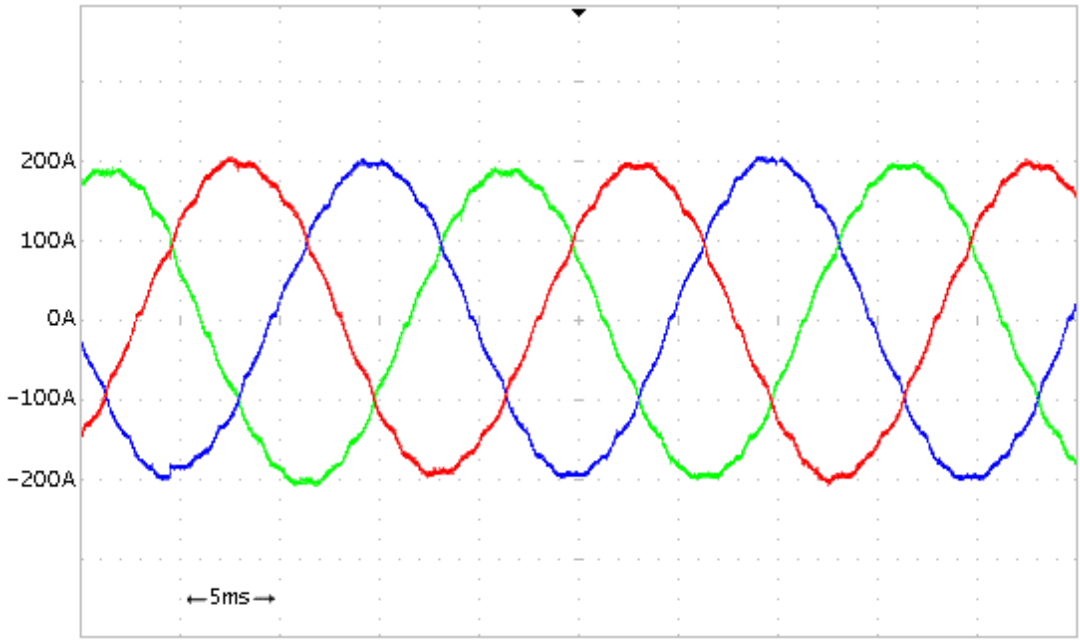

Figure 5.22 Line Currents at 99kVAr Inductive Reactive Power, 100A/div

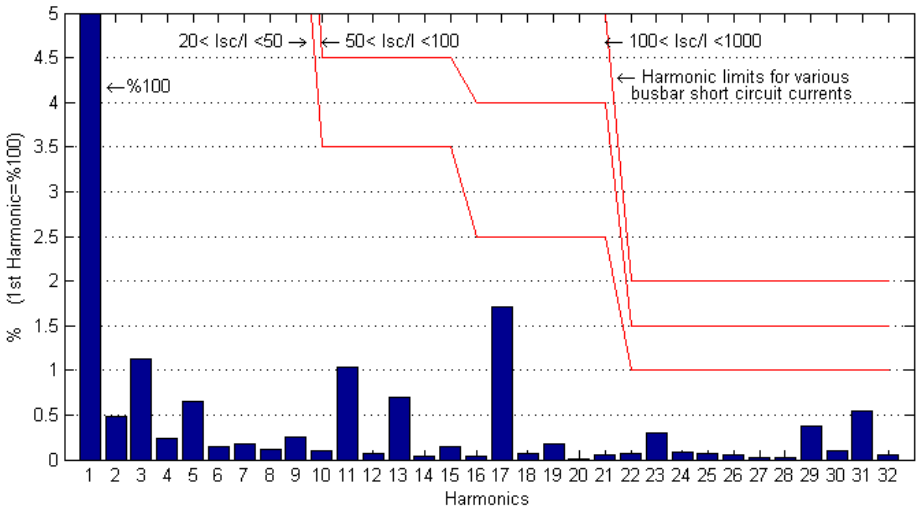

Figure 5.23 Line Current Harmonics at 99kVAr Inductive Reactive Power

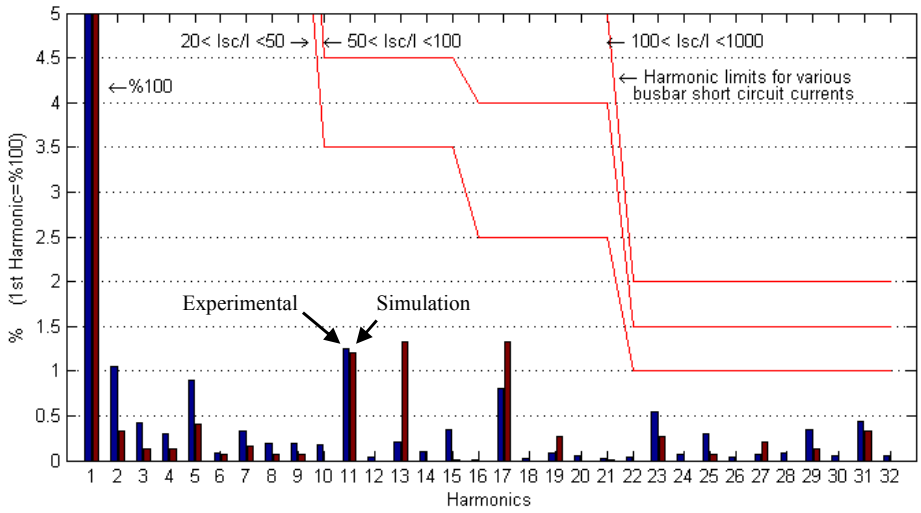

Figure 5.24 Comparison of Simulation and Experimental Line Current Harmonics at 99kVAr Inductive Reactive Power (Blue Bars are Experimental, Brown Bars are Simulation Results)

In Figure 5.24, laboratory test results and simulation results of line current harmonics are presented. Although there are slight differences between them, the variation trend of the graphs are similar. 11^{th}, 13^{th} and 17^{th} harmonics are expected at the simulation stage. Since same harmonic components are present in the laboratory test results, it can be concluded that experimental results are consistent with the simulation results. Similar results are obtained for other reactive power levels as well. Therefore simulation and experimental results are presented on the same graph only for 99kVAr inductive reactive power operation.

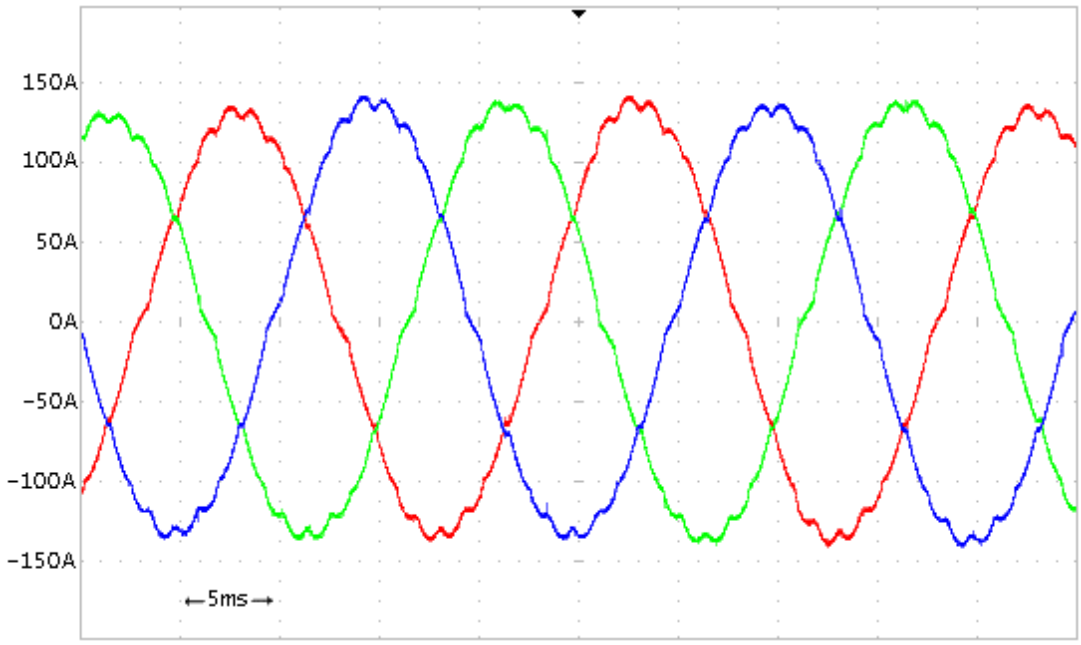

Figure 5.25 Line Currents at 66kVAr Inductive Reactive Power, 50A/div

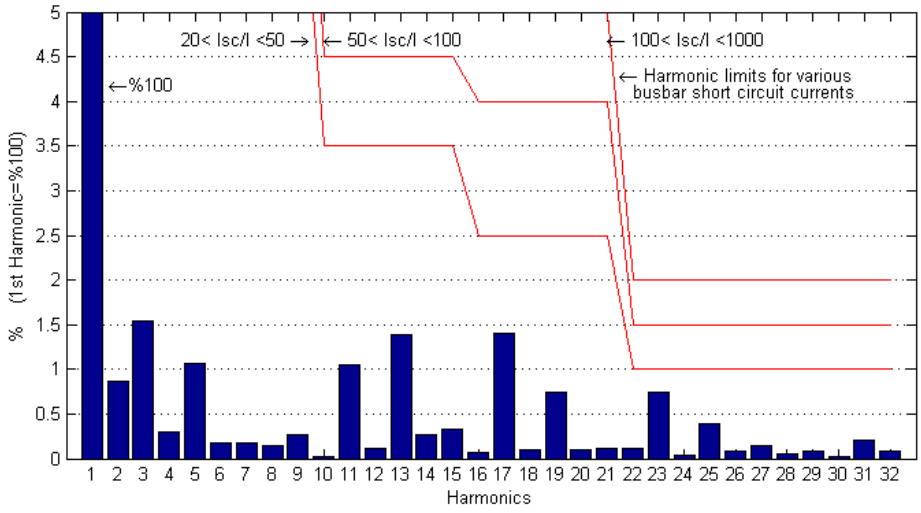

Figure 5.26 Line Current Harmonics at 66kVAr Inductive Reactive Power

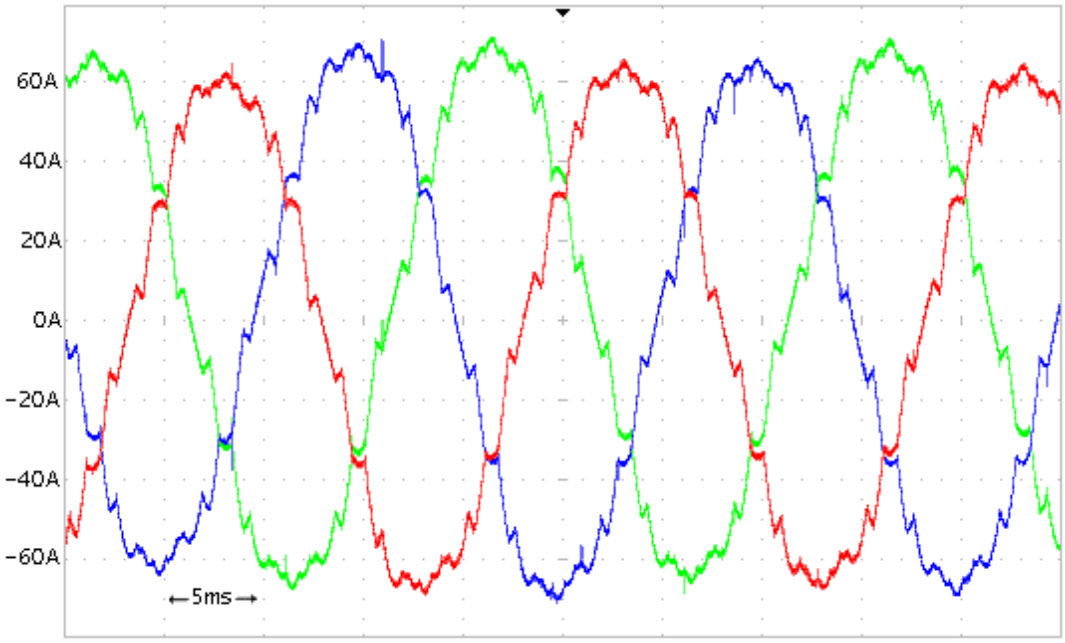

Figure 5.27 Line Currents at 33kVAr Inductive Reactive Power, 20A/div

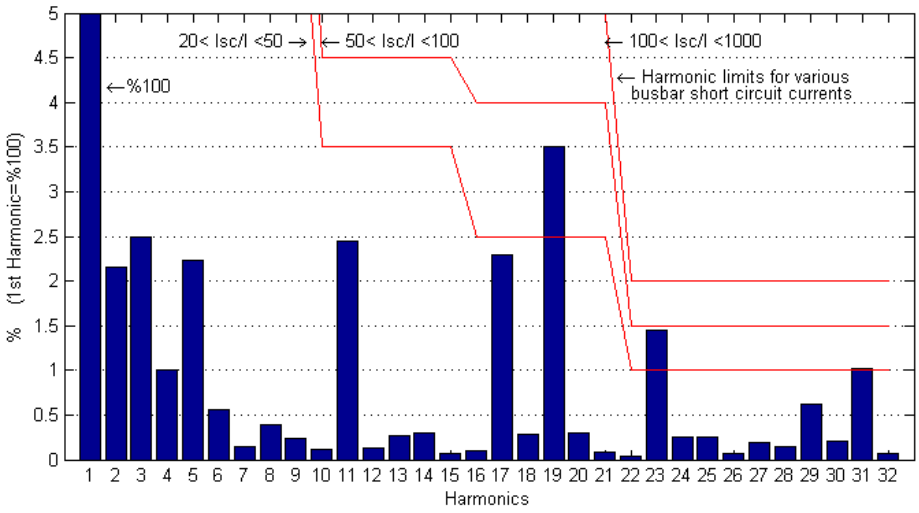

Figure 5.28 Line Current Harmonics at 33kVAr Inductive Reactive Power

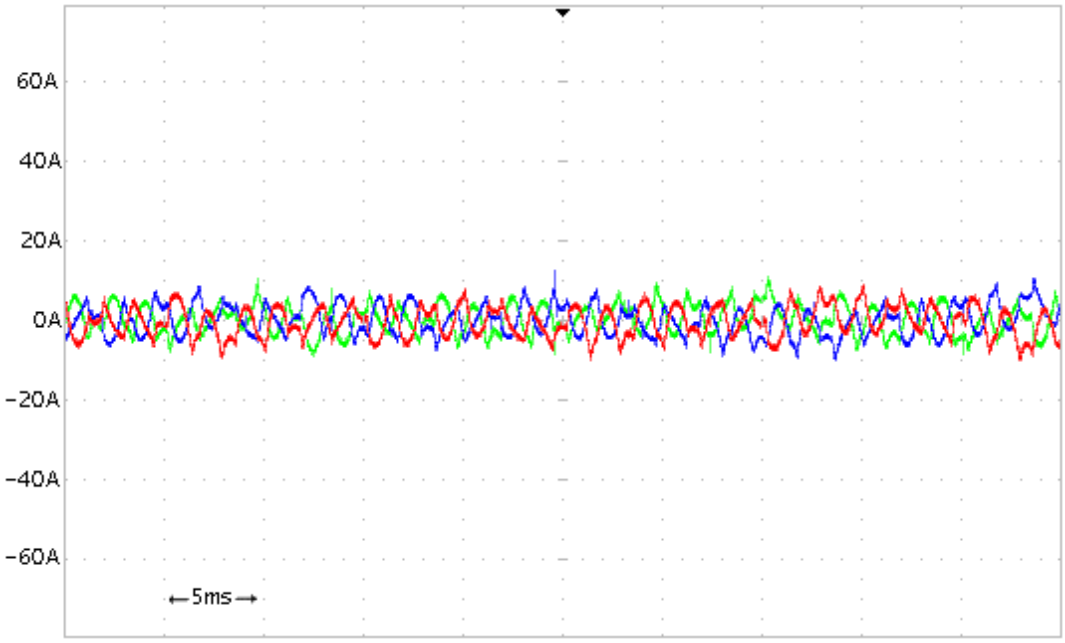

Figure 5.29 Line Currents at 0VAr Reactive Power, 20A/div

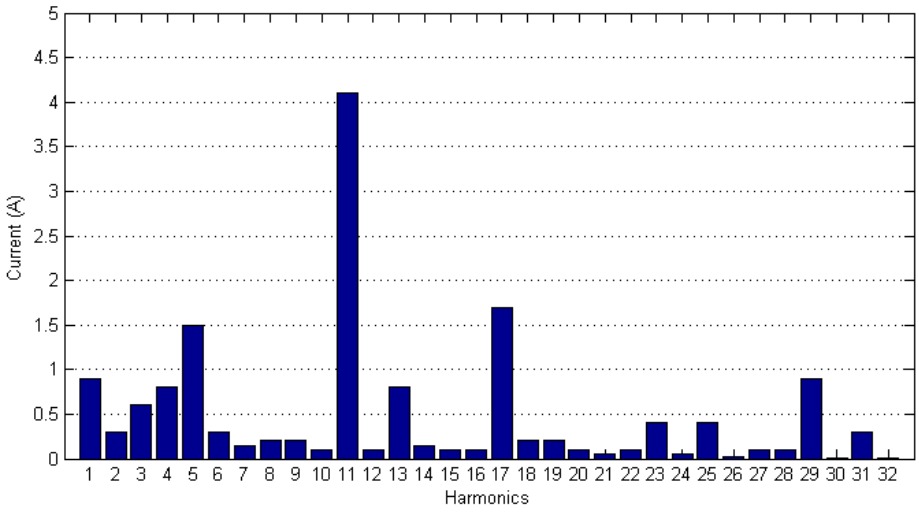

Figure 5.30 Line Current Harmonics at 0VAr Reactive Power

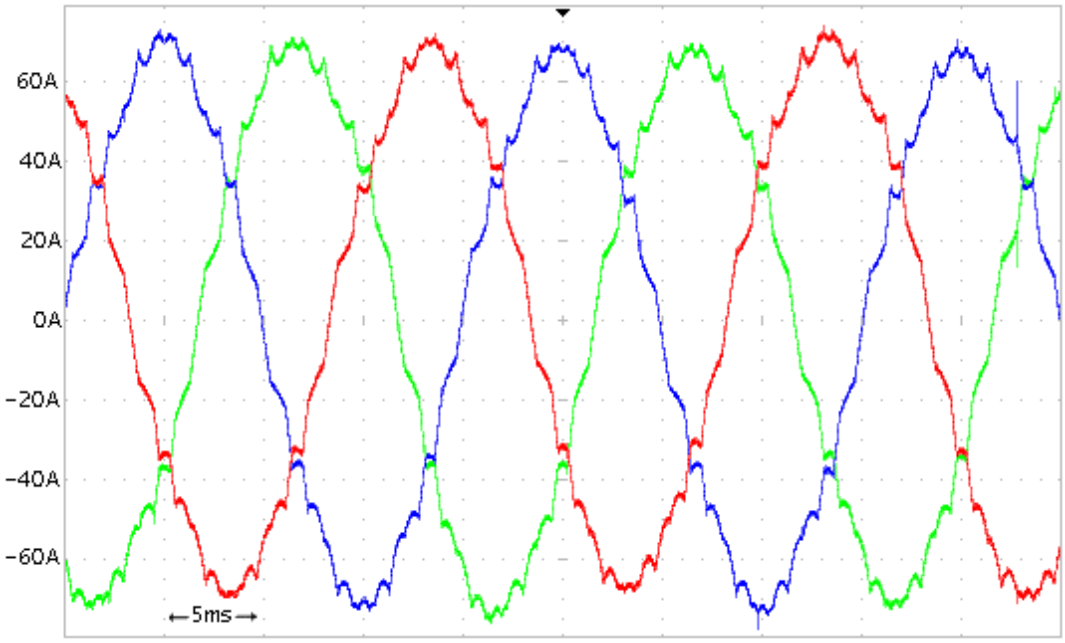

Figure 5.31 Line Currents at 33kVAr Capacitive Reactive Power, 20A/div

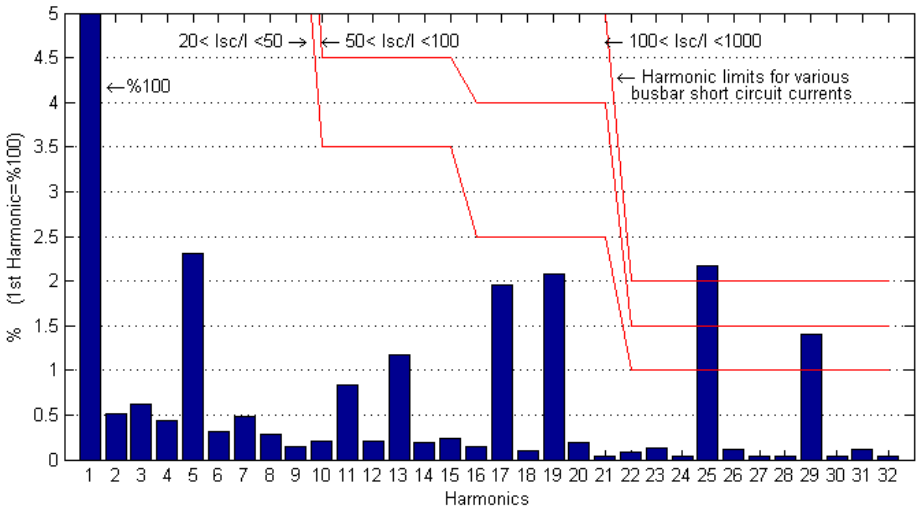

Figure 5.32 Line Current Harmonics at 33kVAr Capacitive Reactive Power

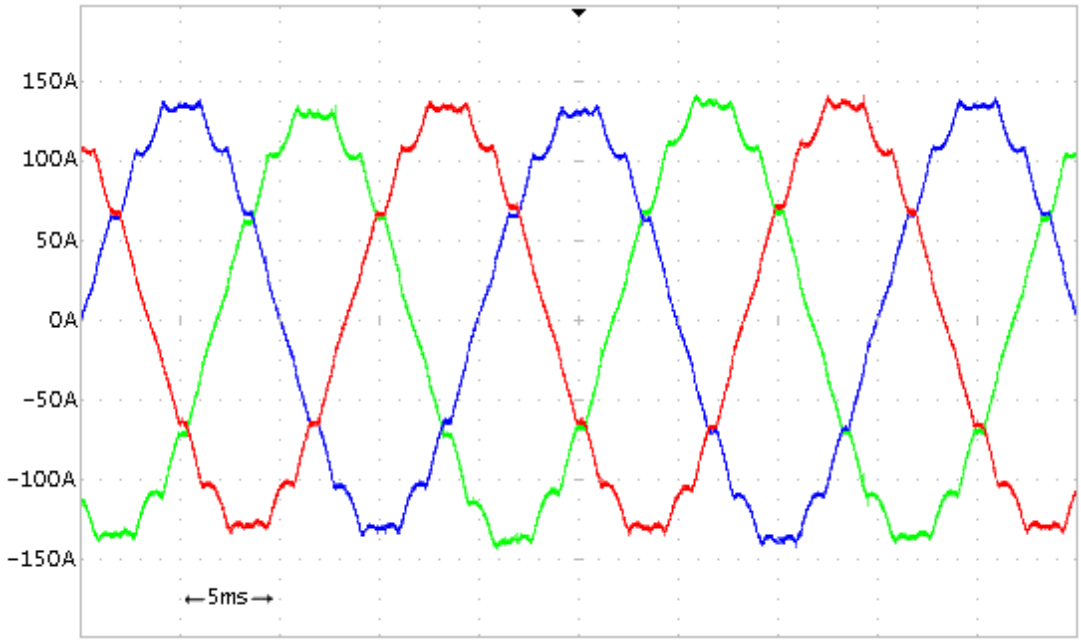

Figure 5.33 Line Currents at 66kVAr Capacitive Reactive Power, 50A/div

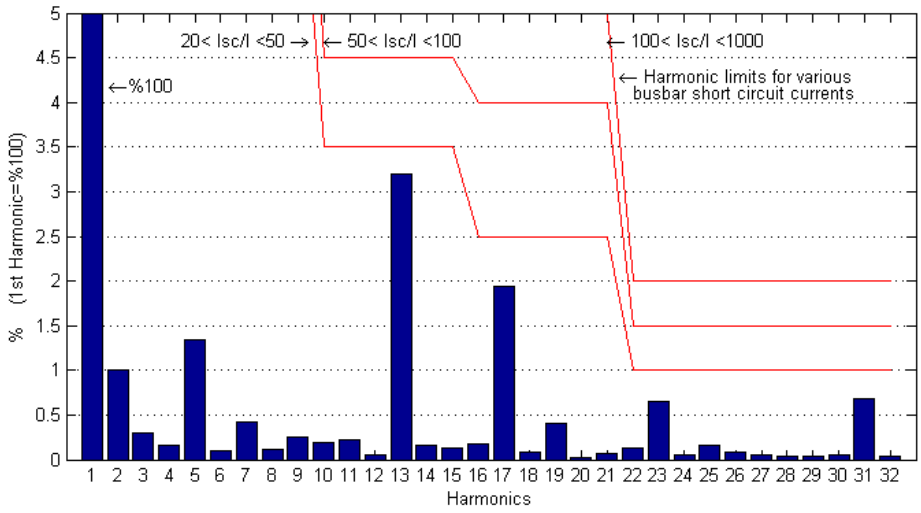

Figure 5.34 Line Current Harmonics at 66kVAr Capacitive Reactive Power

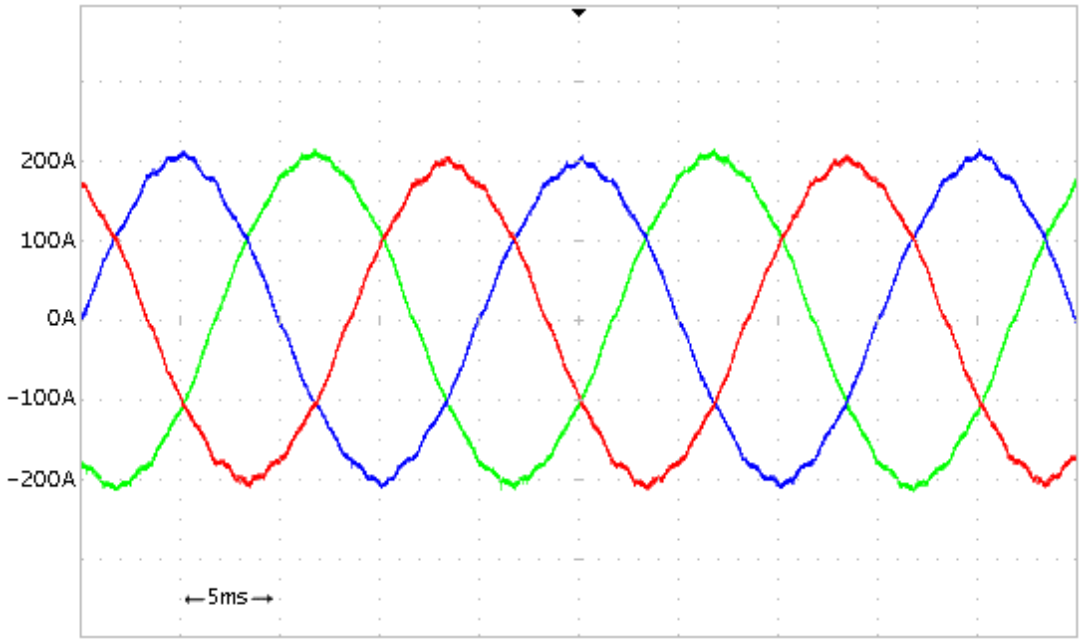

Figure 5.35 Line Currents at 99kVAr Capacitive Reactive Power, 100A/div

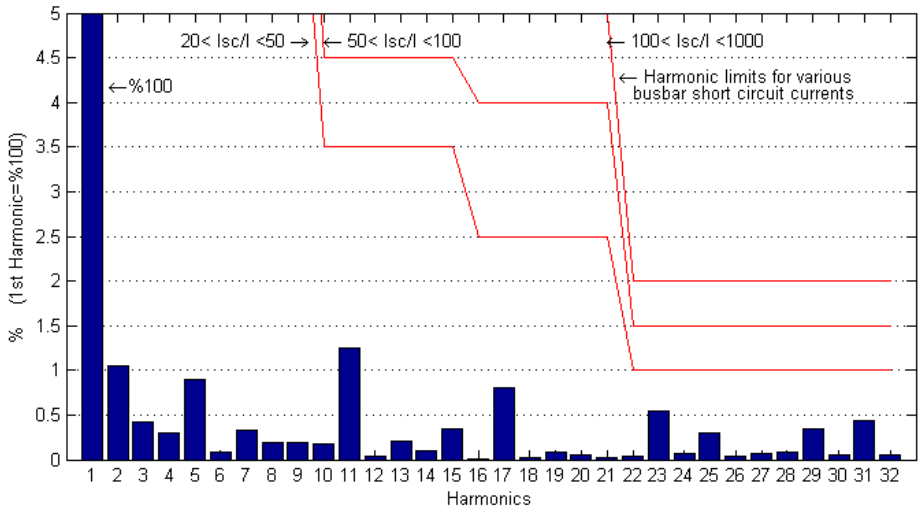

Figure 5.36 Line Current Harmonics at 99kVAr Capacitive Reactive Power

5.4 Line to Neutral Voltages and Line Currents

Line to Neutral Voltages and Line Currents for different reactive powers are given in Figure 5.37 though Figure 5.43. Line current lags the fundamental line to neutral voltage by 90° in inductive reactive power mode (Figure 5.37), as expected.

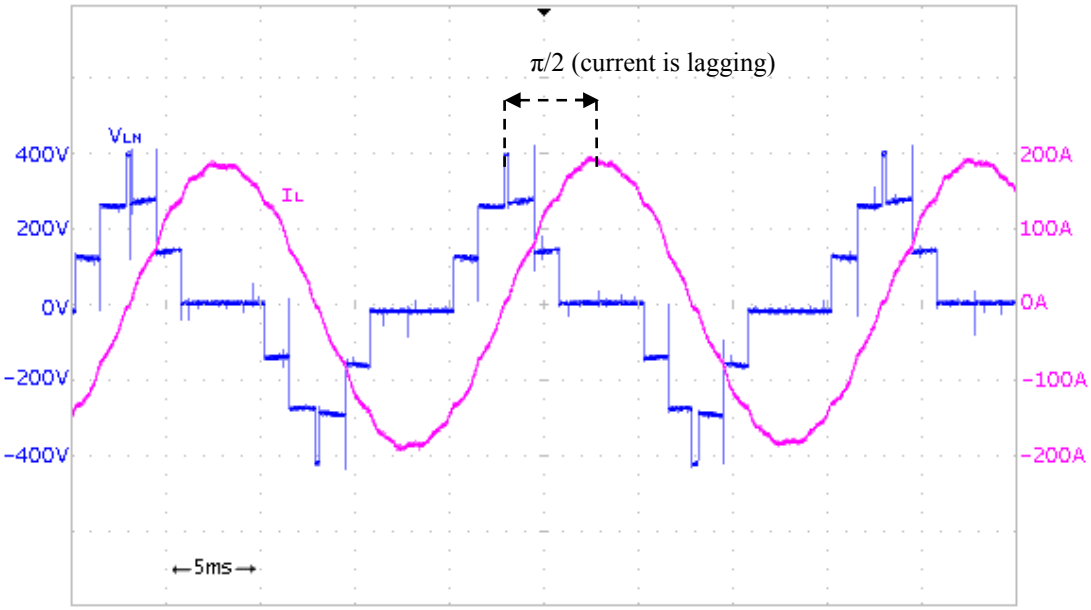

Figure 5.37 Line to Neutral Voltage (blue, 200V/div) and Line Current (pink, 100A/div) at 99kVAr Inductive Reactive Power

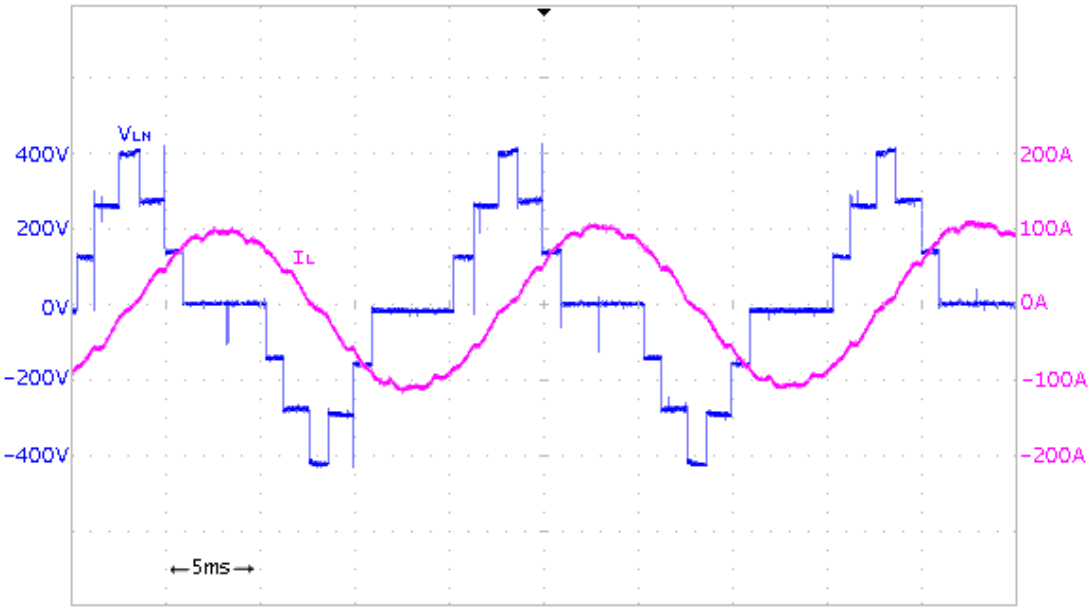

Figure 5.38 Line to Neutral Voltage (blue, 200V/div) and Line Current (pink, 100A/div) at 66kVAr Inductive Reactive Power

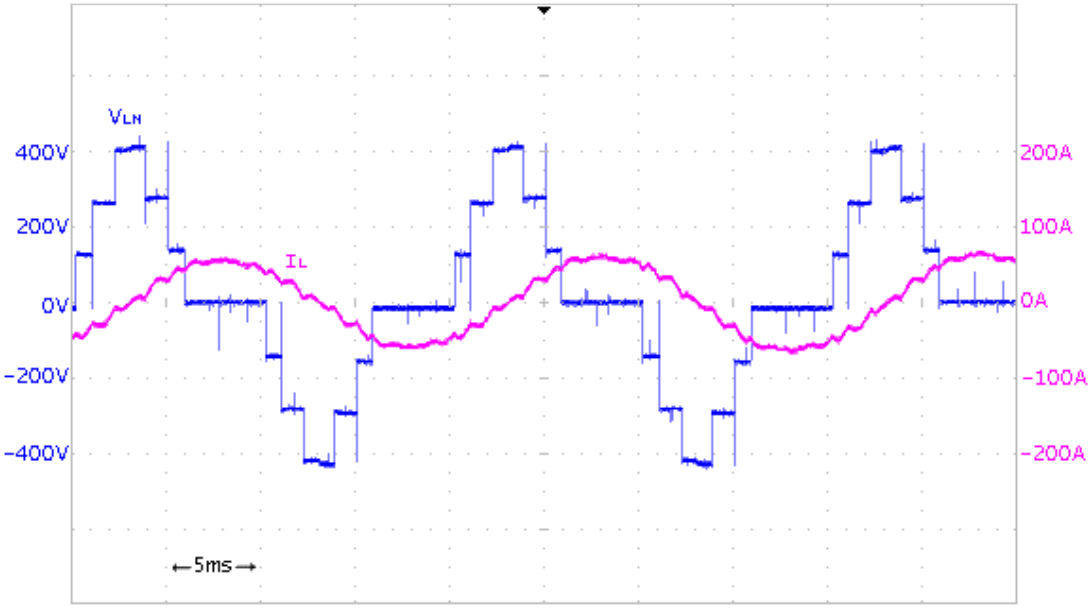

Figure 5.39 Line to Neutral Voltage (blue, 200V/div) and Line Current (pink, 100A/div) at 33kVAr Inductive Reactive Power

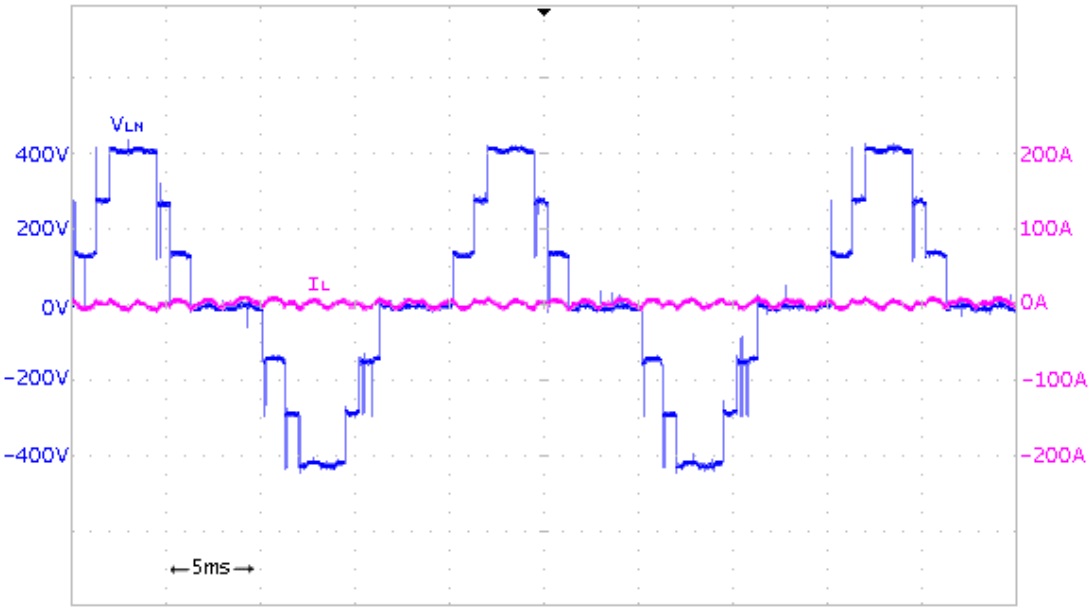

Figure 5.40 Line to Neutral Voltage (blue, 200V/div) and Line Current (pink, 100A/div) at 0VAr Reactive Power

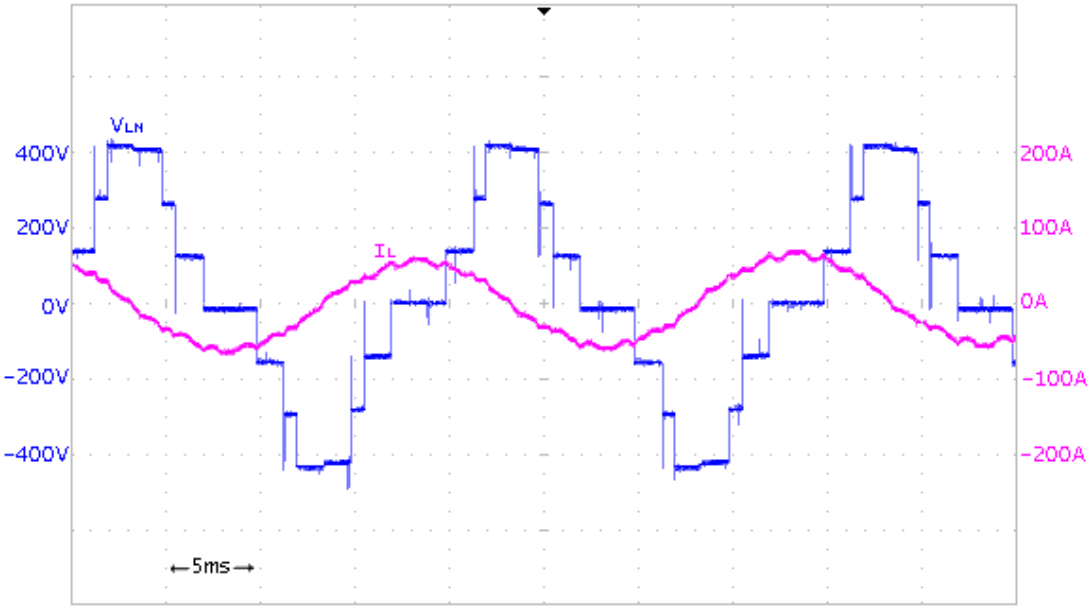

Figure 5.41 Line to Neutral Voltage (blue, 200V/div) and Line Current (pink, 100A/div) at 33kVAr Capacitive Reactive Power

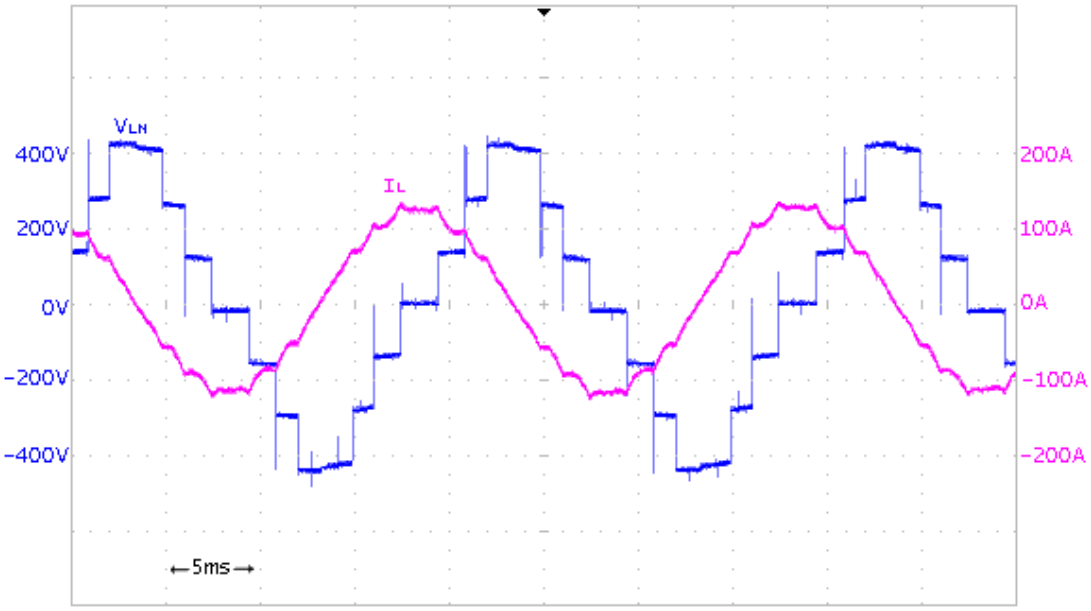

Figure 5.42 Line to Neutral Voltage (blue, 200V/div) and Line Current (pink, 100A/div) at 66kVAr Capacitive Reactive Power

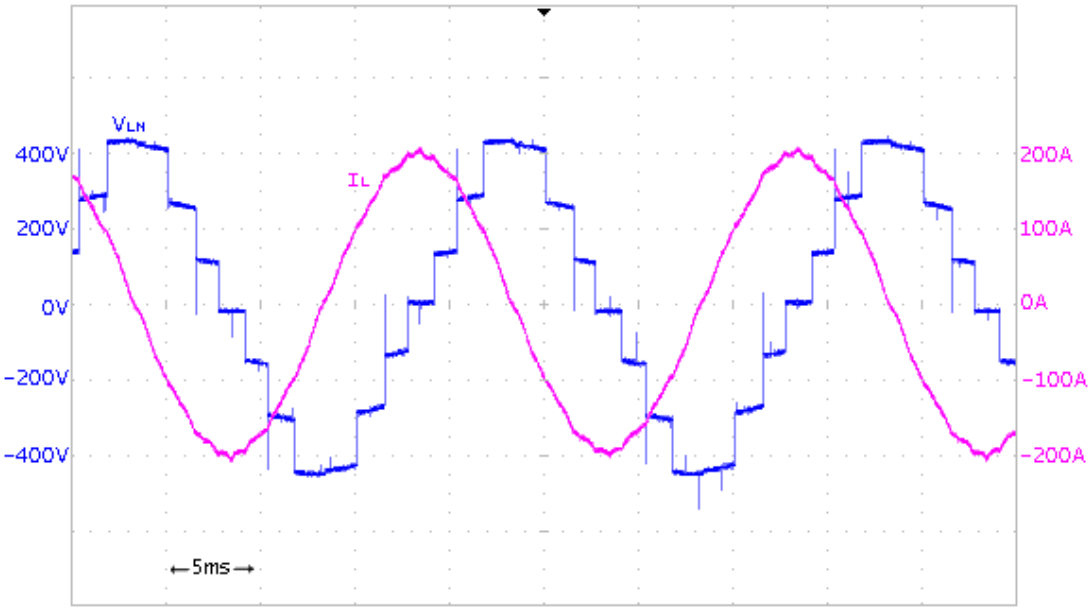

Figure 5.43 Line to Neutral Voltage (blue, 200V/div) and Line Current (pink, 100A/div) at 99kVAr Capacitive Reactive Power

5.5 Voltage and Current THD

THD values for full inductive power (+100kVAr) and full capacitive power (-100kVAr) are obtained.

Results are compared with one of the weakest bus THD limits ($20<I_{sc}/I_{load}<50$) according to IEEE Std. 519-1992 [15] in Table 5.1. THD values for low voltage (<1kV) are considered.

Table 5-2 THD Comparison

	Laboratory Results THD, %	IEEE Std. 519-1992, limits for I_{SC}/I_{LOAD}=20-50 %
Current THD @ 100kVAr	7	8
Voltage THD @ 100kVAr	1.5	3
Current THD @ -100kVAr	5	8
Voltage THD @ -100kVAr	1.5	3

Even in the absence of any filtering component, THD values are below the standards. As number of levels increases, THD values are expected to decrease further.

5.6 Response to the Reactive Power Change

Reactive power settling time for -99kVAr to 99kVAr transition is around 10 cycles (200ms) in Figure 5.44 . Actually the response is slow for an IGBT based converter. In STATCOM subproject of the National Power Quality Project of Turkey, PI parameters are adjusted to optimal values and feed forward control is added to control loop. In this way, response time is decreased to 2 cycles (40ms). Therefore, it can be stated that response time can be decreased significantly by changing the control loop. Transition waveforms are presented in Figure 5.44 and Figure 5.45 .

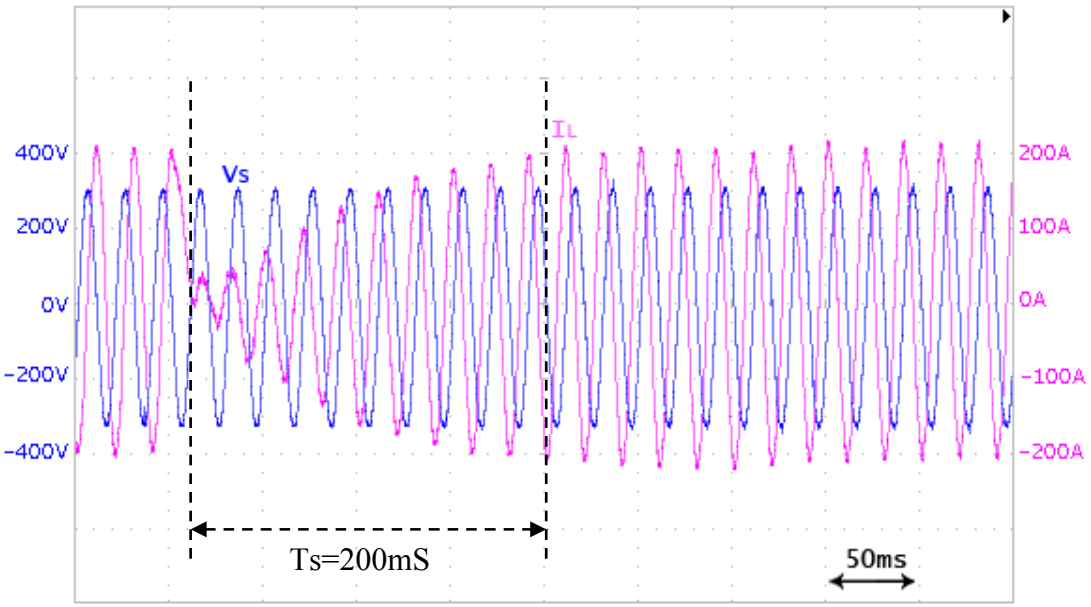

Figure 5.44 Source Line to Neutral Voltage (blue, 200V/div) and Line Current (pink, 100A/div) at 99kVAr to -99kVAr transition

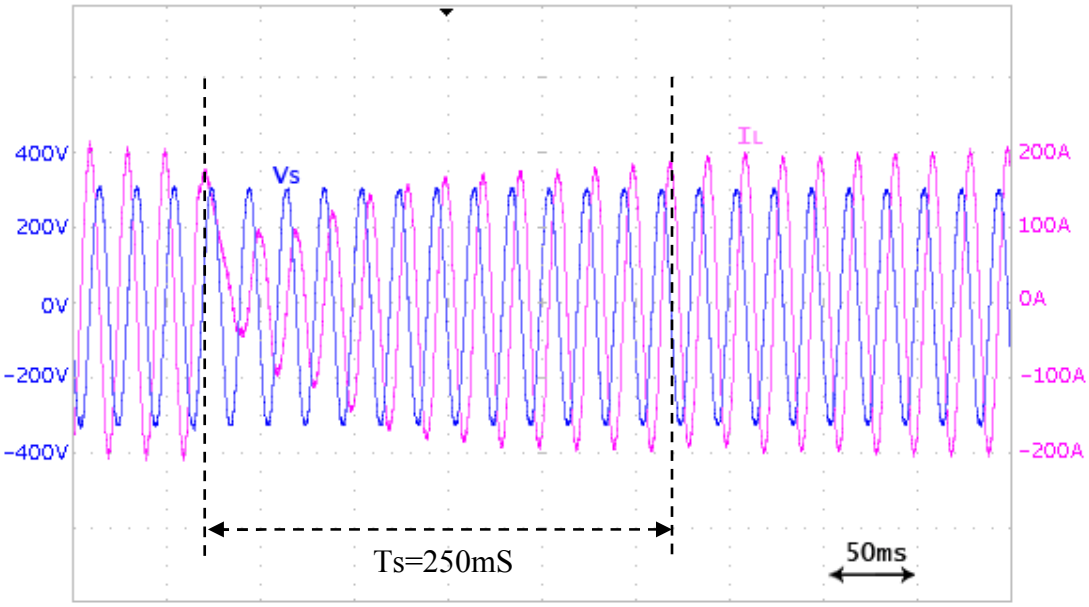

Figure 5.45 Source Line to Neutral Voltage (blue, 200V/div) and Line Current (pink, 100A/div) at -99kVAr to 99kVAr transition

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1. CONCLUSIONS

Among various multilevel converter topologies investigated, the Cascade Multilevel Inverter has been found as the most appropriate and promising topology for STATCOM applications, where a high number of voltage levels is required for either THD minimization and/or medium voltage operation. A 7-level Cascade Multilevel Inverter Based STATCOM has been designed and implemented as a laboratory prototype to verify the operating performance. The implemented system is a compact and modular system made up of three H-Bridges in each phase, controlled by a single DSP-FPGA combination. During research and simulations, it has been realized that known methods for capacitor voltage balancing do not work effectively for all operating conditions (i.e. for all modulation index values). To cope with this problem, a new capacitor voltage balancing method is proposed as explained in [8]. The overall performance of the CMI based STATCOM has been verified both by EMTDC/PSCAD simulations, and by using the 7-Level ±100kVAr laboratory prototype implemented within the scope of the thesis. It has been shown both by simulation and experimental results that the CMI can be satisfactorily operated as a STATCOM in both the steady-state and the transient operating conditions.

According to the experimental results obtained on the 400V line to line, 100kVAr laboratory prototype, the application of modified selective swapping method results in a peak-to-peak capacitor voltage ripple of maximum 14% at rated capacitive reactive power, and 6% at rated inductive reactive power output.

The harmonic content of line currents of STATCOM has been measured for various operating conditions in both the inductive and capacitive reactive power ranges, and it has been found that the implemented 7-level CMI-based STATCOM meets the harmonic current standard limits specified in IEEE Std. 519-1992 [15], except for weakest buses with $I_{sc}/I_{load}<50$. For such weak buses, only high order harmonic current content does not meet the limits specified in [15], which can be easily filtered out by means of small low pass LC filters connected to the ac lines of STATCOM

6.2. FUTURE WORK

By increasing the number of levels, a converter which can be directly connected to medium voltage bus (<36kV) can be implemented. In the absence of a coupling transformer, the cost for medium voltage applications decreases significantly. This can yield to a new era for power quality solutions at medium voltage level.

6500V IGBTs are the commercially available highest voltage switches which can operate at 4500V DC-Link voltages [13]. The number of H-Bridges per phase to generate 20kV line to neutral voltage (36kV line-line) can be calculated as:

$$n = \frac{20000.\sqrt{2}}{4500} = 6.28 \tag{6.1}$$

By using 7 H-Bridges per phase (total 21 H-Bridges), an inverter directly connected to medium voltage bus via a coupling reactor can be realized. Commercial 6500V IGBTs can be used at 300A RMS current [13]. The power of such an inverter can be calculated as:

$$S = V_L.I_L.\sqrt{3} \tag{6.2}$$

$$S = 36000.300.\sqrt{3} = 18MVA \tag{6.3}$$

For more power, 18MVA modules can be paralleled.

Besides reactive power, active power can also be injected to the grid if energy storage elements are connected to DC-Links. As a storage element, battery technologies are evolving. Recent developments in NaS (sodium-sulfur) battery [16] made it possible to use in grid applications. NaS batteries have 5000 cycle life and over 90% charge discharge efficiency. By use of Cascade Multilevel Inverters with DC links supplied with NaS batteries, high power and high efficiency active and reactive power applications can be implemented.

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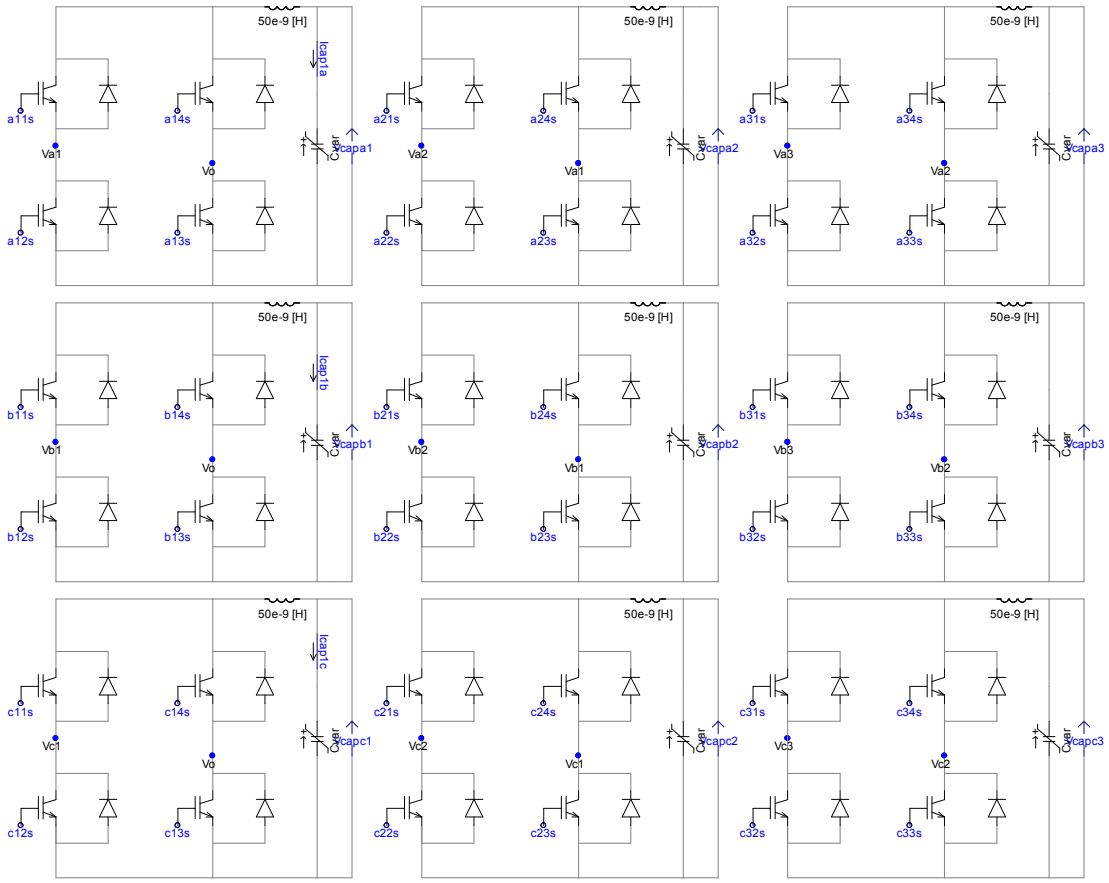
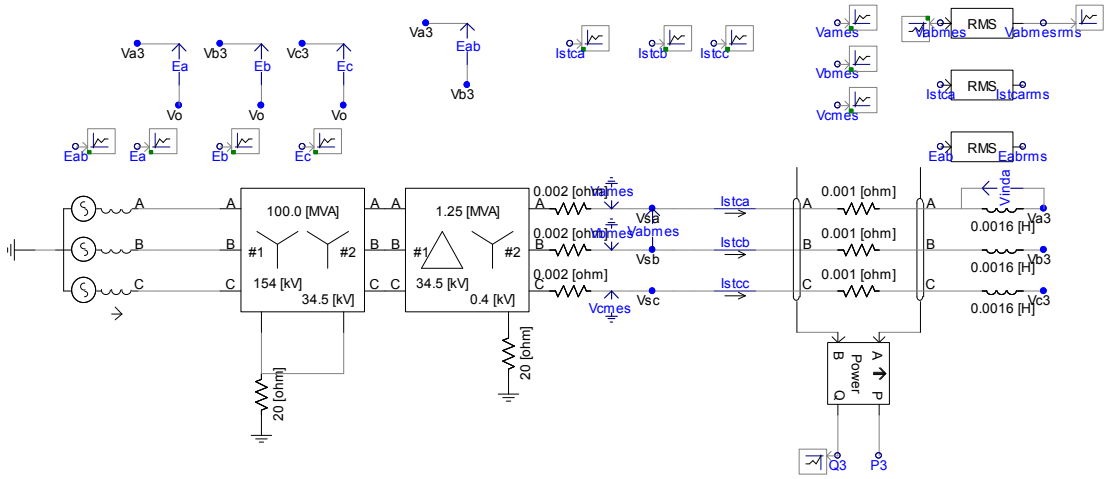
APPENDIX – A

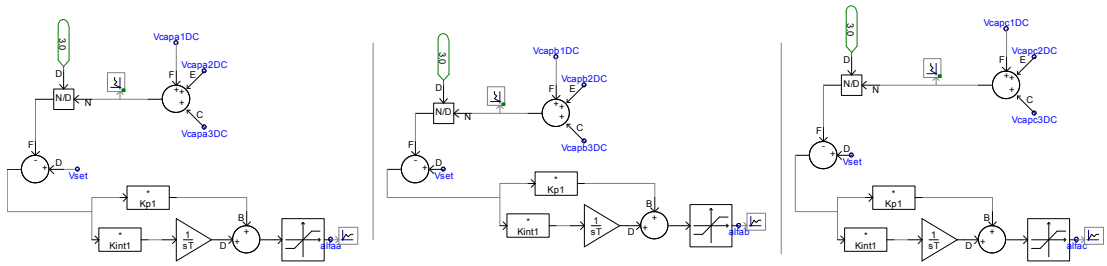
PSCAD EMTDC SIMULATION CIRCUITS



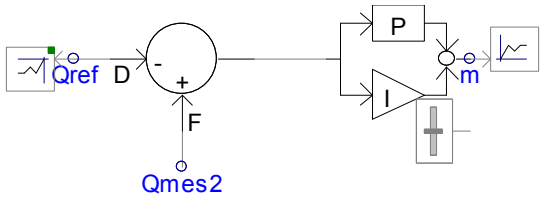
Converter Stage



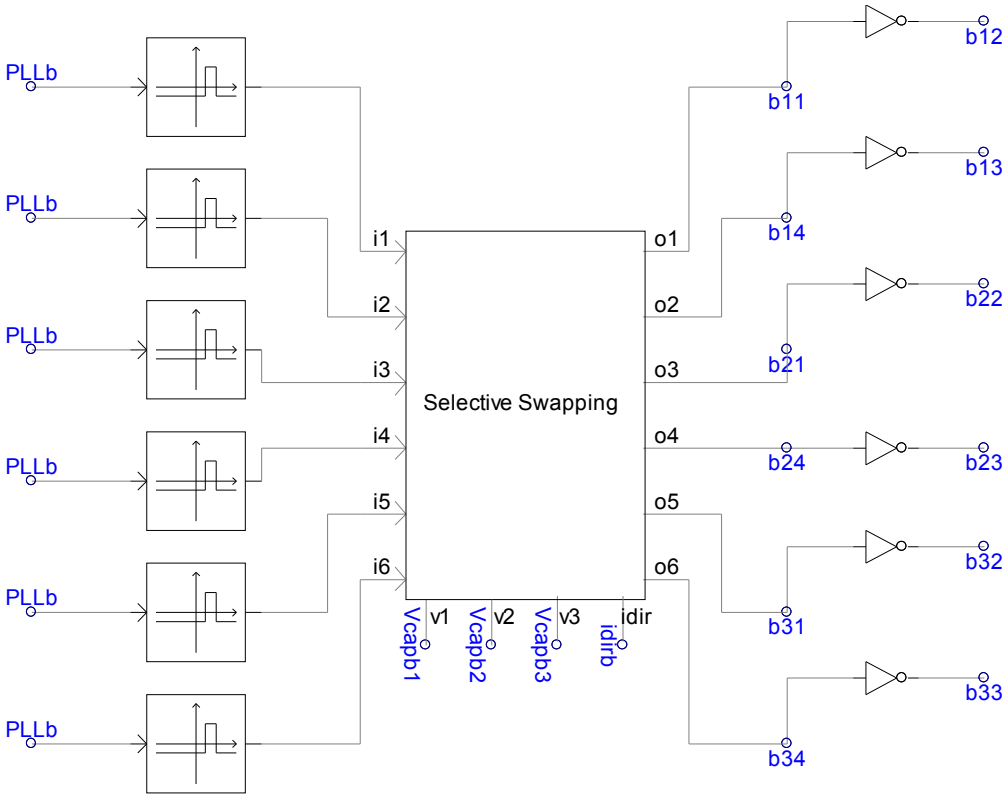
Coupling Stage between Converter and Supply



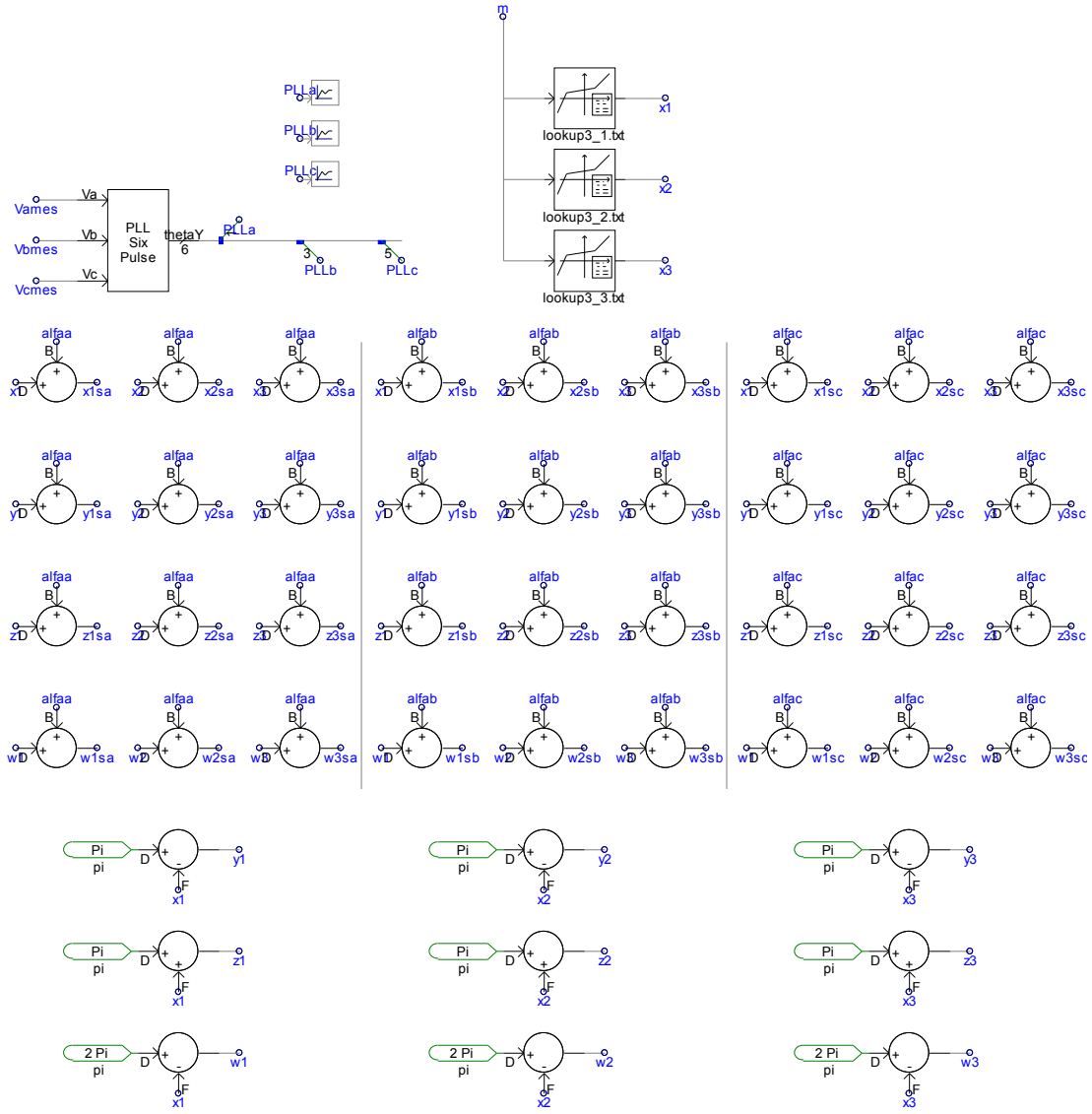
Active Power Controllers



Reactive Power Controller



Selective Swapping Module



Switching Angle Look-up Tables

APPENDIX – B

COOLING FAN PROPERTIES

FP-108D/DC

80x80x25.4mm

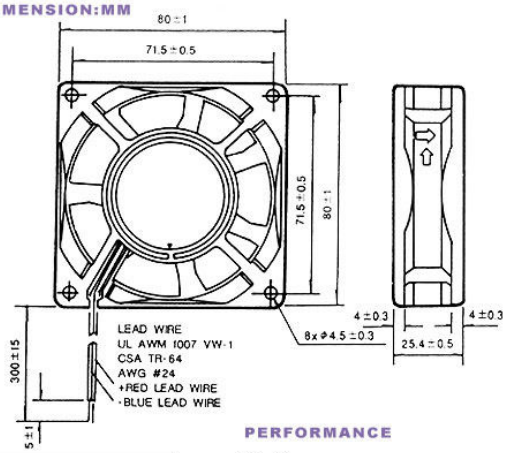
DESIGN FEATURES

*BEARING SYSTEM:	SLEEVE BEARING & BALL BEARING
*WEIGHT:	100(g)
*IMPELLER:	PLASTIC WITH FIBER GLASS FILLED UL 94V-0
*HOUSING:	PLASTIC WITH FIBER GLASS FILLED UL 94V-0
*MOTOR:	BRUSHLESS DC
*CONNECTING:	WIRE LEADS
*SPEED:	S-1 HIGH SPEED TYPE S-2 MEDIUM SPEED TYPE S-3 LOW SPEED TYPE

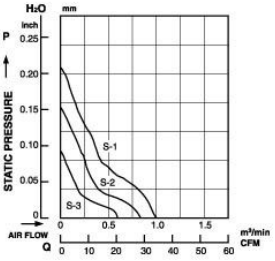
*AVAILABLE FG TYPE FOR SPEED AENSOR SIGNAL

*AVAILABLE RD FOR ROTOR LOCKED ALARM SIGNAL

DIMENSION:MM



PERFORMANCE



SPECIFICATIONS

Model No.	Voltage (VDC)	Air (CFM)	Volume (M^3/Min)	Current (A)	Power (W)	Speed (RPM)	Static pressure (Inch-H_2O)	Noise (dBA)
FP-108D/DC (S-1)	12	40	1.13	0.20	2.40	3200	0.22	35
	24	40	1.13	0.13	3.12	3200	0.22	35
FP-108D/DC (S-2)	12	33	0.93	0.16	1.92	2600	0.15	32
	24	33	0.93	0.11	2.64	2600	0.15	32
FP-108D/DC (S-3)	12	27.8	0.79	0.12	1.44	2200	0.09	25
	24	27.8	0.79	0.09	2.16	2200	0.09	25