# SYNTHESIS AND CHARACTERIZATION OF SEMICONDUCTOR NANOWIRES VIA ELECTROCHEMICAL TECHNIQUE

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**I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.**

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# ABSTRACT

SYNTHESIS AND CHARACTERIZATION OF SEMICONDUCTOR NANOWIRES VIA ELECTROCHEMICAL TECHNIQUE

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This thesis aims to investigate structural, optical and photoelectrochemical behavior of CdS nanowires and their heterojunctions with CdTe and polypyrrole nanowires. In the first part, CdS nanowires have been synthesized via electrochemical template-based route. It has been observed that synthesis conditions, such as bias voltage and deposition time, affect the morphology, optical and photoelectrochemical characteristics of CdS nanowires. Depending on the deposition time, length of the CdS nanowires changed from 100-200 nm to 3-4 μm. Also the diameter of the nanowires increased with increasing the deposition time. Structure of the CdS nanowires has been confirmed by X-ray diffraction spectrometry and EDX analysis. Phototelectrochemical performances of the CdS nanowires have been changed dramatically with bias voltage and deposition time.

In the second part of this thesis, CdTe nanostructures have been deposited on CdS nanowires. Change in optical and photoelectrochemical behavior of CdS nanowires after CdTe deposition has been investigated.

Organic semiconductors and their composites with inorganic materials have been gaining attention due to tunable optical, electrical and magnetic properties. Also, ease of fabrication techniques, and therefore, low cost made these materials attractive for lots of applications including photovoltaic devices and flexible electronics.

In the last part of this thesis, heterojunctions of CdS and Polypyrrole (Ppy) nanowires have been synthesized. Like CdS/CdTe heteronanostructures, first the CdS nanowires have been electrochemically deposited in anodized alumina template and then Ppy has been successfully deposited on CdS nanowires. In order to investigate the effects of polypyrrole synthesis conditions on CdS/Ppy heteronanostructures, CdS nanowire synthesis conditions have been kept constant. It has been observed that morphology and photoelectrochemical behavior of the Ppy nanowires has been affected from Ppy synthesis conditions. The photoelectrochemical performance changes of CdS/Ppy heteronanostructures have been also investigated in this part.

**Keywords:** Cadmium sulfide, Polypyrrole, Cadmium Telluride, Nanowire, Semiconductor, Photovoltaic, Morphological Properties, Optical Properties, Electrical Properties, Photoelectrochemical Properties.

# ÖZ

YARI İLETKEN NANOÇUBUKLARIN ELEKTROKİMYASAL TEKNİKLE SENTEZLENMESİ VE KARAKTERİZASYONU

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Bu tezde CdS nano çubukların yapısal, optik ve fotoelektrokimyasal yapılarının ve bu nano çubukların CdTe ve polipirol nano çubuklara heteroekleminin incelenmesi amaçlanmaktadır. Tezin ilk aşamasında CdS nano çubuklar elektrokimyasal yöntemle sentezlenmiştir. Sentez koşullarının (uygulanan voltaj, kaplama süresi gibi) CdS nano çubukların morfolojisini, optik ve fotoelektrokimyasal özelliklerini etkilediği gözlemlenmiştir. Kaplama süresine bağlı olarak CdS nano çubukların boyları 100-200 nm'den 3-4 μm' ye kadar değişmiştir. CdS nano çubukların yapıları X-ray ve EDX analizleri ile doğrulanmıştır. CdS nano çubukların fotoelektrokimyasal performansları uygulanan üretim voltajına ve süreye bağlı olarak çarpıcı şekilde değişmiştir. Tezin ikinci aşamasında CdTe nano yapılar CdS nano çubukların üzerine biriktirilmiştir. CdS nano çubukların CdTe nano yapılar eklendikten sonraki optik ve fotoelektrokimyasal davranşlarındaki değişimler

incelenmiştir. Organik yarı iletkenler ve bunların inorganik malzemelerle olan kompozitleri ayarlanabilir optik, elektriksel ve manyetik özelliklerinden dolayı gün geçtikçe ilgi çekmektedir. Ayrıca kolay fabrikasyon teknikleri ve buna bağlı olarak düşük maliyetleri bu tür malzemeleri içinde fotovoltaik cihazlar ve esnek elektroniklerin de bulunduğu birçok uygulama için ilgi çekici kılmaktadır. Tezin son kısmında ise CdS ve polipirol (Ppy) heteroeklem nano çubuklar sentezlenmiştir. CdS/CdTe heteronano yapılarda olduğu gibi, önce CdS nano çubuklar elektrokimyasal yöntemle anotlanmş alüminyum kalıplarının içinde sentezlenmiş daha sonra Ppy başarıyla CdS nano çubukların üstüne kaplanmıştır. Polipirol sentez koşullarının CdS/Ppy heteronano yapılar üzerindeki etkisini inceleyebilmek için, CdS nano çubuk sentezleme koşulları sabit tutulmuştur. Polipirol nano çubukların morfolojisinin ve fotoelektrokimyasal özelliklerinin Ppy sentezleme koşullarından etkilendiği gözlemlenmiştir. CdS/Ppy heteronano yapıların fotoelektrokimysal performaslarının değişimleride bu bölümde incelenmiştir.

**Anahtar Kelimeler:** Kadmiyum sülfit, Polipirol, Kadmiyum tellurit, Nanoçubuk, Yarıiletken, Fotovoltaik, Morfolojik Özellikler, Optik Özellikler, Elektriksel Özellikler, Fotoelektrokimyasal Özellikler.

**To my beloved family…**

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# ABBREVIATIONS

| | |
|---|---|
| **Cd** | Cadmium |
| **S** | Sulphur |
| **CdS** | Cadmium Sulfide |
| **PET** | Polyethylene Terephthalate |
| **AAO** | Anodized Alumina Oxide |
| **PPy** | Polypyrrole |
| **CdTe** | Cadmium Telluride |
| **SEM** | Scanning Electron Microscope |
| **EDX** | Energy Dispersive X-Ray |
| **XRD** | X-Ray Diffraction |
| **PEC** | Photoelectrochemical Cell |
| **$CdCl_2$** | Cadmium Chloride |
| **DMSO** | Dimethyl Sulfoxide |
| **$Na_2S$** | Sodium Sulfide |
| **NaOH** | Sodium Hydroxide |
| $V_{oc}$ | Open Circuit Potential |
| $I_{sc}$ | Saturation Current |

# CHAPTER 1

# INTRODUCTION

## 1.1 Semiconductors

The solid materials are categorized in three ways when their current carrying capabilities take into account: conductors, semiconductors and insulators. The electronic conductivity of a solid material depends on the movement of the electrons through the structure. Since the core electrons are tightly bound to their own nuclei, the conductivity of the solids is determined by the free electrons in the higher energy levels of the structure. The conductors have plenty of free electrons which are the charge carriers but the insulators have limited free electrons which makes them poor conductor of electricity. On the other hand, a semiconductor is a material having conductance between a conductor and an insulator. It is neither a good conductor nor a good insulator. [1]

The main difference between a metallic conductor and a semiconductor is that the current is carried by the flow of electrons in metallic conductor but in a semiconductor, the current can be carried either by the flow of electrons or by the flow of positively-charged “holes” in the electron structure of the material. “Holes” are lack of electrons in covalent bonds and act equivalently as positive charge carriers. [2.a]

The electrical resistivity of solids varies from the order of $10^{16}$ ohm.m for a good insulator to nearly $10^{-8}$ ohm.m for a conductor. The resistivity of semiconductors lies

within the range $10^{-4}$ to $10^{4}$ ohm.m. Whereas the conductors have positive temperature coefficient of resistivity, semiconductors have negative temperature coefficient. This means that at very low temperatures, semiconductors behave like an insulator but at higher temperatures their resistivity decreases. [3.a]

Furthermore, the conductivity of a pure semiconductor can also be increased by adding certain impurities to it which is called "doping". Such types of semiconductors are called extrinsic semiconductors which will be discussed in 1.3. The specific properties of a semiconductor depend on the impurities, or dopants, added to it.

## 1.2 Band Theory of Solids

Since the atoms in gaseous state are far away from each other, they have limited influence on each other's electronic energy levels. Therefore, their electronic energy levels are the same for a single free atom. However, the energy levels in a crystal are determined by the interaction between the atoms since the atoms are so closely packed. When the atoms form a crystal, the core electrons is screened by the outer-shell electrons so the energy levels of these core electrons are not affected very much but the energy levels of the outer-shell electrons are changed considerably as these electrons are shared between the atoms in the crystal. Because of the very large number of atoms in a crystal, the energy levels are closely spaced so instead of having discrete energy levels as in the case of free electrons, the available energy states form "bands" in crystals.

Whereas *valance band* is the highest energy filled band which is the highest occupied molecular orbital in a molecule (HOMO), *conduction band* is the next higher band which is the lowest unoccupied molecular orbital in a molecule (LUMO). There is an energy gap between two bands which is known as *forbidden energy gap* and no electrons can occupy states in this gap.

The materials can be classified as conductors, semiconductors and insulators according to the fillings of these bands and the size of the energy gap.

There are two possibilities for *conductors*. First, the valance band is not completely filled so an electron can move throughout the structure by jumping to the higher energy level in the valance band Fig. 1.1(b). Secondly, there is very small energy gap between the valance band and the conduction band, moreover, the valance and conduction bands can overlap and the energy gap could even disappear Fig. 1.1 (a). For conductors these movements of electrons need very small amount of energy so significant amount of electrons are thermally exited to the empty energy levels by creating holes in the valance band. By the movement of electrons in the conduction band and holes in the valance band throughout the structure electricity is easily conducted.

In *semiconductors* the valance band is filled so electrons must jump to the conduction band to conduct electricity. Although there is an energy gap between valance and conduction band, it is small enough to excite small number of electrons to the conduction band due to thermal energy Fig. 1.1 (c). As the name implies, they conduct poorly.

In *insulators* the valance band is also filled so electrons must jump to the conduction band to conduct electricity. However, the energy gap between the valance and conduction band is large so the electrons cannot be promoted to conduction band due to thermal energy so that these materials are not good conductors of electricity Fig. 1.1(d), [2.b].

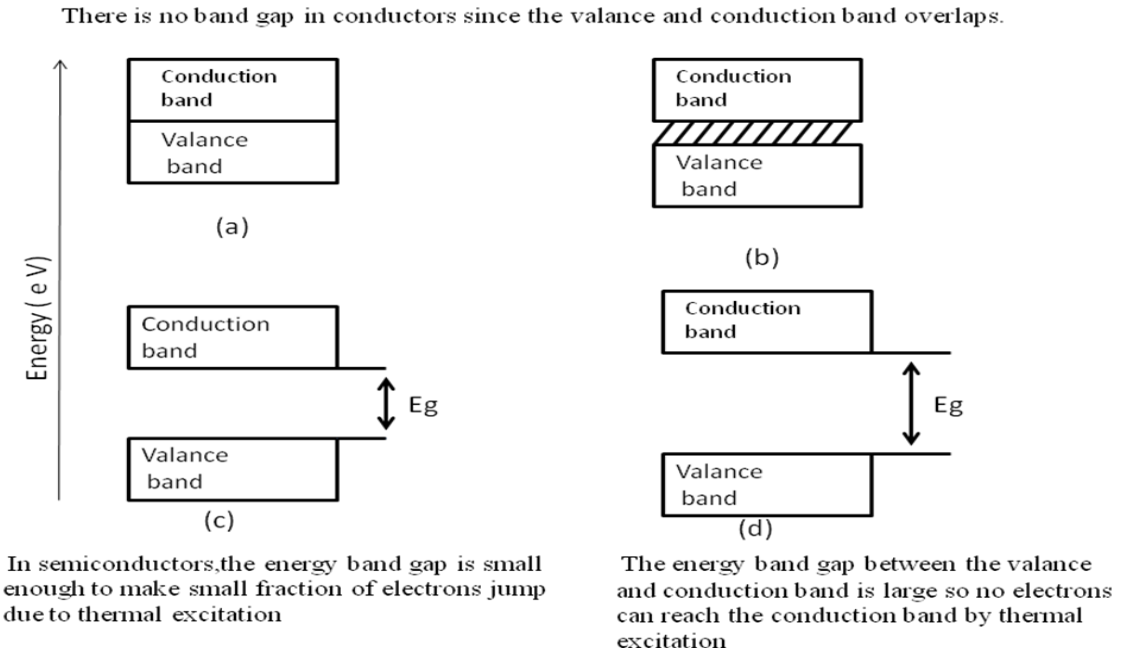



Figure 1.1 Energy band gaps of (a)-(b) conductors, (c) semiconductors, (d) insulators

## 1.3 Semiconductor Types

All the materials which have got semiconducting properties can be categorized in two ways: *organic and inorganic semiconductors*.

***Organic Semiconductor*** is a carbon-based material which shows semiconductor properties. Traditionally organic materials were considered as insulators but in 1963 Weiss *et al.* reported the first conductive organic material "iodine doped oxidized polypyrrole" [4, 5, 6]. After that, in 1977 Alan J. Heeger, Alan MacDiarmid and Hideki Shirakawa reported metallic conductivity in iodine-doped polyacetylene and they received the 2000 Nobel prize in Chemistry *"For the discovery and development of conductive polymers"*[7, 8]. Organic semiconductors have wide applications in

electronics, optoelectronic devices like organic solar cells, and organic light emitting diodes (OLED), displays, batteries and biosensors.

***Inorganic Semiconductors*** are semiconductors made from non-carbon based materials. Inorganic semiconductors could be elemental like silicon, gallium and arsenide or binary compounds like CdS, CdTe, GaAs, InP. Inorganic semiconductors have applications almost in all the fields in which organic semiconductors is used.

Both of the organic and inorganic semiconductors have advantages and disadvantages. First of all, organic semiconductors can be deposited on plastic films which make them inexpensive, flexible and durable. However, organic semiconductors are restricted by low carrier mobility, poor efficiency, large operating voltages and short device lifetimes.

Semiconductors can also be classified according to their purity: *Intrinsic and Extrinsic semiconductors.*

***Intrinsic semiconductors*** are essentially pure semiconductors. The material should not contain any impurities to be called an intrinsic semiconductor. Intrinsic semiconductors could be elemental or compound. Si, Ge, and CdTe are some examples of intrinsic semiconductors. At absolute zero (0 K) all electrons are tied up strongly to their atom so all semiconductors become an insulator at absolute zero since the electrons on valance band cannot jump to the conduction band because of the lack of enough thermal energy to make the electrons jump. A schematic representation of crystalline Si at absolute zero is given in Fig. 1.2.

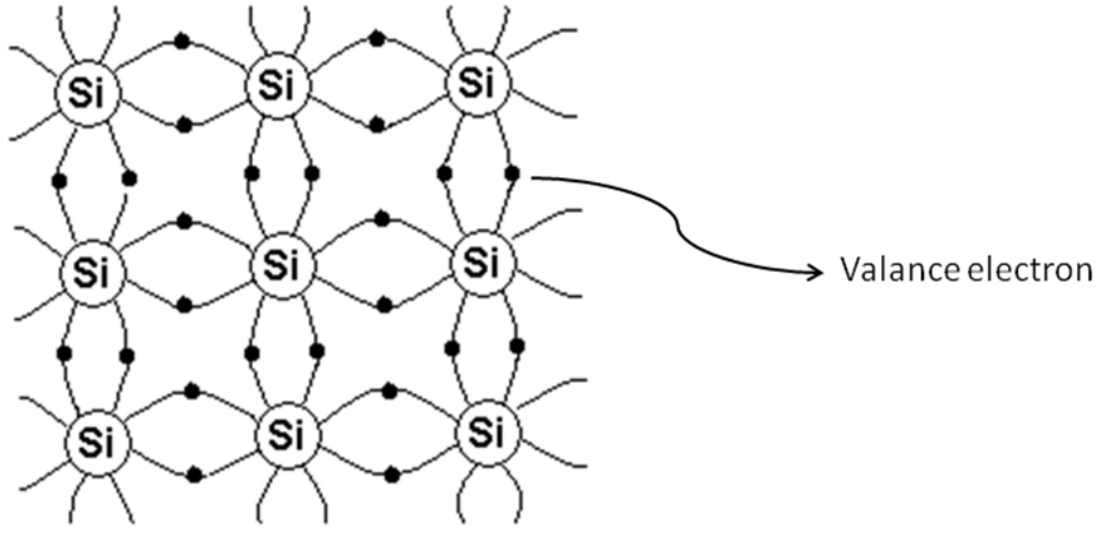



Figure 1.2 Schematic representation of crystalline Si at absolute zero

At any temperature above the absolute zero, some electrons in valance band gain enough thermal energy to jump the conduction band and they leave a vacancy in the valance band. This vacancy can be thought as a positive charge and it is called a “hole”. Thus, every hole in the valance band corresponds to an electron in the conduction band and the number of the electrons in the conduction band is equal to the holes in the valance band Fig. 1.3.a. As the electrons flow through the material, holes flow in the opposite direction and this creates an electrical current in the direction of the motion of the holes Fig. 1.3.b. As a result of these motions, the conductivity of a semiconductor depends on the motion of the holes and electrons. The conductivity of intrinsic semiconductor are very small.

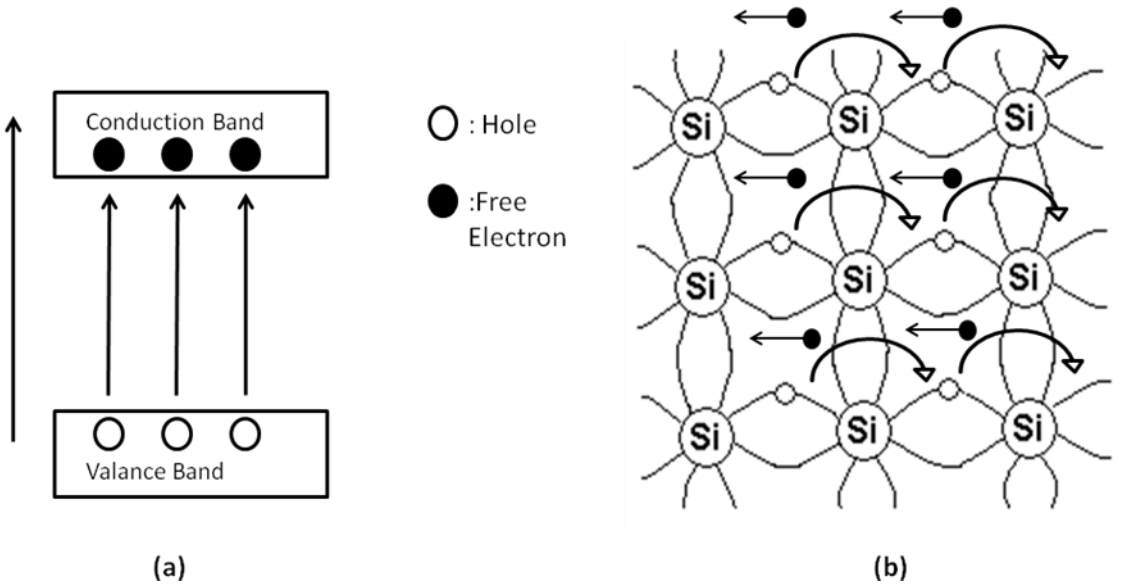



Figure 1.3 Schematic Representation of (a) electron hole pair of semiconductors, (b) flow of electrons and holes

Since the conductivity of intrinsic semiconductors is very small, it can be increased by adding proper impurities in very small proportion. This process is called doping. Doping process changes the conductivity of an intrinsic semiconductor due to the change of the electron and hole carrier concentrations of the semiconductor at thermal equilibrium. A doped semiconductor is called ***extrinsic semiconductors***. It is categorized into two groups: n-type semiconductors and p-type semiconductors.

If an impurity from group V is added to group IV semiconductor, the number of free negative charge carriers increases. The impurity is called donor impurity as it donates electrons and the newly formed crystal is called *n-type semiconductor*. The impurity added should be in a small quantity and it should not disturb the physical state of the crystal. For instance, silicon, which has 4 valance electrons, could be doped with

arsenic, which has 5 valance electrons to get an n-type semiconductor as shown in Fig.1.4.

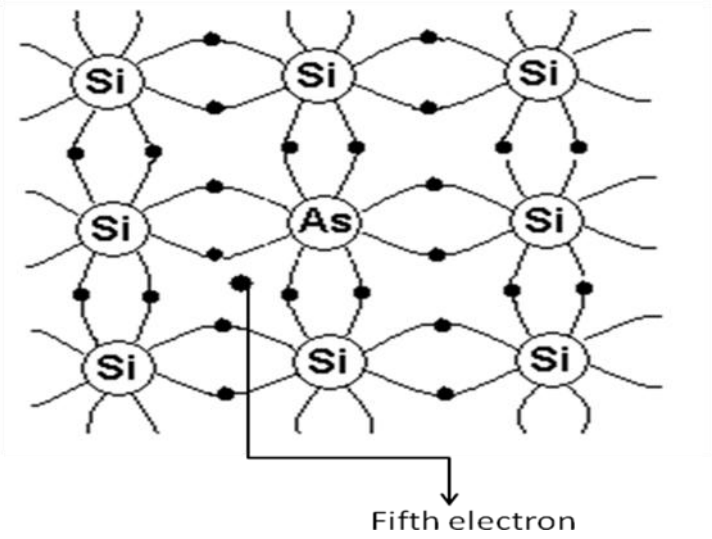



Figure 1.4 n-type Semiconductor

In this case, since the donor atoms give lots of free electrons to the pure semiconductor, which does not have so much free electrons in normal conditions, the majority of the charge carriers are the negative electrons and the holes are the minority.

The energy band diagram of an n-type semiconductor is a little different from a pure semiconductor. Actually, there is another energy level which is close to the conduction band for the donor electron. Therefore, the forbidden band of the donor electron is smaller than the forbidden band of the valance electron Fig. 1.5. That's why n-type semiconductors conduct electricity better than pure semiconductors.

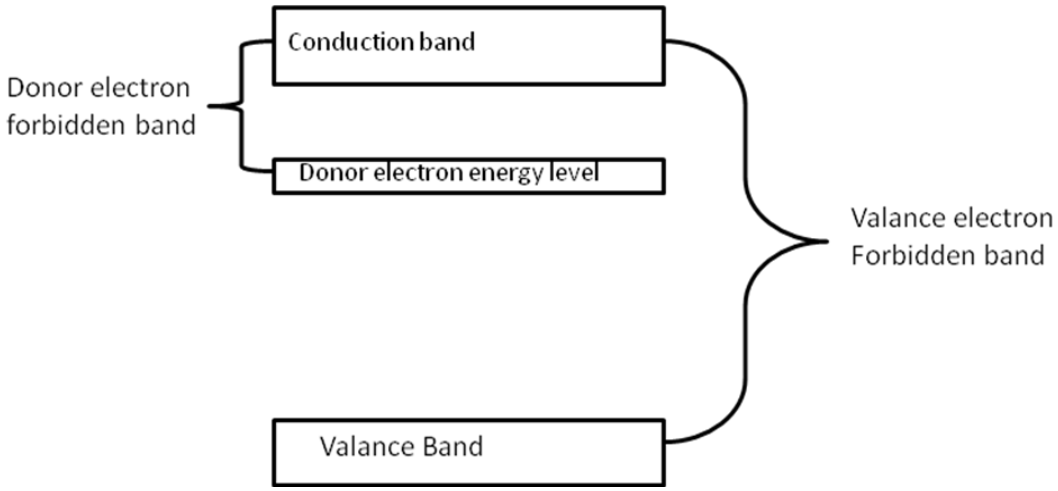



Figure 1.5 Energy band gap of an n- type semiconductor

When a group III element (like B) is added to an intrinsic semiconductor from group IV (like Si), a small proportion of group IV atom is displaced with group III element. However, the boron atom has an insufficient number of bonds to share bonds with the surrounding silicon atoms. One of the Silicon atoms has a vacancy for an electron. It creates a hole that contributes to the conduction process at all temperatures. Doped atoms that create holes in this manner are known as acceptors. This type of extrinsic semiconductor is known as *p-type semiconductors* as it create positive charge carriers Fig. 1.6.

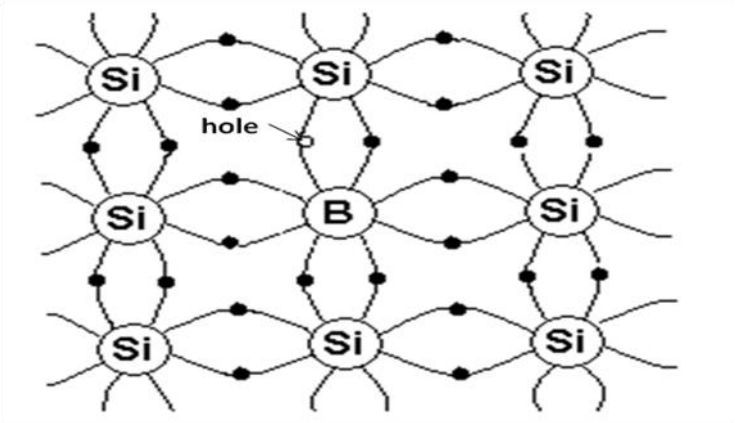



Figure 1.6 p-type semiconductor

In p-type semiconductors the majority of the charge carriers are the holes because of the electron deficiency of the acceptor atom.

The energy band diagram of a p-type semiconductor is also a little different from a pure semiconductor. The acceptor energy band is a little higher than the valance energy band which makes the p-type semiconductors conduct electricity better than pure semiconductors but not as good as n-type semiconductors. [2.c, 9-11].

## 1.4 p-n Junction

When we combine a p-type and n-type semiconductors in a very close contact, the resulting combination is lead to the *p-n junction*. This junction has great importance in the basis of modern semiconductor technology.

n-type semiconductors have high concentrations of free electrons whereas p-type semiconductors have high concentrations of positively charged holes. When these two are brought into contact with each other, some of the free electrons in n-region, which

have reached the conduction band, diffuse into the holes in p-region Fig. 1.7.b. Filling a hole in p-region make a negative ion and leaving in n-region a positive ion. Therefore, a net positive charge in n-region and a net negative charge in p-region are occurred. The resulting junction region then contains practically no mobile charge carriers since positive charge on n-region repels holes to enter from p-type to n-type and negative charge on p-region repels free electrons to move from n-type to p-type , and the fixed charges of the dopant atoms create a potential barrier which inhibits further flow of electrons and holes Fig. 1.7.c. This is called a junction barrier or potential barrier.

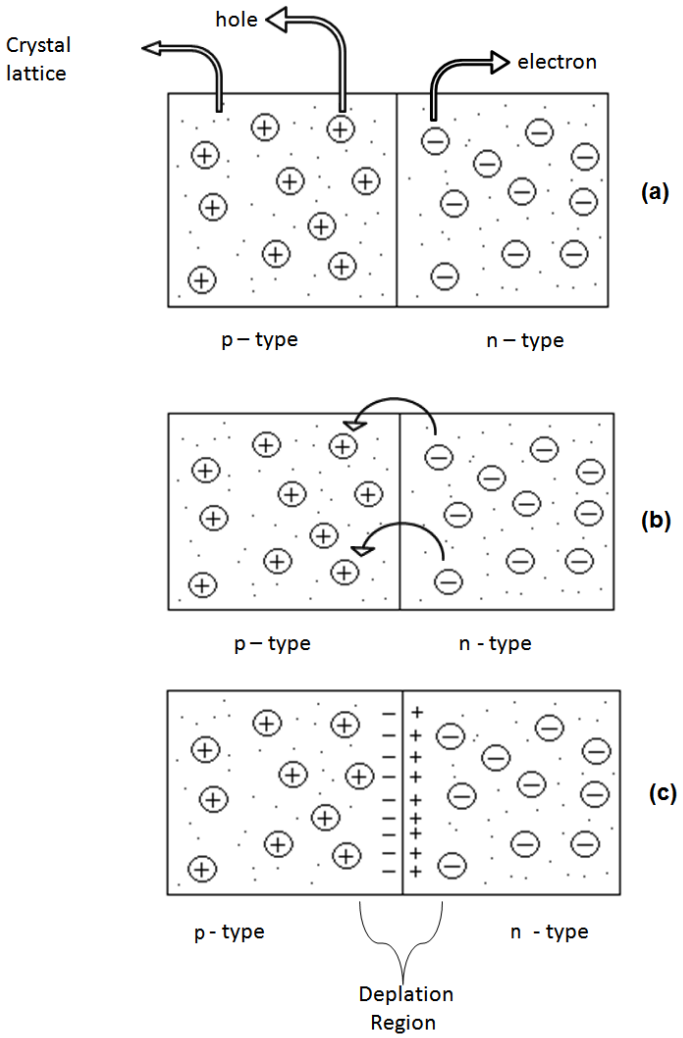


Figure 1.7 (a) p-n junction, (b) diffusion in p-n junction, (c) deplation layer in p-n junction

After the potential barrier formed, the junction has reached equilibrium. Other electrons from the n-region cannot migrate because they are repelled by the negative ions in the p-region and attracted by the positive ions in the n-region. Therefore, with the p-n junction alone, the action stops. To provide the current flow, a battery can be connected to overcome the junction barrier. If the negative terminal of the battery is connected to n-type semiconductor, the negative terminal supplies electrons, which diffuse toward the junction and the positive terminal removes the electrons from p-type semiconductor by creating holes that diffuse toward the junction. This reduces the junction resistance to almost zero and a large current can be produced even for the small potential difference applied. Such a junction is said to be *forward biased* Fig. 1.8.a. If the battery polarity is reversed, there will be very high resistance to current flow and the charge carriers cannot combine at the junction. This type of connection is called *reversed bias* Fig. 1.8.b, [2.d],[3.b].

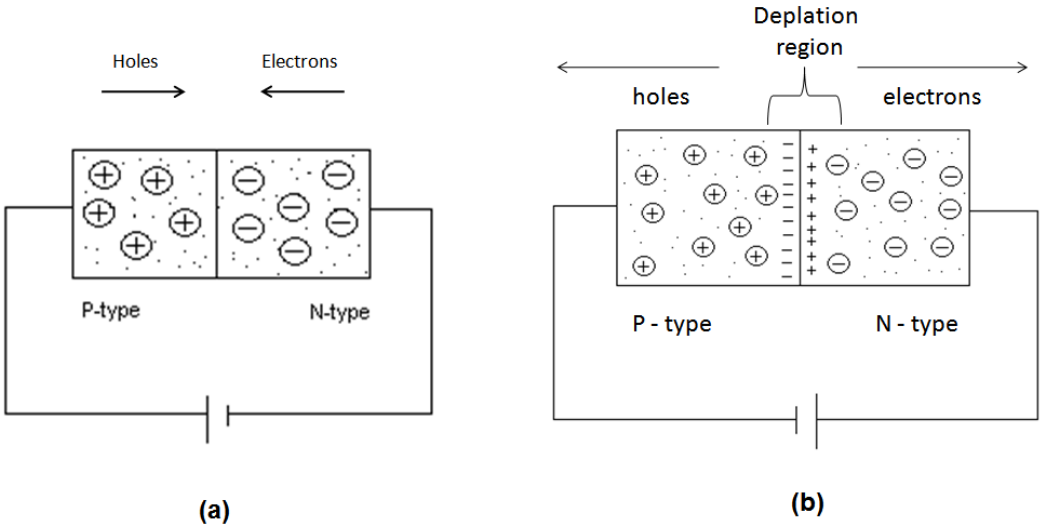



Figure 1.8 (a) Forward biased p-n junction, (b) Reverse biased p-n junction

## 1.5 Nanostructures

Nanotechnology and nanoscience are one of the hottest fields in the last two decades because of their promising applications. The great interest in this field has been started with the famous speech of physicist Richard P. Feynman entitled “There is plenty of room at the bottom” to American Physical Society at Caltech in 1959 [12]. Although Feynman did not mention nanoscience or nanotechnology in his speech, he predicted that materials behave differently in nanoscales and make the people understand the advantages of this brand new field.

The prefix “nano” means one billionth and its origin comes from the Greek word “nanos” which means dwarf [13]. Molecules and structures with at least one dimension roughly between 1 and 100 nm are the main concepts of Nanoscience and these structures can be named as Nanostructures. Nanotechnology is the application of these nanostructures, which are the main promising key building blocks for the construction of nanoscale devices[14].

Scientists have growing interests on nanostructures due to their unique properties and applications since they show different properties compared to their bulk counterparts. For example, in Fig. 1.9 the increase in the number of the publications about nanowires can be seen. Nanostructures offer us large number of opportunities almost in all fields of science and the most successful examples are seen in microelectronics where smaller always means greater performance. When we move to the nanoscales, the surface area to volume ratio increases due to the decrease in the particle size and it is critical to improve the performances of the technologies like batteries and fuel cells [15-17].

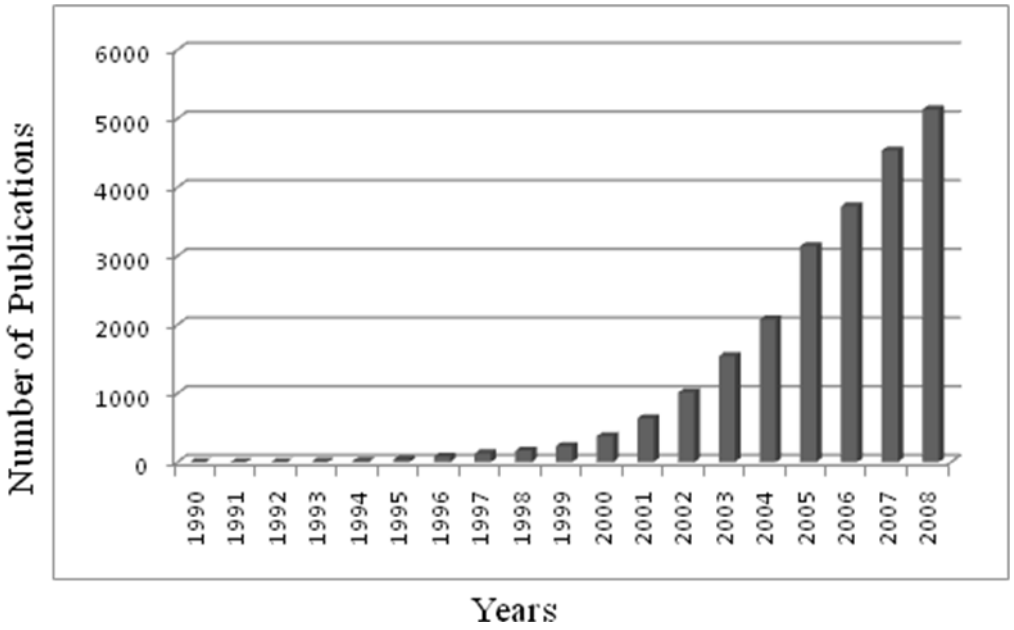



Figure 1.9 Number of publications containing the concept of nanowires by year, determined from CAS Scifinder search

Nanostructures are categorized in four groups considering their dimensions: (i) nanocomposites [3D], (ii) quantum wells [2D], (iii) nanowires and nanotubes [1D], nanoparticles and quantum dots [0D] Fig. 1.10, [18]. These nanostructures have been studied for many years in different fields of technology but in our study we focused on semiconductor nanowires which will be discussed in detail in 1.6.

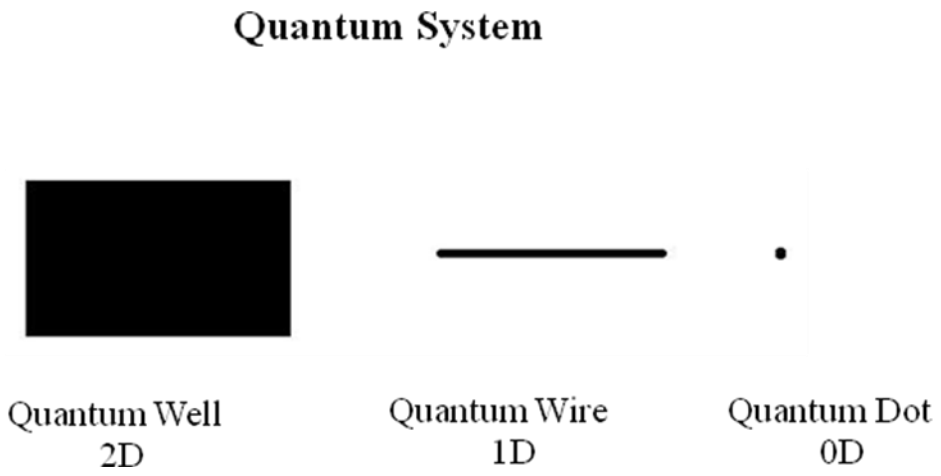



Figure 1.10 Geometrical dimensions of nanostructures

## 1.6 Semiconductor Nanowires

As it is seen in Fig[1.9], in recent years scientists have an increasing interest on nanowires because of their unusual physical properties. It can be said that, the studies of Wagner and Ellis on Si whisker growth at Bell Labs is the starting point of nanowires [19]. In 1970s and 1980s a lot of work was done on the synthesis of different whisker materials. In 1990s with the study of Haraguchi *et al.* on InAs/GaAs based nanowires, a large interest has been started on nanowire concept [20].

Semiconductor nanowires are anisotropic, one dimensional nanocrystals. Generally, their diameters are between 1-200 nm and their lengths could be up to several micrometers. Nanowires show different electronic and optoelectronic properties compared to their bulk counterparts since they have two quantum confined dimensions and one unconfined dimension [21]. Because of the high surface area to volume ratio of the nanowires, majority of the atoms in the nanowire are located on the surface and as a

result of this, the transport of the charge carriers through nanowire is very sensitive to analytes, chemical and biological species that adsorb to the nanowire surface [22-24]. Moreover, nanowires differ from their bulk counterparts due to their increased excitation binding energy, high density of electronic state, diameter depended band-gap enhanced surface scattering of electrons and phonons. Therefore, they show unique magnetic, optical, thermoelectric and chemical properties [25].

## 1.7 Applications of Semiconductor Nanowires

Due to their unique properties, which are described in 1.6, semiconductor nanowires are the potential building blocks for various nanoscale devices like light emitting diodes (LEDs) [26], field effect transistors (FETs) [26], logic gates [27], lasers [28], photodetectors [29], sensors for gases and biomolecules [30] and solar cells [31-32]. Among all of these potential application we are going to focus solar cell applications in this work.

### 1.7.1 Photovoltaics (Solar Cells)

*Photovoltaic* is just a Latin word which is the combination of two words; photo=light and voltaic=electricity. A Photovoltaic cell (Solar cell) is, in principle, a simple semiconductor device that converts light into electric energy by using the radiant energy that comes from the sun. Solar cells can be made from single crystals, crystalline and amorphous semiconductors and they provide us an alternative source of environmental-friendly energy and a solution to the global warming.

The solar cell operation is based on the ability of semiconductors to convert sunlight directly into electricity by exploiting the photovoltaic effect. Basically, when light strikes the cell, a certain portion of it is absorbed within the semiconductor material. This means that the energy of the absorbed light is transferred to the semiconductor. The

energy knocks electrons loose from their atoms, allowing them to flow through the material in a certain direction. This flow of electrons generates a current, and by placing metal contacts on the top and bottom of the PV cell, we can draw that current off to use externally and produce electricity.

The first photovoltaic effect was found by a French physicist Alexandre Edmond Becquerel [33] but the first commercially available solar cell was introduced at Bell Laboratories in 1954 by doping silicon with certain impurities [34]. The first silicon based solar cell had very low efficiency (around 4%) but scientists reported around 25% efficiency solar cells in the passing 50 years [35]. This efficiency value is very close to the theoretical limit (around 31%) for a single junction under sun illumination [36-37]. However, although silicon is the second most abundant element in earth's crust, to produce such efficient bulk Si solar cells are very expensive so the today's commercially available solar cells have 14-17% efficiencies. Since the single junction solar cells do not absorb the significant fraction of the photons in the solar spectrum, their efficiencies are restricted to 31%. The large area, high quality and single junction devices can be categorized as First Generation solar cells. The second generation solar cells based on thin films over various substrates to reduce the material mass, therefore costs and improve the efficiencies. The third generation solar cells aim to enhance poor electrical performance of second generation and single junction devices and they consist of multi-junction nanowire and organic dye solar cells [38]. And this work deals with semiconductor nanowire materials which could be used in third generation solar cells.

Alivisatos and his co-workers achieved to produce the first nanowire solar cell in 2002 in which CdSe nanowires were used as the electronic conducting layer of a hole conducting polymer matrix solar cell [39]. Although scientists have worked a lot to produce a high efficiency nanowire solar cell, a commercially available nanowire solar cell is not available yet. However, it is expected that nanowire solar cells have better efficiencies than the commercially available solar cells since nanowire solar cells offer

us some advantages. First, the optical path in a nanowire solar cell is longer than the one in the first and second generation solar cells due to scattering. As a result of this, the optical absorption increases significantly. Second, the path in nanowires, which the charge carriers (electrons and holes) need to travel, is a much shorter path so that the performance of the cell can be improved. Third, since the size of the nanowire is important to decide the energy band gap, by changing the sizes the energy band gaps can be adjusted. Therefore, better absorber and window layers can be designed [40-42].

## 1.8 Fabrication Techniques of Semiconductor Nanowires

### 1.8.1 Template Based Synthesis

The template based nanowire synthesis is increasingly being employed by the fabrication of nanowires. In this technique, pores of the template serves as a scaffold and by filling of the pores with specific materials, they take the exact shape of the hosting pores. Self-ordered nanoporous membrane, track etched polymer, nano-channel array glass, radiation track-etched mica and anodic aluminium oxide (AAO) are the basic templates used in template based synthesis method. Performing annealing treatments without losing crystallinity and ability of making single nanoscale heterojunctions inside the pores are two main advantages of using an insulating template in nanowire synthesis. Besides nanowires, nanotubes and nanofibers can also be synthesized by this methodology.

AAO is the most functional one when compared with other template types because of the regular pore distribution, high pore density and high aspect ratio of pores. AAO templates can easily be prepared by electrochemical anodization of pure aluminium metal in which oxidation takes place in an electrolyte solution. By changing the anodization parameters like anodization voltage, current, bath temperature and

composition, the desired length, size and diameter of the pores can be obtained during the fabrication of AAO.

In summary, template based synthesis method provide us to fabricate uniform nanowires which are vertically directed at almost identical distance from each other and to control the sizes of the nanowires by changing the sizes of the pores in the membrane [43-46].

Nanowires can be fabricated in the pores of the templates by different deposition methods such as electrodeposition [47], solution-liquid-solid (SLS) method [48], vapor-liquid-solid [49] growth, laser ablation [50] and thermal evaporation [51]. Among all of these growth techniques we choosed electrodeposition method to fabricate nanaowires and it will be discussed in 1.8.2 in details.

### 1.8.2 Selected Growth Technique: Electrodeposition

When electrodeposition is compared with the other growth techniques mentioned above, it is obvious that electrodeposition is the most attractive one because of its simplicity, low cost, scalability and manufacturability. At industrial level, electrodeposition is a widely used method for depositing metals and metallic alloys with a wide range of applications. Therefore electrodeposition of semiconductor materials is a hot subject nowadays, not only from academic point of view, but also industrial point of view since it offers large area, cost effective and low temperature production possibilities.

Semiconductor nanowires can also be grown by this method in the pores of the used templates (self-ordered nanoporous membrane, track etched polymer, nano-channel array glass, radiation track-etched mica and AAO). Nanowires, produced in the pores of the templates by electrodeposition, are mechanically stable therefore they are easy to handle.

Simply, the electrodeposition technique is based on applying potential to an electrolyte solution, which maintains the flow of current. The system also includes a substrate as a

working electrode, a counter electrode and a reference electrode. By the application of the potential to the electrolyte solution, a current flow occurs inside the solution and the cations and anions in the solution start to move towards cathode and anode. Electrodeposition can proceed cathodically and anodically. As a result of this movement, charge transfer reaction and deposition on the substrate takes place. The surface of the substrate must have an electrically conducting coating otherwise the reaction will fail. The conducting coating on the substrate should be uniform to provide a homogeneous deposition of the material. Moreover, the substrate should be stable in the electrolyte solution and the surface of the solution should be clean. The experimental conditions (temperature, deposition potential, deposition time etc.) are also important features to have an effective deposition.

## 1.9 Aim of the Work

The aim of this work is to synthesize CdS, CdTe, polypyrrole nanowires and heterojunctions of CdS\CdTe, CdS\polypyrrole nanowires by using anodic aluminium oxide (AAO) as an template. Electrodeposition method was selected to synthesize these nanowires since it is a cost effective and low temperature technique. Chemical, physical and electrical properties of the nanowires was investigated by several characterization methods.

CdS and CdTe are two of the promising materials which could be used in photovoltaic applications. First of all, they are cheaper than photovoltaic applications based on silicon technology. Nanowires are in the class of third generation solar cells and the promising properties of nanowires, which are disscused before, give hopes to improve more efficient solar cells. The nanowires of CdS and CdTe are one of the best candidates to make efficient solar cells since n-CdS and p-CdTe have good electrical and junction properties which are necessary for a high efficient solar cells. There are lots of research groups all around the world working on this subject but a commercial nanowire solar

cell has not been avaliable yet. Therefore one of the aim of this work is to synthesize and chracterize CdS and CdTe nanowires and heterojunction of CdS\CdTe nanowires that could be used in photovoltaic applications.

Another aim of this project is also to synthesize polypyrrole nanowires and study polypyrrole\CdS nanowire heterojunction to investigate the chemical, physical and electrical properties of an inorganic and organic nanowire.

Commercially avaliable AAO was used as a template since it is cheap and well suited to our objectives. One face of AAO membrane was coated with gold by sputtering method since a conductive surface is needed for electrodeposition of the nanowires. The nanowires was grown in the pores of the AAO membrane. The detailed information about the membrane and growth conditions of the nanowires will be given in the experimental part.

Morphological properties and chemical compositions of the nanowires were investigated by Scanning Electron Microscope (SEM) and Energy Dispersive X-Ray Spectroscopy (EDAX) respectively, crystal structure was determined by X-Ray Diffraction (XRD), band gap, transmittance and absorption values were obtained by UV-Vis Spectroscopy and photoelectrochemical (PEC) properties was examined by potentiostat via Linear Sweep Voltammetry method.

# CHAPTER 2

# EXPERIMENTAL

## 2.1 CdS

CdS is a II-IV group semiconductor compound which is transparent in visible region with 2.42 eV band gap value so it is vital in optoelectronic applications (solar cells, light emitting diodes, etc.) [52]. CdS is used in solar cells as a window layer and it is almost transparent around 510 nm. Therefore it permits the sun light to penetrate into the absorber layer of a solar cell and gives rise to produce a current through the solar cell. In this study n-type CdS was synthesized and when it makes a heterojunction with a p-type semiconductor (CdTe, polypyrrole), it forms the core component of an solar cell. High quality of CdTe can be deposited on top of CdS which leads to heterojunction of n-type CdS and p-type CdTe.

In nature, CdS has two crystal forms; hexagonal wurtzite structure and cubic zinc blend structure [53]. The band gap and transmittance values and crystal structure of CdS synthesized in this study will be discussed in details in later chapters.

Deposition technique is a key factor to have good p-n junction since the properties of junction depends on the quality of the interaction between n-type semiconductor and p-type semiconductor. CdS can be deposited by chemical bath deposition (CBD) [54], close space sublimation (CSS) [55], sputtering [56], high vacuum thermal evaporation [57] and electrodeposition [58].

### 2.1.1 Electrodeposition of CdS Nanowires

In CdS nanowire deposition, gold coated porous AAO membrane was used as the substrate. The solution contains 0.055 M $CdCl_2$, 0.19 M elemental sulfur and DMSO as solvent [59]. The solution temperature was kept at 125 °C and two different deposition voltage 30 V and 20 V DC was sustained as deposition voltages. A platinum cage was used as counter electrode and gold coated AAO membrane was used as working electrode. Nitrogen flow was maintained during deposition to prevent excess $CdSO_4$ formation and after deposition of CdS was finished, the samples were washed with DMSO to remove excess sulfur from the surface. The deposition was performed at three different time ranges (10 min., 20 min. and 30 min.) to see the time effect on the sizes of CdS nanowires. Annealing at 100 °C and 250 °C was carried out for 30 minutes to investigate the changes of average resistances of CdS nanowires deposited on different voltages and times.

The porous AAO membrane used as the substrate is a commercially available Whatman membrane Fig. 2.1. The average diameter of the pores is about 20 nm and the average height of the membrane is about 60 μm. One face of this membrane was coated with gold by sputtering method to get a conductive surface which is necessary for electrodeposition method. The thickness of coated gold was about 20 nm.

The CdS nanowires (Fig. 2.2) was grown inside the pores of the AAO membrane with the experimental conditions mentioned above. Since the sizes of the nanowires are very small, the gold coated surface of the membrane was coated with commercially available epoxy to make morpogological and structural characterizations and the membrane was dissolved in 2 M NaOH solution so that the nanowires was obtained sticked on the surface of epoxy.

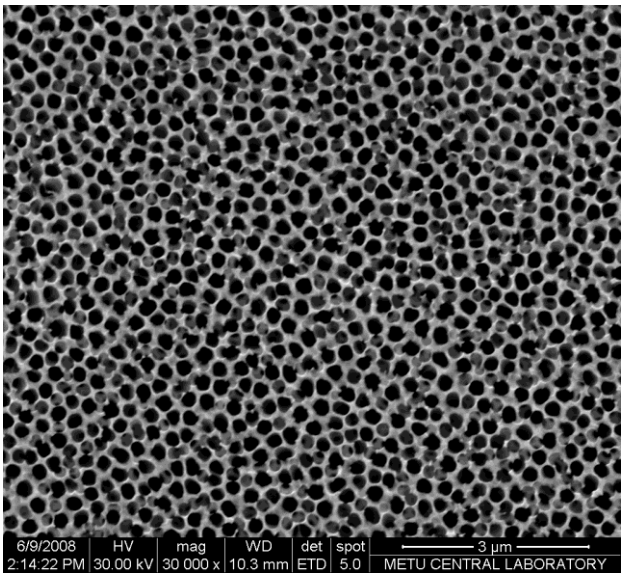



Figure 2.1 Scanning Electron Microscope (SEM) image of Whatman AAO membrane (average diameter→ 20 nm, average height→ 60 µm)

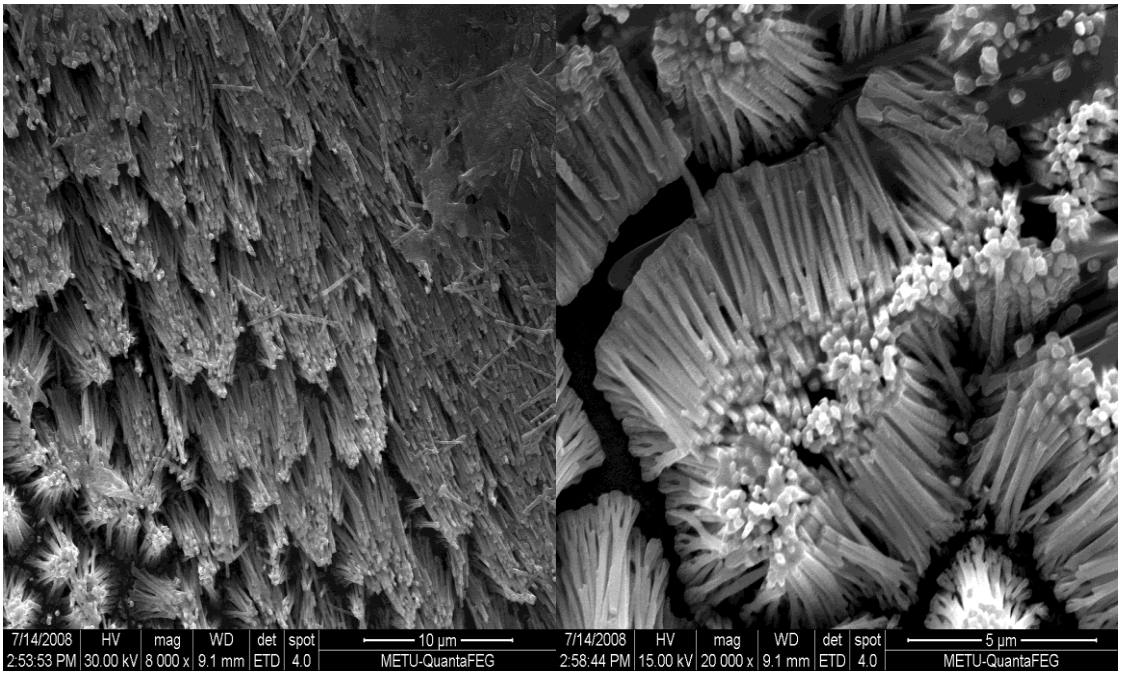



Figure 2.2 SEM images of CdS nanowires produced at 30 V 30 min 125 °C

## 2.2 CdTe

CdTe, with a band gap value of 1.44 eV, is one of the most suitable materials for optoelectronic applications [60-62]. It is used as an absorber layer in photovoltaic applications and p-type CdTe forms the p-part of a p-n junction solar cell. The bad gap value of CdTe (1.44 eV) is very close to theoretically calculated optmum value for solar cells that's why CdTe is one of the most studied semiconductor compound in solar cell application over various substrates [63-65].

CdTe is a good absorber layer in solar cells since it has a high absorption coefficient, so that approximately 99% of the incident light is absorbed. CdTe solar cells are stable under proton, electron and UV irradiation, and under strong temperature changes, therefore suitable for space applications. Moreover, the possibility of deposition of high quality of CdTe on top of CdS leads to heterojunction of n-type CdS and p-type CdTe. Low cost materials can be used as a substrate during fabrication.

From the structural and morphological studies [66,67], it was seen that CdTe has cubic and hexagonal structures. The crystal structure of CdTe depends on the deposition rate and temperature and annealing as a post treatment has an influence on the electrical properties due to the changes in crystal structure [68].

CdTe can be deposited various ways like chemical vapor deposition (CVD) [69], sputtering [70], vacuum evaporation [71], close spaced sublimation (CSS) [72], screen printing [73], molecular beam epitaxy [74] and electrodeposition [75-76]. In this study electrodeposition method was selected since it is a low cost method and easy to control. The detailed information about the experimental conditions of electrodeposition of CdTe nanowires will be given in chapter 2.2.1.

### 2.2.1 Electrodeposition of CdTe nanoclusters

CdTe has been deposited by using 0.1M $CdSO_4$ and 150 ppm $TeO_2$ and ultra pure water as solvent at room temperature and pH=3 over gold coated AAO membrane. The

deposition voltage was kept -0.58 V and Ag/AgCl electrode was used as reference electrode and Graphite rode was used as counter electrode.

## 2.3 Electrodeposition of Polypyrrole Nanowires

Polypyrrole nanowires were synthesized via electropolymerization technique by using 0.1 M $LiClO_4$, 0.01 M pyrole, and $7x10^{-4}$ M sodium dodecylsulfate at room temperature. During synthesis, potential was swept between 0 and 0.85 V at a scan rate of 400 mV/s for various number of scans (100, 400 and 800 scans). The system was three electrodes one compartment system in which silver wire as reference electrode, platinum as a counter electrode and gold coated AAO membrane as working electrode were used.

## 2.4 CdS\CdTe Heterojunction

First CdS nanowires were deposited onto gold coated AAO membrane. The solution contains 0.055 M $CdCl_2$, 0.19 M elementl sulfur and DMSO as solvent. The solution temperature was kept at 125 °C and 30 V DC was sustained as deposition voltage. A platinum cage was used as counter electrode and gold coated AAO membrane was used as working electrode. Nitrogen flow was maintained during deposition to prevent excess $CdSO_4$ formation and after deposition of CdS was finished, the samples were washed with DMSO to remove excess sulfur from the surface. The deposition was performed at two different time ranges (10 min.and 30 min.).

After CdS formation, in order to form CdS/CdTe heterojunction nanostructure, CdTe nanoclusters have been electrochemically deposited on CdS nanowires. For this process, AAO templates with CdS nanowires have been used as working electrode and CdTe formation was carried out by electrodeposition. CdS nanowire deposited AAO sample was immersed into a solution containing 0.1M $CdSO_4$ and 150 ppm $TeO_2$ and ultra pure

water as solvent at room temperature and pH=3. The deposition voltage was kept -0.58 V for three different deposition time ranges and Ag/AgCl electrode was used as reference electrode and graphite rode was used as counter electrode.

## 2.5 CdS\Polypyrrole Heterojunction

First CdS nanowires were deposited onto gold coated AAO membrane. The solution contains 0.055 M $CdCl_2$, 0.19 M elemental sulfur and DMSO as solvent. The solution temperature was kept at 125 °C and 30 V DC was sustained as deposition voltage. A platinum cage was used as counter electrode and gold coated AAO membrane was used as working electrode. Nitrogen flow was maintained during deposition to prevent excess $CdSO_4$ formation and after deposition of CdS was finished, the samples were washed with DMSO to remove excess sulfur from the surface. The deposition was performed at two different time ranges (10 min.and 30 min.).

After CdS formation, in order to form CdS/Polypyrrole (PPy) heterojunction nanostructure, PPy nanowires have been electrochemically deposited on CdS nanowires. For this process, AAO templates with CdS nanowires have been used as working electrode and PPy formation was carried out by electropolymerization. CdS nanowire deposited AAO sample was immersed into a solution containing 0.1 M $LiClO_4$, 0.01 M pyrrole, and $7x10^{-4}$ M sodium dodecylsulfate. During synthesize, potential was swept between 0 and 0.85 V at a scan rate of 400 mV/s for various number of scans (100, 400, 800 scans).

## 2.6 Instrumentation

### 2.6.1 Scanning Electron Microscope (SEM)

SEM was used in order to collect images from the samples' surface for morphological studies. Samples were divided into small pieces with around 1 $cm^2$ surface area. Sample surfaces were coated with an ultrathin layer of gold/palladium alloy in order to enhance the electrical conductivity and improve resolution. Analysis was done in METU Central Laboratory and the equipment used was a QUANTA 400F Field Emission Scanning Electron Microscope with 1.2 nm resolution.

### 2.6.2 Energy Dispersive X-Ray Spectroscopy (EDX)

Chemical characterization and elemental analysis of the films were obtained from EDX which is connected to the QUANTA 400F Field Emission Scanning Electron Microscope.

### 2.6.3 X-Ray Diffraction (XRD)

Crystal structures and grain sizes of the films were determined by Rigaku Miniflex X-ray diffraction system equipped with Cu Kα radiation.

### 2.6.4 UV-Vis Spectroscopy

The transmission spectra of the samples were measured by a Pharmicia LKB Ultraspec III UV-VIS spectrophotometer over the wavelength range of 325-900 nm at room temperature.

### 2.6.5 FTIR Spectroscopy

The IR spectra of the samples were measured by Perkin Elmer Spectrum 100 FTIR Spectrometer at room temperature.

### 2.6.6 Potentiostat

Electrodeposition of CdTe and PPy thin films and PEC characterizations were carried out with a Gamry G750 Potentiostat/Galvanostat/ZRA system placed into a computer with a hardware operator. Potentiostat's main duty in this work is to maintain the working electrode at a specific potential with respect to the reference electrode during electrodeposition. Saturated Calomel Electrode (SCE) and Silver/Silver Chloride (Ag/AgCl) electrodes are the most used type of reference electrodes. Graphite and silver foil are used as counter electrode during electrodeposition.

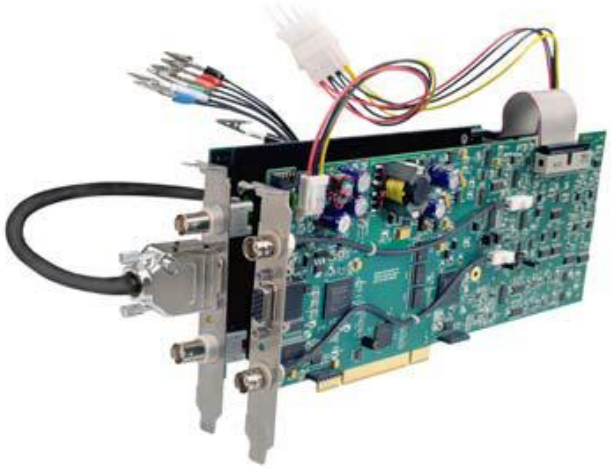


Figure 2.3 Gamry G750 Potentiostat/Galvanostat/ZRA system as a hardware integrated with a computer

# CHAPTER 3

# RESULT AND DISCUSSION

## 3.1 CdS Nanowires

Template synthesis is one of the most successful methods to obtain nanowires (NW) with controlled properties [77, 78]. Anodic aluminum oxide (AAO) templates have been extensively used to synthesize self-aligned photoelectric, magnetic and catalytic nanowires [79-81]. Template synthesis of CdS-NWs is being investigated for many applications, such as photovoltaic cells [82], transistors [83] and photocatalytic hydrogen production [84]. Thermal evaporation [85], chemical vapor deposition [86] and electrochemical deposition [87] techniques are the most commonly used methods for template synthesis of CdS-NWs. Among these methods thermal evaporation and chemical vapor deposition need specific tools. Hence, the manufacturing cost is high. On the other hand, it is possible to deposit nanowires in a relatively simple and cost effective way using dc-electrochemical method. Mo D et al. [87] and Yang Y et al. [88] used ion-track and AAO-Au/Si templates to synthesize CdS-NWs via dc-electrochemical technique. Mondal SP et al. [89] reported the structural and optical properties of dc-electrochemically deposited CdS-NWs. However, according to our best knowledge, this is the first report combining the morphological, structural and photoelectrochemical behavior of dc-electrodeposited CdS-NWs.

In this study, after deposition of CdS-NWs [89], for XRD, PEC and electrical measurement, films were allowed to dry under ambient conditions. For SEM and EDX

measurements templates were dissolved in 2 M NaOH solution after coating one side with epoxy. PEC cell configuration has been formed with CdS-NWs as working electrode into a three-electrode in one compartment cell, with a graphite counter electrode and Ag/AgCl reference electrode. Electrical response of the CdS-NWs under illumination ($35mW/cm^2$) has been recorded using a Gamry G750 Potentiostat/Galvanostat/ZRA system. 0.1M $Na_2S$, 0.1M NaOH and 0.1M S solution has been used as electrolyte. Room temperature electrical conductivity of the nanowires has been performed using a Keithley 2400 I-V source-measure unit. For this purpose, samples with ~25 $mm^2$ area were prepared and silver paste contacts were transferred on both sides of the membranes. This structure made it possible to measure the electrical conductivity through the nanowires.

Deposition temperature, applied voltage and the deposition time are the key factors affecting the CdS nanowire formation. It has been observed that for the temperature lower than 100 °C, the solubility of the elemental sulphur was very poor, and therefore, there has been no material deposition. For high temperatures (>130°C) we obtained loss of electrical contact. Basically, in an electrochemical nanowire formation charged reactive species in the solution diffuse through the pores of the template and reach to the electrode surface by means of an applied electric field. Electrochemical formation of CdS nanowire can be considered in two steps. When an electric field applied, $Cd^{2+}$ ions enter to the pores of template, at cathode reduction of $S^{2-}$ ion occurs and $S^{2-}$ reacts with $Cd^{2+}$, which enters into the pores by the diffusion process, to form CdS [90]. Nucleation and growth process of CdS nanowire occurs in the pores of template. Hence, the pore size, density and wettability affect the morphology of nanowire. In this study, AAO membrane (Whatman, Anodics 47) is used as template, due to its high thermal and chemical stability. The average pore size of the AAO membrane used here is 0.02 μm.

SEM analysis has been performed to investigate the CdS nanowire formation and effect of the process conditions on morphology. As can be seen in Figure 3.1 (a) and (b), CdS nanowires deposited for 10 minute are much shorter than the nanowires deposited for 30 min. It has also been determined that diameter of the CdS nanowires deposited for 10

min is smaller than the diameter of the nanowires deposited for 30 min. The diameter of the nanowires produced for 10 min is about 100 nm. On the other hand, the diameter and the length of the nanowires produced for 30 min reached 200 nm and 4 μm, respectively. Hence, more possibly, nucleation of the CdS nanowires starts on the bottom of the AAO membrane pore instead of the pore wall. Then nanowire formation may occur on top of this seed layer in both upward and sideward dimensions. Figure 3.1 (c) shows the CdS nanostructures deposited at 125 °C, 20 V and 30 min. Compare to the nanowires deposited at the same temperature and the time, but higher voltages, there is a significant change in morphology. CdS nanowires with very small length and the diameter have been observed in this case. Also, nanowires showed a tendency to coalesce. The most probably the applied electric field was not enough to nucleate CdS, which can fill the whole pore. Instead, a few separate CdS seed formed at the bottom. Therefore, at the beginning very small nanowire deposition has occurred, after a critical material deposition obtained these separate nanowires coalesced. Finally, we investigated the effect of temperature on CdS nanowire morphology. For the temperatures higher than 130 °C, we had some problems with metal layer coated on one side of AAO membrane. Hence, the nanowire formation failed at these temperatures. This can be solved by increasing the thickness of the metal layer by further material deposition. As mentioned earlier, for the temperature lower than 90 °C, CdS nanowire formation failed again probably due to the solubility problem. As can be seen in Figure 3.1 (d), CdS nanowires successfully formed at 100 °C at 30 V DC.

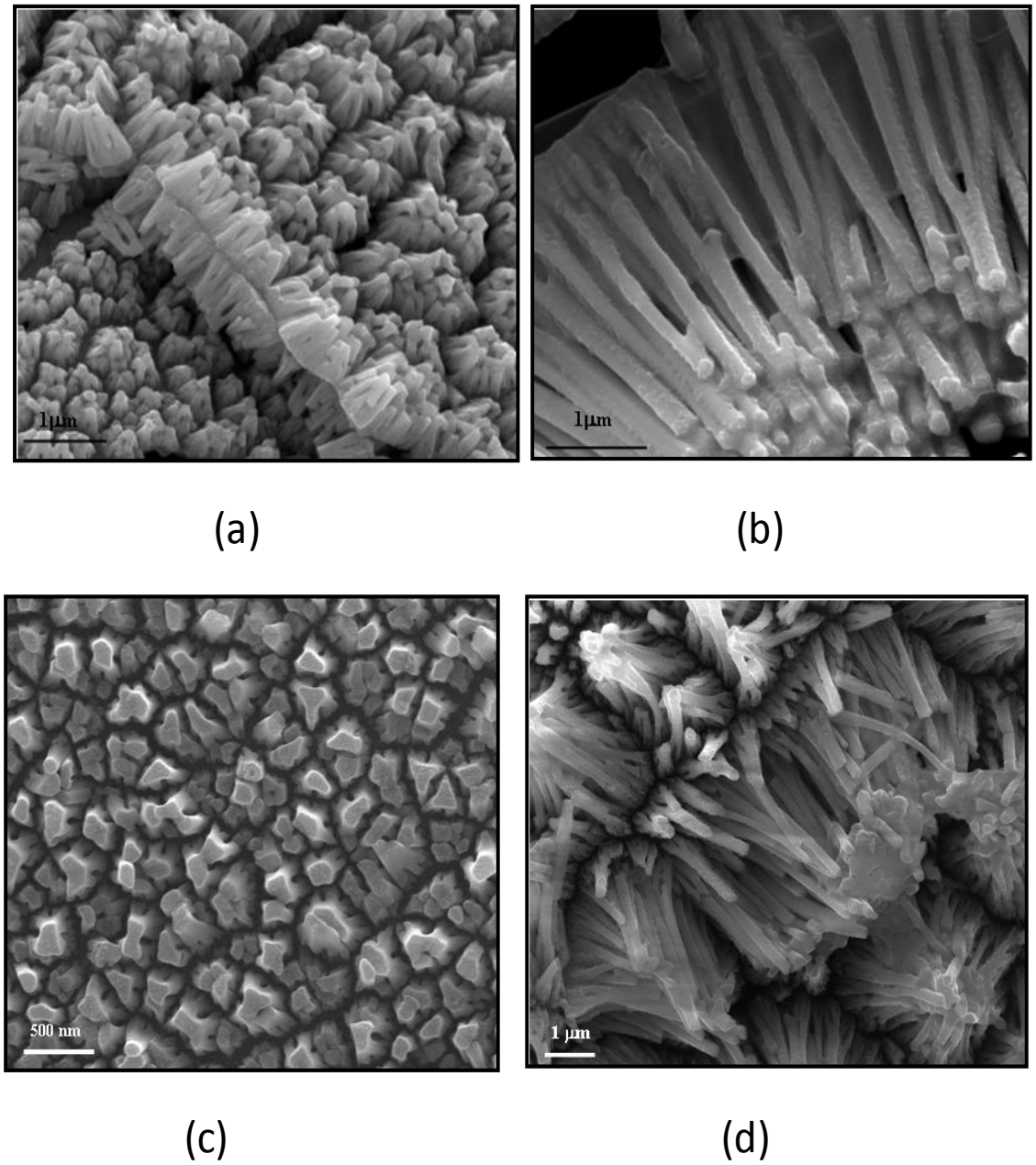



Figure 3.1 SEM images of CdS nanowires grown at 125°C, 30 V **(a)** 10 min **(b)** 30 min. **(c)** 20V 30 min. **(d)** at 100°C 30 V 30 min.

X-ray diffraction analysis (Fig. 3.2) showed that all the samples have a peak around 26° (2θ). Other minor peaks came from gold coated AAO template. Fig. 3.2 also shows that XRD patterns of nanowires synthesized at 30 V is sharper than that of 20 V, indicating the increase in crystal structure with increase in voltage. EDX results also revealed that nanowires composed of Cd and S (Fig. 3.3). There has been an increase in both Cd and S atomic ratio with increasing the voltage. This supports the more material deposition shown in Figure 3.1. The atomic weight percent of Cd and S of the sample deposited at 125 °C, 30 V, 30 min was 20 and 18% mol, respectively.

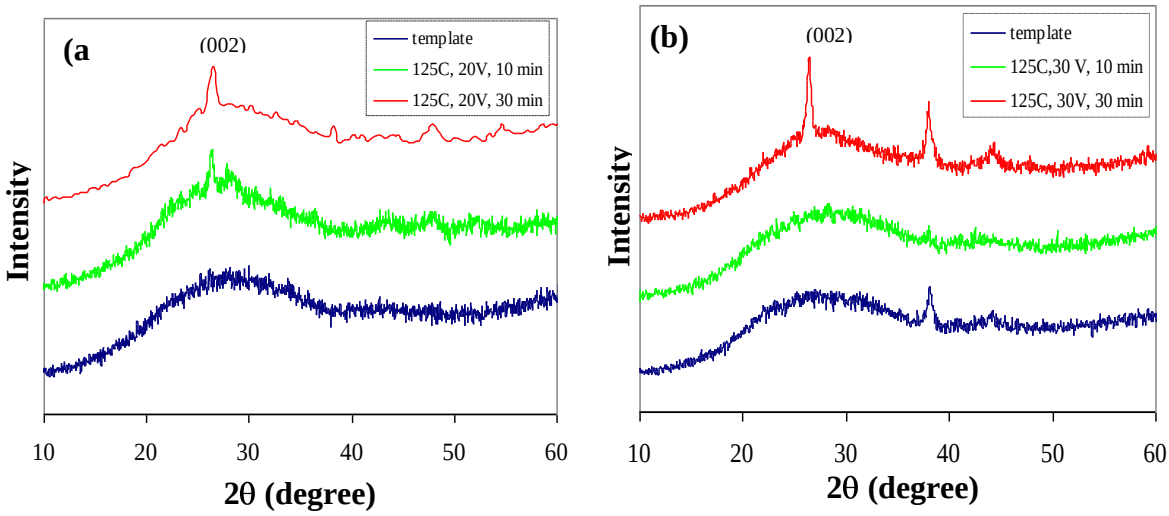



Figure 3.2. X-ray diffraction patterns of CdS-NWs deposited at **(a)** 20V and **(b)** 30V

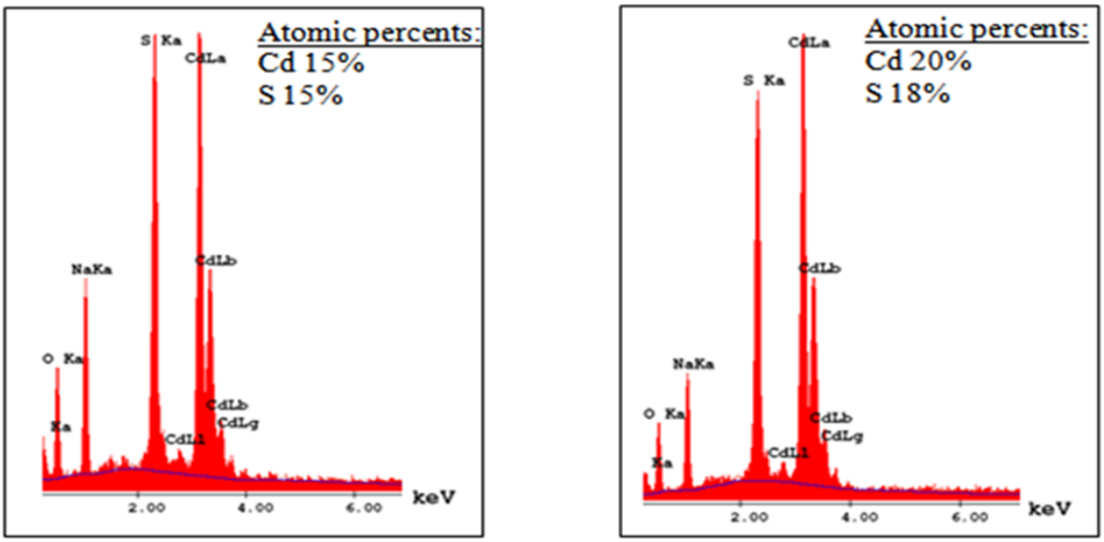



Figure 3.3 EDX results of CdS nanowires grown at 125°C 30 V **(a)** 10 min. **(b)** 30 min.

In Fig. 3.4 the transmittance data of CdS nanowires produced at different voltages and different time ranges can be seen. The transmittance values of CdS nanowires fits in the visible range which is around 500-900 nm and its maximum transmittance is about 40% around 900 nm. Since CdS is used as the window material in photovoltaic applications, it should have transmittance values above 70% at least. However CdS nanowires were taken into the epoxy surface to analyze them in SEM so epoxy decreased the transmittance values of CdS nanowires since it is not completely transparent. It has its own color yellowish color. Therefore the transmittance values are lower than expected.

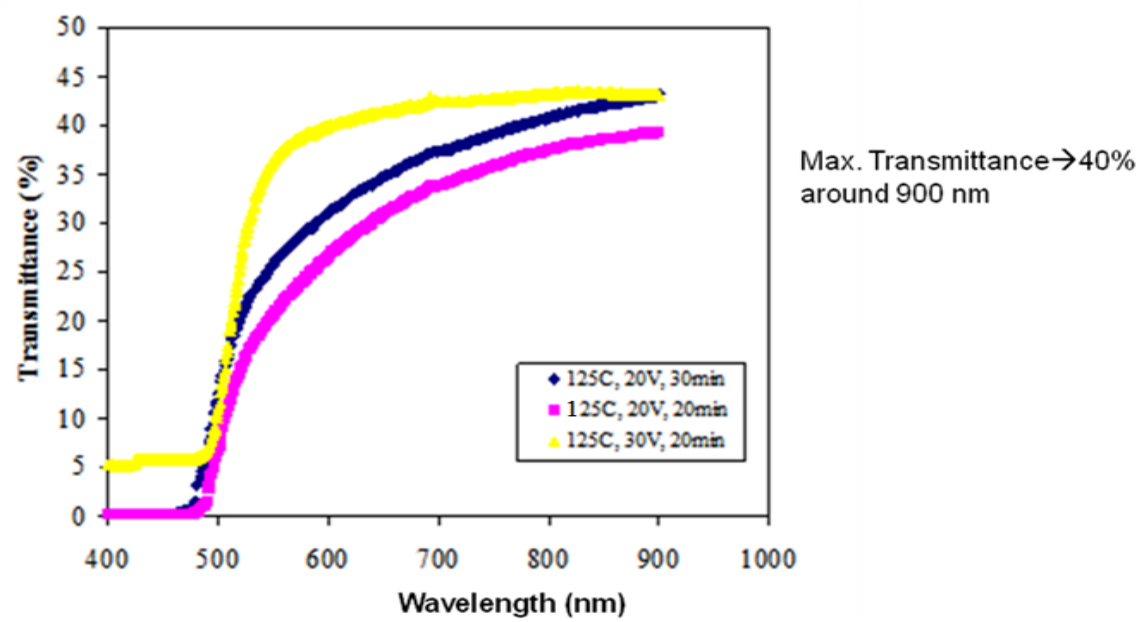



Figure 3.4 Transmittance values of CdS nanowires produced at different voltages and time ranges

The optical band gap energy $E_g$ was calculated from the following variation of the absorption coefficient ($\alpha$) with photon energy;

$$(\alpha h\nu) = A(h\nu - E_g)^n \qquad (1)$$

where $A$ is a constant, and $n$ is the power exponent, which takes 1/2 value for direct allowed transition and 2 for indirect allowed transition. As seen in Fig. 3.5, for all samples, the change of $(\alpha h\nu)^2$ versus photon energy $h\nu$ with $n$=1/2 have very good linearity indicating that the optical transition in CdS-NWs is direct allowed transition. The extrapolation of the straight line of $(\alpha h\nu)^2$ versus photon energy allows us to obtain

the band gap energy values. Band gap energy data of CdS-NWs ranges between 2.48 and 2.40 eV depending on the production conditions.

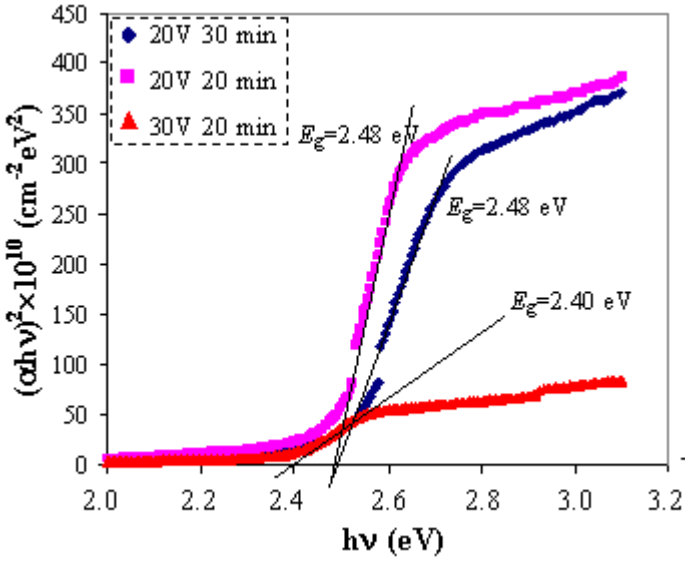



Figure 3.5 $(\alpha h\nu)^2$ versus photon energy $h\nu$ plot of CdS nanowires

A Photoelectrochemical cell (PEC) is a solar cell in which current and voltage are produced at the same time upon absorption of light by one or more electrodes. Usually a semiconductor electrode is used as working electrodes. Our PEC configuration is a three electrode one compartment system in which graphite was used as counter electrode, Ag/AgCl was used as reference electrode and our substrates (CdS, Polypyrrole(PPy), CdS-PPy, CdS-CdTe nanowires) was used as working electrode. Figure 3.6 shows the schematic representation of the three electrode one compartment cell used for photoelectrochemical measurements. Electrical response of the CdS, PPy, CdS-PPy, CdS-CdTe nanowires under constant illumination (35 mW/cm$^2$) has been recorded using

a Gamry G750 Potentiostat/Galvanostat/ZRA system. 0.1M $Na_2S$, 0.1M NaOH and 0.1M S solution has been used as electrolyte.

CdS is among the most promising candidates for PEC applications with its proper band-edge positions for reduction/oxidation of water, high optical absorption and ease of manufacturing techniques [91, 92]. Although, there are some studies of PEC characterization of CdS thin films [93, 94], there are very limited information about CdS nanowires integrated into PEC cell [95]. According to our best knowledge, the maximum reported power conversion efficiency and fill factor of CdS thin film PEC cell is 1.3 and 42 %, respectively [96]. Jang et al. have reported the solvothermally synthesized CdS nanowires with 3.0 $mA/cm^2$ photocurrent density at 0 V potential versus Ag/AgCl and 6 μmol/h hydrogen evolution rate in 0.1M $Na_2S$ + 0.02 M $Na_2SO_3$ electrolyte solution [97]. Also, Dongre et al. have been reported the improvement of the junction ideality factor by replacing the CdS nanoparticles with nanowires in PEC cell [98]. Nevertheless, there has been no report on the CdS/organic hybrid hetero-nano structures for PEC applications. The PEC applications of CdS/Polypyrrole hybrid hetere-nano structures will be investigated in detail in 3.2.

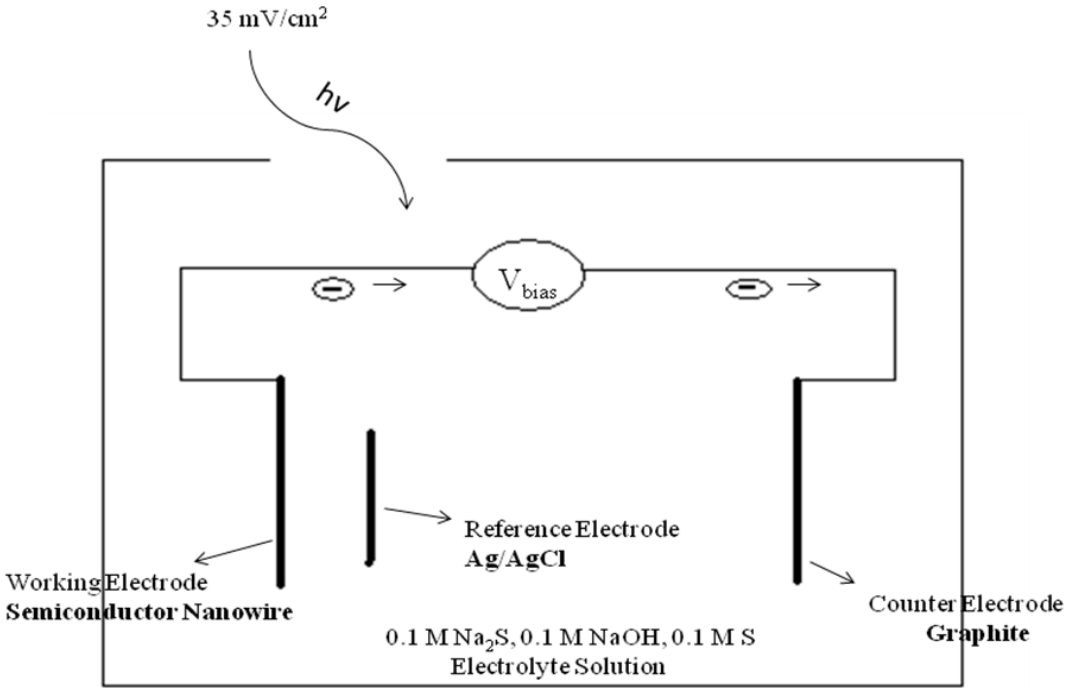



Figure 3.6 Schematic representation of Photoelectrochemical Cell

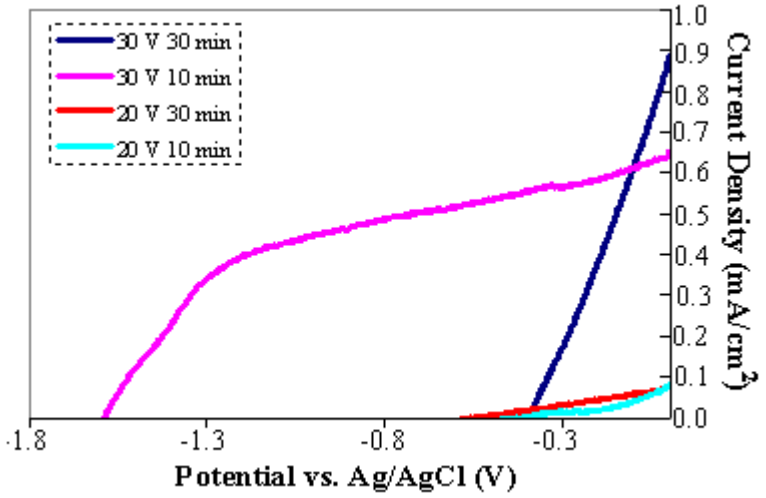



Figure 3.7 Current density-Voltage characteristic of CdS-NWs

Fig. 3.7 shows the current density versus potential graphs for CdS nanowires under illumination. Fill factor (*FF*) of the samples were calculated using the very well known equation;

$$FF(\%) = \frac{I_{\max} V_{\max}}{I_{sc} V_{oc}} x100 \qquad (2)$$

where, $I_{max}$ and $V_{max}$ is maximum current and voltage respectively, $I_{sc}$ is the short circuit current, and $V_{oc}$ is the open circuit potential. Another identifying factor for the PEC solar cell is the power efficiency, which is equal to the percentage of the power converted from the absorbed light to the electricity. Hence, power efficiency ($\eta$) can be calculated from;

$$\eta(\%) = \frac{I_{\max} V_{\max}}{P_i A} \qquad (3)$$

where, $P_i$ is the power of incident light and $A$ is the area of the electrode. As can be seen in Figure 3.7, CdS nanowires deposited at 30 V has much higher $I_{sc}$ compare to that of nanowires deposited at 20 V. This result is consistent with SEM, UV-vis and X-ray analyses. These analyses showed that 30 V deposition voltage resulted more homogenous and well distributed nanowires with better crystalline structure compare to the 20 V. Figure 3.7 also shows that $V_{oc}$ of the CdS deposited at 30 V for10 min is approximately 3 times higher than that of nanowires deposited at 30 V for 30 min. Basically, the open circuit potential for nanowire cell depends on the photocurrent density across the junction area and can be written as [99, 100];

$$V_{oc} = \left(\frac{kT}{q}\right) \ln\left(\frac{J_{sc}}{\gamma J_0}\right) \qquad (4)$$

where $k$ is the Boltzmann's constant, $T$ is the temperature, $q$ is the elementary charge, $J_0$ is the reverse saturation current density over the actual junction area, $J_{sc}$ is the short-circuit current density per unit of projected device area, and $\gamma$ is the ratio of the junction area for a nanowire electrode to a planar electrode, which is given by;

$$\gamma = \frac{A_{NW}}{A_P} = 2\pi r h \rho_{NW} \qquad (5)$$

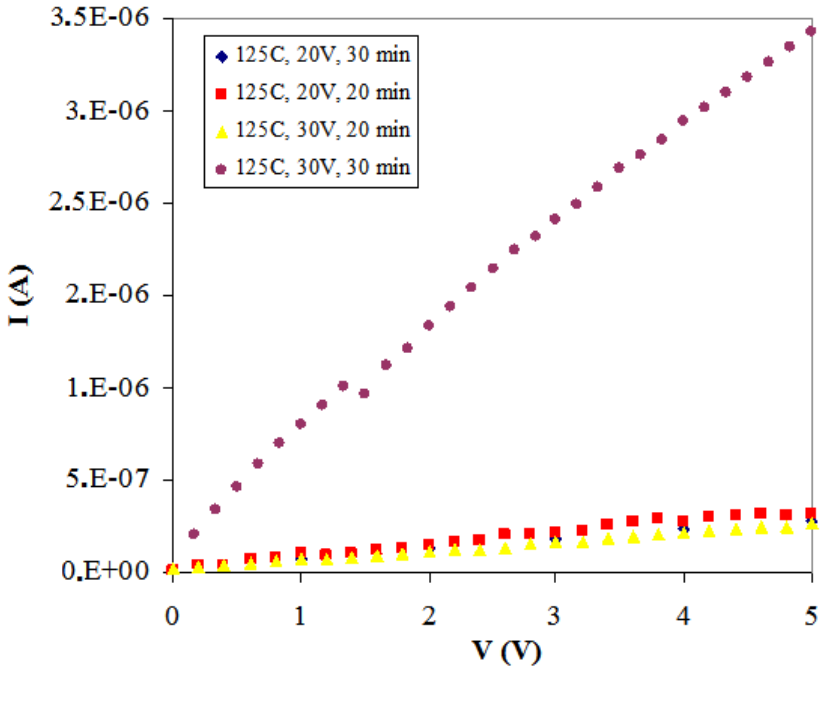
where $A_{NW}$ is the junction area of the nanowire array electrode, $A_P$ is the area of the planar electrode junction, $r$ is the radius of a single nanowire, $h$ is the height of the nanowires, and $\rho_{NW}$ is the density of nanowires. Aforementioned, the diameter and the length of the CdS nanowires deposited for 10 min were much smaller than that of nanowires deposited for 30 min. However, the density of nanowires decreased with increasing the deposition time. The average $\rho_{NW}$ for the CdS nanowires deposited at 30V for 10 min and 30 min is approximately $10^9$ and $10^7$ nanowires/cm$^2$, respectively. This significant decrease in $\rho_{NW}$ may result the decrease in $V_{oc}$ of the nanowires deposited for 30 min. The highest efficiency of the CdS nanowires obtained in this study is about 1.4 % for the nanowires deposited at 30 V for 10 min. The most probable reason of the increase in $V_{oc}$ values is the increase in the cross-section area of the nanowires. Table 1 summarizes all $V_{oc}$, $I_{sc}$, $FF$ and $\eta$ values for CdS nanowires.

**Table 1.** $V_{oc}$, $I_{sc}$, $FF$ and $\eta$ values for the CdS nanowires

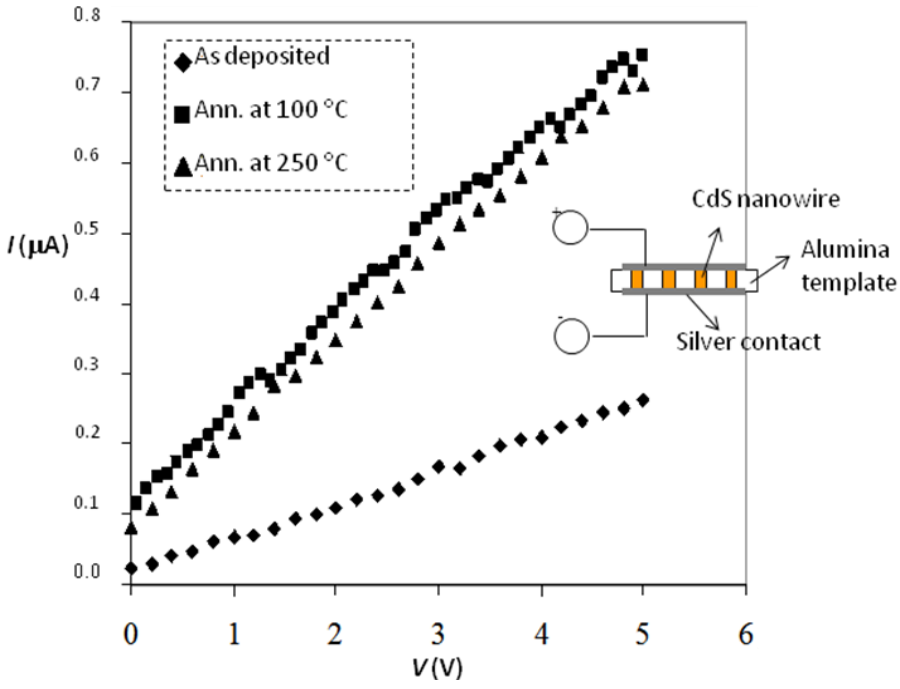
| **Condition** | $V_{oc}$ **(mV)** | $I_{sc}$ **(mA)** | $FF$ **(%)** | $\eta$ **(%)** |
|---|---|---|---|---|
| 30 V, 30 min | 402 | 0.89 | 21.5 | 0.22 |
| 30 V, 10 min | 1590 | 0.65 | 45.7 | 1.36 |
| 20 V, 30 min | 562 | 0.08 | 23.1 | 0.03 |
| 20 V, 10 min | 418 | 0.08 | 15.9 | 0.02 |

For further understanding of the electrical characteristic of the nanowires, room temperature electrical conductivity measurements have been performed. It has been obtained that all nanowires showed ohmic behavior in the potential range between 0 and 5 V. Fig. 3.8.a shows the I-V results of the CdS nanowires which were deposited at 30 V and 20 V DC in different time ranges (30 min. and 20 min.). There is a linear increase for all of the samples with the increase in voltage and the CdS nanowires growth at 30V 30 min. shows the lowest resistivity. Fig. 3.8.b shows the schematic of the conductivity measurement and I-V plot of the nanowires deposited at 30 V for 20 min. As can be seen in this figure, conductivity of the samples increased with annealing process. The conductivity of the 30 V 30 min. sample, which was annealed at 250°C, increased around 1000 times. Table 2 summarizes the resistance of the nanowires deposited at 30 V for two different deposition time and annealing temperature. It was observed that resistance decreased approximately ten times while the deposition time goes from 20 to 30 min. This indicates more material deposition occurs when the deposition time increased, which was also supported by SEM analysis.

In this part of the study, CdS-NWs, having a huge potential to use in photochemical cell applications, have been synthesized via dc-electrochemical template based route. Structural configuration of CdS-NWs was confirmed by EDX and XRD analysis. Depending on synthesize conditions a dramatic change in photoelectrochemical performances of the nanowires has been observed.




(a)




(b)

Figure 3.8 **(a)** The I-V graphs of CdS Nanowires synthesized at 125 °C, 30V, 20 min and 30 min- 20V 20 min and 30 min **(b)** I-V plot of CdS-NWs deposited at 30 V for 30 min.

**Table 2.** Room temperature electrical properties of CdS-NWs deposited at 30 V

| Deposition time (min) | Annealing Temperature (°C) | Resistance (Ω) |
|---|---|---|
| 20 | no annealing | $2.0 \times 10^{7}$ |
| 30 | | $1.7 \times 10^{6}$ |
| 20 | 100 | $5.3 \times 10^{7}$ |
| 30 | | $5.0 \times 10^{6}$ |
| 20 | 250 | $5.4 \times 10^{6}$ |
| 30 | | $1.7 \times 10^{3}$ |

## 3.2 CdS/Polypyrrole Heterojunction Nanowires

Organic-inorganic hybrid (OIH) heterostructures have been gaining more attention, since they combine the high performance of inorganic materials with lower production cost and easy manufacturing techniques of organic materials [101,102]. OIH thin films have been used to fabricate electric and optoelectric devices for more than a decade with the improvement in both material science and device architectures [103,104]. Germanium [105], silicon [106], zinc oxide [107] and cadmium selenide [108] nanowires have been utilized in organic semiconductors for photovoltaic applications. The major drawback of organic semiconductors is their low charge carrier mobilities compare to the inorganic semiconductors. In this respect, organic semiconductor nanowires offer a rapid transport path for charge carrier due to their one-dimensional nature. We report herein, the fabrication of the polypyrrole(PPy) and CdS/Polypyrrole

(PPy) nanowire heterojunctions by an electrochemical route, which is a simple, and therefore, very cost effective method. Morphological, structural and optical properties of PPy nanowires and morphological, structural and phototelectrochemical properties of CdS/PPy heterojunction nanowires have been investigated in this part.

### 3.2.1 Morphological, Structural and Optical Properties of PPy Nanowires

Polypyrrole nanowires were synthesized via electropolymerization technique by using 0.1 M $LiClO_4$, 0.01 M pyrrole, and $7x10^{-4}$ M sodium dodecylsulfate [109]. During synthesize, potential was swept between 0 and 0.85 V at a scan rate of 400 mV/s for various number of scans. The system was three electrodes one compartment system in which silver wire as reference electrode, platinum as a counter electrode and gold coated AAO membrane as working electrode were used. Morphological characterization of the nanowires has been performed using a QUANTA 400F Field Emission Scanning Electron Microscope. For surface SEM, UV-vis and FTIR measurements templates were dissolved in 1 M NaOH solution after coating one side with epoxy. The absorbance spectra of the samples were measured by a Pharmicia LKB Ultraspec III UV-VIS spectrophotometer over the wavelength range of 350-900 nm at room temperature.

The effects of process conditions on the morphology of PPy nanostructures have been studied. Reynes O. et al. [110] have been reported that depending on the pore size of the template, pyrrole monomer concentration and Cyclic Voltammetry (CV) scan rate, either PPy nanotube or nanowire formation occurs. Herein, to control the length and the diameter of the PPy nanowire have been controlled by the number of CV scan. Figure 3.9 (a) and (b) shows the SEM images of PPy nanowires deposited in gold coated AAO membrane. When the number of scan increased, both the length and the diameter of the PPy nanowires increased. The average length and the diameter of the PPy nanowires formed after 200 scans were 3 μm and 300 nm, respectively. When the number of scan increased to 800, average length and the diameter of the nanowires reached to 26 μm and 400 nm. In all cases the surface of the PPy nanowires was rough indicating the

random nucleation position. This could be attributed to the absence of molecular anchors on the alumina pores. Hernandez SC et al. [111] have been reported very smooth PPy nanowires by coating the AAM walls with $SiO_2$ prior to the PPy deposition. They concluded that anionic sites on $SiO_2$ provide preferential nucleation for polypyrrole along the pore walls.

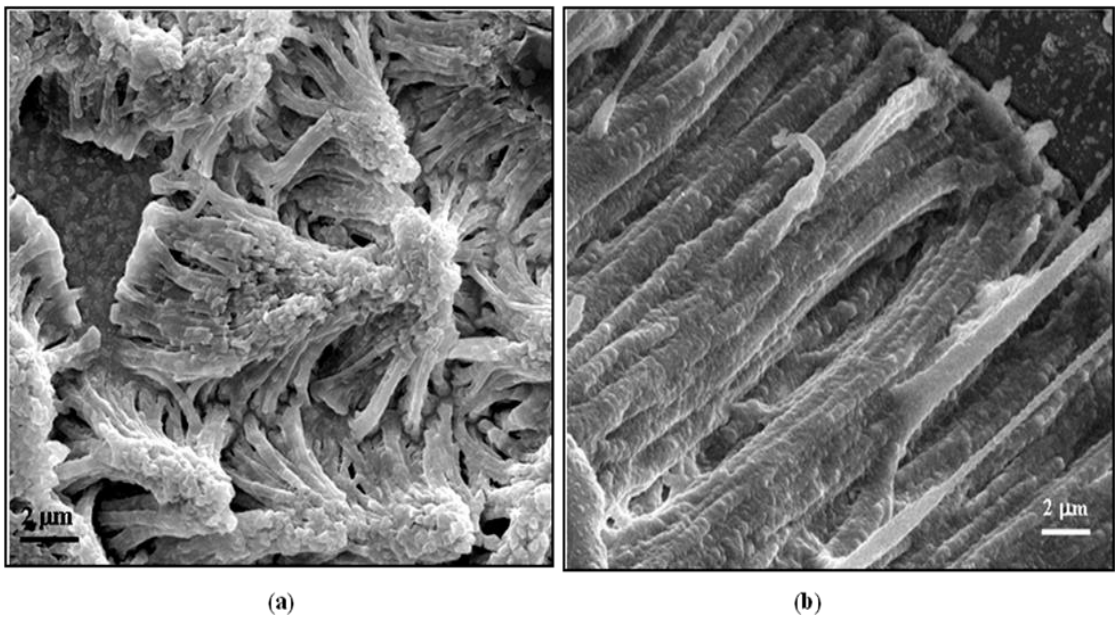



Figure 3.9 SEM images of (a) PPy nanowires deposited from 200 scans, (b) PPy nanowires deposited from 800 scans

The structure of the PPy nanowires has been investigated through FTIR analysis. In order to obtain template free nanowires, one side of the AAO membrane has been covered by epoxy and template has been dissolved in 1 M NaOH solution and samples have been dried at 60 °C over night. Then, these samples were used for FTIR analysis.

Figure 3.10 shows the FTIR spectra of blank epoxy and PPy nanowires deposited for different CV cycles. FTIR spectra support the SEM results. With the increase in the CV cycle number, the amount of the deposited material also increases. For the samples deposited for 400 and 800 cycles, characteristic absorption bands due to the PPy ring structure, which includes the combination of C=C stretch, C-N stretch, and the deformation of the five-membered ring containing the C=C-N, C=C-C deformation [112]. The most impressive characterization difference between epoxy and PPy nanowire attached on the epoxy is the large absorption band for the PPy sample at 1410 $cm^{-1}$. This band could be attributed to the typical PPy ring vibration [113, 114]. Moreover, the peak shift around the 900 $cm^{-1}$ could be attributed to the =C–H out of plane vibration indicating polymerization of pyrrole [114]. For the PPy nanowires, deposited for 100 CV cycle a very slight band shift around 900 $cm^{-1}$, was again obtained probably indicating polymerization of pyrrole. However, for the PPy nanowires deposited for 100 cycle epoxy peaks was dominant at FTIR spectra, most probably due to the less material deposition compare to the 400 and 800 CV cycle.

More structural analysis for the PPy nanowires has been performed via UV-vis spectrophotometer. As can be seen in Figure 3.11, regardless of the CV cycle number, all UV-vis absorption spectra exhibit a sharp absorbance in the 3.9-3.3 eV and broad absorption for smaller energies. These peaks can be assigned to $\pi$–$\pi^*$ transitions in the polymer backbone. For the sample deposited for 800 CV cycle has minor absorbance peaks around 1.6 eV, which could be described as free carrier tail.

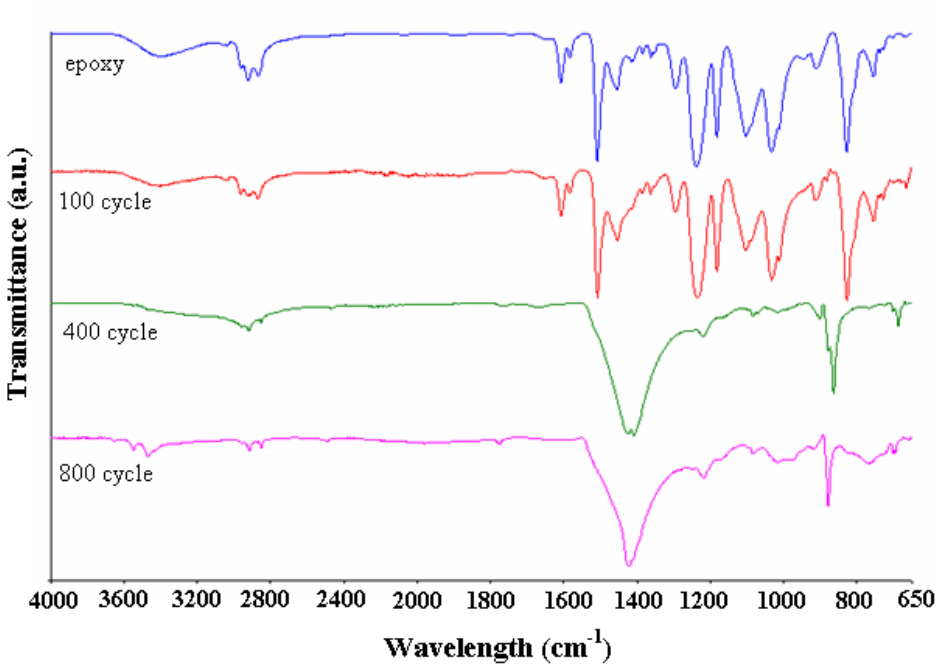



Figure 3.10. FTIR spectra of PPy nanowires and blank epoxy

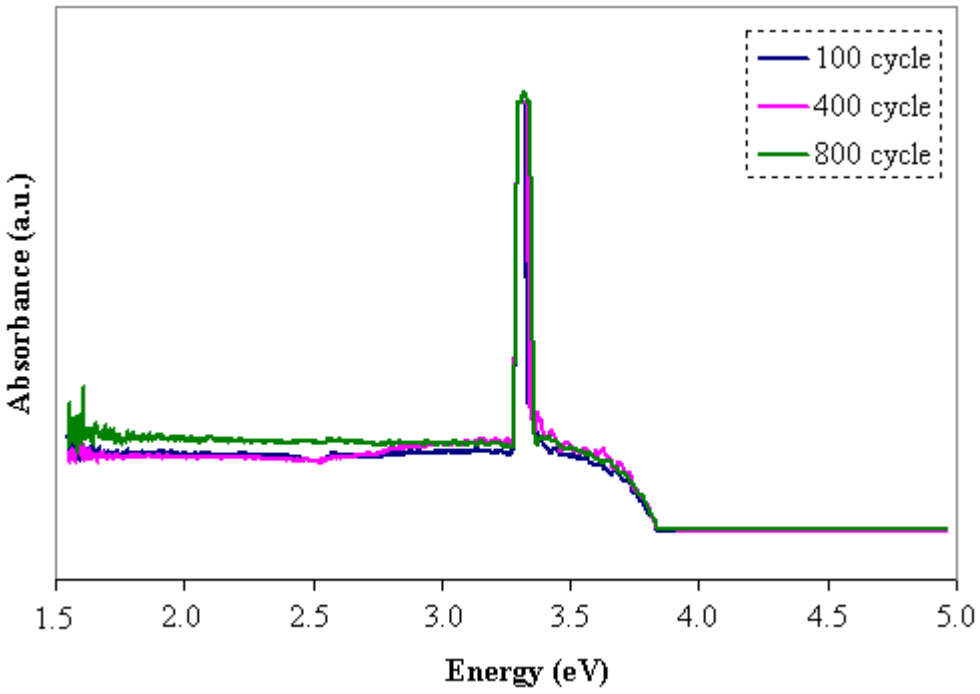
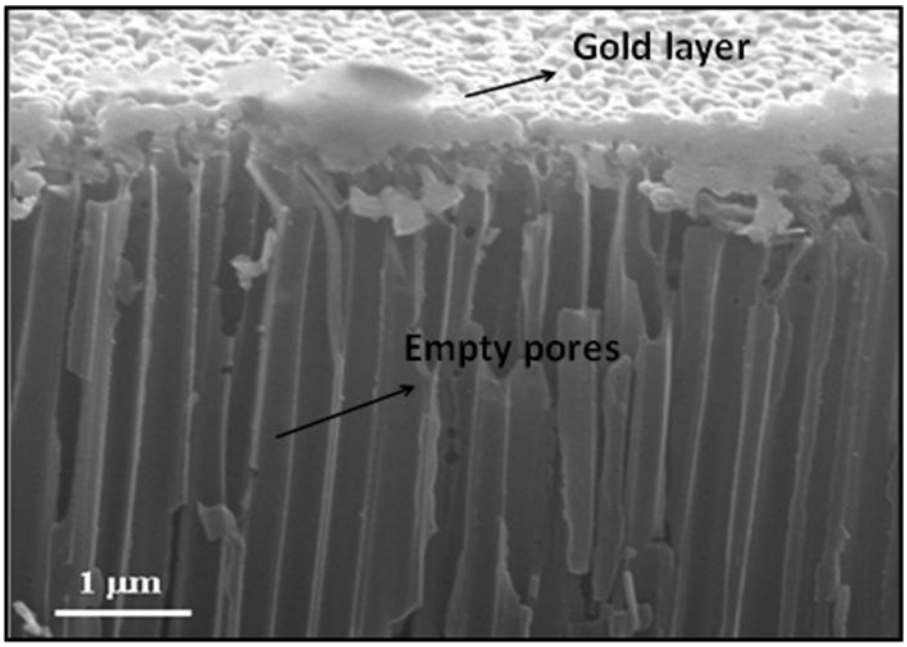



Figure 3.11 UV-vis spectra of PPy nanowires

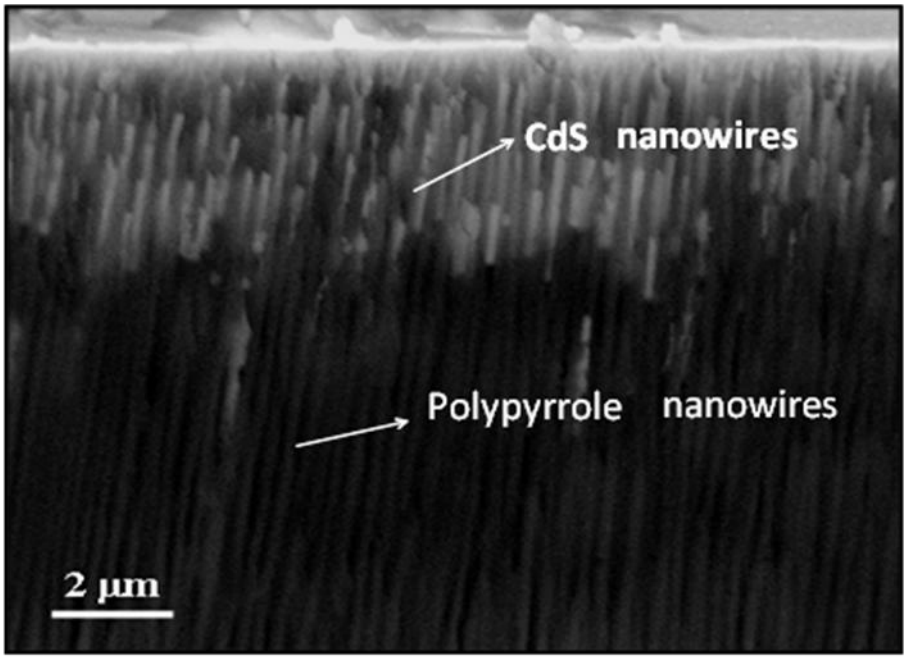
### 3.2.2 Morphological and Photoelectrochemical Properties of CdS/PPy Heterojunction Nanowires

In order to form organic-inorganic hybrid (OIH) structure, polypyrrole nanowires have been electrochemically deposited on CdS nanowires. For this process, AAO templates with CdS nanowires have been used as working electrode and polypyrrole formation was carried out by cyclic voltammetry. First, gold coated anodized alumina oxide (AAO) membranes were immersed into a solution containing 0.055M $CdCl_2$ and 0.19M elemental sulphur. Solution temperature was kept at 125 °C. In order to investigate the effects of process conditions on polypyrrole nanowires formation, two different deposition time (30V-30min and 30V-10 min) have been chosen. After CdS nanowire deposition, polypyrrole nanowires synthesized on the same electrode by using 0.1 M $LiClO_4$, 0.01 M pyrole, and $7x10^{-4}$ M sodium dodecylsulfate. During synthesize, potential was swept between 0 and 0.85 V at a scan rate of 400 mV/s for various number of scans.

The cross sectional SEM images of the gold coated empty AAO membrane and CdS/PPy deposited AAO membrane can be seen in Figure 3.12 (a) and (b).As it can be seen from the figure, the heterojunction of CdS and polypyrrole nanowires have been done successfully.




(a)




(b)

Figure 3.12 SEM images of (a) cross section of gold coated empty AAO (b) cross section of AAO after CdS/PPy deposition.

PEC cell configuration has been formed with CdS and CdS/PPy nanowires as working electrode into a three-electrode in one compartment cell, with a graphite counter electrode and Ag/AgCl reference electrode. Electrical response of the nanowires under illumination ($35mW/cm^2$) has been recorded using a Gamry G750 Potentiostat/Galvanostat/ZRA system. 0.1M $Na_2S$, 0.1M NaOH and 0.1M S solution has been used as electrolyte.

A photoelectrochemical (PEC) cell enables the conversion of the solar energy into chemical energy, which can be used as a fuel. Basically in a PEC cell with n-type semiconductor electrode, photon, which has an energy that is equal or greater than the bandgap, excites the electrons from valance band to the conduction band. These excited electrons travel through the counter electrode where the reduction of water to form hydrogen gas occurs. Fill factor (*FF*), which is equal to the ratio of theoretical power to the actual power of the cell, and the power conversion efficiency ($\eta$), which is a measure of how much of solar energy converted to the electrical energy, are the two key parameters determining the performance of a PEC cell. The calculation of fill factor and power efficiency was done from the equation (2) and (3). In this part of the study, both CdS nanowires and CdS/PPy OIH nanowire structures have been used as semiconductor electrode.

Figure 3.13 shows a set of linear sweep voltammograms recorded on CdS and CdS/PPy nanowires. As mentioned before, the CdS nanowires which were deposited at 30 V for 30 min has the highest $I_{sc}$, about 0.9 mA. On the other hand, nanowires deposited at 30 V for 10 min has the highest $V_{oc}$, and therefore, the highest $\eta$, which is about 1.4 %. Efficiencies of the nanowires deposited at 20 V were very low compare to the nanowires deposited at 30 V. Therefore, we have deposited the PPy nanowires on the CdS nanowires, which have been deposited at 30 V for 30 and 10 min. As can be seen in Figure 3.13, PEC performances of the CdS nanowires improved significantly after PPy nanowire deposition. $V_{oc}$ of the all CdS/PPy heterostructures was comparable and ranging between 500 and 800 mV. On the other hand, $I_{sc}$ values of the heterostructures changed approximately 24 times by changing the CdS deposition time and number of

CV cycle for PPy deposition. The maximum $\eta$, obtained in this study is about 5.0 %. This is one of the highest efficiencies reported in the literature for the nanowire array PEC cells. Feng X et al. have been reported the $TiO_2$ nanowire array grown directly on fluorine-doped tin oxide coated glass having the photoconversion efficiency of 5.02% [115]. Interestingly, it has been obtained that the $\eta$ decreased with increasing the number of CV cycle for PPy deposition. This may be attributed to the increase in the trap levels in PPy nanowires with more material deposition. As seen in SEM pictures surface of the PPy nanowires are very rough, probably indicating the nanowire formation occurs by random nucleation of PPy nanoclusters. Hence, the optical path increases with increasing the nanowire length, which results the decrease in both $V_{oc}$ and $I_{sc}$. Table 3 summarizes the $V_{oc}$, $I_{sc}$, $FF$ and $\eta$ values for CdS/PPy nanowires.

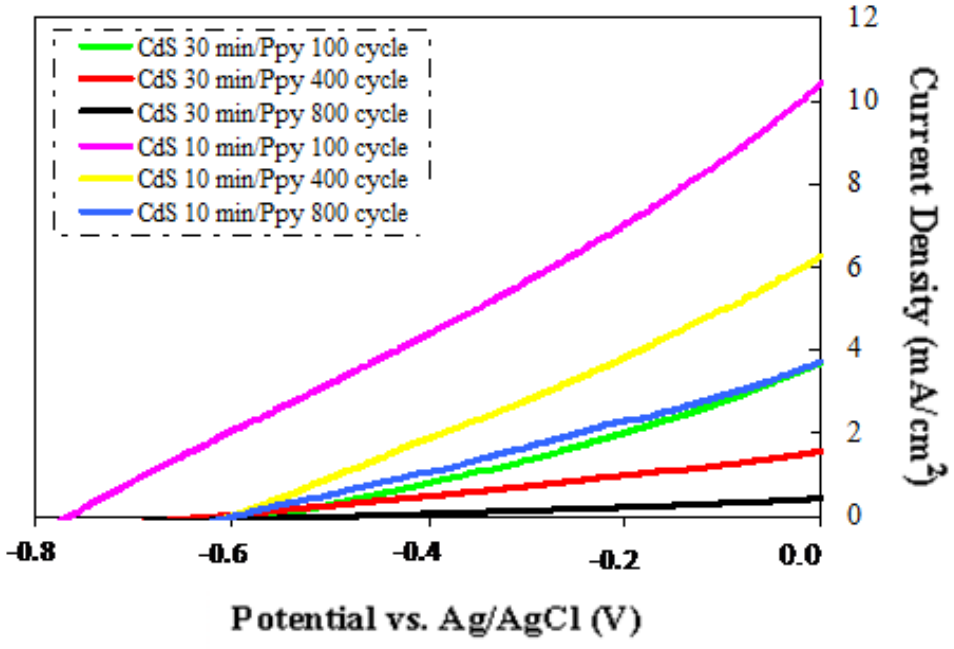



Figure 3.13**.** Potential versus current density graph of CdS (deposited at 30 V, 125 °C) /PPy nanowires

**Table 3.** $V_{oc}$, $I_{sc}$, $FF$ and $\eta$ values for CdS/PPy nanowires

| **Condition** | $V_{oc}$ **(mV)** | $I_{sc}$ **(mA)** | $FF$ **(%)** | $\eta$ **(%)** |
|---|---|---|---|---|
| 30 V, 30 min CdS /100 cycle PPy | 559 | 3.70 | 20.2 | 1.19 |
| 30 V, 30 min CdS /400 cycle PPy | 626 | 1.57 | 21.4 | 0.60 |
| 30 V, 30 min CdS /800 cycle PPy | 508 | 0.44 | 21.5 | 0.14 |
| 30 V, 10 min CdS /100 cycle PPy | 764 | 10.5 | 21.9 | 5.00 |
| 30 V, 10 min CdS /400 cycle PPy | 592 | 6.25 | 22.6 | 2.39 |
| 30 V, 10 min CdS /800 cycle PPy | 588 | 3.72 | 22.9 | 1.43 |

Chemical stability under dark and illumination is among the key factors affecting the performance of a PEC cell. It has been known that most non-oxide semiconductors such as Si, GaAs and CdS are not chemically stable in electrolyte solutions. They generally either dissolve or an oxide layer forms at the semiconductor-electrolyte interface. However, they have very suitable band edge positions to enable reduction/oxidation of water. Therefore, it is very important to improve their resistance against photo-

corrosion. Figure 3.14 (a)(b) indicates the change in $I_{sc}$ with time. For both CdS and CdS/PPy nanowires, $I_{sc}$ stabilized after at a certain time. These equilibrium currents have been used for *FF* and $\eta$ calculations. It has been reported that both poly and nanocrystalline thin films of CdS are very sensitive to redox couple and have a tendency to dissolve in polysulfide electrolyte [116].

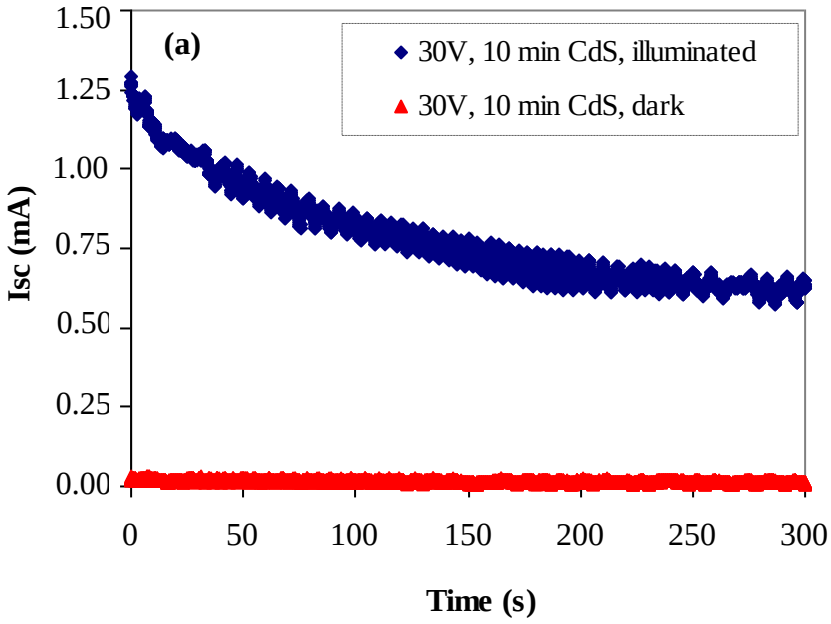



Figure 3.14 **(a)** $I_{sc}$ versus time graphs for CdS nanowires

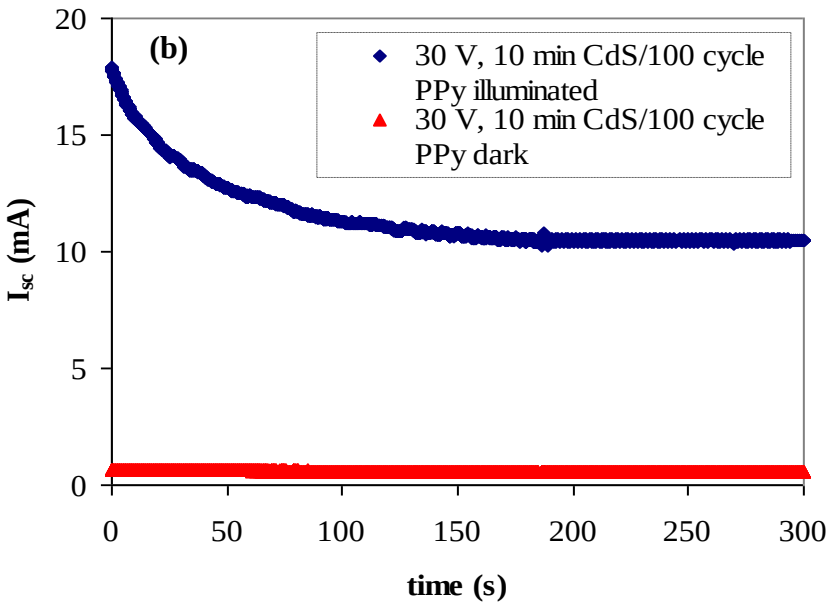



Figure 3.14.continued $I_{sc}$ versus time graphs for **(b)** CdS/PPy nanowires

## 3.3 CdS/CdTe Heterojunction Nanostructures

CdTe has a bandgap value (1.44 eV) which is very close to the theoretically-calculated optimum value for solar cells. That's why it is a very suitble candidate for photovoltaic applications. CdTe constitutes the absorber layer in a photovoltaic cell since it has a high absorption coefficient, so that approximately 99% of the incident light is absorbed. P-type CdTe forms the p part of a p-n junction solar cell. Moreover, high quality of CdTe can be deposited on top of CdS which leads to the heterojunctions of p-type CdTe and n-type CdS to CdS/CdTe solar cells. In addition, CdTe solar cells are stable under proton, electron and UV irradiation, and under strong temperature changes, therefore suitable for space applications.

CdTe has been deposited by using 0.1M $CdSO_4$ and 150 ppm $TeO_2$ and ultra pure water as solvent at room temperature over gold coated AAO membrane. The deposition voltage was kept -0.58 V and Ag/AgCl electrode was used as reference electrode and

Graphite rode was used as counter electrode. Morphological characterization of the CdTe nanostructures has been performed using a QUANTA 400F Field Emission Scanning Electron Microscope. Energy Dispersive X-Ray (EDX) was used for structural configuration. The photoelectrochemical properties of CdS/CdTe heterojunction nanostructures have been investigated by potentiostat.

### 3.3.1 Morphological and Sturctural Properties of CdTe Nanostructures

Figure 3.15 shows the SEM images of CdTe nanostructures deposited at different time ranges. For surface SEM measurements templates were dissolved in 1 M NaOH solution after coating one side with epoxy. As it can be seen from Figure 3.15, the structures of CdTe are not nanowires but nanoclusters. Figure 3.15 (d) is the cross section SEM image of 9 hour CdTe and it is clearly seen that CdTe is deposited as nanoclusters. With the increasing deposition time the density and the average diameter of the clusters increases and the average diameter of the 9 hour CdTe nanoclusters are about 260 nm, Fig 3.16. It has been seen that CdTe has a tendency to grow as clusters but not nanowires with the experimental conditions we used. Figure 3.17 shows the EDX results of the CdTe nanoclusters. From EDX results of CdTe nanoclusters deposited at different time ranges, it can be seen that the main peaks belongs to the cadmium and tellirum.

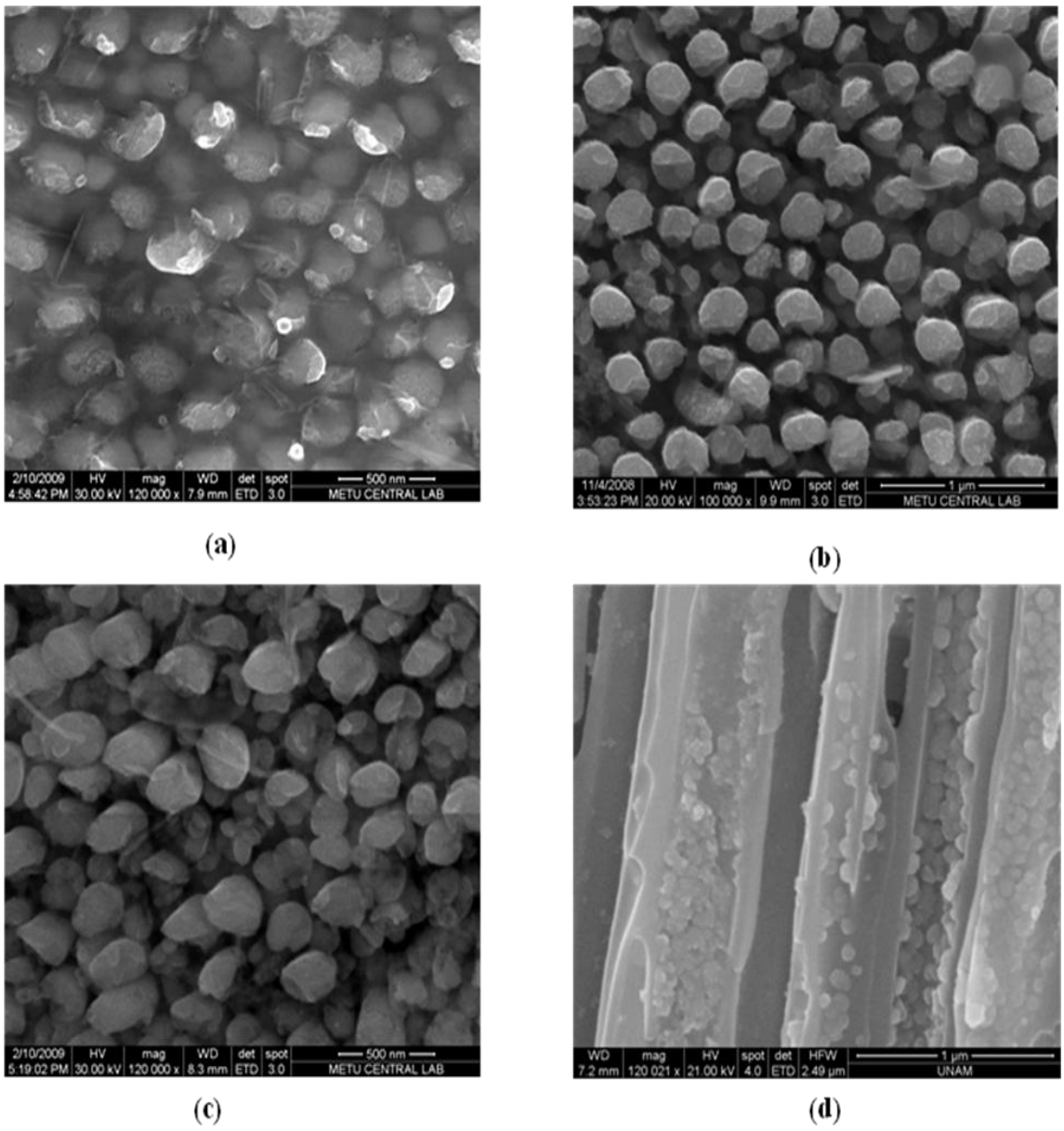



Figure 3.15 SEM images of CdTe nanoclusters (a) 5 (b) 7 (c) 9 hours (d) cross section of 9 hour CdTe nanocluster

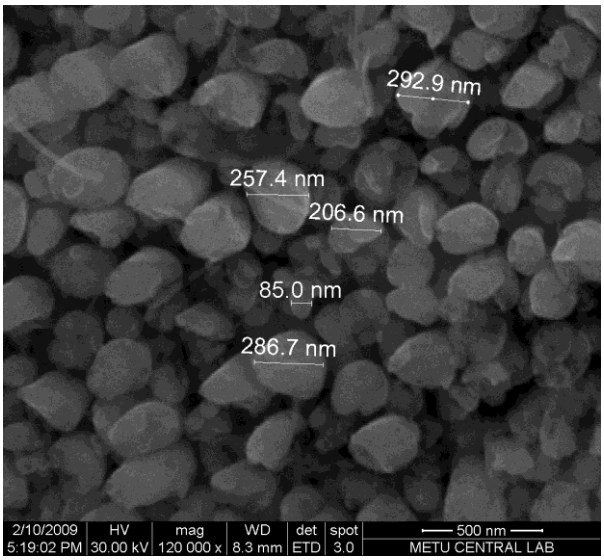



Figure 3.16 Average diameters of CdTe nanoclusters

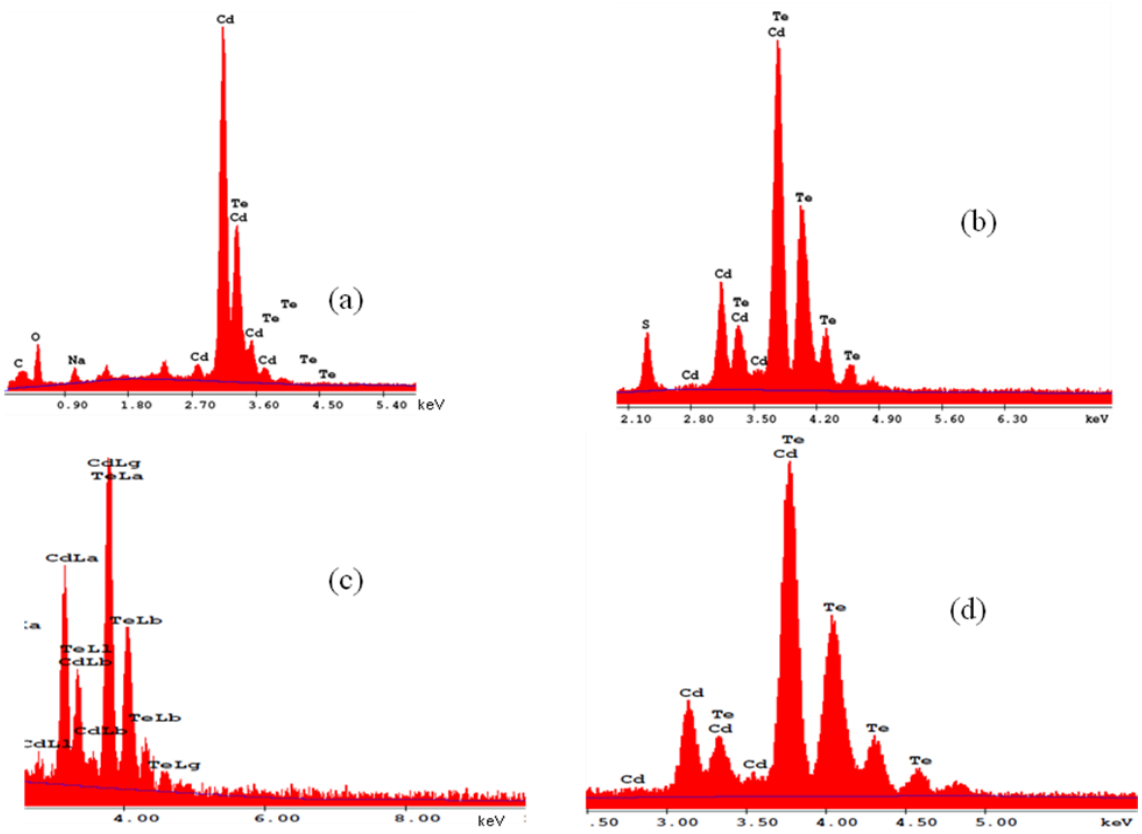



Figure 3.17 EDX Results of CdTe nanoclusters (a) 3 (b) 5 (c) 7 and (d) 9 hours

### 3.3.2 Morphological and Photoelectrochemical Properties of CdS/CdTe heterojunction nanostructures

In order to form CdS/CdTe heterojunction nanostructure, CdTe nanoclusters have been electrochemically deposited on CdS nanowires. For this process, AAO templates with CdS nanowires have been used as working electrode and CdTe formation was carried out by electrodeposition. First, gold coated anodized alumina oxide (AAO) membranes were immersed into a solution containing 0.055M $CdCl_2$ and 0.19M elemental sulphur. Solution temperature was kept at 125 °C. After CdS nanowire deposition at two different time ranges (30 min, and 10 min.), CdTe nanoclusters synthesized on the same electrode by using 0.1M $CdSO_4$ and 150 ppm $TeO_2$ and ultra pure water as solvent at three different time ranges ( 5, 7 and 9 hours).

Morphological characterization of the CdS/CdTe heterojunction nanostructures have been performed by using a QUANTA 400F Field Emission Scanning Electron Microscope.The cross sectional SEM images of the 30 V 30 min CdS/9 hour CdTe heterojunction can be seen in Figure 3.18. As it is seen from the figure, CdTe nanoclusters have been successfully deposited over CdS nanowires. The figure shows the junction area of CdS nanowire and CdTe nanoclusters in one pore of AAO membrane.

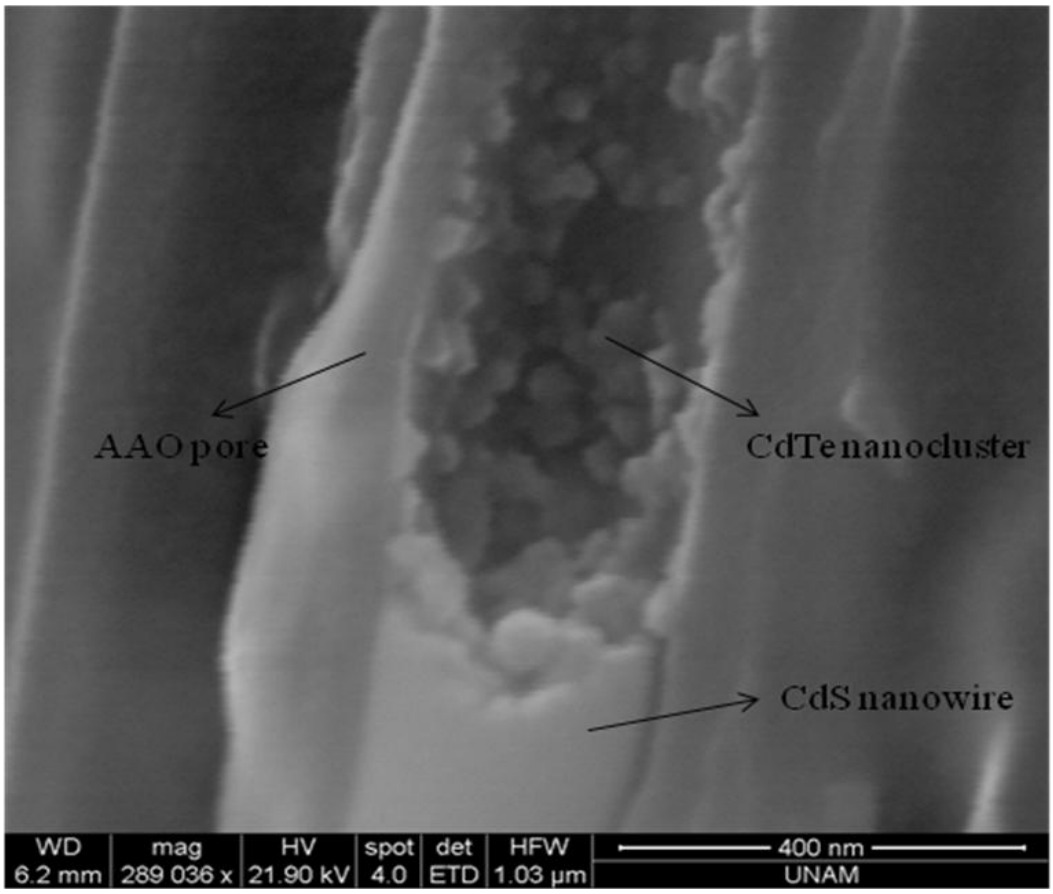
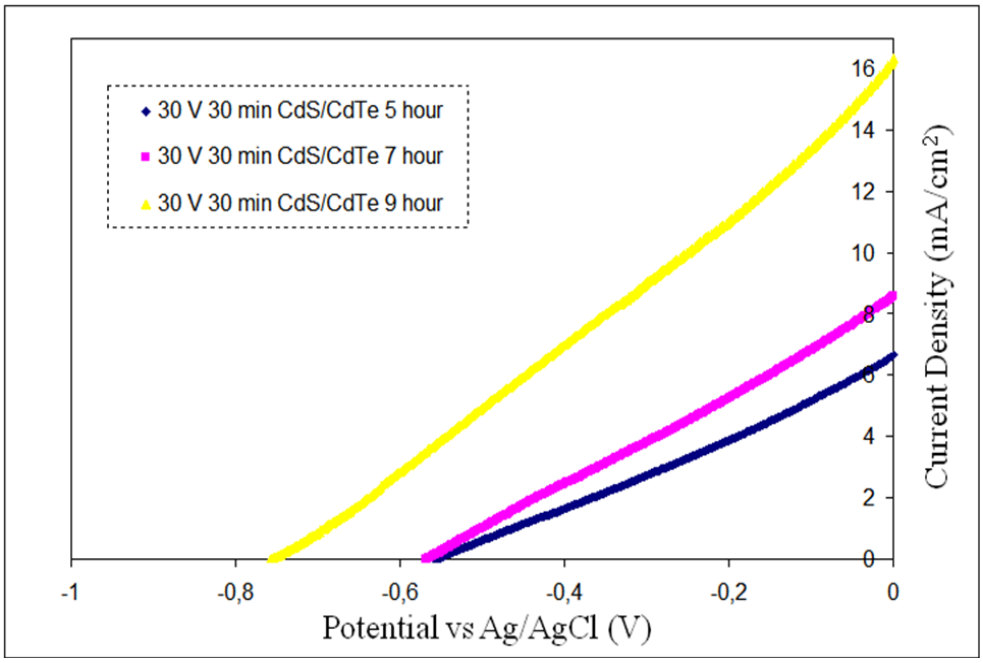



Figure 3.18 The cross section of SEM image of 30 V 30 min CdS/9 hour CdTe heterojunction in one AAO membrane pore

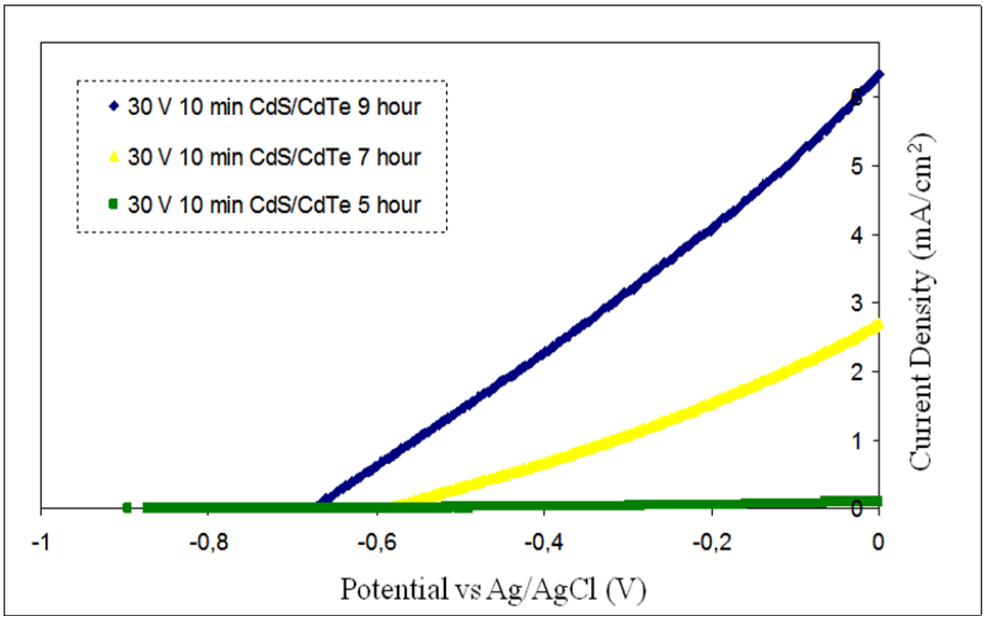
PEC configuration has been formed with CdS/CdTe heterojunction nanostructures as working electrode into a three-electrode in one compartment cell, with a graphite counter electrode and Ag/AgCl reference electrode. Electrical response of the heterojunction under illumination (35 mW/cm$^2$) has been recorded using a Gamry G750 Potentiostat/Galvanostat/ZRA system. 0.1M $Na_2S$, 0.1M NaOH and 0.1M S solution has been used as electrolyte. The experimental setup is the same as in Figure 3.6.

As mentioned before, fill factor (*FF*), which is equal to the ratio of theoretical power to the actual power of the cell, and the power conversion efficiency ($\eta$), which is a measure of how much of solar energy converted to the electrical energy, are the two key parameters determining the performance of a PEC cell. The calculation of fill factor and power efficiency was done from the equation (2) and (3). In this part of the study, CdS/CdTe heterojunction nanostructures have been used as semiconductor electrode in the photoelectrochmical cell configuration.

Since the efficiencies of CdS nanowires deposited at 20 V was very low, in order to investigate the effect of the length of the CdS nanowires on the PEC performances of CdS/CdTe heterojunction, CdS nanowires deposited at 30 V DC and two different time ranges ( 30 V 30 min. and 30 V 10 min.). Figures 3.19 (a) and (b) show a set of linear sweep voltagrams recorded on CdS/CdTe heterojunction. PEC performances of the CdS nanowires (Table 2) improved significantly after CdTe deposition. $V_{oc}$ of the all CdS/CdTe heterostructures was comparable and ranging between 550 and 750 mV. On the other hand, $I_{sc}$ values of the heterostructures vary between 0.01 and 8.62 mA by changing the CdS and CdTe deposition times. The maximum $\eta$, obtained in this study is about 8.0 % for the 30 V 30 min CdS/9 hours CdTe sample. With the increase in the deposition time of the CdTe, there is a linear increase in $\eta$ values for both 10 and 30 minutes deposited CdS nanowires as it was expected. Table 4 summarizes the $V_{oc}$, $I_{sc}$, *FF* and $\eta$ values for the CdS/CdTe heterostructures.




**(a)**




**(b)**

Figure 3.19 Potential versus current density graph of (a) 30 V 30 min CdS-5, 7, 9 hours CdTe (b) 30 V 10 minCdS-5, 7, 9 hours CdTe

**Table 4.** $V_{oc}$, $I_{sc}$, $FF$ and $\eta$ values for the CdS/CdTe heterojunction

| **Condition** | $V_{oc}$ **(mV)** | $I_{sc}$ **(mA)** | $FF$ **(%)** | $\eta$ **(%)** |
|---|---|---|---|---|
| 30 V, 30 min CdS /5 hours CdTe | 541 | 6.67 | 23.1 | 2.38 |
| 30 V, 30 min CdS /7 hours CdTe | 558 | 8.62 | 23.7 | 3.26 |
| 30 V, 30 min CdS /9 hours CdTe | 748 | 16.4 | 23.0 | 8.04 |
| 30 V, 10 min CdS /5 hours CdTe | 638 | 0.01 | 16.1 | 0.03 |
| 30 V, 10 min CdS /7 hours CdTe | 584 | 2.71 | 20.6 | 0.93 |
| 30 V, 10 min CdS /9 hours CdTe | 664 | 6.35 | 22.6 | 2.73 |

# CHAPTER 4

# CONCLUSION

In the first part of this study, CdS nanaowires were successfully deposited onto gold coated anodized alumina oxide (AAO) membrane via dc-electrochemical deposition technique. Morphological, structural, electrical, optical and photoelectrochemical characterizations of the CdS nanowires were performed. SEM analysis confirmed that CdS nanowires have been successfully deposited onto gold coated AAO membrane and it has been observed that the change in the deposition voltage and time changes the length of the CdS nanowires. The most stable and longest ones are the 30 V 30 min samples and the diameter and the length of the nanowires produced for 30 min reached 200 nm and 4 μm, respectively. EDX and XRD measurements were performed to confirm the structural properties of CdS nanowires. The main peaks in the EDX measurements belong to the Cd and S which is a proof that the deposited material is CdS. Moreover, from the XRD measurements, it was understood that the deposited CdS crystals have hexagonal structure. The transmittance values of the CdS nanowires are about 40%. The band gap energies of CdS nanowires vary between 2.40 eV and 2.48 eV depending on the production conditions and these values are acceptable for optoelectronic applications. The photoelectrochemical behaviors of CdS nanowires have also been investigated. The fill factor and power efficiencies were calculated from the linear sweep voltammograms of the CdS nanowires and for the 30 V 10 min sample, one of the highest fill factor (FF) and power efficiency ($\eta$) in the literature, which are 1.4% $\eta$ and 46% FF, has been calculated. For further understanding of the electrical characteristic of the nanowires, room temperature electrical conductivity measurements

have been performed. It has been observed that all nanowires showed ohmic behavior in the potential range between 0 and 5 V. The CdS nanowires growth at 30V 30 min. shows the lowest resistivity. The effect of annealing was also studied and it was seen that the conductivity of the 30 V-30 min. sample annealed at 250°C increased around 1000 times.

In the second part of this study, Polypyrrole (PPy) nanowires and CdS/PPy heterostructure nanowires were synthesized via electrochemical deposition technique onto gold coated AAO membranes. Morphological, structural and optical properties of PPy nanowires and morphological and photoelectrochemical properties of CdS/PPy nanowires were studied. From SEM ananlysis, it was seen that with the increase of Cyclic Voltammetry (CV) scan rates, there is an increase in both length and diameter of the PPy nanowires. The length and diameter of the 800 scan rate of the PPy nanowires are about 26 μm and 400 nm respectively. The structure of the PPy nanowires has been investigated through FTIR analysis. In the IR spectrum of PPy nanowires, all of the characteristic peaks of PPy were identified. More structural analysis for the PPy nanowires has been performed via UV-vis spectrophotometer. All PPy samples showed a sharp absorbance in the 3.9-3.3 eV and broad absorption of smaller energies. These peaks can be assigned to $\pi$–$\pi^*$ transitions in the polymer backbone.

From the cross section SEM image of CdS/PPy nanowires, the heterojunction between CdS and PPy nanowires were assigned successfully. For the investigation of the PEC performances of CdS/PPy nanowires, linear sweep voltammograms were used to calculate FF and $\eta$. Two different deposition times of CdS nanowires and 3 different CV scan rate of PPy nanowires were used to explore the highest $\eta$ of CdS/PPy heterostructure nanowires. The maximum $\eta$ obtained for CdS/PPy heterostructure is 5% for the 30 V 10 min CdS/100 cycle PPy sample. $I_{sc}$ changes with time under illumination and dark of the CdS and CdS/PPy nanowires were also investigated and it was seen that $I_{sc}$ reaches at stable values after at a certain time for both CdS and CdS/PPy nanowires.

In the final part of this study, CdTe nanoclusters and CdS/CdTe heterostructures were synthesized via electrochemical deposition technique onto gold coated AAO membranes. Morphological and structural properties of CdTe nanoclusters and morphological and photoelectrochemical properties of CdS/CdTe nanostructures were studied. From SEM analysis, it was clearly seen that CdTe were deposited as nanoclusters and with the increase in deposition time, the density and the diameter of the nanoclusters increase. The average diameter of the 9 hour CdTe nanoclusters were about 260 nm. EDX results showed that the main peaks belong to Cd and Te.

The heterojunction between CdS nanowires and CdTe nanoclusters were identified from the SEM image of the CdS/CdTe nanostructure. CdTe nanoclusters have been successfully deposited over CdS nanowires. Finally, by using linear sweep voltammogram of CdS/CdTe nanostructures the FF and $\eta$ values were calculated from the PEC configuration. Two different deposition times of CdS nanowires and 3 different depositon time of CdTe nanoclusters were used to explore the highest $\eta$ of CdS/CdTe heterostructure. The maximum $\eta$ was obtained for the 30 V-30 min. CdS/9 hour CdTe sample which is about 8%.

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