HMIC MINIATURIZATION TECHNIQUES AND APPLICATION ON AN FMCW RANGE SENSOR TRANSCEIVER

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ABSTRACT

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This thesis includes the study of hybrid microwave integrated circuits (HMIC), miniaturization techniques applied on HMICs and its application on a frequency modulated continuous wave (FMCW) range sensor transceiver. In the scope of study, hybrid and monolithic microwave integrated circuits (HMIC and MMIC) are introduced, advantages and disadvantages of these two types are discussed. Large size of HMICs is the main disadvantage especially for military and civil applications requiring miniature volumes. This thesis is mainly devoted on miniaturization work of HMICs in order to cope with this problem. In this scope, miniaturization techniques of some HMICs such as 3 dB hybrid couplers and stubs are examined and analyzed. Their simulation and measurement results cohere with original circuit results. Nevertheless, considerable size reduction up to 80% is achieved. Moreover, planar interdigital capacitors (IDC), spiral inductors (SI) and their equivalent circuit models are introduced. Design technique is discussed with illustrative electromagnetic (EM) simulations. Furthermore, FMCW radar is introduced with its basic operation principles, brief history and usage areas. In addition, FMCW range sensor transceiver is designed with its sub-parts; power amplifier, low noise

amplifier (LNA), coupler and front end. Multi technology based on chip transistors, interdigital capacitors, spiral inductors and hybrid couplers with wire-bond connections is used in the design. As the result of using hybrid miniaturized components small layout size is achieved for the transceiver system with its all components.

Keywords: HMIC miniaturization, FMCW, Planar Interdigital Capacitor, Planar Spiral Inductor, Hybrid Coupler

ÖZ

HMIC MİNYATÜRİZASYON TEKNİKLERİ VE FMCW MESAFE ALGILAYICI ALMAÇ GÖNDERMEÇ BİRİMİNDE UYGULAMASI

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Bu tez, hibrit mikrodalga tümleşik devreleri (HMTD), HMTD'lere uygulanan minyatürleştirme teknikleri ve bunların FMCW mesafe algılayıcı alıcı-vericisine uygulanması çalışmalarını içermektedir. Çalışma kapsamında, hibirt ve monolitik mikrodalga tümleşik devreler (HMTD ve MMTD) tanıtıldı, bu iki tipin avantaj ve dezavantajları ele alındı. Özellikle minyatür hacim gerektiren askeri ve sivil uygulamalarda HMTD' lerin büyük boyutları en temel dezavantajıdır. Bu tez temel olarak bu problemi çözmek için yapılan HMTD minyatürleştirme çalışmalarını ele almıştır. Bu kapsamda, 3 dB hibrit bağlaç ve saplama gibi bazı elemanlarda minyatürleştirme teknikleri incelendi ve analiz edildi. Minyatür devrelerin benzetim ve ölçüm sonuçları, orijinal devrelerinki ile uygunluk göstermektedir. Aynı zamanda %80'e varan boyut küçülmesi başarıldı. Bundan başka düzemsel parmaklı sığaç (PS), sarmal indüktör (SI) ve bunların eşdeğer devre modelleri tanıtıldı. Tasarım tekniği örnekleyici elektromanyetik benzetimlerle anlatıldı. Ayrıca, FMCW radar temel çalışma prensipleri, kısa geçmişi ve kullanım alanlarıyla birlikte tanıtıldı. FMCW mesafe algılayıcı alıcı-vericisi alt parçaları olan güç yükselteç, düşük gürültü yükselteci, bağlaç ve ön ucu ile birlikte tasarlandı. Tasarımda, yonga transistor, parmaklı sığaç, sarmal indüktor, hibrit bağlaç ve bunların tel-bağ bağlantısından

oluşan çoklu teknoloji kullanıldı. Hibrit minyatürleştirilmiş parçalar kullanılmasının sonucu olarak bütün parçalarıyla birlikte alıcı-verici sistemi için daha küçük devre alan başarılmış oldu.

Anahtar Kelimeler: HMTD minyatürleştirme, FMCW, Düzlemsel Parmaklı Sığaç, Düzlemsel Sarmal Indüktör, Hibrit Bağlaç

To my family

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LIST OF ABBREVIATIONS

ADS	Advanced Design System
CW	Continuous Wave
EM	Electro-Magnetic
FMCW	Frequency Modulated Continuous Wave
IDC	Interdigital Capacitor
IF	Intermediate Frequency
HMIC	Hybrid Microwave Integrated Circuit
LO	Local Oscillator
MEMS	Micro Electro Mechanical System
MIC	Microwave Integrated Circuit
MMIC	Monolithic Microwave Integrated Circuit
NF	Noise Figure
RF	Radio Frequency
SI	Spiral Inductor
SNR	Signal-to-Noise Ratio
FET	Field Effect Transistor

CHAPTER 1

INTRODUCTION

Radio and microwave frequency circuit design is a challenging task for the designer. Designers are equipped with various techniques that are applicable in different implementation technologies. Microwave integrated circuit (MIC) technology is one of the most popular and frequently used technologies by the designers.

MIC is the technique of incorporating transmission lines, discrete resistors, capacitors, inductors and active devices on planar substrates. For frequencies higher than 2 GHz, parasitic reactances become a limiting factor for microwave circuits especially for broadband applications. Thus, small size is the inevitable solution of those parasitic limitations. To decrease the size, microwave sub-systems are integrated on a few millimeter-square chips or on substrates with the advances of the microwave integrated circuit (MIC) technology. MIC technology gives much better performance for higher frequencies with the elimination of parasitic effects. This advantage of MIC technology results in various applications in both civil and military systems. Some of the common applications of MIC technology are microwave power amplifiers, mixers, couplers, switches, attenuators, low noise amplifiers (LNAs), phase shifters on planar substrates with good reproducibility.

Microwave integrated circuit (MIC) fabrication requires four basic materials; substrate, conductor, dielectric film, resistive film. Substrate is the most critical material among those four; thus its selection is an essential task of the designer. Thickness, dielectric constant, loss tangent and dielectric strength, together with cost, are the selection parameters of the substrate in a microwave circuit design. High dielectric constant is preferred for designs where size consideration is important. On the other hand, for high power applications dielectric strength becomes important in order not to have a voltage breakdown on substrate. Table 1-1 shows parameters of some commonly used substrates.

Another important material is the conductor. In circuit design the conductor should have high conductivity, low temperature coefficient of resistance, low RF resistance and good solderability for better performance [1]. Copper (Cu), Silver (Ag) with high thermal expansion coefficient but with poor adherence to dielectrics, Chromium (Cr), Tantalum (Ta) with good adherence to dielectrics but low thermal expansion coefficients are examples of widely used conductor materials. Dielectric films are used in MIC fabrication as insulators for capacitor, protective layers for active devices and insulating layer for passive circuits [1]. Dielectric Strength and quality factor are important parameters for selection of dielectric film materials. SiO_2, Al_2O_3, Ta_2O_5 are some examples with dielectric strength 10^7, $4x10^6$, $6x10^6$ V/cm respectively. Finally, resistive film materials are essential in the fabrication of terminations, attenuators, bias networks. Table 1-2 shows some resistive film materials used in microwave integrated circuit (MIC) design showing their resistivity and stability measure.

Table 1-1: Properties of Some Commonly Used MIC Substrates

Material	Dielectric Constant (εr)	Loss Tangent (tan δ)	Dielectric Strength (kV /cm)	Application
Alumina	10	$2x10^{-4}$	$4x10^{3}$	Microstrip
Glass	5	$20x10^{-4}$	-	Lumped Element
GaAs	12,9	$6x10^{-4}$	350	Microstrip, MMIC
Si	11,7	$10\text{-}100x10^{-4}$	300	RFIC

Table 1-2: Properties of Some Commonly Used MIC Resistive Film Materials

Material	Resistivity (Ω /square)	Stability
Cr	10-1000	Poor
NiCr	40-400	Good
Ta	5-100	Excellent

There exist two distinct types of microwave integrated circuits; namely, monolithic microwave integrated circuits (MMIC) and hybrid microwave integrated circuits (HMIC).

The first type of microwave integrated circuit is monolithic. A monolithic microwave integrated circuit (MMIC) is a microwave circuit in which all active and passive components are deposited and patterned on the same semiconductor substrate. This meaning is hidden in the word “monolithic”. The word monolithic is derived from the two Greek words monos meaning single and lithos meaning stone [5]. As the result of implementing all components with same semiconductor in small sizes, the frequency of operation ranges from 1 GHz to beyond 100 GHz for monolithic microwave integrated circuits

(MMIC). In order to implement active components such as diodes and transistors, semiconductor material is to be used as substrate. Among semiconductor materials, gallium arsenide (GaAs) has been used extensively in the advancement of microwave integrated circuits (MMIC) which is more recent development of microwave integrated circuit (MIC) technology [2]. The history of MMIC technology is not very old. The first GaAs MMICs, which are Gunn Diode oscillator, frequency multiplier and mixer, are composed of diodes and microstrip lines and reported by Texas Instruments in 1968 [2]. The transistor based layout was first designed by Michael Gay at Caswell which is a receiver [2]. Afterwards, in 1979, IEEE organized a symposium on GaAs integrated circuit (IC) technology. Published papers since then became the milestone in the development of monolithic microwave integrated circuit (MMIC) technology. In 1982, Hornbuckle and Van Tuyl presented the results of direct-coupled amplifiers and level-shifting diodes. After the availability of electromagnetic simulators, designer of monolithic microwave integrated circuit (MMIC) had the ability of modeling circuits with great confidence. In recent MMIC designs, Si, SiGe, GaAs, InP are most commonly used substrate materials with gold, aluminum, copper metal connections. Due to the usage of single substrate with all active, passive components on it, MMIC technology provide small size designs with good repeatability. As the result of small size and good repeatability considerations, MMIC technology is widely used in military, space and civil applications. Among those applications, the electronically steered phased-array antenna is one of an important usage area requiring many identical elements in small sizes.

Monolithic microwave integrated circuit (MMIC) fabrication includes the fabrication of active devices, resistors, capacitors, inductors, distributed matching networks, air bridges, and via holes. Figure 1-1 shows a typical flow chart of a MMIC process [1].

The second and final type of MIC technique is hybrid microwave integrated circuit. A hybrid microwave integrated circuit (HMIC) consists of a metallization layer for conductor and transmission lines with all discrete active and passive components are connected to substrate material by soldering or wire bond connection. As the result of using discrete components in hybrid MICs, high operation frequency is lower compared with MMIC. Thus, the upper frequency of hybrid MIC is confined to 20 GHz for wireless, space and military applications. As in MMICs, substrate material selection is also critical. Alumina, quartz and Teflon are commonly used substrate materials for hybrid MICs. Alumina has relatively high dielectric constant (ε_r=9-10) which reduces the circuit size. On the other hand, quartz is a rigid material and has a lower dielectric constant ($\varepsilon_r \sim 4$) suitable for high frequencies (up to 20GHz) where radiation losses are important. For designs which do not require rigidity and good thermal transfer, Teflon is a better choice with lower cost and dielectric constant ranging from 2 to 10. Another material conductor is also used in HMICs as transmission line, matching network and stub. Copper and gold are most commonly used as conductors in HMIC design [3].

Hybrid MIC fabrication process is started after the circuit is designed. First, a mask is made for metallization layer on a thin sheet of glass or quartz. The metalized substrate is coated with photoresist, covered with mask, and exposed to a light source. Then, the substrate is etched to remove unwanted areas of metal and via holes are drilled. Finally, discrete components are soldered or wire-bonded to the conductors [3].

A microwave integrated circuit (MIC) designer has to decide which technology to use according to his needs before starting. At this point advantages and disanvantages of both technologies should be evaluated. Both monolithic and hybrid technologies have advantages and disadvantages. The key advantage of MMIC is small size. So, in many applications, MMIC technology is the inevitable solution for compactness. However, it is very expensive to start up a MMIC

fabrication; it requires great amount of investment. Conversely, in HMICs, cost of substrate and production is inexpensive, can be laid out, constructed and tested in limited time interval. It is also much easier to tune or repair a hybrid circuit after fabrication than it is for a MMIC. Thus, for applications requiring low noise figure, a tunable hybrid low noise amplifier (LNA) may be preferred. Due to the controlled parasitic, MMICs have good reproducibility. However, very limited choice of component is a disadvantage of MMIC technology. Table 1-3 summarizes the advantages and disadvantages of hybrid and monolithic microwave integrated circuit technologies.

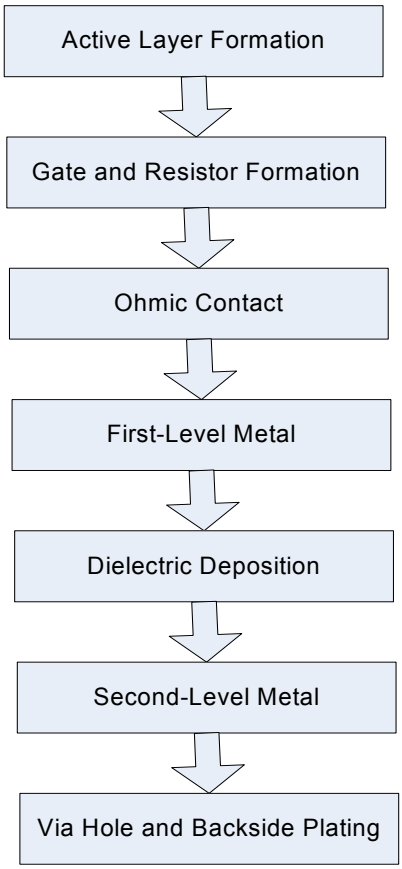


Figure 1-1: Typical MMIC fabrication process

Table 1-3: Comparison Between HMIC and MMIC Technologies

Property	**HMIC**	**MMIC**
Size and Weight	Large	Small
Starting Cost	Low	Very High
Production Cost	High	Low
Broadband Performance	Limited	Good
Reproducibility	Poor	Good
Reliability	Fair to good	Excellent
Operation Frequency	< 20 GHz	< 100 GHz
Tuning	Possible	Impossible
Mass Production	Impossible	Possible
Equipment cost	Low	High
Reparability	Possible	Impossible
Labor Intensive	Yes	No
Controlled Parasitic	No	Yes
Active Devices	Discrete	Deposited
Lumped Elements	Discrete / Deposited	Deposited
Distributed Elements	Microstrip or coplanar waveguide	Microstrip and / or coplanar lines
Interconnections	Wire bonded / Deposited	Deposited
Substrate	Insulator	Semiconductor
Debugging	Easy	Difficult

The critical disadvantage of hybrid technology is its large size. In the scope of this thesis, in order to eliminate this disadvantage, miniaturized techniques and their application in literature of hybrid microwave circuits are searched and presented with simulation and measurement results. A frequency modulated

continuous wave (FMCW) transceiver at center frequency 6 GHz with 1 GHz bandwidth was designed with hybrid microwave integrated circuit techniques. Discrete chip transistors are used and matching networks composed of interdigital capacitors and spiral inductors are designed. All design details and results will be given in the following parts.

In chapter 2, FMCW radar with its principles of operation is introduced. A brief history and its usage areas both for civil and military applications are explained. Range and velocity measurement techniques with their formulation are presented.

Chapter 3 is devoted on hybrid microwave circuits. Miniaturization techniques for HMICs, for which size consideration is a problem, are introduced. For this purpose, miniaturizing of hybrid coupler, radial and quarter wavelength stubs are presented with simulation and measurement results. Size reductions with the conventional ones are compared. Moreover, Interdigital capacitors and spiral inductors are examined. Their lumped element equivalents are formed and electromagnetic simulation results are compared with lumped element equivalent and analytic formulation results.

Chapter 4 focuses on FMCW transceiver design with hybrid circuit techniques which can be used as proximity sensor. Design and results of sub-parts; power amplifier, low noise amplifier, front-end structure, are presented separately.

Finally, Chapter 5 covers the main contributions achieved through out the thesis studies.

CHAPTER 2

BASICS OF FMCW RADAR

2.1. Introduction

Radar is an object detection system that uses electromagnetic waves to identify the range, altitude, direction, or speed of both moving and fixed objects such as aircraft, ships, motor vehicles, weather formations, and terrain. The detection and information gathering about a target is achieved by transmitting electromagnetic waves and receiving the scattered echo signals. Those signals used in radar systems can be pulsed or continuous wave.

In pulsed radars, a short burst of electromagnetic energy is transmitted. After transmission, radar starts waiting for the scattered echo signals. From the scattered echo signal the presence of the target can be detected. It is possible to measure the range of the target by measuring the time difference of the transmitted and the received signals. However, radars using un-modulated continuous waves (CW), the transceiver sends and receives signal continuously. Thus, such a CW radar cannot measure the time difference between transmitted and received signals. They can only measure velocity of the target. In order to measure the range with CW radars modulation is required. Frequency modulation is used in FMCW (Frequency-Modulated Continuous Wave) radars; changing frequency is the time mark which is used to determine the range information of the target. To measure the range, time difference of the transmitted and received signals, which is proportional to the frequency

difference between transmitted and received signals, is needed. This time difference can be easily determined by multiplication of transmitted and received signals. After the multiplication low frequency component is filtered out by low pass filtering.

Some important features of FMCW radars can be summarized as follows [6]:

- Small ranges can be measured and minimum range is comparable to the wavelength of the transmitted signal
- Can measure both range and velocity of target
- Results in small range measurement error
- Can measure small range changes
- Low energy consumption and small weight because of lacking high circuit voltages
- Having compact size, microwave block determines the dimensions of the radar

2.2. Principles of Operation

Frequency modulated continuous wave (FMCW) radar principles can be illustrated by two different block diagrams. The main difference of these block diagrams is the front-end structure used. The first one is shown in Figure 2-1 which uses two different antennas both for transmitting and receiving path. The second block diagram with one common antenna is illustrated in Figure 2-2. In this second topology the isolation between transmitted and received signals is achieved by a circulator which is a widely used microwave component in radar front-ends with single antenna. Instead of a circulator, a duplexer can be used. A duplexer is the network that permits a transmitter and receiver to use the same antenna, at or very near the same frequency. It is also possible to use a 3dB hybrid divider with a dual polarized antenna system which is shown in

Figure 2-3 [7]. In both topologies a reference signal of the transmitter is used in the mixer in order to get the signal with frequency difference of transmitted and received signals. This signal which is output of the mixer is called intermediate frequency (IF) signal. Signal processing system uses IF signal to extract range, velocity information and this information is shown on a kind of display.

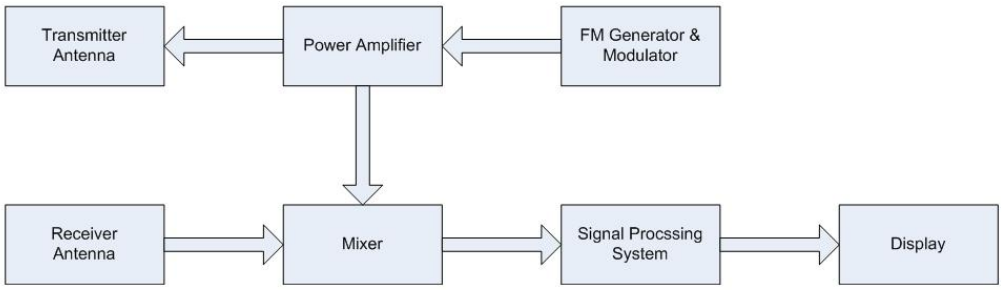


Figure 2-1: Basic block diagram of FMCW radar with two antennas

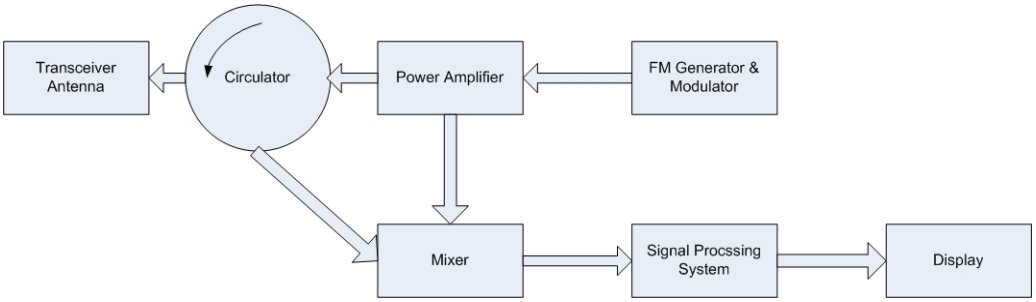


Figure 2-2: Basic block diagram of FMCW radar with one antenna

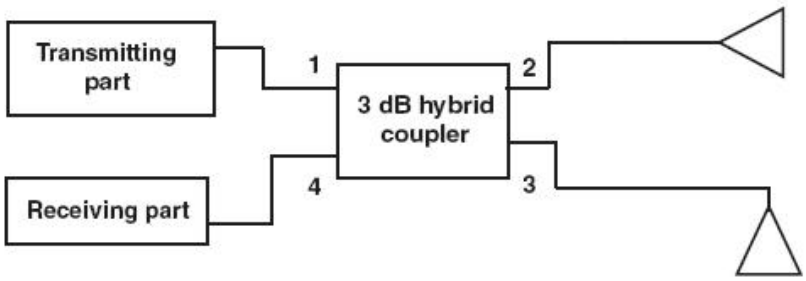


Figure 2-3: Front-end structure of FMCW radar with dual-polarized antenna

In FMCW radars transmitter frequency is changed continuously. This change is done with a periodic waveform which can be triangular, saw tooth, sinusoidal, etc. In Figure 2-4 a typical triangular frequency modulation for a fixed target is illustrated. In this illustration T is the time difference between transmitted and received signals. ΔF is the bandwidth, f_0 is the centre frequency, T_m is the modulation period and f_m is the modulation frequency of the FMCW signal. For a target at range R, the echo signal is shown with dotted line in Figure 2-4. So R can be expressed in terms of T as:

$$R = \frac{T \cdot c}{2} \tag{2.1}$$

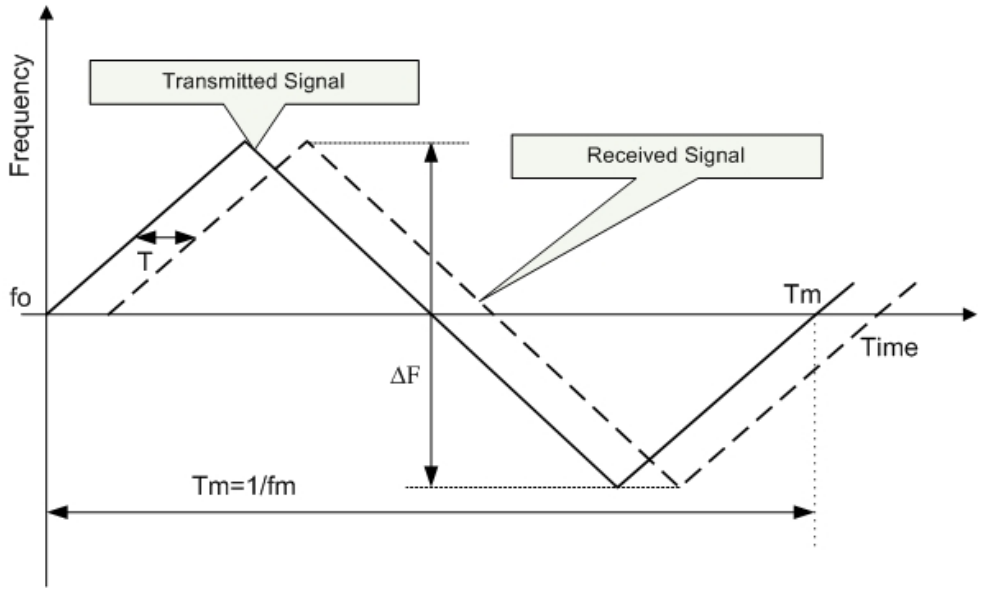


Figure 2-4: Triangular frequency modulation for transmitted and received signals

The transmitted and received signals are multiplied within a mixer and then high frequency term is filtered out. The remaining part is the signal with beat frequency f_b. For stationary targets with no Doppler shift, this beat frequency is the measure of range and $f_b = f_r$ where f_r is the beat frequency due to only target's range. Figure 2-5 shows the beat frequency of the triangular modulated signal in Figure 2-4.

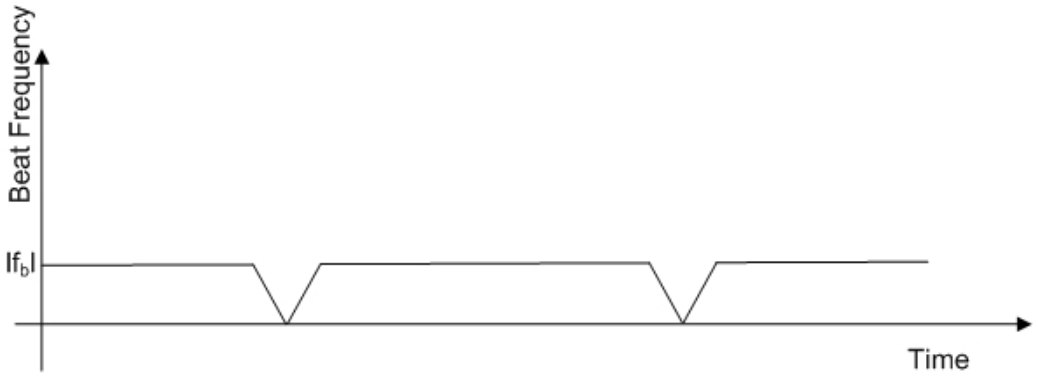


Figure 2-5: The beat frequency of triangular modulated signal

For a triangular modulation with modulation frequency f_m and bandwidth ΔF, the slope m_f of the transmitted waveform can be calculated as:

$$m_f = \frac{\Delta f}{1/2 f_m} = 2\Delta f \cdot f_m \tag{2.2}$$

The beat frequency can be calculated from the slope of Figure 2-4 as:

$$f_b = m_f \cdot T \tag{2.3}$$

Using (2.1), (2.2) and (2.3):

$$f_b = \frac{4R \cdot \Delta f \cdot f_m}{c} \tag{2.4}$$

From (2.4) range measurement R can be expressed as:

$$R = \frac{c \cdot f_b}{4\Delta f \cdot f_m} \tag{2.5}$$

For stationary targets range measure R is proportional with beat frequency f_b as seen in (2.5). However, for moving targets, beat frequency includes the Doppler

shift superimposed on it which is measure of velocity. The transmitted and received signals of triangular frequency modulation for Doppler case are shown in Figure 2-6. In this case, frequency of the received echo is shifted according to the relative direction of the target. Figure 2-7 shows the beat frequency of triangular frequency modulation for moving targets.

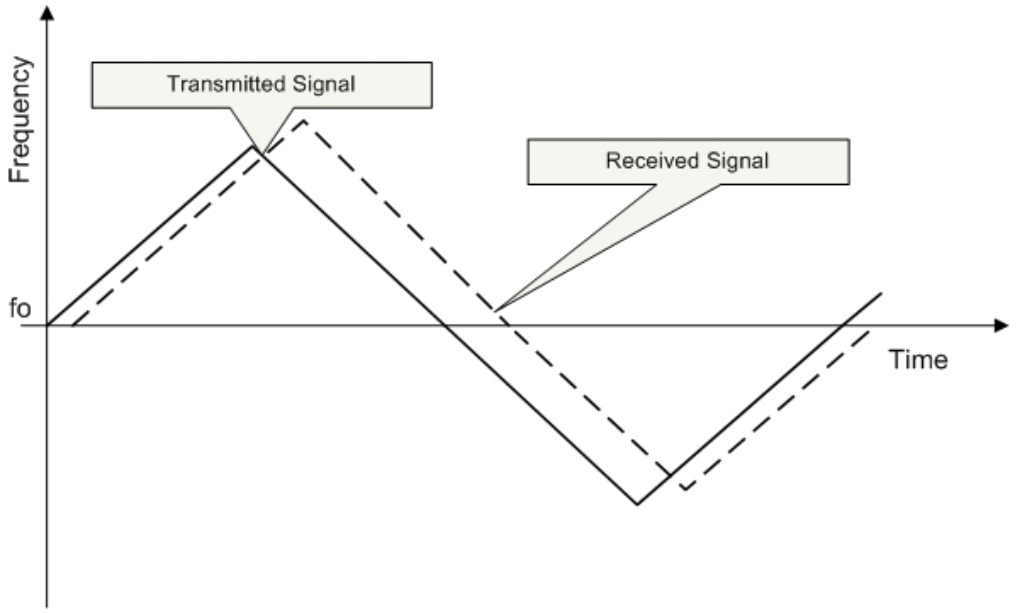


Figure 2-6: Triangular frequency modulation for transmitted and received signals with Dopper shift

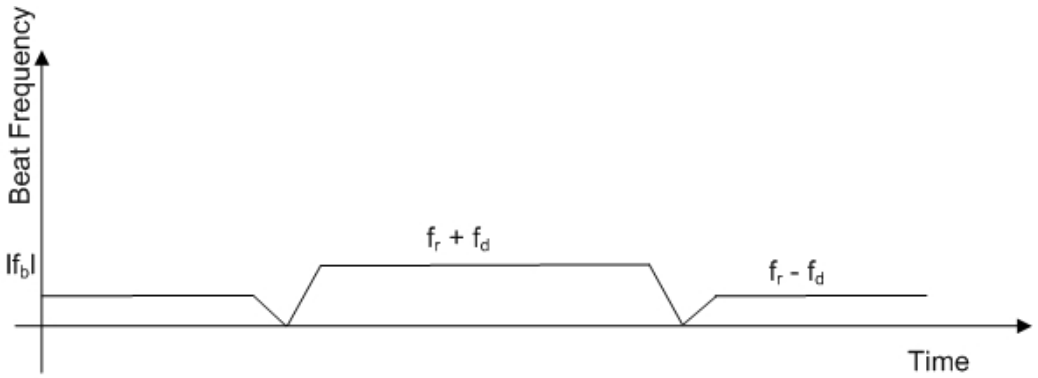


Figure 2-7: The beat frequency of triangular modulated signal with Doppler shift

The beat frequency is increased by Doppler shift on one cycle of modulation, while it is decreased same amount on the other cycle. Thus, two beat frequencies f_{b1} & f_{b2} can be defined as:

$$f_{b1} = f_r + f_d \tag{2.6}$$

$$f_{b2} = f_r - f_d \tag{2.7}$$

The beat frequency f_r for range can be found by averaging two beat frequencies:

$$f_r = \frac{f_{b1} + f_{b2}}{2} \tag{2.8}$$

Similarly, the Doppler frequency f_d can be obtained as:

$$f_d = \frac{f_{b1} - f_{b2}}{2} \tag{2.9}$$

The beat frequency that determines the range is proportional with modulation frequency f_m from equation (2.4). A constant K can be defined as $K = \frac{4\Delta f \cdot f_m}{c}$.

So, minimum beat frequency f_{bmin} can be defined as:

$$f_{b\min} = K \cdot R_{\min} \tag{2.10}$$

The beat frequency should satisfy $f_{b\min} > M \cdot f_m$ where M is an integer. So, IF signal f_b rests on harmonics of f_m. If a necessary isolation between transmitter and receiver is not satisfied, weak echo signal cannot be detected. Therefore, frequency of modulation should be chosen properly such that beat frequency corresponding to R_{min} is on higher harmonics of f_m.

The half-cycle of frequency modulation can be converted to frequency domain by applying discrete Fourier (DFT) or fast Fourier transforms (FFT). The FFT interval is: $T_f = \frac{T_m}{2}$

The beat frequency resolution is defined as:

$$\Delta f_b = \frac{1}{T_f} = 2 f_m \tag{2.11}$$

Using equation (2.5) range resolution ΔR can be defined as:

$$\Delta R = \frac{c}{4\Delta f \cdot f_m} \cdot \Delta f_b = \frac{c}{2\Delta f} \tag{2.12}$$

As can be seen from (2.12) range resolution is inversely proportional with frequency bandwidth of the transmitter. Therefore, for short range applications which require better resolution, higher bandwidth should be preferred. Another important topic for short range measurement is the measurement error. Measurement accuracy with one meter may be considered as good, but it is not for short range radar application. The accuracy depends on bandwidth of the signal and the signal-to-noise ratio (SNR) of the system. In addition to this theoretical inaccuracy, there exist errors due to circuit mismatches, transmitter leakage, device tolerances used.

If a counter is used, the total cycle count is an integer which gives rise to a step error or quantization error. The number of cycles N of beat frequency in a period of f_m is defined as:

$$N = \frac{< f_b >}{f_m} \tag{2.13}$$

Equation (2.5) can be expressed in terms of N as:

$$R = \frac{c \cdot N}{4\Delta f} \tag{2.14}$$

N is an integer number. So, R is the integer multiple of $\frac{c}{4\Delta f}$ and this will give rise to a quantization error equal to:

$$\delta R = \frac{c}{4\Delta f} \tag{2.15}$$

Equation (2.14) shows that measurement error is inversely proportional with

bandwidth of the transmitted FMCW signal. Therefore, especially for short range FMCW radars which require low measurement error, larger bandwidth should be preferred.

2.3. Brief History

The idea of using frequency modulated (FM) signals for range measurement is very old. In 1920s those signals were used for ionospheric research. The first patented work on frequency-modulated continuous wave (FMCW) radar was started in 1928 by J. O. Bentley [8]. Bentley's FMCW radar application was an airplane altitude indicating system. In this radar, the transmitted frequency was modulated with a triangular waveform using an electric motor rotating an adjustable capacitor. Reflected signal from the surface is absorbed by the receiver tuned to the frequency of transmitter. The time delay T between transmitted and received signals is used to measure altitude of the aircraft [6].

Industrial applications of FMCW radar began at the end of the 1930s with the use of ultrahigh frequency band. Signal processing after the mixer of those industrial FMCW radars was performed in a very low-frequency band which makes them very simple and reliable. The simplicity and reliability of FMCW radar applications are the main reasons of using this technique in radio altimeters in military aircraft during World War II, and afterward in civil aircraft. At present low-altitude FMCW radio altimeter is still used for both civil and military applications [6].

Most of the theoretical works on FMCW radar were published during a period from late 1940s to early 1960 [6]. In addition to variable time fuse and radio altimetry, FMCW radars have been developed for many applications in civil industry which are introduced in area of usage of FMCW radar part.

2.4. Area of Usage of FMCW Radar

FMCW radar has widely used both in civil and military applications. In the following sub-parts those most common applications are introduced.

2.4.1. Radio Altimeter

Radio altimeter is widely used in civil and military aircrafts to measure the altitude of the vehicle. Radio altimeter is one of the initial applications of FMCW radar. It serves as a tool to measure the distance to the ground which is very critical especially in low visibility conditions. This application makes the air vehicle to land safely.

2.4.2. Level Measuring Radar

Level measuring radar is used in liquid tanks in order to measure the level of the liquid in the tank. The transmitter of the sensor is placed on the cover of the tank. The beam is directed to the surface of the liquid and from the received signal the distance R from surface to top of the tank is measured. The total height of the tank H is known. Therefore, the level of the liquid L=H-R can be calculated.

2.4.3. Proximity Fuse

Proximity fuse is used to assure that the distance of the target is higher than a certain, predetermined value. The concept originated with British researchers and was developed under the direction of physicist Merle A. Tuve at the Hopkins University Applied Physics Laboratory.

2.4.4. Navigational Radar

One of the applications of FMCW radar is navigational radar for several kilometers. However, FMCW radar is most useful at short ranges, from tens to

hundreds of meters that can be used for surveillance of the sea or large river ports when vessels arrive under conditions of bad visibility. FMCW radar can be used not only to search the water surface of the port but also to measure range and relative speed of any targets within the port [6].

2.4.5. Vehicle Collision Warning System

Vehicle collision warning systems have been developed in response to the substantial traffic growth in cities. In these systems four sides of the vehicle are covered by front, tail, two side mirror radars. The front radar has a range of 300m and provides continuous measurement of range and relative velocity of targets. When a danger, which is determined by measured range and relative velocity, is encountered, the brake system of the vehicle is activated. Tail and side mirror radars operate with same principle, but they are generally used for parking purposes.

2.4.6. Precision Range Meter for Fixed Targets

In precision range meters, multi frequency CW using phase processing of the reflected signal is used. It can measure range up to tens of kilometers with a relative error of the order 10^{-6} by using this technique. However, the disadvantage of this kind of radar is that it can only measure the distance of moving targets [6].

2.4.7. Measurements of Very Small Motions

A typical example of small motion measurement is the observation of vibrations of various components of machines. For such measurement, a device, which has no physical contact with the vibrating component, is needed.

CHAPTER 3

HYBRID MICROWAVE INTEGRATED CIRCUITS

Hybrid microwave integrated circuit (HMIC) is a circuit technique in which all discrete active and passive die or packaged components are connected to each other on a common substrate by soldering, air or wire bonding. Detailed information and comparison with MMIC are given in chapter 1. It is obvious from those comparisons that size of HMIC is bigger than that of MMIC. Therefore, size reduction is needed in some applications that require small size. Through out this chapter, miniaturization techniques of some HMIC will be introduced.

In the following sub-parts, miniaturization techniques applied on hybrid couplers are introduced with measurement results. Moreover, miniaturization of stubs is examined and especially for radial stubs size reduction is achieved. Furthermore, introductory information on fractals is given. Some parts are devoted on spiral inductors (SI) and interdigital capacitors (IDC), by which series size reduction can be achieved when compared with packaged discrete ones and parasitic effect of package can be reduced for HMICs. Equivalent circuit parameters are introduced and simulation results are given.

3.1. Miniaturization of Microwave Hybrid Couplers

Miniaturization of microwave circuit is an important issue for design engineers. In both industrial and military applications, small size is a design requirement.

This requirement forces the designer to develop techniques for miniaturization of microwave circuits. In this part, some useful miniaturization techniques for hybrid couplers are discussed; analysis, simulation and measurement results are presented. Moreover, some of these techniques will be applied to an FMCW range sensor transceiver in chapter four.

3.1.1. Basics of Couplers

Couplers are passive circuits widely used in radio and microwave frequencies to measure forward and reverse power levels, in cases such as to monitor VSWR, to control gain of a power amplifier, etc.

In RF and microwave frequencies coupling of power can be achieved with different coupling mechanisms. For relatively low frequencies where lumped elements such as capacitors and inductors can work, lumped couplers can be implemented. However, for high frequencies where resonance frequencies of lumped elements become a series problem, couplers can be achieved and implemented with microstrip and strip transmission line technology.

A general coupling network is shown in Figure 3-1. It is a four port network. Power is injected from input port and transferred through direct port. Part of this input power is coupled through coupled port. The fourth port is isolated which is critical for directional couplers where both forward and reverse is to be discriminated. P_1, P_2, P_3, P_4 shows the power levels entering or leaving the related ports. The ratio between those power levels determines the performance of the coupler.

Coupling, C, is the ratio of P_3 and P_1 in case of all ports are match terminated. It can be expressed in decibel as:

$$Coupling(dB) = 10\log\frac{P_3}{P_1} \tag{3.1}$$

Isolation and directivity, D, are the key parameters of directional couplers and they can be expressed as:

$$Isolation(dB) = 10\log\frac{P_4}{P_1} \tag{3.2}$$

$$Directivity(dB) = 10\log\frac{P_4}{P_3} \tag{3.3}$$

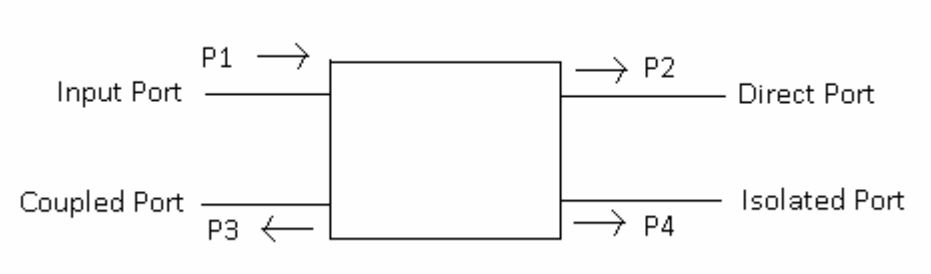


Figure 3-1: A General Coupling Network

There exist different distributed coupler types with microstrip and strip transmission line technology such as coupled line couplers, branch-line and rat race couplers. The choice between these couplers depends on needs of the designer. Parameters such as coupling ratio, bandwidth and phase difference between coupled ports are the critical selection criteria of the designer. These couplers can be analyzed by even and odd mode analyses.

A commonly used type is the coupled line couplers. Figure 3-2 shows the schematic of a coupled line coupler. Especially for applications requiring small coupling ratio in order to monitor power and measure voltage standing wave ratio (VSWR) coupled line couplers can be used. Length and spacing between coupled lines determines the coupling ratio and directivity. However, coupling ratio increases with increasing frequency. Therefore, for a specific frequency band a flat coupling ratio can be achieved with an equalizing network.

In planar transmission line technology, it is difficult to obtain a high coupling ratio between coupled lines because of very small spacing requirement. Therefore, a tight coupling, such as 3 dB, can be achieved with other types of

couplers. These tight couplers, whose sample uses are in balanced mixers and amplifiers, are branch-line couplers, rat-race couplers, lange couplers, and tandem couplers. All these coupler types are implemented using transmission lines whose lengths are around quarter-wavelength at the center frequency. Because of this reason the size of these couplers are comparably large. To be able to implement in integrated circuit technology, miniaturization techniques are developed.

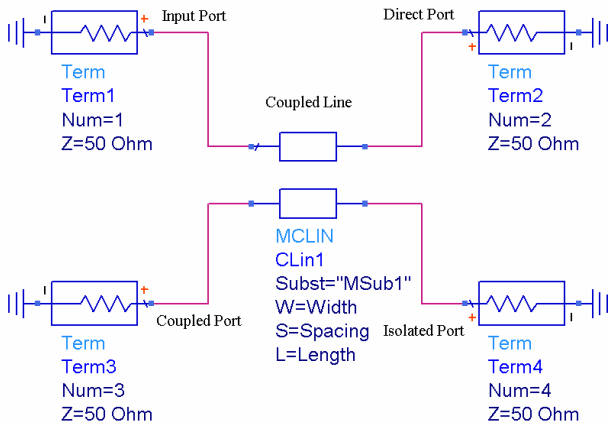


Figure 3-2: Schematic of a Coupled Line Coupler

In the following sub-parts, design, simulation and measurement results of branch-line coupler, miniaturized branch-line coupler and slot-coupled wideband coupler will be presented.

3.1.2. Branch-Line Coupler

Branch-line coupler is a four port network. The input power is divided into two ports with 90° phase difference and the fourth port is isolated from other ports. Figure 3-3 shows the layout of a branch-line coupler. Parallel and series branches are all quarter wavelength. Because of these quarter wavelength branches, branch-line coupler is not suitable for wideband applications. In order to divide input power into two equal amplitudes, the characteristic impedances of the parallel, Z_{0p}, and the series, Z_{0s}, branches must be Z_0 (reference

impedance) and $Z_0 / \sqrt{2}$, respectively, [3] which are obtained by even and odd mode analyses.

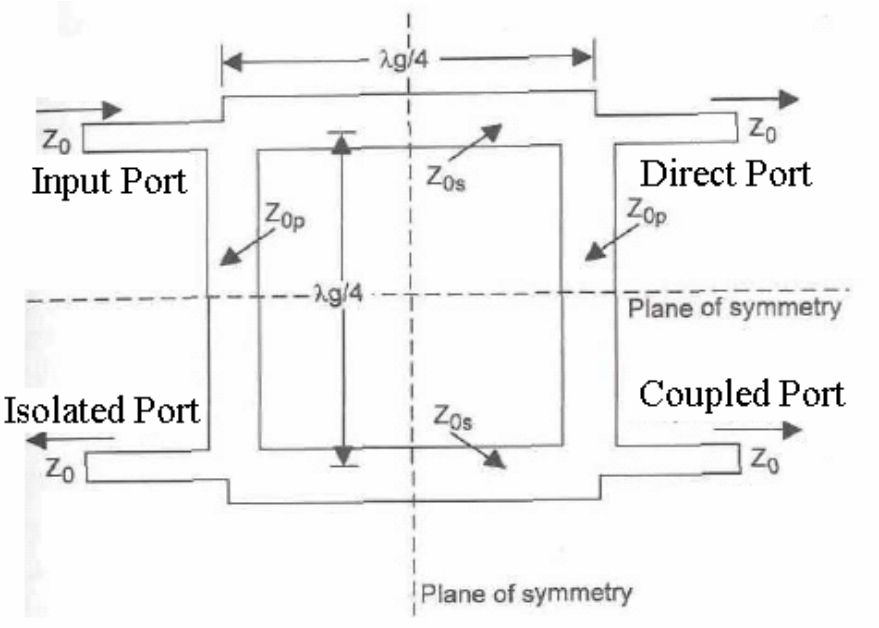


Figure 3-3: Layout of a Branch-Line Coupler

An ideal branch-line coupler shows perfect match at all ports and direct and coupled ports are equal in magnitude with 90° phase difference. S-parameters of an ideal branch-line coupler are given in (3.4).

$$S = \begin{bmatrix} 0 & -j\frac{Z_{os}}{Z_o} & -\frac{Z_{os}}{Z_{op}} & 0 \\ -j\frac{Z_{os}}{Z_o} & 0 & 0 & -\frac{Z_{os}}{Z_{op}} \\ -\frac{Z_{os}}{Z_{op}} & 0 & 0 & -j\frac{Z_{os}}{Z_o} \\ 0 & -\frac{Z_{os}}{Z_{op}} & -j\frac{Z_{os}}{Z_o} & 0 \end{bmatrix} \quad (3.4)$$

3 dB hybrid couplers such as branch-line coupler are widely used in balanced amplifier design in order to get matched input. However, especially at low frequencies of microwave band such as 1-2 GHz, size consideration is a critical issue. Due to the quarter wavelength branches of branch-line coupler, at low frequencies reduction of size become essential. In following parts some of techniques to reduce size of a branch-line coupler will be presented. In order to

compare with real size of a branch-line coupler, a standard branch-line coupler is designed on Rogers 4003 substrate (h=0.8mm). The dielectric constant ε_r is 3.38 and loss tangent is 0.0021 (at 10GHz). The center frequency is chosen as 1060MHz.

Figure 3-4 shows the schematic of the designed branch-line coupler. The lengths of quarter wavelength branches are 41.5mm each. These lengths will be reference for reduced size designs in the following parts.

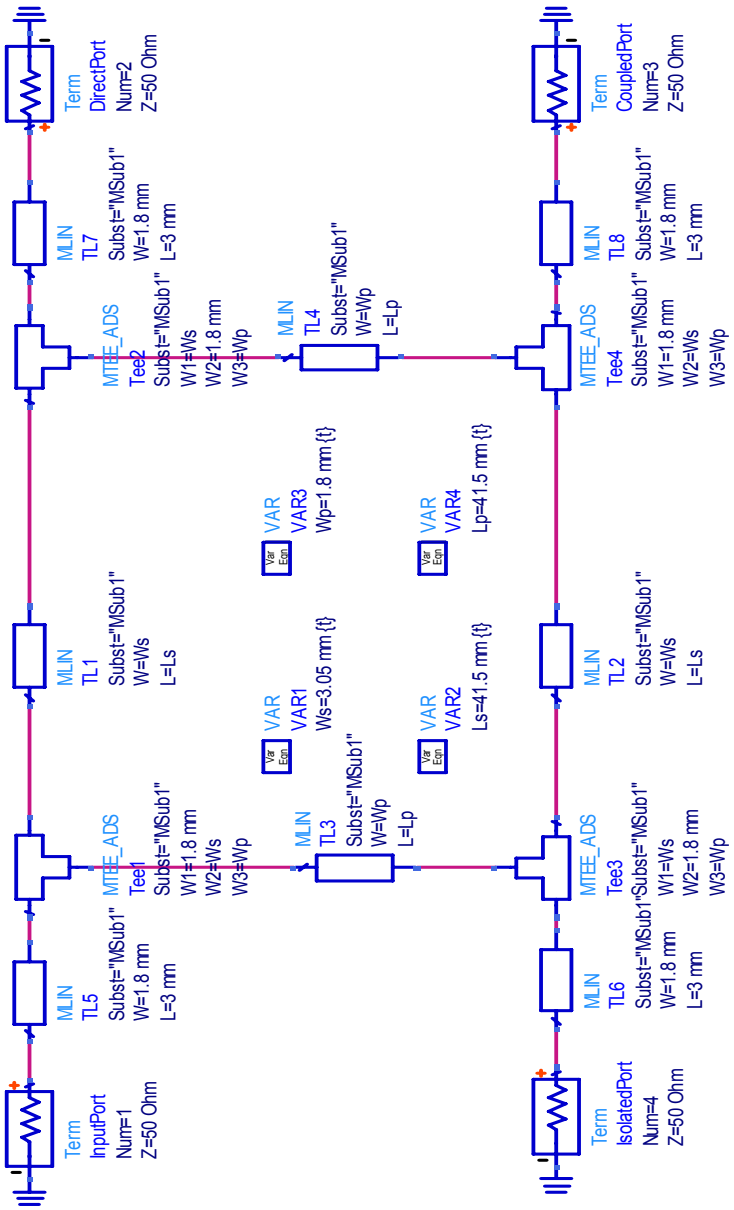


Figure 3-4: Schematic of Branch-Line Coupler at f=1060MHz

Figure 3-5 shows the simulation results of designed branch-line coupler. The results indicate that an ideal 3 dB division is not possible because of microstrip and dielectric losses. It is also notable from results that branch-line coupler is suitable only for narrow band applications.

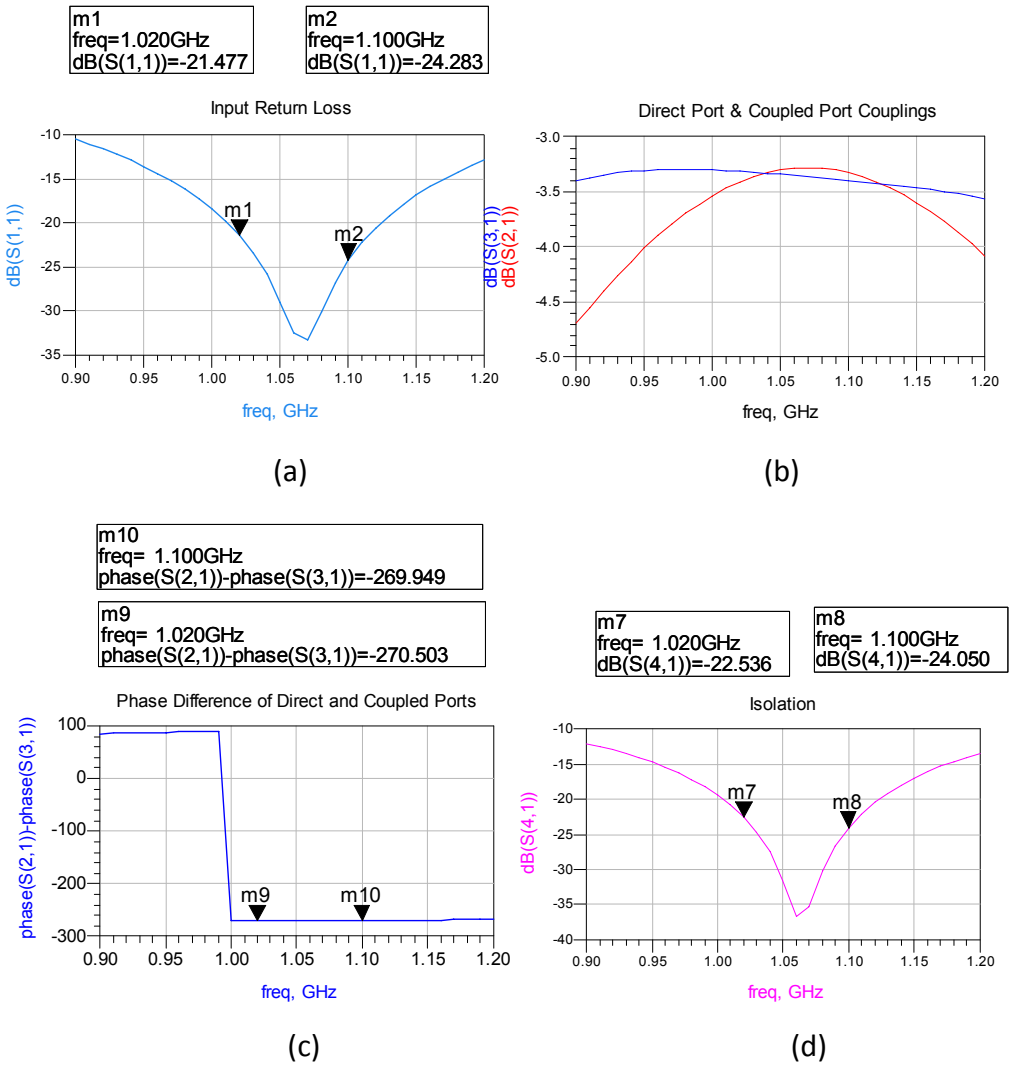


Figure 3-5: Simulation Results of Branch-Line Coupler at Center Frequency 1060MHz (a) Input Reflection (b) Direct and Coupled Port Transmission (c) Phase Difference of the Output Ports (d) Isolation

3.1.3. Branch-Line Coupler With Dual Transmission Lines

The branch-line coupler is composed of quarter wavelength branches. These branches are long for low frequencies. However, especially for portable systems compact solutions are needed. Therefore, size shrinkage becomes an important figure of merit for development. At that point, using dual transmission lines to replace quarter wavelength branches of branch-line coupler can be proposed as a technique of miniaturization [9].

A quarter wavelength transmission line can be represented with dual transmission line as in Figure 3-6. Dual transmission lines have different characteristic impedances (Z_1, Z_2) and electrical lengths (θ_1, θ_2) and satisfies $\theta_2 < 90° < \theta_1$.

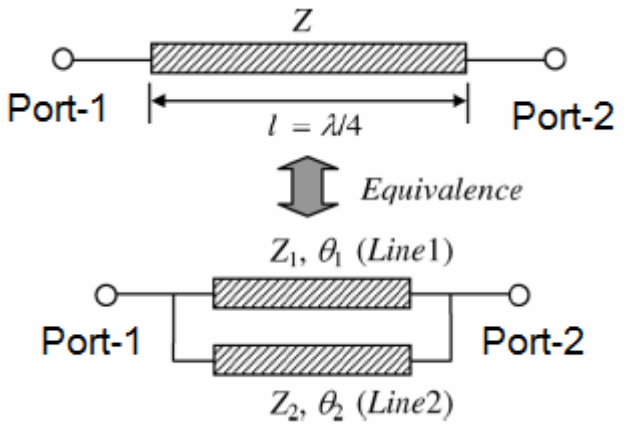


Figure 3-6: Dual Transmission Line Equivalent of Quarter Wavelength Transmission Line

The analytical formulation of parameters of dual transmission line can be derived by equating the ABCD parameters of quarter wavelength transmission line to dual transmission line. ABCD matrices can be expressed as:

(3.5)

$$\begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix}_{Line1} = \begin{bmatrix} \cos\theta_1 & jZ_1 \sin\theta_1 \\ jY_1 \sin\theta_1 & \cos\theta_1 \end{bmatrix} \quad (3.6)$$

$$\begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix}_{Line2} = \begin{bmatrix} \cos\theta_2 & jZ_2 \sin\theta_2 \\ jY_2 \sin\theta_2 & \cos\theta_2 \end{bmatrix} \quad (3.7)$$

After paralleling line 1 and line 2 and equating the result to ABCD parameters of quarter wavelength transmission line, following equations can be obtained.

$$A = \frac{A_1 B_2 + A_2 B_1}{B_1 + B_2} \quad (3.8)$$

$$B = \frac{B_1 B_2}{B_1 + B_2} \quad (3.9)$$

$$C = \frac{(A_2 - A_1)(D_1 - D_2) + (B_1 - B_2)(C_1 + C_2)}{B_1 + B_2} \quad (3.10)$$

$$D = \frac{D_1 B_2 + B_1 D_2}{B_1 + B_2} \quad (3.11)$$

Similar equations can be obtained by equating second parts of matrices in (3.5), (3.6), (3.7) as:

$$Z_1 = Z \frac{\cos\theta_2 - \cos\theta_1}{\sin\theta_1 \cos\theta_2} \quad (3.12)$$

$$Z_2 = -Z \frac{\cos\theta_2 - \cos\theta_1}{\cos\theta_1 \sin\theta_2} \quad (3.13)$$

$$\frac{Z_1}{Z_2} = -\frac{\tan\theta_2}{\tan\theta_1} \quad (3.14)$$

For a 50Ω system, impedances of series and parallel quarter wavelength branches are 35.4Ω and 50Ω respectively. In order to reduce the size, dual transmission line approach can be used. The layout of modified branch-line coupler with dual transmission lines is shown in Figure 3-7. For this design,

again 1060 MHz is chosen as center frequency. The substrate Rogers4003 is used. For a minimum line width of 0.2 mm, maximum characteristic impedance on microstrip is 126Ω.

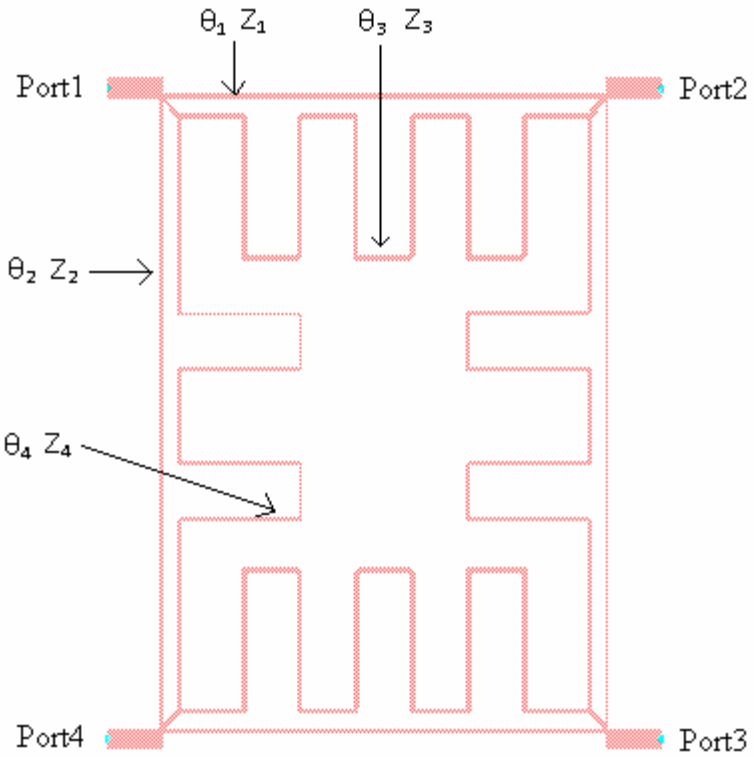


Figure 3-7: Layout of Branch-Line Coupler with Dual Transmission Lines

The electrical lengths of series branches of dual transmission lines θ_1, θ_3 are selected as 45° and 135° respectively. Then, corresponding characteristic impedances Z_1, Z_3 can be determined by using equations (3.12) and (3.13) as Z_1= Z_3= 100Ω. Similarly, by setting electrical lengths of parallel branches of dual transmission lines θ_2, θ_4 as 65° and 115°, respectively, characteristic impedances Z_2, Z_4 are 110,3Ω [9].

The ADS (Advanced Design System) Momentum EM simulation and measurement results of designed dual transmission line branch-line coupler are presented in Figure 3-8 and Figure 3-9 respectively. It is notable from results that input return loss, coupling ratios, isolation and phase balance of measurement are congruent with EM simulation results. On the other hand, these results are also compatible with the results of quarter wavelength

branch-line coupler. As a final measurement of performance, it is essential to give total loss of the coupler which is given in Figure 3-10. The total loss of this designed coupler is lower than 0.3 dB, which is low enough for a 3 dB coupler.

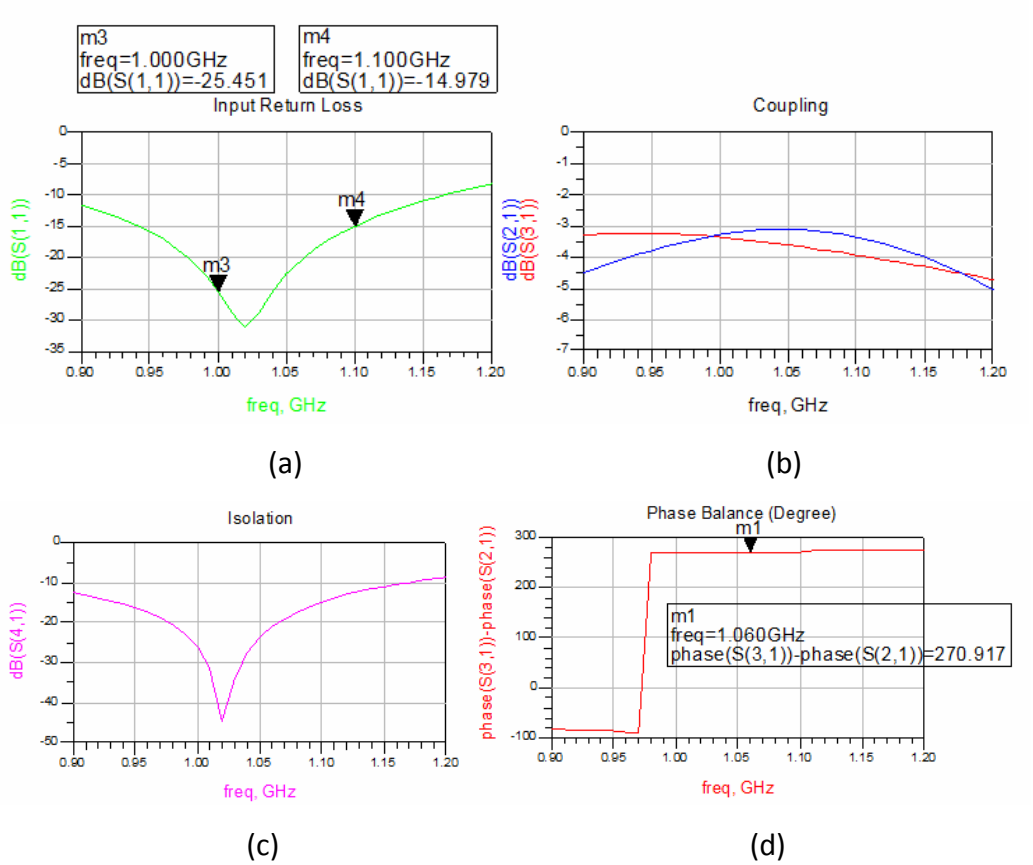


Figure 3-8: EM Simulation Results of Dual Transmission Line Branch-Line Coupler (a) Input Reflection (b) Direct and Coupled Port Transmission (c) Isolation (d) Phase Difference of the Output Ports

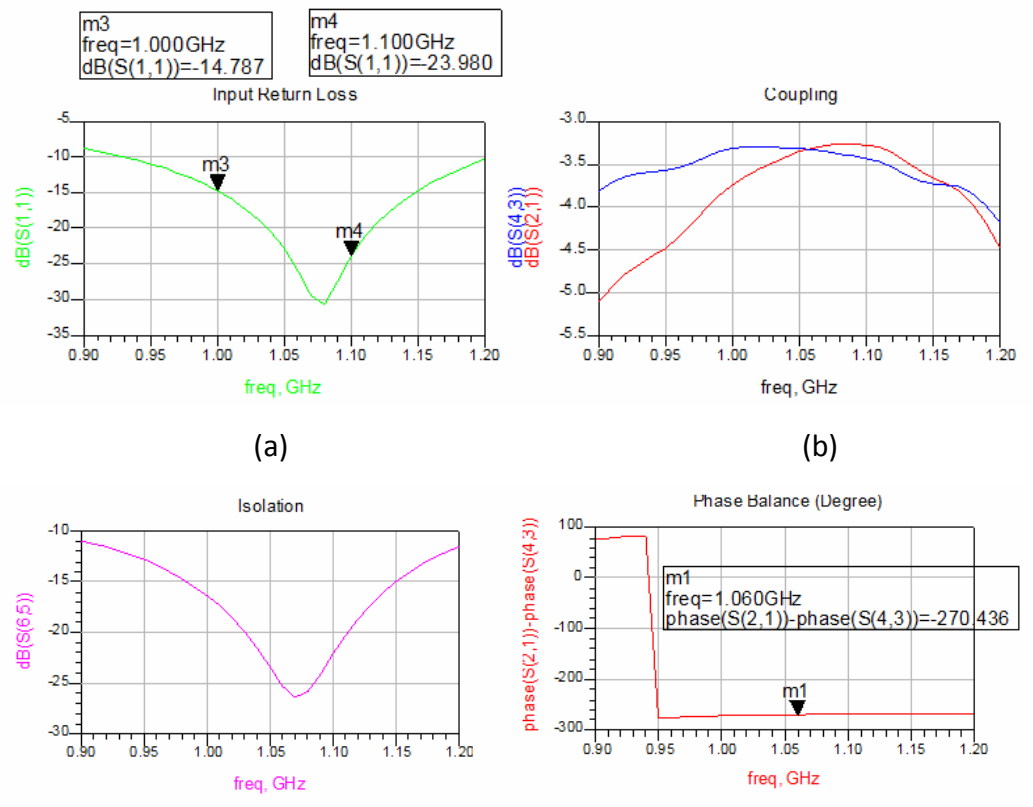


Figure 3-9: Measurement Results of Dual Transmission Line Branch-Line Coupler (a) Input Reflection (b) Direct and Coupled Port Transmission (c) Isolation (d) Phase Difference of the Output Ports

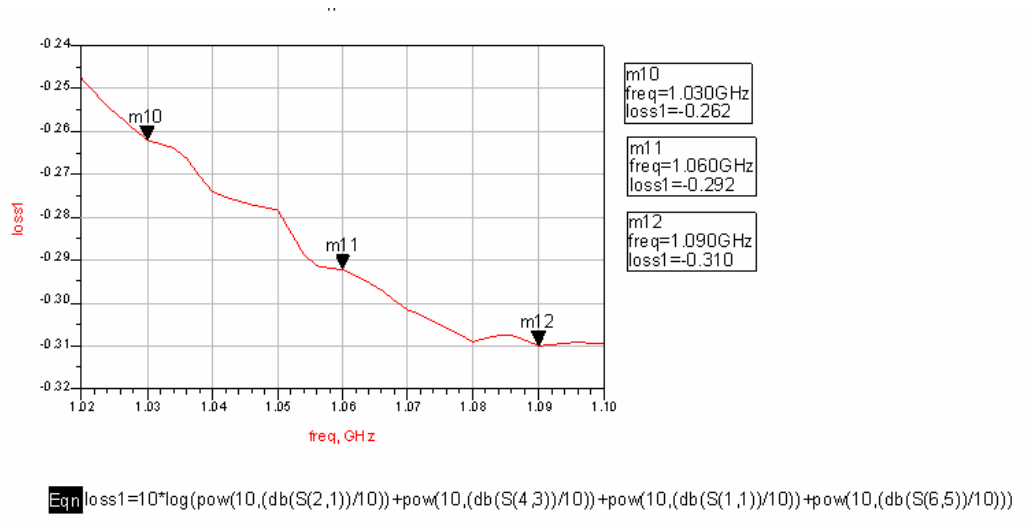
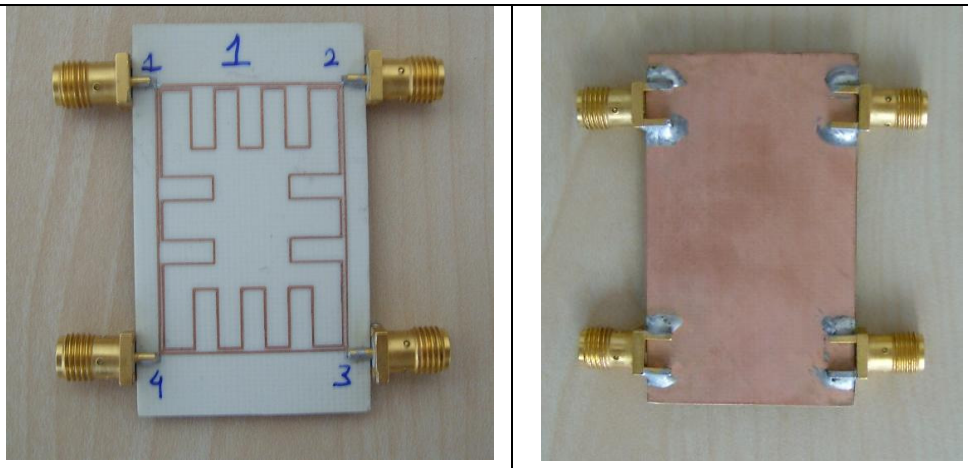


Figure 3-10: Total Loss of Dual Transmission Line Branch-Line Coupler

The photograph of the dual transmission line branch-line coupler is given in Figure 3-11. The dimension of this new designed coupler is measured as 24mm

length and 39mm width. When compared with standard branch-line coupler, a 45 % reduction in size is achieved.



(a) (b)

Figure 3-11: Photograph of Branch-Line Coupler with Dual Transmission Lines, (a) Top view (b) Bottom view

3.1.4. Branch-Line Coupler With Shunt Connected Capacitors

Another miniaturization technique of branch-line coupler is to represent the quarter wavelength branches with a short transmission line with shunt connected lumped elements on both ends. The quarter wavelength transmission line and its equivalent with shunt capacitors are shown in Figure 3-12. This equivalent circuit can also be converted into pure lumped elements by representing short line with an inductor. In Figure 3-12 (a), Z is the characteristic impedance of quarter wave section and in (b) Z_1 and θ_1 are characteristic impedance and electrical length of equivalent short line. Moreover, C is the shunt connected capacitor at both ends of short line.

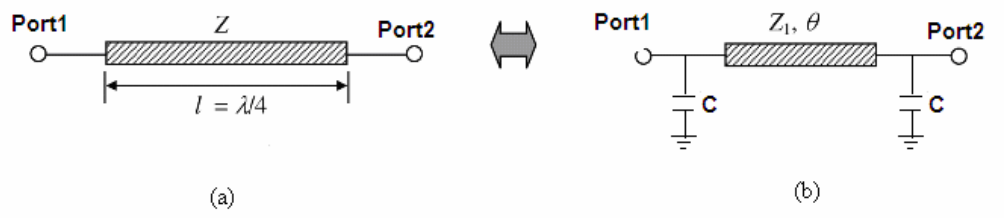


Figure 3-12: (a) Quarter Wavelength Transmission Line (b) Reduced Size Equivalent

The values of Z_1, θ and C can be determined by equating ABCD matrices of quarter wave section and its equivalent. The ABCD matrix of quarter wave is given in (3.5). The ABCD matrix of equivalent circuit can be expressed by cascading ABCD matrices of capacitors and short line as [10]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ jwC & 1 \end{bmatrix} \cdot \begin{bmatrix} \cos\theta & jZ_1 \sin\theta \\ j\dfrac{\sin\theta}{Z_1} & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ jwC & 1 \end{bmatrix} \tag{3.15}$$

$$= \begin{bmatrix} \cos\theta & wCZ_1 \sin\theta \\ j\dfrac{\sin\theta}{Z_1} + 2jwC\cos\theta - j(wC)^2 Z_1 \sin\theta & \cos\theta - wCZ\sin\theta \end{bmatrix} \cdot \begin{matrix} \\ jZ_1 \sin\theta \\ \\ \end{matrix} \tag{3.16}$$

By equating (3.5) and (3.16) Z_1, θ and C are found as:

$$Z_1 = \frac{Z}{\sin\theta} \tag{3.17}$$

$$wC = \frac{\cos\theta}{Z} \tag{3.18}$$

In this miniaturization technique, again Rogers 4003 substrate is chosen in order to be consistent. If the ratio of Z_1/Z is chosen as 2 for 50Ω system, characteristic impedance of new short line for parallel branch Z_1 is 100Ω. In this case electrical length of parallel short line can be calculated as:

$$\theta = \sin^{-1}(\frac{Z}{Z_1}) = \sin^{-1} 0.5 = 30°$$

The corresponding capacitor value can be calculated by using (3.18) at center frequency 1060 MHz as:

$$C = \frac{\cos 30}{50 \cdot 2\pi \cdot 1060 \cdot 10^6} = 2.6pF$$

The same procedure can be repeated for series branch with 35.4Ω

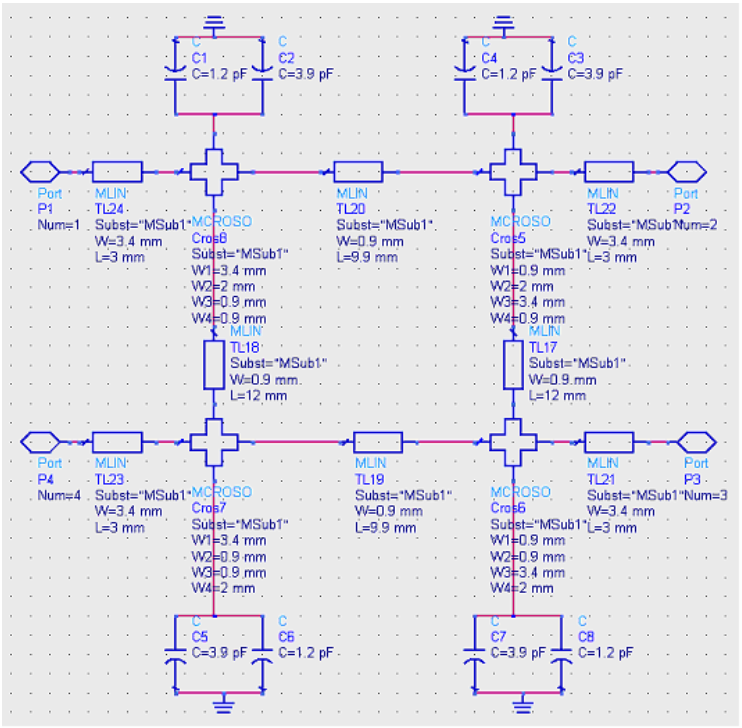
characteristic impedance of coupler and following results are obtained:

$$Z_1 = 100\Omega$$

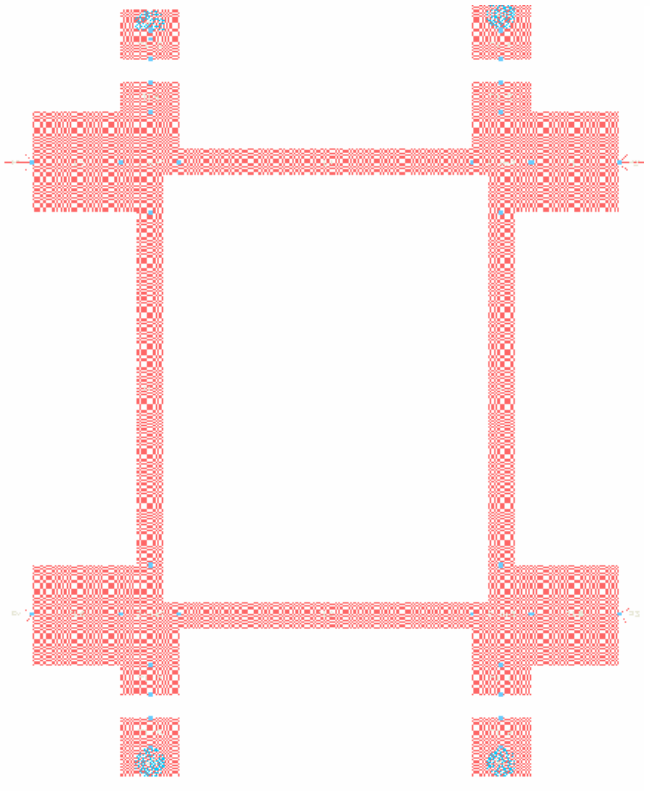
$$\theta = \sin^{-1}(\frac{Z}{Z_1}) = \sin^{-1} 0.354 = 20.7°$$

$$C = \frac{\cos 20.7}{35 \cdot 2\pi \cdot 1060 \cdot 10^6} = 4\,pF$$

These design parameters are used in ADS. The schematic and layout of branch-line coupler with shunt connected capacitors is given in Figure 3-13. After optimization in circuit simulation, design parameters, length and width of lines and capacitance values, are slightly changed. Final values are shown in Figure 3-13 (a).



(a)

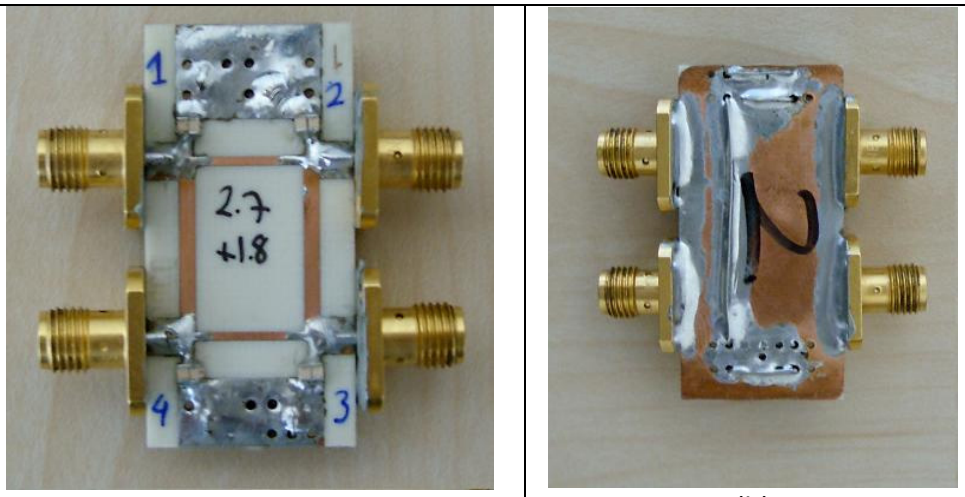


(b)

Figure 3-13: (a) ADS Schematic (b) Layout of Branch-Line Coupler with Shunt Connected Capacitors

The corresponding EM simulation by using the S-parameters of ATC 700A package capacitors and measurement results of the design are given in Figure 3-15 and Figure 3-16, respectively.

Finally, the lengths of branches are 13mm and 23mm, which mean that a reduction of 83% is achieved without considerable degradation in electrical performance. The implemented design photograph is given in Figure 3-14. In order to compare total loss with dual transmission line technique, loss calculation is shown in Figure 3-17. When compared with the loss of dual transmission line case, both has approximately the same loss characteristic.



(a) (b)

Figure 3-14: Photograph of Branch-Line Coupler with Shunt Connected Capacitors, (a) Top view (b) Bottom view

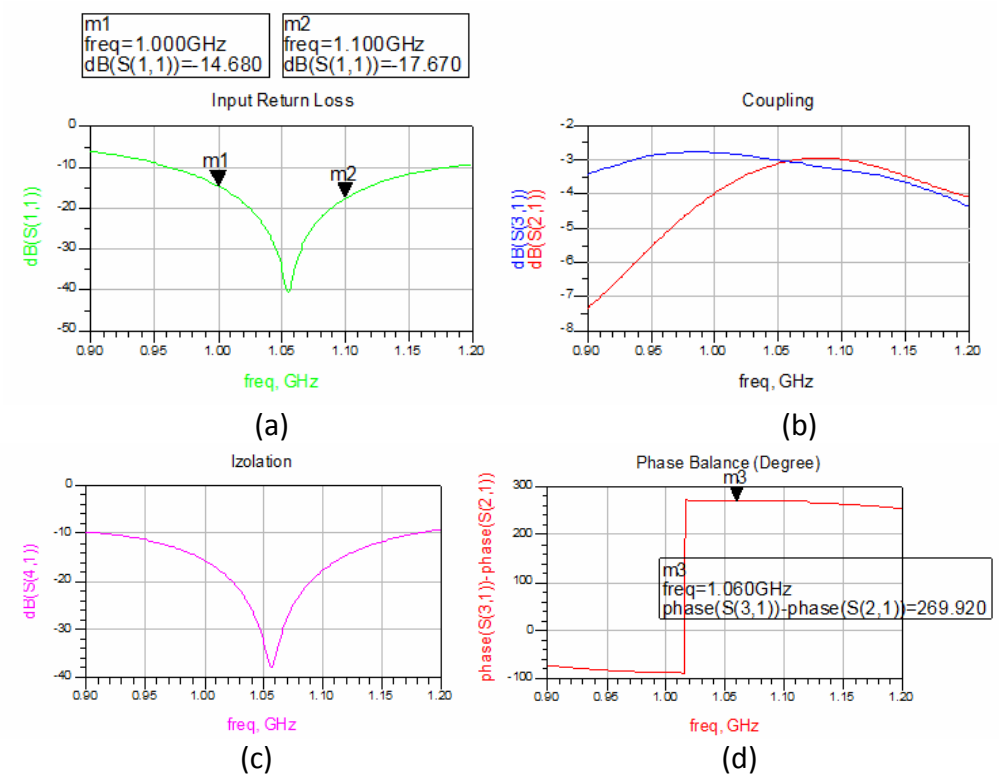


Figure 3-15: EM Simulation Results of Branch-Line Coupler with Shunt Connected Capacitors, (a) Input Reflection (b) Direct and Coupled Port Transmission (c) Isolation (d) Phase Difference of the Output Ports

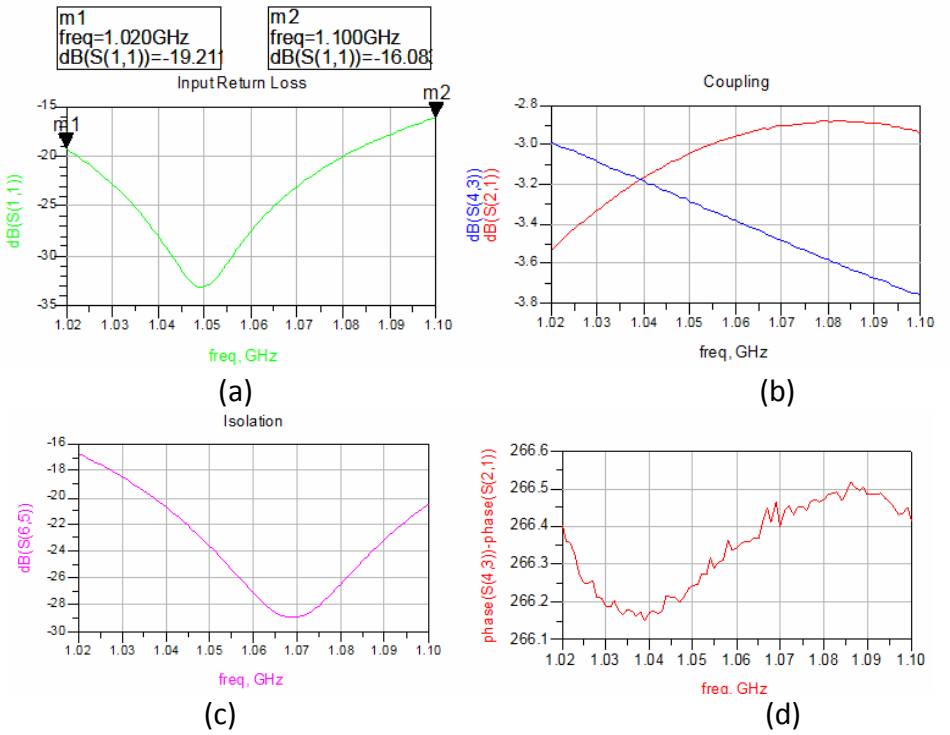


Figure 3-16: Measurement Results of Branch-Line Coupler with Shunt Connected Capacitors, (a) Input Reflection (b) Direct and Coupled Port Transmission (c) Isolation (d) Phase Difference of the Output Ports

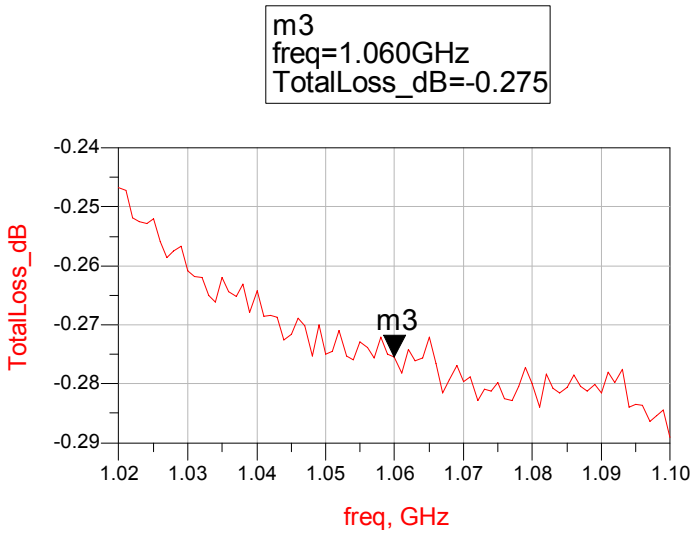


Figure 3-17: Total Loss of Branch-Line Coupler with Shunt Connected Capacitors

3.1.5. Slot-coupled Wideband Coupler

Vertical microstrip-microstrip transition is essential to build compact microwave circuits for multilayer designs. In literature vertical transition is extensively studied and two methods for transition are widely preferred. These methods are via-hole and aperture-coupled transitions [11-15]. The studies show that the former one has drawbacks such as high insertion loss for high frequencies and narrow bandwidth. The latter method is used to design directional couplers and filters [16-17]. In this part, 3 dB hybrid directional coupler applications by using aperture coupled transitions will be examined for a wideband 3-10 GHz. Figure 3-18 shows the layout of this 3 dB hybrid coupler. The transition area can be an elliptical or circular patch both at top and bottom layers.

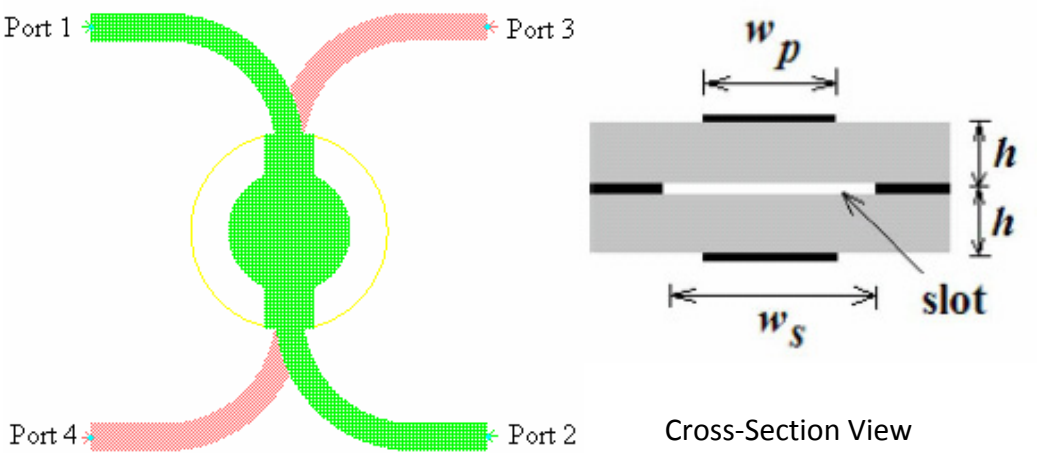


Figure 3-18: Simulated Layout of Aperture Coupled Directional Coupler

ADS is again used in EM simulations. In order to get the desired performance in 3-10 GHz band on Rogers 4003 substrate, diameter of the slot is optimized in electromagnetic simulation. These EM simulation results are shown in Figure 3-19.

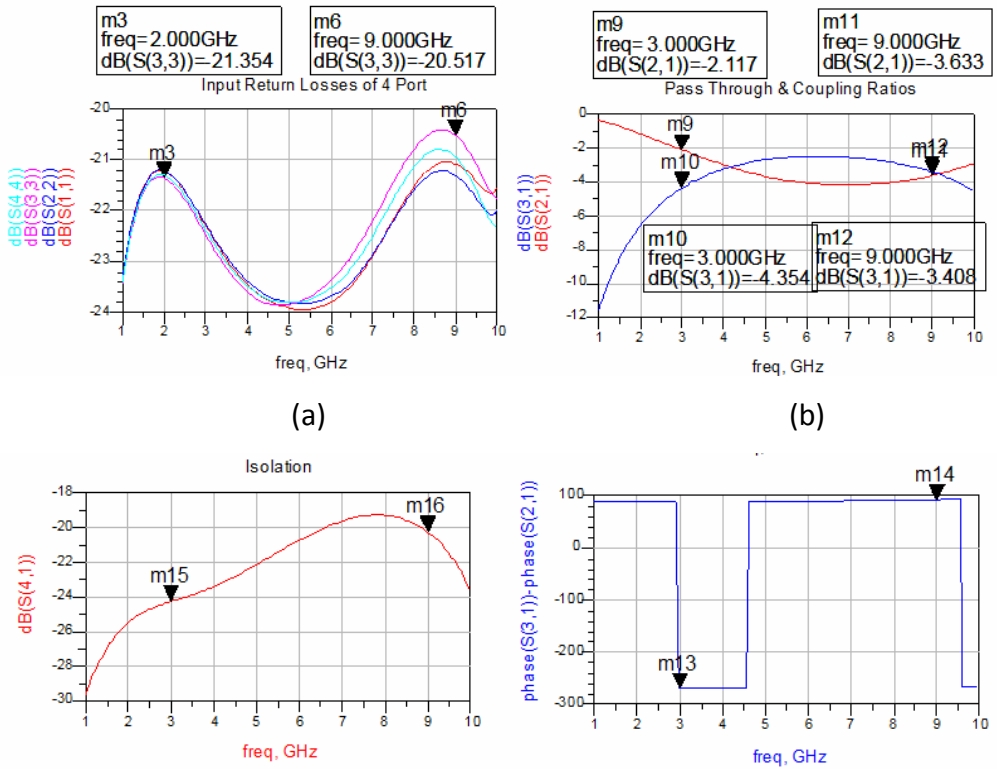


Figure 3-19: EM Simulation Results of 3 dB Directional Coupler, (a) Input Reflection (b) Direct and Coupled Port Transmission (c) Isolation (d) Phase Difference of the Output Ports

In Figure 3-21 and Figure 3-22, measured performance of 3 dB hybrid is presented. These results show that input return loss is better than -10dB, isolation is higher than 15dB and total loss is less than 2 dB in 3-10 GHz frequency band. However, for the through and coupling ratios, the bandwidth is narrower than 3-10 GHz. This is because the top and bottom substrates are attached with screws and nuts as can be seen in the photograph of implemented design Figure 3-20. A better performance could be obtained by sticking substrates each other with a conductive adhesive.

(a) (b)

Figure 3-20: Photograph of Aperture-Coupled Directional 3-dB Hybrid Coupler, (a) Top view (b) Bottom view

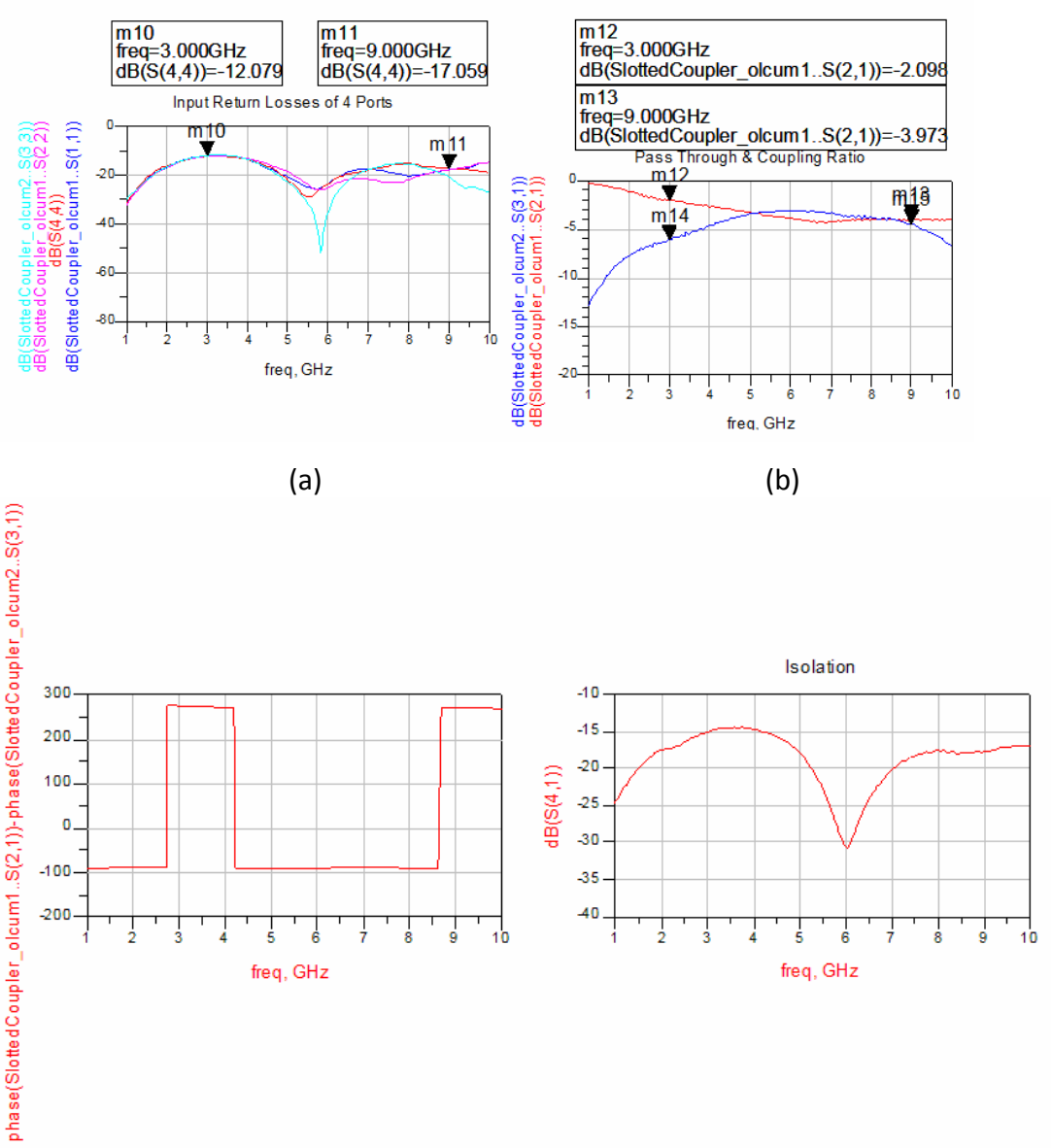


Figure 3-21: Measurement Results of 3 dB Directional Coupler, (a) Input Reflection (b) Direct and Coupled Port Transmission (c) Isolation (d) Phase Difference of the Output Ports

Finally, dimensions of the implemented coupler are 30 mm in width and 21 mm in length. For a wideband application, these dimensions are considered to be small enough for the designer complaining about not having enough size.

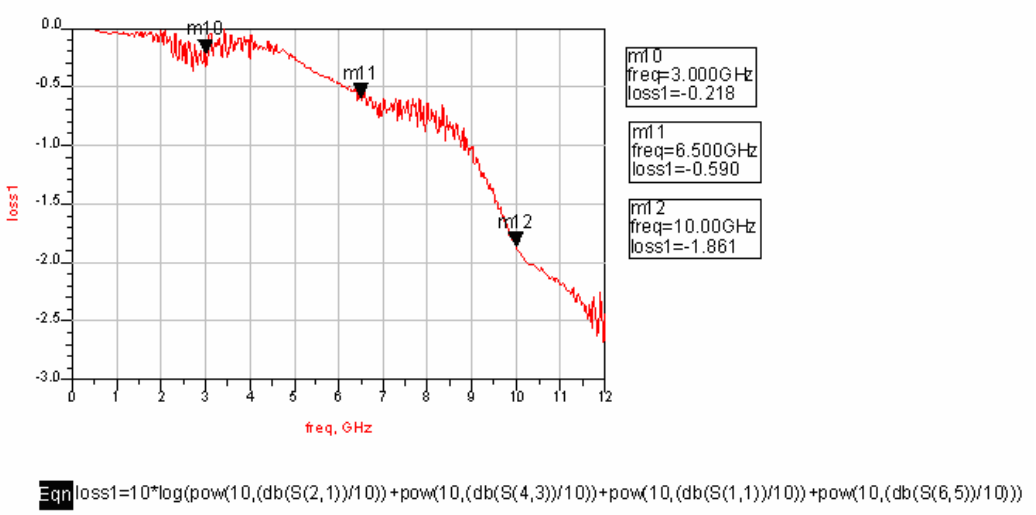


Figure 3-22: Total Loss Calculation of Measured Performance

3.2. Miniaturization of Stubs

Stubs are inevitable components of microwave circuits such as matching networks, biasing networks, filters which use distributed techniques in microwave frequencies. In the design of those microwave circuits, width, which determines the characteristic impedance, length and end effect of the stub, which can be open or short circuited, are the design parameters. Especially for low end of microwave frequencies, large size of stub is the primary problem of the designer to be solved. Therefore, miniaturization of stubs becomes important. For this purpose, miniaturization of quarter wavelength and radial stubs, widely used in biasing networks of microwave active components for narrowband and wideband applications, are analyzed, novel techniques are proposed, and simulation and measurement results are presented in the following sub-parts.

3.2.1. Quarter Wavelength Stub

In the bias networks for narrowband applications, quarter wavelength stubs are used in the form of either short-circuited or open-circuited. In order to decrease the length of stub, two series stubs with different characteristic impedances can be utilized. The schematic of this proposed method is given in

Figure 3-23.

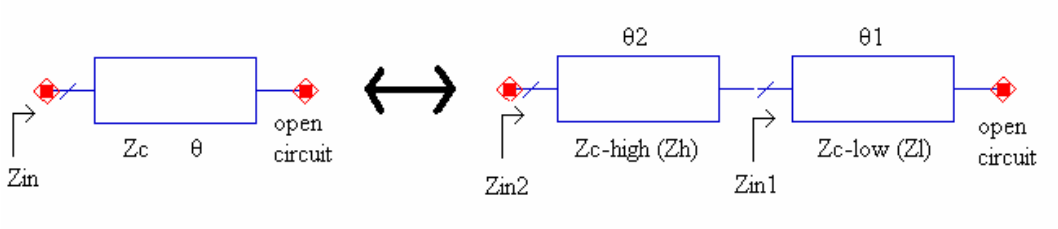


Figure 3-23: Schematic of Proposed Method for Quarter Wavelength Stub

The input impedance of a transmission line terminated with Z_L can be expressed as:

$$Z_{in} = Z_c \frac{Z_L + jZ_c \tan \beta l}{Z_c + jZ_L \tan \beta l} \tag{3.19}$$

where $\beta l = \theta$ is the electrical length.

In case of Z_{in1}, where Z_L is open circuit, it can be expressed by using (3.19) as:

$$Z_{in1} = \frac{Z_l}{j \tan \beta l_1} \tag{3.20}$$

Z_{in2} is terminated with Z_{in1}, so Z_{in2} can be written as:

$$Z_{in2} = Z_h \frac{Z_{in1} + jZ_h \tan \beta l_2}{Z_h + jZ_{in1} \tan \beta l_2} \tag{3.21}$$

Let $t_1 = \tan \beta l_1$ and $t_2 = \tan \beta l_2$, then using (3.20) and (3.21), Z_{in2} can be re-expressed as:

$$Z_{in2} = Z_h \frac{\frac{Z_l}{jt_1} + jz_h t_2}{Z_h + \frac{Z_l}{t_1} t_2} = Z_h \frac{(Z_h t_2 - \frac{Z_l}{t_1})}{(Z_h + Z_l \frac{t_2}{t_1})}$$

In order to get short circuit impedance at the input port, following equation must be satisfied:

$$Z_{in2} = 0 \Rightarrow Z_h t_2 - \frac{Z_l}{t_1} = 0 \Rightarrow t_1 t_2 = \frac{Z_l}{Z_h}$$

Then, substituting t_1 and t_2 into above equation:

$$\tan \beta l_1 \tan \beta l_2 = \frac{Z_l}{Z_h} < 1$$

Assume equal electrical length $\theta_1 = \theta_2$, then $\tan^2 \theta = \frac{Z_l}{Z_h} \Rightarrow \tan \theta = \sqrt{\frac{Z_l}{Z_h}}$

For equal characteristic impedances $Z_l = Z_h$, θ=45° which means a quarter wavelength transmission line. However, for $Z_l < Z_h$, θ is lower than 45°. It is also notable that electrical length θ decreases when the difference between characteristic impedances increases. But, for microstrip technology practical limit of characteristic impedance of transmission lines is between 20-100 Ω.

In order to demonstrate the proposed method, this structure is simulated in ADS. In Figure 3-24, ADS schematic of the proposed method is given. For a quarter wavelength transmission line at center frequency of 1 GHz, the RF short point seen from input port when terminated with open circuit is 1 GHz as expected. However, with this method by using two cascaded transmission lines with 100 Ω and 20 Ω characteristic impedances and 45° electrical length, RF short point is shifted to 535 MHz as seen in Figure 3-25. Similarly, the center frequency 1 GHz can be fixed and by decreasing electrical length of two lines, total length can be decreased as in Figure 3-24-(a). The related simulation result on Smith Chart is presented in Figure 3-26. These results show that approximately 50% reduction in size is achieved for quarter wavelength transmission lines.

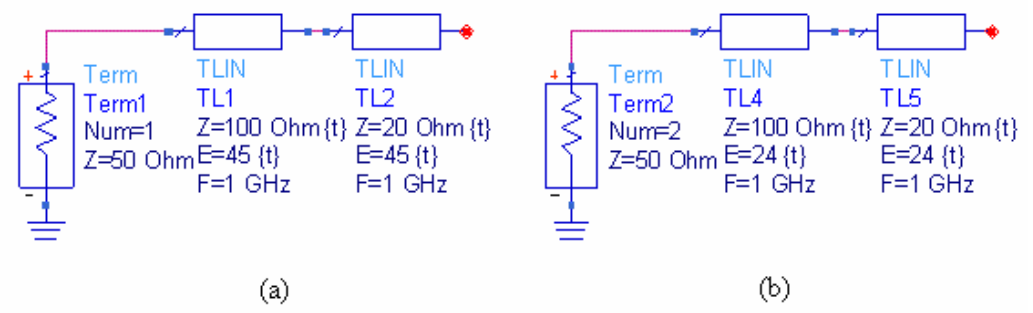


Figure 3-24: ADS Schematics of Proposed Method for Miniaturization of Quarter Wavelength Stubs

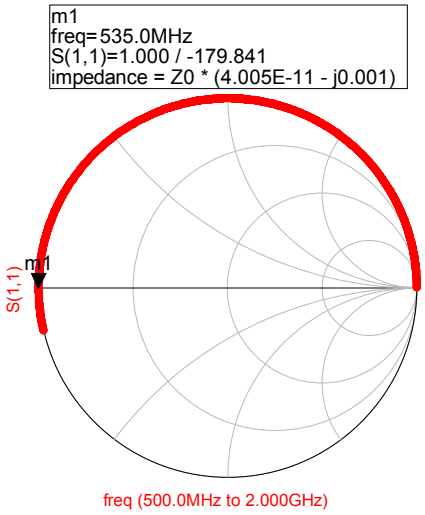


Figure 3-25: Simulation Result of Proposed Method in Figure 3-24-(a) on Smith Chart

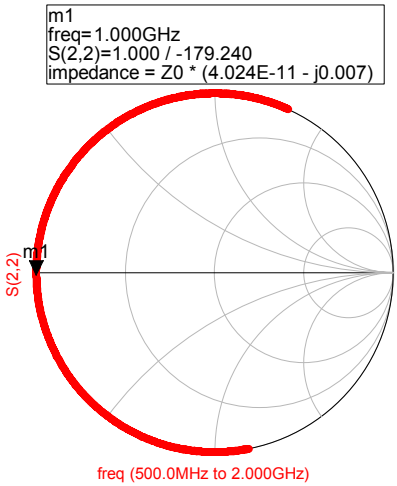


Figure 3-26: Simulation Result of Proposed Method in Figure 3-24-(b) on Smith Chart

3.2.2. Radial Stub

In biasing networks of active devices, microstrip radial stub is an alternative solution of bypass capacitor in a wide frequency band. This wide frequency band property of radial stub is the major advantage when compared with single quarter wavelength transmission line. The geometry of a radial stub is composed of a part of circle as in Figure 3-27. The angle subtended by stub, width of input line W_i and length L are the design parameters of radial stubs. The length is considerably smaller than quarter wavelength transmission line which is taken as $\lambda/8$ at the beginning of design. As expected when the angle of radial stub is decreased the frequency band performance is degraded and the geometry becomes similar to a quarter wavelength transmission line. As will be seen in the simulation results, angle and length of a radial stub are closely related.

In this part of the thesis work, a method is devised to decrease the resonant frequency of the stub which corresponds to the decrease in size at a fixed frequency. The devised method is based on the idea presented above for the rectangular stub; the impedance of the first section of the stub is increased. In order to preserve the structural shape and in order to maintain a long path for the current to have a lower resonant frequency, part of the conductor is removed as explained in the following parts. This geometry can also be named as a defected radial stub.

Part of the radial stub is removed for 40°, 50°, and 60° angles, and this new geometry is simulated in order to compare the miniaturization results. In the design of the regular radial stubs 1 GHz is chosen as the reference frequency as in the previous case.

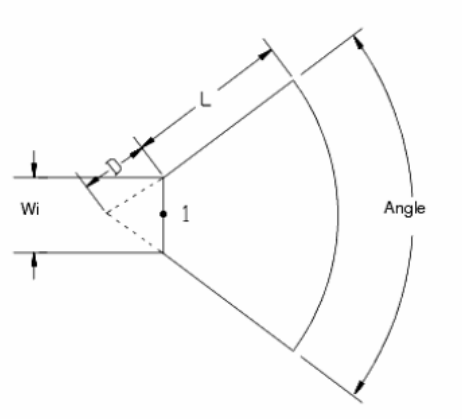


Figure 3-27: Geometry of Radial Stub

Rogers 4003 with 0.8 mm height is used in design. For the starting point, the length of 40°, 50°, 60° angle radial stubs are determined. The ADS schematic is given Figure 3-28 with a 50 Ω line added to the input.

The corresponding lengths, in other words the radii of the radial stubs, are approximately equal to $\lambda/8$ and decrease with the increase of angle which is an expected result. The simulation results of these three radial stubs and a quarter wavelength stub is given in Figure 3-29. The results explicitly show that radial stubs have wider bandwidth than a single quarter wavelength stub. Moreover, wider bandwidth can be achieved by increasing the angle of radial stub.

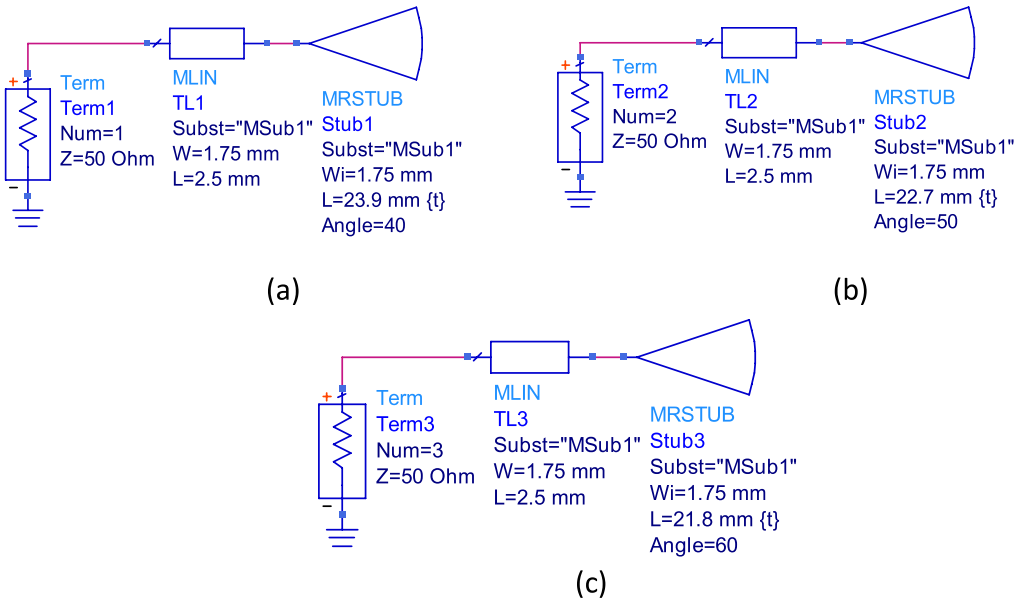


Figure 3-28: ADS Schematic of (a) 40°, (b) 50°, (c) 60° Radial Stubs @ 1 GHz

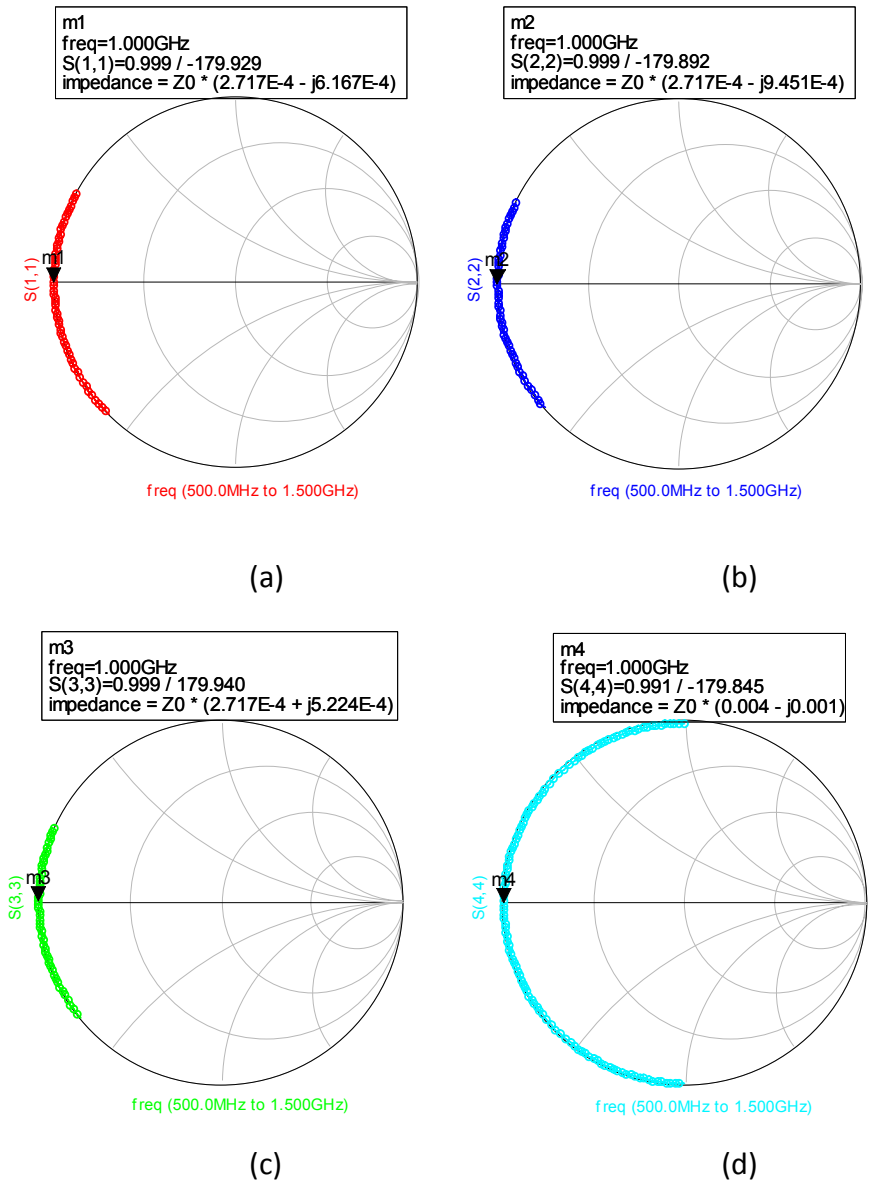
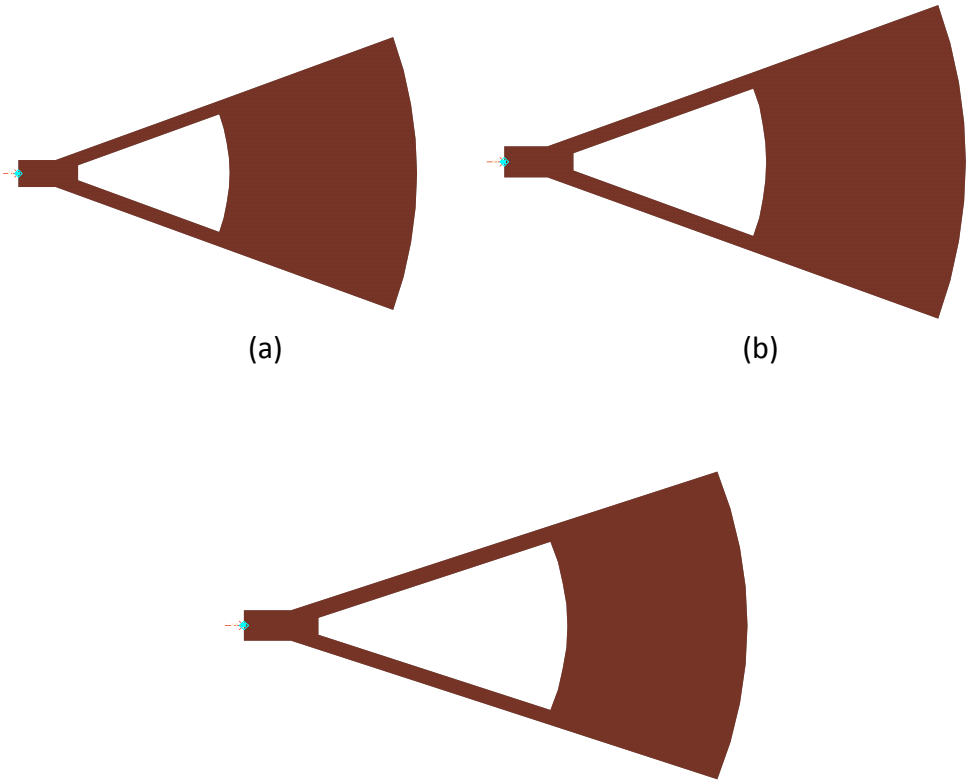


Figure 3-29: Simulation Results of (a) 40°, (b) 50°, (c) 60° Radial Stubs, (d) Quarter Wavelength Stub

In order to shift short circuit resonant frequency to lower values, a part of the radial stub is removed from the internal region. This removed part is also a radial stub with small dimensions as in fractal approach. This approach is applied for all three angles 40°, 50°, 60°, and an optimum length of the removed part is tried to find.

For 40° angle of radial stub case, radial stubs with various lengths of radial defect are simulated in ADS Momentum. Among those lengths of radial defect, 13 mm length is found to be the optimum for 40° of angle. The layout of 10, 11, 13mm length cases are given in Figure 3-30 and corresponding EM simulation results, shown on Smith Chart, are given in Figure 3-31 respectively. According to those results, extracting a radial slot shifts resonance frequency to 900 MHz. Moreover, 13 mm length of radial slot is found to be optimum. However, increasing the length of slot degrades broadband performance.



(a) (b)

(c)

Figure 3-30: Layouts of 40° Radial Stub with Radial Slot Length (a) 10mm, (b) 11mm, (c) 13mm

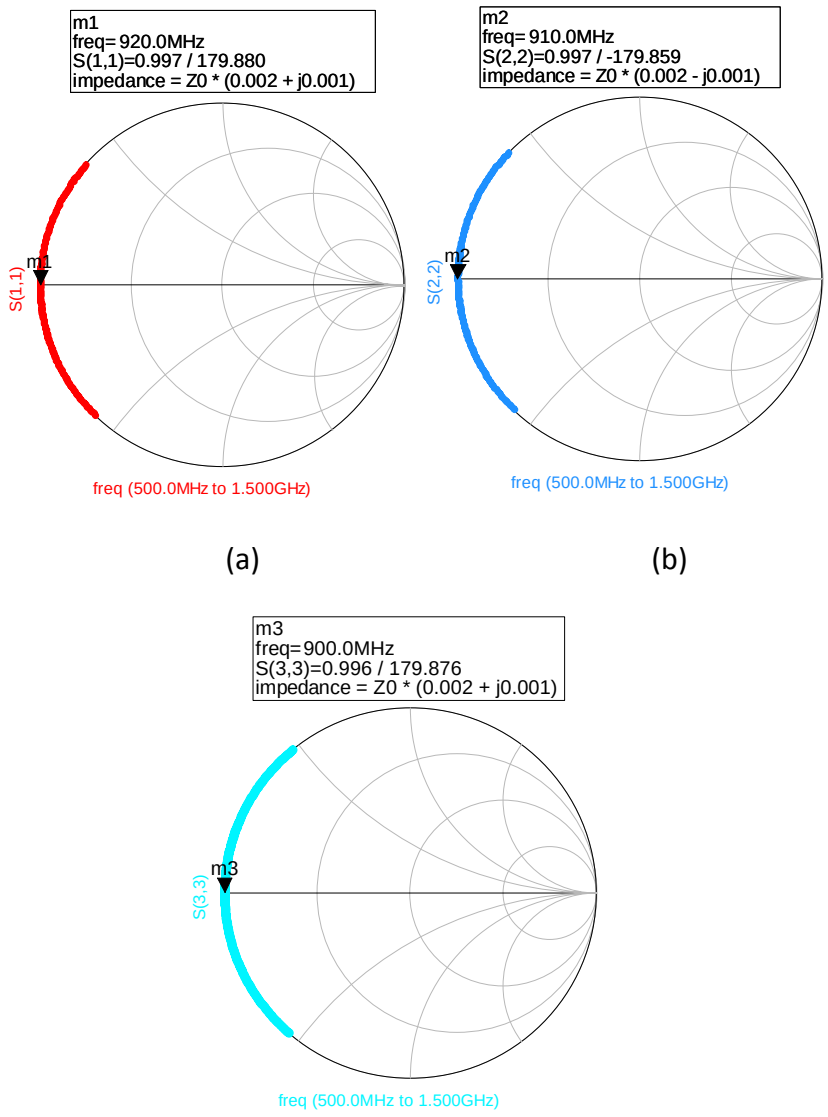


Figure 3-31: EM Simulation Results of 40° Radial Stub with slot length (a) 10mm, (b) 11mm, (c) 13mm

For 50° angle of radial stub case, again as in 40° case, different lengths of radial defect are simulated and an optimum length of 12mm is obtained. Layouts of radial defect lengths of 10mm, 12mm, and 13mm are presented in Figure 3-32 and the corresponding EM simulation results are shown in Figure 3-33. Those results show that 10 mm radial slot length is optimum and it is obvious that 851 MHz of short resonance frequency is the minimum among three cases. As in 40° case, for high radial slot length, frequency bandwidth decreases which is a

drawback of miniaturization of radial stubs.

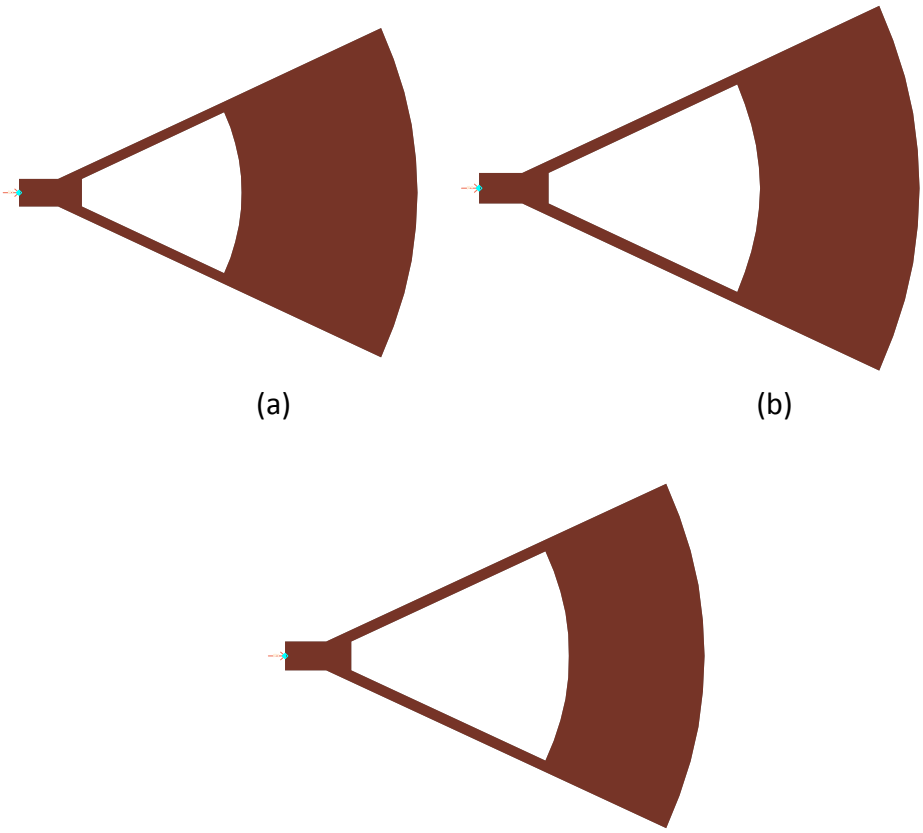


Figure 3-32: Layouts of 50° Radial Stub with Radial Slot Length (a) 10mm, (b) 12mm, (c) 13mm

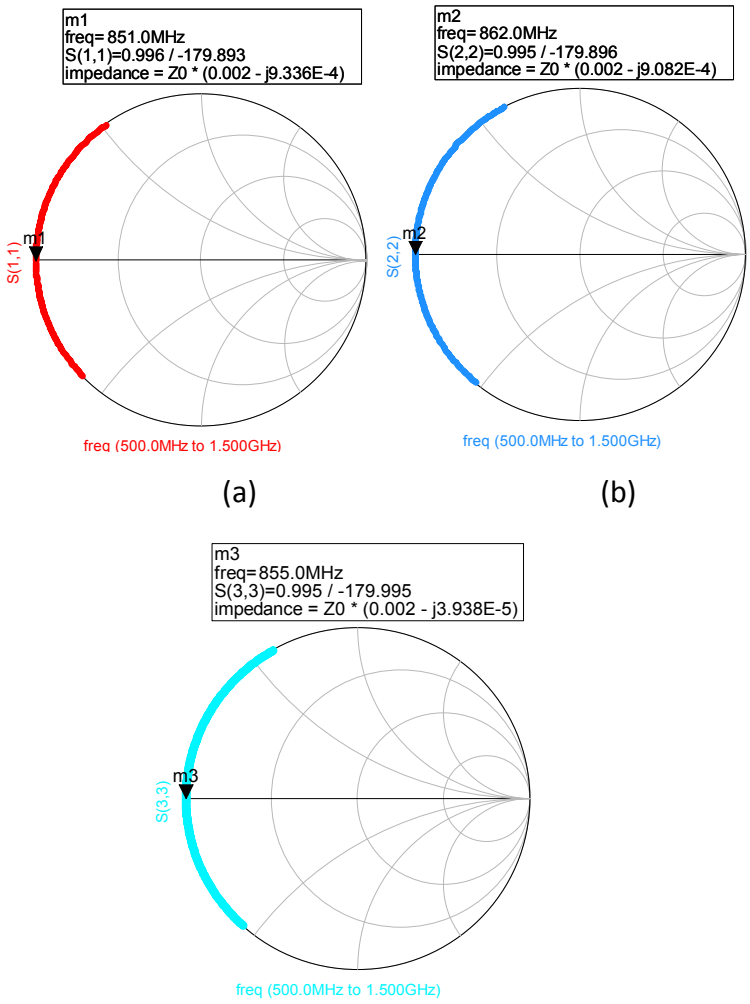


Figure 3-33: EM Simulation Results of 50° Radial Stub with slot length (a) 10mm, (b) 12mm, (c) 13mm

Finally, 60° radial stub is examined and very similar results are obtained. The layouts and simulation results are presented in Figure 3-34 and Figure 3-35 respectively. The optimum resonance frequency of 835 MHz is obtained for radial slot length of 7mm.

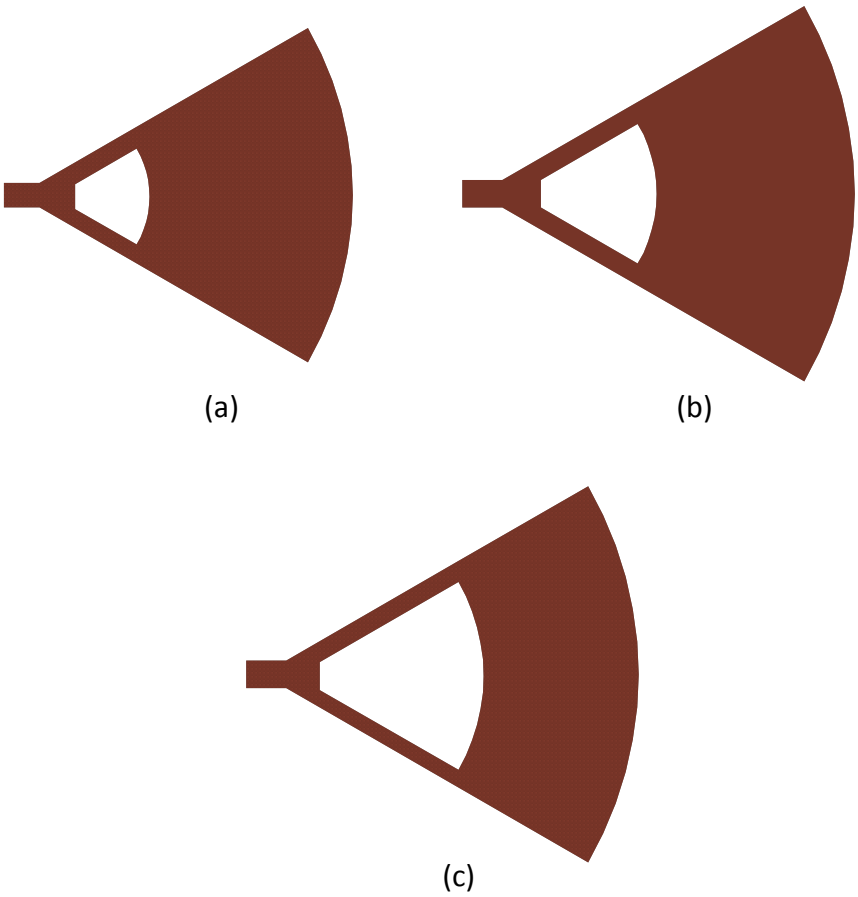


Figure 3-34: Layouts of 60° Radial Stub with Radial Slot Length (a) 5mm, (b) 7mm, (c) 10mm

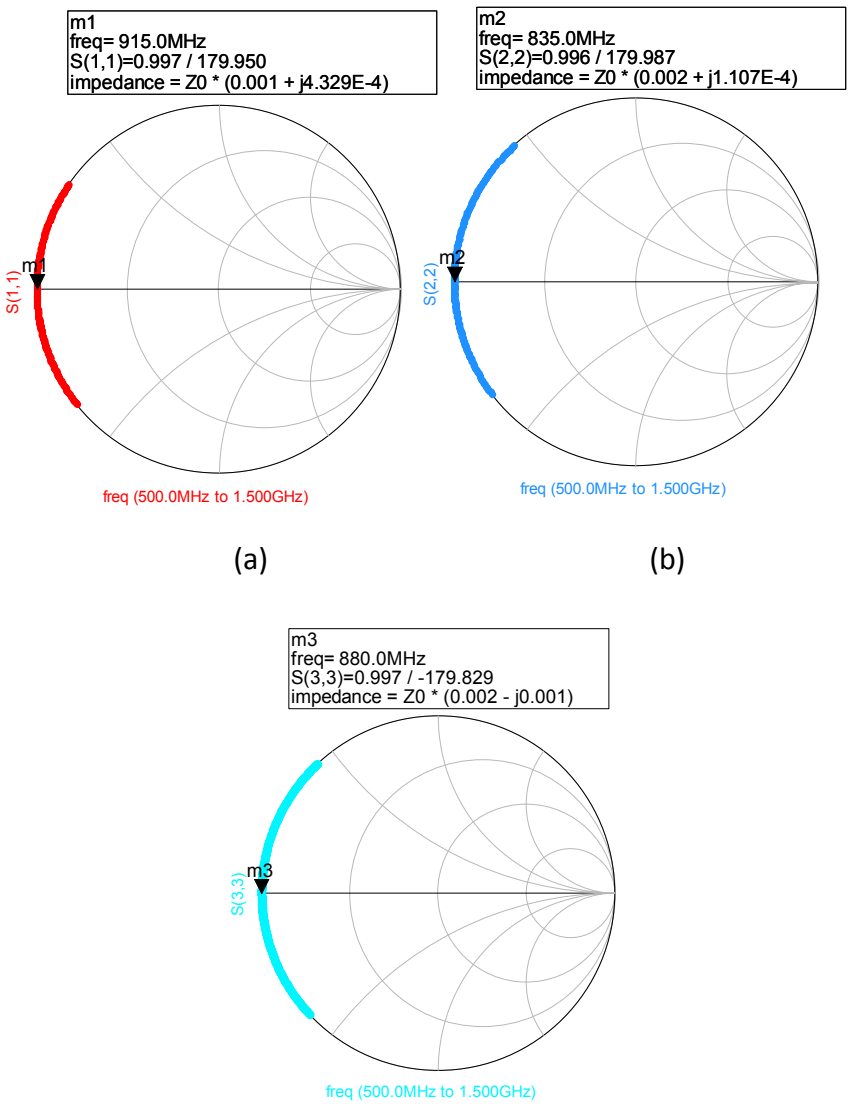


Figure 3-35: EM Simulation Results of 60° Radial Stub with slot length (a) 5mm, (b) 7mm, (c) 10mm

The simulation results of miniaturization work for 40°, 50°, 60° radial stubs showed that optimum slot length depends on radial stub angle. For 40° it is found as 13mm, however it is 7mm for 60° angle. It is also notable that frequency bandwidth performance degrades for those three cases.

At this point a new parameter W_f which is the width between radial stub and radial slot as seen in Figure 3-36 can be defined. The short point is affected by W_f values. In order to prove this, 50° radial stub is used in the trials. The

optimum length of the radial slot is found to be 12mm in the previous simulations. For this case W_f is changed from 125um to 1mm in four steps and results are compared. The layouts of those four cases are given in Figure 3-37. The corresponding EM simulation results are presented in Figure 3-38. It can be clearly seen from those results that for smaller feedline widths lower short point frequency is obtained. Unfortunately, when feedline width is decreased, bandwidth is also decreased. For a 125um width, short point frequency is shifted to 718 MHz while it is 923 MHz for 1mm width.

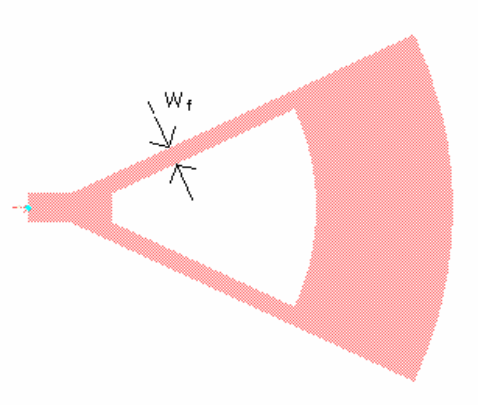


Figure 3-36: Layout of Radial Stub with Radial Slot with W_f Feed-line Width

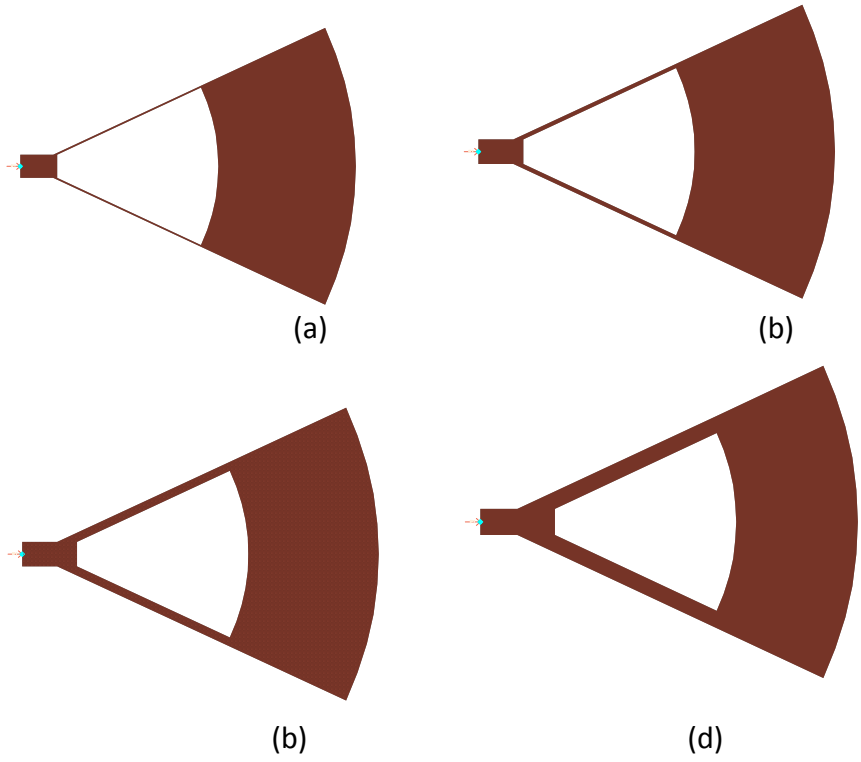


Figure 3-37: Layouts of 50° Miniaturized Radial Stub for Feedline Widths (a) 0.125mm, (b) 0.3mm, (c) 0.6mm, (d) 1mm

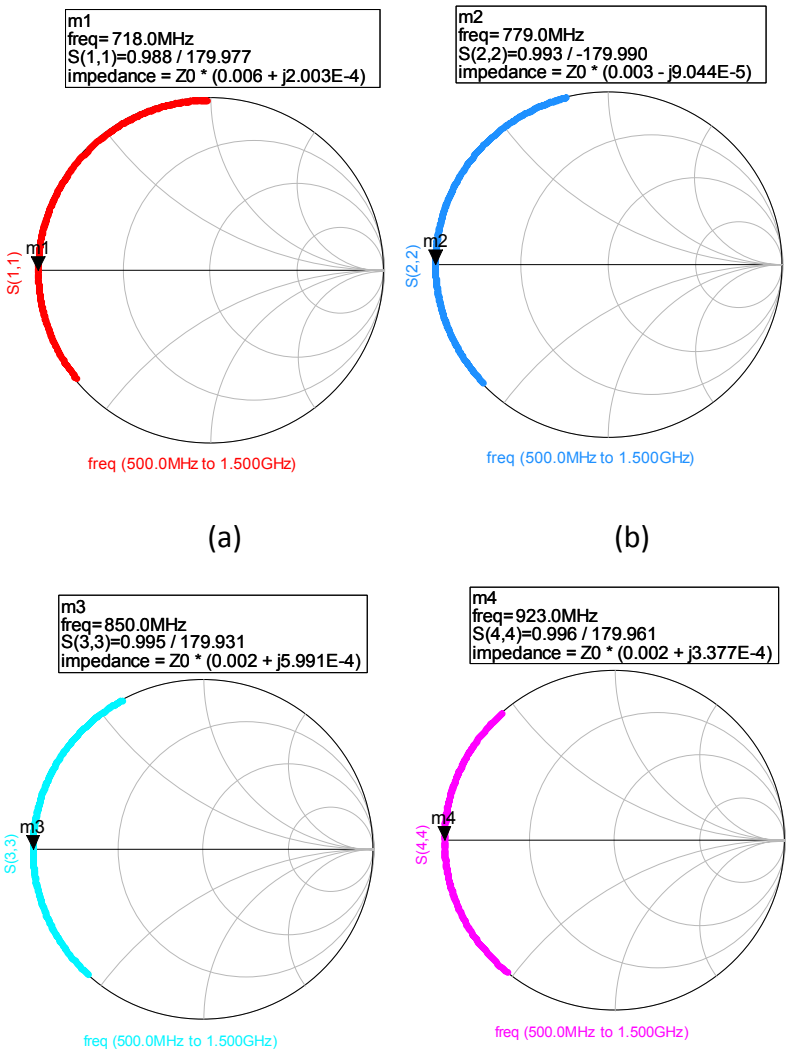
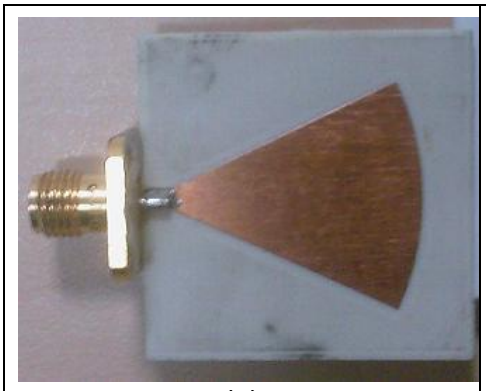


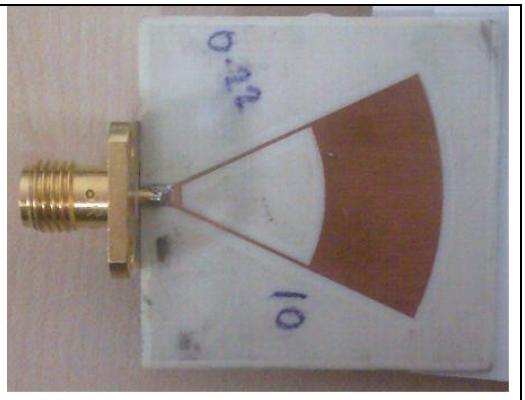
Figure 3-38: EM Simulation Results of 50° Miniaturized Radial Stub for Feedline Widths (a) 0.125mm, (b) 0.3mm, (c) 0.6mm, (d) 1mm

The feedline width of 0.3mm and 1mm are implemented on Rogers 4003 substrate. Network analyzer measurement results are given in Figure 3-40. These results are compatible with EM results. For 0.3mm feedline width, short circuit frequency in EM simulation was 779 MHz, which is 823 MHz in the measurements. Similarly, for 1mm feedline width, short circuit impedance point frequency is shifted from 923 MHz to 937 MHz. The photographs of the realized radial stubs on Rogers 4003 substrate are given Figure 3-39.

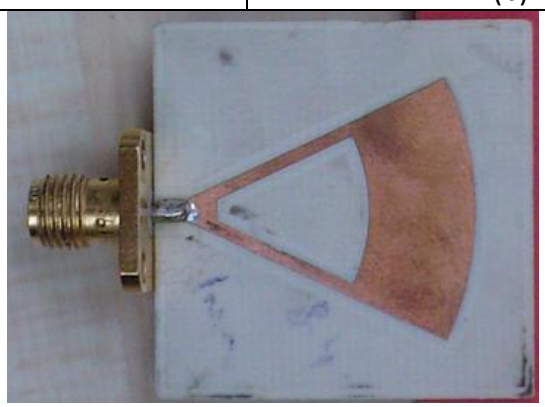
Other than removing a radial slot in a radial stub, different techniques are tried and simulated in order to miniaturize the radial stub. The layouts are given in Figure 3-41. Some of them have similar structures with fractals. However, any considerable improvement is not achieved in these structures.



(a)

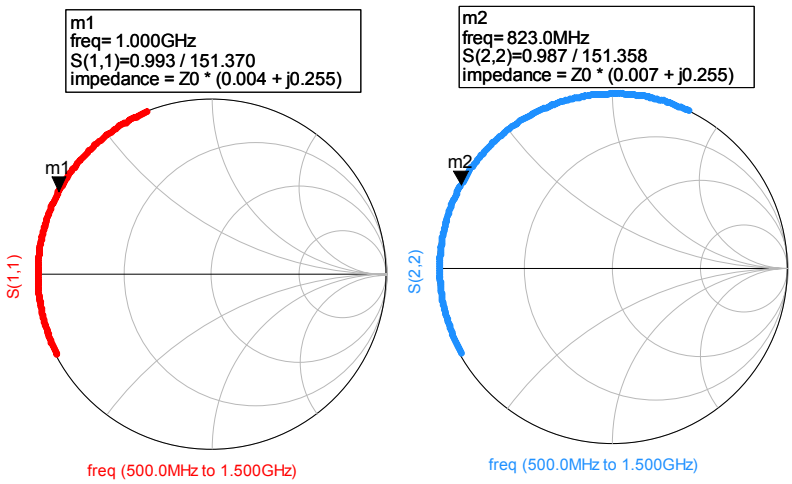


(b)

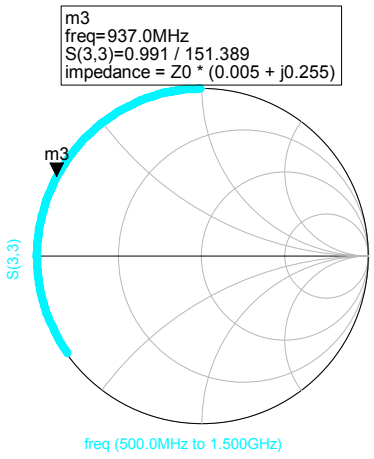


(c)

Figure 3-39: Photograph of 50 °, 22.7 mm Radial Stub , (a) without radial slot, (b) with 10mm radial slot with 0.3mm feedline, (c) with 10mm radial slot with 1mm feedline



(a) (b)



(c)

Figure 3-40: Measurement Results (a) Reference Short Point, (b) 0.3mm, (c) 1mm Feedline Width

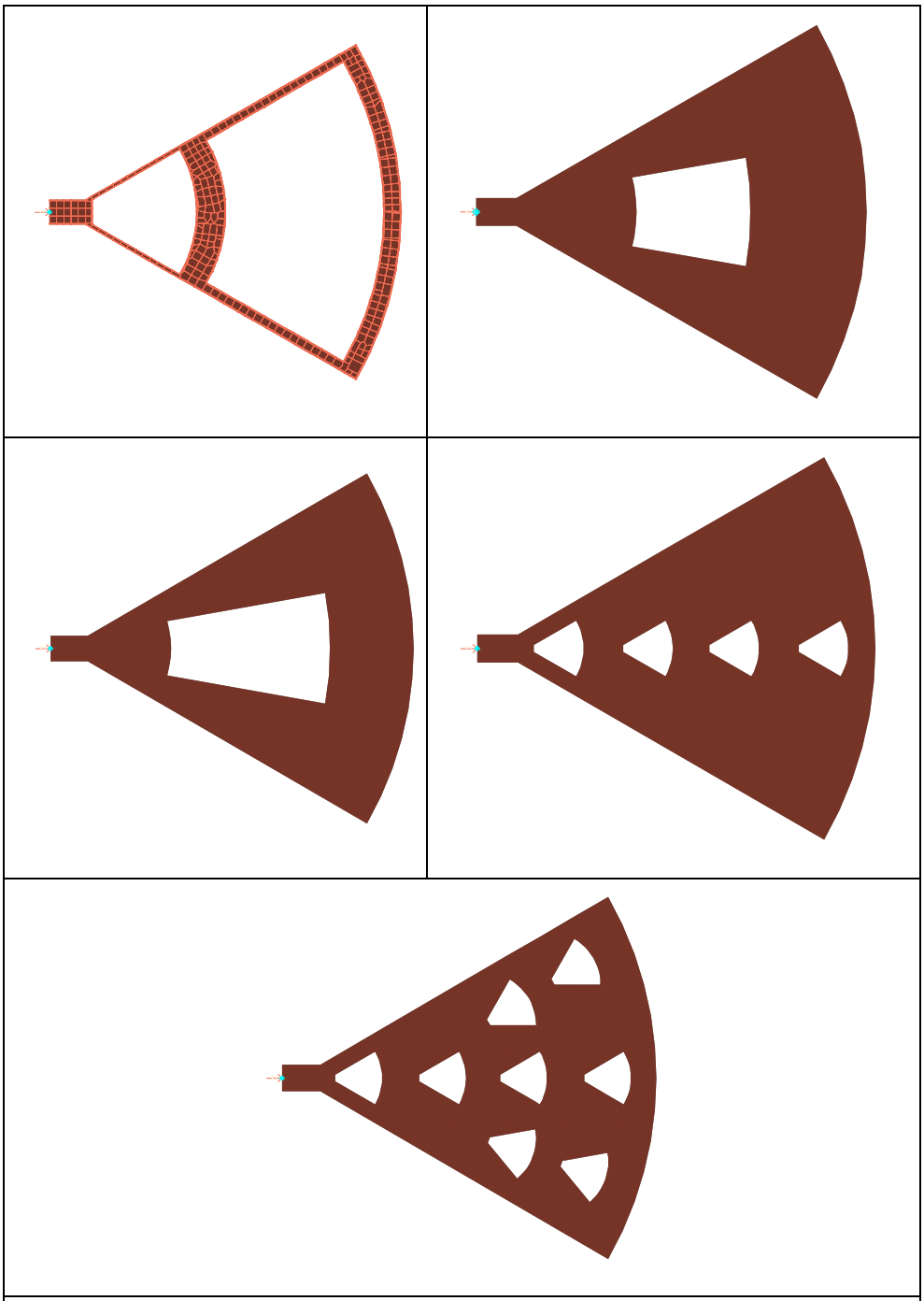


Figure 3-41: Layouts of Tried Techniques for Miniaturization of Radial Stubs

3.3. Interdigital Capacitor

In circuit design technologies, capacitors are widely used such as in matching networks, filter, amplifier, mixer designs etc. Especially for high frequencies, lumped, packaged commercially available capacitors have large parasitic effects. Moreover, for a fixed package capacitor such as 0603 package, all capacitor values have same package. At this point, planar capacitors with distributed circuit techniques are well defined solutions for both size reduction and performance enhancement in terms of parasitic effects.

Interdigital capacitor (IDC) is one of planar capacitor techniques with distributed lines. It is a multi-finger structure as shown in Figure 3-42 which uses the capacitance that occurs across a narrow gap between thin-film conductors. These gaps are essentially very long and folded to use a small amount of area. The gap meanders back and forth in a rectangular area forming two sets of fingers that are interdigital. By using a long gap in a small area, compact single layer low value capacitors 0.05 pF-0.5 pF can be realized. This capacitance can be increased by increasing the number of fingers or by using a thin layer of high dielectric constant materials [18]. Dimension parameters of a typical microstrip layout in Figure 3-42 is tabulated in Table 3-1. In this thesis, for simplicity gap between fingers G and gap at the end of fingers Ge are taken as equal. In the simulations, Alumina (εr=9.6, loss tangent=0.001, conductor thickness=1 μ m) with thickness 0.25mm is used as substrate. The fabrication of design can be realized with the help of RF MEMS technology.

In literature, several analysis and characterization of IDC have been reported [18-20]. In the scope this thesis, these analytical analyses are not revisited. Instead, a lumped element equivalent circuit of IDC is introduced and S-parameters of simulation is tried to match to the S-parameters of equivalent circuit. Furthermore, this approach is used in chapter four in matching of power transistor and noise match of low noise amplifier (LNA).

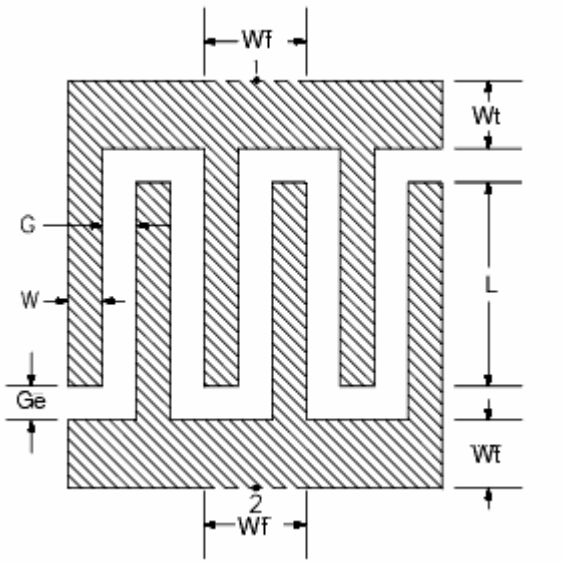


Figure 3-42: Layout of a Typical Microstrip Interdigital Capacitor

Table 3-1: Dimension Parameters of IDC

Name	Description
W	Finger width
G	Gap between fingers
Ge	Gap at end of fingers
L	Length of overlapped region
Np	Number of finger pairs
Wt	Width of interconnect
Wf	Width of feedline

Several similar lumped equivalent circuits for IDC are proposed in literature. The elements in these circuitries represent sub-parts of IDC such as transition, gap or coupled lines shown in Figure 3-43. The resultant equivalent circuit used in simulations is given in Figure 3-44. In this equivalent circuit, Cs, Ls, Rs, Cp represent the effective capacitance of coupled fingers, the inductance of structure, total resistive loss of structure, and capacitance of microstrip lines with respect to ground bottom layer respectively.

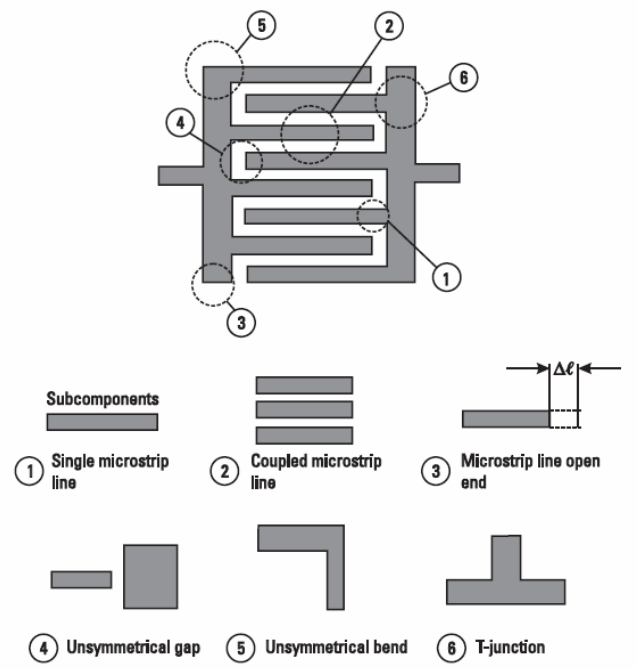


Figure 3-43: Interdigital Capacitor and its Subcomponents

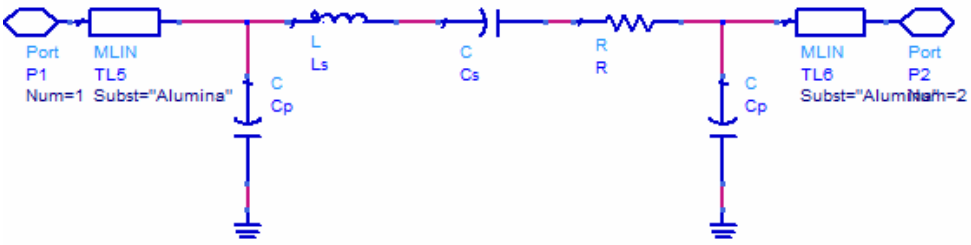


Figure 3-44: Lumped Element Equivalent Circuit of Interdigital Capacitor

The minimum width that can be implemented is 5um by RF MEMS technology in HMIC circuit implementation. So, gap of the fingers are fixed to 5um and as a starting point of simulations L=500um, W=20um, Wt=30um and N=8 is set. As a feed line a microstrip line with width and length 50um is used. Frequency bandwidth is chosen as 5-7 GHz. In order to get the actual series capacitance ADS momentum EM simulation is done. This simulation result is tried to match with equivalent circuit by using optimization tool. In order to observe the effect of L, W, Wt, N on element values, they are changed individually and for each case a new EM simulation is done. For this purpose, L, W, Wt and N are increased to 1mm, 50um, 50um, 16 respectively in each trial individually. The

corresponding EM and equivalent circuit simulation results including return loss, transmission loss and phases are shown on Figure 3-45, Figure 3-46, Figure 3-47, Figure 3-48 and Figure 3-49 respectively. These results point out that EM simulation results cohere with equivalent lumped element circuit in defined frequency band. The element values of equivalent circuit for each trial are given in Table 3-2. These results show that capacitance of IDC can be increased by increasing length or number of fingers. When the length is increased series inductance is also increased, but for the case of increased number of fingers, series inductance decreases since number of parallel fingers are increased. On the other hand, it is also notable that when the dimension of the structure is increased, parallel capacitance is also increased. The total loss resistance Rs is limited to 0.3 Ω which is a considerably small value. For L=500um and N=8, series capacitance value is 0.66pF. When L is doubled, capacitance becomes 1.42 pF and for doubled number of fingers it becomes 1.46 pF. For these changes corresponding dimensions changes from 0.6x0.5mm to 1.1x0.5mm and 0.6x1.1mm respectively. These dimensions are still smaller than a 0603 packaged capacitor.

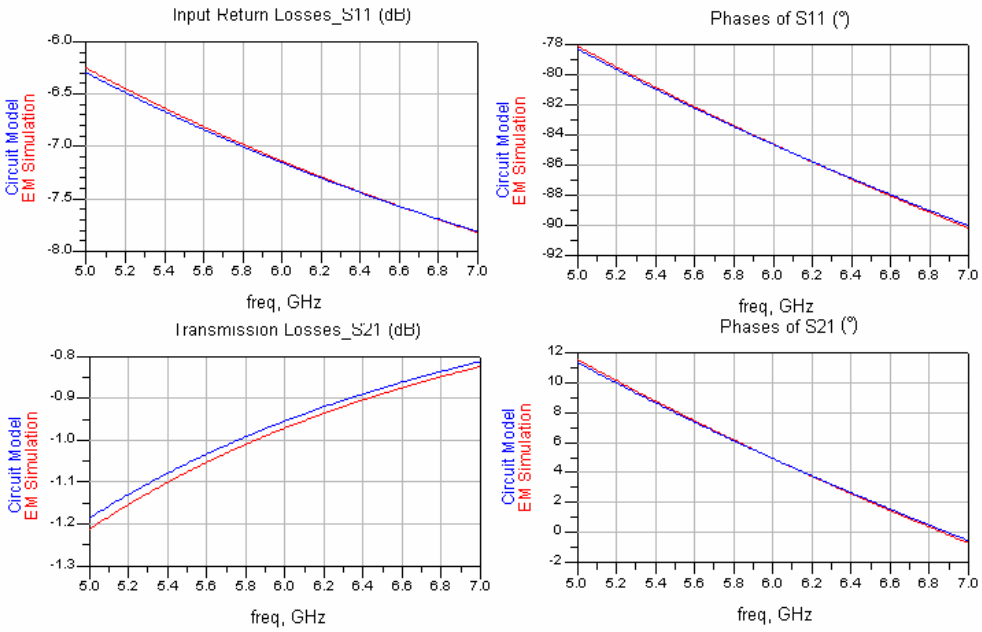


Figure 3-45: EM Simulation and Circuit Model Results of L=500um, W=20um, Wt=30um and N=8

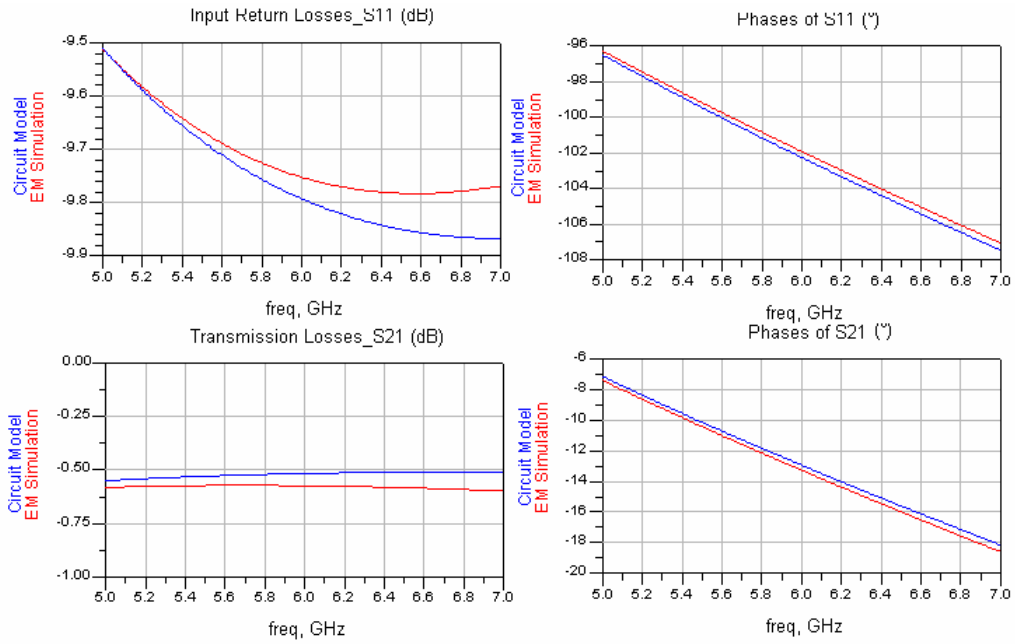


Figure 3-46: EM Simulation and Circuit Model Results of L=1000um, W=20um, Wt=30um and N=8

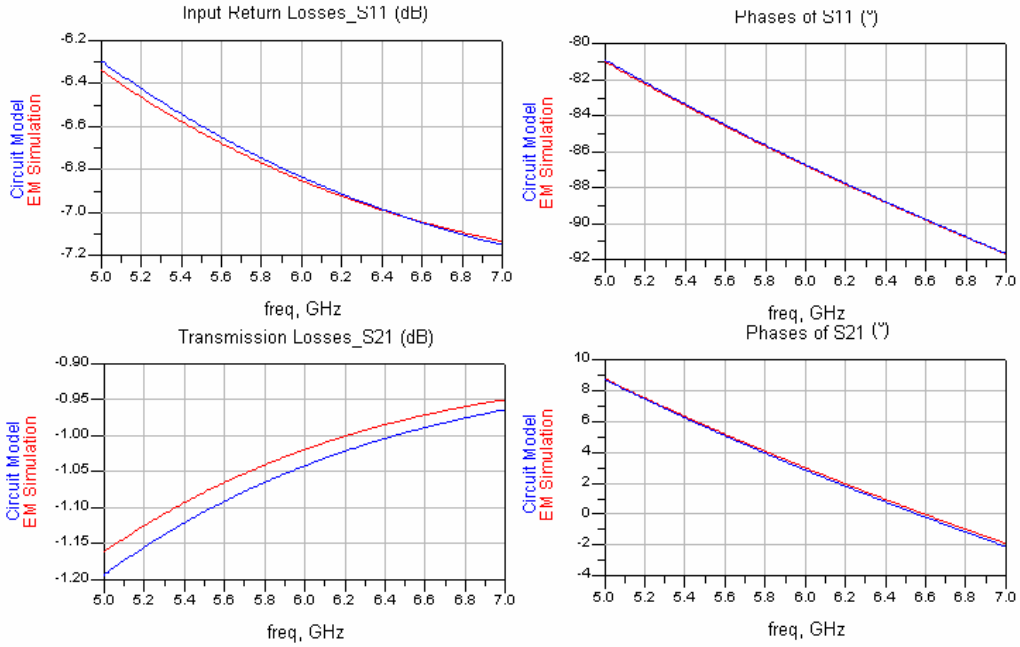


Figure 3-47: EM Simulation and Circuit Model Results of L=500um, W=50um, Wt=30um and N=8

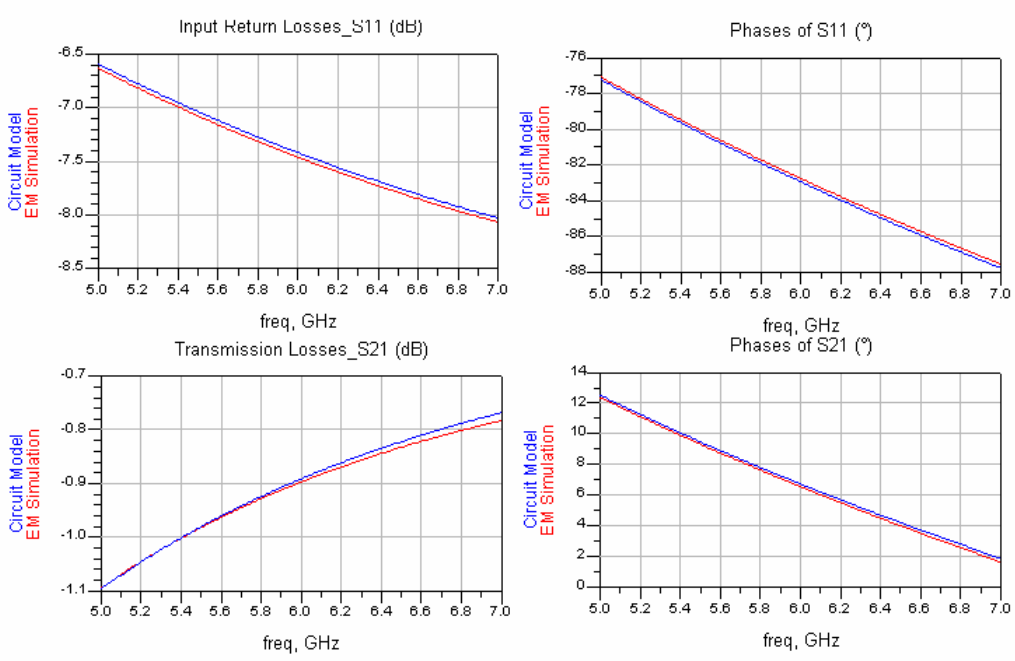


Figure 3-48: EM Simulation and Circuit Model Results of L=500um, W=20um, Wt=50um and N=8

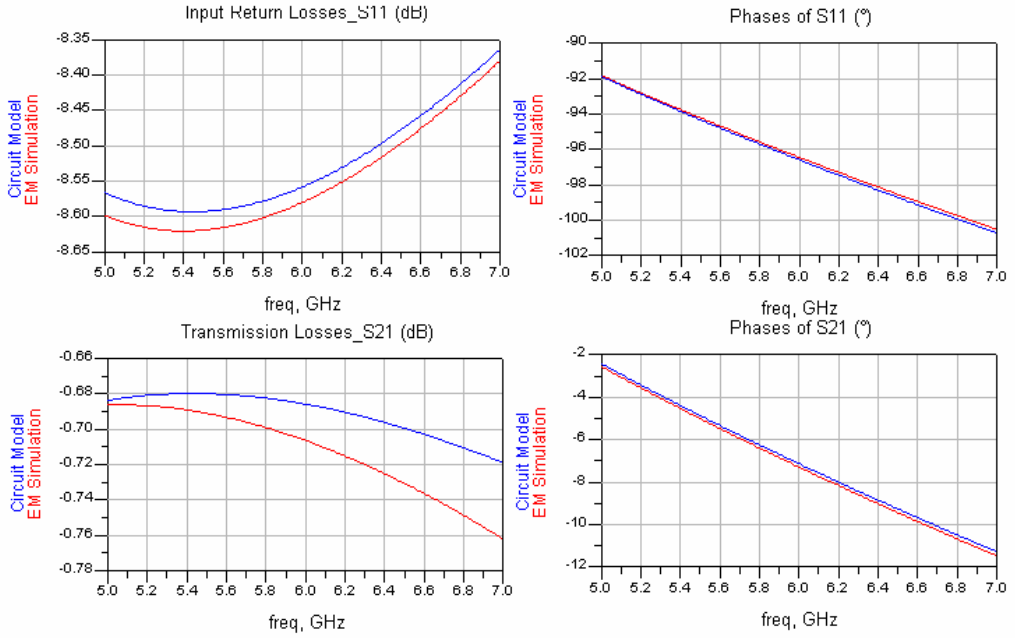


Figure 3-49: EM Simulation and Circuit Model Results of L=500um, W=20um, Wt=30um and N=16

Table 3-2: Equivalent Circuit Element Values of IDC

Condition	Ls (nH)	Cs (pF)	Rs (Ω)	Cp (pF)
L=500um, W=20um, Wt=30um, N=8	0.206696	0.660501	0.175809	0.0952124
L=1000um, W=20um, Wt=30um, N=8	0.278505	1.42412	0.29998	0.145677
L=500um, W=50um, Wt=30um, N=8	0.0884592	0.761475	0.277385	0.108693
L=500um, W=20um, Wt=50um, N=8	0.122519	0.705629	0.182546	0.081381
L=500um, W=20um, Wt=30um, N=16	0.047449	1.45986	0.283887	0.132095

3.4. Spiral Inductor

Usage of planar spiral inductor is emerged from same reasons with interdigital capacitors. They are two dimensional structures that are implemented with RF MEMS technology on printed circuit boards. The only height of inductor only

comes from the transition from inner part to outer. This transition is done with techniques such as wire bond, air bridge, etc. Meander, rectangular, circular and octagonal are two dimensional spiral inductor types as shown in Figure 3-50 [4]. In this study, rectangular shaped spiral inductor is chosen because of its ease of layout.

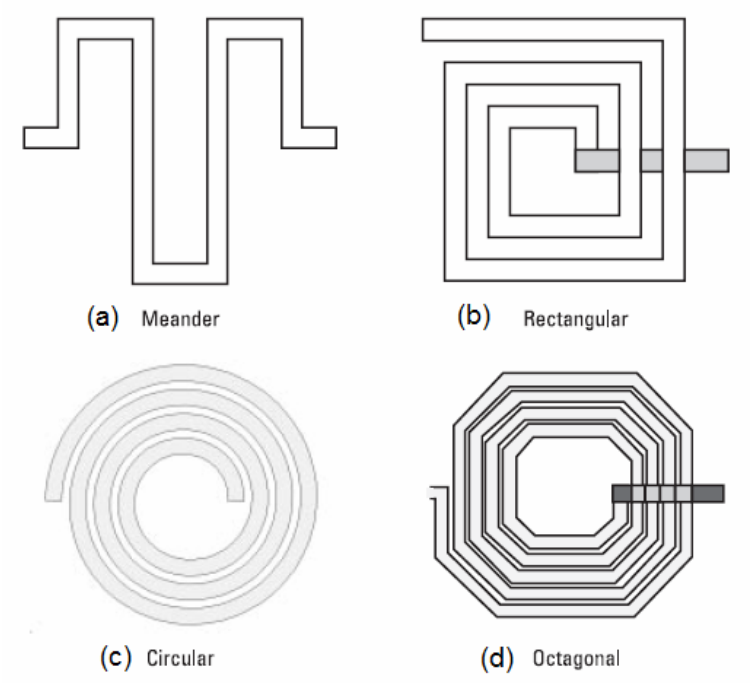


Figure 3-50: Two dimensional Inductor Types, (a) Meander, (b) Rectangular, (c) Circular, (d) Octagonal

Layout of 1 ¾ turn rectangular spiral inductor is given in Figure 3-51. In the structure dimensions Lf, Lx, Ly, W and G represent feedline length, x-dimension length, y-dimension length, conductor width and conductor spacing respectively.

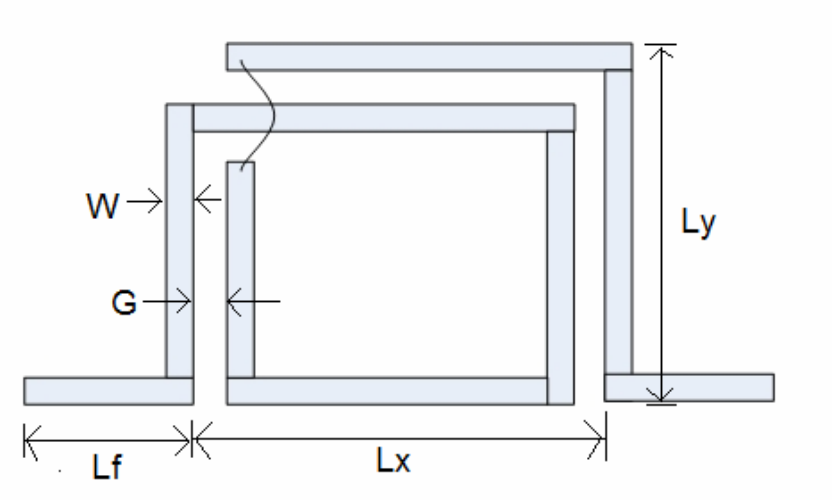


Figure 3-51: Layout of 1 ¾ Turn Rectangular Inductor

For this spiral inductor structure, an equivalent circuit given in Figure 3-52 is used. In this model, L is effective inductance of structure, Cp represents the capacitance of microstrip lines with respect to ground plane and R shows the total resistive loss of structure.

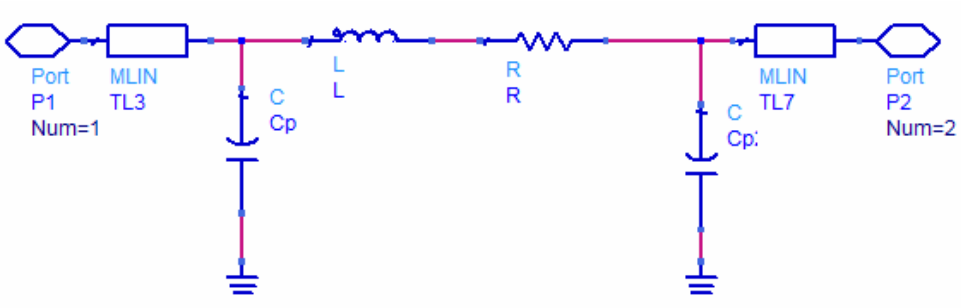


Figure 3-52: Equivalent Circuit for Rectangular Spiral Inductor

In most hybrid RF and microwave circuits bond wires are widely used to interconnect lumped elements, planar transmission lines, solid-state devices and integrated circuits, etc. In this theses both for inner outer part connection of spiral inductors and interconnect of components in next chapter, wire bond is used. In literature, simple inductance calculation formulations of wire bond are driven. One of these formulations for a semi-circle wire bond is given in (3.22) [4].

$$L = 2 \cdot 10^{-4} \cdot l\left(\ln\left(\frac{4l}{d} \right) + 0.5 \cdot \frac{d}{l} - 1 + C \right) \quad (3.22)$$

Where, l and d are diameter and length of wire-bond respectively. C can be expressed in terms of δ (skin-depth) and l as:

$$C = \frac{\delta}{d} \quad (3.23)$$

2.5µm wire-bond diameter and 60 µm length is chosen. For these dimensions the inductance is found as L=0.05nH by using (3.22) and (3.23). So, this result will be added to simulation results in order to take account the wire-bond effect.

In spiral inductor simulation, conductor width and conductor spacing is chosen as 50 µm and 25 µm respectively. ADS Momentum EM simulator is used to simulate the structure on substrate Alumina (εr=9.6, h=0.25mm). In these EM simulations, effect of x and y dimension lengths of spiral inductor is tried to visualize. To do so, three different combinations of Lx and Ly are simulated. These lengths are 250x300 µm, 400x320 µm and 400x400 µm. Afterwards, as in the case of interdigital capacitor, equivalent circuit parameters are determined by using optimization tool. The resultant simulation results of three cases are given in Figure 3-53, Figure 3-54, Figure 3-55 respectively, and equivalent circuit parameters are tabulated in Table 3-3. In these figures, both amplitude and phases of return and transmission loss of EM simulation and circuit model are given. These results show that the series inductance is increased with increasing dimensions.

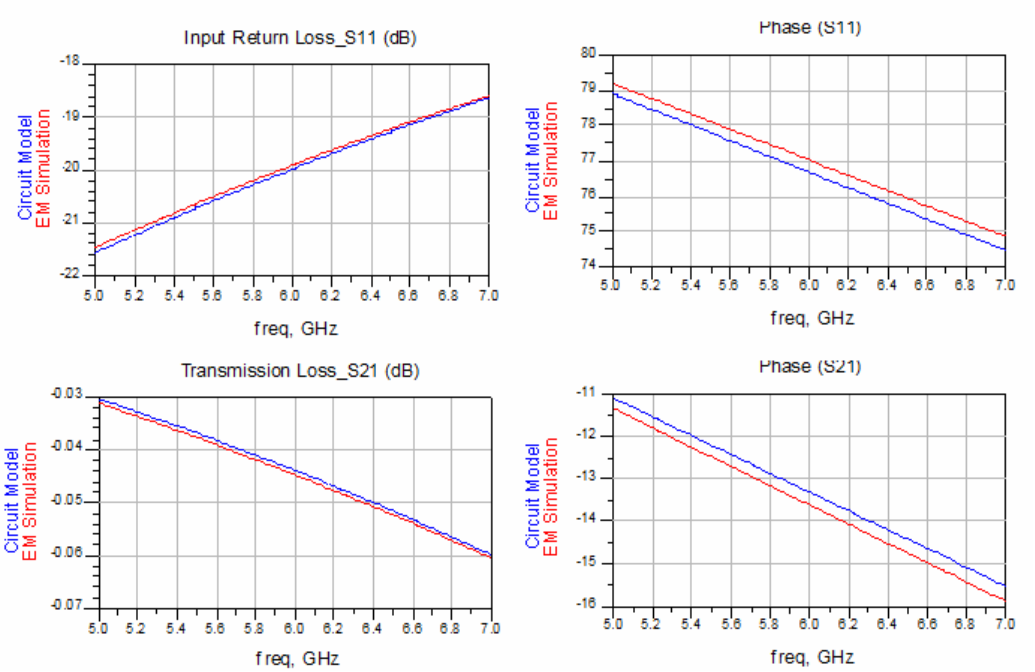


Figure 3-53: EM and Circuit Model Simulation Results of Spiral Inductor with Dimensions 250x300 µm

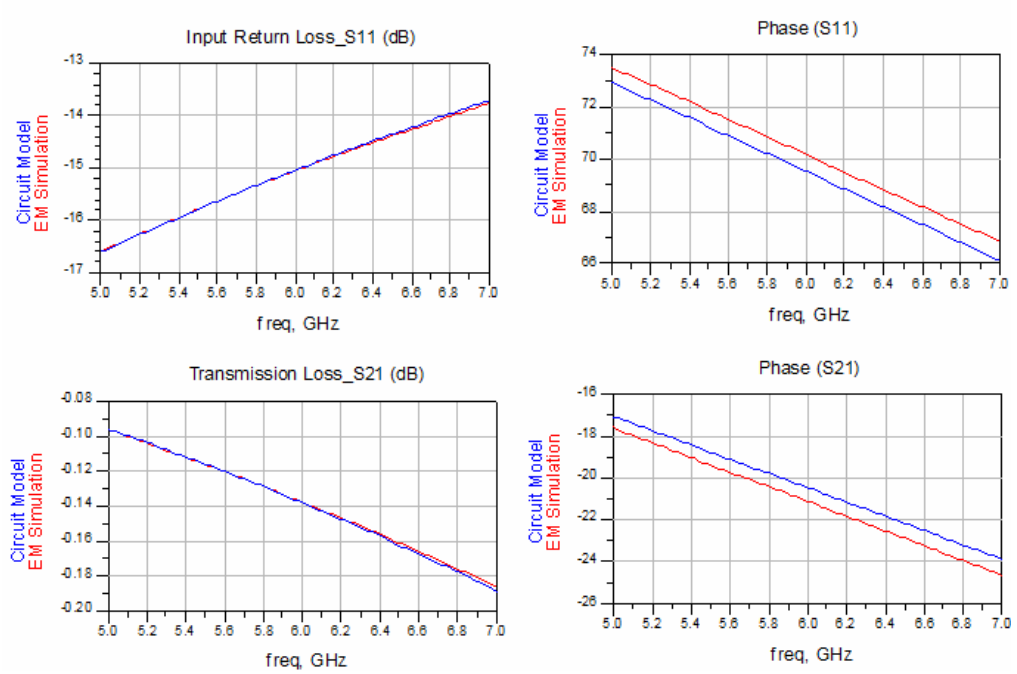


Figure 3-54: EM and Circuit Model Simulation Results of Spiral Inductor with Dimensions 400x320 µm

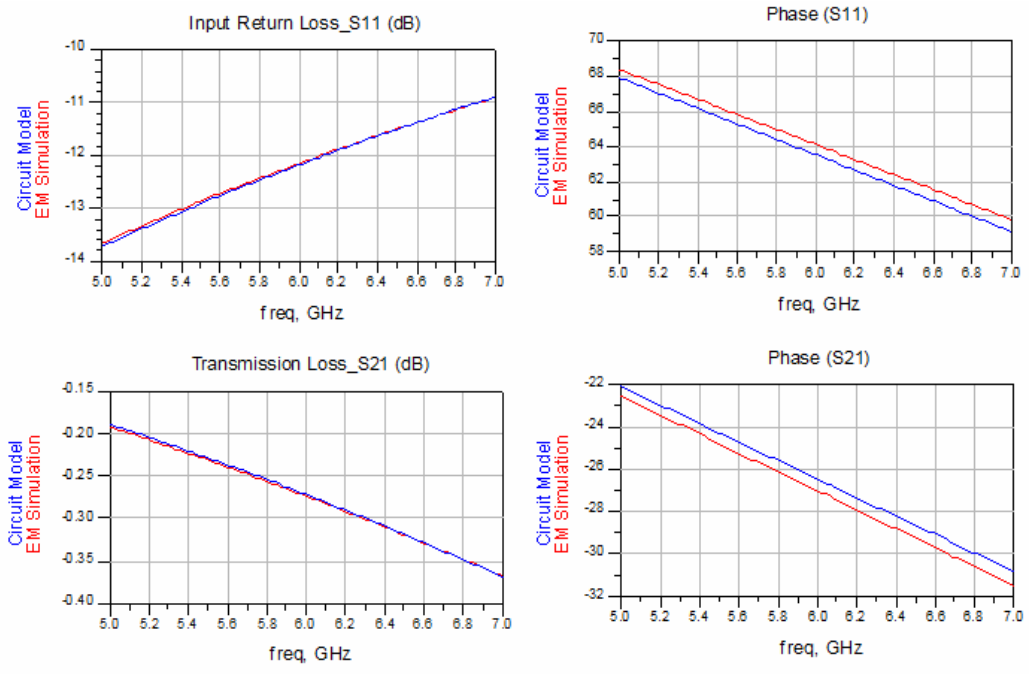


Figure 3-55: EM and Circuit Model Simulation Results of Spiral Inductor with Dimensions 400x400 µm

Table 3-3: Equivalent Circuit Parameters of Simulated Spiral Inductors

Condition	Ls (nH)	Rs (Ω)	Cp (pF)
Lx=250 µm Ly=300 µm	0.440569	0.00051	0.035055
Lx=400 µm Ly=320 µm	0.709831	0.00000119	0.0477169
Lx=400 µm Ly=400 µm	0.946799	0.00008169	0.0568157

3.5. Fractal Techniques

Fractals are another way of miniaturization in RF and microwave engineering. The size compression and multi-band capabilities of fractals allow efficient, broadband and multipurpose devices to be packed in places that were at length inaccessible due to size, weight or appearance constraints. A fractal is a rough

or fragmented geometric shape that can be split into parts, each of which is (at least approximately) a reduced-size copy of the whole. This property is called self-similarity. Roots of mathematical interest in fractals can be traced back to the late 19th Century; however, the term "fractal" was coined by Benoît Mandelbrot in 1975 and was derived from the Latin fractus meaning "broken" or "fractured." A mathematical fractal is based on an equation that undergoes iteration, a form of feedback based on recursion. A fractal is characterized by two factors; the iteration factor and the iteration order. The iteration factor represents the construction law of fractal geometry generation, and the iteration order depicts how many iteration processes are carried out.

In fractal geometry, the fractal dimension, *D*, is a statistical quantity that gives an indication of how completely a fractal appears to fill space, as one zooms down to finer and finer scales. There are many specific definitions of fractal dimension and none of them should be treated as the universal one. From the theoretical point of view the most important are the Hausdorff dimension, the packing dimension and, more generally, the Rényi dimensions [24].

There are two main approaches to generate a fractal structure. One is growing from a unit object and the other is to construct the subsequent divisions of an original structure. Koch curve is an example formation with former technique. It begins with a line of length 1, called initiator (order 0). Then, the middle third of the line is removed and replaced with two lines that each has the same length, called generator (order 1) as shown in Figure 3-56. Sierpinski triangle is an example for the lather formation technique. It stars with a equilateral triangle, then the mid-points of three sides is connected and removed. This inner removed part is also an equilateral triangle. The procedure continues by repeating these steps on smaller triangles. These steps are given in Figure 3-57.

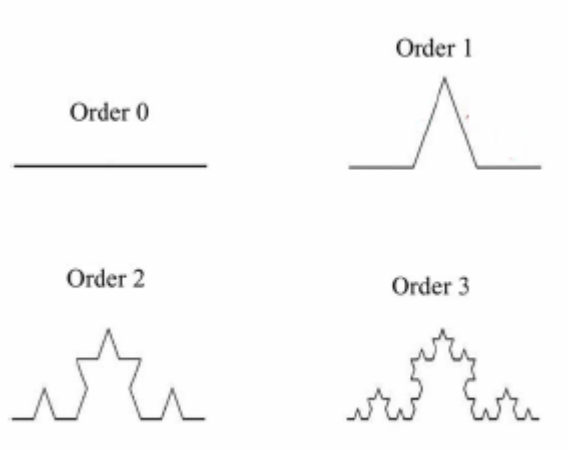


Figure 3-56: Koch Curve Formation

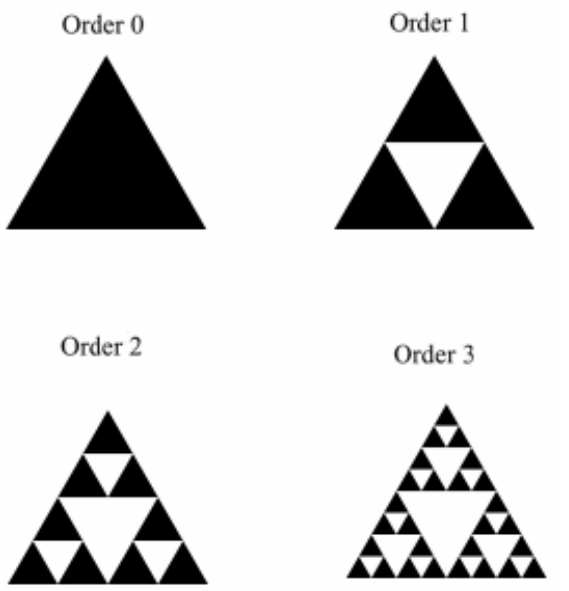


Figure 3-57: Sierpinski Triangle Formation

The dimension of the fractal structure can be calculated with various formulations. The Euclidean dimension D can be defined as:

$$D = \frac{\log N(l)}{\log l} \tag{3.24}$$

where l denotes size reduction in each spatial direction and N denotes the number of self similar objects to cover the original object.

By applying (3.24) to fractal structure, the dimension of the fractal structure in second approach such as Sierpinski triangle can be defined as [24]:

$$D = \lim_{\varepsilon \to 0} \frac{\log N(\varepsilon)}{\log \frac{1}{\varepsilon}} \tag{3.25}$$

where *N(ε)* is the number of self-similar structures of linear size ε needed to cover the whole structure. Using (3.25), dimension of Sierpinski triangle can be calculated as:

$$D = \lim_{\varepsilon \to 0} \frac{\log N(\varepsilon)}{\log \frac{1}{\varepsilon}} = \lim_{k \to \infty} \frac{\log 3^k}{\log 2^k} = \frac{\log 3}{\log 2} \approx 1.585$$

Fractal structures are preferred in RF and microwave designs in order to reduce size of circuits and to get broader bandwidth. It is also possible to design dual-band circuits with the help of fractals. Since infinite length objects fit any small surface and fractional dimension structures fill the space in a more efficient way in fractal structures, long wavelengths can be fitted in small spaces. In literature fractal geometry is used in various circuit deigns. Koch fractal shape is applied to a microstrip band-pass filter to solve 2nd harmonic problem [22]. It is also widely used in antenna design in order to shrink the size, get broader bandwidth and dual-band performance [23]. Even in planar passive circuit elements such as capacitors and resistors, fractal structures are preferred [21]. In distributed matching networks, in order to broad the bandwidth and reduce the size of matching sections Sierpinski approach is adapted [25].

In microwave engineering, matching sections between stages are required to transfer all available power. When the impedance ratio between stages is high, single quarter-wavelength transformer is not sufficient and its frequency band performance is worse. Therefore, multi-stage maximally flat or Chebyshev microstrip matching techniques are applied to solve these problems. At that point to miniaturize matching sections or get wider bandwidth of operation, sierpinski fractal approach can be used [25]. For this purpose two and three

stage maximally flat technique is used to match 7Ω to 50Ω on substrate Alumina (h=0.25mm, εr=9.6) at center frequency 6 GHz. The layouts of these two and three stage matching are given in Figure 3-58. The corresponding section impedances are tabulated in Table 3-4. Sierpinski square approach with iteration factor 1/5 is applied on both matching sections for the iteration order 1. The corresponding layouts are presented in Figure 3-59.

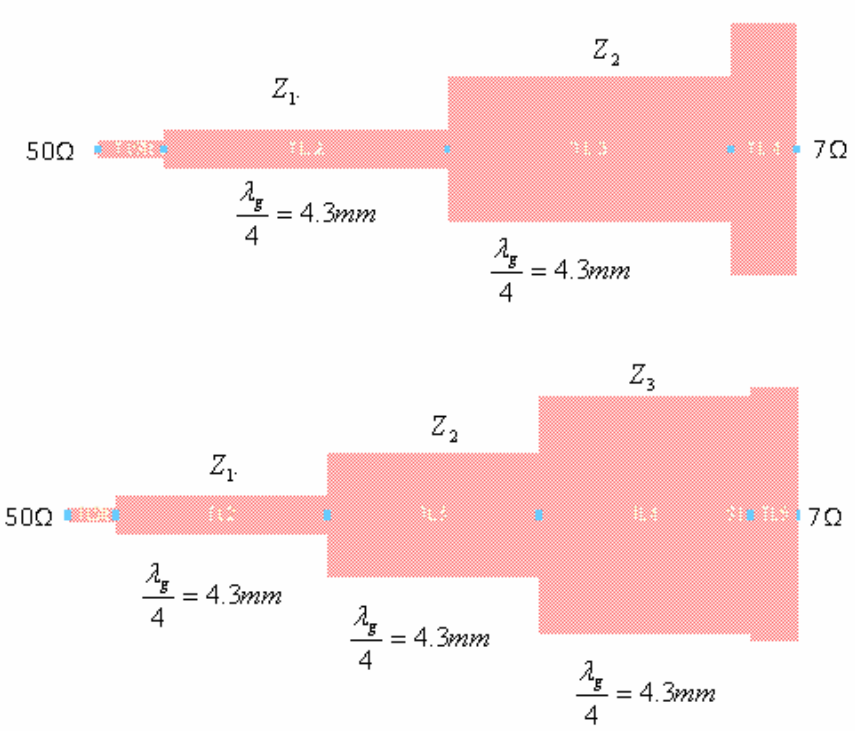


Figure 3-58: Layout of 2 and 3 Stage Matching Sections

Table 3-4: Impedances of Quarter-Wavelength Transformers in 2 and 3 Stage Matching Sections

Number of Sections	Z_1 (Ω)	Z_2 (Ω)	Z_3 (Ω)
2	30.1	11.3	-
3	30.1	12.7	7.4

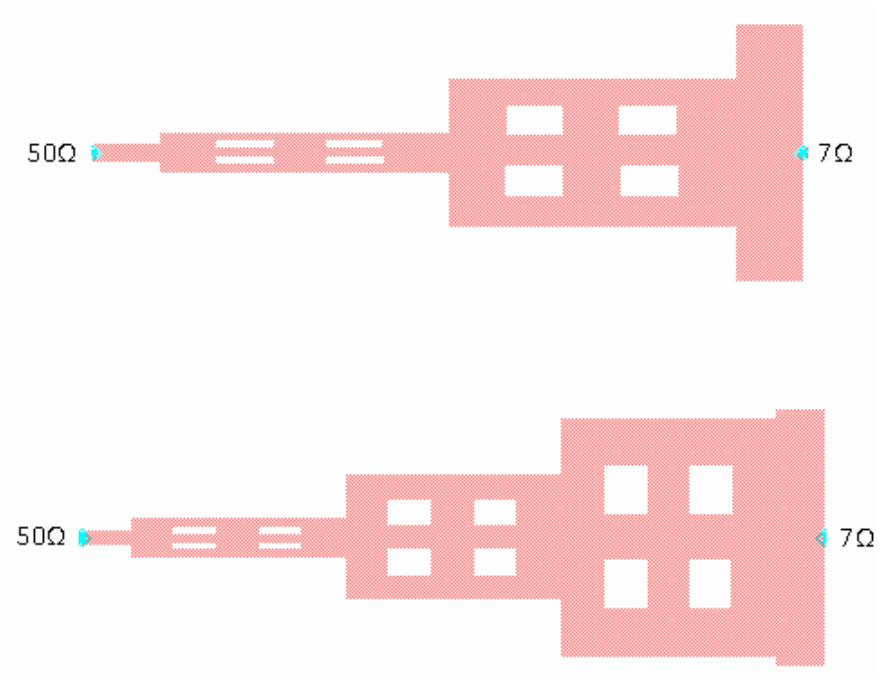


Figure 3-59: Layout of Matching Sections with Sierpinski Square for Iteration Order-1

EM simulation results of both 2 and 3 stage matching sections with zero and first order iterations are given in Figure 3-60 and Figure 3-61 respectively. These results show that for both designs with Sierpinski squares with 1/5 iteration factor, bandwidth is enlarged.

Figure 3-60: EM Simulation Result of 2-stage Matching Section Design

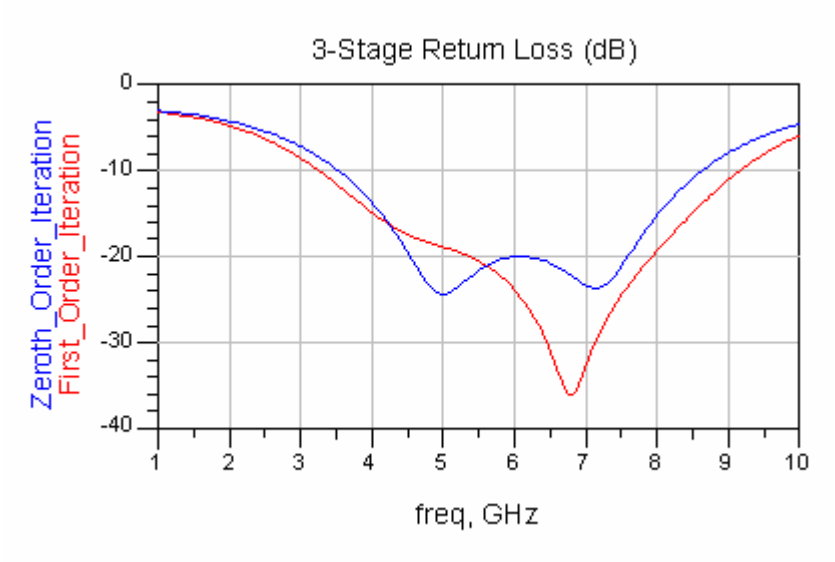


Figure 3-61: EM Simulation Result of 3-stage Matching Section Design

CHAPTER 4

HYBRID FMCW SENSOR DESIGN

Range measurement is a requirement in both military and civil applications, such as proximity fuse, level measuring and vehicle collision warning systems. One of solution for range measurement is FMCW radar. However, in these civil applications small size and low cost of the sensor are important requirements. In this chapter, reduced size FMCW range sensor transceiver design is introduced. Size reduction is achieved by using hybrid technology and miniaturization techniques.

The carrier center frequency for FMCW range sensor is chosen as 6 GHz with bandwidth Δf of 1 GHz. From equation (2.12) range resolution can be found as:

$$\Delta R = \frac{c}{2\Delta f} = \frac{3x10^8}{2x10^9} = 15cm$$

Moreover, for this system minimum range, that can be measured, can be calculated for $f_{b,\min} = 5f_m$ by using (2.10) as:

$$f_{b,\min} = \frac{4\Delta f \cdot f_m}{c} R_{\min} = \frac{4x10^9 x5xf_{b,\min}}{3x10^8} R_{\min} \Rightarrow R_{\min} = 37{,}5cm$$

For modulation frequency of fm=1MHz maximum range that can be measured can also be calculated.

$$R_{\max} \le \frac{c}{4f_m} \Rightarrow R_{\max} = 75m$$

The FMCW range sensor transceiver is composed of its sub-parts; power amplifier, low noise amplifier (LNA), mixer, coupler and front-end structure. The

block diagram of the transceiver is given in Figure 4-1. Impedance matching of transistor in power and low noise amplifier is achieved by spiral inductors and interdigital capacitors. Front-end structure is made up of two stage branch-line coupler and dual-polarized antenna system. The received signal from front-end structure is amplified with LNA and then mixed with a coupled portion of transmitted signal. Therefore, the resultant output is the beat frequency. Design and simulations of all these sub-part will be explained in the remaining part of this chapter.

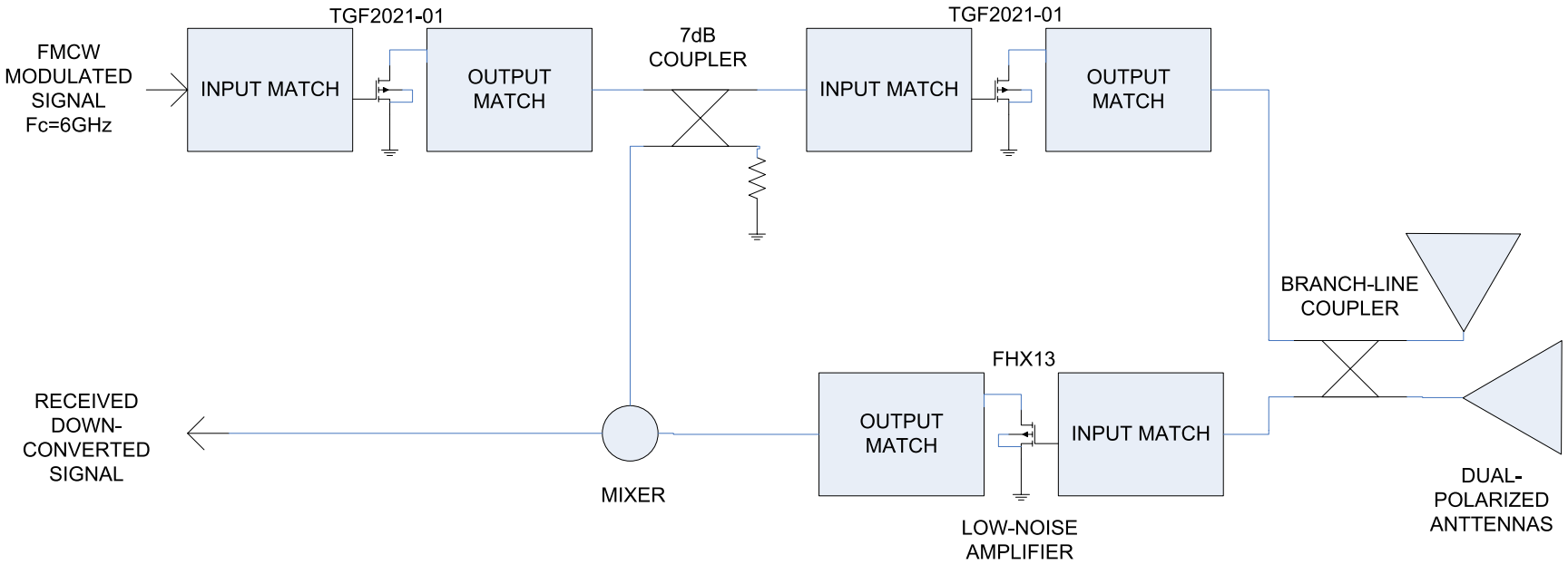


Figure 4-1: Functional Block Diagram of FMCW Transceiver

4.1. Power Amplifier

Power amplifier is the main and an important part of a transceiver. It amplifies the power of the input signal with certain efficiency to desired level. They are either tube based such as travelling tube amplifier or solid state based devices. Tube based amplifiers are not in the scope of this thesis and will not be introduced. Transistors are the main components of solid state technology. However, simply choosing the right transistor is not sufficient for amplifier design. Biasing, input and output matching network are to be designed to get the desired performance from the transistor. A typical single stage power amplifier is given in Figure 4-2. Bias tee consists of DC block capacitors and RF choke inductors in order to isolate DC supply and RF in/out from each other. On the other hand, input and output matching networks are used to match transistor input and output impedances to 50Ω. They are required to achieve desired gain, power, stability, distortion in interested frequency band.

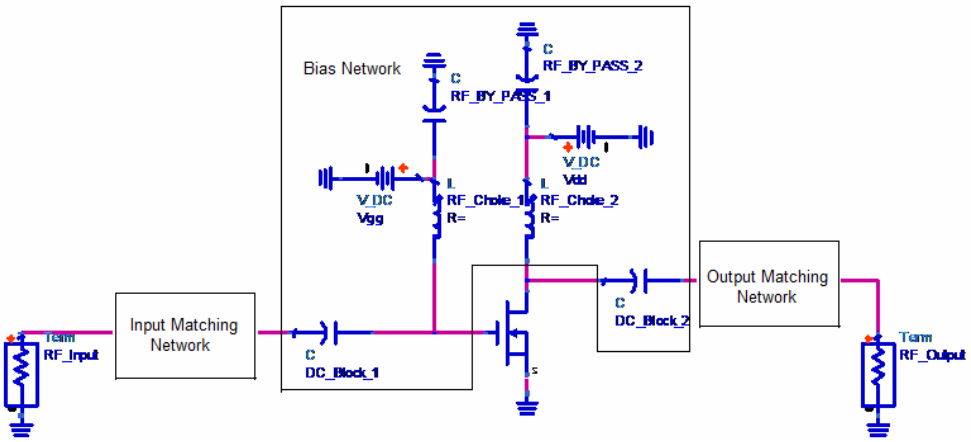


Figure 4-2: A Typical Single Stage Amplifier Schematic

At this point it will be helpful to define gain, efficiency and saturated output power or 1dB compression point. Gain is defied as the ratio of output power to input power. In decibel it can be given as:

$$G = 10\log\left(\frac{Pout}{Pin}\right) \text{ dB} \tag{4.1}$$

Efficiency is the measure of how much of DC power is converted to RF power.

$$Efficiency(\eta) = 100x\frac{RF\_Output\_Power}{DC\_Input\_Power} \quad \% \tag{4.2}$$

Moreover, power added efficiency (PAE) can be defined as the percentage ratio of total output power to total input power:

$$PAE = 100x\frac{RF\_Output\_Power}{RF\_Input\_Power + DC\_Input\_Power} \quad \% \tag{4.3}$$

Another parameter is the output power. In RF power amplifier community, 1 dB compressed power is taken as the maximum output power level of amplifier. The P1dB point is defined as the power level where gain is decreased by 1 dB relative to small-signal.

After defining some basic parameters of power amplifier, it is time to switch design steps of power amplifier of FMCW transceiver. The first step is to choose the right transistor at 6 GHz. The maximum output power is chosen as 1W in order not to encounter thermal constraints. For higher power levels, it will be more difficult to cool very small chip transistors. Therefore, for this application discrete power phemt TGF2021-01 from Triquint Semiconductor is chosen. It has capability of saturated output power higher than 1W and operating frequency band is from DC to 12GHz. Dimensions with 0.57x0.53mm, chip transistor TGF2021-01 is suitable for reduced size FMCW transceiver design.

The manufacturer supplies the linear model and S-parameters of this transistor for several bias conditions. This model and S-parameters will be used in design and simulation of power amplifier. Highest drain voltage 12V with I_{dq}=75mA is chosen and corresponding model for this case is given in Figure 4-3.

In the first step of design, ideal inductors and capacitors are used for biasing and matching. In this step, input and output return losses of better than -10 dB and gain higher than 12 dB is aimed. Simple low-pass series inductor, shunt

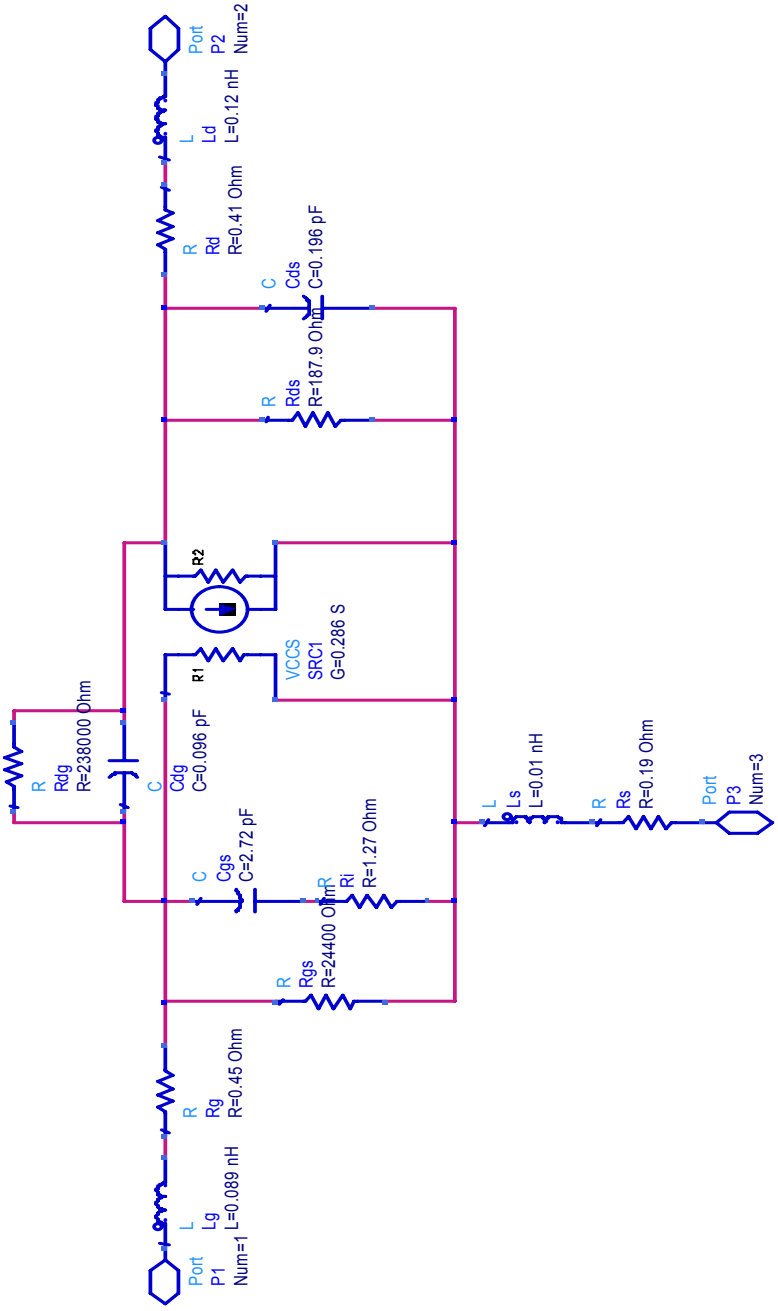


Figure 4-3: Linear Model of TGF2021-01 @ Vd=12V, Idq=75mA

capacitor matching is tried. By using Agilent ADS simulation tool is executed with the help of optimization tool. The resultant design is shown schematically in Figure 4-4 and the component values are tabulated in Table 4-1. The corresponding simulation results including input/output return losses and gain are given in Figure 4-5. According to these results aims are achieved.

In the schematic given in Figure 4-4, it is also notable that an R-L-C circuit from gate to drain is added. This addition is due to the stability considerations. Rollet stability factor, K can be used as the measure of stability [3]. It must be greater than 1 for unconditionally stability. K factors are found as in Figure 4-6, before and after the addition of the stability circuit to the design. Without stability circuit, K factor becomes lower than 1, which means that circuit is potentially unstable. Therefore, for unconditional stability, gate to drain feedback is to be added.

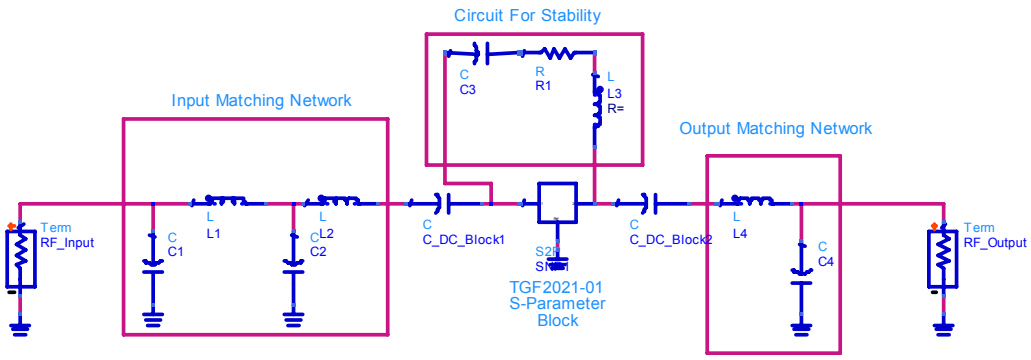


Figure 4-4: TGF2021-01 Input & Output Match with Ideal Components

Table 4-1: Ideal Component Values for TGF2021-01 Match

Component Name	Value
C1	1 pF
C2	3.2 pF
C3	1 pF
C4	0.5 pF
C_DC_Block1	6.4 pF
C_DC_Block2	6.4 pF
L1	0.8 nH
L2	0.45 nH
L3	1 nH
L4	0.7 nH
R1	130 Ω

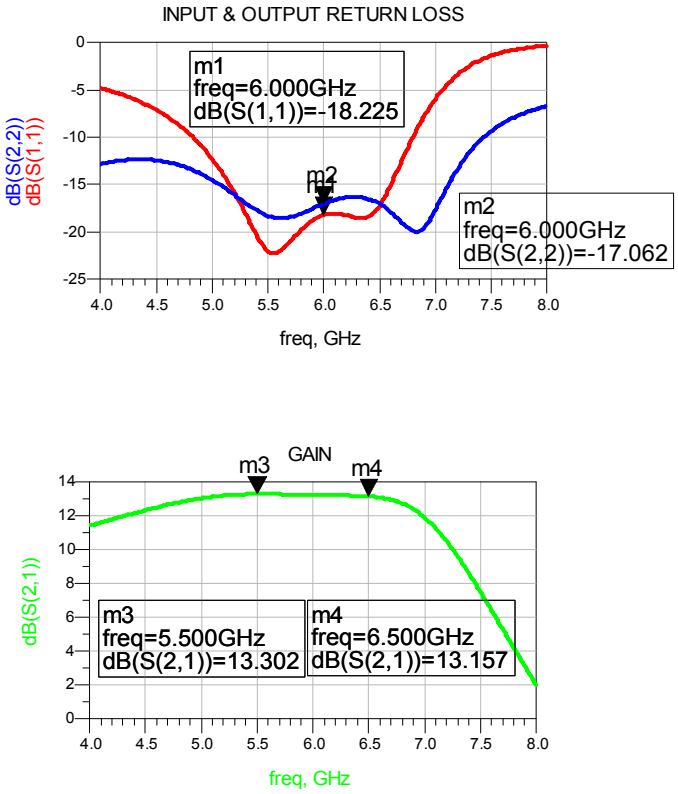


Figure 4-5: Simulation Results of Ideal Component Match of TGF2021-01

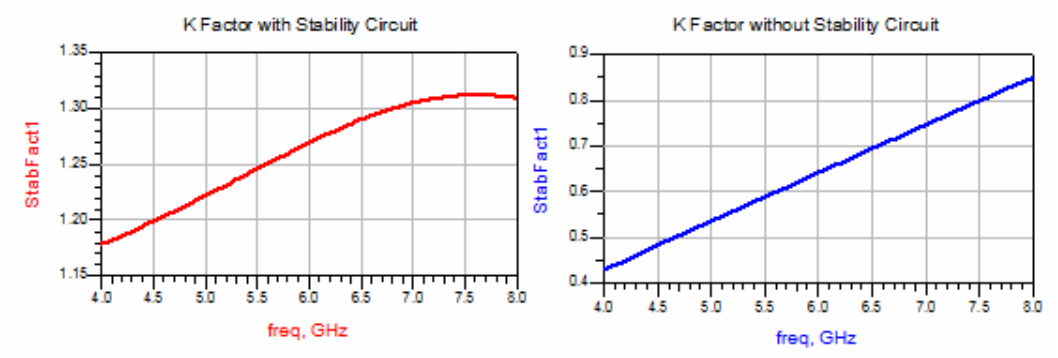


Figure 4-6: Stability Factor-K with and without Stability Circuit

The feedback resistor can be implemented with hybrid technology. In the fabrication, resistive thin films are widely used. Nickel Chrome, having a sheet resistance of 20 Ω / square, is one of the resistive materials. In order to implement 130 Ω with NiCr, 6.5 square sheets must be cascaded.

In the second step of design, the desired inductance and capacitance values given in Table 4-1 are obtained using by interdigital capacitors (IDC) and spiral inductors (SI) as explained in Chapter 3. Again Alumina is used as substrate in simulations (ε_r =9.6, h=0.25mm, tanD=0.001).

In Chapter 3, three spiral inductors with simulation results are given. These values 0.44 nH, 0.95 nH, 0.7 nH are very close to inductors L2, L3, L4 and can be directly used. However, new dimension for L1 must be found. So, 400x350 µm is chosen and simulated. Its value is found to be very close to 0.8 nH. Besides, an RF choke inductor for gate and drain bias is needed. This time a large value of inductor is needed, so number of turns is increased to 2 ¾. This new layout is given in Figure 4-7. As in previous inductors, 50 µm conductor width and 25 µm width between conductors are used. X and Y dimensions are chosen as 1000 µm and 900 µm respectively and simulated. The simulation results including magnitude and phase of return and transmission loss of both EM simulation and circuit model are shown in Figure 4-8. Finally, all circuit parameters and dimensions of spiral inductors are summarized in Table4-2.

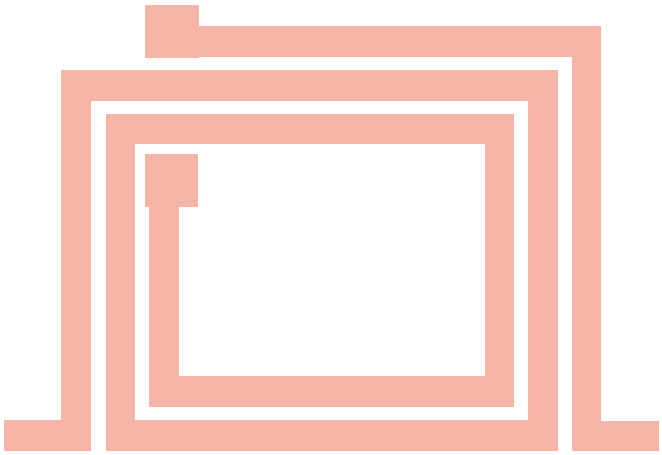


Figure 4-7: Layout of 2 ¾ Turn Spiral Inductor

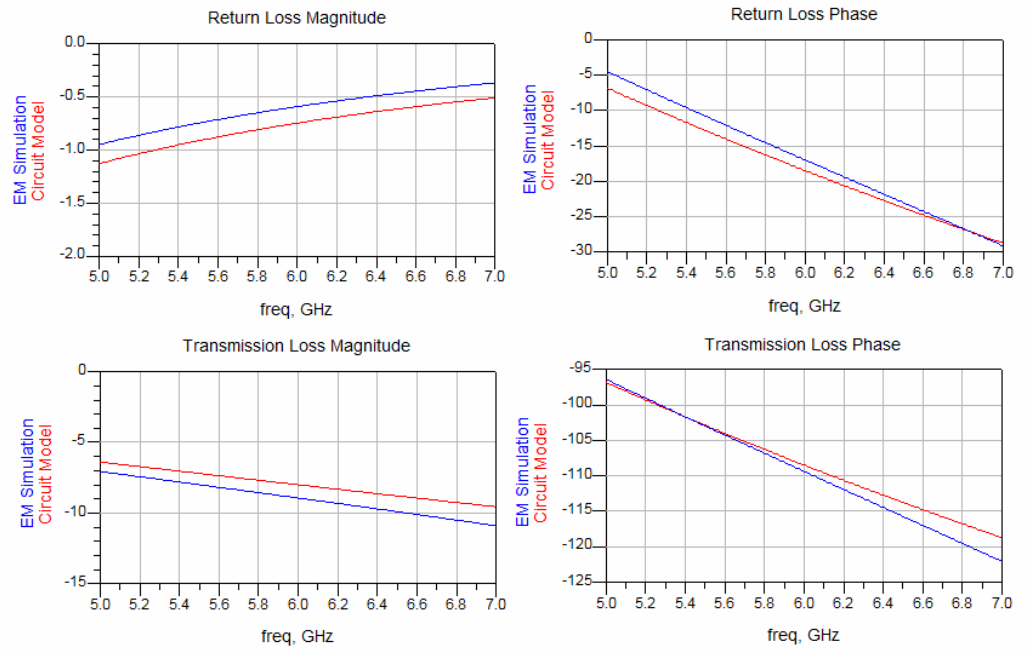


Figure 4-8: EM and Circuit Model Simulation Results of Spiral Inductor with Dimensions 1000x900 µm

Table 4-2: Dimension and Equivalent Circuit Component Values of Simulated Spiral Inductors

Inductor Symbol	**Condition**	**Ls (nH)**	**Rs (Ω)**	**Cp (pF)**
L1	Lx=400 µm Ly=350 µm	0.814723	0.00001051	0.053055
L2	Lx=250 µm Ly=300 µm	0.440569	0.00051	0.035055
L3	Lx=400 µm Ly=400 µm	0.946799	0.00008169	0.0568157
L4	Lx=400 µm Ly=320 µm	0.709831	0.00000119	0.0477169
RF_Choke	Lx=1000 µm Ly=900 µm	6.22667	0.0000442	0.203231

After obtaining the inductors and their S-parameters, it is time to find dimension and number of fingers of 0.5 pF, 1 pF and 3.2 pF IDCs. For this purpose, EM simulation results in Chapter 3 are taken as reference and new dimensions for C1, C2, C3, and C4 are found. The circuit model, EM simulations and equivalent circuit simulation results of 0.5 pF, 1 pF, and 3.2 pF in S-parameter form are given in Figure 4-9, Figure 4-10 and Figure4-11, respectively. In these results error between circuit model and EM simulation of IDC is very small and can be neglected. The equivalent circuit model parameters and IDC parameters for C1, C2, C3 and C4 are tabulated in Table 4-3. Instead of DC block capacitors, it is planned to use two parallel 3.2 pF IDC.

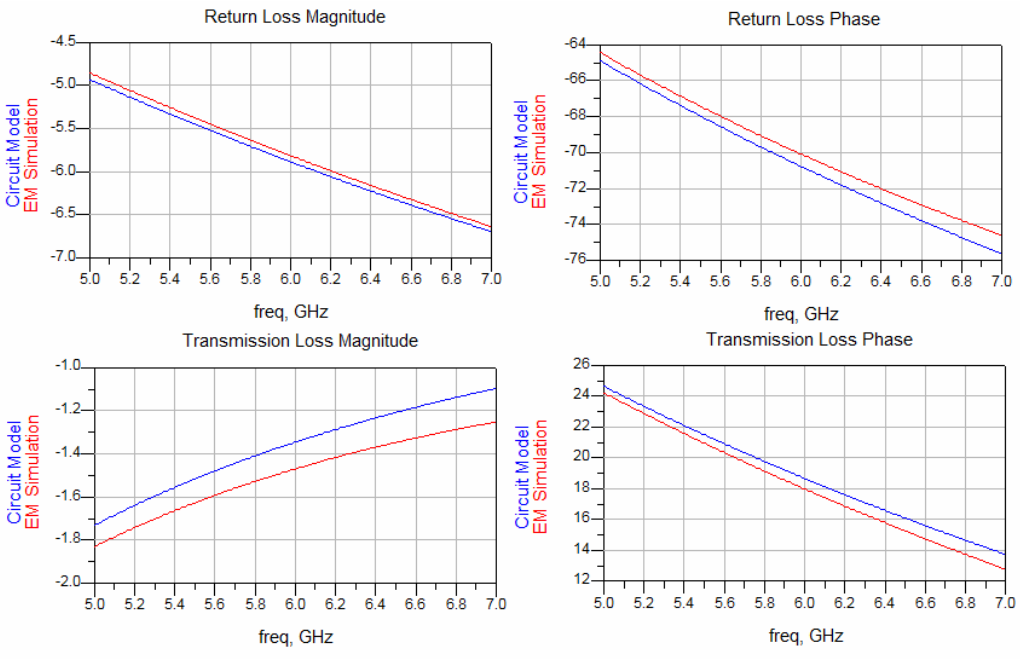


Figure 4-9: EM Simulation and Circuit Model Results of L=350um, W=30um, Wt=30um and N=8

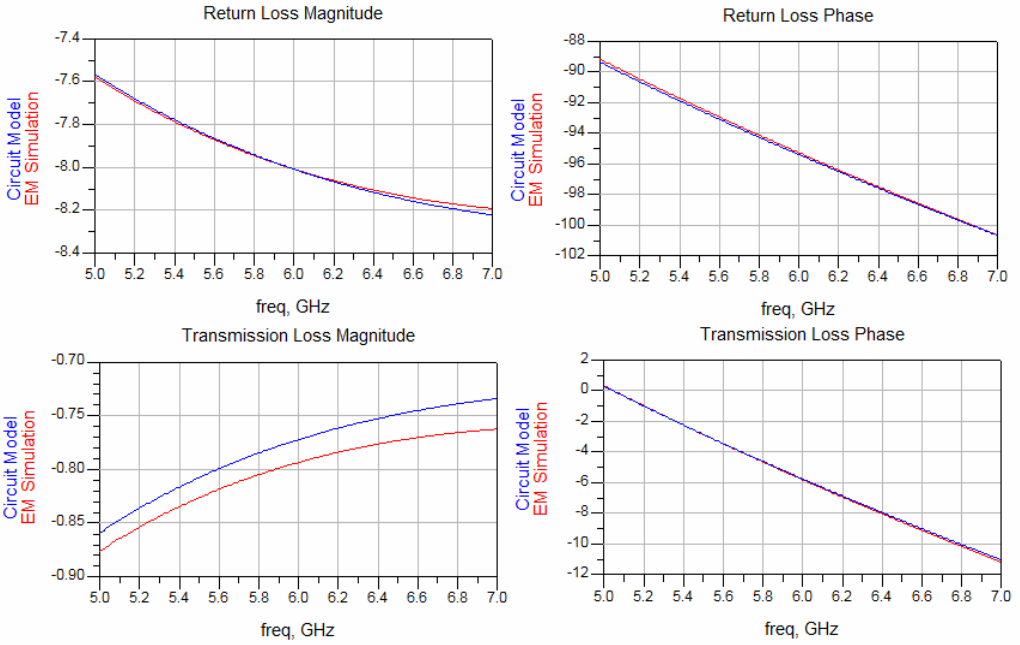


Figure 4-10: EM Simulation and Circuit Model Results of L=500um, W=30um, Wt=30um and N=12

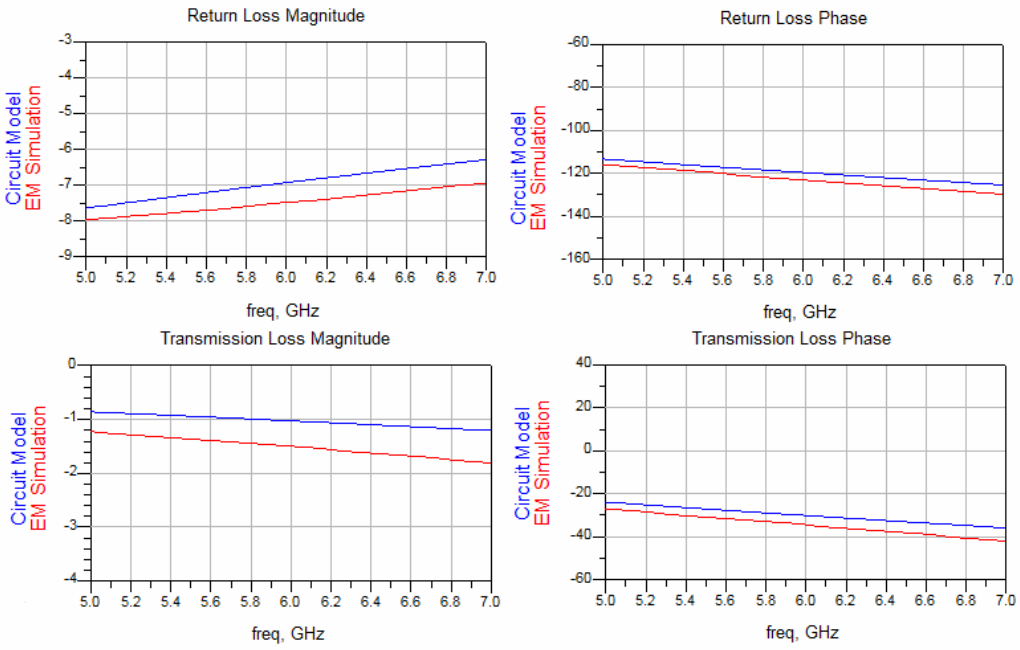


Figure 4-11: EM Simulation and Circuit Model Results of L=500um, W=30um, Wt=30um and N=12

Table 4-3: Dimension and Equivalent Circuit Component Values of Simulated Interdigital Capacitors

Capacitor Symbol	Condition	Ls (nH)	Cs (pF)	Rs (Ω)	Cp (pF)
C4	L=350um, W=30um, Wt=30um, N=8	0.0645349	0.492667	0.5	0.0504617
C1, C3	L=500um, W=30um, Wt=30um, N=12	0.200759	0.987028	0.176207	0.132801
C2	L=1000um, W=30um, Wt=30um, N=20	0.21918	3.15840	0.295	0.27879

All ideal inductor and capacitors in amplifier design can be replaced with SI and IDC equivalents. However, before to do so, an RF by-pass capacitor as seen in Figure 4-2 is to be designed. It is used to show short circuit for RF signal for related frequency. Here, radial stub will be used for broadband RF short. Again on Alumina substrate 50° radial stub is simulated and 2.7 mm length is found as short point for 6 GHz. However, this length is long for a miniaturized hybrid amplifier design. Therefore, technique that is introduced in Chapter 3 will be applied. For this purpose, different lengths of radial stub that is smaller than 2.7 mm with a radial slot are tried. It is found that total length can be decreased to 2.2 mm for 6 GHz RF short. The optimum slot length is 1.6 mm with feedline length of 10 µm. The layouts of radial stub before and after miniaturization are given in Figure 4-12. The corresponding simulation results for both cases are shown in Figure 4-13. Again as in Chapter 3, it is obvious that after miniaturization of radial stub bandwidth degrades.

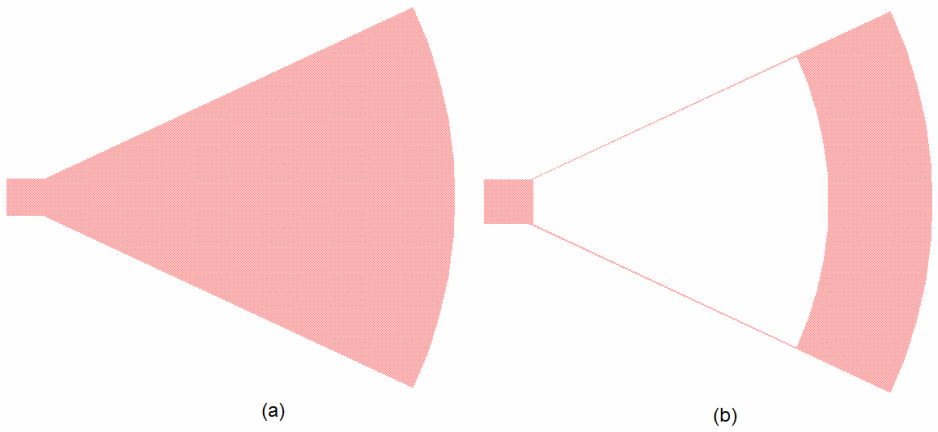


Figure 4-12: Layouts of Radial Stub on Alumina (a) Before and (b) After Miniaturization

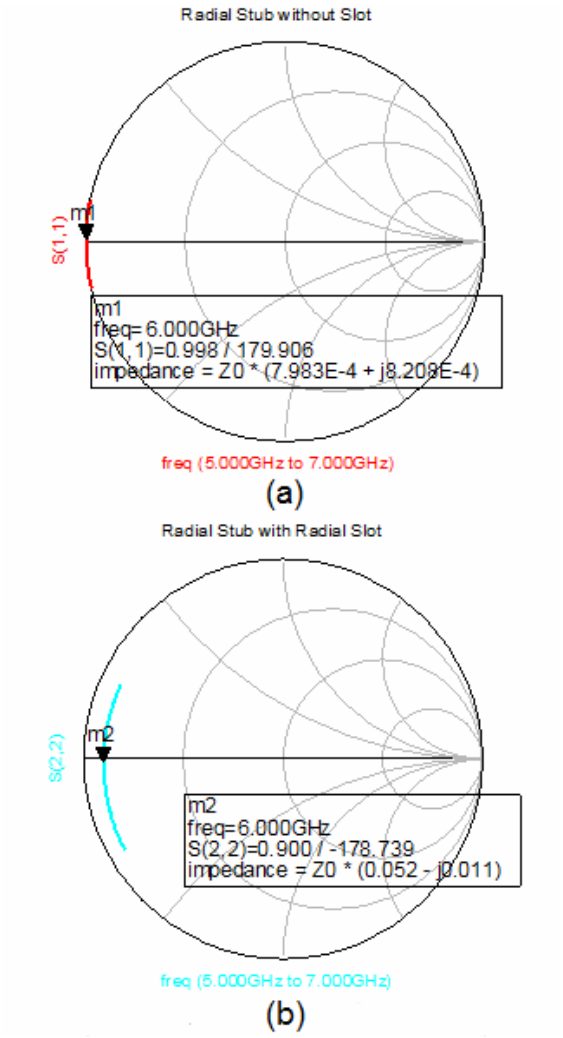


Figure 4-13: The Simulation Results of Radial Stub on Alumina (a) Before and (b) After Miniaturization

In the final step of power amplifier design, ideal matching components are interchanged with S-parameter blocks of equivalent IDCs and SIs. In this step, effects of wire bonding in chip transistor connections to circuit layout is also included. The inductance of wire bond connection is calculated as 0.05 nH in Chapter 3. This inductance effect is included in simulations. The final results of single stage power amplifier design with IDCs and SIs are given in Figure 4-14. It is obvious from these results that degradation is seen for both I/O return losses and gain due to the parasitic effect of both IDC and SI. However, these results still fulfill the aim at the beginning of design. Return losses are lower than -10 dB and gain is higher than 12 dB. This much gain with 30 dBm (1 W) output

power is not enough to drive amplifier with a power level lower than 10 dBm which is maximum synthesizer output. Therefore, two stage of gain block is needed. In this study, identical two TGF2021-01 amplifier stages are cascaded. The simulation results of this new form are given in Figure 4-15. With two stage amplifier, 25 dB gain in 5.5-6.5 GHz band is obtained. So, all amplifier design steps are achieved.

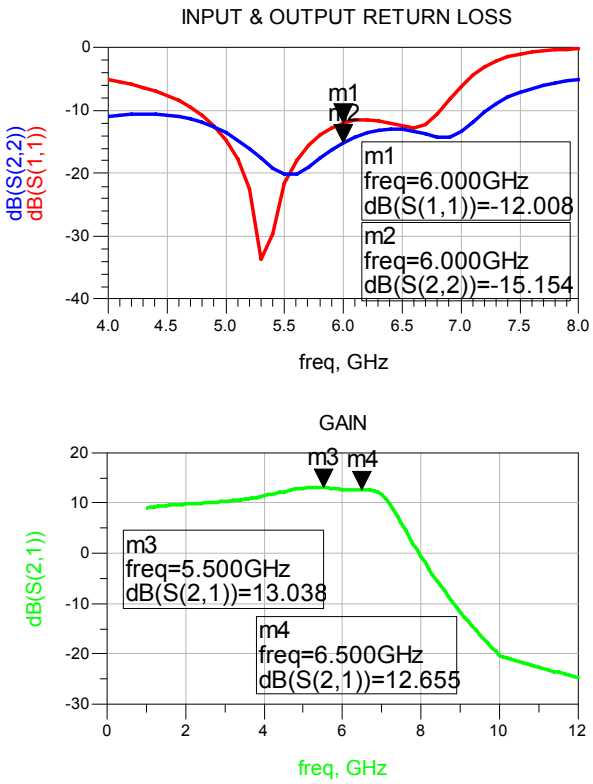


Figure 4-14: Simulation Results of TGF2021-01 I/O Match with IDCs and SIs

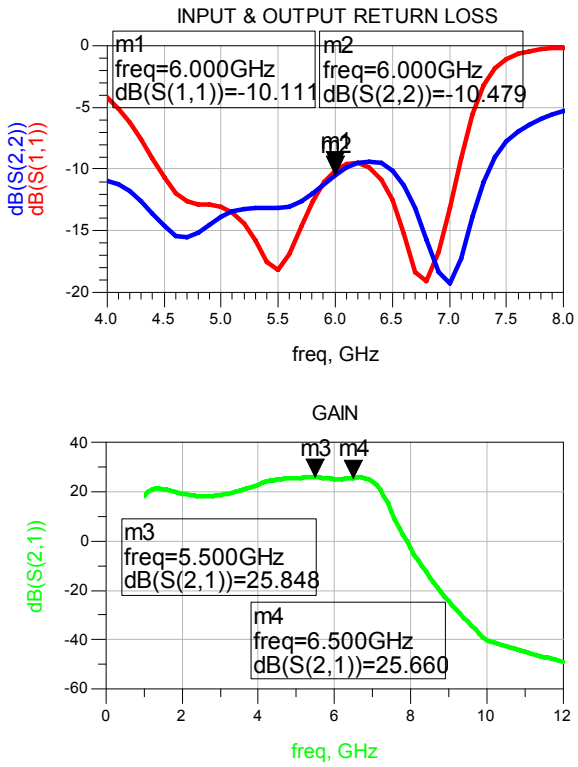


Figure 4-15: Simulation Results of Two Cascaded TGF2021-01 Amplifier

4.2. Low Noise Amplifier

The low-noise amplifier (LNA) is an amplifier used to amplify very weak signals captured by antennas. It is usually located very close to the detection device to reduce losses in the feedline. Using an LNA, the effect of noise from subsequent stages of the receive chain is reduced by the gain of the LNA. In other words, the noise figure of the first stages of receiver path is more important than the others. Noise figure (NF) is a measure of degradation of the signal-to-noise ratio (SNR) at the output of the LNA compared to that at the input. According to Friis formula, total noise figure of the receiver can be formulated in terms of gain and noise figures of individual stages as [26]:

$$F_{total} = F1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots \quad (4.4)$$

Therefore, the noise figure and gain of the first stage is very critical for noise

performance of the receiver. In this part of the study, LNA design steps will be introduced and simulation results of an LNA for FMCW transceiver system will be given.

A typical LNA with input and output transformers can be seen in Figure 4-16. For LNA, two kinds of match can be talked about; noise and impedance match. Since the noise performance is merely related to input impedance, input transformer is used for noise match [2]. So, input return loss has minor importance compared with noise figure. On the other hand, output transformer is used to match output impedance to 50 Ω and to get desired gain. Both input and output matching networks consist of inductors, capacitors or distributed transmission lines. Resistors are not preferred, because they introduce noise to system. However, they may be needed for stability considerations.

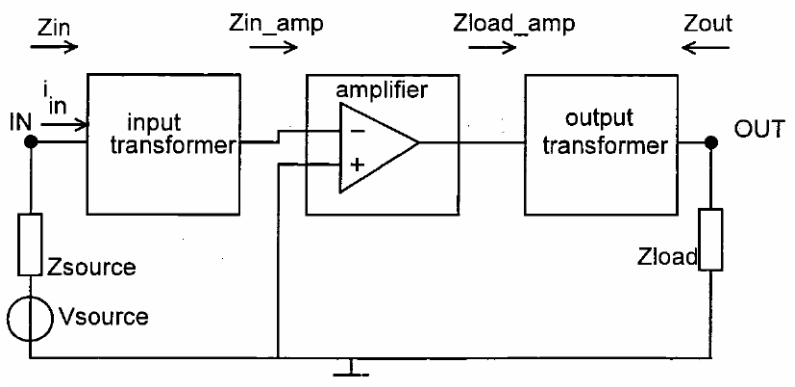


Figure 4-16: LNA with Input and Output Transformers

Let's first summarize design steps of a typical LNA:

- Stability performance is to be checked by calculating Rollet stability factor K using S-parameters of the transistor at the corresponding frequency band.
- If the transistor is potentially unstable, that is to say K is lower than unity; it can be stabilized by adding a ballast resistor at the drain or a

feedback resistor from drain to source. However, this resistive network will increase the noise figure.

- In a simulation tool, NF_{min} and Γ_{opt} are found and a desirable NF higher than NF_{min} is chosen.
- An input reflection coefficient Γ_s or input impedance Z_s that is on the circle of chosen noise figure on Smith chart and is in the stable region is chosen.
- Optimum output impedance is found to get desired gain from the transistor.
- These input and output impedances Z_s and Z_L are matched to reference Z_0 which is usually 50 Ω. This can be done by lumped components like LC based network or distributed elements like open or short-circuited stubs.

For FMCW transceiver design, Eudyna FHX13X chip GaAs FET is planned to use in LNA design. As in the power amplifier part, biasing and matching networks are designed using ideal lumped components. Then, these ideal elements will be replaced by IDC and SI equivalents.

The S-parameter of FHX13X, which is supplied by manufacturer, is used in simulations. Before starting noise and impedance match, the stability condition is to be checked. In order to check stability, the circuit in Figure 4-17 with bias inductors 6.2 nH and feedback network is used. The resulting K factors with and without feedback resistor 1250 Ω is given in Figure 4-18. It is obvious that without stability circuit, FHX13X is potentially unstable. Therefore, a feedback resistor 1250 Ω is used in simulations.

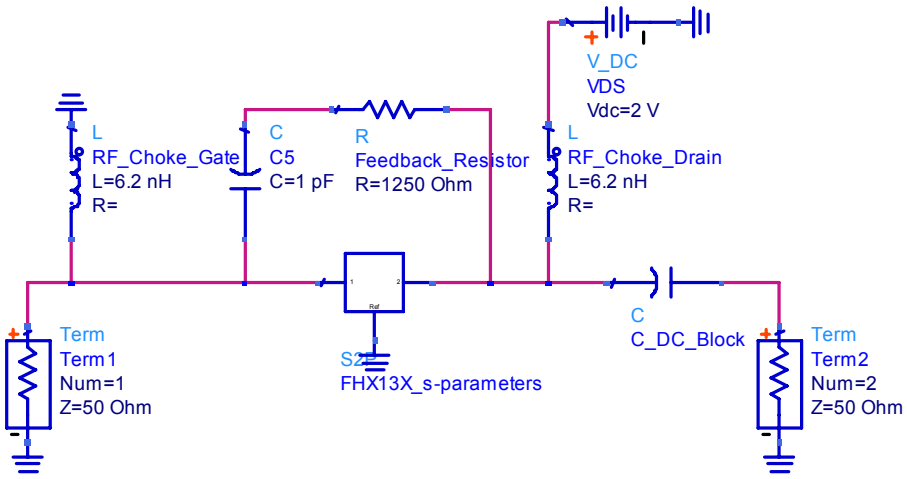
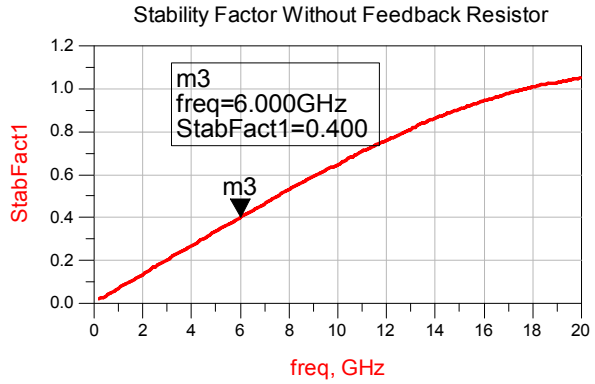
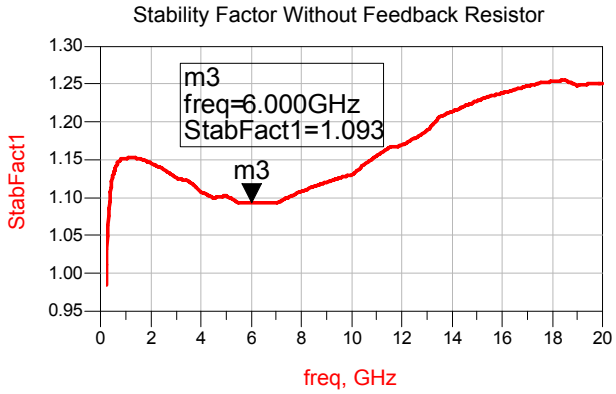


Figure 4-17: Schematic of FHX13X with Bias and Stability Circuits



(a)



(b)

Figure 4-18: Stability Factor K of FHX13X (a) without (b) with Stability Circuit

In the next step of design, optimum noise impedance for noise match will be found. To do so, ADS LNA design example template is used. In this template, for

the chosen point on Smith chart, it gives the noise figure, source impedance, optimum load impedance and stability factor K. Thorough out these simulations FHX13X S-parameters with bias and feedback circuit is used. Before start this step, the role of feedback resistor on noise figure can be determined. For with and without feedback resistor cases, minimum NF of LNA is calculated as 1.162 and 0.32 respectively. This shows that minimum NF of the LNA is increased when an unconditionally stable case is needed.

At the center frequency 6 GHz, available gain, noise, stability circles of FHX13X using ADS LNA simulation template is shown in Figure 4-20. Among those circles, red one shows source stability circle. Outside of this circle is the unconditionally stable region. Therefore, all points inside of Smith Chart are stable which is achieved by feedback resistor. Moreover, blue and brown circles show constant gain and noise figure respectively. For small circles, corresponding gain is high and NF is low. By considering ease of matching, marker GammaS point is chosen for optimum gain and NF. The corresponding NF and source impedance are given in Figure 4-19. After finding source impedance, it is to be matched to 50 Ω and then, load matching network is to be determined for optimum gain and I/O return losses.

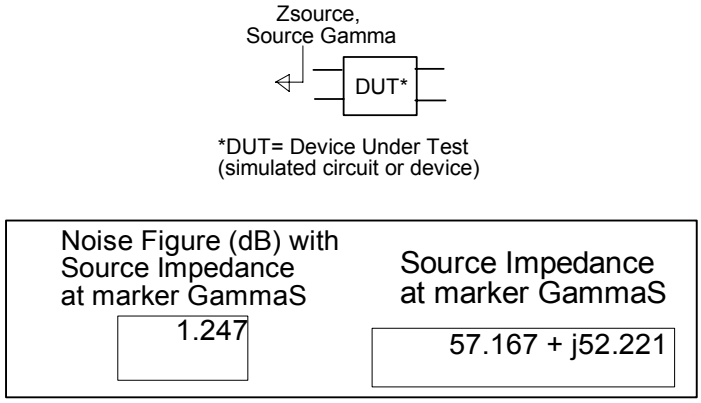


Figure 4-19: The Noise Figure and Source Impedance at Marker GammaS

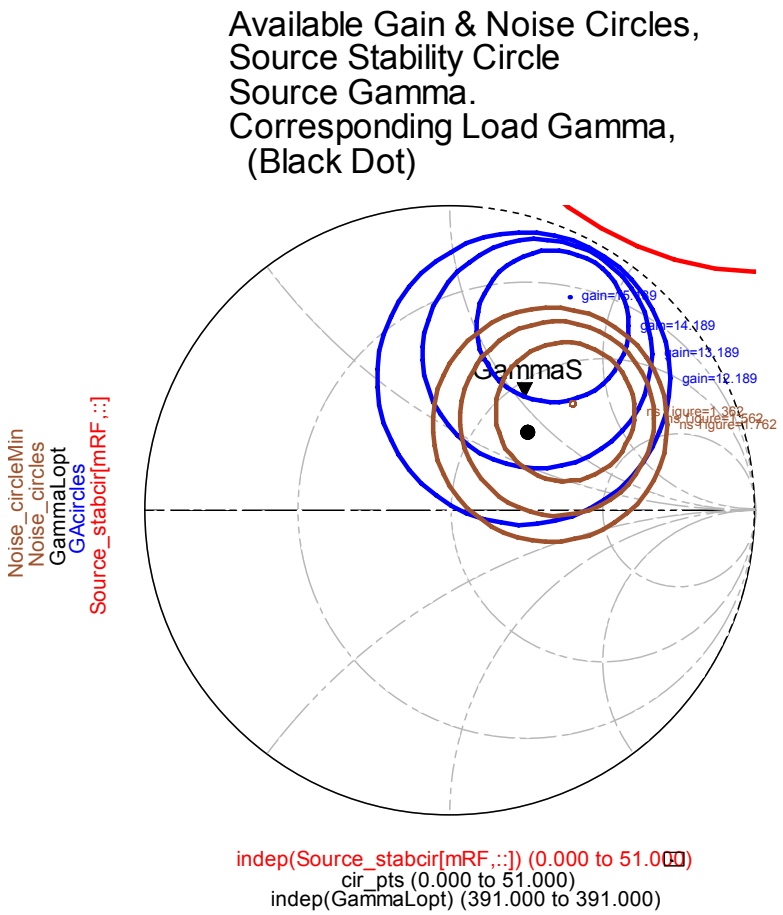
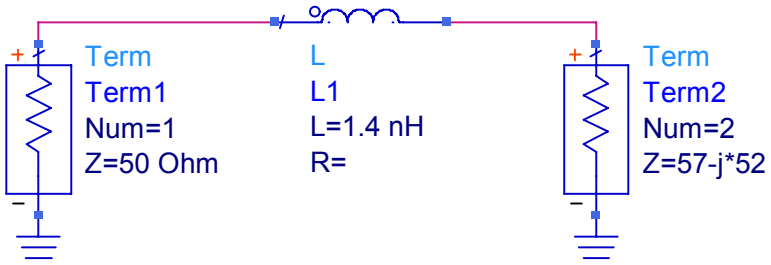
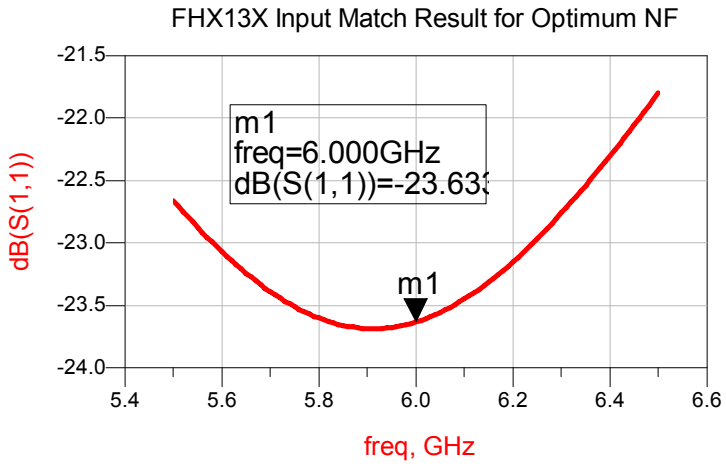


Figure 4-20: Gain, Stability and Noise Circles of FHX13X on Smith Chart

The real part of the source impedance is close to 50 Ω. So, an inductor will be enough to match noise impedance to 50 Ω. In simulation 1.4 nH of inductance is found to be optimum for this purpose. The ADS schematic and corresponding simulation results are given in Figure 4-21 (a) and Figure 4-21 (b). These results show that for NF 1.247 dB source match is achieved. Now, it is time to match output for required gain higher than 10 dB in frequency band 5.5- 6.5 GHz. To achieve this purpose, a simple series capacitance is found to be suitable by optimization, which can also be used for DC block. The final schematic and simulation results of LNA design are shown in Figure 4-22. Gain of FHX13X is 12 dB despite the degradation effect of feedback resistor. Moreover, return loss is less than -10 dB with noise matching network.



(a)



(b)

Figure 4-21: (a) The Schematic, (b) Return Loss of Source Match for FHX13X

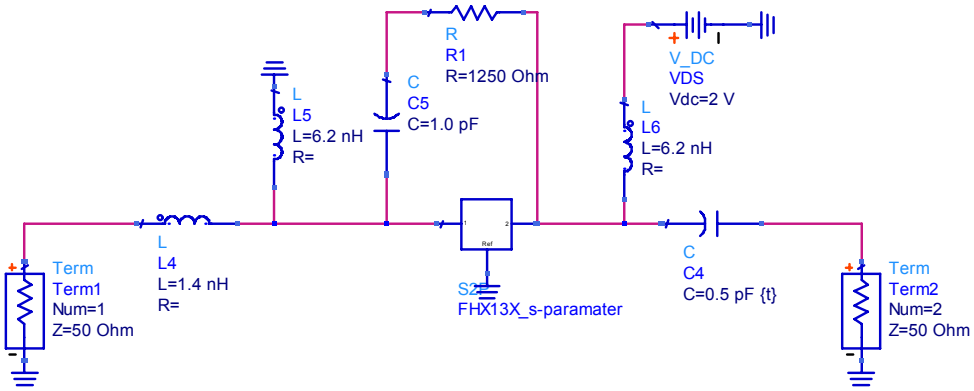
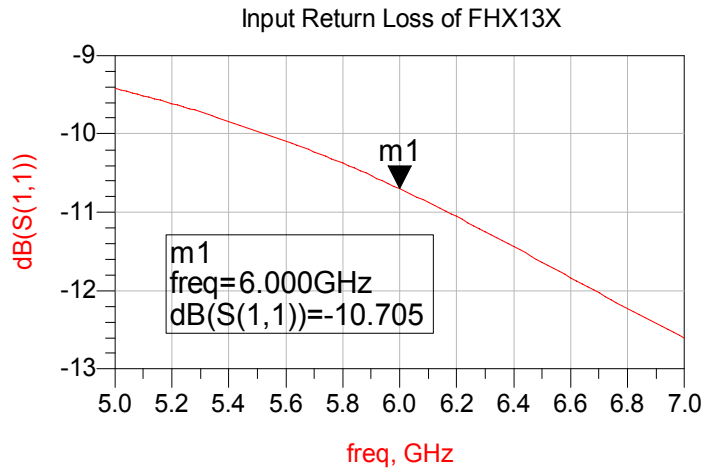
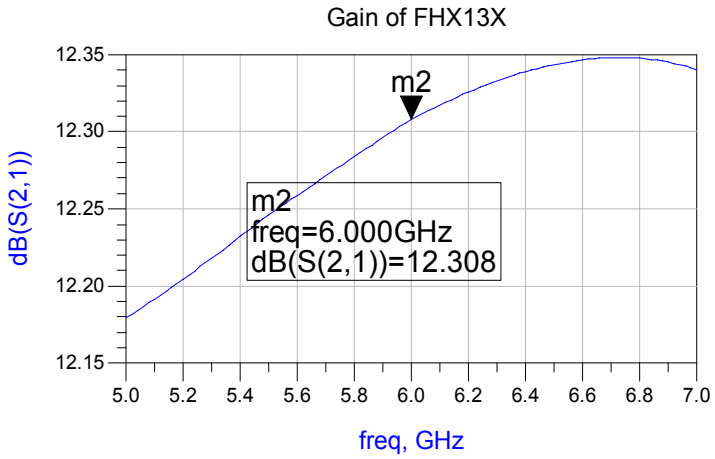


Figure 4-22: Final Schematic of FHX13X LNA Circuit



(a)



(b)

Figure 4-23: (a) Return Loss, (b) Gain of FHX13X with Ideal Components

After obtaining ideal component values for FHX13X matching, as in case of power amplifier all L-C components will be replaced with SI and IDC equivalents. However, except 1.4 nH all other components' equivalents are already found in previous parts. It is enough to find SI equivalent of 1.4 nH. To do this, 1 nH SI with 400x400 µm x-y dimensions and 1 ¾ turn is taken as reference and for 1.4 nH 510x510 µm is tried on Alumina substrate with ADS Momentum EM simulation tool. In this EM simulation series inductance is found 1.38 nH which is very close to required value. The equivalent circuit parameters are shown in Figure 4-24. Moreover, EM and equivalent circuit simulations in terms of magnitude and phases of return and transmission losses

are given in Figure 4-25. These results indicates that parasitic effects of SI such as Cp are low enough and EM and circuit model simulations gives very close results. Therefore, instead of 1.4 nH ideal inductor, 510x510 µm, 1 ¾ turn SI can be used.

Figure 4-24: Circuit Model Schematic of Spiral Inductor with Dimensions 510x510 µm and 1 ¾ Turn

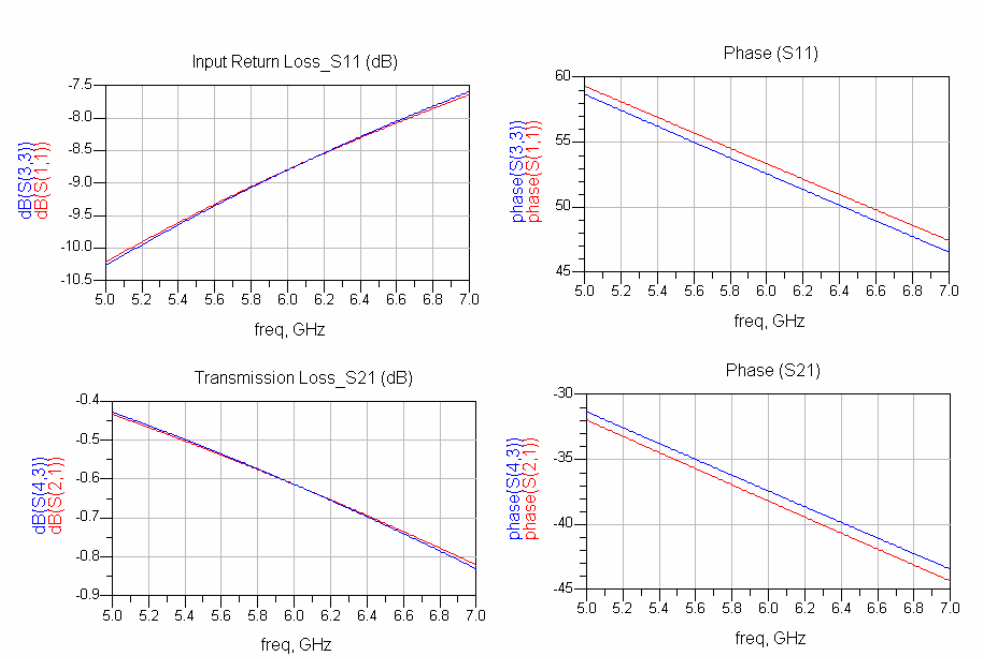
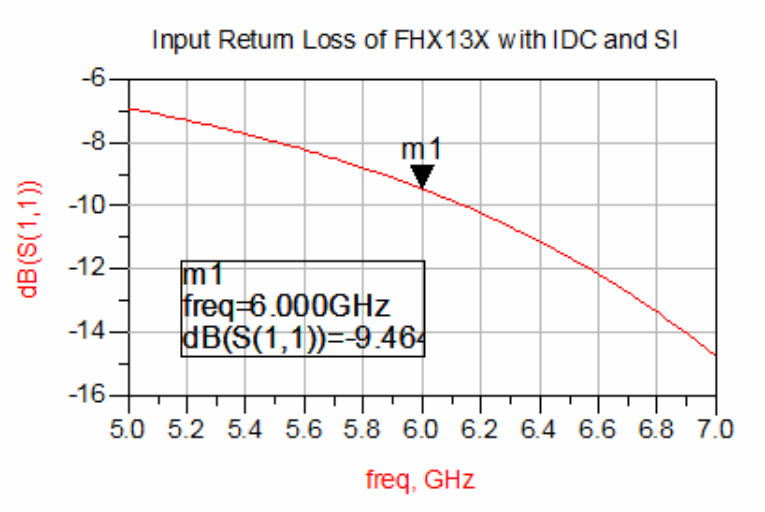
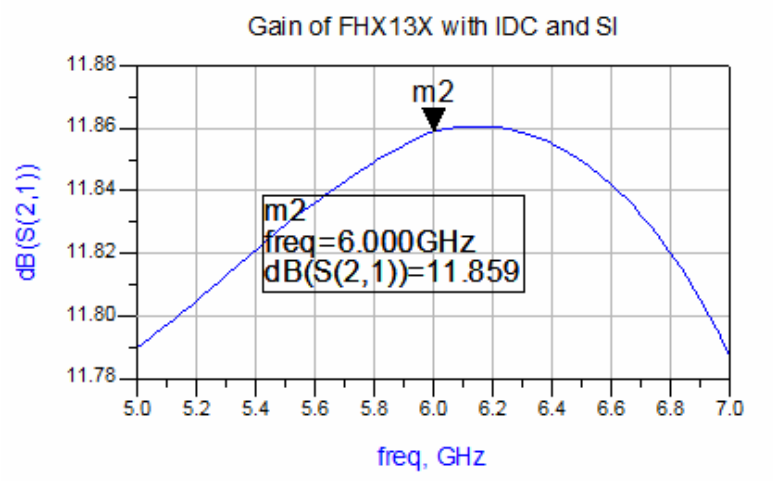


Figure 4-25: EM and Circuit Model Simulation Results of Spiral Inductor with Dimensions 510x510 µm and 1 ¾ Turn

In the final step of LNA design, ideal circuit components are replaced by S-parameter blocks of SIs and IDCs. The corresponding return loss and gain of FHX13X is found as in Figure 4-26. As can be seen from graphs, gain of LNA is approximately 11.8 dB, which is still an acceptable value.



(a)



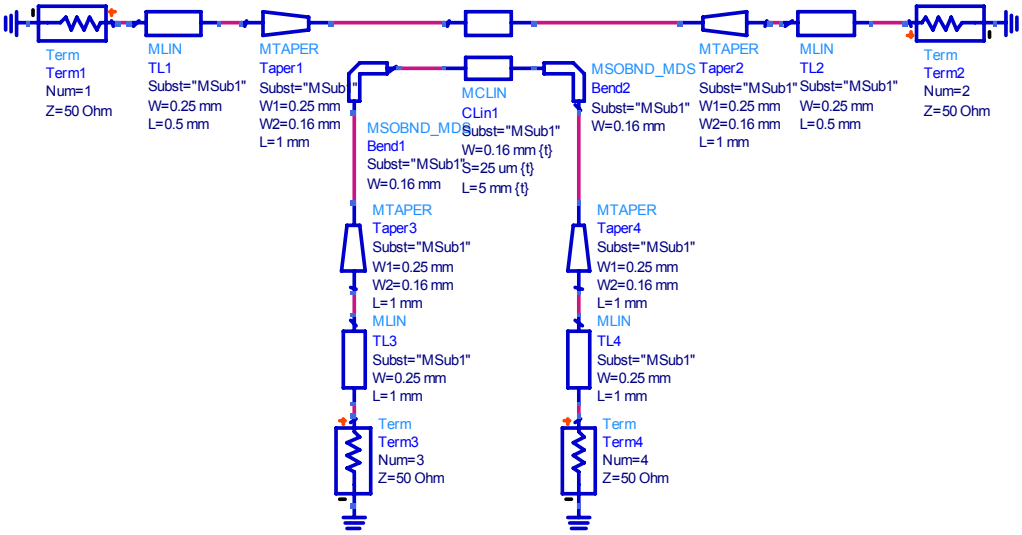
(b)

Figure 4-26: (a) Return Loss, (b) Gain of FHX13X with Ideal Components

4.3. Coupler and Front-End Structure

In this part of the chapter coupled-line coupler and branch-line coupler design details will be given. As can be seen in Figure 4-1, a coupled-line coupler is used to sample the transmitted microwave signal. This sampled signal is used as local oscillator (LO) input of mixer. Hittite HMC525 chip GaAs MMIC mixer for frequency band 4-8.5 GHz is used. By considering input 1 dB compression point and conversion gain of mixer approximately 10-13 dBm LO input is required.

The coupler is placed between power amplifier stages. For 30 dBm power output and 12 dB single stage gain the power level at output of first power amplifier stage will be 18 dBm. Therefore, combining all these gives that 5-8 dB coupler is needed. 7 dB is chosen as design parameter.



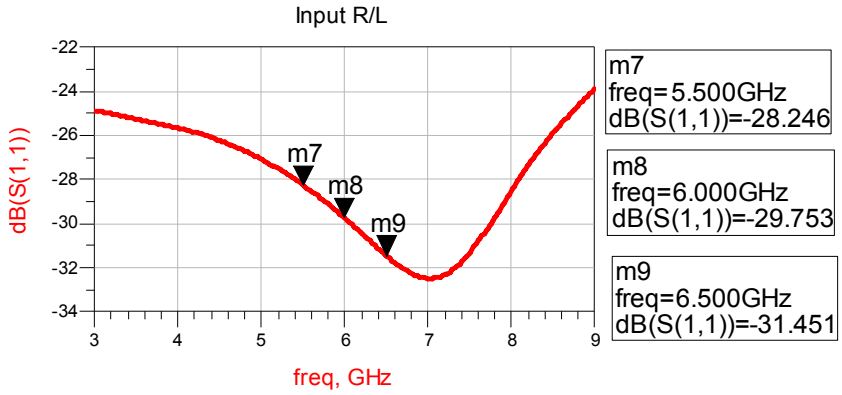
(a)

(b)

Figure 4-27: (a) Schematic, and (b) Layout of 7 dB Coupled-Line Coupler

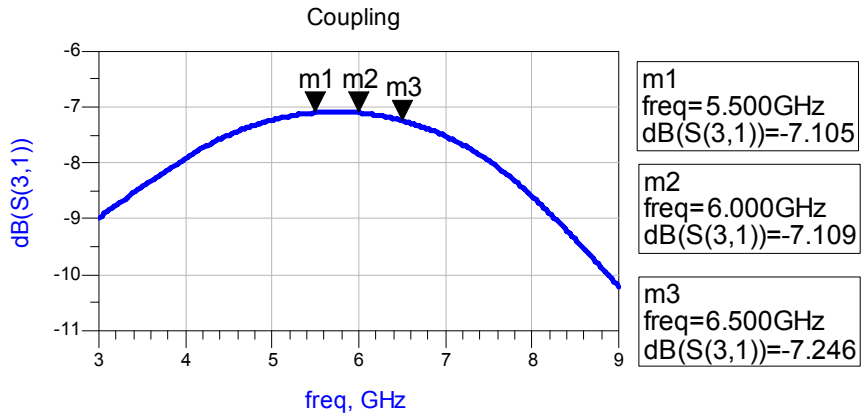
In the design of 7 dB coupled-line coupler on Alumina substrate, coupled-line, tapered lines and transmission line are used as seen in Figure 4-27. The length, width and spacing of coupled-line for 7 dB coupling in frequency band 5.5-6.5 GHz is found by optimization. The remaining feed lines are 50 Ω transmission lines. The EM simulation results including input return loss, coupling ratio and insertion loss are given in Figure 4-28. These results show that 7.1 ± 0.1 dB

coupling is achieved. Furthermore, insertion loss reaches to 1 dB due to high coupling ratio. Finally, it seems that 7 dB coupler is realizable.



(a)

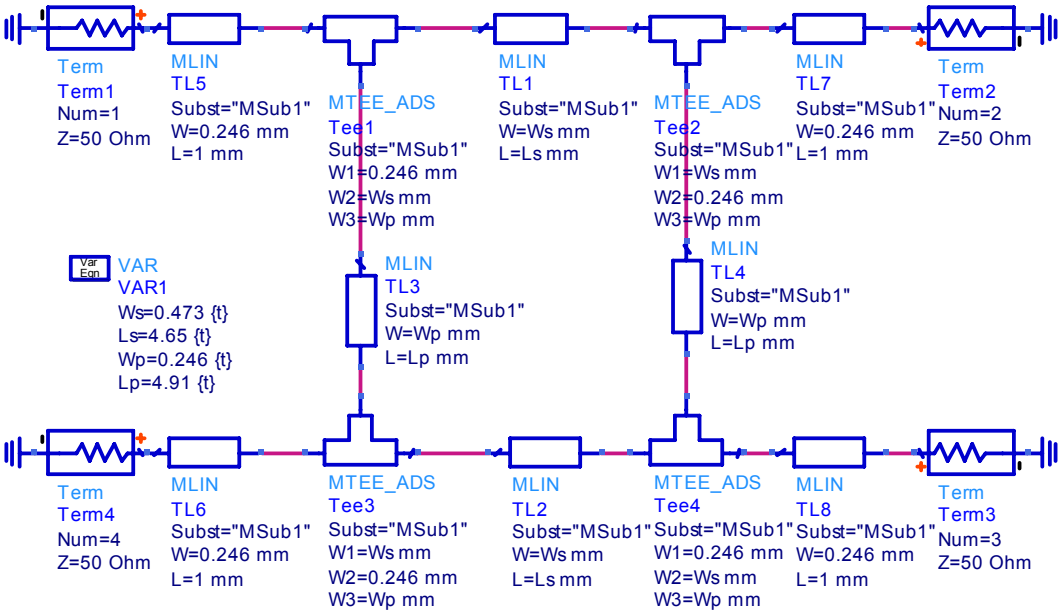
(b)



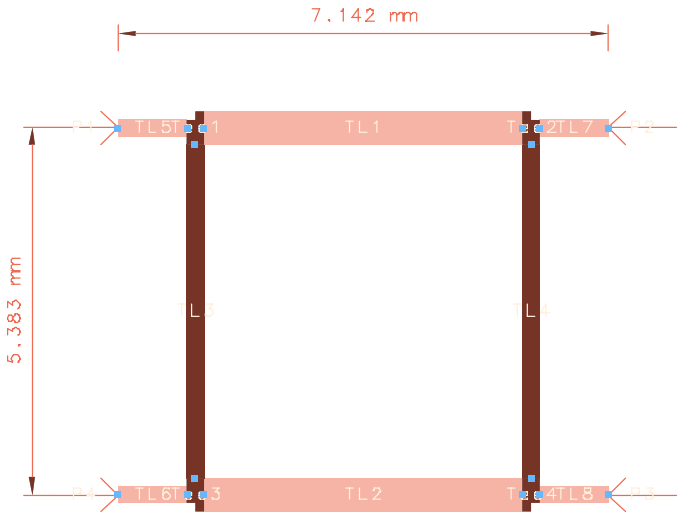
(c)

Figure 4-28: EM Simulation Results of 7 dB Coupler, (a) Input Return Loss, (b) Insertion Loss, (c) Coupling Ratio

After finalizing the design of 7 dB coupler, design and results of front-end structure will be given in remaining part. The FMCW transceiver transmitter and receiver antennas are dual-polarized in order to eliminate 6 dB total loss in front-end structure [7]. The receiver and transmitter paths are separated by 90°, 3 dB branch-line coupler. Detailed analyses of branch-line couplers are examined in chapter 3. Here, branch-line coupler design details on Alumina substrate for frequency band 5.5-6.5 GHz are given. The lengths of branches are quarter wave length where this length for Alumina (ε_r=9.6, h=0.25 mm) substrate is 4.91 mm. This length is taken as reference starting point for simulation. The optimum width and lengths of branches are determined in simulation and are given Figure 4-29 (a) and (b). The lengths are slightly changed due to the effect of T-junctions connecting series and parallel branches. The corresponding EM simulation results of single-stage branch-line coupler are presented in Figure 4-30. According to these results, coupling factor is 3.2 ± 0.2 dB in desired frequency band. Moreover, isolation from port 1 to 4, which also determines transmitter-receiver isolation, increases to -15 dB at the edges of frequency band. In other words, for 30 dBm transmitted power 15 dBm is leaked to receiver side. Therefore, in order to increase isolation a double stage branch-line coupler is preferred.

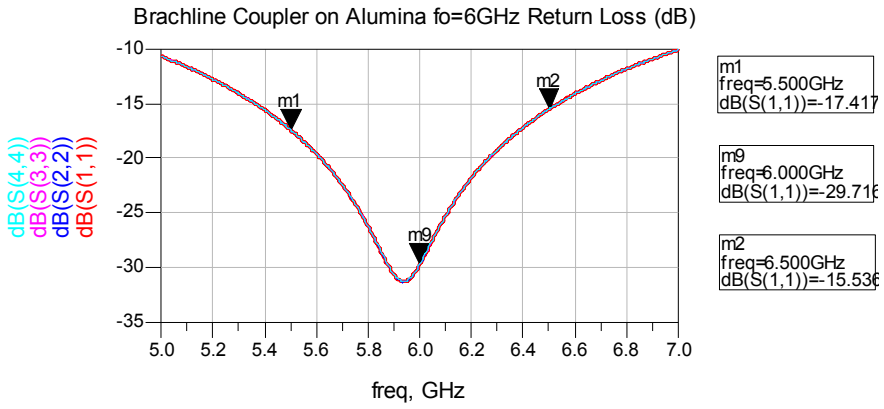


(a)

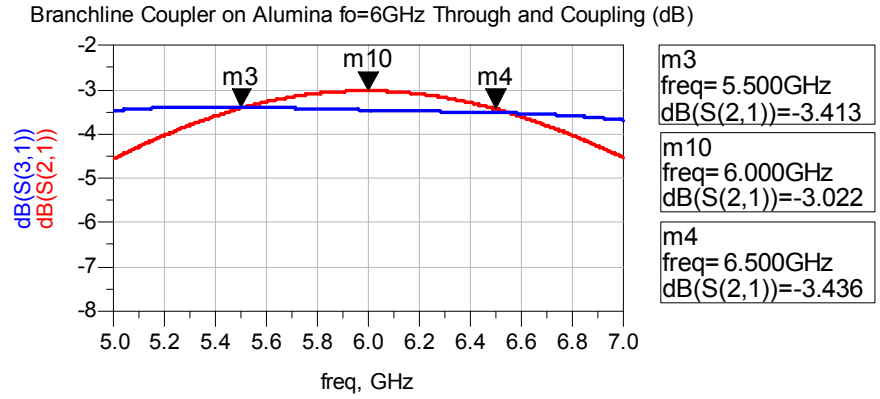


(b)

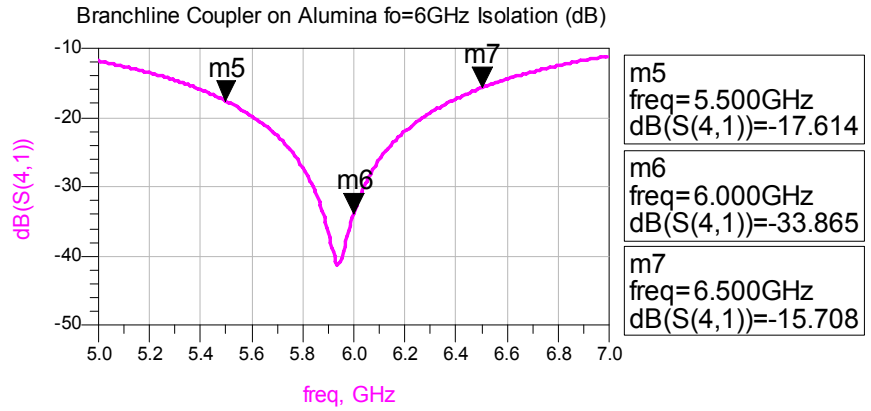
Figure 4-29: (a) Schematic, (b) Layout of Single-Stage Branch-Line Coupler on Alumina


Brachline Coupler on Alumina fo=6GHz Return Loss (dB)
dB(S(4,4))
dB(S(3,3))
dB(S(2,2))
dB(S(1,1))
-10
-15
-20
-25
-30
-35
5.0
5.2
5.4
5.6
5.8
6.0
6.2
6.4
6.6
6.8
7.0
freq, GHz
m1
m2
m9
m1
freq=5.500GHz
dB(S(1,1))=-17.417
m9
freq=6.000GHz
dB(S(1,1))=-29.71
m2
freq=6.500GHz
dB(S(1,1))=-15.53

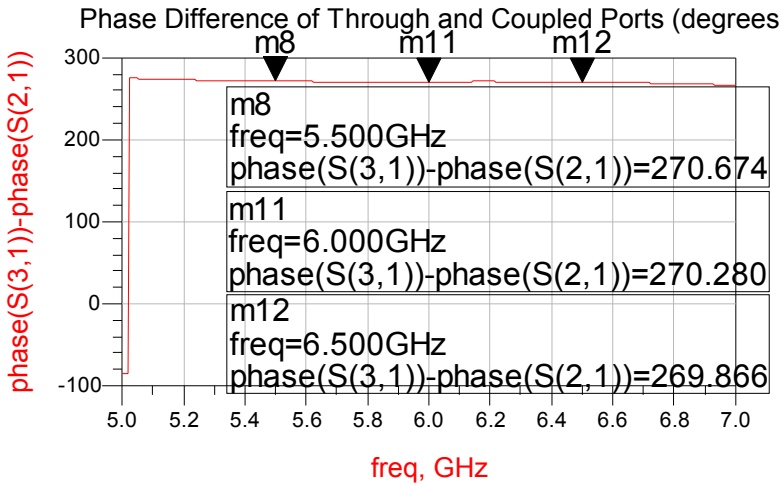
(a)


Branchline Coupler on Alumina fo=6GHz Through and Coupling (dB)
dB(S(3,1))
dB(S(2,1))
-2
-3
-4
-5
-6
-7
-8
5.0
5.2
5.4
5.6
5.8
6.0
6.2
6.4
6.6
6.8
7.0
freq, GHz
m3
m10
m4
m3
freq= 5.500GHz
dB(S(2,1))=-3.413
m10
freq= 6.000GHz
dB(S(2,1))=-3.022
m4
freq= 6.500GHz
dB(S(2,1))=-3.436

(b)


Branchline Coupler on Alumina fo=6GHz Isolation (dB)
dB(S(4,1))
-10
-20
-30
-40
-50
5.0
5.2
5.4
5.6
5.8
6.0
6.2
6.4
6.6
6.8
7.0
freq, GHz
m5
m7
m6
m5
freq=5.500GHz
dB(S(4,1))=-17.614
m6
freq=6.000GHz
dB(S(4,1))=-33.865
m7
freq=6.500GHz
dB(S(4,1))=-15.708

(c)



(d)

Figure 4-30: EM Simulation Results of Single Stage Branch-Line Coupler, (a) Port Return Loss, (b) Through and Coupling Ratio, (c) Isolation, (d) Phase Difference Between Direct and Coupled Ports

A double-stage branch-line coupler is composed of seven quarter wavelength parts as seen in Figure 4-31. Z_1, Z_2, Z_3 are the impedances of lines with widths W_s, W_p, W_{p2} respectively. For a reference impedance Z_0 system, Z_1, Z_2, Z_3 can be calculated by following equations [27]:

$$Z_2 = (1+\sqrt{2}) \cdot Z_0 \tag{4.5}$$

$$Z_3 = \sqrt{2} \cdot \frac{Z_1^{\,2}}{Z_0} \tag{4.6}$$

Since the reference impedance is taken as Z_0 = 50 Ω for FMCW transceiver system, Z_2 is found to be 120.8 Ω with a line width of 15 µm by using (4.5). This length is still achievable with HMIC technology. The series branch impedance Z_1 is chosen to be 50 Ω. Then, Z_3=70.7 Ω is calculated from (4.6). The realization of line widths corresponding to Z_1 and Z_3 is easy compared to Z_2.

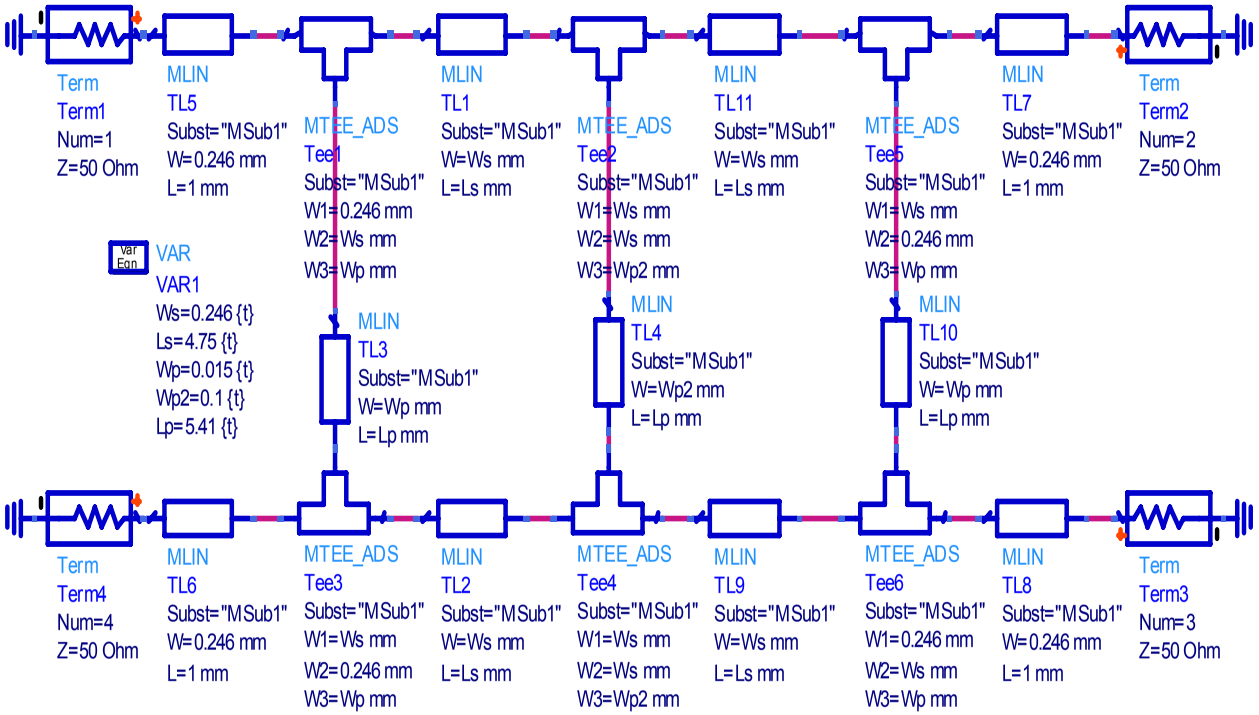
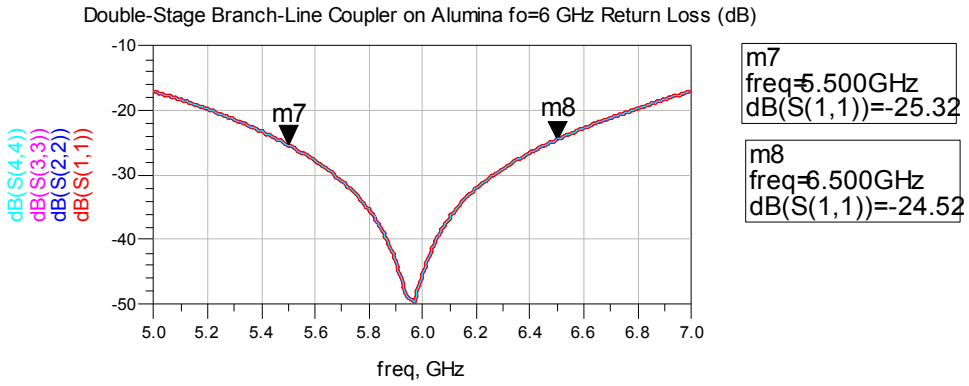
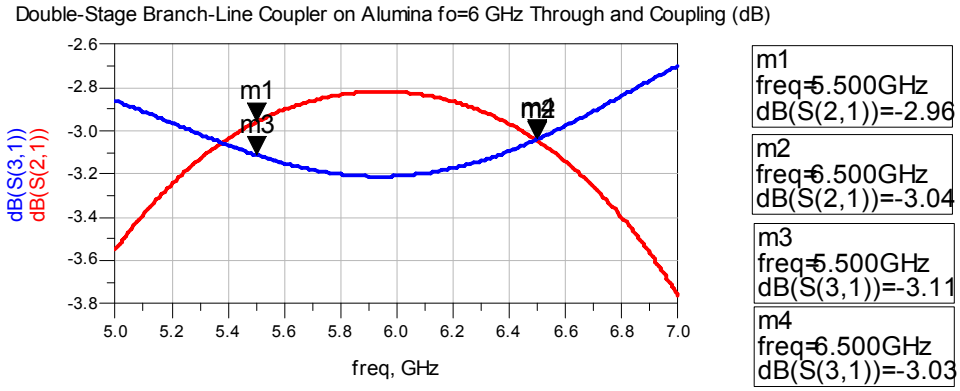


Figure 4-31: Schematic of Designed Double-Stage Branch-Line Coupler

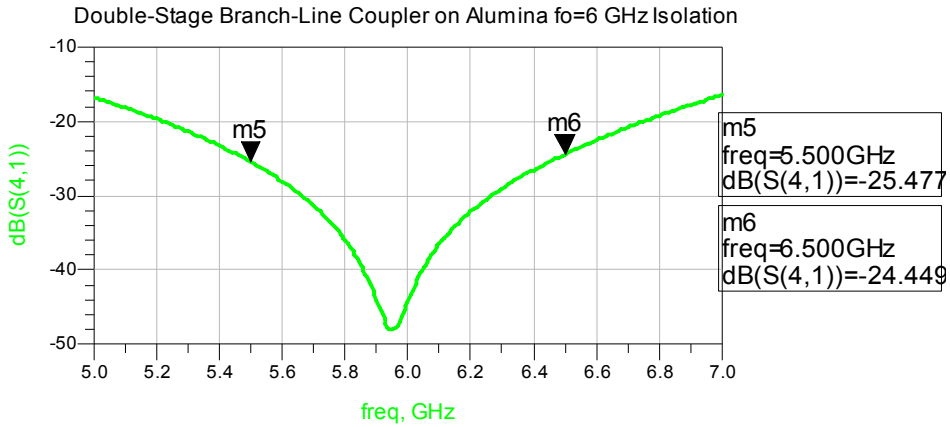
The layout of double-stage branch-line coupler is simulated. The results including return losses of ports, through and coupling ratio, isolation and phase difference between direct and coupled ports are presented in Figure 4-32. It is notable from graphs that an improvement of 10 dB is achieved in isolation. This improvement will directly decrease the leakage from transmitter to receiver.



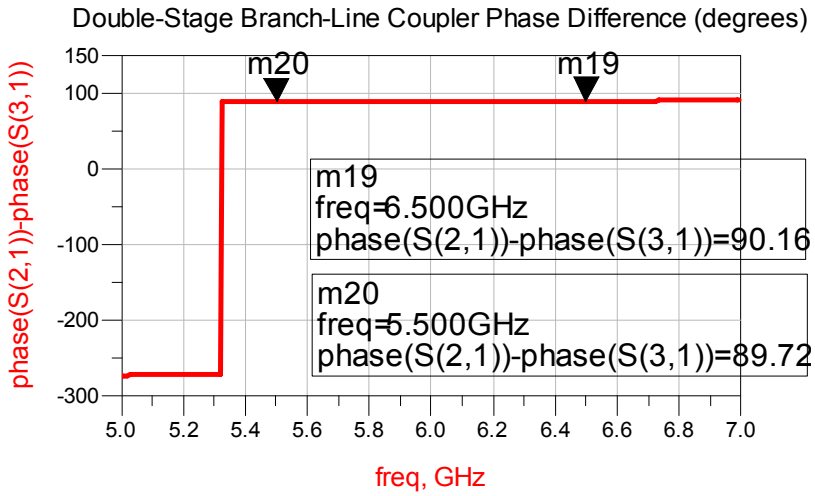
(a)



(b)



(c)



(d)

Figure 4-32: EM Simulation Results of Double Stage Branch-Line Coupler, (a) Port Return Loss, (b) Through and Coupling Ratio, (c) Isolation, (d) Phase Difference Between Direct and Coupled Ports

CHAPTER 5

CONCLUSIONS

In this thesis, some of miniaturization techniques of HMIC design are studied and an FMCW range sensor transceiver design with chip transistors is presented. Firstly, frequently used microwave integrated circuit techniques (MIC) HMIC and MMIC are introduced. Their definitions, materials used are given and fabrication techniques both types are discussed. Application areas and circuit performance comparison are done. Moreover, advantages and disadvantages of both techniques are summarized. Small size and broadband performance are important superiority of MMIC technique over HMIC. On the other hand, lower cost and tunability properties of HMIC make it more favorable. This thesis is mainly devoted on improving the large size property of HMIC technique.

In order to be ready for FMCW transceiver design, FMCW radar theory is examined in chapter 2. Important features and principles of operation are discussed. With FMCW radar, range measurement can be done in addition to velocity measurement. Derivation of formulas for both range and Doppler velocity measurement are given in detail. FMCW waveform and its basic parameters are explained. In addition, a brief history and usage areas including civil and military applications are summarized.

Chapter 3, which is mainly devoted on miniaturization techniques of HMICs, forms the core of this thesis. In the first part, miniaturization of hybrid couplers

is examined. Couplers are critical component of microwave circuits. They are commonly used in power level monitoring of a transmitter, VSWR protection, balanced amplifiers as 3 dB, 90° hybrid divider and combiner. Branchline coupler is the one of the techniques of designing hybrid 3 dB couplers. However, for low frequencies, large dimension of quarter wavelength sections become problem for the designer, requiring compact size solutions. To solve this problem, two techniques, which are tried in literature, are introduced with their analytical background. These techniques are implemented using dual transmission line and shunt connected capacitors. Using these techniques a size reduction up to 80% is achieved without any degrade of electrical performance. Another miniature hybrid coupler technique is achieved by slot coupling. The frequency band performance of this type is wider than a branchline coupler. The simulation and measurement results for 3-10 GHz frequency band are presented. As a future work this structure can be tried for power unequal divider by optimizing the slot shape and using matching sections.

Another miniaturization technique applied on stubs is proposed which is not present in literature. The analytical formulation is derived by dividing an open-circuited quarter wavelength transmission line. It is observed from simulation results that by cascading two transmission lines with high enough and low enough characteristic impedance, %50 size reduction can be achieved for quarter wavelength stubs. As a further study this concept is tried to apply on radial stubs. To do so, a radial defect is opened in radial stub. In simulation media, radial stub with 40°, 50°, 60° angle is simulated. As a result, optimum defect lengths for different angles are determined. It is observed that by applying these defects on radial stub, short-point resonant frequency is decreased for constant length. However, broad band performance is degraded. A radial stub with 50° angle for 1 GHz center frequency is realized for different feedline widths. Measurement results show that smaller feedline widths results in lower resonant frequency.

Planar interdigital capacitors (IDC) and spiral inductors (SI) can be considered as techniques of size reduction for standard packaged capacitors and inductors. Besides, parasitic effects, which are series problem of packaged components, are significantly decreased. Equivalent circuit elements are introduced. Element values are determined by comparing EM simulation results with equivalent circuit.

Fractal technique is another way of miniaturization discussed in chapter 3. Its theory relies on fragmented geometric shape that is split into parts, each of which is reduced size copy of the whole. This technique is applied on planar antennas, filter, matching networks in literature. In this study, fractal Sierpinski square approach is applied on multistage microstrip matching network for two and three stages. The EM simulation results show that bandwidth improvement is achieved by fractal technique.

In chapter 4, a compact 1 W FMCW transceiver design simulation details are given. In this design, chip transistors are used. The input and output matching sections are designed using planar IDC and SI connected by wire bonds. A two stage power amplifier with a gain of approximately 24 dB for frequency band of 5.5-6.5 GHz is designed. Matching sections are mainly composed of L-C type low-pass filters. For stability considerations, drain to gate resistor is needed. Another sub-part low noise amplifier design is achieved with similar approach. However, in this case noise match is the main concern. The final part front end is composed of two stage branchline coupler. This front-end solution can be used with dual polarized antenna system.

As a future work, the designed and simulated FMCW range sensor transceiver can be implemented and measured. The measurement results are compared with simulation results. If there are mismatches, the reasons behind this can be investigated.

REFERENCES

[1] Bahl I., Bhartia P., “Microwave Solid State Circuit Design” 2nd Ed., pp. 851-857, New York, Wiley, 2003.

[2] Robertson I. D., Lucyszyn S., “RFIC and MMIC Design and Technology”, London, The Institution of Electrical Engineers, 2001.

[3] Pozar David M., “Microwave Engineering”, 3rd Ed., New York, Wiley, 2005.

[4] Bahl I., “Lumped Elements for RF and Microwave Circuits”, Boston, Artech House, 2003.

[5] Colin Robert E., “Foundations for Microwave Engineering”, 2nd Ed., pp. 713-716, New York, Wiley, 2000.

[6] Komarov I. V., Smolskiy S. M., “Fundamentals of Short Range FM Radar”, Artech House, 2003.

[7] Secmen M., S. Demir S., Hızal A..: “Dual-polarized T/R Antenna System Suitable for FMCW Altimeter Radar Applications”, IEEE Proc.-Microwave Antennas Propag., Vol153, No. 5, October 2006, pp. 407-412

[8] Bentley, J. O., “Airplane Altitude Indicating System,” U. S. Patent No. 2,011,392, issued August 13, 1935, application August 10, 1928.

[9] Tang C. W., Chen M. G., Tsai C. H., “Miniaturization of Microstrip Branch-Line Coupler with Dual Transmission Lines”, IEEE Microwave and Wireless

Components Letters, Vol.18, No.3, March 2008.

[10] Mongia R., Bahl I., Bhartia P., “RF and Microwave Coupled Line Circuits”, Artech House, 1999.

[11] Gu Q., Yang Y., Tassoudji M., “Modeling and Analysis of Vias in Multilayered Integrated Circuits”, IEEE Trans. Microwave Theory Tech., 1993, 41, (2), pp. 206–214.

[12] Zhu, L., Wu, K., “Ultra Broadband Vertical Transition for Multilayer Integrated Circuits’, IEEE Microwave Guided Wave Letters, 1999, 9, (11), pp. 453–455.

[13] Li, E., “Broadband Vertical Transition at Millimeter-Wave Frequencies Using Microstrip-Fed Cavity Couplers”, IEEE Antennas Propag. Symp., 2004, vol. 4, pp. 3745–3748.

[14] Chen C., Tsai M., Alexopoulos G., “Optimization of Aperture Transitions for Multiport–Microstrip Circuits”, IEEE Trans. Microwave Theory Tech., 1996, 44, (12), pp. 2457–2465.

[15] Abbosh A.M., “Ultra Wideband Vertical Microstrip-Microstrip Transition”, IET Microwave Antennas Propag., 2007, 1, (5), pp.968-972.

[16] Abbosh A.M., Bialkowski M.E., “Design of Compact Directional Couplers for UWB Applications”, IEEE Trans. Microwave Theory Tech., 2007, vol.55, no.2.

[17] Abbosh A.M., “Planar Band-pass Filters for Ultra-wideband Applications”, IEEE Trans. Microwave Theory Tech, 2007, vol.55, no.10.

[18] Alley G. D., ‘‘Interdigital Capacitors and Their Application in Lumped

Element Microwave Integrated Circuits,'' IEEE Trans. Microwave Theory Tech., Vol. MTT-18, December 1970, pp. 1028–1033.

[19] Hobdell, J. L., ''Optimization of Interdigital Capacitors,'' IEEE Trans. Microwave Theory Tech., Vol. MTT-27, September 1979, pp. 788–791.

[20] Esfandiari R., Maki D. W., Sircusa M., ''Design of Interdigitated Capacitors and Their Application to GaAs Filters,'' IEEE Trans. Microwave Theory Tech., Vol. MTT-31, January 1983, pp. 57–64.

[21] "Fractal miniaturization in RF and microwave networks", 2001, from http://www.fractal.org/Fractal-Research-and-Products/Fractal-waves.pdf, last accessed date: 25/05/2009.

[22] Kim I1 K., Kingsley N., Morton A. M., Pinel S., Papapolymerou J., Tentzeris M. M., Laskar J., Yook J. G., "Koch Fractal Shape Microstrip Bandpass Filters on High Resistivity Silicon for Suppression of the 2nd Harmonic", Journal of the Korea Electromagnetic Engineering Society, Vol. 6, No. 4, December 2006.

[23] Patnam R. H., "Broad band CPW-Fed Planar Koch Fractal Loop Antenna", IEEE Antenna and Wireless Propag. Letters, Vol. 7, 2008.

[24] "Fractal Dimension", Updated April 5, 2010, from http://en.wikipedis.org/wiki/Fractal_dimension, last accessed date: 20/04/2010.

[25] Chen W. L., Wang G. M., Qi Y. N., Liang J. G., "Fractal-Shaped Stepped-Impedance Transformers for Wideband Application", Microwave and Optical Technology Letters, Vol. 49, No. 7, July 2007.

[26] Leenaerts D., van der Tang J., Vaucher C., "Circuit Design For RF

Transceivers", Kluwer Academic Publishers, pp. 79-111.

[27] "Double-Box Brachlines", Updated April 28, 2006, from http://www.microwaves101.com/encyclopedia/Branchline-couplers.cfm, last accessed date: 12/01/2010.

[28] Korkmaz H., Demir Ş., Şen B., "Minyatür Bağlaç ve Güç Bölücü Yapıları", Ursi-Akdeniz Üniv., Ekim 2008.

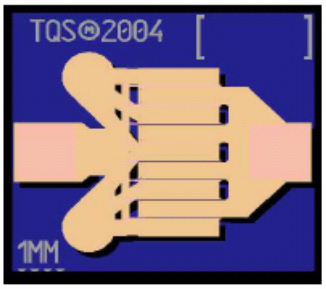
APPENDIX A

DATASHEET OF TRIQUINT TGF2021-01 DISCRETE POWER pHEMT

TriQuint SEMICONDUCTOR

Product Datasheet
August 7, 2007

DC - 12 GHz Discrete power pHEMT — TGF2021-01



Key Features and Performance

- Frequency Range: DC - 12 GHz
- > 30 dBm Nominal Psat
- 59% Maximum PAE
- 11 dB Nominal Power Gain
- Suitable for high reliability applications
- 1mm x 0.35µm Power pHEMT
- Nominal Bias Vd = 8-12V, Idq = 75-125mA (Under RF Drive, Id rises from 75mA to 240mA)
- Chip Dimensions: 0.57 x 0.53 x 0.10 mm (0.022 x 0.021 x 0.004 in)

Product Description

The TriQuint TGF2021-01 is a discrete 1 mm pHEMT which operates from DC-12 GHz. The TGF2021-01 is designed using TriQuint's proven standard 0.35um power pHEMT production process.

The TGF2021-01 typically provides > 30 dBm of saturated output power with power gain of 11 dB. The maximum power added efficiency is 59% which makes the TGF2021-01 appropriate for high efficiency applications.

The TGF2021-01 is also ideally suited for Point-to-point Radio, High-reliability space, and Military applications.

The TGF2021-01 has a protective surface passivation layer providing environmental robustness.

Lead-free and RoHS compliant

Primary Applications

- Point-to-point Radio
- High-reliability space
- Military
- Base Stations
- Broadband Wireless Applications

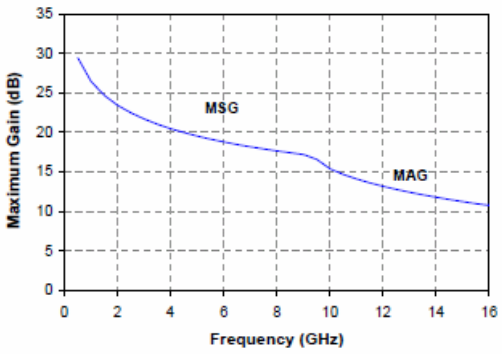


TABLE I
MAXIMUM RATINGS

Symbol	Parameter 1/	Value	Notes
V^+	Positive Supply Voltage	12.5 V	2/
V^-	Negative Supply Voltage Range	-5V to 0V	
I^+	Positive Supply Current	470 mA	2/
$\lvert I_G \rvert$	Gate Supply Current	7 mA	
P_{IN}	Input Continuous Wave Power	25 dBm	2/
P_D	Power Dissipation	See note 3	2/ 3/
T_{CH}	Operating Channel Temperature	150 °C	4/
T_M	Mounting Temperature (30 Seconds)	320 °C	
T_{STG}	Storage Temperature	-65 to 150 °C	

1/ These ratings represent the maximum operable values for this device.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

3/ For a median life time of 1E+6 hrs, Power dissipation is limited to:
$P_D(max) = (150\ °C - TBASE\ °C) / 86.5\ (°C/W)$

4/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

TABLE II
DC PROBE CHARACTERISTICS
(T_A = 25 °C, Nominal)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Idss	Saturated Drain Current	-	300	-	mA
Gm	Transconductance	-	375	-	mS
V_P	Pinch-off Voltage	-1.35	-1	-0.65	V
V_{BGS}	Breakdown Voltage Gate-Source	-30	-	-8	V
V_{BGD}	Breakdown Voltage Gate-Drain	-30	-	-15	V

Note: For TriQuint's 0.35um power pHEMT devices, RF breakdown >> DC breakdown

TABLE III
RF CHARACTERIZATION TABLE 1/
(T_A = 25 °C, Nominal)

SYMBOL	PARAMETER	Vd = 10V Idq = 75mA	Vd = 12V Idq = 75mA	UNITS
Power Tuned:				
Psat	Saturated Output Power	30.8	31.5	dBm
PAE	Power Added Efficiency	50	48	%
Gain	Power Gain	11	11	dB
Γ_L 2/	Load Reflection coefficient	0.541 ∠ 147.9	0.546 ∠ 140.6	-
Efficiency Tuned:				
Psat	Saturated Output Power	30	30.7	dBm
PAE	Power Added Efficiency	59	55	%
Gain	Power Gain	11.5	11	dB
Γ_L 2/	Load Reflection coefficient	0.643 ∠ 130.3	0.640 ∠ 125.9	-

1/ Values in this table are taken from a 1mm unit pHEMT cell at 10 GHz

2/ Optimum load impedance for maximum power or maximum PAE at 10 GHz.

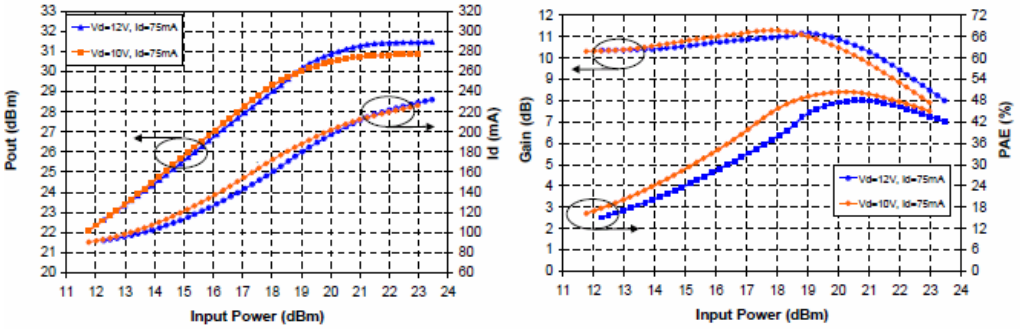
TABLE IV
THERMAL INFORMATION

Parameter	Test Conditions	T_{CH} (°C)	θ_{JC} (°C/W)	T_M (HRS)
θ_{JC} Thermal Resistance (channel to backside of carrier)	Vd = 12 V Idq = 75 mA Pdiss = 0.9 W	148	86.5	1.2 E+6

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature.

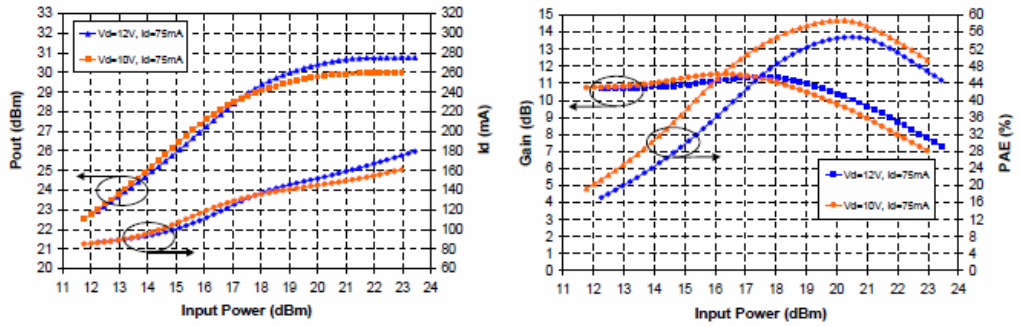
Measured Fixtured Data

Power tuned data at 10GHz



For power tuned devices at 10GHz
Input matched for maximum gain & output load is:
Vd=12V, Idq=75mA: Γ_L= 0.546, θ = 141°
Vd=10V, Idq=75mA: Γ_L = 0.541, θ = 148°

Efficiency tuned data at 10GHz



For efficiency tuned devices at 10GHz:
Input matched for maximum gain & output load is:
Vd=12V, Idq=75mA: Γ_L = 0.640, θ = 126°
Vd=10V, Idq=75mA: Γ_L = 0.643, θ = 130°

APPENDIX B

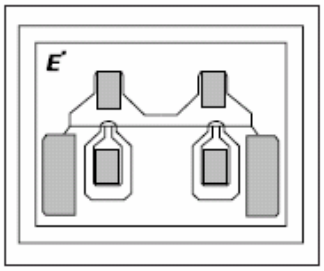
DATASHEET OF EUDYNA FHX13X GAAS FET

FHX13X, FHX14X

GaAs FET & HEMT Chips

FEATURES

- Low Noise Figure: 0.45dB (Typ.)@f=12GHz (FHX13)
- High Associated Gain: 13.0dB (Typ.)@f=12GHz
- Lg ≤ 0.15μm, Wg = 200μm
- Gold Gate Metallization for High Reliability



DESCRIPTION

The FHX13X, FHX14X are Super High Electron Mobility Transistor (SuperHEMT™) intended for general purpose, ultra-low noise and high gain amplifiers in the 2-18GHz frequency range. The devices are well suited for telecommunication, DBS, TVRO, VSAT or other low noise applications.

Eudyna stringent Quality Assurance Program assures the highest reliability and consistent performance.

ABSOLUTE MAXIMUM RATING (Ambient Temperature Ta=25°C)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	3.5	V
Gate-Source Voltage	V_{GS}	-3.0	V
Total Power Dissipation	P_t*	180	mW
Storage Temperature	T_{stg}	-65 to +175	°C
Channel Temperature	T_{ch}	175	°C

*Note: Mounted on Al_2O_3 board (30 x 30 x 0.65mm)

Eudyna recommends the following conditions for the reliable operation of GaAs FETs:

1. The drain-source operating voltage (V_{DS}) should not exceed 2 volts.
2. The forward and reverse gate currents should not exceed 0.2 and -0.05mA respectively with gate resistance of 4000Ω.
3. The operating channel temperature (T_{ch}) should not exceed 80°C.

ELECTRICAL CHARACTERISTICS (Ambient Temperature Ta=25°C)

Item		Symbol	Test Conditions	Limit Min.	Limit Typ.	Limit Max.	Unit
Saturated Drain Current		I_{DSS}	V_{DS} = 2V, V_{GS} = 0V	10	30	60	mA
Transconductance		gm	V_{DS} = 2V, I_{DS} = 10mA	35	50	-	mS
Pinch-off Voltage		V_p	V_{DS} = 2V, I_{DS} = 1mA	-0.1	-0.7	-1.5	V
Gate Source Breakdown Voltage		V_{GSO}	I_{GS} = -10μA	-3.0	-	-	V
Noise Figure	FHX13X	NF	V_{DS} = 2V I_{DS} = 10mA f = 12GHz	-	0.45	0.50	dB
Associated Gain	FHX13X	G_{as}		11.0	13.0	-	dB
Noise Figure	FHX14X	NF		-	0.55	0.60	dB
Associated Gain	FHX14X	G_{as}		11.0	13.0	-	dB
Thermal Resistance		R_{th}	Channel to Case	-	220	300	°C/W

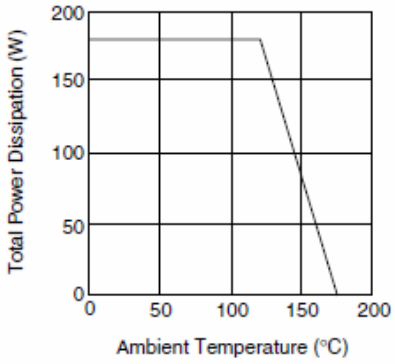
Note: RF parameter sample size 10pcs. criteria (accept/reject)=(2/3)

The chip must be enclosed in a hermetically sealed environment for optimum performance and reliability.

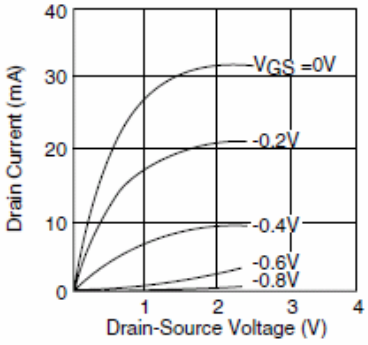
FHX13X, FHX14X

GaAs FET & HEMT Chips

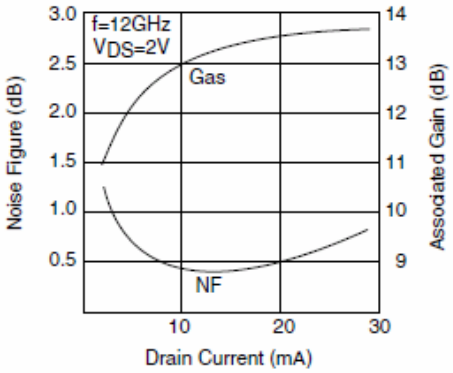
POWER DERATING CURVE



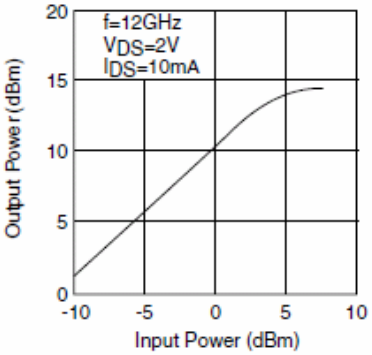
DRAIN CURRENT vs. DRAIN-SOURCE VOLTAGE



NF & Gas vs. I_{DS}



OUTPUT POWER vs. INPUT POWER



NOISE PARAMETERS

V_{DS}=2V, I_{DS}=10mA

Freq. (GHz)	Γopt (MAG)	Γopt (ANG)	NFmin (dB)	Rn/50
2	0.92	13	0.28	0.65
4	0.84	25	0.30	0.54
6	0.77	38	0.32	0.41
8	0.71	51	0.34	0.31
10	0.66	65	0.39	0.23
12	0.61	79	0.45	0.17
14	0.58	93	0.56	0.12
16	0.56	108	0.68	0.09
18	0.54	122	0.86	0.07
20	0.52	136	1.03	0.07
22	0.50	150	1.22	0.07
24	0.46	162	1.43	0.07

Ga (max) & $|S_{21}|^2$ vs. FREQUENCY