A CURRENT SOURCE CONVERTER BASED STATCOM FOR REACTIVE POWER COMPENSATION AT LOW VOLTAGE

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Approval of the thesis:

A CURRENT SOURCE CONVERTER BASED STATCOM FOR REACTIVE POWER COMPENSATION AT LOW VOLTAGE

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ABSTRACT

A CURRENT SOURCE CONVERTER BASED STATCOM FOR REACTIVE POWER COMPENSATION AT LOW VOLTAGE

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This research work is devoted to the analysis, design and development of the Current-Source Converter (CSC) based distribution-type Static Synchronous Compensator (D-STATCOM) for low-voltage applications in reactive-power control in order to achieve i) faster transient response in reactive-power control, ii) lower current harmonic distortion, iii) lower power losses and iv) minimum storage elements in comparison with conventional solutions. The developed CSC-D-STATCOM includes a low-pass input filter and a three phase forced-commutated CSC which is composed of six insulated gate bipolar transistors (IGBT) with built-in series diodes. The analysis and the control of the CSC-D-STATCOM are carried out in dq-synchronous reference frame in order to obtain the reference current waveform which is to be generated by switching the IGBTs at 3kHz with the use of space vector modulation.

Keywords: Reactive Power Compensation, Current Source Converter, STATCOM, pulse-width modulation

ÖZ

DÜŞÜK GERİLİMDE REAKTİF GÜÇ KOMPANZASYONU İÇİN AKIM KAYNAKLI ÇEVİRGECE DAYALI STATKOM

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Mayıs 2010, 105 sayfa

Bu çalışma, düşük gerilim seviyesinde yapılan reaktif güç kontrolü uygulamalarında geleneksel çözümlere oranla i) daha hızlı geçici tepki elde edilmesi ii) akım harmonikleri bozulumunun azaltılması iii) güç kayıplarının düşürülmesi ve iv) depolama elemanlarının küçültülmesinin başarılabilmesi için Akım Kaynaklı Çevirgece (AKÇ) dayalı dağıtım tipi Statik Senkron Kompanzatörünün (D-STATKOM) analizi, tasarımı ve geliştirilmesine hasredilmektedir.

Geliştirilen AKÇ-D-STATKOM, düşük geçirgen giriş filtresi ve altı adet seri diyotlu IGBT'den müteşekkil üç fazlı cebri anahtarlamalı AKÇ' den oluşmaktadır. Uzay vektörü darbe genliği kiplenimi metodu kullanılarak IGBT' lerin 3kHz frekansında anahtarlanmasıyla üretilecek olan referans akım dalga şeklinin elde edilebilmesi için AKÇ-D-STATCOM' un analizi ve kontrolü dq-senkron referans düzleminde gerçekleştirilmiştir.

Anahtar Kelimeler: Reaktif Güç Kompanzasyonu, Akım Kaynaklı Çevirgeç, STATKOM, Uzay vektörü darbe genliği kiplenimi.

To My Family

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INTRODUCTION

1.1 Reactive Power Compensation

The reactive power is defined as the ac component of the instantaneous power, with a frequency equal to 100 Hz in a 50-Hz system. As illustrated in Figure 1.1 the reactive power generated by the ac power source is stored in a capacitor or a reactor during a quarter of a cycle, and in the next quarter cycle is sent back to the power source. In other words, the reactive power oscillates between the ac source and the capacitor or reactor, and also between them, at a frequency equals to two times the rated value (50 Hz), [1]. In order to carry this oscillating power by transmission systems rated value of the installed devices should be higher, this increases the cost of transmission systems and power losses, and also the power system stability is affected by reactive power.

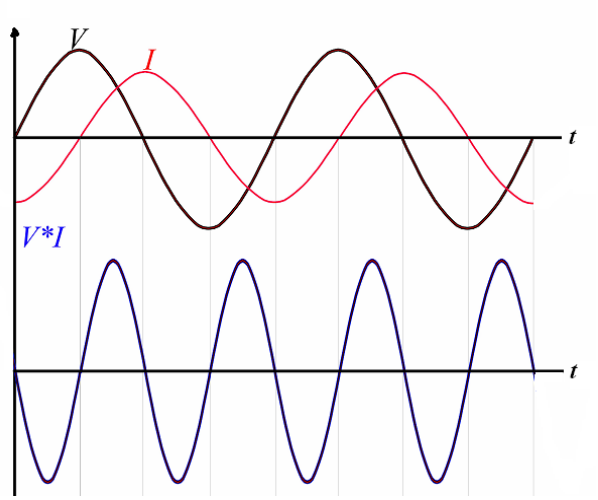


Figure 1.1 Instantaneous Power (Inductive Load)

In order to avoid this problem, the reactive power should be compansated using volt-ampere-reactive (VAR) generators. VAR generators can be connected in parallel or in series.

- ***Shunt Compensation:***

Figure 1.2 (b) shows the principles and theoretical effects of shunt reactive power compensation in a basic ac system with an inductive load. V_1 is the source voltage and V_2 is the load voltage. I_P represents active component of the line current and I_Q reactive component of the load. I_Q increases the magnitude of the total line current $I\angle\varphi$ which is supplied by the source. If reactive power is compansated near the load by injecting the reactive current -I_Q, the magnitude of the line current can be reduced to its active component. Hence, the power losses can be reduced and the voltage regulation can be improved at the load terminals. This can be done by one of three ways; 1) using capacitor for inductive load and reactor for capacitive load , 2) using a voltage source, 3) using a current source. The illustrated example shows a current source type compensator. The main advantage of using a voltage or current source VAR generators (instead of inductors or capacitors) is the reactive power generated is independent of the voltage at the point of connection.

- ***Series Compensation:***

As can be seen Figure 1.2 (c) in series compensation V_{COMP} has been added between the line and the load to change the angle of V_2 in order to make the angle between line current I_P and V_2 zero. Like shunt compensation, series compensation may also be implemented with current- or voltage-source devices. Typical series compensation systems use capacitors to decrease the equivalent reactance of a power line at rated frequency in order to increase angular stability

of the power line, improve voltage stability and optimize power sharing between parallel circuits.

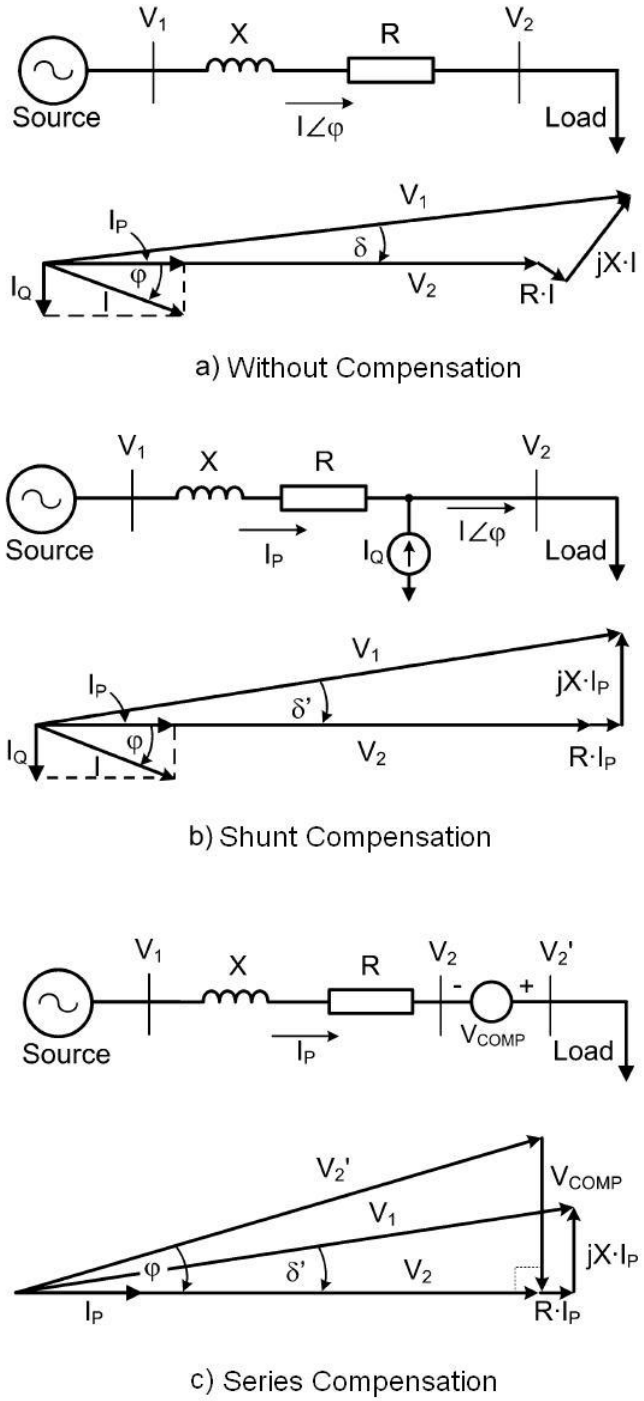


Figure 1.2 Phasor Diagrams for Different VAR Compensation Approach

1.2 Compensation Systems

Compensation systems are classified depending on the way of connection to the power line (shunt or series) and depending on the technology used in their implementation. Mechanically switched capacitors and synchronous machines were the only reactive power compensators before the invention of power electronic devices. With the developments in power semiconductor technology , different static VAR generators have been developed. A brief explanation of various compensation ststems is as follows.

- ***Mechanically Switched Capacitors:***

  Shunt capacitors were first employed for reactive power compensation in the first decades of the 20th century. Depending on the total VAR requirement capacitors are switched in or switched out by using mechanical switches such as contactors or circuit breakers. Reactive power generated by mechanically switched capacitors is illustrated in Figure 1.3.

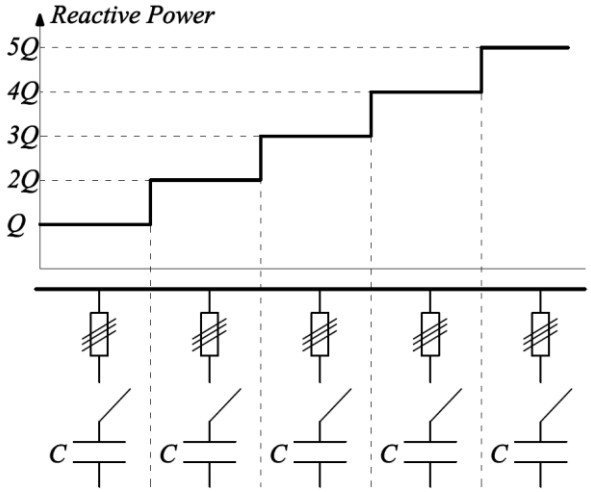


Figure 1.3 Reactive Power Generation by Mechanically Switched Capacitors

Since the reactive power is generated in discrete steps, load may be instantaneously over-compensated or under-compensated. Also the response of the system is very slow due to delay in mechanical switches and discharge time of the capacitors. Moreover, high in-rush current during switch in and frequent maintenance of the mechanical switchgear are other concerns of this system. This type of compensation is commonly used in low voltage applications because of its low cost and simple installation. On the other hand, a satisfactory compensation for slowly changing inductive loads can be achieved by using sufficient number of capacitors.

- ***Synchronous Condensers:***

Synchronous machines can be used as reactive VAR generators by adjusting its field current in order to generate or absorb reactive power. The continuous control of reactive power is achieved by using automatic exciter circuit. Synchronous condensers connected to transmission systems are used commonly for 50 years in order to improve stability of the power system and keep voltages within limits under varying load conditions and contingency situations. Disadvantages of these systems are 1) slow response for rapidly changing loads, 2) significant amount of starting and protective equipment, 3) contribution to the short circuit current, 4) high maintenance and 5) much higher losses as compared with the other compensation systems.

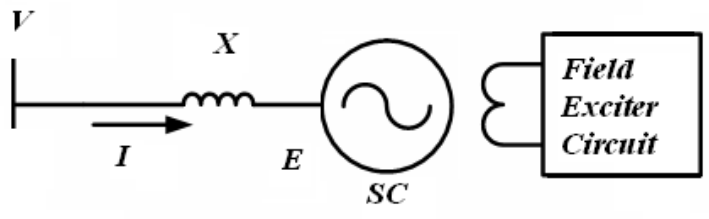


Figure 1.4 Synchronous Condenser

- ***Thyristor Switched Capacitor (TSC):***

As shown in Figure 1.5 capacitors are connected to system with back-to-back connected thyristor pairs. The use of thyristor as a switching element presents a transient free switching-in of capacitors without inrush current. It also eliminates the requirement for the discharge of capacitors. This is supplied by switching-on and switching-off thyristors at the instances when *dv/dt* rating on capacitor is zero. L may be connected not only limiting the fault current but also designing a tuned harmonic filter.

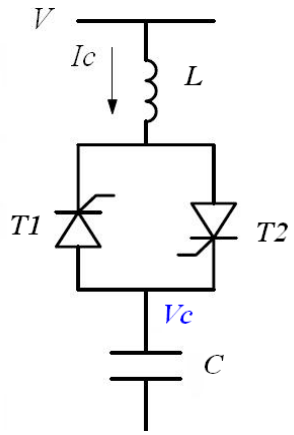


Figure 1.5 Thristor Switched Capacitor

The disadvantages of TSC are stepwise control of reactive power demand of the load, like mechanically switched capacitor and selection of the peak voltage rating of the thyristor with two times the peak value of supply voltage.

Thyristor Controlled Reactor (TCR):

Stepless, smooth control of reactive power can be achieved by means of firing angle (α). However, TCR injects current harmonics as the firing angle is changed and these harmonic currents should be filtered by using appropriated harmonic filters with TCR. Therefore, TCR systems are generally implemented with harmonic filters which provide capacitive reactive power. The net reactive power of complete system is then equal to the difference between the capacitive reactive power of the harmonic filter and the inductive reactive power of TCR. These harmonic filters can be arranged as thyristor switched filters in order to adjust the reactive power control range of the system adaptively without excessive losses in TCR (see Figure 1.6). The adjustment of α can be made instantaneously; which provides compensation of reactive power demand of rapidly changing loads. The disadvantages of TCR are mainly the generation of low order harmonic currents, hence large harmonic filters, large system footprint and higher reactor losses.

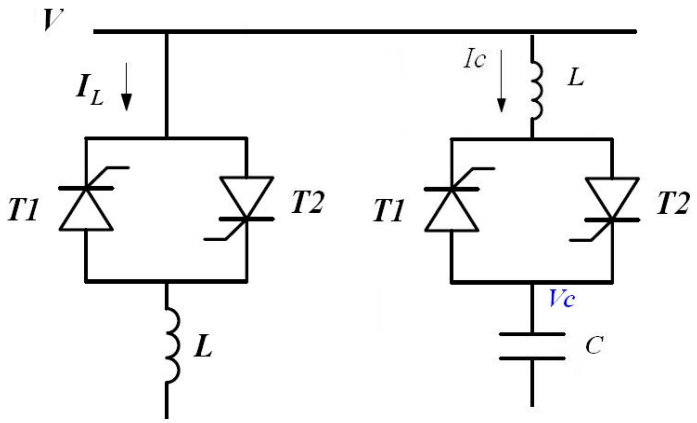


Figure 1.6 TCR with TSC

1.3 STATCOM (Static Synchronous Compensator)

With developments in semiconductor technology, the switching power converters where self commutated power semiconductors are switched at high voltage, high current and high frequency have become widely applicable in high power applications. This presents the use of switching converters which generate controlled inductive or capacitive currents independent of the ac system voltage with minimum energy storage elements such as capacitors or reactors. The shunt connected of these switching power converters are termed as STATCOM.

The switching power converters may be either voltage source type (VSC) (see Figure 1.7) or a current source type (CSC) (see Figure 1.8). In VSC based STATCOM, the converter produces a set of controllable three-phase output voltage (V_1, V_2 and V_3) at supply frequency from a dc-voltage provided by dc-link capacitor. Each output voltage is in phase with and coupled to the corresponding phase of ac system via coupling reactor (including reactance of the coupling transformer) so that required reactive current can be injected into the power system. On the other hand, CSC produces a set of controllable three-phase output current (I_1, I_2 and I_3) at supply frequency from a dc-current provided by the dc-link reactor. The switching frequency harmonics of these output currents are filtered by the input filter and then injected directly into the power system.

Commercially available STATCOM systems are mainly based on voltage source converter and there has been excessive research on VSC based STATCOM because of the following reasons.

i) The semiconductors used in current source converters should have bidirectional voltage blocking capability, but available high power semiconductors with gate turn-off capability (GTOs, IGBTs) cannot block reverse voltage. Reverse

voltage blocking diodes should be used in series with semiconductor switches which is increasing conduction losses.

ii) Current source converter dc-link reactor losses are higher compared to voltage source converter dc-link capacitor losses.

iii) VSC requires series reactors connected to ac side of the converter in order to filter voltage harmonics and this may be naturally provided by the leakage inductance of the coupling transformer. CSC requires capacitors on ac terminals in order to filter current harmonics.

Inspite of these facts, CSC based STATCOM is still promising attractive features such as, a) it does not need precharching of dc-link and it does not require inrush current limiting equipment, b) better ac current waveforms can be obtained by current source converter at relatively lower switching frequency, c) it does not inject harmonics in 'idle' state.

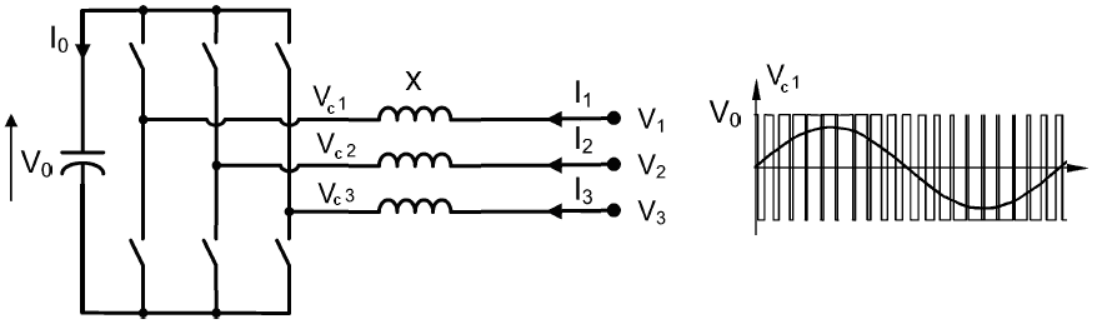


Figure 1.7 Voltage Source Converter (VSC) Based STATCOM

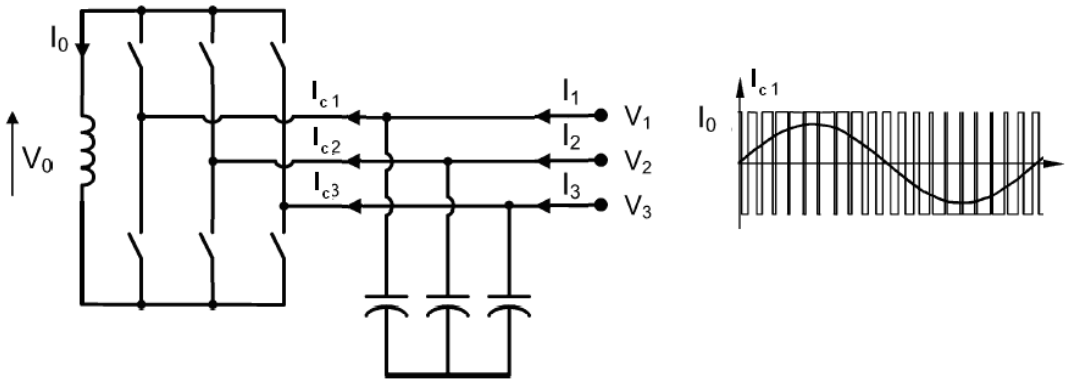


Figure 1.8 Current Source Converter (VSC) Based STATCOM

1.4 Literature Survey on Current Source Converter

As compared with VSC STATCOM, there are limited researches on CSC STATCOM [2-6]. These are summarized as follows.

The research work in [2] presents the method of reactive current control by using phase angle control. The proposed method is applied to a laboratory set-up of 117V, 1.1kVA CSC STATCOM, where off-line PWM method with a switching frequency of 660Hz is used. The resultant system does not minimize the energy storage elements (e.g., inductance of the dc-link reactor and the filter reactor is 27mH and 6.6mH, respectively). Moreover, the transient response of the system is not considered.

The operating principles of CSC STATCOM with an alternative reactive power control is presented by [3], where the modulation index is controlled together with the phase angle. Dc-link current is regulated at a constant value by phase angle control and the reactive power is controlled by varying modulation index. CSC is modulated by space vector PWM with a switching frequency of 1620Hz. However,

the results are also lack of practical considerations, such as transient response, harmonic distortion levels, minimization of energy storage elements.

The analysis and modeling of CSC STATCOM in dq-synchronous reference frame is presented in [4]. The simultaneous control of phase angle and modulation index is compared with only phase angle control. A mutlivariable full state feedback control is employed for reactive power control in order to achieve fast and non-oscillatory response. It is shown that the proposed control results in satisfactory transient response.

The first industrial application of CSC STATCOM at 1kV, ±500kVA level is presented in [7]. In this application, selective harmonic elimination method (SHEM) is used as modulation method in order to minimize lower order harmonics and switching losses. Reactive power is controlled by varying the dc-link current via phase-shift-angle. The design methods are set out for an application of CSC STATCOM to a medium voltage application. The proposed methods are verified by the results obtained from the field tests. However, the transient response is inherently slow due to the use of off-line modulation technique and the system losses can not be decreased further by the elimination of damping resistors in the input filter.

1.5 Scope of the Thesis

Within the scope of this thesis, the anaylsis, design and implementation of a CSC based STATCOM for low-voltage applications are studied in order to obtain i) fast transient response in reactive power control, ii) low current harmonic distortion, iii) low power losses, iv) minimum storage elements. For this purpose, the simplest three phase current source converter topology is used with an optimized input filter and dc-link reactor. The analysis and the control of CSC STATCOM are carried out in dq-synchronous reference frame and the CSC is modulated by the space vector PWM in

order to generate the reference current waveform. Active damping method is also employed in the control system in order to damp the characteristic of the input filter around its resonance frequency. The proposed control and design methods are verified on a laboratory prototype.

The organization of this thesis is given as follows.

In chapter 2, system description and operation principles of CSC STATCOM is described. Current control method and reference current generation by using dq theory is explained with current control block illustrations. Active damping method and passive damping method is compared and the theory of active damping technique is explained. Different on-line PWM methods are evaluated and finally current commutation types are described.

In chapter 3, design principles of CSC STATCOM are presented. Specifications of designed laboratory prototype is given first and secondly selection of modulation technique is explained. Design of dc-link reactor and input filter is described in detail. Selection of power semiconductors and design of power stage is explained and finally control system design is presented.

In chapter 4 theoretical and experimental results are presented.

In chapter 5, contributions of the thesis are summarized and concluding remarks, and recommended future works are proposed.

The simulation model of the CSC STATCOM is given in appendix A. In appendix B, the block diagrams for the generation of switching signal are given for dead band sinusoidal pulse-width modulation and space vector modulation, respectively. The internal structure of the insulated gate bipolar transistor which is used in this research is presented in appendix C.

CHAPTER 2

SYSTEM DESCRIPTION

2.1 Introduction

The problems on electrical power quality have been seriously considered by the utility authority and the consumers in Turkey, since 2000. Therefore, the Energy Regulatory Authority of Turkey imposed strict limits on the harmonic currents and the reactive power demand for the consumers in order to improve the power quality and reliability of the Turkish Electricity System. As the limits get tighter, new power quality conditioners which present fast, accurate and complete solution for the power quality problems have been introduced. Static synchronous compensator (STATCOM) which has been known and mainly applied to medium voltage for nearly 20 years become a strong candidate for low-voltage distribution systems as the cost of system parts in STATCOM decreases.

In addition to reactive power compensation, a distribution type static synchronous compensator (D-STATCOM) may have the capability of filtering load harmonics and balancing unbalanced loads. These features are only achieved by the application of an on-line generated pulse-width modulation (PWM) to the switching power converter of STATCOM. The switching power converters are basically classified as voltage-source converter and current-source converter. In spite of the extensive research and application of voltage-source converter based STATCOM, the current-source converter based STATCOM has not been well exploited in industry, yet.

The three phase current source converter based static synchronous compensator (CSC STATCOM) is composed of a current-source type converter and can be applied as a D-STATCOM in the distribution systems by employing appropriate PWM technique and control methods.

In this chapter, system description and operating principles of CSC STATCOM will be covered. Current control of CSC STATCOM will be analyzed in detail. Active damping method and PWM modulation technique will be described theoretically. Finally commutation types will be presented.

2.2 Basic Circuit Configuration and Operating Principles

CSC STATCOM is composed of a forced-commutated current source converter (CSC), a low pass filter, a dc-link reactor and a control system. It generates three phase sinusoidal currents at fundamental frequency with controlled amplitude and phase angle. It is connected to distribution bus as shown in Figure 2.1. CSC STATCOM is able to compensate loads which have rapidly changing reactive power demand.

Undesired reactive components of load currents can be eliminated by generating the current waveforms which have the same amplitude but anti-phase, as shown in Figure 2.2. CSC generates three phase reference currents from dc-link current by switching semiconductors. While dc-link current is kept constant, the amplitude and phase of three phase currents can be adjusted by controlling switching signals.

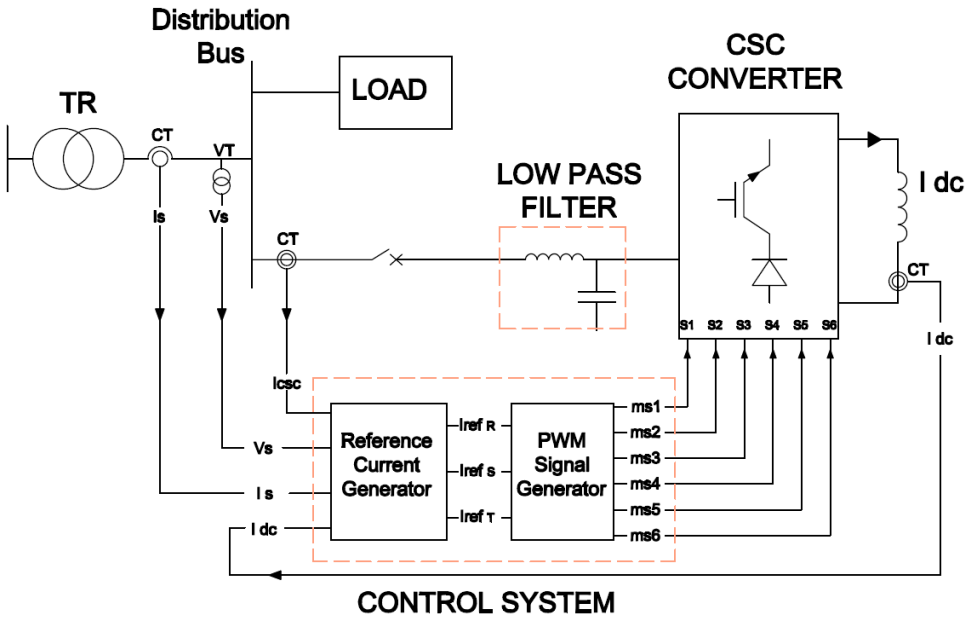


Figure 2.1 CSC STATCOM

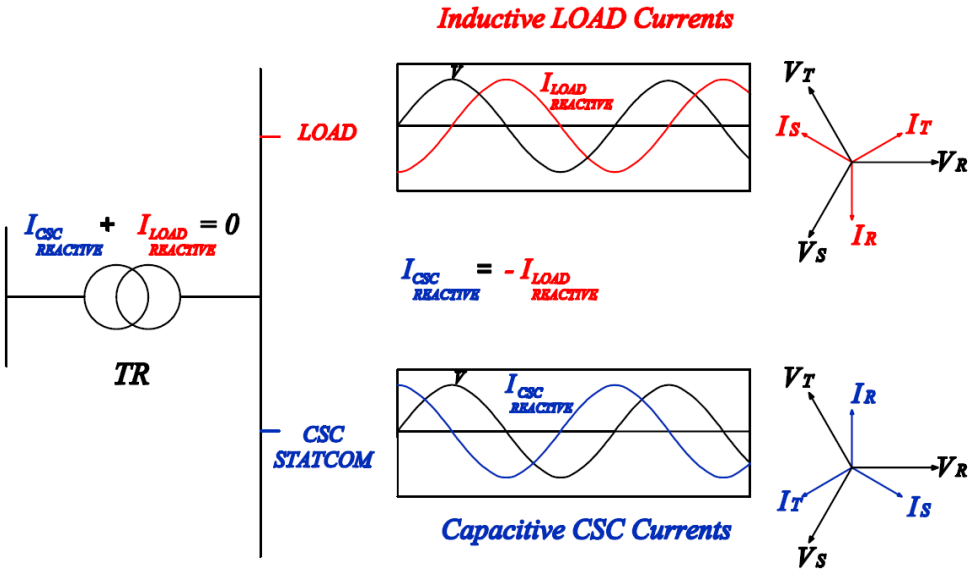


Figure 2.2 Reactive Current Components of Load and CSC STATCOM

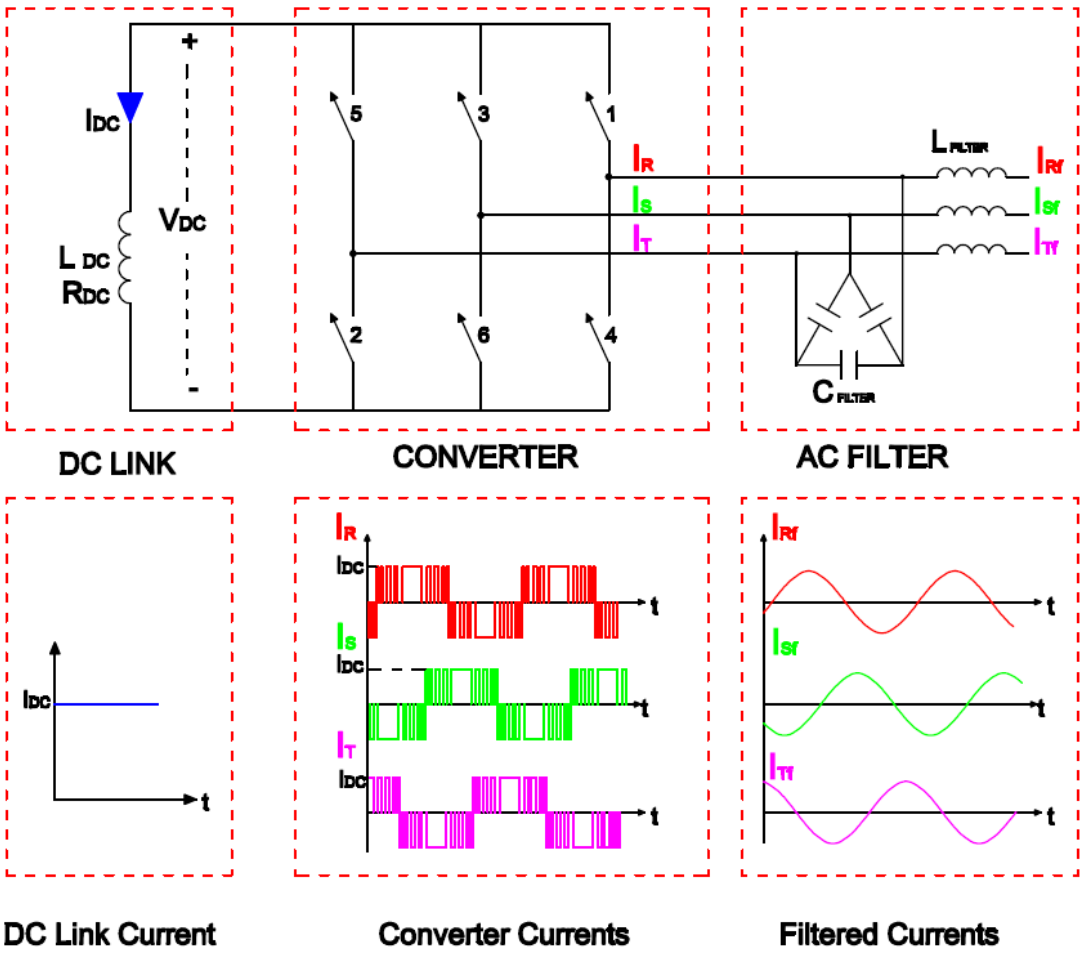


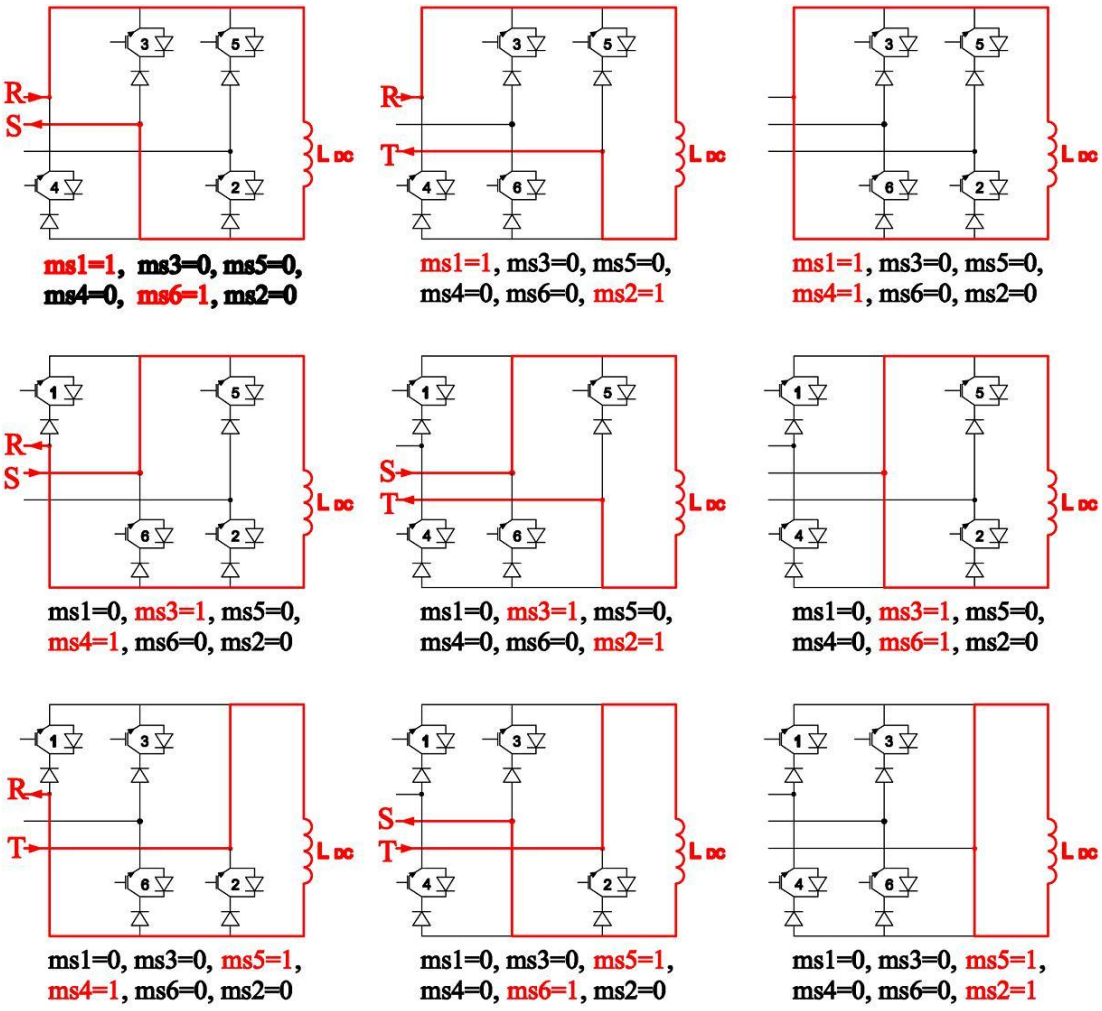
Figure 2.3 Basic Circuit Configuration

Basic circuit configuration of current source converter is shown in Figure 2.3. It is different than voltage-source converter (VSC), such as

- The voltage on each semiconductor switch may be either positive or negative and the current through each semiconductor switch flows only in one direction. This requires fully controllable semiconductor switches, each of which has a unidirectional current carrying and bipolar voltage blocking capability.
- In order to obtain a dc-current source, a reactor has been used in dc-link as the energy storage element. The power loss of the dc-link reactor is represented by its internal resistance R_{dc}.

- Due to the presence of the reactor in the dc-link, the flow of dc-link current must be continuous such that one switch from the upper half and one switch from the lower half of the converter must be conducting at any time.
- The currents generated by the converter are constructed from the dc-link current by switching the power semiconductors with an appropriate modulation technique, as shown in Figure 2.3. They have harmonic current components and should be filtered by a low pass filter to obtain nearly sinusoidal three phase currents at supply frequency.

Control system calculates the reactive components of the load currents by the use of voltage signals at the point of common coupling. Then, it generates the required reference current waveforms (i_{Rref}, i_{Sref}, i_{Tref}) as can be seen in Figure 2.1. PWM signal generator generates switching signals (m_{s1}, m_{s2}, m_{s3}, m_{s4}, m_{s5} and m_{s6}) for the corresponding power semiconductors according to the reference current waveforms. The switching signal is equal to 1 if the corresponding power semiconductor is to be turned on. Otherwise, it is equal to 0. All possible conducting semiconductors and converter line current directions according to the switching signals are shown in Figure 2.4 and Figure 2.5, respectively.



Rule for current source converter switching :

$$ms1 + ms3 + ms5 = 1,$$
$$ms4 + ms6 + ms2 = 1$$

Figure 2.4 Switch Positions

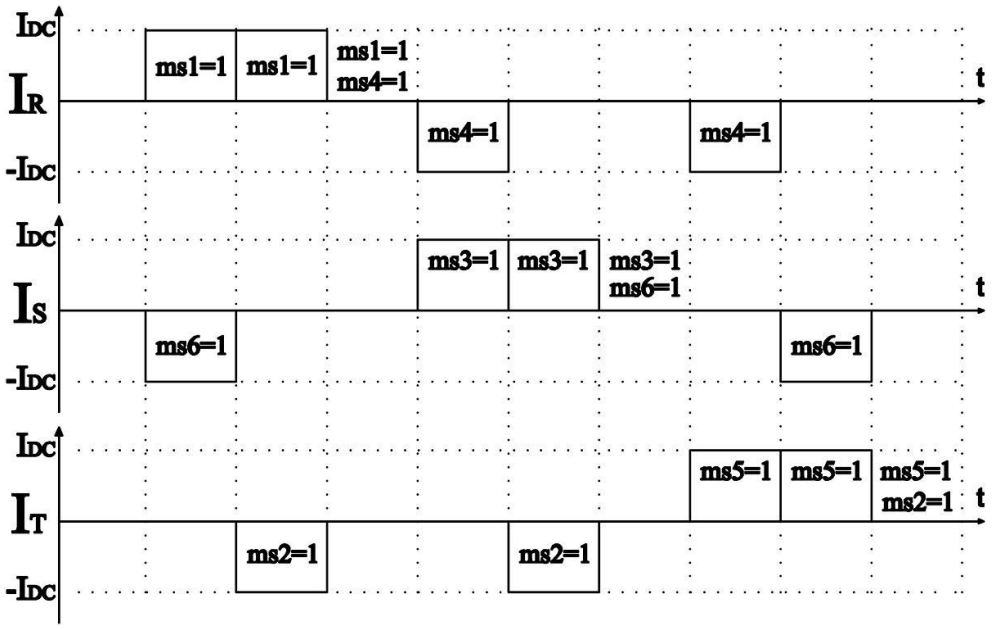


Figure 2.5 Phase Currents

The relation between the switching signals and the converter line currents are illustrated in Figure 2.5 and given in (2.1).

$$\begin{aligned} I_R(t) &= (m_{s1} - m_{s4})Idc = M.I_{dc.}\sin(\omega t + \theta) + \sum_{h=2}^{\infty} I_h \sin(\omega_h t - \lambda_h) \\ I_S(t) &= (m_{s3} - m_{s6})Idc = M.I_{dc}.\sin(\omega t + \theta - 2\pi/3) + \sum_{h=2}^{\infty} I_h \sin(\omega_h t - \varsigma_h) \\ I_T(t) &= (m_{s5} - m_{s2})Idc = M.I_{dc}.\sin(\omega t + \theta - 4\pi/3) + \sum_{h=2}^{\infty} I_h \sin(\omega_h t - \psi_h) \end{aligned} \qquad (2.1)$$

For the converter line currents, the use of an appropriate modulation technique ideally provides a component at the fundamental frequency (e.g., the supply frequency or the frequency of the reference current waveform) and the harmonic components at the carrier frequency and its multiples, as in (2.1). These harmonic components of converter line currents are filtered out and only the fundamental component is used to compensate the reactive load currents.

By the applied modulation method, the modulation index (M) is defined as the ratio of the amplitude of the fundamental component in the converter line current (I_{CSC}) to the dc-link current (I_{dc}).

$$M = \frac{I_{CSC}}{I_{DC}} \tag{2.2}$$

As shown in Figure 2.6, the fundamental component of the converter line current can be decomposed into active and reactive components. Active component is in phase with the corresponding line voltage and the reactive component is in quadrature axis, lagging or leading the corresponding line voltage. Active and reactive components of generated phase currents can be controlled independently. This will be explained in detail by using equivalent circuit of CSC STATCOM in dq-synchronous reference frame.

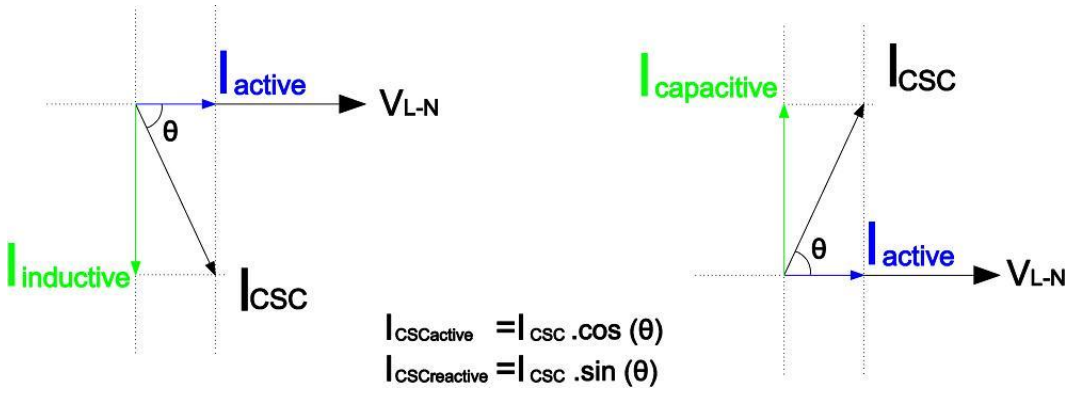


Figure 2.6 Vector Representation of Capacitive and Inductive Currents

2.2.1 Modeling of CSC STATCOM in dq Synchronous Reference Frame

CSC based STATCOM will be modeled in dq-synchronous frame for balanced AC supply. Modelling in dq-synchronous frame supply less number of control variables which are dc at supply frequency. Obtaining dc control variables instead of ac variables provides better filtering of harmonic components and simplicity in controlling the system.

For modeling, the equivalent circuit shown in Figure 2.7 will be used. In this circuit, three phase delta connected filter capacitor bank is connected in wye and equivalent capacitance of each capactior is taken as 3C. Following assumptions will be considered in the modeling:

i)all the power semiconductor switches are lossless

ii)three phase balanced AC supply having harmonic-free line voltages, as defined in Figure 2.7.

$$\begin{aligned} V_R &= V\cos(\omega t) \\ V_S &= V\cos(\omega t - 2\pi/3) \\ V_T &= V\cos(\omega t - 4\pi/3) \end{aligned} \tag{2.3}$$

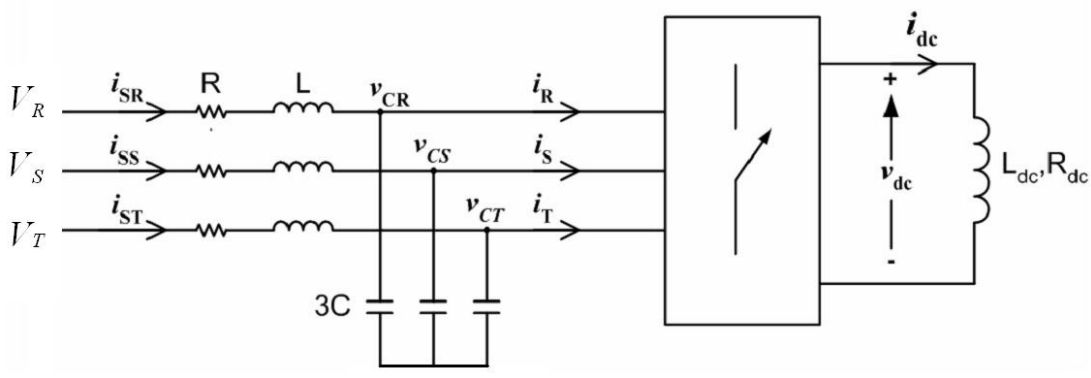


Figure 2.7 Circuit diagram of CSC based STATCOM to be used for modeling

AC side differential equations are given in (2.4) for phase *R*. Same equations can be easily written for the other phases, *S* and *T*.

$$\begin{aligned} \mathrm{V_R} &= \mathrm{Ri_{SR}} + L\frac{di_{SR}}{dt} + V_{CR} \\ i_{SR} &= 3C\frac{dv_{CR}}{dt} + i_R \end{aligned} \tag{2.4}$$

Dc side differential equation of CSC based STATCOM is as follows

$$\mathrm{V_{dc}} = L_{dc}\frac{di_{dc}}{dt} + R_{dc}i_{dc} \tag{2.5}$$

AC side and dc side quantities are coupled with switching functions as in (2.6).

$$\begin{aligned} V_{dc} &= (m_{s1} - m_{s4})V_{CR} + (m_{s3} - m_{s6})V_{CS} + (m_{s5} - m_{s2})V_{CT} \\ I_R &= (m_{s1} - m_{s4})i_{dc} \\ I_S &= (m_{s3} - m_{s6})i_{dc} \\ I_T &= (m_{s5} - m_{s2})i_{dc} \end{aligned} \tag{2.6}$$

Using (2.4), (2.5) and (2.6) these switching functions can be expressed in terms of their Fourier components as in (2.7).

$$\begin{aligned} m_{s1} - m_{s4} &= M\sin(\omega t + \theta) + b_h\sin(\omega_h t - \lambda) \\ m_{s3} - m_{s6} &= M\sin(\omega t + \theta - 2\pi/3) + b_h\sin(\omega_h t - \xi) \\ m_{s5} - m_{s2} &= M\sin(\omega t + \theta - 4\pi/3) + b_h\sin(\omega_h t - \psi) \end{aligned} \tag{2.7}$$

Switching functions do not linearly dependent on the control variables modulation index, *M* and phase angle, θ since they contain harmonic components, which do not depend on modulation index and phase angle explicitly.

In order to linearize the switching functions harmonic components should be neglected. This does not cause any problem in analyzing the system performance since harmonics do not contribute to active and reactive power flow. Then, switching functions can be approximated as in (2.8).

$$\begin{aligned} m_{s1} - m_{s4} &\cong M\sin(\omega t+\theta) \\ m_{s3} - m_{s6} &\cong M\sin(\omega t+\theta-2\pi/3) \\ m_{s5} - m_{s2} &\cong M\sin(\omega t+\theta-4\pi/3) \end{aligned} \tag{2.8}$$

Before applying transformation from *abc*-rotating frame to *0dq* -synchronous frame, (2.4) and (2.6) must be rearranged and put into appropriate matrix form as in (2.9) (2.10) and (2.11) where $p=d/dt$

$$\begin{bmatrix} V_R \\ V_S \\ V_T \\ i_R \\ i_S \\ i_T \end{bmatrix} = \begin{bmatrix} Lp+R & 0 & 0 & 1 & 0 & 0 \\ 0 & Lp+R & 0 & 0 & 1 & 0 \\ 0 & 0 & Lp+R & 0 & 0 & 1 \\ 1 & 0 & 0 & -3Cp & 0 & 0 \\ 0 & 1 & 0 & 0 & -3Cp & 0 \\ 0 & 0 & 1 & 0 & 0 & -3Cp \end{bmatrix} \begin{bmatrix} i_{SR} \\ i_{SS} \\ i_{ST} \\ v_{CR} \\ v_{CS} \\ v_{CT} \end{bmatrix} \tag{2.9}$$

$$v_{dc} = \begin{bmatrix} M\sin(\omega t+\theta) & M\sin(\omega t+\theta-120^0) & M\sin(\omega t+\theta-240^0) \end{bmatrix} \begin{bmatrix} v_{CR} \\ v_{CS} \\ v_{CT} \end{bmatrix} \tag{2.10}$$

$$\begin{bmatrix} i_R \\ i_S \\ i_T \end{bmatrix} = \begin{bmatrix} M\sin(\omega t+\theta) \\ M\sin(\omega t+\theta-120^0) \\ M\sin(\omega t+\theta-240^0) \end{bmatrix} \begin{bmatrix} i_{dc} \end{bmatrix} \tag{2.11}$$

Transformation takes place first from abc-rotating frame to *0αβ*-rotating frame, then to *0dq*-synchronous frame. These are done by proper transformation matrices. These transformation matrices are derived referring to Figure 2.8 as in (2.12) - (2.15).

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = C_1 \begin{bmatrix} 0 \\ \alpha \\ \beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} 0 \\ \alpha \\ \beta \end{bmatrix} \tag{2.12}$$

$$\begin{bmatrix} 0 \\ \alpha \\ \beta \end{bmatrix} = C_2 \begin{bmatrix} 0 \\ d \\ q \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\omega t & -\sin\omega t \\ 0 & \sin\omega t & \cos\omega t \end{bmatrix} \begin{bmatrix} 0 \\ d \\ q \end{bmatrix} \tag{2.13}$$

$$C_1 = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \tag{2.14}$$

$$C_2 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\omega t & -\sin\omega t \\ 0 & \sin\omega t & \cos\omega t \end{bmatrix} \tag{2.15}$$

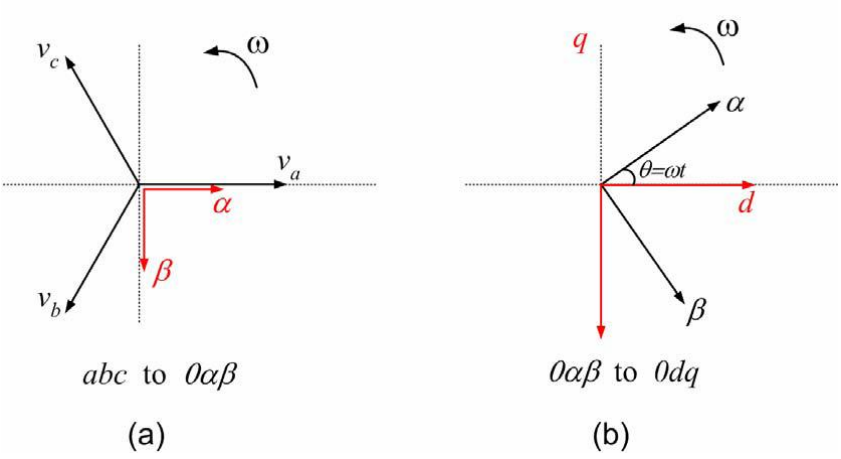


Figure 2.8 Phasor diagrams used in deriving transformation matrices

Since transformation matrices are “orthogonal matrices”, such that they satisfy (2.16) and (2.17).

$$C_1^T C_1 = 1 \tag{2.16}$$

$$C_2^T C_2 = 1 \tag{2.17}$$

The transformation matrices are applied to both sides of (2.9) as in (2.18). These tranformation matrices are also applied to right-hand side of (2.10) and lefthand side of (2.11) as in (2.18) and (2.19) respectively.

$$C_1C_2\begin{bmatrix} v_0 \\ v_d \\ v_q \\ i_0 \\ i_d \\ i_q \end{bmatrix} = \begin{bmatrix} Lp+R & 0 & 0 & 1 & 0 & 0 \\ 0 & Lp+R & 0 & 0 & 1 & 0 \\ 0 & 0 & Lp+R & 0 & 0 & 1 \\ 1 & 0 & 0 & -3Cp & 0 & 0 \\ 0 & 1 & 0 & 0 & -3Cp & 0 \\ 0 & 0 & 1 & 0 & 0 & -3Cp \end{bmatrix} C_1C_2\begin{bmatrix} i_{S0} \\ i_{Sd} \\ i_{Sq} \\ v_{C0} \\ v_{Cd} \\ v_{Cq} \end{bmatrix} \tag{2.18}$$

$$\mathrm{v_{dc}} = \begin{bmatrix} M\sin(\omega t+\theta) & M\sin(\omega t+\theta-120^0) & M\sin(\omega t+\theta-240^0) \end{bmatrix} C_1C_2\begin{bmatrix} v_{C0} \\ v_{Cd} \\ v_{Cq} \end{bmatrix} \tag{2.19}$$

$$\mathrm{C_1C_2}\begin{bmatrix} \mathrm{i_0} \\ \mathrm{i_d} \\ \mathrm{i_q} \end{bmatrix} = \begin{bmatrix} M\sin(\omega t+\theta) \\ M\sin(\omega t+\theta-120^0) \\ M\sin(\omega t+\theta-240^0) \end{bmatrix} \begin{bmatrix} i_{dc} \end{bmatrix} \tag{2.20}$$

Equations in (2.18) and (2.20) can be arranged as in (2.21) and (2.22) respectively.

$$\begin{bmatrix} v_0 \\ v_d \\ v_q \\ i_0 \\ i_d \\ i_q \end{bmatrix} = C_2^{-1}C_1^{-1}\begin{bmatrix} Lp+R & 0 & 0 & 1 & 0 & 0 \\ 0 & Lp+R & 0 & 0 & 1 & 0 \\ 0 & 0 & Lp+R & 0 & 0 & 1 \\ 1 & 0 & 0 & -3Cp & 0 & 0 \\ 0 & 1 & 0 & 0 & -3Cp & 0 \\ 0 & 0 & 1 & 0 & 0 & -3Cp \end{bmatrix} C_1C_2\begin{bmatrix} i_{S0} \\ i_{Sd} \\ i_{Sq} \\ v_{C0} \\ v_{Cd} \\ v_{Cq} \end{bmatrix} \tag{2.21}$$

$$\begin{bmatrix} \mathrm{i}_0 \\ \mathrm{i}_\mathrm{d} \\ \mathrm{i}_\mathrm{q} \end{bmatrix} = C_2^{-1}C_1^{-1}\begin{bmatrix} M\sin(\omega t+\theta) \\ M\sin(\omega t+\theta-120^0) \\ M\sin(\omega t+\theta-240^0) \end{bmatrix}\begin{bmatrix} i_{dc} \end{bmatrix} \tag{2.22}$$

In applying transformation matrices, the effect of operator "*p*" should be noted as given in (2.23). After applying transformation matrices to (2.19), (2.21) and (2.22), expressions in *0dq*-synchronous frame are obtained and given in (2.24), (2.25) and (2.26).

$$(L_p+R)\cos\omega t = -\omega L\sin\omega t + \cos\omega t(L_p+R) \tag{2.23}$$

$$\begin{bmatrix} v_0 \\ v_d \\ v_q \\ i_0 \\ i_d \\ i_q \end{bmatrix} = \begin{bmatrix} Lp+R & 0 & 0 & 1 & 0 & 0 \\ 0 & Lp+R & -\omega L & 0 & 1 & 0 \\ 0 & \omega L & Lp+R & 0 & 0 & 1 \\ 1 & 0 & 0 & -3Cp & 0 & 0 \\ 0 & 1 & 0 & 0 & -3Cp & 3\omega C \\ 0 & 0 & 1 & 0 & -3\omega C & -3Cp \end{bmatrix}\begin{bmatrix} i_{S0} \\ i_{Sd} \\ i_{Sq} \\ v_{C0} \\ v_{Cd} \\ v_{Cq} \end{bmatrix} \tag{2.24}$$

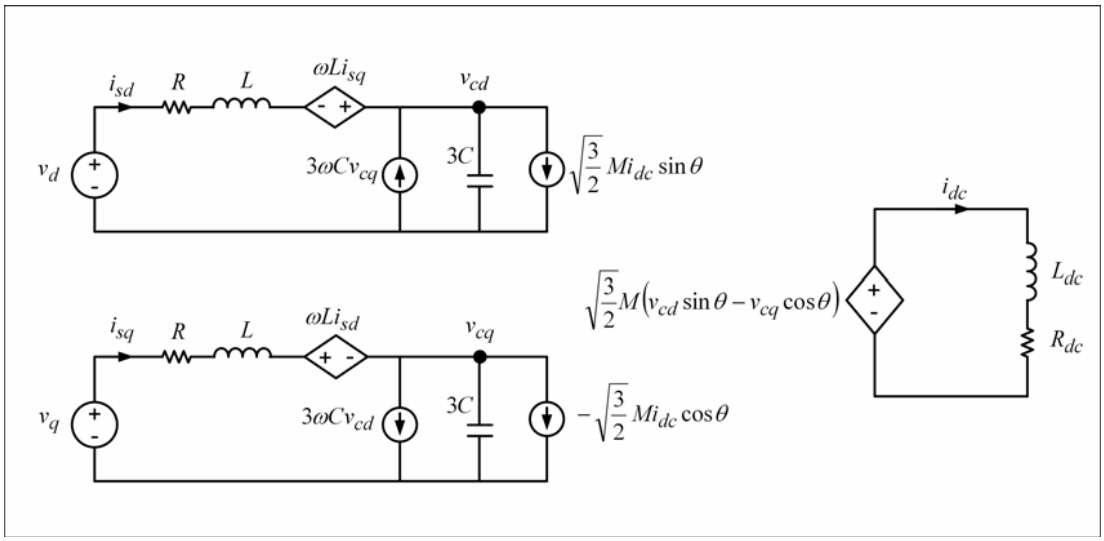
$$\begin{bmatrix} \mathrm{i}_0 \\ \mathrm{i}_\mathrm{d} \\ \mathrm{i}_\mathrm{q} \end{bmatrix} = \begin{bmatrix} 0 \\ \sqrt{\frac{3}{2}}M\sin\theta \\ -\sqrt{\frac{3}{2}}M\cos\theta \end{bmatrix}\begin{bmatrix} i_{dc} \end{bmatrix} \tag{2.25}$$

$$\mathrm{v}_{\mathrm{dc}} = \begin{bmatrix} 0 & \sqrt{\frac{3}{2}}M\sin\theta & -\sqrt{\frac{3}{2}}M\cos\theta \end{bmatrix} \begin{bmatrix} v_{C0} \\ v_{Cd} \\ v_{Cq} \end{bmatrix} \tag{2.26}$$

From the representation of CSC STATCOM in (2.24), (2.25) and (2.26) equivalent circuit in *dq*-synchronous frame can be found as given in Figure 2.9. Advantage of the equivalent circuit in Figure 2.9 is that all quantities at supply frequency become dc quantity in steady-state as shown in Figure 2.10. Based on the transformation matrices and equivalent circuits, active and reactive power can be defined as in (2.27) and (2.28).

$$P = V_d I_{sd} + V_q I_{sq} \tag{2.27}$$

$$Q = -V_d I_{sq} + V_q I_{sd} \tag{2.28}$$



(a)

Figure 2.9 Equivalent circuit of CSC based STATCOM in dq-synchronous frame for transient state

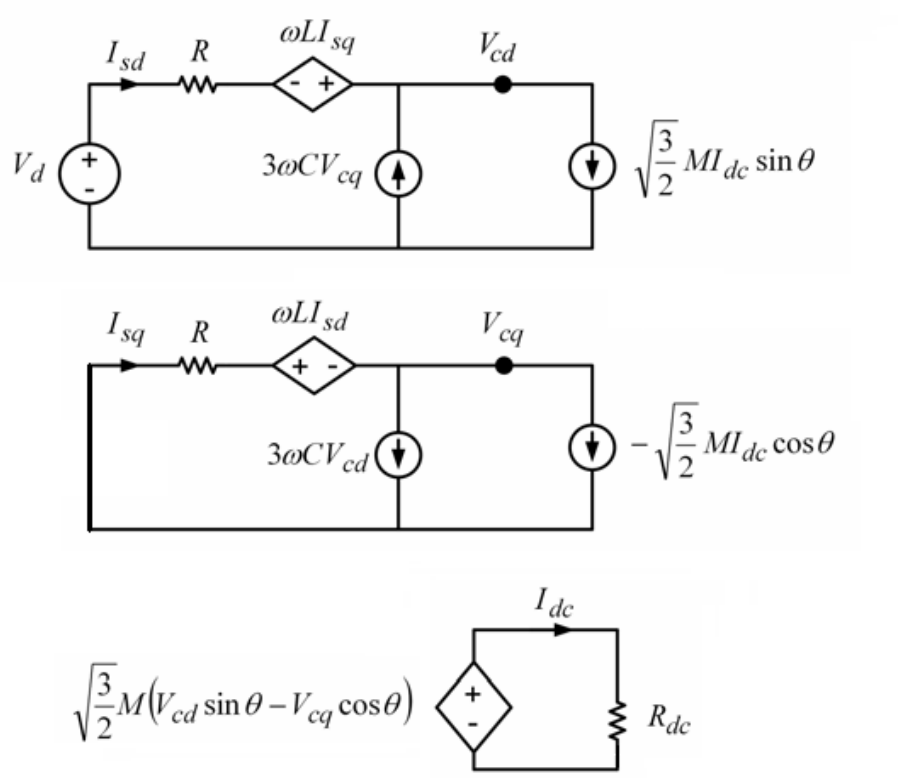


Figure 2.10 Equivalent circuit of CSC based STATCOM in dq-synchronous frame for steady state

In the presented steady state dq model which is given in Figure 2.10, since the supply voltage is balanced V_q component is zero and active power drawn by CSC STATCOM can be calculated by the formula (2.29). Since V_d is constant active power is controlled by changing I_{sd}. I_{sd} is controlled by controlling active component of converter current i_d.

$$P = V_d I_{sd} + V_q I_{sq} = V_d I_{sd} \tag{2.29}$$

In the steady state model of dc-link only internal resistance of the dc-link reactor is taken into account and active power of dc-link can be calculated by (2.30).

$$P_{dc} = \sqrt{\frac{3}{2}} MI_{dc} \sin\theta . v_{Cd} - \sqrt{\frac{3}{2}} MI_{dc} \cos\theta . v_{Cq} = I_{dc}^2 R_{dc}$$
$$i_d = \sqrt{\frac{3}{2}} MI_{dc} \sin\theta \qquad i_q = \sqrt{\frac{3}{2}} MI_{dc} \cos\theta \tag{2.30}$$
$$P_{dc} = i_d v_{Cd} - i_q v_{Cq} = I_{dc}^2 R_{dc}$$

As can be seen in (2.30) P_{dc} should be kept constant in order to have constant dc-link current I_{dc}. Since P_{dc} is constant i_d will be affected from changes in i_q during reactive power control. By controlling i_d dc-link current is tried to be kept constant. Control of dc-link current is achieved by using control blocks given in Figure 2.11.

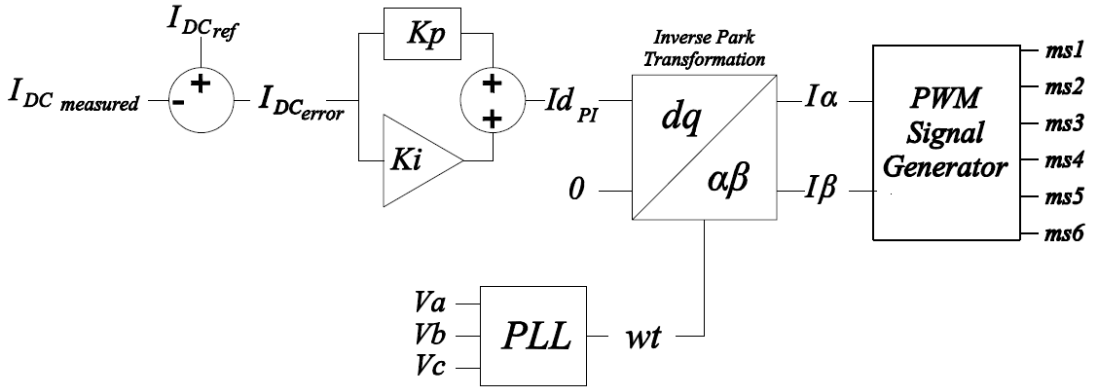


Figure 2.11 Active Current Control

I_{DCref} is the set value for dc current. $I_{DCmeasured}$ is the measured dc-link current value. The difference between reference dc current and measured dc current is kept zero by close loop PI type controller. PI controller gives (Id_{PI}) current as output and it is

transformed by inverse park transformation block. PWM signal generator calculates m_{s1}, m_{s2}, m_{s3}, m_{s4}, m_{s5} and m_{s6} switching signals which generates active current component. If Iq_{PI} component is taken as zero CSC STATCOM does not generate reactive current. By using this control method dc-link current is kept at a constant I_{DCref} value. Dc-link current value limits the peak value of generated CSC current. If modulation index takes its maximum value M=1 dc-link current is equal to peak value of CSC current (2.2).

As can be seen in Figure 2.10 V_q component is zero in steady state conditions and reactive power can be calculated by using (2.31). Since the supply voltage V_d is constant reactive power can be controlled by controlling I_{sq}. I_{sq} is controlled by controlling reactive component of converter current i_q.

$$Q = -V_d I_{sq} + V_q I_{sd} = -V_d I_{sq} \tag{2.31}$$

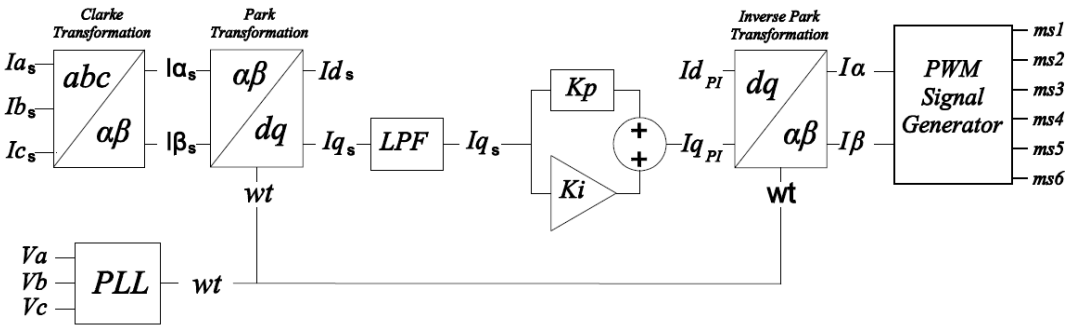


Figure 2.12 Reactive Current Control

In Figure 2.12 three phase supply currents at point of common coupling (Ia_s ,Ib_s and Ic_s) are transformed by Clarke and Park transformations and Iq_s is obtained. Fundamental component of reactive supply current is filtered by a low pass filter.

Fundamental component of Iq_s is kept zero by using close loop PI type controller. PI controller gives Iq_{PI} current as output. Iq_{PI} and is transformed by inverse park transformation block. PWM signal generator calculates m_{s1}, m_{s2}, m_{s3}, m_{s4}, m_{s5} *and* m_{s6} switching signals which generates reactive current component.

The total block diagram of the proposed control system based on dq-synchronous reference frame is given in Figure 2.13. Since the equivalent circuit of CSC STATCOM in dq-synchronous reference frame presents decoupled control variables (i_d, i_q), the dc-link current can be controlled by active power transfer from ac-side to dc-side or vice versa via i_d. On the other hand, the reactive current of CSC STATCOM can be indepedently controlled via i_q.

Therefore, the control system is composed of two parts: dc-link current control and the reactive curent control. The conventional proportional-integral (PI) controller is used both for the dc-link control and the reactive current control.

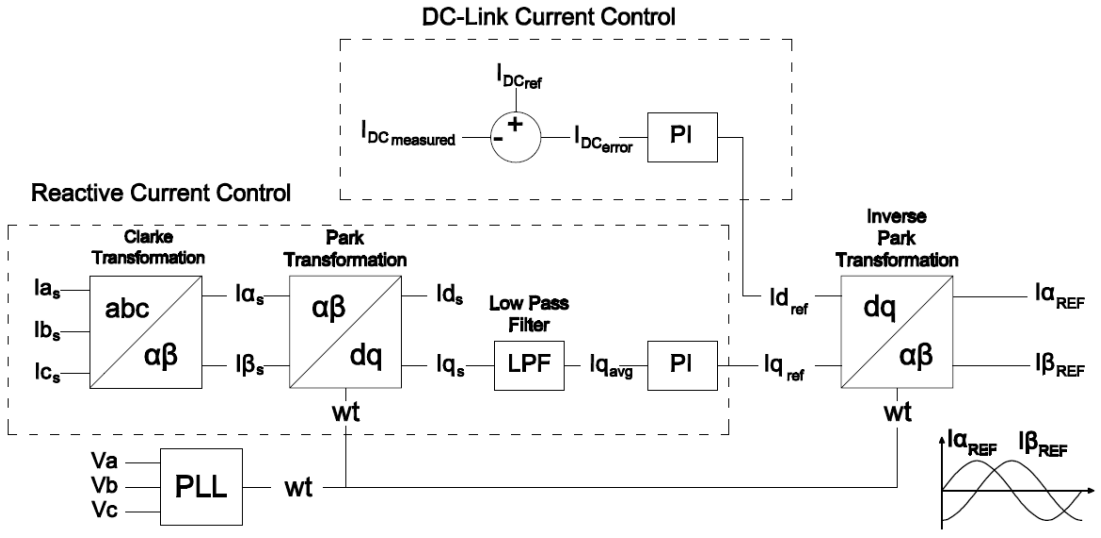


Figure 2.13 Reference Current Generation

Direct axis component of reference current (Id_{ref}) gives active component information of reference current and quadrature axis component (Iq_{ref}) gives reactive component information of reference current. Id_{ref} and Iq_{ref} components are converted to $I_{\alpha REF}$ and $I_{\beta REF}$ by using inverse park transformation block.

2.2.1.1 Active Damping Method

In Figure 2.14, a typical frequency response of a LC filter is given. The red line shows the lightly damped frequency response, where the power loss in the filter is negligibly small (i.e., the internal resistance of the filter reactor, r_f is small). The blue line shows under damped frequency response where a considerable power loss in the filter exists due to the presence of R_d.

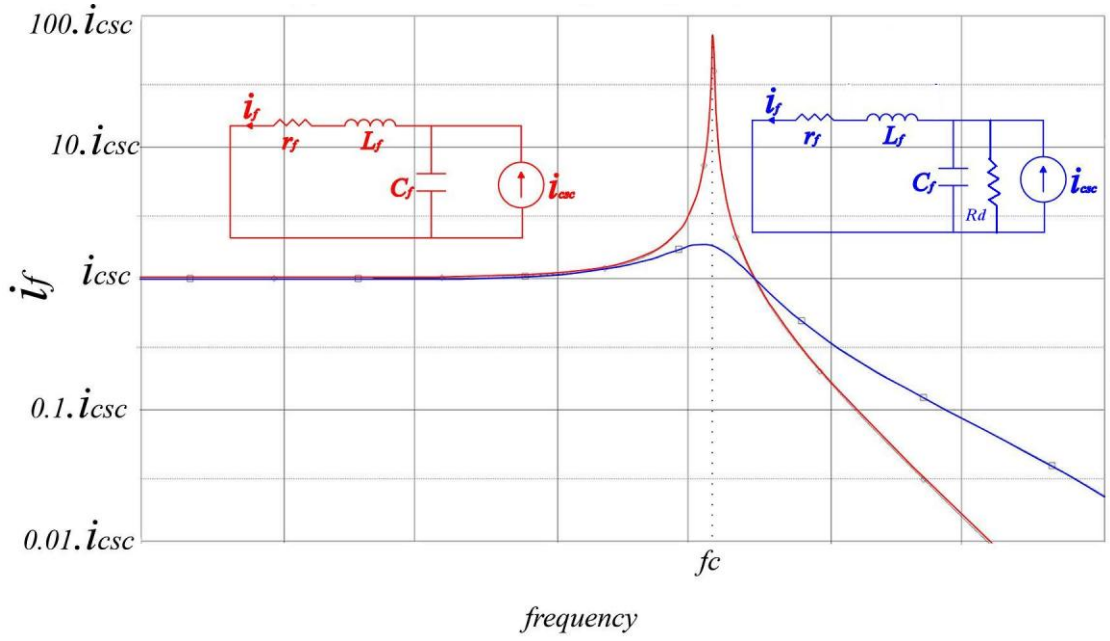


Figure 2.14 Frequency Response of LC filter with & without Damping Resistor

Lightly damped LC filters used in current source converter applications may cause oscillations even if a small harmonic component of the converter line current exists at a frequency around the corner frequency (f_c). In order to damp these oscillations quality factor Q of the designed filter should be low. Introducing a damping resistor increases the power loss in the filter and minimizes quality factor Q of the filter (2.32) ω is defined to be the angular frequency of the system.

$$Q = \omega \times \frac{\text{Energy Stored}}{\text{Power Loss}} \tag{2.32}$$

As can be seen in Figure 2.15, damping resistor can be connected in series with filter reactor, parallel to filter reactor [6], in series with filter capacitor or parallel to filter capacitor. But in high power applications, this resistor causes undesired power losses.

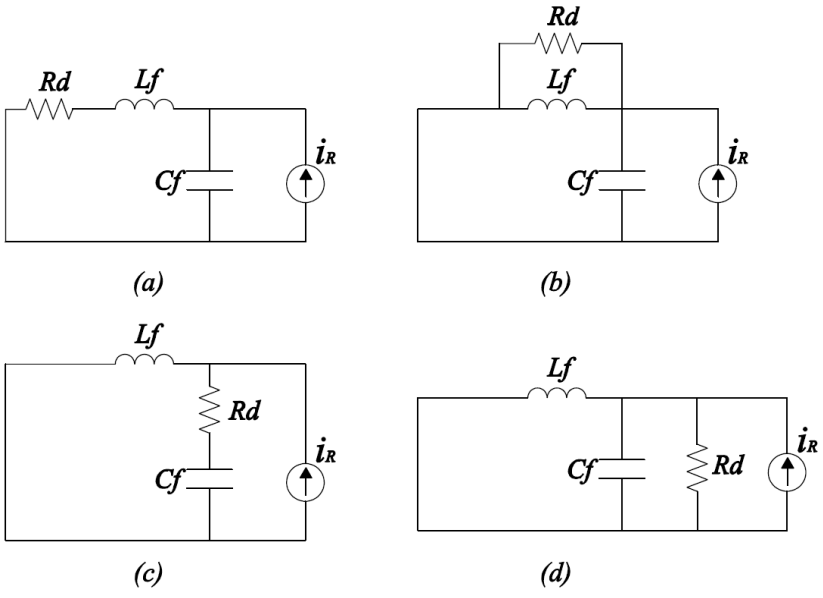


Figure 2.15 Connection of Damping Resistor

Active damping method proposes that a virtual damping resistor can be implemented by the flexible current generating capability of CSC, where on-line PWM methods are employed [10-14].

As can be seen in Figure 2.16, voltage across the damping resistor is equal to voltage across the filter capacitor V_c. Since the damping resistor is not effective at the fundamental frequency, i.e., the supply frequency, the supply voltage can be considered to be short circuit in the equivalent circuit in Figure 2.16. Moreover, if filter resistance (r_f) is ignored, then the voltage across R_d is also equal to the voltage across the filter inductance V_l. V_l can be calculated by measuring the line current of the filter reactor.

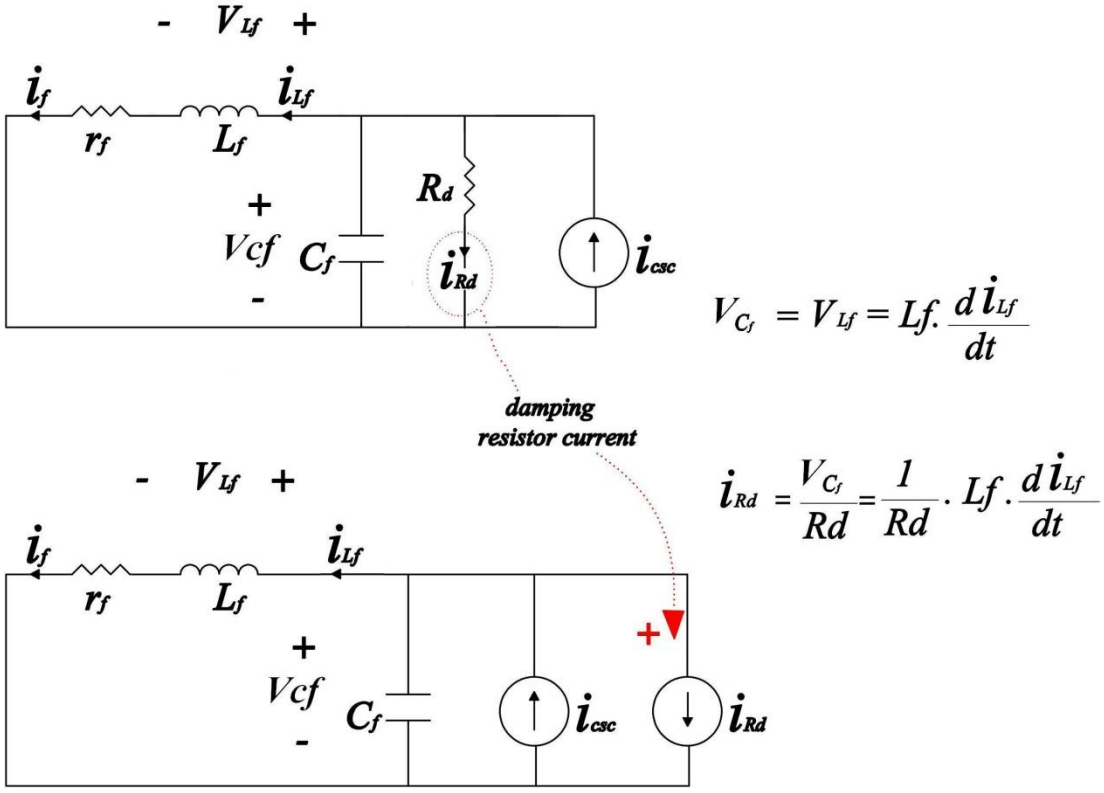


Figure 2.16 Active Damping Method

By taking the derivative of measured STATCOM line current and multiplying it by the inductance of the filter reactor and then dividing it to the resistance of the virtual damping resistor, the damping current can be obtained (see Figure 2.16).
Since the reference current waveform to be generated by the CSC is obtained in α-β rotating frame, the currents of the virtual damping resistor are also obtained in α-β rotating frame. For this purpose, the three-phase STATCOM line current quantities transformed into α-β rotating frame by Clarke transformation.

The current waveform of the virtual damping resistor can then be added to reference currents which are calculated from dc-link current and reactive current control, I_{dref} and I_{qref}, respectively as illustrated in Figure 2.17.

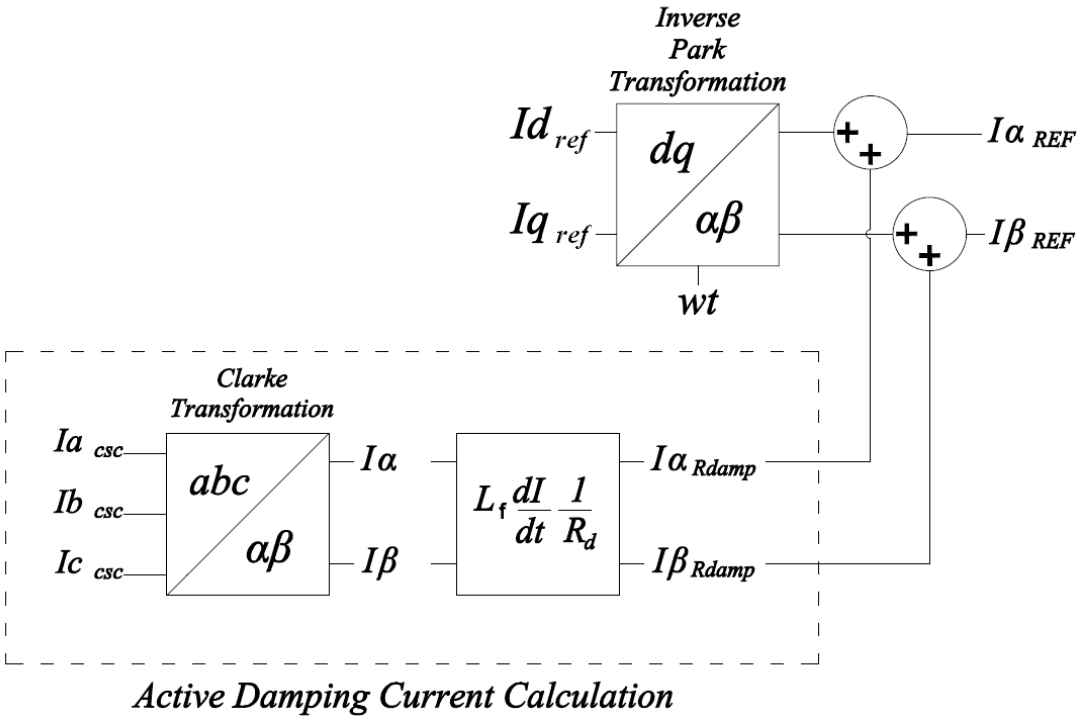


Figure 2.17 Active Damping Reference Current Calculation

Selection of the virtual damping resistance requires a good compromise. A small damping resistance is preferred for decreasing *Q* of the filter, thus minimizing the oscillations around corner frequency. On the other hand, unnecessarily small damping resistance makes the active damping loop gain too high such that the contribution of the damping current to the reference current becomes too high and the dc-link current and the reactive current control is lost. Selection of damping resistor will be explained in chapter 3 in filter design part.

2.3 Modulation Techniques

In voltage source and current source converter applications switching pattern of semiconductor switches are generated by different modulation methods [15-17]. Developments in semiconductor production technologies and the evolution and variation of these modulation techniques are dependent to each other. The frequency limit of the semiconductor switches is the most important parameter which determines the modulation type.

Developed modulation techniques are implementable to high frequency current source converter applications [18-24]. High frequency modulation methods provide the advantage of generating sinusoidal currents with negligible lower order harmonics. Since the lower order harmonics are negligible a smaller low pass input filter can be designed by selecting a higher corner frequency in order to filter harmonics around switching frequency.

Also by applying high frequency modulation techniques dc-link current ripples will be minimized. As long as the modulation frequency is increased a smaller dc-link reactor with a lower time constant will be sufficient in order to generate constant dc current on dc-link of the converter. But as a drawback increase in switching frequency increases switching losses.

Modulation techniques have different nature depending on how they have been generated. They are categorized as off-line techniques and on-line techniques. In off-line techniques switching signals are calculated by optimization techniques as constant patterns in order to eliminate lower order harmonics but, the tradeoff is slow dynamic response and imprecise control of the ac line current. Selective Harmonic Elimination Method (SHEM) is an off-line modulation technique [25]. Online modulation techniques can be classified in analog modulation techniques and digital modulation techniques. Analog modulation techniques are based on the comparison of a reference signal with a carrier signal; they are also named as carrier based modulation methods. Sinusoidal pulse width modulation (SPWM), dead band SPWM (DSPWM) [23], modified dead band SPWM (MDSPWM) are some examples to carrier based PWM techniques which will be analyzed in the scope of the thesis. Digital modulation techniques are based on the space vector technique. There are several space vector PWM (SVPWM) methods which propose different switching patterns are available in literature [26, 24]. And also in this thesis SVPWM method is analyzed and compared with DSPWM and MDSPWM methods. In appendix B generation methods for DSPWM and MDSPWM methods are illustrated.
On-line pattern generation methods are more preferable in high frequency applications with respect to off-line methods, because on-line methods provide faster dynamic response, continuous and precise control of the ac current. Also active damping method is applicable only with on-line modulation techniques.
Comparison results between modulating signals with active damping method will be presented in chapter 3.

2.4 Commutation Types

In the forced-commutated CSC in Figure 2.3, only two power semiconductors, one in the upper half and one in the lower half of the bridge are in conduction at any time so

that the continuous flow of dc-link current can be guaranteed. However, during commutation which can be defined as the transfer of dc-link current among the power semiconductors and takes less than a microsecond for IGBTs, the dc-link current is transferred from one semiconductor to another in the same half of the bridge while one of the semiconductors in the other half is in conduction as shown in Figure 2.18. All possible commutation paths of the current between incoming and outgoing switches are as given in Figure 2.19.

There are two types of commutation; forced commutation and load commutation.

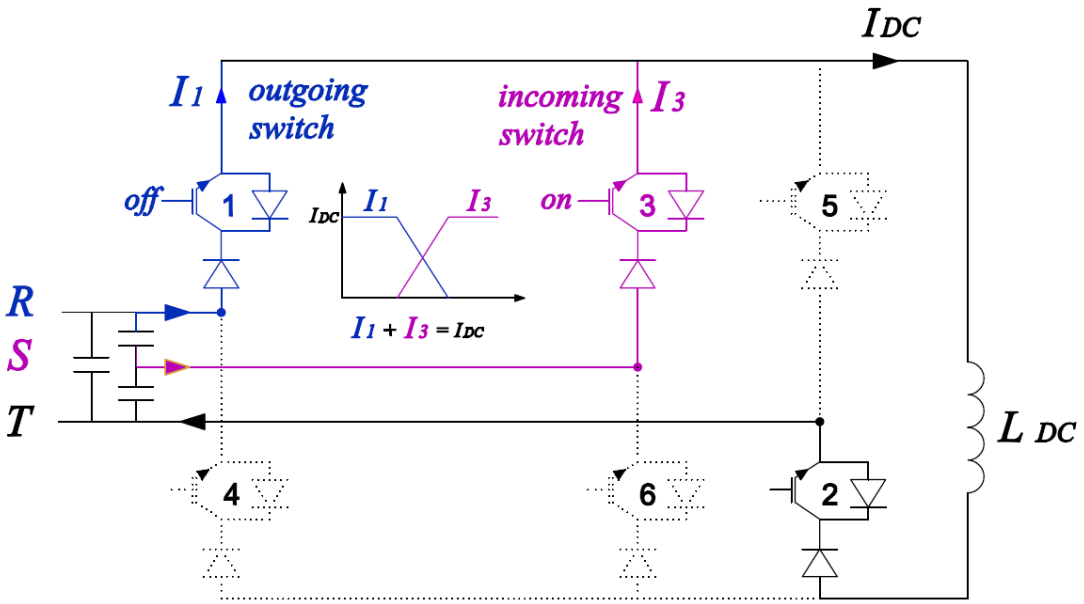


Figure 2.18 Commutation path

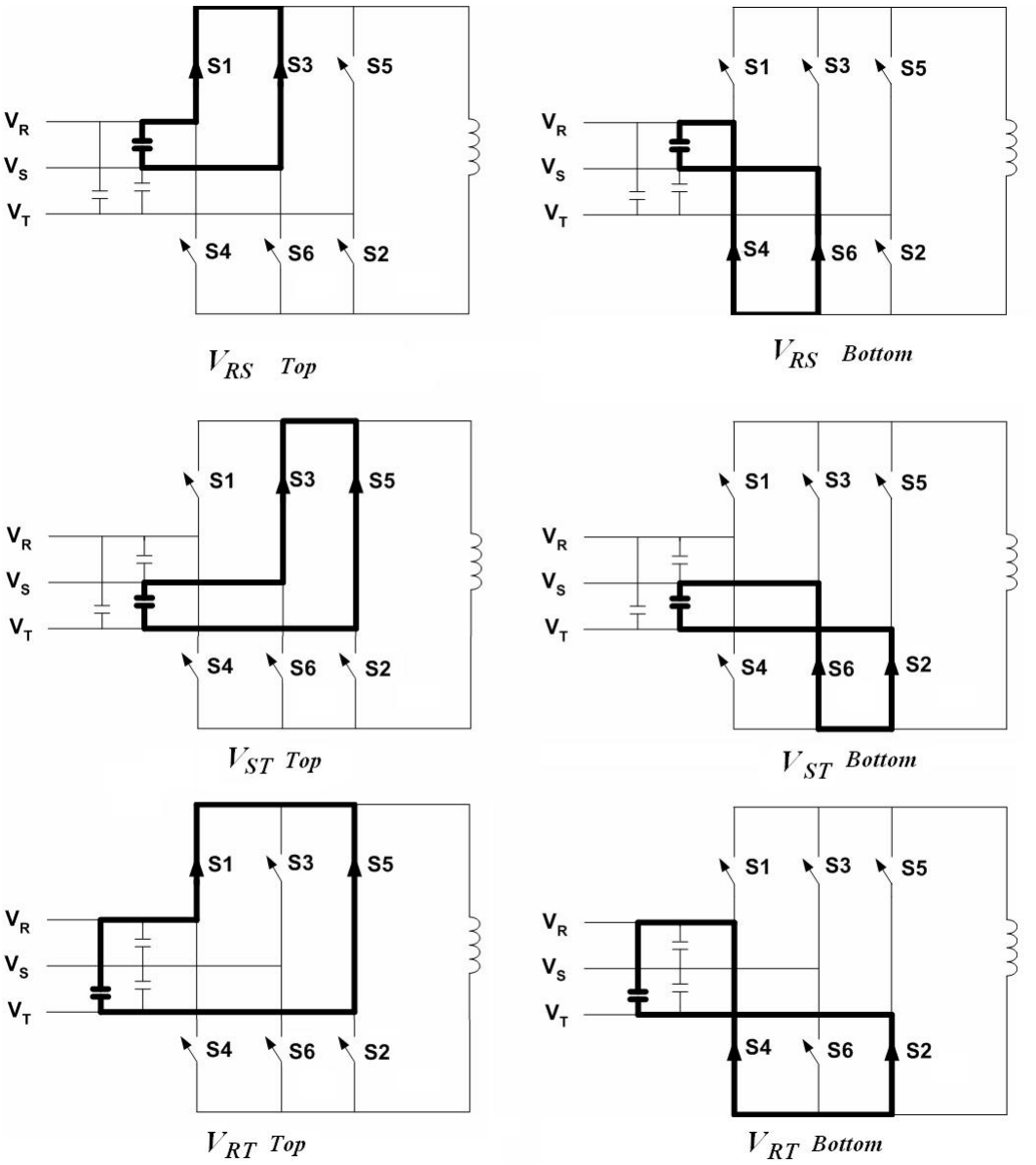


Figure 2.19 Commutation Paths

2.4.1 Forced Commutation

If the voltage across the incoming switch (S_3) is negative just before the commutation (i.e., $V_{RS} > 0$ and series diode of S_3 is reverse-biased and blocking this negative voltage as shown in Figure 2.21), the voltage across the outgoing switch (S_1) will be positive (i.e., IGBT of S_1 will block as shown in Figure 2.21). When the incoming switch receives ON signal, its current does not increase until the voltage across it decreases to zero (i.e., the series diode of the incoming switch is forward-biased). As the outgoing switch receives OFF signal, its voltage starts to increase to line-to-line voltage (i.e., V_{RS} in Figure 2.20). This simultaneously decreases the voltage across the incoming switch. When the voltage across the outgoing switch is equal to line-to-line voltage, the voltage across the incoming switch is equal to zero. After that, the current through the outgoing switch starts to transfer to incoming switch. This transfer continues until the incoming switch full takes over the dc-link current.

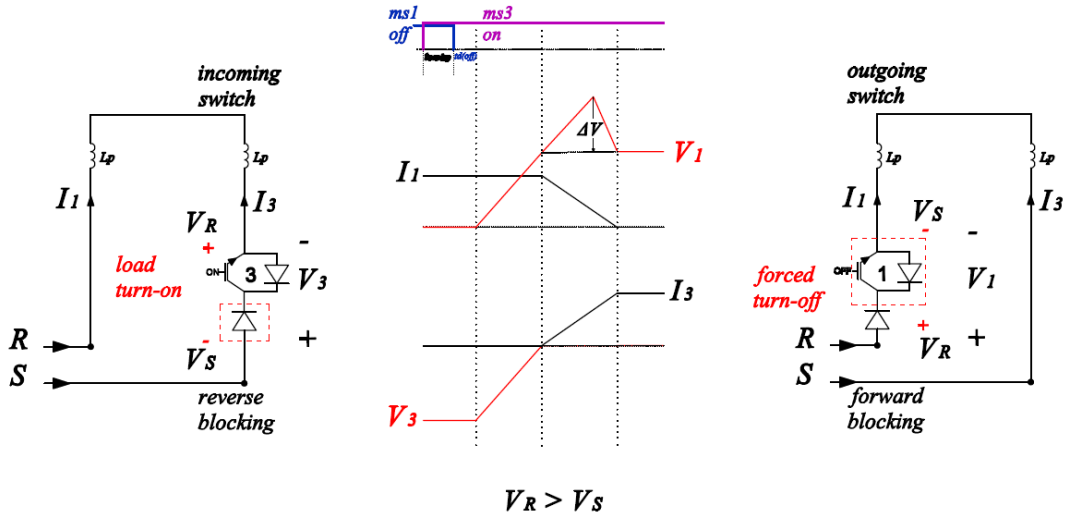


Figure 2.20 Forced Commutation

The mechanism which starts with the generation of ON signal for the incoming switch and ends with the complete transfer of dc-link current from the outgoing switch to incoming switch is called as ***forced commutation***.

The turn-off of the outgoing switch is called as ***forced turn-off*** and the turn-on of the out-going switch is called as ***load turn-on***.

Forced commutation requires that the incoming switch should receive ON signal before the outgoing switch receives OFF signal because the incoming switch should be ready to take over the current before the transfer of dc-link current is initiated. This is illustrated in Figure 2.20 as an overlap in the switching signals, m_{s1} and m_{s3}.

2.4.2 Load Commutation

As shown in Figure 2.21, if $V_R < V_S$ incoming switch voltage polarity is positive when it is not conducting. And the forward voltage is blocked by S_3 IGBT. When S_3 receives on signal the voltage on S_3 starts to decrease after a delay time and current through S_3 starts to increase. This type of turn on is called as ***device turn-on***. Since current on S_1 is decaying, voltage V_1 starts to decrease to V_{RS} value.

When the voltage on S_3 is equal to zero, voltage on S_1 decreases to negative V_{RS} voltage and this reverse voltage is blocked by S_1 diode. This type of turn-off mechanism is called as ***load turn-off***. S_1 switch is turned off by applying reverse voltage on diode without any turn-off signal applied to gate.

Reverse recovery current of diode can be minimized by choosing a better diode characteristics or reducing rate of change of current (*di/dt*). Since the total current I_1+I_3 should be equal to I_{dc}, during reverse recovery process I_3 current exceeds I_{dc} value. Semiconductor current carrying capacity should meet this excessive current.

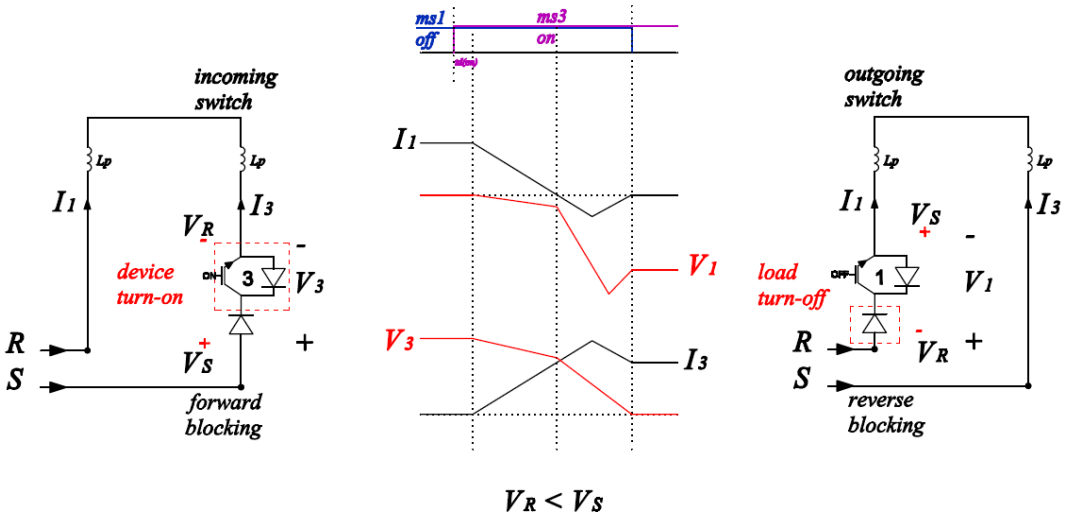


Figure 2.21 Load Commutation

Commutation mechanism, voltage and current characteristics of semiconductor switches during commutation should be understood carefully in order to design current source converter power stage and determine semiconductor device parameters. Selection of semiconductor devices and design of power stage will be explained in detail in chapter 3.

2.5 Summary

In this chapter, system description and operating principles of three phase CSC based STATCOM have been presented. DQ model of CSC STATCOM is derived and dq-control method is explained in detail. The relation between direct axis component of CSC STATCOM current and active power control, and quadrature axis component of converter current and reactive power control is described. Active damping method is introduced and modulation methods for current source converters are discussed. Finally current commutation types are explained and the voltage and current behaviors during commutation are illustrated with figures.

CHAPTER 3

DESIGN OF CSC STATCOM

3.1 Introduction

In chapter 2, theoretical background and operating principles of current source converter (CSC) based STATCOM is introduced. Modulation technique, active and reactive power control technique and active damping method have been explained in detail. These techniques and theoretical methods are modeled by using PSCAD/EMTDC simulation tool [27]. These simulations have shown that the CSC STATCOM provides fast and satisfactory reactive power compensation.

In this chapter design principles of CSC STATCOM will be presented for the implementation of the prototype at low voltage. The design work has been carried out by using simulation tools: PSCAD/EMTDC, MATLAB and ORCAD [27-29].

First, the technical specifications of the prototype are specified. Then, the candidate modulation techniques for the generation of switching signals are benchmarked. The considerations in the design input filter and selection of dc-link reactor are presented. Afterward, the determination of the ratings for power semiconductors is stated. The most challenging design work on the design of power stage is set out in view of the chosen power semiconductors. Finally, the principles in tuning the parameters of the control system are described.

3.2 Design Specifications of CSC STATCOM

Within the scope of this research, the prototype of CSC STATCOM will be designed and implemented at low voltage in order to achieve i) fast transient response in reactive power compensation, ii) low current harmonic distortion, iii) low power losses, iv) minimum storage elements. The technical specifications of the laboratory prototype are given in Table 3.1.

Table 3.1 Technical Specifications of CSC STATCOM

Converter Reactive Power	± 70 kVAr
System Voltage	400V ± %10, 50Hz
Cooling System	Air forced cooling
I_TDD	≤ 5 %

3.3 Selection of Modulation Technique

As mentioned in part 2.3 on-line modulation techniques are compared in this Section. Dead-band sinusoidal pulse width modulation (DSPWM), modified dead-band sinusoidal pulse width modulation (MDSPWM) and space vector pulse width modulation SVPWM techniques are the most common on-line modulation techniques in current source converter applications. The comparison criteria are based on switching frequency, total harmonic distortion and the magnitude of the low-order harmonics.

Switching frequency:

The switching losses directly depend on the switching frequency. Therefore, low switching frequency is preferred. The comparison of the modulation techniques is given in Table 3.2. DSPWM has the highest switching frequency for the same carrier frequency.

Table 3.2 Modulation Technique vs. Switching Frequency

f_c is carrier frequency and f_{cyc} is the sampling frequency

Modulation Technique	Switch.Freq.
DSPWM	$\frac{2}{3} fc$
MDSPWM	$\frac{1}{2} fc$
SVPWM	$\frac{1}{2} fcyc$

Total Harmonic Distortion:

The THD of current is defined as in (3.1) where the I_h is the rms value of the current harmonic components and I_1 is the rms value of the fundamental current component.

$$THD_I = \frac{\sqrt{\sum_{h=2}^{h_{max}} I_h^2}}{I_1} \tag{3.1}$$

The THD_I defining the distortion level can exhibit quite high (misleadingly, unacceptable) values for nonlinear loads operating under light load conditions. However, since the magnitude of harmonic components is low, this high THD_I value is not critical and the influence of the harmonic current on the PCC voltage distortion

is insignificant. In order to avoid such misinterpretation, IEEE 519 defines the term Total Demand Distortion (TDD), which is given in (3.2) where I_h is the rms value of current harmonic hth component and I_L is the rated rms value of the load current at fundamental frequency.

$$TDD = \frac{\sqrt{\sum_{h=2}^{h_{max}} I_h^2}}{I_L} \tag{3.2}$$

This definition accounts for the loading effect of nonlinear loads. Therefore, the harmonic current limits proposed by IEEE 519 are expressed in terms of TDD rather than THD and are given in Table 3.3 for the customers.

Table 3.3 IEEE 519 harmonic current limits

I_{SC}/I_{L1}	h<11	11≤h<17	17≤h<23	23≤h<35	35≤h	TDD (%)
<20	4.0	2.0	1.5	0.6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

To determine optimum modulation technique for CSC STATCOM, PSCAD simulation results are compared for TDD values calculated at two diffrent operating modes; capacitive mode and inductive mode. Carrier frequencies are specified as 6250 Hz and I_L is 70 Arms. In all cases fundamental current component generated by CSC STATCOM is 70Arms and harmonic currents are plotted starting from 2nd harmonics in order to see graphical values. And the TDD value is calculated by the formula given in (3.3).

$$TDD = \frac{\sqrt{\sum_{h=2}^{19} I_h}}{I_L} \tag{3.3}$$

According to the simulation results given in Figure 3.2-3.4, TDD performances of SVPWM and MDSPWM are nearly the same and DSPWM method gives better results, but DSPWM method has higer swithing frequency. DSPWM and MDSPWM are analog on-line modulation techniques and SVPWM is digital modulation technique. Since implementation of SVPWM is more convenient in digital applications it is selected as the modulation technique of CSC STATCOM.

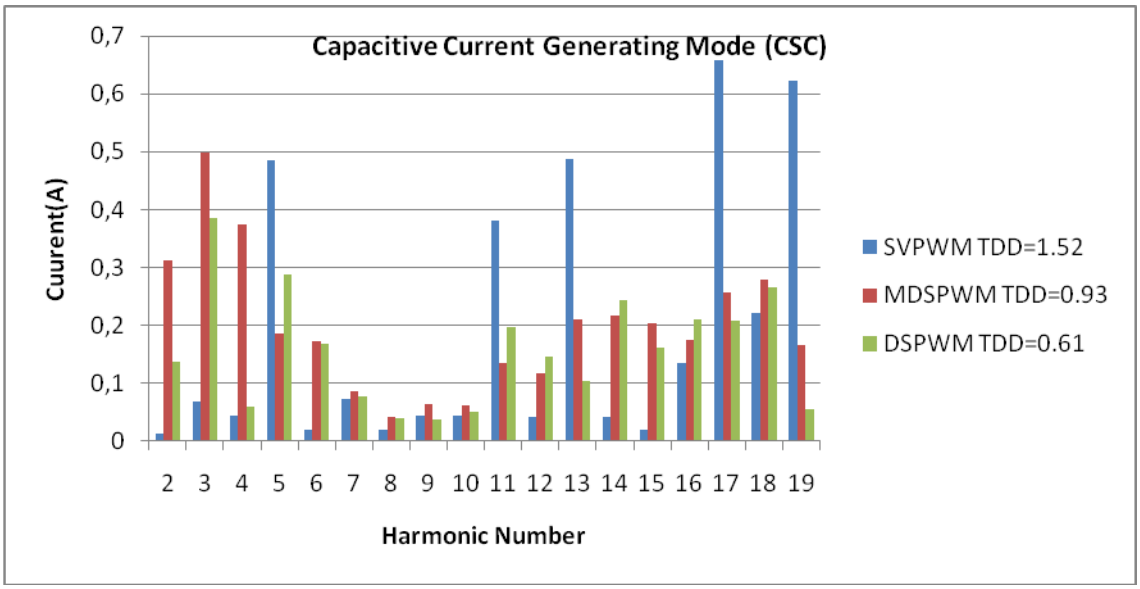


Figure 3.1 Harmonic Spectrum of CSC Current Capacitive Mode

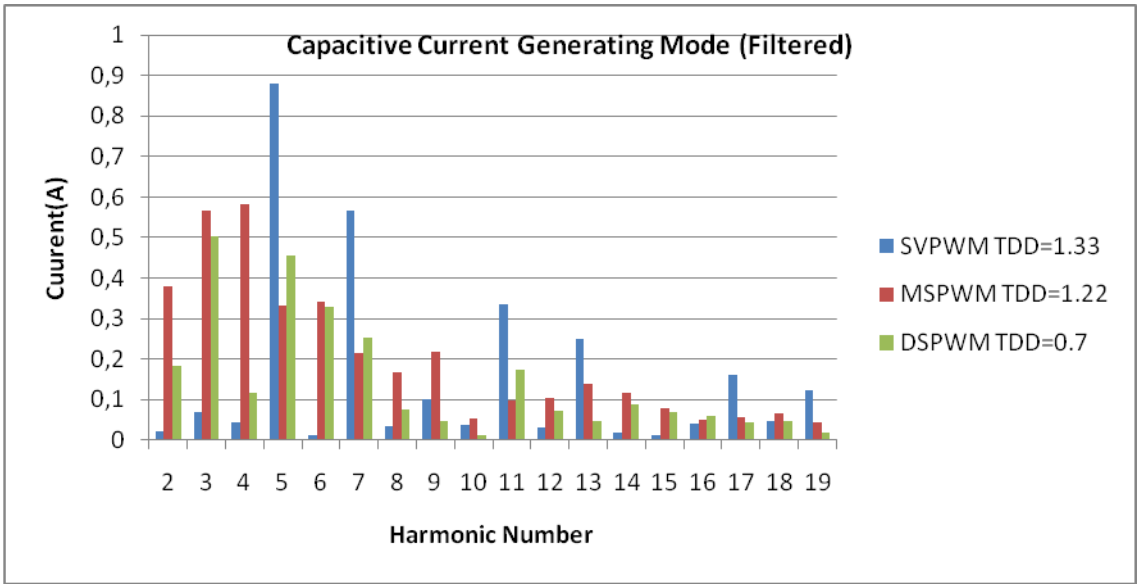


Figure 3.2 Harmonic Spectrum of Filtered CSC Current Capacitive Mode

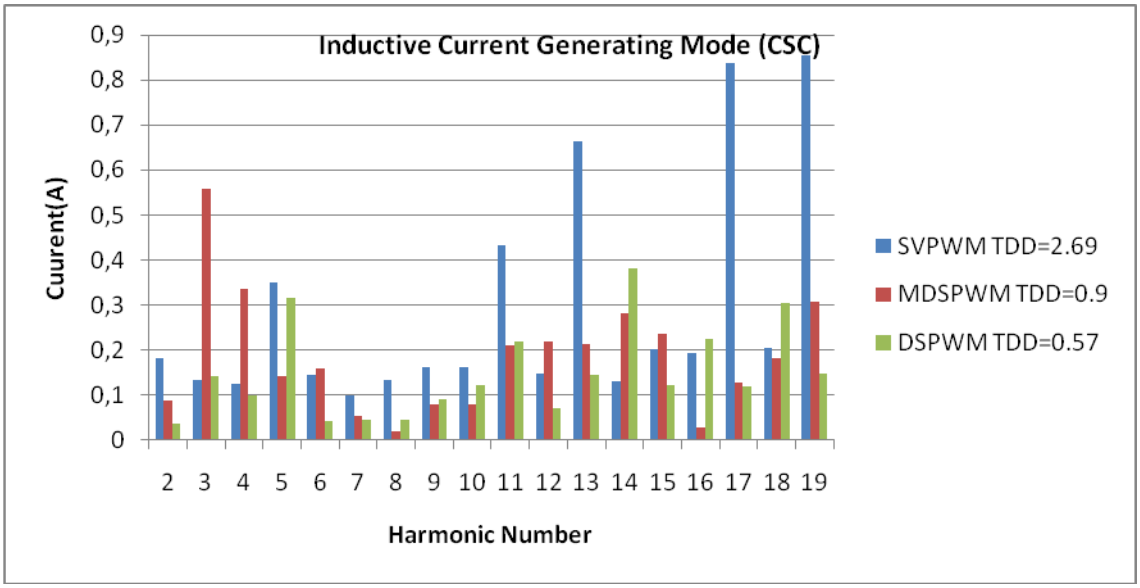


Figure 3.3 Harmonic Spectrum of CSC Current Inductive Mode

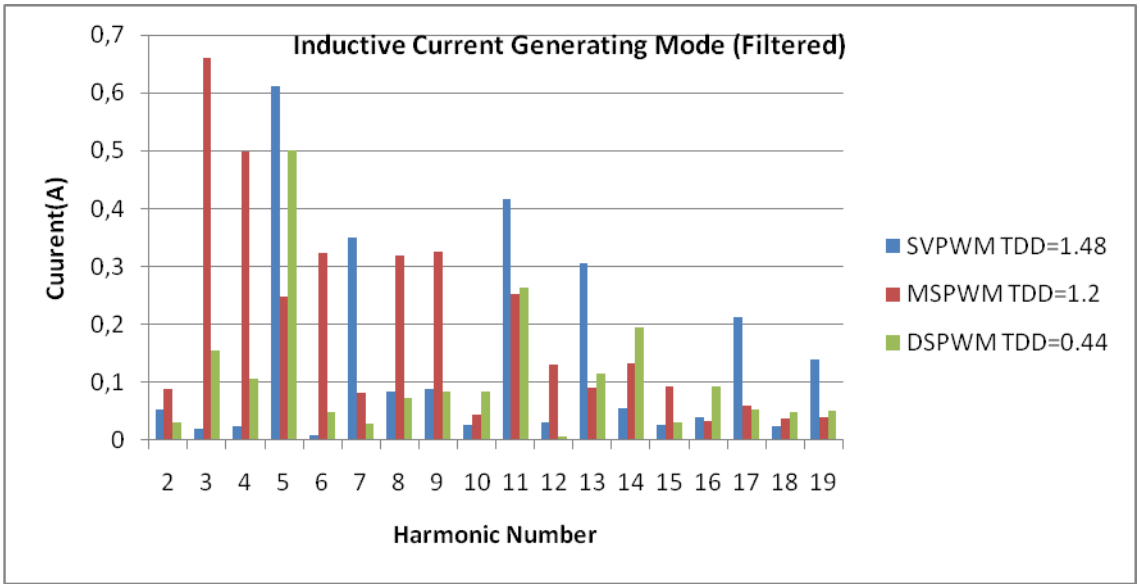


Figure 3.4 Harmonic Spectrum of filtered CSC Current Inductive Mode

3.4 Design of DC Link Reactor

In order to select optimized dc-link reactor value for current source converter, two parameters should be considered; peak-to-peak ripples in dc-link current and the reactor losses.

In Figure 3.5 the variation of dc-link voltage and dc-link current is given. DC-link voltage $V_{dc}(t)$ is composed of mean voltage v_{dc} and ac component $v_{ac}(t)$ which is composed of segments of line-to-line input voltage waveform of CSC and zero voltage segments corresponding to freewheeling operation. Since the voltage pulses are very narrow in high frequency SVPWM modulated current source converters, each pulse can be approximated to step functions as given in (3.8) where n is the number of step functions in one complete cycle and $u_{dc,k}(t)$ is given in Figure 3.5. $i_{dc,k}(t)$ can be found as given in (3.5).

$$V_{dc}(t) = \sum_{k=1}^{n} u_{dc,k}(t) \tag{3.4}$$

$$i_{dc,k}(t) = I_{dc0,k} + \frac{u_{dc,k}(t)}{R_{dc}}(1 - e^{-t/\tau_{dc}}) \tag{3.5}$$

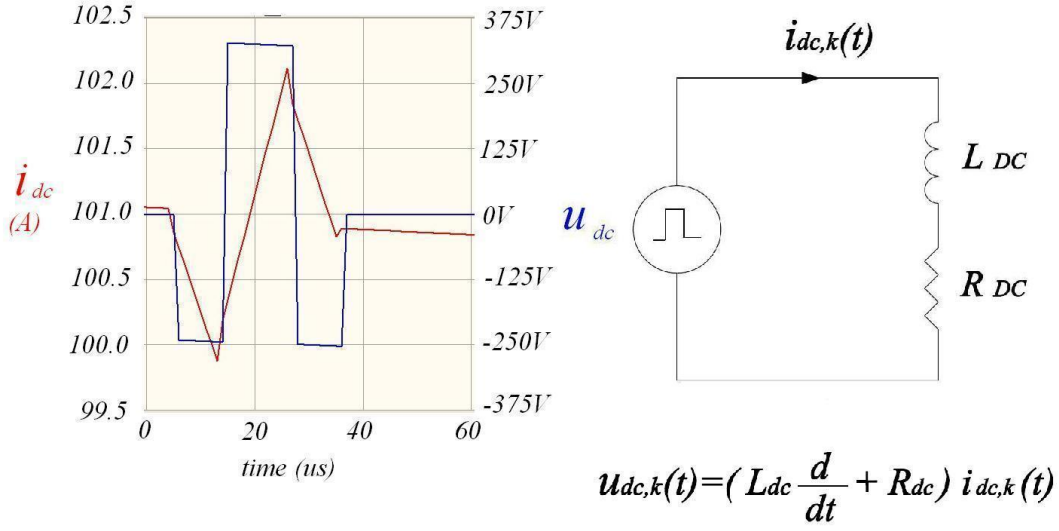


Figure 3.5 DC-Link Voltage and Current

Since time constant of dc-link reactor will be very high (milliseconds) as compared to voltage pulse width (microseconds), (3.5) can be approximated as given in (3.6)

$$i_{dc,k}(t) \cong I_{dc0,k} + \frac{u_{dc,k}(t)}{L_{dc}} t \tag{3.6}$$

As can be understood from Figure 3.5 and dc-link current formula (3.6), changes in dc-link current is directly related with voltage pulse width and amplitude and inversely related with dc-link inductance value. Increase in modulation frequency decreases voltage pulse width. As can be observed from Figure 3.6 if the switching

frequency is increased, peak-to-peak ripples in dc current can be decreased for the same dc-link reactor. On the other hand, this increases the switching loss. If the inductance value is increased when the modulation frequency is kept constant, again the ripples in dc-link current can be minimized. In order to increase DC-link reactor value, the number of turns in the reactor increases, which causes higher copper losses.

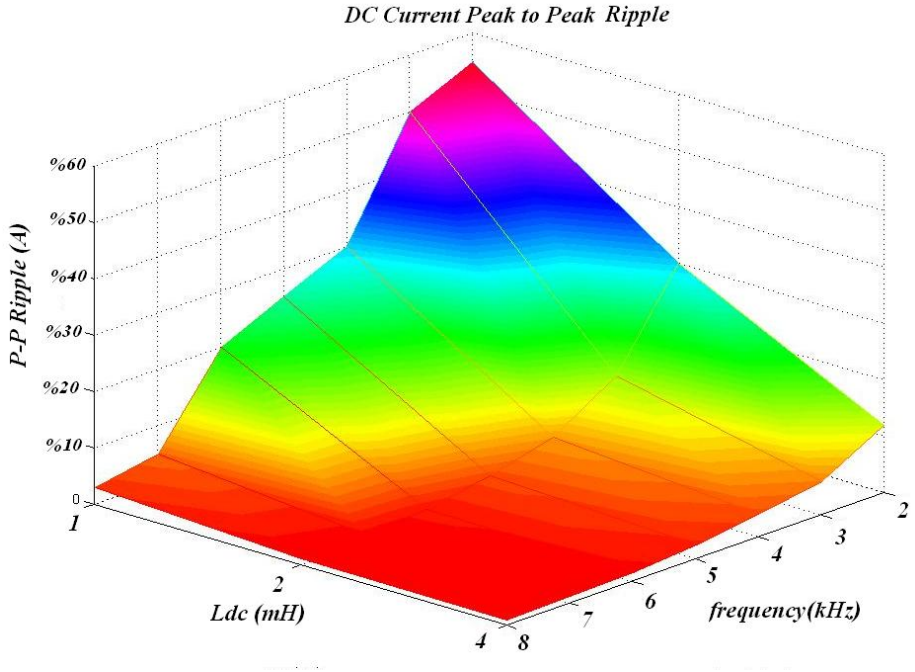


Figure 3.6 DC Current Peak to Peak Ripple

Peak-to-peak ripple (Δi_{dc}) should be minimized because the distorted dc-link current increases harmonic distortion (TDD) in STATCOM line currents. Maximum current, that will be turned off by the semiconductors is given in (3.7). Also, increase in peak-to-peak ripple currents causes higher turn-off current for the semiconductor.

$$I_T = I_{dc} + (\Delta i_{dc} / 2) \tag{3.7}$$

In view of these considerations, the optimum dc-link inductance is chosen to be in order to minimize peak-to-peak ripple, switching losses and dc-link reactor losses. In Figure 3.6 red colored area offers more than one solution at different frequency and different inductance values, but 2mH inductor value is selected at 6250 Hz modulation frequency value as optimum solution.

3.5 Input Filter Design

In order to specify ac filter type and parameters, modulation method should be specified first and harmonic spectrum of generated ac signal should be analyzed.

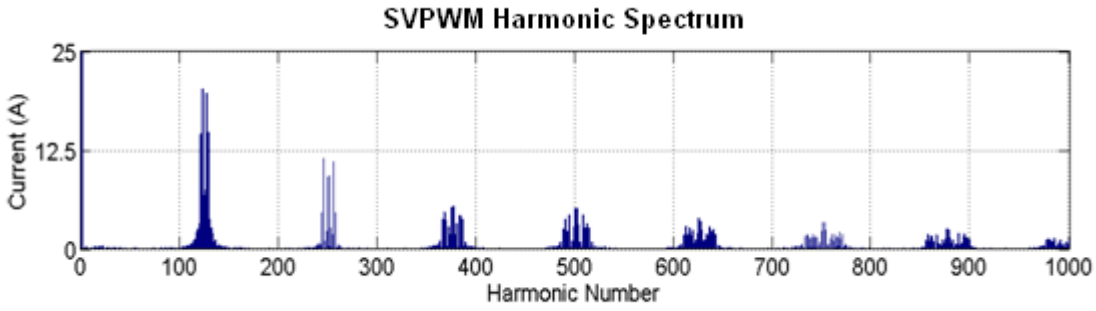


Figure 3.7 (SVPWM) Generated AC Current (I_R) Harmonic Spectrum

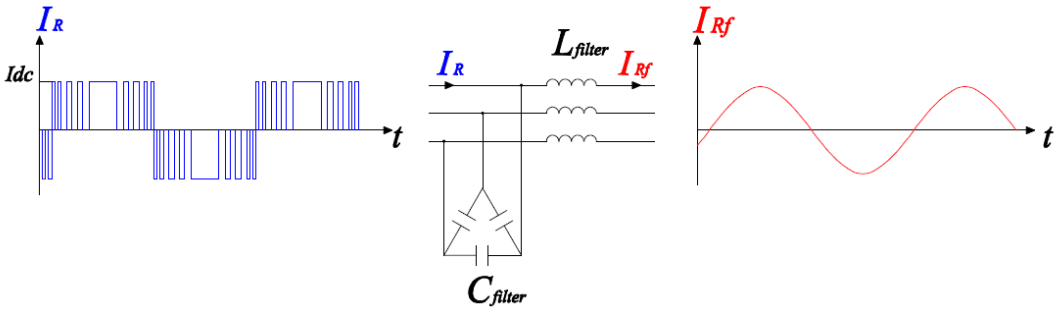


Figure 3.8 Low Pass Filter

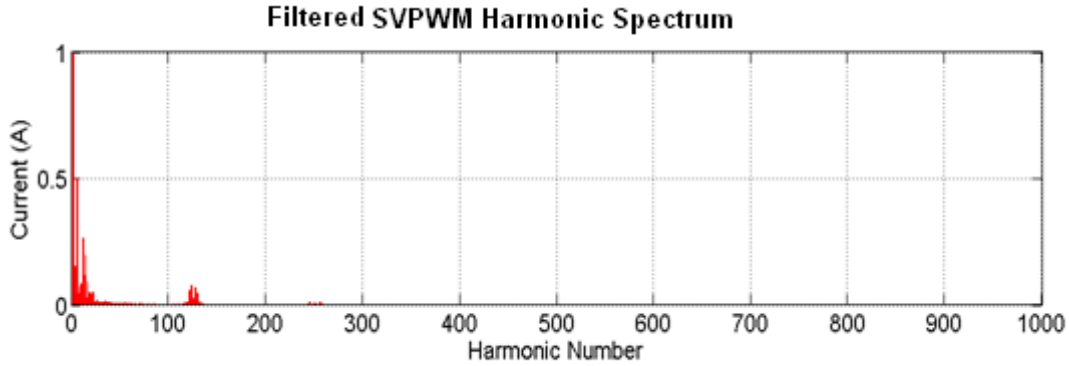


Figure 3.9 (SVPWM) Filtered AC Current (I_{Rf}) Harmonic Spectrum

SVPWM is selected due to its TDD performance and switching frequency as mentioned in part 3.3 .Harmonic spectrum of generated ac signal by SVPWM method is given in Figure 3.7. DC-link current is 100A and carrier frequency is 6250Hz. In Figure 3.7 lower order harmonics are minimized by SVPWM technique, harmonic currents are significant around carrier frequency and its multiples. As illustrated in Figure 3.8 low pass filter should be used to filter these higher order harmonics. In Figure 3.9 filtered ac current harmonic spectrum is given. Only lower order harmonics under corner frequency can pass from this type of low pass LC filter.

Specification of corner frequency (f_c), filter inductance, filter capacitance and damping resistance is the most critical items affecting filter performance.

The single line diagram of LC input filter and un-damped resonance frequency fc of filter is given in Figure 3.10. f_c should be placed between supply frequency and the most significant harmonic components in the converter line current. It should be set to a value as close as the supply frequency to achieve better filtering performance so that these significant high order harmonic components are considerably attenuated. Capacitance value determines the total capacitive VAr produced by the input filter as can be calculated by formula given in Figure 3.10, f_1 denotes supply frequency and V is the rated line to line rms voltage. Capacitive reactive power supplied by filter should be adjusted by considering the inductive reactive power capacitiy of the load.

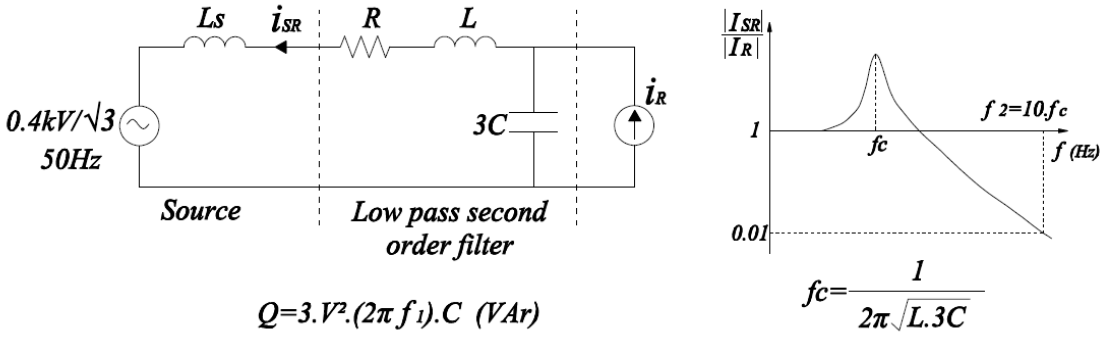


Figure 3.10 Single line diagram of the input filter

As given in

Table 3.4, since input filter supplies constant capacitive reactive power, it should be minimized if the loads are fully capacitive, because STATCOM generates more inductive reactive power in order to compensate same load. It should be increased if the loads are fully inductive, because STATCOM can compensate same load by generating less capacitive reactive power.

Table 3.4 Reactive Power Generation of STATCOM

Input Filter	LOAD	STATCOM
Q kVAr (cap.)	Q kVAr (cap.)	2Q kVAr (ind.)
Q kVAr (cap.)	2Q kVAr (ind.)	Q kVAr (cap.)

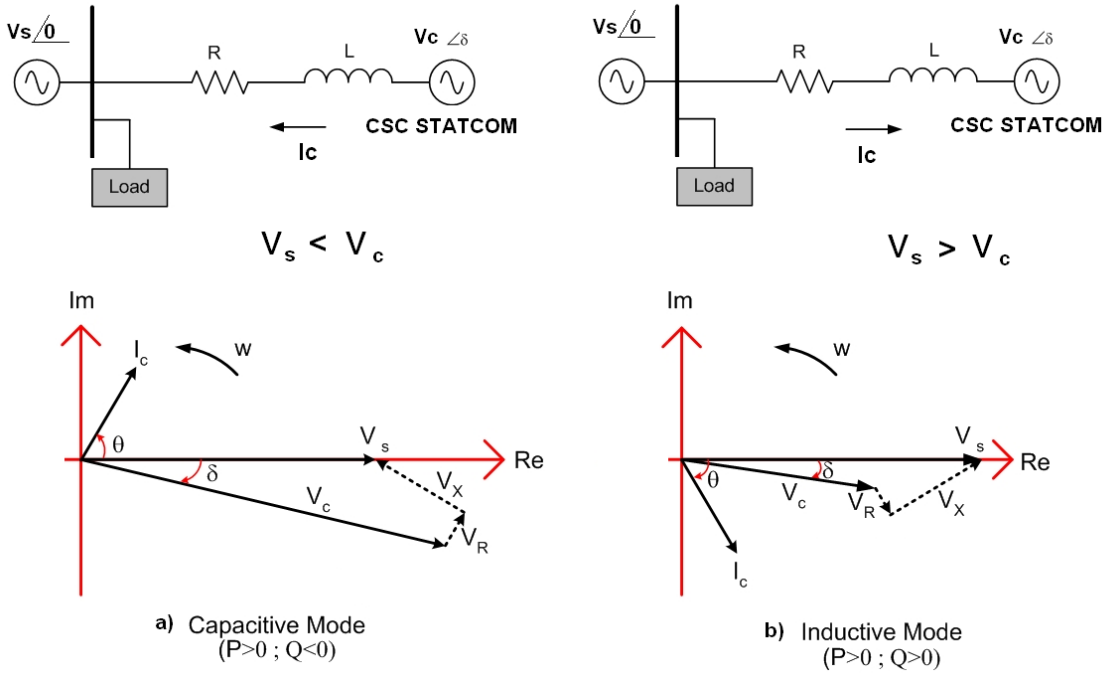


Figure 3.11 Converter Voltage Variation a) Capacitive Mode b) Inductive Mode

Due to presence of the filter inductance, voltage at the input terminals of the converter *Vc* varies with VAr generation of STATCOM, as illustrated in Figure 3.11.

Vc increases over rated system voltage value *Vs* when STATCOM is in capacitive mode and *Vc* is lower than rated system voltage value *Vs* when STATCOM is in

inductive mode. If we assume resistance of filter inductance is negligible (R=0) *Vc* can be calculated roughly by formula given (3.8).

$$V_c = V \pm \frac{Q}{V}(2\pi f).L_f \tag{3.8}$$

Increase in converter voltage in capacitive mode is directly related with filter inductance value, so filter inductance should be optimized while designing input filter. Due to the selected filter inductance maximum converter voltage V_{cmax} is seen at maximum capacitive reactive power generation condition.Vcmax should be taken into account while determining filter capacitor voltage rating and power semiconductor voltage rating.

Another important criteria in filter design is transient response of the input filter. Transient response of the input filter affects overall transient response of CSC based STATCOM. Since the transfer function of the filter has a standart form of second order underdamped system settling time of the system can be defined as given in (3.9). If the damping ratio is decreased and corner frequency is increased settling time decreses and transient response of the system will be better.

$$settling \quad time, \quad t_s = \frac{4Q}{(\pi f_c)} \tag{3.9}$$

Depending on the mentioned filter design criterias, filter capacitance is decided to be 200uF/phase-delta and filter inductance is decided to be 300uH /phase. Corner frequency of the filter is calculted as 383 Hz . As can be seen in Figure 3.12 (70Arms) ac currents generated by SVPWM method in 6250Hz have very small lower order harmonic currents. Selected corner frequency is around 7^{th} harmonic but the effect of transformer lekage reactance reduces corner frequency around 5^{th}

harmonic. By the effect of active damping method sufficient attenuation around corner frequency is provided by using 1Ω damping resistor. As can be understood from Figure 3.12 higher order harmonics are attenuated succesfully by designed ac filter.

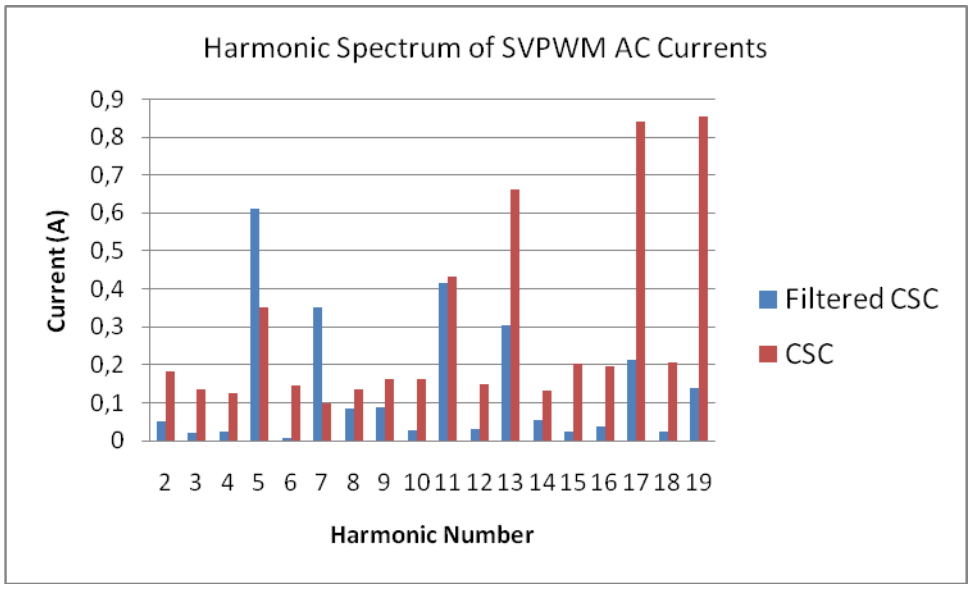


Figure 3.12 Harmonic Spectrum of Generated CSC Currents and Filtered CSC Currents

Reactive power of filter is calculated as 30kVAr capacitive at 400V. CSC Converter rated power is specified as ±70kVAr. Maximum capacitive reactive power generated by STATCOM is 100kVAr.

Table 3.5 Reactive Power Generation Limits of STATCOM

Input Filter	CSC	STATCOM
30 kVAr (cap.)	70 kVAr (cap.)	100 kVAr (cap.)
30 kVAr (cap.)	0 kVAr (cap.)	30 kVAr (cap.)
30 kVAr (cap.)	70 kVAr (ind.)	40 kVAr (ind.)

Maximum converter voltage at maximum capacitive generation condition is calculated as 423.56V given in (3.10).

$$Vc = 400V \pm \frac{100kVAr}{400V}(2\pi 50).300uH = 423.56V \tag{3.10}$$

While selecting filter capacitors calculated maximum voltage value should be taken into account. Also another critical parameter for capacitor selection is the internal inductance of the capacitor. It should be minimized in order to minimize total parasitic inductance value which causes voltage spikes during commutations. As mentioned in part 2.4 total parasitic inductances on a commutation path is multiplied by high *di/dt* value (rate of change of current) in order to calculate voltage spike value. 5×40uF low inductance (Electronicon [31]) capacitors are connected in order to obtain 200uF/phase-delta capacitance value. Each capacitor has 100nH inductance value and since they are connected in parallel inductance value is reduced to 20nH value. In power stage design part the effect of internal inductance will be explained in detail. 300uH filter reactor is selected as three phase iron core reactor.

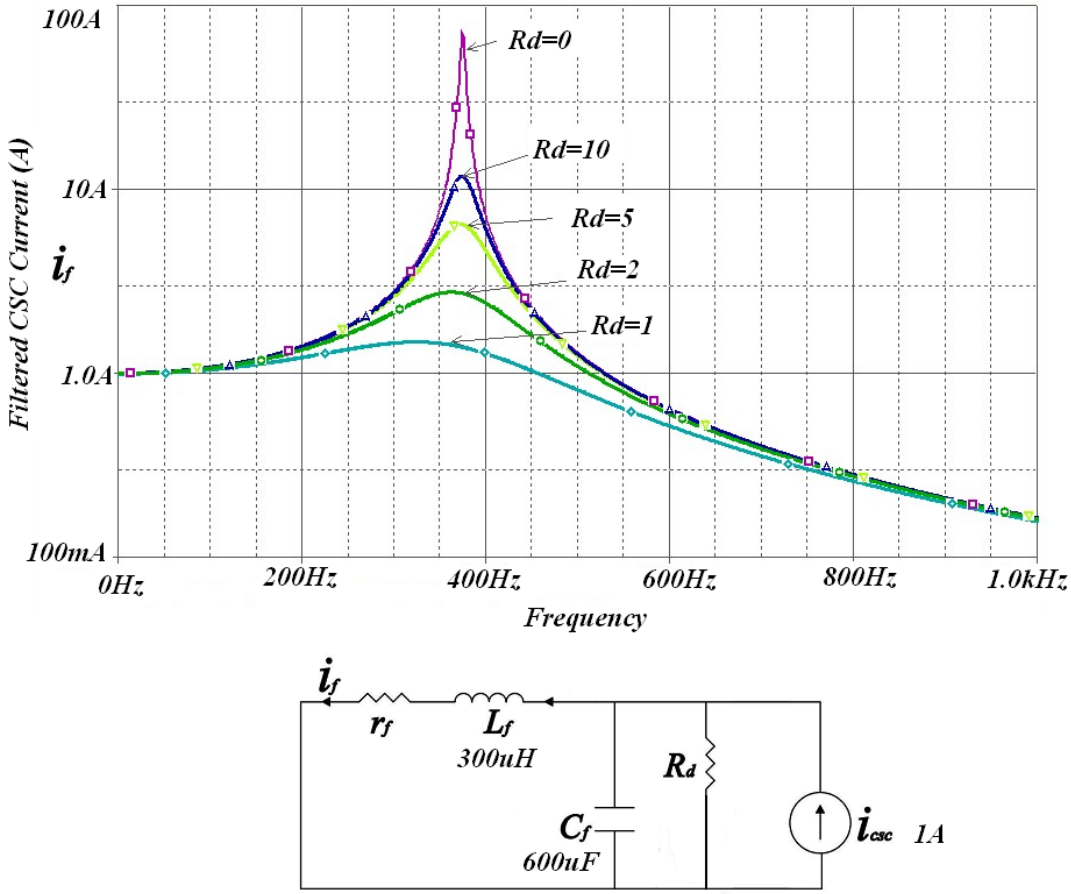


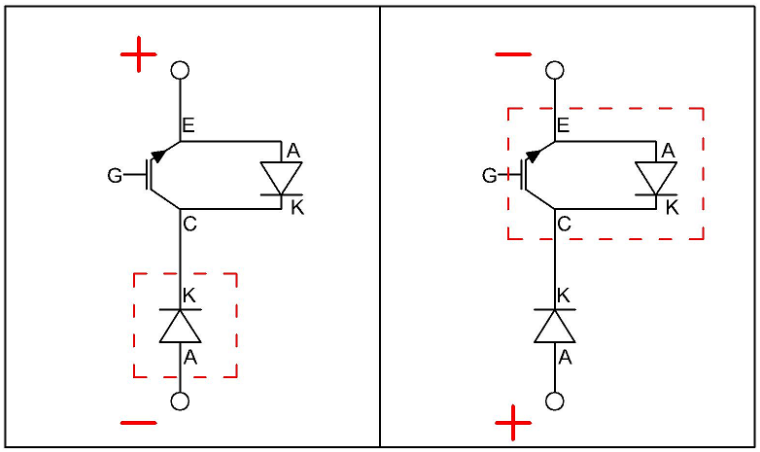
Figure 3.13 Frequency Response of Designed Input Filter

Frequency response of designed input filter with various damping resistor values can be seen in Figure 3.13. As mentioned in chapter 2.2.1.1 a small damping resistance is preferred for decreasing *Q* of the filter, thus minimizing the oscillations around corner frequency. On the other hand, unnecessarily small damping resistance makes the active damping loop gain too high such that the contribution of the damping current to the reference current becomes too high and the dc-link current and the reactive current control is lost.

As a result active damping resistance value is selected to be R_d=1.

3.6 Selection of Power Semiconductors

Power semiconductors are specified by voltage rating and voltage blocking capability, current carrying capacity and switching frequency limits. There are different type of commercial semiconductors are available in market. Thyristors, GTOs, IGCTs and IGBTs are the most common type of semiconductors. In this current source application SVPWM method is used and high switching frequency in high power applications can be applied only by using IGBT type semiconductor. In current source converter applications power semiconductor should have bipolar voltage blocking capability. Commercially available IGBTs cannot block reverse voltage. As can be seen in Figure 3.14 by using a series diode with IGBT, bipolar voltage blocking capability can be added. In Figure 3.14 (a) series diode can withstand applied voltage, and in Figure 3.14 (b) IGBT can withstand applied voltage. This type of semiconductor is called as symmetrical semiconductor.



(a) (b)

Figure 3.14 IGBT with series diode (a) Reverse blocking (b) Forward blocking

- **Voltage Rating:**

Semiconductor voltage rating should be higher than the maximum peak value of the converter input voltage (line-to-line). Maximum voltage condition is experienced if the supply voltage is increased to maximum permissible voltage limits, CSC STATCOM is in maximum capacitive reactive power generating mode and harmonic currents on filter inductance has an additional effect to voltage increase on converter side.

CSC STATCOM supply voltage is $400V_{l\text{-}l}$, it can change ±%10 within the permissible limits. As calculated in (3.10) in maximum capacitive reactive power generating mode converter voltage is increased due to the filter inductance value (300uH). As can be observed in Figure 3.12 converter generates 250Hz maximum %0,5 dominant current harmonic component. These three effects are added in order to calculate maximum converter voltage (3.11).

$$\hat{V} = \sqrt{2} \times (400V(1+0{,}1) + 300uH \frac{100kVAr}{400V} 2\pi(50Hz + 0{,}05 \times 250Hz)) = 655{,}28V \quad (3.11)$$

Maximum peak voltage on semiconductors are higher than calculated (3.11) converter voltage. As mentioned in part 2.4 during current commutations from one leg to other, outgoing semiconductors are subjected to voltage spikes due to high rate of change of current (*di/dt*) and parasitic inductances on commutation path. Voltage spike on voltage is calculated $\Delta V = L_{pt}.(di/dt)$. Considering additional voltage on semiconductors 1200V semiconductor voltage is selected to be on safe side.

- **Current Rating:**

CSC Converter reactive power is specified as ±70kVAr. As calculated in (3.12) and (3.13) phase current of CSC will be 141 A_{peak}. Dc-link current will be 150 A at steady-state conditions. This value is increased over 150A in transient-states. As mentioned in part 3.4 peak to peak ripple effects on dc-link current which is given by formula (3.7) should be considered.

As illustrated in Figure 2.21 during load commutation instances reverse recovery current of series diode is carried by semiconductor. Reverse recovery current should be added on steady state dc-link current in order to find peak value of current. Current rating of semiconductor is inversely related with switching frequency. SVPWM modulation frequency is specified as 6250Hz in previous parts.

$$I_{CSC\ rms} = \left[\frac{70kVAr}{400V * \sqrt{3}} \right] = 100A_{rms} \tag{3.12}$$

$$I_{CSC\ peak} = 100A_{rms} * \sqrt{2} = 141A_{peak} \tag{3.13}$$

As shown in Figure 3.15 operating frequency vs. collector current graphic of candidate semiconductor APTGF300U120DG, shows that when switching frequency is increasing collector current should be decreased while using same semiconductor device. In given graph selected frequency and current should be within hard switching area.

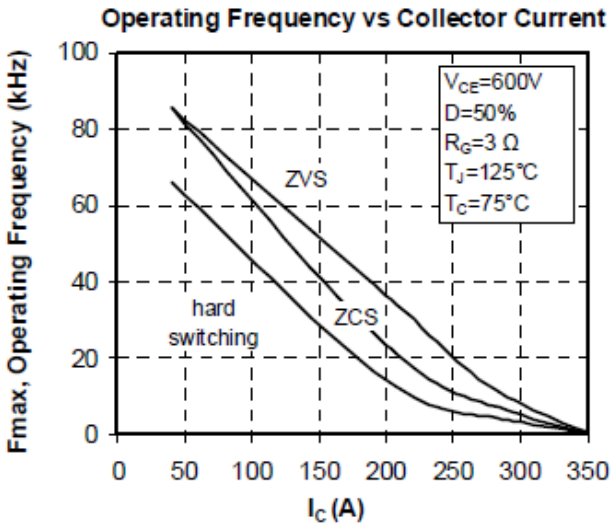


Figure 3.15 Operating Frequency vs. Collector Current of APTGF300U120DG

- **Diode Selection:**

  Additional series diode should be selected to make the device symmetrical (bidirectional voltage blocking) semiconductor. Voltage and current ratings of diode should be compatible with IGBT voltage and current ratings. Selected series diode should be fast recovery type, fast recovery type diodes are designed for use in applications requiring fast switching. Since the switching frequency is high in this application diode should turn on and turn off as fast as IGBT. As mentioned before since the reverse recovery current is added to dc-link current value during load commutation instances, also reverse recovery current of diode should be low. High reverse recovery currents cause high reverse recovery losses.

Voltage blocking specifications, current and frequency ratings are evaluated and candidate IGBT and diode is searched. SEMIKRON, MITSUBISHI, DYNEX, ABB, HITATCHI, IXYS, INFINEON and MICROSEMI are current semiconductor manufacturers. These manufacturers except MICROSEMI do not produce IGBT with series diode within same package. Only MICROSEMI produces IGBT with series diode in same package. As shown in Table 3.6 absolute maximum ratings of candidate IGBT APTGF300U120DG is given. It is decided to use MICROSEMI APTGF300U120DG IGBT for CSC STATCOM [32]. Internal structure of APTGF300U120DG is given in appendix C.

Table 3.6 Absolute maximum Ratings of APTGF300U120DG

Symbol	*Parameter*		*Max ratings*	*Unit*
V_{CES}	Collector - Emitter Breakdown Voltage		1200	V
I_C	Continuous Collector Current	$T_c = 25°C$	400	A
		$T_c = 80°C$	300	
I_{CM}	Pulsed Collector Current	$T_c = 25°C$	600	
V_{GE}	Gate – Emitter Voltage		±20	V
P_D	Maximum Power Dissipation	$T_c = 25°C$	1780	W
RBSOA	Reverse Bias Safe Operating Area	$T_j = 150°C$	600A @ 1200V	

3.7 Design of Power Stage

Power stage design of CSC STATCOM is composed of two stages; electrical connections and mechanical connections of used circuit components.

Electrical Connections:

As illustrated in Figure 3.16 six semiconductor switches are connected to AC and DC side of the circuit by colored connections and L_p means parasitic inductance of these connections.

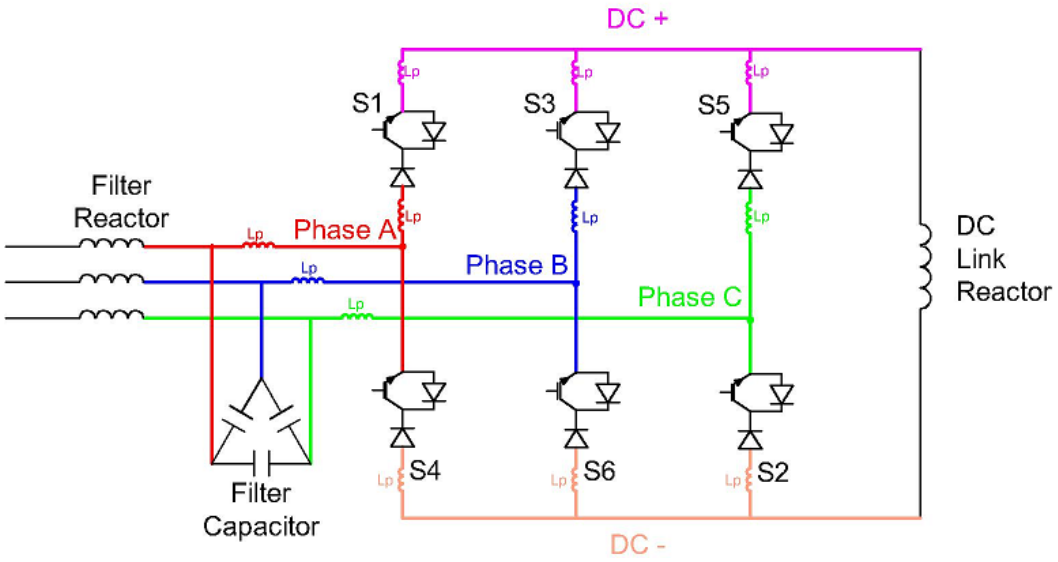


Figure 3.16 CSC STATCOM Circuit Electrical Connections

As indicated in Figure 3.17 and (3.14) switching of power semiconductors causes voltage overshoots because of these parasitic inductances present in the circuit.

$$\Delta V = \mathrm{L_p}(total) \times \frac{di}{dt} \tag{3.14}$$

These voltage overshoots are seen across the power semiconductors during commutations between semiconductor switches and it must be verified that the maximum permissible blocking voltage of the power semiconductor is never exceeded.

In order to minimize parasitic inductances, commutation path length and area inside the commutation path which can be seen in Figure 3.17 should be minimized, filter capacitors should be low inductance special power electronic capacitors and distance between semiconductor switches should be minimized.

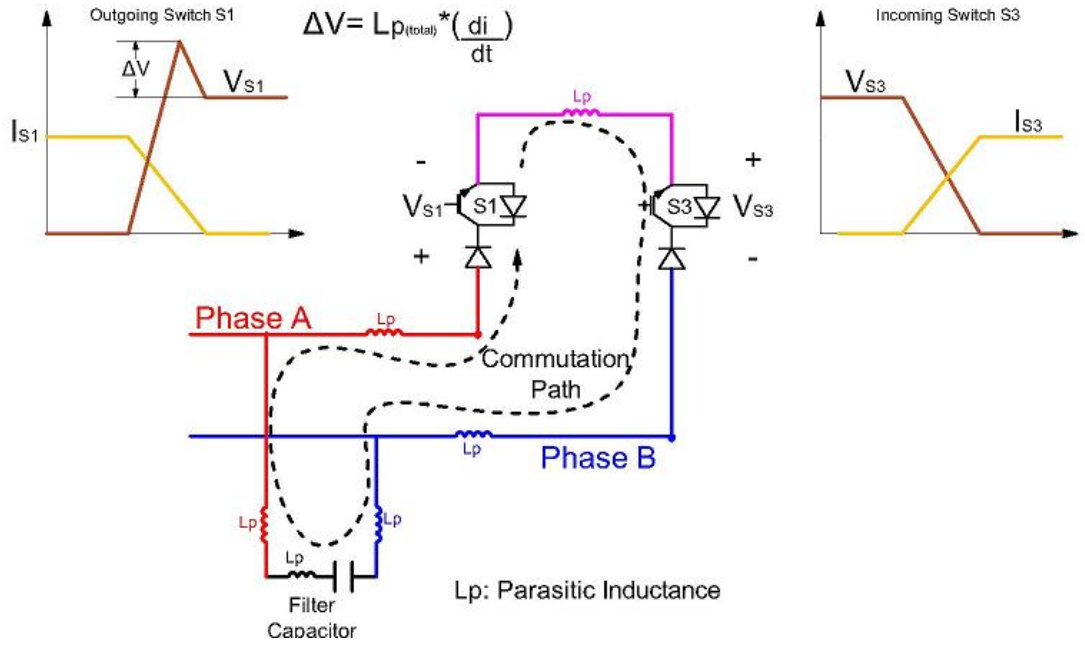


Figure 3.17 Commutation Path between S1 and S3

This is achieved by using laminated type bus bar to make phase A, phase B, phase C connections. Dc-link connections should not be laminated type because by using laminated type connections at dc+ and dc- terminals capacitance of dc-link increases, high *dv/dt* voltage changes on dc-link may cause current distortions on dc-link. In

order to minimize dc-link capacitance dc+ and dc- terminals should be as far as possible to each other. As can be seen in Figure 3.18 5×40uF filter capacitors are connected in parallel between each phase for delta connection. Each capacitor has 100nH self inductance and by connecting five capacitors in parallel total inductance value can be reduced to 20nH, also in order to minimize commutation path and reduce commutation path total parasitic inductance 3uF snubber capacitors are connected close to semiconductor terminals.

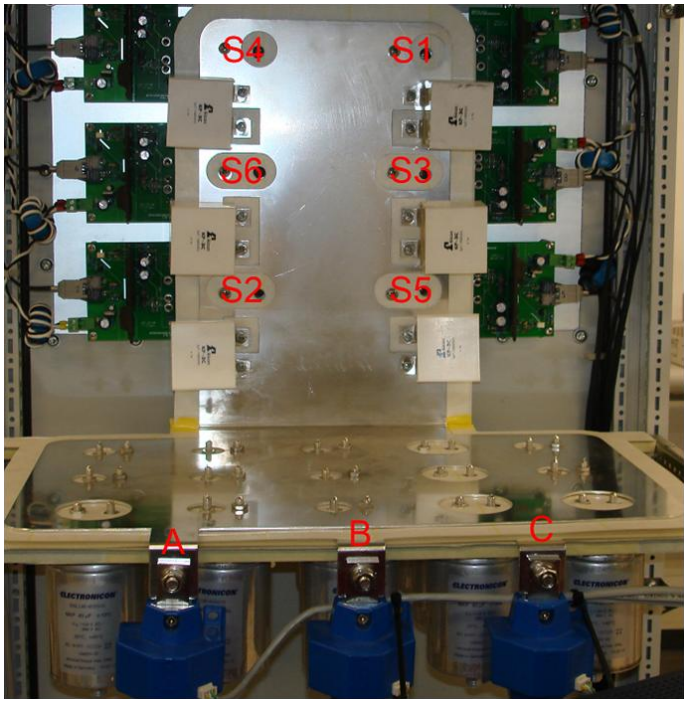
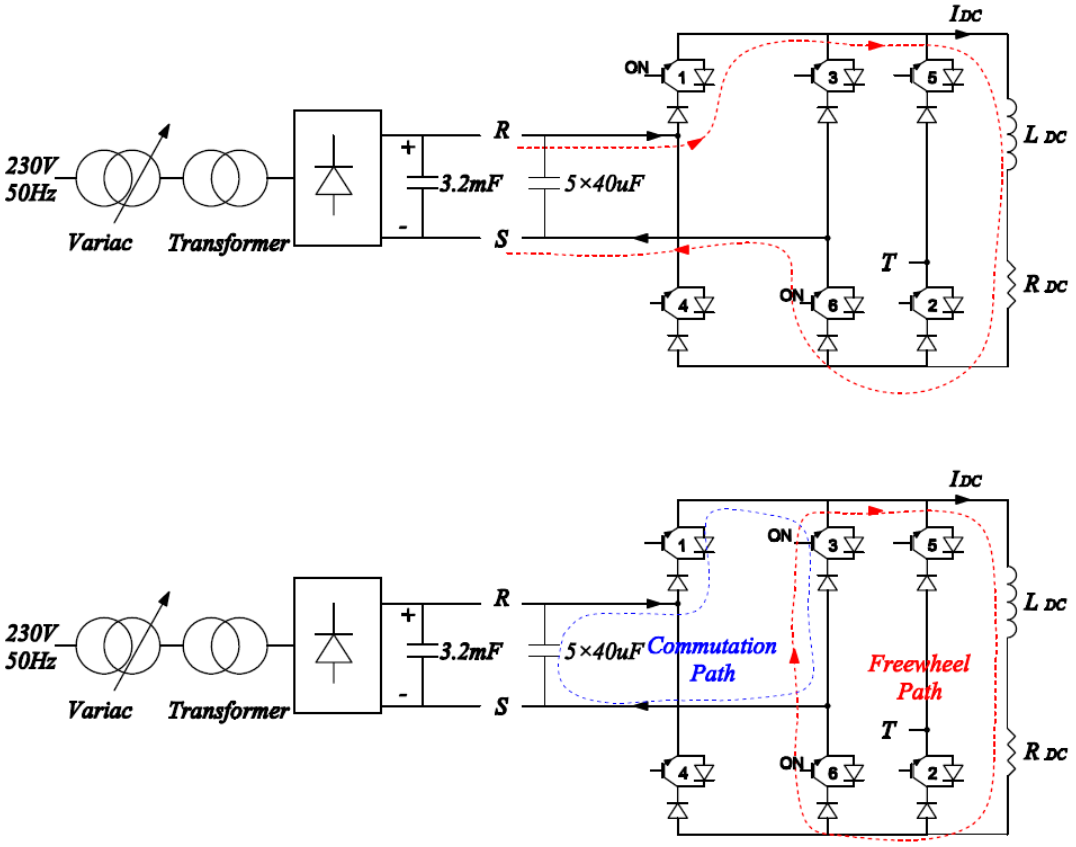


Figure 3.18 Power Stage of CSC STATCOM

Switching tests are applied to each commutation path to measure parasitic inductances and voltage spikes over semiconductor terminals. Switching test setup is illustrated in Figure 3.19. 600V dc voltage is applied between line-to-line terminals and R_{DC}=2,5Ω is connected to dc-link in order to limit current to 125A. Effect of parasitic inductances on semiconductor voltages is illustrated in Figure 3.17. Calculated parasitic inductance values are given in Table 3.7.



TEST SETUP MEASUREMENT DEVICES	
Current Probe	Powertek, Rogowski Current Transducers CWT 15B
Voltage Probe	Tektronix P5210 High Voltage Differential Probe
Scope	Tektronix TDS5054 Digital Phosphore Oscilloscope

Figure 3.19 Switching Test Setup

Table 3.7 Commutation Path Parasitic Inductances

Commutation Path	Total Parasitic Inductance	Commutation Path	Total Parasitic Inductance
V_{RS} Top	108 nH	V_{RS} Bottom	110 nH
V_{ST} Top	108 nH	V_{ST} Bottom	100 nH
V_{RT} Top	150 nH	V_{RT} Bottom	150 nH

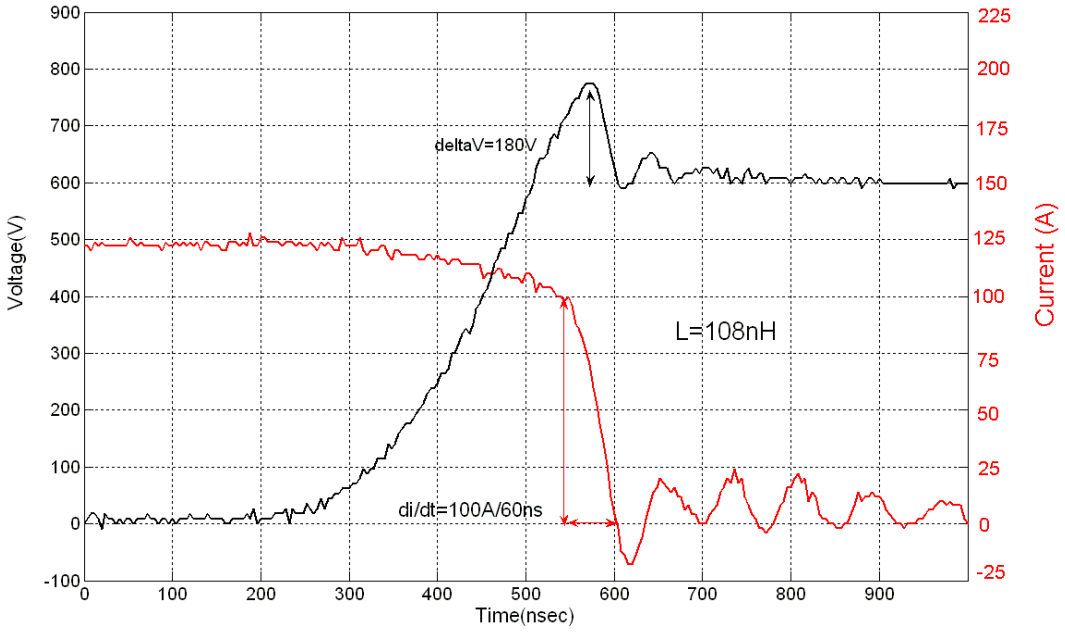


Figure 3.20 S1 Turn-off Voltage & Current (V_{RS} Top Commutation Path)

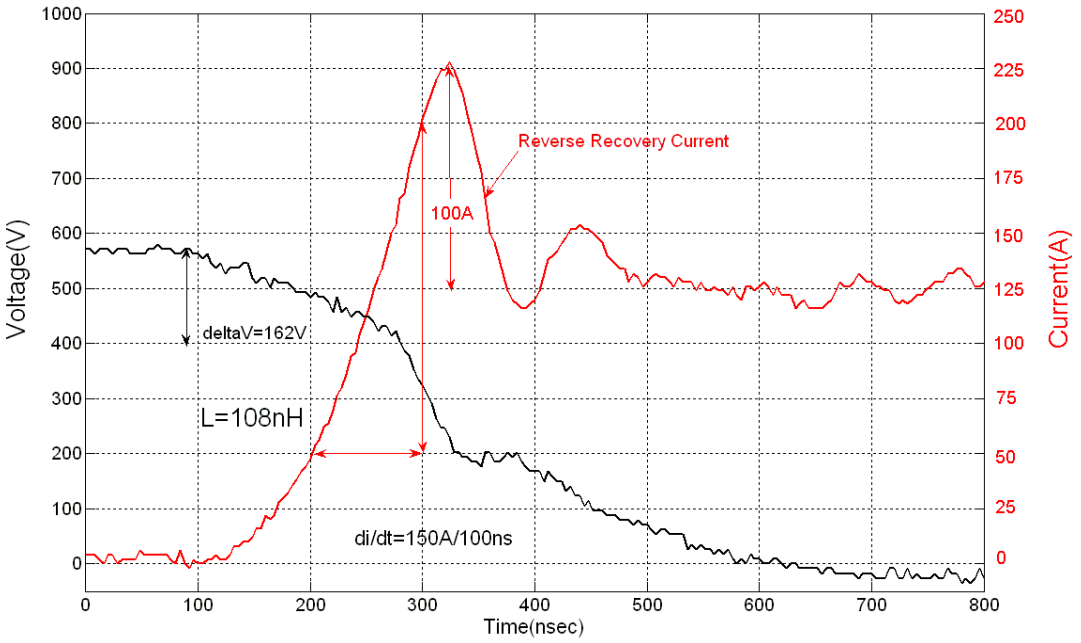


Figure 3.21 S1 Turn-on Voltage & Current (V_{RS} Top Commutation Path)

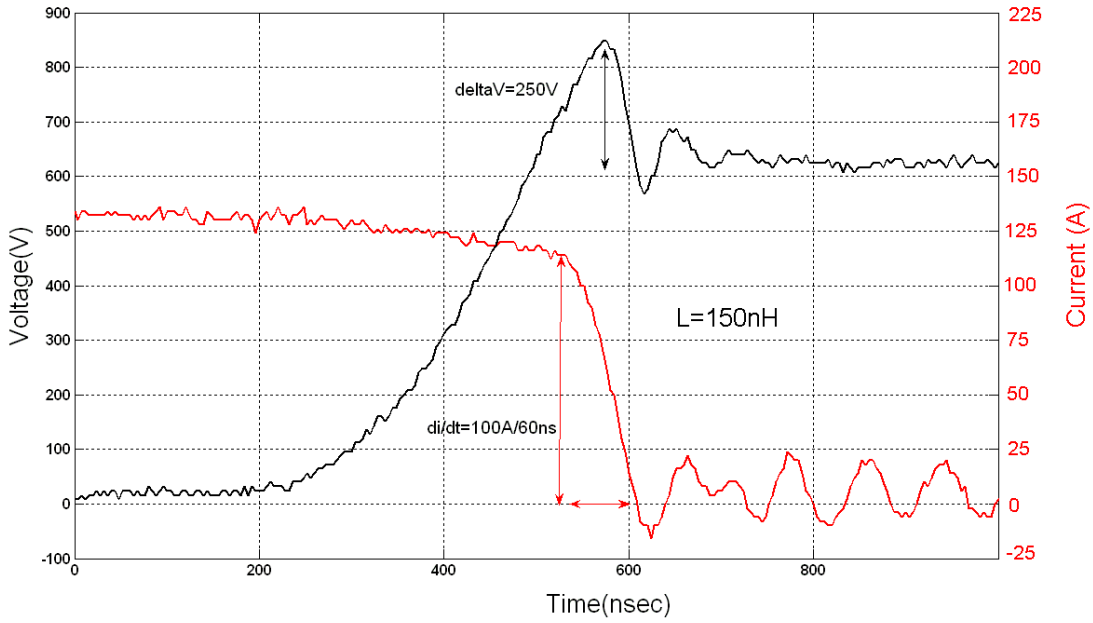


Figure 3.22 S1 Turn-off Voltage & Current (V_{RT} Top Commutation Path)

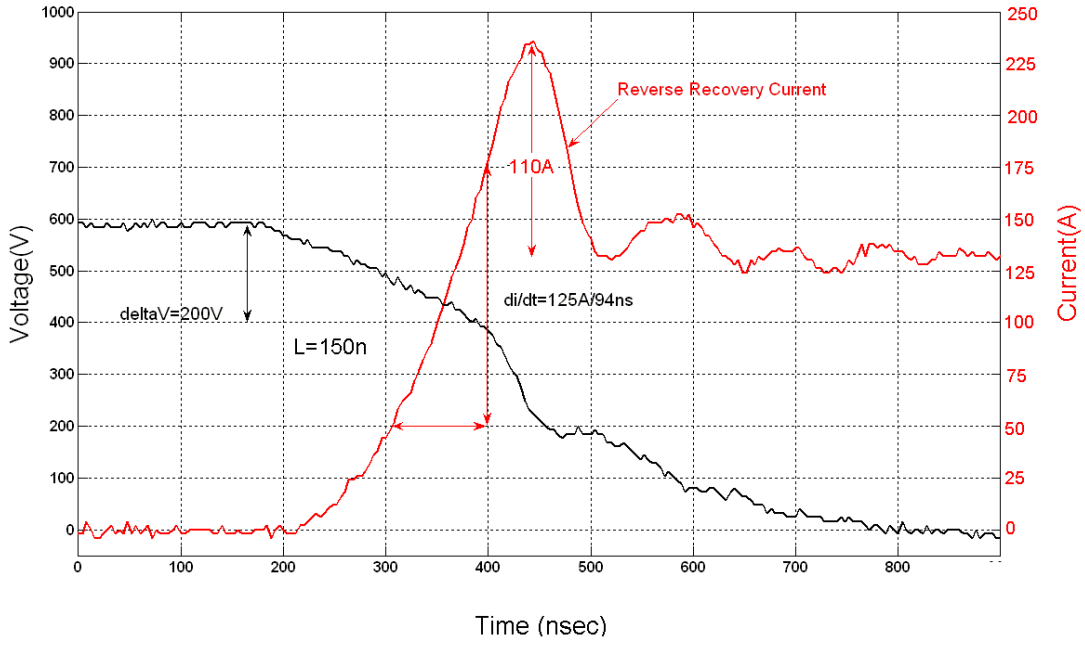


Figure 3.23 S1 Turn-on Voltage & Current (V_{RT} Top Commutation Path)

Measurement results for V_{RS} top commutation path and V_{RT} top commutation path are given in Figure 3.20, Figure 3.21, Figure 3.22 and Figure 3.23. Commutation path inductance of V_{RT} top commutation path is 150nH and V_{RS} top commutation path is 108nH. The commutation path length of V_{RT} is longer than V_{RS} and this causes increase in inductance value.

3.8 Design of Control System

Principles of current control are described and block diagrams of the proposed control method are given in detail in chapter 2. In order to implement current control techniques which is given in Figure 2.13 , digital control system is designed by employing eZDSP TMS320F28335 [33]. Control system is composed of five sub-units as can be seen in Figure 3.24.

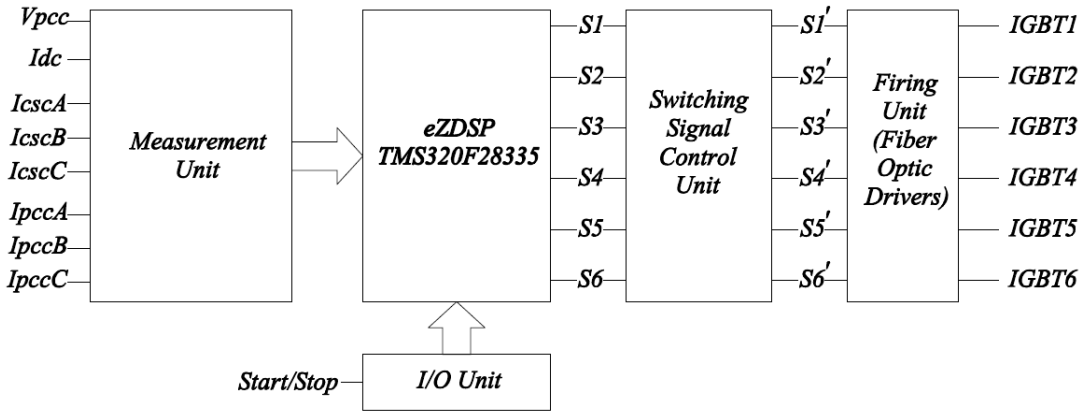


Figure 3.24 Control System Sub Units

- Measurement unit of control system collects voltage and current data which are sent by voltage and current transducers of the system. Collected analog signals are converted to proper voltage levels which can be processed by the analog to digital converter of the DSP unit.

- I/O (input/output) unit of the control system receives and sends interface signals such as start/stop and circuit breaker contact position and it isolates external signals from DSP by using optocouplers.
- EZDSP TMS320F28335 unit receives input data coming from measurement unit and I/O unit. All the received analog voltage and current signals are converted to digital signals and processed digitally by digital signal processor of EZDSP TMS320F28335 unit. Switching signals are generated and send to switching signal control unit.
- Switching signal control unit add overlap times to switching signals and generates freewheel signals under fault conditions. During current commutations from one switch to another overlap times should be enough for commutation time period.
- Finally controlled switching signals are sent to IGBT driver cards by firing unit. Firing unit is composed of fiber optic drivers and signals are sent optically in order to isolate power stage from control units.

3.9 Summary

In this chapter design principles of CSC STATCOM have been presented. In this design method, firstly modulation technique is selected by evaluating harmonic performance and switching frequency values of different on-line PWM techniques, secondly dc-link reactor is selected by using the switching frequency, reactance value versus dc current peak to peak ripple graph. After selecting modulation technique, switching frequency and dc-link inductance value, input filter is designed in order to filter current harmonics which are generated by current source converter.

Since the voltage, current and frequency ratings are important in semiconductor selection, limit voltage and current values are calculated by using designed dc-link inductance and input filter parameters. After selection of semiconductor switches design of power stage is explained and laboratory switching test results for the

designed power stage are presented. Finally designed control system is described briefly.

In the next chapter experimental results of designed laboratory prototype will be presented.

CHAPTER 4

EXPERIMENTAL RESULTS

4.1 Introduction

Using the design principles given in chapter 3, +/- 70kVAr CSC based STATCOM has been developed at 400V. SVPWM method is used as modulation technique at 6250Hz and the proposed control system in Fig.2.17 is applied to the prototype.

The laboratory tests are performed at 200V and +/- 17kVAr for different operating conditions. Various characteristics of CSC based STATCOM have been obtained. The records have been obtained by the measuring apparatus, which are listed in Table 4.1 .

Table 4.1 List of Measurement Devices

Oscilloscope 1	Tektronix TDS5054 Digital
Oscilloscope 2	LeCroy WaveJet 324
High Voltage Differential Probe	Tektronix P5210 (50MHz)
Passive Voltage Probe 1	Tektronix P5050 (500MHz)
Passive Voltage Probe 2	Tektronix PMK PHV1000 (400MHz)
Current Probe	Powertek, Rogowski Current Waveform Transducers CWT 15B, 2mV/A
Current Transducer	LEM LA255-T

The complete circuit diagram of the developed CSC STATCOM is given in Figure 4.1 and the component list is given in Table 4.2. Front and back view of laboratory prototype is given in Figure 4.2.

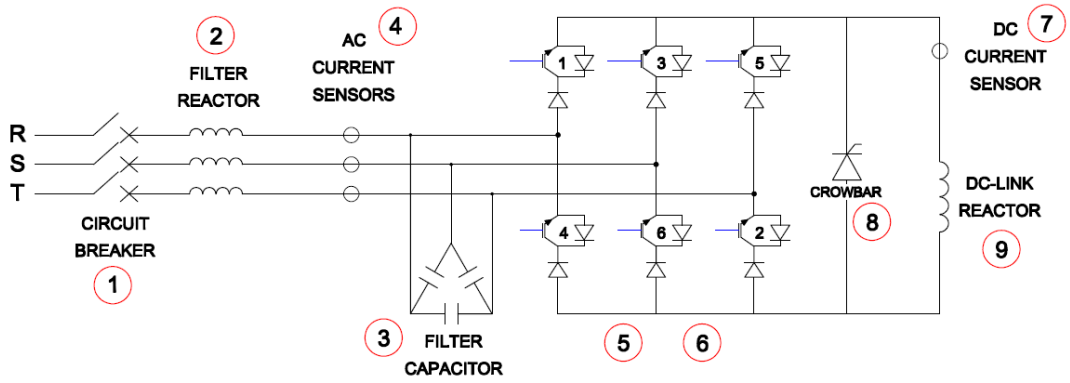


Figure 4.1 CSC STATCOM Circuit

Table 4.2 CSC STATCOM Component List

NO	COMPONENT	FEATURE
1	Circuit Breaker	ABB 400V, In=400A
2	AC Filter Reactor	300uH (Iron core)
3	AC Filter Capacitor	5×40uF (200uF/delta)
4	AC Current Sensor	LEM 200Arms
5	IGBT Driver & IGBT	VLA500-01R & APTGF300U120DG
6	Laminated Bus Bar	2mm Copper Plate
7	DC Current Sensor	LEM 250Arms
8	Crowbar Circuit and Thyristor	IXYS MCC 162-14
9	DC-Link Reactor	2 mH (Iron core)
10	Heat Sink (Air Cooler)	AUSTERLITZ KS 300-14
11	Cooler Fan	EBMPAPST D2E160

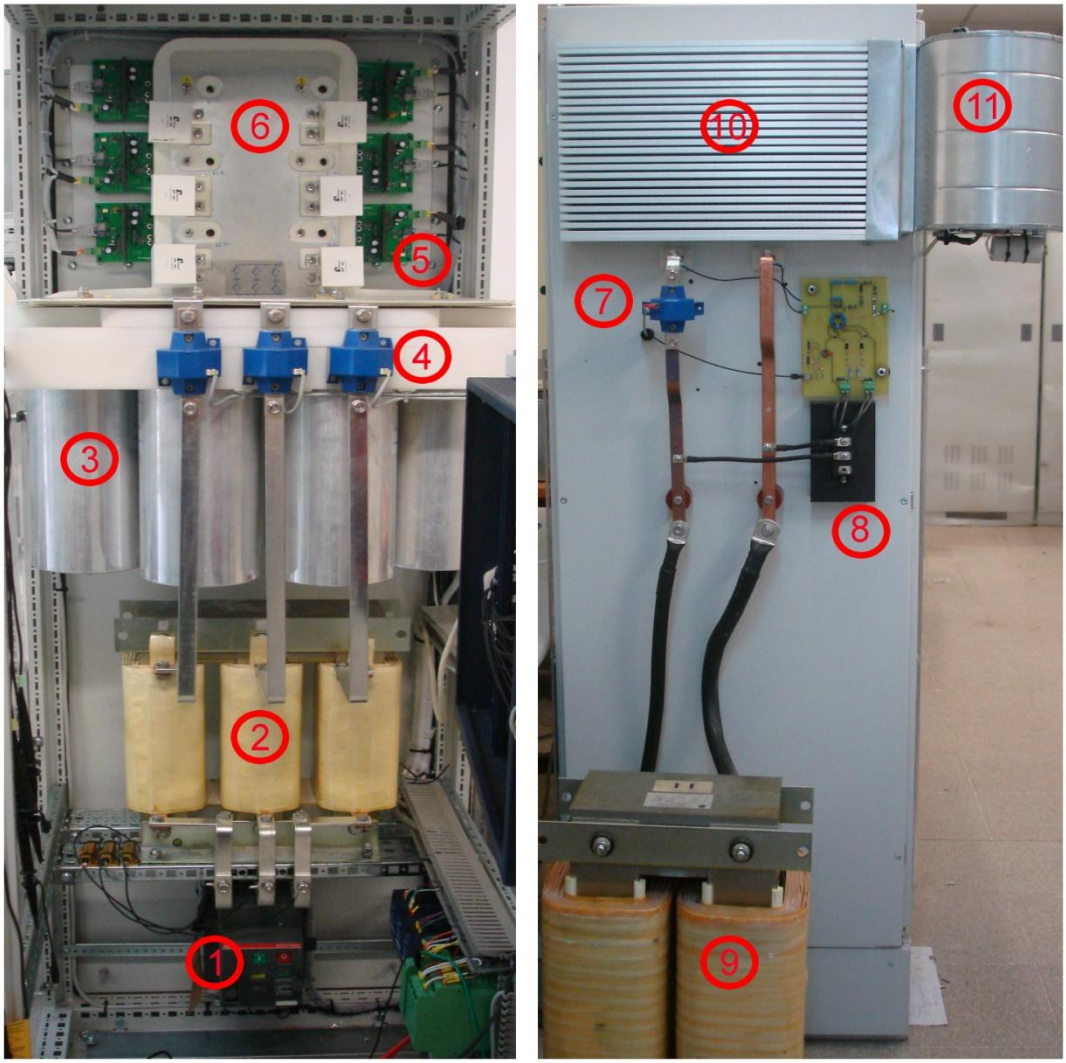


Figure 4.2 CSC STATCOM Front and Back view

The list of designed control system electronic cards is given in Table 4.3 and front and back view of the control system cards is given in Figure 4.3.

Table 4.3 List of Control System Cards

NO	CARD NAME
1	DSP_MU (Measurement Unit Card)
2	DSP Card (EzDSP TMS320F28335)
3	DSP-LCU (Logic Control Unit Card)
4	DSP-OCU (Opto Coupler Unit Card)
5	DSP – FOU (Fiber Optic Unit Card)

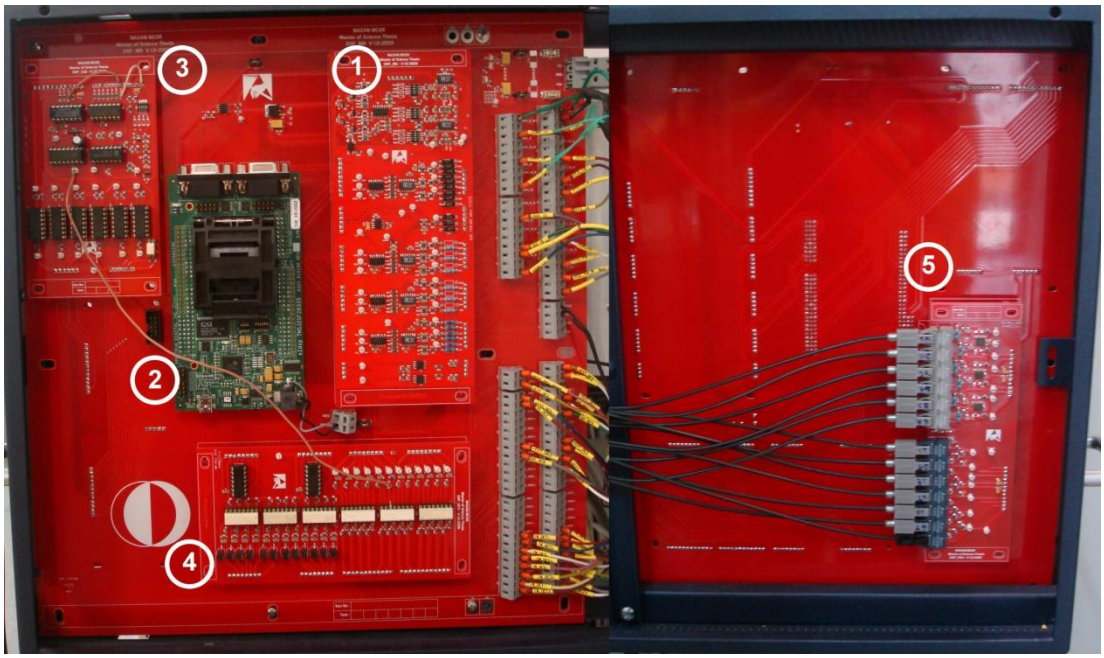


Figure 4.3 Electronic Control System Front and Back View

4.2 Experimental Results

4.2.1 Current and Voltage Waveforms of Power Semiconductors

Current and voltage waveforms of IGBT1 and IGBT5 have been recorded by the use of Rogowski coils (RC1 and RC2) and Tektronix P5210 high voltage differential probes (HV1 and HV2) as illustrated in Figure 4.4. Two sample records, one for 17kVAr capacitive and the other for 17kVAr inductive reactive power generation of overall STATCOM are given in Figure 4.5 and Figure 4.6 respectively for one cycle (20msec).

The voltage and current waveforms of IGBT1 and IGBT5 during load commutation are given in Figure 4.7 and voltage and current waveforms during forced commutation are given in Figure 4.8. The waveforms are in consistent with the description of commutation types in chapter 2.4.

Supply voltage is 200V line-to-line and dc-link current is 120A during commutation instances.

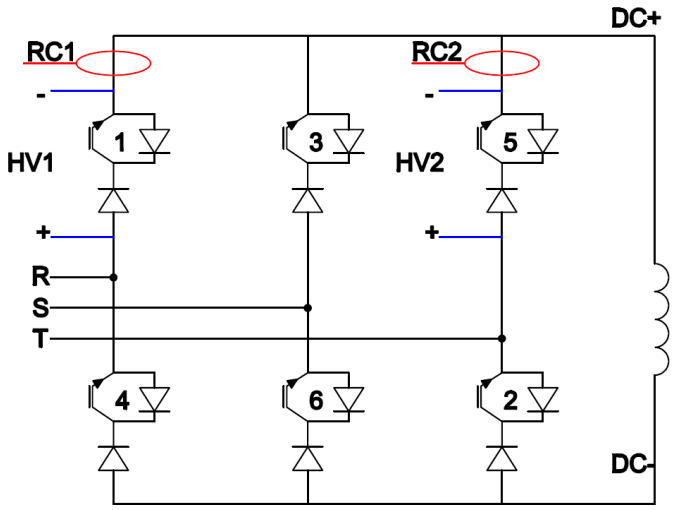


Figure 4.4 Power Semiconductor Current & Voltage Measurement Set-up

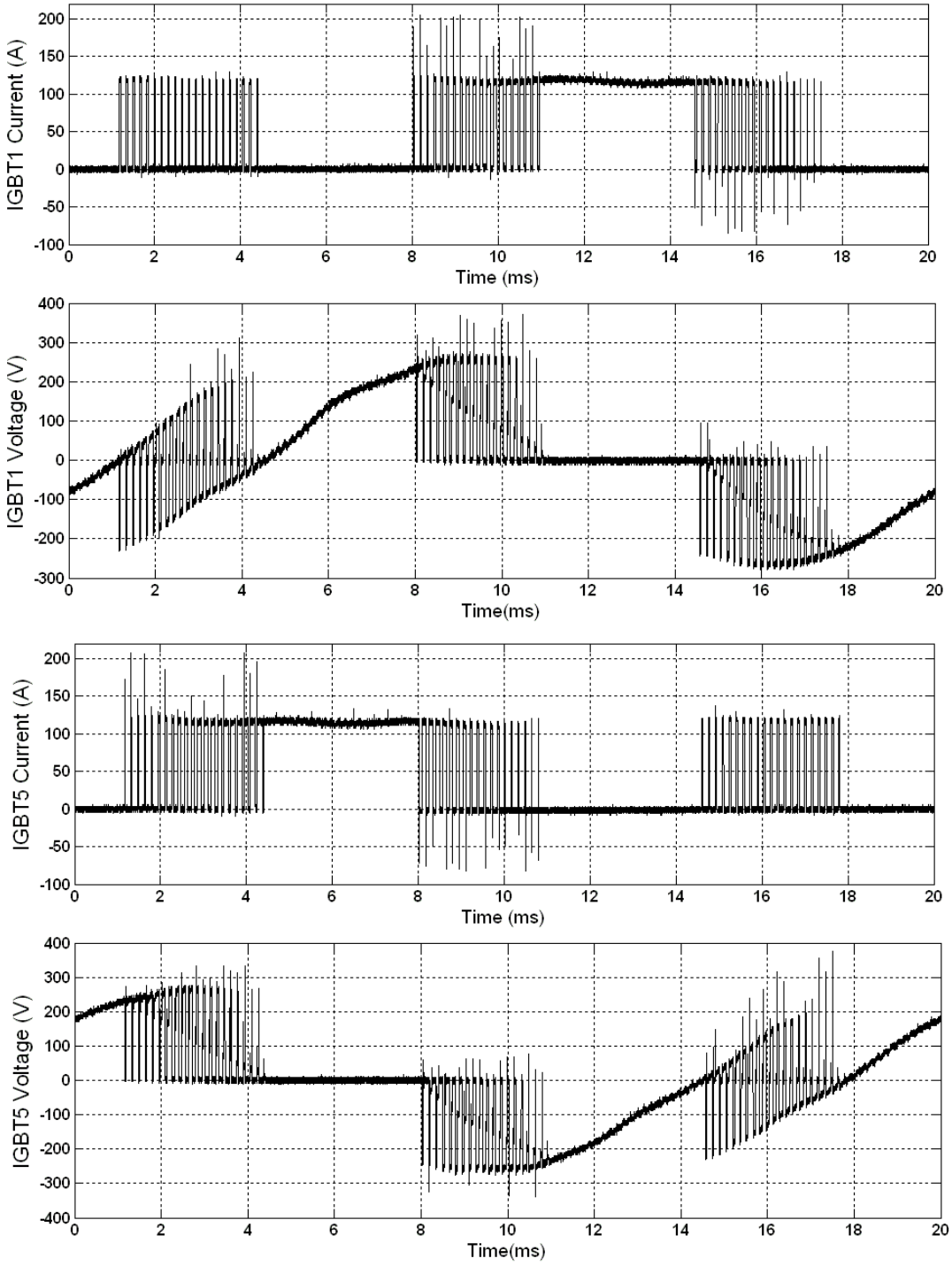


Figure 4.5 Voltage and Current Waveforms of IGBT1 and IGBT5 for 17kVAr Capacitive Reactive Power Generation of STATCOM (sampling rate=5 MS/s)

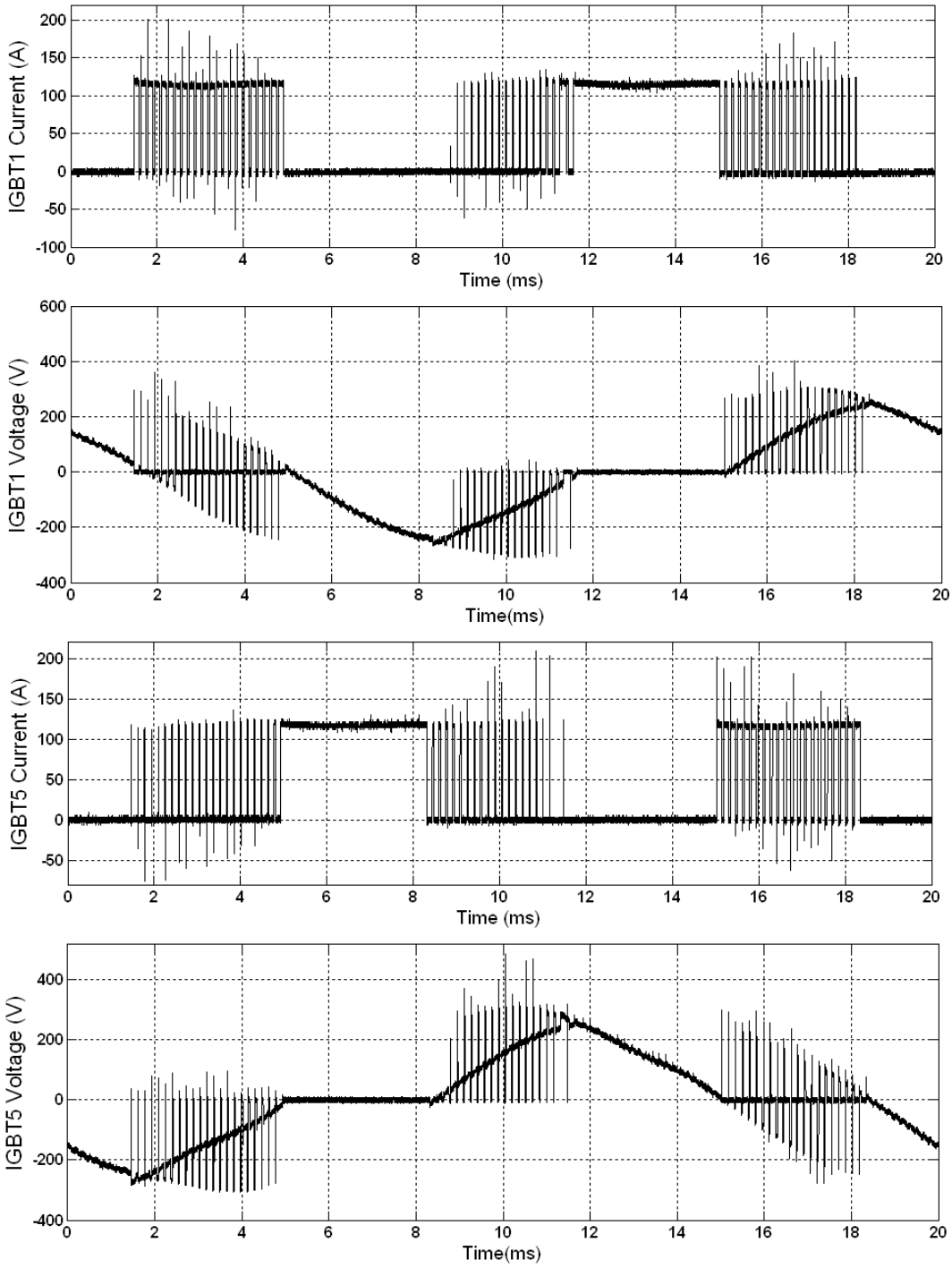


Figure 4.6 Voltage and Current Waveforms of IGBT1 and IGBT5 for 17kVAr Inductive Reactive Power Generation of STATCOM (sampling rate=5 MS/s)

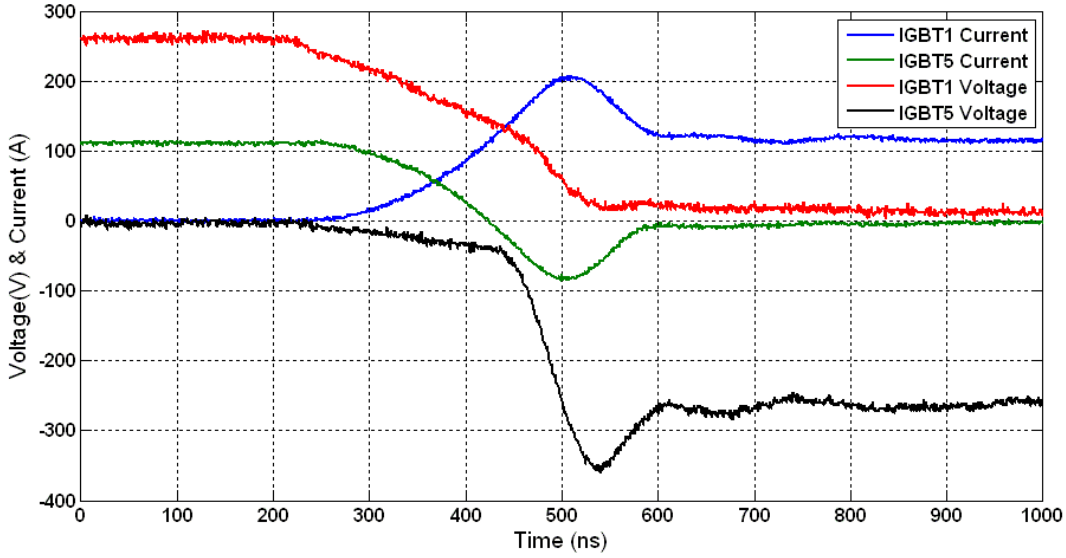


Figure 4.7 Voltage and Current Waveforms of IGBT1 and IGBT5 during Load Commutation (sampling rate=25GS/s)

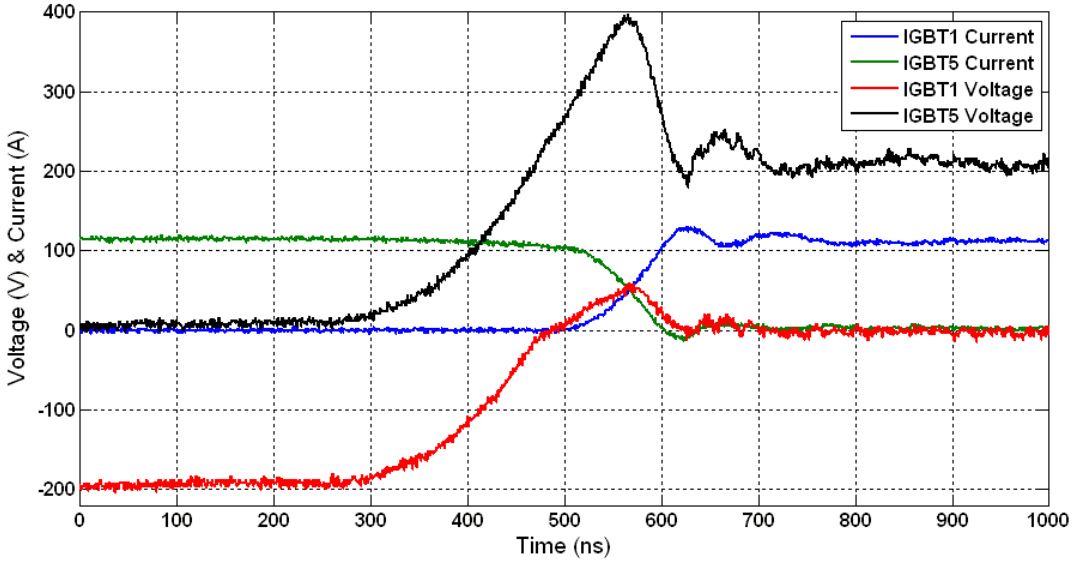


Figure 4.8 Voltage and Current Waveforms of IGBT1 and IGBT5 during Forced Commutation (sampling rate=25GS/s)

4.2.2 AC Side Voltage and Current Waveforms

Converter current (i_R) and filtered converter current (i_{RF}) waveforms have been recorded by the use of Rogowski coils (RC1 and RC2) and phase to phase voltage of converter has been recorded by using Tektronix P5210 high voltage differential probes (HV1) as illustrated in Figure 4.9. Two sample records, one for 17kVAr capacitive and the other for 17kVAr inductive reactive power generation of overall STATCOM are given in Figure 4.10 and Figure 4.12 respectively for 40msec.

In Figure 4.10 and Figure 4.12 converter currents generated by SVPWM method at 6250 Hz contain pulses, which are filtere out by filter capacitors. Filtered converter currents are nearly sinusoidal.

Converter voltage V_{ST} is higher than supply voltage at capacitive mode of operation and it is lower in inductive mode of operation.

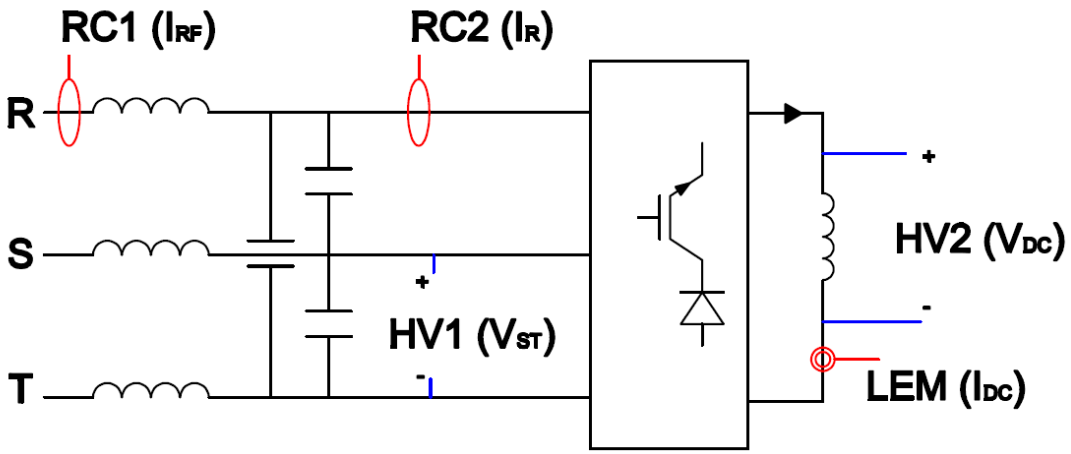


Figure 4.9 Current & Voltage Measurement Set-up

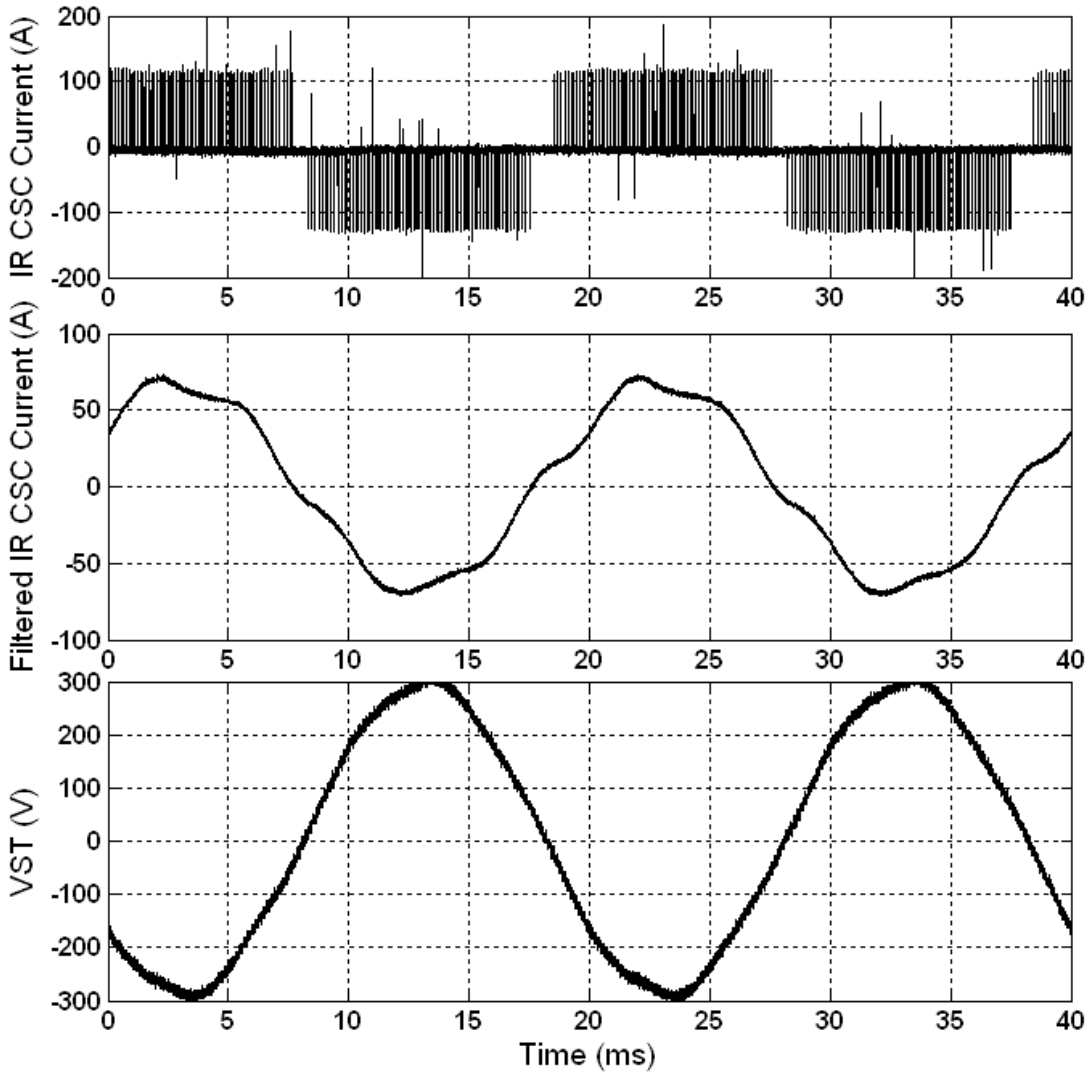


Figure 4.10 Voltage and Current Waveforms of Converter Current I_R, Filtered Converter Current and Phase-to-phase Voltage V_{ST} for 17kVAr Capacitive Reactive Power Generation of STATCOM (sampling rate=2.5MS/s)

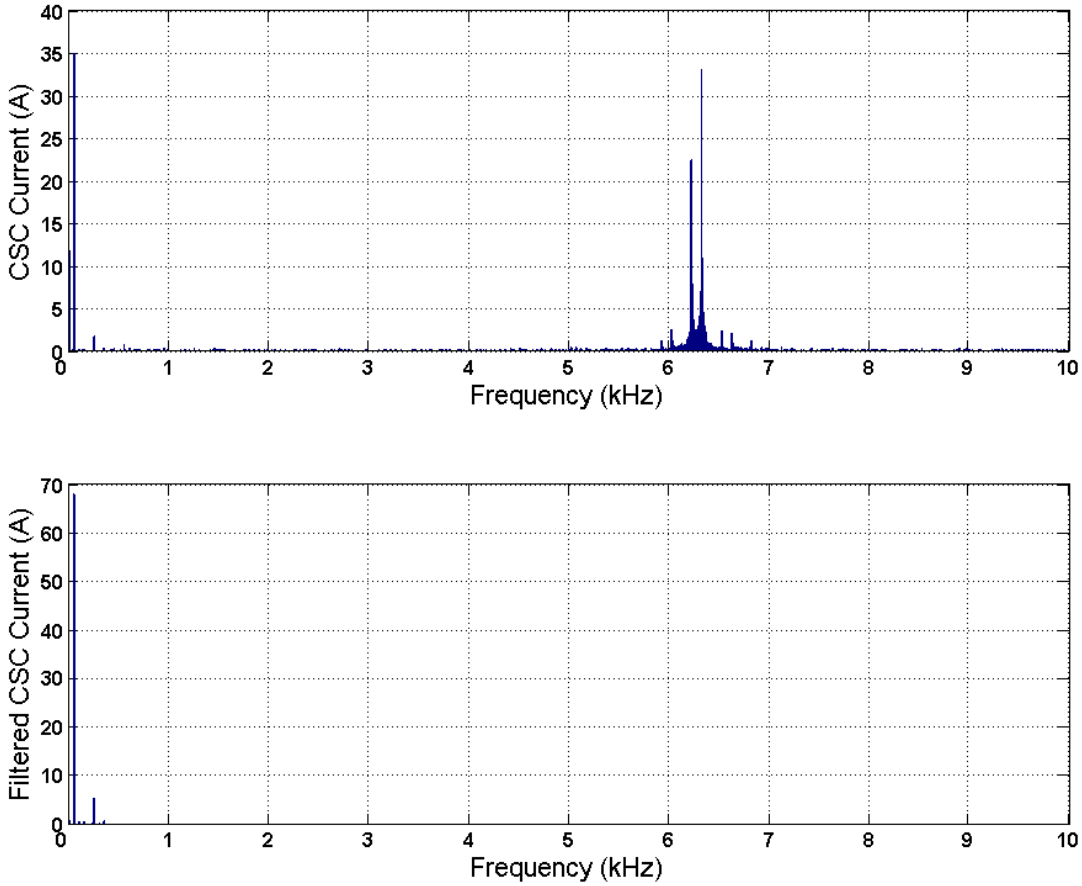


Figure 4.11 Harmonic Spectrum of Converter Current I_R and Filtered Converter Current for 17kVAr Capacitive Reactive Power Generation of STATCOM

Table 4.4 Lower order Harmonics of Converter Current I_R and Filtered Converter Current for 17kVAr Capacitive Reactive Power Generation of STATCOM and Limit Values Recommended by IEEE Std. 519-1992

Harmonic Number	CSC Current (A)	STATCOM Current (A)	Harmonic Current / Fundamental Current	Limit recommended by IEEE Std. 519-1992
1	34,87	67,76		I_{Sc}/I_L
3	0,21	0,70	% 1	%4
5	1,73	5,55	%8	%4
7	0,41	0,78	% 1	%4
11	0,78	0,10	% 0,1	%2
13	0,18	0,06	% 0,1	%2

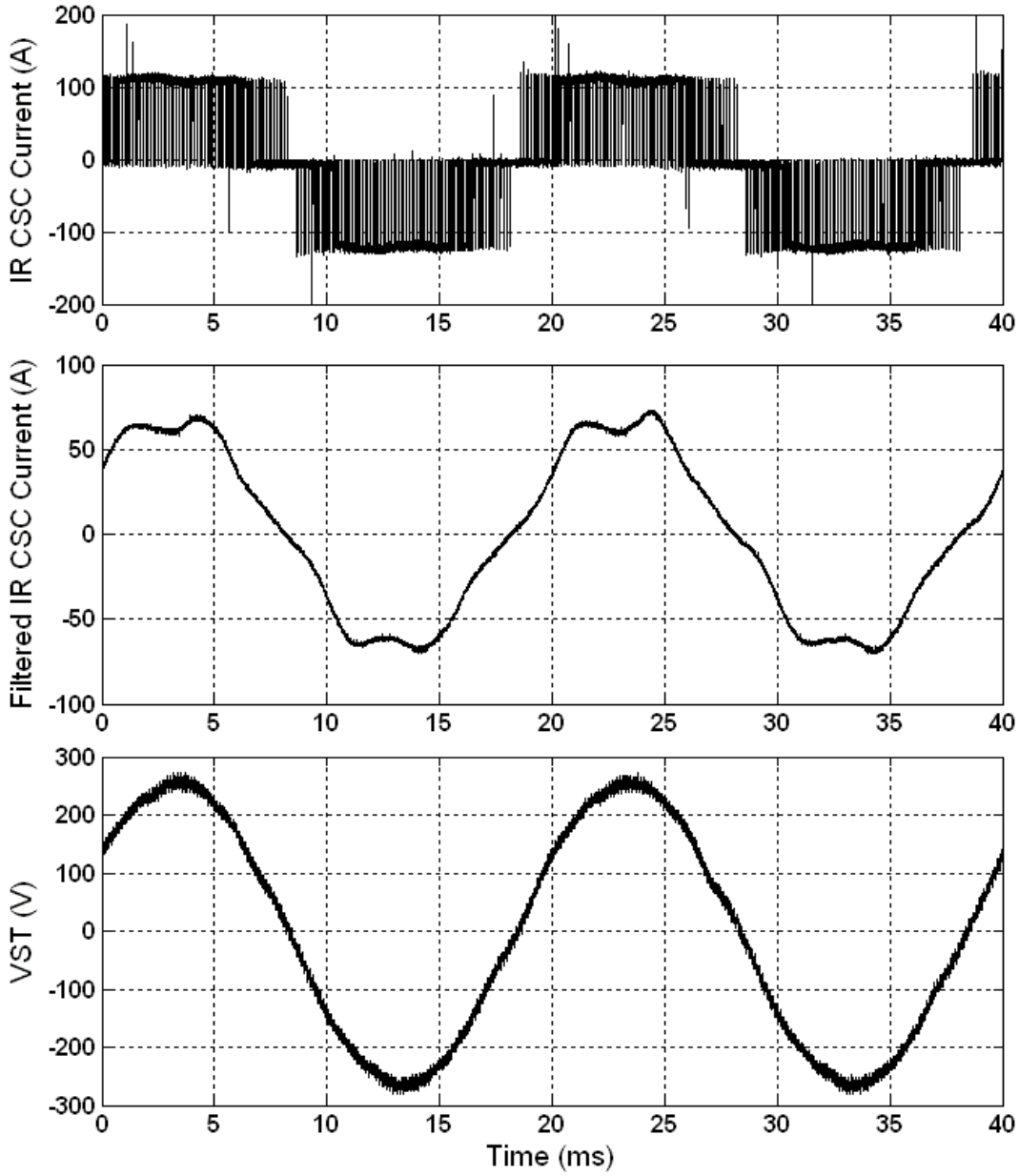


Figure 4.12 Voltage and Current Waveforms of Converter Current I_R, Filtered Converter Current and Phase-to-phase Voltage V_{ST} for 17kVAr Inductive Reactive Power Generation of STATCOM (sampling rate=2.5MS/s)

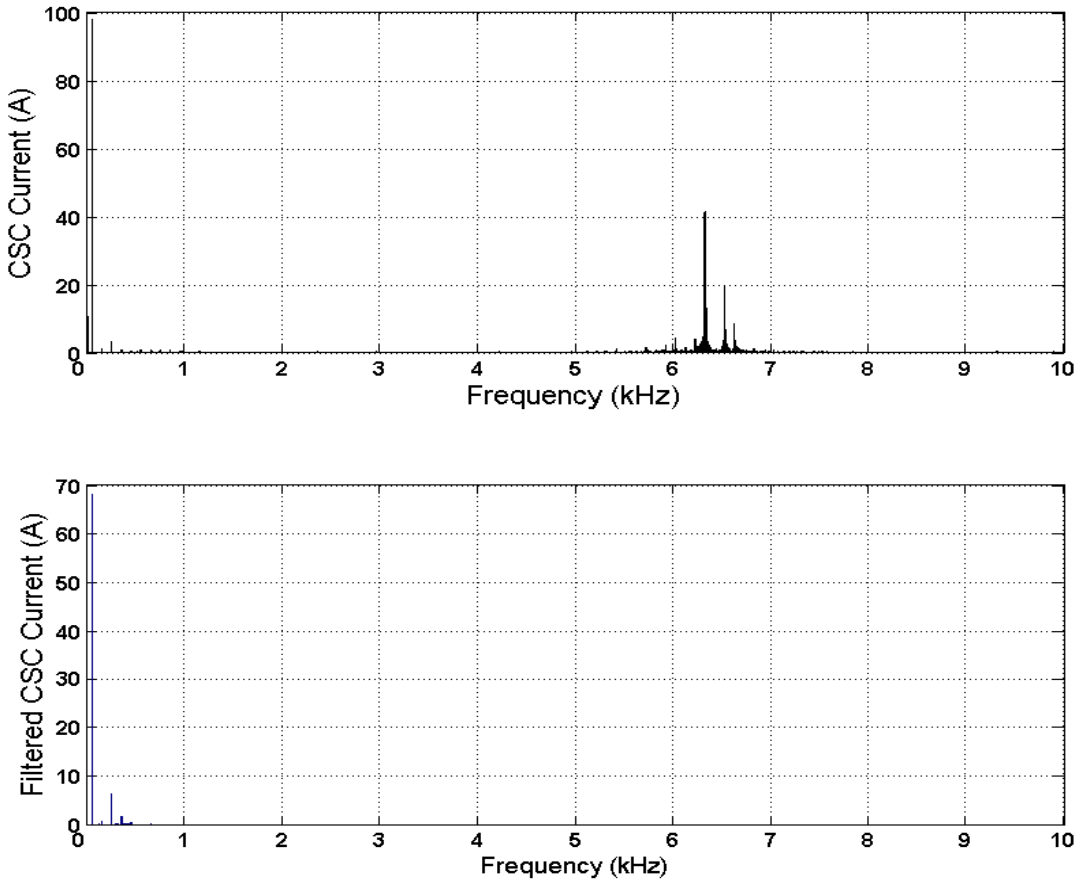


Figure 4.13 Harmonic Spectrum of Converter Current I_R and Filtered Converter Current for 17kVAr Inductive Reactive Power Generation of STATCOM

Table 4.5 Lower order Harmonics of Converter Current I_R and Filtered Converter Current for 17kVAr Inductive Reactive Power Generation of STATCOM and Limit Values Recommended by IEEE Std. 519-1992

Harmonic Number	CSC Current	Filtered CSC Current (A)	Harmonic Current / Fundamental Current	Limit recommended by IEEE Std. 519-1992
1	97,71	67,83		I_{SC}/I_L
3	1,06	0,96	% 1	%4
5	3,27	6,42	%9	%4
7	0,95	1,95	% 3	%4
11	0,94	0,22	% 0,3	%2
13	0,96	0,37	% 0,5	%2

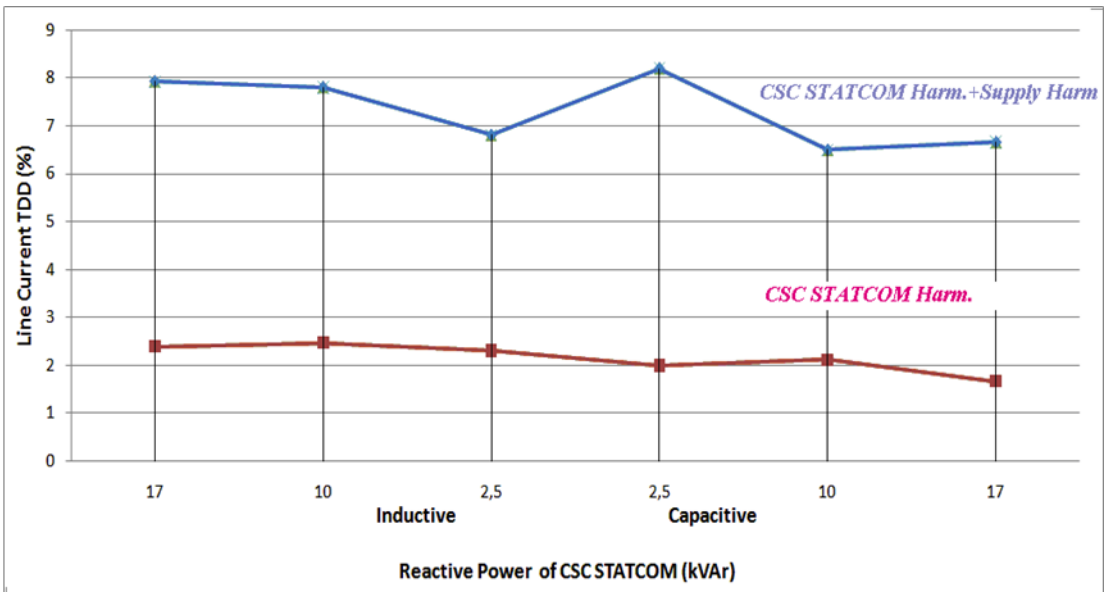


Figure 4.14 Variations in TDD of CSC based STATCOM line current

Harmonic spectrum of converter currents are given in Figure 4.11 and Figure 4.13.

It can be seen that designed low pass LC input filter, filters harmonic currents around 6250 Hz (switching frequency) and by active damping method current amplification around corner frequency can be damped succesfully. In Table 4.4 and Table 4.5 lower order harmonics are compared with limit values given in IEEE Std. 519-1992.

As can be seen in Table 4.4 and Table 4.5 5^{th} harmonic of filtered CSC current exceeds limit values, because harmonic currents at supply side are filtered by LC input filter and these currents affect measurement values.

TDD versus reactive power graph shows two TDD values. The blue line shows CSC STATCOM + Supply TDD values are around %7,which exceeds limit value (%5) of IEEE Std. 519-1992, if the effect of supply harmonics are subtracted the red line can be obtained, which shows only CSC STATCOM TDD values around %2.

4.2.3 Power Losses

Total power loss values of CSC STATCOM for different reactive power values can be seen in Figure 4.15. Values given in graph are calculated by active power calculation method. Total value includes switching losses, dc-link reactor losses and input filter losses. Losses are maximum %10 at 17kVAr inductive reactive power generation mode and minimum %3 at 17kVAr capacitive reactive power generation mode.

In inductive mode of operation CSC converter generates more reactive power than load in order to compensate filter capacitance and reactive power of the load so losses are higher with respect to capacitive mode of operation.

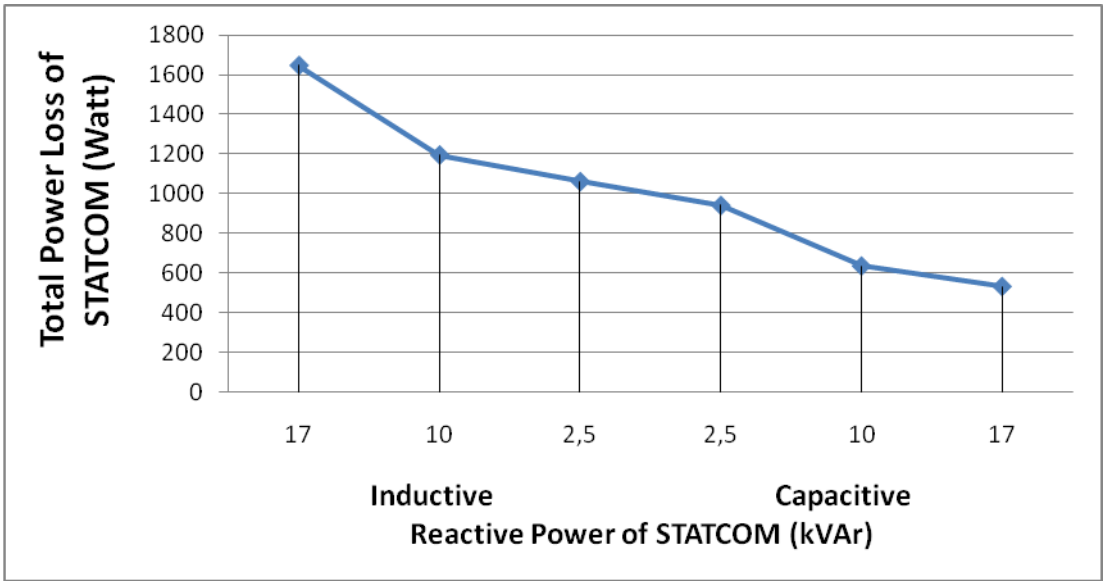


Figure 4.15 Total STATCOM losses against reactive power

4.2.4 DC Side Voltage and Current Waveforms

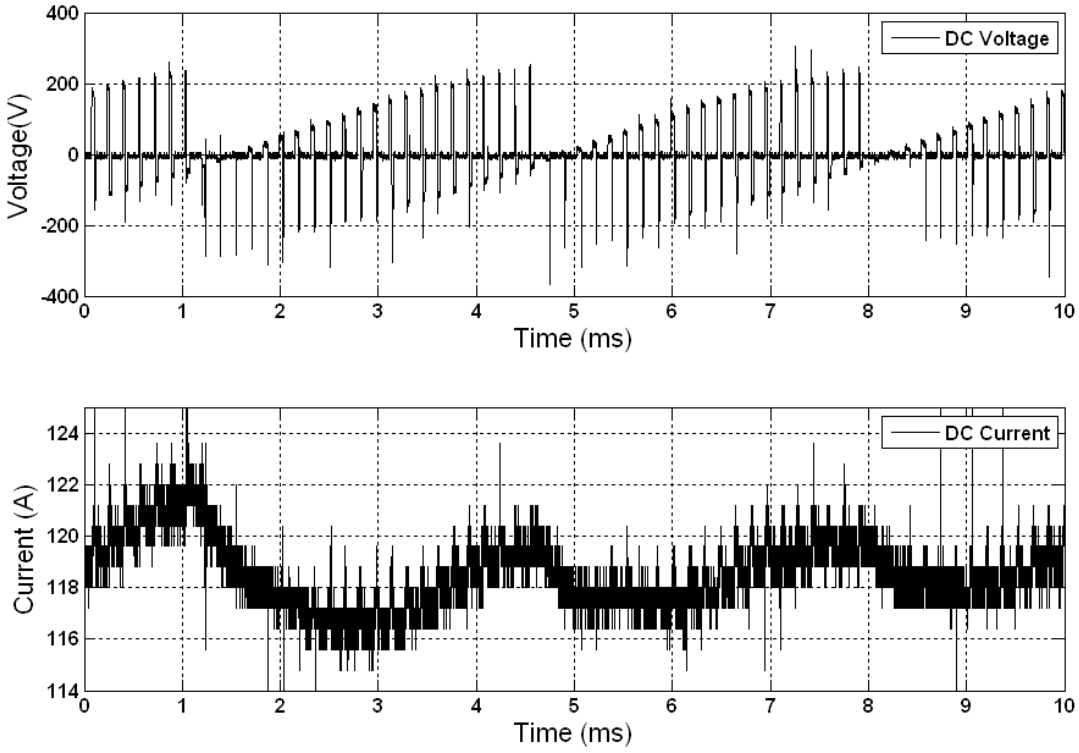


Figure 4.16 DC link waveforms of CSC for 17 kVAr Capacitive Reactive Power Generation of STATCOM (sampling rate=2.5MS/s)

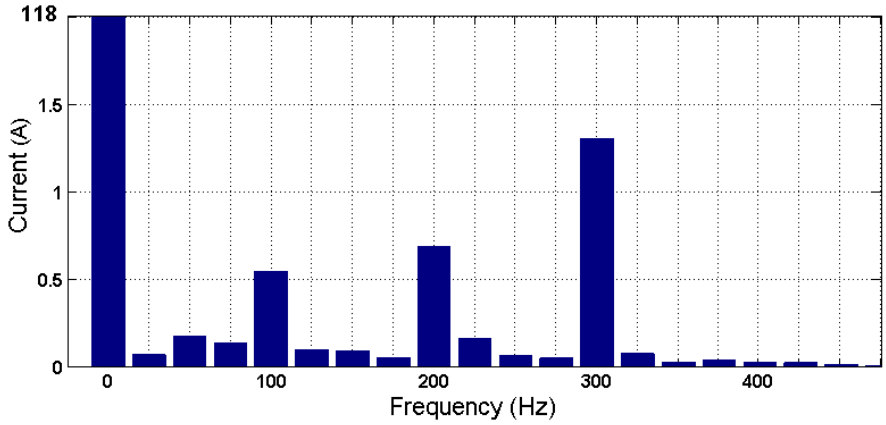


Figure 4.17 Harmonic Spectrum of DC Link Current for 17 kVAr Capacitive Reactive Power Generation of STATCOM

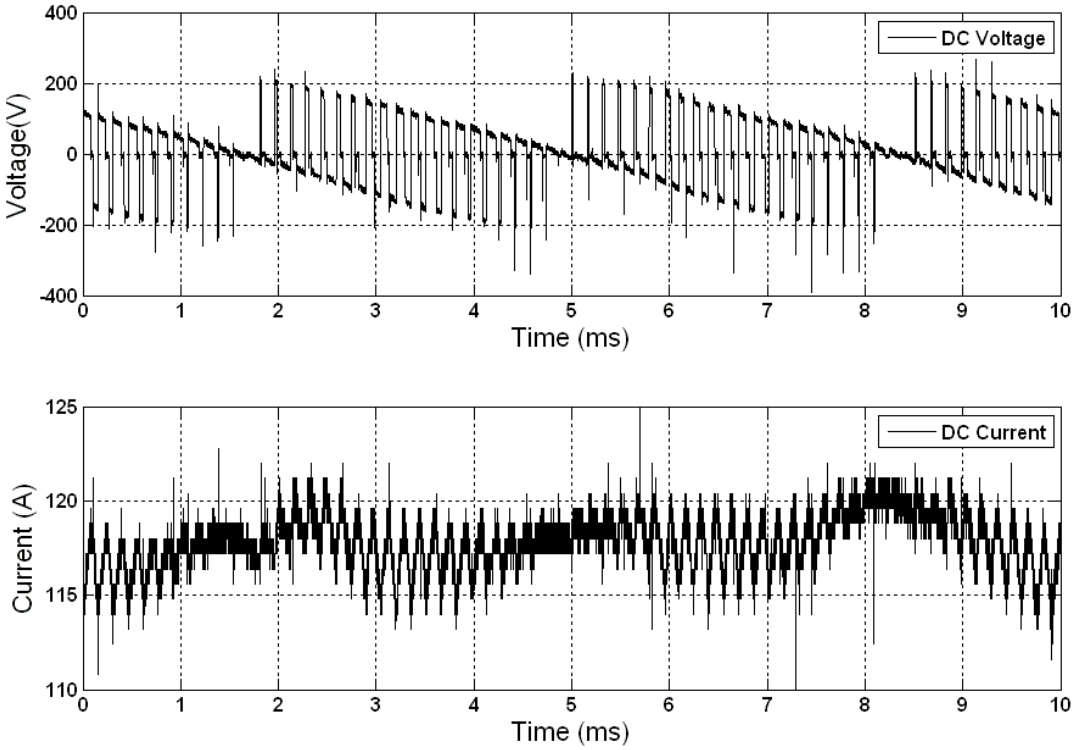


Figure 4.18 DC link waveforms of CSC for 17 kVAr Inductive Reactive Power Generation of STATCOM (sampling rate=2.5MS/s)

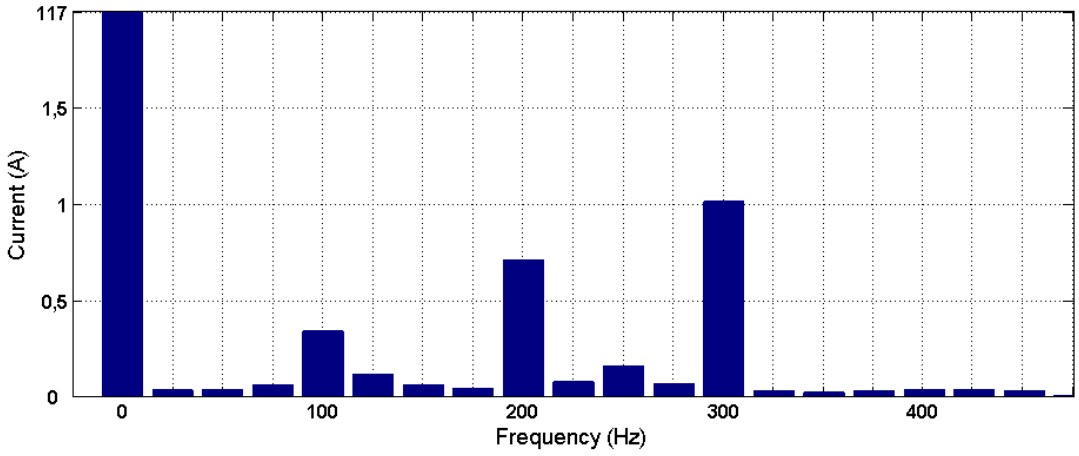


Figure 4.19 Harmonic Spectrum of DC Link Current for 17 kVAr Inductive Reactive Power Generation of STATCOM

Dc-link voltage and current waveforms are as given in Figure 4.16 for 17 kVAr capacitive reactive power generation of STATCOM and Figure 4.18 for 17 kVAr inductive reactive power generation of STATCOM. Voltage waveform has been recorded by a Tektronix P5210 high voltage differential probe. DC-link current has been measured by LA 255 LEM current transducer. The peak-to-peak ripple in dc-link current is 6A (% 5 of dc-link current) at 17 kVAr reactive power generation of STATCOM (both inductive and capacitive mode of operation).
Harmonic spectrum of dc-link current can be seen in Figure 4.17 and Figure 4.19 for related measurement data given in previous figures.

4.2.5 Reactive Power Compensation Performance

In order to test reactive power compensation performance of CSC STATCOM square wave is generated by signal generator and generated signal is given as reference reactive power to analog to digital converter of digital signal processor of control system. Maximum and minimum values of square wave is calibrated to maximum capacitive reactive power and maximum inductive reactive power.

As can be seen in Figure 2.13 there are two control loops in reference current generation algorithm. First one is dc-link current generation control loop and second one is reactive current generation control loop. Since dc-link current is constant, the effect of PI parameters in dc-link control loop to reactive power compensation performance is negligible.

By adjusting proportional constant and integral constant of reactive current generation control loop, transient performance of CSC STATCOM is improved to 20ms in PSCAD simulations, but in experimental work it is only improved up to 50ms. The effect of low pass filter which is used to filter quadrature axis component I_{qref} of reference current (as can be seen in Figure 2.13) on transient response of CSC

STATCOM is observed in Figure 4.20, Figure 4.21, Figure 4.23, Figure 4.22, Figure 4.24 and Figure 4.25.

Dc-link current changes during transient states. This can be understood from the formula (4.1).

$$P = V_d I_{sd} + V_q I_{sq} \tag{4.1}$$

During transient states V_q component does not equal to zero. It takes negative values at the transition instances from inductive to capacitive mode. In order to make active power constant at transient states dc-link controller increases the I_{dref} value instanly. V_q takes positive values at the transition instances from capacitive to inductive mode. Dc-link current controller decreases I_{dref} value instanly in order to keep active power constant.

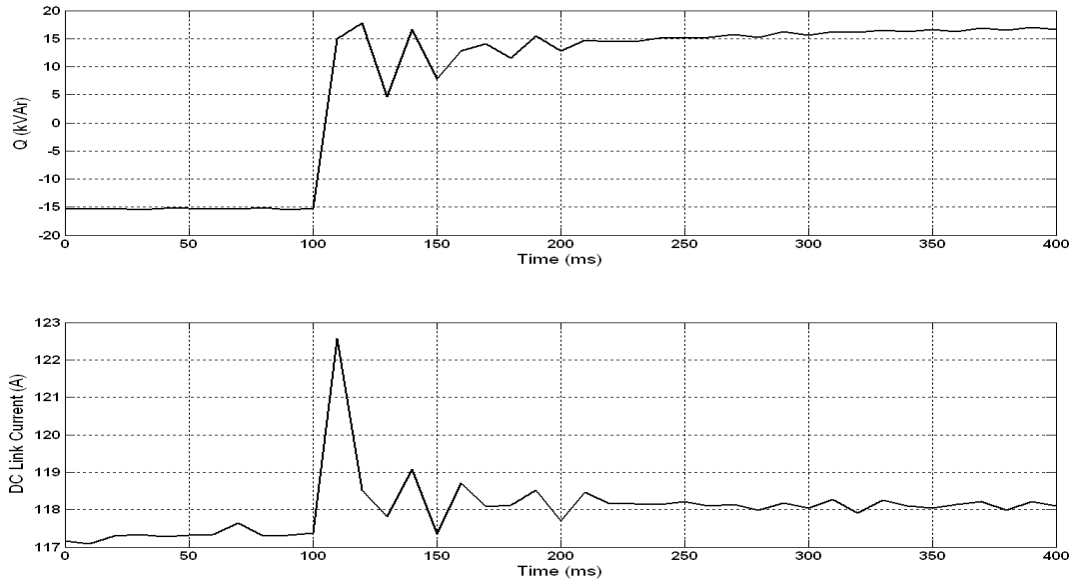


Figure 4.20 Transient response of reactive power control loop and dc-link current to a step input changing from maximum inductive reactive power to maximum capacitive reactive power (q is averaged at every 20 ms) (sampling rate= 100 KS/s and averaged at every 1000 sample)

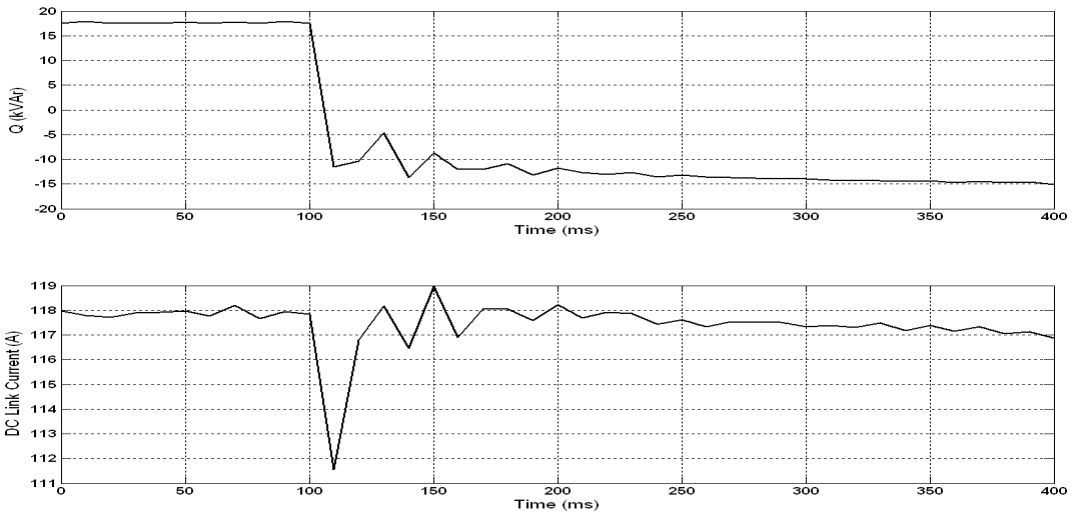


Figure 4.21 Transient response of reactive power control loop and dc-link current to a step input changing from maximum capacitive reactive power to maximum inductive reactive power (q is averaged at every 20 ms) (sampling rate= 100 KS/s and averaged at every 1000 sample)

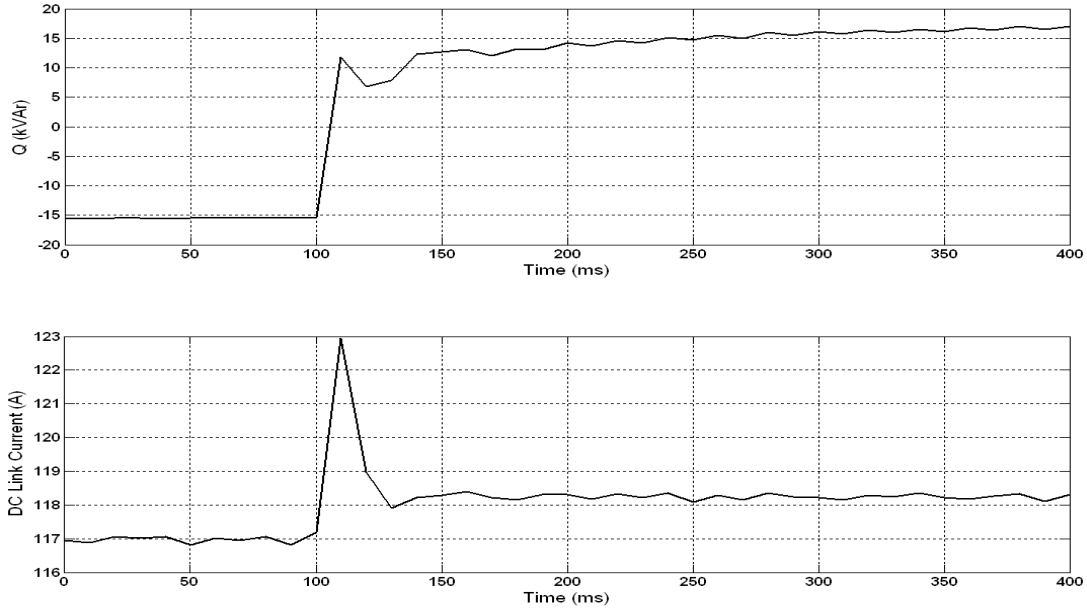


Figure 4.22 Transient response of reactive power control loop and dc-link current to a step input changing from maximum inductive reactive power to maximum capacitive reactive power (q is averaged at every 10 ms) (sampling rate= 100 KS/s and averaged at every 1000 sample)

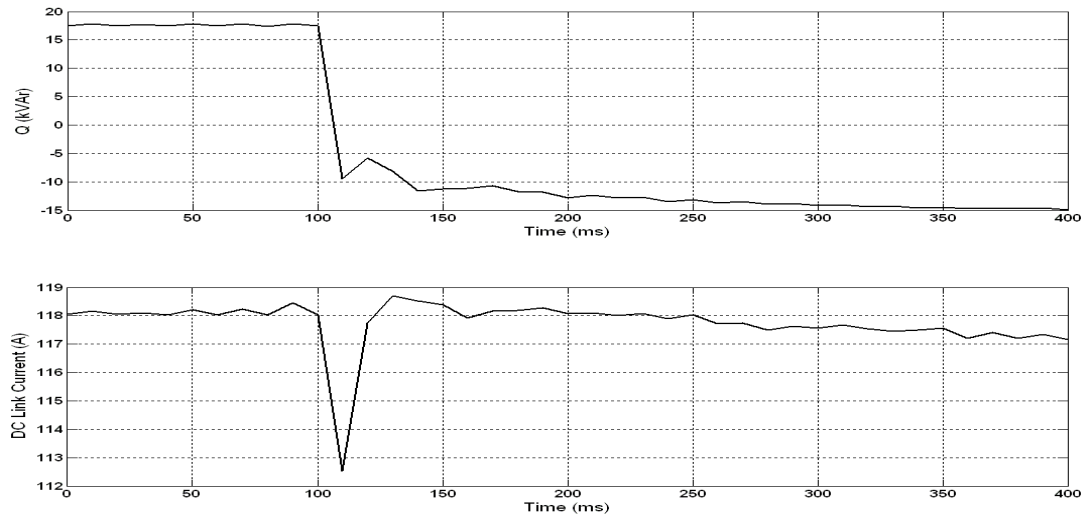


Figure 4.23 Transient response of reactive power control loop and dc-link current to a step input changing from maximum capacitive reactive power to maximum inductive reactive power (q is averaged at every 10 ms) (sampling rate= 100 KS/s and averaged at every 1000 sample)

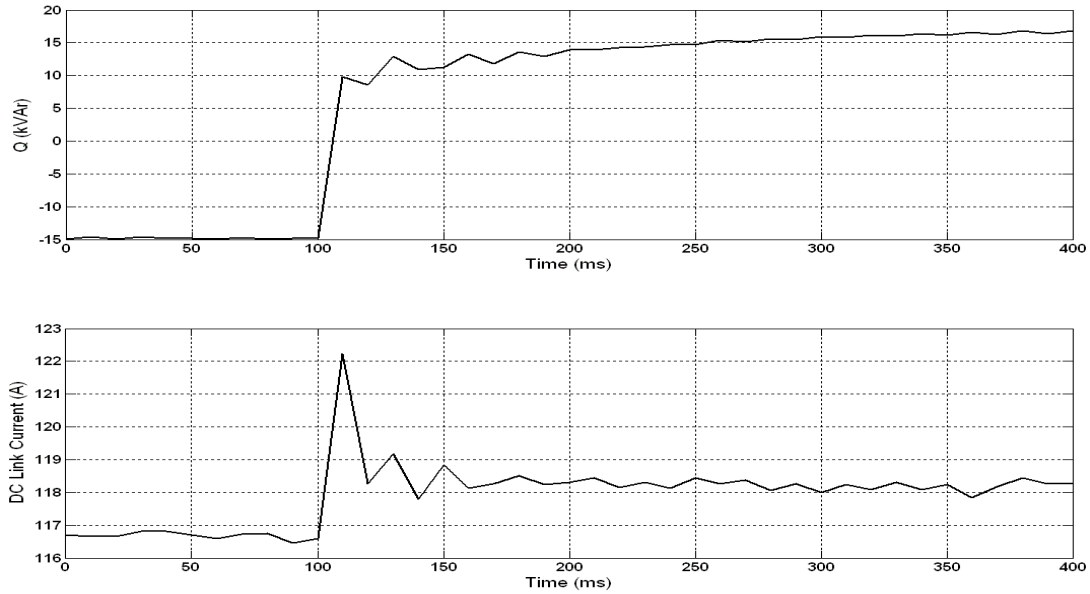


Figure 4.24 Transient response of reactive power control loop and dc-link current to a step input changing from maximum inductive reactive power to maximum capacitive reactive power (q is averaged at every 5 ms) (sampling rate= 100 KS/s and averaged at every 1000 sample)

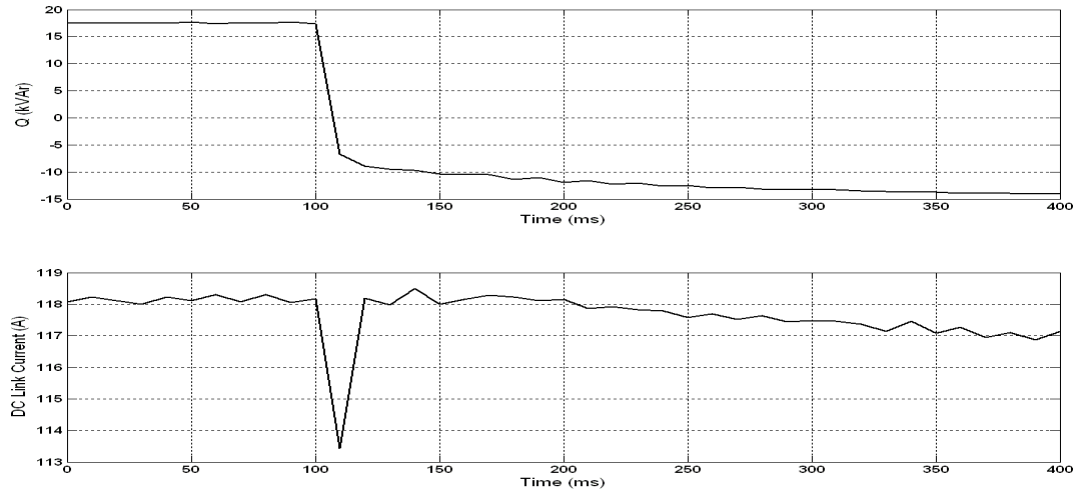


Figure 4.25 Transient response of reactive power control loop and dc-link current to a step input changing from maximum capacitive reactive power to maximum inductive reactive power (q is averaged at every 5 ms) (sampling rate= 100 KS/s and averaged at every 1000 sample)

CHAPTER 5

CONCLUSION

The design and implementation of a three phase single stage CSC based STATCOM laboratory prototype has been carried out in this research work. The developed system is composed of a single full-bridge current-source converter topology modulated with space vector pulse width modulation technique at 6250Hz sampling frequency and an ac input filter.

Designed power stage with laminated bus bar providing minimized parasitic inductances, selected bipolar voltage blocking semiconductors and low commutation times between semiconductor switches provides high frequency current switching.

High frequency SVPWM method provides negligible lower order harmonics and harmonics around switching frequency generated by current source converter are filtered succesfully by designed low pass LC input filter. The line currents of CSC based STATCOM at common coupling point comply with IEEE Std. 519-1992. TDD performance of the STATCOM is improved by high switching frequency SVPWM modulation method , it can be seen from the results that the designed system provides satisfactory TDD performance at the selected switching frequency.

Dc-link current peak-to-peak ripples are minimized by selecting optimum dc-link reactor value at determined switching frequency.

Transient response of the system can be improved by adjusting proportional constant and integral constant of the PI control loop.

Following conclusions can be drawn from the results of theoretical and experimental work carried out within the scope of this research work:

− The technical feasibility and viability of an low voltage IGBT based SVPWM modulated CSC STATCOM application have been proven.

− The current harmonic standards can be met by using high frequency modulated current source converter based STATCOM.

− The CSC STATCOM topology is very flexible so that asymmetrical operating characteristics can be easily realized by using larger input filter capacitor banks and/or by connecting plain capacitor or tuned LC filters.

− The developed system gives a satisfactory performance in both steady state and transient state. A complete transition from maximum inductive VAr production to maximum capacitive VAr production or vice versa takes place in a time period less than 50 msec. The use of smaller input filter components and on-line PWM technique reduce response time significantly at the expense of higher switching frequency. With the use of state feedback control method, dynamic response of CSC based STATCOM is improved.

− Instead of using damping resistors in ac filter, using active damping method decreases the power losses of CSC STATCOM.

Proposed further works can be done in the future:

- In order to obtain a lower power loss profile over a wide operating range, an adaptive control can be employed for dc-link current.
- An advanced controller, such as fuzzy-logic or adaptive PI-controller can be applied to improve the transient response.
- Load balancing feature (i.e., compensation of negative sequence components of the load currents) with minimum energy storage elements can be analyzed and implemented.

REFERENCES

[1] Juan Dixon, L. M. (*Dec. 2005*). "Reactive Power Compensation Technologies: State-of-the-Art Review". *IEEE JNL Volume 93, Issue 12, Page(s):2144 - 2164* .

[2] L.Moran, P. G. (March/April 1989). "Analysis and Design of a Three-Phase Current Source Solid-State Var Compensator". *IEEE Tran. Ind. Appl. , vol.25*.

[3] Wang BS, C. J. (Nov 2003). "DSP-controlled, Space-Vector PWM, Current Source Converter for STATCOM application. *Elect. Pow. Syst. Res. , vol.67* (no.2), pp. 123-131.

[4] D.Shen, P. (2002). "Modeling, Analysis, and Control of a Current Source Inverter-Based STATCOM". *IEEE Tran. Power Delivery , vol.17, no.1*.

[5] Y.Ye, M. V. (April 2005). "Current-Source Converter Based STATCOM: Modeling and Control". *IEEE Tran. Power Delivery , vol.20.* (no.2).

[6] F. Bilgin, M. E. (Jan./Feb.2007). "Reactive Power Compensation of Coal Mining Excavators by Using a New-generation STATCOM". *IEEE Trans. On Industry Applications , vol.43* (no.1), pp.97-110.

[7] Bilgin, H. (2007). *"Design and implementation of a current source converter based statcom for reactive power compensation,".* Ph.D. Dissertation,METU.

[8] J.Espinoza, G. (Feb. 1998). "State Variable Decoupling and Power Flow Control in PWM Current Source Rectifier". *IEEE Tran. Ind. Electr.*

[9] H.Akagi, E. M. (2007). "Instantaneous Power Theory and Applications to Power Conditioning". *IEEE Press* .

[10] Y.W.Li, B. N. (July 2007). "Damping of PWM current source rectifiersusing a hybrid combination approach". *IEEE Trans. on Power Electronics , vol.22* (no.44), 1383-1393.

[11] Y.Sato, T. (May/June 1996). "A Current-Type PWM Rectifier with Active Damping Function". *IEEE Trans. On Industry Applications , vol.32*, pp.533-541.

[12] M.Salo, H. (May 2000). "A vector controlled current-source PWM rectifier with a novel current damping method". *IEEE Trans. on Power Electronics , vol.15* (no.3), pp.464-470.

[13] Y.Sato, T. (1993). "State feedback control of current-type PWM AC-to-DC converters". *IEEE Trans. on Industry Applications , vol.29* (Issue 6), pp.1090-1097.

[14] K.Toyama, T. N. (August 1997). "Transient oscillation suppression of input filter voltage and current for current-source three-phase PWM AC/DC converter". *Proceedings of the Power Conversion Conference-Nagoka , vol.1*, pp.253-258.

[15] D.G.Holmes, T. (2003). *Pulse width modulation for power converters: Principles and Practice.* New Jersey: IEEE Press.

[16] J.Holtz. (October 1992). "Pulsewidth Modulation-A Survey". *IEEE Trans. on Industrial Electronics , vol.39* (no.5), pp.410-420.

[17] M.A.Boost, P. (Match/April 1988). "State of the art carrier PWM techniques: a critical evaluation. *IEEE Trans. on Ind. Applications , vol.24* (Issue2), pp.271-280.

[18] G.Ledwich. (October 1991). "Current source inverter modulation". *IEEE Trans. on Power Electronics , vol.6* (Issue 4), pp.618-623.

[19] M. Hombu, S. Y. (Sept/Oct. 1985). "A new current source GTO inverter with sinusoidal output voltage and current. *IEEE Trans. Ind. Appl. , vol.IA-21* (no.5), pp.1192-1198.

[20] P.N. Enjeti, P. Z. (May/June 1991). "A current source PWM inverter with instantaneous current control capability". *IEEE Trans. on Industry Applications , vol.10* (no.3).

[21] X.Wang, B.-T. O. (July 1993). "Unity PF current-source rectifier based on dynamic trilogic PWM". *IEEE Trans. on Power Electronics , vol.8* (Issue 3), pp. 288-294.

[22] B.H.Kwon, B. (June 1993). "A Fully Software Controlled PWM Rectifier with Current Link". *IEEE Tran. Ind. Electr.*

[23] V.G. Agelidis, P. Z. (July 1996). "Dead-band PWMswitching patterns". *IEEE Trans. on Power Electronics , vol. 11* (Issue 4), pp. 522-531.

[24] J. Dai, Y. L. (Nov. 2009). "A multisampling SVMscheme for current source converters with superior harmonic performance". *IEEE Trans. on Power Elect. , vol. 24* (no. 11), pp. 2436-2445.

[25] H.R.Karshenas, H. S. (Sept. 1995). "Generalized techniques of selective harmonic elimination and current control in current source inverters/converters". *IEEE Tran. on Power Elect. , vol.10* (no.5).

[26] B. -H. Kwon, B. M. (June 1993). "A fully software-controlled PWM rectifier with current link". *IEEE Trans. on Industrial Electronics , vol. 40* (Issue 3), pp. 355-363.

[27] *"Specification for PSCAD V4.2"*. http://www.pscad.com last accessed date: 01/04/2010

[28] *"MATLAB"*. http://www.mathworks.com last accessed date: 01/04/2010

[29] *"ORCAD"*. http://www.cadence.com/products/orcad last accessed date: 01/04/2010

[30] G. Joos, J. R. (Nov. 1993). "PWM Control Techniques in Current Source Rectifiers". *IEEE IECON'93 International Conference on Industrial Electronics Control, and Instrumentation* , pp.1210-1214.

[31] *"Capacitors for power electronics"*. http://www.electronicon.com last accessed date: 01/04/2010

[32] *"Microsemi Power Semiconductors"*. http://www.microsemi.com last accessed date: 01/04/2010

[33] *"eZDSP TMS320F28335"*. http://focus.ti.com/ last accessed date: 01/04/2010

APPENDIX A

PSCAD/EMTDC MODEL FOR VSC BASED STATCOM

CSC based STATCOM system is simulated in PSCAD/EMTC program. Converter waveforms, input filter waveforms, line currents are analyzed and closed loop control of STATCOM system is tested.

0.4 kV CSC STATCOM model is given in Fig. A.1.

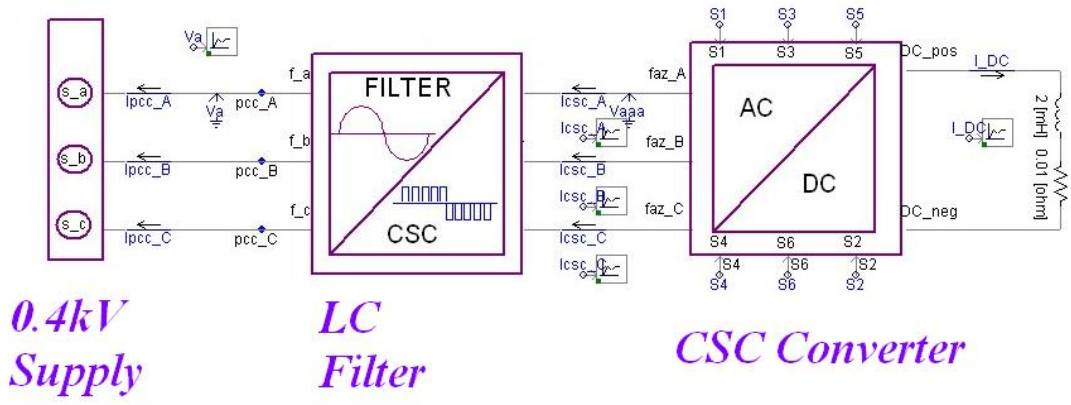


Figure A.1 *CSC STATCOM Model*

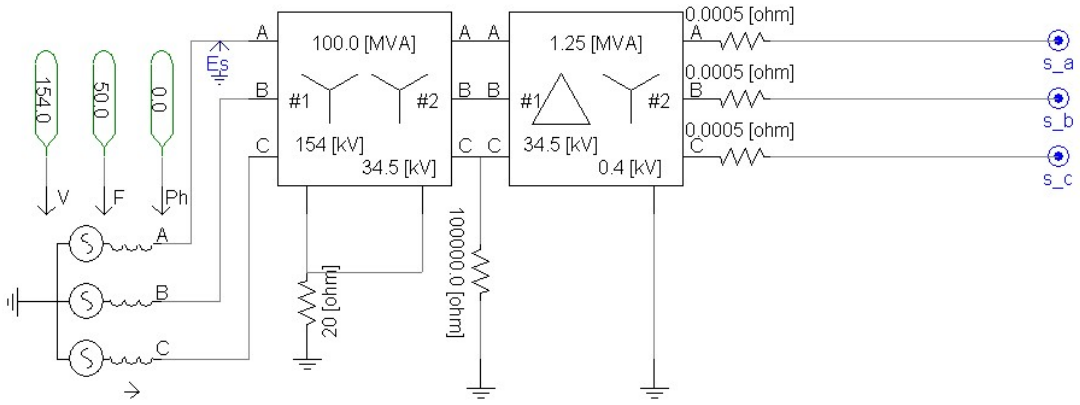


Figure A.2 *0.4kV Supply Model*

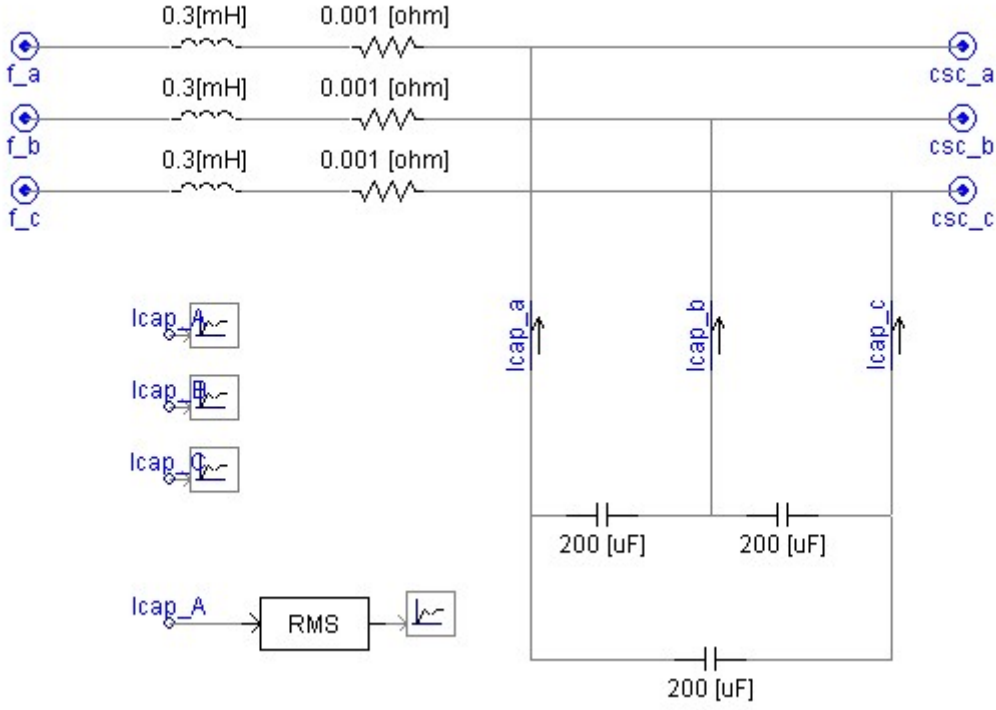


Figure A.3 *LC Filter Model*

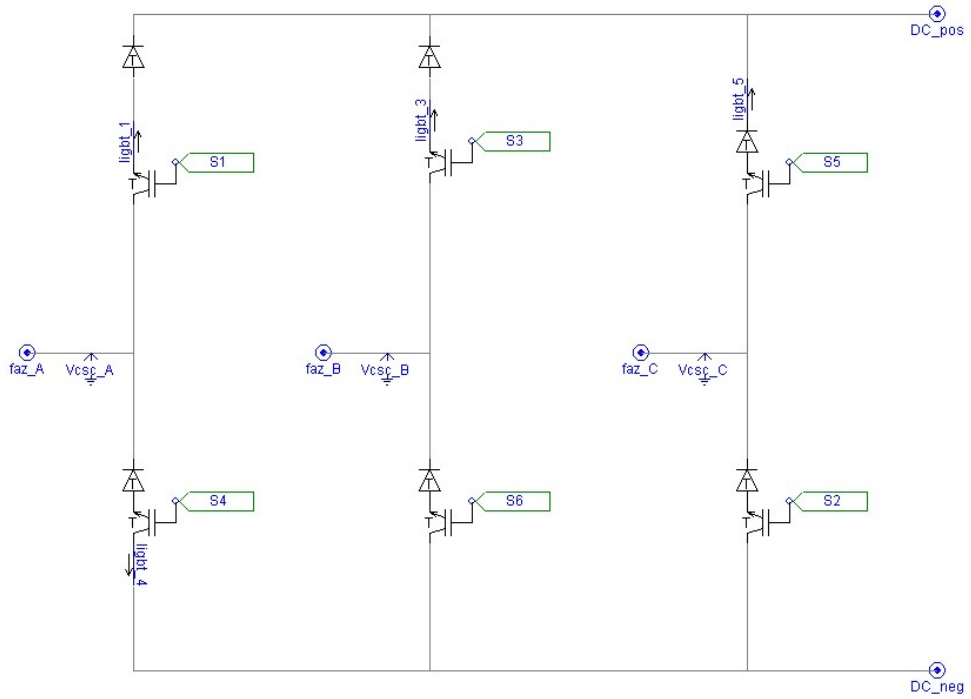


Figure A.4 *CSC Converter Model*

APPENDIX B

PWM PATTERN GENERATORS

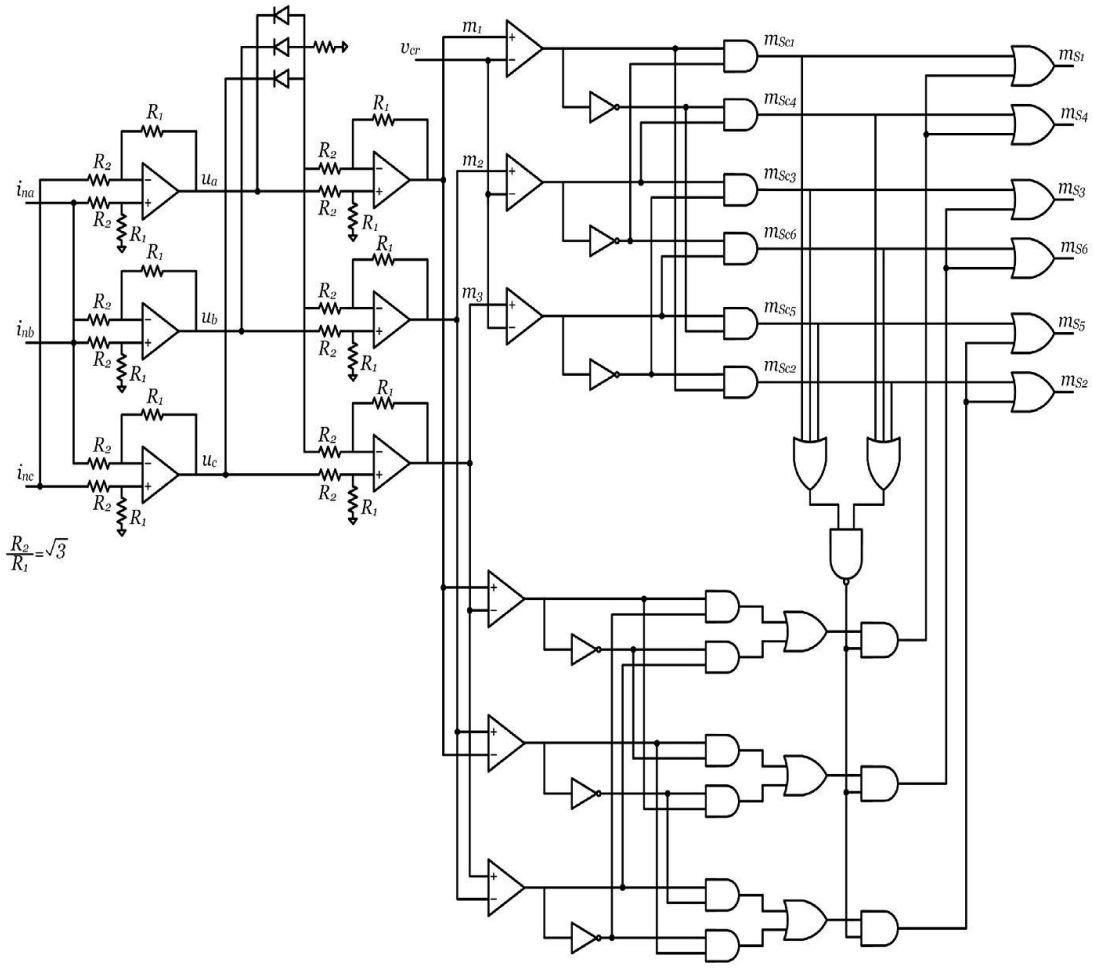


Figure B.1 *Analog Circuit Representation of the DSPWM Based Pattern Generator*

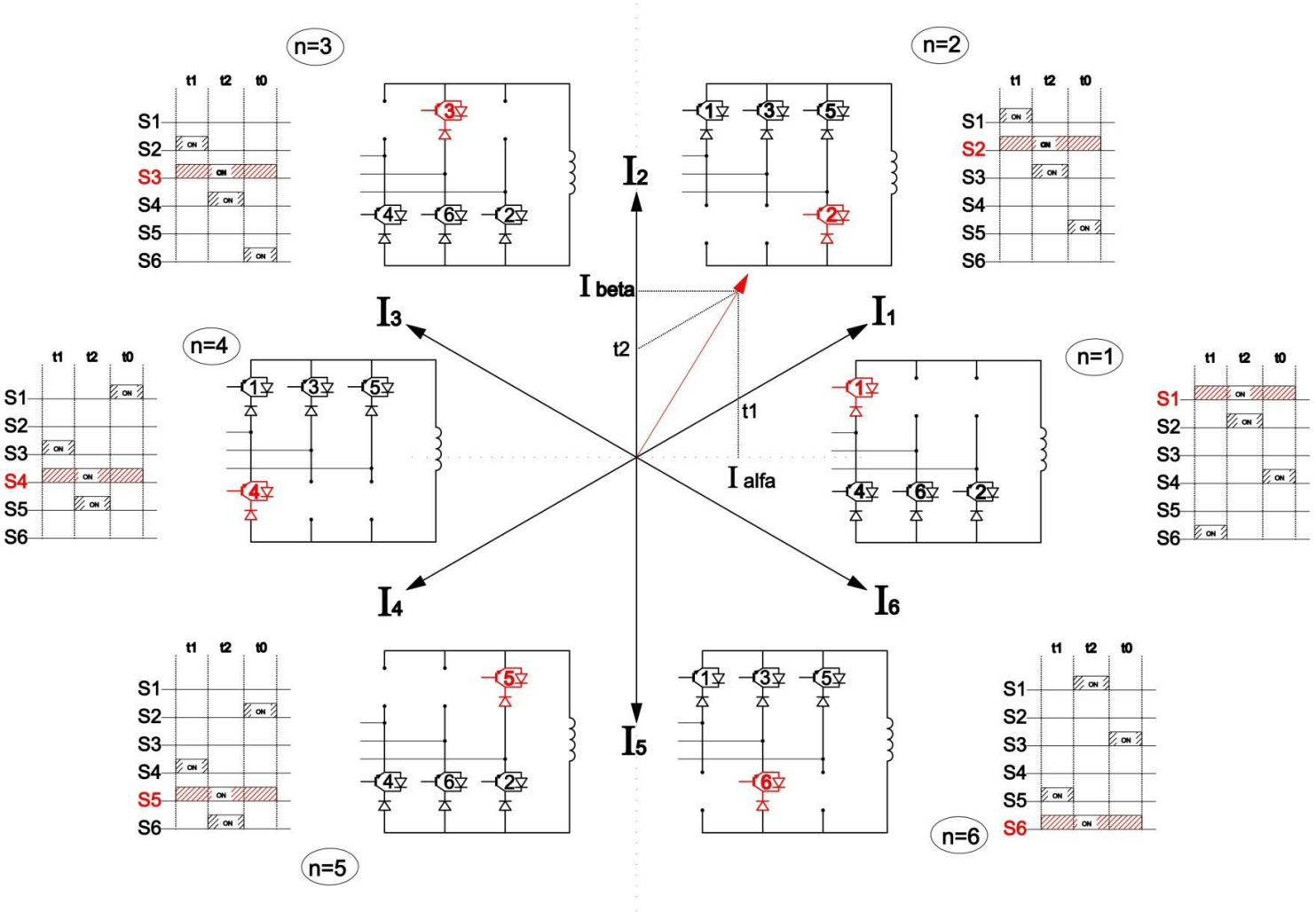


Figure B.2 *Graphical Illustration of SVPWM Based Pattern Generator*

APPENDIX C

INTERNAL STRUCTURE OF APTGF300U120DG

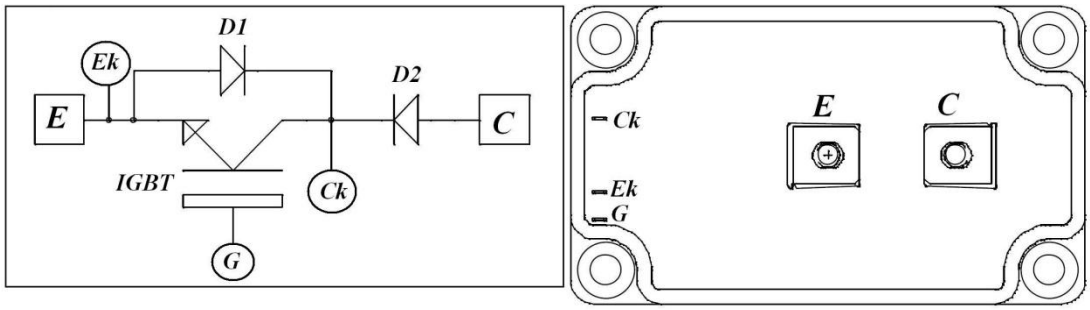


Figure C.1 *APTGF300U120DG*

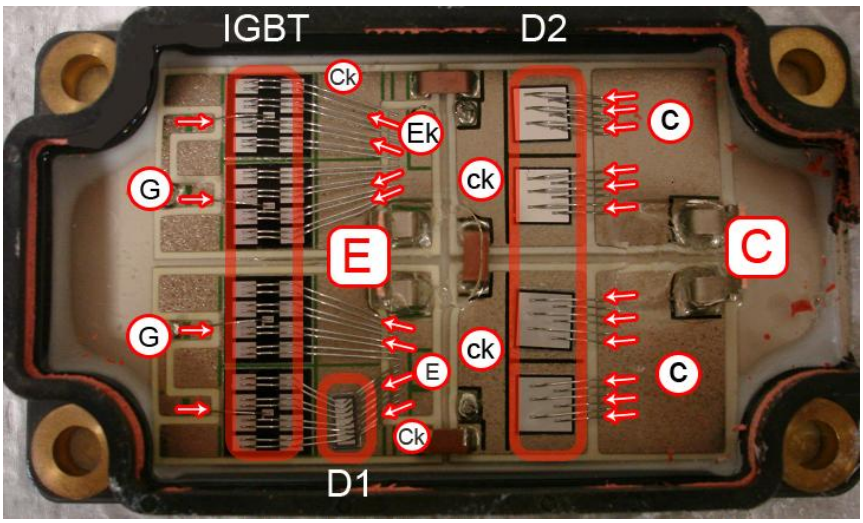


Figure C.2 *Internal Structure of APTGF300U120DG*