Z-SOURCE, FULL BRIDGE DC/DC CONVERTER

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ABSTRACT

Z-SOURCE, FULL BRIDGE DC/DC CONVERTER

Pekuz, Çağdaş

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The thesis is related to investigate characteristics and performance of a Z-source full bridge dc/dc converter which boosts the input voltage to a higher output voltage. Z-source structure increases the reliability of the converter according to current fed full bridge dc/dc converter and also reducing the complexity according to two stage design approach (boost followed by full bridge). Operating principles of the Z-source dc-dc converter is described by current and voltage waveforms of the components and mathematical expressions. Moreover, small signal models and transfer functions are derived for both continuous current mode (CCM) and discontinuous current mode (DCM) operations of the converter. Waveforms obtained, mathematical expressions, small signal models and transfer functions derived are confirmed by simulations. Performance of the converter and controller are both tested in laboratory prototype.

Keywords: Z-source, full bridge dc/dc converter.

ÖZ

Z KAYNAKLI, TAM KÖPRÜLÜ DC/DC ÇEVİRİCİ

Pekuz, Çağdaş

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Bu tezde, Z-kaynak yapısı kullanılarak, giriş gerilimini daha yüksek bir çıkış gerilimine dönüştüren Z-kaynaklı tam köprülü bir dc/dc çeviricinin karakteristiği ve performansı incelenmiştir. Z-kaynak yapısı, akım beslemeli tam köprülü dc-dc çeviriciye göre daha güvenilirdir. Ayrıca, iki aşamalı (tam köprülü çevirici ve yükseltici çeviricinin arka arkaya kullanılması) çeviricinin karmaşıklığını azaltmaktadır. Devrenin çalışma ilkeleri, matematiksel denklemler ve dalga şekilleri ile açıklanmıştır. Devrenin hem sürekli akım durumundaki hem de aralıklı akım durumundaki küçük sinyal modelleri ve iletim fonksiyonları bulunmuştur. Bulunan matematiksel denklemler, dalga şekilleri, küçük sinyal modelleri ve iletim fonksiyonları benzetim sonuçlarıyla doğrulanmıştır. Çeviricinin performansı ve tasarlanan kontrol döngüsü örnek devreyle test edilmiştir.

Anahtar Kelimeler: Z-kaynak, tam köprülü dc/dc çevirici.

To my dear family

Hasan PEKUZ

Gülgün PEKUZ

Çağlar Kâzım PEKUZ

ACKNOWLEDGEMENTS

I would like to thank to my supervisor Prof. Dr. Aydın Ersak because of his supports, suggestions, and guidance throughout this thesis study.

I would like to express my gratitude to my family because of their love and support.

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CHAPTER 1

INTRODUCTION

1.1 General

In some application, such as battery powered, photovoltaic or fuel cell systems, load requires higher dc voltage than dc source voltage. In this circumstance, the usage of dc/dc converter becomes compulsory in terms of efficiency reasons. Traditionally, a boost converter can be used to increase the input voltage to a higher voltage level. The other topologies, used to boost the input voltage, such as flyback and current-fed converters are derived from the boost converter. Furthermore, in many applications of the dc/dc converters the electrical isolation between the input and output grounds is the main requirement to prevent dc current flows between the input ground and output ground. Dc current which flows between the input and output grounds can decrease the overall system reliability and cause failures at the load side. If the electrical isolation between the input and output stages is a concern than the usage of traditional boost converter is inconvenient and transformer based dc/dc converters must be used.

The main transformer-based boost converter is flyback converter because it is a buck-boost derived converter. The flyback converter is generally used up to 100-150Watts. However, if the load power and current demand increases it has some drawbacks [1]. The voltage stress on the switch is high because of the topology. If the output power increases as well which causes a considerably energy stored on the leakage inductance of the transformer increases and causes large voltage spike on the switch. This phenomenon limits the flyback converter output power rating. The full-bridge structure is preferred if the load power demand increases beyond 250-300 watts for isolated dc/dc converters.

The conventional full-bridge topology reducing the input voltage to a lower level is normally a buck derived topology because the energy drawn from the source is delivered to the load instantaneously. However, voltage-fed full-bridge converter with step-up transformer and current-fed full-bridge converter can be used for boost applications.

Voltage-fed full-bridge converter for a step-up application has been analyzed before together with the effects of turn-ratio and leakage inductance of the transformer and output inductor, [2]. This studt shows that the rms current which flows through MOSFETs increases in case the transformer turn-ratio increases. This leads to higher power loss on MOSFETs and reduction of the converter efficiency. Another study reported in the literature on a zero voltage switching (ZVS) application of voltage-fed full-bridge dc/dc converter reduces the switching losses on the MOSFETs and the conduction losses on the transformer, [3]. In conventional ZVS application of voltage-fed full-bridge dc/dc converter, the idle current flow through the primary side of the transformer and through MOSFETs during freewheeling interval is high. Another ZVS voltage-fed converter is proposed in [4]. This proposed scheme reduces the idle current to lower levels. Thus, the conduction losses of the MOSFETs and transformer are reduced.

There are various studies in the litreture regarding to current-fed full-bridge topologies. [5] analyzes and discuss operational issues of them. [6] proposes a ZVS application of them to reduce the voltage stress on the switching MOSFETs and rectifier diodes. A constant turn-on control, leading to variable switching frequency, to achieve zero-current switching (ZCS) is applied to such topology in [7]. This scheme reduces the current and voltage stresses and the switching losses on the devices. Another benefit of the ZCS application is the elimination of the reverse recovery problems at the rectifier diodes.

Voltage-fed full-bridge converter for step-up applications display low voltage spike on the switches at the primary side compared to current-fed full-bridge converter. Thus, lower voltage rated and lower on state resistance MOSFETs can be used in voltage-fed converter. Also, current-fed converter has start-up problem to the contrary of the voltage-fed converter, [5]. However, the transformer of the voltage-fed step-up full-bridge has high leakage inductance and parasitic capacitance

because of the large turn-ratio. High leakage inductance and parasitic capacitance increase the switching loss, together with the voltage and the current spikes on the components, [7]. Also, high currents through the switches on the primary side and voltage ringing on the rectifier diodes are the other disadvantages of the voltage-fed full-bridge converter compared to current-fed one, [3]. In [8], the current-fed and voltage-fed full-bridge converters are compared in terms of the semiconductor losses, complexity of the converter and the effects of leakage inductance and dimensions of the transformer. It is decided that current-fed converter is more suitable for high voltage applications than the voltage-fed converter because of the semiconductor losses, transformer dimensions and the voltage stress on rectifier diodes. Another criterion to the current-fed converter choice is the smoothness of the current drawn from the source.

The conventional current fed full bridge converter is shown in Fig.1.1.

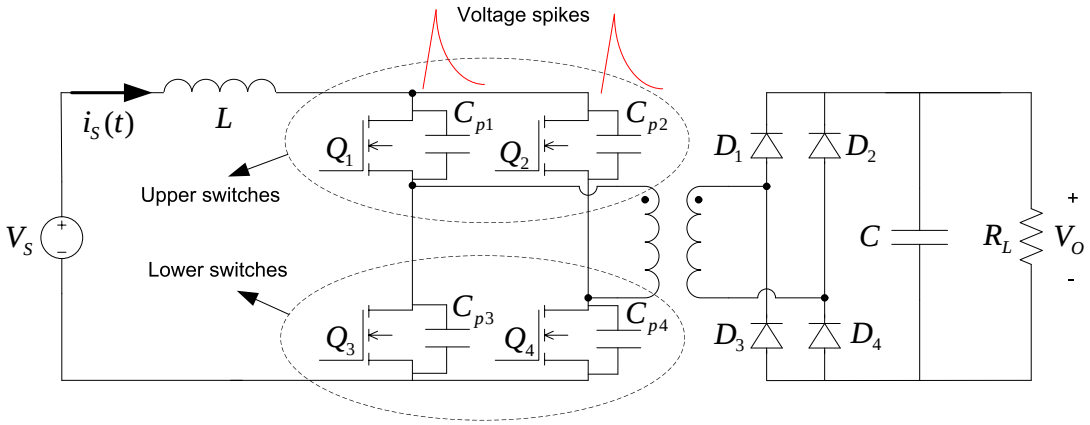

Fig.1.1. Conventional current fed full bridge dc/dc converter

In steady-state operation of the current-fed full-bridge converter, when the duty-factor is high all the switches, Q_1, Q_2, Q_3 and Q_4, are 'ON' and the input is shorted to ground across the inductor, L. In this time interval, the inductor, L, energized. When the duty-factor is low, one of the diagonal switch pairs "(Q_1 and Q_4) or (Q_2

and Q_3)" are in conduction. The conduction of one pair pursues the other. For the first period, if the switch pair, (Q_1 and Q_4), is in conduction then, for the second period, switch pair, (Q_2 and Q_3), will be conducting. Thus, the energy stored in the inductor is delivered to the load when the duty-factor is low.

From Fig.1.1, one of the upper switches (Q_1 and Q_2) and one of the lower switches (Q_3 and Q_4) must be 'ON' for the entire period of operating. If this condition is not satisfied due to the failure of gating of the switches (which can be arises from EMI problems, failure of MOSFET driver circuit, controller failure or etc.), all the stored energy in the inductor is transferred to the parasitic capacitances (C_{p1}, C_{p2}, C_{p3} and C_{p4},) of the switches. The transferred energy causes huge voltage spike, shown in Fig.1.1, because the parasitic capacitances of the switches are too small compared to the amount of the transferred energy to them. The switches are demaged because the voltage spike exceeds the break down voltage. This fact decreases the reliability of the converter.

The reliability problem can be solved in the current-fed full-bridge converter by using Z-source structure instead of a single inductor, L. The proposed scheme is shown in Fig.1.2.

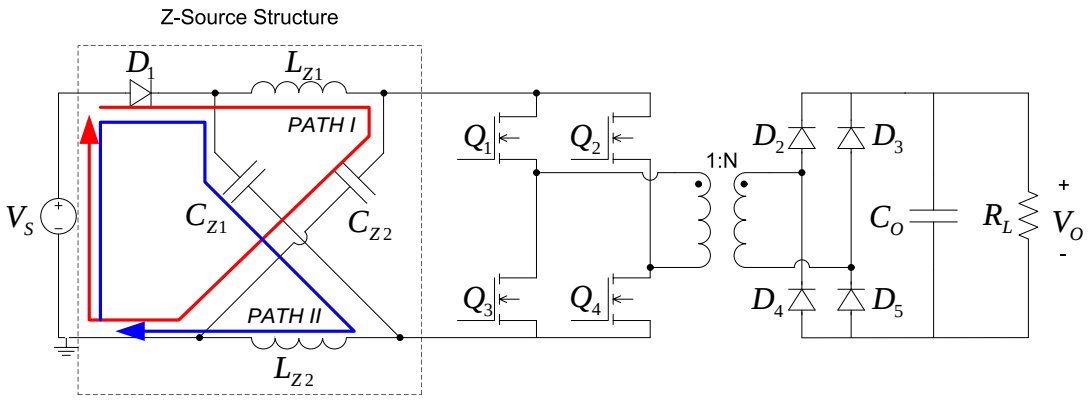

Fig.1.2 Representation of the usage of the Z-source structure instead of single inductor, L, in the current fed full bridge converter

The operating principle of the Z-source full-bridge dc/dc converter is similar to the current-fed full-bridge converter. When the duty-factor is high, all the switches, Q_1, Q_2, Q_3 and Q_4, are 'ON' and the Z-source inductors, L_{Z1} and L_{Z2}, are energized. When the duty-factor is low, the sequential driving of diagonal switch pairs '(Q_1 and Q_4) or (Q_2 and Q_3) transfer the stored energy in the L_{Z1} and L_{Z2} to the load, R_L.

In Z-source full-bridge converter, if the one of the upper switches (Q_1 and Q_2) and one of the lower switches (Q_3 and Q_4) are not gated simultaneously, the stored energy in the Z-source inductor, L_{Z1}, is transferred to the Z-capacitor, C_{Z2}, through the PATH I, as shown in the Fig.1.2. Similarly, the stored energy in the Z-source inductor, L_{Z2}, is delivered to the Z-capacitor, C_{Z1}, through PATH II. Thus, there will be no voltage spike across the switch terminals and the switches will not be damaged. Z-source full-bridge dc/dc converter can be used instead of current-fed full-bridge dc/dc converter to increase the reliability of the converter enormously.

1.2 Motivation

Z-source structure can be used in all types of power conversions such as ac/dc rectifiers, dc/dc converters, dc/ac inverters and ac/ac converters. The main operation principles of Z-source structure and application of Z-source structure to inverter are investigated in detail in [9]. The study discusses the drawbacks of traditional voltage-fed and current-fed inverters also. In voltage-fed inverter, the output ac voltage can not exceed the input dc voltage and upper and lower switches of the same phase can not be made 'ON' at the same time during the operation. Furthermore, in the current-fed inverter, the output ac voltage is always greater than the input dc voltage, and one of the upper switches and one of the lower switches must be 'ON' at any time during the operation. Z-source inverter eliminates these problems and gives an opportunity of using the inverter as a step-up or step-down inverter.

The single phase ac/ac converter application of Z-source structure is investigated in [10]. The most popular topology for the ac/ac converter for the requirement of different output voltage level and variable output frequency is the usage of cascaded

diode rectifier and inverter, respectively. However, if only the voltage regulation at the output side is of concern, the single phase Z-source ac/ac converter can provide a cheaper and lower-sized solution, [10]. Also, the proposed single-phase Z-source ac/ac converter in [10] can be used to tackle voltage sags, surges and load fluctuations. Moreover, the operating principle of the three-phase Z-source ac/ac converter is investigated in [11].

The application of Z-source structure in single-phase rectifier is proposed in [12]. Also, the operating principle of the proposed circuit is investigated in that study. Using single phase Z-source rectifier instead of traditional two-stage ac/dc buck rectifier brings some advantages. It gives the opportunity to adjust the output dc voltage greater or smaller than the input ac voltage. Also, the minimized and single stage structure of the proposed rectifier provides high efficiency and small size, [12]. Furthermore, the three phase rectifier application of Z-source structure is proposed in [13]. In that study, the power-factor of the rectifier is discussed together with the operating principle.

For dc/dc application of Z-source structure, the main studies are [14] and [15]. In both, the analyzed circuit is a simplified version of Z-source full-bridge dc/dc converter, as shown in Fig.1.3.

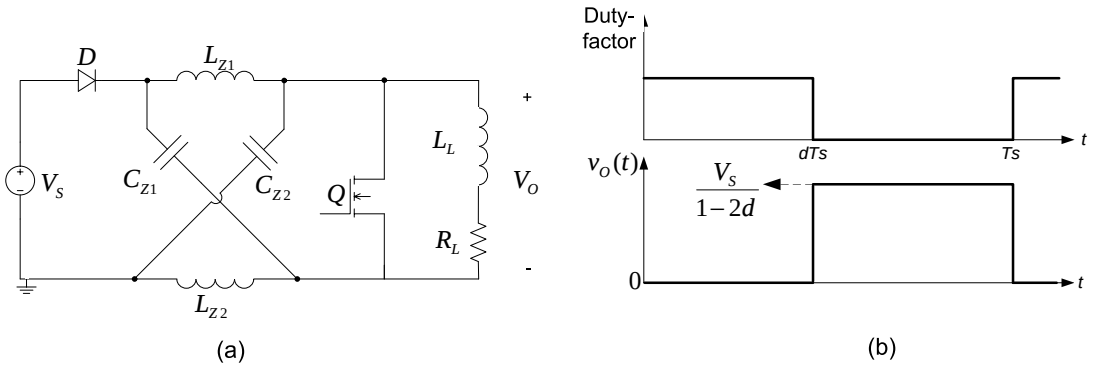

Fig.1.3 a) Investigated Z-source dc/dc converter in [14] and [15], b) output voltage waveform

[14] investigates the main operating principle of the proposed Z-source dc/dc converter, shown in Fig.1.3. The small signal equivalent circuits of the converter and transfer functions of input voltage-to-Z-source capacitor voltage, duty-factor-to-Z-source capacitor voltage, input voltage-to-Z-source inductor current, duty-factor-to-Z-source inductor current are all determined for CCM operation. Referring to Fig.1.3, in time-domain, the output voltage of the converter, $v_O(t)$ is not a purely dc voltage, on the contrary, it is a rectangular wave voltage swinging between zero and its peak value, $\frac{V_S}{1-2d}$, at the switching frequency. The averaged output voltage of the converter, V_O, is equal to the voltage across the Z-source capacitor. Thus, for the determination and compensation of the output voltage, the voltage across the Z-source capacitor is used in the analysis in [14]. In [15], voltage mode and current-programmed mode control techniques are applied to the Z-source dc/dc converter according to the transfer functions founded in [14].

In Fig.1.3, the load is represented as a R_L - L_L. This representation is suitable for inductive loads such as dc motors because the mechanical time constant of a dc motor is much greater than the rectangular wave output voltage period and the output voltage swings do not prevent the operation of the dc motor. However, the proposed circuit is inconvenient for resistive or capacitive type loads. Thus, an output filter must be added at the output of the Z-source dc/dc converter to get a pure dc voltage at the output, [13]. An LC filter can be a good choice for filtering the output voltage. Second-order LC filter results in less voltage ripples at the output and less current stress on the capacitor compared to those of the first-order C filter. The proposed Z-source dc/dc converter to get pure dc voltage at the output side is shown in Fig.1.4.

The differences between the circuits shown in the Fig.1.3 and Fig.1.4 are the addition of diode D_2 in series with the inductor, L_O, and the output capacitor, C_O. Normally, the diode D_2 represents the rectifier diodes of full-bridge dc/dc converter and output capacitor, C_O, is added to achieve second-order filtering at the output.

The addition of C_O changes all the dynamic responses of the converter. The transfer functions given in [14] are not valid for the circuit shown in Fig.1.4 anymore. Thus, the transfer functions of the converter must be determined to design a controller.

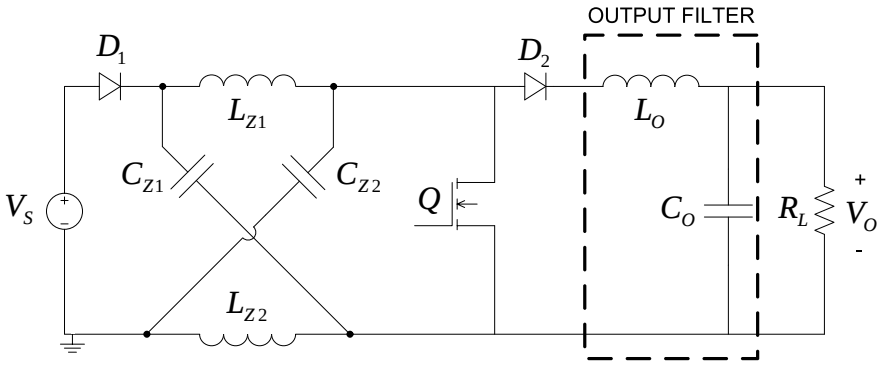

Fig.1.4 The Z-source dc/dc converter with LC filter at the output side

Like every switch mode regulators, Z-source dc/dc converter can operate in two operating modes: continuous current mode (CCM) and discontinuous current mode (DCM). Reffering to Fig.1.4, the proposed Z-source dc/dc converter has two diodes, D_1 and D_2. So, the converter has one CCM and three different DCM of operations such as:

- Continuous Current Mode Operation: In this mode, the currents through the input diode, D_1, and diode, D_2 never fall to zero before the next period starts.
- Discontinuous Current Mode Operation-1: In this mode, the current through the input diode, D_1, falls to zero before the next period beginning, but the current through the diode D_2 never falls to zero for entire period.

- Discontinuous Current Mode Operation-2: In this mode, the current through the diode D_2, falls to zero before the beginning of the next period, but the current through the input diode, D_1, does not fall to zero.
- Discontinuous Current Mode Operation-3: In this mode, both currents through the input diode, D_1, and diode D_2 fall to zero before the beginning of the next period.

In this thesis, only the continuous current mode operation and discontinuous current mode operation-1 are investigated.

1.3 Outline of Thesis

This thesis study is composed of five chapters. The first chapter includes the introduction, aim of the study and the explanation of contents of the chapters. In the second chapter, the theoretical bases of Z-source dc/dc converter are established. The input voltage-to-output voltage relationships, transfer functions, small-signal models of Z-source dc/dc converter in continuous current mode (CCM) and discontinuous current mode (DCM) operations are established. Also, transfer function of controller is derived in chapter two. In chapter three, the derived transfer functions, operating principles of Z-source dc/dc converter are confirmed via SIMPLORER simulations. Besides, the phase margin and gain margin of the controlled converter are determined by MATLAB simulations for both CCM and DCM operations. In chapter four, the experimental results of the circuit are given for both CCM and DCM operations. The simulation results and the experimental results obtained from the prototype circuit are compared. Also, the performance of the controller is shown and power loss on each component is calculated analytically. The fifth and last chapter is a concluding chapter.

CHAPTER 2

THEORETICAL ANALYSIS OF Z-SOURCE DC/DC CONVERTER

2.1 Introduction

In this chapter, operation principles of Z-source dc/dc converter are explained. Input voltage-to-output voltage relationship is derived by analysis for both continuous current mode (CCM) and discontinuous current mode (DCM) operations. Also, the small signal equivalent circuit models are derived for both operation modes. For CCM operation, state space representation method is utilized to derive the small signal equivalent circuit. Additionally, duty factor-to-output voltage and input voltage-to-output voltage transfer functions are attained by using the state equations. Furthermore, duty factor-to-Z-source inductor current and input voltage-to-Z-source inductor current transfer functions are obtained for CCM operation. For peak current control method perturbation and linearization method is utilized to get the control signal-to-output voltage transfer function. Moreover, the small signal equivalent circuit for DCM operation is obtained by utilizing circuit averaging method. Also, the duty factor-to-output voltage and input-voltage-to-output voltage transfer functions are acquired by the analysis of DCM operation equivalent circuit. The boundary between the CCM and DCM operations is found by mathematical equations and finally, the control circuit transfer function is derived.

2.2 Operation Blocks of Z-source Full Bridge DC/DC Converter

Z-source full bridge dc/dc converter is designed for boosting the input voltage to higher output voltage level. The main circuit diagram of the full-bridge Z-source dc/dc converter is shown in Fig.2.1.

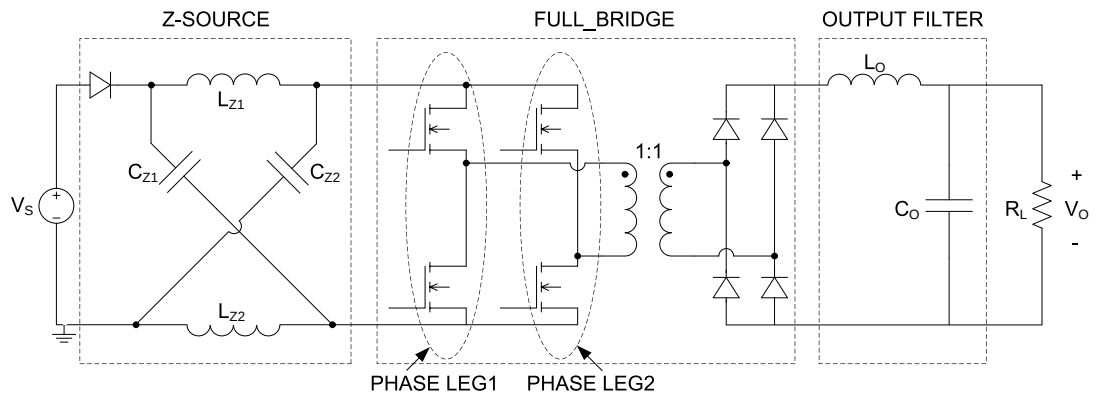

Fig.2.1 Circuit diagram of the Z-source full bridge dc/dc converter

The Z-source part of the converter, shown with dashed part, is used to boost the voltage across the full bridge MOSFETs. Boosting of input voltage is achieved by switching the MOSFETs, in the same line, at the same time. By this way, shoot-through operation is used to energized the Z-source inductors, L_{Z1} and L_{Z2}.

The full bridge part of the circuit is used for isolation and rectification. This part generates ac voltage across the transformer primary side and rectifies the transformer secondary side ac voltage. Simplifying the full bridge part ease the analysis of Z-source dc/dc converter. As mentioned before, in normal operation of Z-source dc/dc converter, one the phase leg shown in Fig.2.1 is shorted to energize the Z-source inductors (L_{Z1} and L_{Z2}) through the Z-source capacitors (C_{Z1} and C_{Z2}). Also, rectification diodes in full bridge part prevents energy flow from output capacitor, C_O, back to the secondary side of transformer. The full bridge part can be replaced by a simple circuital form consisting of a switch, Q_1 and a diode, D_2, as shown in Fig.2.2 without losing anything from the functional features of the bridge. Notable difference is that the electrical isolation between the input and output of the converter in the former is not present in this simplified form. The simplified circuit diagram of Z-source full bridge dc/dc converter, for boosting application, is demonstrated in Fig.2.2.

The output-filter part smoothes the rectified voltage and it constitutes a second order filter. This way, output voltage ripple diminishes dramatically.

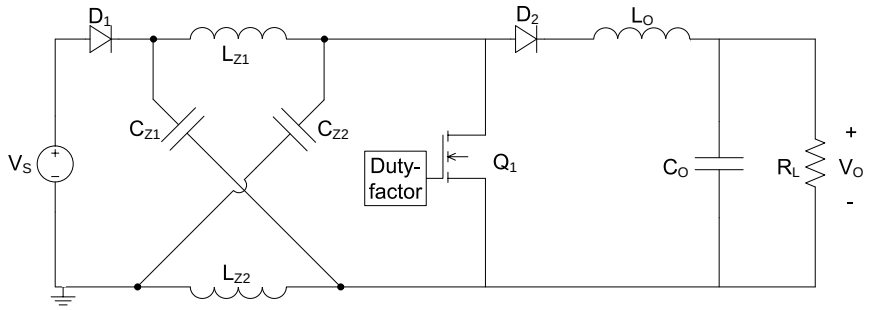

Fig.2.2 Simplified circuit diagram of the Z-source full bridge dc/dc converter

2.3 Analysis of Z-source DC/DC Converter

The analysis of the input voltage to output voltage equation in terms of the duty-factor, D, and other circuit components (inductors, capacitors, load resistance) is made for both in CCM and in DCM operations. Additionally, for both operation modes, the transfer functions and small signal models are derived.

To use the symmetrical behavior of Z-source structure, the Z-source capacitors (C_{Z1} and C_{Z2}) are set equal to each other and Z-source inductors, (L_{Z1} and L_{Z2}) are chosen such as their sizes are same. Then, by the symmetry, voltage waveforms on Z-source inductors come out identical. The current waveforms through Z-source capacitors are also identical over a period. Dc component and small signal components in Z-source capacitor currents are same which is proven at [14]. This fact is same for the inductor voltages as well. So, if

$$L_{Z1} = L_{Z2} = L_Z$$
$$C_{Z1} = C_{Z2} = C_Z \qquad (2.1)$$

is chosen then,

$$
\begin{aligned}
&V_{CZ1}(t) = V_{CZ2}(t) = V_{CZ}(t) \\
&\hat{v}_{CZ1}(t) = \hat{v}_{CZ2}(t) = \hat{v}_{CZ}(t) \\
&V_{LZ1}(t) = V_{LZ2}(t) = V_{LZ}(t) = 0 \\
&\hat{v}_{LZ1}(t) = \hat{v}_{LZ2}(t) = \hat{v}_{LZ}(t) \\
&I_{CZ1}(t) = I_{CZ2}(t) = I_{CZ}(t) = 0 \\
&\hat{i}_{CZ1}(t) = \hat{i}_{CZ2}(t) = \hat{i}_{CZ}(t) \\
&I_{LZ1}(t) = I_{LZ2}(t) = I_{LZ}(t) \\
&\hat{i}_{LZ1}(t) = \hat{i}_{LZ2}(t) = \hat{i}_{LZ}(t)
\end{aligned}
\tag{2.2}
$$

In (2.2), capital letter shows the DC values of currents and voltages of Z-source inductors and Z-source capacitors. The small letters with '^' show the small signal values of currents and voltages.

2.3.1 Mathematical Analysis of Z-source DC/DC Converter in CCM Operation

The circuit diagram of simplified Z-source dc/dc converter can be represented as in Fig.2.3.

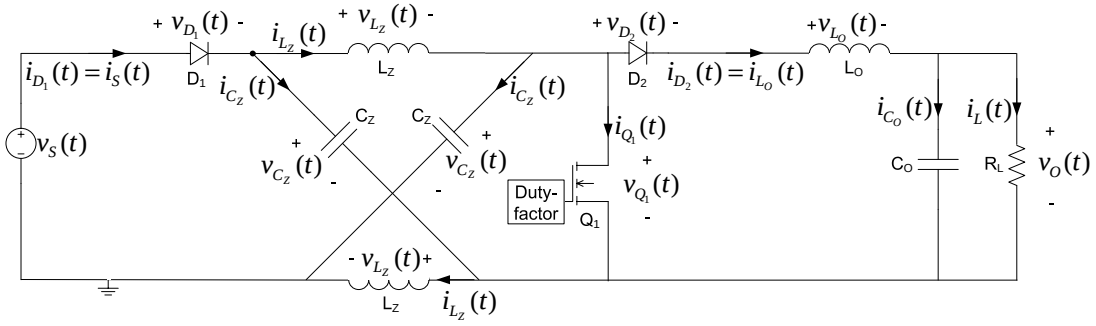

Fig.2.3 Circuit diagram of the Z-source dc/dc converter

In CCM operation, operation of Z-source dc/dc converter in one period can be divided into two modes. Mode 1 begins when switch, Q_1, is switched on at t=0. During this time interval t_1 appearing in Fig.2.6, the Z-source inductors, L_Z, are energized by Z-source capacitors, C_Z. If Kirchhoff's voltage law is applied around LOOP II in Fig.2.4, it can be resulted that Z-source capacitor voltage, $v_{C_Z}(t)$, is equal to Z-source inductor voltage, $v_{L_Z}(t)$, at time interval t_1. Also, using Kirchhoff's voltage law around LOOP I in Fig.2.4, gives an expression for D_1 voltage, $v_{D_1}(t)$. $v_{D_1}(t)$ is equal to $v_S(t)-2v_{C_Z}(t)$. As $v_{C_Z}(t)$ is equal to output voltage, $v_O(t)$, which is proved in (2.14), and $v_S(t)<v_O(t)$ because of boosting operation, $v_{D_1}(t)$ takes negative value. D_1 is reverse biased and does not permit current flow towards source. The load meanwhile is fed by the output inductor, L_O, and output capacitor, C_O. D_2 is clearly forward biased at interval t_1 appearing in Fig.2.6 because the stored energy on L_O forces the current flow through D_2. Also, output inductor voltage, $v_{L_O}(t)$, is equal to $-v_O(t)$ according to LOOP III in Fig.2.4. The equivalent circuit for Mode 1 is represented in Fig.2.4.

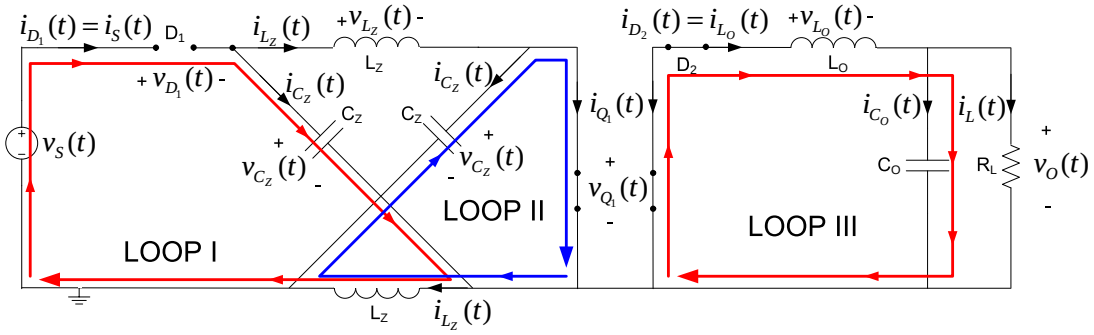

Fig.2.4 Equivalent circuit for Mode 1 in continuous current mode (CCM) operation of the Z-source dc/dc converter

Calling the time elapsed in one cyclic operation of the converter as period, T_S, Mode 2 starts at the instant dT_S when Q_1 switched off at that instant. During the time period in Mode 2, Z-source inductors, L_Z, transfer the stored energies on them to the load. Also, the current drawn from the input is transferred to Z-source capacitors C_Z and load. Inductor L_O is energized during Mode 2. If Kirchhoff's voltage law is applied around LOOP I in Fig.2.5, it can be obtained that the output inductor voltage, $v_{L_O}(t)$, is equal to $2v_{C_Z}(t)-v_S(t)-v_O(t)$ in Mode 2 operation. Similarly, applying Kirchhoff's voltage law at LOOP II brings that Z-source inductor voltage, $v_{L_Z}(t)$, is equal to $v_S(t)-v_{C_Z}(t)$ in Mode 2. The equivalent circuit for Mode 2 is shown in Fig.2.5.

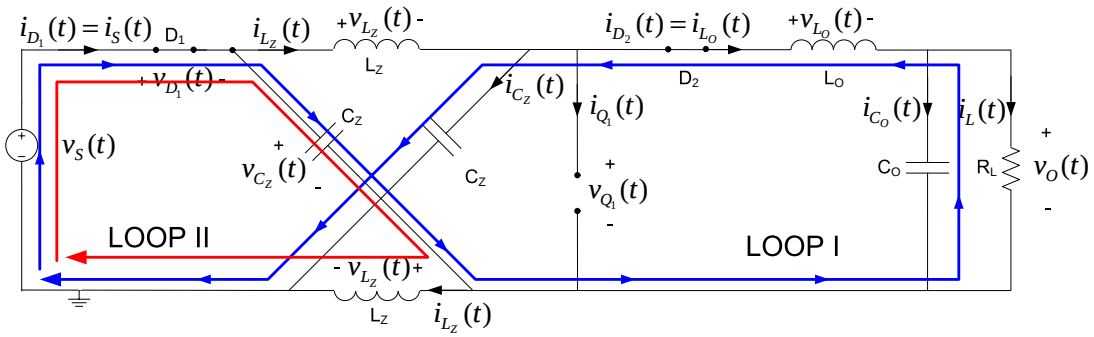

Fig.2.5 Equivalent circuit for Mode 2 in continuous current mode (CCM) operation of the Z-source dc/dc converter

If the capacitor sizes are chosen large enough, the voltage variation across the capacitors over a period is very small in steady state. Also, the input voltage can be determined as constant over a period. Thus, the voltages on capacitors and the input voltage are only dc.

$$v_{CZ}(t) = V_{C_Z}$$
$$v_{CO}(t) = V_{C_O} = V_O \quad (2.3)$$
$$v_S(t) = V_S$$

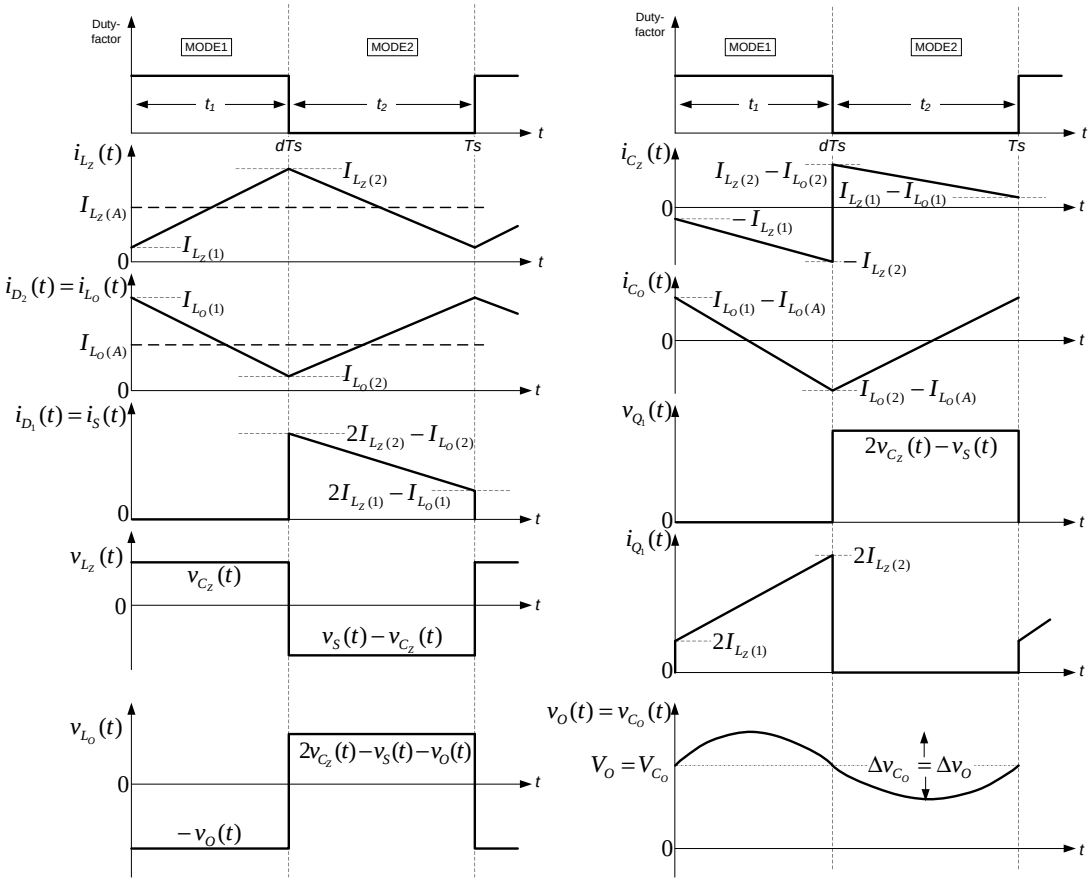

Fig.2.6 Voltage and current waveforms of the inductors (L_Z and L_O), the capacitors (C_Z and C_O) and the nonlinear elements (D_1, D_2, and Q_1) of the Z-source dc/dc converter in CCM operation

The voltages on inductors can be expressed in terms of capacitor voltages and input voltage at any time of period. As the capacitor and input voltages are dc, the voltages on the inductors are dc at any time of the period so, the slope of inductor

current is constant according to (2.4) and the current rises and falls linearly at the inductors. If the capacitor sizes are small, than the voltages across them becomes time dependent. As the voltages of capacitors are time dependent, then the voltages on the inductors become time dependent and this leads to complexity in derivations.

The voltage induced in an inductor due to a current, passing through it, is given by,

$$e_L = L \cdot \frac{di}{dt} \tag{2.4}$$

The voltage and current waveforms of inductors, capacitors and nonlinear elements of the circuit for continuous conduction mode are shown in Fig.2.6. In the figure, $I_{L_Z(A)}$, $I_{L_Z(1)}$ and $I_{L_Z(2)}$ are the abbreviations of average, valley and peak values of Z-source inductors current, respectively. Similarly, $I_{L_O(A)}$, $I_{L_O(1)}$ and $I_{L_O(2)}$ are the abbreviations of average, peak and valley values of output inductor current.

The voltages appearing on inductors, L_Z, are equal to V_{C_Z} in Mode 1 operation, thus considering the differential form of (2.4) expressed in incremental forms of variables then it can be derived;

$$V_{C_Z} = L_Z \cdot \frac{I_{L_Z(2)} - I_{L_Z(1)}}{dT_S} \tag{2.5}$$

or

$$d \cdot T_S \cdot V_{C_Z} = L_Z \cdot \left(I_{L_Z(2)} - I_{L_Z(1)}\right) \tag{2.6}$$

whose left hand side represents volts-second area developed on L_Z inductors during Mode 1 operation. 'd' represents the duty-factor in the equations.

Similarly, the voltage on the Z-source inductors, L_Z, are $V_S - V_{C_Z}$ in Mode 2 so that incremental form of (2.4) yields;

$$(1-d)\cdot T_S\cdot(V_S-V_{C_z})=L_Z\cdot\left(I_{L_z(1)}-I_{L_z(2)}\right) \tag{2.7}$$

whose left hand side represents volts-second area developed on L_Z inductors during Mode 2 operation.

Volt-second areas developed on inductors, L_Z, in one complete switching period, T_S, is to be zero. Using this fact, relationship can be obtained between V_S and V_{C_z}. Sum (2.6) and (2.7) side by side for the purpose so that result will be;

$$V_{C_z}=\frac{(1-d)\cdot V_S}{1-2d} \tag{2.8}$$

Applying the same approach to L_O yields another equation in terms of V_S, V_O and V_{C_z}. The voltage developed on inductor, $v_{L_O}(t)$, at time interval t_1 is

$$v_{L_O(t1)}=-V_O \tag{2.9}$$

Also, in time interval t_2,

$$v_{L_O(t2)}=2V_{C_z}-V_S-V_O \tag{2.10}$$

Since the volt-second area of output inductor, L_O, in one switching cycle is to be zero, again adding (2.9) and (2.10) side by side yields;

$$d\cdot T_S\cdot(-V_O)+(1-d)\cdot T_S\cdot(2V_{C_z}-V_S-V_O)=0 \tag{2.11}$$

Substituting V_{C_z}, obtained in (2.8), into (2.11) gives;

$$\left(d\cdot T_S\cdot(-V_O)\right)+\left((1-d)\cdot T_S\cdot\left(2\cdot\frac{(1-d)V_S}{1-2d}-V_S-V_O\right)\right)=0 \tag{2.12}$$

and which when simplified yields;

$$V_O = \frac{(1-d)\cdot V_S}{1-2d} \tag{2.13}$$

(2.13) gives the relationship between the output voltage, V_O, on the load and the input voltage, V_S, of dc source as function of the duty-factor, d, in CCM operation of Z-source dc/dc converter. Theoretically, it is obvious that the output voltage, V_O, can be adjusted between V_S and infinity. Note that the duty-factor, d, can be of 0.5 maximum, because increasing the duty-factor above 0.5 leads to negative output voltage, which is meaningless. Furthermore, the voltages across the Z-source capacitors, V_{C_z}, are also equal to V_O as depicted by the equality of right hand side (2.8) and (2.13). Therefore,

$$V_{C_z} = V_O \tag{2.14}$$

Generally, in noise sensitive loads, limiting the output voltage ripple in a narrow band is a major demand from switch mode power supplies. Thus, obtaining expressions regarding the output voltage ripple becomes a significant aspect. This requires the use of the ripple current at the capacitor, Δi_{C_O}. The output capacitor used in the circuit eliminates the inductor ripple current, which would be seen by the load. In other words, output capacitor takes the ripple current onto itself as Δi_{C_O} to provide pure current and voltage to the load. If it is assumed that the load ripple current is very small and negligible, then,

$$\Delta i_{L_O} = \Delta i_{C_O} \tag{2.15}$$

Using incremental form of (2.4) on the output inductor, L_O, in Mode 1 one obtains;

$$L_O \cdot \frac{I_{L_O(2)} - I_{L_O(1)}}{dT_S} = -V_O \tag{2.16}$$

or

$$\Delta i_{L_O} = I_{L_O(1)} - I_{L_O(2)} = \frac{V_O \cdot d \cdot T_S}{L_O} \tag{2.17}$$

The peak and valley value of output capacitor current are $\frac{\Delta i_{L_O}}{2}$ and $-\frac{\Delta i_{L_O}}{2}$, respectively. The average value for the capacitor current, I_{C_O}, between the time intervals $\frac{t_1}{2}$ and $\frac{t_2}{2}$ in Fig.2.6, is;

$$I_{C_O} = \frac{\Delta i_{L_O}}{4} = \frac{V_O \cdot d \cdot T_S}{4 \cdot L_O} \tag{2.18}$$

The output capacitor voltage, V_{C_O}, is expressed as;

$$V_{C_O} = \frac{1}{C_O} \int I_{C_O} dt + V_{C_O}(t = 0) \tag{2.19}$$

Peak to peak ripple voltage of the output capacitor, Δv_{C_O}, is;

$$\begin{aligned} \Delta v_{C_O} &= V_{C_O} - V_{C_O}(t = 0) = \frac{1}{C_O} \cdot \int_0^{T_S/2} \frac{\Delta i_{L_O}}{4} dt \\ \Delta v_{C_O} &= \frac{\Delta i_{L_O} \cdot T_S}{8 \cdot C_O} \end{aligned} \tag{2.20}$$

Substituting V_O term given in (2.13), into (2.17) results in an output inductor peak-to-peak current ripple, Δi_{L_O}, expression in terms of V_S, d, T_S and L_O. Substituting that Δi_{L_O} expression into (2.20) yields;

$$\Delta v_{C_O} = \frac{V_S \cdot (1-d) \cdot d \cdot {T_S}^2}{8 \cdot C_O \cdot L_O \cdot (1-2d)} \tag{2.21}$$

(2.21) gives an expression for the output voltage ripple.

Derivation of the inductor ripple currents takes essential part in designing a switch mode power supply. Not only the magnetic core selection and designing, but also determination of the load or frequency that converter passes from CCM operation to DCM operation is directly related to the inductor ripple current.

The ripple currents of Z-source inductors, Δi_{L_z}, can be obtained by reorganizing and summation of (2.6) and (2.7).

Reorganizing (2.6) gives;

$$d \cdot T_S = \frac{L_Z \cdot \left(I_{L_z(2)} - I_{L_z(1)}\right)}{V_{C_z}} \tag{2.22}$$

Reorganizing (2.7) yields;

$$(1-d) \cdot T_S = \frac{L_Z \cdot \left(I_{L_z(2)} - I_{L_z(1)}\right)}{(V_{C_z} - V_S)} \tag{2.23}$$

Summing both sides of (2.22) and (2.23) gives;

$$(1-d) \cdot T_S + d \cdot T_S = T_S = L_Z \cdot \left(I_{L_z(2)} - I_{L_z(1)}\right) \cdot \left(\frac{1}{V_{C_z}} + \frac{1}{V_{C_z} - V_S}\right) \tag{2.24}$$

V_{C_z} can be eliminated by using (2.13) and (2.14) in (2.24) and reorganizing the latter leads to obtain an expression for Z-source inductor current ripple, Δi_{L_z}, in terms of input voltage, V_S, duty-factor, d, period, T_S, and value of Z-source inductor, L_Z.

$$\Delta i_{L_z} = I_{L_z(2)} - I_{L_z(1)} = \frac{(1-d) \cdot d \cdot V_S \cdot T_S}{(1-2d) \cdot L_Z} \tag{2.25}$$

A similar expression for output filter inductor current ripple, Δi_{L_O}, can be obtained by substituting V_O from (2.13) into (2.17) as;

$$\Delta i_{L_O} = I_{L_O(1)} - I_{L_O(2)} = \frac{V_S \cdot (1-d) \cdot d \cdot T_S}{(1-2d) \cdot L_O} \tag{2.26}$$

2.3.2 Determination of Transfer Functions of Z-source DC/DC Converter in CCM Operation

The major feature of switching converter is to provide fixed and non-oscillating output voltage regardless of variations at load current demand and input voltage. Thus, control of a converter plays significant role to fix the output. It is quite understandable that, designing a suitable controller for the converter requires developing the small signal model and transfer function of the power stage.

To obtain the required transfer functions for CCM operation, the state-space averaging method is used. Also, the transfer functions, input voltage-to-output voltage, $G_{vg}(s)$, duty factor-to-output voltage, $G_{vd}(s)$, duty factor-to-Z-source inductor current, $G_{id}(s)$, and input voltage-to-Z-source inductor current, $G_{ig}(s)$, are obtained.

Normally, the only control input to the switch mode power supply is the duty factor. The input voltage and load current variations are out of control. In voltage control method of a converter, the output voltage is sensed and compared by a reference voltage. Duty factor is adjusted until the error between the sensed output voltage and reference voltage is zero. Thus, compensating $G_{vd}(s)$ is enough for voltage control method. Also, the load and input voltage variations should be considered in implementing a controller.

In peak current control method, there are two control loops. In the inner loop, the control circuit limits the peak current of the Z-source inductor. The outer loop compensates the output voltage. The control loop determines directly the current limit of the Z-source inductor current, not the duty-factor. Furthermore, in obtaining

the control-to-output voltage transfer function, $G_{id}(s)$ plays a role with $G_{vd}(s)$ and $G_{ig}(s)$.

2.3.2.1 State Space Representation and Transfer Functions in CCM Operation

The main idea behind the state space representation is linearization and perturbation of the switch mode power supply around an operating point. In normal operation of a converter, the inductor currents and capacitor voltages have only the switching ripples on their dc values. However, at transients, these currents and voltages dc values change slightly for each period. Thus these waveforms include both low frequency components and switching ripple. Averaging the inductor currents and capacitor voltages over a period removes the ripple on the respective waveforms due to the switching. Hence, low frequency components of the waveforms can be modeled. State space representation method allows the changes of averaged values of currents and voltages for each period. In other words, it behaves as a low pass filter to eliminate the switching ripples. Thus, only the low frequency behaviors of inductor currents and capacitor voltages are obtained for an operating point.

The converter contains independent states such as; inductor currents, capacitor voltages, that form the state vector $x(t)$. The converter is fed from an independent source, $u(t)$. When the converter is at Mode 1, the position of switches is fixed and the equivalent reduced circuit in Mode 1 is a linear circuit. During this time interval, the converter can be represented by;

$$\begin{aligned} K\frac{dx(t)}{dt} &= A_1 x(t) + B_1 u(t) \\ y(t) &= C_1 x(t) + E_1 u(t) \end{aligned} \tag{2.27}$$

where K, A_1, B_1, C_1 and E_1 are the matrices which are the coefficients of state vectors and independent source. They are obtained by analyzing the equivalent reduced circuit in Mode 1. $y(t)$ is output vector and it will be chosen as source current to model the input part of the converter.

During the second time interval yielding the operation in Mode 2, the switch positions are altered, so the equivalent reduced circuit changes accordingly so that the linear circuit becomes;

$$K\frac{dx(t)}{dt} = A_2 x(t) + B_2 u(t)$$
$$y(t) = C_2 x(t) + E_2 u(t) \qquad (2.28)$$

where K, A_2, B_2, C_2 and E_2 are coefficient matrices of state vectors and independent source in Mode 2.

A_1, B_1, C_1, E_1, A_2, B_2, C_2 and E_2 matrices are obtained by using the equivalent circuits in Mode 1 and Mode 2. The average values of these matrices over a period gives the average matrices, A, B, C and E.

When the converter is in equilibrium, in steady state, the state space model, which describes the switch mode power supply, is

$$0 = AX + BU$$
$$Y = CX + EU \qquad (2.29)$$

where

$$A = DA_1 + (1-D)A_2$$
$$B = DB_1 + (1-D)B_2$$
$$C = DC_1 + (1-D)C_2$$
$$E = DE_1 + (1-D)E_2 \qquad (2.30)$$

In (2.29) and (2.30) states X, input U, output Y and duty-factor D represent equilibrium (dc) state vector, equilibrium (dc) input, equilibrium (dc) output and equilibrium (dc) duty-factor, respectively.

When (2.29) is solved to find the states and output vectors in equilibrium, one obtains;

$$X = -A^{-1}BU$$
$$Y = (-CA^{-1}B + E)U \tag{2.31}$$

Perturbation and linearization of state vectors about operating point and elimination of dc and higher order terms [16] gives the small signal ac model of the converter such as;

$$K\frac{d\hat{x}(t)}{dt} = A\hat{x}(t) + B\hat{u}(t) + \{(A_1 - A_2)X + (B_1 - B_2)U\}\hat{d}(t)$$
$$\hat{y}(t) = C\hat{x}(t) + E\hat{u}(t) + \{(C_1 - C_2)X + (E_1 - E_2)U\}\hat{d}(t) \tag{2.32}$$

where $\hat{x}(t)$, $\hat{u}(t)$ and $\hat{d}(t)$ are small variations around the operating point.

The detailed expressions for state space averaging method and derivation of equations (2.31) and (2.32) are given in [16].

The independent state vectors of Z-source dc/dc converter are Z-source inductor current, $i_{L_z}(t)$, Z-source capacitor voltage, $v_{C_z}(t)$,output inductor current, $i_{L_o}(t)$, output capacitor voltage, $v_{C_o}(t)$. Hence, the state vector is

$$x(t) = \left[i_{L_z}(t) \quad v_{C_z}(t) \quad i_{L_o}(t) \quad v_{C_o}(t)\right]^T \tag{2.33}$$

The independent source, $v_S(t)$, is stated as input vector, which is the input voltage of the converter.

$$u(t) = \left[v_S(t)\right] \tag{2.34}$$

To model the input port of the Z-source dc/dc converter, the input current, $i_S(t)$ is required. Thus, the input current is chosen as an output vector.

$$y(t) = i_S(t) \tag{2.35}$$

The equivalent circuit of Z-source dc/dc converter for Mode 1 and Mode 2 are represented in Fig.2.4 and Fig.2.5, respectively. If the state equations are derived for the first subinterval from Fig.2.4, Mode 1 state equations are;

$$
\begin{aligned}
L_Z \frac{di_{L_Z}(t)}{dt} &= v_{C_Z}(t) \\
C_Z \frac{dv_{C_Z}(t)}{dt} &= -i_{L_Z}(t) \\
L_O \frac{di_{L_O}(t)}{dt} &= -v_{C_O}(t) \\
C_O \frac{dv_{C_O}(t)}{dt} &= i_{L_O}(t) - \frac{v_{C_O}(t)}{R_L} \\
i_S(t) &= 0
\end{aligned}
\tag{2.36}
$$

If (2.36) is rewritten in matrix form explicitly, then

$$
\begin{bmatrix} L_Z & 0 & 0 & 0 \\ 0 & C_Z & 0 & 0 \\ 0 & 0 & L_O & 0 \\ 0 & 0 & 0 & C_O \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L_Z}(t) \\ v_{C_Z}(t) \\ i_{L_O}(t) \\ v_{C_O}(t) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 \\ 0 & 0 & 1 & -1/R_L \end{bmatrix} \begin{bmatrix} i_{L_Z}(t) \\ v_{C_Z}(t) \\ i_{L_O}(t) \\ v_{C_O}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_S(t)]
$$

$$
[i_S(t)] = [0 \quad 0 \quad 0 \quad 0] \begin{bmatrix} i_{L_Z}(t) \\ v_{C_Z}(t) \\ i_{L_O}(t) \\ v_{C_O}(t) \end{bmatrix} + [0][v_S(t)]
\tag{2.37}
$$

Establishing the equalities between (2.27) and (2.37) the matrices K, A_1, and the vectors B_1, C_1 and E_1 can be determined as;

$$
K = \begin{bmatrix} L_Z & 0 & 0 & 0 \\ 0 & C_Z & 0 & 0 \\ 0 & 0 & L_O & 0 \\ 0 & 0 & 0 & C_O \end{bmatrix}, A_1 = \begin{bmatrix} 0 & 1 & 0 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 \\ 0 & 0 & 1 & -1/R_L \end{bmatrix}, B_1 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}
\tag{2.38}
$$

$$
C_1[0 \quad 0 \quad 0 \quad 0], E_1 = [0]
$$

Similarly finding the coefficients of, A_2, B_2, C_2 and E_2, the state equations are written for the subinterval 2 utilizing Fig.2.5. The state equations for Mode 2 are,

$$
\begin{aligned}
L_Z \frac{di_{L_z}(t)}{dt} &= v_S(t) - v_{C_z}(t) \\
C_Z \frac{dv_{C_z}(t)}{dt} &= i_{L_z}(t) - i_{L_o}(t) \\
L_O \frac{di_{L_o}(t)}{dt} &= 2 \cdot v_{C_z}(t) - v_{C_o}(t) - v_S(t) \\
C_O \frac{dv_{C_o}(t)}{dt} &= i_{L_o}(t) - \frac{v_{C_o}(t)}{R_L} \\
i_S(t) &= 2 \cdot i_{L_z}(t) - i_{L_o}(t)
\end{aligned}
\tag{2.39}
$$

Reorganizing the equations in (2.39) explicitly and in matrix form one obtains;

$$
\begin{aligned}
K\frac{d}{dt}\begin{bmatrix} i_{L_z}(t) \\ v_{C_z}(t) \\ i_{L_o}(t) \\ v_{C_o}(t) \end{bmatrix} &= \begin{bmatrix} 0 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 0 & 2 & 0 & -1 \\ 0 & 0 & 1 & -1/R_L \end{bmatrix}\begin{bmatrix} i_{L_z}(t) \\ v_{C_z}(t) \\ i_{L_o}(t) \\ v_{C_o}(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ -1 \\ 0 \end{bmatrix}\begin{bmatrix} v_S(t) \end{bmatrix} \\
\begin{bmatrix} i_S(t) \end{bmatrix} &= \begin{bmatrix} 2 & 0 & -1 & 0 \end{bmatrix}\begin{bmatrix} i_{L_z}(t) \\ v_{C_z}(t) \\ i_{L_o}(t) \\ v_{C_o}(t) \end{bmatrix} + \begin{bmatrix} 0 \end{bmatrix}\begin{bmatrix} v_S(t) \end{bmatrix}
\end{aligned}
\tag{2.40}
$$

so A_2, B_2, C_2 and E_2 are defined as;

$$
A_2 = \begin{bmatrix} 0 & -1 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 0 & 2 & 0 & -1 \\ 0 & 0 & 1 & -1/R_L \end{bmatrix}, B_2 = \begin{bmatrix} 1 \\ 0 \\ -1 \\ 0 \end{bmatrix}, C_2 = \begin{bmatrix} 2 & 0 & -1 & 0 \end{bmatrix}, E_2 = \begin{bmatrix} 0 \end{bmatrix}
\tag{2.41}
$$

Substitution of A_1, B_1, C_1, E_1, A_2, B_2, C_2, E_2 into (2.30) gives A, B, C and E as;

$$A = DA_1 + (1-D)A_2 = \begin{bmatrix} 0 & 2D-1 & 0 & 0 \\ 1-2D & 0 & -(1-D) & 0 \\ 0 & 2(1-D) & 0 & -1 \\ 0 & 0 & 1 & -1/R_L \end{bmatrix}$$

$$B = DB_1 + (1-D)B_2 = \begin{bmatrix} 1-D \\ 0 \\ D-1 \\ 0 \end{bmatrix} \tag{2.42}$$

$$C = DC_1 + (1-D)C_2 = \begin{bmatrix} 2(1-D) & 0 & -(1-D) & 0 \end{bmatrix}$$

$$E = DE_1 + (1-D)E_2 = \begin{bmatrix} 0 \end{bmatrix}$$

A, B, C and E known, the average values of inductor currents, capacitor voltages and input current can be found by substituting them in (2.31) so that;

$$X = \begin{bmatrix} I_{L_z} \\ V_{C_z} \\ I_{L_O} \\ V_{C_O} \end{bmatrix} = \begin{bmatrix} (D-1)^2 / R_L(1-2D)^2 \\ 1-D/1-2D \\ (1-D)/R_L(1-2D) \\ 1-D/1-2D \end{bmatrix} \cdot V_S \tag{2.43}$$

$$Y = \begin{bmatrix} I_S \end{bmatrix} = \begin{bmatrix} \frac{(1-D)^2}{(1-2D)^2 R_L} \end{bmatrix} \cdot V_S$$

Elements of X and Y in (2.43) represent equilibrium dc values. Note that the terms resulting for V_{C_z} and V_{Co} (which is equal to output voltage, V_O) in (2.43) are is exactly same as those obtained in (2.14). Hence, state space representation gives the same results with the analytical solution of the circuit.

The small signal matrix representation of Z-source dc-dc converter given in (2.32) can be obtained by substituting explicit forms of K, A, B, C, E, A_1, B_1, C_1, E_1, A_2, B_2, C_2 and E_2 matrices into (2.32). After the mathematical calculations and simplifications, the result can be put into a compact form;

$$K\frac{d}{dt}\begin{bmatrix}\hat{i}_{L_z}(t)\\ \hat{v}_{C_z}(t)\\ \hat{i}_{L_o}(t)\\ \hat{v}_{C_o}(t)\end{bmatrix}=A\begin{bmatrix}\hat{i}_{L_z}(t)\\ \hat{v}_{C_z}(t)\\ \hat{i}_{L_o}(t)\\ \hat{v}_{C_o}(t)\end{bmatrix}+B[\hat{v}_S(t)]+\begin{bmatrix}2V_{C_z}-V_S\\ I_{L_o}-2I_{L_z}\\ V_S-2V_{C_z}\\ 0\end{bmatrix}[\hat{d}(t)]$$
$$[\hat{i}_S(t)]=C\begin{bmatrix}\hat{i}_{L_z}(t)\\ \hat{v}_{C_z}(t)\\ \hat{i}_{L_o}(t)\\ \hat{v}_{C_o}(t)\end{bmatrix}+\begin{bmatrix}-2 & 0 & 1 & 0\end{bmatrix}\begin{bmatrix}I_{L_z}\\ V_{C_z}\\ I_{L_o}\\ V_{C_o}\end{bmatrix} \quad (2.44)$$

where $\hat{i}_{L_z}(t)$, $\hat{v}_{C_z}(t)$, $\hat{i}_{L_o}(t)$, $\hat{v}_{C_o}(t)$ and $\hat{i}_S(t)$ represent the small variations around the operating point of Z-source inductor current, Z-source capacitor voltage, output inductor current, output capacitor voltage and input current, respectively.

To model the Z-source dc/dc converter, (2.44) is rewritten in analytical form rather than matrix form. Equations obtained represent the subcircuits corresponding to the state variables considered. Combining the subcircuits gives the total small signal circuit of Z-source dc/dc converter. The total small signal circuit can be used to derive the transfer functions of input voltage-to-output voltage, $G_{vg}(s)$, duty factor-to-output voltage, $G_{vd}(s)$, duty factor-to-Z-source inductor current, $G_{id}(s)$, and input voltage-to-Z-source inductor current, $G_{ig}(s)$. Besides, the same transfer functions can be found directly from (2.44). Rewriting (2.44) in analytical form gives the result such as,

$$\begin{aligned}
L_Z\frac{d\hat{i}_{L_z}(t)}{dt}&=(2D-1)\hat{v}_{C_z}(t)+(1-D)\hat{v}_S(t)+(2V_{C_z}-V_S)\hat{d}(t)\\
C_Z\frac{d\hat{v}_C(t)}{dt}&=(1-2D)\hat{i}_{L_z}(t)+(I_{L_o}-2I_{L_z})\hat{d}(t)+(D-1)\hat{i}_{L_o}(t)\\
L_O\frac{d\hat{i}_{L_o}(t)}{dt}&=(2-2D)\hat{v}_{C_z}(t)-\hat{v}_{C_o}(t)+(D-1)\hat{v}_S(t)-(2V_{C_z}-V_S)\hat{d}(t)\\
C_O\frac{d\hat{v}_{C_o}(t)}{dt}&=\hat{i}_{L_o}(t)-\frac{\hat{v}_{C_o}(t)}{R_L}\\
\hat{i}_S(t)&=(2-2D)\hat{i}_{L_z}(t)+(D-1)\hat{i}_{L_o}(t)+(I_{L_o}-2I_{L_z})\hat{d}(t)
\end{aligned} \quad (2.45)$$

To find the transfer functions, the Laplace transform of (2.45) is written so that;

$$
\begin{aligned}
sL_Z\hat{i}_{L_Z}(s) &= (2D-1)\hat{v}_{C_Z}(s) + (1-D)\hat{v}_S(s) + (2V_{C_Z} - V_S)\hat{d}(s) \\
sC_Z\hat{v}_{C_Z}(s) &= (1-2D)\hat{i}_{L_Z}(s) + (I_{L_O} - 2I_{L_Z})\hat{d}(s) + (D-1)\hat{i}_{L_O}(s) \\
sL_O\hat{i}_{L_O}(s) &= (2-2D)\hat{v}_{C_Z}(s) - \hat{v}_{C_O}(s) + (D-1)\hat{v}_S(s) - (2V_{C_Z} - V_S)\hat{d}(s) \\
sC_O\hat{v}_{C_O}(s) &= \hat{i}_{L_O}(s) - \frac{\hat{v}_{C_O}(s)}{R_L} \\
s\hat{i}_S(s) &= (2-2D)\hat{i}_{L_Z}(s) + (D-1)\hat{i}_{L_O}(s) + (I_{L_O} - 2I_{L_Z})\hat{d}(s)
\end{aligned}
\tag{2.46}
$$

In Fig.2.9, the small signal of output voltage, $\hat{v}_{C_O}(s) = \hat{v}_O(s)$, is the summation of $\hat{d}(s)\cdot G_{vd}(s)$ and $\hat{v}_S(s)\cdot G_{vg}(s)$. Thus, to find $G_{vd}(s)$, $\hat{v}_S(s)$ is set as zero in (2.46) and similarly, to find $G_{vg}(s)$, $\hat{d}(s)$ is set to zero in (2.46). $G_{vd}(s)$ can be expressed as;

$$
G_{vd}(s) = \left.\frac{\hat{v}_{C_O}(s)}{\hat{d}(s)}\right|_{\hat{v}_S(s)=0} = \left.\frac{\hat{v}_O(s)}{\hat{d}(s)}\right|_{\hat{v}_S(s)=0} = \frac{\alpha_1 s^2 + \alpha_2 s + \alpha_3}{\beta_1 s^4 + \beta_2 s^3 + \beta_3 s^2 + \beta_4 s + \beta_5} \tag{2.47}
$$

where,

$$
\begin{aligned}
\alpha_1 &= -\frac{L_Z \cdot C_Z \cdot V_S}{(1-2D)} \\
\alpha_2 &= \frac{(D-1)\cdot V_S \cdot L_Z \cdot (2-2D)}{R_L \cdot (1-2D)^2} \\
\alpha_3 &= V_S \\
\beta_1 &= L_Z \cdot C_Z \cdot L_O \cdot C_O \\
\beta_2 &= \frac{L_Z \cdot L_O \cdot C_Z}{R_L} \\
\beta_3 &= \left[L_O \cdot C_O \cdot (1-2D)^2\right] + \left[L_Z \cdot C_Z\right] + \left[2\cdot(1-D)^2 \cdot L_Z \cdot C_O\right] \\
\beta_4 &= \left[\frac{L_O}{R_L}\cdot(1-2D)^2\right] + \left[\frac{2L_Z}{R_L}\cdot(1-D)^2\right] \\
\beta_5 &= (1-2D)^2
\end{aligned}
$$

Input voltage-to-output voltage transfer function, $G_{vg}(s)$, can be obtained by setting $\hat{d}(s)$ to zero as;

$$G_{vg}(s)=\frac{\hat{v}_{C_O}(s)}{\hat{v}_S(s)}\bigg|_{\hat{d}(s)=0}=\frac{\hat{v}_O(s)}{\hat{v}_S(s)}\bigg|_{\hat{d}(s)=0}=\frac{\eta_1 s^2+\eta_2 s+\eta_3}{\beta_1 s^4+\beta_2 s^3+\beta_3 s^2+\beta_4 s+\beta_5} \tag{2.48}$$

where,

$$\eta_1=-L_Z\cdot C_Z\cdot(1-D)$$
$$\eta_2=0$$
$$\eta_3=\left[2\cdot(1-D)^2\cdot(1-2D)\right]-\left[(1-D)\cdot(1-2D)^2\right]$$

(2.46) can similarly be used to obtain duty factor-to-Z-source inductor current, $G_{id}(s)$, and input voltage-to-Z-source inductor current, $G_{ig}(s)$, transfer functions. From Fig.2.9, the small signal of Z-source inductor current, $\hat{i}_{L_Z}(s)$, is the summation of $\hat{d}(s)\cdot G_{id}(s)$ and $\hat{v}_S(s)\cdot G_{ig}(s)$. Thus to determine $G_{id}(s)$, $\hat{v}_S(s)$ is set to zero and to find $G_{ig}(s)$, $\hat{d}(s)$ is set to zero in (2.46).

Duty factor-to-Z-source inductor current transfer function, $G_{id}(s)$, can be obtained as;

$$G_{id}(s)=\frac{\hat{i}_{L_Z}(s)}{\hat{d}(s)}\bigg|_{\hat{v}_S(s)=0}=\frac{\lambda_1 s^3+\lambda_2 s^2+\lambda_3 s+\lambda_4}{\beta_1 s^4+\beta_2 s^3+\beta_3 s^2+\beta_4 s+\beta_5} \tag{2.49}$$

where,

$$\lambda_1=\frac{V_S\cdot L_O\cdot C_O\cdot C_Z}{2\cdot(1-D)\cdot(1-2D)}$$
$$\lambda_2=\frac{C_Z\cdot L_O\cdot V_S}{2\cdot R_L\cdot(1-2D)\cdot(1-D)}+\frac{(1-D)\cdot V_S\cdot L_O\cdot C_O}{R_L\cdot(1-2D)}$$
$$\lambda_3=\frac{C_Z\cdot V_S}{2\cdot(1-2D)\cdot(1-D)}+\frac{(1-D)\cdot V_S\cdot L_O}{{R_L}^2\cdot(1-2D)}+\frac{V_S\cdot C_O}{2\cdot(1-2D)}$$
$$\lambda_4=\frac{(1-D)\cdot V_S}{2\cdot R_L\cdot(1-2D)\cdot(1-D)}+\frac{(1-D)\cdot V_S}{R_L\cdot(1-2D)}$$

Input voltage-to-Z-source inductor current, $G_{ig}(s)$, can be obtained by setting $\hat{d}(s)=0$ in (2.46), such as;

$$G_{ig}(s)=\frac{\hat{i}_{L_Z}(s)}{\hat{v}_S(s)}\bigg|_{\hat{d}(s)=0}=\frac{\mu_1 s^3+\mu_2 s^2+\mu_3 s+\mu_4}{\beta_1 s^4+\beta_2 s^3+\beta_3 s^2+\beta_4 s+\beta_5} \tag{2.50}$$

where,

$$\mu_1 = L_O \cdot C_O \cdot C_Z \cdot (1-D)$$
$$\mu_2 = \frac{C_Z \cdot L_O \cdot (1-D)}{R_L}$$
$$\mu_3 = \left[C_O \cdot (1-D)^2 \cdot (2D-1)\right]+\left[C_Z \cdot (1-D)\right]+\left[C_O \cdot 2(1-D)^3\right]$$
$$\mu_4 = \frac{(1-D)^2 \cdot (2D-1)}{R_L}+\frac{2 \cdot (1-D)^3}{R_L}$$

Note that denominators of $G_{vd}(s)$, $G_{vg}(s)$, $G_{id}(s)$ and $G_{ig}(s)$ are exactly the same.

2.3.2.2 Peak Current Control Method Transfer Functions in CCM Operation

In current control method, Z-source peak inductor current is controlled, and the control affects directly the inductor current, not the output voltage. The aim of converter control, on the other hand, is regulating the output voltage. This, however, requires the derivation of the control circuit output-to-output voltage transfer function, $G_{vc}(s)$.

The duty-factor generation in peak current control method is shown in Fig.2.7. By using this figure and algebra $G_{vc}(s)$ can be determined.

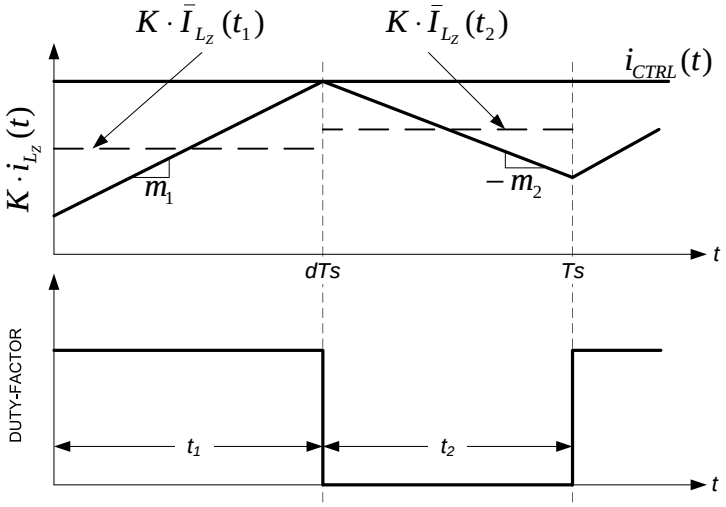

Fig.2.7 Duty-factor generation in peak current control method of CCM operation

It is assumed that, Z-source inductor current is measured by a current sensor, and measured quantity is multiplied by a constant, K. Thus, in Fig.2.7, Z-source inductor current waveform is drawn as $K \cdot i_{L_z}(t)$. In inductor peak current control method, when duty factor is 'high', measured inductor current is increasing up to the value of control signal, $i_{CTRL}(t)$. Once the inductor current reaches the control signal, duty factor becomes 'low' and inductor currents starts and continues decreasing until the end of the T_S. The slope of current is directly proportional to the inductor voltage. From Fig.2.6, it can be determined that, the voltage across the Z-source inductor is $v_{C_z}(t)$, within time interval t_1. The inductor voltage is, however, $(v_S(t) - v_{C_z}(t))$ within the time interval t_2. Thus, slopes m_1 and m_2 can be calculated from (2.4) as;

$$m_1 = \frac{v_{C_z}(t)}{K \cdot L_Z} \tag{2.51}$$

$$m_2 = \frac{v_{C_z}(t) - v_S(t)}{K \cdot L_Z} \tag{2.52}$$

In steady-state operation, Z-source inductor currents at $t = 0$ and $t = T_s$ are same. However, in transient this does not hold. The measured average current, $K \cdot \bar{I}_{L_z}(t)$, of the Z-source inductor within the period, T_s, is calculated for value of the each time intervals t_1 and t_2 individually. The measured average current, $K \cdot \bar{I}_{L_z}(t_1)$, of the Z-source inductor within the time interval t_1 can be written as;

$$K \cdot \bar{I}_{L_z}(t_1) = \bar{I}_{CTRL}(t) - \left(\frac{m_1 \cdot d \cdot T_S}{2} \right) \tag{2.53}$$

$\bar{I}_{CTRL}(t)$ is the average value of the control signal within the period, T_s, under consideration. Similarly the measured average current, $K \cdot \bar{I}_{L_z}(t_2)$, of the Z-source inductor within the time interval t_2 is;

$$K \cdot \bar{I}_{L_z}(t_2) = \bar{I}_{CTRL}(t) - \left(\frac{m_2 \cdot (1-d) \cdot T_S}{2} \right) \tag{2.54}$$

From Fig.2.7, for one switching cycle, the average value of the inductor current can be calculated as;

$$K \cdot \bar{I}_{L_z}(t) = \left(K \cdot d \cdot \bar{I}_{L_z}(t_1)\right) + \left(K \cdot (1-d) \cdot \bar{I}_{L_z}(t_2)\right) \tag{2.55}$$

Substitution of (2.53) and (2.54) into (2.55) gives the result as,

$$K \cdot \bar{I}_{L_z}(t) = \bar{I}_{CTRL}(t) - \left(\frac{m_1 \cdot d^2 \cdot T_S}{2} \right) - \left(\frac{m_2 \cdot (1-d)^2 \cdot T_S}{2} \right) \tag{2.56}$$

Perturbation and linearization of (2.56) gives the small signal values of current control method. To find the small signal value, firstly, the terms in (2.56) are written as summation of dc value and small signal value such as,

$$\bar{I}_{L_Z}(t) = I_{L_Z} + \hat{i}_{L_Z}(t)$$
$$\bar{I}_{CTRL}(t) = I_{CTRL} + \hat{i}_{CTRL}(t)$$
$$d = D + \hat{d}(t) \qquad (2.57)$$
$$m_1 = \frac{v_{C_Z}(t)}{L_Z} = \frac{V_{C_Z}}{L_Z} + \frac{\hat{v}_{C_Z}(t)}{L_Z}$$
$$m_2 = \frac{v_{C_Z}(t) - v_S(t)}{L_Z} = \frac{V_{C_Z} - V_S}{L_Z} + \frac{\hat{v}_{C_Z}(t) - \hat{v}_S(t)}{L_Z}$$

where I_{L_Z}, I_{CTRL}, D, V_{C_Z} and V_S are the representation of dc values of Z-source inductor current, control signal, duty-factor, Z-source capacitor voltage and the input voltage. Also, $\hat{i}_{L_Z}(t)$, $\hat{i}_{CTRL}(t)$, $\hat{d}(t)$, $\hat{v}_{C_Z}(t)$ and $\hat{v}_S(t)$ are the small signal ac values of these terms.

Substituting the terms in (2.57) into (2.56), taking only the first order terms into consideration thus neglecting dc and high order terms, the Laplace transform of the resulting equation leads to;

$$K \cdot \hat{i}_{L_Z}(s) = \hat{i}_{CTRL}(s) + \chi_1 \hat{v}_S(s) + \chi_2 \hat{d}(s) + \chi_3 \hat{v}_{C_Z}(s) \qquad 2.58)$$

where

$$\chi_1 = \frac{T_S \cdot (1-D)^2}{2 \cdot K \cdot L_Z}$$
$$\chi_2 = \frac{T_S \cdot \left(-(4 \cdot D - 2) \cdot V_{C_Z} - (2 - 2 \cdot D) \cdot V_S\right)}{2 \cdot K \cdot L_Z}$$
$$\chi_3 = \frac{T_S \cdot \left(-2 \cdot D^2 + 2 \cdot D - 1\right)}{2 \cdot K \cdot L_Z}$$

Small signal value of Z-source capacitor voltage, $\hat{v}_{C_Z}(t)$, is determined in terms of $\hat{i}_{L_Z}(s)$, $\hat{v}_O(s)$ and $\hat{d}(s)$ using (2.46). By manipulating these equations, $\hat{v}_{C_Z}(t)$ is found as;

$$\hat{v}_{C_z}(s) = \frac{\psi_2(s)}{\psi_1(s)}\hat{d}(s) + \frac{\psi_3(s)}{\psi_1(s)}\hat{v}_S(s) + \frac{\psi_4(s)}{\psi_1(s)}\hat{v}_O(s) \tag{2.59}$$

where,

$$\psi_1 = sC_Z + \frac{(1-2D)^2}{sL_Z}$$
$$\psi_2 = \frac{(1-2D)\cdot(2V_{C_z} - V_S)}{sL_Z} + \frac{(D-1)\cdot V_S}{(1-2D)^2 \cdot R_L}$$
$$\psi_3 = \frac{(1-2D)\cdot(1-D)}{sL_Z}$$
$$\psi_4 = (D-1)\cdot\left(sC_O + \frac{1}{R_L}\right)$$

By substituting $\hat{v}_{C_z}(t)$ value into (2.58) and manipulating the equation to leave $\hat{d}(s)$ at one side results in,

$$F_M \cdot \hat{d}(s) = \hat{i}_{CTRL}(s) - \left(F_L \cdot \hat{i}_{L_z}(s)\right) - \left(F_O \cdot \hat{v}_O(s)\right) - \left(F_V \cdot \hat{v}_S(s)\right) \tag{2.60}$$

where,

$$F_M = \chi_2 + \left(\chi_3 \cdot \frac{\psi_2(s)}{\psi_1(s)}\right)$$
$$F_L = K$$
$$F_O = -\left(\chi_3 \cdot \frac{\psi_4(s)}{\psi_1(s)}\right)$$
$$F_V = -\left(\chi_1 + \chi_3 \cdot \frac{\psi_3(s)}{\psi_1(s)}\right)$$

Functional block diagram of peak current controller corresponding to (2.60) is shown in Fig.2.8. By Fig.2.8, control signal-to-duty factor block diagram has been obtained. The next step is to find control signal-to-output voltage, $G_{vc}(s)$, and input voltage-to-output voltage, $G_{vg-pcm}(s)$, transfer functions by utilizing $G_{vd}(s)$, $G_{id}(s)$, $G_{ig}(s)$ and

$G_{vg}(s)$. If the Z-source dc/dc converter transfer functions are inserted to Fig.2.8, the whole block diagrams results. Fig.2.9 shows this overall block diagram for peak current control method of the Z-source dc/dc converter in CCM operation.

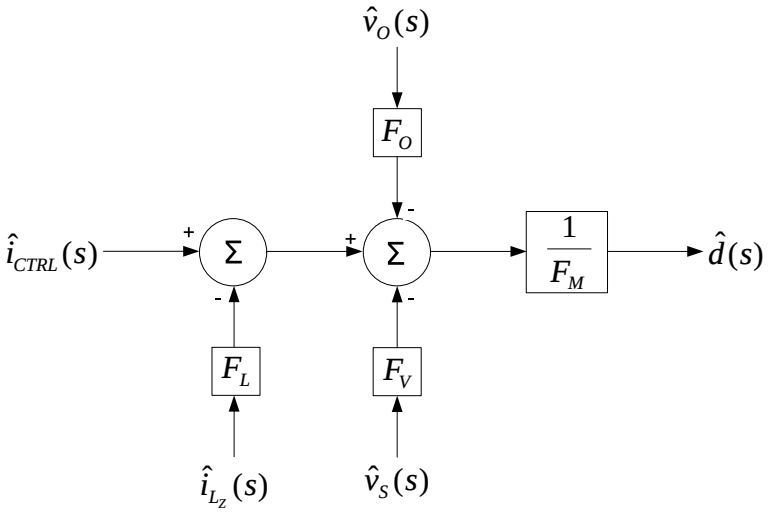

Fig.2.8 Functional block diagram of peak current controller in CCM operation

As in Fig.2.9, small signal value of output voltage is the sum of $\hat{d}(s)\cdot G_{vd}(s)$ and $\hat{v}_s(s)\cdot G_{vg}(s)$. Also, $\hat{v}_O(s)$ is input signal to the F_O block as in Fig.2.8. Small signal value of Z-source inductor current is the sum of the terms $\hat{d}(s)\cdot G_{id}(s)$ and $\hat{v}_s(s)\cdot G_{ig}(s)$. Besides, $\hat{i}_{L_Z}(s)$ is the input signal to the F_L block. Thus, block diagram in Fig.2.9 can be used to get expressions for $G_{vc}(s)$ and $G_{vg-pcm}(s)$. Setting $\hat{v}_S(s)$ to zero and analyzing the block diagram in Fig.2.9 gives the transfer function of control signal-to-output voltage, $G_{vc}(s)$.

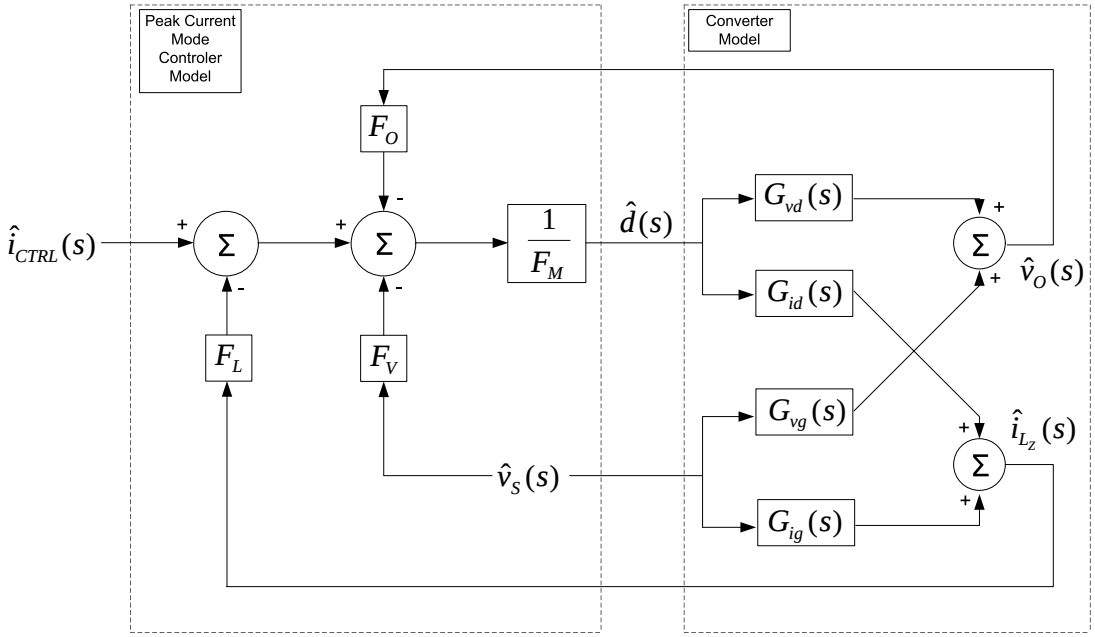

Fig.2.9 Functional block diagram of the Z-source dc/dc converter in CCM operation

$$G_{vc}(s) = \left.\frac{\hat{v}_O(s)}{\hat{i}_{CTRL}(s)}\right|_{\hat{v}_S(s)=0} = \frac{G_{vd}}{F_M + F_L \cdot G_{id} + F_O \cdot G_{vd}} \tag{2.61}$$

Also, for peak current control method, the input voltage-to-output voltage transfer function, $G_{vg-pcm}(s)$, can be determined by setting $\hat{i}_{CTRL}(s)$ equal to zero in Fig.2.9. The resulting expression for $G_{vg-pcm}(s)$ is;

$$G_{vg-pcm}(s) = \left.\frac{\hat{v}_O(s)}{\hat{v}_S(s)}\right|_{\hat{i}_{CTRL}(s)=0} = \frac{F_M G_{vg} + F_L G_{id} G_{vg} - F_L G_{ig} G_{vd} - F_V G_{vd}}{F_M + F_L G_{id} + F_O G_{vd}} \tag{2.62}$$

2.3.3 Developing the Small Signal Model of Z-source DC/DC Converter in CCM Operation

(2.45) describes inductor voltages, capacitor currents and input currents. The first equation at (2.45) gives the small signal value of Z-source inductor voltage,

$L_Z \dfrac{d\hat{i}_{L_z}(t)}{dt}$, in terms of the small signal values of Z-source capacitor voltage, $\hat{v}_{C_z}(t)$, source voltage, $\hat{v}_S(t)$, and duty factor, $\hat{d}(t)$. By using this equation, which is also given at (2.63), a closed loop circuit can be drawn. In Fig.2.10, the small signal circuit for Z-source inductor is shown. In other words, the circuit in Fig.2.10 is the circuit representation of (2.63). The second equation at (2.45), which is also given at (2.64), describes the small signal value of Z-source capacitor current, $C_Z \dfrac{d\hat{v}_{C_z}(t)}{dt}$, in terms of small signal values of Z-source inductor current, $\hat{i}_{L_z}(t)$, duty factor, $\hat{d}(t)$, and output inductor current, $\hat{i}_{L_O}(t)$. By using (2.64), the small signal circuit for Z-source capacitor can be drawn which is shown in Fig.2.11. Similarly, the small signal circuits of output inductor, output capacitor and input port of the converter are shown in Fig.2.12, Fig.2.13 and Fig.2.14, respectively. Related equations for these circuits are given at (2.65), (2.66) and (2.67). Also these equations are the third, fourth and fifth equations of (2.45), respectively.

$$L_Z \frac{d\hat{i}_{L_z}(t)}{dt} = (2D-1)\hat{v}_{C_z}(t) + (1-D)\hat{v}_S(t) + (2V_{C_z} - V_S)\hat{d}(t) \qquad (2.63)$$

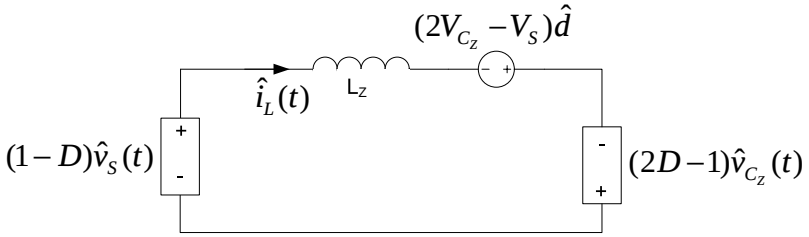

Fig.2.10 Equivalent circuit for (2.63) (the small signal circuit of the Z-source inductor)

The loop current in Fig.2.10 is the Z-source inductor current $\hat{i}_{L_z}(t)$, and the emf induced in this inductor, $L_Z(d\hat{i}_{L_z}(t)/dt)$, is equal to the sum of the other three

voltage sources. Two of them $(2D-1)\hat{v}_{C_z}(t)$ and $(1-D)\hat{v}_S(t)$ are dependent sources because they are driven by state value, $\hat{v}_{C_z}(t)$, and input vector, $\hat{v}_S(t)$. These dependent sources are used to combine the small signal circuit with other small signal circuits of inductors and capacitors. This way overall small signal circuit of the converter is obtained. The third source present in the loop with voltage $(2V_{C_z}-V_S)\hat{d}(t)$ is driven by small signal value of duty factor, $\hat{d}(t)$, and this term is represented as independent voltage source. Furthermore, due to the presence of two Z-source inductors in Z-source dc/dc converter, there are two circuits in overall small signal model, shown in Fig.2.10.

$$C_Z \frac{d\hat{v}_{C_z}(t)}{dt} = (1-2D)\hat{i}_{L_z}(t) + (I_{L_O} - 2I_{L_z})\hat{d}(t) + (D-1)\hat{i}_{L_O}(t) \tag{2.64}$$

(2.64) describes the small signal model of the Z-source capacitor, C_Z. The capacitor current depends according to three other current sources. $(1-2D)\hat{i}_{L_z}(t)$ and $(D-1)\hat{i}_{L_O}(t)$ terms are dependent sources because they are driven by state values $\hat{i}_{L_z}(t)$ and $\hat{i}_{L_O}(t)$. These dependent sources are eventually combined to other dependent source in overall small signal model. $(I_{L_O} - 2I_{L_z})\hat{d}(t)$ is small signal current source due to duty-factor, $\hat{d}(t)$ and represented as independent current source. Apart from that, being of two Z-source capacitor in the main circuit leads to two state equivalent circuit, shown in Fig.2.11, in overall small signal model.

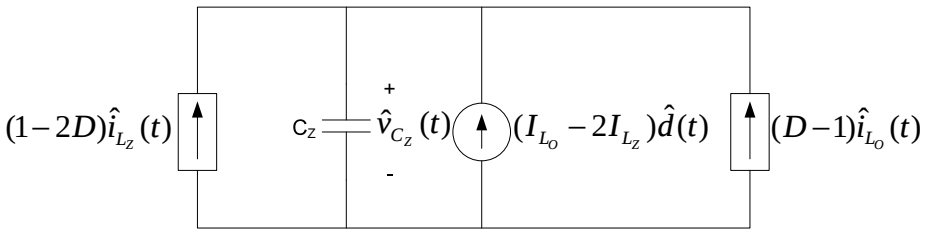

Fig.2.11 Equivalent circuit for (2.64) (the small signal circuit of the Z-source capacitor)

$$L_O \frac{d\hat{i}_{L_o}(t)}{dt} = (2-2D)\hat{v}_{C_z}(t) - \hat{v}_{C_o}(t) + (D-1)\hat{v}_S(t) - (2V_{C_z} - V_S)\hat{d}(t) \tag{2.65}$$

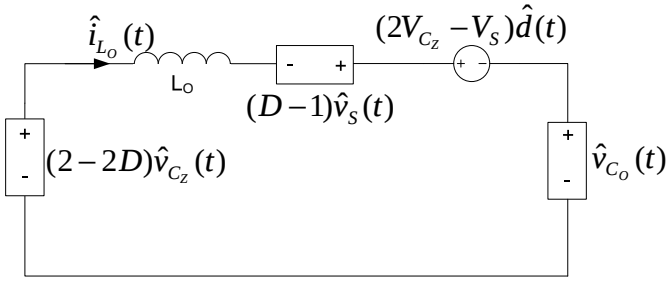

Fig.2.12 Equivalent circuit for (2.65) (the small signal circuit of the output inductor)

The loop current in Fig.2.12 is the output inductor current, $\hat{i}_{L_o}(t)$, and the emf on the inductor due to this loop current, $L_O(d\hat{i}_{L_o}(t)/dt)$, is equal to the sum of the other three voltage sources. Sources with voltages $(2-2D)\hat{v}_{C_z}(t)$ and $(D-1)\hat{v}_S(t)$ in Fig.2.12 are dependent sources because they are driven by state value $\hat{v}_{C_z}(t)$ and input vector $\hat{v}_S(t)$. The source with a voltage $(2V_{C_z} - V_S)\hat{d}(t)$ is driven by duty factor, $\hat{d}(t)$, is represented as independent voltage source.

$$C_O \frac{d\hat{v}_{C_o}(t)}{dt} = \hat{i}_{L_o}(t) - \frac{\hat{v}_{C_o}(t)}{R_L} \tag{2.66}$$

Fig.2.13 represents the equivalent circuit of the output capacitor, C_O, small signal model. Note that the capacitor current here depends only to the output inductor small signal current, $\hat{i}_{L_o}(t)$, and the load resistance, R_L. $\hat{i}_{L_o}(t)$ is a dependent current source because it is driven by a state value, $\hat{i}_{L_o}(t)$.

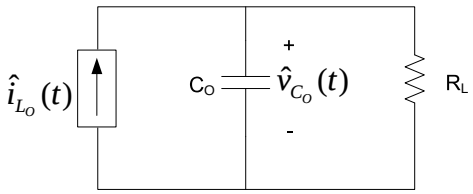

Fig.2.13 Equivalent circuit for (2.66) (the small signal circuit of the output capacitor)

$$\hat{i}_S(t) = (2-2D)\hat{i}_{L_z}(t) + (D-1)\hat{i}_{L_O}(t) + (I_{L_O} - 2I_{L_z})\hat{d}(t) \tag{2.67}$$

The circuit in Fig.2.14 represents the small signal current, $\hat{i}_S(t)$, drawn from the source with voltage, $\hat{v}_S(t)$. The small signal ac input current is equal to sum of the currents in three branches. The first $(2-2D)\hat{i}_{L_z}(t)$ and second $(D-1)\hat{i}_{L_O}(t)$ branches are dependent sources of the ac Z-source inductor current, $\hat{i}_{L_z}(t)$, and ac output inductor current, $\hat{i}_{L_O}(t)$, respectively. The third branch is driven by the control input, $\hat{d}(t)$, thus, it is represented as a independent current source.

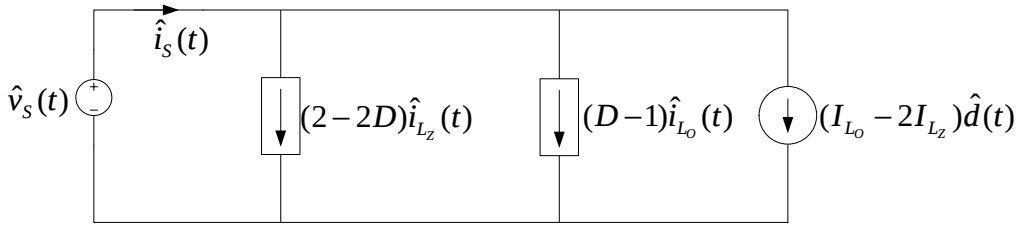

Fig.2.14 Equivalent circuit for (2.67) (the small signal circuit of the input current)

Combining the all these circuits shown in Fig.2.10, Fig.2.11, Fig.2.12, Fig.2.13 and Fig.2.14 representing the state equations individually, through ideal transformers

gives the overall small signal model of the Z-source dc/dc converter in continuous current mode.

Combination of dependent source $(2D-1)\hat{v}_{C_z}(t)$ in Fig.2.10 and dependent source $(1-2D)\hat{i}_{L_z}(t)$ in Fig.2.11 with ideal transformer is shown in Fig.2.15.

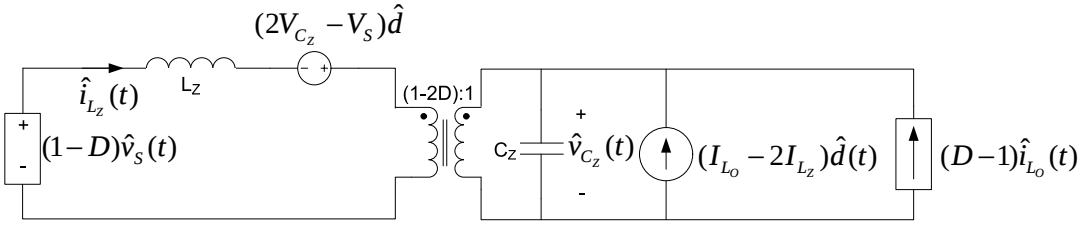

Fig.2.15 Combination of the dependent sources $(2D-1)\hat{v}_{C_z}(t)$ in Fig.2.10 and $(1-2D)\hat{i}_{L_z}(t)$ in Fig.2.11

Fig.2.15 shows the combination of one Z-source inductor and one Z-source capacitor. In fact there are two identical such subcircuits, as shown in Fig.2.15 because in Z-source structure there are two inductors and capacitors, in reality.

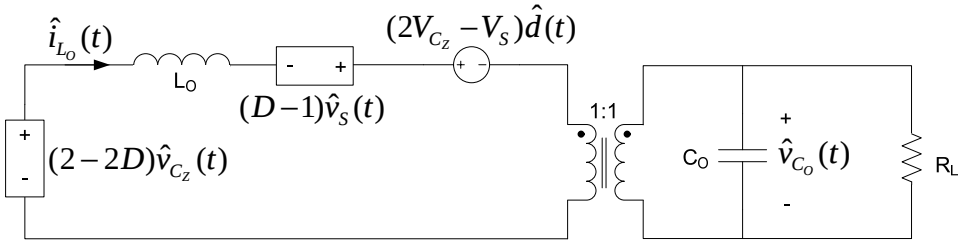

Fig.2.16 Combination of the dependent sources $\hat{v}_{C_o}(t)$ in Fig.2.12 and $\hat{i}_{L_o}(t)$ in Fig.2.13

Integrating the dependent sources $\hat{v}_{C_O}(t)$ of Fig.2.12 and $\hat{i}_{L_O}(t)$ of Fig.2.13 gives the result shown in Fig.2.16.

The overall small signal model of the Z-source dc/dc converter can be obtained by combining the circuits in Fig.2.14, Fig.2.15 and Fig.2.16. Dependent sources are assembled together to constitute ideal transformers. The dependent sources $(2-2D)\hat{i}_{L_z}(t)$, of Fig.2.14, and $(2-2D)\hat{v}_{C_z}(t)$, of Fig.2.16, are separated into two equal dependent sources as $(1-D)\hat{i}_{L_z}(t)$ and $(1-D)\hat{v}_{C_z}(t)$, respectively. Total small signal circuit with dependent sources is represented in Fig.2.17. After combining the dependent sources with ideal transformers, the small signal model of the Z-source dc/dc converter is achieved. The small signal model is shown in Fig.2.18. By using small signal model, the converter transfer functions, $G_{vd}(s)$, $G_{vg}(s)$, $G_{id}(s)$ and $G_{ig}(s)$, can also be attained and the results will be exactly the same as founded in (2.47), (2.48), (2.49) and (2.50).

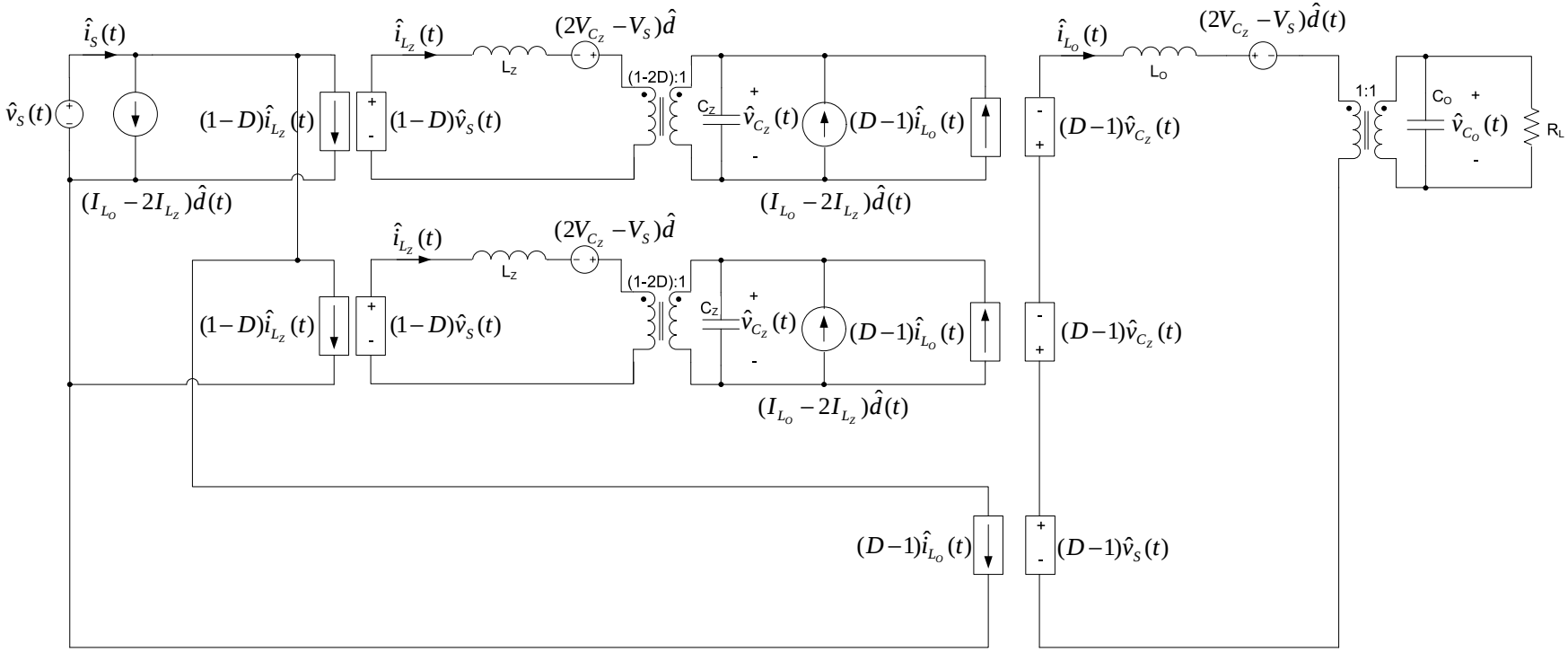

Fig.2.17 Combination of the small signal circuits in Fig.2.14, Fig.2.15 and Fig.2.16

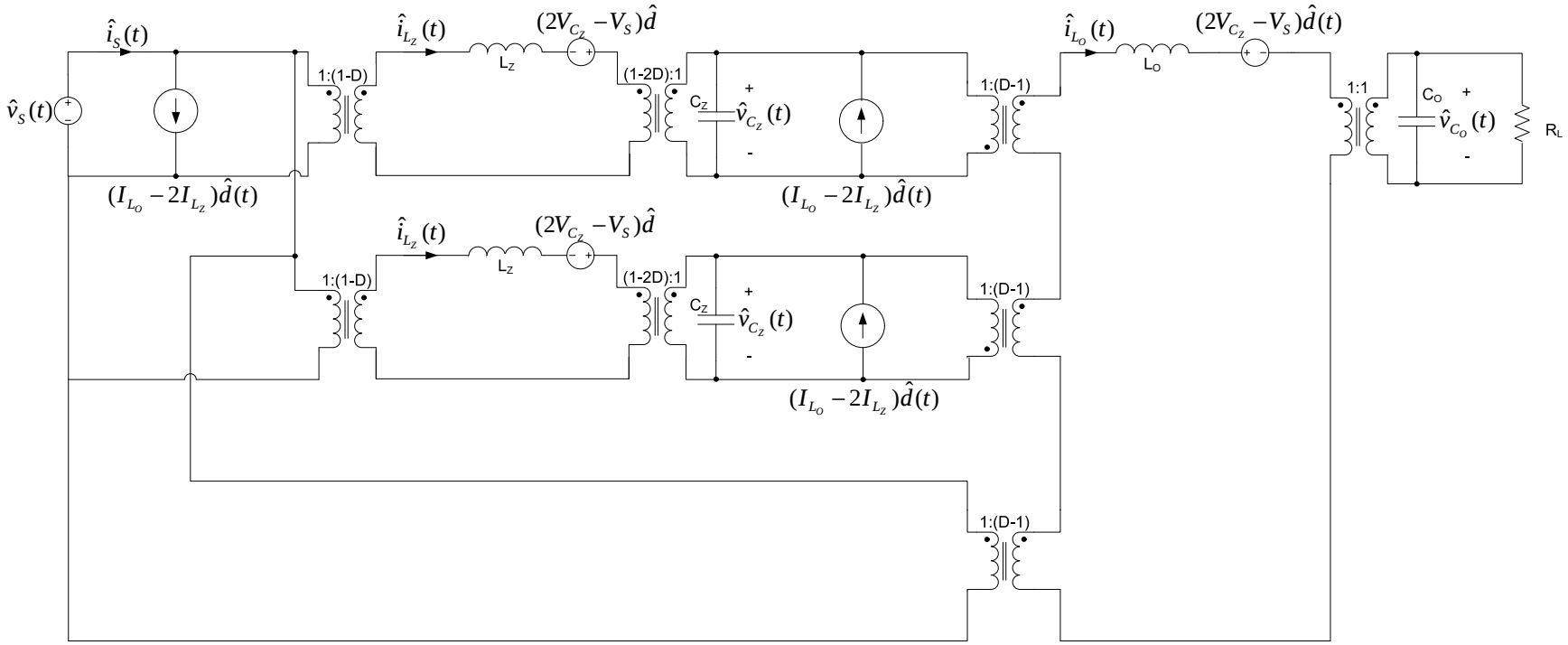

Fig.2.18 Total small signal circuit of the Z-source dc/dc converter

2.3.4 Mathematical Analysis of Z-source DC/DC Converter in DCM Operation

In some applications, power requirement of the load may change in a large extent. Dc/dc converter may be forced to work in discontinuous current mode (DCM) operation at light loads. Also, to reduce the size of the inductor, DCM operation can be chosen at nominal operating condition of dc/dc converter. The analysis of dc/dc converters in DCM operation will be of interest for the designer.

Z-source is different than the other basic dc/dc converter topologies from the DCM operation point of view. In DCM operations in buck, boost or buck-boost converters the energy transfer inductor current becomes zero for a time period in a single switching period; however, this is not an issue in Z-source dc/dc converter. At certain interval of switching period, the currents at the Z-source and output inductors are not zero but they are purely DC value. Ascending or descending behaviors of the currents in inductors at this time interval vanish although there is a current flow through the inductors.

The DCM operation of Z-source dc/dc converter can be divided into three modes such as Mode 1, Mode 2 and Mode 3. Mode 1 begins when switch, Q_1, is switched on at $t = 0$ and remains there during the time interval, t_1 in which the Z-source inductor, L_Z stores energy drawn from the Z-source capacitor, C_Z. The reverse bias on diode D_1 prevents conduction of it so that the input current is zero. During Mode 1 operation the output inductor, L_O, and output capacitor, C_O, feed the load together. Diode D_2 is kept forward biased by the emf produced by the output inductor, L_O, forcing the current flow through the D_2. An equivalent circuit can be developed for the Z-source dc/dc converter operating in Mode 1 as shown in Fig.2.19.

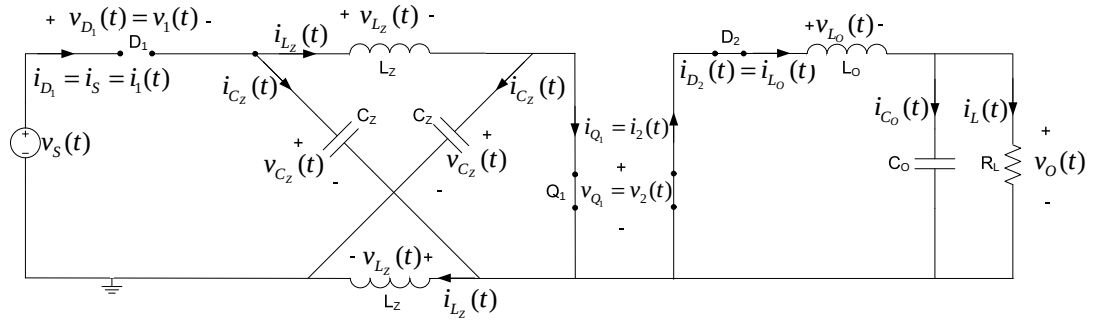

Fig.2.19 Equivalent circuit for Mode 1 in discontinuous current mode (DCM) operation of Z-source dc/dc converter

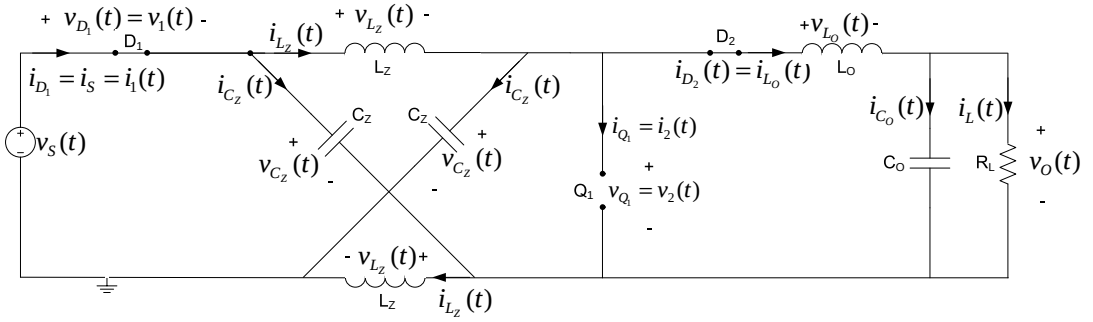

Fig.2.20 Equivalent circuit for Mode 2 in discontinuous current mode (DCM) operation of the Z-source dc/dc converter

Mode 2 operation of Z-source dc/dc converter starts when the switch, Q_1, is switched off and remains in this mode during time interval, t_2 in which Z-source inductor, L_Z, transfers the stored energy to the output. D_1 being forward biased this time a current is drawn from the source and it is transferred to the Z-source capacitors, C_Z, and to the output as well. The output inductor, L_O, and the output capacitor, C_O, both start storing energy in this mode to compensate their expenses which resulted in the previous mode. Mode 2 ends when the source current drawn

from the input decays to zero. An equivalent circuit accounting for Mode 2 operation can be developed as shown in Fig.2.20.

When the diode current, $i_{D1}(t)$, goes to zero, Mode 3 operation in DCM starts. In Mode 3 the diode, D_1, becomes once again reverse biased ensuring the blocking against any current flow from the source. The load is fed by the storage elements Z-source capacitors, C_Z, and output capacitor, C_O. The voltages induced on both Z-source inductors and the output inductor are zero during the Mode 3 time interval, t_3. Thus, there are no ascending or descending variations in currents which flow through these inductors. Thus, it can be assumed that currents in the inductors are purely DC at Mode 3. An equivalent circuit which will be developed for the converter operating in Mode 3 is as shown in Fig.2.21.

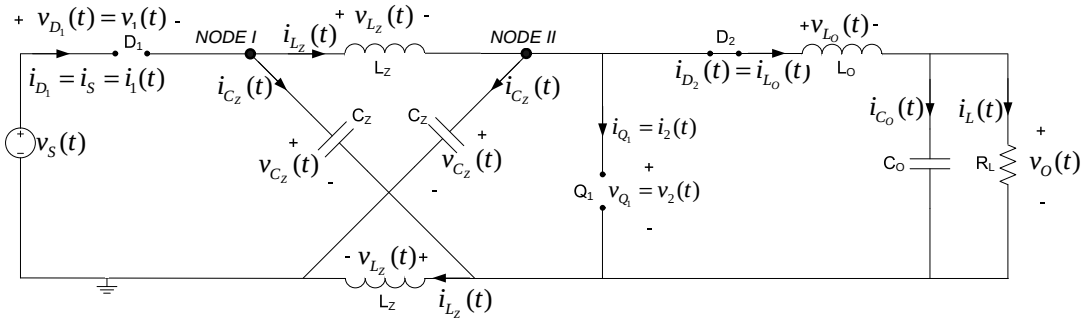

Fig.2.21 Equivalent circuit for Mode 3 in discontinuous current mode (DCM) operation of the Z-source dc/dc converter

In discontinuous current mode analysis, it is assumed that variations both on the voltage across the capacitors and the source voltage are negligibly small. For steady state analysis of converter in DCM operation, the voltages across Z-source capacitor, source and output are dc values which are represented by V_{C_Z}, V_S and V_O respectively. Waveforms for the voltages and currents belonging to capacitors,

inductors, diodes and switch in the converter will result in the form shown in Fig.2.22, respectively.

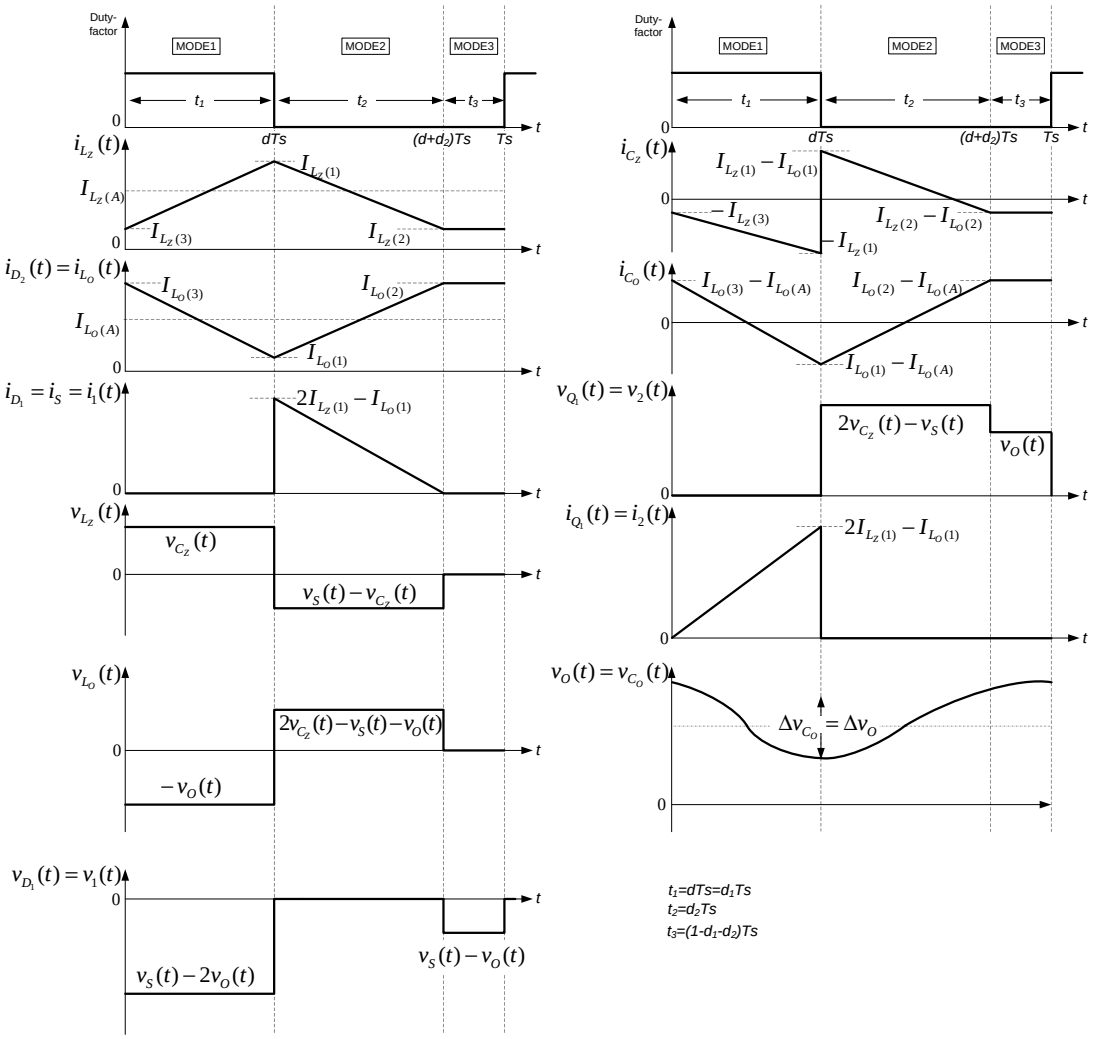

Fig.2.22 Voltage and current waveforms of the inductors (L_Z and L_O), the capacitors (C_Z and C_O) and the nonlinear elements (D_1, D_2, and Q_1) of the Z-source dc/dc converter in DCM operation

During the time interval, t_1, from Fig.2.19, it can be easily derived that the instantaneous voltage across the Z-source inductor, $v_{L_z}(t)\big|_{t1}$, is equal to the Z-source capacitor voltage, V_{C_z}. Also, the instantaneous voltage across the output inductor, $v_{L_o}(t)\big|_{t1}$, can be obtained as negative value of output voltage, $-V_O$. As the voltages across the inductors are dc, the current rises and falls linearly through the inductors.

$$v_{L_z}(t)\big|_{t1} = V_{C_z} \tag{2.68}$$

and,

$$v_{L_o}(t)\big|_{t1} = -V_O \tag{2.69}$$

From Fig.2.20, it can be determined that, in Mode 2, the Z-source instantaneous inductor voltage, $v_{L_z}(t)\big|_{t2}$, is;

$$v_{L_z}(t)\big|_{t2} = V_S - V_{C_z} \tag{2.70}$$

and the output instantaneous inductor voltage, $v_{L_o}(t)\big|_{t2}$, is;

$$v_{L_o}(t)\big|_{t2} = 2V_{C_z} - V_S - V_O \tag{2.71}$$

Referring to Fig.2.21, the total voltage across the Z-source inductor and the output inductor in Mode 3 can be found as;

$$v_{L_z}(t)\big|_{t3} + v_{L_o}(t)\big|_{t3} = V_{C_z} - V_O \tag{2.72}$$

Over one switching period, Ts, individual average voltages appearing on both Z-source inductor, V_{L_z}, and output inductor, V_{L_o}, are zero at steady state. If the

equations of average voltages of inductors are written, equations (2.73) and (2.74) are obtained.

$$V_{L_z} = \left(t_1 \cdot v_{L_z}(t)\Big|_{t1}\right) + \left(t_2 \cdot v_{L_z}(t)\Big|_{t2}\right) + \left(t_3 \cdot v_{L_z}(t)\Big|_{t3}\right) = 0 \tag{2.73}$$

$$V_{L_o} = \left(t_1 \cdot v_{L_o}(t)\Big|_{t1}\right) + \left(t_2 \cdot v_{L_o}(t)\Big|_{t2}\right) + \left(t_3 \cdot v_{L_o}(t)\Big|_{t3}\right) = 0 \tag{2.74}$$

Substituting (2.68)-(2.72), into (2.73) and (2.74) yields;

$$V_{C_z} = V_O \tag{2.75}$$

From (2.75), it can be obviously seen that, the dc voltage across the Z-source capacitor is equal to the output voltage. Thus, after this point, in equations, instead of Z-source capacitor voltage term, V_{C_z}, the output voltage term, V_O, will be used for the analysis of DCM operation.

In establishing a relationship between the input voltage, V_S, and the output voltage, V_O, it is assumed that the converter is a lossless system so that the power drawn from the input is same with the power delivered to the load.

Referring to Fig.2.21, writing the node equation at NODE I for Mode 3 operation gives;

$$i_{L_z}(t)\Big|_{t3} + i_{C_z}(t)\Big|_{t3} = 0 \tag{2.76}$$

Similarly the node equation at NODE II for time interval t_3 gives;

$$i_{L_z}(t)\Big|_{t3} - i_{C_z}(t)\Big|_{t3} - i_{L_o}(t)\Big|_{t3} = 0 \tag{2.77}$$

Combination of (2.76) and (2.77) and elimination of Z-source capacitor current at time interval t_3, $i_C(t)\Big|_{t3}$, results in,

$$i_{L_O}(t)\Big|_{t3} = 2i_{L_Z}(t)\Big|_{t3} \tag{2.78}$$

(2.78) is valid for only Mode 3 operation. From (2.78) and Fig.2.22, it can be concluded that;

$$I_{L_O(2)} = 2 \cdot I_{L_Z(2)} \tag{2.79}$$

and

$$I_{L_O(3)} = 2 \cdot I_{L_Z(3)} \tag{2.80}$$

After this point, in case of $I_{L1(2)}$ and $I_{L1(3)}$ terms, the equivalents of them stated in (2.79) and (2.80) is used, respectively.

If the back emf Z-source inductor written for the for time interval $t_1 = d \cdot T_S$, than;

$$V_{C_Z} = V_O = L_Z \frac{I_{L_Z(1)} - I_{L_Z(3)}}{t_1} = L_Z \frac{I_{L_Z(1)} - I_{L_Z(3)}}{dT_S} \tag{2.81}$$

or

$$I_{L_Z(1)} - I_{L_Z(3)} = \frac{V_O \cdot d \cdot T_S}{L_Z} \tag{2.82}$$

The back emf of output inductor for time interval $t_1 = dT_S$ also leads to;

$$-V_O = L_O \frac{I_{L_O(1)} - I_{L_O(3)}}{t_1} = L_O \frac{I_{L_O(1)} - \left(2 \cdot I_{L_Z(3)}\right)}{dT_S} \tag{2.83}$$

or,

$$I_{L_O(1)} - I_{L_O(3)} = I_{L_O(1)} - \left(2 \cdot I_{L_Z(3)}\right) = \frac{-V_O \cdot d \cdot T_S}{L_O} \tag{2.84}$$

In Mode 2 operation, the back emf of Z-source inductor, L_Z, and output inductor, L_O, is given in equations (2.85) and (2.86), respectively.

$$I_{L_Z(2)} - I_{L_Z(1)} = \frac{(V_S - V_{C_Z}) \cdot d_2 \cdot T_S}{L_Z} = \frac{(V_S - V_O) \cdot d_2 \cdot T_S}{L_Z} \tag{2.85}$$

$$I_{L_O(2)} - I_{L_O(1)} = 2I_{L_Z(2)} - I_{L_O(1)} = \frac{(2V_{C_Z} - V_S - V_O) \cdot d_2 \cdot Ts}{L_O} = \frac{(V_O - V_S) \cdot d_2 \cdot T_S}{L_O} \tag{2.86}$$

In Mode 3 operation, the back emf of L_Z and L_O are given as;

$$v_{L_z}(t)\Big|_{t3} = L_Z \frac{I_{L_Z(3)} - I_{L_Z(2)}}{t_3} = L_Z \frac{I_{L_Z(3)} - I_{L_Z(2)}}{(1 - d - d_2) \cdot T_S} \tag{2.87}$$

$$v_{L_o}(t)\Big|_{t3} = L_O \frac{I_{L_O(3)} - I_{L_O(2)}}{t_3} = L_Z \frac{2I_{L_Z(3)} - 2I_{L_Z(2)}}{(1 - d - d_2)T_S} = L_Z \frac{2(I_{L_Z(3)} - I_{L_Z(2)})}{(1 - d - d_2)T_S} \tag{2.88}$$

If (2.87) and (2.88) are summed and equated to the (2.72), the result is;

$$v_{L_z}(t)\Big|_{t3} + v_{L_o}(t)\Big|_{t3} = (L_Z + L_O) \cdot \frac{I_{L_O(3)} - I_{L_O(2)}}{t_3} = V_{C_z} - V_O \tag{2.89}$$

Using (2.72) and (2.75) together gives a result as;

$$v_{L_z}(t)\Big|_{t3} + v_{L_o}(t)\Big|_{t3} = V_{C_z} - V_O = 0 \tag{2.90}$$

(2.89) and (2.90) gives;

$$v_{L_z}(t)\Big|_{t3} + v_{L_O}(t)\Big|_{t3} = (L_Z + L_O)\cdot\frac{I_{L_O(3)} - I_{L_O(2)}}{t_3} = V_{C_z} - V_O = 0 \tag{2.91}$$

Which implies that ($I_{L_O(3)} - I_{L_O(2)}$) must be zero. Thus, it can be concluded that,

$$I_{L_O(3)} = I_{L_O(2)} \tag{2.92}$$

Combining the (2.79), (2.80) and (2.92) yields;

$$I_{L_z(3)} = I_{L_z(2)} \tag{2.93}$$

From (2.92) and (2.93), it is understand that changes in currents of Z-source inductors and output inductor are zero at time interval t_3. This condition implies that the voltage induced across the inductors is zero during this time interval.

$$v_{L_z}(t)\Big|_{t3} = v_{L_O}(t)\Big|_{t3} = 0 \tag{2.94}$$

Expressing the d_2 value in terms of duty-factor, input voltage and output voltage is necessary to drive the input-output relationship in discontinuous current mode. When (2.93) is inserted into (2.82), then;

$$I_{L_z(1)} - I_{L_z(2)} = \frac{V_O \cdot d \cdot T_S}{L_Z} \tag{2.95}$$

The summing (2.95) and (2.85) gives on the left hand side zero. Thus,

$$(I_{L_z(2)} - I_{L_z(1)}) + (I_{L_z(1)} - I_{L_z(2)}) = 0 = \frac{(V_S - V_O)\cdot d_2 \cdot T_S}{L_Z} + \frac{V_O \cdot d \cdot T_S}{L_Z} \tag{2.96}$$

from which d_2 can be found as;

$$d_2 = \frac{V_O \cdot d}{(V_O - V_S)} \tag{2.97}$$

Recalling the assumption made before about the converter that is a losses system then,

$$P_{in} = P_{OUT} = \frac{V_O{}^2}{R_L} \tag{2.98}$$

with

$$P_{in} = I_S \cdot V_S \tag{2.99}$$

where I_S is average value of input current over one switching cycle at steady state. From Fig.2.22, I_S can be found as;

$$I_S = \frac{\left(2 \cdot I_{L_Z(1)}\right) - I_{L_O(1)}}{2} \cdot d_2 \tag{2.100}$$

Substituting the I_S into (2.98) and (2.99) the result can be put into the following form;

$$\left(2 \cdot I_{L_Z(1)}\right) - I_{L_O(1)} = \frac{2 \cdot V_O{}^2}{R_L \cdot d_2 \cdot V_S} \tag{2.101}$$

and rearranging (2.84) meanwhile gives;

$$I_{L_O(1)} - \left(2 \cdot I_{L_Z(3)}\right) = -\frac{V_O \cdot d \cdot T_S}{L_O} \tag{2.102}$$

Summing (2.101) and (2.102) side by side results in;

$$2(I_{L_Z(1)} - I_{L_Z(3)}) = \left(\frac{2 \cdot V_O{}^2}{R_L \cdot d_2 \cdot V_S} \right) - \left(\frac{V_O \cdot d \cdot T_S}{L_O} \right) \quad (2.103)$$

Substituting the expression (2.82) into (2.103) after simplifying the resulting equation the relationship between input voltage and output voltage is obtained as;

$$\frac{V_O}{V_S} = 1 + \left(\frac{1}{L_O} + \frac{2}{L_Z} \right) \cdot \frac{R_L \cdot d^2 \cdot T_S}{2} \quad (2.104)$$

(2.104) give the relationship between the output voltage and input voltage in discontinuous current mode of Z-source dc/dc converter at steady state. In continuous current mode the ratio of output voltage over input voltage only depends on duty-factor, d . However, in discontinuous current mode the ratio depends on not only duty-factor but also size of inductors, load resistance, and switching frequency. If the inductances and switching frequency are assumed to be constant after the design finalized, it is obvious that the output voltage becomes load dependent in discontinuous current mode.

2.3.5 Developing the Small Signal Model of Z-source DC/DC Converter in DCM Operation

To obtain the small signal model and transfer functions of the Z-source dc/dc converter in CCM operation state-space averaging method was utilized. In discontinuous current mode operation the circuit averaging method is used. At transients, the dc values of inductor currents and capacitor voltages change much smaller than switching frequency. Eliminating the switching ripple from the inductor currents and capacitor voltages waveforms gives the responses of these waveforms to transients. In state space averaging method, the states of the circuit, inductor currents and capacitor voltages, are written in matrix form for all modes of operation individually. Then, the coefficient matrices are averaged over one switching period as at (2.42). The main idea behind the circuit averaging is same as the state space averaging. Both techniques are based on averaging the circuit over one switching period, T_S , and eliminating the switching ripple. In circuit averaging method, the time

varying waveforms of the circuit is averaged directly over a switching cycle, T_S, although state space averaging method uses state equations.

Essentials of the circuit averaging method are replacing the nonlinear elements (diodes and transistors) with dependent and independent voltage or current sources. The average values of the voltage and current waveforms belonging to each nonlinear will be derived in terms of independent sources (such as input voltage, V_S, and duty-factor, d) and the state variables (inductor currents and capacitor voltages) for the purpose. At steady state the inductor current values at the beginning and at the end of a switching cycle is equal to each other. However at transients, this is not the case because the average value of inductor current changes slightly at the end of the switching cycle. Thus, at transients, averaging the inductor current over T_S gives the dc value and the small ac value of the current for that switching cycle. The same case is valid for the capacitor voltages. The average value of components currents and voltages, $\overline{\bullet}$, where $\bullet$ represents the average current or voltage of components within the period T_S under consideration, have a dc and small signal ac value at transients. Consider the voltage waveform, $v_1(t)$, across D_1, shown in Fig.2.22, the average value, $\overline{V}_1(t)$, of the diode D_1 voltage within in the period T_S under consideration is calculated as;

$$\overline{V}_1(t) = \frac{1}{T_S}\int_{t_1}^{t_1+T_S} v_1(t)dt = V_1 + \hat{v}_1 \tag{2.105}$$

V_1 is the dc value of $\overline{V}_1(t)$ and $\hat{v}_1$ is the small signal ac value of $v_1(t)$. By using the waveform of the $v_1(t)$ from Fig.2.22, it can be attained that,

$$\overline{V}_1(t) = \left(d \cdot \left(\overline{V}_S(t) - 2\overline{V}_{C_z}(t)\right)\right) + \left(d_2 \cdot 0\right) + \left(\left(1 - d - d_2\right) \cdot \left(\overline{V}_S(t) - \overline{V}_{C_z}(t)\right)\right) \tag{2.106}$$

In (2.106), $\overline{V}_S(t)$ and $\overline{V}_{C_z}(t)$ are the average values of source voltage and Z-source capacitor voltage within the period, T_S, under consideration, respectively.

Substituting d_2 from (2.97) and the Z-source capacitor average voltage, $\overline{V}_{C_z}(t)$, from (2.75) into (2.106) gives;

$$\overline{V}_1(t) = \overline{V}_S(t) - \overline{V}_O(t) \tag{2.107}$$

where $\overline{V}_O(t)$ is the average value of output voltage within the period, T_S, under consideration. The averaged voltage, $\overline{V}_2(t)$, on switch Q_1 can be obtained from Fig.2.22, such as;

$$\overline{V}_2(t) = (d \cdot 0) + \left(d_2 \cdot \left(2\overline{V}_{C_z}(t) - \overline{V}_S(t)\right)\right) + \left((1 - d - d_2) \cdot \left(\overline{V}_O(t)\right)\right) \tag{2.108}$$

which gives;

$$\overline{V}_2(t) = \overline{V}_O(t) \tag{2.109}$$

After simplifications the average value the current in D_1 , $\bar{I}_1(t)$, is;

$$\bar{I}_1(t) = d_2 \cdot \left(2 \cdot \bar{I}_{L_z}(t) - \bar{I}_{L_O}(t)\right) \tag{2.110}$$

Also, the average current of the switch Q_1 is, then;

$$\bar{I}_2(t) = d \cdot \left(2 \cdot \bar{I}_{L_z}(t) - \bar{I}_{L_O}(t)\right) \tag{2.111}$$

To obtain the small signal model of the converter, the $\bar{I}_1(t)$ and $\bar{I}_2(t)$ expressions must be in terms of average voltage on switch Q_1, $\overline{V}_2(t)$, and D_1 voltage, $\overline{V}_1(t)$. Thus, the average currents through the inductor should be derived.

From Fig.2.22 the Z-source inductor average current, $\bar{I}_{L_z}(t)$, can be written as,

$$\bar{I}_{L_z}(t) = d \cdot \frac{I_{L_z(3)} + I_{L_z(1)}}{2} + d_2 \cdot \frac{I_{L_z(1)} + I_{L_z(2)}}{2} + (1 - d - d_2) \cdot \frac{I_{L_z(2)} + I_{L_z(3)}}{2} \tag{2.112}$$

Using (2.93) and (2.112) gives;

$$\bar{I}_{L_z}(t) = (d + d_2) \cdot \frac{I_{L_z(1)} + I_{L_z(2)}}{2} + (1 - d - d_2) \cdot I_{L_z(2)} \tag{2.113}$$

The waveform of output inductor in Fig.2.22 can be used to find the average current. Then the average current of the output inductor current, $\bar{I}_{L_o}(t)$, is,

$$\bar{I}_{L_o}(t) = d \cdot \frac{I_{L_O(3)} + I_{L_O(1)}}{2} + d_2 \cdot \frac{I_{L_O(1)} + I_{L_O(2)}}{2} + (1 - d - d_2) \cdot \frac{I_{L_O(2)} + I_{L_O(3)}}{2} \tag{2.114}$$

Substituting the value of $I_{L_O(3)}$ from (2.92) into (2.114), using the (2.79) and (2.80) for the values of $I_{L_O(2)}$ and $I_{L_O(3)}$ and also simplifying the result give the output inductor average current, $\bar{I}_{L_o}(t)$, such as;

$$\bar{I}_{L_o}(t) = (d + d_2) \cdot \frac{2 \cdot I_{L_z(2)} + I_{L_O(1)}}{2} + (1 - d - d_2) \cdot I_{L_z(2)} \tag{2.115}$$

Using the average current expressions developed for the Z-source inductor and the output inductor, given in (2.113) and (2.115) respectively. (2.110) gives the expression for the average current in D_1 as;

$$\bar{I}_1(t) = d_2 \cdot (d + d_2) \cdot \left(I_{L_z(1)} - \frac{I_{L_O(1)}}{2} \right) \tag{2.116}$$

Also, substituting (2.113) and (2.115) into (2.111) gives the average current for the switch as;

$$\bar{I}_2(t) = d \cdot (d + d_2) \cdot \left(I_{L_z(1)} - \frac{I_{L_O(1)}}{2} \right) \tag{2.117}$$

By combining (2.84) and (2.82), the expression $\left(I_{L_Z(1)} - \frac{I_{L_O(1)}}{2} \right)$ can be found as;

$$\left(I_{L_Z(1)} - \frac{I_{L_O(1)}}{2} \right) = \frac{V_O}{2} \cdot d \cdot T_S \cdot \left(\frac{2}{L_Z} + \frac{1}{L_O} \right) \tag{2.118}$$

Rewriting the (2.116) and (2.117) by using the (2.118) and substituting d_2 value from (2.97) leads to;

$$\bar{I}_1(t) = \frac{V_O \cdot d}{V_O - V_S} \cdot \left(d + \frac{V_O \cdot d}{V_O - V_S} \right) \cdot V_O \cdot d \cdot \frac{T_S}{2} \left(\frac{2}{L_Z} + \frac{1}{L_O} \right) \tag{2.119}$$

and

$$\bar{I}_2(t) = d^2 \cdot \left(d + \frac{V_O \cdot d}{V_O - V_S} \right) \cdot V_O \cdot \frac{T_S}{2} \cdot \left(\frac{2}{L_Z} + \frac{1}{L_O} \right) \tag{2.120}$$

To find the average values of inductor currents in terms of the average voltage, $\overline{V}_2(t)$, on Q_1 and the average voltage, $\overline{V}_1(t)$, of D_1 (2.107) and (2.109) can be used. Putting V_O and $V_O - V_S$ values from (2.107) and (2.109) into (2.119) and (2.120) leads to;

$$\bar{I}_1(t) = \frac{\overline{V}_2(t) \cdot d^3 \cdot \left(\overline{V}_2(t) - \overline{V}_1(t) \right)}{\overline{V}_1(t)^2} \cdot \frac{Ts}{2} \cdot \left(\frac{2}{L_Z} + \frac{1}{L_O} \right) \tag{2.121}$$

and,

$$\bar{I}_2(t) = \frac{\overline{V}_2(t) \cdot d^3 \cdot \left(\overline{V}_1(t) - \overline{V}_2(t) \right)}{\overline{V}_1(t)} \cdot \frac{Ts}{2} \cdot \left(\frac{2}{L_Z} + \frac{1}{L_O} \right) \tag{2.122}$$

The diode average current, $\bar{I}_1(t)$, has two fundamental components; the dc value, I_1, and the small signal ac value , $\hat{i}_1(t)$.

$$\bar{I}_1(t) = I_1 + \hat{i}_1(t) \tag{2.123}$$

The average current of diode, $\bar{I}_1(t)$, in (2.121), is expressed as a function of duty-factor, $d(t)$, average diode voltage, $\overline{V}_1(t)$, and average switch voltage, $\overline{V}_2(t)$.

$$\bar{I}_1(t) = I_1 + \hat{i}_1(t) = f_1\left(\overline{V}_2(t), \overline{V}_1(t), d(t)\right) \tag{2.124}$$

By perturbation and linearization of (2.121), small ac variation of average diode current, $\hat{i}_1(t)$, can be expressed as a linear function of small ac variations of duty-factor, $\hat{d}(t)$, diode voltage, $\hat{v}_1(t)$, and switch voltage, $\hat{v}_2(t)$. Thus, small signal equation for the current through the diode can be written as;

$$\hat{i}_1(t) = \frac{\hat{v}_1(t)}{r_1} + j_1 \cdot \hat{d}(t) + g_1 \cdot \hat{v}_2(t) \tag{2.125}$$

r_1, j_1 and g_1 terms in (2.125) can be found by applying three dimensional Taylor expansion to the function $f_1\left(\overline{V}_2(t), \overline{V}_1(t), d(t)\right)$.

$$\bar{I}_1(t) = I_1 + \hat{i}_1(t) = f_1(V_1, V_2, D) + \frac{\hat{v}_1(t)}{r_1} + j_1 \cdot \hat{d}(t) + g_1 \cdot \hat{v}_2(t) \tag{2.126}$$

where,

$$\begin{aligned}
I_1 &= f_1(V_1, V_2, D) = \frac{V_2 \cdot D^3 \cdot (V_2 - V_1)}{V_1^2} \cdot \frac{T_S}{2} \cdot \left(\frac{2}{L_Z} + \frac{1}{L_O}\right) \\
\frac{1}{r_1} &= \left.\frac{\partial f_1(\hat{v}_1, V_2, D)}{\partial \hat{v}_1}\right|_{\hat{v}_1 = V_1} = \frac{V_2^2 \cdot D^3 \cdot (V_1^2 - 2 \cdot V_1 \cdot V_2)}{V_1^4} \cdot \frac{T_S}{2} \cdot \left(\frac{2}{L_Z} + \frac{1}{L_O}\right) \\
g_1 &= \left.\frac{\partial f_1(V_1, \hat{v}_2, D)}{\partial \hat{v}_1}\right|_{\hat{v}_2 = V_2} = \frac{D^3 \cdot (3 \cdot V_2^2 - 2 \cdot V_1 \cdot V_2)}{V_1^2} \cdot \frac{T_S}{2} \cdot \left(\frac{2}{L_Z} + \frac{1}{L_O}\right) \\
j_1 &= \left.\frac{\partial f_1\left(V_1, V_2, \hat{d}(t)\right)}{\partial \hat{v}_1}\right|_{\hat{d}(t) = D} = \frac{3 \cdot D^2 \cdot V_2^2 \cdot (V_2 - V_1)}{V_1^2} \cdot \frac{T_S}{2} \cdot \left(\frac{2}{L_Z} + \frac{1}{L_O}\right)
\end{aligned} \tag{2.127}$$

High order terms, which are negligible, are not written in (2.127).

Same as diode average current, $\bar{I}_1(t)$, the average switch current, $\bar{I}_2(t)$, has a quiescent term, I_2, and a small ac term, $\hat{i}_2$ and also from (2.122) $\bar{I}_2(t)$ can be expressed as function of duty-factor, $d(t)$, average diode voltage, $\overline{V_1}(t)$, and average switch voltage, $\overline{V_2}(t)$.

$$\bar{I}_2(t) = I_2 + \hat{i}_2(t) = f_2\left(\overline{V_2}(t), \overline{V_1}(t), d(t)\right) \tag{2.128}$$

By perturbation and linearization of (2.122), small ac variation of average switch current, $\hat{i}_2(t)$, can be expressed as a linear function of small ac variations of duty-factor, $\hat{d}(t)$, diode voltage, $\hat{v}_1(t)$, and switch voltage, $\hat{v}_2(t)$. Small signal equations of switch can be written as,

$$\hat{i}_2(t) = \frac{\hat{v}_2(t)}{r_2} + j_2 \cdot \hat{d}(t) + g_2 \cdot \hat{v}_1(t) \tag{2.129}$$

r_2, j_2 and g_2 terms can be obtained by applying Taylor expansion to average switch current expression, $\bar{I}_2(t)$, in (2.122).

$$\bar{I}_2(t) = I_2 + \hat{i}_2(t) = f_2(V_1, V_2, D) + \frac{\hat{v}_2(t)}{r_2} + j_2 \cdot \hat{d}(t) + g_2 \cdot \hat{v}_2(t) \tag{2.130}$$

where,

$$\frac{1}{r_2} = \left.\frac{\partial f_2(V_1, \hat{v}_2, D)}{\partial \hat{v}_2}\right|_{\hat{v}_2 = V_2} = \frac{D^3 \cdot (V_1 - 2 \cdot V_2)}{V_1} \cdot \frac{T_S}{2} \cdot \left(\frac{2}{L_Z} + \frac{1}{L_O}\right)$$

$$g_2 = \left.\frac{\partial f_2(\hat{v}_1, V_2, D)}{\partial \hat{v}_1}\right|_{\hat{v}_1 = V_1} = \frac{D^3 \cdot V_2^{\,2}}{V_1^{\,2}} \cdot \frac{T_S}{2}\left(\frac{2}{L_Z} + \frac{1}{L_O}\right)$$

$$j_2 = \left.\frac{\partial f_2\left(V_1, V_2, \hat{d}(t)\right)}{\partial \hat{d}(t)}\right|_{\hat{d}(t) = D} = \frac{3 \cdot D^2 \cdot V_2 \cdot (V_1 - V_2)}{V_1} \cdot \frac{T_S}{2} \cdot \left(\frac{2}{L_Z} + \frac{1}{L_O}\right)$$

In discontinuous current mode, diode D_1, has ac small signal terminal voltage, $\hat{v}_1(t)$, and ac small signal terminal current, $\hat{i}_1(t)$. Terminal current is found in (2.125) in terms of small ac variations of duty-factor, $\hat{d}(t)$, diode voltage, $\hat{v}_1(t)$, and switch voltage, $\hat{v}_2(t)$. Thus the diode can be modeled as in Fig.2.23.

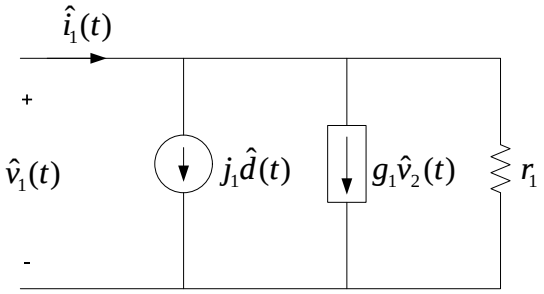

Fig.2.23 Equivalent small signal model of the diode, D_1, in DCM operation

As in the diode D_1 terminal modeling, switch Q_1 can be modeled in the same way from (2.129) and the resulted model for the switch terminal is shown in Fig.2.24.

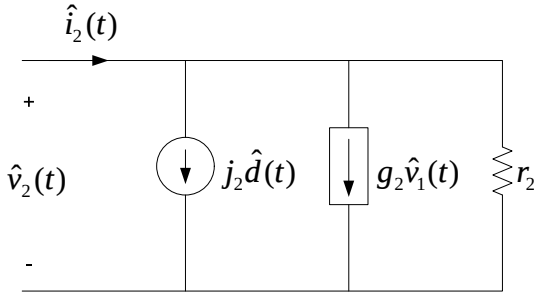

Fig.2.24 Equivalent small signal model of the switch, Q_1, in DCM operation

In Fig.2.23 and Fig.2.24, the models of nonlinear elements of Z-source dc/dc converter (diode D_1 and switch Q_1) are shown. If these models are substituted in small signal Z-source dc/dc converter, the small signal model of Z-source dc/dc converter for DCM operation is obtained. Fig.2.25 represents the small signal model of Z-source dc/dc converter in DCM operation.

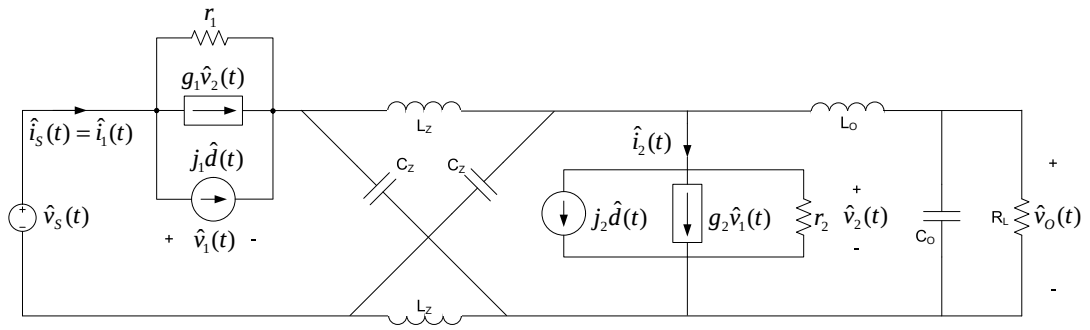

Fig.2.25 Small signal model of the Z-source dc/dc converter in DCM operation

2.3.6 Determination of Transfer Functions of Z-source DC/DC Converter in DCM Operation

In Fig.2.25, input voltage, $\hat{v}_S(t)$, is set to zero to find the duty factor-to-output voltage transfer function for DCM operation, $G_{vd-dcm}(s)$. The poles and right hand zeros caused by inductors are at higher frequencies. The poles caused by capacitors are at low frequencies. Thus, in practice, eliminating the inductors by short-circuiting them in small signal model is a good approximation in determination of transfer functions.

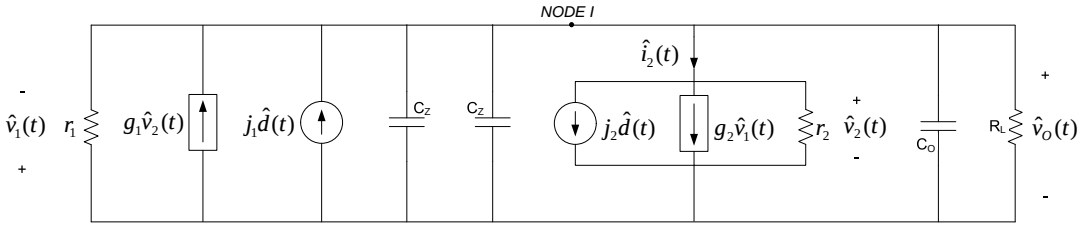

Fig.2.26 Reduced small signal model of the Z-source dc/dc converter to determine the duty factor-to-output voltage transfer function, $G_{vd-dcm}(s)$, in DCM operation

New reduced small signal model can be obtained by setting input voltage to zero, $\hat{v}_S = 0$, and elimination of inductors from Fig.2.25. Fig.2.26 shows the reduced small signal model of Z-source dc/dc converter in DCM operation to determine $G_{vd-dcm}(s)$.

From Fig.2.26, it can be acquired that,

$$\hat{v}_O = -\hat{v}_1 = \hat{v}_2 \tag{2.131}$$

Applying Kirchhoff's current law to NODE I in Fig.2.26 leads to,

$$\hat{v}_O = \left(j_1 \cdot \hat{d} + g_1 \cdot \hat{v}_2 - j_2 \cdot \hat{d} - g_2 \cdot \hat{v}_1\right) \times \left(r_1 // r_2 // R_L // \frac{1}{s(2C + C1)} \right) \tag{2.132}$$

Using (2.131) and (2.132) together and arranging them gives the transfer function of duty factor-to-output voltage, $G_{vd-dcm}(s)$, such as,

$$G_{vd-dcm}(s) = \left.\frac{\hat{v}_O}{\hat{d}}\right|_{\hat{v}_S=0} = \frac{R_T \cdot (j_1 - j_2)}{s(C_T \cdot R_T) + [1 - R_T \cdot (g_1 + g_2)]} \tag{2.133}$$

where,

$$R_T = r_1 // r_2 // R_L = \frac{1}{\frac{1}{r_1}+\frac{1}{r_2}+\frac{1}{R_L}}$$

$$C_T = 2 \cdot C + C1$$

Again small signal model in Fig.2.25 can be used to determine the input voltage-to-output voltage transfer function in DCM operation, $G_{vg-dcm}(s)$. To find $G_{vg-dcm}(s)$, ac small signal value of duty-factor, $\hat{d}$, is set to zero in Fig.2.25. Thus, the independent current sources in Fig.2.25 become open circuit. By the same reason as in determining $G_{vd-dcm}(s)$, inductors are eliminated from Fig.2.25. Replacement of current sources by open-circuits and elimination of inductors reduce the small signal model as shown in Fig.2.27.

By using Kirchhoff's voltage law, it can be determined from Fig.2.27 that,

$$\hat{v}_S = \hat{v}_1 + \hat{v}_O \tag{2.134}$$

and

$$\hat{v}_2 = \hat{v}_O \tag{2.135}$$

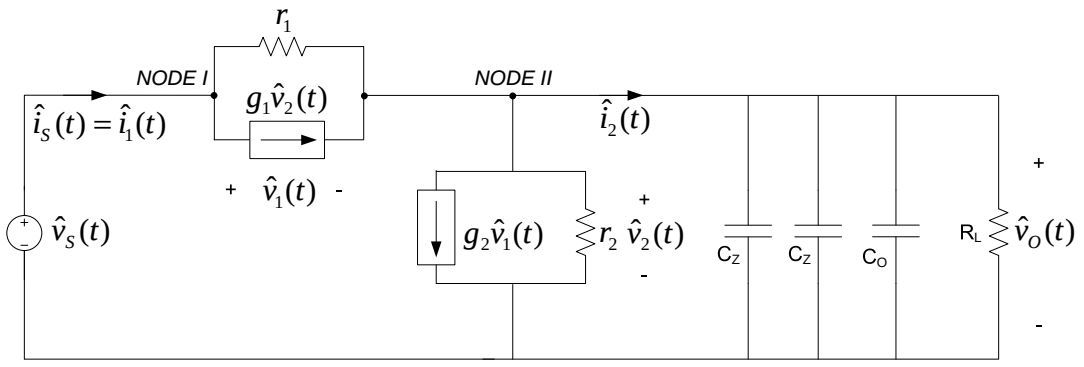

Fig.2.27 Reduced small signal model of the Z-source dc/dc converter to determine the input voltage-to-output voltage transfer function, $G_{vg-dcm}(s)$, in DCM operation

Also, again from Fig.2.27, it can be found as;

$$\hat{v}_O = \hat{i}_2 \cdot \left(R_L + \frac{1}{s(2 \cdot C_Z + C_O)} \right) \tag{2.136}$$

Applying Kirchhoff's current law at NODE I and NODE II in Fig.2.27, results in;

$$\hat{i}_1 = \frac{\hat{v}_1}{r_1} + g_1 \cdot \hat{v}_2 \tag{2.137}$$

and

$$\hat{i}_2 = \hat{i}_1 - \frac{\hat{v}_2}{r_2} - g_2 \cdot \hat{v}_1 \tag{2.138}$$

Substituting (2.137) and (2.138) into (2.136) and using (2.135) gives,

$$\hat{v}_O = \left(\frac{\hat{v}_1}{r_1} + g_1 \cdot \hat{v}_O - \frac{\hat{v}_O}{r_2} - g_2 \cdot \hat{v}_1 \right) \times \left(R_L + \frac{1}{s(2 \cdot C_Z + C_O)} \right) \tag{2.139}$$

Combining (2.134) and (2.139) and rearranging them to get an expression for $\frac{\hat{v}_O}{\hat{v}_S}$ gives the input voltage-to-output voltage transfer function, $G_{vg-dcm}(s)$, for DCM operation as;

$$G_{vg-dcm}(s) = \left. \frac{\hat{v}_{OUT}}{\hat{v}_S} \right|_{\hat{d}=0} = \frac{R_L \cdot \left(\frac{1}{r_2} - g_1 \right)}{s\left[(2 \cdot C_Z + C_O) \cdot R_L \right] + \left(1 + R_L \cdot \left[\frac{1}{r_1} + \frac{1}{r_2} - g_1 - g_2 \right] \right)} \tag{2.140}$$

As it can be noticed from (2.133) and (2.140) both $G_{vd-dcm}(s)$ and $G_{vg-dcm}(s)$ are first order systems. The constants j_1, j_2, g_1, g_2, r_1 and r_2 are dependent parameters on input voltage, V_S, output voltage, V_O, and inductors as stated in (2.127) and

(2.130). These constants also depend on the switching frequency, which makes transfer functions of DCM operation frequency dependent as well. On the contrary, duty factor-to-output voltage transfer function, $G_{vd}(s)$ in CCM operation is frequency independent. Furthermore, $G_{vd-dcm}(s)$ and G_{vg-dcm} are related to capacitor sizes and load resistance as stated at (2.133) and (2.140).

2.4 Transition between CCM and DCM Operations

Generally, switching converters are designed to operate in CCM at full load condition. However, decline of load power forces the converter to operate in DCM operation. The percentage of load power that leads to transition from CCM to DCM can be adjusted at design process. Thus, knowledge of boundary between CCM and DCM operations is a significant aspect in designing a switching converter.

Sizes of selected inductors, switching frequency, duty-factor and load resistance are all affect the transition. In Z-source dc/dc converter, transition condition can be determined by using the equations for DCM operation. From Fig.2.22, for DCM operation the duration of $t_1 + t_2$ must be smaller than switching period, which means,

$$t_1 + t_2 \leq T_S \tag{2.141}$$

(2.141) also leads to;

$$d_1 + d_2 \leq 1 \tag{2.142}$$

If the expression for d_2 in (2.97) is used, then (2.142) can be put into the form as;

$$d_1 + d_1 \frac{V_O}{V_O - V_S} \leq 1 \tag{2.143}$$

Reorganizing (2.143) gives result as,

$$\frac{(1-d_1)}{(1-2d_1)} \leq \frac{V_O}{V_S} \tag{2.144}$$

The input-to-output ratio, $\frac{V_O}{V_S}$, can be replaced by its equivalent seen in (2.104).

$$\frac{(1-d_1)}{(1-2d_1)} \leq 1+\frac{R_L \cdot d_1^{\,2} \cdot T_S}{2} \cdot \left(\frac{1}{L_O} + \frac{2}{L_Z} \right) \tag{2.145}$$

If the simplifications are made in (2.145), the result is;

$$\frac{2}{R_L \cdot d_1 \cdot T_S \cdot (1-2d_1)} \leq \left(\frac{1}{L_O} + \frac{2}{L_Z} \right) \tag{2.146}$$

Note that, if the left hand side of the inequality is strictly less than the right hand side, than the converter operates in DCM, thus the condition for transition from DCM to CCM will take place when both sides in (2.146) are equal to each other.

As it can be determined from (2.146), the condition for transition from DCM to CCM depends on both Z-source inductor, L_Z, and output inductor, L_O. Also, it must be mentioned that, in DCM operation, it is assumed that the output inductor current never becomes zero at any time of switching period. If this transition from DCM to CCM happens due to existences of very light load or due to the presence of low output inductance value, the mode of Z-source dc/dc converter goes other DCM operations. These DCM operations have not been accounted in this study.

2.5 Control Circuit Transfer Function

The strategy of the control for this switching converter is basically related to the objective of obtaining non-oscillating (or non-fluctuating) and stable voltage at the output. The control strategy is also related to keep the settling time and overshoots of the voltage at the output within reasonably low limits if either input voltage level or the load current level varies rapidly. Fig.2.28 shows the main block diagram for a converter plus a suitable control circuit fulfilling such a strategy.

In the control of the converter, the output voltage is measured and compared with a reference, V_{REF}. Thus, K_{FB} block represents the feedback gain of the output voltage. The voltage error is fed to an error amplifier, $K_{EA}(s)$, to produce the control signal, $\hat{v}_{CTRL}(s)$. A PWM block, $K_{PWM}(s)$, generates the required duty-factor, $\hat{d}(s)$, when driven by the control signal. As the duty-factor directly acting on the dc/dc converter represented by the input of duty factor-to-output voltage transfer function, $G_{vd}(s)$ produces the output voltage, $\hat{v}_O(s)$.

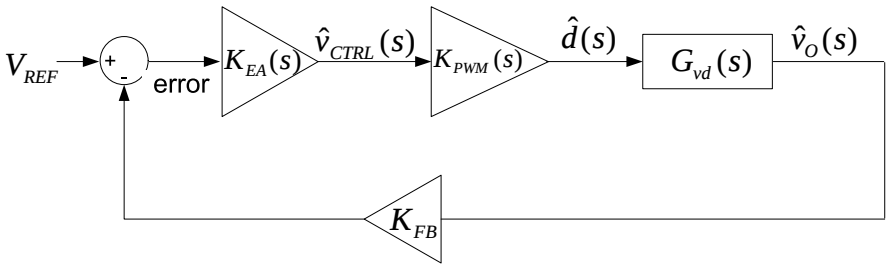

Fig.2.28 Block diagram of the controlled Z-source dc/dc converter

To determine the stability of the control loop, the open loop transfer function, $G_{OPEN}(s)$ should be found. The total gain around the feedback loop gives the open-loop transfer function, $G_{OPEN}(s)$. Thus, $G_{OPEN}(s)$ can be determined as;

$$G_{OPEN}(s) = K_{FB} \cdot K_{EA}(s) \cdot K_{PWM}(s) \cdot G_{vd}(s) \tag{2.147}$$

The implemented circuit to control the Z-source dc/dc converter is shown in Fig.2.29.

In the circuit, R_1 and R_2 are used to divide output voltage to monitor it. Thus, the feedback gain of the output voltage, $K_{FB,}$ is,

$$K_{FB} = \frac{R_1}{R_1 + R_2} \tag{2.148}$$

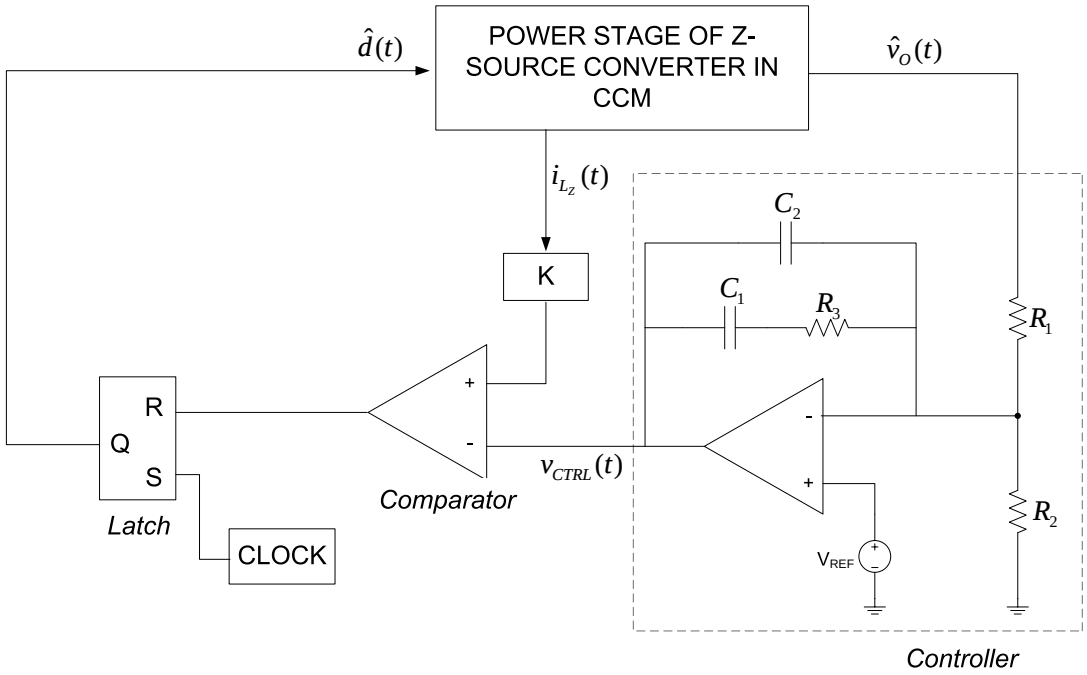

Fig.2.29 Control circuit of the Z-source dc/dc converter

V_{REF} generates the reference voltage that divided output voltage follows this voltage. The resistors R_1, R_3 and capacitors C_1, C_2 determine the transfer function of error amplifier, $K_{EA}(s)$. So,

$$K_{EA}(s) = \frac{1}{R_1 \cdot C_2} \cdot \frac{\left(s + \frac{1}{C_1 \cdot R_3}\right)}{s \cdot \left(s + \frac{C_1 + C_2}{C_1 \cdot C_2 \cdot R_3}\right)} \tag{2.149}$$

The output of error amplifier the control voltage, $\hat{v}_{CTRL}(t)$, is fed to PWM block which compares $\hat{v}_{CTRL}(t)$ with triangular waveform to produce a rectangular wave. Note that the peak-to-peak magnitude of the triangular waveform, $V_{PWM(PP)}$, plays a role in open-loop transfer function. The transfer function of PWM block, $K_{PWM}(s)$, is determined as;

$$K_{PWM}(s) = \frac{1}{V_{PWM(PP)}} \tag{2.150}$$

The resulting open-loop transfer function can be acquired by combining (2.147), (2.148), (2.149) and (2.150). The open-loop transfer function of controlled converter, $G_{OPEN}(s)$, is obtained at the end as;

$$G_{OPEN}(s) = \frac{1}{V_{PWM(PP)}} \cdot \frac{R_1}{R_1 + R_2} \cdot \frac{1}{R_1 \cdot C_2} \cdot \frac{\left(s + \frac{1}{C_1 \cdot R_3} \right)}{s \cdot \left(s + \frac{C_1 + C_2}{C_1 \cdot C_2 \cdot R_3} \right)} \cdot G_{vd}(s) \tag{2.151}$$

2.6 Conclusion of Chapter

In the first part of the chapter, a brief introduction is given and basic operation principles of the Z-source dc/dc converter are explained. In the second part, the mathematical derivations, input-output relationship, the transfer functions and small signal models are founded for continuous current mode operation of the converter. The same items are determined for discontinuous current mode operation in the third part. Furthermore, the transition between CCM and DCM operations are determined in the next part. Finally, the controller transfer function and overall system open loop transfer functions are derived. The next chapter involves the simulation results of both CCM and DCM operations of the converter.

CHAPTER 3

SIMULATION RESULTS OF Z-SOURCE DC/DC CONVERTER

3.1 Introduction

In this chapter, the simulation results obtained in the tests carried out on Z-source full bridge dc/dc converter are presented. First of all, a Z-source dc/dc converter is designed according to the required parameters, given in Table3.1. The objective of conducting the simulations on the converter is to verify the validity of input/output equations and transfer functions developed in previous chapters; and prove that several waveforms regarding to storage elements used in the converter used in idealized forms are close to the real forms. Simulations show also that the simplified circuit used in the analyses is a good approximation. Furthermore, simulations give a means to compare responses obtained both for the actual circuit and the transfer functions against small disturbances occurring in the system. Thus, the transfer functions; transfer function for the input voltage-to-output voltage, $G_{vg}(s)$, transfer function for the duty factor-to-output voltage, $G_{vd}(s)$, transfer function for the duty factor-to-Z-source inductor current, $G_{id}(s)$, and transfer function for the input voltage-to-Z-source inductor current, $G_{ig}(s)$, developed for operations in the continuous current mode are all tested for their exactness and accuracy. The same is followed for the operation in discontinuous current mode to verify the transfer function for the duty factor-to-output voltage, $G_{vd-dcm}(s)$ and transfer function for the input voltage-to-output voltage, $G_{vg-dcm}(s)$. All the circuit simulations are conducted by using SIMPLORER software package from ANSOFT Corporation. In order to accomplish the above defined simulations in CCM and DCM operations controller has been designed for the voltage control loop. Gain and phase margins of overall system have been determined computationally using MATLAB tools.

3.2 Z-source Simulations in CCM Operation

3.2.1 Verification of Component Waveforms in CCM Operation

The main requirements of the Z-source dc/dc converter are listed at Table3.1. According to these requirements Z-source inductors, L_Z, and output inductor, L_O, values are determined and designed Z-source dc/dc converter is simulated.

Table3.1 Main design parameters of the Z-source dc/dc converter in CCM operation

Minimum input voltage	V_S	30	V
Output voltage	V_O	60	V
Output power	P_O	360	W
Peak-to-peak ripple current in Z-source inductor at nominal input voltage (in % of I_{L_z})	Δi_{L_z}	83.3	%
Peak-to-peak ripple current in output inductor at nominal input voltage (in % of I_{L_O})	Δi_{L_O}	66.6	%

Assuming purely resistive loading for the converter, then the load resistor can be found as,

$$R_L = \frac{{V_S}^2}{P_O} = \frac{60^2}{360} = 10\Omega \tag{3.1}$$

The significant part of the design is choosing the inductor and capacitor values and operating frequency. Recalling from Chapter 2 increasing the operating frequency

decreases the inductor sizes and also the physical dimensions of the circuit. However, increasing the frequency means more switching losses, eventually the efficiency of the converter decreases dramatically. On the contrary, use of the low frequency leads to increases both on the size and also the cost of inductors and capacitors. Thus, there is a trade off between the size and efficiency in determining the operating frequency of the converter. For CCM operation, the frequency is selected as $100kHz$. Hence, the period of the circuit is,

$$T_S = \frac{1}{f} = 10^{-5}\,\text{sec} \tag{3.2}$$

The size of the inductors and the average currents through them can not be determined unless the duty-factor is determined. Also, duty-factor is very important in obtaining the transfer functions of the Z-source dc/dc converter. Inserting the input voltage and output voltage values into (2.13) gives the numerical value of duty-factor for the specific case in the simulation as;

$$D = \frac{V_O - V_S}{2V_O - V_S} = \frac{60 - 30}{2 \cdot 60 - 30} = 0.333 \tag{3.3}$$

Noting that, the prospective average current magnitude through an inductor of particular size is an important issue for the inductor design process. Another important parameter in this process is the peak-to-peak current magnitude at normal operation, because this value determines the saturation current level. Hence, the average current, their inductance and the peak-to-peak current magnitude must be determined for both Z-source inductors, L_Z , and output inductor, L_O .

The average current of the Z-source inductor, I_{L_Z} , can be found from (2.43) as,

$$I_{L_Z} = \frac{(D-1)^2 \cdot V_S}{R_L \cdot (1-2D)^2} = \frac{(1-0.333)^2 \cdot 30}{10 \cdot (1-0.666)^2} = 12A \tag{3.4}$$

It is decided in Table3.1 that the peak-to-peak ripple current magnitude at the Z-source inductor, Δi_{L_z}, is 83.3% of average current, I_{L_z}. Thus, the value of Δi_{L_z} is about $10A$. The inductance of the Z-source inductor can be determined by (2.5), as;

$$L_Z = \frac{V_{C_z} \cdot D \cdot T_S}{\Delta i_{L_z}} = \frac{V_O \cdot D \cdot T_S}{I_{L_z(2)} - I_{L_z(1)}} = \frac{60 \cdot 0.333 \cdot 10^{-5}}{10} \cong 20\mu H \tag{3.5}$$

The average current through the output inductor, L_O, can be calculated from (2.43) such as;

$$I_{L_O} = \frac{(1-D) \cdot V_S}{R_L \cdot (1-2D)} = \frac{(1-0.333) \cdot 30}{10 \cdot (1-0.666)} = 6A \tag{3.6}$$

From Table3.1 and (3.6), it can be attained that the magnitude of the peak-to-peak current ripple at the output inductor is $4A$. Also, the output inductance can be achieved by (2.17), as;

$$L_O = \frac{V_O \cdot D \cdot T_S}{\Delta i_{L_O}} = \frac{60 \cdot 0.333 \cdot 10^{-5}}{4} = 50\mu H \tag{3.7}$$

The Z-source capacitors, C_Z, are set to $50\mu F$ each and the output capacitor, C_O, is chosen as $400\mu F$. This way, the peak-to-peak voltage ripple on the Z-source capacitors will be about $0.8V$ and the peak-to-peak voltage ripple on the output capacitor will be about $12mV$.

$$\begin{aligned} C_{Z1} &= C_{Z2} = C_Z = 50\mu F \\ C_O &= 400\mu F \end{aligned} \tag{3.8}$$

Table3.2 summarizes the converter parameters adopted for the converter running in CCM operation.

The simulations of the Z-source dc/dc converter with the parameters summarized in Table3.2 for CCM operation use SIMPLORER Software package from ANSOFT Cooperation.

Table3.2 Z-source dc/dc converter parameters for CCM operation

Z-source inductors, L_Z	20	μH
Z-source capacitors, C_Z	50	μF
Output inductor, L_O	50	μH
Output capacitor, C_O	400	μF
Switching Frequency, f_S	100	kHz
Load resistance, R_L	10	Ω
Input voltage, V_S	30	V
Output voltage, V_O	60	V
Output current, I_L	6	A

Fig.3.1 represents the power stage of the converter. The voltage source, V_S, corresponds to input voltage which is set to $30V$. Duty-factor block generates the required duty-factor and its value is set to 0.333, from (3.3), to get $60V$ output voltage across the load resistance, R_L. The Z-source inductors, L_{Z1} and L_{Z2}, are set to $20\mu H$, and the Z-source capacitors C_{Z1} and C_{Z2}, are chosen as $50\mu F$. As calculated in (3.7), the output inductance, L_O, is assigned to $50\mu H$. Also, the output capacitor, C_O, is chosen as $400\mu F$. The forward voltage drops on diodes, D_1 and D_2, are taken as zero, because the forward voltages of the diodes have not been taken into account in development of the converter model. R_L is set to 10Ω to draw $360W$ power from the supply, V_S.

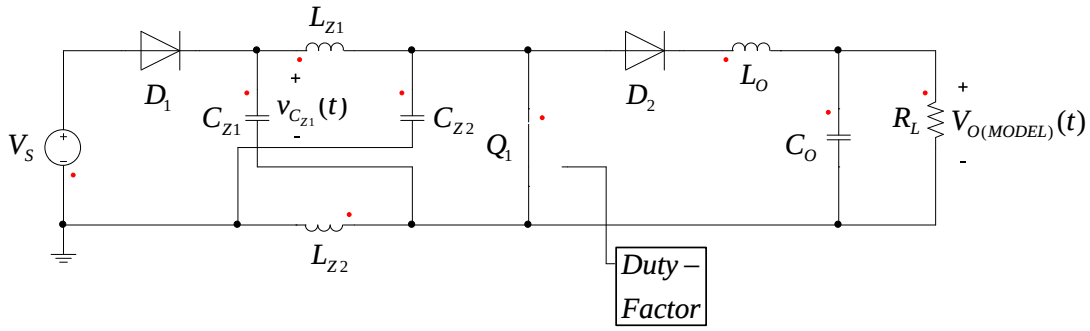

Fig.3.1 Power stage of the Z-source dc/dc converter in CCM operation

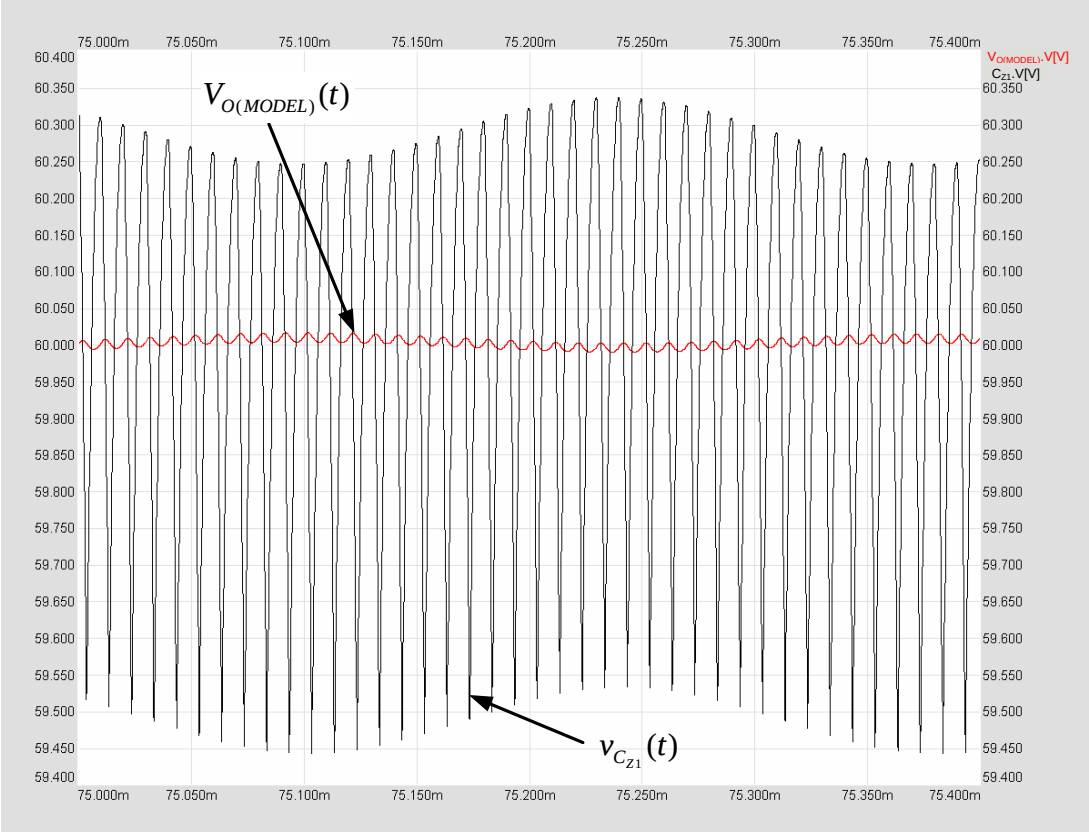

Fig.3.2 Voltage across the load resistor R_L, $V_{O(MODEL)}(t)$, (red), voltage across the Z-source capacitor C_{Z1}, $v_{C_{Z1}}(t)$, (black) in CCM operation

The results obtained in the simulations are shown in figures starting with Fig.3.2. The graphs display responses beginning from $75ms$ on word in order to discard the start up transients. The simulation results seen Fig.3.2 shows that; i. the output voltage, $V_{O(MODEL)}(t)$, on R_L is at $60V$ as desired; ii. and the voltages on Z-source capacitors, $v_{C_{Z1}}(t)$, are equal to the output voltage, $V_{O(MODEL)}(t) = 60V$, as the converter operation requires it.

Fig.3.3 shows the following variables; Z-source inductor current, $i_{L_Z}(t)$, Z-source capacitor current, $i_{C_Z}(t)$, and diode D_1 current, $i_{D_1}(t)$, graphically for CCM operation. Note that, in Fig.3.3 that when duty-factor output (in red) is high i.e. the switch Q_1 is 'ON', Z-source capacitors, C_{Z1} and C_{Z2} feed current (and hence energy) (black for $i_{L_Z}(t)$ and green for $i_{C_Z}(t)$) through the Z-source inductors, L_{Z1} and L_{Z2}, respectively. In this time interval, t_1, D_1 is reverse biased and in blocking state, so no energy will be delivered to the rest of the converter by the source. When the duty-factor output falls to low at zero volts, i.e. the switch is 'OFF' the time interval t_2 is entered. In t_2, Z-source inductors transfer the energy they have stored in t_1 to the load and the output inductor, L_O. D_1 is now forward biased and Z-source capacitors starts charging (green for $i_{C_Z}(t)$) from the input source during t_2. The peak-to-peak magnitude of the current through Z-source inductors is expected to be $10A$ as design criteria. Note that, in Fig.3.3 the inductor current, $i_{L_Z}(t)$, swings between $7A$ and $17A$ in comply with the design criteria. Note also that, the average currents through L_{Z1} and L_{Z2} are $12A$ as they are calculated at (3.4).

For CCM operation, the output inductor current, $i_{L_O}(t)$, the output capacitor current, $i_{C_O}(t)$ and the Z-source inductor current, $i_{L_Z}(t)$, waveforms are displayed in Fig.3.4 together with duty-factor waveform. When the duty-factor output becomes high, at the beginning of time interval t_1 time interval $i_{L_O}(t)$ starts decreasing. This means, output inductor, L_O, transfers the stored energy in its magnetic medium to the output capacitor, C_O, and to the load, R_L.

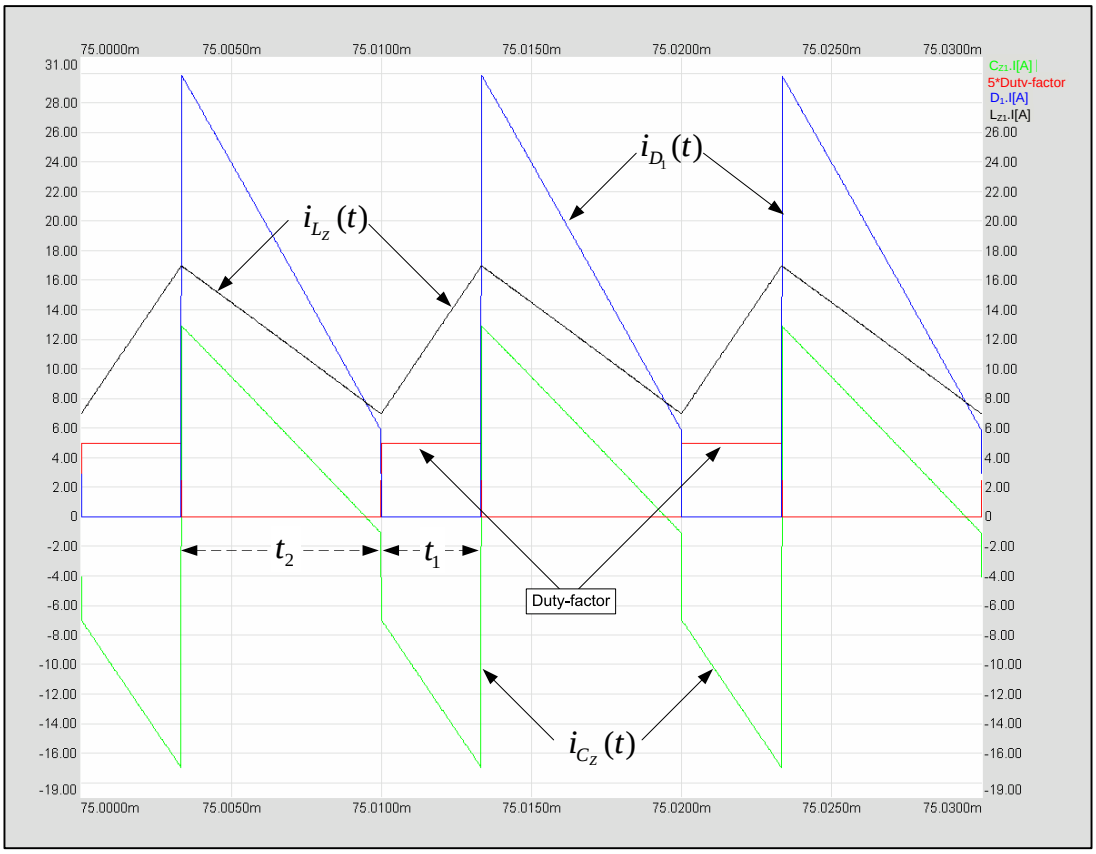

Fig.3.3 Z-source capacitor current, $i_{C_z}(t)$, (green), Duty-factor (red), diode D_1 current, $i_{D_1}(t)$, (blue), and Z-source inductor current, $i_{L_z}(t)$, (black) in CCM operation

*(for the sake of clarity the Duty-factor is multiplied by 5)

When the Duty-factor output becomes low, i.e. the switch becomes 'OFF' in time interval t_2, L_O starts storing energy over inductors L_{Z1} and L_{Z2}. The load is fed by C_O in the first half part of the time interval, t_2. Note that the peak-to-peak current ripple on the L_O current is $4A$ due to the inductor current swing from $4A$ to $8A$. Thus, the average value of L_O current is $6A$ as calculated at (3.6).

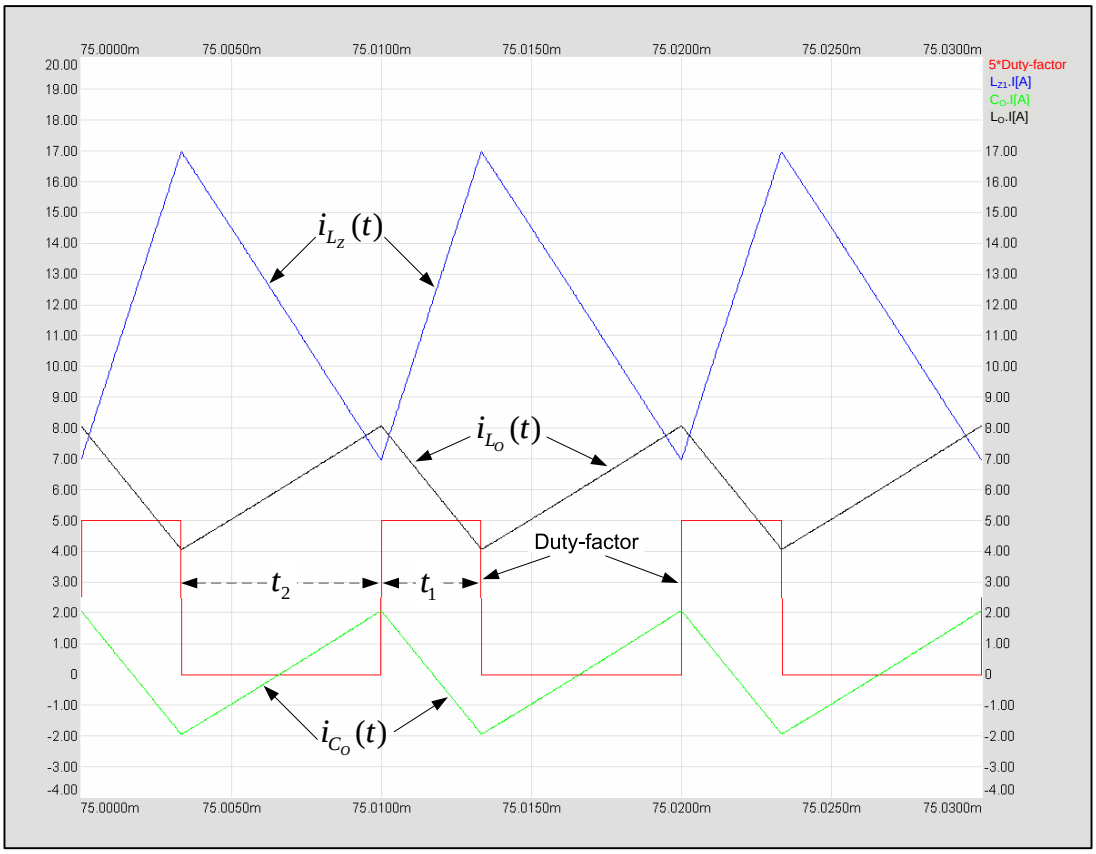

Fig.3.4 Duty-factor (red), Z-source inductor current, $i_{L_z}(t)$, (blue), output capacitor current, $i_{C_o}(t)$, (green), and output inductor current, $i_{L_o}(t)$, (black) in CCM operation

*(for the sake of clarity the Duty-factor waveform is multiplied by 5)

Waveforms seen in Fig.3.3 and Fig.3.4 are same with those theoretically expected shown in Fig.2.6. Also, the peak-to-peak ripple inductor currents are same with those theoretically calculated. Furthermore, in simulation, taking the duty-factor, $D = 0.333$, leads to $60V$ output voltage as calculated in (3.3). Thus, Z-source dc/dc converter simulations for the CCM operation support theoretical results.

3.2.2 Verification of CCM Transfer Functions

In this section, the validity of transfer functions in CCM operation, determined in Chapter 2, are investigated by means of simulations. Transfer functions obtained for the converter model running in CCM operation and the circuit model are run simultaneously and same small step disturbance is applied to both simulated converter system transfer function and circuit model. The response obtained from the transfer function and that obtained from the circuit model, following the application of the step disturbance, d, will be compared in this section. The parameters in Table3.2 are used for the simulation of the circuit model. Also, to find the transfer functions, the expressions, (2.47), (2.48), (2.49) and (2.50) are used.

Transfer functions which will be considered first one; the duty factor-to-output voltage transfer function, $G_{vd}(s)$, and duty factor-to-Z-source inductor current transfer function, $G_{id}(s)$. Fig.3.5 shows scheme used in simulating these transfer functions. The investigation on the circuit model focuses on obtaining the waveforms of output voltage, $V_{O(MODEL)}(t)$, and Z-source inductor current, $I_{L_Z(MODEL)}(t)$, following the application of a small step disturbance, d, is added to the duty-factor, D. Also, the same disturbance, d, is applied to the transfer functions $G_{vd}(s)$ and $G_{id}(s)$ in the simulation. '$Duty-Factor$' block in Fig.3.5 is used to generate the duty-factor output for the circuit model. The duty-factor, applied to the circuit model, is the sum of 'D' and 'd' blocks. 'D' is constant and 0.333. Adding a step disturbance, d, to constant duty-factor, D, is made by that summing operation. 'd' block adds 0.002 as a disturbance to the constant duty-factor upon the circuit reaches at the steady state. The same step disturbance, d, is applied to the transfer functions. '$G_{vd}(s)$' and '$G_{id}(s)$' blocks in Fig.3.5 represents the transfer functions; the duty factor-to-output voltage transfer function and the duty factor-to-Z-source inductor current transfer function, respectively. These transfer function blocks response against the small step disturbance, d, in time domain and the output of these transfer function blocks swing around zero following the application of the step disturbance, d.

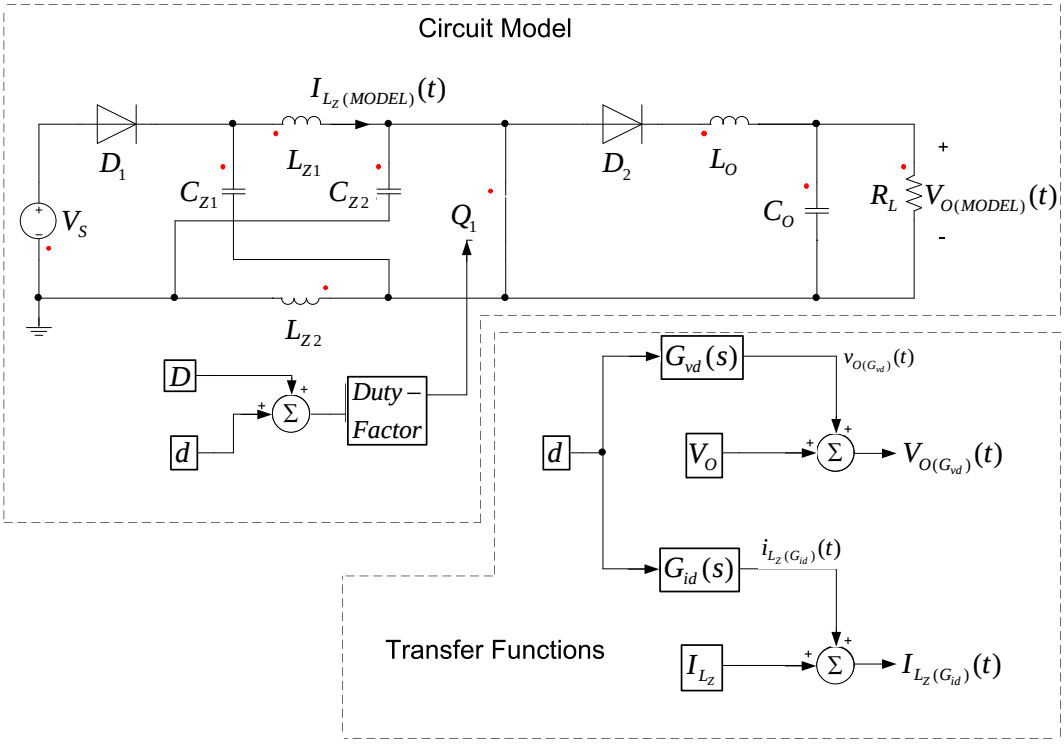

Fig.3.5 The circuit used for the verification of the validity of the transfer functions derived in modeling the converter, $G_{vd}(s)$ and $G_{id}(s)$, in CCM operation

Thereby, the average value of the output voltage, V_O, is added to the output of duty factor-to-output voltage transfer function, $v_{O(G_{vd})}(t)$, under the step disturbance. This way, the response of output voltage obtained from the circuit model, $V_{O(MODEL)}(t)$, and transfer function, $V_{O(G_{vd})}(t)$, can be examined simultaneously in detailed form. For the same purpose, the average current through Z-source inductors, I_{L_Z}, are added to the output of the duty factor-to-Z-source inductor current transfer function, $i_{L_Z(G_{id})}(t)$, under step disturbance. 'V_O' block, in Fig.3.5, sums the average output voltage, V_O, to the response of the transfer function $G_{vd}(s)$ and 'I_{L_Z}' block adds the average current through the Z-source inductors, I_{L_Z}, to the transfer function of $G_{id}(s)$. The responses from $G_{vd}(s)$ and $G_{id}(s)$ can be determined by utilizing the

expressions (2.47) and (2.49), respectively. Substituting the parameters in Table3.2 into the expression for $G_{vd}(s)$ yields;

$$G_{vd}(s)=\frac{-9\cdot10^{-8}s^2-4.8\cdot10^{-4}s+30}{2\cdot10^{-17}s^4+5\cdot10^{-15}s^3+1.033\cdot10^{-8}s^2+2.333\cdot10^{-6}s+0.1111} \tag{3.9}$$

When the same procedure is followed for $G_{id}(s)$ gives;

$$G_{id}(s)=\frac{6.75\cdot10^{-11}s^3+1.369\cdot10^{-7}s^2+0.02141s+10.5}{2\cdot10^{-17}s^4+5\cdot10^{-15}s^3+1.033\cdot10^{-8}s^2+2.333\cdot10^{-6}s+0.1111} \tag{3.10}$$

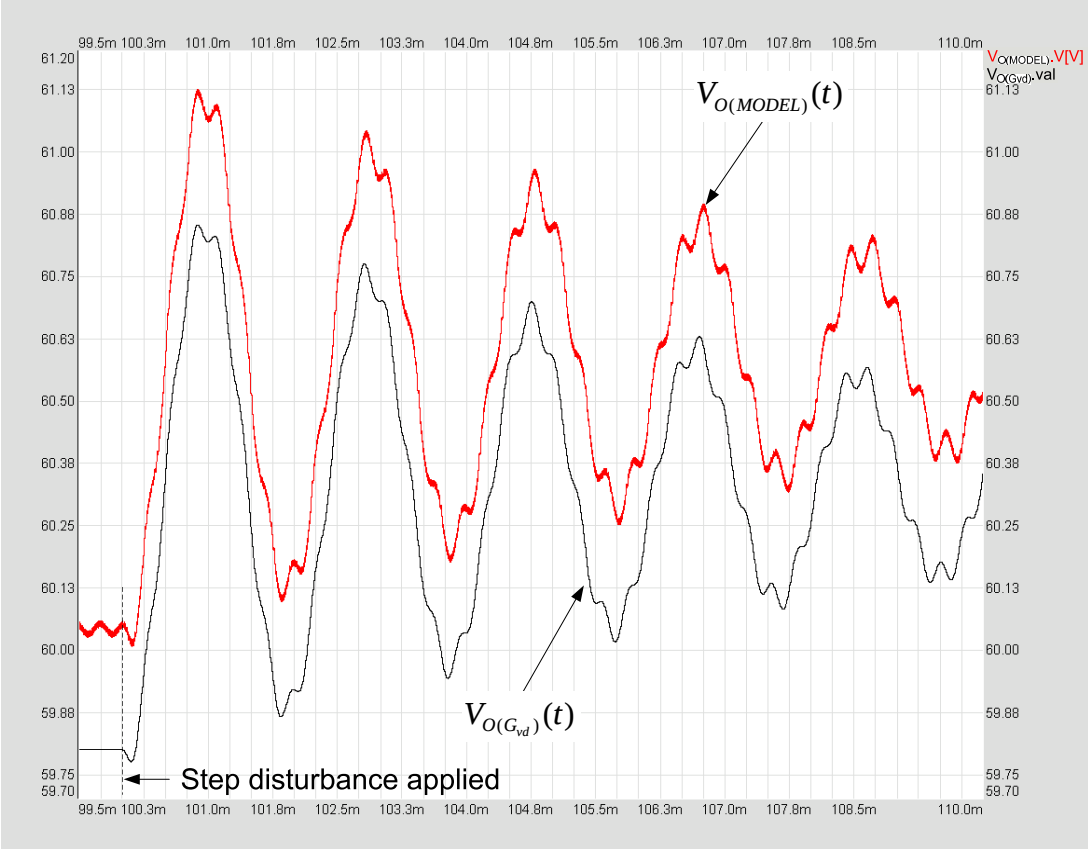

Fig.3.6 Responses against the step disturbance in duty factor, d ; the output voltage, $V_{O(MODEL)}(t)$, in the circuit model (red); the output voltage, $V_{O(G_{vd})}(t)$, computed from the transfer function, $G_{vd}(s)$, (black) in CCM operation

The circuit model output voltage, $V_{O(MODEL)}(t)$, and the response of $G_{vd}(s)$, $V_{O(G_{vd})}(t)$, upon application of step disturbance, d, (at $100ms$ in simulation) are shown in Fig.3.6. $V_{O(MODEL)}(t)$ has both the switching ripple and low frequency components on it, although $V_{O(G_{vd})}(t)$ has only the low frequency components. As expected, the low frequency swings for both $V_{O(MODEL)}(t)$ and $V_{O(G_{vd})}(t)$ are matched to each other exactly.

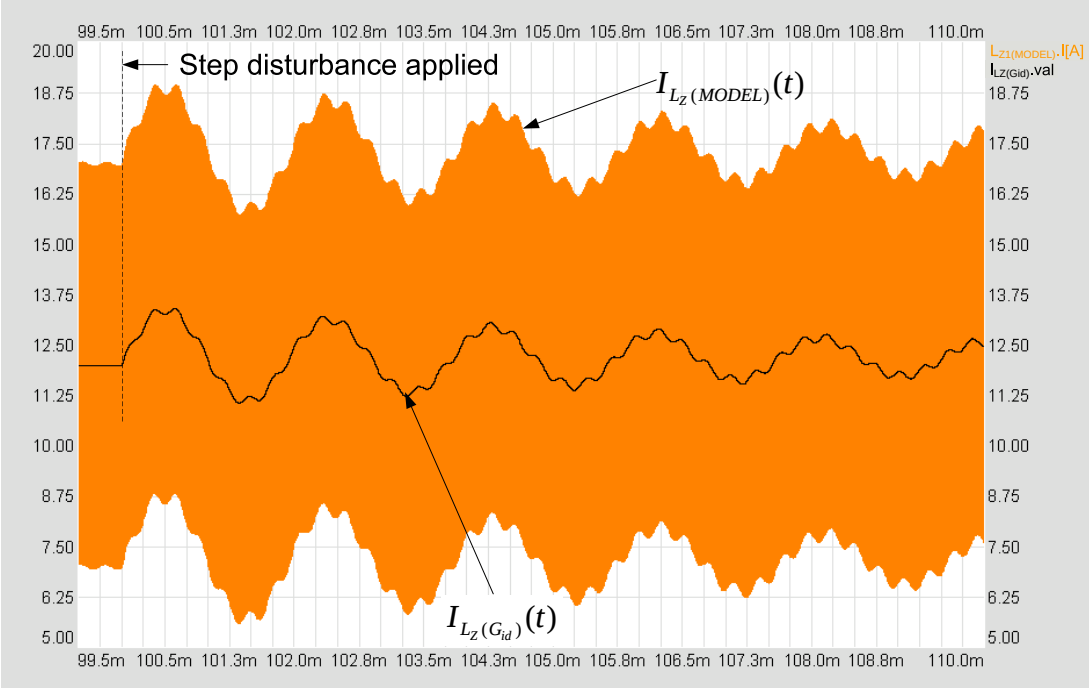

Fig.3.7 Responses against the step disturbance in duty factor, d; the envelop for the Z-source inductor current, $I_{L_Z(MODEL)}(t)$, in the circuit model (orange); the Z-source inductor current, $I_{L_Z(G_{id})}(t)$, computed from the transfer function, $G_{id}(s)$, (black) in CCM operation

The current through the Z-source inductors in circuit model, $I_{L_Z(MODEL)}(t)$ and the response of the transfer function $G_{id}(s)$, $I_{L_Z(G_{id})}(t)$, upon application of step disturbance, d, (at $100ms$ in the simulation running) are shown in Fig.3.7. As in the waveform of $V_{O(MODEL)}(t)$, $I_{L_Z(MODEL)}(t)$ has both switching ripples and low frequency components. The response of the transfer function $G_{id}(s)$ against the step disturbance, $I_{L_Z(G_{id})}(t)$, follows the low frequency component of $I_{L_Z(MODEL)}(t)$ by discarding these switching current ripples through the Z-source inductor.

As expected, in circuit model, the output voltage, $V_{O(MODEL)}(t)$, and the current through the Z-source inductor , $I_{L_Z(MODEL)}(t)$, has both the switching ripples and low frequency components upon the application of step disturbance, d. Also, both waveforms swing around DC value after the disturbance. The response of transfer function $G_{vd}(s)$, $V_{O(G_{vd})}(t)$, and the response of the transfer function $G_{id}(s)$, $I_{L_Z(G_{id})}(t)$, exactly follow the low frequency components of $V_{O(MODEL)}(t)$ and $I_{L_Z(MODEL)}(t)$ by discarding the switching ripples on $V_{O(MODEL)}(t)$ and $I_{L_Z(MODEL)}(t)$. This means that the expressions for the duty factor-to-output voltage transfer function, $G_{vd}(s)$, and duty factor-to-Z-source inductor current transfer function, $G_{id}(s)$, founded in (2.47) and (2.49), are correct.

The circuit in Fig.3.8 is drawn to simulate and verify the input voltage-to-output voltage transfer function, $G_{vg}(s)$ and input voltage-to-Z-source inductor current transfer function, $G_{ig}(s)$ for CCM operation. Circuit model is constructed according to the parameters in Table3.2. '$Duty-Factor$' block generates the required duty-factor signal to drive the circuit model in open-loop. The input voltage of the circuit model, V_S, is $30V$ and a $0.1V$ step disturbance, v_S, is added onto V_S after $100ms$ of the beginning of the simulation running. Also, the same step disturbance, v_S, is applied to the transfer functions $G_{vg}(s)$ and $G_{ig}(s)$. The responses of the transfer functions, $G_{vg}(s)$ and $G_{ig}(s)$, against the disturbance, v_S, are in time domain and swings around zero point. The average value of the output voltage, V_O, and average

value of the Z-source inductor, I_{L_Z}, is added to $G_{vg}(s)$ and $G_{ig}(s)$ transfer functions responses, respectively. This way, the circuit model output voltage, $V_{O(MODEL)}(t)$, and the response of $G_{vg}(s)$, $V_{O(G_{vg})}(t)$, against the step disturbance, v_S, can be examined simultaneously in detailed form. Similarly, the current, $I_{L_Z(MODEL)}(t)$, through the Z-source inductor in circuit model and the response of $G_{ig}(s)$, $I_{L_Z(G_{ig})}(t)$, against the step disturbance, v_S, can be observed simultaneously. The responses from $G_{vg}(s)$ and $G_{ig}(s)$ can be determined from (2.48) and (2.50), respectively. Substituting the parameters in Table3.2 into (2.48) yields;

$$G_{vg}(s) = \frac{-6.667 \cdot 10^{-10} s^2 + 0.2222}{2 \cdot 10^{-17} s^4 + 5 \cdot 10^{-15} s^3 + 1.033 \cdot 10^{-8} s^2 + 2.333 \cdot 10^{-6} s + 0.1111} \qquad (3.11)$$

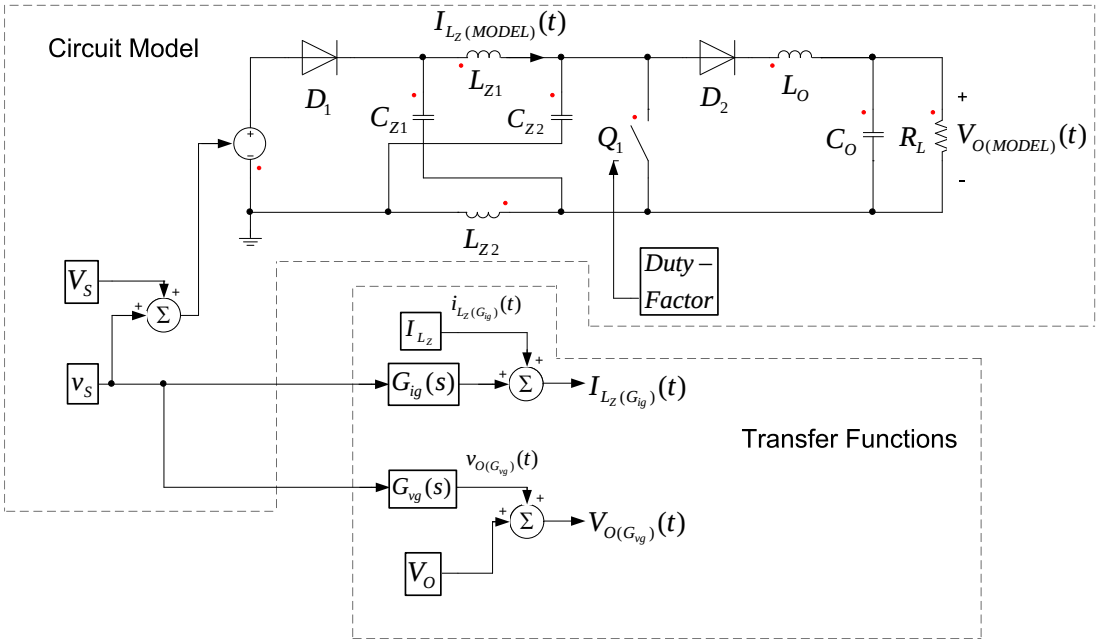

Fig.3.8 The circuit used for the verification of the validity of the transfer functions derived in modeling the converter, $G_{vg}(s)$ and $G_{ig}(s)$, in CCM operation

Similarly, substituting the same parameters into (2.50) gives;

$$G_{ig}(s)=\frac{6.667\cdot10^{-13}s^3+1.667\cdot10^{-10}s^2+2.111\cdot10^{-4}s+0.0444}{2\cdot10^{-17}s^4+5\cdot10^{-15}s^3+1.033\cdot10^{-8}s^2+2.333\cdot10^{-6}s+0.1111} \tag{3.12}$$

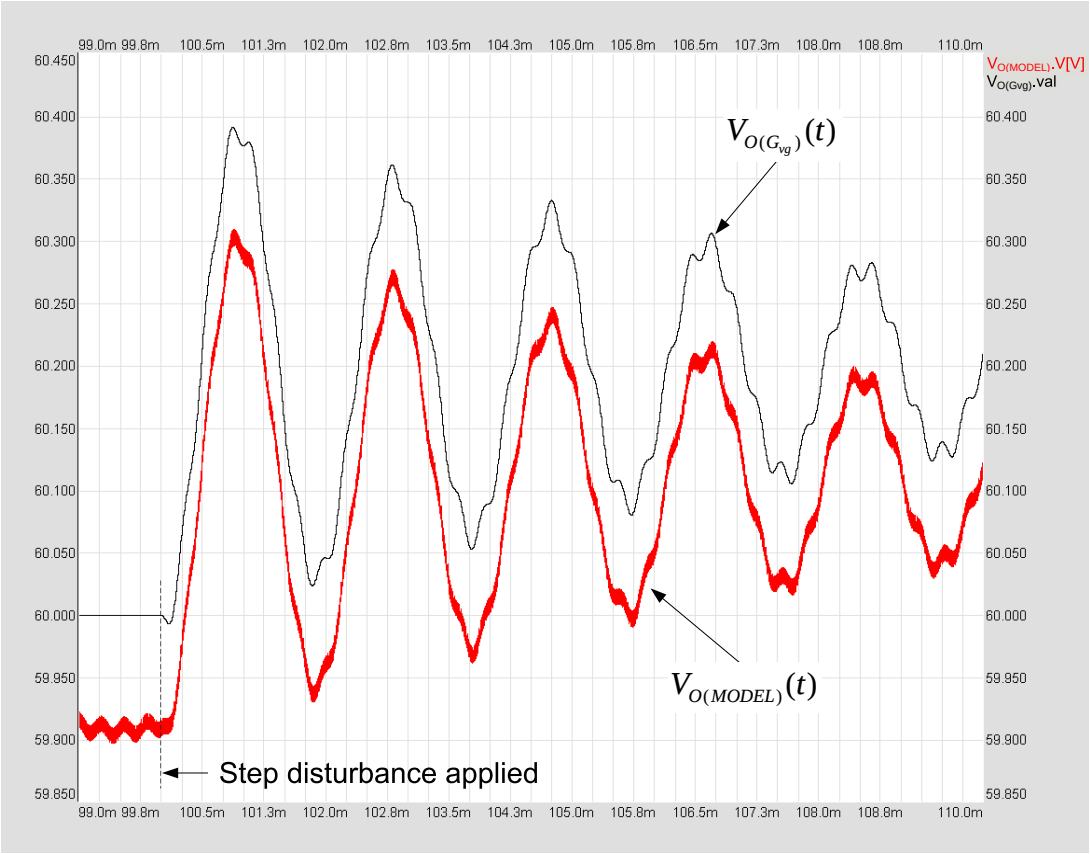

Fig.3.9 Responses against the step disturbance in input voltage, v_S; the output voltage, $V_{O(MODEL)}(t)$, in the circuit model (red); the output voltage, $V_{O(G_{vg})}(t)$, computed from the transfer function, $G_{vg}(s)$, (black) in CCM operation

The waveforms of the circuit model output voltage, $V_{O(MODEL)}(t)$, and the response of $G_{vg}(s)$, $V_{O(G_{vg})}(t)$, are displayed in Fig.3.9. From Fig.3.9, both $V_{O(MODEL)}(t)$ and

$V_{O(G_{vg})}(t)$ follow to each other after the step disturbance, v_S, is applied to the circuit model and to $G_{vg}(s)$. The output voltage of circuit model, $V_{O(MODEL)}(t)$, includes the switching ripples on it, on the contrary; the response of $G_{vg}(s)$, $V_{O(G_{vg})}(t)$, does not, as expected.

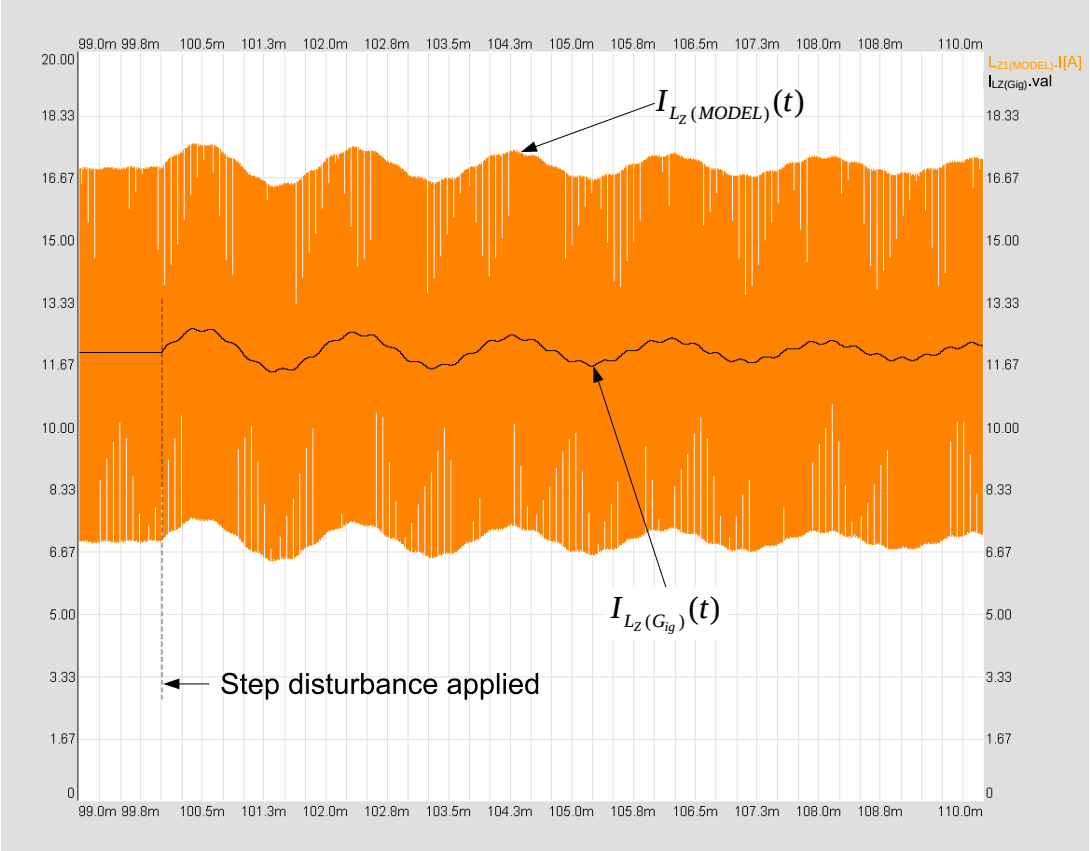

Fig.3.10 Responses against the step disturbance in input voltage, v_S; the envelop for the Z-source inductor current, $I_{L_Z(MODEL)}(t)$, in the circuit model (orange); the Z-source inductor current, $I_{L_Z(G_{ig})}(t)$, computed from the transfer function, $G_{ig}(s)$, (black) in CCM operation

Fig.3.10 displays the response of $G_{ig}(s)$, $I_{L_Z(G_{ig})}(t)$, and the current, $I_{L_Z(MODEL)}(t)$, through the Z-source inductor in circuit model simultaneously against the step disturbance, v_S. In Fig.3.10, although $I_{L_Z(MODEL)}(t)$ involves the switching ripple current, $I_{L_Z(G_{ig})}(t)$ includes only the low frequency dynamics caused by the input voltage step disturbance, v_S. Low frequency components of both signals follow each other.

Converter transfer functions are verified according to the simulation results. Responses of transfer functions, $G_{ig}(s)$ and $G_{vg}(s)$, includes only the low frequency dynamics of related terms by eliminating the switching ripples. Also, the low frequency components of the waveforms, obtained from circuit model and transfer functions, match to each other very well. Thus, it can be concluded that the expressions for transfer functions, $G_{ig}(s)$ and $G_{vg}(s)$, founded in Chapter 2 are correct.

3.3 Z-source Simulations in DCM Operation

3.3.1 Verification of Component Waveforms in DCM Operation

The Z-source dc/dc converter running in discontinuous current mode is simulated to give results which prove the validity of the model developed for the converter. In simulating the DCM operation, inductors and capacitors are chosen equal to those used in simulation for continuous current mode operation. The operating frequency is kept same as $100kHz$ and the desired output voltage is $60V$ again. However, in order to put the converter into discontinuous current mode operation the output power specification and setting has been reduced to $180W$ and the input voltage specification and setting has been increased to $45V$ from $30V$. The specifications of the simulated Z-source dc/dc converter, operates in DCM, are listed in Table3.3.

Table3.3 Main design parameters of the Z-source dc/dc converter in DCM operation

Input Voltage	V_S	45	V
Output Voltage	V_O	60	V
Output Power	P_O	180	W
Switching Frequency	f_S	100	kHz

The load resistance, R_L, for this discontinuous current mode operation results as;

$$R_L = \frac{{V_S}^2}{P_O} = \frac{60^2}{180} = 20\Omega \tag{3.13}$$

Inductors and capacitors being kept same as in the simulations of CCM operation, then, both Z-source inductors are $20\mu H$ and both Z-source capacitors are $50\mu F$. The output inductor, L_O, and the capacitor, C_O, taking place in the output filter portion of the circuit are $50\mu H$ and $400\mu F$, respectively. Selected components and parameters used in DCM operation are summarized in Table3.4.

The average value of the current through the inductor, I_{L_z}, is equal to the load current level. Thus, average current through the output inductor is,

$$I_{L_z} = I_L = \frac{V_O}{R_L} = \frac{60}{20} = 3A \tag{3.14}$$

In accord with the above given parameters the verification of the DCM operation of the converter can be tested by using (2.146). If the Z-source dc/dc converter is running in CCM operation, then the duty-factor, D, is to come out 0.2, which when substituted into (2.146) one obtains;

$$\frac{2}{20\times0.2\times10\times10^{-6}\times(1-0.4)}\leq\left(\frac{1}{50\times10^{-6}}+\frac{2}{20\times10^{-6}}\right) \tag{3.15}$$

Simplifying (3.15) we have $83333.33\leq120000$, the inequality holds, and therefore we understand that the converter is operating in DCM.

Table3.4 Z-source dc/dc converter parameters for DCM operation

Z-source inductors, L_Z	20	μH
Z-source capacitors, C_Z	50	μF
Output inductor, L_O	50	μH
Output capacitor, C_O	400	μF
Switching Frequency, f_S	100	kHz
Load resistance, R_L	20	Ω
Input voltage, V_S	45	V
Output voltage, V_O	60	V
Output current, I_L	3	A

Duty-factor, D, in DCM operation of the Z-source dc/dc converter can be calculated by (2.104). Reorganizing (2.104) leads to;

$$D=\sqrt{\frac{2\cdot\left(\frac{V_O}{V_S}-1\right)}{\left(\frac{1}{L_O}+\frac{2}{L_Z}\right)\cdot R_L\cdot T_S}} \tag{3.16}$$

Substituting the numerical data available into (3.16) yields duty-factor $D=0.1667$. The circuit model used in the simulation of operation in DCM is shown in Fig.3.11.

The '$Duty-Factor$' block generates the duty-factor 0.1667 with the frequency of $100kHz$. The waveform records are taken $60ms$ later the starting of the simulation so as to eliminate start-up transients which may appear on the waveforms. The output voltage of the circuit model, $V_{O(MODEL)}(t)$, is measured on the load resistance, R_L and it is expected to be $60V$.

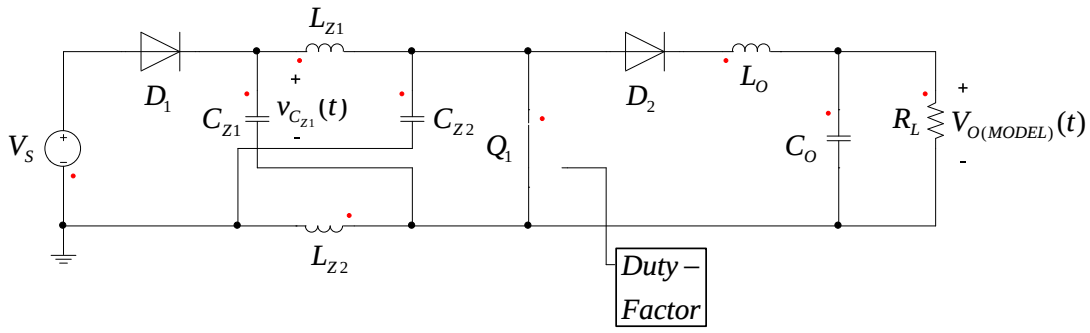

Fig.3.11 Circuit model of the Z-source dc/dc converter in DCM operation

Recalling from (2.75) that average value of the voltage, V_{C_z}, on the Z-source capacitance, C_Z is equal to output voltage, V_O. Thus, the average value of Z-source capacitor voltage, V_{C_z}, is also equal to $60V$. Fig.3.12 shows the output voltage, $V_{O(MODEL)}(t)$, and Z-source capacitor voltages, $v_{C_{Z1}}(t)$, waveforms, in comply with the expectations.

The waveforms regarding to the Z-source inductor current, $i_{L_z}(t)$, the Z-source capacitor current, $i_{C_z}(t)$, and the diode D1 current, $i_{D_1}(t)$, are demonstrated in Fig.3.13. The trace in red there shows duty-factor signal. When the duty-factor output is high, the switch Q_1 in the converter is 'ON' and Z-source inductor current, $i_{L_z}(t)$, starts increasing because it is energized from Z-source capacitor. In this time

interval, t_1, diode D_1 current, $i_{D_1}(t)$, and also the source current is zero. When the duty-factor output is low, the switch Q_1 is 'OFF' and for the converter operation t_2 time interval begins. Diode D_1 is now forward biased and the source current flows through it. Meanwhile, the Z-source inductor current, $i_{L_Z}(t)$, starts linearly decreasing so that it feeds power both to load, R_L, and the output inductor, L_O, thus energizing it. The last time interval, t_3, starts when diode D_1 current, $i_{D_1}(t)$, decays down zero. In t_3, Z-source inductor current, $i_{L_Z}(t)$, is constant, thus the voltage across the inductor, L_Z, is zero. Also, the load is now fed from only the Z-source capacitors, C_Z and output capacitor, C_O.

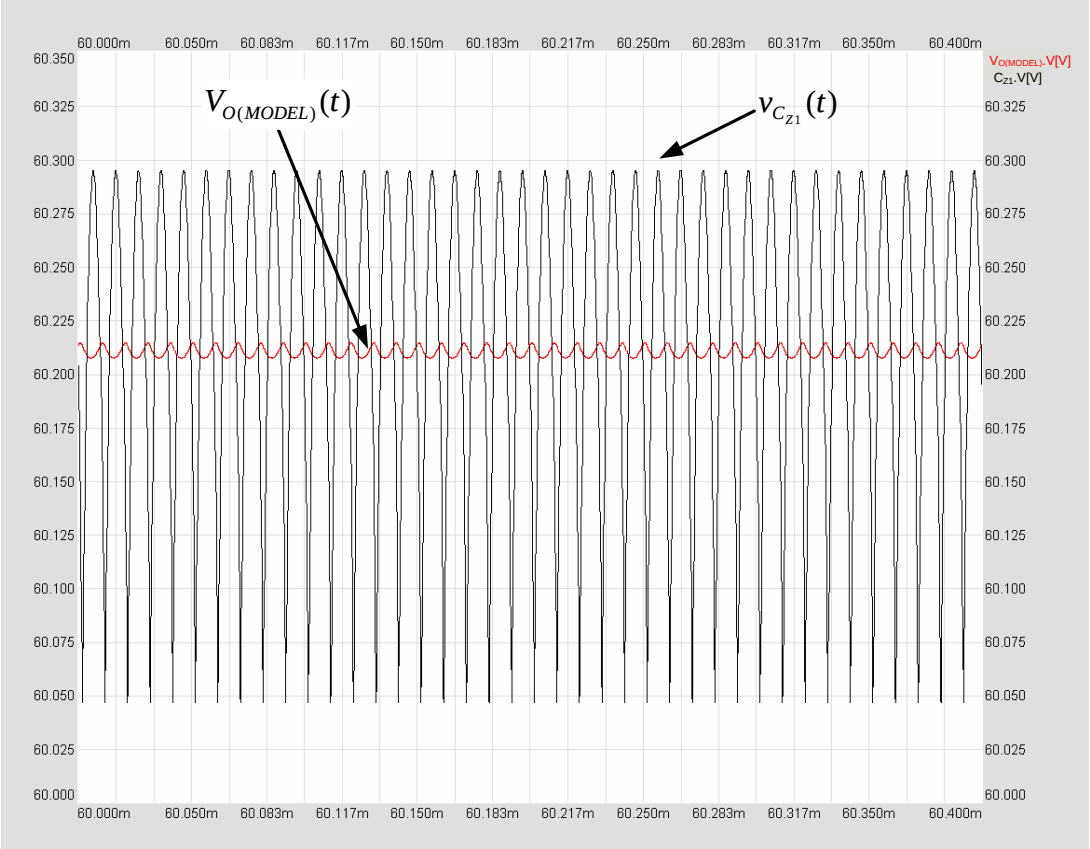

Fig.3.12 Voltage across the load resistor R_L, $V_{O(MODEL)}(t)$, (red), voltage across the Z-source capacitor C_{Z1}, $v_{C_{Z1}}(t)$, (black) in DCM operation

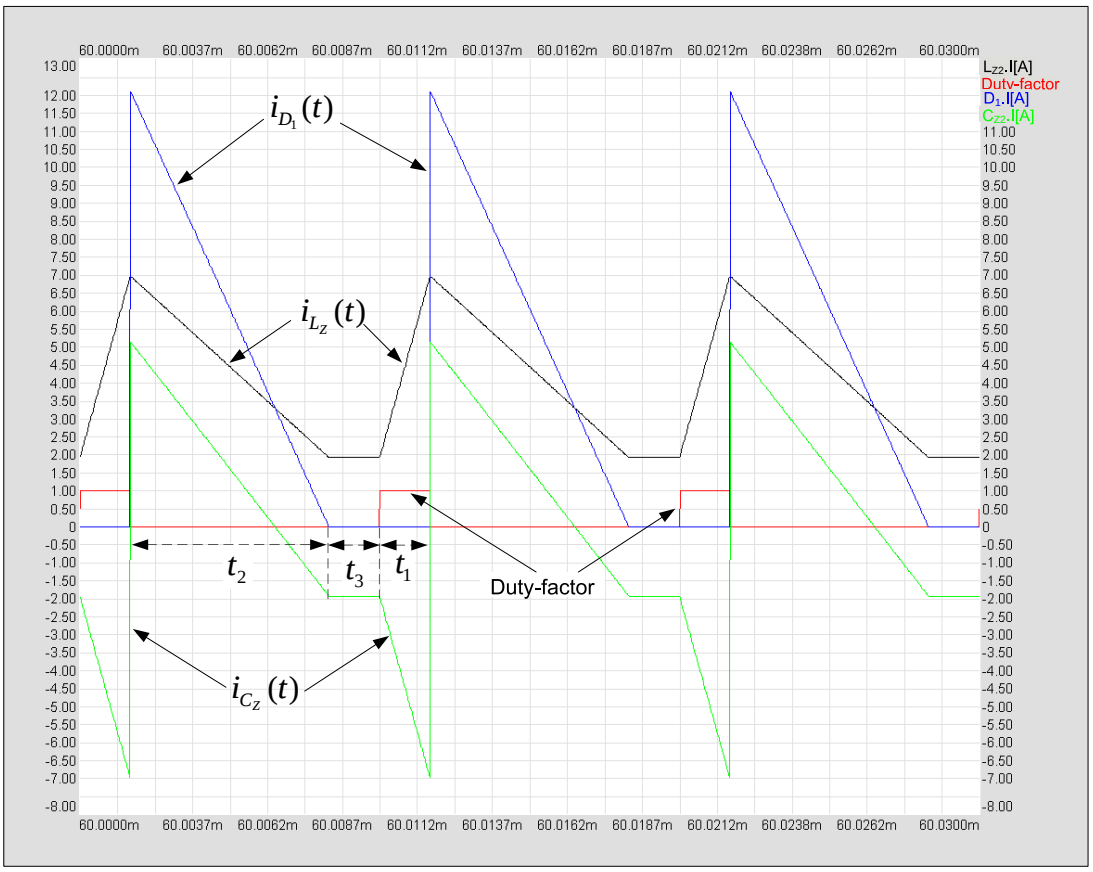

Fig.3.13 Duty-factor signal (red), diode D_1 current, $i_{D_1}(t)$, (blue), Z-source inductor current, $i_{L_z}(t)$, (black), Z-source capacitor current, $i_{C_z}(t)$, (green) in DCM operation

The expected peak-to-peak ripple, Δi_{L_z} ,in the current through the Z-source inductor, can be determined by (2.82) as;

$$\Delta i_{L_z} = I_{L_z(1)} - I_{L_z(3)} = \frac{V_O \cdot d \cdot T_S}{L_Z} = \frac{60 \cdot 0.1667 \cdot 10\mu}{20\mu} \cong 5A \qquad (3.17)$$

Note that in Fig.3.13, the inductor current, $i_{L_z}(t)$, swings between $1.9A$ and $6.9A$ thus, verifying the expectation.

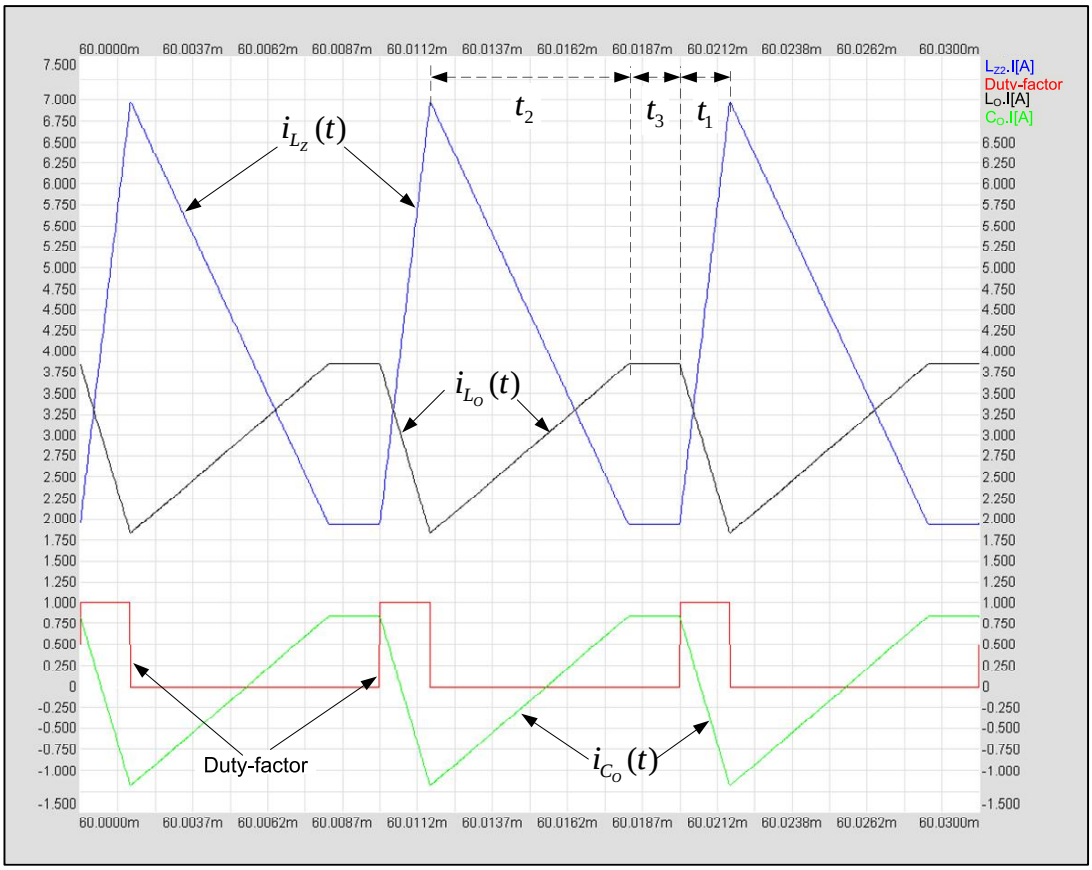

Fig.3.14 Duty-factor signal (red), Z-source inductor current, $i_{L_z}(t)$, (blue), output capacitor current, $i_{C_O}(t)$, (green), output inductor current, $i_{L_O}(t)$, (black) in DCM operation

The output inductor current, $i_{L_O}(t)$, the Z-source inductor current, $i_{L_z}(t)$, and the output capacitor current, $i_{C_O}(t)$, are shown in Fig.3.14 with the superimposed duty-factor output waveform. As can be followed in Fig.3.14, when the duty-factor output goes to high, t_1 period begins and the output inductor current, $i_{L_O}(t)$, starts decaying. Thus, the output inductor, L_O, transfers its stored energy to the load. When the duty-factor output becomes low, Q1 switch is 'OFF' and the output inductor, L_O, is energized from Z-source inductors, L_Z, in this time interval, t_2. Note that, the output capacitor, C_O feeds the load in t_2. When diode D_1 current,

$i_{D_1}(t)$, becomes zero, t_3 interval begins, the output inductor current, $i_{L_O}(t)$, stays constant and the voltage across the inductor, L_O, is zero like in Z-source inductors, L_Z.

Additionally, peak-to-peak ripple on the current, Δi_{L_O}, through the output inductor can be calculated by (2.84) as;

$$I_{L_O(3)} - I_{L_O(1)} = \frac{V_O \cdot d \cdot T_S}{L_O} = \frac{60 \cdot 0.1666 \cdot 10\mu}{50\mu} \cong 2A \tag{3.18}$$

Note again that, in Fig.3.14, the current of output inductor, $i_{L_O}(t)$, swings between $1.8A$ and $3.8A$. Thus, the peak-to-peak ripple on the current is $2A$ verifying the calculated value in (3.18). Recalling furthermore from (2.78), the output inductor current is to be twice of the Z-source inductor current, $i_{L_Z}(t)$, in time interval t_3. A close inspection of Fig.3.14 shows that the output inductor current, $i_{L_O}(t)$, is $3.8A$ and Z-source inductor current, $i_{L_Z}(t)$, is really half of $i_{L_O}(t)$ and $1.9A$. Thus, simulation results and waveforms comply with theoretical calculations and the expected waveforms given in Fig.2.22.

3.3.2 Verification of Transfer Functions in DCM Operation

In this section, validity of the duty factor-to-output voltage transfer function, $G_{vd-dcm}(s)$ and the input voltage-to-output voltage transfer function, $G_{vg-dcm}(s)$, for discontinuous current mode operation are investigated via simulations. Also, the small signal model validity is investigated. In simulation program, the circuit model of the converter, transfer functions and small signal model are run simultaneously and the resulting output waveforms are compared. The data given in Table3.4 are used as the parameters of the converter. The duty factor, D, is set to 0.1666 as found in (3.16) for the large signal model.

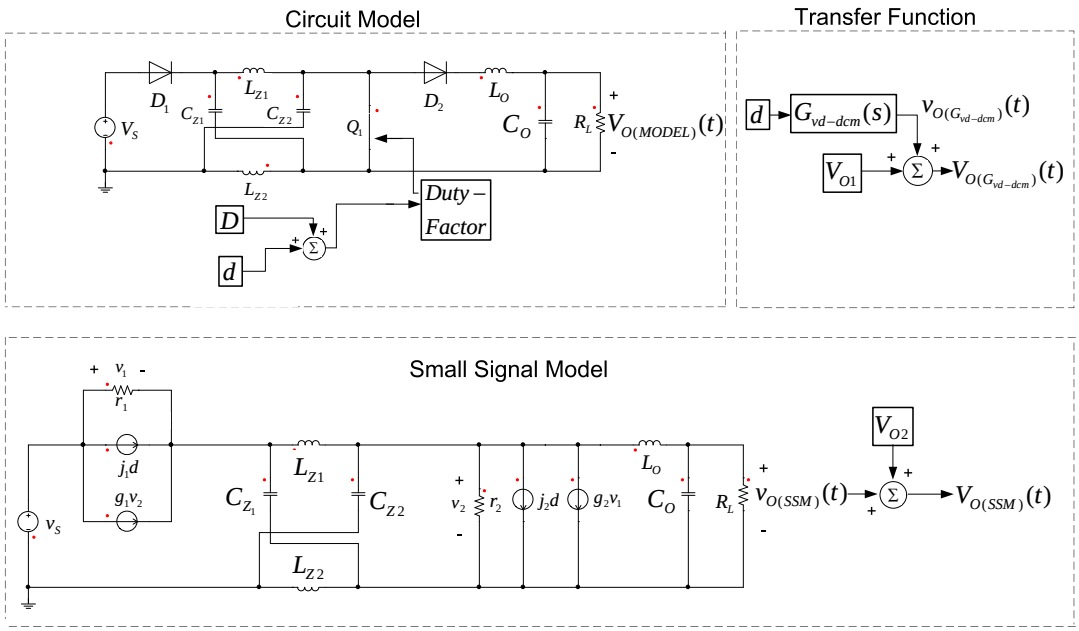

Fig.3.15 The circuit used for the verification of the validity of the transfer function derived in modeling the converter $G_{vd-dcm}(s)$ and small signal model in DCM operation

The circuit used in the simulation to verify duty factor-to-output voltage transfer function, $G_{vd-dcm}(s)$, and small circuit model is as shown in Fig.3.15. The aim of the circuit model is to observe the output voltage waveform against a small step disturbance added to the duty factor. The same step disturbance is also applied to the duty factor-to-output voltage transfer function, $G_{vd-dcm}(s)$, and the small signal model. '$Duty-factor$' block in Fig.3.15 generates again the duty-factor output for the circuit model. The duty factor applied to the circuit model is the sum of 'D' and 'd' blocks. 'D' is the constant value of the duty factor which is 0.1666. The step disturbance added to the duty factor, D, is shown as d ,which is set to 0.002, and added to D when the circuit model reaches steady state. Thus, the step disturbance, d, is applied after $60ms$ after the beginning of the simulation. '$G_{vd-dcm}(s)$' block, in Fig.3.15 represents the duty factor-to-output voltage transfer function. Upon application of d the output of '$G_{vd-dcm}(s)$' block swings around zero

point. Thereby, average value of the output voltage, V_{O1} is added to transfer function output. This way, the responses of the circuit model against the step disturbance in the duty-factor and the transfer function can be examined in detail.

In small signal model, the voltage source 'v_s' represents the small variations in the input voltage and in this simulation, to find $G_{vd-dcm}(s)$, it is set to zero. The nonlinear elements, diodes and switches, are replaced either by independent or dependent current sources and resistors as in Fig.2.25. r_1, j_1, g_1, r_2, g_2 and j_2 are determined using (2.127) and (2.130) by utilizing the circuit parameters given in Table3.4. When the disturbance in the duty-factor is applied to the small signal model, the excursions on output voltage, $v_{O(SSM)}(t)$, come out about zero. These variations in the small signal model output are added onto the average value of the output voltage, V_{O2}, when observed as '$V_{O(SSM)}(t)$' in Fig.3.15.

The numerical value of transfer function $G_{vd-dcm}(s)$ is obtained by using (2.133) as;

$$G_{vd-dcm}(s) = \frac{94.74}{1.053 \cdot 10^{-3} s + 0.5789} \tag{3.19}$$

This transfer function is installed in '$G_{vd-dcm}(s)$' block in simulation, as seen in Fig.3.15. The outputs of the circuit model, $V_{O(MODEL)}(t)$, the transfer function $G_{vd-dcm}(s)$, $V_{O(G_{vd-dcm})}(t)$, and the small signal model, $V_{O(SSM)}(t)$, are shown in Fig.3.16.

Verification of the validity of the input voltage-to-output voltage transfer function, $G_{vg-dcm}(s)$, in DCM operation can be obtained by conducting simulations of the system. The circuit which is simulated is seen in Fig.3.17. Note that this circuit is a modified version of that seen in Fig.3.15. The input voltage step disturbance, v_S, is added onto the value of input voltage, V_S, as seen in Fig.3.17. 'V_S' is the dc value the input voltage and it is $45V$. 'v_S' is a step function of 1V in amplitude and applied

after $60ms$ of simulation starting. This step disturbance, v_S, is the input of the voltage taking place in the small signal model shown in Fig.3.17.

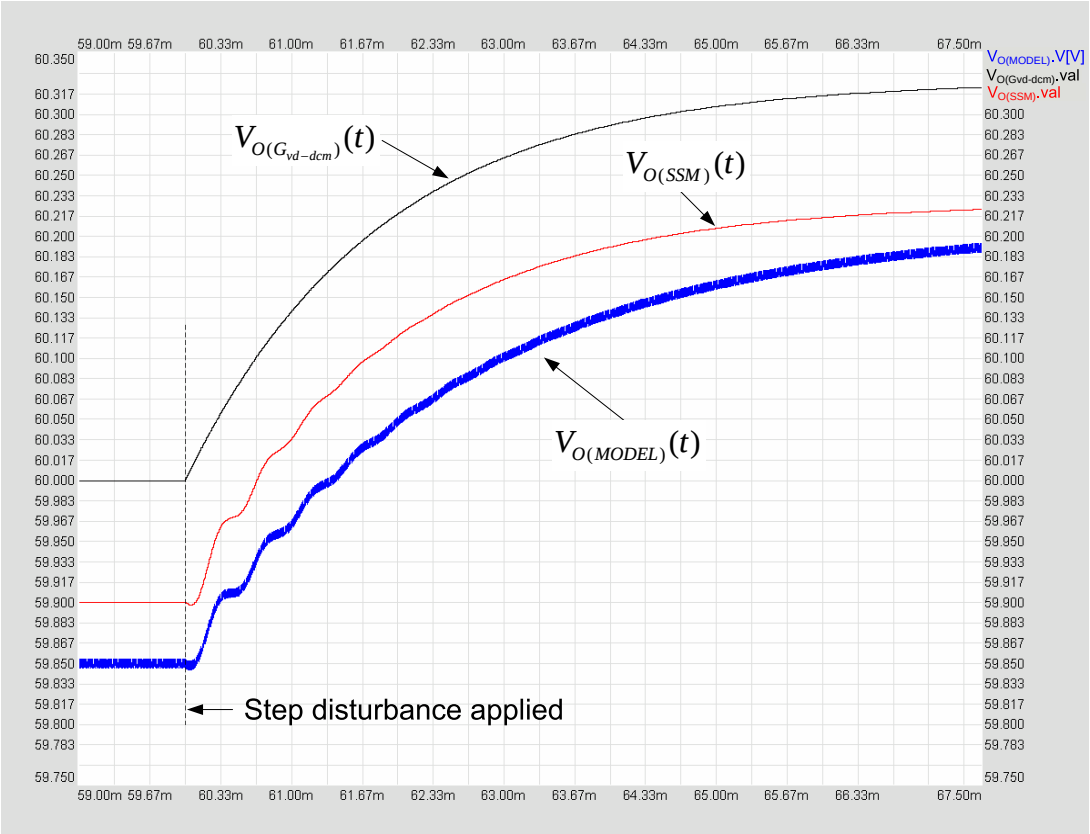

Fig.3.16 Responses against the step disturbance in duty factor, d ; the output voltage, $V_{O(MODEL)}(t)$, in the circuit model (blue); the output voltage, $V_{O(G_{vd-dcm})}(t)$, computed from the transfer function (black), $G_{vg}(s)$; the output voltage, $V_{O(SSM)}(t)$, in small signal model (red) in DCM operation

'$G_{vg-dcm}(s)$' in Fig.3.17 represents the input voltage-to-output voltage transfer function. The outputs of the small signal model, $v_{O(SSM)}(t)$, and $G_{vg-dcm}(s)$, $v_{O(G_{vg-dcm})}(t)$, are constructed for observation as '$V_{O(SSM)}(t)$' and '$V_{O(G_{vg-dcm})}(t)$' by

adding output voltage dc value 'V_{O2}' and 'V_{O1}', respectively. In this way, outputs of circuit model, small signal model and $G_{vg-dcm}(s)$ transfer function can be observed in detail simultaneously.

The numerical value of transfer function $G_{vg-dcm}(s)$ can be obtained by using (2.140) as;

$$G_{vg-dcm}(s) = \frac{7.111}{10^{-2}\,s + 5.5} \tag{3.20}$$

This transfer function is installed in '$G_{vg-dcm}(s)$' block in simulation as seen in Fig.3.17.

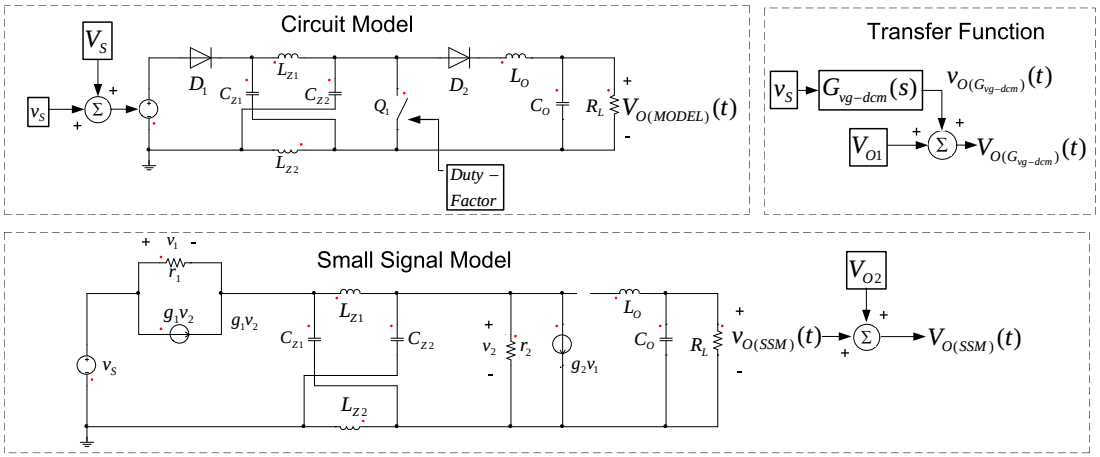

Fig.3.17 The circuit used for the verification of the validity of the transfer function derived in modeling the converter $G_{vg-dcm}(s)$ and small signal model in DCM operation

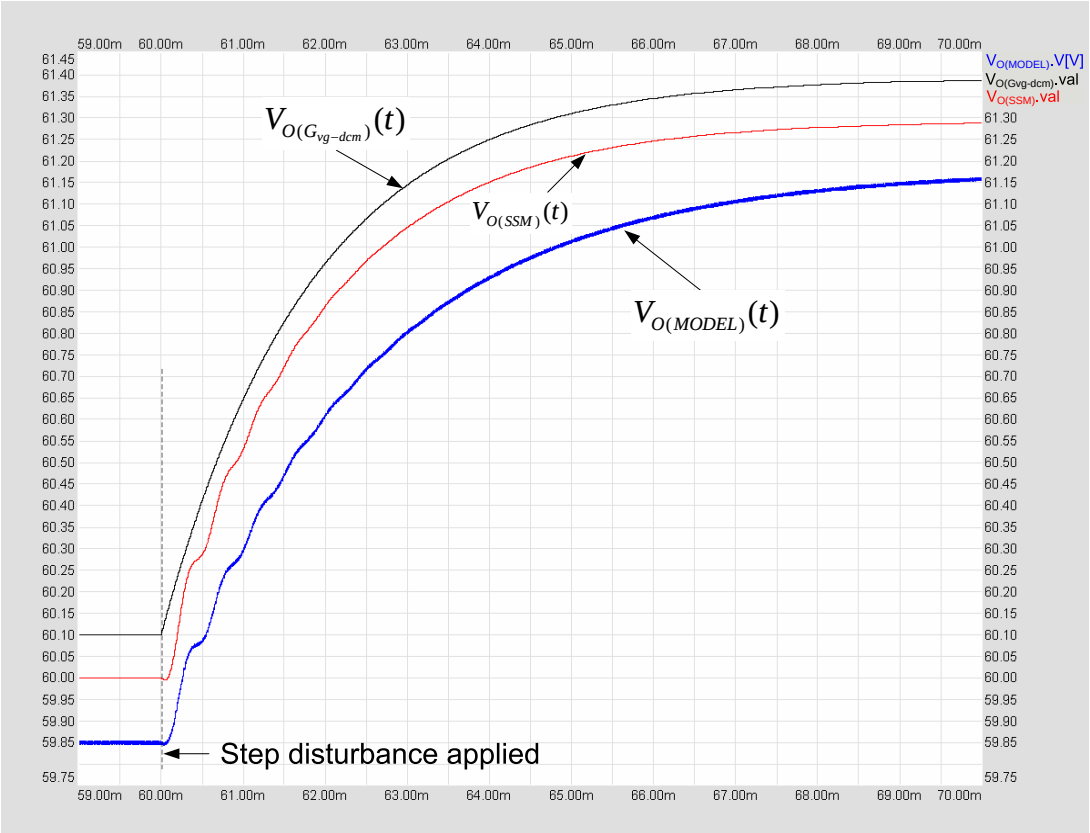

Fig.3.18 Responses against the step disturbance in input voltage, v_S; the output voltage, $V_{O(MODEL)}(t)$, in the circuit model (blue); the output voltage, $V_{O(G_{vg-dcm})}(t)$, computed from the transfer function, $G_{vg}(s)$, (black); the output voltage, $V_{O(SSM)}(t)$, in small signal model (red) in DCM operation

Fig.3.18 shows the outputs of the circuit model, $V_{O(MODEL)}(t)$, the transfer function, $G_{vg-dcm}(s)$, $V_{O(G_{vg-dcm})}(t)$, and the small signal model, $V_{O(SSM)}(t)$.Responses obtained for the circuit model and the small signal model against the step disturbances, d and v_S, involve oscillations at the beginning period of the transient. As $G_{vd-dcm}(s)$ and $G_{vg-dcm}(s)$ are transfer functions related to the first order systems, there are no oscillations at the response of these transfer functions. In determining $G_{vd-dcm}(s)$ and $G_{vg-dcm}(s)$ transfer functions, inductors are not taken into consideration because

it is assumed that inductors introduce poles and zeros at high frequencies. Due to this assumption and choice, there are no high frequency oscillations, which are exist at the beginning of circuit model and small signal circuit responses, in the response of the transfer functions. The outputs of small signal model and the power stage are exactly matching including the oscillations, because the small signal model involve inductors. Furthermore, the output of Z-source dc/dc converter has ripple at the switching frequency but the outputs belonging to the small signal model and the transfer function do not involve ripples at the switching frequency.

3.4 Z-source Full Bridge DC/DC Converter Simulations

In Chapter 2, it is assumed that, the Z-source full bridge dc/dc converter, shown in Fig.2.1, can be reduced to circuit as in Fig.2.2. Also, the model of the converter and input-output relationships are developed using that reduced circuit. Thus, it is expected that, the waveforms obtained in the simulations related to electrical variables associated with inductors and capacitors taking place in the Z-source full-bridge dc/dc converter are almost same with those obtained in reduced circuit simulations.

Z-source full-bridge dc/dc converter simulations are carried out both for CCM and DCM operations. The circuit used for simulations is as shown in Fig.3.19. The input supply 'V_S' here is set to 30V. Inductors and capacitors are same as in Table3.2. Thus, Z-source inductors, L_{Z1} and L_{Z2}, are $20\mu H$ and, Z-source capacitors, C_{Z1} and C_{Z2}, are $50\mu F$. The output inductor, L_O, and the output capacitor, C_O, are set to $50\mu H$ and $400\mu F$, respectively. The electrical isolation between input and output is achieved by using the transformer 'Tr'. In simulation, the magnetizing and leakage inductances of the transformer are set to measured ones obtained from prototype circuit. The magnetizing inductance of the transformer, L_M, is measured from the primary side of the transformer when the secondary open circuited side and the leakage inductance, L_l, is measured from primary side by short-circuiting the secondary side of the transformer. Both L_M and L_l measurements are made at the switching frequency of the transformer, $50kHz$, by using Precision LCR Meter, HP-4285A from Hewlett company. L_M and L_l are measured as $600\mu H$ and $0.8\mu H$,

respectively. Since both winding resistances on primary and secondary sides are very small and could not be measured precisely they are determined computationally as can be followed in Chapter 4.5.5. The computation gives us $4.7m\Omega$ for both windings. This value is used in simulations. The load resistance, R_L, is set to 10Ω and draws $360W$ output power. The forward voltage drops on the diodes at the rated current for D_1, D_2, D_3, D_4 and D_5 are considered to be $0.7V$.

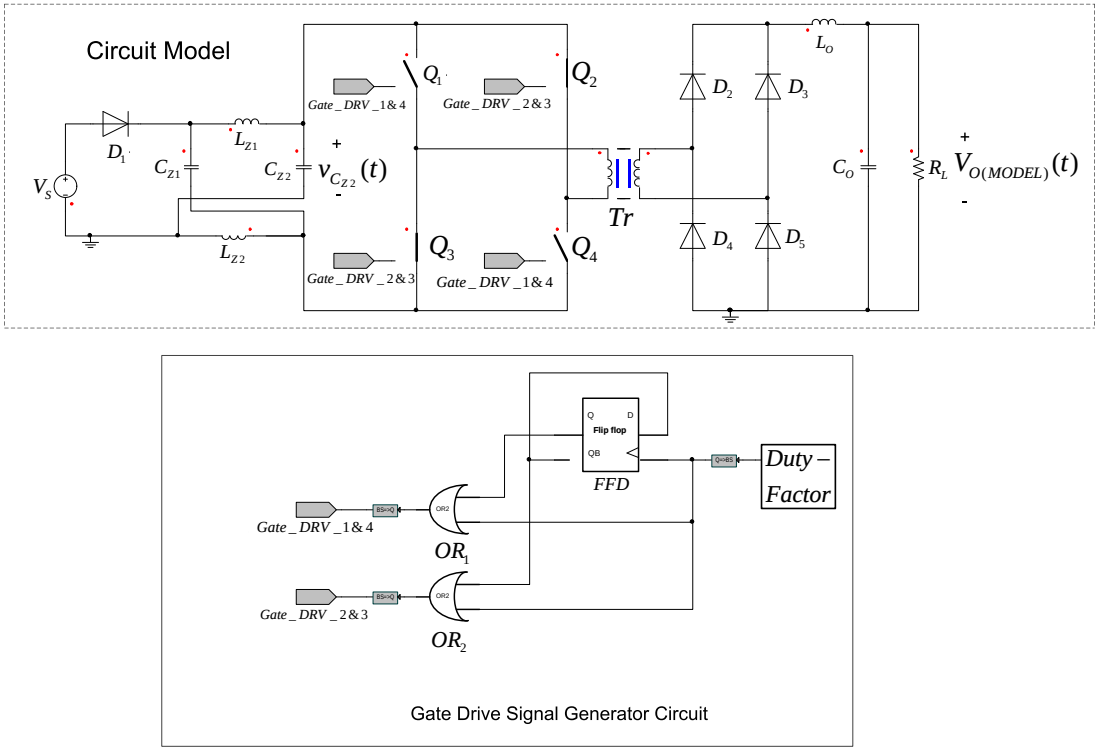

Fig.3.19 Z-source full bridge dc/dc converter power stage and gate drive signal generator circuit

Gate Drive Signal Generator Circuit in Fig.3.19 generates necessary gate drive signals for the switches Q_1, Q_2, Q_3 and Q_4 from '$Duty-factor$' block. When the duty-factor output goes high, all switches in the circuit close and the input is short circuited. Also, when the duty-factor output becomes low, one of the switch pairs

'(Q_1 and Q_4) or (Q_2 and Q_3)' becomes conducting. The conduction of one pair pursues the other. For the first period, if the switch pair, (Q_1 and Q_4), is in conduction then, for the second period, switch pair, (Q_2 and Q_3), will be conducting. This sequence in gate driving is derived from one duty-factor output. Gate Drive Signal Generator Circuit has been designed for this purpose. Fig.3.20 shows the duty-factor signal, OR_1 gate and OR_2 gate outputs.

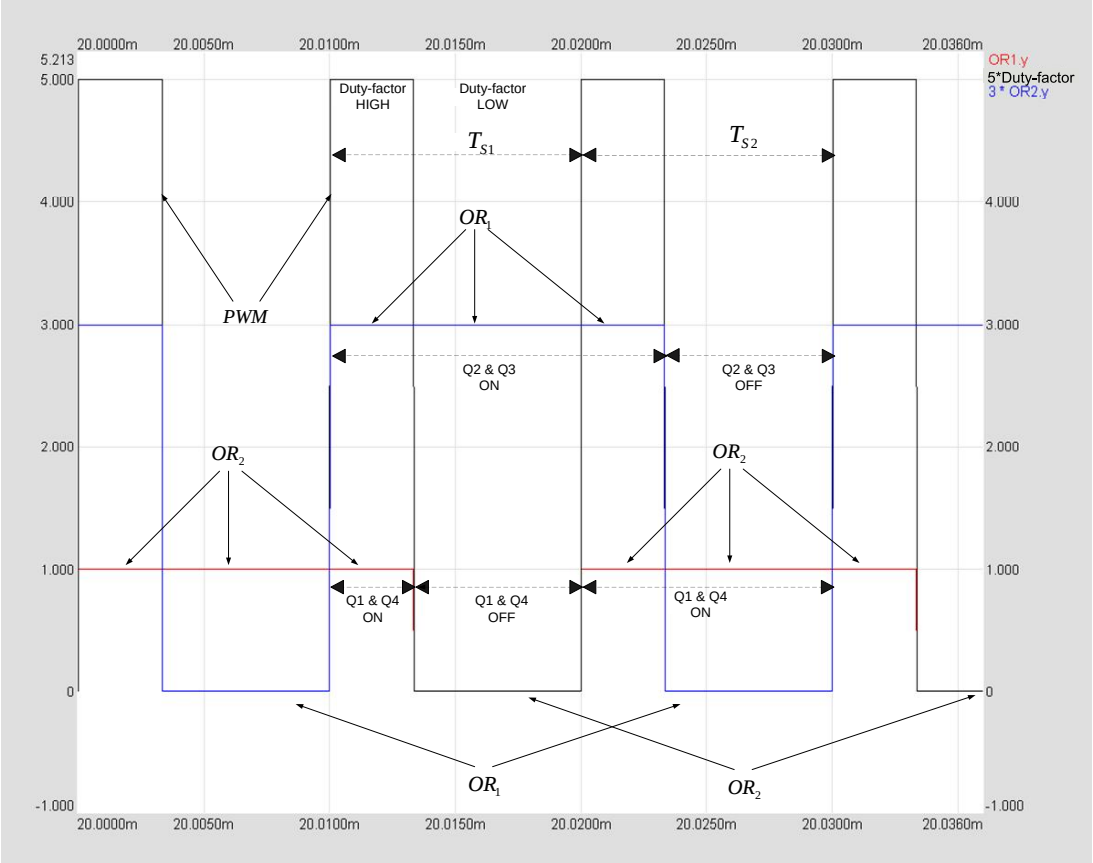

Fig.3.20 Gate drive signal generator circuit outputs: Duty-factor signal (black), OR1 (red), OR2 (blue)

*(for the sake of clarity the Duty-factor waveform is multiplied by 5 and output of OR2 gate is multiplied by 3)

The output of OR_1 is being high means that the switches Q_1 and Q_4 are in conduction. Similarly, if the output of OR_2 is high, the switches, Q_2 and Q_3, are in conduction. In the first period, T_{S1}, when the duty-factor output is high, all the switches are in conduction as shown in Fig.3.20. When the duty-factor drops to low in T_{S1}, Q_1 and Q_4 becomes 'OFF' and switch pair, Q_2 and Q_3, is still in transmission. By the duty-factor being high at beginning of second period, T_{S2}, all the switches are in conduction again. In the second period, T_{S2}, when duty-factor output is low, Q_2 and Q_3 becomes low and Q_1 and Q_4 are still in conduction. By this sequence driving of the switches, shoot-through operation is achieved by duty-factor being high and ac square voltage across the transformer is created. Also, the voltage across the primary side of transformer is zero at shoot-through stage. Furthermore, this gate drive circuit is used both in CCM and DCM operations.

3.4.1 Z-source Full Bridge DC/DC Converter Simulations in CCM Operation

For the CCM simulations of the full bridge dc/dc converter, the duty factor is adjusted to 0.333, as found in (3.3), to get $60V$ output voltage. The output voltage is equal to the voltage across R_L and it is as shown in Fig.3.21. Also, recalling from (2.14) that the dc value for the Z-source capacitance, V_{C_z}, is equal to the output voltage, V_O. Thus, Fig.3.21 shows that the Z-source capacitor voltage verifies (2.14). Although, it is expected that the output voltage is $60V$, in Fig.3.21, it is about $56.1V$. The slight deviation in V_O is due to the forward voltage drop on diodes, and the losses at the transformer because of the high switching frequency. The Z-source capacitor voltage, V_{C_z}, is much closer to $60V$ than the output voltage, V_O, because it is not affected from the forward voltage drop of diodes D_2, D_3, D_4 and D_5. The dc voltage on the Z-source capacitor, V_{C_z}, is about $58V$.

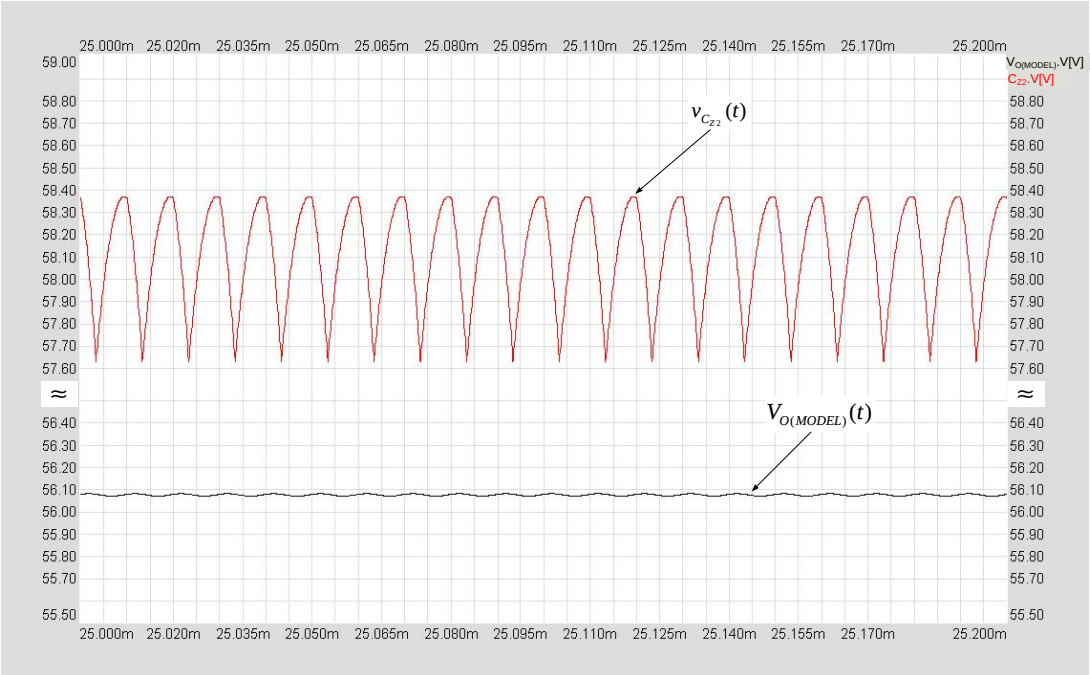

Fig.3.21 Z-source full bridge dc/dc converter in CCM operation: Z-source capacitor voltage (red) and output voltage (black)

Fig.3.22 shows the inductor current, $i_{L_z}(t)$, the capacitor current, $i_{C_z}(t)$, and the diode D_1 current, $i_{D_1}(t)$, together with the duty-factor output for Z-source full-bridge dc/dc converter operating in CCM. When duty-factor output is high, the transformer primary winding is short circuited. In this time interval, t_1, diode D_1 is reversed biased and the Z-source capacitors feed the Z-source inductors and energize them. When the duty-factor output becomes low, D_1 is forward biased and the Z-source capacitors charge. Also, the Z-source inductors deliver the stored energy in their magnetic medium to the load.

Waveforms displayed in Fig.3.22 comply with those shown in Fig.3.3. Thus, we may conclude that the reduced circuit, shown in Fig.2.2, is functionally same with the actual Z-source full-bridge dc/dc converter, shown in Fig.2.1. The peak values for the Z-source inductor current and diode D_1 current are slightly different than those shown in Fig.3.3, because in the full-bridge simulation diodes and the transformer are not chosen as ideal , so there are some losses across these components. At the

falling edge of the duty-factor signal there are high frequency peaks at the Z-source capacitor, $i_{C_z}(t)$, and input diode, $i_{D_1}(t)$ current waveforms. The reason of these high frequency peaks is the leakage inductance, L_l, of the transformer. If the leakage inductance, L_l, of the transformer is increased the magnitude of these peaks are increased also. If the leakage inductance, L_l, of the transformer is set to zero, the high frequency peaks at the Z-source capacitor, $i_{C_z}(t)$, and input diode, $i_{D_1}(t)$ current waveforms are vanished.

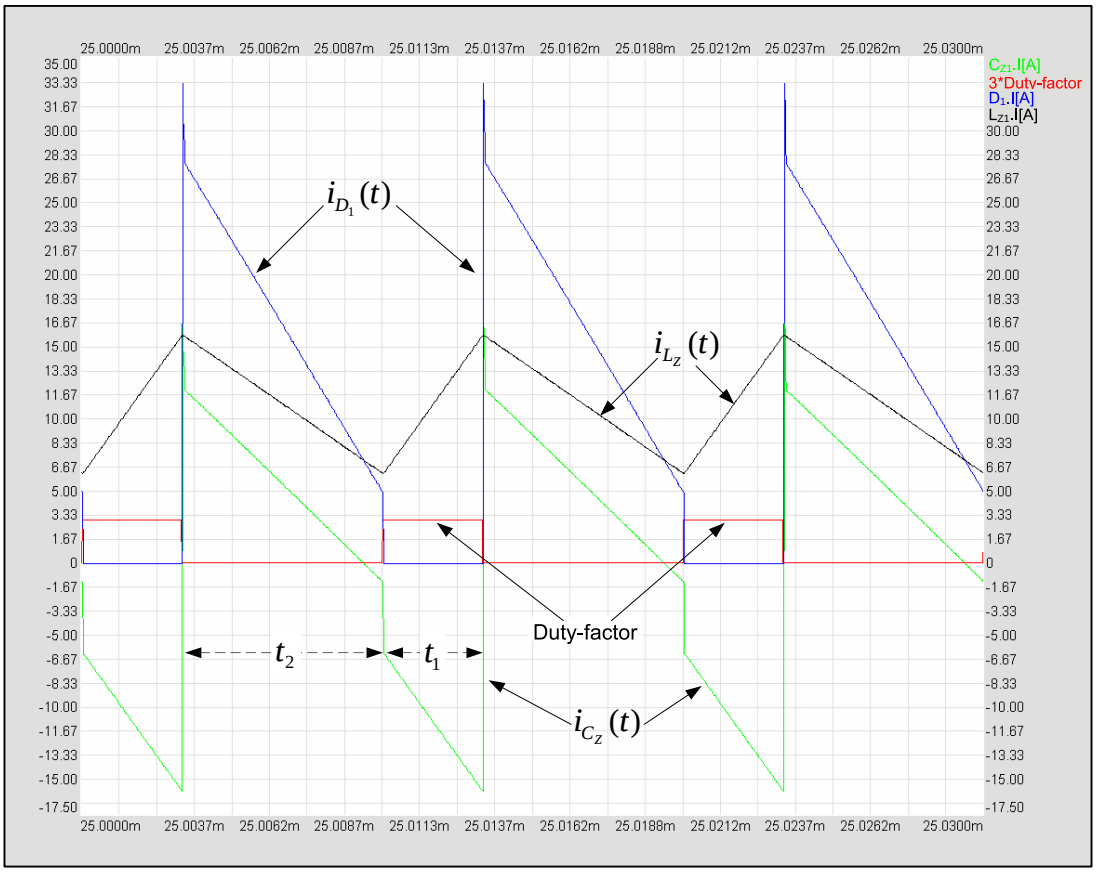

Fig.3.22 Z-source full bridge dc/dc converter in CCM operation: Duty-factor signal (red), diode D_1 current, $i_{D_1}(t)$, (blue), Z-source capacitor current, $i_{C_z}(t)$, (green), Z-source inductor current, $i_{L_z}(t)$, (black)

*(for the sake of clarity the Duty-factor waveform is multiplied by 3)

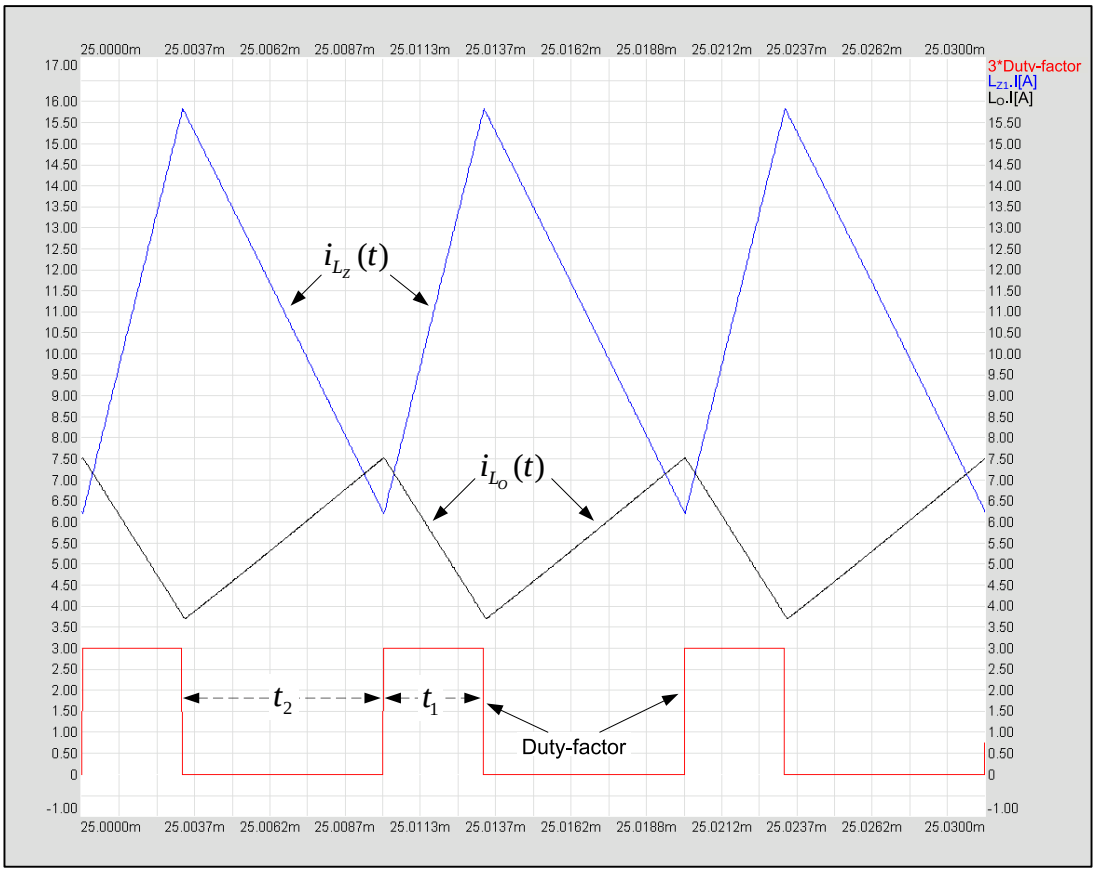

Fig.3.23 Z-source full bridge dc/dc converter in CCM operation: Duty-factor signal (red), output inductor current, $i_{L_o}(t)$, (black), Z-source inductor current, $i_{L_z}(t)$, (blue) *(for the sake of clarity the Duty-factor waveform is multiplied by 3)

Fig.3.23 shows waveforms for the output inductor current, $i_{L_o}(t)$, the output capacitor current, $i_{C_o}(t)$, and the Z-source inductor current, $i_{L_z}(t)$, together with the duty-factor output waveform in a Z-source full bridge dc/dc converter. The waveforms for the output inductor current, $i_{L_o}(t)$, and Z-source inductor current, $i_{L_z}(t)$, resulting from the applied duty-factor signal comply with the waveform, shown previously in Fig.3.4. When duty-factor output is high, output inductor current decays and transfers the stored energy to the load. Also, Z-source inductor, L_Z, stores energy at the time interval, t_1. While the duty-factor output is low at time interval t_2, the output inductor current, $i_{L_o}(t)$, rises and L_O stores energy. Z-source

inductor current decays at t_2. The slight changes noted in inductor currents are due to the non-idealities in the transformer and diodes D_1, D_2, D_3, D_4 and D_5.

3.4.2 Z-source Full Bridge Converter Simulations in DCM Operation

The same circuit in Fig.3.19 is used for the simulating the full-bridge Z-source dc/dc converter operating in DCM. The sizes of inductors and capacitors and the switching frequency are kept same as in Table3.2. However, in order to force the Z-source full bridge dc/dc converter running in DCM operation, the input voltage, V_S, is increased to $45V$ and the output load resistance, R_L, is increased to 20Ω. The parameters are same with those summarized in Table3.4. To get $60V$ output voltage, V_O, duty-factor block is set to 0.1666 as dictated by (3.16). Recalling from (2.75) that the DC value of Z-source capacitor voltage, V_{C_z}, is equal to the output voltage, V_O. Also, waveforms for the output voltage, $v_O(t)$, and the Z-source capacitor voltage, $v_{C_z}(t)$, resulting from the simulation are shown in Fig.3.24. Although, the expected amplitude for V_O is $60V$, it has resulted about $58V$ in the simulation. Like in Z-source full bridge dc/dc converter simulations in CCM operation, the reasons of this slight deviation are the non-ideal diodes and transformer present in the system.

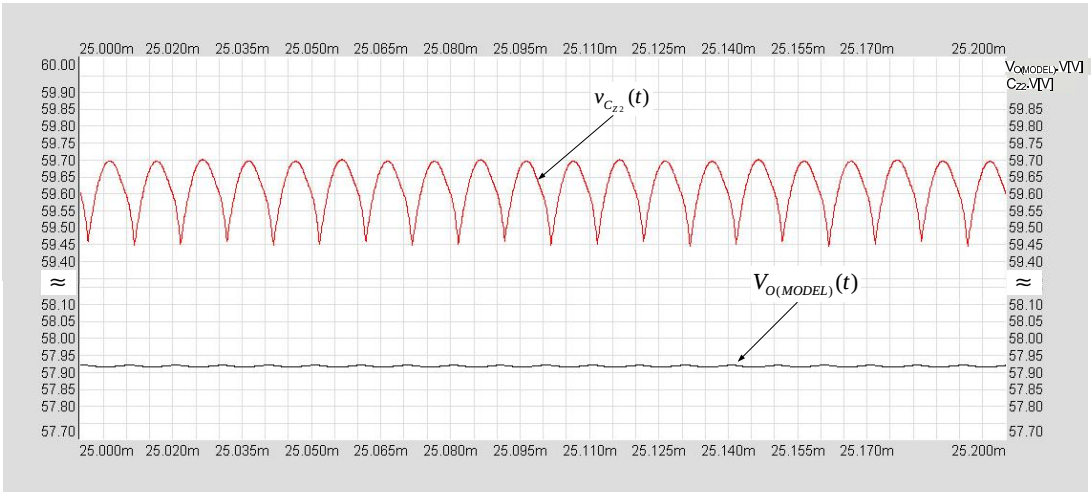

Fig.3.24 Z-source full bridge dc/dc converter in DCM operation: Z-source capacitor voltage (red) and output voltage (black)

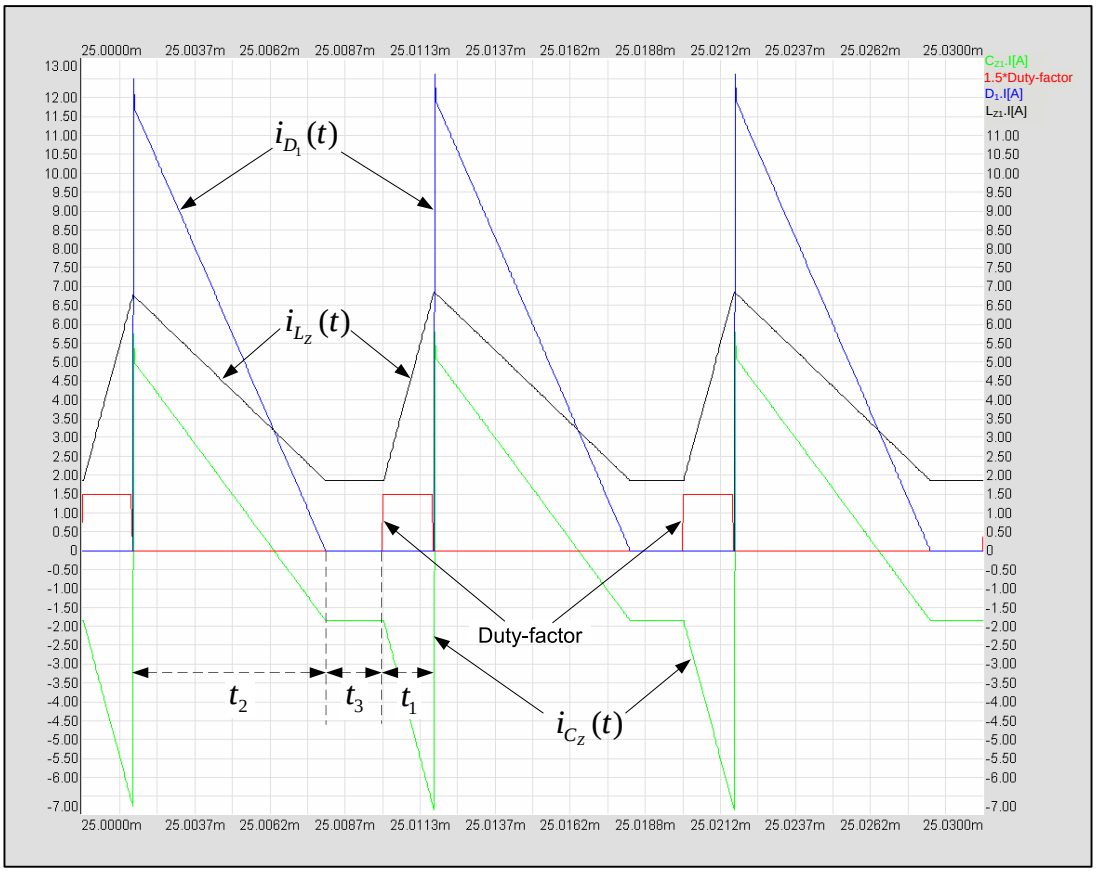

Fig.3.25 Z-source full bridge dc/dc converter in DCM operation: Duty-factor signal (red), diode D_1 current, $i_{D_1}(t)$, (blue), Z-source capacitor current, $i_{C_z}(t)$, (green), Z-source inductor current, $i_{L_z}(t)$, (black)

*(for the sake of clarity the Duty-factor waveform is multiplied by 1.5)

Current waveforms regarding the Z-source inductor, L_Z, the Z-source capacitor, C_Z, and diode D_1 for the full-bridge Z-source dc/dc converter under the applied duty-factor signal waveform are all shown in Fig.3.25. Referring to Fig.3.25, when the duty-factor is high, no current passes through the diode D_1 and Z-source capacitors feed energy to Z-source inductors. By the duty-factor output being low, the diode D_1 forward biased and energy is delivered to change Z-source capacitors from the source. Later when the D_1 current drops down to zero, the Z-source

inductor current, $i_{L_z}(t)$, stays constant for the rest of the switching period. Thus, it is concluded that, the converter is operating in DCM.

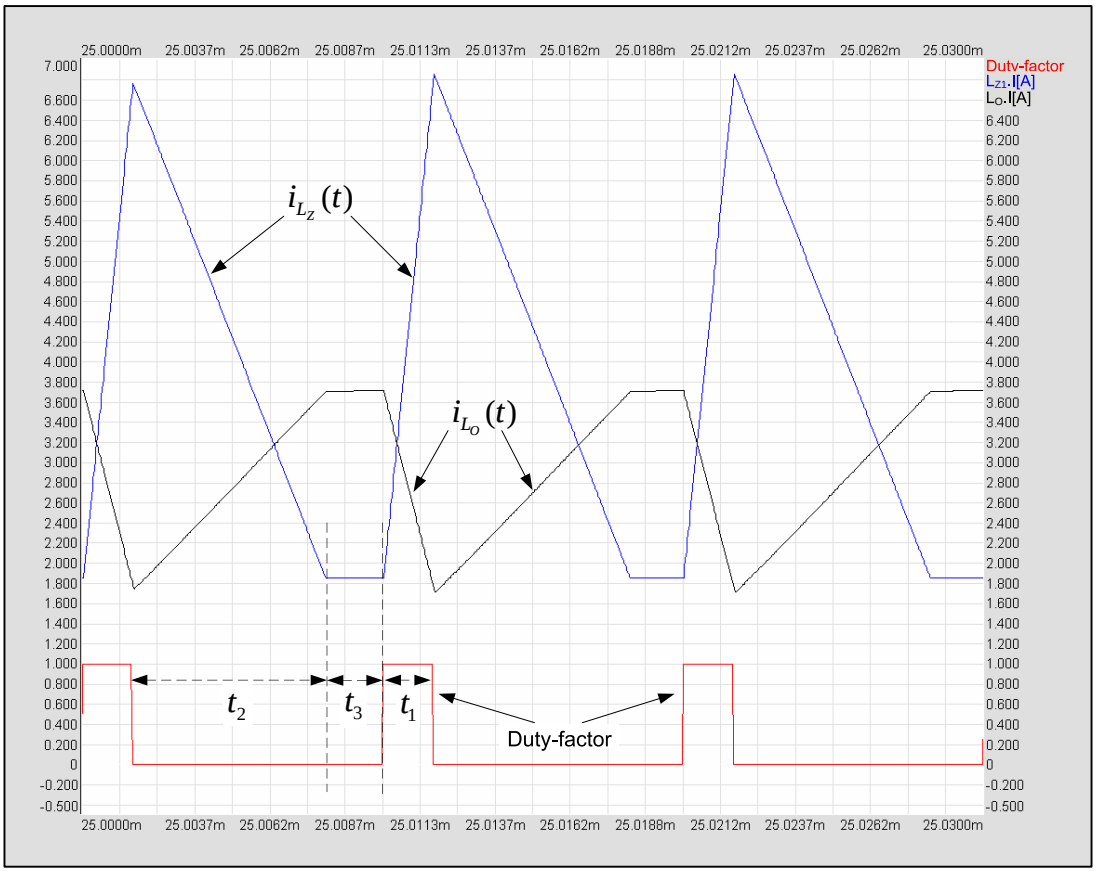

Fig.3.26 Z-source full bridge dc/dc converter in DCM operation: Duty-factor signal (red), Z-source inductor current, $i_{L_z}(t)$, (blue), output inductor current, $i_{L_o}(t)$,(black),

The complementing waveform of the output inductor current, $i_{L_o}(t)$, is shown in Fig.3.26 together with Z-source inductor current, $i_{L_z}(t)$. The output inductor current is decreasing in t_1 time interval accounting for deliver of its energy to the load when the duty-factor is high. Meanwhile, Z-source inductor, L_Z, is storing energy as the rising inductor current depicts the fact. When the duty-factor is low, the Z-source

inductor, L_Z, delivers its stored energy to the load and the output inductor, L_O. Thus, the output inductor stores energy. In time interval t_3, the currents on both Z-source and output inductors, stay constant, thus the back emfs across them are zero. Note that by (2.80) that the current on output inductor, $i_{L_O}(t_3)$, is twice the magnitude of the current on Z-source inductor, $i_{L_Z}(t_3)$, at t_3. A close inspection of Fig.3.26 shows that the Z-source inductor current, $i_{L_Z}(t)$, is about $1.85A$ and output inductor current, $i_{L_O}(t)$, is really twice of $i_{L_Z}(t)$ as $3.7A$. The waveforms in Fig.3.25 and Fig.3.26 comply with the waveforms shown in Fig.3.13 and Fig.3.14. Thus, we may accept that reducing the Z-source full bridge dc/dc converter into the form in Fig.2.2 is quite a good approximation.

3.5 Controller Design of the Z-source DC/DC Converter

In this section, a controller is to be designed which will satisfactorily function both in CCM and DCM operations for Z-source dc/dc converter. For CCM and DCM operations requiring parameters are to be set in accordance with the data given in Table3.2 and Table3.4. Thus, the duty factor-to-output voltage transfer function for CCM operation, $G_{vd}(s)$, and duty factor-to-output voltage transfer function for DCM operation, $G_{vd-dcm}(s)$ are given in (3.9) and (3.19), respectively. A unique voltage controller, $G_C(s)$, is designed to compensate both $G_{vd}(s)$ and $G_{vd-dcm}(s)$. The product of $G_{vd}(s)$ and $G_C(s)$ is the open-loop transfer function for CCM operation, $G_{OPEN-CCM}(s)$, and the product of $G_{vd-dcm}(s)$ and $G_C(s)$ is the open-loop transfer function for DCM operation, $G_{OPEN-DCM}(s)$. The phase and gain margins of the open-loop transfer functions, $G_{OPEN-CCM}(s)$ and $G_{OPEN-DCM}(s)$, are determined by utilizing MATLAB software program.

In voltage method, the output voltage, V_O, is controlled (or regulated) by manipulating the duty factor only. In other words, the output voltage can be maintained constant by adjusting duty factor under varying load and input voltage conditions. Thus, the transfer function, $G_{vd}(s)$, must be controlled to get a stable

system in this control method. When $G_{vd}(s)$'s bode plot is investigated, shown in Fig.3.27, it can be seen that there are two resonance frequency of the transfer function. The reason of this is that Z-source dc/dc converter has two inductor-capacitor pairs. One of these pairs comprises the Z-source inductor, L_Z, and the Z-source capacitor, C_Z, and the other pair is made of the output inductor, L_O, and output capacitor, C_O. These inductors and capacitors bring two imaginary pole pairs to the denominator of transfer function which leads to the two above referred resonant frequencies. Also, at these resonant frequencies ($3310 rad/\sec$ and $22500 rad/\sec$ for the given parameter set) the phase of the transfer function goes down by $180°$ as expected.

The detailed explanation of the gain and the phase margins of a closed-loop transfer function is given in [17]. The summary of the discussion given in [17] is that for stability both the phase margin and the gain margin must be made positive. Also, for a good performance of a controller, the phase margin should be greater than $30°$ and the gain margin should be greater than 6dB. In [18], it is stated that phase margin of the open-loop gain should be set to an angle greater than $60°$ and gain margin should be set to a value greater than 12 dB.

If the unity negative feedback is applied to $G_{vd}(s)$ than it can be observed from the Fig.3.27 that the gain margin is negative. Thus, the overall system will be unstable in this condition. A type 2 controller, which involves two poles (one of these poles is placed at origin) and a zero, is designed to stabilize the converter. To damp the gain of the transfer function, $G_{vd}(s)$, one pole is placed at origin in the controller transfer function, $G_C(s)$. This way, $G_{OPEN-CCM}(s)$ gain decays 20dB starting from $0Hz$. However, setting this pole to origin shifts the phase by $-90°$ and the phase of $G_{OPEN-CCM}(s)$ starts from $-90°$ instead of $0°$. The phase of $G_{OPEN-CCM}(s)$ should be increased before the first resonance frequency, $3310 rad/\sec$, because at resonance frequency the phase drops by $180°$. Thus, a zero is placed in the controller transfer function before the first resonant frequency, $3310 rad/\sec$. This way, the phase of the open-loop transfer function, $G_{OPEN-CCM}(s)$, starts increasing as of the frequency that the zero is placed. The drawback of placing the zero is

stopping the 20dB decaying at the gain of $G_{OPEN-CCM}(s)$. Thus, the second pole is placed between the frequency, the zero is placed, and the first resonance frequency to continue the 20dB decaying of $G_{OPEN-CCM}(s)$ gain.

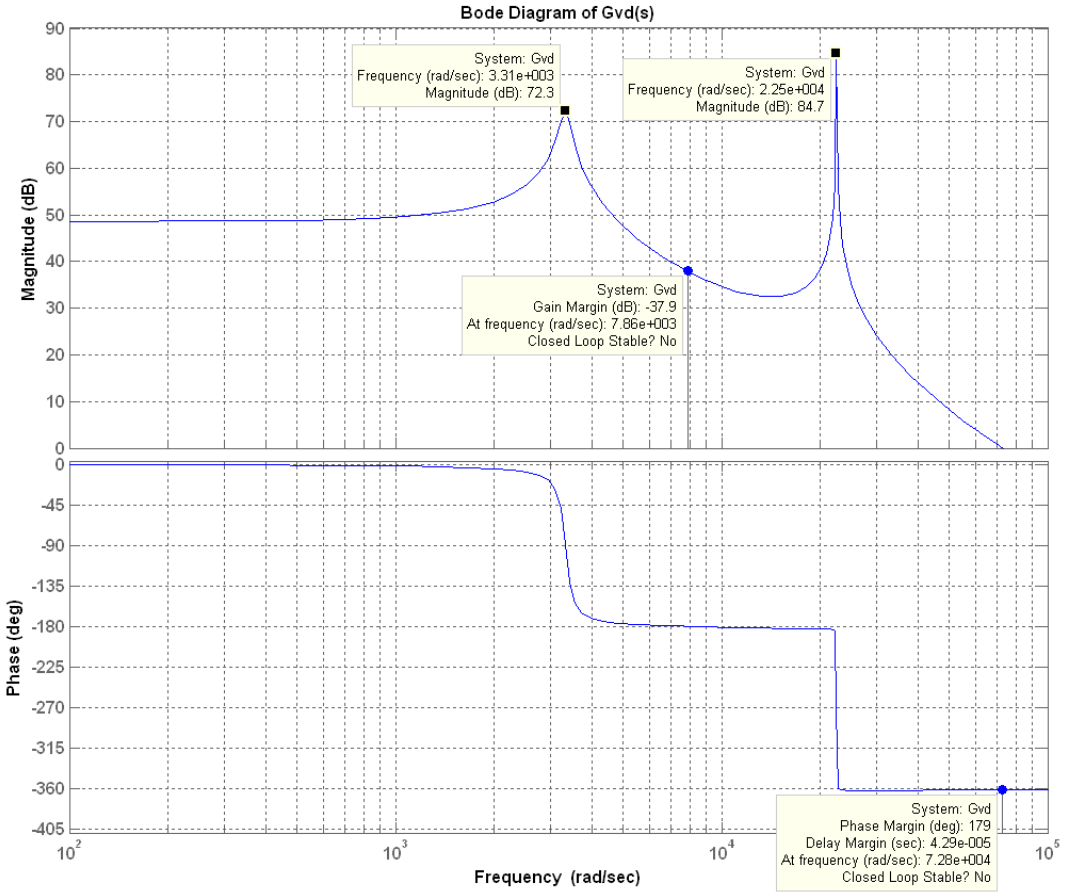

Fig.3.27 Bode plot of duty factor-to-output voltage transfer function, $G_{vd}(s)$, in CCM operation

To determine the open-loop transfer function, $G_{OPEN-CCM}(s)$, the gain and the phase margins, the transfer function $G_{vd}(s)$, of (3.9), is used. As the V_{REF} voltage is chosen as $1V$ and the desired output voltage is $60V$, the feedback gain of the output

voltage, K_{FB}, is $\frac{1}{60}$. Furthermore, the resistors and capacitors in error amplifier circuit, shown in Fig.2.29, are taken as those listed in Table3.5 to place the controller's zero and poles at desired frequencies.

Table3.5 Error amplifier resistors and capacitor values

R_1	59	$k\Omega$
R_2	1000	Ω
R_3	5110	Ω
C_1	1000	nF
C_2	500	nF

The controller, which is used for the generation of duty-factor drive signals, internally compares the error amplifier output with a triangular waveform which has a peak-to-peak value of $3.6V$. Thus, from (2.150), duty-factor transfer function, $K_{PWM}(s)$, is $\frac{1}{3.8}$. When the values of $G_{vd}(s)$, K_{FB}, $K_{PWM}(s)$ and the resistors and capacitors given in Table3.5 are substituted in (2.151) then the open-loop transfer function for CCM operation, $G_{OPEN-CCM}(s)$, is acquired as;

$$T_{CCM}(s) = 9.077 \cdot 10^{-7} \frac{(s+195.7)}{s \cdot (s+391)} \cdot G_{vd}(s) \qquad (3.21)$$

The bode plot of open-loop transfer function for CCM operation, $G_{OPEN-CCM}(s)$, shown in Fig.3.28, is obtained in the simulations carried out using MATLAB to determine the phase and gain margins. As it can be seen from Fig.3.28, the phase margin of $G_{OPEN-CCM}(s)$ is $92.7°$ and the gain margin is 14.4dB. Thus, the closed

loop system for CCM operation is stable and the phase and gain margins meet the conditions of a good controller which are mentioned before.

The cut-off frequency of the converter is at $14.2 rad/\sec$ as shown in Fig.3.28. This frequency is very low for a dc/dc converter open-loop transfer function because, the response of the controller against the load and input voltage variations becomes slower when the cut-off frequency decreases. This situation can lead to undesirable overshoots or undershoots of the output voltage, V_O, at load and input voltage, V_S, transients. In Z-source dc/dc converter, to achieve the desired gain margin, the controller gain is decreased drastically which leads to very low cut-off frequency.

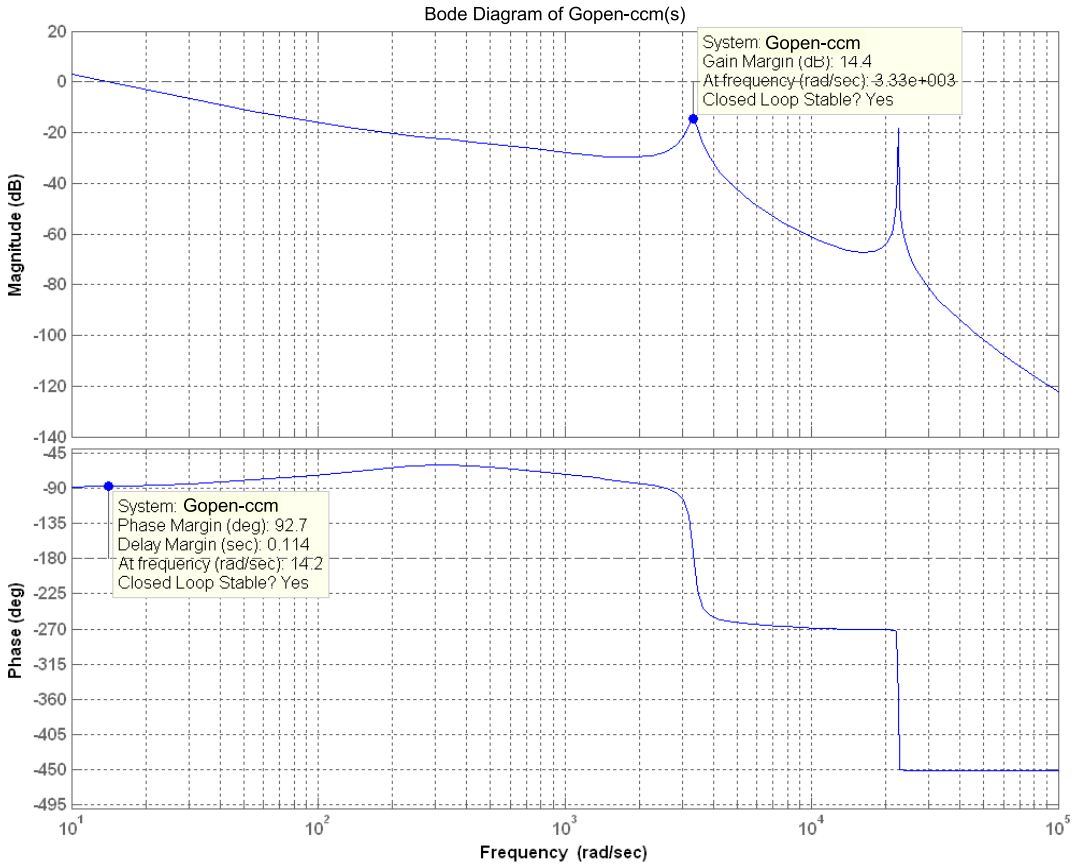

Fig.3.28 Bode plot of open loop transfer function, $G_{OPEN-CCM}(s)$, for CCM operation

Design of a controller for a dc/dc converter entails that the controller is stable for all type of load (no load-to-full load) and input voltage. Thus, the controller, designed for CCM operation, must also be stable in DCM operation.

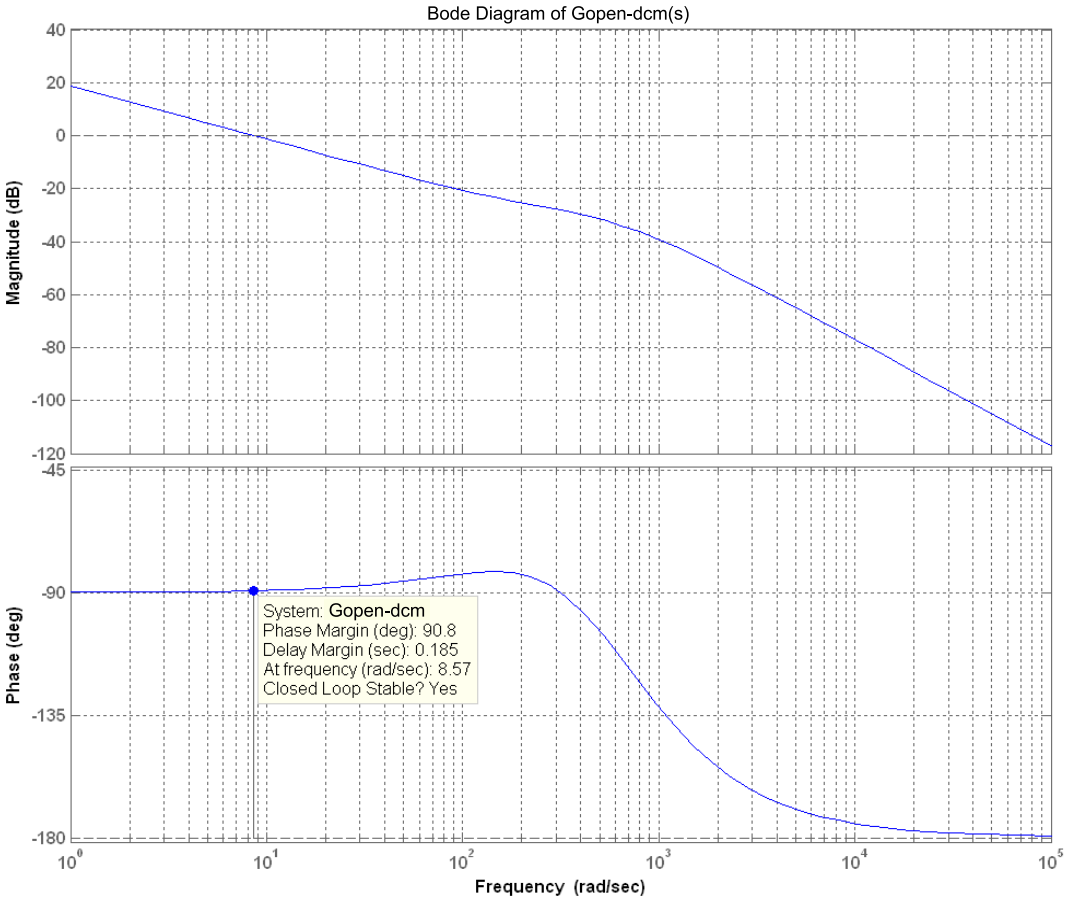

Fig.3.29 Bode plot of open-loop transfer function, $G_{OPEN-DCM}(s)$, for DCM operation

As the controller, designed for CCM operation, is used in DCM operation, the feedback gains, K_{FB}, of the output voltage and $K_{PWM}(s)$, of the PWM transfer function do not change. The only difference between the open loop transfer functions, $G_{OPEN-CCM}(s)$, in CCM operation and $G_{OPEN-DCM}(s)$ in DCM operation, is duty factor-to-output voltage transfer functions. Thus, the duty factor-to-output voltage

transfer function $G_{vd-dcm}(s)$, determined in (3.19), is used to obtain the open-loop transfer function, $G_{OPEN-DCM}(s)$, of DCM operation. As a result, the $G_{OPEN-DCM}(s)$ is,

$$G_{OPEN-DCM}(s) = 9.077 \cdot 10^{-7} \frac{(s+195.7)}{s \cdot (s+391)} \cdot G_{vd\_dcm}(s) \tag{3.22}$$

The bode plot diagram of the transfer function $G_{OPEN-DCM}(s)$, shown in Fig.3.29, is obtained by using MATLAB to determine the phase and gain margins.

The phase margin of $G_{OPEN-DCM}(s)$ is $90.8°$ which is greater than $45°$. As the duty factor-to-output voltage transfer function, $G_{OPEN-DCM}(s)$ has only one pole, it is a first order system. Thus, the gain margin is not valid because the transfer function phase never falls below $180°$. Thus the controller, designed for CCM operation, is also stable for DCM operation as shown in Fig.3.29.

3.6 Conclusion of Chapter

In the first part of the chapter, the required circuit parameters are determined according to the requirements of the Z-source dc/dc converter based on the representation of the system developed in Chapter 2. Then, the power stage of simplified Z-source dc/dc converter is simulated to indicate the compliance between the theoretical results and simulation results for both CCM and DCM operations. Also, the transfer functions obtained in Chapter 2 are simulated here, thus accuracy of the transfer functions are supported via simulations. In the third part, the Z-source full bridge dc/dc converter power stage simulations are run for both CCM and DCM operations to demonstrate the analogy between the simplified Z-source dc/dc converter and Z-source full bridge dc/dc converter. In the last part, design of a voltage controller is investigated for both CCM and DCM operations. The gain and phase margins and bode plots of the open-loop transfer function are determined to investigate the stability of controller and converter.

CHAPTER 4

EXPERIMENTAL RESULTS OF Z-SOURCE FULL BRIDGE DC/DC CONVERTER

4.1 Introduction

In the previous chapters, a model for a Z-source dc/dc converter has been developed and its validity has been shown by conducting several simulations. In this chapter, the experimental results obtained from its laboratory prototype are investigated and compared with simulation results. These studies involve performance of the controller together with the converter too. The efficiency of the prototype circuit is compared with that determined theoretically. Schematics and layouts of the implemented prototype circuit are given in Appendixes A and B. Also, the top and bottom photographs of the prototype circuit are displayed in Appendix C.

4.2 Experimental Results in CCM Operation of Z-source Full Bridge DC/DC Converter

The prototype Z-source dc/dc converter in open-loop CCM operation has been implemented with the following parameters and specifications; the input voltage is set to $30V$ and the PWM is given by a function generator whose duty factor and frequency are set to 0.34 and $100kHz$, respectively. A dc electronic load (Agilent-N3300A) is used to sink current from the converter. The sink current is adjusted such a value that the output is seen as a 10Ω resistor by the converter.

Following currents in the converter; the input diode current, $i_{D_1}(t)$, Z-source inductor current, $i_{L_z}(t)$, output inductor current, $i_{L_O}(t)$, are monitored against PWM signal on

the oscilloscope (Agilent-DSO6054A) screen. Results are shown in Fig.4.1 and Fig.4.2. All current waveforms are measured via current probe (Tetronix-TCP312) whose amplifier output (Tetronix-TCPA300) is adjusted to $10A/V$ which means that $1V$ measurement in oscilloscope screen corresponds to $10A$ for current measurements.

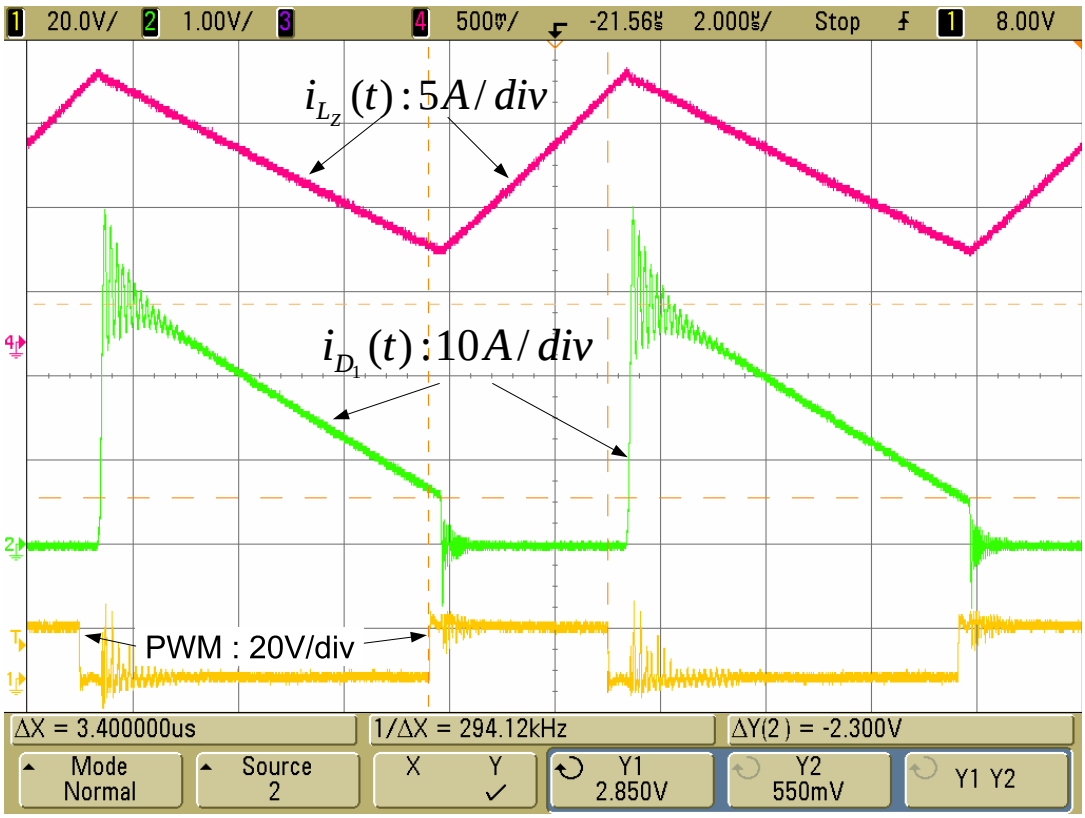

Fig.4.1 Waveforms obtained from prototype of Z-source full bridge dc/dc converter in CCM operation: Z-source inductor current, $i_{L_z}(t)$ (pink-source4), input diode (D_1) current, $i_{D_1}(t)$ (green-source2), PWM drive signal (yellow-source1)

Fig.4.1 shows the Z-source inductor current, $i_{L_z}(t)$, input diode (D1) current, $i_{D_1}(t)$ and PWM. As it can be observed from the figure, by the PWM being low, input diode is forward biased and input current pass through it. When the PWM becomes high,

the diode is reversed biased and the diode current goes to zero and stays there until the PWM output is being high. The peak value of the diode current is $28.5A$ and it falls linearly to $5.5A$ at implemented circuit. In Z-source full bridge dc/dc converter simulation, referring Fig.3.22, the peak value of the diode current, $i_{D_1}(t)$, is about $28A$ and it falls down to $5A$ level linearly. Besides, in Fig.4.1, the Z-source inductor current, $i_{L_Z}(t)$, increases linearly to $16A$ while the PWM is high, and it decreases linearly to $5.6A$ when the PWM is low. The peak-to-peak value of the Z-source inductor current variation is $10.4A$. The simulation results shown in Fig.3.22, indicates that the peak and valley levels for the Z-source inductor current are $15.75A$ and $6.25A$, respectively. Thus, the peak-to-peak value of it is $9.5A$. As a result, the input diode current, $i_{D_1}(t)$, and Z-source inductor current, $i_{L_Z}(t)$, waveforms obtained in the implemented circuit and for the simulated one are quite close to each other.

Fig.4.2 shows waveforms for the Z-source inductor current, $i_{L_Z}(t)$, the output inductor current, $i_{L_O}(t)$, and PWM. The Z-source inductor current and PWM is the same as in Fig.4.1. As it can be observed from Fig.4.2, the synchronization of the output inductor current, $i_{L_O}(t)$, with the Z-source inductor current, $i_{L_Z}(t)$, and PWM output is the same as in the theoretical and simulation waveforms. The Z-source inductor current and the output inductor current vary linearly in both states of the PWM (low and high). In the implemented prototype circuit, the peak value of the output inductor current is $7.6A$ and the valley value of the output inductor current is $3.10A$. In the simulation results for CCM operation, given in Chapter 3, the peak and valley values of the inductor were $7.5A$ and $3.75A$, respectively.

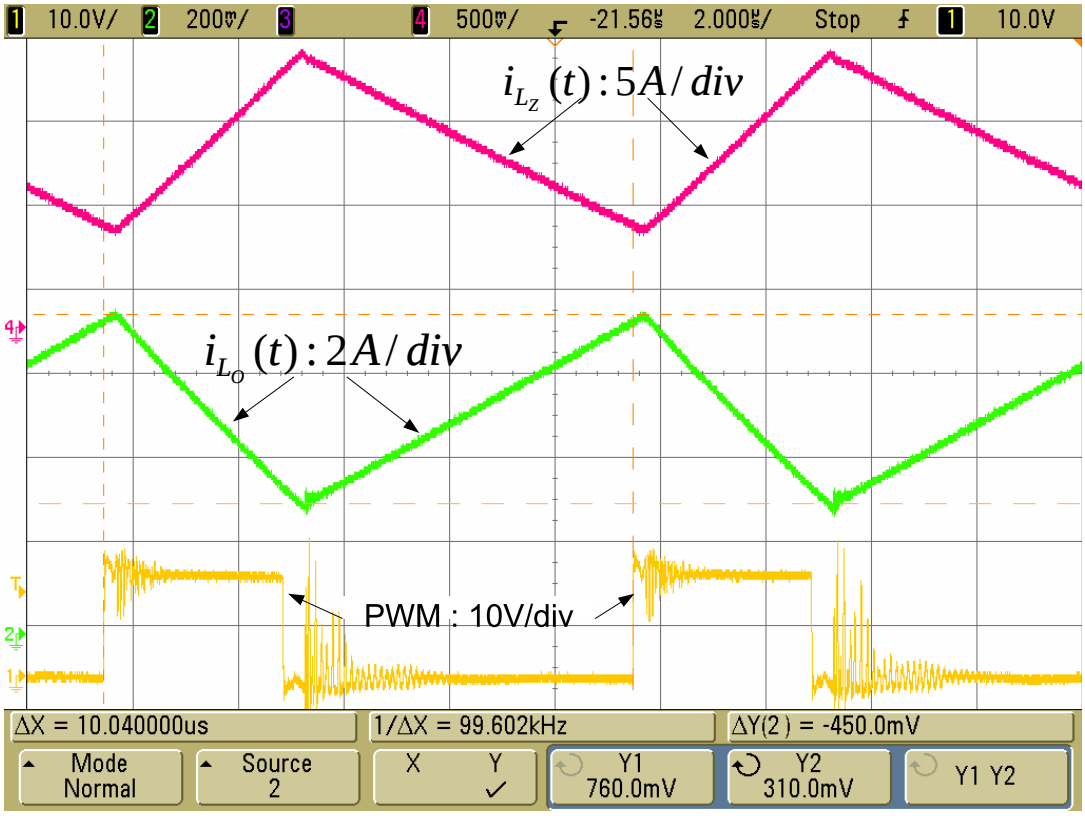

Fig.4.2 Waveforms obtained from prototype of Z-source full bridge dc/dc converter in CCM operation: Z-source inductor current, $i_{L_Z}(t)$ (pink-source4), output inductor current, $i_{L_O}(t)$ (green-source2), PWM drive signal (yellow-source1)

Although forward voltage drop on diodes and transformer equivalent circuit are taken account in computations made for simulations, switching and conduction losses on MOSFETs, ESR (equivalently series resistance) for the Z-source capacitors and the output capacitor and AC and DC losses in inductors are not in the simulation. These additional power losses in the prototype converter lead to slight discrepancies to be taken accounted in the waveforms related to inductors and input diode current. Furthermore, these additional power losses on inductors and capacitors prevent the input power transfer to the load. Thus, output voltage is decreased to $53V$; on the contrary, it is $56.1V$ at simulation results. After all, in general waveforms obtained experimentally are in a good agreement with those expected theoretically and simulations for the CCM operation in open loop.

4.3 Experimental Results in DCM Operation of Z-source Full Bridge DC/DC Converter

In order to compare behavior of the real converter with the simulated one, the prototype is run in open loop for DCM operation. The input voltage is set to $45V$ and the PWM drive signal is given via a function generator. The frequency and duty factor of the PWM signal is set to $100kHz$ and 0.17, respectively, as done in full bridge dc/dc converter simulation. The converter is loaded via a dc electronic load which draws $2.8A$. At this load current, the output voltage, V_O, is $56V$, thus, 20Ω resistor is seen at the output of the converter as in the simulation.

Waveforms regarding to the input diode current, $i_{D_1}(t)$, Z-source inductor current, $i_{L_z}(t)$, output inductor current, $i_{L_o}(t)$, and PWM are recorded by oscilloscope (Agilent-DSO6054A). They are shown in Fig.4.3 and Fig.4.4. Note once again that, all current waveforms are measured via current probe (Tetronix-TCP312) whose amplifier output (Tetronix-TCPA300) is adjusted to $10A/V$.

Fig.4.3 shows waveforms for the Z-source inductor current, $i_{L_z}(t)$, the input diode current, $i_{D_1}(t)$, and the PWM drive signal. As it is seen in Fig.4.3, the input diode, D_1, becomes forward biased to carry the input current, $i_{D_1}(t)$, when the PWM drive signal is low. The diode current, $i_{D_1}(t)$, decays linearly from $12.25A$ to zero and remains there until the beginning of the next PWM drive signal low state. The Z-source full bridge dc/dc converter simulation showed that the diode current, $i_{D_1}(t)$ stepped to $12A$ at the instant of PWM made low and fell linearly to zero as can be seen in Fig.3.25. Besides, in Fig.4.3, the Z-source inductor current, $i_{L_z}(t)$, increases linearly from $1.7A$ to $7.0A$ when the PWM drive is high and it decreases linearly when the PWM drive is made low. This linear decline of the Z-source inductor current continues until the input diode current, $i_{D_1}(t)$, reaches down to zero. Then, Z-source inductor current remains at $1.7A$ at the end of the period. In simulation results of the Z-source full bridge dc/dc converter in DCM operation seen in Fig.3.25, the peak and valley values of $i_{L_z}(t)$ are $1.85A$ and $6.8A$, respectively.

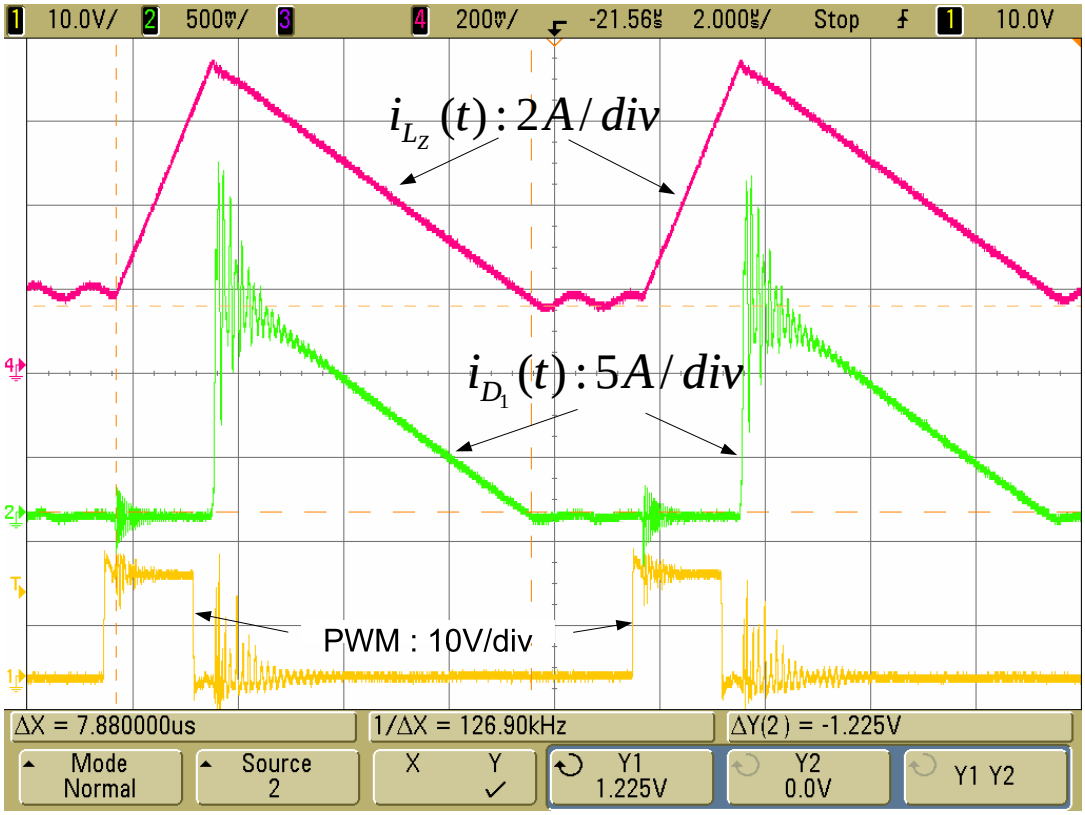

Fig.4.3 Waveforms obtained from the prototype of Z-source full bridge dc/dc converter in DCM operation: Z-source inductor current, $i_{L_Z}(t)$ (pink-source4), input diode (D_1) current, $i_{D_1}(t)$ (green-source2), PWM drive signal (yellow-source1)

Waveforms recorded experimentally for the input diode current, $i_{D_1}(t)$ and the Z-source inductor current, $i_{L_Z}(t)$ are exactly same in the shape with those obtained in simulations. In addition, the peak and valley values on the waveforms obtained in both cases are nearly same.

In Fig.4.4 shows the waveforms obtained experimentally for the Z-source inductor current, $i_{L_Z}(t)$, the output inductor current, $i_{L_O}(t)$, and the PWM drive signal. The Z-source inductor current waveforms, shown in Fig.4.3 and Fig.4.4, are same with each other. While PWM drive signal is low, the output inductor current, $i_{L_O}(t)$,

increases linearly up to $3.75A$ meanwhile $i_{L_z}(t)$ decreases as seen in Fig.4.4. Both remain at their last current levels until the PWM drive signal becomes high again. By the PWM being high, $i_{L_o}(t)$ decreases linearly and relatively fast to $1.5A$ while $i_{L_z}(t)$ increases linearly and relatively fast as well. Referring to Fig.3.26, showing results obtained in the simulation of full bridge dc/dc converter, the output inductor current's peak and valley values were $3.7A$ and $1.75A$, respectively.

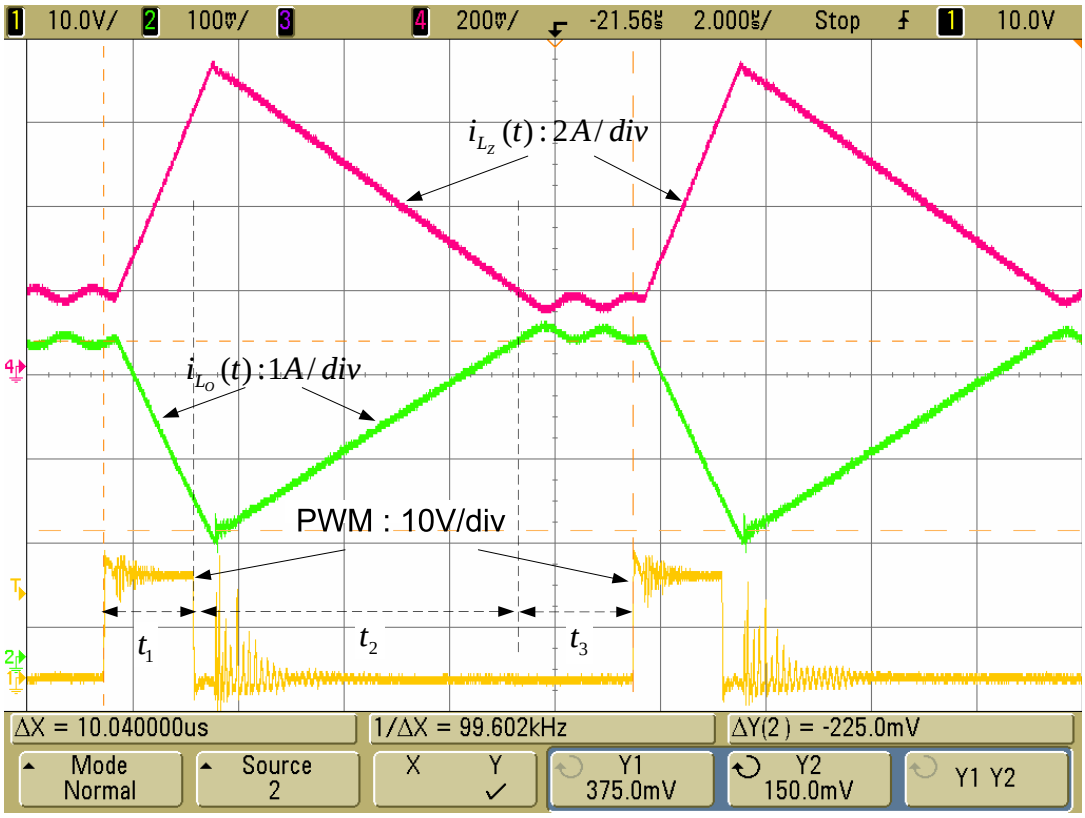

Fig.4.4 Waveforms obtained from the prototype of Z-source full bridge dc/dc converter in DCM operation: Z-source inductor current, $i_{L_z}(t)$ (pink-source4), output inductor current, $i_{L_o}(t)$ (green-source2), PWM drive signal (yellow-source1)

Relatively small discrepancies between results obtained in the simulations and the experiments are due to the presence of switching and conduction losses of MOSFETs, ESR (equivalently series resistance) of the Z-source capacitors and the output capacitor and AC and DC losses in inductors. When the Z-source and the output inductors stay constant at time interval t_3, the currents in the $i_{L_o}(t_3)$ becomes about twice of the $i_{L_z}(t_3)$ in magnitude as calculated theoretically and determined in simulations. To conclude, the experimental results, obtained in DCM operation of the prototype, supports the theoretical expectations and simulation results achieved preliminary.

4.4 Controller Performance of Z-source Full Bridge DC/DC Converter

The controller, whose design in Chapter 3.5, is implemented to control the prototype circuit. The controller makes use the resistors and capacitors given in Table3.5, as its parameters.

The performance of the controller is tested by trying to control the output voltage of the converter under transient conditions due to step disturbances imposed on the input voltage magnitude and output loading. Thus, both the peak value and settling time for the output voltage are recorded during the transient period. Recalling that for CCM operation, the circuit was run at $360\,W$ output power (full load power) and $30V$ input voltage. Similarly, for DCM operation, the output power was set to $180W$ (half of the full load power) and the input voltage was set as $45V$. Remembering that, the no-load condition for the system is also important as much as the loaded conditions, the input transients are applied to the closed-loop controlled converter as step rise from $30V - to - 45V$ and $45V - to - 30V$ under no-load, half and full load conditions. Furthermore, transients due to step loading at the output are applied as step loading from no load-to-half load, from half load-to-full load, from full load-to-half load and from half load-to-no load for the input voltage set to $30V$ once and $45V$ secondly. More severe transient conditions against step loading from no-load-to-full load and full load-to-no load conditions are investigated for the input voltage is set to $30V$ once and $45V$ secondly. Table4.1 summarizes the applied transient

conditions and the related experimental output voltage transient responses. The time interval on the figures, Δt, shows the time between the instant where the output voltage response starts against the transient and enters a voltage zone (between $59V$ and $61V$).

Table4.1 Applied input voltage and output power transient conditions

Fixed Condition	**Applied Transient**	**Related Figure**
Input voltage, $V_S = 30V$	No Load-to-Half Load	Fig.4.5
	Half Load-to-Full Load	Fig.4.6
	Full Load-to-Half Load	Fig.4.7
	Half Load-to-No Load	Fig.4.8
	No Load-to-Full Load	Fig.4.9
	Full Load-to-No Load	Fig.4.10
Input voltage, $V_S = 45V$	No Load-to-Half Load	Fig.4.11
	Half Load-to-Full Load	Fig.4.12
	Full Load-to-Half Load	Fig.4.13
	Half Load-to-No Load	Fig.4.14
	No Load-to-Full Load	Fig.4.15
	Full Load-to-No Load	Fig.4.16
No Load Power	Input voltage, $V_S : 30V - to - 45V$	Fig.4.17
	Input voltage, $V_S : 45V - to - 30V$	Fig.4.18
Half Load Power ($180W$)	Input voltage, $V_S : 30V - to - 45V$	Fig.4.19
	Input voltage, $V_S : 45V - to - 30V$	Fig.4.20
Full Load Power ($360W$)	Input voltage, $V_S : 30V - to - 45V$	Fig.4.21
	Input voltage, $V_S : 45V - to - 30V$	Fig.4.22

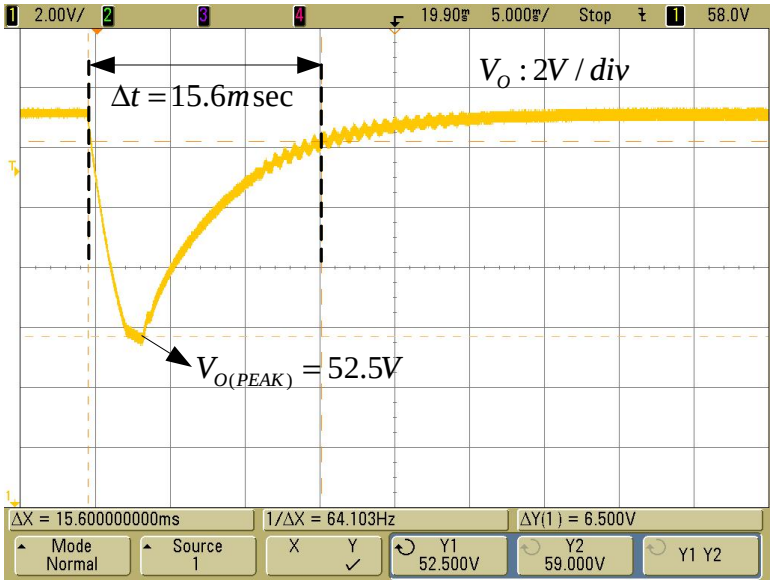

Fig.4.5 The output voltage transient response to step loading disturbance from no-load-to-half load for a constant input voltage magnitude $V_S = 30V$

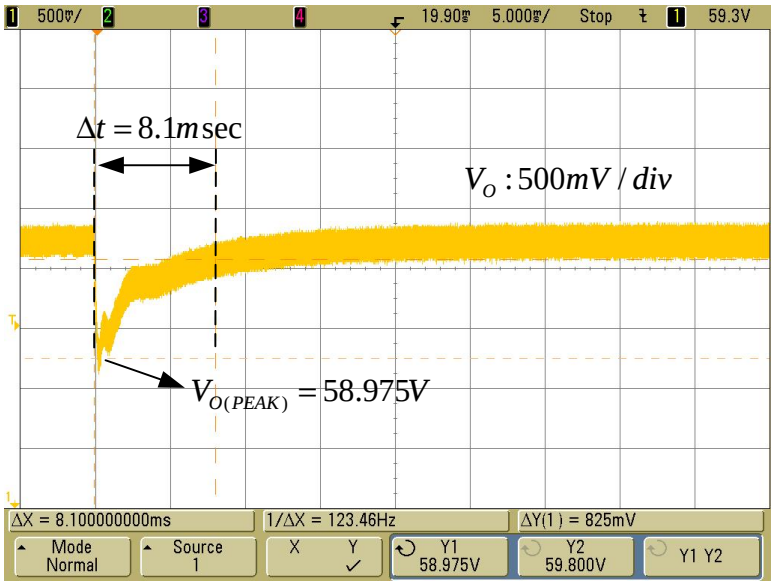

Fig.4.6 The output voltage transient response to step loading disturbance from half load-to-full load for a constant input voltage magnitude $V_S = 30V$

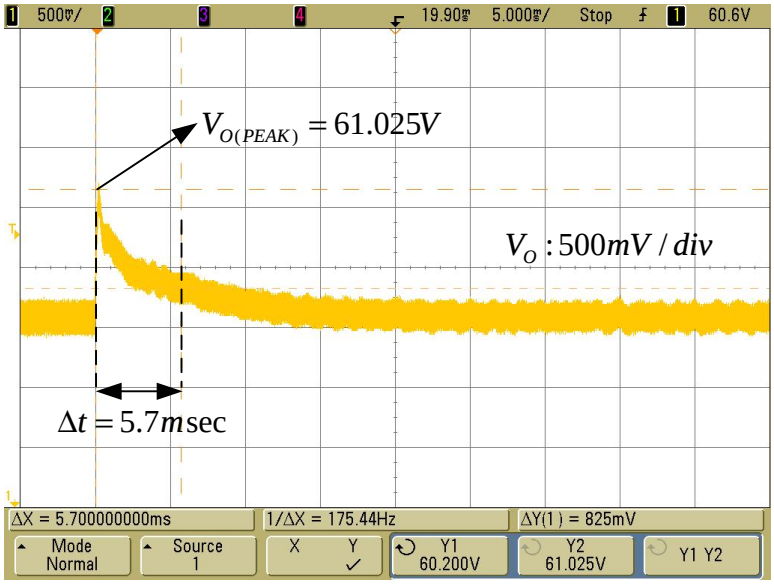

Fig.4.7 The output voltage transient response to step loading disturbance from full load-to-half load for a constant input voltage magnitude $V_S = 30V$

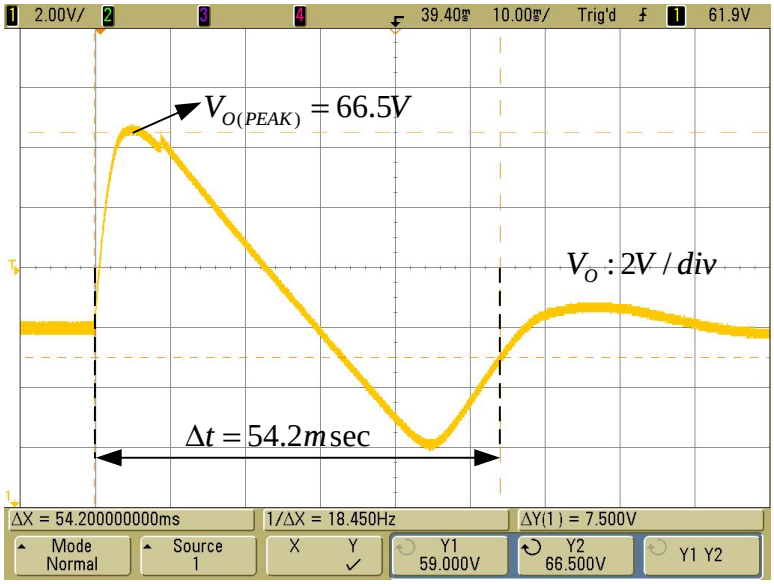

Fig.4.8 The output voltage transient response to step loading disturbance from half load-to-no load for a constant input voltage magnitude $V_S = 30V$

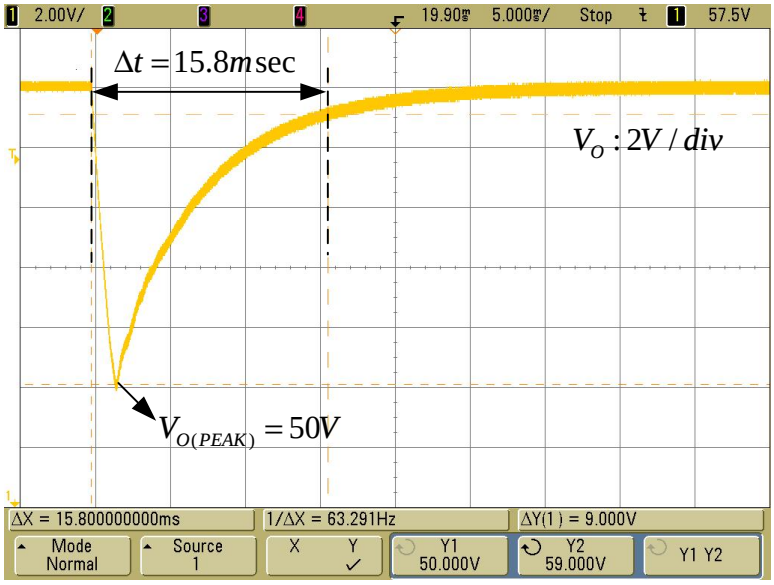

Fig.4.9 The output voltage transient response to step loading disturbance from no load-to-full load for a constant input voltage magnitude $V_S = 30V$

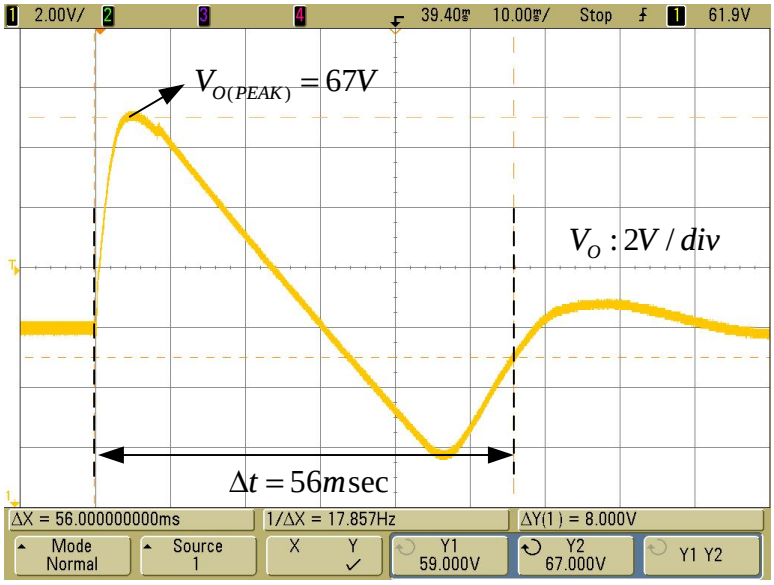

Fig.4.10 The output voltage transient response to step loading disturbance from full load-to-no load for a constant input voltage magnitude $V_S = 30V$

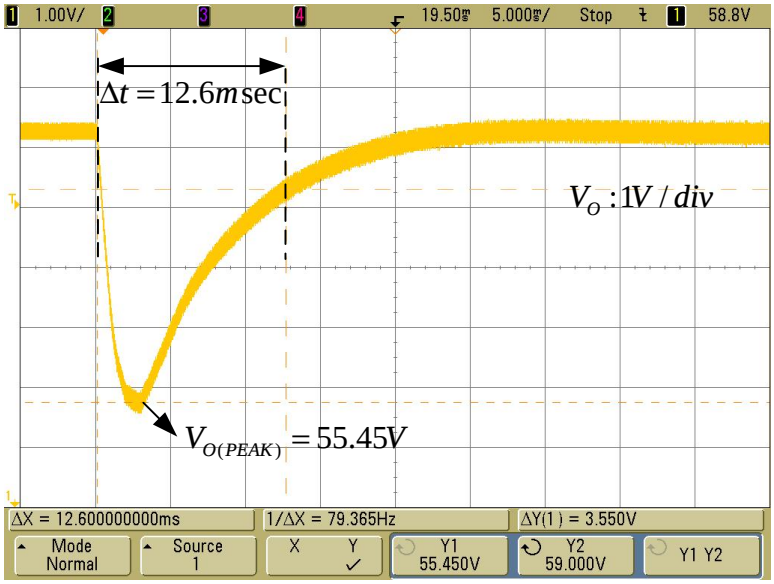

Fig.4.11 The output voltage transient response to step loading disturbance from no load-to-half load for a constant input voltage magnitude $V_S = 30V$

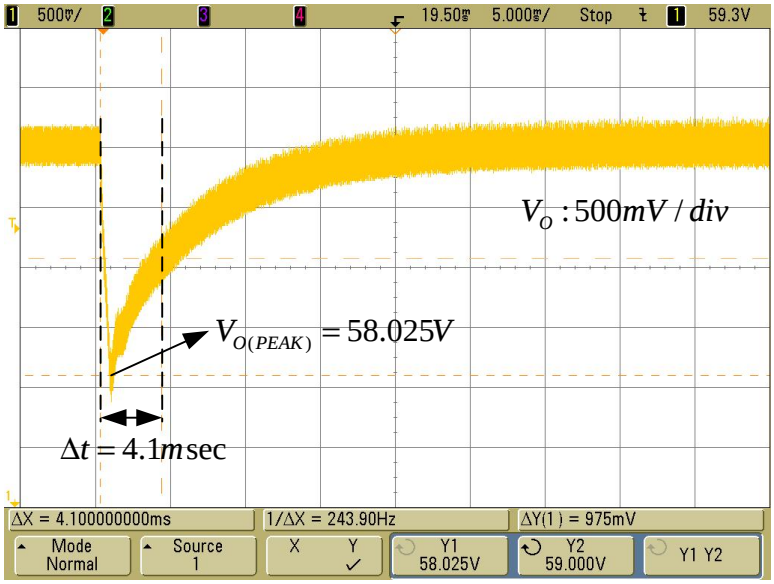

Fig.4.12 The output voltage transient response to step loading disturbance from half load-to-full load for a constant input voltage magnitude $V_S = 45V$

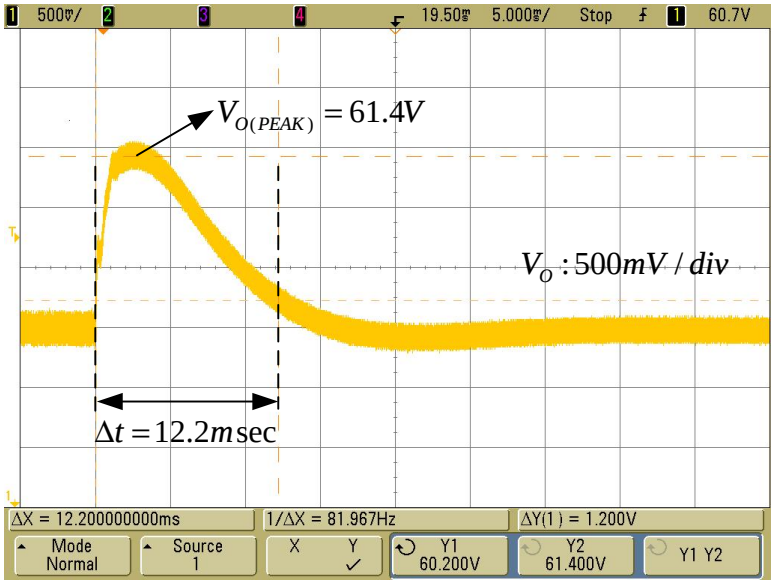

Fig.4.13 The output voltage transient response to step loading disturbance from full load-to-half load for a constant input voltage magnitude $V_S = 45V$

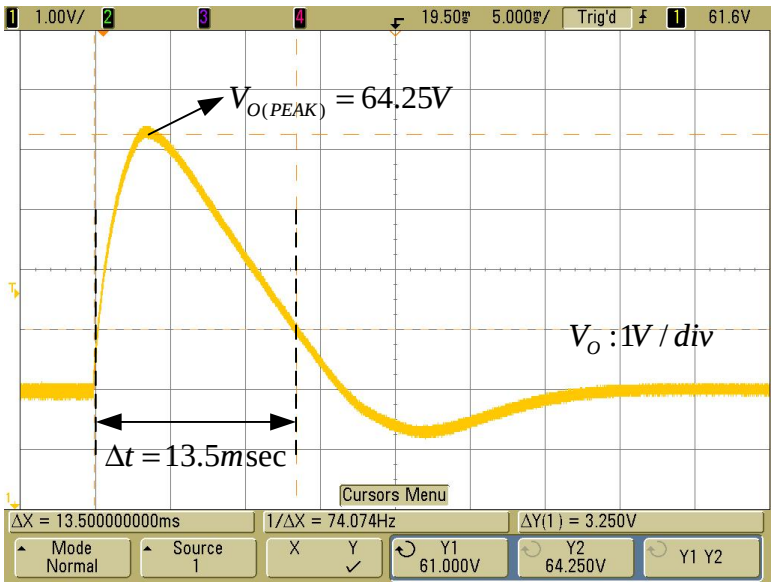

Fig.4.14 The output voltage transient response to step loading disturbance from half load-to-no load for a constant input voltage magnitude $V_S = 45V$

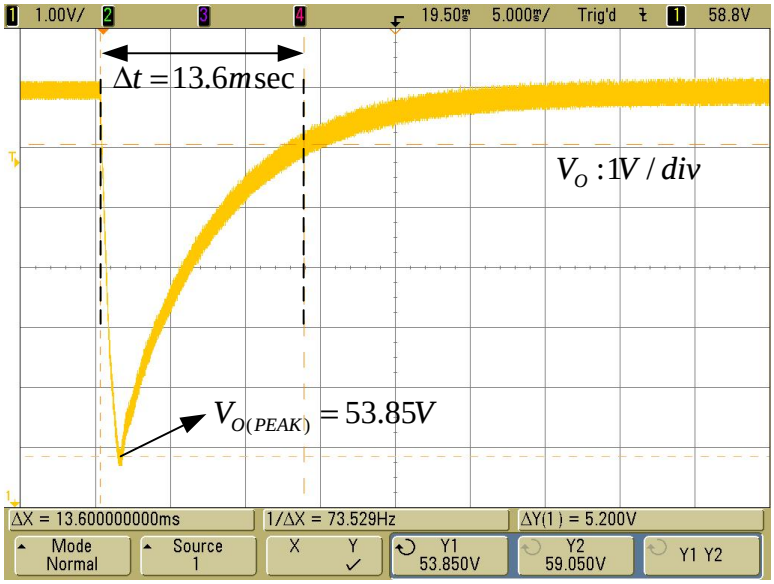

Fig.4.15 The output voltage transient response to step loading disturbance from no load-to-full load for a constant input voltage magnitude $V_S = 45V$

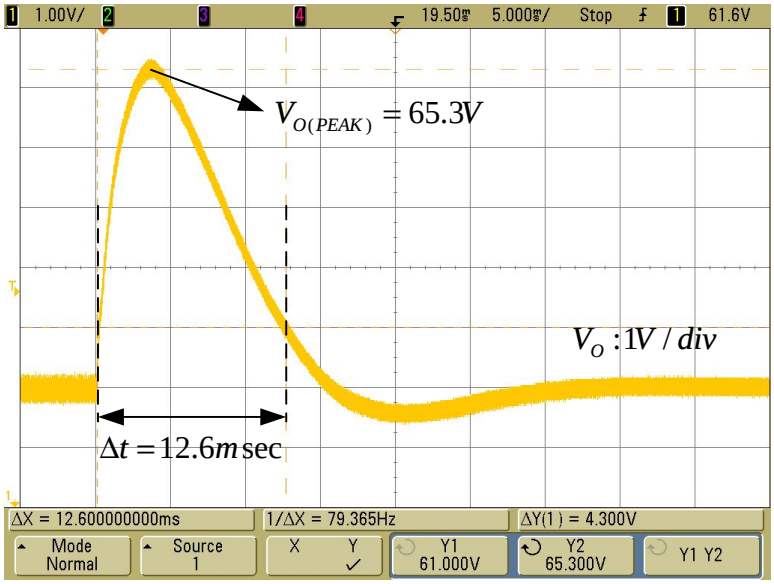

Fig.4.16 The output voltage transient response to step loading disturbance from full load-to-no load for a constant input voltage magnitude $V_S = 45V$

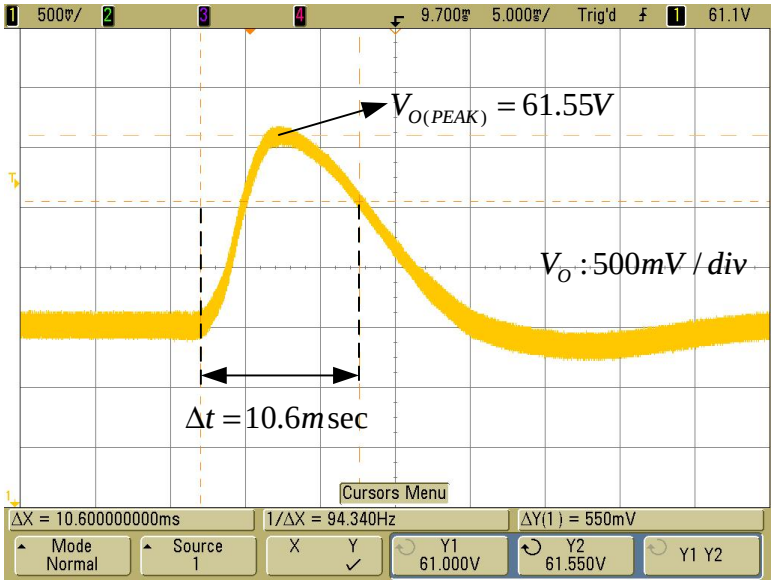

Fig.4.17 The output voltage transient response to input voltage, V_S , step change from $30V - to - 45V$ at no load condition

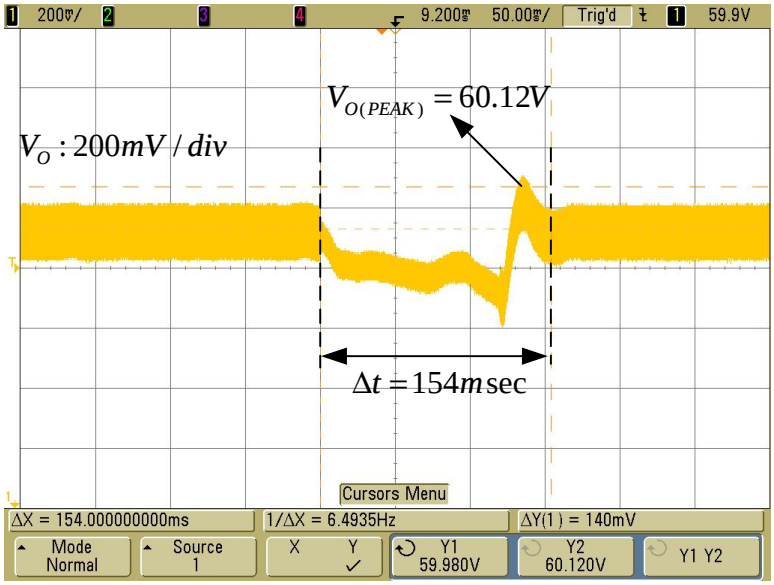

Fig.4.18 The output voltage transient response to input voltage, V_S , step change from $45V - to - 30V$ at no load condition

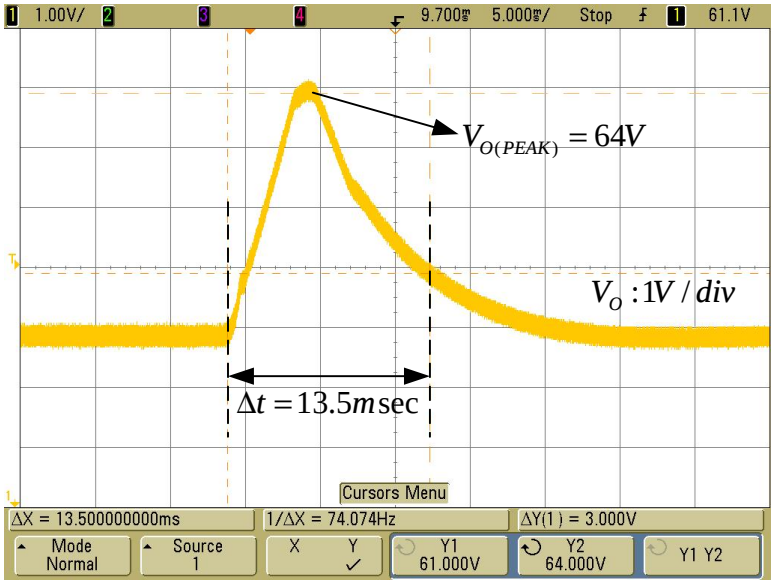

Fig.4.19 The output voltage transient response to input voltage, V_S , step change from $30V - to - 45V$ at half load condition

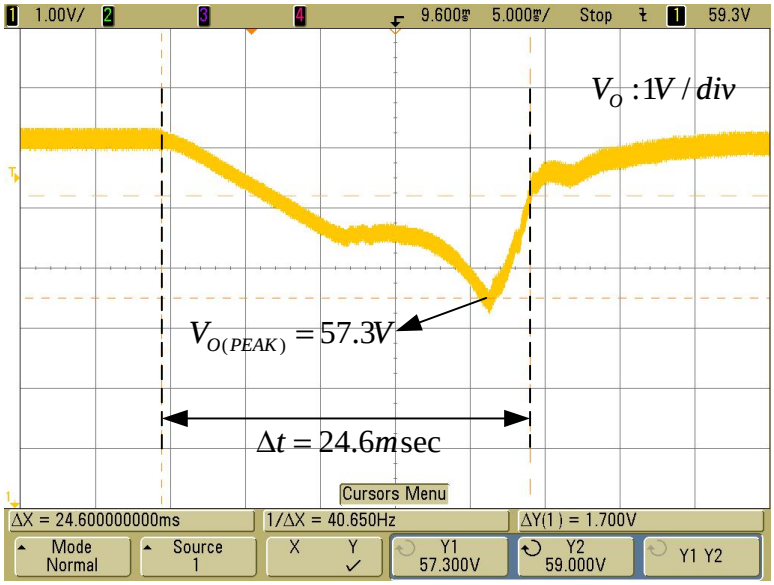

Fig.4.20 The output voltage transient response to input voltage, V_S , step change from $45V - to - 30V$ at half load condition

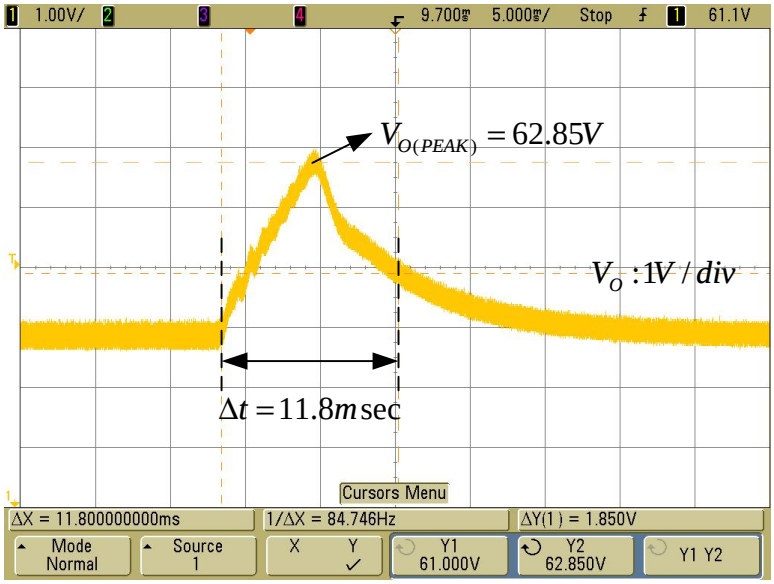

Fig.4.21 The output voltage transient response to input voltage, V_S , step change from $30V - to - 45V$ at full load condition

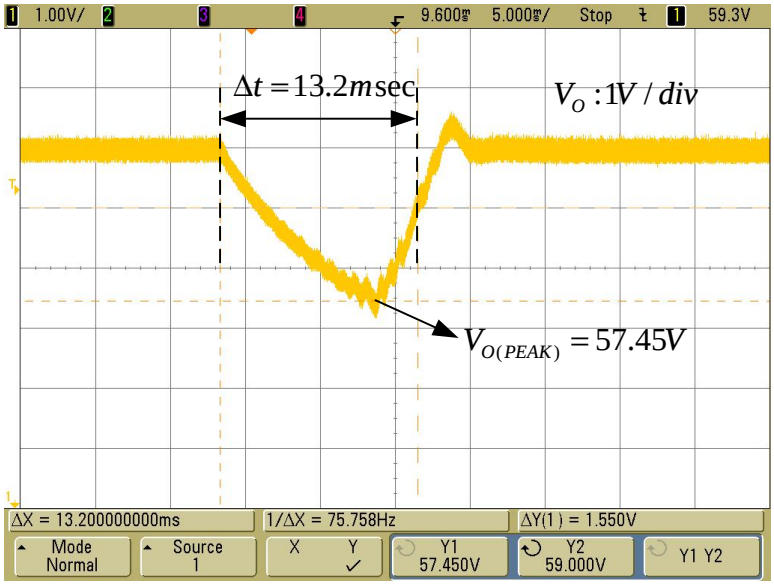

Fig.4.22 The output voltage transient response to input voltage, V_S , step change from $45V - to - 30V$ at full load condition

As it can be concluded from the figures above, the worst case conditions are no load-to-full-load and full load-to-no load transients when input voltage, V_S, is $30V$. The peak value of output voltage is $50V$ at no load-to-full load transient and $67V$ at full load-to-no load transient. At other input and output transients, the output voltage is in the range of $54V - 66V$, which corresponds to $\%10$ overshoot.

In linear systems, it is expected that the responses against the same amount of up and down step disturbances are symmetric according to time axis. In other words, the magnitudes of overshoot and settling time are same for both responses against the up and down step disturbances. However as the dc/dc converters are nonlinear systems the responses against the load and input disturbances are not symmetric. For example, In Fig.4.19 and Fig.4.20, the output voltage transient responses to input voltage, V_S, step change from $30V - to - 45V$ and $45V - to - 30V$ at half load condition are displayed respectively. Although the magnitude of the applied input voltage disturbances are same, $15V$, the responses of the output voltage is not symmetric against these step input voltage disturbances. The reason of these different responses is the nonlinearity of the Z-source full bridge dc/dc converter.

4.5 Efficiency Calculation of Z-source Full Bridge DC/DC Converter

As in the other switching supplies, efficiency is a significant aspect that must be considered for the Z-source dc/dc converter, too. Thus, determination of the sources of power losses at dc/dc converter is inevitable. In this section, the power loss on each component is calculated analytically for the Z-source full bridge dc/dc converter in CCM operation. To compare analytical calculations with the experimental results, the operating point of the converter is chosen same as in Section 4.2.

The sources of the power losses in Z-source dc/dc converter include conduction and switching losses on MOSFETs and diodes, switching and DC losses in magnetic components (inductors and transformer) and ESR losses in capacitors. Calculation of these power losses requires determination of the current waveforms in each component. In Section 4.2, the current waveforms in the input diode, D_1, the Z-

source inductor, L_Z, and the output inductor, L_O are recorded, and current magnitudes are determined . The current waveforms in other components can be determined from them.

By using Kirchhoff's current law at NODE I in Fig.4.23, the Z-source capacitors current, $i_{C_Z}(t)$, can be derived by subtracting the Z-source inductor current, $i_{L_Z}(t)$ from the input diode current, $i_{D_1}(t)$ as in (4.1). Again by using Kirchhoff's law at NODE II, the current entering into the full-bridge (Q_1, Q_2, Q_3 and Q_4), $i_Q(t)$, can be found by subtracting the Z-source capacitor current, $i_{C_Z}(t)$, from the Z-source inductor current, $i_{L_Z}(t)$, as in (4.2).

$$i_{C_Z}(t) = i_{D_1}(t) - i_{L_Z}(t) \tag{4.1}$$

$$i_Q(t) = i_{L_Z}(t) - i_{C_Z}(t) = 2 \cdot i_{L_Z}(t) - i_{D_1}(t) \tag{4.2}$$

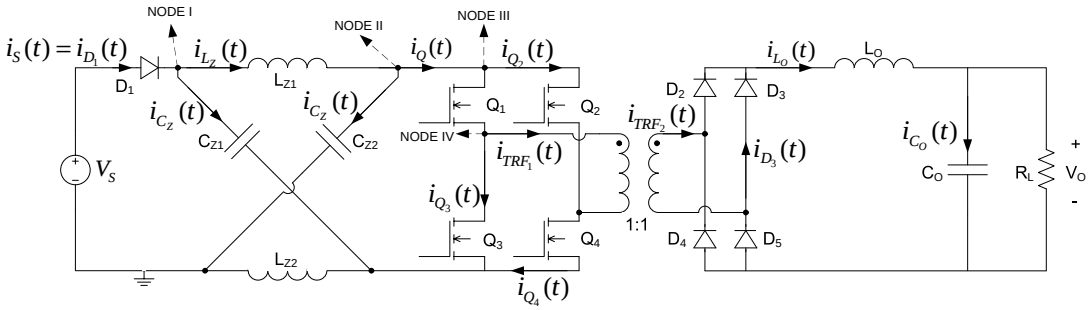

Fig.4.23 Current representation of Z-source full bridge dc/dc converter

The output inductor current, $i_{L_O}(t)$, is the rectified form of the secondary current, $i_{TRF_2}(t)$, of the transformer over a period. Assuming that, the primary and secondary currents of this transformer with turn ratio of 1:1 are equal to each other. Since the

output ripple current of the converter is very small, all ripple current of the output inductor flows through the output capacitor. Then, the output capacitor current, $i_{C_O}(t)$, is equal to the ripple current of output inductor. Waveforms for currents in several elements of the converter running in open loop shown in Fig.4.24 for sequential two periods. Similar waveforms in other elements of the converter are shown in Fig.4.25 as a continuation.

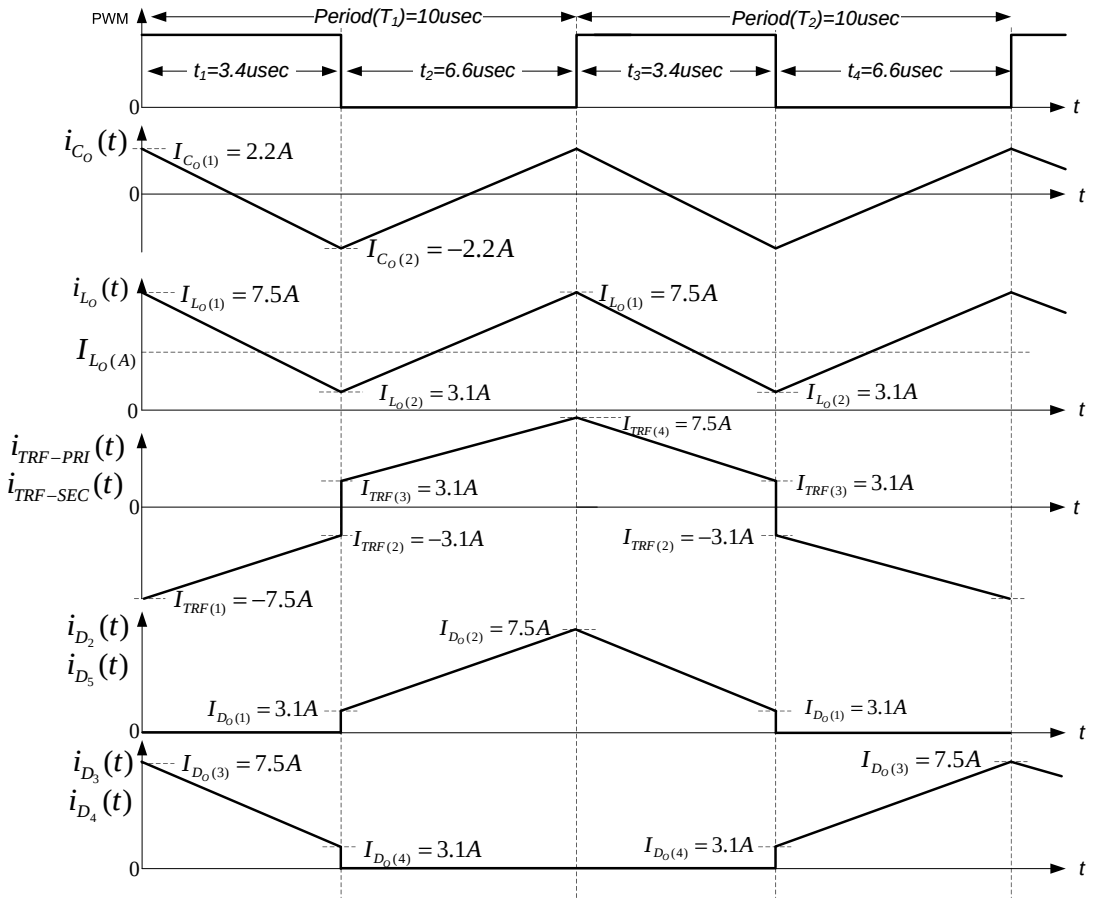

Fig.4.24 Current waveforms for several components of open-loop drive of Z-source full bridge dc/dc converter-1

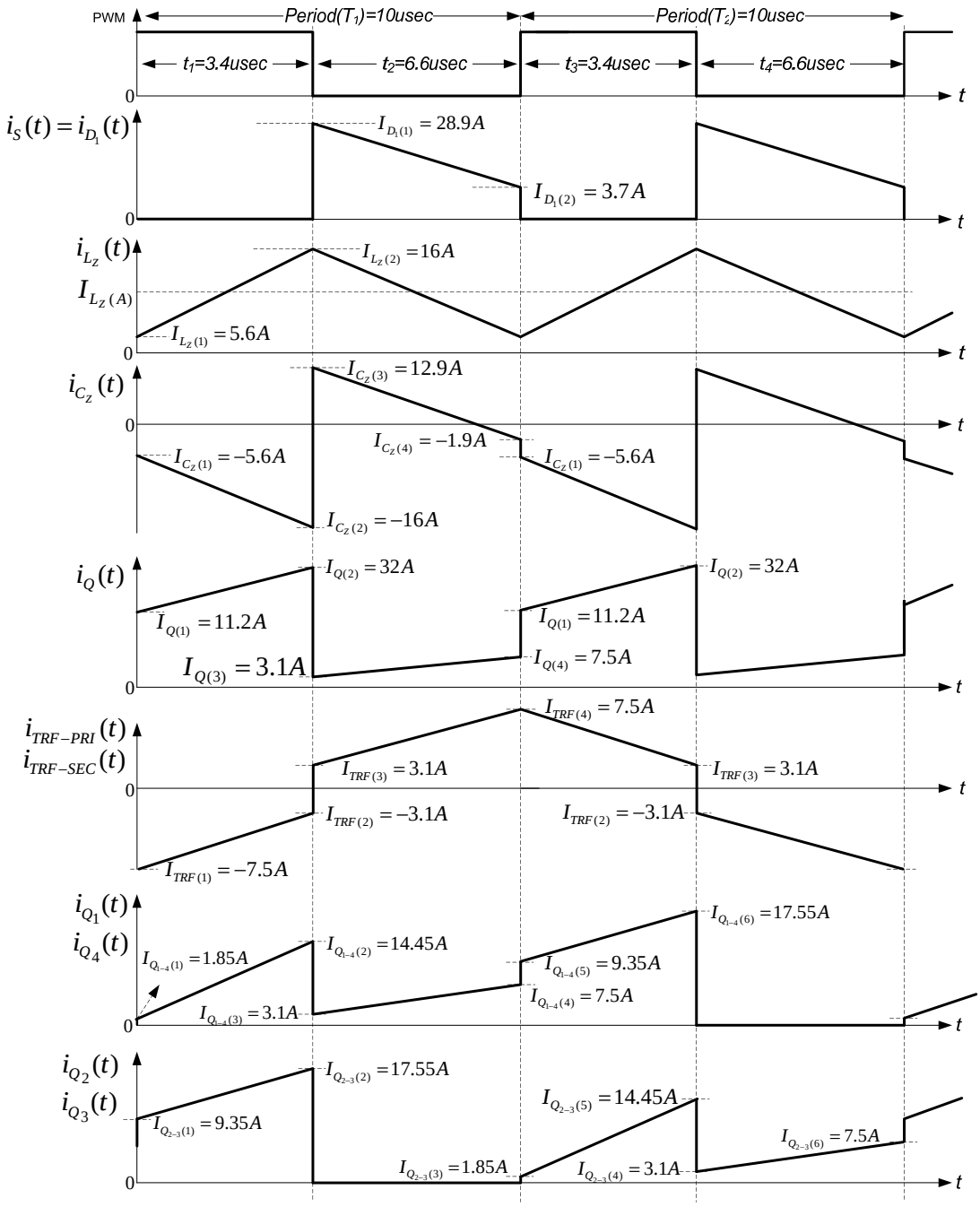

Fig.4.25 Current waveforms for several components of open-loop drive of Z-source full bridge dc/dc converter-2

By the symmetry of the circuit, the instantaneous currents ($i_{Q_1}(t)$ and $i_{Q_4}(t)$) are equal to each other. Also, the instantaneous currents of switches Q_2 and Q_3 ($i_{Q_2}(t)$ and $i_{Q_3}(t)$) are equal to each other. Applying Kirchhoff's current law at NODE III and NODE IV in Fig.4.23 gives the results as;

$$i_Q(t) = i_{Q_1}(t) + i_{Q2}(t)$$
$$i_{Q_1}(t) = i_{TRF-PRI} + i_{Q_3}(t) = i_{TRF-PRI} + i_{Q_2}(t) = \frac{i_{TRF-PRI} + i_Q(t)}{2} \quad (4.3)$$

By using (4.1), (4.2) and (4.3), and also the measurements of Z-source inductor and input diode current from Section 4.2, the current waveforms of switches and Z-source capacitors can be determined. The current waveforms of the input diode, the Z-source inductor, switches and the Z-source capacitors are all shown in Fig.4.25, as complementing waveforms to those given in Fig.4.24.

4.5.1 Power Losses on Switching Elements (MOSFETs)

The losses at MOSFETs can be divided into two groups such as switching losses and conduction losses. Switching losses are occurred at the transition of 'ON' to 'OFF' state or visa versa. The resistance of MOSFET at 'ON' state leads to conduction losses.

From [19], the formula for switching losses of a MOSFET can be expressed as,

$$P_{SW(MOS)} = P_{TURNON} + P_{TURNOFF} = \frac{1}{2} \cdot V_{DS} . I_D \cdot t_{ON} \cdot f_{sw} + \frac{1}{2} \cdot V_{DS} . I_D \cdot t_{OFF} \cdot f_{sw} \quad (4.4)$$

where,

$$t_{ON} = V_{DS} \frac{R_{drive} \cdot C_{rss}}{V_{drive} - \left(V_t + \frac{I_D}{g} \right)} - R_{drive} \cdot C_{iss} \cdot \ln \left(1 - \frac{I_D}{g \cdot (V_{drive} - V_t)} \right)$$

representing the time taken to put the device into the conducting state fully from the 'OFF' state

$$t_{OFF} = \frac{V_{DS} \cdot R_{drive} \cdot C_{rss}}{V_t - \frac{I_D}{g} - V_{sat}} + R_{drive} \cdot C_{iss} \cdot \ln\left(\frac{V_t + \frac{I_D}{g} - V_{sat}}{V_t - V_{sat}} \right)$$

likewise this is representing the time taken to take the device from conducting state to full blocking state.

The terms t_{ON} and t_{OFF} are known as turn on and turn off time, respectively. V_{DS} and I_D are abbreviations of MOSFET's drain-to-source voltage and drain current after (or before) switching. f_{sw} is the switching frequency of the MOSFET which is $50kHz$ in this work. V_{drive}, R_{drive} and V_{sat} are the MOSFET driver circuit parameters which are MOSFET gate-to-source voltage imposed on the gate of the switch when it is 'ON', gate drive circuit impedance, and MOSFET gate-to-source voltage when switch is 'OFF', respectively. The parameters C_{rss}, C_{iss}, V_t and g are obtained from the datasheet of the MOSFET and they correspond to; the reverse transfer capacitance, the input capacitance, the gate threshold voltage and the forward transconductance of MOSFET, respectively.

In MOSFET drive circuit, V_{drive} is set to $15V$ and V_{sat} is $0.2V$. Also, total gate impedance of gate drive is calculated as 9.78Ω. The MOSFET used in prototype is IRFP4568pbf from International Rectifier. The datasheet [20] of the MOSFET defines that, $C_{rss} = 203pF$, $C_{iss} = 10470pF$, $V_t \cong 4V$ and $g = 162S$. Referring to Fig.4.25, it can be seen that MOSFET drain current, I_D, is $17.55A$ during turn-off time and it is $1.85A$ at turn on. Also, drain-to-source voltage, V_{DS}, is $85V$ for both cases. By substituting the numerical data related to parameters into (4.4) gives the switching loss of the MOSFET, used in the circuit as;

$$P_{SW(MOS)} = \frac{1}{2} \cdot 85 \cdot 50000 \cdot \left(1.85 \cdot 15.46n\sec + 17.55 \cdot 48.59n\sec\right) = 1.873W \qquad (4.5)$$

The conduction loss on the MOSFET is the product of, on state resistance of MOSFET, $R_{DS(ON)}$, and the square of MOSFET rms current, $I_{RMS(MOS)}{}^2$. $I_{RMS(MOS)}{}^2$, can be calculated by using the MOSFET current waveform, $i_{MOS}(t)$, appearing in Fig.4.25. Also, $R_{DS(ON)}$ is defined in the datasheet [20] as $5m\Omega$ for IRFP4568pbf. To yield the conduction loss as;

$$P_{COND(MOS)} = I_{RMS(MOS)}{}^2 \cdot R_{DS(ON)} = 55.04A^2 \cdot 5m\Omega = 0.275W \quad (4.6)$$

Thus, the total power loss, P_{MOS}, on MOSFET being the sum of switching loss and conduction loss such as;

$$P_{MOS} = P_{COND(MOS)} + P_{SW(MOS)} = 1.873 + 0.275 = 2.148W \quad (4.7)$$

4.5.2 Power Losses on Switching Elements (Diodes)

As in MOSFETs, diodes also have both switching losses and conduction losses. The conduction losses of the diodes are caused by the forward voltage drop, V_F. In prototype circuit ultra fast rectifier diodes are used to avoid the switching losses, hence the switching losses on the diodes are negligible. Thus, the total power dissipation on diodes is just due to the conduction loss.

Diode conduction loss can be calculated by multiplying the forward voltage drop, V_F, by the average current through the diode, $I_{DIODE(AV)}$, over a period;

$$P_{DIODE} = V_F \cdot I_{DIODE(AV)} \quad (4.8)$$

Note that the input diode, D_1, is a diode from Vishay Company with a code V60120C is used. When the datasheet [21] of the diode is examined, the instantaneous forward voltage drop, $V_{F(D_1)}$, at the instantaneous forward current, I_{D_1}, can be found. Referring to Fig.4.25, the average current of input diode, $I_{D_1(AV)}$, can be calculated. Thus, the power loss on D_1 is determined as;

$$P_{D_1} = V_{F(D_1)} \cdot I_{D_1(AV)} = V_{F(D_1)} \cdot \left(\frac{I_{D_1(1)} + I_{D_1(2)}}{2} \right) \cdot \frac{t_2}{T} = 0.67 \cdot \frac{28.9 + 3.7}{2} \cdot 0.66 = 7.20W \quad (4.9)$$

Considering diodes in the bridge rectifier, D_2, D_3, D_4 and D_5, they are from Microsemi Company with a code UFT20015. The conduction losses on these diodes can be calculated likewise. The forward voltage drop on the diode considered can be gathered from datasheet [22] of the diode due to an average current. The average current through diode can be calculated considering the relevant current waveform seen in Fig.4.24. Thus, the conduction loss on a rectifier diode is;

$$P_{D_2} = V_{F(D_2)} \cdot I_{D_2(AV)} = V_{F(D_2)} \cdot \left(\frac{I_{D_2(1)} + I_{D_2(2)}}{2} \cdot \frac{t_2 + t_3}{2 \cdot T} \right) \quad (4.10)$$

$$P_{D_2} = 0.68 \cdot 2.65 = 1.8W$$

4.5.3 Capacitor Power Losses

Every capacitor has an equivalent series resistance (ESR) and, therefore, there is some power loss on this capacitor whenever ac current pass through it. Thus, in Z-source full bridge dc/dc converter, both the Z-source capacitors and the output capacitor lead to some power losses during the operation.

The power dissipation on a capacitor can be calculated as,

$$P_{CAP} = I_{RMS(CAP)}{}^2 \cdot ESR_C \quad (4.11)$$

In (4.11), $I_{RMS(CAP)}$ corresponds the rms current through the capacitor and ESR_C represents the equivalent series resistance of the capacitor. As Z-source capacitors, five M39003/01-2374C capacitors, from Vishay Company, are used in parallel to reduce the total ESR value. The ESR for one capacitor measured by a Precision LCR Meter, HP-4285A is found as $0.345m\Omega$. Five capacitors being in parallel, the equivalent ESR value, ESR_{C_z}, is $69.3m\Omega$ for Z-source capacitors. Also, capacitor

rms current, $I_{RMS(C_Z)}{}^2$ can be calculated the related waveform seen in Fig.4.25. Thus, the power dissipation in Z-source capacitors is, by (4.11);

$$P_{C_Z} = I_{RMS(C_Z)}{}^2 \cdot ESR_{C_Z} = 74.721A^2 \cdot 69.3m\Omega = 5.178W \quad (4.12)$$

For the output capacitor, four parallel capacitors with the code MAL204313101ES, from Vishay Company, are used. The ESR value of a MAL204313101ES is measured by Precision LCR Meter to be 0.230Ω. Four capacitors being in parallel at the output, the equivalent ESR value is $ESR_{C_O} = \frac{0.23\Omega}{4} = 57.5m\Omega$. Thus, the power dissipation at the output capacitors is,

$$P_{C_O} = I_{RMS(C_O)}{}^2 \cdot ESR_{C_O} = 1.6133A^2 \cdot 57.5m\Omega = 0.092Watts \quad (4.13)$$

4.5.4 Inductor Power Losses

The inductor losses comprise two components, the first is the loss arising in the inductor core and the second is the resistive losses in the winding. Core losses and AC winding losses are due to the ripple existing in the current through the inductor. The average value of inductor current gives rise to DC losses in the inductor winding.

For Z-source inductors, cores with a code K4020E090 from Magnetics Company have been used. 10 turns of 12AWG copper wire is wound around this core to have $20\mu H$ inductance. Referring to Fig.4.25, it can be noted that the Z-source inductor current swings between $5.6A$ and $16A$ with an average value of, $I_{L_Z(A)}$, is $10.8A$ and the peak-to-peak ripple of, $I_{L_Z(P-P)}$, is $10.4A$.

The calculation of the core loss of the Z-source inductor, the Flux Density (kilogauss) versus Core Loss (mW/cm^3) data is needed, a graph for the purpose is provided by the supplier of the core. Since the graph requires the magnetic field flux

density change, ΔB_{L_z}, corresponding to the peak-to-peak ripple current. ΔB_{L_z} can be found as;

$$\Delta B_{L_z} = \frac{N \cdot I_{L_z(P-P)} \cdot \mu_r \cdot \mu_0}{l_e} = \frac{10 \cdot 10.4A \cdot 75 \cdot 4 \cdot \pi \cdot 10^{-7}}{0.0984m} = 0.1T \quad (4.14)$$

where N is the turn number, μ_r is relative permeability, μ_0 is permeability of vacuum and l_e is the effective path length of the core. Although in the datasheet of the core states that μ_r is 90, DC biasing of the core changes the relative permeability. Thus, 75 for μ_r is found by using Permeability versus DC Bias Curve graph, which is supplied by the core manufacturer. The core loss per unit volume, $(P_{C/V})$, at $\Delta B_{L_z} = 0.01T$ can be found from the Flux Density versus Core Loss graph as, $P_{C/V} = 200mW/cm^3$. Thus, the total core loss in the inductor is the product of the effective volume of the core, V_e, by $P_{C/V}$.

$$P_{L_z(CORE)} = V_e \cdot (P_{C/V}) = 18cm^3 \cdot 200mW/cm^3 = 3.6W \quad (4.15)$$

Windings in the inductors used 12AWG copper wire with a resistance per unit length is $0.00522\Omega/m$. The coil bobbin has $0.0914m$ length/turn and inductor has 10 turns. Hence, the DC resistance, R_{DC}, of the winding can be found as,

$$R_{DC(L_z)} = 0.00522\Omega/m \cdot 10 \cdot 0.0914m = 4.77m\Omega \quad (4.16)$$

The ratio of resistance, R_{AC}, to dc resistance, R_{DC}, for the winding can be found by using Dowell's curves [23]. The use of this curve gives,

$$R_{AC(L_z)} \cong 10 \cdot R_{DC(L_z)} = 8.5 \cdot 4.77m\Omega = 40.54m\Omega \quad (4.17)$$

After the determination of R_{AC} and R_{DC}, total winding loss can be expressed as;

$$P_{L_z(WIND)} = R_{DC}.I_{L_z(A)}{}^2 + R_{DC}.I_{L_z(AC-RMS)}{}^2 = R_{DC}.I_{L_z(A)}{}^2 + R_{DC}\cdot\frac{I_{L_z(P-P)}{}^2}{12}$$
$$P_{L_z(WIND)} = 4.77m\cdot 10.8^2 + 40.54m\cdot\frac{10.4^2}{12} = 931mW \quad (4.18)$$

Total power loss on the Z-source inductor is the sum of the winding loss and the core loss than,

$$P_{L_z} = P_{L_z(WIND)} + P_{L_z(CORE)} = 0.931W + 3.6W = 4.531W \quad (4.19)$$

In order to calculate losses on the output inductor, the core loss and winding losses are calculated likewise as in the Z-source inductor case. A core with a code K3515E90 from Magnetics Company is used for the output inductor. 18 turns is wound around the core with 15AWG wire to get $50\mu H$ inductance value. Referring to Fig.4.24, it can be seen that the current passing through the inductor varies between $7.5A$ and $3.1A$ with an average current, $I_{L_O(A)}$, through the inductor of $5.3A$ and the peak-to-peak ripple, $I_{L_O(P-P)}$, magnitude of $4.4A$.

The magnetic field flux density variation, ΔB_{L_O}, corresponding such a ripple current magnitude is found by (4.14) as;

$$\Delta B_{L_O} = \frac{N\cdot I_{L_O(P-P)}\cdot\mu_r\cdot\mu_0}{l_e} = \frac{18\cdot 4.4A\cdot 74.54\cdot 4\cdot\pi\cdot 10^{-7}}{0.0694m} = 0.107T \quad (4.20)$$

Although the relative permeability, μ_r, is 90 according to datasheet, the average current, $I_{L_O(A)}$, causes some dc biasing of the core, so that decreases to 74.74. The new value of μ_r is determined from the Permeability versus DC Bias graph provided by the manufacturer.

By using the Flux Density versus Core Loss graph, the core loss per unit volume can be determined as, $P_{C/V} = 240mW/cm^3$. Since the effective volume of the core is, V_e, is $5.83cm^3$, the core loss in the output inductor is,

$$P_{L_O(CORE)} = V_e \cdot (P_{C/V}) = 5.83cm^3 \cdot 240mW/cm^3 = 1.4W \quad (4.21)$$

The inductor has 18turns, the mean length per turn is $0.0734m$ and the 15AWG wire has $0.01043\Omega/m$ resistance. Thus, the DC resistance, $R_{DC(L_O)}$, of the wire is,

$$R_{DC(L_O)} = 18 \cdot 0.0734m \cdot 0.01043\Omega/m = 13.8m\Omega \quad (4.22)$$

The ratio between the AC resistance, $R_{AC(L_O)}$, and $R_{DC(L_O)}$ of the winding can be found by using Dowell's curves[23]. Thus, $R_{AC(L_O)}$ is,

$$R_{AC(L_O)} \cong 18 \cdot R_{DC(L_O)} = 18 \cdot 13.8m\Omega = 250m\Omega \quad (4.23)$$

Since $R_{AC(L_O)}$ and $R_{DC(L_O)}$ are known, the total winding loss can then be found as;

$$P_{L_O(WIND)} = R_{DC}.I_{L_O(A)}{}^2 + R_{DC}.I_{L_O(AC-RMS)}{}^2 = R_{DC}.I_{L_O(A)}{}^2 + R_{DC} \cdot \frac{I_{L_O(P-P)}{}^2}{12}$$
$$P_{L_O(WIND)} = 13.8m \cdot 5.3^2 + 250m \cdot \frac{4.4^2}{12} = 791mW \quad (4.24)$$

The total power dissipation in the output inductor is the sum of the core and winding losses. Thus, the total loss in the inductor is,

$$P_{L_O} = P_{L_O(WIND)} + P_{L_O(CORE)} = 0.791W + 1.4W = 2.191W \quad (4.25)$$

4.5.5 Transformer Power Losses

Similar to that in the inductor, the power dissipation in the transformer can be divided into two loss components as core and copper losses. The transformer has a ferrite core with a code of OP45530EC P from Magnetics Company. Both windings primary and secondary have 10turns of 11AWG wire.

In order to calculate the core loss in the transformer, the peak-to-peak magnetic field in it must be determined. By using faraday's law ($\int Vdt = N \cdot \phi$) and the equality of $\phi = B \cdot A_e$, the total change in the magnetic field, ΔB, can be found as;

$$\Delta B = \frac{V_O \cdot Ts}{N \cdot A_e} = \frac{53V \cdot 10\mu\sec}{10 \cdot 420mm^2} = 0.126T \tag{4.26}$$

In (4.26), V_O is the output voltage, Ts is the period, N is the number of turns in the secondary winding and A_e is the effective cross sectional area of the core. The core loss per unit volume, $P_{C/V}$, can be determined using the Flux Density versus Core Loss graph provided by the core material manufacturer. Thus, the core loss per unit volume is found as $P_{C/V} = 23.7mW/cm^3$. Considering the effective volume of the core, V_e is $52cm^3$, the core loss of the transformer is found as;

$$P_{TRF(CORE)} = V_e \cdot (P_{C/V}) = 52cm^3 \cdot 23.7mW/cm^3 = 1.232W \tag{4.27}$$

The mean length per turn in either winding is 11.38cm. The resistance of 11AWG wire is $0.004132\Omega/m$ and since both primary and secondary has 10 turns, the DC resistance of primary and secondary winding is found as;

$$R_{DC(PRI)} = R_{DC(SEC)} = 10 \cdot 0.1138m \cdot 0.0041323\Omega/m = 4.7m\Omega \tag{4.28}$$

The AC resistance of the copper can be calculated by using Dowell's curves [23]. When the curve is examined, it is seen that the ratio between R_{AC} and R_{DC} for transformer copper is 7. The AC resistances of both primary and secondary windings are,

$$R_{AC(TRF-PRI)} = R_{AC(TRF-SEC)} = 7 \cdot R_{DC(PRI)} = 7 \cdot 4.7m\Omega = 32.9m\Omega \tag{4.29}$$

The average current through both primary and secondary windings over a period is zero. Therefore, there is no copper loss on the DC resistance in the transformer.

Furthermore, the copper loss due to AC resistance of the primary winding can be calculated as;

$$P_{AC(PRI)} = R_{AC(TRF-PRI)}.I_{RMS(PRI)}{}^{2} = 32.9 \cdot 30.21 = 994mW \quad (4.30)$$

Also, the copper loss due to AC resistance of the secondary side is;

$$P_{AC(SEC)} = R_{AC(TRF-SEC)}.I_{RMS(SEC)}{}^{2} = 32.9 \cdot 30.21 = 994mW \quad (4.31)$$

Thus, the total power loss in the transformer is,

$$P_{TRF} = P_{TRF(CORE)} + P_{AC(PRI)} + P_{AC(SEC)} = 3.22W \quad (4.32)$$

4.5.6 Analytical and Experimental Comparison of Calculated Efficiencies

The total power dissipation in the converter circuit can be found by adding all losses in the components. Noting that, there are two Z-source inductors, and two Z-source capacitors in the circuit, the calculated power loss, P_{L_z}, for the Z-source inductor and the power loss, P_{C_z}, for the Z-source capacitor are to be considered twice in the loss calculation. Furthermore, the power dissipation, P_{MOS}, on MOSFETs and the power dissipation, P_{D_O}, in the output diodes must be multiplied by four in finding the total power dissipation. Thus, calculated overall power loss in the circuit is;

$$\begin{aligned} P_{DISS(CALC)} &= 4 \cdot P_{MOS} + P_{D_1} + 4 \cdot P_{D_O} + 2 \cdot P_{C_z} + P_{C_O} + 2 \cdot P_{L_z} + P_{L_O} + P_{TRF} \\ P_{DISS(CALC)} &= 47.913W \end{aligned} \quad (4.33)$$

The input power, drawn by the circuit, is the multiplication of the average input current and the average input voltage. The total current-time area of the Z-source capacitor and the output capacitor is zero over a period. Thus, from Fig.4.23, it can be seen that, the average input current is equal to the Z-source inductor average current, $I_{L_z(A)}$, and the output current is equal to the output inductor average

current, $I_{L_O(A)}$. By using these facts, input power, output power and measured power dissipation can be found as;

$$\begin{aligned} P_{IN} &= I_{L_Z(A)} \cdot V_S = 10.8A \cdot 30V = 324W \\ P_{OUT} &= I_{L_O(A)} \cdot V_O = 5.3A \cdot 53V = 280.9W \\ P_{DISS(MEAS)} &= P_{IN} - P_{OUT} = 324W - 280.9W = 43.1W \end{aligned} \quad (4.34)$$

There is a little difference between the calculated power dissipation and measured power dissipation. The main reason of this difference is the diodes forward voltage drops and capacitor ESR. When the power dissipation on diodes and capacitors are calculated, it is assumed that the temperature is 25°C. However, the junction temperature of diode or capacitor increases when power dissipation occurs on the component. Increased junction temperature leads to decreasing of forward voltage drop of a diode and reducing the ESR of capacitor. For these purposes, the measured power dissipation is less than the calculated power dissipation.

The efficiency, η, of the converter can be found by dividing the output power to the input power such as,

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{280.9W}{324W} = 0.867 = \%86.7 \quad (4.35)$$

The efficiency, found in (4.35), is the efficiency of the open loop drive when input voltage, V_O, is $30V$, the output resistance is 10Ω and the duty-factor is 0.34. Table4.2 and Fig.4.26 display the measured efficiency of the closed-loop drive under varying output current. Note that Table4.2 displays efficiency for two different input voltage level, $30V$ and $45V$, respectively.

Referring to Fig.4.26, one finds that the closed-loop efficiency at $30V$ input is 76.5% when the load current is $6.11A$. The efficiency of the open loop drive is 86.7%. When the output voltage is regulated, more power is drawn from the source to compensate the power losses in the circuit. More power with fixed input voltage causes more current drawn from the source. Increasing of the current causes more power dissipation on components and this condition lowers efficiency drastically.

Also, the efficiency results of $45V$ input in Fig.4.26 are much higher than $30V$ input conditions. By incrementing the input voltage up, the current drawn from the source decreases and less power dissipation occurs on components. Thus, the efficiency increases. Furthermore, if the load current demand decreases, the current drawn from the source decreases and this also leads to better efficiency.

Table4.2 Efficiency of the Z-source full bridge dc/dc converter prototype against the load current variation

Input Voltage, V_S (Volt)	**Input Current, I_S (Amphere)**	**Output Voltage, V_O (Volt)**	**Output Current (Amphere)**	**Efficiency, η**
29.93	2.60	59.79	1.1	0.845164358
29.89	5.10	59.79	2.1	0.823667172
29.84	7.70	59.78	3.1	0.806543992
29.80	10.20	59.79	4.1	0.806484406
29.75	13.40	59.79	5.1	0.764904051
29.70	16.10	59.79	6.1	0.762739193
44.95	1.48	59.80	1.1	0.988786339
44.93	2.85	59.79	2.1	0.980542833
44.90	4.25	59.78	3.1	0.971141098
44.88	5.70	59.78	4.1	0.958102699
44.85	7.35	59.79	5.1	0.925015357
44.82	8.80	59.78	6.1	0.924551742

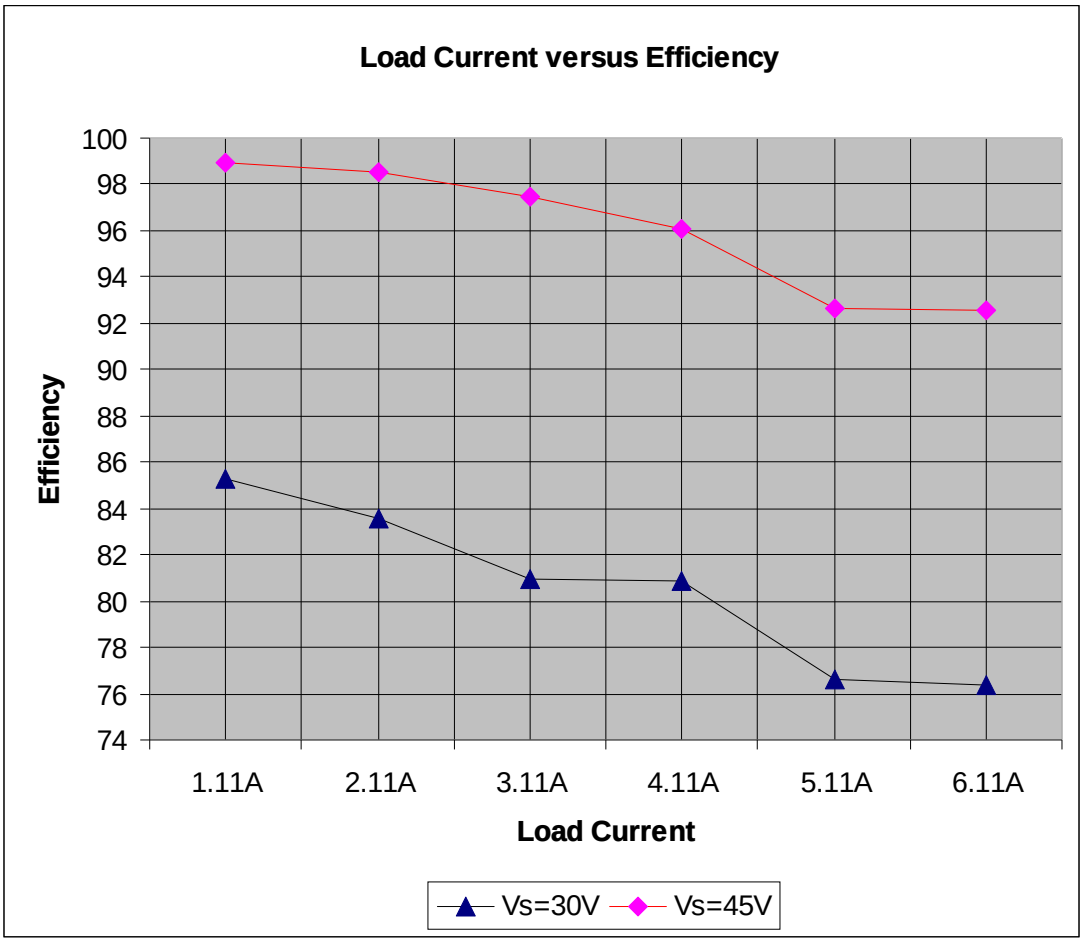

Fig.4.26 Efficiency of the Z-source full bridge dc/dc converter against the load current variations

4.6 Conclusion of Chapter

In the first part of the chapter a brief introduction is given. In the second part, current waveforms of input diode, Z-source inductor and output inductor for the prototype circuit are represented for continuous current mode operation. These waveforms are compared with the simulation results. In the third part, the same current waveforms are given for discontinuous current mode operation and also, these experimental results are compared with the simulation results. It is seen that the experimental results of both CCM and DCM operations are similar in terms of shapes of the

waveforms. Such that, both the peak and bottom values of the measured currents are same, respectively. In the next part, to show the controller performance, the output voltage response to step input voltage and step load current transients are shown. It is seen that the recovery time of the output voltage and both the overshoot and undershoot values are high. This is due to the fact that the cut-off frequency of $G_{OPEN-CCM}(s)$ is decreased down to $14 rad/\sec$. For the last part of the chapter, power dissipations on individual components are calculated and the results are compared with the measured ones. They are about the same with each other. Thus, the power loss on each component can be predicted before the hardware implementation. Also, the efficiency versus load current graph under various input voltages is provided for the closed-loop prototype circuit. From Fig.4.26, for the same output power, if the input voltage is increased, the efficiency of the converter also increases; because the current is drawn from the source is less and therefore power dissipations on the components are decreased.

CHAPTER 5

CONCLUSION AND FUTURE WORKS

5.1 Conclusions

The main scope of this thesis is design and implementation of Z-source full bridge dc/dc converter. Actually, the full bridge dc/dc converter is a buck derived topology, thus, it is used to step down the input voltage to a smaller output voltage. By using the Z-source structure, the full bridge dc/dc converter is used as a step up converter which converts the input voltage to a higher output voltage. Although the Z-source structure is investigated widely in switch mode power supplies, most of the studies met are about inverters, just a few studies on Z-source dc/dc converters are available in the field. Thus, lack of knowledge on the following aspects: investigation of operational principles; analytical derivations of input output relationships; and determination of transfer have, therefore, been the main points of interest of this study.

The circuit analyses of the proposed Z-source full-bridge dc/dc converter were not dealt with before in the literature. Thus, the CCM and DCM operation analyses of the Z-source dc/dc converter are conducted in Chapter 2. The current and voltage waveforms of the components derived in the study and the input voltage-to-output voltage relationship are compared with simulations and prototype circuit measurements. The simulation results closely agree with the theoretical calculations because both theoretical analyses and simulations have been conducted under ideal conditions. The results obtained in the prototype circuit have slightly departed from those obtained from theoretical calculations and simulations. The reason for this is the power losses on the circuital components in the experimental circuit, but they have all been ignored in theoretical calculation and ideal circuit simulations. Furthermore, the shapes of currents through the inductor and the input diode

obtained in theoretical analyses, simulations and measurements made on the prototype circuit exactly match with each other.

When designing a controller for a controller, the transfer functions and small signal model of the power stage must be determined beforehand. Thus the knowledge of duty factor-to-output voltage transfer function, $G_{vd}(s)$, is a good basis to design a voltage controlled converter to start with. Transfer functions on; duty factor-to-output voltage, $G_{vd}(s)$, duty factor-to-Z-source inductor current, $G_{id}(s)$, and input voltage-to-Z-source inductor current, $G_{ig}(s)$ are also investigated to determine the transfer function of control signal-to-output voltage, $G_{vc}(s)$, in peak current control method. The validity $G_{vd}(s)$, $G_{vd}(s)$, $G_{id}(s)$ and $G_{ig}(s)$ are verified via simulations. Hence a voltage controller could be designed to compensate the output voltage. The phase of the $G_{vd}(s)$ decreases by $180°$ at the resonant poles which complicates the controller design because the transfer function has two resonant poles. The gain of the controller has been decreased drastically to obtain the required gain and phase margins. Decrement of the gain lead to very low cut off frequency and it slowed the controller response against the input voltage and load transients. Thus, the settling time and the overshoots of the output voltage were both increased.

The prototype circuit efficiency could be increased. The input diode forward voltage drop led to significant power losses because it carried all the input current. Thus, using MOSFET instead of input diode could increase the efficiency. Also, for secondary side of transformer a full wave rectifier was used. The diodes at rectifier circuit caused power losses because of the forward voltage drop. By using synchronous rectification and center tap structure for secondary side, the efficiency could be increased. Additionally, rms current of Z-source capacitors are the source of significant amount of power losses. Thus, usage of lower ESR capacitors would also increase the efficiency. The core and copper losses of magnetic elements were not well balanced at prototype circuit. Balancing these losses would result smaller inductor and transformer sizes. When the input voltage decreases at Z-source dc/dc converter, more input current is required for the same amount of output power, as expected. However, the rms current of input diode and Z-source capacitors

increases more rapidly than input current. Thus, Z-source can provide high efficiency for high input voltage and low input current applications.

5.2 Future Works

All components of Z-source dc/dc converter are assumed to be ideal in derivation of transfer functions. However, the ESR of Z-source and output capacitors, forward voltage drop on the diodes, on state resistance of MOSFETs and resistance of inductors should also be taken into account to get more accurate representative transfer functions. Furthermore, including the leakage inductance and resistance of transformer in the analysis bring more accurate transfer functions for Z-source full bridge dc/dc converter.

In this research, it is assumed that the output inductor current never falls to zero neither in CCM operation nor in DCM operation. The decrement of load current or output inductor size can cause the current through the output inductor to fall to zero. This effect and transfer functions of this mode can mathematically be analyzed for future research.

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APPENDIX A

CIRCUIT SCHEMATICS OF Z-SOURCE FULL BRIDGE DC/DC CONVERTER

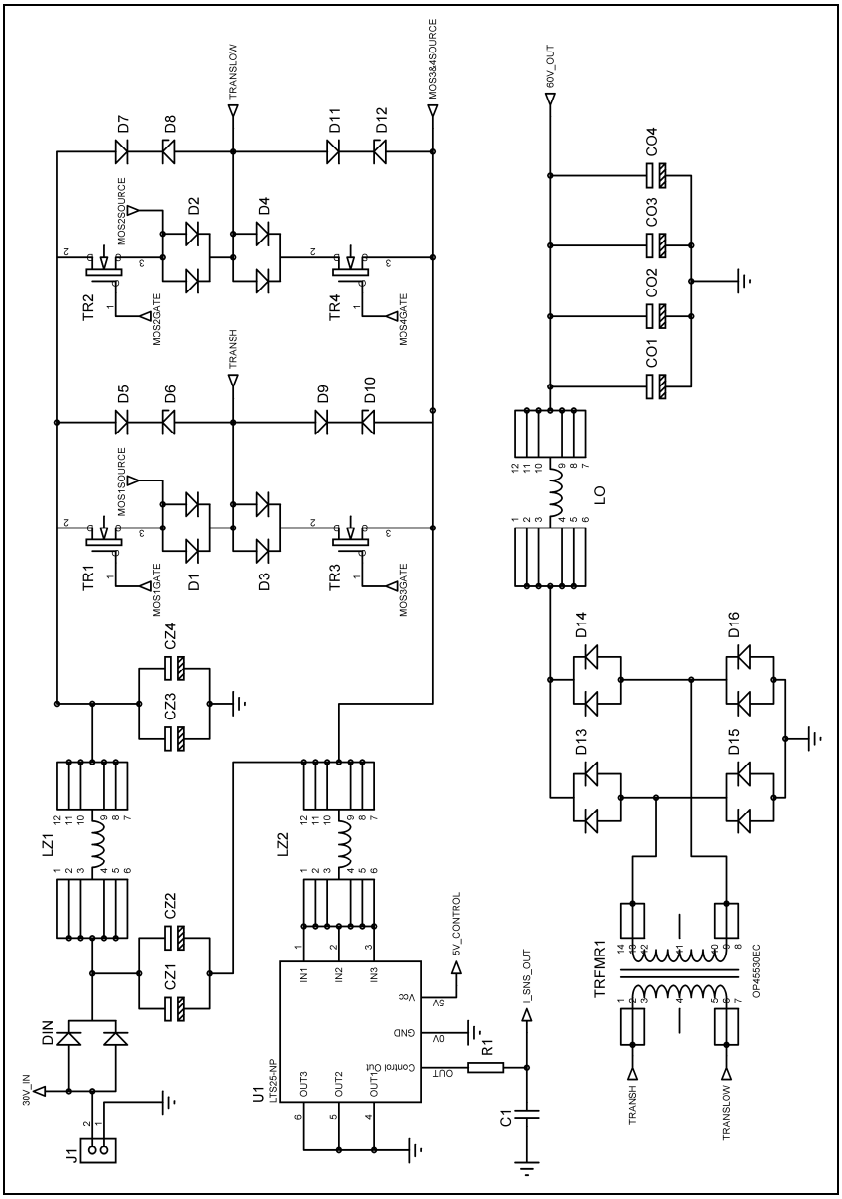

Fig.A.1 Circuit schematic of Z-source full bridge dc/dc converter (power line – sheet 1)

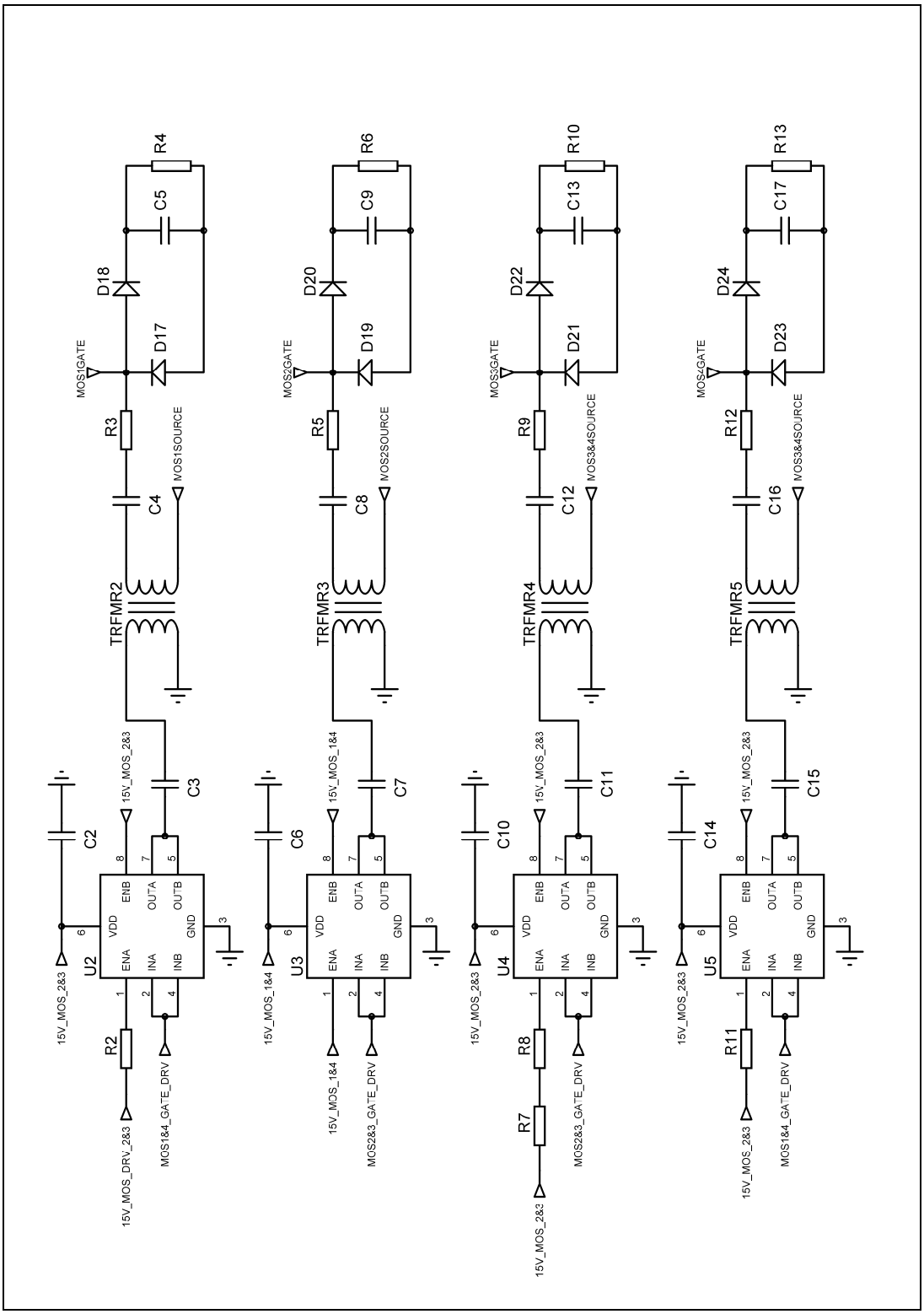

Fig.A.2 Circuit schematic of Z-source full bridge dc/dc converter (MOSFET drivers – sheet 2)

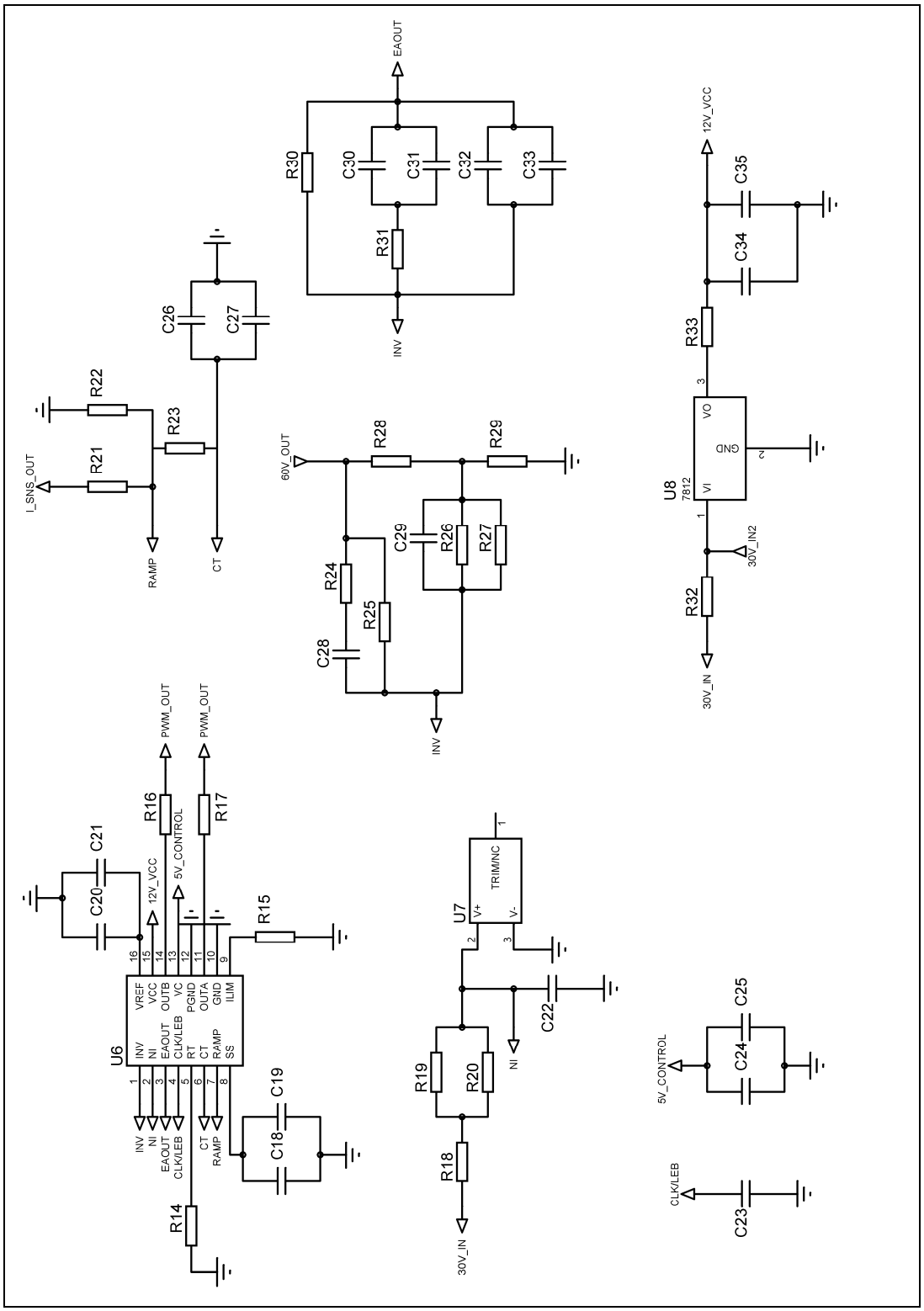

Fig.A.3 Circuit schematic of Z-source full bridge dc/dc converter (controller – sheet 3)

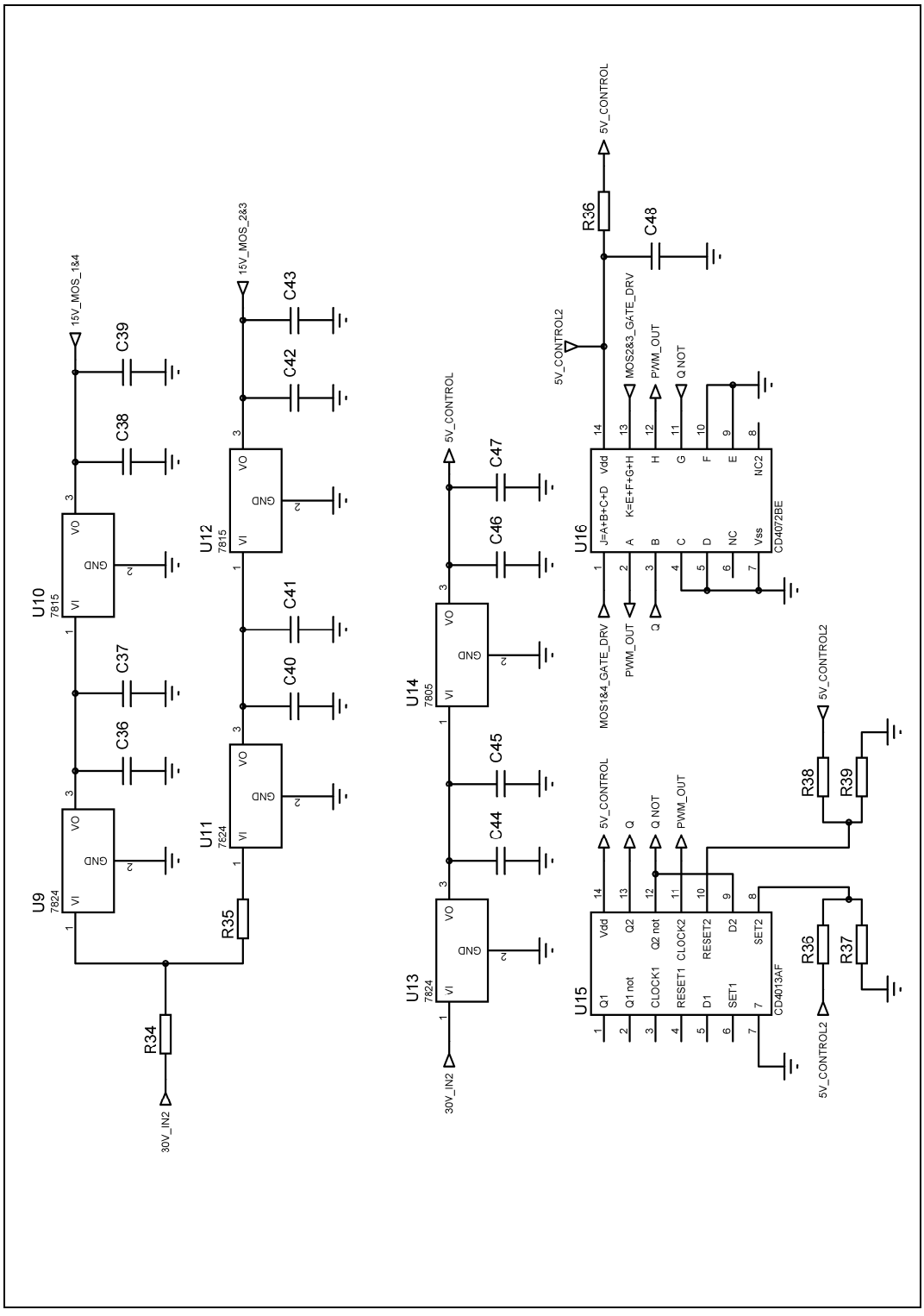

Fig.A.4 Circuit schematic of Z-source full bridge dc/dc converter (supply of internal circuitry and generation of MOSFET drive signals (PWM)– sheet 4)

APPENDIX B

BOARD LAYOUT OF Z-SOURCE FULL BRIDGE DC/DC CONVERTER

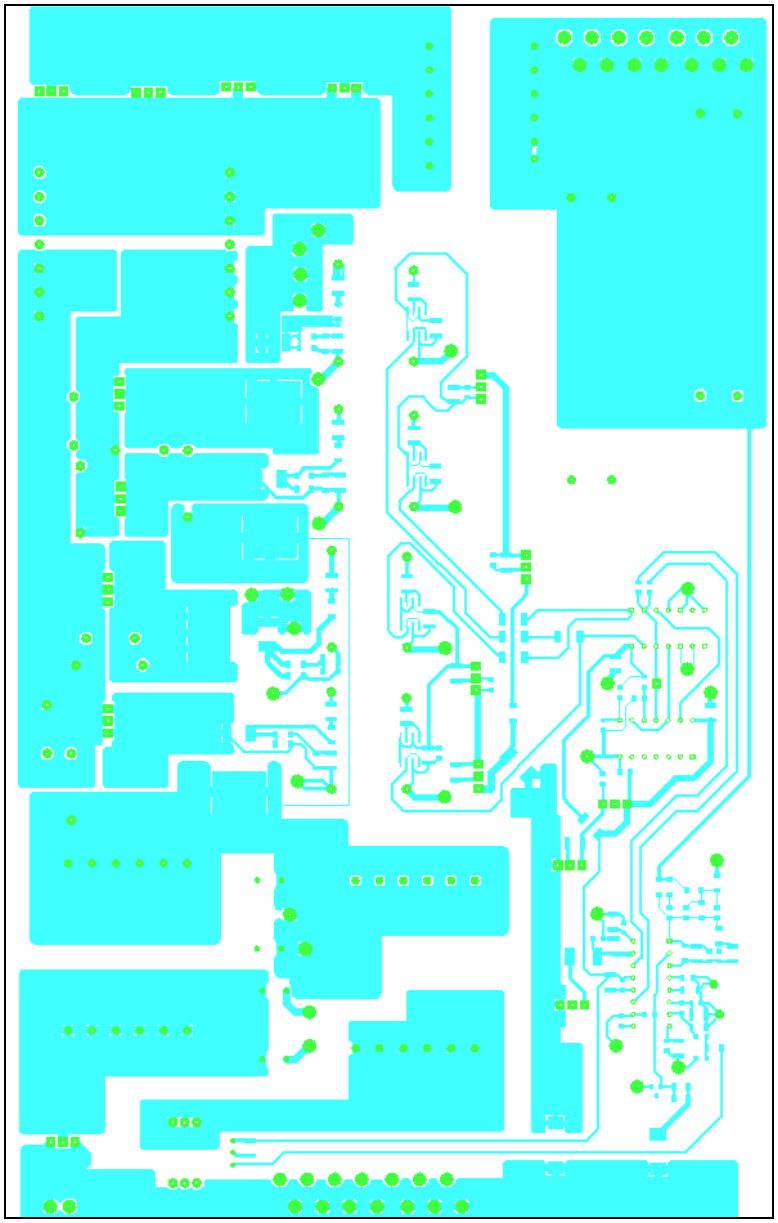

Fig.B.1Top side layout of Z-source full bridge dc/dc converter

Fig.B.2 Bottom side layout of Z-source full bridge dc/dc converter

APPENDIX C

PHOTOGRAPH OF Z-SOURCE FULL BRIDGE DC/DC CONVERTER

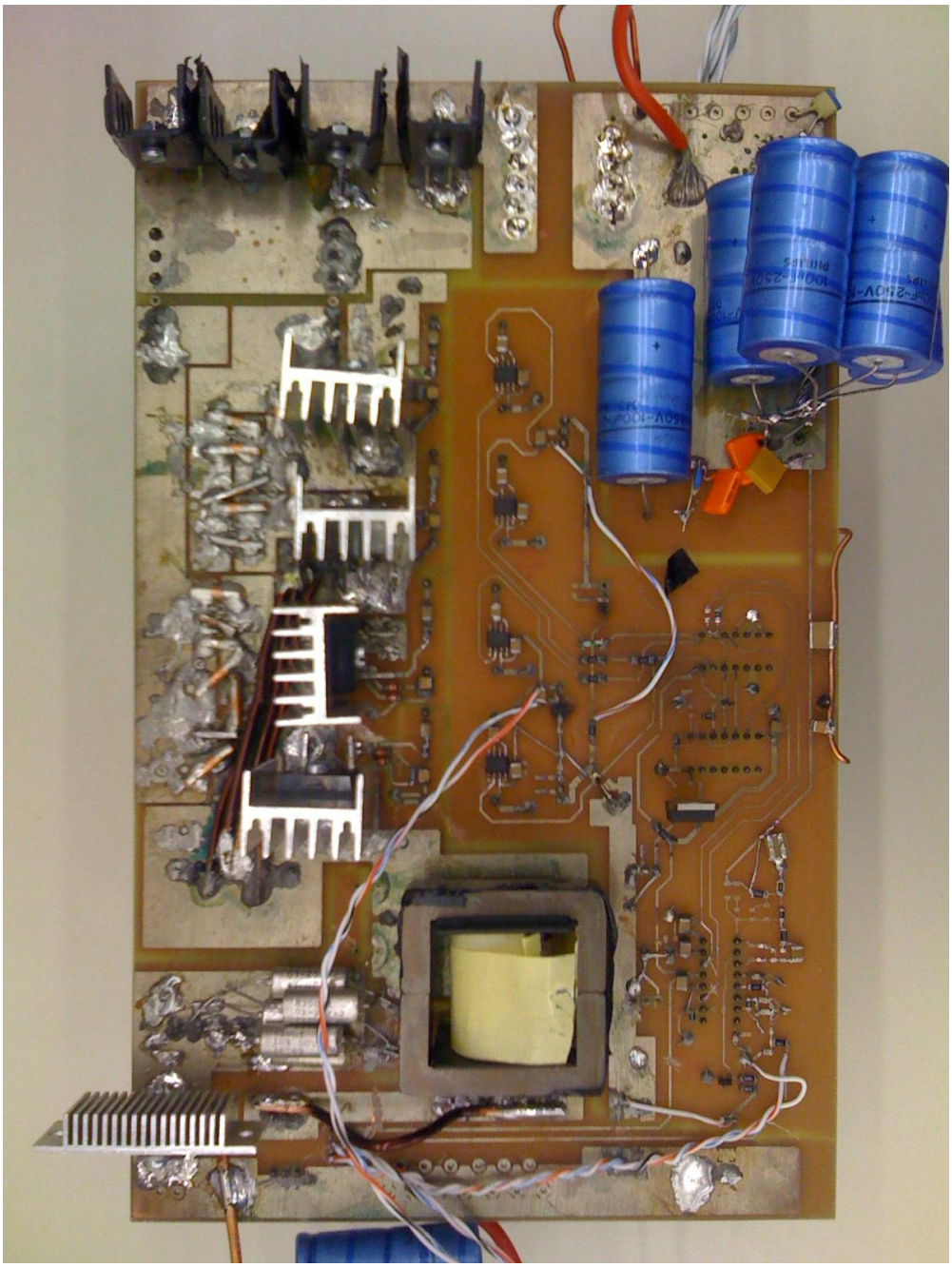

Fig.C.1 Photograph of Z-source full bridge dc/dc converter (component side)

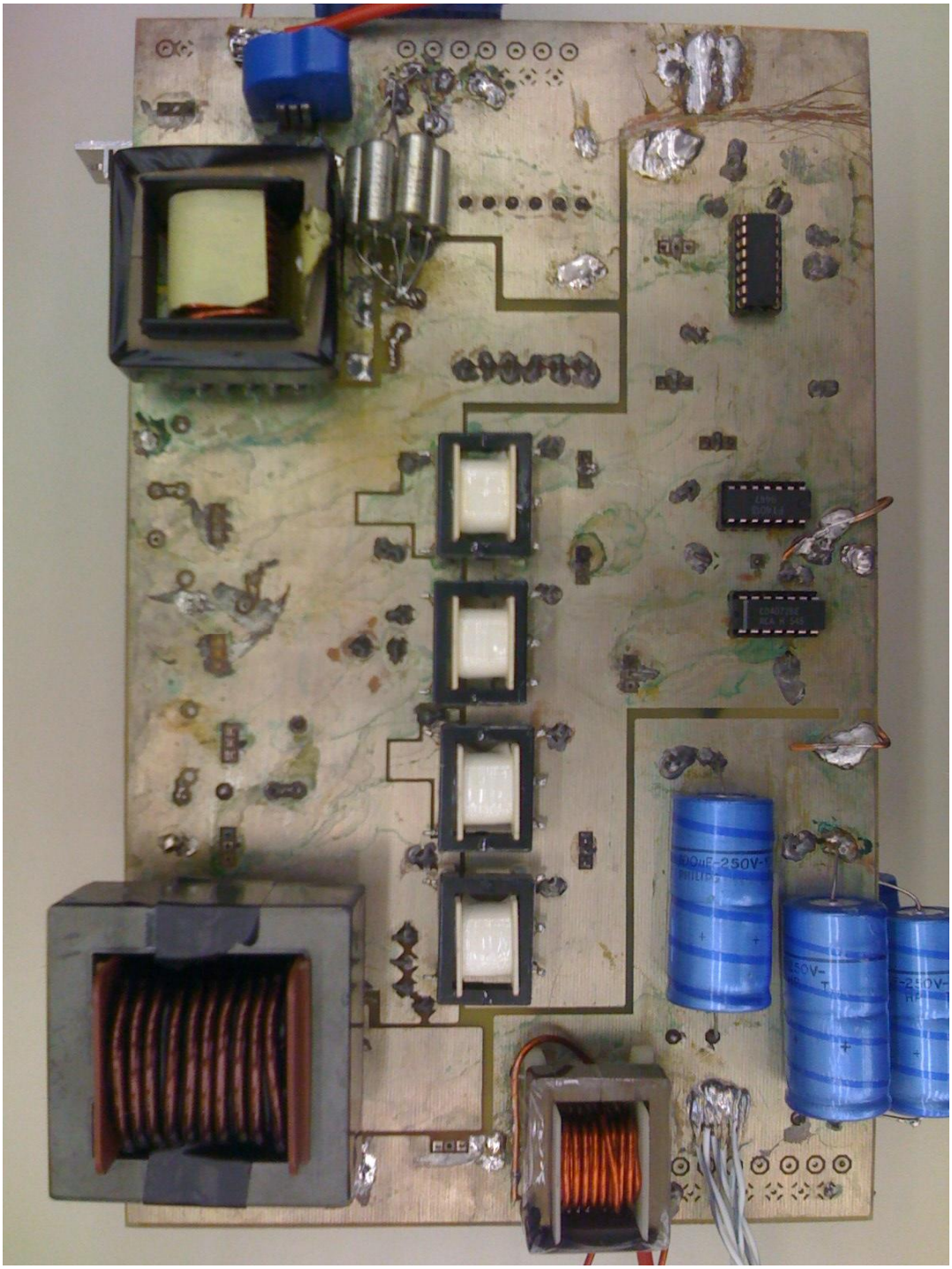

Fig.C.2 Photograph of Z-source full bridge dc/dc converter (solder side)