DEVELOPMENT AND MICROFABRICATION OF CAPACITIVE MICROMACHINED ULTRASOUND TRANSDUCERS WITH DIAMOND MEMBRANES

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

MEHMET CEZAR

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

FEBRUARY 2011

Approval of the thesis:

DEVELOPMENT AND MICROFABRICATION OF CAPACITIVE MICROMACHINED ULTRASOUND TRANSDUCERS WITH DIAMOND MEMBRANES

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ABSTRACT

DEVELOPMENT AND MICROFABRICATION OF CAPACITIVE MICROMACHINED ULTRASOUND TRANSDUCERS WITH DIAMOND MEMBRANES

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February 2011, 129 pages

This thesis presents the development and microfabrication of capacitive micromachined ultrasonic transducers (CMUT) with diamond membranes for the first time in the literature. Although silicon and silicon nitride (Si_3N_4) membranes have been generally used as the membrane material in CMUTs. These membrane materials have moderate properties that can cause damage during the operation of CMUTs. In this thesis, a new material for the membrane is introduced for CMUTs. Diamond has exceptional potential in the area of micro-nano technologies due to unrivalled stiffness and hardness, excellent tribological performance, highly tailorable and stable surface chemistry, high thermal conductivity and low thermal expansion, high acoustic velocity of propagating waves, and biocompatibility. Based on these excellent material properties, diamond is employed in the new generation CMUT structures for more robust and reliable operations.

The microfabrication process of CMUT has been generally performed with either sacrificial release process or wafer bonding technique. High yield and low cost features of wafer bonding process makes it preferable for CMUT devices. In this thesis, plasma-activated direct wafer

bonding process was developed for the microfabrication of 16-element 1-D CMUT arrays with diamond membranes. They were designed to operate at different resonance frequencies in the range of 1 MHz and 10 MHz with different cell diameters (120, 88, 72, 54, 44 μm) and element spacing (250, 375 μm).

1-D CMUT array devices can be used for focusing ultrasound applications. The electronic circuit for 1-D CMUT devices with diamond membranes was designed and implemented on PCB for the ultrasound focusing experiment. This electronic circuit generates continuous or burst AC signals of ± 15 V with different and adjustable phase shifting options at 3 MHz frequency.

16 elements of 72 μm 1-D CMUT array were successfully tested. Fully functional 7 elements of 1-D CMUT array are focused at an axial distance of 5.81 mm on the normal to the CMUT center plane. The CMUT array was excited using 10 V_{p-p} with 10 cycles sinusoidal signals at 3 MHz.

The microfabrication process and focusing ultrasound of 1-D CMUT devices with diamond membranes are done successfully in this thesis.

Keywords: Capacitive Micromachined Ultrasonic Transducers (CMUTs), Ultrasound, Diamond, MEMS, Microfabrication

ÖZ

ELMAS MEMBRANLI KAPASİTİF MİKROÜRETİLMİŞ ULTRASON ÇEVİRGEÇLERİN GELİŞTİRİLMESİ VE ÜRETİLMESİ

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Tez Yöneticisi : Yard. Doç. Dr. Barış Bayram

Şubat 2011, 129 sayfa

Bu tez literatürde ilk defa elmas membranlı kapasitif mikro işlenmiş ultrasonik çevirgeçlerin geliştirilmesini ve mikroüretimini sunmaktadır. Silisyum ve silisyum nitrür (Si_3N_4) membranlar halihazırda CMUT'ların fiziksel yapılarında kullanılmaktadır. Bu ortalama özelliklere sahip membran malzemeleri CMUT'ların çalışma süreçlerinde hasara sebep olabilirler. Bu tezde, CMUT'ların membran yapıları için yeni bir malzeme sunulmuştur. Elmas, mikro-nano teknoloji alanında rakipsiz sertliği ve dayanıklılığı, sürtünmeyle ilgili mükemmel performansı, ayarlanabilen ve dengeli yüzey kimyası, yüksek termal iletkenliği ve düşük termal genleşmesi, içinde yayılan akustik dalgaların hızının yüksekliği, ve biyouyumluluğu ile olağanüstü potansiyele sahiptir. Bu mükemmel özelliklerinden dolayı elmas, yeni jenerasyon CMUT yapılarıyla, daha dayanıklı ve güvenilir çalışmalar için kullanılmıştır.

CMUT'ların mikroüretim işlemi ya feda katmanı işlemiyle ya da pul bağlama tekniğiyle yapılmıştır. Pul bağlama tekniğinin yüksek verim ve düşük üretim maliyeti, CMUT cihazları için tercih sebebi olmuştur. Bu tezde, elmas membranlı, 16 elemanlı 1-D CMUT cihazlarının mikroüretimi plazma ile active edilmiş doğrudan pul bağlama yöntemi ile geliştirilmiştir. 1

ile 10 MHz rezonans frekanslarında çalışabilmeleri için farklı çaplar (120, 88, 72, 54, 44 μm) ve eleman aralıklarıyla (250, 375 μm) tasarlanmışlardır.

1-D CMUT cihazları ultrason odaklama uygulamalarında kullanılabilir. Elmas membranlı 1-D CMUT cihazlarının ultrason odaklama deneyi için, elektronik devresi tasarlanmış ve PCB üzerine monte edilmiştir. Bu elektronik devre ± 15 V'luk sürekli veya burst AC sinyalini, 3 MHz frekansında farklı ve ayarlanabilir faz kaydırma seçenekleriyle üretmektedir.

72 μm 16 elemanlı 1-D CMUT dizisi başarıyla test edilmiştir. Tamamiyle fonksionel olan 7 eleman CMUT'ın merkez yüzeyine dik olan eksen üzerinde 5.81 mm'de odaklanmıştır. CMUT dizileri, 3 MHz'te 10 periyotluk 10 V_{p-p} sinüs sinyali ile uyarılmıştır.

Bu tezde elmas membranlı 1-D CMUT cihazlarının mikroüretim süreci ve ultrason odaklaması başarılı bir şekilde yapılmıştır.

Anahtar Kelimeler: Mikroüretilmiş Kapasitif Ultrason Çevirgeçler (CMUTs), Ultrason, Elmas, MEMS, Mikroüretim

ACKNOWLEDGMENTS

I would like to thank to Prof. Dr. Cengiz Beşikçi, Assoc. Prof. Şimşek Demir, Assoc. Prof. Haluk Külah, Dr. Said Emre Alper for their instructions and attendance to my thesis presentation.

I would like to express my sincere gratitude and thanks to my supervisor Assist. Prof. Dr. Barış Bayram for his support, friendly attitude, guidance and encouragement at each stage of this thesis study.

I would like to thank to members of ULTRAMEMS Research Group, Ahmet Murat Çetin, Serra Altınoluk, Serdar Görümlü, Mehmet Yüksekkaya for their support, sharing their knowledge, and their help in design, microfabrication and test of the CMUT devices and I would also like to express my special thanks İsfendiyar Darbaz for their support, encouragement, and friendship which gave me the energy to complete my thesis.

I would also like to express my special thanks to Orhan Akar for his support, sharing his knowledge, and his help for MEMS microfabrication process.

I would like to present my thanks to M. Yusuf Tanrıkulu and Özge Zorlu for their support, and their help in wire bonding of the CMUT devices.

Lastly, my sincerely thanks go to my parents, Mustafa Cezar and Sergül Cezar, my sister Özlem Cezar Demirer for their support and unlimited love.

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CHAPTER 1

INTRODUCTION

1.1 Micro-Electro-Mechanical Systems (MEMS)

Microelectromechanical systems are miniature and useful microsystems that include integrated electrical and mechanical components. Their size can change from micrometer to millimeter ranges. Advanced fabrication techniques are used to design devices that have complex mechanical components such as diaphragms, gears, etc. Besides, microfabrication technology can also bring cost benefits, which are directly resulted from batch production, low unit cost, and maintenance cost.

The major application areas of MEMS are sensors and actuators including industrial, automotive, and medical purposes. MEMS technology enables the conventional devices to be miniaturized and integrated, which brings smaller, faster and more robust systems. But it doesn‘t mean that MEMS technology is used for only that purpose. On the other hand, it serves as a design subject for novel mechanical devices and microsystems.

MEMS devices are microsystems that can control, sense and activate mechanical responses in micro or macro scales. In addition to this, microfabrication also enables production of large arrays of devices that can accomplish complex functions.

MEMS sensors and actuators have $12 billion market in 2004 and it is estimated $25 billion market in 2009 with 16% growth rate per year from 2004 to 2009 [1]. It is shown in Figure 1.1.

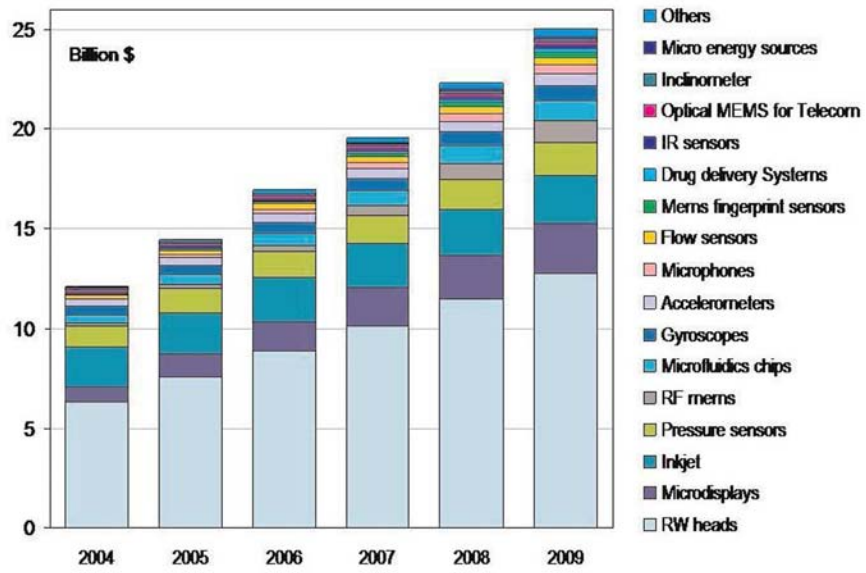

Figure 1.1: Total market for MEMS products [1]

1.2 Brief History of MEMS

Transistor technology was invented at Bell Telephone Laboratories in 1947. The invented new device sparked the growing technology which was microelectronic systems. After a decade, the first integrated circuit was invented by Texas Instruments in 1958. The success of transistors, with being basic components of integrated circuits, will bring microfabrication techniques for the future microsystems. Today, IC industry has a capability to fabricate submicron devices and systems.

Transducers which provide input and output functions from surrounding environment have a great role in microelectronic systems. That is the reason why IC fabrication technology focuses on production of low cost and high performance transducers.

Piezoelectric effect which was one of the most important discovery in 1880s plays a critical role in microsensor and actuator industry [2]. This discovery allows piezoelectric devices to be produced and developed. The National Semiconductor Company, which was established in 1959, was the prior to the production of first high volume pressure sensors [3].

Mechanical elements of the silicon microsensors were fabricated using several process tech-

niques. It was around 1982s when these fabrication techniques were begun to be called ”micromachining”. Isotropic and anisotropic etching approaches were developed in 1960 and 1967, respectively and introduced new capabilities for designing new mechanical elements of silicon microsensors.

Development of isotropic and anisotropic etching and etch-stop techniques precipitated the new idea called bulk micromachining process technique. This process technique is used to etch silicon substrate to keep the desired parts of the micromachine elements. It is one of the powerful processing approaches which opens new concepts and designing techniques for microsystems.

In 1965, Nathanson and Wickstrom deposited a material in order to isolate structural materials [4]. After the deposition process, they etched this material in order to be able to maintain moveable elements on silicon substrate. This processing approaches brought the new idea called sacrificial layer technique. Later on, this sacrificial layer concept supported the rise of new process subject called surface micromachining that uses silicon substrate as a backbone for the micromechanical elements to be fabricated on top of it.

During 1987-1988, pioneering microfabrication techniques were developed. After 1987s, MEMS term, which consists of microsystems and micromachining, was started to be used in whole world.

1.3 Ultrasound Transducers

Sound can be categorized in three section according to its frequency domain; Infrasound, acoustic and ultrasound. Ultrasound region, which is located at upper perception limit of human hearing, is approximately greater than 20 kHz. Categorized sound frequencies are shown in Figure 1.2.

Figure 1.2: Categorized sound frequencies

Ultrasound is used for broad range of applications; such as medical imaging, therapeutic treatments, nondestructive evolution (NDE), industrial cleaning, underwater exploration and ranging. At early ages, the generation of ultrasound waves was a challenging process. However, in 1880, with the discovery of piezoelectric effect, new ideas for the production of ultrasonic waves became possible [5]. This type of piezoelectric devices was used for underwater exploration and imaging during World War I. The medical applications of ultrasound have been developed for medical diagnosis and treatments. Today, focused ultrasonic waves can be potentially used for the treatment of prostate [6], breast [7] and liver [8] cancers.

Piezoelectric materials such as piezoelectric crystals, ceramics, and polymers have been popular materials that are used to emit and receive ultrasonic waves. Advanced fabrication techniques of micromachining technology enable the production of capacitive transducers with very small air gaps. This development makes the capacitive transducers competitive with piezoelectric technology. The first silicon micromachined electrostatic transducer was reported in 1990s [9]. The performance and characterization of the first generation of electrostatic transducers were not competitive with piezoelectric devices. Today, more advanced fabrication techniques are used to produce improved capacitive transducers, which are not only comparable with piezoelectric technology, but also outstanding.

Piezoelectricity is a physical phenomenon of certain crystalline materials that was first reported by Curie brothers in 1880 [10]. When the piezoelectric material was subjected to mechanical force, electrically polarized terminals could have been observed. The magnitude of the created voltage was proportional to the applied force. The reverse response of the piezoelectric material was also verified. The shape of the material started to change under the effect of applied voltage. These behaviors of material were named piezoelectric effect and inverse piezoelectric effect, respectively.

Piezoelectric effect is used in sensing application such as displacement and force sensors. Electrical response of the piezoelectric material requires an amplification block, because the material produces very small voltage excitations under applied force. Inverse piezoelectric effect is mostly used in actuating applications such as sonic and ultrasonic wave generations.

Piezoelectric materials can be categorized in three basic groups; crystals, ceramics and other special materials that show piezoelectric properties. In early ages of piezoelectric transducers, the quartz crystals were primarily used. When the piezoelectric ceramics were available, they were started to be used due to their good piezoelectric properties and ease of fabrication with desired shapes and sizes.

The thickness of the active element of the piezoelectric material plays an important role on the operating frequency of devices. This element will be vibrated under the effect of excitation voltage with a wavelength being equal to the twice of its thickness. If the high frequencies are desired, very thin active elements should be fabricated practically. Nevertheless, these thin elements are so fragile that high frequency piezoelectric transducers are not designed and produced [11]. They are not robust and reliable.

Matching layer on the active element is used to optimize bandwidth of the device and impedance mismatch of the propagation medium [12]. Matching of the impedance to the medium is critical in order to obtain efficient energy transfer between the medium and piezoelectric material. The thickness of the matching layer is adjusted a standard quarter wavelength as stated optimizations. Besides, matching layer keeps the reflected waves in phase when they propagate to the medium. The basic structure for piezoelectric transducer is shown in Figure 1.3.

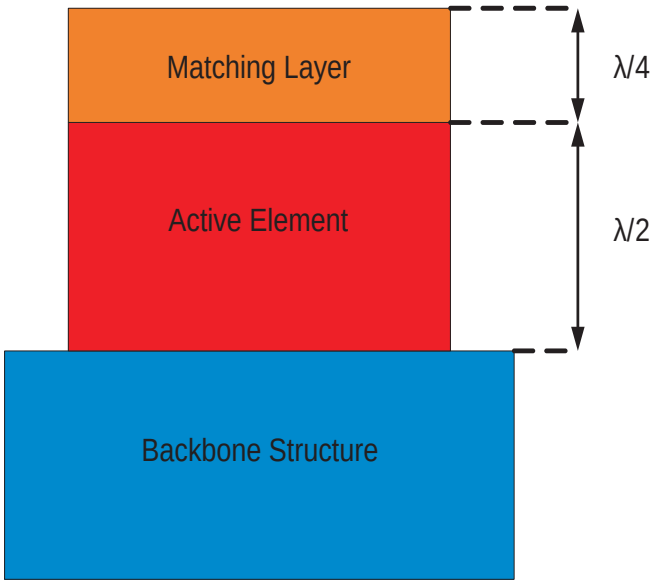

Figure 1.3: Basic structure for piezoelectric transducer [11]

The backbone structure is available for adjusting damping and sensitivity of the transducer device [11]. If the impedance of the active element is the same as backbone structure, it means that the damping is generated efficiently. This style of the transducer gains wider bandwidth and sensitivity.

Piezoelectric transducers are the well known devices that are used in ultrasound applications. This transducers should emit and receive ultrasonic signals with a good efficiency and large bandwidth especially for imaging applications. Medical treatments are another application area that piezoelectric transducers are used. The design of the single piezoelectric transducer for both medical imaging and treatment is a challenging design process.

Piezoelectric ceramics are widely used for the design of the transducers. However, these materials have some stability problems [13]. After polarization, they start to lose their piezoelectric material properties. This effect depends on composition of ceramic and fabrication process. Electrical depolarize effect can be shown as another limitation for piezoelectric ceramics. Powerful electric field that has direction opposite of polarizing field can depolarize the piezoelectric material. This unwanted effect can also depend on temperature and duration of applied electric field. Thermal effect is another point that piezoelectric ceramic causes some limitations. If the material is heated above a certain limit, material will be depolarized

due to the deformation of piezoelectric domains.

1.4 Objective of This Thesis

In this thesis, a new material for the membrane is introduced for CMUTs. Novel microfabrication steps and methods have been demonstrated for diamond material used as a membrane structure of CMUTs. Detailed objectives of this thesis are given below:

1- Diamond material is aimed to be used as a structural material for membranes of CMUTs. UNCD wafers are going to be applied to the flow of CMUT microfabrication steps in order to obtain diamond membranes. Direct wafer bonding technology is going to be used in CMUT microfabrication.

2- UNCD wafers are aimed to be characterized according to their cleanliness, roughness, waviness and stress parameters. These parameters should be chosen properly for robust direct wafer bonding.

3- All requirements of direct wafer bonding is expected to be obtained with deposition of the high temperature oxide (HTO) layer on diamond surface. In order to perform low temperature direct wafer bonding, the plasma activated surfaces are used.

4- Focusing electronics is aimed to be designed for ultrasound focusing experiment.

5- Ultrasound focal point is expected to be observed using 1-D CMUT arrays that are driven by focusing electronics.

In order to obtain stated objectives, several microfabrication experiments should be implemented. Most critical microfabrication process is direct wafer bonding. Silicon dioxide-to-diamond, silicon dioxide-to-silicon dioxide, diamond on PECVD (Plasma enhanced chemical vapor deposition) oxide-to-silicon dioxide, (HTO) diamond on HTO (High temperature oxide) oxide-to-silicon dioxide wafer bonding experiments have been performed and results are stated.

CHAPTER 2

HISTORICAL BACKGROUND OF CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS (CMUT)

2.1 Introduction to CMUTs

Capacitive micromachined ultrasonic transducers (CMUTs) with high performance and well characterization were reported as a novel type of ultrasonic transducers developed in Ginzton Laboratory in 1996 [14]. This new type of ultrasonic transducer was designed to operate in air at very high frequencies (11 MHz) which is compatible with alternative piezoelectric transducers. This design had circular silicon nitride membranes and evaporated gold electrode on top of the membranes in order to be excited by driven voltages. It was potentially shown that this design could emit and detect 11 MHz ultrasonic signals.

Further analysis on CMUTs were done with using several measurement techniques. An optical interferometer was used to observe membrane displacement of CMUT cells[15]. It was shown that average membrane displacement of CMUT cells was 126 Å/V at 16 V peak to peak RF voltage. Impedance analysis was also used to measure electrical impedance of CMUT device under 40 V bias voltage. Another test system was obtained with using 'pitch-catch' system. Two identical CMUTs were used to emit and receive ultrasonic waves.

Ultrasound waves can propagate in solid and fluid mediums. First CMUTs operating in water were reported [16]. CMUT devices were excited at 4 , 6, and 8 MHz signals in water with 4 cycles 16 V tone bursts. Besides, it was potentially shown that CMUT could work in high temperature environments with the low device cost production.

Air coupled transmission of glass was potentially observed and it was indicated that air cou-

pled transmission through steel of ultrasonic waves could be possible [17]. 0.95 mm glass slide was used and located 1 cm away from surface of the transducer. For the measurements, 20 cycle of 16 V burst signal was applied to the emitter and receiver transducers with 30 V bias voltage.

First order analysis, mechanical impedance calculation of membrane and equivalent circuit analysis were reported [18]. Spring softening effect, collapse and snap-back formations of membrane were also potentially calculated and spring softening effect was experimentally tested. In addition to that, air coupled transmission through aluminum of ultrasonic waves was presented with transducer excited at 2.3 MHz in air.

2.1.1 Theoretical Development of CMUTs

The effects of the crosstalk were not contained by the equivalent circuit model of CMUTs that were used for the theoretical analysis. Finite element analysis for immersion of CMUTs were done using ANSYS commercial software in order to obtain the simulation results of crosstalk effect [19]. One transmitter and two receiver CMUT cells were simulated with 6 μm separation on a single silicon wafer in order to observe crosstalk effects. The transmitter cell was actuated and the possible effect was captured from receiver cells. The simulation results showed that the pressure obtained on receiver cells is caused by crosstalk effect. Three possible solutions were applied to the design and simulations. The first solution was decreasing the silicon wafer thickness in order to eliminate crosstalk effect. If the silicon substrate is thick, Lamb wave generates more energy into the fluid medium due to the changes of its critical angle. The reason is, its velocity's in substrate being proportional to the wafer thickness. The other solution was creating trenches between the array elements. However, simulation results showed that trench had no effect on crosstalk reduction. The final solution was building 50 μm width polymer wall between the elements. The analysis of this approach showed that the crosstalk effect was increased at some height of the wall. But, further increase on the height of the wall brought the reduction on the crosstalk effect. Optimal design might be obtained with precise simulations.

Electromechanical coupling coefficient is a crucial value of the analysis both for piezoelectric and capacitive ultrasonic transducers. This coefficient is the ratio of total mechanical energy delivered to a load to the total energy stored in the device. This coupling effect was calculated

and simulated with using parallel plate approximation and ANSYS simulation tool [20]. Both analysis showed that electromechanical coupling coefficient reaches to the maximum value which is unity when the collapse occurs and it is not affected by series and parallel parasitic capacitances of the device. Besides, it was shown that radius of the electrode which was set to the half of the membrane radius was an optimal length for collapse voltage value. Further increase on electrode radius does not affect significantly collapse voltage value. Just the parasitic capacitances will be affected. On the other hand, it was potentially stated that adjusting the series capacitances, it becomes possible to obtain a device without collapse event. A transducer which had approximately 4900 membranes, 55 μm membrane radius, 30 μm electrode radius, 0.9 μm air gap, 0.85 μm membrane thickness was fabricated for actual testing. 0.85 electromechanical coupling coefficient was observed close to the collapse voltage.

While the fabrication techniques were developed, new operation regimes of CMUTs were also raised. Conventionally, CMUT cells were excited at values lower than the collapse voltage. The reported new operation regime of CMUTs required higher voltage level than the conventional range [21]. Firstly, bias voltage higher than the collapse limit was applied to the CMUT membranes. Secondly, applied voltage was reduced between the collapse and snapback levels while CMUT membranes remained collapsed. Finally, AC voltage was superimposed on the DC bias voltage while keeping total voltage between the collapse and snapback limits. This was one of the new operation regime of CMUT devices and it is shown in Figure 2.1. This operation approach was simulated using ANSYS tool in order to compare with conventional CMUT behavior. The simulation results indicated that electromechanical coupling coefficient was higher than the conventional CMUT operation. Besides, this mode of operation allows the CMUT to operate at higher frequencies due to smaller portion of vibrating membrane.

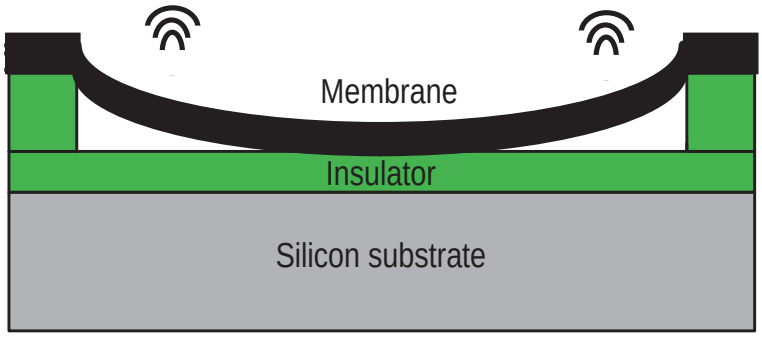

Figure 2.1: Collapse operation regime of CMUT devices [21]

Lamb waves have been considered as being one of the reason for crosstalk effect. But, these waves can be used for main carriers of energy. Capacitive micromachined ultrasonic Lamb wave transducers were fabricated and characterized [22]. This CMUT design had rectangular membranes to emit and receive Lamb waves from the bulk silicon. CMUT equivalent circuit model has been developed for circular membranes and it has not been focused on developing for other shapes of membrane structures. This time, the circuit model was proposed for rectangular membranes keeping the attention to the resistance of membrane. Finite element model simulations was done and the number of 15 emitter and receiver 77 μm x 1 cm rectangular membrane structures were fabricated. Generated Lamb waves from emitters were captured by receiver membranes located 7.8 mm away. The device were operated at 2.1 MHz and it was characterized by using S parameters and laser vibrometer measurements. Insertion loss was stated 20 dB at 2.1 MHz.

High power transmission approach of CMUTs was reported as a new style of the operation regime [23]. Both collapse and snapback operations were considered to perform at high power transmission regime. The membrane was collapsed to the substrate higher than the application of collapse voltage and released under the snapback voltage. This operation regime supports higher acoustic output pressure than the conventional operation mode. The simulations were done using ANSYS and LS-DYNA software tools. Electrode parameters (radius, thickness, position) were changed under the specific collapse and snapback voltages to find the optimum values. The result of the simulations indicated that when the electrode radius was set to a value greater than 60% of membrane radius, the displacement of membrane was enhanced per volt. 2-D CMUT array was used for transmit experiment under the hydrophone setup.

Surface acoustic output pressure of 2-D CMUT was measured 0.47 MPa and 1.04 MPa in the conventional and collapse-snapback mode, respectively. Therefore, this new operation mode provided better acoustic output pressure for CMUT technology.

Static and dynamic models that have been used so far were generated for conventional operation mode of CMUTs. When higher bias DC voltage than the collapse voltage limit is applied, the CMUT membrane goes toward to substrate and the center of membrane can not move under the AC voltage excitation. This contact mode analysis were done using the LS-DYNA software tool available in market [24]. The simulations and experiment analysis were implemented using hexagonal CMUT membranes that increased the active area against the circular structures. The optical interferometer was used in experimental setup in order to compare simulation and actual results. Conventional and collapse modes were measured in oil medium under 130 V and 160 V bias voltages, respectively. It was shown that measurement results were well fitted with simulation results. This model can be used for analyzing the CMUT response when membranes are in contact with substrate material.

Collapse operation mode of CMUT was experimentally characterized and compared with conventional operation mode [25]. A 205 μm x 205 μm 2-D CMUT was manufactured and used for the experimental test. Optical measurement with a laser interferometer, pulse-echo test in vegetable oil medium and impedance measurement in air with impedance analyzer were performed for experimental characterization. It was experimentally shown that the efficiency of collapse operation mode was greater than the conventional operation mode. For the reason that CMUT device produced more acoustic output power as a emitter and had a improved sensitivity as a receiver in collapse mode operation. Beside, center frequency of CMUT device could be changed by adjusting the DC bias voltage. 20 MHz to 28 MHz center frequencies were obtained changing the DC bias voltage of collapsed transducer in oil measurements. In conventional mode, the frequency was measured 10 MHz. 590 kPa and and 370 kPa surface output pressure in the excitation of 25 V unipolar pulse was obtained for collapse and conventional mode operations, respectively.

Crosstalk effect is required to be considered especially in medical imaging and high intensity focused ultrasound treatment (HIFU) in medicine. Crosstalk couples the elements of the transducers and reduces the performance of the device. Crosstalk analysis with finite element model (FEM) and experimental measurements were performed using 1-D CMUT array con-

sidering conventional and collapse mode operations [26]. The FEM analysis were achieved with LS-DYNA software tool and 1-D CMUT array with 64 elements was used to obtain experimental measurements. 41 unit of 64 elements were actively excited in the actual test. The transmitter was the center element and remaining 40 elements were used for receiving. The measurement was performed in the soybean oil and membrane displacements were captured optically with laser interferometer. It was shown that collapse mode had the important advantage over the conventional mode operation due to shifting of center frequency to higher values that reduces the crosstalk effect. On the other hand, the polidimethylsiloxane (PDMS) coating on CMUT elements was examined for the crosstalk effect. It was found that PDMS material did not have any significant reduction effect on crosstalk between CMUT elements.

Fill factor is one of the crucial parameter for CMUT devices. It affects the total output pressure of the emitter and the sensitivity of the receiver transducers. High fill factor is usually required for imaging and therapeutic ultrasound applications. Rectangular CMUT membranes with high fill factor were reported by using wafer bonding approach [27]. It was indicated that this factor depended on the shape of the membrane structure, cell spacing and the aspect ratio of the rectangular cavities. Circular, square, hexagon, rectangle and tent membrane shapes were arranged from low to high fill factor. Some membrane shapes are shown in Figure 2.2. In the measurements, it is shown that small cell spacing caused undesirable effects on adjacent cells. FEM simulations were needed to obtain the cell locations with minimum spacing. Continuous wave (CW) measurement was done in immersion and It was concluded that rectangular shape CMUT membranes could have better fill factor over circular cells but it was not suitable for CW operation due to the emission of low output pressures.

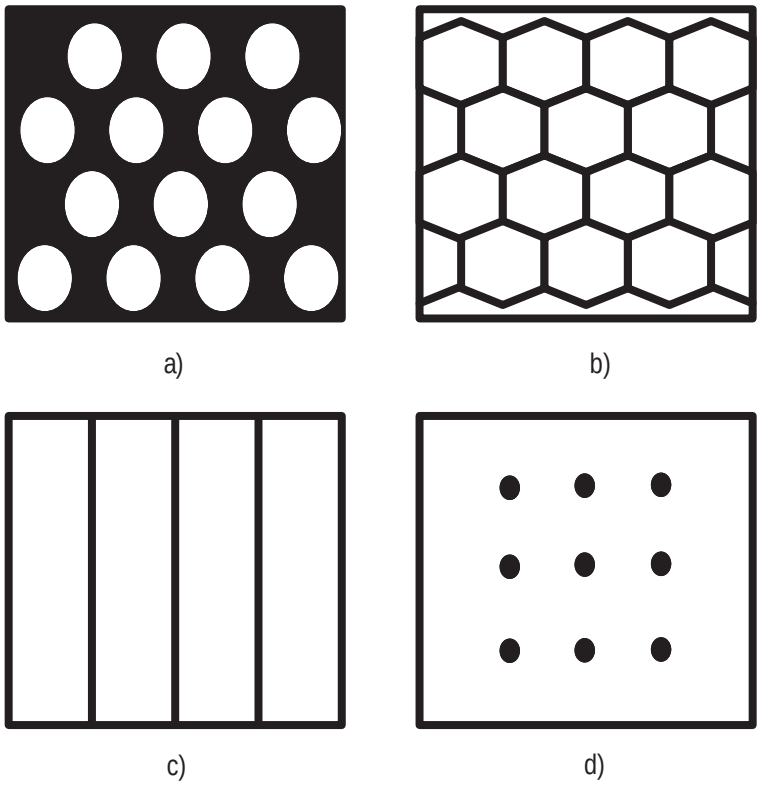

Figure 2.2: a) Circular membranes, b) Hexagon membranes, c) Regtangle membranes, d) Tent membranes [27]

Performance of CMUT devices can be improved with optimizing the membrane shapes and geometries. Piston shape membranes were reported and compared with conventional CMUT structures [28]. Piston CMUT structures had better sensitivity, fractional bandwidth and output pressures over the conventional CMUT devices. The most important difference from conventional CMUT was the suspended mass inside the cavity attached to membrane material as shown in Figure 2.3. Because of that, the fabrication steps were more complex than standard CMUT design. But there were no yield reductions. 8.25 mV/kPa and 4.23 mV/kPa of perception sensitivities were measured for piston and conventional CMUTs, respectively. 5.75 kPa/VAC at 55 DC voltage was the output pressure of the piston CMUT. On the other hand, conventional CMUT had 3.15 kPa/VAC of output pressure at 40 DC voltage. Piston CMUT structure had the better performance characteristics over standard CMUT devices.

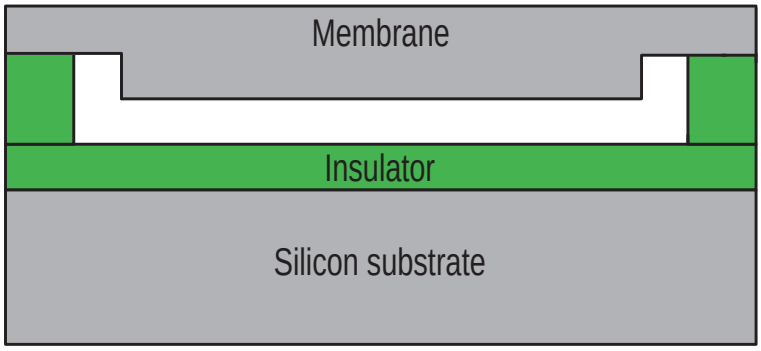

Figure 2.3: The basic structure of piston shape membrane CMUT [28]

2.1.2 Ultrasound Imaging with CMUT Devices

3-D ultrasound imaging is an important area for medical solutions. 2-D CMUT array that was potentially suitable for ultrasound imaging was fabricated and experimentally tested [29]. 400 μm x 400 μm 2-D CMUT array generated 16.4 kPa/V output pressure when excited 3 MHz signal. Fractional bandwidth was obtained more than 100% that enabled the usage of transducer for ultrasound imaging systems.

1-D immersion CMUT characterization was done to show that it was suitable for ultrasound imaging [30]. 1-D CMUT array was experimentally tested at 3 MHz under 35 V bias voltage. The fractional bandwidth was more than 100% and it produced 5 kPa/V output pressure at the surface of the transducer array. On the other hand, the important disturbances considered as the source of acoustic crosstalk were discussed and suggested some improvement in order to eliminate cross coupling effect. There are two sources of the acoustic crosstalk which are Stoneley and Lamb waves. Lamb wave propagates inside the silicon bulk and carries the energy that couples to the CMUT elements. It was potentially shown that deep trench isolation among the CMUT array elements and reducing the thickness of the silicon bulk decreased the crosstalk effects coming from Lamb wave. Stoneley wave propagates at the interface between the solid and fluid mediums. This wave is also caused by the crosstalk effect between the CMUT elements. This coupling effect was decreased with using a lossy medium between the adjacent CMUT elements. Also, lossy mediums located at the edges of CMUT device could help to eliminate Stoneley waves along the edges.

Ultrasound imaging is significant area for medical diagnosis and treatments. 64 and 128 elements 1-D CMUT arrays were fabricated and experimentally tested to show the potential feasibility of CMUTs for ultrasound imaging [31]. Besides, the crosstalk effect between the array elements was examined on image quality and two artifacts were detected.

Magnetic resonance imaging (MRI) and computed tomography (CT) is used to capture of images in medical fields. Hence, the scanning rates of the MRI and CT are not fast enough in order to generate real time imaging. The implementation of 2-D CMUT arrays for real-time 3-D imaging was potentially presented [32]. The volumetric images were captured by using 8 x 16 elements of 2-D CMUT array. 128 x 128 elements of 2-D CMUT arrays were fabricated, but 8 x 16 elements were actively used due to the limitations on number of channels of data acquisition system. 4 x 4 elements in the middle were used to transmit the ultrasonic waves and remaining elements were ready to capture echo signals. RF beamforming and synthetic phase array methods were used to perform image constructions. In the fabrication process, it was proposed to use flip chip bonding technique in order to connect the CMUT structure with the electronic circuit. CMUT device and electronics can be fabricated with different wafers which allow the high temperature CMUT process with high yield and reduced turn-around time. Although it was planned to use integrated circuit design for 2-D CMUT arrays, PCB design was initially preferred to obtain real-time 3-D imaging. 20 V bias voltage and 15 V rectangular pulse signal excited the 2-D CMUT arrays in order to generate ultrasonic waves and capture the echo signals.

The circular CMUT array was designed and fabricated for ultrasound imaging systems. [33]. Trapezoid elements were used in order to increase the active area and transduction efficiency. 64 trapezoid elements were brought together to form annular CMUT array. 13.5 MHz resonance frequency was measured in air using impedance analyzer. Pulse-echo measurement in oil showed that the annular CMUT array had 135% fractional bandwidth in the 5-26 MHz range. Under 40 V bias voltage, surface output pressures were 16.1 kPa/V and 26.7 kPa/V at 10 MHz and 20 MHz, respectively. It was potentially shown that the annular CMUT array was suitable for medical imaging systems.

Intravascular and intracardiac ultrasound applications are crucial for monitoring the operations in heart and veins. CMUT ring array can be potentially used for intravascular and intracardiac ultrasound applications for medical imaging [34]. Custom integrated circuit con-

trolled CMUT ring array was manufactured with 64 elements as shown in Figure 2.4. Each element had size of 100 μm x 100 μm. Experimental results shown that CMUT ring arrays are suitable to generate acceptable images. Besides, collapse and conventional mode of operations can be applied for either better penetration or resolution of captured image profiles.

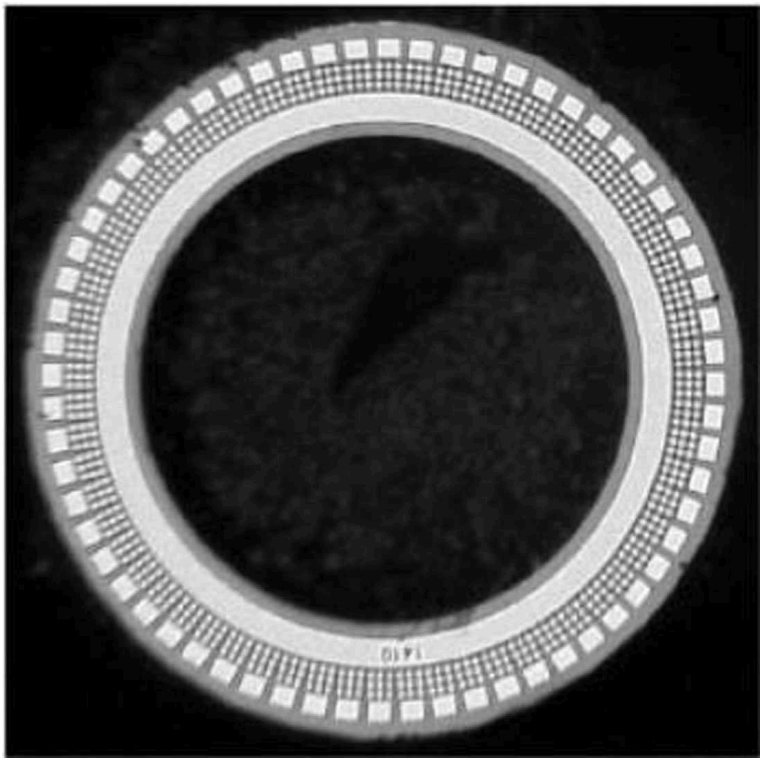

Figure 2.4: 64 elements CMUT ring array [34]

Front-end electronics were integrated to 2-D CMUT arrays using flip chip bonding technique for 3-D volumetric ultrasound imaging [35]. Matching 2-D CMUT arrays with the IC electronics need sensitive approaches and efforts due to small array structures and relatively high parasitic capacitances introduced by connections. IC electronics had 25 V pulsers and transimpedance preamplifiers that connected each array elements of CMUT device. CMUT arrays were fabricated with about 100% yield and a range of the center frequencies were indicated from 2.6 MHz to 5.1 MHz. 3-D ultrasound image was captured using 2-D 16 x 16 elements CMUT device excited by IC electronics. Implementation CMUT arrays with IC electronics brought lower cost, high bandwidth and good sensitivity to volumetric ultrasound imaging.

Intracardiac ultrasound imaging was reported by using 1-D CMUT array integrated with cus-

tom design electronics [36]. 1.73 mm x 1.27 mm 1-D CMUT array was fabricated and covered by PDMS material for electrical isolation. Custom designed electronics was integrated using flip chip approach with 100% yield. Pulse echo measurement in water was done at 9.2 MHz center frequency and obtained 96% fractional bandwidth. 1-D CMUT device was excited to capture the images from a beating rabbit heart using a ultrasound imaging system. The results showed that high frequency transducers could be potentially produced for intracardiac and intravascular imaging applications.

Flip chip bonded 16 x 16 2-D CMUT array with IC electronics was implemented for 3-D ultrasound imaging [37]. IC electronics were used to both transmit and receive operations. It had an 8-bit shift register, a one shot circuit, a comparator and 25 V pulser blocks. The management of the IC electronics was done by field- programmable gate array (FPGA) clocked at 100 MHz signal. Focused ultrasound beams could be generated using the this circuit implementation. 224 elements of CMUT device were used to transmitter and remains were receiver. 2-D and 3-D images of wire and latex heart were obtained with this system.

2-D CMUT array was used to perform 3-D photoacoustic imaging (PAI) [38]. Targeted living tissues are illuminated with laser pulses in order to increase their temperature. Then, thermolesticelastic effect can be a reason for generated acoustic pressure waves which propagates on the surface of targeted tissues. Generated waves were detected by using CMUT devices. 16 x 16 elements of 2-D CMUT with IC electronics were used to create volumetric ultrasound images of transparent fishing lines and polyethylene tubes inside the chicken breast.

2.1.3 High Intensity Focused Ultrasound (HIFU) Applications OF CMUTs

High intensity focused ultrasound (HIFU) is a raising medical application for noninvasive treatments of cancers and tumors. CMUT devices can be considered as suitable technology for HIFU theraphy due to the competitive advantages over dominant piezoelectric technology. Ultrasonic heating of a phantom with CMUT devices was reported [39]. Magnetic resonance imaging (MRI) was used to map the temperature changes. 2.51 mm x 2.32 mm CMUT was excited to heat a phantom with ultrasonic waves. 172 V bias and 250 V AC voltage excitation was applied to CMUT device and it showed 1.3 MPa surface output pressure. it was reported that the phantom was heated 14^oC in 2.5 min with unfocused CMUT device. These experimental results show that CMUT technology is potentially suitable for HIFU therapeutic

applications. Besides, the materials that are used for the microfabrication of CMUT devices can be set to MRI compatibly.

HIFU is one of the therapeutic treatment methods that reduce pain of the patients, medical cost and death rates. The first 8 element concentric ring CMUT array was fabricated and characterized for HIFU applications [40]. Because of the yield issue, 4 elements of the array were used to obtain measurement results. Array simulations showed that 2-3 cm diameter tumor could be potentially destroyed within 1 hour. The gain of the CMUT arrays was calculated 27.4, but 16.6 was obtained. This gain is not suitable to perform HIFU applications. Hence, it was shown that CMUT devices had the robust structure for CW operation in order to destroy tumor or cancer cells.

2.1.4 Microfabrication Technology of CMUTs

The microfabrication of CMUTs has been developed over years. The size of the CMUT cells was a problematic issue due to the duration of the oxide etching. Because cell radius was determined by duration of this etching. Nitride cavity walls and vertical layer for etch-stop technique were used to obtain determined cell sizes instead of time taking oxide etching [41]. Besides, it is potentially introduced that amorphous silicon could be used as a sacrificial layer instead of thermal oxide with better etching selectivity against the nitride membrane. This new fabrication approach brought precise control on resonant frequency of CMUT devices. But, CMUT performance would be lowered due to the nitride layer located between the cavity and negative electrode which reduced strength of applied electric field.

Three CMUT membrane structures were demonstrated and discussed with different sacrificial layers, sealing mechanisms and the effect of the electrode metallization [42]. Silicon nitride and polysilicon materials were used to evaluate membrane structure of CMUT cells. Polysilicon membranes showed the best theoretical results, but nitride membranes served better controllability and reality on fabrication process.

Optimization of the electrode size of CMUTs was done with using theoretical analysis and computer simulations [43]. The basic approach was that the most effective electrostatic force could be applied at the center of the circular membrane structure. The simulations of membrane deflection under different electrode radius was done with using ANSYS software. The

result of the simulations showed that the bandwidth of the CMUT device could be increased by a factor of 2-2.5. The optimum metallization radius of electrode changed between 40 and 50% of the cell membrane radius. Simulations were also run with CMUT devices that had different membrane radius. The same percentage result (that stated)was obtained for different radius of membranes. The badwidth comperison of different radius (r=8 μm and r=20 μm) CMUT membranes is shown in Figure 2.5.

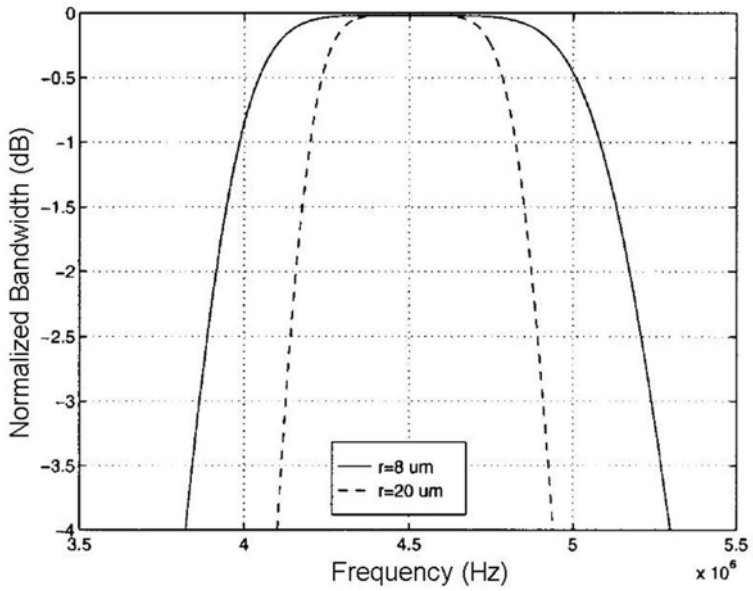

Figure 2.5: The bandwidth comparison of CMUT devices with different membrane radii [43]

The integrated circuit fabrication methods are used to manufacture CMUT devices for air and immersion applications [44]. The most important advantage of this techniques was that CMUT devices could be produced with integrated circuitry with flip-chip bonding. Besides, piezoelectric transducer and fabricated CMUT device were compared theoretically in the aspect of bandwidth and dynamic range. It was potentially shown that CMUT's performance was as good as piezoelectric transducer. If developing fabrication process allowed 500 Å air gap, electric field strength amount the capacitor plates could be much higher without any change on applied bias voltage.

Traditional fabrication technique had some limitations on design and manufacturing of CMUTs. Wafer bonding techniques were brought in the fabrication process of CMUTs [45]. Membrane and cavity formation were separated to different wafers which supports better reliability and

design flexibility. This new method introduced several advantages over traditional fabrication methodology. Firstly, cavity formation became independent of the membrane structure and shape. It was possible to optimize the cavity with shape, size and height without any membrane structure tradeoffs. Secondly, it was possible to change membrane material regardless of cavity style. Traditionally, silicon nitride was widely used as a membrane structure of CMUTs. Silicon nitride was deposited at 800^oC into the reactor on silicon wafer. Electrical and mechanical properties of silicon nitride could not be well controlled. Wafer bonding technology allows to the high resistance silicon for which most of the mechanical and electrical properties are well known can be used as a membrane material. Finally, this advanced fabrication process allows to higher fill factor against to traditional technique. In order to etch the sacrificial layer to form the cavities and membrane, it was required to have holes that enable the wet etching through the sacrificial material. Wafer bonding approach is not needed the etch hole that decreases the active area. For the experimental testing, several designs were produced in order to explore possible problems for new fabrication approach. Electrical and mechanical characterizations were done to obtain the performance behavior of CMUT designs. Interferometer was used to maintain deflection of the CMUT membranes. It was observed that membrane deflections were similar to the wafers obtained from different production runs. Electrical characterization also showed that CMUT devices with improved performance could be produced by using wafer bonding approach. On the other hand, sub MHz CMUT devices had been fabricated and tested for the first time. They were not produced up to now due to the limitations on traditional fabrication technology. In conclusion, wafer bonding technique reduced the fabrication turn-around time with better design and performance of CMUT devices.

Device fabrication and strong electric field applied to the operation of CMUTs were caused by the charging problem in this technology. It was reported that charging problem of CMUTs was solved with using developed PostCMUT process depending on wafer bonding approach [46]. Trapped charges in dielectric materials used in the fabrication of devices can be shown the reason of charging problem. These charges may cause several undesired effects on the operation of CMUT devices. Because, the operation of capacitive transducers heavily depend on electrostatic attraction between the polarized electrodes. Instead of covering hole surface of the substrate under the membrane to prevent possible short between electrodes, the several isolation posts were used to handle that crucial task. These posts have no performance re-

ducing effects on CMUT operations while solving charging problem. Therefore, this was the innovative approach for solving charging problem of CMUT devices. PostCMUT structure is shown in Figure 2.6.

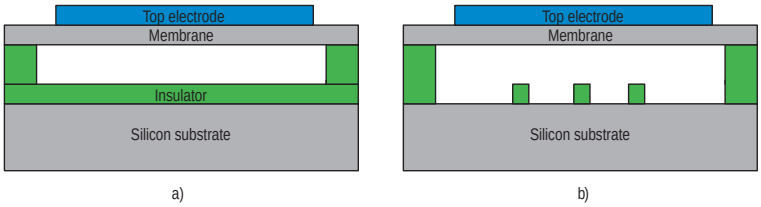

Figure 2.6: a) Conventional CMUT structure, b) PostCMUT structure [46]

Fabrication technologies for CMUTs have been improved significantly. Developed two fabrication processes of CMUTs which are wafer bonding and sacrificial release approaches were reported and compared with several aspects [47].

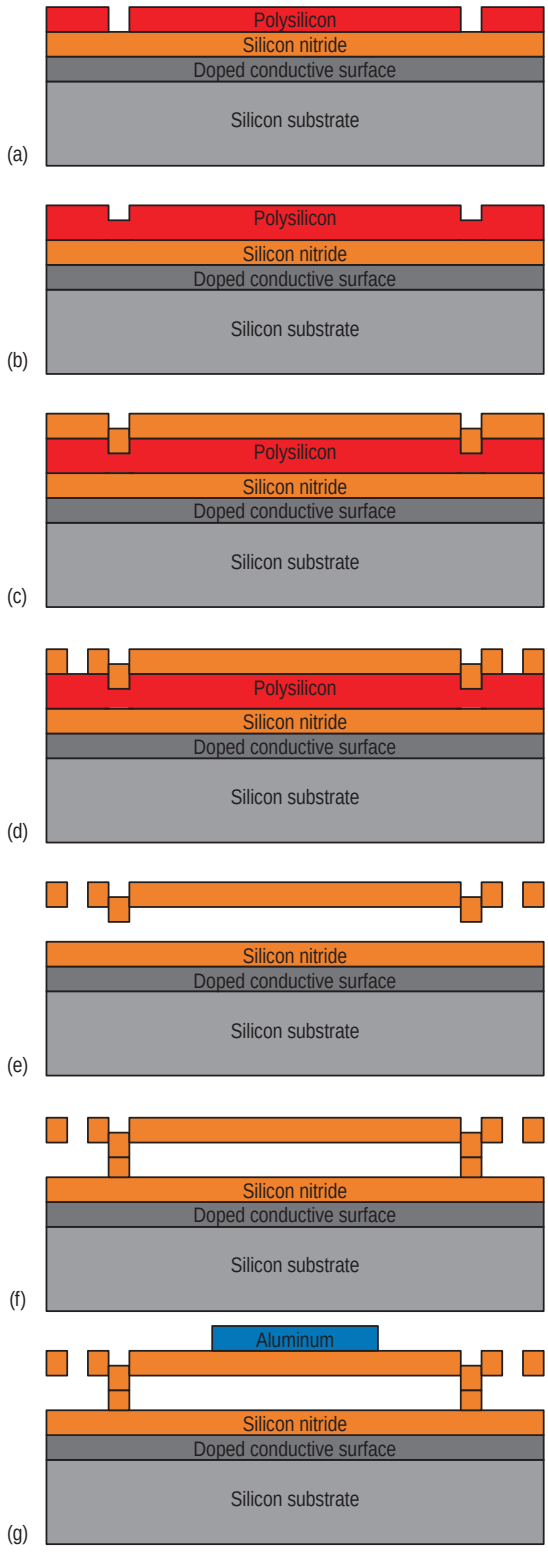

Figure 2.7: Sacrificial release process with silicon nitride membrane [47]. (a) Doping of silicon wafer, deposition of silicon nitride, the first deposition and patterning of polysilicon material for etch channel and membrane formation, (b) the second deposition of polysilicon material to complete etch channel and membrane formation, (c) Deposition of membrane material, (d) Creation of holes for sacrificial material etching, (e) Sacrificial layer etching, (f) Sealing the etch channels, (g) Deposition of top electrode

In sacrificial release process, fabrication steps start with doping the silicon wafer in order to increase the conductivity of its surface. Quality of surface conduction of substrate is one of the most crucial issues. Because it forms the back electrode of CMUT cells. After the doping process, silicon nitride (Si_3Ni_4) is deposited by using low pressure chemical vapor deposition (LPCVD). Deposition of the polysilicon as a sacrificial layer is done and it needs to be patterned to create etch channels for sacrificial layer etching with potassium hydroxide (KOH). When the first deposition of polysilicon layer is patterned with the photolithography using dry etching technique Figure 2.7.a, the second deposition of polysilicon layer is done to complete the formation of etch channels. Later on, polysilicon layer is formed with photolithography and dry etching steps in order to obtain cavities for membrane shape Figure 2.7.b. Deposition of the membrane material which is silicon nitride is the next step of sacrificial release process Figure 2.7.c. The holes which are used for removal of sacrificial material are generated using the dry etching Figure 2.7.d. Next, polysilicon layer that used as a sacrificial layer is etched away by using KOH solution Figure 2.7.e. Third deposition of the silicon nitride is done for sealing the etch channels Figure 2.7.f. For final step, the aluminum is deposited to form the top electrode of the CMUT cell Figure 2.7.g.

Some issues and variations were also reported for sacrificial release fabrication approach [47]. Silicon wafers have been generally used as substrate material. But it is possible to replace it with another material like quartz. However, quartz material as an insulator needs to be covered with a conductive material in order to serve as the back electrode of a CMUT cell. On the other hand, conductive material must be attentively chosen for either high or low temperature processes that will be used for CMUT device production.

Polysilicon is used as a sacrificial layer in order to shape the membrane structure. But this material has high compressive stress. Sacrificial layer etching releases this stress that have a potential to damage the large membranes. Phospho-silicide-glass (PSG) is deposited between the polysilicon and silicon nitride materials as a solution of high compressive stress. This buffer material supports large membranes up to 160 μm diameter [47].

One of the critical problems of sacrificial release process is the membrane sticktion [47]. Remaining water after sacrificial layer etching, is responsible for this sticktion problem. While the water is evaporating inside membrane cavities and channels, capillary force from surface tension pulls the membrane toward the silicon substrate. Membrane must be fabricated with

required thickness that can be done with higher mechanical restoring force than the capillary attraction. Controlling the membrane thickness is another problem during wet etching technique. Sacrificial and membrane materials must be chosen according to their etch rate selectivity of enchant. On the other hand, silicon nitride deposition for sealing the channels also affects the thickness of the membrane material. Thickness of the membrane material should be formed with considering all side effects due to fabrication process steps.

Electronic circuit connection to CMUT devices is a challenging issue due to very small capacitance values of CMUTs [47]. Using cable for connections introduces lots of parasitic capacitances that does not well suit with CMUT arrays. Electronic circuit can be brought close as far as possible to eliminate this parasitic capacitances. Monolithic integration of electronic circuit can be considered as a solution of the problem. Eventhough reduced parasitic capacitances can be obtained, this solution has many limitations and disadvantages. The yield is low due to the complex fabrication steps. This complexity brings the long duration of process and holds the cost high that does not satisfy improved performance. Flip-chip bonding technique not only brings the performance advantages but also decreases the complexity of fabrication process with increased yield. CMUT devices and electronic circuit are fabricated on different wafers, then the wafers are connected with using interconnection process which introduces low capacitance and resistance for electrical connections.

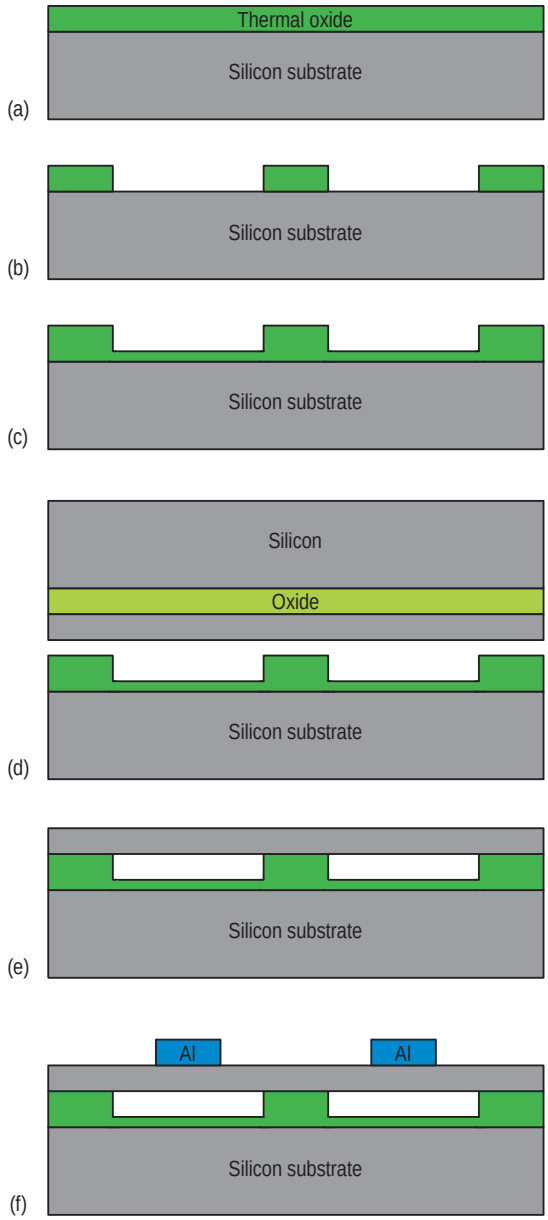

Figure 2.8: Fabrication of the CMUT devices using silicon fusion bonding [47]. (a) Thermal oxide growing on silicon wafer, (b) Etching the thermal oxide to form the CMUT membranes, (c) Thermal oxide grown in order to prevent possible electrical shorts between the substrate and top electrode, (d) Prime and SOI wafer are brought together in vacuum conditions, (e) CMUT device with silicon membrane, (f) Sputtered aluminum electrodes at the top of the CMUT membranes

Fabrication process of CMUTs with silicon fusion bonding was potentially achieved by using silicon as a membrane material [47]. This bonding process has one prime and one silicon-on-insulator (SOI) wafer. Fabrication of the CMUT device starts with the silicon prime wafer. Firstly, thermal silicon dioxide is grown on the surface of silicon wafer at the furnace Figure

2.8.a. Then, thermal dioxide is patterned by using photolithography in order to obtain shape and size of the CMUT membranes Figure 2.8.b. Wet etchant, hydrofluoric acid (HF), or dry etching can be applied to pattern the thermally grown dioxide. The second thermal dioxide is grown on the wafer to avoid the possible electrical shorts between the top electrode and the substrate Figure 2.8.c. Next, surface activated and cleaned silicon and SOI wafers are brought together in vacuum conditions Figure 2.8.d. After successful bonding process, the silicon at the backside of the SOI wafer is etched by wet (KOH or tetra-methyl-ammonium-hydroxide (TMAH) solutions) or dry etching. Remaining oxide layer is also etched away with HF solutions or deep reactive ion etching (DRIE). CMUT device with silicon membrane is shown in Figure 2.8.e. For a final step, aluminum top electrode is sputtered and patterned with photolithography Figure 2.8.f.

Thermal oxidation is used to specify the depth and size of the CMUT membranes. Thickness of the thermal oxidation can be well controlled. Therefore, membrane dimensions can be adjusted to desired size and shape that affect the performance of CMUT operation. Besides, the thickness uniformity all over the wafer is fine with thermal oxidation. 100 mm 20 wafers was thermally oxidized and average uniformity was found 0.64% [47].

Membrane thickness is also controlled regardless of membrane cavity shapes and sizes. This flexibility brings better design approaches. It is possible to choose different membrane and cavity materials that are available at raising MEMS technology. In addition, membrane and cavity materials were produced on different wafers and there is no interaction between them to limit any developments.

Charging problem is a crucial issue for CMUT operations. Silicon dioxide generated on the surface of substrate in the membrane cavity, traps the electrons which affects the normal operation of CMUT device. Isolation post structures [46] can be used to eliminate this charging problem. But wafer bonding approach for CMUT production should be used in order to obtain easy fabrication steps with low cost and efficiency. Fabrication of CMUT devices with wafer bonding technology does not require etch holes and channels. So, missing channels and holes brings the high fill factor. This is an important parameter for performance of CMUT device. Increased active area affects the output pressure for emitter and reduced parasitic capacitances increases the signal to noise ratio of CMUT device's receiver.

Wafer bonding approach brings lots of advantages over sacrificial release process. It is visible

that the number of fabrication steps and turn-around time are reduced, performance, yield and process flexibility are enhanced with wafer bonding.

Developed microfabrication techniques enables high yield ultrasonic CMUT devices that are possible to be used for 3-D real-time imaging [48]. 3-D imaging is an improving area for ultrasonic sensors and it is challenging to design with more than one dimension, large area transducer arrays with piezoelectric technology. With advanced microfabrication technology, 2-D large CMUT arrays can be manufactured for medical real time imaging.

Biocompatibility is one of the most crucial issues of some medical applications using MEMS devices in contact with the living tissues. PDMS and parylene-c coatings for CMUTs were reported and manufactured transducers were characterized [49]. Wafer bonding approach was used to fabricate the transducers with the additional step that inclueded deposition of biocompatible materials. It was shown that resonant frequency was reduced and collapse voltage was increased due to the PDMS and parylene-c coating. The result of the experiments indicated that parylene coated transducers had the potential to used against the skin applications but, it required more developments for imaging inside the body.

Electrical connection of 2-D CMUT elements with driven electronics is a difficult issue for transducer design and its microfabrication. 2-D CMUT device with trench-isolated through wafer interconnections was designed, fabricated and characterized [50]. The IC electronics were integrated with flip-chip bonding approach to the CMUT elements. It was reported that this technique had significant advantages over through wafer vias interconnection method. Firstly, the thickness of the silicon wafer could be optimized for device performance. Secondly, series resistance and electrical cross coupling between the elements is reduced. These advantages made this method attractive for 2-D CMUT device design and fabrication.

Isolation post technique was used to solve the dielectric charging problem in CMUT devices. Reliability of CMUT with isolation post (PostCMUT) and operation beyond the collapse voltage were tested in air and immersion [51]. Conventional CMUT cells have insulation layer covered at the bottom of the membrane cavity. Beyond the collapse voltage, insulation layer is charged and operation voltage level is changed. This undesired effect has been eliminated with using isolation posts. In air measurements, PostCMUT and conventional one had the same resonance frequency in pre-contact region. In contact regime, conventional CMUT had higher resonance frequency than PostCMUT due to the effects of spring softening

and membrane resonance. During immersion measurements, PostCMUT had 6.25 kPa/VAC transmission efficiency and 8.25 mV/kPa reception sensitivity, conventional CMUT had 16 kPa/VAC transmission efficiency and 25 mV/kPa perception sensitivity. Therefore, conventional CMUT showed better transmission and perception efficiencies in the contact mode. But fractional bandwidth of PostCMUT was larger in the post contact regime.

Through wafer via trench isolated fabrication technique was demonstrated by using wafer bonding approach with a supporting frame for 2-D CMUT arrays [52]. 2-D CMUT arrays with 16 x 16 elements were fabricated with 100% yield. This technique solved the yield problem of through wafer via fabrication and increased the reliability of CMUT devices. Another advantage of this method could be small series resistances, low parasitic capacitances and simplified fabrication steps. Fabricated 2-D CMUT arrays were characterized in air and immersion. The average resistance of the contact vias was found 6.6 Ω. It was a relatively small resistance, if it was compared with the impedance of CMUT arrays (kΩ range). Parasitic capacitance was obtained about 0.22 pF range. It was acceptable when compared to the 2 pF CMUT device capacitance. During immersion measurements, the maximum surface output pressure was measured 2.9 MPa at 80 DC voltage. The center frequency and fractional bandwidth were 7.6 MHz and 95%, respectively. Chip to chip bonded with IC electronics was demonstrated and 3-D imaging of straight robes was obtained successfully.

2.1.5 Development of Other Application Areas of CMUTs

The chemical sensor design and implementation with CMUT arrays were reported as a prototype [53]. Conventional CMUT arrays designed for ultrasonic imaging and medical application have potential to be used for mass sensing devices. This prototype was operated at 6 MHz resonating frequency with an oscillator circuit. The surface of the CMUT cells were coated with a material that could detect different types of chemicals. The frequency of the oscillation highly depends on the mass loading on the membrane. The frequency shift was measured in order to detect chemical types and its concentrations.

Highly directional sound was generated with 50 kHz CMUT devices that were fabricated with 8 cm in diameter [54]. Directional sound can be received, if emitter and receiver are in same directional axis. This can be used for office places to transfer information without any disturbances. FEM was used to adjust the membrane thickness and cavity dimensions in

order to obtain resonance frequencies of fabricated CMUTs. On the other hand, it is shown that membranes with large dimensions can be fabricated with using wafer bonding approach for low frequency applications. 135 dB surface output pressure was measured in the excitation of 380 DC and 200 V peak to peak AC voltages. As a result, CMUT devices can be designed for high voltage levels in order to obtain high output pressures and low frequency operations.

2.2 Diamond Material and Diamond Membrane CMUTs

2.2.1 Properties of Diamond and Synthetic Diamond Films

Diamond is the hardest material that have face centered cubic crystal structure composed of carbon atoms. The carbon atoms are arranged in such a proper way that they build the diamond lattice structure. The strength of the covalent bond between carbon atoms gives to diamond the natural hardness and stability. Due to the hardness of the diamond material, it is usually used in cutting and polishing applications in industry.

Diamond provides significant physical, chemical and mechanical properties. High thermal conductivity, high electrical resistivity, hardness, transparency, low friction and thermal expansion coefficient, biocompatibility are the well known properties of diamond material. Typical mechanical properties are given in Table 2.1.

Table 2.1: Typical Mechanical Properties of Diamond

Density, g/cm^3	3.52
Young's modulus, GPa	910-1250
Poisson ratio	0.10-0.29
Compression strenght, GPa	8.68-16.53
Vickers hardness, GPa	60-100
Thermal Conductivity (25^oC), W/m-^oC	600-1000

Diamond material can be naturally found around the volcanic formations. Since, this material is formed inside the earth under high temperature and pressures, and then it is brought to surface by mining or volcanic activities. On the other hand, synthetic diamond can be made using several fabrication methods. High temperature, chemical and physical vapour deposition (CVD and PVD) methods are used to produce diamond materials and thin films. Diamond-

like carbon, single crystal, microcrystalline, nanocrystalline and ultrananocrystalline diamonds are different types of thin films available in the market.

Diamond-like carbon (DLC) films have the unique property combinations from natural diamond and graphite. These carbon films are amorphous and not crystalline like diamond structure [55]. Moreover they also have hardness and transparency properties. The application areas of DLC films can be basically classified as; biomedical coatings, MEMS devices and magnetic storage disks.

Carbon element and an excitation source are required for the deposition of DLC films. The different types of energy and carbon element sources can be used for depositions. There are several deposition methods to create DLC films. Ion beam was the first method used to deposit DLC films [56]. The beam containing approximately 100 eV energy was applied to carbon ions to perform thin DLC film with sp^3 bonding between carbon atoms. Quality of this process depends on individual energy absorbed by each carbon ions. The best performance was maintained when each carbon ions had 100 eV energy. The other deposition method was mass selected ion beam that had better controllability of deposition and energies corresponding each carbon ions. This method uses the magnetic filter to accelerate carbon ions. Then, electrostatic lens is applied to adjust desired ion energies. Another method that is generally found in industrial DLC deposition processes is sputtering. The graphite electrode is bombarded with plasma in order to obtain sp^3 bonding between carbon atoms. The magnets are also can be used to increase the plasma quality for better deposition rate. Plasma enhanced chemical vapour deposition (PECVD) is the popular method for DLC film depositions. Plasma can be generated using RF power source between the electrodes. The quality and deposition rate depend on the type of the gaseous used during PECVD. One type of gas can serve high deposition rate but hardness of deposited DLC film might have low quality. Pulse laser deposition and cathodic arc are other methods for DLC film depositions.

DLC films and diamond properties are compared in Table 2.2.

DLC films generally do not exhibit similar properties of diamond material as given in Table 2.2. Microcrystalline, nanocrystalline and ultrananocrystalline diamond films have better diamond-like features [58]. Therefore, these types of diamond films are preferred for MEMS device fabrications.

Table 2.2: Properties of DLC films and diamond material[57]

Property	DLC	Diamond
sp^3 fraction, %	>80	100
Electrical resistivity, Ω cm	$3x10^{11}$	10^{16}
Hardness, GPa	120	120
Young's Modulus, GPa	650	910-1250

Single crystal diamond (SCD) films are manufactured by CVD processes that eliminate possible impurities in the film structure. It is possible to obtain SCD plates for industrial applications. The main problem is the thickness and size of the SCD films. It was reported that the thickness of the SCD films highly depended on the orientation of the film and was limited to tens of microns [59]. On the other hand, the production steps should be carefully managed for smooth polycrystalline growth. 7 mm x 8 mm x 5 mm SCD was fabricated using microwave plasma chemical vapour deposition (MPCVD) [60]. The manufactured SCD plate is shown in Figure 2.9.

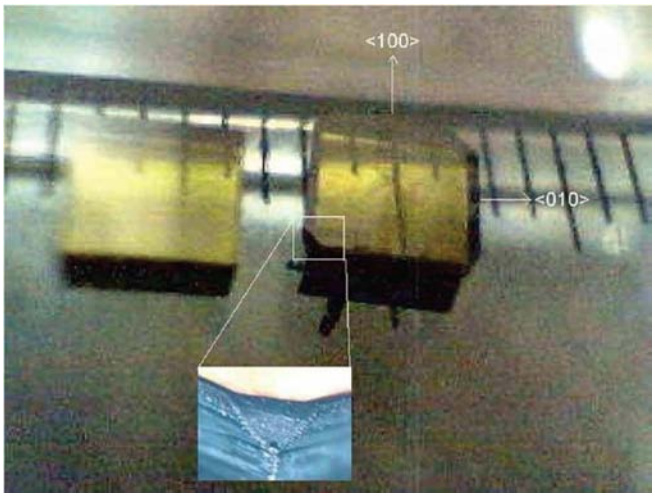

Figure 2.9: Fabricated 7 mm x 8 mm x 5 mm SCD plate [60]

The desired thickness and size of SCD structures are difficult to obtain for industrial and research applications.

Microcrystalline (MCD), nanocrystalline (NCD) and ultrananocrystalline (UNCD) diamonds are the other types of diamond films that can be deposited with using CVD systems. It was

reported that 1 to 3 μm thickness of each types of films were produced with MPCVD method and Young's modulus, burst pressure of the films were described for comparison [61]. These films were classified according to their grain sizes on the surfaces. Grain size of several micrometers was assigned as MCD films, ten to hundred nanometers and several nanometers were assigned as NCD and UNCD films, respectively.

Deposition parameters for these films are given in Table 2.3 [61].

Table 2.3: Deposition Parameters [61]

Parameter	Microcrystalline	Nanocrystalline	Ultrananocrystalline
Pressure, kPa	0.9-2.0	2.7-4.4	16
Power, watts	700	700	1200
Temperature, ^oC	450-550	625-725	<650
Time, h	40	5-20	5-6
H_2 flow, sccm	200	200	1-2
CH_4 flow, sccm	3	3	1
CO_2 flow, sccm	8	8	0
Ar flow, sccm	0	0	100

Young's modulus and burst pressure measurement results are shown in Table 2.4 [61].

Table 2.4: Young's modulus and burst pressures of different diamond film types [61]

Film Types	Young's Modulus, GPa	Thickness, μm	Burst Pressure, kPa	Thickness, μm
UNCD	910	1.23	545	0.97
NCD	710	1.20	200	1.28
MCD	741	2.5	2.34	1.34

Ultrananocrystalline diamond film have the best Young's modulus and burst pressure values. It means that UNCD film have better stress parameters and quality of hardness. Additionally, deposition time and temperature are also at moderate level among the other film types.

Grain size and surface roughness values were described and compared for these film types [58]. It was reported that UNCD films had a good potential on developing high performance MEMS devices. Comparison of grain size and surface roughness values are given in Table 2.5 [58].

Table 2.5: Grain size and surface roughness values of diamond films. [58]

Parameter	Microcrystalline	Nanocrystalline	Ultrananocrystalline
Grain size, nm	500-10000	50-100	2-5
Surface roughness, nm	400-1000	50-100	20-40

All of these comparisons between the diamond films show that UNCD films are the best choice for MEMS devices due to good surface roughness, high Young's modulus, high burst pressure, chemical inertness and compatibility with MEMS fabrication process.

2.2.2 Diamond MEMS structures and Diamond Membrane CMUTs

CVD deposited diamond thin films are used to design and fabricate MEMS devices. It was reported that high temperature and high bandwidth pressure sensors were fabricated with diamond diaphragm [62]. Diamond film deposited by using microwave plasma assisted deposition system and crucial resistivity value of the membrane was controlled during doping step. Fabricated pressure sensor could be potentially operated at 680^oC of temperature conditions. 200 KHz resonant frequency was achieved and burst pressure limit was 46 psi for this sensor.

Diamond film was deposited to fabricate diamond bridge and cantilever beam using surface micromachining for the first time [63]. Selective deposition of diamond film on silicon dioxide/silicon substrate was used to build the MEMS structures. The surface of the silicon dioxide was damaged by methanol containing diamond particles. Therefore, damaged areas were suitable to grow thin diamond film. The first diamond bridge and cantilever beam were fabricated and shown in Figure 2.10[63].

Diamond bonding to the materials used in microfabrication technology is another research area. it is clear that diamond films can be used as structural materials to increase the performance and robustness of MEMS devices. it was reported that highly oriented diamond (HOD) was bonded to silicon wafer in ultra high vacuum (UHV) and under 32 MPa pressure level [64]. The roughness of the HOD film was less than 3 nm (RMS value) and silicon wafer were well polished to obtain smooth contact surfaces for bonding. Hence, the diamond and silicon pieces were small, it was possible to apply 32 MPa at 1150^oC for bonding and resulted some cracks on diamond material (achieved bonding area 100%). Therefore, full wafer bonding

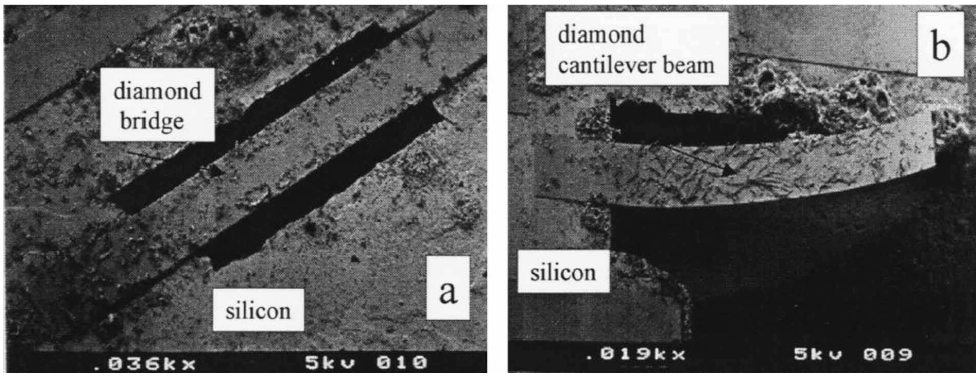

Figure 2.10: a) Fabricated diamond bridge, b) and cantilever beam [63]

approach may have problems on required high amount of pressure level that is proportional to bonding area.

Diamond on insulator (DOI) wafer with UNCD structure was bonded to thermal oxide grown silicon wafer with plasma activated direct bonding [65]. Direct bonding at low temperatures requires high vacuum conditions or plasma activation. Plasma activation was applied to silicon dioxide deposited on DOI wafers. Bonding operation was performed at 550^{o}C, relatively lower temperature condition considering mechanical properties of related materials. This improvement brought new aspect to MEMS devices and transducers having membrane structures. Therefore, diamond can be used as membrane material of CMUTs to improve the performance and reliability.

CHAPTER 3

THEORY AND DESIGN OF THE CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS (CMUT)

3.0.3 Introduction

CMUTs are consisted of membranes that are similar to parallel plate capacitors having a vacuum gap between the conductive plates (electrodes). The typical membrane of CMUTs is shown in Figure 3.1. The basic operation principle of CMUTs depend on the electrostatic attractive force (Coulomb) between the charged parallel plates. One of the electrodes is designed as relatively moveable structure to the other electrode. Therefore, electrostatic force will cause the displacement on the moveable electrode structure. Mechanical restoring force of the membrane acts as a spring and shows an opposite force to the electrostatic attraction. When an alternating voltage is applied to parallel electrodes, it will generate an acoustical wave to the medium which means movable plate's being contacted. Electrostatic force, generated pressure and membrane displacement can be calculated. Hence, analysis of the immersion operation were not quite easy while the membrane structure is under pressure on all sides. Finite element models are used to analyze the complex motion of CMUT membrane.

CMUTs can be used as transmitter and receiver devices. The acoustical waves are generated to the medium when CMUTs are used as transmitter and acoustical waves are sensed when they are used as receiver. For proper operations, DC bias voltage are required to be applied to the membranes of CMUTs. This bias voltage also manages the mode of the operations of CMUT devices.

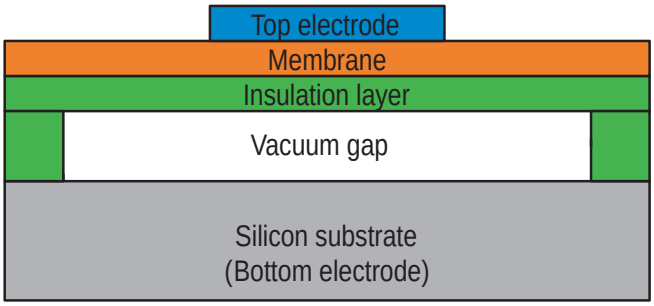

Figure 3.1: Typical membrane structure

3.0.4 Principle of Operation

Lumped electro-mechanical model of CMUT element is shown in Figure 3.2 [14]. Calculations was done considering some assumptions that stated below:

1) Restoring force of membrane is considered as a linear function of displacement.

2) All fringing field is ignored.

3) Assumed CMUT is operated in vacuum and there is no load on membrane.

4) All electrodes is assumed as a perfect conductor.

The force exposed on the mass is supplied by spring and capacitor forces. This equality is given in Equation 3.1.

$$F_{spring} + F_{capacitor} = F_{mass} \tag{3.1}$$

Introduced force value by the capacitor can be found considering the potential energy stored in capacitor according to position of the mass.

$$F_{capacitor} = -\frac{d}{dx}\left(\frac{1}{2}CV^2\right) = -\frac{1}{2}V^2\left[\frac{d}{dx}\left(\frac{\xi S}{d_o - x}\right)\right] = \frac{\xi S V^2}{2(d_o - x)^2} \tag{3.2}$$

'C' is the capacitance, 'V' is the applied voltage between electrodes, 'ξ' is the electrical

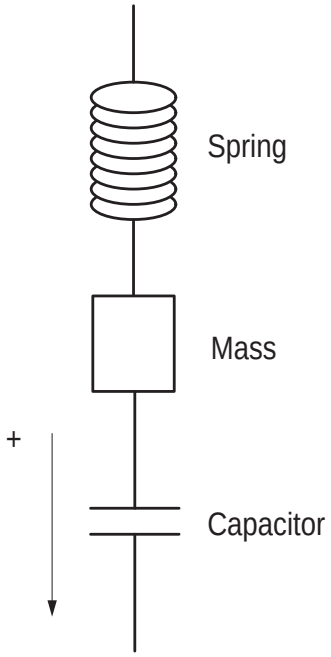

Figure 3.2: Lumped model of CMUT element [14]

permittivity, 'S' is the area of the electrodes, 'd_o' is the initial separation between electrodes, 'x' is the displacement along the direction stated in Figure 3.2. Equation 3.2 indicates that electrostatic force between the parallel electrodes is proportional to the square of the applied voltage and the equivalent permittivity of the medium among the electrodes. On the other hand, it is inversely proportional to the distance between the electrodes.

CMUT operation requires both DC and AC voltages ($V_{total}=V_{AC}+V_{DC}$). Hence, electrostatic force is proportional to the square of the applied voltage, DC voltage should be chosen large enough to obtain linear CMUT operation. Therefore, electrostatic force can be written as in Equation 3.3 [66].

$$F_{elec.force} = \frac{\xi_o S}{2d^2}\left(V_{DC}^2 + 2V_{DC}V_{AC} + V_{AC}^2\right) \tag{3.3}$$

The third term in parenthesis is standing for harmonic contribution of AC voltage. It is clearly seen that high DC voltage can be applied to eliminate the effects of AC harmonics. Therefore, harmonic contribution caused by AC excitation can be ignored for CMUT operations.

3.0.4.1 Collapse Voltage Calculation

Collapse voltage is one of the most crucial parameters for CMUT designs. Because, operation modes of device are set by this voltage value. At this voltage level, mechanical restoring force of membrane can not balance the electrostatic attraction force. Therefore, membrane goes toward the substrate and collapses.

Equation 3.1 can be rearranged with the capacitor, spring and mass force terms and it gives:

$$m\frac{d^2x(t)}{dt^2} - \frac{\xi S\,[V(t)]^2}{2\,[d_o - x(t)]^2} + kx(t) = 0 \tag{3.4}$$

where 'k' is the spring constant. Equation 3.4 is the second order differential equation. Time dependency can be ignored in order to obtain quantitive values for solution. It can be considered V(t)=V_{DC} and the result will be:

$$\frac{\xi S\,V_{DC}^2}{2(d_o - x)^2} = kx \tag{3.5}$$

The solution of the Equation 3.5 gives the approximate collapse voltage and displacement value of the membrane structure before it collapses to the substrate.

$$V_{collapse.voltage} = \sqrt{\frac{8kd_o^3}{27\xi S}} \tag{3.6}$$

$$x_{collapse.displacement} = \frac{d_o}{3} \tag{3.7}$$

The collapse voltage is proportional to the distance between electrode and inversely proportional to the area of the electrodes. These parameters can be controlled by designer to obtain desired collapse voltage. Additionally, it depends on the type of the membrane material and

total electrical permittivity between electrodes. If the membrane is insulating material, Equation 3.6 should be modified as stated in Equation 3.8.

$$V_{collapse.voltage} = \sqrt{\frac{8k}{27\xi S}} \left(\frac{d_{membrane}}{\xi_r + d_o} \right)^{\frac{3}{2}} \tag{3.8}$$

Typical microfabrication of CMUT membrane has the insulation layer on the substrate material. This insulating layer is effective on snap-back voltage at which membrane leaves from substrate and goes to the original position. The equation for snap-back voltage is given [18]:

$$V_{snap-back.voltage} = \sqrt{\frac{2kd_{insulator}^2(d_o - d_{insulator})}{\xi_{insulator} S}} \tag{3.9}$$

Collapse voltage calculation uses the spring constant value that is not easy to be determined for membrane materials. More accurate calculation can be done with using electrostatic force equation for membrane capacitance. The gap can be modeled like several small capacitors. Using this parallel combination of capacitors, the collapse voltage value can be obtained with better accuracy [66]. Corresponding structure is shown in Figure 3.3 [66] and Equation 3.10 [66].

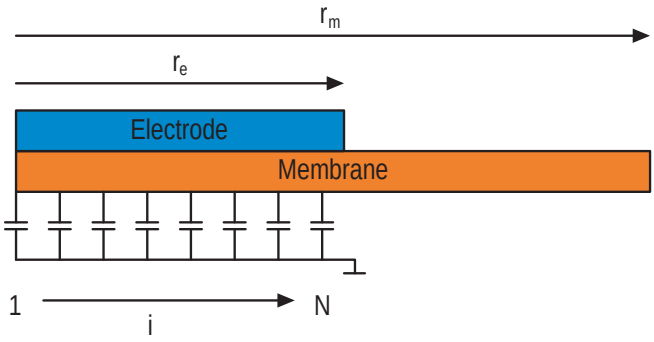

Figure 3.3: Membrane and air gap with small capacitors [66]

$$F_i = \frac{\xi_o V_{dc}^2 S_i}{2d_i^2} \tag{3.10}$$

'S_i' is the area of the small capacitor electrodes and 'd_i' is the effective air gap height as stated below [66]:

$$d_i = \frac{t_m}{\xi_{r1}} + g_i + \frac{t_{ins}}{\xi_{r2}} \tag{3.11}$$

The thickness of the membrane structure and insulator material are given 't_m' and 't_{ins}', respectively. 'ξ_{r1-2}' state the electrical permittivities of mediums.

Plate theory [67] can be used to determine the displacement of electrodes under the effect of electrostatic force. Each capacitor effect is considered in order to obtain total displacement. Equation 3.12 and 3.13 are used to obtain each displacement of segments that effected by related capacitor. Total displacement is maintained by superposing each segment movements.

If r> b_i,

$$w_i(r) = \frac{F_i}{8D\pi}\left\{\frac{(r_m^2 + b_i^2)(r_m^2 - r^2)}{2r_m^2} + (b_i + r^2)ln(\frac{r}{r_m})\right\} \tag{3.12}$$

If r≤ b_i,

$$w_i(r) = \frac{F_i}{8D\pi}\left\{\frac{(r_m^2 + b_i^2)(r_m^2 - r^2)}{2r_m^2} - (b_i + r^2)ln(\frac{r}{r_m})\right\} \tag{3.13}$$

Displacement of each segment is given by '$w_i(r)$' where 'b_i' is the radius of each segment, 'F_i' is the force on that segment and 'D' is the flexural rigidity. Total displacement can be found by summing the all movements comes from segments. Collapse voltage calculations is required iterations until the divergence obtained. When the divergence is reached, it means that applied voltage is larger than the collapse voltage. Therefore, collapse voltage can be determined by using iterations.

3.0.4.2 Electromechanical Coupling Coefficient

Electromechanical coupling coefficient is the ratio of the mechanical energy transferred to the load to the total energy stored in the transducer. Electromechanical coupling coefficient is given in Equation 3.14 [20].

$$k_T^2 = \frac{E_{mech}}{E_{total}} = \frac{1}{1 + \frac{E_{elec}}{E_{mech}}} \tag{3.14}$$

'k_T^2' is the electromechanical coupling coefficient and 'E_{total}' is the total electrical and mechanical energy stored in the device [20]. If the transducer is considered as a piston shape having a similar movement characteristics of it, the equation stated in 3.14 will be [20]:

$$k_T^2 = \frac{2x}{d_o - x} \tag{3.15}$$

'd_o' stand for the initial distance between parallel plates and 'x' is the displacement under the excitation voltage. Until now, it is assumed that membrane forms the conductive electrode, there is no insulation layer between the gap and negative electrode. If these effects are taken into account, 'd_{eff}' stated in Equation 3.16 should be considered [20]:

$$d_{eff} = d_o + \frac{d_t}{\xi_r} \tag{3.16}$$

'd_t' is the total thickness of membrane and insulation layer. 'ξ_r' is the effective relative dielectric constant of the materials. Series capacitances at the vacuum gap of the transducer cause the membrane to collapse at one third of the membrane displacement.

Coupling coefficient can also be expressed with using fixed ('CS') and free ('CT') capacitance approach [68]. The fixed capacitance is the total capacitance under DC bias voltage. The slope of the charge-voltage curve presents the free capacitance. Therefore, coupling coefficient can be determined as stated in Equation 3.17:

$$k_T^2 = 1 - \frac{C_S}{C_T} \tag{3.17}$$

3.0.4.3 Electrostatic Actuation of Membrane

The operation of CMUT membrane requires both AC and DC voltage excitations. Due to the time varying AC signal, the time varying electrostatic force exerted on the membrane is given in Equation 3.18 [69].

$$F = \frac{\xi A V_{bias} V_{ac}}{d^2} cos(\omega t + \phi) \tag{3.18}$$

where 'A' is the capacitor area, 'ξ' is the dielectric constant, 'd' is the initial electrode separation, 'V_{bias}' and 'V_{ac}' are the voltage excitations between the electrodes. Electrostatic pressure on the membrane can be found dividing the Equation 3.18 with capacitor area (Phasor form (3.18) is used) [69]. Electrostatic pressure is given in Equation 3.19.

$$P = \frac{\xi_{eff} V_{bias} V_{ac}}{d_{eff}^2} \tag{3.19}$$

where,

$$\frac{\xi_{eff}}{d_{eff}^2} = \frac{\xi_a \xi_n}{(t_a + t_n)(\xi_a t_n + \xi_n t_a)} \tag{3.20}$$

'ξ_a' and 'ξ_n' are the dielectric constant of air gap and membrane material, respectively. 't_a' is the thickness of the air gap and 't_n' is the membrane thickness.

Resonance frequency is shown in Equation 3.21.It is shown that resonance frequency depends on the radius ('a'), material density ('ρ') and residual stress ('σ') of the membrane.

$$f = 2.405\frac{\pi}{a}\sqrt{\frac{\rho}{\sigma}} \tag{3.21}$$

Mechanical impedance of the membrane is given in Equation 3.22 [69]. This is basically defined as the ratio of the electrostatic pressure to the surface velocity of the membrane. Mechanical impedance of a circular membrane depends on the frequency of applied signal and physical parameters of the membrane.

$$Z_m = \frac{P}{V_{average}} \tag{3.22}$$

Surface velocity of the membrane is defined as [69]:

$$V_{average} = \frac{2j\omega\alpha}{a^2}\oint u(r)rdr \tag{3.23}$$

'α' is a constant describing the fraction of the membrane. It is less than one due to the lack of the total membrane vibration. The reason of that is the edge of the membrane's being mechanically disabled for the vibration under excitation voltage.

3.0.4.4 Electrical Equivalent Circuit of CMUT

Equivalent circuit of the transducer devices is useful for analysis and optimization of the device performance. Most of the transducers in MEMS technology have both electrical and mechanical domains. Electrical equivalent circuit can be obtained by replacing the mechanical quantities with corresponding electrical variables. The electrical capacitance of the membrane can be formed as in Equation 3.24 [18] where 'l_t' is the thickness of membrane, 'l_a' is the separation between the electrodes, 'ξ' is the dielectric constant and 'S' is the area of the capacitor.

$$C(t) = \frac{\xi_o \xi S}{\xi_o l_t + \xi l_a(t)} \tag{3.24}$$

If the applied total voltage is '$V = V_{DC} + V_{ac}sin(\omega t)$' where the '$V_{ac} \ll V_{DC}$', the flowing current through the transducer can be given as stated in Equation 3.25.

$$I = \frac{d}{dt}Q = \frac{d}{dt}(C(t)V(t)) = C(t)\frac{d}{dt}V(t) + V(t)\frac{d}{dt}C(t) \tag{3.25}$$

'$C(t) = C_o + C_{ac}sin(\omega t + \phi)$' can be stated due to the small signal analysis where the '$C_{ac} \ll C_o$'. Equation 3.25 can be rearranged as in Equation 3.26.

$$I = C_o\frac{d}{dt}V_{ac}(t) + V_{DC}\frac{d}{dt}C_{ac}(t) \tag{3.26}$$

The result of the differentiation of the Equation 3.24 is given in Equation 3.27.

$$\frac{d}{dt}C_{ac}(t) = -\frac{\xi_o\xi^2 S}{(\xi_o l_t + \xi l_{ao})^2}\frac{d}{dt}l_a(t) \tag{3.27}$$

Where '$(d/dt)l_a$' is equal to the membrane velocity ('$\bar{v}$') and 'l_{ao}' is the gap spacing under a DC voltage. Substituting the Equation 3.27 to 3.26:

$$I = C_o\frac{d}{dt}V_{ac}(t) - \frac{V_{DC}\xi_o\xi^2 S}{(\xi_o l_t + \xi l_{ao})^2}\bar{v} \tag{3.28}$$

Equation 3.28 show the transform of mechanical quantity to electrical current. Therefore, transformer ratio is given in Equation 3.29.

$$n = \frac{V_{DC}\xi_o\xi^2 S}{\xi_o l_t + \xi l_{ao}} \tag{3.29}$$

The transformer ratio depends on the applied DC bias, membrane and air gap thicknesses. The electrical equivalent circuit of CMUT is given in Figure 3.4.

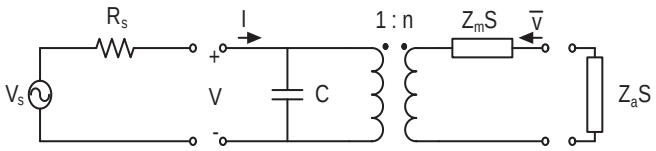

Figure 3.4: Electrical equivalent circuit of CMUT device [18]

3.0.5 Layout Design of 1-D CMUT Arrays

Design of the layouts were done with L-EDIT software released by Tanner EDS company. The design of 1-D CMUT arrays was performed considering different cell sizes, element size depending desired resonance frequencies. Designed CMUT arrays are shown in Table 3.1. They were designed for operating between 1 - 10 MHz signal ranges.

Table 3.1: Different designs of 1-D CMUT arrays

1-D CMUT Arrays	Cell Diameter, μm	Cell Seperation, μm	Element Width, μm
1. Type	120	6	375
2. Type	120	12	375
3. Type	88	6	375
4. Type	88	12	375
5. Type	72	6	250
6. Type	72	12	250
7. Type	54	6	250
8. Type	54	12	250
9. Type	44	6	250
10. Type	44	12	250

The layouts of 1-D CMUT arrays stated in Table 3.1 were designed. 1-D CMUT arrays that includes diameter of 120 μm and 44 μm cells are shown in Figure 3.5.

The cell radius of 1-D CMUT arrays were adjusted for operating at several resonance frequencies. When the cell radius is decreased, the resonance frequency is shifted to higher frequency values. The separation of CMUT cells affects the fill factor of the transducer. Higher output pressure and better sensitivity of CMUTs can be obtained by enhanced fill factor of the device. Hence, increasing the active area of the transducer causes some difficulties in wafer bonding during CMUT fabrication. The contact area is inversely proportional to the fill factor. Calcu-

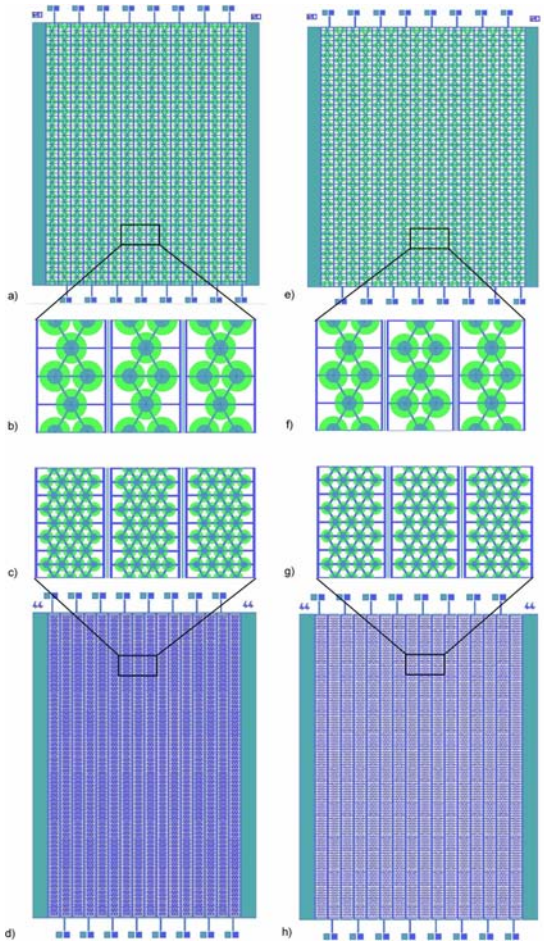

Figure 3.5: a) 120 μm 1-D CMUT transducer with 6 μm cell separations, b) 120 μm CMUT cells with 6 μm separation, c) 44 μm CMUT cells with 6 μm separation, d) 44 μm 1-D CMUT transducer with 6 μm cell separations, e) 120 μm 1-D CMUT transducer with 12 μm cell separations, f) 120 μm CMUT cells with 12 μm separation, g) 44 μm CMUT cells with 12 μm separation, h) 44 μm 1-D CMUT transducer with 12 μm cell separations

lated fill factor and contact area for wafer bonding are shown in Table 3.2.

As shown in Table 3.2, there is a trade-off between the reliability and performance of the transducer according to the fill factor. Besides, higher contact area can be obtained when the cell diameter of CMUT membranes are reduced. The fill factor can also be affected by the shape of CMUT cells.

Elements' width of the CMUT arrays were adjusted to reduce the grating lobes. Spacing between the elements must be less than the half of the operating frequency wavelength to eliminate possible grating lobe creations ($E_{width} < \frac{\lambda}{2}$).

Table 3.2: Calculated active and contact areas

Cell Diameter, μm	Cell Seperation, μm	Active Area, %	Contact Area, %
120	6	82.21	17.79
120	12	74.91	25.09
88	6	79.44	20.56
88	12	70.19	29.81
72	6	77.23	22.77
72	12	66.59	33.41
54	6	73.42	26.58
54	12	60.67	39.33
44	6	70.19	29.81
44	12	55.95	44.05

Metal lines on the CMUT cell electrodes were routed to the main line as many connection as possible in order to decrease the equivalent resistance. Additionally, the top electrodes' radii are patterned as the half of the membrane radius. This approach is efficient to increase the bandwidth of the device. The most mechanically moveable part of the membrane is the middle and areas close to the center. Performing the metallization over the middle of membrane supports better performance of CMUTs. The physical dimension of the 1-D CMUT array including 72 μm diameter cells is shown in Figure 3.6 and Table 3.3.

Table 3.3: Physical diamensions of 72 μm 1-D CMUT array

Number of elements	16
Cells per element	122
Height of elements (h), μm	6000
Width of array (w), μm	3200
Width of elements (a_w), μm	200
Membrane radius (r_m), μm	36
Electrode radius, (r_e), μm	18
Separation of cells (2s), μm	12
Electrode thickness (t_e), μm	0.4
Membrane thickness (t_m), μm	1
High temperature oxide thickness (t_{ho}), μm	0.2
Gap thickness (t_g), μm	1.57
Silicon substrate thickness(t_s), μm	525

Wafer floor planning of 1-D CMUT arrays and single CMUTs are shown in Figure 3.7. Single CMUTs and 1-D CMUT arrays were fabricated on same wafer. The reserved space for each

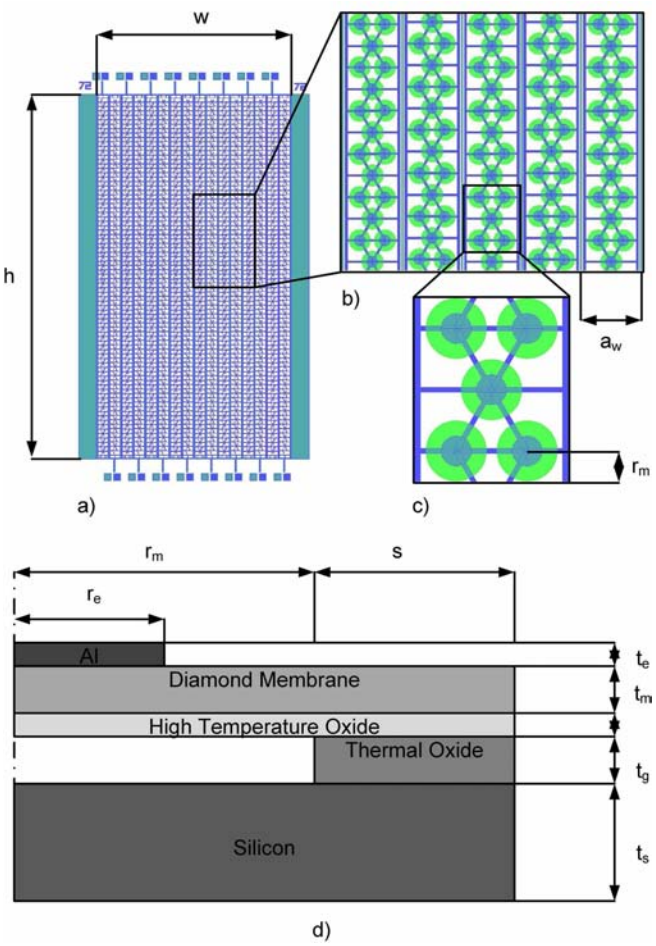

Figure 3.6: Physical dimensions of 72 μm 1-D CMUT array

design was 49 mm^2 for total number of 49 CMUT designs. 20 design areas were used for 1-D CMUT arrays and remaining 28 design areas were reserved for single CMUT devices. The middle part of the wafer was kept empty in order to increase contact area for better fusion bonding in CMUT fabrication.

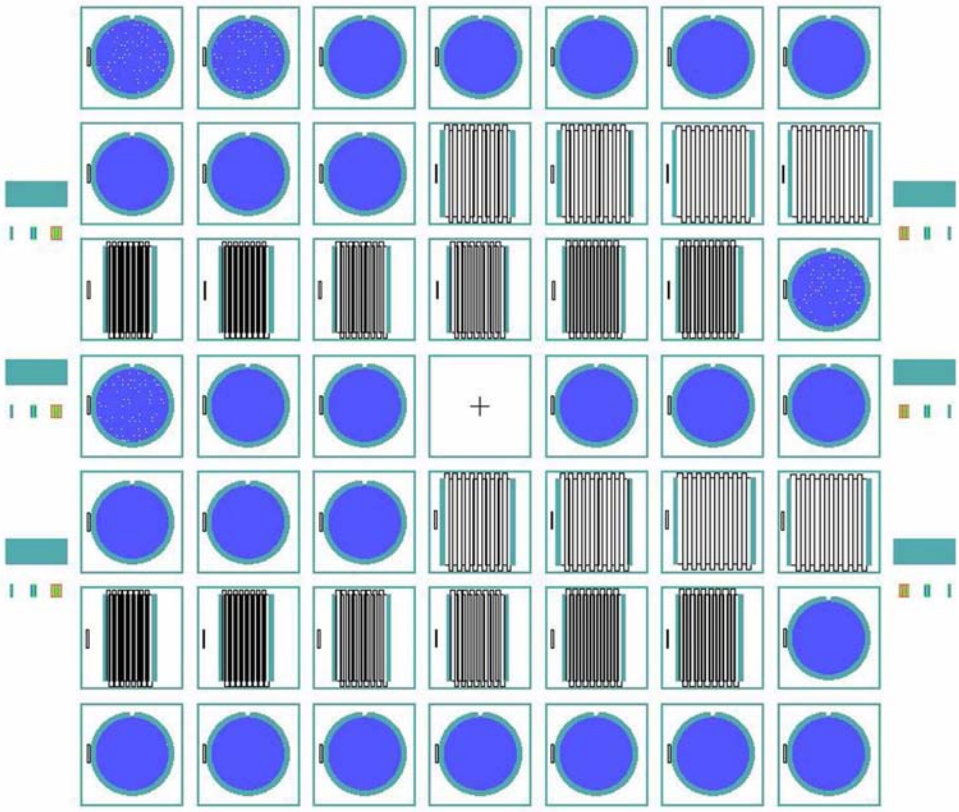

Figure 3.7: Floor planning of 1-D CMUT arrays and single CMUT designs

3.0.6 Capacitance Calculation of CMUT Devices

The capacitance values for both 1-D CMUT arrays and single CMUTs were calculated. The dimensions of the CMUT cells are shown in Figure 3.8.

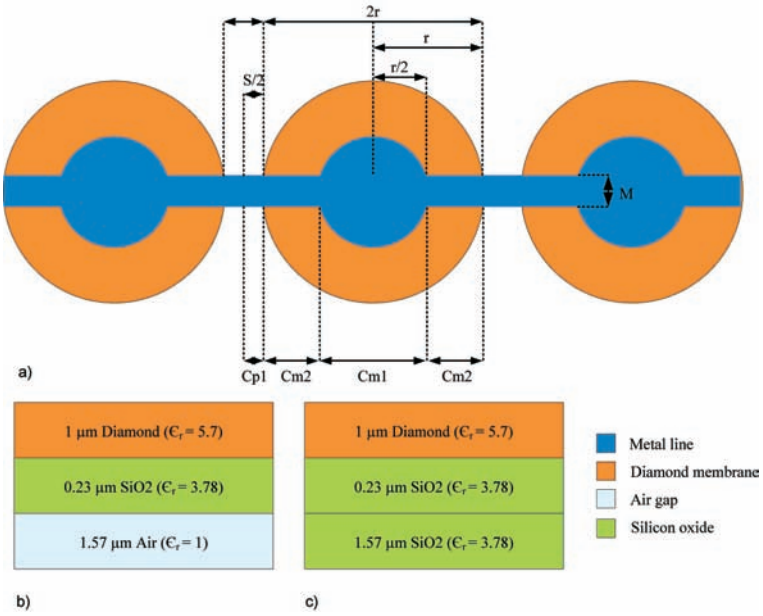

Figure 3.8: a) The physical variables of CMUT cell dimensions, b) Physical structure under the membrane, c) Physical structure under the metal lines where there is no air gap

Capacitance calculation can be divided in to two parts as main capacitance which is under the membrane structures and parasitic capacitance which is considered to be a possible capacitance anywhere else without membrane structures. Due to the different physical structure and number of the CMUT cells, parasitic capacitance calculations for single and array devices should be performed seperately.

Yuan's formula was used to calculate the capacitance values. Formulation of the main capacitance (C_m) under the membrane structure is shown in Equation 3.30. This equation can be used for both single and 1-D CMUT devices in order to calculate main capacitance values under the membrane structures.

$$C_m = \left[\xi_o \frac{\pi(\frac{r}{2})^2}{H_1} + (\pi r - Mn)\xi_o K_1 + \xi_o \frac{n(\frac{r}{2})M}{H_1} + rn\xi_o K_1\right] N \tag{3.30}$$

where,

$$H_1 = \frac{H_{air}}{\xi_{air}} + \frac{H_{SiO_2}}{\xi_{SiO_2}} + \frac{H_{diamond}}{\xi_{diamond}} \tag{3.31}$$

$$K_1 = \frac{\pi}{ln\left[1 + \frac{2H_1}{T}(1 + \sqrt{1 + \frac{T}{H_1}})\right]} - \frac{T}{4H_1} \tag{3.32}$$

'n' is the number of the metal lines in each cells and 'T' is the thickness of the metal line deposited on the CMUT device. 'N' is the number of the cells related to the transducer structure.

Parasitic capacitance calculations were performed seperately for single and 1-D CMUT devices. Formulation of the parasitic capacitance (C_p) for single CMUTs is shown in Equation 3.33.

$$C_p = \left[\left[\frac{n(\frac{s}{2})M}{H_2} + snK_2\right]N + \frac{2\pi Rt}{H_2} + [2\pi(R_{in} + R_{out})]\,K_2 + \frac{ab + cd}{H_2} + Z\right]\xi_o \tag{3.33}$$

where,

$$H_2 = \frac{H_{SiO_2}}{\xi_{SiO_2}} + \frac{H_{SiO_2}}{\xi_{SiO_2}} + \frac{H_{diamond}}{\xi_{diamond}} \tag{3.34}$$

$$K_2 = \frac{\pi}{ln\left[1 + \frac{2H_2}{T}(1 + \sqrt{1 + \frac{T}{H_2}})\right]} - \frac{T}{4H_2} \tag{3.35}$$

$$Z = 2\,[b + d + c]\,K_2\xi_o \tag{3.36}$$

'R_{in}' is the inner, 'R_{out}' is the outer, 'R' is the average radius values and 't' is the width of the surrounding metal line that covers all CMUT cells. 'a, b, c, d' are the dimensions of the pad structure that used to make the connections from CMUT devices to outside world.

Formulation of the parasitic capacitance for 1-D CMUT devices is shown in Equation 3.39.

$$C_{p1} = \left\{ \left[\frac{\frac{s}{2} n_1 M}{H_2} + s n_1 K_2 \right] + \left[\frac{\frac{s}{2} n_2 M}{H_2} + s n_2 K_2 \right] \right\} \xi_o \frac{N}{2} \tag{3.37}$$

$$C_{p2} = \left\{ \left[\frac{2t_o}{H_2} + 4K2 \right] (H + W) + \left[\frac{(ab + cd)}{H_2} + 2(b + d + c) K_2 \right] \right\} \xi o \tag{3.38}$$

$$C_p = C_{p1} + C_{p2} \tag{3.39}$$

where,

$$H_2 = \frac{H_{SiO_2}}{\xi_{SiO_2}} + \frac{H_{SiO_2}}{\xi_{SiO_2}} + \frac{H_{diamond}}{\xi_{diamond}} \tag{3.40}$$

$$K_2 = \frac{\pi}{ln\left[1 + \frac{2H_2}{T}(1 + \sqrt{1 + \frac{T}{H_2}})\right]} - \frac{T}{4H_2} \tag{3.41}$$

'n_1' and 'n_2' are the number of seperate metal lines in related cell structures. 'H' and 'W' are the height and width of the CMUT elements and 't_o' is the width of the metal line.

MATLAB software (The MathWorks Inc., MA, USA) was used to calculate the total capacitance values as shown in Table 3.4. Total capacitance values of single CMUT devices were calculated for all cells in the device. Furthermore, for 1-D CMUT arrays, it shows the calculated capacitance value for a single element. The number in the array name (Array250) indicates the width of the element seperation.

Most capacitance value is introduced by membrane structures. Therefore, total capacitance value is directly proportional to the number of cells in the device. Parasitic capacitance value

can be decreased by denser designs, sacrifying reserved contact areas for direct bonding process.

Table 3.4: Calculated capacitance values of CMUT devices

CMUT	Cell Radius, μm	Cell Seperation, μm	Number of Cells	Calculated Total Capacitance, pF
Array250	44	6	473	4.82
Array250	44	12	431	5.23
Array250	54	6	288	4.13
Array250	54	12	260	4.31
Array250	72	6	132	3.33
Array250	72	12	123	3.42
Array375	88	6	183	4.62
Array375	88	12	173	4.74
Array375	120	6	83	3.83
Array375	120	12	78	3.83
Single	44	6	9656	74.32
Single	44	12	7682	74.72
Single	54	6	6698	65.15
Single	54	12	5538	65.25
Single	72	6	3930	54.97
Single	72	12	3404	54.76
Single	88	6	2708	49.87
Single	88	12	2398	49.30
Single	120	6	1500	43.66
Single	120	12	1372	42.98

MATLAB software was used to calculate the total capacitance values as shown in Table 3.4.

CHAPTER 4

MICROFABRICATION OF CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS WITH DIAMOND MEMBRANES

4.1 Introduction

Microfabrication of CMUT devices with diamond membranes has been firstly performed using new microfabrication techniques and steps. Silicon and silicon nitride (Si_3N_4) materials are generally used to perform membrane structure of CMUTs. Due to weak physical properties of these materials, membrane structure may be damaged during CMUT operation. Diamond is proposed as a new structural material for CMUT membranes that can potentially serve more robust and reliable operation. In this chapter, microfabrication steps of CMUTs with diamond membranes are introduced. Most of the microfabrication steps have been performed at METU-MEMS Research and Application Center.

4.2 Thermal Oxidation, Characterization of Thermally Oxidized Silicon Wafers and Cavity Patterning

In this section, the effect of thermal oxide growth on high resistivity, n-type, highly boron doped p-type and phosphorous doped n-type silicon wafers are investigated. Macro surface profiles of thermally oxidized highly boron doped silicon wafers are explored with profilometer. The effects of wet and dry oxide etching to pattern CMUT cells are examined.

4.2.1 Thermal Oxidation

Thermal oxide growth is performed using THERMCO diffusion oven. Before the oxide growth, process wafers should be cleaned in order to increase the quality of the oxidation step. The recipe for the cleaning process is given in Table 4.1.

Table 4.1: Recipes for cleaning process before oxidation

Cleaning Process 1	Cleaning Process 2	Cleaning Process 3
5:H_2O 1:NH_4OH 1:H_2O_2	6:H_2O 1:HCl 1:H_2O_2	4:H_2O 1:HF –
80^oC, 7 minutes	80^oC, 7 minutes	Room Temperature, 20 seconds

When the cleaning process is completed, the oxidation step should be started in order to keep the wafers as clean as possible.

Thickness of the oxide layer is crucial for the operation of CMUT devices. Since, thickness of thermal oxide layer determines the cavity depth of CMUT cells. Therefore, thermal oxide growth process should be managed sensitively in order to obtain desired oxide thickness. Optimized process steps for thermal oxidation are developed. First, THERMCO furnace is heated up to 1000^oC under nitrogen (N_2) gas and then temperature is adjusted sensitively with three heaters in the furnace. After that, heaters are closed at least for 9 hours in order to decrease the temperature of furnace under 100^oC. Then, cleaned wafers are loaded with the autoloader into the chamber. Next, the heaters are activated to raise the temperature of chamber to 1000^oC. Stabilization is done for 5 minutes under N_2 gas. Then, three steps oxidation process is ready to run. In first step, the oxygen (O_2) gas is delivered to the chamber for dry oxidation for 20 minutes. This oxidation step is crucial for the thermal stabilization and controlling the maximum growth rate of oxide layer.

$$Si + O_2 \rightarrow SiO_2 \tag{4.1}$$

In second step, the wet oxidation is applied by exposing hydrogen (H_2) and oxygen gases into the chamber.

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \tag{4.2}$$

Main thickness of the oxide layer is adjusted in second step with wet oxidation. Duration of the wet oxidation determines the thickness of the oxide layer. In third step, 20 minutes of dry oxidation is applied in order to increase the surface quality of the oxide layer. After, only N_2 gas is used to stabilize the oxidation process for 5 minutes. When the oxidation process ends, it is required to wait at least for 9 hours before unloading the processed wafers. Therefore, temperature of wafers will decrease slowly without having any stress due to the sudden temperature changes.

There are several oxidation processes using high resistivity, n-type, highly boron doped p-type and phosphorous doped n-type silicon wafers. Thermally grown oxide thickness is measured by reflectometer (NANOMETRICS).

The first thermal oxidation was performed to grow 5500 Å thickness of oxide. Average thickness measurements of each 50 processed wafers are shown in Figure 4.1. Thicknesses of each wafer were taken from equally distanced 9-points with reflectometer.

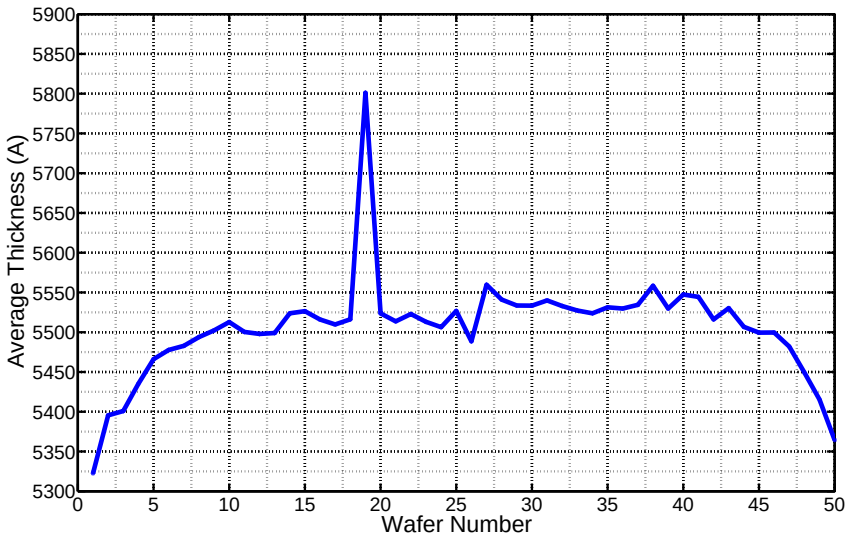

Figure 4.1: Average oxide thickness measurements of 5500 Å thermal oxidation process

Number nineteenth of processed wafers has unexpected oxide thickness due to possible initial cleanliness problem. The prime wafer region of this thermal oxide process is between number

of 20 and 25. The standard thickness deviations of each wafer are shown in Figure 4.2.

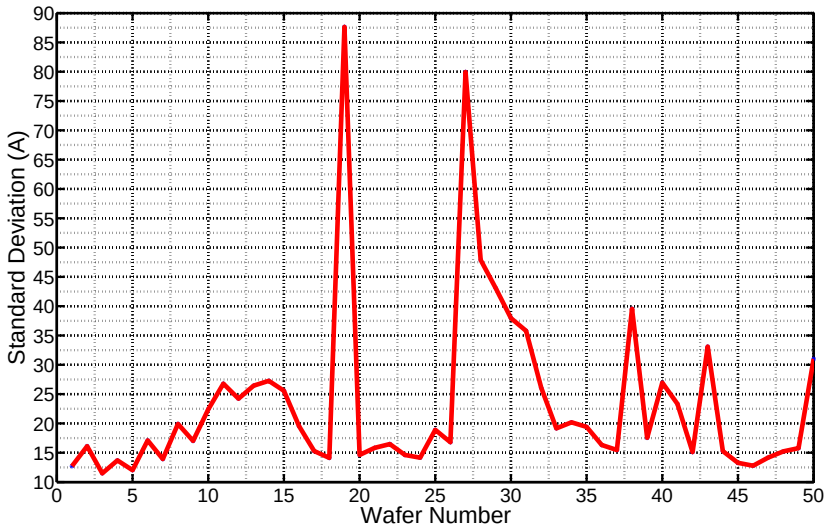

Figure 4.2: Standard thickness deviation of 5500 Å thermal oxidation process

Second oxidation process aimed to obtain 5050 Å thickness of oxide. Average thickness measurements and standard thickness deviations of wafers in prime region are given in Figures 4.3 and 4.4, respectively.

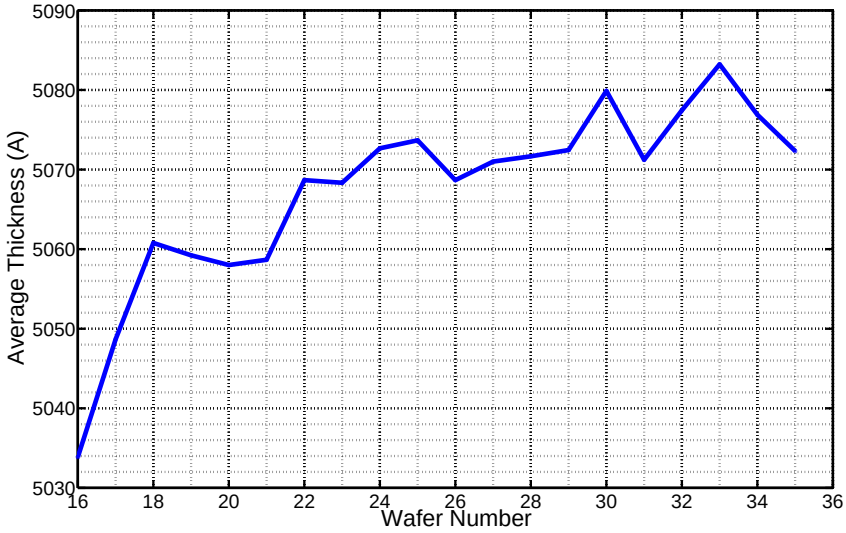

Figure 4.3: Average oxide thickness measurements of 5050 Å thermal oxidation process

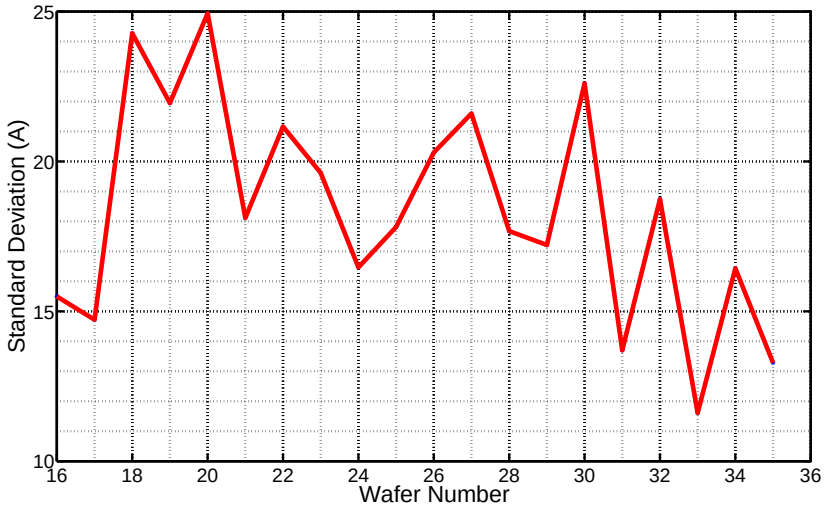

Figure 4.4: Standard thickness deviation of 5050 Å thermal oxidation process

High resistivity, n-type and highly boron doped p-type silicon wafers were used in oxidation process to grow 12000 Å oxide layer. Average thickness measurements and standard thickness deviations of wafers are given in Figures 4.5 and 4.6, respectively.

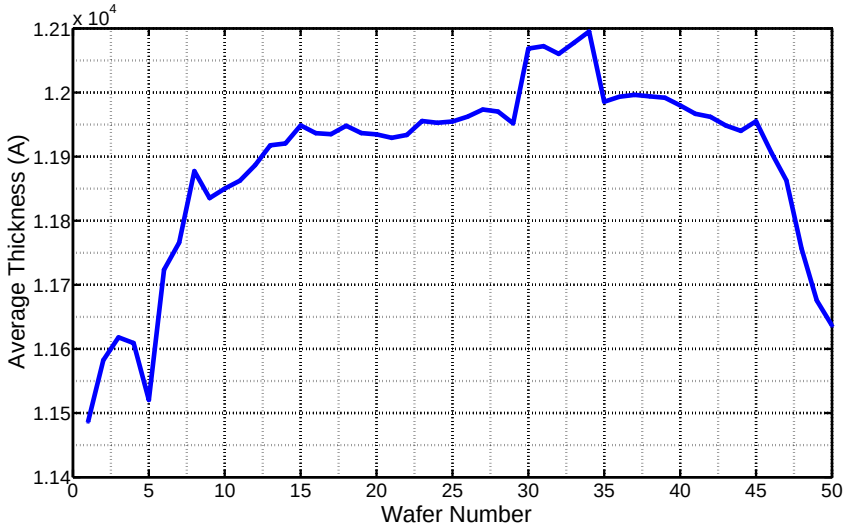

Figure 4.5: Average oxide thickness measurements of 12000 Å thermal oxidation process

One of the important observations of thickness measurement shown in Figure 4.5 is the different oxide thicknesses grown on the processed wafers. Highly boron doped p-type silicon

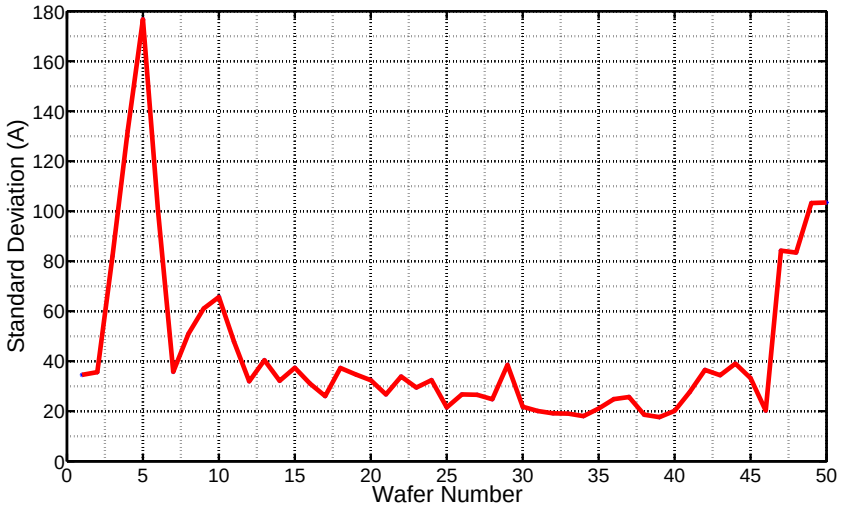

Figure 4.6: Standard thickness deviation of 12000 Å thermal oxidation process

wafers were located between the slot number of 30 and 34. It is shown that these wafers are thicker approximately 100 Å than n-type (wafer number 40-45) and high resistivity (wafer number 11-29) silicon wafers. High resistivity and n-type silicon wafers have similar response of thermal oxidation.

One of the thermal oxidation model is Deal-Grove model and it was reported in 1965 [70]. This model can not satify very thin thermal oxide growth, because of very thin oxide layers' not having been able to be fabricated during the midths of 1960s. When thin oxide generation on silicon was available in semiconductor fabrication technology, the Deal-Grove model was needed to be developed in order to response accurately for thin oxide regime. Deal-Grove concept was improved by Massoud for thin oxide generation in 1985 [71]. Massoud formulation of thin oxide regime is given in Equation 4.3.

$$\frac{dx_o}{dt} = \frac{B}{2x_o + A} + C_1 e^{-\frac{x_o}{L_1}} + C_2 e^{-\frac{x_o}{L_2}} \tag{4.3}$$

Where 'B' and '$\frac{B}{A}$' are the linear rate constants that are stated in Equations 4.4 and 4.5, respectively [72].

$$B = C_B e^{-\frac{E_B}{kT}} \tag{4.4}$$

$$\frac{B}{A} = C_{\frac{B}{A}} e^{-\frac{E_{\frac{B}{A}}}{kT}} \tag{4.5}$$

'C_B', '$C_{\frac{B}{A}}$' constants and 'E_B', '$E_{\frac{B}{A}}$' activation energies depend on crystal orientation of silicon wafer and oxidation temperature. 'C_1' and 'C_2' constants are effective at the begining of oxidation until reaching the growth become pure linear parabolic.

Oxide thicknesses stated in Figure 4.5 are verified with Massoud oxidation method. Highly boron doped p-type silicon wafers have higher oxide generation rate due to the high boron doping. Oxide growth rate of highly boron doped silicon wafers (>1x10^{20} cm^{-3}) is high when it is compared to moderate boron doping level [73]. That is the reason of generated thicker oxide layer on highly boron doped p-type silicon wafers.

Another oxidation process was performed on previously oxidized highly boron doped p-type and n-type silicon wafers in order to observe deviation of the oxide thickness on a single wafer. Average thickness measurements and standard thickness deviations of wafers are given in Figures 4.7 and 4.8, respectively.

Oxide thickness variations are high on highly boron doped p-type silicon wafers (wafer number 31-34). As a result of different oxide thickness variations, every element of the same array may have different operational modes and efficiencies that are not desired for CMUT devices.

Another oxidation process was performed in order to obtain 15000 'Å' thickness of thermal oxide. Phosphorous doped n-type silicon wafers were oxidized. Thermal oxide grown wafers were used in prime CMUT fabrication process. Average thickness measurements and standard thickness deviations of these wafers are shown in Figures 4.9 and 4.10, respectively.

Phosphorous doping level has an effect on thermal oxidation rate [73]. Oxide thicknesses on n-type and phosphorous doped n-type silicon wafers (wafer number 11-40) differs due to the doped phosphorous element. This behavior is also verified by Massoud model of thermal

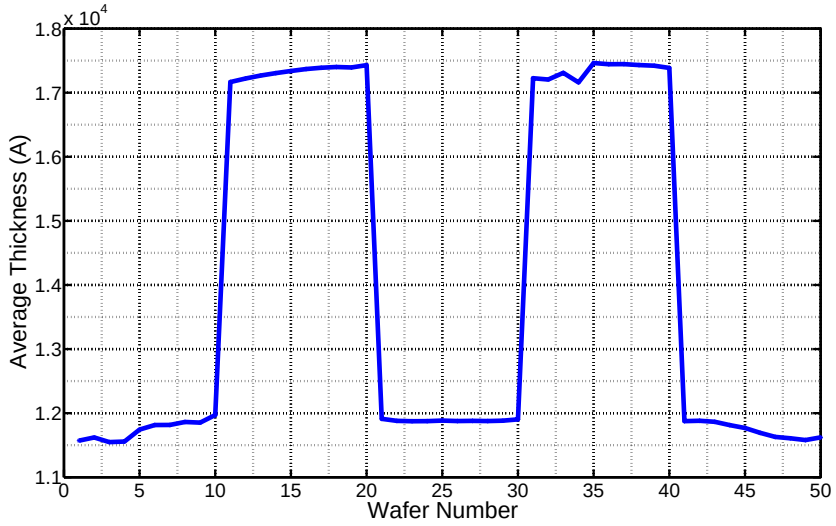

Figure 4.7: Average oxide thickness measurements of 17000 Å thermal oxidation process

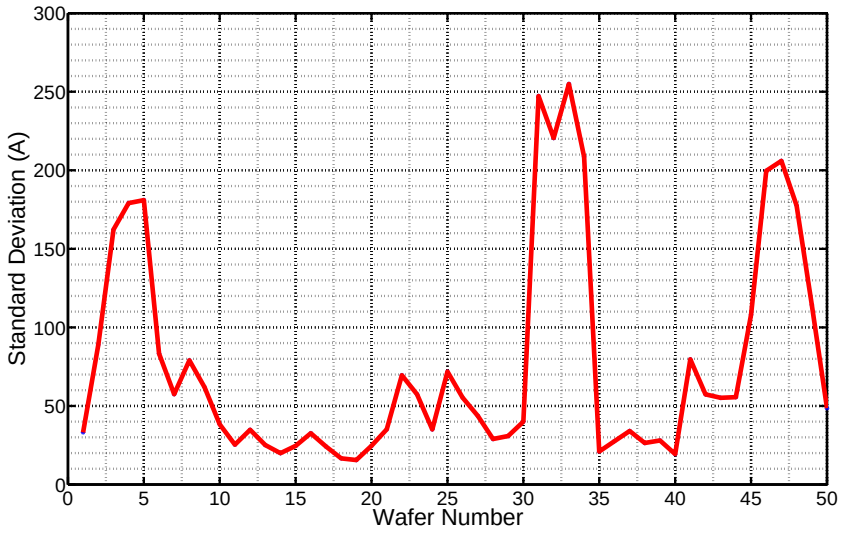

Figure 4.8: Standard thickness deviation of 17000 Å thermal oxidation process

oxidation. Wafers having slot numbers between 17 and 25 were used in prime CMUT device fabrication.

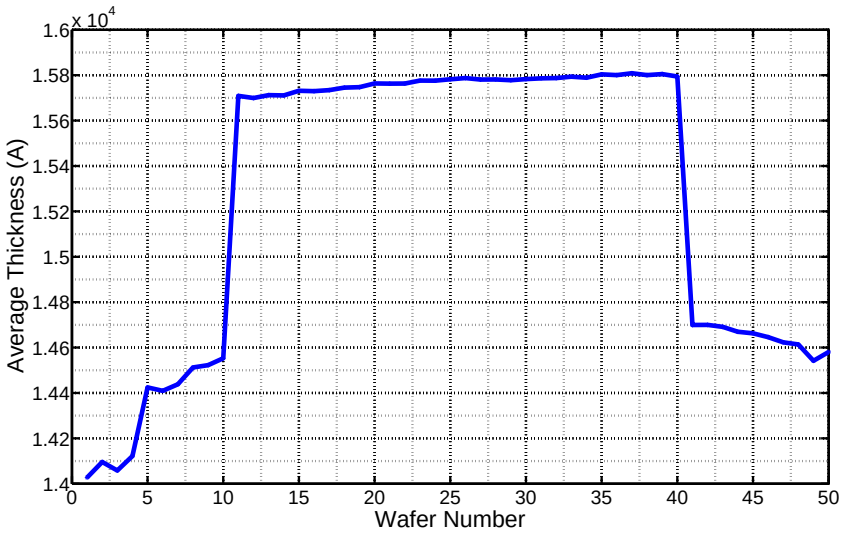

Figure 4.9: Average oxide thickness measurements of 15000 Å thermal oxidation process

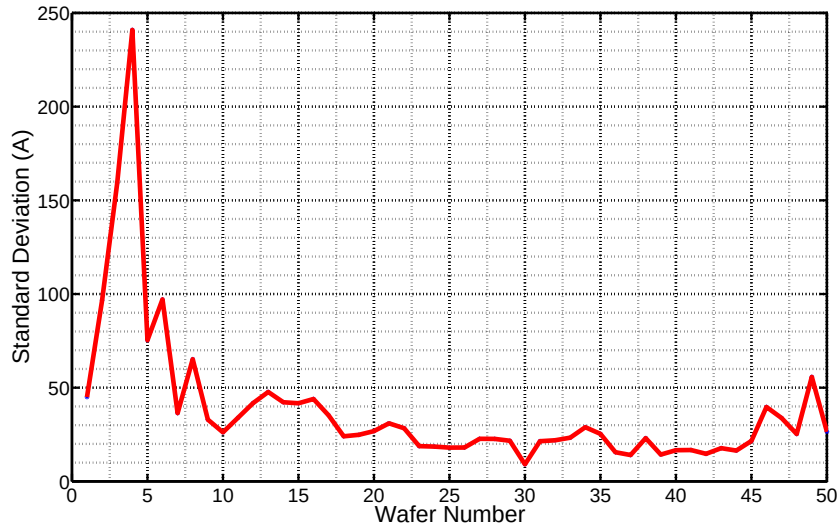

Figure 4.10: Standard thickness deviation of 15000 Å thermal oxidation process

4.2.2 Characterization of Thermally Oxidized Silicon Wafers

Highly conductive (ρ <0.005 ohm-cm) and high quality p-type, <1-0-0> silicon wafers were provided from Silicon Quest International Company. These wafers are going to be used as the bottom electrode structure for CMUT devices. Wafers have very low resistivity that supports the efficient grounding for bottom electrode. Besides, possible low leakage currents can be

eliminated by p-n junction mechanism when p-type wafers are used as the ground electrode. However, these high conductive wafers show macro waviness characteristics on their surface profiles. The surface profile of p-type silicon wafer with standard conductivity is shown in Figure 4.11.a. The white line, which was captured along 5 cm, indicates the surface profile. If the low frequency part is filtered, the surface profile of the wafer can be obtained as shown with blue line.

There is no crucial waviness on silicon wafer with standard conductivity (1 - 5 ohm - cm) as shown in Figure 4.11.a. This surface profile supports highly efficient wafer bonding considering the macro smoothness of the wafer surface. The surface profile measurement of highly conductive wafer (<0.005 ohm - cm) is shown in Figure 4.11.b. This macro waviness on the surface profile of wafer decreases the quality of direct bonding. As a result, these highly conductive wafers are not suitable for CMUT fabrication. Hence, phosphorous doped n-type silicon wafers were employed for diamond membrane CMUT fabrication.

4.2.3 Thermal Oxide Etch and Cavity Patterning

4.2.3.1 Photolithograpy of Thermal Oxide Grown Silicon Wafers

Designed layout mask for CMUT cells is transferred to a quartz mask in order to be used in photolithographic process. One of the critical process for photolithography is spreading out the photoresist material on the wafer surface. First, wafers that have thermal oxide on their surfaces are held in oven at 115^oC for 20 minutes. Because, the SiO_2 may absorb the water molecules from the atmosphere which causes low quality photoresist adhesion. Both faces of the wafers are spread with the photoresist material in order to protect the back side of the wafers from wet etchant. 3000 rpm spinning and S1813 photresist material are used to cover the wafers. After backside covering, wafers are held for 20 minutes in oven to be hard baked. One-minute soft bake is applied to front face of the wafers which are going to be patterned with photolithography. The patterns from mask are transferred to resist covered wafers by EVG620 mask aligner. UV light is exposed for 3.8 seconds to the surface of the wafers and MF-319 developer is used to remove the weaken areas for cell patterning for 45 seconds. After 45 seconds development, the wafers are washed with DI water for 90 seconds. Patterned photoresist structures are shown in Figures 4.12 and 4.13.

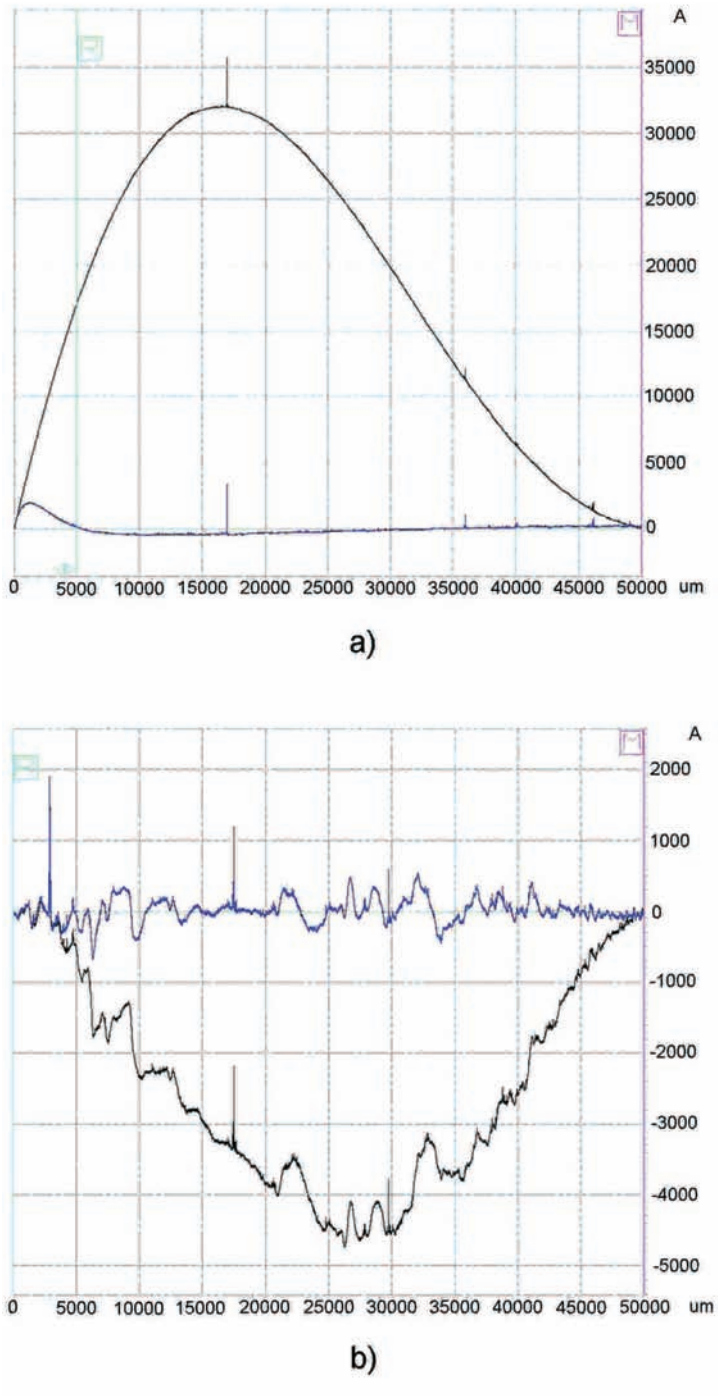

Figure 4.11: a) Surface profile of p-type silicon wafer with standard conductivity (1 - 5 ohm - cm), b) The surface profile of the highly conductive silicon wafer (<0.005 ohm - cm)

4.2.3.2 Wet Etching vs Dry Etching on Cavity Patterning

Oxide wet etching is done with buffered oxide etch (BOE) method for CMUT cavities. First, hydrophilic surface characteristic of wafer is developed using NANOPLAS Descum equip-

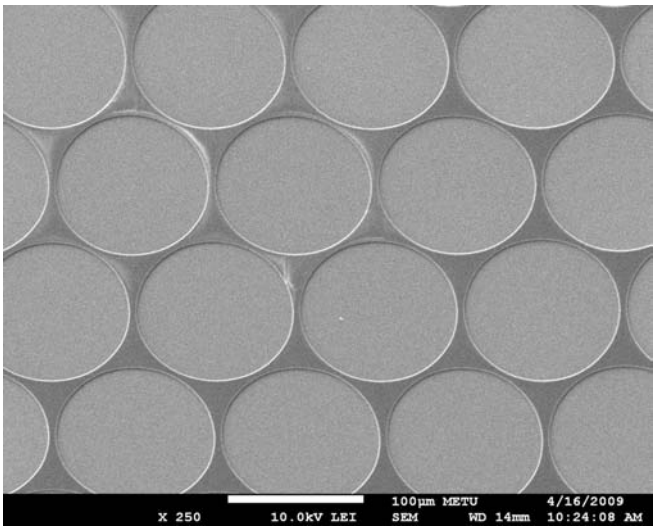

Figure 4.12: SEM image of the patterned photoresist material

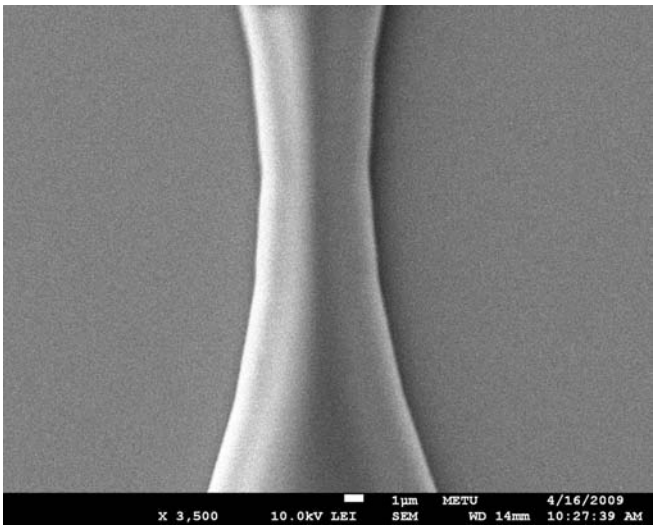

Figure 4.13: SEM image of patterned photoresist material between two adjacent cells

ment. When 60 seconds NANOPLAS Descum process is completed, wafers are held in oven at 115^{o}C for 30 minutes. For the wet oxide etching, required ratio of the mixture is 40% NH_4F (ammonium floride) : 49% HF (hidrofloric acid) (6:1).

Stated mixture has the etching speed of 15.1667 Å/s. The 14000 Å oxide thickness was etched in 1100 seconds which corresponded to 20% more time required for ideal etch duration. Additional time can be applied in order to be sure that oxide layer is totally removed. After

oxide etching, 70 minutes oxygen plasma is applied to strip the photoresist layer from front and back surfaces of the wafer. The BOE results for 14000 Å oxide thickness are shown in Figures 4.14 and 4.15.

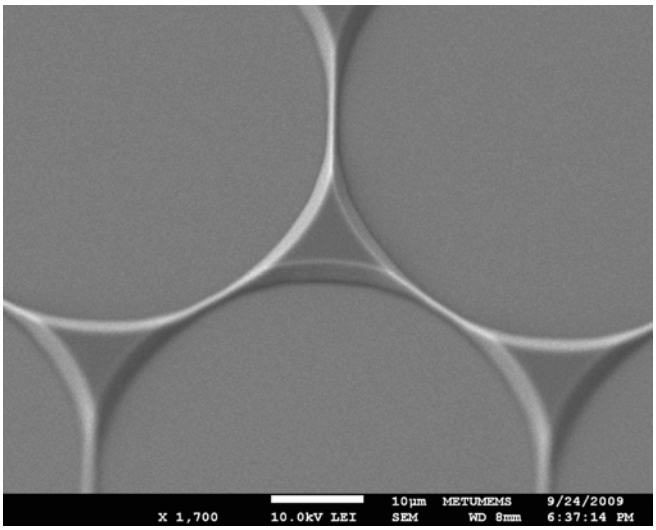

Figure 4.14: SEM image of membrane cavities after BOE method

The images given in Figures 4.14 and 4.15 show that pre-determined contact area for wafer bonding was decreased using wet etching method. For that reason, wet etchant affects the side walls of the oxide and it decreases the width of the oxide layer between the membrane cells. The result of this issue is not acceptable for proper and of high quality wafer bonding. Dry etching method was applied to eliminate further etching on oxide layer between the membrane cells.

Only the front side of the wafer's being covered with photoresist is sufficient for reactive ion etching (RIE). It is not required to cover the backside of the wafer with photoresist material. Only front side of wafer was covered and prepared for photolithographic process. In addition to that, photoresist was covered with 2000 rpm spinning and exposed for 4.5 seconds to be patterned and developed with MF319 for 55 seconds. 15 minutes oxide etching with RIE is applied to the wafers. After RIE oxide etch, the photoresist was striped with NANOPLAS for 2 hours. Finally, cleaning of the photoresist material is done for 15 minutes with H_2SO_4:H_2O_2(2:1) chemical mixture. Obtained membrane cell structures with RIE are shown in Figure 4.16.

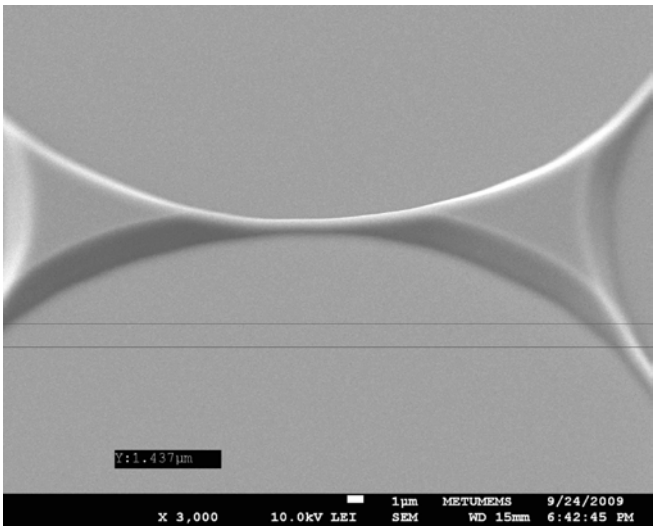

Figure 4.15: SEM image of remaining oxide layer between two membrane cavities

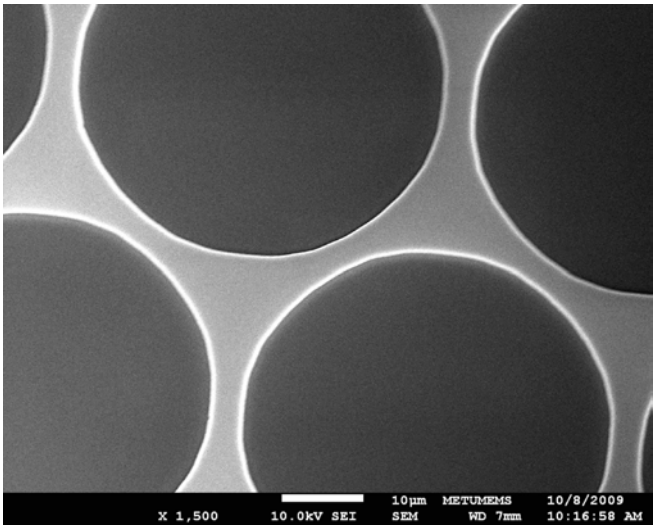

Figure 4.16: SEM image of dry oxide etching with RIE

Dry etching method gives better results for patterning of membrane cavities than wet etching method. The width of the oxide layer between cells is sustained in order to obtain better quality of wafer bonding as shown in Figure 4.16.

4.3 Wafer Bonding for CMUT Devices with Diamond Membrane

Wafer bonding is a crucial process step for CMUT fabrication. Quality of wafer bonding usually determines the yield and robustness of CMUT devices. The type of the membrane material affects the difficulty level of wafer bonding process. Silicon-on-insulator (SOI) wafers have been generally used to construct the membrane material of CMUTs. The new material been introduced here is *'diamond'*. Unrivalled hardness and robustness, excellent thermal properties, high thermal conductivity and biocompatibility of the diamond material can be employed in the new generation CMUT devices for better performance and reliability.

In this section, characterization of diamond surface and direct wafer bonding experiments have been demonstrated. Silicon dioxide-to-diamond, silicon dioxide-to-silicon dioxide, diamond on PECVD (Plasma enhanced chemical vapor deposition) oxide-to-silicon dioxide, (HTO) diamond on HTO (High temperature oxide) oxide-to-silicon dioxide wafer bonding experiments have been performed and results are stated.

4.3.1 Parameters of Direct Wafer Bonding

Surface roughness, waviness, flatness and cleanliness are important paramaters for direct wafer bonding. Surfaces been brought into contact should be flat, clean and smooth for direct bonding. Surfaces that are in contact with each other initially form weak physical forces. This physical forces are converted into strong chemical forces with high temperature annealing. The force may be applied in order to be able to increase the contact area of the surfaces.

4.3.2 Wafer Bonding of Silicon Dioxide-to-Diamond

The first experiment about direct wafer bonding was between silicon on oxide and diamond-on-insulator (DOI) wafers. The direct bonding technique was applied to bond these two wafers. Thermal oxide generation and membrane cell pattering were done for the silicon wafer. Scanning electron microscopy (SEM) image of the DOI wafer is shown in Figure 4.17.

Wafer bow and roughness measurement results of both DOI and silicon on oxide wafer are given in Table 4.2. R_a is the arithmetic average of absolute value and R_q is the root mean

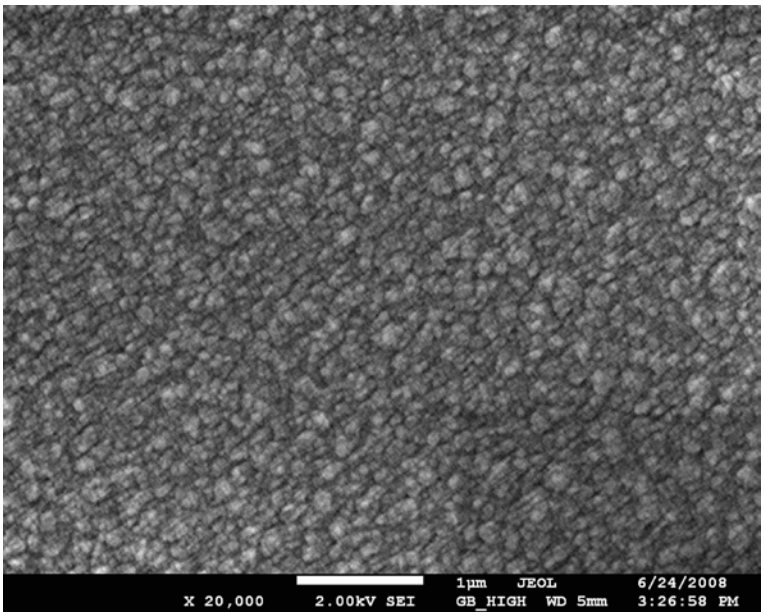

Figure 4.17: SEM image of the DOI wafer

squared value from surface roughness measurement.

Table 4.2: Bow and roughness measurements of DOI and silicon on oxide wafer

Wafers	Surface Roughness,Å	Bow Measurement, Radius μm
Si-SiO_2	R_a=6.7, R_q=8.4	R=41924,1056
Si-SiO_2-C	R_a=35,1, R_q=49	R=262757,4784
After Oxide Etch, Si-SiO_2	-	R=87031448

Full wafer bonding between DOI and silicon on oxide wafer was failed. Direct silicon to diamond bonding was potentially done with very small pieces (very small area) in the literature [64]. Required force for the direct bonding can be supplied for small areas. However, full wafer bonding between silicon dioxide and diamond may be potentially required tens of ton pressures with the perfect surface roughness of contact areas.

4.3.3 Wafer Bonding of Silicon Dioxide-to-Silicon Dioxide

CMUT devices with silicon dioxide membrane were fabricated by direct boning with SOI wafers. The silicon dioxide was used as a structural membrane material. The thermal oxide

was grown on silicon wafers in LPCVD furnace and RIE was applied to pattern the cavities for membrane cells. Before direct bonding process, thermally generated and pattered silicon on oxide wafer was cleaned and surface activated as shown in Table 4.3.

Table 4.3: Surface activation and cleaing of silicon on oxide wafers

Mixture	Duration	Temperature
$NH_4OH:H_2O_2:H_2O$ (0.25:1:5)	10 Minutes	75^oC
-	Rinse, 6 Minutes	-
-	Megasonic cleaning, 3 minutes	-
$HCl:H_2O_2:H_2O$ (1:1:6)	10 Minutes	75^oC
-	Rinse, 6 Minutes	-
-	Spin dry, 10 Minutes	-

After surface activation and cleaning, wafer bonding of silicon wafer with cavities and SOI wafer were implemented using wafer bonder (EVG 501) at 550^oC, under vacuum and 3500 N contact force for 7 hours. Annealing of the oxide bonds was done using THERMCO furnace at 1000-1100^oC.

CMUT devices with silicon dioxide membrane can be obtained using oxide-oxide bond approach. CMUT devices with oxide membranes are shown in Figures 4.18, 4.19, 4.20 and 4.21.

Silicon dioxide is a weak structural material for CMUT membranes. As shown in Figure 4.20 and 4.21, CMUT devices have many cracks and defects due to the weakness of silicon dioxide material. However, it is shown that CMUT devices with silicon dioxide membrane can be fabricated in spite of having low yield and reliability.

4.3.4 Wafer Bonding of Diamond on PECVD Oxide-to-Silicon Dioxide

Full wafer bonding between diamond and oxide surfaces can be considered as a difficult process. Therefore, the surface of DOI wafers was covered with thin oxide layer in order to obtain oxide-oxide surface connections for direct bonding. Besides, the insulation layer between the membrane and bottom electrode will be formed by means of the covered thin

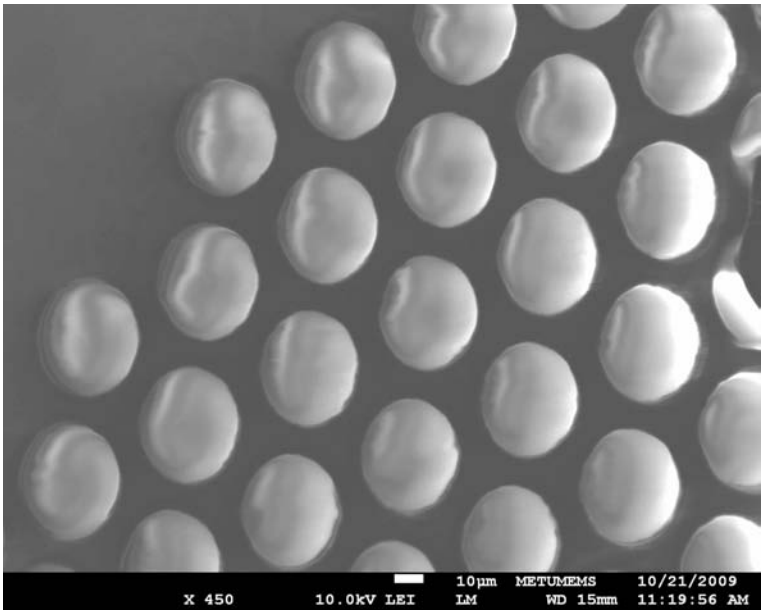

Figure 4.18: SEM image of silicon dioxide membrane CMUT cells

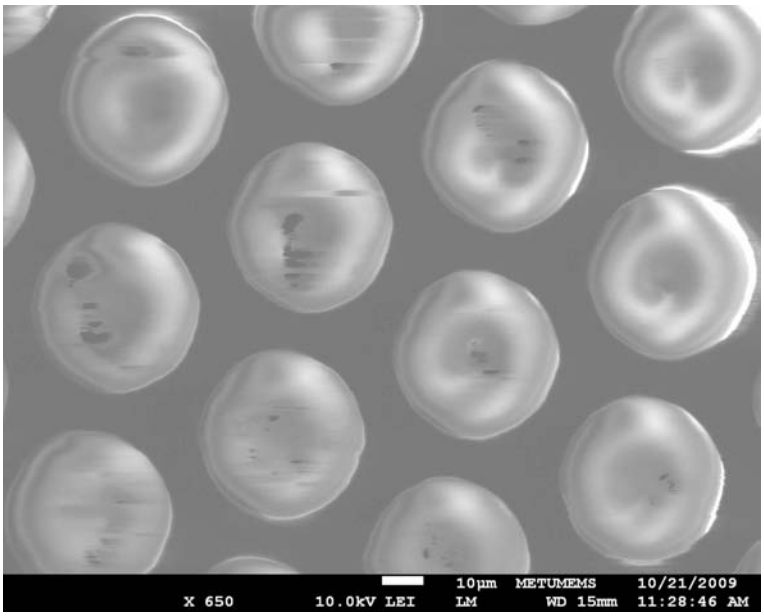

Figure 4.19: SEM image of silicon dioxide membrane CMUT cells

oxide layer on the diamond surface. Thickness, surface roughness, stress and wafer bow characterization of DOI wafers were done before the oxide deposition.

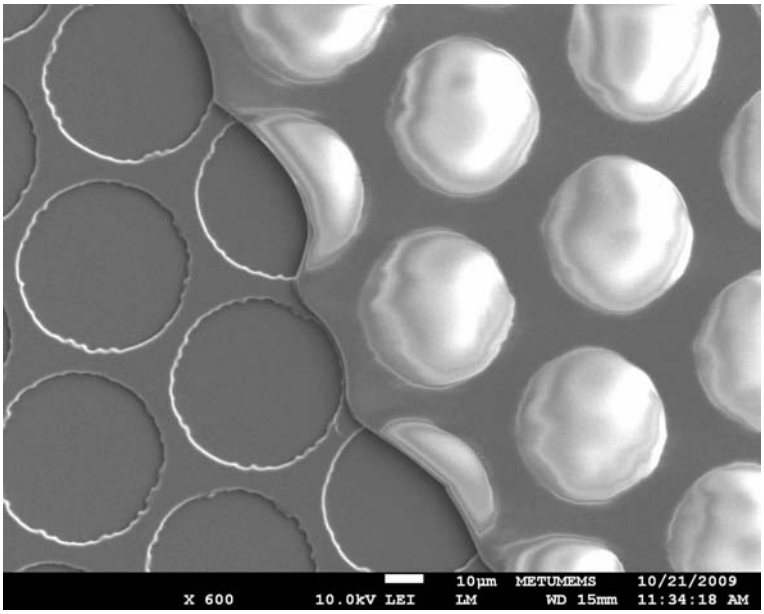

Figure 4.20: SEM image of cracks on CMUT devices with silicon dioxide membrane

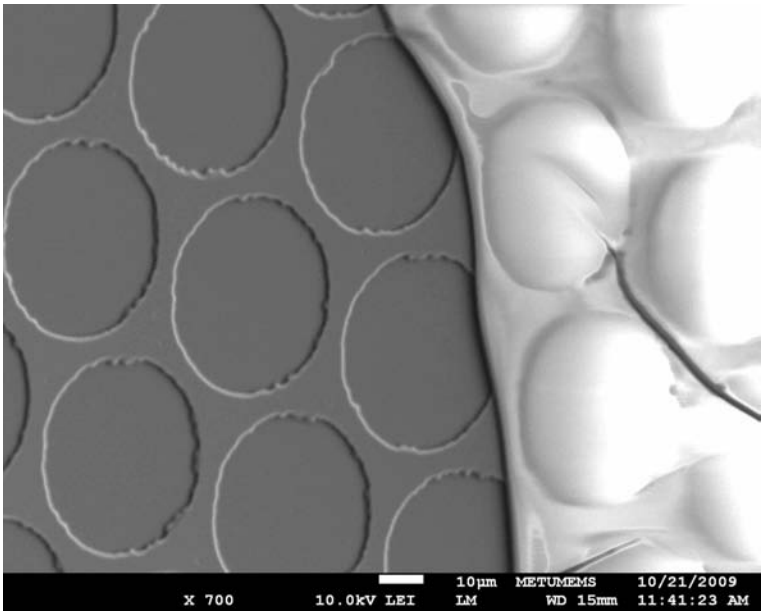

Figure 4.21: SEM image of cracks on CMUT devices with silicon dioxide membrane

4.3.4.1 Characterization of DOI Wafers

Thickness measurements were performed by V-VASE ellipsometer, the stress and wafer bow measurements were done by Toho FLX-2320-S equipment, and surface roughness of DOI

wafers were measured by MFP-3D AFM equipment.

4.3.4.2 Thickness Characterization of DOI Wafers

The thickness measurement of the DOI wafers were done using V-VASE ellipsometer (Lincoln, NE,US). Refractive index for diamond material was used 2.29. Thickness scan directions of wafers were performed as shown in Figure 4.22.

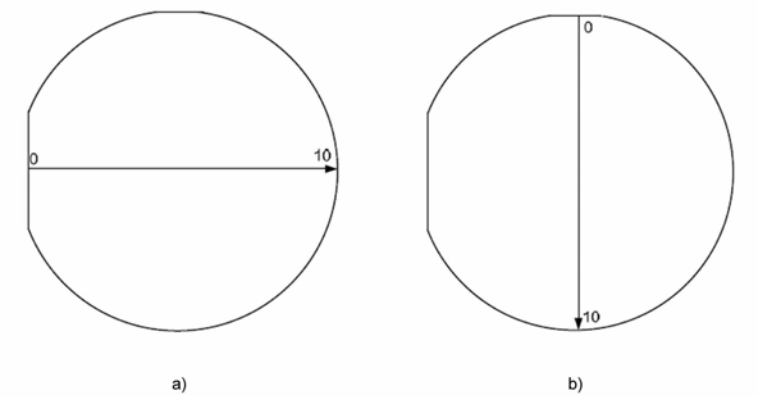

Figure 4.22: a) Left-to-right (LR) thickness scan, b) Top-to-bottom (TB) thickness scan

The thickness measurement of 2 DOI wafers are shown in Figure 4.23.

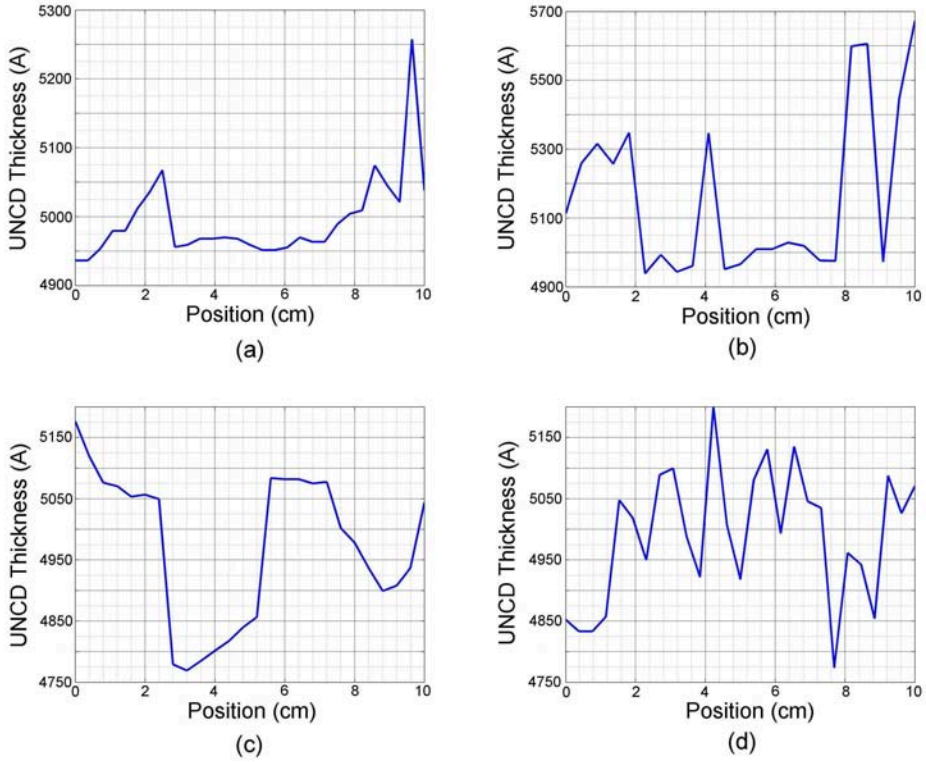

Figure 4.23: a) First wafer LR thickness measurement, b) First wafer TB thickness measurement, c) Second wafer LR thickness measurement, d) Second wafer TB thickness measurement

Thickness variations of diamond layer on DOI wafers affect the electrostatic pressure of CMUT devices. Thickness variations on same wafer may cause different electrostatic pressures on different cells in the same CMUT device. This is an undesired effect for the performance of the device. Deposited oxide layer and CMP process are expected to be able to potentially solve this thickness variations on the diamond layer as well as the membrane structure.

4.3.4.3 Stress Measurements of Diamond Wafers

Wafer bow and stress measurements were done using Toho FLX-2320-S equipment (Toho Technology Corporation, Japan). Tensile or compressive stress parameters are crucial for CMUT membrane structures. CMUT membranes can be buckled or broken by compressive stress. However, CMUT devices can operate under the effect of tensile stress with higher

resonance frequencies due to stress parameters. Stress measurement of DOI wafer being close to the required stress value is given in Figure 4.24.

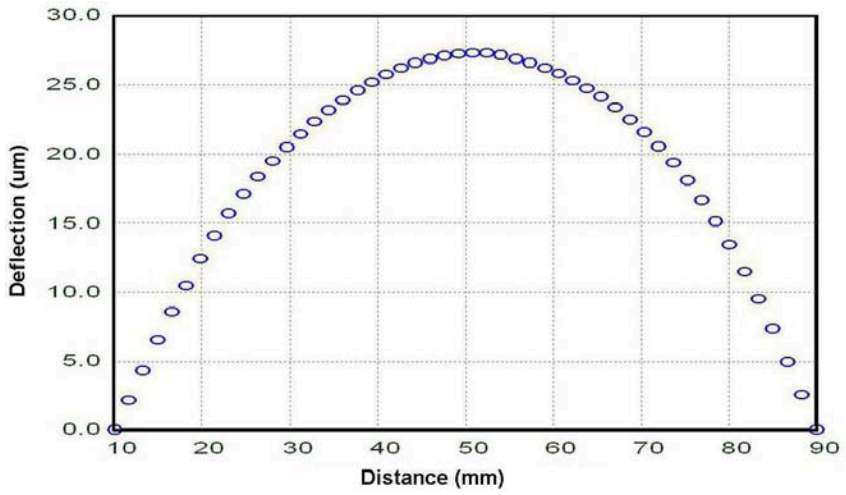

Figure 4.24: Stress and wafer bow measurement of DOI wafer. Wafer bow: 27 μm, Tensile stress: 22 MPa

Stress free wafers are the best choice for the membrane structure of CMUT devices. DOI wafers with compressive stress are not acceptable for the microfabrication of CMUTs. Wafers with tensile stress can be potentially used as a membrane structure with higher resonance frequency. DOI wafers that have high compressive and tensile stresses are shown in Figure 4.25.

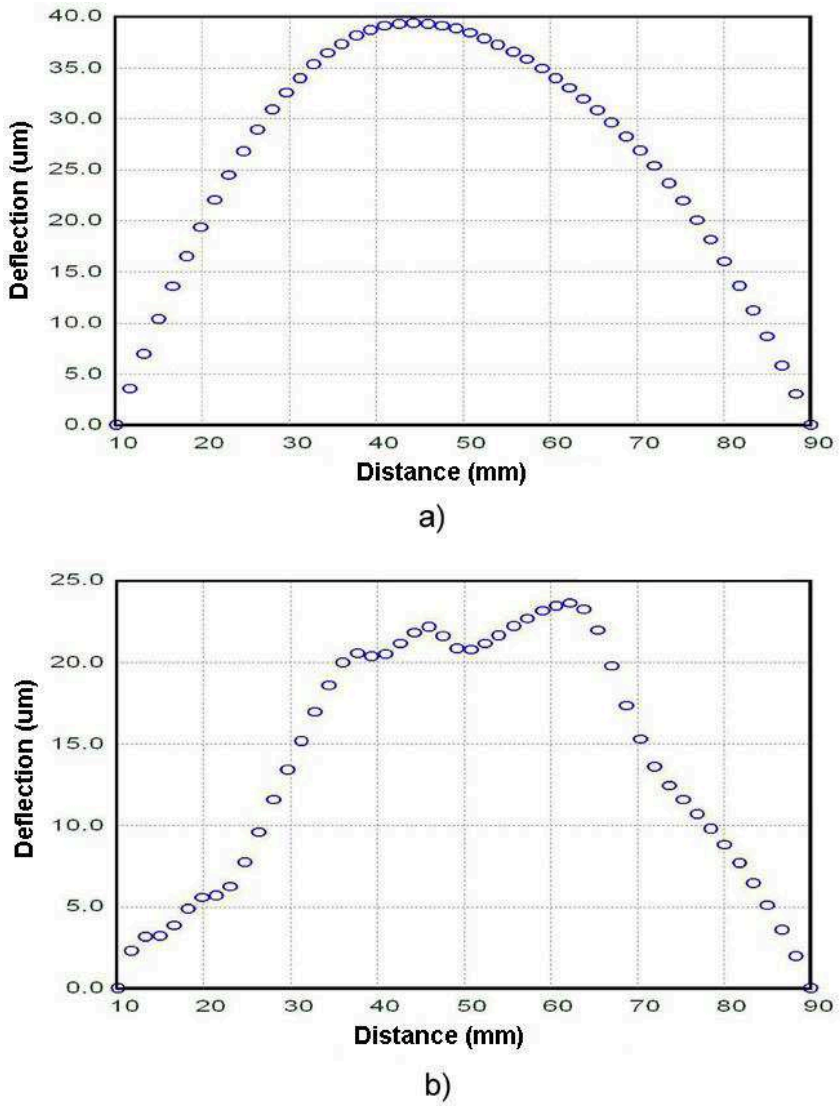

Figure 4.25: a) DOI wafer with compressive stress. Wafer bow: 39 μm, Compressive stress: 217 MPa, b) DOI wafer with tensile stress. Wafer bow: 37 μm, Tensile stress: 160 MPa

4.3.4.4 AFM Measurements of Diamond Wafers

Surface roughness of DOI wafers were determined by using AFM measurements. MFP-3D (Asylum Research, Santa Barbara, US) AFM equipment from Bilkent University was used for the surface roughness measurements. Surface roughness is one of the most crucial parameters for direct bonding. Wafers are expected to have surface roughness lower than 1 nm R_a for the proper bonding operation. DOI wafers had already been polished by Advance Diamond Technologies Company before shipping. Some diamond wafers had slurry remainings that

increased the surface roughness. AFM measurement of diamond wafer with high surface roughness is shown in Figure 4.26.

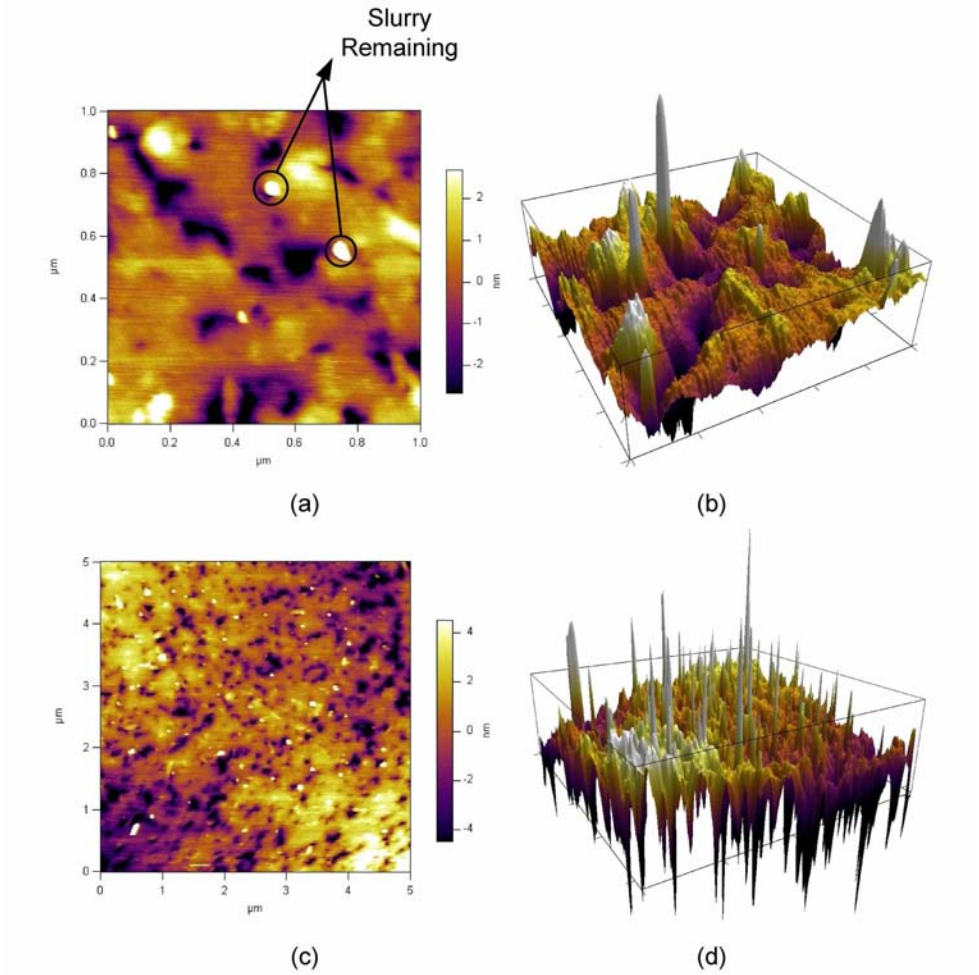

Figure 4.26: a) 2D AFM measurement view of UNCD layer 1 μm x 1 μm, R_q=1.325 nm, R_a=0.907 nm, b) 3D AFM measurement view of UNCD layer 1 μm x 1 μm, c) 2D AFM measurement view of UNCD layer 5 μm x 5 μm, R_q=2.227 nm, R_a=1.641 nm, d) 3D AFM measurement view of UNCD layer 5 μm x 5 μm

Regardless of deposition of oxide layer, surface characteristics of DOI wafers are crucial parameters for wafer bonding. Since, oxide layer is going to be polished and approximately 100 to 200 nm thickness of oxide will remain for direct bonding process. AFM measurement of a qualitative wafer considering its surface roughness is given in Figure 4.27.

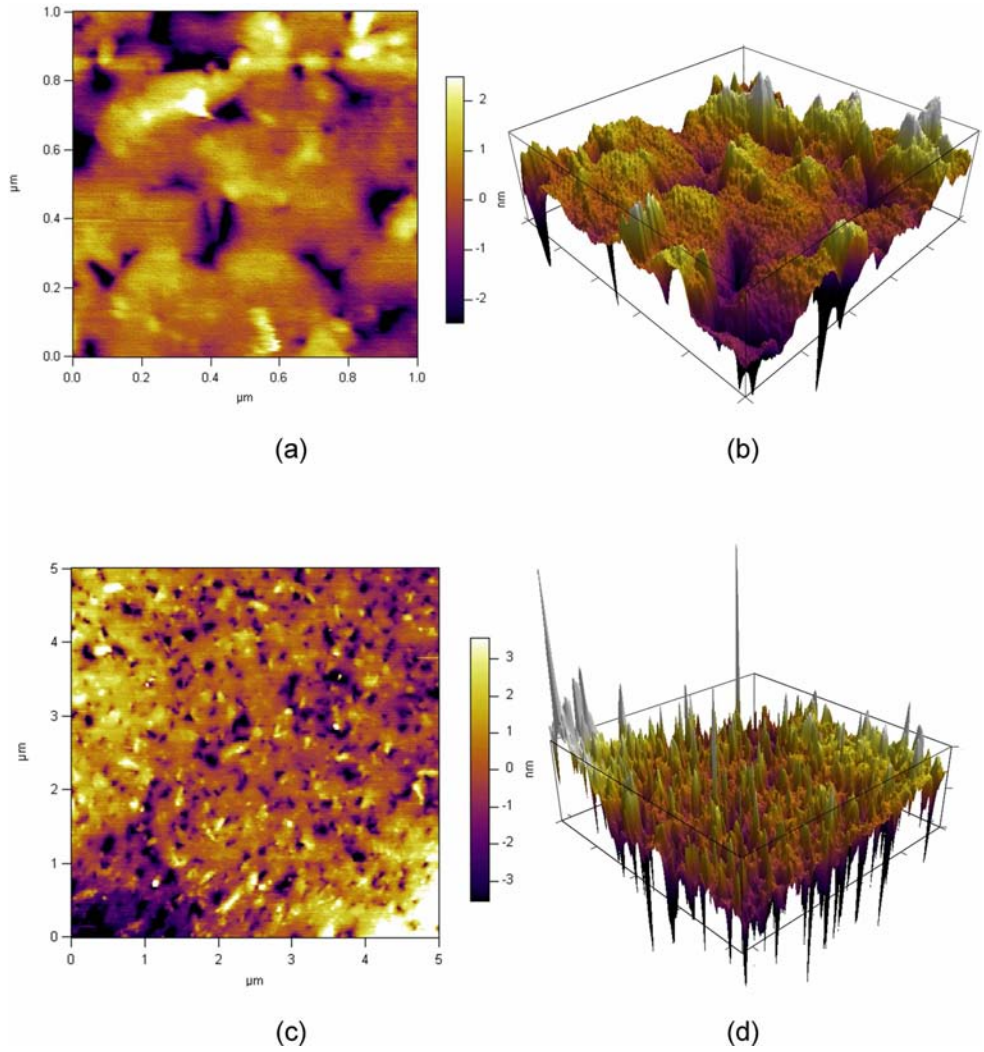

Figure 4.27: a) 2D AFM measurement view of UNCD layer 1 μm x 1 μm, R_q=1.222 nm, R_a=0.833 nm, b) 3D AFM measurement view of UNCD layer 1 μm x 1 μm, c) 2D AFM measurement view of UNCD layer 5 μm x 5 μm, R_q=1.757 nm, R_a=1.231 nm, d) 3D AFM measurement view of UNCD layer 5 μm x 5 μm

4.3.4.5 Characterization Summary

DOI wafers were characterized according to the thickness, stress, and surface roughness of their diamond layer. Additional parameter that has not been mentioned throughout the characterization part is the wafer cleanliness. This parameter affects the quality of the direct bonding. Wafer eliminations related to cleanliness were accomplished according to AFM measurement results. Undesired roughness values obtained from AFM measurements may be caused by slurry remaining. The wafers that do not provide sufficient conditions have to be eliminated for proper direct bonding process.

The wafers that met the desired specifications were used in CMUT fabrication process. PECVD oxide deposition and wafer bonding process were performed on these wafers in order to obtain CMUT devices with diamond membranes.

5000 Å PECVD oxide was covered on UNCD DOI wafers at 300^{o}C. Chemical mechanical polishing (CMP) service was provided from Axus Company in order to obtain better surface roughness on the PECVD oxide layer for direct bonding process. The thickness value of 5000 Å was polished remaining 1000-2000 Å on top of the DOI wafer. Surface roughness measurement (Atomic force microscope, AFM, Bilkent University) of PECVD oxide layer after CMP process is shown in Figure 4.28 and surface roughness measurement of bare silicon wafer is given in Figure 4.29 for better comparison.

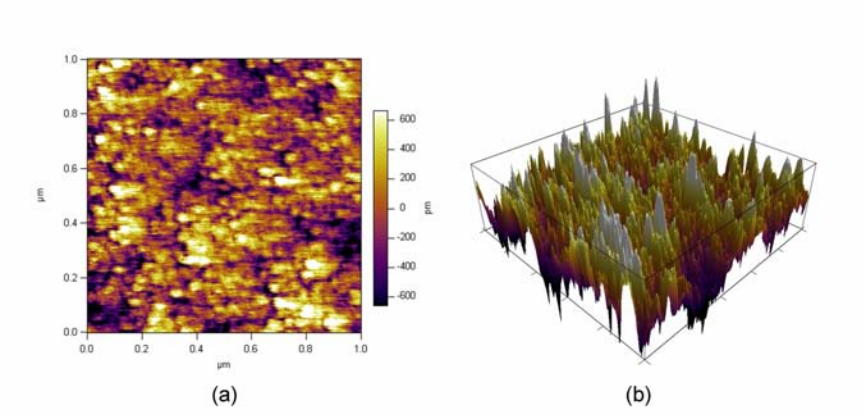

Figure 4.28: a) AFM measurement of PECVD oxide in planar view 1 μm x 1 μm, b) AFM measurement of PECVD oxide in 3D view 1 μm x 1 μm, R_q= 0.327 nm, R_a= 0.255 nm

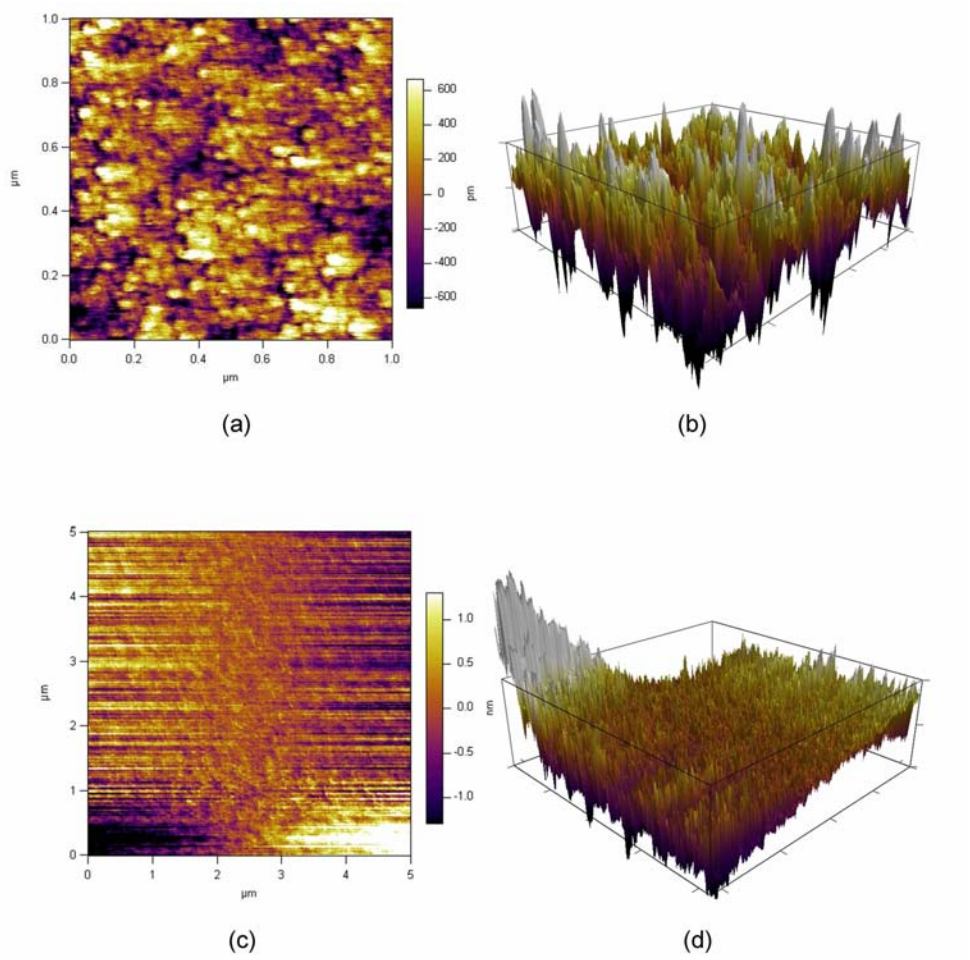

Figure 4.29: a) AFM measurement of bare silicon wafer in planar view 1 μm x 1 μm, R_q=0.101 nm, R_a=0.080 nm, b) AFM measurement of bare silicon wafer in 3D view 1 μm x 1 μm, c) AFM measurement of bare silicon wafer in planar view 5 μm x 5 μm, R_q=0.214 nm, R_a=0.167 nm, d) AFM measurement of bare silicon wafer in 3D view 5 μm x 5 μm

Bare silicon wafer has R_a value which is lower than 0.2 nm. This surface roughness value is sufficient for direct bonding. Polished PECVD oxide layer has R_a value of 0.255 nm which is really close to the surface quality of the bare silicon wafer. The quality of diamond on PECVD oxide surface meet the required surface roughness specification for direct bonding process.

Diamond on oxide-to-silicon dioxide wafer bonding process was performed by EV Group from Austria. This was the first successful bonding process between diamond on oxide surface and silicon dioxide surface for the CMUT devices with diamond membranes. In this

fabrication process, the mask that only has single CMUT designs was used in order to test the quality of bonding service provided from EVG-Austria. Besides, single CMUT designs have more membrane structures than 1-D CMUT designs. Therefore, they have better potential to feedback the quality of bonding on membrane structures.

Fabricated single CMUT devices with diamond membranes are shown in Figures 4.30, 4.31.

The first CMUT devices with diamond membranes have been fabricated using diamond on PECVD oxide layer. However, the gas release problem was reported at the bonding process (550^oC) due to the deposited PEVCD oxide layer at 300^oC. Released gas from oxide layer decreased the bonding quality of the wafers. On the other hand, the membranes were buckled up due to this released gas into the membrane cavities. Under normal circumstances, membranes are expected to be buckled down under the atmospheric pressure. Profilometer was used to capture the membrane shapes of CMUT devices as shown in Figure 4.32.

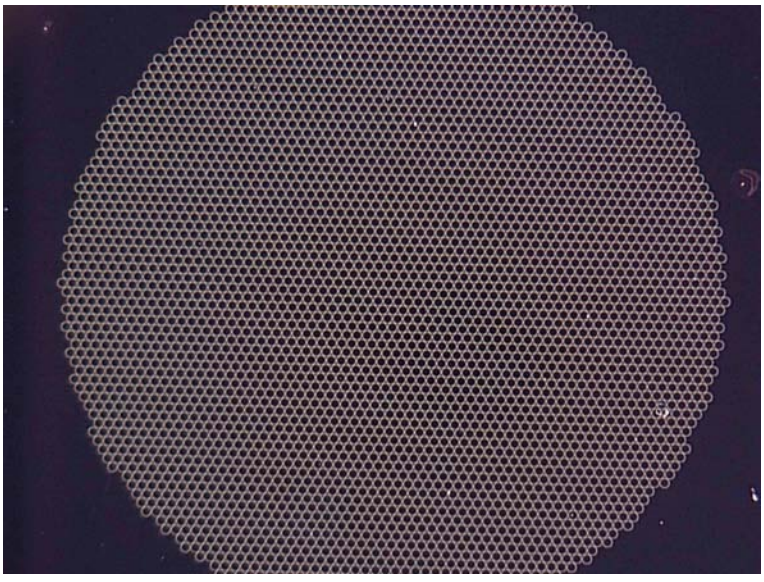

Figure 4.30: The microscope image of robust 72 μm single CMUT

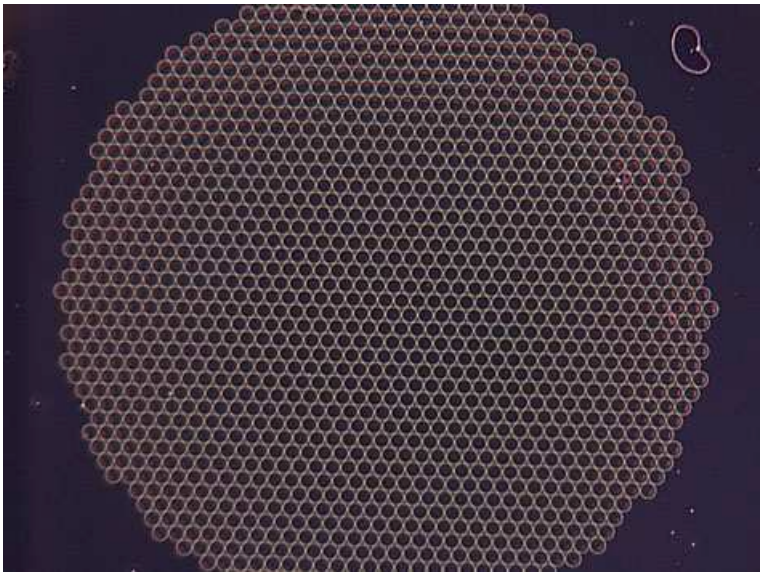

Figure 4.31: The microscope image of robust 120 μm single CMUT

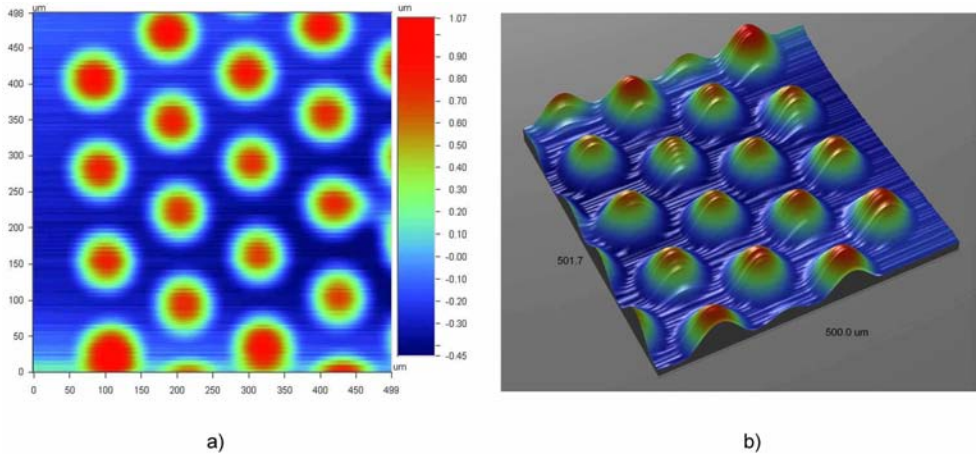

Figure 4.32: a) The planar view of 120 μm single CMUT membranes, b) The 3D Dektak image of 120 μm single CMUT membranes

4.3.5 Wafer Bonding of Diamond on High Temperature Oxide (HTO)-to-Silicon Dioxide

Another method to cover the diamond surface with oxide material is HTO process. This process is conducted at approximately 900^{o}C. Gas molecules are not released during bonding

process under 550^{o}C, because of the high temperature process of oxide layer. Gas release problem was potentially solved with using HTO process to obtain oxide layer on the diamond surface.

UNCD diamond wafers were provided from Advanced Diamond Technologies (ADT) Company for the CMUT fabrication. UNCD diamond layer was deposited on directly silicon substrate with the thickness of 10000 Å.

4.3.5.1 HTO Deposition, CMP and Plasma Activation for Wafer Bonding

The required conditions for deposition of HTO layer are keeping the wafers in LPCVD furnace of 850^{o}C containing SiH_2Cl_2+N_2O gases and applying 400 mTorr pressure. The HTO layer with a thickness of 0.5 μm was deposited on diamond wafers. The surface roughness of HTO layer, which was chemically polished for 15 seconds, was measured on test wafers and it is shown in Figure 4.33. 0.963 R_q and 0.725 R_a values were obtained with AFM measurement from 5 μm x 5 μm area. This surface roughness value was sufficient for proper direct bonding. The service from Axus Company was provided for CMP process in order to obtain HTO layer with a thickness of 0.1-0.2 μm and surface roughness of 0.3 nm (R_a).

Plasma activation which enables the low temperature direct bonding was applied to the surface of the diamond wafers. EVG810LT activation system was used for surface activation with N_2 plasma. EVG520IS bonding system performed the wafer bonding process under the effect of high vacuum (10^{-4} mbar) with a piston force 10 kN. Then, bonded wafers were heated up to 550^{o}C and were kept for 7 hours.

After the proper bonding operation, silicon wafer etching process should be done in order to obtain membrane structures with cavities.

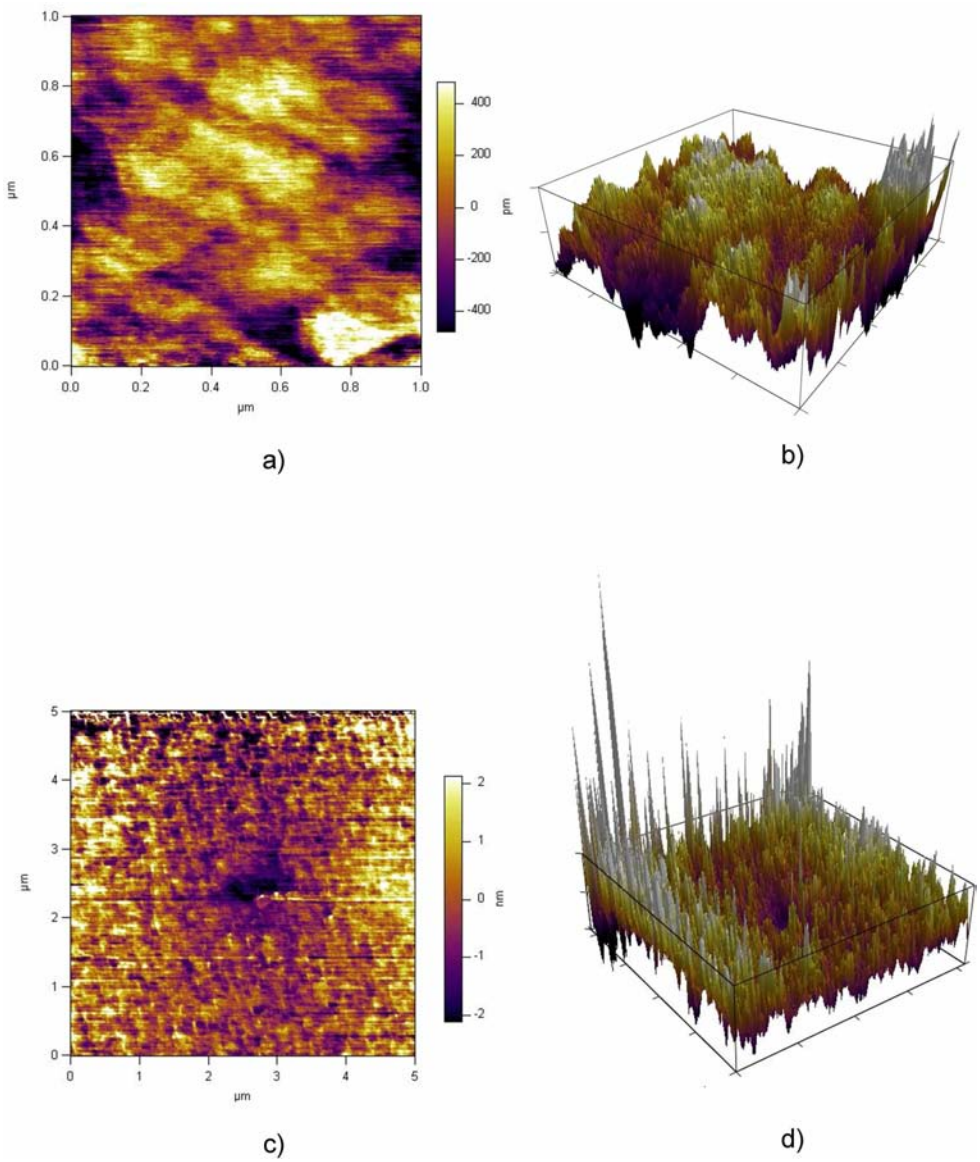

Figure 4.33: a) 2D AFM measurement view of polished HTO layer 1 μm x 1 μm, b) 3D AFM measurement view of polished HTO layer 1 μm x 1 μm, c) 2D AFM measurement view of polished HTO layer 5 μm x 5 μm, d) 3D AFM measurement view of polished HTO layer 5 μm x 5 μm

4.4 Silicon Wafer Etching and Metal Sputtering

4.4.1 Silicon Wafer Etching

Silicon substrate thickness was decreased from 500 μm to 100 μm with grinding in order to have faster chemical membrane releasing. Then, the bottom of the silicon substrate that have cavities was covered with 1 μm PECVD oxide layer for protection from chemical etching. Tetramethylammonium hydroxide (TMAH) was applied at 90^{o}C to etch the 100 μm silicon layer for about 3 hours. Reflux condenser for TMAH etching process eliminates the evaporation of mixture and supports safer process for long term. Process setup is shown in Figure 4.34.

Figure 4.34: TMAH process setup

4.4.2 Etching of Diamond

Cavities supplying the connection for the ground electrodes should be patterned before the metal sputtering. With the second masking process, metal cavities were shaped. PECVD oxide layer was deposited on to the diamond surface and patterned as a protection layer for electrode etching. Connection cavities to the ground substrate were etched with using RIE system. Oxide and diamond layers were etched with $CHF_3\backslash CF_4$ and ICP-O_2 plasma, respectively. Consequently, the metal connection cavities for ground electrode was performed.

4.4.3 Metal Sputtering

In this process step, aluminum was covered and patterned on to the diamond surface to obtain ground and positive electrodes. Aluminum layer was patterned by metal mask. The metal mask of 1-D CMUT array with 72 μm is given in Figure 4.35. This figure shows just the small portion of the total metal mask.

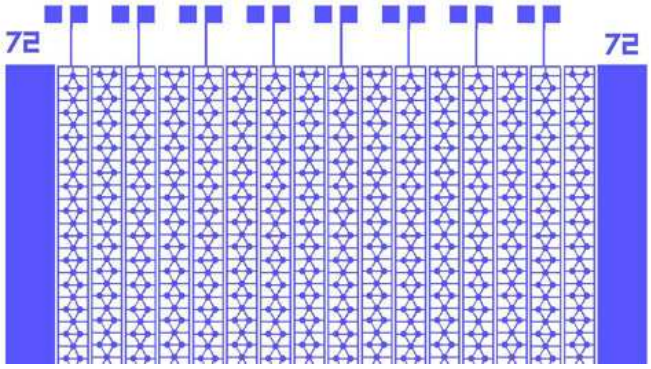

Figure 4.35: Metal mask of 1-D CMUT array with 72 μm

4.4.4 Dicing and Wire Bonding

Full wafer photoresist covering was performed before the dicing process. Covered photoresist layer protected CMUT devices from any possible damages. After this process, CMUT devices were connected to fanout boards by wire bonding with gold (Au) material.

4.5 Microfabrication Summary of CMUTs with Diamond Membranes

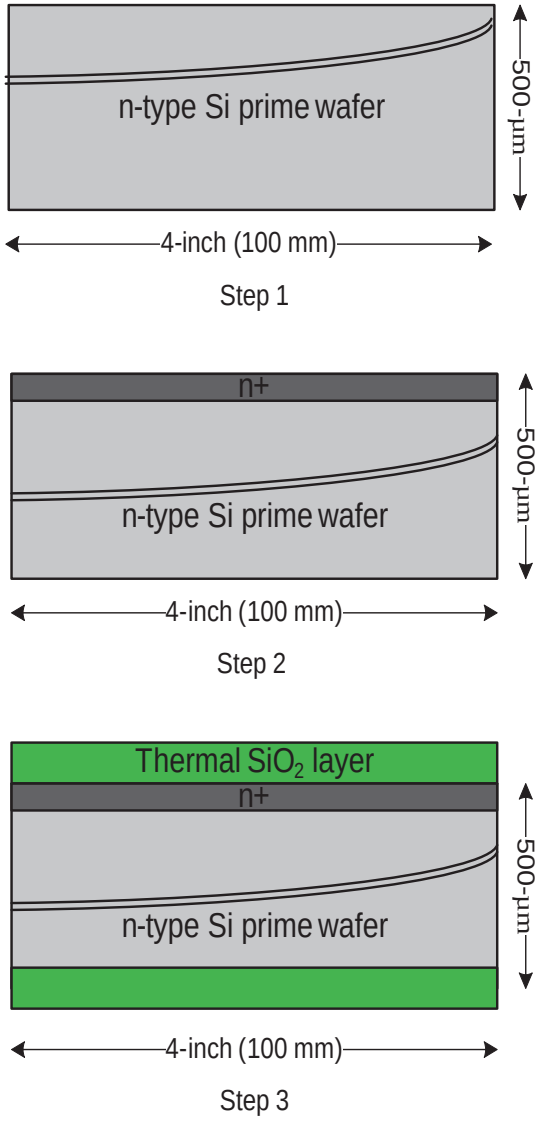

Figure 4.36: Process steps 1 to 3, Step 1: Bottom wafer: n-type silicon wafer, Step 2 : Bottom wafer: P doing for conductive surface, Step 3 : Bottom wafer: Thermal oxide growth

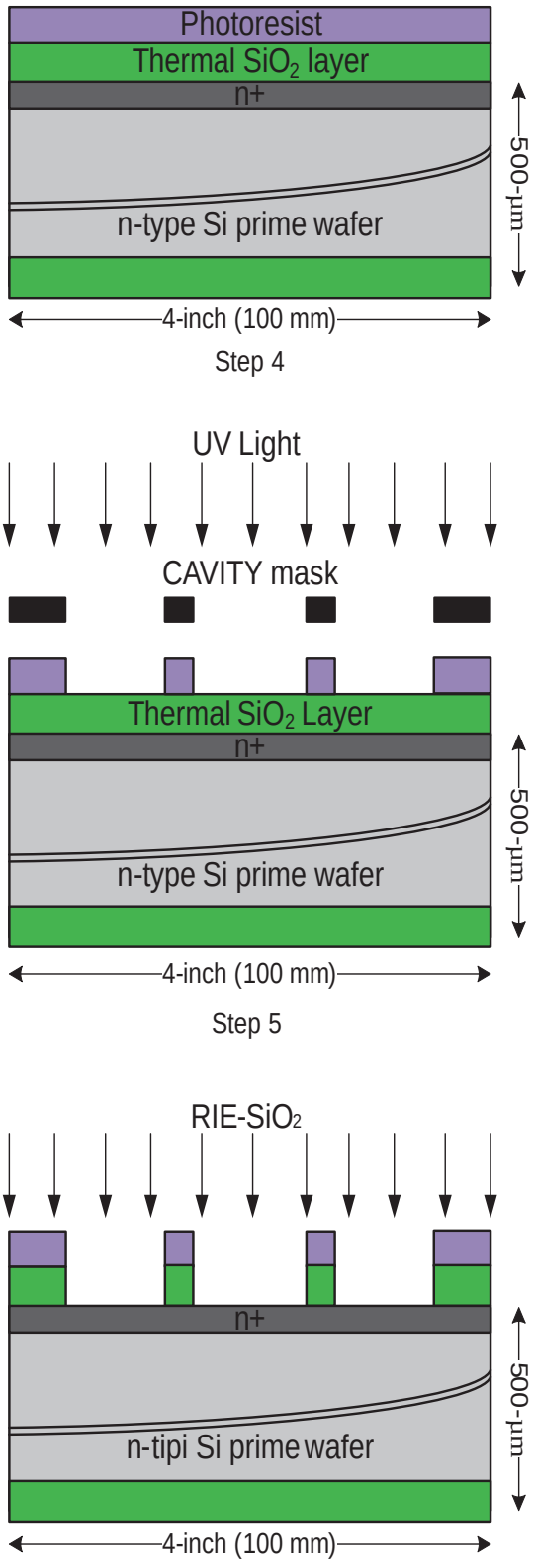

Figure 4.37: Process steps 4 to 6, Step 4 : Bottom wafer: Photoresist covering, Step 5 : Bottom wafer: Photoresist patterning with cavity mask, Step 6 : Bottom wafer: SiO_2 etching with RIE

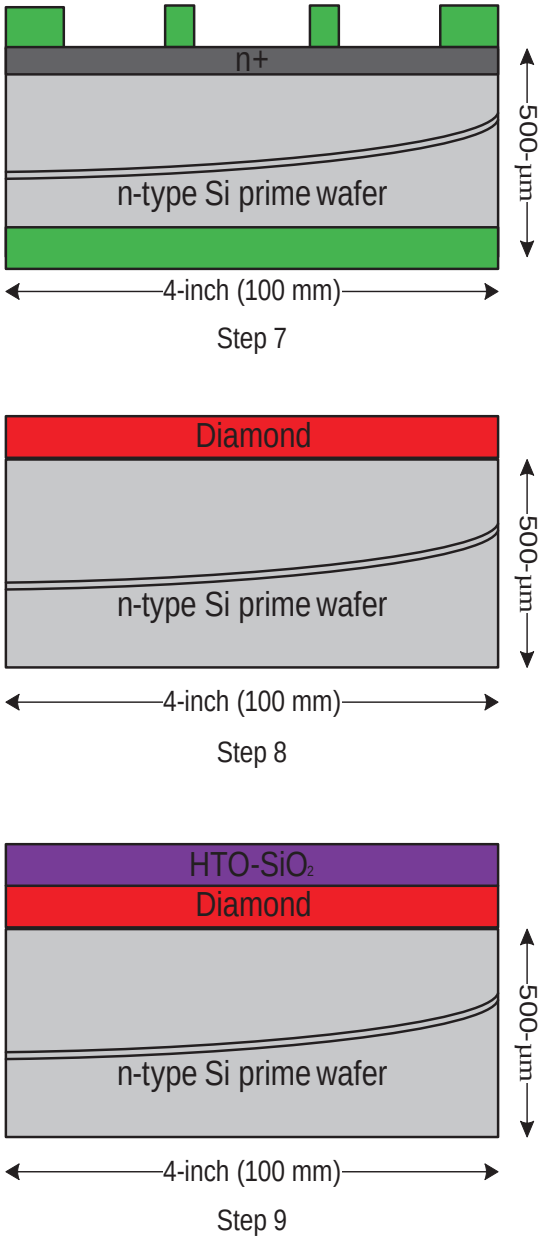

Figure 4.38: Process steps 7 to 9, Step 7 : Bottom wafer: Photoresist stripping with O_2 plasma, Step 8 : Top wafer: Silicon wafer with diamond layer, Step 9 : Top wafer: HTO-SiO_2 deposition in LPCVD furnace

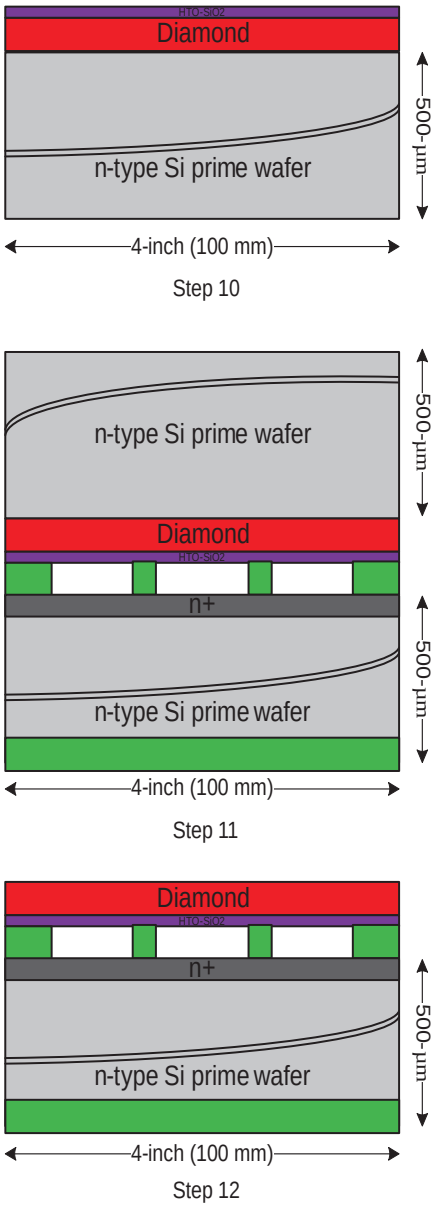

Figure 4.39: Process steps 10 to 12, Step 10 : Top wafer: Satisfy the surface roughness of HTO-SiO_2 with CMP, Step 11 : Bonding of wafers under vacuum at 550^{o}C with plasma activation, Step 12 : Bonded wafers: Total TMAH etching of 525 μm silicon layer of top wafer

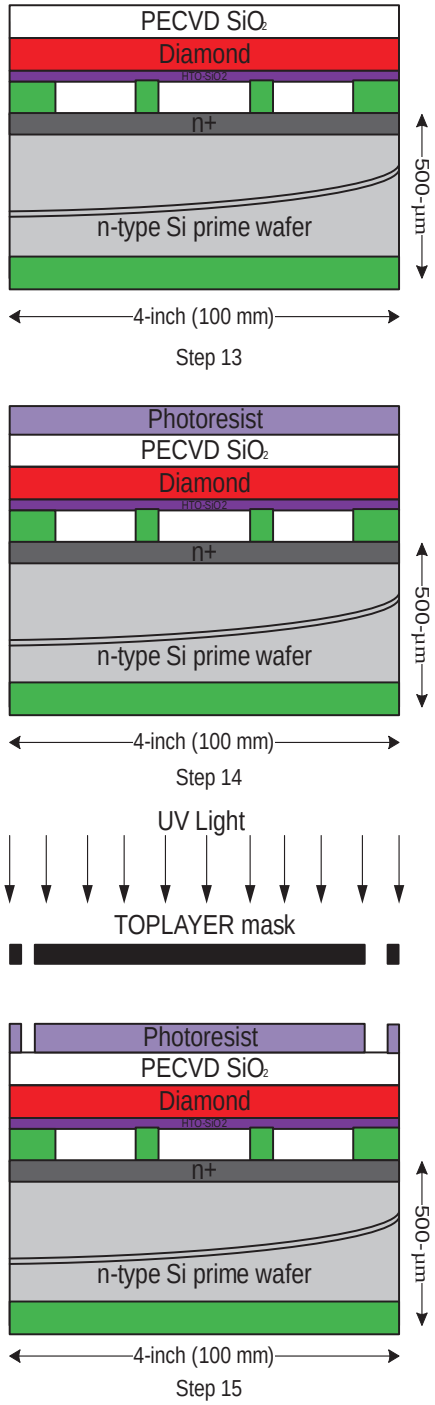

Figure 4.40: Process steps 13 to 15, Step 13 : Bonded wafers: PECVD SiO_2 covering of diamond surface, Step 14 : Bonded wafers: Photoresist covering, Step 15 : Bonded wafers: Photoresist patterning with toplayer mask

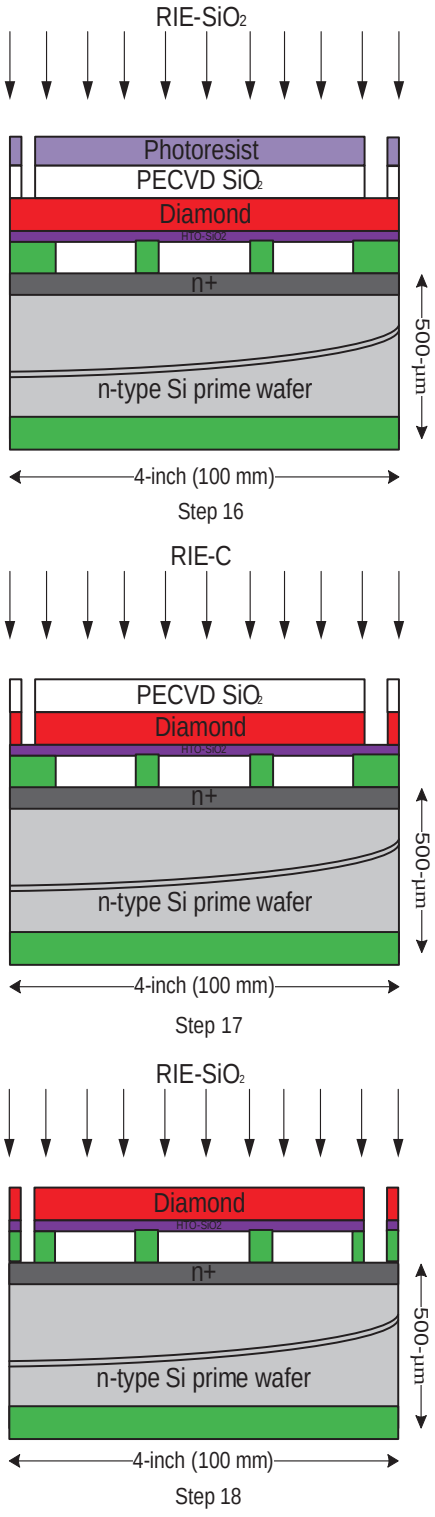

Figure 4.41: Process steps 16 to 18, Step 16 : Bonded wafers: SiO_2 etching with RIE, Step 17 : Bonded wafers: Diamond etching with RIE and photoresist stripping, Step 18 : Bonded wafers: SiO_2 etching with RIE

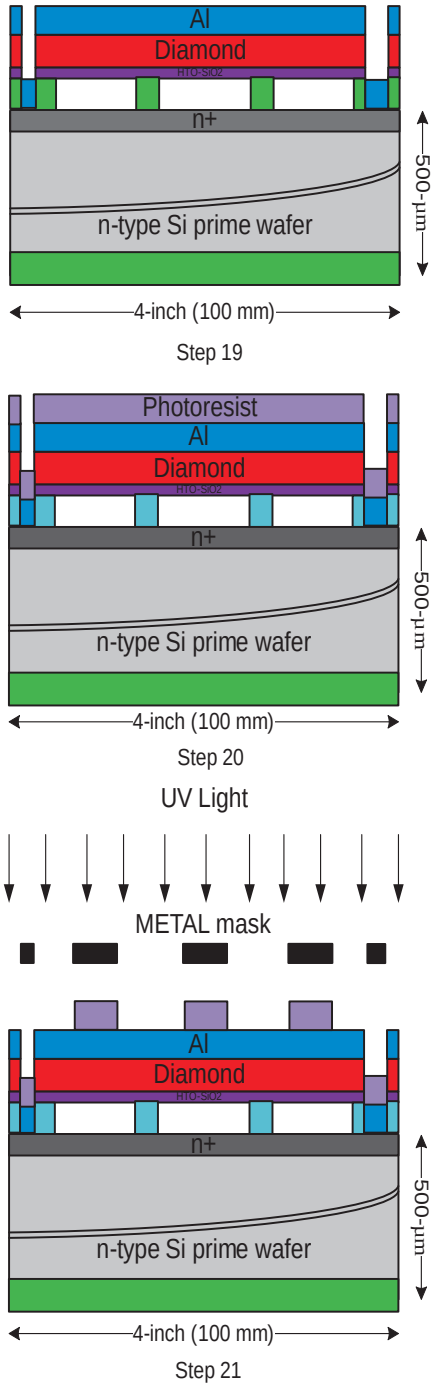

Figure 4.42: Process steps 19 to 21, Step 19 : Bonded wafers: Aluminum covering, Step 20 : Bonded wafers: Photoresist covering, Step 21 : Bonded wafers: Photoresist patterning with metal mask

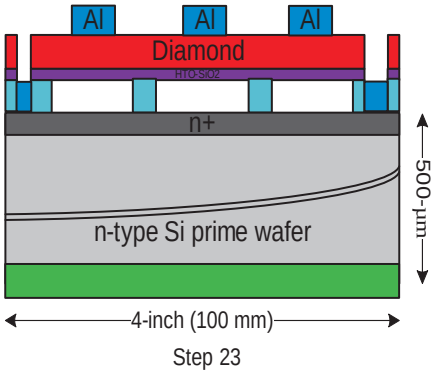

Figure 4.43: Process Step 22 : Bonded wafers: Aluminum etch with chemicals and photoresist stripping with O_2 plasma

The first diamond based capacitive micromachined ultrasonic transducers' microfabrication steps, which were developed after condensed research and improvement, are as in the way given in following figures and explained in Table A.1. First of all, in order to make it more conductive, n- type Si wafer's surface was doped with P-type dopant. This doping step enables to make ohmic contacts for ground connections. The doping process was conducted with $POCl_3$ and O_2 gases at 1050^oC for one hour in doping furnaces. After this process step, the conductivity of the surface was approximately measured 1 ohm\□. Afterwards thermal oxide was generated. The thickness of the thermal oxide is defined with the height of the gap at the design. Thermal oxide is shaped with lithography of the first mask and reactive ion etching (CHF_3/CF_4).

Ultrananocrystalline stress free diamond covered Si top wafer is provided for our process. One of the most crucial properties of diamond used for membrane is the stress value. Optimum value is 50 MPa, higher than this stress value is not suitable for our design procedures.

High temperature oxide is grown on diamond wafer in LPCVD furnace with the reactions of SiH_2Cl_2 and N_2O at 850^oC. This kind of oxide has similar electrical features like thermal oxide. The surface roughness of HTO diamond is decreased under 0.3 nm values with CMP process. Lower than 0.5 nm surface roughness value is necessary for molecular bonding. The required conditions for bonding are keeping the wafers in a furnace of 550^oC, applying 10 kN force on top of the wafer for 7 hours under ultra high vacuum. After conducting these conditions, N_2 plasma activated diamond wafer with decreased surface roughness and patterned thermal oxide grown on Si wafer can be bonded. When the bonding process is done, Si wafer supporting diamond is annihilated totally with chemical and mechanical polishing techniques, remained structure is our diamond membrane. Diamond is covered with PECVD SiO_2 in order to prevent the possible damages caused by ICP-O_2 plasma. SiO_2 covered diamond is patterned with second masking process and etched by RIE (CHF_3/CF_4). Patterned SiO_2 layer is used as protection layer during diamond etching. After diamond etching with ICP-O_2 plasma, another RIE process is applied to etch the bottom SiO_2 until reaching the silicon substrate. The whole surface of the wafer is covered with aluminum in order to pattern ground and top metal electrodes using third mask. Processed wafer is covered with photoresist, as a protection layer, before dicing step. After this step photoresist is completely removed from wafer surface. As final step, CMUT devices are stuck on PCB using epoxy and signal connections are wired to PCB terminals with Au material.

CHAPTER 5

CIRCUIT DESIGN AND PCB IMPLEMENTATION FOR FOCUSING ULTRASOUND

5.1 Phase Shifter Circuit Design

1-D CMUT array has 16 elements consisting of circular cells. Phase shifter circuit is going to be used to focus ultrasonic waves that are generated by each element. This focal point is located at an axial distance on the normal to the 1-D CMUT center plane.

The main operation of the focusing electronics is to adjust relative phase differences between the sinusoidal signals which are applied to the elements of CMUT device. In this way, 16 elements of CMUT focus on a desired point. The focusing schematic of 1-D CMUT with 16 elements is shown in Figure 5.1. The focal point is designated according to the phase differences between sinusoidal signals that are affected by the type and temperature of the propagation medium.

$$d^2 = f^2 + \left[\frac{a}{2}\left(n - \frac{1}{2}\right)\right]^2 \tag{5.1}$$

Where 'f' is the distance from focal point to CMUT device, 'a' is the width of the single CMUT element and 'd' is the distance that can be calculated by using Equation 5.1. (n : Number of the CMUT elements between the center point of device and determined CMUT element).

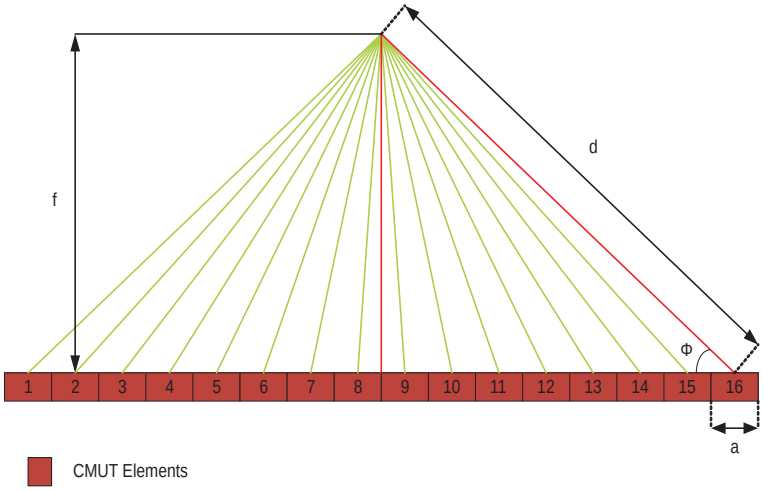

Figure 5.1: The example of the focusing point using 16 elements of 1-D CMUT

$$t = \frac{d}{v} \tag{5.2}$$

Where 'v' is the propagation velocity of the ultrasonic wave in a medium, 't' is the travel time of the ultrasonic wave from CMUT element to focal point. The travel time can be calculated using Equation 5.2.

Ultrasonic fields can be categorized into two regions: Near and Far fields. Near field is located near the transducer surface and every source of acoustic energy will be effective individually in this region. Therefore, this region may not be used for focusing process. The length of the near field depends on the diameter of the emitting sources and the propagation medium (5.3).

$$Z = \frac{D^2}{4\lambda} \tag{5.3}$$

Where 'D' is the diameter of the acoustic source, 'λ' is the wavelength of the signal and 'Z' is the length of the near field. The zone beyond the 'Z' is called far field. Every source of acoustic energy can be considered as a single source and propagation of acoustic waves behave as a single source excitation. Intensity of the acoustic wave varies inversely with the distance along the axis from transducer surface. Phase shifting electronics should be adjusted

in order to obtain focal point in far field region.

The equations stated in 5.1, 5.2, 5.3 are utilized in order to maintain phase differences between the AC signals in order to obtain reasonable focal point coordinates. The focal point was located in far field region due to the required single source behavior of the discrete CMUT elements. The calculated values are shown in Table 5.1. Focal point is 4.47 mm away from CMUT surface. '1–2' presents the calculated phase differences between the first and second signals that are used to excite first and second elements of the 1-D CMUT array.

Table 5.1: Calculated Travel Time Differences

Variables				
C (m/s)	D (μm)	F (MHz)	λ (μm)	Focus (mm)
1462.5	200	3	487.5	4.47

Travel Time Differences (ns)						
1–2	2–3	3–4	4–5	5–6	6–7	7–8
40.85	35.44	28.84	24.08	18.18	12.18	6.11

Travelling times of the ultrasonic waves that are generated by each element are calculated for the focal point and the phase differences between sinusoidal signals are found. The travelling times of the ultrasonic waves have information about the phase differences. The precision of the phase shifter electronics can be changed according to the location of the focal point. Closer focal points to the surface of device require high precision of phase shifting among the signals. Example of the phase shifting is shown in Figure 5.2.

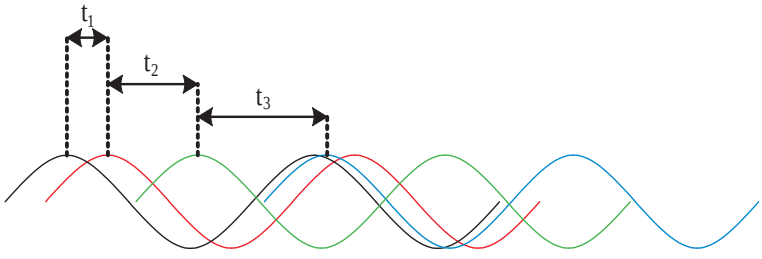

Figure 5.2: The example of the sinusoidal signals in difference phases

t_1, t_2, t_3 show the time differences between sinusoidal signals. Phase differences between

the signals can be adjusted for different focal points. The design of the focusing electronics supports 1 to 6 MHz frequency range and 15 $V_p - p$ output voltage and adjustable phase differences between 8 channel sinusoidal signals. This design has been produced and tested.

Basic block of the phase shifter electronics is shown in Figure 5.3. Output signal has the same properties of input signal except the phase information.

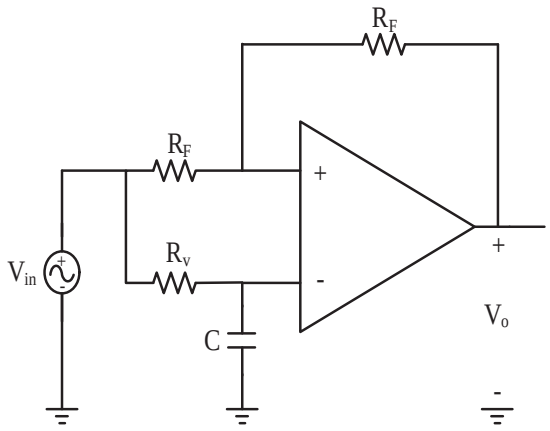

Figure 5.3: Basic block of phase shifter electronics

'R_F' resistances provide equal gain between the input and output terminals. The 'R_V' resistance and 'C' capacitance that are located at the negative terminal of OP-AMP create low pass filter topology. The transfer function of the basic phase shifter electronics is shown in Equation 5.4.

$$H(s) = \frac{1 - sR_vC}{1 + sR_vC} \tag{5.4}$$

The absolute value of the transfer function and the phase information which depends 'R_V' resistance and 'C' capacitance values are given in Equation 5.5.

$$|H(s)| = 1, \phi = -2\arctan(2\omega R_vC) \tag{5.5}$$

The operation frequency of electronics has been determined from 1 to 6 MHz and the product

value of 'R_V' resistance and 'C' capacitance can be changed in order to obtain desired phase shifting among the signals. Designed phase shifter circuit supports up to '90' degree phase shifting.

The focal point of 16 elements is located at an axial distance on the normal to the device center plane. Therefore, 8 different phase shifted sinusoidal signals can be distributed over all elements in twain. Then, it will be sufficient to excite 16 elements of CMUT array with 8 number of signals. The elements of the CMUT device that are going to be excited by same sinusoidal signals are shown in Figure 5.4. 4^{th} and 13^{th} elements of the array are going to have same shifted sinusoidal signals.

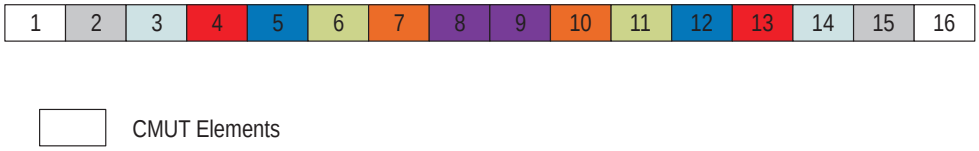

Figure 5.4: Same colored elements are excited with the same phase signals

The designed phase shifter system is shown in Figure 5.5.

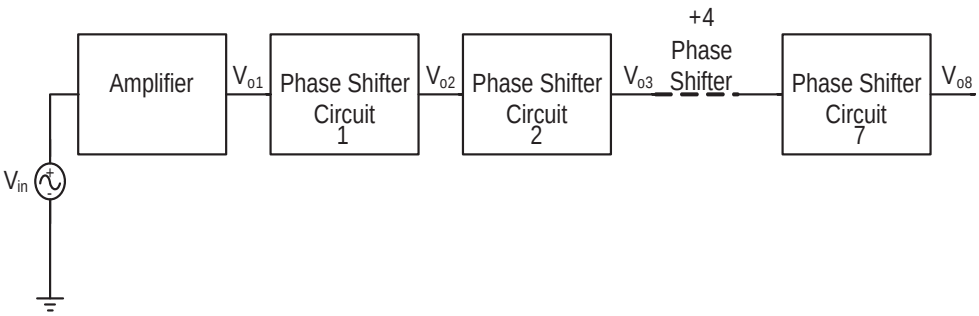

Figure 5.5: Designed phase shifter circuit

The values of 'R_V' resistance and 'C' capacitance are critical for phase shifter circuit. In this design, the value of 'C' capacitor is held constant in order to increase the stability and simplicity of phase shifting. Therefore, phase difference between the signals only depends on 'R_V' resistance value. The value of the capacitor is set to 220 pF according to theoretical calculations, desired frequency range and available capacitance values at the market.

Considering the value of the capacitor, resistance value is calculated between the range of 4 to 200 Ω for desired phase shifting interval.

The simulation of the circuit was done using ORCAD Capture Pspice software. The values of the circuit components is given in Table 5.2.

Table 5.2: Following component values were used for circuit simulations

OP-AMP MODEL	LM7171
DC Voltage	$\pm 15V$
V_{in}	$\pm 14V$
Frequency	3 MHz
R_v	4 Ω – 200Ω
R_F	1 KΩ
C	220 pF

The phase difference between the signals can be changed according to the 'R_V' resistance value in the circuit. The basic block of the phase shifter circuit supports up to '90' degrees phase shift. However, designed circuit serves up to '360' degree phase shift with connecting the basic blocks in series. At 3 MHz, the maximum phase shift between sinusoidal signals, which can run consecutive elements of CMUT device, is 74 ns. Additionally, circuit generates minimum 2 ns phase shift between adjacent signals. The simulation with minimum 'R_v' value ('R_v'=4 Ω) is given in Figure 5.6 and the simulation with maximum 'R_v' value ('R_v' =200 Ω) is given in Figure 5.7.

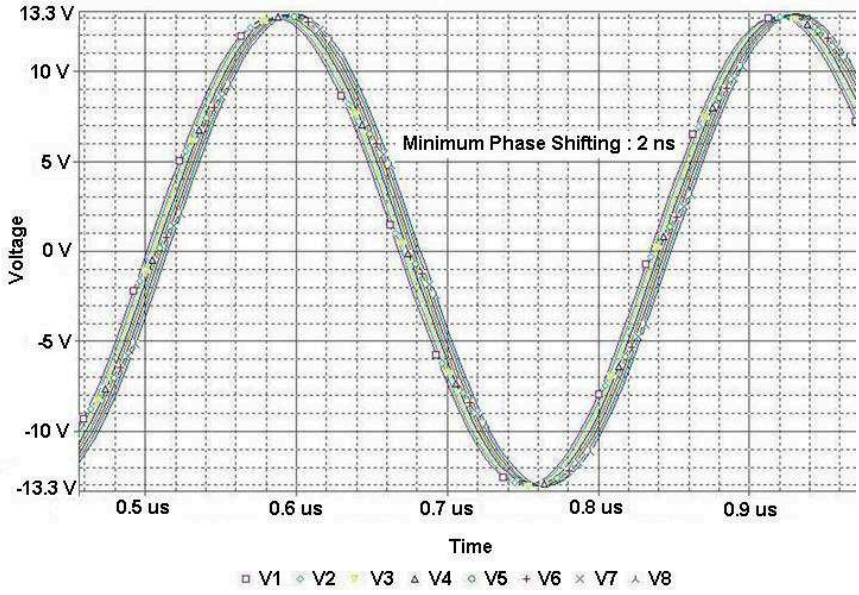

Figure 5.6: Simulation result of phase shifter circuit with minimum R_v value (R_v=4 Ω)

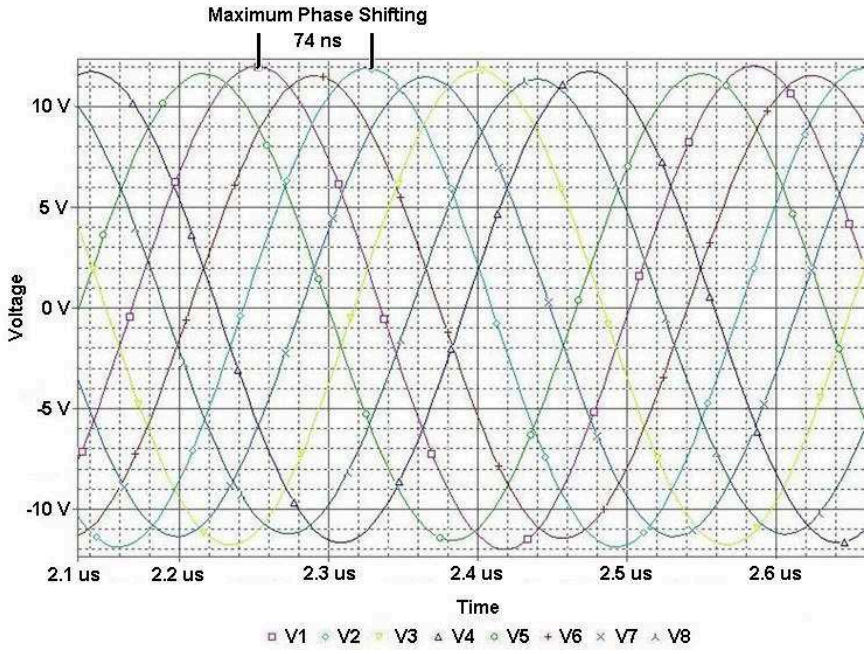

Figure 5.7: Simulation result of phase shifter circuit with maximum R_v value (R_v=200Ω)

5.2 T-Bias Circuit Design

The sinusoidal signals at output terminals are superimposed with the DC bias voltage using T-Bias circuit. It has resitors DC blocking capacitors. The values of the capacitors must be determined according to the operating frequency range. Resistance value is also critical in order to prevent the undesired short circuits of CMUT elements. Any possible high current flowing through CMUT elements can be eliminated with high resistance values. 1 μF and 1 MΩ are the values of the capacitance and resistance, respectively. The schematic of T-Bias circuit is shown in Figure 5.8.

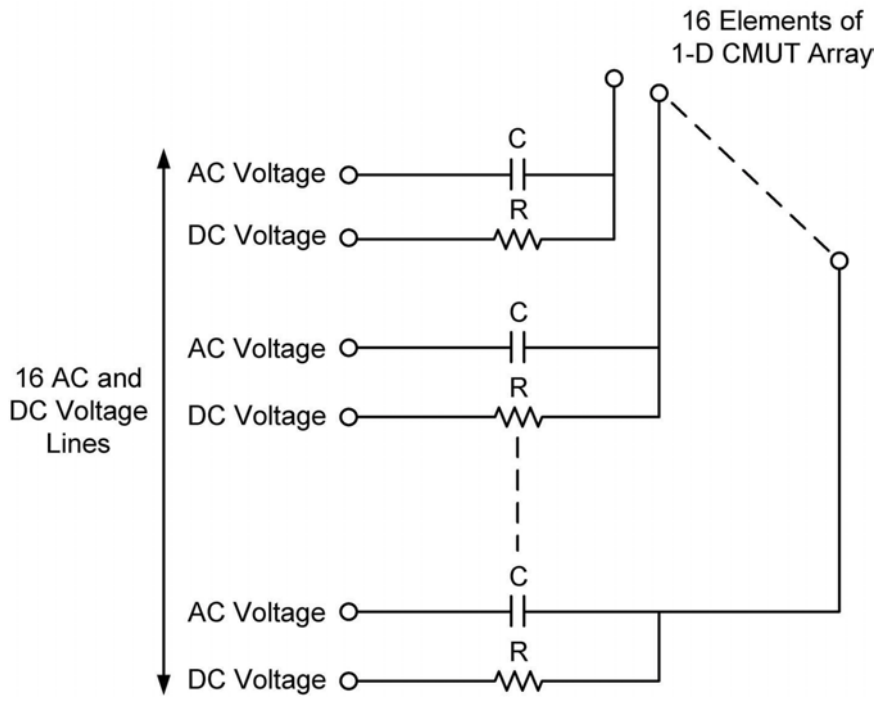

Figure 5.8: The schematic of T-Bias circuit consisting capacitors and resistors

5.3 Printed Circuit Board (PCB) Layout Design of T-Bias, Fanout and Phase Shifter Circuits

The mask of the phase shifter circuit was designed for production of printed circuit board. PROTEUS software (Labcenter Electronics, P 7.0, Canada) was used to design the mask of the circuit layouts. In order to decrease incoming noise; power terminals of every OP-AMPs

had high capacitors (1 μF), one side of the PCBs were totally grounded and high quality circuit components were used. Voltage regulator components were used for both positive and ground terminals in order to stabilize bias voltage of OP-AMPs.

Fanout board was connected to T-bias board with 16 coaxial cable for low noise transmission. Besides, cable connections to the fanout board supports the flexibility to test CMUT devices in different mediums.

5.4 Implementation of Circuit Designs

Production of PCB boards were performed and components were soldered to constitute the full implementation of circuit. For layout implementations, standard copper boards were used and conventional methods were applied. Circuit components were provided from Farnell Company as listed in Table 5.3.

Table 5.3: Circuit components for PCB implementations

Manufacturer - Components	Description
NATIONAL SEMICONDUCTOR - LM7171BIN	OPAMP, H SPEED, 200MHZ
STMICROELECTRONICS - L7815ABV	VOLTAGE REGULATOR, +15V
STMICROELECTRONICS - L7915ACV	VOLTAGE REGULATOR, -15V
TYCO ELECTRONICS - 114780320	CONNECTOR, BNC
SAMTEC - TD108GA	CONNECTOR, 2.54 MM, DUAL, 16WAY
BOURNS - 3299W1201LF	TRIMMER, 25 TURN 200R, 200 Ω
BOURNS - 3299W1202LF	TRIMMER, 25 TURN 2K, 2 k Ω
AVX - 08051A221JAT2A	CAPACITOR, 220 pF, 100V
KEMET - C1206C225K3NACTU	CAPACITOR, 2.2 μF, 25V
KEMET - B45196H5105K109	CAPACITOR, 1 μF, 25V
MULTICOMP - MCCA000434	CAPACITOR, 100 nF, 25V
PANASONIC - ERA3ARW102P	RESISTOR, 1 kΩ, 0.05%
SUSUMU - RR1220P105BT5	THIN FILM CHIP RESISTOR, 1 MΩ, ±0.1%

Produced phase shifter and T-bias board are shown in Figure 5.9.

Figure 5.9: Phase shifter and bias T board is packaged in a box

5.5 Test of the Phase Shifter Circuit

The phase shifter circuit has been tested using a standard DC voltage source with a dual supply, a function generator (33220A, Agilent Technologies, Santa Clara, CA) and an oscilloscope (DSO6014A, Agilent Technologies, Santa Clara, CA). Potentiometer was adjusted to the resistance value of 4 Ω for minimum phase shifting according to the reference signal. Measurement result for this setup is given in Figure 5.10. Then, Potentiometer was adjusted to the resistance value of 200 Ω for maximum phase shifting according to the reference signal. Measurement result for this setup is given in Figure 5.11.

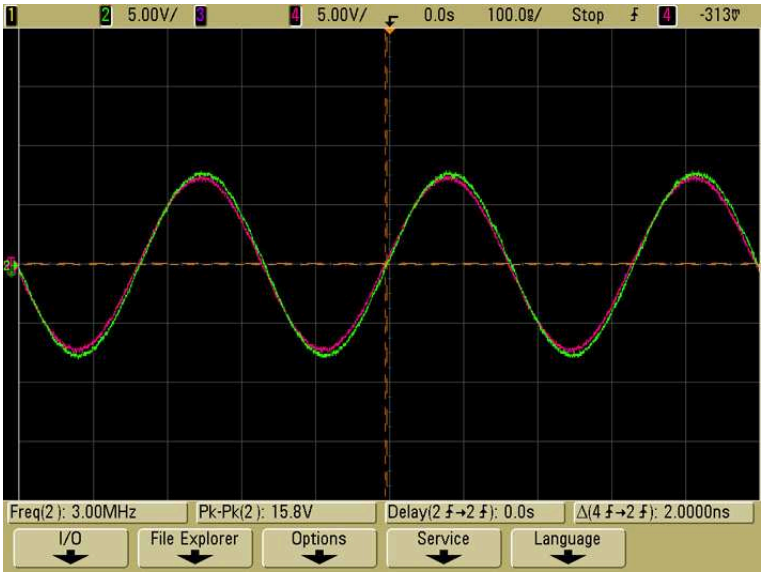

Figure 5.10: Test result for phase shifter circuit ($R_V = 4\ \Omega$)

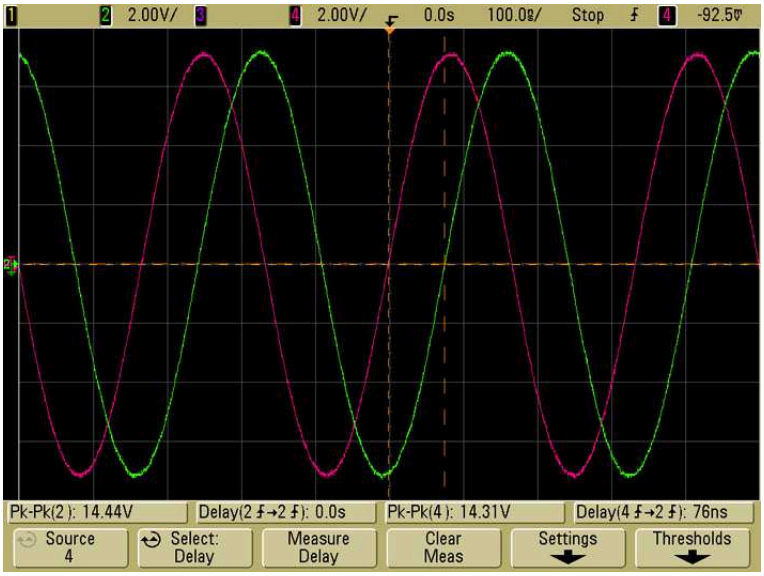

Figure 5.11: Test result for phase shifter circuit ($R_V = 200\ \Omega$)

CHAPTER 6

CHARACTERIZATION OF 1-D CMUTs WITH DIAMOND MEMBRANES

6.1 Test Setup for 1-D CMUT Focusing Measurement

1-D CMUT array was tested using a test setup shown in Figure 6.1.

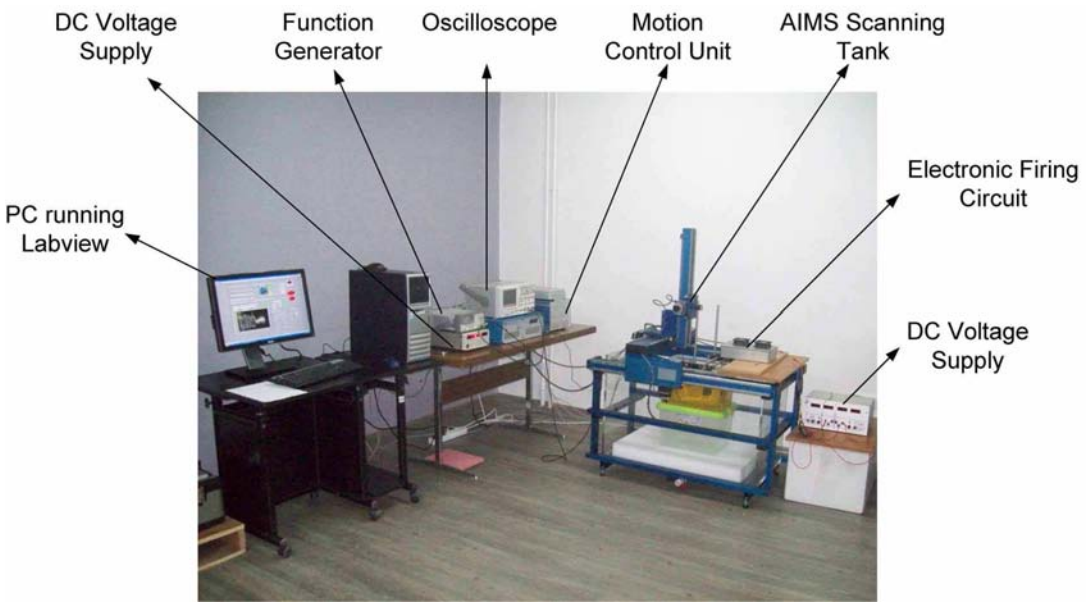

Figure 6.1: The test setup for 1-D CMUT array

This test setup has a desktop computer, a DC voltage source (PS310, Stanford Research Systems, Sunnyvale, CA), a function generator (33220A, Agilent Technologies, Santa Clara, CA), a hydrophone measurement system (ASTS03, AIMS Scanning Tank, Onda Corpora-

tion, Sunnyvale, CA), a preamplifier (AH-2020-DCBSW, Onda Corporation, Sunnyvale, CA) and an oscilloscope (DSO6014A, Agilent Technologies, Santa Clara, CA). ULTRASCAN software was used to control all devices that were used to obtain measurement results.

1-D CMUT array was located inside the sunflower oil and focal point was searched in this medium. The speed of the ultrasonic wave inside the sunflower oil was experimentally measured as 1462.5 m/s. In order to determine the speed of the ultrasonic wave inside the sunflower oil, the burst signal was applied to device and generated ultrasonic wave was measured by hydrophone system. Time delay between the burst and measured signal gives the speed of the ultrasonic wave. Measurement setup delays were neglected. CMUT array and hydrophone setup are shown in Figure 6.2.

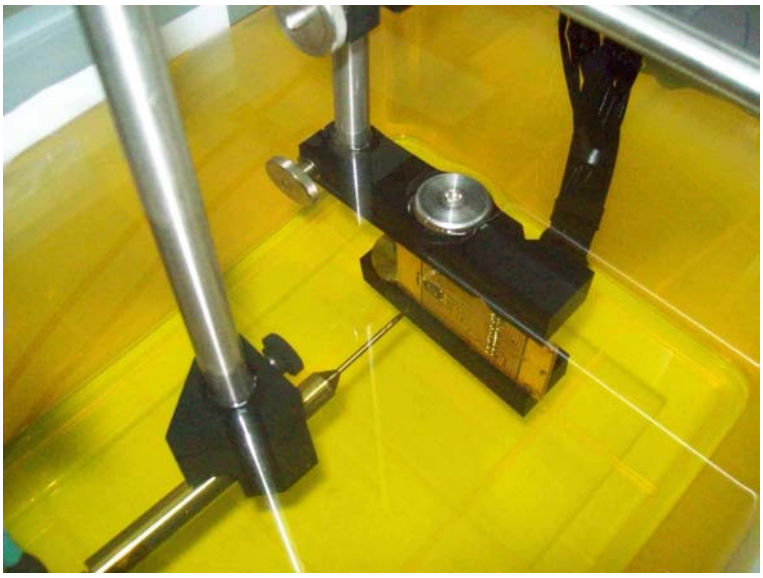

Figure 6.2: 1-D CMUT array and hydrophone in the sunflower oil

6.2 Single Element Excitation of CMUT Array

The operation of the 1-D CMUT array was observed using the test setup given in Figure 6.1. 1-D CMUT array with 72 μm cells was used to perform the ultrasonic focusing experiment.

Physical parameters of 1-D CMUT array used for focusing experiment are given in Table 6.1.

Table 6.1: Physical Parameters of 1-D CMUT array

Number of Elements	16
Cells per Element	122
Height of Elements (h), μm	6000
Windth of Array (w), μm	3200
Windth of Elements (a_w), μm	200
Membrane Radius (r_m),μm	36
Electrode Radius (r_e),μm	18
Membrane Thickness (t_m),μm	1
High Temperature Oxide Thickness (t_{ho}),μm	0.2
Gap Thickness (t_g), μm	1.57
Silicon Substrate Thickness (t_s), μm	525

Active and damaged elements of the CMUT array are shown in Figure 6.3. The possible reasons of damaged elements were due to either microfabrication defects or wire bonding process. Active 7 elements of 1-D CMUT array were excited for the ultrasonic focusing experiment.

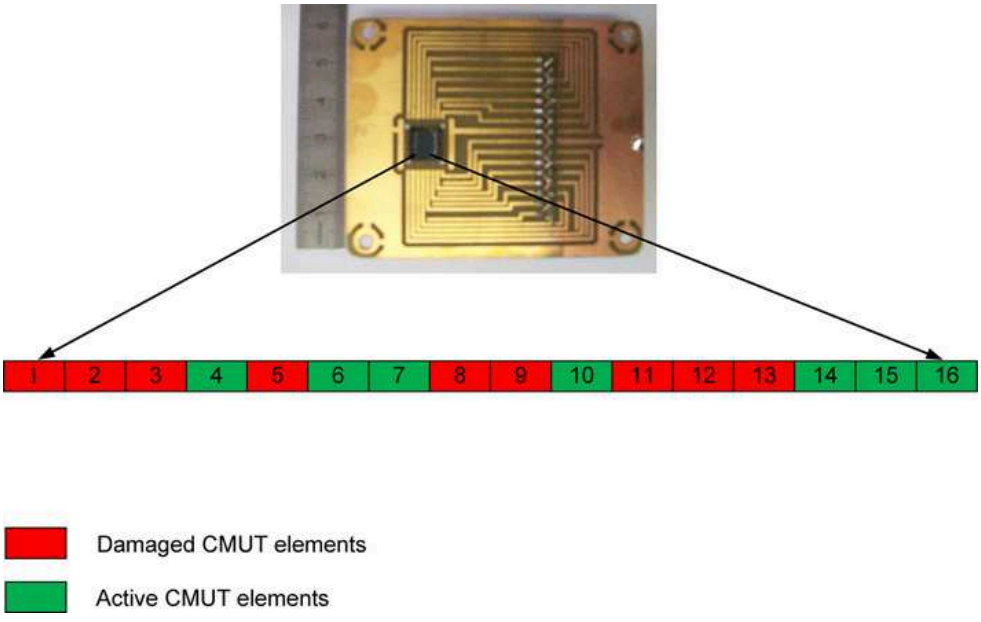

Figure 6.3: Location and condition of elements of 1-D CMUT array

Calculated focal point is located at an axial distance of 4.47 mm on the normal to the 1-D

CMUT center plane. Given schematic view of X-Y plane in Figure 6.4 is used to observe the actual focal point. All measurement was captured using x-y stage and 4096 average value of digital oscilloscope.

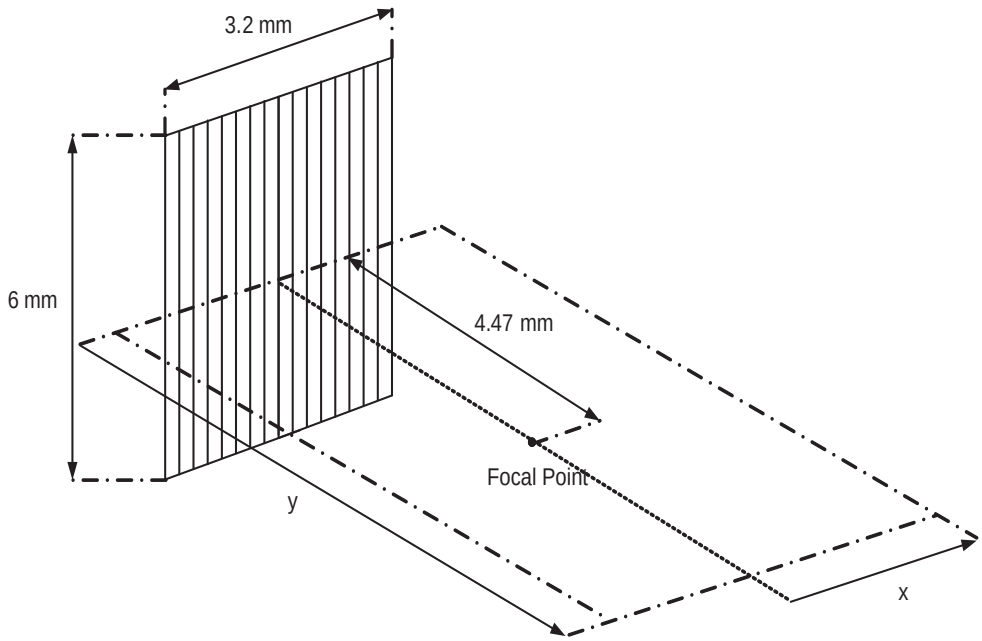

Figure 6.4: Schematic view of X-Y plane that was used to obtain the coordinates of focal point

7^{th} element of 1-D CMUT array was excited to measure the effect of the single element on focal point. Therefore, it will be more easier to experimentally determine ultrasonic focusing of all elements when the effect of single element on focal point is observed. This element was excited at 3 Mhz, 10 V_{p-p} and 10 cycle sinusoidal signal. The measurement result is shown in Figure 6.5.

The hydrophone voltage, at the axial distance on the normal to the CMUT center plane, decreases while hydrophone is moving away from the CMUT surface. This response is shown in Figure 6.6.

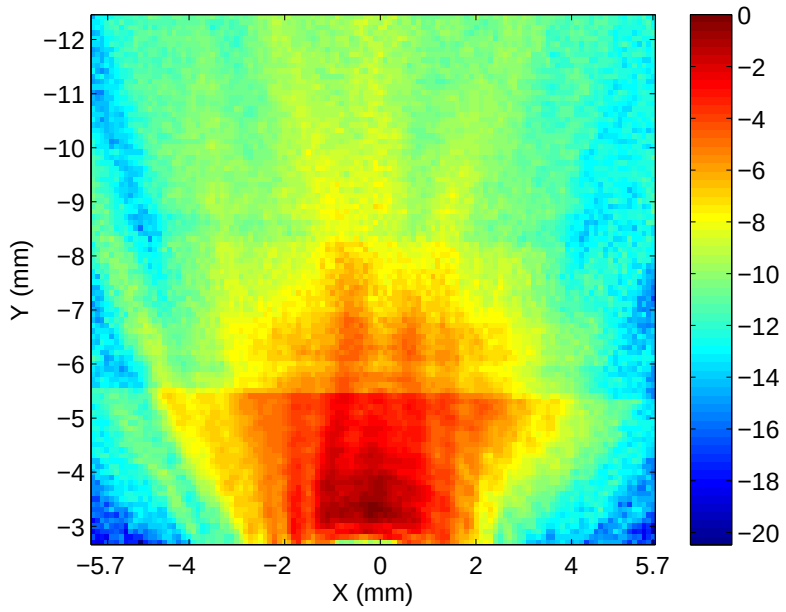

Figure 6.5: Analysis result of the 7^{th} element of 1-D CMUT array with 0.1 mm resolution on X-Y plane (f=3 MHz, V_{p-p}=10 V, 10 cycles sinusoidal signal)

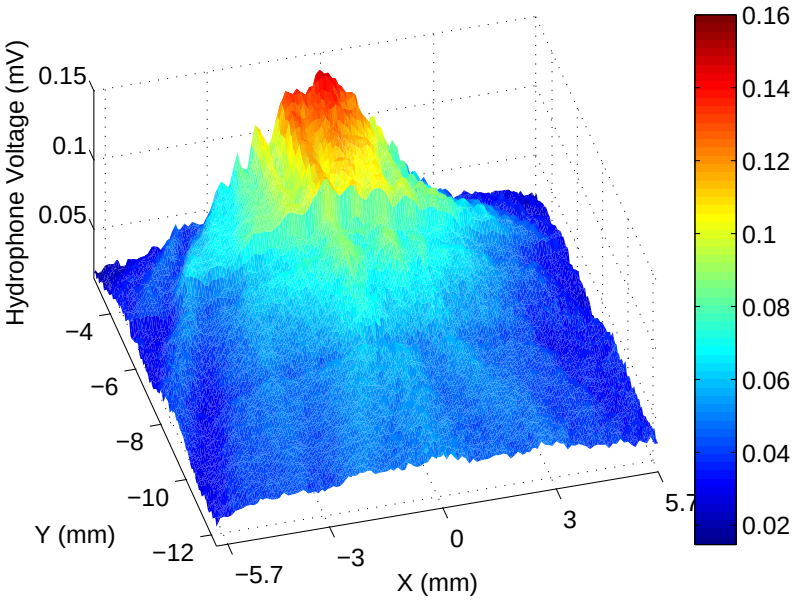

Figure 6.6: 2-D scanning measurement of the 7^{th} element of 1-D CMUT array (f=3 MHz, V_{p-p}=10 V, 10 cycles sinusoidal signal)

The distribution of the hydrophone voltage in X-Y plane for the single element is shown in Figure 6.7. Hydrophone scanning was started approximately 3 mm away from CMUT surface in order to prevent any contact between the transducer of hydrophone.

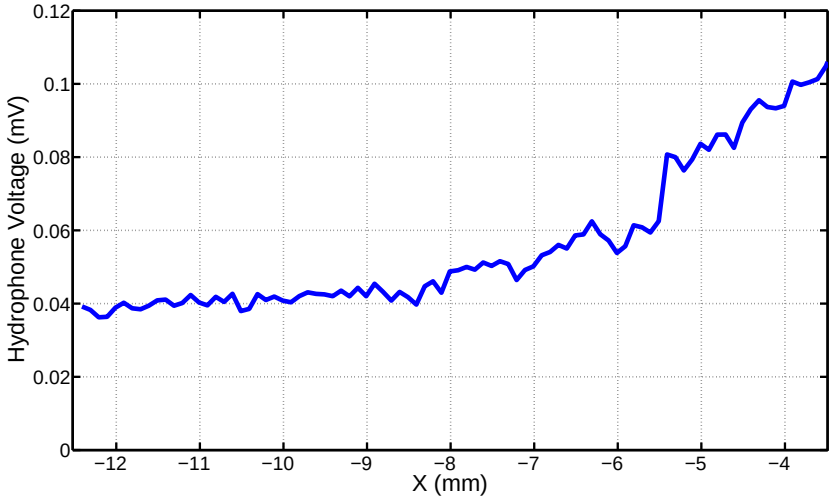

Figure 6.7: Measured voltage distribution of the single element at the axial distance on the normal to the CMUT center plane (f=3 MHz, V_{p-p}=10 V, 10 cycles sinusoidal signal)

6.3 1-D CMUT Array Focusing Measurements

7 elements of 1-D CMUT array were excited with phase shifter electronics in order to focus ultrasonic waves at the axial coordinate on the normal to the CMUT center plane. The phase shifting values of firing circuit were adjusted to obtain a focus at 4.47 mm. The measurement results indicated that focal point was obtained at 5.81 mm and it is shown in Figure 6.8. The focal point in theoretical calculations is at 4.47 mm along the center axis, but it is located at 5.81 mm according to the experimental measurements. The possible reasons of this deviation are diffraction and attenuation effects in the propagation medium being neglected in the theoretical calculations. The other one is due to phase shifting values of the signals that are deviated from the calculated values. Calculated and tested phase shifting values are shown in Table 6.2.

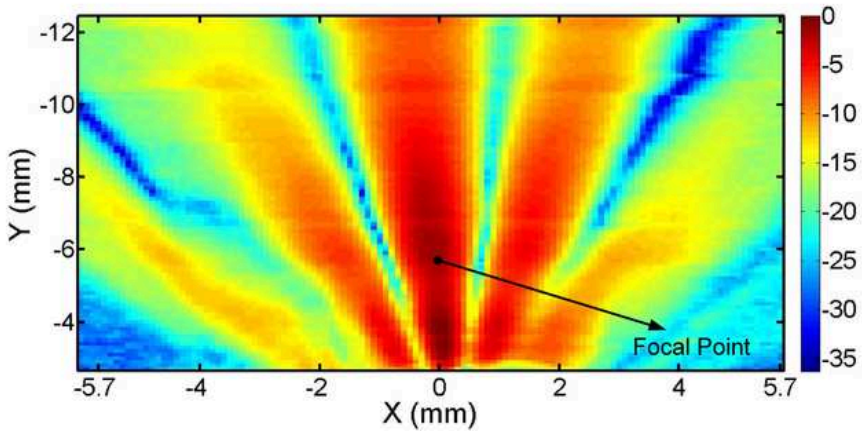

Figure 6.8: 2-D scanning hydrophone results of focusing measurement. It was obtained with 0.1 mm resolution. Focusing point measured at Y=5.81 mm. (f=3 MHz, V_{p-p}=10 V, 10 cycles sinusoidal signal)

Table 6.2: Calculated and actual results obtained for phase shifting circuit

	1–2	2–3	3–4	4–5	5–6	6–7	7–8
Theoretical Results	40.85	35.44	29.84	24.08	18.18	12.18	6.11
Actual Results	40.40	36.00	32.40	25.20	18.00	13.20	7.20
Deviation	1.1%	1.6%	8.6%	4.6%	1%	8.4%	17.8%

Amount of the phase shifting was adjusted by potentiometers with 25 turns. Therefore, desired phase shifting values of the signals could not have been able to be obtained. IC phase shifting circuit design may solve this problem basically by means of better sensitivity and controllability.

Every active elements of 1-D CMUT array were analyzed in order to obtain their ultrasonic responses at the axial coordinate on the normal to the CMUT center plane. Filtered peak values captured from hydrophone is shown in Table 6.3.

Table 6.3: Filtered peak values of 1-D CMUT elements

Number of Element	Filtered V_{p-p} Values (μV)
4	79.49
6	107.70
7	86.85
10	37.12
14	73.68
15	83.05
16	45.25

The sum of the filtered peak values of 1-D CMUT elements is 0.51 μV. The expected value for focal point is lower than this maximum value. Approximately 0.35 μV was observed during focusing experiment as shown in Figure 6.9 and 6.10.

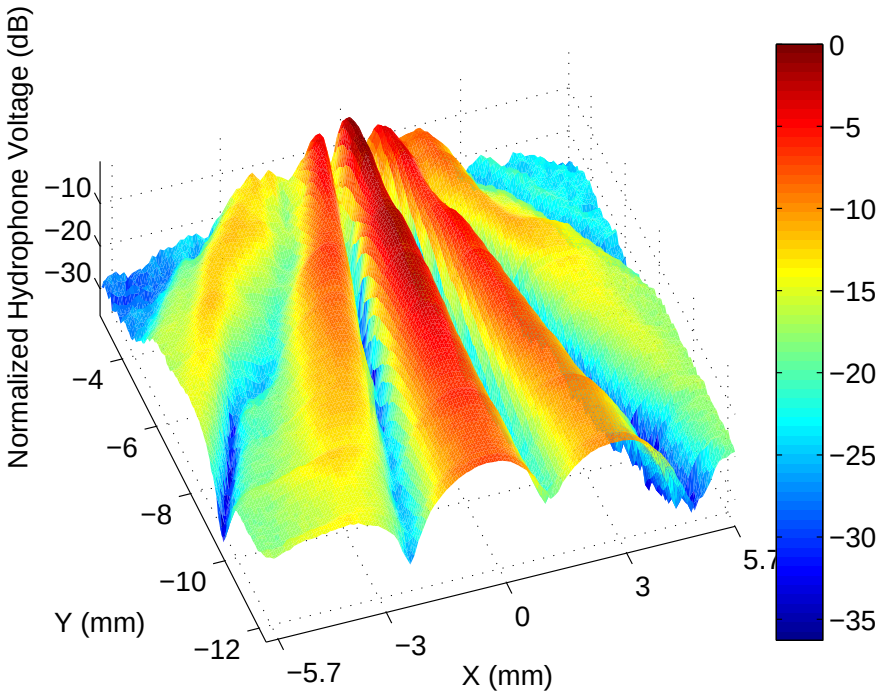

Figure 6.9: The view of the two dimensional focusing point captured with 0.1 mm resolution. Focusing point measured at Y=5.81 mm. (f=3 MHz, V_{p-p}=10 V, 10 cycles sinusoidal signal)

Both single element excitation and focusing experimental results are plotted in the same

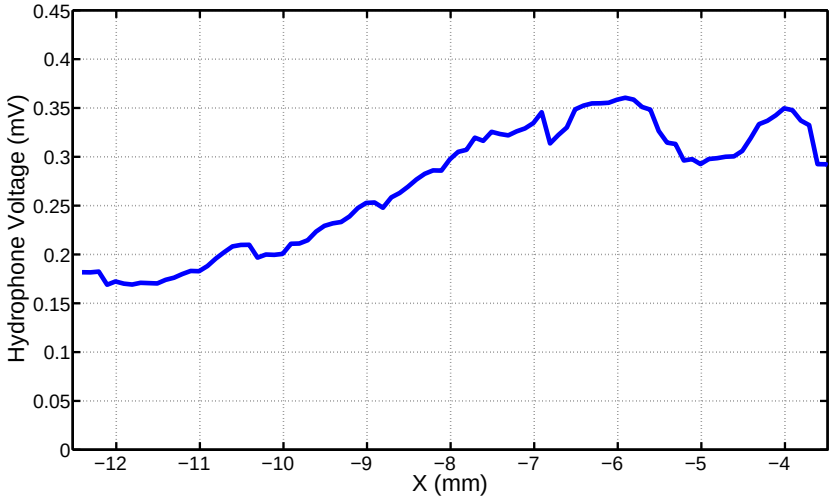

Figure 6.10: The view of the focusing point captured with 0.1 mm resolution along the center axis. (Normalized hydrophone voltages is used). (f=3 MHz, V_{p-p}=10 V, 10 cycles sinusoidal signal)

graphic as shown in Figure 6.11. Focal point of active elements is also marked in the figure.

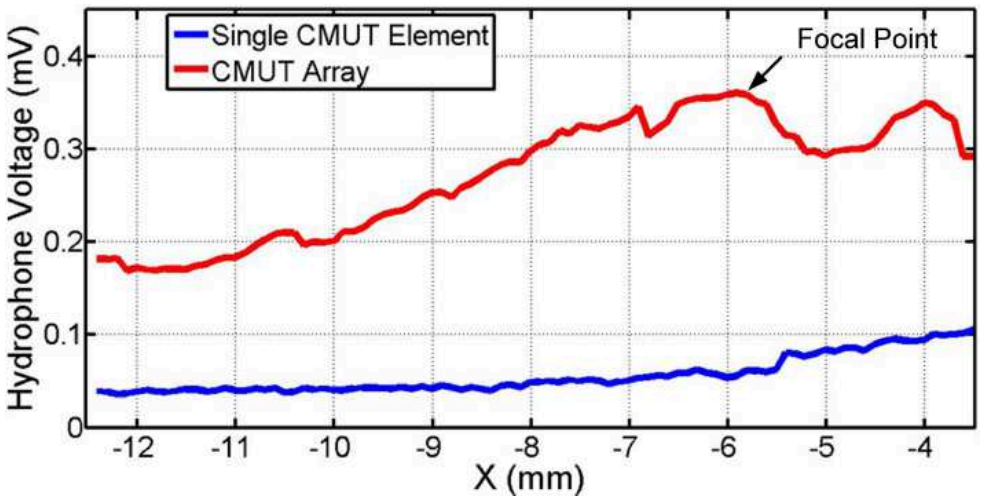

Figure 6.11: The view of the two dimensional focusing point captured with 0.1 mm resolution. (Normalized hydrophone voltages is used). (f=3 MHz, V_{p-p}=10 V, 10 cycles sinusoidal signal)

The investigation of frequency response of 1-D CMUT array at focal point was observed. The

elements of CMUT array were excited using a single cycle sinusoidal signal. The hydrophone voltage at focal point is shown in Figure 6.12. Transfer function of CMUT array at that point can be seen at Figure 6.13.

Transfer function of CMUT array at focal point was investigated using single cycle excitation shown in Figure 6.12. The frequency bandwidth of 1-D CMUT array was observed from 1.7 MHz to 4.2 MHz. The bandwidth frequency was determined within 88%. Focusing process of 1-D CMUT arrays with diamond membranes was done successfully.

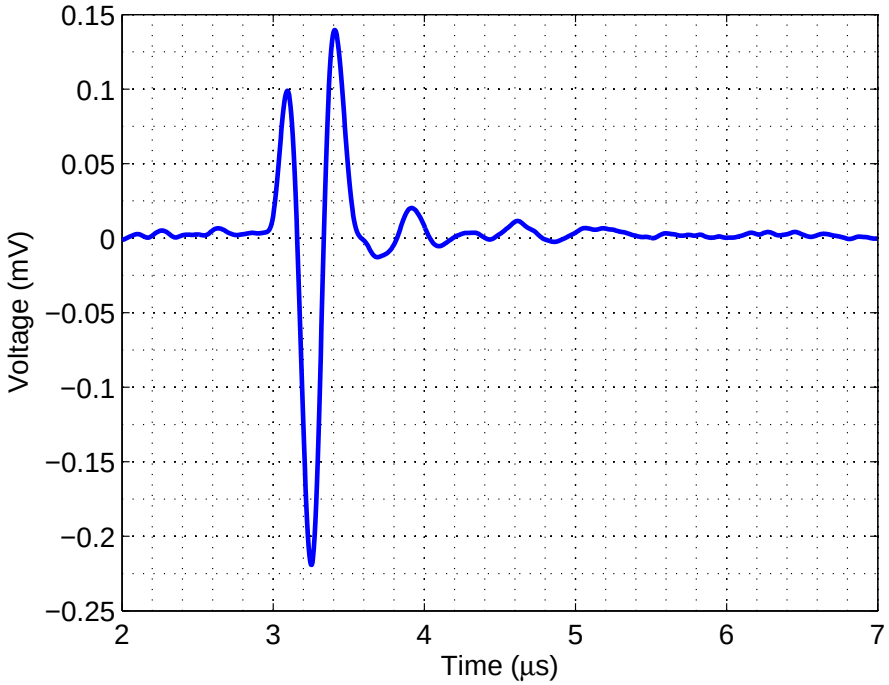

Figure 6.12: The hydrophone voltages of CMUT array. (f=3 MHz, V_{p-p}=10 V, 1 cycle sinusoidal signal)

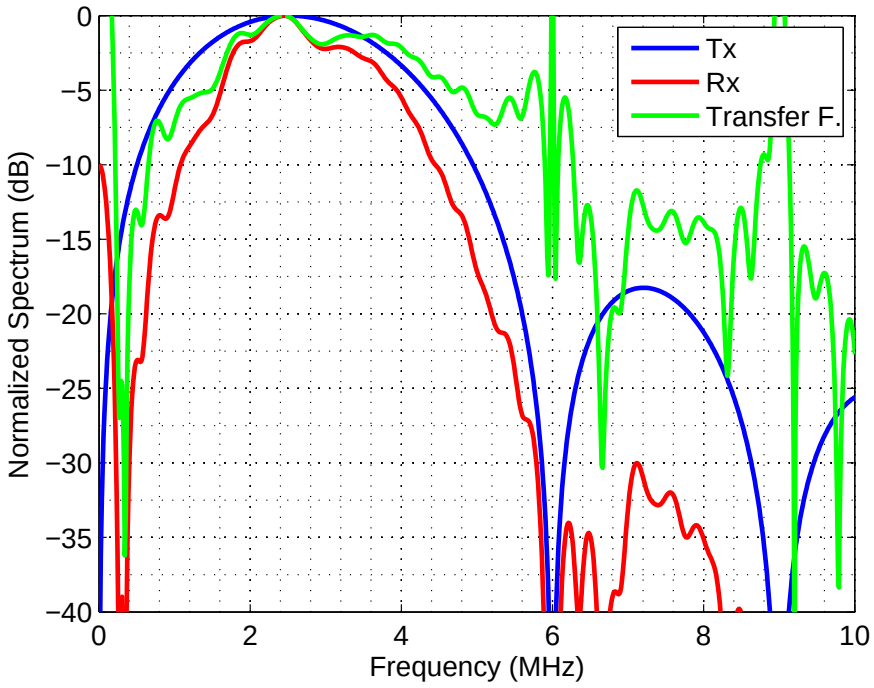

Figure 6.13: Normalized frequency response of CMUT array. (f=3 MHz, V_{p-p}=10 V, 1 cycle sinusoidal signal)

CHAPTER 7

CONCLUSION AND FUTURE WORK

In this thesis, novel microfabrication steps of CMUTs with diamond membranes have been developed and 1-D and single CMUTs have been successfully fabricated. Ultrasound focusing experiment of diamond membrane 1-D CMUTs has been firstly investigated.

CMUT devices were fabricated by conventional method which was sacrificial release process. However, this microfabrication approach introduces the limitations on membrane and cavity sizing. These limitations have been solved by CMUT fabrication with wafer bonding technology. On the other hand, development of the microfabrication processes enables new materials that can be introduced to the CMUT devices. In this thesis, diamond material has been introduced to the CMUT technology and the direct wafer bonding technology has been used to form novel microfabrication steps for diamond based CMUT devices.

This work presents some improvements that are stated below:

1- Silicon nitride and silicon are used to form the membrane structure of CMUT devices in the literature. These materials has low Young's modulus when they are compared to diamond material (Silicon nitride : 290 GPa, Silicon : 169 GPa, Diamond(UNCD) : 910 GPa). Collapse and collapse-snap back modes of operations induce high stresses on membrane material. Therefore, CMUTs with diamond membranes can be operated safer than other materials used in literature for collapse and collapse-snap back modes of operations. These modes generate high output pressures than conventional mode.

2- Full wafer bonding of diamond material on to the oxide grown silicon wafer has been firstly demonstrated in this work. This work can be a reference for diamond based MEMS devices.

In order to enhance the performance and reliability of the CMUTs with diamond membranes and focusing experiment, following improvements can be considered:

1- PADs of the CMUT elements can be modified to obtain more robust connections. The width of the metal connections from PADs to the elements may be increased or these metal lines can be replicated for better connection quality. Besides, contact area of the PADs should be increased for more reliable connections of excitation signals. Because, during wire bonding process, dimension of the PADs brought connectivity errors and defects for the device elements.

2- PCB fanout board was used to connect the signal paths to the driven electronics. The fanout chips with gold wires that are already available in the market can be used to make connections to the electronic circuit. It may serve more reliable signal paths to CMUT devices.

3- Phase shifter circuit was designed in order to perform focusing experiment using 1-D CMUT devices with diamond membranes. This electronic circuit generates AC signals with different phases that can exicite the elements of 1-D CMUT devices. Due to the problems caused by wire bonding process, 7 elements of the device were used for focusing experiment. Optimization of the PADs for future design will eliminate the wire bonding problems and yield issue of elements.

4- During the focusing experiment, 50 V DC voltage was applied to CMUT devices. Elements were operated in conventional mode to propagate the ultrasonic waves to the medium. Collapse or collapse-snap back operation modes of CMUTs can be used to increase the output pressure. Due to the high leakage current in the application of high DC voltages, it is not safe to operate the device in these modes of operations. Observed high leakage current is under investigation to determine the possible reasons in order to optimize the design for high DC voltages.

5- For the optimization of focusing experiment, the driven circuitry can be transferred to IC design, which will most probably be able to eliminate the phase shifting errors and increase the controllability of the system.

In conclusion, development and microfabrication of capacitive micromachined ultrasonic transducers (CMUT) with diamond membranes have been performed for the first time in the literature. For the future work, improved microfabrication of diamond based CMUT devices

are aimed to be developed.

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Appendix A

Novel Microfabrication Process Steps for CMUTs with Diamond Membranes

Table A.1: Novel microfabrication process steps for single and 1-D CMUT devices with diamond membranes

Step Number	Process Information
1	Bottom wafer: n-type silicon wafer
2	Bottom wafer: P doing for conductive surface
3	Bottom wafer: Thermal oxide growth
4	Bottom wafer: Photoresist covering
5	Bottom wafer: Photoresist patterning with cavity mask
6	Bottom wafer: SiO_2 etching with RIE
7	Bottom wafer: Photoresist stripping with O_2 plasma
8	Top wafer: Silicon wafer with diamond layer
9	Top wafer: HTO-SiO_2 deposition in LPCVD furnace
10	Top wafer: Satisfy the surface roughness of HTO-SiO_2 with CMP
11	Bonding of wafers under vacuum at 550^oC with plasma activation
12	Bonded wafers: Total TMAH etching of 525 μ m silicon layer
	of top wafer
13	Bonded wafers: PECVD SiO_2 covering of diamond surface
14	Bonded wafers: Photoresist covering
15	Bonded wafers: Photoresist patterning with toplayer mask
16	Bonded wafers: SiO_2 etching with RIE
17	Bonded wafers: Diamond etching with RIE and photoresist stripping
18	Bonded wafers: SiO_2 etching with RIE
19	Bonded wafers: Aluminum covering
20	Bonded wafers: Photoresist covering
21	Bonded wafers: Photoresist patterning with metal mask
22	Bonded wafers: Aluminum etch with chemicals and photoresist stripping
	with O_2 plasma

Appendix B

PCB Layout Designs

The mask of the phase shifter circuit was designed for production of printed circuit board. PROTEUS software (Labcenter Electronics, P 7.0, Canada) was used to design the mask of the circuit layouts as shown in Figure B.1

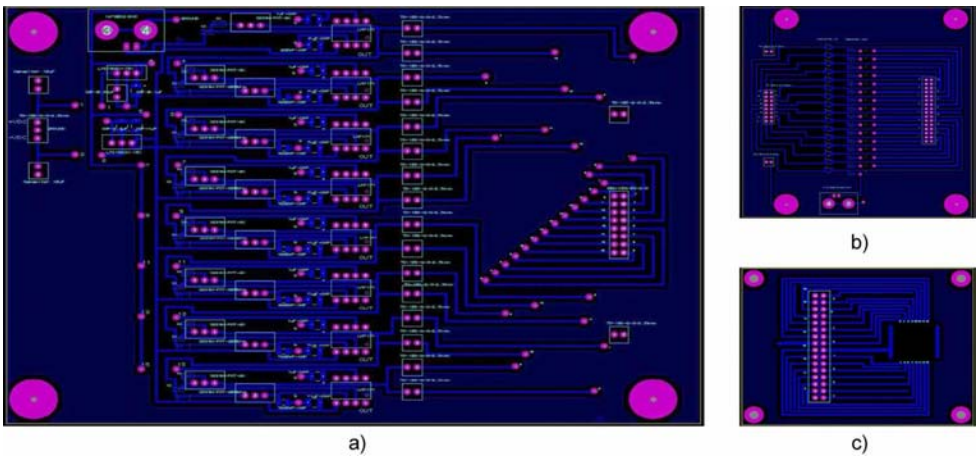

Figure B.1: a)The layout of phase shifter circuit board, b)The layout of T-bias board, c)The layout of the fanout board