WAFER LEVEL VACUUM PACKAGING OF MEMS SENSORS AND RESONATORS

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I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all referenced material and results that are not original to this work.

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ABSTRACT

WAFER LEVEL VACUUM PACKAGING OF MEMS SENSORS AND RESONATORS

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This thesis presents the development of wafer level vacuum packaging processes using Au-Si eutectic and glass frit bonding contributing to the improvement of packaging concepts for a variety of MEMS devices. In the first phase of this research, micromachined resonators and pirani vacuum gauges are designed for the evaluation of the vacuum package performance. These designs are verified using MATLAB and Coventorware finite element modeling tool. Designed resonators and pirani vacuum gauges and previously developed gyroscopes with lateral feedthroughs are fabricated with a newly developed Silicon-On-Glass (SOG) process. In addition to these, a process for the fabrication of similar devices with vertical feedthroughs is initiated for achieving simplified packaging process and lower parasitic capacitances. Cap wafers for both types of devices with lateral and vertical feedthroughs are designed and fabricated. The optimization of Au-Si eutectic bonding is carried out on both planar and non-planar surfaces. The bonding quality is evaluated using the deflection test, which is based on the deflection of a thinned diaphragm due to the pressure difference between inside and outside the package. A 100% yield bonding on planar surfaces is achieved at 390ºC with a

holding time and bond force of 60 min and 1500 N, respectively. On the other hand, bonding on surfaces where 0.15µm feedthrough lines exist can be done at 420ºC with a 100% yield using same holding time and bond force. Furthermore, glass frit bonding on glass wafers with lateral feedthroughs is performed at temperatures between 435-450ºC using different holding periods and bond forces. The yield is varied from %33 to %99.4 depending on the process parameters. The fabricated devices are wafer level vacuum packaged using the optimized glass frit and Au-Si eutectic bonding recipes. The performances of wafer level packages are evaluated using the integrated gyroscopes, resonators, and pirani vacuum gauges. Pressures ranging from 10 mTorr to 60 mTorr and 0.1 Torr to 0.7 Torr are observed in the glass frit packages, satisfying the requirements of various MEMS devices in the literature. It is also optically verified that Au-Si eutectic packages result in vacuum cavities, and further study is needed to quantify the vacuum level with vacuum sensors based on the resonating structures and pirani vacuum gauges.

Keywords: MEMS Fabrication, Wafer Level Vacuum Packaging, Au-Si Eutectic Bonding, Glass Frit Bonding, MEMS Gyroscopes and Resonators, Pirani Vacuum Gauges.

ÖZ

MEMS SENSÖR VE REZONATÖRLER İÇİN PUL SEVİYESİNDE VAKUM PAKETLEME

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Bu tez çeşitli MEMS aygıtlarının paketleme konseptlerinin iyileştirilmesine katkıda bulunulması amacıyla, Altın-Silisyum Ötektik ve Cam hamuru yapıştırma tekniklerini kullanarak pul seviyesinde vakum paketleme tekniklerinin geliştirilmesini sunmaktadır. İlk aşamada, vakum paketlerin performanslarının değerlendirilmesi için MEMS rezonatörler ve pirani vakum ölçerleri tasarlanmıştır. Bu tasarımlar MATLAB ve Coventorware sonlu modelleme aracı kullanılarak doğrulanmıştır. Tasarlanan rezonatörler, pirani vakum ölçerleri ve daha önceden geliştirilen dönüölçerler yanlamasına elektriksel hatlar ile yeni geliştirilen cam-üstü-silisyum üretim tekniği ile üretilmiştir. Bunlara ek olarak, daha kolay paketleme işlemi ve düşük parasitik kapasitans elde etmek için aynı aygıtların dikey elektriksel hatlar ile üretilmesi işlemi başlatılmıştır. Hem yatay hem dikey elektriksel hatlara sahip aygıtlar için kapak pulları tasarlanıp, üretilmiştir. Pürüzsüz ve pürüzlü yüzeyler üzerine Altın-Silisyum Ötektik yapıştırma optimizasyonu gerçekleştirilmiştir. Yapışma kalitesi, prensibi ince bir diyaframın paket içi ve dışı basınç farkından dolayı bükülmesine dayanan bükülme testiyle değerlendirilmiştir.

Pürüzsüz yüzeylere Altın-Silisyum Ötektik yapıştırma sırasıyla 60 dakika bekleme ve 1500 N yapıştırma kuvveti kullanılarak 390ºC'de %100 verim ile başarılmıştır. Diğer taraftan, 0.15µm'lik hatların olduğu yüzeylere Altın-Silisyum Ötektik yapıştırma aynı bekleme ve yapıştırma kuvveti kullanılarak %100 verim ile 420ºC'de yapılabilmiştir. Ayrıca, cam hamuru yapıştırma yanlamasına elektriksel hatların bulunduğu cam pullara 435-450ºC'lik sıcaklık aralığında değişik bekleme ve yapıştırma kuvvetleri kullanılarak gerçekleştirilmiştir. Üretim parametrelerine bağlı olarak %33'den %99.4'e değişen verim alınmıştır. Üretilen aygıtlar, optimize edilen cam hamuru ve Altın-Silisyum Ötektik yapıştırma yöntemleriyle pul seviyesinde vakum paketlenmiştir. Paketlerin performansları paket içine entegre edilen dönüölçer, rezonatör, ve pirani vakum ölçerleri ile değerlendirilmiştir. Cam hamuru paketlerde, literatürdeki çeşitli MEMS aygıtların gereksinimlerini karşılayacak şekilde, 10 mTorr-60 mTorr ve 0.1 Torr-0.7 Torr aralığında basınç değerleri gözlenmiştir. Altın-Silisyum Ötektik paketlemenin de vakumla sonuçlandığı optik olarak doğrulanmış ve rezonatör ve pirani vakum ölçer temelli vakum sensörleriyle vakum seviyesinin sınıflandırılması için daha fazla çalışma gerekmektedir.

Anahtar Kelimeler: MEMS Üretimi, Pul Seviyesinde Vakum Paketleme, Altın-Silisyum Ötektik Yapıştırma, Cam Hamuru Yapıştırma, MEMS Dönüölçerler ve Rezonatörler, Pirani Vakum Ölçerler.

To My Parents

Gül and Bülent Torunbalcı

and

My Love Oylum

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TABLE OF CONTENTS

LIST OF FIGURES

FIGURES

LIST OF TABLES

TABLES

CHAPTER 1

INTRODUCTION

Dr. Richard Feynman, the famous physicist, can be considered as the father of today's miniaturized devices. The history of these devices is based on his famous talk, "There is a plenty of room at the bottom", given in 1959 [1]. In his famous talk, he notified that miniaturization techniques would be capable of writing an entire Encyclopedia Brittanica to be written on the head of a pin. He also noted that new applications would emerge because the behavior of matter is different at the atomic scale compared to the bulk scale. Despite Feynman's doubts about the usefulness of the small machines, these devices are now being used in a wide range of applications in our life.

Micro Electro Mechanical Systems, simply referred as MEMS, is the integration of mechanical and electronic elements at micro scale on silicon chip. These systems provide smart devices having not only sensing ability but also other properties such as data processing, communication and actuation capability [2]. Since MEMS devices are fabricated similar to the IC fabrication techniques, thousands of miniaturized sensors can be produced at one time on a single chip, which makes them smaller than their conventional counterparts [3].

In recent years, MEMS industry has shown a rapid progress with a variety of devices on the market. Commercial MEMS devices such as inertial sensors, flow and pressure sensors, RF MEMS, Optical MEMS, Power MEMS, and BioMEMS have found applications from automotive to human health care. Today, the size of the MEMS industry is over 6.54 billion with an annual growth of almost %15 and is projected to a double digited growth by the year 2014. Figure 1.1 shows the distribution of MEMS market from 2006 to 2014 [4].

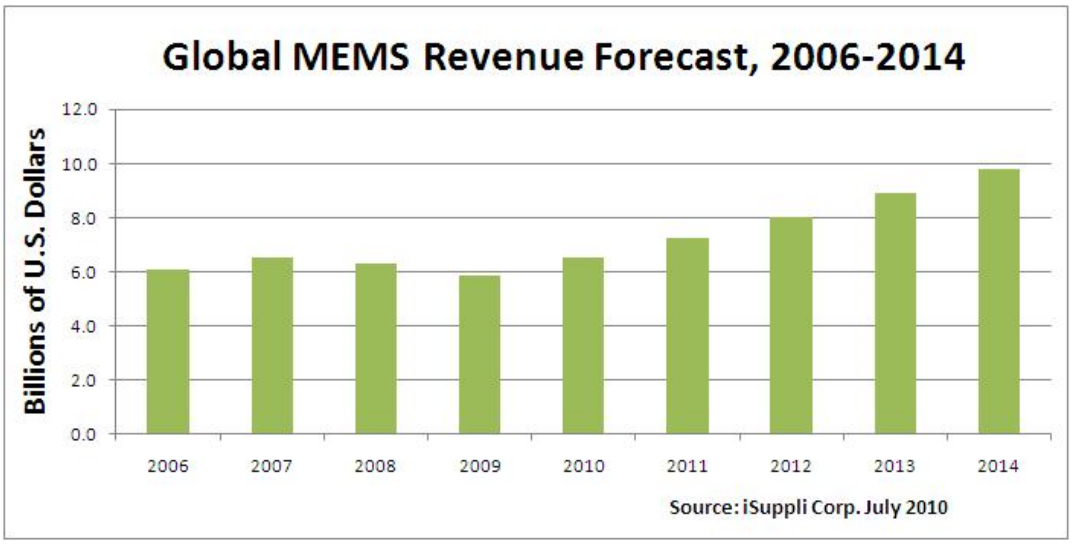


Figure 1.1: The distribution of MEMS market from 2006 to 2014 [4].

Although packaging is a critical step of the commercial success of MEMS devices, the research on this area fell behind. It still remains the most costly and problematic part of the MEMS technology. The cost of a typical packaging process can easily reach to %50 of the total cost of the whole product and a high cost MEMS package has become a major interrupting block in the marketing of MEMS devices.

The packaging of MEMS devices is more difficult and complex than the conventional IC packaging. A MEMS package has to fulfill the requirements of an IC package and enable additional functionalities depending on the type of the device. Thus, MEMS packaging is application specific and the process steps may vary depending on the application [5], [6]. The MEMS industry is trying to find cost effective solutions for the packaging of MEMS devices. The aim of this work is to develop a wafer level vacuum packaging process contributing to the improvement of packaging concepts for a variety of MEMS devices.

In the rest of Chapter 1, Section 1.1 describes the overview of MEMS packaging technology. Section 1.2 presents the MEMS vacuum packaging technology including the requirements, challenges and methods. Section 1.3 gives a brief overview of wafer level vacuum packaging technology, followed by the detailed presentation of the methods used for wafer level vacuum packaging in. Section 1.4 presents the previous wafer level vacuum packaging works reported in the literature. Overall, Section 1.5 gives the research organization and objectives of this work.

1.1 MEMS Packaging

There exist common rules that are generally applicable for the packaging of IC's. However, packaging of MEMS devices is somewhat different and complex than IC's. The major difference is that the MEMS devices have to interact with the environment as most of them serve either as a sensor, a transducer or an actuator. Besides, each MEMS device has its own operational specs and a MEMS package has to be designed specific to the application. This section shortly presents the requirements of MEMS packaging.

1.1.1 Mechanical Support

One of the most important functions of a package is the mechanical protection. MEMS devices consist of fragile and prone-to-damage structures that have to be mechanically protected from mechanical shocks, vibrations, contaminations, and other physical damages during the operation and storage. Furthermore, a MEMS package has to be mechanically rigid and stable throughout the life time. The thermal expansion coefficient of the packaging material has to be selected close to the thermal expansion coefficient of the device material so that a low stress MEMS package can be obtained. In addition to these, the dimensions of the package have to be considered for easy handling, testing and storage.

1.1.2 Protection from the Environment

For many devices, the external environment brings the problems of degradation and erosion of device materials. For instance, aluminum metal lines can easily be damaged by the effect of moisture. Therefore, protection from the undesired effects of the external environment should be one of the major functions of a MEMS package. Ideally, a MEMS package should keep the device safe from the undesired effects of optical, chemical and thermal environments.

The working environment is a key factor in determining the functional behavior of MEMS devices. The requirements are application specific and may vary from device to device. While some devices need vacuum environment, the others require special gas environment or atmospheric environmental conditions. For instance, a MEMS gyroscope requires vacuum environment to have higher performances, whereas a pressure sensor needs to have an access to the external environment

(ambient atmosphere) for sensing. Thus, a MEMS package has to be designed regarding the requirements of the target application.

1.1.3 Electrical Connection

The package is the only interface between the device and the outer world. Therefore, it must be capable of transferring electrical signals to the essential components outside the package. In the case of having a conventional package, the electrical connection is provided by the use of package pins. On the other hand, if MEMS devices are wafer level packaged, two main approaches are used for the electrical connection; lateral feedthroughs and vertical feedthroughs.

For lateral feedthroughs, the electrical signals are horizontally transferred through the outside of the MEMS package by the metal feedthroughs. In the case of the bonding material is not conductive such as glass frit; a capping wafer can directly be bonded on the lateral feedthroughs, sealing the MEMS sensor. However, if the bonding material is conductive, a passivation layer is needed between the bonding material and electrical connection of the MEMS device.

For the vertical feedthroughs, the electrical signals are directly transferred by the vertical conductive vias embedded inside the substrate. This type of connection minimizes the undesired parasitic capacitances since the electrical signals are directly transferred to the outer electronics. This method is compatible with flip-chip bonding and can directly be mounted over the ASIC chip. However, fabrication of a package with vertical feedthroughs is complex and costly.

1.2 Requirements of MEMS Vacuum Packaging

As explained in the previous sections, each MEMS device requires a special operation environment to reach its own specs. While some devices needs vacuum for reaching the optimal operational specs, the other does not. This section presents the requirements of MEMS vacuum packaging.

Typically, there are two types of devices that needs vacuum for the operation. The first group contains resonating structures that require vacuum to reduce damping for achieving higher oscillation amplitudes with smaller actuation voltages. MEMS inertial sensors can be placed into this group. The second group includes sensors

that need vacuum due to high amount of thermal isolation. Microbolometers and RF MEMS sensors can be placed into this group. Table 1.1 presents the vacuum requirements of some common MEMS devices [7], [8].

Table 1.1: Vacuum requirements for some MEMS devices [9].

Sensor	Working Pressure
Accelerometer	300-700 mbar
Resonator	10^{-1}-10^{-4} mbar
Gyroscope	10^{-1}-10^{-4} mbar
RF switch	10^{-1}-10^{-4} mbar
Microbolometers	$<10^{-4}$ mbar

1.2.1 Challenges for MEMS Vacuum Packaging

The main factors affecting the vacuum quality inside a MEMS package are physical leaks, outgassing and permeation of materials used during the fabrication. These factors have to be considered to minimize the degradation of vacuum inside a MEMS package. This section gives a brief explanation about these phenomena's.

1.2.1.1 Leak

A physical leak can be defined as the gas flow into the package through an opening [10]. Since the dimensions of the MEMS packages are so small, physical leaks become a significant issue for the life time performance of the packages.

Table 1.2: Leak rate requirements for vacuum packaged MEMS devices [9].

Class	Leak Rate ($Pa.m^2/s$)
Gross	$>9x10^{-6}$
Moderate	$1x10^{-7}$-$1x10^{-8}$
Fine	$1x10^{-9}$-$1x10^{-10}$
Extra fine	$1x10^{-11}$-$1x10^{-12}$
Super fine	$1x10^{-13}$-$1x10^{-14}$
Ultra Fine	$1x10^{-15}$-$1x10^{-16}$

This type of degradation highly depends on the quality of encapsulation process and can be minimized by successful sealing. The leak rates can be measured using several methods. Helium leak and neon leak tests are the most popular ones. After the test, the leak rate is calculated according to the criteria of MIL-STD-883. Table 1.2 presents the leak rate requirements for hermetically sealed MEMS devices.

1.2.1.2 Outgassing

The outgassing can be defined as the continuous release from the surface of materials [11]. It occurs throughout the life time and it is not possible to completely eliminate it. However, the effect of outgassing can be minimized by the selection of proper materials which have lower outgassing rates. Another way to decrease the outgassing effects is the application of getters inside the sealed volume. Getters absorb the gases whose partial pressures increase inside the package due to the outgassing from the MEMS device or packaging materials. The role of getters on the package performance will be explained in the Section 1.2.1.4.

1.2.1.3 Permeation

Permeation can be defined as the influx of contaminants which goes through the walls of the packaging material by diffusion due to the natural ability of the packaging material.

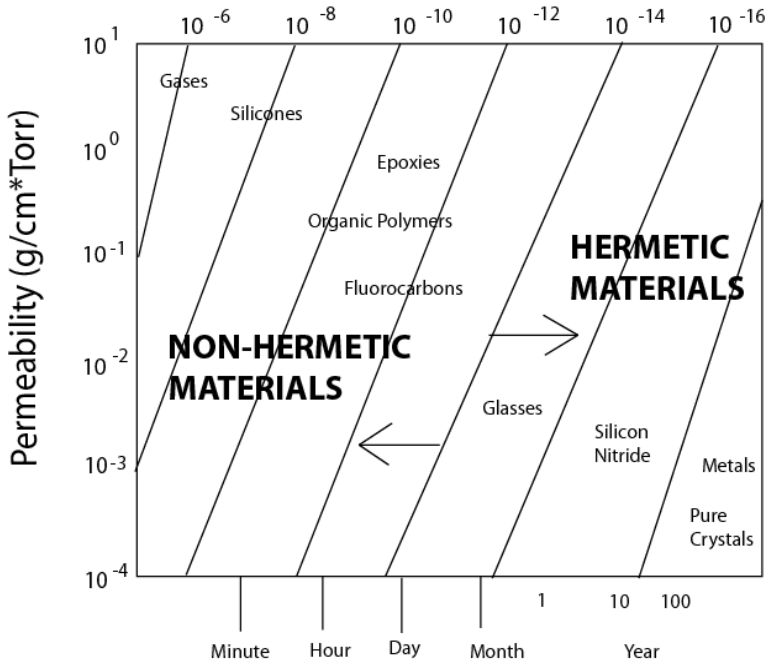


Figure 1.2: Hermeticity of organic and inorganic materials [11].

The effect of permeation can be minimized by the proper selection of packaging material. This selected material has to be a good barrier against diffusion. Figure 1.2 presents the hermeticity of some materials. In this study, typical materials used for the packaging are silicon and glass. Thus, the problem of permeability is minimized.

1.2.1.4 Application of Getters

To maintain the vacuum inside a MEMS package throughout the life time, getters are commonly employed. A getter can be described as an efficient chemical pump which is able to absorb the gas impurities [11], [12]. Getter material has to fulfill some requirements such as chemical stability, mechanical stability, absence of contaminating particles, low gas emission, easy and uniform activation. Considering all these roles and requirements, a getter can be characterized by the following features:

- **Capacity:** The term capacity means the maximum amount of gases absorbed by a getter.
- **Speed:** The amount of absorption per unit time is defined as the speed of the getter. Generally, higher the speed, higher the performance.
- **Selectivity:** Each getter absorbs different types of gases. For instance; while a certain getter alloy can absorb only H_2, another one can absorb all active gases.
- **Conditions of use:** It can be defined as the activation temperature. Lower activation temperature is preferred in order to minimize the risk of damage to the MEMS device when exposed to high getter activation temperatures.

Ti, Zr, Th, and their alloys are examples of the materials which can be used as a getter in a MEMS package. Overall, getters are needed for achieving low pressures during vacuum packaging as well as keeping the pressure stable inside a vacuum package.

1.2.2 Methods of MEMS Vacuum Packaging

There are two applicable methods for the vacuum packaging of MEMS devices; die level packaging and wafer level packaging [13], [14]. Figure 1.3 presents the general process flow of die level packaging. In this method, MEMS device wafer is diced directly after the end of the fabrication. The individual dies are subjected to a series of cleaning steps. After completing the functionality tests of these dies, functional dies are mounted on PCB for integration with its electrical circuit. After completing the tests of the die with its electrical circuit, each die is vacuum packaged one by one.

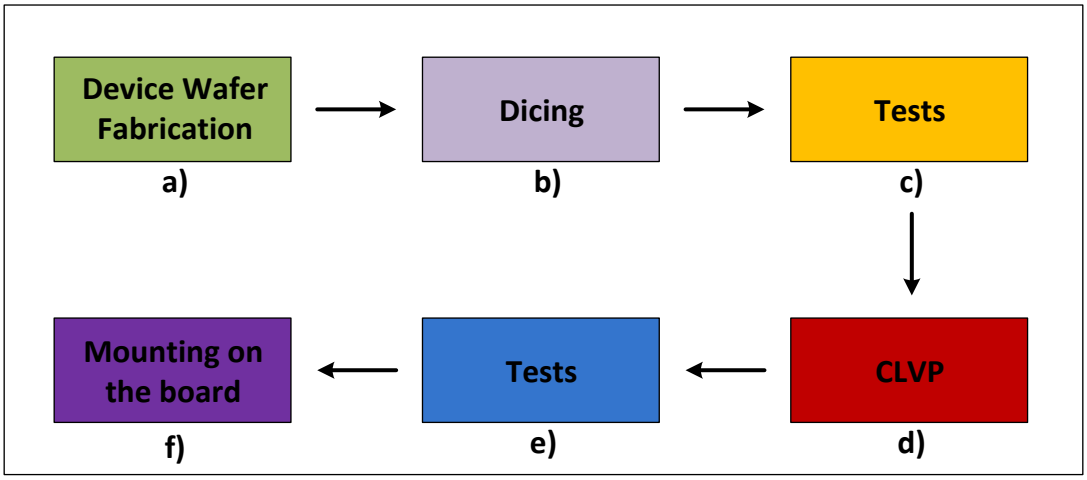


Figure 1.3: The basic concept of die level vacuum packaging: (a) fabrication of device wafer, (b) dicing of the device wafer to obtain individual dies, (c) functionality tests, (d) die level packaging of dies one by one, (e) tests of vacuum packaged dies to see whether vacuum packaging process is successful or not, (f) mounting the vacuum packaged dies on the board for final tests.

Wafer level vacuum packaging method includes an extra fabrication step. This extra fabrication step can be done either by thin film encapsulation or wafer bonding. These techniques will be described in detail in the Sections 1.3.1 and 1.3.2. Unlike die level vacuum packaging, the main advantage of wafer level vacuum packaging is that all dies are vacuum packaged at one time which reduces the packaging and testing cost significantly. Figure 1.4 illustrates the basic process flow of wafer level packaging.

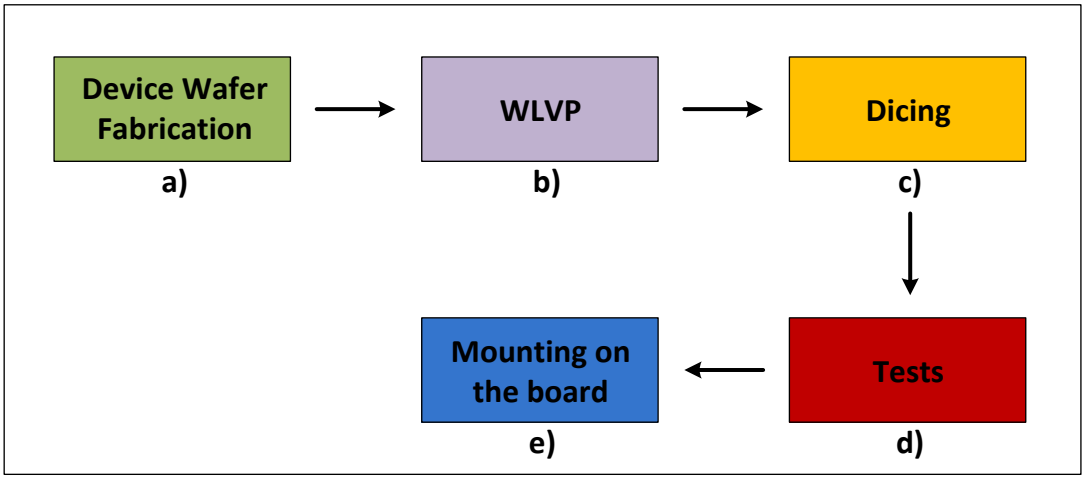


Figure 1.4: The basic concept of wafer level vacuum packaging: (a) fabrication of device wafer, (b) wafer level vacuum packaging process using one of selected wafer level vacuum packaging techniques, (c) dicing of the packaged device wafer to obtain individual dies, (d) tests, (e) mounting the vacuum packaged functional dies on the board for final tests.

1.3 Wafer Level Vacuum Packaging

Two common ways of forming a wafer level vacuum package for MEMS devices are thin film packaging and packaging by wafer bonding [13], [14]. While thin film packaging uses conventional thin film deposition techniques, packaging by wafer bonding technique requires wafer bonding of a cap wafer on the device wafer. This Section gives a brief overview of these methods. Figure 1.5 presents the basic concepts of these methods.

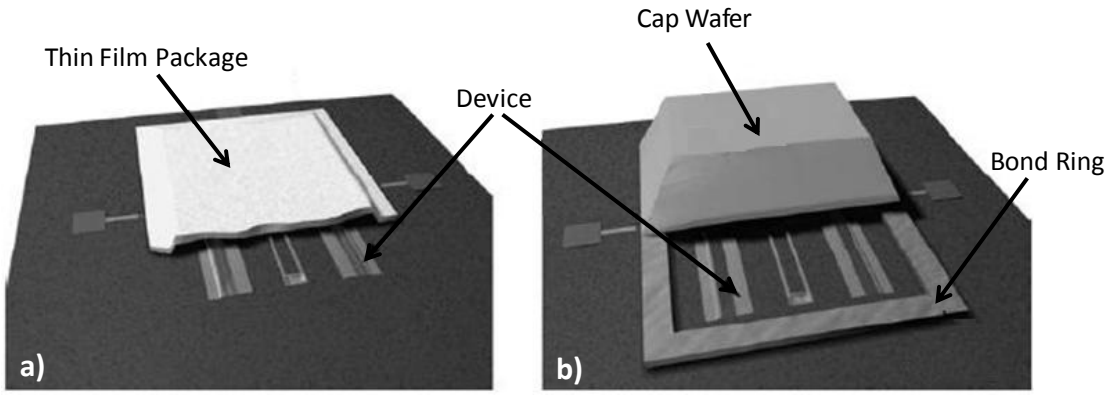


Figure 1.5: Two basic wafer level vacuum packaging approaches: (a) packaging using thin film deposition, (b) packaging using wafer bonding [16].

1.3.1 Packaging by Thin Film Deposition

The way of sealing MEMS devices using thin film deposition is called as thin film packaging. This type of packaging uses deposition and sacrificial layer etching techniques to form a package on the MEMS device. After the end of device wafer fabrication, a series of sacrificial and thin film layers are deposited on the device wafer. The sacrificial layer is then removed using wet or dry etching techniques and the packaging process is completed. If hermeticity is needed, the selection of the packaging material becomes much critical. The selected material has to be a good barrier against the external environment. In the literature, various types of metals, semiconductors and insulators including nickel, polysilicon, amorphous and single crystal silicon, silicon dioxide and polymers are used for that purpose [15]-[20].

Figure 1.6 presents the conceptual process flow of thin film encapsulation. As seen in the figure, after completing the fabrication of the MEMS structure, a sacrificial layer is deposited on the MEMS device. This is followed by the first thin film packaging layer deposition and the formation of etching on holes on it. The sacrificial layer is then released using wet or dry etching techniques. The packaging process is completed by the deposition of another thin film layer, sealing the etch holes in the first layer.

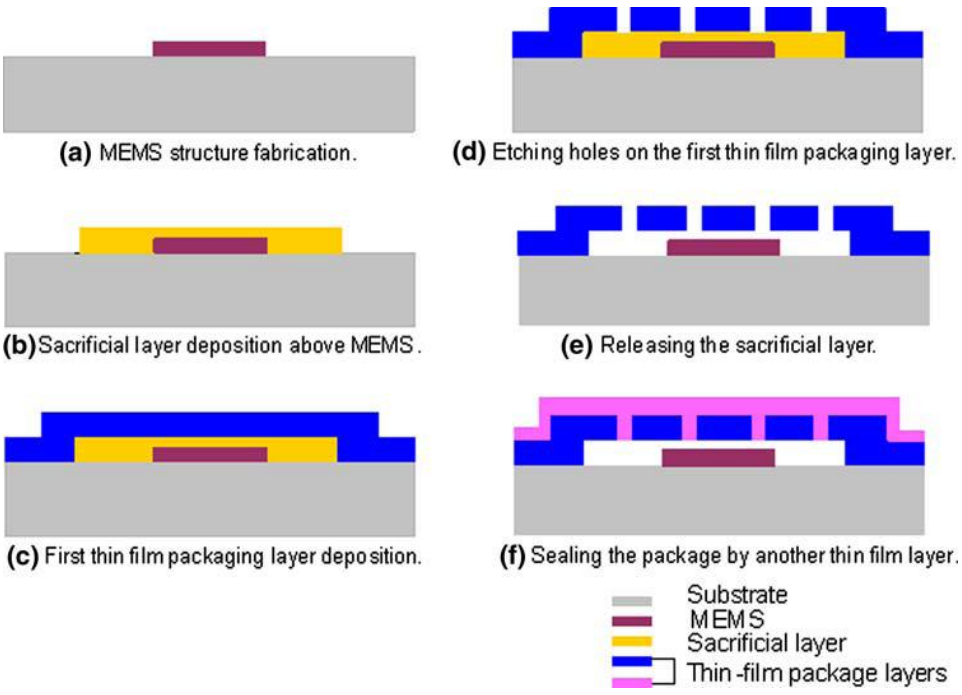


Figure 1.6: A conceptual process flow for thin film packaging [19].

This type of a packaging process offers several advantages. Since there is no need to form a bonding ring for the packaging, the package size is minimized. Moreover, there is no need to fabricate a cap wafer and no need for extra process equipment for packaging process. These decreases the total cost of the packaging process significantly. However, there has been no fully demonstrated thin film encapsulation work in the literature which obtained the performances of the packages formed using wafer bonding technique. Moreover, compared to the packaging using wafer bonding technique, it is a complex process with respect to the number of process masks. The getter integration and the high temperature need for the deposition of some thin film layers are the other problems. Finally, the thermal expansion coefficient difference between the packaging layer and the substrate may cause stress between the packaging layer and the substrate.

In the literature, several authors presented different types of thin film packaging processes. R. N. Candler *et. al.* demonstrated a thin film packaging process in 2004 [15]. They sealed MEMS accelerometers using polysilicon layer as an encapsulation layer. In the same year, B. H. Stark *et. al.* used thin film nickel layer for the packaging process. This study is one of lowest temperature thin film packaging processes reported in the literature. They sealed pirani gauges at nearly 250ºC and obtained a pressure of 1.5 Torr inside the package. Figure 1.7 presents SEM pictures of thin film Ni packages developed in [16], [17].

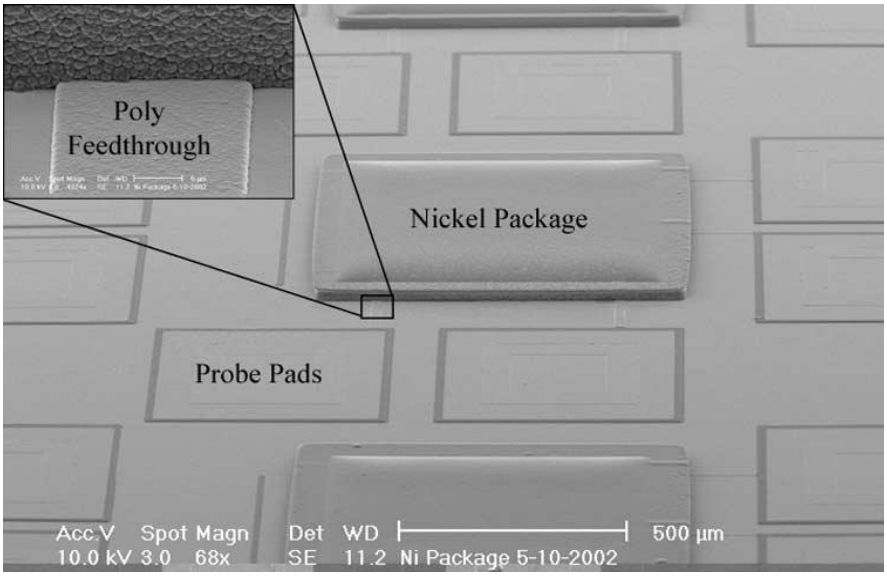


Figure 1.7: A SEM picture of Nickel thin film package developed in 2004 [16].

In 2005, P. Monajemi *et. al.* developed a thin film packaging process using polymers as a package layer [18]. They used micromachined resonators to evaluate the sealing quality and obtained high Q values showing that vacuum packaging process was successful. In 2010, Graham *et. al.* reported another successful thin film packaging process based on the use of epi-silicon as an encapsulation layer on MEMS resonators [20]. Figure 1.8 presents the view of a packaged die developed in this study.

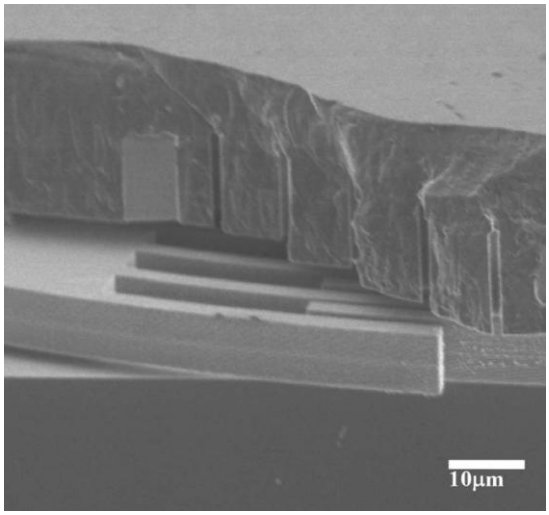


Figure 1.8: Cross section view of sealed resonator die by thin film packaging [20].

Rajaraman *et. al.* reported a thin film packaging study by the use of PECVD a-Si layer. Their study showed that PECVD a-Si can be applied for the thin film packaging process [21]. Figure 1.9 shows one packaged die developed in this study.

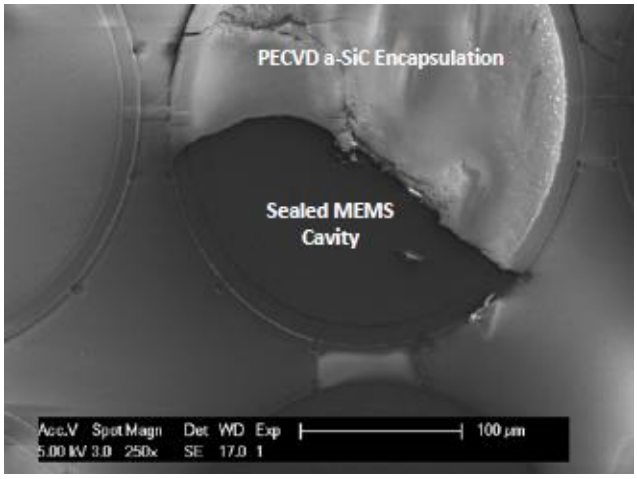


Figure 1.9: Top view of a die sealed by deposition of PECVD a-Si [21].

1.3.2 Packaging by Wafer Bonding

This technique is based on bonding of a cap wafer to the fabricated MEMS device wafer by an additional process step. Various bonding techniques such as anodic, eutectic, glass frit and low temperature fusion bonding can be used for the wafer level vacuum packaging process depending on the requirements. This section presents the description of wafer bonding techniques that can be used for wafer level vacuum packaging process.

1.3.2.1 Anodic Bonding

The most common way of bonding glass and silicon wafers is called anodic bonding. In anodic bonding, silicon and sodium (Na) doped glass wafers are put into contact, heated and an electric field is applied between two wafers. With the effect of temperature and the created electric field, positive Na atoms become mobile and leave the oxygen (O_2) atoms alone at the bonding interface. These oxygen atoms interact with the silicon atoms and form a strong silicon dioxide (SiO_2) bond [22]. Figure 1.10 presents the view of a typical anodic bonding scheme.

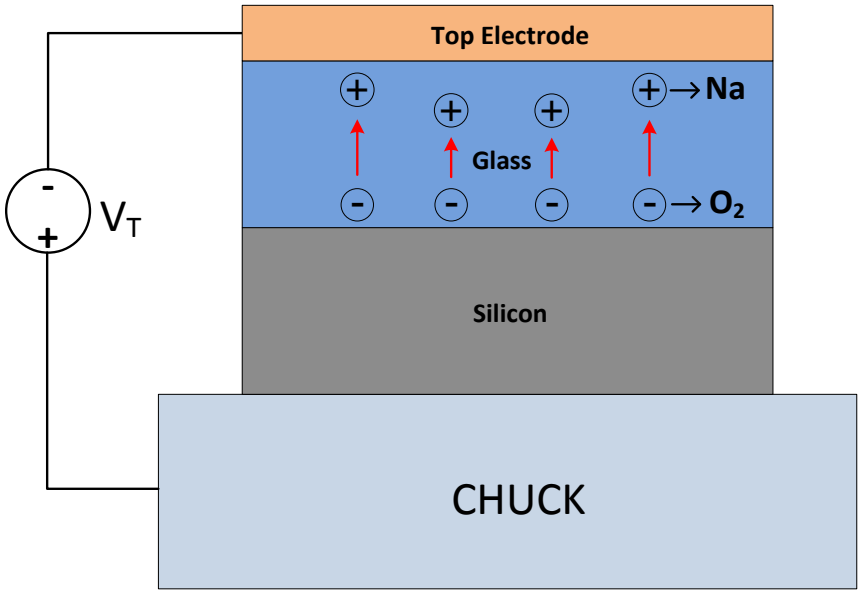


Figure 1.10: A basic anodic bonding scheme.

The main bonding parameters are temperature, applied voltage, time and force. The effect of these parameters on the bonding quality is analyzed in [23]. A typical anodic bonding process can be carried out at temperatures between 300ºC-500ºC and voltages in the range of 500-1500V depending on the application.

A standard anodic bonding (300ºC-1000V) can be used for the wafer level vacuum packaging of MEMS devices. It allows highly reliable vacuum seals at lower temperatures compared to other techniques.

The main drawback of the anodic bonding is that it can only be applied to the specific types of substrates and cap materials and process flows since the surface tolerance of the anodic bonding is in the nanometer range [24] and the need for strong electric field limits the seal of suspended MEMS devices. Moreover, a high amount of oxygen is released during the bonding and a getter has to be integrated into the package for high vacuum levels.

1.3.2.2 Fusion Bonding

The fusion bonding is the way of bonding two polished and chemically active wafer surfaces. It can be used to bond wide range of materials including silicon-silicon, silicon-silicon dioxide, silicon-silicon nitride, silicon-gallium arsenide, and silicon-sapphire [23]. Since a covalent bond is formed, the bonding quality is very high. However, prior to bonding, a treatment is needed to chemically activate the wafer surfaces. This surface treatment can be carried out in a number of ways including wet or dry chemistry. After the surface treatment, wafers are brought into contact and a bond is formed by Van der Waals forces. However, this bond strength is not sufficient to use it in practical applications and has to be increased. To achieve higher bond strengths, wafers are annealed at a temperature where strong covalent bonds forms and as a result bond strength increases significantly. A typical silicon to silicon or silicon to silicon dioxide fusion bonding requires a temperature of 600-1200ºC.

Fusion bonding can not be directly used for the wafer level vacuum packaging of MEMS devices due to its high temperature requirement. Moreover, since fusion bonding has almost no surface roughness or contamination tolerance, it can only be applied on the special process flows.

1.3.2.3 Low Temperature Fusion Bonding

To achieve fusion bonding at lower temperatures, a technique called surface activated bonding is used [25]. The main idea behind this technique is that if the surfaces are clean and free of any other contaminating species, the bond strength is

high even at room temperature. For that purpose, wafers are placed in a vacuum chamber where the wafer surfaces can be chemically activated by using plasma etching, by sputtering a thin layer of material from the surface, by ion beam bombardment or by laser treatment. The high vacuum environment prevents the re-oxidation of surface atoms and if the wafers are brought into contact without breaking vacuum, bonding occurs even at room temperature. Since wafers need to be aligned and then bonded without breaking vacuum, special tools are needed to combine plasma activation and the bonding alignment. Figure 1.11 presents special bonding equipment developed for plasma activated bonding.

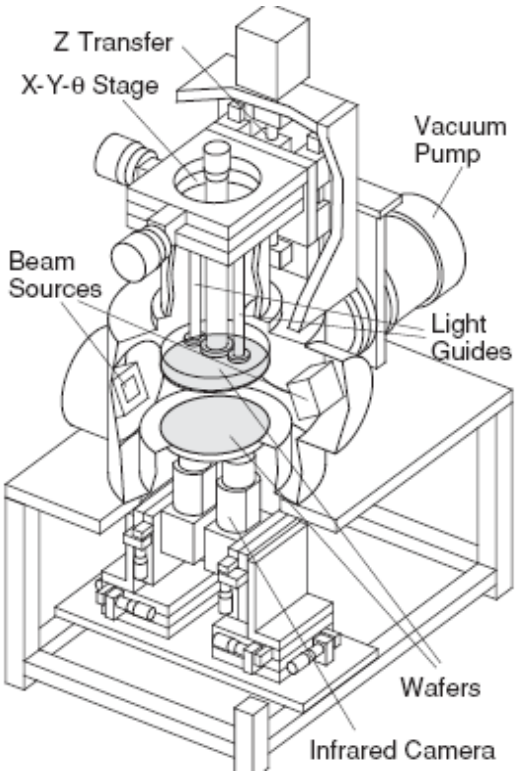


Figure 1.11: Special bonding equipment for surface plasma activated bonding [26].

This technique has an advantage compared to conventional fusion bonding that the bonding can be performed even at room temperature with almost the same bonding strength. Thus, fusion bonding may be applied for packaging of MEMS devices which are temperature sensitive.

1.3.2.4 Eutectic Bonding

The principle of eutectic bonding is based on the formation of an alloy due to diffusion of two materials at their eutectic temperature [23]. The selected materials

are deposited on the bonding interface at a desired composition and forced to have physical contact. Upon heating them above their eutectic point; the surface layer liquidifies due to the interdiffusion. When they are cooled, the mixture solidifies and a strong bond is formed. Figure 1.12 illustrates a eutectic phase diagram.

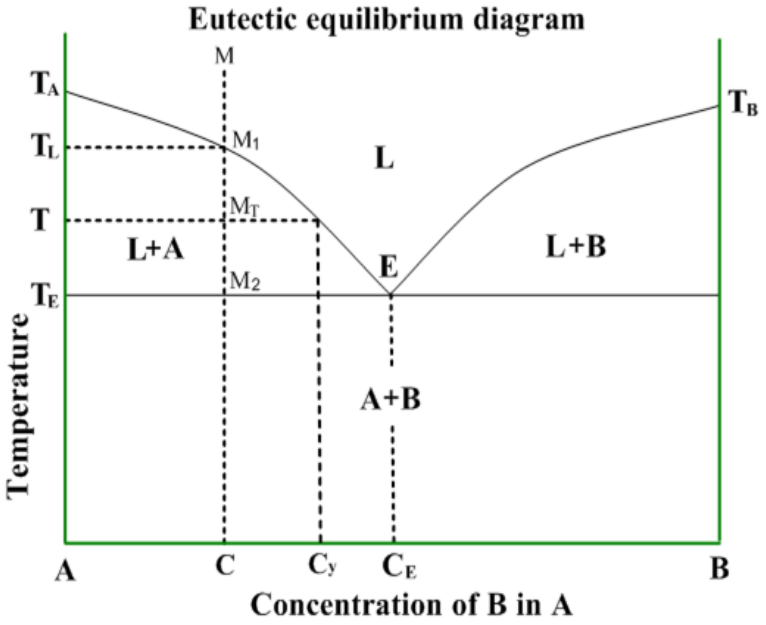


Figure 1.12: A basic eutectic phase diagram.

Various materials can be combined to form a eutectic alloy. Table 1.3 presents the material combinations, their atomic compositions and eutectic points used as a eutectic pair. Au-Si and Au-Sn are the most commonly used eutectic partners used for the wafer level vacuum packaging of MEMS devices [27].

Eutectic bonding offers reliable and high yield vacuum seals. Since the eutectic mixture becomes liquid when it is heated above its eutectic point, this technique can be used for the planarization of the topographic surfaces. This makes eutectic bonding an excellent technique for the wafer level vacuum packaging process. The outgassing rate of the vacuum packages fabricated using this technique is determined by the deposition technique of the eutectic material. In the case of depositing materials by sputtering, the packages suffer from outgassing of argon. As known, since noble gases can not be absorbed by getters, vacuum levels inside the package degrade. In the case of deposition of bonding material by techniques other than sputtering, good vacuum levels can be obtained even without a getter.

Table 1.3: Some famous eutectic pairs.

Alloy	Eutectic Point	Materials	Alloy composition	Melting point
In-Sn	118 ºC	In	%52	156 ºC
		Sn	%48	232 ºC
In-Ag	141 ºC	In	%97	156 ºC
		Ag	%3	962 ºC
Au-Sn	217 ºC	Au	%12	1064 ºC
		Sn	%88	232 ºC
Au-Si	363 ºC	Au	%81.4	1064 ºC
		Si	%18.6	1414 ºC

1.3.2.5 Glass Frit Bonding

The way of bonding two wafers using glass frit material as an intermediate layer is called glass frit bonding [28]. This technique gives chance to bond the wafer on almost any type of material or wafer. The principle of the bonding is based on the heating and applied pressure. In the case of contacting the wafers to be bonded at the desired temperature, the glass frit material softens, covers the surfaces of the wafers, and upon cooling a strong bond is formed.

Glass frit bonding is one of the most reliable and high yield wafer level vacuum packaging methods applied to a wide range of devices and processes. It has the high capability of providing planarization over topographic surfaces up to about 2 µm steps which is an essential property for hermeticity. Moreover, the glass frit is an insulator material and thus it can be directly applied on the electrical feedthroughs of the MEMS devices. The outgassing rate depends on the selected glass frit material. Typically, CO or C_xH_y typed gases are outgasssed during the life time which can be easily absorbed by the integrated getter material. Therefore, good vacuum levels can be obtained with the use of getters in this technique.

The main drawback of glass frit bonding is the high process temperature. Glass frit bonding is typically performed at the temperatures ranging from 435ºC to 450ºC. Thus, in the case of bonding of different types of wafers, the thermal mismatch will

cause a residual stress after cooling. Besides, the bonding line width and resolution is typically limited with the screen printing technique which is used for the glass frit deposition.

1.3.3 Summary of Wafer Level Vacuum Packaging Technologies

This section summarizes previously explained wafer level vacuum packaging approaches in respect to bonding temperature, bond strength, amount of outgassing during the life time, bonding line width, tolerance to surface topography, expected vacuum levels with or without getters, and the leak rate. Table 1.4 summarizes these technologies.

Table 1.4: Summary of Wafer Level Vacuum Packaging (WLVP) technologies.

	Anodic Bonding	**Low Temp. Fusion Bonding**	**Eutectic Bonding**	**Glass Frit Bonding**	**Thin Film Packaging**
Bonding Temperature (ºC)	300-400ºC	200-400ºC	Au-Si: 390-420ºC Au-Sn: 280-300ºC	430-450ºC	300-450ºC
Bond Strength	High	High	High	High	High
Outgassing due to Bonding line	O_2	H_2, H_2O	Noble Gases	CO, C_xH_y	-
Bonding Line Width (µm)	>20 µm	>30% Surface Coverage	>60µm	>250µm	>20µm
Tolerance to Topography (µm)	30 nm	0	Up to 1µm	Up to 2µm	Up to 3µm
Vacuum Level without Getter	Medium	Unknown	Good	Medium	Medium
Vacuum Level with Getter	High	Problem of Activation	Au-Si: High Au-Sn: Problem of Activation	High	-
Leak Rate	Low	Very low	Low	Low	Very Low

1.4 Previous Works on Wafer Level Vacuum Packaging

Since 90's, wafer level vacuum packaging by wafer bonding has been used widely. This section presents some of the significant studies, see also Table 1.5, achieved using anodic, glass frit, and eutectic bonding in the literature.

In 2000, Song *et. al.* presented a vacuum packaging study based on the glass frit bonding [29]. They sealed MEMS gyroscopes using glass frit bonding technique at 450ºC without a getter material. The gyroscopes were used to determine the pressure level inside the micro packages and found as 150mTorr. No long term test data belongs to this study was given.

Another work was published by Sparks *et. al.* in 2001 [30]. Micromachined resonators were wafer level vacuum packaged using solder bonding. They did not use a getter material and obtained 1.5 Torr inside the packages. They observed that there was no change in pressure levels in the packages even after 42 days.

In 2002, Chavan *et. al.* reported another wafer level vacuum packaging work [31]. They fabricated capacitive pressure sensors, packaged by anodic bonding and used them for the monitoring of the pressure levels inside the packages. They obtained a pressure of 0.5 Torr after the process without getter.

In 2003, two similar works based on the wafer level vacuum packaging using anodic bonding were published by Lee *et. al.* and Capler *et. al.* Lee *et. al.* sealed micromachined resonators and used them to measure the pressure inside the packages [32], [33]. Moreover, they carried out a series of experiments to evaluate the amount of Ti material as a getter on the pressure levels. They observed that Ti works as a getter and by changing the surface area of the Ti, lower pressure levels have been achieved from 1 Torr to 1mTorr. They also reported that pressure inside packages were stable after 42 days. On the other hand, Capler *et. al.* used the Nanogetters^{TM} inside their packages and calculated the pressure levels as 3mTorr after the packaging process. They did not present any long term test results.

In 2005, Sparks *et. al.* presented another packaging by glass frit bonding. They detected high vacuum levels inside the packages using the deflection test and integrated resonators. Furthermore, they subjected these packages to a series of bake tests to estimate the package performance throughout the life time [34].

Table 1.5: Previous WLVP works done in the literature.

Author/Year	Wafer Bonding Technique	Sensor	Pressure	Getter	Long Term Data
H. Song *et. al.* /2000 [29]	Glass Frit	Gyroscope	150 mTorr	-	-
D. Sparks *et. al.* /2001 [29]	Solder	Resonator	1.5 Torr	-	42 days
Chavan *et. al.* /2002 [31]	Anodic	Pressure Sensor	0.5 Torr	-	-
B. Lee *et. al.* /2003 [32]	Anodic	Resonator	1 mTorr	Ti	42 days
S. Capler *et. al.* /2003 [33]	Anodic	Resonator	3 mTorr	Nanogetters	-
D. Sparks *et. al.* /2005 [34]	Glass Frit	Resonator	850 µTorr	Nanogetters	-
W. Reinert 2006 [35]	Au-Si Eutectic	Resonator	7.5 Torr	-	-
J. Chae *et. al.* /2008 [36]	Anodic	Pirani Gauge	33 Torr	-	4 month
J. S. Mitchell *et. al.* / 2009 [37]	Au-Si Eutectic	Pirani Gauge	25 mTorr	Nanogetters	4 years
A .Yu *et. al.* / 2010 [38]	Au-Sn Eutectic	Resonator	1 Torr	-	1 week

Wolfgang *et. al.* reported a wafer level vacuum packaging study in 2006 [35]. They packaged micromachined resonators using Au-Si eutectic bonding and obtained a pressure of 7.5 Torr inside the package without getter.

In 2008, Chae *et. al.* published a study based on the wafer level vacuum packaging of MEMS Pirani vacuum gauges using anodic bonding [36]. The pressure inside the packages was found as 33 Torr using these Pirani vacuum gauges. Moreover, they observed that pressure inside the packages remained as 33 Torr after 4 months even without getters.

Another work based on the wafer level vacuum packaging using Au-Si eutectic bonding was published in 2009 by Mitchell *et. al*. [37]. In this work, several experiments on the quality, reliability and yield of Au-Si eutectic bonded packages were carried out. They evaluated the performance of the micro packages using Pirani vacuum gauges and observed that the pressure remained stable as 25mTorr over 4 years using Nanogetters^{TM}.

In 2010, Yu *et. al*. published a study based on the development of a packaging process using Au-Sn eutectic bonding [38]. The packaging process was done at 280ºC, the main advantage of this work, and micromachined resonators were used for characterization. They observed that pressure remained stable as 1 Torr for 1 week.

1.5 Research Objectives and Thesis Organization

The aim of this study is to develop one or more wafer level vacuum packaging processes for MEMS devices fabricated at the METU-MEMS Research and Application Center. The specific objectives of this research are presented as follows;

1. Design of micromachined resonating structures and pirani vacuum gauges to monitor the pressure inside the packages. Modeling of pirani gauges and resonating structures should be done using Coventorware and MATLAB. The sensors should be designed such that they will monitor pressure levels in the range of 1mTorr- 10Torr.
2. Optimization of Au-Si eutectic and glass frit bonding for wafer level vacuum packaging. The Au-Si bonding optimization on topographic and non-topographic surfaces should be evaluated using both glass and silicon wafers.

The Au-Si bond quality should be verified by a technique based on the deflection of a diaphragm due to the pressure difference. The investigation of glass frit bonding quality at different surfaces including Si/Glass Frit to Glass, Si/Glass Frit to Silicon, Si/Glass Frit to Gold and Si/Glass Frit to Silicon Nitride should be performed. The bonding quality should be examined by optical microscope and SEM.

3. Fabrication of MEMS gyroscopes, resonators, and pirani vacuum gauges that will be used for the evaluation of wafer level packaging process. Development of new 7-masked Silicon-on-Glass (SOG) process for devices with lateral feedthroughs. This process has to be compatible with the wafer level packaging process by Au-Si eutectic and glass frit bonding. The problems faced during the device fabrication especially in device release and contact regions should be solved. On the other hand, a separate study for the fabrication of similar devices with vertical feedthroughs should be done. Cap wafers with pad windows for testing for devices with lateral feedthroughs and cap wafers for devices with vertical feedthroughs should be designed and fabricated. The cap wafers that will be used for glass frit bonding should be sent to the company, Nanogetters^{TM}, for glass frit deposition.
4. Sensor level tests of MEMS gyroscopes, resonators, and pirani gauges. The functionality tests of the fabricated MEMS resonators, gyroscopes and pirani gauges should be performed under atmospheric pressure. These devices should then be placed inside a vacuum chamber and their response should be observed at vacuum. Extraction of quality factor versus pressure graphs for resonating structures and the extraction of thermal impedance versus pressure graph for pirani gauges should be completed.
5. Wafer level vacuum packaging using Au-Si eutectic bonding and glass frit bonding. The optimized Au-Si eutectic and glass frit bonding recipes should be applied on the device wafers fabricated with newly developed Silicon-On-Glass (SOG) process. The wafer level vacuum packaged dies should be tested to evaluate the success of the packaging process. A comparison should be done between the packages fabricated using glass frit and Au-Si eutectic bonding with identical MEMS device fabrication steps. These packages

should be subjected to long term tests to predict their long term performances.

The organization of the thesis and the contents of the following chapters are summarized as follows;

Chapter 2 starts with the description of the methods used for the evaluation of the wafer level vacuum packaging process, specifically focusing on the resonating structures and pirani vacuum gauges. It describes the theoretical background necessary for the design of MEMS resonating structures and pirani gauges. The simulation results of the designed devices are also presented in this chapter.

Chapter 3 provides information about the theory and requirements of the Au-Si eutectic and glass frit bonding. It presents the experimental results obtained during the optimization of the Au-Si eutectic and glass frit bonding. Moreover, it describes the fabrication of MEMS devices with lateral and vertical feedthroughs using a new SOI based SOG process and followed by the design and fabrication of cap wafers for these devices. It finally gives the results of the wafer level vacuum packaging process.

Chapter 4 presents the test results of the fabricated MEMS gyroscopes, resonators and pirani vacuum gauges in both atmospheric and vacuum environmental conditions. It also presents the characterization of MEMS devices before the packaging and after packaging processes. It finally gives the performance results of micro packages.

Chapter 5 summarizes the conclusion of this study and the possible future works.

CHAPTER 2

VACUUM SENSOR DESIGN

Reliability is the major interrupting block for the application of MEMS wafer level packages into the industry. A MEMS package has to be subjected to a series of experiments to evaluate some performance parameters including hermeticity and stability during the life time before use. Thus, testing becomes a significant issue in the design of a reliable MEMS package. Testing methodologies of wafer level vacuum packages can be classified into two main groups; external testing and testing by an integrated device.

External testing involves the leak rate and deflection tests. In the leak rate test, the package is placed inside an environment where a pressured gas, typically helium or neon, is applied on it for a period of time. The pressured gas enters the package if there is a leak. The package is then placed into a vacuum chamber and left alone so that the gas leaks out. The amount of gas entered inside the package is determined by a mass spectrometer which is previously connected to the vacuum chamber and the leak rate is calculated according to the criteria of MIL-STD-883. The hermeticity of the package can easily be tested using this method. The advantage of this method is that there is no need of an integrated sensor. However, this test gives no information about the vacuum levels inside the package. Moreover, it is difficult to apply this test on the packages with small dimensions due to the sensitivity of leak detector. Furthermore, the need of special equipments for testing makes this method costly. The second external method is the deflection test. It is based on the deflection of the thinned packaging material due to the pressure difference between the atmosphere and the sealed cavity of the package. The dimensions and mechanical properties of the packaging material can be used to calculate the pressure inside the package once the amount of deflection is measured. The deflection can be

measured using conventional metrology equipments such as optical and surface profilers. This is a simple method which does not only test the hermeticity of the package but also gives information about the vacuum level. However, the residual stress of packaging material may cause an error in the deflection measurement which results less accuracy in pressure prediction. In addition, this is a destructive test method since the packaging material has to be thinned to a known thickness where the amount of deflection can be measured.

The second group of test methodology includes the evaluation of the package using an integrated vacuum sensor. Micromachined resonating structures and pirani gauges are used for that purpose and both the hermeticity and vacuum levels of MEMS packages can be evaluated using these devices. The principle behind the use of resonating structures for vacuum characterization is based on the quality factor extraction. The ambient pressure is inversely proportional to the quality factor. Similarly, pirani vacuum gauges provide excellent solution for monitoring the pressure inside MEMS wafer level packages. The pirani gauge consists of a suspended resistor whose resistance changes as a function of ambient pressure. Both types of sensors are used for the evaluation of the package quality in this work. This chapter gives detailed information about these devices considering the design and modeling. Section 2.1 starts with the overview of MEMS resonating structures. Section 2.2 describes the design procedures of a MEMS resonator including actuation mechanism, spring, mass and damping factor estimation and FEM simulations. Section 2.3 provides information about the theory of MEMS pirani gauges. Section 2.4 explains the modeling and design procedures of a MEMS pirani gauge. Section 2.5 presents the thermal analysis of pirani gauges in Coventorware. Section 2.6 gives information about previously developed pirani gauge structures at METU. Section 2.7 describes the pirani gauges developed in this study. Finally, Section 2.8 ends with a brief summary of this chapter.

2.1 Overview of MEMS Resonating Structures

Today, MEMS resonating structures find use in a wide range of applications from automotive control systems to the military. Typical resonating devices used for different type of applications are gyroscopes, accelerometers, and resonators. This type of devices can also be used for the evaluation of pressure levels inside a MEMS

package. The theory behind this is the quality factor extraction. The pressure is inversely proportional to the quality factor of a resonating structure and pressure inside the package can be predicted if the quality factor of device is known. This section gives a short description of resonating type devices.

A simple micromachined resonator consists of a mass, spring and damper system as shown in Figure 2.1. In the case of moving the system by an external force, the resonance frequency where the system naturally oscillates can be written as in the Equation 2.1 where k is the spring constant and m is the mass of the system.

$$f_r = \frac{1}{2\pi}\sqrt{\frac{k}{m}} \tag{2.1}$$

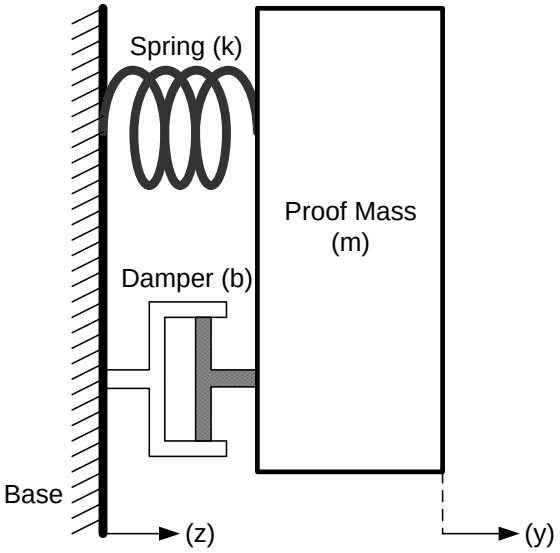


Figure 2.1: A simple micromachined resonator device [40].

This kind of a system can be modeled using the second order differential equations as given in Equation 2.2;

$$F(t) = m\frac{\partial^2 x(t)}{\partial t^2} + b\frac{\partial x(t)}{\partial t} + kx(t) \tag{2.2}$$

where F is the force acting on the system, m is mass of the moving parts of the system, b and k are the damping factor, and spring constant of the system,

respectively. The model can be converted to the frequency domain using Laplace transformation as in Equation 2.3.

$$\frac{X(s)}{F(s)} = \frac{1}{m(s^2 + \frac{b}{m}s + \frac{k}{m})} \quad 2.3$$

The Equation 2.5 is obtained by placing the Equations 2.1 and 2.4, where Q is defined as the quality factor of the resonator, into Equation 2.3 and rearranging them under resonance condition.

$$Q = \frac{\sqrt{km}}{b} \quad 2.4$$

$$\frac{X(jw)}{F(jw)} = \frac{1}{j}\frac{Q}{k} \quad 2.5$$

Expressing the model in the frequency domain provides a direct relation between the applied force (*F*) and the deflection (*X*) in terms of mechanical parameters and the frequency of the applied force. The quality factor *(Q)* varies with the damping factor *(b)*, which depends on the ambient pressure.

2.2 Design of MEMS Resonators

The design procedures of a MEMS resonator are based on the design in both mechanical and electrical domain. Mechanical design procedures include spring constant, mass and damping factor estimation whereas the electrical design contains electrostatic actuation mechanisms. The verification of these parameters is then carried out in FEM simulations. This section gives a brief overview about these design procedures.

2.2.1 Spring Constant, Mass and Damping Factor Estimation

The resonance frequency of the system is one of the significant design parameter in micromachined resonators. Since the resonance frequency has a direct relation with the spring constant and the mass of the system, the spring and mass estimation becomes important.

A spring should provide the easiness of movement in the sensitive direction and the difficulty of movement in the other directions. Therefore, the spring constants at all direction have to be calculated. In this study, dual folded flexures are used and a detailed analysis on this type of flexures can be found in [39].

The mass estimation is other key parameter taking into account in the resonance frequency calculation. The total mass of the system is calculated by multiplying the volume of moving parts with the density of the structural material.

Damping is known as the dissipation of vibration energy. Air damping, thermo elastic damping, anchor, and electronic damping are the four main damping mechanisms in resonant structures. Typically, air damping is dominant at atmospheric pressure. In vacuum environment, the effect of air damping minimizes and the other damping mechanisms become dominant in the system. A detailed analysis on the damping can be found in [39], [40].

2.2.2 Electrostatic Actuation using Parallel Plate Capacitors

The parallel plate is a simple and commonly used configuration in micromachining technologies. The principle behind the electrostatic actuation using parallel plate capacitors is the attraction of two opposite charge plates. The detailed analysis of the parallel plate configuration can be found in [39]. Two basic parallel plate configurations can be used for the actuation mechanism of a micromachined resonator are varying overlap area and varying gap.

For the varying overlap area, the movement is generated along the lateral direction and as a result the capacitance is varied by the change of overlap area. The force between the plates can be expressed as in the Equation 2.6 for this configuration where N is the number of capacitors, V is the applied voltage consists of both DC and AC components, $\mathcal{E}_0$ is the permittivity of free air, t and d are the thickness and gap, respectively.

$$F = \frac{1}{2} N V^2 . \mathcal{E}_0 . \frac{t}{d} \qquad 2.6$$

As seen in the Equation 2.6 the varying overlap area configuration is independent from the overlap area and large displacements can be obtained. For the varying gap

configuration, the movement is generated along the y direction while the gap between the parallel plate's decreases, the anti gap increases. The force equation for this configuration can be written as in Equation 2.7 where N is the number of capacitors, $\mathcal{E}_0$ is the permittivity of air, *t* and *l* are the thickness and overlap area, *V* is the applied voltage.

$$F_y = -\frac{1}{2} N \mathcal{E}_0 t l \left(\frac{1}{(d_{gap} - y)^2} - \frac{1}{(d_{anti-gap} + y)^2} \right) V^2 \qquad 2.7$$

2.2.3 Micromachined Resonators Developed in This Study

In this study, two different resonators based on the varying gap and varying overlap area configurations are developed. This section presents these designs and the verification of designs by FEM simulations.

2.2.3.1 Design-1

This design consists of a resonator with varying overlap area configuration. In the design, there are 2 electrodes for driving the resonator by a differential AC signal, 2 electrodes for differential sensing, and 1 for application of DC signal for proof mass. Figure 2.2 and Table 2.1 present a simplified version of the layout and the design parameters of Design-1.

Table 2.1: Design parameters of resonator Design-1.

Parameter	Driving Electrode	Sensing Electrode
# of fingers (*N*)	210	112
Finger overlap length (*l*)	30 µm	30 µm
Finger width (*w*)	4 µm	4 µm
Finger thickness (*t*)	35 µm	35 µm
Finger gap (*d*)	1 µm	1 µm
Capacitance (*C*)	1.95 pF	1.04 pF
dC/dX	6.5×10^{-8} F/m	3.47×10^{-8} F/m

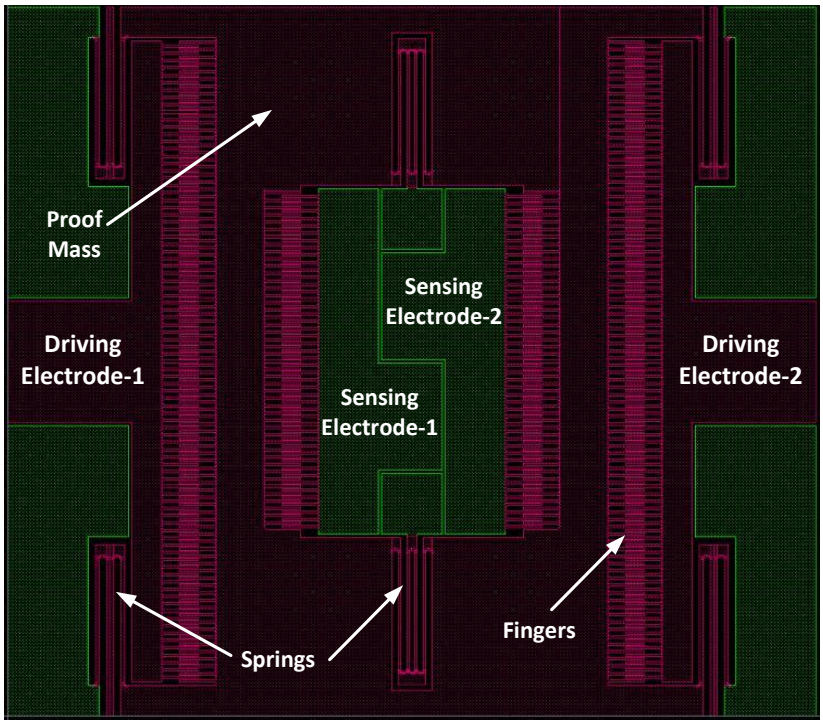


Figure 2.2: Layout of Design-1.

2.2.3.2 Design-2

This design consists of a resonator with varying gap configuration. In the design, there are 1 electrode for driving the resonator by an AC signal, 1 electrode for sensing, and 1 for application of DC signal for proof mass. Figure 2.3 and Table 2.2 present a simplified version of the layout and design parameters of Design-2, respectively.

Table 2.2: Design parameters of resonator Design-2.

Parameter	Driving Electrode	Sensing Electrode
# of fingers (*N*)	56	56
Finger overlap length (*l*)	30 µm	30 µm
Finger width (*w*)	4 µm	4 µm
Finger thickness (*t*)	35 µm	35 µm
Finger gap (*d*)	1 µm	1 µm
Capacitance (*C*)	1.65 pF	1.65 pF
dC/dX	1.65×10^{-6} F/m	1.65×10^{-6} F/m
Capacitance anti gap	0.41 pF	0.41 pF
dC/dX	1.03×10^{-7} F/m	1.03×10^{-7} F/m

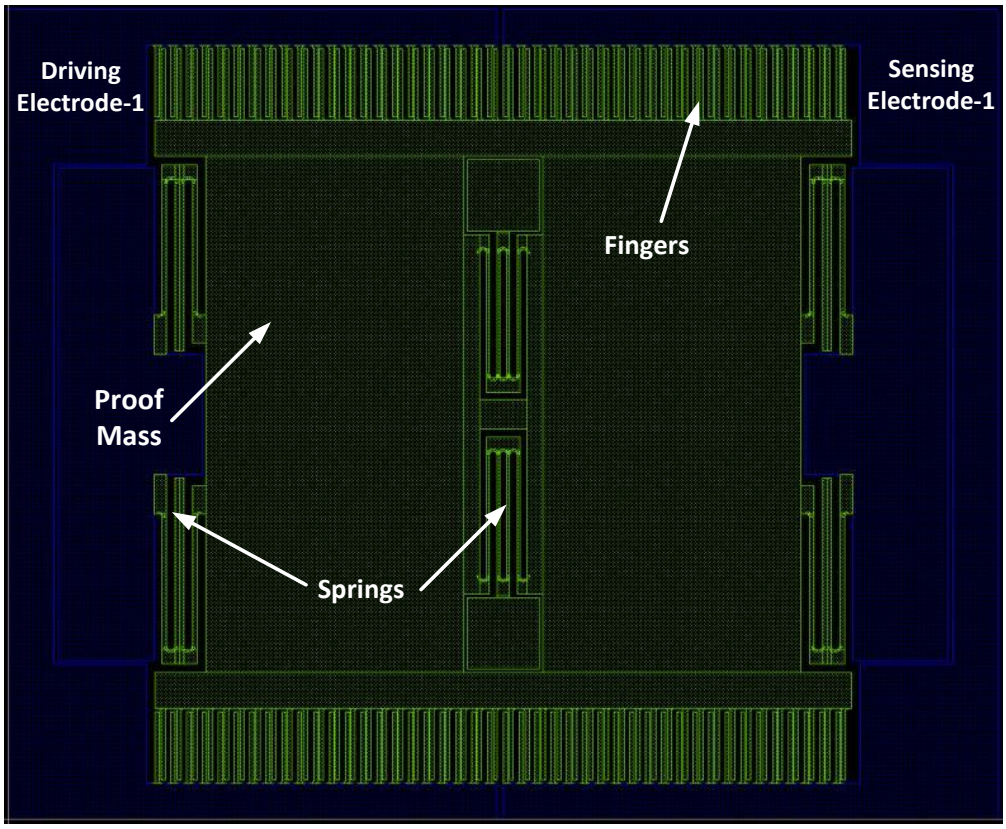


Figure 2.3: Layout of Design-2.

2.2.4 Finite Element Simulations

FEM simulations are important in analyzing the performances of resonating structures. The assumptions done for some simplification always cause some errors. Thus, the design has to be verified by a series of simulations and if there is any missing point, it should be corrected or modified. This section presents the modal analysis of two resonator designs in Coventorware.

2.2.4.1 Design-1

The Design-1 is the comb finger typed of 35 µm thick MEMS resonator having a resonance frequency of 15 kHz. The value of the resonance frequency is selected as 15 kHz for eliminating any susceptibility to the environmental vibrations and noise. The aim of the FEM simulation is to analyze the modes of the resonator, compare with hand calculations and examine their movements. It should be noted that rigid parts have not been included into the simulations because they significantly increase the simulation time, rather proper boundary conditions are assigned to the moving parts that connect to a rigid body.

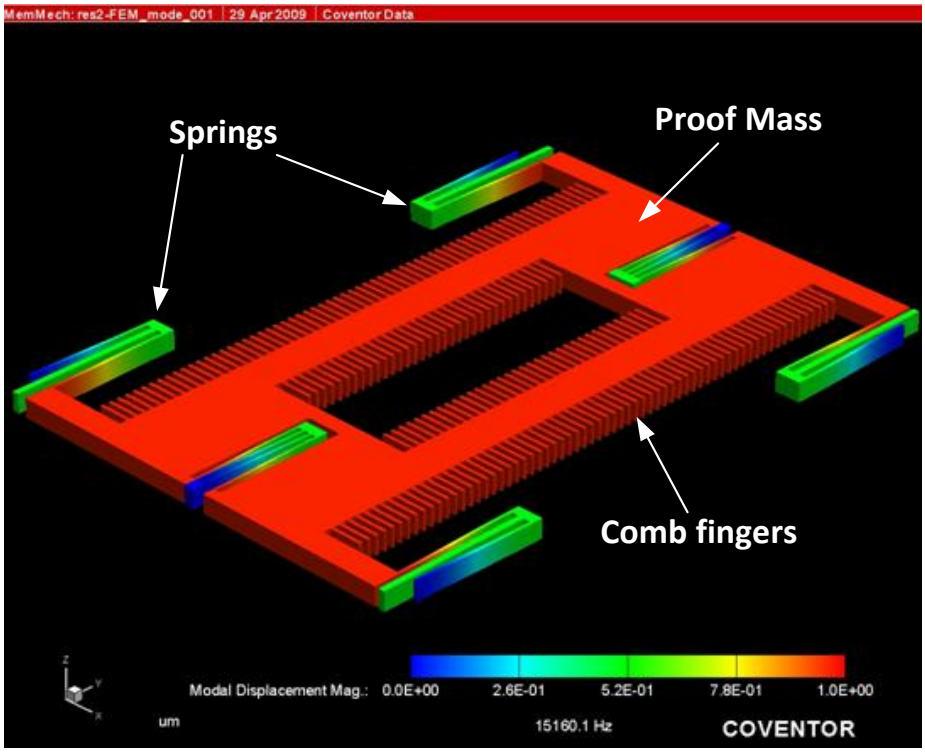


Figure 2.4: First mode of Design-1. The frequency is 15.1 kHz, which is close to the designed frequency of 15 kHz.

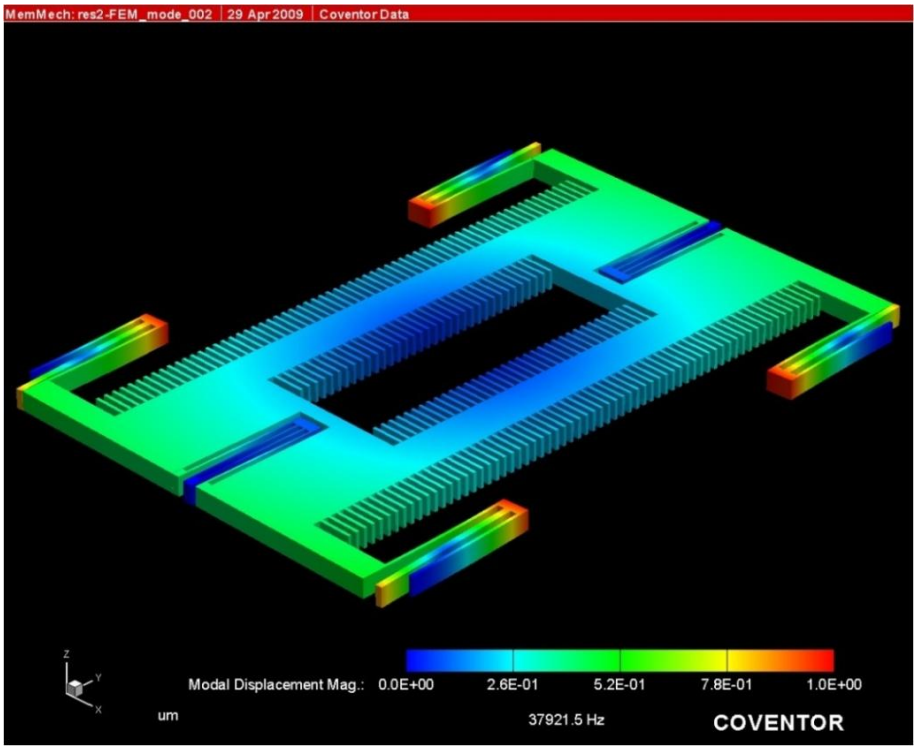


Figure 2.5: Undesired mode which has a movement to out of plane (second mode) at 37.9 kHz.

The first mode of the Design-1 has a movement at 15.1 kHz very close to the hand calculation. The assumptions for the simplicity cause a difference of 155 Hz between the simulation results and hand calculations which are not important and can be neglected. The second mode has a movement to out of plane, an undesired mode. However, it is far away enough from the first mode. Figure 2.4 and Figure 2.5 present the first and second modes of the Design-1, respectively.

2.2.4.2 Design-2

The Design-2 is subjected to the same simulation procedures and its modes are analyzed. The resonance frequencies of the first and second modes are found as 15.1 and 41.7 kHz, respectively. The first mode is almost equal to the hand calculation and the second mode is far away enough from the first mode. Figure 2.6 and Figure 2.7 present the first and second modes of the resonator.

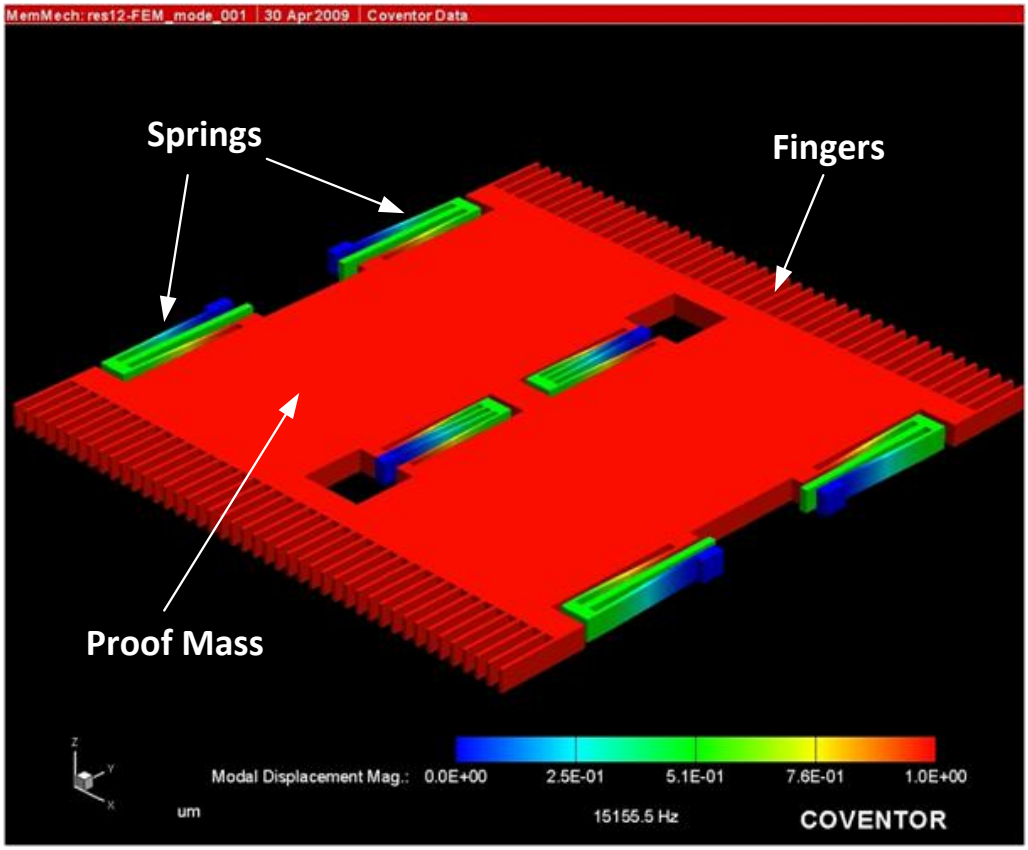


Figure 2.6: First mode of Design-2 at 15.1 kHz. The estimated frequency is 15 kHz, which is close to the simulation result.

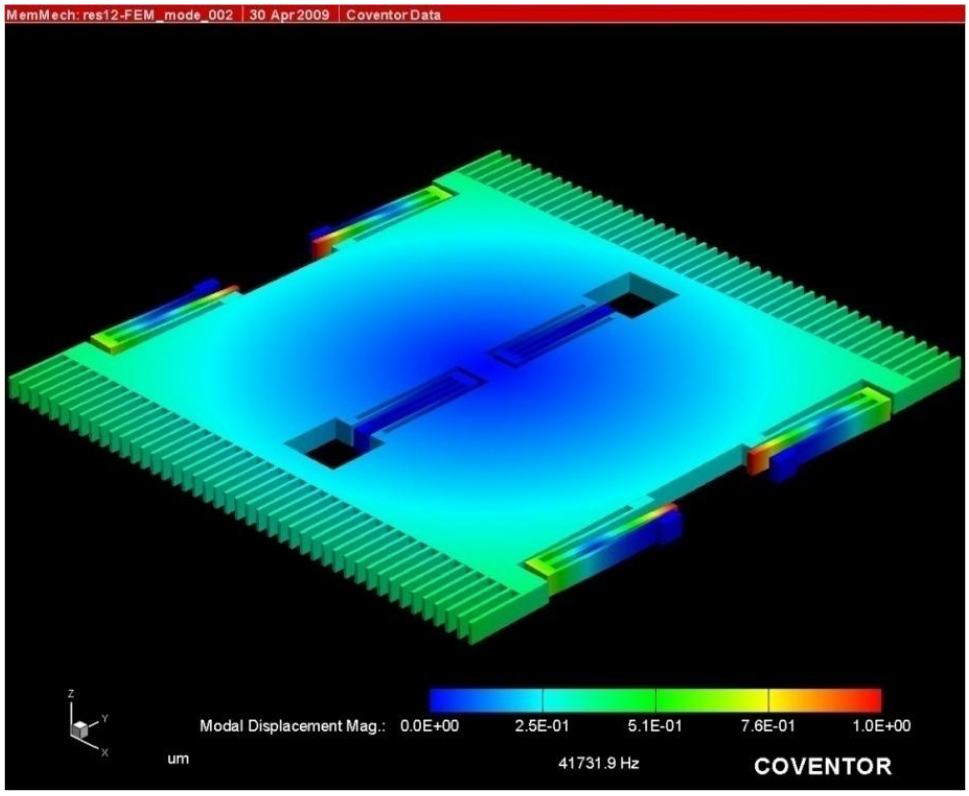


Figure 2.7: Undesired mode which has a movement to out of plane (second mode) at 41.7 kHz.

2.3 Overview of MEMS Pirani Gauges

Pirani gauge consists of a suspended resistor and in the case of an applied current, the temperature of the resistor changes depending on the heat conduction through the gas between the gauge and the heat sinks. The amount of heat conductance directly depends on the pressure of gas. Therefore, there is a direct relation between the ambient pressure and the resistor. This relationship can be used for the measuring the pressure inside the packages.

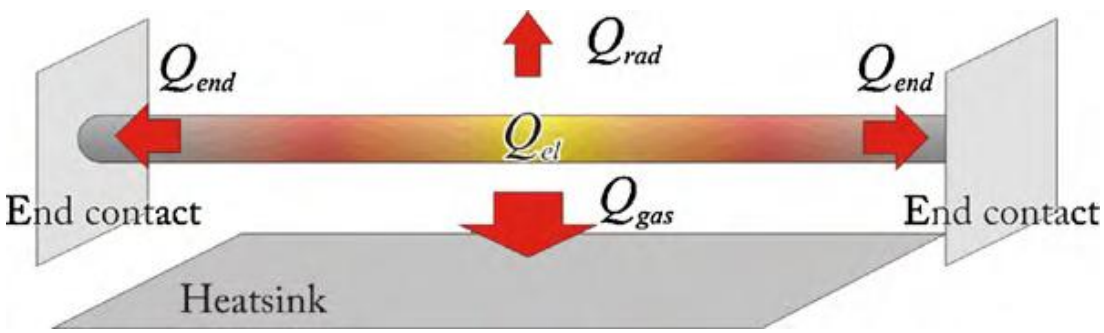


Figure 2.8: Heat loss mechanisms in pirani gauge [51].

To better explain the operation principle of pirani gauge, the heat loss mechanisms should be reviewed. In a typical pirani gauge structure shown in Figure 2.8, the heat conduction is provided by three main sources; radiation, solid and gas conductance. The radiation conductance is negligible for the pressure regimes where pirani gauge operates. For the solid and gas conductance, pirani gauge should be examined in three regions. At high pressures, the distance between the surrounding gas atoms are much smaller than the gap of the pirani gauge. Therefore, the gas has a constant thermal conductance and the pirani gauge is almost insensitive to pressure changes in this region. Reducing the gap between the resistor and heat sinks is the only way of increasing the sensitivity of pirani gauge at high pressures. At moderate pressures, the distance between the gas atoms are much larger than the gap of pirani gauge and the gas atoms interact with each other. As a result pirani gauge is sensitive to the pressure changes in this region. At lower pressures, solid conductance becomes dominant. It can be defined as the heat transfer from resistor to substrate due to the anchors. Thus, the lower pressure limit of the device is determined by the amount of the contact area to anchors. Overall, the pirani gauge should be designed with a minimum gap spacing and minimal solid conductance to obtain a large dynamic range.

Typical pirani gauge structures can be classified into two main groups; the membrane and microbridge structures.

- **The membrane structure:** This structure includes the fabrication of a thin film resistor on a dielectric membrane. Materials with high TCR values including metals and polysilicon are used for the resistor material. To overcome the potential stress in the thin film resistor, a dielectric material is used for the mechanical support and rigidity.
- **The micro bridge structure:** This type of structure consists of a suspended resistor beam. Typically, micro bridge is a simple but problematic structure. It is difficult to achieve longer/thinner structures due to lack of mechanical support resulting pirani gauges structures with limited dynamic range.

Up to now, a variety of pirani gauge structures have been developed in the literature using both membrane and microbridge structures. Table 2.3 presents some of the

pirani gauge structures with respect to the type, fabrication technology and measurement range.

Table 2.3: Some of the pirani gauge structures published in the literature.

Author/Year	Type of the gauge	Fabrication Technology	Measurement Range (Torr)
Mastrengelo and Muller/1991 [41]	Polysilicon microbridge	Surface Micromachining	$7.5x10^{-2}$-75
Shie *et. al.* /1995 [42]	Pt resistor on a dielectric membrane	Surface Micromachining	10^{-7}-1
Chou *et. al.* /1997 [43]	Pt resistor on a dielectric membrane	Surface Micromachining	10^{-1}-10^{2}
Stark *et. al.* /2003 [44]	Pt resistor on a dielectric membrane	Surface Micromachining	10^{-3}-1
Stark *et. al.* /2005 [45]	Polysilicon microbridge	Surface Micromachining	10^{-2}-100
Chae *et. al.* /2005 [46]	Silicon microbridge	Dissolved Wafer Process (DWP)	$2x10^{-2}$-2
Mitchell *et. al.* /2008 [47]	Polysilicon microbridge	Surface micromachining	$2x10^{-3}$-50
Topalli *et. al.* /2009 [48]	Silicon microbridge	Dissolved Wafer Process (DWP)	10^{-2}-2
Topalli *et. al.* /2009 [48]	Silicon microbridge	Silicon on Glass (SOG)	$5x10^{-2}$-5
Zhang *et. al.* /2009 [50]	Silicon microbridge	Dissolved Wafer Process (DWP)	$1.5x10^{-2}$-3
Li *et. al.* /2010 [49[51]	Silicon microbridge	Silicon-on-Insulator (SOI) Process	$8x10^{-2}$-200
Wang *et. al.* /2010 [52]	Pt resistor on a dielectric membrane	Surface micromachining	$7.5x10^{-3}$-2.25

2.4 Modeling Pirani Gauges

This section presents the effect of design parameters on the dynamic range and sensitivity of the pirani gauge structures. The dynamic range of a pirani gauge directly depends on the area of the resistor, heat sinks, and the gap between the resistor and heat sinks. The pirani gauge structure is modeled in MATLAB and the effect of each parameter is examined in detail.

Figure 2.9 presents a simple microbridge structure for a pirani gauge. The analytical model for this type of structures has been derived by Mastrengelo *et. al.* [41].

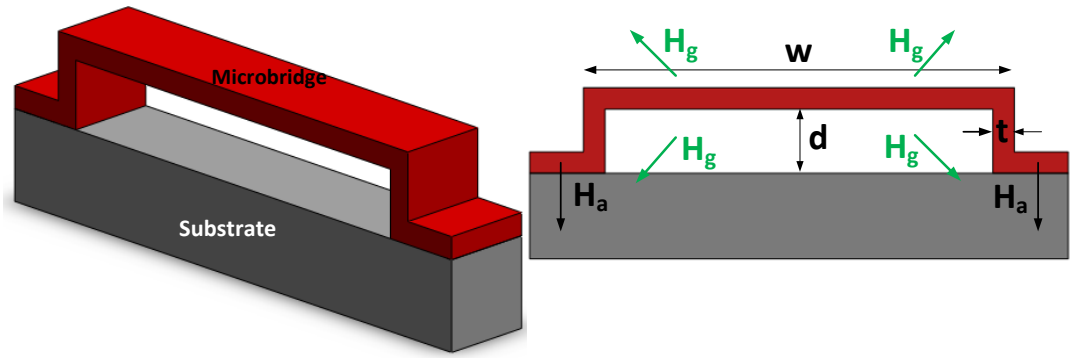


Figure 2.9: Microbridge structure of pirani gauge.

The Equation 2.8 presents the expression for the microbridge resistance R_b with a width of *w*, length of *l*, thickness of *t* and a gap of *d* between the resistor and heat sinks as a function of ambient pressure where δ is the ohmic power generation, ε is the heat loss through the gas, $I_b$is the current passed through the bridge, ξ is the TCR of bridge material, η is the correction factor, $K_{gas}(P)$ is the thermal conductivity through gas, and K_b is the thermal conductivity through the beam.

$$R_b = R_o\left[1+\frac{\delta\xi}{\varepsilon}\left(1-\frac{tanh\sqrt{\varepsilon}\frac{l}{2}}{\sqrt{\varepsilon}\frac{l}{2}}\right)\right] \qquad 2.8$$

$$\delta = \frac{{I_b}^2 R_o}{R_b wlt}, \qquad \varepsilon = \frac{\eta K_{gas}(P)}{K_b td} - \delta\xi \qquad 2.9$$

It is obvious from the Equations 2.8 and 2.9 that for a given current I_b, the temperature across the microbridge increases and as a result microbridge resistance

R_b changes. The average temperature change across the bridge is expressed in the Equation 2.10.

$$\Delta T = \left(\frac{R_b - R_0}{R_o}\right)\frac{1}{\xi} \qquad 2.10$$

The slope of average temperature change across the bridge versus the power dissipation on the resistor graph gives the thermal conductance. The thermal conductance is extracted for different pressure levels and thermal conductance versus pressure graph is obtained. This graph gives the dynamic range of sensor. The sensitivity of the pirani gauge can be extracted from the slope of this graph.

2.4.1 Length of the Resistor

The length of the microbridge resistor has a significant effect on the lower limit of the dynamic range. Since the effective surface area of the resistor increases with the longer resistor structures, the lower limit of dynamic range is extended. Figure 2.10 shows the effect of length on the dynamic range.

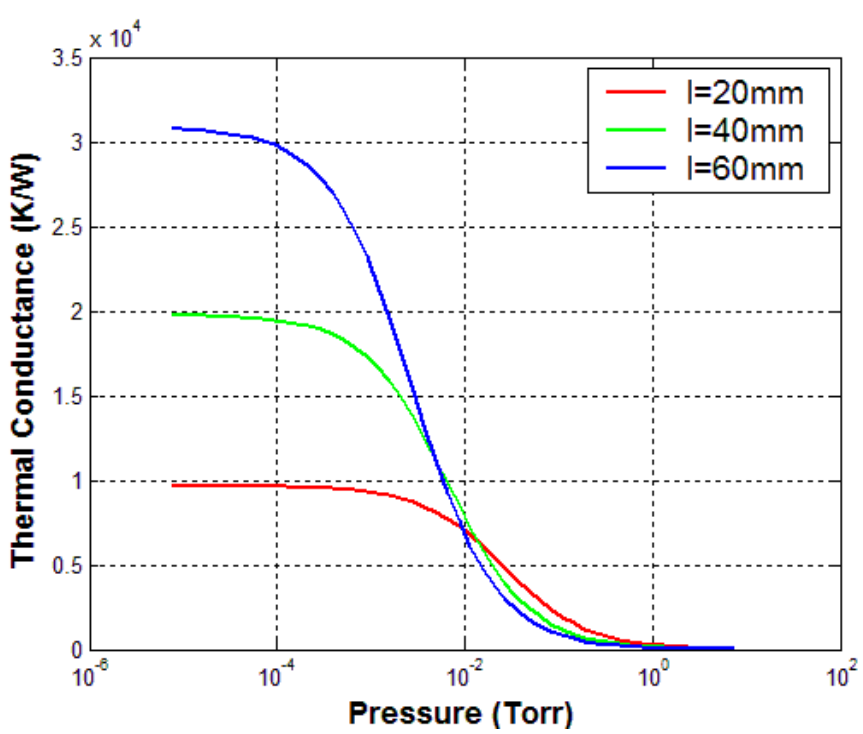


Figure 2.10: The effect of resistor length on the performance of a pirani gauge.

2.4.2 Width of the Resistor

Another critic parameter is the width of the resistor. Larger width resistor structures have higher contact area to the anchors. This increases the heat conduction through anchors and limits the lower measurement limits of the sensor. Figure 2.11 presents 3 different resistor structures with different resistor widths. As seen in the figure, a narrow resistor structure has the higher dynamic range.

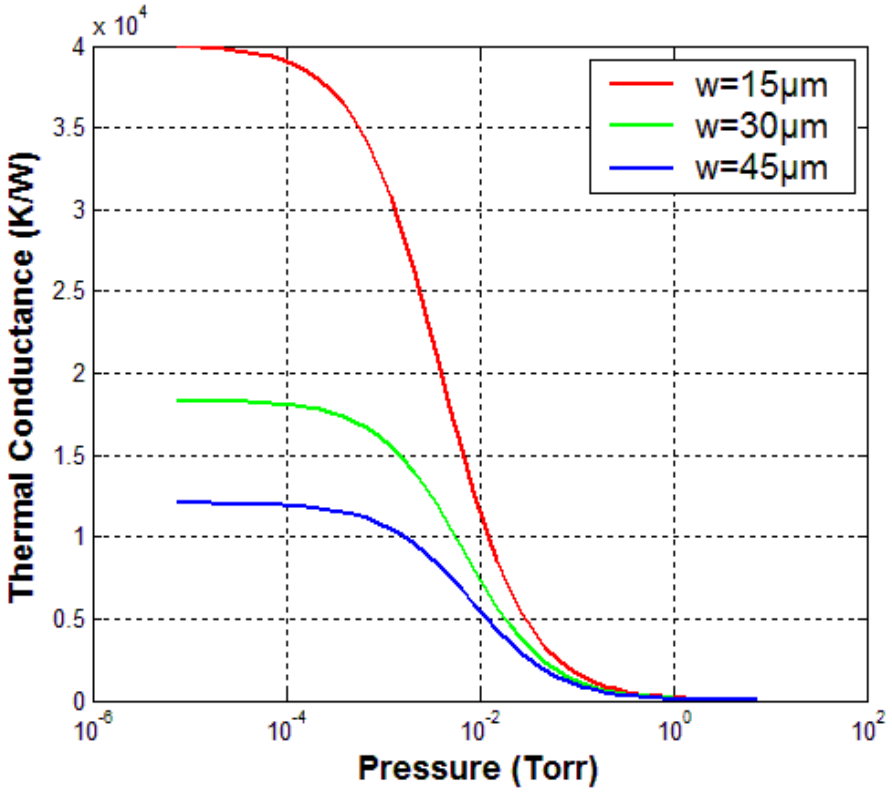


Figure 2.11: The effect of resistor width on the performance of a pirani gauge.

2.4.3 Thickness of the Resistor

The thickness of the resistor has also a significant effect on the lower limit of the dynamic range. Thicker resistor structures have larger contact area to the anchor regions and as a result increases the amount of heat conductance through the anchors. Thus, thicker resistor structures limit the minimum pressure level that a pirani gauge can measure. Figure 2.12 presents the effect of resistor thickness on the lower limit of the dynamic range.

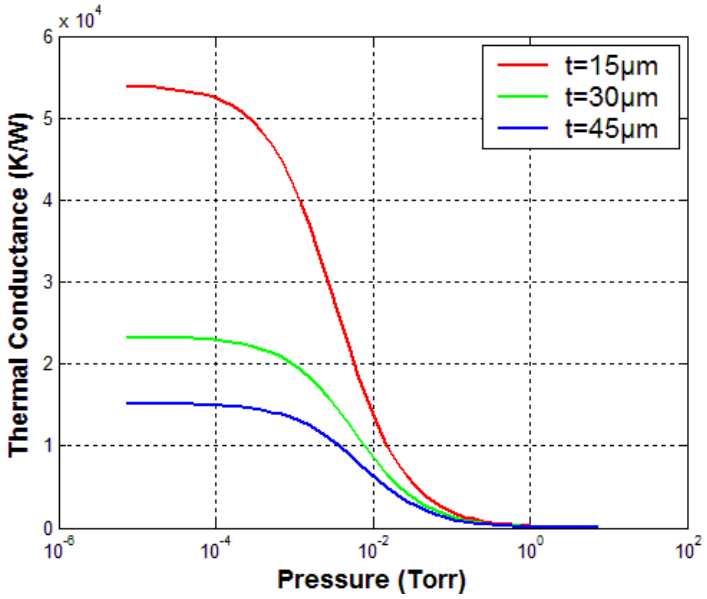


Figure 2.12: The effect of resistor thickness on the performance of a pirani gauge.

2.4.4 Gap between the Heat Sink and the Resistor

The upper limit of the dynamic range can be increased by reducing the gap between the resistor and heat sinks. At higher pressures, the mean free path of the gas molecules is smaller and the interaction between the gas atoms and the resistor can be increased by reducing the physical gap. Figure 2.13 shows the effect of gap on the upper limit of the dynamic range.

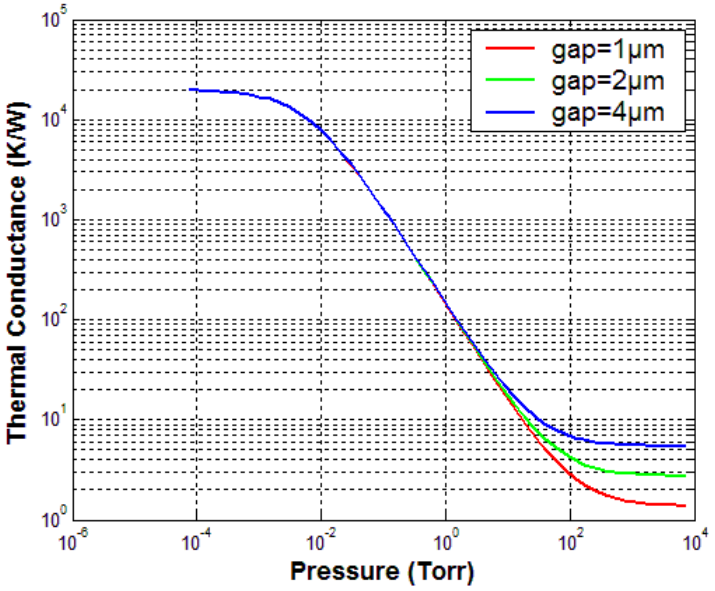


Figure 2.13: The effect of gap between the resistor and heat sinks on the performance of a pirani gauge.

2.4.5 Heat Sinks

Since the operation principle of the pirani gauge depends on the heat flux transfer from resistor to heat sinks, heat sinks play a significant role on the dynamic range. By increasing the area of the heat sinks, both gas conduction and effective resistance increases. Thus, a high sensitive and larger dynamic range pirani gauge is obtained. Detailed analysis on the heat sinks can be found in [46], [49], [51]. Figure 2.14 presents the effect of heat sinks on the performance.

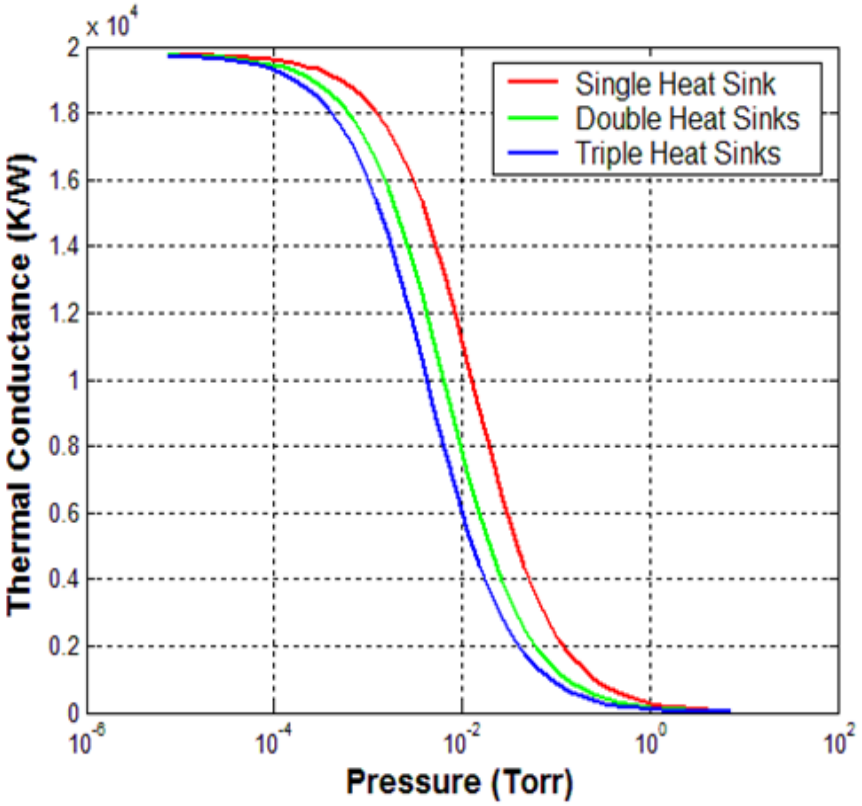


Figure 2.14: The effect of heat sinks on the pirani gauge performance.

2.5 Thermal Analysis of Pirani Gauge in Coventorware

Since pirani gauge is a thermal structure, it is important to analyze the temperature distribution along it. The thermal simulations are carried out in Coventorware. Figure 2.15 presents the temperature distribution along the resistor. The high temperature is observed at the middle of resistor and it decreases towards the regions where the resistor gets contact to anchor as expected.

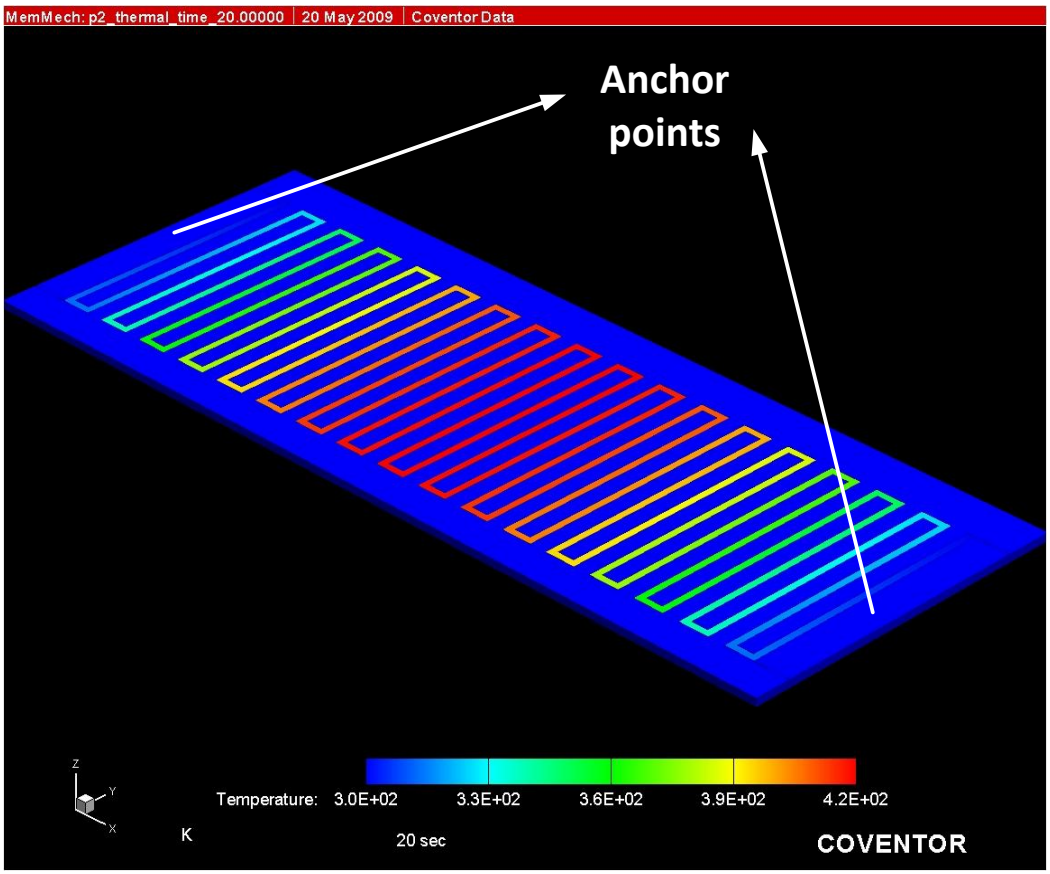


Figure 2.15: The temperature distribution on the resistor.

2.6 Previous Pirani Gauge Studies at METU

Two different pirani gauge structures based on the different fabrication technologies have been developed in METU. The first gauge was fabricated with a 14 µm thick p++ doped silicon micro bridge structure with dual heat sinks and a gap of 2 µm using Dissolved Wafer Process (DWP) and had a measured sensitivity of $4.2x10^4$(K/W)/Torr in the dynamic range of 0.01-2 Torr. However, this gauge had a buckling problem due to the stress in the highly doped thin structural layer as conventionally encountered in DWP. The second gauge was fabricated with a 100 µm p+ doped silicon layer with dual heat sinks and a gap of 3 µm using Silicon-On-Glass (SOG) technology. This gauge had a measured sensitivity of $3.8x10^3$(K/W)/Torr in the dynamic range of 0.05-5 Torr. The SOG pirani has been the most thick pirani gauge reported in the literature. Thus, it has a very high mechanical rigidity, but lower performance compared to the pirani gauges fabricated by DWP technology. Figure 2.16 presents the SEM pictures of both pirani gauge structures [48].

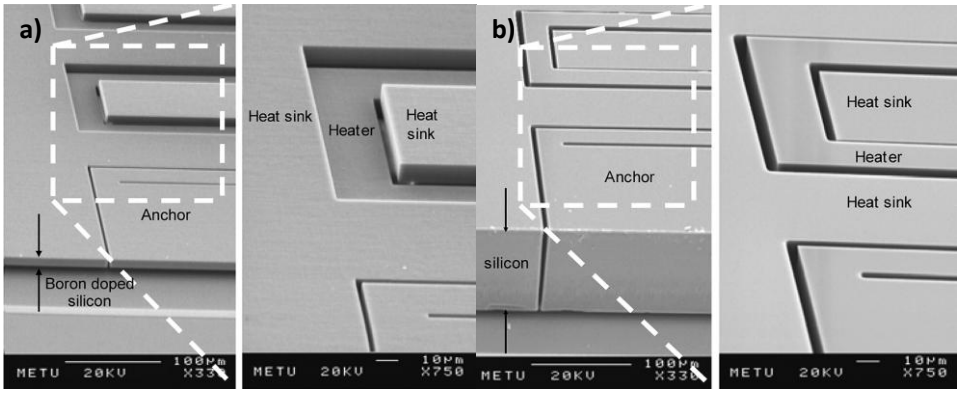


Figure 2.16: The previously developed pirani gauges at METU: (a) DWP pirani gauge, (b) SOG pirani gauge [48].

2.7 Pirani Gauges Developed in This Study

Previous pirani gauge studies in METU includes a 14 µm thick DWP and 100 µm thick SOG pirani gauges. However, these pirani gauges have some problems. While the DWP pirani gauge suffers from the internal stress due to highly doped structural layer, the SOG pirani gauge has lower sensitivity and dynamic range. In this study, three different pirani gauge structures with a meander shaped suspended silicon microbridge resistor and two isolated silicon heat sinks with a 35 µm device layer thickness and a gap of both 1 and 2 µm are developed to obtain optimum device performance. The pirani gauges are fabricated using a new SOG process based on the use of SOI wafer. The fabrication technique will be explained in detail in the Chapter 3. The designs are different from each other with respect to the physical dimensions of resistor structure. Table 2.4 and Figure 2.17 present the physical dimensions, material properties and estimated resistances of Designs-1, Design-2, and Design-3. Figure 2.18 presents the layout of Design-1.

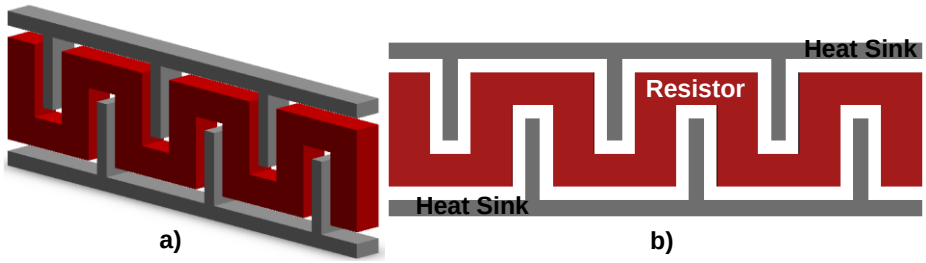


Figure 2.17: The meander shaped suspended microbridge resistor with dual heat sinks structure used in this study: (a) isometric view, (b) top view.

Table 2.4: The physical dimensions, material properties and estimated resistances of pirani gauge structures developed in this study.

		Design 1	**Design 2**	**Design 3**
Physical dimensions	*Width (w)*	20 µm	28 µm	14 µm
	Thickness (t)	35 µm	35 µm	35 µm
	Length (l)	40 mm	50 mm	40 mm
	Gap (d)	1 µm/2 µm	1 µm/2 µm	1 µm/2 µm
Material properties	*TCR*	1500 ppm/ºC	1500 ppm/ºC	1500 ppm/ºC
	Resistivity	$4x10^{-5}$ Ω.m	$4x10^{-5}$ Ω.m	$4x10^{-5}$ Ω.m
Estimated Resistance		2.29 kΩ	2.04 kΩ	3.27 kΩ

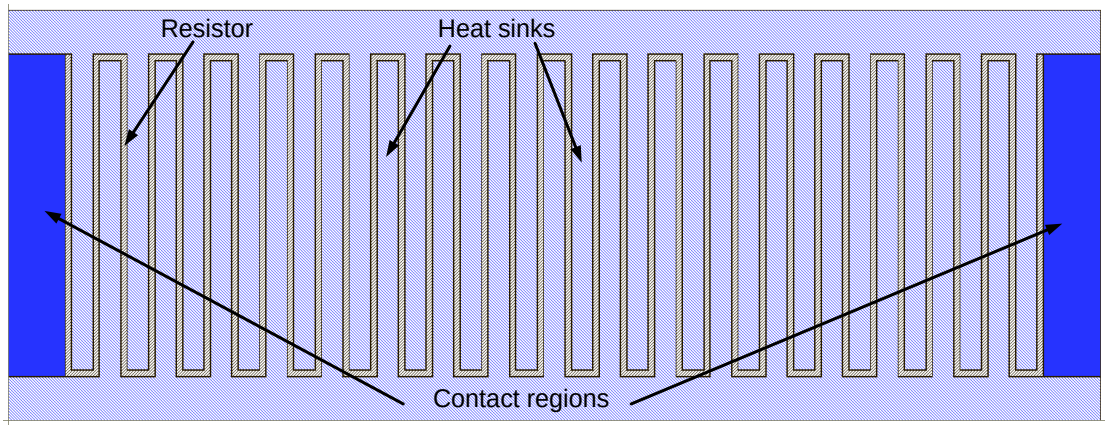


Figure 2.18: The layout of Design-1.

2.8 Summary of the Chapter

This chapter presents the design and modeling of micromachined resonators and pirani gauges. The chapter starts with the brief overview of resonating structures with respect to the review of mechanical and electrical parameters. Two different resonator designs based on the varying overlap area and varying gap configurations are presented. Furthermore, these resonator designs are verified by FEM simulations in Coventorware and the results are compared with the hand calculations. Similarly, the operation principle of MEMS pirani gauges is reviewed and the parameters that have an effect on the dynamic range of the structure are described by simulation

results. The chapter ends with the previous pirani gauge studies at METU and three new pirani gauge structures developed in the scope of this work.

CHAPTER 3

WAFER LEVEL PACKAGING USING Au-Si EUTECTIC and GLASS FRIT BONDING

This chapter first summarizes a detailed investigation of the Au-Si eutectic and glass frit bonding technologies. Then it explains the fabrication of MEMS gyroscopes, resonators and pirani vacuum gauges with lateral feedthroughs. Moreover, it describes a study on the fabrication of similar devices with vertical feedthroughs. Finally, it presents the wafer level vacuum packaging of the fabricated MEMS devices. The organization of this chapter is as follows;

Section 3.1 starts with a brief overview of Au-Si eutectic bonding and the previous works reported. Section 3.2 gives a summary of a series of bonding experiments done for the optimization of Au-Si bonds on both topographic and non-topographic surfaces. Section 3.3 describes the overview of glass frit bonding and followed by the previous works on glass frit bonding. Section 3.4 presents the experimental results of glass frit bonding optimization on different material surfaces. Section 3.5 explains the fabrication of devices with lateral feedthroughs, including the process flow, the problems encountered and the suggested solutions. Section 3.6 describes the studies on the fabrication of devices with vertical feedthroughs. Section 3.7 provides information about the design and fabrication of cap wafers for devices with lateral and vertical feedthroughs. Section 3.8 presents the wafer level vacuum packaging of the fabricated devices using both Au-Si eutectic and glass frit bonding. Finally, Section 3.9 gives a summary of this chapter.

3.1 Overview of Au-Si Eutectic Bonding

The way of mixing the materials at the desired atomic composition forms a eutectic system. This eutectic system involves a eutectic reaction in the case of heating the mixture above its eutectic temperature. The mixture becomes liquid above its eutectic temperature and upon cooling a solid eutectic alloy is formed. The main advantage of the eutectic system is that it has a melting point lower than the original materials. Several eutectic alloys can be used for the bonding of two wafers. Au-Si eutectic pair is one of most well known and practiced eutectic alloy used in the fabrication and wafer level packaging of MEMS devices. Figure 3.1 presents the phase diagram of the Au-Si eutectic system. As seen in the diagram, Au-Si eutectic reaction occurs at 363ºC for the mixture of %19 silicon in gold. In other words, although gold and silicon have melting points of 1063ºC and 1412ºC, the Au-Si mixture has a melting point of 363ºC [53].

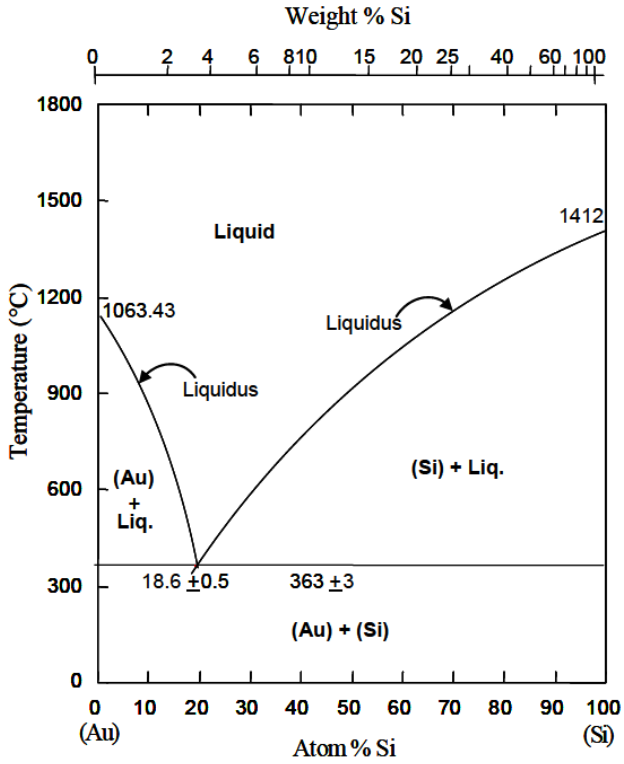


Figure 3.1: The phase diagram of Au-Si eutectic system [53].

There are two common ways to meet the gold and silicon for an atomic contact. A thin gold layer can be deposited onto the device wafer, on which a silicon cap wafer is aligned and pressed. In order to take a direct contact between silicon and gold layers, a short BHF dip should be done on the silicon cap wafer in order to remove

the native oxide on the silicon cap wafer before the bonding. Another way of meeting the gold and silicon is to deposit the correct amounts of thin gold on either the device or cap wafer and deposit either poly or amorphous silicon layers on the other substrate. Both methods can be applied, but in most cases using a silicon cap wafer simplifies the process.

Au-Si eutectic bonding offers excellent properties in the fabrication and wafer level packaging of microstructures. The Au-Si eutectic alloy becomes liquid when heated above its eutectic point and it can then cover the non-planar surfaces up to a topography step of 1µm. Thus, a high yield packaging process can be achieved even on the non-planar surfaces. These properties make the Au-Si eutectic bonding attractive for MEMS people in the packaging of wide range of devices. However, Au-Si alloy is conductive and can not be directly applied on the electrical connections laid over the MEMS device wafer. Therefore, a passivation layer is needed for electrical isolation. The need of the passivation layer increases the number of process masks and makes the process more complex.

3.1.1 Previous Works on Au-Si Eutectic Bonding

Since 90's Au-Si eutectic bonding has been a well known chip bonding technique used in the field of VLSI. In 1994, Wolffenbuttel *et. al.* presented Au-Si eutectic bond experiments at wafer level [27]. In these experiments, they tried to bond silicon wafers each with Ti/Au coated. As expected, Wolffenbuttel *et. al.* observed that a uniform Si diffusion into Au did not occur until the exact eutectic composition was reached. Moreover, Wolffenbuttel carried out a series of Au-Si eutectic bond experiments using again silicon wafers each coated with Ti/Au [54]. Strong bonds were observed only at 800ºC while they were non uniform at 500ºC and 600ºC. These temperatures were seriously higher than the eutectic temperature of Au-Si mixtures. It was proposed that titanium behaved as a diffusion barrier between the silicon and gold layers and prevented the silicon diffusion into the gold until the Si/Ti silicidation formed at 520ºC.

In 2003, Harpster *et. al.* obtained a significant improvement in the Au-Si bond quality by applying a voltage between glass and silicon wafers as done in standard anodic bonding [55]. They proposed that the electrostatic forces provided a higher intimate contact between wafer surfaces necessary to improve the bond quality.

Another work was reported by Chen *et. al.* in which the bond quality of Au and amorphous-Si layers was evaluated [58]. They proposed that eutectic reaction occurs much faster between Au and a-Si compared to the Au/c-Si eutectic partners. This rapid reaction prevents the formation of voids and craters faced during the eutectic bonding of Au and c-Si layers. Figure 3.2 presents the SEM images of bonded Au/c-Si and Au/a-Si pairs.

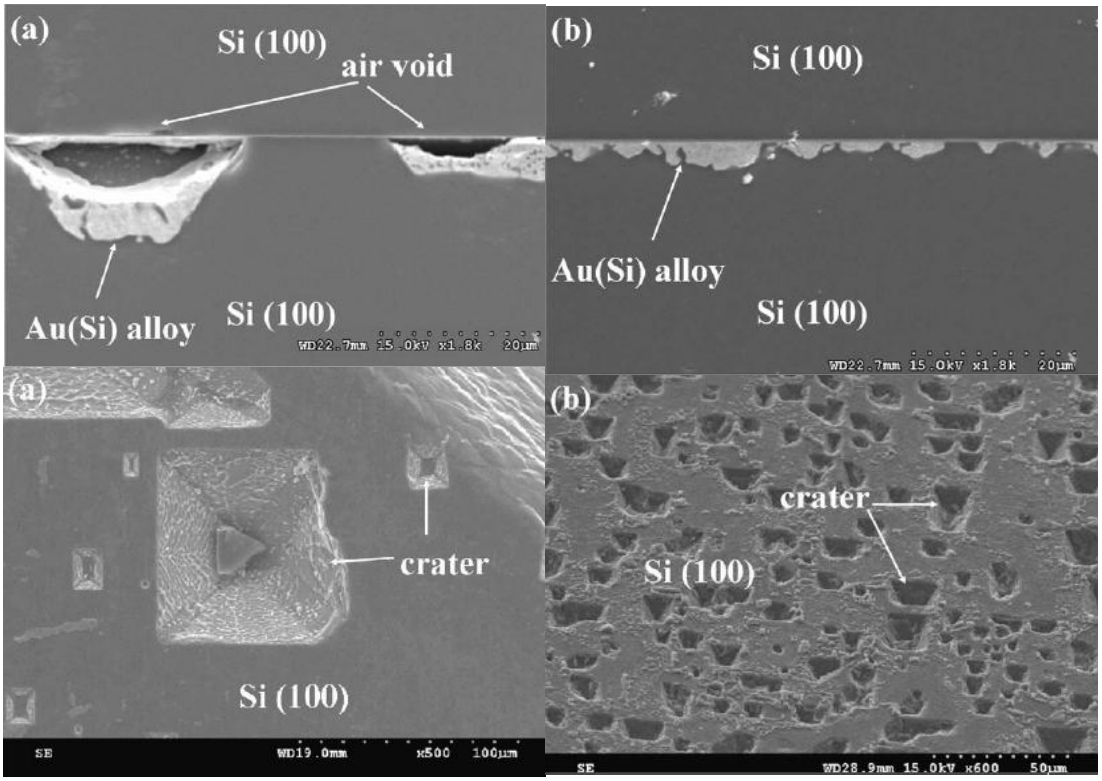


Figure 3.2: The SEM images of bonded wafers: (a) Au/crystal Si eutectic bonds. (b) Au/amorphous Si eutectic bonds [58].

Similarly, Lin *et. al.* compared the quality of the c-Si and a-Si bonded to different dimensions of Au layers. Moreover, the effect of material compositions, bonding parameters and surface pre-treatments on the bonding quality were discussed in this work [60].

One of the other relevant works was presented by Mitchell *et. al.* They carried out series of wafer level packaging experiments using eutectic partners of poly-Si/Au, doped poly-Si/Au and Au/Au. They reported the experimental results of the vacuum packages fabricated by Au-Si eutectic bonding in respect to yield and reliability in [37], [56], [57], [59].

3.2 Optimization of Au-Si Eutectic Bonding

This section presents the experimental results of Au-Si eutectic bonding trials on both non-topographic and topographic surfaces. Before giving the experimental results, the bond recipe and the method used for the evaluation of the bonding quality will be described.

3.2.1 The Bond Recipe

As presented in the previous sections, the eutectic point of Au-Si mixture at a silicon composition of %18.5 in gold is 363ºC. However, a bonding temperature of 363ºC to achieve high quality Au-Si bond is not sufficient in many applications and it has to be increased. In this study, bond temperatures in the range of 390ºC to 420ºC are used depending on the quality of the surface topography.

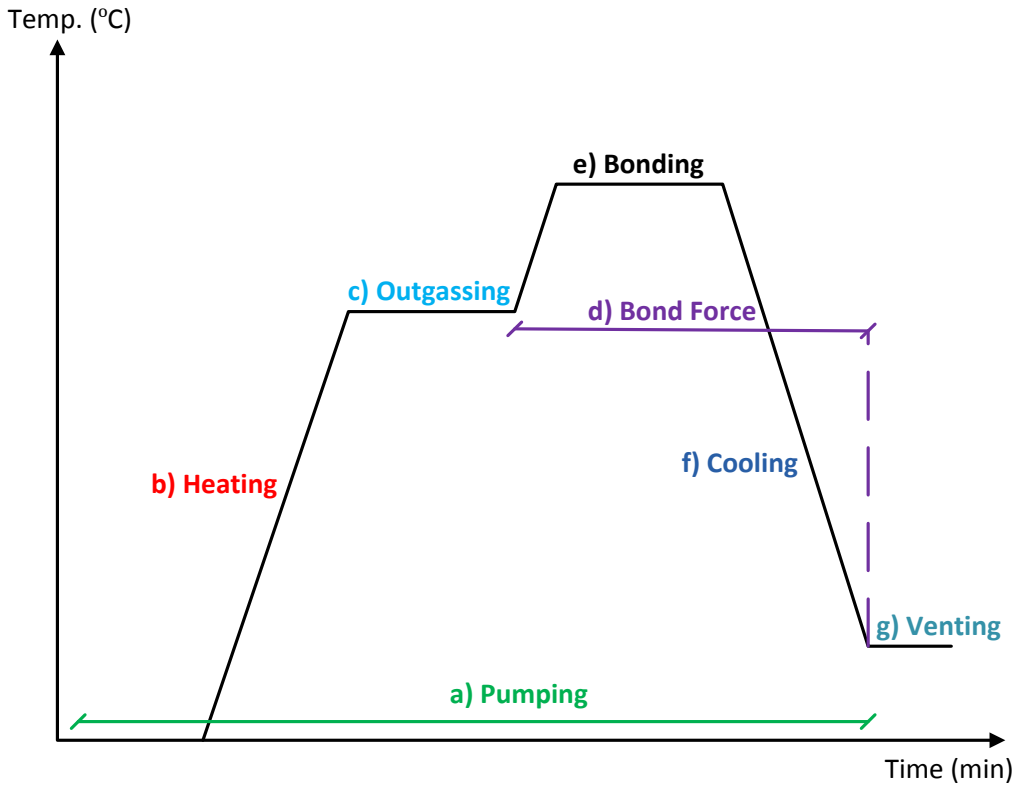


Figure 3.3: The generic bond recipe for Au-Si eutectic bonding.

Figure 3.3 illustrates a conceptual bond recipe for Au-Si eutectic bonding. This recipe includes seven main steps: a) pumping, b) heating, c) outgassing, d) application of bond force, (e) actual bonding, (f) cooling and (g) venting. These steps and their effects on the bonding quality are explained at the following below;

(a) **Pumping:** After the alignment procedures of the wafers to be bonded are completed, they are placed inside the wafer bonder. The chamber of wafer bonder is continuously pumped from the start of the process until the wafers are cooled down to room temperature and the bonding process is completed. This step plays a critic role on the quality of vacuum inside the package because the sealing is carried out at a pressure equal to the pressure of wafer bonder chamber. Thus, a longer pumping period is needed to achieve higher vacuum levels before the actual bonding starts.

(b) **Heating:** This step includes the heating of the wafer pairs up to the set temperature value.

(c) **Outgassing:** This step is the outgassing of the materials used in the fabrication prior to the bonding. Since a MEMS package has smaller dimensions, outgassing becomes the most dominant factor in the performance loss. Therefore, wafers are subjected to an outgassing step at temperatures below than the eutectic temperature of Au-Si eutectic partners, typically at 300-350ºC, for a predetermined period of time.

(d) **Application of bond force:** The bond force is applied directly after the end of outgassing step and kept on the wafers to the end of cooling step. This step has a significant role on the quality of Au-Si bond. The wafers have to be into a good contact for the diffusion process to take place and to cover step heights. However, the higher bond forces result in excessive eutectic flows on the device and cap wafers. In this study, bond forces between 1500N-3500N are used for the Au-Si eutectic bonding.

(e) **Bonding:** Although the eutectic point of gold-silicon pair is 363ºC, it is difficult to obtain a high quality bonding at 363ºC. Thus higher temperatures are needed. In this study, bond temperatures between 390-420 ºC are used depending on the surface quality. The holding time at bond temperature is also important and depends on the topography of surface. Higher surface quality, lower the temperature and holding time.

(f) **Cooling:** This step includes the cooling of the wafers down to the room temperature. The liquid Au-Si eutectic mixture solidifies during cooling and a strong bond is obtained. The cooling period becomes much significant in the case of having an Au-Si eutectic pair between the device metallization

and the structural layer. Gold feedthroughs can be damaged due to a fast cooling period. This situation will be explained in the Section 3.8.2.

(g) **Venting:** The final step is venting the chamber of the wafer bonder. After the venting, the bond process is completed.

3.2.2 Evaluation of the Bond Quality

In the literature, several methods including razor blade and shear test [59], IR inspection [61] and SEM are used to analyze the Au-Si eutectic bond quality. The method used to evaluate the uniformity and quality of Au-Si bond in this work is the deflection test. The principle behind this test is the deflection of a thinned diagram due to the pressure difference between the inside and outside of the package. Figure 3.4 illustrates the principle of the deflection test used for the evaluation of the bond quality.

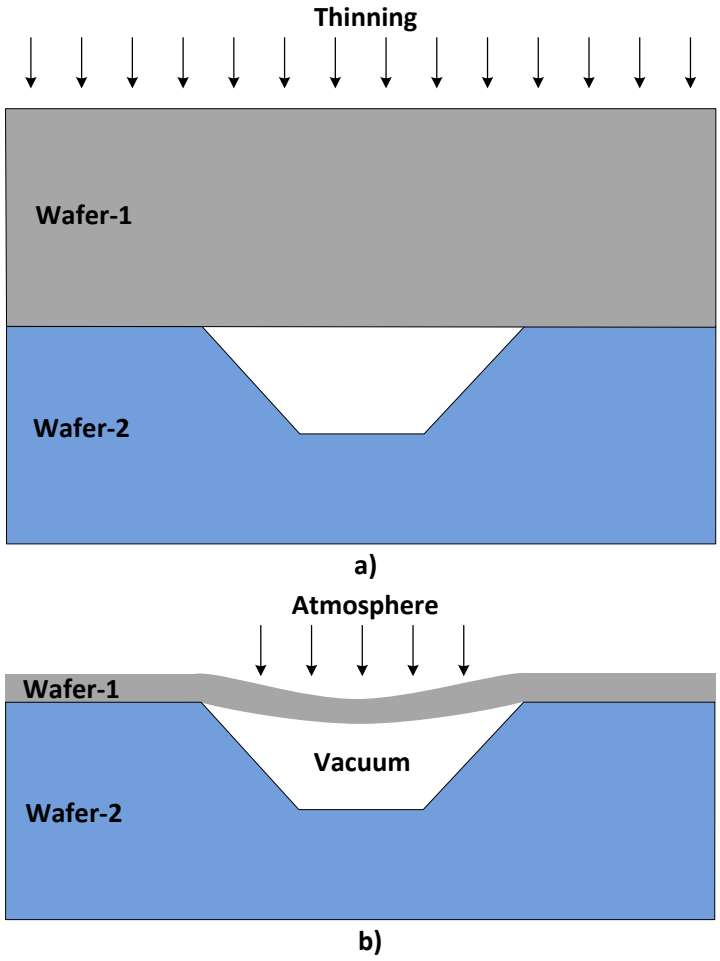


Figure 3.4: The principle of deflection test used for the evaluation of the bond quality: (a) before thinning, (b) after thinning.

After the actual bonding, the backside of the silicon cap wafer is thinned up to a known thickness that it can deflect or not with respect to the pressure level inside the cavity. The thinning process of the silicon cap wafer is carried out using the STS DRIE tool. In the case of having low pressures inside the package, showing that the bond quality is higher, the thinned silicon cap wafer deflects downwards due to the pressure difference. If the bonding quality is weaker, the wafers are broken during the thinning process inside the DRIE chamber due to weak bond forces.

Deflection test is a useful, but a destructive test method, in which the bonded wafers could not be used anymore after the test. If the thickness and properties of the packaging material are exactly known, the pressure inside the package can be easily calculated after measuring the amount of deflection. Thus, not only the hermeticity of the package is tested but also information about the vacuum level can be provided using this method. However, the residual stress of the packaging material may cause inaccuracy in the measurement results.

3.2.3 Results

This section presents the optimization results of Au-Si eutectic bonding. The optimization is carried out on both planar and non-planar surfaces. The details are presented below.

3.2.3.1 Bonding on Planar Surfaces

The bond experiments are carried out between the glass and silicon wafers. The glass wafer is used as a cap wafer and bonded to a dummy silicon wafer. The fabrication of glass cap wafer includes one mask. Since the cavities are formed in HF, the masking material has to be Cr/Au. This masking Cr/Au layer can be also used for Au-Si bond ring and there is no need to repeat the deposition. After depositing Cr/Au on a glass wafer by sputtering or thermal evaporation, the Cr/Au layer is patterned using cap wafer mask and etched in Cr/Au etchants. The wafer is then subjected to pure HF etch until a depth of 50 µm is obtained. A series of cleaning procedures is applied on the glass wafer for PR strip and pre-bonding cleaning. Similarly, blank silicon wafer is subjected to the same pre-bonding cleaning and followed by a short BHF dip to remove the native oxide on it. The bonding recipe described in the previous sections is used by only changing the peak temperature. Table 3.1 presents the experimental results of the bonding trials on the

planar surfaces. It should be noted that the bond quality is evaluated using the deflection test presented above and it is supported by the optical and electron microscope observations. Figure 3.5 and Figure 3.6 present the view of bond #4 after the deflection test and SEM pictures, respectively and Figure 3.7 shows the higher eutectic flow occurred in the bond #6

Table 3.1: Experimental results of Au-Si eutectic bonds on planar surfaces.

Bond #	Cap wafer	Device Wafer	Bond Ring Thickness	Bond Temp.	Bond Force	Bond quality
1	Glass	Blank Si	150 nm Sputtered Gold	390 °C 60 min	1500 N	Vacuum
2	Glass	Blank Si	150 nm Evaporated Cr/Au	390 °C 60 min	1500 N	Vacuum
3	Glass	Blank Si	300 nm Sputtered Gold	390 °C 60 min	1500 N	Vacuum
4	Glass	Blank Si	1 µm Sputtered Gold	390 °C 60 min	1500 N	Vacuum, thicker eutectic alloy
5	Glass	Blank Si	1.5 µm Sputtered Gold	390 °C 60 min	1500 N	Vacuum, thicker eutectic alloy
6	Glass	Blank Si	1.5 µm Sputtered Gold	390 °C 60 min	3500 N	Vacuum, higher eutectic flow
7	Glass	Blank Si	1.5 µm Sputtered Gold	400 °C 60 min	1500 N	Vacuum, higher eutectic flow
8	Glass	Blank Si	1.5 µm Sputtered Gold	420 °C 60 min	1500 N	Vacuum, higher eutectic flow

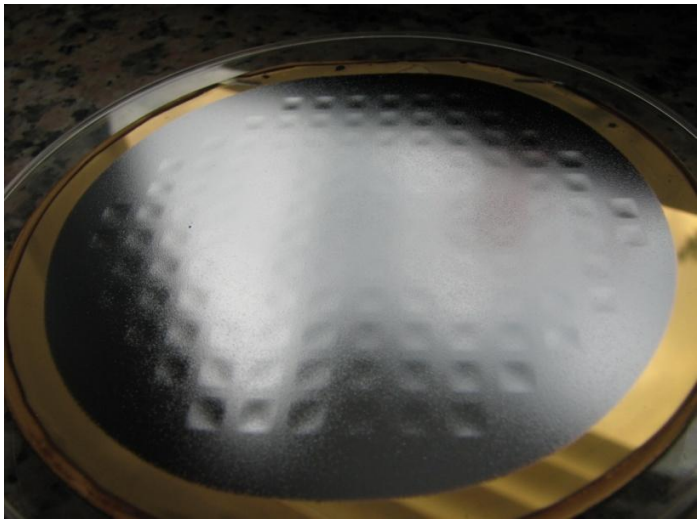


Figure 3.5: The view of bond#4 after the deflection test. The thinned silicon layers deflected to downwards due to the vacuum inside the cavities.

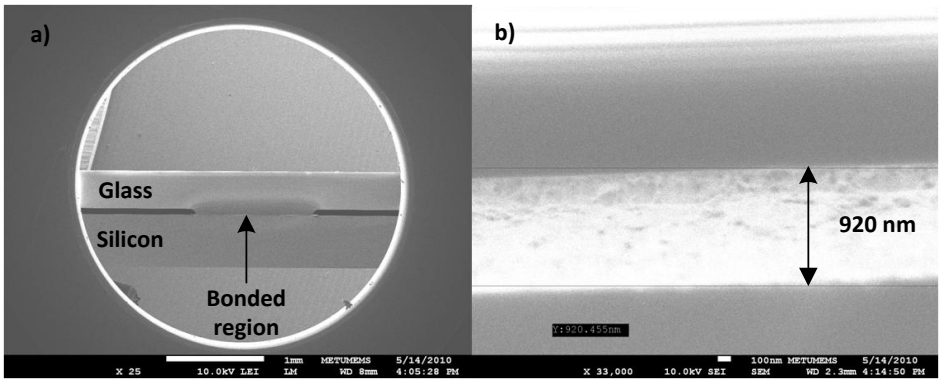


Figure 3.6: SEM pictures of bond#4: (a) the cross sectional view of eutectically bonded glass-silicon wafers, (b) the view of bonding interface.

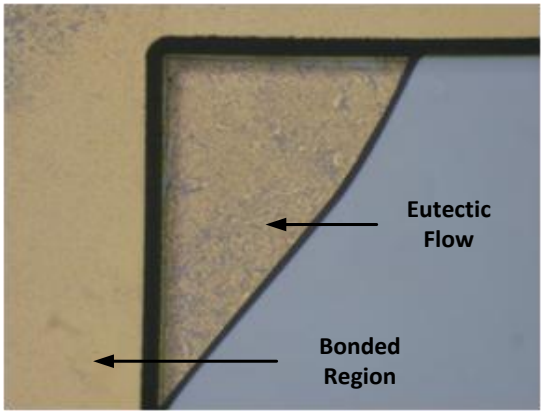


Figure 3.7: An optical microscope picture from bond#6. Higher bond forces resulted in eutectic flow on device area.

The optimization of Au-Si bonds on planar surfaces can be summarized as follows;

- A strong Au-Si bond is obtained at temperatures in the range of 390-420ºC. In the case of increasing the bonding temperature, high amount of lateral eutectic flow on the device area is observed. This is critical since the Au-Si eutectic mixture is conductive and cause short circuit if reaches to the MEMS devices in the sealed cavity. The holding time at bond temperature is the other critical parameter. In this study, all bonding trial has a hold time of 60 min and shorter hold times are not tested.
- The bond force is the other critical parameter for the Au-Si eutectic bonding. For the Au-Si diffusion to occur, wafers have to be in a good contact. On the other hand, higher bond forces cause higher eutectic flow. Therefore, the bond force has to be optimized.
- Since silicon is provided by the 500 µm thick substrate, the thin film gold thickness determines the final thickness of Au-Si eutectic alloy. Thinner gold provides thinner Au-Si eutectic alloy. In this study, different thicknesses of gold are tested and strong bonds are achieved even with 150 nm gold.
- It is relatively easy to apply Au-Si eutectic bonding on planar surfaces without any process flow or design variations. In this study, a high yield Au-Si eutectic bond is obtained at 390ºC with a bond force of 1500N on planar surfaces.

3.2.3.2 Bonding on Non-Planar Surfaces

It is difficult to achieve strong bonds on a surface where lateral feedthroughs exist. A strong bond can only be obtained in the case that the eutectic mixture perfectly covers the topographic surface. In addition to this, Au-Si eutectic alloy can not be directly applied on the electrical connections, otherwise electrically shorting them. These facts require a careful design of process flow and make the process more complex in respect to the number of process masks.

In this study, the bond experiments on non planar surfaces are carried out between the glass and silicon wafers. The silicon wafer is now used as a cap wafer. The fabrication of this silicon cap wafer includes one mask. It is patterned using cap wafer mask and then etched using DRIE until reaching to the desired cavity depth. The silicon wafer is subjected to a series of pre-bonding cleaning steps and followed

by a short BHF dip before the eutectic bonding. The glass wafer is used as a device substrate and thus it has to be fabricated similar to the device wafer. The processes in the order of anchor formation, creating the 0.3 µm thick device metallization, passivation and eutectic bond ring formation are carried out. Details of these process steps will be presented in the Section 3.5. Similar to the silicon cap wafer, glass wafer is subjected to a cleaning step before the bonding. A series of bonding experiments is carried out using these wafers. This section gives the experimental Au-Si bond results on lateral feedthroughs that have topography of 0.15 µm. Table 3.2 presents the experimental results of the bonding trials on the planar surfaces. The bond quality is evaluated using the deflection test and it is supported by the optical microscope observations.

Experimental results show that a strong Au-Si eutectic bond on lateral feedthroughs could only be obtained at 420ºC. Since Au-Si eutectic mixture become more liquidous at higher temperatures, the planarization of topographic surface can be achieved. A 1.5 µm gold layer is used and lower thicknesses are not tested at 420ºC. Figure 3.8 presents the deflection test results of bond#1 and bond#5.

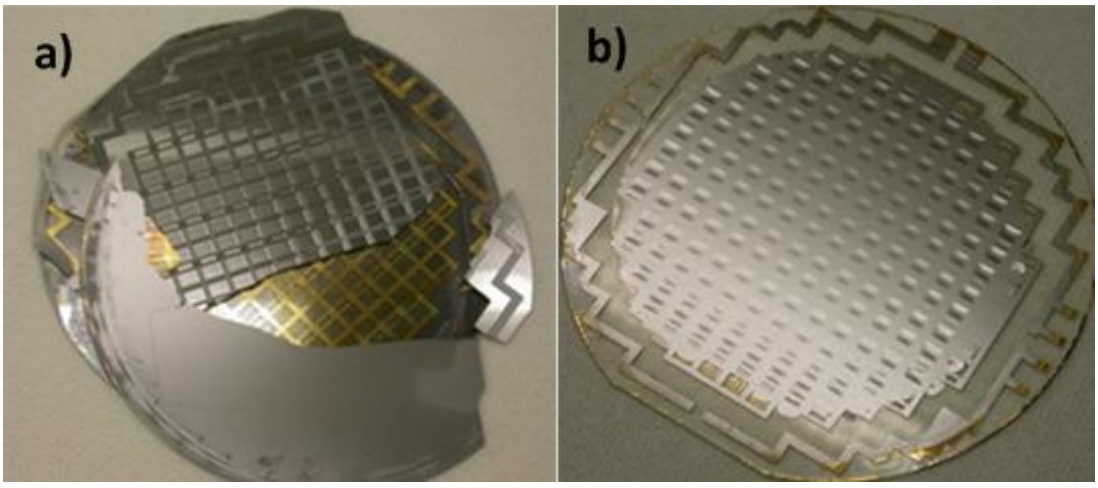


Figure 3.8: The view of bonded wafer pairs after the bond quality test: (a) bond#1. The cap easily separated from the device wafer, (b) bond#5. The cavities are deflected to downwards, which proves the vacuum.

Table 3.2: Experimental results of Au-Si eutectic bonds on non-planar surfaces.

Bond #	Cap wafer	Device Wafer	Bond Ring Thickness	Bond Temp. and Force	Voltage	Bond quality
1	Si	Glass wafer with feedthroughs	300 nm Sputtered Gold	390 °C 60 min 1500 N	No	Very weak bond
2	Si	Glass wafer with feedthroughs	1.5 µm Sputtered Gold	390 °C 60 min 1500 N	No	Very weak bond
3	Si	Glass wafer with feedthroughs	1.5 µm Sputtered Gold	390 °C 60 min 3500 N	No	Very weak bond
4	Si	Glass wafer with feedthroughs	1.5 µm Sputtered Gold	390 °C 60 min 1500 N	Yes	Very weak bond
5	Si	Glass wafer with feedthroughs	1.5 µm Sputtered Gold	420 °C 60 min 1500 N	No	Vacuum
6	Si	Glass wafer with feedthroughs	1.5 µm Sputtered Gold	420 °C 60 min 3500 N	No	Vacuum, higher eutectic flow
7	Si	Glass wafer with feedthroughs	1.5 µm Sputtered Gold	420 °C 60 min 1500 N	Yes	Vacuum, higher eutectic flow

3.3 Overview of Glass Frit Bonding

The glass frit bonding is one of the commonly used technologies for the wafer level vacuum packaging of MEMS devices. It is a well developed technology and a large amount of MEMS products in the market is encapsulated using this technique. The glass frit bonding includes three main steps; a) deposition of glass frit, b) thermal conditioning, and c) bonding.

a) **Deposition of glass frit:** This step includes the deposition of glass frit material by screen printing. Screen printing is a thick film technology used for the deposition materials. Since it is used for the deposition of thick films, the minimum feature size of deposited glass frit is limited up to a width of 190 µm with a minimum spacing of 100 µm. The height of the printed frit is 30µm and after the bonding, it becomes 10 µm.

b) **Thermal conditioning:** The step contains the thermal conditioning of the glass frit material. The organic solvents inside the glass frit should be removed by a thermal treatment where the glass frit does not completely melt. Besides, the properties of glass frit material are fixed and it transforms into a real glass during this conditioning step. This step has a significant effect on the quality on bonding process. In the case of a poor thermal conditioning, voids can be observed inside the glass frit which limits the reliability of the packaging process.

c) **Bonding:** The last step is the bonding. In this step, wafers are heated to a temperature under an applied mechanical pressure where glass frit fully melts, covers the surface of the wafers and forms a hermetic bond upon cooling. A bond temperature of 435-450ºC and a force of 1500-3500N are used for a typical glass frit bond.

Wide range of materials can be bonded using glass frit bonding without any process and design variations because glass frit is nonconductive and can be directly applied on the electrical connections. The glass frit material is superior in planarizing the topographic surfaces up to 2 µm which is essential for the wafer level packaging process. Moreover, it has high bond strength and excellent mechanical properties [65]. The mechanical stress is minimized by adapting the thermal expansion coefficient of glass frit material to the silicon.

The main drawback of the glass frit bonding is the high process temperature. In the case of using gold device metallization for silicon structural layers, high bond temperature exceeds the eutectic point of Au-Si pair and causes degradation in the device metallization. However, this effect can be minimized by controlling the holding time at the bond temperature. In addition to these, the flow of glass frit material on the device region may cause a problem and has to be considered.

Another problem is the limitation of minimum bonding line due to the screen printing process. This limitation increases the package size.

3.3.1 Previous Works on Glass Frit Bonding

Glass frit bonding has been used for bonding wide range of material combinations for a long time in various MEMS applications. This section presents some of the previous glass frit bonding studies in the literature.

In 2000, H. Song *et. al.* demonstrated a wafer level vacuum packaging process using glass frit bonding. They encapsulated MEMS gyroscopes and measured the pressure levels inside the package 150mTorr without using getters [29].

In 2003, D. Sparks *et. al.* developed a chip level vacuum packaging process using glass frit bonding. They used resonators for the vacuum characterization and observed a pressure of 850 µTorr inside the package with the help of Nanogetters™. Figure 3.9 presents MEMS packages fabricated in [62].

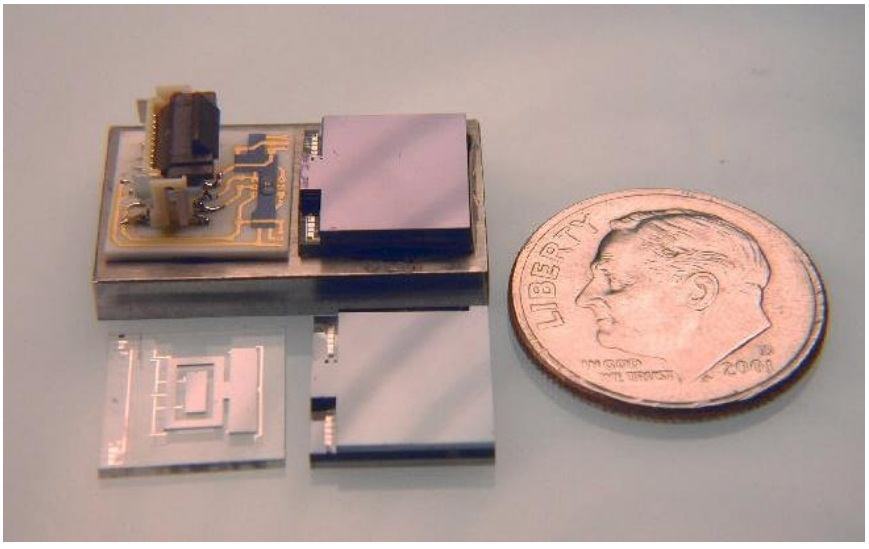


Figure 3.9: Chip level packages developed in [62].

Similarly, D. Sparks *et. al.* published glass frit bonding studies in 2004 and 2005 in which they detected high vacuum levels inside the packages by the deflection test and integrated resonators. Furthermore, they subjected these packages to a series of bake tests to estimate the package performance throughout the life time in [34], [63]. Figure 3.10 presents the view of dimpled packages which proves the vacuum inside the sealed cavities.

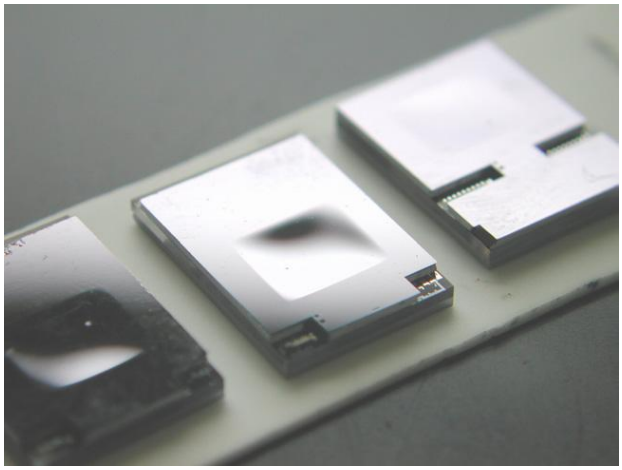


Figure 3.10: Packages subjected to the deflection test for the evaluation of vacuum quality [34].

In 2005 and 2006, R. Knetchel *et. al.* reported studies on glass frit bonding and its application to the wafer level vacuum packaging. They presented detailed information on the characterization of glass frit bonding for the wafer level vacuum packaging [28], [64]. In the same year, C. Dresbach *et. al.* published a work on the mechanical properties of micro packages encapsulated by glass frit bonding. This work includes studies on the methods for testing the bonding quality and numerical stress calculations [65]. In 2008, P. Hothur demonstrated a study on the packaging of biosensors using glass frit technique [66].

3.4 Optimization of Glass Frit Bonding

This section presents the experimental results of glass frit bonding trials on non-topographic and topographic surfaces. Before giving the experimental results, the bond recipe and the method used for the evaluation of the bonding quality are described.

3.4.1 The Bond Recipe

The bond recipe of the glass frit bonding is similar to the Au-Si eutectic bonding recipe, except one step. As described in the previous sections, a thermal conditioning is needed for the glass frit bonding. This is an essential step which determines the quality of the bonding. In this step, the organic solvents inside the glass frit material have to be burned out and transformed into a real glass before the bonding. Thus, glass frit bonding recipe includes an additional step, thermal

conditioning, between the pumping and outgassing steps. In the case of performing the outgassing step at 300ºC, these two steps can be combined and carried out as single step.

3.4.2 Evaluation of the Bond Quality

The razor blade, shear and deflection tests, SEM, optical and infrared microscopes are the common methods for the evaluation of glass frit bond quality. The quality of glass frit bond on glass wafers can be examined by optical microscope, while the silicon to silicon bonds need to use other type of tests. In this study, the bond quality on glass wafers is evaluated using optical microscope. Figure 3.11 presents optical microscope photos from dies having successful and unsuccessful bond qualities. If the bond is successful, the glass frit ring is completely black in color without any voids. On the other hand, if the bond is unsuccessful, voids can be observed at the bonding line.

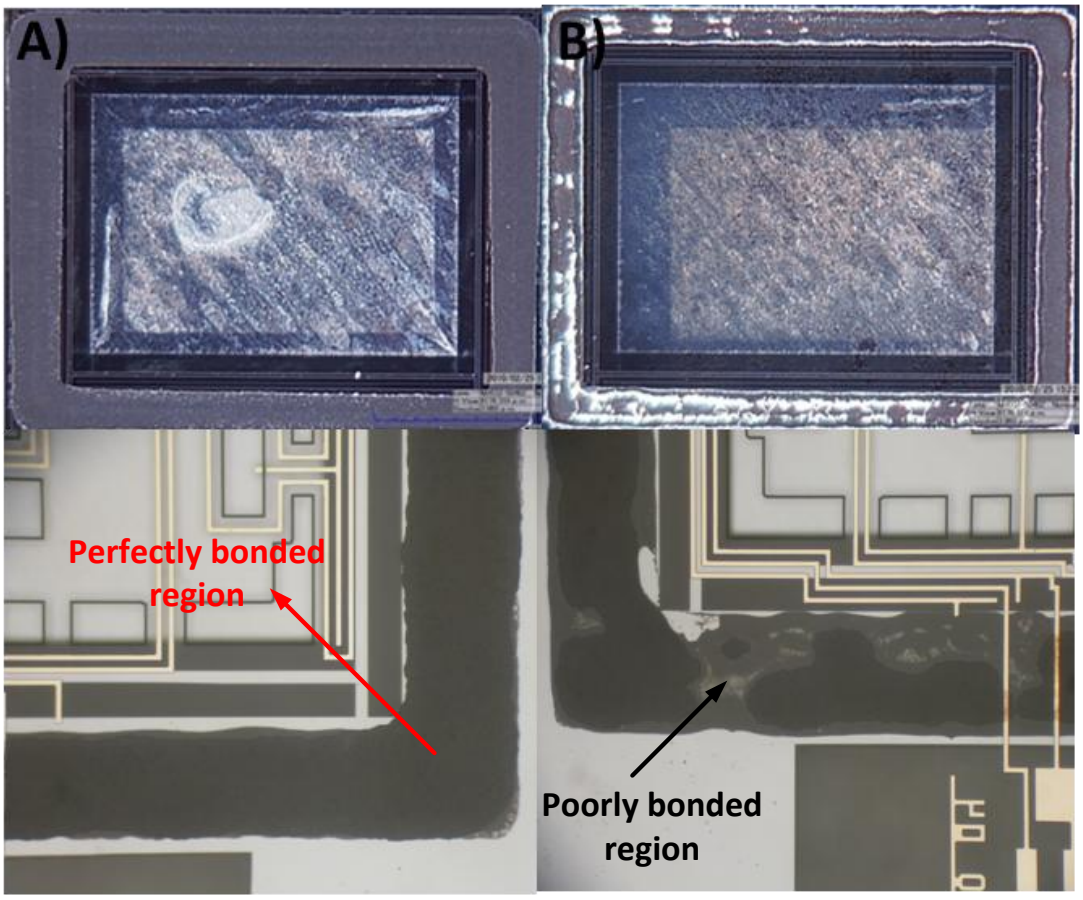


Figure 3.11: The evaluation of bond quality by optical microscope: (a) successful bonding, (b) unsuccessful bonding.

3.4.3 Results

This section presents the optimization results of glass frit bonding. The optimization is carried out for both non-planar surfaces and on the different types of surfaces. The details are provided below.

3.4.3.1 Bonding on Glass Wafers

The bond experiments are carried out between glass and silicon wafers. The silicon cap wafer is bonded on glass wafers with gold feedthroughs. The fabrication of silicon cap wafers used in these trials will be described in detail in the Section 3.7.1. The gold feedthroughs are formed on glass wafer after a number of processes similar to the ones in Section 3.2.3.2 except passivation and eutectic bonding ring formation. Table 3.3 and Figure 3.12 present the experimental results of the glass frit bonding optimization with respect to bond yield.

Table 3.3: Experimental results of glass frit bonds on glass wafer with lateral feedthroughs.

Bond #	Cap Wafer	Device Wafer	Bond Temp. and Hold Time	Bond Force	Bond yield
1	Silicon	Glass wafer with lateral feedthroughs	435ºC 10 min	1500 N	% 31.25
2	Silicon	Glass wafer with lateral feedthroughs	450ºC 10 min	1500 N	% 53.9
3	Silicon	Glass wafer with lateral feedthroughs	435ºC 60 min	1500 N	%77.2
4	Silicon	Glass wafer with lateral feedthroughs	435ºC 60 min	3500 N	% 85.8
5	Silicon	Glass wafer with lateral feedthroughs	450ºC 60 min	1500 N	% 99.4

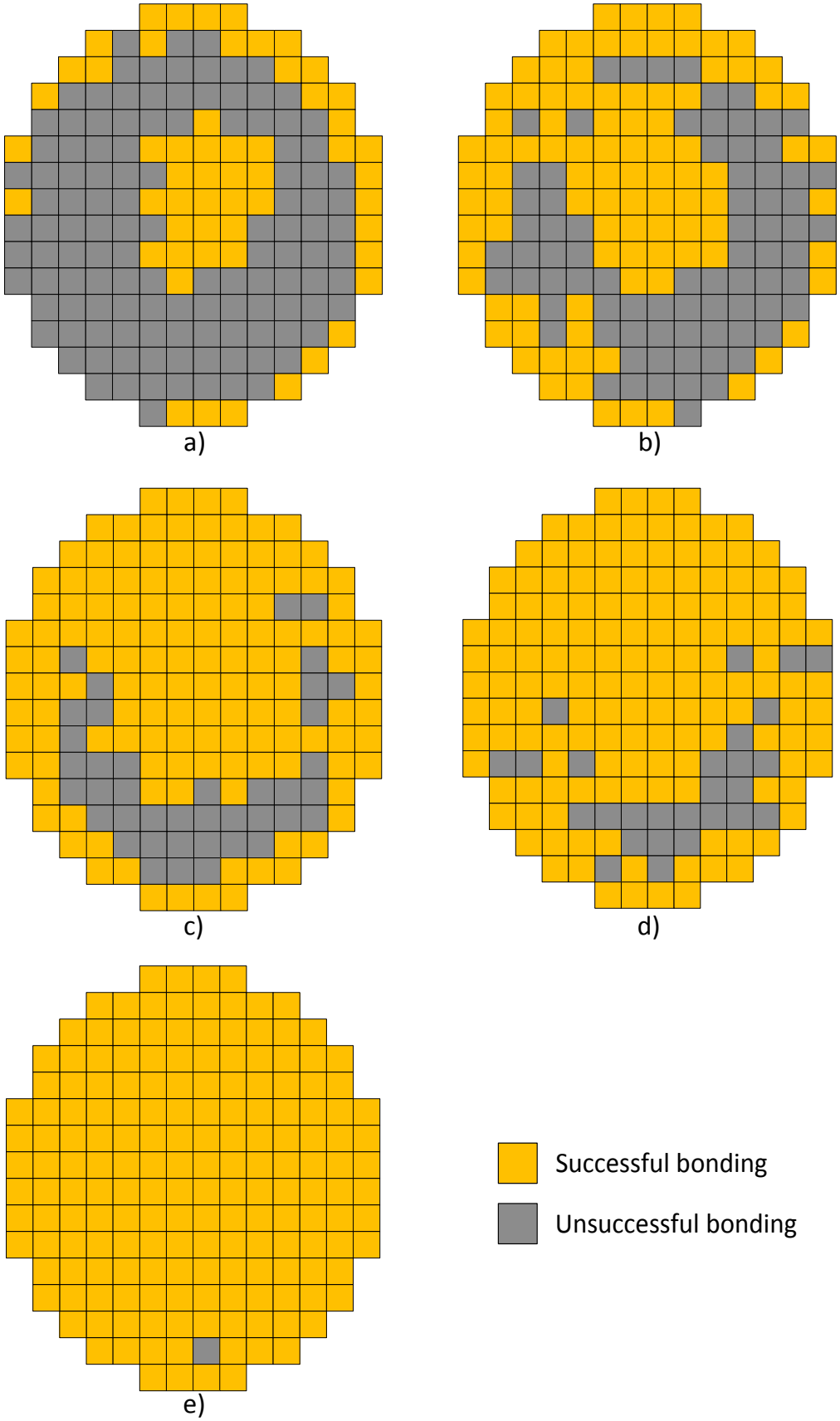


Figure 3.12: The uniformity results of glass frit bonds on glass wafer with lateral feedthroughs: (a) bond#1, (b) bond#2, (c) bond#3, (d) bond#4, and (e) bond#5.

The main problem faced during the optimization of glass frit bonding process is the degradation of the gold feedthroughs. Holding the wafers a long period of time at higher temperatures causes an interaction with gold and glass frit materials. As a result, the gold feedthroughs are damaged and lose their conductivity. This problem can be eliminated using a passivation layer between the gold and glass frit. In this study, PECVD silicon nitride is used between the glass frit and gold feedthroughs for the protection of gold feedthroughs. Figure 3.13 compares the results of bonding directly on gold feedthroughs and bonding when silicon nitride is placed between the gold and glass frit at 435ºC for a period of 60 minutes. It should be noted that this problem can be minimized but not completely eliminated by decreasing the hold time at peak temperature without using the silicon nitride protection layer.

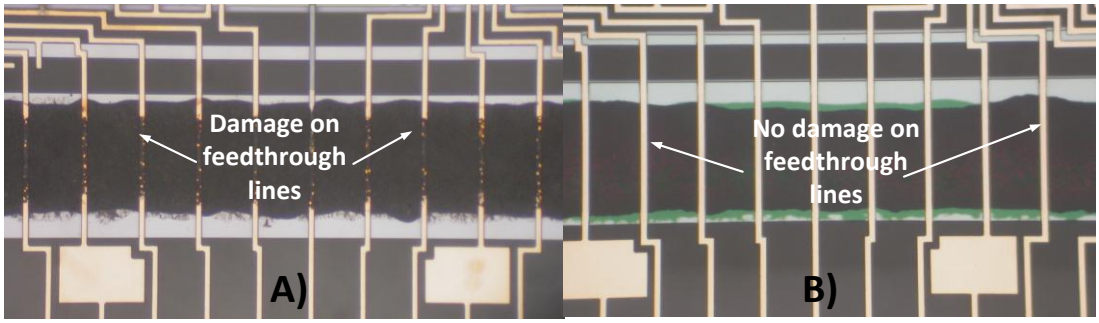


Figure 3.13: The view of gold feedthroughs after glass frit bonding at 435C for a holding period of 60 min: (a) bonding directly on the gold feedthroughs, (b) bonding when silicon nitride protection layer is used between the gold feedthroughs and glass frit.

The main results obtained during the optimization of glass frit bonding on glass wafer with lateral feedthroughs can be summarized as follows;

- Both bonding temperature and holding time at bond temperature are the determining factors in the bond yield. The highest bond yield is obtained at 450ºC for a holding period of 60 min. Lower temperatures are also tested and it is experimentally verified that the yield becomes lower with the decreased bond temperatures. Furthermore, the holding time has a significant effect on the bond yield. A period of time is required for glass frit material to soften and cover the bond surface. Thus, longer holding times also improve the bond quality and increase the yield.

- The bond force is the key parameter for a high yield glass frit bonding. In this study, bond forces of 1500N and 3500N are tested. It is observed that higher bond forces cause glass frit to flow over device area. To overcome this flow problem, the bond force has to be optimized as in eutectic bonding.
- Glass frit and gold have an interaction at high temperatures. This interaction causes gold to lose its conductivity. Shorter holding periods minimizes the problem, but could not solve it completely. Using a passivation layer between the gold and glass frit prevents their interaction. For that purpose, in this study, silicon nitride is used as a protection layer between the gold and glass frit materials.

3.4.3.2 Bonds on Silicon, Silicon Nitride and Gold Surfaces

In this study, the glass frit bonding on silicon, silicon nitride and gold surfaces at 435ºC for a holding period of 60 min is also tested. In the case of bonding on silicon or gold surface, the bond quality is tested by the deflection test. Since the silicon nitride is transparent (the case that silicon nitride is deposited on glass), the bond quality on nitride surface is examined under optical microscope. Bond yields similar to the ones reported in the previous section are obtained. This verifies that the surface material is not important in glass frit bonding and a high quality bonding can be achieved for much different type of materials, once the bond temperature, force and time is optimized.

3.5 Fabrication of Devices with Lateral Feedthroughs

The sensors used to monitor the pressure levels inside the micro packages are fabricated using Silicon-On-Glass (SOG) process. SOG process is the way of forming silicon devices over a glass substrate with recesses and pad metallization [67]. Using a glass wafer as a substrate provides the fabrication of capacitive MEMS inertial sensors which have very low parasitic capacitances and flexible metal routings. The main idea of the SOG process is to anodically bond a glass wafer to a thin silicon wafer, typically 100µm, and form the microstructures using the DRIE after the bonding process. Aspect ratio of 25:1 can be obtained using this process. However, in this process, the critical dimensions cannot exactly be controlled due to the heat generation during DRIE process since the silicon is suspended over a glass substrate [68]. For this purpose, in this study a modified

version of SOG process is developed. This process is based on the anodic bonding of an SOI wafer to a glass wafer. Here, the main difference is the location time of DRIE step in the overall process sequence. Moreover, using SOI wafer gives chance to form microstructures prior to anodic bonding. Thus, the heating problem is completely eliminated. The use of SOI wafer also allows the selection of an optimum device layer thickness. This brings the advantage of achieving maximum aspect ratio in DRIE. In this study, an SOI wafer with 35 μm <111> silicon structural layer and a 500 μm thick pyrex glass substrate are used. The process consists of totally 7 masks: 5 for glass wafer and 2 for SOI wafer. Figure 3.15 presents the main fabrication steps of the process used in this study.

The process begins with the anchor formation on the glass wafer. The anchor regions that will be anodically bonded to silicon are formed on the glass wafer using Hydrofluoric acid (HF). Since HF is an aggressive chemical, PR cannot be used as a mask. Cr/Au is a good solution and can be used as a mask material in HF. The other fact that should be considered is that the polished glass surfaces have to be roughed before the metal deposition. This roughening process, performed in a buffered HF solution, is an essential step to provide a good metal adhesion. Thus, 100Å/1500Å Cr/Au is deposited onto the glass wafers by sputtering or thermal evaporation after this roughening process. The deposited Cr/Au is then patterned using the anchor mask. Wafers are then placed into Cr/Au etchants and HF to form the anchors. The undercut on the glass wafer after HF etching is measured to be close to 1:1.3μm. After forming the anchors, the glass etch masks are stripped and wafer is ready for the second step.

The second step begins with Cr/Au deposition to form lateral feedthroughs. 100Å/1500Å Cr/Au is deposited on the glass wafers after a BHF dip and this Cr/Au is patterned using Metal-1 mask. Here, the most important point that should be considered is that the metal on the anchor regions are not etched. Since the next step of the process includes an etch cycle in BHF, the anchor surfaces have to be protected. Moreover, the thickness of the Cr/Au is also important. The thickness of Cr/Au lateral feedthroughs will determine the surface topography of the bonding region.

The third step includes the deposition of the passivation layer and eutectic bond ring. First, a 5000Å of low stress PECVD Si_3N_4 layer is deposited on the wafers. This layer will be used as a passivation layer between the Cr/Au lateral feedthroughs and the Cr/Au eutectic bonding line. A 300Å Cr/15000Å Au layer is then deposited on the wafers by sputtering or thermal evaporation. The reason that eutectic bonding line is directly deposited on the wafers without patterning the passivation layer is to protect the underlying feedthroughs during the patterning of eutectic bonding line.

The fourth step is the patterning of the passivation layer and eutectic bonding line. First, wafers are patterned using the eutectic mask. This mask forms the eutectic bonding line. The undesired Cr/Au is etched in Cr/Au etchants and the PR mask is then stripped. After forming the bonding line, it is necessary to pattern the passivation layer. The nitride is opened only at the anchor regions using BHF.

The fifth step is carried out to create the contacts on anchor regions using the remained Cr/Au from the previous steps. The contacts are the regions that make electrical contact to the silicon device layer. For this purpose, Metal-2 mask is patterned and the processes of Cr/Au etch and PR strip are performed. This is the final step for the glass wafer. Since the anodic bonding is sensitive to surface contamination, the glass wafer is cleaned in a piranha solution before the anodic bonding process.

The process on SOI wafer begins with Cr/Au deposition. The aim of using Cr/Au layer is to prevent the direct contact of Si and Au. In the case of Au and Si get contacts with each other, the contact regions are damaged at high temperatures necessary for the wafer level vacuum packaging process. The chromium layer is used as a barrier between the silicon and gold. The chromium is a material which is easily oxidized. Thus, a thin layer of gold is placed onto the chromium. The other thing that should be considered is the contact resistances. To obtain good contact resistances, the native oxide on the SOI wafer should be removed by a short BHF dip before the Cr/Au deposition. For that purpose, a 300Å Cr/300Å Au layers are deposited on SOI wafer directly after a short BHF dip. This Cr/Au layer is patterned using contact mask and everywhere is opened except the contact regions. These contact regions will then directly touch to the Cr/Au contact regions on the glass wafer after the anodic bonding.

The second step is the structure formation. The structural layer of SOI is formed by DRIE. The silicon device layer is etched until reaching the buried oxide layer. The timed etch is important to decrease the notching effect. The wafer is then placed into the piranha solution to clean the polymers residues which are formed during the DRIE process. Whenever the polymers residues are completely cleaned, wafer gets ready for the anodic bonding.

One of the most important steps of this process is the anodic bonding of SOI and glass wafers. Normally, the device silicon layer of the SOI wafer should be connected to the chuck of the wafer bonder to get the conventional anodic bonding setup. However, this could not be done due to the buried oxide layer between the handle and device silicon of the SOI wafer. In the literature, there are some methods used to anodically bond SOI to wafer. One of these is to make the device silicon layer of SOI wafer short to its handle silicon layer by metal deposition [69]. Another way, used in this study, is based on the charge distribution on two capacitors in series as in [70]. In this system, presented in Figure 3.14, there are two capacitors in series.

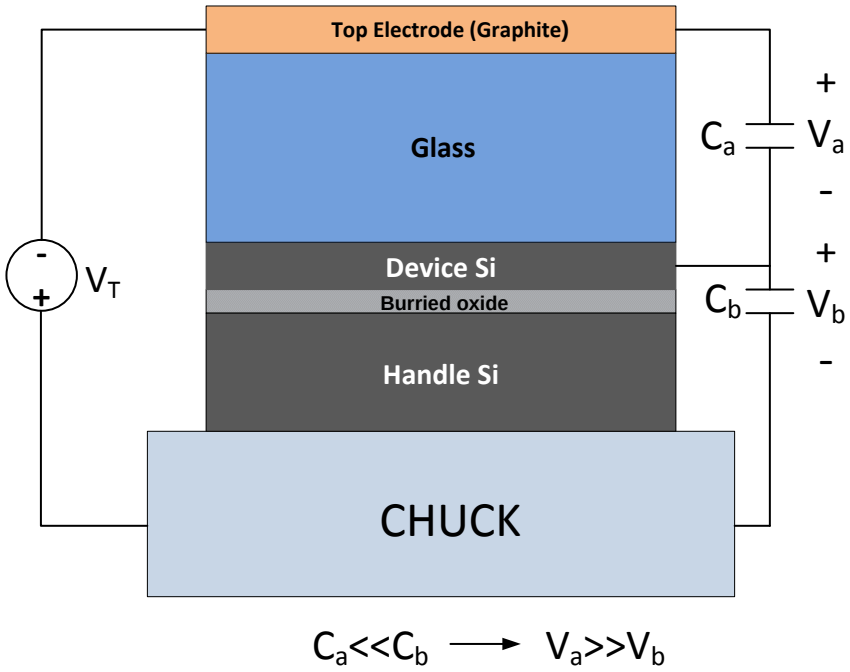
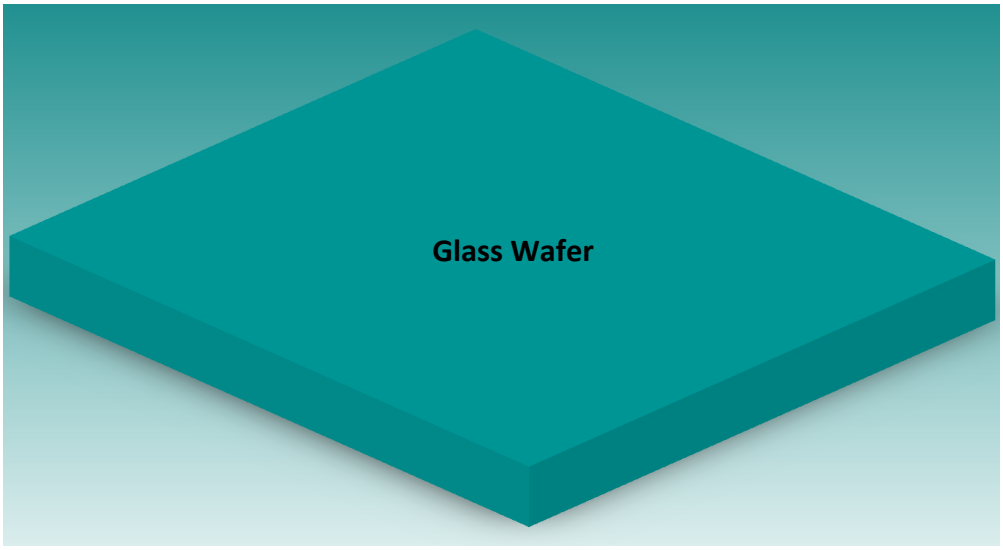


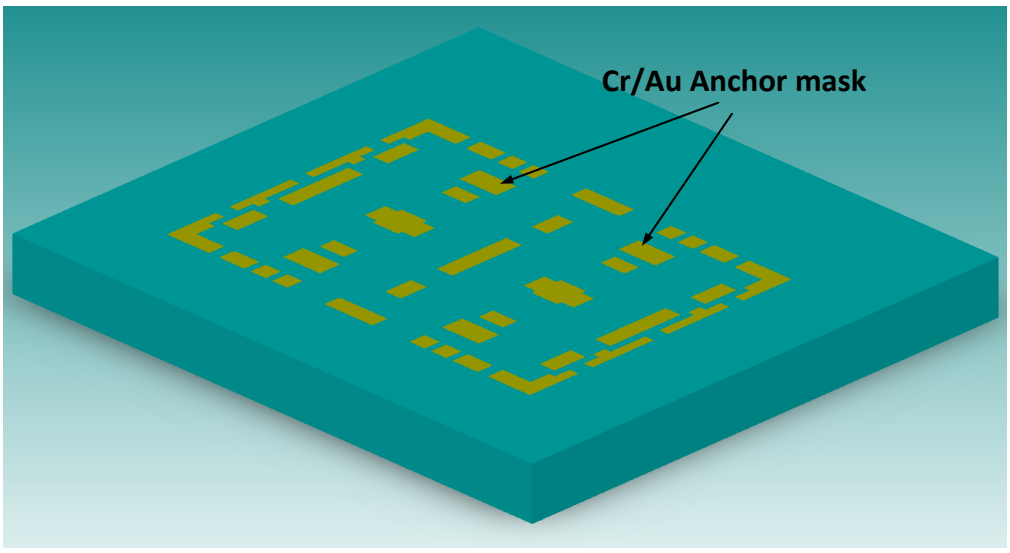
Figure 3.14: The view of anodic bonding scheme.

One (C_a) is between graphite and device silicon layer where glass is defined as insulator between these. The other (C_b) is between the device silicon layer and

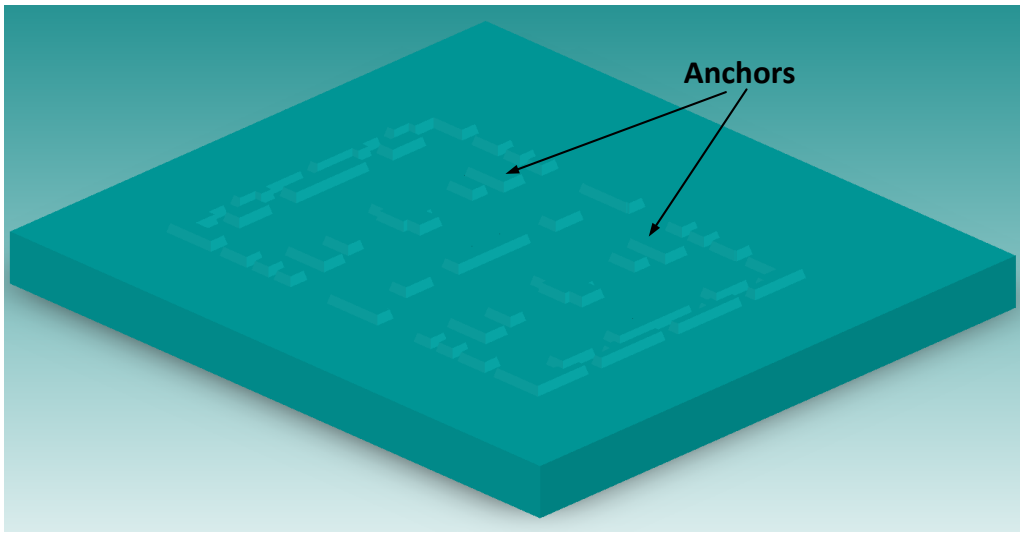
handle silicon layer where the buried oxide is the insulator between these capacitors. The thickness of glass is 500µm while the thickness of the buried oxide is only 2µm. Thus, C_b becomes much larger than C_a. Since these capacitors are connected to each other in series, almost all of the applied potential appears across C_a which is used for the anodic bonding process. After the bonding, the handle layer of the SOI wafer is removed by DRIE. Here, the buried oxide layer of SOI wafer behaves as an etch stop. The device is released after removing the buried oxide layer of the SOI wafer. This is the most critical step of the process and can be achieved either dry or wet etch. Sections 3.5.1 and 3.5.2 will give a detailed explanation about the device release.



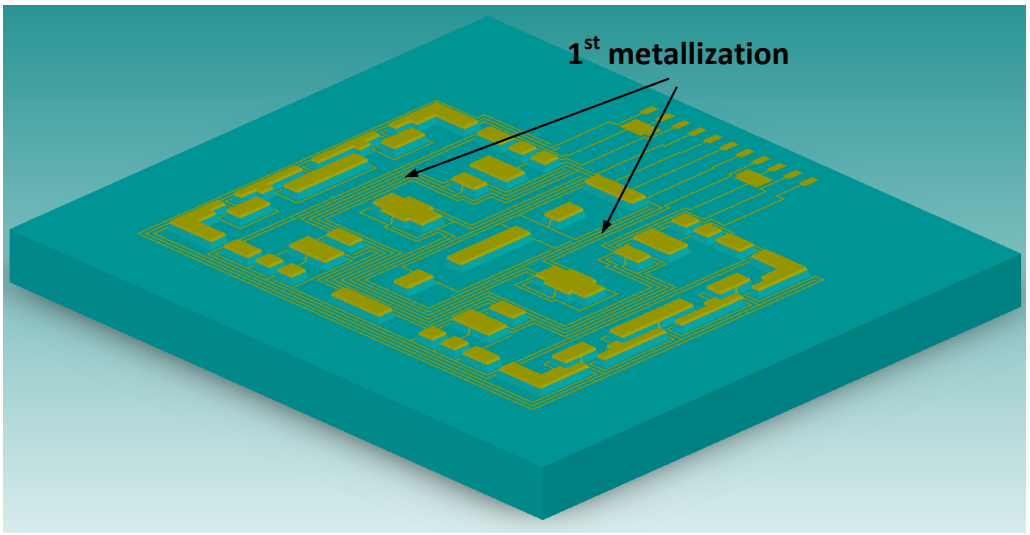
a) Pyrex glass wafer



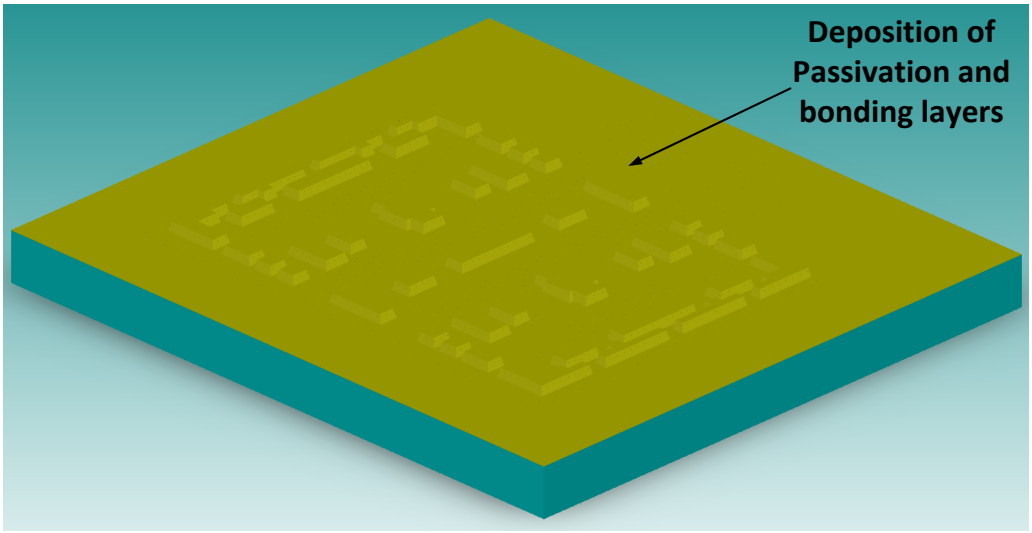
b) Formation of Cr/Au anchor mask



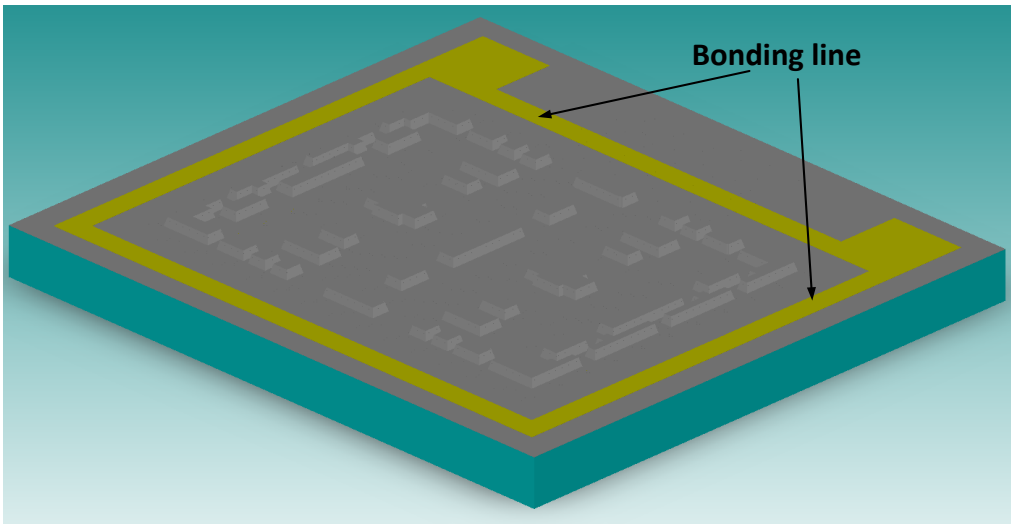
c) Anchor etch



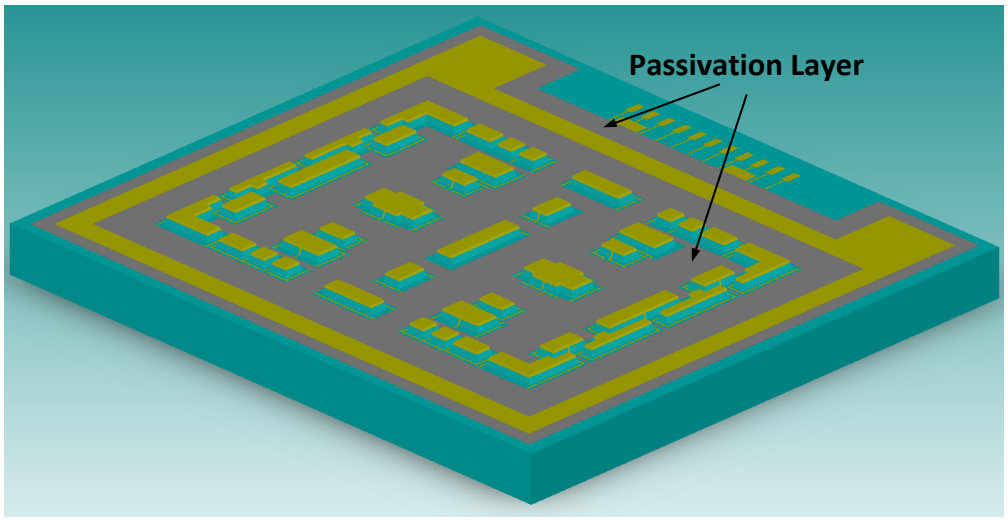
d) 1st device metallization



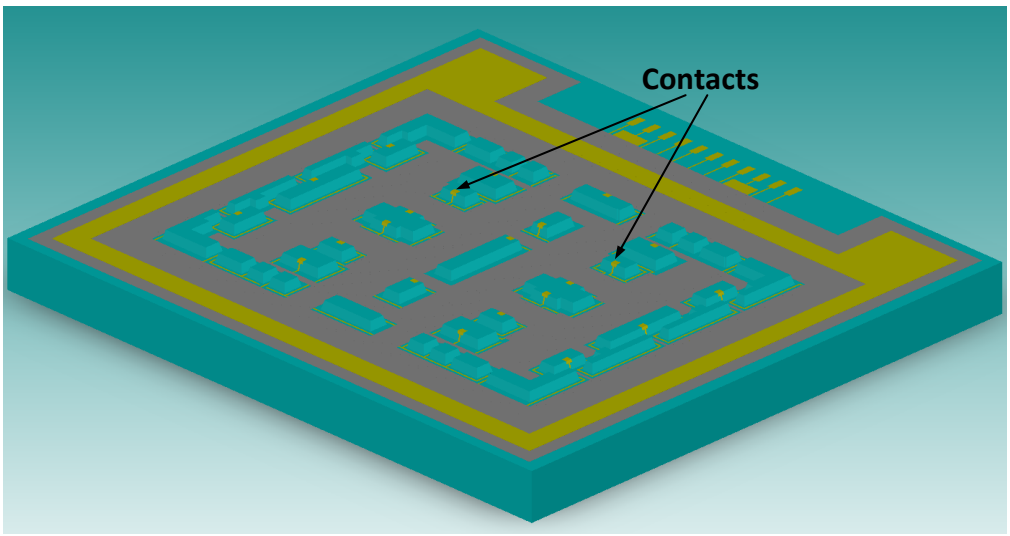
e) Deposition of Si_3N_4 passivation layer and Cr/Au bonding line



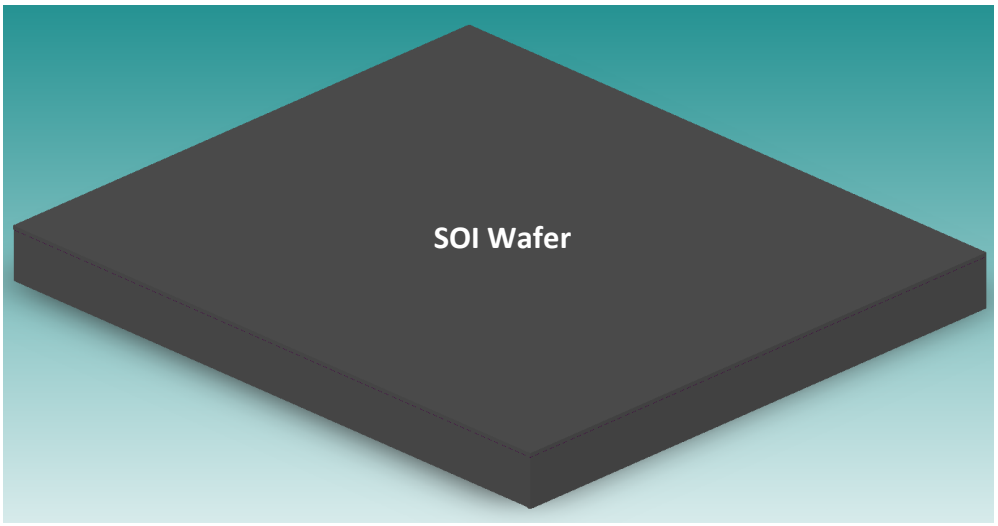
f) Formation of Cr/Au bonding line



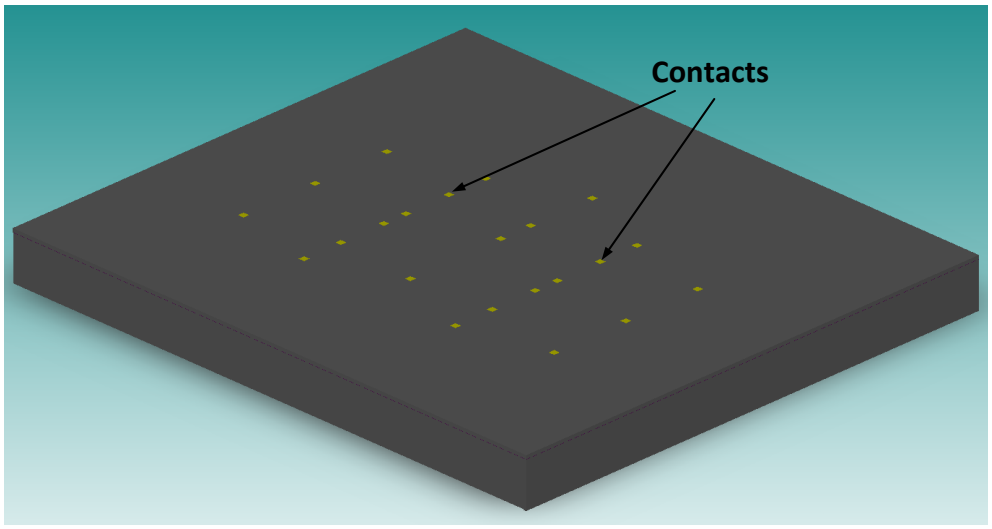
g) Formation of Si_3N_4 passivation layer



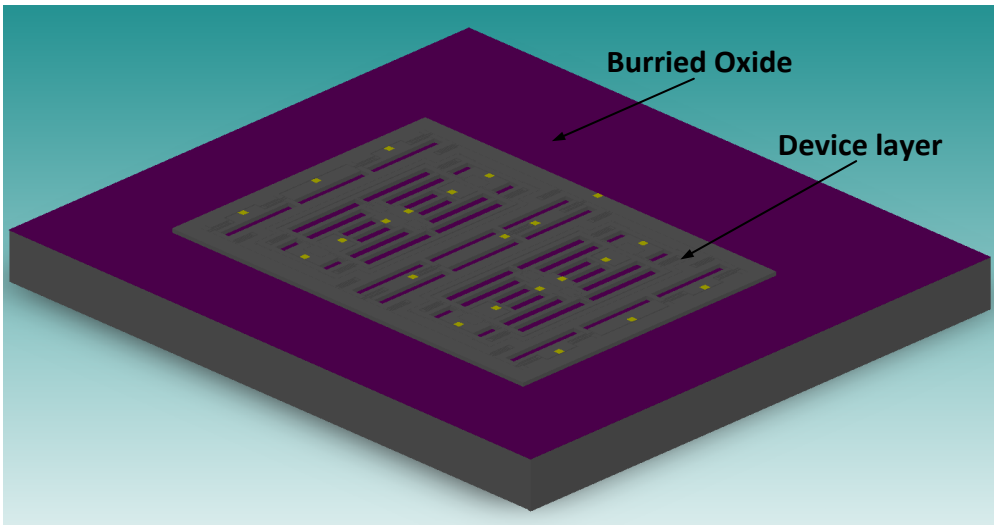
h) Contact formation



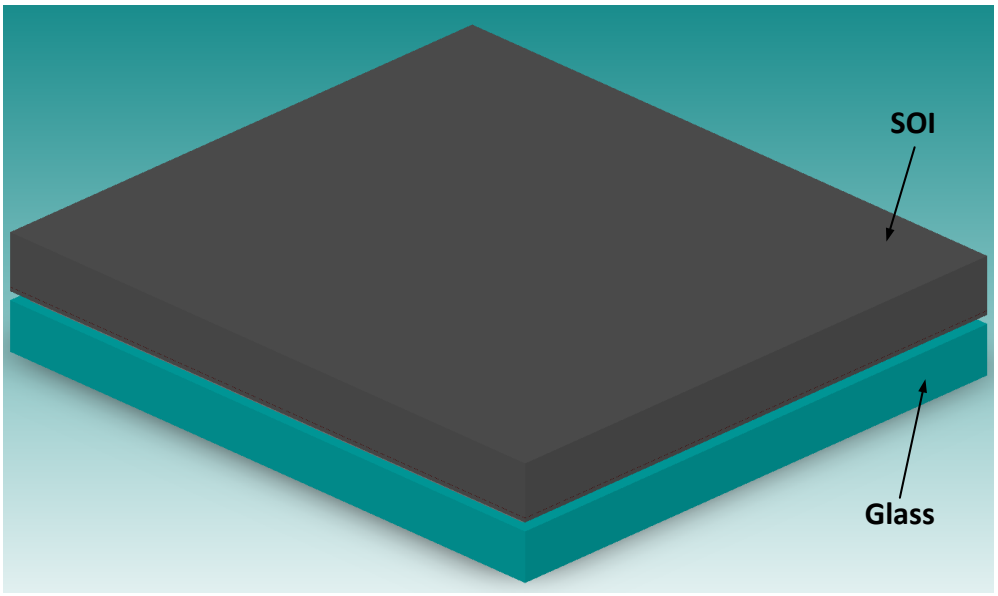
i) SOI wafer



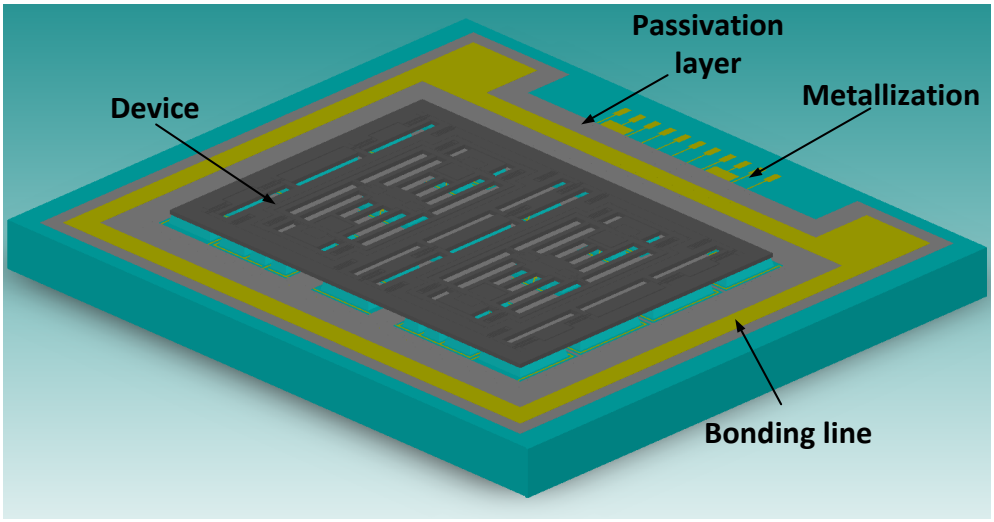
j) Formation of Cr/Au contact regions



k) Etching of SOI device layer until reaching to the buried oxide layer



l) Anodic bonding of glass and SOI wafers



m) Removal of the handle silicon and buried oxide layers of SOI wafer

Figure 3.15: The main fabrication steps of devices with lateral feedthroughs.

3.5.1 Device Release by BHF

Device release is the most significant and problematic fabrication step of this study. The major point to be taken into account in this release process is that the passivation layer should not be damaged during the release of the device. This section presents the experimental results of the device release using 1:5 BHF solution. The thickness of the buried oxide layer of SOI wafer and typical etch rate of the thermally grown oxide in 1:5 BHF is in the order of 2μm and 100 nm/min, respectively. In this case, it is necessary to perform a timed etch since BHF also etches the silicon nitride and

glass substrate. Thus, BHF process is carried out step by step for a period of 20 min. The wafer is then subjected to a series of cleaning and drying procedures to successfully complete the process. The results show it is not possible to remove the buried oxide layer of SOI without eliminating any damage on the silicon nitride passivation layer. Figure 3.16 presents the optical microscope view of a gyroscope die after device release by BHF. It is seen that all nitride layer is removed during the release process.

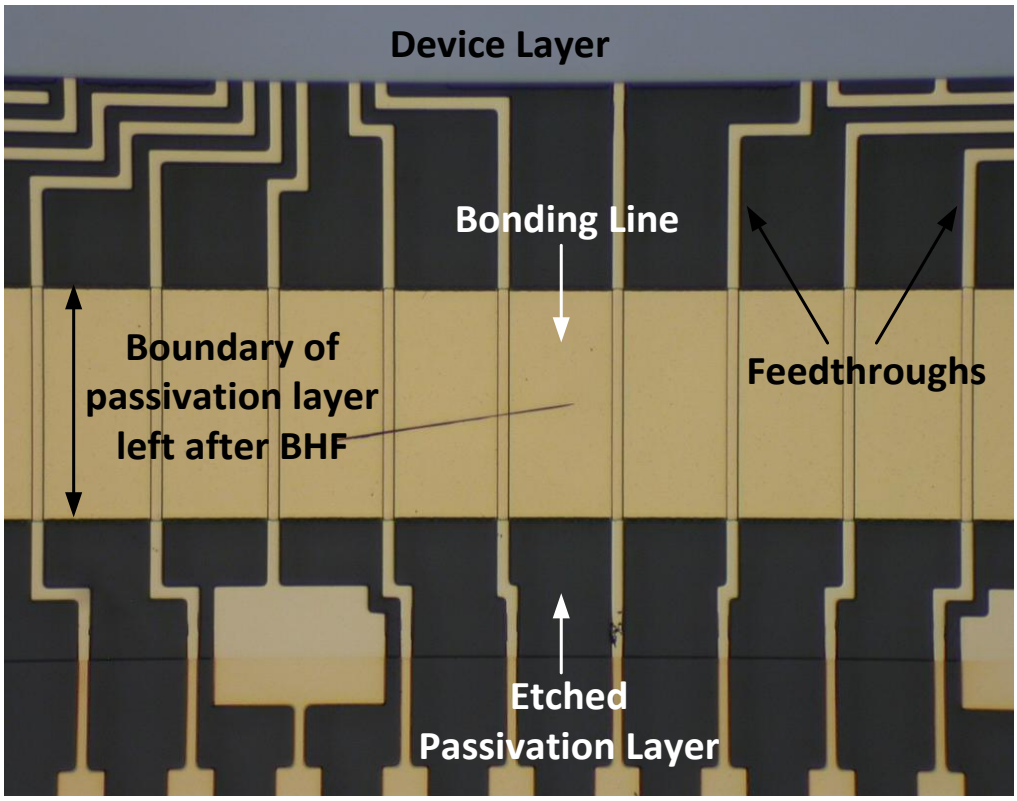


Figure 3.16: The optical microscope view of a gyroscope die released by BHF.

3.5.2 Device Release by RIE

It is possible to remove the buried oxide layer of SOI wafer without damaging the low stress PECVD nitride passivation layer in RIE. It is a well known dry etching technique and in the case of a timed process, almost all of the nitride layer can survive. The device wafer is subjected to a release process in RIE. It is experimentally verified that RIE removed the buried oxide layer of SOI without touching to the nitride layer. Figure 3.17 and Figure 3.18 present the optical microscope view of a gyroscope die and SEM photo of a die including pirani gauge and resonator released by RIE.

RIE not only provides a successful release process as shown, but also it gives a chance to fabricate better contact regions in contrast to BHF. Figure 3.19 compares the contact regions of device wafers released by BHF and RIE, respectively.

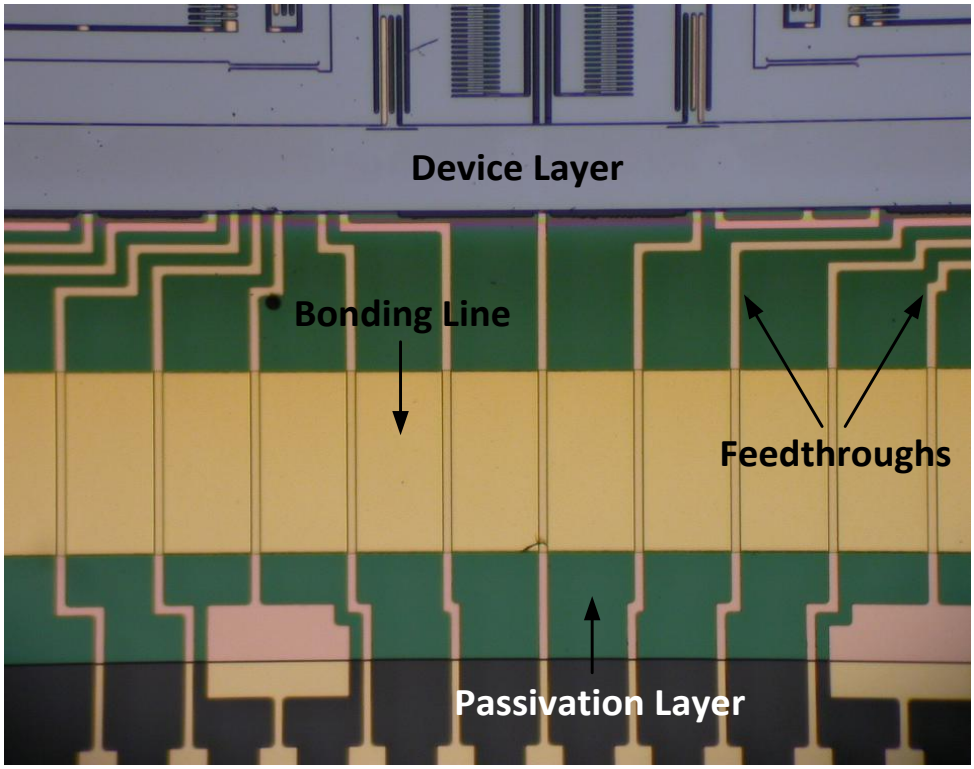


Figure 3.17: The optical microscope view of a gyroscope die released by RIE.

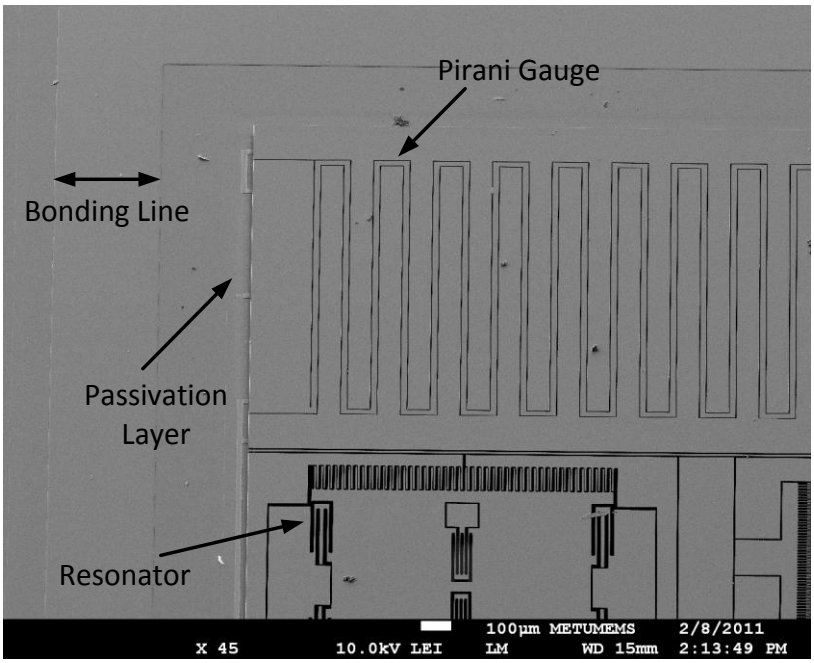


Figure 3.18 : SEM photo of fabricated pirani gauge and resonator.

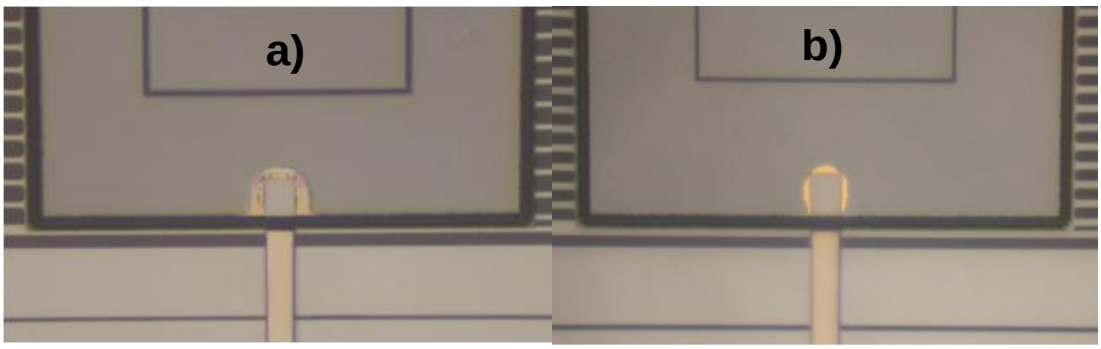


Figure 3.19: The view of contact regions after the release process: (a) photograph of a die released by BHF, (b) photograph of a die released by RIE.

Despite all, RIE has some other problems which affect the wafer level vacuum packaging, especially done with Au-Si eutectic bonding. The problems faced during the wafer level vacuum packaging due to RIE will be explained in the Chapter 5.

3.6 Fabrication of Devices with Vertical Feedthroughs

Clearly, the bonding on a perfectly smooth surface is much easier than bonding on a topographic surface. Thus, devices with vertical feedthroughs provide an easier solution for wafer level vacuum packaging. Moreover, using vertical feedthroughs for electrical connections improves the performance of a variety of MEMS devices, such as capacitive MEMS inertial sensors. This method decreases the amount of parasitic capacitances which are very important for devices that rely on capacitive actuation and sensing. The method of vertical feedthrough is also compatible with flip-chip bonding and thus can be directly mounted on readout circuit chips. The main difficulty of these substrates is the formation of the via openings through the substrate. Even if they are formed; it is also difficult to hermetically fill these openings with a suitable conductor. Some companies offer commercial solutions for fabricating such substrates. In this study, a fabrication flow based on the process offered by the company named Plan Optik is designed. Plan Optik manufactures glass-silicon compound wafers where highly doped silicon vias are isolated from each other with glass. Thus, the glass wafer is supplied by Plan Optik and further process for the fabrication of device wafer with vertical feedthroughs is carried out at METU. The process consists of 5 masks; 3 for glass wafer and 2 for SOI wafer. The process steps are similar, but easier compared to the previous flow presented in

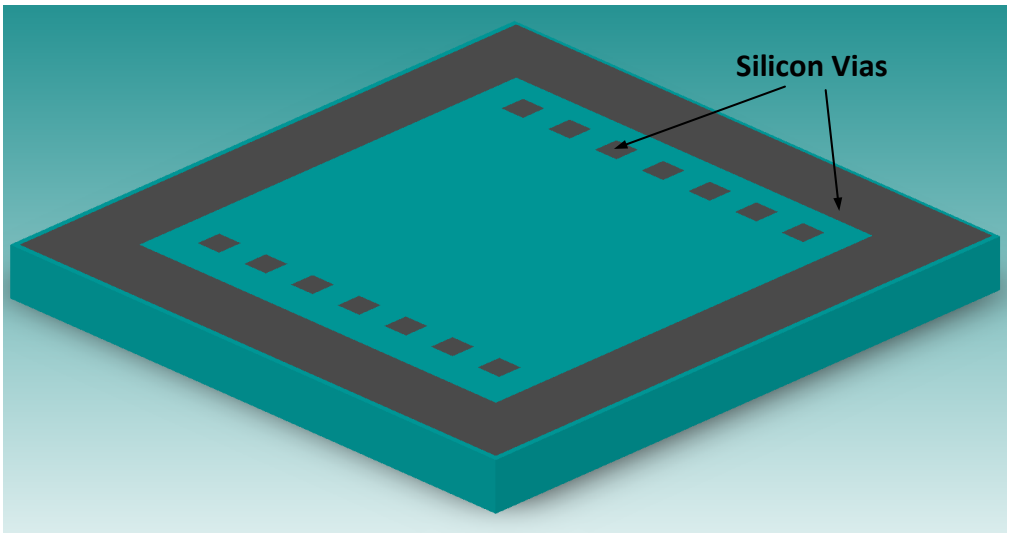
Section 3.5 with respect to the number of process masks. Figure 3.20 presents the main fabrication steps of this process.

The process begins with a Pyrex glass wafer with highly doped silicon vias. After subjecting the wafers into a BHF dip for roughening, 100Å Cr/1500Å Au is deposited by sputtering or thermal evaporation. The anchor regions are defined on this special wafer using the anchor mask. Wafer is then subjected to the process steps of Cr/Au etch, glass etch, and strip, respectively.

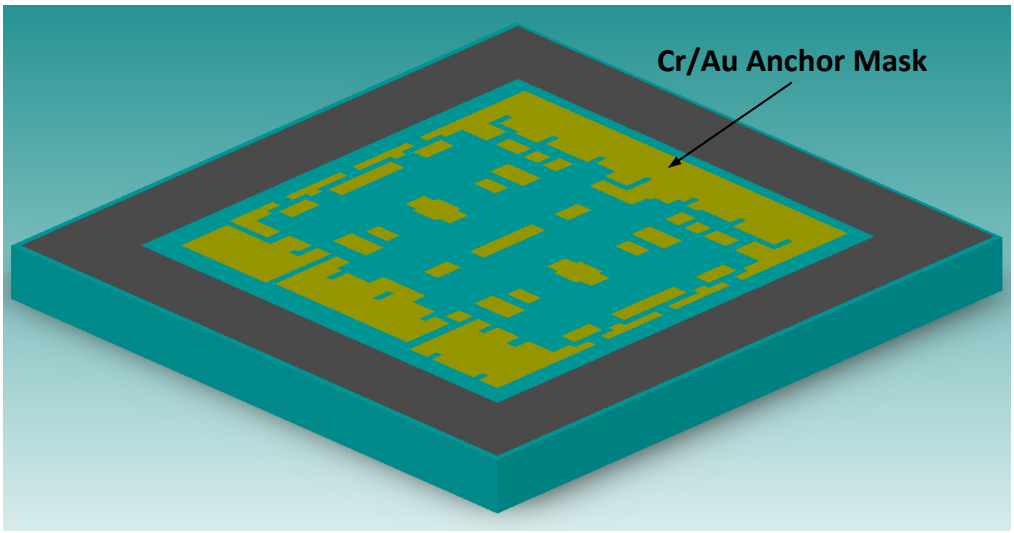
The second step is the formation of electrical connections. After a BHF dip for roughening, 100Å Cr/1500Å Au is deposited by sputtering or thermal evaporation and patterned using metal mask. After etching the Cr/Au and stripping the PR, the fabrication of the glass wafer is completed.

The process steps of the SOI wafer are the same with the previous process. Firstly, contact metals are formed and then microstructures are defined by DRIE.

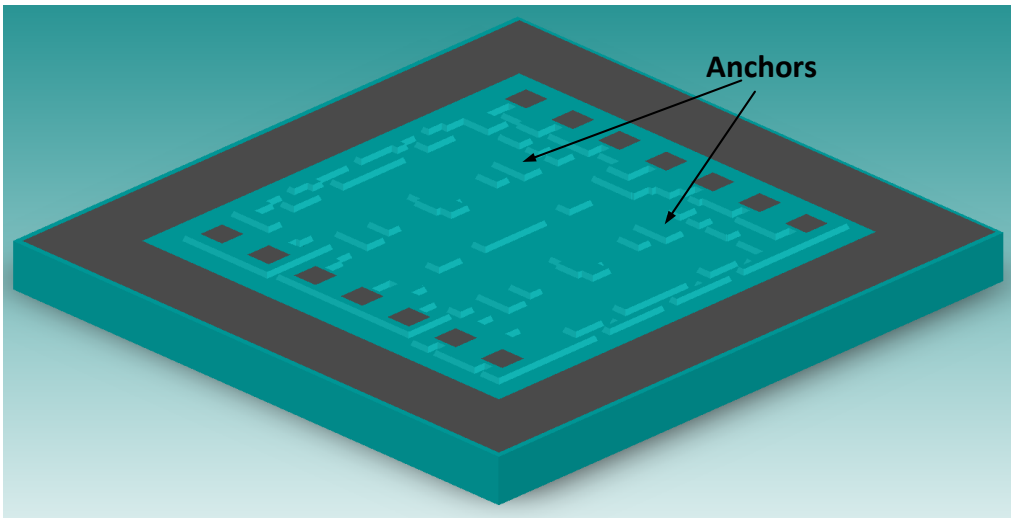
After completing the pre-bonding cleaning procedures of both glass and SOI wafers, anodic bonding is performed. The handle silicon and buried oxide layers of SOI wafer are removed by DRIE and BHF, respectively.



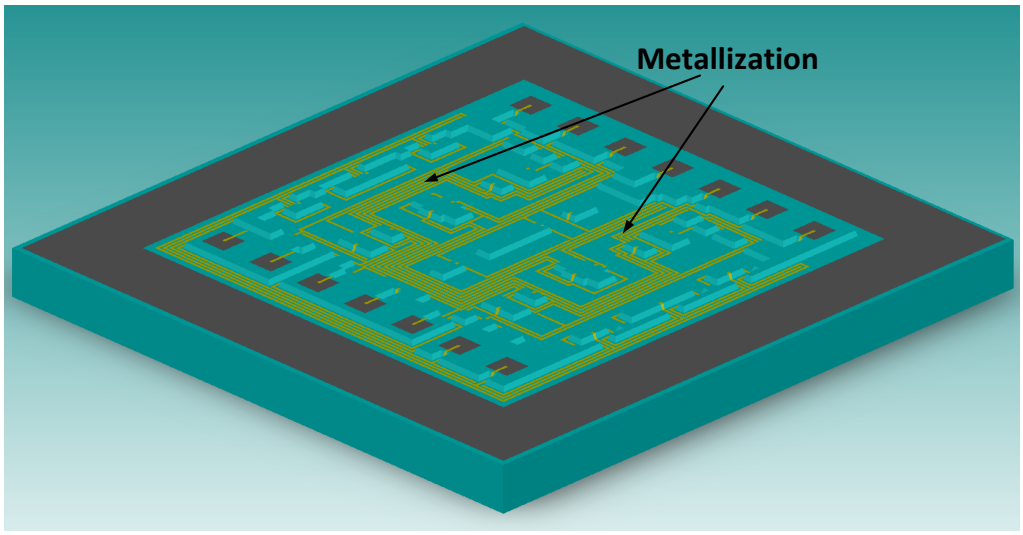
a) Pyrex glass wafer with highly doped silicon vias



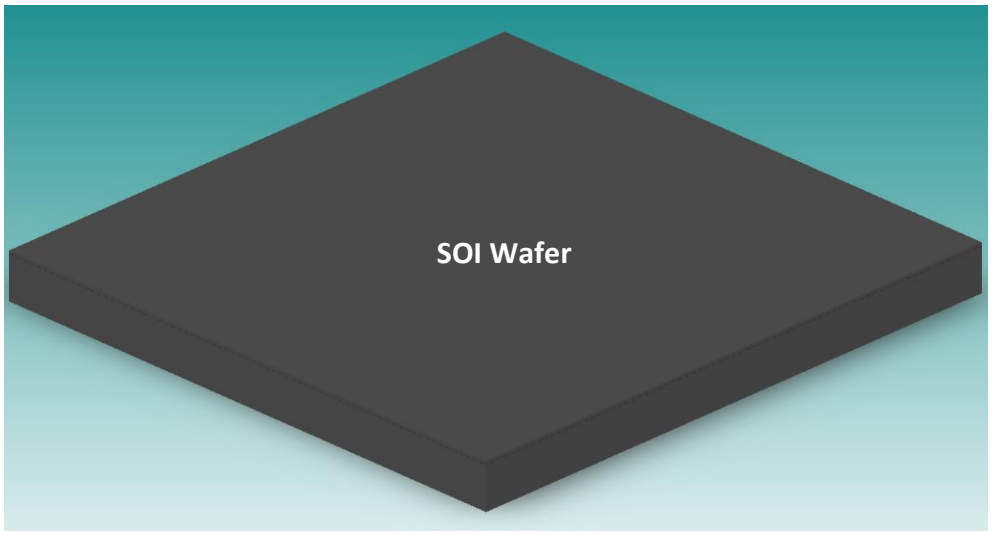
b) Formation of Cr/Au anchor mask



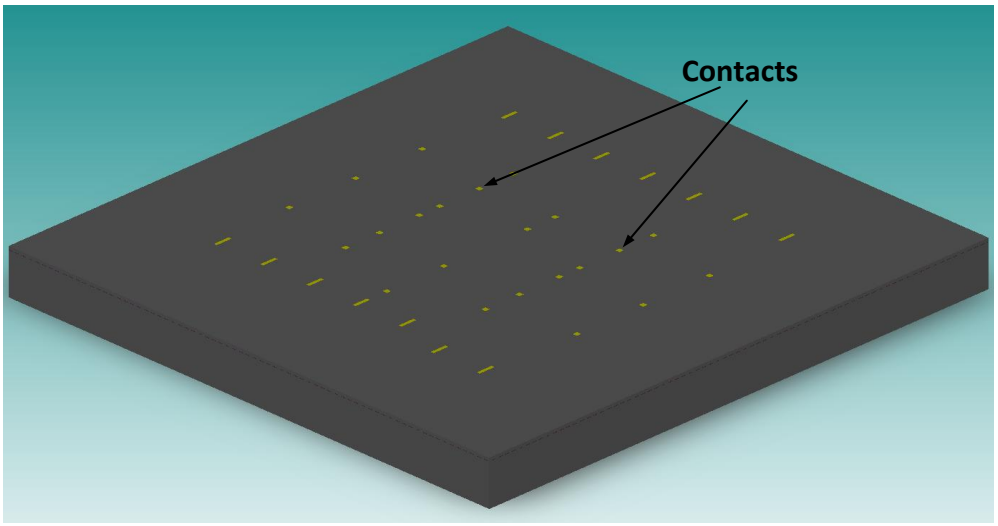
c) Anchor etch



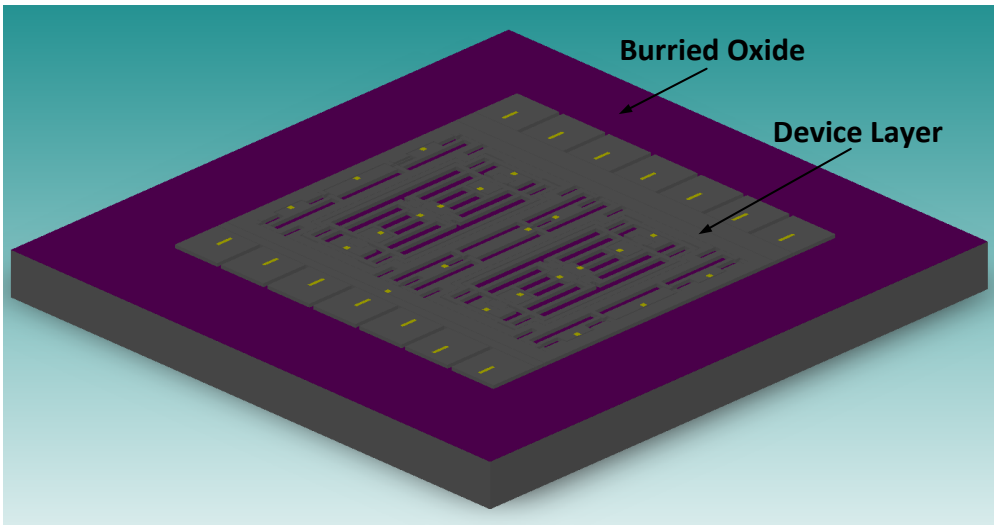
d) Device metallization



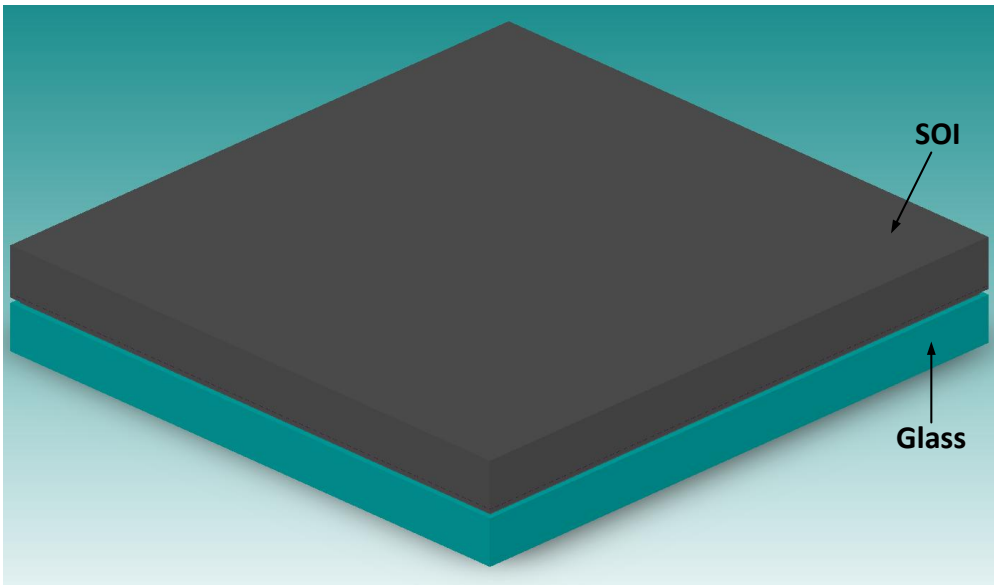
e) SOI wafer



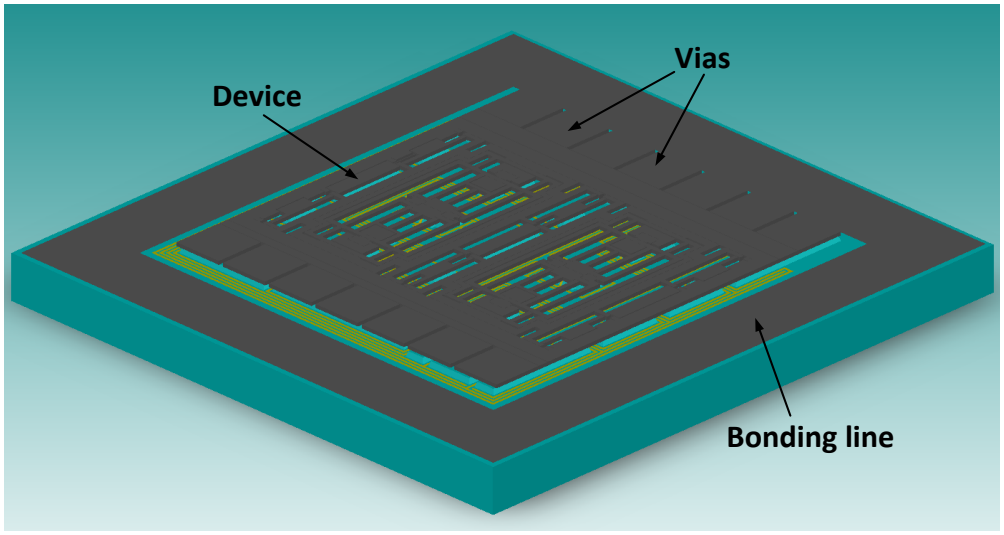
f) Formation of Cr/Au contact regions



g) Etching of SOI device layer until reaching to the buried oxide layer



h) Anodic bonding of glass and SOI wafers



i) Removal of the handle silicon and buried oxide of SOI wafer

Figure 3.20: The basic process steps for the fabrication of devices with vertical feedthroughs.

3.6.1 Problems in Fabrication

The fabrication of glass wafers with highly doped silicon vias is based on the glass reflow process in which a glass wafer is anodically bonded to a silicon wafer patterned using DRIE. The bonded wafers are then placed inside an oven and heated above the melting point of the glass. The melted glass flows through the silicon due to the pressure difference and fills the empty spaces in the silicon. The minimum via

size and the minimum spacing between the vias are determined by the manufacturer, Plan Optik.

The layout, presented in Figure 3.21 is sent to the Plan Optik for the fabrication. Unfortunately, the fabrication of the wafers could not be successfully completed due to several problems that the company faced during the process. The problem is the missing or damaged vias at some regions of the wafer. Figure 3.22 shows a missing via from one sample sent from the company. To overcome this problem, the wafer supplier suggested some modifications in the layout. According to these modifications, a large amount of glass region is replaced by dummy silicon vias, especially dicing streets and outer regions of the wafer. Figure 3.23 presents the modified version of the layout. The production of these glass wafers with highly doped silicon vias are in progress and thus the fabrication of MEMS devices with vertical feedthroughs could not be initiated and will be evaluated in a future work

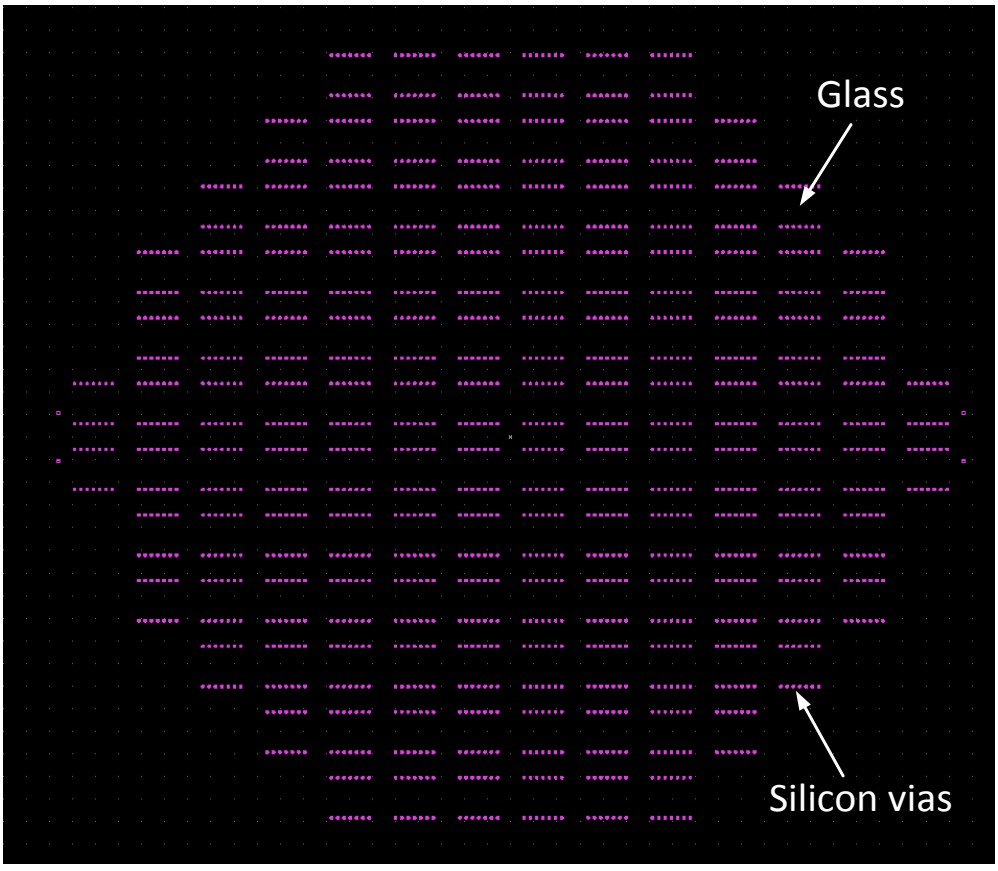


Figure 3.21: The initial layout for the fabrication of glass wafer with highly doped silicon vias.

Figure 3.22: A sample from the first wafer.

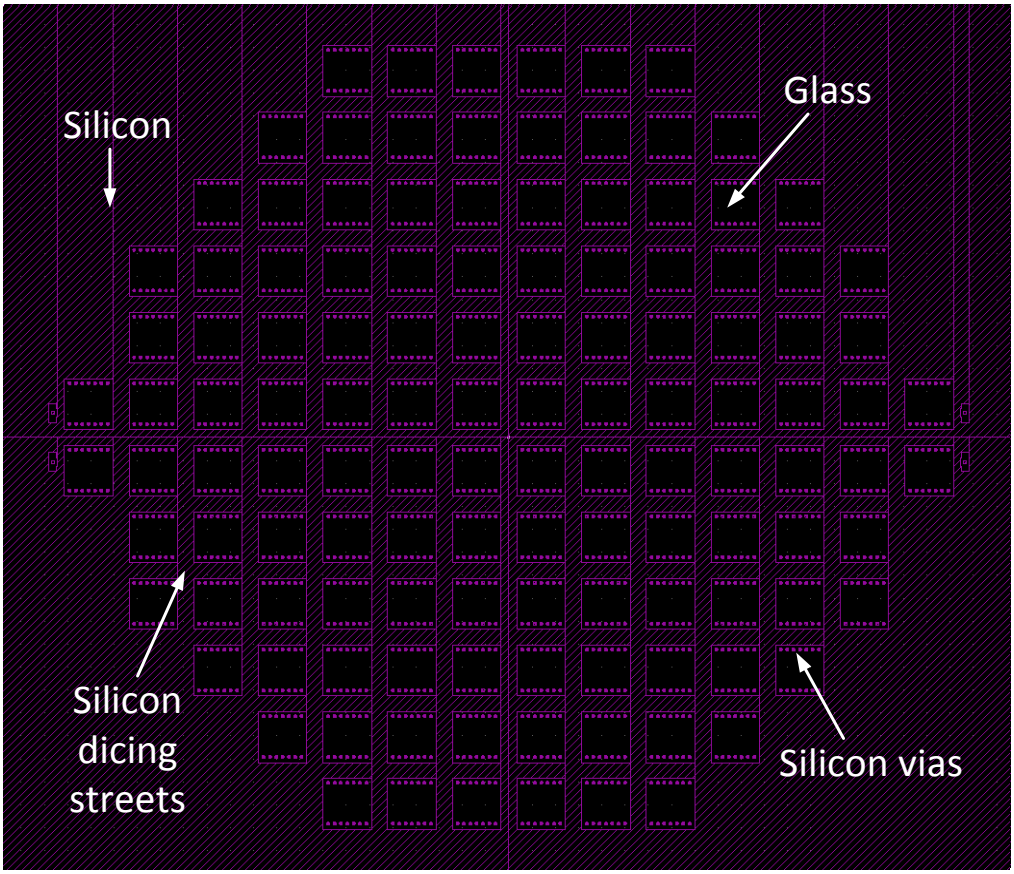


Figure 3.23: The modified layout for the fabrication of glass wafers with highly doped silicon vias.

3.7 Cap Wafer Design and Fabrication

The design of a cap wafer is an essential part of the wafer level vacuum packaging process. As presented above, there are two types of device wafers, with lateral and vertical feedthroughs, planned to be used in this study. The cap wafer requirements for these device wafers are different. The cap design for device wafers with vertical

feedthroughs is easier whereas it is difficult for device wafers with lateral feedthroughs. Not only forming the cavities, but also reaching the feedthroughs for the test after packaging process is essential for device wafers with lateral feedthroughs. These requirements make both design and fabrication of the cap wafer difficult. On the other hand, since the electrical connections are vertically taken outside the package by conductive vias, cap wafer design is simple for device wafers with vertical feedthroughs. This section presents the design and fabrication procedures for both devices wafers with lateral and vertical feedthroughs.

3.7.1 Cap wafers for Devices with Lateral Feedthroughs

For testability purposes, the pad windows have to be formed on the cap wafers in order to gain access to the wire bond pad region. The fabrication of cap wafers mainly consists of two separate KOH processes performed on the both sides of the wafers. Figure 3.24 presents the main process steps of cap wafer fabrication.

The process begins with the thermal oxidation of silicon wafers. Thermal oxide has superior material properties that can be used as a mask against the KOH solution. It has differing selectivity and etch rates depending on the temperature and concentration of the KOH solution. Wafers are placed into a high temperature oxidation furnace after a number of cleaning steps to thermally grow oxide on these wafers. A 1.2 μm of thermal oxide is sufficient for the two KOH processes used to pattern the cap wafer.

The second step is the pad window formation. The backside of the silicon wafer is patterned with the pad window mask. It is important to protect the other side of the wafer to prevent the oxide to be etched during the formation of pad window. Since the thermal oxide is etched in a BHF solution, PR is a good choice in protecting the oxide at the other side of the wafer. A 3M KOH at 80ºC is prepared for the pad window etch. KOH is known as very reliable processes in respect to repeatability in etch rates and selectivity. A nearly 280 μm depth cavity is formed after the first KOH. The selectivity and etch rate of KOH is checked after this process. The etch rate is nearly 51μm/hour and the calculated oxide selectivity is 1μm:390μm which are very similar to the expected values proving that KOH etch is very reliable process. Wafers are then subjected to some cleaning procedures before proceeding with the cavity formation.

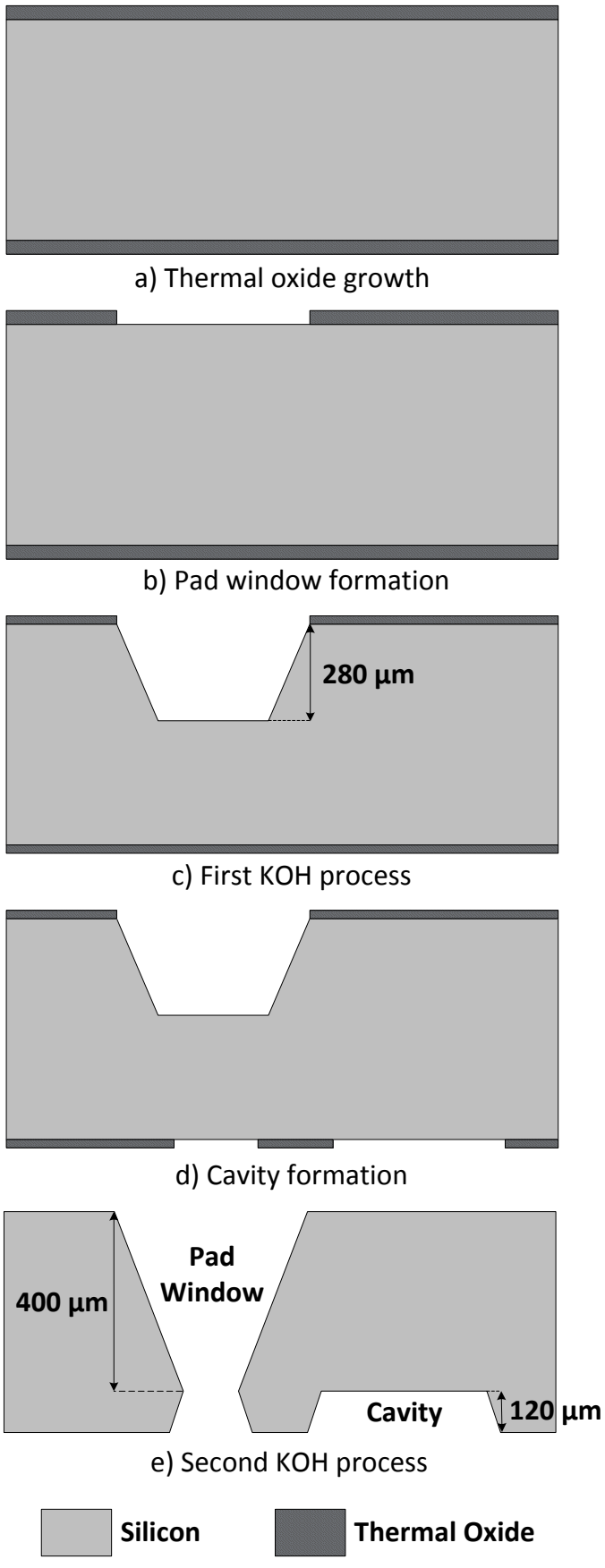


Figure 3.24: The main process steps for the cap wafer fabrication.

Next step is the forming cavity mask on the other side of wafer. Similarly, it is important to protect the oxide on the surface of the wafer that contains pad windows. However, since there are deep pad window cavities, it is difficult to protect this oxide. Spray coating is one way of coating PR especially inside the deep trenches. This side of the wafers is spray coated to protect the remained oxide which is necessary during the second KOH. Wafers are then patterned by cavity mask and placed into BHF solution to form the cavities.

Final step is the second KOH process. It should be noted that the oxide mask is thinned during the first KOH step and it is important to exactly calculate the time that oxide can resist to the second KOH step. Wafers are placed into the same KOH solution and held until pad windows drills. The fabrication of the cap wafers is finalized after completing the necessary cleaning procedures and stripping the remained thin oxide mask layer. According to the bonding type planned to use in wafer level vacuum packaging, wafers are coated with glass frit, Nanogetters^{TM} or neither.

3.7.2 Cap Wafer for Devices with Vertical Feedthroughs

As presented above, cap wafer design is simple for the devices with vertical feedthroughs since there is no need to drill pad windows on the cap wafer to reach the feedthroughs for testability. Thus, just a cavity fulfills the requirements of the cap wafers for devices with vertical feedthroughs. Therefore, the fabrication becomes easier compared to the cap wafer described in the previous section. In this study, cap wafers using both silicon and glass wafers have been fabricated. In the case of fabricating the cap wafer using silicon, both DRIE and KOH can be used for the cavity formation. However, KOH is advantageous compared to DRIE due to its batch processing capability. In the case of fabricating the cap wafer using glass wafers, Hydrofluoric acid (HF) can be used to form the cavities. It is difficult to form very deep trenches using HF with acceptable undercut, since it etches glass isotropically. On the other hand, there is no need to form deeper trenches and nearly 50μm deeper cavities are sufficient for this study.

3.8 Wafer Level Vacuum Packaging using Au-Si Eutectic and Glass Frit Bonding

This section presents the wafer level packaging of the fabricated device wafers. Since devices with vertical feedthroughs could not be fabricated due to problems described in the Section 3.6.1, wafer level vacuum packaging process is only applied to the devices with lateral feedthroughs. The packaging process includes the application of the optimized Au-Si and glass frit bonding recipes on the fabricated sensor wafers. Figure 3.25 presents the conceptual view of wafer level vacuum packaging process. In this figure, the cap wafer is bonded to the bonding line located around the MEMS device.

In this study, 12 sensor wafers were fabricated using the fabrication technique. Prior to the packaging process, gyroscopes, resonators and pirani gauges on the wafer tested at wafer level and working sensors are identified. These wafers are then wafer level vacuum packaged using both glass frit and Au-Si eutectic bonding technologies. Table 3.4 presents the summary of 12 wafer level vacuum packaged sensor wafers. Figure 3.26 and Figure 3.27 show the microscope and SEM pictures of a wafer level vacuum packaged sensor wafer. The test procedures and detailed test results of these devices will be described in chapter 4.

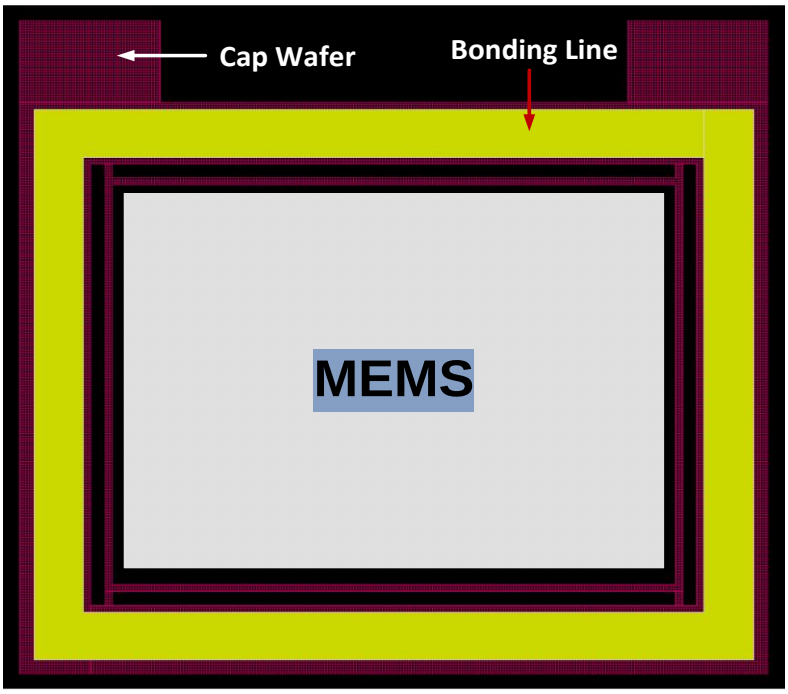


Figure 3.25: The conceptual view of wafer level vacuum packaging.

Table 3.4: Results of wafer level vacuum packaging trials on sensor wafers.

SNW	Release	Contact Region	WLVP	Status
1	BHF	BHF+Contact metal	Glass Frit 450ºC 60 min	No working sensors. Metal lines were damaged.
2	RIE	BHF+Contact metal	Au-Si Eutectic 420ºC 60 min	Wafers were broken during WLVP process
3	RIE	BHF+Contact metal	Au-Si Eutectic 420ºC 60 min	No working sensors. Metal lines were damaged.
4	RIE	BHF+Contact metal	Au-Si Eutectic 420ºC 30 min	No working sensors. Metal lines were damaged.
5	RIE	BHF+Contact metal	-	Unsuccessful release
6	RIE	BHF+Contact metal	Glass Frit 435ºC 60 min	Atmospheric pressure
7	BHF	With BHF	Glass Frit 435ºC 10 min	Vacuum
8	RIE	BHF+Contact metal	-	Unsuccessful release
9	RIE	No BHF	Au-Si Eutectic 420ºC 60 min	Atmospheric pressure
10	RIE	No BHF	Glass Frit 435ºC 60 min	Vacuum
11	RIE	No BHF	-	Unsuccessful release
12	BHF	With BHF	Glass Frit 435ºC 10 min	Vacuum

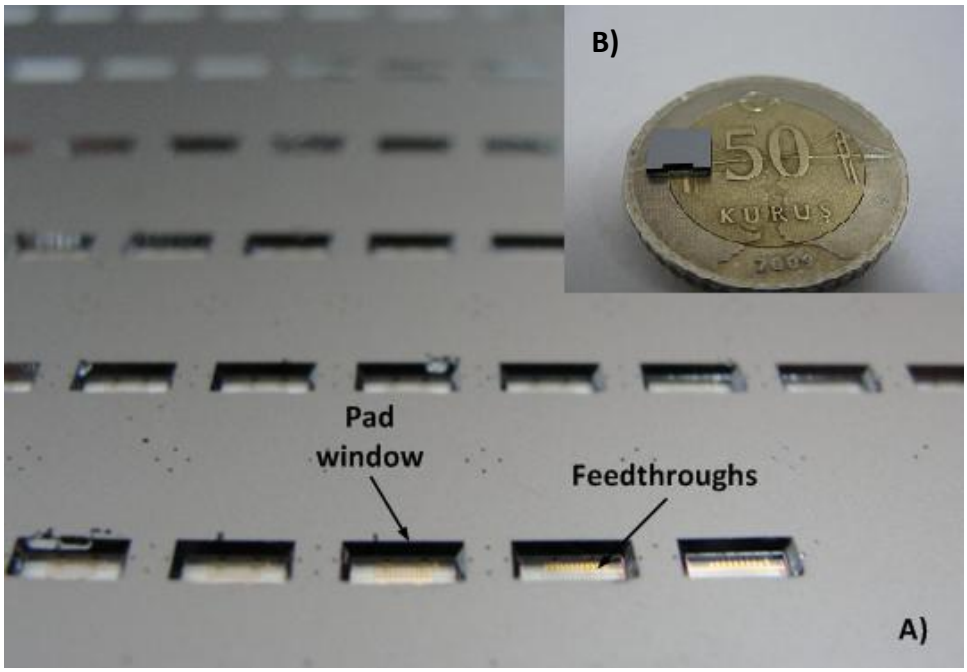


Figure 3.26: The view of device wafer with lateral feedthroughs after wafer level vacuum packaging: (a) top view, (b) view of a gyroscope die after dicing.

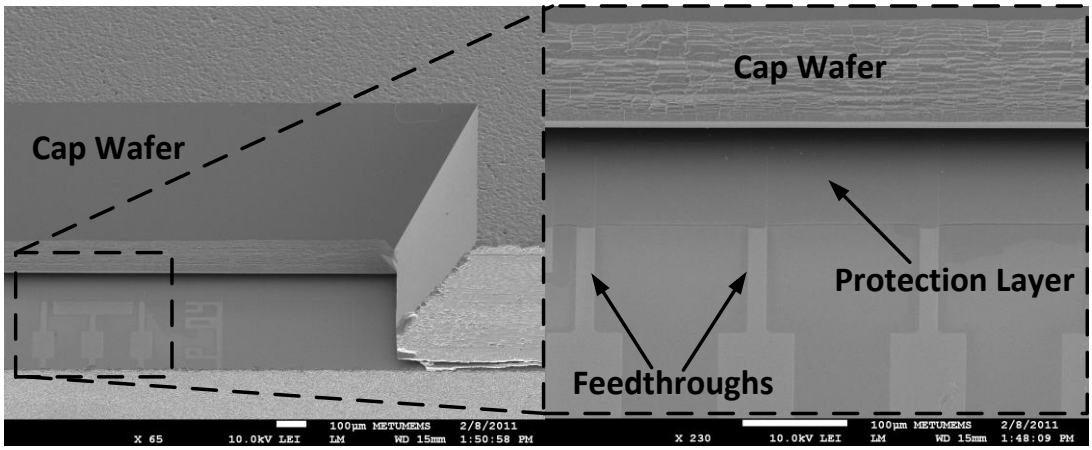


Figure 3.27: SEM pictures of a die from SNW#9 vacuum packaged by glass frit bonding.

3.8.1 Contact Regions at High Temperatures

The main problem faced during the packaging processes is the damage in the contact regions. The gold used for the device metallization is in direct contact with the silicon device layer. At high bonding temperatures, the eutectic temperature of Au-Si pair is exceeded and degradation in device metallization is observed. Most of the devices on the sensor wafer were not able to work because the electrical connections

were lost after the packaging process. To overcome this problem, 3 different contact configurations are used. The properties of these contacts are described as follows;

- **Contacts with BHF:** In this case, silicon is subjected to a short BHF dip to remove the native oxide before anodic bonding. Thus, a direct contact between the gold device metallization and silicon structural layer provides a eutectic formation at the contact regions after anodic bonding. As a result, contact resistances in the range of 100-300Ω are obtained with this case. However, since the eutectic formation has begun even during the device fabrication, these contact regions generally fail at the high temperatures used during the packaging process.
- **Contacts with contact metal and BHF:** To prevent the direct contact of silicon device layer and gold metallization, contact metal layer is used. The Cr/Au contact metal layer is placed between the silicon device layer and gold metallization. The main function of this contact metal is to use the chromium layer as a diffusion barrier. For that purpose, 300 Å Cr/ 300Å Au is deposited and patterned on the silicon wafer after a short BHF dip. This type of contact is more robust than the first one during the packaging process. However, it still shows degradation at high temperatures.
- **Contacts without BHF:** Another configuration is the contact formation between the gold-silicon pair without a BHF step. This configuration shows contact resistances higher than 100kΩ due to the existence of the native oxide layer. Higher contact resistance does not affect significantly the resonating devices due to their readout circuit. However, it has got a significant effect on the performances of pirani gauges and these devices could not be used with such a high contact resistance. On the other hand, these contacts are more robust during the packaging process and prevent the damage at high temperature. Even using the native oxide on silicon is used as a barrier, the diffusion of Au-Si suppress this barrier and a eutectic formation at contact regions are observed after the packaging process. This means that high contact resistance before the packaging process turns into low contact resistance at the end. This is not a good solution, but it works in the protection of Au-Si contact regions during the packaging.

3.8.2 The Effect of Cooling Step on the Contacts

As described previously, the Au-Si contact regions are damaged at high temperatures used for the wafer level vacuum packaging. Experiments show that cooling period has a significant effect on the contact degradation. While the contacts lose their conductivity in the case of packaging using shorter cooling periods, the ones packaged using longer cooling periods work well. Figure 3.28 presents two packaged dies with shorter and longer cooling periods at the same temperature.

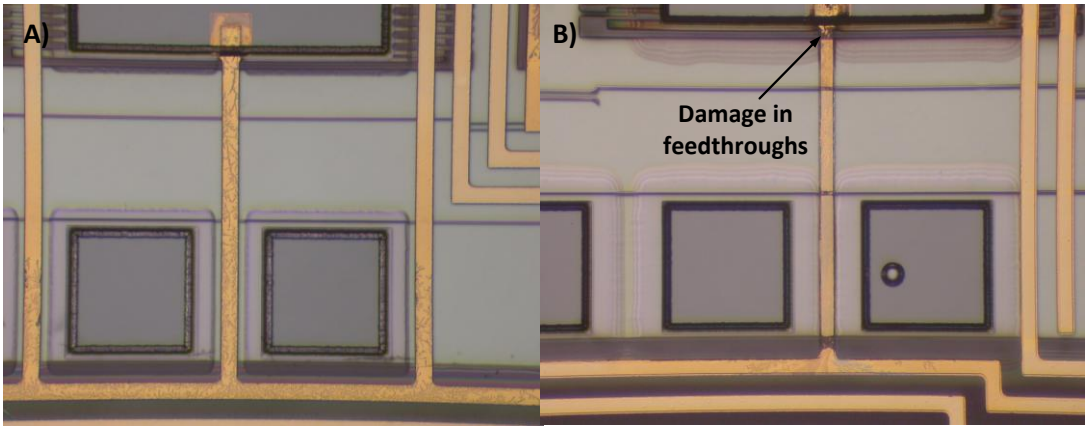


Figure 3.28: Two packaged dies at a temperature of 420°C: (a) longer cooling, (b) shorter cooling.

3.9 Summary of the Chapter

This chapter presents the development of a wafer level vacuum packaging process for MEMS devices. It starts with the detailed investigation of the Au-Si eutectic bonding technology, including the previous works and bonding optimization on both topographic and non topographic surfaces. The Au-Si bond quality is tested using deflection test. The experimental results show that bonding on planar surfaces is achieved at 390ºC whereas a temperature of 420ºC is needed for the non planar surfaces. The bonding yield on both surfaces is 100%. Similarly, glass frit bonding optimization is carried out on different types of surfaces. The bond quality is tested by optical inspection and a yield of %99.4 is obtained at 450ºC for a holding time and bond force of 60 min and 1500 N, respectively.

MEMS gyroscopes, resonators and pirani gauges with lateral feedthroughs are fabricated by a new SOG process. The new SOG process is based on the use of SOI wafers and suitable with wafer level vacuum packaging process using both Au-Si

eutectic and glass frit bonding. On the other hand, a study on the development of similar devices with vertical feedthroughs is proposed. The fabrication of these devices could not be initiated due to the problems with the wafer supplier. The wafer supplier could not achieve to fabricate glass wafers with silicon vias according to the initial layout and a modification in the layout has been requested. The cap wafers for devices with lateral and vertical feedthroughs have been designed and fabricated.

The chapter ends with the wafer level vacuum packaging of fabricated devices using the optimized Au-Si eutectic and glass frit bond recipes. The main problem in this step is the damage of device metallization after the wafer level vacuum packaging process. Since higher temperatures are used, the device metallization is damaged due to the Au-Si eutectic formation between the silicon structural layer and gold feedthroughs. This problem is minimized by extending the period of cooling step in the bonding recipe and using the native oxide on silicon as a barrier. The test results will be presented in Chapter 4.

CHAPTER 4

TEST RESULTS

This section presents the test results of MEMS gyroscopes, resonators and pirani vacuum gauges before and after wafer level vacuum packaging. Section 4.1 starts with the functionality tests of MEMS gyroscopes, resonators and pirani gauges including the test setup and results. Section 4.2 presents the characterization of these sensors at vacuum and gives their performance results as a vacuum sensor. Section 4.3 shows the test results of wafer level vacuum packages fabricated using Au-Si eutectic and glass frit bonding.

4.1 Functionality Tests

After the fabrication is completed, the sensors have to be subjected to the functionality test under atmospheric conditions. The aim of this test is to identify the functional and non-functional dies. This test is different for MEMS resonating structures and pirani gauges. While a simple resistance measurement is sufficient for pirani gauges, the resonance characteristics of MEMS gyroscopes and resonators have to be observed. This section presents the functionality tests of MEMS gyroscopes, resonators and pirani gauges, including the methods and test setups used.

4.1.1 Tests of Gyroscopes and Resonators

The aim of this test is to observe the resonance characteristics of the fabricated gyroscopes and resonators and identify the non-functional dies. Figure 4.1 presents the test setup for the functionality test. The test setup is composed of probe station, dynamic signal analyzer and power supply.

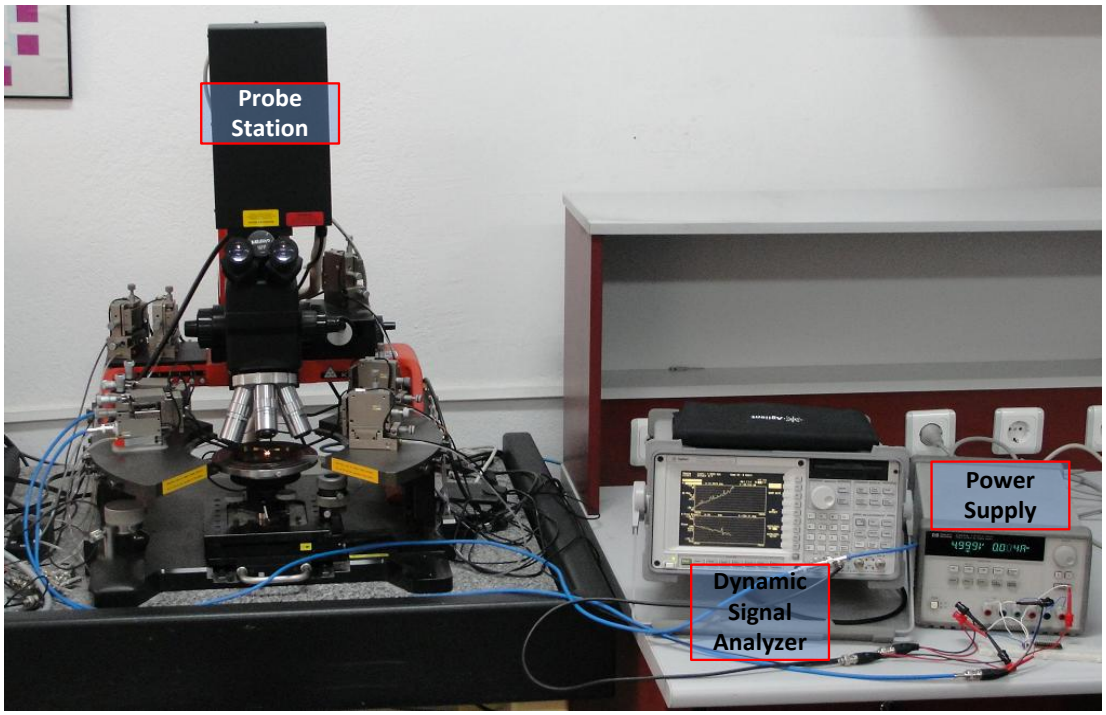


Figure 4.1: The functionality test setup for gyroscopes and resonators.

In the test, the sensor wafer is placed under probe station and fixed. The probe station enables electrical contacts to the sensor. The proof mass voltage and AC source is provided by power supply and dynamic signal analyzer, respectively. The dynamic signal analyzer also sweeps the desired frequency band and gives the resonance characteristics of the sensor. The sensors which pass this test are then subjected to the vacuum tests.

4.1.1.1 Results

This section presents the functionality test results of fabricated gyroscopes and resonators under atmospheric conditions. Drive and sense modes of the gyroscopes and resonators Design-1 and Design-2 are tested at wafer level. Figure 4.2 shows the typical resonance characteristics of gyroscopes and resonators at atmosphere. Table 4.1 and Table 4.2 present the functionality test results of gyroscopes and resonators from different sensor wafers.

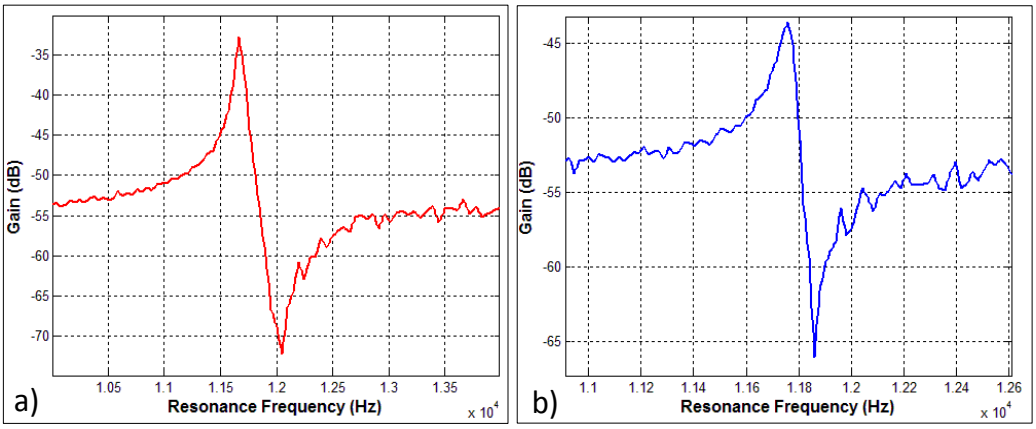


Figure 4.2: Measured resonance characteristics at atmosphere: (a) gyroscope, (b) resonator.

Table 4.1: Measured resonance characteristics of fabricated gyroscopes.

Gyroscope	V_{PM} (V)	V_s (V_{pk})	f_{drive} (kHz)	Gain (dB)	f_{sense} (kHz)	Gain (dB)
SNW#1_K06	10	5	13.1	-38.2	12.4	-23.2
SNW#1_M06	10	5	12.8	-41.2	12.2	-23.4
SNW#2_G02	10	5	12.4	-39.3	12.4	-21.5
SNW#2_O04	10	5	12.9	-40.1	12.5	-21.6
SNW#3_K06	10	5	12.1	-36.1	11.6	-23.9
SNW#3_M06	10	5	12.5	-36.4	12.2	-24.4
SNW#4_G13	15	5	12.2	-32.2	10.7	-20.6
SNW#4_M06	15	5	12.5	-36.4	10.8	-20.1
SNW#6_K06	10	5	11.7	-40.1	11.6	-22.2
SNW#6_M06	10	5	11.5	-41.1	11.3	-24.7
SNW#8_G13	15	5	11.5	-39.1	10.9	-21.1
SNW#8_K08	15	5	10.8	-35.6	10.8	-22.9
SNW#9_G02	15	5	11.7	-36.7	10.7	-19.1
SNW#11_J02	15	5	11.8	-33.3	10.9	-17.4
SNW#11_K08	15	5	11.8	-32.4	10.7	-16.7

Table 4.2: Measured resonance characteristics of resonators; Design-1 and Design-2.

Resonator	V_{PM} (V)	V_s (V_{pk})	$f_{Design-1}$ (kHz)	Gain (dB)	$f_{Design-2}$ (kHz)	Gain (dB)
SNW#1_C02	30	5	11.2	-32.2	11.1	-25.2
SNW#1_F11	30	5	11.8	-31.2	11.7	-25.6
SNW#2_C09	30	5	12.1	-33.3	11.8	-24.8
SNW#2_N09	30	5	11.5	-34.1	11.1	-25.1
SNW#3_F04	30	5	10.9	-32.1	10.7	-24.9
SNW#3_K04	30	5	12.5	-33.4	11.9	-25.1
SNW#4_C02	30	5	11.2	-31.6	10.7	-24.6
SNW#4_K11	30	5	12.5	-35.1	11.7	-24.8
SNW#6_F04	30	5	11.1	-32.3	10.8	-25.2
SNW#6_N02	30	5	11.2	-32.9	11.1	-24.9
SNW#8_C02	30	5	12.5	-31.7	11.9	-25.6
SNW#8_K04	30	5	10.9	-33.1	10.6	-25.4
SNW#9_F11	30	5	11.2	-32.7	10.6	-24.9
SNW#9_K04	30	5	11.9	-32.9	11.2	-25.5
SNW#11_C02	30	5	11.2	-32.9	10.7	-26.2
SNW#11_N09	30	5	12.1	-33.1	11.4 kHz	-26.1

4.1.2 Tests of Pirani Gauges

Compared to the resonating structures, the functionality test of pirani gauges is simple. The test setup consists of probe station and a multimeter. After fixing the wafer under the probe station, the resistances of the pirani gauges are measured using the multimeter. The measured resistances are then compared with the design values to evaluate the success of the process. Table 4.3 presents the resistance measurement results of pirani gauges Design-1, Design-2, and Design-3 from different sensor wafers.

Table 4.3: The measured resistances of Design-1, Design-2, and Design-3.

Pirani Gauge	$R_{Design-1}$ (kΩ)	$R_{Design-2}$ (kΩ)	$R_{Design-3}$ (kΩ)
SNW#1_C09	3.34	-	-
SNW#1_E10	-	2.71	3.62
SNW#2_N02	3.22	-	-
SNW#2_H11	-	2.79	3.59
SNW#3_K11	3.41	-	-
SNW#3_E03	-	2.75	3.64
SNW#5_F04	3.25	-	-
SNW#5_L10	-	2.82	3.62
SNW#6_N02	3.31	-	-
SNW#6_H04	-	2.76	3.65
SNW#10_C02	3.32	-	-
SNW#10_L03	-	2.81	3.67

4.2 Vacuum Tests

For the vacuum tests, the wafer has to be diced. The functional dies from the diced wafer are indentified during the functionality tests and passed for the vacuum test. These dies are placed inside a vacuum chamber and their response is observed at vacuum. The gyroscopes and resonators are characterized at different pressure levels and their quality factor versus pressure graph is extracted. Similarly, the thermal conductance versus pressure graph is extracted for pirani vacuum gauges. This section presents the vacuum tests of MEMS gyroscopes, resonators and pirani gauges, including the methods and test setups used.

4.2.1 Characterization of MEMS Gyroscopes and Resonators at Vacuum

The functional gyroscope and resonator dies are mounted on the hybrid package and electrical connection from sensor to the package is provided by wire bonding. The test is the same with the functionality test except the ambient pressure. In this test, the resonance characteristics of gyroscopes and resonators are examined at different

pressure levels. Figure 4.3 and Figure 4.4 presents the vacuum test setup used and the measured resonance characteristic of a resonator die at a pressure of 1.8 mTorr.

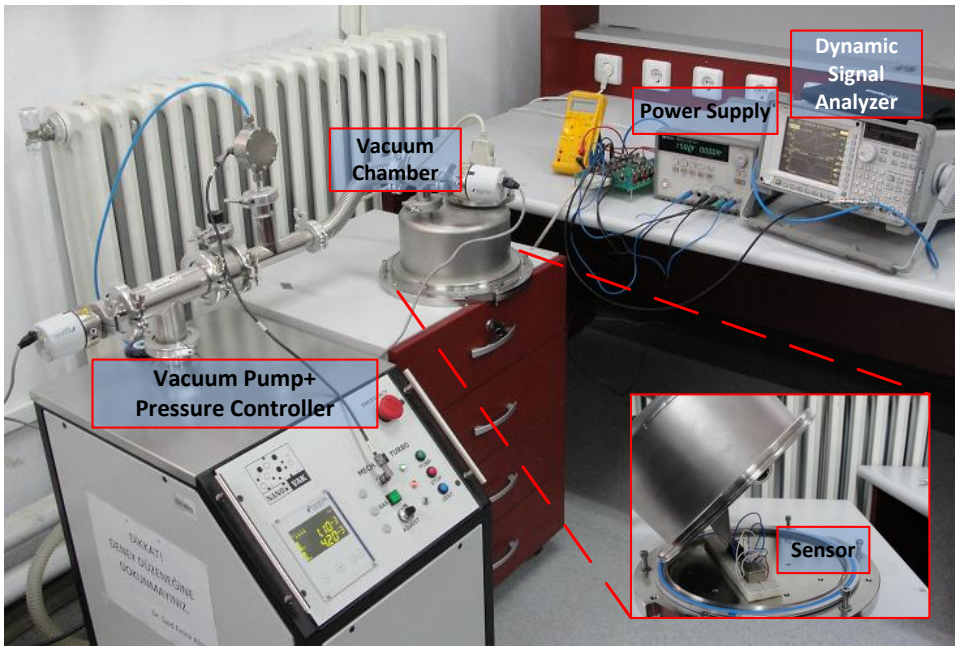


Figure 4.3: The vacuum test setup for gyroscopes and resonators.

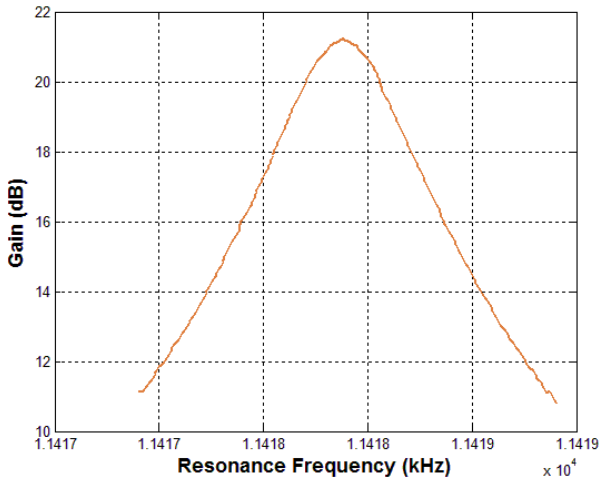


Figure 4.4: Measured resonance characteristic of the resonator Design-1 at 1.8mTorr.

The quality factor is inversely proportional to the pressure and changes when pressure changes. Therefore, by extracting the quality factor value at each pressure level, the vacuum response of the sensor is determined. Table 4.4 and Figure 4.5 presents the quality factor values of a resonator die at different pressure levels. This sensor can be used for measuring the pressure levels in the range of 1 mTorr-0.5Torr.

Table 4.4: The quality factor versus ambient pressure for a resonator die.

Pressure (mTorr)	Quality Factor	Pressure (mTorr)	Quality Factor
1.8	61715	90	15858
10	46601	100	14544
20	38700	125	12546
25	35130	150	10670
30	30446	175	9594
40	27184	200	8616
50	23541	250	7226
60	21341	300	6171
70	18872	400	4807
80	18300	500	3988
85	16915		

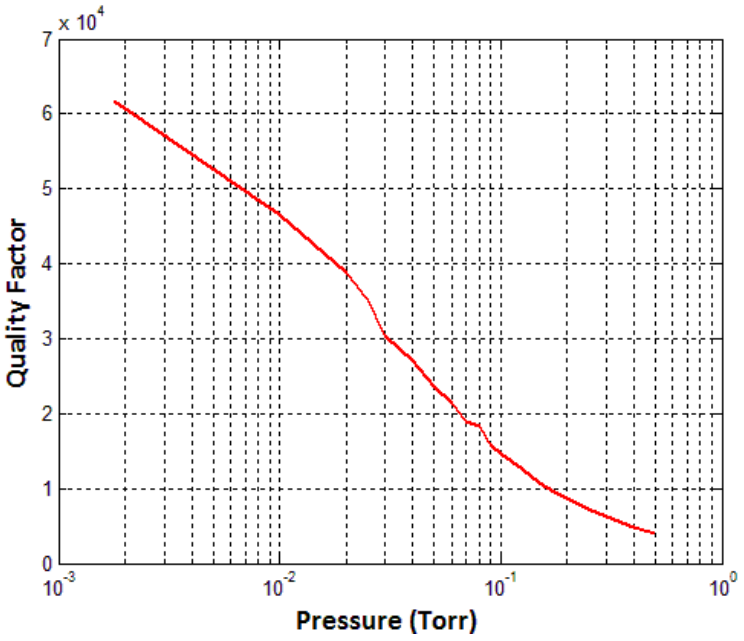


Figure 4.5: The quality factor versus ambient pressure for a resonator die.

The sensors passing from the same fabrication cycle has similar quality factor values and thus the performance of wafer level packages can be predicted using the vacuum test datas of these sensors.

4.2.2 Characterization of Pirani Gauges at Vacuum

The pirani gauge also needs a characterization before use. This characterization is carried out in a vacuum chamber and the response of the sensor at different pressure levels is observed. For that purpose, the functional pirani gauge die is mounted on the hybrid package, the electrical contacts to the package pins are taken by wire bonding and the sensor is placed into the vacuum chamber. In the test, a current is applied to the gauge by a current source and the voltage drop across the same terminals is measured by a multimeter. The average temperature change along the gauge is calculated using the Equation 2.10. The current is increased until the temperature reaches to a selected value, typically 50ºC. Then the power dissipation on the resistor is calculated using the Equation 4.1 where I is the applied current and P is the power on the resistor.

$$P = I^2 R \tag{4.1}$$

The temperature change versus power graph is drawn. The slope of this graph gives the thermal conductance. The pressure of the vacuum chamber can be adjusted by the pressure control unit and these procedures are repeated for different pressure levels. Table 4.5 Figure 4.6 Table 4.6, and Figure 4.7 present the characterization results of pirani gauge Design-1 and Design-2, respectively.

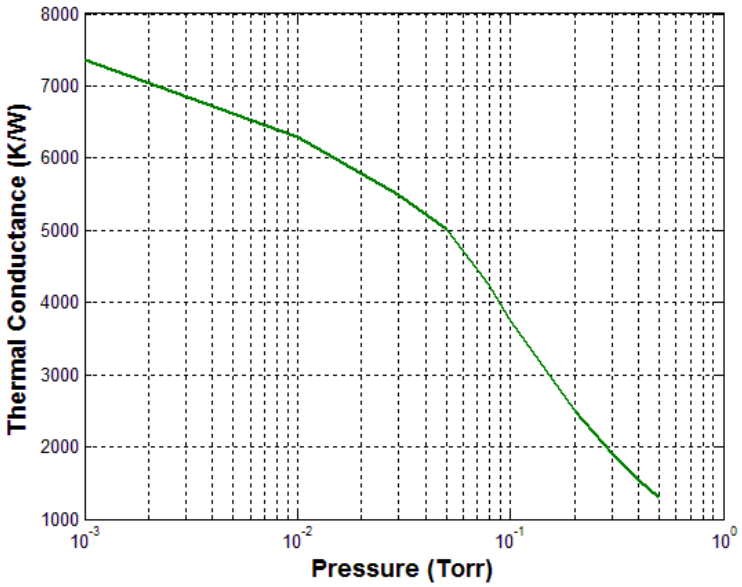


Figure 4.6: The vacuum response of the pirani gauge Design-1.

Table 4.5: Measured thermal conductance values at different pressure levels.

Pressure (mTorr)	Thermal Conductance (K/W)
1	7354
10	6302
30	5486
50	5014
80	4225
100	3752
200	2496
300	1915
400	1541
500	1304

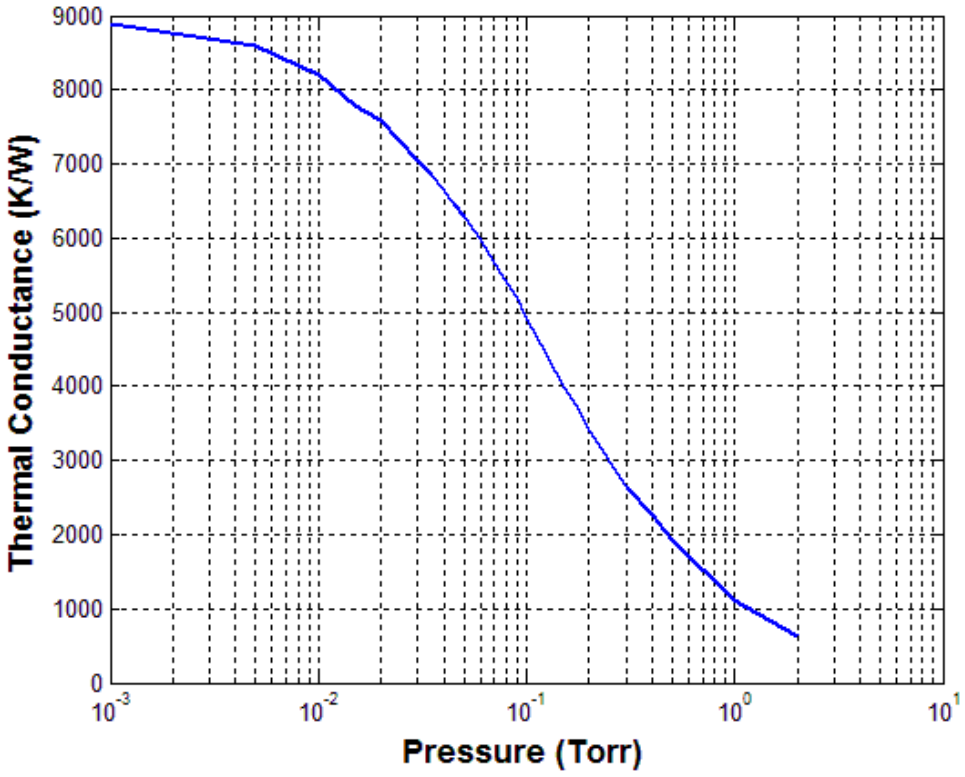


Figure 4.7: The vacuum response of the pirani gauge Design-2.

Table 4.6: Measured thermal conductance values at different pressure levels.

Pressure (mTorr)	Thermal Conductance (K/W)	Pressure (mTorr)	Thermal Conductance (K/W)
1	8894	80	5401
5	8599	90	5196
10	8198	100	4925
15	7782	125	4425
20	7601	150	4004
25	7294	175	3724
30	7044	200	3423
35	6860	300	2647
40	6645	400	2260
45	6462	500	1927
50	6286	1000	1118
60	5975	2000	632.2
70	5685		

4.3 Test of Wafer Level Vacuum Packages

This section presents the performance results of wafer level packages fabricated using Au-Si eutectic and glass frit bonding. The performance of wafer level vacuum packages is evaluated using the integrated gyroscopes, resonators and pirani vacuum gauges.

4.3.1 Wafer Level Vacuum Packages Sealed by Au-Si Eutectic Bonding

Totally, 4 wafer level vacuum packages are fabricated using Au-Si eutectic bonding. Table 4.7 summarizes the wafer level vacuum packaging processes on 4 sensor wafers. The sensor wafer 2 is broken during the packaging process and could not be tested. The metal feedthroughs of the sensor wafers 3 and 4 are damaged during the packaging process. Thus, no response could be taken from devices corresponding to

these wafers since the electrical connection is lost. The sensor wafer 9 is the first Au-Si eutectic wafer fabricated without any damage to the metal lines. The performance of sensor wafer 9 is tested using the integrated gyroscopes, resonators and pirani gauges. The test results show that the pressure inside the Au-Si wafer level packages is equal to the atmospheric pressure. To examine the bond quality, the cap wafer is pushed away by an external force. The cap and device wafers are easily separated from each other, which show the bond quality is very weak. Figure 4.8 presents the view of device and cap wafers after the decapping.

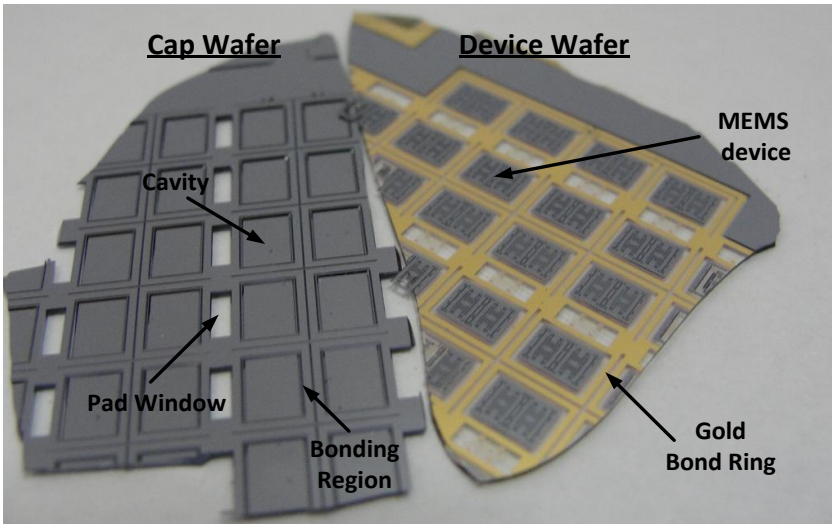


Figure 4.8: The device wafer can easily be separated from the silicon cap wafer, showing that wafer level vacuum packaging is unsuccessful.

The device wafer is then examined under SEM and undesired polymers residues on silicon areas are detected. This thin polymer layer is coated during the device release by RIE. Figure 4.9 presents the SEM photos of a gyroscope die.

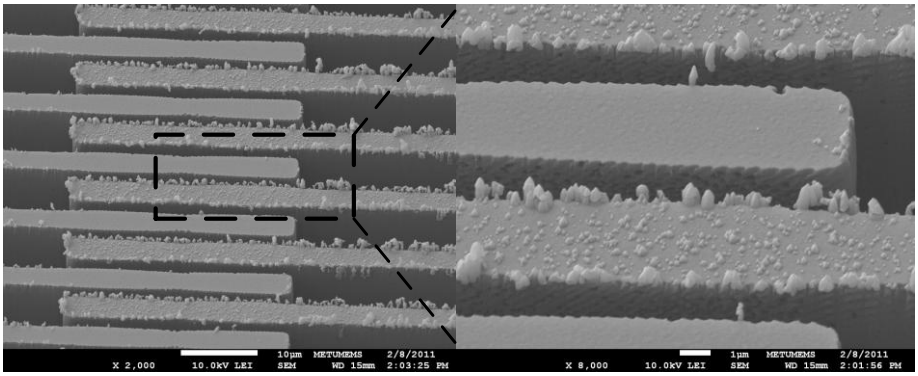


Figure 4.9: The polymer residues detected over the finger regions.

This thin polymer layer prevents the diffusion of gold and silicon necessary for the eutectic bonding. Thus, the vacuum packaging process is unsuccessful.

Table 4.7: The summary of wafer level vacuum packaging processes using Au-Si eutectic bonding.

# of SNW	Packaging Process	Comments
2	420ºC, 60 min	Wafers were broken during the bonding process.
3	420ºC, 60 min	Metal lines were damaged
4	420ºC, 30 min	Metal lines were damaged
9	420ºC, 60 min	Atmospheric pressure

4.3.2 Wafer Level Vacuum Packages Sealed by Glass Frit Bonding

This section presents the performance results of 4 wafer level vacuum packages fabricated by glass frit bonding (see Table 4.8). The metal feedthroughs of sensor wafer 1 are damaged during the wafer level vacuum packaging process and the electrical connection to the device is lost. Thus, no response from the devices could be taken. The sensor wafer 6 is tested and the pressure inside the packages is found as atmospheric pressure. The reason of atmospheric pressure inside the packages is the excessive proceeding of Au-Si eutectic from contact regions under the bonding line. Pressures ranging from 10 mTorr to 60 mTorr are measured in the glass frit packages of sensor wafer 7 and 0.1 Torr to 0.7 Torr are observed inside sensor wafers 10 and12. The pressure levels inside the sensor wafer 10 and 12 are higher than sensor wafer 7. This is due to the different outgassing rates of materials used during the fabrication. The metal lines of sensor wafer 7 are formed by evaporated Cr/Au while the metal lines of sensor wafer 10 and 12 are fabricated by sputtered Cr/Au. The sputtered Cr/Au includes high amount of Argon gas which getter is not able to absorb. Therefore, the outgasssed Argon during the packaging process increases the pressure levels inside the sensors wafers 10 and 12. Table 4.9, Table 4.10, Table 4.11, and Figure 4.10 present the performance measurements of glass frit packages.

Table 4.8: The summary of wafer level vacuum packaging processes using glass frit bonding.

SNW	Packaging Process	Comments
1	435ºC, 60 min	Metal lines were damaged.
6	435ºC, 60 min	Atmospheric pressure
7	435ºC, 10 min	Vacuum
10	435ºC, 60 min	Vacuum
12	435ºC, 10 min	Vacuum

Table 4.9: The performance glass frit packages (SNW#7).

Sensor	ID	Quality Factor	Pressure
Gyroscope	A-04	72148	35 mTorr
Gyroscope	H-08	89500	10 mTorr
Gyroscope	J-01	57024	60 mTorr
Gyroscope	J-14	77949	30 mTorr
Gyroscope	P-01	89548	10 mTorr

Table 4.10: The performance of glass frit packages (SNW#10).

Sensor	ID	Quality Factor/ Thermal Conductance	Pressure
Gyroscope	A-04	17225	0.2 Torr
Resonator/ P.Gauge	C-02	12251/1654	0.3 Torr
Gyroscope	M-06	6050	0.6 Torr
Gyroscope	M-12	5728	0.6 Torr
Resonator	N-04	9874	0.4 Torr
Gyroscope	P-04	8771	0.5 Torr

Table 4.11: The performance glass frit packages (SNW#12).

Sensor	ID	Quality Factor/ Thermal Conductance	Pressure
Gyroscope	A-01	9797	0.2 Torr
Resonator	C-02	14521	0.3 Torr
P. Gauge	C-09	1412	0.4 Torr
Gyroscope	G-07	6050	0.7 Torr
Gyroscope	I-01	15138	0.3 Torr
Gyroscope	I-07	21378	0.2 Torr
Gyroscope	I-08	11000	0.4 Torr
Gyroscope	J-14	24528	0.1 Torr
Resonator/P.Gauge	N-09	15214/1621	0.3 Torr/0.2 Torr

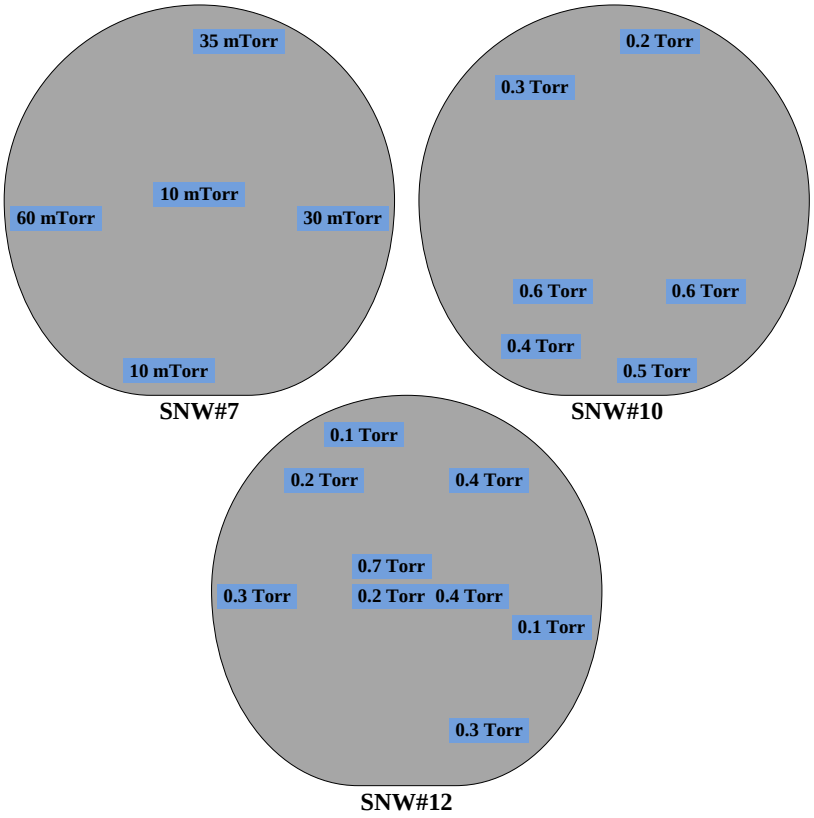


Figure 4.10: The measured pressure distribution over the sensor wafers 7, 10, and 12 that are wafer level vacuum packaged using glass frit bonding.

4.4 Summary of the Chapter

This chapter presents the test results of the fabricated gyroscopes, resonators and pirani vacuum gauges before and after the vacuum packaging process. The chapter starts with the functionality tests of these devices under atmospheric environment. While a simple resistance measurement is performed for pirani gauges, the resonance characteristics of gyroscopes and resonators are observed. The working sensors are then placed in the vacuum chamber and their response is observed at different vacuum levels. Quality factor versus pressure graphs for resonating structures and the thermal impedance versus pressure graphs for pirani gauges are extracted. The performance of wafer level vacuum packages fabricated using Au-Si eutectic and glass frit bonding is evaluated using the integrated sensors. While different vacuum levels are measured inside the glass frit packages, no vacuum data can be obtained using Au-Si eutectic bonding. The reason of atmospheric pressure inside the Au-Si wafer level packages is related with the device release in RIE. The thin polymer layer coated during the device release in RIE prevents the diffusion of gold and silicon necessary for the eutectic bonding.

CHAPTER 5

CONCLUSION AND FUTURE WORK

This work presents the development of wafer level vacuum packaging processes for MEMS devices using Au-Si eutectic and glass frit bonding. In the first phase of this research, MEMS resonators and pirani vacuum gauges are designed for the evaluation of the package performance. A new version of Silicon-On-Glass (SOG) process is developed for the fabrication of resonators and pirani gauges designed in this study and the gyroscopes previously developed at METU with lateral feedthroughs. The potential damage of the low stress silicon nitride passivation layer during the device release is minimized by using RIE instead of BHF. A separate study on the fabrication of similar devices with vertical feedthroughs is also initiated. However, the fabrication of these devices could not be completed due to the manufacturing problems from the wafer supplier in the fabrication of glass wafers with highly doped silicon vias. Furthermore, cap wafers for both types of devices with lateral and vertical feedthroughs are designed and fabricated. The fabricated devices are wafer level vacuum packaged using these cap wafers by Au-Si eutectic and glass frit bonding. The main problem faced during the wafer level vacuum packaging process is the degradation of gold feedthrough lines. Since the high temperature used for the packaging process exceeds the eutectic point of Au-Si, the regions where gold device metallization contacts the silicon device layer is damaged and the electrical connection to the device is lost. This problem is solved by increasing the period of the cooling step of wafer bonding and the robustness of the contacts. The performance of the wafer level vacuum packages is evaluated using the integrated gyroscopes, resonators and pirani vacuum gauges. While different vacuum levels are detected inside the glass frit packages, no vacuum data can be obtained using Au-Si eutectic bonding. The reason of atmospheric pressure

inside the Au-Si wafer level packages is related with the device release in RIE. The thin polymer layer coated during the device release in RIE prevents the diffusion of gold and silicon necessary for the eutectic bonding.

Based on the accomplishments and results of this research following conclusions can be done:

1. Design of MEMS resonators and pirani vacuum gauges is completed. Two different resonators are developed and these designs are verified by FEM simulations in Coventorware. The simulation results are compared with the hand calculations and desired modifications are done. The effect of design parameters on the performance of pirani vacuum gauges is investigated and modeled in MATLAB. Furthermore, thermal analysis of pirani gauges is carried out in Coventorware. Three different pirani gauge structures which are capable of measuring the pressures in the range of 10mTorr-5Torr are designed.
2. Optimization of Au-Si eutectic bonding is completed. A series of Au-Si bond experiments are carried out on both planar and non-planar surfaces. The bond quality is evaluated using deflection test. The principle of this test is the deflection of a thinned diaphragm due to the pressure difference between inside and outside of the package. Therefore, the wafers subjected to the deflection test are thinned and in the case of vacuum inside the package, the thinned packaging material is deflected to downwards. A 100% yield Au-Si eutectic bond on planar surfaces is obtained at 390ºC with a holding time and bond force of 60 min and 1500N. The higher bond temperatures and forces are also tested and lateral eutectic flow on the device area is observed. On the other hand, Au-Si eutectic bond on a surface where 0.15 µm thick lateral feedthroughs exist could be obtained only at 420ºC with a bond force of 1500N. The yield of the process is also %100. The wafers could not be bonded at temperatures lower than 420ºC even under the application of electrostatic bond forces.
3. Optimization of glass frit bonding is carried out. The first optimization is performed between the silicon cap and glass wafers with lateral feedthroughs and the bond quality is evaluated by optical inspection. A bond yield of

%99.4 is obtained at 450ºC with hold time and bond force of 60 min and 1500N, respectively. The lower temperatures and holding periods are also tested and it is experimentally verified that the yield decrease from %99.4 to %33 with the decreased bond temperatures and hold periods. The main problem during the glass frit bonding is the damage of gold feedthroughs. The glass frit and gold have an interaction at high temperatures and gold loses its conductivity. This problem is solved by using a silicon nitride protection layer between the gold and glass frit. Glass frit bonding on gold, silicon and silicon nitride surfaces are also investigated. The bond quality is evaluated using the deflection test. The same results with the bonding on glass wafers are obtained and it is experimentally verified that a high quality glass frit bond can be done even on all type of materials.

4. A new version of SOG process is developed for the fabrication of MEMS gyroscopes, resonators, and pirani vacuum gauges with lateral feedthroughs. This process is based on the use of silicon device layer of SOI wafers and suitable with Au-Si eutectic and glass frit bonding. The main problem faced during this process is the removal of buried oxide layer of SOI wafer which is necessary for the device release. The underlying silicon nitride passivation layer should be protected during the release. However, the low stress PECVD silicon nitride is completely etched during the device release in BHF. This problem is solved by the replace of BHF by RIE. The silicon nitride is successfully protected during the release performed by RIE.
5. A study on the fabrication of MEMS gyroscopes, resonators, and pirani gauges with vertical feedthroughs is done. For that purpose, a process based on the use of glass wafers with highly doped silicon vias is developed. The company, Plan Optik, is selected for the fabrication of these glass wafers and a layout is drawn according to their design rules and sent to this company. The fabrication of glass wafers with highly doped silicon vias is based on the glass reflow process in which a glass wafer is anodically bonded to a silicon wafer patterned using DRIE. In the case of heating above the melting point of the glass, the glass melts and flows through the silicon due to the pressure difference and fills the empty spaces in the silicon. The company faced with some problems during the fabrication and suggested a layout modification.

In the new layout, a large amount of glass is replaced with dummy silicon vias, especially dicing streets and outer region of the wafer. This layout sent to Plan Optik. The fabrication of the glass wafers with silicon vias is still in progress and left as future work.

6. Cap wafers for devices with lateral and vertical feedthroughs are designed and fabricated. The cap wafer design for lateral feedthroughs is more complex since there is a need for reaching the feedthroughs for testability. Thus, there should be pad windows on the cap wafer and this makes the fabrication difficult. The fabrication of these wafers is performed with two stepped KOH process. In the first step, backside of the cap wafer is etched to 280 μm while protecting the front side with thermal oxide. The second step involves a double side etch in KOH where some parts of wafers are drilled for pad windows and 120 μm depth cavities are formed at the device regions. On the other hand, fabrication of cap wafers for vertical feedthroughs consist of one process step, in which a cavity is formed using DRIE/KOH or HF according to the type of the cap wafer. The fabricated cap wafers are then sent to the company, Nanogetters^{TM}, for glass frit and getter deposition according to the requirements of wafer bonding process.
7. The fabricated gyroscopes, resonators, and pirani gauges are subjected to the functionality tests under atmospheric conditions to identify the working sensors. A simple resistance measurement is sufficient for pirani gauges, whereas the resonance characteristics of MEMS gyroscopes and resonators have to be observed. The working sensors are tested at different vacuum levels for the identification of their vacuum response. The gyroscopes and resonators are characterized at different pressure levels and their quality factor versus pressure graph is extracted. Similarly, the thermal conductance versus pressure graph is extracted for pirani vacuum gauges.
8. The fabricated devices are wafer level vacuum packaged using Au-Si eutectic bonding and glass frit bonding. The main problem in this step is the damage of device metallization during the wafer level vacuum packaging process. The high bonding temperatures used for the packaging process damages the device metallization due to the Au-Si eutectic formation between the silicon structural layer and gold feedthroughs. This problem is minimized by

extending the period of cooling step in the bonding recipe and using the native oxide on silicon as a barrier between the silicon and gold.

9. The performance of wafer level vacuum packages is evaluated using the integrated gyroscopes, resonators and pirani vacuum gauges. Pressures ranging from 10 mTorr to 60 mTorr in the glass frit packages of SNW#7 and 0.1 Torr to 0.7 Torr inside SNW#10 and12 are observed. The pressure levels inside SNW#10 and SNW#12 are higher than SNW#7 even the use of getter. This may be due to the high outgassing rate of some materials, especially Argon coming from sputtered device metallization, which getter is not able to absorb. For wafer level vacuum packaging using Au-Si eutectic bonding, no vacuum data has been obtained and the pressure inside the package is equal to the atmosphere. After these tests, Au-Si wafer level package is examined and confirmed that the Au-Si bonding is not successful. This may be due to the polymer coated during the device release in RIE. The RIE polymer behaves as a barrier between the gold bond ring and silicon cap wafer and prevents the diffusion necessary for Au-Si eutectic bonding.

The main conclusion of this study can be summarized as; wafer level vacuum packaging is essential part of the MEMS devices for their integration in the market. It not only reduces the cost of packaging process, but also brings the advantages of protection of dies during handling, testing and storage. The aim of this research is to present wafer level vacuum packaging processes contributing to the improvement of MEMS devices developed at METU. To further increase the performance and reliability some of the future research topics can be listed as follows:

1. The silicon nitride deposition should be optimized. A silicon nitride which has higher BHF selectivity should be developed to get rid of RIE. Thin film polymer layer coated during the device release by RIE prevents the silicon-gold diffusion necessary for Au-Si eutectic bonding. Thus, wafer level vacuum packaging with Au-Si eutectic bonding could not be achieved. In the case of having a higher BHF selective silicon nitride, the device release could be carried out in BHF. Therefore, the BHF selectivity of silicon nitride should be increased by changing the deposition conditions. One way to do

this is increasing the ratio of SiH_4. In this case, silicon nitride will be more robust to BHF and the buried oxide of SOI wafer will be removed in BHF without completely etching the silicon nitride. This will solve the problem faced during the wafer level vacuum packaging using Au-Si eutectic bonding.

2. The gold device metallization can be replaced with aluminum. The Al-Si eutectic reaction occurs at 577ºC, which is higher than the temperatures used for the wafer level vacuum packaging process. Therefore, no damage will be observed in the aluminum feedthroughs during the wafer level vacuum packaging. Besides, aluminum does not interact with glass frit and thus, the need of protection layer will be eliminated.
3. Another way of solving the degradation at the silicon-gold contact regions is the use of localized heating. Localized heating provides a wafer bonding process in which only the regions that will be bonded is heated. Thus, the device area and contact regions will not be subjected to the high temperatures during the wafer level vacuum packaging.
4. The fabrication of devices with vertical feedthroughs should be completed. After receiving the glass wafers with silicon vias fabricated according to the modified layout, the fabrication of devices will be initiated. The process steps are easier than the process used for the fabrication of devices with vertical feedthroughs and so that the fabrication will be finalized without any problems. The devices should be characterized and if desired performance is obtained, the wafer level vacuum packaging will be done. Since the packaging will be carried out on planar surfaces, lower bonding temperatures should be used which reduces the risk of degradation in contact regions. After the packaging process, the performance of packages should be evaluated using integrated sensors. Besides, long term tests should be done to predict the life time performance of the fabricated devices.
5. For the reliability of glass frit packages, the long term tests should be maintained. This is an essential step to predict the life time performance. The period of these tests could be shortened by replacing them with the accelerated performance tests defined in the literature.

In conclusion, in the scope of this study wafer level vacuum packaging processes using Au-Si eutectic and glass frit bonding is developed. While packaging by glass frit bonding is successfully fabricated, packaging with Au-Si eutectic bonding is under development. The Au-Si eutectic bonding is a promising method for wafer level vacuum packing of MEMS devices and expected to replace the glass frit packages in the future.

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