TOLERANCE BASED RELIABILITY ANALYSIS OF AN ANALOG ELECTRIC CIRCUIT

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

SİNAN ÇAKIR

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
OPERATIONAL RESEARCH

JANUARY 2011

Approval of the thesis:

TOLERANCE BASED RELIABILITY ANALYSIS OF AN ANALOG ELECTRIC CIRCUIT

submitted by **SİNAN ÇAKIR** in partial fulfillment of the requirements for the degree of **Master of Science in Operational Research Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen _____
Dean, Graduate School of **Natural and Applied Sciences**

Prof. Dr. Çağlar Güven _____
Head of Department, **Operational Research**

Assoc. Prof. Dr. Yasemin Serin _____
Supervisor, **Industrial Engineering Dept., METU**

Examining Committee Members:

Assoc. Prof. Dr. Canan Sepil _____
Industrial Engineering Dept., METU

Assoc. Prof. Dr. Yasemin Serin _____
Industrial Engineering Dept., METU

Prof. Dr. Meral Azizoğlu _____
Industrial Engineering Dept., METU

Asst. Prof. Dr. Sedef Meral _____
Industrial Engineering Dept., METU

Alper Ünver, M.Sc. _____
Chief Researcher, TÜBİTAK-SAGE

Date: _____

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last Name: Sinan Çakır

Signature :

ABSTRACT

TOLERANCE BASED RELIABILITY ANALYSIS OF AN ANALOG ELECTRIC CIRCUIT

Çakır, Sinan
M.Sc., Department of Operational Research
Supervisor: Assoc. Prof. Dr. Yasemin Serin

January 2011, 82 pages

This thesis deals with the reliability analysis of a fuel pump driver circuit (FPDC), which regulates the amount of fuel pumped to a turbojet engine. Reliability analysis in such critical circuits has great importance since unexpected failures may cause serious financial loss and even human death.

In this study, two types of reliability analysis are used: "Worst Case Circuit Tolerance Analysis" (WCCTA) and "Failure Modes and Effects Analysis" (FMEA). WCCTA involves the analysis of the circuit operation under varying parameters in their tolerance bands. These parameters include the resistances of the resistors, operating temperature and voltage input value. The operation of FPDC is checked and the most critical parameters are determined in the worst case conditions. While performing WCCTA, a method that guarantees the exact worst case conditions is used rather than probabilistic methods like Monte Carlo analysis. The results showed that the parameter variations do not affect the circuit operation

unfavorably; operating temperature, voltage input variation and tolerance bands for the resistances are fairly compatible with the circuit operation.

FMEA is implemented according to the short circuit and open circuit failures of all the electronic components used in FPDC. The components whose failure has catastrophic effect on the circuit operation have been determined and some preventive actions have been offered for some catastrophic failures.

Keywords: Reliability, Worst Case Circuit Analysis, Failure Modes and Effects Analysis, Analog Circuit Analysis, Tolerance Analysis

ÖZ

BİR ANALOG ELEKTRİK DEVRESİNİN TOLERANS TABANLI GÜVENİLİRLİK ANALİZİ

Çakır, Sinan
Yüksek Lisans, Yöneylem Araştırması Bölümü
Tez Yöneticisi: Doç. Dr. Yasemin Serin

Ocak 2011, 82 sayfa

Bu tezde bir yakıt pompası sürücü devresinin güvenilirlik analizi gerçekleştirilmiştir. Bu devre, bir turbojet motora yeterli miktarda yakıt pompalanmasından sorumludur ve kritik bir öneme sahiptir. Bu türde kritik öneme sahip devrelerde oluşabilecek beklenmedik hatalar ciddi maddi hasara ve hatta ölümlere sebep verebileceği için güvenilirlik analizi büyük önem taşımaktadır.

Bu çalışmada, iki tür güvenilirlik analizi gerçekleştirilmiştir: "En Kötü Durum Devre Tolerans Analizi" (EKDDTA) ve "Hata Türü ve Etkileri Analizi" (HTEA). EKDDTA ile temel olarak, değişkenler tolerans aralıkları içerisinde değerler alırken devrenin analizi gerçekleştirilmektedir. Yakıt pompası sürücü devresindeki karar değişkenleri, direnç değerleri, devrenin çalışma sıcaklığı ve girdideki voltaj seviyesidir. En kötü durumda devrenin işlevselliği kontrol edilerek en kritik öneme sahip devre elemanları belirlenmiştir. EKDDTA gerçekleştirilirken Monte Carlo analizi gibi rassal yöntemler yerine en kötü duruma kesin olarak ulaşmayı sağlayan bir yöntem kullanılmıştır. Yapılan analizler sonucunda, değişkenlerin tolerans

aralıkları içerisinde aldıkları değerler devrenin işleyişini istenmeyen şekilde etkilemediği; devrenin çalışma sıcaklığı, girdi voltajı aralığı ve dirençlerin tolerans aralığının devrenin işleyişi ile uyumlu olduğu gözlenmiştir.

HTEA ise, devredeki elemanların kısa devre ve açık devre hatalarına uğradıkları durumda devrenin analizinin incelenmesi yoluyla gerçekleştirilmiştir. Yıkıcı etkiye sebep olacak parça hataları belirlenmiş ve bu hatalardan uygun olanları için engellemeye yönelik önleyici faaliyetler önerilmiştir.

Anahtar Kelimeler: Güvenilirlik, En Kötü Durum Devre Analizi, Hata Türü ve Etkileri Analizi, Analog Devre Analizi, Tolerans Analizi

To Ayşegül

and My Family

ACKNOWLEDGMENTS

This thesis work has been completed with the help and support of a considerable number of people. It is a pleasure for me to have the opportunity to acknowledge their help and support here. I apologize and express my gratitude to the ones whose names have not been mentioned in this limited space.

First and foremost, I would like to express my sincere gratitude to Dr. Yasemin Serin for all her valuable efforts in every step of this thesis. Her encouragement, support and patience always guided me throughout this period.

My last two years as a research engineer at TÜBİTAK-SAGE have shaped up my area of interest and my personality. During these two years, I have had the opportunity to work in a nice environment, which I am greatly indebted to the staff of the institute and improved myself in many various disciplines. Above all, I have most felt the encouragement and support of my senior colleagues: Alper Ünver and Kenan Bozkaya, who have witnessed my thesis work from the beginning and have been very helpful with their experience and knowledge about the topic. I feel very lucky to share the same office and work together with them.

This thesis would never be complete without the reviews and comments of the examining committee, Dr. Canan Sepil, Dr. Meral Azizoğlu and Dr. Sedef Meral. I appreciate the valuable feedback I have received from them.

I am also grateful to Murat Tunç for all his efforts to explain all the details of the circuit handled in this study and Ali Karakoç for his valuable aids on the computational part. Also I would like to thank Melih Çelik for all his supports that he gave to me, being a new student in the department.

I also thank the other residents of 20/15, Şafak Bayram and Kutay Erbayat for providing me a warm and sincere home environment. Kutay deserves an extra gratitude for creating a competitive atmosphere and encouraging me to complete this study just in time.

My family deserves special mention for their everlasting support. I am very grateful for their trust, understanding and patience.

Last and the most, I would like to express my gratitude to Ayşegül Yılmaz, who was beside me in the whole period. During my study, my dear Ayşegül never got tired of encouraging me and I always felt her great support on me. I am extraordinary fortunate for having her love, patience and confidence.

TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

CHAPTER 1

INTRODUCTION

In today's competitive world, reliability is a very important concept in electric circuits, which may be considered as the brain of many technological devices. There are many factors that affect the reliability of a circuit. Also there is a list of issues like cost, logistics, usability etc. required to be considered while keeping the reliability at high levels. However, ensuring a high reliability must be the primary concern in the circuits that have critical tasks. Therefore, reliability analysis should be performed on all circuitry that is safety critical. Most effective actions to make a circuit more reliable are taken in the design phase by following the advised procedures and performing various reliability analyses. There are many reliability analysis methods, like worst case circuit tolerance analysis, failure modes and effects analysis, fault tree analysis, reliability allocation and prediction. In this study, worst case circuit tolerance analysis and failure modes and effects analysis of a fuel pump driver circuit will be performed. This circuit has a very critical mission, which is supplying the required amount of fuel to a turbojet engine. In case of a failure; the air vehicle, whose thrust is created by the amount of the fuel pumped, is subject to fall.

Worst case circuit analysis takes the component variability into consideration and investigates the circuit operation under the worst case conditions, which consists of most extreme environmental and operating conditions. Temperature, radiation and humidity can be considered as the most effective environmental factors and the worst case operating conditions are usually formed by the external electrical inputs.

Failure modes and effect analysis is another important analysis method used in circuit reliability analysis. In this analysis, the failure mechanisms of the components and their effects on the circuit operation are examined. With this analysis, it is aimed to design robust circuits, which can even withstand failures of some components in the circuit.

Both worst case circuit analysis and failure modes and effects analysis must be performed in the design phase to take the necessary actions at the right time. Several actions, like modifying the circuit design, adding new components or changing the components used in the circuit, can be taken to make a circuit more reliable. In the design phase, the designer has more flexibility and the modifications will not increase the cost significantly. However, if the reliability analyses are skipped in the design phase and a major defect is realized after the manufacturing phase, it will have a huge effect on the cost of the project and surely the customer satisfaction will decrease. Catastrophic failures may even cost a human's life.

Hereafter, review on the worst case circuit tolerance analysis and failure modes and effects analysis, both of which are applied to the fuel pump driver circuit, will be given. Furthermore, brief information about the fault tree analysis, reliability allocation and prediction will be supplied.

1.1. Review of Worst Case Circuit Tolerance Analysis

Worst case circuit tolerance analysis is performed under the toughest environmental and operating conditions, while the component variables take value in their tolerance bands. However, finding the worst case conditions is the challenging part of this analysis. There are various methods generated for this purpose and these methods will be described below.

Worst case circuit analysis can be performed in time and frequency domain depending on the operation of the circuit under consideration. Actually, in which domain the circuit is to be analyzed in is determined by the circuit itself.

The analyses performed in time domain can be classified in two topics: Transient analyses, which focuses on the circuit timing during the transitions and the steady

state analyses, which investigate the circuit operation after all the transients are finished.

If the worst case is analyzed in frequency domain, time is not considered and the circuit operation is analyzed under various frequencies. Not whole of the electronic circuits can be analyzed in frequency domain, since the signal that runs through the circuit must be oscillating with a frequency for the circuit to be analyzed in frequency domain. However, this is not the case in all the circuits.

Most common method for the worst case circuit analysis is the well-known Monte Carlo method. Monte Carlo method is a stochastic method and used frequently in SPICE (Simulation Program with Integrated Circuit Emphasis) programs, which simulate the circuit operation depending on the simulation models of the components used in the circuit. However, it is not guaranteed to reach the worst case conditions in the circuit with this method due to its probabilistic nature. To approach the worst case conditions, performing very large numbers of Monte Carlo simulation may be required.

"Tolerance Design of Electronic Circuits" composed by Spence and Soin [7] is a very good reference for understanding tolerance based circuit design and analysis. In this book, the authors started with presenting general concepts and representations for tolerance design and analysis. They supplied an overview of tolerance design for various circuit types and explained Monte Carlo tolerance analysis method with supportive examples. Finally, they gave suggestions for circuit performance calculations and dealt with the use of sensitivity analysis.

"Worst Case Circuit Analysis Application Guidelines" published by Reliability Information Analysis Center (RIAC) [16] is as well a good reference particularly for the worst case circuit tolerance analysis. In this document, worst case circuit analysis techniques and methods are reviewed and the worst case analyses of an analog circuit and a digital circuit have been performed. The analysis of the analog circuit has been made with three different methods: Extreme value analysis, root-sum-squared analysis, Monte Carlo analysis and the results obtained with each method are compared, in order to observe their successes in determining circuit

performance. In digital circuit analysis, worst case analysis is based on the timing parameters and required delay times in the circuit. Extreme value analysis, which is the only applicable method in this case, has been used for the analysis.

In the literature, there are a number of studies, in which the worst case analyses of various circuits are performed. Most outstanding studies can be listed as follows: Tian and Shi [8] and Dreyer [1] performed the worst case analyses of electronic circuits in frequency domain while generating new algorithms to reach the worst case conditions. Likewise, Femia and Spagnuolo [2] and Tian and Ling [9] investigated the operations of various circuits in time domain. Kolev [4] generated a method to reach the exact worst case solution in the time domain. However, the majority of the studies in the worst case circuit analysis concentrate on the frequency domain analysis since it is fairly easier and is a more applicable analysis method.

The earliest studies that could be found about the effect of the components' tolerance on the circuit performance are White's papers: "Introduction to Six Sigma with a Design Example" [11] and its continuation study, "Component Tolerance and Circuit Performance: A Case Study" [12] . In these studies, main aim is to reach six sigma quality by choosing electronic components with adequate tolerance bands. In these studies, a simple overcurrent detector circuit has been analyzed and Monte Carlo simulation method has been used. White used uniform distribution for the components' tolerances in [11], then he repeated the same study in [12] with normal distribution. White has approached the problem with a statistical point of view and constituted the following distributions as shown in Figure 1.1 and Figure 1.2.

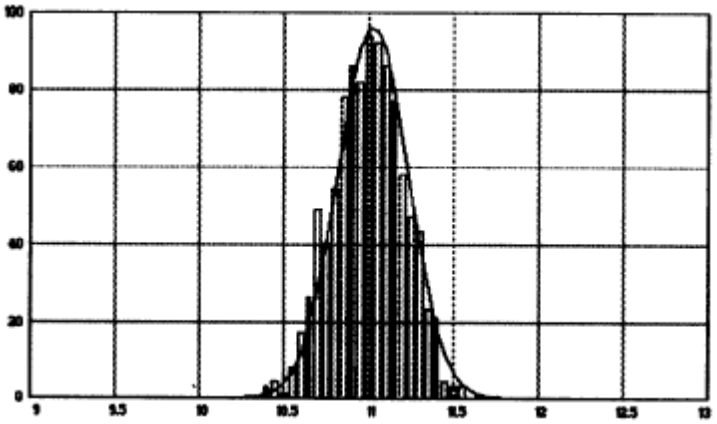

Figure 1.1. Distribution & Histogram of Overcurrent Circuit Output for Normal Tolerance Parts [12]

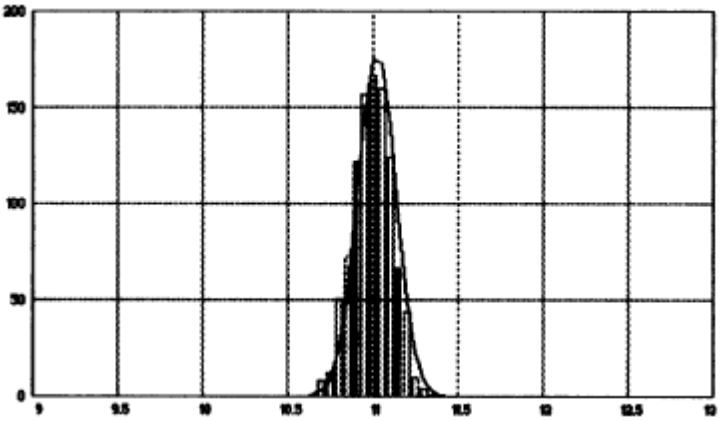

Figure 1.2. Distribution & Histogram of Overcurrent Circuit Output for Tight Tolerance Parts [12]

Figure 1.1 and Figure 1.2 shows the effect of normal and tight tolerances on the circuit performance. In his paper, White also compared the results obtained for normally distributed components values with the uniformly distributed components in [12] and concluded that more realistic results are obtained with normally distributed tolerances.

In 1996, Tian and Ling [9] have improved two complementary algorithms: Analytical and accurate algorithms to obtain the worst case solutions. While the analytical algorithm is faster than the accurate algorithm, it comprises more interval expansion error. They applied their algorithms both in time domain and frequency

domain and compared the results obtained with the analytical and accurate algorithms.

Tian and Shi [8] took various circuits in their study and made their analyses in frequency domain. They defined the monotonicity concept and performed their worst case analysis checking the monotonicity condition of the relevant function. According to Tian and Shi, a function is monotonic if this function is monotonically decreasing or increasing due to the changes in the parameter space, where the parameters are defined in an interval. After the specified algorithms are run, the sensitivities of the voltage or current levels according to the components in the circuit are drawn in frequency domain. Figure 1.3 shows the sensitivity of voltage, V(2) versus circuit parameter R over the parameter space.

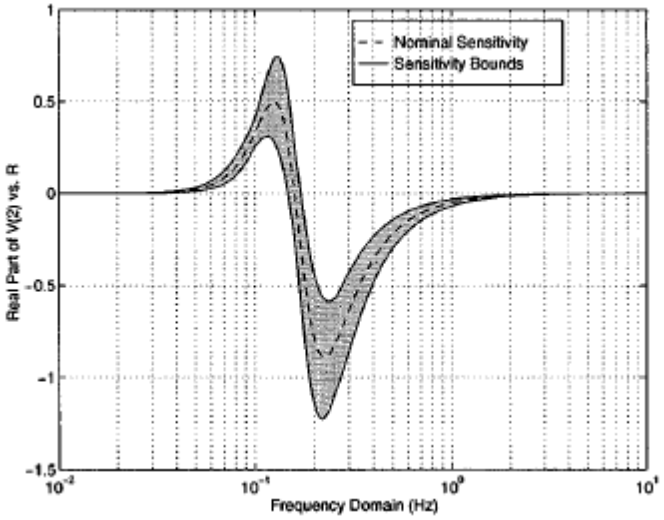

Figure 1.3. Sensitivity over Various Frequency Levels [8]

Dreyer [1] focused on the worst case analysis of integrated circuits and performed his analyses with successive application of the interval-valued Sherman-Morrison formula. In his study, he dealt with an operational amplifier, which includes several transistors and resistors inside. However, he simplified the circuit scheme by using the small-circuit equivalent schematics for the transistors and supplied the sensitivity analysis result in frequency domain like Tian and Shi [8].

Kolev [4] generated a method to reach the exact worst case solution. While reaching the exact solution, inner and outer solutions are found first and the exact

solution is determined if the certain monotonicity conditions are fulfilled. He applied his methods to a notch filter circuit. Although this circuit can be analyzed in frequency domain, he has chosen to analyze it in time domain. By fixing the operating frequency of the circuit, the transient analysis is performed according to the methods he generated.

Femia and Spagnuolo [2] also performed analyses in time domain, however with fairly different methodology. Like Kolev, they also aimed to reach the exact or with their words, 'true' worst case conditions with a new approach. Their method is based on the joint usage of genetic algorithms and affine arithmetic. They offered the usage of genetic algorithms to reach the inner solution and minimize the underestimation error obtained in stochastic methods. Likewise, affine arithmetic is used to reach the outer solution and minimize the overestimation errors obtained with the interval arithmetic methods. They performed the transient analyses of various circuits and compared their results with the Monte-Carlo analysis results. In Figure 1.4, step response of the inductor L_x is given with comparison of the genetic algorithm and Monte-Carlo analysis with 100 trials. Where the lower bound results are found the same in three of the analyses, GA generation #100 showed that Monte-Carlo analysis results can misguide.

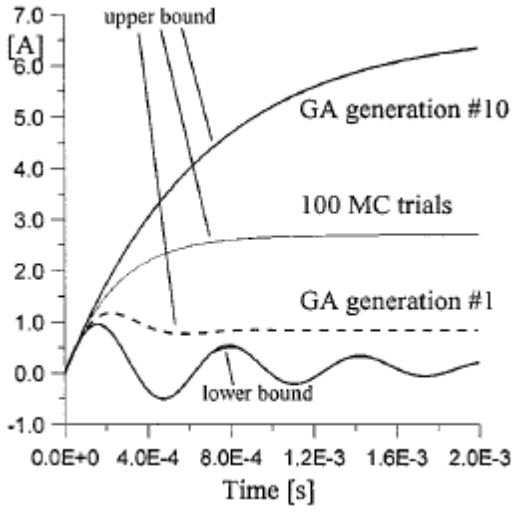

Figure 1.4. Step Response of the Inductor L_x [2]

In this thesis, the exact or true worst case conditions are aimed and instead of using Monte Carlo simulation method, a deterministic optimization model that ensures to reach the worst case is constructed. This model is solved using MATLAB and ModeFRONTIER softwares. The worst case circuit tolerance analysis is performed according to:

- Resistance variations within the tolerance bands

- Operating temperature interval of the circuit (environmental condition)

- Voltage input variations (operating condition)

In the reliability analysis of the fuel pump driver circuit, the operating region of the transistors are taken as base and the effects of component variability, temperature and the voltage input are assessed by checking the operating regions of the transistors if they remain in their desired regions. In the literature, no study that considers the operating regions of the transistors and performs the reliability analyses according to these conditions has been found to our best knowledge. Dreyer [1] and Tien and Ling [9] performed the worst case analysis of circuits that include transistors in their scheme. However, in their analyses they used the small signal models for the transistors, which simulate the operation of the transistors only while they are operating in small currents.

1.2. Review of the Failure Modes and Effects Analysis

Failure modes and effect analysis is another important concept in circuit reliability analysis. By applying this method, it is aimed to examine the effects of the components' failures in the circuit. Each component has different failure modes with different probabilities. Most common failure modes can be listed as follows:

- Open circuit
- Short circuit
- Part-parameter shift
- Dielectric breakdown
- Wear

This analysis method is well defined in U.S. military document MIL-HDBK-338B [13] and the failure distributions for each part are given in FMD-97 document [15]. These two documents constitute a base for FMEA and are taken into consideration in the FMEA studies done in this thesis. Depending on the FMEA results, the weak parts of the circuit in issue have been determined and some modifications to minimize the number of catastrophic and critical circuit failures have been suggested.

In the literature, there are two outstanding studies that are fairly related with the content of FMEA submitted in this thesis. Wang and Yang [10] examined the parametric faults in their study considering the component tolerances. While performing parametric fault test with tolerance analysis, they used both sensitivity method and fuzzy analysis method. They dealt with a video amplifier circuit and constituted fault set and test nodes for that circuit. Using membership function, they investigated the effect of each fault and aimed to decrease the computation time. Table 1.1 includes the fault set generated for the video amplifier circuit.

Table 1.1. Fault Set of Video Amplifier Circuit [10]

No.	fault name	No.	fault name	No.	fault name
f_0	normal	f_1	C2 short	f_2	L1 open
f_3	L2 open	f_4	Q1 B-E short	f_5	Q1 C-E short
f_6	Q1 B-C short	f_7	R1 short	f_8	R2 open
f_9	R2 short				

Another important study in FMEA topic is published by Liu and Ozev [5]. In their study, they have performed a detailed fault analysis by presenting statistical test development and defining hierarchical variability analysis technique. Their main aim is to reduce the analog circuits' test time during the development phase. They classified the faults in analog domain into two major types; catastrophic and parametric faults. Catastrophic faults include short and open circuit failures of the components. Liu and Ozev [5] constituted a model to simulate the short and open circuit failures as shown in Figure 1.5.

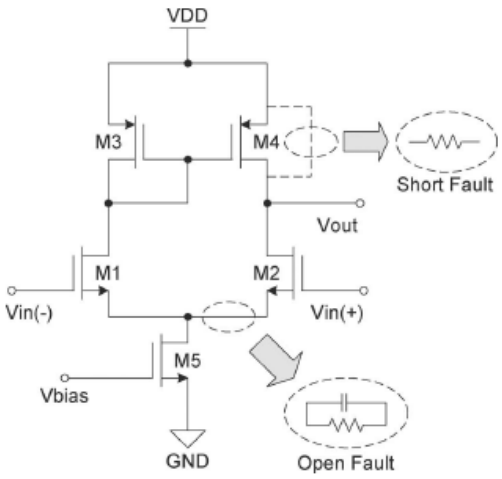

Figure 1.5. Open and Short Circuit Failure Simulation [5]

1.3. Reliability Allocation and Prediction

These two reliability tools target to enhance the reliability of the overall system. Reliability allocation sets reliability goals at subsystem level by distributing the overall reliability goal of the system to the subsystems. There are various reliability allocation methods. The simplest method involves simply distributing the system reliability goal equally among all subsystems. Majority of the reliability allocation methods require a survey, which gives idea about the priority of each subsystem and allocation is performed according to priorities.

Since FPDC is a subsystem itself, it is not meaningful to perform reliability allocation in this study.

Reliability prediction is an application that is highly related with the reliability allocation. Reliability prediction is performed at component level and the reliability of the subsystem can be obtained simply with the multiplication of the predicted reliability values of all components assuming that there are no redundant parts in the circuit. Multiplication method implies that the failure of any electronic component in the circuit cause the circuit malfunction. This case is assumed to be valid unless a detailed failure analysis is performed and non-critical components are determined.

Obtained reliability prediction results are compared with reliability allocation values and it is checked if the target values hold. Thus, actions to enhance reliability are taken at the design phase. However, it must be kept in mind that reliability prediction values are only approximated values and do not reflect the real reliability values, which can only be obtained by performing appropriate reliability tests.

There are many reliability prediction methods and standards in the industry. Most common reliability prediction standard is the U.S. military standard, MIL-HDBK-217F [13]. This document classifies electronic components under 19 different types and provides formulation for failure rate computation of each component type. Common factors that contribute to failure rate prediction are temperature, environment, quality and stress values. For instance, failure rate formulation for FET type transistors is as the following.

$$\lambda_p = \lambda_b \pi_T \pi_A \pi_Q \pi_E \quad \text{Failures}/10^6 \text{ hours} \tag{1.1}$$

λ_p : Failure rate of the FET transistor

λ_b : Base failure rate

π_T : Temperature factor

π_A : Application factor

π_E : Environment factor

π_Q : Quality factor

Factors in the formula take different values for different applications, temperatures, quality levels etc. Table 1.2 includes the temperature factors for the temperatures in 25-175 °C interval.

Table 1.2. Temperature Factors for Low Frequency FET Type Transistors [13]

T_J (°C)	π_T	T_J (°C)	π_T
25	1.0	105	3.9
30	1.1	110	4.2
35	1.2	115	4.5
40	1.4	120	4.8
45	1.5	125	5.1
50	1.6	130	5.4
55	1.8	135	5.7
60	2.0	140	6.0
65	2.1	145	6.4
70	2.3	150	6.7
75	2.5	155	7.1
80	2.7	160	7.5
85	3.0	165	7.9
90	3.2	170	8.3
95	3.4	175	8.7
100	3.7		

Values for all other factors are determined in a similar manner. Calculated failure rates are converted to reliability using exponential distribution. Exponential distribution is a well accepted model for calculating reliability of electronic components in electronics industry.

All the factors for the components depend on the laboratory results and rely on the documents published by Rome Laboratory (RL) in New York (formerly Rome Air Development Center (RADC)). Full reference list can be reached from the bibliography of MIL-HDBK-217F document [13].

In this study, reliability prediction is not implemented either because of the straightforward approach of the method. This analysis method only takes into consideration the parts list and does not require circuit scheme. Thus, reliability prediction is not circuit specific and it is performed automatically by many software tools once the application information (operating temperature, application, environment etc.) is entered.

Other reliability prediction models include Telcordia, FIDES, 217Plus, however most common model is the U.S. military standard MIL-HDBK-217F.

1.4. Fault Tree Analysis

Fault tree analysis is also a failure analysis method, in which undesired operation of circuit is analyzed using boolean logic. In this analysis, the circuit malfunctions arising from the combination of more than one component failure are investigated. Fault tree analysis is usually performed by constructing a fault tree consisting of logic gates as shown in Figure 1.6. However, this analysis requires deep knowledge about the operation of the circuit under consideration. Implementing fault tree analysis in FPDC requires a detailed analysis and long computational time; therefore this application is left as a future study.

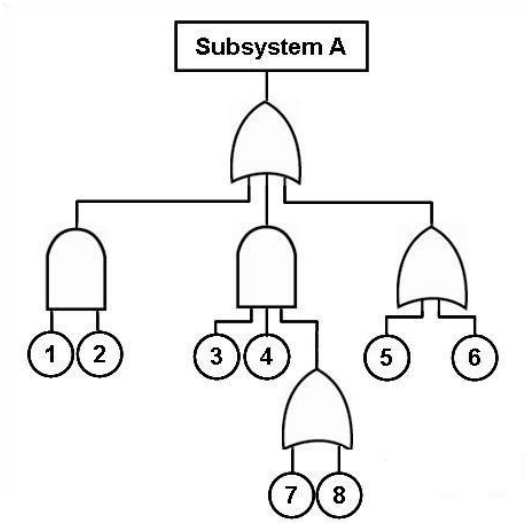

Figure 1.6. Sample Fault Tree

The outline of this thesis is as follows. In Chapter 2, the main set of rules and concepts for electrical circuit analysis is summarized. This chapter provides quick knowledge about the general electrical terms, circuit elements while introducing the laws used in generating the circuit equations. Chapter 3 includes the problem definition and the solution methods; while the results for the worst case circuit tolerance analysis is given in Chapter 4 and the failure modes and effects analysis in Chapter 5. We conclude the study in Chapter 6.

CHAPTER 2

PRINCIPLES OF ELECTRIC CIRCUIT ANALYSIS

There are many different elements in an electronic circuit and each of these elements has several parameters that affect the circuit's performance. However, most of these parameters vary due to imperfect manufacturing process. In this study, we investigate the operation of an electronic circuit which controls the power supply of a fuel pump that is responsible from pumping fuel to a turbojet engine when the control variables are in their tolerance bands while proposing an alternative methodology to basic circuit simulation methods.

In Figure 2.1, the schematic of the Fuel Pump Driver Circuit is shown. In this circuit, there are 6 different elements, each of which contributes to the circuit's performance in various ways. They are:

1) Resistor
2) Capacitor
3) Bipolar Junction Transistor (BJT)
4) Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
5) Zener Diode
6) Comparator

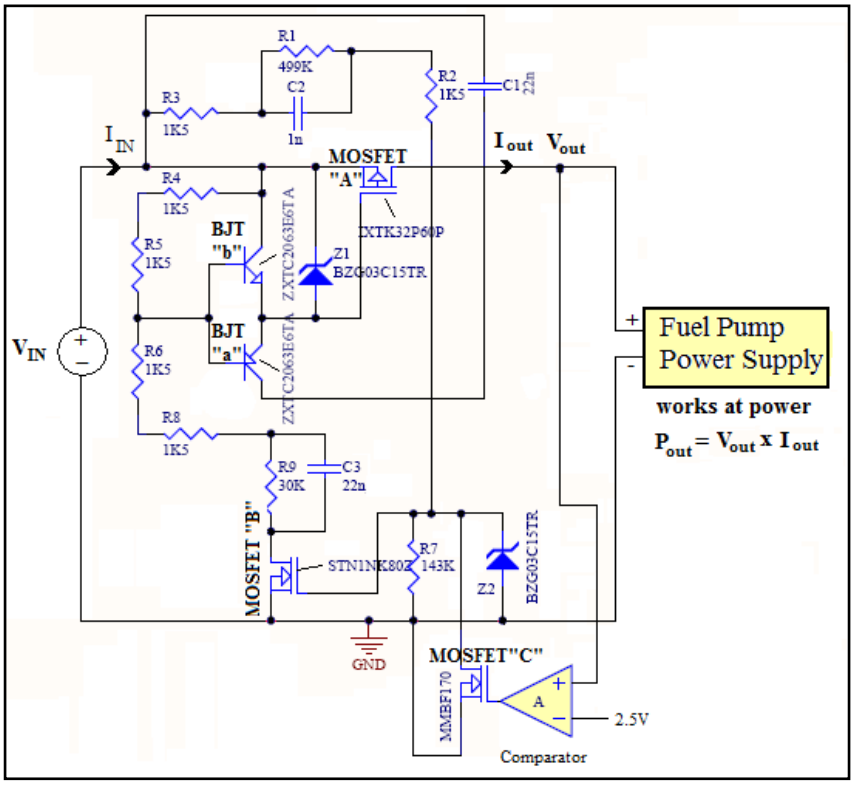

Figure 2.1. Schematic Representation of Fuel Pump Driver Circuit

Before giving the characteristics of these elements, explaining the basic terms that are used in electronic circuit analysis can be useful.

2.1. Current, Voltage and Power

Current, shown as I, can be defined as the flow of an electric charge measured in amperes (A). Voltage, V, is the name for electrical force difference between two terminals of an electronic component and measured in volts (V). It can fundamentally be said that if there is a voltage between the terminals of a component then a current is driven through it. The relation between these two terms depends on the electronic component. For instance, in a resistor current depends on the voltage linearly, whereas in a BJT current varies exponentially with the voltage across its terminals.

Power, P, is the rate at which the electrical energy is transferred by an electronic component and measured in watts (W) in SI units.

Power is basically the product of the voltage and current: P = V x I

2.2. Ground (GND) Node

This node is the reference node in a circuit which is basically assumed to have “0” voltage so that all the elements in the circuit will function correctly having the same point of reference.

2.3. Circuit Elements

The operations of the electronic components used in the circuit are summarized below.

2.3.1. Resistor

Resistor is a two terminal electronic component that produces voltage across its terminals. It can be used for maintaining the voltage at a terminal at desired levels or regulating the current that flows through a path to a desired level. Actually, resistors are very basic circuit elements and used for many purposes in electronic circuits. The main characteristics of a resistor are its resistance, tolerance and power rating. The resistance is represented with letter “R” and the SI unit for it is “ohm” (Ω). Figure 2.2 shows a schematic representation of a resistor.

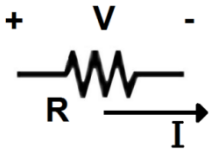

Figure 2.2. Schematic Representation of a Resistor

The behavior of an ideal resistor is dictated by the relationship specified in Ohm’s law:

$$V = I \times R \tag{2.1}$$

As can be figured from the formula, in a resistor current through a resistor varies linearly with the voltage across its terminals.

Resistors as manufactured are subject to a certain percentage tolerance. This tolerance may be as low as 0.01% of the resistance or up high like 5% or even

10%. Using a resistor with a tight tolerance can make the design more robust, but it slightly increases cost. However choosing a resistor with a wide tolerance, thus with a lower cost, may cause the circuit fail in some cases. In this study, the tolerance for all the resistors are 5% and the analyses are carried out for the varying resistance values within this 5% tolerance band.

2.3.2. Capacitor

A capacitor is an electronic component which consists of two parallel conductor plates and dielectric (insulator) material in between them. A capacitor is characterized by a constant value, capacitance that is measured in the SI unit "farads" (F).

The current through a capacitor is driven by the rate of change in the voltage across its terminals:

$$\mathbf{I}(t) = \mathbf{C}\frac{\mathbf{dV}}{dt} \tag{2.2}$$

Thus, the current flows through a capacitor if the voltage across its terminal changes in time. But since we investigate only the steady state condition in the present analysis, the currents through the capacitors are assumed to be zero.

Figure 2.3 shows the schematic representation of a capacitor.

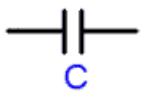

Figure 2.3. Schematic Representations of a Capacitor

2.3.3. Zener Diode

Zener diode is a two-terminal semiconductor electronic component which has different characteristics depending on the direction of the current. Current can be driven in both ways unlike the typical diodes which conducts the current in only one direction.

The symbolic representation of a zener diode is included in Figure 2.4.

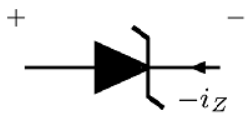

Figure 2.4. Schematic Representation of a Zener Diode

The general diode current-voltage characteristics are shown in Figure 2.5.

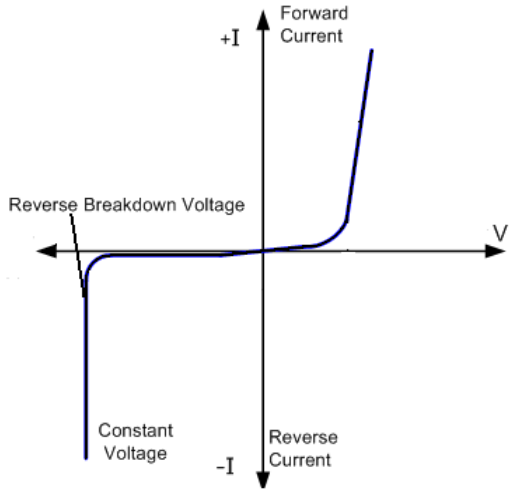

Figure 2.5. I-V Characteristics of a Diode

As can be seen from Figure 2.5, the forward current increases exponentially with the increasing voltage as

$$I = I_S\left[e^{\left(\frac{V}{V_t}\right)} - 1\right] \tag{2.3}$$

where V_t is the thermal voltage and varies with temperature and I_s is saturation current (or scale current).

Typical diodes are damaged once reverse breakdown voltage is applied between their terminals. This is why the zener diode manufacturing has begun. Zener diodes can also operate in negative voltages greater than the reverse breakdown voltage. This property provides the zener diodes an important role in circuit operation. Zener diodes are usually operated in the reverse region that is shown in Figure 2.5, so that it prevents the voltage between two terminals go beyond the reverse

breakdown voltage and contributes to the circuit operation with that valuable property.

Unfortunately, a general formula that characterizes the reverse current does not exist. Reverse current vs. the voltage characteristics can only be obtained from circuit simulation tools. That is how the reverse characteristics of BZG03C15 coded zener diode which is used in our circuit are generated.

2.3.4. Bipolar Junction Transistor (BJT)

A Bipolar Junction Transistor is a three terminal semiconductor electronic component. It can be used in different circuit applications like switching and amplifying, that is, increasing the input current in the output.

BJT's have two different types: NPN and PNP. The operations of these two types of BJT's are slightly different. The schematics of NPN and PNP are given in Figure 2.6 where B stands for "base", C for "collector" and E for "emitter".

PNP type BJT NPN type BJT

Figure 2.6. Schematic Representations of NPN and PNP type BJT's

The main difference between NPN and PNP is the direction of the currents. While in NPN the current flows from collector to the base and emitter, in PNP it flows from emitter to base and collector. Also it must be noted that NPN is faster at switching when compared to PNP.

Transistors are fairly more complicated components compared to the resistors, capacitors and diodes. There are four different operating regions for the BJT's.

1. Forward Active Region: Usually used for amplification purposes.
2. Saturation Region: Usually used in switching applications.

3. Cut-off Region: Off condition for a BJT (no current flows through the terminals)

4. Reverse-Active Region: Collector and emitter changes roles, seldom used.

Each of these regions is characterized by the voltages across the terminals.

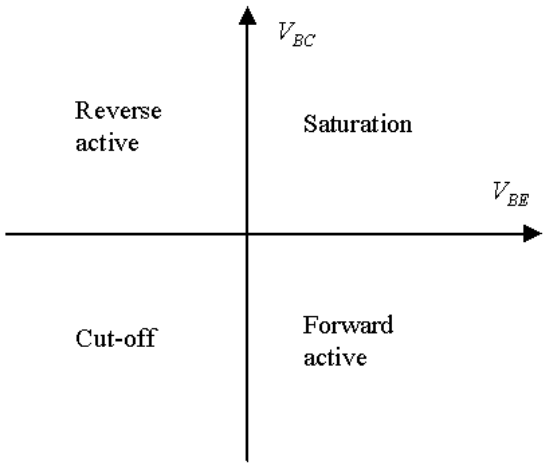

Figure 2.7. Operating Modes of a NPN Transistor

Figure 2.7 shows the operating modes of a NPN transistor according to the voltages across base, collector and emitter terminals where V_{BC} means the voltage between base and collector terminals and V_{BE} between base and emitter terminals:

$$V_{BC} = V_B - V_C \qquad \text{and} \qquad V_{BE} = V_B - V_C \tag{2.4}$$

Before showing the requirements for the operating regions, it is important to give the relationship between the voltages between the terminals:

$$V_{CE} = V_{CB} + V_{BE} \text{ (for NPN) and } V_{EC} = V_{EB} + V_{BC} \text{ (for PNP)} \tag{2.5}$$

The required voltage levels for each operating region of NPN and PNP transistors are shown in Table 2.1.

Table 2.1. BJT Operating Regions and Voltage Requirements

Region	For NPN	For PNP
Forward Active	$V_{CE} > V_{CE(sat)}$, $V_{BE} > V_{BE(on)}$ and $V_{BC} < 0$	$V_{EC} > V_{EC(sat)}$, $V_{EB} > V_{EB(on)}$ and $V_{CB} < 0$
Saturation	$V_{CE} < V_{CE(sat)}$, $V_{BE} > V_{BE(on)}$ and $V_{BC} > 0$	$V_{EC} < V_{EC(sat)}$, $V_{EB} > V_{EB(on)}$ and $V_{CB} > 0$
Cut-off	$V_{BE} < V_{BE(on)}$ and $V_{BC} < 0$	$V_{EB} < V_{EB(on)}$ and $V_{CB} < 0$
Reverse Active	$V_{BE} < V_{BE(on)}$ and $V_{BC} > 0$	$V_{EB} < V_{EB(on)}$ and $V_{CB} > 0$

In Table 2.1, $V_{BE(on)}$ ($V_{EB(on)}$) term is introduced. This voltage characterizes the operating region of a BJT and varies with the temperature and the collector current. Figure 2.8 shows the variation of $V_{BE(on)}$ values of the BJT "b" used in the circuit with respect to collector current (I_C) and temperature.

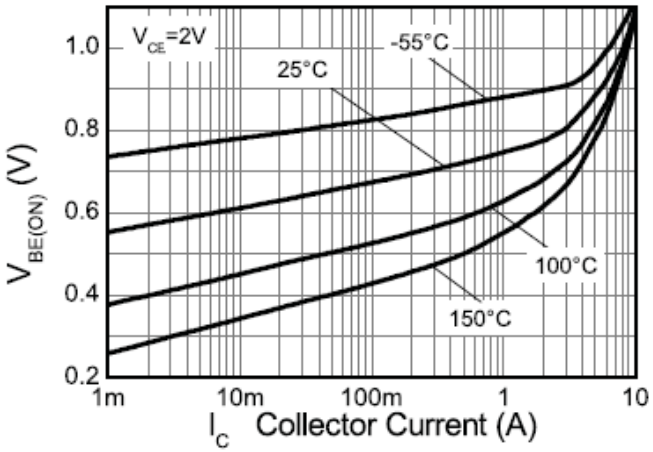

Figure 2.8. $V_{BE(on)}$ vs. I_C Characteristics of ZXTN2063E6 BJT "b"

Figure 2.8 shows that the temperature plays a very important role on the circuit analysis. Temperature also takes part in the current calculation formulas. While calculating the BJT currents, Gummel-Poon model is chosen and the Gummel-Poon transistor equations are used. For instance, collector current calculation for BJT "a" in saturation region can be shown as:

$$I_C = \frac{Is}{q_B}\left[e^{\left(\frac{V_{EB}}{n_F V_t}\right)} - e^{\left(\frac{V_{CB}}{n_R V_t}\right)}\right] - \frac{q_B Is}{\beta_R}\left[e^{\left(\frac{V_{CB}}{n_R V_t}\right)} - 1\right] - I_{SC}\left[e^{\left(\frac{V_{CB}}{n_C V_t}\right)} - 1\right] \quad (2.6)$$

It can be figured out from the formula that there are various parameters like I_s, the transport saturation current; $V_{t,}$ the thermal voltage and β_R, the ideal maximum forward beta that effect the current values of a BJT. Details of the Gummel-Poon model and the complete set of current equations can be reached from [1].

In the circuit scheme supplied in Figure 2.1, there are two BJT's, one NPN and one PNP. In the circuit operation, these transistors are used as switches and their normal region of operation must be Cut-off and Saturation respectively in order to run the circuit properly. Throughout this study, PNP transistor in the circuit is called as BJT "a" and the NPN transistor as BJT "b".

2.3.5. Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

Metal Oxide Semiconductor Field Effect Transistors or shortly MOSFET's are one of the most crucial elements in circuit operation. Just like BJT's, they can be used for amplifying and switching purposes.

A MOSFET has three terminals and its operation is similar to BJT's. It has three different operating regions and in each region the current through the terminals show different characteristics.

There are two types of MOSFET's, NMOS and PMOS, each of which is shown schematically in Figure 2.9.

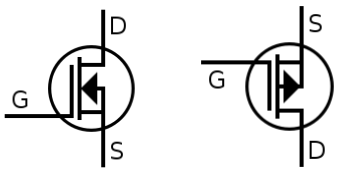

Figure 2.9. Schematic Representations of MOSFET Transistors

Both NMOS and PMOS transistors have gate “G”, drain “D” and source “S“ terminals. In NMOS transistors, the current flows from drain to source, whereas in PMOS’s it flows from source to drain. Gate current is assumed to be zero in MOSFET’s. Therefore in MOSFET’s, drain current is always equal to source current.

The three operating regions of MOSFET’s and the requirements for these regions are summed in Table 2.2.

Table 2.2. MOSFET Operating Regions and Voltage Requirements

Region	NMOS	PMOS
Saturation	$V_{GS} > V_t$ and $V_{DS} > V_{GS} - V_t$	$V_{GS} < V_t$ and $V_{DS} < V_{GS} - V_t$
Triode	$V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$	$V_{GS} < V_t$ and $V_{DS} > V_{GS} - V_t$
Cut-Off	$V_{GS} < V_t$	$V_{GS} > V_t$

In Table 2.3, drain-source current formulation for each region is introduced.

Table 2.3. MOSFET Current Characteristics in Different Operating Regions

Region	**I_{DS} (for NMOS) or I_{SD} (for PMOS)**
Saturation	$I = K(V_{GS} - V_{th})^2$
Triode	$I = K[2(V_{GS} - V_{th})V_{DS} - V_{DS}^2]$
Cut-Off	$I = 0$

Transconductance parameter, K is a constant for a MOSFET and depends on the geometry of internal structure of the MOSFET. The threshold voltage, V_{th} characterizes the operating regions of the MOSFET’s.

In our application, there are two NMOS and one PMOS transistors, each of which is used as switches and operate either in cut-off or triode region. In Figure 2.1, PMOS transistor is named as MOSFET “A” and the NMOS transistors are named as MOSFET “B” and MOSFET “C”. In this study, the operation of MOSFET “C” is not checked since it is driven by the comparator, whose operation cannot be

simulated with basic simulation tools. Thus, MOSFET "C" is assumed to be operating properly since it only depends on the proper operation of the comparator.

Throughout this study, PMOS transistor is referred as MOSFET "A" and NMOS transistor, whose operation is checked, as MOSFET "B".

2.3.6. Comparator

A comparator is a basic integrated circuit which compares two voltage inputs and generates an output voltage depending on the comparison of the input voltage. In our circuit, one of the input nodes is connected to the reduced output voltage and the other to 2.5V reference voltage. The reduced output voltage will be around the reference voltage depending on the input voltage.

So what the comparator output will be:

- 5V if the reduced output voltage is higher than 2.5V
- 0V if the reduced output voltage is lower than 2.5V

A basic circuitry consisting of three resistors are used to reduce the output voltage to voltages around 2.5V.

2.4. Circuit Analysis

In order to perform performance analysis for the circuit given in Figure 1, a set of equations is generated utilizing the characteristics of each circuit element explained above. However, the characteristics of the elements are not sufficient to build up all the equations. Two basic principles are taken into consideration in the circuit analysis: Kirchhoff's Voltage Law and Kirchhoff's Current Law. These two laws are briefly explained next.

2.4.1. Kirchhoff's Voltage Law (KVL)

KVL basically implies that the sum of all voltages around any closed circuit (loop) equals zero. It can be formulated as

$$\sum_{k=1}^{n} V_k = 0 \tag{2.7}$$

where V_k is the voltage of element k in the loop, k=1, 2, …, n.

For instance, the equation $V_2 + V_1 + V_N - V_3 = 0$ can be drawn from the KVL loop illustrated in Figure 2.10.

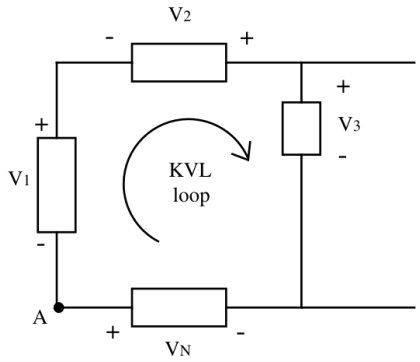

Figure 2.10. KVL Loop Example

2.4.2. Kirchhoff's Current Law (KCL)

KCL implies that the sum of incoming currents to a node is equal to the sum of outgoing currents from that node. Just like KVL, it can be formulated as

$$\sum_{k=1}^{n} I_k = 0 \tag{2.8}$$

where I_K is the current on branch k connected to the node, k=1, 2, …, n.

A sample KCL equation can be written for the case in Figure 2.11 as $I_2 + I_3 = I_1 + I_4$.

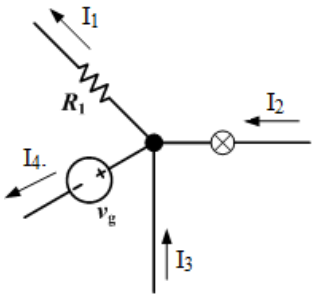

Figure 2.11. KCL Node Example

CHAPTER 3

PROBLEM DEFINITION

Monte Carlo simulation is widely used in reliability analysis of complicated electronic circuits ([2],[4],[8],[11],[12]). Given the tolerance bands of the elements in the circuit, simulation produces the possible realizations of the circuit performance. However, this simulation can only provide limited worst case results. The main purpose of this study is to perform reliability analysis of the fuel pump driver circuit ensuring the real worst case conditions. The worst case results are obtained by solving linear and nonlinear circuit equations taking into consideration the tolerance bands of resistances and temperature interval.

Unlike most of the worst case circuit analysis studies in the literature, temperature effect is also taken into account by defining it as a decision variable varying in the operating temperature interval of the circuit. This helps us to see the circuit's performance in harsh environments.

There are various issues in reliability analysis. In this work we perform the following two analyses:

1) Worst case circuit tolerance analysis at discrete power output requirements
2) Failure modes and effect analysis

Before starting with the analysis, the fuel pump driver circuit's normal operation will be explained.

3.1. Description of the Fuel Pump Driver Circuit (FPDC)

The circuit scheme of FPDC is supplied in Figure 3.1. In this study, the reliability analysis of this circuit is performed according to resistance values R_1, $R_2 \ldots R_9$ varying in their tolerance bands and temperature T, which as well can take values inside the specified operating temperature interval of FPDC: $-30 \leq T \leq 55$.

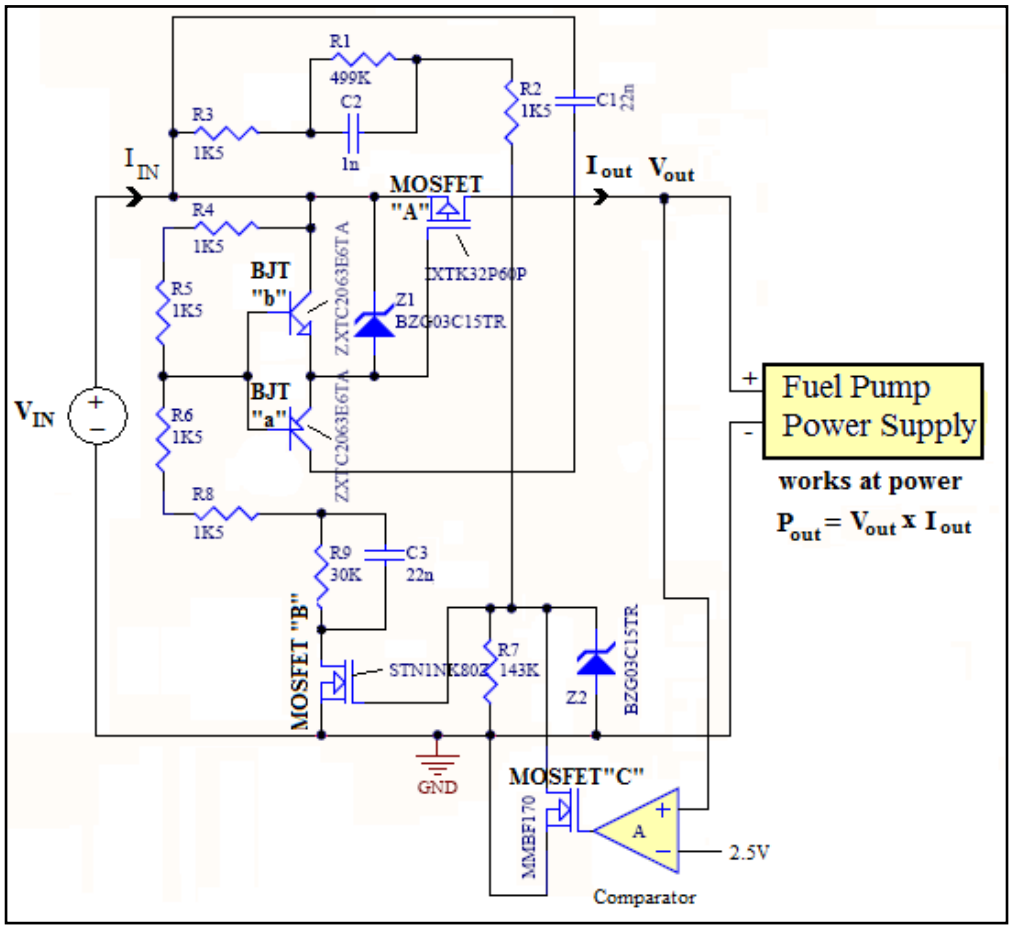

Figure 3.1. Schematic Representation of Fuel Pump Driver Circuit

As a whole, FPDC can be handled as a switch which controls the current going to power supply of the fuel pump. The fuel pump is responsible from pumping fuel to the turbojet engine. The speed of the engine, thus required amount of fuel to be pumped to the engine, is determined by the main computer and addressed to Fuel Pump electronic circuit which is not in the scope of this study. So depending on the speed of the engine, the fuel pump power supply requires different voltage and current values from FPDC to pump the required fuel to the engine.

The alternator which converts the mechanical energy of the engine to electrical energy supplies voltage to FPDC. Faster the engine rotates the higher voltage the alternator generates. Thus a linear relationship can be established between the output power requirement and the input voltage of the pump driver circuit.

Figure 3.2 draws the relation of the fuel pump driver circuit, fuel pump, turbojet motor and the alternator.

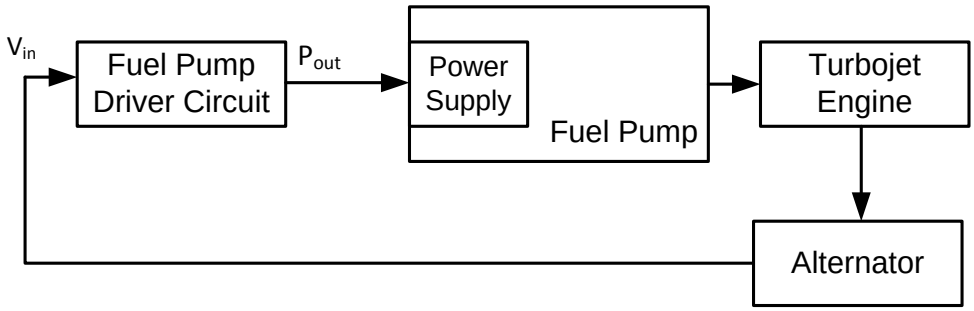

Figure 3.2. Relationship Between the Circuit and Other Elements

According to the relevant technical document, the fuel pump may require a power between 50W and 750W during its operation depending on the fuel requirement of the turbojet engine. The fuel pump driver circuit is designed so that the input voltage (rectified alternator voltage) will be between 200V and 350V. Assuming that the input voltage varies linearly with the output power level, the relationship between the input voltage and the output power level can be dictated by the following equation.

$$V_{IN} = \frac{3P_{out} + 2650}{14} \tag{3.1}$$

The main purpose of the circuit is to maintain the voltage at the output below 280V using the MOSFET "A" as a switch. When the output voltage exceeds 280V, the circuit will open the MOSFET "A" by operating it in cut-off region and when the output voltage remains below 280V, MOSFET "A" will operate at triode region letting the current pass through it and supply voltage to the power supply of the fuel pump.

Normally the circuit is expected to operate at a maximum of 280V input voltage. So in normal conditions, MOSFET "A" is not expected to turn on and off during its

operation. In this study, assuming the input voltage will remain below 280V, the operation of the circuit will be analyzed for tolerant resistance values and varying temperature at discrete input voltages or output powers.

3.2. Problems Under Consideration

The problem considered here serves purpose for analyzing the circuit operation by checking the transistor voltage levels. In this problem, the control/decision variables are resistance values R_1, $R_2 \ldots R_9$, temperature T and the voltage input V_{IN}. The rest of the variables (voltage, current levels etc..) are determined by these control variables. Their values are uniquely determined according to T and V_{IN} values at the instance. Note that R_1, $R_2 \ldots R_9$ vary within their tolerance bands which is ±5% in our case and T can take any value between -30 and 55 °C.

In the real case, neither tolerant resistance values, nor the temperature and the voltage input values can be controlled. However, they are treated as control variables in the optimization routine. The optimizations are performed in discrete V_{IN} instances, while R_1, $R_2 \ldots R_9$ and T variables are iteratively generated by ModeFrontier program and sent to MATLAB, where the problem is defined and the equations are solved for the instant R_1, $R_2 \ldots R_9$ and T values.

By solving the problem defined here, it is intended to observe:

1) The effect of the resistor tolerances which arises from manufacturing process and cannot be controlled.
2) To verify that the circuit operates properly in the specified operating temperature of the circuit.
3) To make sure that the circuit operates properly in $200 \leq V_{IN} \leq 280$ interval.

The problem is handled by solving several non-linear programs. The objective function will be changed sequentially to check the condition at certain nodes of the circuit while all of the constraints governing the system are satisfied.

In this section, the description of the variables, constants, constraints and the objectives with their check conditions are provided. Firstly, the decision variables

and the constants that are used in the problem will be introduced. There are 44 variables including the decision variables and the uncontrollable variables. Table 3.1 lists the uncontrollable variables and their descriptions.

Table 3.1. Descriptions of Uncontrollable Variables

Decision Variable	Description
$\mathbf{I_1}$	Current through R_3
$\mathbf{I_2}$	Current through R_4
$\mathbf{I_3}$	Current through R_7
$\mathbf{I_{z1}}$	Reverse Current through Z_1
$\mathbf{I_{z2}}$	Reverse Current through Z_2
$\mathbf{I_{Ca}}$	Collector Current of BJT “a”
$\mathbf{I_{Ea}}$	Emitter Current of BJT “a”
$\mathbf{I_{Ba}}$	Base Current of BJT “a”
$\mathbf{I_{Cb}}$	Collector Current of BJT “b”
$\mathbf{I_{Eb}}$	Emitter Current of BJT “b”
$\mathbf{I_{Bb}}$	Base Current of BJT “b”
$\mathbf{I_{SDA}}$	Current through MOSFET “A”
$\mathbf{I_{DSB}}$	Current through MOSFET “B”
$\mathbf{I_{IN}}$	Input Current
$\mathbf{V_{DSB}}$	Drain-to-Source Voltage of MOSFET “B”
$\mathbf{V_{GSB}}$	Gate-to-Source Voltage of MOSFET “B”
$\mathbf{V_{DSA}}$	Drain-to-Source Voltage of MOSFET “A”
$\mathbf{V_{GSA}}$	Gate-to-Source Voltage of MOSFET “A”
$\mathbf{V_{Eca}}$	Emitter-to-Collector Voltage of BJT “a”
$\mathbf{V_{Eba}}$	Emitter-to-Base Voltage of BJT “a”
$\mathbf{V_{Bca}}$	Base-to-Collector Voltage of BJT “a”
$\mathbf{V_{Ceb}}$	Collector-to-Emitter Voltage of BJT “b”
$\mathbf{V_{Beb}}$	Base-to-Emitter Voltage of BJT “b”
$\mathbf{V_{CBb}}$	Collector-to-Base Voltage of BJT “b”

Table 3.1 (cont'd)

$\mathbf{V_{C1}}$	Voltage Across the C_1
$\mathbf{V_{out}}$	Voltage at the Output
$\mathbf{V_{z1}}$	Reverse Voltage Across Z_1
$\mathbf{V_{z2}}$	Reverse Voltage Across Z_2
$\mathbf{V_t}$	Thermal Voltage
$\mathbf{q_{Ba}}$	Normalized majority base charge of BJT "a"
$\mathbf{q_{1sa}}$	Variable used in Normalized majority base charge calculation of BJT "a"
$\mathbf{q_{2sa}}$	Variable used in Normalized majority base charge calculation of BJT "a"
$\mathbf{P_{out}}$	Output Power
$\mathbf{V_{EBaON}}$	Emitter-Base Turn-On Voltage of BJT "a"

In Table 3.2, intervals of each decision variable are given. Variables with "R" representation correspond to the tolerant resistance values of each resistor used in the circuit and T denotes the temperature which is assumed to vary between -30 and 55 °C.

Table 3.2. Intervals of Decision Variables

Decision Variable	Minimum Value	Nominal Value	Maximum Value
$\mathbf{R_1}$	474,050	499000	523,950
$\mathbf{R_2}$	1425	1500	1575
$\mathbf{R_3}$	1425	1500	1575
$\mathbf{R_4}$	1425	1500	1575
$\mathbf{R_5}$	1425	1500	1575
$\mathbf{R_6}$	1425	1500	1575
$\mathbf{R_7}$	135,850	143000	150,150
$\mathbf{R_8}$	1425	1500	1575
$\mathbf{R_9}$	28,500	30000	31,500
T	-30	N/A	55

Note that each resistance value varies 5% around its nominal value. This 5% tolerance arises from the manufacturing process and it is remarked at the technical specification of every resistor.

Table 3.3 lists the constant values used in the constraints and their descriptions.

Table 3.3. Parameters and Constants Used in the Constraints

Constant	Value	Description
$\mathbf{K_A}$	0.955	Transconductance parameter of MOSFET "A"
$\mathbf{K_B}$	0.00428	Transconductance parameter of MOSFET "B"
$\mathbf{V_{thA}}$	-4.5	Threshold voltage of MOSFET "A"
$\mathbf{V_{thB}}$	4.5	Threshold voltage of MOSFET "B"
$\mathbf{I_{Sa}}$	4×10^{-13}	Transport saturation current of BJT "a"
$\mathbf{I_{Sea}}$	0	Base-to-emitter leakage saturation current of BJT "a"
$\mathbf{I_{Sca}}$	0	Base-to-collector leakage saturation current of BJT "a"
$\mathbf{n_{Fa}}$	1	Forward current emission coefficient of BJT "a"
$\mathbf{n_{Ra}}$	1	Reverse current emission coefficient of BJT "a"
$\mathbf{VAR_a}$	+INF	Reverse Early Voltage of BJT "a"
$\mathbf{VAF_a}$	23	Forward Early Voltage of BJT "a"
$\mathbf{I_{kfa}}$	3.5	Forward beta hi current roll-off for BJT "a"
$\mathbf{I_{kra}}$	+INF	Reverse beta hi current roll-off for BJT "a"
$\mathbf{n_{Ea}}$	1.5	Base-emitter leakage emission coefficient of BJT "a"
$\mathbf{n_{Ca}}$	2	Base-collector leakage emission coefficient of BJT "a"
$\mathbf{B_{Ra}}$	97	Ideal maximum reverse beta of BJT "a"
$\mathbf{B_{Rb}}$	470	Ideal maximum forward beta of BJT "a"
$\mathbf{I_{Sb}}$	5.1×10^{-13}	Transport saturation current of BJT "b"
$\mathbf{I_{SCb}}$	1.1×10^{-13}	Base-to-collector leakage saturation current of BJT"b"
$\mathbf{I_{Seb}}$	1.2×10^{-13}	Base-to-emitter leakage saturation current of BJT "b"
$\mathbf{\beta_{Rb}}$	65	Ideal maximum reverse beta of BJT "b"
$\mathbf{\beta_{Fb}}$	480	Ideal maximum forward beta of BJT "b"
k	1.380×10^{-23}	Boltzmann's constant
q	1.602×10^{-19}	Magnitude of electric charge on the electron

The circuit equations obtained by using KVL and KCL are used as constraints in this analysis. There are a total of 34 constraints and Table 3.4 presents the complete set of constraints and the methods used for obtaining each. Bold characters denote the variables.

Table 3.4. Constraints

Constraint	Method
$\mathbf{I_{IN} = I_1 + I_{SDA} + I_{z1} + I_2 + I_{Cb} - I_{Ca}}$	KCL
$\mathbf{I_2 = I_{DSB} - I_{Ba} + I_{Bb}}$	KCL
$\mathbf{I_{Ea} = I_{z1} + I_{Eb}}$	KCL
$\mathbf{I_1 = I_3 + I_{z2}}$	KCL
$\mathbf{I_{Ea} = I_{Ca} + I_{Ba}}$	KCL
$\mathbf{I_{Eb} = I_{Cb} + I_{Bb}}$	KCL
$\mathbf{I_{Ca}} = 0$	See Note 1
$V_{IN} = \mathbf{V_{DSB}} + \mathbf{I_{DSB}}(R_6 + R_8 + R_9) + \mathbf{I_2}(R_4 + R_5)$	KVL
$V_{IN} = \mathbf{I_3}R_7 + \mathbf{I_1}(R_1 + R_2 + R_3)$	KVL
$\mathbf{V_{CBb} = I_2}(R_4 + R_5)$	KVL
$\mathbf{V_{BEb} = -V_{EBa}}$	KVL
$\mathbf{V_{GSA} = -V_{CEb}}$	KVL
$\mathbf{V_{GSB} = I_3}R_7$	KVL
$\mathbf{V_{CEb} = V_{CBb} + V_{BEb}}$	KVL
$\mathbf{V_{ECa} = V_{EBa} + V_{BCa}}$	KVL
$\mathbf{V_{CEb} = V_{z1}}$	KVL
$\mathbf{V_{GSB} = V_{z2}}$	KVL
$\mathbf{V_{ECa} = V_{GSA} + V_{C1}}$	KVL
$V_{IN} = \mathbf{-V_{DSA} + V_{OUT}}$	KVL
$\mathbf{I_{SDA}} = K[2(\mathbf{V_{GSA}} - V_{thA})\mathbf{V_{DSA}} - \mathbf{V_{DSA}^2}]$	MOSFET Eqn.'s (Triode region)
$\mathbf{I_{DSB}} = K[2(\mathbf{V_{GSB}} - V_{thB})\mathbf{V_{DSB}} - \mathbf{V_{DSB}^2}]$	MOSFET Eqn.'s (Triode region)

Table 3.4 (cont'd)

$\mathbf{I_{Cb}} = \frac{I_{Sb}}{\beta_{Rb}} + I_{SCb}$	Gummel-Poon BJT Eqn.'s (Cut-off region)
$\mathbf{I_{Bb}} = -I_{Sb}\left(\frac{\beta_{Fb}+\beta_{Rb}}{\beta_{Fb}\beta_{Rb}}\right) - (I_{Seb} + I_{SCb})$	Gummel-Poon BJT Eqn.'s (Cut-off region)
$\mathbf{I_{Ba}} = \frac{I_{Sa}}{\beta_{Fa}}\left[e^{\left(\frac{\mathbf{V_{EBa}}}{n_{Fa}\mathbf{V_t}}\right)} - 1\right] + I_{Sea}\left[e^{\left(\frac{\mathbf{V_{EBa}}}{n_{Ea}\mathbf{V_t}}\right)} - 1\right] + \frac{I_{Sa}}{\beta_{Ra}}\left[e^{\left(\frac{\mathbf{V_{CBa}}}{n_{Ra}\mathbf{V_t}}\right)} - 1\right] + I_{Sca}\left[e^{\left(\frac{\mathbf{V_{CBa}}}{n_{Ca}\mathbf{V_t}}\right)} - 1\right]$	Gummel-Poon BJT Eqn.'s (SAT region)
$\mathbf{I_{Ca}} = \frac{I_{Sa}}{\mathbf{q_{Ba}}}\left[e^{\left(\frac{\mathbf{V_{EBa}}}{n_{Fa}\mathbf{V_t}}\right)} - e^{\left(\frac{\mathbf{V_{CBa}}}{n_{Ra}\mathbf{V_t}}\right)}\right] - \frac{\mathbf{q_{Ba}}I_{Sa}}{\beta_{Ra}}\left[e^{\left(\frac{\mathbf{V_{CBa}}}{n_{Ra}\mathbf{V_t}}\right)} - 1\right] - I_{SCa}\left[e^{\left(\frac{\mathbf{V_{CBa}}}{n_{Ca}\mathbf{V_t}}\right)} - 1\right]$	Gummel-Poon BJT Eqn.'s (SAT region)
$\mathbf{q_{Ba}} = \frac{\mathbf{q_{1sa}}}{2}(1 + \sqrt{1 + 4\mathbf{q_{2sa}}})$	Gummel-Poon BJT Eqn.'s (SAT region)
$\mathbf{q_{1sa}} = \frac{1}{1 - \mathbf{V_{EBa}}/\mathrm{VAR_a} - \mathbf{V_{CBa}}/\mathrm{VAF_a}}$	Gummel-Poon BJT Eqn.'s (SAT region)
$\mathbf{q_{2sa}} = \frac{I_{Sa}}{I_{kfa}}\left[e^{\left(\frac{\mathbf{V_{EBa}}}{n_{Fa}\mathbf{V_t}}\right)} - 1\right] + \frac{I_{Sa}}{I_{kra}}\left[e^{\left(\frac{\mathbf{V_{CBa}}}{n_{Ra}\mathbf{V_t}}\right)} - 1\right]$	Gummel-Poon BJT Eqn.'s (SAT region)
$\mathbf{I_{z1}} = (4.571\mathrm{x}10^{-38})e^{(5.294\mathbf{V_{z1}})}$	See Note 2
$\mathbf{I_{z2}} = (4.571\mathrm{x}10^{-38})e^{(5.294\mathbf{V_{z2}})}$	See Note 2
$\mathbf{P_{OUT}} = \mathbf{V_{OUT}}\mathbf{I_{SDA}}$	Output Power Equation
$\mathbf{V_t} = \frac{k(\mathbf{T} + 273)}{q}$	Thermal Voltage Equation

Table 3.4 (cont'd)

$\mathbf{V_{IN}} = \frac{3\mathbf{P_{out}} + 2650}{14}$	$V_{in} - P_{out}$ Relationship
$\mathbf{V_{EBaON}} = -0.02241\mathbf{T} + 0.4108$	See Note 3
$474{,}050 \leq \mathbf{R_1} \leq 523{,}950$	R_1 tolerance
$1425 \leq \mathbf{R_2} \leq 1575$	R_2 tolerance
$1425 \leq \mathbf{R_3} \leq 1575$	R_3 tolerance
$1425 \leq \mathbf{R_4} \leq 1575$	R_4 tolerance
$1425 \leq \mathbf{R_5} \leq 1575$	R_5 tolerance
$1425 \leq \mathbf{R_6} \leq 1575$	R_6 tolerance
$135{,}850 \leq \mathbf{R_7} \leq 150{,}150$	R_7 tolerance
$1425 \leq \mathbf{R_8} \leq 1575$	R_8 tolerance
$28{,}500 \leq \mathbf{R_9} \leq 31{,}500$	R_9 tolerance
$-30 \leq \mathbf{T} \leq 55$	Temperature interval

Note 1: It is known that $I_{Ca} = -I_{C1}$ and $I_{C1}(t) = C_1 \frac{dV_{C1}}{dt}$. Since the circuit is analyzed at steady state conditions and at no voltage variations, we can say that V_{C1} does not vary with time. Therefore we can conclude that $I_{Ca} = -I_{C1} = 0$ as shown in the table.

Note 2: Actually in the literature no relationship has been established between reverse voltage (V_z) and reverse current (I_z) of zener diodes. What we have done here to relate them is to use the simulation results of the zener diode with part number BZG03C15TR which is used in the design and fit the simulation characteristics into an equation.

Note 3: There is no formulized relationship between V_{BEaON}, I_{Ca} and T in the literature as well. The data points in Figure 3.3 which represents V_{BEaON} vs. I_{Ca} relationship of BJT "a" at various temperatures are used to relate V_{BEaON} and T.

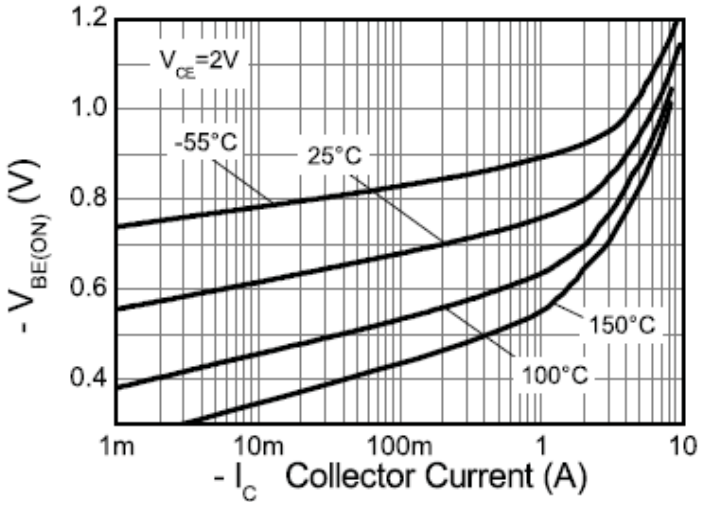

Figure 3.3. V_{BEaON} vs. I_{Ca} Characteristics [17]

Noting that $I_{Ca} = -I_{C1} \approx 0$, the relationship between V_{EBaON} and T has been formed using the data points in the leftmost part of the graph (the points with the smallest I_{Ca} values).

3.3. Objectives

There are 8 linear objectives each of which will be optimized separately. The objectives are chosen in order to check the circuit's operation in different temperature and resistance values.

The transistors in FPDC behave like switches such that the circuit operates properly only if each transistor stays in its correct position. So it is vital to check all the MOSFET and BJT voltages if they remain in the range that obeys the assumed operation regions. Table 3.5 shows the region each transistor is assumed to operate in and the conditions for those regions.

Table 3.5. Assumed Transistor Operating Regions and Required Conditions

Transistor	Operating Region	Required Conditions
BJT "b"	Cut-off	$V_{CBb} \geq 0$ **AND** $V_{BEb} \leq V_{BEbON}$
BJT "a"	Saturation	$V_{BCa} \leq 0$ **AND** $V_{EBa} \geq V_{EBaON}$
MOSFET "A"	Triode	$V_{GSA} \leq V_{thA}$ **AND** $V_{DSA} \geq V_{GSA} - V_{thA}$
MOSFET "B"	Triode	$V_{GSB} \geq V_{thB}$ **AND** $V_{DSB} \leq V_{GSB} - V_{thB}$

Note that $V_{EC} < V_{ECa(sat)}$, which as well is a required condition for MOSFET "A" to operate in saturation region, is missing in Table 3.5. This is because running computational analysis for this objective is unnecessary since V_{ECa} is minorly affected by R_1, $R_2 \ldots R_9$ and T variations and the exact value of $V_{ECa(sat)}$ cannot be exactly determined. According to technical datasheet of BJT "a", $V_{ECa(sat)}$ value is around 0.01 V and V_{ECa} is found to be 0.0003 ± 0.0001 V in any R, T and V_{IN} values. Thus, it is assumed that this condition is satisfied and no computational analysis will be performed for V_{ECa}.

The objective function forms and their check conditions are listed in Table 3.6.

Table 3.6. Objective Functions and Check Conditions

Objective Function	Check Condition
Minimize V_{CBb}	$\mathbf{V_{CBb}} \geq 0$
Maximize V_{BEb}	$\mathbf{V_{BEb}} \leq \mathbf{V_{BEbON}}$
Maximize V_{BCa}	$\mathbf{V_{BCa}} \leq 0$
Minimize $(V_{EBa} - V_{EBaON})$	$\mathbf{V_{EBa}} - \mathbf{V_{EBaON}} \geq 0$
Maximize V_{GSA}	$\mathbf{V_{GSA}} \leq V_{thA}$
Minimize $(V_{DSA} - V_{GSA})$	$\mathbf{V_{DSA}} - \mathbf{V_{GSA}} \geq -V_{thA}$
Minimize V_{GSB}	$\mathbf{V_{GSB}} \geq V_{thB}$
Maximize $(V_{DSB} - V_{GSB})$	$\mathbf{V_{DSB}} - \mathbf{V_{GSB}} \leq -V_{thB}$

If at any temperature and resistance value, for instance, V_{CBb} is below 0 or V_{BEb} is above V_{BEbON}, it can be said that BJT "b" operates in wrong region and circuit fails at that temperature and resistance value.

3.4. Solution Method

To solve the nonlinear optimization problems defined above, MATLAB (ver. R2006a) and ModeFRONTIER (MF) (ver. 4.0) softwares are used.

Note that when the variables R and T are fixed, the system of equations in Table 3.4 has a unique solution. We observed that MATLAB can quickly give this unique

solution whereas the optimization problem takes a long time in MATLAB when R and T variables change in tolerance limit. On the other hand, ModeFRONTIER can optimize the defined objective in an impressively short time by generating smart R and T values iteratively and solving the equations in MATLAB with the generated values. Hence we decided to use them sequentially, making evaluations in MATLAB and improvements in MF. The solution times for each problem vary with the complexity of the relevant objective function. However, it can be said that the maximum solution time in one V_{IN} instance is reduced to 24 minutes with the iterative use of MATLAB and MF.

Figure 3.4 shows the optimization flowchart of the problem. This optimization routine is repeated for all the objectives defined in Table 3.6.

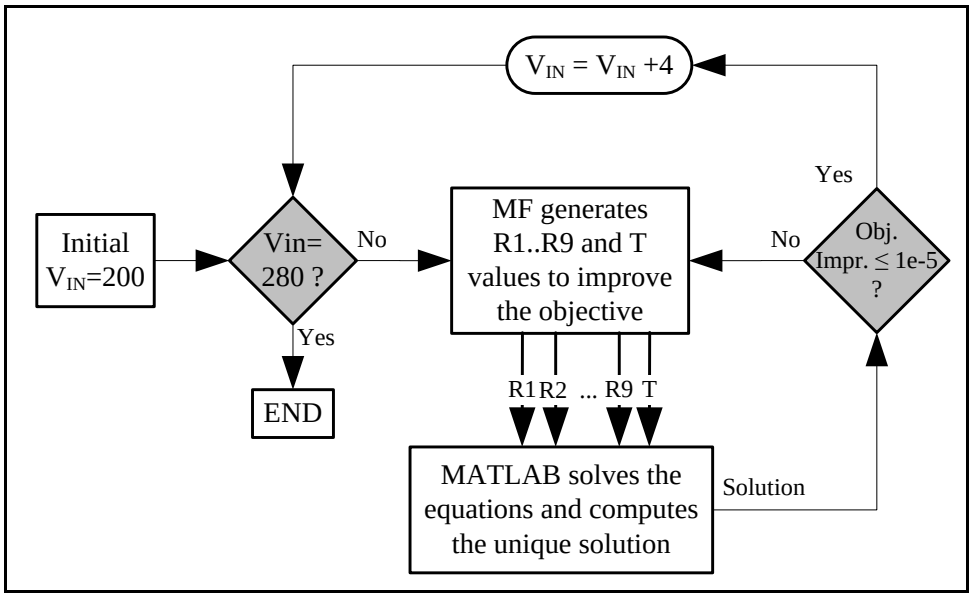

Figure 3.4. Optimization Flowchart

MATLAB is used for defining all the constant values and the constraints. Decision variables, T and R_1, $R_2 \ldots R_9$ are also defined as constants in MATLAB code. However the values of these variables are generated from MF.

The objective functions are described in MF and the software runs a pre-defined algorithm for optimization. In this study, each objective is optimized for 21 different power output (P_{out}) requirements and the optimum values in different requirements are graphically illustrated below.

To optimize each objective, MF continuously generates R and T values and runs MATLAB code in batch mode by taking into consideration the chosen algorithm. In this study since every time a single objective is optimized, SIMPLEX algorithm which is based on "Nelder & Mead Simplex method" [6] is used. This method always improves the objective value while handling non-linear equations.

Firstly the optimization of the objectives was tried to be performed in MATLAB defining $R_1 \ldots R_9$ and T values as variables and using "fmincon" function. But because of very long runtimes in MATLAB, ModeFRONTIER program, which reduces the runtime extremely, is decided to be used.

The graphical interface of MF file, "fmin.prj" is shown in Figure 3.5. T, $R_1 \ldots R_9$ and V_{IN} values are generated within this file and entered into MATLAB node. The objectives are placed in RHS. The direction of the arrow suggests if the relevant objective will be minimized or maximized and the blue arrow represents that the objective is active. MF solves the problem for the active objective with the chosen algorithm, which is SIMPLEX in our case. The active objective is sequentially changed to optimize each of the objectives.

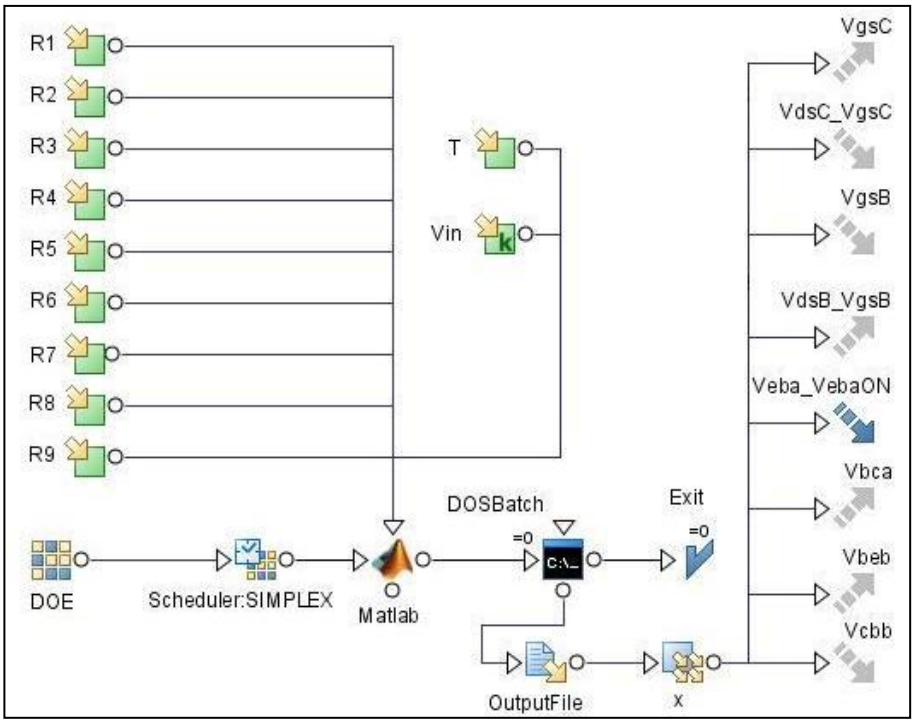

Figure 3.5. ModeFRONTIER File Graphical Interface

CHAPTER 4

WORST CASE CIRCUIT TOLERANCE ANALYSIS

In this chapter, circuit performance is examined under varying temperature and resistance values. The following sections include the optimization results of the problems defined in CHAPTER 3. The optimum values achieved for each of the objectives represent the worst case conditions for the circuit operation. In this way, it is aimed to observe that the circuit operates properly even in the worst case conditions.

4.1. Optimization Results

This section includes the results obtained by MATLAB and ModeFRONTIER softwares. The optimum values of the objectives shown in Table 3.6 are respectively supplied for the required range $50 \leq P_{out} \leq 420$ watts in figures and the binding tolerance constraints for each objective are given.

4.1.1. Minimization of V_{CBb}

Figure 4.1 shows the results for the minimization of V_{CBb} problem in P_{out} interval of 50-420 W.

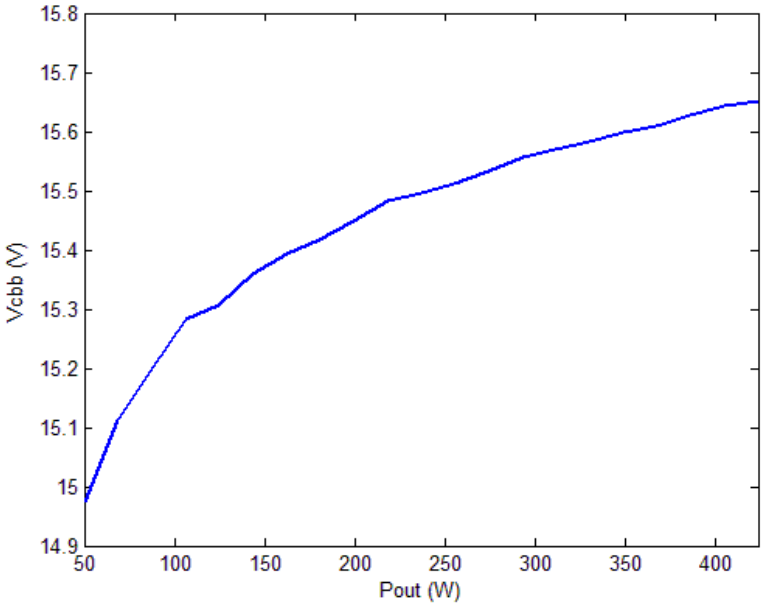

Figure 4.1. Minimized V_{CBb} vs. P_{out} Characteristics under varying T and $R_1 \ldots R_9$ variables

Recall that the check condition for V_{CBb} is $V_{CBb} \geq 0$ which is confidently fulfilled for the whole P_{out} interval. So we can say that the tolerance bands of resistors and the interval allowed for temperature is fairly satisfactory for V_{CBb}. The binding constraints are the same for whole P_{out} interval and given in Table 4.1.

Table 4.1. Binding Constraints for Min. V_{CBb}

Binding Constraint	Equality at
$1425 \leq R_4 \leq 1575$	Lower Bound
$1425 \leq R_5 \leq 1575$	Lower Bound
$1425 \leq R_6 \leq 1575$	Upper Bound
$1425 \leq R_8 \leq 1575$	Upper Bound
$28500 \leq R_9 \leq 31500$	Upper Bound
$-30 \leq T \leq 55$	Lower Bound

4.1.2. Maximization of V_{BEb}

In Figure 4.2, the results for the maximization of V_{BEb} problem are given in P_{out} interval of 50-420 W.

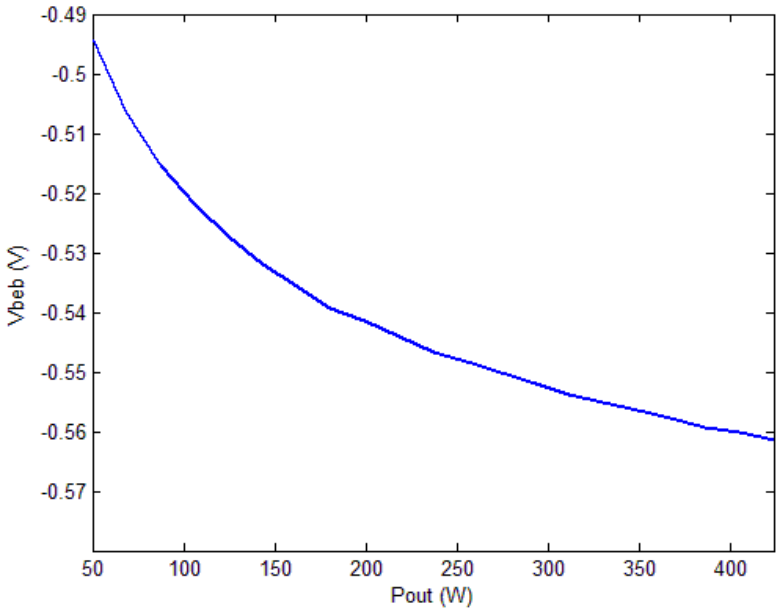

Figure 4.2. Maximized V_{BEb} vs. P_{out} Characteristics under varying T and $R_1 \ldots R_9$ variables

The check condition, which is $V_{BEb} \leq V_{BEbON}$, for V_{BEb} is, as well, met for all P_{out} requirements. Actually, V_{BEbON} value is not known and its value can be estimated from the datasheet of the transistor just like in V_{EBaON} case. However, it is known that $V_{BEbON} \geq 0$ and there is no need to know the exact value since maximized V_{BEb} values are far below 0.

Therefore, it can be said that 5% tolerance band of resistors and temperature variations do not affect the operation of BJT "b" after interpreting the V_{BEb} and V_{CBb} optimization results in any P_{out} value.

The binding constraints do not change due to P_{out} values and they are supplied in Table 4.2.

Table 4.2. Binding Constraints for Max. V_{BEb} Problem

Binding Constraint	Equality At
$1425 \leq R_4 \leq 1575$	Lower Bound
$1425 \leq R_5 \leq 1575$	Lower Bound
$1425 \leq R_6 \leq 1575$	Upper Bound
$135850 \leq R_7 \leq 150150$	Lower Bound
$1425 \leq R_8 \leq 1575$	Upper Bound
$28500 \leq R_9 \leq 31500$	Upper Bound
$-30 \leq T \leq 55$	Lower Bound

4.1.3. Maximization of V_{BCa}

Figure 4.1 shows the results for the maximization of V_{BCa} problem in P_{out} interval of 50-420 W.

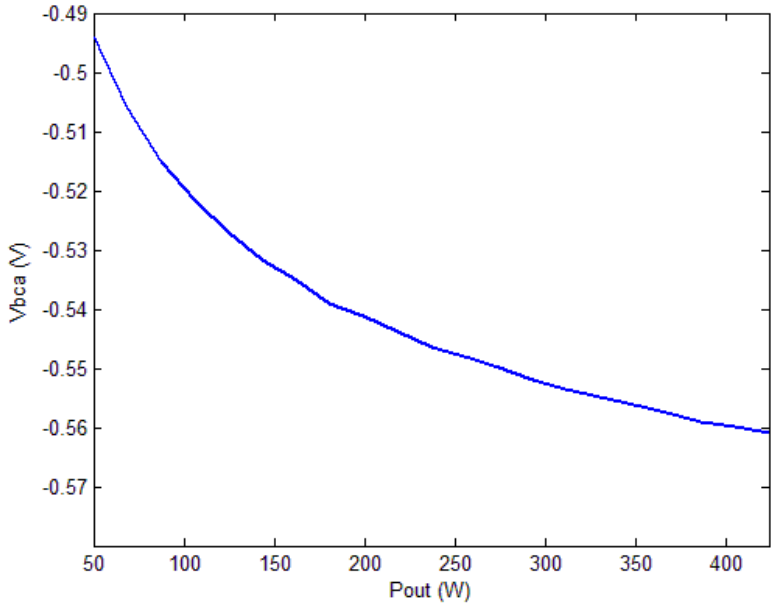

Figure 4.3. Maximized V_{BCa} vs. P_{out} Characteristics under varying T and $R_1 \ldots R_9$ variables

V_{BCa} values across the whole region P_{out} are fairly below the zero voltage. Therefore the results show that V_{BCa} stands off the limit in any resistance level combination within the tolerance band of the resistors within the allowed temperature interval.

The binding constraints are the same for whole P_{out} interval and provided in Table 4.3.

Table 4.3. Binding Constraints for Max. V_{BCa} Problem

Binding Constraint	Equality At
$1425 \leq R_4 \leq 1575$	Lower Bound
$1425 \leq R_5 \leq 1575$	Lower Bound
$1425 \leq R_6 \leq 1575$	Upper Bound
$135850 \leq R_7 \leq 150150$	Lower Bound
$1425 \leq R_8 \leq 1575$	Upper Bound
$28500 \leq R_9 \leq 31500$	Upper Bound
$-30 \leq T \leq 55$	Lower Bound

4.1.4. Minimization of (V_{EBa} - V_{EBaON})

In Figure 4.4, the results for the minimization of (V_{EBa} - V_{EBaON}) problem are given in P_{out} interval of 50-420 W.

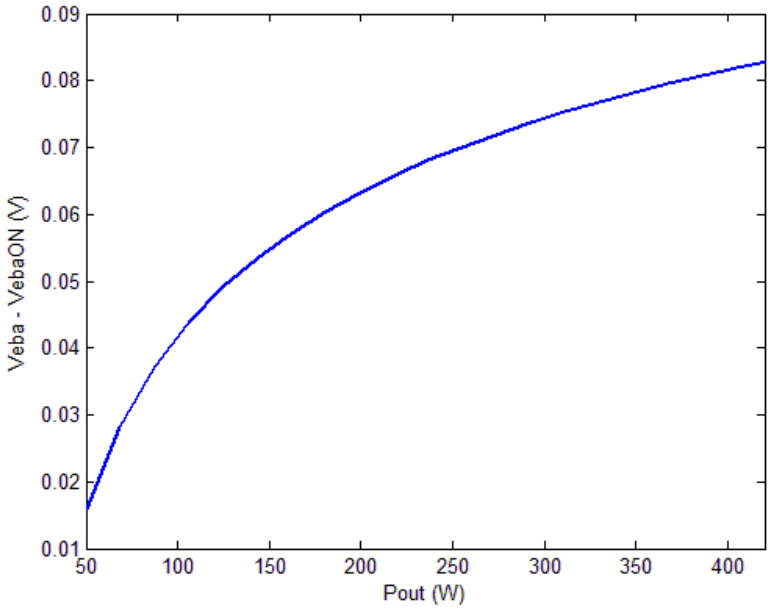

Figure 4.4. Minimized ($V_{EBa} - V_{EBaON}$) vs. P_{out} Characteristics under varying T and $R_1 \ldots R_9$ variables

Figure 2.1 admits that ($V_{EBa} - V_{EBaON}$) value, especially at low power requirement, is critically close to limit value which is zero voltage. The results show that the worst case conditions are obtained at -30 °C temperature and 50 W power requirement. Even though, it is shown that the ($V_{EBa} - V_{EBaON}$) difference stays slightly above zero, 0.017V is not a good margin for a circuit which has a very critical task. Actually there are many uncontrollable and hard-to-model factors like electromagnetic interference, aging, humidity that can cause ($V_{EBa} - V_{EBaON}$) go below zero. That is why a higher margin must be achieved. The binding constraints at 50 W and the whole P_{out} interval are included in Table 4.4.

Table 4.4. Binding Constraints for Min. ($V_{EBa} - V_{EBaON}$) Problem

Binding Constraint	Equality At
$1425 \leq R_4 \leq 1575$	Lower Bound
$1425 \leq R_5 \leq 1575$	Lower Bound
$1425 \leq R_6 \leq 1575$	Upper Bound
$1425 \leq R_8 \leq 1575$	Upper Bound
$28500 \leq R_9 \leq 31500$	Upper Bound
$-30 \leq T \leq 55$	Lower Bound

Thus, what must be done to generate a safety margin for ($V_{EBa} - V_{EBaON}$) difference is to take care of the variables included in Table 4.4. It is vital to interpret which variables are controllable and which are not. We can say that the temperature is out of our control, since the electronic circuit will be located and operated in an uncontrolled environment. However, choosing resistors with narrower tolerance band can incredibly increase the margin of ($V_{EBa} - V_{EBaON}$).

To see the significant effect of the tolerance band of resistors, the same optimization is repeated for R_4, R_5, R_6, R_8 and R_9 resistances with 1% tolerance interval. The optimum values of ($V_{EBa} - V_{EBaON}$) in P_{out} interval of 50-420W is given in Figure 4.5, where it can be figured out that the tolerance bands of R_4, R_5, R_6, R_8 and R_9 resistances have considerable effect on ($V_{EBa} - V_{EBaON}$) values. Therefore, to be confident also at low power applications and low temperature levels, R_4, R_5, R_6, R_8 and R_9 resistors must be chosen with narrower tolerance band.

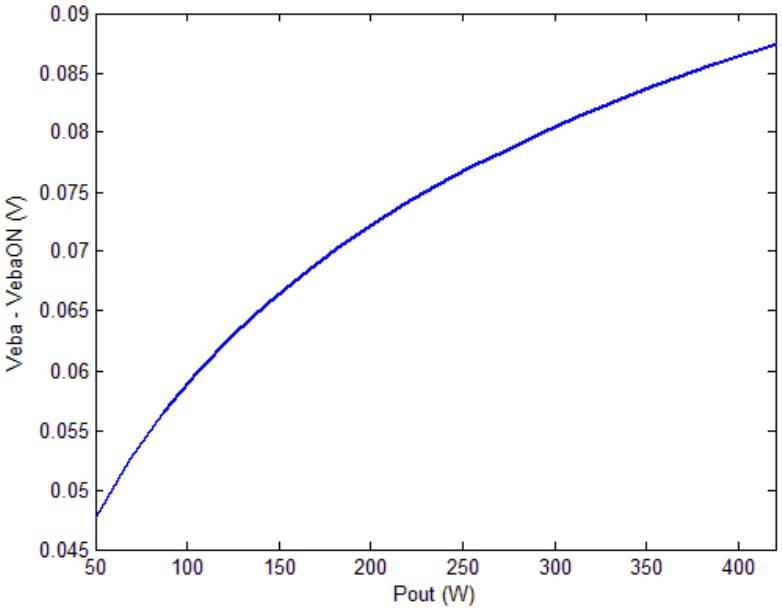

Figure 4.5. Minimized ($V_{EBa} - V_{EBaON}$) vs. P_{out} Characteristics under varying T and $R_1 \ldots R_9$ variables (R_4, R_5, R_6, R_8 and R_9 with 1% tolerance band)

4.1.5. Maximization of V_{GSA}

Figure 4.6 shows the results for the maximization of V_{GSA} problem in P_{out} interval of 50-420 W.

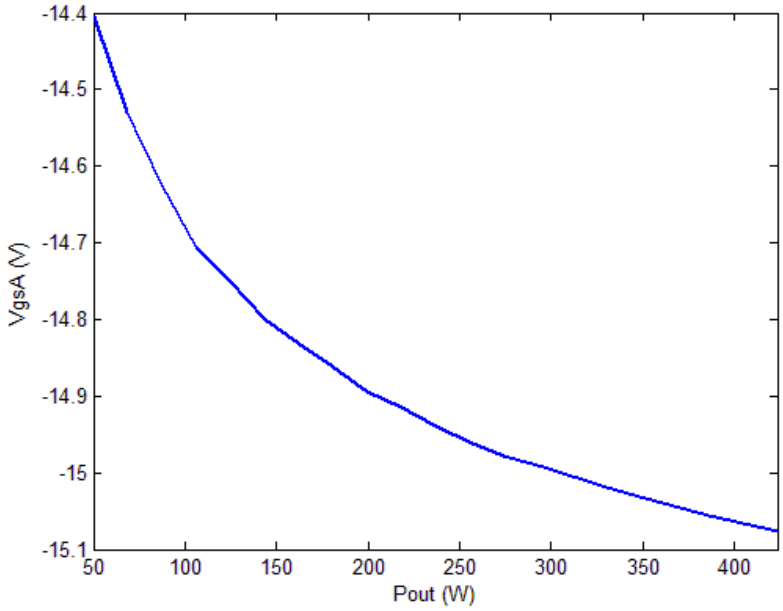

Figure 4.6. Maximized V_{GSA} vs. P_{out} Characteristics under varying T and $R_1 \ldots R_9$ variables

From Figure 4.6 it can be concluded that V_{GSA} is not affected from resistance temperature variations. Its worst case value -14.405, is far below threshold voltage of MOSFET "A", V_{thA} which is equal to -4.5V. The binding constraints are the same for whole P_{out} interval and provided in Table 4.5.

Table 4.5. Binding Constraints for Max. V_{GSA} Problem

Binding Constraint	Equality At
$1425 \leq R_4 \leq 1575$	Lower Bound
$1425 \leq R_5 \leq 1575$	Lower Bound
$1425 \leq R_6 \leq 1575$	Upper Bound
$1425 \leq R_8 \leq 1575$	Upper Bound
$28500 \leq R_9 \leq 31500$	Upper Bound
$-30 \leq T \leq 55$	Upper Bound

4.1.6. Minimization of (V_{DSA} - V_{GSA})

In Figure 4.7, the results for the minimization of ($V_{DSA} - V_{GSA}$) problem are given in P_{out} interval of 50-420 W.

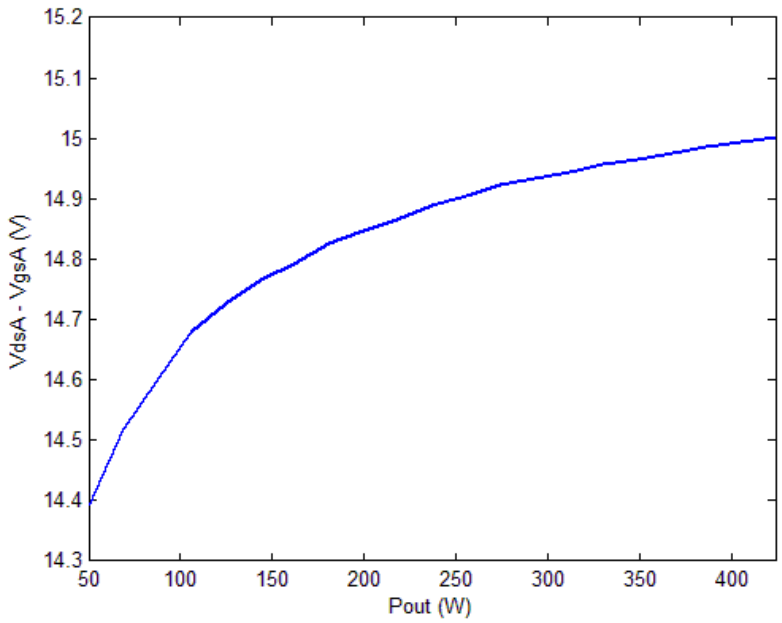

Figure 4.7. Minimized (V_{DSA}-V_{GSA}) vs. P_{out} Characteristics under varying T and R_1…R_9 variables

Figure 4.7 shows that even the worst case (V_{DSA}-V_{GSA}) value is confidently above the minus threshold voltage of MOSFET "A" (-V_{thA}=4.5 V). Thus, taking into account this result and the one obtained from V_{GSA} maximization, it can be said that MOSFET "A" is highly compatible to resistance and temperature variations.

In Table 4.6, binding constraints for maximization of (V_{DSA}-V_{GSA}) is given.

Table 4.6. Binding Constraints for Max. (V_{DSA}-V_{GSA}) Problem

Binding Constraint	Equality At
$1425 \leq R_4 \leq 1575$	Lower Bound
$1425 \leq R_5 \leq 1575$	Lower Bound
$1425 \leq R_6 \leq 1575$	Upper Bound
$1425 \leq R_8 \leq 1575$	Upper Bound
$28500 \leq R_9 \leq 31500$	Upper Bound
$-30 \leq T \leq 55$	Upper Bound

4.1.7. Minimization of V_{GSB}

Figure 4.8 shows the results for the minimization of V_{GSB} problem in P_{out} interval of 50-420 W.

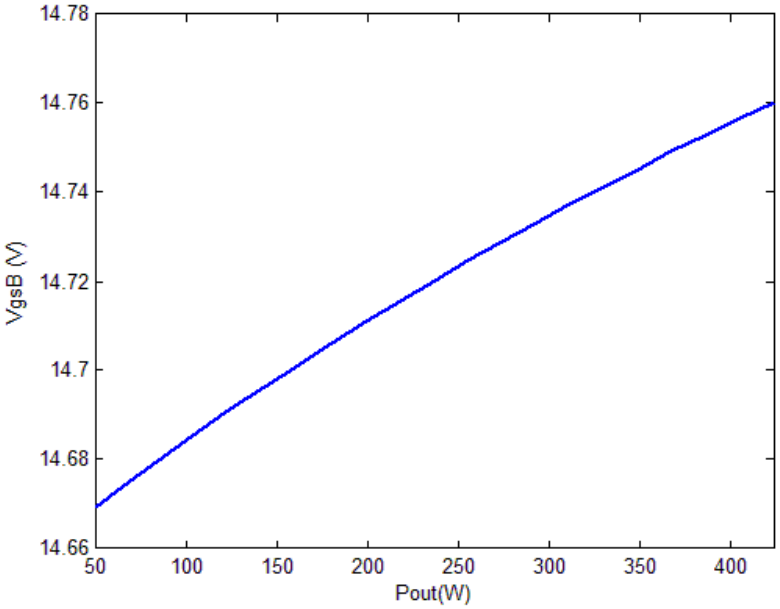

Figure 4.8. Minimized V_{GSB} vs. P_{out} Characteristics under varying T and R_1…R_9 variables

V_{GSB}, as well, is confidently consistent with its check condition, which is "$V_{GSB} \geq V_{thB}$" where V_{thB} = 4.5V. Thus the results show that V_{GSB} is compatible with the whole interval of resistance and temperature values.

Table 4.7 includes the binding constraints for maximization of V_{GSB} problem.

Table 4.7. Binding Constraints for Max. V_{GSB} Problem

Binding Constraint	Equality At
$474050 \leq R_1 \leq 523950$	Upper Bound
$1425 \leq R_2 \leq 1575$	Upper Bound
$1425 \leq R_3 \leq 1575$	Upper Bound
$135850 \leq R_7 \leq 150150$	Lower Bound

4.1.8. Maximization of (V_{DSB} - V_{GSB})

In Figure 4.7, the results for the maximization of ($V_{DSB} - V_{GSB}$) problem are given in P_{out} interval of 50-420 W.

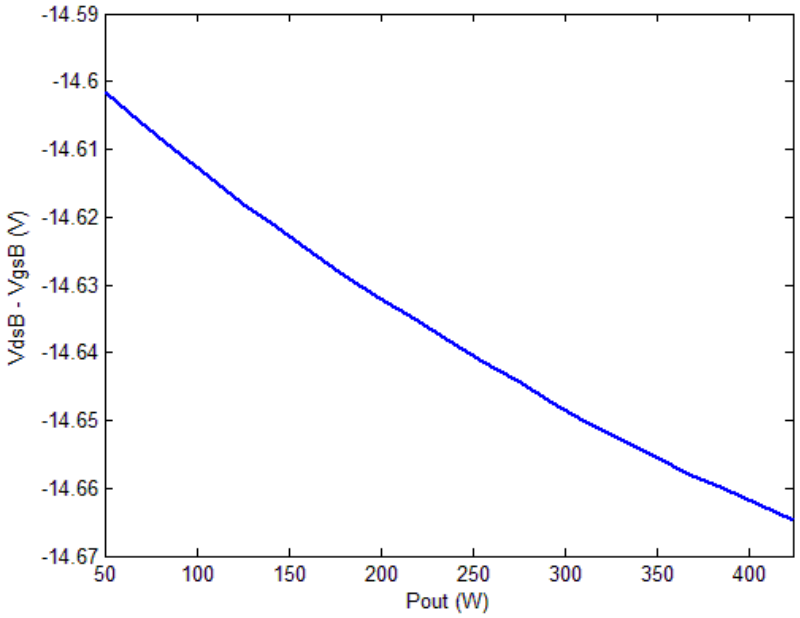

Figure 4.9. Maximized (V_{DSB} - V_{GSB}) vs. P_{out} Characteristics under varying T and $R_1 \ldots R_9$ variables

Figure 4.9 indicates that (V_{DSB} - V_{GSB}) objective also holds its check condition (V_{DSB} - V_{GSB}) ≤ -V_{thB}. Therefore, taking into consideration the optimization results of V_{GSB} and (V_{DSB} - V_{GSB}), it can be concluded that MOSFET "B" operates in the right region within the tolerance band of resistors and the temperature variations.

The binding constraints for maximization of (V_{DSB} - V_{GSB}) are included in Table 4.8.

Table 4.8. Binding Constraints for Max. V_{GSB} Problem

Binding Constraint	Equality At
$474050 \leq R_1 \leq 523950$	Upper Bound
$1425 \leq R_2 \leq 1575$	Upper Bound
$1425 \leq R_3 \leq 1575$	Upper Bound
$1425 \leq R_6 \leq 1575$	Lower Bound
$135850 \leq R_7 \leq 150150$	Lower Bound
$1425 \leq R_8 \leq 1575$	Lower Bound
$28500 \leq R_9 \leq 31500$	Lower Bound

4.2. Interpretation of Optimization Results

The optimization results show that under varying T and $R_1 \ldots R_9$ variables all the check conditions hold in any P_{out} value in the interval of 50-420 watts. While some objectives like (V_{EBa} - V_{EBaON}) are slightly above or below their limit, some are confidently consistent with their check conditions.

When dealing with the results component by component, it can be said that BJT "a" has the most critical condition, by means of its (V_{EBa} - V_{EBaON}) voltage. To apply a meaningful safety margin for that voltage level, R_4, R_5, R_6, R_8 and R_9 resistors must be replaced with their identical parts with 1% tolerance band.

The voltage levels of BJT "b", MOSFET "A" and MOSFET "B" have enough safety margin from their critical value, thus we can conclude that these components are highly compatible to temperature variations between -30°C / 55°C and 5% tolerance band of the resistors.

Table 4.9 shows the optimum values of each objective including the P_{out} and T values. It can easily be observed that all the optimum values are obtained at P_{out} of 50W. Therefore, special attention must be drawn upon low powered operations. It is more probable for the circuit to fail in low powered operations.

Unlike P_{out} values, temperature values are not always the same at optimum values of all objectives. However, the temperature at the optimum value of the most critical voltage, (V_{EBa} - V_{EBaON}) is found to be -30°C, which therefore can be assumed to be the most critical temperature value.

Table 4.9. P_{out} and T Values at Optimum Value of Each Objective

Objective	Check Condition	Optimum Value	P_{out} at Optimum Value	T at Optimum Value
Min. V_{BCb}	$V_{BCb} \geq 0$	14.9740	50	-30
Max. V_{BEb}	$V_{BEb} \leq 0$	-0.4943	50	-30
Max. V_{BCa}	$V_{BCa} \leq 0$	-0.4940	50	-30
Min. V_{EBa} - V_{EBaON}	V_{EBa} - $V_{EBaON} \geq 0$	0.01632	50	-30
Max. V_{GSA}	$V_{GSA} \leq 0$	-14.4050	50	55
Min. V_{DSA}-V_{GSA}	V_{DSA}-$V_{GSA} \geq 0$	14.3920	50	55
Min. V_{GSB}	$V_{GSB} \geq 0$	14.6691	50	Not binding
Max. V_{DSB}-V_{GSB}	V_{DSB}-$V_{GSB} \leq 0$	-14.6023	50	Not binding

CHAPTER 5

FAILURE MODES AND EFFECTS ANALYSIS

Each electronic component has a possibility of failing and the mechanisms of these failures vary from component to component. Most common failures are short circuit and open circuit failures which are the primary causes of the failures for most of the components. Other failures cover drift, parameter change, intermittent connection etc.. However, the failures which affect the circuit operation in the worst manner are the short and open circuit failures.

In this study, the effects of open circuit and short circuit failures of all the components in FPDC will be examined. Some failures do not affect the circuit operation at all, while some may cause catastrophic circuit failure. To examine the effects of each failure, tolerance analysis is carried out when necessary. Yet the effects of some failures are so obvious that they can be figured out at a glance on the circuit scheme. Thus; no further analyses are needed for the failures whose effect can be obviously realized. In this study, only the failures whose effect cannot be obviously figured out are handled.

In this section, primarily brief information about short circuit and open circuit failures is given and then the effects of short and open circuit failures of each component used in the circuit are analyzed.

5.1. Short Circuit Failure

When a component undergoes a short circuit failure, an extremely low resistance is observed between its terminals and the component acts simply like a wire. So while analyzing the short circuit failure of a component, whatever its type is, the component will be bypassed with simple wire across its terminals. The effect of this failure will be analyzed with MATLAB and ModeFRONTIER, when necessary.

5.2. Open Circuit Failure

This failure causes an unexpected disconnection between the terminals of a component. When an open circuit failure happens in a component, no current passes through it and the path including the component acts like a cut wire.

This, as well, is a very important type of failure and can happen in most of the components. While analyzing the open circuit failure, the current through the relevant path is assumed to be zero and the effect of the failure will be again examined with MATLAB and Mode FRONTIER over the whole region of V_{IN}, when necessary.

5.3. FMEA Matrix

There are a total number of 18 electronic components in FPDC. Investigating the short circuit and open circuit failures of each component by MATLAB and ModeFRONTIER softwares takes extremely long time. Hence, it is unnecessary to perform the analysis for the failures whose effect is obvious and can be realized without any computation.

In this section, a matrix which includes the failures of each component and their effects is given. In this matrix, the failures that need a computational analysis are also shown.

Table 5.1. Short and Open Circuit Failures Examination

Component	Open Circuit Failure Effects	Short Circuit Failure Effects
R_1	Circuit Fails	Computational Analysis Needed
R_2	Circuit Fails	Computational Analysis Needed
R_3	Circuit Fails	Computational Analysis Needed
R_4	Circuit Fails	Computational Analysis Needed
R_5	Circuit Fails	Computational Analysis Needed
R_6	Circuit Fails	Computational Analysis Needed
R_7	Computational Analysis Needed	Circuit Fails
R_8	Circuit Fails	Computational Analysis Needed
R_9	Circuit Fails	Computational Analysis Needed
C_1	Circuit Continues Proper Operation	Circuit Fails
C_2	Circuit Continues Proper Operation	Computational Analysis Needed (Same analysis with R_1 short circuit failure analysis)
C_3	Circuit Continues Proper Operation	Computational Analysis Needed (Same analysis with R_9 short circuit failure analysis)
Z_1	Computational Analysis Needed	Circuit Fails
Z_2	Computational Analysis Needed	Circuit Fails
BJT “a”	Circuit Fails	Circuit operates properly in short circuited B-E failure, fails in short circuited B-C and E-C failures
BJT “b”	Circuit Fails	Circuit Fails
MOSFET “A”	Circuit Continues Proper Operation	Circuit Fails
MOSFET “B”	Circuit Fails	Circuit Fails

Table 5.1 lists the necessary computation analyses by showing the effects of each failure. As can be figured out from that figure, the effect of some failures can be easily recognized by inspection and does not require computational analysis. Next we examine the failures that require computational analysis to see their effects.

There are some identical failures whose analyses and effects are exactly the same. These identical failures involve the short circuit failure of R_1 and C_2, plus the short circuit failure of R_9 and C_3. With this additional information, the required computational analyses that will be carried out are listed in Table 5.2.

Table 5.2. Failures That Will Be Analyzed Computationally

#	Failure Analysis
1	Short Circuit Failure of R_1 (identical with short circuit failure of C_2)
2	Short Circuit Failure of R_2
3	Short Circuit Failure of R_3
4	Short Circuit Failure of R_4
5	Short Circuit Failure of R_5
6	Short Circuit Failure of R_6
7	Open Circuit Failure of R_7
8	Short Circuit Failure of R_8
9	Short Circuit Failure of R_9 (identical with short circuit failure of C_3)
10	Open Circuit Failure of Z_1
11	Open Circuit Failure of Z_2

To perform each failure analysis, the modifications arising from the relevant failure must be reflected into circuit equations.

To reflect the short circuit failure of a resistor, we set the resistance to zero. Similarly, the resistance of the failed resistor is set to infinity to simulate the open circuit failure of a resistor.

To simulate the effects of open circuit failure of the zener diodes, Z_1 and Z_2, we set the zener currents, I_{z1} and I_{z2} to zero. While carrying out failure analysis, one extra objective for each zener diode failure is optimized to check if they remain in the allowed interval. New objectives and their check conditions are shown in Table 5.3.

Table 5.3. New Objectives, When to Use and Their Check Conditions

No.	Objective Function	When Used?	Check Condition
9)	Minimize V_{GSA}	In Open Circuit Failure of Z_1	$V_{GSA} \geq V_{GSAmax}$ (= -20 V)
10)	Maximize V_{GSB}	In Open Circuit Failure of Z_2	$V_{GSB} \leq V_{GSBmax}$ (= 30 V)

Actually; V_{GSA} and V_{GSB}, were optimized before, however these terms are now optimized in both directions, i.e. V_{GSA} was maximized in Section 4.1.5, in this section additionally it is minimized. Similarly, V_{GSB} was minimized in Section 4.1.7, in this section additionally it is maximized. The aim to perform these two extra analyses is to check if V_{GS} voltages go beyond their absolute maximum voltage ratings, both of which are included in the datasheets of the parts. According to these datasheets, V_{GSAmax} is -20 V and V_{GSBmax} iso 30 V. These voltages are not checked in CHAPTER 4, because of the protective behavior of the zener diodes. In their normal operation, zener diodes protect MOSFET "A" and MOSFET "B" from excessive gate-source voltages by limiting V_{GSA} and V_{GSB} voltages below their maximum ratings. The failure of the zener diodes requires checking the maximum (or minimum) V_{GS} voltages.

The analysis is fairly different than that performed in CHAPTER 4. In this section, instead of examining the transistor voltages in $200 \leq V_{IN} \leq 280$ V interval, V_{IN} is let as a variable to be determined by the model. Thus the optimum voltages obtained reflect the worst case conditions in the whole V_{IN} interval.

5.4. FMEA Results

In this section, the results of open and short circuit failures are provided. While performing analyses to see the effects, the objectives are not optimized at discrete P_{out} instances. Instead, P_{out} is also taken as a variable and varying between 50 and 420 watts. Thus, the optimum values include P_{out} values, which form the worst case condition.

5.4.1. Short Circuit Failure of R_1

Results shown in Table 5.4 suggest that the short circuit failure of R_1 does not affect the circuit operation seriously.

Table 5.4. Short Circuit Failure Effect of R_1

Objective	Optimum Value	Check Condition
Min. V_{BCb}	14.985	$V_{BCb} \geq 0$
Max. V_{BEb}	-0.494	$V_{BEb} \leq 0$
Max. V_{BCa}	-0.496	$V_{BCa} \leq 0$
Min. V_{EBa} - V_{EBaON}	0.01598	V_{EBa} - $V_{EBaON} \geq 0$
Max. V_{GSA}	-14.398	$V_{GSA} \leq 0$
Min. V_{DSA}-V_{GSA}	14.385	V_{DSA}-$V_{GSA} \geq 0$
Min. V_{GSB}	15.704	$V_{GSB} \geq 0$
Max. V_{DSB}-V_{GSB}	-15.643	V_{DSB}-$V_{GSB} \leq 0$

Simulation of the short circuit failure of R_1 is performed in MF by changing the resistance of R_1 to "0" which implies that R_1 has failed and acts like a short circuit.

Even if this failure does not affect the circuit operation seriously, it affects the circuit elements by loading stress on them in terms of power, voltage or current. Short circuit failure of R_1 causes current that flows through R_2 and R_3 increase and loads more power stress on the resistances, R_2 and R_3. More stress the component operates under; more probably it faces with a failure.

Furthermore, it must be noted that the short circuit failure of C_2 shows the same effect with the short circuit failure of R_1 since they are connected in parallel in the circuit scheme. Therefore, the short circuit failure of either R_1 or C_2 causes the current flow through the short circuited path and bypasses the other component in parallel. Thus the non-defect component becomes unfunctional when the component in parallel becomes short circuit.

5.4.2. Short Circuit Failure of R_2

Table 5.5 includes the results of short circuit failure analysis of R_2. It can be easily seen that all the check conditions are satisfied and the short circuit failure of R_2 does not affect the circuit operation seriously.

Table 5.5. Short Circuit Failure Effect of R_2

Objective	Optimum Value	Check Condition
Min. V_{BCb}	15.014	$V_{BCb} \geq 0$
Max. V_{BEb}	-0.497	$V_{BEb} \leq 0$
Max. V_{BCa}	-0.496	$V_{BCa} \leq 0$
Min. V_{EBa} - V_{EBaON}	0.01590	V_{EBa} - $V_{EBaON} \geq 0$
Max. V_{GSA}	-14.404	$V_{GSA} \leq 0$
Min. V_{DSA}-V_{GSA}	14.384	V_{DSA}-$V_{GSA} \geq 0$
Min. V_{GSB}	14.671	$V_{GSB} \geq 0$
Max. V_{DSB}-V_{GSB}	-14.604	V_{DSB}-$V_{GSB} \leq 0$

Moreover, the short circuit failure of R_2 does not load stress on the other electronic components in the circuit since the resistance value of R_2 is very small when compared to R_1, which is connected in series with R_1 in the circuit. So neither directly nor indirectly, the short circuit failure of R_2 affects the circuit operation.

5.4.3. Short Circuit Failure of R_3

The effect of the short circuit failure of R_3 can be followed from Table 5.6. Like in the short circuit failure of R_2, all the check conditions hold in this failure. Thus, it can be concluded that the short circuit failure of R_3 does not affect the circuit operation seriously.

Table 5.6. Short Circuit Failure Effect of R_3

Objective	Optimum Value	Check Condition
Min. V_{BCb}	15.014	$V_{BCb} \geq 0$
Max. V_{BEb}	-0.497	$V_{BEb} \leq 0$
Max. V_{BCa}	-0.496	$V_{BCa} \leq 0$
Min. V_{EBa} - V_{EBaON}	0.01590	V_{EBa} - $V_{EBaON} \geq 0$
Max. V_{GSA}	-14.404	$V_{GSA} \leq 0$
Min. V_{DSA}-V_{GSA}	14.384	V_{DSA}-$V_{GSA} \geq 0$
Min. V_{GSB}	14.671	$V_{GSB} \geq 0$
Max. V_{DSB}-V_{GSB}	-14.604	V_{DSB}-$V_{GSB} \leq 0$

Since R_3 is connected in series with R_1 whose resistance is very large when compared to R_3, the short circuit failure of R_3 does not load stress on the other electronic components in the circuit. Therefore, the short circuit failure of R_1 does not affect the circuit operation indirectly, either.

5.4.4. Short Circuit Failure of R_4

Table 5.7 shows that the short circuit failure of R_4 fails the whole circuit operations since the check conditions for three of the objectives are not met. From this table, it can be concluded that BJT “a” and BJT “b” cannot operate at their desired region, which is saturation for BJT “b” and cut-off for BJT “a”. The reason why the circuit fails when R_4 shows short circuit failure is that this resistor has a very critical location in the circuit, R_4 and R_5 together set the operation regions of BJT “a” and BJT “b”. Thus, the failure of either R_4 or R_5 causes a catastrophic failure in FPDC.

Table 5.7. Short Circuit Failure Effect of R_4

Objective	Optimum Value	Check Condition
Min. V_{BCb}	7.899	$V_{BCb} \geq 0$
Max. V_{BEb}	4.252	$V_{BEb} \leq 0$ **(X)**
Max. V_{BCa}	7.174	$V_{BCa} \leq 0$ **(X)**
Min. $V_{EBa} - V_{EBaON}$	-4.538	$V_{EBa} - V_{EBaON} \geq 0$ **(X)**
Max. V_{GSA}	-7.605	$V_{GSA} \leq 0$
Min. V_{DSA}-V_{GSA}	7.562	V_{DSA}-$V_{GSA} \geq 0$
Min. V_{GSB}	14.669	$V_{GSB} \geq 0$
Max. V_{DSB}-V_{GSB}	-14.601	V_{DSB}-$V_{GSB} \leq 0$

5.4.5. Short Circuit Failure of R_5

When the circuit scheme of FPDC is reviewed, it can easily be observed that R_4 and R_5 are identical since they have the same resistance and are connected in series. Therefore, the short circuit failure of R_5 has the same effect on the circuit operation as R_4. Table 5.8 shows that BJT "a" and BJT "b" cannot operate at their desired region, as well when the short circuit failure of R_5 occurs. Thus, R_5 also causes a catastrophic failure in FPDC.

Table 5.8. Short Circuit Failure Effect of R_5

Objective	Optimum Value	Check Condition
Min. V_{BCb}	7.899	$V_{BCb} \geq 0$
Max. V_{BEb}	4.252	$V_{BEb} \leq 0$ **(X)**
Max. V_{BCa}	7.174	$V_{BCa} \leq 0$ **(X)**
Min. $V_{EBa} - V_{EBaON}$	-4.538	$V_{EBa} - V_{EBaON} \geq 0$ **(X)**
Max. V_{GSA}	-7.605	$V_{GSA} \leq 0$
Min. V_{DSA}-V_{GSA}	7.562	V_{DSA}-$V_{GSA} \geq 0$
Min. V_{GSB}	14.669	$V_{GSB} \geq 0$
Max. V_{DSB}-V_{GSB}	-14.601	V_{DSB}-$V_{GSB} \leq 0$

5.4.6. Short Circuit Failure of R_6

Table 5.9 includes the optimum values of the objectives when the short circuit failure of R_6 occurs. It can easily be figured out that this failure does not affect the circuit operation seriously.

Table 5.9. Short Circuit Failure Effect of R_6

Objective	Optimum Value	Check Condition
Min. V_{BCb}	15.203	$V_{BCb} \geq 0$
Max. V_{BEb}	-0.516	$V_{BEb} \leq 0$
Max. V_{BCa}	-0.516	$V_{BCa} \leq 0$
Min. V_{EBa} - V_{EBaON}	0.03849	V_{EBa} - $V_{EBaON} \geq 0$
Max. V_{GSA}	-14.644	$V_{GSA} \leq 0$
Min. V_{DSA}-V_{GSA}	14.679	V_{DSA}-$V_{GSA} \geq 0$
Min. V_{GSB}	14.669	$V_{GSB} \geq 0$
Max. V_{DSB}-V_{GSB}	-14.601	V_{DSB}-$V_{GSB} \leq 0$

Since R_6 is connected in series with R_9 whose resistance is very large when compared to R_6, the short circuit failure of R_9 does not load stress on the other electronic components in the circuit. Therefore; the short circuit failure of R_9 does not affect the circuit operation indirectly, either.

5.4.7. Open Circuit Failure of R_7

Different from the other resistors, the short circuit failure of R_7 does not require computational analysis. Instead, computational analysis is needed in the open circuit failure R_7 and its effects are presented in this part.

The motivation for analyzing the open circuit failure of R_7 is the parallel connected elements in the circuit. Thus, the effect of its open circuit condition is not easy to observe. However, it can easily be observed that the short circuit failure of R_7 fails the circuit operation by conditioning MOSFET “B” to Cut-Off region, which is the undesired operating region for this transistor.

Table 5.10. Open Circuit Failure Effect of R_7

Objective	Optimum Value	Check Condition
Min. V_{BCb}	15.011	$V_{BCb} \geq 0$
Max. V_{BEb}	-0.497	$V_{BEb} \leq 0$
Max. V_{BCa}	-0.496	$V_{BCa} \leq 0$
Min. V_{EBa} - V_{EBaON}	0.01596	V_{EBa} - $V_{EBaON} \geq 0$
Max. V_{GSA}	-14.405	$V_{GSA} \leq 0$
Min. V_{DSA}-V_{GSA}	14.384	V_{DSA}-$V_{GSA} \geq 0$
Min. V_{GSB}	15.001	$V_{GSB} \geq 0$
Max. V_{DSB}-V_{GSB}	-14.906	V_{DSB}-$V_{GSB} \leq 0$

Table 5.10 shows the effects of the open circuit failure of R_7. From the table, it can be observed that this failure neither affect the circuit operation seriously, nor it loads stress on the other components. The reason why the open circuit failure of R_7 does not seem to affect any component in FPDC is the zener diode Z_2 connected in parallel. Z_2 compensates the open circuit failure of the resistor by letting more current pass through its terminals. Yet, the increased current through Z_2 still remains too low from its absolute maximum current rating. Thus, it can be concluded that the open circuit failure of R_7 does not affect the circuit operation directly or indirectly.

5.4.8. Short Circuit Failure of R_8

The results obtained for the short circuit failure of R_8 is shown in Table 5.11. It can easily be seen that this failure does not fail FPDC. Since both R_6 and R_8 have the same resistance and connected in series, it is natural to obtain the same results for their short circuit failure. Not to mention, R_8 does not either load stress on the other electronic components.

Table 5.11. Short Circuit Failure Effect of R_8

Objective	Optimum Value	Check Condition
Min. V_{BCb}	15.203	$V_{BCb} \geq 0$
Max. V_{BEb}	-0.516	$V_{BEb} \leq 0$
Max. V_{BCa}	-0.516	$V_{BCa} \leq 0$
Min. V_{EBa} - V_{EBaON}	0.03849	V_{EBa} - $V_{EBaON} \geq 0$
Max. V_{GSA}	-14.644	$V_{GSA} \leq 0$
Min. V_{DSA}-V_{GSA}	14.679	V_{DSA}-$V_{GSA} \geq 0$
Min. V_{GSB}	14.669	$V_{GSB} \geq 0$
Max. V_{DSB}-V_{GSB}	-14.601	V_{DSB}-$V_{GSB} \leq 0$

5.4.9. Short Circuit Failure of R_9

Table 5.12 shows that the check conditions for all the objectives hold in the short circuit failure of R_9. So it can be said that this failure does not affect the circuit operation seriously. However, short circuit failure of R_9 loads stress on R_6 and R_8, which are connected in series with R_9 since the current is increased as a result of the reduced resistance on the path. Thus, in the consequence of the increased current, more power is loaded on the series resistors, R_6 and R_8.

Table 5.12. Short Circuit Failure Effect of R_9

Objective	Optimum Value	Check Condition
Min. V_{BCb}	16.315	$V_{BCb} \geq 0$
Max. V_{BEb}	-0.6285	$V_{BEb} \leq 0$
Max. V_{BCa}	-0.62795	$V_{BCa} \leq 0$
Min. V_{EBa} - V_{EBaON}	0.15048	V_{EBa} - $V_{EBaON} \geq 0$
Max. V_{GSA}	-15.685	$V_{GSA} \leq 0$
Min. V_{DSA}-V_{GSA}	15.673	V_{DSA}-$V_{GSA} \geq 0$
Min. V_{GSB}	14.669	$V_{GSB} \geq 0$
Max. V_{DSB}-V_{GSB}	-13.654	V_{DSB}-$V_{GSB} \leq 0$

Furthermore, it must be noted that the short circuit failure of C_3 shows the same effect with the short circuit failure of R_9 since they are connected in parallel in the circuit scheme. Since the short circuit failure of either R_9 or C_3 causes the current flow through the short circuited path and bypasses the other component in parallel, the non-defect component becomes unfunctional when the component in parallel becomes short circuit.

5.4.10. Open Circuit Failure of Z_1

In FPDC, the zener diodes have very critical task, which is limiting the gate voltages (V_{GS}) of the MOSFET's. The need to limit the gate voltages arise from the absolute maximum voltage ratings of the MOSFET's. In FPDC, Z_1 limits V_{GSA} voltage below the minus of its zener voltage which is around 15 V. For MOSFET "A" to operate properly, V_{GSA} must stay above "-20 V", which is the absolute maximum rating for its gate voltage. Thus; in addition to all the objectives used so far, one more objective which is "minimize V_{GSA}" has to be included to check V_{GSA} stay above -20V.

Table 5.13 includes the objective functions, the optimum values for the objectives and their check conditions. It can easily be observed that the open circuit failure of Z_1 fails FPDC by violating two of the check conditions.

This failure prevents BJT "a" to operate at its desired region by driving emitter-to-base voltage, V_{EBa} out of its limit for saturation region, below V_{EBaON}.

Furthermore; the open circuit failure of Z_1 fails MOSFET "A" by causing V_{GSA} go below $V_{GSA\text{-}max}$, which is -20 V. Therefore; even though V_{GSA} and (V_{DSA}-V_{GSA}) voltages obey their limits for triode region, MOSFET "A" fails since it exceeds its maximum gate voltage rating.

Thus, open circuit failure of Z_1 has catastrophic effect on the circuit operation and preventive actions must be taken in order to make FPDC more robust.

Table 5.13. Open Circuit Failure Effect of Z_1

Objective	Optimum Value	Check Condition
Min. V_{BCb}	15.204	$V_{BCb} \geq 0$
Max. V_{BEb}	-0.20402	$V_{BEb} \leq 0$
Max. V_{BCa}	-0.20402	$V_{BCa} \leq 0$
Min. V_{EBa} - V_{EBaON}	-0.17119	V_{EBa} - $V_{EBaON} \geq 0$ **(X)**
Max. V_{GSA}	-14.894	$V_{GSA} \leq 0$
Min. V_{DSA}-V_{GSA}	14.887	V_{DSA}-$V_{GSA} \geq 0$
Min. V_{GSB}	14.669	$V_{GSB} \geq 0$
Max. V_{DSB}-V_{GSB}	-14.603	V_{DSB}-$V_{GSB} \leq 0$
Min. V_{GSA}	-25.298	$V_{GSA} \geq V_{GSA\text{-}max}$ (= -20) **(X)**

5.4.11. Open Circuit Failure of Z_2

Z_2 operates in a similar manner with Z_1 in the way that it limits the gate voltage of MOSFET "B" below its zener voltage, which is around 15 V. In the open circuit failure analysis of Z_2, the objective "Minimize V_{GSB}" is included, whose optimum solution is used to check if the gate voltage of MOSFET "B" exceed its maximum rating, which is 30 V.

The analysis results are given in Table 5.14. The obtained results are very interesting in the way that the first eight objectives hold their check conditions, whereas "Minimize V_{GSB}" objective fails its condition. This suggests that even though the open circuit failure of Z_2 does not affect the transistor voltages and does not violate their operating regions, it loads stress on MOSFET "B" and causes it fail. Thus, open circuit failure of Z_2 has catastrophic effects on the circuit operation and preventive actions must be taken in order to make FPDC more robust.

Table 5.14. Open Circuit Failure Effect of Z_2

Objective	Optimum Value	Check Condition
Min. V_{BCb}	14.976	$V_{BCb} \geq 0$
Max. V_{BEb}	-0.4971	$V_{BEb} \leq 0$
Max. V_{BCa}	-0.4953	$V_{BCa} \leq 0$
Min. V_{EBa} - V_{EBaON}	0.01608	V_{EBa} - $V_{EBaON} \geq 0$
Max. V_{GSA}	-14.412	$V_{GSA} \leq 0$
Min. V_{DSA}-V_{GSA}	14.434	V_{DSA}-$V_{GSA} \geq 0$
Min. V_{GSB}	40.991	$V_{GSB} \geq 0$
Max. V_{DSB}-V_{GSB}	-40.977	V_{DSB}-$V_{GSB} \leq 0$
Min. V_{GSB}	67.041	$V_{GSB} \leq V_{GSB\text{-}max}$ (=30) **(X)**

5.5. Interpretation of FMEA Results

In this chapter, short and open circuit failures of each component and their effects to the circuit operation are investigated. The results show that there are some critical circuit elements, whose effect is catastrophic. In this section, FMEA Matrix in Table 5.1 will be revised with respect to the analysis results and the possible preventive actions to eliminate the effects of catastrophic failures will be suggested.

Table 5.15 lists the effects of each failure, including the ones which need computational analysis.

Table 5.15. Revised FMEA Matrix

Component	Open Circuit Failure Effects	Short Circuit Failure Effects
R_1	Circuit Fails	Circuit Continues Proper Operation
R_2	Circuit Fails	Circuit Continues Proper Operation
R_3	Circuit Fails	Circuit Continues Proper Operation
R_4	Circuit Fails	Circuit Fails
R_5	Circuit Fails	Circuit Fails
R_6	Circuit Fails	Circuit Continues Proper Operation
R_7	Circuit Continues Proper Operation	Circuit Fails
R_8	Circuit Fails	Circuit Continues Proper Operation
R_9	Circuit Fails	Circuit Continues Proper Operation
C_1	Circuit Continues Proper Operation	Circuit Fails
C_2	Circuit Continues Proper Operation	Circuit Continues Proper Operation
C_3	Circuit Continues Proper Operation	Circuit Continues Proper Operation
Z_1	Circuit Fails	Circuit Fails
Z_2	Circuit Fails	Circuit Fails
BJT “a”	Circuit Fails	Circuit operates properly in short circuited B-E failure, fails in short circuited B-C and E-C failures
BJT “b”	Circuit Fails	Circuit Fails
MOSFET “A”	Circuit Continues Proper Operation	Circuit Fails
MOSFET “B”	Circuit Fails	Circuit Fails

From this table, it can be concluded that the most critical circuit elements are MOSFET’s, BJT’s and the zener diodes, since almost all the failures of these elements cause catastrophic error. Among the capacitors, C_1 is the most critical circuit elements since the short circuit failure of this capacitor fails the circuit operation, whereas in the short and open circuit failures of C_2 and C_3, circuit continues its proper operation.

Open circuit failures of the resistors, except than R_7 fails the circuit operation which is the expected result since the continuity of the circuit is violated. However, the circuit also fails in the short circuit failures of R_4, R_5 and R_7. Therefore, it can be said that the most critical resistors are R_4 and R_5 since they cause circuit fail both in their open circuit and short circuit failure.

Before suggesting some precautions to minimize the possibility of catastrophic failures, it is important to mention the probability each component type will face open and short circuit failures. FMD-97 - *Failure Mode Distribution of Parts* [13] document of Reliability Information Analysis Center (RIAC) is a good reference for determining the failure modes and their effects and probabilities for each component type. According to this document, distribution of the open circuit and short circuit failures among all failure types for the components found in FPDC are given in Table 5.16. Note that the failures other than short and open circuit failures are not shown in this table.

Table 5.16. Failure Distributions According to FMD-97

Component Type	**Open Circuit Failure Distribution (%)**	**Short Circuit Failure Distribution (%)**
Resistor (Metal Film)	38	5
Capacitor (Metallized Paper Plastic)	27	63
Zener Diode (Voltage Regulator)	41	18
BJT	28	40
MOSFET	16	28

The information supplied in Table 5.16 gives an idea about the considerable component failures. For instance, the short circuit failures of R_4, R_5 and R_7 cause the circuit operation fail, however the short circuit failure probability among all types of failures for the resistors is very low. Therefore, it is not wise to connect resistors in series with R_4, R_5 and R_7 to eliminate their short circuit failures, since

open circuit failure is more probable for the resistors and this action doubles the risk of open circuit failure.

Table 5.16 suggests that the majority of the capacitor failures arise from the short circuit failure. In FPDC, only the short circuit failure of C_1 has catastrophic effect on the circuit operation. However, there is no available simple method to eliminate the short circuit failure of C_1.

In the zener diodes case, open circuit failure probability is reasonably high, so it is worth to take some preventive actions to eliminate the effects of zener diode open circuit failures. Most basic action against the open circuit failure of the zener diode is to connect an identical zener diode in parallel. Thus, the relevant parts of FPDC will be as shown in Figure 5.1 and Figure 5.2.

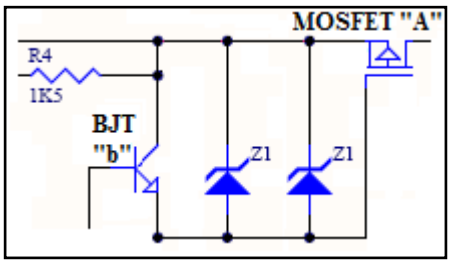

Figure 5.1. Preventive Action for Open Circuit Failure of Z_1

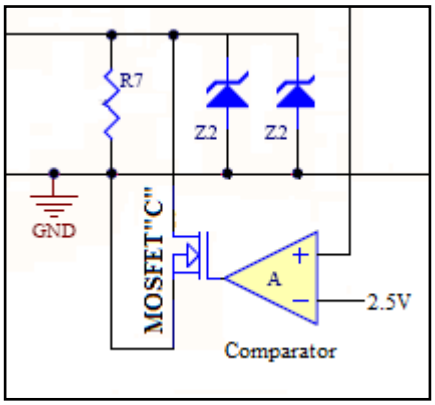

Figure 5.2. Preventive Action for Open Circuit Failure of Z_2

Connecting two zener diodes in parallel ensures the open circuit failure of either one does not affect the circuit operation. However, this action does not provide any protection for the short circuit failures of the zener diodes, besides short circuit failure of either zener diode fails the circuit operation. Therefore, this configuration

doubles the risk of circuit failure arising from short circuit failure of zener diodes. From this reason, it is wise to calculate the combined failure probability and compare it with the original case with one zener diode.

The failure probability arising from the open circuit and short circuit failure mechanisms for the original configuration is $P_{failure} = P_{short} + P_{open}$ and can be calculated as:

$$P_{original} = 0.18 + 0.41 = 0.59$$

Failure probability calculation for the configuration with two parallel zener diodes can be followed as:

$$P_{revised} = (P_{short-1} + P_{short-2} - P_{short-1} \times P_{short-2}) + P_{open-1} \times P_{open-2} \quad (5.1)$$

$$P_{revised} = (0.18 + 0.18 - 0.18^2) + 0.41^2 = 0.4957$$

Thus, it can easily be seen that $P_{revised} \leq P_{original}$, which implies that the failure probability of the revised configuration, which consists of two parallel connected zener diodes, is lower than the original configuration. Hence, it can be said that connecting two zener diodes in parallel reduces the risk of failures originating from zener diodes.

Simple modifications to eliminate BJT and MOSFET failures are not possible since these elements are operated like switches and the circuit operation depends on the position of these switches.

CHAPTER 6

CONCLUSION

Circuit reliability analysis is a critical application that is performed frequently especially in analog circuit design phase. This analysis becomes more of an issue in the circuits which have critical tasks. In this thesis, the reliability analysis of the Fuel Pump Driver Circuit (FPDC) is examined. This circuit is responsible from supplying the power that the fuel pump requires in order to pump the required amount of fuel to the turbojet engine. FPDC has a very critical mission in such a way that if this circuit fails, the turbojet engine rotation will slow down and the air vehicle will face the risk of falling. Therefore, it is desirable to confirm that the circuit operates properly in the worst case conditions, or even at the failure of some components in the circuit.

The primary tools for circuit reliability can be counted as reliability allocation and prediction, worst case circuit tolerance analysis, failure modes and effects analysis and fault-tree analysis. The applicable reliability analyses for FPDC are the worst case circuit tolerance analysis and the failure modes and effects analysis. During the reliability analysis of FPDC, these two analyses are performed to observe the effects and conditions are checked if the circuit operates correctly.

Firstly, the worst case circuit tolerance analysis of FPDC has been performed. This analysis investigates the effects of the tolerant resistances, different temperature and input voltage values on the circuit operation.

In the worst case analysis of FPDC, the effort is to find the input voltage, temperature and resistance values that constitute the worst case condition for the defined objective function. Once the optimum value for the objective function is reached, we check if it remains in the feasible interval. This analysis is repeated for eight objectives, each of which sets a check condition for the operating region of a transistor. These analyses are run utilizing two software programs: MATLAB and ModeFRONTIER. Parameter values are generated in ModeFRONTIER and these values are sent to MATLAB to solve the equations defined in it.

The worst case circuit analysis results show that FPDC operates with no problem in the whole band of resistance tolerances, temperature and input voltage interval. Therefore, we can conclude that FPDC withstands all variations in the circuit. Optimum objective values are drawn in power output band and the most critical power requirement condition has been determined to be 50 W, which is the lower bound for the power output. Similarly, the most critical temperature seems to be -30 °C since it is the binding constraint for four of the objectives.

After completing the worst case analysis, the failure modes and effects analysis is performed. This analysis is fulfilled by examining the short circuit and open circuit failures of all the components used in the circuit. However, computational analysis is performed only for the failures, whose effect is not obvious and cannot be observed by inspection. The computational analyses are also performed in MATLAB and ModeFRONTIER programs. The components whose failure cause catastrophic circuit failure have been determined according to the FMEA results. The failure distributions of each component type per FMD-97 document have been introduced and some preventive actions are suggested to minimize the number of catastrophic failures taking into consideration the failure distributions.

In real world applications, Monte Carlo analysis is used frequently to perform circuit worst case analysis and failure modes and effects analysis. Besides, basic circuit simulation tools (more generally SPICE tools) depend on Monte Carlo analysis while carrying out worst case circuit tolerance analysis. Nevertheless, Monte Carlo analysis is a probabilistic method and does not guarantee to reach the

worst case conditions. In this study, by moving the circuit analysis to a deterministic model and presenting an alternative method for circuit reliability analysis, the real worst case conditions have been reached. Therefore, it can be said that it is ensured that FPDC operates properly in the desired region in any condition with certainty depending on the results obtained with this method.

An initial effort has been made to reflect the equations that govern the circuit operation; this is the most time consuming part of this study. However, once the circuit equalities are introduced to MATLAB and ModeFRONTIER, this method provides great flexibility and enables the user to reach the worst case results in a meaningful time.

Furthermore, transistors are also included in the tolerance analysis in this study. As far as we know, no other study considered the operating regions of the transistors in the reliability analysis applications. In this thesis, the reliability analysis is performed on the basis of the operating regions of the transistors. The impression about the correct operation of the circuit is obtained from the operating regions of the transistors.

The method used in this study can be applied to other circuits, which do not include complex components like integrated circuits and operate in the steady state conditions. In the case of larger electronic circuits, this method can be applied with no problem by decomposing the circuit into smaller fragments so that the solution times do not increase seriously and complete reliability analysis of the circuit can be performed by composing the results obtained from each fragment.

To apply the method presented in this study, the steady state conditions are necessary, since timing is not considered in the calculations and it is assumed that no transitions occur in the circuit. However, the circuits which are used for switching application usually have two states: ON and OFF condition. In FPDC case, there are two states, as well. The investigated state in this study is the default ON state, which includes the normal operating conditions. Unless the input voltage V_{IN} exceeds 280 V, this state is preserved and the steady state conditions are reached if V_{IN} does not vary in time. In this thesis, the analyses are performed

assuming that V_{IN} does not vary in time and remains below 280 V. The OFF state, which includes the operation where V_{IN} is larger than 280 V, is aimed to be analyzed as well. But because of the lack of steady state conditions in that state, the analyses with the methods used in ON state got difficult to use and the analyses for the OFF state is excluded from the content of this study. However as a future study, it may be aimed to analyze OFF state of FPDC presenting new methods and complete reliability analysis of this circuit.

REFERENCES

[1] Dreyer, A., Interval *Analysis of Linear Analog Circuits*, 12th GAMM - IMACS International Symposium on Scientific Computing, Computer Arithmetic and Validated Numerics (2006), 14-22.

[2] Femia, N. and Spagnuolo, G., *True Worst-Case Circuit Tolerance Analysis Using Genetic Algorithms and Affine Arithmetic*, IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 47-9 (2000), 1285-1296.

[3] Gummel, H.K. and Poon, H.C., *An Integral Charge Control Model of Bipolar Transistors*, Bell Systems Technical Journal, 49 (1970), 827-852.

[4] Kolev, L., *Worst-Case Tolerance Analysis of Linear DC and AC Electric Circuits*, IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 49-12 (2002), 1693-1701.

[5] Liu, F. and Ozev, S., *Statistical Test Development for Analog Circuits Under High Process Variations*, IEEE Transactions On Computer-Aided Design of Integrated Circuits and Systems, 26-8 (2007), 1465-1477.

[6] Nelder, J.A. and Mead, R.A., *Simplex for Function Minimization*, The Computer Journal, 7 (1965), 308–313.

[7] Spence, R. and Soin R., *Tolerance Design of Electronic Circuits*, Addison-Wesley (1988),

[8] Tian, M.W. and Shi, R.C.-J., *Worst Case Tolerance Analysis of Linear Analog Circuits Using Sensitivity Bands*, IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 47-8 (2000), 1138-1145.

[9] Tian, M.W., Ling, X.-T. and Liu, R.-W., *Novel Methods for Circuit Worst-Case Tolerance Analysis*, IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 43-4 (1996), 272-278.

[10] Wang, P. and Yang, S., *A New Diagnosis Approach for Handling Tolerance in Analog and Mixed-Signal Circuits by Using Fuzzy Math*, IEEE Transactions on Circuits and Systems – I, 52-10 (2005), 2118-2127.

[11] White, R. V., *An Introduction to Six Sigma With a Design Example*, IEEE Applied Power Electronics Conference and Exposition, (1992), 28-35.

[12] White, R. V., *Component Tolerance And Circuit Performance: A Case Study*, IEEE Applied Power Electronics Conference and Exposition, (1993), 922-927.

[13] *Reliability Prediction of Electronic Equipment*, MIL-HDBK-217F, U.S. Department of Defense (1991).

[14] *Electronic Reliability Design Handbook*, MIL-HDBK-338B, U.S. Department of Defense (1998).

[15] *Failure Mode/Mechanism Distributions*, FMD-97, Reliability Information Analysis Center (RIAC), Rome (NY, USA) (1998), sample version available online at http://src.alionscience.com/pdf/RAC-1ST/FMD97_1ST.pdf (last accessed 23rd January 2011).

[16] Worst Case Circuit Analysis Application Guidelines, Reliability Information Analysis Center (RIAC), Rome (NY, USA) (1993)

[17] *ZXTC2063E6, Complementary Medium Power Transistors Datasheet* (2007), available at http://www.diodes.com/datasheets/ZXTC2063E6.pdf (last accessed 25th January 2011).

APPENDIX A

CODE DESCRIPTIONS

Two .m files are created in MATLAB for the optimization: fmin.m and NLEqn.m. fmin.m includes some of the constant values, linear equations, boundaries for the variables (each of which is unbounded in both sides) and the initial values for each variable. In this file, $R_1 \ldots R_9$ and T are defined as constants. Moreover, fmin.m includes "fmincon" function which runs an optimization routine for the defined objective. However, fmincon function is not used for its optimization property; instead ModeFRONTIER is used for that purpose. "fmincon" still exist in fmin.m, but since the problem has unique solution for the constant "T" and "R" values, optimization property of fmincon function remains redundant and this function is used only for solving the equations and assign values to the variables. NLEqn.m file contains the non-linear constraints and the constants included in the non-linear equations. This file is called by fmin.m and makes contribution to the optimization.

Two ModeFRONTIER files are used to perform the optimization jobs: "fmin.prj" and "fminsolver.prj". While fmin.prj calls MATLAB in batch mode and runs fmin.m file generating $R_1 \ldots R_9$ and T values for the specific V_{IN} value, fminsolver.prj generates V_{IN} values starting from 200 to 280 with 4 volts step and runs fmin.prj for each V_{IN} value such that the optimum values of the variables can be observed in 200-280 Volts band of V_{IN}.

While performing FMEA, minor changes in MATLAB and MF files are necessary. Modifications in MF files are fairly more applicable rather than MATLAB files.

This is because MF has good interface and the modifications can be done easily and quickly. Not modifying the MATLAB codes is highly desirable; however it is not possible for the open circuit failures of the zener diodes, Z_1 and Z_2. Fortunately, failures of the resistors can be simulated only by modifying the MF file, fmin.prj. It is simply applied by changing the resistance value of short circuited resistor to zero and open circuited resistor to infinity instead of defining it in an interval, like what is done in tolerance analysis case.

Also in FMEA, V_{IN} is let as a variable to be determined by the model. This modification is also introduced in fmin.prj defining V_{IN} as a variable, varying in 200-280V interval.

The content of fmin.m and NLEqn.m is provided in the following pages. Note that the scripts after "%" sign stand for the comments

```
%The following scripts are from fmin.m
ISb=5.1E-13; ISCb=1.1E-13; ISEb=1.2E-13; BRb=65; BFb=480; %constants used in current calculation of BJT "b"


%Vt and Pout equations are linear equations that can be calculated once in every run
Vt=(8.6171E-5*(T+273)); %eq.32
Pout=(14/3)*(Vin-200+150/14); %eq.33
%Aeq is the matrix form of the coefficients in the linear equations
Aeq=[1  1  0  1  0 -1  0  0  1  0  0  0  0  0  0  0  0  0  0  0  0 -1  0  1  0  0  0  0  0  0  0  0; %eq.1
      0 -1  0  0  0  0 -1  0  0  1  0  0  0  0  0  0  0  0  0  0  0  0  0  0  1  0  0  0  0  0  0  0; %eq.2
      0  0  0  1  0  0  0 -1  0  0  0  0  0  0  0  0  0  0  0  0  0  0  1  0  0  0  0  0  0  0  0  0; %eq.3
     -1  0  1  0  1  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0; %eq.4
      0  0  0  0  0  1  1 -1  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0; %eq.5
      0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0 -1  1  1  0  0  0  0  0  0; %eq.6
      0  0  0  0  0  1  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0; %eq.7
      0 (R4+R5) 0 0  0  0  0  0  0 (R6+R8+R9) 1 0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0; %eq.8
      (R1+R2+R3) 0  R10 0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0; %eq.9
      0 (R4+R5) 0 0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0 -1  0  0  0  0  0  0  0  0  0  0  0  0; %eq.10
```

```
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0; %eq.11
0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0; %eq.12
0 0 R10 0 0 0 0 0 0 0 0 -1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0; %eq.13
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 -1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0; %eq.14
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 -1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0; %eq.15
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 -1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0; %eq.16
0 0 0 0 0 0 0 0 0 0 0 -1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0; %eq.17
0 0 0 0 0 0 0 0 0 0 0 0 1 -1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0; %eq.18
0 0 0 0 0 0 0 0 0 0 0 0 -1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0; %eq.19
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 -1 0 0 0 0 0 0 0; %eq.22
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 -1 0 0 0 0 0 0; %eq.23
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1]; %eq.34

beq=[0; 0; 0; 0; 0; 0; Vin; Vin; 0; 0; 0; 0; 0; 0; 0; 0; 0; 0; -(ISb/BRb + ISCb);
 (ISb*((BFb+BRb)/(BFb*BRb)) + (ISEb + ISCb)); Vin; (-0.002241*T + 0.4108)]; %RHS of the linear equations

lb=[-inf;  -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf;
 -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf; -inf]; %lower bounds for the variables
```

```
ub=[inf; inf; inf; inf; inf; inf; inf; inf; inf; inf; inf; inf; inf; inf; inf; inf; inf; inf; inf;
 inf; inf; inf; inf; inf; inf; inf; inf; inf; inf; inf; inf; inf];  %upper bounds for the variables

x0=[0.001; 0.005; 0.001; 0.001; 0.001; 0; 0.001; 0.001; 2; 0.005; 0.05; 15; -0.1; -15; 0.001; 0.6; -0.6; 15;
   -0.6; 15; 15; 2; 0; 0; 0; 250; 15; 15; 0.1; 0.1; 0.1; 0.3]; %initial values for the variables

options=optimset('MaxFunEvals',1500,'TolCon',1e-20,'TolFun',1e-20,'TolX',1e-20);
%optimization parameters for %fmincon function

[x]=fmincon(@(x)(x(6)),x0,[],[],Aeq,beq,lb,ub,@(x) NLeqn(x,Pout,Vt),options); %fmincon function solves the linear
%constraints defined in this .m file and the nonlinear constraints by calling %NLEqn.m file which contains all the %nonlinear
equations.

save('D:\GK-5\MFSolver10\MF.txt','x','-ASCII') %result of fmincon function (x vector) is written into a text file to
%form a suitable interface for ModeFRONTIER
%end of fmin.m
```

```
%The following scripts are from NLeqn.m
function [c, ceq] = NLeqn(x,Pout,Vt)
KB=0.00428; KC=0.955; VthB=4.5; VthC=-4.5; %MOSFET “A” and “B” parameters
ISa=4E-13; ISEa=0; ISCa=0; BFa=470; BRa=97; NFa=1; NRa=1, NEa=1.5; NCa=2; VARa=inf; VAFa=23; IKFa=3.5; IKRa=inf;
%BJT “a” parameters
ceq = [-x(9) + KC*(2*(x(14) - VthC)*x(13) - x(13)^2);%eq.20      /ceq contains the non-linear equalities
    -x(10) + KB*(2*(x(12) - VthB)*x(11) - x(11)^2);%eq.21
    -x(7) + (ISa/BFa)*(exp(x(16)/(NFa*Vt))-1) + ISEa*(exp(x(16)/(NEa*Vt))-1)
    + (ISa/BRa)*(exp(-x(17)/(NRa*Vt))-1) + ISCa*(exp(-x(17)/(NCa*Vt))-1);%eq.24
    -x(6) + (ISa/x(29))*(exp(x(16)/(NFa*Vt))-exp(-x(17)/(NRa*Vt)))
- ((x(29)*ISa)/BRa)*(exp(-x(17)/(NRa*Vt))-1) – ISCa*(exp(-x(17)/(NCa*Vt))-1);%eq.25
    -x(29) + (x(30)/2)*(1 + sqrt(1 + 4*x(31)));%eq.26
    -x(30) + 1/(1 - x(16)/VARa + x(17)/VAFa);%eq.27
    -x(31) + (ISa/IKFa)*(exp(x(16)/(NFa*Vt))-1) + (ISa/IKRa)*(exp(-x(17)/(NRa*Vt))-1);%eq.28
    -x(4) + (4.571E-38)*exp(5.294*x(27));%eq.29
    -x(5) + (4.571E-38)*exp(5.294*x(28));%eq.30
    -Pout + x(26)*x(9)];%eq.31
c=[]; %c is for non-linear inequalities which is empty since there is no in this problem %end of NLeqn
```