CAPACITIVE CMOS READOUTS FOR HIGH PERFORMANCE MEMS
ACCELEROMETERS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

FEBRUARY 2011

Approval of the thesis:

CAPACITIVE CMOS READOUTS FOR HIGH PERFORMANCE MEMS ACCELEROMETERS

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ABSTRACT

CAPACITIVE CMOS READOUTS FOR HIGH PERFORMANCE MEMS
ACCELEROMETERS

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February 2011, 140 pages

MEMS accelerometers are quickly approaching navigation grade performance and navigation market for MEMS accelerometer systems are expected to grow in the recent years. Compared to conventional accelerometers, these micromachined sensors are smaller and more durable but are generally worse in terms of noise and dynamic range performance. Since MEMS accelerometers are already dominant in the tactical and consumer electronics market, as they are in all modern smart phones today, there is significant demand for MEMS accelerometers that can reach navigation grade performance without significantly altering the developed process technologies.

This research aims to improve the performance of previously fabricated and well-known MEMS capacitive closed loop $\Sigma\Delta$ accelerometer systems to navigation grade performance levels. This goal will be achieved by reducing accelerometer noise level through significant changes in the system architecture and implementation of a new electronic interface readout ASIC. A flexible fourth order $\Sigma\Delta$ modulator was chosen as the implementation of the electro-mechanical closed loop system, and the burden of noise shaping in the modulator was shifted from the mechanical sensor to the programmable electronic readout. A novel opera-

tional transconductance amplifier (OTA) was also designed for circuit implementation of the electronic interface readout.

Design and fabrication of the readout was done in a standard 0.35 μm CMOS technology. With the newly designed and fabricated readout, single-axis accelerometers were implemented and tested for performance levels in $\pm$ 1g range.

The implemented system achieves 5.95 μg/$\sqrt{\text{Hz}}$, 6.4 μg bias drift, 131.7 dB dynamic range and up to $\pm$ 37.2 g full scale range with previously fabricated dissolved epitaxial wafer process (DEWP) accelerometers in METU MEMS facilities. Compared to a previous implementation with the same accelerometer element reporting 153 μg/$\sqrt{\text{Hz}}$, 50 μg bias drift, 106.8 dB dynamic range and $\pm$ 33.5 g full scale range; this research reports a 25 fold improvement in noise, 24 dB improvement in dynamic range and removal of the deadzone region.

Keywords: sigma delta modulation, MEMS accelerometer, sensor interface electronics, capacitive readout, low noise electronics

ÖZ

MEMS İVMEÖLÇERLER IÇIN YÜKSEK PERFORMANS KAPASITIF OKUMA
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Şubat 2011, 140 sayfa

MEMS ivmeölçer sistemleri, son yıllarda olan gelişimleri ile seyrüsefer uygulamaları için gerekli performans kriterlerine yaklaşmaktadır, ve de bu nedenle seyrüsefer sistemler piyasasının MEMS ivmeölçerlere olan ilgisinin gelecek yıllarda artması beklenmektedir. Klasik ivmeölçer sistemlerine kıyasla, MEMS ile mikroişlenmiş duyargalar çok daha küçük ve de dayanıklı ancak performans olarak daha kötü olmaktadırlar. Ancak MEMS ivmeölçerlerin taktik uygulamalarda ve de elektronik aletler piyasasında kullanımının yaygınlaşmasına bağlı olarak, MEMS ivmeölçerlerin üretim süreçlerinin ciddi şekilde değişmeden seyrüsefer uygulamalarında da kullanılabilmesine dair ciddi bir ilgi vardır.

Bu araştırmanın amacı, daha önceden üretilmiş kapasitif kapalı döngü MEMS ivmeölçerlerin performans seviyesine seyrüsefer uygulamalarına hazır hale getirmektir. Bu amaca ulaşmak için sistem seviyesindeki mimari değişiklikler ve de yeni bir elektronik devre tasarımı ile, ivmeölçer gürültüsünün düşürülmesi planlanmaktadır. Değişik ivmeölçerlere uygulanabilir bir dördüncü derece $\Sigma\Delta$ modülatör mimarisi seçilmiştir, ve de bu sayede gürültü şekillendirme fonksiyonu mekanik yapıdan programlanabilir elektronik devreye aktartılmıştır. Ayrıca, tasarlanan okuma devresinin performansını iyileştirmek amacıyla yeni bir operasyonel transkon-

düktans yükseltgeç (OTA) devre mimarisi geliştirilmiştir.

Elektronik devrenin tasarım ve de üretimi 0.35 μm CMOS teknolojisinde geliştirilmiştir. Yeni tasarlanan okuma devreleri ile birlikte üretilen MEMS ivmeölçer duyargaları birleştirilmiştir ve de ivmeölçerlerin ± 1g içerisinde performans seviyeleri ölçülmüştür.

Hibrit ivmeölçer sisteminin 5.95 μg/$\sqrt{\text{Hz}}$ gürültü, 6.4 μg ofset kararsızlığı, 131.7 dB dinamik aralık ve ± 37.2 g ölçülebilir ivme aralığı performans kriterlerine sahip olduğu test edilmiştir. ODTÜ'de aynı ivmeölçer ile daha önceden yapılan bir uygulamada elde edilen 152 μg/$\sqrt{\text{Hz}}$ gürültü, 50 μg ofset kararsızlığı, 106.8 dB dinamik aralık ve ± 33.5 g ölçülebilir ivme aralığı değerlerine kıyasla gürültüde 25 katlık ve de dinamik çalışma aralığında 24 dB'lik gelişme gösterilmiştir.

Anahtar Kelimeler: sigma delta modülasyonu, MEMS ivmeölçer, duyarga elektronik devresi, kapasitif okuma devresi, düşük gürültü elektronik

To the memory of my grandfather Hüseyin Sönmez, and all who have made sacrifices in the pursuit of education and knowledge

ACKNOWLEDGMENTS

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CHAPTER 1

INTRODUCTION

The great physicist Albert Einstein is once quoted to say "Any fool can make things bigger, more complex, and more violent. It takes a touch of genius, and a lot of courage, to move in the opposite direction". Ironically, the great evolution of the electronics and micro-mechanical systems industry in the last quarter of twentieth century would follow the direction of making things, smaller, simpler and cheaper. Einstein would not live on to see this day, but the widespread application of miniature MEMS (Micro Electro Mechanical Systems) sensors today is a testimony to this direction.

Micromechanical sensors, working by the simple principle of inertial movement, are present in our daily lives, and in fact in our pockets. Modern cellular phones all have MEMS accelerometers built inside them, a recent practice spurned by the rapidly falling prices of such devies combined with steady improvements of performance. Indeed, according to a professional report [1] whose result can be seen figure 1.1, the MEMS accelerometer market worlwide will reach 1.5 billion $ volume in 2012. At the current trend of economic implementation and performance improvements, in a couple of years it might even be possible to see integrated MEMS-based navigation applications in our mobile devices.

While the MEMS market is growing, it also drives the semiconductor industry alongside since nearly all the MEMS sensors implemented up to this date require an electronic interface circuitry in order to traslate the motion of the MEMS sensor into electronic domain. In the modern analog/mixed-signal semiconductor market, the MEMS sensor is usually integrated with interface electronics and fabricated in single or two fabrication batches. This approach saves on die area, fabrication cost and time, and makes the final product cheaper and flexible. After all, the MEMS sensor elements implemented in modern mobile consumer devices are

expected to be very small.
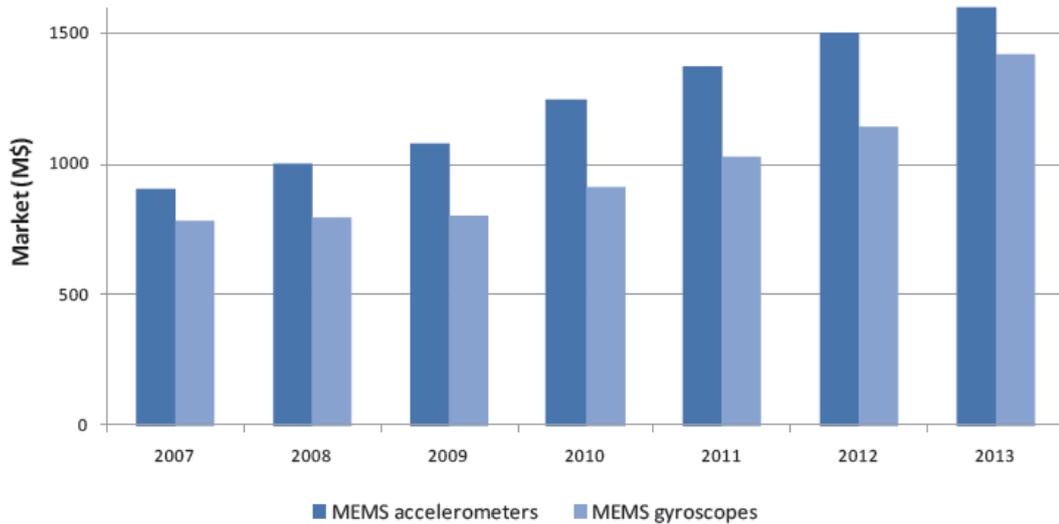
Figure 1.1: MEMS accelerometer and gyroscope worldwide market trends and prediciations from 2008 to 2013.

Despite the advantages of this integrated fabrication approach however, integrated micro accelerometers could not penetrate the more demanding, but stable applications such as tactical military or navigation. Especially for navigation applications, expectations required from MEMS sensors are quite high and even modern MEMS fabrication techniques are insufficient to produce the required sensors on the same die with CMOS electronics. Therefore, in the field of military and navigation applications, hybrid MEMS accelerometer systems combined from individual sensor and electronic circuits are very common.

The necessity for high performance navigation grade MEMS accelerometers are even more evident from reports that the mobile navigation market is expected to grow in 2011 and beyond [2]. Currently, the mobile navigation market is saturated with GPS devices, however military applications are already integrating MEMS accelerometers for navigation purposes along with GPS devices in order to improve accessibility, reliability and performance. Therefore, it can be expected that when MEMS accelerometers reach the level of maturity expected from small, reliable and high performance navigation sensors; there will be further usage of MEMS accelerometers in the mobile consumer market.

At the current technology level, high performance MEMS accelerometers require specialized ultra low noise interface circuits, or readouts, in order to reach navigation grade. In the

literature, design of a readout is usually tailored specifically for an accelerometer design; and a customizable readouts that can perform very well with several different accelerometers are hard to find. This is more true for closed loop sensors, which are generally preferred for improved linearity and tolerance to process variations. Therefore, design of universal high performance readouts are critical for demanding applications of MEMS accelerometers. If readout design and implementation stage is not done in detail, final performance of the MEMS element will suffer significantly.

1.1 Classification of Microaccelerometers and Interface Circuits

While MEMS accelerometers have become very popular over decades, they have also become very diverse. Many different microaccelerometer types exist in the literature and commercial market, some of them even specialized for special applications such as space navigation [3].

In fact, since the applications for and types of MEMS accelerometers have grown so much over the years, it is no longer possible or sensible to classify MEMS accelerometers by one subject alone. In this thesis, classification of MEMS accelerometers will be done over three topics: applications or specifications, micro sensor type and interface circuit. The last classification is especially important in order to consider various type of interface circuits used with different accelerometers.

1.1.1 Classification by Application

Microaccelerometers have a wide range of application areas ranging from navigation and seismic applications to tilt detection. Some of the application areas of microaccelerometers are:

- Navigation and inertial navigation systems

- Tilt sensing

- Orientation sensing

- Crash detection

- Free fall detection&protection

- Vibrating monitoring

- Structural monitoring

- Animal tracking

- Medical applications

- Inertial guidance and smart munitions

- Motion input detector

- Image stabilization

- Seismic detection

Most application areas have quite specific performance requirements from microaccelerometers. For example, navigation and seismic detection applications require the best resolution; while vibration monitoring and image stabilization applications require a large bandwidth and flat frequency response. Crash detection and inertial guidance applications require a large full scale range up to ± 100g's in order to work with practical situations [6].

Inertial navigation is a newly emerging, but potentially very beneficial application area for MEMS accelerometers. Navigation grade accelerometers are required to have a very good resolution and are expected to be very predictable with very low drift and offset values. This is absolutely necessary since position updates are done by "dead reckoning", which is very vulnerable to static errors in determination of position from previously experienced acceleration values. Figure 1.2 shows an example dead reckoning plot taken from a marine navigation guide.

Other common application areas of microaccelerometers are tilt and orientation sensing, used mainly in mobile devices to discern the orientation of the device with respect to earth's surface. These applications can work with low bandwidth, low resolution accelerometers and hence the primary concern in these applications are device size and cost.

Vibration, structural monitoring and animal tracking applications require the ability to detect fast motion and vibrations of the bodies they are attached to. Hence, a large and flat bandwidth
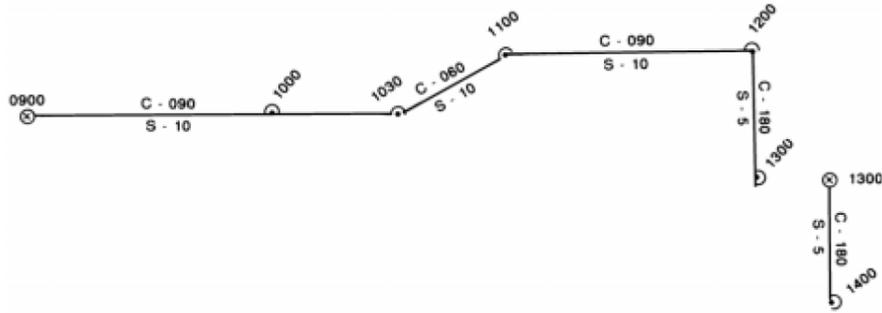
Figure 1.2: An example dead reckoning plot [7].

is absolutely necessary for these applications. However, resolution and range requirements are more relaxed since the bodies under surveillance are not likely to experience long periods of significant acceleration and the results are intended to be collected when the body is relatively stationary and external acceleration levels are low.

Crash detection is a unique, but very popular application for microaccelerometers. Usually implemented by automotive industry in order to detect potential vehicle crashes, so that airbags can be deployed safely, this application requires accelerometers that can withstand and detect large amounts of acceleration. However, resolution can be very low since the threshold for crash detection is generally much higher than any acceleration that be experienced in normal time.

Finally, tactical grade military applications are another unique application area. Tactical grade accelerometers are used in various systems in military equipment, from turret stabilization to guidance systems. Tactical grade accelerometers are required to be a mix of high resolution and high full scale range accelerometers, and hence dynamic range is a critical performance parameters for these sensors [19]. The resolution requirement however, is more relaxed compared to navigation grade accelerometers.

High resolution navigation and seismic are possibly the most challenging applications for the implementation of a MEMS accelerometer readout circuitry. Due to the high resolution requirements, electronic noise sources are of primary concern and performance limitations by the electronic readout circuitry is very common in the literature. Therefore, in order to classify the electronic readout circuitry for specific applications, we have to define suitable

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performance requirements expected from the MEMS accelerometer.

Navigation grade microaccelerometers are generally defined to have to have the following specifications: [4] [17][19].

- Full Scale Range > 2 g

- Bias Drift < 10 µg

- White Noise < 5 µg/ $\sqrt{Hz}$

- Non-Linearity < 0.1 %

- Bandwidth > 10 Hz

The choice and implementation of readout circuitry is especially critical in opitimization of white noise, bias drift, non-linearity and bandwidth specifications. In order to meet these non-linearity and bias drift specifications, a closed loop structure is absolutely necessary.

1.1.2 Classification by Microaccelerometer Type

Microaccelerometers can also be classified by their mechanical sense mechanisms: [19]

- Capacitive / Electrostatic

- Piezoelectric

- Piezoresistive

- Thermal

- Resonant

- Magnetic

- Optical

- Tunneling Current

Capacitive, thermal, resonant, magnetic, optical and tunneling accelerometers rely on the inertial movement of a solid/fluid mass under external acceleration. What differs in each sensor type is the transduction technique used to detect this movement.

Piezoelectric and piezoresistive accelerometers detect the stress imposed on them by an external acceleration. Piezoelectric accelerometers are much more sensitive to high frequency vibrations compared to DC stress levels and hence are not suitable for high performance accelerometer applications such as inertial navigation, which require excellent performance for low frequency excitations. However, due to their simplicity piezoelectric accelerometers are still used very frequency in vibration sensing applications where their high bandwidth, simple electronics and good resolution are advantegous.

Piezoresistive sensors, while having very simple readout schemes are susceptible to temperature variations in the environment. Moreover, piezoresistive sensors suffer from low sensitivity in typical applications, limiting their usefulness to low resolution industrial applications [19].

Capacitive accelerometers are very popular in a wide variety of applications. They are relatively small, temperature independent, consume very little power, have moderate sensitivity and are easy to implement with microfabrication techniques. Due to these advantages, capacitive sensors are the default choice when a designer want to design an accelerometers. As another advantage, capacitive accelerometers can also be designed as actuators; so the electronic readout circuitry can easily multiplex between position sensing and feedback actuation stages with a simple mechanical structure. For this reason, capacitive accelerometers can be easily integrated with closed loop architectures and closed loop electronic readouts.

However, other accelerometer types also find usage in specific applications. For example resonant accelerometers are more advantageous in space navigation applications since they are much more resistant to space radition levels [3]. Tunneling current accelerometers are able to reach very low noise levels, but are more expensive and susceptible to temperature and bias variations [5].

Since the capacitive accelerometer is a good trade-off between price and compatibility vs. performance, we will consider the simple sense/actuator multiplexable electrostatic capacitive MEMS sensor element in this thesis.

1.1.3 Classification by Interface Circuit

The last classification we will consider is on accelerometer interface electronics. Electronic interface circuits for microaccelerometers can be broadly put into two categories:

- Open Loop Electronics: Open loop readout circuits aim to convert the proof mass data, or the amount of deflection into a voltage or current. Deflection of the proof mass under acceleration is necessary and is designed to be large in order to improve sensitivity. These electronic circuits are usually simple and easy to design and have a single analog output. Due to their simplicity, they usually have minimal noise at their outputs; however nonlinearity, bias drift, bandwidth and temperature sensitivity specs suffer. Some of these designs utilize electronic feedback techniques to improve these specs inside the ASIC [8], however any interface circuit that is not applying direct feedback to the sensor in order to keep the proof mass constant is actually working in open loop.

- Closed Loop Electronics: Closed loop readout circuits apply electromechanical feedback to the sensor in order to keep the proof mass stationary. This way, nonlinearities due to the motion of proof mass and/or springs are prevented. Since position of the proof mass is kept constant, bias drift and temperature sensitivity is decreased. The main disadvantage is the increased circuit complexity, power consumption and sometimes white noise. In order to prevent the feedback from increasing white noise floor, closed loop accelerometers sometimes use "noise shaping" techniques in order to shape unwanted electronic noise sources around the band of interest.

Due to bias drift and temperature immunity requirements, closed loop interface electronics are preferred over their open loop counterparts, especially in navigation grade applications. It should also be noted that closed loop electronics require some sort of electromechanical actuation mechanism in order to keep the proof mass stationary.

Another criteria for classification of interface electronics is the type of data output. In general, analog output accelerometers are easier to design and implement, but they may require a high resolution analog/digital converter (A/DC) at their outputs in order to convert the acceleration information into digital domain. Digital output accelerometers are easier to implement, since they do not require an external A/DC. Digital output accelerometers are also more advantageous in area constrained applications, since the addition of an external high resolution

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A/DC will consume a lot of area on a PCB implementation. For this reason, the A/DC may sometimes be moved inside an analog accelerometer readout ASIC in order to save space.

In addition to analog feedback accelerometers, there are also pulse density modulated (PDM) digital output accelerometers. Such an electronic circuit when combined with a capacitive accelerometer, forms an electromechanical (EM) $\Sigma\Delta$ modulator [14]. $\Sigma\Delta$ modulation is used mainly in data converter applications, and can be configured to be A/DC or D/AC data converters. EM$\Sigma\Delta$ modulators directly convert input acceleration (or rotation in the case of gyroscopes) into a digital output and give the output directly. This digital output is also given as feedback to the sensor, and this feedback actuation keeps the proof mass stationary even under acceleration. For this reason, EM$\Sigma\Delta$ modulated accelerometers are also called as "force balanced" systems[14].

Obviously, such modulators need mixed-signal readout circuits in order to convert the analog position information into a voltage, convert this voltage into digital domain and then give a force feedback to the system depending on the value of the digital output. Therefore, design of the electronic interface circuitry is critical.

An example of an EM $\Sigma\Delta$ accelerometer with a simulation demonstration can be seen in Mirabilis design's website [15], with the example covering one of the first designed EM $\Sigma\Delta$ modulators by Mark A. Lemkin in University of California, Berkeley.

In the last years, EM $\Sigma\Delta$ modulated microaccelerometers are increasing in popularity and availability due to several advantages:

1. Force balancing action keeps the accelerometer proof mass stationary and eliminates bias drift due to displacement of proof mass and springs.

2. Since the proof mass is kept stationary, sensitivity is also kept constant and linearity is improved.

3. Full scale range of the device depends on the feedback strength of the loop, which can be increased more easily than mechanically-constrained open loop designs

4. PDM digital output requires only simple digital filters, which can be applied by any microprocessor system

5. For high order modulators, loop control can be easily modified by altering the chracter-istics of the electronic readout circuitry

6. No external circuitry is necessary and the total electronic readout chip area is compara-ble to simple open loop designs.

In this thesis, we will consider the EM $\Sigma\Delta$ modulator for MEMS capacitive accelerometers in Chapters 2 and 3.

1.2 History of $\Sigma\Delta$ MEMS Accelerometer Interface Circuits

Previous works on $\Sigma\Delta$ MEMS accelerometers in the literature started in a paper published in 1990 by W. Henrion et. al., which was the first reported accelerometer system having a digital EM feedback with a direct digital output [9]. The first EM $\Sigma\Delta$ modulation analysis in the literature is done in this paper, and it is proven that the MEMS accelerometer can act as a mechanical filter to EM $\Sigma\Delta$ modulation. The accelerometers used in this work had very large proof masses, hence their full scale range was $\pm$ 0.1 g and resonance frequency was 266 Hz. Reported resolution was 10 μg/ $\sqrt{Hz}$, with a dynamic range of 80 dB. A newer design that is expected to achieve 100 dB dynamic range is also mentioned, but no test results are given.

The second breakthrough in the literature was achieved by C. Lu, M. Lemkin and B. E. Boser by their implementation of MEMS sensor and readout circuitry in a monolithic die [10]. Nov-elties in this work include stability analyses, the addition of lead compensators in feedforward path (see Section 2.3.3), and first theoretical emergence of deadzone phenomena. Minimum resolution of the accelerometer is 1.6 mg/ $\sqrt{Hz}$ at a full scale range of 69 dB. As explained in the paper, this low performance level is due to a high resonance frequency at 4.7 kHz.

At this point in the literature, it was realized that the performance specifications of MEMS accelerometers relied too heavily on sensor parameters. This reliance made it especially dif-ficult to implement low noise, small and monolithic accelerometers. Therefore, research was focused on methods to improve sensor dynamic range and noise floor by advancements in the electronic interface circuitry.

Petkov et. al. reported such an advancement by their fourth order $\Sigma\Delta$ modulated interface circuitry, designed for both MEMS accelerometer and gyroscopes [11]. This work establishes

the framework for modern higher order ΣΔ modulator, and discusses why increasing the mod-ulator order is necessary. In addition, electronic implementation of higher order modulation is also discussed. Figure 1.3 shows the electronic noise shaping filter designed by Petkov et. al. in order to improve quantization noise. Resolution of the accelerometer in this work is 150 μg/$\sqrt{\text{Hz}}$; however it is also reported that 120 dB dynamic range was achieved for gyroscope implementation.

C_A	100fF	C_{B2}	400fF
C_B	300fF	C_b	1pF
C_{A1}	50fF	C_c	200fF
C_{B1}	250fF	C_{f_A}	100fF
C_{A2}	200fF	C_{f_B}	3.1pF
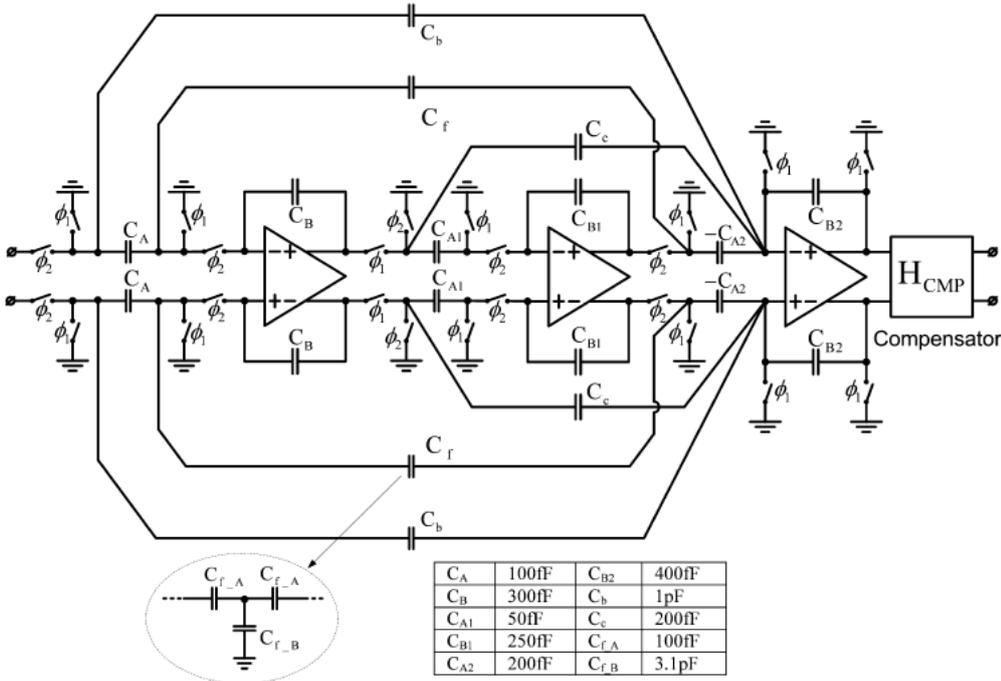
Figure 1.3: Electronic noise shaping filter implemented by Petkov et. al. [11].

In 2006, H. Kulah et. al. published their work on noise analysis of second order ΣΔ modulated accelerometers [12]. This is another critical paper on accelerometer interface circuit design, since the paper discusses every possible noise source present in a ΣΔ modulator. Closed loop accelerometer resolution is 10 μg/$\sqrt{\text{Hz}}$ for a full scale range of ± 10 g. Dynamic range for 1 Hz is therefore 100 dB. Figure 1.4 shows the hybrid implementation done in this work, with the MEMS accelerometers implemented with electronic readouts on a hybrid package.

In 2007, Abdolvand et. al. reported the first sub-μg accelerometer in the literature with a resolution of 231 ng/$\sqrt{\text{Hz}}$ [13]. While this work uses advanced fabrication techniques to utilize a very thick proof mass, high order ΣΔ modulation is also used to improve dynamic
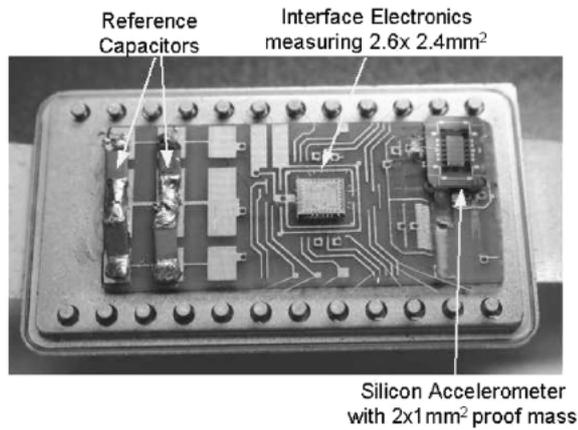
Figure 1.4: Hybrid accelerometer package by Kulah et. al. [12].

range and resolution.

In the last three years, there have been several new enhancements in high order EM $\Sigma\Delta$ modulators and significant performance improvements can be observed. Raman et. al. investigated a systematic approach for designing EM $\Sigma\Delta$ modulators, with a focus on exact pole/zero placement in such modulators [21]. Previously, high order modulator interface electronics were designed for specific sensors; since it was derived that stability of such systems would only be conditional. A new architecture was proposed in this paper, and a rigorous analysis shows that with this new architecture, system pole/zeros can be placed as desired. This makes the EM modulator design procedure to be similar to standard electronic $\Sigma\Delta$ modulators and gives great flexibility to the designer.

Recently, Colibrys announced a new $\Sigma\Delta$ modulated MEMS accelerometer that can achieve 136 dB dynamic range, 1.7 μg/$\sqrt{\text{Hz}}$ resolution and $\pm$ 11 g [17]. High voltage switch feedback technique was first introduced in this paper, with the ASIC implemented in a high-voltage option fabrication process.

Further detailed information on history of MEMS accelerometers can be obtained from Ilker E. Ocak's PhD thesis [19].

1.3 Previous Work on MEMS Accelerometer Interface Circuits in METU

MEMS accelerometers and MEMS accelerometer readout circuits are not new topics in METU. Previously, Ilker E. Ocak and Reha Kepenek from METU Electrical and Electronics Engineering and METU-MEMS Center worked on MEMS accelerometers and readout circuis respectively [19][20].

Works on MEMS accelerometers started in 2003 in METU with silicon-on-insulator designs, and fabrication done by MemsCap company. Later on, fabrication of MEMS accelerometers started to be done in METU-MEMS facilities [19]. With fabrication, demand for a high performance custom readout ASIC also increased and such an ASIC was designed by Reha Kepenek as part of his M.Sc. thesis [20].

Previous works on accelerometers in METU focus on the basic second order $\Sigma\Delta$ modulator with relatively small amount of circuit components. However while simple, second order $\Sigma\Delta$ modulated accelerometers have significant problems with noise and deadzone; and hence it was realized that more efficient electronic interface circuits are necessary.

As a comparison, the performance of the accelerometer presented in [19] with a second order readout is 153 $\mu g/\sqrt{Hz}$ and 96 dB at 1 Hz, while the objective of this thesis is <10 $\mu g/\sqrt{Hz}$ and >120 dB with the same accelerometer.

1.4 Objectives of This Thesis

Building upon the previous works on METU-MEMS Center, this thesis aims to improve the performance of $\Sigma\Delta$ accelerometers by making core architectural and circuit level changes to the accelerometer electronic interface circuitry. A comprehensive list of the objective of this thesis are given below:

1. Accelerometer white noise level is aimed to be <10 $\mu g/\sqrt{Hz}$. This will be done by properly modelling EM $\Sigma\Delta$ quantization noise and minimization of electronic noise sources.

2. Similarly, accelerometer bias drift is aimed to be <10 μg.

3. Dynamic range of the accelerometer is expected to be >120 dB for 1 Hz band.

4. The designed readout circuitry should be able to drive the accelerometers designed in METU-MEMS facilities to a full scale range of at least ± 10 g.

5. Complete system bandwidth must be at least 200 Hz.

6. In order to improve performance, a higher order EM $\Sigma\Delta$ modulator will be designed. Stability of the modulator should be guaranteed for a large range of operation.

7. Deadzone phenomena, characteristic of poorly designed $\Sigma\Delta$ modulators, and seen in previous accelerometer designs will be removed.

8. A more accurate model for EM $\Sigma\Delta$ modulators will be built so that previous design failures can be analyzed more thoroughly.

9. The designed model is expected to be verified by simulation results and experimental data from actual MEMS accelerometers and a new readout design.

10. A new readout ASIC will be designed in order to implement all of these improvements. The ASIC should be flexible enough to explore trade-offs between noise, full scale range and stability. This new ASIC will be implemented in a better fabrication process than the previous implementations, in order to improve the performance of the readout, and the $\Sigma\Delta$ modulator.

In order to achieve these results, several circuit level improvements will also need to be implemented. In order to decrese quantization noise and improve stability, sampling frequency of the readout ASIC must be reduced. Hence, settling times of the OTAs will need to be reduced. Moreover, in order to improve bias stability, bias voltage of critical blocks in readout will need to be generated inside the ASIC, which will be much more controllable than external sources. As a last remark, the implemented system should be able to interface with a microcontroller.

1.5 Outline of This Thesis

Remainder of this thesis is divided into five chapters, with Chapter 2 beginning from the principles of EM $\Sigma\Delta$ modulation. This chapter discusses basic EM $\Sigma\Delta$ modulators, starting from principles of $\Sigma\Delta$ conversion. A comparison with electrical $\Sigma\Delta$ modulators will be made,

and it will be shown that the techniques of analyzing purely electrical and EM ΣΔ modulators should be differentiated due to poor performance of the mechanical filter element. A proper model for basic second order EM ΣΔ modulators will be discussed in detail, and performance of the modulator using a practical accelerometer design will be evaluated.

Chapter 3 discusses the design of a higher order "unconstrained" EM ΣΔ modulator [21]. While originally intended for MEMS gyroscopes, it will be shown that this architecture is suitable for accelerometers as well. The unconstrained architecture allows arbitrary placement of modulator poles and zeros, significantly improving modulator stability while decreasing noise floor at the same time. Optimizations on the architecture will be made by a custom made MATLAB code and simulations, and trade-offs between noise, stability and full range will be investigated. Finally, a MATLAB simulation model including all expected noise sources will be presented. This simulation model will be used to predict the final results expected from ASIC implementation.

Chapter 4 discusses the electronic interface ASIC implementation of the unconstrained fourth order ΣΔ modulator. Detailed discussions will be made on design of critical circuit components such as front-end sensor interface, high speed OPAMPs, internal discrete integrator blocks, high voltage feedback blobks and the 1-bit quantizer/comparator.

Chapter 5 discusses the experimental results obtained from the fourth order readout circuitry combined with MEMS accelerometers fabricated in METU-MEMS facilities. Experimental setup will be described and results obtained from closed loop operation experiments will be shown. Test results will verify the trade-offs between noise, stability and full scale range.

Finally, Chapter 6 will end this thesis with comments on the performance of the readout circuitry and will discuss possible future works.

CHAPTER 2

Electro-Mechanical $\Sigma\Delta$ Modulation

2.1 Principles of Sigma Delta ($\Sigma\Delta$) Modulation

Sigma Delta ($\Sigma\Delta$) modulation is a popular and powerful technique, primarily used in data converter (A/DC and D/AC) circuits to achieve high resolution signals with low cost integrated circuit(IC)s. Perhaps the most important feature of $\Sigma\Delta$ modulation is the trade-off between signal resolution and bandwidth: as the signal bandwidth requirement is reduced, resolution of the output signal is increased. Due to the high bandwidth of modern CMOS ICs, this trade-off works to the advantage of the designer; which can use trade this high bandwidth for improved signal resolution. Obviously, such data converters work have to work beyond the Nyquist frequency of the signal of interest, and hence are called 'oversampled' data converters. Aliasing and noise problems in baseband are solved by moving the undesired signals and noise components to higher frequencies than the baseband. This technique, also known as noise shaping, is popularly used in many popular oversampled data converter circuits. These oversampled data converters with noise shaping characteristics are usually designed as complete blocks of small mixed-signal ICs and are also considered to be purely electrical $\Sigma\Delta$ modulators.

A basic $\Sigma\Delta$ modulator is shown in Figure 2.1. The defining characteristic of this loop, and all $\Sigma\Delta$ modulators is the usage of the quantizer block just before the feedback stage. This quantizer block can be realized by any data converter circuit, from single-bit comparators to large multi-bit pipeline AD/Cs.

What is critical is the theoretically infinite gain provided by the quantizer to every signal that fits within the bandwidth of the loop. While this characteristic guarantees that even
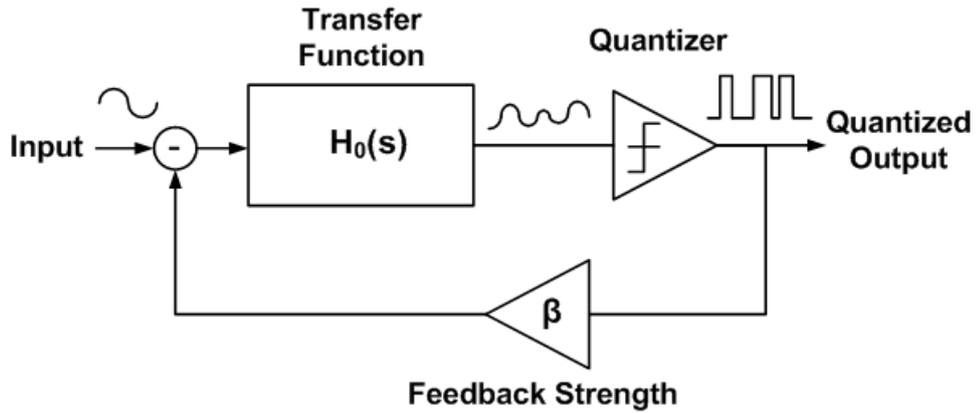
Figure 2.1: Block diagram of a ΣΔ modulator.

very slight perturbations in the input analog signal will be reflected to the output, it also introduces the designer with the non-linearity problem of the quantizer itself. In addition, the quantizer introduces an error between the analog input and digital output every time the quantizer is utilized. This error, called quantization error; is a critical parameter in ΣΔ loops and is assumed to be a white noise source introduced by the quantizer block for generic modulators. If not properly taken care of, this quantization noise can dominate the noise floor of a ΣΔ modulator; especially when a single-bit quantizer is used.

Fortunately, by modifying the loop transfer function H_0(s) it is possible to shape the quantization error or noise introduced by the modulator. In order to comprehend this feature, we have to look at Figure 2.2 which has an additional noise source N_{QN} introduced as the quantization noise. In order to make the analysis simpler, non-linear quantizer has been replaced by a linear element with gain of G_Q. For this linear system, the total noise introduced by the quantizer can be derived to be:

$$N_Q \quad = \quad N_{QN} \frac{1}{1 + G_Q \beta H_0(s)} \tag{2.1}$$

Where N_Q is the shaped quantization noise that is directly added to the loop. Note that the term βH_0(s) can be combined into a singular term H(s), which will be defined as the loop transfer function. We will not integrate G_Q into this term, since G_Q is a practically complex and non-linear term that depends on the input signal. As the input signal increases, G_Q is expected to decrease. For small signal analyses however, we can assume G_Q is relatively high. Also, it can be derived from Equation 2.1 that G_Q has no effect on the noise shaping

characteristic of the loop.
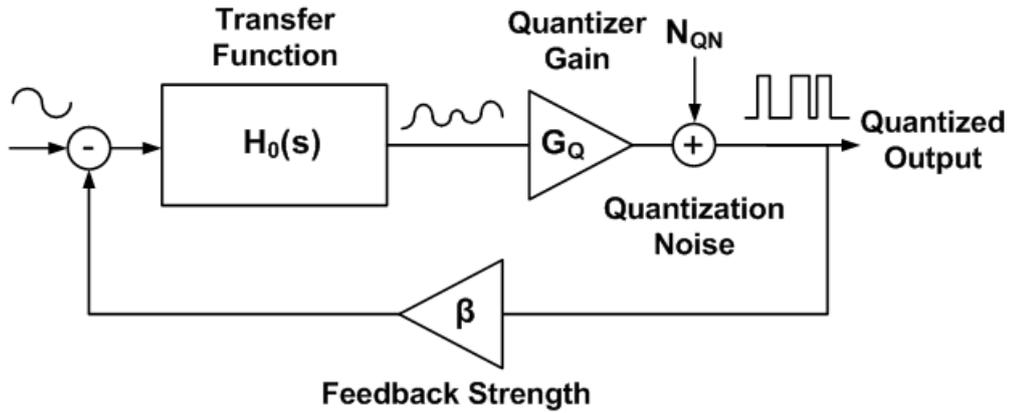
Figure 2.2: Linearized block diagram of a $\Sigma\Delta$ modulator with quantizer noise.

With these considerations in mind, we will define a term NTF_Q called the quantization noise transfer function. This term will define the transfer function from the white quantization noise N_{QN} to the shaped quantization noise N_Q. From Equation 2.1, it is trivial to determine NTF_Q as:

$$NTF_Q \quad = \quad \frac{1}{1 + G_Q H(s)} \tag{2.2}$$

NTF_Q or simply NTF, is a critical parameter in $\Sigma\Delta$ modulators and determines how quantization noise is shaped in the desired band of operation. The critical parameter here is the frequency dependent transfer function H(s). Poles of H(s) will appear as zeros in the NTF and hence will shape the quantization noise around those frequencies. Quantizer gain G_Q, theoretically, only modifies the amount of quantization noise generated. However in practice, the amount of noise or error generated by the quantizer will depend only on the resolution of the quantizer and loop full scale range (feedback strength). It is therefore, unnecessary to calculate G_Q; and it is only included in these equations for the sake of completeness.

Figure 2.3 shows the NTF of a $\Sigma\Delta$ modulator with a low pass integration transfer function of H(s)= 1/s. Note that due to the pole at DC, there is significant noise shaping around low frequencies (up to 100 Hz). From Equation 2.2 it is possible to deduce that the NTF is the inverse of H(s), and quantization noise within the band of H(s) will be significantly suppressed.

At this point, we can appreciate that H(s) and quantizer resolution are critical parameters defining various ΣΔ modulators with different functions. It is therefore natural to differentiate ΣΔ modulators depending on the transfer function order and quantizer resolution.

The first differentiation is due to the frequency characteristic and order of H(s). H(s) is typically chosen as either a low-pass or band-pass filter; which result in quantization noise suppression within those regions respectively. Bandpass ΣΔ modulators are typically chosen for narrow band signals around a carrier frequency, or in resonating structures such as gyroscopes. For the simple electronic ΣΔ modulator, we will consider the classic or low pass ΣΔ modulator.

Order of H(s), which is also defined as the order of modulator is also important. As can be expected, a higher order low pass transfer function has a narrower band and sharper cutoff, resulting in a much better noise suppression. Therefore, higher order ΣΔ modulators are usually preferred for low noise applications. However, increasing the modulator order above 2 results in multiple poles in the system, which can make the modulator unstable. In order to avoid stability issues, higher order modulators are carefully designed to avoid stability issues by either adding additional zeros to the transfer function, or more commonly by careful placement of pole&zero pairs. Unfortunately, due to system non-linearity, it is often not possible to determine the stability of high order ΣΔ modulators systematically. In the literature, ad-hoc calculations and transient simulation results are done for high order modulators to guarantee stability.

Figure 2.3 shows the NTFs similar modulators as in Figure 2.3 with first to fourth order transfer functions $H(s)=1/(s+10\pi)^N$, where N is the modulation order.

Quantizer resolution is another important parameter used in differentiation of ΣΔ modulators. Single bit and multi bit quantizers can be used in ΣΔ loops to achieve digital conversion and quantization. Single bit quantizers may seem a bit counter-intuitive at first, since they will introduce extreme amounts of quantizer errors (quantization noise) when compared to multi bit implementations. However, single bit quantizers have the advantage of inherent linearity due to well defined quantization values (±1), while multi bit quantizers can suffer from accuracy problems. Accuracy problems are more evident in fast quantizers such as pipeline or flash A/DCs where process mismatches can result in significant errors at the output. Since ΣΔ modulators require significant oversampling, using slow quantizers such as integrating
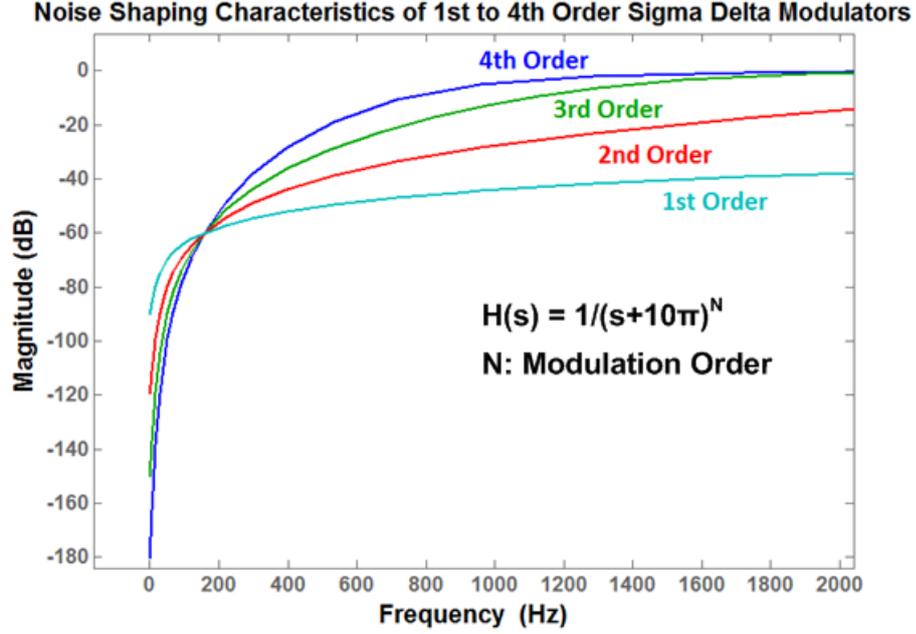
Figure 2.3: NTFs or noise shaping characteristics of first to fourth order $\Sigma\Delta$ modulators, shown with example transfer functions.

A/DCs are not an option, and accuracy problems must be considered in multi bit $\Sigma\Delta$ applications. Since the modulator output always follows the quantizer performance, these errors will directly translate as nonlinearity errors. For this reason, we will only consider single bit quantizers with ±1 outputs within this work.

Now that we have selected a modulator type, we can begin analyzing single bit, low pass $\Sigma\Delta$ modulators. We will first assume that the loop transfer function is a perfect low pass discrete filter with $H(z)=1/(z-1)^N$ and try to determine the shaped quantization noise generated by the modulator. Since we did not assume anything about the continuous nature of the filter, we can easily use a sampled filter instead; which will make the electronic implementation much easier.

Assuming quantization error is uniformly distributed between maximum and minimum range of the modulator, with Δ being the total range and e_Q being the quantization error, the RMS value of quantizer error will be:

$$e_{\text{RMS}} = \sqrt{\frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e_Q \, de} = \frac{\Delta}{\sqrt{12}} \tag{2.3}$$

We already know the noise transfer function of the modulator from Equation 2.2. Since the

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sampled nature of the signal is already encoded in H(z), sampled NTF will be no different than the continuous case:

$$NTF \quad = \quad \frac{1}{1 + H(z)G_Q}$$

(2.4)

Replacing H(z) with 1/(z-1) and assuming G_Q is large enough we obtain,

$$NTF \quad = \quad \frac{z-1}{z+G_Q} \approx \frac{1}{G_Q}\frac{z-1}{z}$$

(2.5)

Note that for an arbitrary Nth order transfer function H(z), the NTF will take the form,

$$NTF \quad = \quad \left(\frac{z-1}{z}\right)^N$$

(2.6)

Since we already calculated the RMS quantization error in Equation 2.3, we no longer need to determine G_Q to find the magnitude of error. Therefore, the RMS spectral density of the quantization noise will be found to be:

$$N_{Q(RMS)} \quad = \quad e_{RMS}\left(\frac{z-1}{z}\right)^N$$

(2.7)

Assuming a band of f_B within a sampling frequency of f_S such that $f_B \ll f_S$, we can determine the amount of total quantization noise for the whole f_B band to be:

$$N_{QB(RMS)} \quad = \quad e_{RMS}\frac{\pi^N}{\sqrt{2N+1}}\left(\frac{2f_B}{f_S}\right)^{N+0.5}$$

(2.8)

Note that in Equation 2.8, the shaped quantization noise in band will not be white just like in 2.3. Instead, the noise will be shaped by the NTF and this is why with there is a nonlinear relationship between bandwidth f_B and total RMS quantization noise $N_{QB(RMS)}$. As a last remark, we will define a new term called the oversampling ratio OSR=f_B/f_S and place it into Equation 2.8 to obtain,

$$N_{QB(RMS)} \quad = \quad e_{RMS}\frac{\pi^N}{\sqrt{2N+1}}\left(\frac{2}{OSR}\right)^{N+0.5}$$

(2.9)

In Equation 2.9 we can clearly see the advantage of using $\Sigma\Delta$ modulators. As the sampling frequency is increased and OSR is improved, quantization noise is expected to decrease significantly. A similar effect can also be reproduced by increasing N, the modulation order. However, in order to reach this result we have to remember that we made several important assumptions:

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1. H(z) loop transfer function is a perfect low pass filter with pole(s) at DC. The filter can be discrete or continuous, but the important thing is the availability of poles at DC or low frequencies. This filtering characteristic will be hard to obtain especially with electro-mechanical filter elements.

2. G_Q is large enough. Quantizer gain can be seriously decreased if the amplitude of the signal appearing at its input is large.

3. Baseband frequency is much smaller than the sampling frequency.

Considering these basic principles of $\Sigma\Delta$ modulators, we will first look at the purely electronic modulator before considering the electro-mechanical case.

2.2 Electronic $\Sigma\Delta$ Modulator and Finite OPAMP Gain

For the analysis of an electronic modulator, we will first consider a 2nd order $\Sigma\Delta$ modulator with a single bit quantizer as in Figure 2.4.
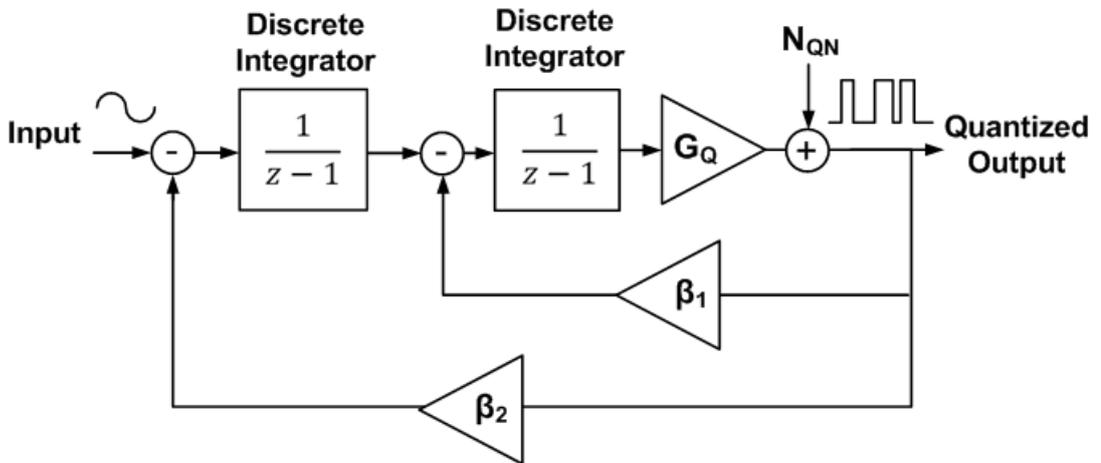
Figure 2.4: Linearized model of a second order electronic $\Sigma\Delta$ modulator.

From Equation 2.4 we can derive the NTF of this second order modulator to be,

$$NTF = \frac{(z-1)^2}{z^2 + (G_Q\beta_2 - 2)z + G_Q(\beta_1 - \beta_2) + 1} \tag{2.10}$$

Again, by approximating $G_Q \beta_2 >> 2$ and assuming G_Q is large enough, we can simplify Equation 2.10 into,

$$NTF \quad = \quad \frac{1}{G_Q} \frac{(z-1)^2}{z^2 + \beta_2 z + (\beta_1 - \beta_2)} \tag{2.11}$$

In order to draw the bode diagram and pole zero maps of the modulator, we will design the system so that G_Q=2000,and β_1=0.1 and β_2=0.3. For these values, the NTF will have the pole-zero map in Figure 2.5 and two pairs of z-domain poles and zeros at:

$$P_{1,2} \quad = \quad -0.05 \pm j\,444 \tag{2.12}$$

$$Z_{1,2} \quad = \quad 1 \tag{2.13}$$
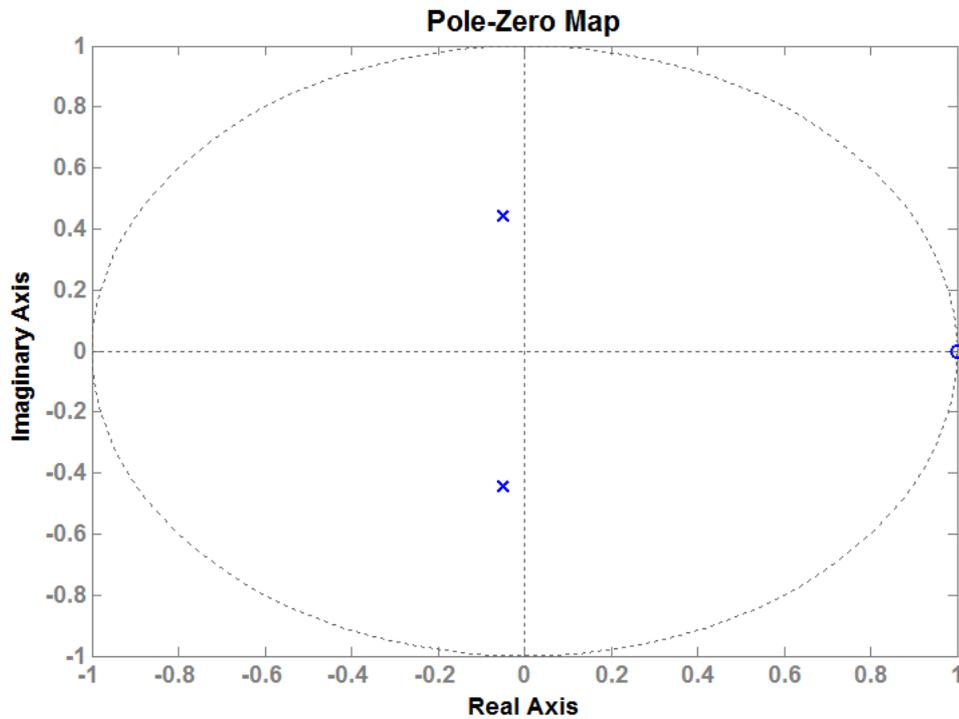
Figure 2.5: Pole zero map of the modulator in Figure 2.4.

Note that pole and zeros are inside or on the unit circle and the zeros are at DC, so the system is stable. Looking at the NTF, we will see its Bode magnitude plot (sampling frequency = 1 MHz) in Figure 2.6. Especially for frequencies below 10 kHz, a very sharp noise shaping behavior can be observed.

Up to this point, this modulator design seems very solid with guaranteed stability and significant noise shaping. The discrete integrators included in the transfer function can be easily

Bode Diagram
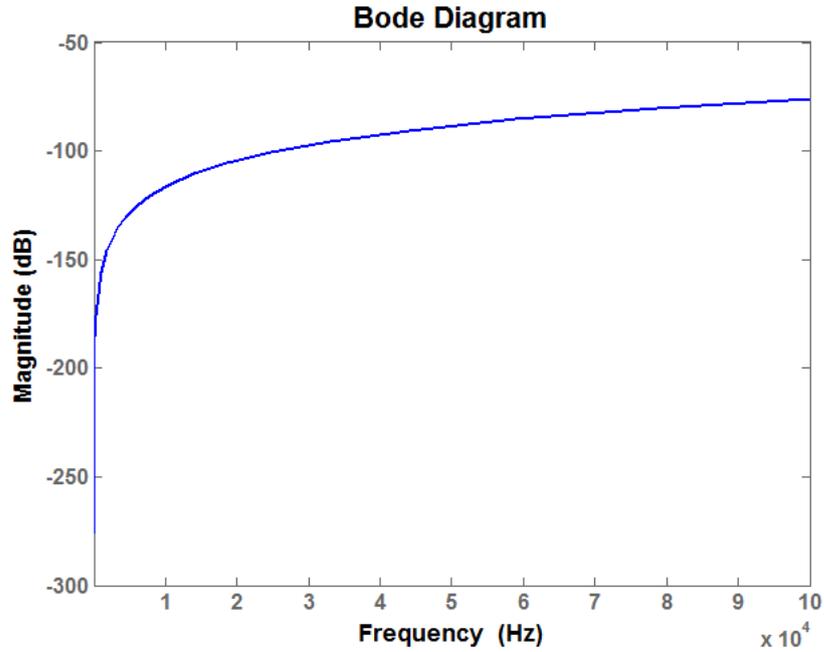
Figure 2.6: Bode magnitude plot of the NTF in Equation 2.11.

realized with switched-capacitor circuits in analog domain. However, by closer inspection of the terms we see that the gain for the integrators go to infinity at DC. It is impossible to find an analog counterpart for this behavior; because every analog integrator will leak some voltage and hence will not attain an infinite gain. For example, in Figure 2.7, the integrator gain is limited by the OPAMP gain A. Maximum voltage stored on the capacitor can be (A-1)V_I, and hence the integrator can only reach a gain of A-1. For extremely high values of A, capacitor leakage will be a limiting factor; since the capacitor will slowly discharge over its finite parallel resistance. However, we will assume that the capacitors are high quality and the OPAMP gain term A-1 dominates the integrator gain.

A leaky integrator corresponds to a stable low pass filter with a cut-off frequency higher than DC, and the discrete domain version of the integrator now becomes,

$$H_0(z) = \frac{1 - \dfrac{1}{A-1}}{z - 1 + \dfrac{1}{A-1}} = \frac{A-2}{(A-1)z - (A-2)} \tag{2.14}$$

The corresponding NTF is,

$$NTF = \frac{1}{G_Q} \frac{[(A-1)z - (A-2)]^2}{(A-1)z^2 + \beta_1(A-1)(A-2)z + (A-2)(\beta_2 - \beta_1)} \tag{2.15}$$

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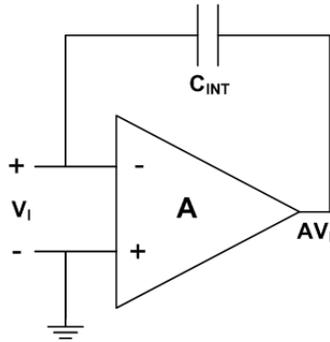
Figure 2.7: Simplified schematic of a discrete integrator during integration phase, showing input/output voltages for maximum gain case.

Looking at the NTF derived in Equation 2.15, we can see that the pole/zero positions are slightly different from the ideal case. However, the real impact of finite OPAMP gain can be observed by plotting the Bode magnitude plots of the idealized and finite OPAMP gain NTFs. By selecting a typical OPAMP gain of 60 dB, the comparative Bode magnitude graph in Figure 2.8 can be drawn.
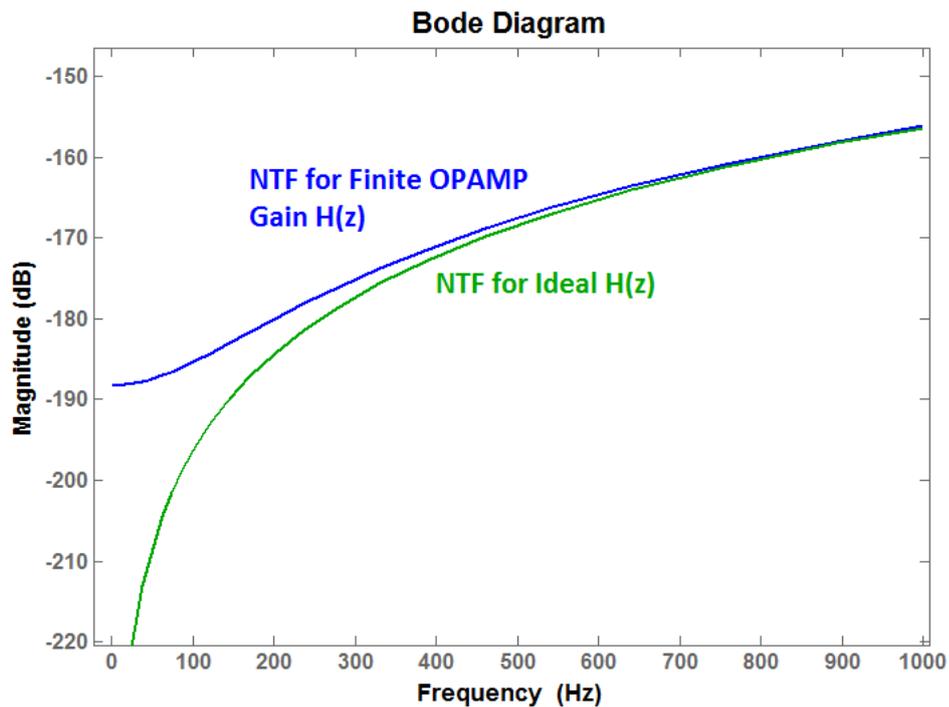
Figure 2.8: Bode magnitude plots of the idealized and practical NTFs in equations 2.11 and 2.15.

From Figure 2.8, it can be inferred that even a high OPAMP gain of 60 dB causes significant degradation in noise shaping for low frequency signals. It is also evident that for the finite

OPAMP gain case, the quantization noise expressions derived in 2.8 and 2.9 are no longer valid if f_B is small. For the case in 2.8, the cut-off where the practical and ideal quantization noise calculations diverge is about 1000 Hz. This band can be expected to be much larger for smaller OPAMP gain values.

2.3 Electro-Mechanical Sigma Delta ($\Sigma\Delta$) Modulator

After going over some basic concepts on $\Sigma\Delta$ modulators and electronic modulators, we now look at the main concern of this chapter: The Electro-Mechanical (EM) $\Sigma\Delta$ modulator. Different from the electronic modulator, the EM $\Sigma\Delta$ modulator uses mechanical filtering elements as the transfer function $H_0(s)$. For this work, we will consider the case where a micro mechanical, or MEMS capacitive accelerometer will be the mechanical filter element.

In order to understand how mechanical filtering is done, sense and actuation mechanisms of a MEMS capacitive accelerometer will be briefly described and the relationship between the MEMS sensor element and the electronic $\Sigma\Delta$ readout circuitry will be analyzed. Finally, mathematical models of the MEMS accelerometer element will be combined with the readout circuitry to obtain a comprehensive model of the accelerometer EM $\Sigma\Delta$ modulator.

2.3.1 Mechanical Filter Element: MEMS Accelerometer

MEMS accelerometers are mechanical sensor elements that detect the inertial force applied on them by the deflection of their sensitive elements. In a capacitive accelerometer this element is called the proof mass, and the deflection caused by the external force is detected as a change in capacitance between the electrodes of the accelerometer. Since the mass of the MEMS element is known from the design, the acceleration applied on the sensor can be directly converted into acceleration from Newton's law:

$$F \quad = \quad ma \tag{2.16}$$

Usually, the proof mass of the accelerometer is released as the moving element and the capacitive electrodes are fixed in position. This way, when the proof mass moves, the capacitances between the proof mass and electrodes are changed from rest values. Figure 2.9 shows such an accelerometer system with a proof mass in the center and electrodes on the sides. In order

to increase the sensitivity from proof mass displacement to capacitance, finger type structures are used between the proof mass and electrodes. The electrodes and proof mass are kept stationary by anchor structures. Last of all, elastic springs are placed on the sensitivity axis to regulate the amount of displacement due to inertial forces according to Stoke's law:

$$F \quad = \quad Kx \tag{2.17}$$
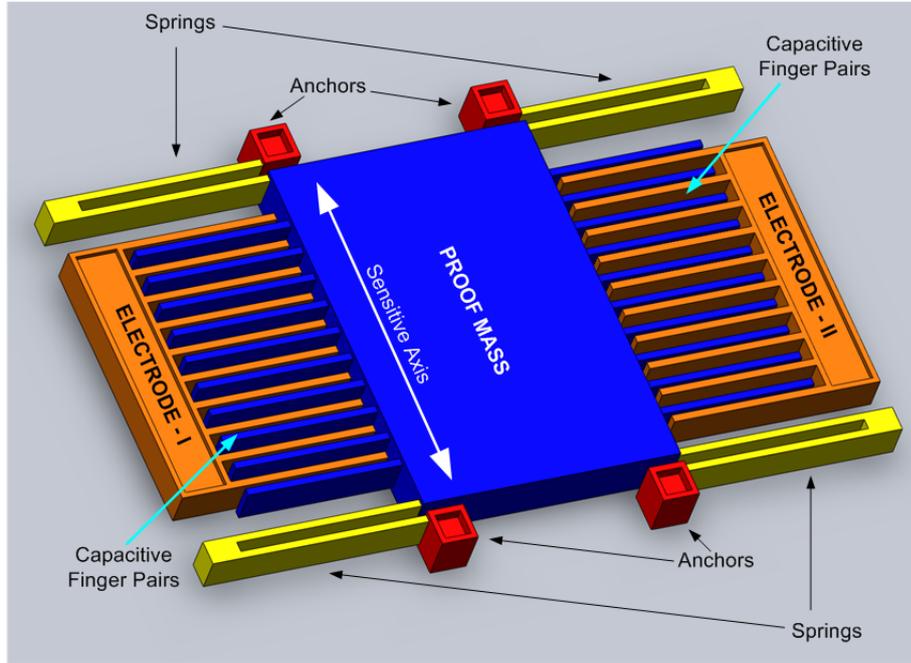
Figure 2.9: A capacitive MEMS accelerometer structure. Photo courtesy of Ilker E. Ocak [19].

Arranging equations 2.17 and 2.16 together we obtain,

$$x \quad = \quad \frac{m}{K} a \tag{2.18}$$

Equation 2.18 gives the total displacement due to acceleration for steady-state analysis. However, for a complete model that can be used in a $\Sigma\Delta$ modulator, we need the dynamic expression over the sampling frequency band. Thus, we will model the accelerometer as a second order spring-mass-damper system with a constant damping coefficient [19][12]. A spring-mass-damper system with a constant damping coefficient is known to have a transfer function in the form of

$$H_M(s) \quad = \quad \frac{m}{ms^2 + \beta s + K} \tag{2.19}$$

Where m is the proof mass, K is the spring constant in Equation 2.18, β is the damping coefficient and $H_M(s)$ is the transfer function from acceleration to displacement. By looking at $H_M(s)$ we can immediately make two observations:

1. $H_M(s)$ is in the form of a low-pass function, thus the accelerometer can be used as a filtering element for a low pass $\Sigma\Delta$ modulator.

2. $H_M(s)$ is a second order filter and proof mass velocity is neither observable nor accessible.

For the expression 2.19, we will also define two quantities: the resonance frequency and the quality factor of the sensor. The resonance frequency of a spring-mass-damper system is defined as

$$f_0 \quad = \quad \sqrt{\frac{K}{4\pi^2 m}} \tag{2.20}$$

The corresponding quality factor the resonant MEMS sensor is also known to be

$$Q \quad = \quad \frac{\sqrt{Km}}{B} \tag{2.21}$$

Since the objective of the MEMS accelerometer is to act as a mechanical low pass filter for the $\Sigma\Delta$ loop, it is desirable to keep the quality factor down, and hence the damping coefficient high.

The electronic interface cannot directly "sense" the displacement of proof mass, thus we need to calculate the sensitivity of proof mass-electrode capacitance to proof mass displacement. Again, we will consider the varying-gap MEMS accelerometer in Figure 2.9. For a varying gap structure, the capacitance dependent on position for a single sense finger is

$$C \quad = \quad \frac{\varepsilon_0 L h}{d - x} \tag{2.22}$$

Where L is the finger overlap length , h is the height or structural thickness of the same finger, d is the gap between the proof mass and electrode fingers and x is proof mass displacement. From Equation 2.22 we can calculate the sensitivity of capacitance to position to be

$$\frac{dC}{dx} \quad = \quad \frac{-N\varepsilon_0 L h}{(d - x)^2} \tag{2.23}$$

Where N is the number of proof mass sense fingers per side. For the MEMS accelerometer in Figure 2.9, it can also be seen that a proof mass finger is in the vicinity of two electrode fingers with different gap lengths. Since these fingers that belong to the same electrode are on the opposite sides of the proof mass, their effects need to be subtracted from each other. Then, Equation 2.23 takes the form of

$$\frac{dC}{dx} = -\varepsilon_0 L h \left(\frac{N}{(d_1 - x)^2} - \frac{N-1}{(d_2 + x)^2} \right) \tag{2.24}$$

Where d_1 is the gap width and d_2 is the anti-gap width. Typically gap and anti gap values are selected so that $d_1 < d_2$ in order to have a meaningful sensitivity. Equation 2.24 shows us that MEMS sensor sensitivity is dependent heavily on proof mass position. However, a $\Sigma\Delta$ modulated loop will have a very small static displacement due to acceleration and we will assume $x \approx 0$ for the calculation of sensitivity. The final form of Equation 2.24 is then

$$\frac{dC}{dx} = -\varepsilon_0 L h \left(\frac{N}{d_1^2} - \frac{N-1}{d_2^2} \right) \tag{2.25}$$

Note that there are two capacitances between proof mass and two electrodes, and as the proof mass moves in one direction, one capacitance will decrease but the corresponding capacitance pair will increase by the same amount. Accelerometers with this operation principle are known as fully differential accelerometers.

Finally, we have to derive the feedback term β, defining actuation strength. Actuation mechanism for varying-gap accelerometers are well known, and the total force acting on the sensor is dependent on the feedback voltage as in

$$F_{FB} = \frac{V^2}{2} \frac{dC}{dx} \tag{2.26}$$

Where V is the feedback voltage and dC/dx was derived in Equation 2.25. In an electromechanical $\Sigma\Delta$ modulator, the feedback will be pulsed and the expression derived in Equation 2.26 for continuous feedback will not be very accurate. We can modify the equation to account for pulsed natured of feedback with the addition of a variable t_p, which will denote the amount of duration of each pulse. More generally, we can define t_p as the difference between t_1 and t_s where t_1 is the time the initial pulse is applied and t_s is the sampling time. It is also not necessary to derive the force sensitivity expression, since the previous input from quantizer always has a fixed magnitude of one, and only sign of the applied force is changed. With this

interpretation, the force applied to the proof mass for each pulse will be

$$F_{PULSE} = \frac{t_p V^2}{2} \frac{dC}{dx} \qquad (2.27)$$

In frequency domain, we can express this pulsed behavior as the subtraction of two step functions with different delays and hence the laplace domain expression for 2.27 will be

$$F_{PULSE} = \frac{V^2}{2} \frac{dC}{dx} \frac{e^{-st_1} - e^{-st_s}}{s} \qquad (2.28)$$

Note that the maximum amount of force that can be applied to the sensor element is the multiplication of Equation 2.27 with f_s, or division by t_s. Therefore, maximum amount of force that can be applied to the sensor is

$$F_{PULSE} = \frac{V^2 t_p}{2t_s} \frac{dC}{dx} \qquad (2.29)$$

It is trivial to convert the applied force to acceleration by using the Newton's law in Equation 2.16.

2.3.2 Electronic Interface

Since a differential accelerometer is being used, we will also consider the electronic interface circuitry to be fully differential as well. This will give some advantages to the design such as elimination of correlated noise sources and the suppression of supply noise.

Block diagram of a basic readout circuitry is given in Figure 2.10. In order to convert the capacitance deviation (ΔC) into voltage, a C/V circuitry is commonly used. There are a variety of C/V converter architectures available at different accuracy and speed specs, however we will consider a generalized architecture where the amount of conversion from ΔC into ΔV is linear with a small amount of delay. If the sample and hold circuitry operating after the C/V converter samples it's input after the delay, then we can safely assume C/V conversion to be linear over the whole sampling frequency range.

From previous discussions in oversampling data converters, we had established that sampling frequency was of utmost concern in order to suppress quantization noise. For this reason, the architecture in Figure 2.10 is ideal for $\Sigma\Delta$ modulator implementations because of its simplicity. If the quantizer delay is kept low, the only delays arising from this readout circuitry are
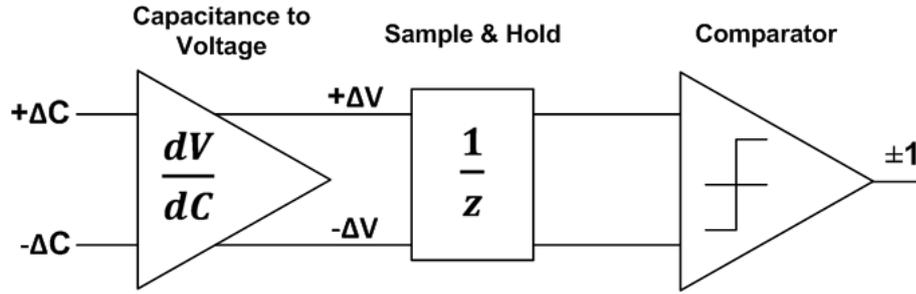
Figure 2.10: Block diagram of a generalized readout circuitry for a fully differential MEMS accelerometer.

due to the C/V converter and sample&hold circuit. Both of these circuit elements are usually limited by the speed of their OPAMPs, and hence designing a fast OPAMP is critical in order to reduce quantization noise.

Due to the architecture of the MEMS sensor presented in Figure 2.9, electronic sense and actuation mechanisms have to be multiplexed and actuation phase has to wait for the readout operation to finish. Therefore, sampling time of the circuit is the sum of actuation phase and delays due to sense phases. More specifically, sampling time can be defined as

$$t_S \quad = \quad t_P + t_{dC/dV} + t_{S\&H} + t_Q \tag{2.30}$$

Where $t_{dC/dV}$, $t_{S\&H}$ and t_Q are the delays due to readout circuit elements. Since t_P defines the amount of force applied to the sensor at each feedback cycle, we can observe that there exists a direct relationship between sampling time and maximum range of the sensor. A similar trade-off can be observed in Equation 2.3 where the amount of quantization noise is dependent on maximum range as well. Therefore, was can conclude that there exists several trade-offs between quantization noise and range of an electro-mechanical $\Sigma\Delta$ modulator.

It should also be noted that the electronic readout circuitry only contributes additional delay to the loop and does not add any pole/zeros to the frequency response. Therefore, with the presented electronic readout circuitry a $\Sigma\Delta$ MEMS accelerometer system is expected to be, by default, a 2nd order modulator.

2.3.3 Analysis of the Basic Electro-Mechanical ΣΔ Modulator

After establishing the behavior of the mechanical sensor and the electronic interface, we can start analyzing the complete electro-mechanical system. Simply by assembling the previously established electronic and mechanical blocks, the model in Figure 2.11 can be established.
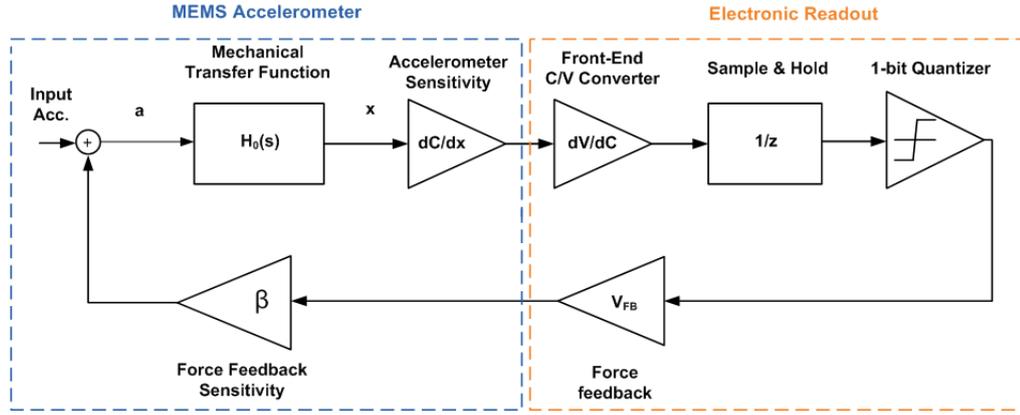
Figure 2.11: System level block diagram of a second order ΣΔ capacitive MEMS accelerometer.

One problem with this model can be immediately observed. There are two poles due to the the low pass transfer function of the mechanical sense element $H_0(s)$, but no zeros exist in the system. Therefore, if the two poles introduced by $H_0(s)$ are close to each other and system gain is large enough; then the ΣΔ modulator might be unstable. This problem is not present in purely electronic modulators since there is at least one zero in the transfer function.

In order to avoid such stability issues, a phase lead compensator, or a differentiator, can be used to stabilize the loop. Typically, such a compensator is implemented as a discrete switched-capacitor filter inside the readout, right after the sample & hold circuitry. More commonly however, sampling functionality is done automatically by the lead compensator and both blocks are combined inside the compensator. With this modification, block diagram of the generalized 2nd order modulator takes the form in Figure 2.12.

Where the phase lead compensator $H_C(s)$ is of the form

$$H_C(s) \quad = \quad \frac{z - 0.5}{z} \tag{2.31}$$

Note that theoretically, the zero placed by the compensator will at a much higher frequency than the poles of the mechanical transfer function, so the noise shaping behavior will not
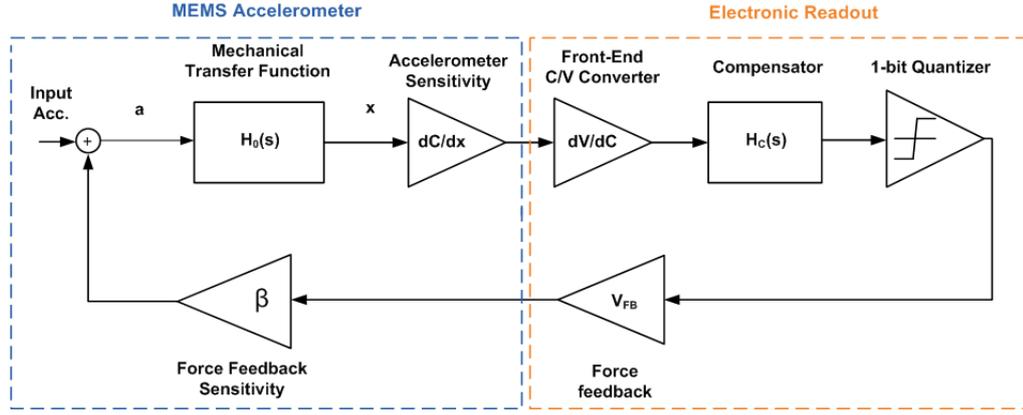
Figure 2.12: System level block diagram of a lead compensator stabilized second order ΣΔ capacitive MEMS accelerometer.

change. However in practice, the compensator will serve to amplify the output of the C/V converter for high frequency signals and noise components and will significantly decrease quantizer gain. This will be reflected as an increased quantizer error, and the theoretically calculated e_{RMS} value will be higher than expected.

Nevertheless, we will assume that the quantizer gain remains high despite the compensator and find the NTF of this ΣΔ modulator. By multiplication of the terms in the loop, we obtain the loop transfer function H(s) as

$$H(s) \quad = \quad \beta\, H_0(s)\, H_C(s)\, \frac{dC}{dx}\, \frac{dV}{dC} \tag{2.32}$$

We can replace β with the expression of feedback force of a single pulse in Equation 2.28. Substituting all the values and linearizing dV/dC into a constant gain term A we obtain the loop transfer function

$$H(s) \quad = \quad A\, \frac{V^2}{2}\, \frac{dC}{dx}\, \frac{e^{-st_1} - e^{-st_s}}{s}\, \frac{1}{ms^2 + \beta s + K}\, \frac{z - 0.5}{z} \left[\varepsilon_0 L h \left(\frac{N}{d_1^2} - \frac{N-1}{d_2^2} \right) \right]^2 \tag{2.33}$$

The equation derived in 2.33 includes both discrete and continuous domain terms and hence must be converted into a single domain before a meaningful NTF can be obtained. We will follow the discrete domain analysis and the methods shown in [21] to convert H(s) into z domain. First of all, we need to determine the poles of the mechanical transfer function; which gives the complex conjugate pair

$$s_m \quad = \quad -2\pi f_0 e^{j\theta_D} \tag{2.34}$$

$$s_m^* \quad = \quad -2\pi f_0 e^{-j\theta_D} \tag{2.35}$$

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such that

$$\theta_D = cos^{-1}(\frac{B}{2\sqrt{Km}}) \tag{2.36}$$

These pole solutions can be converted into their z domain correspondents by

$$z_m = e^{s_m t_s} \tag{2.37}$$

$$z_m^* = e^{s_m^* t_s} \tag{2.38}$$

The goal is to substitute s_m and s_m^* into the feedback actuation term β, and then convert the term $\beta H_0 s$ into discrete domain. This conversion will not be done here but the interested reader can see the derivation in [21]. In the end, we will obtain the expression

$$H_M(z) = \frac{\alpha}{z - z_m} + \frac{\alpha^*}{z - z_m^*} \tag{2.39}$$

such that

$$\alpha = \frac{V^2}{2K}\varepsilon_0 L h \left(\frac{N}{d_1^2} - \frac{N-1}{d_2^2}\right) e^{-j\theta_D} \left(\frac{(e^{-t_1 s_m} - e^{-t_S s_m})z_m}{2j\sin(\theta_D)}\right) \tag{2.40}$$

$$\alpha^* = \frac{V^2}{2K}\varepsilon_0 L h \left(\frac{N}{d_1^2} - \frac{N-1}{d_2^2}\right) e^{j\theta_D} \left(\frac{(e^{-t_1 s_m^*} - e^{-t_S s_m^*})z_m^*}{-2j\sin(\theta_D)}\right) \tag{2.41}$$

In Equation 2.39, $H_M(s)$ denotes the transfer function due to the mechanical sensor, or the combination of $H_0(s)$ and β. Since the remaining terms are non variant with respect to frequency (except $H_C(s)$), it is trivial to find $H(s)$ from $H_M(s)$ by multiplying it with $A\frac{dC}{dx}$. As a last remark, it should not be missed that $H_M(s)$ has an additional zero in the form of

$$z_z = \frac{\alpha z_m^* + \alpha^* z_m}{\alpha + \alpha^*} \tag{2.42}$$

After the derivation of H(s) from $H_M(s)$, we can finally determine the NTF as

$$NTF = \frac{1}{G_Q} \frac{1}{\frac{1}{G_Q} + H_M(s) H_C(s) A \frac{dC}{dx}} \tag{2.43}$$

At this point we have to appreciate that the primary poles and zeros of the NTF are due to the mechanical MEMS sensor, and the contribution of the readout circuitry to the NTF is minimal. This creates a number of problems for the accelerometer system as outlined below.

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1. The loop transfer function and NTF are dependent on the mechanical parameters of the accelerometer K,B and m; which in turn depend on the process quality during fabrication. Errors and mismatches during fabrication can create large discrepancies resulting from the shift of these mechanical values and hence shifts on the NTF as well.

2. Available values of K,m and B are usually not not flexible enough to allow the MEMS accelerometer to act as a high quality low pass filter. Hence, noise shaping in baseband (frequencies up to 1 kHz) is severely degraded. Even if a good MEMS accelerometer can be designed to fulfill the requirements of a good low pass filter, it will need to have an extremely large mass, a very small spring constant and a relatively large damping coefficient; making the implementation and fabrication tedious and expensive.

3. Accelerometer simulation and verification procedure is tedious, and even minor modifications to accelerometers in order to improve process conditions requires verification by simulations to minimize quantization noise.

Therefore, in order to observe the noise shaping characteristic of the NTF we have to select a suitable accelerometer design for implementation. In this thesis, MEMS accelerometers designed by Ilker E. Ocak in METU-MEMS facilities were used [19]. Table 2.1 outlines the complete specs of the accelerometer used in this thesis.

Table 2.1: Parameters of the MEMS accelerometer used in the EM $\Sigma\Delta$ modulator.

Parameter	Units
K	56.3 N/m
B (Air)	8.5 Ns/m
m	263.9 μg
d1	2 μm
d2	7 μm
Number of Fingers	351
h	35 μm
L	140 μm

Note that the accelerometer is not a very small design, with its total area encompassing 5 mm x 5 mm area. With the parameters in table 2.1, we will obtain the resonance frequency f_0 and

quality factor Q as

$$f_0 \quad = \quad 2.32 kHz \qquad (2.44)$$

$$Q \quad = \quad 0.455 \qquad (2.45)$$

Following the NTF analysis beginning from Equation 2.35, we will obtain the s domain poles of the mechanical transfer function at

$$s_m \quad = \quad 1.49 kHz \qquad (2.46)$$

$$s_m^* \quad = \quad 3.62 kHz \qquad (2.47)$$

In order to convert the mechanical transfer function into discrete domain, we need to specify the feedback voltage and sampling frequency. Considering a CMOS readout fabricated at 0.18-0.6μm process technology range, it is logical to choose a sampling frequency of 1 MHz and feedback voltage of 5V for closed loop operation. The discrete domain poles and zero is then determined to be

$$z_m \quad = \quad 0.9907 \qquad (2.48)$$

$$z_m^* \quad = \quad 0.9775 \qquad (2.49)$$

$$z_z \quad = \quad 0.9868 \qquad (2.50)$$

Finally, the NTF can be determined. After obtaining the corresponding NTF in MATLAB and multiplying the NTF with e_{RMS} to obtain an approximation quantization noise PSD function, the resulting noise estimation plot takes the form in Figure 2.13. For this estimation, G_Q was taken as 1000.

The minimum quantization noise power around 1kHz band is around -73.6 dB, which corresponds to an RMS noise of 208 μg/ $\sqrt{Hz}$. This is an extremely high value, and it is evident that the quantization noise shaping is not good around these frequencies. Moreover, by looking at the poles of the mechanical transfer function s_m and s_m^*, we conclude that the corresponding zeros of the NTF must be around these frequencies as well. Hence, the noise shaping is significantly worse than the purely electronic modulator case.

It is also obvious that the quantization noise formula in Equation 2.9 is grossly inaccurate for the second order electro-mechanical modulator. Therefore, in order to get accurate results a
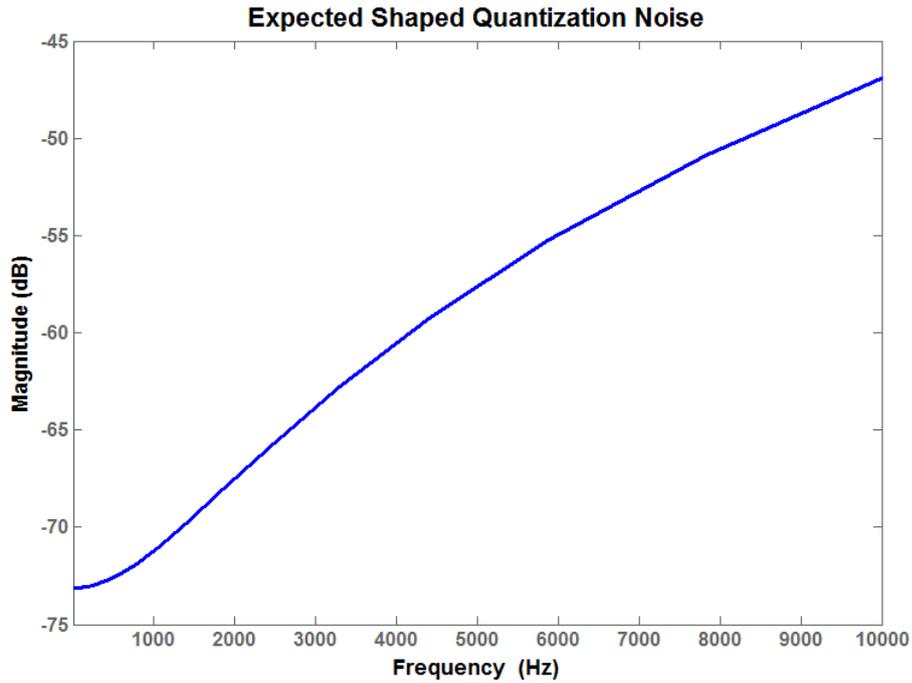
Figure 2.13: Noise shaping characteristics of a second order ΣΔ MEMS accelerometer.

simulation must be used to verify the operation of the modulator. It should also be remembered that the derivations and equations of the NTF up to this point are approximates and estimations, and a transient simulation is necessary to verify the stability and performance of the modulator. In this thesis, MATLAB Simulink will be used to simulate the ΣΔ modulators used in the design of electro-mechanical modulators.

A second order modulator model, including the MEMS sensor parameters in table 2.1 and constructed in Simulink is presented in Figure 2.14. Simulating the model with t_S = 1 MHz results in the output noise PSD in Figure 2.15. From the Figure, the average noise power in band can be extracted to be -73 dB, which corresponds to about 220 µg/$\sqrt{\text{Hz}}$. This simulated noise value is very similar to the expected value of -73.6 dB or 208 µg/$\sqrt{\text{Hz}}$ that we have found before.

One important discussion on these "bad" performance specs is to understand why quantization noise shaping for the electro-mechanical modulator is much worse than the purely electronic case. The answer lies in the fact that the mechanical sensor is a worse filter than the electronic discrete switched capacitor filters. While the electronic filters were limited by the gains of their OPAMPs, which is comparatively large; the electro-mechanical filter's transfer function

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Figure 2.14: Second Order ΣΔ MEMS accelerometer simulink block model.

Figure 2.15: Second Order ΣΔ MEMS accelerometer simulated quantization noise power.

is dominated by its pole pairs around the resonance frequency. So, in effect, it is possible to improve the performance of the electro-mechanical ΣΔ modulator by decreasing f_0 or K/m. However in order to decrease the resonance frequency significantly, a large proof mass with soft springs must be used. This is not desirable for applications requiring small sensors, since a massive accelerometer with soft springs will consume a huge amount of area as a die. It is much better solve this problem electronically, since we observed electronic circuits are much more adaptable to ΣΔ modulators compared to mechanical structures.

2.3.4 Deadzone in Electro-Mechanical ΣΔ Modulators

Another problem that appears with the electro-mechanical modulator is the deadzone phenomenon, commonly associated with ΣΔ modulators with filters having insufficient DC gain. In order to see how this problem comes to be, we need to look at the ΣΔ modulator block diagram again. Figure 2.16 shows the simplified block diagram of the second order ΣΔ accelerometer with all inputs and noise sources, including quantization noise set to zero. For this case, the steady-state solution can be found to be an oscillatory output with frequency proportional to f_S.
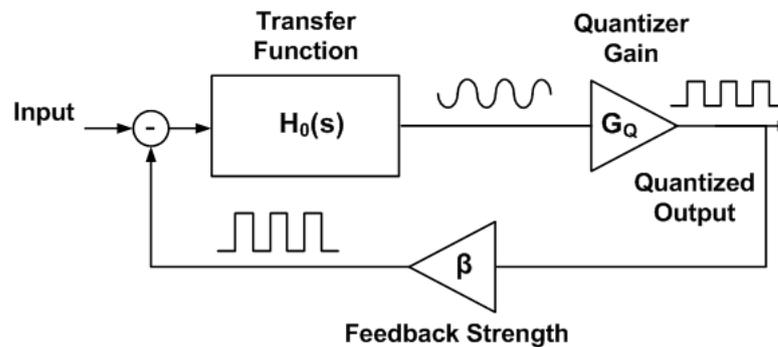
Figure 2.16: Simplified Second Order ΣΔ MEMS accelerometer model with noise sources removed.

Now, assume that there is a slight DC acceleration being applied to the system, as in Figure 2.17. As long as the applied acceleration is less than the amplitude of the oscillation, the system will keep oscillating at the same frequency. This is due to,

1. Electro-mechanical $H_0(s)$ has a finite DC gain, usually a moderate number expressed by the formula $x = a\dfrac{m}{k}$, and a DC acceleration therefore results in proportional displacement. In an electronic modulator, the discrete integrator circuit will have a much higher gain limited by its OPAMP.

2. The 1-bit quantizer only samples the sign of its input and does not care about amplitude. Therefore, as long as the DC perturbation does not cause the sign of the input to change at the time of sampling; output bit stream will remain the same.

This phenomenon results in an interesting conclusion: the output bit stream is the same for no acceleration case and a slight DC acceleration applied. Therefore, for an observer monitoring

the digital output, no acceleration change can be registered when the accelerometer is in dead-zone. This behavior can be easily checked at simulation level by applying a ramp response to the accelerometer and hence can be clearly in Figure 2.18, where the accelerometer output between ± 1 mg is constrained to zero g.
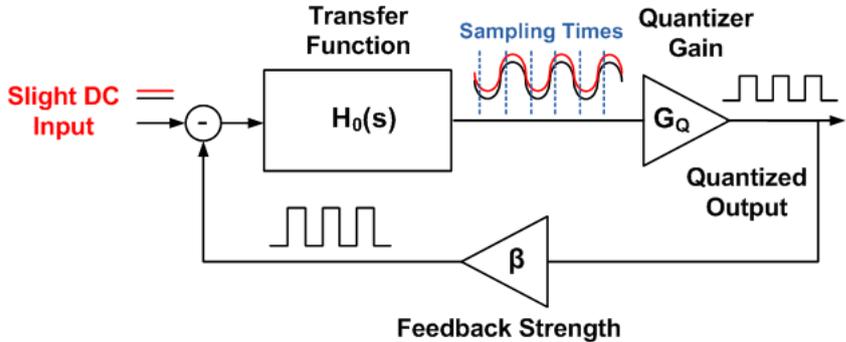
Figure 2.17: Simplified Second Order $\Sigma\Delta$ MEMS accelerometer model, showing the origin of deadzone.
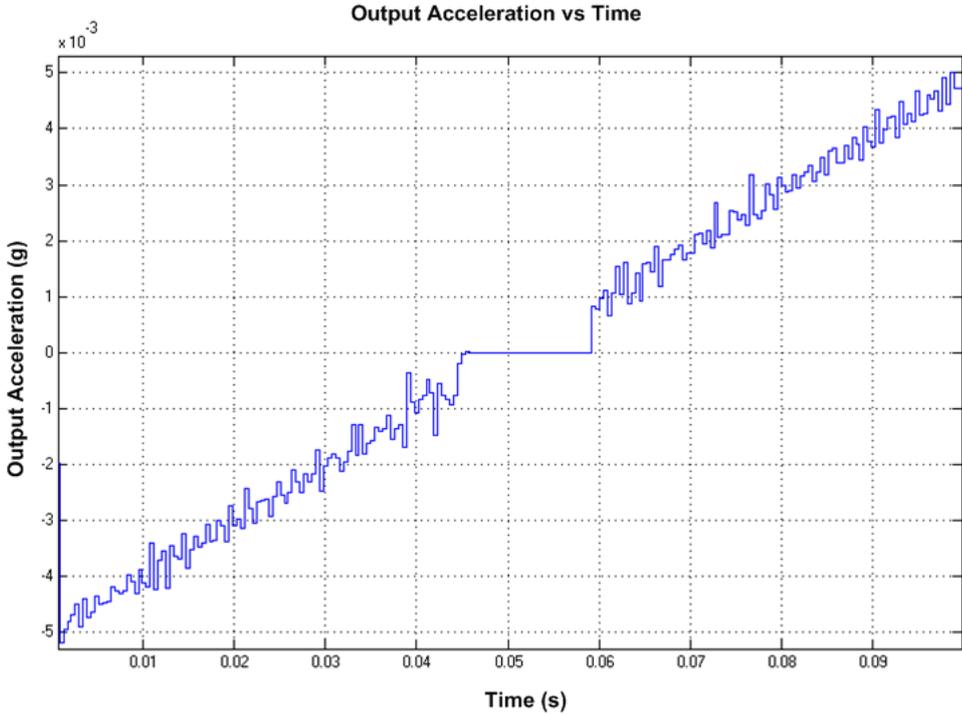
Figure 2.18: Deadzone seen at the output of a $\Sigma\Delta$ MEMS accelerometer in a ramped transient simulation.

There are various techniques that can be applied to improve the deadzone in second order $\Sigma\Delta$ accelerometers, however the best method is to eliminate the deadzone completely with

the addition of an integrator after $H_0(s)$ to improve the amplitude of input acceleration at low frequencies without increasing the amplitude of oscillation. We can also increase the ratio K/m to improve the sensitivity of the accelerometer to smaller perturbations, but this will increase the amplitude of oscillation as well. Note that the addition of discrete integrator(s) will increase the order of the modulator to a higher order, and can be expected to improve quantization noise as well.

Another solution to the deadzone problem is the addition of noise or dither, to a system in order to break the positive feedback oscillatory loop in Figure 2.17. If at any time the additional noise causes the sign of the oscillation signal to be sampled as "flipped", then the loop is broken and the modulator operates normally. In order to guarantee this behavior however, the dither added to the system must be comparable to the magnitude of the deadzone region, which can found to be ±1 mg in the simulations. This is not an elegant solution since it puts the designer at a very unproductive trade-off between deadzone and noise.

2.4 Summary of the Chapter

In this chapter, the electro-mechanical $\Sigma\Delta$ modulation technique used in performance improvement of MEMS accelerometers was introduced. Specifically, the second order $\Sigma\Delta$ modulator with single bit quantizer architecture was analyzed. Although the electronic $\Sigma\Delta$ architecture is simple, highly linear and allows spontaneous A/D conversion at high resolution; it was shown that the electro-mechanical modulator has significant problems with deadzone, quantization noise and sensitivity to process variations. It should also be remembered that we had to assume quantizer gain was relatively high in order to reach the results outlined in this chapter. When a compensator is used for stability reasons in a second order modulator, the effective quantizer gain will be expected to decrease and $\Sigma\Delta$ modulator noise shaping is expected to suffer even more [11].

All of these problems stem from the inefficiency of the MEMS sensor to act as a high quality low pass filter for the loop, and degrade stability by disallowing direct accessibility to the result first mechanical integration: proof mass velocity. Hence, filtering, noise shaping and stability characteristics of the $\Sigma\Delta$ modulator depend on the mechanical parameters of the MEMS accelerometer, which cannot be changed arbitrarily. Stable and noise efficient ac-

celerometer designs are counter intuitive to micro fabrication techniques and generally require low ratios of K/m values, or very soft springs combined with a huge proof mass. Moreover, variations on these critical process parameters are not controlled by the closed loop structure and directly affect the performance of the $\Sigma\Delta$ accelerometer.

In the next chapters, an improved higher order architecture to solve these problems will be introduced; and the focus of noise shaping will be shifted towards the electronic circuit. This will allow the implementation of a flexible NTF with much better noise suppression in base-band, eliminate the deadzone and improve compatibility with various accelerometer implementations. However, this does not mean that the reliance of the performance on mechanical MEMS sensor specifications will be eliminated. Instead, the specifications expected from the MEMS device will be much more relaxed compared to the demands of the second order $\Sigma\Delta$ accelerometer.

CHAPTER 3

Design and Analysis of an Unconstrained Fourth Order EM $\Sigma\Delta$ Accelerometer

Previous discussions and analyses in Chapter 2, Section 2.3 proved that the simple second order $\Sigma\Delta$ accelerometer is as good as its mechanical element. The necessity for high performance MEMS elements are however contradictory to requirements for cheap, small and reliable devices. A second-order $\Sigma\Delta$ accelerometer system needs a large MEMS accelerometer in order to avoid deadzone and achieve desired noise specifications. This requirement completely nullifies the most critical advantage of MEMS sensors: size.

In addition, second-order $\Sigma\Delta$ accelerometer systems have additional problems due to the implementation of a lead compensator in order to achieve stability. The lead compensator amplifies electronic noise at its input, and hence can significantly increase the amplitude of quantizer input [11]. This, in turn, decreases quantizer gain and further degrades the performance of the system.

Finally, reliance of the system on the mechanical element increases the sensitivity of the accelerometer system to process variations, and significantly limits system flexibility.

Considering these deficiencies, it is much more logical to let the readout circuitry dominate system noise floor and stability. The readout circuit can be programmed easily, increasing implementation flexibility. Letting the burden of noise shaping fall on the readout is also useful, since the readout circuitry can be more easily customized in order to minimize system noise. This process also allows the MEMS fabrication engineer to design the sensors in a more relaxed fashion, and encourages him/her to focus on reliability instead of performance.

The best way to shift the focus of noise shaping from MEMS element to the readout is by

building a high order $\Sigma\Delta$ modulator. The additional NTF zeros, or modulator orders, can be achieved by implementing discrete integrators on the readout to aid mechanical filtering. While high order EM $\Sigma\Delta$ modulators have been present for nearly a decade [18], many of these systems have problems with stability, and the high order readout circuits are designed to be specific to a sensor. Again, this increases sensor costs enormously since every new accelerometer design needs a new readout as well. In the commercial market, there is a growing demand for a standard type readout circuit that can drive *any MEMS accelerometer* within a high order loop.

This chapter focuses on the design and analysis of a newly emerging high order $\Sigma\Delta$ modulator architecture, called "unconstrained EM $\Sigma\Delta$", which has several advantages compared to previous high-order $\Sigma\Delta$ implementations [21]. Originally intended for gyroscope applications [22] and only theoretically analyzed for MEMS accelerometers, the unconstrained architecture will be analyzed for optimum accelerometer performance. Adjustments on the architecture will be made to improve flexibility of readout circuitry and explore the trade-offs between noise, stability and full scale range.

3.1   High Order Unconstrained EM $\Sigma\Delta$ Modulator

Unconstrained architecture for MEMS accelerometers was first proposed by Raman et. al. in their paper "An Unconstrained Architecture for Systematic Design of Higher Order $\Sigma\Delta$ Force-Feedback Loops" [21]. Figure 3.1 shows a generalized mixed-feedback architecture, applicable to any closed loop electro-mechanical sensor application.

The architecture in Figure 3.1 is significantly different than the second order $\Sigma\Delta$ modulator proposed in Figure 2.12. First of all, there is an additional electronic feedback path through H_{NS2} so the architecture is a mixed-feedback type. In addition, noise shaping filter H_{NS2} is added to improve modulator order by providing two additional orders of modulation. H_{NS1} and H_{NS2} are typically constructed from cascaded discrete integrators in order to provide additional electronic noise shaping.

It is possible to simplify the model in Figure 3.3 by integrating the compensator within H_{NS1}. We will not do the derivation here, but including H_C within H_{NS1} can be simply done by modifying H_{NS1} to include a feed-forward block to bypass the first discrete integration function
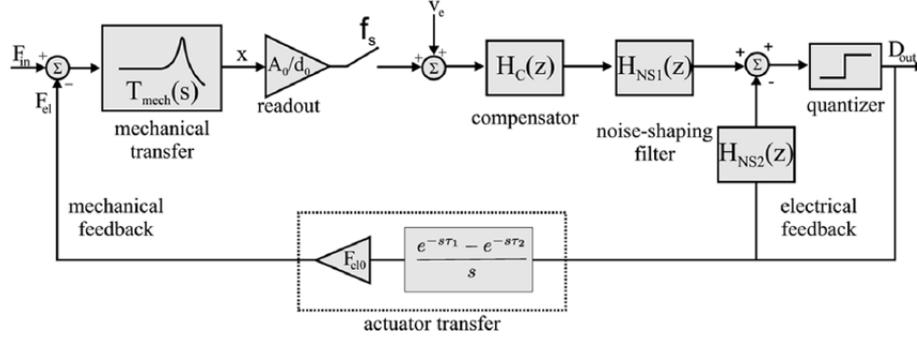
Figure 3.1: Model of the unconstrained mixed-feedback high order EM ΣΔ modulator proposed by Raman et. al. [21].

[21]. Implementation of H_{NS1} and H_{NS2} can also be combined inside a single block in order to simplify implementation.

Figure 3.2 shows such an implementation, with H_{NS1} and H_{NS2} combined into a single block. Note that the two discrete integrators increase modulator order by two, and along with two modulation order obtained by the accelerometer, the ΣΔ modulator will have a modulation order of four.

From the Figure, H_{NS1} (z) and H_{NS2} (z) can be derived to be

$$H_{NS1} = \frac{AB + CB(z-1)}{(z-1)^2} \tag{3.1}$$

$$H_{NS2} = \frac{DA + EB(z-1)}{(z-1)^2} \tag{3.2}$$

Equations 3.1 and 3.2 can assume the form of any double pole, single zero discrete transfer function depending on the values of A,B,C,D, and E. Thus, it is theoretically possible to implement any second order noise shaping function through H_{NS1} and $_{NS2}$. This is a very critical point, since it allows the stability of the modulator to be directly set by adjusting the zeros of H_{NS1} and H_{NS2}.

Another important note is about the poles of H_{NS1} and H_{NS2}. Equations 3.1 and 3.2 show that both transfer functions have double poles at z = 1, corresponding to DC frequency. In theory, this means that gains of H_{NS1} and H_{NS2} approach infinity as frequency approaches to zero, much like the case of the electronic discrete integrator in Section 2.2.

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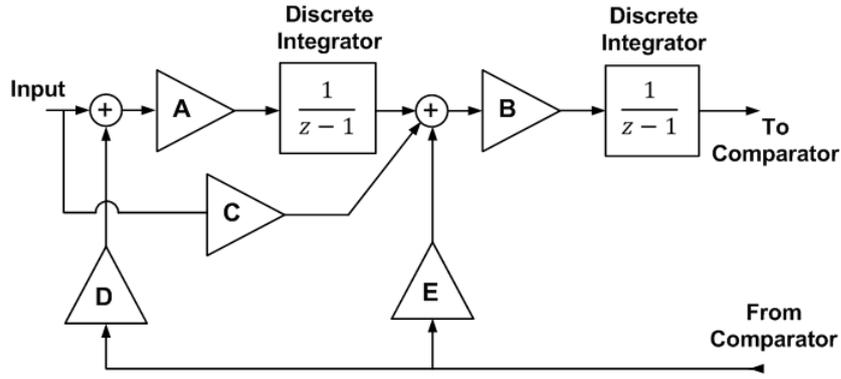
Figure 3.2: Block diagram of H_{NS1} and H_{NS2} noise shaping blocks integrated together.

However, just like the discrete integrators, DC gains of H_{NS1} and H_{NS2} will be limited by either capacitor leakages and/or OPAMP gains, and hence integrator gain will reach a limit. Assuming both integrators are limited by a shared OPAMP gain, and by defining $\alpha = 1/A$ where A is the OPAMP gain, H_{NS1} and H_{NS2} can be re-written as, [23]

$$H_{NS1} = \frac{(1-\alpha)^2 AB + (1-\alpha) * CB(z-1+\alpha)}{(z-1+\alpha)^2} \tag{3.3}$$

$$H_{NS2} = \frac{(1-\alpha)^2 DA + (1-\alpha) * EB(z-1+\alpha)}{(z-1+\alpha)^2} \tag{3.4}$$

Assuming A = 60 dB, the corresponding double poles can be found to be at,

$$z_{HNS1-1,2} = 0.999 \tag{3.5}$$

$$z_{HNS2-1,2} = 0.999 \tag{3.6}$$

The exact frequencies of $z_{HNS1-1,2}$ and $z_{HNS2-1,2}$ depend on the sampling frequency, however it can be easily assumed that the frequency domain poles correspond to low values. Therefore, like the discrete electronic $\Sigma\Delta$ modulator, H_{NS1} and H_{NS2} provides very good electronic filtering for the low frequency band. This information is very valuable for the following analyses.

It is also worth noting that, other than the adjustable zeros of H_{NS1} and H_{NS2}, the determined double pole frequency depends on the sampling frequency. This may seem to be counter-intuitive; after all, flexibility was one of the goals of such an architecture. Indeed, the general unconstrained $\Sigma\Delta$ architecture in [21][22] has additional feedback paths to adjust the poles of H_{NS1} and H_{NS2}.

The choice of double poles at extremely low frequencies is however, not accidental. As will be seen in following analyses, the presence of noise shaper poles at near-DC frequencies significantly suppresses quantization noise levels at low frequencies. This is a desired effect since the accelerometers are required to have low noise values for the low frequency bandwidth. Moreover, these poles can also help to suppress bias drift and random walk arising from electronic noise sources.

3.2 Design and Analysis of Fourth Order EM $\Sigma\Delta$ Modulator

In accordance with the analysis technique described in Section 2.3.3, we will begin analyzing the unconstrained $\Sigma\Delta$ modulator and convert all the model blocks into discrete domain. Before that analysis however, it is helpful to draw the block diagram of the simplified modulator. Fourth order modulation has been preferred in this thesis, since analytical results will show us that quantization noise is sufficiently suppressed and increasing modulation order furthermore is not necessary. Note that in the following analysis, the notation and variables described in Section 2.3.3 will be used. This is encouraged by the fact that much of the mechanical analysis and re-sampling methods introduced in that section is also applicable to unconstrained modulator as well.

Figure 3.3 shows the block diagram of the fourth order unconstrained $\Sigma\Delta$ accelerometer system. H_{NS1} and H_{NS2} are implemented as in Figure 3.2 with gain coefficients A-E to be determined by design.

For this architecture, we can combine and find the term $\beta \dfrac{e^{-st1} - e^{-st2}}{s} H_0$ (z) by deleting the compensator terms from Equation 2.33. We will name this function as $H_M(s)$, which will be equivalent to

$$H_M(s) \quad = \quad A\, \frac{V^2}{2}\, \frac{dC}{dx}\, \frac{e^{-st_1} - e^{-st_s}}{s}\, \frac{1}{ms^2 + \beta s + K}\, \left[\varepsilon_0 L\, h\left(\frac{N}{d_1^2} - \frac{N-1}{d_2^2}\right)\right]^2 \qquad (3.7)$$

Similar with second order EM $\Sigma\Delta$ analysis, we will find the conjugate poles of the mechanical transfer function in both s and z domains.

$$s_m \quad = \quad -2\pi f_0 e^{j\theta_D} \qquad (3.8)$$

$$s_m^* \quad = \quad -2\pi f_0 e^{-j\theta_D} \qquad (3.9)$$
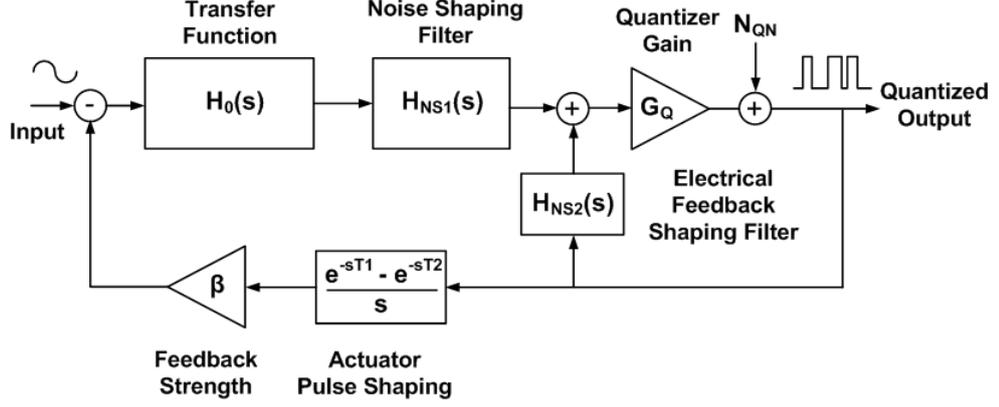
Figure 3.3: Unconstrained EM $\Sigma\Delta$ modulator block diagram.

such that

$$\theta_D \quad = \quad cos^{-1}\left(\frac{B}{2\sqrt{Km}}\right) \tag{3.10}$$

Discrete forms of the conjugate poles are,

$$z_m \quad = \quad e^{s_m t_s} \tag{3.11}$$

$$z_m^* \quad = \quad e^{s_m^* t_s} \tag{3.12}$$

In the end, we will obtain,

$$H_M(z) \quad = \quad A\,\frac{dC}{dx}\left(\frac{\alpha}{z-z_m} + \frac{\alpha^*}{z-z_m^*}\right) \tag{3.13}$$

such that

$$\alpha \quad = \quad \frac{V^2}{2K}\,\varepsilon_0 L\,h\left(\frac{N}{d_1^2} - \frac{N-1}{d_2^2}\right)e^{-j\theta_D}\left(\frac{(e^{-t_1\,s_m} - e^{-t_S\,s_m})z_m}{2\,j\,sin(\theta_D)}\right) \tag{3.14}$$

$$\alpha^* \quad = \quad \frac{V^2}{2K}\,\varepsilon_0 L\,h\left(\frac{N}{d_1^2} - \frac{N-1}{d_2^2}\right)e^{j\theta_D}\left(\frac{(e^{-t_1\,s_m^*} - e^{-t_S\,s_m^*})z_m^*}{-2\,j\,sin(\theta_D)}\right) \tag{3.15}$$

After determination of $H_M(z)$, we will need to derive the quantization NTF. Since there are two feedback paths in this architecture, we need to combine them in order to obtain the generalized loop transfer function H(z). From Figure 3.3 H(z) can be simply derived to be,

$$H(z) \quad = \quad H_M(z)\,H_{NS1}(z) + H_{NS2}(z) \tag{3.16}$$

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Quantization noise NTF then takes the form,

$$NTF \quad = \quad \frac{1}{1 + G_Q H(z)} \qquad\qquad (3.17)$$

Advantage of the unconstrained architecture is clear when equations 3.16 and 3.17 are considered. By adjusting the gain parameters A-E in H_{NS1} (z) and H_{NS2} (z), it is possible to adjust the NTF into desired shape and magnitude. This does not mean that NTF is dominated by H_{NS1} (z) and H_{NS2} (z), electro-mechanical transfer function H_M (z) still plays a great role in optimization of NTF, however it is no longer the solitary factor determining quantization noise and process critical parameters of H_M (z) can be easily relaxed.

If gain coefficients A-E and all the accelerometer and system parameters in equations 3.7 to 3.15 are known, then we can easily determine the quantization noise NTF for the given configuration. It then becomes possible to analyze the parameters that directly affect the NTF inside the desired bandwidth. Since the equations involved are very complex,a MATLAB command list was written to ease the task of design. These commands are given in Appendix A, and include plotting commands to help the designer visualize options available. The code can also be modified for parametric sweeps of MEMS sensor parameters, noise values and/or gain coefficient variables in order to optimize the performance of accelerometer system.

An important concern is the availability of H_{NS1} (z) and H_{NS2} (z) gain coefficients A-E in order to realize the desired transfer function H(z) and quantization NTF. In the circuit implementation of the noise shaper block (see Section 4.2.1), electronic feedback gains D and E were set to be adjustable by a programmable bank of capacitors. With the current implemented ASIC, D and E are equivalent to -3.3*C_{FB}/1.5 pF, where C_{FB} is the feedback capacitance setting of the readout. C_{FB} is adjustable between 0.1 pF and 1.5 pF, with steps of 0.1 pF; thus gain coefficients D and E are both adjustable between -3.3 and -0.22.

Other gain parameters A,B and C are defined in ASIC as fixed values and are set to be A = B = 0.25 and C = 8/3. However, the readout front-end gain term $\frac{dV}{dC}$ can be adjusted by changing C_{INT} integration capacitance, which is also programmable (see Section 4.1).

Thus, there are two programmable parameters, C_{INT} and C_{FB}, that can be modified to adjust the NTF. C_{INT} changes H_M (z), or the gain in forward path of the modulator, while C_{FB} changes strength of the electronic feedback. With adjustable H_M (z) and H_{NS2} (z), it is possible to modify H (z) according to specific accelerometers. Hence, it becomes possible to adjust

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the stability (dependent on H(z) zeros) and quantization noise (dependent on H(z) poles) parameters of a high order MEMS accelerometer system by only changing two readout parameters. For better control, the remaining gain coefficients A-C can also be made programmable to improve flexibility.

Another interesting parameter that modifies H(z) is the quantizer gain G_N, which is dependent on the input signal and amount of noise injected to the system. G_N is also hard to determine by analytical methods since it is used to model the nonlinearity of the quantizer, although thorough analyses do exist [16].

For further analyses and determination of NTFs, accelerometer parameters must be defined. We will use the MEMS accelerometer parameters in table 2.1, and assume the sampling frequency of modulator to be 1 MHz.

Figure 3.4 shows the quantization NTFs plotted for different values of V_{FB}, and fixed values of C_{INT}, C_{FB}, and G_N. Note that C_{INT} and C_{FB} can be fixed by default due to readout's programmability and G_N can be expected to be constant for a given input excitation. From the Figure, it can be seen that the optimization of readout and accelerometer parameters can be complex, even for a single variable, due to the innate complexity of the system.

In addition to quantization NTF, electronic noise NTF or NTF_E should also be investigated in EM $\Sigma\Delta$ modulators [11]. This arises from the necessity to determine the amount of electronic noise contributed to the system at high frequencies, and how much this noise affects the quantizer gain of this system. Even though electronic noise in midband can be easily calculated, if abnormal amount of electronic is present at higher frequencies then G_N can be expected to suffer and hence.

Quite similar to quantization NTF, NTF_E can also be calculated from equations 3.7 to 3.15, and is derived to be:

$$NTF_E(z) \quad = \quad H_{NS1}(z)\frac{1 - NTF(z)}{H_M(z) + H_{NS2}(z)} \tag{3.18}$$

Figure 3.5 shows a comparative plot of quantization NTF and electronic NTF_E of the fourth order modulator, along with the total expected noise power spectral density (PSD). Note that only a small impact of NTF_E can be seen in mid-frequency band, and quantization NTF still dominates system performance.
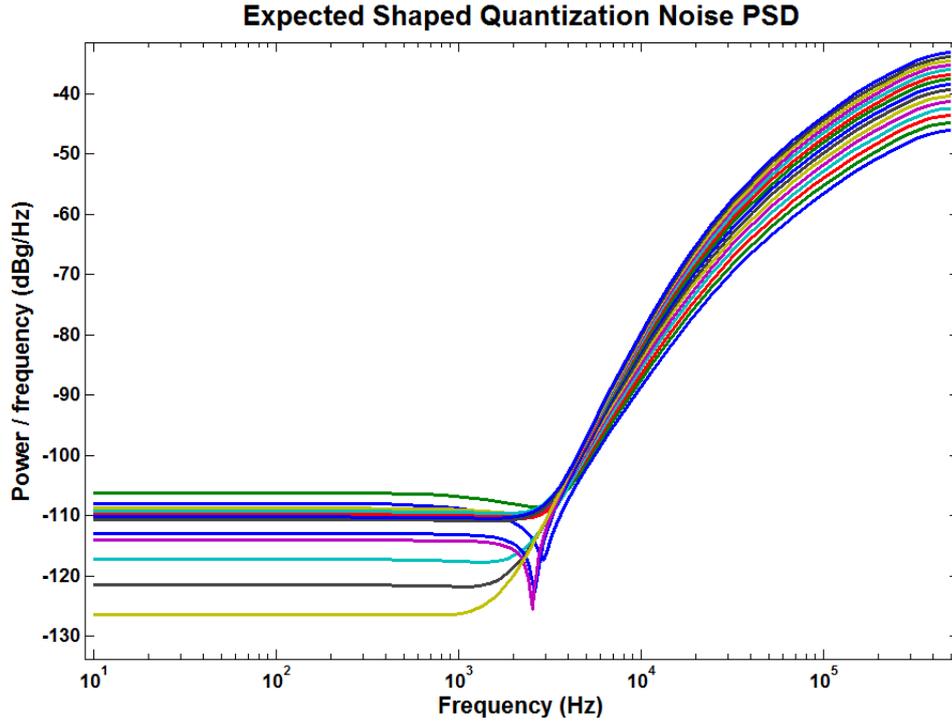
Figure 3.4: Expected quantization noise of the modulator for feedback voltages ranging from 7.5V to 16V. C_{INT} = 12 pF, C_{FB} = 200 fF and G_N = 350.

3.3 Model Verification and Simulations

The linear analysis method described in Section 3.2 is a good approximation of the fourth order unconstrained architecture, however this model should be verified by nonlinear transient simulations. Simulations are critical for modelling and implementation of $\Sigma\Delta$ modulators, since the modulator itself contains nonlinear elements, is subject to chaotic behavior and can be unstable. Therefore, simulation results can be expected to be better approximations than the expected noise results obtained from quantization and electronic NTFs since secondary effects are included in the simulations.

Moreover, modulator stability should be checked at simulation levels, since theories for stability of high order $\Sigma\Delta$ modulators are generally not analytical and depend on ad-hoc methods [24].
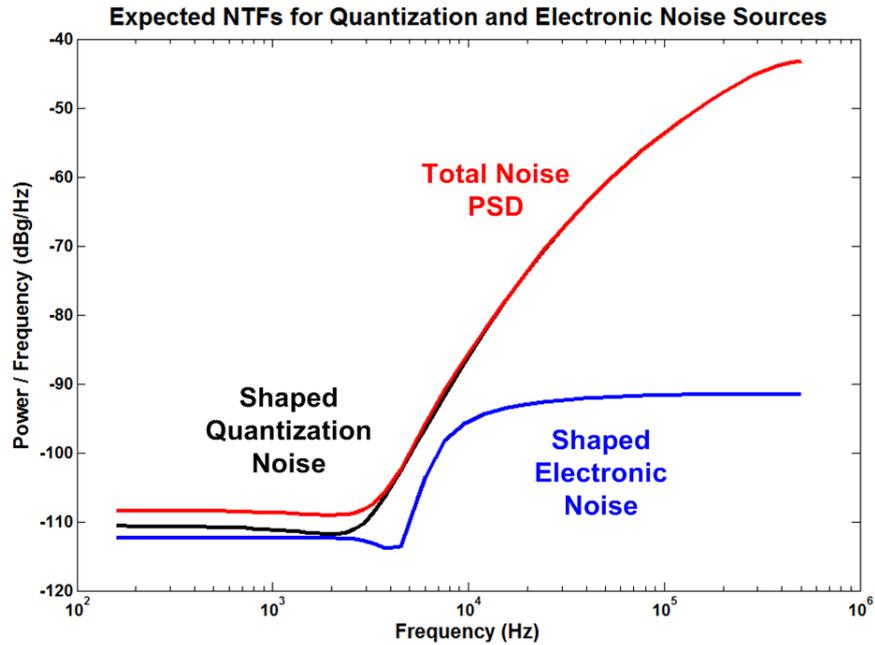
Figure 3.5: Expected quantization and electrical noise transfer functions, plotted for C_{INT} = 15 pF, C_{FB} = 100 fF and G_N = 350.

3.3.1 Nonlinear MATLAB-Simulink Model

MATLAB-Simulink environment was chosen to be a suitable environment for the simulation of the fourth order unconstrained accelerometer system. For this reason, a $\Sigma\Delta$ accelerometer model was constructed in Simulink environment and all electronic noise sources extracted from post-layout simulations of readout circuitry were included at simulation level in order to evaluate noise performance of the accelerometer.

Figure 3.6 shows the general Simulink model of the accelerometer used for simulations, and Figures 3.7 and 3.8 show the block diagrams of the electro-mechanical feedback and noise shaping blocks. Note that all nonlinear effects such as electronic saturation limits, 1-bit quantizer noise & drift sources and feedback pulse waveform nonlinearities are included in the model. Each block has been colored according to its sampling time by MATLAB, and hence sampling resolution of analog, discrete sampled and digital signals can be easily tracked.
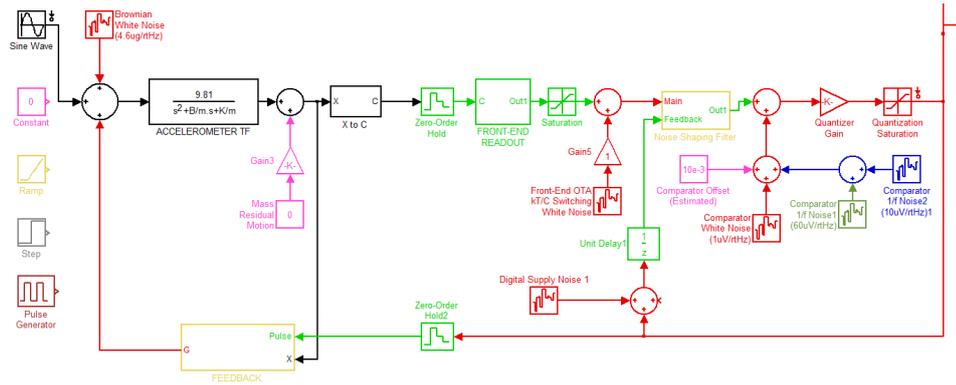
Figure 3.6: Constructed simulink model of the fourth order $\Sigma\Delta$ accelerometer.
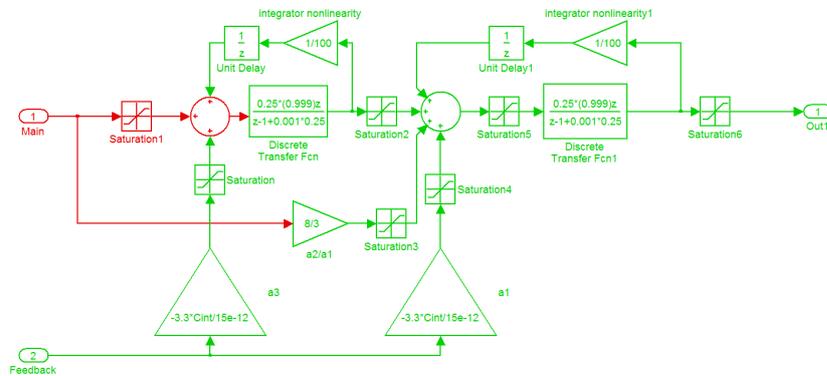
Figure 3.7: Noise shaper block in simulink model shown in Figure 3.6.
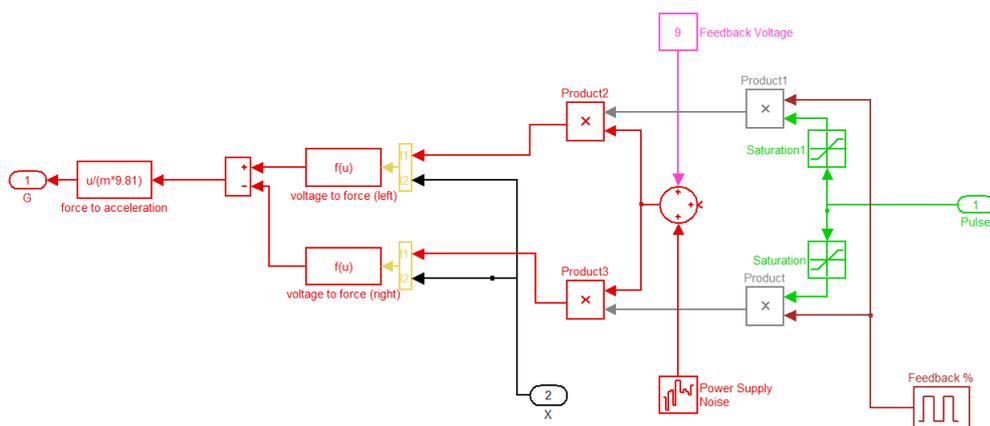
Figure 3.8: Feedback block in simulink model shown in Figure 3.6.

3.3.2 Simulation Results

By simulating the model constructed in Figure 3.6, we can obtain the simulated noise PSD
of the accelerometer circuitry. Figures 3.9 and 3.10 show the simulated noise PSDs of the
designed accelerometers when compared with theoretical expectations. Figure 3.9 contains
only the mechanical (brownian) noise of the accelerometer (see Section 3.4), while Figure
3.10 contains all noise sources including power supply noise Figures. For both Figures, simu-
lations and calculations were done for C_{INT} = 12 pF, C_{FB} = w00 fF and G_N = 350 settings. In
order to cancel out the undesirable effects of quantization, and to observe any possible mod-
ulator nonlinearities, simulation model has been applied 10 mg 100 Hz input excitation. No
noticeable harmonic distortion effects or limit cycles can be observed in the simulated PSDs.
It is important to mention that simulation results are in general agreement with the expected
NTFs derived in Section 3.2, which also proves that modulator stability is preserved.
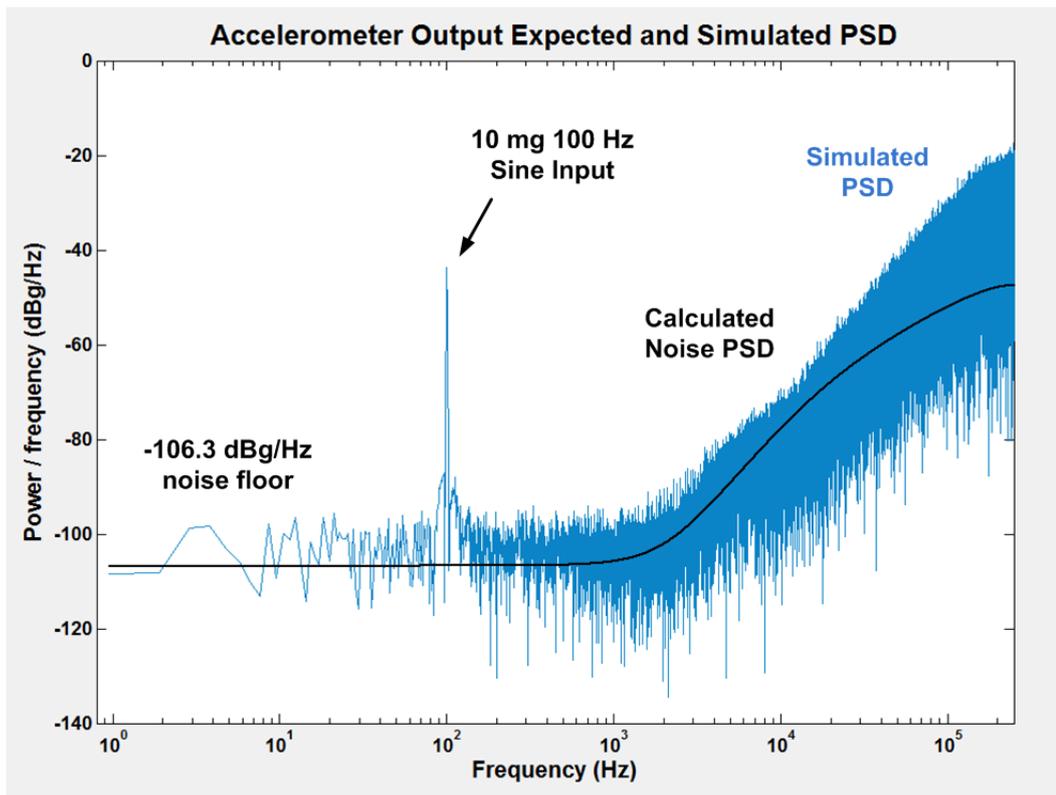
Figure 3.9: Calculated and Simulated PSDs of the designed $\Sigma\Delta$ accelerometer, with only
quantization and Brownian noise sources present.
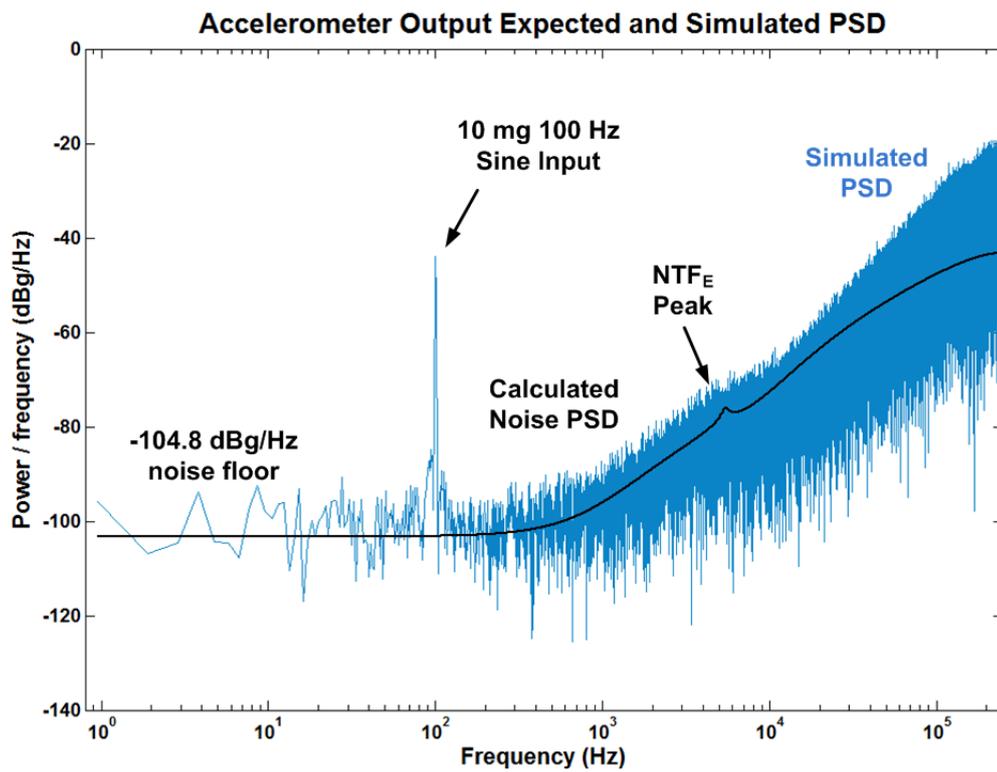
Figure 3.10: Calculated and Simulated PSDs of the designed $\Sigma\Delta$ accelerometer, with all noise sources included.

From simulations, the expected noise floor of the fourth order unconstrained $\Sigma\Delta$ accelerometer can be found to be -104.8 dB, or 5.75 $\mu g/\sqrt{Hz}$ for all noise sources included.

3.4 Noise Analysis

A complete noise analysis of the fourth order architecture is necessary in order to include the contribution of all noise sources. All the possible noise sources that can affect the fourth order accelerometer system are:

1. Quantization Noise: This noise is caused by quantization errors caused by the 1-bit quantizer, and is modeled well with the quantization NTF. The value of quantization noise inside the band should be estimated from the estimated NTF or from simulation results.

2. Front-End Electronic Noise: Caused due to electronic noise sources at the front-end amplifier. While NTF_E can be used to estimate the electronic NTF, in-band electronic noise is expected to be constant and hence can be directly estimated by multiplying the electronic noise with voltage sensitivity of the accelerometer. Noise sources from noise shaping blocks should also be combined with the noise generated from the C/V converter.

3. kT/C Noise: Caused due to folding of switch-capacitor noise into sampling bandwidth. Since kT/C noise also originates at the end of charge converter circuitry, it can be combined with front-end electronic noise at block diagram level.

4. Electronic Feedback Voltage Noise: Caused by the noise on the gain coefficients D and E, which are expressed as the ratio of 3.3 Volts * C_{FB} / 1.5 pF. Any amount of noise on the 3.3V reference voltage will directly affect electrical feedback coefficients D and E, adding some uncertainty to system output. For small amount of deviation of D and E, this noise can be modeled as an additional noise source applied through electronic feedback.

5. EM Feedback Voltage Noise: Caused by the variation on electro-mechanical actuation voltage V_{FB}, which is related with the force feedback applied to the system at each

cycle. Since force feedback is $\alpha\, V_{FB}^2$, this noise source actually affects the system nonlinearly and increasing V_{FB} results in a sharp increase in this noise source.

6. Brownian Noise: Caused by the mechanical motion of the accelerometer, and can be calculated

By estimating noise results expected from an ASIC implementation, we can obtain the expected noise results of the fourth order accelerometer system. We will estimate a white noise floor of 120 nV/$\sqrt{\text{Hz}}$ for the front-end C/V converter (including kT/C noise) and input referred noise of discrete noise shaping blocks. Therefore, the total electronic noise of the readout will be estimated as $\sqrt{2}$120 nV/$\sqrt{\text{Hz}}$ = 170 nV/$\sqrt{\text{Hz}}$.

We will also estimate both the electronic and actuation feedback voltage supply noises as 100 nV/$\sqrt{\text{Hz}}$. Since these noise sources are due to external supplies, an estimation of 100 nV/$\sqrt{\text{Hz}}$ is a good Figure for the low frequency band.

Finally, Brownian noise of the accelerometer can be found from the accelerometer parameters as, [19]

$$N_B \quad = \quad \frac{\sqrt{4\,\text{k}\,\text{T}\,\text{B}}}{m} \tag{3.19}$$

Calculating the contributions of each noise source we obtain the results in table 3.1. The estimated total noise value of 6.1 μg/$\sqrt{\text{Hz}}$ is close to the simulated results of 5.75 μg/$\sqrt{\text{Hz}}$.

Table 3.1: Estimated noise contributions from all sources in the fourth order $\Sigma\Delta$ modulator

Noise Source	Noise Power	Noise Magnitude
Quantization Noise	-110.8 dBg/Hz	2.88 μg/$\sqrt{\text{Hz}}$
Front-End (OTA+kT/C) Noise	-117.4 dBg/Hz	1.35 μg/$\sqrt{\text{Hz}}$
EM Feedback Voltage Supply Noise	-112.3 dBg/Hz	2.43 μg/$\sqrt{\text{Hz}}$
Electronic Feedback Voltage Supply Noise	-122.8 dBg/Hz	0.7 μg/$\sqrt{\text{Hz}}$
Brownian Noise	-106.7 dBg/Hz	4.6 μg/$\sqrt{\text{Hz}}$
Total Noise	-104.3 dBg/Hz	6.1 μg/$\sqrt{\text{Hz}}$

3.5 Summary of the Chapter

In this chapter, design and analysis of the fourth order unconstrained $\Sigma\Delta$ accelerometer system has been explained in detail. The mixed-feedback architecture was discussed, and programmable parameters have been evaluated. Flexibility of the architecture was also shown by the fact that variable readout gains can be adjusted the forward and electronic feedback path transfer functions. Hence, only by modifying the readout circuitry it becomes possible to adjust the NTF of the system and improve noise performance.

Noise transfer functions for electronic and quantization noise sources have been analyzed in detail. A MATLAB code was also written to evaluate noise performance of the accelerometer and to optimize the variable readout parameters. Nonlinear simulations in MATLAB have been conducted to verify the analytical models. Finally, expected noise performance level of readout ASIC implementation has been derived from noise analyses.

CHAPTER 4

Design and Implementation of the Fourth Order Readout ASIC

With the fourth order unconstrained $\Sigma\Delta$ model designed and verified, the next step is the design and implementation of the readout circuitry. From discussions in previous chapters, there are some constraints on and requirements for the design of the readout. Perhaps the most important of these requirements is about the sampling frequency. It was observed that increasing the sampling frequency of the system decreases quantization noise and increases stability for the unconstrained fourth order modulator. Therefore, the primary concern in the implementation of readout ASIC is the speed or settling times of individual circuit blocks. Other important design parameters are supply, OPAMP and kT/C related noise sources, integrator linearity, power consumption, temperature and drift(offset) immunity.

Considering all of these parameters, most of the readout was implemented with switched-capacitor circuits and filters. There are a variety of reasons for this:

1. Switched-capacitor filters can be adjusted to be offset free with the addition of auto-zeroing or correlated double sampling capacitors (see Section 4.1). While offset cancellation can also be achieved by chopper stabilization, auto-zeroing is generally favored in bandwidth critical applications.

2. Switch capacitor integrators are usually favored over their analog counterparts in order to avoid process mismatch and noise issues related with in-chip resistors.

3. Similarly, switched capacitor C/V converters have the advantage of a much faster response when compared to analog capacitive type TIAs.

4. Utilizing only capacitive elements as feedback elements and output loads allows the designer to simplify OPAMP design. Instead of standard OPAMPS, operational transcon-

ductance amplifier(OTA)s with high output resistance can be used. Since OTAs don't need an output buffer stage, their power consumption and speed is better compared to standard OPAMPs.

5. Switched capacitor filters are inherently discrete-time systems, and hence are more easy to integrate with the discrete EM $\Sigma\Delta$ model constructed in Chapter 3. Also by using a combination of multiple capacitors with different ratios, it is possible to build complex discrete functions from simple capacitors and OTAs (see Section 4.2.1).

However, there are also some disadvantages of switched-capacitor designs, which can all be addressed by careful design:

1. Switched capacitor filters suffer from an additional noise source, called kT/C noise, that arises due to randomness of the charge stored on capacitors. In order to limit kT/C noise, charge storing capacitors must be maximized and frequency of operation must be increased.

2. Switched capacitor designs require careful switch size selection and tricky implementation methods in order to limit charge injection and clock feed through phenomena[25]. Similar precautions must be taken at layout level in order to minimize charge injections through parasitic capacitances.

3. Due to the periodic nature of switched capacitor filters, it is impossible to linearize them around a time-invariant DC operating point. Hence, standard DC, AC and noise simulation techniques cannot be used for the simulation of switched capacitor circuits. Instead, time-extensive Periodic Steady State (PSS) simulations must be done in order to linearize the circuits around a time-variant periodic operating point. Fortunately the spectreRF simulator of Cadence Virtuoso Environment, available to METU-MEMS Center researchers, can run PSS analyses as well as periodic noise (PNoise), periodic AC (PAC), periodic transfer function (PXF) and similar analyses.

As a summary, the disadvantages of switched capacitor systems lie in their difficulty of implementation. As we shall see, it is possible to avoid most of these problems with careful design procedures. On the other hand, advantages of switched capacitor implementations in speed and offset cancellation can decrease accelerometer bias drift and white noise floor. The

troublesome kT/C noise, can be eliminated by aggressively increasing sampling frequency
and maximizing charge storage capacitors.

The general architecture of the designed switched capacitor fourth order readout circuitry can
be seen in Figure 4.1. For the sake of convenience, the readout circuitry will be divided into
two blocks: the front-end readout and back-end blocks. Front-end consists of core circuitry
including the switched-capacitor C/V converter and all supporting bias generators, regulators
and multiphase clock generators that are necessary in order to run the charge integrator circuit.
Back-end consists of the noise shaping filters, the comparator and high voltage control blocks.
Note that, while the back-end block controls the feedback cycles, it is the front-end that
contains the high-voltage switches that are used to give the adjustable feedback voltage to
the MEMS sensor.
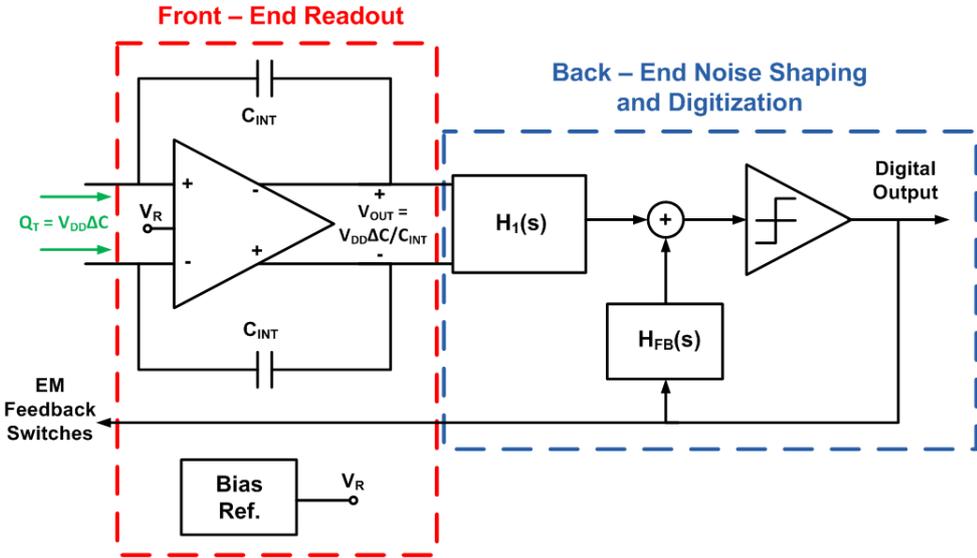
Figure 4.1: General architecture of the readout circuitry.

The following sections will discuss front-end and back-end blocks, with all sub circuits, in
detail.

4.1   Front-End Sensor Interface

Front-end sensor interface is the core of accelerometer readout circuitry, converting the po-
sition dependent capacitance between accelerometer electrodes and proof mass into voltage.

This C/V conversion is achieved by a fully differential charge integrator circuit as in Figure 4.2, and is based on the principle of charge conservation. Along with C/V conversion; offset and 1/f frequency components of the OTA are dynamically canceled at each reading thanks to an extra correlated double sampling (CDS) capacitor pair. This noise and offset cancellation technique is also known as auto-zeroing.

The main architecture used in this front-end interface is the fully differential architecture with a fully differential OTA, two differential accelerometer capacitances C_R, C_L and two identical reference capacitors C_{REF}.
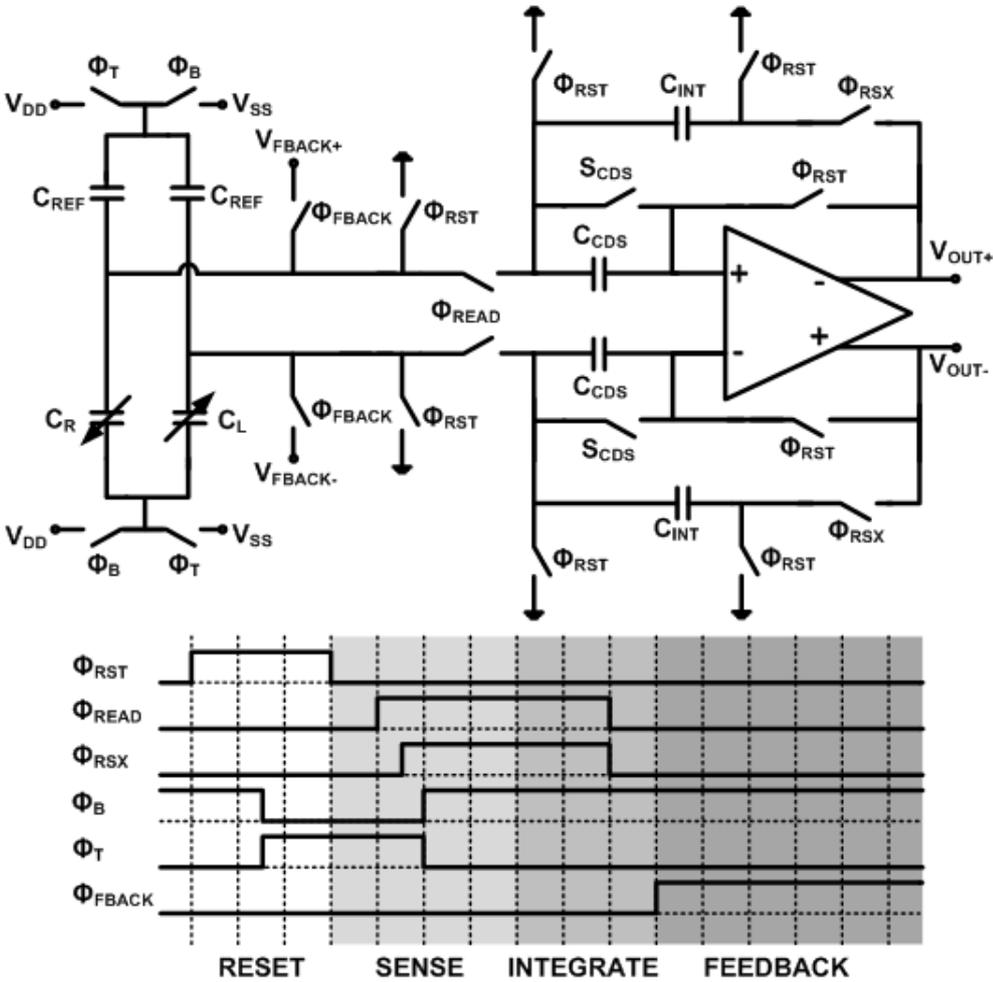
Figure 4.2: Front-end sensor interface or the charge integrator C/V conversion circuitry.

In order to understand the operation of the front-end interface circuitry, the timing diagram

in Figure 4.2 should be considered. Note that in addition to the timing diagram, reset phase of C_{INT} capacitor and the buffer phase of the OTA is active in both Φ_{RST} and Φ_{FBACK} cycles. This is done to guarantee the discharge action of C_{INT} capacitor and to allow the OTA to settle into buffer configuration before the sense phase begins.

Except S_{CDS}, which is a configuration switch to (en/dis)able correlated double sampling, all of the switches in the charge integrator circuit are controlled by a multiphase clock generator circuit, which is discussed in more detail in Section 4.1.3.

The reading or sense cycle of the charge integrator circuit starts with reset state, which also corresponds to state S0 in Figure 4.15. In this state, integration capacitances C_{INT} are shorted by forcing both of their electrodes to ground. Instead of using simple switches to short the capacitor, the capacitor has its both ends shorted to ground to make sure that the top plate of the CDS capacitors are also forced to the ground node at the same time. At the same time, OTA is forced into a buffer mode; where its input referred offset is stored on capacitors C_{CDS}.

After the accelerometer capacitances are discharged in Φ_{RST} phase; Φ_{READ} phase begins. During Φ_{READ}, the accelerometer is directly connected to the charge integrator circuit. Before this phase, it is necessary to avoid direct electrical connection between the accelerometer and the sensitive OTA, since the high amount of charge stored on MEMS device capacitors can suddenly discharge onto the OTA and damage the circuit.

After read phase begins, the readout circuit exits reset state and enters sense state, as in 4.15. In the sense state, the circuit stays in read and rsx phases, and reset switches are always off. In rsx phase, integration capacitances are connected to the OTA; and OTA is removed from buffer mode and put into integration mode with the capacitive feedback element C_{INT}.

At this state, the circuit is ready for C/V conversion. The exact conversion happens on the moment where Φ_B and Φ_T phases are interchanged at the same time. Before this moment, the total charge stored on two pairs of reference and accelerometer capacitances are:

$$Q_R(N-1) = -V_{SS}C_R - V_{DD}C_{REF} \tag{4.1}$$

$$Q_L(N-1) = -V_{SS}C_L - V_{DD}C_{REF} \tag{4.2}$$

The total charge stored on the right and left side of the MEMS device is given as Q_R and Q_L

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respectively. After Φ_B and Φ_T phases switch, the charges stored on the same nodes are:

$$Q_R(N) = (V_+ - V_{DD})C_R - (V_{SS} - V_+)C_{REF} \tag{4.3}$$

$$Q_L(N) = (V_- - V_{DD})C_L + (V_{SS} - V_-)C_{REF} \tag{4.4}$$

Due to charge conservation, $Q_R(N-1) = Q_R(N)$ and $Q_L(N-1) = Q_L(N)$. Hence solving for V_+ and V_- yields:

$$V_+ = (V_{DD} - V_{SS})\frac{C_R - C_{REF}}{C_R + C_{REF}} \tag{4.5}$$

$$V_- = (V_{DD} - V_{SS})\frac{C_L - C_{REF}}{C_L + C_{REF}} \tag{4.6}$$

The designed front-end interface is programmable, so the designer is always able to choose a C_{REF} such that $2C_{REF} = C_R + C_L$. Also, by defining a parameter $\Delta C = C_R - C_L$, we can simplify Equation 4.5 and 4.6 to:

$$V_+ = (V_{DD} - V_{SS})\frac{\Delta C/2}{C_R + C_{REF}} \tag{4.7}$$

$$V_- = (V_{DD} - V_{SS})\frac{-\Delta C/2}{C_L + C_{REF}} \tag{4.8}$$

This much potential difference is equivalent to a charge difference of $V_+(C_R+C_{REF})$ and $V_-(C_L+C_{REF})$, which will flow from the sensor and reference capacitors into the charge integrator circuit. This charge can only flow to C_{CDS} and C_{INT} capacitors.

C_{CDS} capacitors have floating ends at this stage, their bottom plates are only connected to the inputs of the OTA. Therefore, any potential difference on one end of C_{CDS} must follow the other. However, it should be remembered that during reset phase these C_{CDS} were charged with the input offset voltages. Therefore, at the moment of integration the relation between the two ends of C_{CDS} capacitors are:

$$V_+ = \frac{V_{IN+}C_{CDS} - V_{IN+}(N - 1)C_{CDS}}{C_{CDS}} + V_{CM} \tag{4.9}$$

$$V_- = \frac{V_{IN-}C_{CDS} - V_{IN-}(N - 1)C_{CDS}}{C_{CDS}} + V_{CM} \tag{4.10}$$

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V_{IN+}, V_{IN-} are the input voltages of the OTA and $V_{IN+}(N-1)$, $V_{IN-}(N-1)$ are the differential off-set voltages stored on the capacitors in reset phase. V_{CM} is the common mode offset voltage.

Assuming that the differential input offset voltage of the OTA does not change between and during the reset and sense states (in the time-span of several hundred nanoseconds), or equivalently if $V_{IN+}= V_{IN+}(N-1)$ and $V_{IN-}= V_{IN-}(N-1)$ then:

$$V_+ = V_- = V_{CM} \tag{4.11}$$

$$V_+ - V_- = 0 \tag{4.12}$$

Therefore, we have proved that the potential difference between V_+ and V_- voltages must be zero since the OTA is always trying to preserve the potential difference between its input terminals. Hence, all of the charge coming from the accelerometer must be compensated from C_{INT} capacitors.

Due to the feedback configuration, the OTA outputs will conduct charge to and from C_{INT} capacitors until all the extra charges $V_+(C_R+C_{REF})$ and $V_-(C_L+C_{REF})$ are canceled by an equivalent amount of charge delivered from OTA outputs. This will create a potential difference of V_{INT+} and V_{INT-} on the integration capacitors, which can be calculated to be:

$$V_{INT+} = (V_{DD} - V_{SS})\frac{\Delta C/2}{C_{INT}} \tag{4.13}$$

$$V_{INT-} = (V_{DD} - V_{SS})\frac{-\Delta C/2}{C_{INT}} \tag{4.14}$$

From Equations 4.11 and 4.12 we can derive that the difference of 4.13 and 4.14 is equal to the differential output of the OTA. Therefore,

$$V_{OUT+} - V_{OUT-} = (V_{DD} - V_{SS})\frac{-\Delta C}{C_{INT}} \tag{4.15}$$

It should be noted that Equation 4.15 is clearly independent of OTA input offset voltage, which was eliminated by the CDS capacitors.

4.1.1 Recycling Folded Cascode OTA with NCFF Compensation

The most critical analog component used in the CMOS readout circuitry is the OPAMP, used in various discrete-time switched capacitor circuits, such as the integrators in the internal

second order $\Sigma\Delta$ modulator/compensator, the front-end readout and sample & hold buffers. The OPAMP or OTA circuits used in the implementation of these switched-capacitor circuits directly affect noise, precision, speed and linearity of these systems.

For best performance in switched-capacitor circuits, operational transconductance amplifiers (OTAs) are better than standard OPAMPs; since the low output impedance of an OPAMP is not required for C/V converter or discrete integrator applications [12] and an OTA is simpler and much easier to design. In the case of a high performance 4th order $\Sigma\Delta$ accelerometer readout circuit, an exceptionally fast, low noise, and high dynamic range OTA is necessary. Fully differential architecture is preferred for improved CMRR and power supply noise suppression.

Considering all these points, a list of important performance criteria for the fully differential OTA can be assembled:

- Speed

- Gm (Amplifier Transconductance)

- Gain-Bandwidth Product

- Slew Rate

- Settling Time

- Noise

- Stability: Phase Margin

- Dynamic Range

- DC Gain

- PSRR

- CMRR

- Temperature Sensitivity

- Common Mode Voltage Stability

- Power Consumption

The designed OTA is required to meet respectable specifications for each of these performance criteria. In order to achieve fast settling with a good dynamic range, the folded cascode OTA architecture is preferred over telescopic and two-stage OTA architectures. For linearity reasons, class A amplifiers were preferred over their class AB counterparts with higher slew rates. Folded cascode architecture also provides good noise specifications when driven by high enough currents.

However, the folded cascode OTA is not ideal for high speed operations, since the additional folding node introduces an extra pole to the system and degrades the phase margin as well as the gain-bandwidth product. In order to remove this pole to higher frequencies, process technologies with wide transistors consuming enormous amounts of power, or small transistors with less parasitic drain and source capacitances are needed. This makes the speed-critical design of classic folded cascode OTAs limited by power and layout area considerations.

In order to combat these deficiencies, the recycling folded cascode OTA architecture is utilized [26]. Figure 4.3 shows the implemented recycling folded cascode amplifier with additional no capacitor feed-forward compensation to improve phase margin of the amplifier.
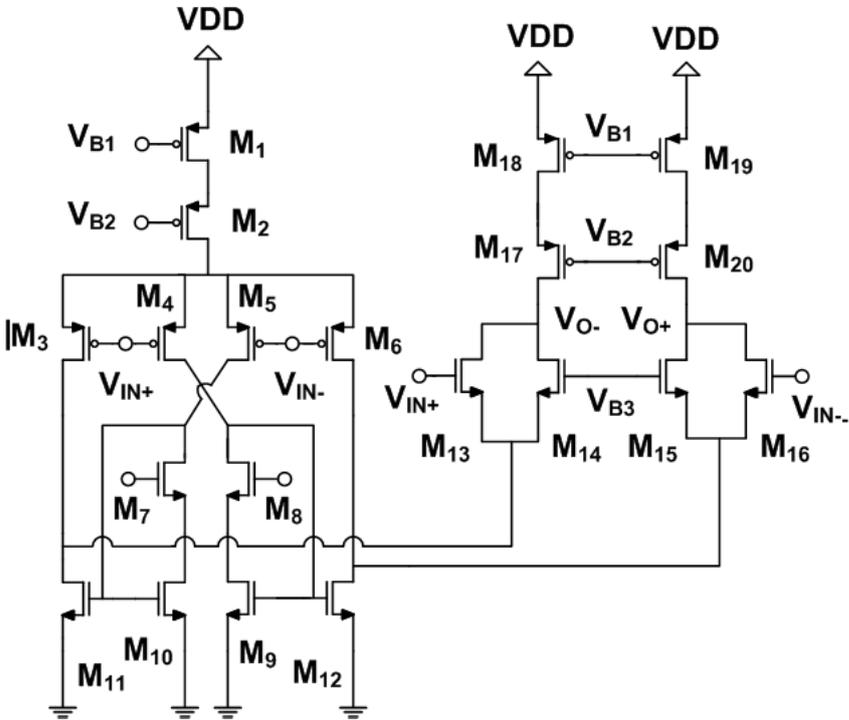
Figure 4.3: Schematic view of the recycling folded cascode OTA with NCFF.

The operational amplifier in Figure 4.3 is a modified type of folded cascode OTA, and the analysis of the amplifier can be started as if to analyze a folded cascode amplifier. Transistors M1 and M2 force a current I_{B1} through the identical quadruplets of M3-6 transistors. Hence, each transistor consisting from M3 - M6 conducts $I_{B1}/4$ current. Transistors from M7-12 are actually two parallel current mirrors that amplify the current received from M4 and M5 by a factor of K, which is the ratio of $(W/L)_{11}$ to $(W/L)_{10}$. The amplified current $(1+K) I_{B1}/4$ at each output branch is received by the transistor pairs of M13,M14 and M15,M16.

For the case of K = 2, the branch current is equivalent to $I_{B1}/2$; which is the case for a standard symmetric folded cascode configuration. However, for K > 2, the branch current and consequently the slew rate of the OTA is improved.

In order to determine the small signal transconductance characteristics of the OTA, a similar approach to the DC branch current case can be considered. Assuming that transistor set M3-6 is a perfectly identical quadruplet, and also assuming a frequency of analysis below the primary frequency pole; the small signal current through M11 and M13 will be:

$$i_{11} = i_{13} = gm_3(1 + K)(V_{IN+} - V_{CM}) \qquad (4.16)$$

Where V_{CM} is the common mode reference voltage and K is the gain of the current mirror. Neglecting the contribution from the feed-forward path transistors M15 and M18, the total differential mode gain of the amplifier can be calculated to be:

$$A_{DM} = (Kgm_5 + gm_6)(gm_{17}r_{O17}(r_{O13}//r_{O14}//r_{O6})//gm_{20}r_{O20}r_{O22}) \qquad (4.17)$$

With M15 and M18, assuming both transistors are identical, an additional transconductance term can be added:

$$A_{DM} = (Kgm_5 + gm_6 + gm_{18})(gm_{17}r_{O17}(r_{O13}//r_{O14}//r_{O6})//gm_{20}r_{O20}r_{O22}) \qquad (4.18)$$

Typically, gm_{18} needs to be smaller than gm_5 or gm_6, since the overdrive potential V_{GS18}, or the difference between the common mode potential and the drain of M13 and M14 needs to be large. It's also beneficial to keep $(WL)_{18}$ small in order to reduce the parasitic capacitances contribution of C_{GD18}. Combined with the reduction of the miller effect due to smaller gm_{18}, the small signal pole formed by C_{GD18} can thus be transferred to higher frequencies and the contribution from gm_{18} can be preserved even at very high frequencies where the folding and current mirror poles diminish the contributions from Kgm_5 and gm_6.

Thus, the overall low frequency small signal gain is dominated by $Kgm_5 + gm_6$, whereas the contribution from gm_{18} increases at higher frequencies. The effect of this contribution can be modeled as a high-frequency zero added to compensate the phase margin of the amplifier. Called no capacitor feed-forward compensation (NCFF), this technique is utilized in OPAMPs to improve the phase margin and gain-bandwidth product of the amplifiers by providing a low gain high frequency path from input to output. Combined with the recycling folded cascode's slower path through the current mirror, this amplifier has three transconductance paths from input to output, as illustrated in Figure 4.4.
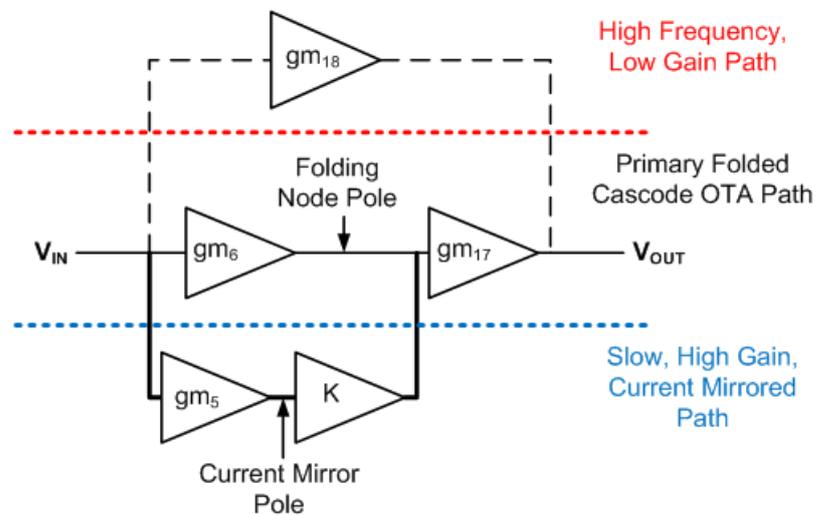
Figure 4.4: Simplified block diagram of the recycling OTA with NCFF in frequency domain, showing various paths from input to output.

The advantage of the three pathway amplifier is evident. At low frequencies, the slow path is dominant with its higher gain thanks to the amplification provided by the current mirror. After the first pole which is conveniently placed by the load capacitance, the current mirror pole is designed as the secondary pole. In the mid-frequency band where the gain is less than the DC gain, the contribution from current mirrored path is less and the primary path is dominant. In this range, no additional poles or zeros which can destabilize the system or increase the amplifier settling time are sought. Finally, at very high frequencies, the primary pathway is degraded and the feed-forward path becomes dominant.

When the amplifier is used in feedback, slower paths force the output; however the addition of an extra feed-forward path increases transconductance at higher frequencies, and improves

the phase margin. Improvements in phase margin value up to 15-20° are possible to achieve with carefully selected transistor dimensions, at the cost of only a small area increase and no additional power consumption.

One drawback is the addition of a pole to the system by the current-mirror path, on top of the zero provided by the feed-forward path. The addition of an extra pole-zero to the classic folded cascode amplifier, while seemingly innocent in frequency domain can be harmful in time domain. The amplifier system grows beyond a second order system, the analysis becomes more complex and the amplifier settling times are degraded. In order to make the system easier to design, system poles and zeros should be placed in such a manner to minimize their impacts on a second order system [27]. This can be achieved by placing the pole and zeros much further than the gain-bandwidth (GBW) product of the system. If this is not possible, then the additional pole and zero should be at high frequencies (greater than the GBW product) to minimize their impact.

Figure 4.5 shows the simulated AC response of the designed recycling folded cascode OTA with NCFF compensation, showing the relevant poles and zeros of the system. Two poles at 105 kHz and around 120 MHz are visible while the amplifier gain degrades to 0 dB at 370 MHz. An additional zero can be observed at around 1 GHz and the tertiary pole is around 2-3 GHz. Actually, there is an additional zero at 1.2 GHz and a fourth pole beyond 10GHz, but these cannot be easily deducted from the Figure. Clearly, all the additional poles and zeros introduced by the amplifier are at frequencies high enough to minimize the effect on the time-domain response of the system.

Another important factor in the design of the recycling folded cascode OTA is the current mirror gain, also known as K. When K = 2, the system is equivalent to a symmetric folded cascode OTA, however as K increases DC gain of the amplifier increases while the bandwidth is preserved. In turn, phase margin of system is degraded since increasing K moves the current mirror pole due to C_{DS13} to lower frequencies. In the implemented design, for the optimal stability and noise configuration, K is selected to be 1.5.

Fully differential implementation of the amplifier also requires a common mode feedback (CMFB) circuit to stabilize the common mode output voltage of the amplifier. Shown in Figure 4.6, CMFB circuit samples the average of output voltages and compares it to a reference
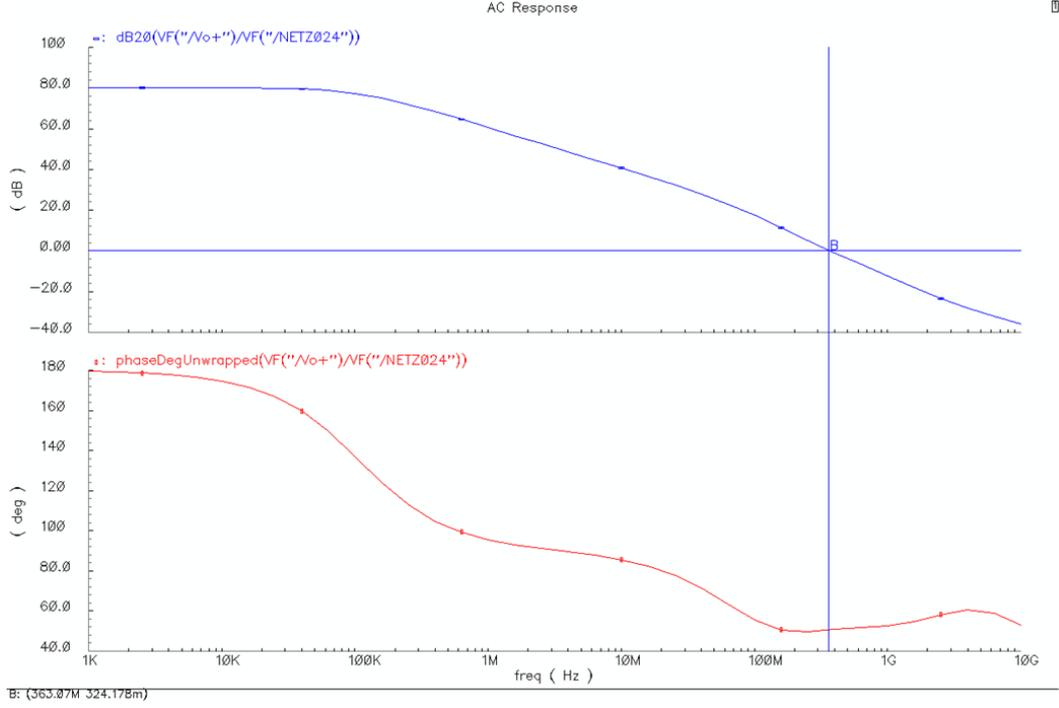
Figure 4.5: Frequency domain response of the designed recycling folded cascode OTA.

common mode voltage V_{CM} by a differential amplifier. The differential amplifier has two extra resistors R_1 and R_2 added to increase and convert the differential gain into common mode gain. V_{CMFB}, which is proportional to the difference between V_{CM} and amplifier common mode voltage.

The precise operation of the CMFB circuit in Figure 4.6 depends on accurate sampling of OTA common mode voltage and reference voltages. For this purpose, M3-M4 and M7-M8 pairs are always kept in deep triode region. Hence the total current passing through M2 and M6 are always proportional to V_{OUT+} + V_{OUT-} and V_{CM}. Since M1 and M5 are diode connected and assuming that M1 = M5; the resistance seen by these currents are $1/gm_1$. Thus, the total differential voltage seen by the differential amplifier consisting of M9-M13 is:

$$V_{DIFF\_IN} = \frac{(V_{OUT+} + V_{OUT-})(R_3//R_4)}{gm_1} \qquad (4.19)$$

Where R_3 and R_4 are the resistances of M3 and M4 in deep triode region and assuming that M3, M4, M7 and M8 transistor set is an identical quadruplet. In order to keep current consumption small, gm_1 is kept small which also increases R_3 and R_4.

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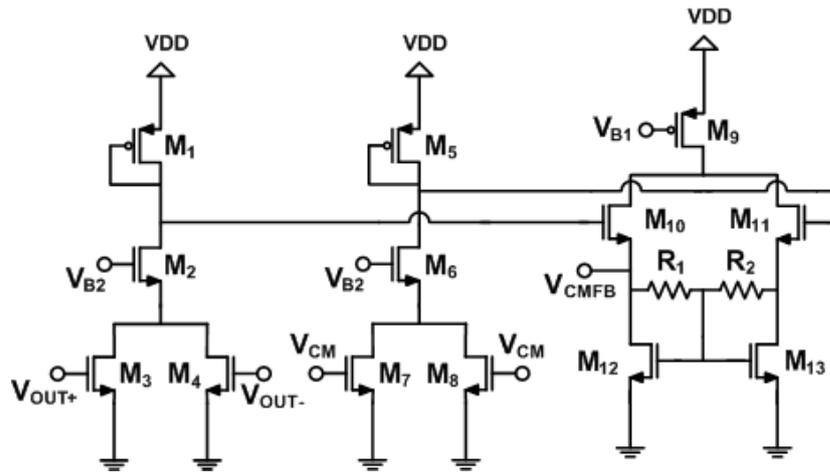
Figure 4.6: Schematic of the OTA CMFB circuit.

For a strong CMFB circuit (meaning a high immunity to common mode voltage variation over a large mismatch and temperature range) M1 needs to conduct a respectable amount of current to drive M10 and M11 into deep saturation region with low overdrive voltages. This is true since the deep triode resistance of M3-M4 and M7-M8 pairs cannot be arbitrarily increased for stability reasons, and a respectable differential voltage gain between amplifier output and reference common mode voltages is necessary. Therefore, transistors M1 and M2 are designed to conduct up to 100 µA for a high gain and stable CMFB circuit.

For the readout implementation, recycling folded cascode OTA with NCFF compensation is primarily designed for the front-end sensor interface, but the design is also used in the implementation of switched-capacitor integrators for the noise shaping modulator block. These two implementations have different slew rate and GBW requirements, so two OTAs were designed. The primary (front-end) OTA's device dimensions, including the CMFB circuit, are given in tables 4.1 and 4.2. OTAs used in integrator implementations are further discussed in Section 4.2.1.

Table 4.1: Transistor dimensions for the designed OTA (Figure 4.3) used in front-end sensor interface.

Transistors	W/L (µm/µm)	M (Gate Number)
M1, M2	14 / 0.7	28
M3, M4, M5, M6	14 / 0.7	22
M7, M8	14 / 0.7	16
M9, M10	18.5 / 3.15	6
M11, M13	28 / 3.15	6
M12, M14	10 / 2.8	6
M15, M16, M17, M18	14 / 0.7	4
M19, M20	14 / 1.4	18
M21, M22	14 / 0.7	16

Table 4.2: Transistor dimensions for the CMFB circuit shown in Figure 4.6 and utilized inside the designed OTA (Figure 4.3 and Table 4.1).

Transistor(s) or Resistors	W/L (µm/µm) or Resistance (Ω)	M (Gate Number)
M1, M5	6.2 / 4.2	1
M2, M6	6 / 4.2	1
M3, M4, M7, M8	3.25 / 2.1	1
M9	14 / 2.8	3
M10, M11	7 / 0.7	4
M12, M13	8.25 / 4.2	6
R1, R2	8.7 KΩ	-

For a comprehensive simulation of the OTA, different analysis techniques of Cadence SpectreRF tool was utilized. DC gain and bandwidth characteristics of the OTA are derived from AC analysis results in Figure 4.5. Noise characteristics are derived from the analysis in Figure 4.7. Slew rate and settling times are extracted from transient simulation results, such as in Figure 4.8. Expected input offset variations are extracted from the Monte Carlo simulation in Figure 4.9. CMRR and PSRR values are obtained from AC and XF (transfer function) analyses. Finally, power consumption is calculated by extracting the current consumption at DC operating point.

The full list of simulated performance parameters of the front-end OTA can also be seen in Table 4.3.
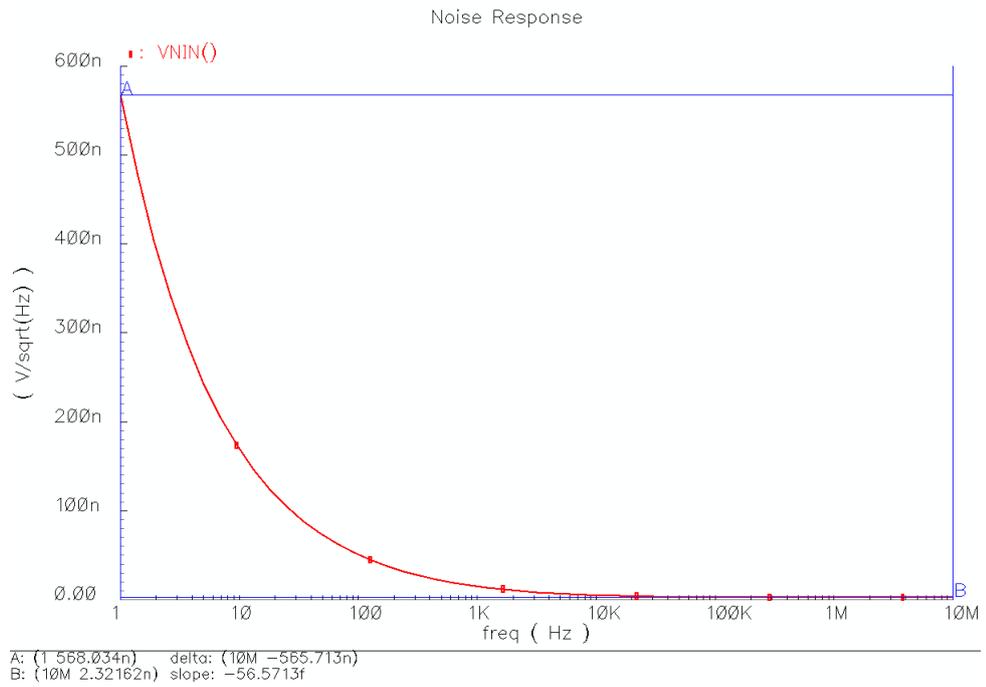
Figure 4.7: Noise analysis results of the designed OTA.
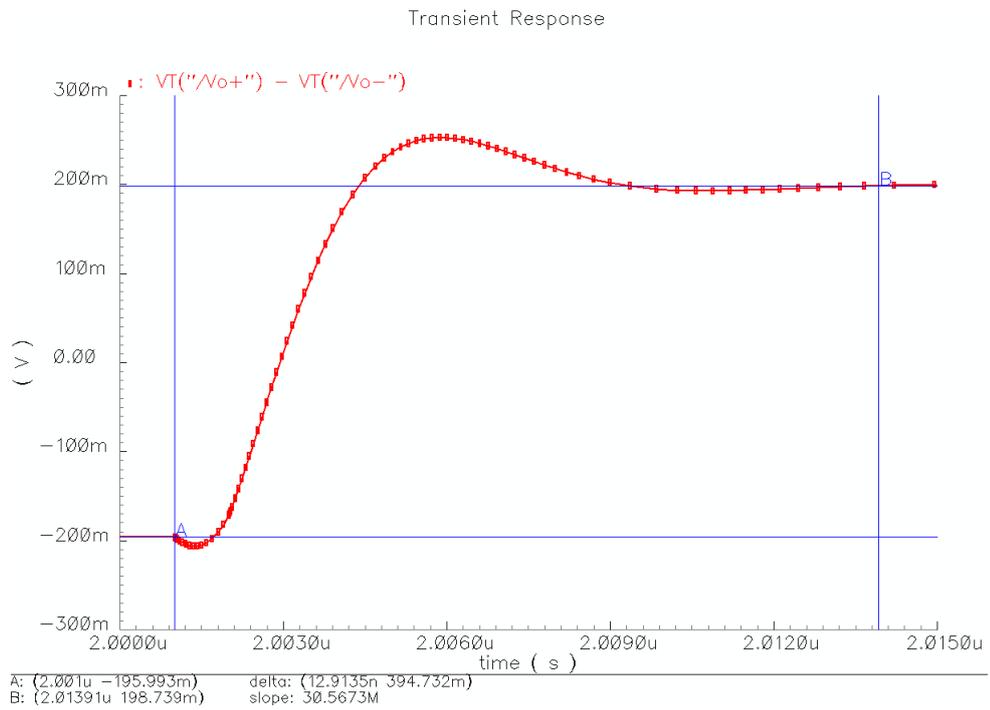
Figure 4.8: Settling of the OTA in unity-gain configuration and for 0.4V input pulse.

Table 4.3: Performance parameters of the OTA used in front-end sensor interface implementation.

Performance Parameter	Value
DC Gain	80 dB
Bandwidth (3 dB)	105.4 KHz
Gain Bandwidth Product (GBW) @ C_{LOAD} = 1 pF	1.05 GHz
Unity GBW @ C_{LOAD} = 1 pF	363 MHz
Phase Margin	57.2°
Slew Rate @ C_{LOAD} = 1 pF	694 V/µs
Settling Time @ 0.4V pulse input, Gain = 1	12.9 ns
Input Offset	± 2 mV
Input Offset, Temperature Sensitivity	28.7 nV/°C
1 / f Noise @ 1 Hz	568 nV/$\sqrt{\text{Hz}}$
White Noise Floor	2.32 nV/$\sqrt{\text{Hz}}$
Corner Frequency	4.74 kHz
CMRR	103 dB
PSRR	96 dB
Power Consumption	6.93 mW
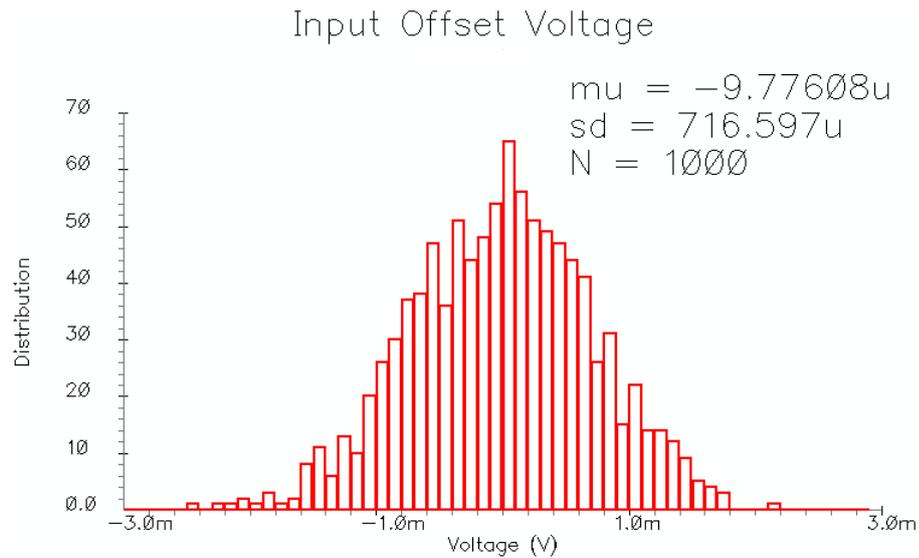
Figure 4.9: Input offset variation from Monte Carlo simulations with N = 1000.

4.1.2 Bandgap Voltage Reference and Low Dropout Voltage Regulators

In order to generate the necessary customized bias voltages to the designed folded cascode OTAs, a bias generator circuit is necessary. While there are several approaches to the bias generation problem, a bandgap voltage reference is an easy and efficient solution to the problem. Bandgap voltage references produce a voltage and temperature-independent output voltage that can be buffered to voltage regulators.

Since the complete readout circuitry uses three OTAs, with different sampling and integration periods; the load that the bandgap voltage reference is supposed to drive is very variable. Hence, a regulator that can drive the load OTAs without compromising stability and voltage and temperature independence is necessary. Figure 4.10 shows the low-dropout (LDO) regulator structure used widely in the literature and commercial regulators. The regulators are driven by VDD, so the drop-out voltage is non-critical. However, stability of the regular is very critical and it is necessary to provide regulator stability with in-chip built capacitances. Therefore, instead of standard implementations with a PMOS regulating transistor, an NMOS is chosen in order to guarantee stability. The extra V_{GS} drop-out voltage of the NMOS is not critical for this application.
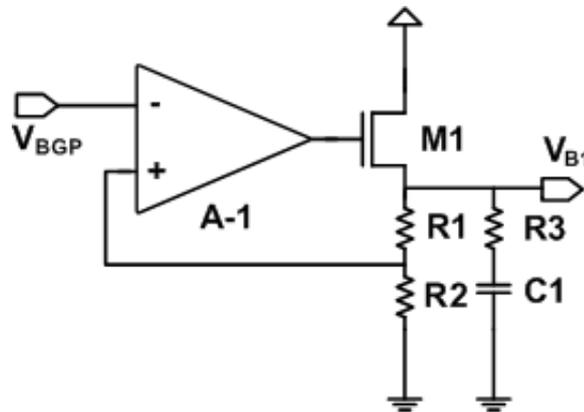
Figure 4.10: Stable LDO with NMOS regulator transistor.

The LDO in Figure 4.10 has a simple operation principle. High gain OPAMP A-1 aims to settle its non-inverting input into V_{BGP}, hence:

$$V_{B1} = \frac{R1}{R1 + R2} V_{BGP} \qquad\qquad (4.20)$$

Note that due to high closed loop feedback caused by the OPAMP gain A_{VO} and -gm_{M1}(R1+R2)//R3, Equation 4.20 holds true even for significant temperature and process parameter variations. Similarly, unless the power supply voltage shifts dramatically, variations in the power supply voltage are not transferred to the output. Illustrating this point, Figure 4.11 shows the power supply rejection of the low dropout regulator: 78dB rejection for low frequencies up to 100 Hz.

In order to cut back on the design time, X-FAB's propriety XH035 technology aopac08 OPAMPs were used in the implementation of LDO regulator circuits. Similarly, XFAB's abgpc07 bandgap voltage generator circuit was used to generate the reference voltage for the LDOs.
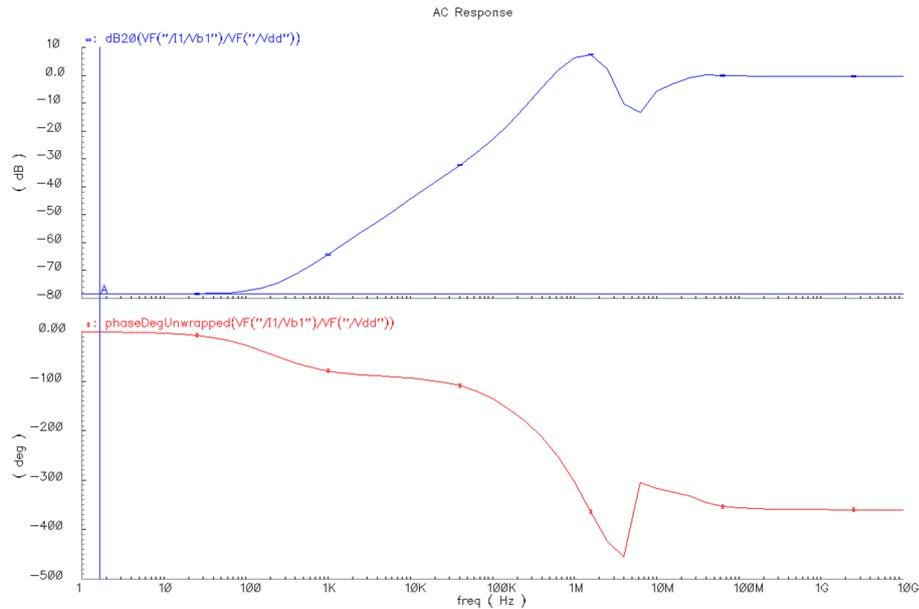
Figure 4.11: Power supply rejection ratio vs. frequency plot of the designed LDO.

For the low dropout regulator, stability is a real concern. Commercial regulators generally require at least several hundred nFs to be unconditionally stable. Such a big load cannot be possibly drawn on chip; therefore additional zeros were placed by the addition of R3 and C1 into the circuit and this way reasonable phase margins could be achieved. While this approach

does not guarantee unconditional stability, this is not needed since the loads that the regulator needs to drive are known (determined by the dimensions of the OTA). Hence, instead of unconditional stability; achieving conditional stability for pre-determined loads was the goal of design procedure.

In case the extra zero was not sufficient to drive the load, another zero was added as C3 capacitor in Figure 4.12, to help with the phase margin. The additional capacitor C3 bypassing R4 acts as a feed-forward path and increases the closed loop gain at high frequencies.
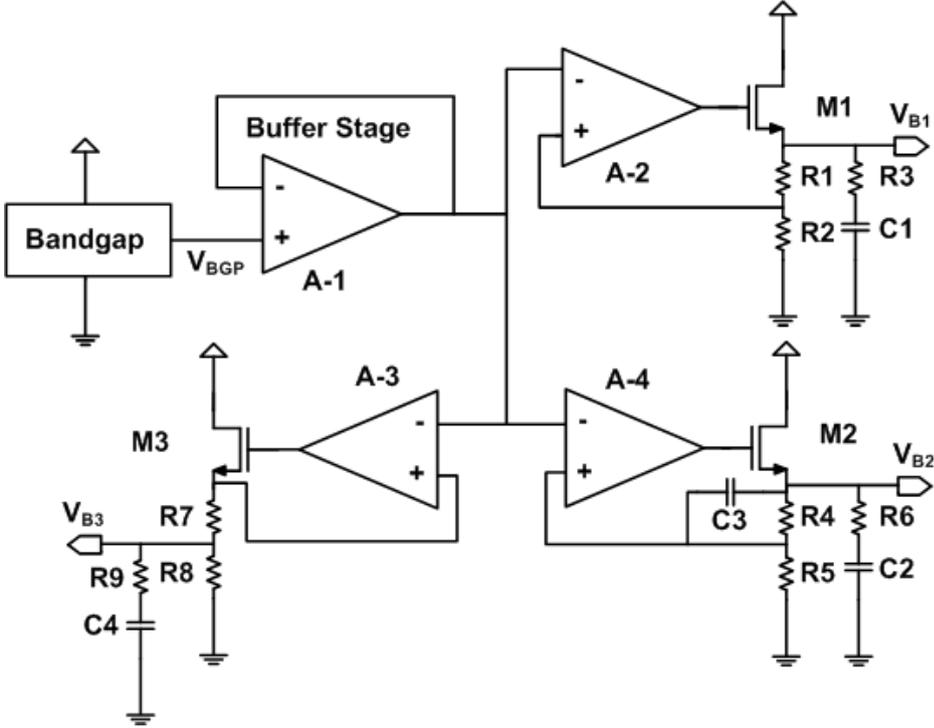
Figure 4.12: Overall voltage reference generator circuit with bandgap voltage reference circuit and three LDOs to regulate voltages for in-chip OTAs.

In order to demonstrate that the OTA does not suffer from stability problems, Figure 4.13 shows the transient response of the regulators to a sudden demand to one of the OTAs loading it. The regulator outputs spike up to 11 mV, but settle to normal voltage levels under 50ns. No residual tones or ringing can be observed.

Temperature sensitivity of the regulators is shown in Figure 4.14, where the maximum deviation of the regulated voltages can be seen to be 7 mV over 65 °C. The graphs of the final output voltages also closely follow graph of bandgap voltage reference's output. Hence, it can

be observed that the designed LDOs do not put a strain on the temperature immunity of the bandgap voltage reference circuit.

Table 4.4 also lists the final simulated performance parameters of the designed bandgap & LDO regulators.
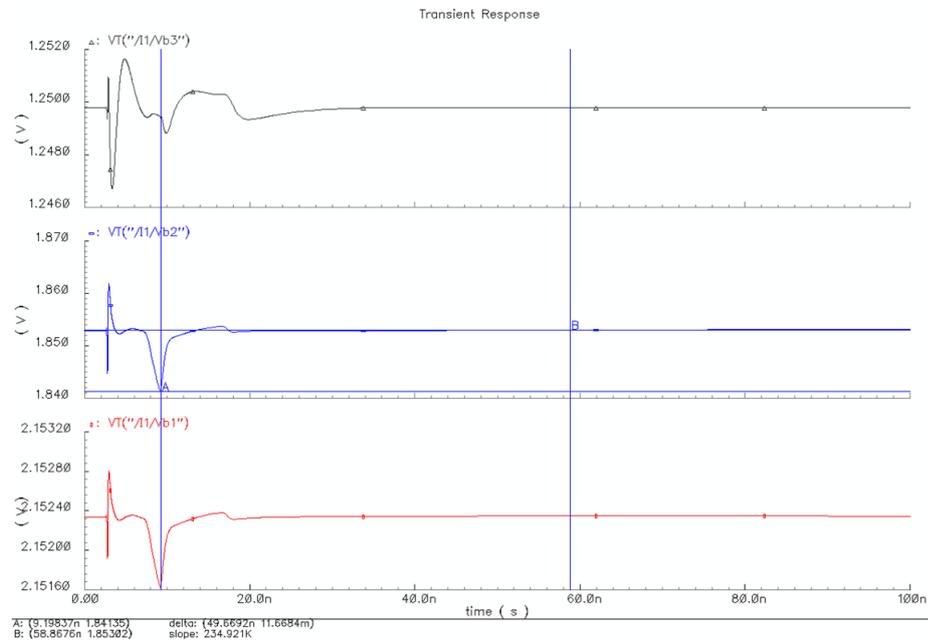
Figure 4.13: Transient response of the regulated bias voltages.

Table 4.4: Performance parameters of the reference voltage generators.

Performance Parameter	Value
Generated Bias Voltages **VB1, VB2, VB3**	2.15 V, 1.85 V, 1.25 V
Temperature Sensitivity from -40 to 90 °C	
VB1 (worst deviation)	11.18 mV
VB2 (worst deviation)	8.47 mV
VB3 (worst deviation)	6.74 mV
PSRR @ 100 Hz	78 dB
Power Consumption	2.72 mW
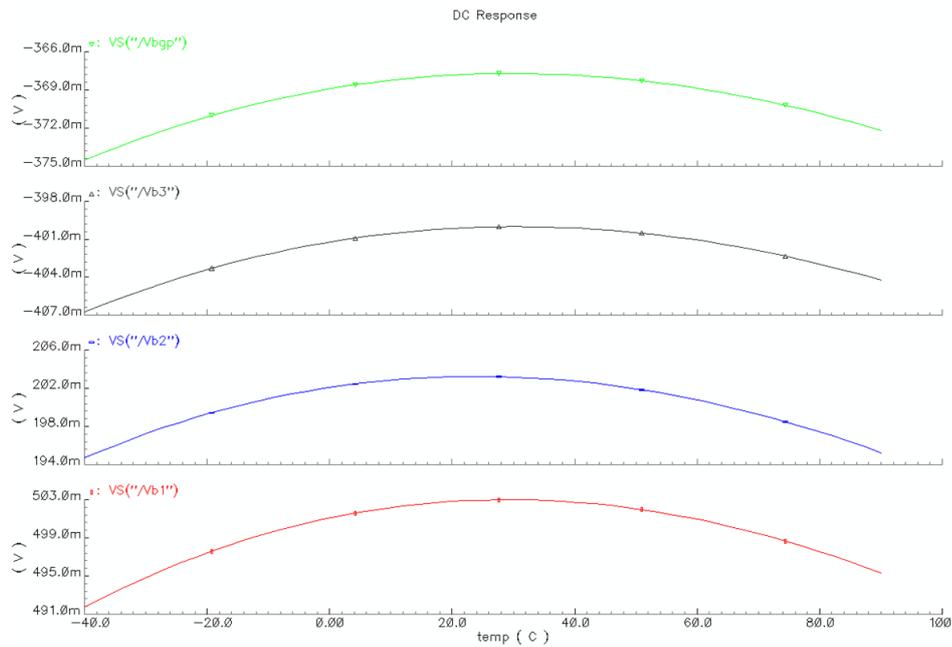
Figure 4.14: Temperature sensitivity of the regulated bias voltages, and the internal bandgap voltage.

4.1.3 Digital Multiphase Clock Generator

The capacitive fourth order circuitry is mainly switch-capacitor based and requires a multiphase clock generator to produce non-overlapping clock signals or sometimes deliberately overlapping complementary clock signals required to drive the CMOS switches in the circuit. In order to prevent parasitic charge injection, or de-synchronization of complementary clocks; all clocks including complementary clock signals driving CMOS switches are exclusively generated within and distributed from this block. No external inverters or other digital blocks are used near other analog, digital or mixed-signal CMOS switch blocks.

Complementary clock signals are carried next to each other to the rest of circuit in the layout, so that any possible glitches in other analog lines that cross these digital signals are canceled by the signal's complement.

In order to generate high precision clock signals with accurate delay times between them, a high frequency input reference clock is necessary. The multiphase clock generator circuit is designed to work with a 50 MHz 50% pulse width reference clock signal, however the circuit can also work with slower clocks albeit at the cost of circuit sampling time. Faster clock

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signals are not recommended, since they cause the outputs of analog blocks to be sampled before they can settle. Nevertheless, reference clocks up to 100 MHz are still okay; however at the cost of significant precision.

Clock generation is done completely by digital blocks, and since a reference clock is used external factors such as temperature or in-chip noise factors such as jitter are relatively insignificant for this block. However, the reference clock is required to be precise; thus a PLL is necessary to drive this readout circuit. Thankfully, most FPGAs today in the market have internal PLLs that can be integrated with the readout circuitry to achieve synchronization between the readout and the FPGA reading the digital output of the circuit.

Operation of the digital clock generator is simple. The circuit has three major states, which can be summarized as RESET, SENSE and FEEDBACK; with a state diagram illustrating the relation between the states in Figure 4.15.
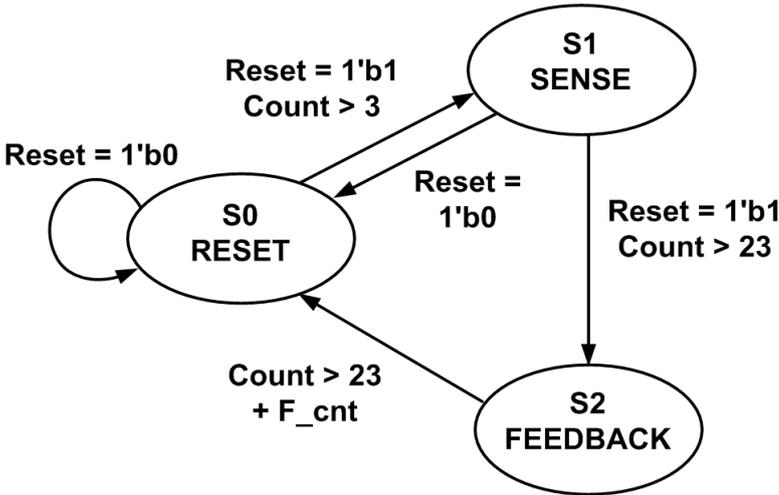
Figure 4.15: State transition diagram of the fully digital multiphase clock generator.

As can be seen from the Figure the digital circuit counts up the number of elapsed phases from the reset phase. In the sense phase, various multiphase clocks are generated for front-end capacitive sensing and noise shaping operations. At the end of sense phase, comparator samples the output of analog blocks and the new 1-bit digital information is stored on a D flip-flop.

Then, the relevant feedback information is given back to the MEMS sensor by a pulse during

the feedback phase; whose duration is determined by the selected reference clock frequency and an external setting, preset before operation by wire bond connections.

After the feedback cycle completes, the clock generator enters reset phase which lasts for 3 cycles. This reset phase is used to discharge all capacitors in the circuits, including the MEMS accelerometer capacitances that were charged by the feedback action, and puts all the analog blocks into buffering mode for the correlated double sampling circuitry.

It is also possible to force the whole circuit into reset phase by setting the external RESET pin of the readout to 0 or ground. In this case, the readout never leaves reset phase and all switches are forced to low (high for PMOS switches). This is a useful function to control the power-up sequence of the readout circuit. In order to make sure that digital logic blocks settle before the analog for circuit stability and a correct power-up sequence, the readout circuit should always start with the external input RESET = 0 which will then be turned into 1 after a sufficient amount of time has passed.

The digital clock generator circuitry also has four possible modes that determine the time duration of the feedback pulse applied during feedback phase. These are determined by the external digital inputs Pwid0, Pwid1 and Pwid2; which control the variable F_{CNT} in Figure 4.15. Table 4.5 lists the values that F_{CNT} obtains for various values of Pwid0, Pwid1 and Pwid2.

Table 4.5: Number of feedback cycles applied to the MEMS accelerometer, depending on external inputs.

Pwid0	Pwid1	Pwid2	Number of Feedback Cycles
0	0	0	0
0	0	1	7
0	1	0	23
0	1	1	39
1	0	0	55
1	0	1	71
1	1	0	87
1	1	1	103

Considering that the sense phase takes 23 cycles, and each cycle corresponds to one period of the reference clock signal, table 4.5 can be extended into table 4.6 which lists the number of

cycles and exact times for a complete readout sampling time and pulse feedback percentage. The reference clock is assumed to be 50 MHz (20 ns period); if a different clock period is used then the sampling time and frequency can be adjusted by the ratio of the applied clock period to 20 ns.

Table 4.6: Number of sense plus feedback cycles and sampling times for different configurations (50 MHz ref. clock)

Pwid0	Pwid1	Pwid2	Nr. of Feedback Cycles	Nr. of Total Cycles	Feedback %	Sampling Time	Sampling Frequency
0	**0**	**0**	**0**	**23**	**0 %**	**460 ns**	**2.17 MHz**
0	0	1	7	30	23 %	600 ns	1.67 MHz
0	**1**	**0**	**23**	**46**	**50 %**	**920 ns**	**1.08 MHz**
0	1	1	39	62	63 %	1.24 μs	806 kHz
1	0	0	55	78	70 %	1.56 μs	641 kHz
1	0	1	71	94	75 %	1.88 μs	532 kHz
1	1	0	87	110	79 %	2.20 μs	454 kHz
1	1	1	103	126	82 %	2.52 μs	396 kHz

In Table 4.6 the first configuration is obviously not suitable for closed loop operation, and for optimized operation it's recommended to have the feedback pulse as 50% and $P_{wid2}P_{wid1}P_{wid0}$ = 010. For such a configuration with reference clock at 50 MHz, the timing diagram of the clocks generated by the circuit can be seen in Figure 4.16.
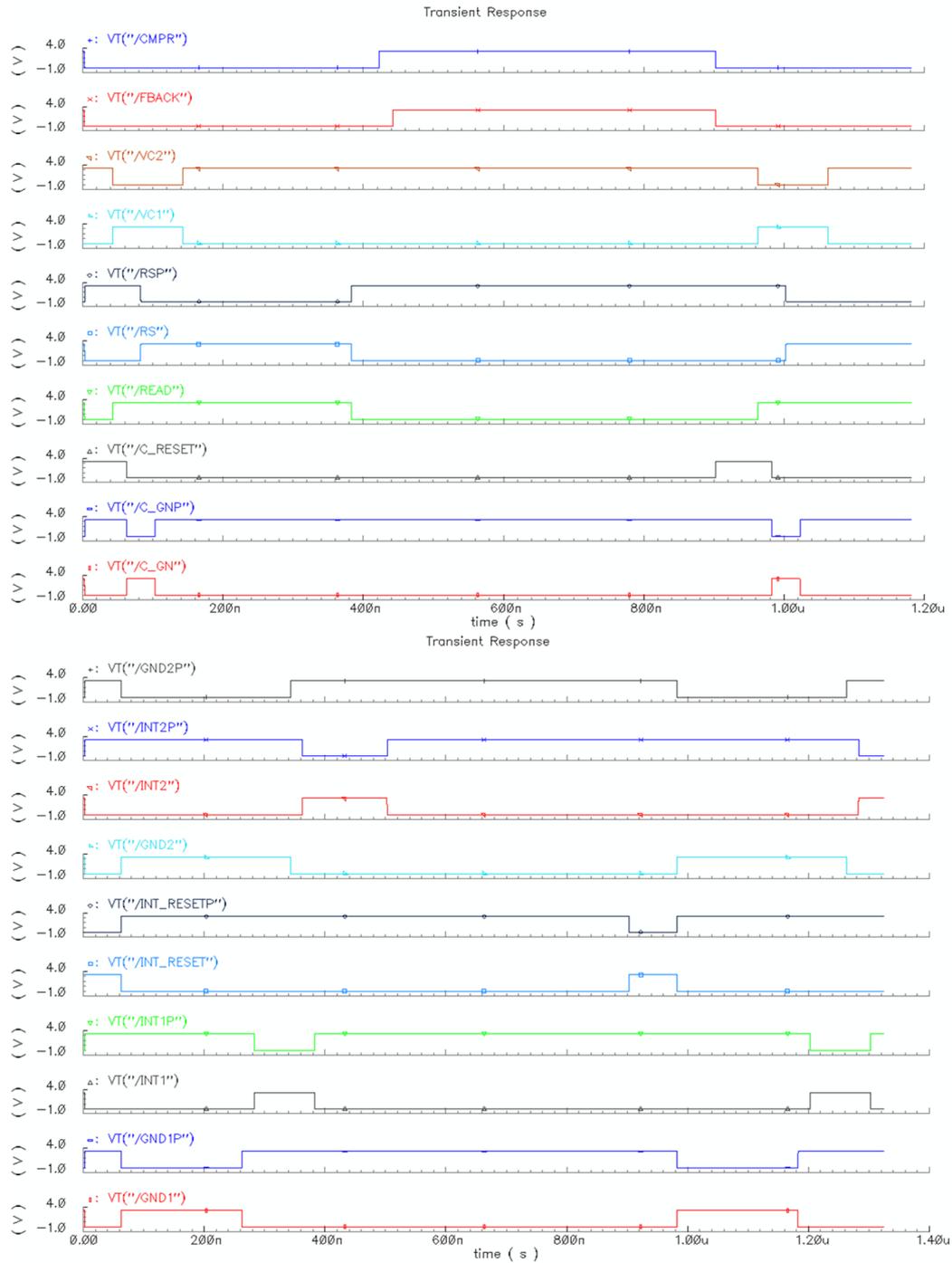
Figure 4.16: Transient simulation result showing multiphase clocks generated by the digital clock generator circuit with 50 MHz reference clock.

4.2 Back-End Noise Shaping and Digitization

Back-end readout contains the noise shaping transfer function made from discrete integrators, 1-bit quantizer and high voltage control blocks converting core 3.3V digital control signals into high-voltage feedback signals. High-voltage control and converter blocks are digital switch-type level shifters, and always function as digital buffers/level shifters from 3.3V up to 14V. These circuits are relatively simple and pose no challenge to design, so their design procedure will not be explained in detail.

In a single readout cycle, back-end readout blocks work sequentially starting from the noise shaping, moving on to quantizer and high voltage blocks. Back-end's function is finally completed when high voltage feedback signals are ready at the output.

The back-end outputs (high voltage signals) are then fed back into front-end feedback control switches in order to start the feedback phase. These switches are Φ_{FBACK}, Φ_{RST} and Φ_{READ} switches in Figure 4.2. Aside from the switches, feedback voltage levels V_{FBACK-} and V_{FBACK+} are also controlled by the back-end. By this way, front-end sense and back-end feedback mechanisms can use the same MEMS sensor electrodes, and hence these functions must be multiplexed in time domain. Synchronization of this multiplexing achieved by the multiphase clock generator.

4.2.1 Noise Shaping Discrete Integrators

As discussed in previous chapters, fourth order $\Sigma\Delta$ modulation at system level can be achieved in an accelerometer system with the addition of extra electronic integrators. The extra integrators, along with a properly designed electronic feedback mechanism is used to achieve internal modulation, and significantly increase the forward DC gain of the accelerometer; hence improving quantization noise shaping as well as eliminating any undesired effects such as dead-zone that are directly related with low DC gain in a $\Sigma\Delta$ modulated system.

The implementation of the cascaded integrators at circuit level is a challenging task; since the performance parameters of the integrators, especially those of the first stage, directly contribute to the final performance of the readout. Therefore, determination of critical circuit parameters are necessary in order to achieve a solid design.

First of all, electronic noise sources must be considered. Circuit noise from the first integrator stage contributes directly to the input-referred noise; while the noise of the subsequent integrator is suppressed at low frequencies by the previous one and is less critical.

Integrator nonlinearity is also critical at high input signal levels, where severe nonlinearity can degrade G_Q, the quantizer gain. This degradation results in poor SNR (Signal-to-Noise Ratio) levels at high acceleration inputs, and can be a limiting factor for the maximum operating range of the system. However, the nonlinearity requirement for low input signals is not critical, since G_Q is sufficiently high at low acceleration levels and the nonlinearity due to integrators is suppressed in base band.

DC gain of the integrators is also critical, and the integrators should provide enough DC gain to complement the low DC gain of the accelerometer. Since the intended fourth order $\Sigma\Delta$ loop is a discrete system the internal integrators are also required to be discrete; hence discrete integrator architectures with switch capacitor elements are preferred in implementation.

Different from a classical integrator, the transfer functions of the integrators used for noise shaping also require two or more differential inputs for correct operation. Thus, a fully differential integrator with multiples of inputs is necessary for correct implementation. Considering all these parameters, an optimal solution for the integrator implementation can be found with the discrete auto-zeroing sample and integrate circuitry in Figure 4.17.

The operation of the integrator in Figure 4.17 is simple, the circuit first samples the differential input voltages on capacitors C_{FB1} and C_{IN1} and then transfers the charge accumulated on these capacitances to C_{INT}. A fully differential OTA is used to achieve the charge transfer to the integration capacitors in integration phase. A more detailed analysis of the circuit is presented to understand some of the features and disadvantages of this integrator compared to classical blocks in the literature. Note that the actual switch clock phases can also be followed from the multiphase clock generator's output in Figure 4.16.

Assuming that the integrator starts in Φ_{SMP} phase, when the input voltages directly see the input capacitances C_{FB1} and C_{IN1}. Φ_{SMP} phase follows from Φ_{RST} phase, which is a short phase with the purpose of aiding the CMRR of the OTA and to correct the input common mode voltages of the OTA to the midpoint voltage, hence guaranteeing that the OTA starts in normal operation mode in Φ_{SMP} phase.
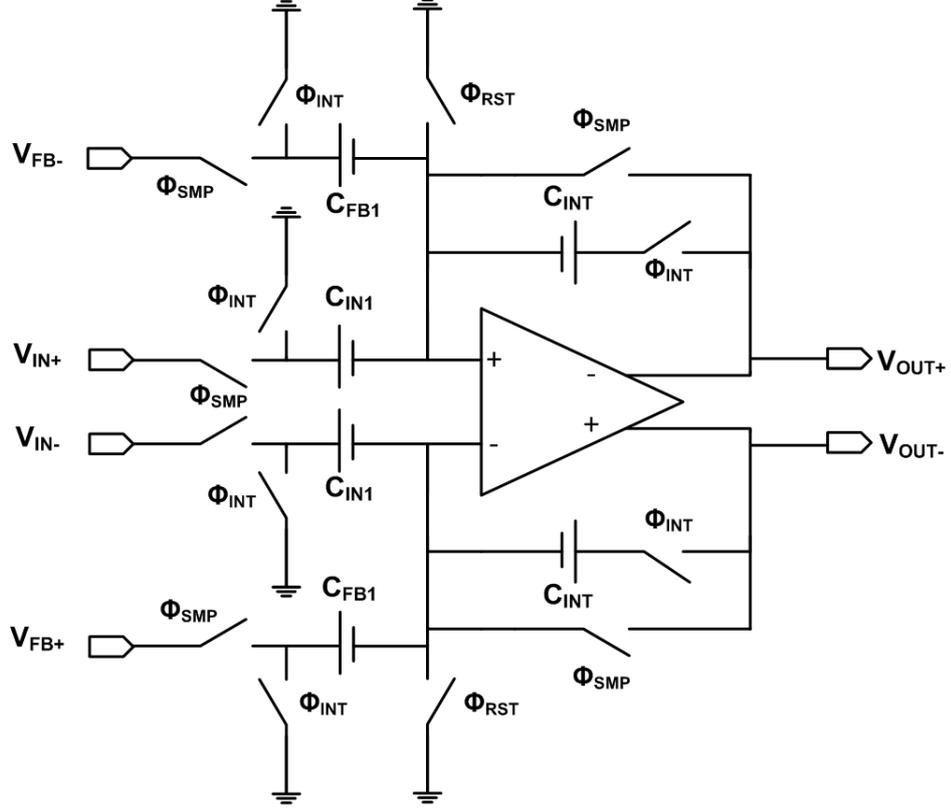
Figure 4.17: Discrete integrator block schematic with auto-zeroing offset cancellation.

In the Φ_{SMP} phase, Φ_{INT} is always low and hence the integration capacitances C_{INT} have floating nodes and previously stored charge on C_{INT} is kept. In this phase, OTA is also kept in buffer configuration where common mode and differential input offset values can be directly observed on the input nodes of the OTA. Since the inputs of the OTA must show the offset values, and bottom plate of the capacitors C_{FB1} and C_{IN1} must show the input voltage values, these capacitors are charged/discharged with a total charge of:

$$Q_{IN+} = C_{IN1}(V_{IN+} - V_{OCM} - V_{ODF+}) \qquad (4.21)$$

$$Q_{IN-} = C_{IN1}(V_{IN-} - V_{OCM} - V_{ODF-}) \qquad (4.22)$$

$$Q_{FB1+} = C_{FB1}(V_{FB+} - V_{OCM} - V_{ODF+}) \qquad (4.23)$$

$$Q_{FB1-} = C_{FB1}(V_{FB-} - V_{OCM} - V_{ODF-}) \qquad (4.24)$$

Where V_{OCM} is the common mode offset voltage and V_{ODF-} and V_{ODF+} are the differential offset voltages of the OTA.

After Φ_{SMP} phase, integration (Φ_{INT}) phase follows. In this phase, sampling switches are always off and the charge over the sampling capacitors C_{FB1} and C_{IN1} are summed at integration capacitances C_{INT}. There is no pathway for the charges accumulated on C_{FB1} and C_{IN1} to flow, so charge stored on these capacitors will stay constant. Assuming that the offset voltages do not change between the sampling and integration phases, the total charge remaining on the sampling capacitors at this stage are:

$$Q_{IN+} = C_{IN1}(-V_{OCM} - V_{ODF+}) \tag{4.25}$$

$$Q_{IN-} = C_{IN1}(-V_{OCM} - V_{ODF-}) \tag{4.26}$$

$$Q_{FB1+} = C_{FB1}(-V_{OCM} - V_{ODF+}) \tag{4.27}$$

$$Q_{FB1-} = C_{FB1}(-V_{OCM} - V_{ODF-}) \tag{4.28}$$

Rest of the charge is dumped on the integration capacitances by the OTA, hence:

$$Q_{INT+} = C_{IN1}V_{IN+} - C_{FB1}V_{FB-} + Q_{PREV+} \tag{4.29}$$

$$Q_{INT+} = C_{IN1}V_{IN-} - C_{FB1}V_{FB+} + Q_{PREV-} \tag{4.30}$$

The previous charge on the integration capacitors, denoted Q_{PREV}, was never discharged; hence the new charge is only added to the previous value. This accumulated charge on integration capacitances change the output voltage levels to:

$$V_{OUT+} = \frac{(C_{IN1}V_{IN+} - C_{FB1}V_{FB-}) + Q_{PREV+}}{C_{INT}} + V_{OCM} + V_{ODF+} \tag{4.31}$$

$$V_{OUT-} = \frac{(C_{IN1}V_{IN-} - C_{FB1}V_{FB+}) + Q_{PREV-}}{C_{INT}} + V_{OCM} + V_{ODF-} \tag{4.32}$$

It can be seen that for differential outputs, the common mode offset values of V_{OCM} cancel each other out, while the differential offset levels V_{ODF+} and V_{ODF-} are still present. This may seem to be a problem, as this design is not able to totally cancel out reflection of input offset values to the differential output. However, the important requirement is the cancellation of the input referred offset and 1/f noise, which are actually suppressed significantly.

In order to observe this suppression, let us consider the next cycle of the integrator. For this, the circuit goes back to Φ_{RST} and Φ_{SMP} phases. The total charge kept on the integrator, before integration step is:

$$Q_{INT+} = C_{IN1}V_{IN+} - C_{FB1}V_{FB-} + Q_{PREV+} \tag{4.33}$$

$$Q_{INT+} = C_{IN1}V_{IN-} - C_{FB1}V_{FB+} + Q_{PREV-} \tag{4.34}$$

We can safely assume that the integration is fast enough and neither V_{IN} nor V_{FB} values change during the integration cycle. Then, after the integration step, the total charge can be found as:

$$Q_{INT+} = 2(C_{IN1}V_{IN+} - C_{FB1}V_{FB-}) + Q_{PREV+} \qquad (4.35)$$

$$Q_{INT+} = 2(C_{IN1}V_{IN-} - C_{FB1}V_{FB+}) + Q_{PREV-} \qquad (4.36)$$

Repeating this integration cycle N times; the total charge accumulated on the integration capacitances are:

$$Q_{INT+} = \sum_{i=1}^{N} [C_{IN1}V_{IN+}(i) - C_{FB1}V_{FB-}] + Q_{PREV+} \qquad (4.37)$$

$$Q_{INT-} = \sum_{i=1}^{N} [C_{IN1}V_{IN-}(i) - C_{FB1}V_{FB+}] + Q_{PREV-} \qquad (4.38)$$

Assuming the input offset voltage has DC and 1/f noise components, and $f_S/N \gg f_C$, where f_S is the integrator sampling frequency and f_C is the 1/f noise corner frequency; we can safely assume that V_{OCM} and V_{ODF} values are constant throughout N integration cycles. Then, the final output voltages after N integration cycles are:

$$V_{INT+} = \sum_{i=1}^{N} \left[\frac{C_{IN1}V_{IN+}(i) - C_{FB1}V_{FB-}}{C_{INT}} \right] + \frac{Q_{PREV+}}{C_{INT}} + V_{OCM} + V_{ODF+} \qquad (4.39)$$

$$V_{INT-} = \sum_{i=1}^{N} \left[\frac{C_{IN1}V_{IN-}(i) - C_{FB1}V_{FB+}}{C_{INT}} \right] + \frac{Q_{PREV-}}{C_{INT}} + V_{OCM} + V_{ODF-} \qquad (4.40)$$

In order to derive the effect of input referred offset on the final output for N integration cycles, we need to derive the transfer function for the input-output offset relationship. The transfer function from the differential input ($V_{IN} = V_{IN+} - V_{IN-}$) to the differential output ($V_{OUT} = V_{OUT+} - V_{OUT-}$) can be derived as: (also note that $V_{FB} = V_{FB+} - V_{FB-}$ and $V_{ODF} = V_{ODF+} - V_{ODF-}$)

$$V_{OUT} = \sum_{i=1}^{N} \left[\frac{C_{IN1}V_{IN}(i) - C_{FB1}V_{FB}}{C_{INT}} \right] + \frac{Q_{PREV}}{C_{INT}} + V_{ODF} \qquad (4.41)$$

In order to compare the contribution of offset signal V_{ODF+} on the input signal V_{IN} we have to assume that V_{IN} and V_{ODF+} lay in the same frequency band, otherwise the comparison is meaningless. Thus, we can conclude that V_{IN} is also constant for N cycles, and the final expression simplifies down to:

$$V_{OUT} = N \frac{C_{IN1}V_{IN} - C_{FB1}V_{FB}}{C_{INT}} + \frac{Q_{PREV}}{C_{INT}} + V_{ODF} \qquad (4.42)$$

From this expression, it can be seen that the input voltage is amplified NC_{IN1}/C_{INT} times, while the differential offset voltage is not. Hence, the output referred offset voltage is suppressed NC_{IN1}/C_{INT} times when it is referred to the input. N is defined by the $f_S/N \gg f_C$ requirement; thus faster sampling and lower 1/f noise corner frequency results in better suppression. Faster sampling time is a critical factor depending on the slew rate and gain-bandwidth product of the OTA. If noise contribution outside the baseband is filtered, as is the case for the decimated $\Sigma\Delta$ modulator, then f_C can be substituted by f_B, the baseband frequency and the requirement changes to $f_S/N \gg f_B$.

In the implemented circuit, f_S = 1.08 MHz, C_{IN1}/C_{INT}= 0.25 and if a base bandwidth of 200 Hz is chosen, the achieved theoretical 1/f noise suppression is 1350, or 61 dB. This is a significant amount and for practical purposes serves as a complete offset and 1/f noise cancellation.

For better accuracy, Cadence SpectreRF PSS and PAC analyses have been conducted to simulate this suppression effect with real circuit elements. Figure 4.18 shows the periodic noise simulation results of the integrator. Due to offset cancellation 1/f noise is significantly suppressed. While the offset cancellation feature significantly suppresses the low frequency noise, thermal noise is not suppressed and hence dominates the input referred noise of the integrator.

From Equation 4.42 it is also possible to calculate the transfer function of the discrete integrator. Neglecting any offset components and assuming that the initial charge stored on the integrators is zero; it is possible to convert the input-output transfer function of the integrator into z-domain and obtain the relation:

$$V_{OUT} = \frac{C_{IN1}V_{IN}\,z}{C_{INT}(z-1)} - \frac{C_{FB1}V_{FB}\,z}{C_{INT}(z-1)} \tag{4.43}$$

Despite the 1/f noise cancellation feature, one disadvantage of this architecture is the nonlinearity of this integrator due to sensitivity to junction capacitance parasitics. An input-referred charge is stored on the parasitics of the input and feedback switches in the Φ_{SMP} phase, and during the Φ_{INT} phase this charge is stored on C_{IN1} and C_{FB1} capacitances. Due to charge conservation principle, this extra charge stored on C_{IN1} and C_{FB1} are transferred to C_{INT} and are summed up with the input-referred V_{IN} voltage. However, this effect is only significant when the input voltage is large enough. Fortunately, this only happens in a fourth order$\Sigma\Delta$

loop if the input acceleration level is very high. If G_Q, the quantizer gain is large enough, then the binary feedback is guaranteed to linearize this error. However for low G_Q values, this nonlinearity begins to degrade the SNR of the system.
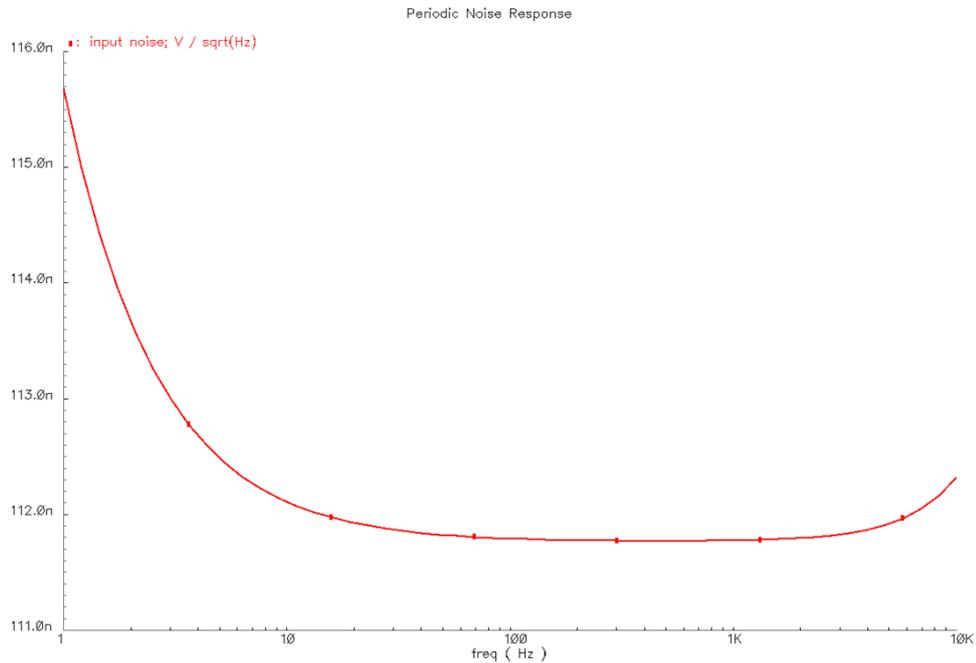
Figure 4.18: Periodic noise simulation result of the offset cancelling integrator in Cadence SpectreRF.

Another important parameter, the DC gain of the integrator can be inferred from the open loop analysis of the system to be equal to OTA open loop gain; barring any significant leakage in the capacitors. Hence, along with the thermal noise and gain-bandwidth requirements, a high DC gain is another requirement for the OTA. For the implementation; a low noise, high gain and high speed fully differential folded cascode OTA has been designed to satisfy all these requirements.

The recycling folded cascode OTA in Figure 4.3, is also used for these OTAs as well as front-end designs; however transistor dimensions have been modified. Since the integrator OTAs do not need drive as much capacitance as the front-end OTA, speed and slewing are less critical.

Also, since the auto-zeroing integrators inherently cancel out 1/f noise; hence the previously mentioned low frequency noise problem of the recycling folded cascode architecture is significantly suppressed. Hence, the recycling folded cascode architecture can be used to reduce the

power consumption of the circuit while preserving the thermal noise floor. Like its predecessor in the front-end interface, the integrator OTA also features NCFF compensation technique to boost the gain-bandwidth and phase margin specs.

Table 4.7 lists the modified transistor dimensions of the OTA used for integrator implementation, while Table 4.8 lists the simulated performance parameters of the OTA. Figure 4.19 shows the open loop characteristics of the OTA; with 82 dB DC gain, 103 MHz unity gain-bandwidth and 58° phase margin @ 1 pF load.

Table 4.7: Transistor dimensions of the OTA used in discrete integrator implementation.

Transistors	W/L (µm/µm)	M (Gate Number)
M1, M2	14 / 2.8	8
M3, M4, M5, M6	14 / 1.05	8
M7, M8	14 / 0.7	5
M9, M10	7 / 1.4	4
M11, M13	12 / 1.05	4
M12, M14	17 / 1.05	2
M15, M16	14 / 0.7	2
M17, M18	14 / 0.7	1
M19, M20	20 / 0.7	2
M21, M22	13 / 0.7	2

After a single stage integrator is complete, two stages can be cascaded to implement the desired noise shaping functions. Figure 4.20 shows the cascaded integrators forming the complete noise shaper block, along with the electronic feedback. In layout implementation, C_{FB} type capacitors selected from fully adjustable capacitor banks, allowing on-the-fly modification of electronic feedback gain coefficient. As mentioned before in Chapter 2, this approach gives great flexibility to the readout. Other capacitors are chosen by design to be:

$$C_{INT1,2} = 6pF \tag{4.44}$$

$$C_{IN1} = 1.5pF \tag{4.45}$$

$$C_{IN2} = 4pF \tag{4.46}$$

$$C_{FR} = 1.5pF \tag{4.47}$$

Table 4.8: Performance parameters of the OTA designed for discrete integrator implementation.

Performance Parameter	Value
DC Gain	82 dB
Bandwidth (3 dB)	10.2 KHz
Gain Bandwidth Product (GBW) @ C_{LOAD} = 1 pF	128.4 MHz
Unity GBW @ C_{LOAD} = 1 pF	103.5 MHz
Phase Margin	58.3°
Slew Rate @ C_{LOAD} = 1 pF	292 V/μs
Settling Time @ 0.4V pulse input, Gain = 1	21.4 ns
Input Offset	± 2 mV
1 / f Noise @ 1 Hz	3.8 μV/ $\sqrt{Hz}$
Integrator 1 / f Noise @ 1 Hz	116 nV/ $\sqrt{Hz}$
White Noise Floor	9.05 nV/ $\sqrt{Hz}$
Corner Frequency	33.45 kHz
CMRR	119 dB
PSRR	131 dB
Power Consumption	540 μW
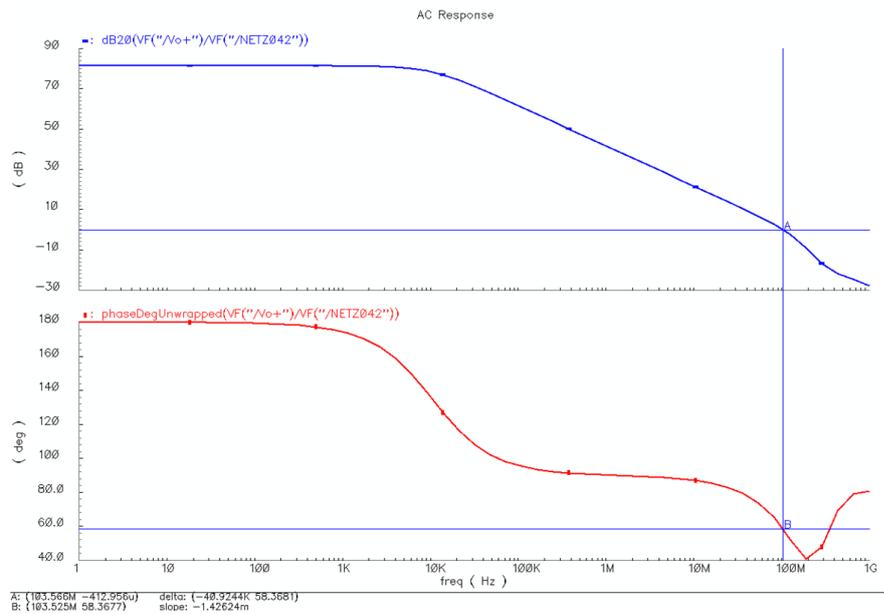
Figure 4.19: Open loop AC characteristics of the designed OTA for integrator implementation.
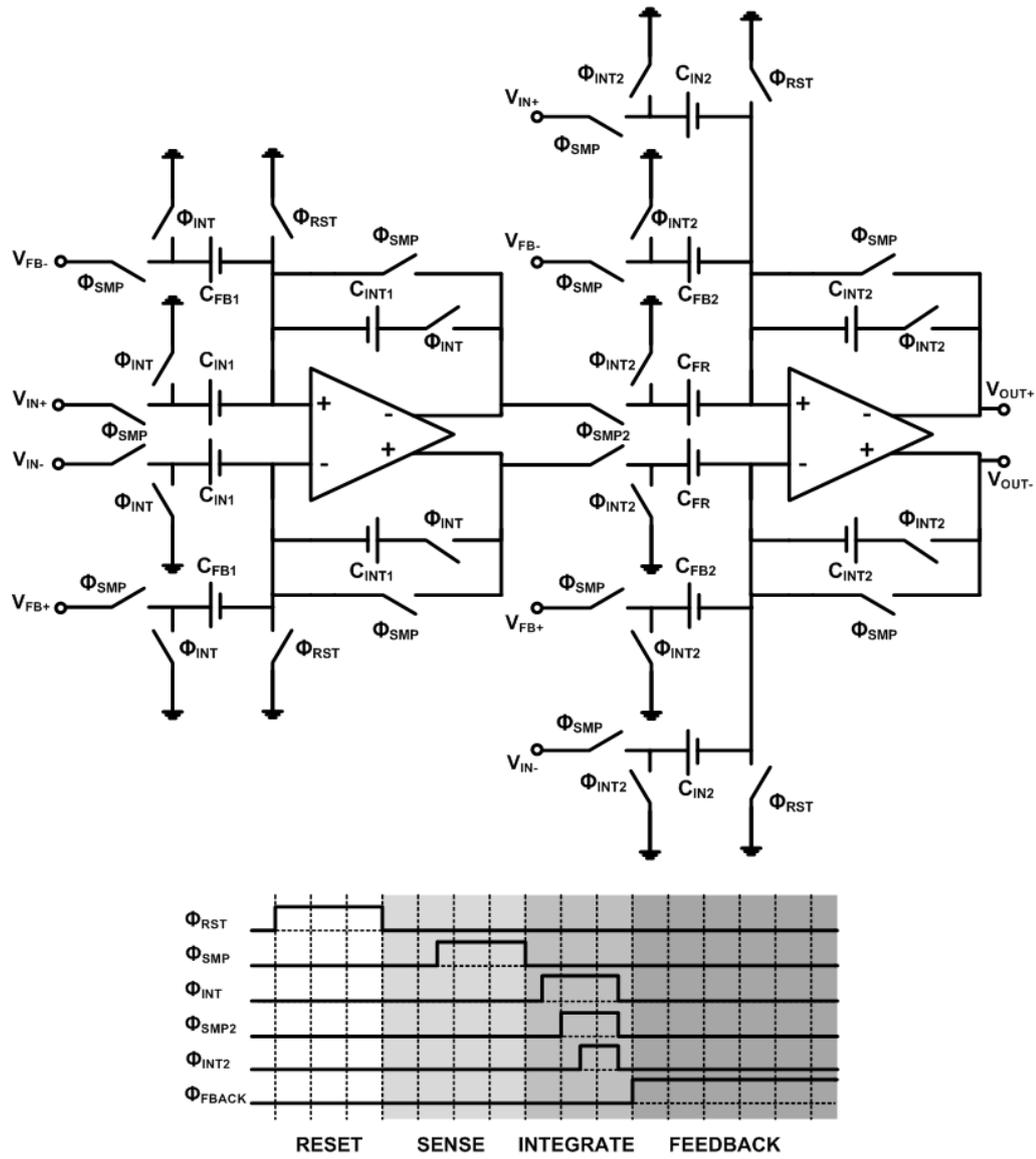
Figure 4.20: Schematic of the complete noise shaping discrete filter and electronic feedback, along with the associated timing diagram.

As a final note, it should be mentioned that in Figure 4.20, the discrete integrators sample their feedback and standard inputs sequentially, except for the feedforward input to the second integrator. In other terms, first and second integrators sample and store the front-end output and previous feedback values at the same time; while the second integrator waits for the first integrator to finish before calculating the final result.

4.2.2 Low Kickback Latched Dynamic Comparator

After the noise shaping block, a 1-bit quantizer is the final block in the forward path of the proposed fourth order accelerometer architecture. Due to the previous electronic and mechanical integrators, noise offset and nonlinearities of the comparator are significantly suppressed in the base band. Thus, design criteria of the comparator are relatively relaxed, especially if a dynamic comparator design is preferred in order to minimize power consumption.

Figure 4.21 shows the implemented latched dynamic comparator, with modifications to reduce kickback noise. The comparator samples and computes the comparison of analog input voltages V_{IN+} and V_{IN-} during rising clock edge and holds the computed output during CLK high phase, due to the double latch structure. During CLK low phase, outputs are cleared to low and the two latches are disconnected from each other.

Kickback noise, a problem with dynamic latched comparators, results when the dynamic comparator receives the rising clock edge and is busy calculating its outputs. During this stage, due to sharp rising edge of the clock signal, NMOS transistors are suddenly turned on and due to the parasitic CGS capacitance, inject some charge into their source nodes. The injected charge is generally not so small since the clock signal is driven hard by a digital buffer and has generally high frequency components during rising clock edge. Some of this injected charge is transferred from the transistor channels to the input gates nodes through CDS capacitances of input transistors.

Since the amount of charge that is discharged from the transistor channels depend on the instantaneous current flowing though the transistors during the clock edge, which directly depend on V_{IN+} and V_{IN-} ; the amount of charge that leaks into input gate nodes are dependent on the input analog voltage levels. If the previous stage driving the comparator has a low output resistance, then the charge transferred to the input gates can be discharged through the low impedance path easily. Otherwise, the accumulated charge is converted into voltage potential on the input parasitics of the comparator. Since this operation coincides with the calculation of the comparator output, an input-dependent offset called "kickback noise" results and directly influences the comparator output.

The amount of charge injected into the input depends on the input voltage levels, and to other factors such as instantaneous current flowing through the transistors during the comparison
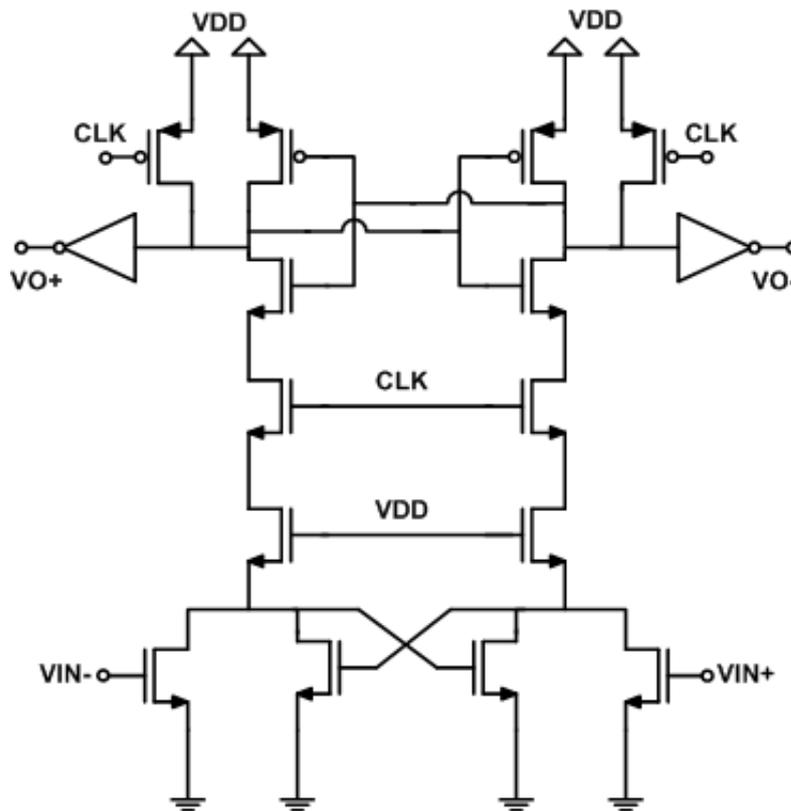
Figure 4.21: Schematic of the low kickback latched dynamic comparator.

event; making it is very hard to develop an accurate model of the kickback noise in comparators. However, accurate analysis results from Cadence Spectre transient and transient noise simulations show that, if no precautions are taken, kickback noise levels of $\pm$ 10 mV are possible. The fact that the comparator is driven by an OTA, a highly resistive component, makes the problem even worse.

The proposed structure in Figure 4.21 alleviates the kickback noise problem by preventing the charge injected from the clocked NMOS transistors to travel through the input transistors. This is achieved by significantly increasing the small signal resistance seen from the source of the NMOS transistors by the addition of a cascode pair. Since the charge injection is almost instantaneous and only contains high frequency components, the significantly increased small signal resistance prevents most of the injected charge to flow through the input transistors. Instead, the additional charge flows through the output transistor pairs and is safely discharged to AC ground via VDD. The parasitic C_{DS} capacitance of the cascode pair also

absorbs significant amount of the injected charge and discharges it through VDD again.

The additional cascode transistors however increase the transient delay of the comparator since the resistance seen from the output capacitors is increased. Despite the increase in delay, the response time of the comparator is still very low with approximately 5 ns.

Due to its latched structure, dynamic comparators have practically infinite DC gain spec; and the theoretical maximum quantizer gain G_Q is infinite. This is a definite advantage in $\Sigma\Delta$ modulators over static comparators.

Finally, this architecture has the disadvantage of having potentially significant offset due to capacitance and transistor mismatches. However, this offset is suppressed by the DC gain of electronic integrators (164 dB). Due to this significant suppression any amount of offset will not affect the output unless the operating point of the comparator is shifted near to power rails.

4.3 Complete Readout and Post Layout Verification

The designed readout circuitry was implemented in X-FAB's XH035 0.35 μm process with high-voltage option transistors. Die photo of the implemented readout can be seen in Figure 4.22.

Figures 4.23, 4.24, 4.25 and 4.26 show various results from post-layout simulations.

In Figure 4.23, 20 fF capacitance difference is read with 4 pF integration capacitance setting; registering 5 mV voltage output. This means that there is only 14 fF mismatch between the positive and negative terminals. The saturating signals before & after reading are due to significant amount of charge being injected by feedback signals into parasitic switch capacitances and the front-end registering this charge in its buffer mode.

For Figure 4.24, input capacitance was kept constant at 0.01 pF, however the output still appears to be pulse density modulated. This behavior is due to internal modulation from second order $\Sigma\Delta$ effect of the electronic feedback loop.
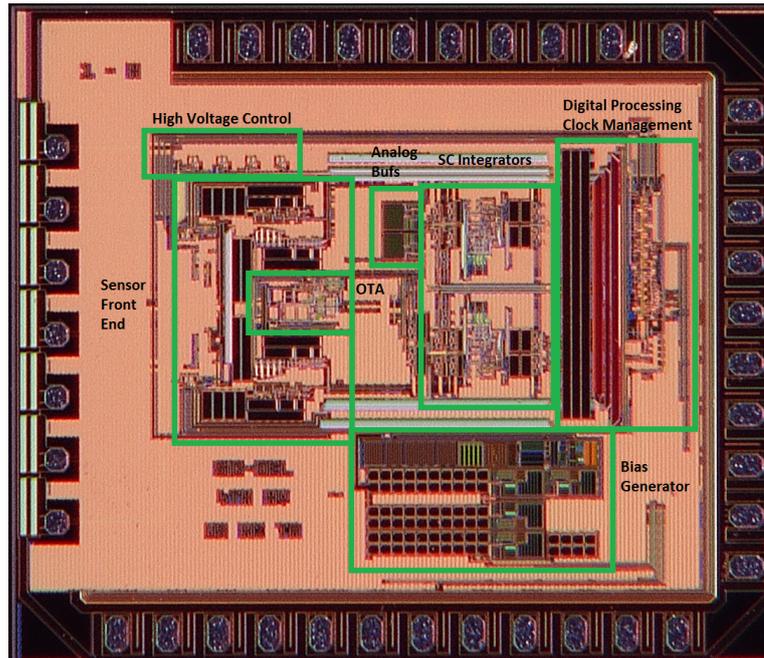
Figure 4.22: Die photo of the readout.
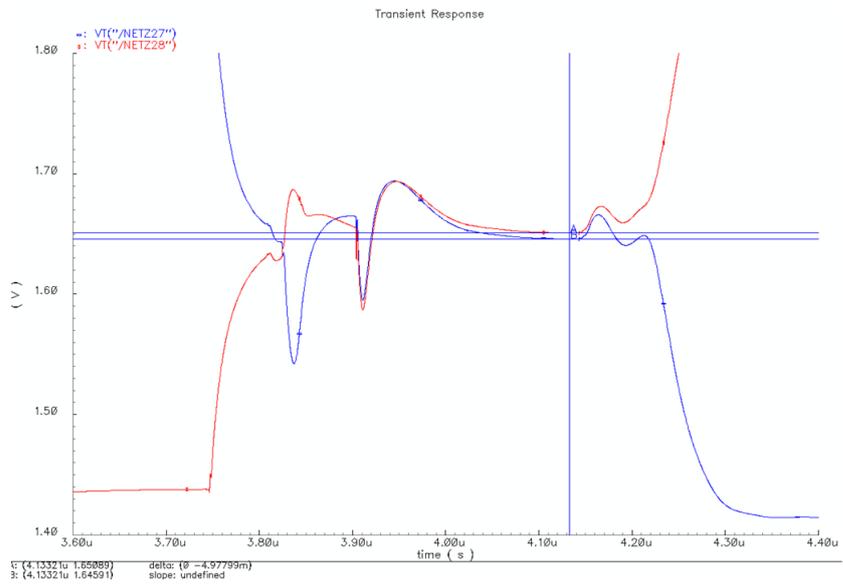
Figure 4.23: Pad level post-layout simulation result of analog outputs of the readout.
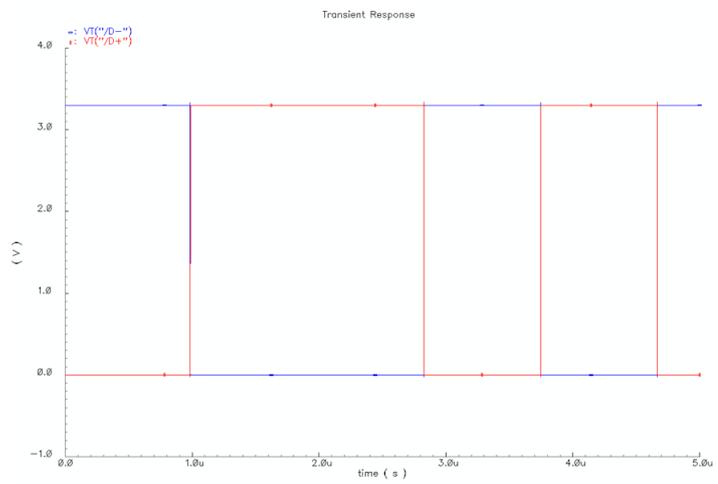
Figure 4.24: Pad level post-layout simulation result of digital outputs of the readout.

Figure 4.25 shows transient voltage levels at I/Os of the readout connected to MEMS sensor electrodes and proof mass. Modulated EM feedback action at 9V feedback voltage can be clearly seen, and feedback pulses appear to be very smooth despite significant load capacitances due to the MEMS sensor. Glitches are actually caused by changes in the other electrodes being reflected through MEMS sensor capacitances, and they can only be avoided by increasing rise/fall times of feedback pulses.

The final result shown in Figure 4.26 is very critical, since it discusses power or energy delivered to the accelerometer at each feedback cycle. Since EM feedback acceleration is directly proportional to V^2 (2.26), power delivered by the readout is directly referred to input as acceleration. Therefore any noise and/or glitch in this waveform would be registered as an acceleration source. By comparing Figure 4.26 with Figure 4.25, we see that the glitches seen in latter do not exist in former; and we can also confirm that there are no abnormalities on the power feedback signal.

Once the complete readout has been assembled and verified by simulations, total electronic noise due to OTA and kT/C sources can now be correctly simulated. This is achieved by running SpectreRF's PSS simulation in order to find the periodic steady state of the front-end C/V converter at $\Delta C = 0$ setting [28][29]. After a periodic steady state is found by Cadence SpectreRF, PNoise can be run in order to find the contribution of all voltage and jitter related noise sources to output voltage. Unfortunately, it is practically impossible to run PSS for the complete extracted layout; since doing so would require enormous amount of simulation time and memory. Therefore, digital parts of the readout were first simulated in transient mode, and their outputs were saved as piecewise-linear (PWL) function text documents. By introducing these documents to Spectre as PWL file (PWLF) sources, it is possible to run PSS+PNoise analyses with back annotated analog block schematics. PNoise simulation result in Figure 4.27 verifies the noise floor to be 125.5 nV/$\sqrt{Hz}$ with a corner frequency of 6.8 Hz. For this simulation, PSS *maxacfreq* parameter in spectreRF was selected to be 70 MHz and PNoise *maxsideband* parameter was chosen to be 50. This selection is expected to give a maximum noise error $<\pm$ 1 % [28].
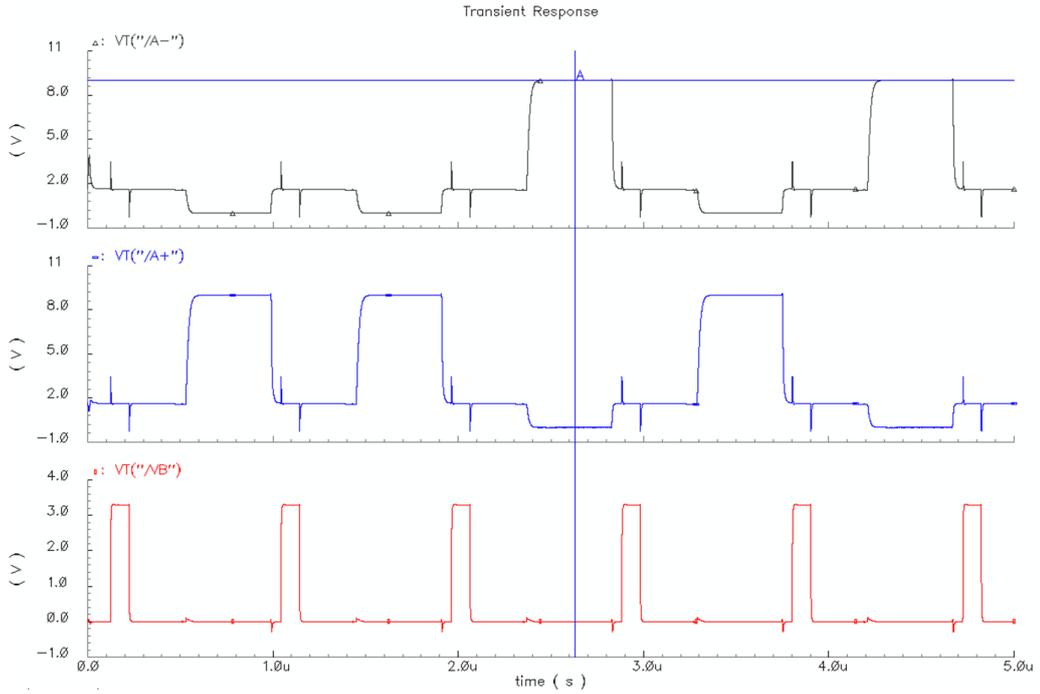
Figure 4.25: Pad level post-layout simulation result of sensor interface I/Os of the readout.
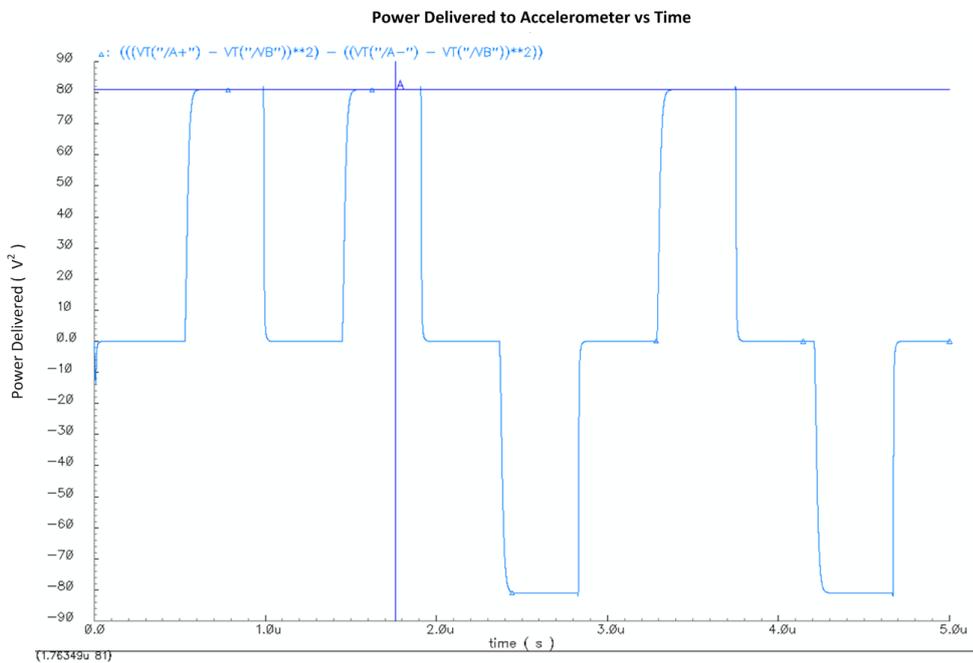
Figure 4.26: Pad level post-layout simulation result showing power delived to MEMS sensor.
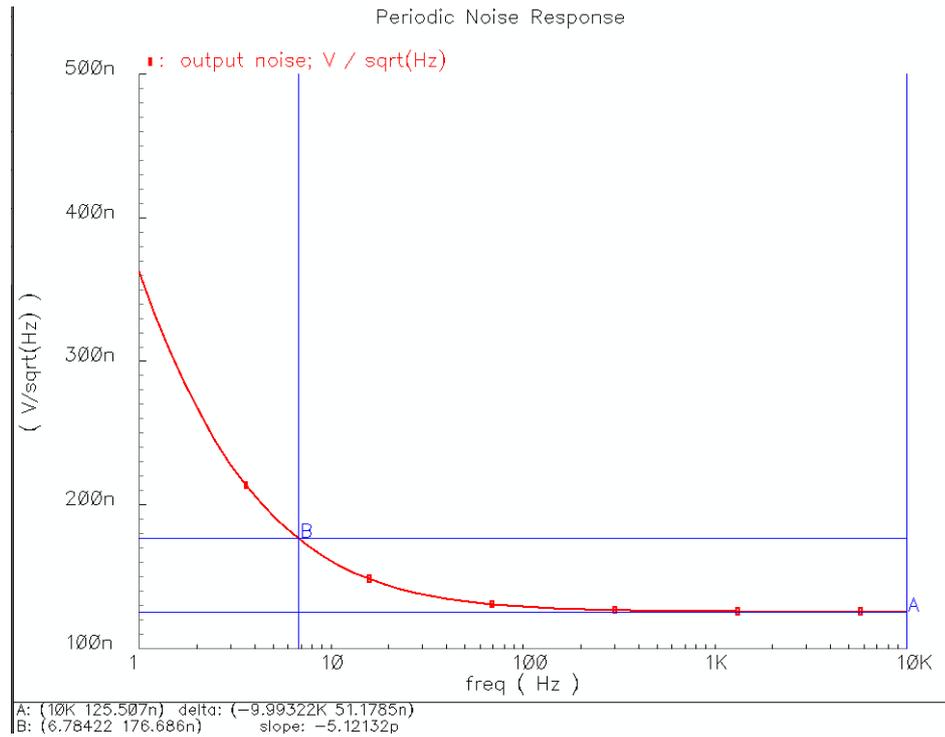
Figure 4.27: Simulated noise at the output of front-end C/V converter.

4.4 Summary of the Chapter

In this chapter, design simulation and implementation of the fourth order $\Sigma\Delta$ readout circuitry was discussed. Building upon the models introduced in Chapters 2 and 3, the focus of this chapter was on design and implementation of the aforementioned models in silicon. Several circuit-level novel designs such as the recycling folded cascode OTA with NCFF were also discussed in this chapter. Discussion on circuit elements started from the front-end C/V converter up to the latched quantizer, and every part of the $\Sigma\Delta$ ASIC was mentioned. Simulation techniques for periodic analyses of switched-capacitor circuit were also discussed. Finally, detailed simulation results from individual sub-circuits and complete readout are given in order to verify the operation of the readout ASIC.

With silicon implementation complete, the next chapter will focus on the results obtained from the fabricated chips.

CHAPTER 5

Implementation and Results

This chapter discusses the implementation of and test results obtained from the designed fourth order unconstrained $\Sigma\Delta$ accelerometer readout. In the first section, implementation of the readout with the MEMS accelerometer will be briefly explained. Then, the ASIC-computer interface established via an FPGA will be detailed. Along with the FPGA, the decimation filter used in processing the 1-bit digital raw data will be discussed. Finally, results form various noise, deadzone and stability tests will be discussed to conclude this chapter.

5.1 Test Setup Implementation of the Fourth Order $\Sigma\Delta$ Accelerometer Readout

Implementation and testing of the MEMS accelerometer readout system is done and by a layered approach. At the top level, a PC software communicates with the FPGA, which regulates the data coming from the readout circuitry mounted in a hybrid package on a PCB. At low level, interfaces between external electronics and readout, and between MEMS sensor and readout circuitry will be discussed. Figures 5.1 and 5.2 show the block diagrams of low and top level interfaces respectively.

At the lowest level, the readout circuitry is interfaced with the MEMS sensor on a hybrid package, as in section 5.2. Then, only the readout circuitry is interfaced with external electronics through this hybrid package. Even though the $\Sigma\Delta$ readout gives digital output, it still requires several well controlled voltage inputs in order to function properly. These are,

1. Power V_{DD} (3.3V) in order to supply power to analog blocks, such as bias generators and OPAMPs.

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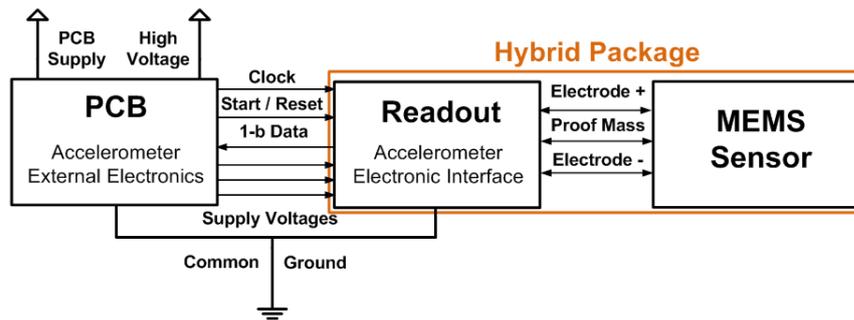
Figure 5.1: Low level data and voltage interface between PCB, Readout and MEMS sensor.

2. Digital V_{DD} (3.3V) in order to supply all digital blocks.

3. Signal V_{DD} (3.3V) in order to supply a clean reference potential as V_{FB} to discrete integrator feedback capacitors C_{FB}.

4. Mid-point potential V_{MID} to reset the charge on sensor and reference capacitors during front-end sense phase.

5. High voltage V_{HFB} to be given in 1-bit PDM fashion as feedback to MEMS sensor.

All of these voltages must be generated by external electronics in order to keep the readout operation stable. This is achieved by a PCB design consisting mainly of adjustable high performance low noise regulators, hybrid package and the package - FPGA interface.

At top level in Figure 5.2, the FPGA is the critical interface block. It receives the data from readout via the designed PCB, processes the 1-bit data by a decimation filter (see Section 5.3) and then returns the high resolution data to a PC software. The FPGA interface can be directly controlled by the written PC software, so in effect, the complete accelerometer system can be directly interfaced to a PC without any hassle.

Considering the size and ease of implementation of all these components, this is actually an easy setup for a high performance inertial sensor system. It is important to remember that the simplicity of this setup is due to our choice of using a $\Sigma\Delta$ modulated accelerometer system. Direct digital feedback immensely simplifies the external electronics and the hybrid package, and in turn system integration becomes managable.
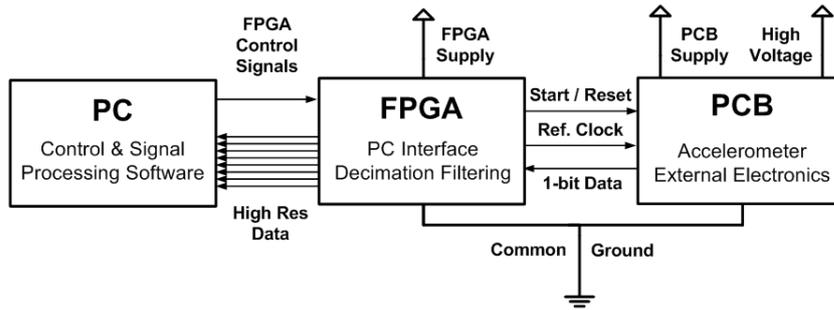
Figure 5.2: Top level control and data flow interface between a PC, FPGA and the PCB board.

5.2 Hybrid Packaging and Interface PCB

In order to integrate MEMS sensors and electronic interface circuits on a hybrid package, single mask gold-metalized glass substrates were used. Figure 5.3 shows the layout drawing of the single layer mask used for patterning the metal used in this process. As can be seen from the Figure, there are two "lumped" gold area on the substrates, where the MEMS sensor and readout will be placed. Around the readout circuitry, there are additional gold paths that extend from hybrid package pins. These paths will be connected to readout pads by wire bonding.

A printed circuit board is also necessary in order to house the interface the between the hybrid package (readout) and an FPGA. As mentioned before, this PCB is also used to generate all the necessary voltages in order to run the readout in stable, low noise operation. For this reason, three regulators are used to generate 3.3V, 1.65V and adjustable V_{HFB} ranging from 7 - 14 V. If the regulator output is grounded via a large capacitance; and separate wide bonds, PCB paths and hybrid package paths are used for power, signal and digital V_{DD}s, then a single regulator can be used to power all three of these sources. Cross-talk and noise interference from each of these signals can be avoided by using a star-connection between these signals. Linear technologies LT1762 regulators were chosen for implementation, since these regulators are fully adjustable between 1.22V and 18V, and have very low output noise levels. In addition, their noise can also be reduced by an adjustment to their bypass capacitors [32].

Figure 5.4 shows the layout of the designed PCB used in readout tests, and Figure 5.5 shows the photo of the PCB along with the hybrid packaged accelerometer system.

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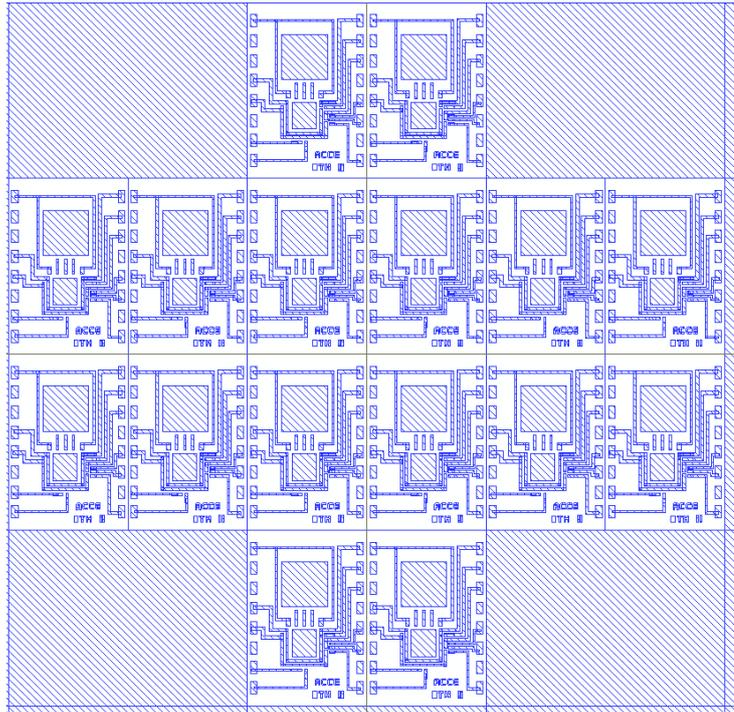
Figure 5.3: Layout drawing of masks used for fabrication of single layer metal glass substrates.
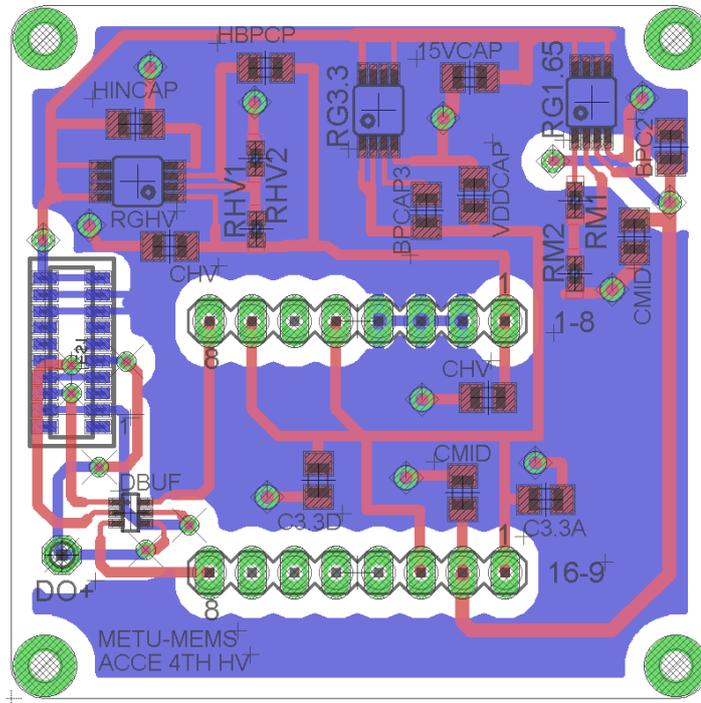
Figure 5.4: Layout drawing of the interface PCB holding various voltage regulators and readout-FPGA interface.

Figure 5.5: Photo of the test system with interface PCB and hybrid accelerometer package.

5.3 Decimation Filter Implementation

Up to this point in this thesis, we have only talked about the "Delta" part of $\Sigma\Delta$ modulation. Consistent with this preference, the ASIC readout used in the implementation has a Δ or pulse density modulated (PDM) 1-bit output. In order to convert this PDM 1-bit stream into a multi-bit digital value, a Σ (summation) demodulator should be used. This demodulator is also known as a decimation filter, since it has three jobs that it must fulfill:

1. High speed 1-bit stream should be summed in order to obtain a high resolution output signal.

2. Bandwidth of the output bit stream, normally f_S, must be reduced to the intended base-band f_B.

3. Noise outside the intended baseband f_B must be properly removed before it can fold into the baseband.

Since the oversampling ratio defined by f_S/f_B is large, summing the 1-bit information over large numbers of data results in a high resolution output. However, a direct summation and decimation method is not generally preferred because practical one-step decimation filters are generally insufficient to prevent the noise folding from higher frequencies [24].

Therefore, a three step decimation filter is generally preferred to achieve good noise suppression and reasonable resolution. Stepwise approach is generally useful for suppressing the signals at frequencies above the sampling frequency of each step and eliminate aliasing or folding effects as much as possible. Figure 5.6 shows the block diagram of such a decimation filter, with a high order sinc filter block, low pass filter and a first order accumulate and dump (sinc_1) block. The addition of low pass filter before the last block prevents aliasing and improves final noise performance.

Bandwidth and resolution of the final bit stream depends on filter orders and decimation levels, as well as the bandwidth of the low pass filter. Since accelerometer quantization noise bandwidth is limited, target decimation filter bandwidth was selected to be 250 Hz.

Using reference book [24], the first and last stage sinc filters are designed by the selection of target bandwidth. Sinc_1 filter at last stage is set to have a decimation level of 4, so the first
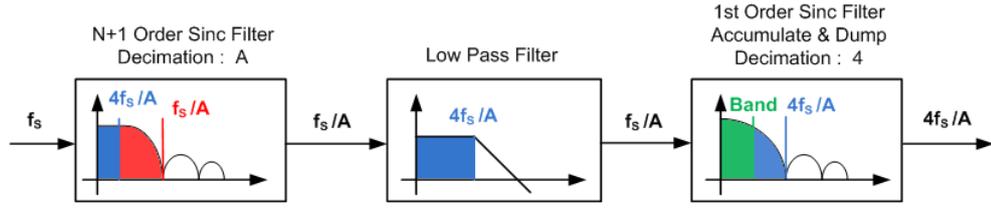
Figure 5.6: Block diagram of the implemented decimation filter, with colored regions showing the bands of interest.

sinc filter must have a decimation level of,

$$M_1 \quad = \quad \frac{f_S}{8 f_B} \tag{5.1}$$

Since 2^B type implementation of sinc filters are easier, we will choose $M^1 = 512$ and B = 9. It is also advised for the first sinc filter to have an order N+1, where N is the modulator order. Hence, a fifth order sinc filter with M = 512 will be chosen. This sinc filter will have the discrete transfer function

$$H_{SINC5}(z) \quad = \quad \frac{z^{2560} - 5\,z^{2048} + 10\,z^{1536} - 10\,z^{1024} + 5\,z^{512} - 1}{z^{2560} - 5\,z^{2559} + 10\,z^{2558} - 10\,z^{2557} + 5\,z^{2556} - z^{2555}} \tag{5.2}$$

Although the transfer function in Equation 5.2 seems complex, it is very easy to implement in Verilog HDL. In fact, this transfer function can be realized by a cascade of N+1 additive registers. Each register adds its input with the previous value M times, with the inputs being sampled when the previous filter has completed an addition cycle. After addition stages, differentiation register subtract their values from previous intputs. Again, a cascade of N+1 subtractive registers with M number of cycles, are used.

Resolution of such a sinc filter will be B*N+1, from the fact that each additive cycle will increase bit number B times, and N cascaded additive registers will increase resolution B*N times. Since modulator output is 1-bit, final resolution is B*N+1 bits. Thus, each additive and subtractive register must have B*N+1 bit size. Bandwidth of the filter will be reduced by M times, so for M=512 and input sampling frequency of 1.08 MHz filter output bandwidth will be 1.055 kHz.

If implementation is done so that B is an integer and 2^B = M, then registers are allowed to overflow naturally. This is much practical than preventing overflow, since the content of the

additive registers will grow exponentially.

A Verilog HDL code was written in order to implement this filter in an FPGA. This Verilog implementation can be seen in Appendix B, Section B.1.

Second stage low pass filter was designed in MATLAB with the help of MATLAB Filter Design and Analysis (FDA) toolbox. Figure 5.7 shows the designed low pass filter's frequency response characteristics. The filter is designed to remove aliasing effects over 250 Hz and has a cut-off at 300 Hz. Out of band suppression is 40 dB, and filter registers are 48-bits (calculated from B*N+1 plus two bits for sign interpretation and overflow). The last two extra bits can be removed at the output, since signed interpretation is needed only for internal calculations and overflow bit is only used for error checking.

As can be seen in Figure 5.7, the filter has been successfully quantized by MATLAB and implemented as a Verilog HDL block.
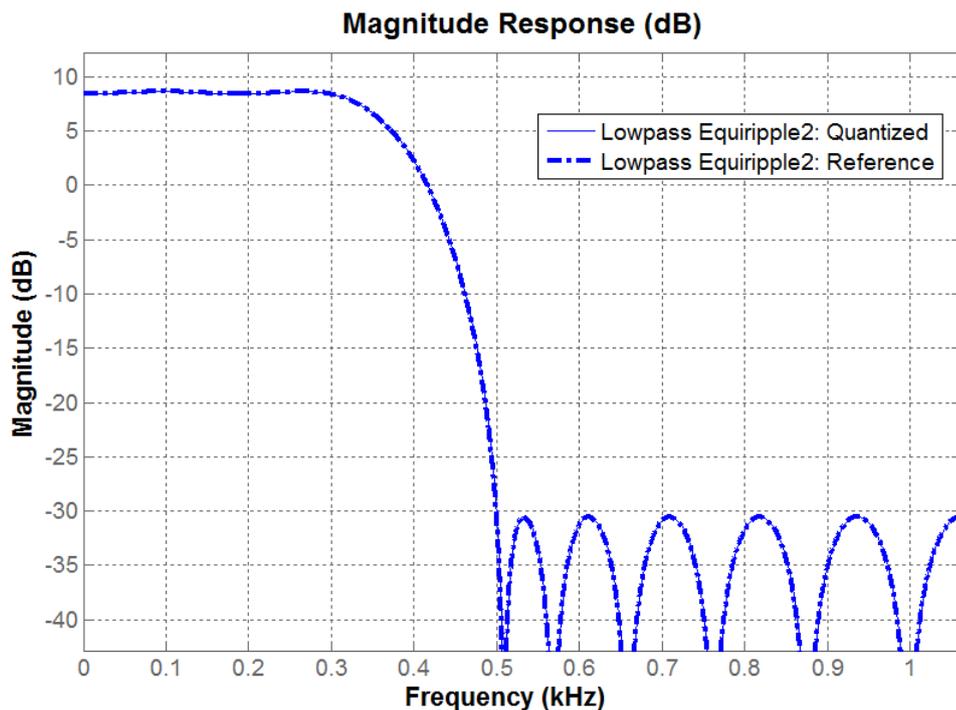
Figure 5.7: Frequency response of the designed low pass filter used for second stage decimation.

Last stage of the decimation filter is the accumulate and dump filter, which is actually a $sinc_1$ filter with a decimation order of 4. This filter sums its input 4 times, then stores the value in a

register and subtracts the values stored in this register four times from previous values. In the end, resolution is improved 4 times while bandwidth is reduced by 4. Verilog implementation of this filter can be seen in appendix B, Section B.2.

With these stages, final output will have a resolution of 48 bits while final decimation filter bandwidth is 263 Hz.

5.4 Test Results

Once the accelerometer and readout setup is complete, the accelerometer readout ASIC can be finally tested. For testing, MEMS accelerometers with the performance parameters specified in table 2.1 are used. These accelerometers were fabricated with dissolved epitaxial wafer process in May 2010 by Ilker E. Ocak as part of his PhD thesis works, and were wire bonded with the fourth order readouts in September and November 2010.

In total, four single-axis accelerometers were bonded with the designed readout ASICs. These are designated as DEWP#1-I 10, DEWP#1-F 5, DEWP#1-F 9 and DEWP#1-I 12. DEWP#1-I 10 and DEWP#1-F 5 were bonded and tested with an older generation of fourth order readouts in September. DEWP#1-F 9 and DEWP#1-I 12 were bonded in late November with a newer and improved generation of readout ASICs, so their results will be reported in more detail. Of particular significance is DEWP#1-I 12, which was used in detailed tests regarding optimization of filter coefficients to reduce noise and improve stability.

5.4.1 ± 1g Performance and Bias & Scale Factor Determination

Before doing any sophisticated tests, bias and scale factor of the implemented accelerometers must be tested. Since the data coming from FPGA is purely digital, a test must be done in order to match this data into actual acceleration values.

The decimated data at the output of the FPGA will almost certainly contain an "offset" or bias, since the 1-bit information coming from the readout is registered to be as either a 1 or 0. Therefore in ideal conditions, bias of the decimated data will be exactly half of decimation filter's full scale range. However due to electronic and mechanical offsets, fabrication mismatches and environmental variations, this bias point will differ between different ac-

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celerometers, and will even shift in time for a specific accelerometer. The term "bias drift" in Section 5.4.2 refers to this phenomenon when bias is observed to be drifting in time for a specific accelerometer. Bias point can be experimentally determined, and it corresponds to the mean output value under zero-g conditions. Bias drift is determined from Allan Variance analyses in Section 5.4.2.

Scale factor is a constant value that maps the deviation seen in digital output values into actual acceleration, so it defines how much change in sensor output actually corresponds to actual 1g deviation. For a linear system, scale factor is a constant value for any acceleration value that fits within the band of operation. Scale factor can be determined by measuring the output of the accelerometer in fixed 1-g condition (earth's gravity), and then subtracting this value from bias point. Then we know that the remaining value corresponds to 1g acceleration.

Once the bias point and scale factor parameters are determined, output of the accelerometer can be easily mapped into real acceleration values by the linear Equation 5.3. In the equation, G is the real acceleration value, S_F is the scale factor, X_{DEC} is the decimation filter output and B is the bias point.

$$G = S_F(X_{DEC} - B) \tag{5.3}$$

First of all, accelerometer I-10 was tested for linearity, bias point and scale factor between ± 1g on a rotating table. This test is not intended to be very accurate since linearity, scale factor and bias errors can be limited by the performance of the rotating table itself. Figures 5.8 and 5.9 show that this may be true, since no significant abnormalities between ± 1g range could be observed and any errors obtained from these data streams can easily be attributed to misalignment errors of the rotating table. Glitches observed in these Figures are caused by external vibrations applied accidentally by hand during testing. Figure 5.9 also shows that accelerometer linearity is actually very good, although a better setup is required in order to remove any potential errors caused by the rotating table.
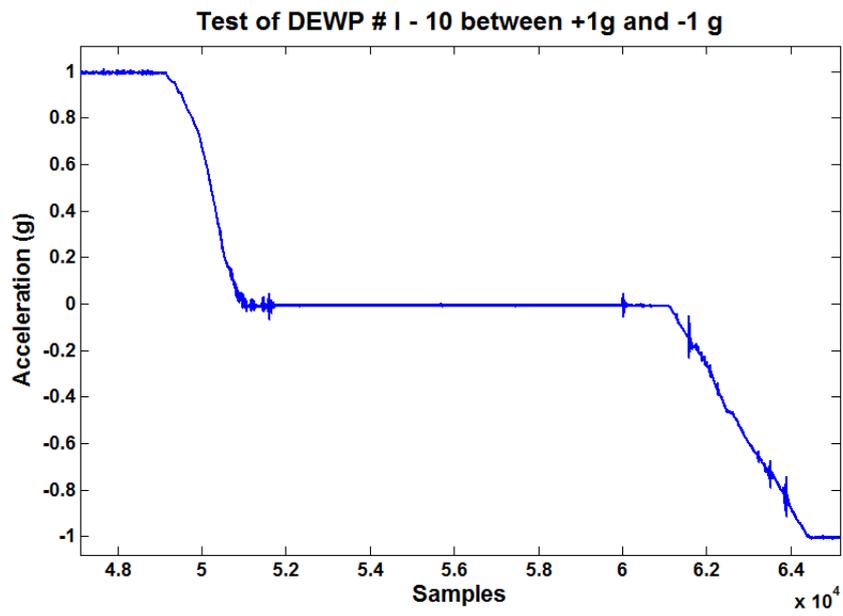
Figure 5.8: Test of DEWP# I-10 between ± 1g.
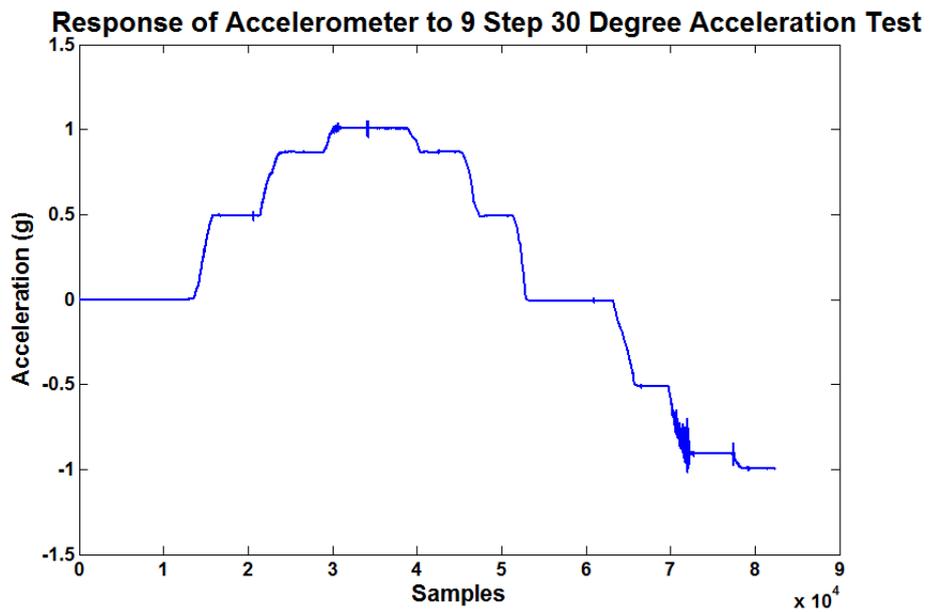
Figure 5.9: Accelerometer test on a rotating table, with each step corresponding to 30 °rotation.

5.4.2 Noise, Bias Drift and Dynamic Range

According to ANSI verified IEEE Standard 1293 - 1998 (R2008) [30], noise and bias drift tests of accelerometers should be evaluated by power spectral density (PSD) and Allan Variance graphs measured at zero-g conditions. In compliance with this standard, noise tests were done in a zero g environment, and the whole setup was fixed to a stationary table. However, it is also important to note that further improvements in noise setup can be made by using a setup fixed to a geologically stable bedrock in order to remove geological noise sources [17].

Furthermore, IEEE standard establishes that accelerometer noise results should be evaluated by a one-sided PSD from a discrete filtered output. Since a decimation filter is already present and aliasing effects are significantly suppressed due to the three stage filtering structure [24], further signal processing before noise evaluation is not necessary.

Figure 5.10 shows the PSD obtained from DEWP I-12 during a zero-g test. This result was obtained with V_{FB} = 8.2 V, readout sampling frequency of 1 MHz, C_{INT} = 15 pF and C_{FB} = 200 fF.
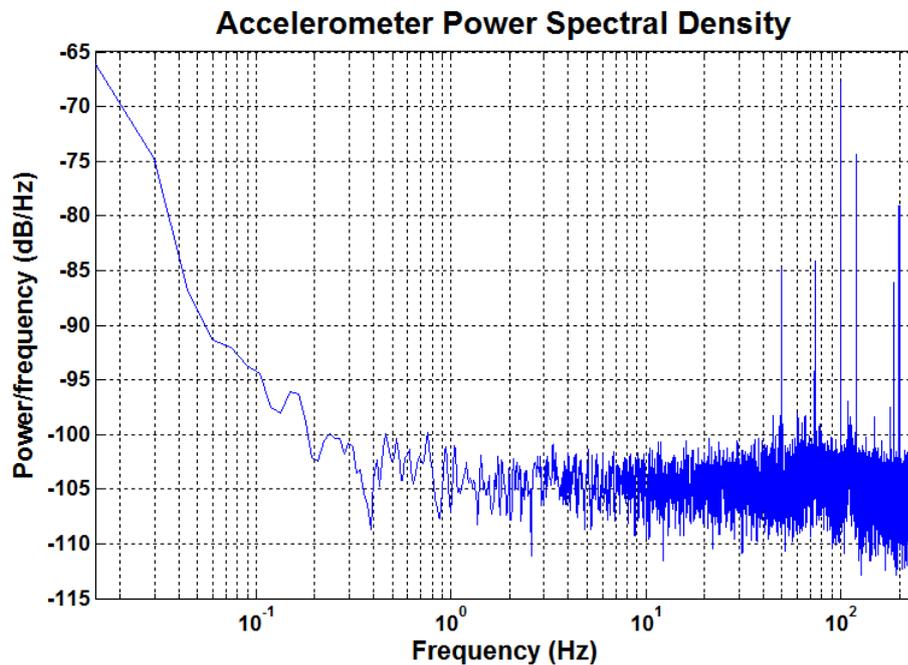
Figure 5.10: Noise PSD of DEWP I-12 for ± 18.5g range.

From Figure 5.10, white noise floor can be extracted to be -104.5 dBg/Hz or 5.95 μg/ $\sqrt{Hz}$.

An estimate for the white noise floor can also be made from peak to peak noise in transient data. Figure 5.11 shows the transient data obtained from DEWP I-12 for three minutes under zero-g conditions. Note that a 600 μg peak to peak noise can be clearly observed. Conversion from peak to peak noise into RMS noise can be done by the following formula:

$$N_{RMS} \quad = \quad \frac{1}{6} \frac{N_{PtP}}{\sqrt{F_B}} \tag{5.4}$$

Where N_{RMS} is the RMS noise in μg/$\sqrt{Hz}$, N_{PtP} is peak to peak noise in μg and F_B is signal bandwidth in terms of Hz. In Figure 5.11, readout sampling frequency was set to be 1 MHz, so final decimation filter bandwidth will be 244 Hz. Calculating the RMS noise for 600 μg noise over 244 Hz results in an estimated RMS white noise of 6.4 μg/$\sqrt{Hz}$. This result is in close accord with the results obtained from PSD analysis.
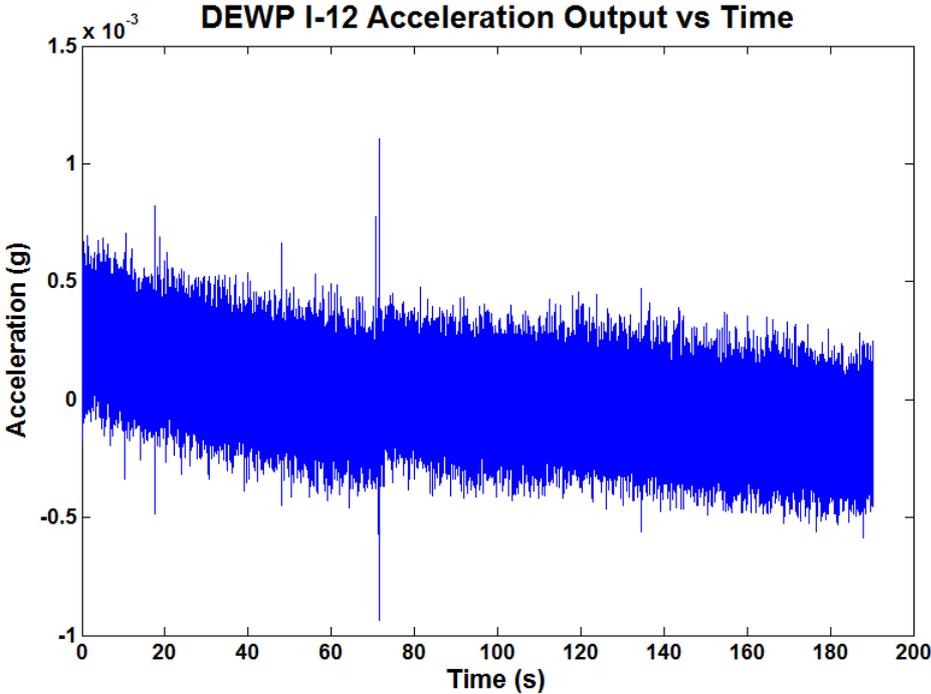
Figure 5.11: DEWP I-12 acceleration output for three minutes under zero-g condition.

Bias drift of the accelerometer should be measured by an Allan Variance analysis [30], so Allan Variance plot of accelerometer output was also generated. Figure 5.12 shows an example log-log Allan Variance plot for a gyroscope, with slopes caused by different noise sources marked on the plot. Note that bias drift can be easily extracted from the plot as the point where the log-log AlaVar plot slope is zero.

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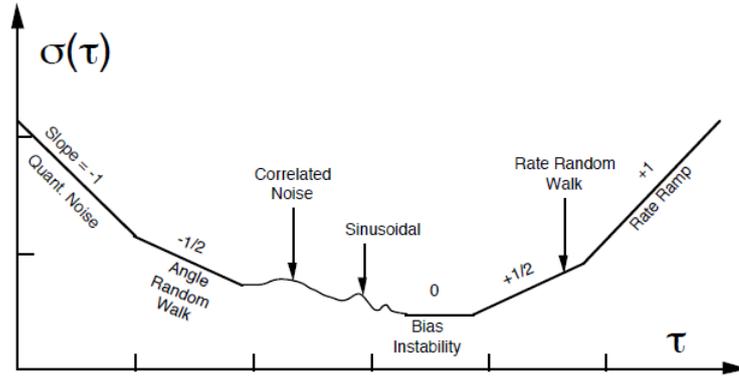
Figure 5.12: Example of an Allan Variance plot and noise sources corresponding to various slopes on the plot [31].

Of particular significance in Figure 5.12 is the angular random walk specification. For an accelerometer, the corresponding specification is called velocity random walk [30] and is closely related with the white noise floor of an accelerometer system. Following the derivation in IEEE Standard for Single-Axis Interferometric Fiber Optic Gyroscopes [31], it is possible to derive that the relationship between velocity random walk V_{RW} (m/s/ $\sqrt{s}$) and accelerometer white noise density N_{RMS} (m/s^2/ $\sqrt{Hz}$) is,

$$N_{RMS} = \sqrt{2}\, V_{RW} \tag{5.5}$$

This is caused by the fact that Allan Variance derivations in [31] use double sideband PSD as a reference. However up to this point in this work, we have only considered single sideband PSD analysis of noise sources. Therefore, converting from double sideband noise information obtained from the Allan Variance plot into single sideband PSD requires the noise density to be multiplied by a factor of 2 [30]. Since all electronic and mechanical noise sources are defined for a single sideband interpretation, this is the best approach to extract white noise data from Allan Variance plots. Therefore, Allan Variance can also be used to find the velocity random walk in m/s/ $\sqrt{s}$ or g/ $\sqrt{Hz}$ units and then this information can be multiplied by $\sqrt{2}$ to obtain the accelerometer's white noise.

Figure 5.13 shows the Allan Variance plot DEWP I-12's output under zero-g conditions. From the plot, 6.4 µg bias drift and 4.5 µm/s/ $\sqrt{s}$ (equivalent to µg/ $\sqrt{Hz}$) velocity random walk can be observed. Multiplying the observed velocity random walk with $\sqrt{2}$, we obtain an expected noise floor of 6.3 µg/ $\sqrt{Hz}$ for the accelerometer.

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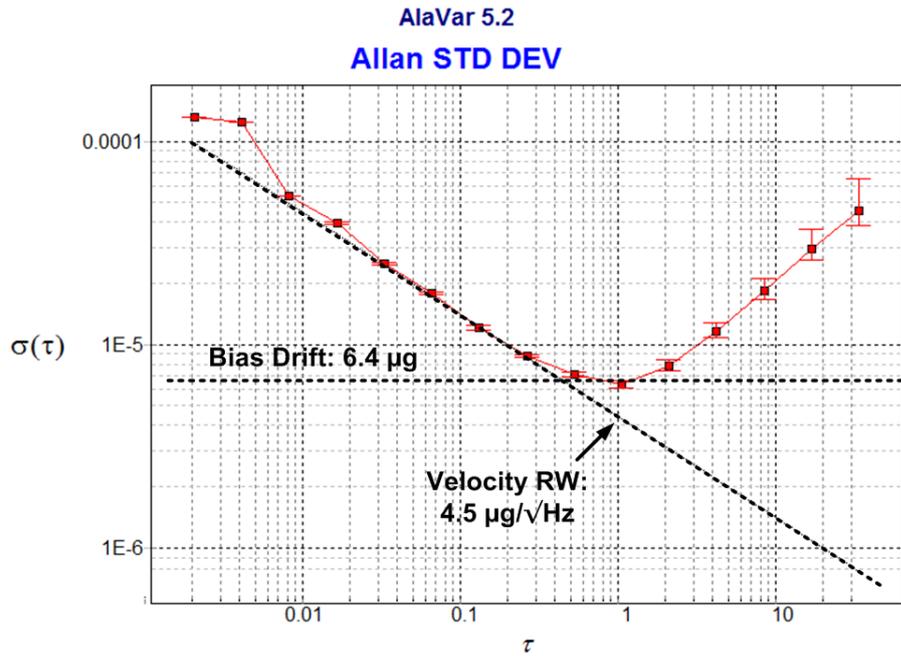
Figure 5.13: Allan Variance plot $\sigma(\tau)/\tau$ of DEWP I-12 output under zero-g condition.

By comparing all three white noise determination methods, we can conclude that every method checks out the obtained 5.95 μg/ $\sqrt{Hz}$ value. Although there are variations on the exact noise number by a factor of approximately % 10, we will take the PSD noise as the final result due to its significance in the IEEE standard for accelerometers [30]. Peak to peak and Allan Variance noise derivation methods are valuable methods that can be used to verify the PSD noise data.

As a summary, we can conclude that the accelerometer system using the designed fourth order readout ASIC was able to achieve a noise floor of 5.95 μg/ $\sqrt{Hz}$, and a bias drift of 6.4 μg. The accelerometer system achieves these specifications with an estimated full scale range of ± 18.5 g, and hence dynamic range of the sensor is 129.8 dB for this configuration.

Sensor noise and dynamic range parameters are variable according to readout parameters, especially on C_{INT}, C_{FB} and V_{FB}. These parameters also define loop stability, so as explained in Chapter 3 trade-off between noise and stability is inevitable. A similar trade-off also exists between noise and full scale range. Since these relationships are complex and not inherently linear due to multiple independent noise sources having different variables gains, minimum resolution specification does not necessarily net the best dynamic range performance. There-

fore, the best dynamic range performance of the accelerometer system should also be tested and verified.

Figures 5.14 and 5.15 show the noise performance of DEWP I-12 for 9.3V feedback voltage and ± 24.5g full scale range. PSD plot shows a minimum noise floor of -103.9 dB/Hz or 6.38 μg/$\sqrt{\text{Hz}}$, while Allan Variance plot shows a velocity random walk of 4.65 μg/$\sqrt{\text{Hz}}$ corresponding to a noise density of 6.57 μg/$\sqrt{\text{Hz}}$. Again, noise values obtained from PSD and Allan Variance are close to each other. Assuming PSD noise is more accurate, the dynamic range of this configuration is 131.7 dB, larger than 129.8 dB obtained for lowest noise specification.
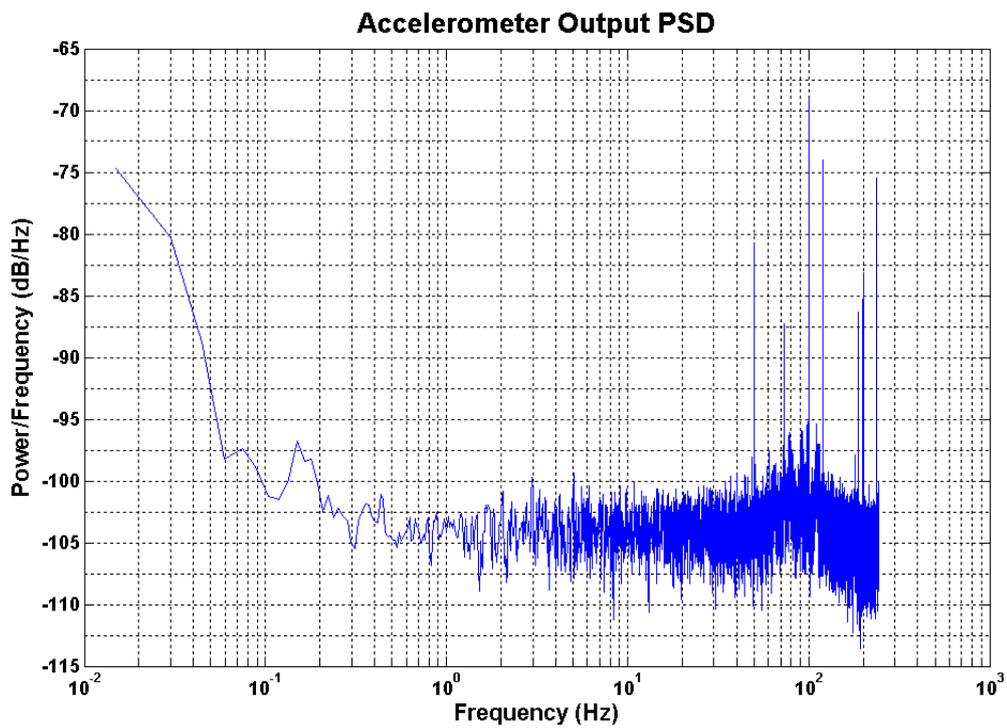
Figure 5.14: Noise PSD of DEWP I-12 for ± 24.5g range.
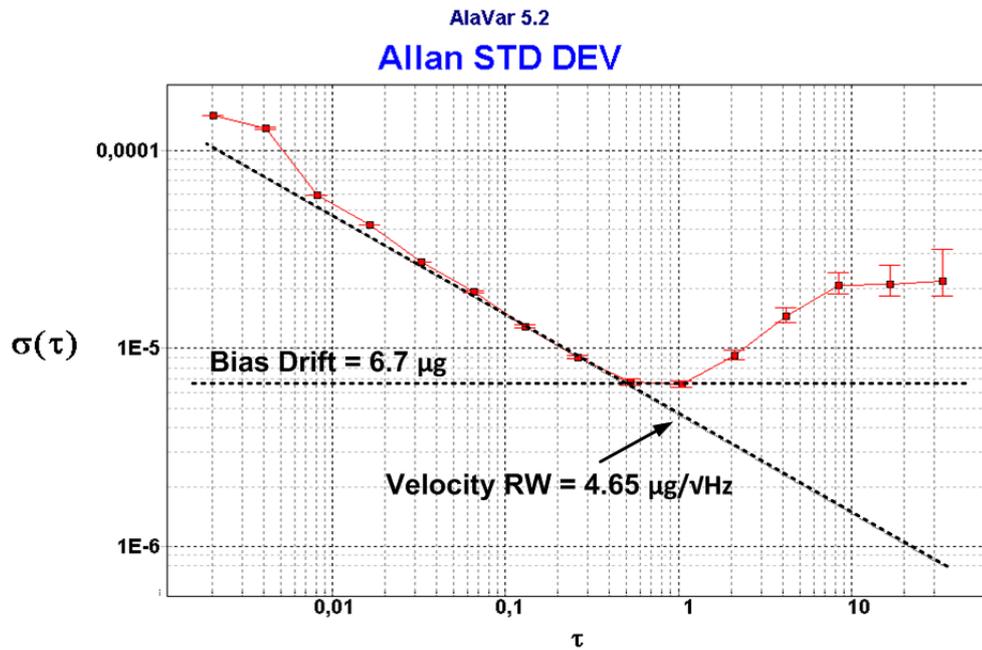
Figure 5.15: Allan Variance plot $\sigma(\tau)/\tau$ of DEWP I-12 output for $\pm$ 24.5 range.

5.4.3 Deadzone

The designed fourth order EM $\Sigma\Delta$ accelerometer is expected to be completely free from deadzone effects. For this reason, a deadzone test was done on a rotating table in order to evaluate the performance of the accelerometer system around zero g. Figure 5.16 shows results obtained from such a test, showing that transition between zero-g to normal acceleration values occur normally.

Another proof for the elimination of deadzone can be obtained by analyzing the digital output of accelerometer. Figure 5.17 shows the digital output of DEWP I-10 at zero-g. Even though the sum of 1 and 0s result in an approximate average of 0.5, there are multiple patterns or frequencies in the bit stream. The deadzone phenomena only happens when the digital output "locks" to a specific frequency at the output, and hence indiciation of multiple frequencies proves that no deadzone exists for zero-g condition.
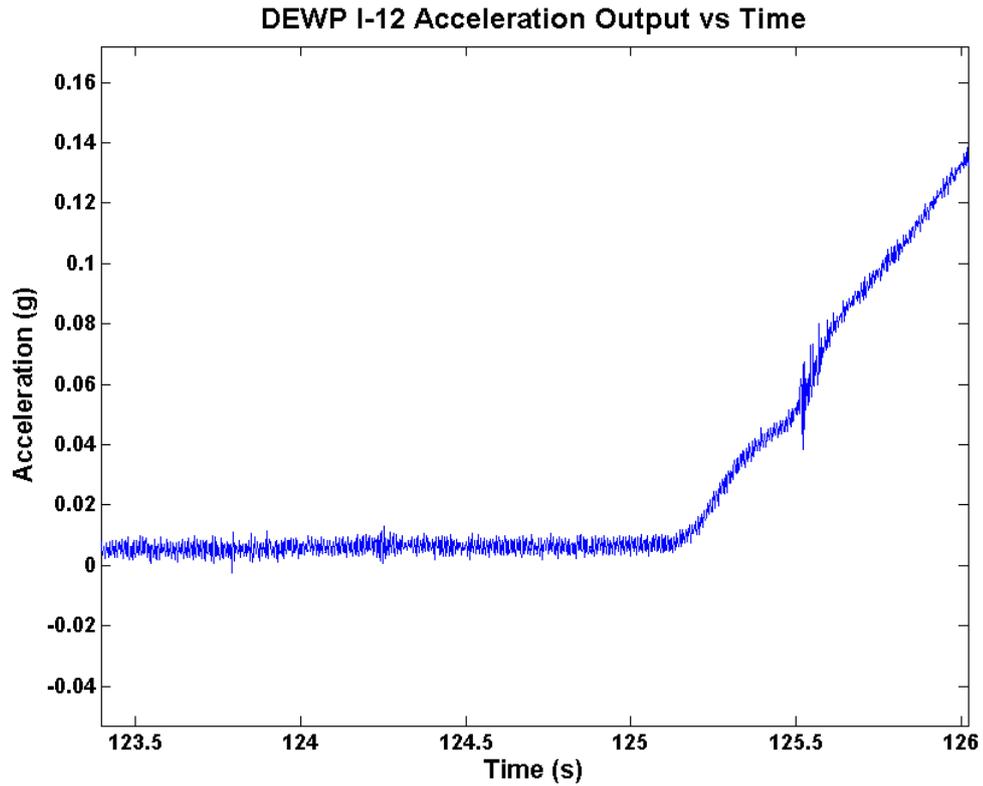
Figure 5.16: DEWP I-12 acceleration output showing no visible deadzone, even within a range of 0 to 14mg.

5.4.4 Stability

Stability is a major concern for high order $\Sigma\Delta$ systems, and this concern is also valid for the fourth order EM $\Sigma\Delta$ accelerometer system. In Chapter 3, it was established that system stability relies on the following parameters:

1. Mechanical parameters such as mass, damping and spring constants. These parameters cannot be changed once the accelerometer is fabricated.

2. Accelerometer sensitivity $\dfrac{dC}{dx}$

3. C_{INT}: Integration capacitance setting of the front-end converter

4. C_{FB}: Feedback capacitance of the noise shaper in back-end readout

5. V_{FB}: Feedback voltage
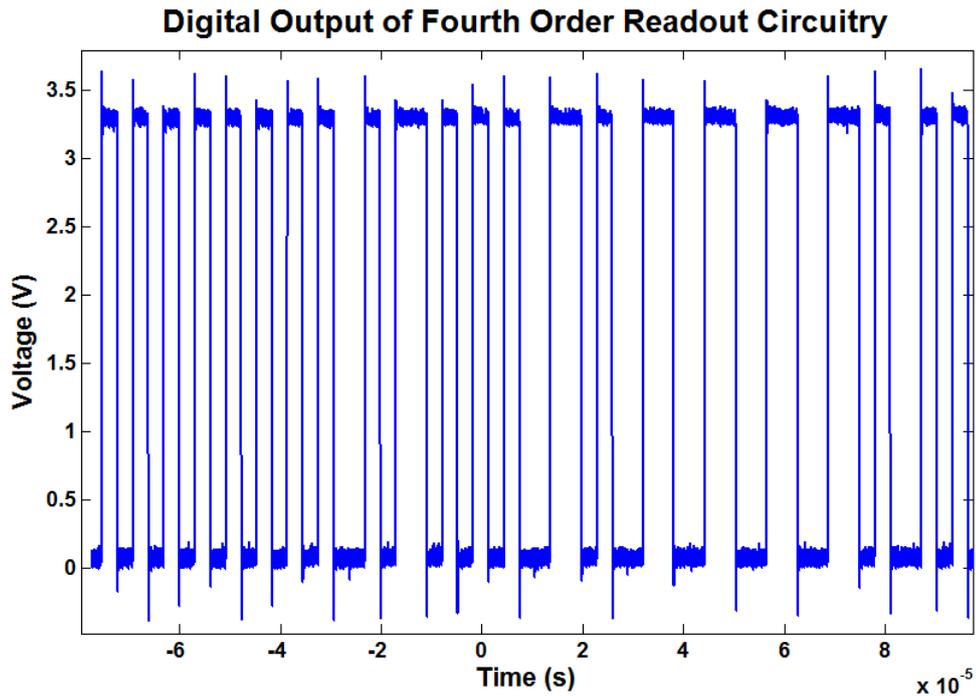
Figure 5.17: DEWP I-10 readout ΣΔ modulated digital output showing multiple frequencies in the output signal.

In theoretical design chapter, it was determined that the accelerometer system utilizing the DEWP accelerometer design should be stable for the whole range of parameters specified above. In some cases, accelerometer FSR might be degraded but stability for ± 1g range should be guaranteed.

During stability tests, this was found to be true for a wide range of these parameters. However, for C_{FB} <200 fF, the accelerometer was found to unstable. This might be caused by additional electromechanical offset effects shifting the operating point of the noise shaper integrators, or due to additional parasitic effects causing nonlinearity for the integrators. Figure 5.18 shows the output for DEWP I-12 accelerometer when it is forced to operate in unstable configuration. From the Figure, instead of white noise, a periodic signal can be detected. Note that the amplitude of this periodic signal is very low, so low acceleration noise sources will not be observed. This experimental result shows us if weird pehonema such as deadzones, glitches and periodic waveforms are seen at an accelerometer's output, a stability problem might the culprit.

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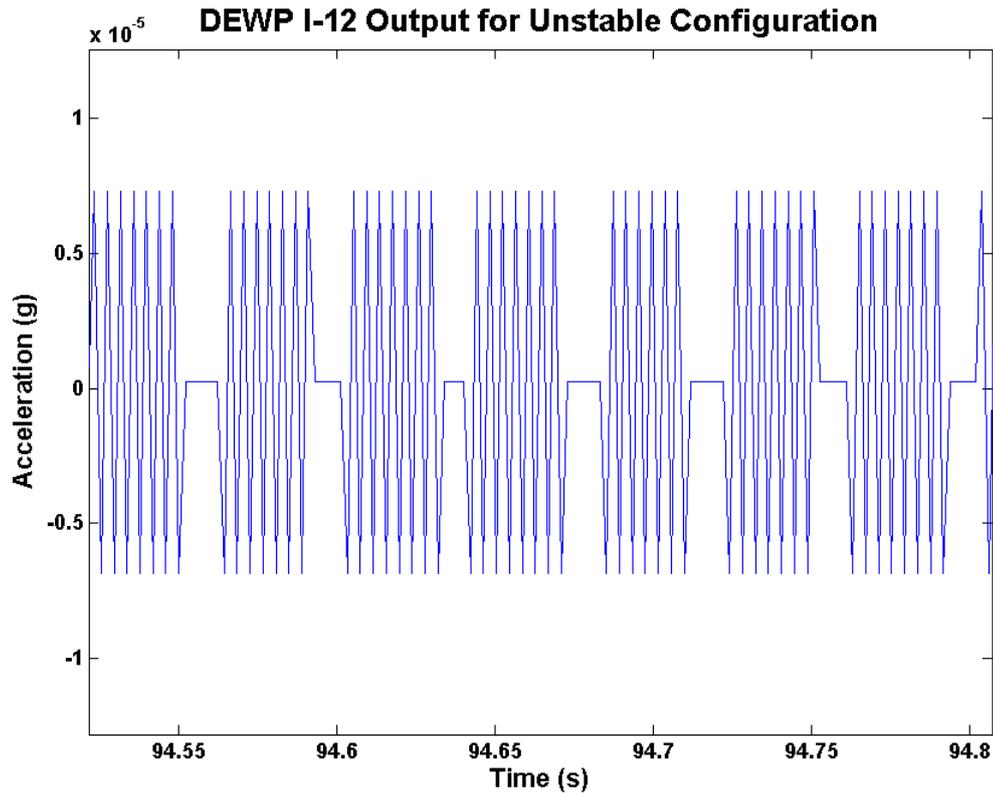
Figure 5.18: DEWP I-12 output for unstable configuration, showing a deadzone-like periodic behavior.

Accelerometer DEWP I-12 was tested thoroughly in order to replicate the instability condition for $C_{FB} > 200$ fF, however all the tested configurations were found to be stable.

5.4.5 Full Scale Range

In previous works on accelerometers in METU-MEMS Center, full scale range tests of accelerometers were done in TUBITAK-SAGE's high-range compliant rotating chambers [19]. Unfortunately, full scale range tests could not be done with fourth order accelerometers due to problems related with TUBITAK-SAGE's setup. Therefore, it was not possible to obtain experimental results of the accelerometers beyond ± 1g, which is the maximum amount of acceleration that can be applied to the accelerometer without a special setup.

It is however, possible to estimate the full scale range from bias and scale factor parameters calculated in Section 5.4.1. Assuming bias drift due to mechanical and electronic offsets are

small and with bias point (B) and scale factor (S_F) parameters known; the full scale range (FSR) can be found to be,

$$FSR = \pm \frac{B}{S_F}$$ (5.6)

This relationship can be easily obtained from the assumption that in a 1-bit 0-1 output accelerometer system, bias point corresponds to zero-g condition, while zero output corresponds to maximum negative acceleration. Subtracting the bias point from zero and dividing by scale factor, therefore gives an estimation of full scale range.

Table 5.1 lists the estimated full scale range specifications of DEWP I-12 under various feedback voltage levels. Note that, as feedback voltage increases FSR increases parabolically.

Table 5.1: Full Scale Range of DEWP I-12 for different feedback voltage levels

Feedback Voltage	$\pm$ FSR
8.2	18.5 g
9.3	24.5 g
10	28.3 g
10.6	30.6 g
11.3	34.1 g
12.1	37.2 g

5.5 Summary of the Chapter

In this chapter, implementation of the readout circuitry with a live MEMS accelerometer and results obtained from this implementation was discussed. Design of a hybrid package for MEMS-ASIC implementation and an interface PCB was also discussed, as well as the integration between the interface PCB and FPGA. A decimation filter was implemented on the FPGA to convert the PDM 1-bit readout output to a high resolution digital signal.

The designed fourth order readout circuits worked as expected, and complete accelerometer performance specifications were considerably improved. Deadzone phenomena was completely eliminated, and a best noise performance of 5.95 µg/$\sqrt{\text{Hz}}$ was obtained. Estimated full scale range of the implemented accelerometers can be improved up to $\pm$ 37.2g, a best dynamic range value of 131.7 dB was obtained.

CHAPTER 6

CONCLUSION

In this thesis, a readout circuitry for high performance MEMS capacitive accelerometers has been designed and implemented. Using a fourth order $\Sigma\Delta$ architecture, the implemented readout circuitry achieves 5.95 μg/$\sqrt{\text{Hz}}$ resolution, 6.4 μg bias drift, up to $\pm$ 37.2 g expected full scale range and 131.7 dB dynamic range. Table 6.1 compares these performance specifications to results obtained in the literature, and the designed system compares very favorably to state of the art implementations.

Table 6.1: Comparison of performance parameters of various state-of-the-art accelerometers

Accelerometer	$\Sigma\Delta$ Order	Noise	FSR	DR
This Work	4	5.95 μg/*sqrt*Hz	$\pm$ 37.2 g	131.7 dB
Colibrys [17]	5	1.7 μg/*sqrt*Hz	$\pm$ 11.7 g	136.8 dB
Boser [11]	4	150 μg/*sqrt*Hz	-	-
Ayazi [13]	4	0.2μg/*sqrt*Hz μg	$\pm$ 0.1 g	113.97 dB
Wu [34]	3	-	$\pm$ -	100 dB

In another work [33], simulated noise of the unconstrained fourth order accelerometer has been found to be 0.4 μg/*sqrt*Hz, with a dynamic range of 120 dB. Also, no implementation with an ASIC was reported. The current implementation in this work is the only and best unconstrained $\Sigma\Delta$ accelerometer implementation, and as far as we know, the second best accelerometer in the literature in terms of dynamic range. The final accelerometer system is also very close to reaching navigation grade specifications, and only fails to do so because of mechanical noise limitation.

This work has additional benefits other than significant improvements to accelerometer dy-

namic range performance, and these can be listed as:

1. A novel OTA suitable for oversampled data converters was investigated in this work. The designed OTA uses the recycling folded cascode architecture first conceived by Asaad et. al. [26], and improves its performance by minimization of 1/f noise sources and gain-bandwidth & phase margin optimization through feedforward techniques. The designed OTA can reach up to 1 GHz gain-bandwidth product with a power consumption as low as 6.9 mW.

2. Previous readout circuits designed in METU-MEMS facilities were designed in 0.6 μm technology and with this work, the process technology of further circuits have been upgraded to 0.35 μm technology.

3. Deadzone problem of previous $\Sigma\Delta$ accelerometer systems designed in METU were completely eliminated.

4. A more concrete model for calculation and estimation of quantization noise in EM was $\Sigma\Delta$ modulators was developed. An advanced simulation including all noise sources was designed in MATLAB-Simulink in order to verify this model.

5. A working test setup for noise tests of accelerometers in ± 1 g range was developed in METU. noise data of the accelerometers could be directly obtained from the readout circuits with the help of an FPGA and an interface PCB.

6. Part of this implementation including the novel OTA will be presented in International Solid State Circuits Conference 2011, in Student Research Preview event. Also, a submission has been made to TRANSDUCERS 2011 and a journal publication is being written for Journal of Solid State Circuits 2011.

Even though the performance of the final system is very good, there are several improvements that can be made to further improve the performance and flexibility of the system:

1. The $\Sigma\Delta$ analysis methodology in Chapter 3 can be improved to include noise shaping due to all noise sources and secondary effects. This can give a more clear picture about the complex relationship between noise, stability and full scale range.

2. Full scale range and linearity tests can be done to evaluate the performance of readout over the whole range.

3. The noise shaper circuitry can be modified to be full customizable, and hence NTF can be adjusted more easily.

4. A temperature sensor can be implemented inside ASIC in order to account for temperature variations and temperature sensitivity of the readout and MEMS sensor.

5. Potentially troubling noise due to actuation and electronic feedback voltage sources can be controlled by moving these voltage sources inside the ASIC. For this, a very high performance DC-DC regulator design will be necessary.

6. The MEMS sensor can be sealed with a low pressure gas in order to reduce Brownian noise, and hence noise of the complete system can be improved.

7. Additional quantization noise improvements can be done by investigation of higher (5+) order architectures, or multi feedback modulators.

As a final note, this work managed to get very close to the initial expectations of achieving navigation grade performance with a $\Sigma\Delta$ MEMS accelerometer system. With further encouragement and rigorous optimization of noise sources, the designed accelerometer system can be improved to obtain a noise floor <5 μg/*sqrt*Hz and bias drift <5 μg.

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Appendix A

MATLAB Code for Design of Unconstrained Sigma Delta Accelerometer

```matlab
% Input variables
% K = spring constant
% m = proof mass
% B = spring constant
% ts = sampling time
% Vfb = feedback voltage
% d1,d2,N,L_fin,E0,Str_th = necessary accelerometer parameters (gap, anti-gap,
% number of fingers, finger overlap area, E0 and structural thickness)
% Cint = integration capacitance
% Cfb = electronic feedback capacitance


% Assuming 50% feedback cycle from ts/2 to ts

ts=1e-6;


HSARR = tf(zeros([1 1 16]));
NTFQARR = tf(zeros([1 1 16]));
NTFEARR = tf(zeros([1 1 16]));
NTFBEARR = tf(zeros([1 1 16]));
NTFBVARR = tf(zeros([1 1 16]));
MRMARR = tf(zeros([1 1 16]));


Gn = 350; % Quantizer Gain, should be found by determining the covariance between
%a nominal quantizer input signal and quantizer output


i=1;


Cint= 12e-12;


Vfb = 9;
```

```matlab
Cfb = 2e-13;

B_acce = B;

K_acce = K;

m_acce = m;

for i=1:1:10

Vfb=9;

z=tf('z',ts);

DTHE = acos(B/sqrt(K*m)/2); % Damping theta => Ddamping Theta = arccos(1/(2*Quality_factor))

w0 = sqrt(K/m);              % Resonance frequency*2*pi

sm = -1*w0*exp(1i*DTHE);     % Sm and Sm_conjugate: Frequency domain poles of the MTF
sm_cj = -1*w0*exp(-1i*DTHE);

zm = exp(sm*ts);             % zm and zm_conjugate : Z domain poles of MTF
zm_cj = exp(sm_cj*ts);

% Now calculating accelerometer/readout feedback sensitivity
% and forward (sense) gain

% Feedback sensitivity (approx. range if feedback cycle=100%)
Fb_sens = Vfb*Vfb*0.5*E0*L_fin*Str_th*(N/((d1)^2)-(N-1)/((d2)^2));

% dc/dx differential sensitivity Assuming small variations
Ff_sens = 2*E0*L_fin*Str_th*(N/d1/d1-(N-1)/d2/d2);

% Note that the above relation is in Force (N) units. 1/(9.81*m) is ignored!
Rd_sens = 3.3/Cint;

M0 = Fb_sens*Ff_sens*Rd_sens*1/K;

R0 = M0*exp(-1i*DTHE)*(exp(-1*ts/2*sm)-exp(-1*ts*sm))*zm/(2i*sin(DTHE));
R0_cj = M0*exp(1i*DTHE)*(exp(-1*ts/2*sm_cj)-exp(-1*ts*sm_cj))*zm_cj/(-2i*sin(DTHE));

R0_cj_orj = M0*exp(1i*DTHE)*(exp(-1*ts/2*sm_cj)-exp(-1*ts*sm_cj))*zm_cj/(-2i*sin(DTHE));

zz = (R0*zm_cj+R0_cj*zm)/(R0+R0_cj);

A0 = 1;  % Should be left as 1
B0 = -3.3*Cfb/1.5e-12; % Variable D in main thesis text
```

```
C0 = 8/3;  % Variable C in main thesis text
D0 = -3.3*Cfb/1.5e-12; % Variable E in main thesis text
G0 = 0;  % Should be left as 0, if <0 then noise shaper gain is decreased.
 % if >0 then noise shaper resonates: poles move to higher freqs!


K1= 1/4;  % Variable A in main thesis text
K2= 1/4;  % Variable B in main thesis text


TD = minreal((R0)/(z-zm)+(R0_cj)/(z-zm_cj));


HNS1 = minreal((A0.*K1.*K2.*z.*z+C0.*K2.*(z-1).*z)/((z-1).*(z-1)-G0.*K1.*K2.*z));


HNS2 = minreal((B0.*K1.*K2.*z+D0.*K2.*(z-1))/((z-1).*(z-1)-G0.*K1.*K2.*z));


HS = minreal(((A0.*K1.*K2.*z.*z+C0.*K2.*(z-1).*z)*(R0*(z-zm_cj)+R0_cj*(z-zm))+
(B0.*K1.*K2.*z+D0.*K2.*(z-1))*(z-zm)*(z-zm_cj))/((z-1).*(z-1)-G0.*K1.*K2.*z)/(z-zm)/(z-zm_cj));


K1P= K1*0.999; % Finite Opamp gain (60 dB)
K2P= K2*0.999;


HNS1_FG = minreal((A0.*K1.*K2.*z.*z+C0.*K2.*(z-1+0.001*K1).*z)/
((z-1+0.001*K1).*(z-1+0.001*K2)-G0.*K1.*K2.*z));


HNS2_FG = minreal((B0.*K1.*K2.*z+D0.*K2.*(z-1+0.001*K1))/
((z-1+0.001*K1).*(z-1+0.001*K2)-G0.*K1.*K2.*z));


HS_FG = minreal(((A0.*K1P.*K2P.*z.*z+C0.*K2P.*z.*(z-1+0.001*K1))*(R0*(z-zm_cj)+R0_cj*(z-zm))+
(B0.*K1P.*K2P.*z+D0.*K2P.*(z-1+0.001*K1))*(z-zm)*(z-zm_cj))/
((z-1+0.001*K1).*(z-1+0.001*K2)-G0.*K1P.*K2P.*z)/(z-zm)/(z-zm_cj));


HS_FG0 = minreal(((A0.*K1P.*K2P.*z+C0.*K2P.*(z-1+0.001*K1))*(R0*(z-zm_cj)+R0_cj*(z-zm))+
(B0.*K1P.*K2P.*z+D0.*K2P.*(z-1+0.001*K1))*(z-zm)*(z-zm_cj))/
((z-1+0.001*K1).*(z-1+0.001*K2)-G0.*K1P.*K2P.*z)/(z-zm)/(z-zm_cj));


HSARR(:,:,i)=HS_FG;


NTFQARR(:,:,i)=minreal(1/(1+Gn*HS_FG)*1/(1+Gn*HS_FG));


NTFEARR(:,:,i)= minreal((1+Gn*HNS2_FG)/(1+Gn*HS_FG)*(1+Gn*HNS2_FG)/(1+Gn*HS_FG));


NTFBVARR(:,:,i)= minreal(minreal(HS_FG)/(1+HS_FG)/Vfb*2*minreal(HS_FG)/
(1+HS_FG)/Vfb*2,sqrt(eps)*100e3);


QNMAG = Fb_sens/m/9.81/Gn;
ENMAG = 125e-9/M0*Fb_sens/m/9.81;
FVNMAG = 150e-9*Vfb/7*QNMAG*Gn;
```

```
figure(1);
[Mag1,Phs,W] = bode(QNMAG*1/(1+Gn*HS_FG)*QNMAG*1/(1+Gn*HS_FG),{10*2*pi,500000*2*pi});


plot(W/2/pi,10*log10(Mag1(:,:)));


title('Expected Shaped Quantization Noise');


hold all;


figure(2);
[Mag2,Phs] = bode(ENMAG*NTFEARR(:,:,i)*ENMAG*NTFEARR(:,:,i),W);


plot(W/2/pi,10*log10(Mag2(:,:)));


title('Expected Shaped Front-End (OTA+kT/C) Noise');


%hold all;


figure(3);
[Mag3,Phs] = bode(FVNMAG*NTFBVARR(:,:,i)*FVNMAG*NTFBVARR(:,:,i),W);


plot(W/2/pi,10*log10(Mag3(:,:)));


title('Expected Shaped Mechanical Feedback (HVDD) Noise');


hold all;


figure(4);


plot(W/2/pi,10*log10(Mag4(:,:)+Mag2(:,:)+Mag1(:,:)));


title('Expected Total Noise');


hold all;


end


%bodemag(HS_FG,{1e-12*2*pi,100000*2*pi});


%bodemag(NTFQARR(:,:),{1e-3*2*pi,20000*2*pi});


Poles = pole(HSARR(:,:,:));
Zeros = zero(HSARR(:,:,:));


B=B_acce;
K=K_acce;
m=m_acce;
```

```
figure(1);
h = findobj(gcf,'type','line');
set(h,'linewidth',2.5);
hold off;

figure(2);
h = findobj(gcf,'type','line');
set(h,'linewidth',2.5);
hold off;

%figure(3);
%h = findobj(gcf,'type','line');
%set(h,'linewidth',2.5);
%hold off;

figure(4);
h = findobj(gcf,'type','line');
set(h,'linewidth',2.5);
hold off;

%pzmap(HS_FG)
%zgrid;
```

Appendix B

Decimation Filter Verilog Implementation

B.1   First Stage Decimation Filter

```
module FirstDec_Filter_512_5thOrder(

input clk_in,
input dec1_inp,
input reset,

output [45:0] dec1_out,
output clk_mid_out

    );

// N = 512
// k = 5
// b = 1

// Every register -> k*log2(N)+b = 46 bits

reg [45:0] acc1;
reg [45:0] acc2;
reg [45:0] acc3;
reg [45:0] acc4;
reg [45:0] acc5;

//reg [45:0] acc5_d;

reg [45:0] dif0;
reg [45:0] dif1;
reg [45:0] dif2;
reg [45:0] dif3;
reg [45:0] dif4;
```

```verilog
reg [45:0] dif5;
/*
reg [45:0] dif1_d;
reg [45:0] dif2_d;
reg [45:0] dif3_d;
reg [45:0] dif4_d;
*/

always @ (posedge clk_in or posedge reset)

if (reset)

begin

acc1 <= 0;
acc2 <= 0;
acc3 <= 0;
acc4 <= 0;
acc5 <= 0;

end

else

begin

 acc1 <= acc1+dec1_inp;
 acc2 <= acc2+acc1;
 acc3 <= acc3+acc2;
 acc4 <= acc4+acc3;
 acc5 <= acc5+acc4;

end

// CLOCK DIVIDER

reg clk_mid;
reg [10:0] count;

reg [45:0] dif_reg;

assign dec1_out = dif_reg;
assign clk_mid_out = clk_mid;

always @ (negedge clk_in or posedge reset)

if (reset)
```

```
begin

clk_mid <= 0;
count <= 0;

end

else if (count == 255)

begin

clk_mid <= ~(clk_mid);
count <= 0;

end

else

begin

count <= count+1;

end

// END OF CLOCK DIVIDER

always @ (posedge clk_mid or posedge reset)

if (reset)

begin

dif0 <= 0;

dif1 <= 0;
dif2 <= 0;
dif3 <= 0;
dif4 <= 0;
dif5 <= 0;

/*acc5_d <= 0;
dif1_d <= 0;
dif2_d <= 0;
dif3_d <= 0;
dif4_d <= 0;*/
```

```
end

else  begin

dif0 <= acc5;
dif1 <= acc5 - dif0;
dif2 <= acc5 - dif0 - dif1;
dif3 <= acc5 - dif0 - dif1 - dif2;
dif4 <= acc5 - dif0 - dif1 - dif2 - dif3;
dif5 <= acc5 - dif0 - dif1 - dif2 - dif3 - dif4;

dif_reg <= dif5;

end

endmodule
```

B.2   Second Stage Accumulate and Dump Filter

```
module SecondDec_Filter_4_AccumulateDump(

input [45:0] AD_inp,
input clk_mid,
input reset,

output clk_final_out,
output [47:0] AD_out

    );

reg [47:0] AD_outp;
reg [47:0] AD_outr;
reg [3:0] count;

assign AD_out = AD_outp;

always@ (posedge clk_mid or posedge reset)

if (reset)

begin

AD_outp <= 0;
```

```verilog
        AD_outr <= 0;
        count <= 3;

    end

    else if (count < 4)

    begin

        AD_outr <= AD_outr+AD_inp;
        count<=count+1;

    end

    else if (count == 4 )

    begin

        AD_outp <= AD_outr;
        AD_outr <= AD_inp;
        count <= 1;

    end


    // CLOCK DIVIDER

    reg clk_final;
    reg [2:0] ccount;

    assign clk_final_out = clk_final;

    always @ (negedge clk_mid or posedge reset)

    if (reset)

    begin

        ccount <= 0;
        clk_final <= 0;

    end

    else if (ccount == 1)

    begin
```

```verilog
        clk_final <= !clk_final;

        ccount <= 0;

    end

    else

    begin

        ccount <= ccount+1;

    end

    // END OF CLOCK DIVIDER

endmodule
```