FABRICATION OF SILICON NANOWIRES BY ELECTROLESS ETCHING AND INVESTIGATION OF THEIR PHOTOVOLTAIC APPLICATIONS

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ABSTRACT

FABRICATION OF SILICON NANOWIRES BY ELECTROLESS ETCHING AND INVESTIGATION OF THEIR PHOTOVOLTAIC APPLICATIONS

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Silicon is the most important semiconducting material for optoelectronics owing to its suitable and tunable physical properties. Even though there are several alternatives, silicon based solar cells are still the most widely produced and commercially feasible system. Extensive efforts have been spent in order to increase the efficiency and decrease the cost of these systems. The studies that do not focus on replacement of the semiconducting material, mostly concentrate on the developments that could be brought by nanotechnological approaches. In this aspect, utilization of silicon nanowires has been predicted to improve the efficiency of the silicon based solar cell technology. Moreover, besides solar cells, silicon nanowires have been investigated for many other electronic systems such as thermoelectrics, light emitting diodes, biological/chemical sensors, photodetectors and lithium ion

batteries. Therefore, production of silicon nanowires through a cost-effective and well controlled method could make important contributions to many fields.

In this thesis, electroless etching method, which is a novel and solution based method enabling vertically aligned silicon nanowire array fabrication over large areas, is investigated. A detailed parametric study resulting in a full control over the resultant nanowire morphology is provided. The parameters affecting the structure have been determined as etching time, solution temperature, solution concentration, pressure and starting wafer characteristics. The results show that electroless etching method could replace the conventional silicon nanowire fabrication methods. It was shown that specific nanowire lengths for any application, can be obtained simply by adjusting the parameters of electroless etching system.

One of the most crucial features of vertically aligned silicon nanowire arrays is their remarkable antireflective properties. The optical reflectivity measurements showed that 42% reflectivity of pristine polished silicon wafer decreases down to 1% following fabrication of silicon nanowire arrays on their surface. This unique characteristic reveals that these nanowires could be used as antireflective surfaces in solar cells. Moreover, it was determined that p-n heterojunctions that are formed by silicon nanowires, namely radial heterojunctions, would yield higher efficiencies compared to planar heterojunctions because of the dramatic increase in the charge carrier collection efficiency and orthogonal photon absorption. On this subject, n-type silicon nanowire arrays were fabricated by electroless etching followed by drop casting Poly(3,4-ethylenedioxythiophene)poly(styrenesulfonate) (PEDOT:PSS) organic layer on these nanowires as the complementary layer, forming the radial heterojunction. The energy conversion efficiency of silicon nanowire / PEDOT: PSS device was found as 5.30%, while planar silicon / PEDOT: PSS control device displayed only 0.62% efficiency. Developments and optimizations in both the electroless etching method and solar cell models could lead to important developments in photovoltaic industry.

Keywords: silicon nanowires, radial heterojunction solar cells, PEDOT:PSS

ÖZ

SİLİSYUM NANOTELLERİN ELEKTROKİMYASAL DAĞLAMA İLE ÜRETİMİ VE GÜNEŞ PİLİ UYGULAMALARININ ARAŞTIRILMASI

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Silisyum, oldukça uygun ve kolaylıkla değiştirilebilir fiziksel özellikleri sayesinde optoelektronik alanı için en önemli konumda olan yarıiletken malzemedir. Alternatif malzemeler geliştirilmiş olmasına rağmen, silisyum bazlı güneş pilleri halen en yaygın olarak kullanılan ve ticari anlamda en uygulanabilir sistemlerdir. Güneş pillerinin verimliliğinin artırılması ve maliyetinin düşürülmesi üzerine oldukça yoğun çalışmalar yapılmaktadır. Bu sistemlerin temel yarıiletken malzemesini değiştirmeyi amaçlamayan çalışmalar genellikle nanoteknolojik yaklaşımlardan yararlanmayı amaçlamışlardır. Bu bağlamda, silisyum nanotellerin güneş pillerinin verimliliğini artırabileceği öngörülmüştür. Ayrıca, güneş pillerine ek olarak, silisyum nanotellerin termoelektrik sistemler, ışık yayan diyotlar, biyolojik/kimyasal sensörler, fotodedektörler ve lityum iyon pilleri gibi birçok elektronik sistemde de kullanımları araştırılmaktadır. Bu gelişmeler, silisyum nanotellerin ucuz ve kontrollü bir şekilde üretilebildiği durumlarda bir çok alanda önemli gelişmeler sağlanabileceği sonucuna işaret etmektedir.

Bu tez çalışmasında, dik olarak hizalanmış nanotellerin geniş alanlarda üretilebilmesine olanak sağlayan, oldukça yeni ve çözelti bazlı bir yöntem olan elektrokimyasal dağlama yöntemi araştırılmıştır. Ortaya çıkacak nanotel morfolojisinin kontrol edilebilirliğini gösteren detaylı bir parametrik çalışma yapılmıştır. Bu parametreler zaman, çözelti sıcaklığı, çözelti konsantrasyonu, basınç ve başlıngıç siliyum altlığın özellikleri olarak belirlenmiştir. Elde edilen sonuçlar elektrokimyasal dağlama yönteminin önceki çalışmalarda faydalanılan klasik yöntemler yerine tercih edilebileceğini göstermiştir. Her uygulama için gerekli olan belirli nanotel boylarının elektrokimyasal dağlama yönteminin parametrelerinin ayarlanmasıyla elde edilebileceği ortaya konulmuştur.

Dik olarak hizalanmış nanotellerin en önemli özelliklerinden biri mükemmel optik yansıtmazlık özellikleridir. Başlangıç silisyum altlığı %42 optik yansımaya sahipken, üzerinde nanotel oluşturulduktan sonra bu değer %1'e düşmüştür. Bu özellik silisyum nanotellerin yansıtmaz yüzeyler olarak güneş pillerinde kullanılabileceğini göstermiştir. Ayrıca, silisyum nanoteller ile oluşturulan, radyal farklı tip p-n eklemlerinin düzlemsel farklı tip p-n eklemlerine göre çok daha yüksek verimliliğe sahip oldukları belirlenmiştir. Bu konuda, n-tipi silisyum nanoteller üzerine p-tipi PEDOT:PSS damlatılarak kaplanması ile radyal farklı tip eklemler oluşturulmuştur. Bu radyal eklemli aygıtların enerji dönüşüm verimlilikleri %5.30 olarak elde edilirken, aynı koşullarda üretilen düzlemsel kontrol cihazı sadece %0.62 verimliliğe sahiptir. Hem elektrokimyasal dağlama yönteminde hem de güneş pili modellerinde yapılacak iyileştirmeler ve gelişmeler güneş pili endüstrisinde önemli gelişmeler sağlayabilecektir.

Anahtar Kelimeler: silisyum nanoteller, radyal değişik tür eklemli güneş pilleri, PEDOT:PSS

To My Family...

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CHAPTER 1

INTRODUCTION

There are three major global problems that coincide with each other; the rapid increase in the world's energy demand, insufficient petroleum based energy sources and emission of the harmful fossil fuel products that causes major pollution and health problems. These facts have directed researchers to develop systems that serve to the energy demand utilizing renewable energy sources. Among these alternatives, solar cell technology stands as the most practical and feasible one, as it is based on the direct conversion of the solar energy into electricity without the need of any moving or complex parts.

Following the discovery of the photovoltaic effect, many different types of solar cells have been produced and they are grouped according to their material types. Silicon, the most well-known semiconductor with a narrow band gap and tunable physical and electrical properties, has been the most feasible and commercially available material. Although silicon based solar cell systems outperform other systems with relatively high energy conversion efficiencies, these wafer based technologies require large amounts of investments. The equipments for high temperature doping processes are still expensive and these systems require high energy and labor inputs. Also, excessive amounts of materials are spent in a regular crystalline silicon based solar cell production procedure and post treatments. In order to increase the cost-effectiveness of such systems, scientists focused on either new semiconducting materials, thereby completely new systems or the use of nanostructures and the strategy of quantum confinement leading to developments in the silicon based photovoltaic technology. Solar cells are classified into three categories, depending on their time of discovery and the type of materials they utilize. The first generation

solar cells are crystalline silicon based conventional solar cells that has been studied over many years. The second generation systems have been gaining market share since 2008 and are based on thin film materials. This group of solar cells aims to use alternative material deposition techniques that avoid high temperature processing, decrease the production costs and minimize material use. They also enable use of flexible substrates. However, defective structures restrict them from performing as efficient as first generation solar cells. The most recent studies, namely third generation solar cells, are supposed to become high efficiency-low cost systems, but they have not been commercialized yet. Nanocrystalline silicon solar cells, dye sensitized solar cells, organic solar cells, multi-junction tandem solar cells and photoelectrochemical cells belong to this category. They aim to enhance poor electrical performance of second generation technologies, while maintaining very low production costs.

Nanotechnology is based on the reduction of the size of the materials down to nanoscale or changing the atomic structure of a material in nanoscale to increase its performance, both of which would then bring completely new characteristics. A material with at least one dimension below 100 nm is accepted as a nanomaterial (or nanostructured material). Nanomaterials can be fabricated through two approaches. First one is the bottom-up approach, where one uses atoms to assemble nanomaterial of interest. In the second method, called top down, bulk materials are refined down to nanomaterials using chemical or physical means. Application of nanomaterials in optoelectronics has been investigated in many studies. Especially over the last decade, silicon nanowires have drawn attention as they introduce unique optical and electrical properties to the systems they are utilized. It was also observed that their characteristics change depending on their morphologies, whether they are synthesized in horizontal networks, vertically standing arrays, stacked arrays with extremely high aspect ratios. Considering the fact that different applications would require different nanowire geometries, it is essential to produce them as accurately and precisely as possible.

Most of the researchers have preferred to employ vapor-liquid-solid (VLS) method for the synthesis of silicon nanowires. This is because VLS facilitates a full control

over the resultant nanowire structure. Other bottom-up techniques like physical vapor deposition and laser ablation were also used for the silicon nanowire synthesis. Although most of these methods have shown reliable results in terms of yielding desired nanowire structure, they all contain two important drawbacks, which are not only valid for silicon nanowire based fields, but also major concerns for many nanoscience related studies. The first one is high equipment costs and the second one is the area limitation. The basis for applying nanotechnological methods would be to improve the cost effectiveness of the electronic devices. Therefore, using such expensive set-ups for fabrication of nanomaterials would be in contrary to the starting motivation of this concept; unless an extremely large improvement in the performance of the electronic systems with nanowires is attained. The second issue, area limitation is another factor that would prevent commercial scale applications. Nanowires can only be fabricated on the substrates that are large enough to fit inside the chamber of the growth apparatus. Consequently, only a lab-scale study can be carried out using these methods and any large-scale production falls out of consideration. Therefore, new methods should be designed and developed, such that the resultant structure must be comparable in terms of the material quality, precision, reliability and reproducibility and at the same time the method should not involve costly set-ups and allow the synthesis of nanowires over large areas, if an application such as solar cells is sought.

In comparison with all the other conventional techniques, electroless etching stands as a solution based alternative that fits the profile of being a cost-effective approach. It was first introduced as a two step etching technique [1]. The first step involved coating of the silicon wafer by homogeneous silver (Ag), gold (Au),iron (Fe), platinum (Pt), copper (Cu) or nickel (Ni) films. Then, the second step was to immerse the wafer into hydrofluoric acid/hydrogen peroxide (HF/H_2O_2) solution, facilitating galvanic reactions between the metal and HF, inducing formation of pores leaving columnar, wire-like structures at the surface. This method was converted into single step etching mechanism by Peng et. al. [2], as the wafer was directly placed into hydrofluoric acid/silver nitrate ($HF/AgNO_3$) solution facilitating vertically aligned silicon nanowire fabrication. This simple method has drawn attention and several research groups have been working on exploration of the

mechanism behind this procedure. In this thesis, in the first part (Chapter 2) electroless etching method was studied and a detailed parametric study leading to the fabrication of silicon nanowires with desired length and distribution was conducted. There has been an important gap in the literature on the reliability of this method in terms of yielding a well controlled structure that is comparable to the nanowires produced by conventional methods. This detailed parametric study provided herein also filled this gap in the literature by revealing the effects of all process parameters on the nanowire length.

One of the most important features of vertically aligned silicon nanowire arrays fabricated by electroless etching is their remarkable antireflectivity. As the black and dull appearance of the surface containing silicon nanowires suggests, the optical reflectivity of the silicon substrate dramatically decrease following the etching process. This is due to the facts that both the optical path travelled by the incoming photons and the number of scattering events are increased, substantially. In this aspect, optical reflectivity measurements were carried out and it was found that the samples had as low as 1% reflectivity. These results point out that the silicon nanowires would not only function as the active layer of the photovoltaic device, but also act as the antireflective surface, eliminating the need of antireflective coating. Considering the fact that almost 30% of the efficiency losses are caused by reflective losses, silicon nanowire arrays would have an important contribution to solar cell systems, if an efficient model making use of these nanowires could be designed.

There are several different ways that silicon nanowires could be utilized in solar cell technology. Both homojunction and heterojunction (hybrid) solar cells could be fabricated based on nanowires. The main goal in this thesis was to get around vacuum systems and high temperature doping processes, another cost effective system. Therefore, production and characterization of silicon nanowire based radial heterojunction solar cells was investigated in the second part of this thesis (Chapter 3). It was predicted that the efficiency of planar hybrid heterojunctions, created by deposition of a complementary semiconducting thin film on a semiconducting substrate, could be increased by implementing the radial heterojunction concept that utilize nanowire arrays as one side of the junction. In this thesis, a radial

heterojunction was formed by coating p-type poly (3,4 ethylenedioxythiophene) poly (styrenesulfonate), (PEDOT:PSS), semiconducting polymer as the complementary film on n-type vertically aligned silicon nanowire arrays. This creates a three dimensional junction and a fully light absorbing active layer. The diffusion distances of the generated charge carriers were minimized. Radial heterojunctions provide much more efficient photon absorption, charge transfer and collection compared to planar heterojunctions. In order to investigate this, a control sample with planar silicon / PEDOT:PSS heterojunction was fabricated under the same conditions. Both types of devices were fully characterized and the mechanisms leading to the obtained differences were discussed. It was found that both planar and radial devices can harvest light in 300-1200 nm interval of the spectrum with radial heterojunctions displaying almost 8 folds higher efficiencies compared to planar heterojunctions. In addition, the effect of nanowire length on the device performance was determined.

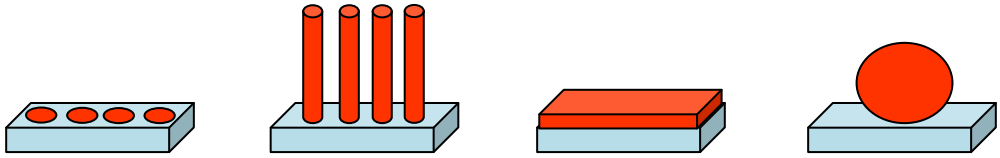
CHAPTER 2

SILICON NANOWIRE FABRICATION BY ELECTROLESS ETCHING

2.1. Introduction

2.1.1. Features of Nanowires

Nanotechnology involves working at the atomic and molecular levels in the length scale of 1 - 100 nm, in order to understand and create materials, devices and systems with fundamentally new properties and functions because of their small structure. Bulk materials consist of grains, the size of which ranges from several microns to millimeters and in each grain, they contain billions of atoms. On the other hand, nanostructured materials have much smaller grains, each consisting of only several hundreds of atoms. As a consequence of this dramatic decrease, the volume fraction of the grain boundaries and interfaces increase significantly. Considering the fact that the chemical potential at the surface of a material is much higher compared to the bulk region due to unfilled bonds of the constituent atoms, nanostructured materials gain enhanced mechanical, optical, magnetic, electrical properties, compared to their bulk counterparts. Using a variety of synthesis methods, it is possible to produce nanostructured materials in different geometries, as shown in Figure 2.1.



0-D Quantum dots **1-D Nanowires** **2-D Thin Films** **3-D Nanoparticles**

Figure 2.1. Representative schemes of nanostructured materials, which are grouped according to their dimensionality.

Nanowires, compared to other low dimensional systems, have two quantum confined directions, while still leaving one unconfined direction for electrical conduction. This allows nanowires to be used in applications where electrical conduction, rather than tunneling transport, is required. The enhanced optical and electrical properties of nanomaterials originate from the quantum confinement effect. Quantum confinement is the trapping of charge carriers in a space small enough that their quantum (wave-like) behavior dominates over their classical (particle-like) behavior. In quantum mechanical terms, for quantum confinement to occur the dimension of the confining device or particle must be comparable to, or smaller than, the de Broglie wavelength of the carriers, the carrier inelastic mean free path and electron-hole Bohr radius of the material it's made from. Because of their unique density of electronic states, nanowires in the limit with sufficiently small diameters are expected to exhibit significantly different optical, electrical and magnetic properties from their bulk counterparts. The increased surface area to volume ratio, very high density of electronic states and joint density of states near the energies of their van Hove singularities, enhanced exciton binding energy, diameter-dependent bandgap, and increased surface scattering for electrons and phonons are just some of the ways in which nanowires differ from their bulk counterparts [3].

Nanowires are expected to become important functional components as integrated circuits continue to shrink in size. In addition to enabling small circuit dimensions, nanowires are known to exhibit low capacitance which helps to reduce power consumption and enhance signal speeds in future integrated circuits. Based on the

unique electrical properties, one of the most important research fields of nanoelectronics is the nanowire based field effect transistors. Various designs of nanowire based transistors have been demonstrated in the last few years and IBM introduced silicon nanowire transistors with 2.6 nm features in 2009. Nanowires have also been proposed for applications associated with extraordinarily high piezoresistive nanomaterials [4] and superconducting nanowires [5]. Furthermore, they have been used as electron field emission sources [6] of flat panel displays since their small diameter and large curvature at the tip, reduce the threshold voltage for the electron emission [7] and display remarkable field emission characteristics.

Fabrication of chemical and biological sensors with nanowires as the active component is also an attractive application area. Nanowire sensors will potentially be smaller, more sensitive, demand less power and react faster than their macroscopic counterparts. Arrays of nanowire sensors could, in principle, achieve nanometer scale spatial resolution and therefore provide accurate real-time information. This information not only includes the concentration of a specific analyte, but also its spatial distribution. They could also provide the corresponding information on other analytes within the same submicron volume. The increased sensitivity and faster response time of nanowires is a result of their large surface-to-volume ratio and the small cross-section available for conduction channels. In the bulk, on the other hand, the abundance of charges can effectively shield external fields, and the abundance of material can afford many alternative conduction channels. Therefore, a stronger chemical stimulus and longer response time is necessary to observe changes in the physical properties of a sensor with bulk active elements in comparison to a sensor fabricated with a nanowire [3].

Another novel characteristic of nanowires is their interesting magnetic properties. It has been demonstrated that arrays of single domain magnetic nanowires, arranged in a close-packed ordered array, can be prepared with controlled diameter and length, aligned along a common direction and that the magnetic properties (coercivity, remanence and dipolar magnetic interwire interaction) can be controlled to achieve a variety of magnetic applications [8]. One of the most interesting applications is for

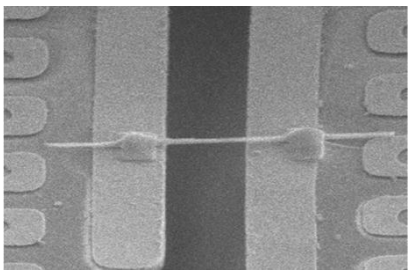
magnetic data storage, where the large nanowire aspect ratio (length/diameter) is advantageous. At the onset of the superparamagnetic limit, the magnetization direction in the magnetic grains can be reversed by the thermal energy, resulting in loss of recorded data in the magnetic recording medium. In nanowires, the anisotropy is very large and yet the wire diameters are small, so that the magneto-static switching energy can easily be above the thermal energy while the spatial resolution is large.

Nanowire based solar cells have also become one of the hot topics. With remarkable electrical and optical contributions, these systems are heavily investigated by many researchers. One of those new approaches is hybrid solar cells, where organic and inorganic materials are used in conjunction. Both the large surface area and high conductivity along the length of nanowires are favorable for their use in inorganic-organic hybrid solar cells [9] which is promising both in manufacturability and cost. In a hybrid solar cell, the incident light could form bound electron-hole pairs (excitons) in both the inorganic nanocrystal and in the surrounding organic medium. These excitons diffuse to the inorganic-organic interface and disassociate to form an electron and a hole. Since conjugated polymers usually have poor electron mobilities, the inorganic phase is chosen to have a higher electron affinity than the organic phase so that the organic phase carries the holes and the semiconductor carries the electrons. The separated electrons and holes drift to the external electrodes through the inorganic and organic materials, respectively. Silicon nanowires have a direct band gap unlike their bulk counterparts [10]. They exhibit high effective masses of electrons and holes. This is quite advantageous as it allows for extended carrier lifetime and binding energies [11]. The energy gap changes with the size of the nanowires, hence they have tunable, or wavelength selective, optical and electrical properties. For instance, the optical absorption trend could be tuned for maximum optical absorption over the spectrum of the incoming solar irradiation. In addition to this concept, silicon nanowire solar cells with coaxial and radial heterojunctions are offering unique advantages over thin film solar cells. Vertically aligned arrays of silicon nanowires enable orthogonal photon absorption and carrier collection. This allows enhanced optical absorption due to light trapping and improved carrier collection, where the carrier collection distances become comparable to minority

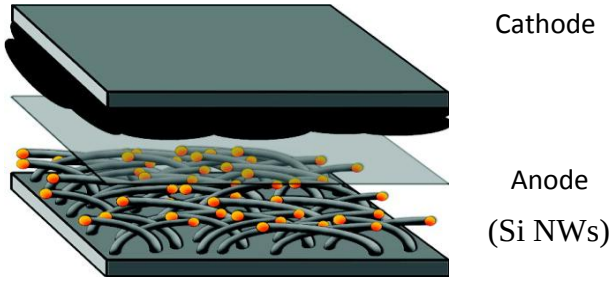
carrier diffusion lengths [12,13]. These properties point out that nanowire based solar cell technologies have great potential for development and could lead to breakthroughs in the field as the intensive research continues.

Owing to their unique properties, silicon nanowires (Si NWs) have been used in many research fields, especially in microelectronics and photonics [14,15]. In addition, silicon nanowires have been fabricated for the applications shown in Figure 2.2. List of applications include, but not limited to thermoelectric systems [16,17], lithium batteries [18,19], field effect transistors [20,21], photodetectors [22], light emitting diodes [23] and bio/chemical sensors [24]. Furthermore, it was discovered that they exhibit remarkable improvements for many different solar cell types [25,26]. In this thesis, vertically aligned silicon nanowire fabrication and their use in heterojunction solar cells are investigated.

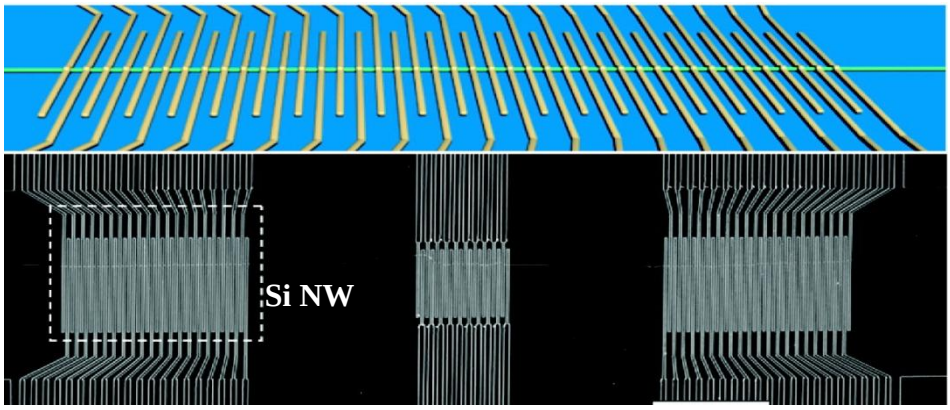
(a) Thermoelectric systems [16]



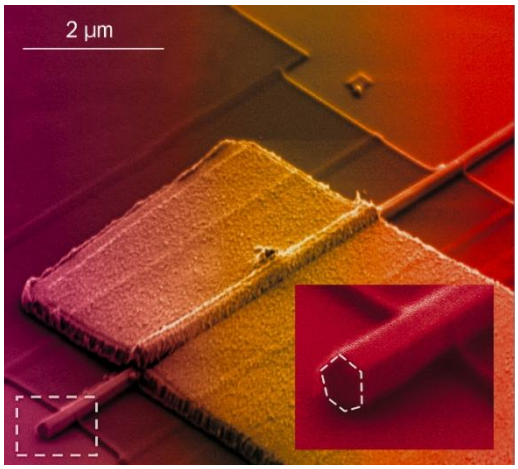
(b) Lithium Batteries [27]



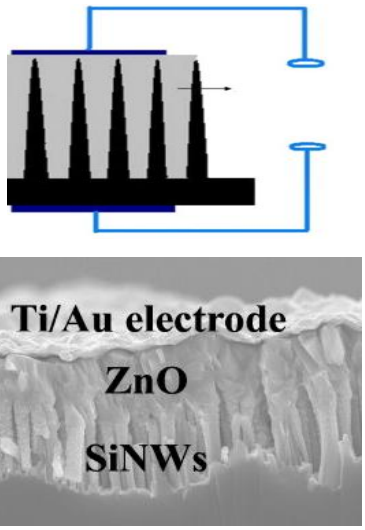
(c) Field Effect Transistors [28]



(d) Light Emitting Diodes [29]



(e) Photodetectors [30]



(f) Bio/chemical Sensors [31]

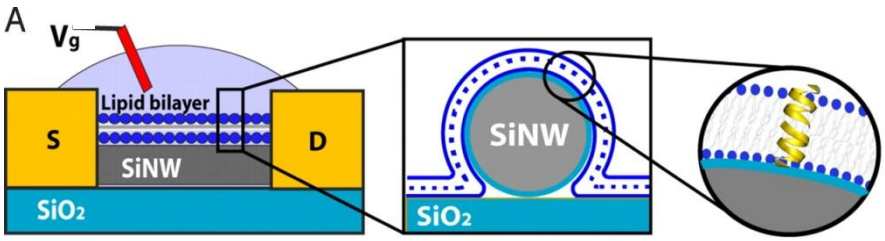


Figure 2.2. Applications of silicon nanowires other than solar cells.

2.1.2 Conventional Silicon Nanowire Synthesis Methods

Following the realization of silicon nanowires, a large number of fabrication methods have been reported. These methods are grouped according to their main mechanism such as bottom-up and top-down methods as explained before. Among these, commonly used silicon nanowire production methods are listed in Figure 2.2. The most widely used silicon nanowire fabrication method is Vapor-Liquid-Solid (VLS) method [32,33]. Also there are other bottom-up alternatives such as chemical vapor deposition [34], thermal evaporation [35], molecular beam epitaxy [36], supercritical fluid-liquid-solid [37] and laser ablation [38] that have been frequently reported. As opposed to those, silicon nanowires can also be produced by top-down approaches. Several top-down methods have been reported, namely lithographical methods [39] and direct reactive ion etching (DRIE) [40]. In this section, the most commonly encountered silicon nanowire fabrication methods are introduced.

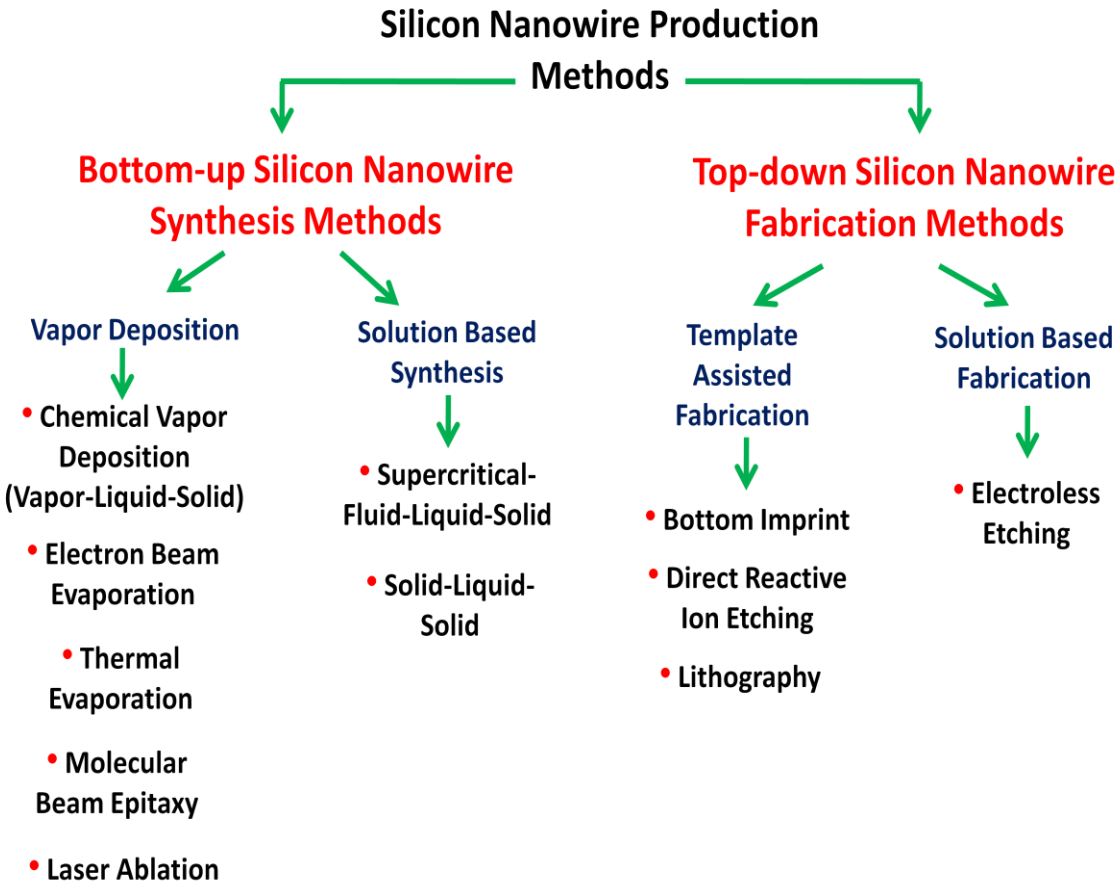


Figure 2.3. Silicon nanowire fabrication methods.

2.1.2.1. Vapor Deposition

Growth of nanowires through vapor deposition includes physical vapor deposition (PVD), thermal evaporation and chemical vapor deposition (CVD). These methods usually require a vacuum system and a reactor through which the precursor gas flows. In the PVD technique, the precursor is heated for sublimation, which then meets with the cold substrate and condenses [41]. Similarly, in CVD method, the precursor vapor is passed through a reactor. A schematic of a typical reactor is given in Figure 2.4. In this method, upon decomposition of the precursor gas, nanowires nucleate on a cold substrate, the size of which is determined by the particle residence time, temperature, precursor composition and pressure. In most of these studies, nanowires are guided through a template in order to control the shape of the resultant structure.

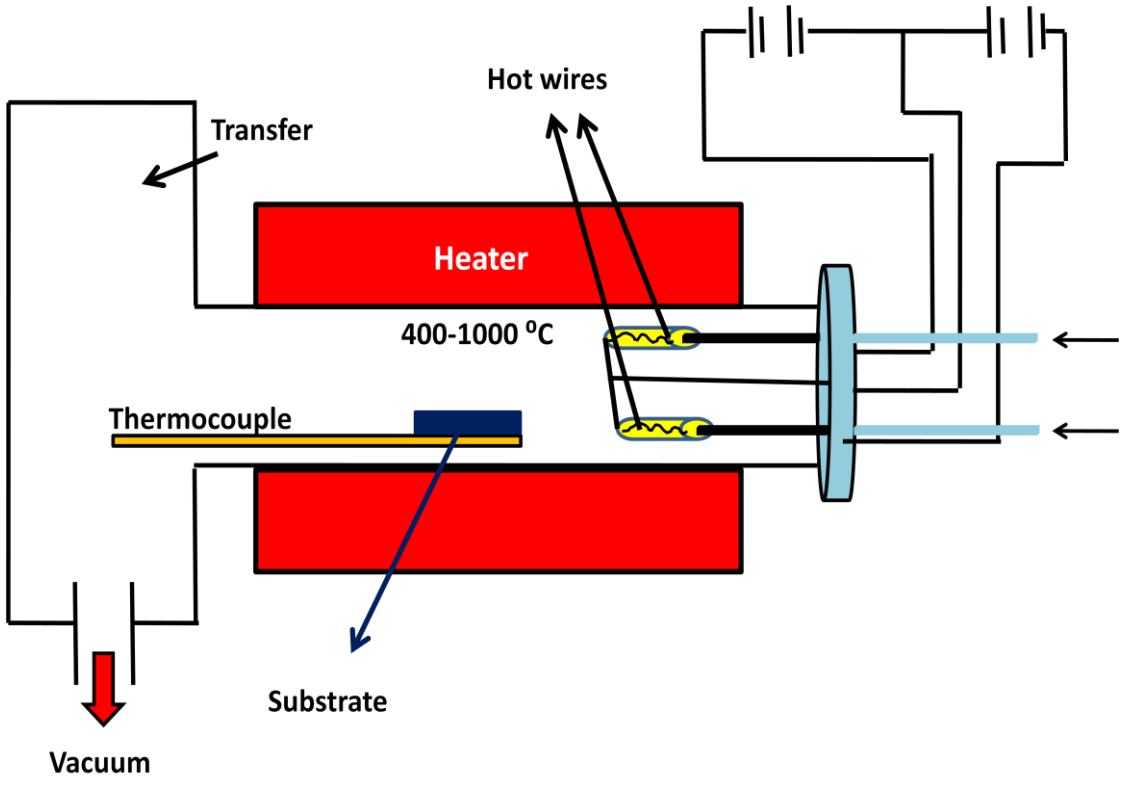


Figure 2.4. Schematic of a typical CVD reactor.

2.1.2.2. Vapor-Liquid-Solid (VLS) Method

Following Wagner and Eliss' first proposal of vapour-liquid-solid (VLS) mechanism of anisotropic crystal growth to produce semiconductor nanowires in 1964 [33], a wide range of other studies utilizing this technique have been reported. This technique allows a great control over the resultant structure and the most recent publications reporting successful synthesis of silicon nanowires utilize this method.

The growth mechanism in this method, schematically shown in Figure 2.5., can be divided into two stages; *i)* the nucleation and growth of Au-Si eutectic alloy droplets and *ii)* the growth of silicon nanowires. Au is generally used as the catalyst and silane gas ($SiCl_4$) is used as the Si source, because this system facilitates wire growth at low temperatures, in the range of 550 – 900 °C [32]. Following silane exposure, an Au-Si liquid alloy is formed. Upon supersaturation of the liquid alloy, a nucleation event generates a solid precipitate of the source material. This seed serves as a preferred site for further deposition of material at the interface of the liquid droplet, promoting the elongation of the seed into a nanowire or a whisker, suppressing further nucleation events on the same catalyst. Since the liquid droplet catalyzes the incorporation of material from the gas source to the growing crystal, the deposit grows anisotropically as a whisker whose diameter is dictated by the diameter of the liquid alloy droplet. The nanowires thus obtained are of high purity, except for the end containing the solidified catalyst as an alloy particle [42]. The presence of gold on the tip of the nanowires limits their utilization in complementary metal oxide semiconductor (CMOS) devices.

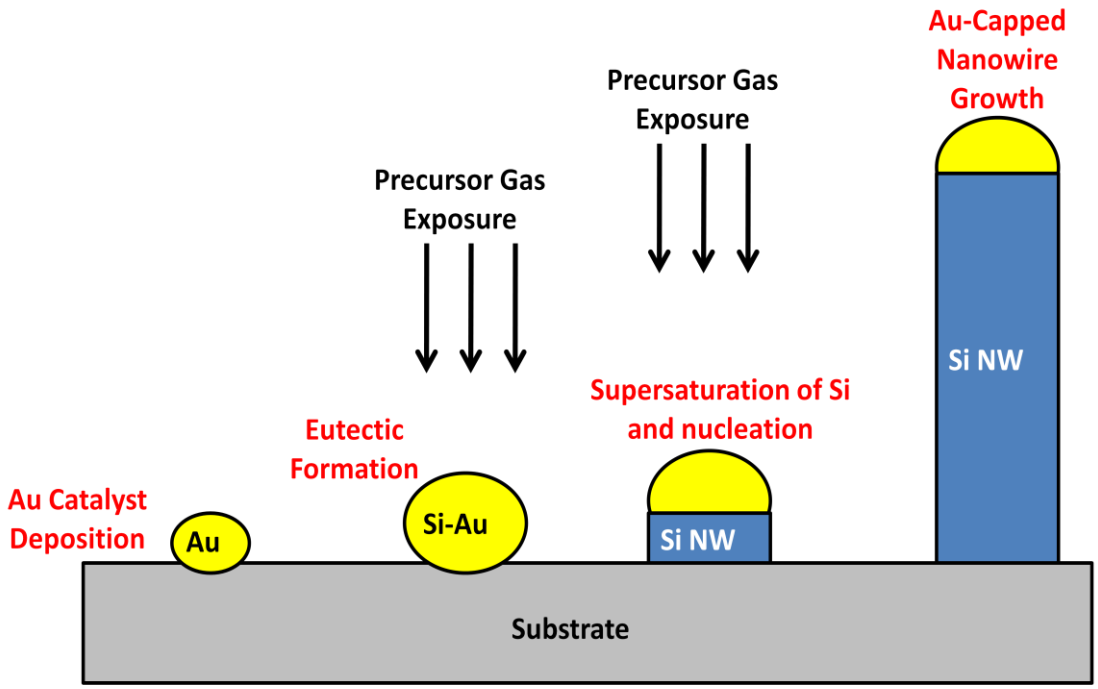


Figure 2.5. Representative sketch showing the stages of VLS growth mechanisms of silicon nanowires.

2.1.2.3. Template Assisted Growth

In template-assisted synthesis of nanowires, the chemical stability and mechanical properties of the template, as well as the diameter, uniformity and density of the pores are important characteristics to consider. Templates frequently used for nanowire synthesis include anodic alumina (Al_2O_3). Porous anodic alumina (AAO) templates are produced by anodizing pure aluminum (Al) films in various acids [43]. The concept of template assisted synthesis of nanowires is important since templates could also be adapted to the other methods. Template assisted growth yields a well controlled resultant structure and depending on the method it is assisting, highly crystalline silicon nanowires with very low density of defects could be produced.

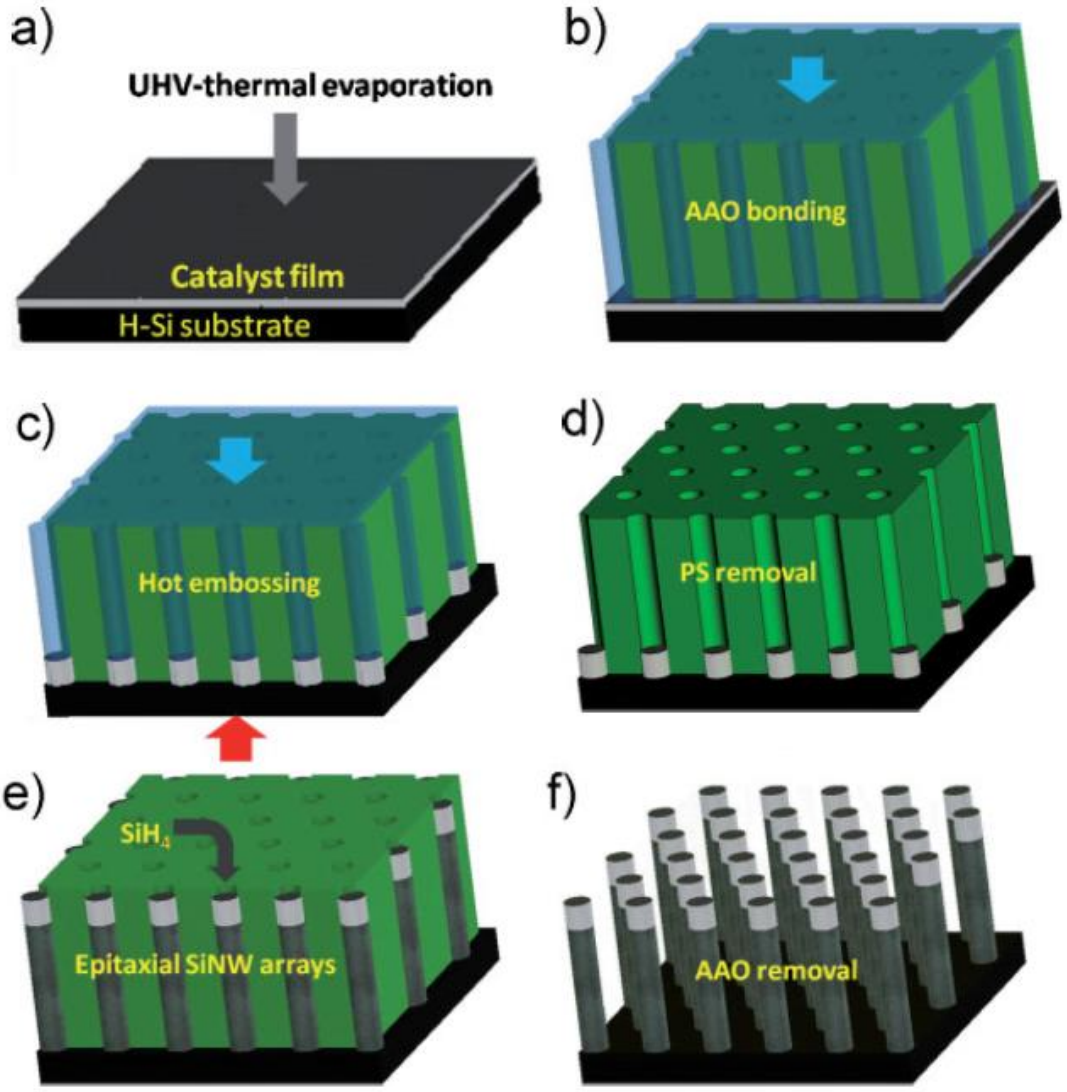


Figure 2.6. Schematic representation of silicon nanowire production using bottom imprint method [44].

A commonly used example for template assisted growth of silicon nanowires would be bottom imprint technique, shown in Figure 2.6 [44] . In this method, a hydrogen-terminated single crystal silicon substrate is covered by a homogeneous metal film, which is a catalytic agent to grow silicon nanowires. A pore-through AAO membrane filled with polystyrene (PS) is prepared and bonded to the substrate. PS occupies the pores by spin-coating on the as-anodized sample. The metal film is deformed and extruded into the end of the pores and the surrounding alumina wall is connected with the silicon substrate. To grow silicon nanowires, the imprinted sample is dipped into chloroform to remove the PS. Therefore, silicon can be grown

epitaxially inside the template by applying the CVD process. The AAO template can easily be removed by selective chemical etching and the resulting epitaxially grown nanowires have the same diameters as the imprints.

2.1.2.4. Direct Reactive Ion Etching (DRIE) Method

A typical direct reactive ion etching procedure involves several stages. A nanoimprint process is conducted first. Nanoimprinting process includes pressing a mold into a thin thermoplastic polymer film on a substrate to create vias and trenches using electron beam lithography and etching a few hundred nm into the silica layer is carried out. During the imprinting, both the mold and a polymer such as poly(methyl methacrylate) (PMMA) are first heated to a temperature higher than the glass transition temperature of the polymer. Then the mold is compressed against the sample and held there until the temperature dropped below the polymer's glass transition temperature. Isotropic plasma etching of the silicon by sulfur hexafluoride/dioxide (SF_6/O_2) is then followed by plasma deposition of octafluorocyclobutane (C_4F_8) to passivate the sidewalls and suppress lateral etching of the silicon during the isotropic step. Aspect ratios as high as 60:1 are reported for nanowires with 50 nm diameters using reduced cycle times and gas flow [45]. A representative SEM image is provided in Figure 2.7, showing well-aligned low-diameter silicon nanowire arrays produced by DRIE.

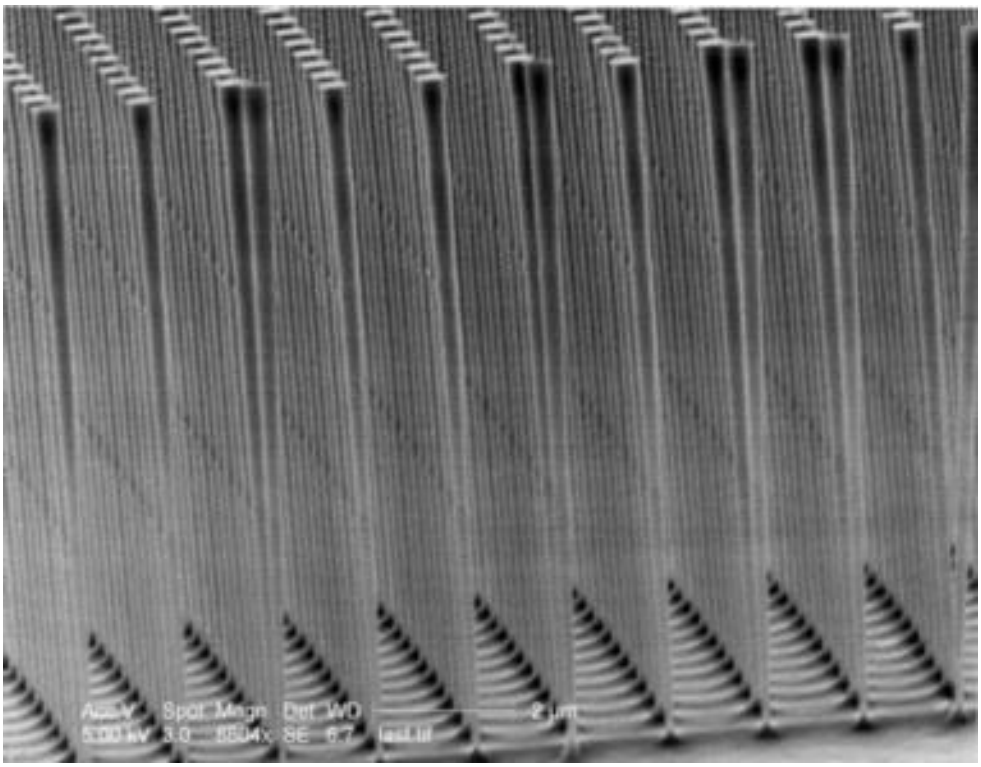


Figure 2.7. SEM image of DRIE etched silicon nanowires [40].

2.1.3. Electroless Etching Method

2.1.3.1. History and Development of Electroless Etching Method

This solution based etching method, called as "metal assisted chemical etching", was first introduced by Dimova Malinovska et. al. in 1997 [46]. The idea was to obtain porous silicon by etching an aluminum covered silicon substrate in a solution containing HF, nitric acid (HNO_3) and deionized water. The conclusion they came up with was the dramatic increase in the rate of pore formation due to the Al film. Following this study, Li and Bohn worked on this method in 2000 using various noble metals like gold (Au) and palladium (Pd) instead of Al and examined how these metals reacted with HF, hydrogen peroxide (H_2O_2) and ethanol (EtOH) solution [1]. They obtained rather sharper and straight pores within the silicon substrate. Developments in this metal assisted chemical etching method and porous silicon characteristics directed many other research groups into this cost effective method. The idea behind this mechanism is the exposure of silicon substrate which was partly covered by a noble metal to HF and an oxidizing agent, resulting in a rapid etching of the parts of the silicon substrate that are not coated with metal. This

causes the nobel metal to sink through the initially created pores and form a porous or preferentially a columnar structure.

In 2002, Peng et. al. who widely investigated the metal assisted chemical etching method, came up with a one step process. As the name suggests there is no pre-coating mechanism involved in this method. The silicon substrate was placed in $HF/AgNO_3$ solution and Ag coating and silicon etching simultaneously took place yielding a nanowire-like structure. In their study, they investigated the function of various oxidizing agents and different nitrates facilitating the galvanic reactions. In conclusion, they were able to form nanowire-nanobelt structure in a single step process, with the best results observed for the solution containing $AgNO_3$ and HF. They called this single step process as electroless etching method in their latter studies [2].

Following these studies, several other attempts understanding the mechanism and gaining control over the resultant structure were carried out [47-55]. Although this important solution based method has been widely investigated, the exact mechanism leading to selective etching has not been cleared out yet.

2.1.3.2. Electroless Etching Mechanism and Reactions

Silicon nanowire arrays form on silicon substrates by successive reduction-oxidation reactions, which take place along certain energetically favorable crystallographic orientations.. Large amounts of silver dendrides immediately cover the etched silicon wafer as a result of intense galvanic displacement reactions. Thus, the surface morphology can not be readily accessible throughout the etching duration. Nevertheless, there are two different models to explain the formation of silicon nanowires with unique shape. The first one is based on a self-assembled localized microscopic electrochemical cell model [48]. At the initial stage, silicon etching and silver deposition occur simultaneously on the silicon wafer surface. The deposited silver atoms coming into contact with silicon nucleate and grow forming nanoclusters, which are distributed throughout the surface of the silicon wafer. These

silver nanoclusters and the silicon surrounding these silver nuclei can, respectively, act as local cathodes and anodes in the electrochemical redox reactions:

$$Ag^{+} + e^{-} \rightarrow Ag_{(s)} \quad (2.1)$$

$$Si + 6F^{-} \rightarrow SiF_6^{2-} + 4e^{-} \quad (2.2)$$

These nanometer-sized, free standing excessive numbers of electrolytic cells could be spontaneously assembled on the surface of the substrate. As silver is deposited, the surrounding silicon acting as the anode is etched away as a result of the reaction with fluorine ions (F^{-}), meanwhile silver particles acting as the cathode are dispersed in the silicon nanowire array. Therefore, selective etching of the silicon wafer takes place and the silver ion and reducing agent in the solution react directly at catalytic sites on the surface without involving the substrate in the charge transfer process.

In the second model, suggested by Peng et. al., Si/$AgNO_3$/HF system is composed of a corrosion-type redox couple: the cathodic reduction of Ag^{+} ions and its counterpart, the anodic oxidation and dissolution of silicon, taking place underneath the Ag deposits. Right after immersion of the substrate into the solution, Ag^{+} ions near the surface of the substrate come into contact and capture electrons from valence band of silicon to become Ag(s) nuclei or aggregate. Due to the available extra energy around the defects, heterogeneous nucleation of Ag(s) by this electron exchange mechanism is more favourable. Due to having a high electronegativity to adhere, Ag nuclei strongly attracts electrons from silicon and become negatively charged. As a result of this phenomenon, silver nuclei serve to catalyze the subsequent reduction of Ag^{+} ions, and causes silicon oxidation. The other Ag^{+} ions coming close to the silicon surface preferentially get electrons from the silver nuclei, and are deposited around them. Consequently, growth of the silver nuclei into larger clusters occurs as the reaction goes on. Simultaneously, excess local oxidation occurs, and silicon dioxide (SiO_2) is produced underneath these silver nanoparticles. As SiO_2 is formed, it reacts with HF already present in the solution and pits would immediately form

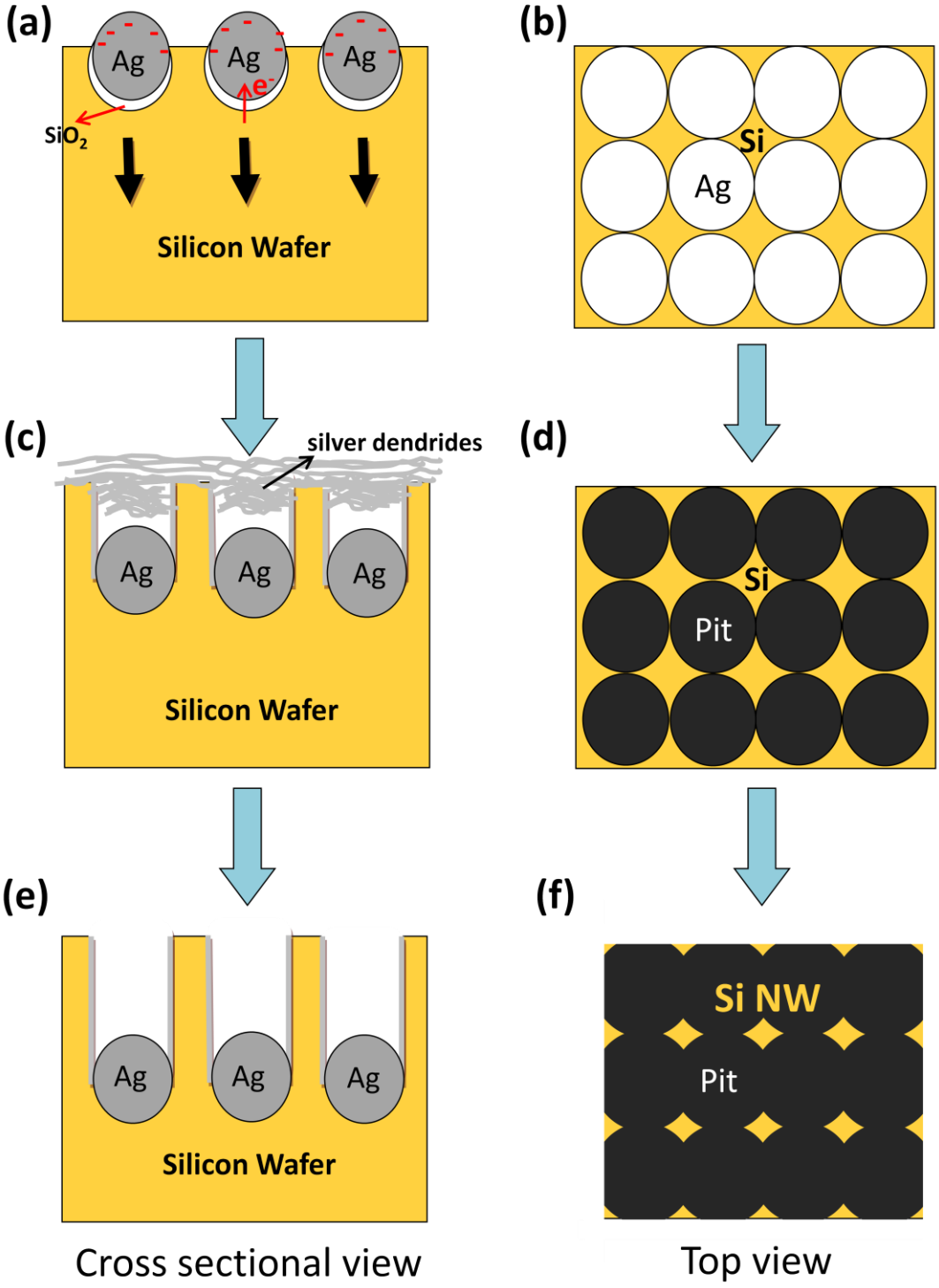


Figure 2.8. The representative scheme showing nanowire formation mechanism during various stages of the electroless etching from cross-sectional and top views. (a), (b) represent the initial stages where Ag ions come into contact with silicon and catalyze redox reactions. (c), (d) show the vertical etching of silicon leaving nanowire structure, (e) represents the final stage where silver dendrides are removed by nitric acid.

beneath the Ag nanoparticles. As a result of having a higher electronegativity, the Ag particles trapped in these pits do not move horizontally [55]. The representative figures indicating various stages of electroless etching mechanism can be found at Figure 2.8. With longer immersion times in the $HF/AgNO_3$ solution, the Ag particles that do not enter the pits would grow into branched Ag dendrites, as shown in Figure 2.8 (c). The galvanic reactions suggested by the second model are as follows [55]:

$$Ag^{+} + e^{-} \rightarrow Ag(s) \qquad (2.3)$$

$$Si(s) + H_2O \rightarrow SiO_2 + 4H^{+} + 4e^{-} \qquad (2.4)$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \qquad (2.5)$$

2.1.3.3. Comparison of Electroless Etching with the Conventional Methods

Bottom-up methods usually require complex equipment, involves high temperatures, high vacuum and hazardous silicon precursors all of which drastically increase the cost of the processes. Moreover, silicon nanowire production over large areas is not possible due to limitations in the growth setups used. DRIE, on the other hand, is an equipment and cost intensive method, where large area and homogeneous production of silicon nanowires is non-trivial. However, electroless etching method stands out in all of these important concerns. It is a rather new silicon nanowire fabrication method that provides a low temperature, cost effective and solution based alternative that enables production of vertically aligned silicon nanowire arrays over large areas. In addition, silicon nanowires formed by electroless etching method have exactly the same properties with the starting substrate (i.e. doping type and density), while those synthesized with bottom-up approaches may need to be tuned for the desired characteristics. Considering these important advantages, electroless etching method is expected to become the leading technique to produce one dimensional arrays of silicon nanowires with further developments. In the following part of this thesis, fabrication of silicon nanowires using the electroless etching method over large areas is reported. A detailed parametric study on the electroless etching process parameters such as time, temperature and the nature of the substrate were performed. Also an

analysis on the reflection characteristics of the as-produced nanowires indicating the necessary conditions for the nanowire fabrication so that they can be used as efficient absorbers in heterojunction solar cells is provided. As a consequence of geometrical dependence of physical and electrical properties of silicon nanowire based devices, it is very important to fabricate silicon nanowires in a well controlled manner. The nanowires that are produced via electroless etching method may be up to several tens of microns in length and the nanowire length variation throughout the whole surface is almost negligible. It was also found that, both polycrystalline (pc-Si), as well as monocrystalline (mc-Si) silicon substrates yield aligned silicon nanowires.

2.2. Experimental Details

Electroless etching (EE) process begins with the cleaning of silicon substrates. 400 microns thick, one side polished substrates were used. In order to observe the effect of the properties of the starting substrates, silicon wafers having different doping types (n-type, p-type), resistivities (0.1-1Ω.cm, 1-10 Ω.cm), crystal structure (monocrystalline, multicrystalline) and crystallographic orientations (100, 111) were selected as the starting substrates. Also a study on unpolished wafers was carried out. Some of these unpolished wafers were chemically cleaned and directly went under electroless etching, while some of them were saw-damage etched using potassium hydroxide (KOH) solutions prior to electroless etching. All the chemicals used in this study were purchased from Sigma Aldrich and used without further purification.

In order to obtain a homogeneous nanowire structure at the end of the galvanic etching reactions, the substrates must be completely free of impurities. Any contaminated region of the substrate may result in a disrupted structure or no nanowire formation at all. In this chemical cleaning stage, silicon substrates were consecutively sonicated in acetone (99.8%), isopropanol (99.8%) and deionized water baths for 10 minutes each. This step was followed by preparation of piranha solution by mixing sulfuric acid (H_2SO_4, 95-97%) and hydrogen peroxide (H_2O_2, 35%) in 3:1 volume ratio and immersion of the samples in this solution for 30 minutes. Then the samples were removed out of the piranha solution, rinsed under

deionized water and dipped into dilute hydrofluoric acid (HF, 38-40%) solution for 2 minutes to remove the native oxide and allow the substrate surface to become hydrophobic.

The electroless etching solution was prepared and chemically cleaned silicon substrates were immersed into that solution kept in a Teflon beaker at atmospheric pressure. The representative schematic of the experimental setup is shown in Figure 2.9. EE solution consists of $AgNO_3$ (99.5%) and HF (38-40%). In order to determine the effect of each parameter on the resultant silicon nanowire structure, cleaned silicon substrates (having various properties mentioned above) were immersed into the solution having different concentrations, for various durations (up to 10 hours), at different temperatures (0-50°C). Moreover, in order to observe the effect of high pressures on the process, the experiment was carried out in an autoclave (Parr Inst. 4744 General Purpose Acid Digestion Vessel) instead of the Teflon beaker open to atmosphere.

Prior to the immersion of the substrates into etching solution, the samples were fixed on a teflon disc by kapton tape in order to isolate the unpolished side of the wafer. This was found to be necessary since the unpolished rough surface were not facilitating vertical alignment each time, leading to confusion during SEM analysis. Although the EE mechanism is known as intrinsically anisotropic and the silicon nanowire growth direction is <100>, multicrystalline silicon substrates or substrates without smooth surfaces may result in nanowire alignments in various directions.

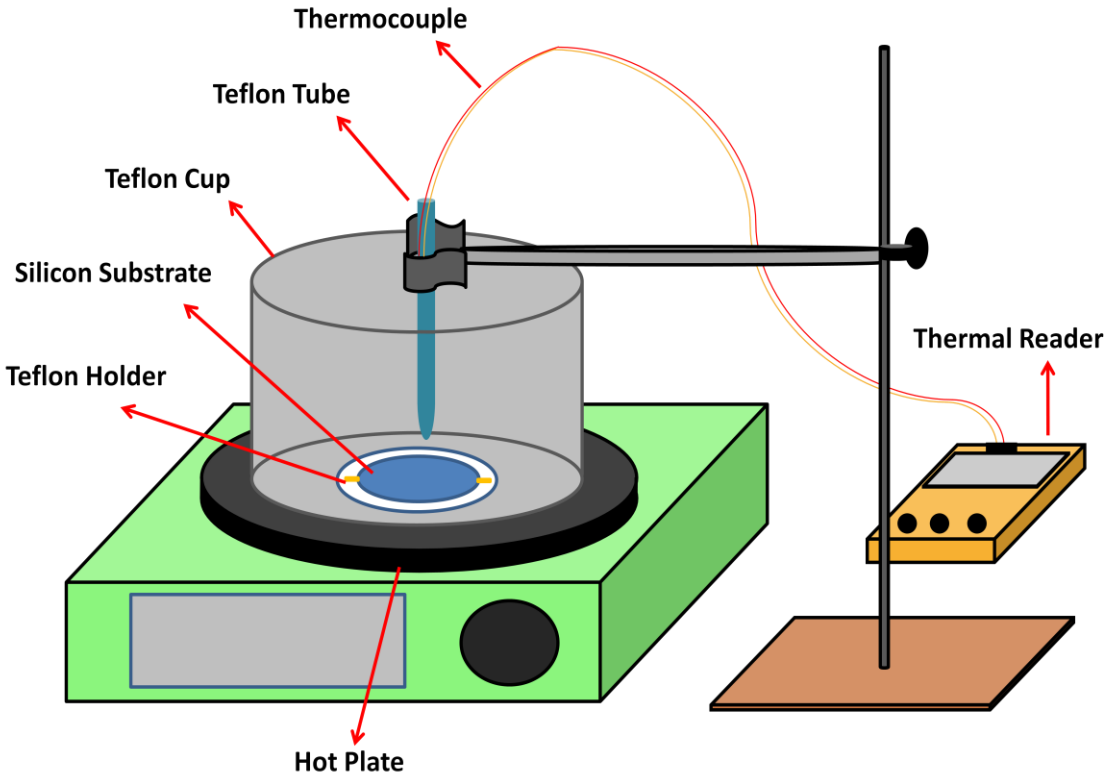


Figure 2.9. The experimental setup facilitating silicon nanowire fabrication by electroless etching method.

The desired silicon nanowire structures containing Ag dendrides are shown in Figure 2.10 (a) and (b). At the end of the etching process, samples were rinsed with deionized water and placed in dilute nitric acid (HNO_3, 65%) solution for 30 minutes to remove the Ag dendrite layer formed on top of the nanowire arrays. As the final stage of the process, samples were rinsed with deionized water and dried with a nitrogen gun. The relationship of silicon nanowire length and distribution with each EE processing parameter, namely etching time, solution temperature and concentration, wafer orientation, resistivity and doping type was determined. In order to observe this relation, only one parameter was changed at a time while the others were kept constant.

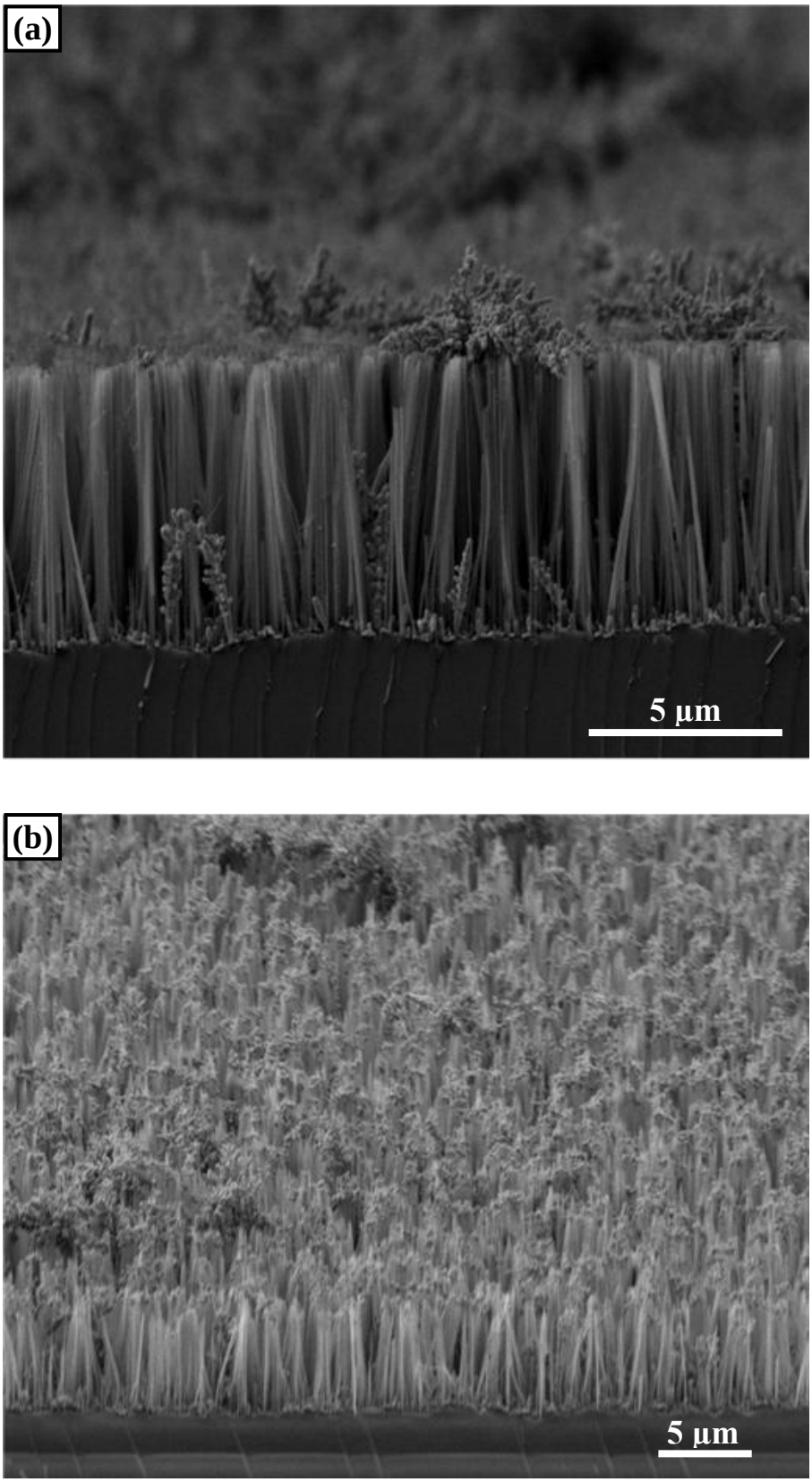


Figure 2.10. (a) Cross-sectional and **(b)** 45^0 tilted SEM images of an electroless etched silicon sample containing 8 µm long silicon nanowire arrays. The SEM examination was carried out before silver dendride removal by nitric acid.

2.3. Nanowire Characterization Methods

2.3.1. Scanning Electron Microscopy (SEM)

The resultant lengths and distributions of silicon nanowires were analyzed by FE-SEM (Nova NanoSEM 430) operated at 10 keV voltage. Cross sectional SEM images were obtained from cleaved edges of the silicon substrates. Both cross-sectional and top view SEM images were examined following each parametric change in the experimental procedure. No gold or carbon coating was utilized.

2.3.2. Transmission Electron Microscopy (TEM)

Transmission Electron Microscope (TEM) was used to observe the surface morphology in atomic scale and obtain crystallographic data. The silicon nanowire arrays were scraped off of silicon substrates, dispersed in isopropanol and drop casted on holey carbon coated 400 mesh copper grids. A JEOL 2010 high-resolution transmission electron microscopy (HRTEM) operated at 200 kV was used for characterization.

2.3.3. Optical Reflectivity Measurements

Reflectivity measurements were made through a silicon photodetector calibrated integrated sphere (Newport 70679NS) which also takes into account the diffuse reflectance. The schematic of the reflectivity set-up is given in Figure 2.11. There is a halogen lamp for light generation, chopper, a monocromator to obtain the reflectivity over a spectral bandwith and an integrated sphere with both the sample and the silicon photodetector attached.

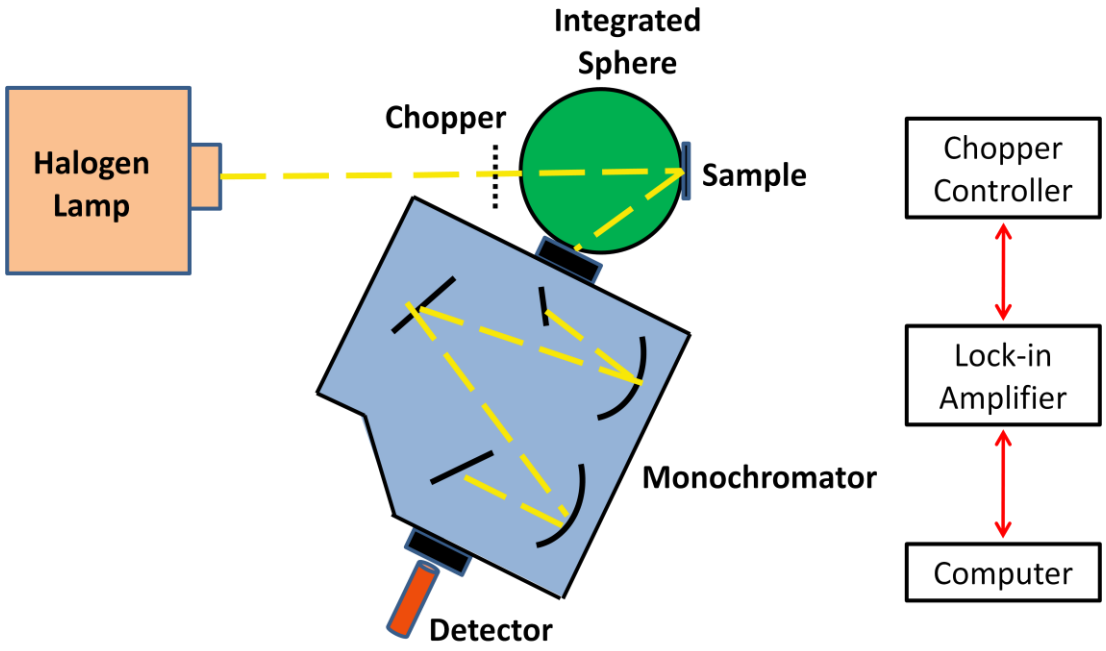


Figure 2.11. The optical reflectivity measurement set-up.

2.3.4. Field Emission Measurements

The field emission measurements of the silicon nanowires were carried out in a vacuum chamber at a pressure of $5x10^{-5}$ Pa. The current density–voltage (J–V) curves were performed using a Keithley 4200 high source measure unit. This study also included stability measurements and current-emission field characterization. The gap between the anode and the cathode was 200 µm. The average area of each sample was 2 cm^2. The setup used for the field emission measurements is shown in Figure 2.12. Field emission measurements of the silicon nanowire arrays were conducted at the Electrical Engineering Division of University of Cambridge.

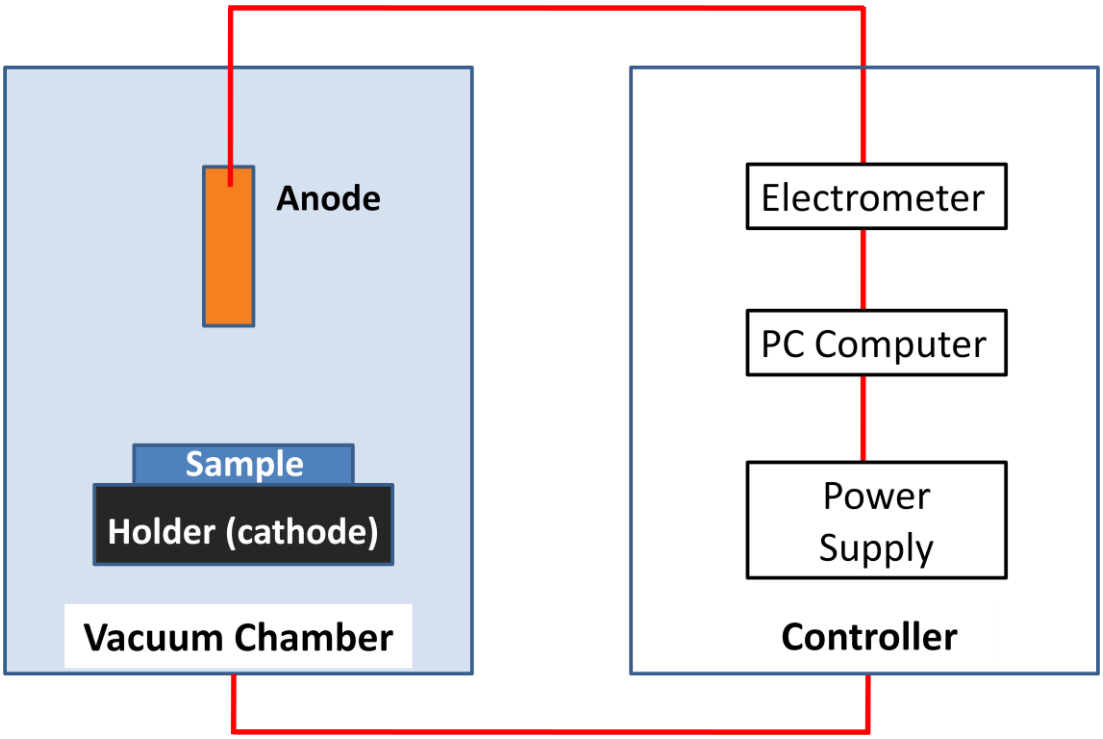


Figure 2.12. The field emission measurement set-up.

2.4. Results

2.4.1. Determination of the Electroless Etching Parameters

2.4.1.1. Solution Concentration

The most critical parameter for the fabrication of silicon nanowires with EE method is the solution concentration due to the nature of this top-down approach. Following the first report on the single step chemical etching [2] (i.e. electroless etching), a solution concentration of 0.02 M $AgNO_3$ / 4.6 M HF was often reported in the literature. The effect of solution concentration by reducing and increasing the concentrations of $AgNO_3$ and HF one at a time was investigated in this thesis. However, in all cases a more disrupted structure was obtained as the concentration was changed. The results of several attempts towards the optimization of the solution concentration are shown in the SEM images of the produced structures given in Figure 2.13. It is appearent that the silicon nanostructures in Figure 2.13 (a), (b) and (c) are not well aligned and reveal sharp nanowire morphologies; (d) on the other

hand displays vertically well aligned silicon nanowires that are homogeneously distributed over the entire surface. Therefore, the remaining process parameters were all determined using a solution concentration of 0.02 M $AgNO_3$ / 4.6 M HF.

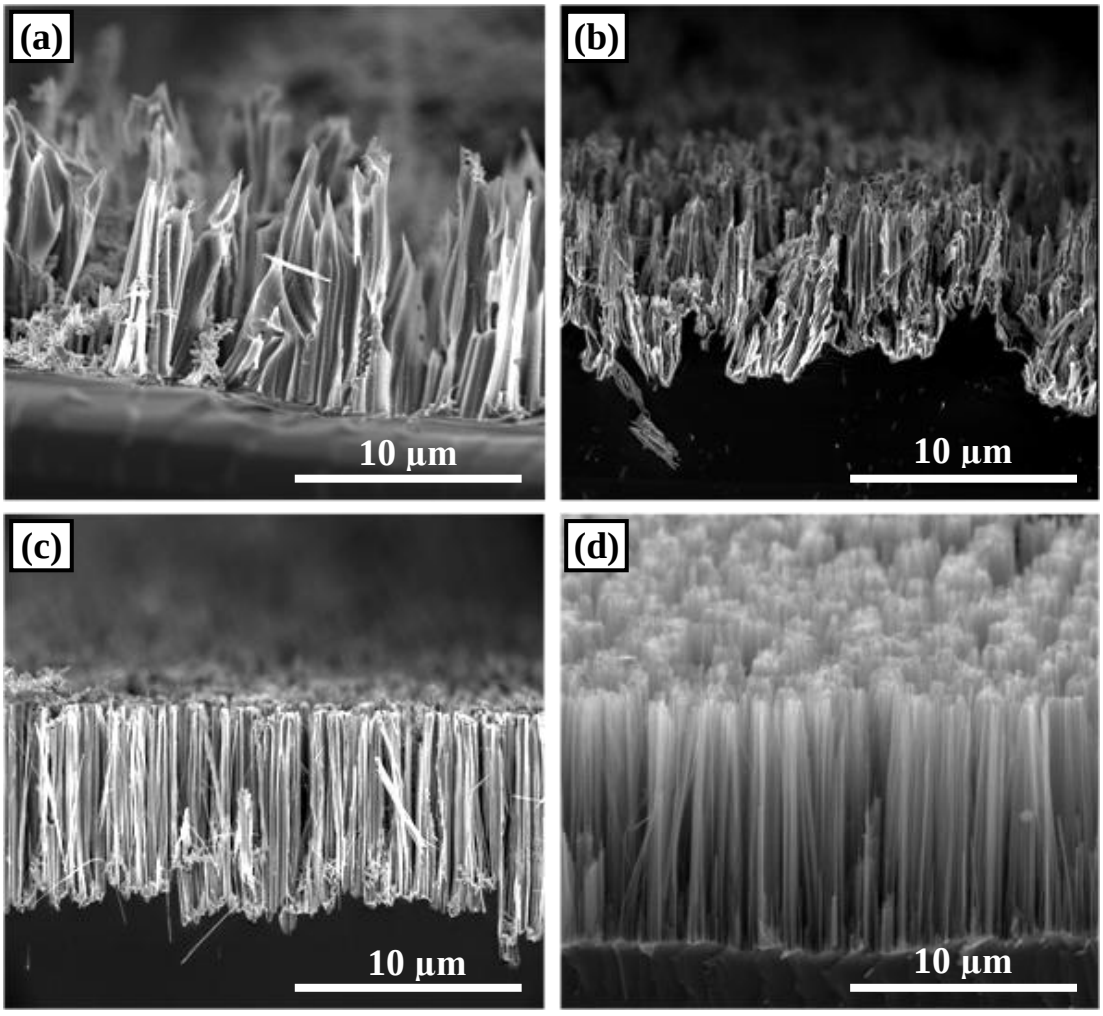


Figure 2.13. Cross-sectional SEM images of samples that are electroless etched in solutions having concentrations of (a) 0.01M $AgNO_3$ / 4.6M HF, (b) 0.02M $AgNO_3$ / 7M HF, (c) 0.04M $AgNO_3$ / 4.6M HF and (d) 0.02M $AgNO_3$ / 4.6M HF.

2.4.1.2. Time

Etching time has a direct influence on the resultant nanowire lengths. Nanowires were fabricated within etching durations of 8, 16, 40, 60, 120, 180, 240, 360, 450 and 600 minutes, while maintaining the solution concentration at 4.6 M HF/ 0.02 M $AgNO_3$ and temperature at 40°C. Among these samples, SEM images of the silicon nanowires fabricated within 8, 40, 120 and 360 minutes, are shown in Figure 2.14 (a)-(d), respectively. Vertically aligned silicon nanowire arrays can be clearly seen in

all the images. Moreover, the nanowire length as a function of etching time is plotted in Figure 2.15.

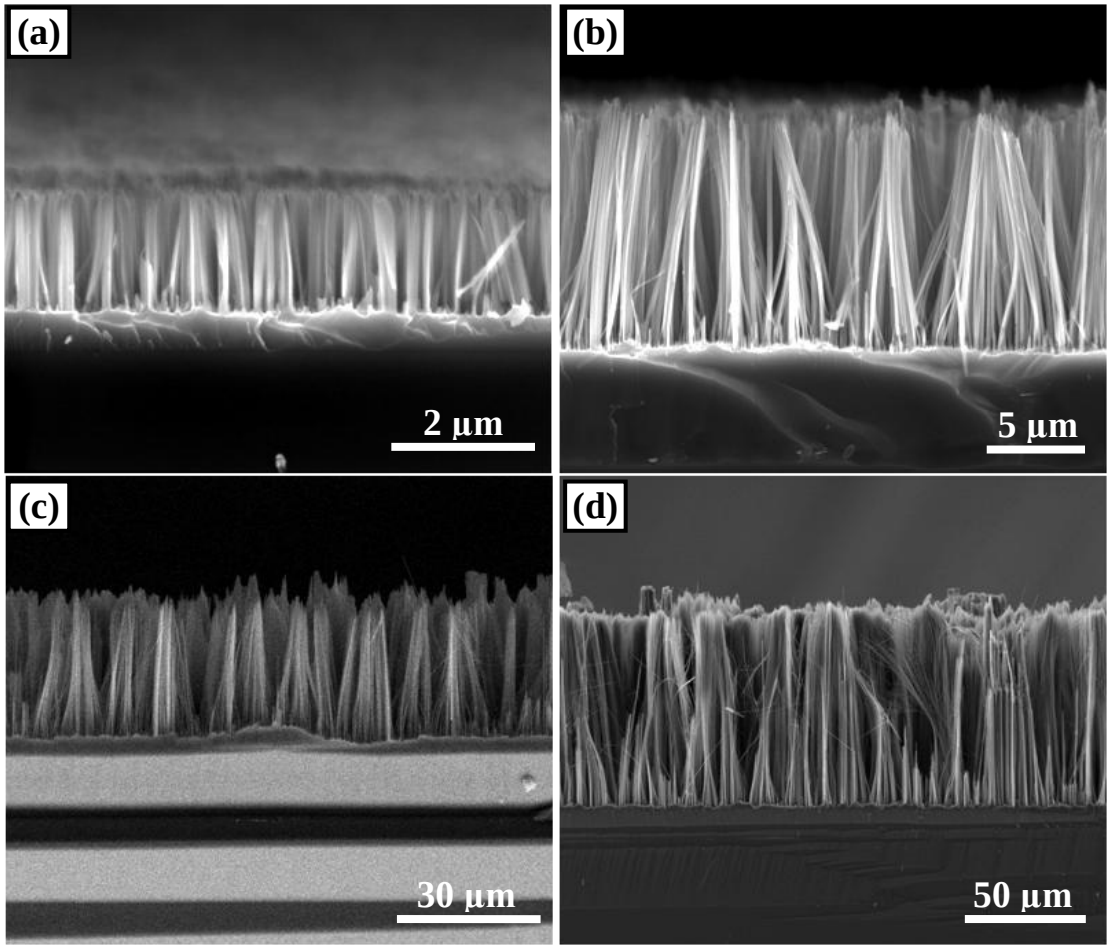


Figure 2.14. Cross-sectional SEM images of the vertically standing silicon nanowire arrays obtained by electroless etching at 40^0C in a solution containing 4.6 M HF / 0.02 M $AgNO_3$ for (a) 8 minutes, (b) 40 minutes, (c) 120 minutes and (d) 360 minutes.

In accordance with the previous work, a linear relationship between etching time and nanowire length was obtained for etching durations up to 4 hours with an etching rate of 0.25 µm/min. This clearly indicates the speed of EE process. Further etching, beyond 4 hours, again revealed a linear relationship with a change in the etching rate of the nanowires as shown in Figure 2.15. Etching rate of the nanowires between 4 to 10 hours was determined to be 0.1 µm/min. This clearly indicates that the reaction slows down due to the decrease in the reaction kinetics. This decrease in the reaction

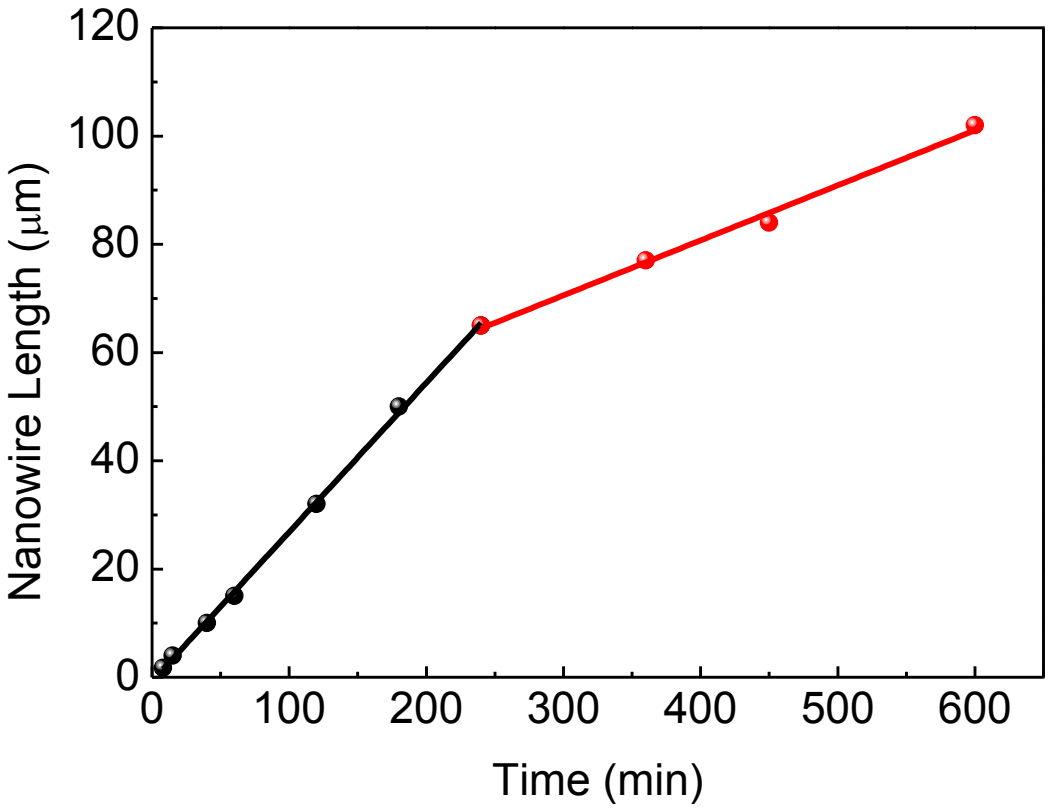


Figure 2.15. Variation of nanowire length with etching time

kinetics can be attributed to the inhibition of the sinking mechanism of Ag^+ ions to the bottom of the nanowire arrays, leading to decrease in Ag concentration. Since the reduction-oxidation reactions selectively take place at the interface between the bottom of the nanowires and the top of the bulk substrate, the drop in Ag concentration causes the etching rate to slow down.

Another aspect in the time dependent nanowire characteristics is the nanowire distribution and alignment. As the nature of the EE method, the nanowires tend to form bundles due to the capillary forces upon pulling them out from the etching solution [56]. As the etching time increases with the nanowire length, these forces become more dominant resulting in a bundled structure rather than vertically aligned individual nanowire arrays, as shown in Figure 2.16 (a). The effects of forming several tens of microns long nanowire bundles on reflectivity are also discussed within the reflectivity measurements.

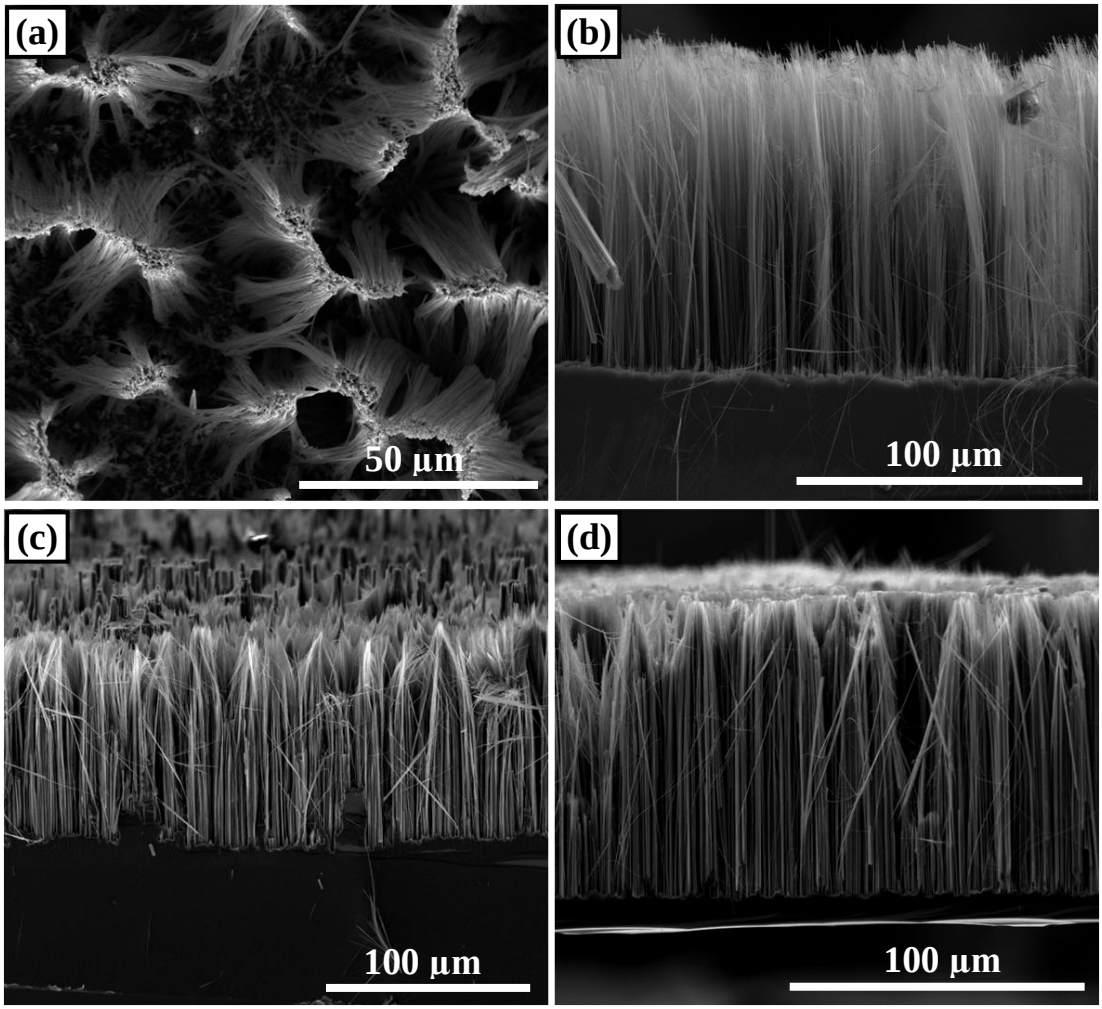


Figure 2.16. (a) Top-view SEM image of agglomerated tips of the approximately 80 µm long nanowires. (b) and (c) cross-sectional SEM images of samples with nanowire arrays longer than 100 µm. (d) Cross-sectional SEM image of electroless etched thin silicon wafer just before complete conversion into nanowires.

For several applications, relatively long silicon nanowires may be required. Even though the reaction kinetics slow down and the nanowires tend to form bundles, individually standing nanowires could still be obtained. Figure 2.16. (b) and (c) shows SEM images of silicon nanowires longer than 100 microns. Especially for the sample in Figure 2.16 (c), the bundling mechanism is considerably dominant. In addition to etching 400 µm thick silicon wafers, previously lapped approximately 110 µm thick silicon wafer was etched in order to obtain complete etching of the silicon substrate and nanowires in powder form instead of arrays. Lapping is a procedure, in which the backside of the wafer is brought into contact with an abrasive slurry to remove material from the backside. The slurry is a combination of

lapping oil and silicon carbide or aluminium oxide. The EE experiment was supposed to last until the substrate is completely converted into nanowires; however, in the late stages of EE, Ag dendride film completely covered the reacting interface and stopped the reaction from going further. SEM image in Figure 2.16 (d) pointed out that the sample had 100 μm long nanowires standing on top of only 10 μm thick substrate. Before the SEM examination, the dendride film was removed by nitric acid treatment and following the SEM analysis, the sample was immersed into a second electroless etching solution and converted completely into 110 μm long silicon nanowires.

2.4.1.3. Temperature

Temperature of electroless etching solution is another factor that has a direct influence on nanowire length, since it changes the kinetics of the reduction-oxidation reactions. The effect of the temperature was investigated in a range of 0-50 °C and it was found that the length of the silicon nanowires is linearly proportional to the solution temperature. We have avoided temperatures in excess of 50 °C due to safety reasons and to keep the solution concentration stable. Also, taking into account that one of the biggest advantages of this process is the ability to work at low temperatures, low temperatures should be preferred. SEM images of the silicon nanowires fabricated at temperatures of 0, 10, 25 and 50°C are shown in Figure 2.17 (a)-(d) respectively. Nanowire length as a function of temperature is plotted in Figure 2.18 and a linear relationship between temperature and nanowire length is obtained.

Similar to the effect of etching time, conducting the process at high temperatures cause nanowires to agglomerate into each other, meanwhile lower solution temperatures, hence slower reaction kinetics provide well aligned nanowires distributed uniformly throughout the whole wafer surface.

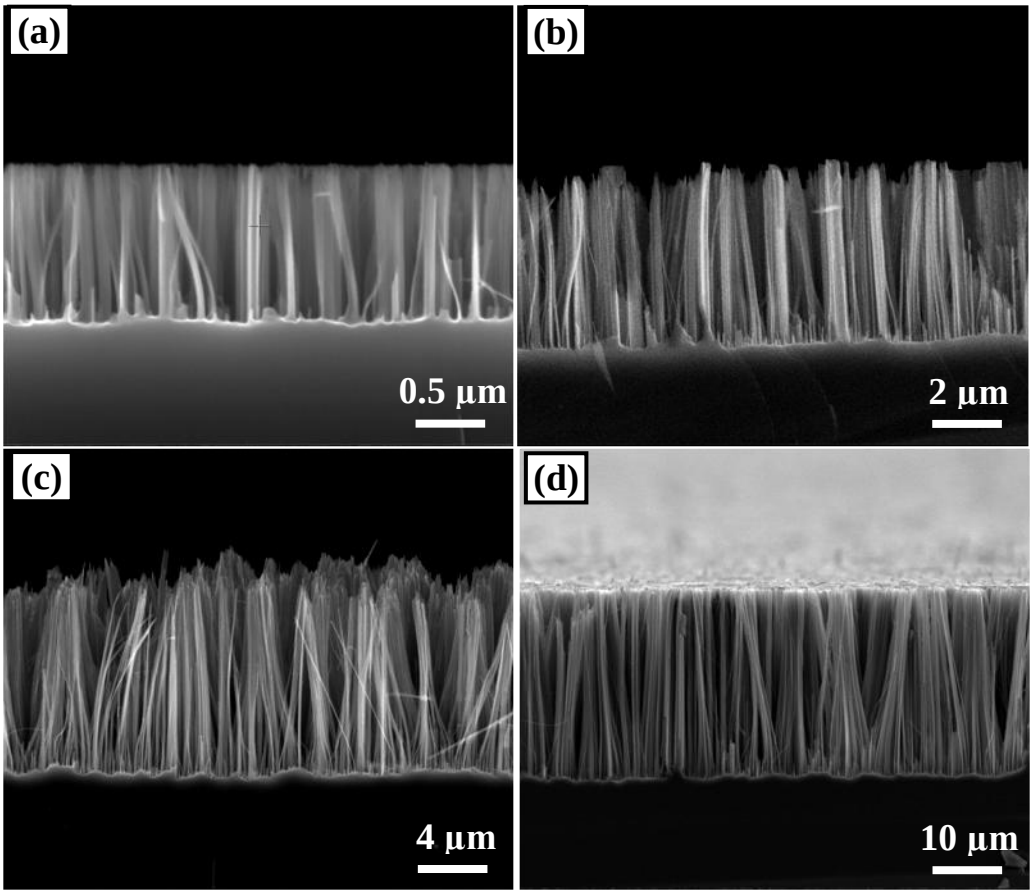


Figure 2.17. Cross-sectional SEM images of silicon nanowire arrays obtained by electroless etching method conducted at (a) 0^0C, (b) 10^0C, (c) 25^0C and (d) 50^0C upon 1 hour etching in a solution containing 4.6 M HF / 0.02 M $AgNO_3$.

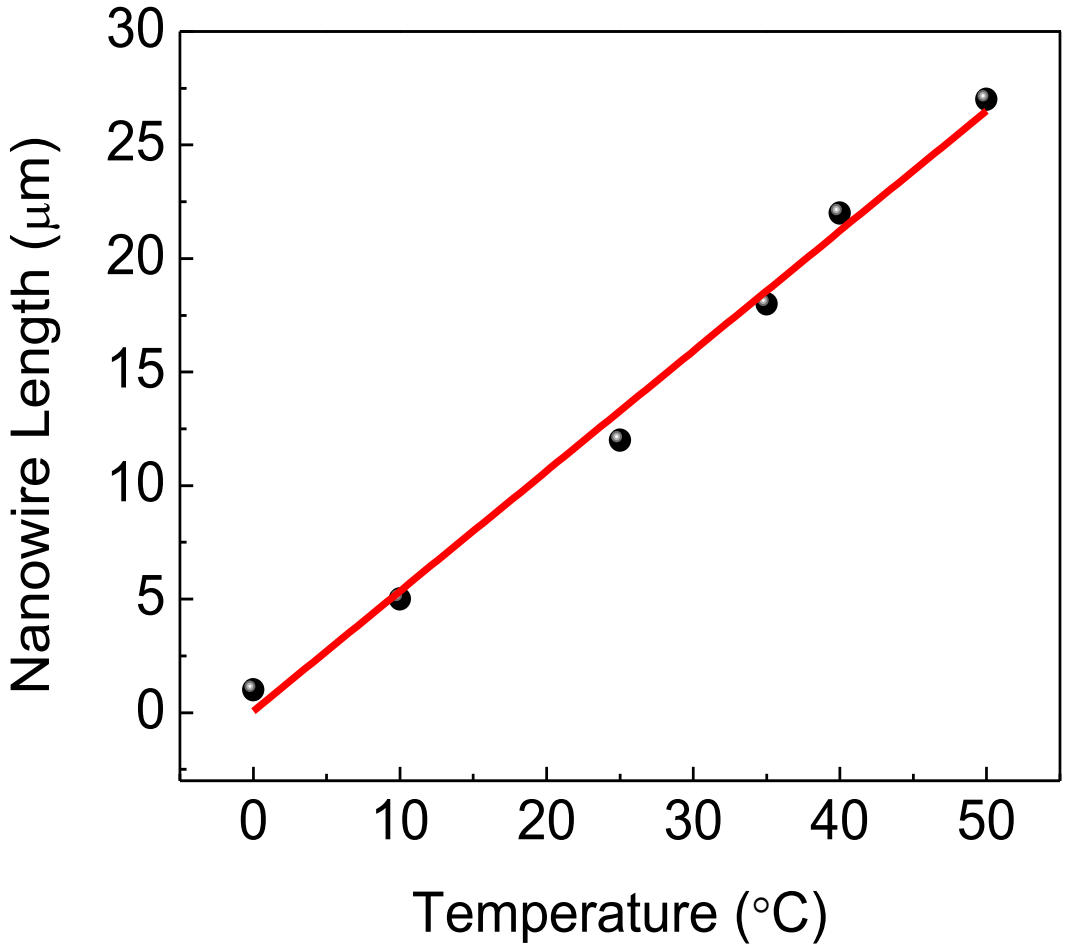


Figure 2.18. Variation of nanowire length with solution temperature.

2.4.1.4. Pressure

Nanowire fabrication by electrochemical etching experiments were conducted in teflon beakers open to atmosphere. However, carrying out this process at a high pressure was predicted to facilitate a homogeneous distribution of nanowire arrays in terms of length and alignment. Also, the electrochemical reactions were estimated to take place more rapidly resulting in longer nanowires in shorter etching durations. In order to observe the effect of pressure, a Teflon lined stainless steel autoclave (Digestion bomb) was utilized. High pressure experiments were carried out within the autoclave using a solution concentration of 0.02 M $AgNO_3$ / 4.6 M HF. During the reaction, autoclave was kept at 40°C for 40 minutes. However, in the contrary to expectations, nanowire formation could not be obtained at high pressures. Different concentrations, temperatures and durations were applied, but the resultant structures were similar to the one provided in the SEM image given in Figure 2.19. It can be

seen that instead of nanowires, randomly distributed columnar structures were obtained.

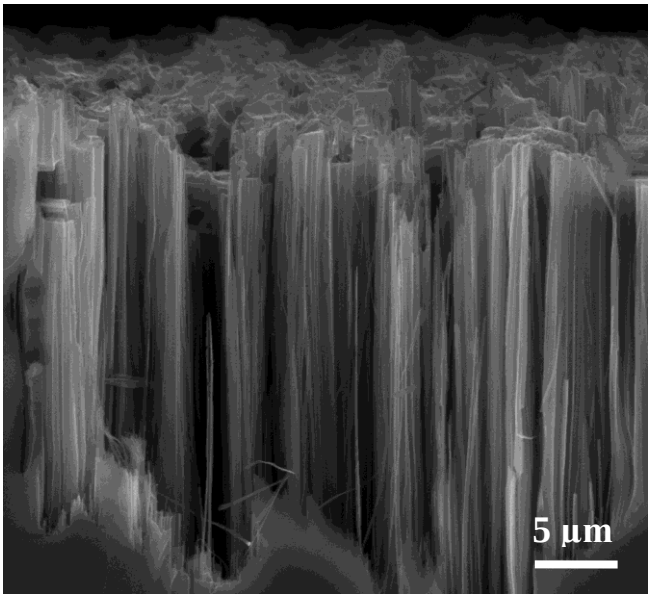


Figure 2.19. Micron-sized columnar structures obtained by high pressure experiments.

2.4.1.5. Silicon Wafer Characteristics

2.4.1.5.1. Doping Type, Crystallographic Orientation and Resistivity

The characteristics of the starting silicon substrate in terms of doping type and density, crystallographic orientation and resistivity were expected to affect the growth rate and the structure of the nanowires during the electroless etching process. This prediction was based on the idea that n-type silicon would have a larger number of electrons available at the surface and also the hole concentrations would be different. In addition, one of the previous studies [55] showed Ag nanoparticle deposition on n-type and p-type silicon substrates. It was reported that Ag distribution becomes higher for n-type silicon substrates, on the other hand Ag particle sizes become relatively larger on the p-type silicon substrates. However, as a result of successive experiments, it was determined that the EE method is almost independent to the doping type and doping level of the starting silicon substrate.

SEM images of electroless etched p-type and n-type silicon wafers are given in Figure 2.20 (a) and (b), respectively.

It was also suggested by the earlier reports that the crystallographic orientation of the monocrystalline silicon wafer changes the alignment of the silicon nanowires that are produced by EE [57]. This is investigated by etching silicon wafers with (100) and (111) crystallographic orientations under the same conditions. SEM images of the electroless etched n-type (100) and n-type (111) substrates are given in Figure 2.20 (a) and (c), respectively. The nanowire alignment was vertical in both cases; therefore, it can be said that the polished monocrystalline silicon wafers are all etched with similar reaction kinetics independent of their doping and resistivities and the nanowire alignment was found to be vertical, independent from the crystallographic orientation of the starting silicon substrates.

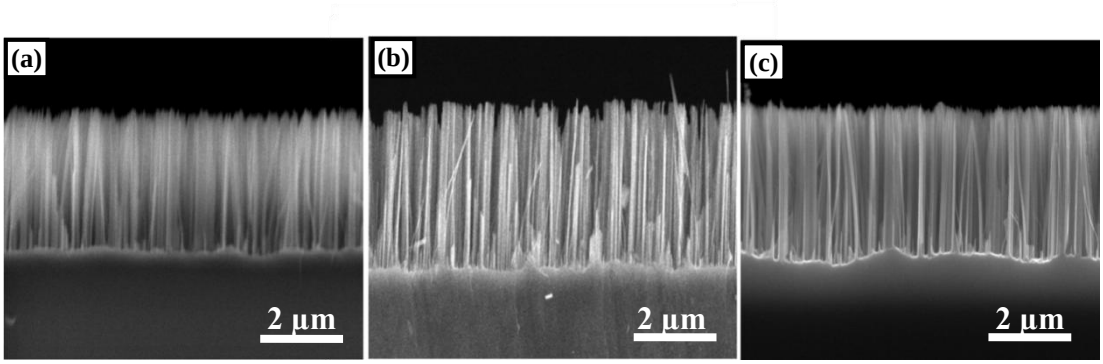


Figure 2.20. Cross-sectional SEM images of electroless etched (a) n-type (100), (b) p-type (100) and (c) n-type (111) silicon wafers having 1-5Ω.cm, 10-20 Ω.cm and 10-20 Ω.cm resistivities.

Furthermore, positioning of the silicon substrate in the electroless etching solution, whether the substrate is in a horizontal or vertical position, hung from the lid of the Teflon cup upside down or placed on a holder at a certain angle were investigated. The resultant nanowire structure was the same (vertically aligned) with very minor variations in the reaction kinetics, which were assumed to be resulted due to partially isolated interface (i.e. hanging the sample upside down from the lid of the cup may

lead to a decreased number of silver ions coming into contact with the reacting front).

2.4.1.5.2. Crystallinity

All of the reported results related to fabrication of silicon nanowires using EE method belong to etching of monocrystalline silicon substrates up to this section. In this section, the effect of crystallinity of the starting substrate was observed by comparing the morphologies of electroless etched mono and multicrystalline silicon substrates.

As it was mentioned in the previous section, etching of single crystalline substrates with any crystallographic orientation yields vertical alignment. The validity of silicon nanowire fabrication over multicrystalline wafers is also important for optoelectronic applications, since the production costs of the multicrystalline silicon wafers are relatively lower than the single crystalline ones. Furthermore, there was very limited studies that involve etching of multicrystalline silicon wafers in the literature. Cross-sectional and top view SEM images of the silicon nanowires fabricated from multicrystalline and monocrystalline silicon wafers are shown in Figures 2.21 (a) - (b) and (c), respectively. Our results demonstrate that silicon nanowire arrays can be fabricated over multicrystalline substrates through this method as well. Figure 2.21 (a) reveals that alignment and length of the nanowires are different in each grain, clearly demonstrating that the etching rate changes with crystallographic orientation associated with the different chemical reactivity of grains. On the other hand, the distribution of the nanowires and their length within each grain was found to be very homogeneous similar to the ones fabricated from monocrystalline silicon. Grain boundaries are also clearly visible in Figure 2.21 (a) and (b).

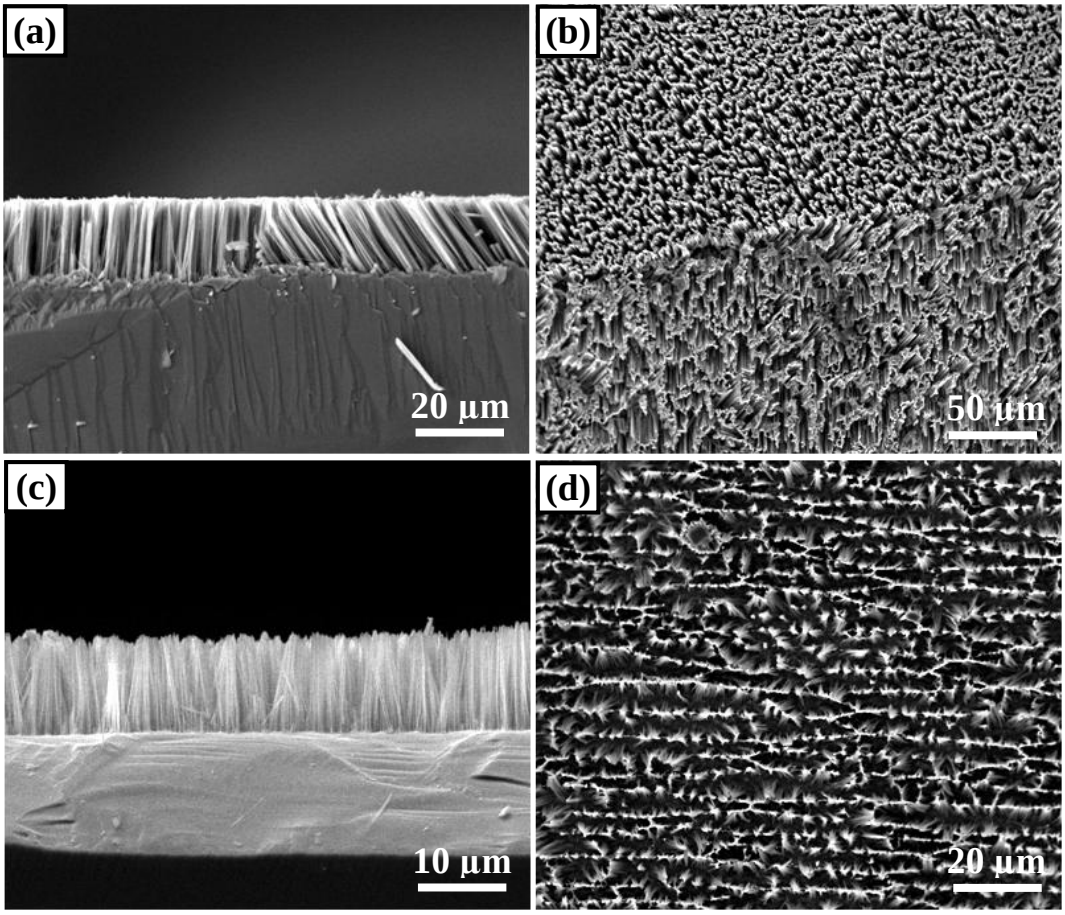


Figure 2.21. (a) Cross-sectional view and (b) top-view of multicrystalline silicon substrate; (c) cross-sectional view and (d) top-view of monocrystalline silicon substrate, electroless etched under the same conditions.

2.4.1.5.3 Polishing

The previous results of etched monocrystalline silicon wafers belong to one-side polished silicon wafers. However, especially for the photovoltaic applications, where mass production of silicon wafer based solar cells are concerned and large numbers of silicon wafers are used, unpolished wafers are generally purchased in order to decrease the cost. In a practical and realistic approach, the viability of silicon nanowire fabrication using electroless etching method should be applicable to these unpolished wafers with large areas. Considering the previously discussed etching models, these wafers were predicted to yield different alignments of silicon nanowires upon etching. Initial experiments on electroless etching of these unpolished silicon wafers resulted in nanowire formation without alignment.

Following acquiring such structures, a simple pre-treatment to obtain a smooth structure prior to electroless etching process was investigated.

Wafer sawing is used to cut silicon ingot into wafers, but induces small cracks that reduce the mechanical strength of the wafer. Also a rough surface is attained as a result of this procedure. As a common approach, acidic solutions were applied to remove saw-damage on as-cut wafers and avoid expensive lapping and polishing processes [58]. Similar to this process, a pretreatment in a potassium hydroxide (KOH) based solution was carried out for 200 μm thick, 16x16 cm p-type silicon wafers (both multi and mono crystalline) with 0.8-2.5 Ω.cm resistivities. The pretreatment solution contained 10% KOH and the treatment duration was limited to 6 minutes. The standard electroless etching procedure with various etching durations for both kinds of samples, the ones prepared with and without KOH pretreatment step, was carried out and the resultant structures were examined by SEM. In Figure 2.22 (a), (c), (e) and (f), SEM images of KOH pre-treated and electroless etched substrates are shown. The positive effect of the pre-treatment is clearly observed in these SEM images. Comparing the resultant structures of monocrystalline silicon samples, the defective structure caused by wafer sawing is visible at Figure 2.22 (b) and almost the same results obtained from polished silicon wafers is apparent at Figure 2.22 (a).

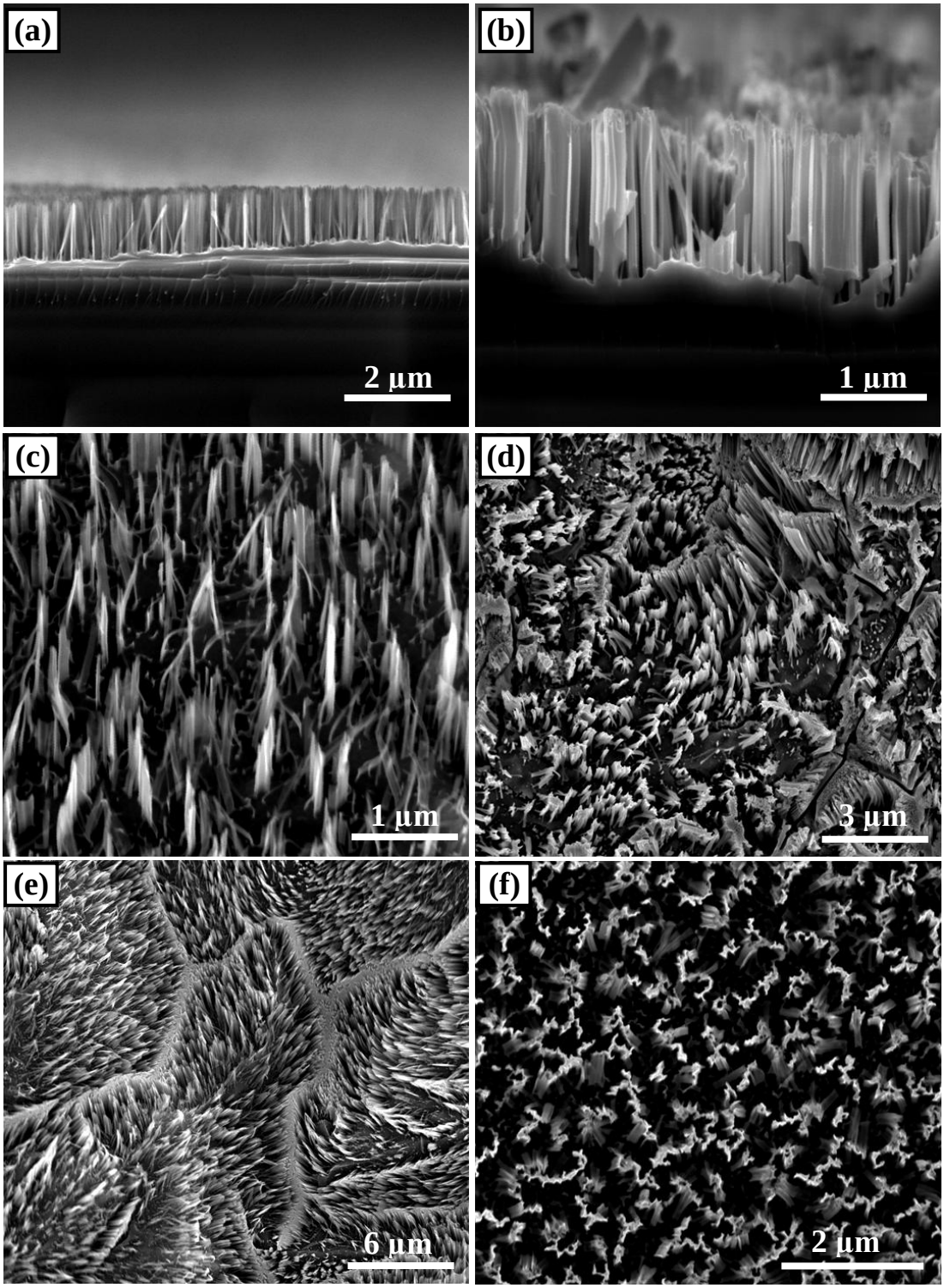


Figure 2.22. SEM images of monocrystalline samples electroless etched for 15 min., (a) with and (b) without KOH treatment. SEM images of multicrystalline samples electroless etched for 24 minutes (c) with and (d) without KOH treatment. (e) and (f) SEM images of silicon nanowire arrays fabricated after KOH pre-treatment.

2.4.1.6. Mixing, Microwave Heating and Pre-Coating

Silicon nanowire fabrication by EE is carried out within a stationary etching solution. It was predicted that mixing the solution might increase the etching kinetics, since the galvanic displacement reactions are catalyzed by Ag^+ ions coming into contact with the silicon substrate surface. The idea was to constantly regenerate the immobilized Ag^+ ions, meanwhile as-produced Ag dendrides would be removed away from the interface accelerating the etching rate. A step motor attached to Teflon blades was mounted in the middle of the lid of the Teflon cup and the standard EE procedure was followed. However, these experiments were not successful as a nanowire structure could not be obtained. It is believed that instead of donating new ions, this mixing mechanism removed the reacting Ag^+ ions away and inhibited the etching process.

There are several reports on the synthesis of nanostructures by microwave heating. Carbon nanotubes and ZnO nanowires have been reported to be produced very rapidly in a microwave [59,60]. Electroless etching method was suitable to be carried out in a commercially available microwave oven (2.45 GHz) as it only involves an etching solution prepared inside a Teflon cup. In order to prevent excessive HF evaporation, which would lead to changes in solution concentration, the power of the microwave oven was kept low. Samples were etched inside a microwave oven for 5 and 10 minutes, at powers adjusted to 100 Watts and 200 Watts. Similar to the effect of mixing the solution that was discussed previously, nanowires could not be produced by microwave heating.

In the earliest studies with an intention of fabrication of silicon nanowires, a two step process was often used consisting of thin film coating of a noble metal on the silicon surface as the first step and EE as the second step. Several researchers continued to work with this method even after the development of the single step process, EE. In the recent reports, utilizing EE of the coated wafers, Ag was often preferred as the coating material and HF/H_2O_2 solution as the etching solution [61,62]. In this thesis, this mechanism was also investigated and the resultant structure of this process was compared to the ones obtained by EE process. Ag coating was carried out using both

sputtering (deposition rate of 0.5 kÅ/sec with an overall film thickness of 20 nm) and solution based methods ($AgNO_3$ / HF solution). For the latter procedure, approximately 10 nm thick Ag coating was achieved by immersing the silicon wafer into the solution containing 4.6 M HF and 0.02 M $AgNO_3$ for 1 minute. Both samples were then immersed in a solution containing 5M HF and 0.5M H_2O_2 at 40°C for 40 minutes. Although a very homogeneous structure was obtained, the silicon nanostructures are not standing as individuals. The SEM images are provided in Figure 2.23 for those samples. It is clear that rather than individual nanowire arrays, columnar structures were obtained. Also, in accordance with the previous reports [63], higher etching rates were obtained using this process compared to the single step etching, due to the availability of Ag particles around the reacting front and efficient hole injection from the etchant.

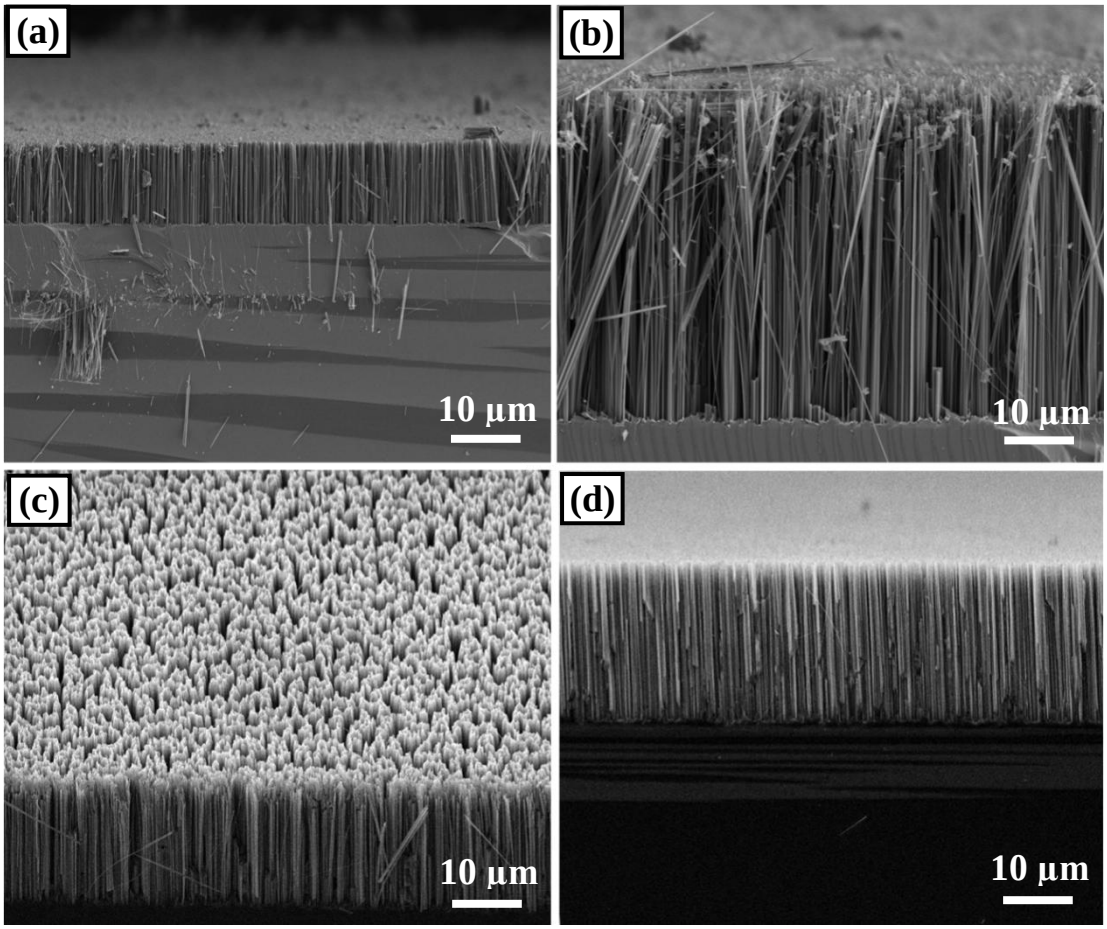


Figure 2.23. Cross-sectional and oblique-view SEM images of the silicon wafers etched using two-step electrochemical etching procedure.

2.4.2. TEM Analysis of Silicon Nanowires Fabricated by Electroless Etching

TEM characterization was carried out in order to examine silicon nanowire surfaces. It was observed that most of the nanowires have very smooth surfaces with almost no change in diameter from tips to the middle sections. These smooth surfaces prove that selective etching took place and the reduction-oxidation reactions did not affect the side walls of the nanowires. However, there are also a few nanowires with rough surfaces present in the TEM sample. This could mean that at certain local points, either presence of impurities changed the reaction dynamics or nitric acid, which is used for silver dendride removal, damaged nanowires due to its high concentration.

TEM image of silicon nanowires in Figure 2.24 (a) proves that electroless etched, vertically aligned silicon nanowires could be scraped off and used for applications requiring horizontal networks. It is apparent that almost all nanowires have very smooth surfaces. Electroless etching does not allow a precise control over the silicon nanowire diameter, although silicon nanowire alignment, distribution and lengths are well controlled. The resultant silicon nanowire diamaters are generally in the range of 25-250 nm range, also confirmed by Figure 2.24 (a) and (b).

The high resolution TEM (HRTEM) image in Figure 2.24 (c) shows that a thin oxide layer was formed on the surface of silicon nanowires and the selected area diffraction pattern, available at the inset provides the crystallographic information of silicon nanowires. The crystal structure of silicon nanowires was found as diamond cubic. As a consequence of using a top down silicon nanowire fabrication method, the crystal structures of nanowires are the same as their bulk counterparts. Also [100] nanowire growth direction was obtained, which supports the vertical alignment of as-grown silicon nanowires over a silicon substrate having (100) crystallographic orientation.

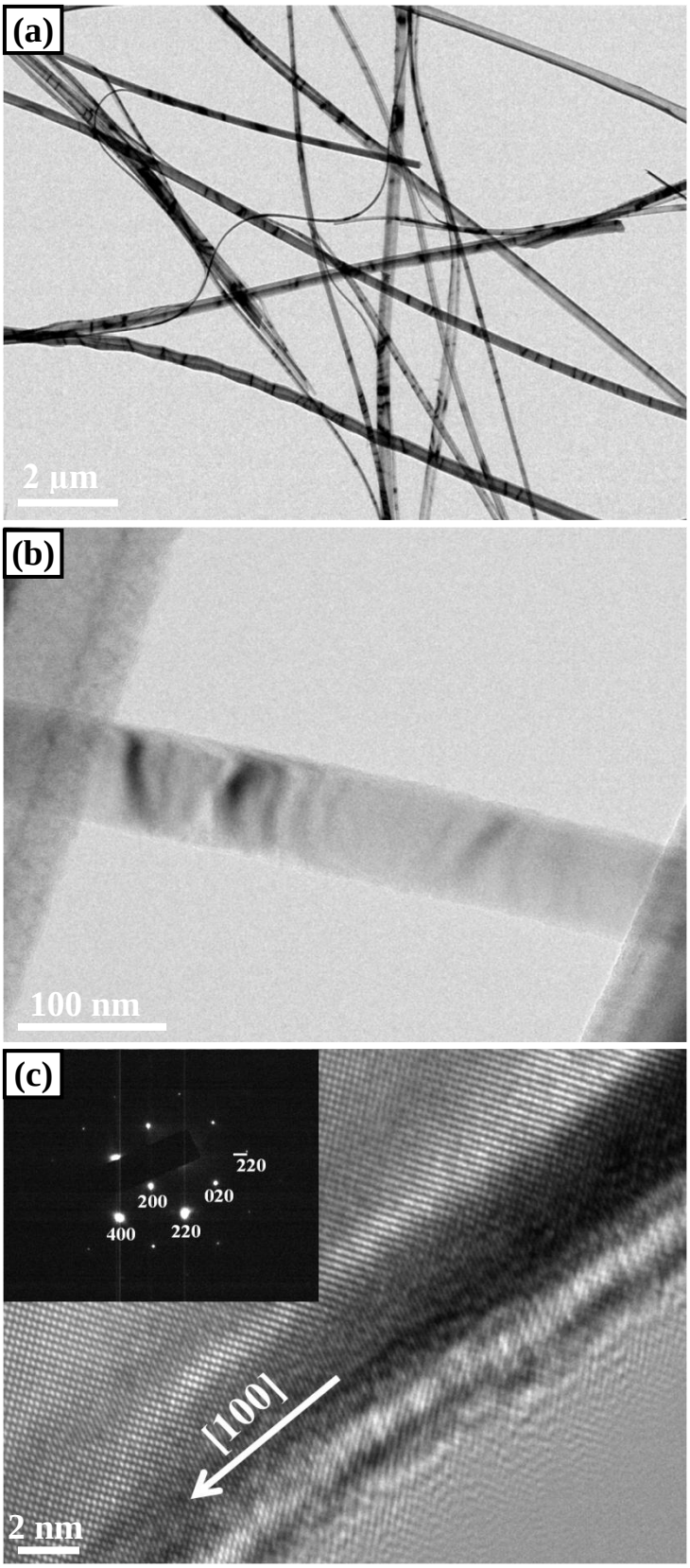


Figure 2.24. TEM image of silicon nanowires with various diameters at (a), an individual silicon nanowire with smooth surface at (b), HRTEM images of the nanowires in (c) and (d). Inset reveals the selected area diffraction pattern of the silicon nanowires.

2.4.3. Optical Reflectivity of Silicon Nanowires Fabricated by Electroless Etching

One of the most important features of silicon nanowire arrays is their unique and remarkable antireflective properties. Photographs of the silicon substrate before and after silicon nanowire fabrication are given in Figure 2.25. The shiny and reflective grey colored surface of the substrate turned into black and dull following the fabrication of silicon nanowire arrays. Reflectivity measurements of the bare silicon wafer compared to silicon wafers with different lengths of silicon nanowire arrays are given in Figure 2.26. This graph proves that silicon nanowire arrays fabricated by EE method significantly decrease the reflectivity of the starting substrate over a wide spectral bandwidth. The reflectivity was measured as low as 1.16% with 10 μm long nanowire arrays. These measurements were carried out on the samples, which were produced by electroless etching process with a solution concentration of 4.6M HF, 0.02M $AgNO_3$ processed at 40 °C for different etching times. Reflectivity of these samples, measured at a wavelength of 500 nm, with respect to the nanowire length is plotted in Figure 2.27. A sharp decrease in reflectivity with nanowire length was observed up to a nanowire length of 10 μm. These results are consistent with the previous studies focused on silicon nanowire length dependency on reflectivity [64]. However, this work has been further extended in this thesis and the reflectivity values of longer silicon nanowires were also investigated. Further increase in the nanowire length revealed a slight increase in the reflectivity of the samples. This could be due to the bundle formation which decreases the uniformity of the distribution of nanowires, increasing the void space. As indicated before, silicon nanowire arrays transforms into bundles with increased nanowire length as shown in the top view SEM images given in the inset of Figure 2.27. The sample with 10 μm long nanowire arrays revealed the strongest light trapping mechanism [65,66] due to its higher nanowire density, small void space and homogeneously distributed arrays, giving the best antireflective performance.

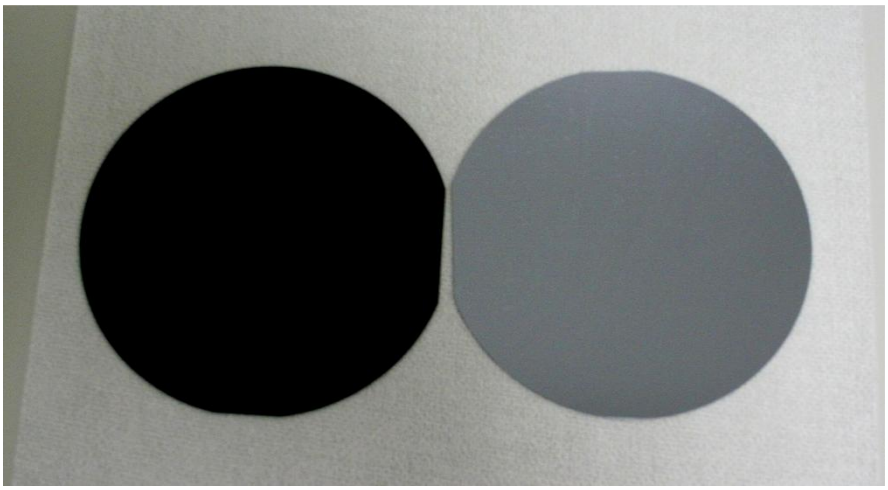


Figure 2.25. Photograph of 7.5 cm silicon wafer before (on the right) and after (on the left) silicon nanowire array fabrication by electroless etching.

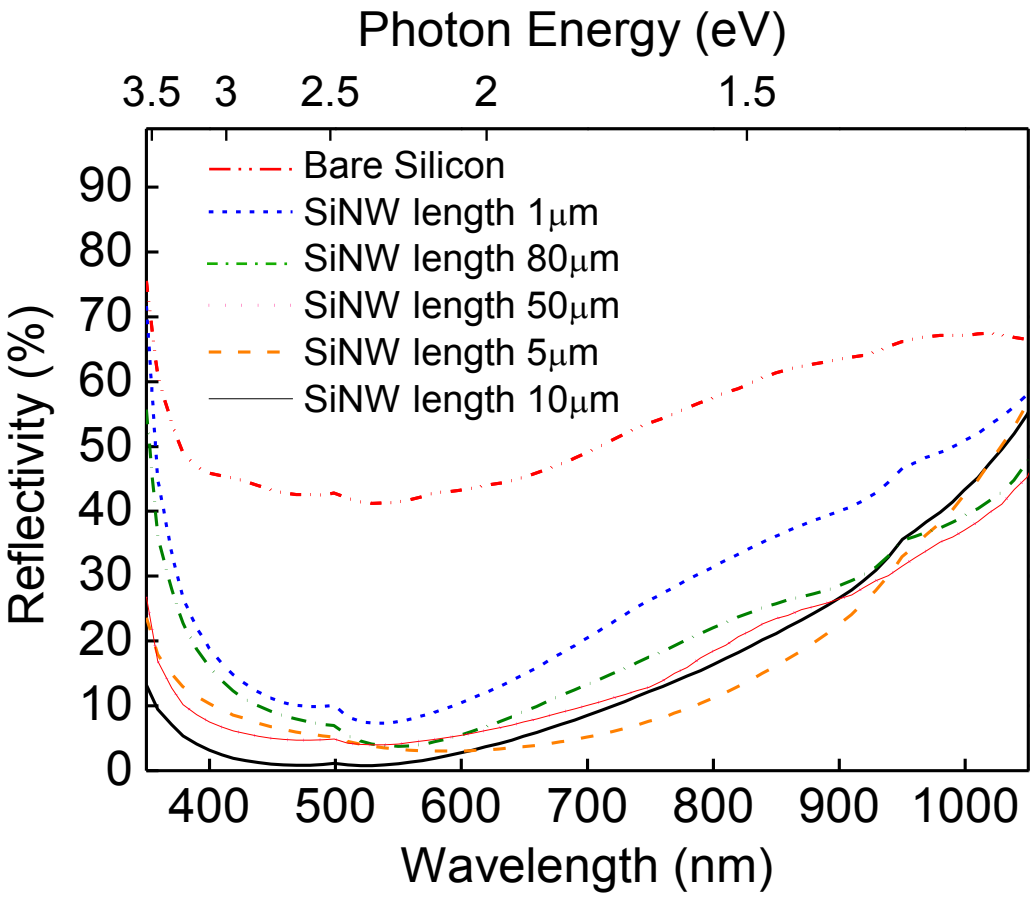


Figure 2.26. Optical reflectivity measurements of bare silicon and silicon samples containing various lengths of silicon nanowire arrays in a 350-1050 nm spectral bandwitdth.

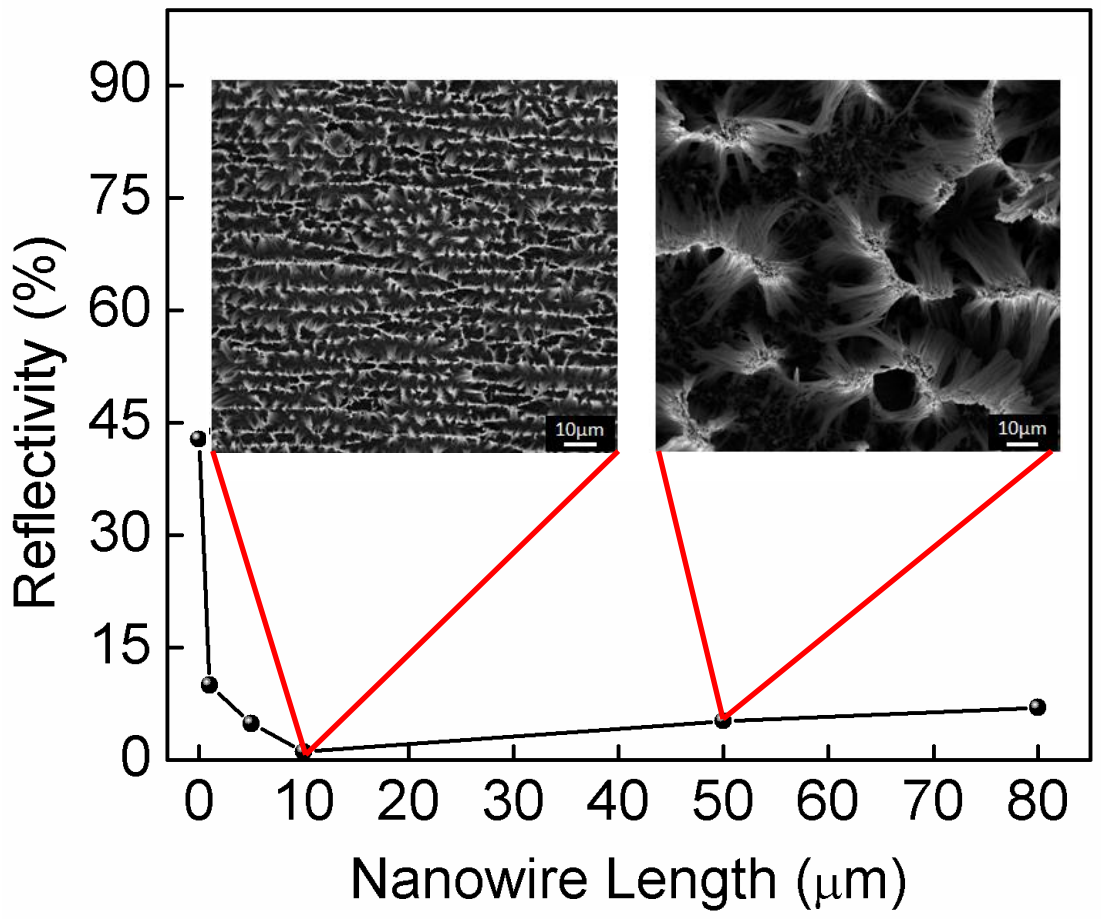


Figure 2.27. Nanowire length dependent reflectivity values (measured at 500 nm) Inset shows the relative top-view SEM images of corresponding silicon nanowires.

The absorption enhancement phenomenon has been studied for many years and one of the important methods is to increase the total internal reflection of the systems by texturing the surface of the semiconductor. The studies behind this idea also led research groups to work with nanowire / nanorod structures to achieve maximum light trapping and absorption. Total internal reflection term is simply the integral of the energy transferred by the incoming photons via the scattering events taking place at the surface or inside the medium. Maximum achievable absorption of light for a planar sheet absorber ideally uses random Lambertian light trapping mechanism [67]. It was found that the nanowire array's absorption exceeds the planar light trapping limit and this behavior exemplifies a useful property of nanostructured non-planar absorber geometries. In that, they can achieve greater absorption per material volume than achievable by any textured surface [68]. Thus, silicon nanowire array geometry

exceeds the theoretical absorption limit and forms a fully light absorbing layer, especially in the photon energies near the band gap of the absorber [65].

The large area applicability and this remarkable antireflective property of silicon nanowires reveal their potential to be utilized in solar cell applications. The photographs of bare, antireflective nitrate layer coated and silicon nanowire containing multicrystalline silicon wafers are presented in Figure 2.28 (a)-(c), respectively. In order to decrease the reflectivity losses, antireflective coating is generally applied on standard crystalline silicon solar cells. The most widely used antireflective material is silicon nitrate (Si_3N_4) giving the navy blue color to the surface. These thin film antireflective layers are deposited by a plasma enhaced chemical vapor deposition (PECVD) system at high temperatures (200-400 ^{o}C) depending on the coating material. This costly process can be avoided when silicon nanowire arrays, already displaying remarkable antireflective properties, are fabricated on the surface of the solar cells.

Figure 2.28. (a) Bare multicrystalline silicon (mc-Si) wafer, **(b)** mc-Si wafer with anti-reflective coating, **(c)** mc-Si solar cell with silicon nanowire arrays.

2.4.4. Field Emission Characteristics of Silicon Nanowires

Following the breakthrough discovery of carbon nanotube field emitters, field emission (FE) characteristics of silicon nanowires have also been investigated and studies to develop more efficient and simple processes have drawn attention. Different geometries of silicon nanowires could be formed using various methods as mentioned previously and it is known that the geometry is one of the most important factors, directly affecting the field emission characteristics of the system. Milne et. al. provided a study on the effect of tip shapes of carbon nanotubes on their field emission characteristics and according to their study, the best field emission characteristics is attained for vertically standing rounded-whiskers [69]. The effect of different nanowire diameters on the field emission characteristics have also been investigated and lower turn on voltages were obtained for smaller diameters [7]. Both vertically standing arrays and horizontal networks of silicon nanowires formed by VLS method were investigated as field emission sources [70,71]. Among those systems, vertically standing silicon nanowires displayed relatively improved FE characteristics. Furthermore, the effects of multiwalled carbon nanotube deposition, nanowire orientation and post treatments were reported on the performance of silicon nanowire field emitters [72]. In these studies, silicon nanowire arrays were produced using a two-stage etching procedure involving Ag coating of the silicon substrates and etching in a H_2O_2/HF based solution. However, as the resultant silicon nanostructures constitute morphologies similar to thin films, screening effect of the neighboring silicon nanowires was dominant and the field emission results were not as good as the ones obtained by VLS method. In this thesis, silicon nanowires were fabricated by EE method, yielding individually standing nanowires to decrease the screening effect and to provide an alternative to VLS-produced silicon nanowires. Also the effect of nanowire length on FE characteristics was investigated.

Silicon nanowires were fabricated using etching solutions of 0.02 M $AgNO_3$ and 4.6 M HF at 40°C. Etching durations were 20, 40 and 240 minutes, corresponding to the nanowire lengths of 5, 10 and 70 μm, respectively. The emission field dependent current density measurements are shown in Figure 2.29. As expected, following the turn on field value, the emission current density increases exponentially with the

applied emission field. The term, turn-on field, represents the degree of emission field necessary to be applied in order to obtain a certain current level. A material with relatively low turn on field points out its strength as a field emitter. Here in this study, the turn on field was defined as the electric field required to produce a current density of 10 μA cm^{-2} in order to compare these results with the previous reports. The turn-on fields of 5, 10 and 70 μm long silicon nanowire arrays were obtained as 5.08, 2.73 and 2.2 V/μm respectively. These results, especially the turn on field of 70 μm long silicon nanowires are comparable and lower than those reported in the literature concerning silicon nanostructures with similar morphologies [61,72-75]. The field emission properties of 70 μm long silicon nanowires were much better compared to the ones obtained from shorter nanowires, as shown in Figure 2.29. Much higher current density levels were attained with increasing emission field.

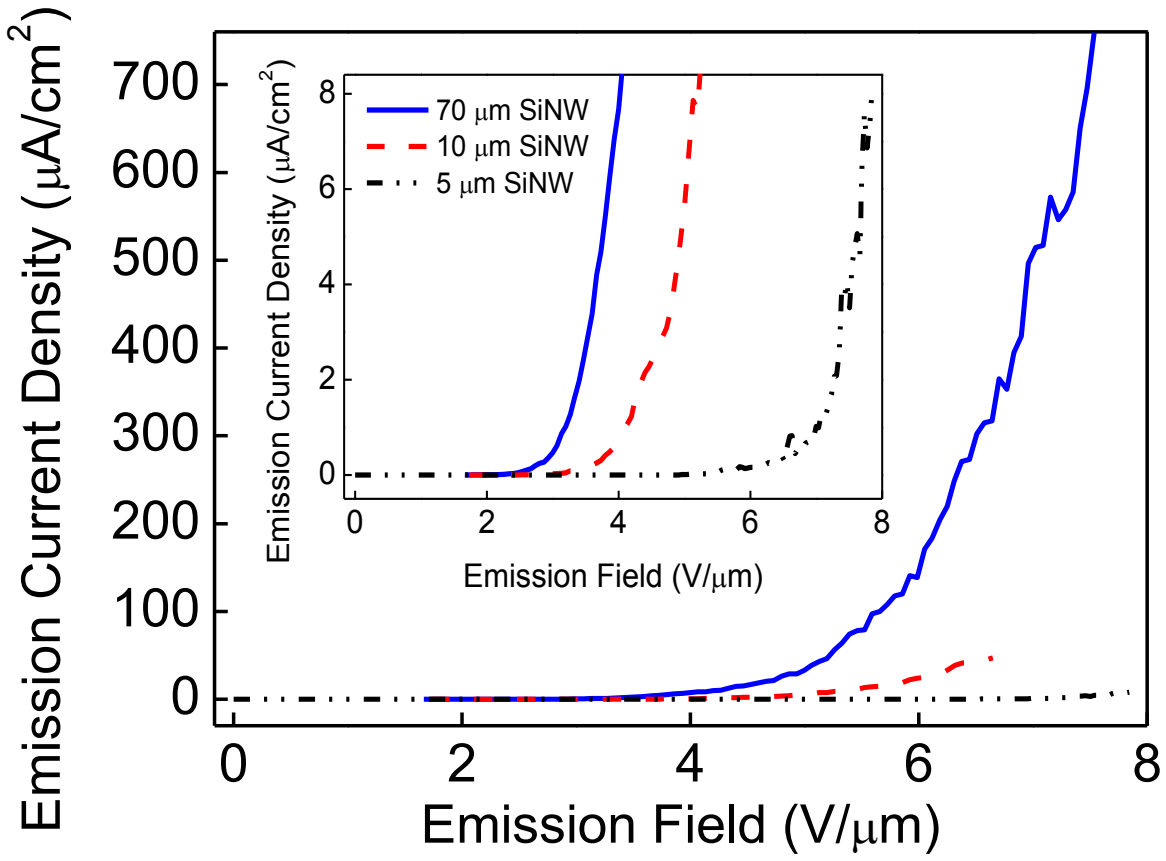


Figure 2.29. Emission field dependent current density values for 5, 10 and 70 μm silicon nanowire arrays. Inset shows the magnified portion of the lower emission current densities.

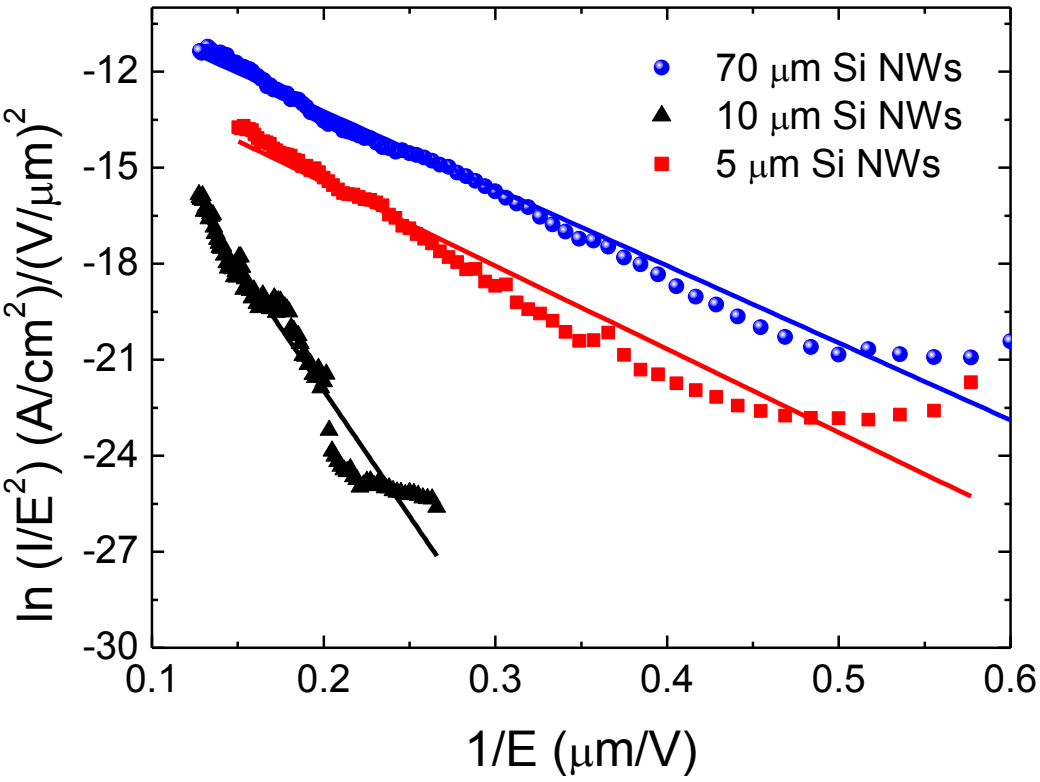


Figure 2.30. Fowler-Nordheim fit of the emission field dependent current density.

The field emission enhancement is generally analyzed using the Fowler– Nordheim (FN) equation;

$$ln\left(\frac{J}{E^2}\right) = ln\left(\frac{A\beta^2}{\emptyset}\right) - \frac{B\emptyset^{3/2}}{\beta E} \qquad (2.6)$$

where A and B are constants equal to 1.54×10^{-6} A eV V^{-2} and 6.83×10^{3} V μm^{-1} $eV^{-3/2}$, respectively. J is the current density, E is the applied field, and ϕ is the work function of the emitting material, which is 3.6 eV for silicon [7], β is the field-enhancement factor, which is related to emitter geometry, crystal structure, vacuum gap and spatial distribution of the emitting center. From the slope of Fowler-Nordheim graphs, given in Figure 2.30, the field enhancement factors (β) of the

samples were calculated as 582.522, 1618.657 and 1780.52 for nanowire lengths of 5, 10 and 70 μm, respectively. These results prove that enhanced field emission characteristics were displayed for relatively longer silicon nanowires and in addition, these vertically aligned silicon nanowires fabricated by EE method have great potential to become a cost effective alternative to current field emitters.

Stability and lifetime of the field emitters is another important factor. Emission stability of silicon nanowires was monitored by maintaining an electric field of 5.65 V μm^{-1} over a period of 10000 seconds and the results are shown in Figure 2.31 for three different nanowire lengths. No obvious emission current degradation or noticeable fluctuation was observed during this period, again revealing potential of silicon nanowire arrays fabricated by EE method as a field emitter.

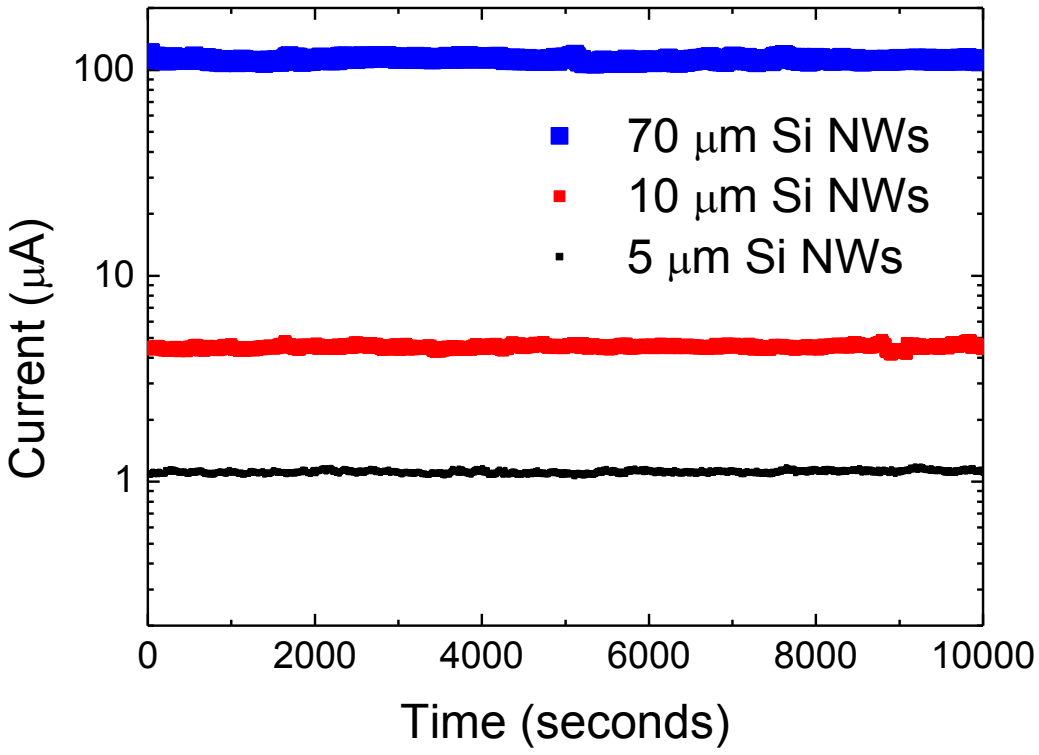


Figure 2.31. Emission current stability of silicon nanowires.

CHAPTER 3

SILICON NANOWIRE / PEDOT:PSS HETEROJUNCTION SOLAR CELLS

3.1. Introduction

3.1.1. Historical Survey

The photovoltaic effect was first observed by Becquerel in 1839. He discovered that a photovoltage forms upon the exposure of light on an electrode in an electrolyte solution. Following this discovery, in 1877 Adams and Day encountered a similar phenomenon in solid selenium. Following these occasions, subsequent efforts were devoted to this subject and in 1954 the modern era for photovoltaics began with the first single crystal silicon solar cell having 6 % efficiency, demonstrated by Chapin et. al. in Bell Laboratories. The silicon based solar cells have become the research model of all homojunction solar cells. In 1950s and 1960s, photovoltaic technology was mostly used for spacecraft applications. The first spacecraft to use solar panels was the US satellite "Vanguard 1", launched in March 1958 with solar cells made by Hoffman Electronics. This milestone created interest in producing and launching a geostationary communications satellite, in which solar energy would provide a viable power supply. This was a crucial development which stimulated funding from several governments into research for improved solar cells [76]. Then all-thin-film heterojunction solar cells were developed in 1980s with less material usage. This is followed by the addition of organic photovoltaics and dye sensitized solar cells into the equation, providing cost-effective production mechanisms, opening a new era of excitonic solar cells. The solar cell industry has rapidly evolved and completely new concepts have been designed, aiming higher efficiencies and lower production costs. The highest efficiency belongs to a multi-junction tandem solar cell, reported as 42.8 % in 2007 from University of Delaware [77].

3.1.2. The Current Status of Solar Cell Technology

Solar cells are optoelectronic devices which directly convert sunlight into electricity. According to many scientists, one of the most realistic ways to respond to the increasing energy demand of the world in the future will be photovoltaic technology. It is well known that the solar energy, irradiated onto the earth in a few hours, is more than enough to supply the annual energy need of the entire population. Based on this fact, solar energy is often termed as an infinite energy source. Furthermore, besides being a free energy source, there are also other critical facts for the growing interest in photovoltaic conversion, such as global warming and pollution. The pie chart in Figure 3.1 shows the energy consumption percentages of major energy resources [78]. According to this data, more than 80% of the overall energy is supplied by coal, oil and gas. These are fossil fuels, threatening the world's atmosphere by producing greenhouse gases as the products, which lead to global warming, major pollution and health problems. Moreover, fossil fuels are not renewable meaning that once they are burned, they can not be recovered. Therefore, they will eventually come up short to provide sufficient energy as these inverse trends of the world's tremendously increasing energy demand and depletion of fossil fuel deposits continue. As a consequence of these considerations; solar cells with various advantages compared to the other renewable energy resources will become one of the primary technologies. The bar chart in Figure 3.2 demonstrates the already growing potential of solar cell technology as the energy production has shown an exponential increase over the past decade.

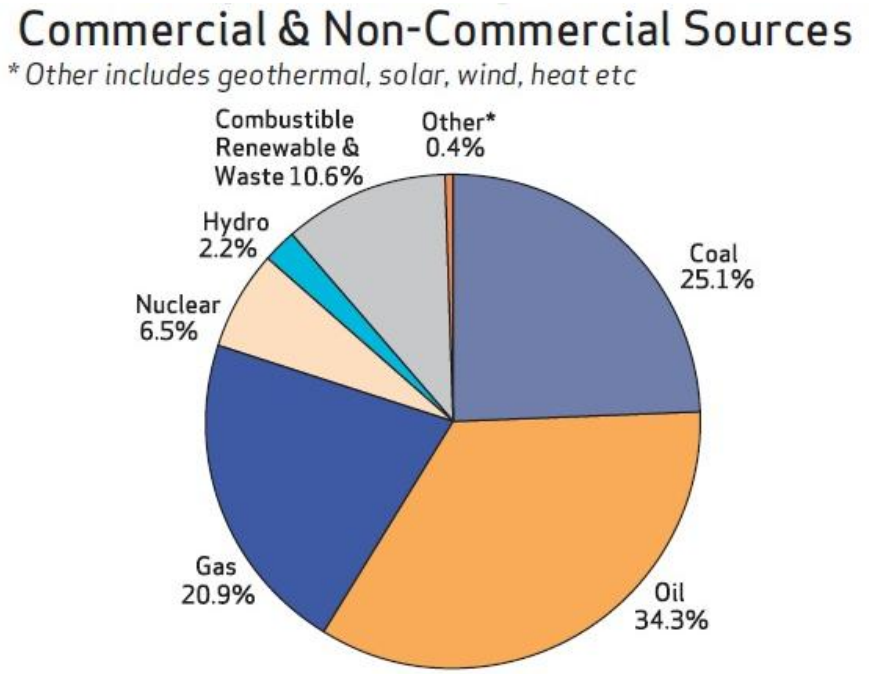


Figure 3.1. The pie chart revealing the role of each energy resource by their energy percentages over the total energy supplied [78].

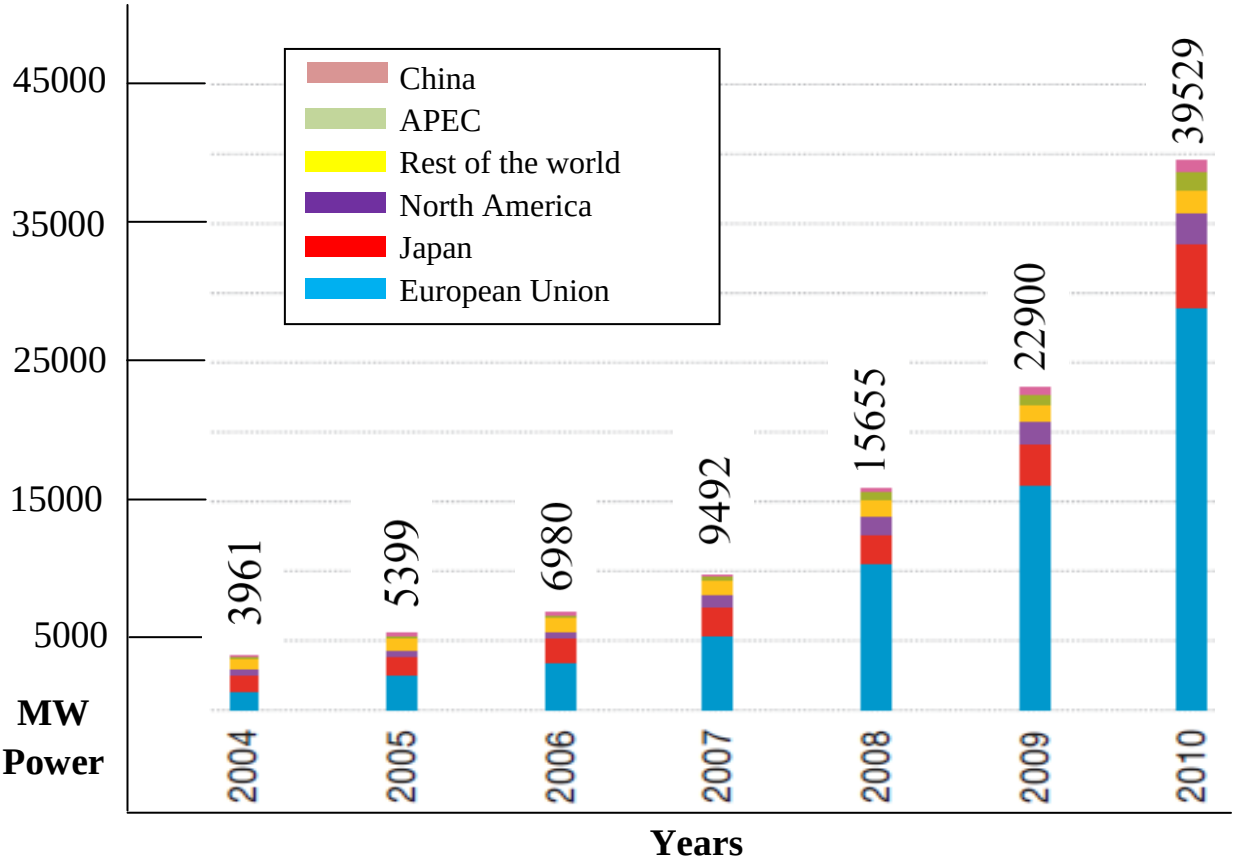


Figure 3.2. Historical development of global cumulative PV power installed per region [79].

Although intensive efforts have been given in laboratory scale research to produce various solar cell models using different material types, only commercially available solar cells are the first two generations, crystalline silicon and thin film solar cells. Organic solar cells are still suffering from the low efficiencies and low life spans, while the other types of solar cells such as III-V semiconductor (GaAs) solar cells and multijunction tandem solar cells have high material and production costs. The cost-efficiency and commercial availability of different photovoltaic technologies are compared in Figure 3.3. It can be said that the most feasible and cost effective solar cells are still crystalline silicon solar cells.

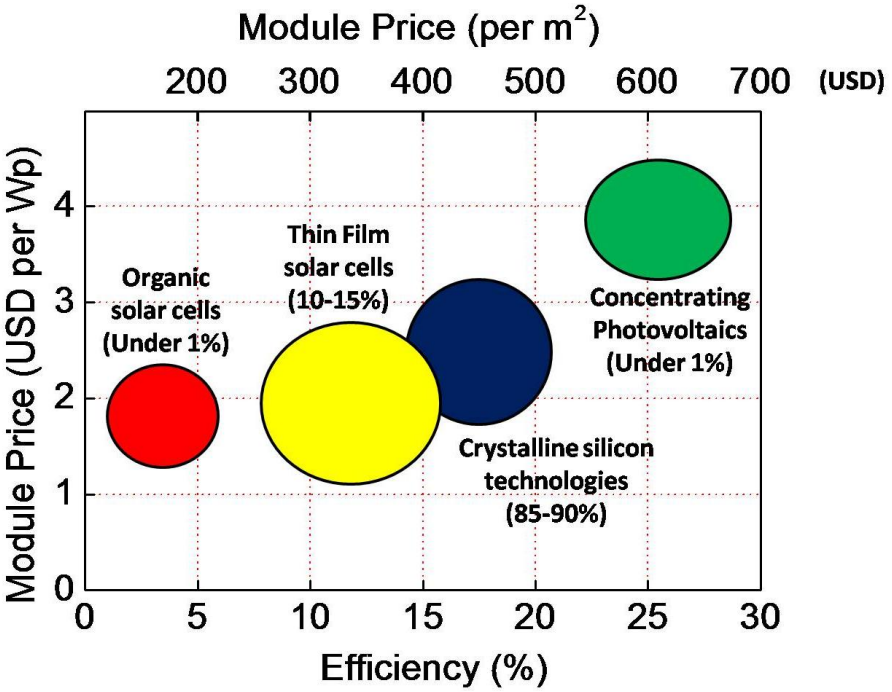


Figure 3.3. Performance and cost comparison of commercially available photovoltaic technologies [80].

3.1.3. Solar Cell Characteristics

Solar cells are optoelectronic devices consisting of p and n-type semiconducting materials. In a typical solar cell, incident light excites electrons from valence band to conduction band and generates electron-hole pairs. Photogenerated electrons (in the

n-type) and holes (in the p-type) diffuse to the p-n junction. Then they are swept away by the built in electric field across the junction and collected in the respective contact metals. Therefore the electrons enter the external load and generate photo-generated electrical current. In this part of the thesis, basic parameters of the solar cells are introduced.

3.1.3.1. Solar Spectrum

The sun is a complex radiator whose spectrum can be approximated by a 6050 ºK blackbody. Figure 3.4 shows the solar spectrum outside and inside the atmosphere. Solar irradiation reaching earth's surface, which is $1.5x10^{11}$ meters away from the sun, is about 1350 W/m^2.

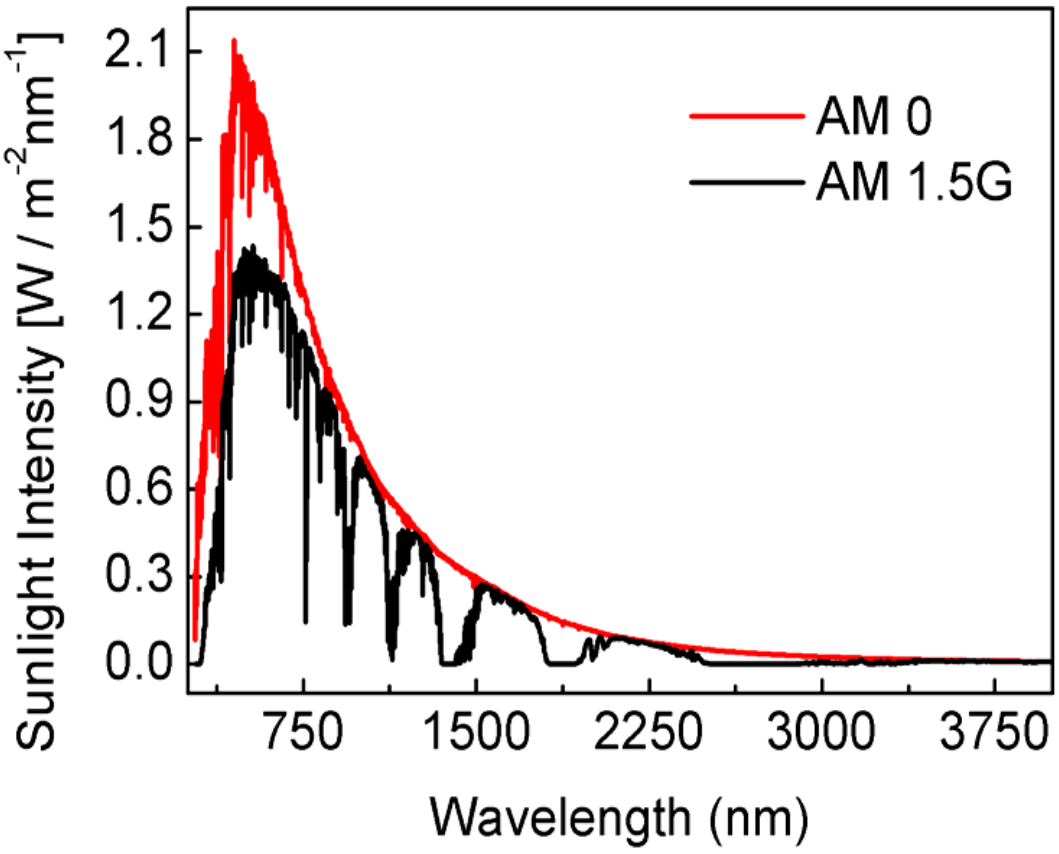


Figure 3.4. AM 0 and AM 1.5G solar spectrum [81].

On its way through the atmosphere, the sunlight is modified by three major processes:

1) Rayleigh scattering, which is responsible for the blue color of the sky,

2) Absorption due to oxygen, carbon dioxide, water and ozone,

3) Scattering by aerosols or particulate matter.

"AM 1.5G" indicated on the graph is an abbreviation for "air mass 1.5 global". This is a standard figure of merit used for solar testing, characterization and simulation. Air mass is the amount of distance travelled by sunlight within the atmosphere which clearly depends on the angle of incidence. Also 1.5 corresponds to the angle at which the height of an object is equal to the length of its shadow. For instance, in AM 1.5G conditions this angle becomes 48.2 °. The general formula for AM calculations is;

$$AM = \frac{1}{\cos\,\theta} \tag{3.1}$$

, where θ is the angle between incident light and the vertical (normal) of the surface.

3.1.3.2. Solar Cell Parameters

Solar cell efficiency, η, is defined as the ratio of electrical power out (at an operating condition of maximum power output), P_{out}, divided by total optical power in, P_{in}, typically under AM 1.5G illumination at an intensity of 100 W/cm^2,

$$\eta = \frac{Pout}{Pin} \tag{3.2}$$

$$\eta = \frac{\text{Voc} \times \text{Jsc} \times \text{FF}}{Pin} \tag{3.3}$$

,where the open-circuit voltage (Voc) is the voltage or bias across the cell at zero current level, the short-circuit current density (Jsc) is the current density at zero applied bias, and the fill factor (FF) is the ratio of the maximum electrical power output to the product of Voc and Jsc. The maximum power point is the point at which the product of current and voltage is maximum, which is illustrated in Figure 3.5. FF is expressed with the following formula;

$$FF = \frac{Imax \times Vmax}{Isc \times Voc} \tag{3.4}$$

Considering a solar cell as an ideal diode in parallel with a pure light-generated current source leads to the following expression for current generation in a planar pn junction solar cell [82]:

$$J = J_{sc} - J_0 \left[\exp\left(\frac{qV}{k_B T}\right)\right] - 1 \tag{3.5}$$

This in turn leads to the following expression for Voc:

$$V_{oc} = \frac{k_B T}{q} ln \left[\frac{J_{sc}}{J} + 1\right] \tag{3.6}$$

,where q = 1.602193×10^{-19} C is the magnitude of the electronic charge, k_B = 1.38073×10^{-23} m^2 kg s^{-2} K^{-1} is Boltzmann's constant, the temperature T is assumed to be 300 K and J_0 is the saturation current density. V_{oc} could also be treated as the potential difference between the components of the p-n junction generated as a result of different energy band states. According to these expressions, the solar cell efficiency is supposed to increase logarithmically with incident power. However, there is an upper boundary induced by the thermal effects and efficiency losses. Therefore, the optimum conditions are present at a finite power input level.

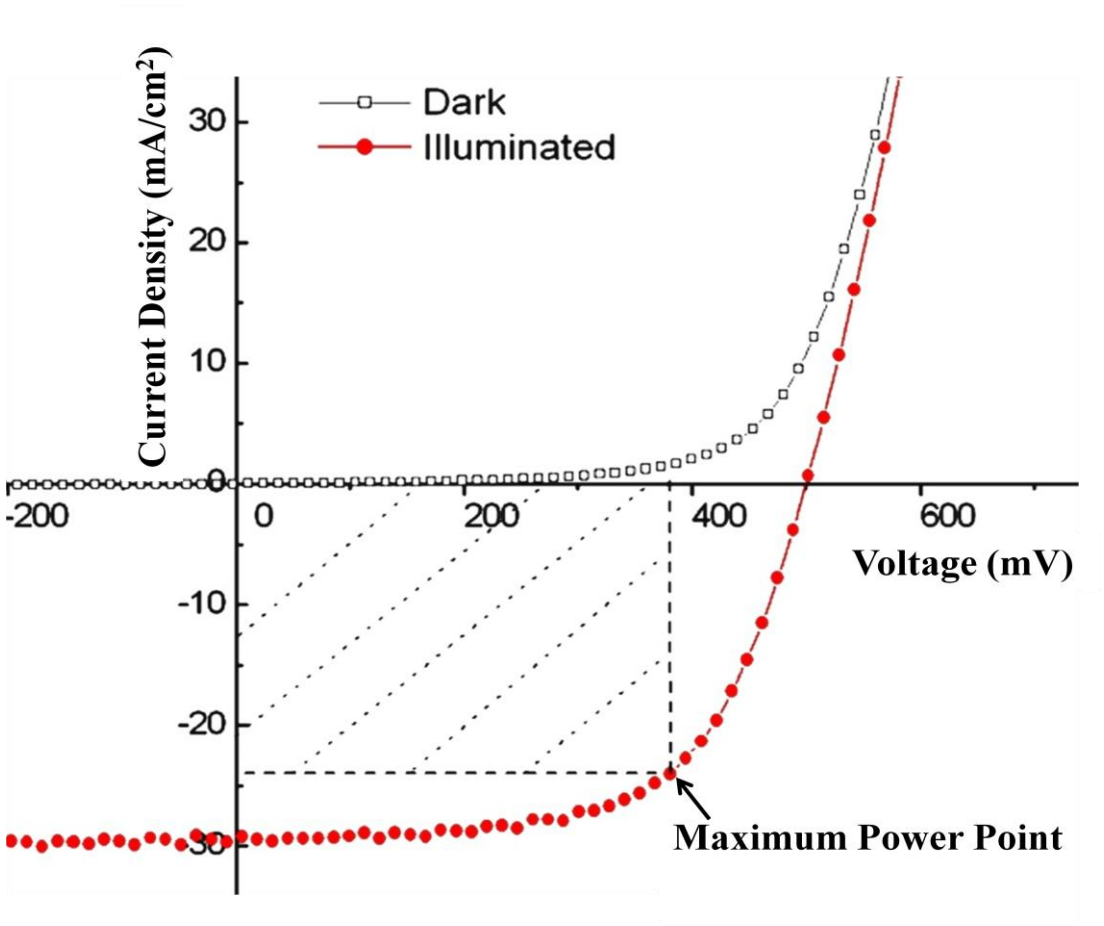


Figure 3.5. Typical current-voltage curve of a diode in dark and illuminated condition. Shaded area represents the maximum power generated by the diode [83].

Two other significant parameters of the solar cell that can be extracted from current-voltage curves are series (Rs) and parallel (shunt, Rsh) resistances. Their effects on the solar cell parameters can be derived from the equivalent circuit model of a solar cell, as shown in Figure 3.6.

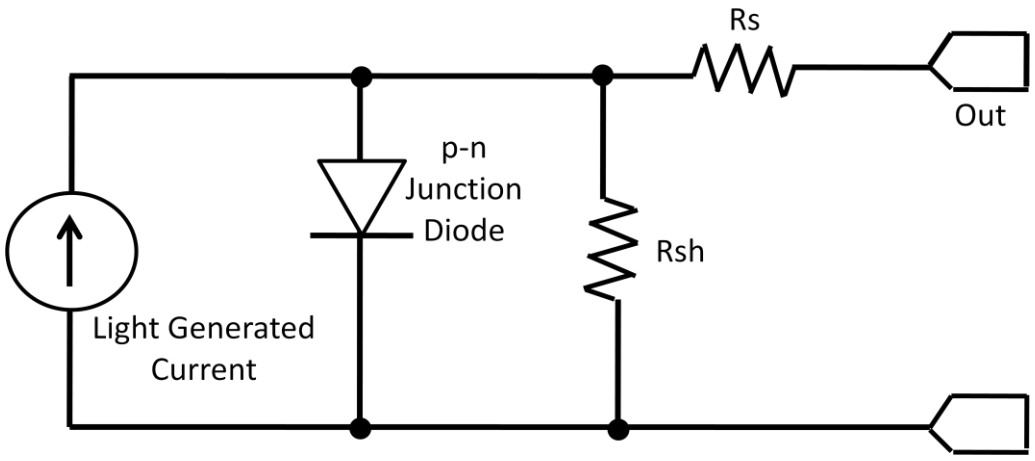


Figure 3.6. Equivalent circuit model of a solar cell.

Series resistance in a solar cell has three causes; firstly, the movement of current through the emitter and base of the solar cell; secondly, the contact resistance between the metal contact and the semiconductor; and finally the resistance of the top and back metal contacts. The main impact of series resistance is reduction of the fill factor, although excessively high values may also reduce the short-circuit current. Low shunt resistance causes power losses in solar cells by providing an alternative current path for the light-generated current. Such a diversion reduces the amount of current flowing through the solar cell junction and reduces the voltage from the solar cell [84]. For an efficient solar cell, Rsh would be much larger than Rs. Since the effect of Rsh is negligible near short circuit current conditions, the slope of the current-voltage curve in that vicinity indicates Rs. Conversely, the effect of Rs is negligible in the vicinity of open circuit voltage, the slope of the curve at that point shows the Rsh value. The expressions of Rs and Rsh are as follows:

$$R_s = \left.\frac{1}{\frac{dI}{dV}}\right|_{V = V_{oc}} \tag{3.7}$$

$$R_{sh} = \left.\frac{1}{\frac{dI}{dV}}\right|_{V = 0} \tag{3.8}$$

3.1.4. Different Solar Cell Models

3.1.4.1. Single-crystalline and Multicrystalline Silicon Solar Cells

First generation solar cells are often called as wafer based technologies. Single-crystalline and multi-crystalline silicon solar cells belong to this classification. The classic types of single junction silicon based solar cells consist of a homojunction, formed by a doping procedure. Although the power conversion efficiencies of single crystalline silicon solar cells are higher, due to the ease and relatively lower production costs, multicrystalline silicon solar cells have a higher market share. First generation solar cells have a life-span of 20-25 years, which is generally higher than the rest of the solar cell types and furthermore, the energy payback period of these solar cells still have a decreasing trend. Commercially available monocrystalline [85] and multicrystalline [86] silicon solar cell modules are shown in Figure 3.7.

3.1.4.2. Thin Film Solar Cells

Thin film solar cells, frequently termed as second generation solar cells, have been developed to address energy requirements and production costs of first generation solar cells. Heterojunction solar cells, formed by the deposition of complementary p-type and n-type thin films of semiconducting materials and amorphous silicon (a-Si) solar cells lie in this group. Flexible substrates like stainless steel or glass are commonly preferred for these devices.

The most successful second generation materials have been cadmium telluride (CdTe), copper indium gallium selenide (CIGS) and amorphous silicon, structures of which are provided in Figure 3.7 [87,88]. The major advantages of these systems are lower manufacturing costs, reduced mass, increased absorption and operationability on light or flexible materials, even textiles. However, the obtained efficiency values from thin film solar cells are still lower than the crystalline silicon solar cells.

3.1.4.3. Novel Solar Cell Designs

Solar cells, utilizing novel concepts, new materials and nanostructures are classified in this group, such as nanocrystalline silicon solar cells, photoelectrochemical solar cells, dye sensitized solar cells, organic solar cells, hybrid (organic-inorganic) solar cells and tandem solar cells.

The working mechanisms of these solar cells do not always rely on a classical p-n junction operation. One of the most successful concepts in terms of industrial aspects is dye sensitized solar cells. Relatively high efficiencies and processibility on glass or flexible substrates have made them one of the major research topics. However, stability is still one of the major issues for dye sensitized solar cells. In dye sensitized solar cells (DSSC), the dye is placed over a semiconductor film, in contact with an electrolyte, as shown in Figure 3.7 [89]. The excitation of the dye upon irradiation is followed by injection of the resulting electrons into the conduction band of the semiconductor, from where they reach the cell anode. Regeneration of dye electrons occurs through donation from a redox electrolyte in contact with the dye. This typically occurs through an organic solvent containing an iodide/triiodide couple. Triiodide is reduced in turn at the counter electrode, while electron migration from the anode to the counter electrode closes the circuit. The voltage generated is equal to the difference between the Fermi level of the semiconducting nanoparticles (TiO_2) and the redox potential of the electrolyte [90].

Another example for these novel concepts is multi-junction solar cells, which are originally developed for space applications. They have been reported to yield high efficiencies, even above the theoretical efficiency limit of silicon based solar cells, as a result of the stacked cells. The basic idea behind these solar cells is that multi layers of p-type and n-type structures are deposited on each other in an order of the widest band gap to lowest band gap semiconductors that are electrically integrated. Therefore, each cell absorbs different sections of the incoming solar irradiation due to difference in the band gaps and efficiencies may exceed theoretical limits of single junction solar cells.

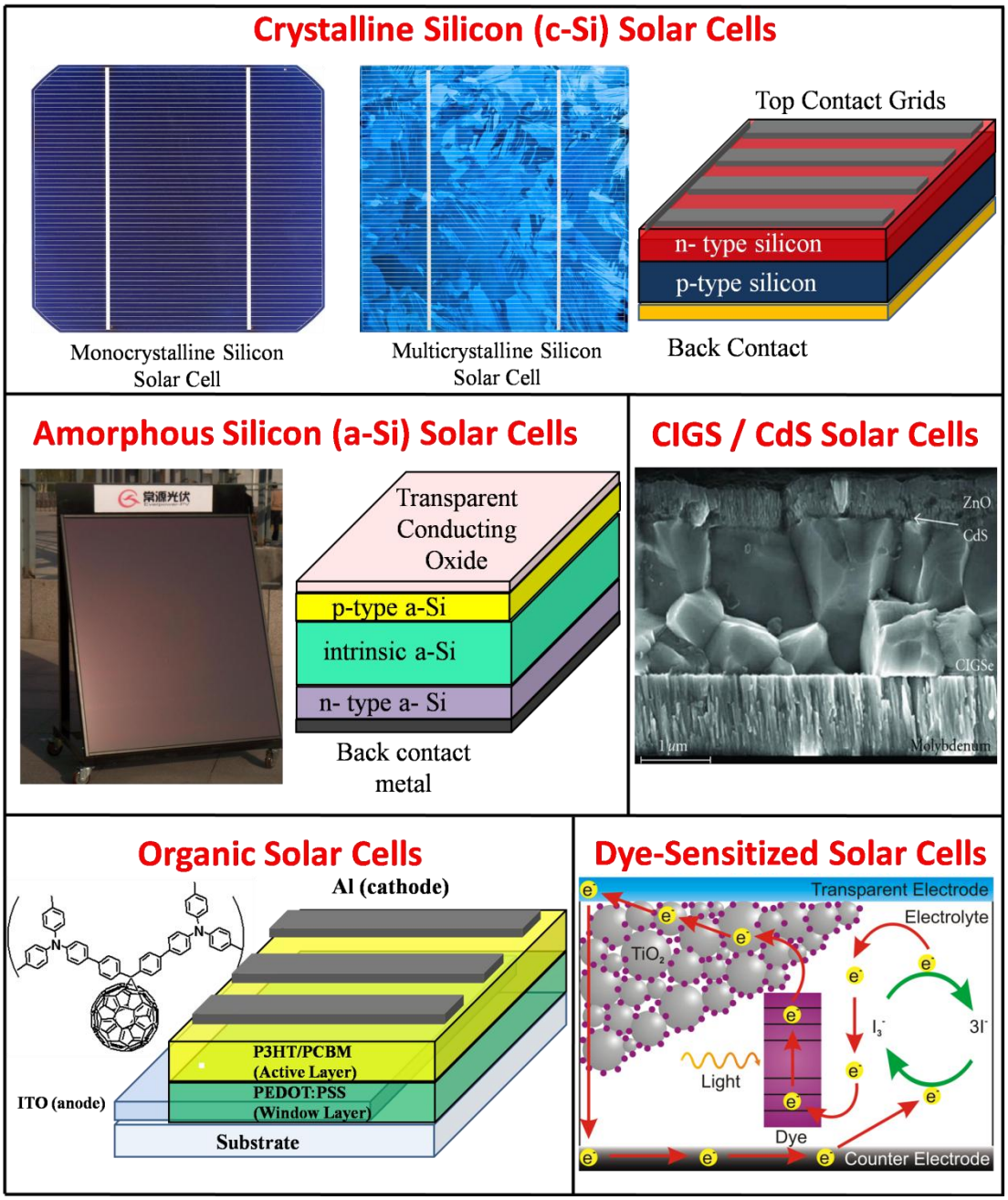


Figure 3.7. Structures of various types of solar cells.

3.1.4.4. Heterojunction Solar Cells

First of all, there are several requirements that the material couple must meet, in order to constitute a decent heterojunction solar cell [82]:

1) The absence of conduction (or valence) band spikes that could impede photogenerated current,

2) Conduction and valence band discontinuities, as close to zero as possible,

3) Energy gap of the absorber, in a range of 1.4-1.6 eV to take advantage of the maximum of the solar spectrum,

4) Energy gap of the window layer, large enough to allow transmittance of as much of solar spectrum as possible,

5) Small lattice mismatch and

6) Small thermal expansion mismatch.

Among these issues, the most problematic one is the lattice mismatch leading to poor heterojunction quality and charge carrier diffusion. One of the most important features of nanowire based radial heterojunctions is that the complementary thin film is deposited, or in other words infiltrated between the nanowire arrays, eliminating the lattice constant mismatch considerations. Together with the enhanced elasticity and deformability of the nanowires, force fields are generated around the radial interface upon thin film deposition, resulting in a rigid structure. Similarly, thermal expansion mismatch is less of a consideration for the radial heterojunctions.

Another important mechanism leading to a great improvement in the solar cell characteristics for radial heterojunctions is the orthogonalized carrier diffusion paths and considerably smaller carrier diffusion distances. There are two basic mechanisms that should take place effectively for solar cells; the electron-hole generation as a result of photon absorption and extraction of photo-generated electrons and holes to the p-n junction and hence, to the appropriate contacts. It was already discussed in Chapter 2 that a fully light absorbing layer is achieved when vertically aligned

silicon nanowires are formed on the surface. Radial heterojunctions also allow the formation of a three-dimensional junction, instead of a two dimensional one in the case of planar heterojunctions. The significance of this concept could be well revealed when the carrier diffusion lengths are examined together with modeling both structures. The minority carrier diffusion length, L_n (or L_p for holes), is a measure of the average distance that a carrier can move from the point of its generation before it recombines. It is directly related to carrier mobility and life-time. In a planar heterojunction solar cell model, given in Figure 3.8., the cell thickness must be greater than the optical thickness "1/a", where "a" is the absorption coefficient of the material and carrier diffusion length must be long enough to reach the p-n junction before recombination. Therefore, only the charge carriers generated in depletion region or diffusion distance to depletion region contributes to the photogenerated current. This limits carrier collectivity of the planar heterojunction devices.

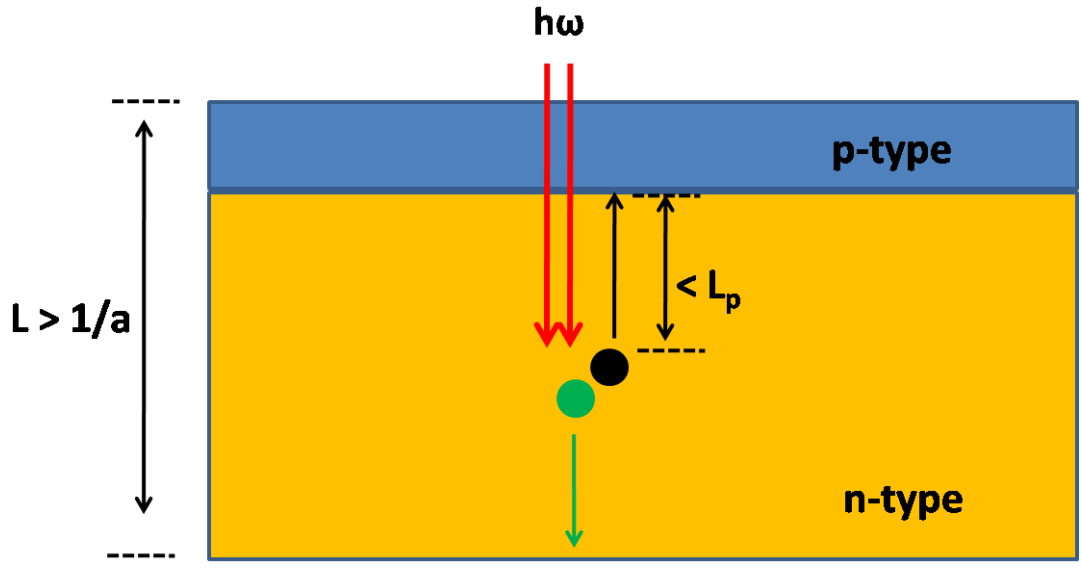


Figure 3.8. Schematic of a planar heterojunction solar cell.

Radial heterojunction solar cells on the other hand, hold important advantages owing to their three-dimensional junctions. As it can be understood from Figure 3.9, the diffusion distance Lp is decreased dramatically due to the presence of nanowires and photogenerated charge carriers are separated and extracted along orthogonal paths,

which is the most efficient case for the charge transport. Furthermore, because of the light trapping nature of the nanowires, incident photon gets scattered multiple times increasing its optical path. This in turn, reduces the optical thickness of the cell to 1/a and sets a lower limit on the diffusion length that is acceptable for making high-efficiency solar cells from a given material in a traditional, planar pn junction geometry. Thus, lower quality materials can also be used in radial heterojuntion geometry, since low carrier diffusion distances is no more an issue.

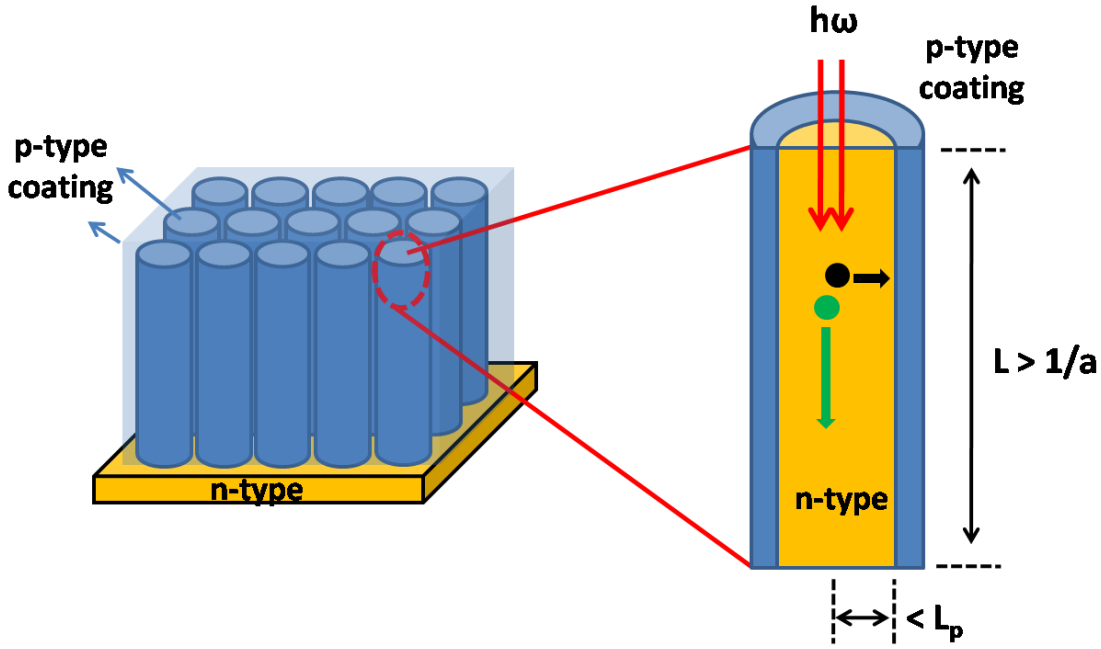


Figure 3.9. Schematic showing the structure and carrier diffusion distance and directions of radial heterojunction solar cells.

3.2. Experimental Details

A schematic of silicon nanowire/PEDOT:PSS solar cells fabricated in this thesis is given in Figure 3.10.

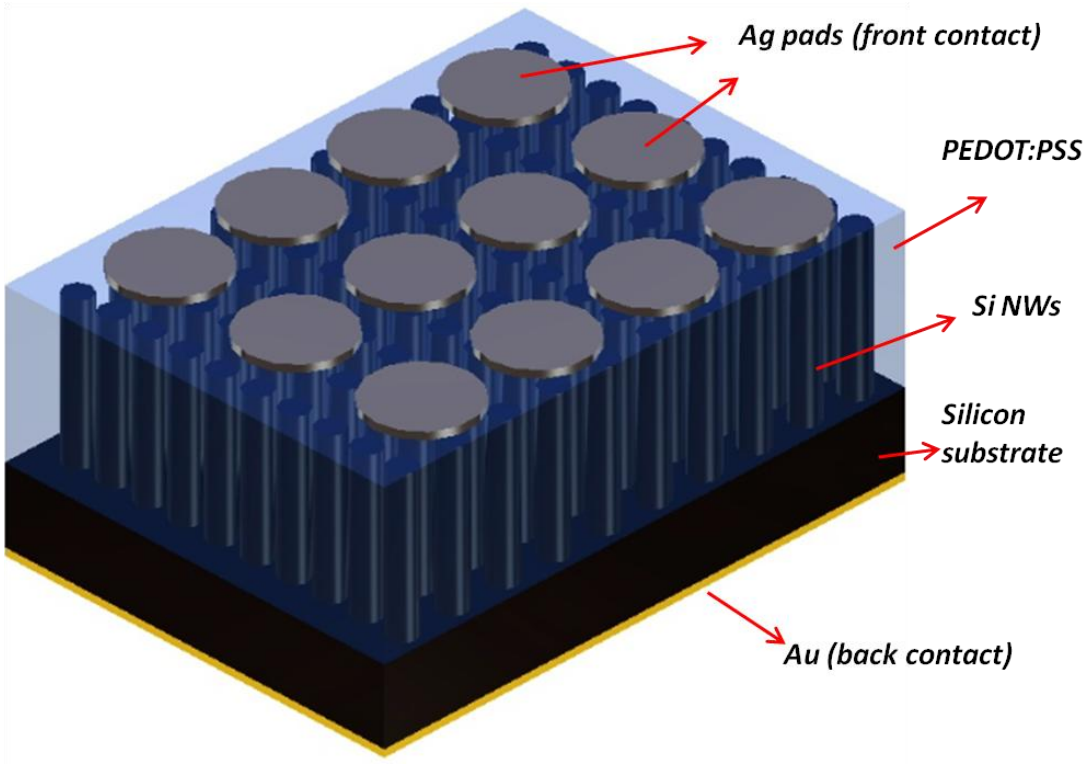


Figure 3.10. Schematic of silicon nanowire/PEDOT:PSS hybrid heterojunction solar cells.

Vertically aligned silicon nanowire arrays were fabricated using electroless etching method, following the previously reported procedure. In brief, 400 μm thick n-type monocrystalline silicon wafers having (100) crystallographic orientation and 1-10 Ω.cm resistivities were used as the starting substrates. Electroless etching was carried out in an etching solution with a concentration of 0.02 M $AgNO_3$ / 4.6 M HF at 20 °C. Nanowire length was controlled by the etching duration. Silver dendrides formed as a result of electroless etching process were removed by nitric acid baths. This was followed by a native oxide removal process conducted through dipping the substrates into HF solution.

Following the nanowire fabrication, back contact evaporation was carried out. This metal/semiconductor (in our case n-type Si) junction is supposed to be an ohmic junction and in order to obtain enhanced device properties, the series resistance at the junctions should be as low as possible. There are many studies indicating that gold has appropriate work function to form ohmic contact with n-type silicon substrates [91]. Furthermore, there are several studies indicating a decrease in series resistance in metal/semiconductor junctions by increasing lateral conductivity with a thin layer of antimony (Sb) [92]. Consequently, Au/Sb (99%:1%) was selected as the back contact material and was evaporated using a thermal evaporator. It is also a well known concept that the ohmic contacts are supposed to be annealed for relieving stress as well as for inducing any desirable reactions between the metal and the semiconductor. This in turn decreases the resistivity of the junction. Back contact annealing was carried out in a quartz tube furnace under nitrogen (N_2) atmosphere at 450 °C for 30 minutes.

As the next step of this process, silicon nanowire/PEDOT:PSS heterojunctions were formed by drop casting PEDOT:PSS onto the silicon nanowire arrays. PEDOT:PSS is a conductive polymer blend dispersed in water. PEDOT:PSS solution used in the experiments was conductive grade and contained 0.5 weight % PEDOT and 0.8 weight % PSS. Drop casting is a simple procedure, widely used for coating of polymeric materials or any material that can be dispersed in a solution. However, the surface properties of the substrate to be coated must be suitable. For instance, if the surface is too hydrophobic or the surface energy of the substrate is too large, drop casting would not be an appropriate method. A similar issue was faced with PEDOT:PSS coating of silicon nanowire arrays by drop casting. This was the most critical part of the device fabrication since the heterojunction quality mostly determines the performance of the solar cells. Several attemps were made for the dispersion of PEDOT:PSS and finally a pre-treatment method was found to yield a homogeneous infiltration of drop casted PEDOT:PSS within the silicon nanowire arrays. This pre-treatment is called “soft baking”. Soft baking includes heating of the surface up to 30-35 °C, which is used in polymdimethylsiloxane (PDMS) microchips before coating epoxy modified polymers [93]. It is also a part of the standard

photolithography process. Soft baking of silicon nanowire containing substrates were carried out at 35 °C for 15 minutes and PEDOT:PSS was drop casted and spreaded homogeneously throughout the surface of the sample. The amount of PEDOT:PSS to be drop casted was optimized after a few attempts. In order to obtain stabilized attachment of polymer onto the silicon nanowire arrays and complete removal of the solvent, in which the polymer is dispersed, a post annealing treatment was also necessary. Approximately 70-100 μL of PEDOT:PSS was coated onto silicon nanowire arrays. Post annealing was conducted at 100 °C for 30 minutes. The annealing temperature was gradually increased in 10 °C steps holding at each step for 10 minutes. Optimization of this procedure and the SEM images of the polymer coated silicon nanowires will be given in the next part of the thesis.

Top contacts of the silicon nanowire/PEDOT:PSS heterojunction solar cells were deposited by thermal evaporation of Ag through a shadow mask. The thickness of the resultant array of circular Ag pads/dots was 500 nm. These Ag pads had a radius of 400 μm and the linear spacing between each Ag pad was 1.25 mm. Such a top contact structure contains several important advantages. Firstly, a thin film of Ag deposition as the top contact would not have been suitable since 500 nm thickness would have made them opaque. Instead of depositing a thin film layer, an array of top contacts were evaporated with an optimized spacing, both allowing photons to enter the active layer of the devices and effective collection of the photogenerated charge carriers (i.e. holes in the p-type side of the junction). Secondly, due to the nature of the drop casting procedure, it is possible that a homogeneous layer of polymer may not have been coated on silicon nanowire arrays. If there is a continuous contact metal, collecting the charge carriers from the entire substrate, the parts that are not conformally coated corrupts the overall performance. Therefore, the current losses that would have been occurred due to the inhomogeneities of the polymer coating were prevented by creating many individual devices on a single substrate and this structure also provided ability to check all the individual contacts for any poor performance throughout the structure before connecting them together with the wiring procedure. In short, top contacts as arrays of silver pads provide a great flexibility for the device characterization.

The photograph and schematic of the thermal evaporation system are shown in Figure (a) and (b), respectively. The shadow mask used for this procedure was first designed in Corel Draw and printed on a photographic film, provided in Figure 3.11 (c). A copper sheet was sprayed with photoresist and dried using a heat gun. The photographic film was placed on the photoresist coated copper sheet, fixed by glass laminate and exposed to halogen lamp (UV) for 15 minutes. Then a developer solution was prepared by mixing NaOH and deionized water. The solution contained approximately 0.6% (by volume) NaOH. The light-exposed copper sheet was immersed in the developer solution until the circular mask patterns are visible. Wet etching solution was prepared by mixing HCl, H_2O_2 and deionized water in a volume ratio of 8:4:,1 respectively. The shadow mask was formed by placing the copper sheet into this solution and finally, following a water rinse, the residual photoresist was removed by acetone.

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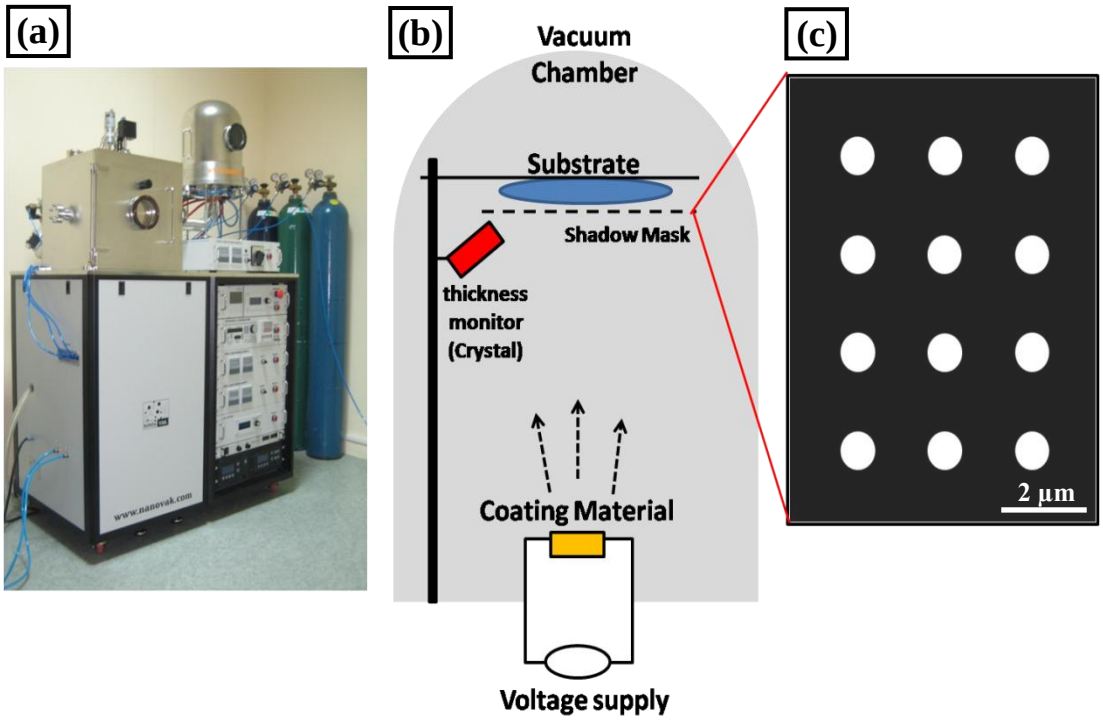


Figure 3.11. (a) Thermal evaporator used for metallization. **(b)** The representative scheme showing the components inside the chamber of the evaporator. **(c)** The shadow mask that was designed and printed on a photographic film.

In order to measure external quantum efficiency and current-voltage characteristics of the devices, solar cells were pasted on printed circuit boards (PCB)'s. Thin gold wires (50 μm in diameter) were attached on the top contact spots to connect them with the printed board's corresponding circuits. Silver paste was used for all attachments. Finally, thick copper wires were soldered on PCB's to collect the overall signal from the connected top contacts. Fabrication procedure for the silicon nanowire / PEDOT:PSS solar cells fabricated in this thesis is given as a flow chart in Figure 3.12 for clarification.

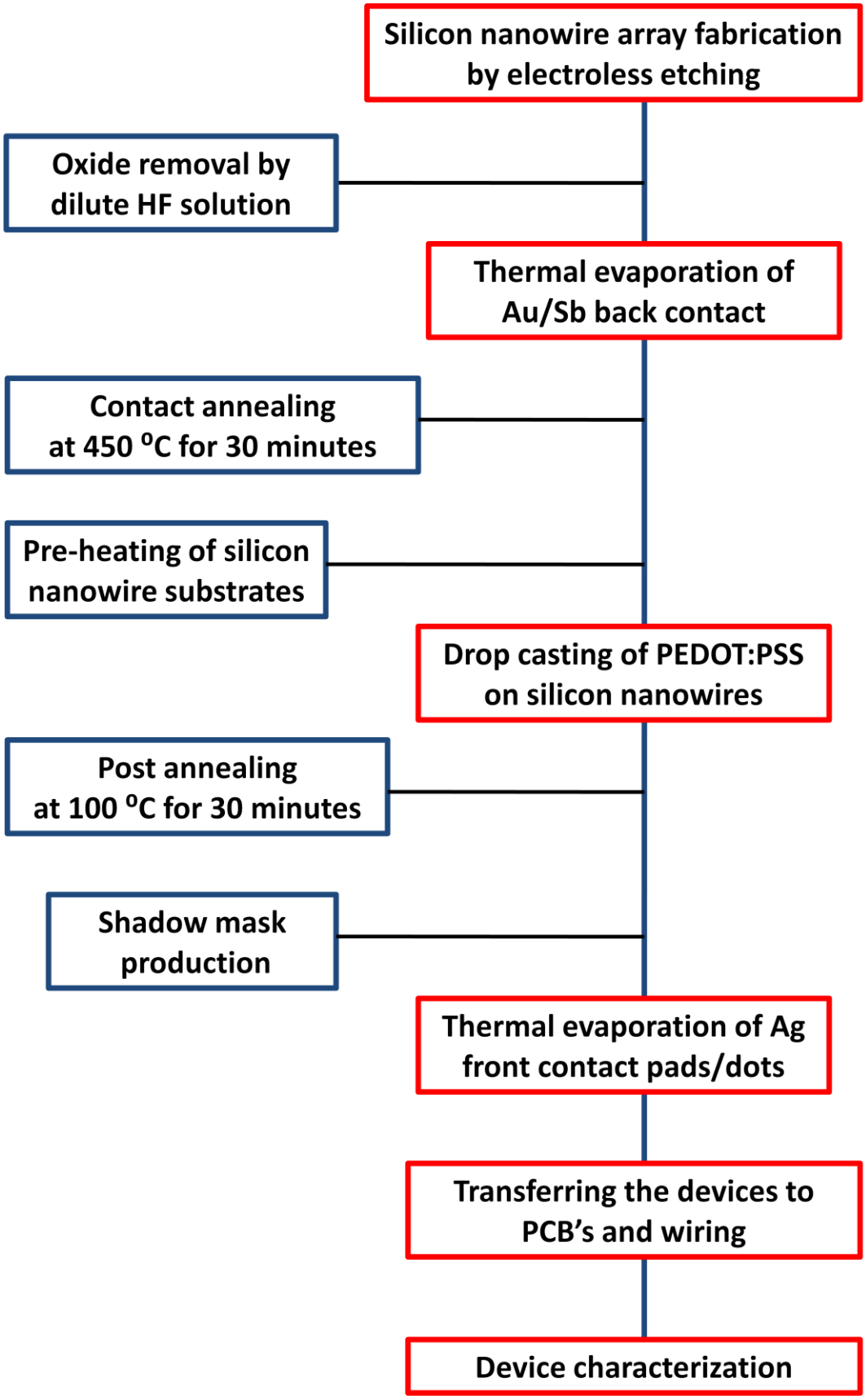


Figure 3.12. Flow chart revealing the procedure of silicon nanowire/PEDOT:PSS heterojunction solar cell fabrication.

3.3. Device Characterizarion Methods

3.3.1. Scanning Electron Microscopy (SEM)

Both as-fabricated and PEDOT:PSS coated silicon nanowires were analyzed by FE-SEM (Nova NanoSEM 430) in 10 keV voltage. In order to obtain cross-sectional images, the polymer containing solar cells were frozen by liquid nitrogen. The frozen samples were cut and the cleaved surfaces with relatively solid structures were examined. In order to prevent charging during SEM examination, which is frequently encountered for polymeric materials, 7 nm of gold layer was sputtered on the samples. Through iterative and consecutive fabrication and SEM analysis, radial heterojunction formation was optimized.

3.3.2. Current-Voltage (I-V) Measurements

Current-voltage (I-V) measurement is the most important and fundamental characterization for solar cells. There are two modes of current-voltage characterization, both of which were carried out. The first one is dark current-voltage measurements. As a result of I-V measurements in dark conditions, several important properties such as resistance and rectification behavior can be determined. In addition, quality of the diode can also be inferred. The second type of I-V measurements are conducted using a solar simulator. These measurements were carried out using an ORIEL 92192 Full Spectrum Solar Simulator, which has a 1600 W, 4 x 4 inch collimated output with a calibrated light spectrum of AM 1.5G. The intensity was set to 0.75 SUN during the measurements to prevent degredation of PEDOT:PSS.

3.3.3. External Quantum Efficiency Measurements

External quantum efficiency (EQE) measurement, sometimes called as spectral photoresponse measurement, is also an important and essential tool in solar cell characterization of solar cells. A light source-monochromator-power display set-up was used for the EQE measurement of heterojunction devices. These measurements

were carried out in 300-1200 nm spectral bandwidth. The power of the light source was measured to eliminate the contribution of the incoming light to the overall signal.

3.4. Results

3.4.1. Silicon Nanowire/PEDOT:PSS Heterojunction Formation

There are two critical points about the formation of radial heterojunction solar cells. The first important point is the quality of the heterojunction, meaning that the coating procedure must yield well attachment and infiltration of the polymer in between the nanowire arrays. The second one is the relative band structures between two complementary layers in terms of the work function, highest occupied molecular level and lowest unoccupied molecular level. In the case of this study, the first issue was fulfilled by optimizing drop casting parameters. Coating processes requiring high vacuum systems, expensive and complex equipments were deliberately avoided in order to maintain the overall cost-effectiveness of this new design of solar cell. There have been a few attempts in literature focusing on hybrid solar cells based on radial heterojunction concept. Among those, the most successful one was by Shiu et. al. Schematic of their solar cell is provided in Figure 3.13 [94].

In their work, silicon nanowire/PEDOT:PSS solar cells were fabricated using a different procedure. According to their procedure, indium tin oxide (ITO) coated glass was preferred as the contact layer, allowing light to transmit into the photo-active region. PEDOT:PSS was spin coated on ITO and before drying of the solvent, silicon nanowire sample is simply pressed by mechanical forces allowing the polymer attachment to the nanowires. Comparing the preferred fabrication route in this thesis with the work of Shiu et. al. a few points have to be addressed. Firstly, the attachment of silicon nanowires with PEDOT:PSS layer was carried out using mechanical forces. This process may induce a deteriorated or even broken structure of silicon nanowire arrays since the substrate is simply pressed and held until the solvent dries out. On the other hand, drop casting of polymer and annealing on a hot plate is much easier and reproducible. If the process parameters such as the amount

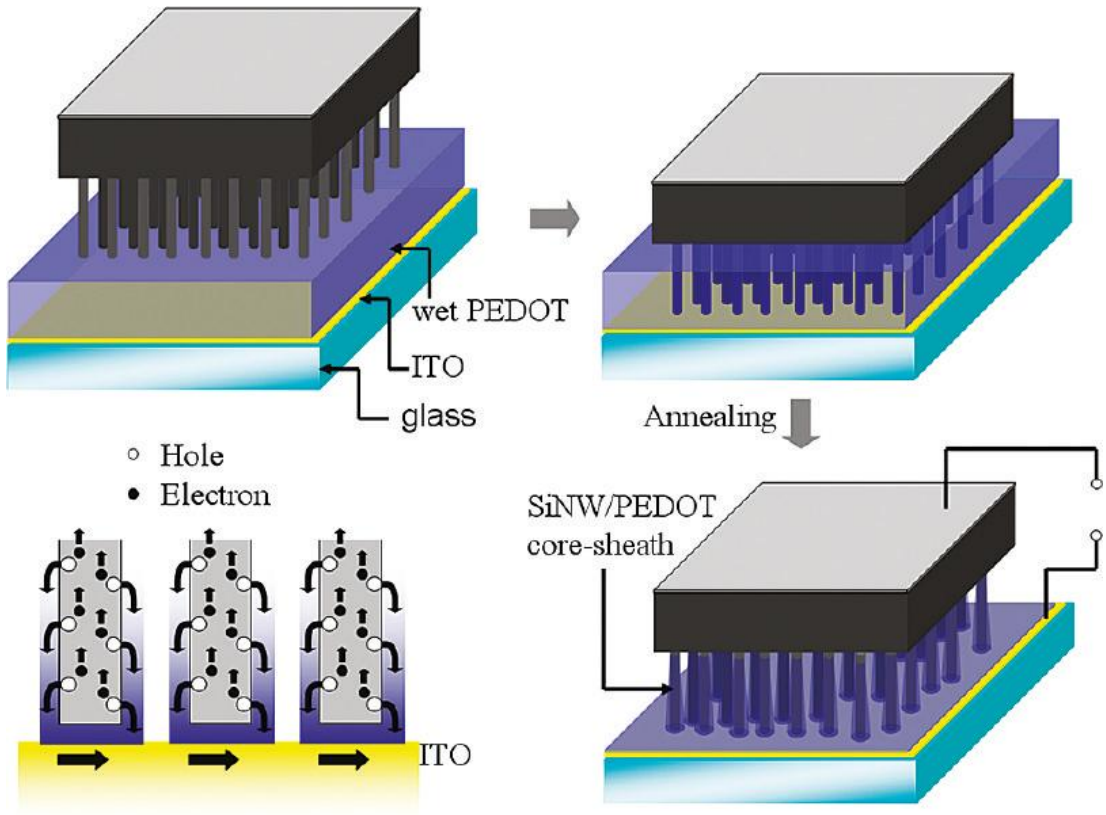


Figure 3.13. Schematic of the fabrication procedure employed by Shiu et. al. SiNW/PEDOT:PSS core-sheath heterojunction solar cells [94].

of polymer, substrate temperature and annealing conditions, are optimized, this process yields a high quality radial heterojunction.

SEM images from the first set of samples showed that the infiltration of the polymer into the nanowires was not proper and the radial junction could not be formed. Figure 3.14 (a)-(d) shows the resultant cross sectional SEM images of those first set of samples containing various lengths of silicon nanowire arrays. Apparently, a proper coating could not be achieved for these samples, especially for the ones at Figure 3.14 (a) and (b). Following these experiments, the coating treatment and the amount of polymer were changed to enhance the coating quality and finally results similar to Figure 3.14 (e) and (f) were obtained. After achieving such a structure, the contacts were deposited and device characterization was carried out. SEM images of the

sample containing 2.65 μm long silicon nanowire arrays before and after PEDOT:PSS coating is shown in Figure 3.15 (a) and (b), respectively.

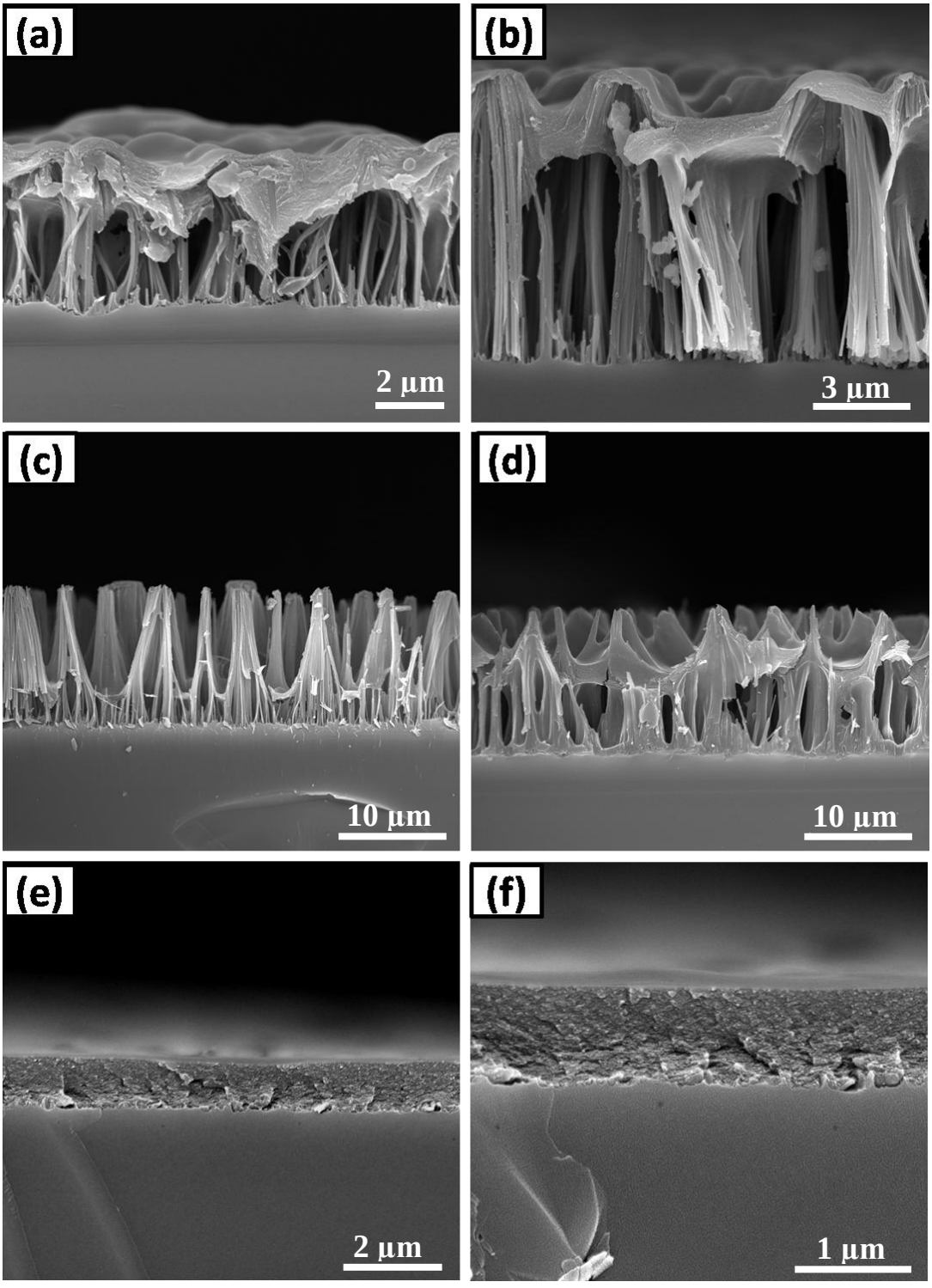


Figure 3.14. Cross-sectional SEM images of first set of silicon nanowire-PEDOT:PSS heterojunctions in **(a) – (d)** and optimized samples in **(e)** and **(f)**.

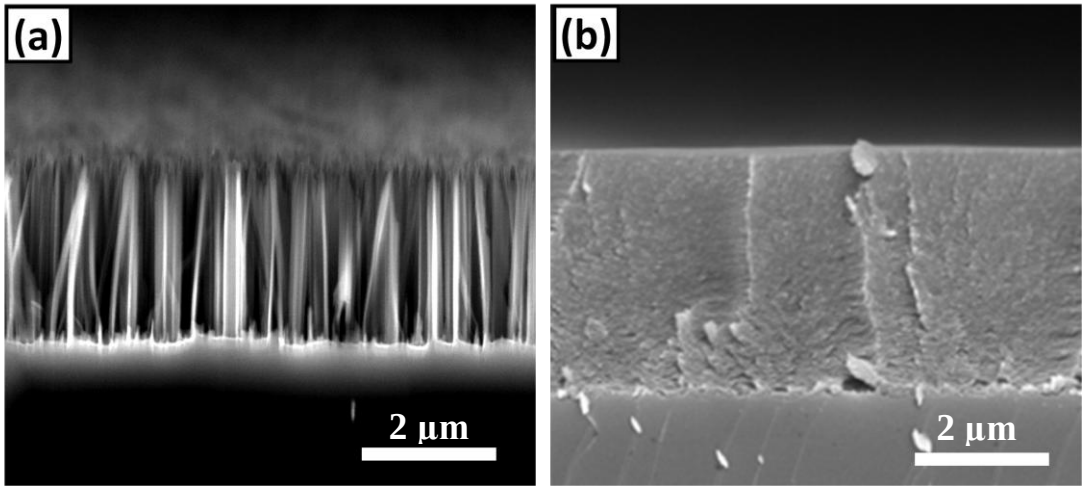


Figure 3.15. Cross-sectional SEM images of **(a)** silicon nanowires before and **(b)** after PEDOT:PSS drop casting. A complete infiltration of polymer into the nanowires was achieved.

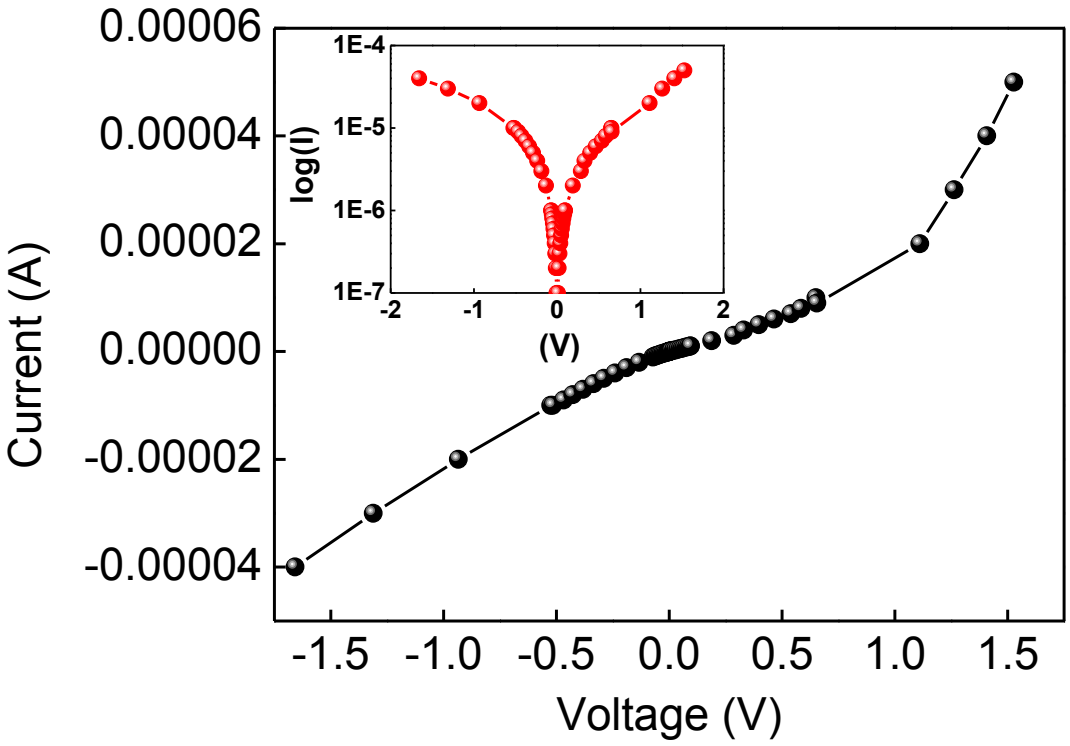
It was explained in the "Experimental Details" part of Chapter 3 that following PEDOT:PSS coating, an annealing treatment is necessary in order to remove the solvent of the polymer, maintain a stable attachment within the radial heterojunction and achieve as low resistance as possible. Therefore, a study was carried out to determine the best annealing condition resulting in the lowest resistivity, thereby the best rectification behavior. There are several studies in the literature related to resistivity of PEDOT:PSS based devices. However, those results are not very consistent with each other as they point out an annealing procedure, carried out at a wide temperature range of 70 – 300 °C [95,96]. Furthermore, a spin coating procedure is generally used in the production of organic and hybrid solar cells. In this aspect, a parametric study was carried out to designate a procedure yielding the lowest reflectivity, while maintaining the cost effectiveness and simplicity of the fabrication of these hybrid solar cells. Ten samples with 1.5 µm long silicon nanowire arrays were fabricated by electroless etching method. First of all, it was observed that PEDOT:PSS coating must be carried out on a pre-heated substrate. This is achieved by a soft-baking process, stated in the "Experimental Details" part in Chapter 3. Then these soft-baked samples were coated with PEDOT:PSS, following various procedures, given in Table 3.1. All samples were annealed for 30 minutes at the given temperatures and resistivity of each sample was calculated.

Following contact metal deposition, current-voltage characterization of the diode was carried out. A continuous and homogeneous coating throughout the silicon nanowire surface could not be achieved with spin coating speeds below 1000 and above 2000 rpm. Current-voltage characteristics of the samples prepared using different annealing procedures are given in Figure 3.16. Almost an ohmic junction characteristics with no rectification behavior was obtained for the sample shown in Figure 3.16 (a). Resistivity of the samples given in Figure 3.16 (a) and (b) were found to be relatively higher than the other samples, as shown in Table 3.1. On the other hand, drop casted samples annealed at 75 and 100 °C, given in Figure 3.16 (c) and (d) respectively, revealed decent rectification behavior. The most proper diode behavior together with the lowest resistivity was obtained for the sample in Figure 3.16 (d). This procedure was then chosen as the optimum recipe for the PEDOT:PSS coating onto silicon nanowire arrays.

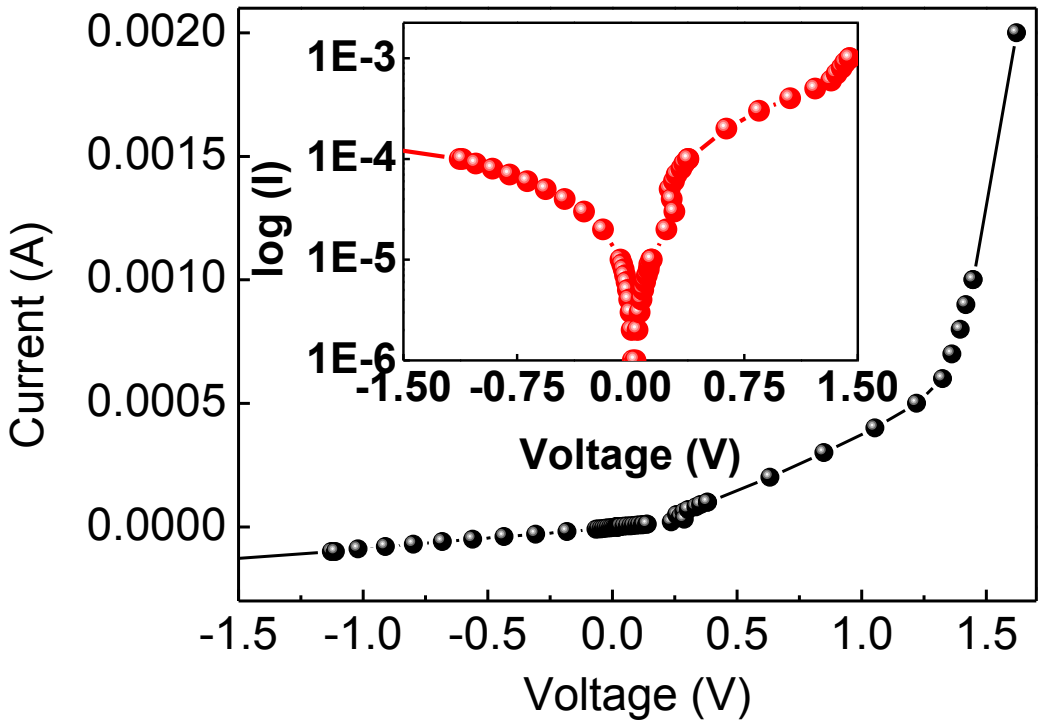
Table 3.1. Annealing temperature, coating procedure and the resulting resistivities of silicon nanowire / PEDOT:PSS devices.

PEDOT:PSS Coating Procedure	**Annealing Temperature (°C)**	**Resistivity (Ω) (at 1.5 V)**
Spin coating at 1000 rpm	75	1450
Spin coating at 1000 rpm	140	18750
Spin coating at 2000 rpm	75	4525
Spin coating at 2000 rpm	140	37500
Drop casting	75	367.5
Drop casting	**100**	**190**
Drop casting	125	3252
Drop casting	140	30605
Drop casting	170	38461
Drop casting	200	50666

(a)


0.00006
0.00004
0.00002
0.00000
-0.00002
-0.00004
Current (A)
-1.5 -1.0 -0.5 0.0 0.5 1.0 1.5
Voltage (V)
1E-4
1E-5
1E-6
1E-7
log(I)
-2 -1 0 1 2
(V)

(b)


0.0020
0.0015
0.0010
0.0005
0.0000
Current (A)
-1.5 -1.0 -0.5 0.0 0.5 1.0 1.5
Voltage (V)
1E-3
1E-4
1E-5
1E-6
log (I)
-1.50 -0.75 0.00 0.75 1.50
Voltage (V)

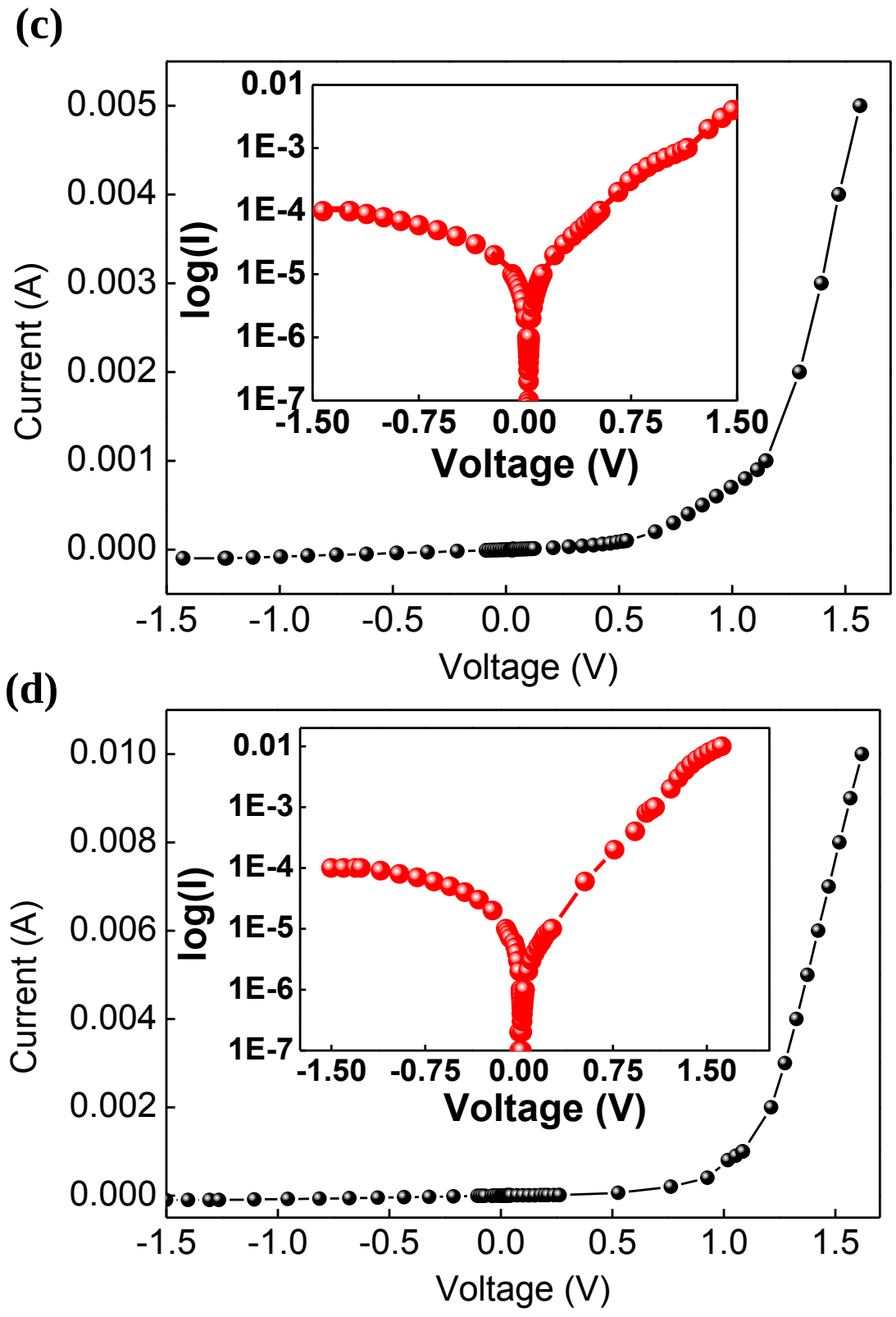


Figure 3.16. The insets show logarithmic I-V curves for the samples revealing their rectification behavior. Current-voltage (dark condition) curves for the samples that were **(a)** spin coated (at 2000 rpm) and annealed at 140 ^{0}C, **(b)** spin coated (at 1000 rpm) and annealed (at 75 ^{o}C), **(c)** drop casted and annealed at 75 ^{o}C, **(d)** drop casted and annealed at 100 ^{o}C.

Charge transfer is driven by the energy band alignments of the components relative to each other. Hence, the energy levels of the materials should be taken into account and the heterojunction band structure that would allow an efficient charge transfer mechanism should be formed by proper material selection. There are three major issues that need to be addressed. The first one is the electron hole generation due to photon absorption, the second one is the charge seperation at the heterojunction and finally the transportation of the seperated charges to the corresponding contacts to generate the photo-induced external current. Energy levels relative to the vacuum level are shown in Figure 3.17 for the components of the silicon nanowire/PEDOT:PSS heterojunction photovoltaic cell (without any adjustments for dipole formation or band bending due to Fermi levels).

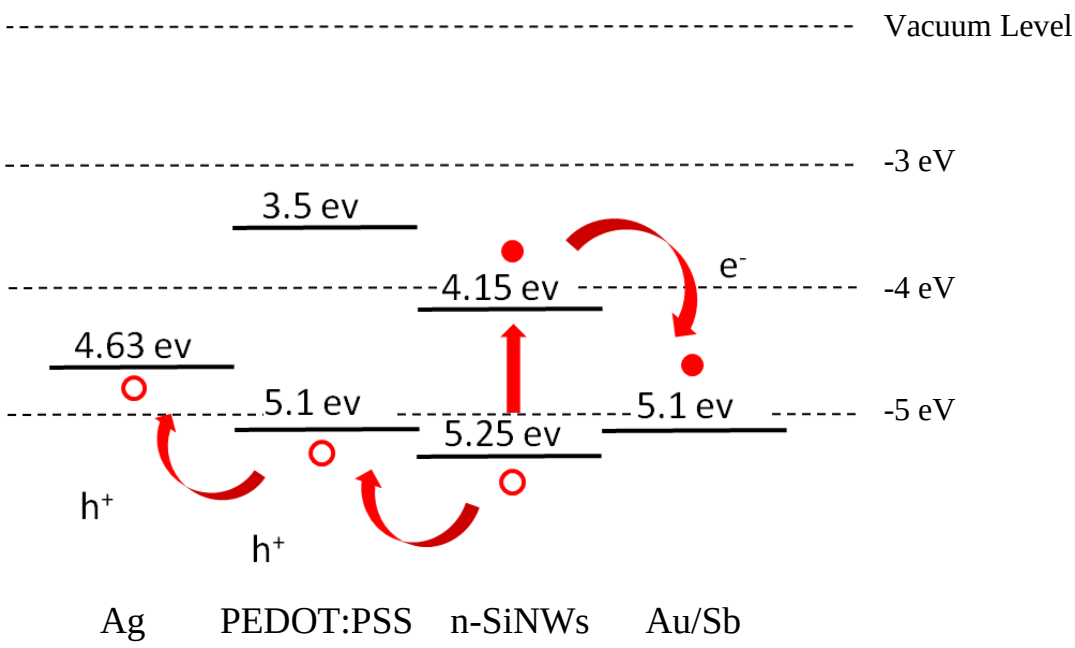


Figure 3.17. The energy band diagram for the heterojunction revealing a suitable band alignment of the components allowing efficient charge generation and transfer across the neighboring layers.

Upon irradiation, electrons excited into the conduction band of the silicon are preferentially collected by the Au contact. Injection of electrons from the silicon to the Ag top electrode is prevented by the continuous PEDOT:PSS layer, which

isolates Ag electrodes from the tips of silicon nanowires. The highest occupied molecular orbital level of PEDOT:PSS is positioned to inject holes into the Ag electrode, and should accept holes generated by absorption in the silicon nanowires. The light trapping nature of silicon nanowires provide very strong absorptivity, consequently an effective charge generation takes place in the semiconducting materials. Although the lowest unoccupied molecular orbital of the semi-transparent PEDOT:PSS is positioned above the fermi level of the silicon nanowires, photogenerated electrons do not have a sufficient contribution to the overall photocurrent due to dominating recombination mechanisms. Nevertheless, electrons generated in the silicon nanowires are efficiently separated and transferred into the Au contact. The radial heterojunctions provide relatively much smaller diffusion lengths for these charge carriers enabling an effective charge collection mechanism. In short, the energy levels in silicon nanowire/PEDOT:PSS solar cell are appropriately aligned allowing a decent charge transfer mechanism.

The light trapping effect of silicon nanowire arrays have been discussed in Chapter 2. In the previous reports related to operation of silicon nanowire based solar cells, it was stated that the exciton binding energy, together with the charge carrier life-time decreases with increasing silicon nanowire length [11]. In addition, longer silicon nanowire arrays provide a higher density of energy trap sites due to the broken bonds of silicon atoms along the interface. Longer nanowires also decrease the quality of the heterojunction as the polymer infiltration towards the bottom of the nanowires become more difficult. Furthermore, increasing the thickness of polymer layer would increase the resistivity of the device. Considering all these important facts, it was predicted that relatively shorter nanowires would be more suitable for radial heterojunction solar cells. The reflectivity of 1 μm long silicon nanowire arrays are provided in the Figure 3.18, revealing the dramatic decrease in the reflectivity. Therefore, it could be concluded that, even though the previous silicon nanowire length dependent reflectivity study pointed out that 10 μm long silicon nanowire arrays exhibit the lowest reflectivity; relatively shorter nanowires, which still decrease the reflective losses remarkably, must be preferred for the heterojunction solar cell applications.

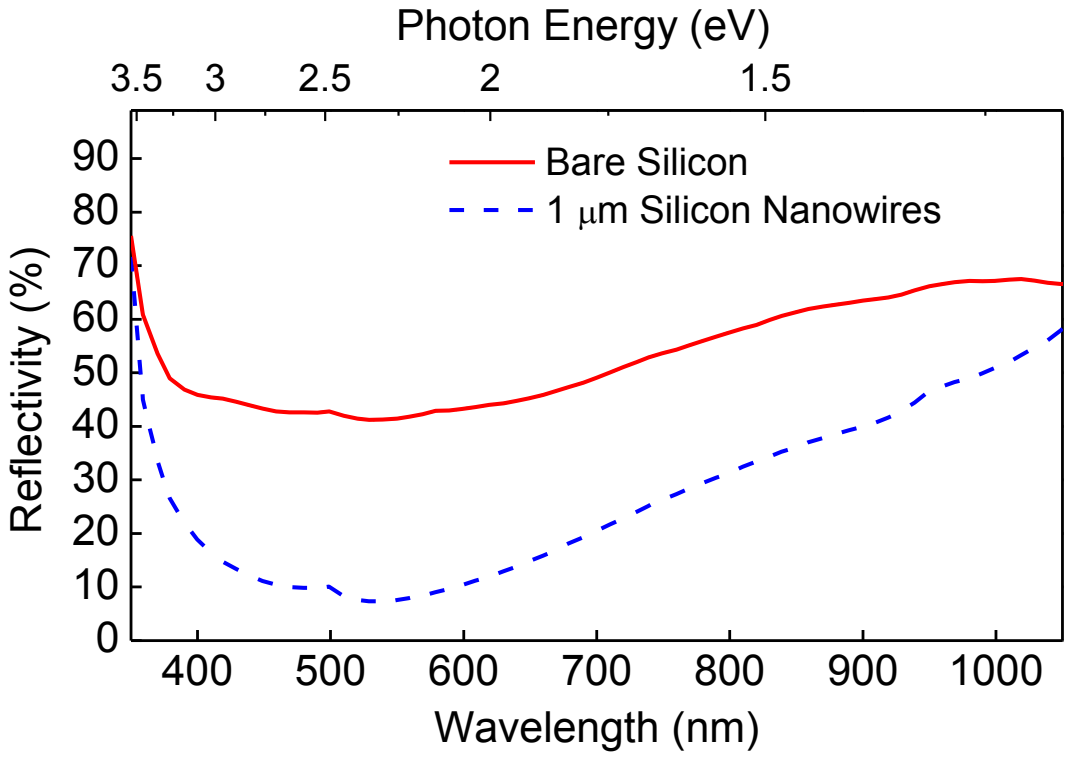


Figure 3.18. Reflectivity of 1 μm long silicon nanowires in comparison to bare silicon wafer.

Dark current-voltage measurements are quite important for solar cells since they reveal diode properties and the rectification behavior. Upon illumination of the system, even small fluctuations in the incoming light intensity introduce a large amount of noise to the system making it difficult to characterize. On the other hand, dark current-voltage measurements do not involve photogenerated current, rather the system's electronic properties are determined. The dark current-voltage graph of both silicon/PEDOT:PSS (planar heterojunction solar cell) and silicon nanowire/PEDOT:PSS (radial heterojunction solar cell) are provided in Figure 3.19. Length of the silicon nanowires utilized within this solar cell was 0.88 μm. A decent diode behavior was presented for radial heterojunction solar cells. The rectification ratios ($I_{forward}$ / $I_{reverse}$) of radial and planar heterojunction solar cells are calculated as 370 and 79, respectively. This clearly points out that a more efficient carrier transport and current output are obtained for radial heterojunctions owing to the three

dimensional interface and enhanced carrier transport properties brought by nanowire arrays.

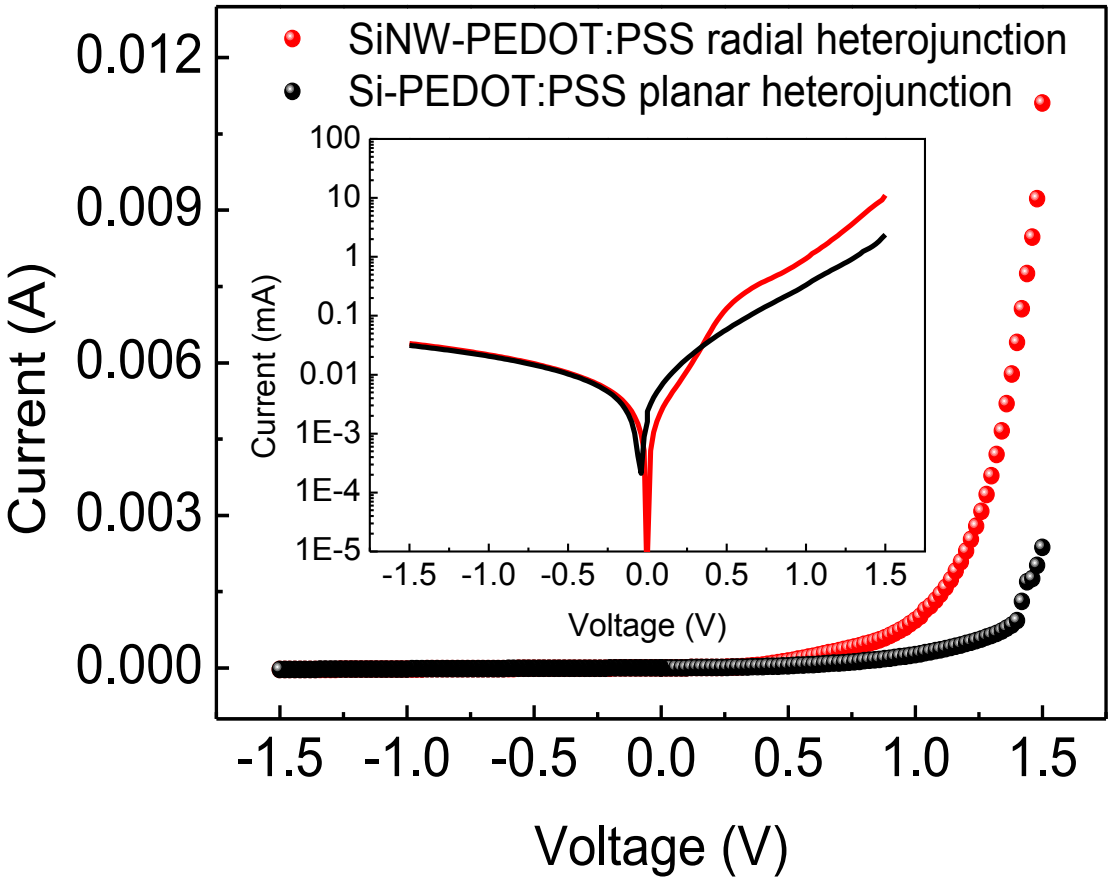


Figure 3.19. Dark current-voltage measurements of radial and planar heterojunctions. Inset shows the logarithmic plot of I-V characteristics.

The most important solar cell characteristic is the power conversion efficiency. For the calculation of power conversion efficiency, the area that current is drawn over, must be determined precisely. This is one of the critical issues related to radial heterojunction solar cells, especially for circular top contact arrays. In order to resolve this issue, maximum area leading to the highest current was determined. For this purpose, two silicon nanowire / PEDOT:PSS solar cells with only one top contact (Ag pad) were fabricated under the same conditions. A metallic mask, as shown in Figure 3.20, was fabricated following the recipe given in Chapter 2. AM

1.5G simulated light was illuminated on the samples through this shadow mask, centering the Ag pad within the voids of the shadow mask. Then, the resulting current generated by the solar cell was measured. As the size of the holes illuminating the sample increases, current generated by the solar cell was found to increase until it saturates. Saturation shows the limiting area for current collection.

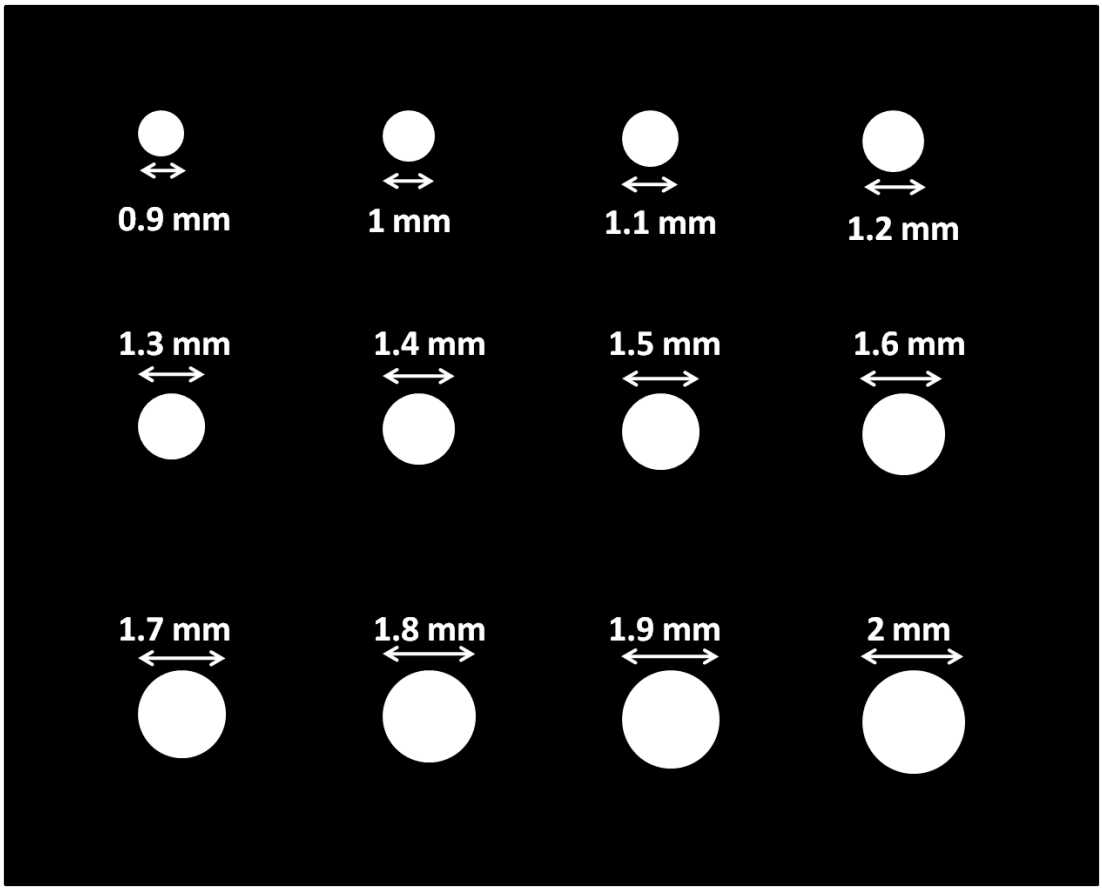


Figure 3.20. The shadow mask designed to determine the limiting area, over which light could be collected by a single Ag top contact.

The same procedure was carried out for both samples in order to validate the measurement. The current vs. diameter of the illuminated circular area plots of both solar cells are given in Figure 3.21. The results were consistent with each other and it was concluded that the limiting area was 1.767 mm^2, including the circular area of Ag contact of 0.5 mm^2.

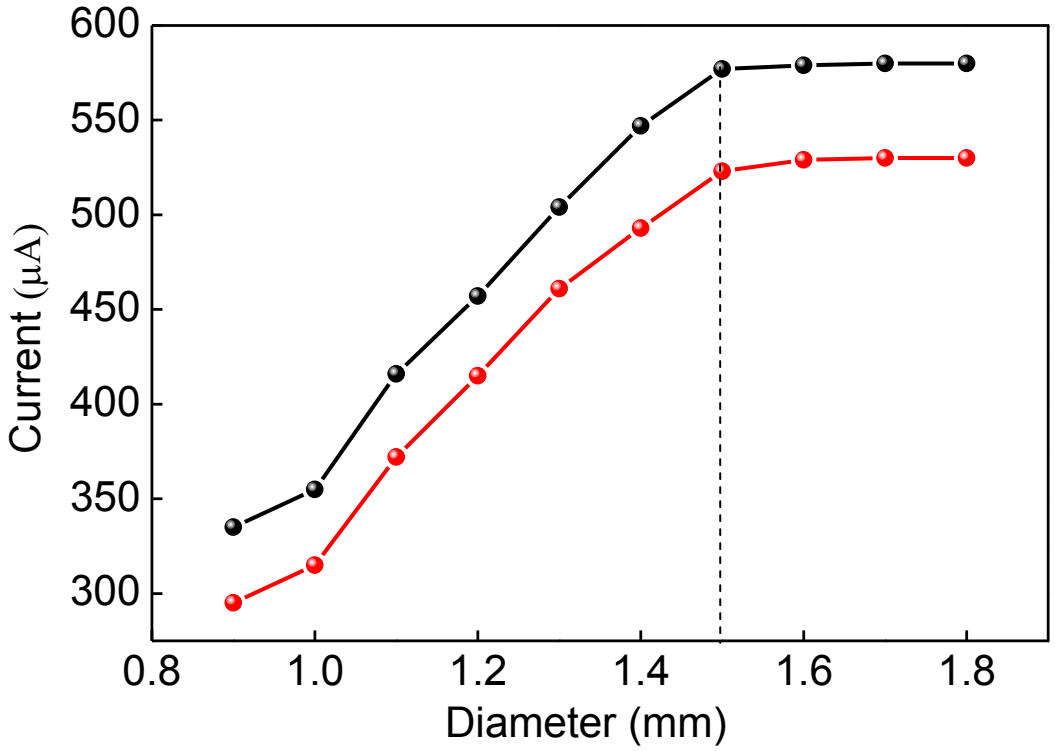


Figure 3.21. The current change versus the diameter of the illuminated region.

As a result of this study, 31.99 mm^2 was determined as the limiting area that was supposed to be entered as the input of the solar simulator software. Figure 3.22 is a representative schematic, showing this limiting area for current collection.

The current density – voltage characteristics of the Si NW-PEDOT:PSS device with 0.88 μm long nanowires compared to the planar heterojunction is shown in Figure 3.23. It points out a 24.6 mA/cm^2 increase in short-circuit current density (Jsc), and more than 100 mV increase in the open-circuit voltage (V) and approximately 8.5 folds increase in the energy conversion efficiency of the radial heterojunction over the planar heterojunction device. Efficiency of the planar heterojunction was found to be 0.62 %, whereas it was 5.30 % for the radial heterojunction.

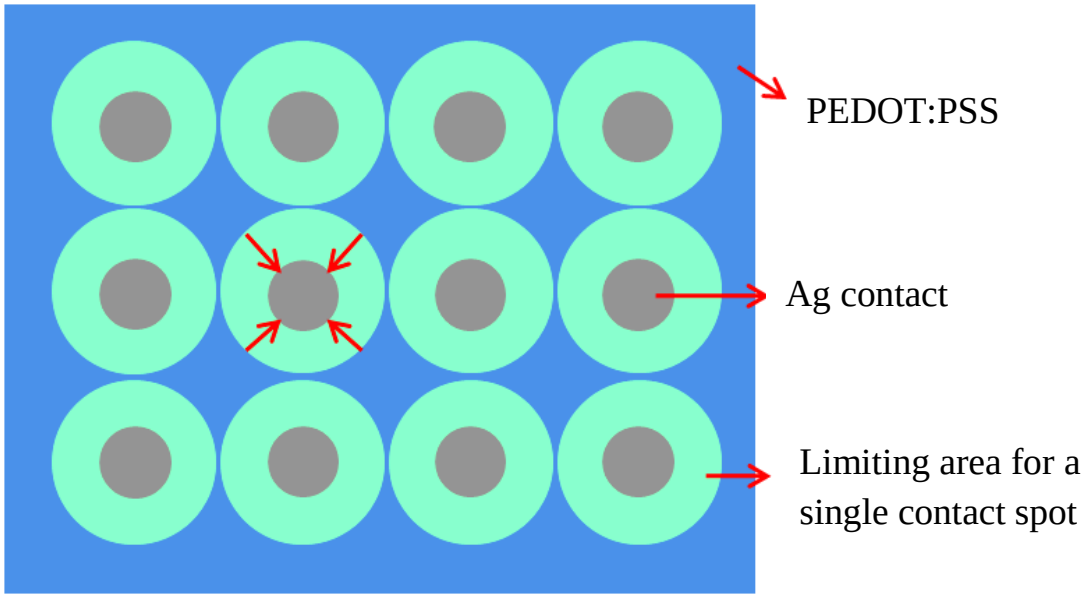


Figure 3.22. Schematic showing the limiting area over which the photogenerated current is collected by the circular top contacts.

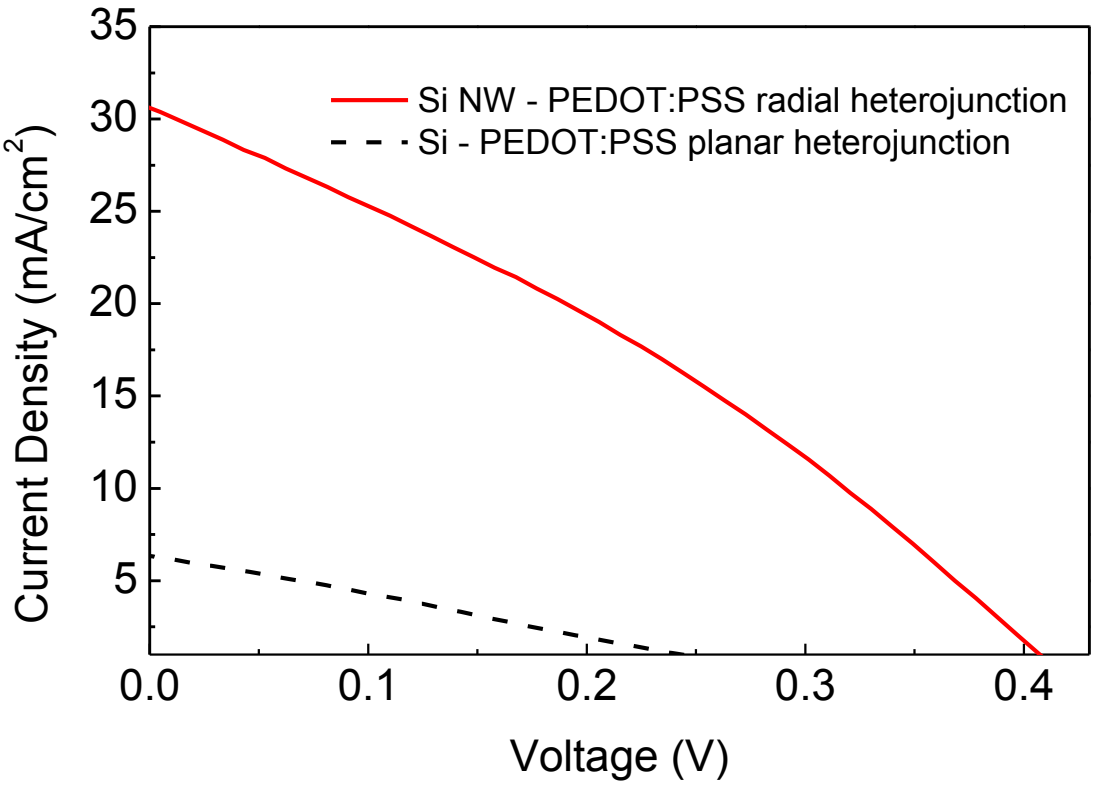


Figure 3.23. Current density-voltage graph of radial and planar heterojunction solar cells obtained under AM 1.5G simulated light.

The reason for low efficiency for the planar silicon/PEDOT:PSS solar cell was mainly due to the recombination of electron-hole pairs generated away from the diffusion distance into the two dimensional junction. On the other hand, much shorter diffusion lengths of the photogenerated electron-hole pairs and much more efficient charge transport could be attained for three dimensional radial heterojunction leading to higher efficiency. Low shunt resistance (1350.7 $\Omega.cm^2$) and high series resistance (605.9 $\Omega.cm^2$) are evident in Figure 3.23 together with the low fill factor (FF, 30.8%), for the silicon nanowire/PEDOT:PSS heterojunction solar cell. Low shunt resistance could be attributed to a few silicon nanowires within the arrays making contact with Ag top electrodes. Although electroless etching method leads to the formation of nanowires with uniform length, drop casting process could easily lead to a few uncovered nanowire tips. This could provide alternative electrical pathways that do not contribute to photocurrent. High series resistance, on the other hand, could be due to the long distances that holes need to travel before getting collected by the Ag top electrode. High sheet resistance of the polymer layer as compared to the silicon used in this work could also contribute to the sheet resistance. This in turn becomes more prominent when the silicon nanowire arrays get longer.

Up to this point, the radial heterojunction concept has been set forth in comparison with planar heterojunctions and a tremendous improvement has been observed for these systems. In this part of the thesis, the effect of silicon nanowire length on the solar cell characteristics is investigated. It would be a straightforward prediction that silicon nanowire length would affect the radial heterojunction dynamics in many ways. First of all, polymer infiltration and thereby the heterojunction quality is much better for shorter nanowires. Carrier transport to respective contacts becomes rather problematic for longer nanowires, due to the significant increase in the number of recombination sites present along the silicon nanowire/PEDOT:PSS interface. On the other hand the reduction in the reflectivity for longer nanowires must facilitate a more efficient photon absorptivity. In order to confirm these theoretical predictions, electroless etching processes was conducted for 5, 10, 20, 40 and 50 minutes, resulting in nanowire lengths of 0.88, 1.68, 2.65, 5 and 6.58 μm, respectively. These

samples were coated with PEDOT:PSS and their device characteristics were measured and compared with each other. Figure 3.24 (a) shows the current density-voltage characteristics of the devices under AM 1.5G simulated light. Obtained photovoltaic conversion efficiency values with respect to the nanowire length are plotted in Figure 3.24 (b). Highest performance was obtained from the solar cell fabricated with 0.88 μm nanowires. The performance of the solar cells was found to decrease with increasing nanowire length. There could be several reasons for this behavior. Firstly, deterioration in the vertical alignment of nanowires negatively affect the orthogonality of photon absorption and carrier diffusion paths, causing less efficient current generation. Secondly, as the nanowires grow longer, bundling mechanism becomes more dominant and consequently the nanowires may not be completely covered with PEDOT:PSS.

Attempts on the formation of nanowires below 0.88 μm were not successful. In those experiments, silicon substrates that were removed just after the initial stages did not contain well defined nanowires. Instead, a textured surface structure similar to porous silicon was present; therefore, the shortest nanowires used in the fabrication of the solar cells were 0.88 μm long. All of the measured solar cell parameters, efficiency (η), short circuit current density (Jsc), open circuit voltage (Voc) and fill factor (FF) are tabulated and given in Table 3.2.

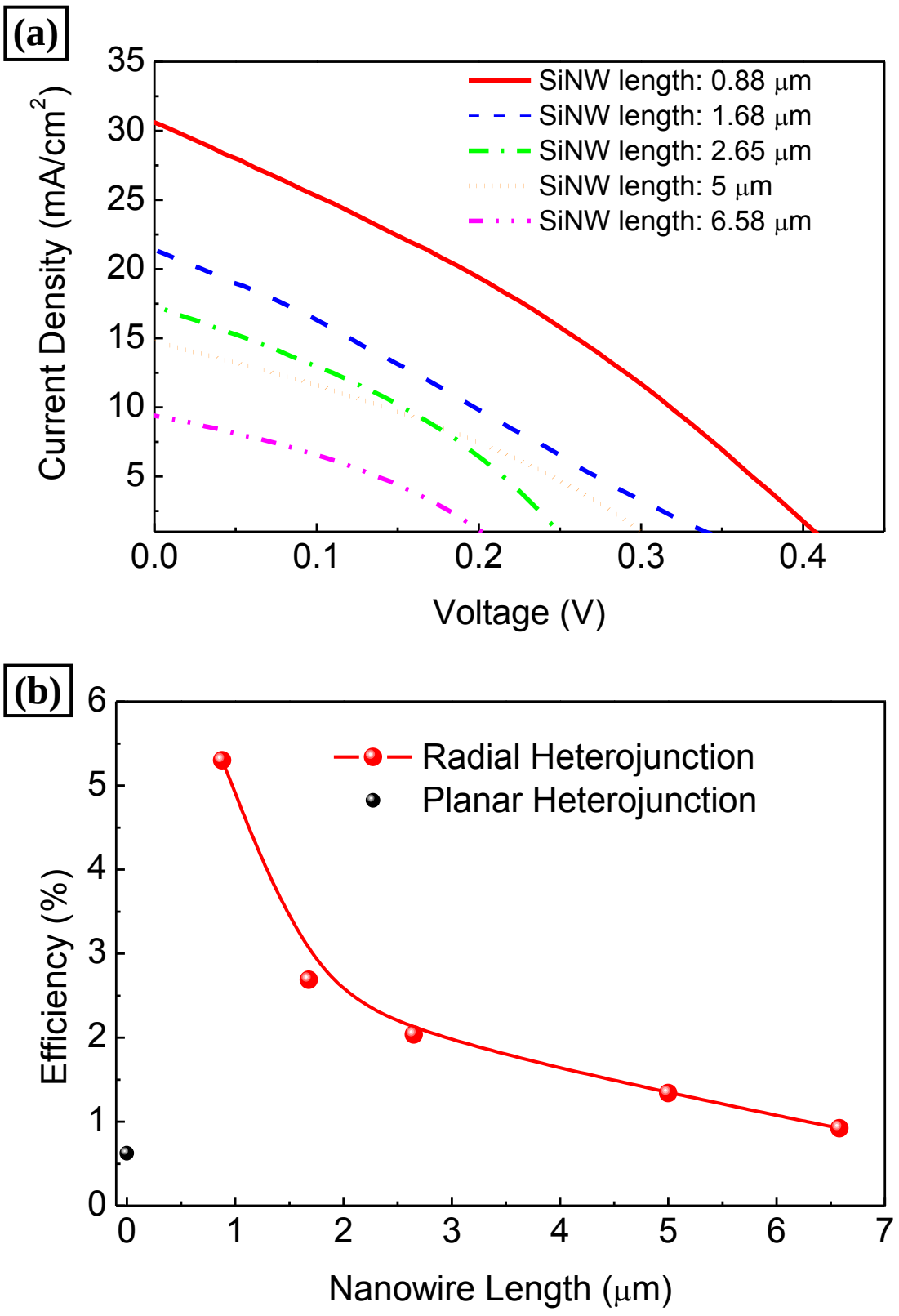


Figure 3.24. Silicon nanowire length dependent **(a)** current-voltage characteristics and **(b)** photovoltaic conversion efficiency.

Table 3.2. Characteristics of silicon nanowire/PEDOT:PSS solar cells with different silicon nanowire lengths.

SiNW/PEDOT:PSS Samples	η (%)	Jsc (mA/cm^2)	Voc (V)	FF(%)
0.88 μm SiNWs	5.30	31.3	0.417	31
1.43 μm SiNWs	2.69	21.3	0.359	26
2.65 μm SiNWs	2.04	17.5	0.256	34
5.00 μm SiNWs	1.34	10.0	0.311	33
6.58 μm SiNWs	0.92	9.4	0.214	34

EQE measurements of both radial and planar heterojunctions have been carried out for comparison. The devices show photoresponse over the entire spectral bandwidth and comparison between their EQE curves provides insights into the photoconversion efficiency, absorption enhancement and current generation mechanisms in both PEDOT:PSS and silicon nanowire layers, as shown in Figure 3.25. High EQE of silicon nanowire based radial heterojunction cell shows that light absorption over the entire spectral bandwidth, electron-hole pair generation, separation of these charge carriers in the junction and carrier transport to the contacts take place effectively. The maximum EQE value of 77% was observed at 500 nm. On the other hand, lower EQE of the planar heterojunction solar cell could be attributed to lower light absorption and higher recombination of generated electron-hole pairs due to longer diffusion distances. Both radial and planar heterojunction devices show the same behavior in the whole interval. At the low wavelength portion (300-400 nm) EQE of the devices decreases, which can be attributed to surface recombination of charge carriers. Also the decrease in EQE at the higher wavelength portion of the curve (1000-1200 nm), near the band gap of silicon, is a consequence of reduced absorptivity of the devices. In addition, the tail band states of silicon results in photoresponsivity below the band gap of silicon (above 1100 nm).

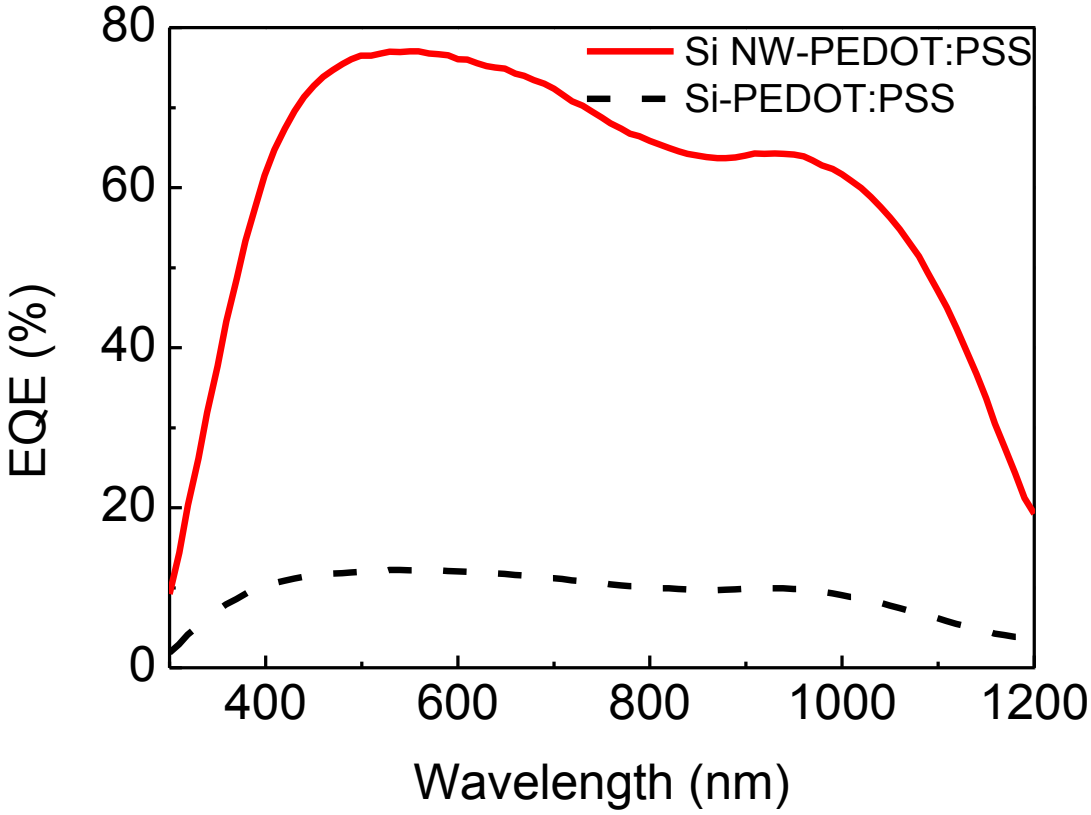


Figure 3.25. EQE measurements of radial and planar heterojunction solar cells.

CHAPTER 4

CONCLUSIONS AND FUTURE RECOMMENDATIONS

4.1. Conclusions

This thesis consists of a detailed parametric study on the fabrication of vertically aligned silicon nanowire arrays using electroless etching method and utilization of these silicon nanowires in heterojunction solar cells.

In the first stage, the electroless etching mechanism was investigated and the process conditions for the fabrication of silicon nanowire arrays using electroless etching method was studied in detail as a function of temperature, etching time, etching solution concentration, pressure and starting substrate characteristics. This detailed study was necessary in order to prove that electroless etching process could be well controlled and it can be used as an alternative to the conventional nanowire fabrication methods. The results revealed that silicon nanowires with desired lengths can be rapidly grown over large areas with the electroless etching method and diameters of the as fabricated silicon nanowires are mostly in the range of 50-150 nms. Silicon nanowire length was found to increase with processing temperature and time. Longer nanowires were found to form bundles due to increased capillary forces formed upon pulling the samples out of the etching solution. Reflection measurements were carried out and the effect of processing parameters on the reflectivity of the substrates were elaborated. Following the formation of the nanowires on silicon substrates, reflectivity of the samples decreased drastically, which then start to increase with further increase in the nanowire length. Silicon substrate with 10 μm long silicon nanowire arrays was found to have the lowest reflectivity.

In the second part, silicon nanowire based radial heterojunction solar cells with complementary p-type (PEDOT:PSS) polymer were fabricated using simple and cost effective procedures. A study was conducted to figure out the optimum polymer coating and annealing conditions. This was done in order to achieve high quality heterojunctions, where conformal coating of the polymer layer on the nanowires was achieved. In addition, it was also done to get the lowest resistivity value within the polymer layer. Solar cells, fabricated with this optimized procedure then resulted in the highest photovoltaic conversion efficiency. Photovoltaic conversion efficiency of the radial heterojunction cells were compared to that of the planar ones fabricated under the same conditions and a great enhancement was observed in the radial heterojunction. It was found that the optimum silicon nanowire length, facilitating the best electron-hole pair separation in the junction and collection in the contacts, was 0.88 μm. The highest energy conversion efficiency obtained was 5.30%. EQE measurements revealed that silicon nanowire/PEDOT:PSS devices can harvest photon energy over a very broad spectral range, with the highest EQE value of 77% located at 500 nm. This work demonstrates that with the further developments and optimizations, silicon nanowire based hybrid heterojunction solar cells could have a great potential to replace conventional solar cells.

4.2. Future Recommendations

In this thesis, it is proven that silicon nanowires with desired lengths can be fabricated. Precise control of nanowire diameters on the other hand is very difficult since this is a solution based top-down approach. It was initially predicted that diameters of nanowires could be adjusted by changing the molarity of silver nitrate, thereby the amount of silver ions coming into contact with the silicon wafer and causing simultaneous reduction-oxidation reactions. However, the resultant structures obtained from solution concentrations different than a specific value were far from being individual and vertical nanowires. Therefore, in order to attain well control over the diameters and have a sharp diameter distribution, lithographical tools could be used. This involves electron beam lithography or alternatively nanosphere lithography. Due to time and cost constraints electron beam lithography

could be omitted. In nanosphere lithography, a monolayer of commercially available polystyrene or silica nanospheres could be deposited onto silicon substrates that are going to be etched. Silver thin films could then be deposited onto the empty spaces left between the spheres. Following the removal of the nanospheres, the substrate could be electroless etched to have individual nanowires with desired diameters, set by the void spaces between nanospheres.

As it was discussed, silicon nanowires are widely used for many laboratory scale applications. Especially electroless etched silicon nanowires have a great potential to be used in field effect transistors for enhanced charge transport and as anode material in lithium ion batteries, owing to their large surface areas and high lithium uptake. Also it was realized during TEM sample preparation stage that silicon nanowires could be scraped off of the silicon substrate and dispersed quite homogeneously in deionized water. Therefore, they could be coated on a flexible subsrate to serve as the semiconducting element in any flexible electronics application.

Finally, silicon nanowire based radial heterojunctions are proven to lead to significant developments in heterojunction solar cells. Silicon nanowire/PEDOT:PSS radial heterojunction model was very suitable in terms of energy band alignments and material processibility. In addition to this structure, there are many other materials that have a potential to serve well as a complementary thin film that can be coated onto silicon nanowire arrays. Theoretically, inorganic thin films such as ZnO and CdTe could be coated on p-type and n-type silicon nanowire arrays, respectively. These structures have potential to reveal great solar cell or photodiode characteristics.

REFERENCES

[1] Li X., and Bohn P. W., 2000, "Metal-assisted chemical etching in HF-H2O2 produces porous silicon," Applied Physics Letters, **77**(16), pp. 2572-2574.

[2] Peng K.-Q., Yan Y.-J., Gao S.-P., and Zhu J., 2002, "Synthesis of Large-Area Silicon Nanowire Arrays via Self-Assembling Nanoelectrochemistry," Advanced Materials, **14**(16), p. 1164.

[3] Bhushan B., 2007, "Springer Handbook of Nanotechnology," Springer 2nd Edition.

[4] Cao J. X., Gong X. G., and Wu R. Q., 2007, "Giant piezoresistance and its origin in Si(111) nanowires: First-principles calculations," Physical Review B, **75**(23), pp. 3-6.

[5] Bezryadin A., and Goldbart P. M., 2010, "Superconducting nanowires fabricated using molecular templates," Advanced Materials, **22**(10), pp. 1111-1121.

[6] Ding M., Kim H., and Akinwande A. I., 1999, "Observation of valence band electron emission from n-type silicon field emitter arrays," Applied Physics Letters, **75**(6), p. 823.

[7] Au F. C. K., Wong K. W., Tang Y. H., Zhang Y. F., Bello I., and Lee S. T., 1999, "Electron field emission from silicon nanowires," Applied Physics Letters, **75**(12), p. 1700.

[8] Thurn-Albrecht T., Schotter J., Kastle G. A., Emley N., Shibauchi T., Krusin-Elbaum L., Guarini K., Black C. T., Tuominen M. T., and Russel T. P., 2000, "Ultrahigh-Density Nanowire Arrays Grown in Self-Assembled Diblock Copolymer Templates," Science, **290**(5499), pp. 2126-2129.

[9] Huynh W. U., Dittmer J. J., and Alivisatos A. P., 2002, "Hybrid nanorod-polymer solar cells," Science, **295**(5564), pp. 2425-2427.

[10] Chang Y., and Sanders G. D., 1992, "Theory of optical properties of quantum wires in porous silicon," Physical Review, **45**(16), pp. 9202-9213.

[11] Parkash V., Member S., and Kulkarni A. K., 2010, "Optical Absorption Characteristics of Silicon Nanowires for Photovoltaic Applications," IEEE Proceedings, pp. 1-5.

[12] Kayes B. M., Atwater H., and Lewis N. S., 2005, “Comparison of the device physics principles of planar and radial p-n junction nanorod solar cells,” Journal of Applied Physics, **97**(11), p. 114302.

[13] Fan Z., Ruebusch D. J., Rathore A. A., Kapadia R., Ergen O., W P., and Javey A., 2009, “Challenges and Prospects of Nanopillar-Based Solar Cells,” Nano Res, **2**(11), pp. 829-843.

[14] Zhao X., Wei C. M., Yang L., and Chou M. Y., 2004, “Quantum Confinement and Electronic Properties of Silicon Nanowires,” Quantum, (June), pp. 1-4.

[15] Cui Y., and Lieber C. M., 2001, “Functional Nanoscale Electronic Devices Assembled Using Silicon Nanowire Building Blocks,” Science, **291**, pp. 851-853.

[16] Hochbaum A. I., 2008, “Enhanced Thermoelectric Performance of Rough Silicon Nanowires,” Nature, **451**, pp. 163-168.

[17] Boukai A. I., Bunimovich Y., Tahir-kheli J., Yu J. K., Goddard W. A., and Heath J. R., 2008, “Silicon Nanowires as Efficient Thermoelectric Materials,” Nature, **451**, pp. 168-171.

[18] Chan C. K., Peng H., Liu G., McIlwrath K., Zhang X. F., Huggins R. A., and Cui Y. I., 2008, “High-Performance Lithium Battery Anodes Using Silicon Nanowires,” Nature Nanotechnology, **3**, pp. 31-35.

[19] Chan C. K., Patel R. N., O Connell M. J., Korgel B. A., and Cui Y., 2010, “Solution-Grown Silicon Nanowires for Lithium-Ion Battery Anodes,” ACS Nano, **4**(3), pp. 1443-1450.

[20] Goldberger J., Hochbaum A. I., Fan R., and Yang P., 2006, “Silicon Vertically Integrated Nanowire Field Effect Transistors,” Nano, **6**(5), pp. 973-977.

[21] Schmidt V., Riel H., Senz S., Karg S., Riess W., and Gosele U., 2006, “Realization of a Silicon Nanowire Vertical Surround-Gate Field-Effect Transistor,” pp. 85-88.

[22] Bae J., Kim H., Zhang X. M., Dang C. H., Zhang Y., Choi Y. J., Nurmikko A., and Wang Z. L., 2010, “Si Nanowire Metal – Insulator – Semiconductor Photodetectors as Efficient Light Harvesters,” Nanotechnology, **21**, p. 095502.

[23] Qian F., Gradec S., and Lieber C. M., 2005, “Core / Multishell Nanowire Heterostructures as Multicolor , High-Efficiency Light-Emitting Diodes,” Nano Letters, **5**(11), pp. 2287-2291.

[24] Cui Y., Wei Q., Park H., and Lieber C. M., 2001, “Nanowire Nanosensors for Highly Sensitive and Selective Detection of Biological and Chemical Species,” Science, **293**(5533), pp. 1289-1292.

[25] Hu L., and Chen G., 2007, "Analysis of Optical Absorption in Silicon Nanowire Arrays for Photovoltaic Applications," Nano Letters, **7**(11), pp. 3249-3252.

[26] Sivakov V., Andra G., Gawlik A., Berger A., Plentz J., Falk F., and Christiansen S. H., 2009, "Silicon Nanowire-Based Solar Cells on Glass: Synthesis, Optical Properties, and Cell Parameters," Nano Letters.

[27] Yang Y., McDowell M. T., Jackson A., Cha J. J., Hong S. S., and Cui Y., 2010, "New Nanostructured Li2S/silicon Rechargeable Battery with High Specific Energy.," Nano Letters, **10**(4), pp. 1486-91.

[28] Park W. I., Zheng G., Jiang X., Tian B., and Lieber C. M., 2008, "Controlled synthesis of millimeter-long silicon nanowires with uniform electronic properties.," Nano letters, **8**(9), pp. 3004-9.

[29] Zimmler M. a, Bao J., Shalish I., Yi W., Yoon J., Narayanamurti V., and Capasso F., 2007, "Electroluminescence from single nanowires by tunnel injection: an experimental study," Nanotechnology, **18**(23), p. 235205.

[30] Huang C.-ying, Yang Y.-jay, Chen J.-ying, Wang C.-hsiung, Chen Y.-fang, Hong L.-sheng, Liu C.-sheng, and Wu C.-yin, 2010, "p-Si nanowires/SiO 2 /n-ZnO heterojunction photodiodes," pp. 2-4.

[31] Misra N., Martinez J. a, Huang S.-C. J., Wang Y., Stroeve P., Grigoropoulos C. P., and Noy A., 2009, "Bioelectronic silicon nanowire devices using functional membrane proteins.," Proceedings of the National Academy of Sciences of the United States of America, **106**(33), pp. 13780-13784.

[32] Westwater J., 1997, "Growth of silicon nanowires via gold/silane vapor–liquid–solid reaction," Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, **15**(3), p. 554.

[33] Wagner R. S., and Ellis W. C., 1964, "Vapor liquid solid mechanism of single crystal growth," Applied Physics Letters, **4**(5), pp. 89-90.

[34] Cheng G. S., Zhang L. D., Chen S. H., Li Y., Li L., Zhu X. G., Zhu Y., Fei G. T., and Mao Y. Q., 2011, "Ordered Nanostructure of Single-Crystalline GaN Nanowires in a Honeycomb Structure of Anodic Alumina," Journal of Materials Research, **15**(02), pp. 347-350.

[35] Yu D. P., Bai Z. G., Ding Y., Hang Q. L., Zhang H. Z., Wang J. J., Zou Y. H., Qian W., Xiong G. C., Zhou H. T., and Feng S. Q., 1998, "Nanoscale silicon wires synthesized using simple physical evaporation," Applied Physics Letters, **72**(26), p. 3458.

[36] Büttner C. C., Zakharov N. D., Pippel E., Gösele U., and Werner P., 2008, "Gold-enhanced oxidation of MBE-grown silicon nanowires," Semiconductor Science and Technology, **23**(7), p. 075040.

[37] Holmes J. D., 2000, “Control of Thickness and Orientation of Solution-Grown Silicon Nanowires,” Science, **287**(5457), pp. 1471-1473.

[38] Morales A. M., and Lieber C. M., 1998, “A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires,” Science, **279**, p. 7.

[39] Mart J., and Garcia R., 2010, “Silicon nanowire circuits fabricated by AFM oxidation nanolithography,” Small, **21**, p. 245301.

[40] Fu Y. Q., Colli A., Fasoli A., Luo J. K., Flewitt A. J., Ferrari A. C., and Milne W. I., 2009, “Deep reactive ion etching as a tool for nanostructure fabrication,” Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, **27**(3), p. 1520.

[41] Synthesis and galvanomagnetic properties,” Physical Review B, Heremans J., Thrush C., Lin Y.-M., Cronin S., Zhang Z., Dresselhaus M., and Mansfield J., 2000, “Bismuth nanowire arrays: **61**(4), pp. 2921-2930.

[42] Wang Z. L., Liu Y., and Zhang Z., 2002, “Handbook of Nanophase and Nanostructured Materials,” Springer Press.

[43] Y.-M. Lin, X. Sun, S. Cronin, Z. Zhang J. Y. Y. and M. S. D., 1999, “Fabrication and transport properties of Te-doped Bi nanowire arrays,” Molecular Electronics: MRS Symposium Proceedings, Boston.

[44] Zhang B. Z., Shimizu T., Chen L., Senz S., and Go U., 2009, “Bottom-Imprint Method for VSS Growth of Epitaxial Silicon Nanowire Arrays with an Aluminium Catalyst,” Advanced Materials, **21**, pp. 1-5.

[45] Chou S. Y., Krauss P. R., and Renstrom P. J., 1995, “Imprint of sub-25 nm vias and trenches in polymers,” Applied Physics Letters, **67**(21), p. 3114.

[46] Dimova-Malinovska D., Sendova-Vassileva M., Tzenov N., and Kamenova M., 1997, “Preparation of thin porous silicon layers by stain etching,” Thin Solid Films, **297**(1-2), pp. 9-12.

[47] Peng K., Xu Y., Wu Y., Yan Y., Lee S. T., and Zu J., 2005, “Aligned Single Crystalline Silicon Nanowire Arrays for Photovoltaic Applications,” Small, **1**(11), p. 1062.

[48] Qiu T., Wu X. L., Siu G. G., and Chu P. K., 2006, “Intergrowth mechanism of silicon nanowires and silver dendrites,” Journal of Electronic Materials, **35**(10), pp. 1879-1884.

[49] Peng K., Wu Y., Fang H., Xiaoyan Z., Xu Y., and Zhu J., 2005, “Uniform, Axial-Orientation Alignment of One- Dimensional Single-Crystal Silicon Nanostructure Arrays,” Angewandte Chemie International Edition, **44**, pp. 2737 -2742.

[50] Cheng S. L., Chung C. H., and Lee H. C., 2008, "A Study of the Synthesis, Characterization, and Kinetics of Vertical Silicon Nanowire Arrays on (001)Si Substrates," Journal of the Electrochemical Society, **155**(11), pp. 711-714.

[51] Chen C., Wu C., Chou C., and Yen T., 2008, "Morphological Control of Single-Crystalline Silicon Nanowire Arrays near Room Temperature," Advanced Materials, **20**, pp. 3811-3815.

[52] Peng K., Hu J., Yan Y., Wu Y., Fang H., Xu Y., Lee S., and Zhu J., 2006, "Fabrication of Single-Crystalline Silicon Nanowires by Scratching a Silicon Surface with Catalytic Metal Particles," Advanced Functional Materials, pp. 387-394.

[53] Kumar D., Srivastava S K., Singh P. K., Sood K N., Singh V N., Dilawar N. H. M., 2010, "Room temperature growth of wafer-scale silicon nanowire arrays and their Raman characteristics," Journal of Nanoparticle Research, **12**, pp. 2267-2276.

[54] Peng K., and Zhu J., 2004, "Morphological selection of electroless metal deposits on silicon in aqueous fluoride solution," Electrochimica Acta, **49**, pp. 2563-2568.

[55] Peng K., Fang H., Hu J., Wu Y., Zhu J., Yan Y., and Lee S., 2006, "Metal-Particle-Induced, Highly Localized Site-Specific Etching of Si and Formation of Single-Crystalline Si Nanowires in Aqueous Fluoride Solution," Chemistry a European Journal, **12**, pp. 7942 - 7947.

[56] Kang S. H., Pokroy B., Mahadevan L., and Aizenberg J., 2010, "Control of Shape and Size of Nanopillar Assembly by Adhesion-Mediated Elastocapillary Interaction," ACS Nano, **4**(11), pp. 6323-6231.

[57] Huang Z., Shimizu T., Senz S., Zhang Z., Zhang X., Lee W., Geyer N., and Gösele U., 2009, "Ordered arrays of vertically aligned [110] silicon nanowires by suppressing the crystallographically preferred <100> etching directions.," Nano Letters, **9**(7), pp. 2519-2525.

[58] Lee G., Lee I., Shim J., and Park J., 2010, "Single-Crystalline Si Nanowire on Pyramid with Extremely Low Reflectivity Independing on Light Incident Angle," The Electrochemical Society 218th ECS Meeting.

[59] Unalan H. E., Hiralal P., Rupesinghe N., Dalal S., Milne W. I., and Amaratunga G. a J., 2008, "Rapid Synthesis of Aligned Zinc Oxide Nanowires," Nanotechnology, **19**(25), p. 255608.

[60] Druzhinina T., Hoeppener S., and Schubert U. S., 2009, "On the Synthesis of Carbon Nanofibers and Nanotubes by Microwave Irradiation: Parameters, Catalysts, and Substrates," Advanced Functional Materials, **19**(17), pp. 2819-2825.

[61] Zhao F., Cheng G.-an, Zheng R.-ting, Zhao D.-dan, Wu S.-long, and Deng J.-hua, 2011, "Field emission enhancement of Au-Si nano-particle-decorated silicon nanowires," Nanoscale Research Letters, **6**(1), p. 176.

[62] Huang Z., Geyer N., Werner P., Boor J. de, and Gösele U., 2010, "Metal-Assisted Chemical Etching of Silicon: A Review," Advanced Materials, pp. 1-24.

[63] Chartier C., Bastide S., and Levyclement C., 2008, "Metal-assisted chemical etching of silicon in HF–H2O2," Electrochimica Acta, **53**(17), pp. 5509-5516.

[64] Srivastava S. K., Kumar D., Singh P. K., Kar M., Kumar V., and Husain M., 2010, "Solar Energy Materials & Solar Cells Excellent antireflection properties of vertical silicon nanowire arrays," Solar Energy Materials and Solar Cells, **94**(9), pp. 1506-1511.

[65] Garnett E., and Yang P., 2010, "Light Trapping in Silicon Nanowire Solar Cells.," Nano letters, pp. 6-11.

[66] Kelzenberg M. D., Boettcher S. W., Petykiewicz J. A., Turner-Evans D. B., Putnam M. C., Warren E. L., Spurgeon J. M., Briggs R. M., Lewis N. S., and Atwater H. A., 2010, "Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications," Nature Materials, **9**(3), pp. 239-244.

[67] Campbell P., and Green M. A., 1987, "Light Trapping Properties of Pyramidally Textured Surfaces," Journal of Applied Physics, **62**, pp. 243-249.

[68] Yablonovitch E., 1982, "Statistical ray optics," Journal of the Optical Society of America, **72**(7), p. 899.

[69] Milne W. I., Teo K. B. K., Amaratunga G. a J., Legagneux P., Gangloff L., Schnell J.-P., Semet V., Thien Binh V., and Groening O., 2004, "Carbon nanotubes as field emission sources," J. of Mater. Chem., **14**(6), p. 933.

[70] Zeng B., Xiong G., Chen S., Jo S. H., Wang W. Z., Wang D. Z., and Ren Z. F., 2006, "Field emission of silicon nanowires," Applied Physics Letters, **88**(21), p. 213108.

[71] Liu Y., and Fan S., 2005, "Field emission properties of carbon nanotubes grown on silicon nanowire arrays," Solid State Communications, **133**(2), pp. 131-134.

[72] Qinke S., Wei J., Wang K., Gui X., Ma C., Zhu H., Jia Y., Li X., Guo N., and Wu D., 2010, "Fabrication and field emission properties of multi-walled carbon nanotube/silicon nanowire array," Journal of Physics and Chemistry of Solids, **71**(4), pp. 708-711.

[73] Nai G. S., Meng F. Y., Au F. C. K., Li Q., Lee C. S., Bello I., and Lee S. T., 2002, "Fabrication and field emission of high density silicon cone arrays," Advanced Materials, (18), pp. 1308-1311.

[74] Wang Q., Li J. J., Ma Y. J., Bai X. D., Wang Z. L., Xu P., Shi C. Y., Yue S. L., and Gu C. Z., 2005, "Field emission properties of carbon coated Si nanocone arrays on porous silicon," Nanotechnology, **16**(12), pp. 2919-2922.

[75] Sun M., Gao Y., Zhi C., Bando Y., and Golberg D., 2011, "Silicon multi-branch nanostructures for decent field emission and excellent electrical transport.," Nanotechnology, **22**(14), p. 145705.

[76] Scribd http://www.scribd.com/doc/19346852/Solar-Cell (last visited on 01.07.2011), 2011, "Solar Cell."

[77] University of Delaware, 2010, "University Of Delaware-Led Team Sets Solar Cell Record (last visited on 04.07.2011)," Science, (July 2007).

[78] World Coal Institute (WCI), 2006, "Coal Facts," http://www.worldcoal.org (last visited on 04.07.2011).

[79] European Photovoltaic Industry Association (EPIA), 2009, "Global Market Outlook For Photovoltaics Until 2013," http://www.epia.org/fileadmin/EPIA_docs/publications/epia/Global_Market_Outlook_Until_2013.pdf (Last visited on 05.07.2011).

[80] International Energy Agency (IEA Publications), 2010, "Technology Roadmap Solar photovoltaic energy," http://www.iea.org/papers/2010/pv_roadmap.pdf (Last visited on 05.07.2011).

[81] National Renewable Energy Laboratory (NREL), "Air Mass 1.0 and 1.5 Spectra http://rredc.nrel.gov/solar/spectra/am1.5/ (Last Visited on 05.07.2011)."

[82] Bube R. H., and Fahrenbruch A. L., 1983, "Fundamentals of Solar Cells Photovoltaic Solar Energy Conversion," Academic Press.

[83] Li X., Li J., Chen T., Tay B. K., Wang J., and Yu H., 2010, "Periodically Aligned Si Nanopillar Arrays as Efficient Antireflection Layers for Solar Cell Applications.," Nanoscale Research Letters, **5**(11), pp. 1721-1726.

[84] Honsberg C., and Bowden S., 2008, "PV Education," http://www.pveducation.org/pvcdrom (last visited on 11.07.2011).

[85] "Solar Store http://www.solarstore.co.kr/bbs/board.php?bo_table=pro02 (Last Visited on 05.07.2011)."

[86] "Your Sun Your Energy http://www.yoursunyourenergy.com/Solar-cells.htm (Last visited on 05.07.2011)."

[87] "DIY Trade http://www.diytrade.com/china/4/products/5480436/a-si_thin_film_solar_cells.html (Last visited on 05.07.2011)."

[88] Poortmans J., and Archipov V., 2006, "Thin Film Solar Cells," John Wiley & Sons, New York USA.

[89] "UC of Santa Barbara - Department of geography News http://www.geog.ucsb.edu/events/department-news/723/inventor-of-dye-sensitized-solar-cells-awarded-millennium-technology-prize/ (Last visited on 05.07.2011)," Geography.

[90] Mario P., Palmisano G., and Ciriminna R., 2010, "Working principles of dye-sensitised solar cells and future applications http://www.physics.hku.hk/~phys0628/DSSC%20Working%20Principle.pdf (Last Visited on 05.07.2011)," Photovoltaics International.

[91] Niesar S., Dietmueller R., Nesswetter H., Wiggers H., and Stutzmann M., 2009, "Silicon/organic semiconductor heterojunctions for solar cells," Physica Status Solidi (a), **206**(12), pp. 2775-2781.

[92] Ay I., and Tolunay H., 2007, "The influence of ohmic back contacts on the properties of a-Si:H Schottky diodes," Solid-State Electronics, **51**(3), pp. 381-386.

[93] Wu D., Qin J., and Lin B., 2007, "Self-assembled epoxy-modified polymer coating on a poly(dimethylsiloxane) microchip for EOF inhibition and biopolymers separation," Lab on a Chip, **7**(11), pp. 1490-1496.

[94] Shiu S. C., Chao J. J., Hung S. C., Yeh C. L., and Lin C. F., 2010, "Morphology Dependence of Silicon Nanowire/Poly(3,4-ethylenedioxythiophene):Poly(styrenesulfonate) Heterojunction Solar Cells," Chemistry of Materials, **22**(6), p. 3108.

[95] Friedel B., Keivanidis P. E., Brenner T. J. K., Abrusci A., Mcneill C. R., Friend R. H., and Greenham N. C., 2009, "Effects of Layer Thickness and Annealing of PEDOT : PSS Layers in Organic Photodetectors," Macromolecules, **42**, pp. 6741-6747.

[96] Kim Y., Ballantyne A. M., Nelson J., and Bradley D. D. C., 2009, "Effects of Thickness and Thermal Annealing of the PEDOT : PSS Layer on the Performance of Polymer Solar Cells," Organic Electronics, **10**(1), pp. 205-209.