DESIGN AND IMPLEMENTATION OF LOW POWER INTERFACE ELECTRONICS FOR VIBRATION-BASED ELECTROMAGNETIC ENERGY HARVESTERS

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ABSTRACT

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For many years batteries have been used as the main power sources for portable electronic devices. However, the rate of scaling in integrated circuits and micro-electro-mechanical systems (MEMS) has been much higher than that of the batteries technology. Therefore, a need to replace these temporary energy reservoirs with small sized continuously charged energy supply units has emerged. These units, named as energy harvesters, use several types of ambient energy sources such as heat, light, and vibration to provide energy to intelligent systems such as sensor nodes. Among the available types, vibration based electromagnetic (EM) energy harvesters are particularly interesting because of their simple structure and suitability for operation at low frequency values (< 10 Hz), where most vibrations exits. However, since the generated EM power and voltage is relatively low at low frequencies, high performance interface electronics is required for efficiently transferring the generated power from the harvester to the load to be supplied.

The aim of this study is to design low power and efficient interface electronics to convert the low voltage and low power generated signals of the EM energy

harvesters to DC to be usable by a real application. The most critical part of such interface electronics is the AC/DC converter, since all the other blocks such as DC/DC converters, power managements units, etc. rely on the rectified voltage generated by this block. Due to this, several state-of-the-art rectifier structures suitable for energy harvesting applications have been studied. Most of the previously proposed rectifiers have low conversion efficiency due to the high voltage drop across the utilized diodes. In this study, two rectifier structures are proposed: one is a new passive rectifier using the Boot Strapping technique for reducing the diode turn-on voltage values; the other structure is a comparator-based ultra low power active rectifier. The proposed structures and some of the previously reported designs have been implemented in X-FAB 0.35 μm standard CMOS process. The autonomous energy harvesting systems are then realized by integrating the developed ASICs and the previously proposed EM energy harvester modules developed in our research group, and these systems have been characterized under different electromechanical excitation conditions. In this thesis, five different systems utilizing different circuits and energy harvesting modules have been presented. Among these, the system utilizing the novel Boot Strap Rectifier is implemented within a volume of 21 cm^3, and delivers 1.6 V, 80 μA (128 μW) DC power to a load at a vibration frequency of only 2 Hz and 72 mg peak acceleration. The maximum overall power density of the system operating at 2 Hz is 6.1 $\mu W/cm^3$, which is the highest reported value in the literature at this operation frequency. Also, the operation of a commercially available temperature sensor using the provided power of the energy harvester has been shown. Another system utilizing the comparator-based active rectifier implemented with a volume of 16 cm^3, has a dual rail output and is able to drive a 1.46 V, 37 μA load with a maximum power density of 6.03 $\mu W/cm^3$, operating at 8 Hz.

Furthermore, a signal conditioning system for EM energy harvesting has also been designed and simulated in TSMC 90 nm CMOS process. The proposed ASIC includes a highly efficient AC-DC converter as well as a power processing unit which steps up and regulates the converted DC voltages using an on-chip DC/DC converter and a sub-threshold voltage regulator with an ultra low power management

unit. The total power consumption on the totally passive IC is less than 5 μW, which makes it suitable for next generation MEMS-based EM energy harvesters.

In the frame of this study, high efficiency CMOS rectifier ICs have been designed and tested together with several vibration based EM energy harvester modules. The results show that the best efficiency and power density values have been achieved with the proposed energy harvesting systems, within the low frequency range, to the best of our knowledge. It is also shown that further improvement of the results is possible with the utilization of a more advanced CMOS technology.

Keywords: Vibration-based energy harvester; Electromagnetic power generation; High efficiency, low voltage AC-DC conversion; Low power interface IC design, on-chip power management design.

ÖZ

TİTREŞİME DAYALI ELEKTROMANYETİK ENERJİ ÜRETEÇLERİ İÇİN DÜŞÜK GÜÇLÜ ARAYÜZ ELEKTRONİK DEVRELERİNİN TASARIMI VE UYGULAMASI

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Uzun yıllardır, taşınabilir elektronik cihazlar için ana güç kaynağı olarak piller kullanılmaktadır. Ancak, entegre devreler ve mikro-elektro-mekanik sistemlerin (MEMS) ölçekleme oranındaki gelişmeler pil teknolojilerininkinden çok daha hızlı ilerlemiştir. Bu nedenle, pil gibi geçici enerji rezervuarlarını sürekli olarak enerji üreten küçük boyutlu modüllerle değiştirme ihtiyacı ortaya çıkmıştır. Enerji üreteçleri olarak adlandırılan bu modüller, ortamdaki ısı, ışık ve titreşim gibi enerji kaynaklarını kullanarak duyarga ağları gibi akıllı sistemlere enerji sağlarlar. Mevcut enerji üreteçleri arasında elektromanyetik (EM) üreteçler basit yapıları ve pek çok titreşimin bulunduğu düşük frekans değerlerinde (<10 Hz) çalışmaya uygunlukları nedeniyle ön plana çıkmaktadırlar. Ancak, düşük frekanslı titreşimlerden üretilen EM gerilim ve güç düşük olduğu için, üretilen enerjinin sürülen yüke verimli bir şekilde iletilebilmesi için yüksek performanslı arayüz elektroniği devreleri gerekmektedir.

Bu çalışmanın amacı, EM enerji üreteçlerinde üretilen düşük voltaj ve güçteki sinyalleri gerçek uygulamalarda kullanılabilecek doğru akıma çeviren düşük güçte

çalışan verimli bir arayüz elektroniği tasarlamaktır. Bu tür elektronik devrelerin en önemli elemanı AC/DC (Alternatif Akım / Doğru Akım) doğrultuculardır. Çünkü devrenin, DC/DC (Doğru Akım - Doğru Akım) çeviricisi, güç yöneticisi gibi diğer tüm bloklarının performansı AC/DC doğrultucuda üretilen doğru akıma bağlıdır. Bu sebeple, üreteci uygulamaları için uygun olan birçok doğrultucu üzerinde çalışılmıştır. Daha önceden tasarlanmış doğrultucular, kullanılan diyotların üzerinde oluşan yüksek gerilim kayıpları nedeni ile düşük verimde çevirme oranına sahiptirler. Bu çalışmada iki tip doğrultucu yapısı önerilmiştir: bunların ilki diyotların açılma gerilimlerinin düşmesini sağlayan "Boot Strapping" tekniğini kullanan yeni bir pasif doğrultucudur; diğeri ise karşılaştırıcı yapısı üzerine kurulu ultra düşük güç harcayan aktif doğrultucudur . Önerilen bu yapılar ve daha önceden rapor edilmiş birkaç başka tasarım X-FAB 0.35 µm standart CMOS teknolojisinde üretilmiştir. Daha sonra bağımsız enerji üretim sistemleri, üretilen entegre devre ve daha önce araştırma grubumuz tarafından geliştirilmiş EM enerji üreteçleri kullanılarak gerçeklenmiş ve farklı elektromekanik uyarma koşulları altında karakterize edilmişlerdir. Bu tezde, farklı devrelerden ve enerji üretçlerinden oluşan beş farklı sistem sunulmuştur. Bunlar arasında, 2 Hz frekansta ve 72 mg tepe ivmelenmesinde çalışan, "Boot Strap" doğrultucu kullanan 21cm^3 hacmindeki özgün sistem, bağlanan yüke1.6 V, 80 µA (128 µW) doğru akım gücü iletebilmektedir. 2 Hz çalışma frekansında sisteminin maksimum güç yoğunluğu 6.1 µW/cm^3'dür ki bu da bu çalışma frekansı için literatürde rapor edilmiş en yüksek değerdir. Ayrıca piyasada bulunan bir sıcaklık duyargasının, bu enerji üretecinden sağlanan güç ile sürülebileceği gösterilmiştir. Karşılaştırıcı yapısı içeren aktif doğrultucu kullanan diğer bir sistem ise 16 cm^3 hacimde 8 Hz çalışma frekansında çift çıkışlı 1.46 V, 37 µA'lik bir yük sürebilmektedir ve bu sistemin maksimum güç yoğunluğu da 6.03 µW/cm^3'tür.

Bunların yanıda, EM enerji üreteci için bir sinyal iyileştirme sistemi de TSMC 90 nm CMOS teknolojisi kullanılarak tasarlanmıış ve simule edilmiştir. Önerilen entegre, yüksek verimli bir AC/DC doğrultucu ve doğrultulan gerilimi çip üzerinde DC-DC çeviricisi ve voltaj regülatörü kullanarak yükseltecek ve regüle edecek ultra düşük güç yönetimi ünitesi içermektedir. Bu pasif entegre devrenin toplam güç

tüketimi 5 μW'tan azdır ve bu değer yeni nesil MEMS tabanlı EM enerji üreteçleri ile beraber kullanım için uygundur.

Bu çalışma kapsamında, yüksek verimlilikteki CMOS doğrultucu entegre devreleri tasarlanmış ve birkaç titreşim tabanlı EM enerji üreteci modulü ile birlikte test edilmiştir. Sonuçlar, sunulan enerji üreteç sistemlerinin düşük frekanslarda bilinen en verimli sistemler olduğunu ve en yüksek güç yoğunluklarına sahip olduklarını göstermektedir. Buna ek olarak, daha gelişmiş bir CMOS teknolojisi kullanarak tasarlanacak devrelerle daha iyi sonuçlara ulaşılabileceği de gösterilmiştir.

Anahtar kelimeler: Titreşim-tabanlı enerji üreteci; Elektromanyetik (EM) güç üretimi; Yüksek verimli, düşük voltajlı analogtan dijtale çevirici (AC-DC); Düşük güçlü entegre devre tasarımı, çipte güç yönetimi tasarımı

To My Parents

and

To Melina

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CHAPTER 1

INTRODUCTION

The wireless systems technology with a wide variety of applications in portable and implantable devices has been rapidly growing during recent years. The advances in Microelectronics and Micro Electromechanical Systems (MEMS) technology have allowed the realization of portable low power and low cost micro sensors and actuators which find many applications in our daily life. Some of these applications are biomedical implants for health care and monitoring systems, industrial like structural health monitoring sensor networks, and in automotive industry as in tire pressure monitoring systems. The main power sources for these portable electronic devices are batteries; however, the improvement in the battery technology is not as fast as the Microelectronics and Integrated Circuits technology [1] . While these systems scale down, the lack of compact and efficient power sources has become a limitation in enabling the increased utilization of them in wireless applications; since, the use of bulky batteries as well as their frequent replacement in such systems is impractical. Therefore, there is a widespread need for compact and efficient energy harvesting devices that are lifetime, low cost, and environmental friendly to power the portable systems. Fortunately, the reduced power demand in new generation integrated circuits has allowed the use of energy harvesters as primary power sources in those small systems. As a result, temporary energy reservoirs like batteries can be replaced with energy storage elements in such systems, which are continuously being charged using the ambient energy sources.

Although, many efforts have been done to design and implement mechanical transducers to harvest energy from ambient energy sources, only a few studies try to

improve the performance of interface electronics for energy harvesters. This is particularly important due to the low voltage and low power characteristics of the harvested energy.

This thesis aims to design ultra low power interface electronics to convert the low voltage and low power generated signals of the electromagnetic energy harvesters to DC to be usable by a real application. This chapter gives an introduction on the energy harvesting motivation and required interface electronics with a focus on vibration-based electromagnetic energy harvesting systems. Section 1.1 describes the available ambient energy sources and different methods of energy transduction and their potential to be usable as a power source. Section 1.2 explains the operation principle of electromagnetic energy harvesters, and a state-of-the-art review of the technology. Sections 1.3 explains the typical interface electronics for vibration-based energy harvesters with each subsection describing the specific design considerations for most commonly available types including piezoelectric, electrostatic, and electromagnetic energy harvesters. Section 1.4 provides a comprehensive list of goals and achievements to be considered by this thesis study, and Section 1.5 ends the chapter by giving the outline of the thesis including a summary of contents.

1.1 Ambient Energy Sources and Energy Harvesters

The most commonly available ambient energy sources are heat, light, and vibration [2] - [4]. Table 1.1 presents the energy sources, transduction methods, and power density of the most recent energy harvester modules ([5], [6]). The power density of the energy sources has been compared for 1-year and 10-year lifetime in separate columns. In the case of ambient energy sources, the power density stays the same for long lifetime due to the availability of the free source in the nature through the time; however, it significantly decreases for the capacitive sources using electrochemical transduction (last three rows). The other disadvantages of these limited sources are relatively low power density, need for replacement, and the environmental issues associated with disposal; making them not suitable for long lifetime operation in portable and wireless systems.

Table 1.1: Comparison of energy scavenging sources, their transduction mechanism, and power density.

Energy Source	**Transduction Mechanism**	**Power Density ($\mu W/cm^3$) 1-year lifetime**	**Power Density ($\mu W/cm^3$) 10-year lifetime**
Solar	Photovoltaic	15,000 $_{sunny}$ 150 $_{cloudy}$	15,000 $_{sunny}$ 150 $_{cloudy}$
Vibration	**Piezoelectric Electrostatic Electromagnetic**	**4-800**	**4-800**
Temperature Gradient	Thermoelectric	60 @ 5ºC gradient	60 @ 5ºC gradient
Radio Frequency @ 2.4 GHz [35]	Electromagnetic Induction	400 @ 1 m 15.8 @ 5 m	400 @ 1 m 15.8 @ 5 m
Fluid Flow	Wind, Wave	air: 200-800 water: 500 mW/cm^3	-
Batteries (Lithium) (non-rechargeable)	Electrochemical	89	7
Batteries (Lithium) (rechargeable)	Electrochemical	13.7	0
Fuel Cells (methanol)	Electrochemical	560	56

Photovoltaic solar cells are good alternatives for long lifetime operation with a high power density compared with other ambient energy sources, but the amount of sunlight highly depends on the geographic location and is not always available especially for indoor applications. A thorough description, operation principle, and comparison of ambient sources and energy harvesters can be found in [4]. Among these energy sources, vibration is particularly attractive due to its abundance. Some vibration sources in the environment are vehicle motion, human movements, and seismic vibrations that widely vary in frequency and amplitude. However, most of these vibrations occur at low frequencies (<10 Hz), leading to low power levels at the output, introducing some challenges in the efficient system design.

In vibration-based energy harvesters, the relative displacement of a mechanical structure leads to generation of electrical energy. Energy can be harvested from

these vibrations by using different methods such as piezoelectric, electrostatic, and electromagnetic transduction. In electromagnetic energy harvesters, the relative motion of a magnet with respect to a coil induces a voltage across the coil based on Faraday's law of induction. In piezoelectric scavengers, the vibration results in a strain and stress over the piezoelectric material, and this generate an output voltage across its terminals. In electrostatic harvesters, the vibration leads to movement of plates of a variable, previously charged capacitor, and an output voltage variation is generated. The micro fabrication of them is easily achievable due to the availability of variable capacitors using MEMS technology.

Piezoelectric and electrostatic energy harvesters can provide high output voltages; however, most of the reported modules operate at high excitation frequency range, which makes them not suitable for ambient low frequency applications [7]. Although there are electrostatic and piezoelectric energy harvesters reported in the literature that can provide considerably high output voltages at low operation frequencies [8] - [12]; they have high output impedance values, and thus require extra impedance matching networks, resulting in additional design complexity and power losses.

On the other hand, electromagnetic energy harvesters are inherently better candidates for the applications at low frequency range (1-10 Hz) due to the presence of a magnet which acts as a mass, decreasing the resonance frequency. They have low output impedance (few Ω's to kΩ's), easier to implement, and do not rely on extra components such as electrets or external voltage supplies as in the case of electrostatic harvesters. However, the electromagnetically generated peak voltage is relatively low for vibrations at low frequency leading to some challenges in the efficient design of their interface circuitry.

1.2 Electromagnetic Energy Harvesting

In electromagnetic energy harvesters, the electrical energy is generated by the relative motion between a permanent magnet and a moving coil and a voltage is induced across the coil based on Faraday's law of induction:

$$\varepsilon(t) = -\frac{d\phi}{dt} = -\frac{d\left(\sum_{i=1}^{n}\left(\vec{B}.\vec{A}_i\right)\right)}{dt} \tag{1.1}$$

where ε is the electromotive force induced voltage, Φ is the magnetic flux density, B is the magnetic field strength of the utilized magnets, A_i is the area of each coil turn, t is time, and n is the total number of coil turns. The operation principle representation of the generator is shown in Figure 1.1.

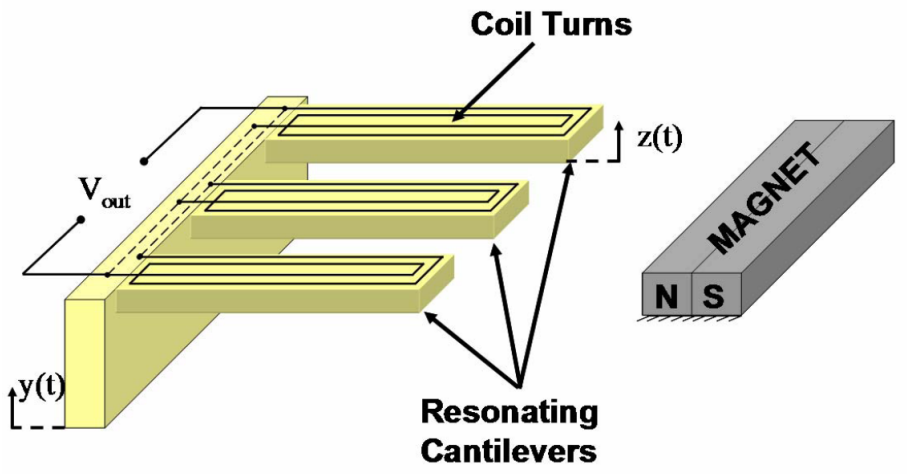


Figure 1.1: The operation principle of electromagnetic energy harvesters [13].

The relatively simple structure of these energy harvesters may allow the realization of macro model devices in which each mechanical parameter could be easily varied in order to see the direct effect of it on the output voltage and power ([14], [15]). Most of the reported electromagnetic energy harvester modules operate at vibration frequencies larger than 50 Hz in order to achieve high power density levels. Hami *et al.* introduced a resonant energy harvester that is able to produce 2208 μW/cm^3 AC power density at a resonance frequency of 322 Hz [16]. This power level is obtained only when the input frequency is matched with the resonance frequency. Ching *et al.* presented a multimodal resonant energy harvester with an *rms* power density of 830 μW/cm^3, yet the vibration frequency ranged between 60–110 Hz [17]. Beeby *et al.* fabricated a cantilever and coil-based electromagnetic energy harvester with optimized magnet geometry, which can generate 306 μW/cm^3 at 52 Hz input vibration [18].

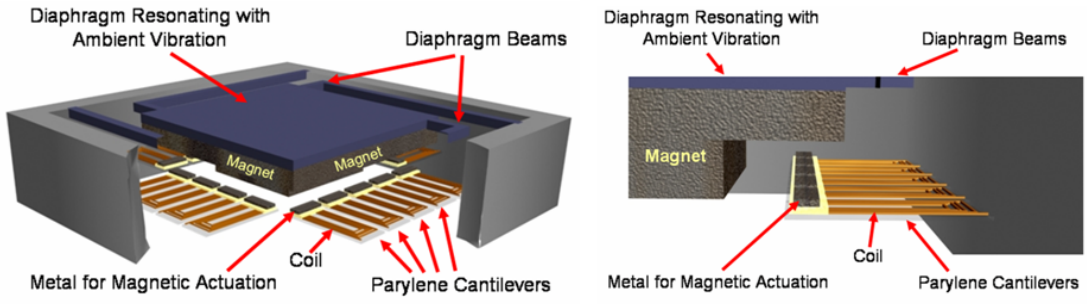


Figure 1.2: The frequency up-conversion based electromagnetic micro generator [19].

It is observed from the reported energy harvesters that the power density of the device tends to diminish as the operation frequency and the device volume decrease. However, it's desired to power the portable and wireless applications using efficient energy harvesters which operate at low frequencies as the frequencies in the nature are in the range of 1–10 Hz. In addition, small size is also essential for these applications. Several attempts have been made to increase the output power of these generators while keeping the operation frequency at a low level ([20] - [22]). A novel method, called frequency up-conversion, utilizing the magnetic pull force between a permanent magnet and a magnetic material to up-convert the operation frequency of the harvester, has been proposed by Kulah and Najafi [20]. In this method, the magnet moving on a diaphragm with the ambient vibration frequency periodically catches and releases a magnetic piece which is placed on a cantilever for up-converting the vibration frequency, hence increasing the energy harvesting efficiency. The reported energy harvester prototype has a power density of 0.05 $\mu W/cm^3$ within a practical prototype volume of about 2.3 cm^3, operating at 1 Hz input vibration frequency. A micro fabricated version of this device is also reported by Sari *et al*. [21] (Figure 1.2). In [22], another method called *mechanical* frequency up-conversion has been proposed which eliminates the use of an extra magnet for realizing the up-conversion. The reported power density of the energy harvester prototype is 184 $\mu W/cm^3$ for a device volume of 2.96 cm^3 operating under 10 Hz vibration frequency. The frequency-increased generation technique has been used in [23] to harvest low frequency vibrations (Figure 1.3). In this design, a power generation magnet has been placed on a diaphragm having a resonance frequency higher than the ambient vibrations. At presence of low frequency ambient

vibrations, the inertial mass vibrates and touches and releases the magnet on the diaphragm, resulting in a high frequency oscillation at the output. The device with a volume of 43 cm^3 is able to generate a peak power of 57 μW under a 2 Hz vibration frequency.

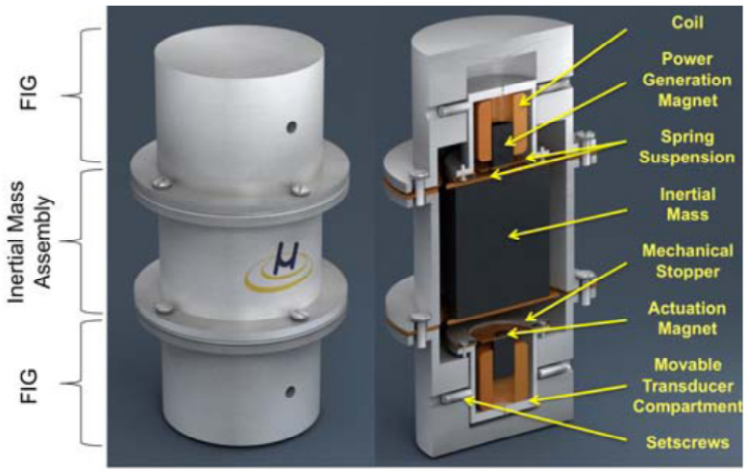


Figure 1.3: The reported frequency-increased generator for low frequency harvesting [23].

The above electromagnetic energy harvesters do not consider the interface electronics and report the mechanical transducer design and measure the generated AC voltage. They use a load resistance equivalent to the resistance of the utilized coils and report the AC generated power. These studies tend to overestimate the available power to a realistic load, since they ignore the potentially high losses associated with the power processing network to rectify the generated power and make it usable by a real device. On the other hand, the primary disadvantage of the electromagnetic energy harvesters is the relatively low generated voltage levels compared to similar size piezoelectric and electrostatic energy harvesters. This adds to the importance of the interface electronics to be high performance, enabling the electromagnetic energy harvesters as a feasible power source for powering the sensor networks.

1.3 Interface Electronics for Vibration-based Energy Harvesters

There are different approaches that will be briefly introduced in this section, which are followed in the design of the interface electronics for piezoelectric, electrostatic, and electromagnetic energy harvesting devices. However, the interfacing electronics

are all composed of similar blocks in the system level. The generic interface electronics for vibration-based energy harvesters is depicted in Figure 1.4. It includes an AC-DC power converter as the foregoing block; since the generated voltage is alternating and needs to be converted to a DC voltage. The power processing unit includes post-DC-conversion blocks such as DC-DC converters to step up the primary converted DC voltage, and voltage regulators to control and smooth the converted DC voltage. The energy storage element could be a rechargeable battery, a super capacitor, or any other storage component. The power management unit is required before delivering the converted voltage to the load which decides whether to provide power for the output load based on the input conditions. For instance, it disconnects the path to the load whenever input power is not available or not sufficient to drive the load; letting the storage capacitors be charged up to a desired threshold and connects the path afterward. The main consideration in designing each block is to consume as low power as possible such that the total power consumption of the interface circuitry is much lower than the input harvested power.

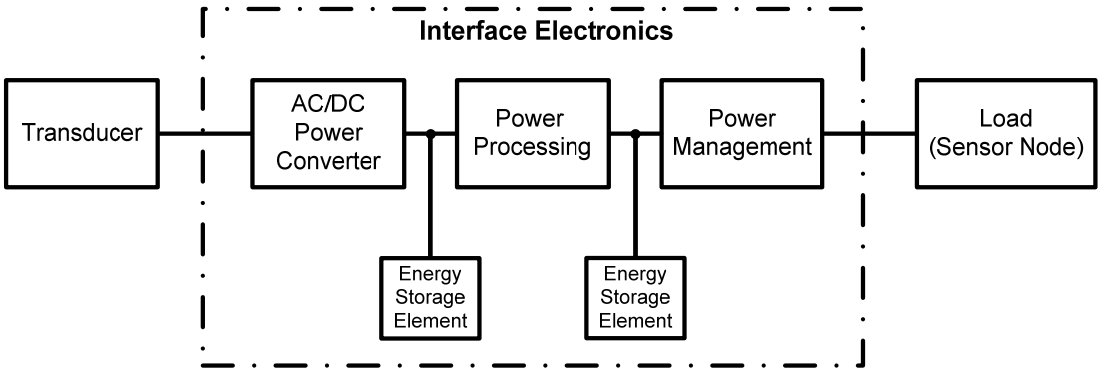


Figure 1.4: The generic interface electronics for vibration-based energy harvesting.

1.3.1 Interface Electronics for Piezoelectric Energy Harvesters

Piezoelectric energy harvesters can naturally provide high output voltages depending on the amplitude and frequency of excitation and membrane characteristics. Therefore, there are many types of interface electronics which are reported for power conversion of these energy harvesters. The primary disadvantage of them is the relatively high output impedance (in the range of MΩ's) which is generally much

higher than the input impedance of the upcoming interface circuitry, not allowing the direct connection of them to the network. The model of a piezoelectric device together with the conventional piezo voltage doubler is depicted in Figure 1.5 [24] where the piezoelectric device is modeled as a current source in parallel with its output impedance. The source current should charge and discharge the C_P at each period of the input; so, a high portion of the current is wasted for this operation, because C_P is large. In this design, a switch-based converter has been proposed for piezoelectric energy harvesters, in which a switch makes a short circuit path between terminals of the device once in each period. This increases the charging rate of C_P while the switch is ON; therefore, much higher amount of source current is used to charge the output instead of the internal capacitor, which increases the performance and the converted output power significantly.

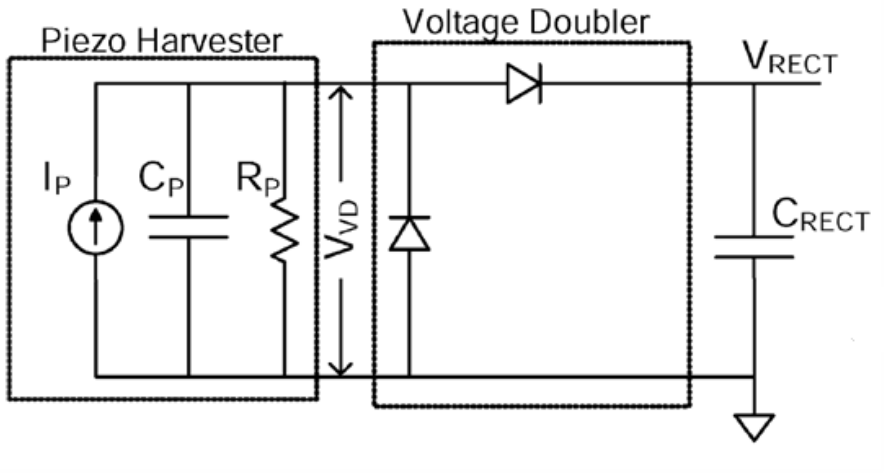


Figure 1.5: The piezoelectric energy harvester model, and the conventional piezo voltage doubler [24].

In [25], an adaptive method has been proposed which continuously transfers the maximum power from the harvester to the load. The design needs extra components and driving instruments for controlling the Pulse Width Modulation (PWM) DC-DC converter and is complicated. In [26], a piezoelectric energy harvesting system is proposed which uses the conventional Villard multipliers using the custom ultra low threshold-voltage diodes. In [27], simpler types of passive and active rectifiers are proposed for a resonant piezoelectric membrane. An impedance matching network has been used for interfering with the electronics. It is stated that active rectification is a possible solution for high efficiency power conversion where an efficiency of

more than 90% has been achieved for load currents greater than 5 μA. A passive rectifier using boot-strap technique has also been reported in [27] which utilizes the internal capacitance of the piezoelectric device in one half of a period to store voltage, leading to a full wave passive rectifier where a maximum efficiency of 70% is achieved.

1.3.2 Interface Electronics for Electrostatic Energy Harvesters

The electrostatic energy harvesters generate peaks of DC voltages and therefore; they don't require a rectifier, which is a very power hungry component. Their main drawback is the very huge generated voltages (e. g. 300 V) which are much higher than the breakdown voltage of standard CMOS processes when they work in the constrained-charge mode, making them not compatible with standard processes. An alternative way is to operate them in voltage-constrained mode where their output voltage is clamped to a battery voltage and is constant. In this mode, the resulting harvested charge is transferred to the battery using a control unit as shown in Figure 1.6. The reported power electronics for these devices generally use a rechargeable battery as the storage element and transfer the charge by clamping the output voltage to the constant voltage of the battery ([28], [29], [30]).

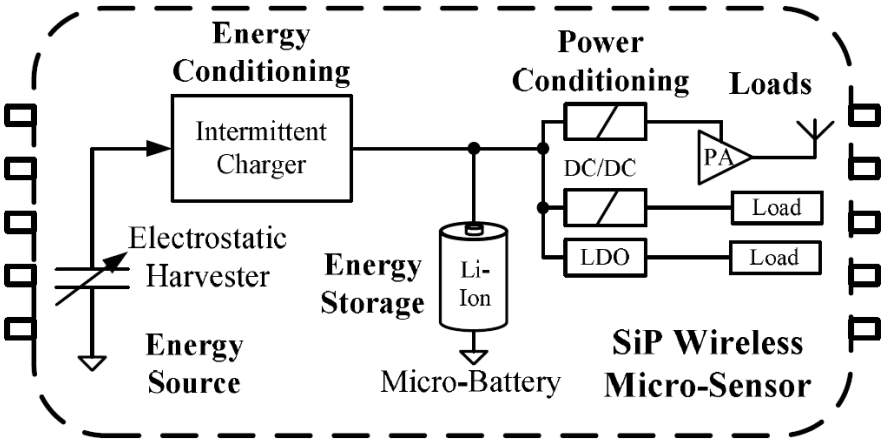


Figure 1.6: Typical interface circuitry for electrostatic energy harvesters [30].

1.3.3 Interface Electronics for Electromagnetic Energy Harvesters

Most of the related publications in the literature report the electromagnetic transducer design and optimization and do not consider the design of interface electronics and

power conversion. Some of the published works use simple bridge rectifiers and smoothing capacitors which are integrated with electromagnetic energy harvesters [4], [5]. The system performance of these designs is low due to the low conversion efficiency of the interface electronics, even though the transducer is optimized.

There are a few examples in the literature that combine an electromagnetic energy harvester with more sophisticated customized power electronics for a full-system solution. In [31] an electromagnetic energy harvesting system is proposed which uses a diode bridge rectifier and PWM DC-DC converter. The converted DC voltage is boosted using a feed-forward and feedback PWM boost converter (Figure 1.7). The maximum output power of 4 mW has been achieved; however, the volume of the system is large and it operates at 41 Hz. This is not suitable for ambient low frequency energy harvesting applications. Furthermore, the designed interface electronics needs an extra 3.3 V supply which not only increases the system volume, but is costly and needs periodic replacement.

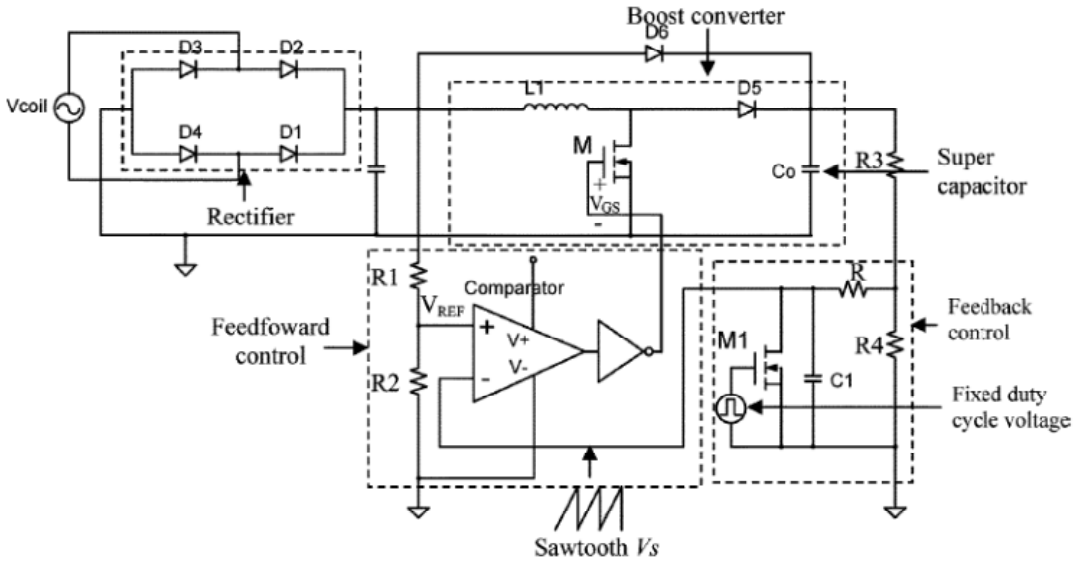


Figure 1.7: The proposed PWM method for electromagnetic power conversion in [31].

In [32], conventional Villard multipliers are used to convert and boost the generated voltage of the energy harvester which is based on Frequency-Increased Generation technique operating at 2 Hz. The design uses low efficiency conventional interface

electronics and has similar size as the one in [31], yielding a lower system power density.

The state-of-the-art electromagnetic energy harvesting systems are usually large and have low power density due to poor power conversion efficiency. Also, most of the previously reported works are not suitable for ambient vibrations due to the high resonance frequency and narrow band operation. There is an imminent need for a compact energy harvesting System-on-Package (SoP) that comprises of an energy harvester module and integrated interface electronics which can efficiently rectify low AC voltage levels with low power from low frequency vibrations to guarantee the maximum power transfer from the harvester to the load.

1.4 Objectives of the Thesis

The aim of this thesis is to design and implement low power and high efficiency interface electronics to be used for power extraction and conversion from vibration-based electromagnetic energy harvesters operating at minimum vibration frequency. A comprehensive list of objectives of this thesis is as following:

1. Study and characterization of the required blocks for the design of high efficiency interface electronics for vibration-based electromagnetic energy harvesters.

2. Design and implementation of a highly efficient interface electronics including different types of rectifiers, optimized for the demanded applications. These rectifiers include a passive rectifier to convert the low power generated voltages of the electromagnetic energy harvesters to DC without using any extra battery and active rectifiers with a very high conversion efficiency at low AC voltage levels.

3. Implementation of platforms for testing the fabricated ASICs by integrating the energy harvester modules and the fabricated interface electronics as a complete System-on-Package in order to realize autonomous systems that are able to harvest energy under low frequency vibrations and convert it to a usable signal for powering an external application.

4. Design of an energy harvesting IC in an advanced low threshold (LVT) CMOS technology as interface for next generation MEMS-based electromagnetic energy harvesters. This circuitry includes a highly efficient AC/DC converter as well as a power processing unit which steps up, regulates, and manages the power transfer between the interface electronics and the load.

1.5 Outline of the Thesis

The rest of this thesis is divided into 5 chapters, beginning from Chapter 2 describing the detailed theory and analysis of all the building blocks of the interface electronics. The state-of-the-art designs for each block as well as a brief literature review for each block is explained in this chapter.

Chapter 3 describes the design and simulation results of the passive and active rectifier blocks which are implemented in a 0.35 μm CMOS process to be integrated with the energy harvester modules. The detailed design considerations and optimization techniques are also discussed in this chapter.

Chapter 4 introduces the design and simulation results of the interface ASIC in a 90nm CMOS process which includes some blocks that cannot be implemented in the previous technology for the required system specifications. The low-voltage and low-power scheme is the main consideration in design of this ASIC. The maximum efficiency and best achievable performance results using this technology is also given.

Chapter 5 gives the experimental results of the fabricated ASIC in 0.35 μm CMOS process including different designed circuits. The integration of the blocks in the fabricated ASIC with several electromagnetic energy harvester modules has also been done and the realized system prototypes are tested. In the end, the performance comparison of the proposed energy harvesting systems with the ones available in the literature has been presented.

Chapter 6 ends this thesis by summarizing the achievements during this study and showing the path of future research under the thesis subject.

CHAPTER 2

INTERFACE ELECTRONICS FOR ENERGY HARVESTERS

The aim of an energy harvesting system is to power up an applicable load such as a sensor node which generally needs a DC power supply. Therefore, the interface electronics is required to be integrated with energy harvesters to convert the alternating generated voltage to a smooth and usable voltage. Most of the past studies have used a simple matched resistive load at the output of the harvester modules, and reported the generated AC power delivered to this load. However, there are potentially high losses associated with the power conversion network which is comparable to the amount of harvested power, recognizing the importance of interface electronics. The reported energy harvesters including rectifying electronics are mostly piezoelectric transducers, as their output voltage is relatively high [24] - [27]. On the other hand, there are few examples in the literature that combine an EM energy harvester with customized power electronics for a full-system solution [31] - [32]. Furthermore, the rectification efficiency of these systems is low due to the voltage drops across the utilized diodes, as these systems employ conventional passive rectifiers.

This chapter explains the operation principle, analysis, and literature review of all the building blocks that are required for the interface electronics of a vibration-based energy harvester. The important design considerations which are taken into account for the vibration-based energy harvesters are also discussed. Section 2.1 gives the overview of the blocks that are discussed in this chapter by introducing the operation of each block and explaining how it relates to other blocks in the system. Section 2.2

describes the operation of passive and active rectifiers which are used in AC-DC converters and the state-of-the-art rectifiers which are proposed for low power energy harvesting applications. Section 2.3 explains different types of DC-DC converters and the specific design requirement for on-chip and low voltage energy harvesting interface electronics. It also introduces the charge-pumps which are an important family of on-chip DC-DC converters and gives the simple theory and some state-of-the-art charge-pump designs. Section 2.4 gives the concept of voltage regulation and the limitations with the conventional voltage regulator designs. It also introduces the alternative designs which are proposed for the ultra low power voltage regulator blocks. Section 2.5 states the idea of on-chip power management and its importance in power harvesting applications. Section 2.6 summarizes this chapter and gives a short view of the next chapter.

2.1 System Level Overview

Figure 2.1 shows the system level overview including the building blocks of a typical vibration-based energy harvesting interface electronics.

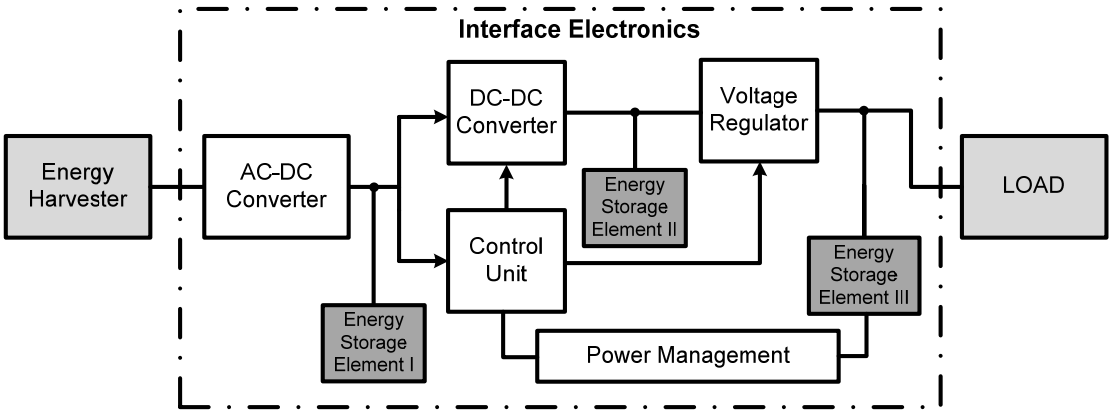


Figure 2.1: System level overview of the interface electronics for vibration-based energy harvesters

The AC-DC converter is the first block in a vibration-based energy harvesting system which converts the AC voltage to DC and stores it on the first storage capacitor (energy storage element I). The DC-DC converter is required to change the level of converted DC voltage depending on the peak value of the input AC signal and input mechanical excitation. For electromagnetic energy harvesters, it's

generally required to boost the DC voltage to a value greater than the maximum input peak voltage due to the small AC generated voltages in order to deliver a higher amount of DC output to the load than the input peak voltage. Energy storage element II stores the output voltage of DC-DC converter. The final block is the voltage regulator block which guarantees the stability of the desired voltage level at the output to be delivered to the load which is independent of input excitations. Due to the varying input characteristics, a power management block is also needed to shut down the load whenever the load power demand is higher than the harvested power. This will continue by the time that enough voltage is stored on the output capacitor, then, the power management block will connect the load to the interface electronics. Energy storage element III stores the permanent voltage of the harvesting system and is normally selected to be larger than other two capacitors to store more energy. The control unit includes the circuits which are used to operate the other blocks such as an oscillator which is used to drive the DC-DC converter and the control scheme which is required to manage their operation. Also, a voltage reference will be generated inside this block which will be used for the voltage regulator block.

2.2 The AC-DC Converters

The core of the AC-DC converters is a rectifier which rectifies the cycles of an alternating input voltage or current such that the rectified waveform is able to charge an output capacitor, yielding a DC voltage. There are two types of rectifiers: passive rectifiers and active rectifiers. Passive rectifiers are generally composed of diode bridges. A half-wave or full-wave diode bridge can simply rectify the AC signals and is generally used for AC-DC converters. However, due to the low voltage and low power characteristics of the signals to be rectified in energy harvesting applications, the voltage drop and power dissipation of the utilized diodes become a critical design consideration. Therefore, either low V_{TH} diodes available in special semiconductors technologies could be used or circuit techniques are required to be employed in standard design processes for increasing the performance of power conversion. For the cases, where the peak of the signal to be rectified is low, active rectifiers may also be preferred, however, as the name implies, these rectifiers should be supplied with and external power supply. This may still be acceptable for some energy harvesting applications where the converted DC supply could also be used for

powering the active block; however it still needs a pre-charged or rechargeable battery. Another scheme which is proposed in this study is to use a passive block to drive the active rectifier and use the active circuit as the main AC-DC converter. This is explained in more detail in section 3.4.

2.2.1 Passive Rectifiers

Passive rectifiers are circuits that rectify the AC voltages based on a diode-based operation, simply a diode bridge rectifier where no external power supply is required. In IC design, diode-connected transistors are normally used for on-chip diode operation. The very simple rectifier is a half-wave diode rectifier in which positive peaks of input signal is passed through the diode and negative peaks are lost. An improvement is the simple full-wave bridge rectifier (FWBR) which is most commonly used in the literature in which four diodes are employed in a bridge, realizing the full-wave rectification. Due to the high voltage drop across the diodes and low power conversion efficiency, Schottky diodes with smaller threshold voltage are employed for some energy harvesting applications; however it introduces another problem related with their high reverse current which affects the total performance. This effect is studied in an interface electronics design for a piezoelectric energy harvester in [33].

An improved version of the FWBR is the gate cross coupled rectifier (GCCR) which is proposed to increase the converted power from inductive RF energy harvesters [34]. Both FWBR and GCCR structures are shown in Figure 2.2. In GCCR topology, a pair of diode-connected transistors in FWBR is replaced with a pair of cross-connected NMOS transistors, where the first pair of transistors rectifies the input AC voltage and the second pair passes the rectified current through its drain-source. These two circuits are in more detailed explained in section 3.2.

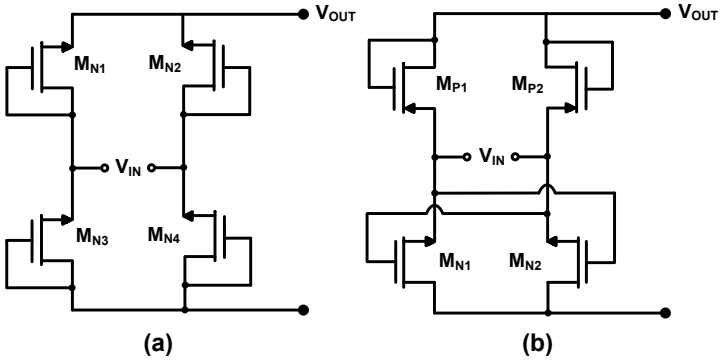


Figure 2.2: The schematics of (a) full-wave bridge rectifier (FWBR), and (b) gate cross coupled rectifier (GCCR).

In integrated circuits design, techniques could be used to alleviate the threshold voltage of the diode-tied transistors to increase the performance of rectification without using an external battery. One of these techniques is utilized in [27] where a passive rectifier based on boot-strap technique is proposed for piezoelectric energy harvesters. The advantage is to use modified diode blocks within the architecture which is the same conventional topology based on the operation principle of the piezoelectric devices and has been previously explained in section 1.3.1. Figure 2.3 shows the schematic where the diodes, D_1 and D_2 are reduced turn-on voltage diodes which are used in a full-wave configuration. At negative peaks of input voltage, the bottom part of the circuit in Figure 2.3 (b) (D_2 in Figure 2.3 (a)) clamps the input to ground to charge up the internal capacitor of the piezoelectric device, and D_1 rectifies and stores the voltage on the output capacitors. A modified version of this rectifier has been proposed in this study and will be explained in next chapter.

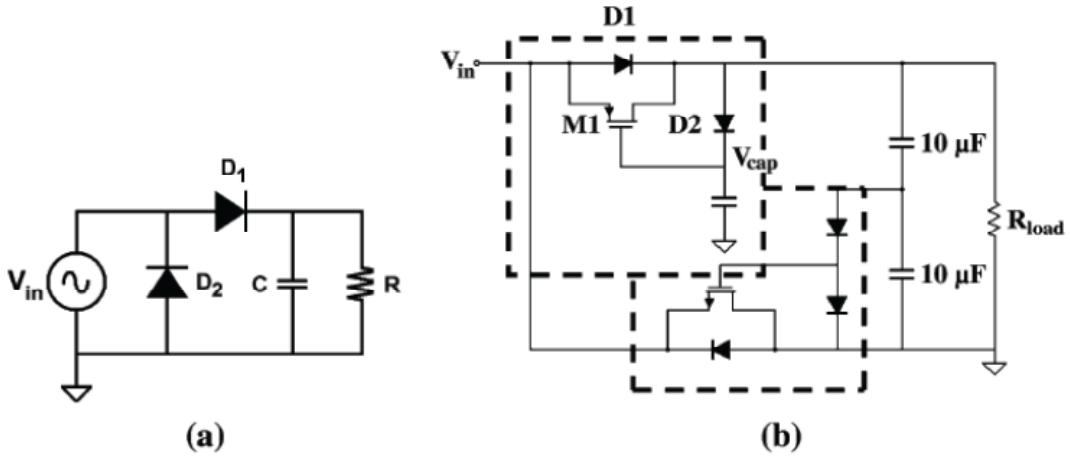


Figure 2.3: The full-wave passive rectifier for piezoelectric energy harvesters [27].

A passive method for increasing the power extraction from wirelessly powered devices by decreasing the voltage drop across the rectifying transistors has been proposed in [35]. Figure 2.4 shows the schematic in which M_1 and M_2 are gate-cross-coupled transistors which pass the current which is rectified by other two modified diode blocks. The transistors M_1 and M_4 contribute during rectification by closing the current from the input source to the output capacitor at one peak of the input voltage. At positive peaks, when the negative terminal of the input source goes lower than ground, transistor M_8 starts conducting and connects the gate of M_6 to ground, forcing it to turn on, because its source terminal is connected to V_{In+}. Therefore, the gate of M_4 will also be connected to the positive terminal of input source and starts conducting and closing the current path. As a result, two drain-to-source voltage drops are replaced with two threshold voltage drops in this configuration compared to a diode bridge rectifier, and the output voltage at positive peaks is:

$$V_{Out} = V_{In} - (V_{DS,M_1} + V_{DS,M_4}) \tag{2.1}$$

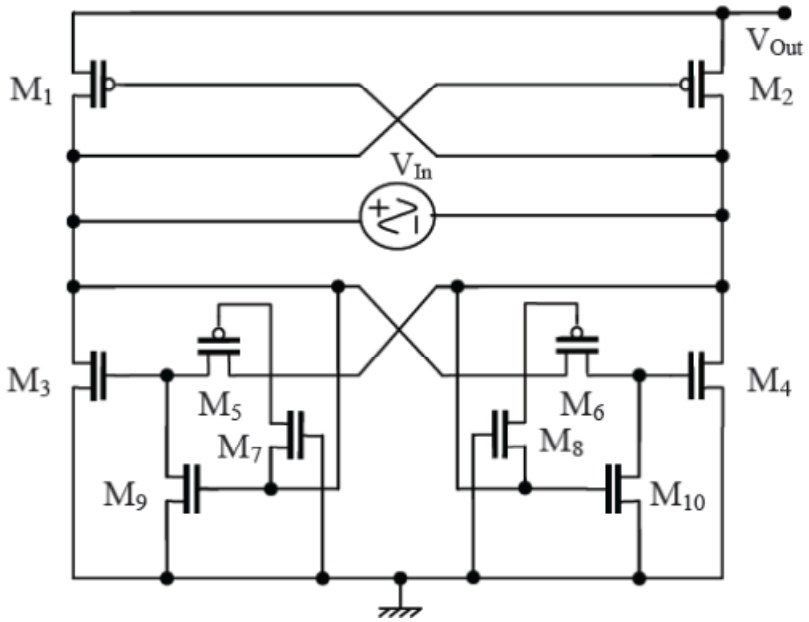


Figure 2.4: The passive full-wave rectifier for wirelessly powered devices in [35].

This design shows a power conversion efficiency greater than 90% for high input voltage peaks [35]. However, it cannot provide high efficiency at low input voltages due to its operation principle which is explained as following: Although the voltage

drops across the transistor channels is decreased, since the utilized controlling transistors (M_5 - M_{10}) need a minimum threshold voltage difference to turn on and drive the pass transistors, M_3 and M_4 in Figure 2.4; this design cannot operate for very low input voltages (lower than V_{TH}) and it has a very low performance for low voltage ranges (< 2 V) according to [35]. However, it has an improved performance for high input voltage peaks compared to conventional passive rectifiers. Therefore, based on the reported works, there is a major missing point in the literature for high efficiency, low voltage passive rectification.

2.2.2 Voltage Multipliers

The voltage multiplier circuits are networks of passive components such as diodes and capacitors which convert the input AC signals to DC and multiply it stage by stage. Their advantage is the simple structure and easily integrated to any system to generate and step up the DC voltages from input AC signals without using any magnetic component. However, its main limitation is very low power conversion efficiency due to the threshold voltage of the utilized diodes, which depends on the number of stages. Two voltage multiplier architectures which have been widely used in the literature are Dickson and Villard voltage multipliers.

Figure 2.5 depicts the two stages of Dickson voltage multiplier which has been extensively used in the literature, especially for RF energy harvesting [55] - [57]. By increasing the number of stages, higher DC voltage could be converted at the cost of losing power.

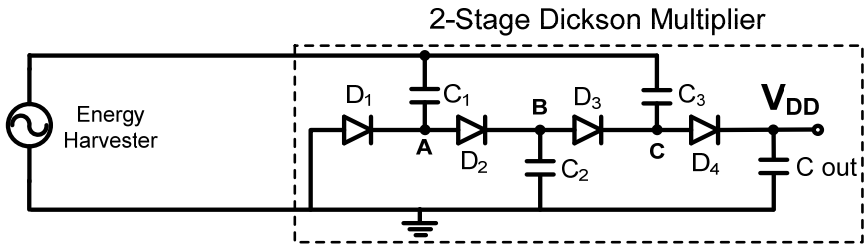


Figure 2.5: The two stage Dickson multiplier.

The operation principle could be explained as the following: In Figure 2.5, C1 and C3 are the AC bypass capacitors and C_2 and C_{out} store the DC voltage. If C_1 is chosen large enough to filter DC, node A follows the AC input signal. Capacitor C_2

and diode D_2 form a half-wave rectifier such that the DC voltage after the first stage at node B is,

$$V_B = V_{IN-peak} - V_{th} \tag{2.2}$$

where V_{th} is the threshold voltage of the utilized diodes. Similarly, the voltage at node C is the sum of the DC voltage from node B and the amplitude of the input AC. The V_{DD} voltage is then,

$$V_{DD} = 2 \times (V_{IN-peak} - V_{th}) \tag{2.3}$$

As it can be seen from equation (2.3), low threshold-voltage diodes are needed to increase the output DC voltage and the power conversion efficiency. Since they are not available in the utilized CMOS process, several methods have been proposed to increase the performance of this multiplier using special technologies. In [56], a Dickson multiplier with 16 stages have been proposed for RF to DC conversion, where special type Zero-V_T transistors available in TSMC 0.25 µm CMOS, are used. The circuit is able to generate up to 4 V from 150 mV AC peak voltages with 11.4 % power conversion efficiency.

The second widely used multiplier is the Villard type as shown in Figure 2.6. The peak of the input AC voltage is stored over the capacitors and is stepped up in each stage similar to previous discussion on Dickson multiplier.

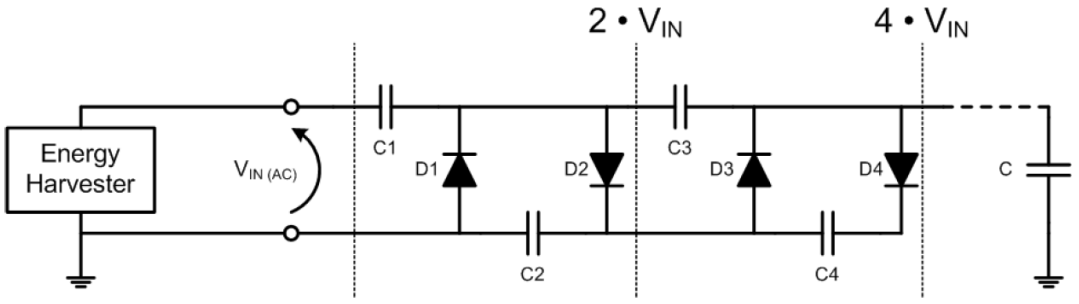


Figure 2.6: The 4-stage Villard multiplier [59].

2.2.3 Active Rectifiers

The main job of a rectifier is to turn on the charging path from the input to the output whenever the input AC voltage is higher than the output DC. Active rectifiers simply use a comparator and a switch to monitor the input and output and charge the output at the times that $V_{in} > V_{out}$. Higher conversion efficiency can be achieved with active rectifiers, due to the much smaller drop voltages compared to passive rectifiers. However, due to the cost and size of the required extra battery, they may not be suitable for energy harvesting applications where the realization of a fully self-powered system is intended.

In [27], an active rectifier which is utilized in a voltage doubler configuration is proposed for piezoelectric energy harvesters. The conversion efficiency of more than 90% is achieved for load currents above 4 μA while the active power consumption is 165 nW. The more efforts have been done to boost the performance of active rectifiers by modifying the switching schemes, switch transistor optimization and comparator design. In [36], a full-wave rectifier which uses a pair of gate-cross-coupled transistors and a pair of active diodes, is presented. In this design, a 4-input comparator is used with a reverse current control (RCC) scheme to turn on the active diode exactly at the time that input goes higher than output (Figure 2.7). Therefore, the conversion efficiency is improved by improving the switching times of the active block. A conversion efficiency of about 90% is achieved for input peak voltages higher than 2 V.

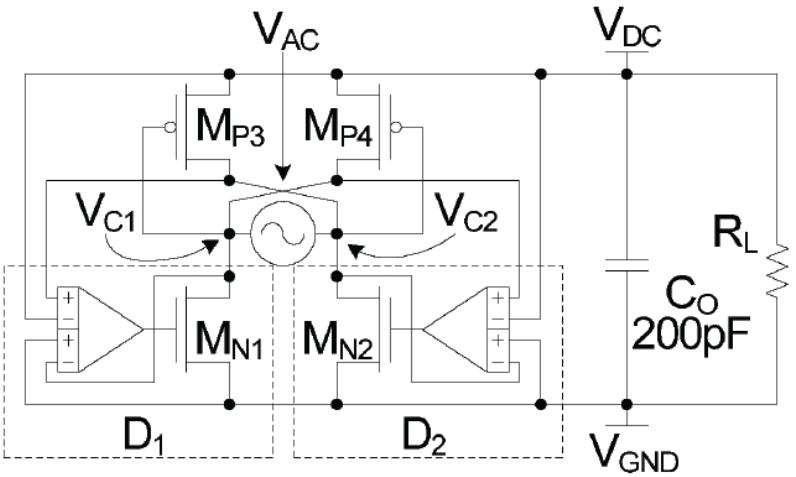
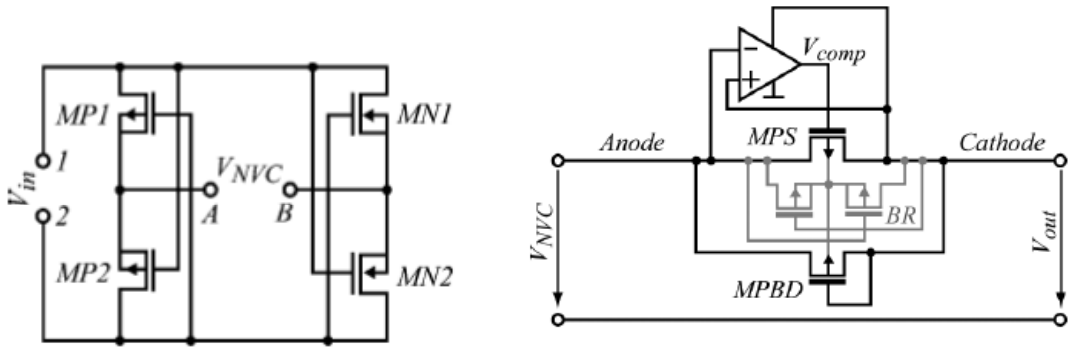


Figure 2.7: The 4-input comparator-based active rectifier utilizing RCC switching [36].

The power consumption of the active rectifier must be as low as possible in order to achieve a high system efficiency which is more explained in section 5.5.5. Due to the need for a double comparator rectifier for full-wave rectification, the required power consumption is double of a comparator. Another approach for an active rectifier which is full wave while utilizing only one active rectifier is proposed in [37] and [38]. In this design, a negative voltage converter (V_{NVC} in Figure 2.8 (a)) firstly, converts the negative peaks of the input voltage to positive in a gate-cross-coupled configuration. However, this voltage cannot be used to charge up an output capacitor since it is not rectified and backward reverse current discharges the output capacitor. Therefore, by using an active rectifier using single switch as in Figure 2.8 (b), it's possible to charge the output capacitor and store the DC voltage from positive peaks. Although, this design benefits from the low voltage drop and high conversion efficiency for high AC input voltage peaks (> 2 V), it has the same problem as the proposed passive design in Figure 2.4 for lower AC peaks. This is due to the fact that a minimum voltage peak ($V_{IN} > V_{TH}$) is required to turn on the transistors in Figure 2.8 (a) such that those transistors conduct and the whole circuit operates. Therefore, it still cannot have high conversion efficiency for low AC input peaks (< 1 V) which is the case for electromagnetic energy harvesters.



(a) (b)

Figure 2.8: The negative voltage converter utilizing active switch in [37].

2.3 DC-DC Converters

DC-DC converters are the second critical blocks in the interface electronics design for energy harvesting applications, as they change the level of converted DC voltage to a desired value. They may be boost (step up) or buck (step down) converters, depending on the level of the input AC peak voltage and the converted DC voltage of the rectifier stage. Several switching converter designs are reported in the literature; however, only a few of them are targeted to operate efficiently in low power conditions. Conventional DC-DC converters based on inductors are not suitable for energy harvesting applications due to the high power losses which are much higher than the harvested power. Switching DC-DC converters based on charge-pumps are good candidates to be used in low power and low voltage applications as they are not depending on the inductors and can be easily integrated into a chip. A good converter design must have a high power efficiency across a wide range of DC input voltages. The typical efficiency of the converters operating in low power range of 20 μW is above 60% [39] - [43].

2.3.1 Switching DC-DC Converters

The switching DC-DC converters can widely be categorized into two bunches: inductive-based and capacitive-based converters. Inductive-based converters normally use a modulation technique to charge the inductor and use the stored current to boost the DC voltage over a capacitor. On the other hand, capacitive-based converters generally use a switching scheme to change the level of DC voltage by transferring the charge between capacitors.

2.3.1.1 Inductive-based Switching Converters

The inductive-based converters use an LC network and operate based on tracking the input voltage by using a Pulse Width Modulation (PWM) technique to regulate the output voltage, as is shown in Figure 2.9. The voltage boosting operation of the inductive converter can be explained in two phases: (1) the inductor, L_1, charges up from the voltage source whenever the switch transistor is on, and (2) the stored current is transferred into the output capacitor, boosting its voltage, when the switch is off. The V_{REF} is the feedback voltage that monitors the input voltage. The

comparator turns on the switch transistor whenever the sawthooth voltage goes higher than the V_{REF}. Therefore, the V_{GS} of the switch is modulated and a regulated output voltage is converted at the load side. This converter is capable of driving load currents in the range of a few hundred micro-amperes to amperes. The inductor size required to realize a highly efficient LC based converter at light loads is too large (typically in the range of 100 nH to 1 μH) to have an integrated on-chip solution [39].

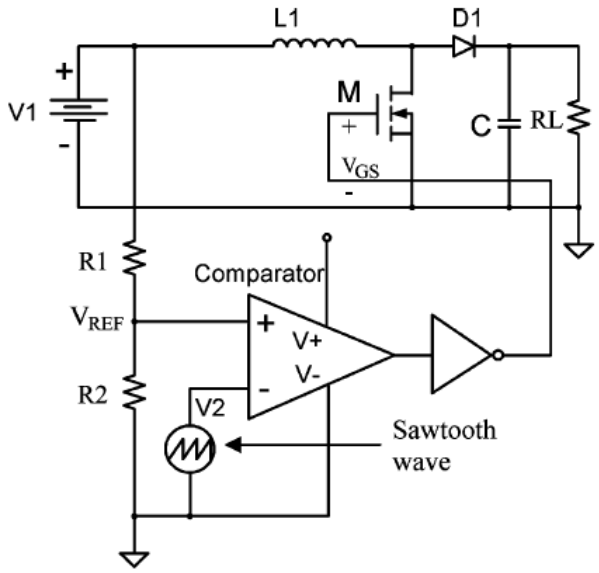


Figure 2.9: The schematic of the PWM switching converter using feedforward control [31].

2.3.1.2 Capacitive-based Switching Converters

The capacitive-based solution operates on the principle of charge transfer between capacitors to build the required output voltage. Their main advantage is the integration capability into a silicon chip, due to the availability of on-chip capacitors in standard processes. This type of converter is mainly used in applications requiring a lower load current which is within the range of tens of micro-amperes to a few hundred milli-amperes.

Figure 2.10 shows the schematic of the 4-stage switched capacitor DC-DC converter proposed in [44]. It works in two operating phases. Firstly, when CLK is high, the top NMOS switches and bottom transmission gates turn on, making all the capacitors parallel to each other and connected to V_{rect}. In the second phase, when CLK goes

low, the capacitors are in series and a voltage close to $4\times V_{rect}$ is stored at the output. A 1 V output voltage is generated using this converter for an input power of about 25 µW. At a 10% duty cycle, a 0.9 V output across a 5 MΩ load is generated which delivers 162 nW of DC power to the load from 2.5 mW of input power.

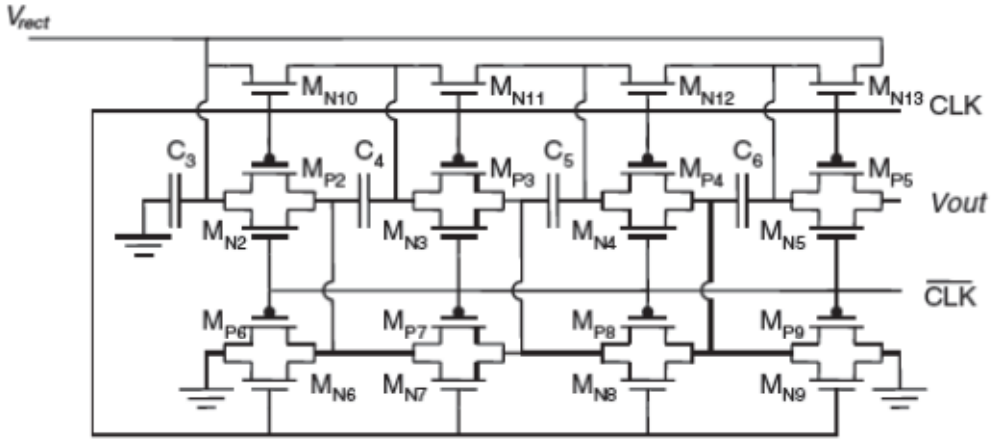


Figure 2.10: The switched capacitor DC-DC converter proposed in [44].

There are more different networks for realizing a switched capacitor converter: Ladder, Dickson, Fibonacci, Doubler and the Series-Parallel network. Extensive analysis and comparison of these different topologies is done in [43], where an optimization technique using cost metrics involving optimal area and total capacitively stored energy is also presented.

2.3.2 Charge-pump DC-DC Converters

The charge-pump circuits are type of switched capacitor converters that work on the principle of charge sharing between the input and output capacitors during non-overlapping clock phases. Their main advantage is that they do not rely on inductors and as a result; they could be implemented on chip via CMOS technology. For vibration-based energy harvesters, charge-pumps could be used in order to get rid of the input transformer in low voltage applications, which makes the design fully integrated.

Different types of charge-pumps have been introduced in the literature. The first proposed charge-pump circuit is the simple Dickson design [45] (Figure 2.11). The

operation is based on pumping the charge to the next stage such that in every stage, ideally, one step up of the input voltage is reached. The efficiency of the Dickson charge-pump is low due to the power losses over the utilized diodes because of their non-zero threshold voltage. Dickson has shown that ideally output current is independent of the number of stages [46]:

$$I_{Out} = f \times (C_{pump} \times C_{stray}) \times V_L \tag{2.4}$$

where, f is the clock frequency, C_{pump} is the intentional coupling capacitance, C_{stray} is the stray capacitance per node, and V_L is the voltage by which capacitors are charged and discharged.

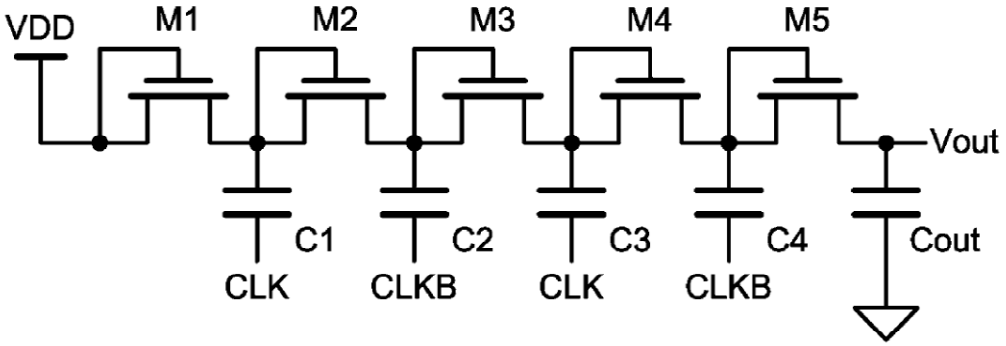


Figure 2.11: The conventional Dickson charge-pump [45].

It's also possible to show that output voltage depends on many parameters as:

$$V_{Out} = V_{In} + N\left[\left(\frac{C}{C + C_s}\right) \times V_{CLK} - V_{TH}\right] - V_{TH} - N.\left(\frac{I_{Out}}{(C + C_s).f}\right) \tag{2.5}$$

where N is the number of stages, V_{CLK} is the clock amplitude, and V_{TH} is the forward bias diode voltage. The voltage swing at each stage of a Dickson charge pump is:

$$\Delta V = \left(\frac{C}{C + C_s}\right) \times V_{CLK} - \left(\frac{I_{Out}}{(C + C_s).f}\right) \tag{2.6}$$

Therefore, by selecting C >> C_s, the full term can be approximated as V_{CLK}, when C is significantly larger than C_S and I_{out} is small. The fundamental problem related with the Dickson charge-pump is the increase in the V_{TH} of the utilized diodes due to

the significant body effect at higher stages, when bulk of the NMOS transistors are grounded. Voltage gain at stage N is:

$$Voltage\ gain = \Delta V - V_{TH}(N) \tag{2.7}$$

where V_{TH} (N) is the diode threshold voltage at stage N. Therefore, for *T* stage Dickson charge pump, the output voltage is,

$$V_{Out} = \sum_{N=1}^{T} (V_{in} - V_{TH}(N)) \tag{2.8}$$

Therefore, this type of charge-pump circuit is not suitable for low voltage applications due to the high power losses. There are many efforts which have been done to boost the performance of the charge-pump circuits. These methods include the 4-phase charge pump utilizing the 4-phase clocking scheme, the modified 4-phase charge pump, the boosted pump clock scheme, a CTS scheme, and several hybrid versions of these combinations, to get around problems of V_{TH} dependence and to increase the circuit efficiency for chips operating below 2.5 V supply voltages. A wide discussion on charge-pumps theory, different types of charge-pumps and their design considerations has been brought in [47].

In the conventional 4-phase charge pumps, the pumping gain can be increased by increasing the source to gate voltage drop using the special 4-phase clocks, so the gain degradation due to threshold voltage can be alleviated. Also a 2x–4x boosted pump clock source is often used as an easy way to increase efficiency and obtain higher output voltages.

In the CTS scheme, an additional pass transistor is added for each stage; the gate of the pass transistor is controlled by the next stage voltage, which is in opposite phase. In [48] an inductor-based charge-pump circuit has been proposed to boost the voltages from very small levels down to 0.2 V. The charge-pump structure is the same to previously reported designs; however, it uses a pass transistor with a series inductor connected to V_{DD} (Figure 2.12). When the clock changes its state, the current through the inductor cannot change instantaneously and therefore, spikes of

higher voltages will be generated depending on the value of inductance. This leads in generation of higher voltages than input supply at the cost of an off-chip inductor.

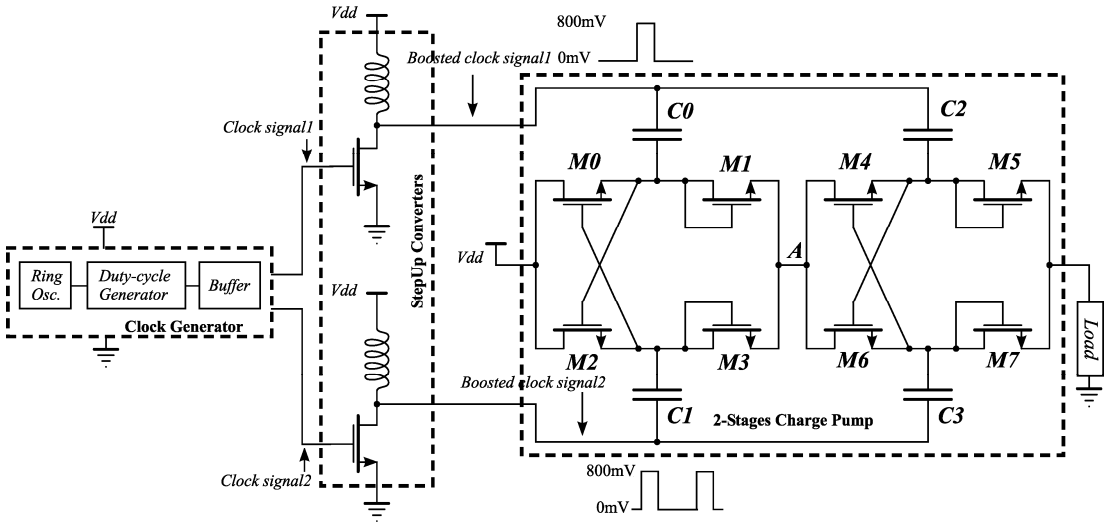


Figure 2.12: The structure of the inductor-based charge-pump circuit for low voltage applications [48].

Due to the body effect related with NMOS switches, lower conversion efficiency is achieved in the circuits which use NMOS transistors. In [48], an all PMOS approach has been proposed for a charge-pump circuit which utilizes two auxiliary PMOS transistors for diminishing body effect and 4-phase clocking. The conversion efficiency of 70% is achieved for a load current of 15 µA with a 4-stage charge-pump.

A major improvement to degrade the effect of V_{TH} in a conventional charge-pump circuit is to use CMOS cross-connected design as in [49]. In this design, the threshold voltage of the diode-connected transistors is replaced with the sum of drain-to-source voltages of a PMOS and NMOS transistor, which is typically much lower than V_{TH}. The body effect problem related with transistors in higher stages, is also solved using this topology, since the performance is related to V_{DS} and not directly dependent to V_{TH}. This circuit has been implemented in a 0.35 µm CMOS process and show a significant improvement in the amount of output voltage over previously reported charge-pump circuits. An optimized version of this design has been simulated in 90nm CMOS process and is explained in section 4.4.

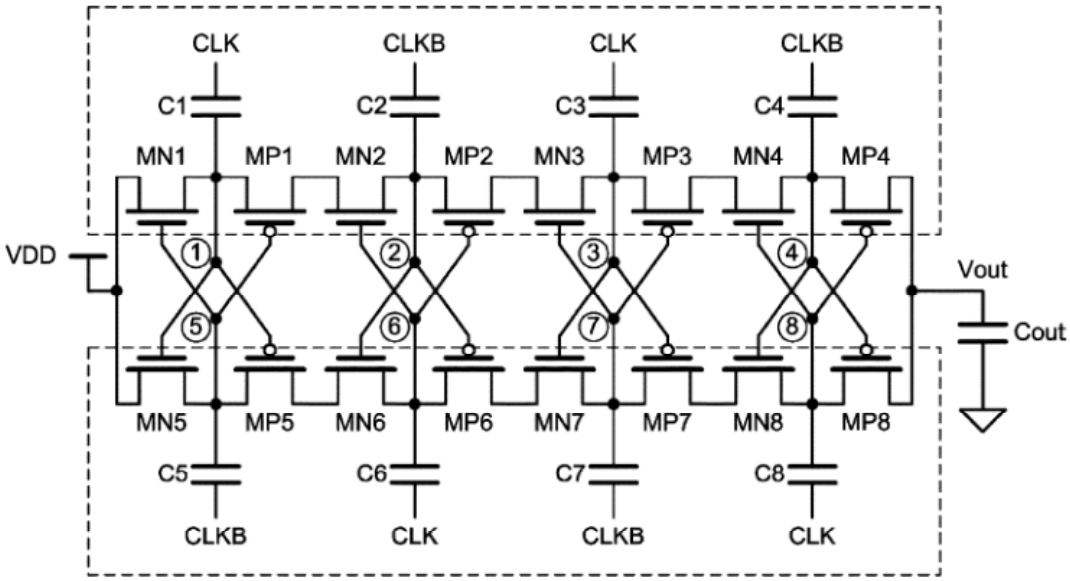


Figure 2.13: The cross-connected CMOS charge-pump for low voltage applications [49].

2.4 Voltage Regulators

A voltage regulation block is required for achieving a constant and reliable output DC to be delivered to the load. There are several methods of voltage regulation to be discussed in this section. Among them, the most important design consideration for an energy harvesting application is to be as low power as possible. In other words, the quiescent power which is consumed by the voltage reference block and the regulator block should be much lower than the harvested power. Therefore, many conventional voltage regulators which consume milli watts of power or hundreds of micro watts could not be used for energy harvesting applications.

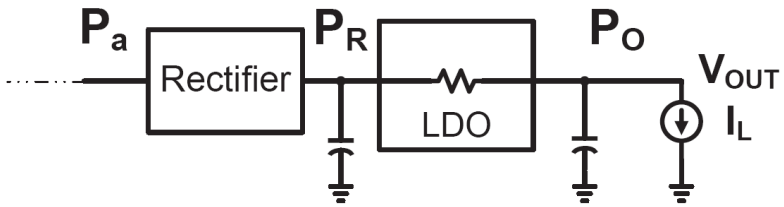
2.4.1 Linear Voltage Regulators

The simplest available regulator is a DC-DC linear voltage regulator, which regulates any input voltage higher than the required output voltage to a targeted stable DC output voltage. The voltage difference between the input and the output, referred to as the dropout voltage, is dissipated as heat across a pass transistor (Figure 2.14 (a)) in the output signal path. This internal power loss makes the linear regulator the most inefficient power converter when used in a system where the required output voltage is significantly lower than the input voltage. Figure 2.14 (b) shows the schematic of the LDO, where a comparator compares the generated voltage of a

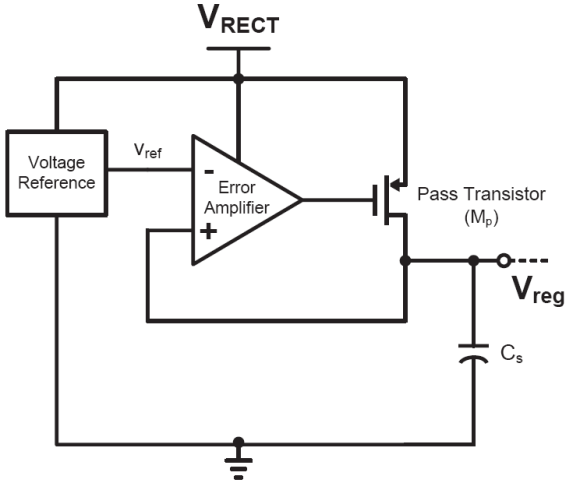
voltage reference with output and drives the pass transistor. The voltage gain of the linear regulator is,

$$LDO\,Voltage\,Gain = \frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_{out} + V_{do}} < 1 \tag{2.9}$$

where V_{out}, V_{in}, and V_{do} are the output, input and dropout voltages of the regulator, respectively. Therefore, the regulated output voltage of an LDO regulator is always lower than input voltage, as shown in the equation.



(a)



(b)

Figure 2.14: The operation principle of linear voltage regulator [39].

If I_{out} is the output load current and I_q is the internal circuitry loss, then the efficiency of the LDO is given as,

$$LDO\ Efficiency: \eta_{LDO} = \frac{P_{out}}{P_{in}} = \frac{V_{out} \times I_{out}}{V_{in} \times (I_{out} + I_q)} \times 100 \quad (2.10)$$

Assuming negligible losses in the regulator circuitry (I_q),

$$\eta_{LDO} \approx \frac{V_{out}}{V_{in}} \quad (2.11)$$

Equation (2.9) suggests that linear regulators are power efficient only when the output voltage is close to the input voltage and their efficiency peaks only when the dropout voltage is small. Earlier work done on energy harvesting using linear regulators in [51] suffers from low overall conversion efficiencies because of the larger difference between V_{in} and V_{out}.

2.4.2 Sub-threshold Voltage Regulation

In previous section, it is stated that conventional regulators are not good candidates for energy harvesting applications due to their low power conversion efficiency and high quiescent power consumption. The comparison of specifications for a low power voltage regulator and conventional regulators is given in Table 2.1.

Table 2.1: The comparison of specifications of low power voltage regulation and conventional voltage regulators.

Specifications	**An LDO for energy harvesting application**	**A conventional LDO**
Output capacitance	250 pF	5 µF
Load current range	0.1 µA– 25 µA	0.1 mA– 100 mA
Quiescent current	< 1 µA	< 100 µA
PSRR (Power Supply Rejection Ratio)	@100 kHz < -20 dB	@1 kHz < -20 dB

2.4.2.1 Sub-threshold Voltage Reference Designs

The voltage reference block generates a voltage which is independent of the input voltage and temperature. Because a voltage reference circuit is always active by drawing current from the power supply, its power consumption should always be kept as low as possible by operating most of the transistors in sub-threshold region. Typical band-gap voltage reference generators are not suitable for the low voltage and low power applications. Most of them generate a reference voltage higher than 1.2 V; however sub-1 V reference voltage is required in low voltage applications. Also, they use a BJT which is not available in many standard CMOS processes and is area hungry. Therefore, MOSFETs operating in sub-threshold region could be used in generating a PTAT voltage.

In [51], a voltage reference design is proposed which utilizes the fact of operating a pair of transistors in sub-threshold region and a pair of them in saturation region. Figure 2.15 shows the schematic in which M_1 and M_3 are high V_{TH} transistors that are biased in sub-threshold region and M_2 and M_4 operate in saturation. Two current mirrors force the same currents to be passed through transistors which are biased in different modes. As a result, by solving the equations of currents for saturation and sub-threshold regions, it's possible to show that a voltage independent current, I_0, is generated as below:

$$I_0 = \frac{\mu C_{ox}(W_4/L_4)}{2(N-1)^2} m^2 V_T{}^2 ln^2\left(\frac{W_3/L_3}{W_1/L_1}\right) \tag{2.12}$$

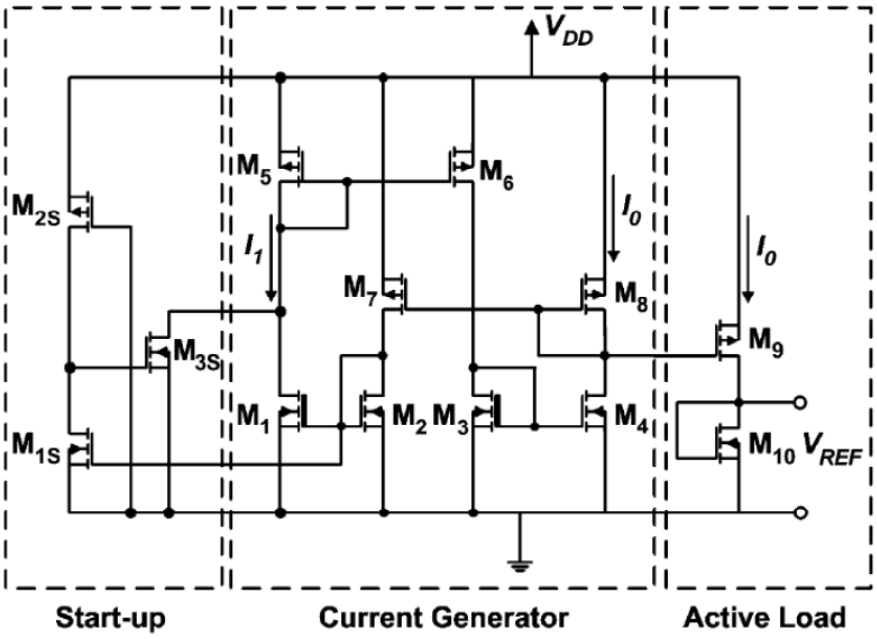


Figure 2.15: The sub-threshold voltage reference proposed in [51].

The generated I_0 is then passed through diode-connected M_{10} transistor and V_{REF} is generated as below:

$$V_{REF} = V_{TH,M_{10}} + \frac{mV_T}{N-1}\sqrt{\frac{W_4/L_4}{W_{10}/L_{10}}}ln\left(\frac{W_3/L_3}{W_1/L_1}\right) \tag{2.13}$$

The generated V_{REF} is totally independent of power supply while the design doesn't use any resistors for keeping the power consumption of the circuit in a low level. This decreases the amount of area demand, significantly. In order to operate the circuit in the lowest power consumption level, the I_0 current, related with the transistors working in the saturation region must be kept minimum. Therefore, the M_4 transistor in Figure 2.15 is biased such that $V_{GS4} \approx V_{TH4}$ to ensure lowest possible current:

$$I_{0,min} = \frac{\mu C_{ox}(W_2/L_2)}{2} m^2 {V_T}^2 ln^2\left(\frac{W_3/L_3}{W_1/L_1}\right) \tag{2.14}$$

Also, the $(W/L)_2$ and $(W/L)_3$ must be kept as low as possible to achieve lowest power consumption.

2.4.2.2 Sub-threshold Voltage Regulator Designs

A series voltage regulator is normally used together with a voltage reference to regulate the input voltage. A typical voltage regulator stage for low voltage passive RFID applications has been shown in Figure 2.16. The first stage is a comparator which compares the output regulated voltage with a reference voltage. The second stage is a buffer stage and the third stage is the pass transistor which regulates the output voltage. The power consumption of this circuit mostly depends on the power which is consumed by the op-amp stage and should be kept in the minimum level.

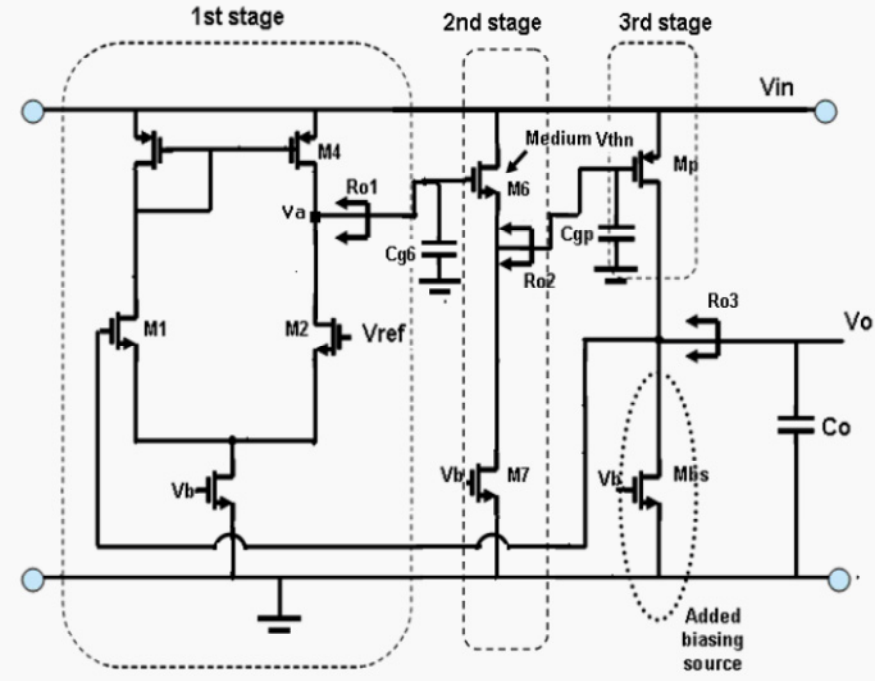


Figure 2.16: The typical voltage regulator stage for low voltage applications [53].

2.5 On-Chip Power Management

A power management may refer to a wide range of applications in the literature; however, in interface electronics of energy harvesting applications, it means how the connection between the converted power of the harvester and the output load is controlled. This is particularly important when the energy harvester is connected to power up a real load like a sensor node. The power management unit continuously monitors and controls the power demand at the load side and the harvested power of the mechanical transducer and shut down the load when enough power is not available. In the standby mode, the system waits for the storage capacitor to reach a

minimum voltage and connects the load after this point. Since this block is active all the time, it should also have a very low quiescent current drawing from the supply.

In [54], a simple power management block has been used for thermoelectric power harvesting (Figure 2.17). There are two comparator circuits which decide to charge up the output reservoir by comparing the fed back output voltage and the voltage of the thermoelectric generator.

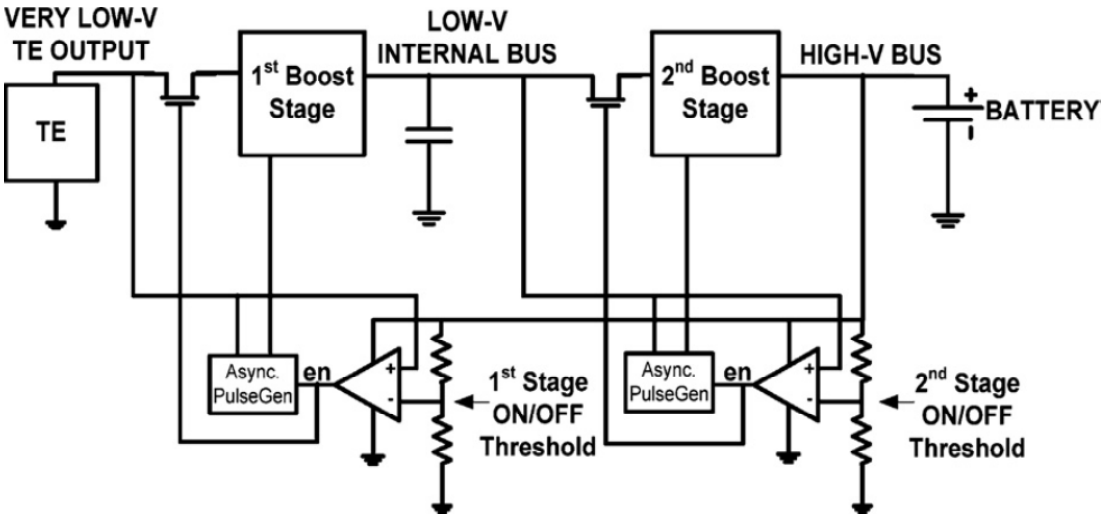


Figure 2.17: The thermoelectric power management unit proposed in [54].

In [55], a mode selector has been used to track the converted DC voltage supply and two trip points have been generated using resistive ladders, by which the output enable signal goes *low* or *high*. The quiescent power consumption of this block is 2.7 μW at maximum.

2.6 Summary of the Chapter

In this chapter, a complete overview on the required building blocks for realizing a typical energy harvesting interface electronics has been discussed. The theory, design and the state-of-the-art designs for each block is explained. Based on the provided information, special design considerations are required for low voltage, low power energy harvesting applications and with respect to that, a discussion for each block is given. Next chapter explains the design and simulation results of the proposed energy harvesting circuits in 0.35 μm CMOS process which are compatible with the mentioned design considerations in this chapter.

CHAPTER 3

THE ENERGY HARVESTING IC IN 0.35 μm CMOS TECHNOLOGY

The previous chapter introduced the different building blocks that are needed for a typical energy harvesting interface circuitry. Among them, the highly efficient rectifiers are the most important blocks for a vibration-based energy harvesting system due to the alternating output characteristic. On top of that, the other post-DC-conversion blocks including active rectifiers, DC-DC converters, and the voltage regulators use the provided DC voltage of the first rectifier block in a fully self-powered system. Therefore, the rectifier efficiency as the very first block in an interface circuitry plays a significant role in the total performance of the system.

In this chapter, the theory, design, and simulation results of different rectifiers are explained, which have been designed in a standard 0.35 μm CMOS process that is a low cost and widely available technology. Some of the previously reported passive rectifiers have also been simulated and their performance results are compared with the proposed architectures. Section 3.1 explains the general overview of the IC by introducing the implemented blocks. Section 3.2 explains the theory and simulation results of the previous most commonly used passive rectifiers. Section 3.3 gives the schematic, design and simulation results of the proposed passive rectifier which is designed for low voltage and low power applications. Different metrics of the rectifier are simulated and characterized, and also, a performance comparison of the proposed design and pervious reported designs is given. Section 3.4 presents the design and simulation results of the proposed active rectifier for low voltage applications. Section 3.5 describes the limitations and challenges of a standard

design environment and states the potential improvements that are expected once moving to a more advanced technology for low power applications. Finally, section 3.6 summarizes this chapter.

3.1 The Energy Harvesting IC Overview

The proposed energy harvesting IC includes different types of rectifiers which are implemented on the same chip. Since all circuit topologies are different, and they all share the same substrate, only one of the circuits could be operated at a time, and all other pads should be remained open circuit. Figure 3.1 shows the top level view of the ASIC with different circuits which have been designed and implemented. In the remaining sections of this chapter, the design and simulation results of each of these circuits have been discussed.

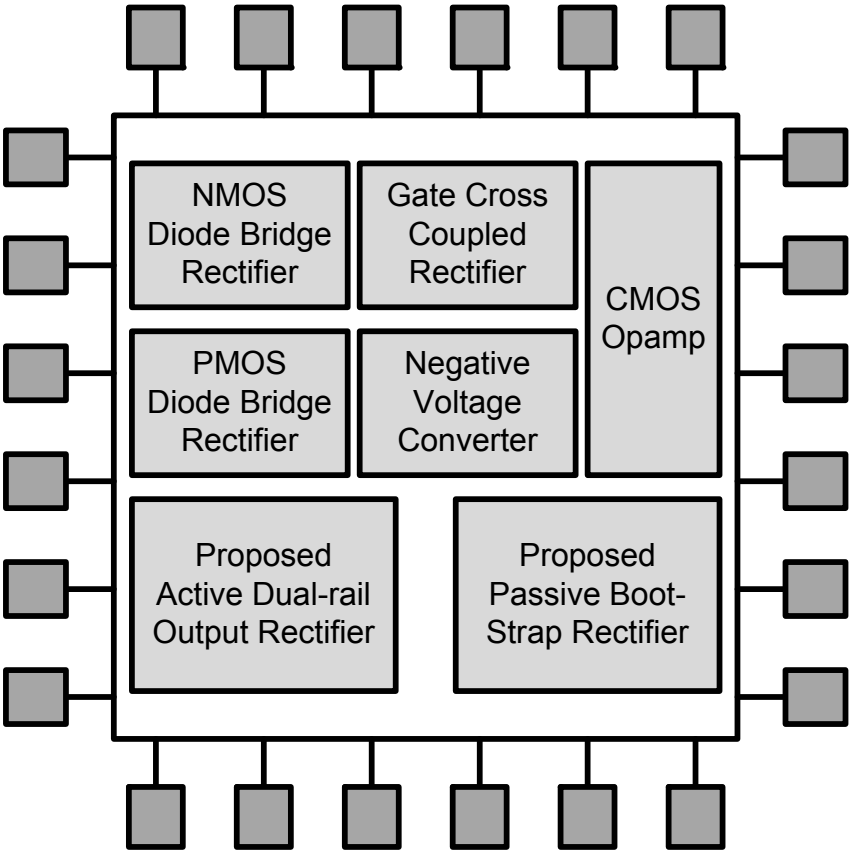


Figure 3.1: The overview of the energy harvesting IC in 0.35 μm CMOS technology.

3.2 The Common Passive Rectifiers

In this section, different passive rectifiers which have been previously reported and most widely used in the literature are explained. The main reason of explaining them is to make a fair comparison between the newly proposed design and previously reported circuits, while using the same technology.

Passive rectifiers are circuits that rectify the AC voltages based on a diode-based operation, simply a diode bridge rectifier. In IC design, diode connected transistors are used as diodes. Figure 3.2 (a) shows the simple structure: a full-wave bridge rectifier (FWBR) in which the output peak voltage is two diode threshold-voltage drops below the input:

$$V_{OUT} = V_{IN} - 2\,|V_{THN}| \tag{3.1}$$

Hence, the total conversion efficiency of this circuit is low, especially for low input AC voltages. Reducing the rectifier drop voltage, decreases the power dissipation of the rectifiers and improves its power conversion efficiency. The voltage drop of the diode connected transistors in Figure 3.2 (a) which are operating in saturation region is:

$$|V_{GS}| = |V_{DS}| = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}} \tag{3.2}$$

where V_{GS}, V_{DS}, and V_{TH} are gate-to-source, drain-to-source, and the threshold voltage of the transistor, I_D is its drain-source current, $\mu_n C_{ox}$ is the intrinsic transconductance, and W and L are width and length of the transistors in the utilized technology, respectively. V_{TH} is a process dependent parameter and could be minimized by eliminating the body effect [54]. In order to minimize the second term in (3.2), the (W/L) of the transistor should be increased as much as the area availability and the parasitic capacitance permits.

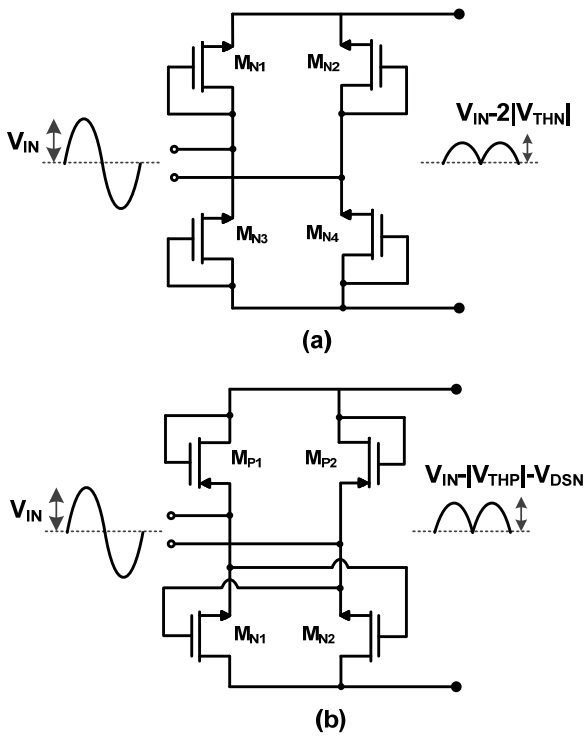


Figure 3.2: (a) The full-wave bridge rectifier, (b) the gate-cross-coupled rectifier.

The V_{TH} of the diode-connected transistors could be reduced to very small values (~ 100 mV) using special technologies and combined semiconductors [23]. However, very small V_{TH} transistors are not available in standard CMOS processes, even though they are widely required, especially in low voltage applications such as in interface electronics for energy harvesters. Therefore, circuit techniques are employed to decrease the effective V_{TH} of the transistors while remaining in the same standard technologies.

An improved version of the FWBR is the gate cross coupled rectifier (GCCR) [23] where a pair of diode-connected transistors are replaced with a pair of cross-connected NMOS transistors (Figure 3.2 (b)). In this configuration, a pair of transistors rectifies the AC input and one pair only passes the current through its drain-source. Therefore, the threshold voltage of the diode connected transistors (M_{N3} and M_{N4} in Figure 3.2 (a) is replaced with the drain-source voltage of the NMOS transistors (M_{N1} and M_{N2} in Figure 3.2 (b)) and full-wave rectification is achieved where,

$$V_{OUT} = V_{IN} - (|V_{THP}| + V_{DSN}) \tag{3.3}$$

where, V_{THP}, and V_{DSN} are the threshold voltage of the PMOS diode and drain-to-source voltage of the NMOS cross coupled transistors, respectively. This results in higher conversion efficiency due to the lower V_{DS} of the diode-tied transistors. Figure 3.3 and Figure 3.4 show the simulation results of the transient response of the FWBR and GCCR circuits with (W/L) of the diode-tied transistors and the gate cross coupled transistors as 20 µm/0.35 µm and using C_{OUT} =100 nF, R_L=100 kΩ for a floating sinusoidal voltage source with frequency of 1 kHz and 1 V peak and 5 V peak, respectively. For a 1 V peak input, the generated output voltage is significantly lower for FWBR compared with GCCR due to the high threshold-voltage transistors available in the utilized standard CMOS process ($|V_{THP}|$=0.73V, V_{THN}=0.55V). For higher input AC voltages, the effect of high threshold voltage is less and the gap between the output voltages is smaller, as depicted in Figure 3.4 for a 5 V peak input. The other simulation results describing the behavior of the circuits are placed in the next section for the comparison purposes with the proposed BSR design.

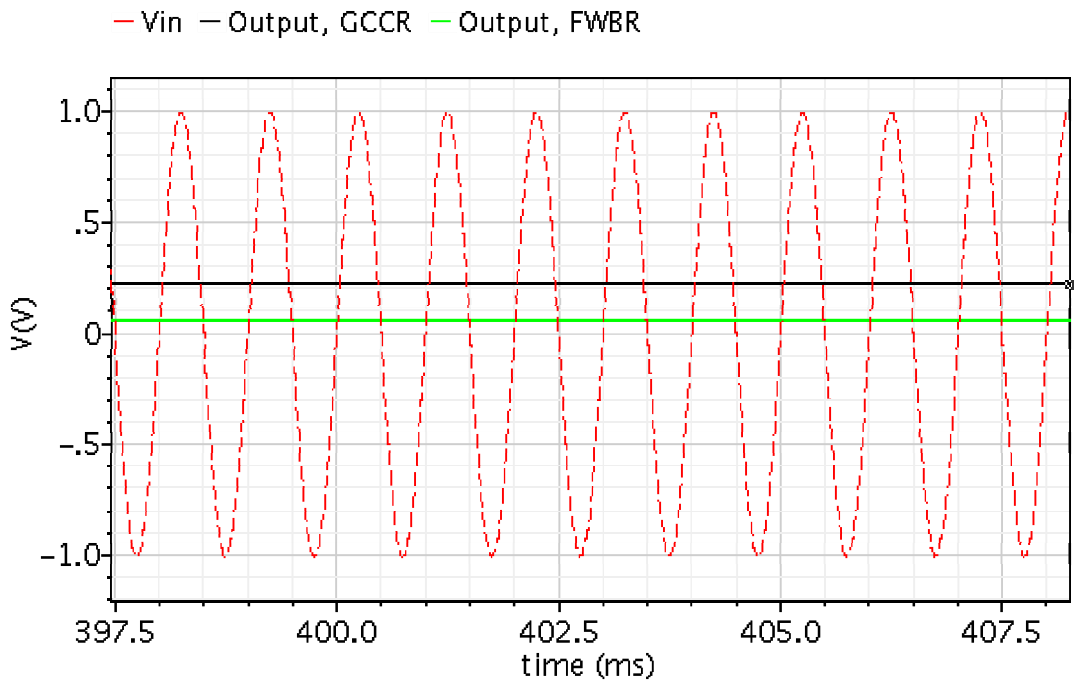


Figure 3.3: The transient simulation result of the FWBR and GCCR designs for a sinusoidal input voltage with 1 V peak using C_{OUT}=100 nF, R_L=100 kΩ and (W/L) = 20 µm/0.35 µm.

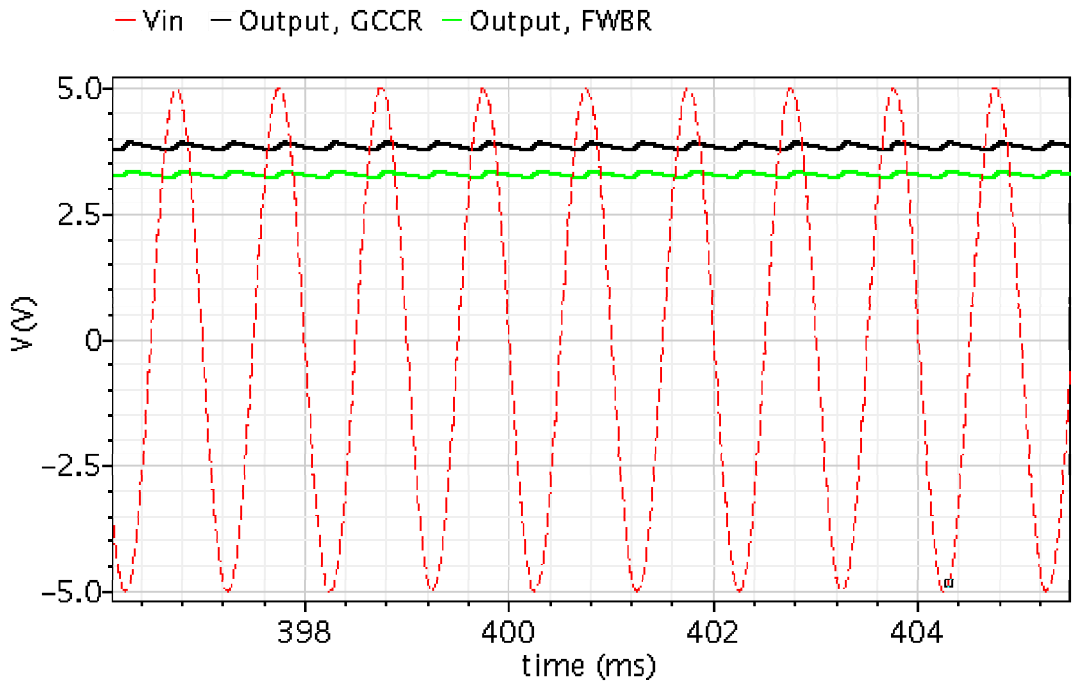


Figure 3.4: The transient simulation result of the FWBR and GCCR designs for a sinusoidal input voltage with 5 V peak using C_{OUT} =100 nF, R_L=100 kΩ (W/L) = 20 µm/0.35 µm.

3.3 The Proposed Passive Full-Wave Rectifier

In previous section, two most commonly used passive rectifiers for energy harvesting applications have been discussed. The gate cross coupled rectifier (GCCR) significantly improves the performance of rectification compared to full-wave diode bridge rectifier (FWBR); however, the efficiency is still low due to the voltage drop over a pair of diode-tied transistors. In this section, a new design of a passive full-wave rectifier in standard 0.35 μm CMOS process, which is developed in the frame of this study, has been described.

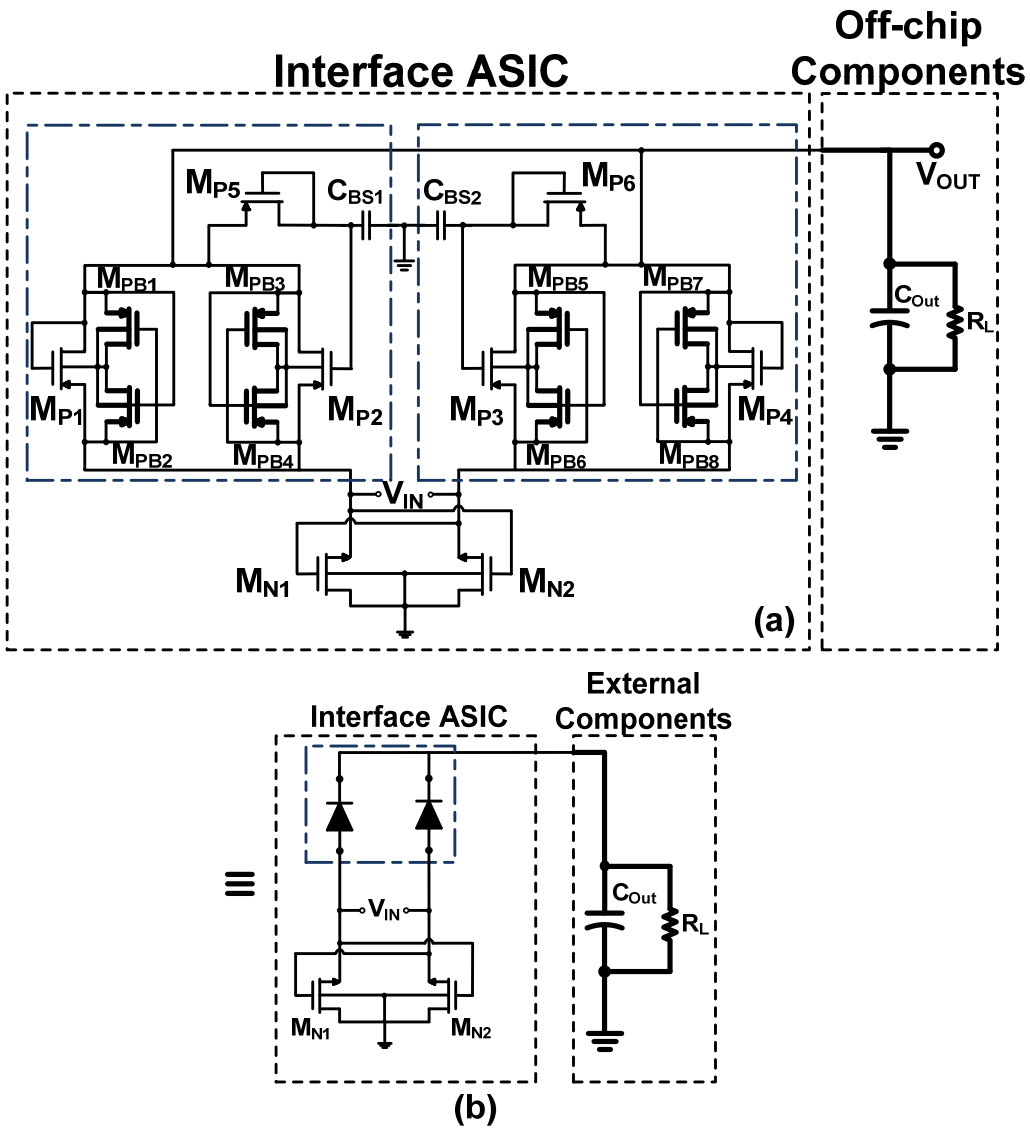


Figure 3.5: (a) The proposed boot-strap rectifier (BSR) schematic, (b) the view of the BSR design which shows the modified diodes together with the gate-cross-coupled (GCC) transistors.

This proposed design utilizes the gate cross coupled transistors as in [23] for current passing through the drain-source (as described in section 2.2.1) and the rectification is served using a pair of boot-strap connected modified diodes in order to reduce the threshold voltage of the diode connected transistors [24], increasing the conversion efficiency. Figure 3.5 shows the proposed rectifier schematic, which includes a pair of gate-cross-coupled (GCC) transistors and a pair of boot-strap connected transistors, forming together a full wave rectifier.

In this structure, M_{N1} and M_{N2} are the GCC transistors; M_{P1}, M_{P2}, and M_{P5} are the boot-strap transistors, where C_{BS1} is the boot-strap on-chip capacitor, such that the whole highlighted block in Figure 3.5 acts as a modified diode. In order to eliminate the body effect, hence, to decrease the V_{TH} of transistors, the bulk connection of NMOS transistors is directly connected to ground and body effect plays no role for them. For the PMOS transistors, M_{P1}- M_{P4}, since their source is connected to V_{IN} which is largely varying while the transducer is connected, there is high risk of latch-up. As another consideration for these transistors, since each of them is placed in a separated N-well, there is a high risk that the vertical PNP transistor turns ON, increasing the substrate leakage current. Therefore, M_{PB1}-M_{PB8} are utilized as the bulk regulating transistors to dynamically boost the bulk of PMOS transistors to the higher available voltage to avoid the latch-up effect of PMOS devices [23].

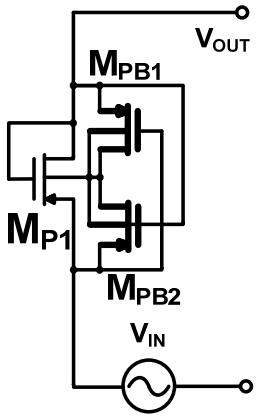


Figure 3.6: The bulk regulation concept to avoid latch-up in PMOS transistors.

This phenomenon is explained in more detail in Figure 3.6. The bulk and drain connections of M_{PB1} and M_{PB2} transistors are connected to the bulk connection of M_{P1}. Whenever M_{P1} is ON ($V_{IN} > V_{OUT} + V_{THP1}$), M_{PB2} also starts to conduct since

the M_{P1} and M_{PB2} share the same source and M_{PB2} connects the substrate (N-Well) to the highest voltage at this time (V_{IN}). At the time that V_{IN} is less than V_{OUT} by at least one V_{THP1}, M_{PB1} conducts by connecting the bulk to V_{OUT}. Therefore, the bulk of the main PMOS device is connected to the highest available voltage at all the time, diminishing the body effect.

Figure 3.7 presents the simplified half-circuit schematic of the modified diode, explaining the operation principle. The boxed block shows the modified boot-strap connected diode with anode terminal connected to one terminal of V_{IN} and the other terminal of it is connected to the drain of the GCC transistor, M_{N2}.

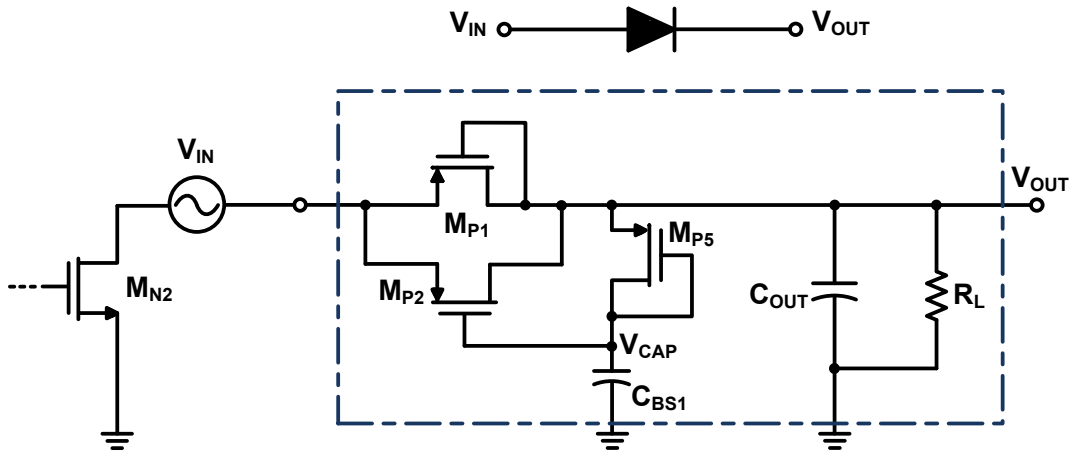


Figure 3.7: The simplified half-circuit schematic of the modified diode block.

The output capacitor starts being charged through the diode-connected transistor, M_{P1}, when,

$$V_{OUT} = (V_{IN} - V_{DSN2}) - |V_{THP1}| \tag{3.4}$$

where V_{THP1} is the threshold voltage of M_{P1}, and V_{DSN2} is the drain-to-source voltage of M_{N2}. While the output node is being charged through M_{P1}, a charge will be captured on the internal capacitor, C_{BS1} and the voltage across it will be:

$$V_{CAP} = V_{OUT} - |V_{THP5}| = (V_{IN} - V_{DSN2}) - |V_{THP1}| - |V_{THP5}| \quad (3.5)$$

At the beginning of the operation, since the output voltage has not been fully charged and while the source-gate voltage of it is higher than its threshold voltage ($|V_{THP1}|+|V_{THP5}|>|V_{THP2}|$), M_{P2} starts conducting and C_{BS1} starts being charged. The gate voltage of M_{P2} (V_{CAP}) increases up to its cut-off point:

$$V_{SG2} = (V_{IN} - V_{DSN2}) - V_{CAP} = |V_{THP2}| \quad (3.6)$$

By substituting (3.2) into (3.3),

$$V_{SG2} = (V_{IN} - V_{DSN2}) - V_{CAP} = |V_{THP2}| \quad (3.7)$$

$$\begin{aligned} V_{SG2} &= (V_{IN} - V_{DSN2}) - V_{CAP} \\ &= (V_{IN} - V_{DSN2}) - (V_{OUT} - |V_{THP5}|) = |V_{THP2}| \end{aligned} \quad (3.8)$$

$$(V_{IN} - V_{DSN2}) - V_{OUT} + |V_{THP5}| = |V_{THP2}| \quad (3.9)$$

$$V_{OUT} = V_{IN} - (|V_{THP5}| - |V_{THP2}|) - V_{DSN2} \quad (3.10)$$

As observed in equation (3.7), the threshold voltage of the diode-connected transistor in GCCR design is replaced with the difference of the threshold voltages of M_{P2} and M_{P5}. Therefore, the effective threshold voltage is significantly decreased compared to FWBR and GCCR configurations (equations (2.1) and (2.3), respectively). Thus, the converted output DC voltage, the output power, and the AC/DC power conversion efficiency are increased.

The proposed BSR circuit and the previously reported FWBR and GCCR circuits are simulated using X-FAB 0.35 µm standard CMOS process under Cadence environment. Two latter circuits have been validated in order to make a realistic comparison with the proposed structure. The designs are optimized in such a way

that all three circuits achieve the highest DC output. Table 3.1 summarizes the selected (W/L) values of transistors of the proposed design.

Table 3.1: The (W/L) values of transistors of the proposed BSR design.

Transistor	W/L (µm)
M_{P1}, M_{P4}	1 / 0.35
M_{P2}, M_{P3}	20 / 0.35
M_{P5}, M_{P6}	6 / 0.35
M_{N1}, M_{N2}	20 / 0.35
M_{PB1}, M_{PB8}	1 / 0.35

Figure 3.8 and Figure 3.9 show the transient response of the BSR circuit using C_{OUT} =100 nF, R_L=100 kΩ for a floating sinusoidal voltage source with frequency of 1 kHz and 5 V peak and 1 V peak, respectively.

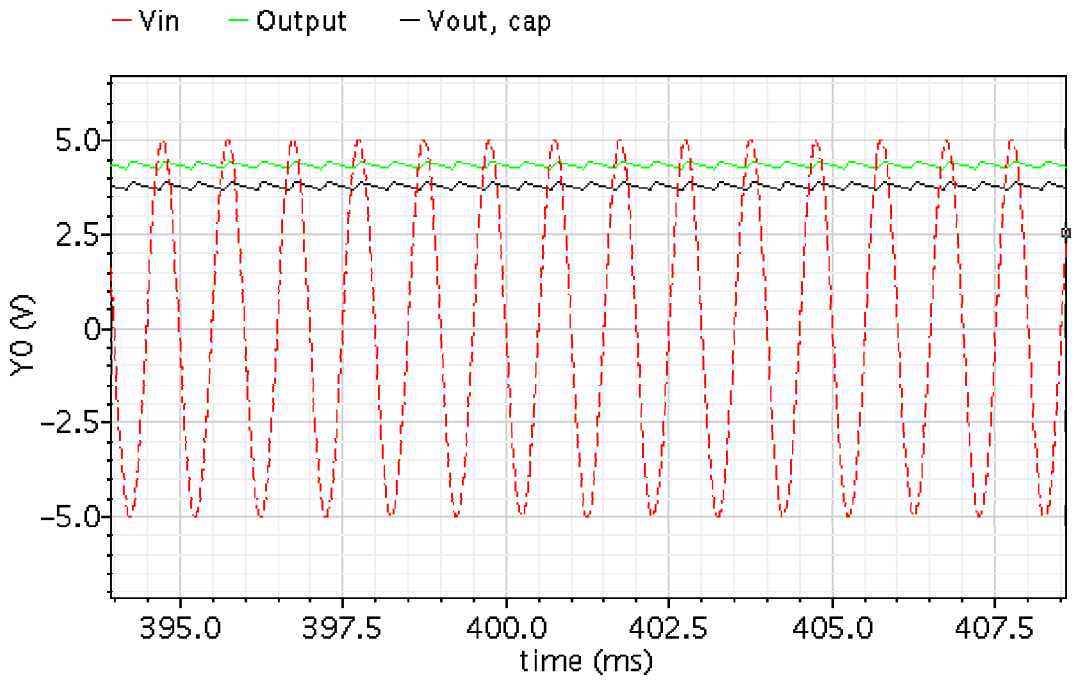


Figure 3.8: The transient simulation result of the BSR rectifier for a sinusoidal input voltage with 5 V peak using C_{OUT}=100 nF, R_L=100 kΩ.

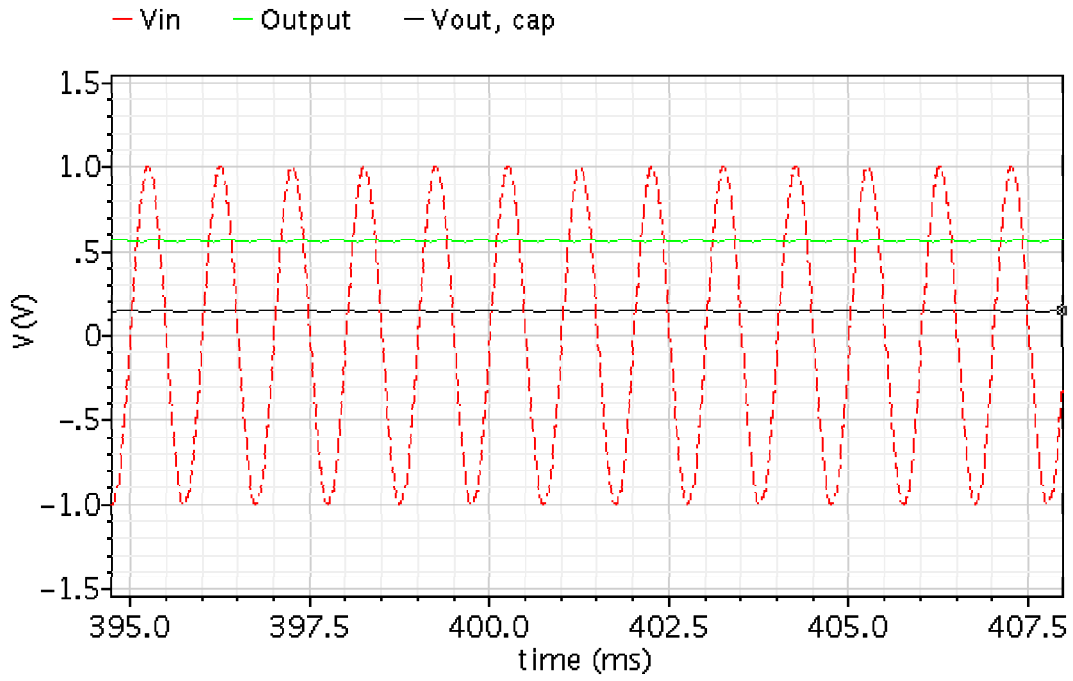


Figure 3.9: The transient simulation result of the BSR rectifier for a sinusoidal input voltage with 1 V peak using C_{OUT}=100 nF, R_L=100 kΩ.

The output DC voltage is closer to the peak value of the input voltage for higher peak AC inputs (Figure 3.8) which shows the higher efficiency of the passive circuit for higher input peak values. This voltage can reach the peak value of the input AC source at maximum. The V_{CAP} trace has also been shown in order to see the effect of bulk regulation technique to eliminate the body effect. By comparing equations 3.2 and 3.7, both of them have same terms except plus V_{THP2} and minus V_{THP1} for V_{OUT} and V_{CAP}, respectively. Therefore, the V_{OUT} is at a higher value compared with V_{CAP}, as expected from above equations.

The converted output voltage of a rectifier can reach the peak value of the input AC voltage for an ideal diode with zero threshold voltage, if there is no load connected at the output to discharge the storage capacitor. In order to find out the effect of input peak variation on the voltage conversion behavior of the rectifier, the voltage efficiency is defined as,

$$Voltage\ Efficiency\ [\%] = \frac{V_{Output,DC}}{V_{Peak,AC}} \tag{3.11}$$

Figure 3.10 depicts the voltage efficiency of three rectifiers at different sinusoidal input voltage peak values at frequency of 1 kHz for the no-load output case. The voltage efficiency for the proposed BSR circuit is above 80% for input voltages higher than 700 mV peak and is more than 90% for input peak voltages of more than 2 V. It drops for the input peaks of less than 500 mV due to the high threshold voltage transistors which are available in the utilized standard CMOS process. However, the same voltage efficiency of 80% is reached for GCCR and FWBR after 2.5V and 4.5V peak input voltages, respectively. This proves the much higher performance of the proposed BSR design in converting the AC voltages to DC, especially for low voltage AC inputs.

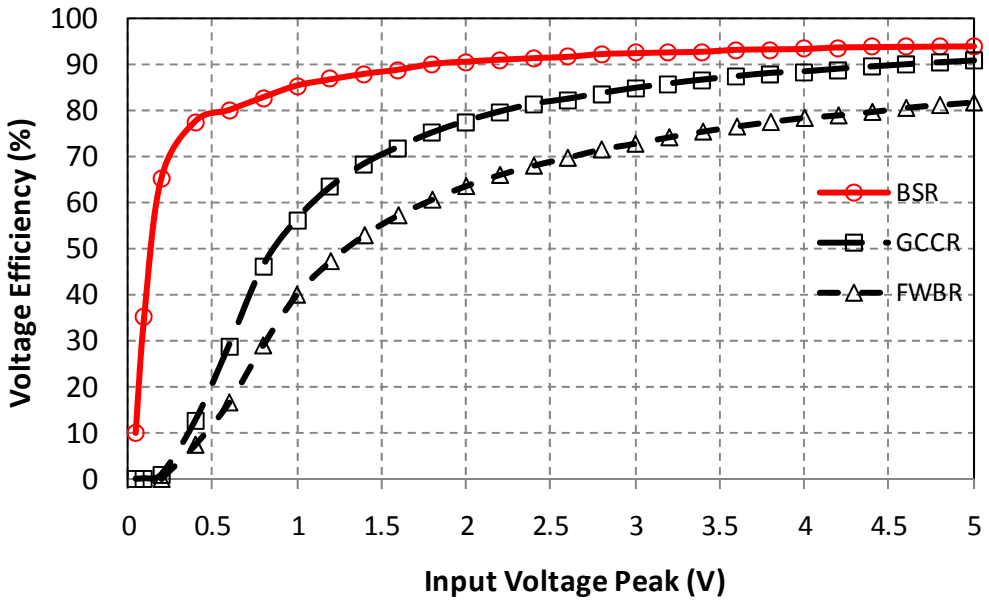


Figure 3.10: The voltage efficiency of the BSR circuit for different input voltage peak values at no-load condition.

In order to check the performance of the rectifiers; they are also tested under different load conditions. The output storage capacitor could be of any size and its value doesn't define the final converted DC voltage. Instead, its value yields the amount of storable energy at the output by increasing the storage time while:

$$Output\ Stored\ Energy[J] = P_{out} \times \Delta t\ (Charging\ Time) \tag{3.12}$$

Also, by increasing the output storage capacitor value, the ripple of the output voltage will be decreased due to the increased time constant of the circuit. Figure 3.11 shows the converted output voltage for a typical sinusoidal input of peak 2 V, versus the output load resistance values. The resistive load parallel with the output capacitor has been swept from 1 kΩ to 10 MΩ. By decreasing the load resistance, the output voltage also starts to decrease due to the higher rate of output capacitor discharge.

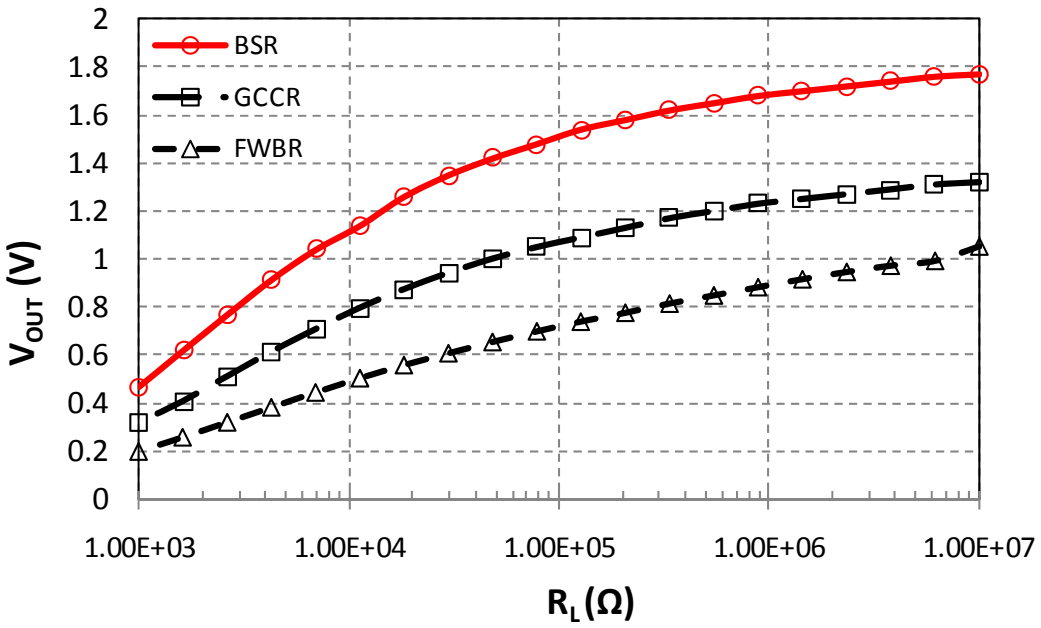


Figure 3.11: The output voltage of the rectifiers versus different load values for a sinusoidal input voltage of peak 2 V.

Figure 3.10 depicts the voltage efficiency of the rectifiers versus different input values at no-load condition. However, as another comparison, the output voltage and voltage efficiency of the circuits have been compared while a typical 50 kΩ load is connected at the output, depicted in Figure 3.12.

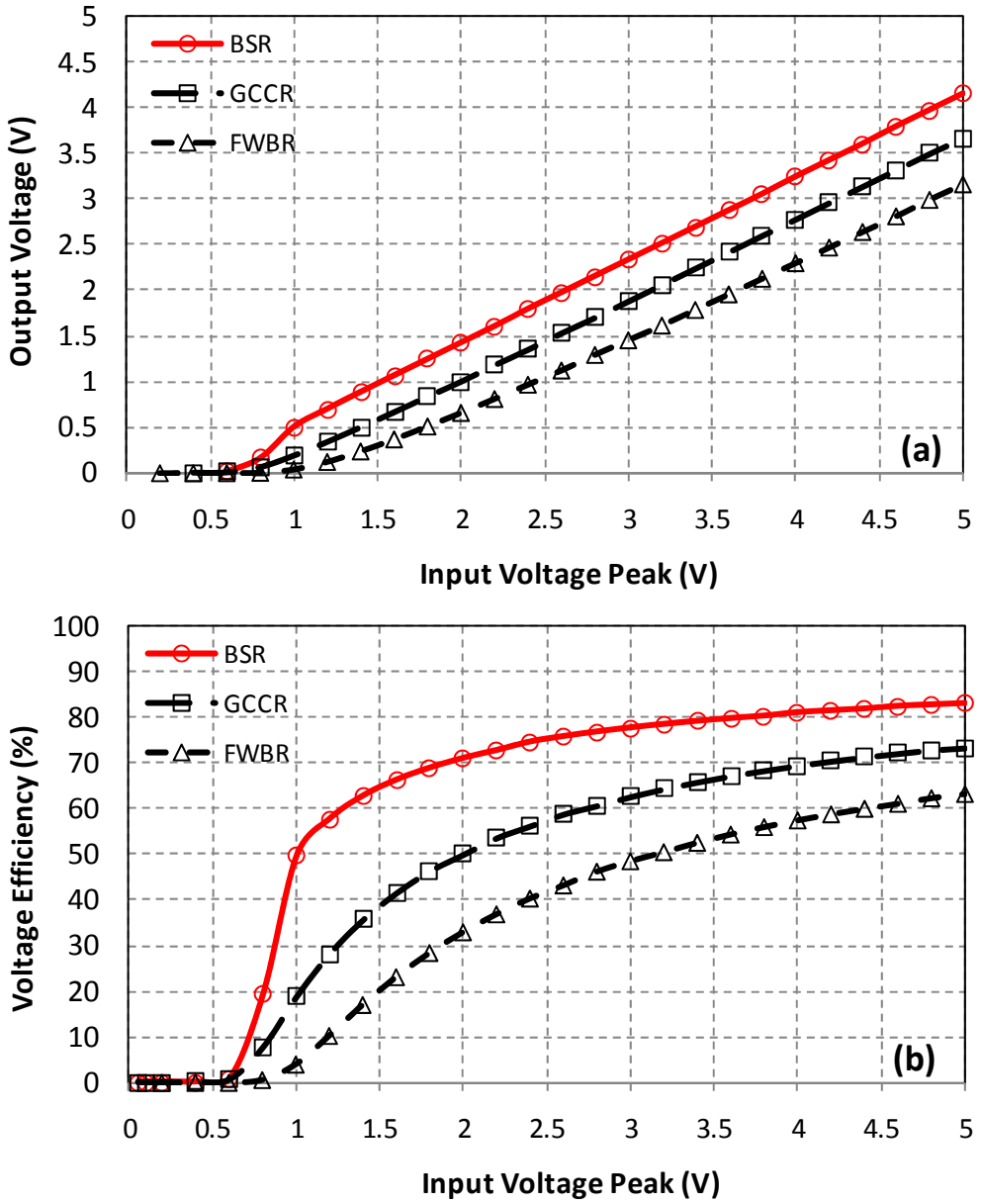


Figure 3.12: (a) The converted output voltage, (b) the voltage efficiency of the rectifiers versus different input peak values for R_L=50 kΩ.

Another metric to be taken into account for comparing the rectifiers is their power conversion efficiency. This is done by comparing the input with the output power. The input power is the generated AC power from the AC source and the output power is the converted DC power at the output:

$$P_{input} = I_{input\,[rms]} \times V_{input\,[rms]} \tag{3.13}$$

$$P_{output} = I_{out[DC]} \times V_{out[DC]} \tag{3.14}$$

The power conversion efficiency is then defined as,

$$Power \quad Efficiency \quad [\%] = \frac{P_{output}}{P_{input}} \times 100 \tag{3.15}$$

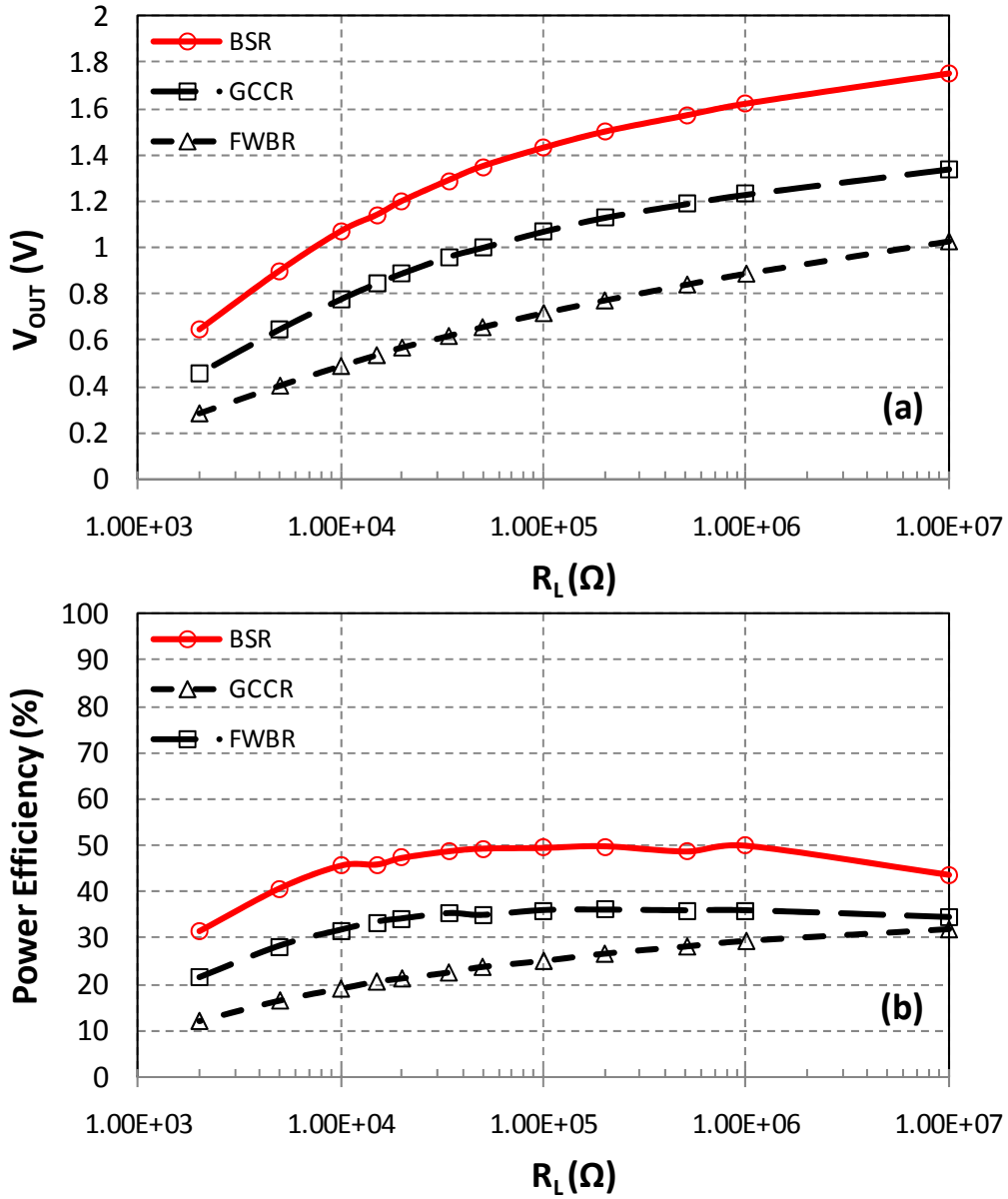


Figure 3.13: The converted output voltage and the power conversion efficiency of the rectifiers for different load values.

Figure 3.13 shows the converted output voltage and the power conversion efficiency of the rectifiers under different load conditions ranging from 2kΩ - 10 MΩ for an AC

input voltage of 2 V peak and 1 kHz frequency. The converted output voltage and power conversion efficiency is significantly higher using the proposed BSR design.

In this section, a novel design for a passive rectifier has been described and the simulation results showing its performance over previously reported circuits, are presented. In a passive design, effort is done to alleviate the effective threshold voltage of the diode-based operations. However, the threshold voltage still could be lowered using an active design which dynamically compares the input and output voltages using an external comparator. Next section gives the design and optimization which has been made for an active rectifier design to reach the maximum conversion efficiency.

3.4 The Proposed Active Full-Wave Rectifier

The theory, design, and operation of the active rectifiers as well as their state-of-the-art have been fully described in section 2.2.2. The proposed active design is a comparator-based full-wave rectifier with dual-rail output which is designed to convert the generated AC voltage to a smooth DC voltage with a high efficiency. Figure 3.14 shows the schematic of the proposed design in which two comparators along with the two switch transistors (M_{SP} and M_{SN}). When the input voltage is higher than V_{out+}, the comparator turns ON the switch M_{SP} to charge the positive output capacitor. The switch M_{SP} is OFF during the negative cycles of the input voltage to keep the charge on the output capacitor. Negative DC voltage (V_{out-}) is stored on the second capacitor when the second comparator activates the switch M_{SN} in a similar manner, during negative cycles.

An external double supply (V_{DD} and V_{SS}) is used to power the comparators as shown in Figure 3.14. Therefore, the comparators should consume as low power as possible such that the consumed power by the circuit is much less than the generated power of the energy harvester; hence the complete system efficiency remains high. Also, the active rectifier should be optimized for the desired voltage range in order to deliver the maximum power from the harvester to the load.

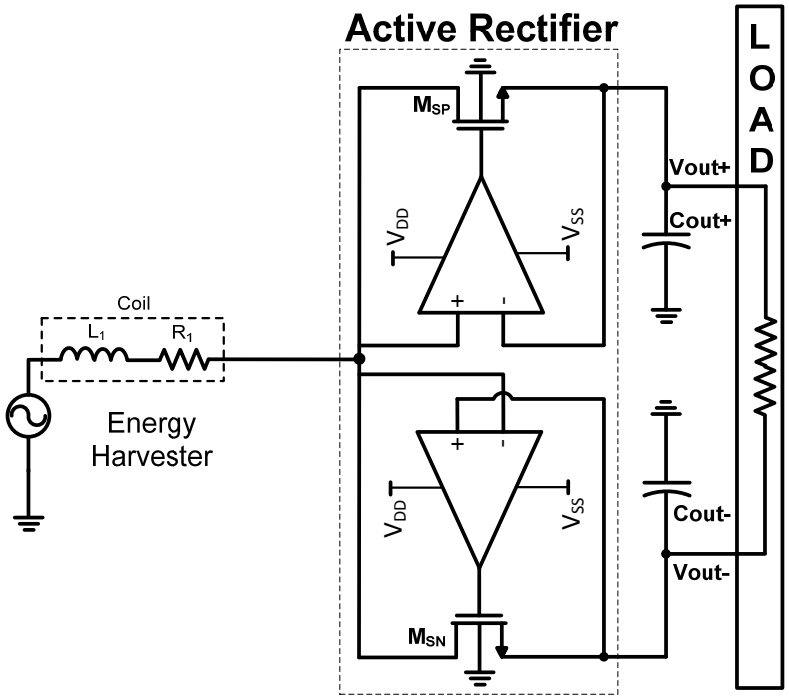


Figure 3.14: The schematic of the proposed active rectifier.

An important issue in the design of the active rectifier is the selection of the (W/L) ratio of the switch transistors to maximize the output DC voltage. Generally, a high (W/L) is selected for the switches to decrease the DC voltage drop over them, increasing the converted output voltage on the storage capacitors.

The simulations show that, the above statement holds for input voltages higher than 500 mV for the given technology and increasing $(W/L)_{switch}$ doesn't necessarily lead to higher output DC voltage for lower amplitude AC inputs due to the higher backward discharge current. Figure 3.15 (a) depicts the simulation results of the circuit for a sinusoidal input voltage with V_{peak}=200 mV at no-load condition for two different W_{switch} values, where L_{switch} is kept at 1 µm. Figure 3.15 (b) shows the output ripple and the effect of the backward discharge current. When the input voltage goes below the output, the switch does not turn OFF immediately due to the non-zero input voltage offset of the comparator, resulting in the backward current flow from the output capacitor to the source which decreases the DC voltage output. This is presented by two simulation results in Figure 3.15 (b) with green and black traces showing the output voltage for W_{switch}=10 µm and W_{switch}=200 µm, respectively. 15 mV higher output voltage is reached for W_{switch}=10 µm, where the backward discharge current is lower. The selection of the transistor dimensions also

affects the ripple of the output voltage. For higher W_{switch} values, since the switch transistor is ON for a longer time, the output ripple will be non preferably higher. This is also presented in Figure 3.15 (b).

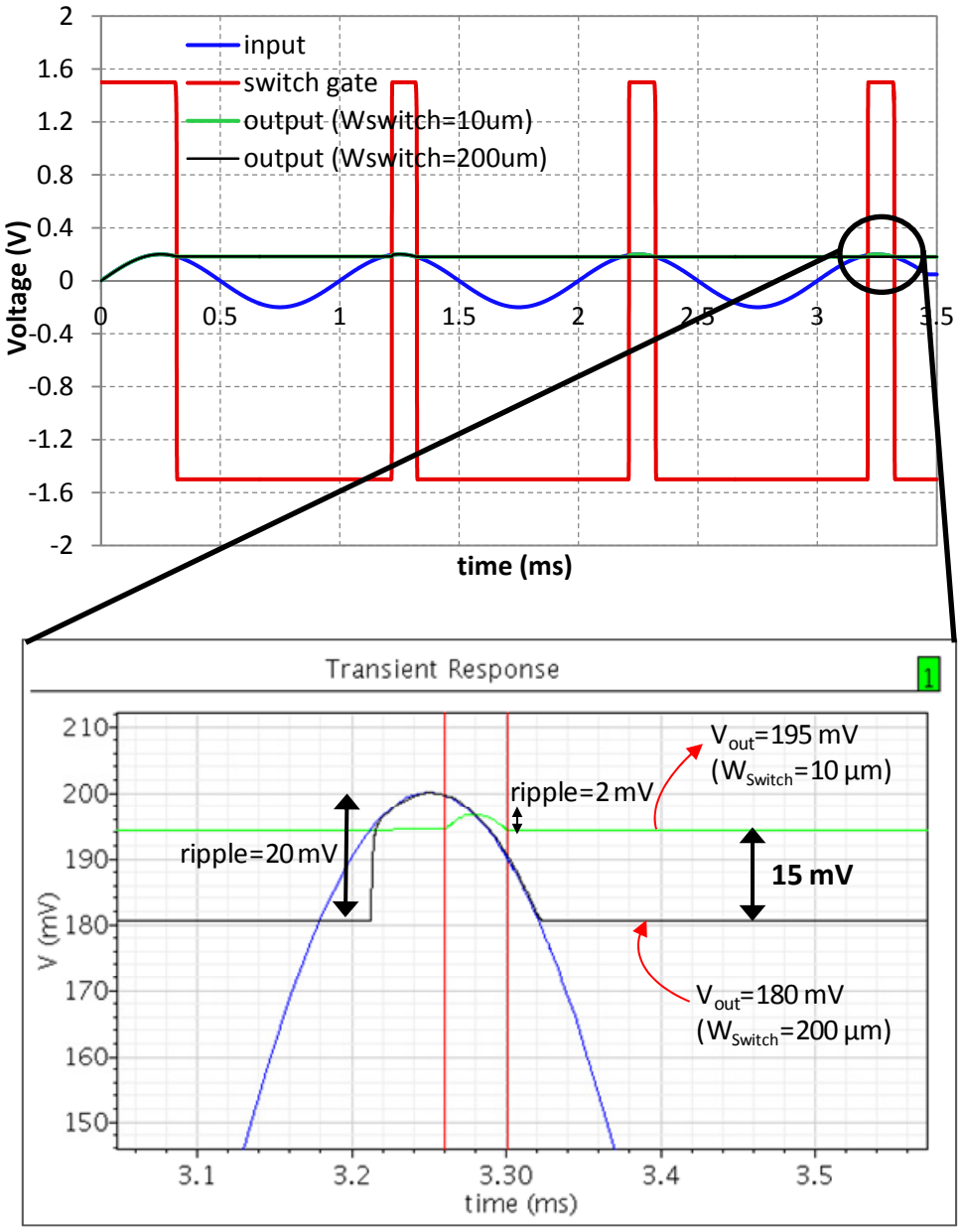


Figure 3.15: The simulation results of the active rectifier for sinusoidal input with V_{peak}=200 mV; (b) the output ripple and backward discharge current - when input goes below the output, the switch is still ON which discharges the capacitor, for two different W_{switch} values (10 µm and 200 µm), while L_{switch} is 1 µm.

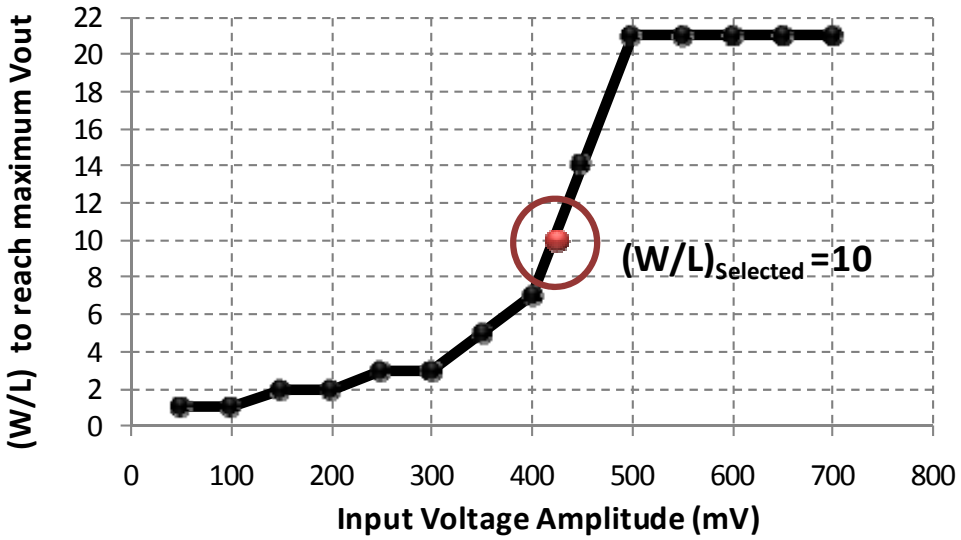


Figure 3.16: The (W/L) ratio required to reach maximum output at different input voltage amplitudes.

Figure 3.16 depicts the optimized $(W/L)_{switch}$ ratios leading to maximum DC output voltage for different input peak voltage levels. The simulations show that the effect of the backward discharge current can be neglected for input voltages with 500 mV amplitude and higher. Below this value, the $(W/L)_{switch}$ ratio should be selected according to the results presented in Figure 3.16. Considering the AC output voltage range of a typical EM energy harvester [10], the $(W/L)_{switch}=10$ is selected.

Figure 3.17 illustrates the schematic of the designed comparator, where the transistor dimensions are also presented. The input transistors are selected relatively large (300 µm / 3 µm) to minimize the input offset of the comparator [27], maximizing the power conversion efficiency. In order to keep the circuit in the lowest power consumption mode, a very low (W/L) ratio (0.4 µm / 150 µm) is chosen for the current source transistor, M_{P3} such that the supply current is kept as small as possible, while all the transistors except M_{P3} operate in sub-threshold region.

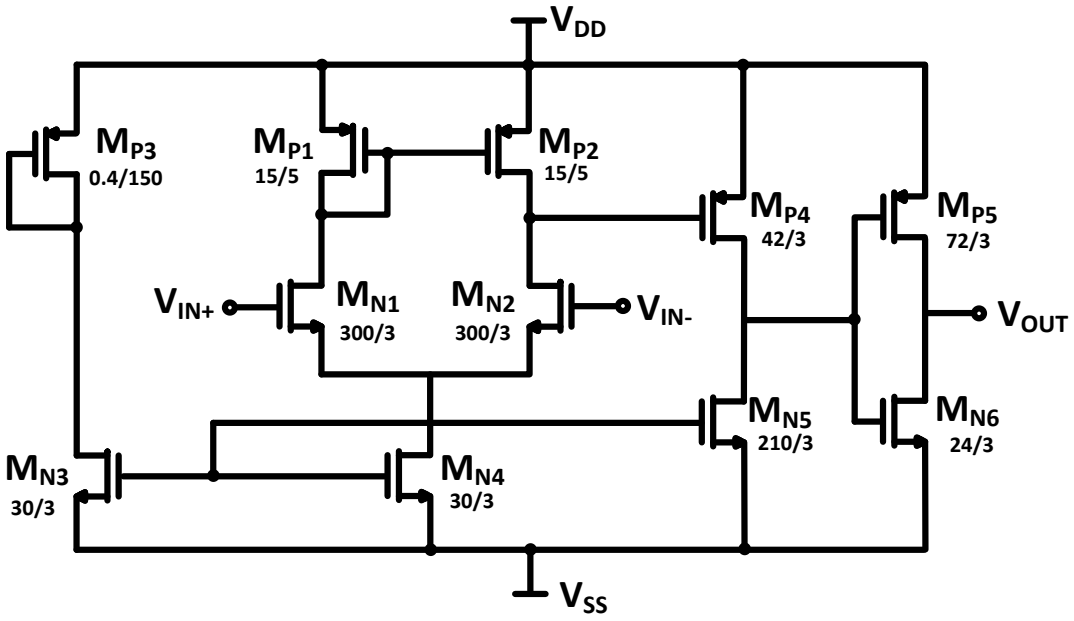


Figure 3.17: The schematic of the designed sub-threshold comparator in X-FAB 0.35 µm CMOS. The dimensions of the transistors are in µm.

3.5 Challenges and Limitations of the Standard 0.35 µm CMOS Process

In the area of vibration-based energy harvesters, especially electromagnetic transducers, the generated signals from the harvester, are not only low voltage, but, very low power. Therefore, in the design of rectifying electronics for such kind of applications, the voltage drop over the transistors and the dissipated power are major concerns and should be kept as low as possible. The standard CMOS processes, including the utilized CMOS process in this work, generally don't contain low voltage electrical models and are not efficient for energy harvesting applications. The efficiency of interface circuitry could be significantly improved by moving to an advanced technology where smaller range of voltages can be processed with higher performance. Apart from that, in the design of power processing unit (Figure 1.4), there are active blocks that need power to operate and their consumed power should be kept much lower than the generated power. This could be achieved in a design environment that different types of transistor models are available such that biasing the transistors in sub-threshold region and forcing them to consume least amount of power is feasible (to be discussed in Section 4.3).

As discussed in this chapter, while the amplitude of the alternating signal increases, the effect of dissipated power across the interface electronics diminishes. Therefore, one alternative is to use small size and efficient transformers to step up the AC signal and use the stepped up voltage as the input of the interface electronics. This option is considered reasonable to be used together with EM energy harvesting systems as their size is comparable to the unavoidable magnets in these systems. However, because transformers cannot be integrated onto the chip; this cannot be used for MEMS-based energy harvesters and transferring to an LVT (Low Threshold Voltage) CMOS process is needed.

3.6 Summary of the Chapter

In this chapter, the design, and simulation results of the proposed energy harvesting IC in 0.35 μm CMOS process has been demonstrated. The designed ASIC includes different types of rectifiers which are specifically designed to interfere the low power and low voltage electromagnetic energy harvesters. The design of a newly proposed passive and active rectifier has been explained. The passive one uses BSR technique, improving the conversion performance of the system with respect to the previously reported rectifiers in the literature. The active rectifier uses an optimized comparator-based design for very high efficiency power conversion performance. Finally, the limitations of a standard CMOS process for low-voltage energy harvesting applications have been discussed. Next chapter describes the design and simulation results of a new energy harvesting IC in an advanced CMOS technology, suitable for next generation MEMS-based energy harvesters.

CHAPTER 4

THE ENERGY HARVESTING IC IN 90 nm CMOS TECHNOLOGY

In the previous chapter, the design and simulation results of the proposed energy harvesting IC in the standard 0.35 μm CMOS has been explained. The novel designs for rectifiers have been developed and analyzed using this technology. However, in the design of power processing unit discussed in section 1.3, better performance is achievable using an advanced low voltage CMOS technology for a typical energy harvesting interface circuitry. In this chapter, the theory, design, and simulation results of different blocks of a complete energy harvesting interface electronics are explained, which have been designed in TSMC LVT 90 nm CMOS process.

Section 4.1 explains the overview of the IC by introducing each implemented block. Section 4.2 describes the design of ultra low voltage charge-pump circuit and the simulation results proving its improved performance over conventional charge-pumps. Section 4.3 presents the design of a low power ring oscillator based on current starving method to be utilized together with the charge-pump circuit of Section 4.2. Section 4.4 explains the theory, design and simulation results of a sub-threshold voltage regulator suitable for low voltage and low power energy harvesting applications. Finally, Section 4.5 summarizes this chapter by highlighting the achievements and important design points.

4.1 The Energy Harvesting IC Overview

Figure 4.1 shows the overview of the proposed architecture for the energy harvesting IC in TSMC 90 nm CMOS process. The energy harvesting IC includes different blocks which are implemented on the same chip, realizing a complete interface

electronics to be incorporated with an electromagnetic power generator. The maximum expected power consumption of each block has also been depicted. The designs for highly efficient rectifier including both passive and active designs have been fully explained in previous section in 0.35 µm CMOS process. In the remaining sections of this chapter, the more focus has been taken for the design and simulation results of each of the remaining blocks in Figure 4.1 including the DC-DC converter, the voltage regulator designs, and the power management unit, with expected maximum current consumption values.

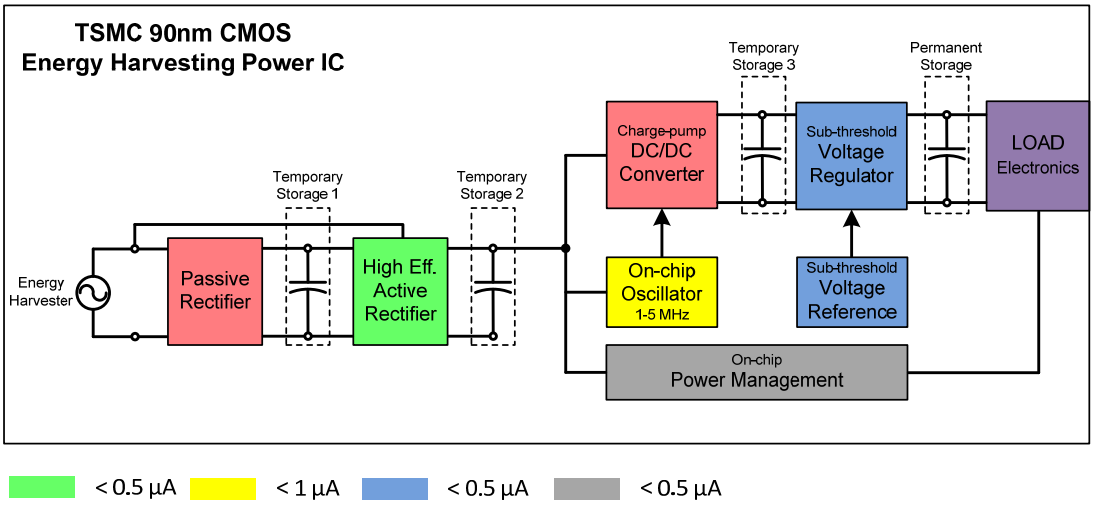


Figure 4.1: The overview of the proposed energy harvesting IC in 90 nm CMOS.

4.2 The Designed Charge-Pump DC-DC Converter

The theory and state-of-the-art designs for different charge-pump circuits have previously explained in section 2.3.2. In this study, a CMOS low voltage charge-pump circuit utilizing the cross connected transistors has been designed.

Figure 4.2 shows the schematic of the designed charge-pump circuit in TSMC 90 nm CMOS process. The V_{TH} problem which is the main source of low efficiency in most charge-pump circuits has been significantly solved using this design due to its replacement with the drain-to-source voltage which is much smaller than the threshold voltage.

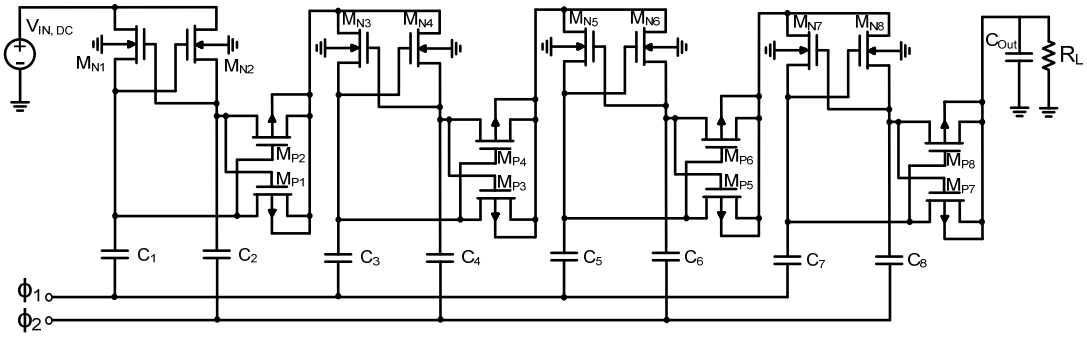


Figure 4.2: The 4-stage cross-connected CMOS charge-pump circuit for low voltage applications.

Figure 4.3 shows the simulated output voltages of the designed charge-pump circuit for R_L=100 kΩ and C_{out}= 100 pF. In order to make a comparison, the simulation results of conventional Dickson charge-pump have also been shown. The utilized cross-connected design shows a significantly higher performance due to its decreased threshold voltage mechanism. For the input voltages above 0.4 V, or load current higher than 4 µA, an output voltage of 1 V is generated at the output which is high enough to be used for driving other next blocks such as voltage reference block. The generated voltage stays above 2 V for the input voltages higher than 0.6 V.

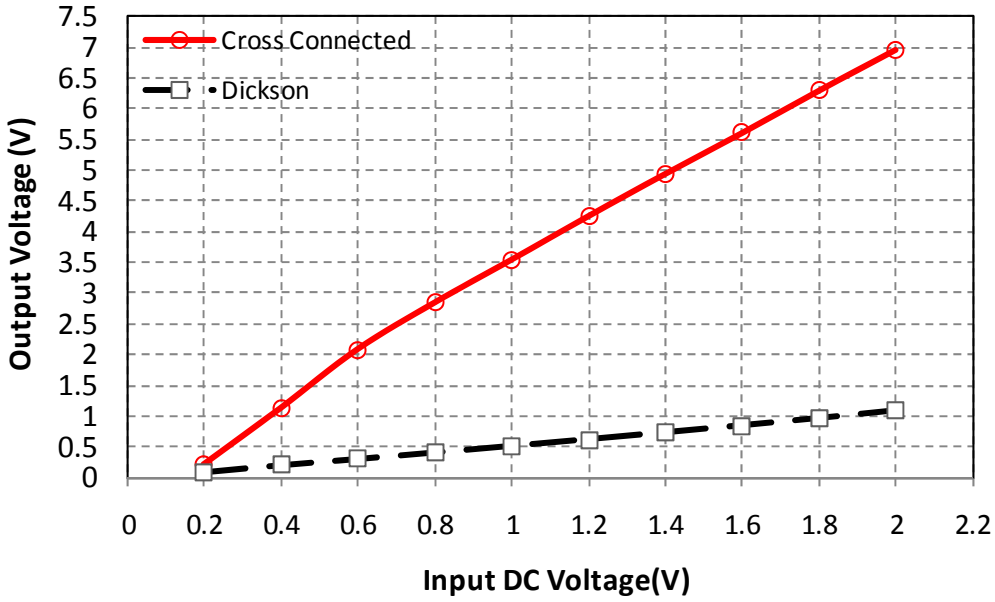


Figure 4.3: The simulated output voltages of the charge-pump circuits for R_L=100 kΩ and C_{out}= 100 pF.

The charge-pump circuits have also been tested under different load conditions for a fixed amount of input voltage. Figure 4.4 shows the generated output voltage of the circuits while the load value has been swept from 1 kΩ to 1 MΩ for an input voltage of 0.6 V. The cross-connected design is able to generate output voltages more than 1 V for the load values higher than 30 kΩ.

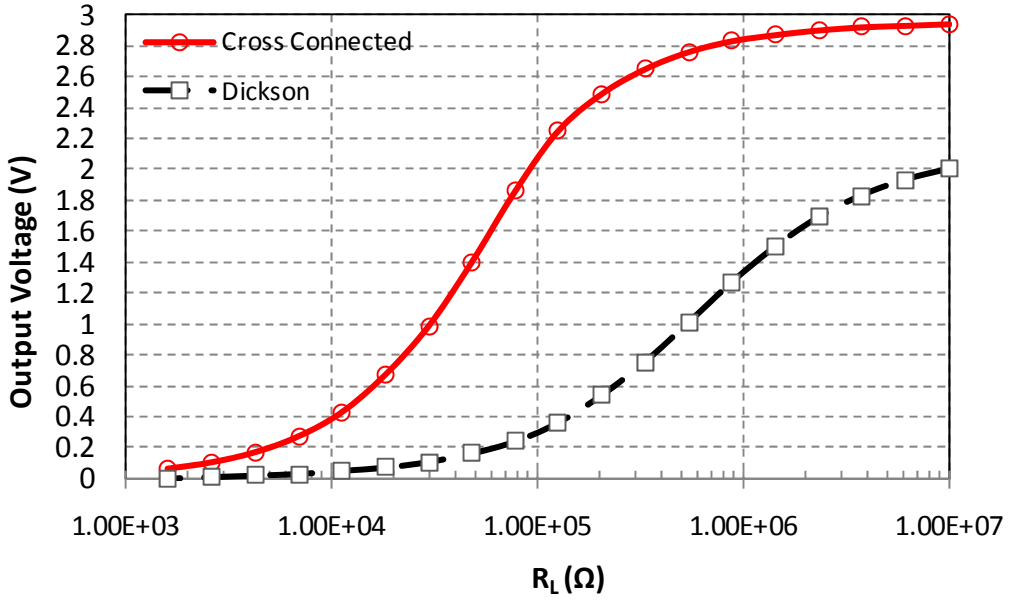


Figure 4.4: The output voltage of the circuits for different output loads for V_{in}=0.6 V.

Table 4.1: The design parameters of the charge-pump DC-DC converter.

Cross Connected	M_N and M_P (W/L)	5 µm / 200 nm
	C_1-C_8	5 pF
Dickson	M_N (W/L)	20 µm / 100 nm
	C_{pump}	5 pF

4.3 The Oscillator Design for the Charge-Pump Circuit

As shown in Figure 4.2, there are two non overlapping clocks in the design of the utilized charge-pump which expresses the need for an oscillator. Normally, ring oscillators are used to generate an on-chip oscillator in CMOS technology. The power consumption of a ring oscillator depends on the output load capacitor, operation frequency and the supply voltage. In this work, a current starved ring oscillator has been designed to greatly decrease the power consumption of the

oscillator as shown in Figure 4.5. The EN pin in the input of the NAND gate, enables the circuit to oscillate when is logic *high.* In this design, a separate current source formed by the left part of the circuit generates a current and biased the digital blocks of the oscillator using that current. A maximum total current of 1 μA is drawn from the power supply using this method for an oscillation frequency of 2 - 7 MHz.

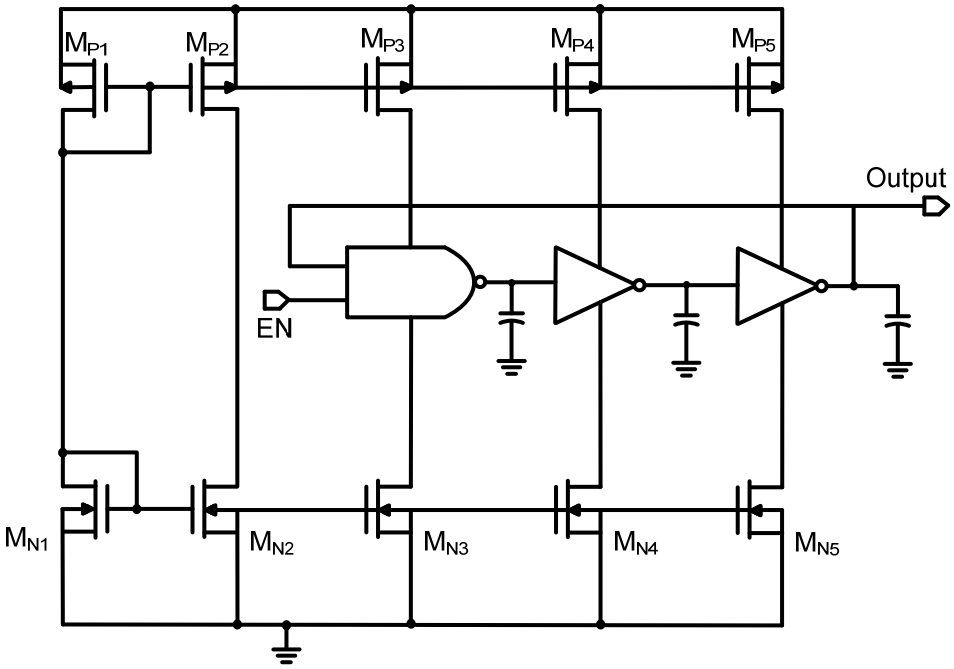


Figure 4.5: The current-starved ring oscillator designed in TSMC 90 nm CMOS process.

Table 4.2: The (W/L) of the ring oscillator circuit in Figure 4.5.

Transistor	W/L
M_{P1}	200nm / 20 μm
M_{N1}-M_{N5}	200nm / 600 nm
M_{P2}-M_{P5}	200nm / 600 nm
M_N, M_P (NAND)	200nm / 600 nm
M_N, M_P (INV)	200nm / 600 nm

4.4 The Designed Voltage Regulator

The theory and different designs for voltage regulators have been previously discusses in Chapter 2. There are a few architectures which are proposed for the low power energy harvesting applications and the main design for it has been shown in section 2.4.2. Figure 4.6 depicts the schematic of the designed voltage reference generator. It consists of a current source generator in the left and a circuit to create a supply and temperature independent voltage reference. The current source sub-circuit is based on a β multiplier self-biasing circuit and uses a MOS resistor M_R instead of an ordinary passive resistor. This greatly decreases the required area of the circuit by operating the M_R transistor in the linear region. The bias-voltage sub-circuit accepts the current through PMOS current mirrors and generates the reference voltage. The bias-voltage sub-circuit consists of a diode-connected transistor (M_{N5}) and two differential pairs (M_{N6}-M_{N7}, M_{N8}-M_{N9}) and is based on the translinear principle. All the MOSFETs are operated in the sub-threshold region except for MOS resistor M_R, which is operated in deep triode region. An operational amplifier and NMOS current mirror (M_{N1}, M_{N2}) are used to improve the power supply rejection ratio (PSRR) and line sensitivity of the circuit.

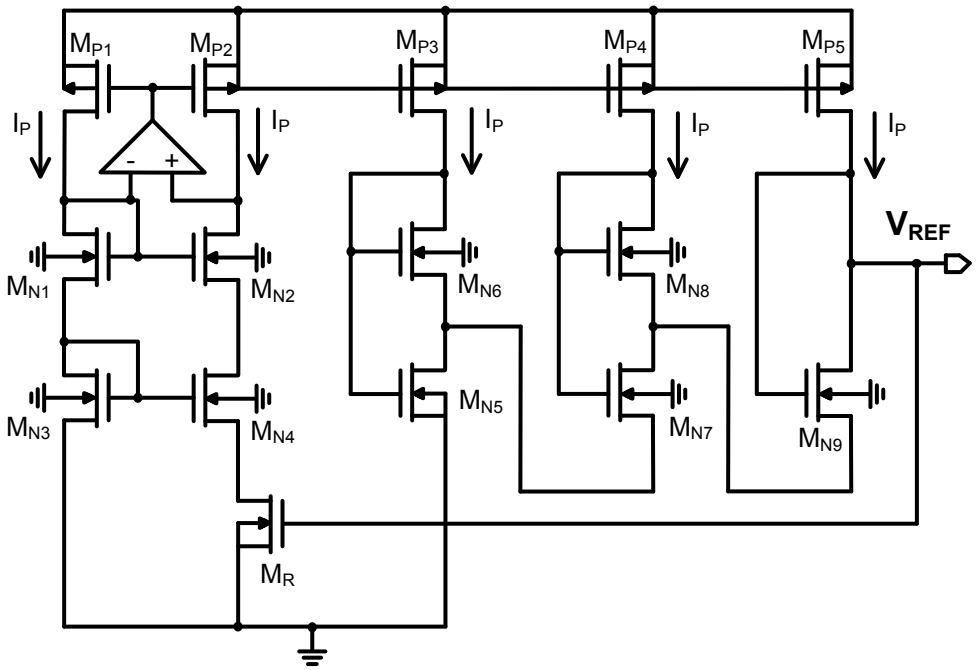


Figure 4.6: The schematic of the designed voltage reference in TSMC 90 nm CMOS.

The sub-threshold MOS current I_D can be expressed as

$$I_D = KI_0 exp((V_{GS} - V_{TH})/\eta V_T) \tag{4.1}$$

where K is the aspect ratio ($=W/L$) of transistors, $I_0 (= \beta(\eta-1)V_T^2)$ is the process-dependent parameter, V_T ($= k_B T/q$) is the thermal voltage, V_{TH} is the threshold voltage of a MOSFET, and η is the sub-threshold slope factor. In the circuit in Figure 4.6, the current I_P flowing in the circuit is determined by the ratio of M_{N3} and M_{N4} and the resistance of MOS resistor M_R, and it is given by

$$I_P = \beta(V_{REF} - V_{TH})\eta V_T ln(K_2 / K_1) \tag{4.2}$$

where β is the current gain factor. In the bias-voltage subcircuit, gate-source voltages of transistors ($V_{GS,\ MN5}$ through $V_{GS,\ MN9}$) form a closed loop with the reference voltage V_{REF}, so it could be found that,

$$\begin{aligned} V_{REF} &= V_{GS,MN5} - V_{GS,MN6} + V_{GS,MN7} - V_{GS,MN8} + V_{GS,MN9} \\ &= V_{GS,MN5} + \eta V_T ln(\frac{2K_6K_8}{K_7K_9}) \end{aligned} \tag{4.3}$$

where,

$$V_{GS.MN5} = V_{TH} + \eta V_T ln(3I_P / K_5 I_0) \tag{4.4}$$

Because the voltages in the V_{REF} equation have negative (V_{TH}) and positive (V_T) temperature dependence, respectively, a constant voltage reference circuit with little temperature dependence can be constructed by adjusting the size of the transistors. Note that the threshold voltages of the transistors in the source-coupled pairs (M_{N6}-M_{N7}, M_{N8}-M_{N9}) are canceled each other by source-coupled circuit configuration.

The temperature dependence of the threshold voltage can be given by $V_{TH} = V_{TH0} - \kappa T$, where V_{TH0} is the threshold voltage at absolute zero, and κ is the temperature coefficient of the threshold voltage [61]. On the condition where $V_{REF} - V_{TH0} << \kappa T$, temperature coefficient of reference voltage is,

$$\frac{dV_{REF}}{dT} = -k + \frac{\eta k_B}{q} ln\left\{ \frac{6q\eta k}{k_B(\eta - 1)} \frac{K_R K_6 K_8}{K_5 K_7 K_9} ln(\frac{k_2}{k_1}) \right\} \tag{4.5}$$

A constant voltage with a zero temperature coefficient could be achieved properly by setting the aspect ratios such that $dV_{REF}/dT = 0$ in equation (4.5). Then, the output voltage V_{REF} is given by

$$V_{REF} = V_{TH0} \tag{4.6}$$

Therefore, the circuit generates the threshold voltage of MOSFET (M_{N5}) at absolute zero temperature. Figure 4.7 shows the op-amp which has been used in Figure 4.6 and operates in the sub-threshold region. Table 4.3 presents the W/L ratio of the transistors which are used in Figure 4.6 and Figure 4.7.

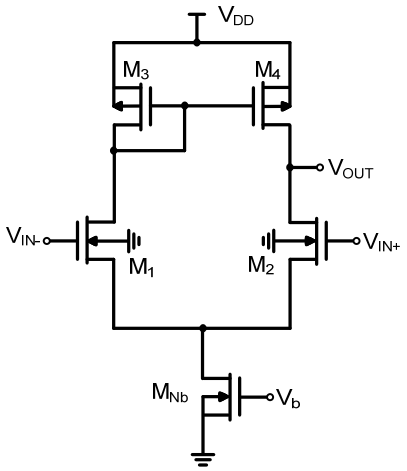


Figure 4.7: The sub-threshold op-amp which is designed and utilized in Figure 4.6.

Table 4.3: The W/L ratio of the transistors of the voltage reference generator.

Transistor	W/L
M_{P1}- M_{P5}	10 µm / 10 µm
M_{N1}, M_{N3}	60 µm / 3 µm
M_{N2}, M_{N4}	600 µm / 2.8 µm
M_{N5}, M_{N7}, M_{N9}, M_{Nb}	6 µm / 3 µm
M_{N6}, M_{N6}	252 µm / 3 µm
M_R	500 nm / 20 µm
M_1, M_2	2 µm / 2 µm
M_3, M_4	200 nm / 10 µm

Figure 4.8 shows the simulation results of the generated V_{REF} for different supply voltages. Based on the transistor configurations and design for temperature compensation, a reference voltage of 485 mV is generated while V_{supply} is slightly higher than 500 mV. The variation of V_{REF} is within the range of ± 6 mV for 0.6 < V_{supply} < 2.8 V. Figure 4.9 shows the output V_{REF} voltage for while the temperature has been swept within a range of 0º to 60º C, where the voltage variation is about 12 mV. The power consumption of the voltage reference generator is 1.5 µW at maximum.

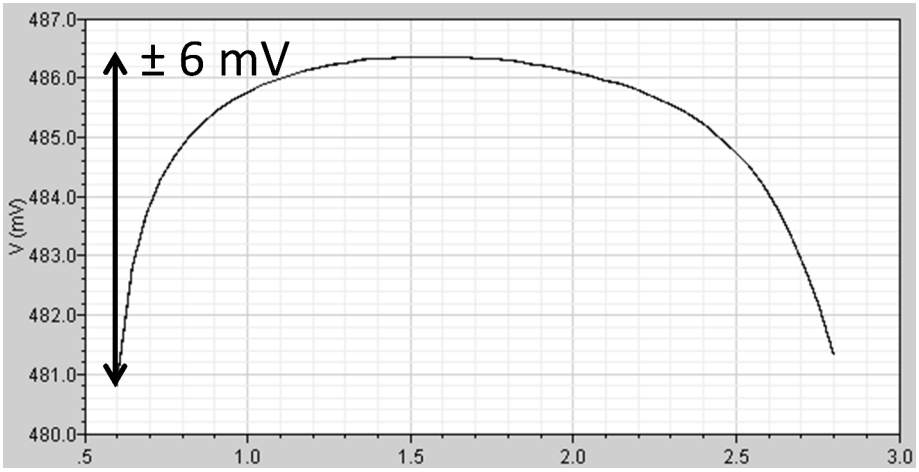


Figure 4.8: The generated V_{REF} for different supply voltages.

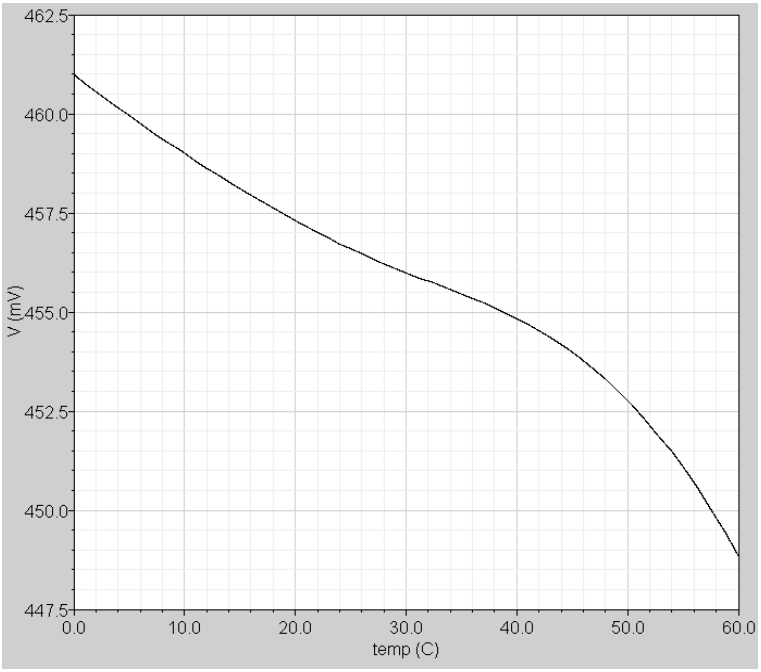


Figure 4.9: The generated V_{REF} for different temperatures.

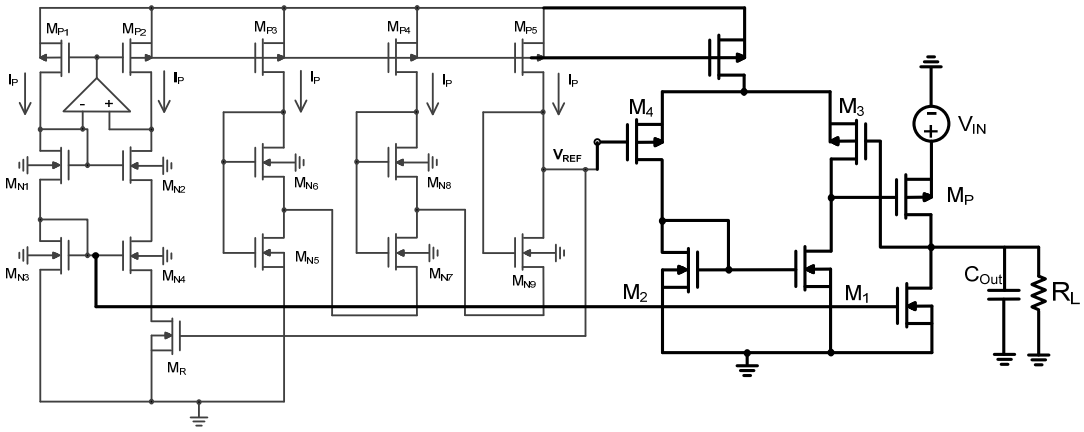


Figure 4.10: The voltage regulator stage with previously designed voltage reference.

Figure 4.10 shows the designed voltage regulator stage along with the previously designed voltage reference block. It consists of a PMOS input operational amplifier and a pass transistor to regulate the input voltages. The amplifier compares the voltage difference between the reference voltage and the output DC voltage and drives the pass transistor accordingly.

4.5 Summary of the Chapter

In this chapter, the design, and simulation results of the proposed architecture for energy harvesting IC in TSMC 90 nm CMOS process, has been demonstrated. The designed ASIC includes different blocks which are required to realize a complete energy harvesting interface electronics. The designs that were discussed in this chapter include the charge-pump DC-DC converter, the on-chip ring oscillator, and an ultra low power voltage regulator block. The achieved power consumption of each block is the least, reported in the literature. The proposed IC is a novel solution to be interfered to low voltage and low power micro power generators.

CHAPTER 5

THE EXPERIMENTAL RESULTS AND IMPLEMENTED ENERGY HARVESTING SYSTEMS

This chapter describes the experimental measurements related with the fabricated energy harvesting IC and the constructed energy harvesting *systems*. Firstly, the proposed block diagram for each energy harvesting system is given in which each type of the energy harvester module is integrated with its interface electronics depending on the characteristics. Then, the design and implementation of the constructed prototype is explained. Finally, the constructed energy harvester systems have been tested at different external vibration conditions and the performance parameters of the system including the energy harvester mechanical characterization and results of the interface electronics for each input excitation have been explained. Section 5.1 describes the implemented energy harvesting system by using discrete components. Although it is not a very efficient system, it shows the feasibility of integrating the energy harvesting module with circuitry and highlights the important parameters for an efficient system design. Section 5.2 explains the measurement results of the system which is composed of an energy harvester based on frequency-up-conversion method and a highly efficient passive rectifier in 0.35 μm CMOS process. In Section 5.3, a modified version of the system in 5.2 is presented in which the same circuitry is combined with an energy harvester module which operates in a smaller frequency range, suitable for ultra low frequency applications. Section 5.4 describes operation and measurement results of a very compact electromagnetic energy harvesting system. Section 5.5 ends this chapter by explaining the system which uses an energy harvester module similar in Section 5.4 and an active rectifier

for converting the generated power with maximum efficiency. Also, the proposed architecture for providing the power of the active rectifier using a network of small sized discrete components is explained

5.1 The Energy Harvesting System Utilizing Discrete Components

In this section, the implementation and measurement results of an energy harvesting system which uses an interface electronics by discrete components, is explained. The feasibility of integrating an energy harvester with some electronics, the effect of threshold voltage on the total performance of the system, and the powering up a commercial IC using the provided supply has been demonstrated.

5.1.1 The System Block Diagram

Figure 5.1 shows the block diagram of the system based on discrete components. A two stage Dickson charge pump circuit has been used to realize the rectification and step up as described in section 2.2.1. A transformer (1:15) has also been used to efficiently step up the AC voltage at the first stage to avoid the use of more low-efficient charge pump stages. The last stage enclosed in a dashed box in the figure is used as a realistic active load including a commercially available IC, as discussed later in next section.

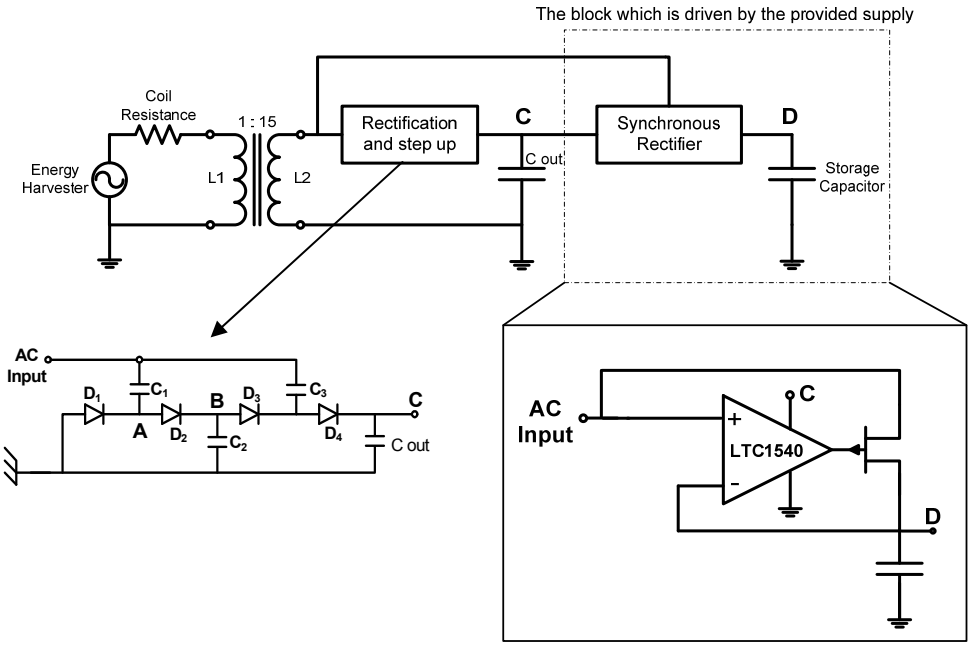


Figure 5.1: The block diagram of the system based on discrete components.

5.1.2 The Frequency Up-Conversion Energy Harvester

The utilized electromagnetic energy harvester, or micro-power generator, was constructed at our lab based on *mechanical* frequency up-conversion [2, 3] technique, as depicted in Figure 5.2 (a). The structure consists of a fixed-free cantilever beam with a pick-up coil attached on the free edge, a magnet placed on a vibrating diaphragm, and a mechanical barrier arm. The system is designed in a way that the resonance frequency of the cantilever is much higher than the resonance frequency of the support to realize the mechanical frequency up-conversion. This module is beneficial for harvesting very low frequency ambient vibrations (< 10 Hz).

Figure 5.2 (b) and (c) show the operation principle of the energy harvester module. At the presence of low frequency external vibrations, the support carrying the magnets move from its rest position (a), upwards (b), or downwards (c), following the initial acceleration. The barrier arm touches, bends, and releases the cantilever during this movement. When the cantilever is released, it vibrates at its resonance frequency, which is much higher than the ambient vibration frequency. The same stimulus occurs when the support is moving in the opposite direction.

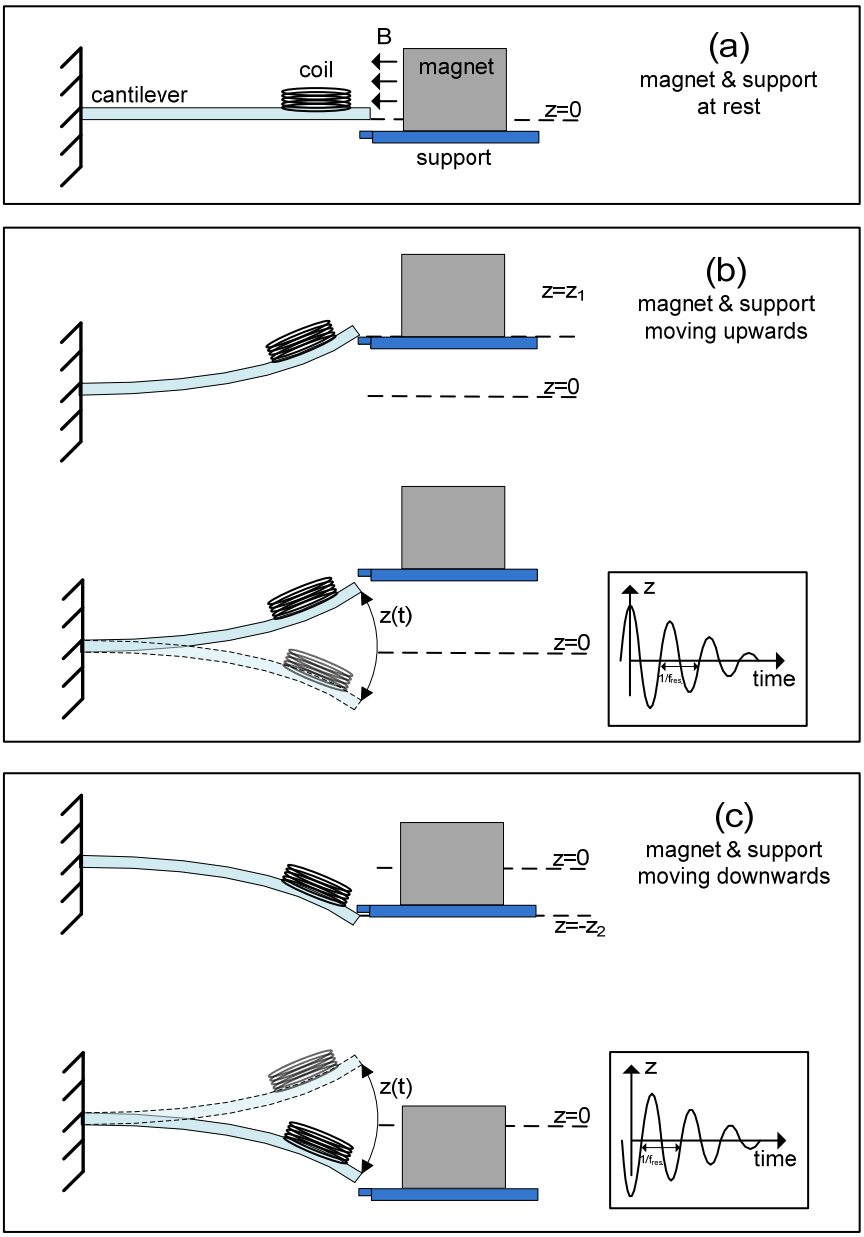


Figure 5.2: The EM harvester operation principle: (a) rest position; support moving (b) upwards, and (c) downwards [36].

As a result, up-conversion is realized twice in each period of the excitation. This causes a change in the relative position of the pick-up coil with respect to the magnet, and a decaying sinusoidal voltage is induced across its terminals with a frequency much higher than the excitation frequency. With this, higher power levels could be harvested from low ambient vibration frequencies. The detailed analysis and simulation results of the utilized energy harvester structure have been previously

reported in [21]. Figure 5.3 shows the output voltage waveform across the pick-up coil at an excitation frequency of 5 Hz.

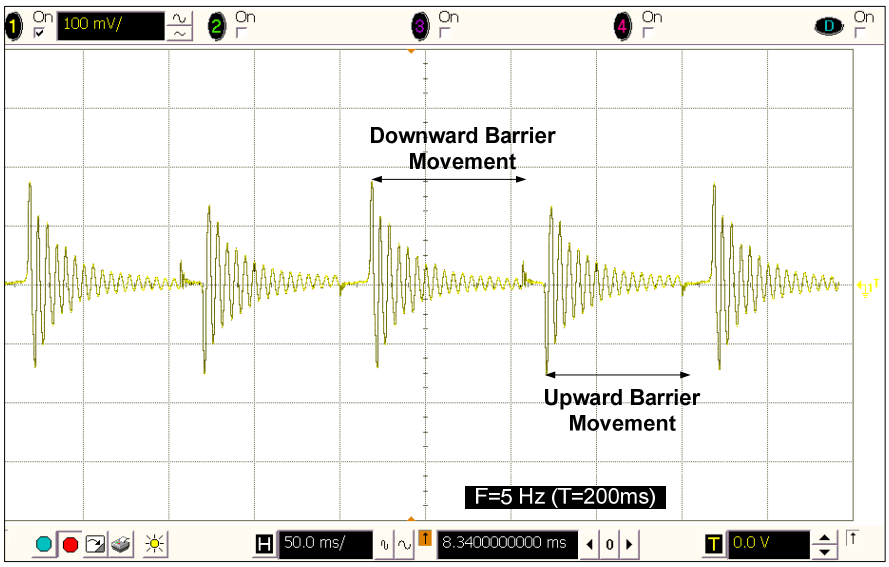


Figure 5.3: The measured output voltage of the energy harvester at $F_{excitation}$=5 Hz.

5.1.3 The Experimental Results

Figure 5.4 depicts the constructed energy harvester prototype based on frequency up-conversion technique. The cantilever is 9 mm long, 7.5 mm wide with two cascaded 7.5×7.5×7.5 mm^3 magnets placed on the support. The displacement of the cantilever tip before release from its rest position is around 2 mm. The diaphragm is vibrated at an excitation frequency of 5 Hz with a shaker table, imitating the ambient vibration. The up-converted frequency, or the resonance frequency of the cantilever, is around 150 Hz in this prototype.

The schematic of the rectifier stages has been depicted in Figure 2.5 at section 2.2.2. Two rectifier circuit prototypes were built, one using standard V_{TH} IN4007 diodes, and the other using lower V_{TH} Germanium 1N60 Schottky diodes. The capacitance values are selected as C_1=C_2=C_3=1 µF, and C_4=C_{out}=10 µF (Figure 2.5) to minimize output ripple. Figure 5.5 shows the output 4.5 V DC which is achieved for a load current of 5 µA, which has a generally acceptable output ripple of only 2.5%.

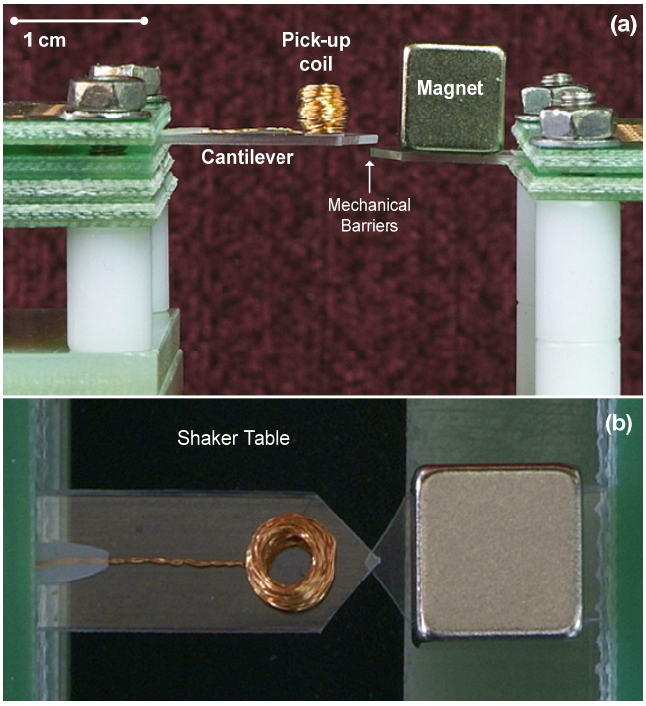


Figure 5.4: (a) Side, and (b) top view of the constructed harvester prototype.

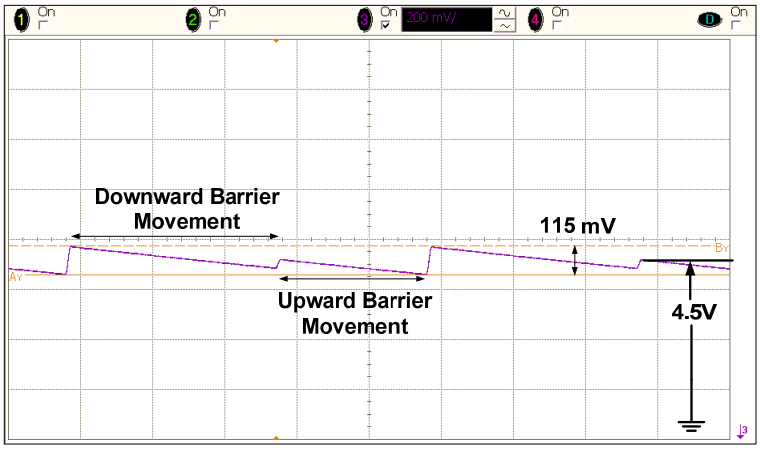


Figure 5.5: The output DC voltage of the system using C_{out}=10 µF at I_{Load}=5 µA.

Figure 5.6 indicates the measured sensitivity curves for output voltage, output power, and power conversion efficiency for both regular diode and Schottky 1N60 diode implementations. The output voltage, power, and power efficiency of the two variations of the interface circuit are validated with a range of resistive loads. The schottky diode implementation performs better than the implementation with regular diodes due to the lower threshold voltages. For the load current between 15-20 µA, an efficiency of 35% is achieved using schottky diodes, whereas the efficiency does not exceed 25% using regular diodes.

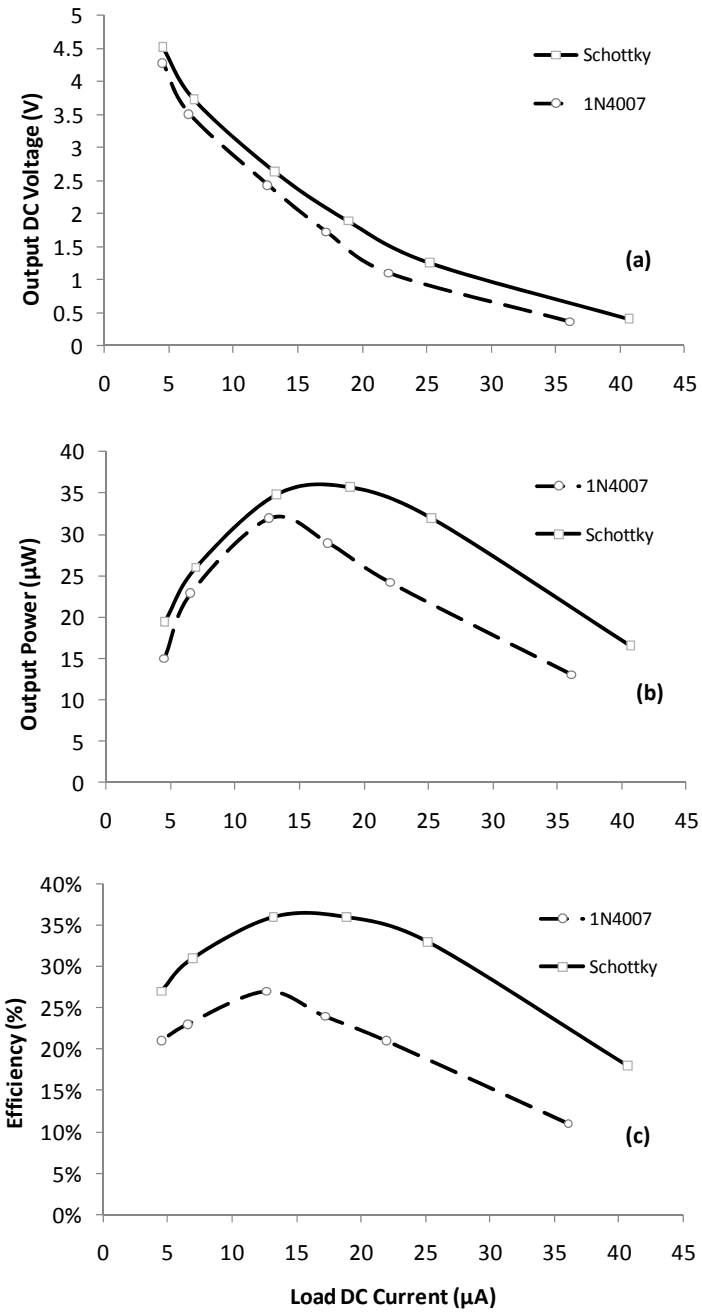


Figure 5.6: The (a) output DC voltage, (b) output power, and (c) power conversion efficiency, with varying DC load current, and V_{TH}.

A comparator in synchronous rectifier configuration (Figure 5.1) was selected as the active load [5] to demonstrate a real application of the provided supply of the energy harvester. The LTC1540 comparator IC has been used at the core of the active rectifier which compares the input AC voltage to the output DC voltage at node D, utilizing the provided voltage of the system at node C. Figure 5.7 shows the synchronous rectifier output. A voltage of 2.5 V is achieved at the output of node D.

The top smooth signal shows the output DC voltage at node D. The level of the highest peak of the stepped up AC signal at the second winding of the transformer is 3 V and is also shown in Figure 5.7.

Figure 5.7: The stepped-up harvested voltage and the output DC voltage of the synchronous rectifier.

In this system, an interface circuit is presented for a vibration based electromagnetic (EM) energy harvester which works with the mechanical frequency-up-conversion principle. The AC signal of the Energy Harvester is fed to the circuit and an acceptable value for the output voltage with a reasonable ripple is achieved. At load current of 5 µA, a DC voltage of 4.5 V with a 2.5% ripple is achieved. The maximum power efficiency of 35% is validated with a voltage range of 2–2.5 V and a load range of 15–20 µA. It was concluded from the experiments that the combined efficiency of the rectification and step-up could be further improved when the design is integrated into an IC process with low V_{TH} options.

5.2 The Energy Harvesting System Utilizing Highly Efficient CMOS Passive Rectifier Operating at 10 Hz

This section presents the constructed vibration-based electromagnetic energy harvesting system utilizing the novel and highly efficient passive interface electronics. This system is composed of an energy harvester module, and a compact 0.35 µm CMOS IC, which have been previously explained. The proposed system is realized as a complete System-on-Package and is fully validated. It is capable of powering a 1.5 V, 15 µA load with 65% conversion efficiency, and 5% ripple, at an

external vibration frequency of 10 Hz. The recorded efficiency is the highest achieved value for vibration-based EM energy harvesters with passive rectification to the best of author's knowledge.

5.2.1 The System Block Diagram

The energy harvesting module operates based on the same principle as described in 5.1.2, up-converting the environmental low frequency vibrations for increased AC power output. The interface circuitry is based on the proposed passive boot-strap rectification technique (BSR) which has been fully explained in 3.3. Figure 5.8 depicts the block diagram of the proposed system. The system consists of an energy harvester module, a transformer, a power IC, and an external output capacitor to store the converted DC voltage. The generated AC signal is stepped up using a (1:10) small-sized transformer. The power IC converts the stepped-up AC signal to DC by using a boot strap rectifier (BSR), and stores it on the output capacitor. Two other state-of-the-art rectifiers (explained in 3.2) are implemented on the same chip, in addition to the proposed BSR, to make a realistic performance comparison. Figure 5.9 shows the wire-bonded 0.35 µm CMOS ASIC which is used during testing.

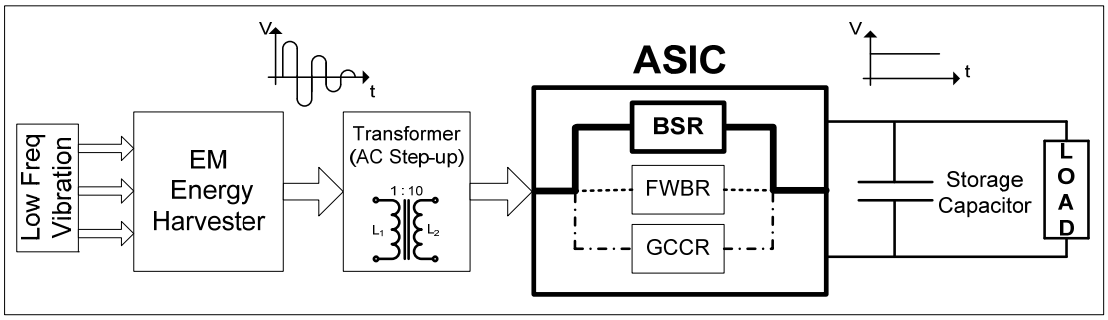


Figure 5.8: The block diagram of the proposed system operating at 10 Hz.

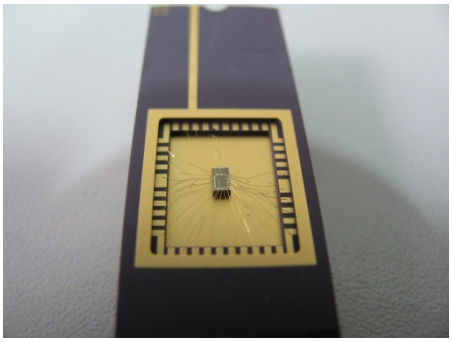


Figure 5.9: The implemented 0.35 µm CMOS ASIC packaged for testing.

5.2.2 The System Implementation and Experimental Results

Figure 5.10 depicts the constructed prototype of the proposed system. The electromagnetic energy harvester module consists of a fixed-free cantilever beam with a 200-turn pick-up coil attached on the free edge, two cascaded 7.5×7.5×7.5 mm^3 magnets placed on the diaphragm, and a mechanical barrier arm. The generated voltage across the coil terminals is stepped-up with a (1:10) transformer. The power IC which does the AC/DC conversion is placed on a ceramic substrate and the generated DC voltage is stored on a 10 µF capacitor.

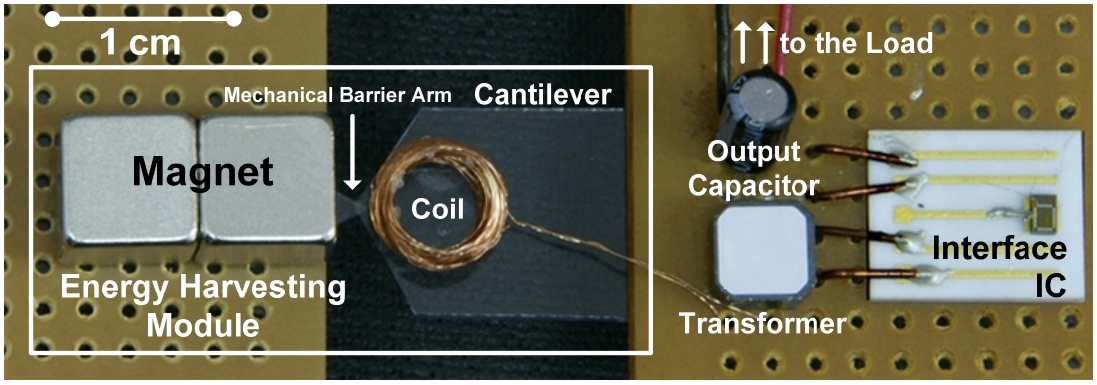


Figure 5.10: The constructed energy harvesting system prototype.

The constructed energy harvesting system has been tested using a shaker setup. Figure 5.11 shows the full test setup, which is composed of a shaker table, a control unit, an amplifier, an accelerometer, and an interface computer. The desired control input values, such as acceleration, velocity, and displacement levels, are all entered to the system through the user interface running on a computer.

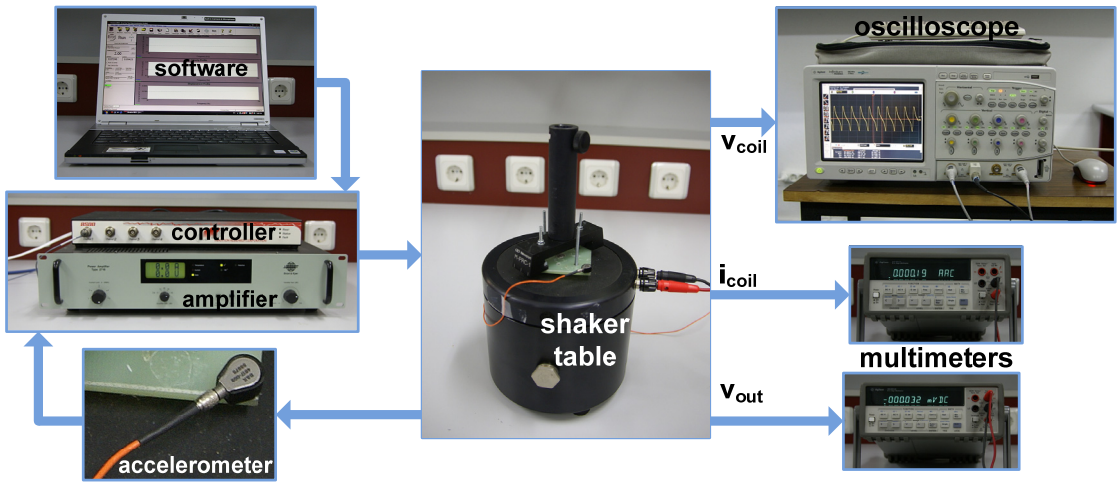


Figure 5.11: Test setup and photograph of the components and measurement devices.

The energy harvester module has been stimulated at 10 Hz external vibration frequency for each of the validated circuit types. Two periods of the generated voltage at the energy harvester terminals are depicted in Figure 5.12 after step-up using the transformer, while the up converted frequency is around 100 Hz.

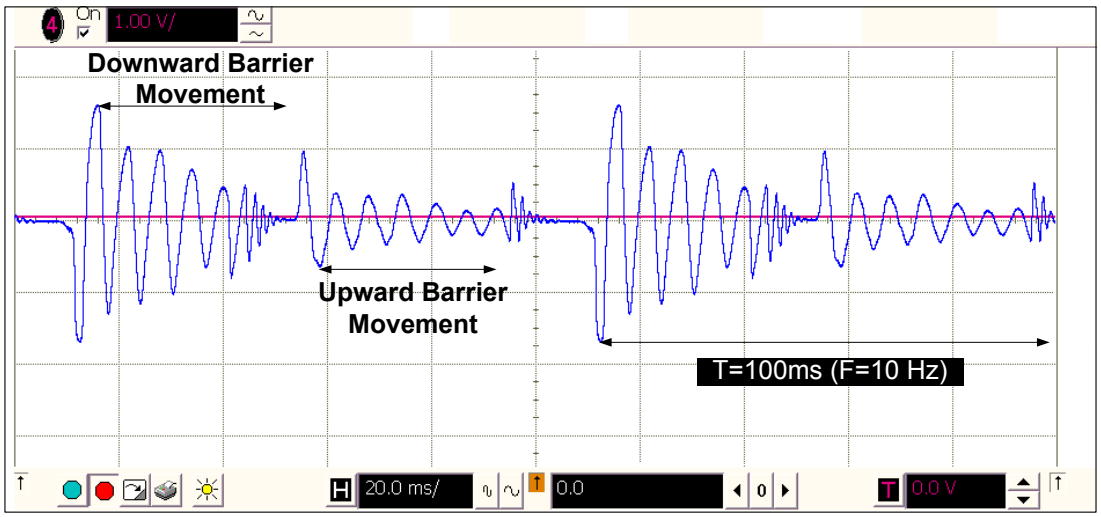


Figure 5.12: The generated output voltage of the energy harvester after the step-up.

All three implemented circuits have been validated with the same energy harvester module to provide a realistic comparison. The load current for each circuit was swept within 2 - 42 µA range by modifying a resistive load connected in parallel with the output capacitor. The output voltage, the output power, and the power efficiency of the rectifiers have been characterized for each configuration. Figure 5.13 presents the validation results. A maximum efficiency of 65% for 1.5 V, 15 µA

load is achieved with the proposed BSR design, whereas the conversion efficiency is less than 30% for FWBR and GCCR designs, proving the significance of the reduced threshold voltage of BSR diodes. The improvement in the efficiency is roughly 100% compared to the previously reported interface circuit topologies.

Figure 5.14 depicts the output DC voltage and its ripple, generated by the BSR circuit. The ripple value is 67 mV over 1.4 V, which is less than 5% of the output voltage level for a 10 μF storage capacitor. The ripple values associated with FWBR and GCCR are also presented for the same voltage, showing that the BSR circuit provides a better ripple performance.

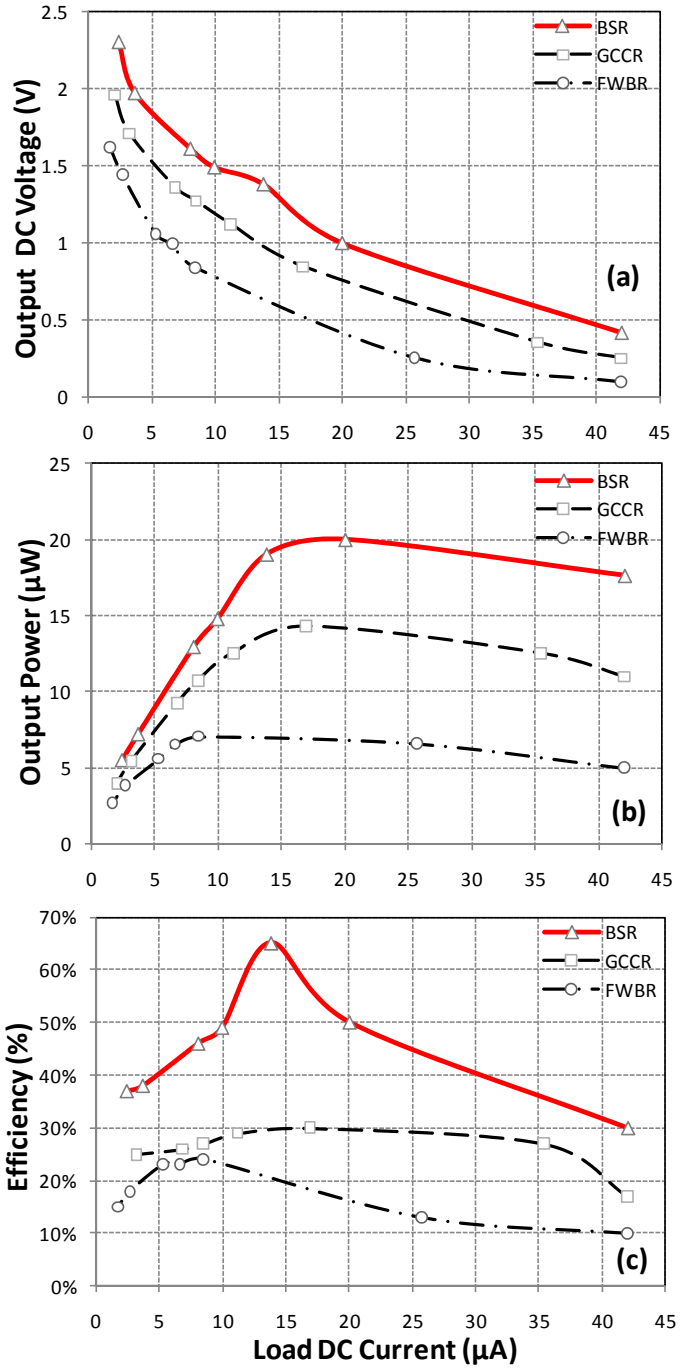


Figure 5.13: (a) The output voltage, (b) the output power, and (c) the power conversion efficiency of different rectifiers versus the output load current. The current is swept within a 2 - 42 µA range.

Table 5.1 presents the comparison of performance results using 3 rectifiers for the proposed system operating in 10 Hz and Table 5.2 summarizes the proposed system specifications. The results of this work have been presented in Transducers'11 conference [15].

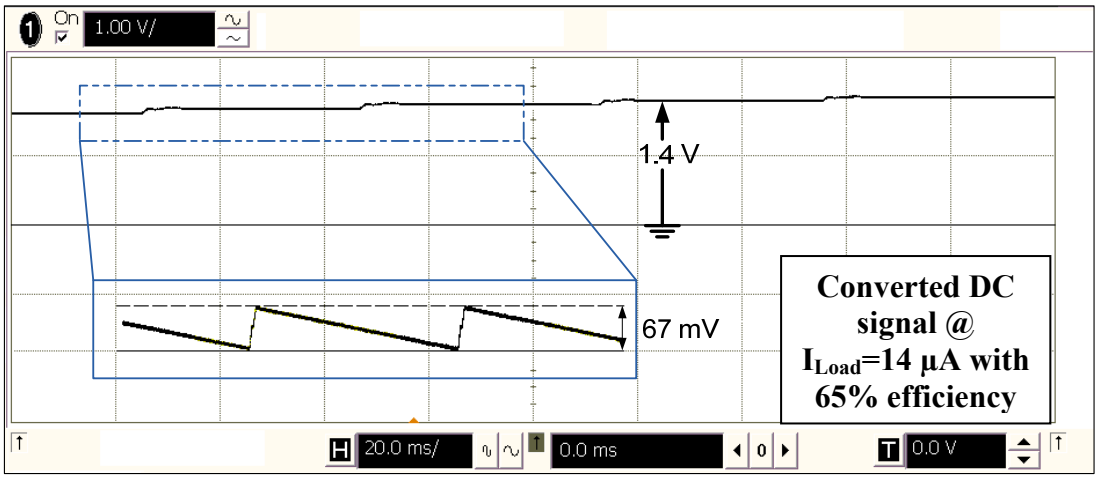


Figure 5.14: The output DC voltage of BSR and the ripple values for different rectifiers at V_{out}=1.4 V.

Table 5.1: Comparison of performance results using 3 rectifiers for the proposed system operating in 10 Hz.

Rectifier	**P_{max} (µW)**	**Efficiency (%)**	**Ripple (mV)**
FWBR	7.5	25	86
GCCR	14.5	30	126
BSR	**20**	**65**	**67**

Table 5.2: The proposed system specifications operating in 10 Hz.

Operation Frequency	10 Hz
Magnet Specification	Two NdFeB Magnets 7.5×7.5×7.5 mm^3
Saturation Magnetization	1.2 T
Number of coil turns	200
Interface IC Technology	X-FAB 0.35 µm CMOS
Max. power conversion efficiency	65% (for 1.5 V 15 µA load)
Max. output power	22.5 µW
Max. output voltage ripple	67 mV (over 1.5 V)

5.3 The Energy Harvesting System Utilizing Highly Efficient Passive Rectifier Operating at 2 Hz

This section describes the results of an electromagnetic energy harvesting system operating at very low frequency vibrations (< 5 Hz). In order to achieve high power output from ultra low frequency vibrations, the same frequency up-conversion mechanism has been used for realizing the energy harvester module. Also, a new prototype is constructed utilizing the larger volume magnets and higher turn coil. The complete system has a larger volume compared to the presented system at section 5.2; however it is able to harvest high power at presence of ultra low vibration frequencies. Furthermore, the reliable operation of a commercially available temperature sensor, as a realistic load, has also been demonstrated by using the energy harvester as a DC supply, operating at minimum external vibration level.

5.3.1 The System Implementation

The system block diagram is the same as in Figure 5.8 where the passive BSR design has been used as the interface electronics for efficient power conversion. Figure 5.15 shows the implemented energy harvesting system which is designed to operate for ultra low frequency vibrations. The electromagnetic energy harvester module consists of a fixed-free cantilever beam with a pick-up coil attached on the free edge, five cascaded cylindrical magnets placed on a support. Two mechanical barrier arms are formed on the tip of the cantilever and the support. The generated voltage across the coil terminals is stepped-up using a (1:4) transformer. The coil has 1000 turns and its resistance (47 Ω) is matched to the primary DC resistance of the transformer to transfer the maximum power from the coil to the interface electronics. The power ASIC which does the AC/DC rectification is placed on a ceramic substrate and the generated DC voltage is stored on a 10 μF SMD capacitor. The stepped-up AC signal is converted to DC by using the passive interface electronics and is stored on the output capacitor. The core of the AC/DC converter is a boot-strap rectifier (BSR) as in 5.2 which is able to rectify the induced AC voltage with high efficiency without using any external battery or start-up circuitry. Similarly, two other most commonly used passive rectifiers are also implemented on the same chip, in addition to the proposed BSR, to make a realistic performance comparison. The details of the utilized interface electronics are given in Table 5.3. The resistive loads have been

used to validate the interface electronics; in addition, a series of temperature sensors have also been used as the load to prove the operation of the energy harvesting system at low vibration levels (< 100 mg).

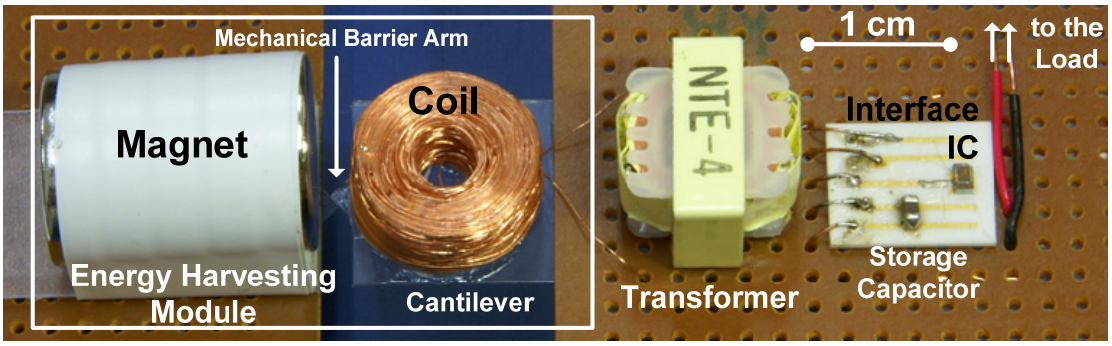


Figure 5.15: The constructed prototype of the energy harvesting system operating at 2 Hz.

Table 5.3: Specifications of the interface electronics.

IC Technology	X-FAB 0.35µm 2P4M CMOS
Active Chip Area	BSR: 120µm×170µm GCCR: 50µm×50µm FWBR: 30µm×40µm
Chip Area with Bond Pads	0.3 mm^2
CMOS $\|V_{TP}\|/V_{TN}$	0.73V/0.55V
On-chip C_{BS}	poly-poly, 5 pF
Storage Capacitor	10 µF, AVX-CER 0805
Capacitor Dimensions	2 mm ×1.25 mm ×0.5 mm
Transformer Type	NEUTRIK, NTE-4

5.3.2 The Experimental Results

The constructed energy harvesting system has been tested using a shaker setup, the same as in Figure 5.11. Figure 5.16 shows two periods of the generated AC voltage where an excitation frequency of 2 Hz has been up-converted to 100 Hz, under 72 mg peak acceleration while no interface network is connected.

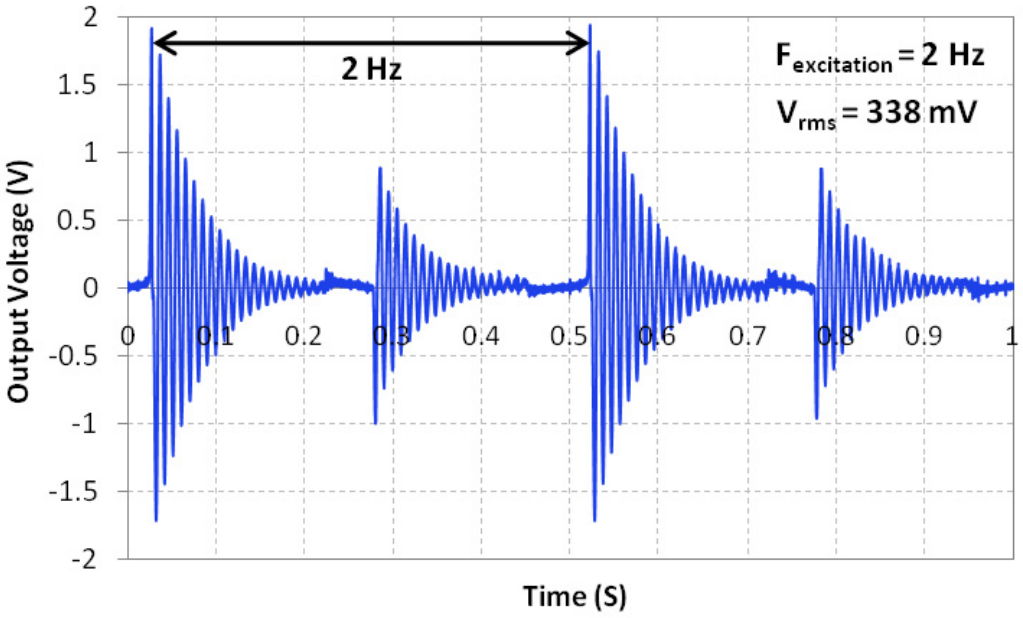


Figure 5.16: The generated AC voltage under 2 Hz, 72 mg peak acceleration excitation.

The constructed system has been tested at different external vibration conditions and the performance parameters have been recorded. The energy harvester module was validated to operate under ultra low vibration levels over a frequency range of 2 Hz-10 Hz and acceleration range between 0.072g - 1.81g. The system is targeted to operate at very small vibration frequency and acceleration (< 100 mg) levels which are abundant in many environments and generate DC voltage usable by an external load. The constructed system is able to operate at higher frequency and acceleration excitations; however, the test results are limited with the operation range of the shaker setup.

Figure 5.17 presents the performance characterization results of the energy harvesting system utilizing BSR as the interface electronics in terms of the generated

output voltage (Figure 5.17 (a)) and power (Figure 5.17 (b)) for several output load currents at four different excitation frequencies. For this characterization, the output DC load current is measured as:

$$I_{out} = \frac{V_{out,DC}}{R_{Load}} \tag{5.1}$$

where $V_{out,\ DC}$ is the converted output DC voltage, which is stored on the output capacitor, and R_{Load} is the resistive load at the output. The input power is measured as the *rms* AC power and the output power is the converted DC power on the storage capacitor as follows:

$$P_{input} = I_{Coil[rms]} \times V_{Coil[rms]} \tag{5.2}$$

$$P_{out} = I_{out} \times V_{out,DC} \tag{5.3}$$

The conversion efficiency of the active rectifier is the ratio of the total DC output power to the generated AC input power:

$$Conversion\ \ Efficiency\ \ [\%] = \frac{P_{out}}{P_{input}} \times 100 \tag{5.4}$$

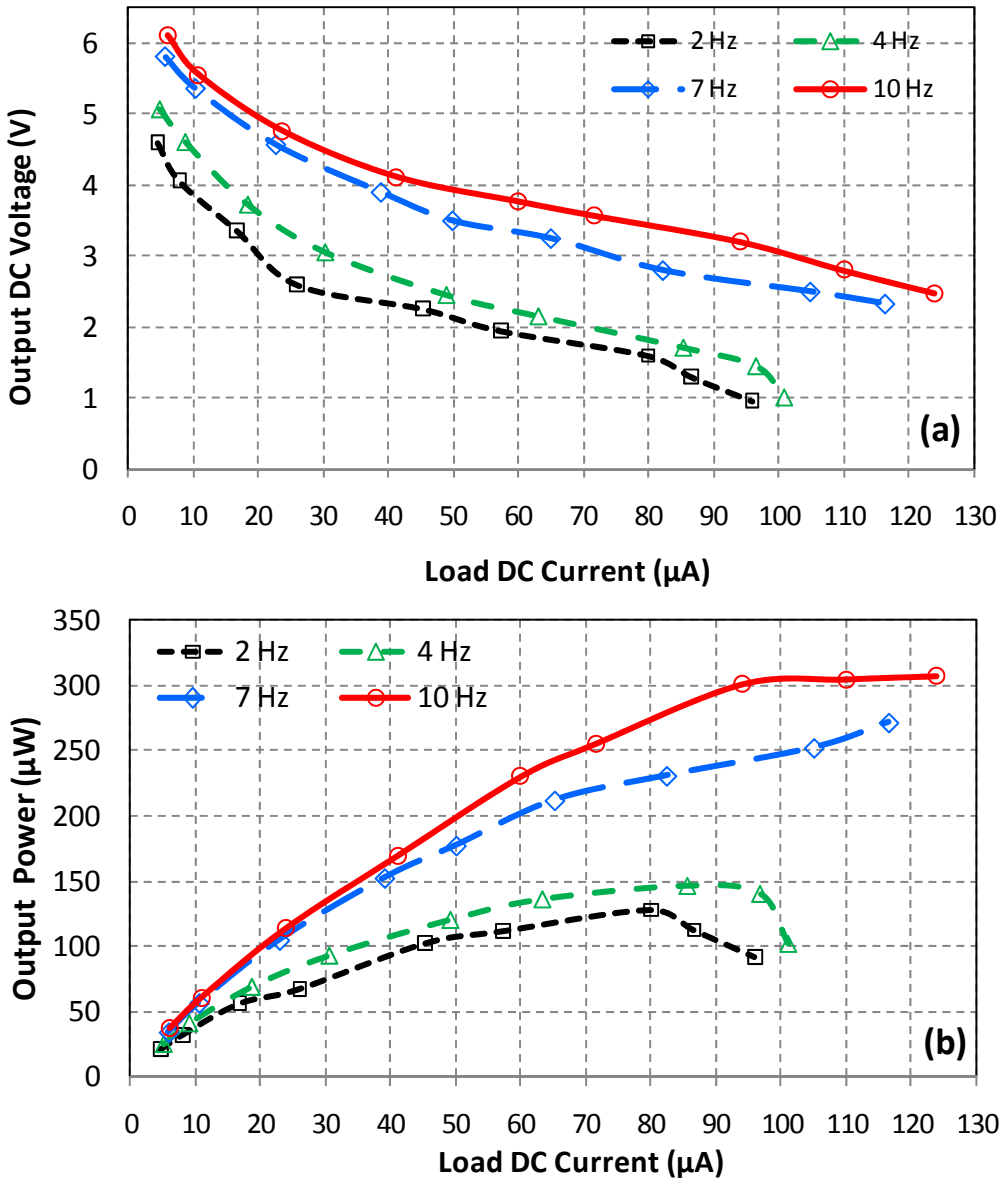


Figure 5.17: The converted output DC voltage and output power of the system utilizing BSR as the interface electronics for different load currents under four excitation frequencies while excitation displacement is 9 mm.

It is seen from Figure 5.17 (a) and (b) that, as the excitation frequency increases, the converted output voltage and power is continuously increased for higher operation frequency values, due to the higher available generated power of the energy harvester. However, the range is limited at lower frequencies due to the less available generated power at higher load current, since the storage capacitor is fully discharged and a very small DC voltage is stored for high load currents. At higher

excitation frequencies, the generated power is also expected to start decreasing at some point farther than the one for lower frequencies.

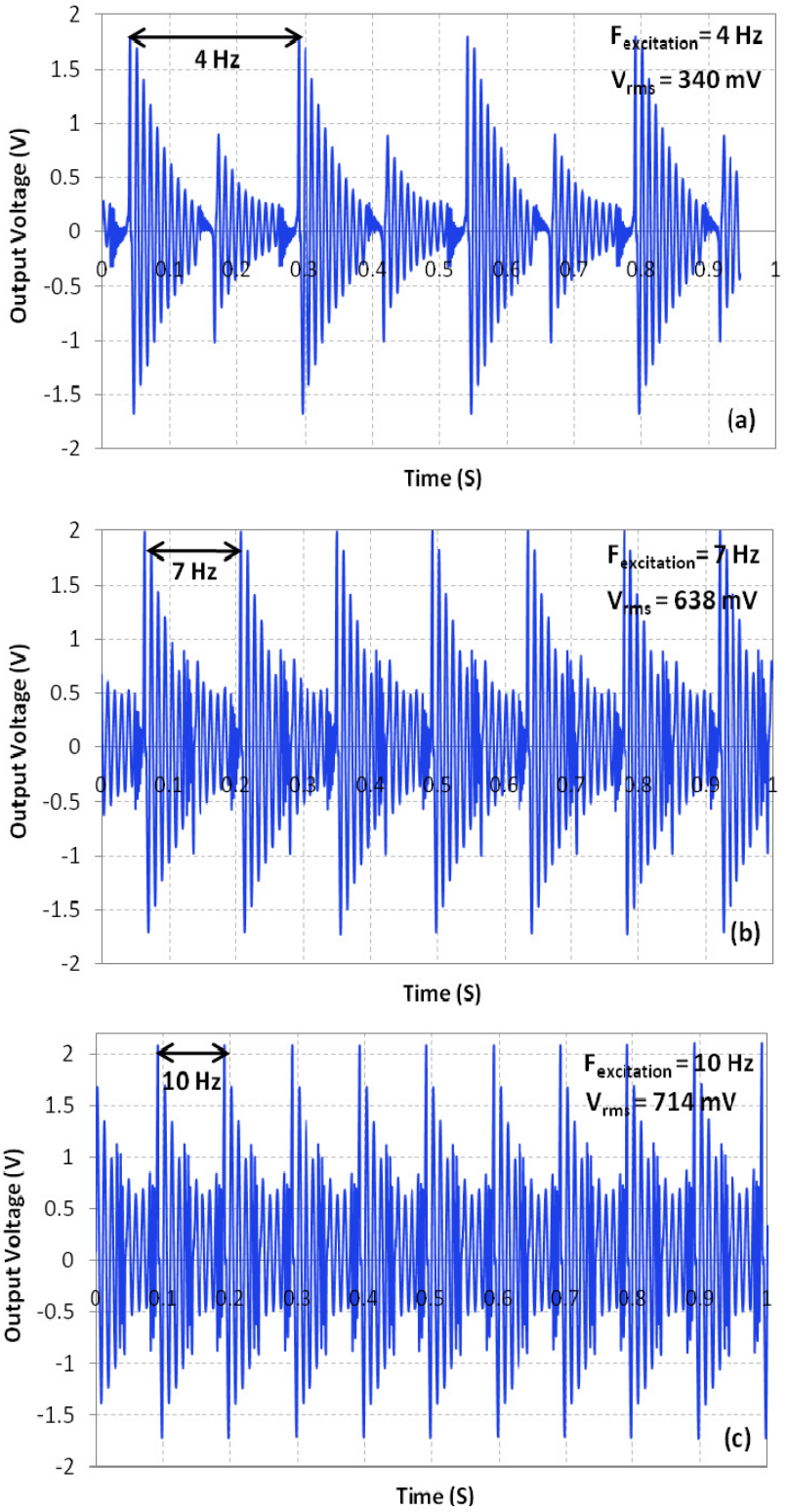


Figure 5.18: The generated AC voltage across the coil of the energy harvester module for (a) 4 Hz, (b) 7 Hz, and (c) 10 Hz excitation frequency while BSR interface circuit is connected at no-load output condition.

Figure 5.18 shows the generated voltage waveforms across the coil of the energy harvester for three different excitation frequencies, where the up-converted frequency is the same (100 Hz) for all three cases as it depends on the resonance frequency of the cantilever. The generated voltage of the energy harvester decays after the release of the cantilever, until the next contact to the support (Figure 5.16). However, at higher vibration frequencies, the *rms* value of the generated voltage is increased due to the fact of shorter intervals between damping of the decaying sinusoidal waveform. Therefore, the finally converted output voltage and power is increased. This implies a higher rate for charging the output capacitor at higher excitation frequencies, which accounts for the increased output voltage and output power of the system (Figure 5.17).

The maximum achieved output power of the energy harvesting system operating at 2 Hz, 72 mg peak acceleration, is 128 μW at 80 μA load current where a 1.6 V DC voltage is generated. It is also possible to extract a 310 μW of DC power over a 2.5 V load and 124 μA under an excitation frequency of 10 Hz.

Figure 5.19 presents the comparison results of the output voltage, the output power, and the power conversion efficiency of three implemented rectifiers on the same IC, which have been tested with the same energy harvester module at 2 Hz and 72 mg external vibration. The load current for each circuit is swept within 5 - 95 μA range by modifying a resistive load connected in parallel with the output capacitor. A maximum efficiency of 75% for 3.4 V, 17 μA load is achieved with the proposed BSR design, and the efficiency stays above 60% for a relatively wide range of load currents (< 50 μA). The maximum generated output power is 40 μW and 55 μW for the FWBR and GCCR designs, respectively, which is less than half of the proposed structure (128 μW) under the same conditions. Table 5.4 presents the specifications of the proposed system.

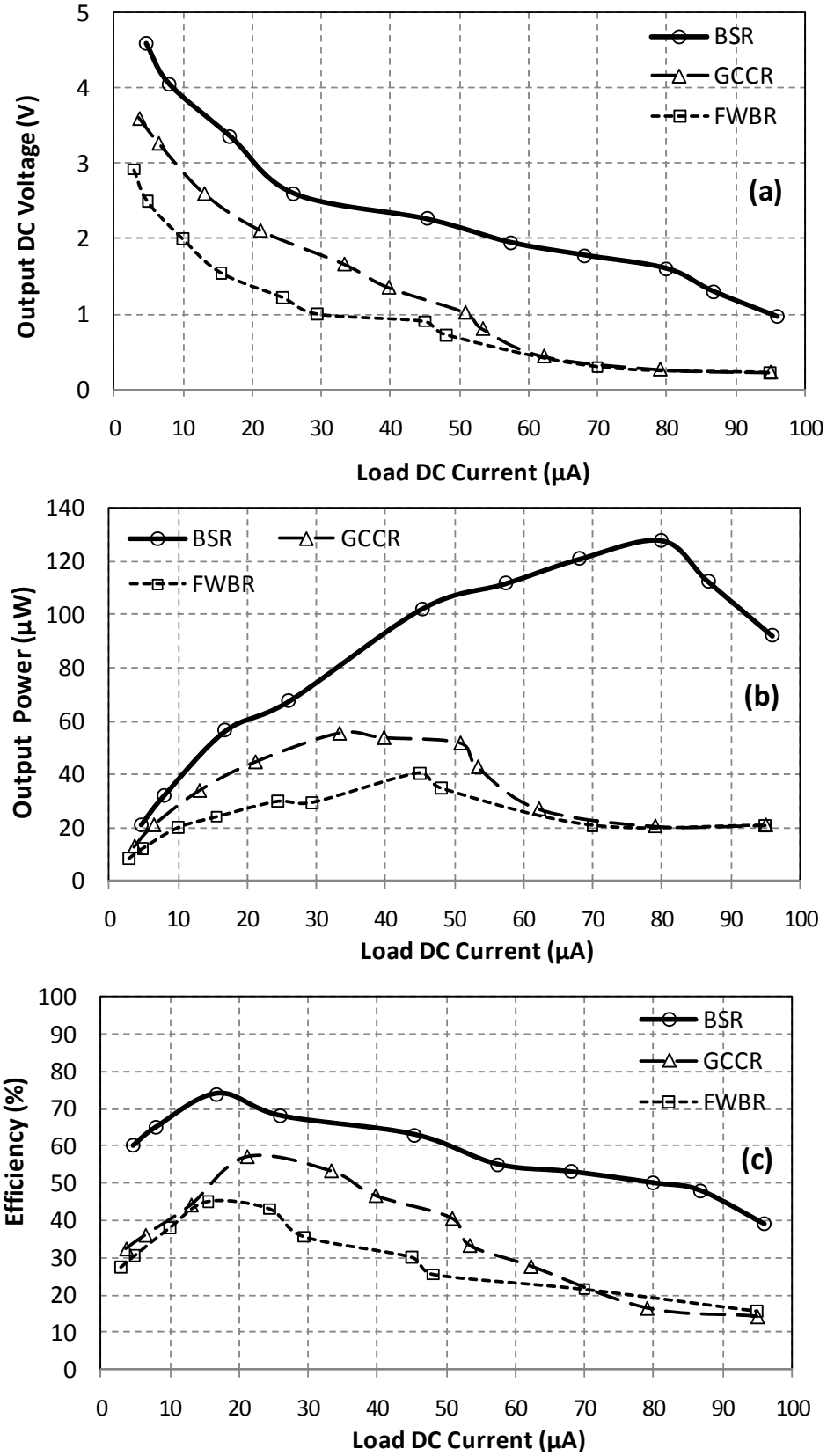


Figure 5.19: (a) The output voltage, (b) the output power, and (c) the power conversion efficiency of three implemented rectifiers versus the output load current at excitation frequency of 2 Hz.

Table 5.4: The summary of system specifications.

Operation Frequency	2 Hz
Magnet Dimension	15 mm (diameter)×2.5 mm(height) × 5
Saturation Magnetization	1.2 T
Cantilever Dimensions	15 mm × 15 mm
Cantilever Resonance Frequency	100 Hz
Number of Coil Turns	1000
Coil Resistance	47 Ω
The System Volume	21 cm^3 (70 × 20 × 15)
Max. Output Power	128 μW
Max. Power Density	6.1 $\mu W/cm^3$

5.3.3 The Operation of a Temperature Sensor Network Utilizing the Energy Harvesting System Working at 2 Hz

The proposed system is combined with a commercially available temperature sensor [25] to demonstrate its feasibility with a real application. The sensors are tested in a temperature controlled oven which is controlled by LakeShore Croyotronics® 330 cryogenic temperature controller. Temperature and output voltage is read by Agilent VEE® with Lakeshore Cryotronics® and Agilent® 34401 Multimeter via GPIB connection.

Figure 5.20 shows the performance results of the temperature sensor characterization. Two sets of sensors are tested such that one set is supplied using a regular DC supply and the other set is supplied by using the proposed energy harvesting system, operating with 2 Hz, 72 mg vibrations. According to Figure 5.19, the energy harvesting system utilizing BSR as the interface electronics is able to deliver 3 V DC voltage at 20 μA load current. Figure 5.20 (a) shows the comparison of the output of two temperature sensors, one operated with a DC supply, and the

other one operated by using the energy harvester. Figure 5.20 (b) shows the difference of the output voltages of temperature sensor sets according to:

$$\text{Voltage Difference}[\%] = \frac{V_{out}[using\ power\ supply] - V_{out}[using\ energy\ harvester]}{V_{out}[using\ power\ supply]} \times 100 \quad (5.5)$$

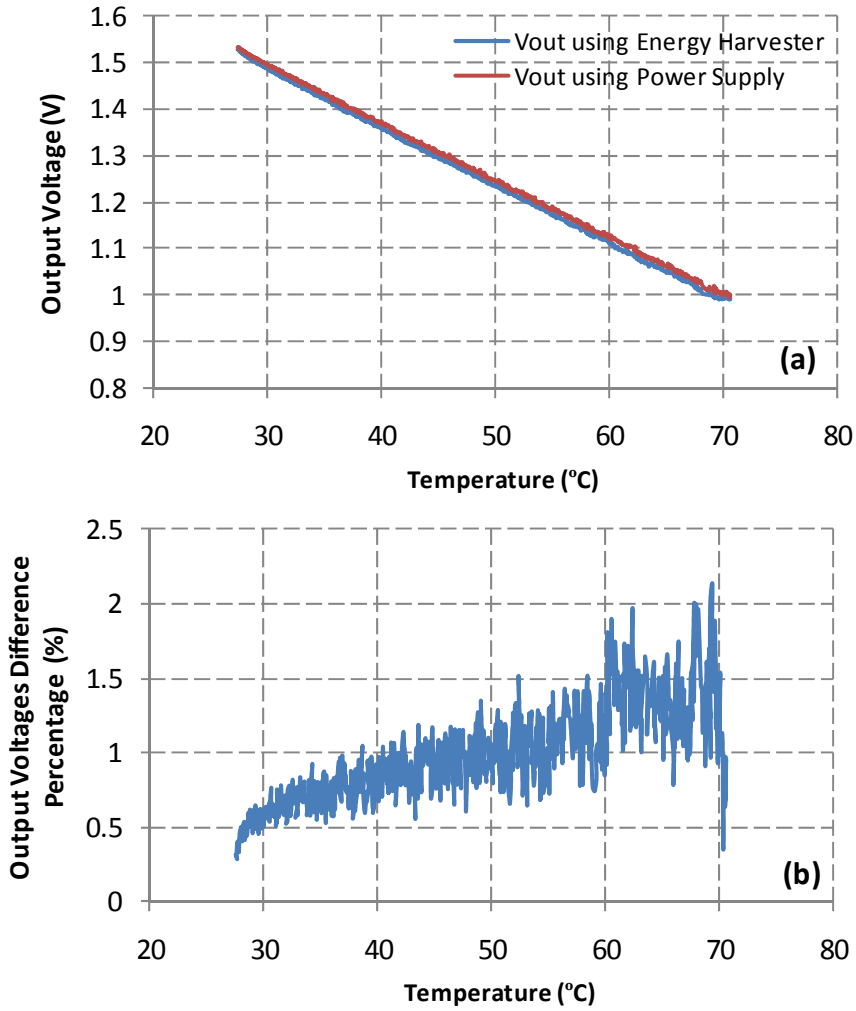


Figure 5.20: (a) The results of the temperature sensor using both energy harvesting system operating at 2 Hz, 72 mg acceleration, and external power supply, (b) The difference percentage of the output voltage of temperature sensors driven by harvester and power supply.

The voltage difference of the temperature sensor outputs are less than 2% over the measurement range, which is within the specifications of the temperature sensor, showing that the energy harvester is able to supply a practical load.

5.4 The Compact Electromagnetic Energy Harvesting System Utilizing Passive Interface Electronics

In this section, a compact vibration-based EM energy harvesting system utilizing passive rectifier as interface electronics has been presented. The energy harvester module consists of an AA-battery sized cylinder tube with an external coil winding, a fixed magnet at the bottom of the tube, and a free magnet inside. The transducer is able to operate at low external vibration frequencies within a relatively high bandwidth. The generated AC voltage is converted to DC using an optimized gate cross coupled (GCC) rectifier circuit in order to decrease the effective threshold voltage of the utilized diodes, increasing the DC output power delivered to the load. The autonomous system, composed of an EM energy harvester module and a 0.35μm CMOS IC, delivers 11.6 μW power to a 41 μA load at an external vibration frequency of 12 Hz. The volume of the total system is 4.5 cm^3, and the overall system power density is 2.6 $\mu W/cm^3$.

5.4.1 The System Block Diagram

Figure 5.21 (a) presents the block diagram of the proposed energy harvesting system. The system consists of an energy harvester module, a power ASIC and an external storage capacitor. The kinetic energy resulting from the ambient vibrations is converted to electrical energy by using an in-house EM energy harvester where an induced voltage is generated across a coil due to the motion of a magnet with external vibrations. There is no peripheral requirement such as a start-up battery, step-up transformer, etc. for the IC in order to start or maintain its operation. Figure 5.21 (b) depicts the schematic of the utilized energy harvester module which consists of a cylinder tube with an external 1200-turn coil winding, a fixed magnet at the bottom of the tube, and a free magnet inside. The same poles of the magnets face each other to suspend the free magnet. The free magnet starts moving in presence of external vibrations.

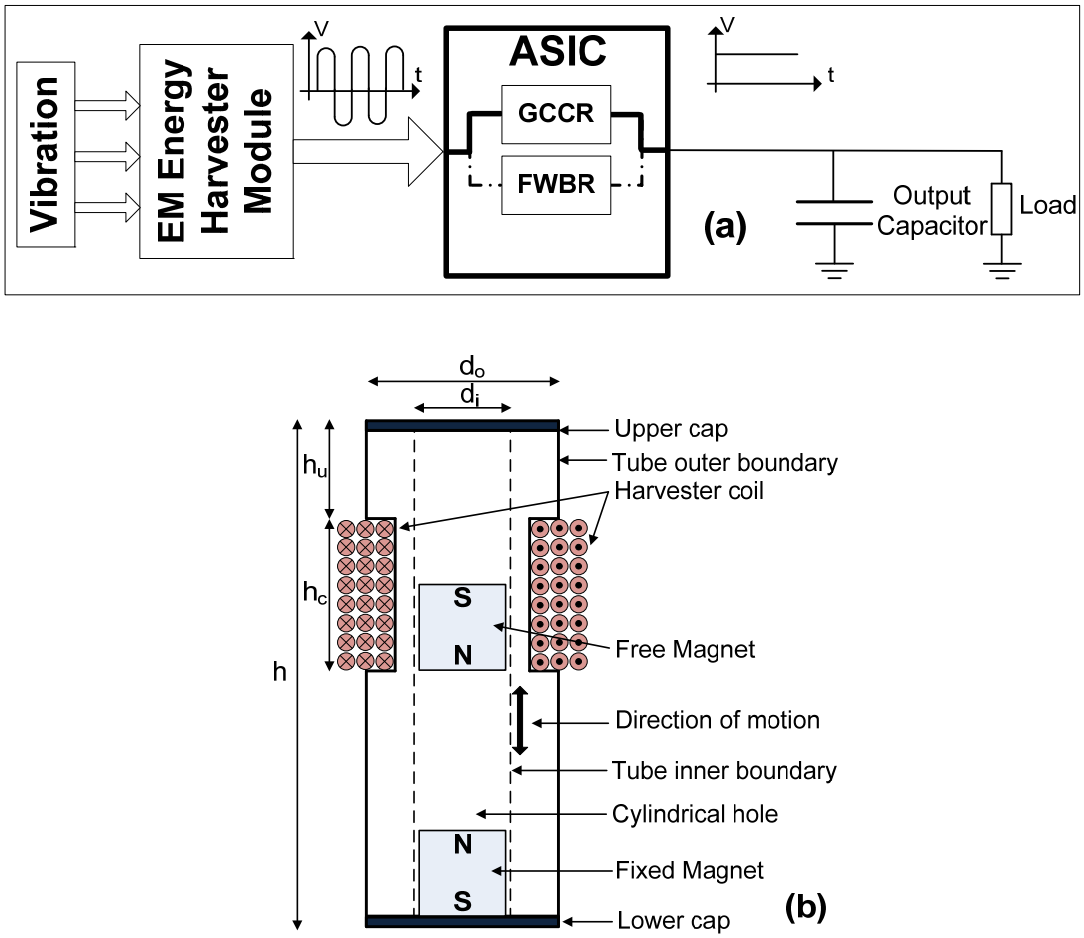


Figure 5.21: (a) The system block diagram, (b) the schematic of the energy harvester module.

5.4.2 The Experimental Results

The fabricated prototype of the proposed system is shown in Figure 5.22. The total volume of the prototype is 4.5 cm^3 including the energy harvester module, the interface electronics, and the external storage capacitor. A small-sized 10 µF SMD 0805 capacitor, mounted on the same substrate next to the IC, is used for storing the output DC voltage. The constructed system has been characterized for different excitation vibration frequencies and the generated *rms* voltage across the coil has been depicted in Figure 5.23. Also, the harvested AC waveforms at three different frequencies are depicted in Figure 5.24. The highest induced *rms* voltage (650 mV) is reached for an excitation frequency of 12 Hz and the operation bandwidth of the harvester is 2.5 Hz.

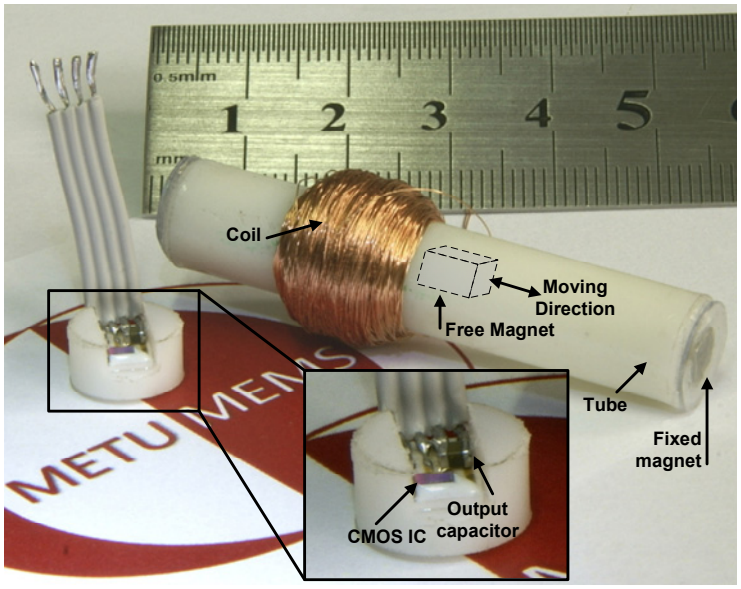


Figure 5.22: The fabricated compact energy harvesting system prototype.

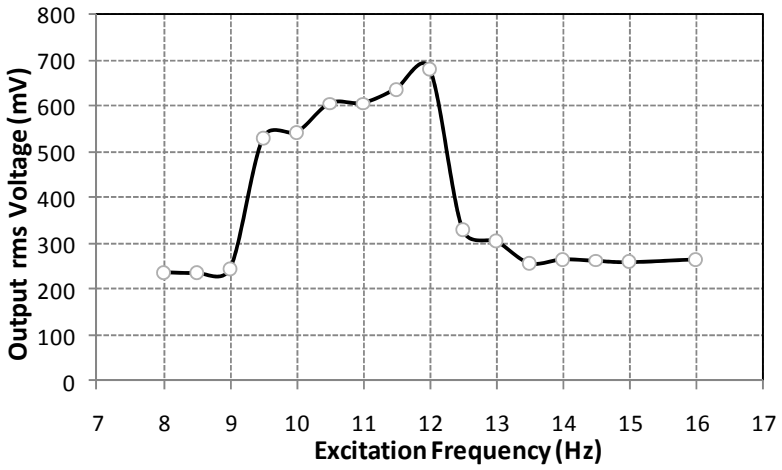


Figure 5.23: The output RMS voltage of the energy harvester for different excitation frequencies.

Figure 5.25 shows the comparison of the output voltage and output power of the implemented circuits against the load current which is swept within a 1 µA to 64 µA range. The maximum output power of 11.6 µW is achieved using the GCCR design however the maximum extracted power of FWBR is 2.35 µW which highlights the improved performance of threshold-voltage reduction effect of GCCR design in a standard CMOS technology.

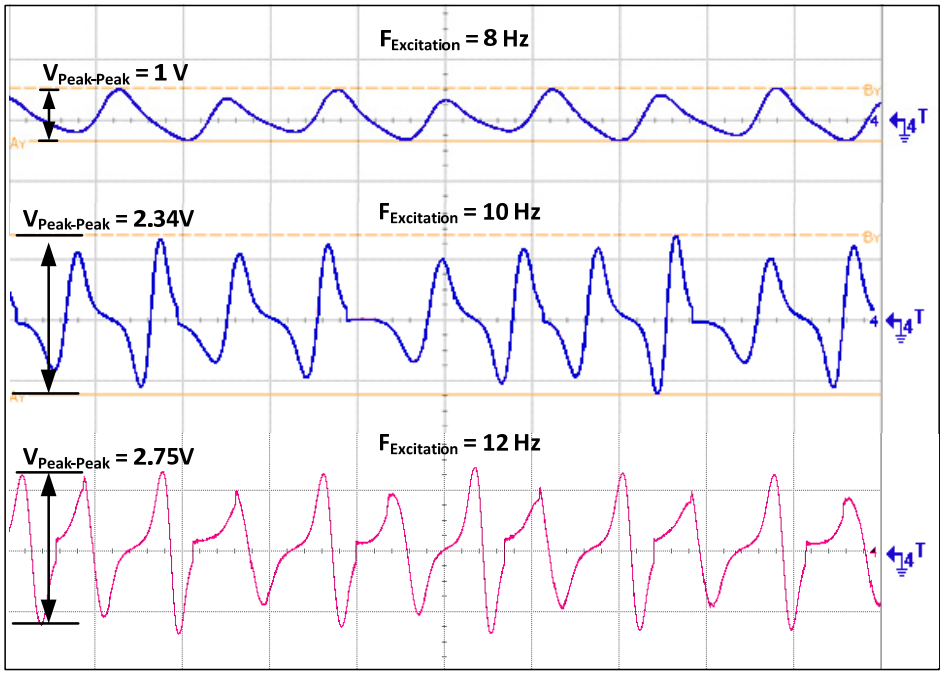


Figure 5.24: The harvested waveforms of the compact energy harvester at frequencies = 8, 10, and 12 Hz.

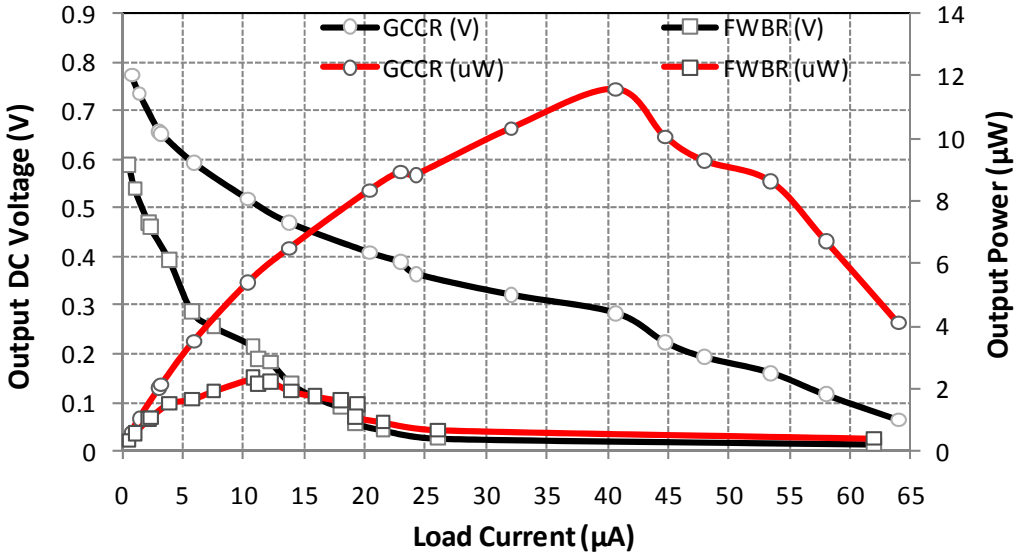


Figure 5.25: The output voltage and output power of two rectifiers versus load current which is swept from 1 to 64 µA.

Figure 5.26 illustrates the generated AC voltage of the energy harvester module and output DC voltage with a mechanical excitation profile of 12 Hz, 2.26g peak acceleration at output I_{Load}=41 µA where maximum output power is achieved. The induced peak-peak voltage is 2.75 V with 650 mV *rms* and converted output DC

voltage is 285 mV with 50 mV ripple (for R_L=7 kΩ). The system specifications are summarized in Table 5.5. The results of this work have been presented in Eurosensors 2011 conference [60].

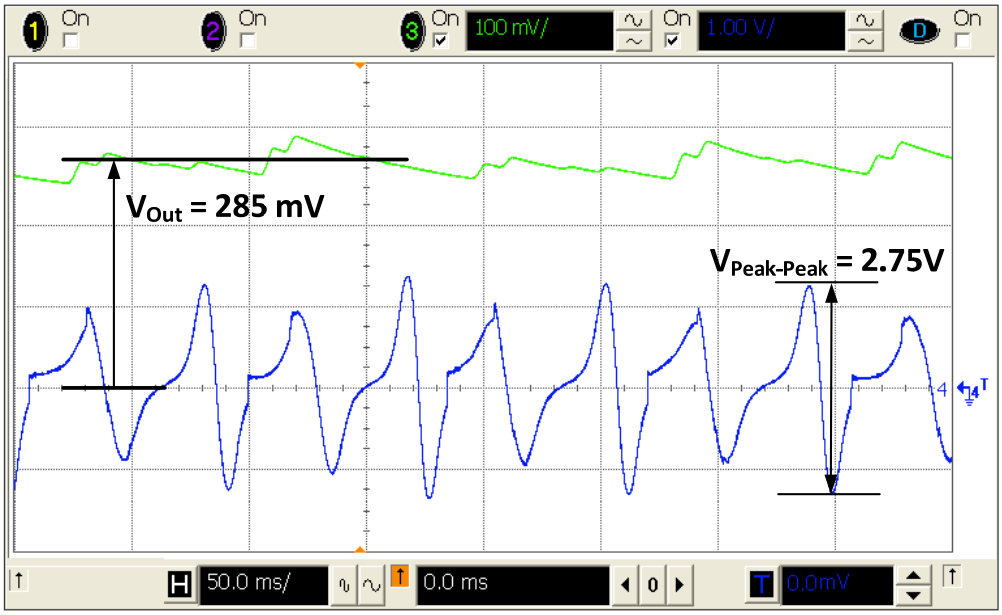


Figure 5.26: The output of the energy harvester module (blue) and converted DC voltage (green) at I_{Load}=41 µA.

Table 5.5: The compact energy harvesting system specifications.

Operation Frequency	12 Hz
Magnet Dimensions	4x4x4 mm^3
Number of coil turns	1200
Coil resistance	60 Ω
IC Technology	0.35 µm CMOS
The System Volume	4.5 cm^3
Max. Output Power	11.6 µW
Max. Power Density	2.6 µW/cm^3

5.5 The Fully Self-Powered Energy Harvesting System with Highly Efficient Active Dual Rail Output

In previous section, a compact EM energy harvesting system is presented which uses a passive interface electronics. However, as discussed in section 3.2, the conversion efficiency of passive rectifiers is low due to the voltage drop across the diode-based blocks. In the other hand, active rectifiers can provide much higher conversion efficiencies as they can be optimized to have very low voltage drop and therefore very high conversion efficiency. Their main obstacle is that they need an extra power supply for powering the active blocks.

In this section, a fully *self-powered* electromagnetic energy harvesting system utilizing a double coil transducer and a highly efficient dual rail active rectifier (as described in section 3.4) is presented. The proposed compact EM energy harvesting system has a larger volume than the system presented in previous section; however, it attains high power generation density when subjected to low frequency vibrations. A dedicated coil provides the required DC power to drive the active rectifier without the need for any battery. The +/- DC voltage pair for the active rectifier is generated through a network of ultra-low threshold voltage diodes and chip capacitors. The complete harvesting system is implemented as a System-on-Package (SoP) with a size of a C-Type battery, and delivers a smooth dual rail DC voltage which can directly be utilized by common sensor networks.

5.5.1 The Proposed Energy Harvesting System

Figure 5.27 presents the block diagram of the designed energy harvesting system. The system consists of an energy harvester module, a set of surface-mounted discrete diodes and capacitors, a custom power ASIC, and two external output storage capacitors. The kinetic energy resulting from the ambient vibrations is converted to electrical energy through a low cost and simple EM energy harvester, where an induced voltage is generated across the terminals of two separated coils (Coil 1 & Coil 2). The harvested AC signal on Coil 2 is fed to the bias generator network of rectification and step-up circuits that is built from ultra low threshold-voltage diodes and small sized capacitors. The network converts and steps up the AC signal into two DC voltage supplies, V_{DD} and V_{SS}. The produced double supply voltage is used

to provide DC power for the ASIC active rectifier, which converts the main AC signal on Coil 1 to dual rail DC, and stores it on two external output capacitors, C_{out+} and C_{out-}. The interface electronics is packed on a compact circular PCB and placed below the energy harvester module.

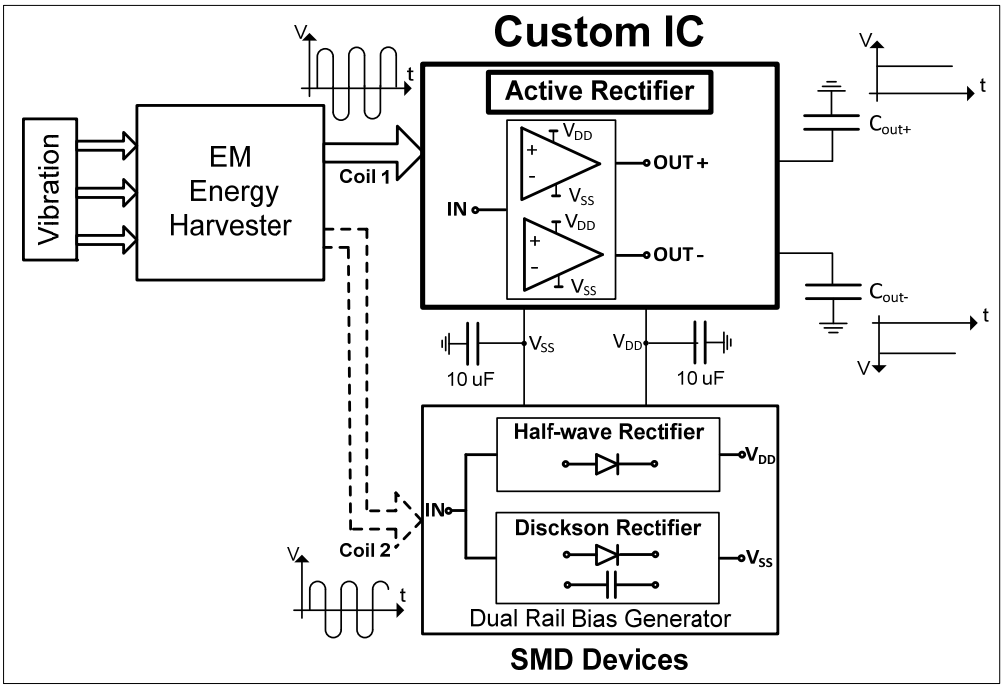


Figure 5.27: The block diagram of the proposed energy harvesting system utilizing active dual-rail output.

5.5.2 The Utilized Energy Harvester Module

The utilized energy harvester module is a simple and low cost EM energy harvester structure [23-24], which is adopted as the power source for the system (Figure 5.28). The package structure is similar to the module in section 5.4 and is a cylinder tube with a cylindrical hole inside it and two caps at bottom and top ends. A magnet is fixed on the bottom cap, and a free magnet is placed inside the tube such that the same poles of the magnets face each other to suspend the free magnet. Two separate coils are wound around the designated cavities on the outer boundary of the tube with lengths h_{uc} and h_{dc}.

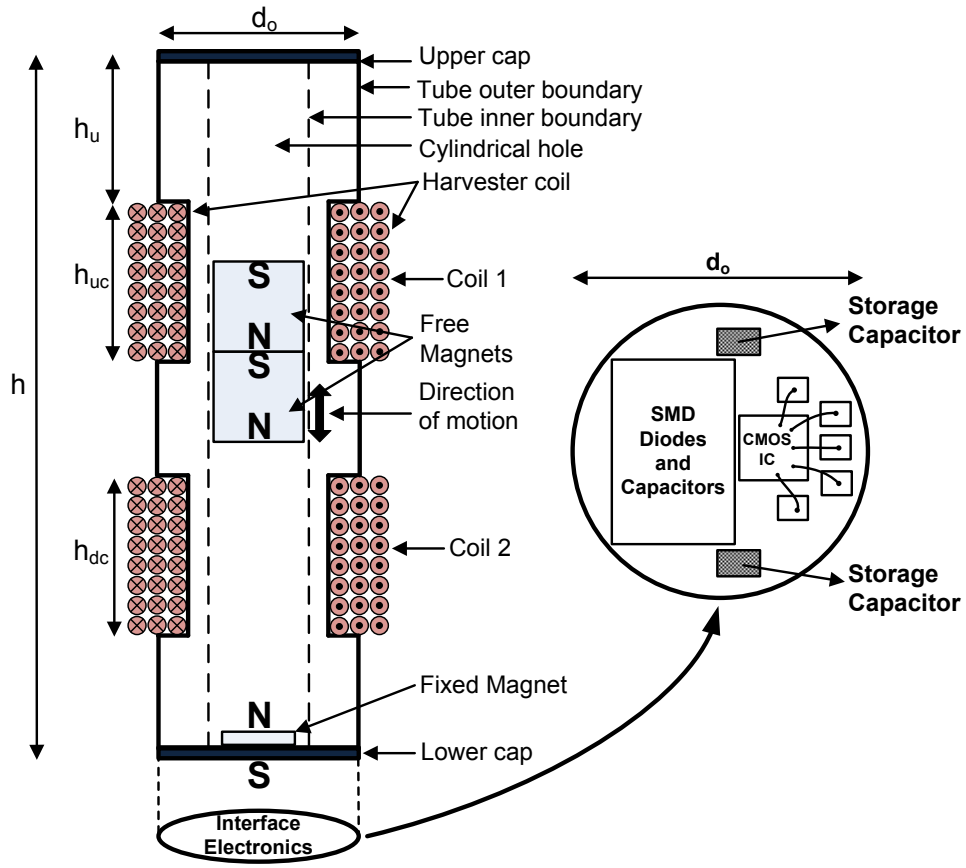


Figure 5.28: The detailed structure of the EM harvester module together with the schematic view of the overall system.

The free magnet starts moving and travels through the tube at presence of external vibrations, inducing AC voltages across the terminals of the two coils. There are several forces acting on the magnet during motion which are: the gravitational force $m\vec{g}$, input force to the system by the vibration $\vec{F}_{in}$, magnetic repulsion force resulting from the interaction with the fixed magnet $\vec{F}_{mag}$, electromagnetic damping force of the magnetic field of the coils $\vec{F}_{b,coil}$, air damping force $\vec{F}_{b,air}$, frictional force between the tube walls and the magnet edges $\vec{F}_{fric}$, and the crash-impact force $\vec{F}_{crash}$ which exists during the momentum change when the magnet touches to the upper cap [23]. So, the net force on the magnet can be formulated as:

$$\vec{F}_{net} = m\vec{g} + \vec{F}_{in} + \vec{F}_{mag} + \vec{F}_{b,coil} + \vec{F}_{b,air} + \vec{F}_{fric} + \vec{F}_{crash} = m\vec{a}(t) \quad (5.6)$$

where m is the mass of the magnet, $\vec{g}$ is the gravitational acceleration, and $\vec{a}(t)$ is the instantaneous acceleration of the magnet. The last three terms in (5.6) are dissipative force terms and these should be minimized for a more efficient energy conversion. Among these, $\vec{F}_{b,air}$ is minimized by introducing a hole on the upper cap, and $\vec{F}_{fric}$ is minimized by using rectangular magnets while the tube is cylindrical. The losses during the non-elastic collusion between the magnet and the upper cap could be reduced by using a proper non-magnetic spring; however this is not preferred for the sake of structural simplicity. Another option is to use a third magnet attached to the upper cap as in [24], however this sets the operation frequency of the system much above the desired range (< 10 Hz).

The operation frequency of the energy harvester is determined by the force interaction between the magnets (hence, the sizes of the magnets), the mass of the free magnet, and partly by the total length of the cylindrical tube for the cases where the magnet crashes the upper cap during operation. The desired operation frequency range of 6 to 10 Hz is reached by using a 5.3×5.3×0.5 mm^3 fixed magnet and a 7.5×7.5×15 mm^3 free magnet placed inside a 50 mm-long cylindrical tube having 4 mm and 10 mm inner and outer radius, respectively. The total size of the system is kept close to the size of a regular AA or C-Type battery.

The number of turns of the coils around the tube is determined regarding the overall performance and efficiency of the system. Different prototypes with different coil turns have been tested at different vibration conditions. A system with 600 turns for both coils has been characterized, operating at 6 Hz, rectifying low amplitude induced voltages; another system is also presented with a high power density, optimized for relatively high input voltage levels, with coil turns of 600 and 300 for Coil 1 and Coil 2, respectively. The details of these are discussed in Section 5.5.5.

5.5.3 The Dual-Rail Interface Electronics

The core of the interface electronics is the active rectifier which has been previously described in 3.4. A bias generator block comprising of high performance and very small sized discrete components is used to power the active blocks using Coil 2 (Figure 5.29).

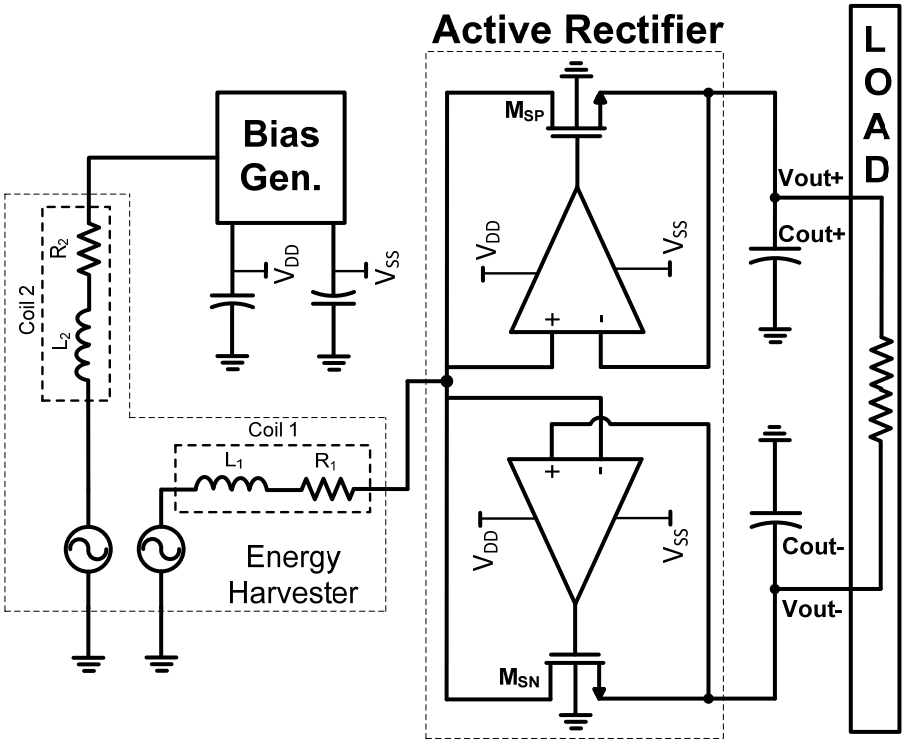


Figure 5.29: The schematic of the interface electronics.

Figure 5.30 shows the schematic of the bias generator block that generates a dual rail DC voltage (V_{DD} and V_{SS}) from Coil 2 to power up the active rectifier. A two-stage Dickson charge pump [25] is used to generate VDD (Section 2.2.2), which rectifies and steps up the AC voltage on Coil 2. The low threshold-voltage diodes are needed to increase the output DC voltage and the power conversion efficiency. Since they are not available in the utilized CMOS process, this block had to be built with high performance and small sized discrete components. Schottky diodes are good candidates to built up this block as they can provide very low threshold-voltages (<100 mV). However, they have relatively high reverse current values (> 1 μA), limiting the efficiency of the circuit. Several types of Schottky diodes have been

tested considering both of these factors, and ultra-low threshold voltage chip diode, PMEG2005EL from NXP Semiconductors [26] has been selected to be used in this block. In order to generate V_{SS}, a half-wave rectifier circuit using the same diodes and capacitors are used for powering the negative supply of the active rectifier (Fig. 4). By using this circuit, a smaller $|V_{SS}|$ is generated compared to V_{DD}, which enables biasing the active block with a lower power consumption, increasing the system efficiency. The capacitors, C_1, C_2, and C_3 are selected to be 1 µF based on the targeted frequency range (< 10Hz), and the output storage capacitors, C_{temp+} and C_{temp-} are selected as 10 µF.

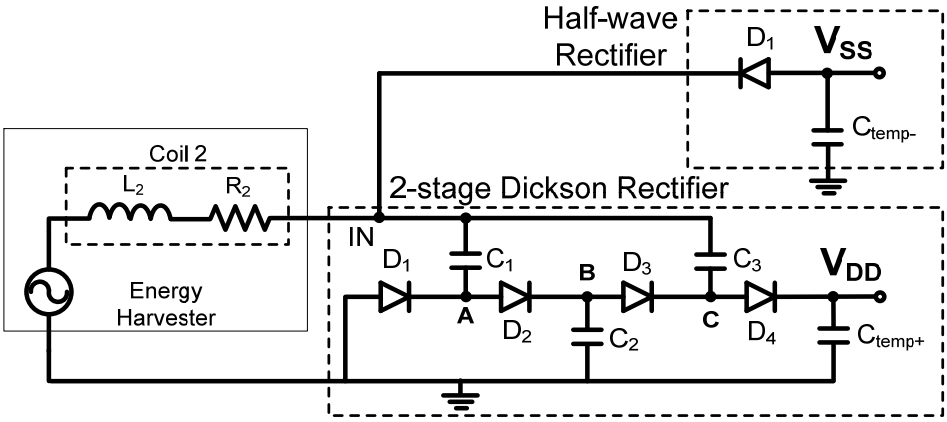


Figure 5.30: The schematic of the dual rail bias generator.

5.5.4 The System Implementation and Experimental Results

Figure 5.31 (a) depicts the constructed prototype of the proposed energy harvesting system. The electromagnetic energy harvester module consists of a cylindrical tube with two caps on top and bottom, one flat magnet which is placed at the backside of the PCB which also serves as the bottom cap, two cascaded free magnets inside the tube and two coils with 300 and 600 turns which are wound around the tube (Figure 5.31 (b)). The interface electronics, including the custom ASIC and dual rail bias generator components, has been implemented on a circular printed circuit board (PCB), (Figure 5.31 (c)) and is attached under the harvester module. All four storage capacitors (10 µF) are surface-mounted on the PCB substrate as well. The size comparison of the prototype with AA and C-Type batteries is presented in Figure 5.31 (d). Table 5.6 presents the specifications of the utilized interface electronics.

Table 5.6: The Specifications of the active dual-rail interface electronics.

IC Technology	XFAB 0.35μm 2P4M CMOS
Chip Area	0.0572 mm^2 (active chip area) 0.3 mm^2 (with bond pads)
CMOS $\|V_{TP}\|/V_{TN}$	0.73V/0.55V
Schottky Diodes	Philips PMEG2005EL
Diode Area	0.6 mm^2
$V_{\text{Forward Bias, Diode}}$	125 mV
Diode Reverse Current	< 1 μA
Chip Capacitors	AVX-CER0805
Capacitor Dimensions	2 mm ×1.25 mm ×0.5 mm
Total PCB Area	3.14 cm^2

Figure 5.31: Photographs of the proposed energy harvesting system. (a) fixed magnet attached to the backside of the PCB, (b) the free magnet placed to the cylindrical tube, (c) photograph of the PCB indicating the utilized diodes, capacitors, and the CMOS IC, (d) completely assembled system, and (e) size comparison with AA and C-type batteries.

The fabricated energy harvesting system has been tested using a shaker setup similar to Figure 5.11, which is composed of the energy harvesting system prototype, a shaker table, a control unit, an amplifier, an accelerometer, and an interface computer (Figure 5.32).

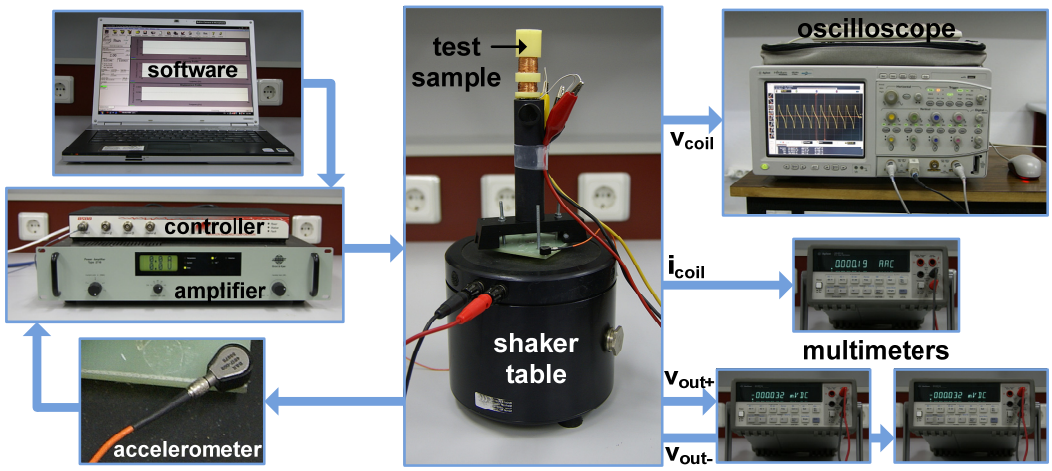


Figure 5.32: The test setup and photograph of the components and measurement devices.

The constructed energy harvester system has been tested at different external vibration conditions and the performance parameters have been recorded for each mechanical excitation. The test results of two different prototypes are presented in this section, with different number of coil turns. The first prototype with 600 turns each for Coil 1 and Coil 2, is designed for high efficiency operation at low vibration excitation levels, leading to low generated power values. The second prototype is optimized for operation at higher generated power levels, and has 600 and 300 turns for Coil 1 and Coil 2.

The prototype with 600 turns for both Coil 1 and Coil 2 has been tested where the system operates at 6 Hz, inducing 500 mV peak voltage across Coil 1. Figure 5.33 (a) and (b) show the generated AC voltage, on Coil 1 and Coil 2, respectively. The peak-to-peak displacement amplitude is 7 mm, corresponding to a peak acceleration level of 0.5g.

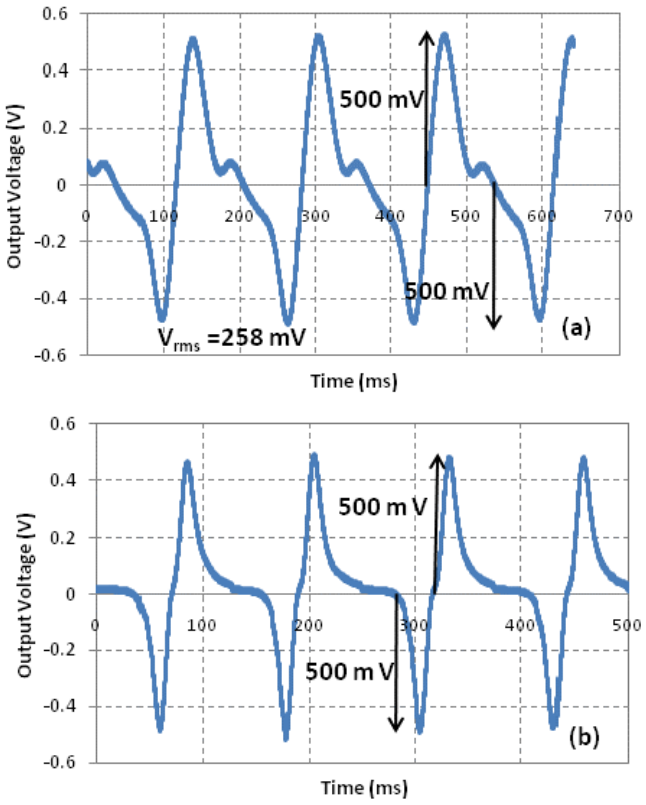


Figure 5.33: Generated output voltage of the energy harvester across (a) Coil 1, and (b) Coil 2. Both coil turns are 600.

Figure 5.34 shows the generated peak-to-peak voltage on both Coil 1 and Coil 2 for different vibration frequencies. The highest induced peak-to-peak voltage for both coils has been reached for an excitation frequency of 7 Hz at 7 mm peak-to-peak displacement. However, the results at 6 Hz, 7mm peak-to-peak excitation has been presented in order to show the performance of the interface electronics at low induced voltage levels.

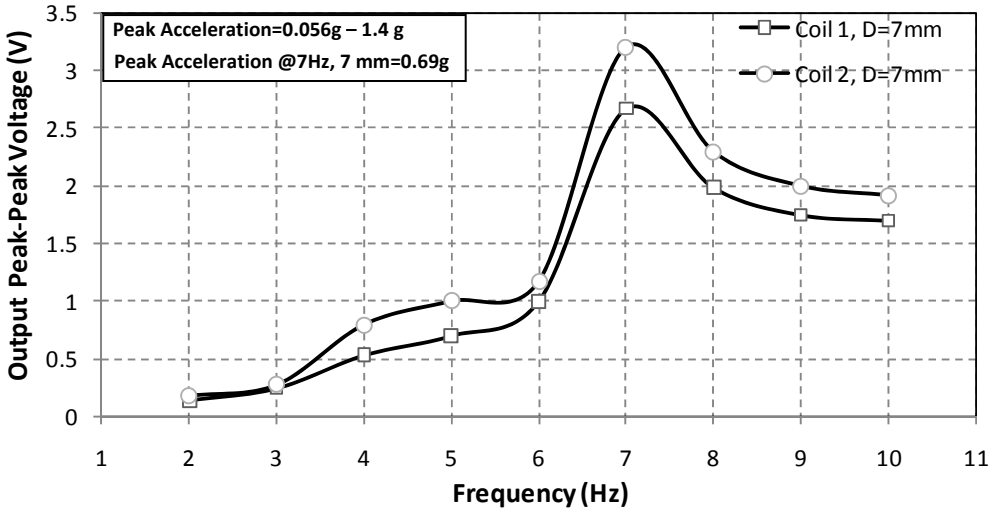


Figure 5.34: The output peak-to-peak voltage of the energy harvester for different excitation frequencies with a displacement of 7 mm.

Figure 5.35 presents the performance characterization results of the interface electronics for the specified vibration conditions in terms of the output voltage, output power, and the circuit conversion efficiency for several output load currents. For this characterization, the output DC load current is measured as:

$$I_{out} = \frac{V_{out+} - V_{out-}}{R_{Load}} \tag{5.7}$$

where V_{out+} and V_{out-} are the positive and negative output DC voltages, which are stored on the output capacitors, and R_{Load} is the resistive load which is placed between dual rail outputs. Figure 5.35 (a) depicts the converted output DC voltages versus the load current. The input power is measured as the *rms* AC power and the total output power is the summation of the stored DC power values on the storage capacitors. These are formulated as follows:

$$P_{input} = I_{Coil1[rms]} \times V_{Coil1[rms]} \tag{5.8}$$

$$P_{out} = I_{out} \times (V_{out+} - V_{out-}) \tag{5.9}$$

where P_{out} is the total output power of both positive and negative outputs for the same I_{out} value.

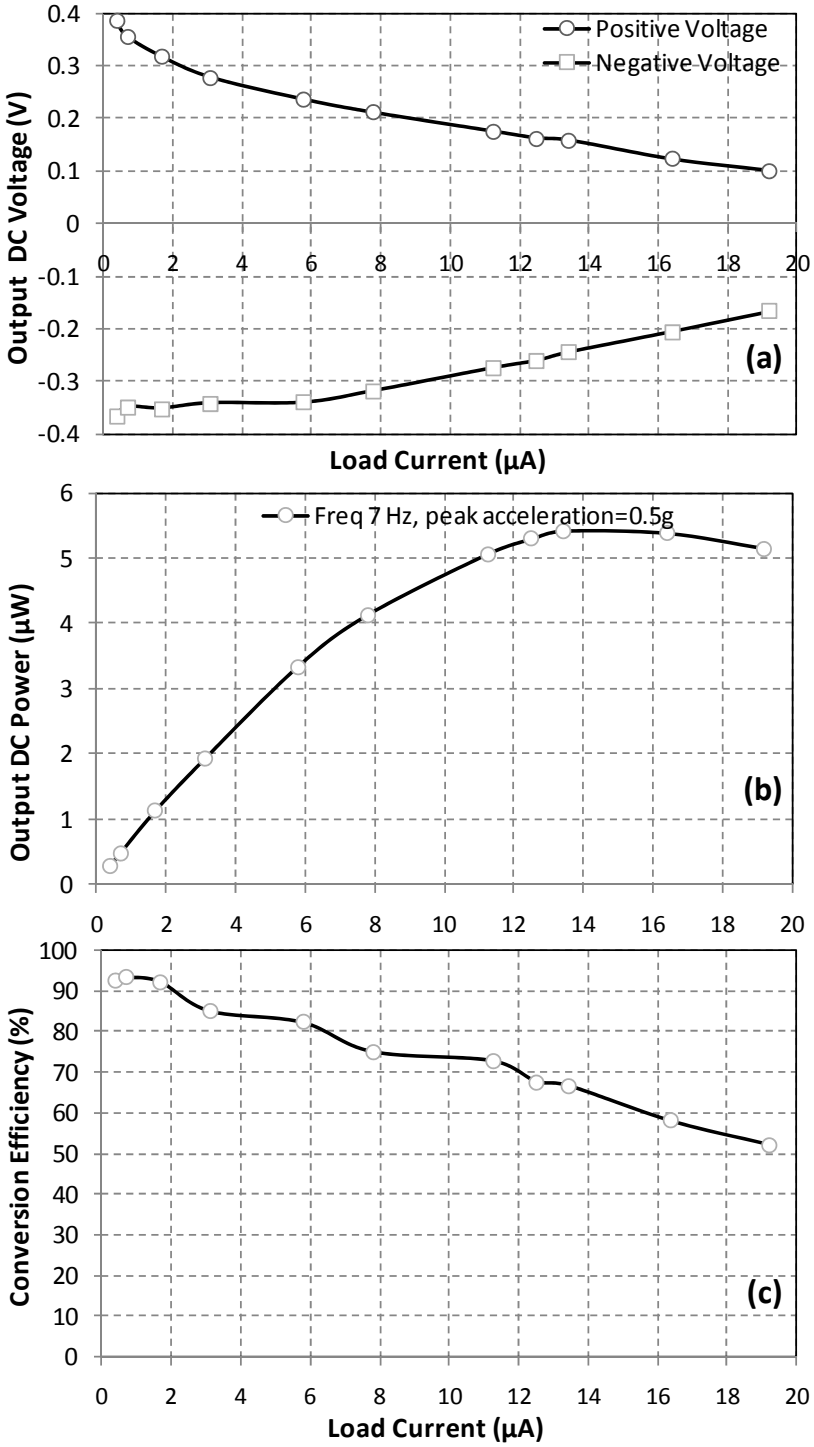


Figure 5.35: (a) The converted positive and negative output voltages, (b) the output power, and (c) the AC/DC power conversion efficiency of the main rectifier, versus I_{out}. The vibration frequency is 6 Hz and the peak-to-peak displacements 7 mm, corresponding to a peak acceleration of 0.5g.

The conversion efficiency of the active rectifier is the ratio of the total DC output power to the AC input power across Coil 1,

$$Conversion\,Efficiency \quad [\%] = \frac{P_{out}}{P_{input}} \times 100 \tag{5.10}$$

Figure 5.35 (b) and (c) depict the total DC output power and AC/DC power conversion efficiency of the rectifier versus the load current. The results prove that the designed interface electronics is able to convert the low voltage (500 mV_{peak}) and low power (< 5 μW) AC signals to DC. The efficiency of the interface electronics remains over 80% for load currents below 6 μA. The generated DC power is maximized at 5.5 μW over a 13.5 μA (17 kΩ) load with 68 % conversion efficiency, while providing a 0.42 V dual rail DC supply with V_{out+} and V_{out-} are realized as 0.162 V and -0.261 V, respectively.

In order to demonstrate the high input voltage case, arising from a higher amplitude and higher frequency vibration, the second prototype with coil turns of 600 and 300 for Coil 1 and Coil 2, respectively, has been characterized. The maximum induced voltage for this system is reached for 8 Hz, 8 mm peak-to-peak excitation, corresponding to 1.03g peak acceleration. Figure 5.36 (a) and (b) show the generated AC voltage for this case on Coil 1 and Coil 2, respectively.

Figure 5.36 shows the generated peak-to-peak voltage of this prototype for different vibration frequencies while the displacement is set to 8 mm. A relatively wideband operation is observed for frequencies between 6 Hz and 10 Hz. The frequencies higher than 10 Hz could not be tested due to the limitations of the shaker table.

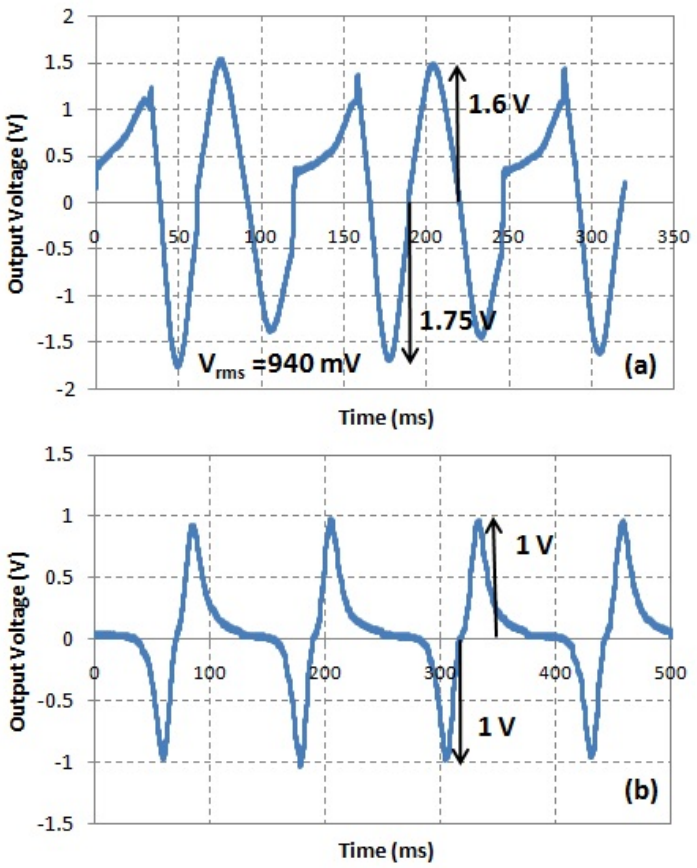


Figure 5.36: The generated output voltage of the energy harvester across (a) Coil 1, and (b) Coil 2. The coil turns are 600 and 300, respectively.

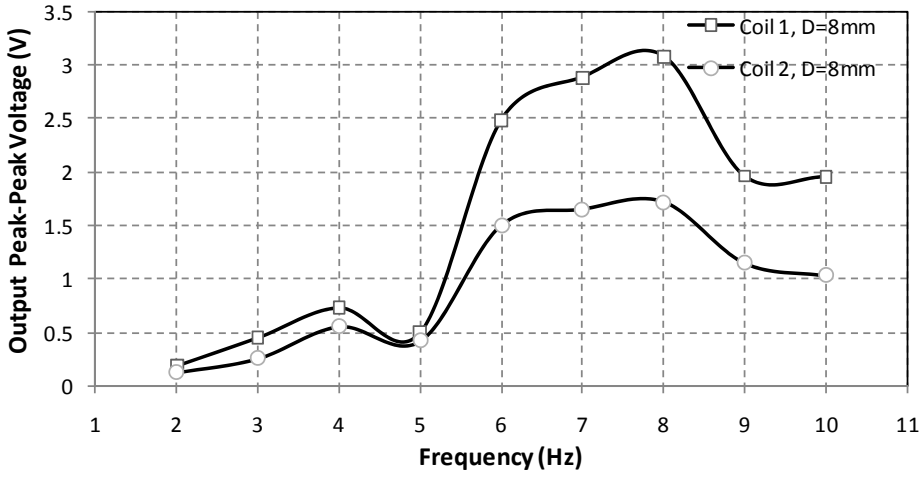


Figure 5.37: The output peak-to-peak voltage of the energy harvester for different excitation frequencies with a displacement of 8 mm.

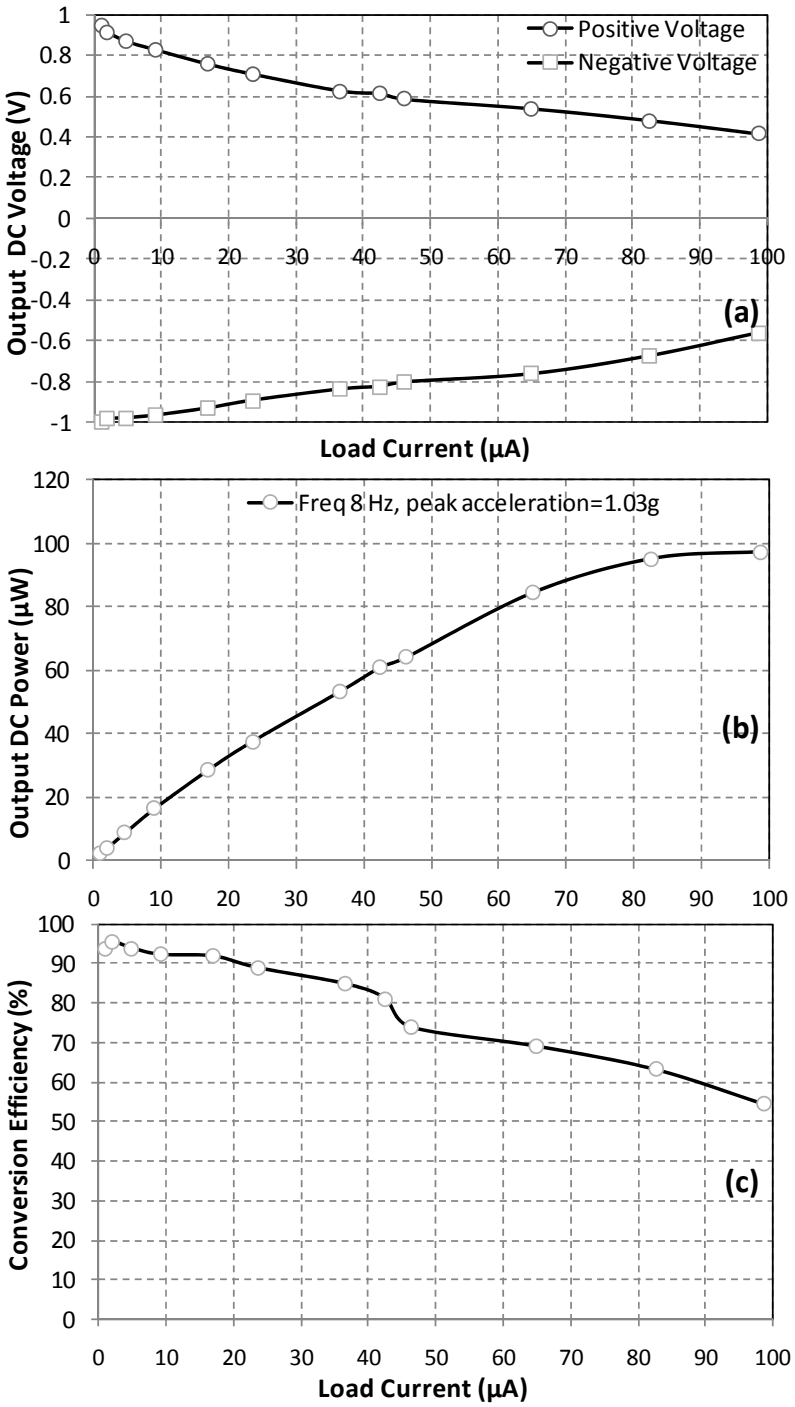


Figure 5.38: (a) The converted positive and negative output voltages, (b) the output power, and (c) the AC/DC power conversion efficiency of the main rectifier, versus I_{out}. The vibration frequency is 8 Hz and the peak-to-peak displacements 8 mm, corresponding to a peak acceleration of 1.03g.

Figure 5.38 presents the performance characterization results of the interface electronics for the specified vibration conditions and coil turns for a wide range of

output load currents. The designed circuit is able to generate 54 μW DC power over a 37 μA (40 kΩ) load with 85 % conversion efficiency, while providing a 1.46 V dual rail DC supply with V_{out+} and V_{out-} are realized as 0.62 V and -0.84 V, respectively.

It is seen from Figure 5.38 (a) that the converted output DC voltage decreases in amplitude almost linearly with increasing load current (decreasing load resistance) implying the higher discharge rate of the output capacitors at higher load current values. However, the relatively low slope indicates the efficient conversion of the AC voltage to DC. The conversion efficiency is almost constant (> 90%) for a load current range of 1 to 20 μA. The efficiency tends to decrease slightly for higher load current values since the mechanically generated input power starts to limit the charging rate of the output capacitor. In other words, the discharge rate of the output capacitors with a resistive load in parallel is higher than its charging rate; leading to the conversion efficiency drop of the active rectifier. However, the efficiency remains above 80% up to 42 μA of load current.

Figure 5.39 (a) and (b) show the generated AC input power on Coil 1, and the conversion efficiency of the active rectifier versus different resistive loads, respectively. It is seen from Figure 5.39 (a) that the input AC power generated over the coil is dependent on the output load resistance of the system. As the output load increases, the generated AC power decreases. This can be explained as follows: According to (5.8), the generated input power is the multiplication of the induced voltage across the coil by the coil current. Since the coil has a very low impedance compared to the effective input impedance of the rectifier, it could be said that the induced voltage across the coil depends only on the mechanical input characteristics, independent of the electrical network which is connected to the coil. Furthermore, in a similar way, the current of the coil depends on the connected electrical network and output load of the AC/DC converter. By decreasing the output load impedance connected in parallel with the output capacitor (increasing the load current), higher current is drawn from the coil, and the generated AC input power from the energy harvester is increased.

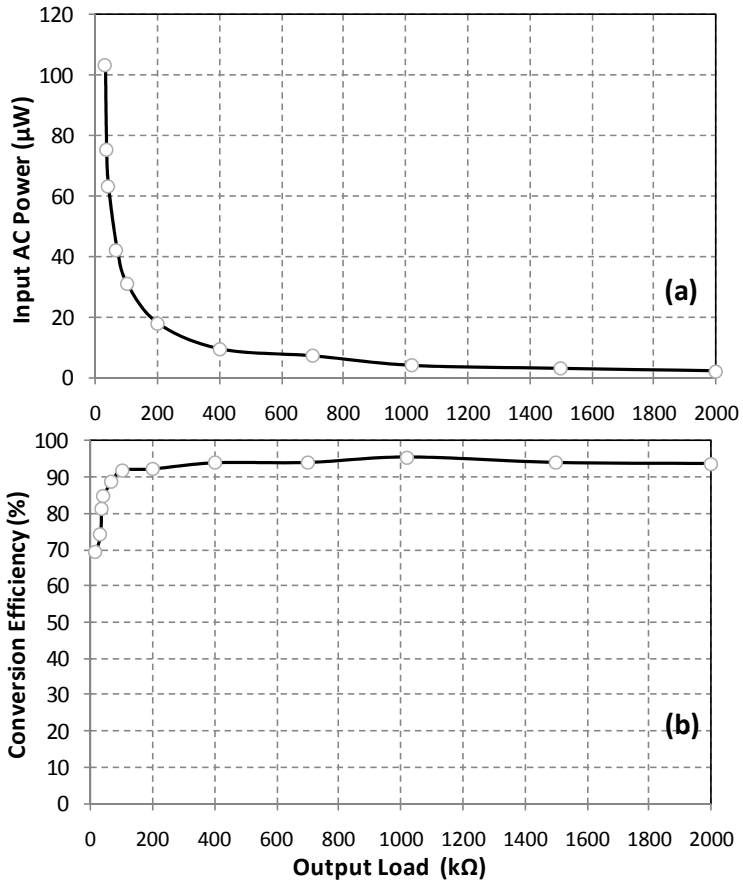


Figure 5.39: (a) The generated AC input power, and (b) the conversion efficiency of the AC/DC converter versus load values.

5.5.5 The System Efficiency

A portion of the generated power is consumed by the operation of the active rectifier block. Hence, while calculating the efficiency of the total system, the consumption of the active rectifier should also be considered. The system efficiency is defined as:

$$System \quad Efficiency \quad [\%] = \frac{P_{output} - P_{Active\ \ Consumption}}{P_{input}} \times 100 \tag{5.11}$$

According to equation (5.11), maximizing the *system efficiency* requires the minimization of $P_{Active\ Consumption}$, the amount of power that is consumed by the active rectifier during AC/DC conversion. The active rectifier is designed to operate for a wide range of supply voltages (V_{DD} and V_{SS}); however its power consumption- is variable for different supply values, affecting the total system efficiency. Since the

active block needs a minimum DC voltage supply to operate, the total system needs a minimum vibration input, hence minimum induced voltage in order to start power conversion. By increasing the number of coil turns, it is possible to induce higher voltages for the same vibration condition. Similarly, it is also possible to operate the system at a lower mechanical vibration levels. However, the power consumption of the active circuit becomes higher at higher induced AC voltages, which decreases the total system efficiency. Therefore, a compromise must be made between the coil turns and amount of generated voltage to maximize the total system efficiency. In order to investigate this phenomenon, several prototypes with different coil turns have been tested under different input vibration conditions. Table 5.7 presents the prototype coil turns, vibration conditions, and the corresponding performance results. The maximum achieved *system efficiency* is 81% for a 37 μA load current corresponding to 40 kΩ load resistance (54 μW), and 600 and 300 turns for Coil 1 and Coil 2, respectively while the input excitation frequency is 8 Hz with a peak acceleration of 1.03g. The volume of the total system including the mechanical transducer and interface electronics is 16 cm^3 and the corresponding maximum power density is 6.06 μWcm^{-3} for the above configuration.

It should also be noted that the case A in Table 5.7 (as in Figure 5.35), presents a low vibration level condition for the proposed system, for which the interface electronics is mainly designed. A system efficiency of 80% is also reached for this case, proving the operation of the electronics for low input AC voltage conditions. In addition to this, the consumption of the rectifier is much lower than the other cases. On the other hand, since the input power is low, the generated power at this configuration also low, leading to a low output power and power density. If the input vibration is increased (cases B-D), the output power increases with the cost of a decrease in the system efficiency. In such cases, since the peak amplitude of the AC signal is higher, the rectifier has to be biased with higher V_{DD} and V_{SS}, resulting in an increase in its power consumption, and a decrease in the total system efficiency.

Table 5.7: The prototype coil turns, vibration conditions, and the corresponding performance results.

Case	*Coil1 / Coil2 #turns*	*Excitation Peak Acceleration (×g)/ Frequency (Hz)/ Peak to Peak Displacement (mm)*	*Generated V_{DD} (V)/ V_{SS} (-V)*	*Active Power Consumption (µW)*	*Max. Achievable Output Power (µW)*	*The maximum system efficiency @ I_{Load}, P_{out}*
A	600 / 600	**0.5/ 6 / 7**	**1.2/0.45**	**0.16**	**5.5**	**80% @ 5.75 µA, 3.5 µW**
B		0.57/ 6/ 8	1.5/0.75	1.7	11	73% @ 16.5 µA, 11.5 µW
C		0.69/ 7/ 7	2.8/1.4	30	89	52% @ 50.5 µA, 76 µW
D		1.03/ 8/ 8	3.2/1.5	47	125	46% @ 54 µA, 100 µW
E	600 / 300	0.69/ 7/ 7	1.95/0.83	4.6	72	72% @ 33 µA, 43 µW
F		**1.03/ 8/ 8**	**2/0.85**	**5.4**	**97**	**81% @ 37 µA, 54 µW**
G	300 / 300	1.03/ 8/ 8	2/0.85	5.4	19	62% @ 15 µA, 16 µW

Another point that should be discussed is the achieved system efficiency improvement by using the designed rectifier ASIC. This is done by comparing the efficiency values of the system utilizing the ASIC and the discrete dual rail rectifier constructed on the PCB. Naturally, the system is able to convert the generated AC voltage by using only the passive circuitry on the PCB without the active rectifier ASIC. For instance, the Dickson charge pump could be used to generate positive output voltage from Coil 1, and the half-wave rectifier could be used to generate negative output voltage from Coil 2. In this configuration, both coils are utilized to generate DC voltage s without the active ASIC. Figure 5.40 illustrates the obtained total output DC power and the conversion efficiency of the system by testing the described scenario. The maximum generated power is 34 μW at 41% conversion efficiency and the maximum conversion efficiency of 44% is achieved for a load current of 19 μA when compared to the 81% maximum efficiency of the proposed system at 37 μA, proving the improvement realized by introducing the ASIC to the system. Table 5.8 summarizes the comparison results of the interface circuitry with and without the active ASIC.

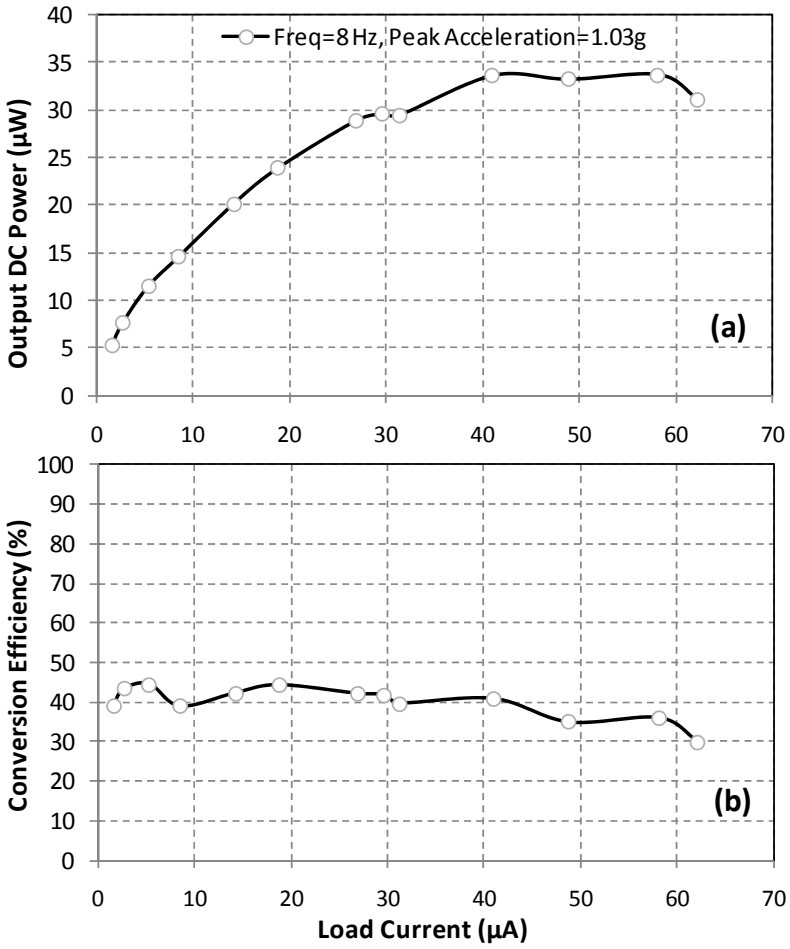


Figure 5.40: Test results of the rectifier composed of only discrete components, without utilizing the active ASIC. Coil 1 is connected to the Dickson charge pump to generate positive output and the half-wave rectifier is used to generate negative output voltage from Coil 2. The specifications of the system are summarized in Table 5.9.

Table 5.8: The comparison of performance results of the interface circuitry with and without ASIC.

Circuitry	**Max. Output Power (µW)**	**Max. Efficiency**	**Max. Load Current (µA)**
With ASIC	97	System eff. 81% Conversion eff. 95%	99
Without ASIC	34	System eff. 44%	62

Table 5.9: Summary of System Specifications.

Operation Frequency	6-10 Hz
Fixed Magnet Dimensions	5.3×5.3×0.5 mm^3
Free Magnet Dimensions	7.5×7.5×7.5 mm^3 ×2
Saturation Magnetization	1.2 T
Number of Coil Turns	300/600
Coil Resistance	300 #turn 27.5 Ω 600 #turn 55 Ω
Max. Efficiency	81 % (@ 37μW)
$V_{rail\text{-}to\text{-}rail}$ @ max. eff.	1.46 V (0.62 V& -0.84 V)
The System Volume	16 cm^3
Max. Output Power	97 μW
Max. Power Density	6.03 μWcm^{-3}

5.6 The Performance Comparison of the Realized Energy Harvesting Systems

In this study, different types of electromagnetic energy harvesting systems have been constructed based on the integration of an electromagnetic micro power generator and high performance interface electronics. Depending on the electrical specifications of the energy harvester module and the range of generated voltage and power, some specific interface circuitry is decided to be interfered, realizing the energy harvesting systems.

Table 5.10 shows the comparison of the realized electromagnetic energy harvesting systems and the state-of-the-art. The shaded parts of the table are the systems that have been realized during this study and are explained in this chapter. Although there are many efforts to improve the power density of electromagnetic energy harvesters, there are a few publications that integrate the EM generator and customized interface electronics, expressing the usable amount of power (DC power). There are many other EM energy harvester modules in the literature; however, most of them give the AC power values only and therefore aren't comparable with the complete systems in Table 5.10.

Table 5.10: Comparison of the proposed energy harvesting system with literature.

Ref.	Volume (cm^3)	Operation Frequency (Hz)	Max Output Power (µW)	Max System Efficiency (%)	Power Density (µW/cm^3)	Circuitry	Additional Requirements
5.1	-	5	35	35	-	Dickson rectifier	Low eff. discrete components
5.2	15	10	20.5	65	1.33	Passive BSR rectifier	Step-up transformer
5.3	**21**	**2**	**128**	**75**	**6.1**	**Passive BSR rectifier**	**Step-up transformer**
5.4	4.5	12	11.6	-	2.6	Passive GCC rectifier	-
5.5	16	8	97	81	6.03	Active AC/DC Conv., Dickson rectifier	SMD components on PCB
[31]	31.5	41	4 mW	-	126	Diode AC/DC, DC/DC PWM boost converter	Additional 3.3 V battery
[23]	68	2	57	-	1.32	Cockcroft-Walton multiplier	Low eff. discrete components
[32]	43	10	30-100	-	-	Cockcroft-Walton multiplier	Low eff. discrete components

Based on the measurements, the proposed system in 5.3, demonstrates a 6.1 $\mu W/cm^3$ power density at ambient vibration frequency of only 2 Hz. The system is suitable to directly be utilized by common sensor networks, as one example was shown in section 5.3.3.

5.7 Summary of the Chapter

In this chapter, the experimental results related with the integration of the implemented interface electronics and the electromagnetic micro power generators have been explained. In each of the sections, the results of one type of interface electronics which is incorporated with a specified electromagnetic energy harvester is given. Firstly, the block diagram of the proposed system including the operation principle of the overall system is discussed and then, the experimental results of the systems under different electromechanical conditions are given. Finally, a further discussion is given for each system describing the achievements and limitations of each realized energy harvesting system.

In the end of the chapter, the fabricated energy harvesting systems are compared with the state-of-the-art electromagnetic energy harvesting system, discussing the system design, system specification, and the overall system performance results. The proposed energy harvesting systems proved to show the highest performance compared with the reported systems.

CHAPTER 6

CONCLUSIONS AND FUTURE WORKS

In this thesis, highly efficient interface electronics for electromagnetic energy harvesters have been designed, and implemented. The aim of the interface electronics is to convert the low voltage and low power generated signals of the electromagnetic energy harvesters to a DC voltage to be usable by a real application. The implemented interface electronics are finally merged with the previously proposed mechanical transducers in METU MEMS center and complete energy harvesting systems have been developed.

Accomplishments and results of this thesis work are listed as following:

1. A comprehensive and detailed study has been made on the building blocks and their design considerations which are required for the realization of high efficiency interface electronics for vibration-based electromagnetic energy harvesters. A state-of-the-art literature review has also been made for all the blocks to characterize the available architectures and highlight the points that need improvement for each block.

2. New architectures are proposed for high efficiency rectifiers which are required to convert the low power generated voltages of the electromagnetic energy harvesters to DC without using any extra supply (battery). The performance comparison of these designs has also been made with previous designs to prove their improvement and to show the feasibility of highly efficient power transfer from low power energy sources.

3. The mechanical transducers based on the available theory for electromagnetic energy harvesters have been developed and incorporated with the implemented circuits in X-FAB 0.35 μm CMOS process to realize energy harvesting systems. During this study, five different prototypes have been fabricated and tested for a wide range of input excitations and are fully validated. Also, the operation of a commercial sensor as a potential application for these systems has been proven. The measured power densities out of the systems in this work are the highest reported in the literature. As an instance, a power density of 6.1 $\mu W/cm^3$ is reported for the system operating at an external vibration frequency of only 2 Hz which is a significant improvement in this area.

4. A complete energy harvesting IC including more active circuits such as charge-pump DC-DC converter, the on-chip ring oscillator, and an ultra low power voltage regulator block, has been designed in TSMC low threshold (LVT) CMOS technology The simulated power consumptions are among the lowest reported in the literature and the feasibility of providing such power has previously shown. Therefore, the proposed solution is suitable for next generation MEMS-based electromagnetic energy harvesters.

5. Part of the results of this work has been presented in conferences such as *TRANSDUCERS'11* and *EUROSENSORS XXV* and in *IEEE Sensors Journal*. Also, another journal paper has been recently submitted to the *Sensors and Actuators: A. Phys. Journal.*

Since this work is one of the first conducted researches on interface electronics design for electromagnetic energy harvesters, there is a high potential of further research. A comprehensive list of future works is listed below:

1. Due to the unavailability of MEMS-based electromagnetic energy harvesters, the implemented systems are macro power generators; they were not microfabricated. Currently, there is research going on developing MEMS-based power generators with considerable output power in METU MEMS center. The previously manufactured ASIC and the prospective ASIC could be combined with the MEMS-based energy harvesters to realize complete micro power generation systems.

2. The designed ASIC in TSMC 90 nm process is to be sent for fabrication. The fabricated IC's will be tested with the energy harvesters.

3. Design of a load as a real application to be added on chip next to interface IC to have the complete system fully integrated. This load is preferably a CMOS compatible sensor such as a temperature sensor.

4. The incorporation of the realized system with some RF MEMS-based device to be able to transmit the data wirelessly. Such system, could be a solution for biomedical implants or any other environment that is inaccessible and needs remote monitoring.

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