DESIGN AND FABRICATION OF A HIGH GAIN, BROADBAND MICROWAVE LIMITING AMPLIFIER MODULE

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submitted by **HASAN HÜSEYİN KILIÇ** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. İsmet Erkmen
Head of Department, **Electrical and Electronics Engineering** _____

Assoc. Prof. Dr. Şimşek Demir
Supervisor, **Electrical and Electronics Eng. Dept., METU** _____

Examining Committee Members:

Prof. Dr. Canan Toker
Electrical and Electronics Engineering Dept., METU _____

Assoc. Prof. Dr. Şimşek Demir
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Sencer Koç
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Nevzat Yıldırım
Electrical and Electronics Engineering Dept., METU _____

Dr. Muhammet Mustafa Akkul
ASELSAN _____

Date: 14.09.2011

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last Name : Hasan Hüseyin KILIÇ

Signature :

ABSTRACT

DESIGN AND FABRICATION OF A HIGH GAIN, BROADBAND MICROWAVE LIMITING AMPLIFIER MODULE

Kılıç, Hasan Hüseyin
M. Sc., Department of Electrical and Electronics Engineering
Supervisor: Assoc. Prof. Dr. Şimşek Demir

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Microwave limiting amplifiers are the key components of Instantaneous Frequency Measurement (IFM) systems. Limiting amplifiers provide constant output power level in a wide input dynamic range and over a broad frequency band. Moreover, limiting amplifiers are high gain devices that are used to bring very low input power levels to a constant output power level. Besides, limiting amplifiers are required to provide minimum small signal gain ripple in order not to reduce the sensitivity of the IFM system over the operating frequency band.

In this thesis work, a high gain, medium power, 2-18 GHz limiting amplifier module is designed, simulated, fabricated and measured. First, a 3-stage cascaded amplifier with 27 dB small signal gain is designed and fabricated. The 3-stage amplifier is composed of a novel cascaded combination of negative feedback and distributed amplifiers that provides the minimum small signal gain ripple and satisfactory input

and output return losses inside 2-18 GHz frequency band. Then, the designed two 3-stage amplifiers and one 4-stage amplifier are cascaded to constitute a limiting amplifier module with minimum 80 dB small signal gain. The designed 10-stage limiting amplifier module also includes an analog voltage controllable attenuator to be used for compensating the gain variations resulting from temperature changes. The fabricated 10-stage limiting amplifier module provides 20 +/- 1.2 dBm output power level and excellent small signal gain flatness, +/- 2.2 dB, over 2-18 GHz frequency range.

Keywords: Microwave Limiting Amplifier, Instantaneous Frequency Measurement System, Negative Feedback Amplifier, Distributed Amplifier, Cascaded Amplifier.

ÖZ

YÜKSEK KAZANÇLI, GENİŞ BANTLI MİKRODALGA SINIRLAYICI YÜKSELTEÇ MODÜLÜ TASARIMI VE ÜRETİMİ

Kılıç, Hasan Hüseyin
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Doç. Dr. Şimşek Demir

Eylül 2011, 98 sayfa

Mikrodalga sınırlayıcı yükselteçler Anlık Frekans Ölçümü (AFÖ) sistemlerinin önemli parçalarındandır. Sınırlayıcı yükselteçler, geniş giriş dinamik alanda ve geniş frekans aralığında sabit çıkış gücü seviyesi sağlarlar. Ayrıca sınırlayıcı yükselteçler çok düşük giriş güç seviyelerini sabit bir çıkış güç seviyesine getirmek için kullanılan yüksek kazançlı cihazlardır. Bunun yanında, sınırlayıcı yükselteçler, AFÖ sisteminin çalışma frekans bandındaki duyarlılığını düşürmemek için, en az düşük sinyal kazanç dalgalanmasını sağlamalıdır.

Bu tez çalışmasında, yüksek kazançlı, orta güçlü, 2-18 GHz bir sınırlayıcı yükselteç modülü tasarlanmış, benzetimleri yapılmış, üretilmiş ve ölçülmüştür. İlk olarak, düşük sinyal kazancı 27 dB olan 3-aşamalı bir yükselteç tasarlanmış ve üretilmiştir. Tasarlanan 3-aşamalı yükselteç, 2-18 GHz frekans bandında en az düşük sinyal kazanç dalgalanmasını ve tatmin edici giriş ve çıkış geri dönme kayıplarını

sağlayacak şekilde, ters geri beslemeli ve dağıtık yükselteçlerin özgün bir şekilde peş peşe bağlanmasından oluşmaktadır. Daha sonra, tasarlanan iki adet 3-aşamalı yükselteç ve bir adet 4-aşamalı yükselteç, en az 80 dB düşük sinyal kazançlı bir sınırlayıcı yükselteç modülünü oluşturacak şekilde, peş peşe bağlanmıştır. Tasarlanan 10-aşamalı sınırlayıcı yükselteç, sıcaklık değişimlerinden kaynaklanan kazanç değişikliklerini telafi etmek için kullanılacak, analog voltaj ile kontrol edilebilen bir zayıflatıcıyı da içermektedir. Üretilen 10-aşamalı sınırlayıcı yükselteç modülü, 2-18 GHz frekans aralığında, 20 +/- 1.2 dBm çıkış güç seviyesi ve çok iyi düşük sinyal kazanç dalgalanması, +/- 2.2 dB, sağlamaktadır.

Anahtar Kelimeler: Mikrodalga Sınırlayıcı Yükselteç, Anlık Frekans Ölçüm Sistemi, Ters Geri Beslemeli Yükselteç, Dağıtık Yükselteç, Peş Peşe Bağlanmış Yükselteç.

To My Family

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LIST OF ABBREVIATIONS

Al_2O_3	**:**	Aluminum Oxide (Alumina)
AlGaAs	**:**	Aluminum Gallium Arsenide
AlSi	**:**	Aluminum Silicon
CPW	**:**	Coplanar Wave
DC	**:**	Direct Current
DFD	**:**	Digital Frequency Discriminator
DIST	**:**	Distributed Amplifier
EM	**:**	Electromagnetic
FET	**:**	Field Effect Transistor
FBK	**:**	Feedback Amplifier
GaAs	**:**	Gallium Arsenide
GSG	**:**	Ground-Signal-Ground
HEMT	**:**	High Electron Mobility Transistor
HFET	**:**	Heterojunction Field Effect Transistor
HFSS	**:**	High Frequency Structure Simulator
HMIC	**:**	Hybrid Microwave Integrated Circuit
IFM	**:**	Instantaneous Frequency Measurement
InGaAs	**:**	Indium Gallium Arsenide
JEDEC	**:**	Joint Electron Device Engineering Council
LNA	**:**	Low Noise Amplifier
MAG	**:**	Maximum Available Gain
MESFET	**:**	Metal Semiconductor Field Effect Transistor
MMIC	**:**	Monolithic Microwave Integrated Circuit
NF	**:**	Noise Figure
PA	**:**	Power Amplifier

PAE	**:**	Power Added Effciency
PHEMT	**:**	Pseudomorphic High Electron Mobility Transistor
RF	**:**	Radio Frequency
SMA	**:**	Sub-Miniature A Connector
SOLT	**:**	Short-Open-Load-Thru
TaN	**:**	Tantalum Nitride
TOM	**:**	Triquint's Own Model
TRL	**:**	Thru-Reflect-Line
VNA	**:**	Vector Network Analyzer
VSWR	**:**	Voltage Standing Wave Ratio

CHAPTER 1

INTRODUCTION

Signal amplification is one of the most interested research areas over the years. The introduction of radar in World War II revealed the significance of the amplification of microwave signals. Since then, amplifiers have been discussed in numerous articles, book chapters and technical journals.

Early microwave amplifiers used klystrons, vacuum tubes and magnetrons as amplifying devices. Today, most of the microwave amplifiers are solid state amplifiers which use transistors. The fabrication of high performance microwave transistors has enabled the amplifiers to operate at much higher microwave frequencies.

There are various types of amplifiers that give priority to different microwave characteristics. For example, low noise amplifiers (LNAs) are the essential components in receivers to amplify low input power levels without lowering the sensitivity of the system. On the other hand, power amplifiers (PAs) are basically used in transmitters to bring microwave signals to be transmitted to sufficient power levels. Instead of LNAs and PAs, there are also other types of amplifiers serving some special functions; such as, limiting amplifiers.

Microwave amplifiers are designed by considering many characteristics; such as, frequency range, dynamic range, input and output VSWR, power gain, noise figure

(NF), 1-dB compression point (P_{1dB}), power added efficiency (PAE), third-order intermodulation product (IP3) and stability.

1.1. Microwave Limiting Amplifiers

Microwave limiting amplifiers are the key components of Instantaneous Frequency Measurement (IFM) receivers [1]. The basic function of a limiting amplifier in an IFM receiver is to compress wide input dynamic range to a constant output dynamic range. In order to bring wide input power levels to a constant output power level, small signal gain of a limiting amplifier can be as high as 90 dB [2]. A typical input-output characteristic of a microwave amplifier is shown in Figure 1-1. Linear amplifiers give nearly constant gain in small-signal input range up to 1 dB compression point. However, limiting amplifiers provide constant saturated output power beyond some input signal level. Therefore, a limiting amplifier can be described as a saturated, high-gain microwave amplifier.

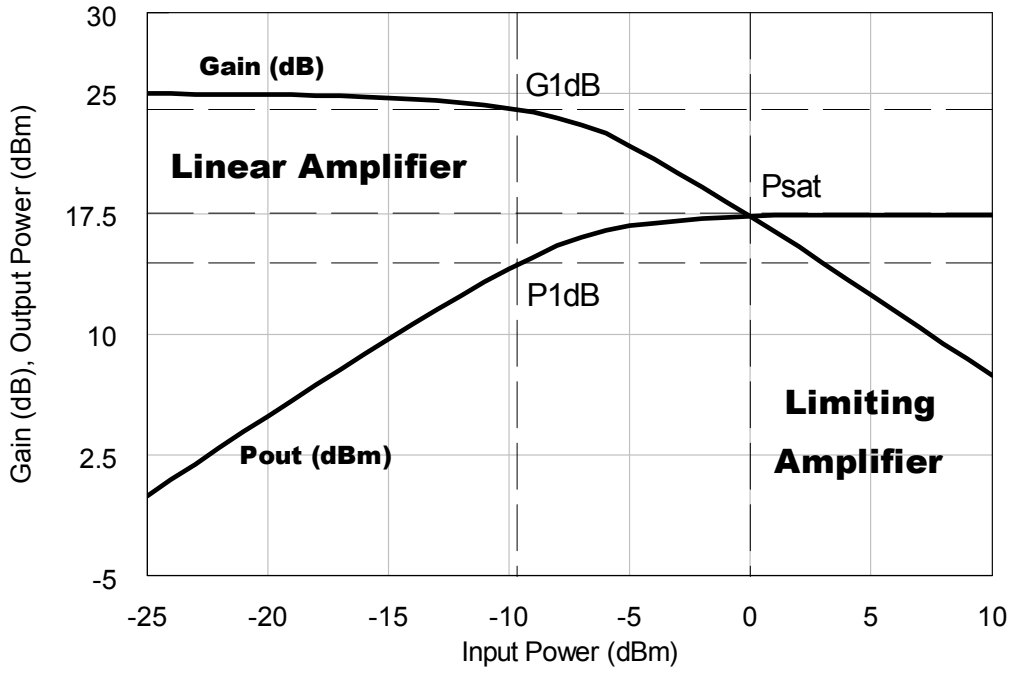


Figure 1-1: Output power vs. input power of a typical amplifier

High gain can be achieved by cascading a number of gain stages. Cascaded gain stages may be of thin film transistor gain modules [2] or MMIC amplifiers [3].

Operating frequency range of a microwave limiting amplifier may be as wide as an octave band such as 2 to 4 GHz or multi-octave band such as 2 to 18 GHz. Small signal gain flatness and output power flatness inside the operating frequency range are the two important parameters especially for multi-octave band limiting amplifiers.

A high-gain microwave amplifier can serve as a limiting amplifier. Besides, limiting amplifier can be composed of a high-gain microwave amplifier at the input and a limiter at the output stage as shown in Figure 1-2. In this structure, amplifier provides the sufficient gain for the weakest input signal and limiter provides constant output power.

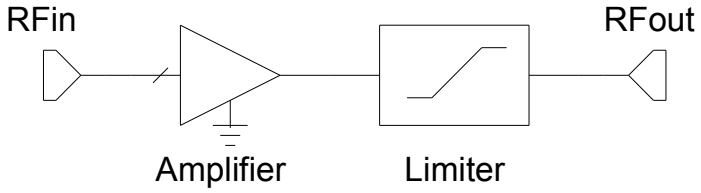


Figure 1-2: Limiting amplifier composed of high-gain amplifier and limiter

Diode limiters are the commonly used limiter types used in limiting amplifiers. The structure of a two-diode limiter is illustrated in Figure 1-3. The two diodes separated by a length of transmission line are connected in reverse directions. When the input signal exceeds a certain threshold level, the positive side of the input signal is clipped by one diode and the negative side is clipped by the other diode. Therefore, the input signal level is limited at the output of limiter.

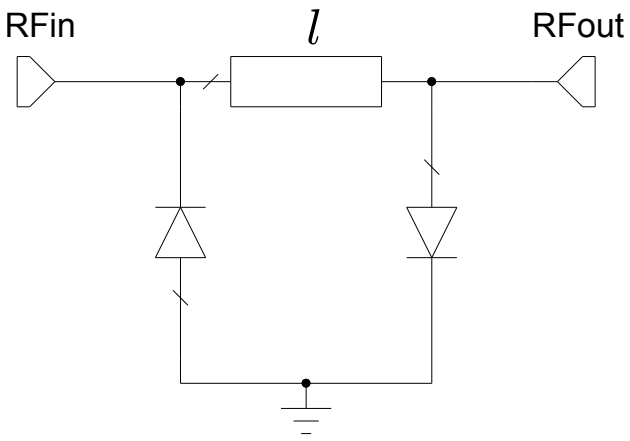


Figure 1-3: Schematic diagram of a two-diode limiter [4]

Another way of designing limiting amplifier is using alternating limiter and amplifier stages as shown in Figure 1-4.

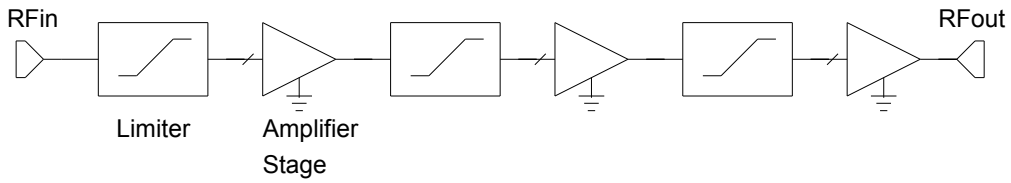


Figure 1-4: Limiting amplifier block diagram utilizing limiter/amplifier pairs [5]

The advantage of using limiters between the amplifier stages is to restrict signal levels at the input of amplifier stages such that the amplifier stages work in linear region inside the operating input dynamic range. Therefore, second harmonic levels at the output are reduced significantly even the amplifier stages are driven into deep saturation.

1.2. Instantaneous Frequency Measurement (IFM) System

The realization of an IFM receiver dates back to 1948 [6]. An IFM system measures the frequency of incoming signal by using a known delay line [7]. Digital IFM receiver known as Digital Frequency Discriminator (DFD) provides digital output of RF input signal frequency [8]. A typical IFM system is an integrated microwave/video assembly as shown in Figure 1-5. Digital IFM system owns an extra digital assembly to encode frequency information digitally.

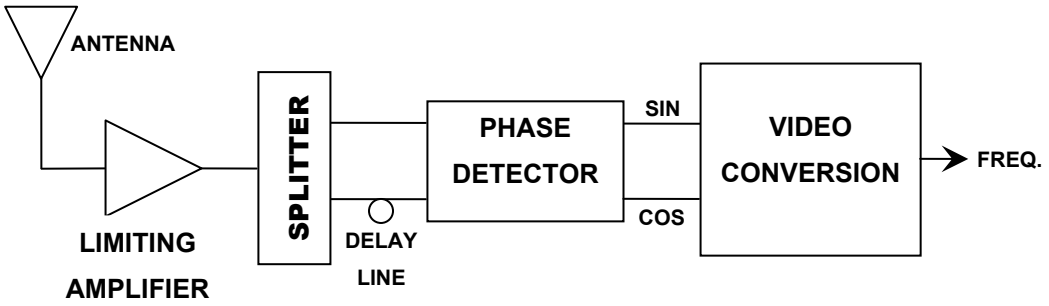


Figure 1-5: Block diagram of an IFM system

The functions of the five basic components illustrated in Figure 1-5 are listed below;

- ***Limiting Amplifier*** is capable of receiving a wide dynamic range of input signals and providing a constant power level at the output. Therefore, the capability of the IFM system to work with weak RF signals is improved by the high gain of limiting amplifier [9]. The minimum signal level to be detected in an IFM system is limited by the small signal gain of limiting amplifier. Therefore, the output of limiting amplifier should saturate when the minimum signal is applied to the input.

  The basic operating principle of an IFM system is explained assuming the input signal is a pure sinusoid. However, limiting amplifier is a nonlinear device; therefore, the harmonics at the output of limiting amplifier should be kept as low as possible for proper operation of the IFM system.

When simultaneous signals are available at the input of limiting amplifier, intermodulation products are generated. Since, IFM receiver detects one signal at a time, the performance of IFM receiver is not disturbed by the generated intermodulation products. However, limiting amplifier cannot be used at the input of any receiver other than IFM.

- ***Splitter*** divides the output of limiting amplifier into two paths. For ultra-broadband IFM receivers, multi-section power dividers are required. In order to cover 10:1 frequency range, 7-section stepped power divider is sufficient [11].

- ***Delay line*** gives a phase shift to the signal in one of the two paths of splitter output. Delay line determines the frequency resolution of IFM system. Broadband IFM systems require more than one delay line in order to resolve the ambiguities during frequency measurement. The phase difference between the delayed and undelayed path is related to frequency and group delay as given in the following formula.

$$\theta = \omega\tau \tag{1.1}$$

- ***Phase detector*** produces two video voltages from delayed and undelayed signals. The two video voltages related to frequency are sin(ωτ) and cos(ωτ). Phase detector can be designed by using hybrid couplers and mixers [9].

- ***Video converter*** extracts frequency information from the two video voltages as follows.

$$\theta = \tan^{-1}\left(\frac{\sin(\theta)}{\cos(\theta)}\right) = \omega\tau \tag{1.2}$$

1.3. Properties of Microwave Limiting Amplifiers

Since, the main application area of microwave limiting amplifier is IFM receiver, the specifications of limiting amplifier are usually dictated by the requirements of IFM receiver. Common properties of microwave limiting amplifiers are as follows.

1.3.1. Small Signal Gain

Small signal gain of a limiting amplifier depends on the minimum input signal level to be limited and the output power level. The input signal level that puts limiting amplifier into 1 dB compression point should be selected as 3 or 5 dB below the minimum input level in order to ensure that limiting amplifier is well saturated over the whole input dynamic range [1].

Small signal gain flatness of limiting amplifier is also an important parameter to be considered which is defined as shown in Figure 1-6.

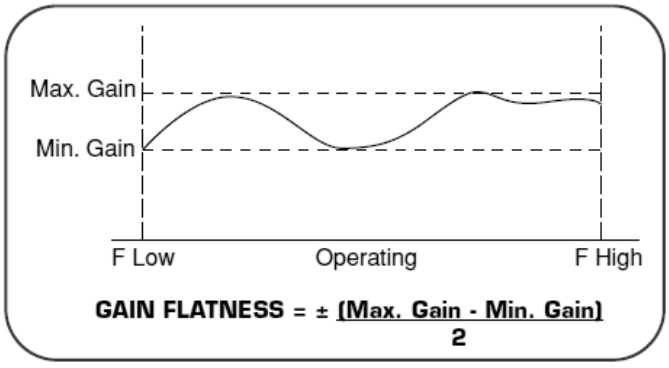


Figure 1-6: Definition of gain flatness

Gain flatness of a limiting amplifier is important for simultaneous signal performance of the IFM receiver. The relative levels of simultaneous signals in different parts of the frequency band may lead to uncertainty in frequency measurement priorities of the signals. Even the amplitude separation of two signals of different frequencies is sufficiently large at the input of limiting amplifier, the weak signal may reach the same level with the strong signal at the output if the

limiting amplifier exhibits poor gain flatness. Hence, the probability that IFM receiver to report the frequency of weak signal rather than that of strong signal increases.

1.3.2. Output Power Flatness

Output power flatness of the limiting amplifier describes the deviation of output power level with respect to frequency. As shown in Figure 1-5, there are both microwave and video components at the output of limiting amplifier. In order not to lower the sensitivity of these components over the frequency band, the output power of limiting amplifier should be kept as flat as possible.

1.3.3. Output Harmonics

Since limiting amplifier is a nonlinear device, harmonic components are present at the output of the limiting amplifier. If the limiting amplifier is multi-octave, the harmonics will fall inside the operating band that degrades the performance of IFM receiver. The harmonic performance of a typical limiting amplifier is given in Figure 1-7.

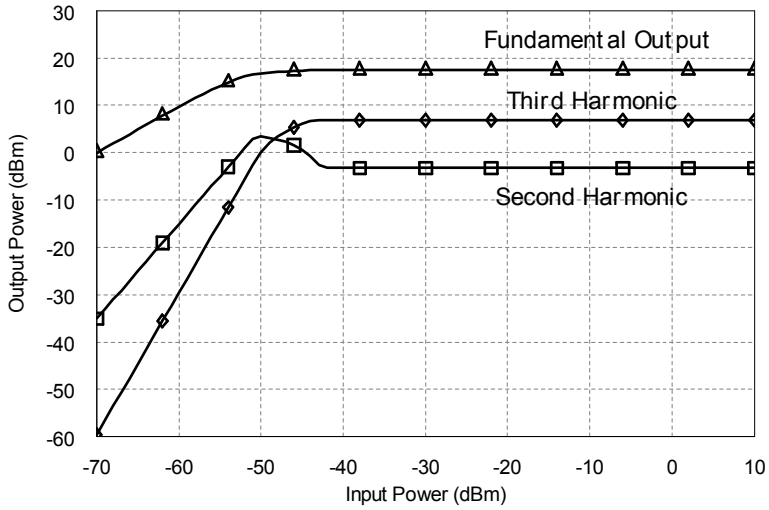


Figure 1-7: Harmonic performance of a typical limiting amplifier

Most of the time, harmonics other than 2nd and 3rd degree are ignored. Harmonic levels are expressed relative to the fundamental tone as "dBc". Typical maximum levels for the 2nd and 3rd order harmonics are -15 dBc and -9 dBc respectively. In order to obtain much lower 2nd harmonic level, amplifier/limiter pairs as shown in Figure 1-4 may be used.

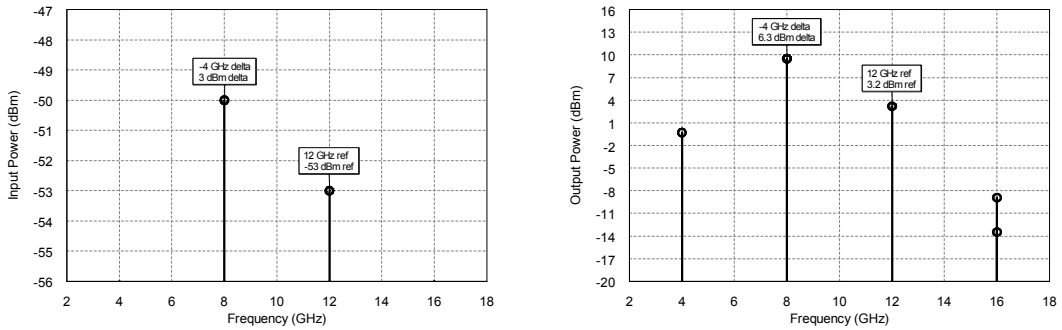
1.3.4. Small Signal Suppression

A typical limiting amplifier response can be approximated by the following formula [9].

$$V_o = \frac{\alpha}{\pi} \tan^{-1} \frac{\pi V_i}{\alpha} \tag{1.3}$$

where α is a constant related to the limiting power level and V_i and V_o are the input and output voltages, respectively.

When two simultaneous signals are present at the input of the limiting amplifier, the weak signal is suppressed more than the strong one. In other words, the difference between the power levels of two signals is increased at the output of limiting amplifier. The fact that strong signal depresses the weak signal can easily be observed by simulating a typical limiting amplifier.



(a) (b)

Figure 1-8: Simulated small signal suppression of a typical limiting amplifier (a) Input signal spectrum, (b) Output signal spectrum

For example, if two signals with 3 dB separation are applied to the input of a limiting amplifier as shown in Figure 1-8, the difference between power levels of these two signals will be approximately 6 dB, greater than 3 dB, at the output. Then, the amount of suppression is said to be equal to 3 dB for this case. As the separation between input signal levels is increased, the amount of suppression at the output of limiting amplifier will also increase. Jones, et. al, showed that maximum small signal suppression for an ideal limiter is 6 dB for large input signal separation and 4 dB for 3 dB input signal separation [10].

1.4. Research Objectives and Outline of the Thesis

The main objective of this thesis is to develop a method of cascading different types of single stage amplifiers to minimize small signal gain flatness over a wide frequency range. Then, this method is applied to the design and fabrication of a 2-18 GHz limiting amplifier module with minimum 80 dB small signal gain.

The following capabilities are acquired on the way of designing the limiting amplifier with aimed specifications.

- ***Small signal modeling of a die transistor:*** A die transistor is chosen, measured and modeled at different biasing conditions. Hence, by using the created model rather than the measured results of the transistor in amplifier simulations, the fabricated amplifier response can be predicted much more accurately. Furthermore, the comparison of small signal model parameters according to different biasing conditions enables the optimum selection of transistor biasing for different amplifier types.

- ***Analysis of different broadband amplification methods:*** Negative feedback and distributed amplification methods are analyzed and evaluated for limiting amplifier design. Then, single stage amplifiers designed by applying each method are simulated, fabricated and measured individually.

- ***Designing a multistage amplifier by applying different broadband amplification methods:*** Different types of designed single stage broadband amplifiers are cascaded to obtain higher gains. Some characteristics of multistage amplifier; such as gain flatness and return loss, are shown to be improved by cascading different types of single stage amplifiers in different orders. The optimized multistage amplifiers are also cascaded for a much higher gain limiting amplifier.

- ***Fabricating a broadband hybrid amplifier:*** The designed amplifiers are fabricated in hybrid form. Thin film circuits are integrated with discrete components such as transistor dies and chip capacitors by bondwire connections. It is shown that a broadband microwave amplifier can be fabricated in hybrid form by modeling discrete components and interconnects accurately.

- ***Tuning and improving the performance of the fabricated amplifier:*** The reasons for the variations between the performance of the fabricated amplifiers and that of the simulated amplifiers are investigated. Then, possible countermeasures against these variations are investigated in simulation environment. Finally, the performance of the fabricated amplifier is improved either by the tuning elements in thin film circuits or by changing the length of interconnects.

This thesis outlines the planning, design, simulation, fabrication and measurements of the limiting amplifier module with aimed specifications in six chapters as follows.

In Chapter 2, various transistor types used at microwave frequencies are described and compared. Different approaches for extracting small signal model of microwave FETs are also explained.

In Chapter 3, common broadband amplification methods are investigated. Moreover, circuit models and some design equations related to distributed and feedback amplifiers are given.

In Chapter 4, design process of a 2-18 GHz limiting amplifier is presented. First, the small signal modeling of the transistor to be used for limiting amplifier design is described. Then, the design steps of negative feedback amplifier and 2-stage distributed amplifier are explained. Finally, different cascade connections of three stages of designed amplifiers are simulated for minimum small signal gain ripple.

In Chapter 5, fabrication of the designed single stage and 3-stage cascaded amplifiers are presented. Then, the fabrication of a 10-stage limiting amplifier including two 3-stage and one 4-stage amplifiers in cascade is described. Moreover, the measured results of the realized amplifiers are compared with the results of EM simulations.

In Chapter 6, the thesis is concluded with a discussion of future works related to the subject.

CHAPTER 2

MICROWAVE TRANSISTORS

2.1. Transistor Types

In early years, klystrons, vacuum tubes, tunnel and varactor diodes were used in microwave amplifier design [12]. After the invention of silicon transistor, the use of transistors in microwave amplifiers has been a major research area over years. The invention of high performance semiconductors and the progress in material production technology offer development of transistors to be used at microwave frequencies. At microwave frequencies, most of the transistors are field-effect type (FET). The two common microwave FET's are metal semiconductor field effect transistor (MESFET) and high electron mobility transistor (HEMT)

2.1.1. MESFET

The MESFET was first suggested by Mead in 1966 [13]. Hooper and Lehrer showed the use of GaAs MESFET at microwave frequencies in 1967 [13]. The physical structure of MESFET is illustrated in Figure 2-1.

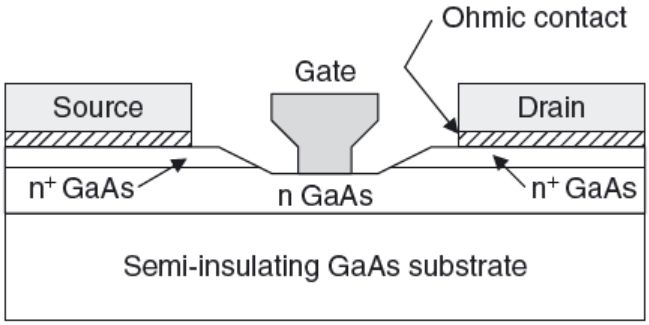


Figure 2-1: Physical structure of MESFET [14]

Gate contact of MESFET is formed by metal-semiconductor (Schottky barrier) contact. Due to the built-in potential difference between metal and semiconductor, depletion region is formed underneath the gate. Therefore, MESFET is a depletion type field effect transistor and threshold voltage (V_T) is negative. In order to create a conducting channel between drain and source, a negative gate-source voltage greater than threshold voltage ($V_{GS}>V_T$) should be applied.

Drain and source contacts of MESFET are ohmic contacts. Mostly, the source terminal of MESFET is connected to ground. A nonzero voltage applied to drain terminal ($V_D>0$) enables the drain current to flow. Above a sufficient drain voltage, drain current is saturated at I_{Dsat} value. MESFETs are mostly operated in this constant drain current (saturation) region. The saturation current is independent of drain voltage and depends on applied gate voltage. As the gate voltage becomes more negative, the saturation current I_{DSAT} starts to decrease.

2.1.2. HEMT

High electron mobility transistor (HEMT) offers superior RF performance compared to MESFET. HEMT's acquire lower noise figure, higher transconductance and higher frequency operation compared to MESFET's. The first HEMT was realized by Mimura et al. in 1980 [1]. The physical structure of HEMT is illustrated in Figure 2-2.

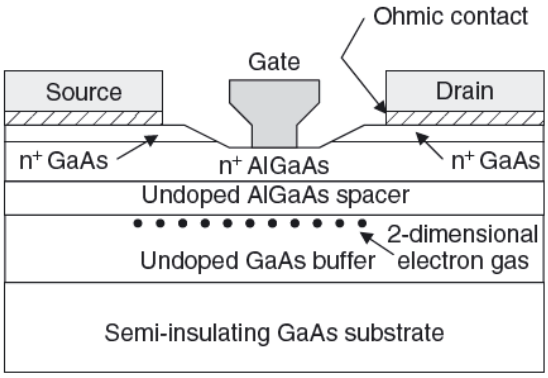


Figure 2-2: Physical structure of HEMT [14]

The structure of the HEMT is a layered structure with materials different from the MESFET structure shown in Figure 2-1. There is an AlGaAs layer on top of the GaAs layer. Due to this AlGaAs/GaAs heterojunction, HEMT is also named as heterojunction field effect transistor (HFET). AlGaAs material has higher energy bandgap compared to GaAs material. Due to this difference in energy band gaps, band-bending occurs in heterojunction interface as shown in Figure 2-3. Hence, a large population of electrons resides on heterojunction and forms two-dimensional electron gas.

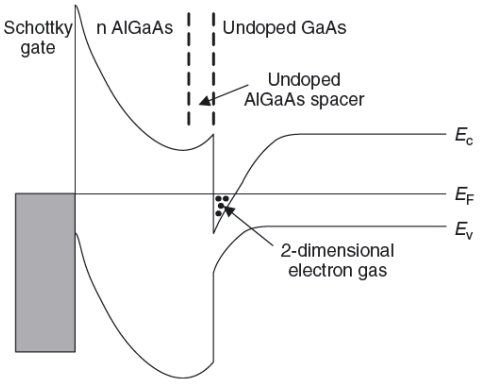


Figure 2-3: Energy band diagram of HEMT [14]

AlGaAs layer under the gate is doped; whereas, GaAs layer is undoped. Therefore, electrons from the donor AlGaAs atoms move to undoped GaAs layer with low energy level and current conduction occurs in the GaAs layer. Since, donors and electrons are at different layers, the collision between the two is minimized; hence, the velocity of electrons is increased. This is the reason why HEMT's offer higher frequency operation than MESFET's.

Different variations of HEMT have been realized over years. Pseudomorphic HEMT (pHEMT) whose physical structure is shown in Figure 2-4 is one of the variants of HEMT. InGaAs material is used between undoped GaAs and doped AlGaAs materials. Since the energy bandgap of InGaAs is lower than both GaAs and AlGaAs, the electrons have much higher velocities. Therefore, the RF performance of pHEMT is superior compared to HEMT and GaAs MESFET.

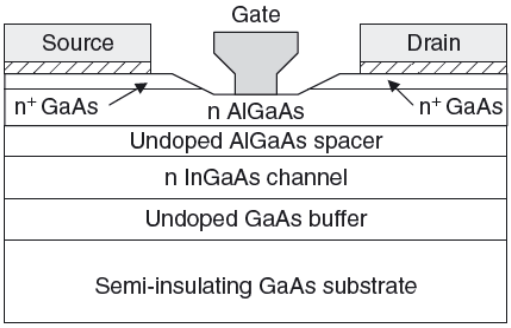


Figure 2-4: Physical structure of pHEMT [14]

2.2. Small Signal Modeling of Microwave FET's

Accurate modeling of transistor is important for amplifier design. Several methods have been proposed for determining small-signal equivalent circuit of FET at microwave frequencies [15]-[17]. The small-signal equivalent circuit elements were first determined for MESFET. However, the same equivalent model is used for HEMT due to structural similarities between MESFET and HEMT. A small-signal equivalent circuit of a field-effect transistor is comprised of 15 variables as illustrated in Figure 2-5.

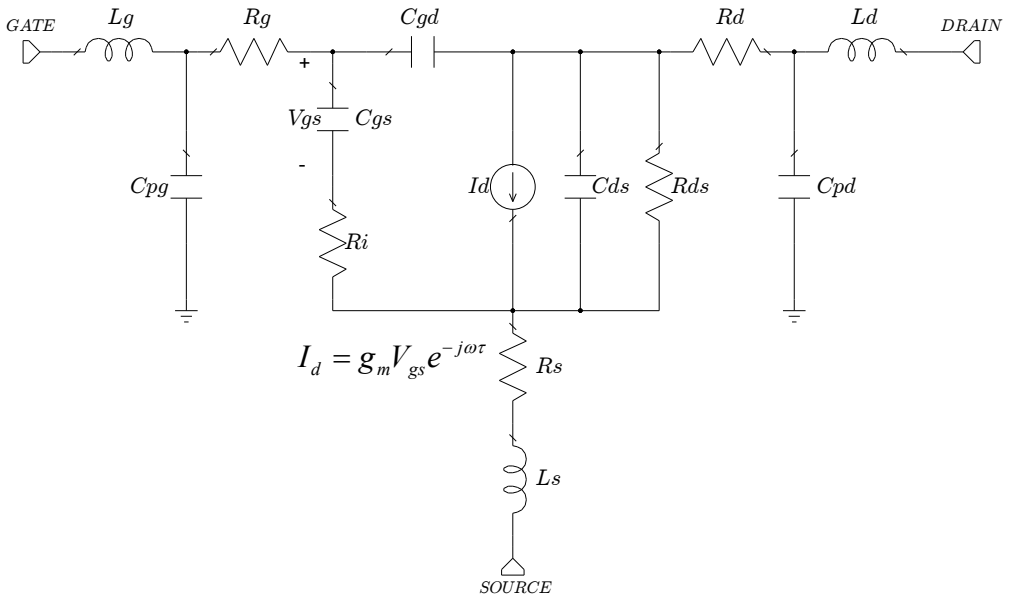


Figure 2-5: Small signal equivalent circuit of field effect transistor

Accurate broadband S-parameter measurement of FET is required to extract equivalent circuit's element values. Equivalent circuit of FET consists of elements independent of biasing conditions (extrinsic elements) and elements depending on biasing conditions (intrinsic elements). Extrinsic elements are L_g, R_g, C_{pg}, L_d, R_d, C_{pd}, L_s and R_s. Intrinsic elements are C_{gs}, C_{gd}, R_i, C_{ds}, R_{ds} and a voltage-controlled current source which depends on g_m and τ parameters .

2.2.1. Determination of Extrinsic Elements

Dambrine [15] used S-parameter measurements at zero drain-source (V_{ds}=0) voltage and gate-source voltage greater than pinch-off voltage (V_{gs}>V_p) for determination of parasitic inductances (L_g, L_d, L_s). Moreover, package capacitances (C_{pg}, C_{pd}) are determined for V_{ds}=0 and V_{gs}<V_p biasing condition and parasitic resistances are extracted by using dc measurements in Dambrine's paper [15]. Yanagawa showed that parasitic resistances and inductances can be extracted from S-parameters of pinched-off FET at zero drain-source voltage [17]. GaAs FET biased at V_{ds}=0 is named as "cold FET" and equivalent circuit of pinched-off cold FET is illustrated in Figure 2-6.

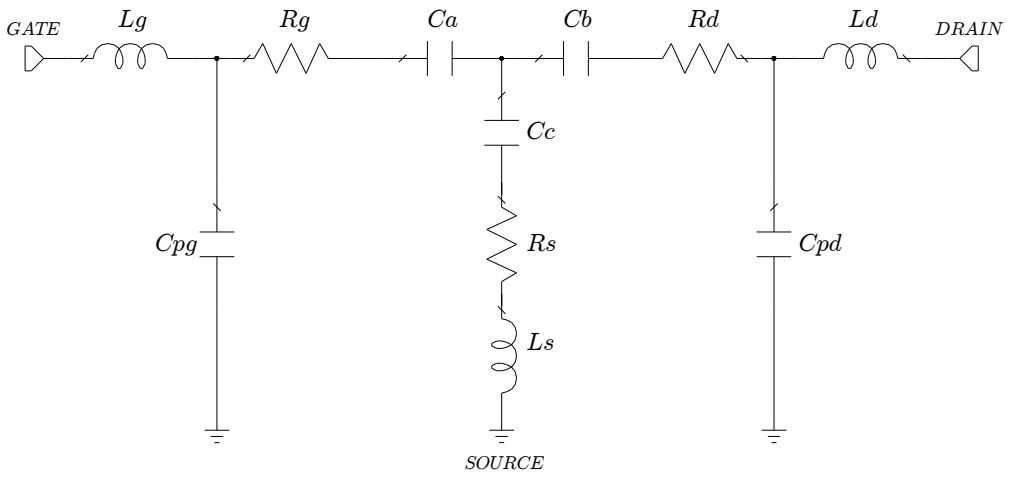


Figure 2-6: Equivalent circuit of pinched-off cold FET [17]

For GaAs FETs with negligibly small pad capacitances, neglecting C_{pg} and C_{pd} from equivalent circuit in Figure 2-6 does not cause too much error. Then, parasitic resistances (R_g, R_d, R_s) and parasitic inductances (L_g, L_d, L_s) can be analytically extracted from Z-parameters of pinched-off cold FET as,

$$R_g = \mathrm{Re}(Z_{11} - Z_{12}) \tag{2.1}$$

$$R_d = \mathrm{Re}(Z_{22} - Z_{12}) \tag{2.2}$$

$$R_d = \mathrm{Re}(Z_{11}) \tag{2.3}$$

$$\omega\,\mathrm{Im}(Z_{11}) = \omega^2(L_g + L_s) - \frac{1}{C_{ab}} \tag{2.4}$$

$$\omega\,\mathrm{Im}(Z_{22}) = \omega^2(L_d + L_s) - \frac{1}{C_{bc}} \tag{2.5}$$

$$\omega\,\mathrm{Im}(Z_{12}) = \omega^2 L_s - \frac{1}{C_b} \tag{2.6}$$

$$C_{ab}^{-1} = C_a^{-1} + C_b^{-1} \tag{2.7}$$

$$C_{bc}^{-1} = C_b^{-1} + C_c^{-1} \tag{2.8}$$

Parasitic inductances (L_g, L_d, L_s) can be obtained from the slopes of straight lines formed by $\omega\mathrm{Im}(Z_{11})$, $\omega\mathrm{Im}(Z_{22})$ and $\omega\mathrm{Im}(Z_{12})$ against ω^2. Package capacitances (C_{pg}, C_{pd}) can be estimated from geometrical bond-pad capacitances. Moreover, by using pinched-off cold model of FET, parasitic resistances and parasitic inductances have negligible effect on imaginary part of Y-parameters at low frequencies. Then, C_{pg} and C_{pd} can be calculated up to a few gigahertz as [15],

$$\mathrm{Im}(Y_{11}) + 2\,\mathrm{Im}(Y_{12}) = j\omega C_{pg} \tag{2.9}$$

$$\mathrm{Im}(Y_{22}) + \mathrm{Im}(Y_{12}) = j\omega C_{pd} \tag{2.10}$$

C_{pg} and C_{pd} can be estimated from the slopes of (2.9) and (2.10) against ω.

2.2.2. Determination of Intrinsic Elements

The S-parameter measurement of FET at operating bias point is required for determination of intrinsic elements. The analytically extracted extrinsic elements can be de-embedded from two-port S-parameter measurement according to the equivalent circuit of FET in Fig. 4. After de-embedding extrinsic elements, the equivalent circuit becomes as in Fig. 7. Since, the FET is biased at operating point, it is called as hot FET as in Figure 2-7. The modeling of FET at operating bias point is also cold as "*hot modeling*".

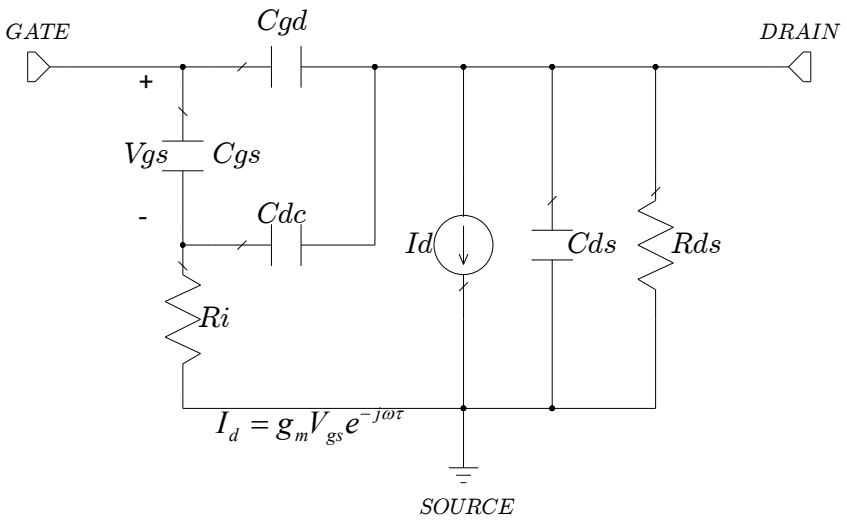


Figure 2-7: Equivalent circuit of hot FET [17]

The equivalent circuit of hot FET in Figure 2-7 includes eight elements contrary to seven-element model in Figure 2-5. Eight-element model has an additional element, C_{dc}, which represents the effect of drain-to-channel feedback capacitance. The intrinsic parameters of the FET can be calculated from the following formulas by using Y-parameters of the FET which can be obtained by the transformation of measured S-parameters to Y-parameters.

$$C_{gs} = \frac{\left|Y_{11} + Y_{12}\right|^2}{\omega \,\mathrm{Im}(Y_{11} + Y_{12})} \tag{2.11}$$

$$C_{dc} = \frac{C_{gs}\,\mathrm{Re}(Y_{12})}{\mathrm{Re}(Y_{11})} \tag{2.12}$$

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega} - \frac{\omega^2 \tau_1 \tau_2 C_{gs}}{1 + (\omega \tau_2)^2} \tag{2.13}$$

$$R_i = \frac{\mathrm{Re}(Y_{11})}{\omega C_{gs}\,\mathrm{Im}(Y_{11} + Y_{12})} \tag{2.14}$$

$$\tau_1 = R_i C_{dc} \tag{2.15}$$

$$\tau_2 = R_i (C_{gs} + C_{dc}) \tag{2.16}$$

$$g_m = \left|Y_{21} - Y_{12}\right| \frac{\sqrt{(1 + \omega {\tau_2}^2)}}{\sqrt{(1 + \omega {\tau_1}^2)}} \tag{2.17}$$

$$\tau = \frac{1}{\omega}\left[-\tan^{-1}\left\{\frac{\mathrm{Im}(Y_{12} - Y_{21})}{\mathrm{Re}(Y_{12} - Y_{21})}\right\} + \tan^{-1}\left\{\frac{\omega(\tau_1 - \tau_2)}{1 + \omega^2 \tau_1 \tau_2}\right\}\right] \tag{2.18}$$

$$G_{ds} = \mathrm{Re}(Y_{22} + Y_{21}) - \frac{g_m(\cos \omega\tau - \omega\tau_2 \sin \omega\tau) + \omega^2 \tau_1 (C_{dc} + C_{gs})}{1 + (\omega \tau_2)^2} \tag{2.19}$$

$$C_{ds} = \frac{\omega\tau_2\,\mathrm{Re}(Y_{22} + Y_{21}) + \mathrm{Im}(Y_{22} + Y_{21}) - \omega\tau_2 G_{ds} + g_m \sin \omega\tau}{\omega} - C_{dc} \tag{2.20}$$

After intrinsic elements are obtained by using (2.11) to (2.20), the complete 16 elements constituting small signal model of FET are extracted analytically. For higher accuracy, analytically extracted element values are taken as starting values and the small-signal model elements are optimized by using a suitable optimization routine.

2.3. Figures of Merit

2.3.1. Cut-off Frequency

Cut-off frequency (f_T) is a measure of high-speed capability of FET. Cut-off frequency is the frequency at which the FET has unity current gain. When FET parasitics are ignored, f_T can be represented by the following expression [13],

$$f_T = \frac{g_m}{2\pi((C_{gs} + C_{gd})} = \frac{v}{2\pi L} \tag{2.21}$$

Here, v is the drift velocity and L is the gate length. Hence, (2.21) relates L/v with cut-off frequency and FET parameters (g_m, C_{gs} and C_{gd}). Since, $C_{gs}>>C_{gd}$ for most of the FET's, f_T is proportional to g_m/C_{gs} ratio. Drift velocity (v) is the same with saturation velocity (v_{sat}) for short channels. Besides, v_{sat} is specific to the material used for FET production. Therefore, f_T can be increased by either shortening the gate length or using a material with higher v_{sat}.

A more accurate expression for cut-off frequency including the effects of FET parasitics is given below [13],

$$f_T = \frac{g_m}{2\pi((C_{gs} + C_{gd})\left(1 + \frac{R_d + R_s}{R_{ds}}\right) + C_{gd} g_m (R_d + R_s) + C_{pg}} \tag{2.22}$$

2.3.2. Maximum Frequency of Oscillation

Another figure of merit for high frequency performance of FET is the maximum frequency of oscillation (f_{max}). The maximum available gain (MAG) of the FET can be approximated as [14],

$$MAG = \left(\frac{f_T}{f}\right)^2 \frac{1}{4R/R_{ds} + 4\pi f_T C_{gd}(R + R_g + \pi f_T L_s)} \tag{2.23}$$

where

$$R = R_g + R_i + R_s + \pi f_T L_s \text{ and } f_T = \frac{g_m}{2\pi C_{gs}} \tag{2.24}$$

As can be seen from (2.23), MAG is inversely proportional to f^2. Therefore, MAG decreases by 6 dB/octave over frequency. Maximum frequency of oscillation (f_{max}) is defined as the frequency at which MAG drops to unity as given by [14],

$$f_{\max} = f_T\left[4R/R_{ds} + 4\pi f_T C_{gd}(R + R_g + \pi f_T L_s)\right]^{-1/2} \tag{2.25}$$

Both (2.22) and (2.25) show that parasitics of FET have deteriorating effect on both f_T and f_{max}.

CHAPTER 3

BROADBAND AMPLIFICATION METHODS

Many systems such as electronic warfare and optical communication systems require broadband amplifiers [18]. The three commonly used techniques to realize broadband amplifiers are reactive/lossy matching, travelling-wave (distributed) and parallel feedback approaches.

3.1. Reactively/Lossy Matched Amplifiers

As mentioned in Chapter-2, maximum available gain of a FET rolls of 6 dB/octave over frequency. This 6 dB/octave gain roll-off can be compensated by input and output matching networks. The schematic of a reactively/lossy matched amplifier is shown in Figure 3-1.

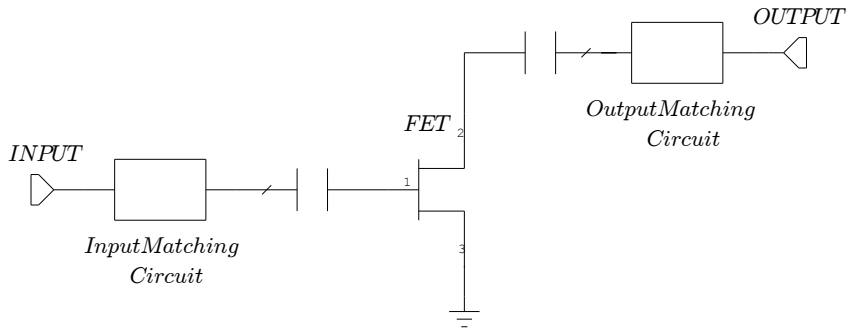


Figure 3-1: Schematic of a reactively/lossy matched amplifier [18]

The gain responses of matching networks should present a positive roll-of in order to equalize the gain response of the FET. The type of matching network used for amplifier determines whether the amplifier is reactively matched or lossy matched. Some commonly used gain equalizing networks are illustrated in Figure 3-2.

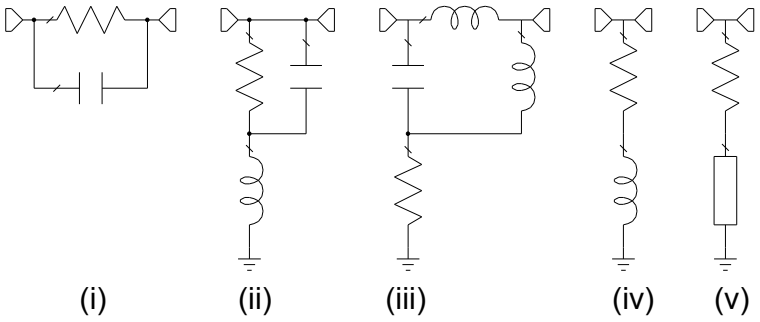


Figure 3-2: Gain equalizing networks [14]

3.2. Distributed Amplifiers

Distributed amplification is the most widely used broadband amplification method in the literature. The concept of distributed amplification was first suggested by William S. Percival in 1936 [19]. However, a significant improvement to Percival's idea was made by the paper of Edward L. Ginzton in 1948 [20]. The *distributed amplifier* term was first mentioned in Ginzton's paper by using vacuum tubes. After transistors took the place of vacuum tubes at microwave frequencies, analysis of distributed amplifiers using discrete FET's became popular. A common approach for designing distributed amplifier is to absorb FET parasitics into input and output transmisson lines. A schematic representation of four stage distributed amplifier is shown in Figure 3-3.

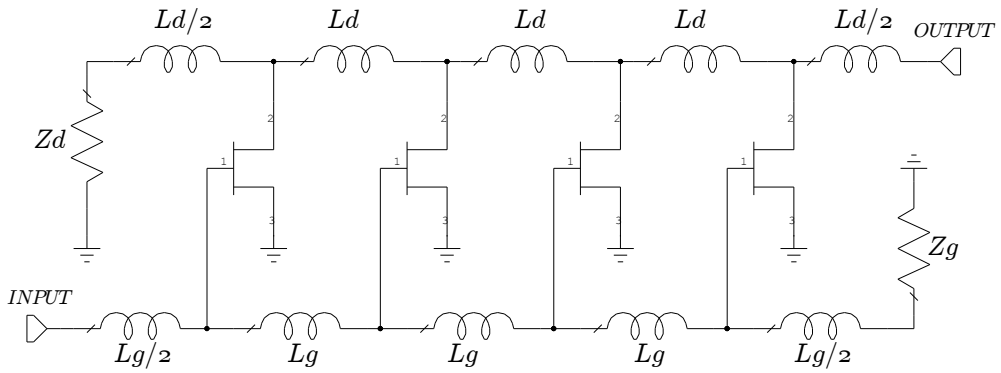


Figure 3-3: Schematic of four stage distributed amplifier [21]

Simplified schematic diagrams of input and output transmission lines of four-stage distributed amplifier are illustrated in Figure 3-4. Input transmission line formed by the gate parasitics of the FET and lumped inductors is referred to as gate line. Similarly, output transmission line formed by the drain parasitics of the FET and lumped inductors is referred to as drain line. Gate and drain lines are coupled to each other by the transconductance, g_m, of the FET.

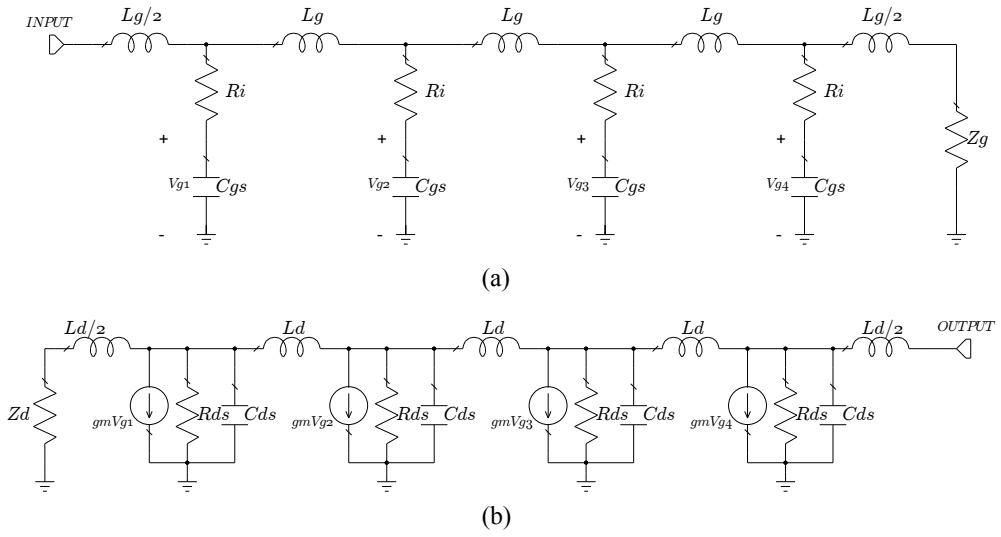


Figure 3-4: Equivalent schematics of (a) gate line, (b) drain line

Neglecting gate and drain line losses, the overall gain of an n-stage distributed amplifier can be written as [21];

$$G \cong \frac{g_m{}^2 n^2 Z_0{}^2}{4} \tag{3.1}$$

This expression shows that the gain of distributed amplifier is proportional to n^2, whereas, the gain of cascaded amplifier increases by $g_m{}^n$. Therefore, the gain of distributed amplifier is smaller than cascaded amplifier assuming the same number of stages is used. Another characteristic of distributed amplifier is that due to gate and drain line losses, gain cannot be increased indefinitely by increasing the number of active devices, n. Above a specific number of active devices, attenuation of gate and drain lines become dominant and gain of the amplifier begins to decrease. Therefore, there is an optimum number of active devices that maximizes the gain at a specific frequency as [22];

$$N_{opt} = \frac{In(A_d / A_g)}{A_d - A_g} \tag{3.2}$$

where A_d and A_g are expressions for attenuations on gate and drain lines [22].

The characteristic impedances of gate and drain lines are given by

$$Z_{0g} = \sqrt{\frac{L_g}{C_{gs}}} \tag{3.3}$$

$$Z_{0d} = \sqrt{\frac{L_d}{C_{ds}}} \tag{3.4}$$

Similarly the cut-off frequencies of gate and drain lines are [22]

$$\omega_{cg} = \frac{2}{\sqrt{L_g C_{gs}}} \tag{3.5}$$

$$\omega_{cd} = \frac{2}{\sqrt{L_d C_{ds}}} \tag{3.6}$$

The following conditions should apply for distributed amplifiers to operate properly [23];

$$Z_{0g} = Z_{0g} = Z_0 \tag{3.7}$$

$$\omega_{cg} = \omega_{cd} = \omega_c \tag{3.8}$$

These conditions require L_g=L_d and C_{gs}=C_{ds}. Since $C_{gs} > C_{ds}$ for GaAs FET's, gate and drain capacitances can be equalized by adding extra shunt capacitance (C_p) to drain terminal of the FET as in Figure 3-5 [23]. Then,

$$C_{gs} = C_{ds} + C_p \tag{3.9}$$

The disadvantage of adding shunt capacitance to drain terminal is that the cut-off frequency of drain line is decreased. Another method of equalizing gate and drain capacitances without lowering the cut-off frequency of drain line is to add series capacitance to gate terminal of the FET as in Figure 3-6.

$$C_{ds} = \frac{C_{gs} C_s}{C_{gs} + C_s} \tag{3.10}$$

By following this technique, the cut-off frequency of gate line is increased such that the bandwidth of the amplifier is extended. However, the voltage swing accross the gate terminal of the FET is reduced as in the following relation;

$$C_{ds} = \frac{C_s}{C_s + C_{gs}} V_g \tag{3.11}$$

The reduction in voltage swing leads the overall gain of the amplifier to drop. However, this also increases the power handling capacity of the transistor. Therefore, this method is mostly used for high power amplifiers rather than high gain amplifiers.

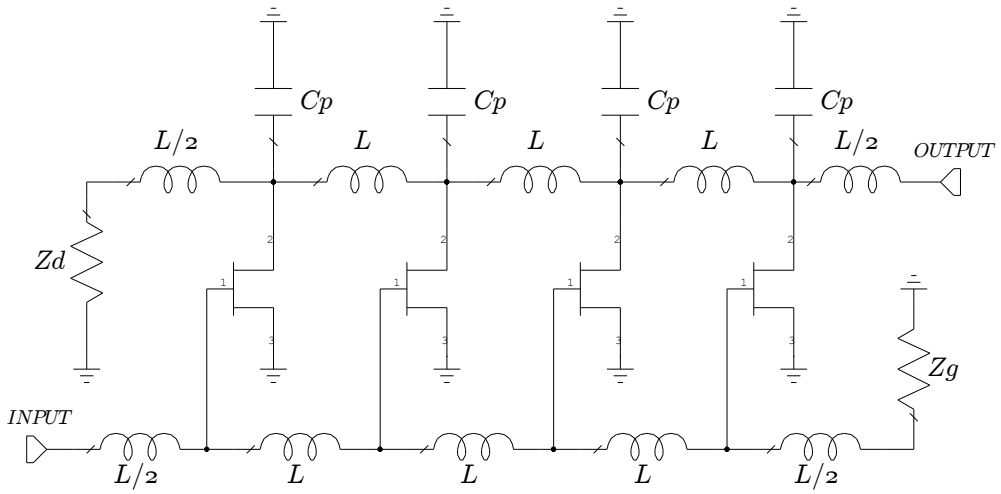


Figure 3-5: Schematic of four stage distributed amplifier with extra shunt drain capacitance (Cp) [24]

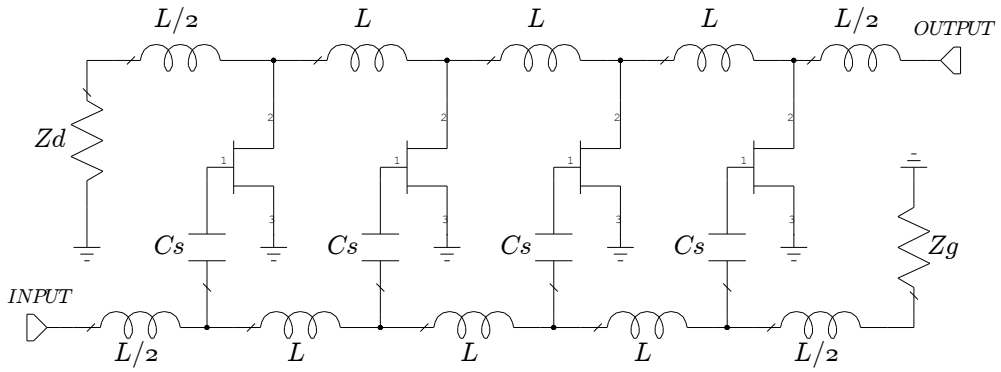


Figure 3-6: Schematic of four stage distributed amplifier with extra series gate capacitance (Cs) [24]

3.3. Negative Feedback Amplifiers

Another widely used broadband amplification method is negative feedback amplification. The *negative* term is due to the 180 degrees phase difference between input and output for a FET type transistor. The schematic diagram of the basic feedback amplifier is shown in Figure 3-7

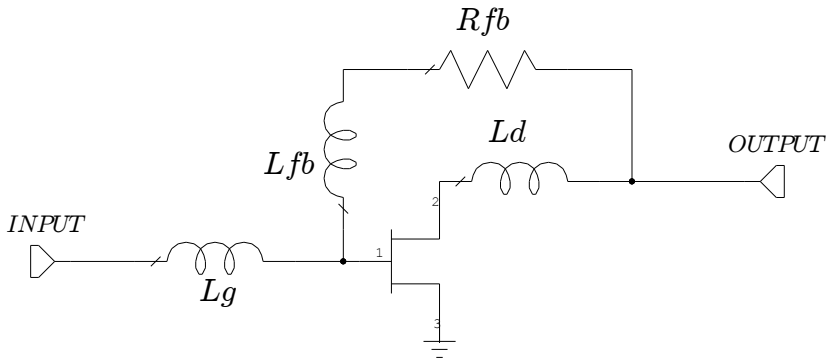


Figure 3-7: Schematic of negative feedback amplifier [25]

The gain of a FET has 6 dB/octave slope with frequency as in Figure 3-8. Feedback resistor, R_{fb}, is responsible from the reduction of gain to desired gain level, G_{DES}, at f_1 frequency. The gain at the upper frequency f_2 should be kept constant at G_{DES} in order to obtain a flat gain characteristic between f_1 and f_2 frequencies. This is achieved thanks to feedback inductance, L_{fb}, since it presents high impedance at f_2 frequency, such that feedback from output to input is highly reduced at this frequency. The effect of drain inductance, L_d, is to extend the upper frequency band from f_2 to f_3 frequency by compensating the parasitic drain capacitance of the FET such that output matching of the FET is improved. Another beneficial effect of L_d is to increase the gain at f_2 frequency; then, by appropriate choice of R_{fb}, the gain between f_1 and f_2 frequencies can be drawn to a higher level.

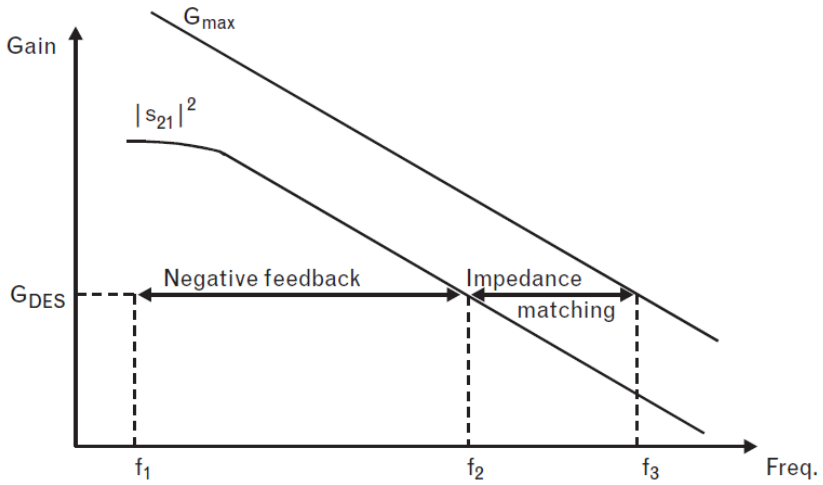


Figure 3-8: Open loop gain of a FET and the effect of negative feedback [26]

The analysis of feedback amplifier at high frequencies is difficult, because of the complexity of transistor model. Low-frequency analysis of feedback amplifier is much simpler and enables the selection of R_{fb} for optimum matching condition. The low-frequency model of feedback amplifier is illustrated in Figure 3-9.

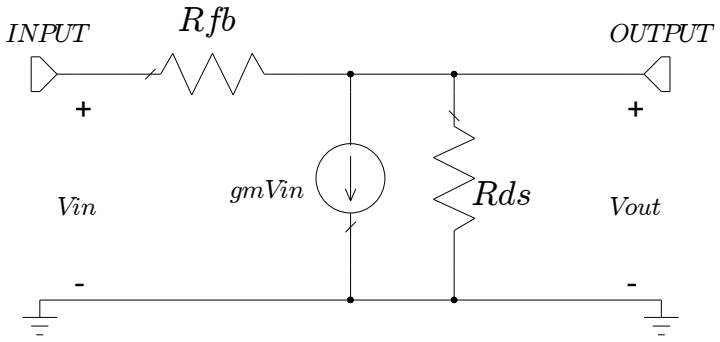


Figure 3-9: Low-frequency model of feedback amplifier [25]

Niclas, et. al, showed that the ideal matching condition (S_{11}=S_{22}=0) is only satisfied when 1/R_{ds}=0. Then, the value of R_{fb} for ideal matching is found as;

$$R_{fb} = g_m Z_0^{\,2} \tag{3.12}$$

For this feedback resistor value, the S parameters become;

$$S_{11} = S_{22} = 0 \tag{3.13}$$

$$S_{12} = \frac{1}{g_m Z_0 + 1} \tag{3.14}$$

$$S_{21} = -(g_m Z_0 - 1) \tag{3.15}$$

CHAPTER 4

BROADBAND LIMITING AMPLIFIER DESIGN

In this work, a medium power limiting amplifier working across 2-18 GHz frequency range is aimed to be designed and fabricated. First, a 3-stage limiting amplifier with nearly 27 dB gain is designed and optimized for minimum small signal gain flatness. Then, a 10-stage limiting amplifier with nearly 80 dB gain is designed by cascading 3-stage designs. 10-stage limiting amplifier design includes an analog voltage controlled attenuator for temperature compensation. Moreover, both 3-stage and 10-stage limiting amplifiers can be biased from a single +12 V biasing voltage.

The selection of a suitable microwave transistor is the starting point of the limiting amplifier design. Output power, gain and cut-off frequency are the three major parameters when determining the transistor. Then, the chosen transistor is measured and modeled at different biasing conditions.

Since the designed limiting amplifier should operate satisfactorily across the ultra-wideband frequency range (2-18 GHz), both distributed amplification and negative feedback amplification methods are applied during the limiting amplifier design. First, single stage distributed and negative feedback amplifiers are designed individually. Then, in order to obtain desired 27 dB small signal gain, three single stage amplifiers are cascaded.

The designed single stage amplifiers are self-biased amplifiers; such that, a single biasing voltage is enough for the operation of cascaded amplifier.

The amplifier simulations and transistor modeling are carried out using Microwave Office^{TM}. Besides, the simulations of transistor interconnects are carried out using Ansoft HFSS^{TM} 3D simulation package.

4.1. Transistor Selection and Modeling:

4.1.1. Transistor Selection:

As explained in Chapter-2, pHEMT type transistors have superior RF performance as compared to MESFET and HEMT. Therefore, RFMD-FPD200 pHEMT die is chosen for limiting amplifier design. FPD200 is an AlGaAs/InGaAs pHEMT featuring 0.25umx200um schottky barrier gate [27]. The cut-off frequency of FPD200 can be calculated by using the formula,

$$f_T = \frac{v}{2\pi L} \tag{4.1}$$

where v=1x10^7 cm/s for InGaAs material and L=0.25 um for FPD200. Then, cut-off frequency (f_T) can be calculated as 63.66 GHz.

The features of FPD200 are summarized in Table 4-1.

Table 4-1: Features of FPD200

Output P_{1dB}	19 dBm
Power Gain at 1dB (G_{1dB})	13 dB @ 12 GHz
Maximum Stable Gain (S_{21}/S_{12})	17 dB @ 12 GHz, 12 dB @ 18 GHz
Noise Figure	1.2 dB
Power Added Efficiency (PAE)	45%

The large-signal model of FPD200 is supplied by the manufacturer. However, for small-signal design this is not sufficient; since, large signal model does not fit small

signal model at all bias points. Therefore, using large-signal model for small-signal amplifier design is not the appropriate choice. Some S-parameter measurements of FPD200 are also available. However, the supplied S-parameters are measured at limited number of bias points. Besides, the effects of transistor interconnects are not possible to be extracted from S-parameter measurements. Hence, the small-signal modeling of FPD200 is very important for the aim of designing a limiting amplifier with desirable small-signal gain flatness.

4.1.2. Small Signal Modeling of FPD200

Accurate broadband S-parameter measurement of FPD200 is required for accurate extraction of small-signal model elements. The calibration of network analyzer plays an important role on accurate S-parameter measurements. Different calibration standards are used for network analyzer calibration. Short, open, load and through (SOLT) standards are one of the commonly used calibration standards especially for coaxial medium. The description of SOLT standards is illustrated in Figure 4-1.

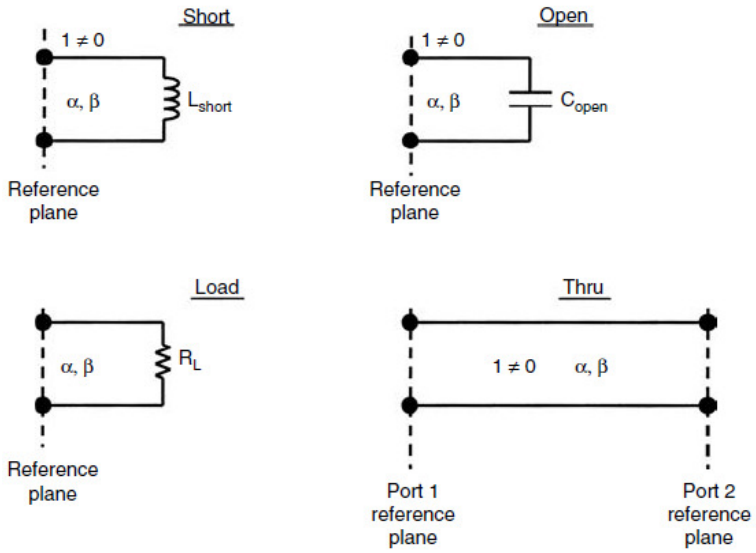


Figure 4-1: SOLT calibration standards [28]

As can be seen from Figure 4-1, SOLT standards use nonzero length transmission lines. Therefore, these nonzero length transmission lines lead to calibration errors especially at high frequencies.

Due to high frequency errors of SOLT calibration method, thru, reflect and line (TRL) standards have become popular. TRL calibration is also more suitable to microstrip environment than SOLT calibration. Besides, the characterization of reflect standard (open or short), which is another limitation of SOLT calibration, is not required in TRL calibration. Moreover, either zero-length or nonzero-length thru standard may be used. The length of line standard is determined such that insertion phase of line standard is between acceptable limits inside the calibration frequency range. The recommended insertion phase interval of line standard is between 20 and 160 degrees; therefore, only 8:1 frequency range can be covered with a single line standard [29]. In order to cover frequency span greater than 8:1, multiple lines must be used. TRL also requires specially built split-block test fixture as shown in Figure 4-2. The fixture given in the following figure provides connection interface repeatability; hence, the measurements of all calibration standards can be made with the same connection interface.

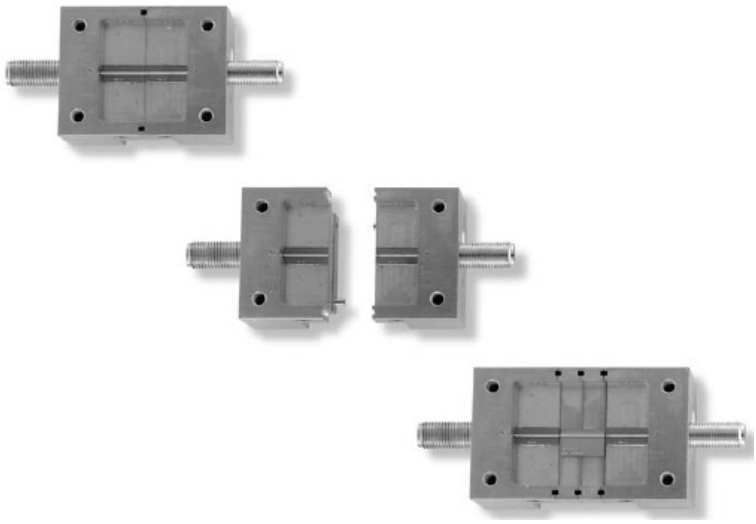


Figure 4-2: Split-block fixture for TRL calibration [29]

Another common method for measuring S-parameters of a transistor is using an on-wafer test setup. RF probes are connected to microstrip lines via coplanar-waveguide (CPW) interface. The effect of RF probes and interconnecting lines can be removed by high-precision CPW-microstrip adapters and calibration kits [30]. Therefore, the reference plane for S-parameter measurement can be transferred to the contact point of the transistor.

The picture of FPD200 die with input and output CPW-microstrip adaptors is shown in Figure 4-3. Ground-signal-ground (GSG) type RF probes are used for S-parameter measurements in the probe-station. Gate and drain supply voltages of FPD200 are applied by using broadband bias-tees at both input and output. The effects of bias-tees are also included in the calibration. The effects of CPW-microstrip adaptors are removed by a special calibration substrate, such that, S-parameters of FPD200 die are measured just at the contact points of gate and drain bondwires. Therefore, the measurements only include transistor parasitics.

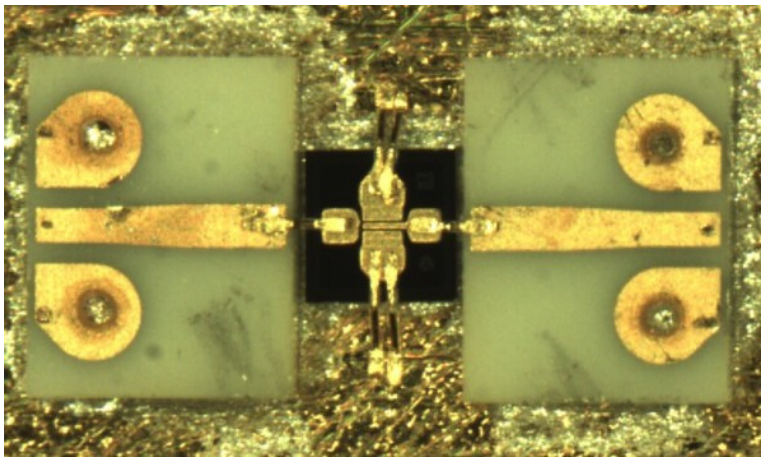


Figure 4-3: Picture of FPD200 chip with CPW-microstrip adapters

Small signal S-parameters of FPD200 are measured at different gate and drain supply voltages in 2-18 GHz frequency range. Moreover, pinched-off S-parameters are measured in order to determine parasitic elements analytically. After S-parameter measurements, the small signal model elements are extracted analytically as explained in Chapter-2. The extracted element values are taken as starting values and

optimized for higher accuracy. During optimization, higher weights are given to phases of S-parameters. The obtained small signal model elements of FPD200 before and after optimization for V_{gs}=-0.45V, V_{ds}=3V and I_{ds}=32mA biasing conditions are given in Table 4-2.

Table 4-2: Small-signal model element values of FPD200 before and after optimization

Element	Before Optimization	After Optimization	Unit
Rg	2.5	2.8	ohm
Rd	3.5	4	ohm
Rs	3	3	ohm
Lg	0.16	0.16	nH
Ld	0.17	0.15	nH
Ls	0.035	0.037	nH
Cpg	0.06	0.06	pF
Cpd	0.06	0.06	pF
Cgs	0.38	0.37	pF
Cgd	0.018	0.017	pF
Cds	0.045	0.042	pF
Cdc	0.01	0	pF
Ri	3.5	2	ohm
Rds	280	280	ohm
gm	104	106	mS
tau	0.4	0.6	psec

It can be seen from Table 4-2 that no significant difference exists between analytically extracted and optimized small signal model elements. Hence, analytical extraction method is proven to be used conveniently for small signal modeling of pHEMT type transistors.

The comparison of S-parameters of modeled and measured FPD200 in 2-18 GHz frequency range is shown in Figure 4-4.

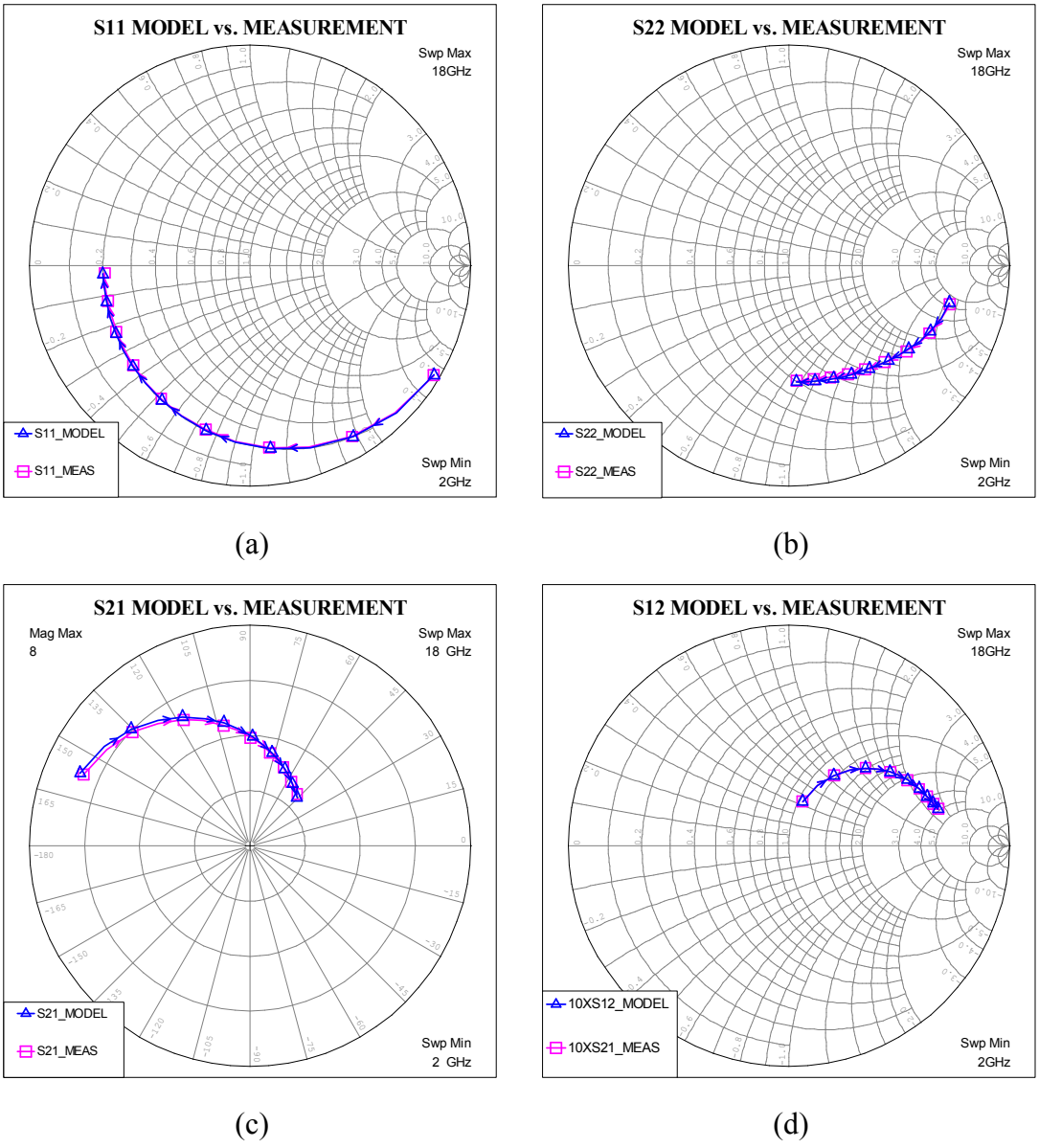


Figure 4-4: Comparison of small-signal model and measured S-parameters, (a) S_{11}, (b) S_{22}, (c) S_{21}, (d) S_{12}

The created small signal model of FPD200 fits quite good to measurements over 2-18 GHz frequency range as Figure 4-4 depicts.

4.1.3. Large Signal Model of FPD200

Large signal model of a transistor is required for performing nonlinear simulations. Since large signal modeling of a transistor is much more complicated and time consuming task as compared to small signal modeling, the supplied large signal model of FPD200 is used for simulating nonlinear properties of the designed amplifiers.

TOM2 and TOM3 models of FPD200 are supplied by RFMD company. TOM which stands for Triquint's Own Model is a nonlinear MESFET model developed by Triquint Inc. [31]. TOM3 model is superior than TOM2 model due to its advanced charge model [32]. Moreover, most simulators include TOM3 model rather than TOM2 model.

Extracted parasitic components of FPD200 are combined with the supplied TOM3 model for higher accuracy as illustrated in Figure 4-5.

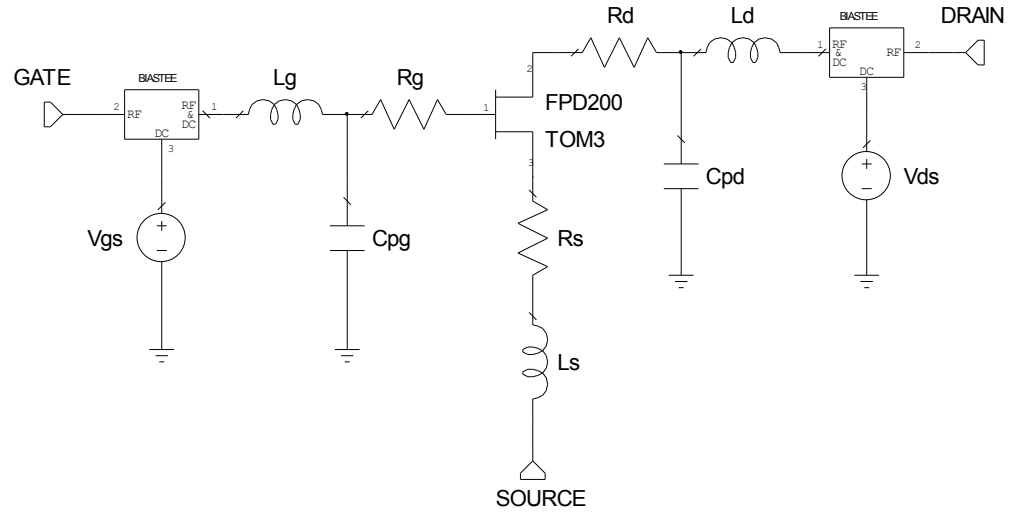


Figure 4-5: The combination of TOM3 model of FPD200 with the modeled gate, drain and source parasitics

The IV characteristics and output power characteristics of FPD200 are simulated as shown in Figure 4-6 and Figure 4-7 respectively.

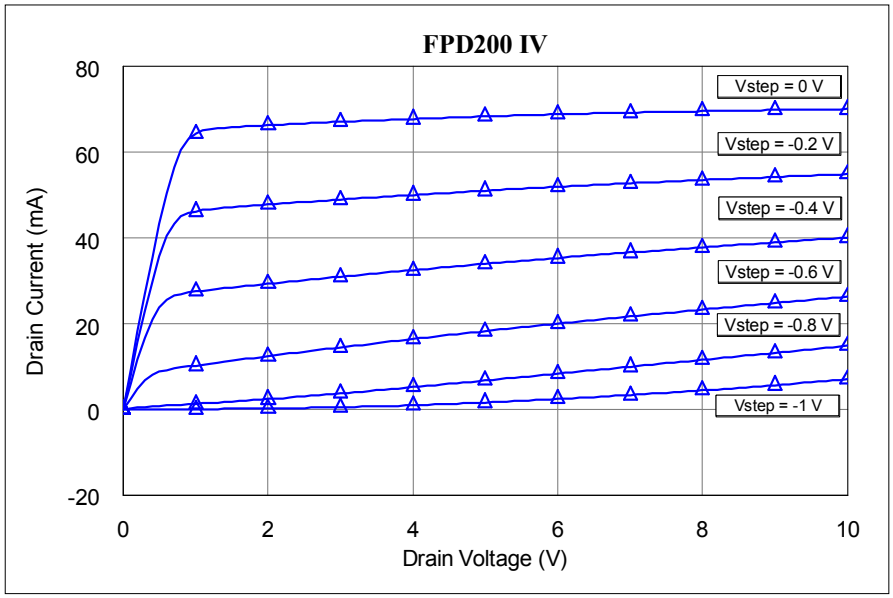


Figure 4-6: Simulated IV curves of FPD200

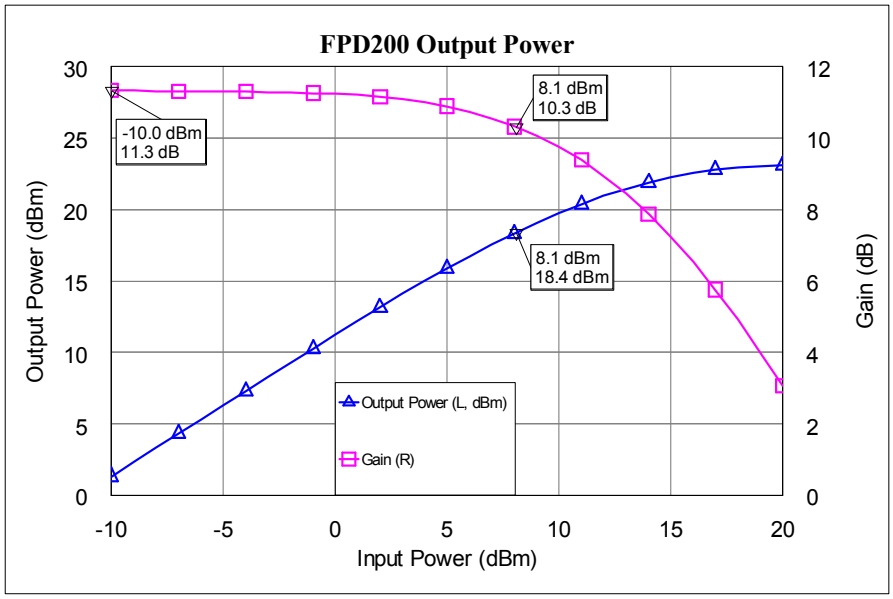


Figure 4-7: Simulated output power of FPD200 @10 GHz

4.2. Feedback Amplifier Design

The equivalent schematic of the designed feedback amplifier is given in Figure 4-8.

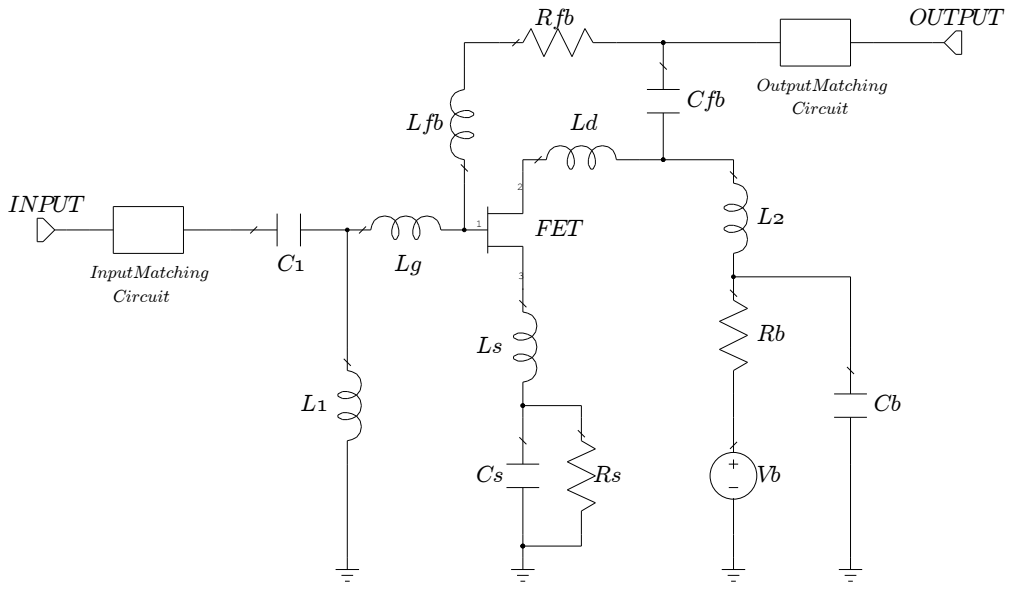


Figure 4-8: Equivalent schematic of the designed feedback amplifier

The schematic of the designed feedback amplifier is more detailed than the analyzed feedback amplifier schematic in Chapter-3. As mentioned previously, R_{fb} and L_{fb} constitute frequency dependent feedback loop. In order to eliminate feedback current, a capacitor (C_{fb}) is added between drain terminal of the FET and feedback loop. The amplifier is self-biased by shunt connected R_s and C_s elements. When current flows through drain terminal, a positive voltage occurs at the source terminal. Since, L_1 pulls gate terminal to ground, a negative gate-to-source voltage is applied. A constant biasing voltage (V_b) is applied through a biasing resistor (R_b) to drain terminal of the FET; such that, drain voltage can be controlled by R_b.

The complete high frequency model of feedback amplifier is difficult to analyze due to the complexity of FET small signal model. One of the methods followed for feedback amplifier design is selecting feedback resistor according to low-frequency equivalent model of FET as mentioned in Chapter-3. However, the selection of feedback resistor by this method is not optimum considering the high-frequency

performance of feedback amplifier. Therefore, a more systematic approach is followed for feedback amplifier design.

4.2.1. Open Loop Gain Adjustment

The ideal negative feedback amplifier model is shown in Figure 4-9.

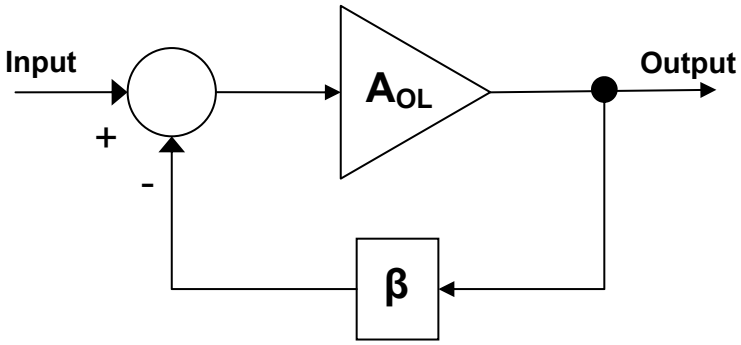


Figure 4-9: Ideal negative feedback amplifier model

Ideally, there is 180 degrees of phase difference between input and output for a microwave FET. However, in reality, insertion phase of a FET decreases with increasing frequency as in Figure 4-10.

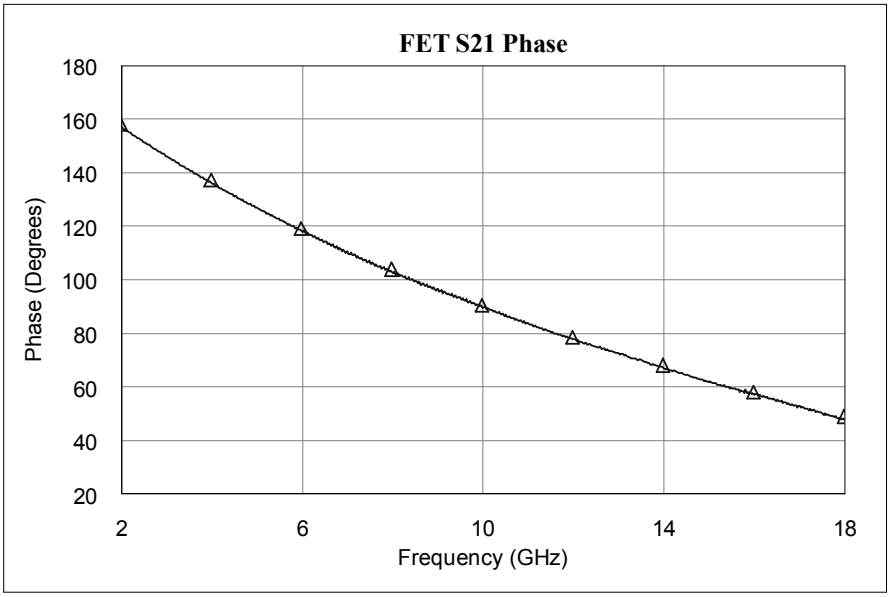


Figure 4-10: Insertion phase of a FET

Closed loop gain of an ideal negative feedback amplifier is always smaller than open loop gain. In broadband microwave feedback amplifiers, the frequency response of feedback loop is adjusted; such that, the gain of FET decreases significantly at low frequency end; whereas, the gain at high frequency end does not change. Therefore, the gain of FET is equalized to high frequency gain in a wide frequency range.

The first step for microwave feedback amplifier design is to adjust open loop gain in order to maximize the gain at high frequency end. The open loop amplifier of the feedback amplifier shown in Figure 4-8 is given in Figure 4-11.

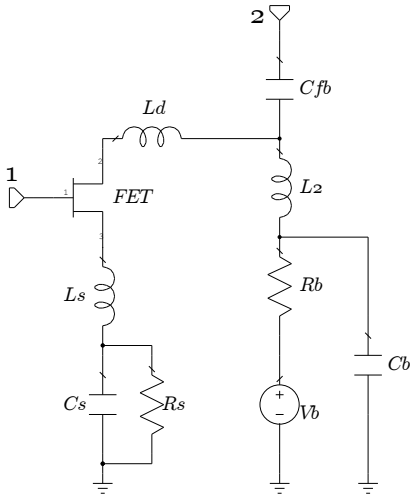


Figure 4-11: Open loop amplifier of feedback amplifier

Open loop amplifier includes self-biasing elements (R_s, C_s). According to gate bias (V_{gs}) and drain current (I_d) of FET, R_s is selected as,

$$R_s = \frac{|V_{gs}|}{I_d} \tag{4.2}$$

C_s should be selected to provide low impedance at 2 GHz, in order to provide RF grounding for source terminal of FET. The impedance of a capacitor at 2 GHz can be formulated as,

$$Z_c = \frac{79.58}{C(pF)} \tag{4.3}$$

If Z_c satisfies both $Z_c<0.1R_s$ and $Z_c<3\ \Omega$ conditions, sufficient RF grounding at 2 GHz is provided [14].

Drain biasing inductor (L_2) is chosen for resonance free operation inside 2-18 GHz band. Besides, L_2 should provide high impedance at 2 GHz. Hence, a 4-turn 14 nH air coil inductor is suitable for resonance free operation inside 2-18 GHz frequency band.

High frequency open loop gain is mostly affected by source inductance (L_s) and drain inductance (L_d). Inductance at the source terminal of FET decreases the gain at high frequencies. However, a small source inductance improves the stability of the amplifier by creating series feedback. Actually, L_s is limited by the layout of FET and bondwire connections. Drain inductance (L_d) resonates with the drain capacitance of FET; hence, output matching of FET is improved especially at high frequencies. Therefore, the available gain at 18 GHz can be increased by a suitable choice of L_d. However, selecting L_d so large leads to positive feedback at high frequencies. Then, feedback amplifier becomes prone to oscillations. Therefore, the value of L_d is selected by looking at the insertion phase of the open loop amplifier in Figure 4-11. As a rule of thumb, the value of L_d is increased up to insertion phase becomes 90 degrees at the center frequency (10 GHz) as shown in Figure 4-12.

As demonstrated in Figure 4-12, when the insertion phase is 90 degrees at 10 GHz, it is 179 degrees at 2 GHz and 42 degrees at 18 GHz. Therefore, a pure negative feedback is obtained at 2 GHz. However, positive feedback may occur at 18 GHz. Niclas, et al. [2] showed that positive feedback caused by L_d at high frequencies has a beneficial effect of elevating insertion gain above that of the open loop amplifier. Therefore, the closed loop gain at 2-18 GHz range will be equalized to the open loop gain at 18 GHz which is 8 dB as can be seen from Figure 4-12.

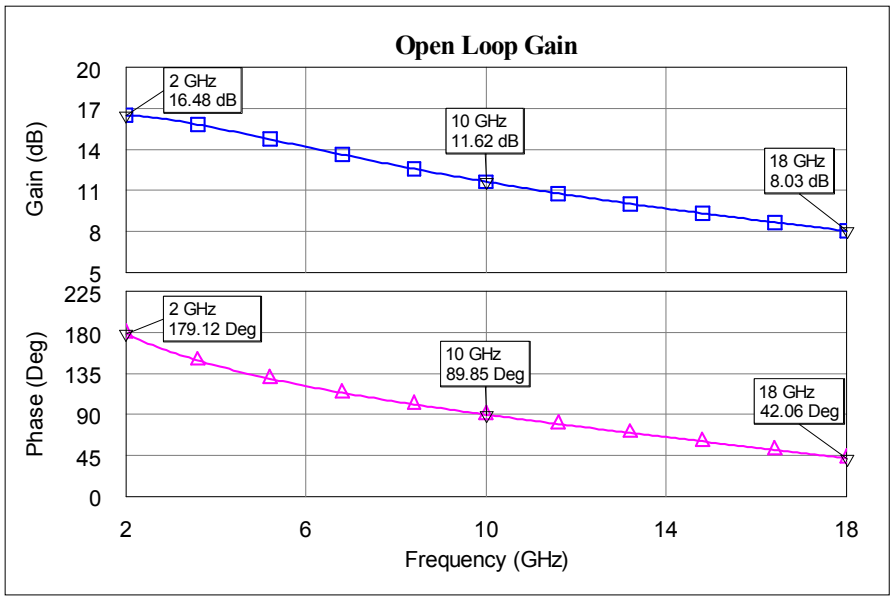


Figure 4-12: Open loop gain of the feedback amplifier for L_d=0.4 nH

4.2.2. Closed Loop Gain

After open loop gain is adjusted by L_s and L_d at 18 GHz, feedback components (R_{fb}, L_{fb}) are inserted into feedback path as shown in Figure 4-13.

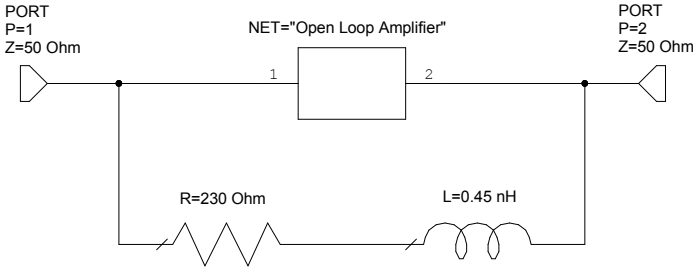


Figure 4-13: Closed loop amplifier without matching

The open loop gain at 2 GHz is reduced by a suitable choice of R_{fb}. Besides, L_{fb} should present sufficient high impedance at 18 GHz. When R_{fb} and L_{fb} are chosen as 230 Ω and 0.45 nH respectively, the response of closed loop amplifier becomes as shown in Figure 4-14.

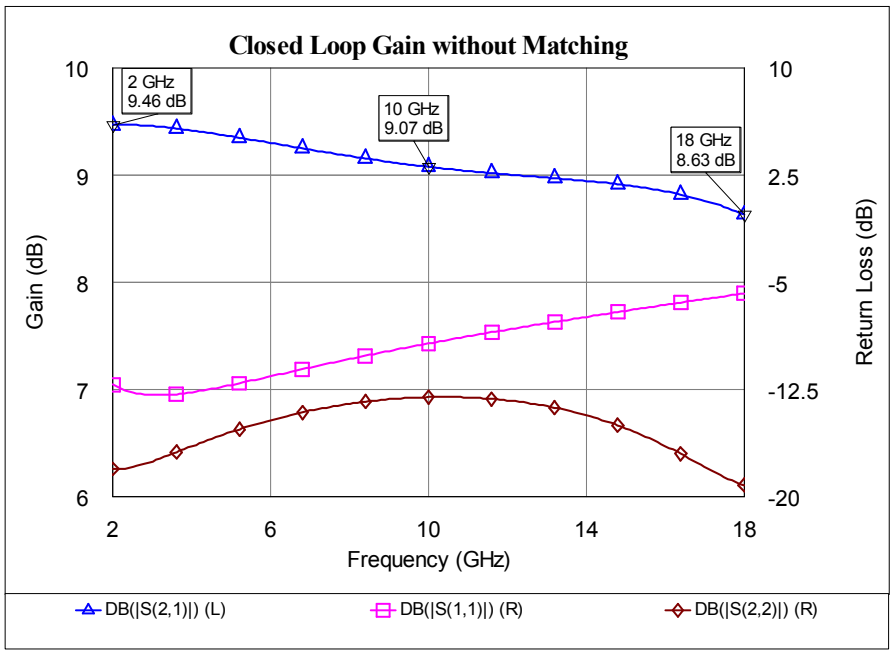


Figure 4-14: Closed loop amplifier response without matching

Figure 4-14 shows that, output stage of closed loop amplifier does not need any matching circuit. However, input return loss of the closed loop amplifier needs to be improved especially at high frequencies. After input matching circuit is inserted, the gain at high frequencies will be increased. Therefore, the unmatched closed loop gain has a small negative slope that will be compensated after input matching circuit is added. Besides, the closed loop gain is higher than the open loop gain at 18 GHz as Figure 4-12 and Figure 4-14 show because of the beneficial positive feedback occurring at 18 GHz.

4.2.3. Matching Circuit Design

The output return loss of the feedback amplifier is below -12.5 dB even without output matching circuit as shown in Figure 4-14. However, input matching circuit design is required for a satisfactory input return loss. Input matching circuit should include gate inductance of FPD200, self-biasing inductance and input dc-block capacitance. A simple single stub matching circuit is enough to bring input return

loss below -10 dB over 2-18 GHz frequency range as illustrated in Figure 4-15 and Figure 4-16.

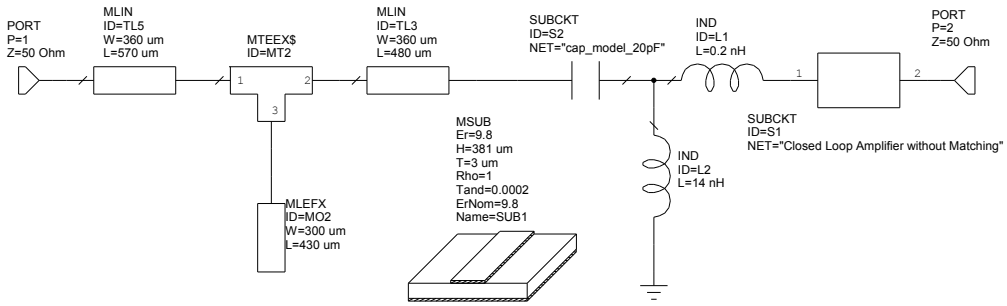


Figure 4-15: Closed loop amplifier with input matching circuit

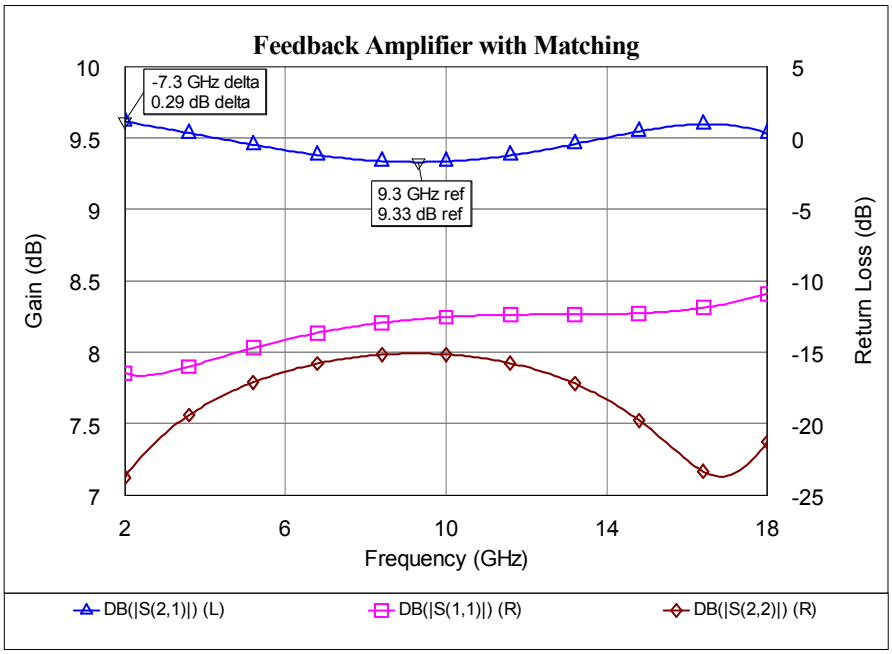


Figure 4-16: Closed loop amplifier response with matching

After inserting input matching circuit, high frequency gain of the feedback amplifier is also increased; such that, the gain over 2-18 GHz frequency range becomes approximately 9.5 dB with a ripple of 0.29 dB.

In Figure 4-17, the Rollet's stability factors (K) of both open loop and closed loop amplifiers are demonstrated. The closed loop amplifier presents unconditionally stable operation even outside the operating frequency range.

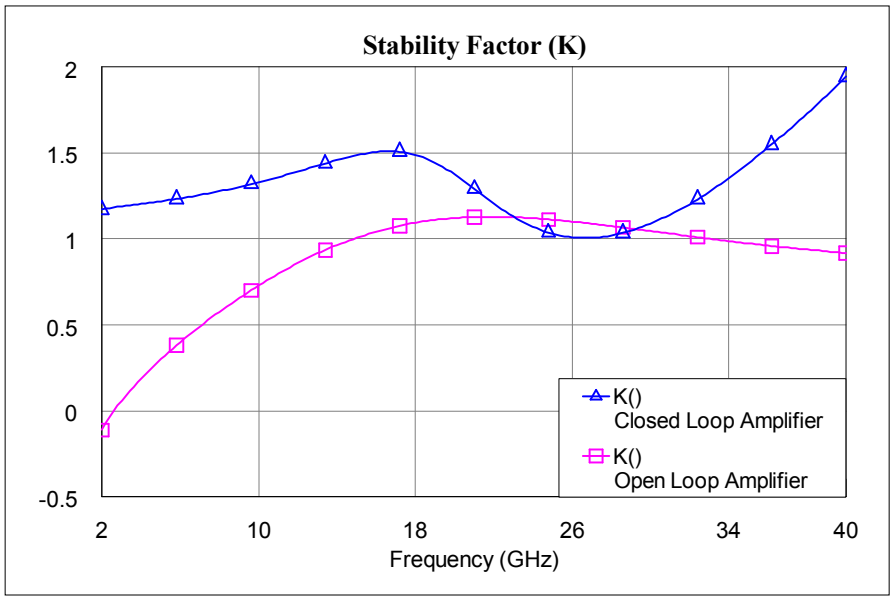
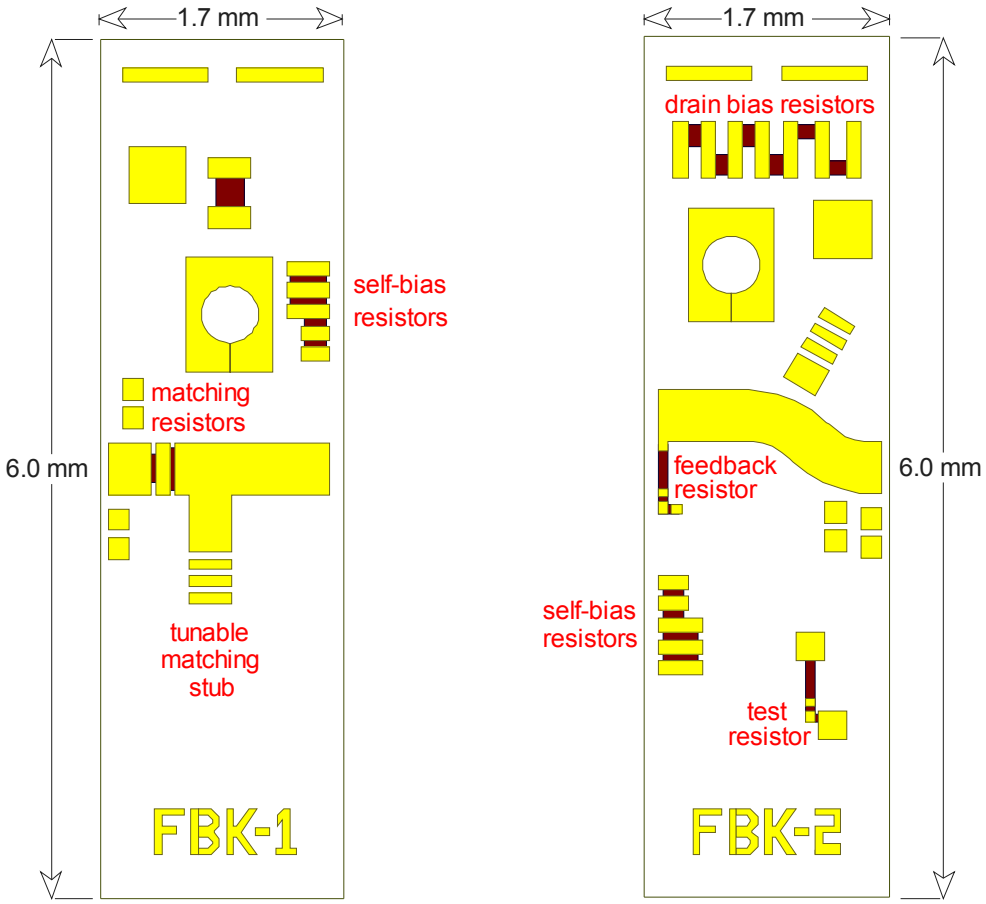


Figure 4-17: Stability factors of open loop and closed loop amplifiers

4.2.4. Feedback Amplifier Layout and EM Simulations

According to feedback amplifier schematic given in Figure 4-8, input and output circuits are designed on 15 mil Alumina substrate. The layouts of input and output circuits are created such that the performance of feedback amplifier can be tunable as shown in Figure 4-18. Tunable bising resistors allow biasing of feedback amplifier at different gate and drain supply voltages. Feedback resistor is also made changable in order to compensate for the production tolerance on thin film resistors. Besides, a test resistor is added to measure the resistance of feedback resistor after production.



(a) (b)

Figure 4-18: Input (a) and output (b) circuits of feedback amplifier

The assembly drawing which shows the integration of circuit elements with input and output thin film circuits is given in Figure 4-19. The drawing includes other versions of the created input and output thin film circuits with added CPW-microstrip test points. Thanks to these test points, the performance of feedback amplifier can be measured in a probe station. The input matching resistors can be shorted by multiple bondwires or ribbons. Since, there are two matching resistors of 5 ohms and 10 ohms, it is possible to obtain 15 ohms series resistance in total. The function of these series input resistors other than matching is improving the stability of the amplifier. The disadvantage is the reduction in the gain of the amplifier.

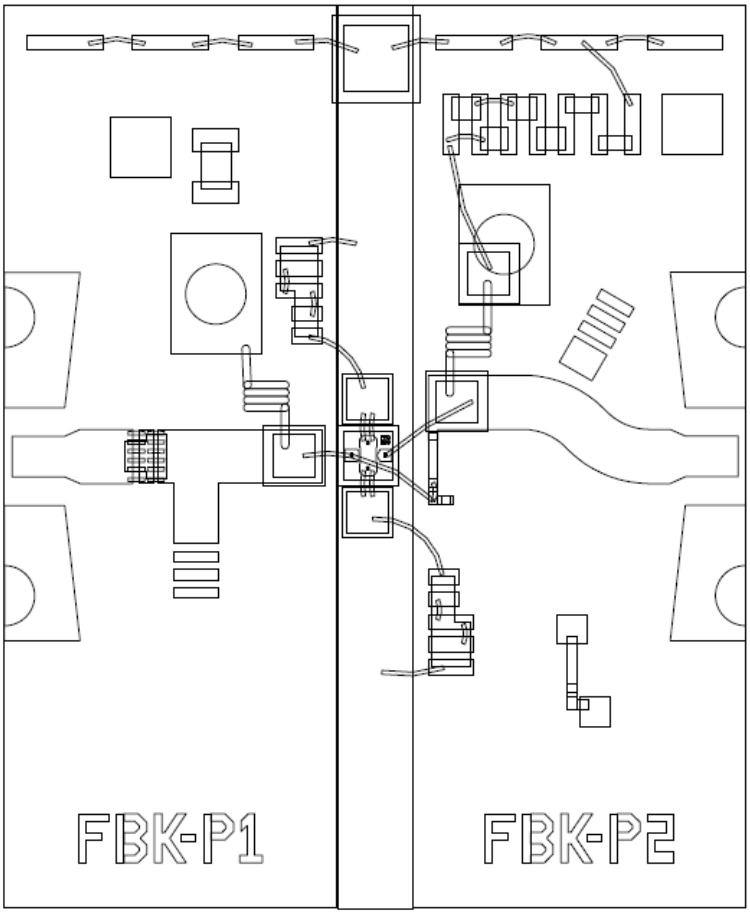


Figure 4-19: Assembly drawing of feedback amplifier with input and output test points

The important point in simulating the performance of designed feedback amplifier is modeling the bondwires connected to transistor chip. The height of thin film circuits is 15 mils. However, the thicknesses of FPD200 chip and capacitors are 3 mils and 4 mils respectively. Therefore, FPD200 chip is elevated nearly 15 mils; such that, the length of bondwire connections from FPD200 chip to input and output capacitors is minimized.

Bondwire connections of FPD200 chip are modeled in HFSS^{TM} in order to represent the real situation accurately. The HFSS^{TM} simulation setup created for feedback bondwire stretching from gate pad of FPD200 to feedback resistor is illustrated in Figure 4-20. The shape of bondwire is selected as the JEDEC 5-point standard. Moreover, bondwire loop was created such that it would fit best to the real situation.

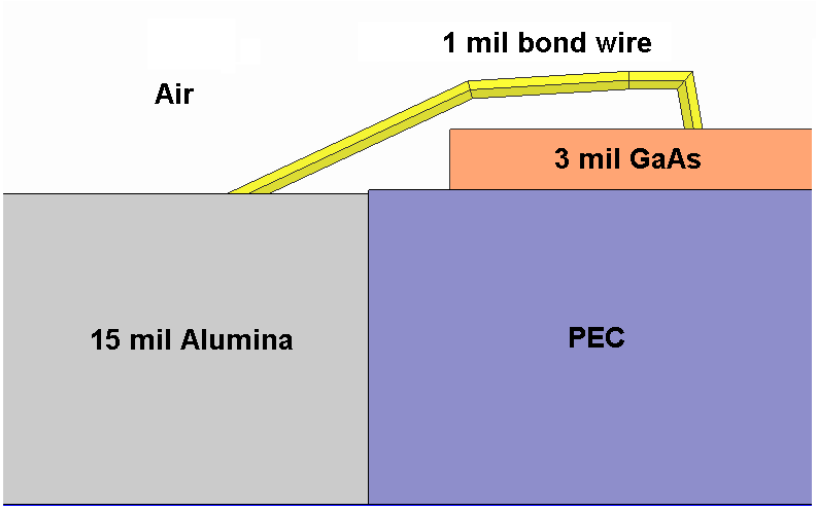


Figure 4-20: HFSS simulation setup for feedback bondwire (L_{fb})

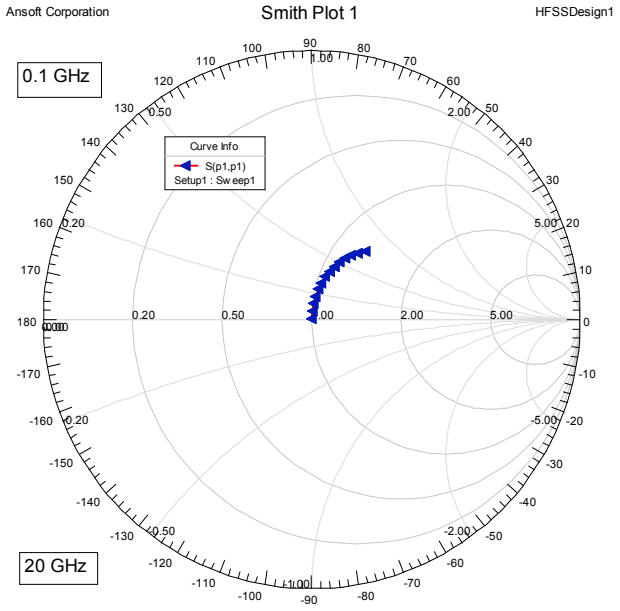


Figure 4-21: Simulation result of feedback bondwire

The HFSS™ simulation of feedback bondwire deviates from an ideal inductor characteristic as shown in Figure 4-21. A shunt capacitive effect, which is consistent to bondwire model, can be seen from the figure. The actual model of a bondwire inductor is not only composed of a lumped inductor but also additional shunt capacitors and series resistor as shown in Figure 4-22 [33].

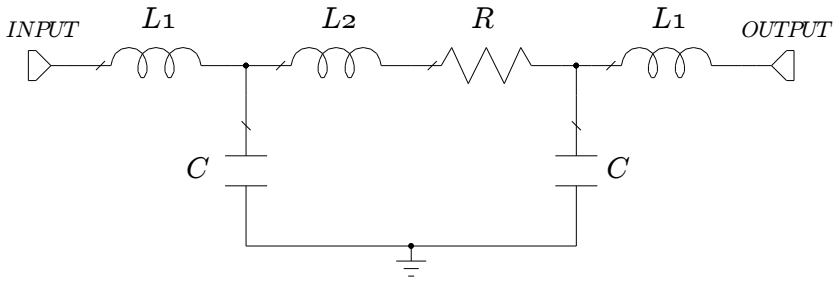


Figure 4-22: Simple lumped element circuit model for bondwire

The bondwire model includes an ideal inductor L_2 in series with an ideal resistor R due to wire inductance and loss respectively. The shunt capacitor C at the input and output represents the capacitance between bonding pad to ground. Moreover, the series inductors at the input and output represent the end inductances.

EM simulations of input and output microstrip lines, input matching stub and thin film feedback resistor are carried out in Microwave Office. Then, the EM simulated input and output circuits are integrated with the HFSS simulated gate, drain and feedback bondwires as shown in Figure 4-23.

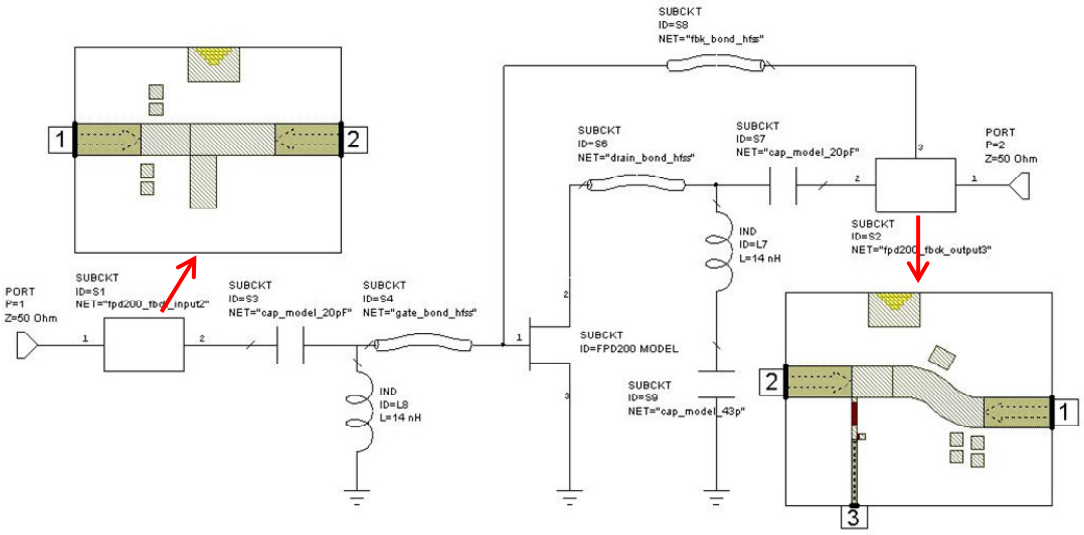


Figure 4-23: Feedback amplifier circuit with input and output EM structures

Simulation results of the feedback amplifier circuit in Figure 4-23 are obtained as given in Figure 4-24. The predicted gain of the feedback amplifier is approximately 9 dB with 0.5 dB ripple over 2-18 GHz frequency range. Besides, input and output return losses inside 2-18 GHz frequency range are expected to be below -10 dB as shown in Figure 4-24

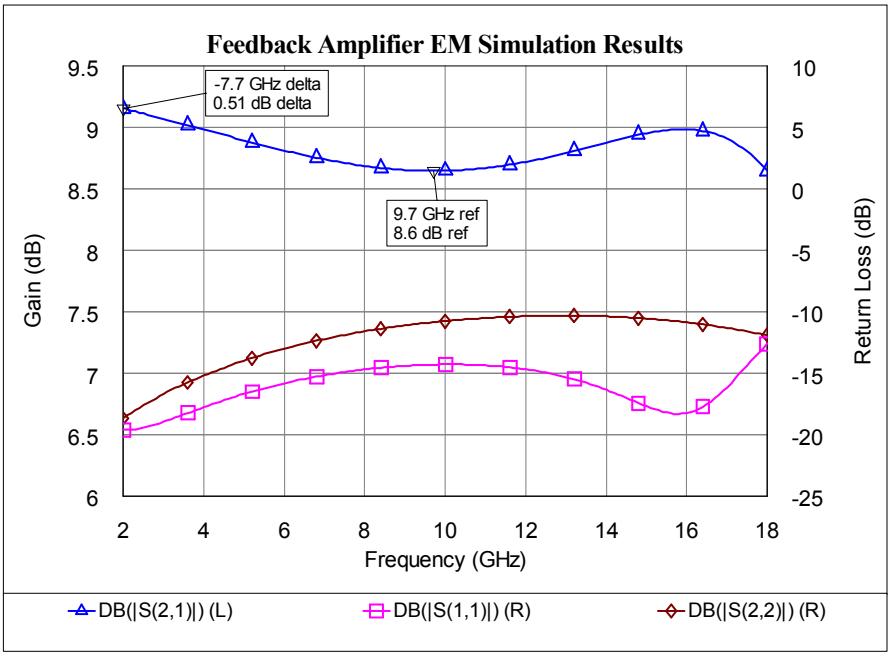


Figure 4-24: EM simulation results of feedback amplifier

4.3. Distributed Amplifier Design

Distributed amplifiers are usually multistage in order to obtain high gains. MMIC type multistage distributed amplifiers are widespread in literature. However, distributed amplifiers with number of stages greater than 3, are not suitable for hybrid MIC production. Therefore, 2-stage distributed amplifier is chosen as a cascaded gain stage in limiting amplifier design in order to ease fabrication process.

4.3.1. Ideal 2-Stage Distributed Amplifier

A common approach for designing distributed amplifier is equalizing gate and drain capacitances of FET by inserting an extra shunt capacitance to drain, as mentioned in Chapter-3. Besides, gate and drain inductances are made equal (L_g=L_d) for in-phase addition of the amplified signals from each FET. Then, the design equations of distributed amplifier are as follows.

$$Z_{0g} = Z_{od} = \sqrt{\frac{L_g}{C_{gs}}} = 50\Omega \tag{4.4}$$

$$\omega_{cg} = \omega_{cd} = \sqrt{\frac{2}{L_g C_{gs}}} = \omega_c \tag{4.5}$$

By using (4.4) and (4.5), gate inductance and cut-off frequency can be expressed in terms of C_{gs} as follows;

$$L_g(nH) = 2.5 * C_{gs}(pF) \tag{4.6}$$

$$f_c(GHz) = \frac{6.37}{C_{gs}(pF)} \tag{4.7}$$

In Section 4.1.2, gate-to-source capacitance, C_{gs}, of FPD200 is extracted as 0.37 pF and drain-to-source capacitance, C_{ds}, is extracted as 0.042 pF. Therefore, a 0.33 pF shunt capacitance should be added to drain terminals of FETs in order to equalize gate and drain capacitances. Moreover, L_g is calculated as 0.925 nH and f_c is found as 17.2 GHz for these element values.

The low-frequency gain of an n-stage distributed amplifier can also be calculated by the following formula.

$$G \cong \frac{g_m{}^2 n^2 Z_0{}^2}{4} \tag{4.8}$$

Hence, the low-frequency gain of a 2-stage distributed amplifier for g_m=0.106 and Z_0=50 can be calculated as 14.49 dB.

The simulated schematic of 2-stage distributed amplifier with extra drain capacitances is shown in Figure 4-25. The model used for FPD200 transistor in the following schematic is the ideal FET model which includes only C_{gs} and C_{ds}.

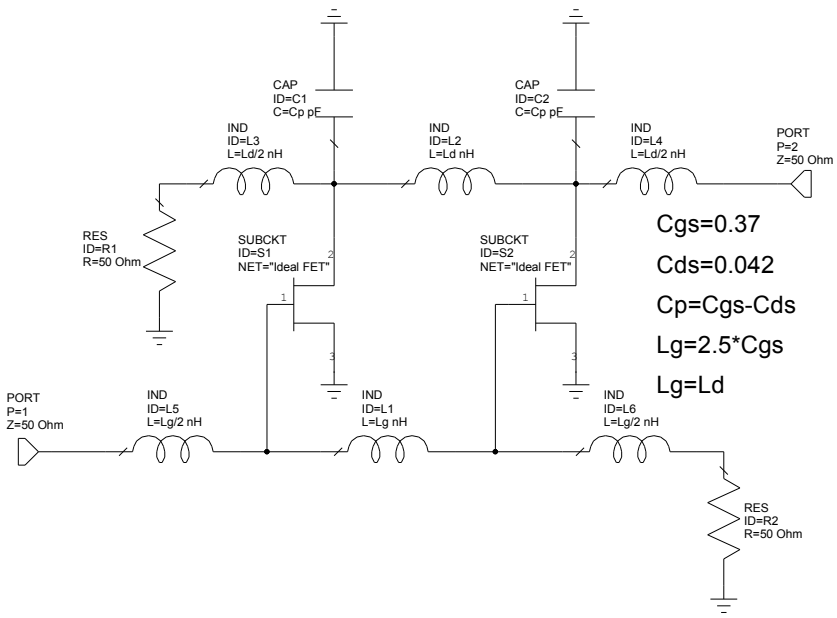


Figure 4-25: Schematic of ideal 2-stage FPD200 distributed amplifier

Simulation results of the above 2-stage distributed amplifier are illustrated in Figure 4-26. The amplifier provides nearly 14.5 dB gain at low frequencies as predicted from (4.8). Moreover, the gain of the amplifier drops nearly 1 dB at the calculated cut-off frequency, 17.2 GHz.

When the complete small signal model of FPD200 transistor is used in the schematic given in Figure 4-25, the response of 2-stage distributed amplifier will be as demonstrated in Figure 4-27.

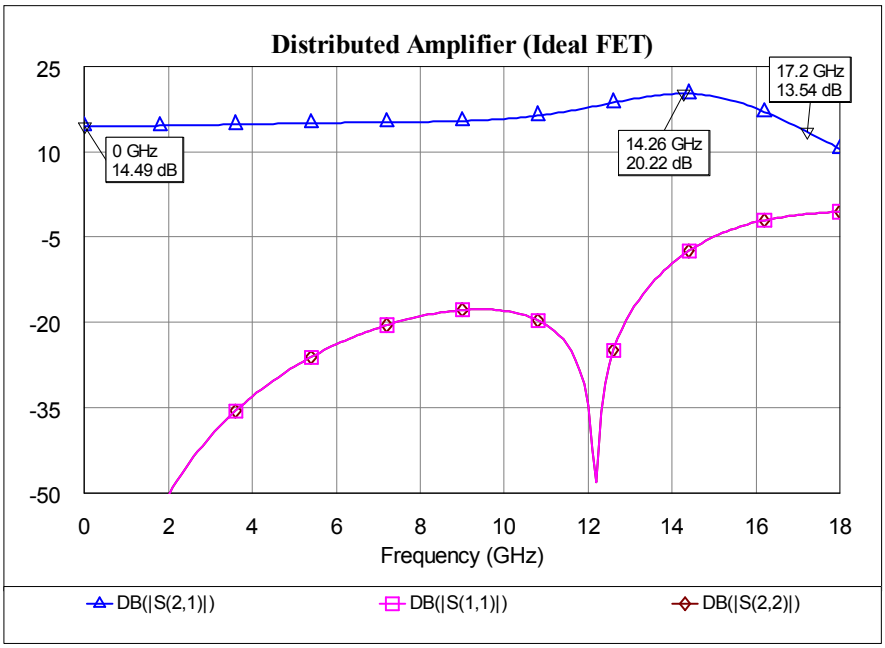


Figure 4-26: Simulation results of 2-stage distributed amplifier with the ideal FPD200 model

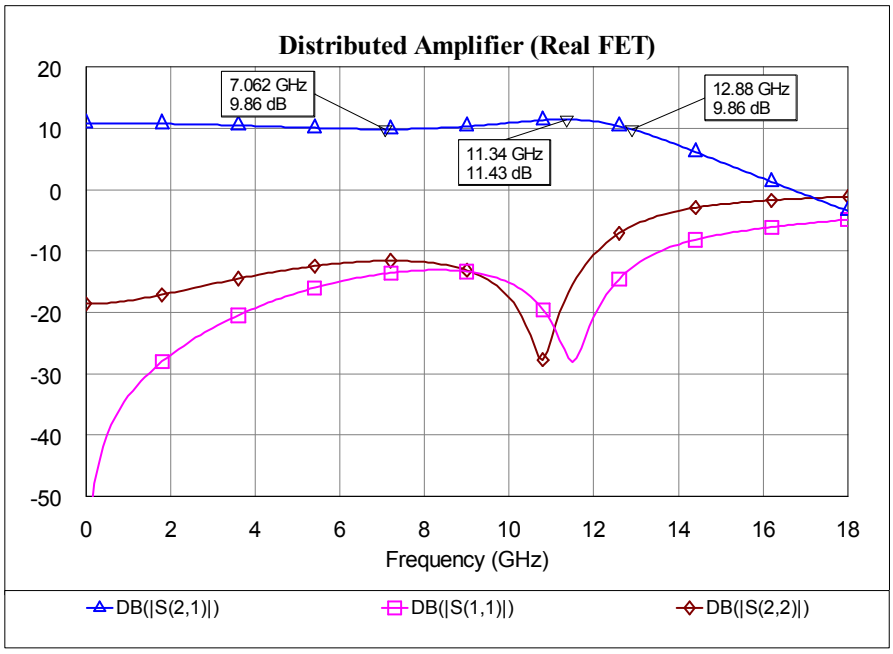


Figure 4-27: Simulation results of 2-stage distributed amplifier with the complete FPD200 model

Figure 4-26 shows that ideal FET model is not sufficient for predicting the real amplifier response. When the complete FPD200 model is inserted in the amplifier schematic, cut-off frequency of the amplifier is lowered as can be seen from Figure 4-27. Moreover, by inserting extra shunt capacitance to drain of FPD200, the cut-off frequency of drain line is decreased. Therefore, 2-stage amplifier designed by equalizing gate and drain capacitances of FPD200 is not capable of covering 2-18 GHz frequency range.

4.3.2. Modified 2-Stage Distributed Amplifier

Inserting shunt capacitance to drain terminal of FET lowers the cut-off frequency of drain line as well as the bandwidth of distributed amplifier. One method of widening the bandwidth of distributed amplifier is inserting series capacitor to gate terminal of FET such that the input capacitance of FET is decreased and the cut-off frequency of gate line is increased. However, less gain can be obtained from distributed amplifier designed by this method.

Termination resistors are used for absorbing unwanted reflections in distributed amplifiers. Gate termination resistor (R_g) terminates the propagating input signal at the end of transistor stages. Drain termination resistor (R_d) terminates the reflected signals due to mismatch at the output of distributed amplifier. Moreover, the amplified signal by the first transistor is splitted into two paths at the drain terminal of the first transistor. Some portion of the amplified signal is absorbed in R_d and the remaining portion propagates through the drain line. Therefore, it is possible to increase the bandwidth of distributed amplifier by reducing the power lost in R_d at high frequencies. For this purpose, the schematic of distributed amplifier is modified as shown in Figure 4-28. A simple LC low-pass network is inserted before R_d such that the amplified signal by the first transistor sees a high impedance from the termination arm at high frequencies. Hence, a larger portion of the amplified signal by the first transistor propagates through drain line and is summed up with the amplified signal by the second transistor at high frequencies.

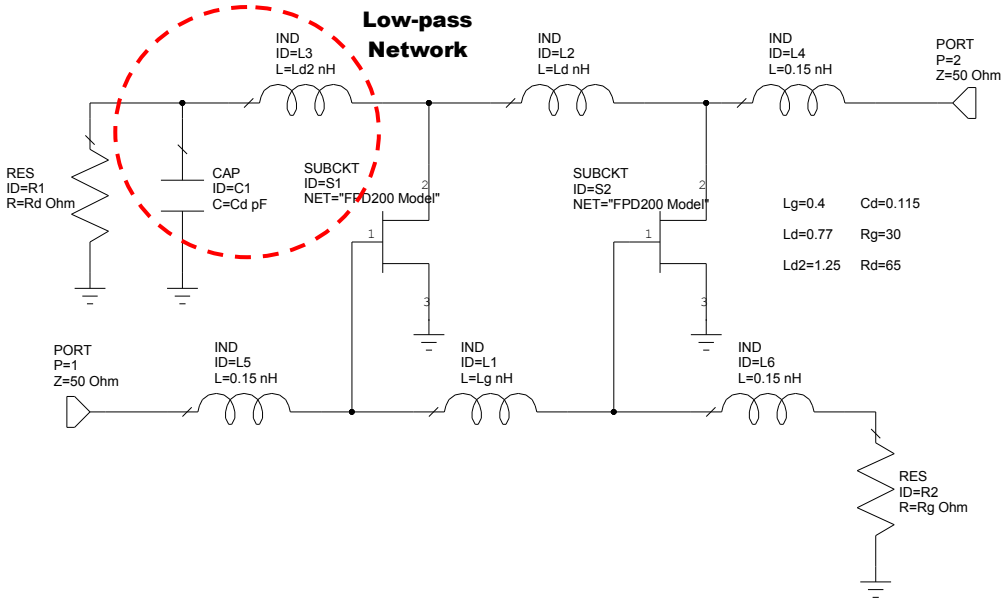


Figure 4-28: Schematic of the modified 2-stage distributed amplifier

After optimizing the elements given in Figure 4-28, it is possible to achieve a gain characteristic with a perfect flatness as shown in Figure 4-29. It can also be seen from Figure 4-28 that termination resistors are different from 50 ohms.

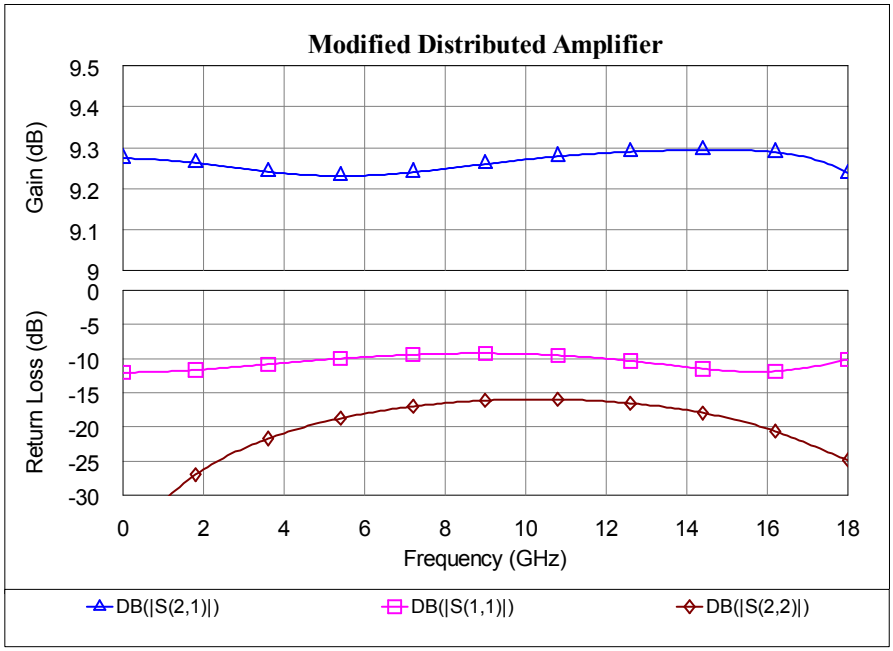


Figure 4-29: Simulation results of the modified 2-stage distributed amplifier

The modified 2-stage distributed amplifier presents unconditionally stable operation up to 40 GHz as demonstrated in Figure 4-30.

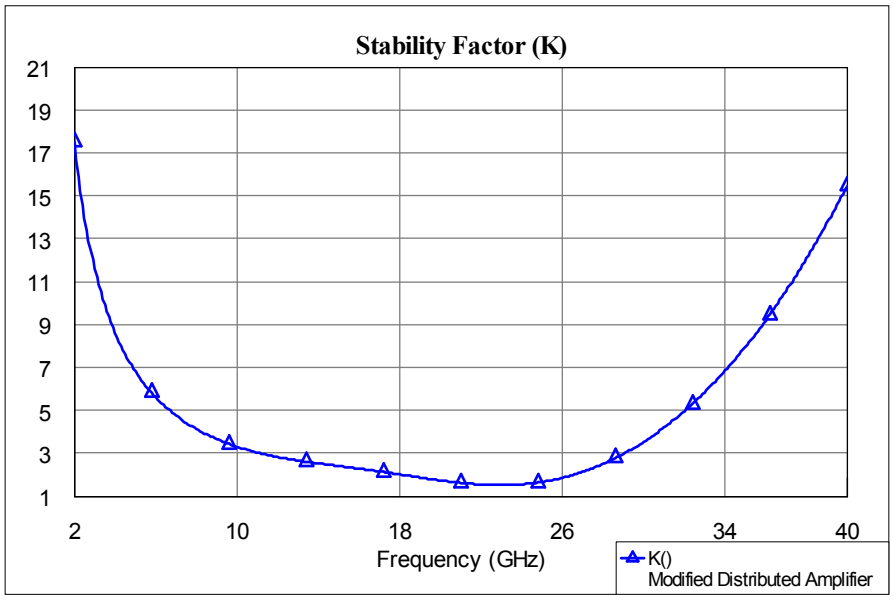
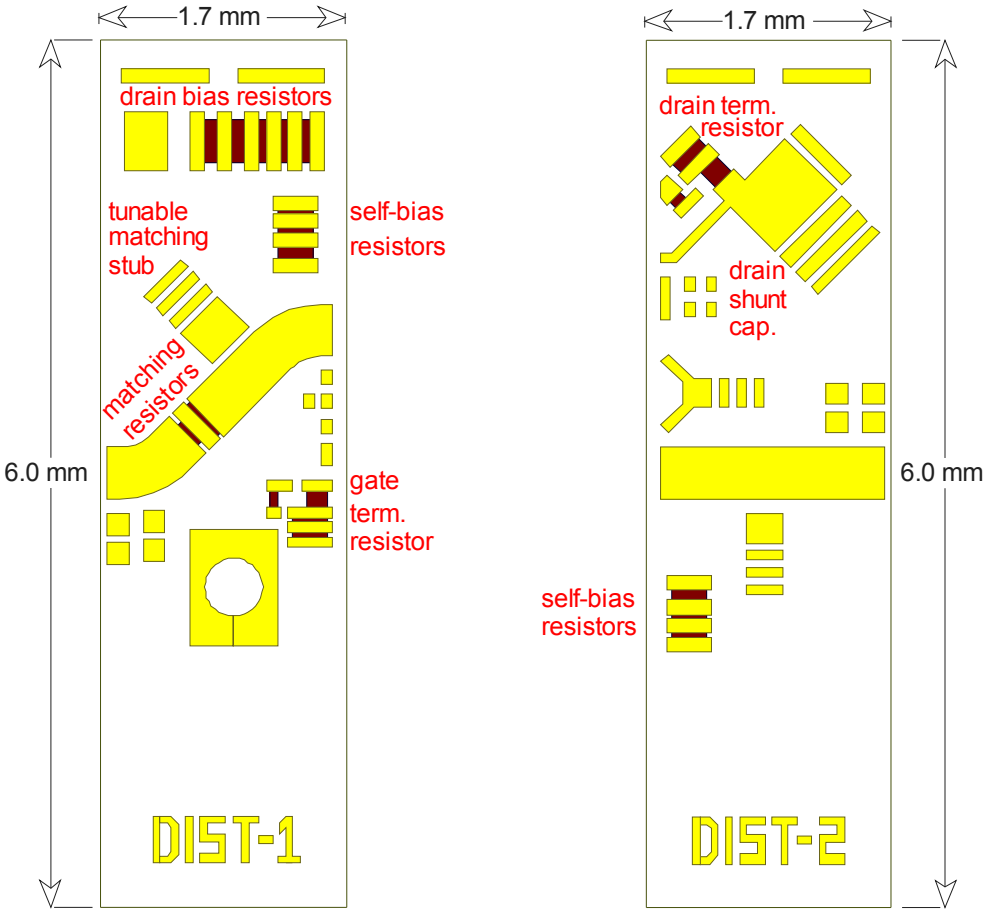


Figure 4-30: Stability factor of the modified 2-stage distributed amplifier

4.3.3. 2-Stage Distributed Amplifier Layout and EM Simulations

In order to provide consistency with feedback amplifier design, input and output circuits of 2-stage distributed amplifier are also designed on 15 mils thick alumina ceramic as shown in Figure 4-31. Moreover, the circuits are designed in the same dimensions with the feedback amplifier circuits such that the two amplifiers can be cascaded interchangeably for a multistage design. Besides, the layouts of input and output circuits are created such that the performance of distributed amplifier can be tuned similar to feedback amplifier design. The main function of tuning is to compensate the variations between modeled and realized bondwires.



(a) (b)

Figure 4-31: Input (a) and output (b) circuits of distributed amplifier

The drawing, which shows the connections of FPD200 chips and other components to thin film circuits, is illustrated in Figure 4-32. Input and output circuits of distributed amplifier are also designed with embedded coplanar test points such that the performance of distributed amplifier can be measured in a probe station. Moreover, the two FPD200 chips and source capacitors are mounted on a 15 mil thick mechanical post such that the lengths of input, output and source bondwires is minimized.

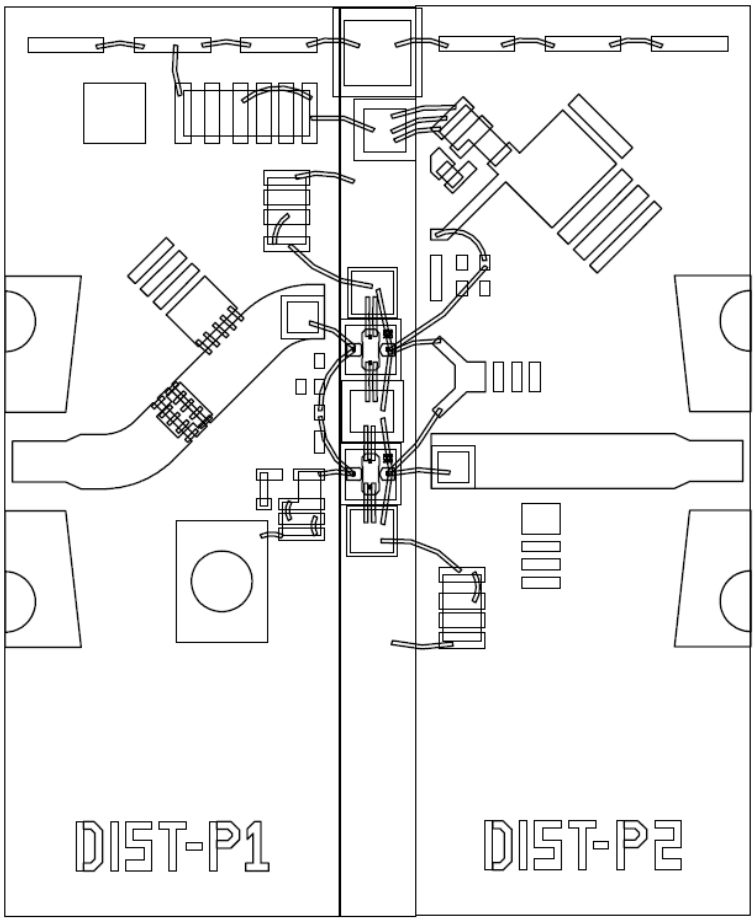


Figure 4-32: Assembly drawing of distributed amplifier with input and output test points

Distributed amplifier design includes several bondwire connections as demonstrated in Figure 4-32. Critical bondwire connections, especially FPD200 interconnects, are simulated in HFSS™ as in the case of feedback amplifier design. Moreover, electromagnetic simulations of microstrip lines, tuning stubs and thin film resistors are carried out using Microwave Office.

Input and output circuits are splitted into small independent circuits during EM simulation. Then, the created EM structures for these circuits are combined with the simulated bondwires and other components to constitute the complete 2-stage distributed amplifier structure as shown in Figure 4-33. The gain and return loss performance of the created amplifier schematic is illustrated in Figure 4-34.

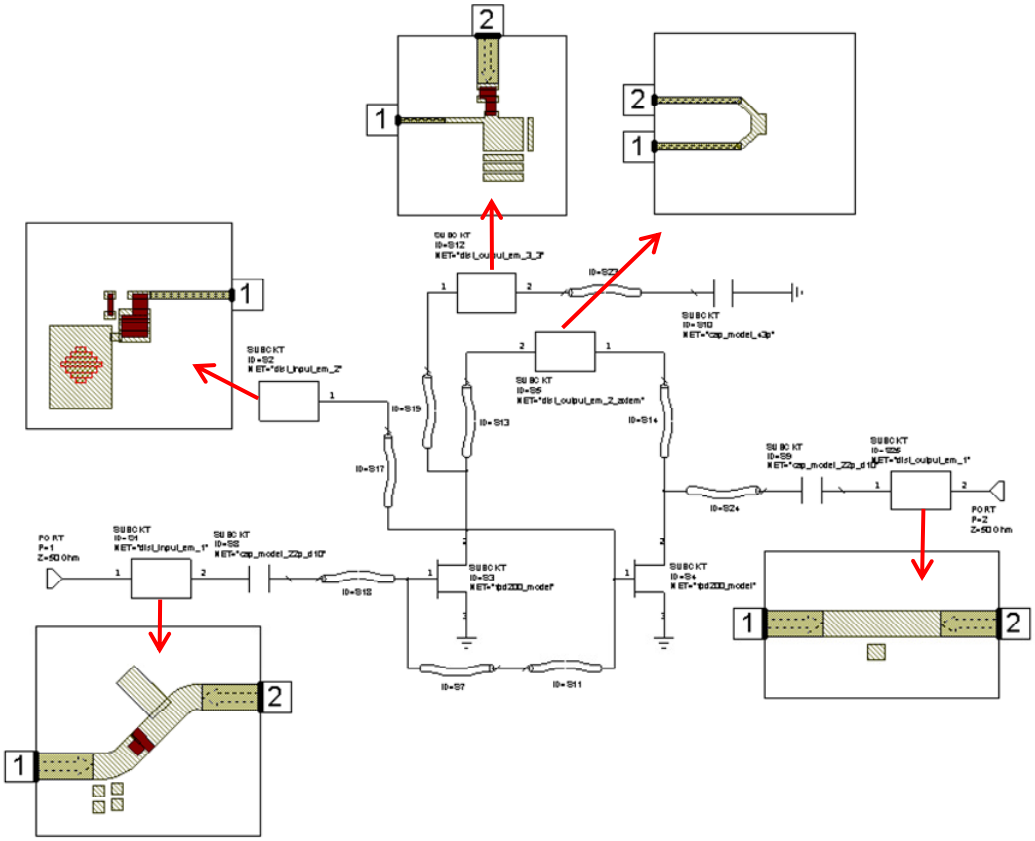


Figure 4-33: 2-Stage distributed amplifier circuit with the simulated EM structures

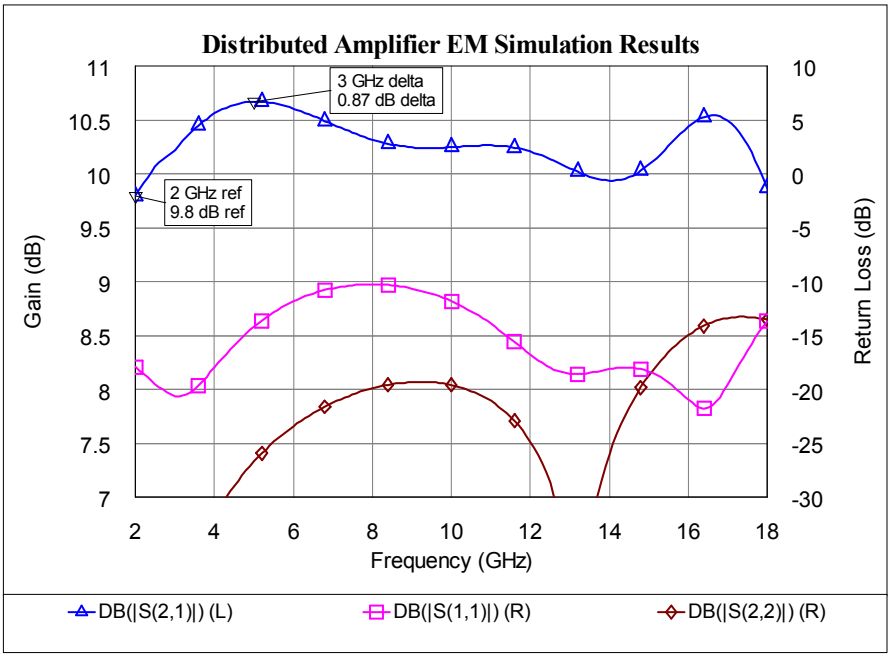


Figure 4-34: EM simulation results of distributed amplifier

The predicted gain level from 2-stage distributed amplifier design is nearly 10.25 dB with +/-0.45 dB flatness inside 2-18 GHz frequency range. Besides, both input and output return losses are below -10 dB.

4.4. 3-Stage Cascaded Amplifier Design

In order to obtain higher small signal gains, the designed amplifiers would be cascaded. It is possible to obtain a minimum of 25 dB small signal gain by connecting three amplifier stages in cascade. Then, a number of designed cascaded amplifiers would be cascaded to constitute a limiting amplifier capable of providing saturated output power for -50 dBm input signal level. Hence, the required number of cascaded stages in the final limiting amplifier would be chosen according to minimum input signal level and saturated output power level.

4.4.1. Selection of Single Stage Amplifiers to be Cascaded

It was aimed to design a 3-stage cascaded amplifier with minimum gain flatness and acceptable input and output return losses. Single stage amplifier designs show that feedback amplifier provides flatter gain response as compared to distributed amplifier. Hence, one might think that cascading three feedback amplifiers would result in the flattest gain response. Three cascaded feedback amplifiers result in 26.5 +/- 1.1 dB gain level as shown in Figure 4-35. The simulated gain ripple is greater than that is expected from single stage feedback amplifier results. Moreover, the return loss characteristics of single stage feedback amplifier are not preserved.

When three 2-stage distributed amplifiers are cascaded, the predicted gain level will be 30.65 +/- 1.25 dB as demonstrated in Figure 4-36. It was obtained 0.85 dB gain ripple from a single distributed amplifier. Therefore, the gain ripples of each of three distributed amplifiers are nearly summed up when connected in cascade. Moreover, the return loss characteristics of cascaded amplifier are approximately the same with

that of single distributed amplifier different from cascaded feedback amplifier case. Besides, cascaded distributed amplifier provides 4 dB larger gain than cascaded feedback amplifier.

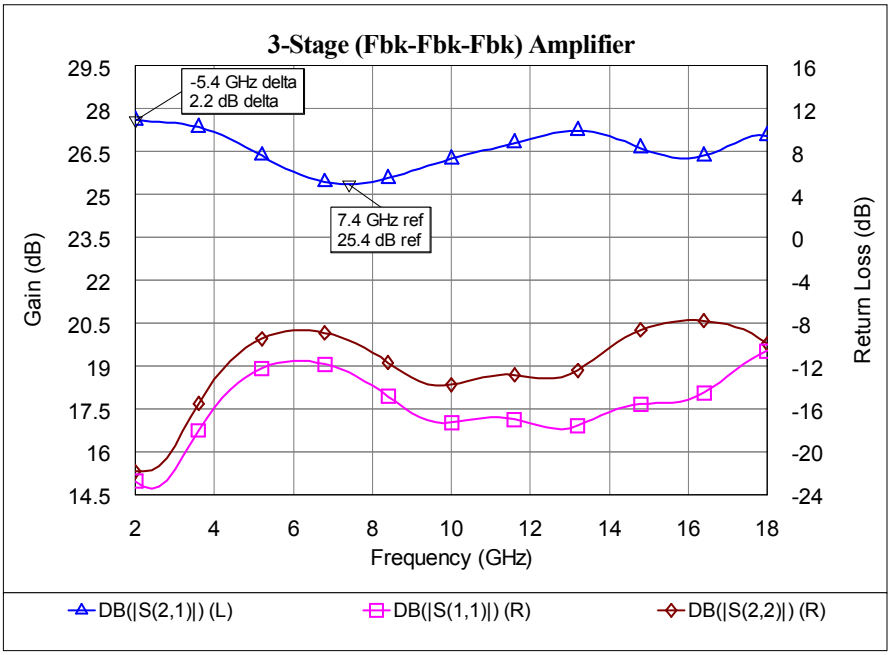


Figure 4-35: The response of three feedback amplifiers in cascade

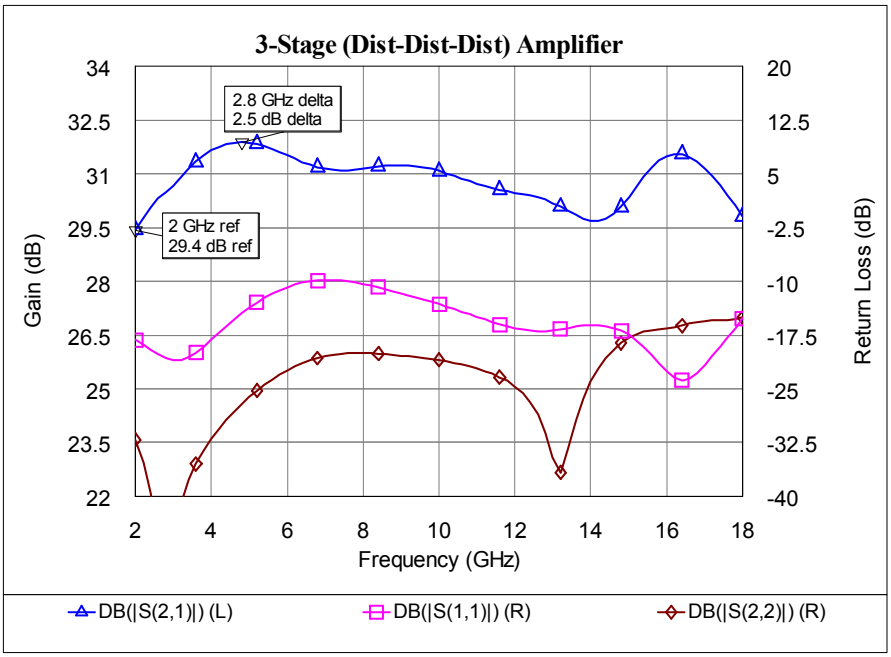


Figure 4-36: The response of three distributed amplifiers in cascade

A significant difference between feedback and distributed amplifiers is the isolation of the amplifiers as shown in Figure 4-37.

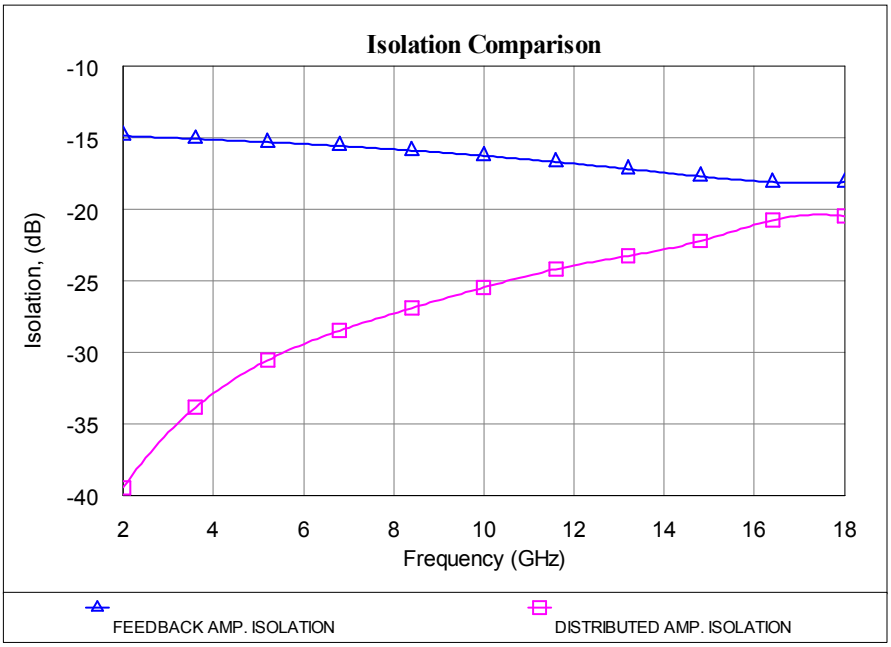


Figure 4-37: Comparison of isolation characteristics of feedback and distributed amplifiers

Since there is a feedback loop from output to input for a feedback amplifier, the isolation of the feedback amplifier is poor even at low frequencies. However, low frequency isolation of distributed amplifier is much better than feedback amplifier. Moreover, the isolation of feedback amplifier is always worse than that of distributed amplifier over 2-18 GHz frequency interval. Because of this difference in isolation characteristics of feedback and distributed amplifiers, these two amplifiers present different features when connected in cascade.

It can be seen from Figure 4-38 how the isolation of the first stage amplifier affects the input return loss of the cascaded amplifier. In a typical scenario, the gain, isolation and input return loss of the first stage amplifier are 10 dB, -10 dB and -10 dB respectively. The input signal of 0 dBm level is amplified to 10 dBm by the first amplifier. Then, the amplified signal is reflected by the second amplifier. The

reflected signal level will be 0 dBm because of the -10 dB input return loss of the second amplifier. Finally, the reflected 0 dBm signal leaks to the input of the first amplifier as -10 dBm due to the isolation of the first amplifier. If the first reflected -10 dBm signal and the second reflected -10 dBm signal is added in phase, the total reflected signal level from the input of cascaded amplifier will be -4 dBm. Therefore, the input return loss of the cascaded amplifier becomes -4 dB; even though, the input return loss of the first stage amplifier is -10 dB.

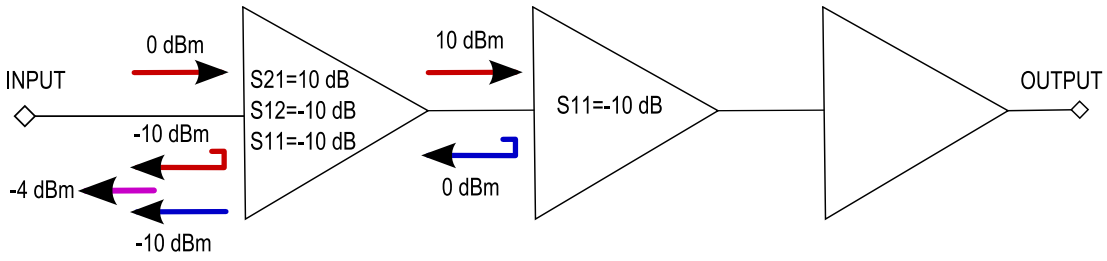


Figure 4-38: A sample 3-stage cascaded amplifier scenario

The resulting input return losses of the cascaded amplifier shown in Figure 4-38 according to different isolation levels of the first amplifier is tabulated in Table 4-3. The numbers in the following table refers to the worst case return loss values assuming in phase addition of the reflected signals.

Table 4-3: Effect of isolation of 1st stage amplifier to return loss of cascaded amplifier

S_{12} of the 1st stage	S_{11} of the 1st stage	S_{11} of the cascaded amp.
-40 dB	-10 dB	-9.73 dB
-25 dB	-10 dB	-8.58 dB
-15 dB	-10 dB	-6.12 dB
-10 dB	-10 dB	-4 dB

A similar situation exists for the output return loss of the cascaded amplifier. In other words, the output return loss of the cascaded amplifier will be nearly the same with that of the last amplifier, if the last amplifier provides adequate isolation from output to input.

Since distributed amplifier provides better isolation characteristics compared to feedback amplifier, input and output stages of 3-stage cascaded amplifier were selected as distributed type. Hence, the deviation of input and output return losses of cascaded amplifier from that of single stage distributed amplifier design would be minimized. Feedback amplifier stage was inserted between two distributed amplifiers because of the flatter gain of feedback amplifier. Then, the response of the new 3-stage cascaded amplifier was predicted as illustrated in Figure 4-39.

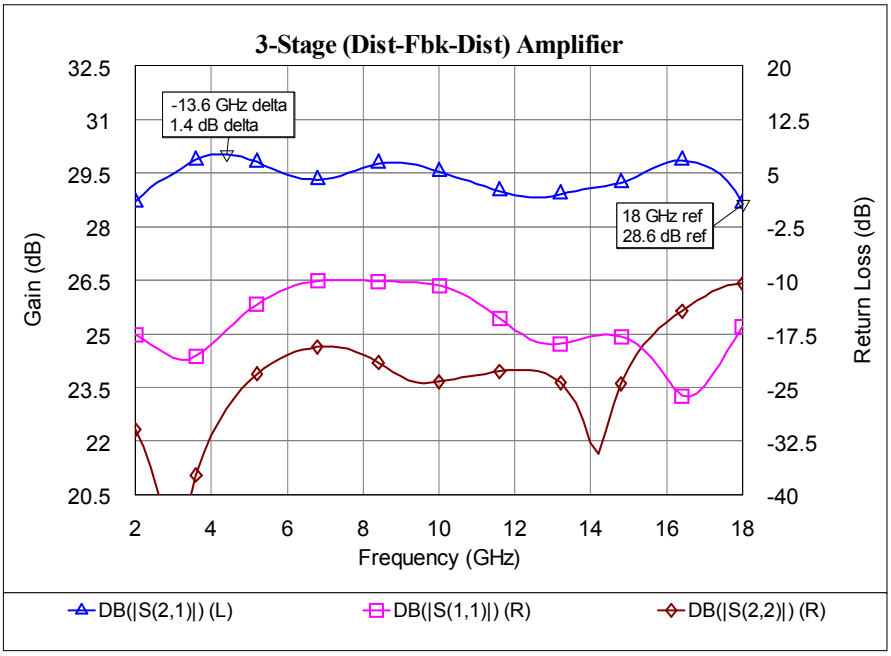


Figure 4-39: Simulation results of the 3-stage amplifier in distributed-feedback-distributed cascaded combination

The 3-stage amplifier with this new combination provides 29.3 dB +/- 0.7 dB gain and at most -10 dB input and output return losses. Moreover, the shapes of input and

output return losses of the cascaded amplifier are nearly the same with that of single stage distributed amplifier.

A 4-stage amplifier can also be designed by following a similar procedure. The first and the last stage amplifiers were selected as distributed type. Then, two cascade connected feedback amplifiers were inserted between input and output stages. The simulated response of the designed 4-stage amplifier is shown in Figure 4-40.

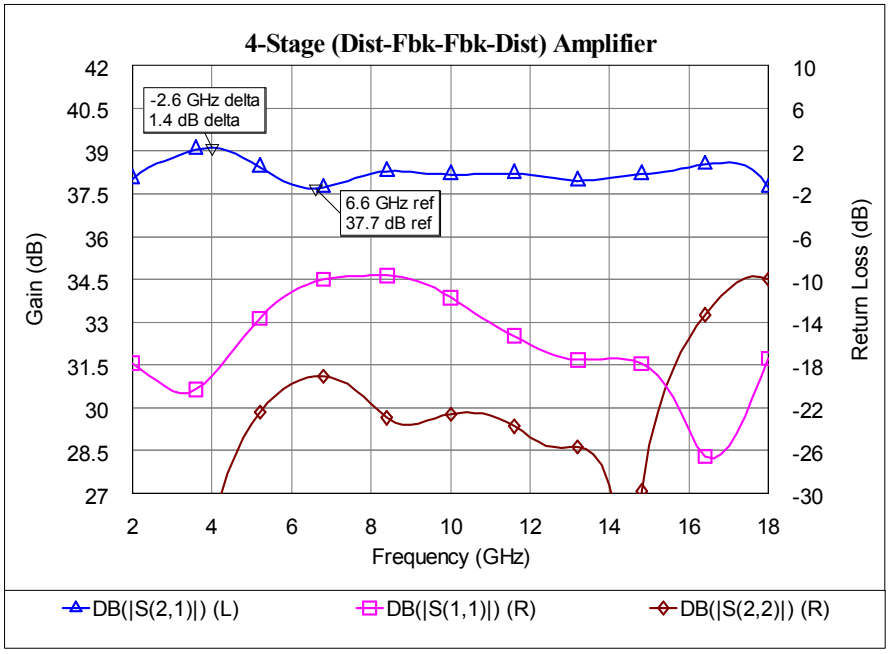


Figure 4-40: Simulation results of the 4-stage amplifier in distributed-feedback-feedback-distributed cascaded combination

This 4-stage amplifier is capable of providing 38.4 dB +/- 0.7 dB small signal gain. Even though, this design gives 9 dB higher gain than the 3-stage design, the gain ripples of these two amplifier are nearly the same.

The designed multistage amplifiers can also be cascaded in order to design a limiting amplifier with much higher small-signal gain. For example, it is possible to design a 10-stage limiting amplifier by cascading two 3-stage amplifiers and one 4-stage amplifier.

4.4.2. Output Power of 3-Stage Amplifier

The output power of designed 3-stage amplifier is simulated in harmonic balance simulator of Microwave Office by using large signal model of FPD200 given in Figure 4-5. Since the last amplifier stage is chosen to be distributed type, the nonlinear simulation of distributed amplifier is sufficient to predict the output power of 3-stage amplifier. Besides, harmonic balance simulator converges much faster when only the last stage amplifier is simulated.

The transistors in the last stage distributed amplifier are biased at V_{gs}=-0.45 V. Transistors nearly draw half of the saturation current at this gate-to-source biasing voltage; therefore, the output power is maximized. Both 1-dB and 3-dB compression points of distributed amplifier are calculated according to frequency at two different drain-to-source biasing cases as demonstrated in Figure 4-41 and Figure 4-42.

The saturated power of an amplifier can be approximated by 3-dB compression power. Therefore, the predicted saturated output powers of distributed amplifier at 10 GHz for V_{ds}=3V and V_{ds}=5V are nearly 18 dBm and 21 dBm respectively as Figure 4-41 and Figure 4-42 show. It can be seen from Figure 4-6 that Class-A biasing conditions of FPD200 transistor are approximately V_{gs}=-0.45 V and V_{ds}=5 V. Therefore, the maximum saturated power level of distributed amplifier is expected to be nearly 21 dBm as shown in Figure 4-42.

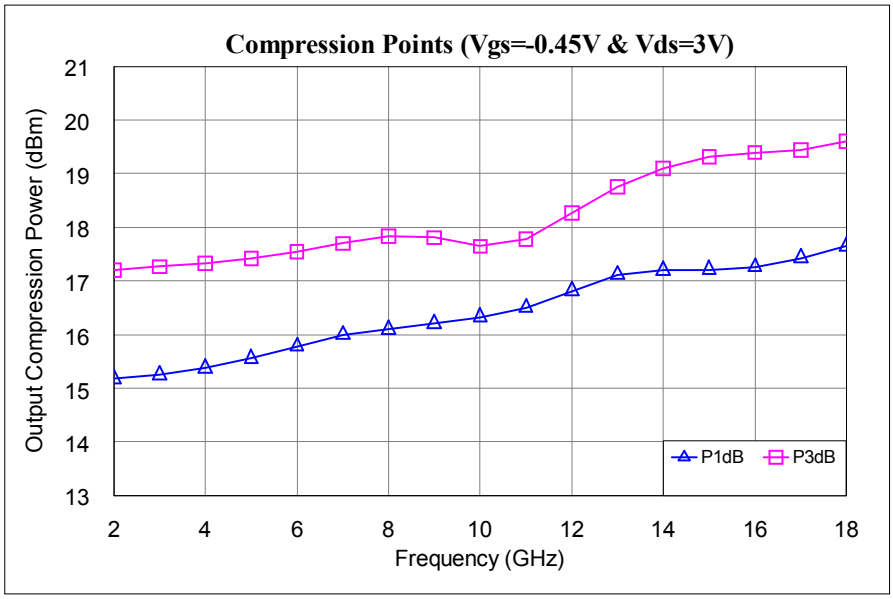


Figure 4-41: Simulated 1-dB and 3-dB compression points of 2-stage distributed amplifier for Vds=3V

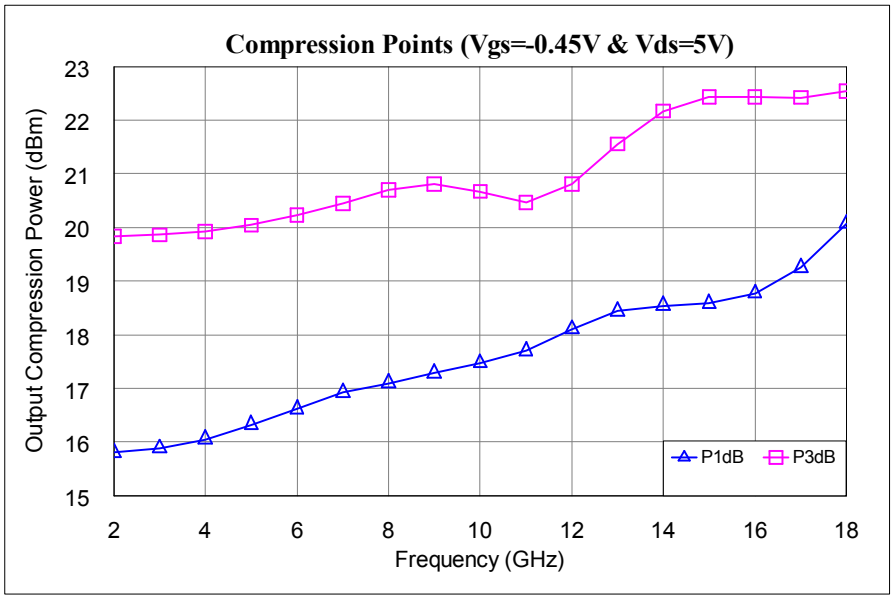


Figure 4-42: Simulated 1-dB and 3-dB compression points of 2-stage distributed amplifier for Vds=5V

CHAPTER 5

LIMITING AMPLIFIER FABRICATION AND MEASUREMENTS

The designed amplifiers are fabricated as hybrid microwave integrated circuits (HMICs). Discrete components and thin film circuits are used together in an HMIC. Transistor dies, single layer capacitors and air coil inductors are the three basic discrete components used in fabricated amplifier circuits. Moreover, thin film circuits are designed on Alumina (Al_2O_3) ceramic of 15 mils thickness due to its high dielectric constant (ε_r ~9.8) and low loss tangent (~0.0002 @ 10 GHz). Besides, thin film resistors are designed by 50 ohms/square TaN resistive films.

The connections of FPD200 transistor die to thin film circuits and capacitors are carried out by gold wire of 1 mil diameter. The gold wires are bonded to FPD200 die using ultrasonic wedge-bonding machine shown in Figure 5-1..

Figure 5-1: Westbond manual wedge-bonding machine

Measurements of the designed single stage and multistage amplifiers are performed by using the measurement setup given in Figure 5-2. The measurement setup is composed of a vector network analyzer (VNA), a power supply, a power meter and a power sensor. VNA is used to measure both small signal and large signal performance of the designed amplifiers. The ports of VNA are calibrated by using a 3.5 mm SOLT calibration kit. Besides, power meter and power sensor are used to calibrate the power level of the input port of VNA. During small signal gain measurements of fabricated amplifiers, the input power of VNA is reduced sufficiently such that the measured amplifier is not compressed. Especially for the fabricated 80 dB gain limiting amplifier module, the input power of VNA is reduced below -70 dBm during measurements. In general, the calibration of VNA should be performed under the same settings as the measurement. However, the dynamic accuracy of the used VNA is extremely good such that performing calibration at a different power level does not result in a significant error [34]. Moreover, it is better to calibrate the VNA at a higher power level during measurements of high gain amplifiers in order to reduce uncertainties due to noise [34]. Besides, the saturated output power level of a fabricated amplifier inside the operating frequency band is measured by summing the input power level and the measured gain when the amplifier is highly compressed.

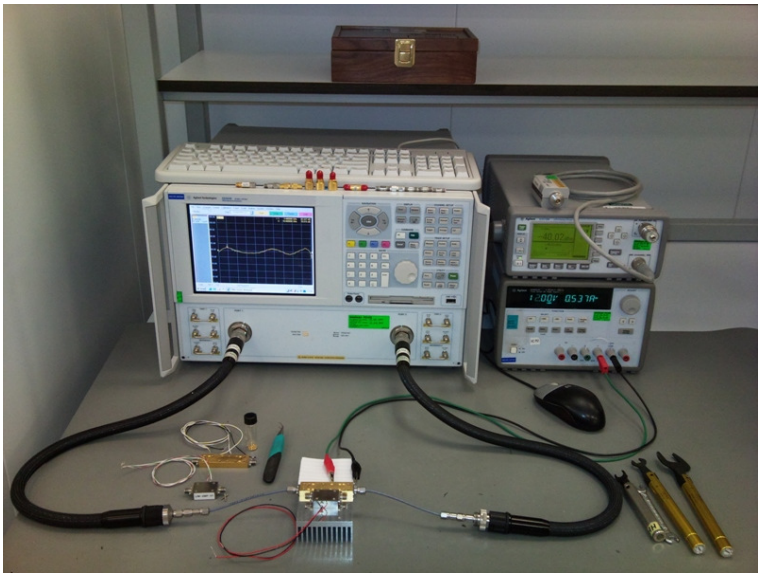


Figure 5-2: A photograph of the measurement setup for the fabricated amplifiers

5.1. Fabrication and Measurements of Single Stage Amplifiers

The designed single stage feedback type and distributed type amplifiers are fabricated individually. The fabricated amplifiers are measured in a probe station thanks to CPW-microstrip test points combined with input and output thin film circuits.

5.1.1. Feedback Amplifier

The fabricated single stage feedback amplifier is illustrated in Figure 5-3.

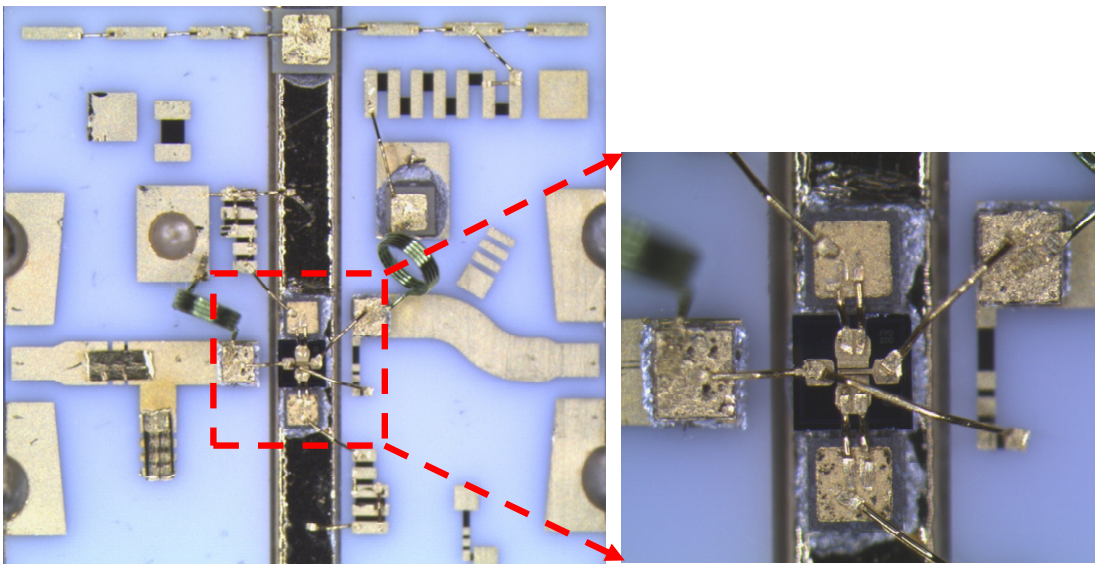


Figure 5-3: A photograph of the fabricated single stage feedback amplifier with coplanar test points

As can be seen from the above figure, FPD200 transistor die and source capacitors are mounted on a mechanical post of 15 mils thickness such that transistor die and input and output capacitors are nearly at the same level. Gate pad of FPD200 is connected to ground by a 4-turn 14 nH inductor such that gate pad of FPD200 is grounded at DC with minimal effect on RF performance of the amplifier. Tunable drain biasing resistors shown at the right top of Figure 5-3 are used to set drain

voltage of FPD200 from a fixed supply voltage. Then, it is able to bias the transistor at different drain voltages without varying the main supply. Since the two source pads of FPD200 are not shorted by an air bridge, one self biasing resistor is used for each source pad such that half of the drain current passes through each resistor. The matching resistors at the input are shorted by a gold ribbon in order to eliminate the effects of these resistors.

The fabricated single stage feedback amplifier is measured in a probe station with GSG probes. The measurement results along with the simulated responses are given in Figure 5-4. The measured gain level is about 8.5 dB with 0.45 dB ripple. Besides, simulated and measured gain characteristics show quite a good fit to each other. Moreover, the worst input return loss is measured as -8.4 dB inside the operating frequency range.

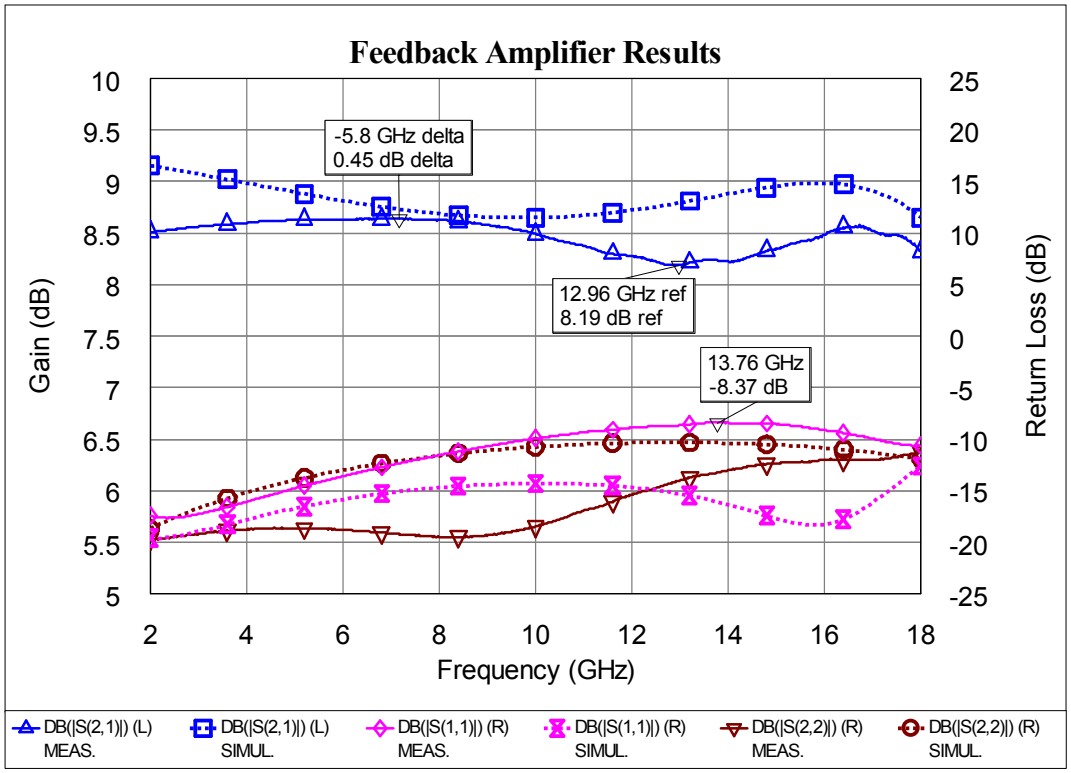


Figure 5-4: Measured (solid) and simulated (dotted) performance of single stage feedback amplifier

The performance of feedback amplifier is affected from fabrication tolerances of thin film circuits. For example, a typical tolerance value for thin film resistors is +/-10 %. Therefore, if feedback resistor is designed to be 200 ohms, it can become any value between 180 ohms and 220 ohms after fabrication. A 220 ohms feedback resistor is found to be optimal for a 2-18 GHz feedback amplifier design. However, the fabricated resistor can be measured as 240 ohms from the test resistor that is put into the thin film circuit. In Figure 5-5, the measured gain responses of feedback amplifier are demonstrated for two different feedback resistances; namely, 220 ohms and 240 ohms. Feedback resistor affects mainly the low frequency gain of the feedback amplifier as Figure 5-5 depicts. Then, feedback resistor can be designed smaller than the optimum value in order to compensate a possible positive tolerance of thin film resistors. Similarly, feedback resistor should be designed such that the feedback resistance can be increased in order to compensate a possible negative tolerance of thin film resistors. Moreover, a tunable feedback resistor is beneficial for tuning the low frequency response of a multistage amplifier including a feedback amplifier.

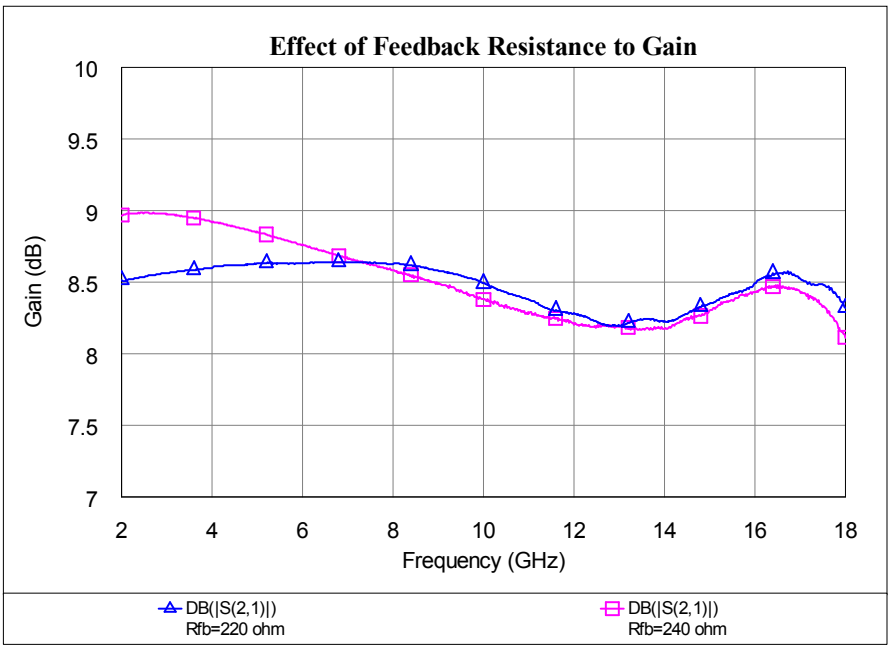


Figure 5-5: Measured gain of single stage feedback amplifier at two different feedback resistor values

5.1.2. Distributed Amplifier

The fabricated 2-stage distributed amplifier is illustrated in Figure 5-6.

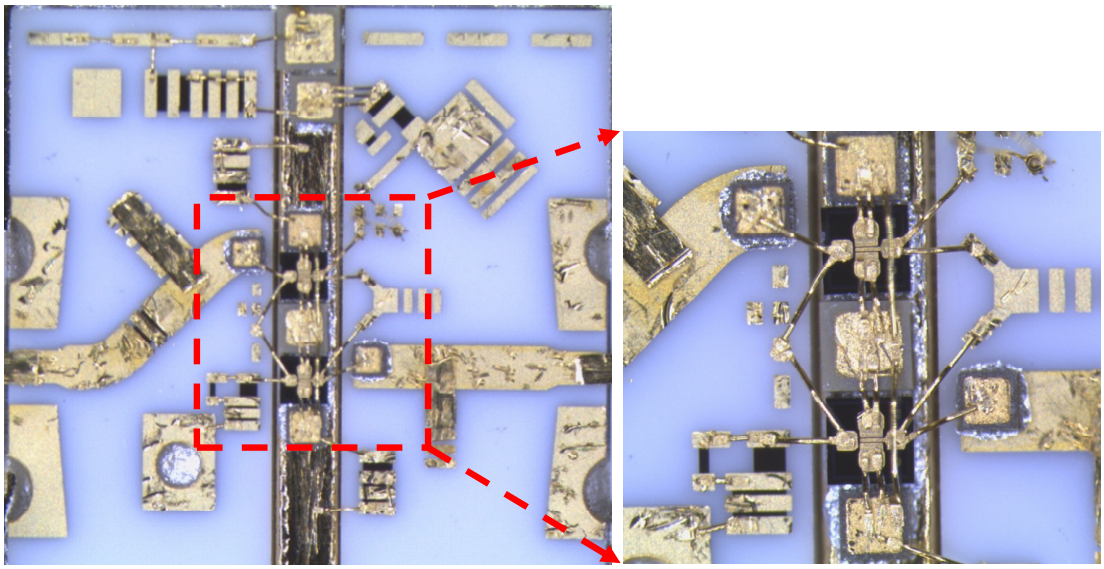


Figure 5-6: A photograph of the fabricated 2-stage distributed amplifier with coplanar test points

Similar to the fabricated feedback amplifier shown in Figure 5-6, transistor dies and source capacitors are brought to the same level of thin film circuits. The two source pads of FPD200 transistor is shorted in DC by a wire bond between source capacitors. In order to improve the high frequency gain of distributed amplifier, the length of bond-wire between drain terminal of the first transistor and drain termination resistor can be tuned with the help of small pads. Therefore, the length of drain termination bond-wire can be changed without disconnecting the bond-wire at the drain terminal of FPD200. Moreover, the shunt capacitance before the drain termination resistor can be varied by extending the open stub with the help of thin strips.

The measured and simulated S-parameters of 2-stage distributed amplifier are given in Figure 5-7.

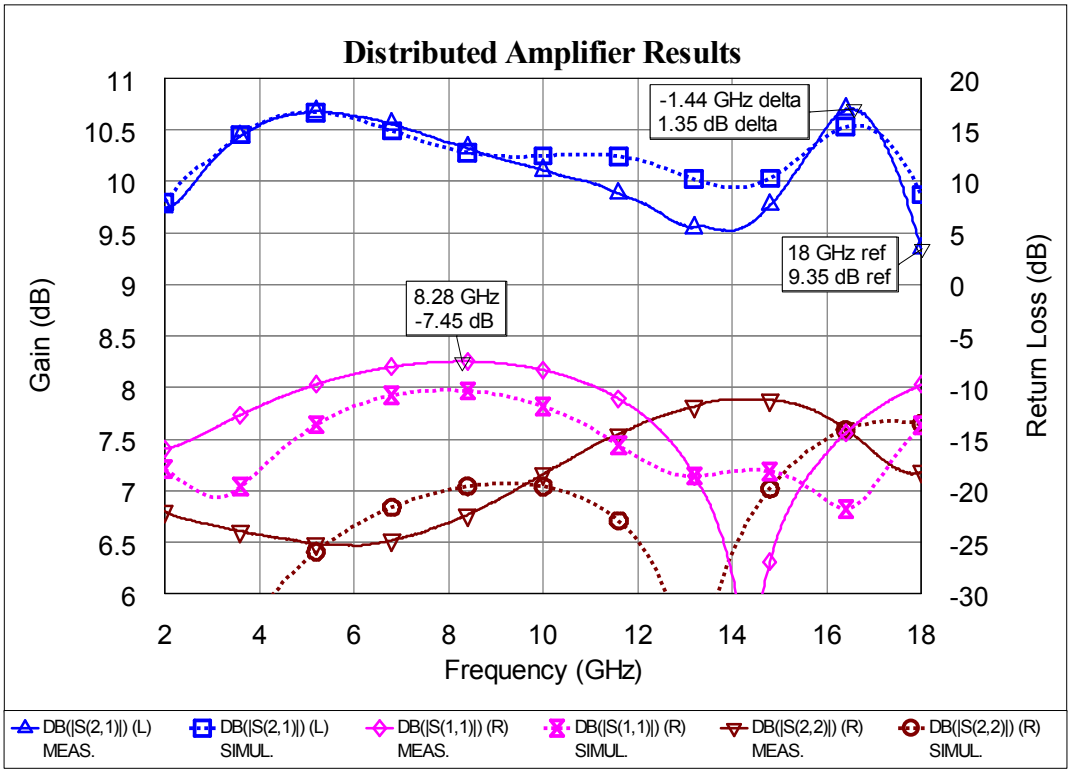


Figure 5-7: Measured (solid) and simulated (dotted) performance of 2-stage distributed amplifier

The measured and simulated gain characteristics of distributed amplifier are very similar to each other as shown in Figure 5-7. The input return loss of the measured amplifier is a bit worse than that of the simulated amplifier. However, input return loss can be improved by using series matching resistors inserted into the thin film circuit at the input. The input return losses of the distributed amplifier for different values of input series resistor are demonstrated in Figure 5-8. The best input matching is obtained when the maximum designed series resistance, 15 ohms, is applied to the input. However, the gain of the amplifier decreases over 1 dB as can be seen from Figure 5-9. Moreover, noise figure of the amplifier is degraded with the addition of input series resistor. Since, noise figure is not very important for limiting amplifiers, resistive matching can be used at the input stage of a limiting amplifier at the expense of nearly 1 dB reduction in gain.

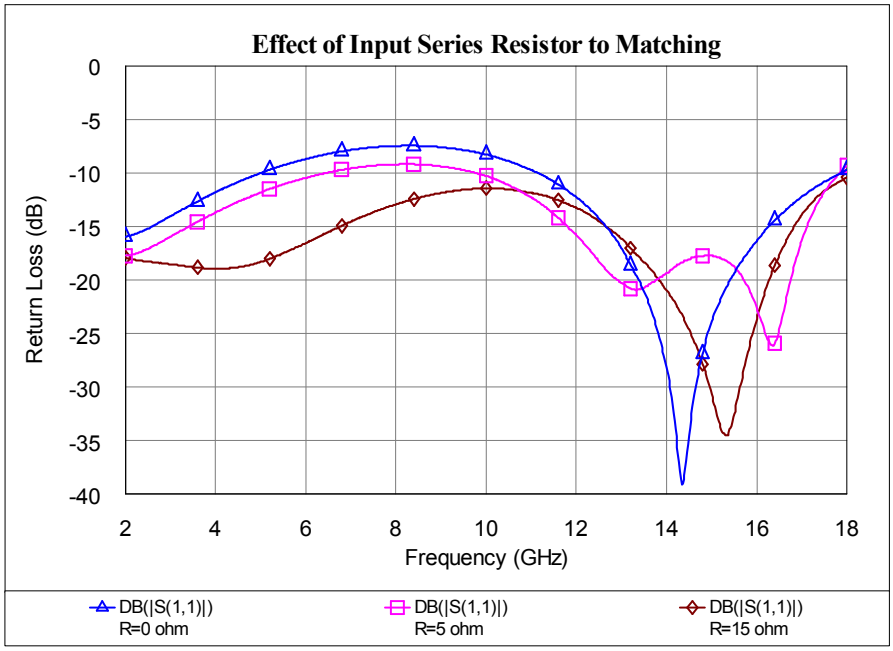


Figure 5-8: Effect of series input resistor to measured input return loss of distributed amplifier

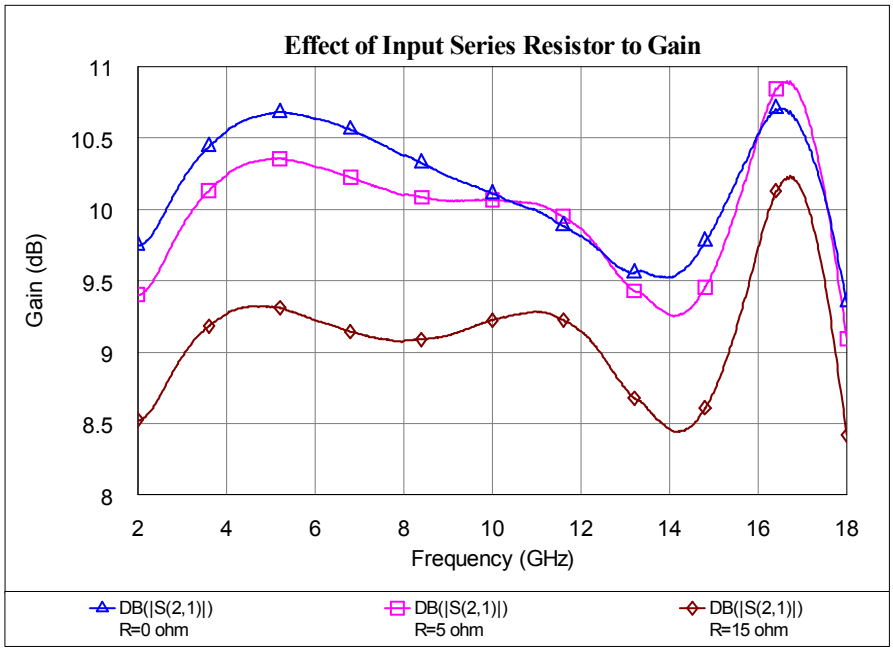


Figure 5-9: Effect of series input resistor to measured gain of distributed amplifier

5.2. Fabrication and Measurements of 3-Stage Amplifier

The 3-stage amplifier is designed such that the input and output stages are distributed amplifiers and the middle stage is feedback amplifier. Then, thin film circuits of each amplifier are placed as shown in Figure 5-10.

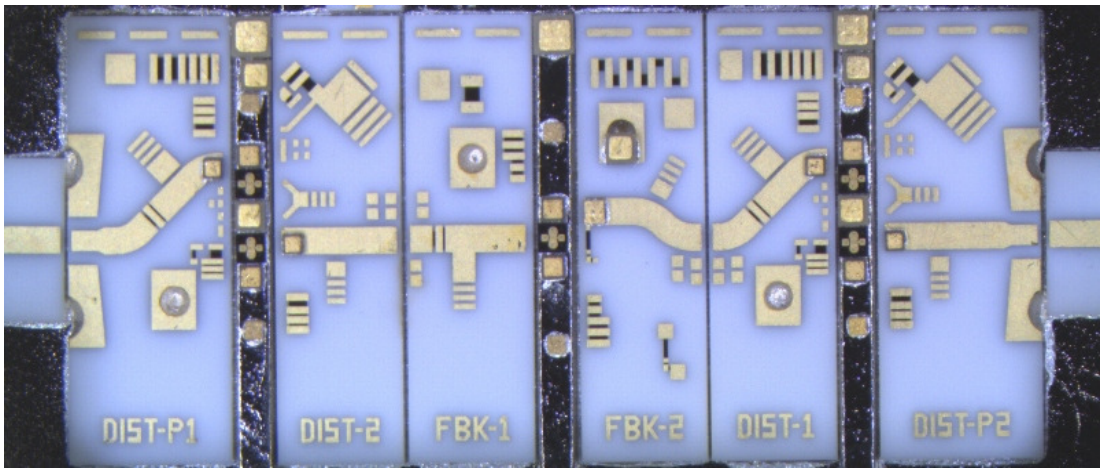


Figure 5-10: Placement of thin film circuits and discrete components in 3-stage amplifier layout

Transistor dies and chip capacitors are placed on mechanical posts between thin film circuits. While measuring the performance of 3-stage amplifier, gold disks are used to improve the performance of 3-stage amplifier as illustrated in Figure 5-11.

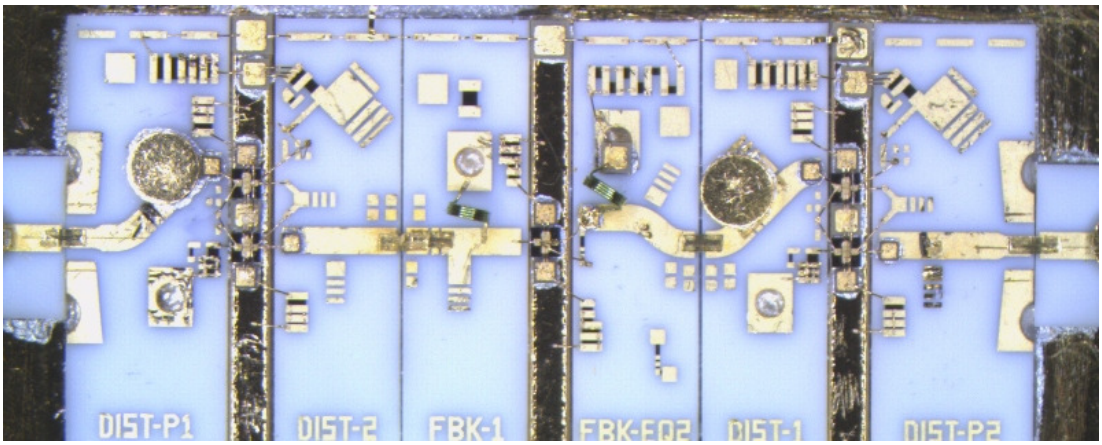


Figure 5-11: Gold disks used for tuning the performance of 3-stage amplifier

Thin film circuits and discrete components are arranged inside a mechanical housing as shown in Figure 5-12.

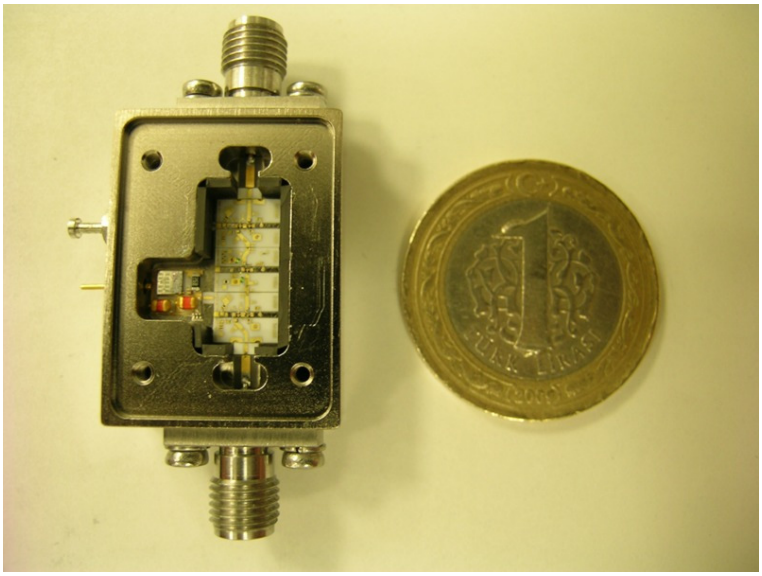


Figure 5-12: A photograph of the fabricated 3-stage amplifier module

AlSi material is chosen for the fabrication of the amplifier module instead of Aluminum; because, its coefficient of thermal expansion is more closely matched to GaAs and Alumina ceramic. The material characteristics of Alumina, GaAs, Aluminum and AlSi are shown in Table 5-1.

Table 5-1: Characteristics of different materials [35]

Material	Thermal Conductivity (W/m.K)	Coef. of Thermal Expansion (ppm/ºC)
Alumina	20-30	6.5
GaAs	54	6.5
Aluminum	205	23.9
Al-40%Si	170	13

The 3-stage amplifier module has a single 12V supply pin for common biasing of amplifier stages. Then, 12V supply voltage is reduced to a convenient voltage level

by a variable voltage regulator. Moreover, drain bias voltage of each amplifier stage is adjusted by using thin film resistors. The 3-stage amplifier module, whose measured performance is demonstrated in Figure 5-13, draws approximately 150 mA from 12V supply.

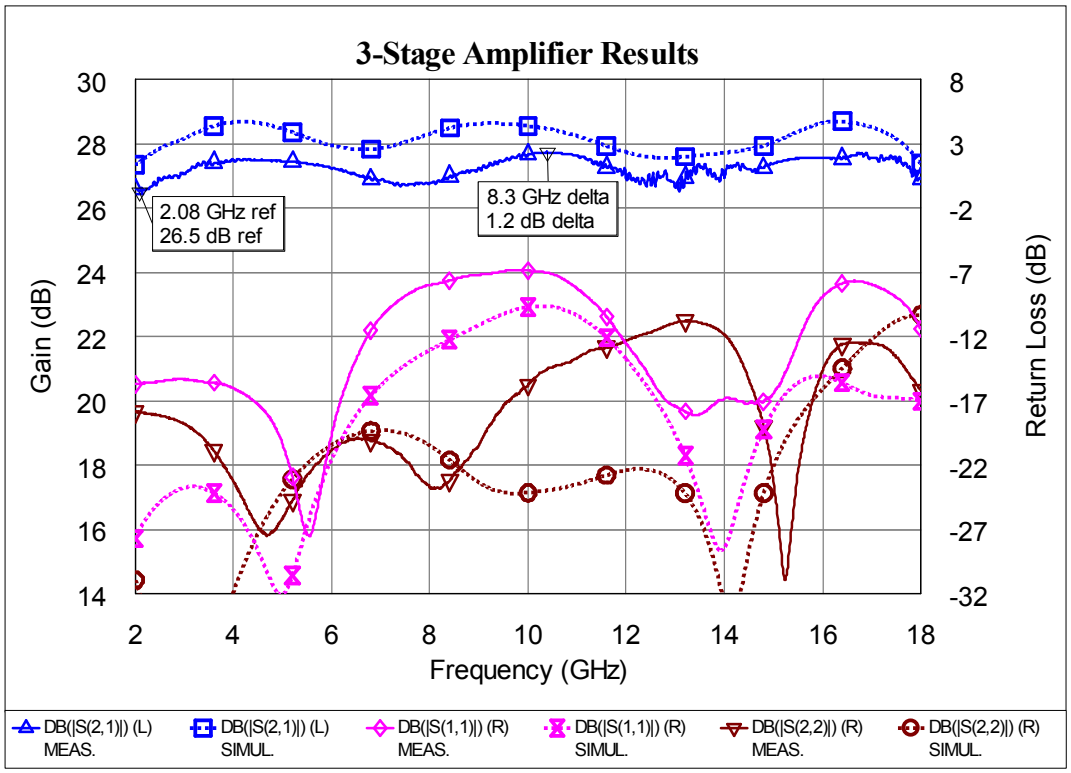


Figure 5-13: Measured (solid) and simulated (dotted) performance of 3-stage cascaded amplifier

The small signal gain of 3-stage amplifier is measured approximately as 27dB +/- 0.6dB. Besides, the shape of the measured gain response according to frequency is very similar to that of simulated response. The difference between the levels of measured and simulated gain may be due to unsimulated input and output SMA connector to microstrip transitions. Moreover, transconductance of FPD200 transistor is not exactly the same for all products. Therefore, transistors used in the amplifier module may have lower transconductance than simulated and modeled transistors such that the simulated gain level is greater than the measured gain level. The shapes of simulated and measured input return loss characteristics nearly match

to each other. However, the measured input return loss closes to -7 dB in the middle region of operating frequency band. In order to improve the return loss in this region, tuning gold disk shown in Figure 5-11 is used at the input of distributed amplifier in the first stage. Then, the performance of the newer version of 3-stage amplifier with optimized input return loss is measured as illustrated in Figure 5-14.

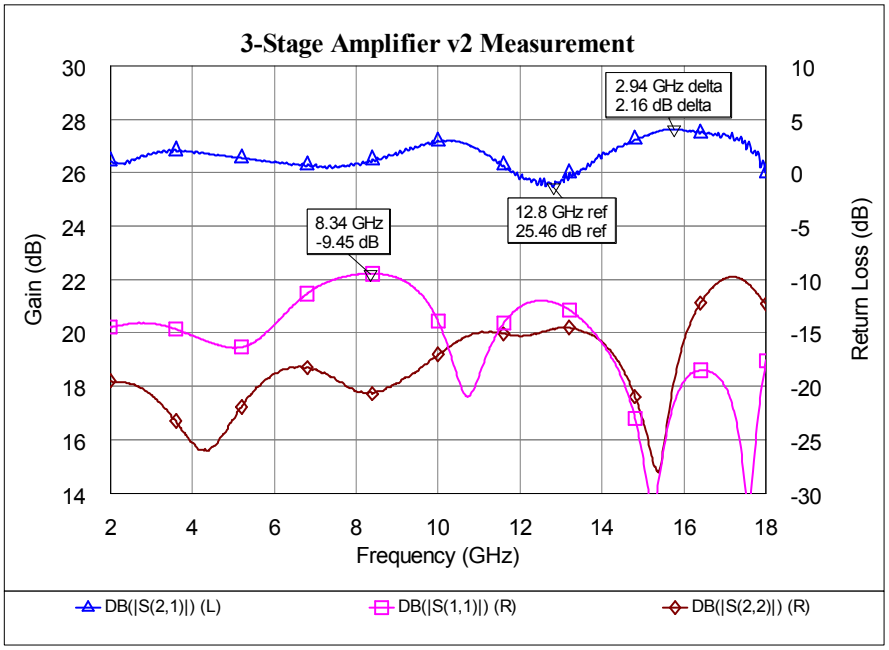


Figure 5-14: Measured performance of 3-stage cascaded amplifier with improved input return loss

The gain level of the optimized 3-stage amplifier is similar to the original one. However, the gain ripple is increased to 2.2 dB from 1.2 dB. Moreover, both input and output return losses are below -10 dB over 2-18 GHz range.

The output power of 3-stage amplifier is measured for two different drain voltages of output stage amplifier at different input power levels as illustrated in Figure 5-15 and Figure 5-16. The saturated output power is approximately 17.5 dBm for Vds=3V and 19 dBm for Vds=5V. The variation of saturated output power levels is within +/- 1dB inside the operating frequency range. Moreover, the measured ouput power characteristics show a positive slope with increasing frequency similar to

simulations. This positive slope of output power will be beneficial for compensating high frequency losses of the circuits connected at the output of limiting amplifier.

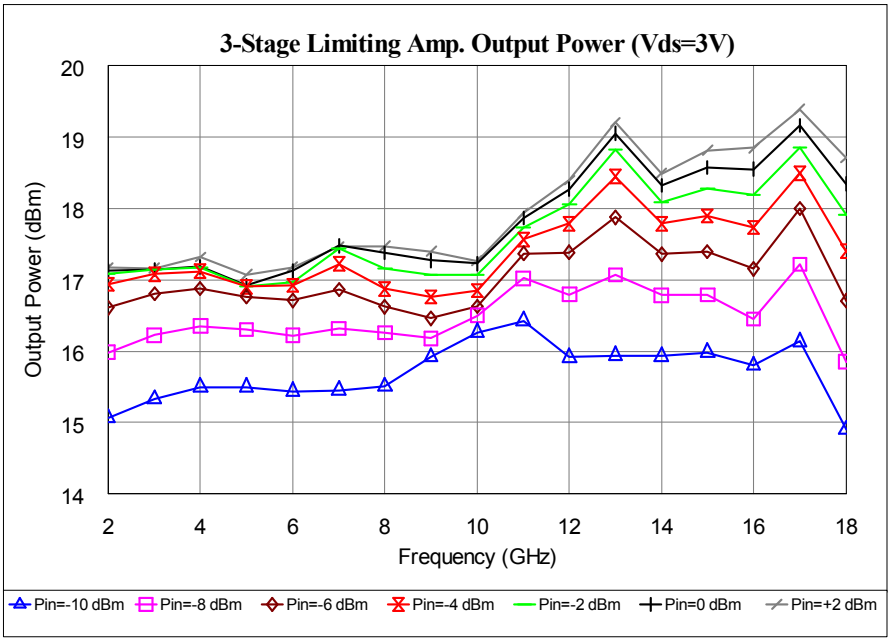


Figure 5-15: Measured output power of 3-stage amplifier for Vds=3V

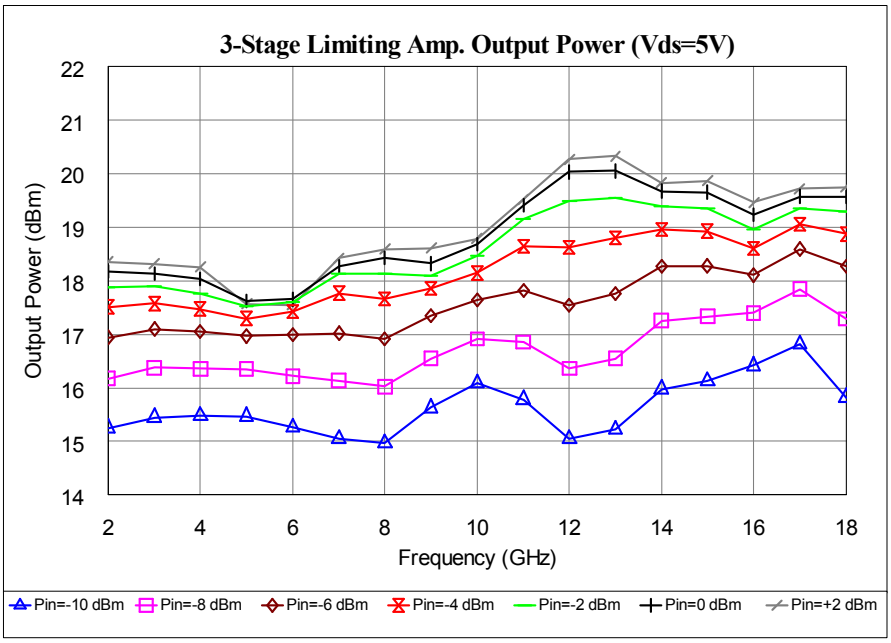


Figure 5-16: Measured output power of 3-stage amplifier for Vds=5V

The fabricated 3-stage amplifier module can also be used as a limiting amplifier for applications not requiring wide input dynamic range. As can be seen from Figure 5-15 and Figure 5-16, the 3-stage amplifier module provides nearly constant output power for input power levels greater than -4 dBm. Moreover, the separate 3-stage amplifier modules can be cascaded to realize a limiting amplifier with much wider input dynamic range.

Since a low noise amplifier is used before limiting amplifier in a receiver system, noise figure is not a primary concern for limiting amplifier design. However, the noise figure of the 3-stage amplifier is measured for two different input series resistances used for matching as depicted in Figure 5-17.

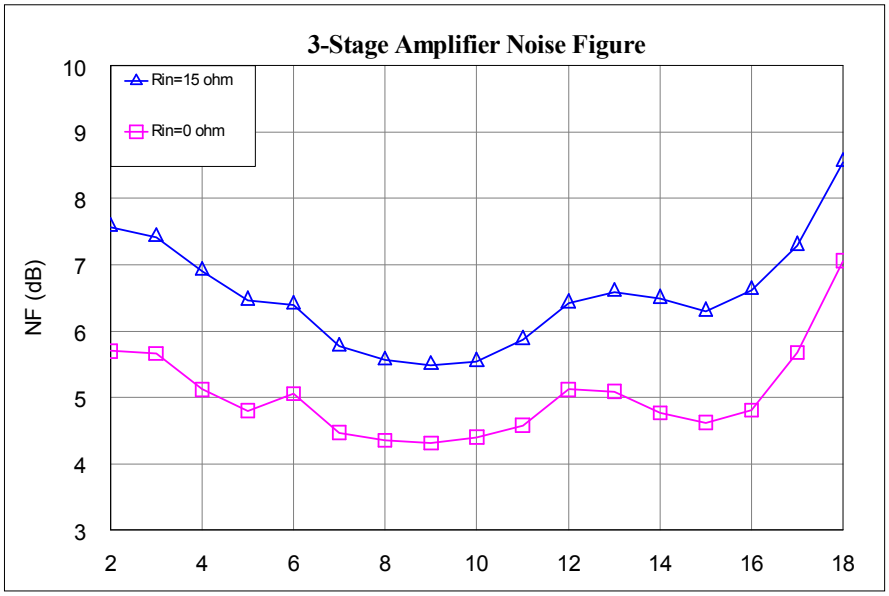


Figure 5-17: Measured noise figure of 3-stage amplifier

The noise figure at 10 GHz is measured as 4.5 dB for no input resistor case and 5.5 dB for input resistor of 15 ohms. Therefore, a series resistor of 15 ohms can be used to improve input matching of the 3-stage amplifier with nearly 1 dB degradation in both noise figure and gain.

5.3. Fabrication and Measurements of 10-Stage Limiting Amplifier Module

It is aimed to design a limiting amplifier capable of providing constant output power to a minimum -50 dBm input signal. Since the maximum saturated output power of 3-stage amplifier is measured nearly as 20 dBm, the minimum input signal level is ensured to be saturated if the small signal gain of the limiting amplifier is greater than 75 dB. Moreover, the limiting amplifier should include a variable analog attenuator such that the variations in gain due to temperature changes can be compensated. The attenuation of variable attenuator at room temperature is planned to be nearly 9 dB; therefore, the control voltage of variable attenuator should be arranged such that the attenuation applied at cold temperatures is greater than 9 dB and that applied at high temperatures is lower than 9 dB. Therefore, a minimum of 83 dB gain should be obtained from cascaded gain stages.

The gain of the 3-stage amplifier is measured as 27 dB. Therefore, cascade connection of three 3-stage amplifiers is not sufficient to satisfy the minimum gain requirement. Hence, the realized amplifier should include at least ten stages of amplifiers. The 10-stage limiting amplifier is decided to be realized as shown in Figure 5-18.

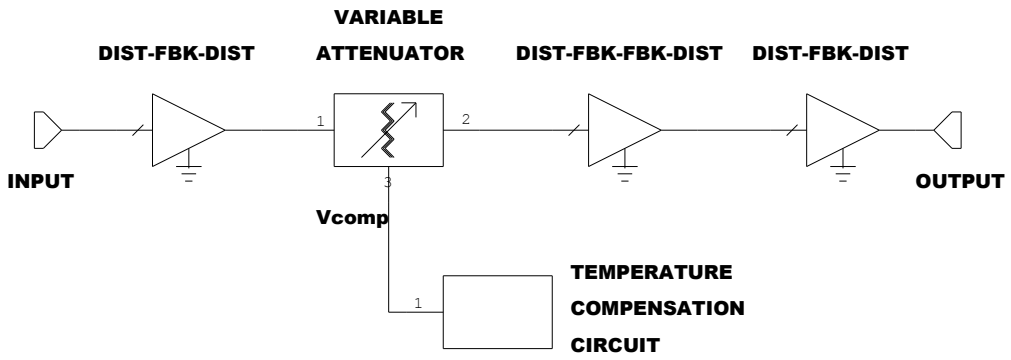


Figure 5-18: Realization of temperature compensated 10-stage limiting amplifier

10-stage limiting amplifier is designed to include three multistage amplifiers in cascade. The input and output stages are 3-stage amplifiers in distributed-feedback-distributed configuration. The middle stage is a 4-stage amplifier in distributed-feedback-feedback-distributed configuration. Simulation results of the 4-stage amplifier in this configuration show flat gain characteristics inside 2-18 GHz frequency range. Moreover, variable attenuator is placed between the first and middle stages of multistage amplifiers. The control voltage of variable attenuator can be produced by an external temperature compensation circuit.

The fabricated 10-stage limiting amplifier module is shown in Figure 5-19. The amplifier module is designed as a channelized structure where thin film ceramics and other components are placed. The separation of side walls is made sufficiently small such that unwanted modes cannot propagate inside the operating frequency interval. Moreover, high-gain multistage amplifier stages are separated by straight walls in order to eliminate possible oscillations.

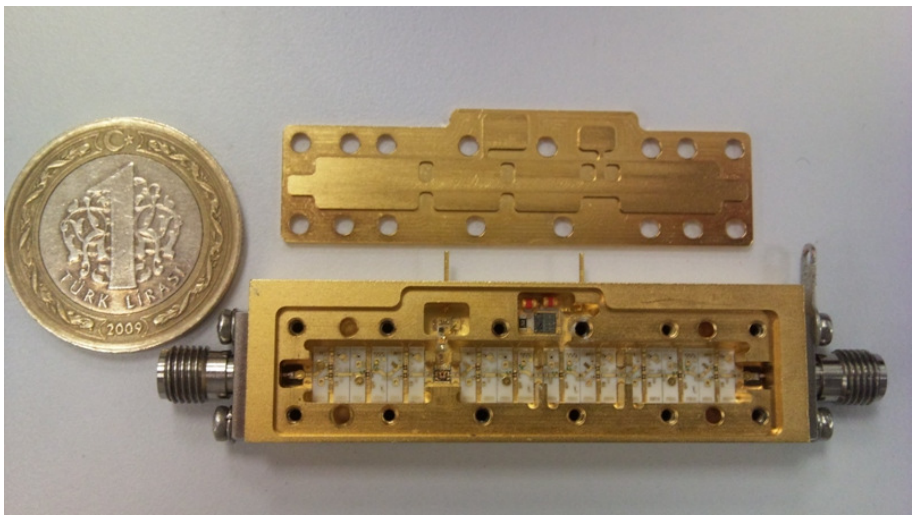


Figure 5-19: A photograph of the fabricated 10-stage limiting amplifier module

The fabricated limiting amplifier includes two external pins. One pin is for DC regulator supply (12V) and the other pin is for the control voltage of variable attenuator. The variable attenuator is biased externally without temperature

compensation circuit. However, a suitable temperature compensation circuit can be integrated externally with the limiting amplifier module.

The optimized small signal gain of 10-stage limiting amplifier module is measured as shown in Figure 5-20.

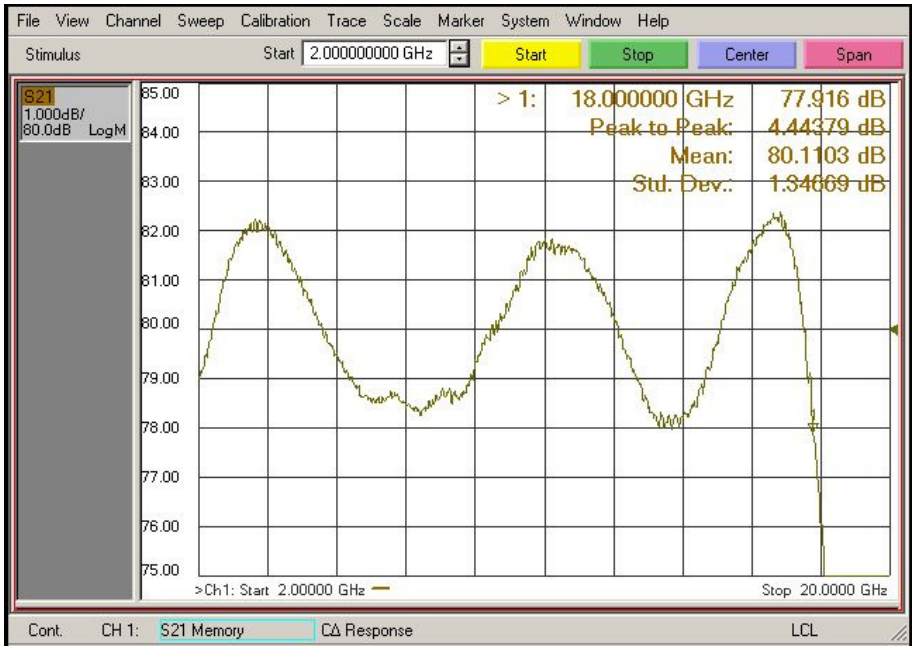


Figure 5-20: Measured small signal gain of 10-stage limiting amplifier module in 2-20 GHz range

The fabricated limiting amplifier module presents 80 dB small signal gain with excellent flatness, +/-2.2 dB, inside 2-18 GHz frequency range. Moreover, the lowest gain measured at 18 GHz (77.9 dB) is sufficient to saturate the output of limiting amplifier.

The fabricated limiting amplifier module is simulated by including the effects of tuned elements. Input and output connectors are not included in the simulations. The simulated small signal gain response closely fits to the measured response as illustrated in Figure 5-21.

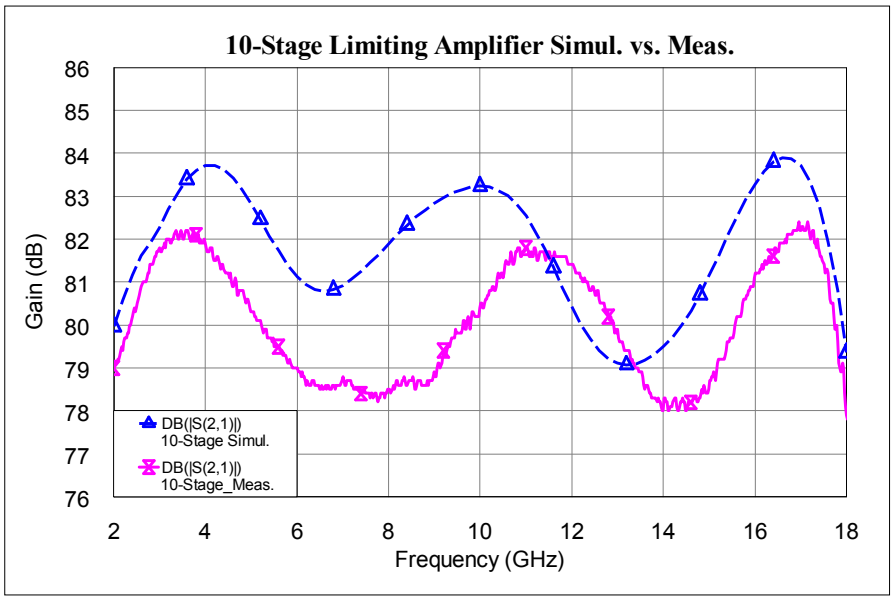


Figure 5-21: Measured (solid) and simulated (dashed) performance of 10-stage limiting amplifier

Measured input and output return loss performances of the fabricated limiting amplifier are shown in Figure 5-22. Both input and output return losses are below -10 dB nearly over the whole operating frequency range.

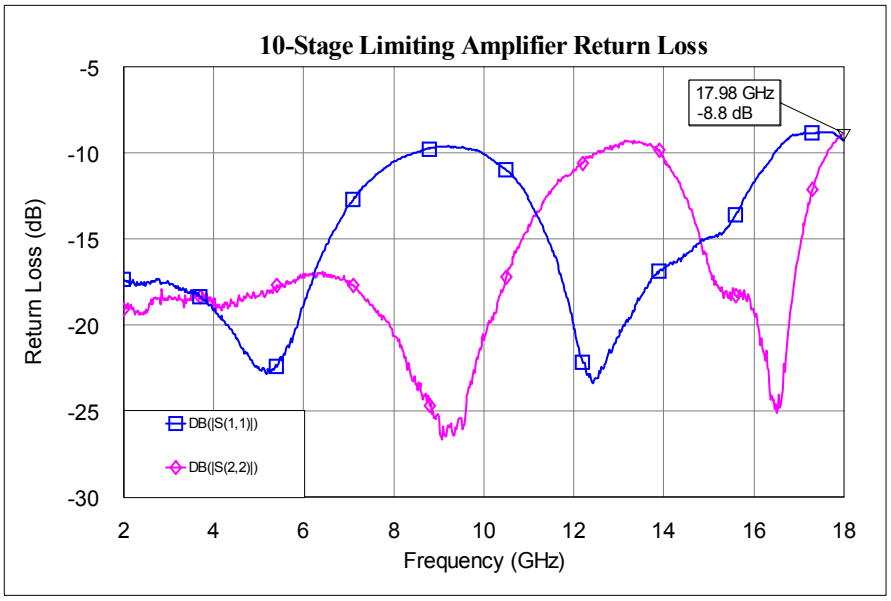


Figure 5-22: Measured input and output return losses of 10-stage limiting amplifier

Output power of limiting amplifier module is measured at different input power levels as shown in Figure 5-23. The small signal gain of limiting amplifier is sufficient to saturate input power levels greater than -50 dBm over the whole operating frequency range. The saturated output power level is approximately 20 dBm with a flatness of +/-1.2 dB. The measured saturated output power level of 10-stage limiting amplifier module is consistent to both the measured and simulated output power level of 3-stage amplifier.

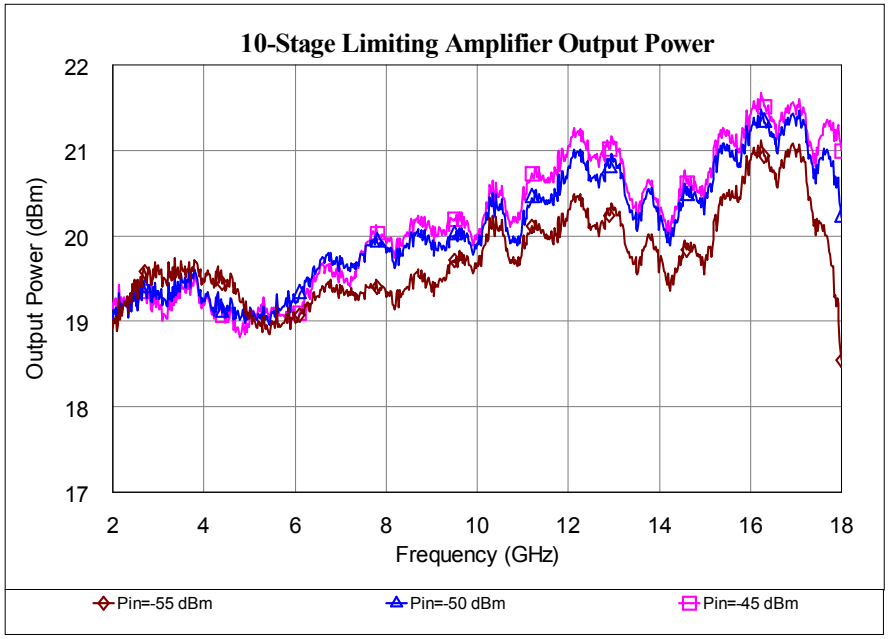


Figure 5-23: Measured output power of 10-stage limiting amplifier

CHAPTER 6

CONCLUSION AND FUTURE WORK

Microwave limiting amplifiers are the key components of Instantaneous Frequency Measurement (IFM) receivers. The basic function of a microwave limiting amplifier in an IFM receiver is to compress a large dynamic range of input signals into a nearly constant output dynamic range over a wide frequency range. Therefore, microwave limiting amplifiers are designed with sufficiently high small signal gains to ensure the compression of the amplifier at minimum input signal levels. Besides, small signal gain flatness of a limiting amplifier is important in terms of the simultaneous signal performance of the IFM system. A large variation of gain inside the operating frequency band degrades the sensitivity of the IFM system such that the probability of the IFM system to report the wrong frequency increases.

In this thesis, the design, fabrication and measurement results of a limiting amplifier with 80 dB small signal gain are presented. The fabricated limiting amplifier provides excellent gain flatness, +/-2.2 dB, inside the 2-18 GHz frequency band. Moreover, the limiting amplifier is able to bring input signal levels greater than -50 dBm to +20 dBm output power level. The flatness of saturated output power level is also within +/-1.2 dB inside the operating frequency range.

Transistor selection and modeling is the starting point of the limiting amplifier design. The chosen transistor is measured in a probe station by using high precision calibration substrates. Then, accurate small signal model of the chosen transistor is obtained by the combination of analytical extraction and optimization. The excellent

agreement between the measured and simulated responses of designed amplifiers proves the accuracy of the small signal model of the transistor used.

The application of two main broadband amplification methods; namely, negative feedback and distributed amplification, to limiting amplifier design provides excellent broadband characteristics. First, a three stage amplifier module consisting of cascaded negative feedback and distributed amplifiers in a novel configuration was designed and fabricated. The fabricated amplifier module provides excellent gain flatness and satisfactory input and output return losses. Then, the cascade connections of two three stage amplifiers and one four stage amplifier result in a very high gain limiting amplifier with excellent flatness.

The designed amplifiers are fabricated as hybrid microwave integrated circuits (HMICs). Thin film ceramics are combined with discrete components such as transistor dies and chip capacitors. The use of die transistors instead of packaged transistors enables broadband operation close to one decade. Moreover, the amplifier circuits are miniaturized thanks to high dielectric constant of Alumina ceramic material used for thin film circuits. Even the longest dimension of the fabricated 80 dB gain limiting amplifier is shorter than 6 centimeters.

Since a lot of bondwire connections exist in fabricated amplifier circuits, variations between simulated and measured amplifier responses inevitably occur. In order to eliminate these variations, a compensation technique like the following may be applied. First, the fabricated amplifier is measured and the variations between the measurements and simulation results at different parts of the frequency band are determined. Then, the interconnects whose lengths appear to be different from simulated ones are either shortened or lengthened. If there is still difference between the simulated and measured responses, the measured response is tried to be improved by using built-in tuning elements. The effects of the tuned elements can be predicted by applying tuning in simulation environment first.

The mechanical construction of a high gain amplifier module is important in terms of stability. The amplified signals from amplifier stages are reflected back to input and cause oscillations. One way of eliminating oscillations is to use an absorbing material on the cover of the module. A properly designed amplifier module isolating cascaded amplifier stages properly and preventing higher order modes to propagate does not cause oscillations even without absorbing material on the cover.

The future works can be summarized as follows,

- Small signal gain variation of the fabricated limiting amplifier module will be determined between -40 °C and 85 °C. Then, a temperature compensation circuit can be designed to create suitable analog voltage variation with respect to temperature to be applied as control voltage of a variable attenuator. Since, the amplifier stages are designed as self biased, the gain variation of ten amplifier stages over temperature is predicted to be minimal. The gain of solid state amplifiers decreases with increasing temperature due to temperature characteristics of transistors. Therefore, the limiting amplifier module gives more small signal gain at temperatures lower than the room temperature. Since larger gains at cold temperatures still saturate the output of limiting amplifier, no temperature compensation is required for cold temperatures. However, gain drop at high temperatures may be problematic for this limiting amplifier. If the limiting amplifier provides sufficient small signal gain to saturate the output even at the maximum temperature, no temperature compensation will be required.

- Simultaneous signal performance of the fabricated limiting amplifier module will also be measured. First, two signals at different frequencies with a predefined amplitude separation will be applied at the input of limiting amplifier. Then, the amplitude difference between the two signals will be measured at the output in order to detect how much the weak signal is suppressed. Moreover, the harmonic performance of the limiting amplifier will be analyzed. Since, the 2^{nd} and 3^{rd} harmonics of input signals up to 6

GHz fall into 2-18 GHz frequency interval, it is sufficient to measure 2nd and 3rd harmonic levels at the output for these input signals.

- The fabricated limiting amplifier module will be inserted into the front-end of an IFM system. Then, it is investigated how some characteristics of the limiting amplifier such as gain flatness, harmonics and small signal suppression affect the performance of the IFM system.

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Appendix A: TOM3 Model Parameters of FPD200

Table A-1: TOM3 model parameters of FPD200 transistor [32]

VTO	-0.6471 V	**QGG0**	1.227E-16
ALPHA	3.053	**CDS**	0.000234
BETA	0.000682	**IS**	1E-11 mA
LAMBDA	-0.02432	**EG**	0.8 V
GAMMA	0.03358	**N**	1
Q	0.9352	**XTI**	2
K	4.279	**TAU**	0.001 ns
VST	0.05677	**VBI**	1 V
MST	0.2041	**TAU_GD**	1000 ns
ILK	1.8E-6 mA	**KGAMMA**	0.01194
PLK	1.5 V	**RG**	0.01 Ω
QGQH	7.349E-16	**RGSH**	0 Ω
QGSH	8.451E-16	**RD**	0.01 Ω
QGDH	2.073E-17	**RS**	0.01 Ω
QGIO	2.002E-6	**LS**	0 nH
QGQL	8.58E-16	**LG**	0 nH
QGAG	2.21	**LD**	0 nH
QGAD	2.241	**NG**	2
QGCL	7.715E-17	**W**	100
QGGB	144.55		

Appendix B: Fitted vs. Modeled Characteristics of TOM3 Model

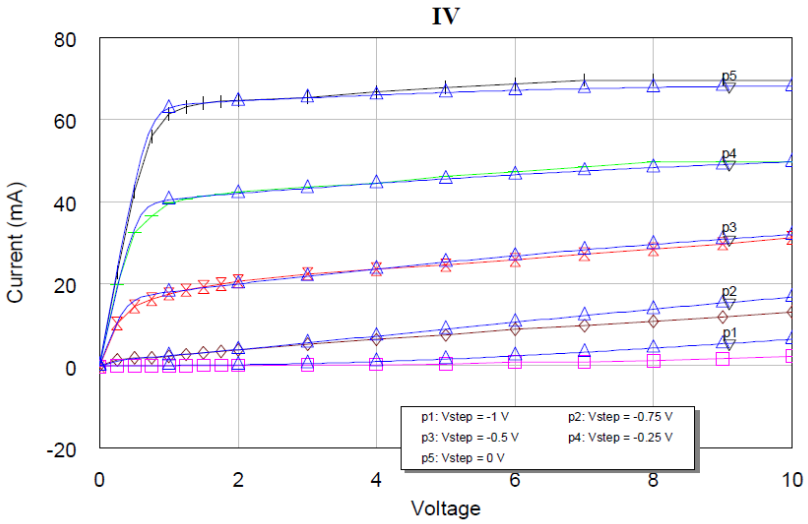

Figure B-1: Fitted vs. modeled IV curves [32]

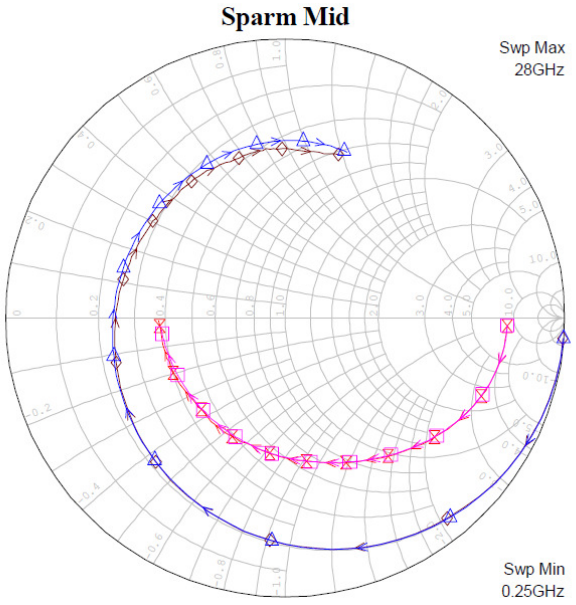

Figure B-2: Fitted vs. modeled S-parameters (biased at Vg=-0.3V, Vd=7V) [32]