CMOS INTEGRATED SENSOR READOUT CIRCUITRY FOR DNA DETECTION APPLICATIONS

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ABSTRACT

CMOS INTEGRATED SENSOR READOUT CIRCUITRY FOR DNA DETECTION APPLICATIONS

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This study presents a CMOS integrated sensor chip suitable for sensing biological samples like DNA. The sensing part of the chip consists of a 32 X 32 pixel array with a 15 µm pixel pitch. Pixels have 5 µm X 5 µm detector electrodes implemented with the top metal of the CMOS process, and they are capable of detecting charge transferred or induced on those electrodes with a very high sensitivity. This study also includes development of an external electronics containing ADC for analog to digital data conversion. This external circuitry is implemented on a PCB compatible with the Opal Kelly XM3010 FPGA that provides data storage and transfer to PC.

The measured noise of the overall system is 6.7 e^- (electrons), which can be shrunk down to even 5.1 e^- with an over sampling rate. This kind of sensitivity performance is very suitable for DNA detection, as a single nucleotide of a DNA contains 1 or 2 e^- and as 10 to 20 base pair long DNA's are usually used in microarray applications. The measured dynamic range of the system is 71 dB, in other words, at most 24603 e^- per frame (20 ms) can be detected. The

measured leakage is 31 e^-/frame, but this does not have a dramatic effect on the sensitivity of the system, noting that the leakage is a predictable quantity.

DNA detection tests are performed with the chip in addition to electronic performance measurements. The surface of the chip is covered with a nitride passivation layer to prevent the pixel crosstalk and is modified with an APTES polymer for suitable DNA immobilization. DNA immobilization and hybridization tests are performed with 5'-TCTCACCTTC-3' probe and its complementary 3'-AGAGTGGAAG-5' target sequences. Hybridization performed in 1 pM solution is shown to have a larger steady state leakage than the immobilization in a 13 µM solution, implying the ability to differentiate between the full match and full mismatch sequences. To best of our knowledge, the measured pM sensitivity has not yet been reported with any label free CMOS DNA microarrays in literature, and it is comparable with the sensitivity of techniques like QCM or the fluorescence imaging. The 1 pM sensitivity is not a theoretical limit of the sensor, since theoretically the sensitivity level of 6.7 e^- can offer much better results, down to the aM level, as far as the noise of electronics is considered, nevertheless the sensitivity is expected to be limited by DNA immobilization and hybridization probabilities which are determined by the surface modification technique and applied protocol. Improving those can lead to much smaller detection limits, such as aM level as stated above.

Keywords: DNA, microarray, single nucleotide polymorphism, charge sensor.

ÖZ

DNA TESPİT UYGULAMALARI İÇİN CMOS ENTEGRE SENSÖR OKUMA DEVRESİ

Musayev, Javid

Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü

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Eylül 2011, 103 sayfa

Bu çalışmada DNA ve benzeri biolojik örnekleri tespit edebilir CMOS entegre sensör çipi sunulmuştur. Çipin algılayıcı kısmı 15 µm büyüklüğünde piksellerden oluşan 32 X 32 dizinden ibarettir. Piksellerin üzerinde iletilen veya indüklenen yükü yüksek hassaslıkla algılaya bilecek, CMOS işleminin üst metalinden oluşan 5 µm X 5 µm büyüklüğünde elektrotlar bulunmaktadır. Bu çalışma kapsamında aynı zamanda analog sensör sinyalini sayısal sinyale çeviren ADC içeren, ve bilgisayara bilgi gönderecek ve bilgiyi kaydedecek olan FPGA'le uyumlu çalışacak dış devre elektroniği de tasarlanmıştır.

Toplam sistemin gürültü seviyyesi 6.7 e^- (elektron) olarak ölçülmüştür, ve bu değerin daha hızlı örnek alma sonrasında 5.1 e^-'a düşebileceği gösterilmiştir. Mikrodizinlerde kullanılan DNA'ların genelde 10-20 nukleotitten oluştuğu ve bir nukletidin 1 veya 2 elektron taşıdığı düşünülürse belirtilen gürültü seviyesinin DNA tespit uygulamaları için çok uygun olduğu anlaşılır. Bir kadraj okuma süresinde (20 ms) ölçülebilir en fazla electron sayısı 24603'tür, bir başka deyimle ölçülen dinamik aralık 71 dB'dir. Ölçülen sızıntı miktarı 31 elektrondur, fakat

sızıntı miktarının tahmin edilebilir olduğu için çipin hassasiyetine ciddi bir kötü etkisi bulunmamaktadır.

Elektronik performans ölçümlerinin yanısıra, çiple DNA testleri de yapılmıştır. Piksellerin karşılıklı etkileşimini önlemek için, çip yüzeyi nitrit passivasyon katmanıyla kaplanmış, ve DNA tutunması için üzerine APTES polimeri serilmiştir. DNA tutunma ve hibritleşmesi deneyleri sırasında 5'-TCTCACCTTC-3' ve bunun karşılığı olan 3'-AGAGTGGAAG-5' serileri kullanılmıştır. 1 pM yoğunluklu çözeltide yapılmış olan hibritleşme 13 µM yoğunlukta yapılmış olan tutunmaya göre daha fazla durgun durum sızıntı akımına neden olmuştur. Bu sayede tamamen uyumlu ve tamamen uyumsuz DNA dizimlerinin ayırt edilebileceği gösterilmiştir. Bildiğimiz kadarıyla, şimdiye kadar literatürde etiketlenmemiş CMOS DNA mikro dizinlerinde pM yoğunluğunda DNA tesbiti rapor edilmemiştir, ve bu yoğunluk derecesi çok hassas olan QCM ve floresan görüntüleme yöntemleriyle kıyaslanabilinir düzeydedir. 1 pM yoğunlukta algılama aygıtın teorik performans limiti değildir ve elektronik devrenin gürültü seviyyesi dikkate alınırsa, 6.7 e^- hassaslık seviyesi teorik olarak aM gibi çok daha hassas ölçümlere yol açabilir. Hassasiyetin DNA tutunma ve hibritleşme olasılıklarıyla sınırlı olacağı beklenmektedir ve bu olasılık yüzey değişikliğine ve uygulanan protokole bağlıdır. Bu kriterleri iyileştirmek belirtildiği gibi aM kadar düşük algılama seviyelerine yol açabilir.

Anahtar kelimeler: DNA, mikrodizin, tek nukleotit polimorfizmi, yük sensörü.

To my mother

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I would like to thank my friend Burak Eminoğlu for his company during endless tape-out nights, and for his enthusiastic help attempts regarding problems I had encountered during analog IC design. I am also grateful to Dinçay Akçören for his precious help in drawing the PCB for the external circuitry, and in writing Verilog and C++ codes for test purposes. His contribution saved a considerable amount of time and helped me better understand these tools.

I want to thank Mikro-Tasarım San. ve Tic. Ltd. Şti. for its support during the design phase of the DNA sensor chip developed in this thesis.

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CHAPTER 1

INTRODUCTION

Deoxyribonucleic acid (DNA) is an essential macromolecule carrying the genetic code of living organisms. This genetic code, also called gene, is a huge amount of information contained within chromosomes, which is used to synthesize proteins and define their function. Because of the highly polymorphic structure of the DNA, people can have different specific sequences for a typical protein. This leads to a different level of activity in the protein, thus susceptibility of an individual to the diseases influenced by the function of that protein changes. Polymorphisms (sequence variations) of genes may result in inherited or acquired genetic disorders. These can be either inherited single gene disorders that affect an individual from birth or shortly thereafter, or multi-factorial disorders that make an individual disease-prone because of his/her genetic structure. Cancer, diabetes, cardiovascular diseases, Alzheimer disease and respiratory disorders are examples of such multi-factorial disorders and even if not inherited, such diseases are of genetic origin [1]. In this respect, genetic testing has become an important part of molecular biology in recent years and a lot of effort was spent to develop reliable, cost effective, and portable tools for DNA mutation analysis.

Other than recognizing genetic disorders, DNA mutation detection is useful in identifying genetically modified products, or food ingredients containing genetically modified organisms [2]. But the most important contribution of DNA detection is expected to be in the personalized medicine.

This is a new research area, also called pharmacogenomics, where genetic structure of an individual is analyzed to define and predict an individual's response to certain drugs, and thereby prescribe the most suitable one. Nutrigenomics is another field investigating the relation between individual's genome and nutrition, hence providing personalized diet. Analyzing individual's genes can also help to diagnose in time and prevent multi-factorial disorders.

This thesis presents implementation of a CMOS integrated sensor chip for DNA immobilization and hybridization detection. Detection relies on the pre-sensing and sensing charge detection, as described in the patent application [3]. The chip consists of a 32 X 32 pixel array with the pixel structure similar to a 3-T pixel of CMOS image sensors [4]. Detection relies on DNA backbone charge sensing, and the noise level is measured to be less than 7 e^-. With its array structure and high sensitivity, this chip has a potential to be utilized as a DNA microarray, exceeding the sensitivity limit of the most sensitive gravimetric and optic detection methods, which are described in the following sections of this chapter.

1.1 DNA Structure

DNA is a molecule strand formed by 4 types of nucleotides: adenine, thymine, cytosine and guanine (*A, T, C*, and *G*). The sequence of these nucleotides in a strand defines the genetic code. Nucleotides are composed of three building blocks, which are sugar deoxyribose, a phosphate group and a nitrogen containing base (Figure 1.1). Sugar-phosphate group forms the backbone of the strand, while bases determine the type of a nucleotide. Phosphate groups in the backbone of a DNA carry negative charge of 1 or 2 e^- per nucleotide, depending on the pH of the ambient solution [5]. *A* base of a DNA can form hydrogen bonds with a complementary base. *A* is a complement of *T* base, and *G* is a complement of *C* base.

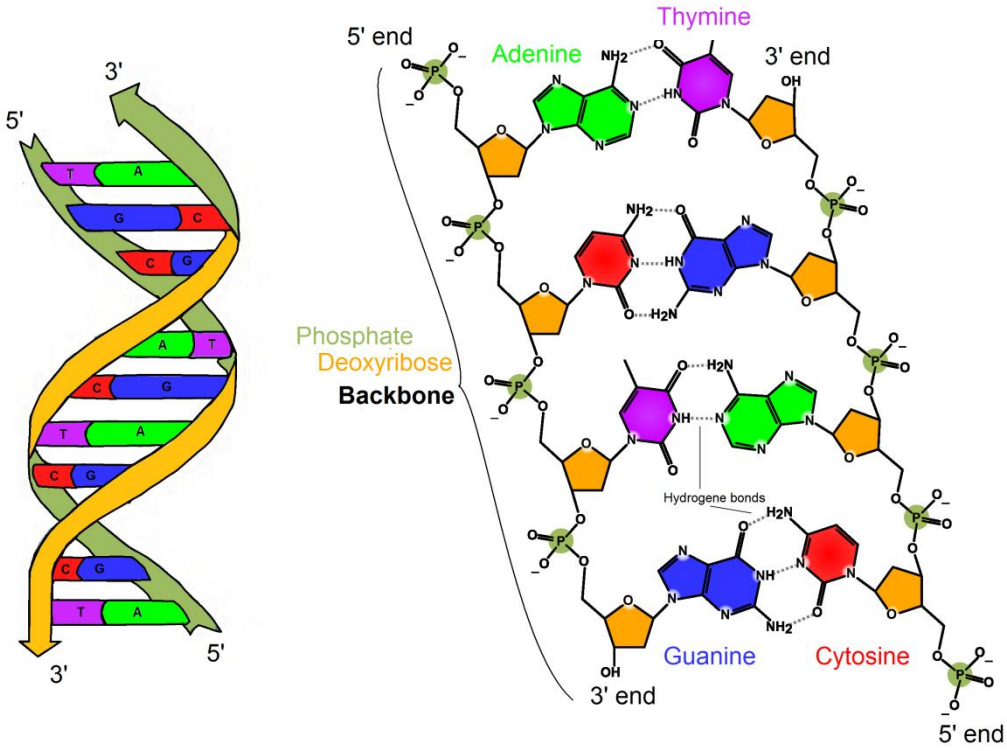


Figure 1.1: Structure of a double stranded DNA.

In case of matching codes, two single stranded DNA molecules (ssDNA) attach to each other (hybridize) by forming such bonds and compose a helical double stranded DNA (dsDNA), as was discovered by James Watson and Francis Crick [6] in 1953. This utility is the basis of the genetic code transcription and translation. A DNA strand has an orientation "from 5' to 3' end", where the former indicates the side with a phosphate group at 5' carbon, and the latter indicates the side with a hydroxyl group at 3' carbon of a nucleotide. In a dsDNA the two strands have an antiparallel orientation.

1.2 Single Nucleotide Polymorphism

The aforementioned term "polymorphisms" indicates changes (mutations) in the sequence of a DNA which can be insertion, deletion, or replacement of a nucleotide. Single nucleotide polymorphism (SNP) is the

mutation of one the nucleotides in a gene. If the replaced nucleotide has much different size, polarity and electrical charge, SNP can change the activity of a protein and result in a disorder or an adverse drug effect. About 15 million SNP's have been characterized in a human genome [1], and SNP detection in a lowest DNA concentration has been a major focus in DNA detection devices and especially microarrays. The conventional SNP detection relies on the statistical approach, so that SNP reduces the bonding force between the two strands and decreases the probability of hybridization. Thus, whatever the detection technique is, the difference between the full match and partial mismatch cases is detected. Generally 10 to 20 base pair long DNA oligonucleotides are used in SNP detection microarrays, so it becomes possible to identify SNP, however it would be much harder to detect SNP in longer sequences, because contribution of a single nucleotide to the overall bonding force would be small.

1.3 Conventional Detection Techniques - Microarray Technology

As in all fields, development of the micro-technology had a revolutionary effect on molecular biology. Introduction of DNA microarrays in 1990s has rendered genome wide screening and thereby detection of disease markers possible. Thousands of different oligonucleotides (probes) are attached to different spots on a solid surface (e.g. silicon or glass substrate) with very accurate robotic pins, and a target of interest is introduced to the surface [7]. In case of matching codes hybridization occurs more rapidly, and matching sides are identified (Figure 1.2). A conventional strategy is to use fluorescent tags for the hybridized target identification [8-13]. Variants in the HIV genome [9,10], human mitochondria mutations [11,12], β-talassemia and glycose-6-phosphate dehydrogenase deficiency [14] are among mutations detected with this technique so far.

The fluorescent detection technique is very sensitive but requires expensive chemical tags and an optical setup. Despite its sensitivity, this method requires visual inspection, therefore might be error prone unless a sophisticated image processing software is used.

Mass spectrometric methods [15-17] are label free and very sensitive techniques that can detect DNA due to the change in mass upon hybridization. Quartz Crystal Microbalance [16,17] is the most common mass spectrometric method used in DNA detection. In this method, DNA probes are immobilized on a gold electrode of a quartz resonator. Mass attached to the electrode changes the resonance frequency of the crystal, thus a hybridized DNA can be sensed.

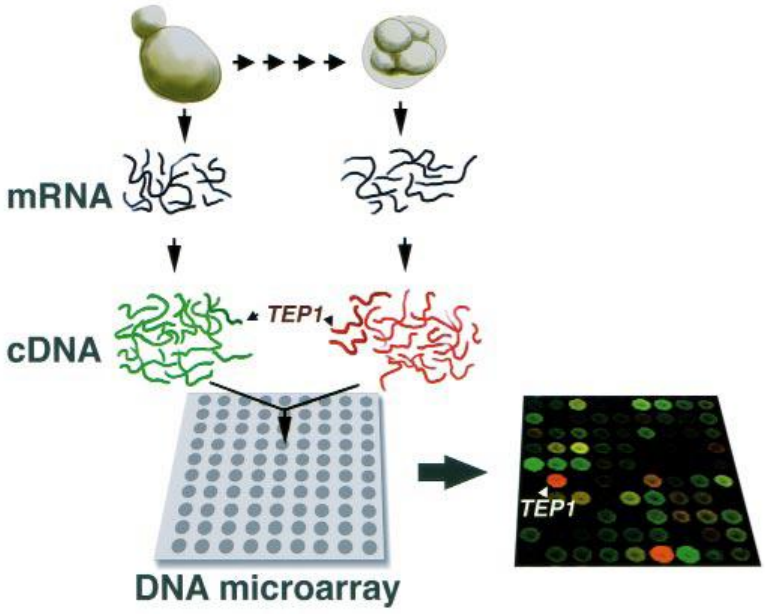


Figure 1.2: RNA sample is taken from two different cells, marked with different colors, mixed and added to the microarray with different genes at each spot. Color dominancy indicates grater relative abundance of the corresponding gene in a sample. For example TEP1 gene is more frequent in the RNA marked with red tags [18].

The sensitivity of this method can reach ng/mL levels corresponding to pM concentrations depending on the size of the DNA molecule. The drawback of mass spectroscopic methods is the need for expensive external equipment and mechanical structures (like quartz resonators or mechanical cantilevers [19]) which are not very suitable for the microarray applications.

Surface Plasmon Resonance (SPR) is another optical, but label free method to detect the DNA hybridization [20-22]. It is not as sensitive as QCM but can be easily applied to microarray structures. The operation principle relies on the change of refractive index and surface plasmon properties of the surface containing probe DNA molecules, as both thickness and the dielectric constant of the surface changes after hybridization. Reflection patterns and the angle of the reflected light are observed to get the data. With this method DNA of nM concentration can be detected [23], although with some enzymatic amplification detection limit of fM concentration is also reported [24]. The disadvantage of this method is obviously SPR optics that obstructs portability of the system and increases the cost.

Another optical detection technique relies on interferometric properties of the light reflected from the microarray surface [25,26]. In case of hybridization, variation in surface properties results in different interference patterns observed with a CCD camera. This system can sense µM concentration of DNA, and requires optical setup as well.

A much more sensitive optical detection method uses nanometallic labels instead of fluorescent tags [27]. A microarray is implemented on a CMOS image sensor, and labeled target DNAs are detected due to the opacity of silver enhanced gold nanoparticles, which prevent light incident on a microarray chip. The sensitivity to a 10 pM target concentration is reported for this method.

1.4 Electrical Detection Techniques

Some of the detection techniques mentioned above are quite sensitive, however, none of them provide means to produce a portable, low cost, and easy to use device, because they require either bulky and expensive optical setups or enzymatic additions. Therefore, in the last 10 years, a lot of effort was spent to merge microarray technology to a CMOS/MEMS compatible platform. Then, it would be possible to miniaturize the system and use a smart CMOS circuitry to get rid of the labeled detection. Electronic properties of DNA and their variation with the hybridization event are taken advantage of, to realize such sensor microarrays. There are two main types of electrical detection, which are explained in detail below. The first one relies on the impedance variation at the DNA-electrode interface and the second one takes advantage of a DNA phosphate backbone charge to detect hybridization.

1.4.1 Impedance Based Detection

There are several types of impedance measurement techniques to detect hybridization. The first method is to label target oligonucleotides with redox (reduction-oxidation) enzymes. The current between the two electrodes of a microarray pixel would increase upon hybridization due to chemical properties of a redox enzyme (Figure 1.3). The generated current is detected with CMOS readout circuitry, eliminating the need for an optical setup.

Another technique is to apply coulostatic pulses to the electrode with a probe DNA in presence of a redox activated solution and measuring the relaxation time [28]. The relaxation time is a function of interface impedance, so dsDNA can be differentiated from ssDNA due to the change in the solution-electrode interface impedance. The best sensitivity achieved with this method is the detection of 0.1 μM DNA concentration.

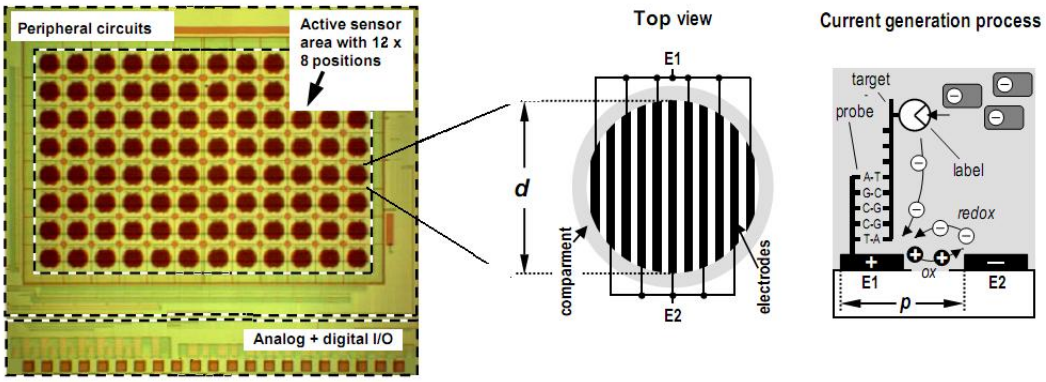


Figure 1.3: Current measurement in a microarray between the two electrodes. If redox enzyme labeled target hybridizes to a probe, current increases because interface impedance reduces due to redox ions [29].

To get rid of the redox enzyme, different surface modifications can be implemented on electrodes to make the interface more sensitive to surface variations [30,31], but in this case, the process becomes less CMOS compatible and implementation of electronics gets harder. Therefore, the electrochemical impedance spectrometry (EIS) is used to define the interface impedance. This requires a device to perform EIS, so the overall cost increases and portability of the system becomes compromised.

C. Guidicci *et. al.* introduced a new method based on the interface impedance detection between two electrodes [32]. She proposed an impedance model for the interface (Figure 1.4) and has shown that it is dominated by capacitance, which decreases upon hybridization. This structure was extended to a CMOS microarray, where readout circuitry was used to determine capacitance changes [33,34]. This method found an extensive use in CMOS microarrays. Different readout techniques were utilized. Generally RC ring oscillators were used, where resonance frequency depends on the value of the interface capacitance Cp [35-40].

Another electrical detection method is to sense the DNA presence due to the charge of its sugar-phosphate backbone, like was done in this study as well. The following subsection summarizes devices relying on this sensing principle.

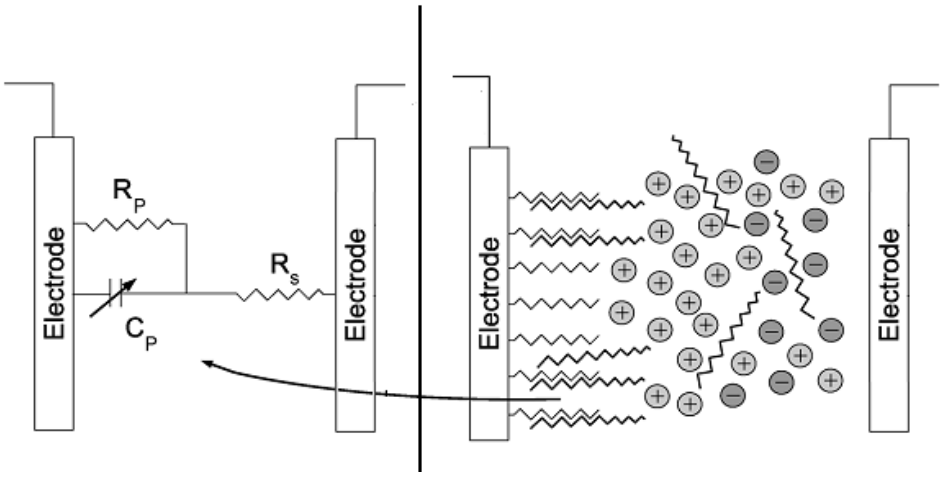


Figure 1.4: Impedance between the two electrodes can be modeled by series resistor Rs, and parallel resistor and capacitor Rp and Cp. Cp dominates for this kind of structure. After hybridization the distance between the electrode and the solution ions increases resulting in the decrease in capacitance [34].

1.4.2 Phosphate Backbone Charge Based Detection.

Phosphate backbone of a DNA nucleotide possesses a negative charge of 1 or 2 e^- depending on the pH of the solution it is located in. During hybridization the number of nucleotides increases, therefore this phenomenon can be used as a detection mechanism. Ion sensitive field effect transistors (ISFET) are used to sense this negative charge of a DNA [41-47]. ISFET's are MOS transistors with floating gate modified so as to be available for the DNA immobilization (Figure 1.5). Attached DNA molecules modify the threshold voltage due to their negative charge, which in turn affects current flowing through an ISFET. Current variations are interpreted as DNA detection. Thickness of the gate oxide determines the sensitivity of ISFETs, and generally

they are able to detect µM concentrations. Diamond field effect transistors are used to improve sensitivity, since that structures do not have any gate oxide and DNA probes attach right above the diamond gate [43]. With this method SNP was detected in 100 pM DNA solution and 3-mer mismatch was detected in 10 pM solution. Although this method provides very high sensitivity, an unconventional process is required to form such ISFETs, increasing the cost of the overall system.

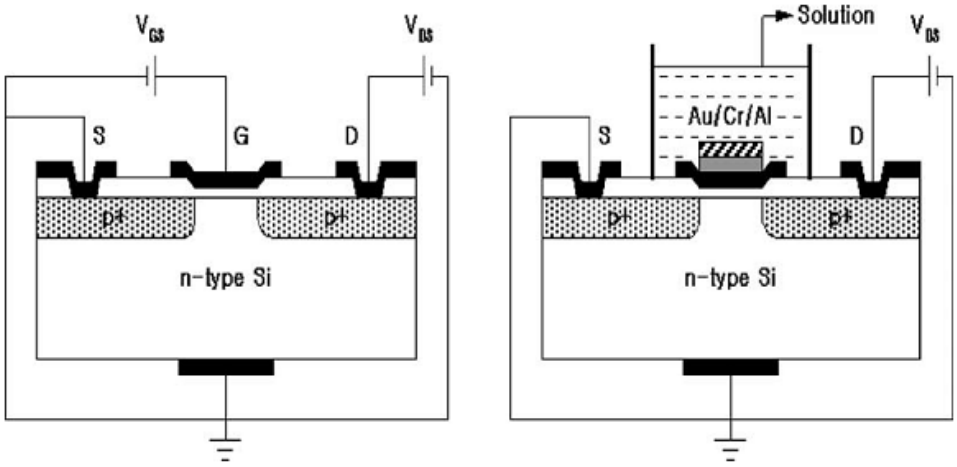


Figure 1.5: Comparison of MOSFET and ISFET Structure, gate of the ISFET is modified with gold for DNA immobilization and is left floating so that DNA backbone charge can regulate the FET current [48].

J. Fritz *et. al.* [49] has used an alternative charge detection method. He immobilized and hybridized DNA on negatively doped cantilevers. A depletion region was generated on the interface of the DNA and cantilever. Depletion capacitance was measured to get an idea about the DNA charge. SNP was detected in a 2 nM concentration with 12-mer oligonucleotides.

Advancement in nanotechnology has boosted DNA detection techniques as well. Electrical properties of carbon nanowires and nanotubes are very sensitive to environmental factors. New devices have been fabricated using this

idea in recent years. Carbon nanowires are grown between two gold electrodes, and DNA is immobilized on the nanowire [50-52]. Impedance of the nanowire is measured, and since it is very sensitive to its ambient, hybridization can be detected in a very low concentration. Generally sub-pM concentration is achieved, but in one particular example 10^{-16} M detection is reported [53].

A microarray relying on a different charge sensing mechanism was fabricated by E. Anderson *et. al*. [54-56]. He has implemented an in pixel CTIA to detect induced charge during DNA polymerization (Figure 1.6). There is no ohmic contact between the DNA and the detector metals, but when the DNA approaches to the surface, some surface charge density appears on those metal electrodes of the pixels. This charge flows through integration capacitor and results in an output voltage change. The capacitance value is chosen to be 30 pF in this design, and the noise floor results in a 0.35 fC detection limit, corresponding to 2203 e^-. Correlated double sampling is claimed to be ineffective due to dominating solution buffer noise, and the capacitance value is not reduced below 30 pF to prevent an early saturation of the opamp. Hybridization of DNA with a 500 nM concentration was detected in that study.

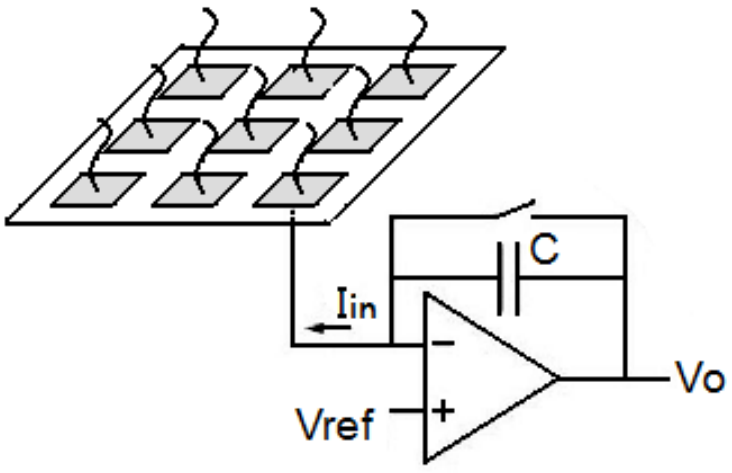


Figure 1.6: A microarray with in pixel CTIA. Charges induced to the microarray detector metals flow through capacitor and change the output voltage [54].

1.5 Detection Method Implemented in This Study

The DNA detection chip designed in METU relies on the operation principle similar to a 3-T image sensor [4]. In the pixels of image sensors, active photodiode area captures photons, thus electron hole pairs are generated and photon is sensed. In our design, we did not implement a photodiode, but instead connected the sense node to the metal detector of the microarray. DNA would be immobilized on those metal detectors and charges resulting from hybridization would be sensed as if they were photon induced carriers. The sense node capacitance in our design may be thought to be equivalent to the integration capacitor of the CTIA microarray described above, but in our design capacitance of the sense node is chosen as 6 fF to increase sensitivity, and CDS is implemented to eliminate the reset noise. Although it was claimed that reducing capacitance and implementing CDS would not lead to better results [56], we have achieved 7 e^- measured noise level, which is 315 times better than the result obtained in literature [56]. Our aim is to detect hybridization in 1 pM DNA concentration. This kind of sensitivity has not been reported to best of our knowledge with label-free CMOS DNA microarrays and it is very close to the sensitivity of the most sensitive QCM or carbon nanotube utilizing methods.

Thesis organization:

Chapter 2 deals with the architecture of the CMOS sensor readout circuit by giving detailed description of the circuitry and operation principle of analog and digital blocks.

Chapter 3 provides theoretical analysis and simulation results of the system noise and leakage, which are the two metrics defining performance of the system.

Chapter 4 is dedicated to electronic functionality and performance tests. Measured noise and leakage values are given in that chapter. External electronics and the test setup are also described there.

Chapter 5 explains surface modifications required to perform DNA tests, provides testing method and its results for the two tests, namely single pixel and multi pixel tests.

Chapter 6 concludes the thesis by summarizing and stating the importance of conducted work, also defines future research objectives to increase the performance even further.

CHAPTER 2

ARCHITECTURE OF THE BIOMEMS DNA SENSOR CHIP

This chapter deals with the detailed description of the BioMEMS DNA Sensor (BMDS) chip. BMDS contains a 32 X 32 pixel array of 15 µm pixel pitch, with detector top metals of 5 µm X 5 µm size on each pixel. The chip is able to detect charges induced on or transferred to those detectors. It also contains analog circuitry to properly bias the pixels and digital circuitry to maintain the control of the system. The noise of the chip is on the level of few electrons, which enables a sensitive detection of an immobilized or hybridized DNA. A voltage proportional to the charge difference appeared on the pixel due to biological interactions is obtained at the output. The chip consists of analog and digital parts that execute described tasks. The following sections explain their design procedure and operation.

2.1 Analog Circuitry Architecture

There are two basic analog blocks in the chip. The first one is a 32 X 32 pixel array consisting of 1024 identical pixels. Internal circuitry of the pixel is responsible for converting incoming charge to voltage, then buffering and transferring this voltage to the column bus. The other block is the analog circuitry providing pixels with the required bias current. The next two subsections provide detailed description of the analog blocks.

2.1.1 Pixel Structure

Internal structure of the pixel is very similar to a 3-T CMOS image sensor pixel [4] and is shown in Figure 2.1. The main difference is the absence of a photodiode at the sensing node, which is instead connected to the top metal detector. This metal detector surface is modified to enable DNA immobilization, by post CMOS processing as described in Chapter 5. During an immobilization or hybridization process DNA molecules that have negatively charged phosphate backbone induce their charges on the detector plate and due to the capacitance of the sense node C_d, a voltage difference proportional to this charge is generated at the gate of M2 transistor of Figure 2.1. In order to define this voltage difference, initial voltage of the detector must be known. Therefore, pixels are reset to some initial voltage V_{ch} before charge integration. This voltage is transmitted to the C_d through M1 NMOS switch controlled by the digital V_{set} signal.

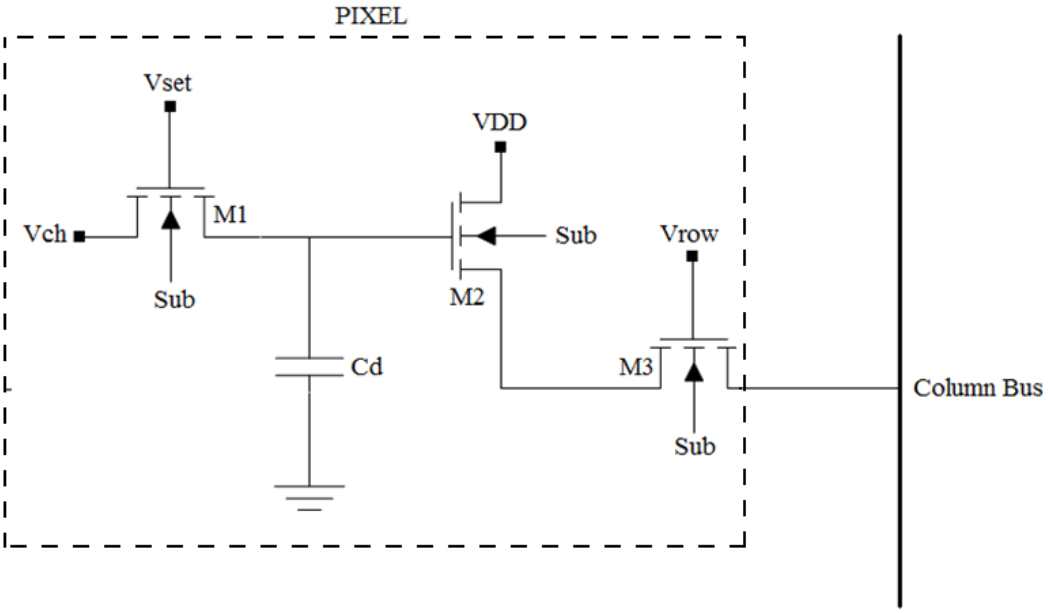


Figure 2.1: Pixel structure of the chip. M1 is the pixel reset switch, M2 is the pixel source follower and M3 is the row switch transistor that transfers the pixel data to the column bus.

It is better to use only NMOS transistors inside a pixel to minimize its area. Therefore the inequality,

$$V_{ch} < V_{DD} - V_{TN} \quad (2.1)$$

where V_{DD} is the supply voltage and V_{TN} is the threshold of the NMOS switch M1, must hold considering that the V_{set} signal cannot exceed V_{DD}. This condition is satisfied by setting V_{ch} to 2.4 V. It is better to set the voltage of C_d (V_{Cd}) to a maximum value in terms of dynamic range, because integrating electrons discharge C_d and reduce V_{Cd}. Then, assuming V_{TN} to be 0.6 V, maximum V_{ch} can be 2.7 V in 3.3 V CMOS process. But as explained in section 2.1.2, due to the restrictions introduced by the bias circuitry, V_{Cd} can range between 1.57 V to 2.71 V according to CADENCE Spectre dc simulations. Violating these limits pushes one of the biasing transistors into linear region. Consequently, V_{ch} is selected in between these values to leave some margin to the edge of saturation, but closer to the upper limit to increase dynamic range. During normal operation, V_{set} is low and detector is disconnected from V_{ch} voltage. In this case V_{Cd} is sensitive to any charge variation on the detector metal plate. Assuming that the source follower M2 transistor is properly biased, it buffers the V_{Cd} voltage to the column bus. Bias is provided by the current flowing through M2 when M3 transistor switch is on. This transistor is controlled with the digital signal V_{row} that realizes row selection. When a row in the array is active, all pixels in that row transmit their V_{Cd} voltages to the corresponding column buses. Further selection, which is column discrimination, is done by column transistor switches, located outside the pixel area as explained in the next section. Hence, just one pixel's V_{Cd} is transferred to the output at a time.

The biasing is provided by the current sources as described in Section 2.1.2. When a pixel is active, the biasing current flows through it and due to

the V_{GS} potential of M2 source follower transistor, voltage on the column bus becomes equal to

$$V_{col} = V_{Cd} - V_{GS2} \quad (2.2)$$

Since the matter of interest is the voltage difference created at the sensing node and V_{GS2} is fixed by the bias current, the change in V_{col} can be assumed to be equal to the change in V_{Cd}. Still, V_{GS2} loss is compensated with some circuitry outside the pixel, which also improves capacitive load driving capability at the output, as revealed in the section 2.1.2.

The critical point in the design of the pixel is selection of the value of the detector capacitance C_d. First of all, accumulated charge Q generates voltage difference on this capacitor, equal to

$$\Delta V_{Cd} = \Delta Q / C_d \quad (2.3)$$

So, making C_d small increases conversion gain, which is the amount of voltage difference induced by one electron. On the other hand, each time C_d capacitor is set to V_{ch} potential, due to the thermal noise of M1 transistor after the reset operation, reset noise is generated on the capacitor. As explained in Section 3.1.1 larger capacitance results in larger charge noise, so it is reasonable to keep C_d small for better noise performance as well. Capacitance should be as small as possible to make the conversion gain greater than the noise level to achieve required resolution. Actually, in order to achieve the smallest capacitance possible, no physical capacitor is implemented inside the pixel. The capacitor is formed by the gate capacitance of M2 and the parasitic capacitances which are around 3.78 fF and 2.275 fF respectively as observed in dc simulations and parasitic extractions. The total capacitance is 6.055 fF which corresponds to 26.42 µV/e conversion gain. The reset noise is around 30 e^-, which is much higher than the desired noise performance, but since correlated double sampling (CDS) is implemented, the reset noise eventually becomes of no

importance. Other major sources of noise are the flicker noise of M2 transistor and the thermal noise of the bias circuitry. It is possible to minimize the latter as described in Section 3.1.2. Actually 81.2% of the overall noise is the flicker noise of M2. Reducing transistor gate area increases the flicker noise but increasing dimensions of M2 would reduce conversion gain due to the increase in the gate capacitance. Consequently, if the gate area was increased, SNR would decrease, because order of conversion gain decrease is greater than the order of flicker noise reduction with respect to the gate area increase (Section 3.1.3). Considering these tradeoffs and by making iterative simulations to find the optimum point, dimensions of M2 are selected as in Table 2.1.

Table 2.1: Dimensions of the pixel transistors (M1-M3), and the column select switch transistor (M4).

	M1	**M2**	**M3**	**M4**
W/L (µm/µm)	0.4/0.5	1.5/0.7	0.7/0.35	1.4/0.35

For these dimensions and 5 µA bias current V_{GS2} becomes 1.08 V. Another advantage of not making M2 minimum length is a better output resistance. In 0.35 µm CMOS process 0.35 µm is the minimum achievable transistor length and the output resistance of a transistor improves significantly if its length is increased. This provides better buffering performance for M2 so that the gain becomes closer to unity and more linear due to reduced channel length modulation effect. Other pixel transistor dimensions are shown in Table 2.1 as well. The width of M1 switch is minimized to reduce the leakage as explained in section 3.2.2. M3 switch has minimum dimensions to reduce the pixel area. The layout of the pixel, which has 15 µm pitch, is shown in APPENDIX A.

2.1.2 Bias Circuitry

The bias circuitry is an important part of the analog circuitry, which can be represented with one pixel, column select transistor switch M4, a simple output buffer to drive the output capacitive load and compensate for V_{GS2}, and current sources as shown in Figure 2.2, where digital signals are shown in red.

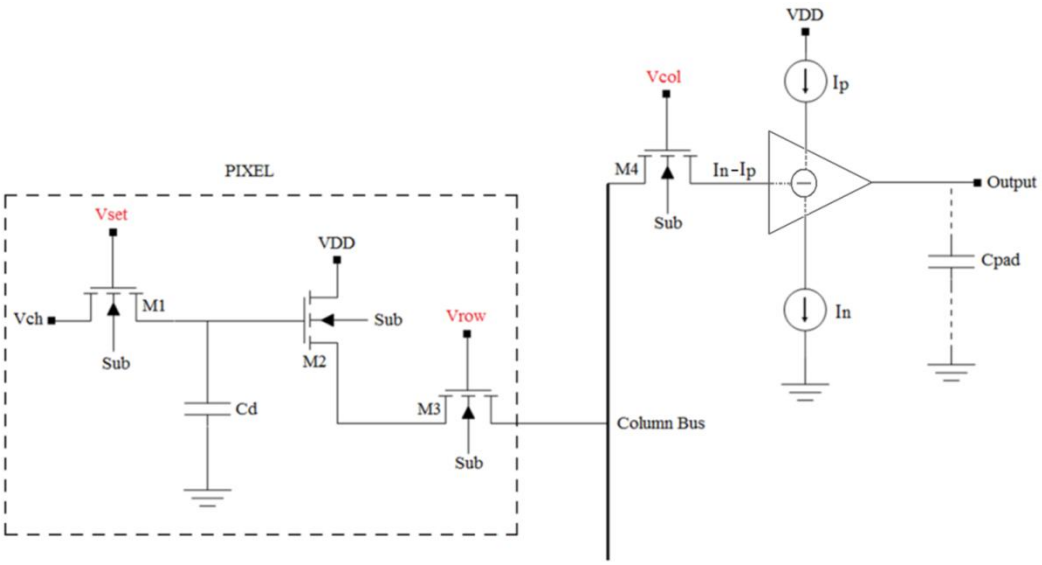


Figure 2.2: Symbolic schematic of the analog circuitry of the chip. The analog block consists of a pixel, column select transistor switch (M4), the output buffer to compensate for V_{GS2} and to drive the output load, and two current sources.

The output buffer can be represented with four terminals. I_n and I_p feed the two supply terminals, output terminal drives the output load with I_n and I_p, and $I_n - I_p$ amount of current is drawn to input, which also passes through the source follower of the pixel (M2), and biases it, when both V_{row} and V_{col} signals of a pixel are high. Therefore, the voltage equal to

$$V_{in} = V_{Cd} - V_{GS2} - V_{DS3} - V_{DS4} \qquad 2.4$$

appears at the input of the buffer. After compensating for the voltage drop as noted above, the voltage at the output of the buffer becomes equal to,

$$V_{out} = V_{Cd} - V_{GS2} - V_{DS3} - V_{DS4} + V_{comp} \quad (2.5)$$

Another advantage of this structure is the fact that I_p can be relatively large when compared to $I_n - I_p$, which is the pixel bias current, and can drive larger output capacitive loads. It is selected as 25 µA. With this amount of current and a proper buffer design, V_{comp} becomes 1.145 V. This compensates for both V_{GS2} and $V_{DS3} + V_{DS4}$ which are around 1.081 V and 32.5 mV respectively. There is only one output buffer in the chip, so it does not contribute to the overall area much.

Since, $I_n - I_p$ is 5 µA, I_n must be 30 µA. Digital circuit is operated with 100 kHz clock, and a single pixel is read in 10 µs. Assuming 20 pF C_{pad} capacitance and noting that V_{out}=2.43 V, less than 2 µs is enough to charge C_{pad} in worst case (from 0 to V_{out}) according to Eq. 2.6. So, I_p= 25 µA is enough to drive the output load.

$$T_{charge} = \frac{(C_{pad} * V_{out})}{I_p} = \frac{20\ pF * 2.43\ V}{25\ \mu A} = 1.994\ \mu s \quad (2.6)$$

Two current sources are required to realize the biasing. One is I_n which generates 30 µA current between ground and a given node. The other one is I_p which generates 30 µA current between V_{DD} and a given node. A simple current mirror structure illustrated in Figure 2.3 is implemented for this purpose. The reference current I_{ref} is generated by adjusting external resistor R_{ext}. Resistor R is implemented inside the chip for the protection purpose. The current is not directly mirrored, but n-pair to p-pair and p-pair to n-pair transitions are used as can be seen from Figure 2.3. That is instead of connecting M11 gate to M6 gate and M16 gate to M8 gate, transition stages M7-M8-M9-M10 and M12-M13-

M14-M15 are used in each case respectively. This is done to make I_{ref} current less sensitive to variations resulting from the load, so that I_n and I_p loads do not affect each other. To clarify, assume that due to some undesired effect gate voltage of M11 has changed.

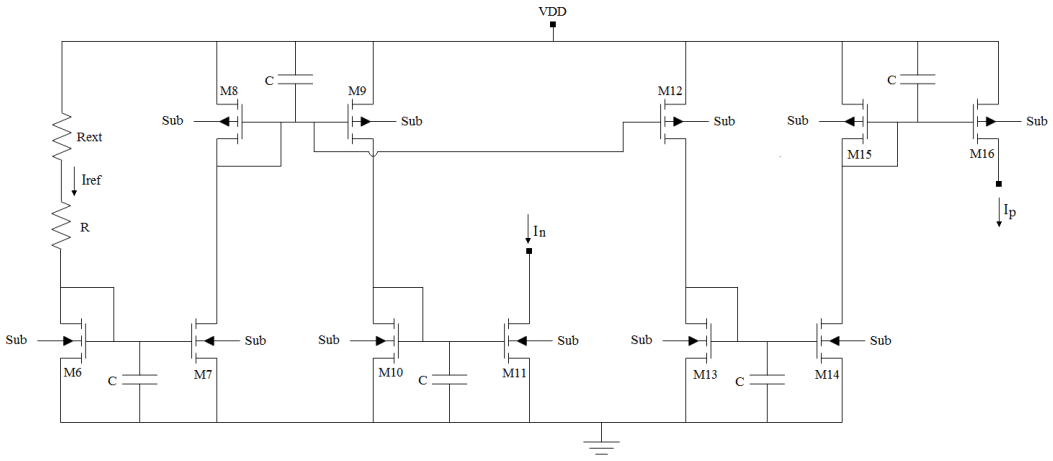


Figure 2.3: The current mirror circuitry generating the two current sources I_n and I_p, by mirroring a reference current I_{ref}. R is the resistor implemented inside the chip and R_{ext} is an external resistor.

Then the gate of M10 will also be affected since they are the same, and considering that M10 is diode connected and always is in saturation, its current would change. However, this would not affect M9 gate voltage since it is fixed by M8. Eventually, I_{ref} would not be affected. For each current mirror stage, capacitance of 2 pF is connected between the gate and source so as to prevent sudden V_{GS} variations like glitches or coupled noise. I_{ref} is selected as 200 µA, transistor and resistor values are shown in Table 2.2. The values are chosen so as to minimize the current source noise, and provide required voltage swing. The overdrive voltage of M11 limits the minimum output voltage, while the overdrive of M16 limits the maximum output voltage, and according to dc simulation results the output voltage can range between 1.57 V and 2.71 V.

These matters are addressed in Section 3.1.2. It is shown that the noise contribution of the bias circuitry accounts for less than 20% of the overall noise.

Table 2.2: Dimensions of the transistors and resistor values used in the design of bias circuitry.

	M6	**M7**	**M8**	**M9**	**M10**	**M11**	**M12**
W/L (µm/ µm)	$\frac{85}{15}$	$\frac{85}{15}$	$\frac{80}{20}$	$\frac{80}{20}$	$\frac{75}{15}$	$\frac{15}{20}$	$\frac{80}{20}$
	M13	**M14**	**M15**	**M16**	**R**	**Rext**	
W/L (µm/ µm)	$\frac{80}{20}$	$\frac{20}{20}$	$\frac{70}{15}$	$\frac{35}{15}$	4.2kΩ	6.03kΩ	

2.2 Digital Circuitry Architecture

To better understand the function of each digital block the overall operation of the chip is described first. The smaller chip with 2 X 2 pixel array is shown in Figure 2.4. Digital blocks are the control unit, column and row registers, and the timing and buffer circuitry. The control unit arranges timing and control signals for the registers. The row and the column registers activate one column and one row, thereby enabling only one pixel at a time. The whole array is scanned sequentially. The timing circuitry prevents overlaps during register shift operation, and buffers are used just for safer and faster operation. Initially, all pixels are reset to V_{ch} potential and the whole array is scanned. Then, pixels are read once more, this time without being initially reset. The voltage difference between the two readings corresponds to the voltage difference generated on detectors resulting from induced or transferred electrons.

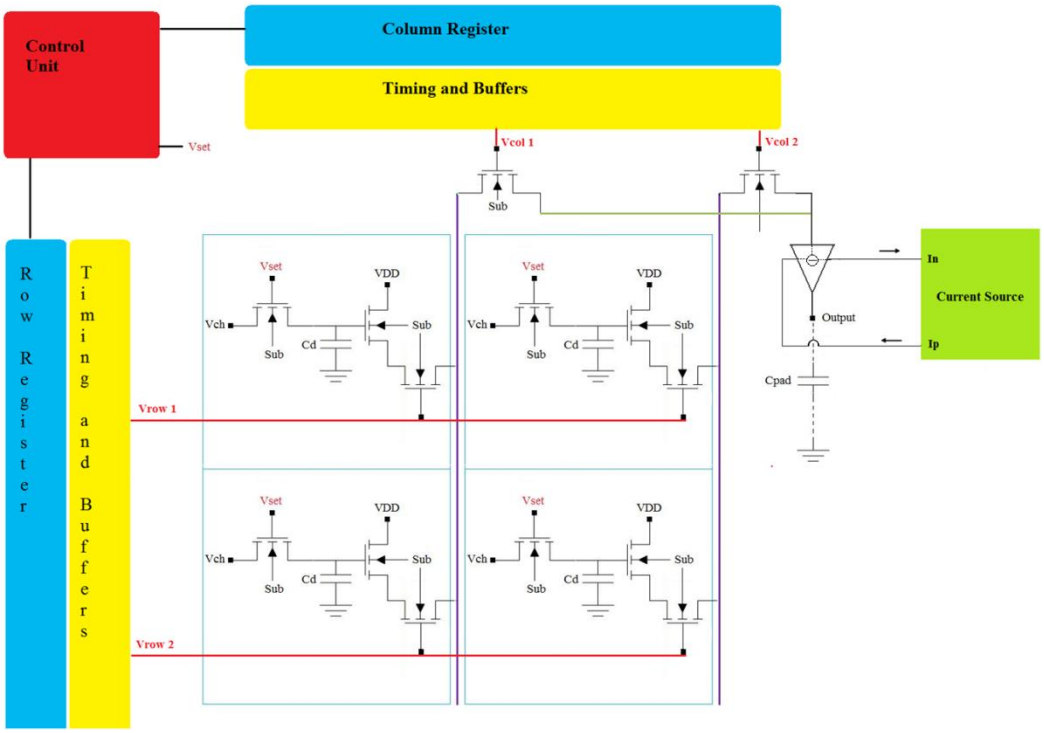


Figure 2.4: A system with a 2 X 2 pixel array representing interconnections of all digital and analog blocks of the chip.

By this manner CDS is done as well, and aforementioned reset noise explained in Section 3.1.1 is eliminated. Another factor which results in an error at the output is the pixel leakage. In Figure 2.1 M1 transistor is a switch which charges C_d capacitor to V_{ch} when V_{set} is high. When V_{set} becomes low, ideally M1 would be off and C_d capacitor would keep its charge. However in practice there are two leakage sources, which cause capacitor C_d to gradually discharge. To minimize the effect of leakage, C_d capacitor is reset between every two readings. Consequently, to get the output, the array is read twice, first time with resetting all pixels and the second time without resetting. Then leakage time is reduced to array scan time, which is 10 ms in this case for 32 X 32 array with clock frequency of 100 kHz. As simulation results shown in Section 3.2.2 reveal, during this period the amount of leakage corresponds to approximately

3.6 e^- (although measured leakage came out to be 31 e^- as revealed in Section 4.2.2). These requirements give us an idea about how to design the control unit and registers. The array should be reset and read twice. Registers should sequentially activate one row or one column at a time. All digital blocks are designed according to these requirements and their description is given in the following sections.

2.2.1 Registers

Registers should sequentially activate one column and one row at a time to scan the array. Register operation for a smaller array is shown in Figure 2.5. It is obvious that while the column register performs shift at clock frequency, the row register should shift at frequency 32 times smaller than the clock frequency.

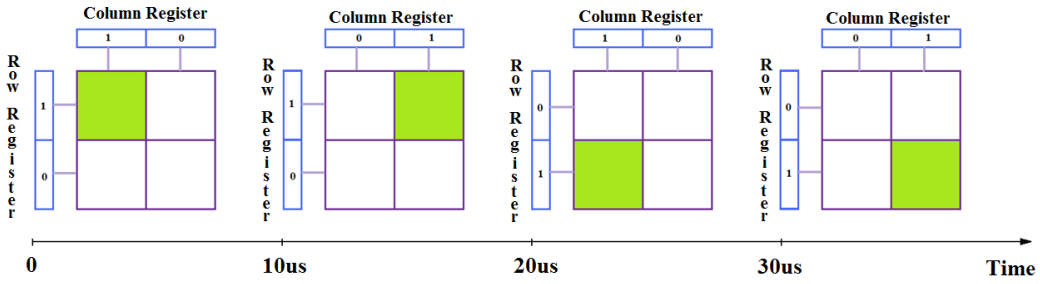


Figure 2.5: Illustration of row and column bit shifts for a 2 X 2 array.

To implement this task it is enough to have a shift register with load and shift functions. Register should have an input L signal, so that when L is high, input at the data port is loaded to the output of register at the proper clock edge, and when it is low, the content of the register is shifted. Register cell schematic possessing these properties is shown in Figure 2.6. It consists of a D flip-flop with and an asynchronous reset function, three NAND gates, one having inverting input, and a buffer. The NAND logic multiplexes either $Data$ or $Shift$ input with the help of L select signal to the input of D flip-flop.

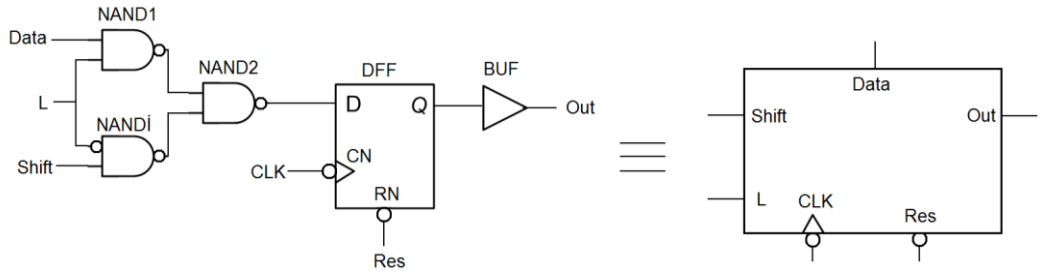


Figure 2.6: The schematic of the register cell and an equivalent symbol.

A buffer is used at the output, so that when such cells are connected in series, after the clock edge, the output is kept at the previous value for some time. The data can be transferred to the subsequent stage during shift operation more safely in this case. Output of a cell should be connected to the $Shift$ input of the next one to form a shift register as shown in Figure 2.7 for 2 bit case.

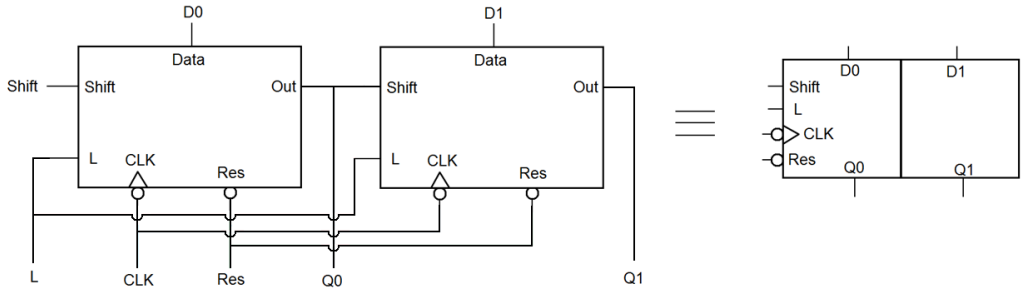


Figure 2.7: The register cells can be cascaded to form multi-bit registers, 2 bit example is shown.

Any number of such cells can be connected to form registers. Since a 32 X 32 array is implemented in the chip, 32 such cells are connected to form a 32 bit shift register. Register has a parallel data input $D0 - D31$, parallel output $Q0 - Q31$, $Shift$ input, control signal L, $Clock$ and $Reset$ inputs. All cells of the column and the row registers are identical except for the first cell of the row register. The D flip-flop of this cell has an active low set input, instead of active low reset as in all other cells of row and column registers. This is done to ensure

that during reset, row register is reset to 1000..., while column register is reset to 0000… The reason will be clear during the control unit discussion in Section 2.2.3.

2.2.2 Timing Circuitry and Buffers

Timing circuitry and buffers provide faultless operation by guaranteeing that only one output Q_i of column and row registers is 1 at a time while all other bits are zero. As this 1 bit propagates inside the register, array pixels are activated sequentially. However, since transition from 1 to 0 or 0 to 1 within a cell of a register takes some time, overlap of the output logic value may occur between the adjacent cells, both Q_i and Q_{i+1} being 1 during transition time as illustrated in Figure 2.8.

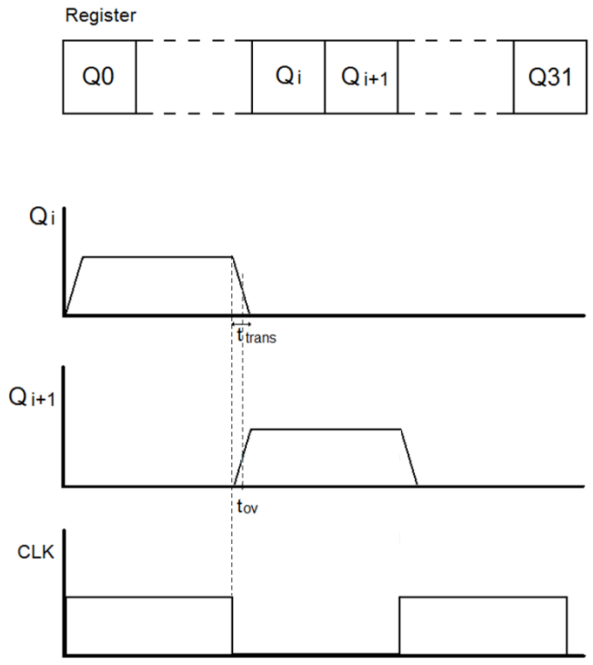


Figure 2.8: If timing is not properly adjusted, two adjacent bits of the register can have undefined output value during shift operation at the instant t_{ov}.

Note that at the overlap instant t_{ov}, which occurs during transition time t_{trans}, both Q_i and Q_{i+1} are at neither high nor low level, so they both could be interpreted as high level. In this case, switches of the two adjacent pixels would be on and they both would draw current to the source follower transistor M2. Since the total supplied current is 5 µA, each pixel would draw 2.5 µA. Then, M2 transistors of pixels would have smaller V_{GS2}. This would increase the voltage at the output node and result in undesired voltage peaks during transitions. Obviously, it is better to avoid such a behavior, so timing circuitry is used to make outputs of register cells non-overlapping.

The circuitry in Figure 2.9 is implemented to create a delay between the outputs. Such cells are connected to Q_i output of each register cell. Q_i is delayed and ANDed with itself to create a delay at the beginning of each output pulse. By this manner non-overlapping output signals are generated. The last buffer is used to ensure a safe operation by keeping the logic value at the output for long enough, so that no error occurs during the clock edges.

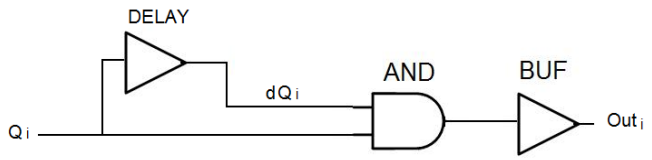


Figure 2.9: The schematic of the timing and buffer circuitry.

Figure 2.10 shows the timing diagram for clarification. If this circuit is used, outputs of a register will be as illustrated in Figure 2.11 for shift operation. Note that, during t_{delay} none of the register outputs is high, thus the switch of neither pixel is open, and the bias current $I_n - I_p$ cannot flow through any pixel. Then, I_n and I_p become equally 25 µA. In this case M11 transistor of the current source goes into linear region and voltage across it drops, resulting in a voltage

drop at the output. It is not a problem considering that the output node will start charging to the value of the corresponding pixel from the lower limit of the voltage swing. Then the pixel charge time will be even smaller than defined by Eq. 2.6, because the lower limit is assumed to be 0 V there.

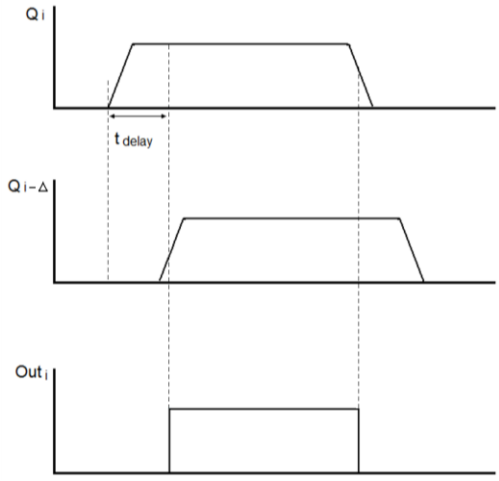


Figure 2.10: An output of a register after passing through timing and buffer circuit block.

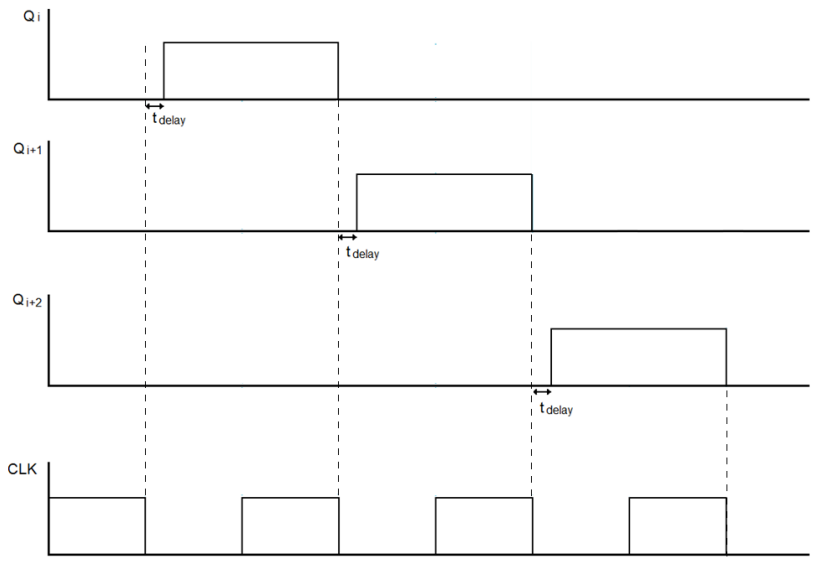


Figure 2.11: Outputs of three consecutive bits of a shift register with timing and buffer circuitry. Outputs do not have any overlaps in this case.

2.2.3 Control Unit

The control unit (CU) regulates and synchronizes all signals related with the operation of the chip. Description of the circuit operation is provided in Section 2.2. An ASM (algorithmic state machine) chart that would perform described tasks is designed accordingly as shown in Figure 2.12. CU design is based on that ASM chart. The CU has digital inputs $Start$, Res, CLK, $Eset$, C_b, R_b and digital outputs L_r, L_c, $Read$, $Vset$, Row_set. $Start$ signal is applied externally by the user to initiate operation of the device. Res is an active low reset which sets the CU to its initial state. C_b and R_b, are the last bits of the column and the row registers respectively.

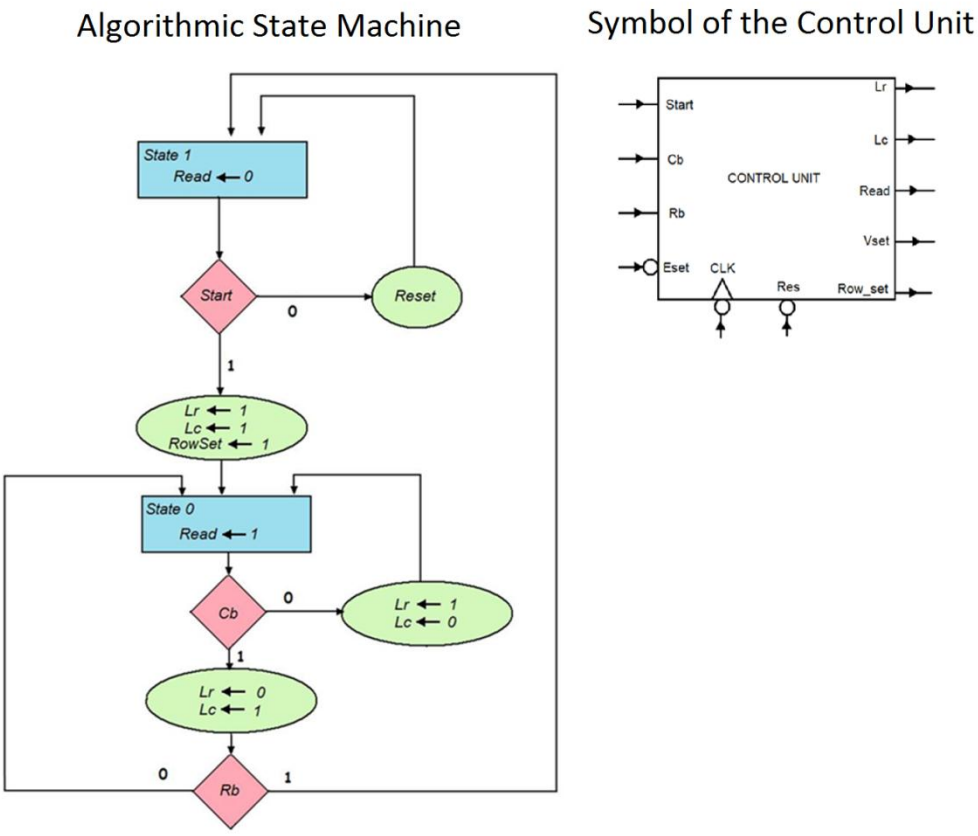


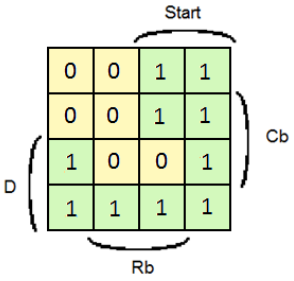
Figure 2.12: The ASM chart design according to the circuit operation description given in Section 2.2, and a symbol of the control unit showing input-output pins.

They are used as input control signals, so that when a row or a column scan is completed and the digital high reaches the last cell of a register, CU can understand it. $Eset$ is an active low enable signal for $Vset$ output. When it is enabled ($Eset = 0$), $Vset$ signal is generated once in every two reading cycles at the beginning of reading. By this manner pixel detector capacitors are reset to V_{ch} voltage. But if $Vset$ is disabled ($Eset = 1$), pixels are never reset. By enabling and disabling $Eset$ signal, the rate of pixels reset can be controlled. L_r and L_c outputs are load signals of the row and column registers respectively. $Vset$ signal is already explained in Section 2.1.1. $Read$ is a digital output signal indicating when pixels should be read, i.e. when the voltage of the output node corresponds to the voltage of the pixels $Read$ signal is high, otherwise it is low. This signal is only useful for the external electronics to understand when the data should be stored. It does not have any functionality in terms of chip operation. Row_set signal is a reset signal applied to the row register. As, already mentioned in Section 2.2.1, the row register is different than the column register in a sense that when it is reset its output becomes 1000… that is the initial bit Q_0 becomes 1. By making use of this fact CU is designed in such a way that, at the beginning of each cycle reset signal is generated and row register is reset to its initial value. Another difference between the row and the column registers is that, output bits of the row register are fed back to its data in port, while $D_0 - D_{31}$ inputs of column register are connected to logic 1000… Consequently, when L_r is high, the row register preserves its content, but when L_c is high, the column register is loaded with 1000… sequence. At the beginning of the operation, CU is in State 1 and $Read$ signal is low, meaning that scanning has not started yet. Until $Start$ signal is 1, CU stays in that state and keeps itself at reset. But this reset is not to be confused with the Res input of the CU, because it is an internal reset keeping CU at State 1. When $Start$ signal is asserted, CU goes to State 2, by making signals L_r, L_c, and Row_set high. Then, the row register is reset to 1000… and is kept at this value because L_r is high,

and column register loads the data which is 1000… as well. Therefore, when the CU enters the State 2 for the first time, the first row and the first column become active and switches of the first pixel turn on. At all times, while in State 2, $Read$ signal is 1 meaning that scanning is in progress and the output data can be stored. When at State 2, first C_b is checked, if it is 0, meaning that the current row is not fully scanned, L_r and L_c are made 1 and 0 respectively, so that at the next clock row register content is not changed, but column register is shifted. This goes on until the whole row is scanned and when C_b becomes 1, L_r and L_c are changed to 0 and 1. This time the row register is shifted, so that the next row is activated, and the column register is loaded with 1000… sequence, in order to make reading start from the first pixel of the corresponding row. Selected row is read in the same manner. When reading reaches the last row and the last column both C_b and R_b become 1 and CU goes in State 1 again. If $Start$ signal is not 0, then the whole array is read again with the same manner and this goes on until $Start$ signal is turned off. This ASM chart gives no information about the $Vset$ output signal. Since $Vset$ is activated only once in two readings including it would make the chart more complicated. In the real implementation, toggle JK flip-flop is used, which toggles every time in State 1. By this manner it is possible to identify at which cycles $Vset$ should be activated.

As apparent from the ASM chart, only two states are required, so a single D flip-flop with some extra gates would be sufficient for implementing the CU because the output of the flip flop can have either high or low value and each would correspond to one state. According to the ASM chart karnaugh map can be derived as in Figure 2.13. The formula for D input of the flip flop can be derived according to this karnaugh map as in Eq. 2.7.

D	Start	Cb	Rb	$\overline{D}$
0	0	X	X	0
0	1	X	X	1
1	X	0	X	1
1	X	1	0	1
1	X	1	1	0



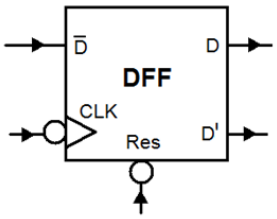


Figure 2.13: The truth table of the ASM chart with D=0 corresponding to State 1 and D=1 to State 2. Karnaugh map for a single D Flip-flop implementation and the D Flip-flop to be used are also shown.

$$\overline{D} = D'Start + D(C_b' + R_b') \qquad 2.7$$

A simple NAND gate logic shown in Figure 2.14 can be used to implement this function. This schematic provides state transitions, but the CU also has to generate control output signals L_r, L_c, V_{set} and Row_set that were mentioned before. Equations 2.8 to 2.11 are expressions for those signals derived according to the ASM chart. To generate V_{set}, JK flip-flop is required as explained before. Its output is indicated as Q_{jk} in those equations.

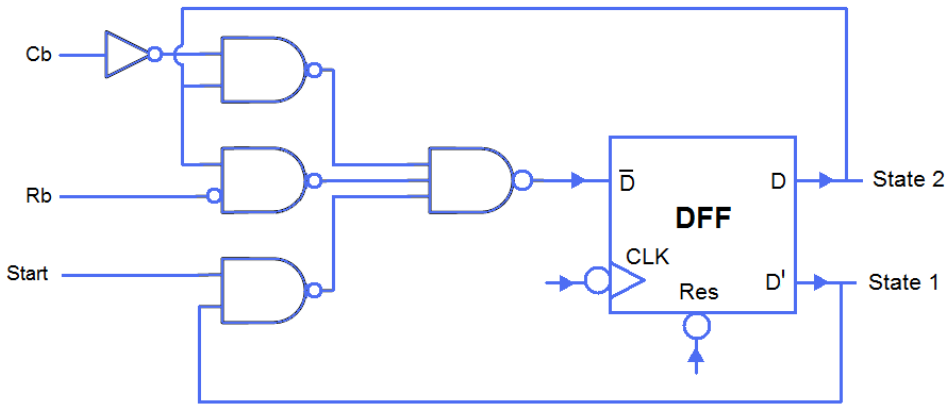


Figure 2.14: The D flip-flop implementation of the state transition circuitry of the control unit.

$$L_r = State\ 1 + \ C_b' = (State\ 2 * C_b)' \tag{2.8}$$

$$L_c = State\ 1 + \ C_b = (State\ 2 * C_b')' \tag{2.9}$$

$$Row\_set = (Start * State1)' \tag{2.10}$$

$$V_{set} = E_{set}' * State1 * Q_{jk}{}' = (E_{set} + State2 + Q_{jk})' \tag{2.11}$$

According to these formulas, signals can be easily implemented with some NAND-NOR logic. Figure 2.15 shows complete schematic of the control unit. The state transition circuitry is given in blue, output signals in green and reset circuitry in red (internal reset and external reset are ANDed so that either one can reset the system).

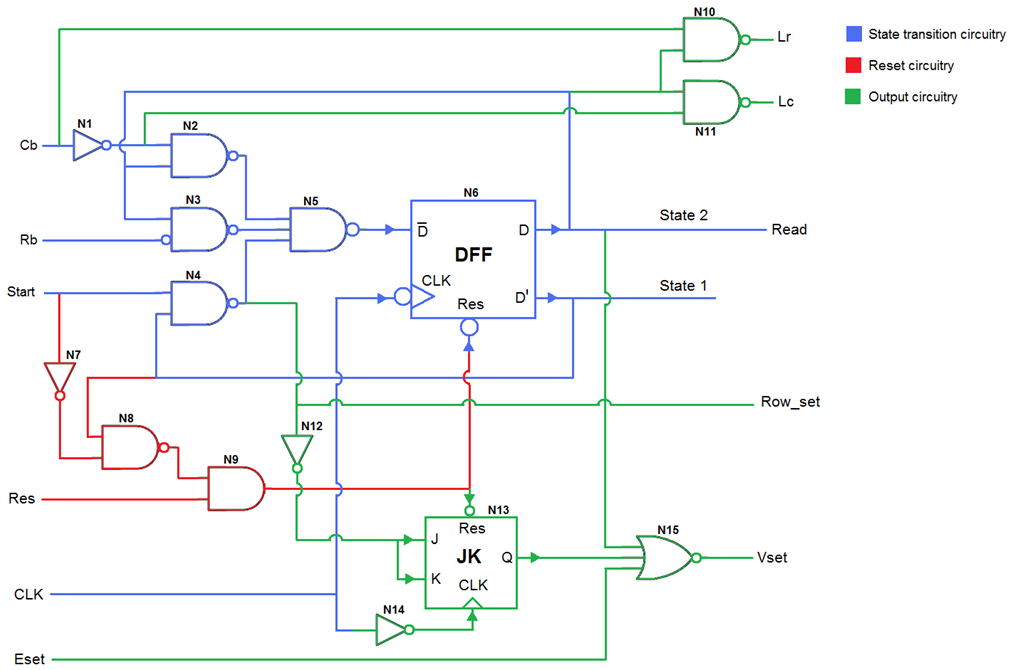


Figure 2.15: The complete schematic of the control unit. The state transition circuitry is given in blue, output signal circuitry in green and the reset circuitry in red.

2.3 Summary and Conclusions

This chapter describes the entire architecture of the chip. Analog circuitry consists of a 32 X 32 pixel array and the pixel bias circuitry, which sets the active pixel to the proper dc operating point. Pixel has a 3-T structure. Its sense node capacitance where the charge to voltage conversion takes place is around 6.055 fF corresponding to 26.42 µV/e conversion gain. Bias circuitry generates 25 µA and 30 µA current sources that drive the output. Pixel is biased with their difference which is 5 µA. Consequently, required small bias current is generated but the output capacitance driving capability is not limited to that small current. Digital Circuitry of the pixel consists of row and column registers for sequential pixel scanning, timing and buffer circuitry for non-overlapping register output generation, and a control unit for system synchronization and control. Figure 2.16 shows placement of the mentioned blocks in the chip core. The full chip layout with I/O pads is given in APPENDIX B.

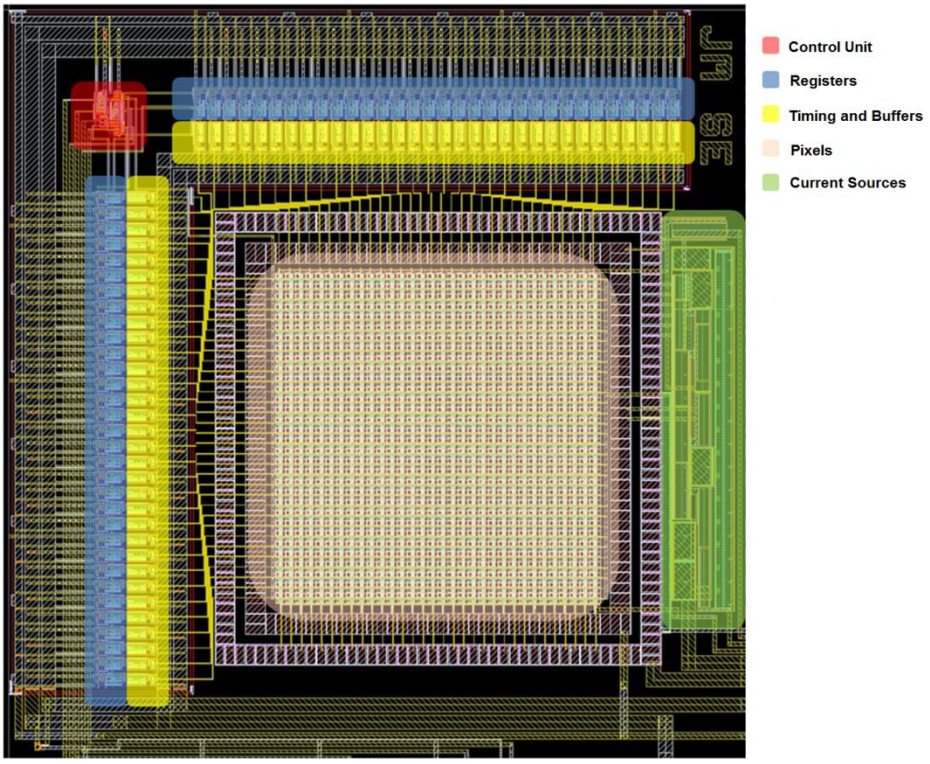


Figure 2.16: The layout of the chip core and organization of the system blocks.

CHAPTER 3

NOISE AND LEAKAGE ANALYSIS

This chapter analyzes the noise performance of the chip theoretically. Taking into account results of this analysis system parameters are defined so as to minimize the noise. Simulations are done with chosen parameters to verify the results. The pixel leakage, which is another factor resulting in an output error, is simulated as well. Finally, some calculations are done with the simulated parameters to verify the effect of the supply noise which is not accounted for in the simulation.

3.1 Noise Analysis

There are three main sources of noise in the chip: The reset noise resulting from the pixel reset, thermal noise of the bias network transistors and the flicker noise of the pixel source follower transistor. Certainly, pixel transistors have some thermal noise and bias network transistors have some flicker noise as well but their contribution is so small that is not worth mentioning, as will be revealed in noise simulation Section 3.2.1.

3.1.1 Reset Noise

All pixels are reset to V_{ch} potential trough transistor switch M1 of Figure 2.1, as mentioned in Section 2.1.1. Depending on the instant when switching of M1 occurs, due to the thermal noise of M1, some uncertain DC

voltage value freezes on the capacitor C_d. This uncertainty is called the reset noise [57] and is calculated as in Eq. 3.1,

$$Q_{reset} = \sqrt{\mathrm{kTC_d}} \tag{3.1}$$

where k is the Boltzmann constant and T is the absolute temperature. Equation 3.1 represents the charge noise. Since the input to the system is electrons of a DNA, the noise in terms of charge rather than voltage must be measured to interpret SNR. With 6.055 fF capacitance, noise contribution of the reset would be 31 e^- as shown in Eq. 3.2. However this is much larger than the intended noise floor. To eliminate the reset noise correlated double sampling (CDS) is done.

$$\mathrm{Q_{reset}} = \sqrt{\mathrm{kTC_d}} = \sqrt{1.38 * 10^{-23} * 300 * 6.055 * 10^{-15}}\mathrm{C} = 31.3\ \mathrm{e^-} \tag{3.2}$$

Array is scanned twice after the pixel reset and the difference of the two readings is considered to be the effective output. Consequently, the reset noise which is the common factor of the two readings vanishes and has no effect on the SNR of the system.

3.1.2 Bias Circuit Noise

There are two current sources used in the bias circuitry. Major thermal noise contribution comes from those current sources. Assuming that we can draw transistors of the bias circuitry big enough to make flicker noise negligible, (which is the case according to the simulation results in Section 3.1.4) the thermal noise can be calculated to first order using the model in Figure 3.1. The current noise is represented by a current source connected between the drain and the source of each transistor. Current noise power density is equal to $4kT\gamma gm$ for a transistor with a transconductance gm [57]. Since $4kT\gamma$ is a common factor for all transistors, it is replaced with a constant A in Figure 3.1

and proceeding equations. The small signal model is also shown in Figure 3.1 from which the total noise can be calculated.

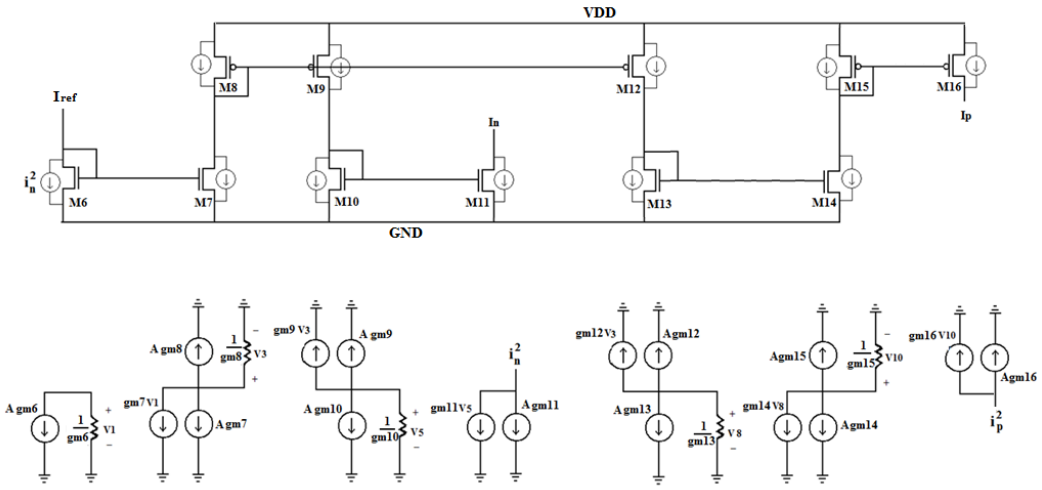


Figure 3.1: The small signal model to calculate the noise contribution of the bias circuit. Values before current sources in the figure represent current noise power I^2_{noise}.

From the model in Figure 3.1 i_n^2 and i_p^2 noises can be derived as in Eq. 3.3 and 3.4. Since we are interested in the voltage noise at the output node, output resistances over which the current noises flow should also be accounted for.

$$i_n^2 = \frac{\left(\frac{\left(\frac{A}{gm_6}gm_7^2 + Agm_7 + Agm_8\right)gm_9^2}{gm_8^2} + Agm_9 + Agm_{10}\right)gm_{11}^2}{gm_{10}^2} + Agm_{11} \quad 3.3$$

$$i_p^2 = \frac{\left(\frac{\left(\frac{\left(\frac{A}{gm_6}gm_7^2 + Agm_7 + Agm_8\right)gm_{12}^2}{gm_8^2} + Agm_{12} + Agm_{13}\right)gm_{14}^2}{gm_{13}^2} + Agm_{14} + Agm_{15}\right)gm_{16}^2}{gm_{15}^2} + Agm_{16} \quad 3.4$$

A simplified model shown in Figure 3.2 is used to estimate the output resistance, and the effects of the two current sources are superposed as in Equations 3.5 to 3.7.

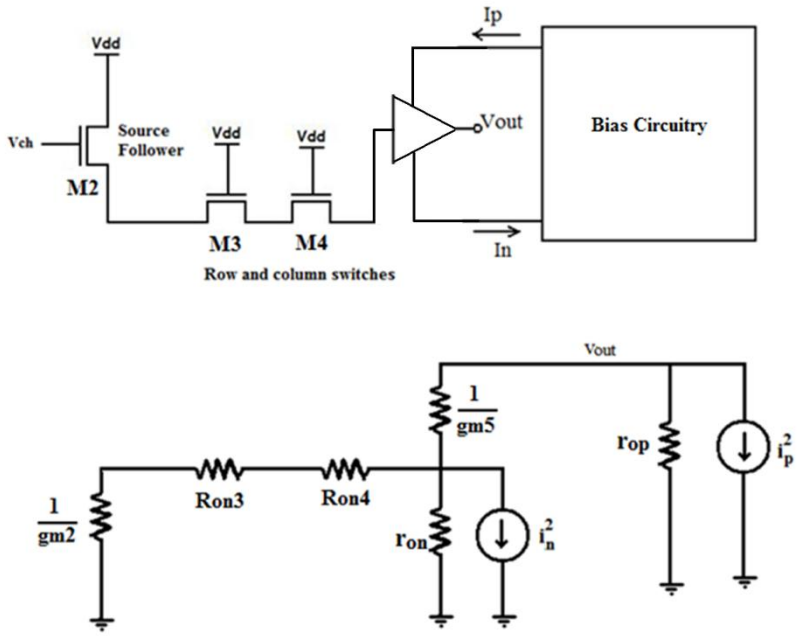


Figure 3.2: A model to estimate the effect of the current noises on the output voltage noise considering the small signal output resistance. gm_5 is the transconductance of the transistor of the output buffer.

r_{on} and r_{op} are the output resistances of M11 and M16 of Figure 2.3, R_{on4} and R_{on3} are on resistances of the switches, and g_{m2} is the transconductance seen at the source of M2.

$$v_n^2 \cong i_n^2\left[r_{on}\|\left(\frac{1}{gm_5}+r_{op}\right)\middle\|\left(R_{on3}+R_{on4}+\frac{1}{gm_2}\right)\right]^2 \cong i_n^2\left(\frac{1}{gm_2}\right)^2 \qquad 3.5$$

$$v_p^2 = i_p^2\left[r_{op}\|\left(\frac{1}{gm_5}+r_{on}\|\left(R_{on3}+R_{on4}+\frac{1}{gm_2}\right)\right)\right]^2 \cong i_p^2\left(\frac{1}{gm_2}+\frac{1}{gm_5}\right)^2 \qquad 3.6$$

$$v_{noise}^2 = v_n^2 + v_p^2 \qquad 3.7$$

Note that, resistances are dominated by g_{m2} and g_{m5}. Transconductance of an NMOS transistor can be expressed as in Eq. 3.8.

$$g_m = \frac{\mu_n C_{ox} W}{L}(V_{GS} - V_{TN}) \tag{3.8}$$

The only adjustable parameters in this equation are W, L, and V_{GS}. However increasing V_{GS2} reduces bottom level of the voltage swing. On the other hand, WL product of M2 is limited by M2 capacitance, as discussed in Section 2.1.1. Consequently, W cannot be increased too much, and L cannot be decreased beyond process limits. Eventually, g_{m2} which is a common factor in both resistance equations cannot be further increased. To increase g_{m5} on the other hand I_p current should be increased, and since $I_n > I_p$, I_n would be increased as well. But I_n and I_p have a direct effect on i_n^2 and i_p^2 as will be revealed later in this section, so it is not a way to reduce noise. On the other hand even if g_{m5} was much larger, still g_{m2} would dominate in the resistance of Eq. 3.6. Consequently, it is better to decrease i_n^2 and i_p^2 current noises if possible to obtain a smaller total noise. Simplifying Equations 3.3 and 3.4 and ignoring A multiplier which is a common factor, we can obtain expressions for i_n^2 and i_p^2 in terms of transistor transconductance values, as shown in Eq. 3.9 and 3.10.

$$i_n^2 \propto \left(\frac{gm_7^2 gm_9^2 gm_{11}^2}{gm_6 gm_8^2 gm_{10}^2} + \frac{gm_7 gm_9^2 gm_{11}^2}{gm_8^2 gm_{10}^2} + \frac{gm_9^2 gm_{11}^2}{gm_8 gm_{10}^2} + \frac{gm_9 gm_{11}^2}{gm_{10}^2} + \frac{gm_{11}^2}{gm_{10}} + gm_{11}\right) \tag{3.9}$$

$$i_p^2 \propto \left(\frac{gm_7^2 gm_{12}^2 gm_{14}^2 gm_{16}^2}{gm_6 gm_8^2 gm_{13}^2 gm_{15}^2} + \frac{gm_7 gm_{12}^2 gm_{14}^2 gm_{16}^2}{gm_8^2 gm_{13}^2 gm_{15}^2} + \frac{gm_{12}^2 gm_{14}^2 gm_{16}^2}{gm_8 gm_{13}^2 gm_{15}^2} + \frac{gm_{12} gm_{14}^2 gm_{16}^2}{gm_{13}^2 gm_{15}^2} + \frac{gm_{14}^2 gm_{16}^2}{gm_{13} gm_{15}^2} + \frac{gm_{14} gm_{16}^2}{gm_{15}^2} + \frac{gm_{16}^2}{gm_{15}} + gm_{16}\right) \tag{3.10}$$

Equations are consistent with the common intuition, so that gm values of the diode connected transistors (gm_6, gm_8, gm_{10}, gm_{13}, gm_{15}) should be increased, because currents are converted to voltage and mirrored over $1/gm$ of those transistors. Transconductance of the other transistors

(gm_7, gm_9, gm_{11}, gm_{12}, gm_{14}, gm_{16}) should be made as small as possible, because they directly affect current noise contribution. At first glance, since the two requirements are contradicting, it is hard to make a judgment on whether to increase or decrease the current in the circuit. However, if we express gm in terms of circuit parameters like the reference current (I_R) and overdrive voltages (V_{od}), the problem will be simplified. Equations 3.11 to 3.21 show gm parameters of all transistors. k_1 to k_6 are current mirroring coefficients of the bias circuitry.

$$gm_6 = \frac{I_R}{V_{gs6} - V_{TN}} = \frac{I_R}{V_{od1}} \tag{3.11}$$

$$gm_7 = \frac{k_1 I_R}{V_{gs6} - V_{TN}} = \frac{k_1 I_R}{V_{od1}} \rightarrow k_1(\frac{W}{L})_6 = (\frac{W}{L})_7 \tag{3.12}$$

$$gm_8 = \frac{k_1 I_R}{V_{sg8} - |V_{TP}|} = \frac{k_1 I_R}{V_{od2}} \tag{3.13}$$

$$gm_9 = \frac{k_2 k_1 I_R}{V_{sg8} - |V_{TP}|} = \frac{k_2 k_1 I_R}{V_{od2}} \rightarrow k_2(\frac{W}{L})_8 = (\frac{W}{L})_9 \tag{3.14}$$

$$gm_{10} = \frac{k_2 k_1 I_R}{V_{gs10} - V_{TN}} = \frac{k_2 k_1 I_R}{V_{od3}} \tag{3.15}$$

$$gm_{11} = \frac{k_3 k_2 k_1 I_R}{V_{gs10} - V_{TN}} = \frac{k_3 k_2 k_1 I_R}{V_{od3}} \rightarrow k_3(\frac{W}{L})_{10} = (\frac{W}{L})_{11} \tag{3.16}$$

$$gm_{12} = \frac{k_4 k_1 I_R}{V_{sg8} - V_{TN}} = \frac{k_4 k_1 I_R}{V_{od2}} \rightarrow k_4(\frac{W}{L})_8 = (\frac{W}{L})_{12} \tag{3.17}$$

$$gm_{13} = \frac{k_4 k_1 I_R}{V_{gs13} - V_{TN}} = \frac{k_4 k_1 I_R}{V_{od4}} \tag{3.18}$$

$$gm_{14} = \frac{k_5 k_4 k_1 I_R}{V_{od4}} \rightarrow k_5(\frac{W}{L})_{13} = (\frac{W}{L})_{14} \tag{3.19}$$

$$gm_{15} = \frac{k_5 k_4 k_1 I_R}{V_{sg15} - |V_{TP}|} = \frac{k_5 k_4 k_1 I_R}{V_{od5}} \tag{3.20}$$

$$gm_{16} = \frac{k_6 k_5 k_4 k_1 I_R}{V_{od5}} \rightarrow\ k_6 (\frac{W}{L})_{15} = (\frac{W}{L})_{16} \tag{3.21}$$

If these equations are replaced in Eq. 3.9 and 3.10, we can get expressions for i_n^2 and i_p^2, as shown in Eq. 3.22 and 3.23.

$$i_n^2 \propto \frac{k_1^2 k_2^2 k_3^2 I_R}{V_{od1}} + \frac{k_1 k_2^2 k_3^2 I_R}{V_{od1}} + \frac{k_1 k_2^2 k_3^2 I_R}{V_{od2}} + \frac{k_1 k_2 k_3^2 I_R}{V_{od2}} + \frac{k_1 k_2 k_3^2 I_R}{V_{od3}} + \frac{k_1 k_2 k_3 I_R}{V_{od3}} \tag{3.22}$$

$$i_p^2 \propto \frac{k_1^2 k_4^2 k_5^2 k_6^2 I_R}{V_{od1}} + \frac{k_1 k_4^2 k_5^2 k_6^2 I_R}{V_{od1}} + \frac{k_1 k_4^2 k_5^2 k_6^2 I_R}{V_{od2}} + \frac{k_1 k_4 k_5^2 k_6^2 I_R}{V_{od2}} + \frac{k_1 k_4 k_5^2 k_6^2 I_R}{V_{od4}} + \frac{k_1 k_4 k_5 k_6^2 I_R}{V_{od4}} + \frac{k_1 k_4 k_5 k_6^2 I_R}{V_{od5}} + \frac{k_1 k_4 k_5 k_6 I_R}{V_{od5}} \tag{3.23}$$

Equations 3.22 and 3.23 can be further simplified by noting the relation in Eq. 3.24. Simplification is done for Eq. 3.22 only, because the structure is symmetric and the same discussion will be valid for Eq. 3.23 as well.

$$I_n = k_1 k_2 k_3 I_R \tag{3.24}$$

$$i_n^2 \propto \frac{I_n^2}{I_R V_{od1}} + \frac{k_2 k_3 I_n}{V_{od1}} + \frac{k_2 k_3 I_n}{V_{od2}} + \frac{k_3 I_n}{V_{od2}} + \frac{k_3 I_n}{V_{od3}} + \frac{I_n}{V_{od3}} \tag{3.25}$$

V_{od3} limits the output voltage swing, so provided that some output swing restriction is present, it is hard to increase V_{od} of the transistors to reduce the noise. The same is valid for V_{od1} and V_{od2} since they are correlated with V_{od3}, so that V_{DD} puts a limit on $V_{od3} + V_{od2}$ and $V_{od2} + V_{od1}$. I_n is the output current defined by design requirements, so that it is the sum of 5 µA pixel bias current and 25 µA I_p current that drives the output load. So it is hard to reduce I_n because output driving capability will be directly affected. Consequently, we need to keep I_R as large as possible, so that the first term in Eq. 3.25 decreases.

Also, increasing I_R makes k_1 to k_3 parameters smaller for fixed I_n. This reduces other terms in the Eq. 3.25. In practice I_R cannot be infinitely increased and 200 µA is chosen as a reasonable value. Still the last term cannot be decreased unless we sacrifice from the voltage swing or the output current as obvious from the Eq. 3.25. Other adjustable parameters are k_1, k_2, and k_3. Obviously, $k_1k_2k_3$ multiple is fixed, and each of k values is less than 1, so that current does not exceed I_R.

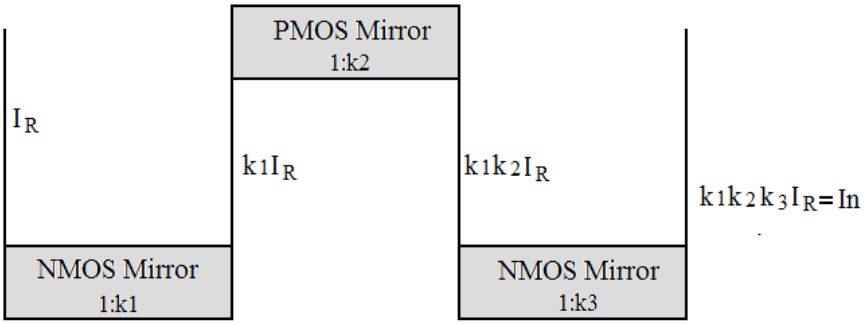


Figure 3.3: Illustration of the mirroring coefficients in the bias circuit.

Since k_3 appears in more terms than k_2, and k_1 does not appear in Eq. 3.25 at all, it is reasonable to keep $k_1 = k_2 = 1$ and $k_3 = I_n/I_R$. Then, by replacing these k values in Eq. 3.25, we get a very simplified expression for the current noise of the circuit in terms of currents and overdrive voltages as in Eq. 3.26. A similar result can be derived for i_p^2 as well and it turns out to be as in Eq. 3.27. To satisfy required overdrive voltages, the reference current I_R, output currents I_n and I_p, and current transfer ratios, transistor parameters are selected as in Table 2.2.

$$i_n^2 \propto \frac{I_n^2}{I_R}\left(\frac{2}{V_{od1}} + \frac{2}{V_{od2}} + \frac{1}{V_{od3}}\right) + \frac{I_n}{V_{od3}} \qquad 3.26$$

$$i_p^2 \propto \frac{I_p^2}{I_R}\left(\frac{2}{V_{od1}} + \frac{2}{V_{od2}} + \frac{2}{V_{od4}} + \frac{1}{V_{od5}}\right) + \frac{I_p}{V_{od5}} \qquad 3.27$$

Simulation results provided in Section 3.2.1 reveal that with these design parameters the noise of the current source becomes negligible and 81.2% of the overall noise is flicker noise of the pixel source follower transistor M2.

3.1.3 Flicker Noise of the Pixel

The flicker noise of the source follower transistor M2 (Figure 2.2) has a direct effect on the system noise the gate of the M2 transistor is the sensing node of the system and its input referred voltage noise directly mixes with the input information. Power spectral density of the flicker noise of M2 is equal to

$$\overline{V_{1/f}^2} = \frac{\mathrm{K}}{\mathrm{C_{ox}WLf}} \tag{3.28}$$

where K is some process dependent constant, $\mathrm{C_{ox}}$ is the gate capacitance per unit area, W and L are transistor dimensions and f is the frequency [57]. As mentioned earlier, transistor dimensions cannot be increased to reduce the noise, because conversion gain reduces with increased area as well. Moreover, conversion gain is related with WL while the flicker noise is related with $\sqrt{\mathrm{WL}}$, consequently SNR would reduce with increasing area. The only way to reduce the flicker noise further would be to increase the scanning rate of the array, because the flicker noise has more power at low frequencies as evident from its spectral density, and CDS, whose rate depends on array scanning rate, reduces low frequency noises. However there is a limit on maximum scanning rate, depending on ability of the chip to drive output capacitive load, and on noise and speed performance of the external ADC. The normal operating frequency of the chip is 100 kHz, but to see the effect of increased scanning rate, in Section 4.2.2, noise measurement results for operation at clock frequencies of 100 kHz and 250 kHz are given.

3.1.4 Supply and Bias Resistor Noise

This section deals with the effect of the supply variation and resistor noise on the output, eventually showing that these imperfections do not have a critical effect on the output noise. Consequently, even though generating a reference current as shown in Section 2.1.2 Figure 2.3, is not a best way in terms of insensitivity to temperature or supply variation, this structure is still preferred in order to avoid design labor of a more powerful reference current generator or a band gap reference. The supply noise and resistor thermal noise can be modeled as in Figure 3.4.

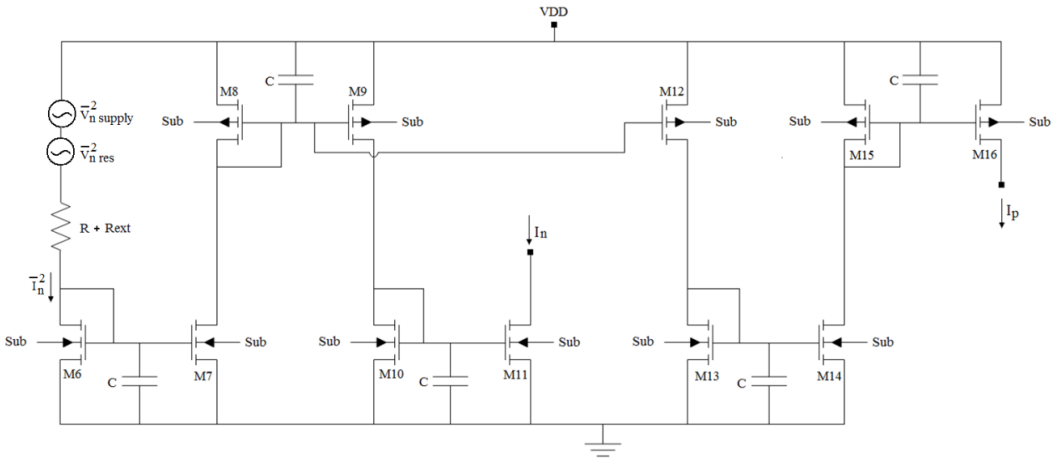


Figure 3.4: Illustration of voltage noises of the biasing resistors and supply. The supply noise effect is not considered at other branches like the source terminals of M8 and M9, because mirroring eliminates the effect of supply variation.

Note that all PMOS transistors have a connection to V_{DD}, but since V_{SG} is common for all mirror pairs, change in the source potential of those transistors does not affect the value of the mirrored current. The only point where supply noise has a contribution is the resistive branch where the reference current is generated. Consequently, resistor noise and supply noise can be treated

equivalently and the net current noise effect on the output can be found as in Equations 3.29 and 3.30,

$$\overline{i_{nSR}^2} = \frac{4\mathrm{kTR_{tot}} + \overline{v_{nS}^2}}{(\mathrm{R_{tot}} + \frac{1}{\mathrm{gm_6}})^2} * (0.15)^2 \qquad 3.29$$

$$\overline{i_{pSR}^2} = \frac{4\mathrm{kTR_{tot}} + \overline{v_{nS}^2}}{(\mathrm{R_{tot}} + \frac{1}{\mathrm{gm_6}})^2} * (0.125)^2 \qquad 3.30$$

where subscripts S and R stand for the supply and resistor, $\mathrm{R_{tot}}$ is the sum of external and internal resistors, $4\mathrm{kTR}$ is the formula of the PSD of a resistor thermal noise, and finally 0.15 and 0.125 are the current mirroring coefficients from 200 µA to 30 µA and to 25 µA for I_n and I_p respectively. $\mathrm{R_{tot}}$ is around 10 kΩ considering 4 kΩ internal and 6 kΩ external resistors, and $\overline{v_{nS}^2}$ depends on the choice of a voltage regulator. Results of these equations are compared with Eq. 3.26 and 3.27 in Section 3.2.3, and these noise effects seem to be negligible according to that comparison.

3.2 Simulation Results

This section describes simulation methods and gives simulation results for the noise and pixel leakage. Moreover, transistor parameters extracted from the simulation are used to evaluate numerical values of the equations derived in the previous sections. All simulations are performed in Cadence Spectre.

3.2.1 Noise Simulation

To analyze the noise performance, analog circuitry of the chip shown in Figure 2.2 was simulated with the schematic given in Figure 3.5. This simulation would give a precise idea about the noise at the output, because during

operation only one pixel becomes active and takes place in the analog network at a time. Remaining pixels have only capacitive effect on the row and column buses, which are mimicked by adding 31 off transistors to proper locations. Moreover, column and row bus capacitance effects are generated by adding 160 fF (5 fF per pixel) capacitors. Parasitic instances are shown in yellow in Figure 3.5.

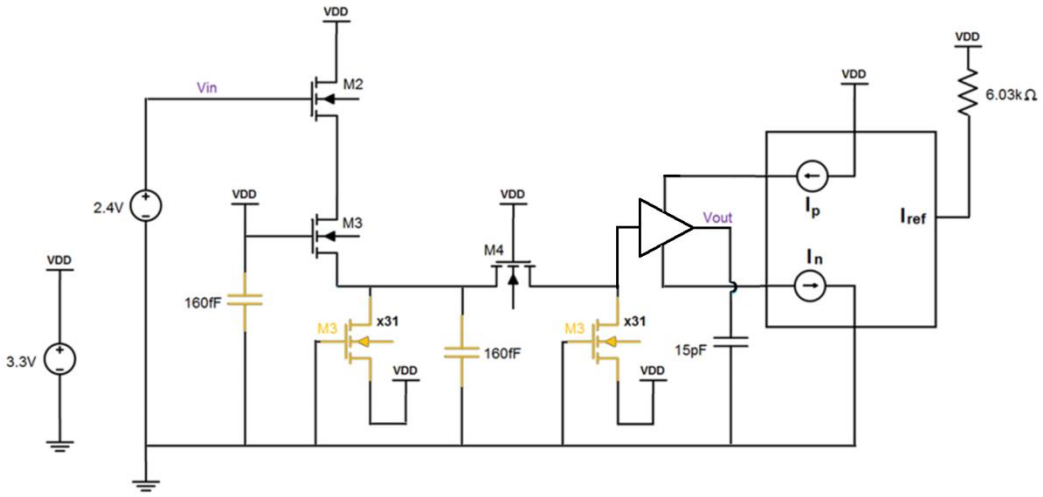


Figure 3.5: The schematic used for the noise simulation. Instances added to account for parasitic effects are shown in yellow.

An external resistance of 6030 Ω is connected to the current source to provide required 200 µA reference current. A 15 pF capacitor is used at the output node to represent the effect of pad and bonding capacitances, also the capacitance of the interface between the chip and external circuitry (e.g. input capacitance of ADC buffer). This capacitor also filters out some portion of high frequency thermal noise. Noise simulation is performed in the frequency range of 0.1 Hz to 10 GHz. Overall output noise plot is given in Figure 3.6. But rather than the plot of the output noise, overall integrated noise should be analyzed to get an idea about the noise contributors.

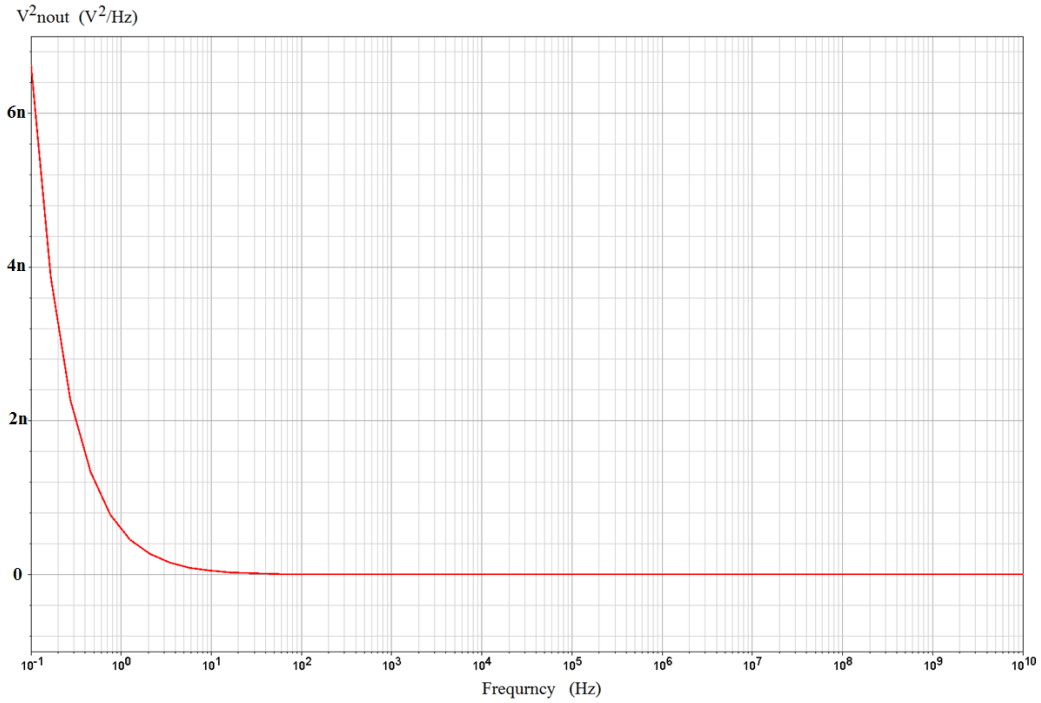


Figure 3.6: Power spectral density plot of the total output noise from 0.1 Hz to 10 GHz.

The total noise integrated from 0.1 Hz to 10 GHz comes out to be 89.58 µV. The noise summary is provided in Table 3.1 with the percentage contribution of each transistor noise. Flicker noise of M2 transistor which is the source follower of the pixel, accounts for 81.2% of the overall noise. This result justifies discussions on the bias circuitry noise because contribution of the current sources comes out to be around 15% only. Increasing the area of M2 transistor would reduce the flicker noise but would not increase the noise performance due to the tradeoff explained in Section 2.1.1, that is conversion gain would also decrease. Therefore, this performance seems to be the best that can be achieved in the given 0.35 µm CMOS process. Since the conversion gain is 26.42 µV/e, noise corresponds to 89.58 µV / (26.42 µV/e) = 3.39 e^-. This is a sufficient performance to detect two base-pairs, because a single base-pair corresponds to either 1 or 2 e^-.

Table 3.1: The noise summary of performed simulation. 81.2% of the total noise is due to the flicker noise of the pixel source follower transistor.

Device	Noise type	% of Total
M2	Flicker	81.20
M16	Thermal	4.69
M11	Thermal	3.74
M15	Thermal	2.08
M14	Thermal	1.84
M2	Thermal	1.21
M3	Thermal	0.82
M3	Flicker	0.55
M4	Thermal	0.35
M5	Thermal	0.32
Other bias	Thermal/Flicker	2.5
Total Noise		99. 3

3.2.2 Leakage Simulation

In Section 2.2 it was mentioned that there are two sources of leakage which result in a gradual data loss, that is, discharge of the capacitor C_d. First of all, after switching operation, even if we expect the voltage of C_d capacitor to be equal to V_{ch} , due to charge injection, and clock feed trough effects, it slightly decreases and becomes 2.36 V as simulation reveals. This results in nonzero V_{DS} voltage across M1 and even if M1 is off, still some leakage I_{DS} current flows

through it. On the other hand, source of M1 transistor is connected to the detector capacitor C_d and due to the reverse biased n-p junction formed at the source of M1, saturation current passes through that node. This is the reason why M1 transistor is designed to have minimum width, thus small junction area and consequently small leakage current. Figure 3.7 gives a representation of these two leakage currents on the schematic to simulate the leakage. Since $Vset$ signal is activated for one clock period in every two reading cycles, a square wave with 20 ms period and 10 µs pulse width is used to switch M1 transistor. The drain of M1 is connected to 2.4 V V_{ch} , and the source is connected to 6.1 fF C_d detector capacitor.

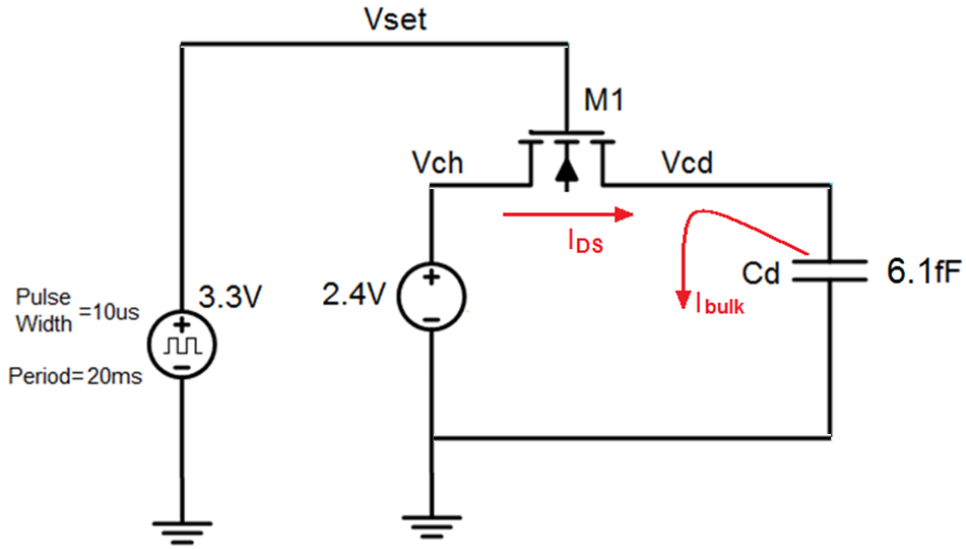


Figure 3.7: The circuit schematic for simulation and leakage sources.

Figure 3.8 shows simulation results. Since the effect of leakage is not so obvious from the plot, zoomed view is provided in Figure 3.9. The time between the two successive readings of a pixel voltage (the first one with being set and the second without being set) is 10 ms, so the voltage drop in 10 ms is observed. The voltage difference comes out to be 95.7 µV, which corresponds to 3.62 e^-, considering 26.42 µV/e conversion gain. To find out the contribution of each leakage, DC operating points are analyzed. Leakage resulting from I_{DS} comes

out to be extremely small when compared to the leakage through reversed biased diffusion area. According to the simulation I_{DS} = 13.7 $*$ 10^{-9} aA, while I_{bulk} = 65.9aA. This result is consistent with the previous calculations, because the leakage due to I_{bulk} in 10 ms, can be found as in Eq. 3.31, which is close to the previous result.

$$Q_{leak} = 65.9aA * 10ms = 6.59 * 10^{-19} C = 4.1\ electrons \qquad 3.31$$

In Section 4.2.2 the measured leakage comes out to be much larger than this value. As explained in that section, resistive substrate leakage is eliminated during simulation by setting g_{min} parameter to 10^{-20} which is 10^{-12} in default, because the real resistance of the substrate of the process was unknown. When g_{min} is set to 10^{-14} result closer to the measured one can be obtained.

The overall error at the output considering both the noise and the leakage is less than 8 e^-. However, the amount of leakage is deterministic and by smart software can be accounted for, during readout. Consequently, the overall error can be considered to be only the noise level, which is 3.4 e^-. The only noise that is not accounted for in the simulations is the supply noise. Its effect will be shown to be negligible in the next section.

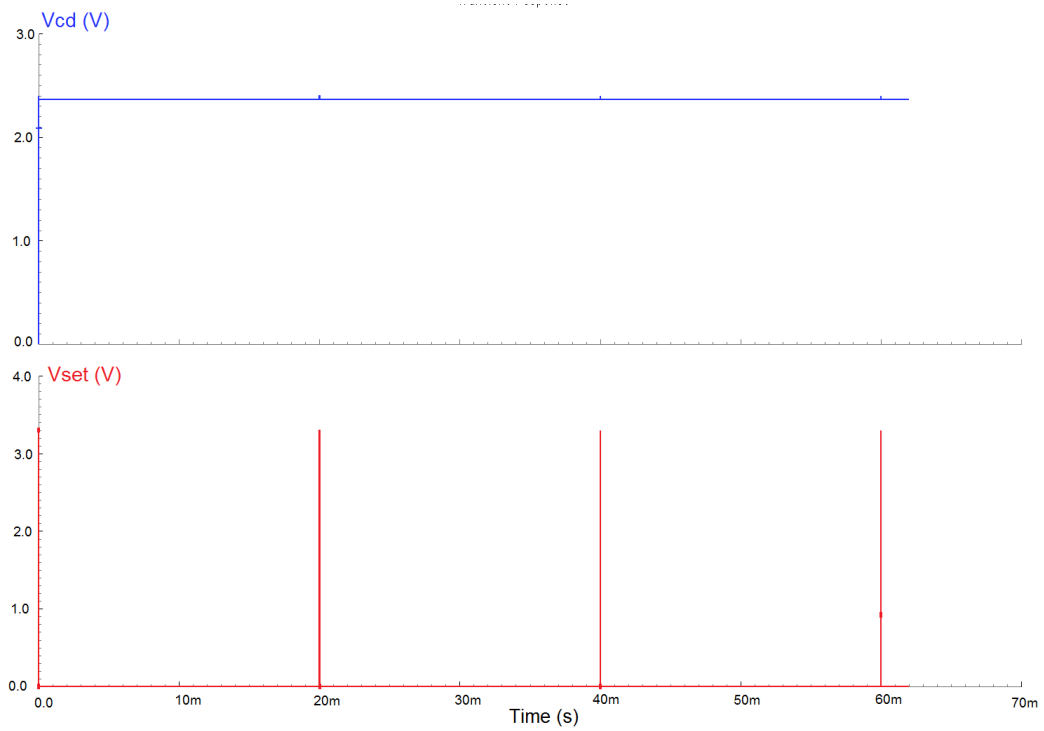


Figure 3.8: Leakage simulation results.

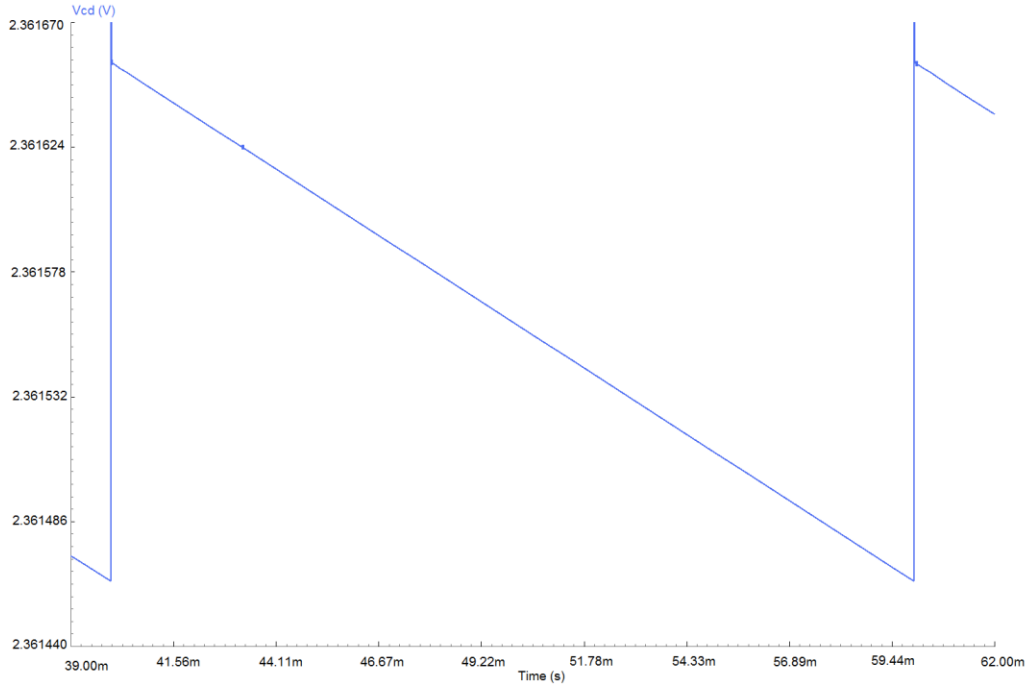


Figure 3.9: Zoomed view of the V_{cd} potential between 20 ms resets.

3.2.3 Noise Calculations Using Simulated Parameters and Equations

In the previous sections some noise equations were derived and a strategy to reduce that noise was given, but numeric values of those equations were not calculated. In this section, transistor parameters like transconductance values and overdrive voltages obtained from DC simulations are used to evaluate those values. There was a common factor A in noise equations of Section 3.1.2, which is equal to,

$$A = 4kT\gamma = 4 * 1.38 * 10^{-23} * 300 * \frac{2}{3} = 11 * 10^{-21}\ J \qquad 3.32$$

For i_n^2 and i_p^2 calculation we need overdrive voltages as evident from Eq. 3.26 and 3.27. Simulated parameters are shown in Table 3.2. Then, i_n^2 and i_p^2 can be calculated as in Eq. 3.33 and 3.34.

Table 3.2: Transistor parameters obtained from the DC simulation.

V_{od1}	V_{od2}	V_{od3}	V_{od4}	V_{od5}	gm_2	gm_5	gm_6
572mV	1.343V	611mV	684mV	578mV	55uS	182uS	584uS

$$\begin{aligned} i_n^2 &= A * \left(\frac{I_n^2}{I_R}\left(\frac{2}{V_{od1}} + \frac{2}{V_{od2}} + \frac{1}{V_{od3}}\right) + \frac{I_n}{V_{od3}}\right) \\ &= 11 * 10^{-21} * 30\mu * (0.15 * 6.64 + 1.64) \\ &= 87 * 10^{-26}\ A^2/Hz \end{aligned} \qquad 3.33$$

$$\begin{aligned} i_p^2 &= A * \left(\frac{I_p^2}{I_R}\left(\frac{2}{V_{od1}} + \frac{2}{V_{od2}} + \frac{2}{V_{od4}} + \frac{1}{V_{od5}}\right) + \frac{I_p}{V_{od5}}\right) \\ &= 11 * 10^{-21} * 25\mu * (0.125 * 9.65 + 1.73) \\ &= 81 * 10^{-26}\ A^2/Hz \end{aligned} \qquad 3.34$$

Now let's examine the effect of resistor thermal noise and supply noise. Equations 3.29 and 3.30 have two terms related with each noise respectively. Resistor thermal noise effect on i_n^2 and i_p^2 can be calculated according to the Eq. 3.35 and 3.36 once gm_6 is known.

$$\overline{i_{nR}^2} = \frac{4\mathrm{kTR_{tot}}}{(\mathrm{R_{tot}} + \frac{1}{\mathrm{gm_6}})^2} * (0.15)^2 = \frac{4 * 1.38 * 10^{-23} * 300 * 10k}{(10\mathrm{k} + \frac{1}{584\mu})^2} * (0.15)^2 \qquad 3.35$$
$$= 2.7 * 10^{-26}\ (A^2/Hz)$$

$$\overline{i_{pR}^2} = \frac{4\mathrm{kTR_{tot}}}{(\mathrm{R_{tot}} + \frac{1}{\mathrm{gm_6}})^2} * (0.125)^2 = 1.875 * 10^{-26}\ A^2/Hz \qquad 3.36$$

As obvious from the results, resistor noise is negligible when compared to the thermal noise of the transistors of the bias circuitry. Note that this is consistent with the fact that resistor noise did not appear among 99.3% of the noise contributors in simulation results, in Table 3.1.

To estimate the supply noise, we must start with some $\overline{v_{nS}^2}$ assumption. Let's assume that the voltage regulator has a $30\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ average noise density in the band of interest. Then the supply noise contribution can be found as in Eq. 3.37 and 3.38.

$$\overline{i_{nS}^2} = \frac{\overline{v_{nS}^2}}{(\mathrm{R_{tot}} + \frac{1}{\mathrm{gm_6}})^2} * (0.15)^2 = \frac{(30 * 10^{-9})^2}{(10\mathrm{k} + \frac{1}{584\mu})^2} * (0.15)^2 \qquad 3.37$$
$$= 14.76 * 10^{-26}\ A^2/Hz$$

$$\overline{i_{pS}^2} = \frac{\overline{v_{nS}^2}}{(\mathrm{R_{tot}} + \frac{1}{\mathrm{gm_6}})^2} * (0.125)^2 = 10.24 * 10^{-26}\ A^2/Hz \qquad 3.38$$

Note that these values are also sufficiently smaller than the current noise density due to the thermal noise of the bias circuitry transistors. Moreover, the thermal noise of the bias circuitry accounts for only 15% of the overall noise. Consequently, the effect of supply noise will be even smaller when the total noise is considered. Now we need to justify the 30 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ assumption for the voltage regulator noise. As described in the next section LT1762 voltage regulators are used in external electronics to provide low noise power. With the proper configuration these regulators have less than 20 μV_{rms} noise in 10 Hz to 100 kHz band. Our system has a bandwidth around 500 kHz considering the output capacitance of 15 pF and output resistance of 24 kΩ (Figure 3.2, Eq. 3.39).

$$R_{out} = \frac{1}{gm_2} + \frac{1}{gm_5} = \frac{1}{55\ uS} + \frac{1}{182\ uS} = 18.18\ k\Omega + 5.49\ k\Omega = 23.67\ k\Omega \qquad 3.39$$

From the output noise spectral density of the regulator in Figure 3.10, note that the most of the noise power is concentrated at frequencies up to 100 kHz, consequently with increased bandwidth, total RMS noise would not change much.

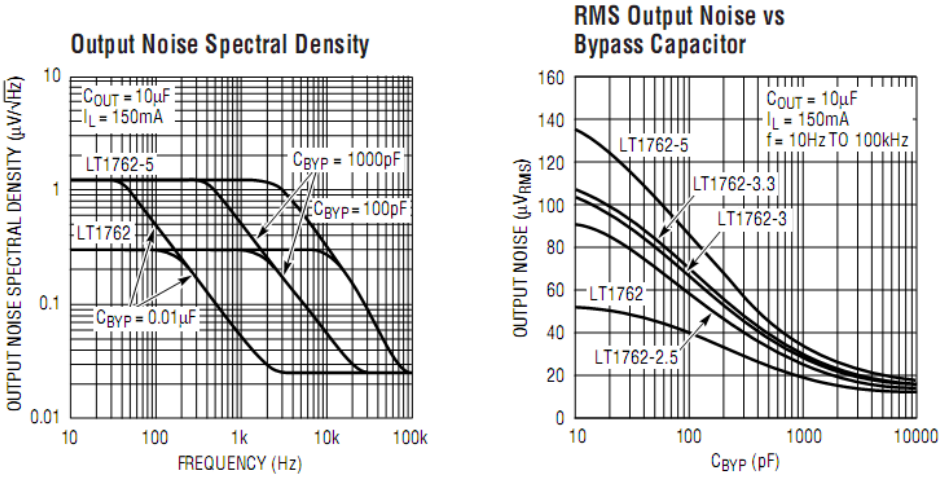


Figure 3.10: The output noise spectral density and RMS output noise of the LT1762 voltage regulator obtained from the datasheet of the device

Then, from Eq. 3.40 the regulator may be assumed to have an average noise density of 28.3 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ in the frequency band of 500 kHz, which is even smaller than the 30 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ assumption.

$$\sqrt{\overline{v_{nS}^2}} = \overline{v_{nS}} = 20\ \mu\frac{V_{rms}}{\sqrt{500\ kHz}} = 28.3\ nV/\sqrt{Hz} \qquad 3.40$$

Consequently, the supply noise becomes negligible with respect to the internal chip noise as well with the choice of a proper external regulator.

3.3 Summary and Conclusions

Theoretical analysis of noises like the reset noise, flicker and thermal noises was done, in order to define the milestones in minimizing the overall noise. Based on these analysis circuit parameters were defined and simulations were performed. The total noise (excluding supply and reset noise) came out to be 89.58 µV or 3.39 e^-. Supply noise would not contribute much to the total noise according to the calculations and the reset noise would be eliminated by CDS. The leakage of the pixels was also simulated and came out to be around 3 to 4 e^-.

CHAPTER 4

ELECTRONIC TEST RESULTS

This chapter first describes the external hardware and test software required to perform proper electronic and biological tests. Then it reveals results of the electronic functionality and performance tests, performed with a suitable packaging and a low noise test setup, which are required to accomplish high sensitivity DNA detection. Functionality is proven by operating the chip as an image sensor. The output voltage swing, noise and leakage values are measured to define performance of the chip.

4.1 External Electronics and the Test Setup

This section describes external hardware and software required to perform electronic tests. To analyze, quantify, process digitally or save the output of the chip, its analog value must be first converted to a digital signal. An external ADC is used for this purpose. Moreover, FPGA is used to generate necessary digital inputs and realize PC interface for data manipulation.

4.1.1 External Hardware

The main component of the external electronics is the analog to digital converter AD7679 of Analog Devices. The other parts are supporting units of this converter. The block diagram of the external electronics is shown in

Figure 4.1. AD7679 is an 18 bit ADC with the throughput rate up to 570 kSPS. The noise level of the chip was found to be around 90 µV, according to the simulations. With this noise level, 16 bit resolution with LSB corresponding to 60 µV, considering 4 V full scale would be enough, but 18 bits are used for a better precision, because LSB corresponds to 15 µV in that case, which is lower than the conversion gain of the pixel. Normally, ADC is operated at the rate of 100 kSPS, but 250 kSPS tests are also done for noise analysis as described in Section 4.2.2. The parallel output interface of the ADC is used. It requires 5 V analog and digital supplies but the output interface can be operated at 3.3 V by supplying 3.3 V to the OVDD (output VDD) pin. Therefore, ADC becomes compatible with the 3.3 V XEM3010 FPGA of Opal Kelly which is used to generate required digital signals for the chip and ADC control, and to generate appropriate interface with PC via USB port.

Signals generated by the FPGA which control ADC timing are 3.3 V, therefore 74LVX3245, a 3.3 V to 5 V level shifter, is used to provide a compatible interface.

The ADC requires differential input, while the output of the chip is single ended. Single ended to differential converter structure, utilizing two opamps AD8021, is used as offered in the datasheet of the ADC. The output of the chip cannot be directly connected to the input of the AD8021 opamp, because it requires 7.5 µA to 10.5 µA input bias current. The chip cannot supply this current since it would disturb its biasing structure shown in Figure 2.2. Hence, AD8655 opamp is used as a buffer stage. This is a low noise CMOS opamp and requires only 1 pA to 10 pA input bias current. The GBW of the opamp is 28 MHz and noise level is 2.7 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, which would result in about 8 μV_{rms} noise in 10 MHz band, so it does not contribute to the overall noise significantly.

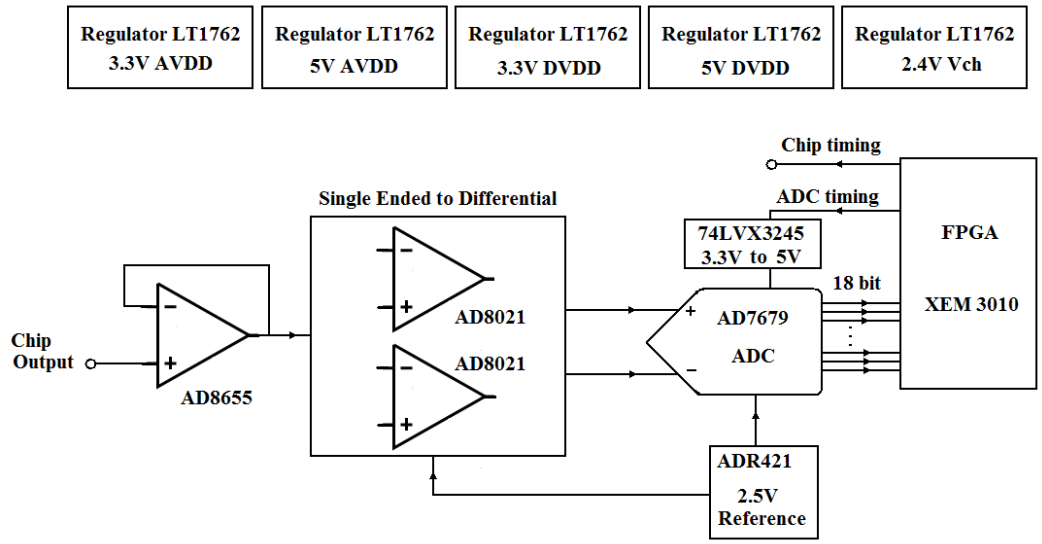


Figure 4.1: The block diagram of the external components and their interconnections.

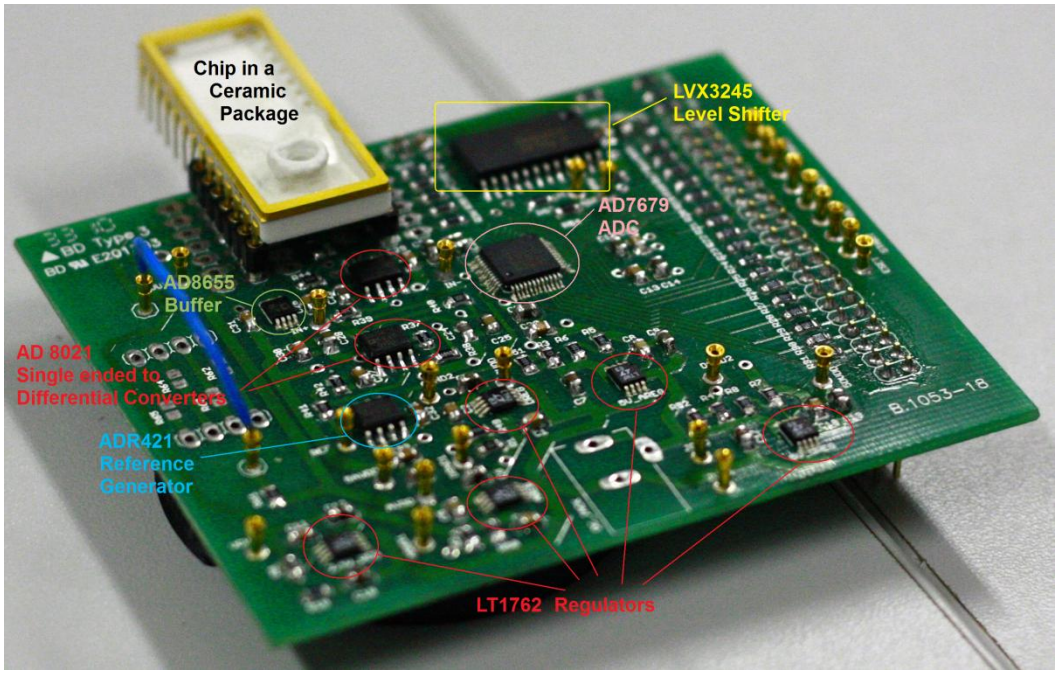


Figure 4.2: Designed external PCB with the components and a chip bonded to a ceramic package on top of it.

There are five LT1762 regulators in the circuit. 3.3V digital and analog supply regulators are used for chip AVDD and DVDD. The 3.3V digital supply regulator also feeds OVDD of the ADC as mentioned before. The 5V analog supply regulator is used for opamps and ADC analog supply. The 5V digital supply regulator is used for ADC digital supply. The 2.4V supply is used to provide V_{ch} input to the chip. 3.3V regulators are fixed LT1762 regulators and the others are adjustable LT1762 regulators. Noise of those regulators can be shrunk down to 20 μV_{rms}, and in Section 3.2.3 it was shown that this noise performance is sufficient in order not to disturb the overall noise level.

ADR421 is a 2.5V reference generator for the ADC. 4V corresponding to the full scale is generated in the internal reference buffer of the ADC when 2.5V reference voltage is applied to the corresponding pin. Actually, the range of the reference voltage that can be applied is 1.8 to 2.6V. In this case, some reference voltage taken from the chip can be used as a reference for the ADC to eliminate noises coupled to the ground of the chip. Such a reference can be taken from the I_{ref} pad of the chip, which is the interconnection point of external and internal resistors in Figure 2.3. Voltage of that node is 2.275 V, provided that 200 µA is current is sourced to the I_{ref} pin. ADR421 output feeds single ended to differential converter as well, and that block draws some extra current around 200 µA. If a reference from the chip is used, that extra current I_X will flow through external resistor, then the value of R_{ext} should be chosen according to the Eq. 4.1. Figure 4.2 shows the designed PCB comprised of listed components.

$$R_{ext} = \frac{\left(VDD - V_{I_{ref}}\right)}{I_{ref} + I_X} = \frac{(3.3 - 2.275)\ V}{200\ \mu A + 200\ \mu A} = 2.56\ k\Omega \qquad 4.1$$

As mentioned earlier Opal Kelly XM3010 FPGA is used for programming and PC interface. A PCB comprised of the aforementioned external components

is designed in such a way that it can be plugged into a BRK3010 board containing the FPGA. Figure 4.3 shows the photograph of the PCB on top of a BRK3010 board and a chip bonded to a ceramic DIL package that is plugged to the PCB.

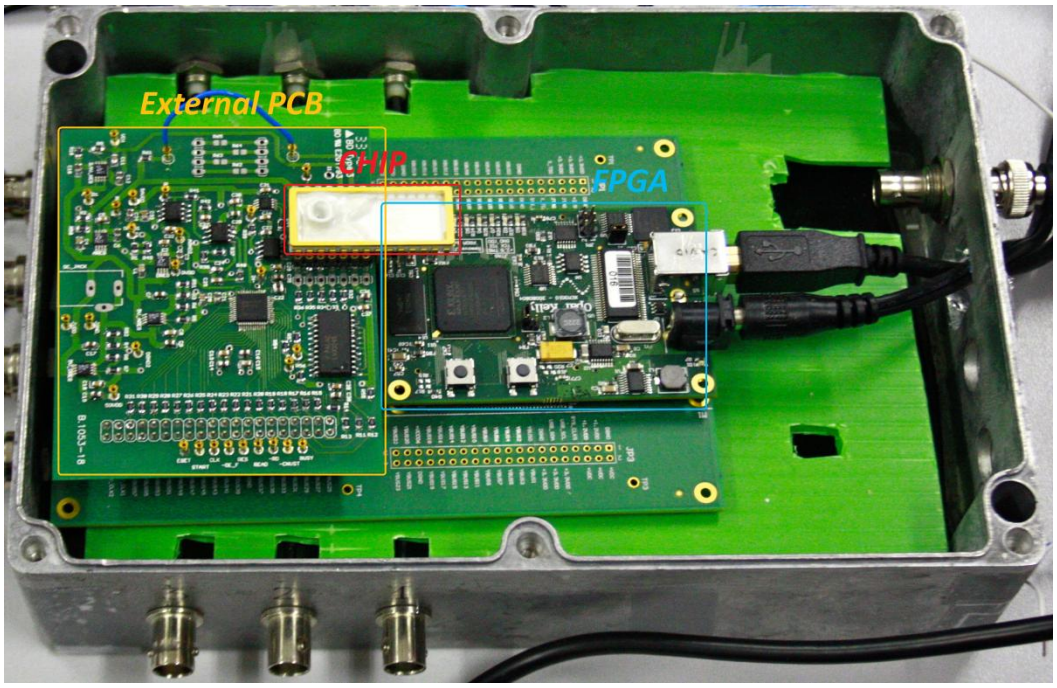


Figure 4.3: The designed PCB with the external components and a chip bonded to a ceramic DIL package. PCB is plugged to a BRK 3010 board containing Opal Kelly XEM3010 FPGA.

4.1.2 Test Software

A Verilog code and a C++ code are written to for the FPGA control and data manipulation respectively. The FPGA generates required clock and digital control signals to control the chip and the ADC, stores the data of the ADC to its internal RAM and sends the data to PC. Internal 100 MHz clock of the FPGA is used to generate required 100 kHz clock. Opal Kelly Front Panel modules are used to realize the data transfer to the PC. Internal RAM, one read and one

write FIFO are used to store the data and realize synchronization between the FPGA and the PC.

A C++ program is written to receive the data from the FPGA, process it, display it on the PC screen, and also to store it as a txt file. The program can also control the digital signals of the chip trough interface provided by the front panel modules of the Opal Kelly FPGA. GLUT and GLUI libraries are used to generate image and to create a control panel respectively. A screenshot view from the panel is shown in Figure 4.4. "BMDS Video" window is a visual interface, where a 32x32 pixel array is displayed in an 8 bit grayscale format.

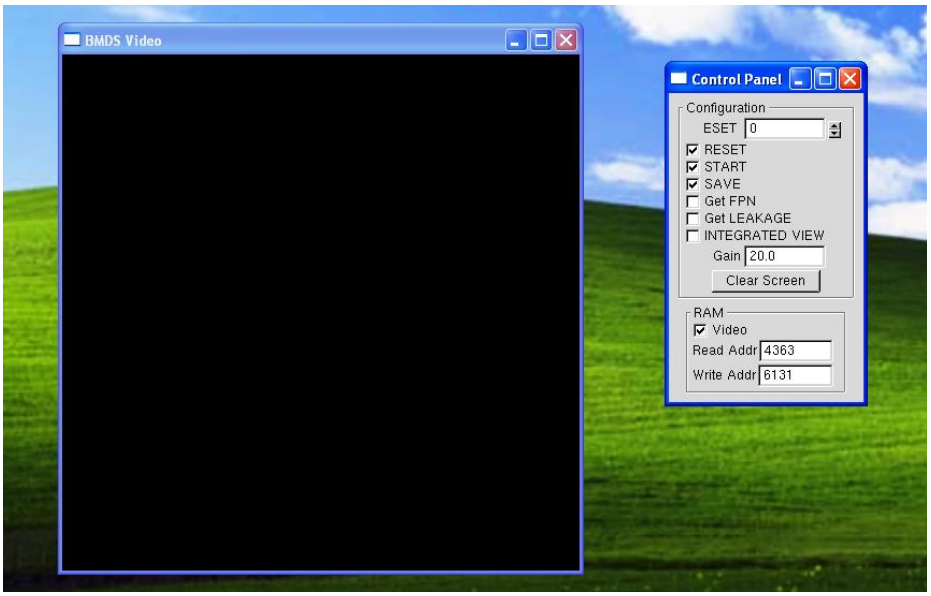


Figure 4.4: Interface generated by the C++ code using GLUI and GLUT libraries. Control panel regulates the operation, and "BMDS Video" window generates 32X32 images in 8-bit grayscale format.

"ESET" entry adjusts the rate of the pixel reset. When it is 0, array is reset once in every two frames, when it is 1 in every four frames, and by this manner up to 6, the rate of reset decreases. When "Eset" is 7, array is never reset. "Start" checkbox is the start input of the chip's control unit and the "Reset"

checkbox is the global reset of the chip. If “Save” checkbox is active, read frames are stored as a txt file. If “Get FPN” checkbox is active, the first 100 frames are averaged to extract the fixed pattern noise, in other words the value of each pixel right after pixel reset is read 100 times and all values are averaged. The values of subsequent frames are compared with the FPN value to get an idea about the input data. Similarly, when “Get LEAKAGE” checkbox is active, the leakage value between reset and non-reset frames is measured 100 times, averaged and stored for each pixel. It is possible to adjust software gain of the pixels with “Gain” panel. It is helpful to make pixels brighter when the data is too low to be observed with bare eyes. This option is especially useful when the data is below LSB of 8 bit, but much larger than the LSB of 18 bit, because unless some gain is added, pixel with that data will have no change in color.

There are two imaging modes, integrated and non-integrated mode. In case of non-integrated mode, the difference of each frame and FPN is displayed on the screen. This mode is helpful to observe the rate of discharge in every frame, in other words it gives information about instantaneous discharge but does not give an idea about the accumulated data. In case of integrated view, the difference of each frame and the corresponding reset frame is calculated and if it is greater than the leakage value of a pixel, the data is displayed and accumulated on the screen. This is helpful to observe accumulated data over time, however in time pixels saturate and turn completely white. “Clear Screen” button clears the old data from the display and integration starts over.

The data transfer to the PC starts only when “Video” checkbox is active. The only problem with the imaging is that, the output data is 18 bit while only 8 bit grayscale image can be displayed on screen as mentioned. However full data is stored as a text file and test results can be analyzed later on to get a more precise idea about the performance. Another advantage of storing the data is that, generated image refers to FPN or saved leakage values, but DNA tests can

take hours, and during that period drifts and temperature change can alter the FPN or leakage. Consequently, visual results can be misleading over long time interval. Therefore, “BMDS Video” window is used to get a first order idea about the performance rather than a precise quantitative result.

In summary, the external software realizes user friendly interface to control the chip, display the data with 8 bit precision for preliminary idea about the process, and to store the data for further analysis.

4.2 Electronic Tests

This section provides results of preliminary electronic test. The PCB plugged to Opal Kelly BRK 3010 board was put inside a Faraday cage as in Figure 4.5. 6V supply of Agilent power supply was used to supply the circuit. Supply connections to the PCB were provided with a BNC cable. USB connector and the power adaptor of the FPGA passed through a 2 cm X 2 cm hole made on the Faraday cage. The hole was sealed with an aluminum foil.

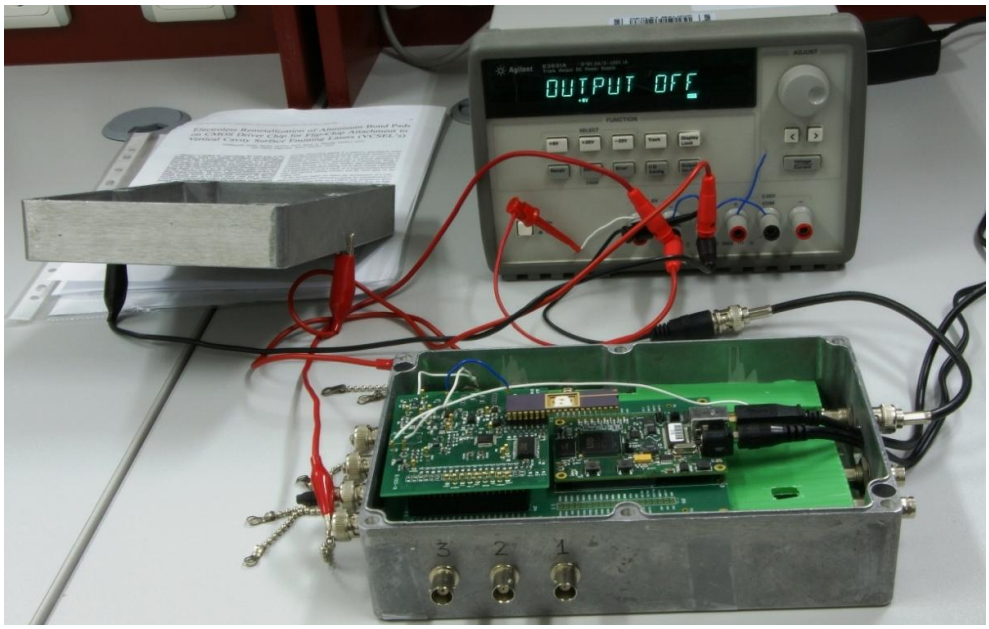


Figure 4.5: The test setup. PCB and the FPGA are enclosed in a Faraday cage and supplied with an Agilent triple output DC power supply.

4.2.1 Functionality Test

Digital signals and the analog output were observed with the oscilloscope to verify functionality. Figure 4.6 shows the analog $Output$ and digital $Read$ signals. $Read$ signal goes low for one clock period at around every 10 ms indicating the end of a frame. Noting that the frequency is 100 kHz and that there are 1024 pixels, frame period should be 10.24 ms as measured. The level of the output signal is around 1.99V, which is smaller than expected 2.4V V_{ch} value. Probably charge injection and clock feed trough effects during pixel reset result in larger voltage drop than in simulations. The other unexpected behavior is that the first and the last rows settle to a voltage different than 1.99 as all other rows after the reset. The first row settles at 1.82V while the last row settles at 2.25V.

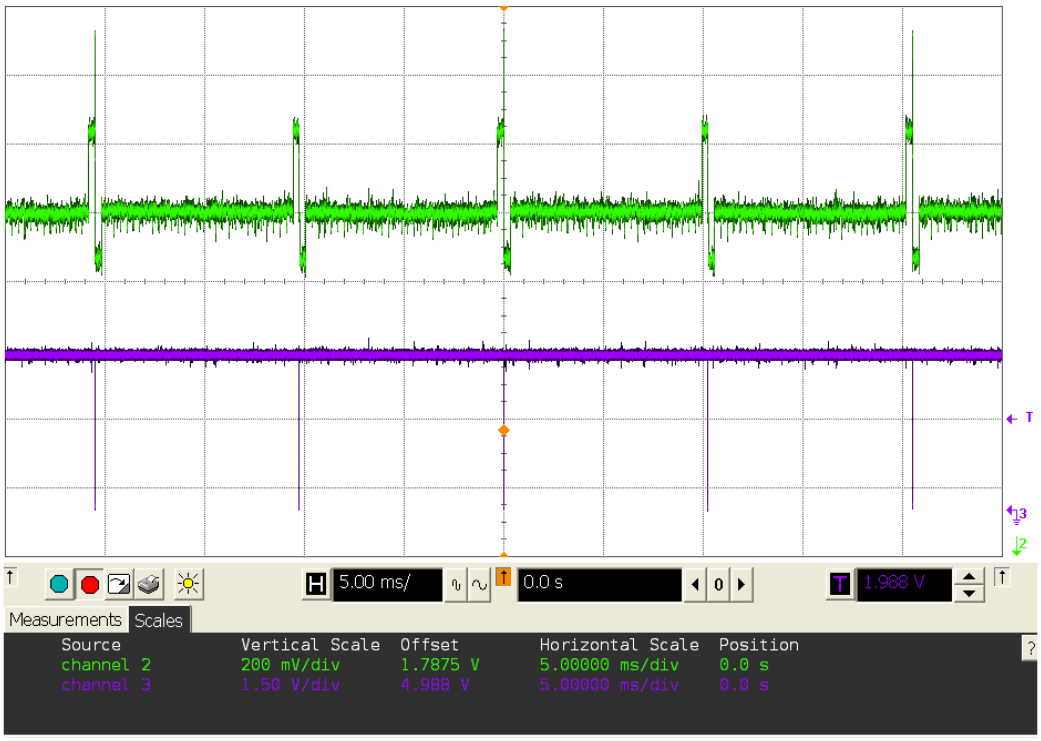


Figure 4.6: The analog *Output* signal of the chip and the digital *Read* output. *Read* signal goes low for 1 clock before each frame, and enables frame recognition.

The reason is probably some effect of digital switching order, and is not fully understood, but this artifact does not have a critical effect on the operation (other than modified output voltage swing for those rows) as long as the voltage difference between two consecutive frames is considered. Consequently, judging by the analog $Output$ signal, chip is working as expected.

Another tested digital signal is $Eset$ controlling the rate of the pixel reset. In Figure 4.6 glitches at the beginning of every two frames can be observed in the $Output$ signal which indicates that the reset occurs once in two frames. By adjusting $Eset$ enable signal reset can be disabled during any frame. The pulse width of $Eset$ is adjusted by the "ESET" entry of the control panel. Figure 4.7 shows $Eset$ pulses for "ESET"=1 and "ESET"=4. As can be seen from the Figure 4.7 $Eset$ is synchronized with the $Read$ signal, when it is 1 the array is reset in every 4 frames, and when it is 4, once in every 10 frames.

After testing the basic functionality, response of pixels to the incoming data was observed. In real tests, DNA charge would be the information discharging pixels, but since the pixels have a structure of a basic CMOS image sensor, visible light could be used as an input for verification test. Oscilloscope data was observed under fluorescent light illumination and the amount of illumination was enough to saturate pixels and define the voltage swing. Figure 4.8 shows comparative results of the output data under no illumination and maximum illumination. Linearly discharging pattern is observed because the first pixel is exposed to light for the shortest period while the last pixel is exposed to light for the longest period after the pixel reset. All pixels are saturated by the end of first frame, settling to 1.34 V. The voltage swing can be determined when this value is subtracted from 1.99V which is the settling voltage under no illumination. It comes out to be 650 mV, which corresponds to 24603 e^- considering 26.42µV/ e^- conversion gain. Noting that about 0.4V of V_{ch} voltage is lost during reset, V_{ch} can be raised to increase voltage swing further.

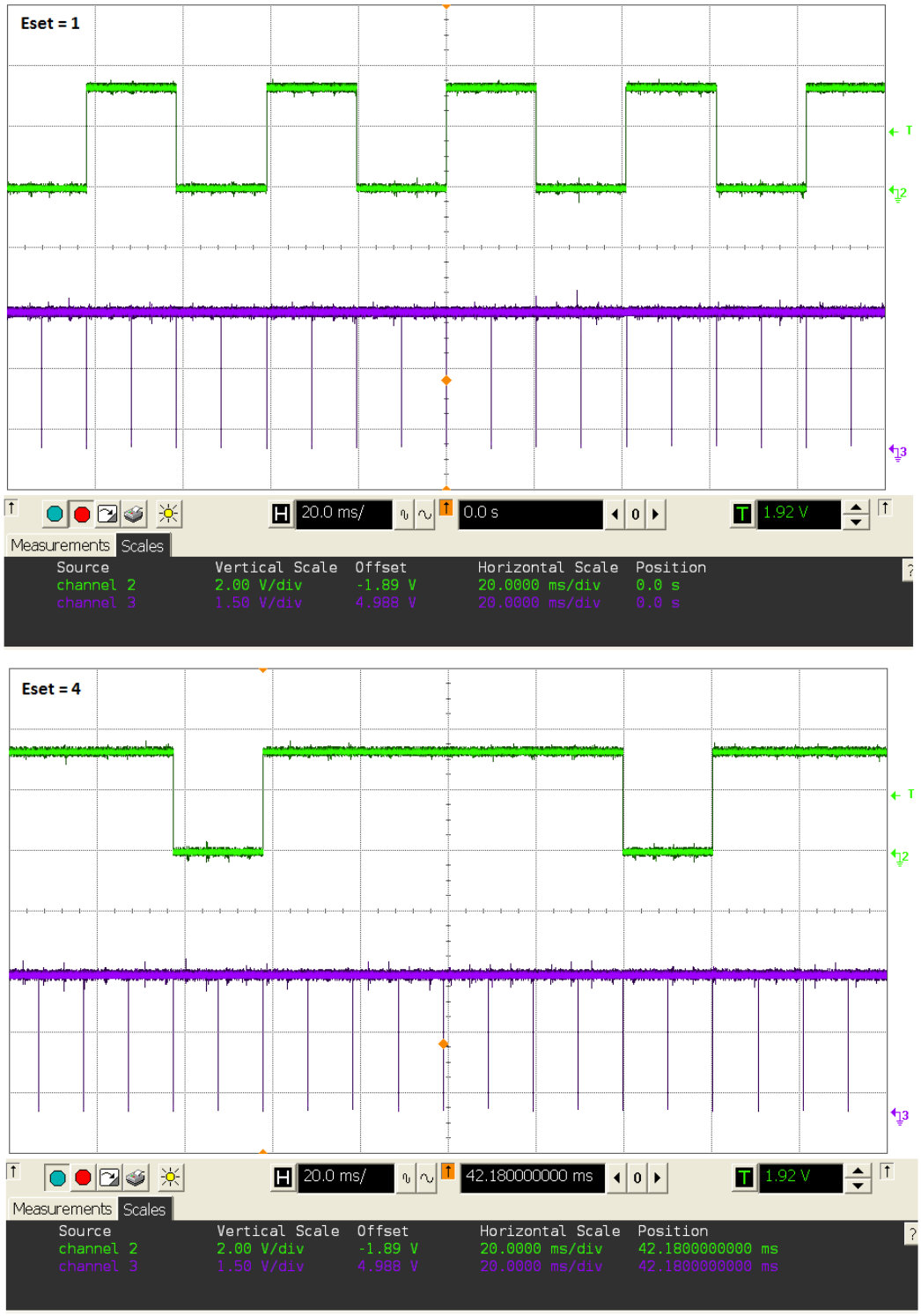


Figure 4.7: *Eset* input signal synchronized with the *Read* output signal for "ESET"=1 and "ESET"=4.

But this measured output swing is already enough considering that it is refreshed in every 20 ms, because every time the pixel reset is applied, pixels are pulled back to 1.99 V reaching their full well capacity.

The final functionality test was done by observing selective response of pixels to light. A laser pointer was passed through a light mask so that it illuminated only some portion of the array. Figure 4.9 shows the view obtained in “BMDS Video” window when the array is fully illuminated, and illuminated at three different spots. Non-integrating view is used to obtain shown images.

Conducted tests show that the chip has required functionality. To define the quality of its performance, noise and leakage tests are done as described in the next section.

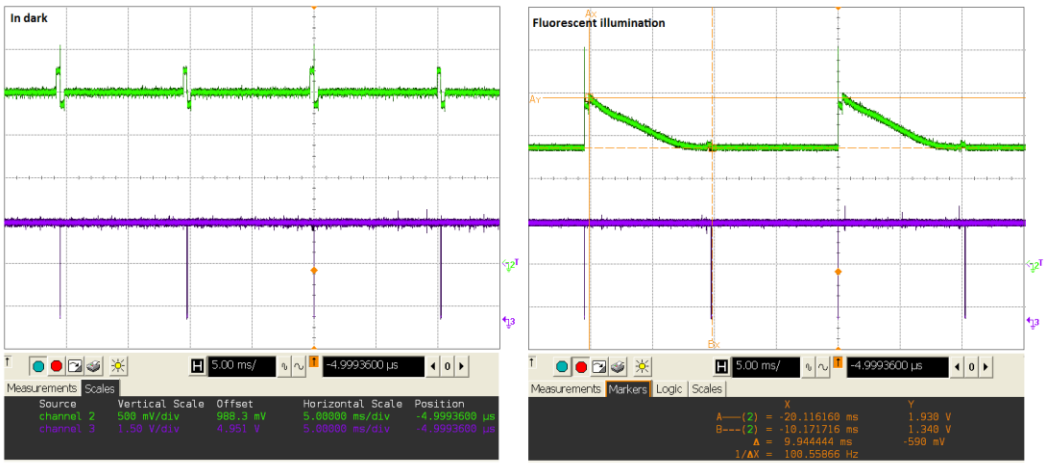


Figure 4.8: The analog output of the chip inside a dark Faraday cage with no incident light and under a fluorescent lamp illumination. Pixels are fully discharged to 1.34 V in 10 ms. Pixels settle to 1.99 V without illumination, meaning that the voltage swing is about 650 mV.

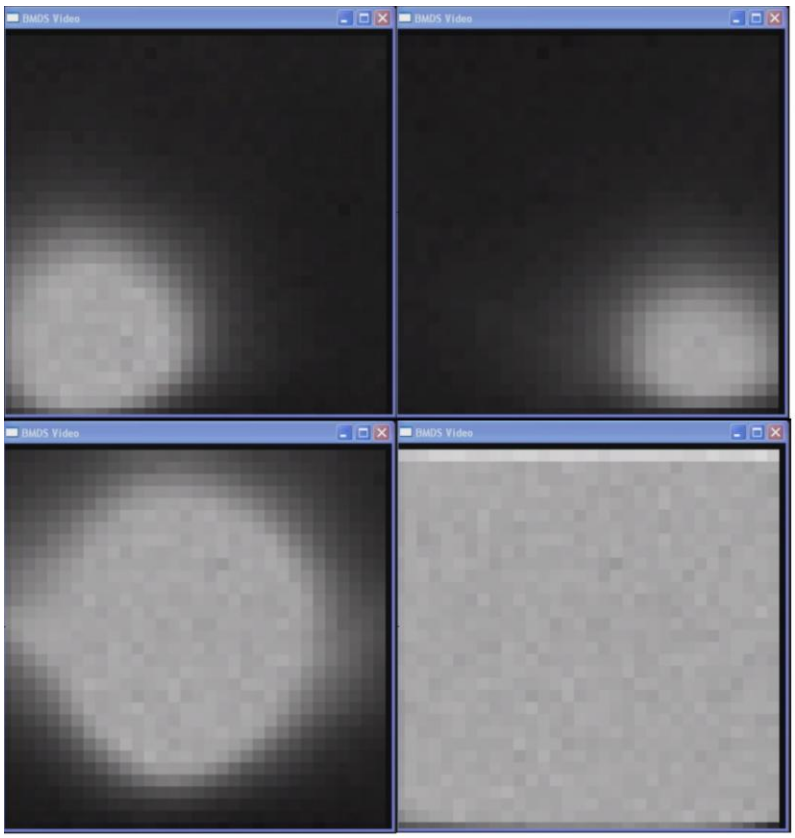


Figure 4.9: Images obtained from the chip for partial illumination at three different spots and under full illumination.

4.2.2 Performance Tests

The two main aspects of system performance are the noise and leakage, because they directly determine the sensitivity of the system. Most of the noise contributions were simulated and calculated in Chapter 3, and the total noise came out to be below 100 μV_{rms} according to those simulations. The noise of the external electronics was not precisely calculated but supply regulator noise and the noise of the output buffer were estimated to have negligible contribution.

External electronics noise was measured first. Measurement was done by disconnecting chip output from the input of the ADC buffer and connecting the output of the regulator generating 2.4 V V_{ch} voltage to it. The digital interface of the chip was used by this manner to communicate with the FPGA and ADC, so that the software described in Section 4.1.2 could be used, because only the analog output of the chip was faked. The regulator has around 20 μV_{rms} noise according to the datasheet. If the noise of external electronics was greater than or equal to that noise we would observe noise greater than 28 μV_{rms} at the output assuming that the external circuitry noise and the regulator noise are uncorrelated. But if noise was smaller than 20 μV_{rms} it would not have a significant contribution considering the total noise. To measure the noise, output of the ADC was stored during 5 minutes. Considering the frame rate of 10 ms, and 1024 pixels, 30.72 M samples were taken during that time. Measured noise became 1.59 ADC counts which corresponds to 24 µV considering 15 µV LSB. Then, the noise of the external electronics must be smaller than 20 μV_{rms}, according to the above discussion. But even if the regulator had an ideal performance with no noise contribution and 24 µV was purely due to the external electronics, this noise is still smaller than the conversion gain of 26.42 $\mu V/e^-$, and would have an insignificant effect on the total noise.

After measuring the noise of the external electronics, noise of the chip was measured. The first measurement was taken for 5 minutes at 100 kHz frequency. 300 k samples were taken from each pixel during that time. Pixel reset was done once in every two frames. The average pixel noise of the real data, which is the difference of those two frames, was measured to be 11.78 ADC counts corresponding to 176.7 µV or 6.7 e^-. This noise does not contain reset noise because CDS is done when the difference of two consecutive frames is taken.

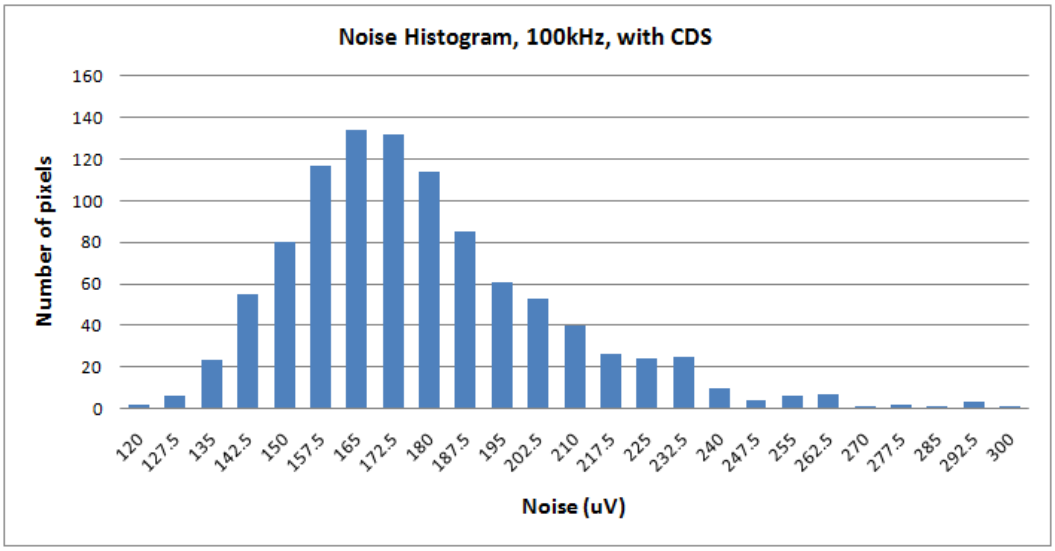


Figure 4.10: The noise histogram for the output measured for 5 minutes. The chip is operated at 100 kHz. CDS is performed and the average noise is 176.7 µV.

Figure 4.10 shows the histogram of the pixel noise for this measurement. The noise came out to be larger than the simulated and calculated noise. This is not very unexpected, because the dominant noise contribution in the system is the flicker noise, which probably was not precisely modeled in the simulation software. To confirm the fact that the most of the noise is due to the flicker noise, the same measurement was done at 250 kHz frequency. Again 300 k samples were taken. The noise was expected to reduce because, the flicker noise is dominant at lower frequencies and the over sampling filters out some portion of low frequency noises. The average pixel noise became 8.98 ADC counts, or equivalently 134.7 µV or 5.1 e^-. Figure 4.11 shows the histogram of the pixel noise for this measurement. Noise of the previous measurement was 6.7 e^-, which means that total noise power has reduced by 42%. This observation backs up the claim that the dominant noise contributor is the flicker noise of the pixel source follower transistor and that it has reduced due to the over sampling. Sampling rate faster than 250 kHz is not favorable because it

limits the output driving capability of the chip and also deteriorates the noise performance of the ADC.

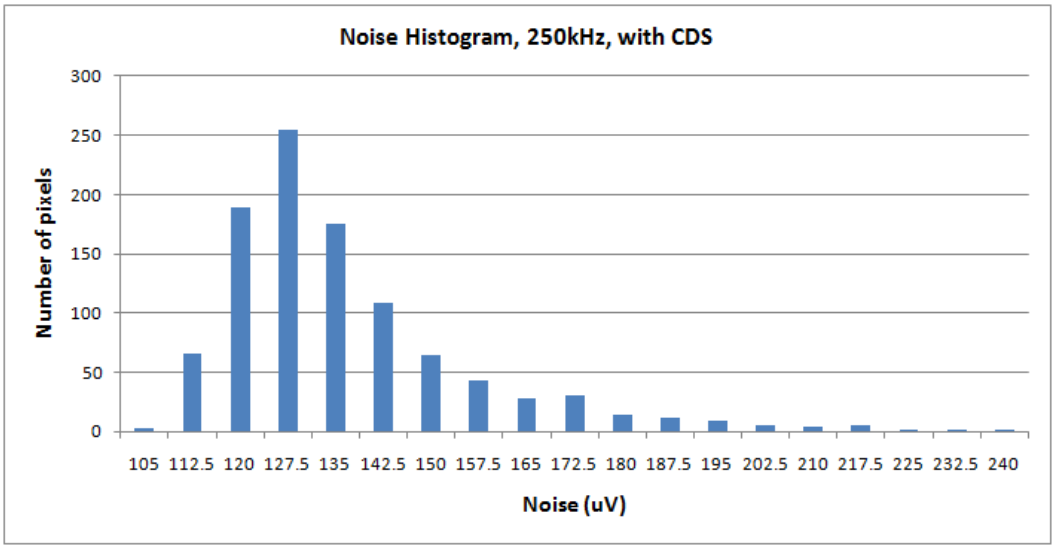


Figure 4.11: The noise histogram for the output. 300 k samples are taken. The chip is operated at 250 kHz. CDS is performed and the average noise is 134.7 µV.

To verify the effect of the CDS, data of these two measurements were analyzed without implementing CDS, in other words noise of the frame data was measured without taking the difference of consecutive frames. Figure 4.12 and Figure 4.13 show the noise histograms for the two measurements. The average noise was measured to be 67.9 ADC counts, equivalently 1.02 mV or 38.55 e^- for 100 kHz measurement, and 59.6 ADC counts, equivalently 894 uV or 33.8 e^- for 250 kHz measurement.

The reset noise calculated in Section 3.1.1 was 31.3 e^-, which is quite close to the measured value. This value was calculated using the pixel capacitance, which was 6.055 fF according to the parasitic capacitance extraction of CADENCE. Variation of only 1 fF, that is 7 fF capacitance would result in 36 e^- reset noise, implying that the measured results are consistent with the theory.

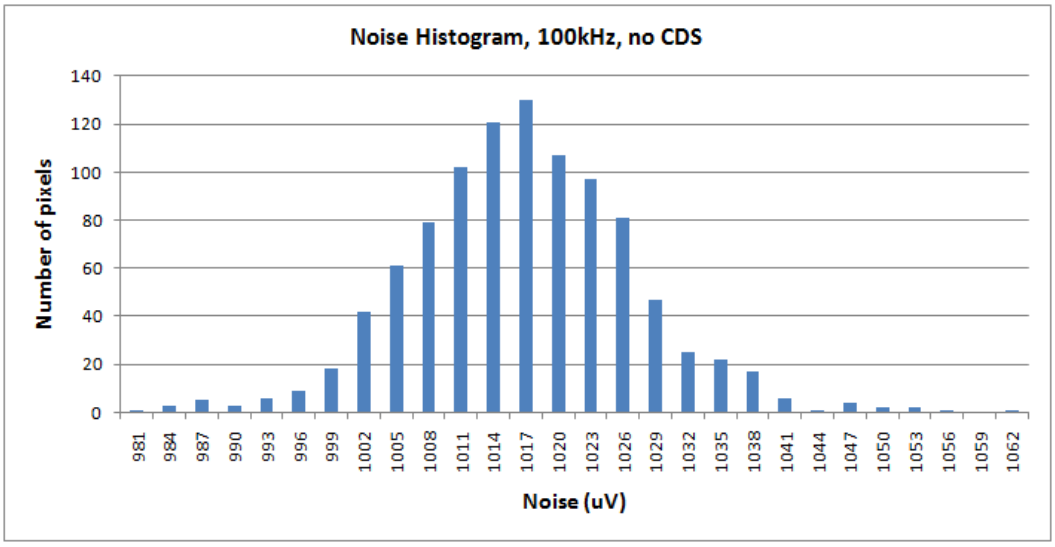


Figure 4.12: The noise histogram of the 300 k sample data taken at 100 kHz when the CDS is not performed. Average noise becomes 1.02 mV.

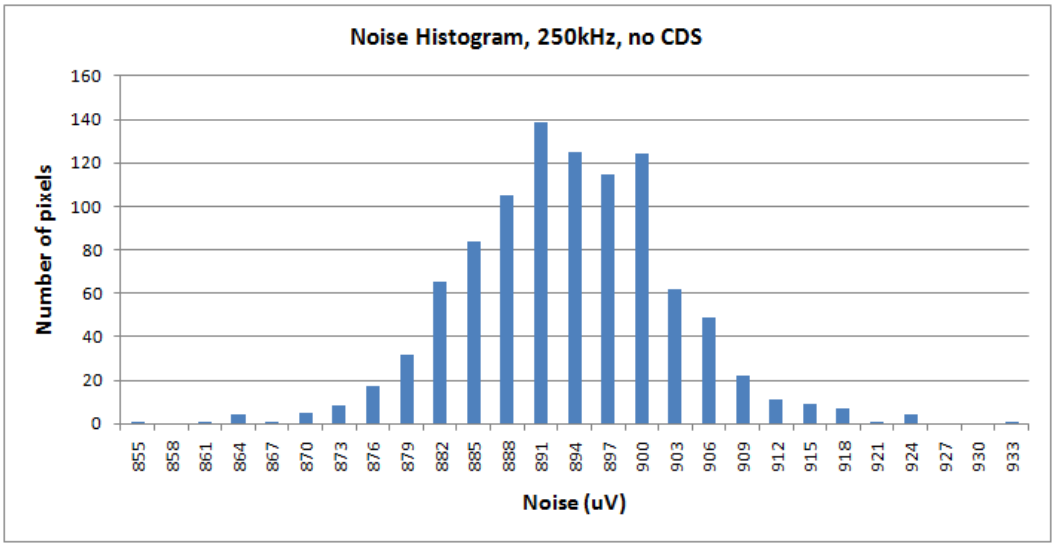


Figure 4.13: The noise histogram of the 300 k sample data taken at 250 kHz when the CDS is not performed. Average noise becomes 894 uV.

The pixel leakage is another artifact resulting in the output error. The main source of leakage was shown to be the saturation current of reversed

biased diode generated at the drain terminal of reset transistor M1. According to the simulation results provided in Section 3.2.2, leakage comes out to be 3.62 e^-/frame for 100 kHz operation frequency. Leakages were calculated from the measured data. Figure 4.14 shows the histogram of pixel leakage for 100 kHz operation frequency and the average pixel leakage comes out to be 54.7 ADC counts, which is equivalently 820.5 µV or 31 e^-. Note that the measured result came out to be 8.8 times larger than the simulated leakage.

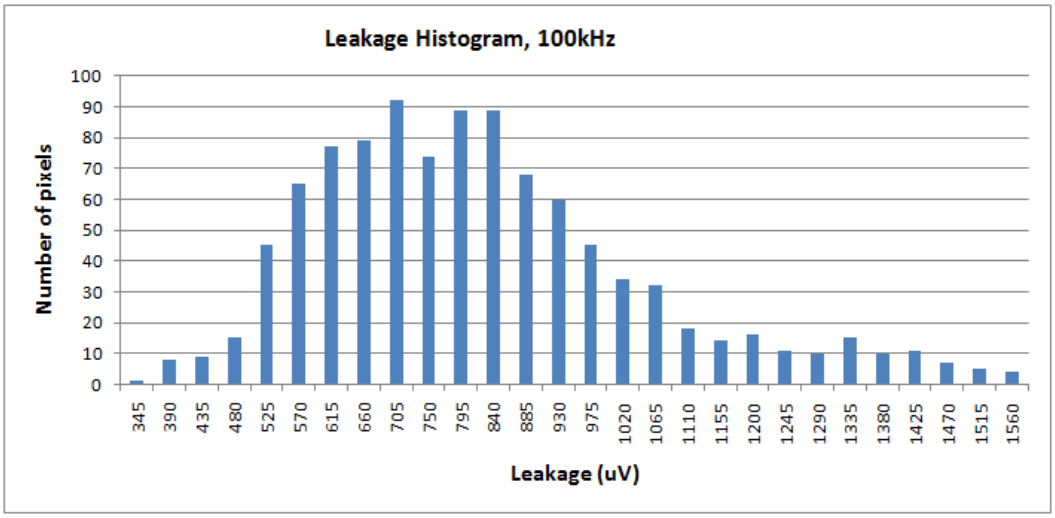


Figure 4.14: The histogram of pixel leakage at 100 kHz operation frequency. Average leakage becomes 820.5 µV.

However, in the leakage simulation, the resistive substrate leakage was ignored by setting g_{min} parameter of the simulation to 10^{-20}, while the default value was 10^{-12}. For g_{min} =2*10^{-14} leakage becomes 11 times greater than the previously simulated value. Consequently, the fact that the measured leakage deviates from the simulated value is acceptable. The leakage of 250 kHz data was calculated as well. Figure 4.15 shows the histogram of pixel leakage for 250 kHz operation. Average leakage becomes 27.9 ADC counts, which is 418.5 µV or 16 e^-. If the leakage had a linear relation with the frame period, we would

expect 2.5 times smaller leakage at 250 kHz when compared to 100 kHz. However, leakage came out to be 1.94 times smaller indicating that the linear relation is not valid. Note that in Section 3.2.2 both transient and dc leakage simulations were performed. Then the dc simulation results were compared with the transient simulation results by assuming a constant leakage during the frame period. Leakages became 3.62 e^-/frame and 4.1 e^-/frame implying that indeed the leakage varies over time, resulting in nonlinear relation. Hence, the measured leakage results do not contradict with the theory.

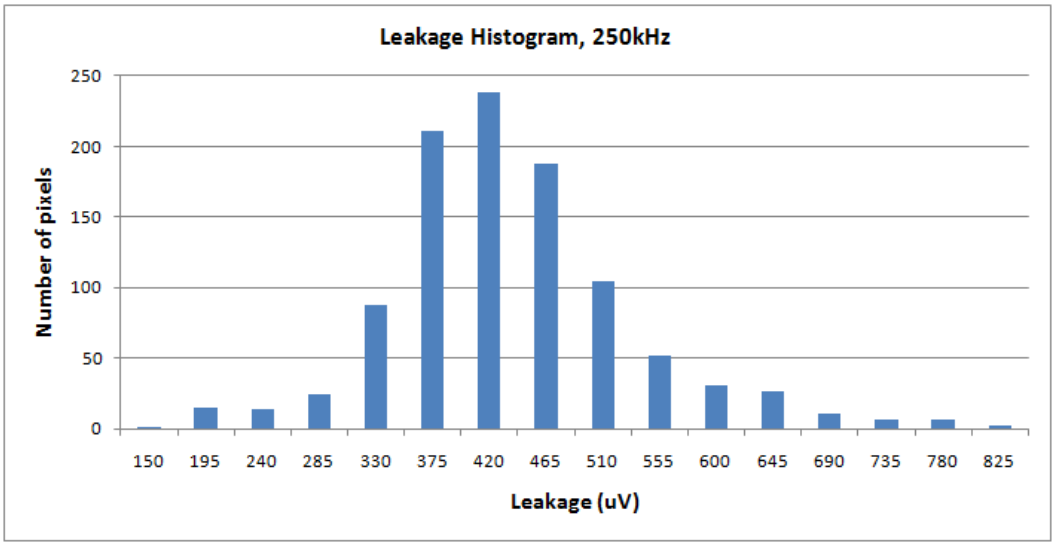


Figure 4.15: The histogram of pixel leakage at 250 kHz operation frequency. Average leakage becomes 418.5 µV.

Although measured leakage came out to be much larger than the noise level, unlike noise, leakage is a predictable event and can be accounted for during the tests. The leakage can drift with temperature in long duration tests, but that variation is expected to be slower than the events of DNA immobilization or hybridization. Consequently, it must not be hard to differentiate the true data from the leakage variation. Moreover, a setup can be

improved so as to maintain ambient temperature in order not to affect the measurements.

4.3 Summary and Conclusions

This chapter began with the description external hardware and test software to explain the test setup and the methods used to perform the electronic tests. The external components used to maintain the proper operation of the chip were shown in blocks. The fact that an FPGA is used to create an interface with the PC and the chip, and a C++ code is used to generate an easy to use control panel was mentioned. Then, the results of functionality and performance tests were given. The outputs of the chip were observed with an oscilloscope to verify functionality. Moreover, the written code was used to operate the chip as an image sensor and verify response of the pixels by partially illuminating the array. The noise tests were done and it came out to be 176.7 μV and 134.7 μV for 100 kHz and 250 kHz operation frequencies respectively, when the CDS was performed. The simulated and calculated result was around 100 μV. Since the dominating noise factor is the flicker noise of the pixel, which was also verified by the noise reduction as sampling rate increased, we argued that, the flicker noise model of the simulation is not precise. The lowest measured noise, which is 134.7 μV, corresponds to 5.1 e^-. When the CDS was not performed, the reset noise dominated and noise became approximately 34-39 e^-. The theoretical value for extracted pixel capacitance was 31.3 e^-, meaning that the real pixel capacitance is actually very close to the simulated value. The leakage was also measured to be 31 e^- for 100 kHz operation frequency, while the simulation result was 3.62 e^-. This large difference was a result of not accounting for the resistive substrate leakage in the simulation. Nonetheless, leakage is a predictable event and can be accounted for during measurements, consequently the chip has a sufficient performance to be used in biological tests.

CHAPTER 5

DNA TESTS

This chapter presents the post CMOS modification of the chip surface for suitable DNA immobilization, tests procedures and test results. Two kinds of tests were performed. We started with a single pixel test to verify the response of a pixel to different solution media and according to the feedback received from that test, surface was modified differently to perform a complete test of the chip.

5.1 Single Pixel Test

Single pixel test was performed by modifying surface such that the top metal of only one pixel was exposed to solution. The other pixels were covered by a nitride passivation layer. The exposed pixel was covered with gold as shown in Figure 5.1. The probe DNA used in this test had thiol modified 3' end and its sequence was 5'-TCTCACCTTC-3'-SH. Targets had complementary sequence of 3'-AGAGTGGAAG-5'. Both immobilization and hybridization were performed in 40 µL solution of 100 µM concentration. In Section 5.1.1 surface modification steps and the packaging technique are described, and then in Section 5.1.2 results of the performed tests are provided.

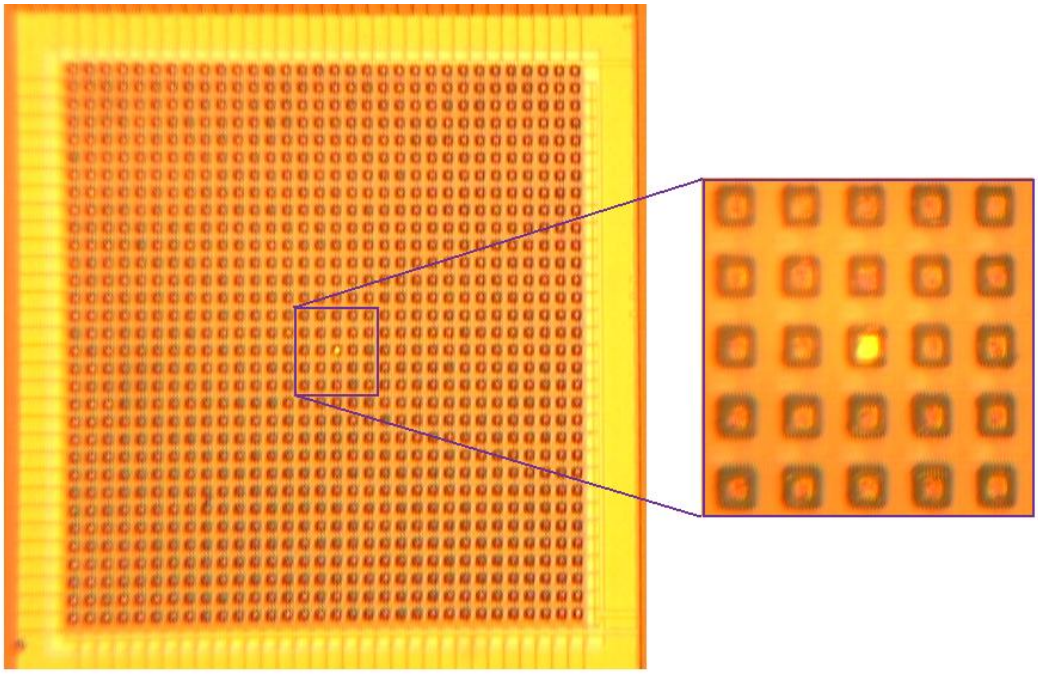


Figure 5.1: A microscope view of the chip surface with the single gold coated and exposed pixel. The other pixels are covered with a nitride passivation layer.

5.1.1 Post CMOS Surface Modification and Packaging

The surface modification of the chip was performed in METU-MEMS Center. Figure 5.2 shows process steps and a cross section of the packaged chip. The chip produced in XFAB CMOS FAB had passivation openings on pixels and bonding pads. Those opening were gold coated by lift off process. Then, a nitride layer was deposited over the chip and was etched from the surface of the single pixel and bonding pads. This enabled single pixel exposure and isolation of the rest of pixels. The chip was bonded to a dual in line package (DIL-40). Bonding pads were sealed and reservoir to contain DNA solution was formed by white epoxy as in Figure 5.3. The chip was tested with the setup shown in Figure 4.5.

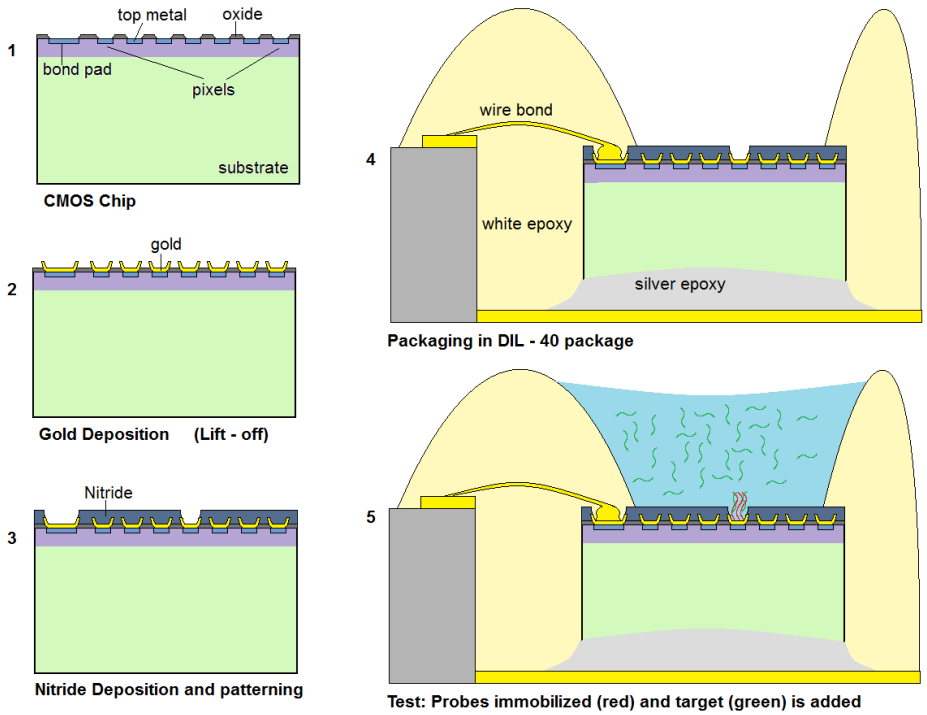


Figure 5.2: Illustration of the post-CMOS process (1-3), packaging (4), and testing (5) of the chip. 1-The CMOS chip with passivation openings on pixels and bonding pads. 2-Openings, gold coated by lift off process. 3- Nitride deposited and etched over a single pixel and bonding pads. 4,5- Chip attached to a DIL-40 package by silver epoxy, bonding pads isolated and DNA reservoir formed with white epoxy.

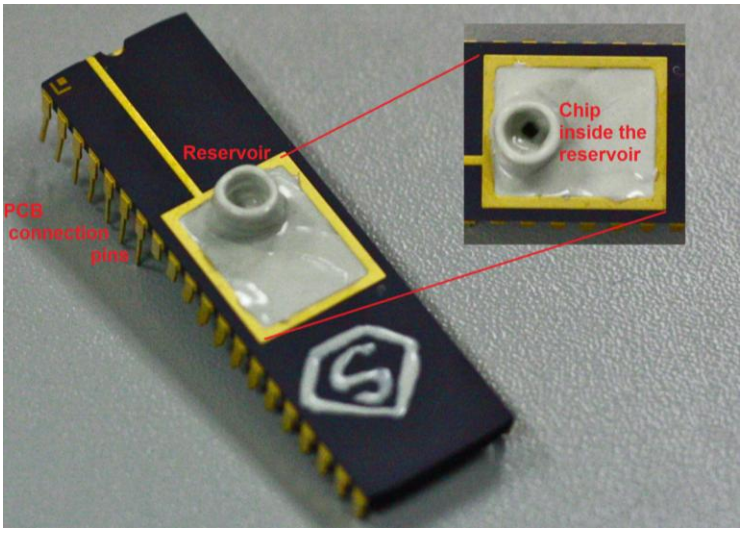


Figure 5.3: The chip bonded to a DIL-40 package and a white epoxy reservoir.

5.1.2 Performed Tests and Their Results

The DNA hybridizes and immobilizes better in acidic buffer solutions because, normally negatively charged DNA molecules repel each other while ions contained in buffer solution provide better alignment. However, using a buffer solution in our test setup might have had a negative impact on the sensitivity as we are trying to detect charge accumulation on the surface. Ions contained in buffer would make it harder to detect a DNA charge. To see the difference between the buffer and DI water we performed tests in KH_2PO_4 buffer solution and in DI water for about two hours. Figure 5.4 shows leakage variation of pixels over time for both cases.

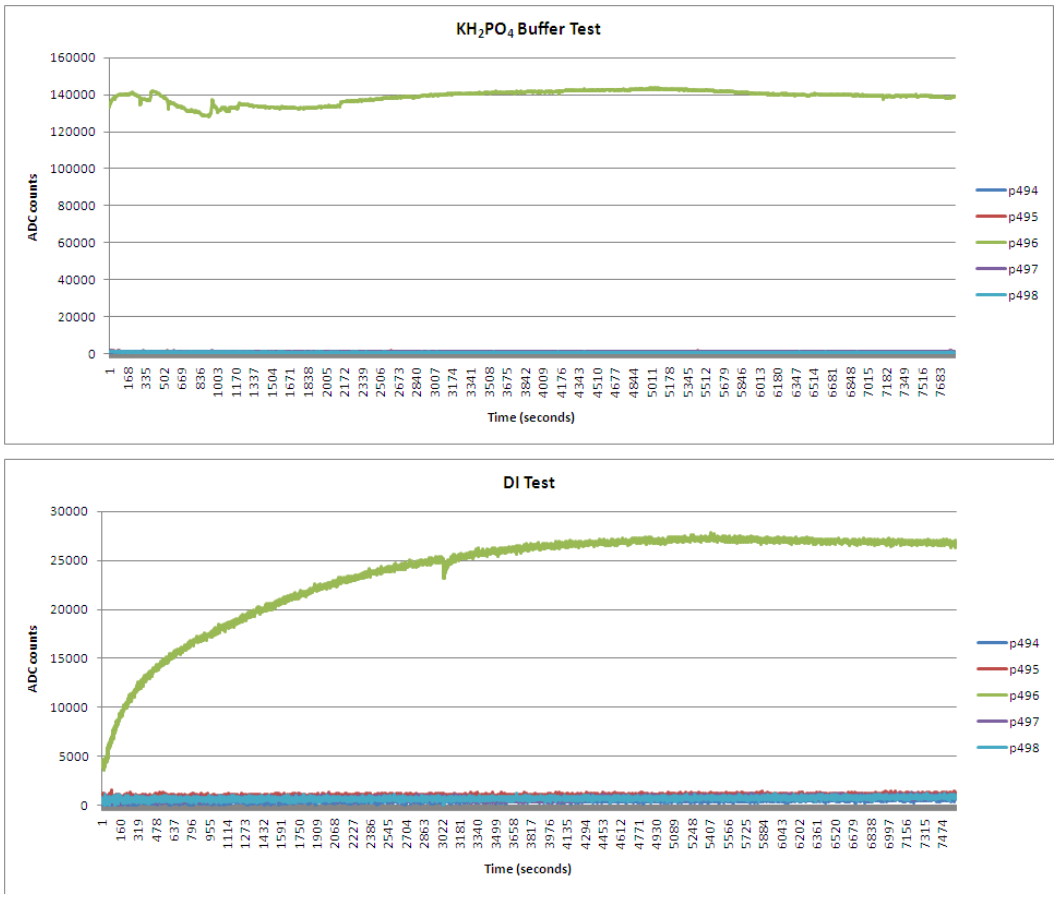


Figure 5.4: Leakage variation of pixels over time (the exposed pixel-p496 and the neighboring 4 pixels) in buffer and DI tests.

p496 (green) is the data corresponding to the exposed pixel, while the others are neighboring 4 pixels in the same row. The Y axis corresponds to a leakage per second, which is the sum of leakages of 50 frame pairs, as the scanning rate is 100 FPS and the leakage is evaluated by taking the difference of consecutive reset and non-reset frames as explained before. So to evaluate the leakage per frame in terms of voltage, reader is free to divide respective ADC counts value by 50 and multiple by 15 µV (LSB of the ADC), or to evaluate the leakage in terms of electrons, divide the calculated voltage by 26 $\mu V/e^-$ (conversion gain). In the rest of this thesis the leakage value will be given in ADC counts for better correlation with graphs.

As evident from Figure 5.4, exposed pixel was directly affected by the buffer solution and DI water. Since the other pixels were protected with nitride passivation, they were not affected by the solution at all. The leakage value of the other pixels was around 2000 counts, corresponding to 600 µV/frame, which is similar to performance test results provided in Section 4.2.2. Therefore the nitride passivation seems to work fine for pixel isolation purpose. The leakage in the buffer solution was enormously large and settled at 140000 counts corresponding to 42 mV/frame (much smaller than the voltage swing, so no saturation problem exists) while the leakage in case of DI water settled at 25000 counts. It would be hard to observe the effect of DNA inside the buffer solution because the leakage would be significantly dominated by buffer ions. Therefore, we performed the DNA tests inside DI water.

There are 1024 pixels and only 5 of them are shown in Figure 5.4. Most of the remaining passivated pixels had shown similar characteristics but few pixels had elevated leakage level. The number of such pixels increased after each test, which indicated that solution penetrated through possible cracks in the nitride more and more with each test and interacted with the pixels.

Overnight immobilization of probes in a 40 µL solution of 100 µM concentration was performed after the DI test. Figure 5.5 shows the result of 11 hours of immobilization. The leakage of the exposed pixel increased up to 110000, but did not exceed the buffer leakage level observed in the previous test. In this test however, isolated pixels started showing some increased leakage performance as well. This might have been due to two reasons: either solution penetrated through nitride cracks as explained before and reached those pixels or DNA molecules somehow adsorbed to the nitride, and induced charge on the other pixels. The latter possibility was eliminated later on, when we washed the surface after hybridization test and repeated the DI test. Had this effect been a result of charge induction due to the DNA, the next DI test would have resulted in normal leakage level again. However the leakage level of passivated pixels remained elevated in the following tests. Therefore, increased leakage of remaining pixels had to be due to cracked nitride, corrupted even more by repeated tests. Still, the exposed pixel showed increased leakage level, which initially was interpreted as the effect of immobilized probes.

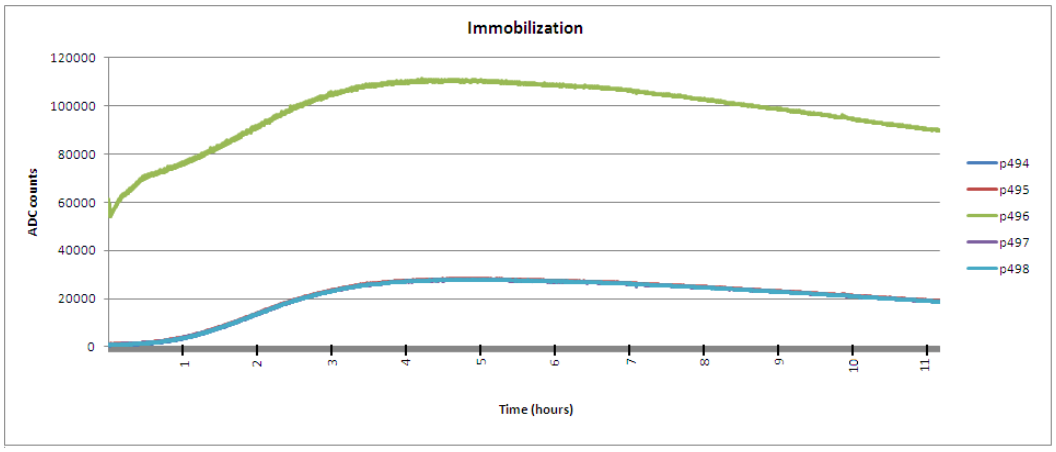


Figure 5.5: The result of the immobilization test performed in a40 µL, 100 µM probe DNA solution. Passivated pixels had elevated leakage level as well.

Hybridization with the complementary target sequence was performed next (Figure 5.6). Leakage of the exposed pixel increased again but its maximum value reached 85000 counts, which was less than in immobilization test. The same concentration and volume were used for the test. The passivated pixels had increased leakage as in immobilization test again. The surface was washed which resulted in sudden decrease of the leakage level, indicating that indeed the chip could sense the DNA presence (Figure 5.7).

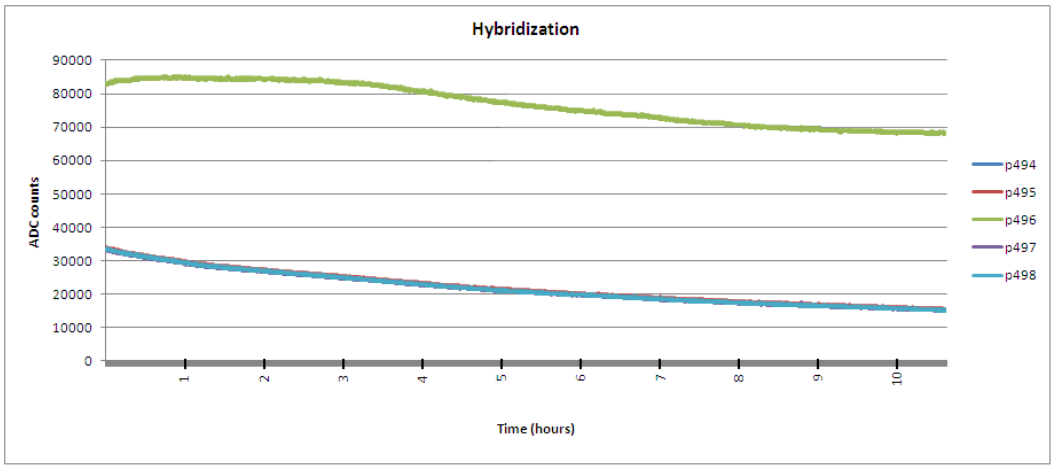


Figure 5.6: The hybridization test performed for about 10 hours in a40 µL, 100 µM target DNA solution.

These results seemed to be quite motivating and we decided to perform hybridization with a pM concentrated target solution. During that test we have observed that when the solution starts evaporating, leakage enormously increases exceeding even the leakage value of the buffer test. Then we realized that we have been monitoring ionic content of the solution rather than immobilized or hybridized DNA. A resistive path formed between the exposed pixel and ground by series combination of solution and the epoxy resistances was discharging pixels (Figure 5.8). Even though R_{epx} remained the same, ionic content of the solution changed R_{sol}, thus different leakage levels were observed for different solutions. In the final test with a pM concentration, as solution

evaporated, ionic concentration increased which resulted in smaller resistance and higher leakage.

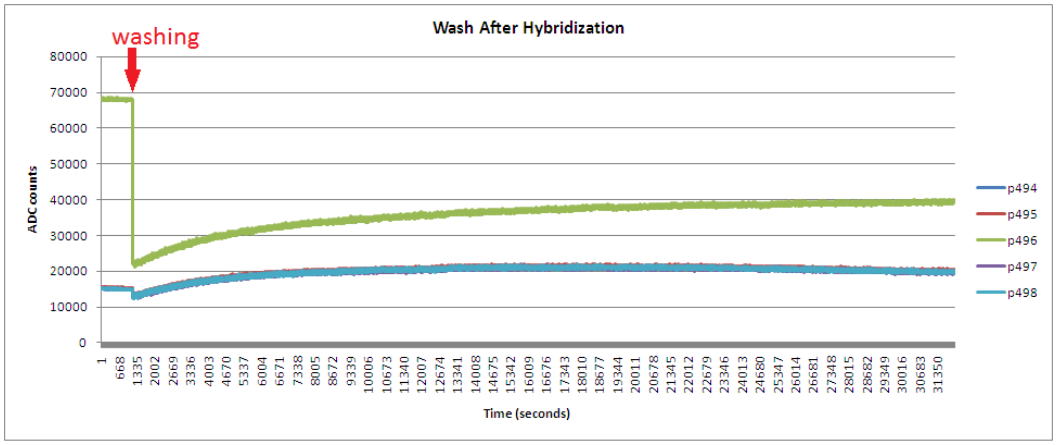


Figure 5.7: The washing and DI test performed after hybridization. Decrease in the leakage of the exposed pixel at the washing instant is observed.

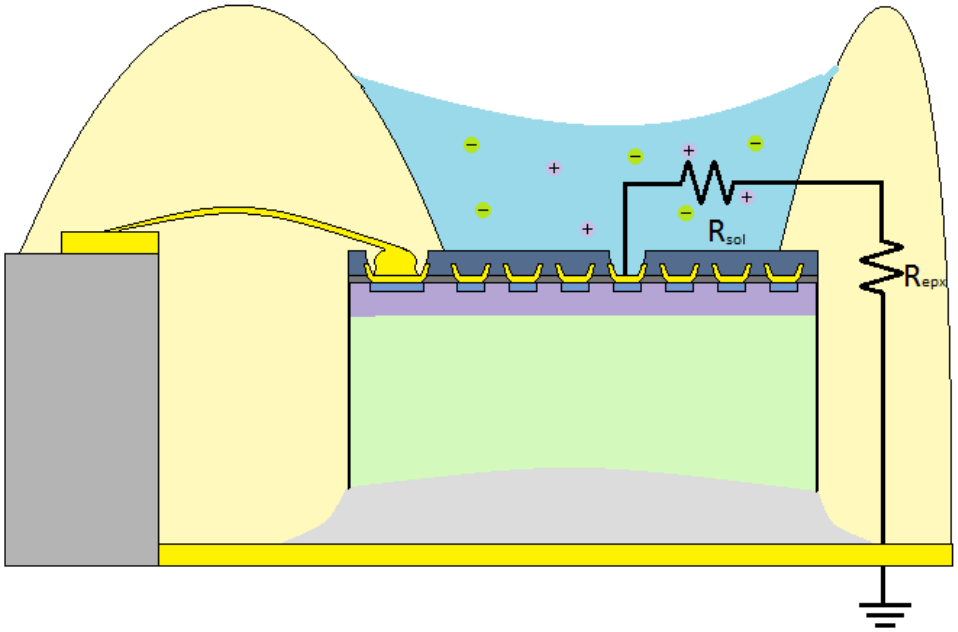


Figure 5.8: The resistive path formed between the pixel and ground, due to the series connection of solution and the epoxy resistances.

White epoxy is an insulating material, however because of the extreme sensitivity of the chip its resistance is not enough to provide proper isolation. Note that even the ions of DI water have increased the normal leakage value 10 times (Figure 5.4). Even in the buffer test, which is the most conductive case, leakage value was 140000 counts/seconds, which corresponds to 12.6 fA, and assuming pixel voltage to be around 2V, resistance comes out to be 80 TΩ.

Even though results of this experiment were misleading, they bare significance, because the next modifications and tests were done according to these results. We have proven that the chip is very sensitive to ions, confirming that it can be used for sensitive DNA detection with proper packaging. In initial buffer and DI tests, passivated pixels were not affected by solution, pointing out that nitride layer indeed can be used for isolation. Moreover we have decided not to use a package with metallic floor, but instead used a ceramic package in the next experiment, in order to avoid resistive leakage to ground. But even if a resistive leakage path to ground was avoided, in multiple pixel tests pixels would interact with each other through solution resistance and considering very small separation distance (10 µm) the value of the crosstalk resistance would be smaller than the resistance formed in the single pixel test. This would result in erroneous output data. Moreover charge to voltage conversion would be realized through complex impedance network rather than a single pixel capacitance as was modeled before. This might have had an impact on the sensitivity. Solutions indeed were observed to deteriorate chip performance during initial performance tests, when small droplets of DI water or salt solution were added on the pixel array. Hence, the new package had to resolve pixel isolation problem as well.

5.2 Full Chip Test

A new strategy was developed according to the results of the previous tests, so that multi-pixel test could be done. We have decided to use charge induction concept similar to conventional ISFET technology [41-47]. The surface of the chip was completely isolated by nitride to prevent pixel crosstalk. Then a polymer layer suitable for the DNA immobilization was incubated on the surface. The thickness had to be large enough to avoid cracks but much smaller than the width of the pixel detector metal in order not to prevent capacitive charge induction [53]. Therefore the thickness was chosen to be 0.5 μm. The following sections provide better description of post CMOS process and the results of performed tests.

5.2.1 Post CMOS Surface Modification and Packaging

The CMOS chip was coated with nitride and only the parts above the bonding pads were etched with laser to enable wire bonding. The chip was bonded to a ceramic package and a white epoxy reservoir was formed as before. The surface of the chip was covered with amino-propyl-triethoxy-silane (APTES) polymer, by overnight incubation of APTES on the surface in ethanol solution (Figure 5.9). This polymer has positively charged molecules that attract DNA and enable immobilization. However, in this case immobilization occurs directly through attraction of negatively charged backbone, rather than thiol group as before, so DNA attaches to APTES in a horizontal orientation. The drawback of this kind of immobilization is the fact that unless the surface is fully covered with probes, targets can also horizontally attach to the APTES resulting in nonspecific binding. We ignored this fact in the test because the main focus was on determining whether we could sense the DNA with this method or not. Figure 5.10 shows the packaged chip. First dry test and DI tests were performed

to check functionality of the chip. Then we continued with immobilization and hybridization tests.

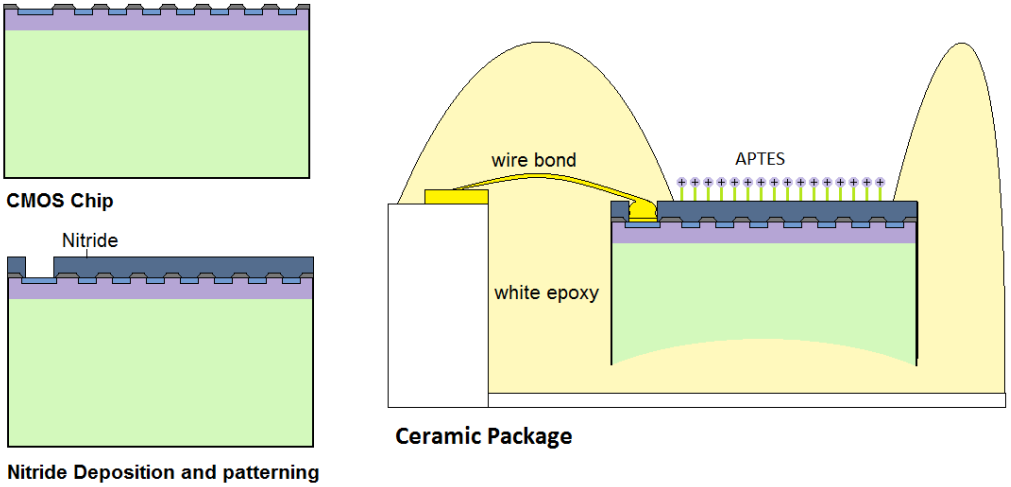


Figure 5.9: Post CMOS surface modification and packaging of the chip for the multi pixel test. The chip is fully coated with nitride, except for bonding pads. It is bonded to a ceramic package, and white epoxy reservoir is formed. The chip surface is modified with an APTES polymer.

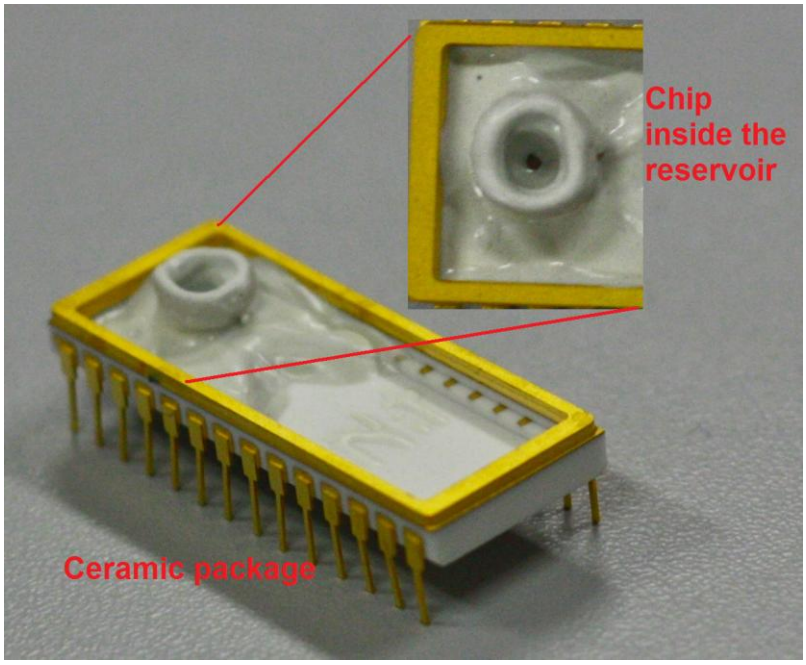


Figure 5.10: The nitride coated chip in a ceramic package.

5.2.2 Performed Tests and Their Results

Tests with a dry chip and in DI water were performed for half an hour to verify performance of the chip. Dry test was performed before, and DI test after surface APTES modification. Figure 5.11 shows results for 5 pixels. The rest of the pixels had similar characteristics. Relative performance of the pixels was almost the same in two tests meaning that the nitride layer was able to provide required isolation.

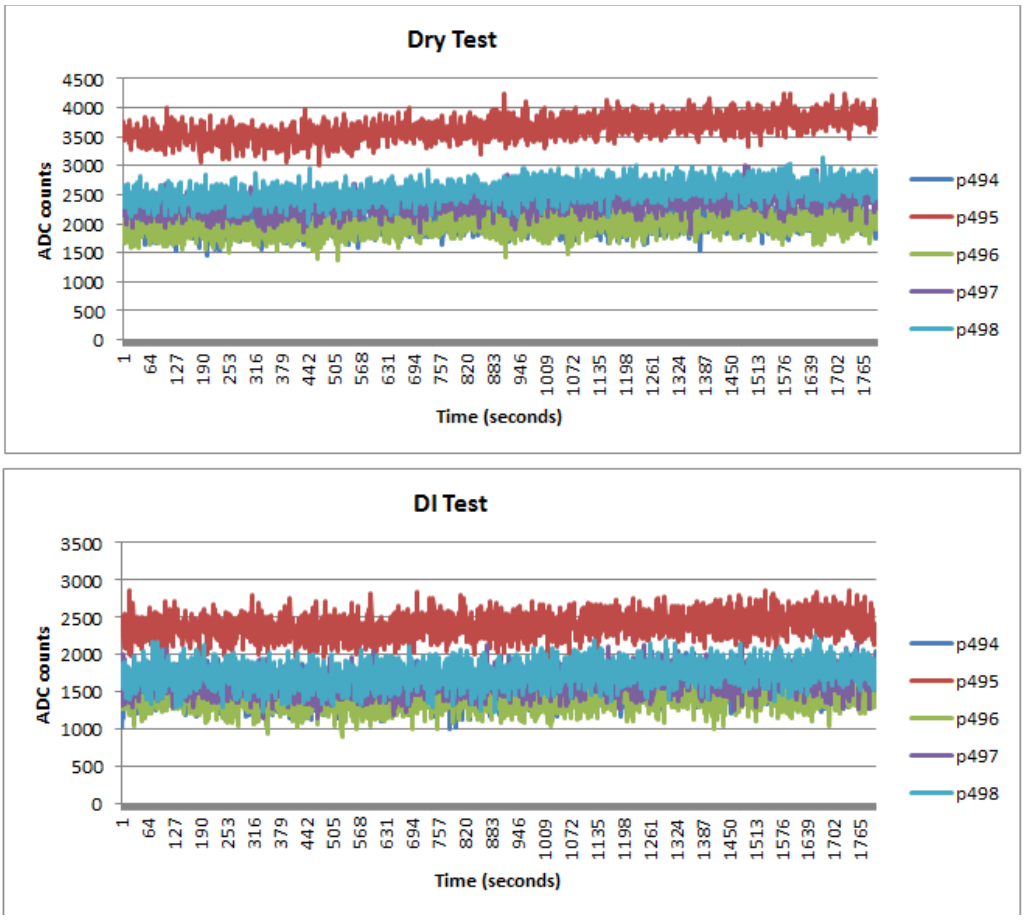


Figure 5.11: Results of leakage performance of 5 pixels for dry and DI tests performed on the chip for half an hour.

The only difference was the fact that the leakage values in DI test were slightly lower, which could be either a result of increased capacitance due to

APTES modification and existence of DI layer (the same leakage current would result in smaller voltage change), or because added DI cooled down the chip, resulting in smaller leakage performance. In any case, we would be able to observe the change of leakage value relative to DI level, so results seemed to be good enough to proceed with the DNA tests.

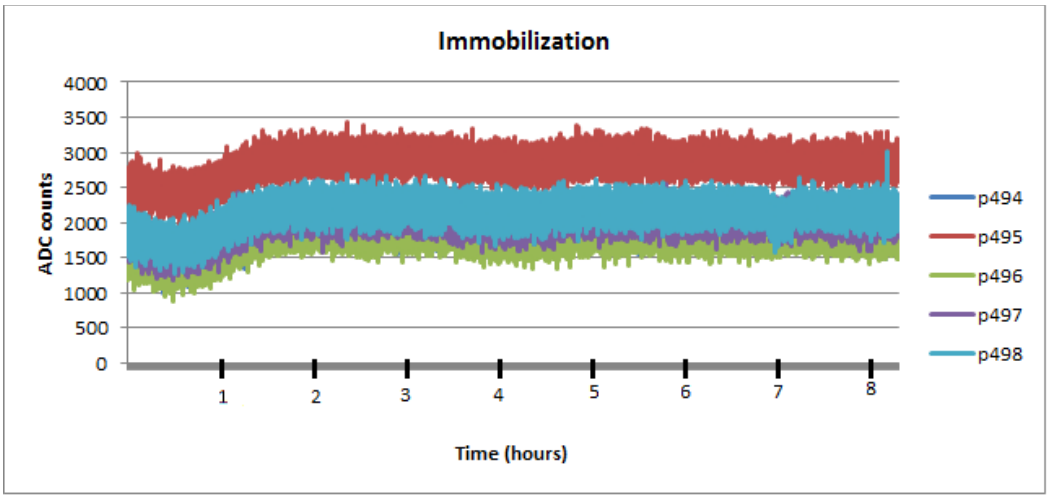


Figure 5.12: The immobilization test, leakage results for 5 pixels.

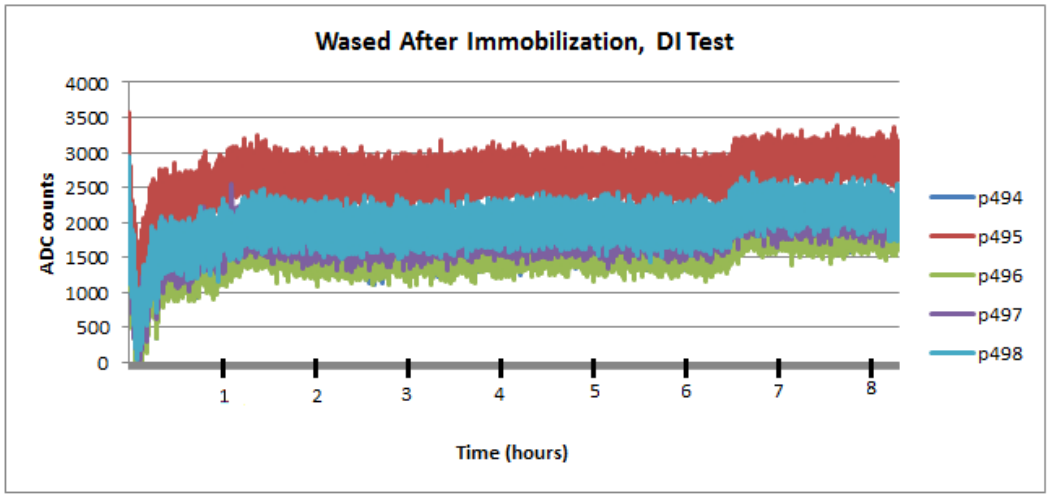


Figure 5.13: The chip surface was washed after hybridization and a DI test was performed for more than 8 hours.

Overnight immobilization was done in a 30 µL, 13µM solution. Results of about 8 hours are shown in Figure 5.12. The leakage value seemed to be settled after 1.5 hours and then remained stable. Then the chip was washed and 10 hours of DI test was performed (Figure 5.13). Hybridization with a30 µL, 1pM concentrated target DNA followed by another washing and DI test was done afterwards. Figure 5.14 and Figure 5.15 show leakage results for those tests.

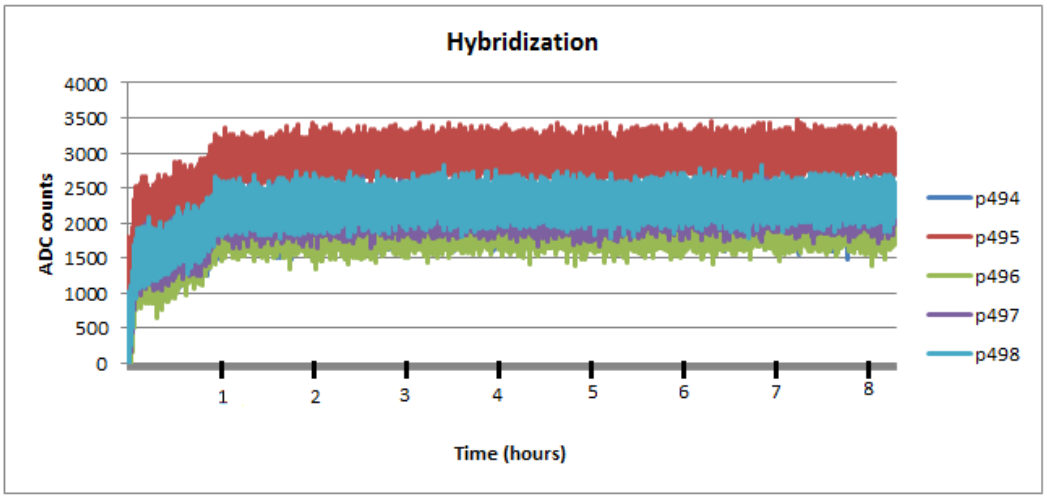


Figure 5.14: The hybridization test in a 1pM, 30uL target DNA solution.

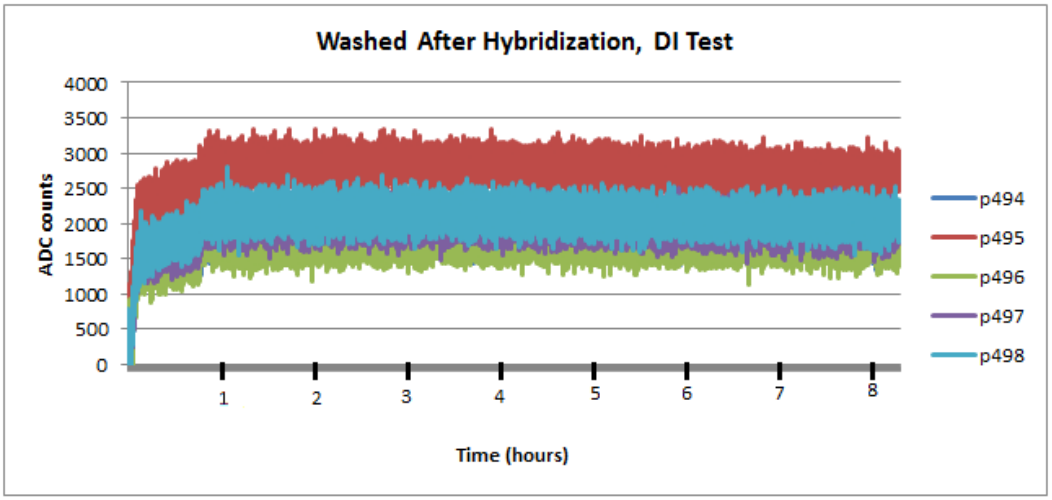


Figure 5.15: The DI test performed for 8 hours after washing the surface of the chip after hybridization test.

In all tests leakage has stabilized after about 1.5 hours. Only in the DI test performed after immobilization, leakage has shown another slight transition after 6.5 hours. We have been sealing the reservoir with a stretch film to prevent evaporation. Probably in that test the film did not properly cover the surface, and by 7 hours water evaporated resulting in such data (the difference in leakage of dry and wet cases was shown to exist during dry and DI tests before).

We were expecting to get some transient impulses resulting from the DNA during immobilization and hybridization tests, because the effect of the DNA charge could only be observed at the instant of attachment to the surface and would vanish after next pixel reset according to our expectations. However we have noticed that the steady state leakage value itself was changing with each test, and we thought that maybe immobilization and hybridization information could be extracted from those steady state values.

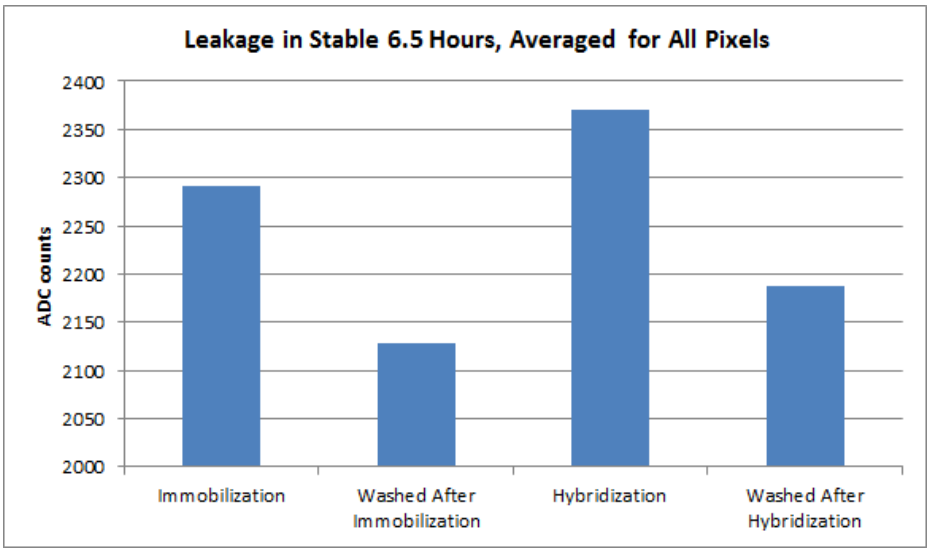


Figure 5.16: Average leakage of pixels for stable 6.5 hours, in performed tests.

When we measured the average leakage values of each pixel during stable 6.5 hours, and averaged all pixel leakages (except for the pixels of the first

and last row, to avoid edge effects), a very interesting result popped out that indeed made sense. Figure 5.16 shows the result of that calculation. Note that, during immobilization and hybridization leakage level was higher than in DI tests performed after washing. Moreover leakage of the hybridization exceeds the leakage of immobilization. Then the following claims can be propounded:

1- The chip can sense existence of the DNA as the steady state leakage in immobilization and hybridization cases exceeds the leakage in DI tests.

2- This change in leakage is not due to a resistive leakage trough solution and epoxy as in single pixel case due to the following three facts: First of all, the pixels are isolated with nitride which prevented such leakage even in single pixel test. Then, used package has a ceramic floor, so there is no available ground other than thin wire bond where the current can leak to. And finally, the soundest proof is that, the concentration in immobilization test was 13 µM, while concentration in hybridization test was only 1 pM. If the leakage was due to the ionic content, immobilization leakage would far exceed hybridization leakage. Despite this fact we observed the contrary effect and hybridization leakage exceeded immobilization leakage.

3- The full match sequence case can be differentiated from complete mismatch even with 1 pM concentration, as hybridization steady state leakage level exceeded immobilization level.

All these claims are based on the assumption that the existence of DNA alters the steady state leakage rather than resulting in transient leakage change. The nature of physics of this process is not fully understood though and is left for future work.

5.3 Summary and Conclusions

The DNA tests were performed in two steps. First, single pixel test was done by covering all pixels but one with a nitride passivation layer. The pixel had a gold coating. Buffer test, DI water test, immobilization of thiol modified probes and hybridization of targets was done. Acquired data showed characteristics depending on ionic content of the solution rather than the surface charge density of ions. This was interpreted as resistive leakage from the single exposed pixel to grounded metal floor of the package. Therefore multi-pixel tests seemed to be impossible with this kind of packaging, due to high sensitivity of the pixels.

To prevent problems observed in the single pixel test, conventional surface modification by isolating all pixels with a nitride passivation and depositing APTES polymer on surface for DNA immobilization was done. Moreover, a ceramic package was used instead of DIL- 40 package to prevent the leakage to ground through the metallic floor of the package. Immobilization with 13 µM and hybridization with 1 pM concentrated solutions in 30 µL volume was done with intermediate washing steps. Steady state leakage of DNA tests exceeded the leakage of DI water tests, indicating selectivity to DNA, and leakage of hybridization exceeded the leakage of immobilization indicating ability to differentiate between the full match and full mismatch sequences. This kind of behavior was surprising, as we expected steady state leakage to be the same for all cases, and DNA to result in transient leakage increase during surface attachment period. The nature of the process is not fully understood and is left for future research.

CHAPTER 6

CONCLUSION AND THE FUTURE WORK

This study presents a label free CMOS DNA microarray utilizing a pixel structure similar to a pixel of 3-T CMOS image sensor. The chip was fabricated in 0.35 µm, 4 metal CMOS process of XFAB. It is comprised of a 32 X 32, 15 µm pitch pixel array, and required digital and analog circuitry to transmit the analog pixel data to the output. External circuitry containing an 18 bit ADC to realize analog to digital conversion was implemented. An Opal Kelly XM3010 FPGA was used for storing the data and maintaining the PC interface. Test software, like the Verilog code for FPGA and chip control and the C++ code for data manipulation and storage were written. After verifying satisfactory operation of the system by electronic functionality and performance tests, DNA immobilization and hybridization tests were performed on the chip. Biological tests required post CMOS surface modification, which was done at METU MEMS Center. Two kinds of DNA tests were performed. The first one was a single pixel test. Post CMOS modification for this tests required gold coating of pixels followed by a nitride coating of the surface. The nitride was etched from the surface of only one pixel and bonding pads. Immobilization was performed with thiol terminated probes on gold surface. The results of the single pixel test led us to modify the surface structure and perform the next test, which was the multi pixel test. The surface modification required for multi pixel test was only a nitride deposition. The surface of none of the pixels was etched after nitride deposition, which significantly simplified the post CMOS process as lithography

was not required. The surfaces of the bonding pads were etched with laser to enable wire bonding. An APTES polymer was deposited on the nitride coated surface to enable horizontal DNA immobilization. Results of the multi pixel test have shown that the DNA detection is possible even with 1 pM concentrated solution. Results of the study can be summarized as follows:

1- The design aimed to have a low noise performance and dynamic range as wide as possible. This was achieved by implementing pixels with as small detection capacitance as possible. The CDS was performed in contrast to the similar study [56], to reduce the low frequency noises and the reset noise, and was shown to be effective. The measured noise came out to be 6.7 e^- with an optimum clock frequency of 100 kHz, and 5.1 e^- with increased clock frequency of 250 kHz, as 1/f noise was further suppressed.

2- The voltage swing of pixels was measured to be 650 mV which corresponds to 24603 e^-. This range is refreshed in every two frames with application of the pixel reset. Considering 6.7 e^- noise, the dynamic range can be calculated to be 71 dB. This range is quite enough because the maximum discharge observed in the single pixel buffer test came out to be only 42 mV/ frame.

3- The measured leakage was 820.5 µV/frame, corresponding to 31 e^-/frame. Being a predictable quantity, leakage does not affect the sensitivity of the chip too much, and can be accounted for with a smart software.

4- Theoretically, even a single DNA can be detected as it would carry electrons equal or twice as much as the number of its nucleotides. We have used 10 base pair long DNA's, while usually 25-20 base pair strands are used in microarrays. Then, considering 6.7 e^- sensitivity, minimum detection level is limited by immobilization and hybridization efficiencies rather than the chip's noise floor. These efficiencies can be improved by a proper surface modification

which is out of scope of this study. So far we have tried to detect 1 pM concentration as there is no example of this much sensitive detection with label free CMOS microarray in literature. Only SPR and microchips utilizing carbon nano-wires have been reported to demonstrate better sensitivity in fM range. The widely utilized and sensitive methods like QCM and fluorescence microarrays have pM sensitivity. The thin gate diamond ISFETs are reported to have 10 pM sensitivity. Eventually, our achievement has a potential to be a breakthrough in DNA microarrays considering its simple fabrication and high sensitivity, and noting the fact that the measured 1 pM sensitivity is not the limit of abilities of this chip.

The following items can be considered to be the future work, aimed to achieve more reliable and more sensitive results.

1- The surface modification should be revised. 0.5 µm nitride coating reduces the efficiency of charge induction. If possible, individual reservoirs with no passivation over pixels must be implemented for the best sensitivity.

2- The APTES modification should not be preferred to thiol immobilization, because its selectivity to probes and targets is not good and nonspecific binding probability with APTES is high. On the other hand, single stranded DNAs randomly attach to the APTES surface horizontally and no self-assembled monolayer is formed in this case, which further inhibits hybridization.

3- Tests should be repeated with different concentrations to verify obtained results, moreover, DNA samples with a single nucleotide mismatch should be ordered and tested to verify the ability of the chip to detect SNP.

4- The reason why DNA resulted in steady state leakage change in the multi pixel test must be analyzed and physics of occurring processes must be understood to better exploit the chip.

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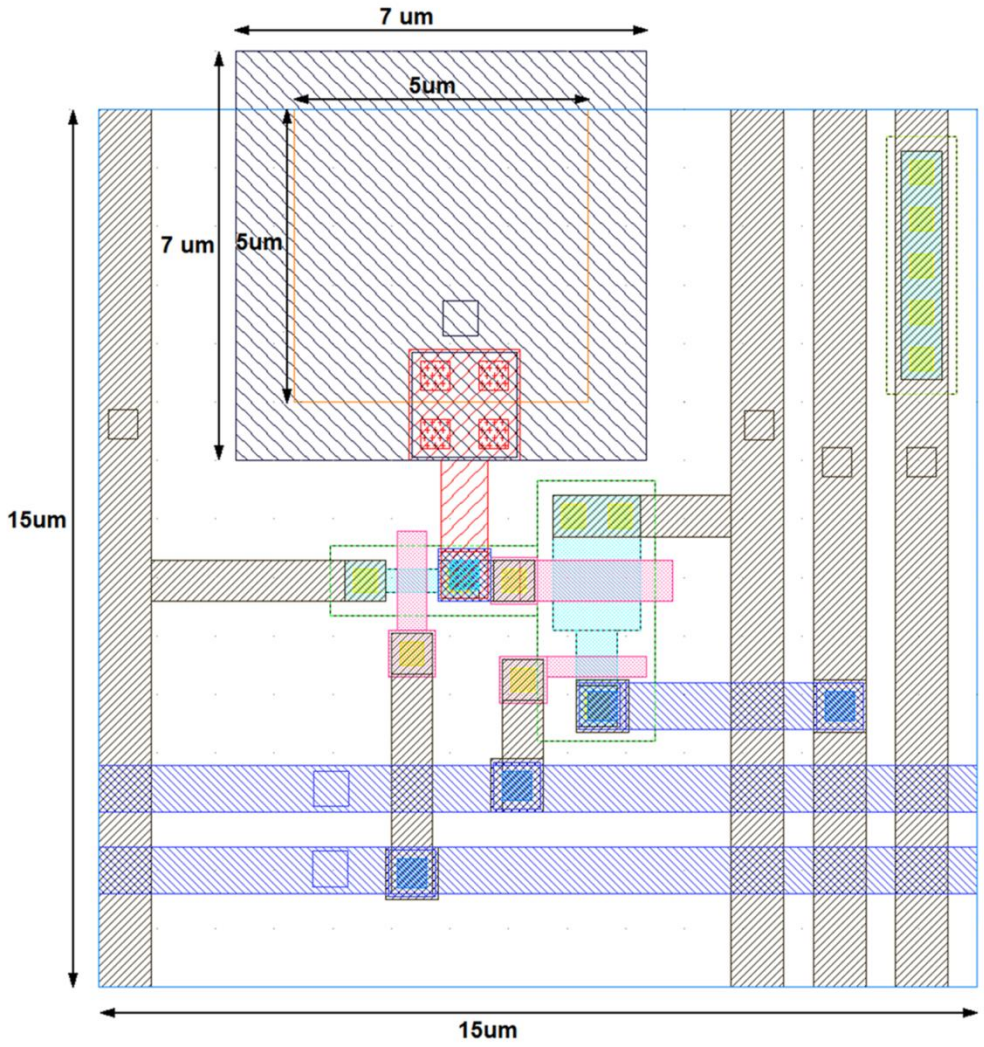
APPENDIX A

PIXEL LAYOUT



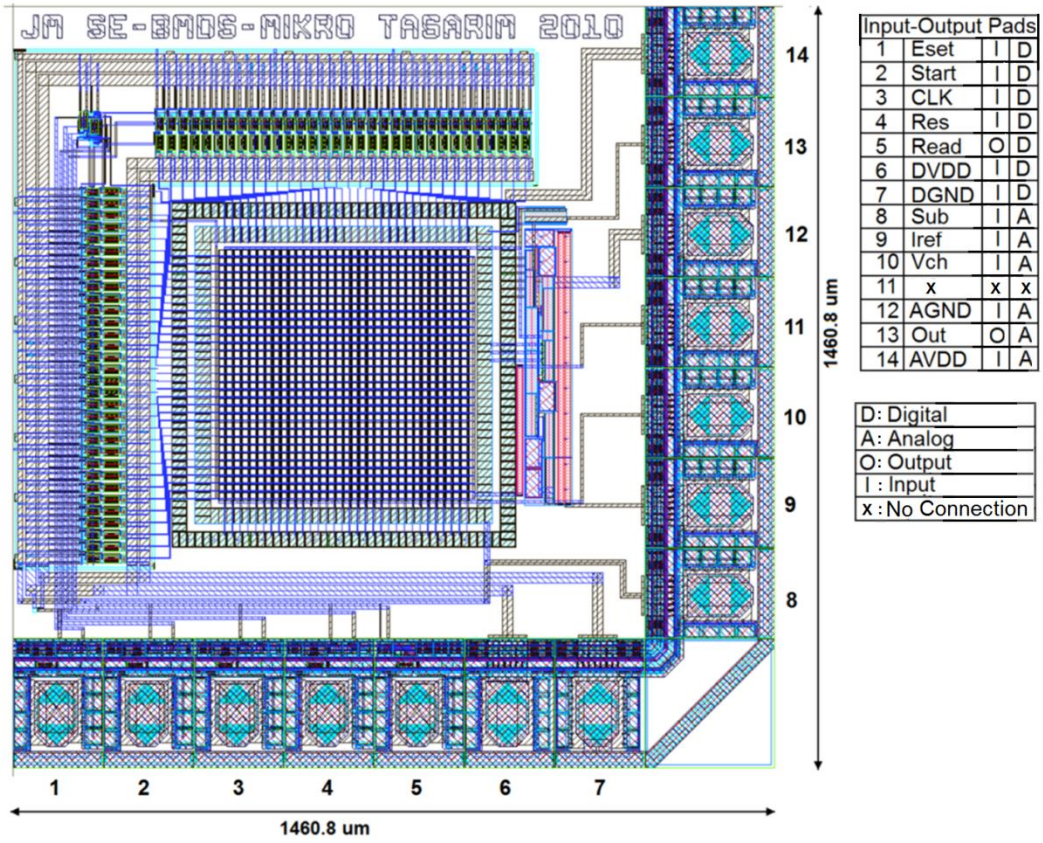
Notes:

1- The chip is fabricated in 0.35 µm, 1-poly, 4-metal, and 3.3 V CMOS process.

2- Pixels have 15 µm pitch. 7 µm X 7 µm detector metal is implemented with the top metal, and 5 µm X 5 µm pad opening is located at the center of that metal.

APPENDIX B

FULL CHIP LAYOUT



Input-Output Pads			
1	Eset	I	D
2	Start	I	D
3	CLK	I	D
4	Res	I	D
5	Read	O	D
6	DVDD	I	D
7	DGND	I	D
8	Sub	I	A
9	Iref	I	A
10	Vch	I	A
11	x	x	x
12	AGND	I	A
13	Out	O	A
14	AVDD	I	A

D: Digital
A: Analog
O: Output
I : Input
x : No Connection

Notes:

1- The chip is fabricated in 0.35 µm, 1-poly, 4-metal, and 3.3 V CMOS process.

2- Mikro-Tasarım San. ve Tic. Ltd. Şti. (the label on the chip) is an IC design company founded by Prof. Dr. Tayfun Akın and Assist. Prof. Dr. Selim Eminoğlu in November 2008 within the METU Technolopolis, a university incubation center for high-tech startups. Mikro-Tasarım San. ve Tic. Ltd. Şti. works on the development of low-noise, low-power imaging sensors and integrated electronics for sensors and sensor systems. It supported the design phase of this BMDS chip.