DESIGN AND FABRICATION OF A DETECTOR LOGARITHMIC VIDEO AMPLIFIER

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

MUSTAFA BARIŞ DİNÇ

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2011

Approval of the thesis:

DESIGN AND FABRICATION OF A DETECTOR LOGARITHMIC VIDEO AMPLIFIER

submitted by **MUSTAFA BARIŞ DİNÇ** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. İsmet Erkmen
Head of Department, **Electrical and Electronics Engineering** _____

Prof. Dr. Nevzat Yıldırım
Supervisor, **Electrical and Electronics Eng. Dept., METU** _____

Examining Committee Members:

Prof. Dr. Canan Toker
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Nevzat Yıldırım
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Sencer Koç
Electrical and Electronics Engineering Dept., METU _____

Assoc. Prof. Dr. Şimşek Demir
Electrical and Electronics Engineering Dept., METU _____

Tuncay Erdöl, M.Sc.
ASELSAN _____

Date: 15.09.2011

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name: Mustafa Barış Dinç

Signature:

ABSTRACT

DESIGN AND FABRICATION OF A DETECTOR LOGARITHMIC VIDEO AMPLIFIER

Dinç, Mustafa Barış
M. Sc., Department of Electrical and Electronics Engineering
Supervisor: Prof. Dr. Nevzat Yıldırım

September 2011, 102 pages

In this thesis a single stage detector logarithmic video amplifier is designed with a dynamic range of 40dB in 2-6GHz frequency band. Since the detector logarithmic video amplifier (DLVA) is used to convert the power of the RF signals to video voltages in logarithmic scale, it can be regarded as a logarithmic converter instead of logarithmic amplifier. The design is composed of two main parts: The Schottky diode detector rectifies the incoming RF signal and produces a video voltage and the logarithmic amplifier transforms the scale of the video voltage from linear scale to logarithmic scale in order to observe the RF signals with a wide amplitude range. The approximation of the logarithmic function is obtained by the summation of the output currents of the differential amplifiers operating as logarithmic stages. Offset voltage of the DLVA is minimized in order to obtain maximum sensitivity; this makes the detection of RF signals with low power possible.

The study is composed of mainly three parts: First, brief information about logarithmic amplification techniques is given and the circuit architecture is developed for logarithmic amplification and video detection, second these circuits are simulated and finally the design is implemented and tested.

Keywords: Logarithmic amplification, diode detector, differential amplifier

ÖZ

DEDEKTÖR LOGARİTMİK VİDEO YÜKSELTECİ TASARIMI VE ÜRETİMİ

Dinç, Mustafa Barış
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Prof. Dr. Nevzat Yıldırım

Eylül 2011, 102 sayfa

Bu tezde 2-6GHz bandında çalışan 40dB dinamik alana sahip olan tek kademeli dedektör logaritmik video yükselteci tasarlanmıştır. Detektör logaritmik video yükselteci RF işaretlerin gücünü logaritmik ölçekte video gerilimlerine çevirdiği için logaritmik yükselteç yerine logaritmik çevirici olarak görülebilir. Tasarım iki ana bölümden oluşmaktadır: Schottky diyot dedektör gelen RF işareti doğru akıma çevirir ve bir video gerilimi üretir ve logaritmik yükselteç de geniş bir genlik aralığındaki RF işaretlerin gözlemlenebilmesi için video geriliminin ölçeğini doğrusal ölçekten logaritmik ölçeğe dönüştürür. Logaritmik fonksiyon yaklaştırması logaritmik kademeler olarak kullanılan fark yükselteçlerinin çıkış akımlarının toplanmasıyla elde edilir. DLVA'nın offset gerilimi duyarlılığı en iyi seviyeye getirmek için en aza indirilmiştir; bu da düşük güçlü RF işaretlerin fark edilmesini mümkün kılar.

Bu çalışma temel olarak üç parçadan oluşmaktadır: İlk olarak, logaritmik yükseltme teknikleriyle ilgili özet bilgi verilmiş ve logaritmik yükseltme ve video tesbiti için devre mimarisi geliştirilmiştir, ikinci olarak bu devreler simule edilmiş ve son olarak da tasarım uygulanmış ve test edilmiştir.

Anahtar sözcükler: Logaritmik yükseltme, diyot dedektör, fark yükselteci

To My Family

ACKNOWLEDGEMENT

I would like to present my appreciation to my supervisor Prof. Dr. Nevzat YILDIRIM for his guidance and valuable recommendations.

I would like to thank my manager Dr. Muhammet Mustafa AKKUL for orientating me in this study and his support.

I would also like to thank my group leader Tuncay ERDÖL for his support and knowledge in the thesis work.

I would also like to thank to my colleagues for their understanding and tolerance.

I would also like to thank TÜBİTAK (The Scientific and Technical Research Council of Turkey) for their support during my M. Sc. Studies with their scholarship.

Finally, I am grateful to my family through all my life.

TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

CHAPTER 1

INTRODUCTION

Logarithmic amplifiers are used to compress the dynamic range of RF signals having a wide power range by providing high gain to low power signals and low gain to high power signals. Logarithmic amplifiers can be regarded as automatic gain circuits because of this gain adjustment. However; superior performance of the logarithmic amplifiers compared to the automatic gain circuits observed in impulse response and settling time makes them possible to be used in radar systems [1]. Some other application areas are electronic warfare and instrumentation [2].

1.1 Features of Logarithmic Amplifiers

Small logarithmic error, low tangential signal sensitivity (TSS), fast pulse response and high dynamic range are the desirable features of a logarithmic amplifier. These terms will be explained briefly in order to make the following sections clear.

- Logarithmic error: The logarithmic error is the deviation of the logarithmic response from the linear approximation obtained by best line curve fitting [3].
- Pulse response: The pulse response consists of rise, fall, settling and recovery times of the detected signal and it is determined by the video bandwidth [4].
- Frequency flatness: The variation of the output video voltage with frequency at a constant temperature and constant RF input power gives the frequency flatness [5].
- Tangential signal sensitivity (TSS): TSS is the minimum power level of the pulse to be detected.

- Logging dynamic range: Logging dynamic range is the widest range satisfying the specified logarithmic error interval [5].
- Dynamic range: Dynamic range is defined from TSS to the upper limit of the logging dynamic range [5].

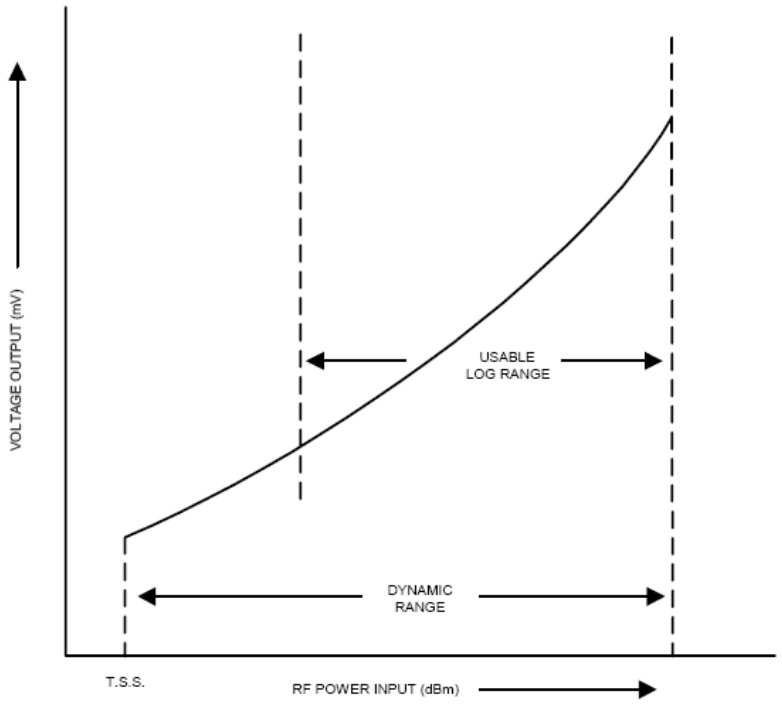

Figure 1-1: Dynamic range and logging dynamic range [5]

- Rise time: The time elapsed between 10% and 90% of the output voltage at the rising edge of the pulse is the rise time [5].
- Fall time: The time elapsed between 90% and 10% of the output voltage at the falling edge of the pulse is the fall time [5].
- Settling time: The time elapsed between the 10% of the output voltage to a time when the video output has reached a stable state at a specified tolerance at the rising edge of the pulse is the settling time [5].

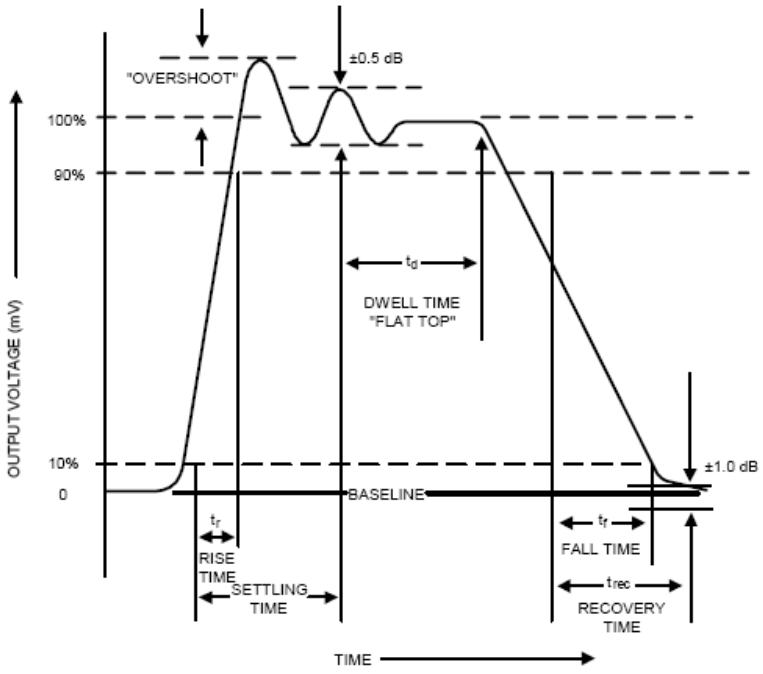

Figure 1-2: Pulse response [5]

1.2 Classification of Logarithmic Amplifiers

Logarithmic amplifiers can be classified into two basic types according to the demodulation and non-demodulation of the RF signal [6]:

a) True logarithmic amplifiers

b) Demodulating logarithmic amplifiers

1.2.1 True Logarithmic Amplifiers

The preserved phase information of the incoming signal makes the true logarithmic amplifiers possible to be used in moving target identification (MTI) radar systems since the logarithm of the signal is provided without detecting or demodulating the signal [3][7]. The output is a carrier frequency with voltage amplitude directly proportional to the logarithm of the incoming signal power level.

Two basic circuit topologies are used to obtain true logarithmic amplifiers [6]:

1. Series linear-limit logarithmic amplifier
2. Parallel-summation logarithmic amplifier

1.2.1.1 Series Linear-Limit Logarithmic Amplifier

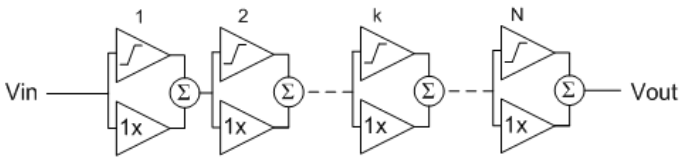

Figure 1-3: Series linear-limit logarithmic amplifier [6]

The most widely used circuit topology for the true logarithmic amplifiers is shown in Figure 1-3. The topology is constructed by the cascade connection of the dual gain stages which consist of a unity gain stage and a high-gain path. Both of the gain paths are fed through the same input and their outputs are summed after amplification. The high gain stage has a smaller compression point and saturates before the unity gain stage which has a high compression point relative to the high-gain stage [6].

A circuit topology for a dual gain stage is given in Figure 1-4 [4][7][8].

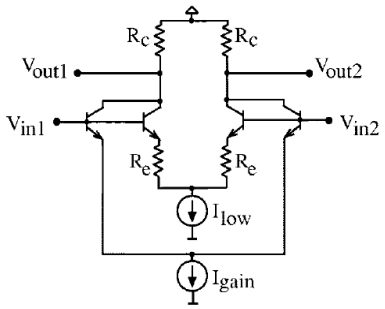

Figure 1-4: High-gain limiter and unity-gain buffer in parallel [6]

Emitter degeneration is used to provide low gain and the high gain stage uses the undegenerated version.

Signals with low power will be amplified; however, high-gain path will be compressed for high power signals and only the unity gain buffer will be effective. The gain change can be seen in Figure 1-5.

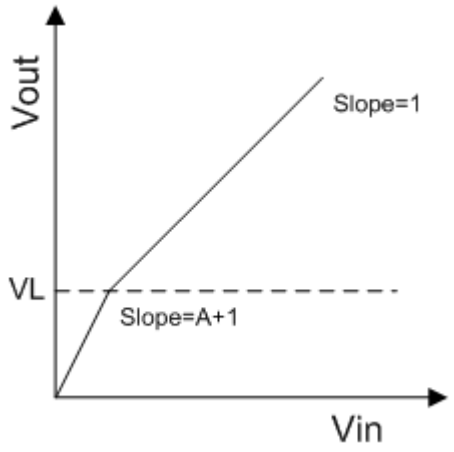

Figure 1-5: Voltage-gain characteristics of one dual-gain stage [9]

Cascading the dual gain stages provides the logarithmic response obtained from the piecewise approximate linear line as seen in Figure 1-6. The dual gain stages begin to compress from the last stage to the first stage producing a constant voltage.

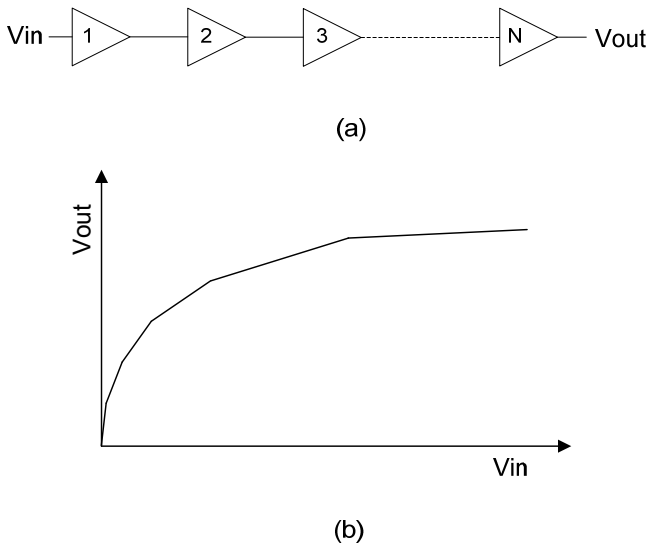

Figure 1-6: (a) Cascaded dual gain stage amplifier (b) Transfer characteristics [7]

The logarithmic response depends on the number of the dual gain stages and their gain. The number of the dual gain stages can be increased to obtain a wider dynamic range or the gain of the dual gain stages can be increased; but increasing the gain results in a larger logarithmic error. In order to reduce the logarithmic error the number of dual gain stages with small gain must be increased. At the same time, the dual-gain stage parameters, A and V_L, must be optimized to obtain a good logarithmic response. V_L has a deterministic effect on the pulse response of the logarithmic amplifier. Reducing V_L provides the desired logarithmic accuracy by decreasing the logarithmic slope and preventing the devices to go too deeply into the nonlinear region. However, this results in the reduction of small signal bandwidth due to the larger Miller effect resulting from the first amplifying differential pair. High-gain path is effective in the bandwidth of each dual-gain stage. Since the unity gain buffer has low gain and high current it does not dominate the bandwidth performance [3].

Since cascade connection is used in this topology, all stages will be affected nearly in the same manner by process variations. For instance, if the gain of one dual gain stage is decreased or increased, the logarithmic slope will also decrease or increase in

the same way; however this does not cause a change in the logarithmic response of the amplifier. Compensating the gain variation of this stage with another stage is the solution as expected. Increasing the number of dual-gain stages will provide a wider dynamic range [6]. Cascading the dual gain stages also solves the phase equalization problem [7].

Because of the cascading structure the unity gain buffer in the last stage must buffer the signal generated by the preceding stages. Considering the current values for high-gain and low gain paths in Figure 1-4, this results in a constraint that [6]

$$\frac{I_{low}}{I_{gain}} > N \qquad (1\text{-}1)$$

where N is the number of dual-gain stages

Since I_{gain} may be required to be large for amplification, it is obvious from (1-1) that I_{low} must be large in the same manner. Large devices with high parasitic capacitances will be needed to obtain this high I_{low} current. However, this poses a restriction in the bandwidth. The buffer gain can be decreased smaller than unity to solve this problem, so they require a larger input voltage to limit and their current can be decreased. The parasitic capacitance of the unity-gain buffer can still load the gain stage in parallel with it even if smaller devices are used [6].

The design of the high gain path is a crucial point in this approach. The high-gain path should have a significant small signal gain and much lower limiting level. The phase shift between the high-gain path and the unity-gain buffer should ideally remain constant with input signal level at every frequency in the operating bandwidth [9].

Another constraint in the design of a true logarithmic amplifier is the accuracy of the unity gain buffer of each stage to prevent the generation of a nonlinear logarithmic response curve; this problem cannot be corrected after the logarithmic amplifier unless another nonlinear device is used [9].

1.2.1.1.1 Mathematical Model [7]

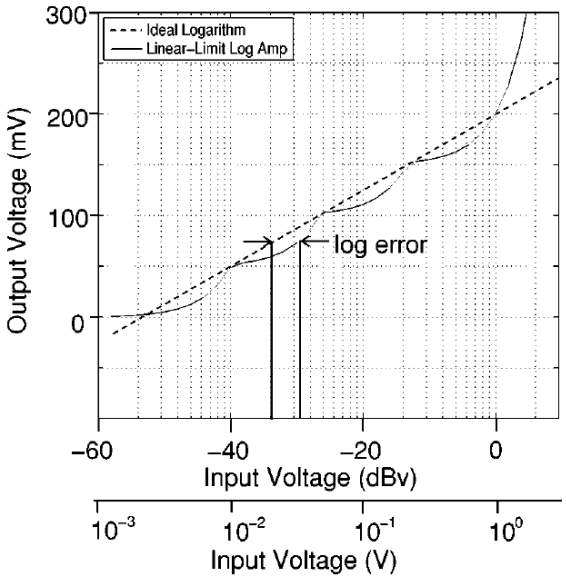

Figure 1-7: Linear-limit logarithmic amplifier response [6]

The desired logarithmic response by the series linear-limit method is seen in Figure 1-7. The response consists of a series of straight lines with breakpoints.

Consider a series linear-limit logarithmic amplifier consisting of N identical dual gain stages with a high gain value of A.

For a dual-gain stage, not limiting;

$$V_o = (A+1)V_{in} \tag{1-2}$$

For a limiting dual gain stage;

$$V_o = V_{in} + V_L \tag{1-3}$$

where V_L is the limiting voltage

At the verge of limiting,

$$V_{in} = \frac{V_L}{A} \tag{1-4}$$

$$V_o = V_L\left(1 + \frac{1}{A}\right) \tag{1-5}$$

It is explained that the dual gain stages begin to saturate from the last stage to the first stage. Assume the m_{th} stage is at the verge of limiting, this means that the dual gain stages following the m_{th} stage reached their limiting values; and the dual gain stages preceding the m_{th} stage are amplifying.

The input of the m_{th} stage is

$$V_{in_m} = \frac{V_L}{A} \tag{1-6}$$

which is amplified through the preceding stages of the m_{th} stage with an amplification factor of (A+1). This amplification is expressed as;

$$V_{in_m} = V_{in}(A+1)^{m-1} \tag{1-7}$$

Equating these two expressions gives;

$$\begin{aligned} \frac{V_L}{A} &= V_{in}(A+1)^{m-1} \\ m-1 &= \log_{A+1}\left(\frac{V_L}{AV_{in}}\right) \end{aligned} \tag{1-8}$$

The output voltage of the logarithmic amplifier when the m_{th} stage is at the verge of limiting is

$$V_o = (N-m)V_L + \left(1 + \frac{1}{A}\right)V_L = V_L\left[N + \frac{1}{A} - (m-1)\right] \tag{1-9}$$

Substituting (1-8) in (1-9) gives

$$V_o = \left[N + \frac{1}{A} + \log_{A+1}\left(\frac{AV_{in}}{V_L}\right)\right]V_L \tag{1-10}$$

(1-10) proves the logarithmic relation between the input voltage and the output voltage.

Since the total gain of each gain stage is (A+1) and the number of the dual-gain stages is N, the dynamic range of the series linear-limit true logarithmic amplifier is $(A+1)^N$.

1.2.1.2 Parallel Summation Logarithmic Amplifier

The high and low gain paths are separated to prevent loading observed in the series linear limit case [6]. The logarithmic response depends on the number of gain stages and their gain as in the true logarithmic amplifier case. The number of amplifiers or the amplifier gains should be increased to get a wide dynamic range. However, larger amplifier gain results in larger logarithmic error. Decreasing the gain causes a smaller logarithmic error; but, at the same time makes the dynamic range narrower [7]. The minimum logarithmic error is obtained by increasing the number of amplifier stages with reduced gain [9]. The amplifier explained in [10] shows that the parallel summation provides high bandwidth and logarithmic slope while consuming relatively low power.

Two methods, progressive-compression method and parallel-amplification method, can be used to obtain parallel summation logarithmic amplifiers.

1.2.1.2.1 Progressive-Compression Parallel Summation Logarithmic Amplifier [6]

The progressive-compression parallel summation logarithmic amplifier topology shows a great similarity with the series linear-limit method because of the cascaded gain stages as seen in Figure 1-8. However, the voltages from each gain stage are converted to currents with transconductance elements having the same slope but different limiting current to achieve a good logarithmic response. The currents are summed in parallel and the total current constitutes the output signal.

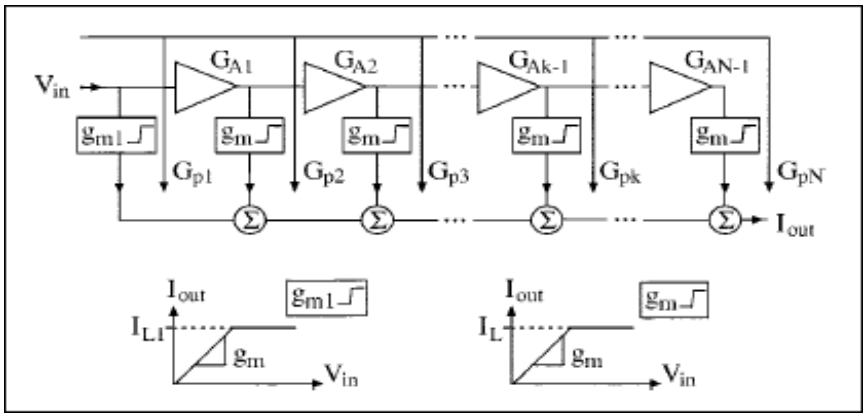

Figure 1-8: Progressive-compression parallel summation logarithmic amplifier [11]

In the progressive compression parallel summation method the phase delays of each current component is different due to the number of gain stages they are amplified. For example, the current maintained from the first transconductance element will have a zero phase lag because of not undergoing any gain stages; however, the current maintained from the last transconductance element will have a high phase lag due to the output capacitances of each gain stages. Delay amplifiers can be used to obtain currents with equal phase lag [6].

Similar to the series linear-limit logarithmic amplifiers, increasing the number of cascaded amplifiers results in a wider dynamic range.

1.2.1.2.2 Parallel-Amplification Parallel Summation Logarithmic Amplifier [6]

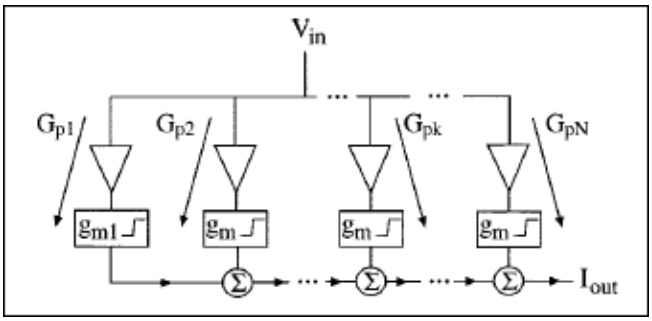

Figure 1-9: Parallel-amplification parallel summation logarithmic amplifier [6]

The parallel amplification method is another type of parallel summation. Figure 1-9 shows that, different from the previous methods, each gain path is independent of each other and the parallel summation of the currents obtained from the transconductance elements constitutes the output signal.

Compared to the progressive compression method, the parallel amplification method is efficient in low dynamic range applications; and, the phase and group delay matching are improved [6].

Increasing the number of amplifier stages to achieve a wider dynamic range in successive detection logarithmic amplifiers (SDLA) reduces the bandwidth and the system stability will be deteriorated. These problems can be solved by the parallel amplification parallel summation logarithmic amplifiers [12].

1.2.1.2.3 Mathematical Model [6]

For both of the parallel summation techniques the desired transfer function is seen in Figure 1-10. A logarithmic relationship will be proved between the input voltage and the output current. First, some definitions must be made to understand Figure 1-10 and associate with the previous figures, Figure 1-8 and Figure 1-9.

N : the number of stages

A : the factor increase in the input voltage

I_S : the increment in the output current corresponding to the factor increase in the input voltage

C : the minimum current level that can be read at the output

G_k : total circuit gain

G_{pi} : individual gain of each amplifier

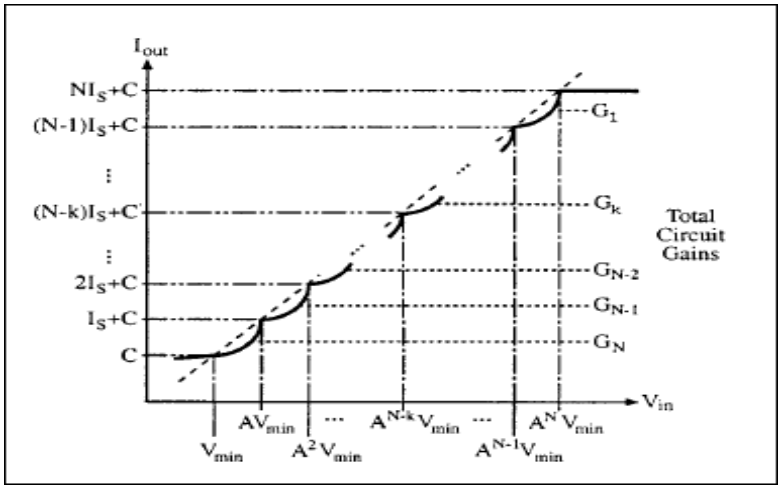

Figure 1-10: Parallel summation logarithmic amplifier transfer function [6]

It is known that the input is amplified by all stages unless the compression point is reached by any of the amplifier stages. The number of stages effective in amplification decreases beginning from the outermost amplifier. So, the total circuit gains are expressed as;

$$
\begin{aligned}
&G_N = G_{p1} + G_{p2} + ... + G_{pN} \\
&G_{N-1} = G_{p1} + G_{p2} + ... + G_{p(N-1)} \\
&..... \\
&G_k = G_{p1} + G_{p2} + ... + G_{pk} \\
&..... \\
&G_1 = G_{p1}
\end{aligned}
\qquad (1\text{-}11)
$$

The current supplied from the amplifier stages that have already reached their compression point and the current from the amplifier stages not saturated constitute the output current of the logarithmic amplifier. The saturated amplifiers supply a

fixed current which is denoted by I_L. When the graphical solution given in Figure 1-10 is matched with the currents obtained from the circuit topology, the currents can be equated to determine the total circuit gains.

$$
\begin{aligned}
&C = V_{\min} G_N \\
&I_S + C = A V_{\min} G_{N-1} + I_L \\
&2I_S + C = A^2 V_{\min} G_{N-2} + 2I_L \\
&3I_S + C = A^3 V_{\min} G_{N-3} + 3I_L \\
&\cdots\cdots\cdots\cdots \\
&(N-k)I_S + C = A^{N-k} V_{\min} G_k + (N-k)I_L \\
&\cdots\cdots\cdots\cdots \\
&(N-2)I_S + C = A^{N-2} V_{\min} G_2 + (N-2)I_L \\
&(N-1)I_S + C = A^{N-1} V_{\min} G_1 + (N-1)I_L \\
&NI_S + C = V_{\min} G_N + NI_L
\end{aligned}
\tag{1-12}
$$

Let $I_S = I_L$ for simplicity.

$$
\begin{aligned}
&C = V_{\min} G_N && C = V_{\min} G_N \\
&I_S + C = A V_{\min} G_{N-1} + I_L && C = A V_{\min} G_{N-1} \\
&\cdots\cdots\cdots\cdots && \cdots\cdots\cdots\cdots \\
&(N-k)I_S + C = A^{N-k} V_{\min} G_k + (N-k)I_L \Rightarrow && C = A^{N-k} V_{\min} G_k \\
&\cdots\cdots\cdots\cdots && \cdots\cdots\cdots\cdots \\
&(N-1)I_S + C = A^{N-1} V_{\min} G_1 + (N-1)I_L && C = A^{N-1} V_{\min} G_1 \\
&NI_S + C = V_{\min} G_N + NI_L && C = V_{\min} G_N
\end{aligned}
\tag{1-13}
$$

Equating the expressions in (1-13) gives,

$$
\begin{aligned}
&A^{N-2} V_{\min} G_2 = A^{N-1} V_{\min} G_1 \Rightarrow G_2 = A G_1 \\
&A^{N-3} V_{\min} G_3 = A^{N-2} V_{\min} G_2 \Rightarrow G_3 = A G_2 \Rightarrow G_3 = A^2 G_1 \\
&A^{N-4} V_{\min} G_4 = A^{N-3} V_{\min} G_3 \Rightarrow G_4 = A G_3 \Rightarrow G_4 = A^3 G_1 \\
&\cdots\cdots\cdots\cdots
\end{aligned}
\Rightarrow G_k = A^{k-1} G_1 \tag{1-14}
$$

It is obvious from the Figure 1-8 and Figure 1-9 that $G_{p1} = g_{m1}$ and the slopes g_m and g_{m1} are the same, except their limiting values, I_L and I_{L1}. Then, the total circuit gains according to the expression in (1-14) are found as;

$$
\begin{aligned}
&G_1 = G_{p1} = g_m \\
&G_2 = g_m A \\
&\text{.....} \\
&G_k = g_m A^{k-1} \\
&\text{.....} \\
&G_{N-1} = g_m A^{N-2} \\
&G_N = g_m A^{N-1}
\end{aligned}
\qquad (1\text{-}15)
$$

After finding these expressions for parallel summation it is possible to determine the gains in parallel-amplification and progressive-compression methods.
By using (1-11) and (1-15), the individual gain of each summed stage, G_{pi}, is found as;

$$
\begin{aligned}
&G_{p1} = g_m \\
&G_{p2} = g_m (A-1) \\
&G_{p3} = g_m A(A-1) \\
&\text{.....} \\
&G_{pk} = g_m A^{k-2}(A-1) \\
&\text{.....} \\
&G_{pN} = g_m A^{N-2}(A-1)
\end{aligned}
\qquad (1\text{-}16)
$$

The gain values found in (1-16) corresponds to the gains in parallel amplification method. The coefficient g_m is the transconductance coefficient.

Using the gain values found in (1-16) the gains used in the progressive compression method are;

$$
\begin{aligned}
&G_{A1} = A-1 \\
&G_{A2} = A \\
&\text{.....} \\
&G_{Ak-1} = A \\
&\text{.....} \\
&G_{AN-1} = A
\end{aligned}
\tag{1-17}
$$

In the following step the logarithmic relationship between the input voltage and the output current will be proved.

Assume that the k_{th} stage is at the verge of limiting.

The input voltage is;

$$V_{in_k} = V_{in} = \frac{I_L}{G_{pk}} \tag{1-18}$$

It is also known from (1-16) that

$$G_{pk} = g_m A^{k-2}(A-1) \tag{1-19}$$

Substituting (1-19) into (1-18) gives

$$V_{in} = \frac{I_L}{g_m A^{k-2}(A-1)}; k \geq 2 \tag{1-20}$$

Since the k_{th} stage is at the verge of limiting, the output current consists of the limiting part and the amplified part.

$$I_{out} = (N-k)I_L + G_k V_{in} \tag{1-21}$$

Substituting (1-15) and (1-20) into (1-21) gives;

$$I_{out} = (N-k)I_L + \frac{AI_L}{A-1} \tag{1-22}$$

Some transformation on (1-19) gives the value of k.

$$V_{in} = \frac{I_L}{g_m A^{k-2}(A-1)} \Rightarrow A^k = \frac{I_L A^2}{g_m (A-1)V_{in}} \Rightarrow k = \log_A \left[\frac{A^2 I_L}{g_m (A-1)V_{in}} \right] \tag{1-23}$$

Finally substituting the value k into (1-21) gives;

$$I_{out} = I_L\left[N + \frac{A}{A-1} + \log_A \frac{g_m(A-1)V_{in}}{A^2 I_L}\right] \tag{1-24}$$

For different values of k, I_{out} values are calculated from (1-22) as;

$$\begin{aligned}
&k = N \Rightarrow I_o = I_L\left[\frac{A}{A-1}\right] = I_L\left[1 + \frac{1}{A-1}\right] \\
&k = N-1 \Rightarrow I_o = I_L\left[1 + \frac{A}{A-1}\right] = I_L\left[2 + \frac{1}{A-1}\right] \\
&\text{.....} \\
&k = 2 \Rightarrow I_o = I_L\left[N-1 + \frac{1}{A-1}\right]
\end{aligned} \tag{1-25}$$

It is obvious from (1-25) that there is a fixed value in the output current expression, and this corresponds to C in Figure 1-10.

$$C = \frac{I_L}{A-1} \tag{1-26}$$

$V_{\min}$ from Figure 1-10 is defined as;

$$V_{\min} = \frac{C}{G_N} = \frac{I_L}{(A-1)g_m A^{N-1}} \tag{1-27}$$

The output current is calculated from the last amplifier stage to the second amplifier stage in (1-25). The k=1 case, i.e. the case where the first amplifier is limited, is not examined. When the second gain path has reached its compression point, the input voltage is;

$$V_{in} = \frac{I_L}{G_{p2}} = \frac{I_L}{g_m(A-1)} \tag{1-28}$$

This point corresponds to the output current value of $(N-1)I_S + C$ in Figure 1-10. The current provided by the lowest gain path at this input voltage is;

$$I = G_{p1} V_{in} = g_m V_{in} = \frac{I_L}{A-1} = C \tag{1-29}$$

In order to reach the $NI_S + C$ output current in Figure 1-10; in other words, the first amplifier is saturated, the lowest gain path must supply another I_S current. So the output current supplied by the lowest gain path is;

$$I_{L1} = \frac{I_L}{A-1} + I_L = I_L \frac{A}{A-1} \tag{1-30}$$

With these parameters the dynamic range of the logarithmic amplifier is A^N.

1.2.1.3 Comparison of These Methods

- Series linear limit log amp:

  +Process variations affect each stage more or less equally
  +Solution of phase equalization
  -Because of loading: Limited BW

- Progressive-compression parallel-summation log amp:

  +High dynamic-range applications
  -Phase delay

- Parallel-amplification parallel-summation log amp:

  +Improved phase and group-delay matching
  -Low dynamic-range applications

1.2.2 Demodulating Logarithmic Amplifiers

When the envelope of the signal is of interest, the demodulating logarithmic amplifiers are used. The phase information is not preserved because of detection and phase delays. There are two kinds of demodulating logarithmic amplifiers:

- Detector logarithmic video amplifiers (DLVA)
- Successive detection logarithmic amplifiers (SDLA)

1.2.2.1 DLVA

RF signal is demodulated with a diode detector and converted to low frequency video signals, which is then amplified logarithmically [4]. The dynamic range of the DLVA depends on the detector diode (-45 to +15 dBm is Schottky diode detectors are used and -40 to +5 dBm for tunnel diode detectors). Since a single stage DLVA provides a limited input dynamic range, a parallel detection approach can be used to obtain an extended dynamic range as seen in Figure 1-11 [13][14].

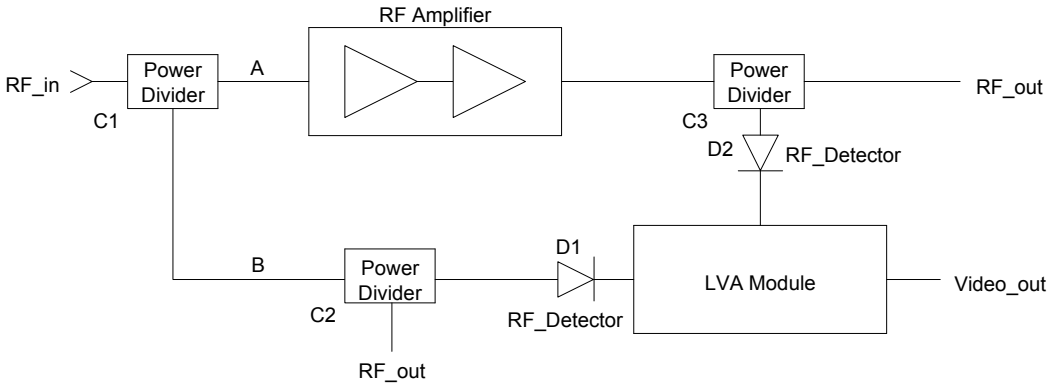

Figure 1-11: Block diagram of a wide dynamic range DLVA [13]

The RF signal feeds the power divider. The signal following path A is amplified and makes the low power signals detectable at the diode detector; in other words, this amplification increases the sensitivity of the DLVA. The signal following path B feeds the power divider and demodulated at the other diode detector. The low frequency video signals are logarithmically amplified at the LVA (logarithmic video amplifier) module after the conversion of the RF signals to low frequency video

signals by demodulating at the RF detectors and summed to give a logarithmic video output over the extended dynamic range [4][13].

DC drift and offset are the primary problems observed in this type of amplifiers [2].

1.2.2.2 SDLA

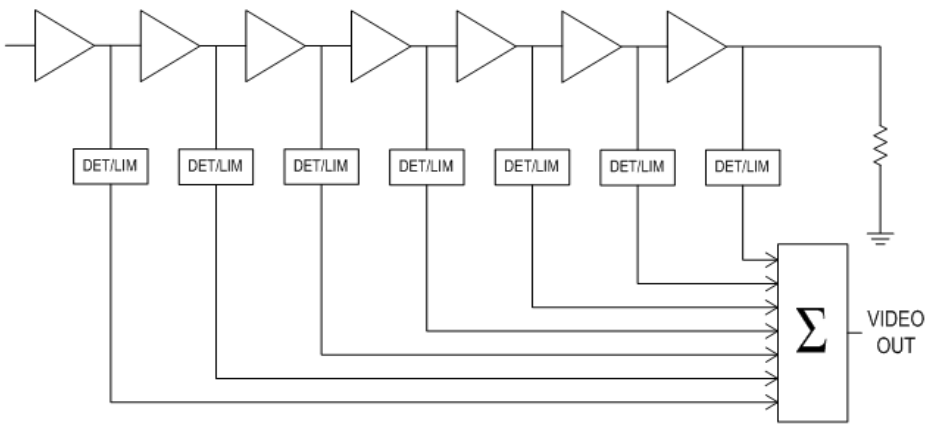

Figure 1-12: Block diagram of a successive detection logarithmic amplifier (SDLA) [15]

As seen from Figure 1-12 the SDLA topology shows a great similarity with the progressive compression parallel summation method. The signals amplified through the RF amplifiers are demodulated with detectors followed by limiters and the demodulated signals are summed to give a piecewise linear approximation of a logarithmic curve. The output is a video signal with amplitude proportional to the logarithm of the carrier amplitude [15].

Although detector logarithmic video amplifiers are widely used for EW systems requiring detection above 2 GHz, some limitations arise from the DLVA topology. The successive detection logarithmic amplifiers are the solutions to some of these limitations with an increased number of RF amplifiers and detector stages [16]. It is observed in the study [13] that SDLA shows superior pulse response and dynamic range performance compared to DLVA.

As in the progressive compression parallel summation method the input dynamic range of the logarithmic amplifier can be increased by increasing the number of the amplifier stages; however this poses a limitation on the bandwidth and the system stability will be deteriorated [12]. Smaller logarithmic error can be achieved by increasing the number of stages with less gain. In order to obtain an optimum SDLA, with small logarithmic error and high dynamic range, the RF amplifier stages, detectors and limiters must be identical and the logarithmic response must not change with temperature variations. These problems can be solved by monolithic integration [15].

CHAPTER 2

LOGARITHMIC STAGES (DIFFERENTIAL AMPLIFIERS)

From the articles examined it is obvious that the differential amplifier topology is the most widely used circuit architecture for logarithmic amplification. The gain, the limiting output voltage and the input voltage range for amplification can be adjusted according to the system requirements with this topology. The clipping type of the differential amplifier has a deterministic effect on the logarithmic error of the logarithmic amplifier. After the summation of the differential amplifier outputs a logarithmic response must be obtained with minimum deviation from the best fit line constructed with the logarithmic amplifier output response. The current mode limiting amplifiers result in hard clipping, whereas the voltage mode limiting amplifiers result in soft clipping, which is preferred to maintain smaller logarithmic error [17]. As seen in Figure 2-1 soft clipping results in smaller logarithmic error with respect to hard clipping.

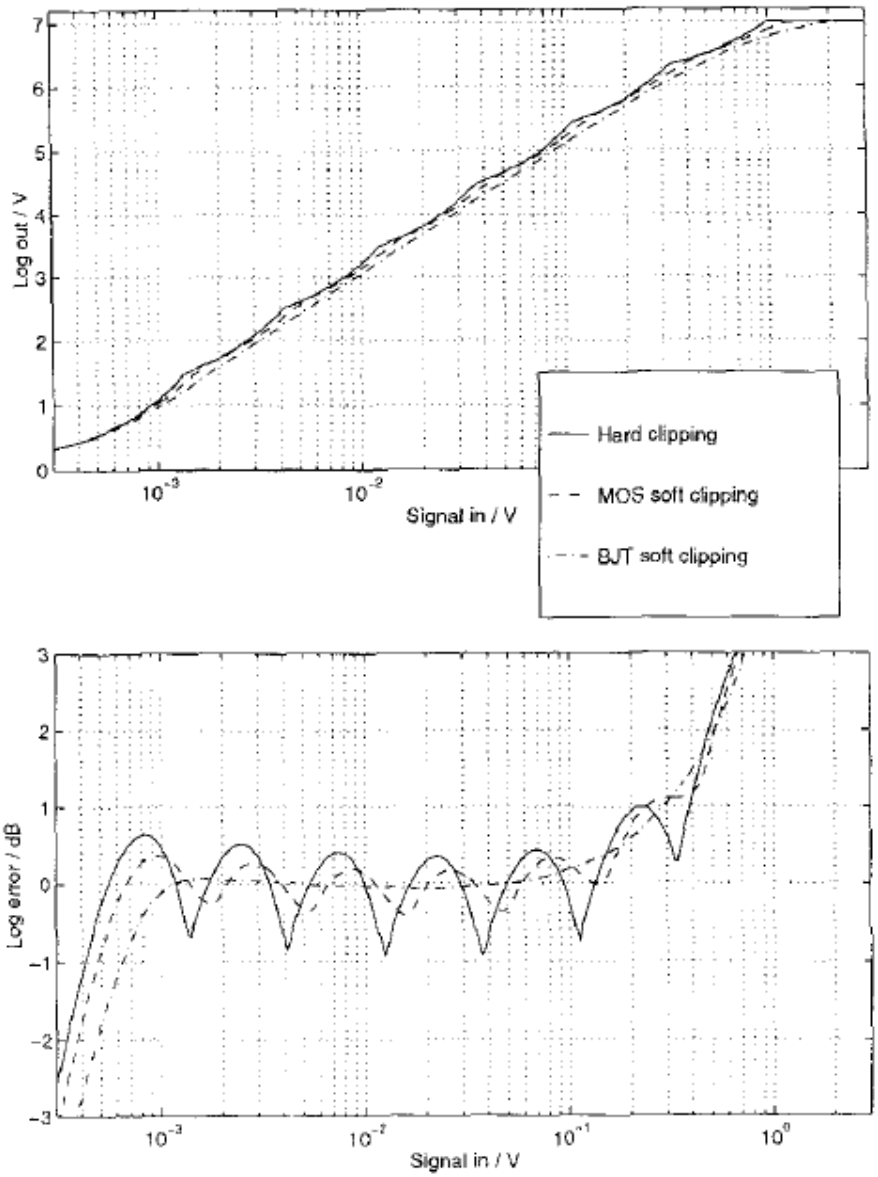

Figure 2-1: The accuracy of pseudologarithmic amplifiers with hard-clipping and MOS and BJT soft-clipping [17]

Figure 2-1 also shows that BJT soft clipping is superior to MOS soft clipping in logarithmic error. This stems from the BJT characteristics such as better device matching, exponential based nonlinear function, higher transconductance and output impedance for higher gain and lower distortion and lower 1/f noise when compared to MOS characteristics [4]. With the help of this knowledge BJT differential pairs are chosen for differential amplifier topology.

2.1 Theoretical Analysis of BJT Differential Pairs

In order to obtain brief information about input voltage-output voltage characteristics of BJT differential pairs a theoretical analysis is made for small signal and large signal operations with the corresponding mathematical models.

At the beginning it will be beneficial to start with the Ebers-Moll model of the npn transistor seen in Figure 2-2 which predicts the input-output characteristics in all of its possible operation regions.

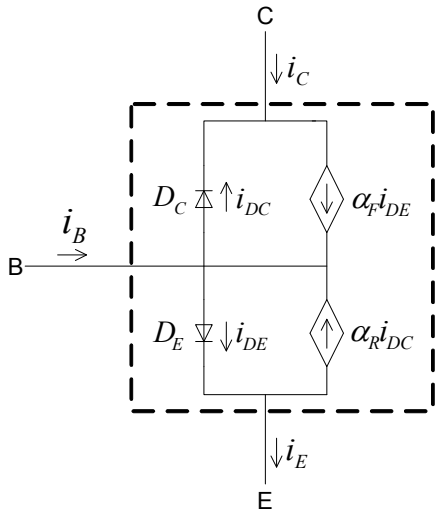

Figure 2-2: The Ebers-Moll model of the npn transistor [18]

The corresponding current expressions for the Ebers-Moll model of an npn transistor are summarized as follows according to Figure 2-2:

$$\begin{aligned} i_E &= i_{DE} - \alpha_R i_{DC} \\ i_C &= -i_{DC} + \alpha_F i_{DE} \\ i_B &= (1-\alpha_F) i_{DE} + (1-\alpha_R) i_{DC} \end{aligned} \tag{2-1}$$

The diode current expressions are used to maintain i_{DE} and i_{DC}.

$$i_{DE} = I_{SE}(e^{v_{BE}/V_T} - 1)$$
$$i_{DC} = I_{SC}(e^{v_{BC}/V_T} - 1) \qquad (2\text{-}2)$$

Letting $\alpha_F I_{SE} = \alpha_R I_{SC} = I_S$ and substituting (2-2) in (2-1) results in

$$i_E = \frac{I_S}{\alpha_F}(e^{v_{BE}/V_T} - 1) - I_S(e^{v_{BC}/V_T} - 1)$$
$$i_C = I_S(e^{v_{BE}/V_T} - 1) - \frac{I_S}{\alpha_R}(e^{v_{BC}/V_T} - 1) \qquad (2\text{-}3)$$
$$i_B = \frac{I_S}{\beta_F}(e^{v_{BE}/V_T} - 1) + \frac{I_S}{\beta_R}(e^{v_{BC}/V_T} - 1)$$

where $\beta_F = \frac{\alpha_F}{1-\alpha_F} and \beta_R = \frac{\alpha_R}{1-\alpha_R}$

Assume v_{BE} is positive and v_{BC} is negative. So;

$$i_E \cong \frac{I_S}{\alpha_F} e^{v_{BE}/V_T} + I_S(1 - \frac{1}{\alpha_F})$$
$$i_C \cong I_S e^{v_{BE}/V_T} + I_S(\frac{1}{\alpha_R} - 1) \qquad (2\text{-}4)$$
$$i_B = \frac{I_S}{\beta_F} e^{v_{BE}/V_T} - I_S(\frac{1}{\beta_F} + \frac{1}{\beta_R})$$

Since v_{BE} is positive and $\begin{matrix}\alpha_F \cong 1\\ \alpha_R \cong 1\end{matrix}$ and $\begin{matrix}\beta_F >> 1\\ \beta_R >> 1\end{matrix}$, the second terms of the right hand side of the expressions in (2-4) will be negligible with respect to the first terms. So, the expressions in (2-4) are transformed to (2-5).

$$\begin{matrix} i_E \cong \frac{I_S}{\alpha_F} e^{v_{BE}/V_T} \\ i_C \cong I_S e^{v_{BE}/V_T} \\ i_B = \frac{I_S}{\beta_F} e^{v_{BE}/V_T} \end{matrix} \quad \Rightarrow \quad \begin{matrix} i_E \cong (\beta_F + 1) i_B \\ i_C \cong \beta_F i_B \end{matrix} \qquad (2\text{-}5)$$

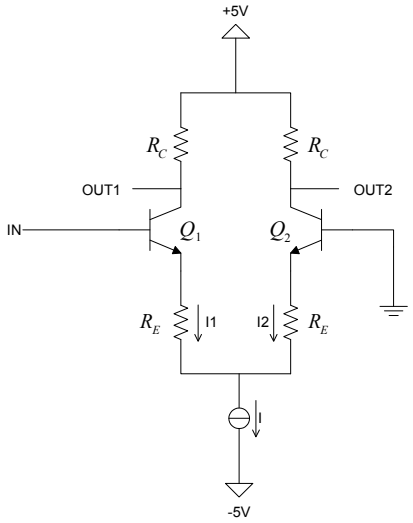

Figure 2-3: BJT differential amplifier

The BJT differential pair given in Figure 2-3 is examined through small signal analysis and large signal analysis.

Small signal analysis:

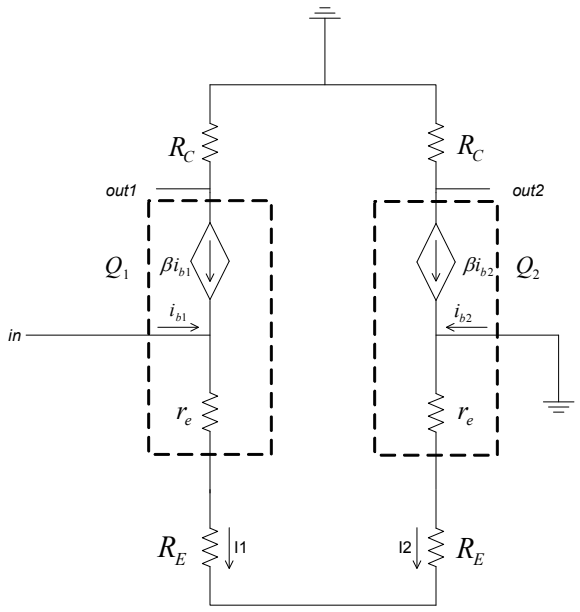

Figure 2-4: BJT differential amplifier small-signal analysis

The input and output voltages given in Figure 2-4 are calculated as:

$$\begin{aligned} v_{in} &= (\beta+1)(r_e + R_E)i_{b1} - (\beta+1)(r_e + R_E)i_{b2} \\ v_{out} &= v_{out1} - v_{out2} = -\beta R_C i_{b1} - (-\beta R_C i_{b2}) \end{aligned} \tag{2-6}$$

It is obvious from Figure 2-4 that $i_{b1} = -i_{b2}$. v_{in} and v_{out} are expressed in terms of i_{b1} by rearranging the expressions in (2-6).

$$\begin{aligned} v_{in} &= 2(\beta+1)(r_e + R_E)i_{b1} \\ v_{out} &= -2\beta R_C i_{b1} \end{aligned} \tag{2-7}$$

Using the expresions in (2-7) the small-signal gain of the differential amplifier is;

$$Gain = \frac{v_{out}}{v_{in}} = \frac{-2\beta R_C i_{b1}}{2(\beta+1)(r_e + R_E)i_{b1}} = -\frac{\beta R_C}{(\beta+1)(r_e + R_E)} \cong -\frac{R_C}{(r_e + R_E)} \tag{2-8}$$

where $r_e = \frac{V_T}{I_E} = \frac{V_T}{I/2} = \frac{2V_T}{I}$

Large signal analysis:

BJT differential amplifier topology examined for large-signal analysis is seen in Figure 2-5.

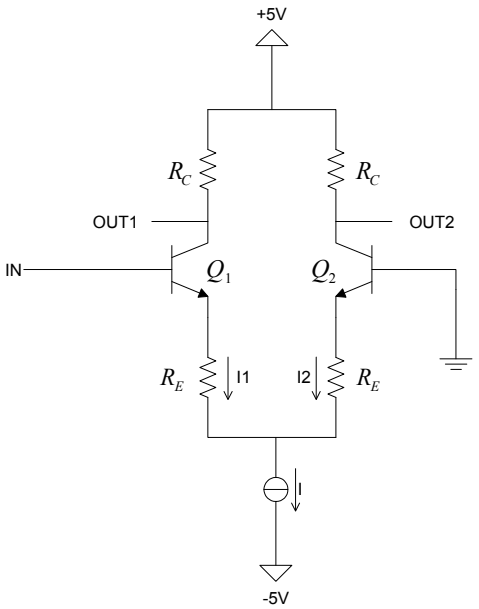

Figure 2-5: BJT differential amplifier large-signal analysis

- Assume +1V is applied to the input port.

$$Since I_1 > I_2; V_{IN} - 0.7 - I_1 R_E + I_2 R_E = 0.3 - R_E(I_1 - I_2) < 0.3V < 0.7V$$

So; $Q_1 : ACTIVE$, $Q_2 : OFF$

$$V_{OUT} = (+5V - IR_C) - (+5V) = -IR_C \quad (2\text{-}9)$$

- Assume -1V is applied to the input port.

$$Since I_1 < I_2;$$
$$0 - 0.7 - I_2 R_E + I_1 R_E - V_{IN} = -0.7 + R_E(I_1 - I_2) + 1 < 0.3V + R_E(I_1 - I_2) < 0.7V$$

So; $Q_1 : OFF$, $Q_2 : ACTIVE$

$$V_{OUT} = (+5V) - (+5V - IR_C) = IR_C \quad (2\text{-}10)$$

2.2 Simulations

After the theoretical analysis of the BJT differential amplifiers the circuit topologies are simulated in order to verify the critical points in the input voltage-output voltage characteristics. The circuits are simulated with LTspice/SwitcherCad III [19].

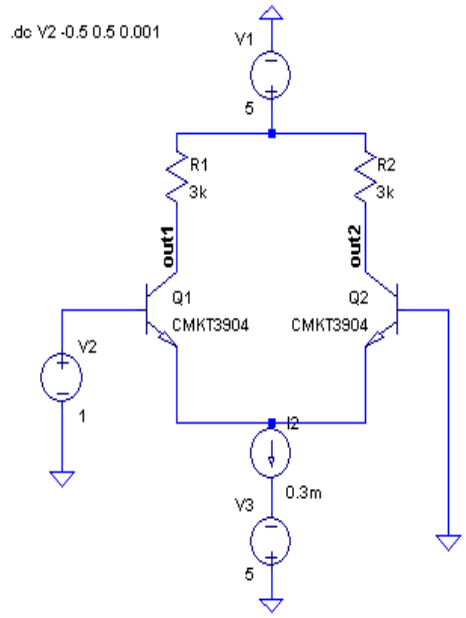

Figure 2-6: Differential amplifier topology

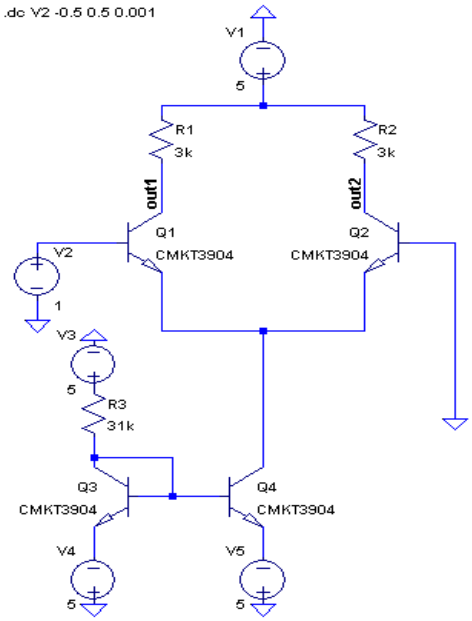

Figure 2-8: Differential amplifier implemented with current mirror as a current source

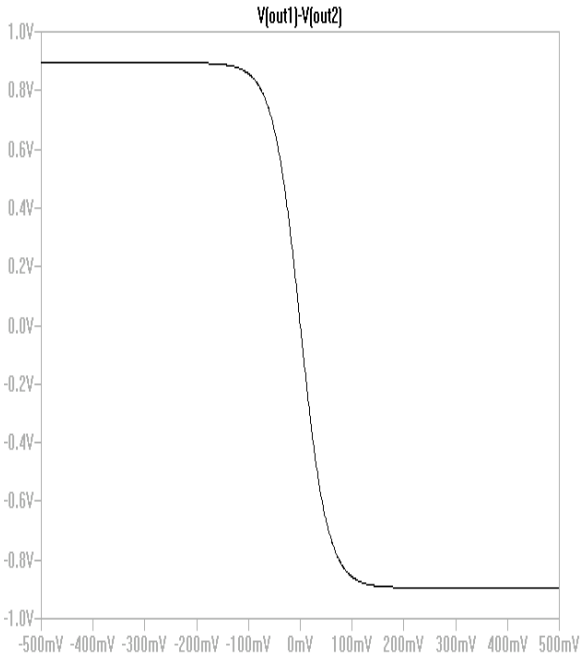

Figure 2-7: Differential amplifier characteristics

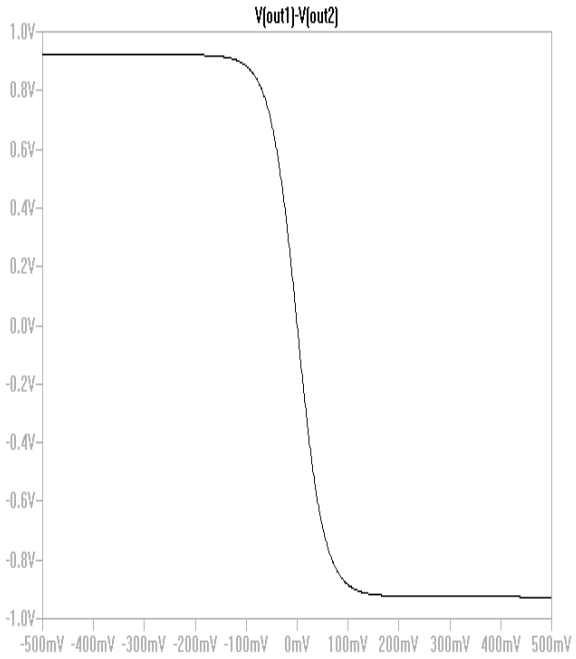

Figure 2-9: Differential amplifier characteristics

When Figure 2-7 and Figure 2-9 are compared, it is obvious that the current mirror can be used as a current source without disturbing the differential amplifier characteristics. The current supplied by the current mirror can be adjusted by changing the value of the resistor R_3 in Figure 2-8. The current supplied by the current mirror is;

$$I = (\frac{+5V - V_d - (-5V)}{R_3}) = \frac{(10 - 0.7)V}{31k\Omega} = 0.3mA$$

which is the same as the supplied current from the current source in Figure 2-6 and the input-output characteristics in Figure 2-7 and Figure 2-9 are identical as expected. The current mirror will be used for current supply.

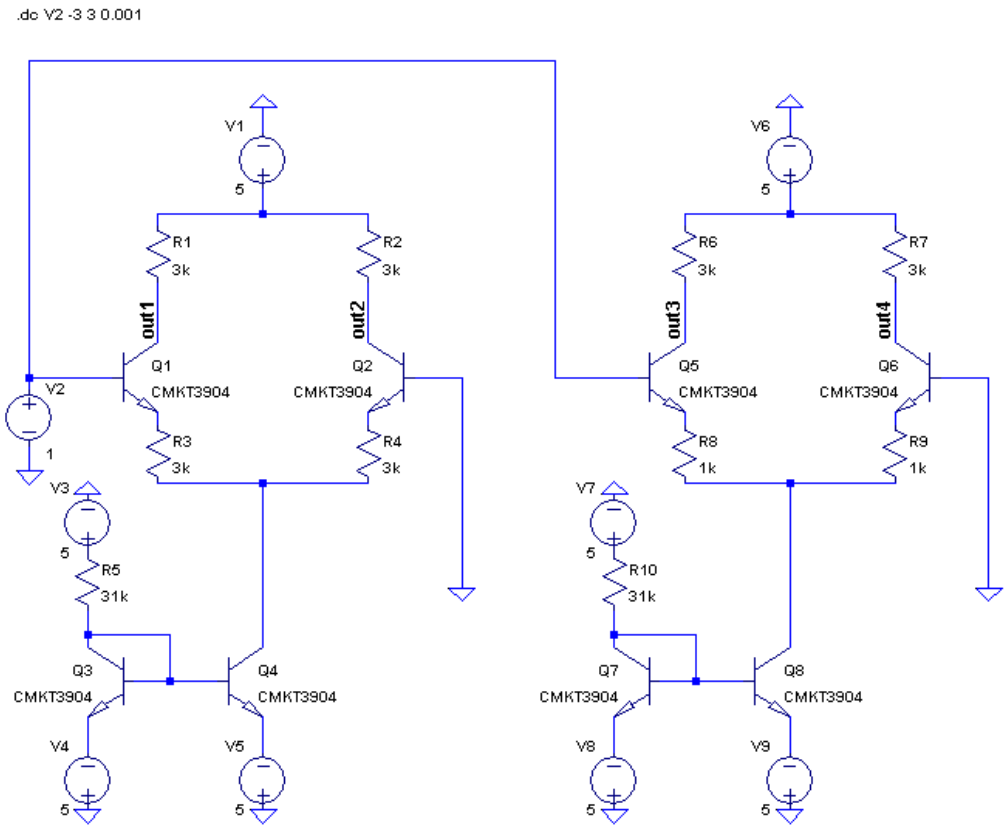

Figure 2-10: Examination of the effect of the emitter resistor R_E

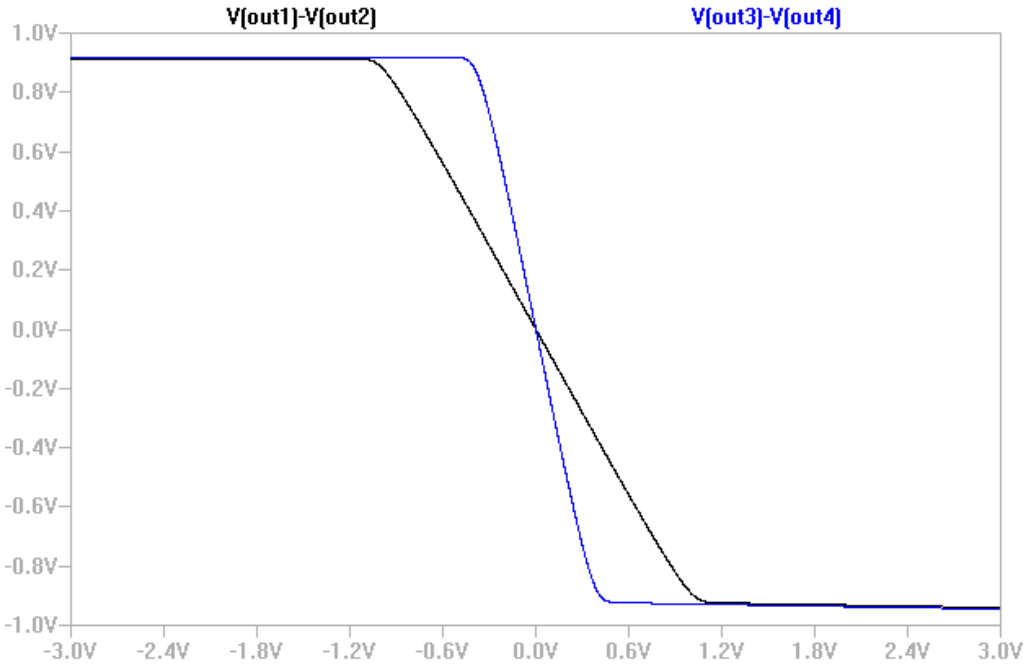

Figure 2-11: Comparison of the outputs of the differential amplifiers

In order to obtain adjustable gain when R_C is kept constant, different R_E values must be used as observed in (2-8) where r_e is negligible. Since the limiting output voltages are independent of the resistor R_E changing the gain also means varying the span of the linear region as seen in Figure 2-11.

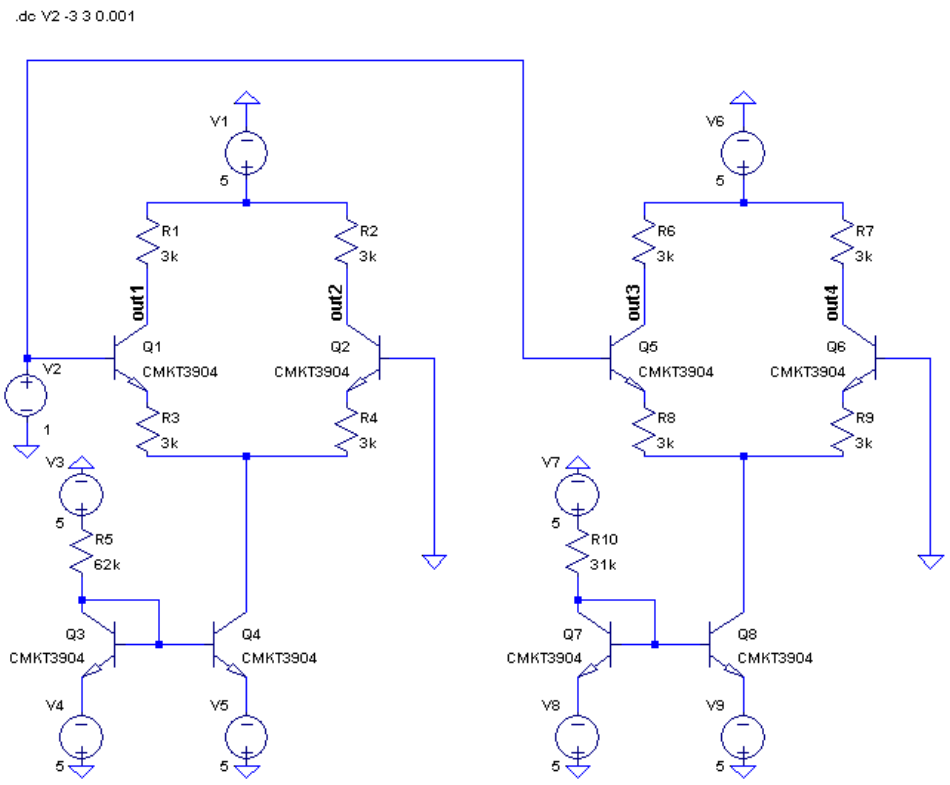

Figure 2-12: Examination of the effect of the current source

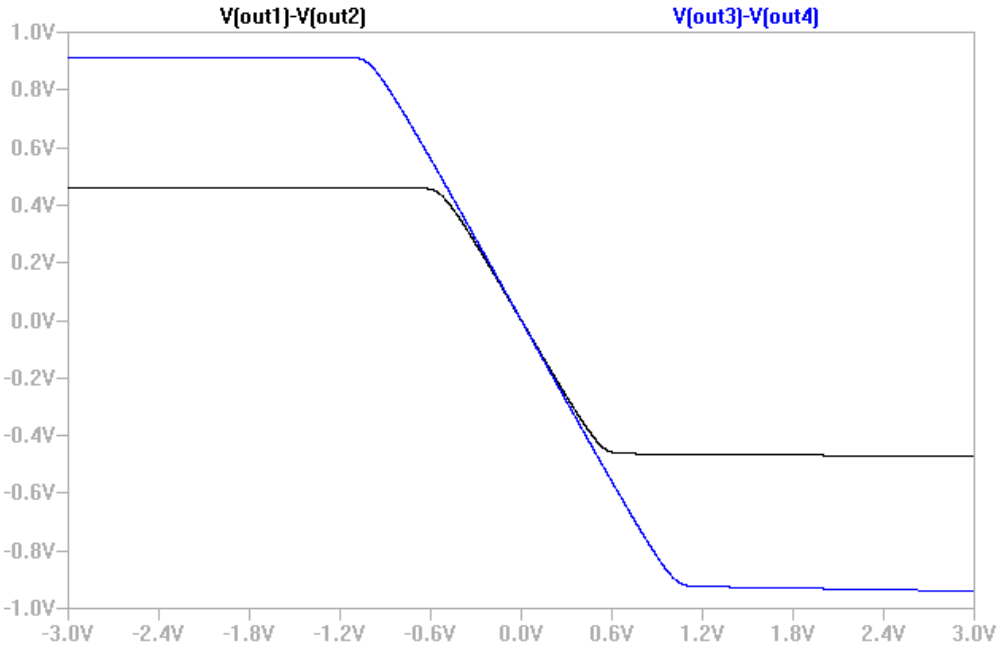

Figure 2-13: Comparison of the outputs of the differential amplifiers

As predicted from (2-9) and (2-10) the resistor in the current mirror has a direct effect on determining the limiting value of the output voltage as seen in Figure 2-13. Since the gain is independent of the resistor in current mirror as obtained in (2-8), it is the same for both circuits.

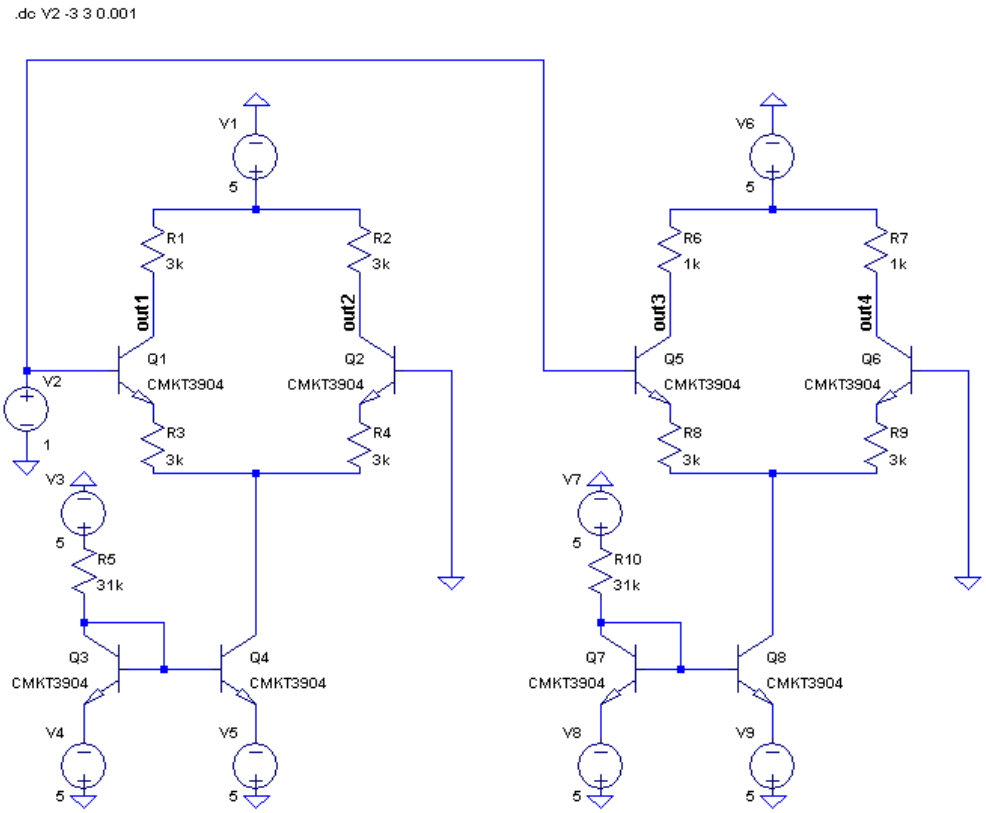

Figure 2-14: Examination of the effect of the collector current

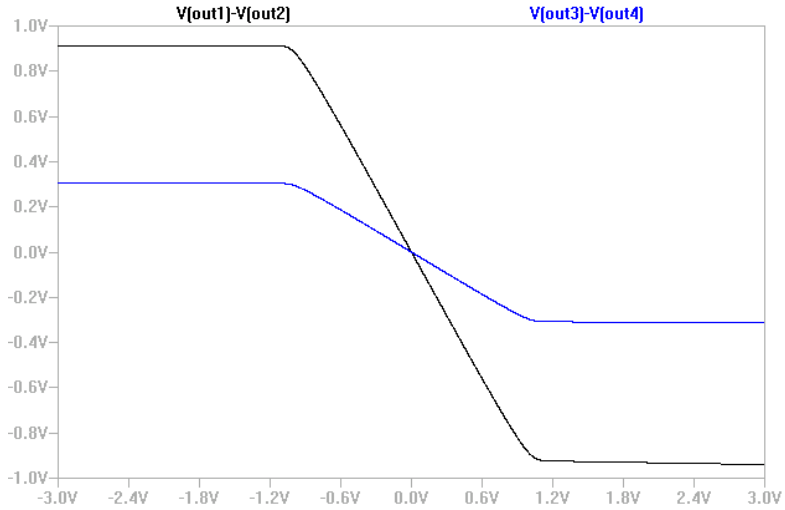

Figure 2-15: Comparison of the outputs of the differential amplifiers

As seen in Figure 2-15 the limiting voltage value and the gain of the differential amplifiers are directly proportional to the collector resistor R_C as predicted from (2-8), (2-9) and (2-10).

Having seen the effect of different circuit components on the differential amplifier characteristics the circuit topology for the parallel-amplification parallel-summation method must be determined.

The most basic circuit topology is examined first as seen in Figure 2-16, the buffers are used to prevent loading and the operational amplifiers are used to obtain the signal resulting from the input signal only. According to the mathematical analysis of the parallel amplification method the circuit components are calculated to obtain the corresponding logarithmic stage characteristics, such as gain and limiting voltage value.

For instance, design a three stage logarithmic amplifier. Choose $R_C = 1.8k\Omega$, $g_m = 0.5$ and $A = 4$. It is known from the mathematical analysis that $I_{L1} = I_L \dfrac{A}{A-1}$ which determines the relation between the currents supplied by the current mirrors.

Let the resistor in the second and third current mirror be $45k\Omega$, so the current supplied by the second and third stage current mirrors is $207\mu A$ which results in $r_e = 242\Omega$, so the current supplied by the first stage must be $275\mu A$ which results in $r_e = 182\Omega$ and this is satisfied when the resistor in the first current mirror is $33{,}8k\Omega$. Then, the corresponding gain of each stage is

$G_1 = g_m = 0.5$

$G_2 = g_m(A-1) = 1.5$

$G_3 = g_m A(A-1) = 6$

The circuit components are calculated according to the gain expression in (2-8) as;

$$G_1 \cong -\frac{R_C}{(r_e + R_E)} = -\frac{1.8k\Omega}{(182\Omega + R_E)} = 0.5 \Rightarrow R_E = 3.42k\Omega$$

$$G_2 \cong -\frac{R_C}{(r_e + R_E)} = -\frac{1.8k\Omega}{(242\Omega + R_E)} = 1.5 \Rightarrow R_E = 0.96k\Omega$$

$$G_3 \cong -\frac{R_C}{(r_e + R_E)} = -\frac{1.8k\Omega}{(242\Omega + R_E)} = 6 \Rightarrow R_E = 58\Omega$$

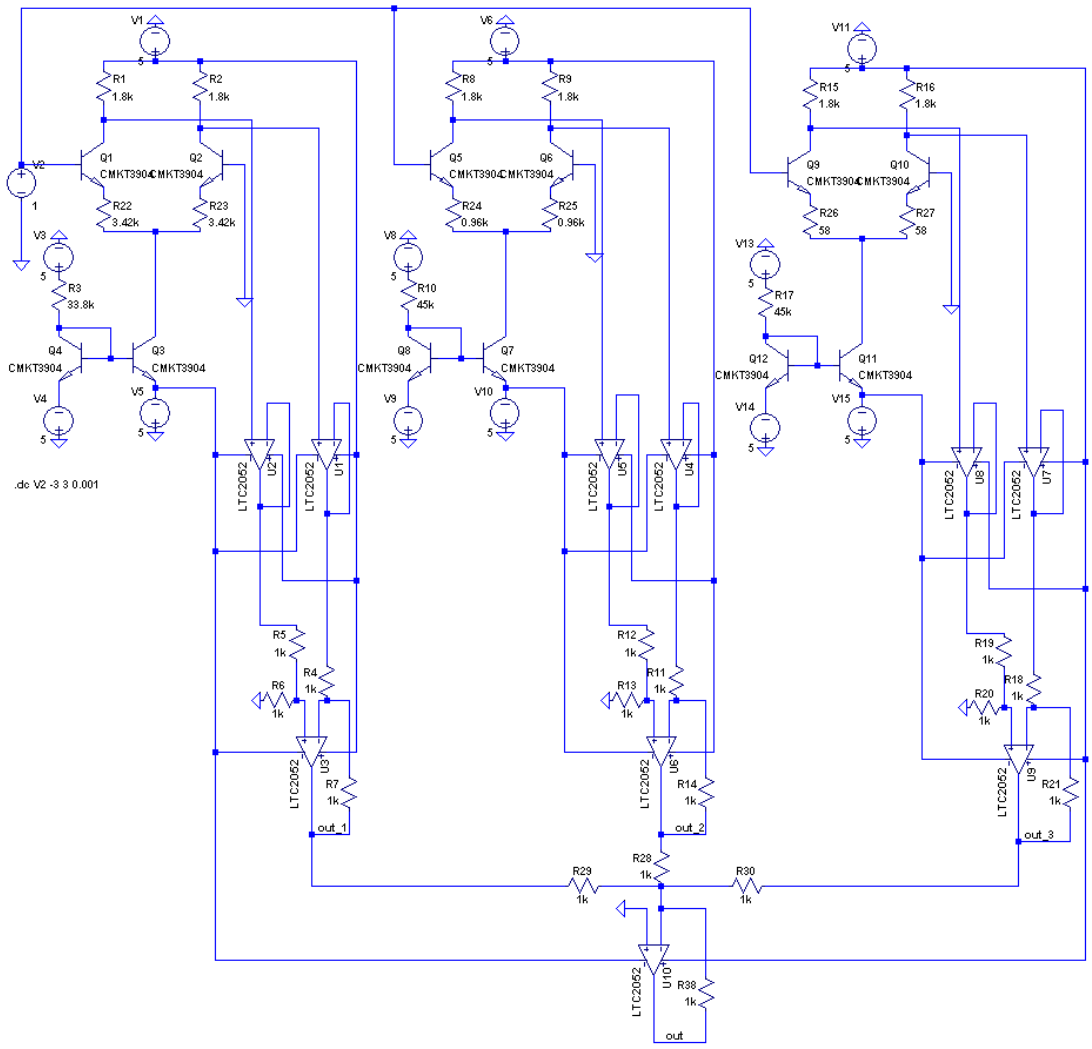

Figure 2-16: Parallel-amplification parallel-summation logarithmic amplifier topology

The simulation results are submitted in linear scale in Figure 2-17 and in logarithmic scale in Figure 2-18.

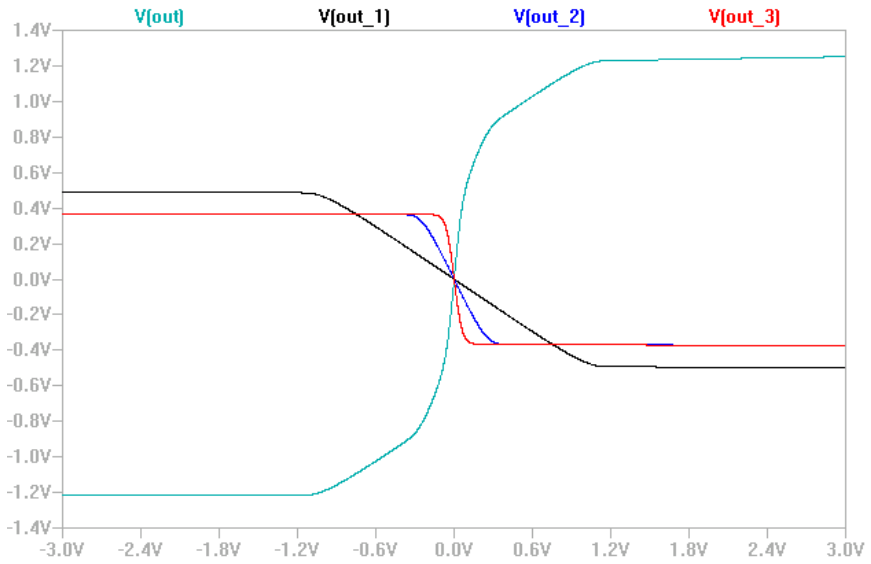

Figure 2-17: Individual characteristics of each gain stage and the overall output characteristics in linear scale

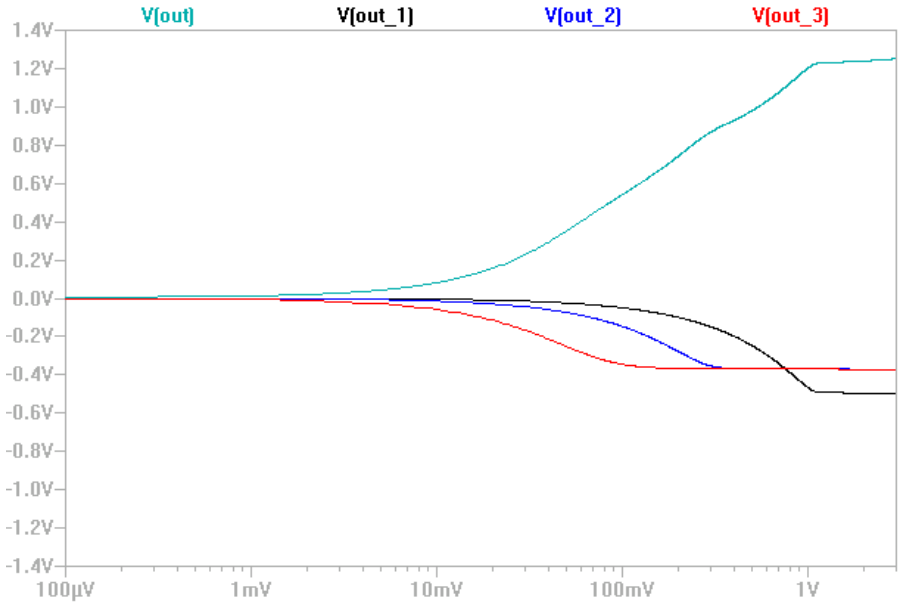

Figure 2-18: Individual characteristics of each gain stage and the overall output characteristics in logarithmic scale

In order to decrease the quantity of the circuit components seen in Figure 2-16 and to simplify the design other possible circuit topologies are examined and compared with this logarithmic response. For instance, the buffers are removed first as observed in Figure 2-19.

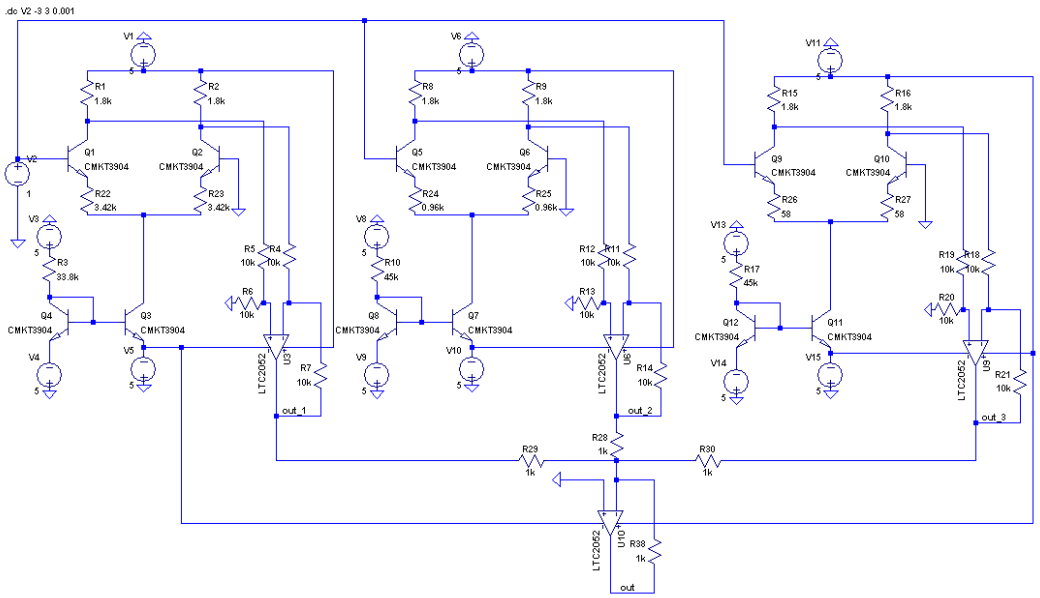

Figure 2-19: Parallel-amplification parallel summation logarithmic amplifier topology without buffers

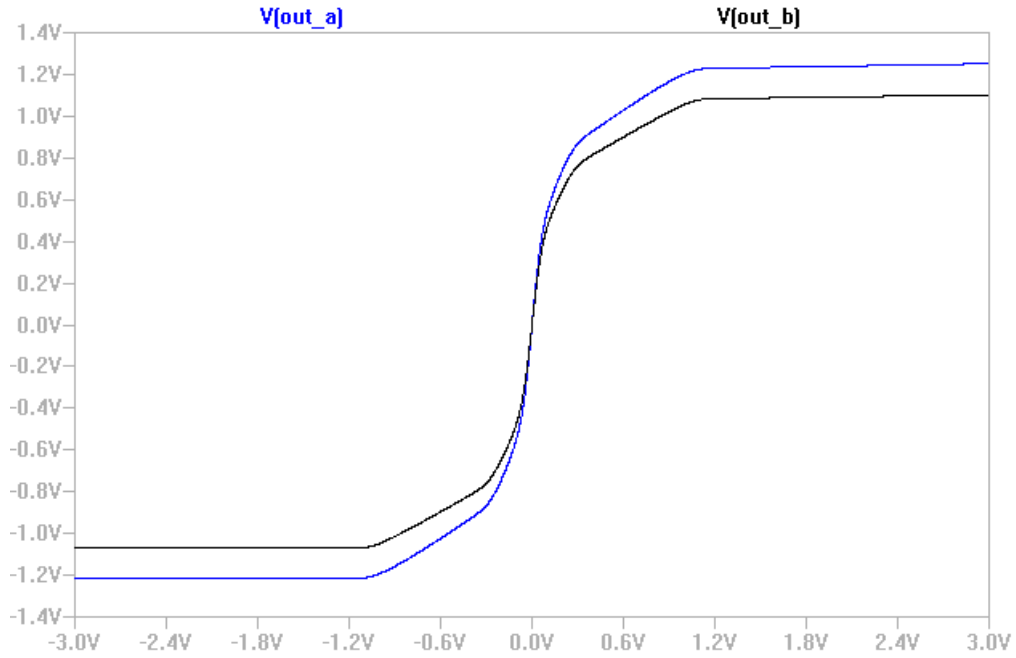

Figure 2-20: Comparison of the output characteristics; out_a: the output of the circuit in Figure 2-16, out_b: the output of the circuit in Figure 2-19

It is known that buffers have high input impedance. The resistors in the op-amp stages after the buffers are changed from 1kΩ to 10 kΩ. The comparison of the circuits given in Figure 2-16 and Figure 2-19 is given in Figure 2-20. It is obvious that there are slight differences in the limiting voltage and the gain of each individual gain stage which can be compensated by changing the circuit components correspondingly. A much closer response can be obtained with impedance greater than 10 kΩ. So, it is determined not to use buffers and a simpler circuit schematic is obtained.

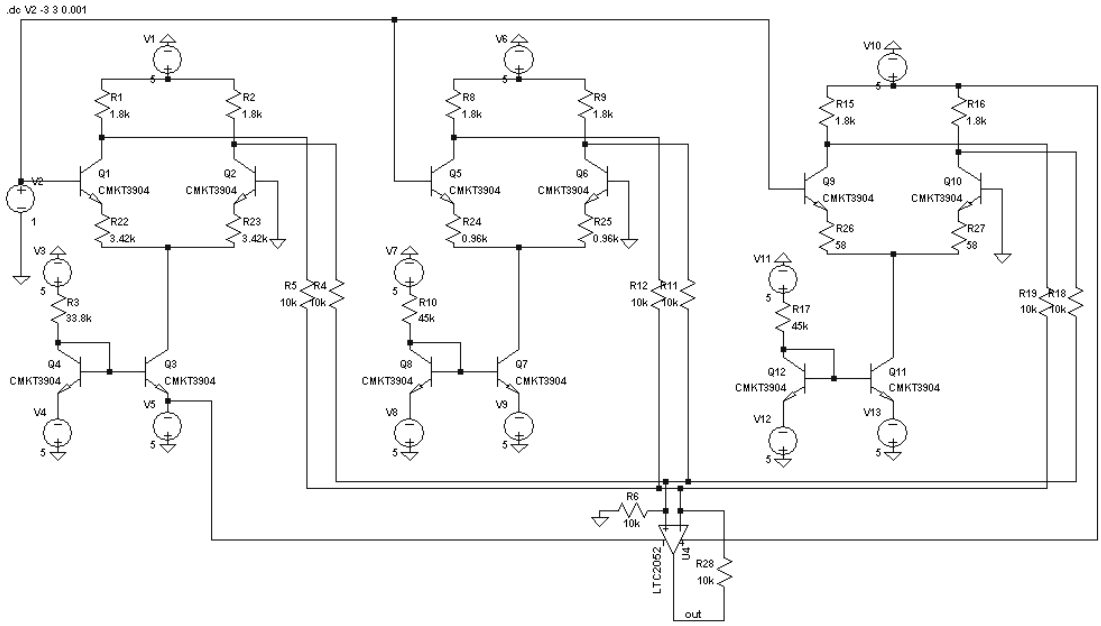

Figure 2-21: Parallel-amplification parallel summation logarithmic amplifier topology with and without differential op-amps

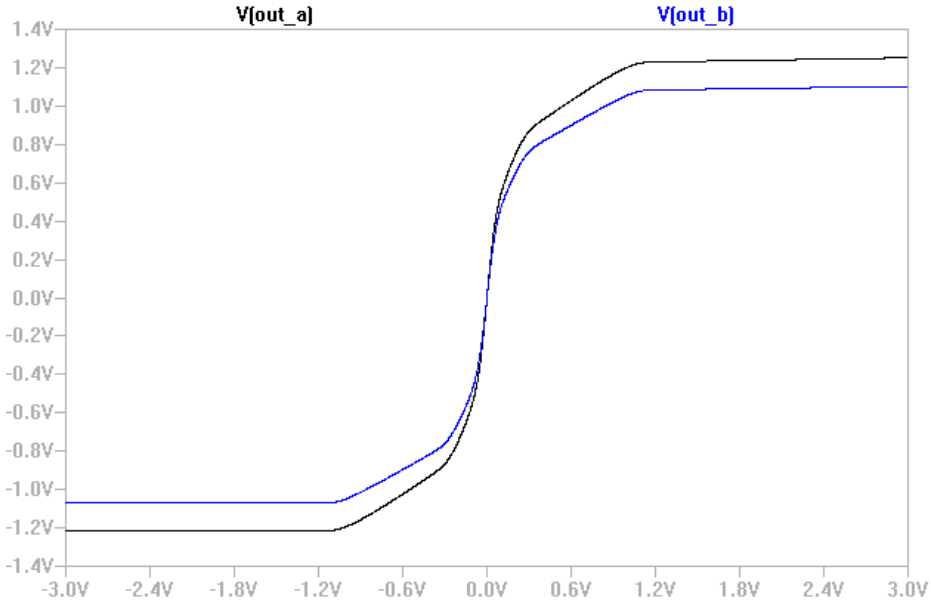

Figure 2-22: Comparison of the output characteristics; out_a: the output of the circuit in Figure 2-16, out_b: the output of the circuit in Figure 2-21

In order to make the circuit simpler than Figure 2-19 the differential op-amps are discarded at this time as seen in Figure 2-21. Differential output is obtained with the differential op-amp in the summing stage at the end. As seen in Figure 2-22 there is a difference in the output characteristics similar to the comparison in Figure 2-20. The variation can be compensated by modifying the circuit components.

2.3 Conclusion

A comparison between different circuit topologies is made and the simplest design is determined; the parallel-amplification parallel-summation topology without buffers and differential op-amps will be used. The chosen parameter values, such as gain and the limiting voltages of the logarithmic stages, are consistent with each other. The number of the gain stages can be adjusted to obtain the desired logarithmic response. As seen from Figure 2-22 the logarithmic responses have a slight difference which can be compensated by proper emitter, collector and current mirror resistors and sufficient number of gain stages.

CHAPTER 3

INTRODUCTION TO SCHOTTKY DIODE DETECTORS

The Schottky barrier diode is a semiconductor diode with low forward voltage and no flow of minority carriers. The diode junction is formed by the contact of a pure metal with a semiconductor doped with n-type or p-type atoms. The electrons in the semiconductor diffuse through the junction into the metal making the semiconductor more positive relative to the metal. The flow of electrons ceases when the internal voltage difference between the two regions is too high that prevents more electrons from diffusing. The internal voltage difference is typically 0.3-0.8 V for Schottky diodes. However, the internal voltage difference can be reduced with the help of an external voltage with correct polarity; in the same way, the internal voltage can be increased with the help of an external voltage with opposite polarity; in other words, the internal voltage can be determined by design according to the design requirements. No flow of minority carriers is another specific property of Schottky diodes which makes them possible to be used in switching applications where fast responses are needed [20].

3.1 Comparison of Schottky Diode with Other Diodes

Since the diode has a deterministic role in the video detector performance the diode must be chosen properly for maximum dynamic range; at the same time, the detector must be insensitive to temperature variations.

3.1.1 Comparison of Schottky Diode with pn Junction Diode

The significant difference results from the adjustable internal voltage and no flow of minority carriers.

The internal voltage is a design parameter for a Schottky diode and can be adjusted according to the design requirements whereas it is fixed for a pn junction diode. This property is useful in power detectors to increase sensitivity. The internal voltage difference of a Schottky diode is typically 0.3-0.8 V which is lower than the pn junction diode internal voltage.

Another specific property of the Schottky diodes is that there is no flow of minority carriers from the metal into the semiconductor. Unlike junction diodes there is no charge storage which makes them possible to be used in fast switching requirements [20].

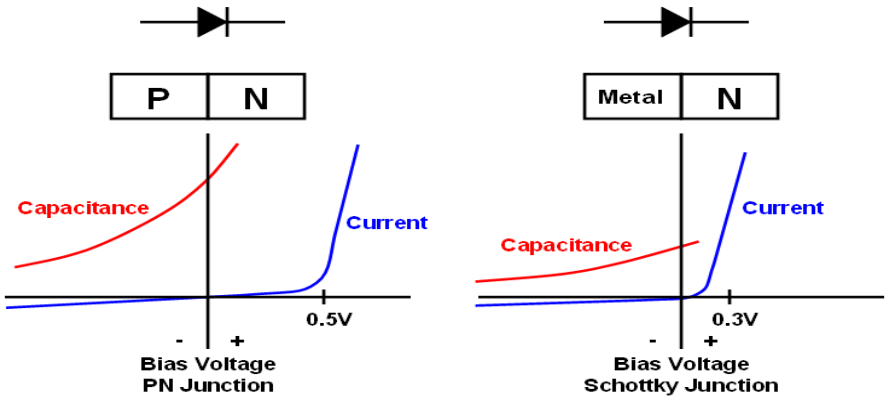

Figure 3-1: IV curve and capacitance comparison [21]

Figure 3-1 shows the IV curve and capacitance comparison of the pn junction diodes and the Schottky diodes. The junction capacitance is larger for the pn junction diode which may result in problems at high frequencies.

3.1.2 Comparison of Schottky Diode with Tunnel Diode [22]

The tunnel diodes are widely used in detector applications. One of the reasons is that they require no bias current to increase sensitivity. The corresponding output voltage of the signals with low power can also be revealed because of the zero offset output voltage and this increases the dynamic range. Temperature stability is another property of the tunnel diode detector. The tunnel diode detectors have some limitations beside these advantages. The useful input dynamic range is narrower, the maximum input power that does not damage the tunnel diode is lower than the Schottky diode counterpart and the operating temperature is lower with respect to the Schottky diode detectors.

These limitations are overcome with the Schottky diode detectors. The dynamic range is almost 20dB wider than the tunnel diode detectors and an input power level of +20dBm do not damage the detector. The Schottky diode detectors can be operated in a wider range of temperature and the pulse response is superior to the tunnel diode detectors.

However, a bias current must be used to increase the sensitivity of the Schottky diode detector. The signal originating from the bias current must be eliminated from the output voltage to obtain the detected signal accurately since the bias current creates an offset preventing the detection of the signals with low power. A Schottky diode pair biased with the same currents is used for this purpose. Taking the difference of the output of the two detectors with an operational amplifier reveals the detected output voltage. The temperature variations are also eliminated by this way since each diode will be affected in the same manner [22].

3.2 Detector Circuits

The Schottky diode detectors rectify the incoming RF signal and produce a low frequency voltage with amplitude proportional to the magnitude of the RF signal power.

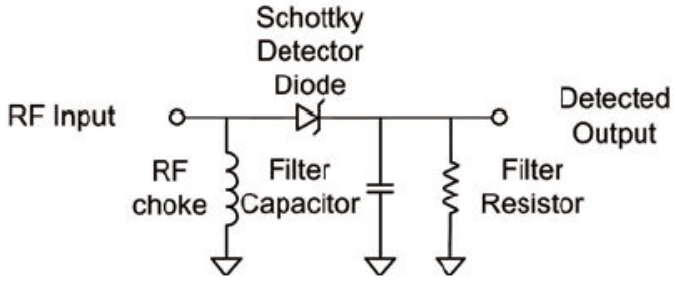

Figure 3-2: The simplest RF detector circuit [20]

The simplest RF detector circuit is given in Figure 3-2. The output filter's capacitor is charged to the low frequency voltage.

The detector characteristics showing the relationship between the input power and the output voltage consists of two detection regions: the square law detection region and the linear detection region. As an example, the input power-output voltage characteristics are given in Figure 3-3 for the specified diodes at the given test conditions.

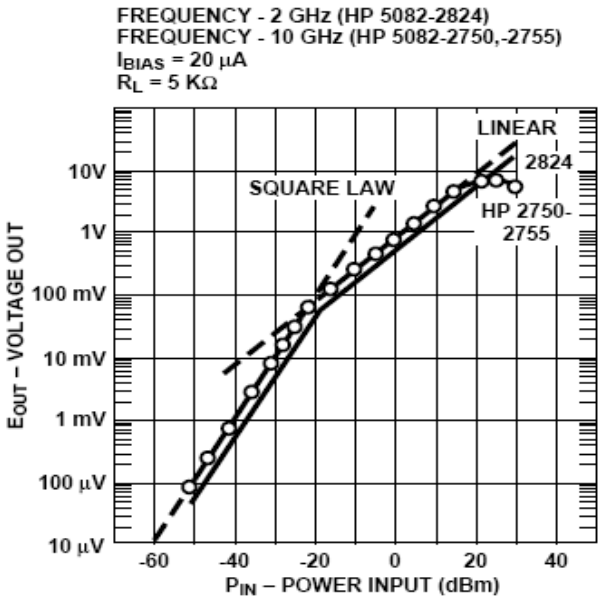

Figure 3-3: Schottky diode detector dynamic characteristics showing square law and linear detection regions for the given diodes at the specified conditions [23]

There is an abrupt change in the slope of the detector characteristics. The barrier height has a deterministic effect on the RF signal power level where the transition from the square law detection region to the linear detection region.

In order to make a Schottky diode detector more sensitive to small RF signals the barrier height must be reduced. Applying an external positive voltage (positive terminal to the anode, negative terminal to the cathode) increases the sensitivity of the diode detector by reducing the barrier height.

3.2.1 Features of Schottky Barrier Diode Video Detectors [23]

A typical video receiver is shown in Figure 3-4.

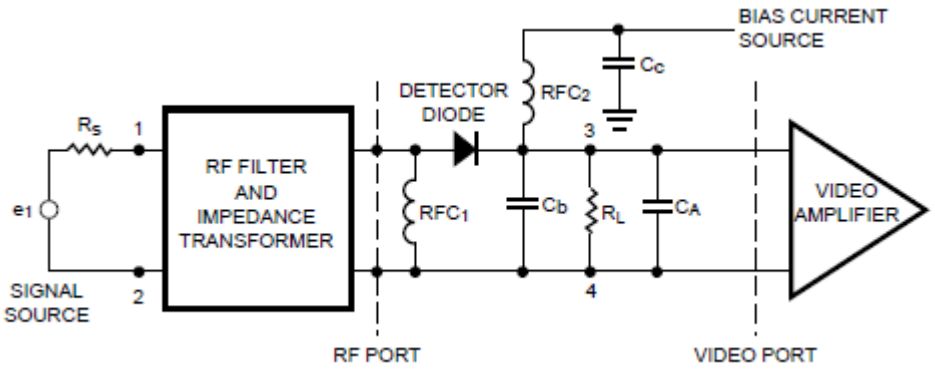

Figure 3-4: Typical video receiver [23]

The circuit operation is examined for RF signals and for low frequency signals.
At RF since the input impedance of the diode detector is not matched to the signal source, an impedance matching network is required in order to deliver all the available power to the detector diode. The RF choke, RFC_1, acts as an open circuit and the capacitor c_b appears as a short circuit in order to maximize the current

passing through the diode and the demodulated video signal appears across the load resistance R_L.

At video frequencies the bias circuit is active; the RF chokes, RFC1 and RFC2, act as short circuits constituting the bias path of the diode to the ground. The capacitors c_b and c_c, appears as open circuits.

In the RF detector design the main aim is to obtain maximum signal sensitivity at a sufficient video bandwidth broad enough to recover RF pulses properly. However, a compromise must be made between the RF signal sensitivity and the video bandwidth. The video bandwidth must be not greater than required in order to obtain maximum sensitivity [23].

3.2.1.1 Diode Performance Characteristics [23]

The tangential signal sensitivity, video resistance and the voltage sensitivity are the parameters that effect diode performance characteristics.

Tangential signal sensitivity (TSS)

The tangential signal sensitivity is the minimum power level of a signal that can be detected in a specified signal to noise ratio at the output of the video detector. TSS depends on

- RF frequency
- Video bandwidth
- Diode DC bias current
- Test mount or circuit
- Video amplifier noise figure

The upper and lower 3dB frequencies of the entire circuit should be stated with the diode's video resistance while specifying the video bandwidth. Since the upper 3dB frequency is much larger than the lower 3dB frequency the bandwidth can be stated with the upper 3dB frequency only, which can cause a misunderstanding; this gives

an impression of the bandwidth extending down to DC. However, the flicker noise deteriorating the TSS is effective at low frequencies.

In order to increase the sensitivity of the diode detector a forward DC bias current can be used. This increases the shot and the flicker noise and reduces the video resistance of the diode resulting in a worse TSS.

The package parameters are also effective on TSS. In order to obtain the repeatability of the measurements the package parameters must be well controlled.

Video resistance

The video resistance is the small signal low frequency dynamic resistance of the diode. The DC bias current used for increasing the sensitivity of the diode detector reduces the video resistance of the diode.

Voltage sensitivity

Voltage sensitivity is the slope of the input power-output video voltage characteristics of the diode detector. It depends on the DC bias current, load resistance, signal level and RF frequency. The slope of the input power-output voltage characteristics changes at the transition from the square law detection range to the linear detection range. The voltage sensitivity is defined for the square law detection range.

3.2.1.2 Optimum Video Detector Sensitivity

Assuming a diode ideality factor of $n = 1.08$ and at room temperature, the TSS of a video receiver can be stated as [24]

$$TSS_{(dBm)} = -107 + 5\log B_V + 10\log I_d + 5\log\left[R_A + \frac{28}{I_d}\left(1 + \frac{f_N}{B_V}\ln\frac{B_V}{f_L}\right)\right] + 10\log\left[1 + \frac{R_S c^2{}_{j(i)} f^2}{I_d}\right] \quad (3\text{-}1)$$

where

B_V = Video bandwidth in Hz

I_d = Diode DC bias in μA

f_N = Diode flicker noise corner frequency, Hz

f_L = Video circuit low frequency 3 dB point, Hz

R_S = Diode series resistance, Ω

$c_{j(i)}$ = Diode junction capacitance, pF, at the bias current I_d

It is obvious from (3-1) that the diode parameters affecting the diode detector sensitivity are f_N, R_S and $c_{j(i)}$. The diode DC bias current can be chosen to obtain maximum sensitivity for a given diode at a specified frequency [23].

3.2.1.3 Bandwidth Requirements

Video bandwidth has a deterministic affect on the recovery of the modulated signal, a diode detector with a video bandwidth smaller than required causes a distorted signal to be observed at the output of the video detector; in other words, the information may be wrong. Since a compromise must be made between the video bandwidth and RF signal sensitivity, the video bandwidth must be not greater than required at the same time [23].

3.2.1.4 Dynamic Range

As seen from Figure 3-3 the input power vs. the video output voltage characteristic is composed of two regions as the square law detection region and the linear region detection region. The dynamic range of a video detector is defined as the square law region where the relationship between the input power and the output video voltage is $V_{out} = \gamma P_{in}$, where γ is the diode voltage sensitivity [23].

3.2.1.5 Design Considerations for Video Detector

The basic video detector circuit and its equivalent representations are given in Figure 3-5; (a) shows the complete video detector circuit, (b) shows the equivalent circuit at the RF port and (c) shows the equivalent circuit at the video port.

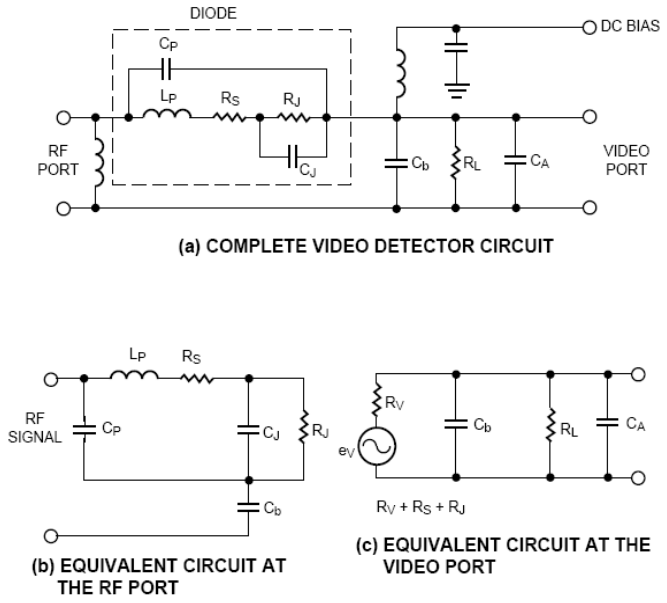

Figure 3-5: Video detector equivalent circuits [23]

3.2.1.5.1 Video Circuit Design Considerations [23]

In Figure 3-5 R_V is the diode video resistance, R_L represents the load resistance or the input resistance of the amplifier, c_b is the RF bypass capacitor and c_A represents the amplifier input capacitance. It is obvious that the equivalent circuit at the video port operates like a parallel RC filter with an upper 3dB frequency $f_{u(3dB)} = \frac{1}{2\pi R_T c_T}$

where $R_T = R_V \,//\, R_L = \frac{R_V R_L}{R_V + R_L}$ and $c_T = c_b + c_A$.

In order to increase the video bandwidth the upper 3dB frequency must be increased, which means the reduction of R_T and c_T. R_V or R_L can be reduced to decrease the value of R_T. However, it may not be possible to decrease R_L because this may lead to a reduction in amplification. Decreasing the value of R_V by biasing the diode with a positive voltage will increase the bandwidth, but decrease the sensitivity of the video detector at the same time. In the same way c_T can be decreased by decreasing

c_b or c_A. Since c_A is determined primarily by the amplifier circuit, decreasing c_b is a more proper choice. However, decreasing the value of c_b much smaller results in the reduction of the signal level delivered to the diode. The reactance of c_b must be smaller than the 10% of the RF impedance of the diode at the operating frequency.

3.2.1.5.2 RF Circuit Design Considerations [23]

RF circuit is composed of an RF filter matching the source resistance to the diode junction resistance R_j. The parameters c_j and R_s given in the equivalent circuit at the RF port introduces an RF loss which can be expressed as;

$$L_{dB} = 10\log\left[1 + \frac{R_s}{R_j} + w^2 {c_j}^2 R_s R_j\right] \qquad (3\text{-}2)$$

where $w = 2\pi f$

Since R_j can be expressed as $R_j \cong \frac{28}{I_d}$, (3-2) becomes

$$L_{dB} = 10\log\left[1 + \frac{R_s I_d}{28} + \frac{28 w^2 {c_j}^2 R_s}{I_d}\right] \qquad (3\text{-}3)$$

It is obvious from (3-3) that the diode DC bias current should be increased to minimize the loss of the signal, which means a less sensitive video detector will be obtained. Decreasing the diode video resistance by giving more DC bias current than required to obtain maximum TSS facilitates the broadband matching of the video detector.

3.3 Video Detector Design

The Schottky diodes are chosen for the detector design because of the reasons explained in the comparison section. In the video detector design Schottky diodes are

used for obtaining a larger dynamic range and making the diode detector operate in a wider temperature range; at the same time superior pulse response can be maintained with Schottky diode detectors.

At all the design steps there are two simulation results that must be checked whether the video detector is operating properly and the RF matching can be realized easily. The electromagnetic simulations are made with ADS^{TM} [25].

The first step in the video detector design is the determination of the RF choke RFC_1 and the bypass capacitor c_b. The values of these components determine the amount of RF signal power induced on the detector diode and the amount of the reflected wave at the input RF port. The detector output must be at reasonable levels and the expected diode detector input power-output video voltage characteristics must be maintained while RF matching is realizable. With these constraints some inductor and capacitor values are tested and optimized for a constant DC bias current.

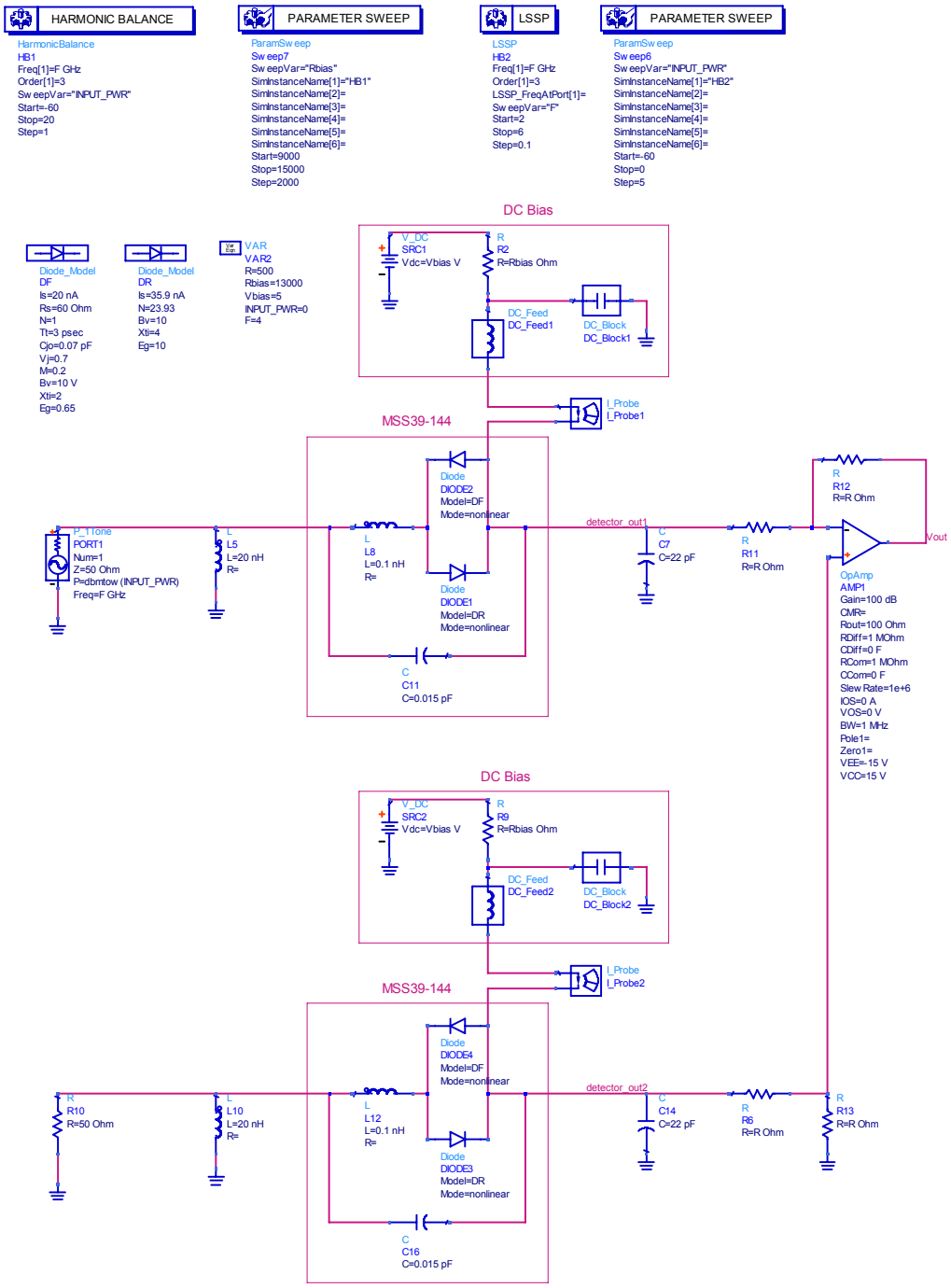

Figure 3-6: Video detector design

The video detector design seen in Figure 3-6 is composed of two identical diode detectors and an operational amplifier used for eliminating the effect of the DC bias current and obtaining the video signal originating only from the incoming RF signal. The inductor and the capacitor values make the S_{11} characteristics rotate in the Smith Chart. The imaginary part of S_{11} is intended to make as small as possible to facilitate RF matching. The appropriate inductor and capacitor values are chosen by optimization and found as $L = 20nH$ and $c = 22\,pF$ which can be obtained easily.

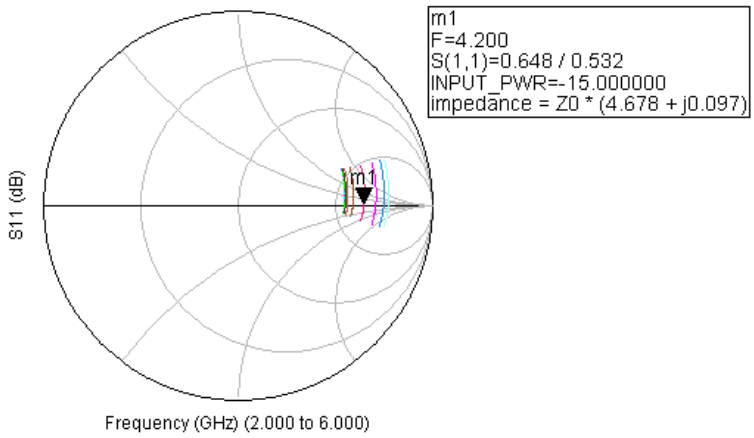

Figure 3-7: S11 characteristics of the video detector at a diode DC bias of $475\mu A$

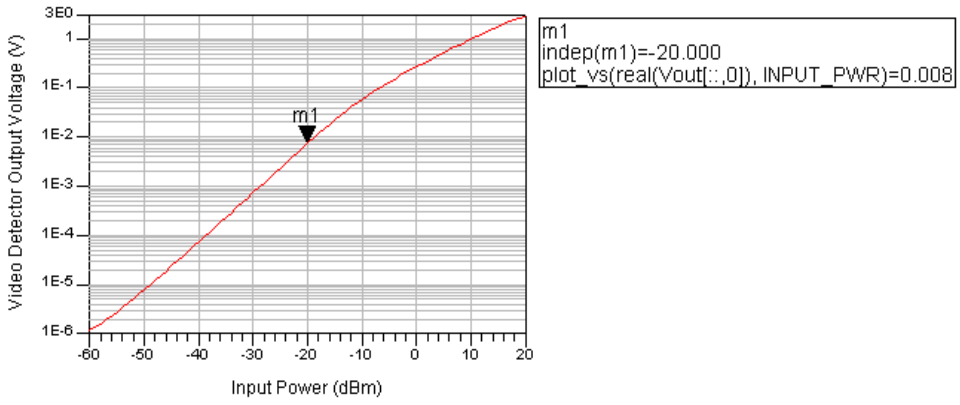

Figure 3-8: Input power-output voltage characteristics of the video detector at a diode DC bias of $475\mu A$

It is obvious from Figure 3-7 that RF matching circuitry is realizable and Figure 3-8 shows that a reasonable video output voltage can be maintained with the chosen inductor and capacitor values. The Schottky diode detector input power-output voltage characteristics composed of two detection regions as expected; the square law detection range and the linear region detection range, is also observed in Figure 3-8.

In order to obtain a more sensitive video detector the diode DC bias current is varied by sweeping the value of R_{bias} as seen in Figure 3-9.

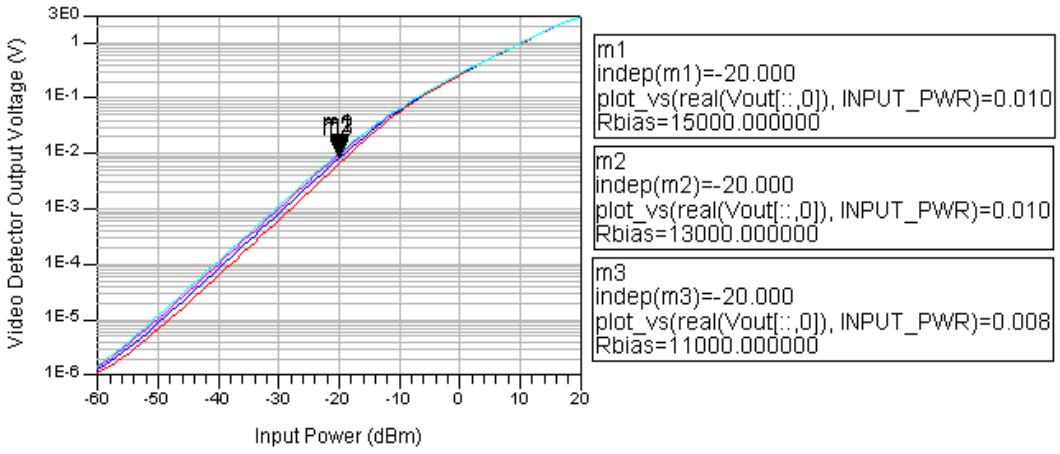

Figure 3-9: The effect of the DC bias current on the input power-output voltage characteristics of the video detector by sweeping the value of bias resistor R_{bias}

It is obvious that the detector is more sensitive when $R_{bias} = 15k\Omega$. However, increasing R_{bias} greater than $13k\Omega$ has no significant effect on sensitivity and increases the diode video resistance by decreasing the diode DC bias current which makes the RF matching circuit design more difficult. So, an intermediate value of $R_{bias} = 13k\Omega$ is chosen and Figure 3-10, Figure 3-11 and Figure 3-12 show the simulation results.

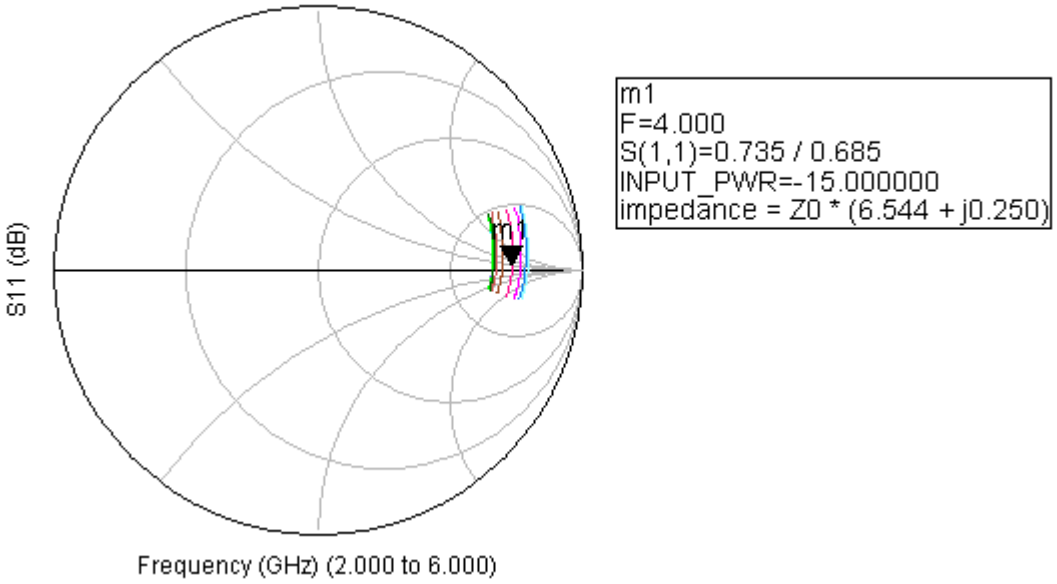

Figure 3-10: S11 characteristics of the video detector at $R_{bias} = 13k\Omega$ on Smith Chart (diode DC bias current $367\mu A$)

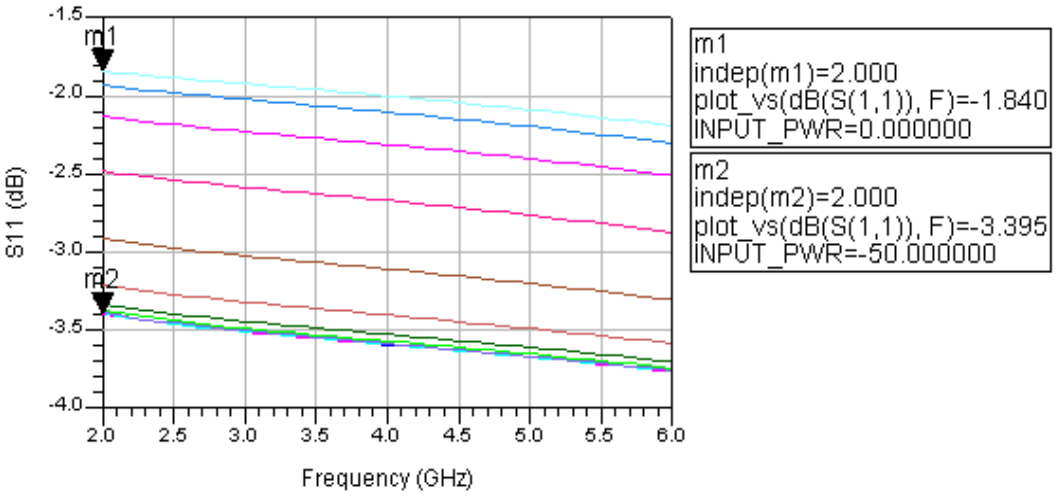

Figure 3-11: S11 characteristics of the video detector at $R_{bias} = 13k\Omega$ on rectangular plot (diode DC bias current $367\mu A$)

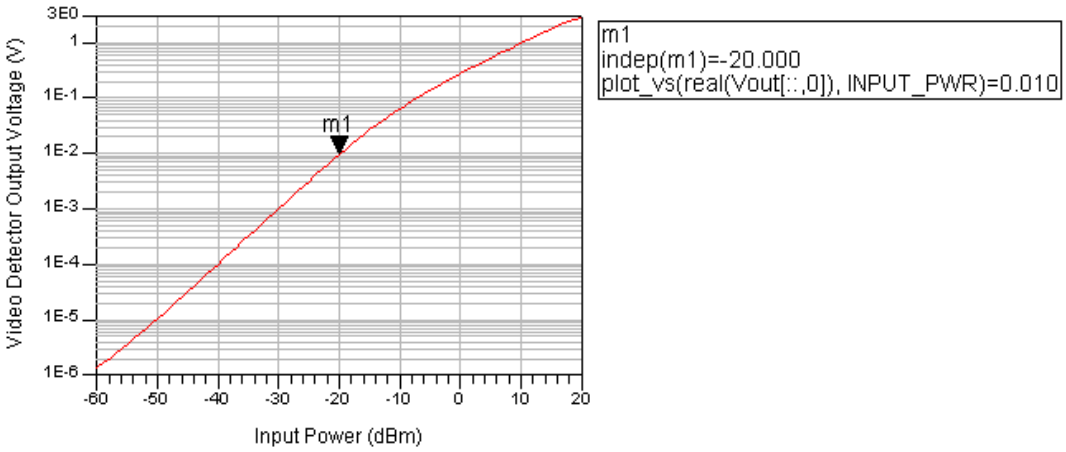

Figure 3-12: Input power-output voltage characteristics of the video detector at $R_{bias} = 13k\Omega$ (diode DC bias current $367\mu A$)

Up to this stage the gain of the operational amplifier is unity. The gain can be adjusted to obtain the desired slope of the video detector. Increasing the gain also improves the S_{11} characteristics of the video detector. However, increasing the gain to a very high value results in the saturation of the operational amplifier and the whole dynamic range cannot be used for video detection. A gain of 4 will be sufficient for this purpose. The resulting S_{11} characteristic of the video detector is given in Figure 3-13.

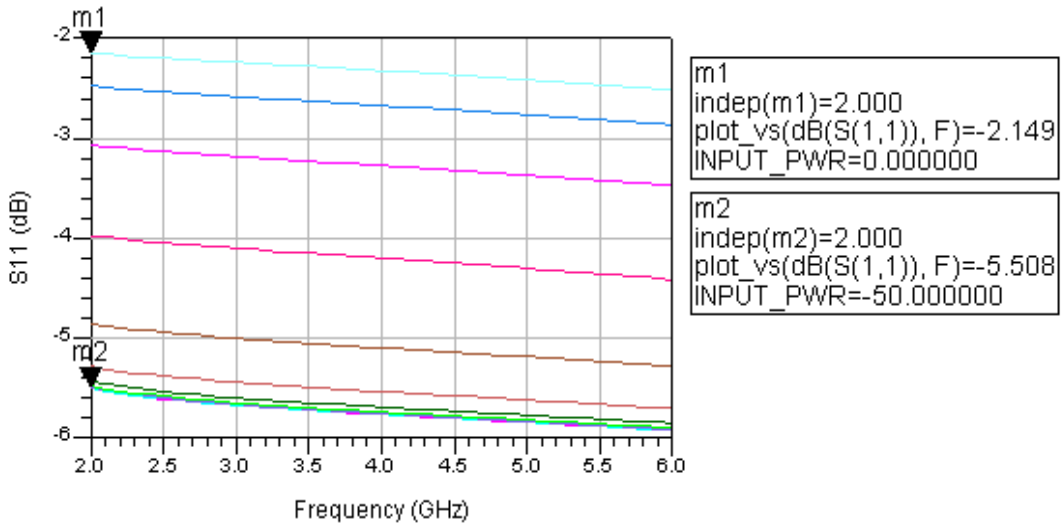

Figure 3-13: S11 characteristics of the video detector at $R_{bias} = 13k\Omega$ with a gain of 4 (diode DC bias current $367\mu A$)

The comparison of Figure 3-11 and Figure 3-13 concludes that increasing the gain of the operational amplifier decreases S_{11} values for the video detector. The improvement is more significant at low signal power levels.

Some lines must be added to mount the detector circuit components without disturbing the S_{11} characteristics; furthermore, these lines may be optimized to maintain better S_{11} characteristics making the RF impedance match easier.

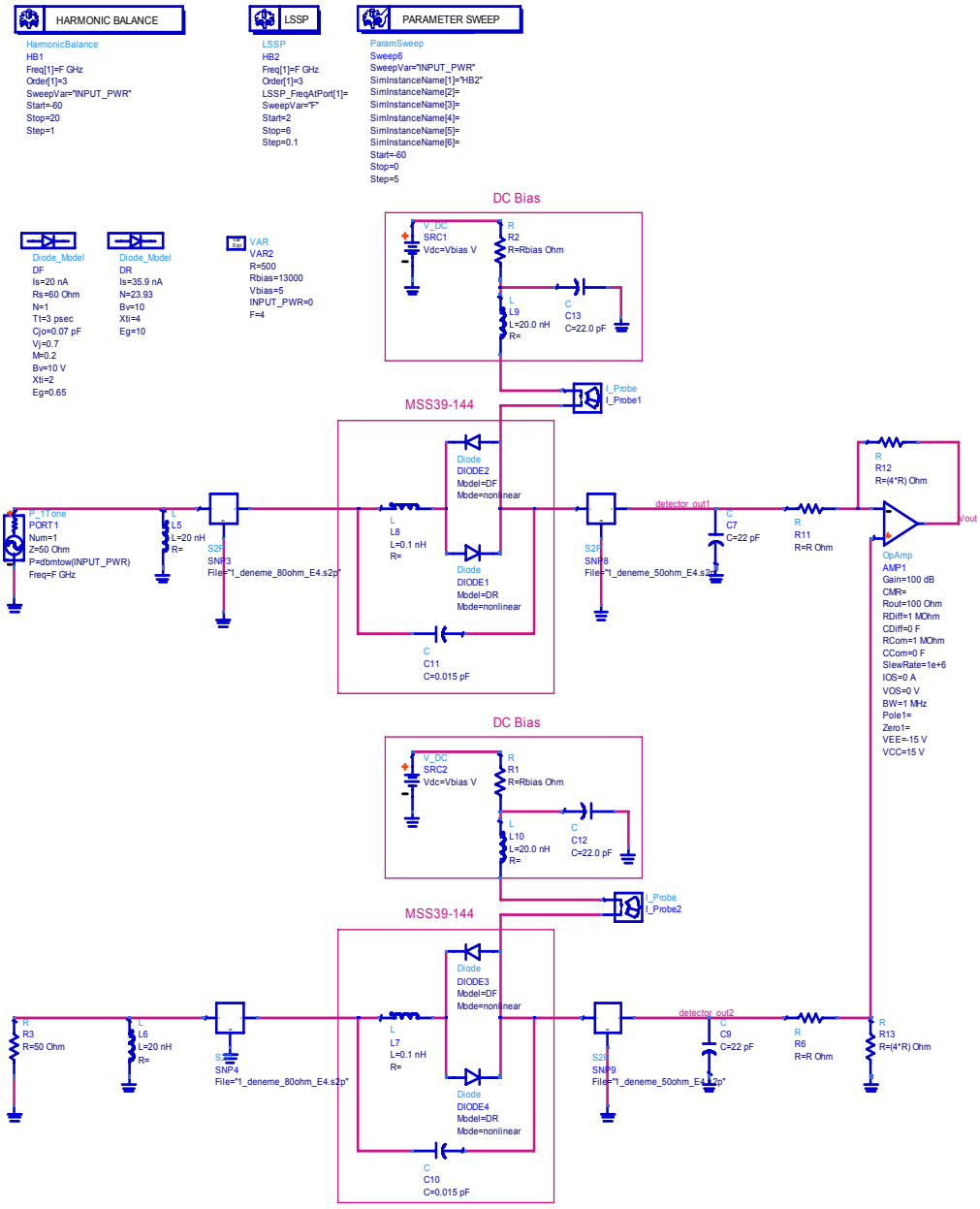

Figure 3-14: Video detector circuit after addition of lines to mount circuit components

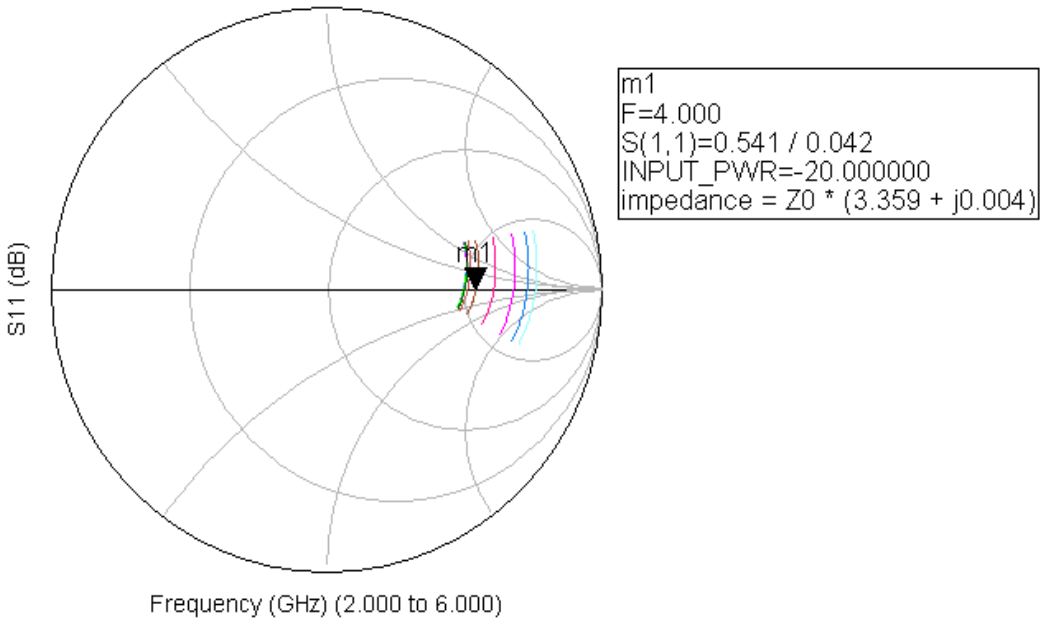

Figure 3-15: S11 characteristics of the video detector after addition of lines to mount circuit components

The next step is the determination of the RF matching circuitry. Quarter wave transformers can be used for broadband matching of real loads [26]. As seen from Figure 3-15 S_{11} at the center of the frequency band is real. So, this makes quarter wave transformers possible to be used for broadband matching of the video detector and the simulation results at the end of the frequency band will be accepted. Impedance matching tool of ADS™ [25] is used to obtain the matching circuitry.

After designing the matching sections with ADS™ [25], the physical dimensions of the transmission lines are determined with MWOffice® [27] and realizable values for the width and length of the transmission lines are chosen for the design. Since the signal is transmitted with a line surrounded by ground planes and the metal back is also grounded, grounded coplanar waveguide structure is chosen to maintain the closest electromagnetic simulation results with the real case as seen in Figure 3-16.

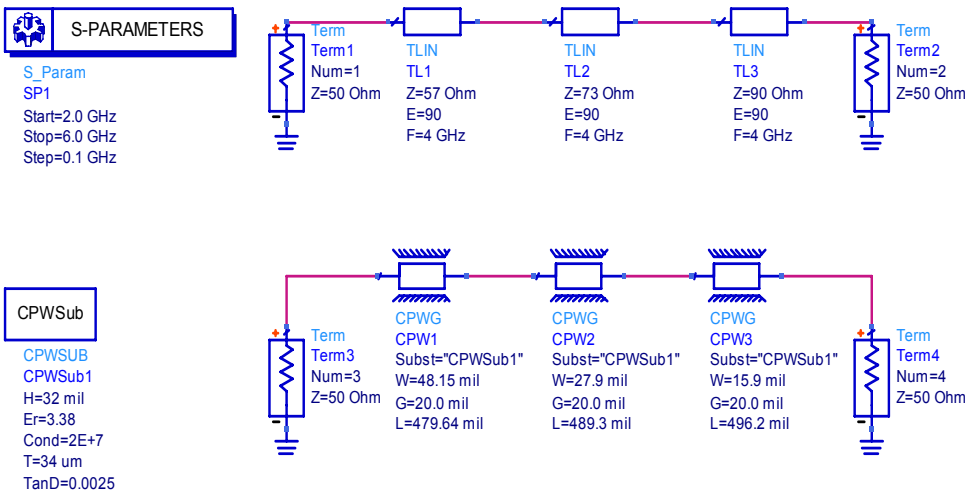

Figure 3-16: RF matching circuitry and its physical dimensions for CPW structure

Electromagnetic Simulation in Momentum [28]

At this stage it is beneficial to explain briefly how electromagnetic simulation is performed in Momentum. Assume a CPW structure as in Figure 3-17 will be simulated in Momentum.

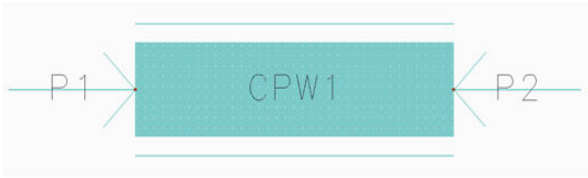

Figure 3-17: CPW structure

There are two ways to perform the electromagnetic simulation:

- Mapping metal layers instead of slot layers and using 2 single and 4 ground ports
- Mapping slot layers instead of metal layers and using 4 coplanar ports

First, consider mapping metal layers instead of slot layers. The conductor of the coplanar waveguide structure is surrounded by two other conductors modeling the ground plane as seen in Figure 3-18.

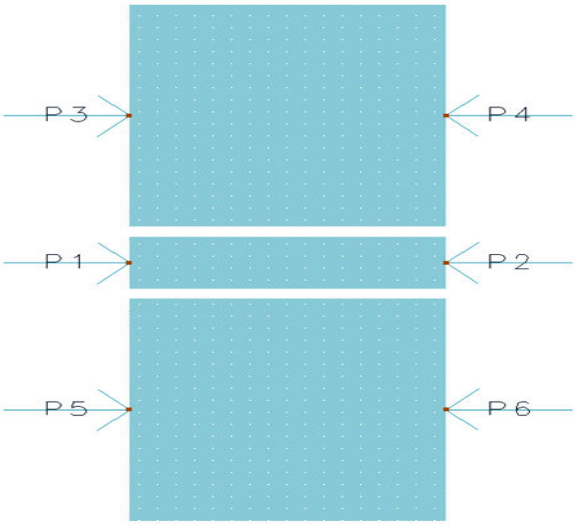

Figure 3-18: Mapping metal layers instead of slot layers

The substrate is updated from the schematic as in Figure 3-19.

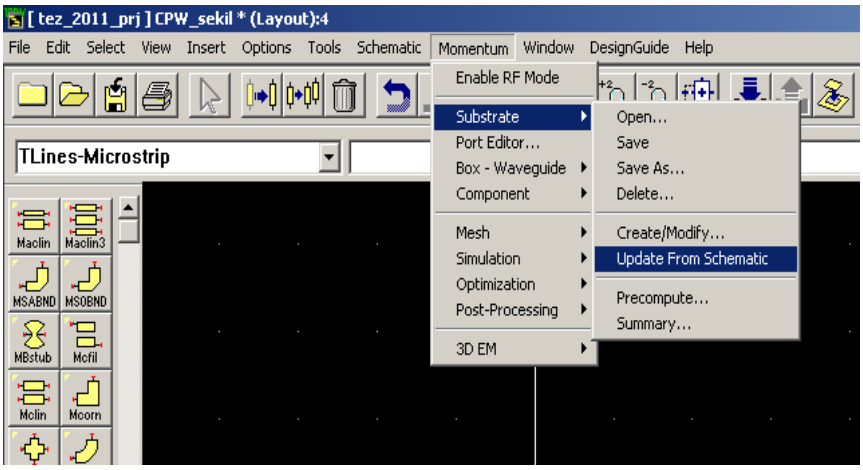

Figure 3-19: Updating the substrate from schematic

After updating the substrate from the schematic the layout mapping layer is modified and determined as strip from Layout Layers tab under Create/Modify Substrate option.

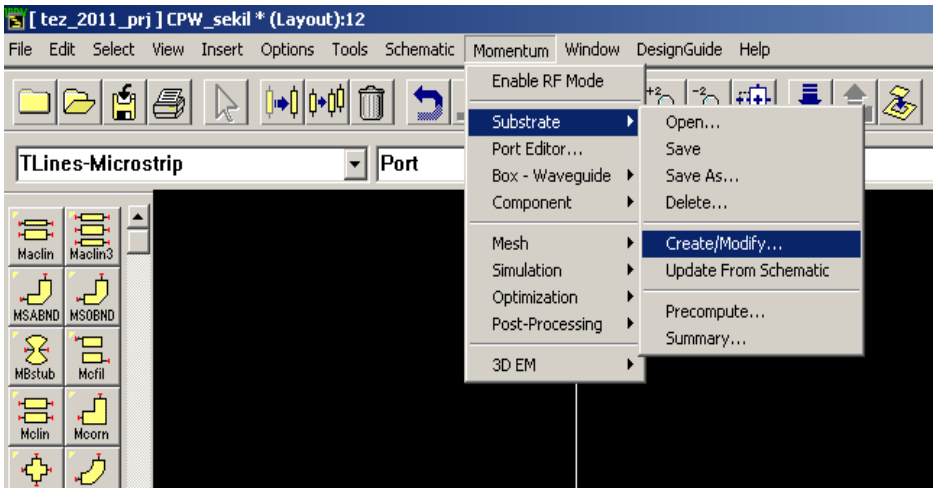

Figure 3-20: Modifying the substrate for strip mapping

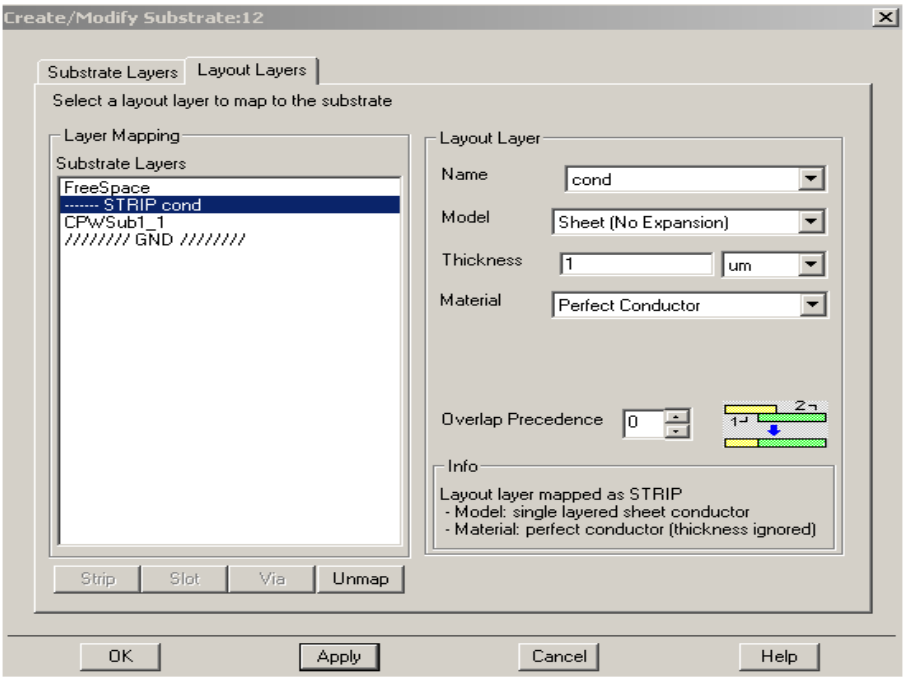

Figure 3-21: Layout layer mapping as strip

Port 1 and port 2 are assigned as single mode ports and the other ports are assigned as ground reference as seen in Figure 3-22.

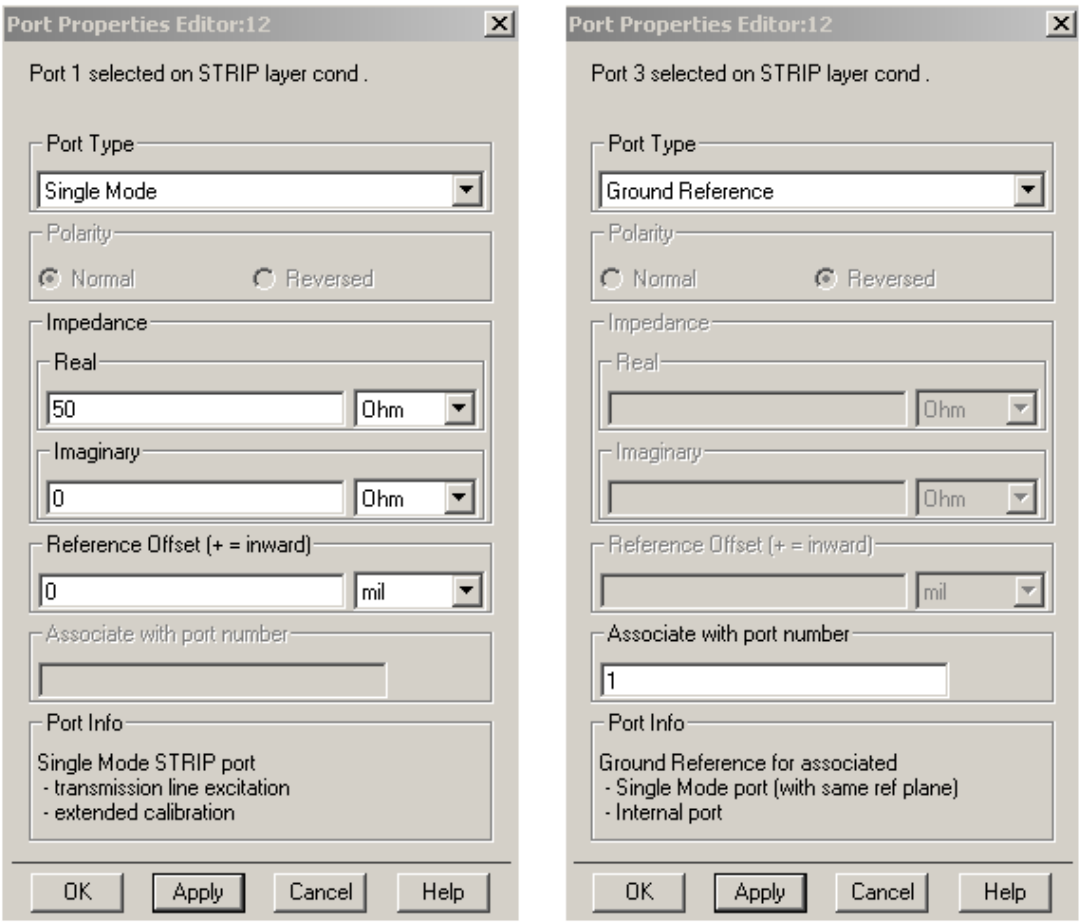

Figure 3-22: (a) Single mode port assignment (b) Ground reference port assignment

Mapping slot layers is a simpler method than mapping metal layers since the physical dimensions of the slots are determined by the coplanar waveguide structure as seen in Figure 3-23.

Figure 3-23: Mapping slot layers instead of metal layers

As in metal layer mapping, after updating the substrate from the schematic the layout mapping layer is modified and determined as slot from Layout Layers tab under Create/Modify Substrate option as seen in Figure 3-24.

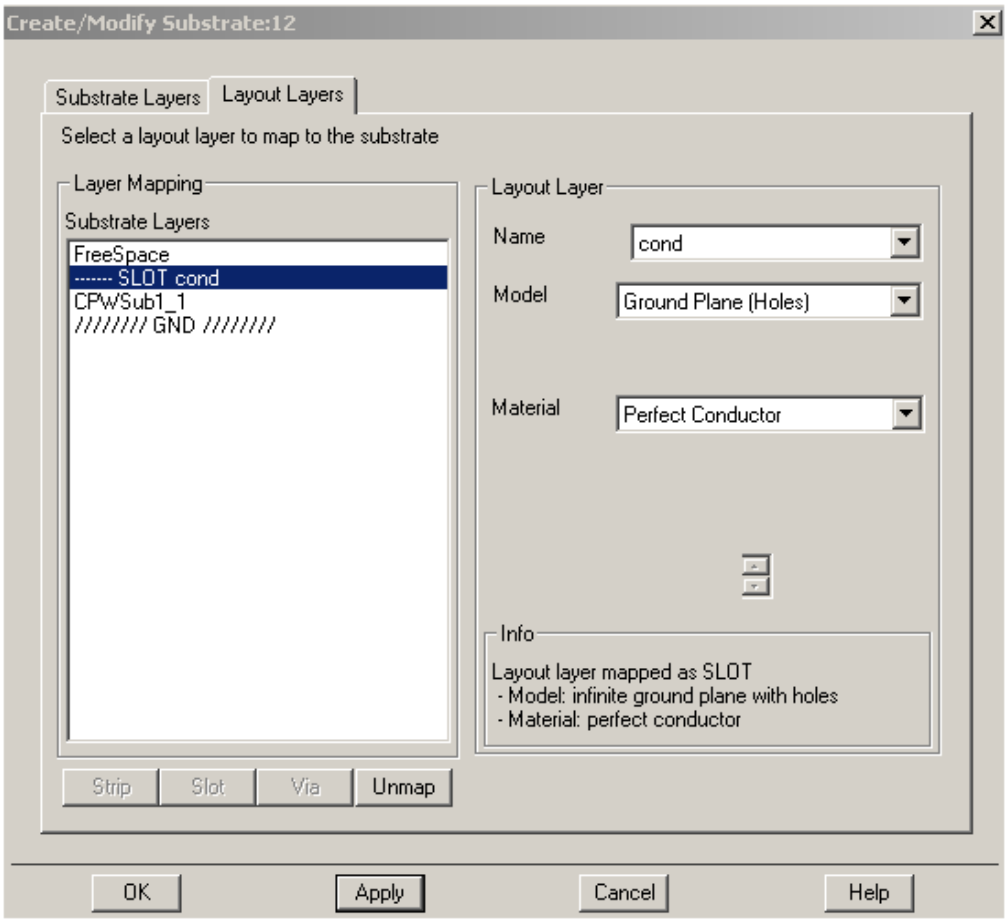

Figure 3-24: Layout layer mapped as slot

All the ports are assigned as coplanar mode ports and associated with the ports on the same side as in Figure 3-25.

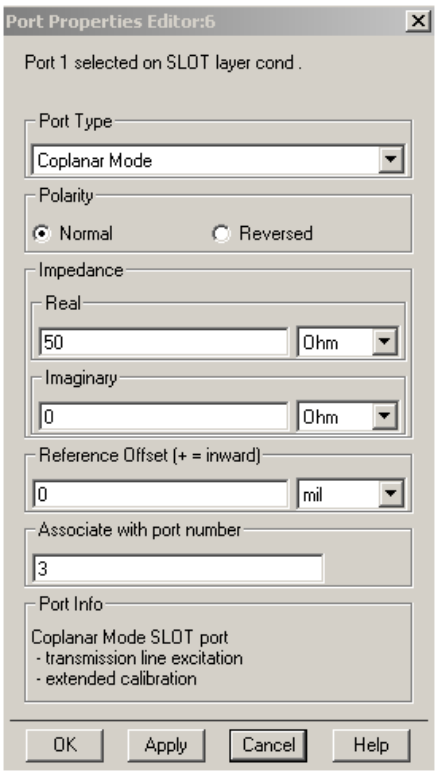

Figure 3-25: Assigning 4 coplanar ports in slot mapping

Mapping slot layers is chosen for its simplicity to perform the electromagnetic simulation in Momentum. The layout of the RF matching circuitry and the corresponding slot layer mapping are given in Figure 3-26 and Figure 3-27 respectively.

Figure 3-26: Layout of RF matching circuitry

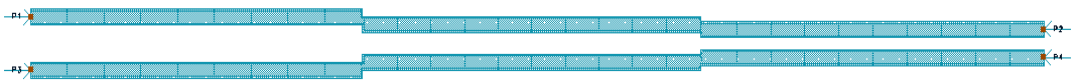

Figure 3-27: Slot layer mapping of the RF matching circuitry layout

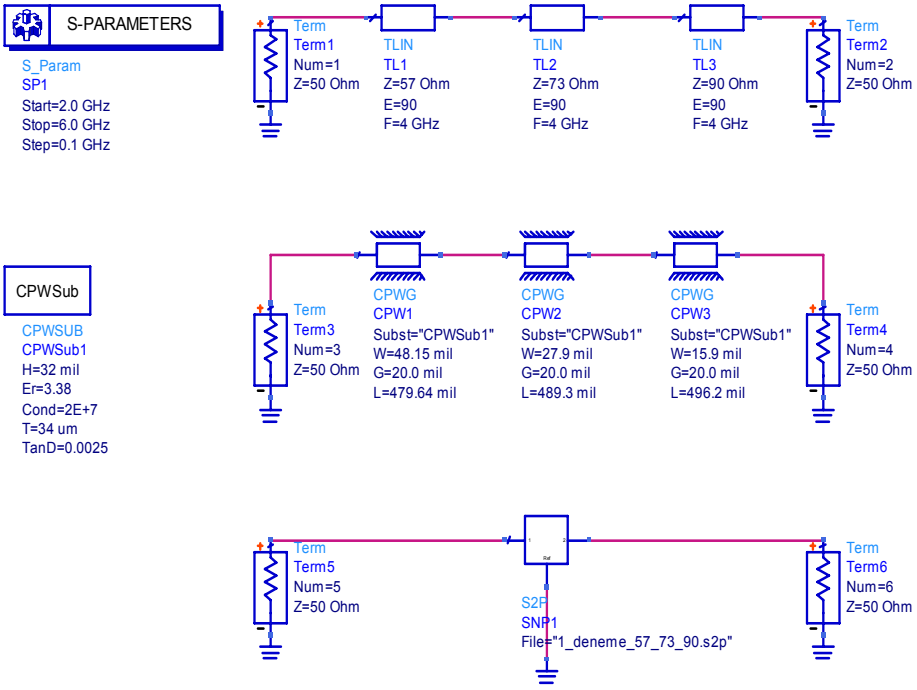

Figure 3-28: RF matching circuitry

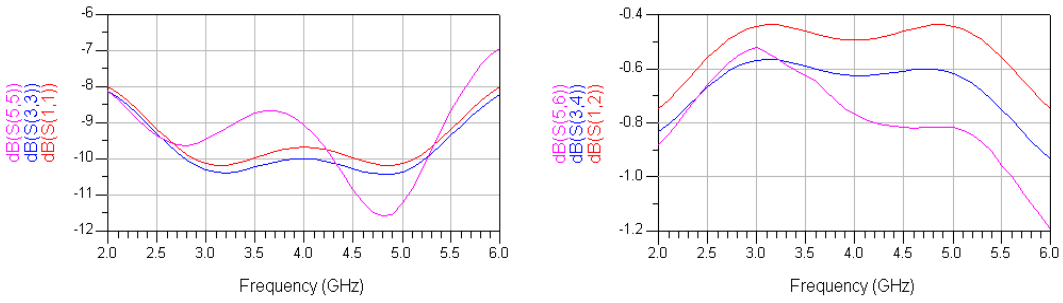

Figure 3-29: The reflection and transmission characteristics of the RF matching circuitry simulated with different methods

The simulations of the first and the second RF matching circuitry are close to each other as expected. The third simulation performed in Momentum has a difference at the end of the frequency band.

The RF matching circuitry is included as an .s2p file obtained from the electromagnetic simulation in Momentum as seen in Figure 3-30.

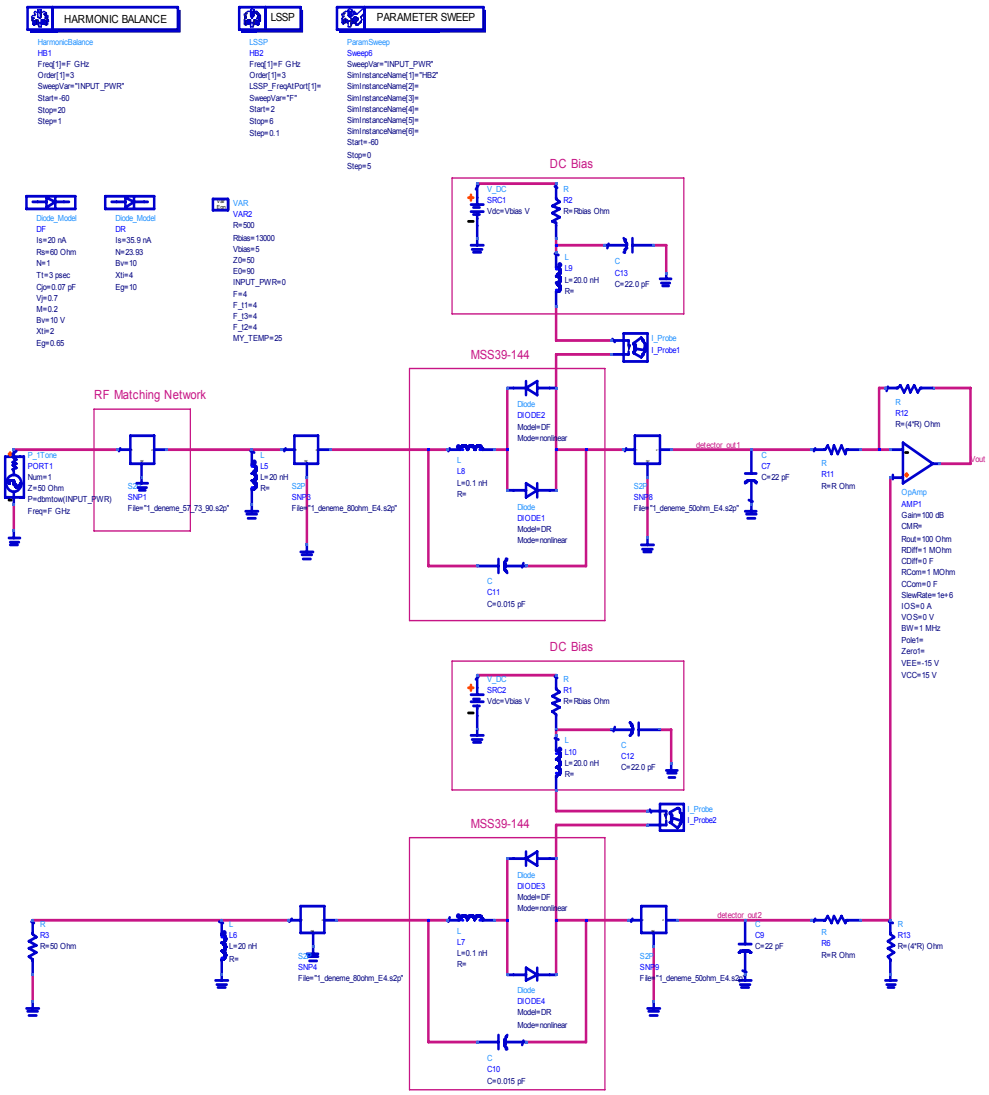

Figure 3-30: Video detector design with RF matching circuitry

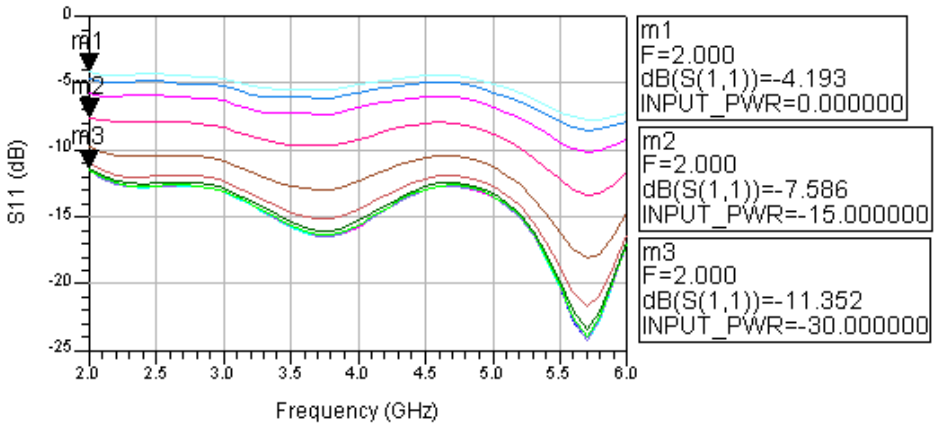

Figure 3-31: S11 characteristics of the video detector after the RF matching circuitry design

The improvement of the video detector S11 characteristics can be observed by the comparison of the Figure 3-13 and Figure 3-31. Since the video resistance of the detector diode is varying with the input signal power S11 characteristics of the video detector changes at the same time. It is acceptable to obtain S11 at a level of -10dB for a video detector at an input power of -20dBm. The resulting output video voltage is simulated in Figure 3-32.

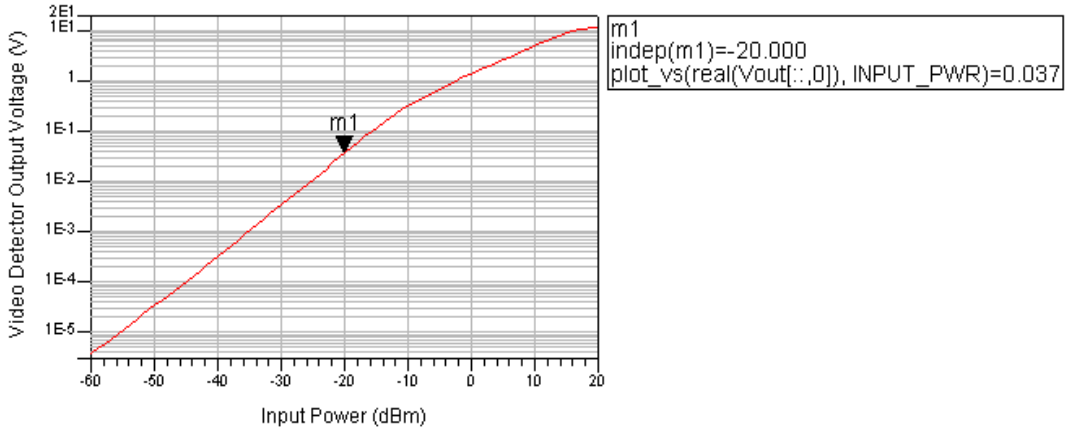

Figure 3-32: Input power-output voltage characteristics of the video detector after the RF matching circuitry design

CHAPTER 4

LOGARITHMIC AMPLIFIER

4.1 Determination of the Operational Amplifier

In order to eliminate the video signal originating from the bias voltages of the Schottky diodes and the offset voltages originating from the temperature differences two Schottky diode detectors are used in a differential manner with an operational amplifier model defined in ADS^{TM} [25] in the previous section explaining the detector design. Since the gain of the logarithmic amplifier is very high, identical detectors must be used to minimize the offset voltage at the output of the operational amplifier; a small offset voltage causes a large video signal at the output of the video amplifier and the operational amplifier summing the video signals obtained from each logarithmic stage saturates making the detection of the RF signals impossible. At the same time, the noise at the output of the operational amplifier eliminating the signal originating from the bias voltages must be minimized to obtain TSS values as small as possible. Two operational amplifiers are compared for these purposes in Table 4-1 and in Table 4-2.

Table 4-1: Offset voltage performance at 25°C [29] [30]

	AD8099		MAX4226		
	Typ.	Max.	Typ.	Max.	Units
Input Offset Voltage	0.1	0.5	0.5	5	mV
Input Offset Voltage Drift	2.3		2		μV/°C

It is obvious from Table 4-1 that the input offset voltage of AD8099 is smaller than the MAX4226 counterpart.

Table 4-2: Noise performance [29] [30]

	AD8099	MAX4226
Input Noise Voltage Density	$0.95nV/\sqrt{Hz}$ at $f = 100kHz$	$2nV/\sqrt{Hz}$ at $f = 10kHz$

It can also be seen from Table 4-2 that the noise performance of AD8099 is superior to MAX4226. Noise performance of MAX4226 and AD8099 are simulated and the results are presented in Figure 4-2 and Figure 4-4.

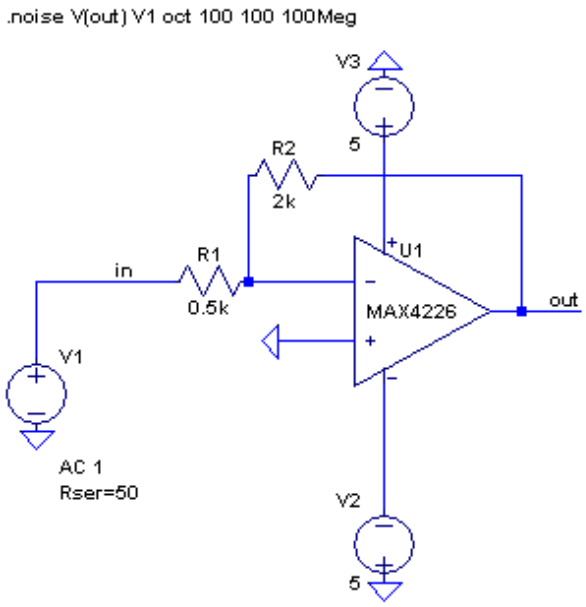

Figure 4-1: MAX4226 circuit schematic

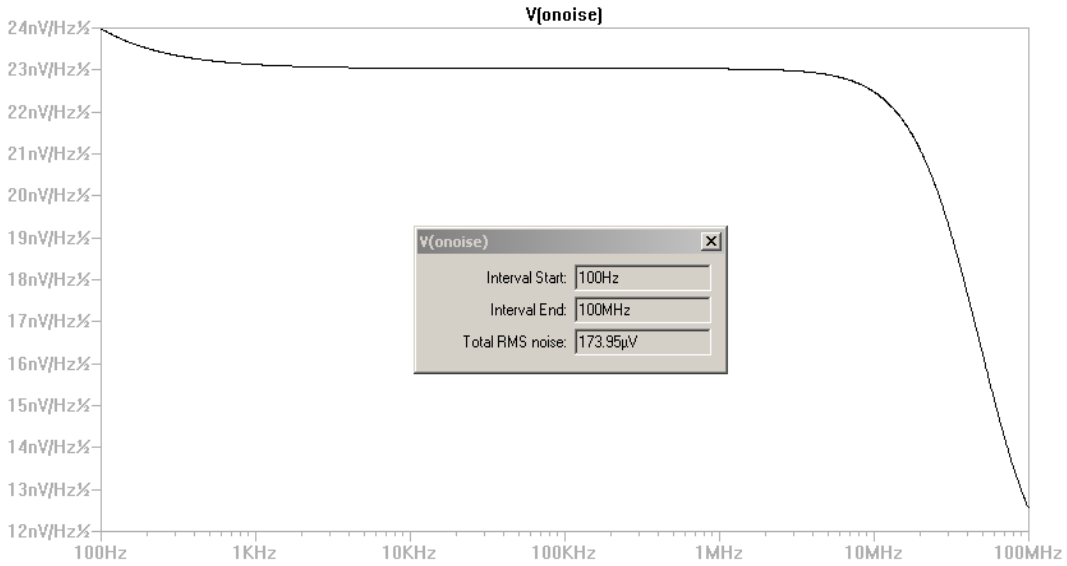

Figure 4-2: MAX4226 noise performance

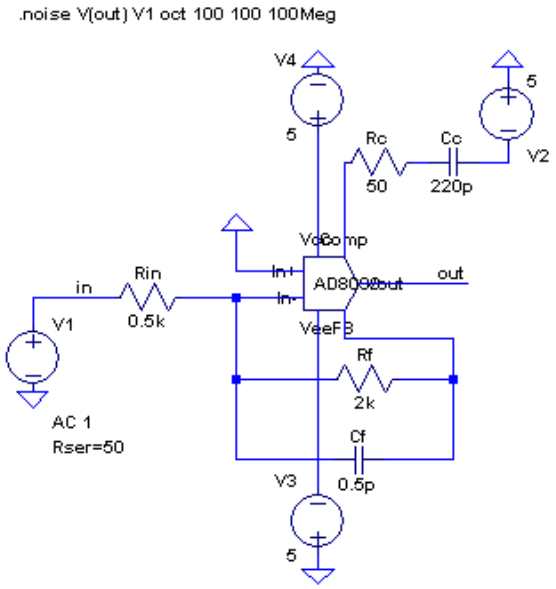

Figure 4-3: AD8099 circuit schematic

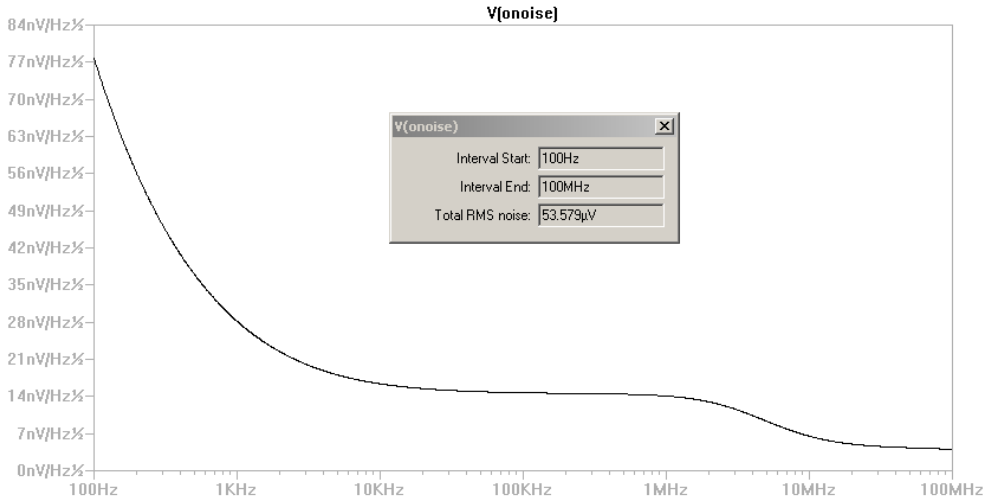

Figure 4-4: AD8099 noise performance

Comparing Figure 4-2 and Figure 4-4 obtained with LTspice/SwitcherCad III [19] shows that AD8099 is more convenient than MAX4226 with a much better noise performance. The noise performance of AD8099 can be improved by adjusting the compensation components, but this may result in the reduction of the bandwidth at

the same time; the compensation components are chosen to maintain this compromise. So, AD8099 is chosen for the design with its superior noise and offset voltage performances.

4.2 Logarithmic Amplifier Specifications

The input power-output video voltage characteristics of the Schottky diode detectors comprises of two detection regions with different slopes: the square law detection region and the linear detection region. In order to obtain a wide dynamic range both of the detection regions must be used and the slopes must be equated for the desired logarithmic response. The gains of each amplifier stage are determined by the parallel amplification parallel summation method explained in the literature survey.

4.2.1 Square Law Detection Region

The dynamic range of the DLVA is chosen as 50dB in order to obtain maximum sensitivity with a small number of realizable gain stages.

Dynamic range (D): 50dB

Number of stages (N): 4

The parameters of the amplifier stages are calculated as;

$$D = A^N \Rightarrow \begin{matrix} 20\log D = 50 \\ 20\log A^N = 50 \end{matrix} \Rightarrow A = 4.217$$

$$I_{L1} = I_L \frac{A}{A-1} = 1.31 I_L$$

Choose $g_m = 1$ for simplicity.

With these parameters the gains of each individual logarithmic stage are calculated according to (1-16) as,

$$G_1 = g_m = 1$$
$$G_2 = g_m (A-1) = 3.217$$
$$G_3 = g_m A(A-1) = 13.57$$
$$G_4 = g_m A^2 (A-1) = 57.2$$

Since the parallel amplification parallel summation method is used the limiting values of the differential amplifier stages constituting the DLVA must be small in

order not to saturate the operational amplifier summing the video signals obtained from different amplifier stages. The collector resistor R_C has a deterministic effect on the limiting voltage values of the differential amplifiers used as logarithmic stages with the current obtained from the current mirror. So, R_C is chosen as $R_C = 1.8k\Omega$ and R_M is chosen as $R_M = 35k\Omega$.

Since $I_{L1} = 1.31 I_L$ and $R_M = 35k\Omega$, the resistor of the current mirror at the amplifier stage with the least gain is calculated as

$$R_{M1} = R_M / 1.31 = 35k\Omega / 1.31 = 26.7k\Omega$$

So, R_{M1} is chosen as $R_{M1} = 26.5k\Omega$.

With these current mirror resistors the corresponding emitter currents are calculated as $I_M = 266\mu A$ and $I_{M1} = 350\mu A$ which result in emitter resistors as $r_e = 188\Omega$ and $r_{e1} = 142.5\Omega$ respectively.

According to (2-8) the circuit components are calculated as;

$$G_1 \cong -\frac{R_{C1}}{(r_{e1} + R_{E1})} = -\frac{1.8k\Omega}{(142.5\Omega + R_{E1})} = -1 \Rightarrow R_{E1} = 1.658k\Omega$$

$$G_2 \cong -\frac{R_{C2}}{(r_{e2} + R_{E2})} = -\frac{1.8k\Omega}{(188\Omega + R_{E2})} = -3.217 \Rightarrow R_{E2} = 371.5\Omega$$

Since the third and the fourth gains are high, two gain stages are used, one of which is common for both logarithmic stages.

$$G_3 \cong -\frac{R_{C3}}{(r_{e3} + R_{E3})}\frac{R_C}{(r_e + R_E)} = -\frac{1.8k\Omega}{(188\Omega + R_{E3})}\frac{3.9k\Omega}{(188\Omega + R_E)} = -13.57$$

Choose $\dfrac{3.9k\Omega}{(188\Omega + R_E)} = 15 \Rightarrow R_E = 72\Omega$

Then $\dfrac{1.8k\Omega}{(188\Omega + R_{E3})} = 0.9047 \Rightarrow R_{E3} = 1.8k\Omega$

$$G_4 \cong -\frac{R_{C4}}{(r_{e4} + R_{E4})}\frac{R_C}{(r_e + R_E)} = -\frac{1.8k\Omega}{(188\Omega + R_{E4})}\frac{3.9k\Omega}{(188\Omega + R_E)} = -57.2$$

Since

$$\frac{3.9k\Omega}{(188\Omega + R_E)} = 15 \Rightarrow \frac{1.8k\Omega}{(188\Omega + R_{E4})} = 3.813 \Rightarrow R_{E4} = 284\Omega$$

The calculated resistor values are $R_{E1} = 1.658k\Omega$, $R_{E2} = 371.5\Omega$, $R_E = 72\Omega$, $R_{E3} = 1.8k\Omega$, $R_{E4} = 284\Omega$ where R_{Ei} represents the emitter resistances of each individual stage and R_E represents the emitter resistor of the common differential amplifier used to obtain high gain values for the third and the fourth stages.

The emitter resistor values are chosen as close as possible to the calculated values and the design is simulated with the resistor values; $R_{E1} = 1.5k\Omega$, $R_{E2} = 357\Omega$, $R_E = 75\Omega$, $R_{E3} = 1.8k\Omega$, $R_{E4} = 274\Omega$.

The gain resistors at the output stage of the DLVA summing the video signals obtained from different logarithmic stages are chosen as $5k\Omega$ in order to prevent the operational amplifier LMH6725 from going into saturation.

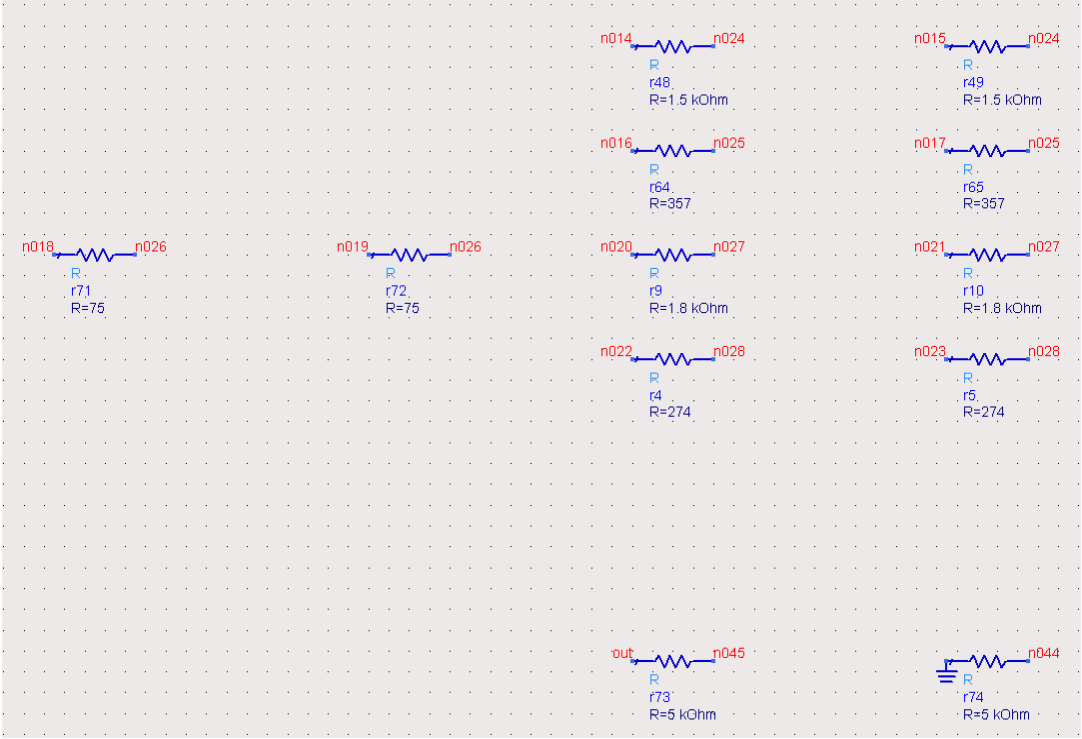

Figure 4-5: Selected resistor values for logarithmic amplification

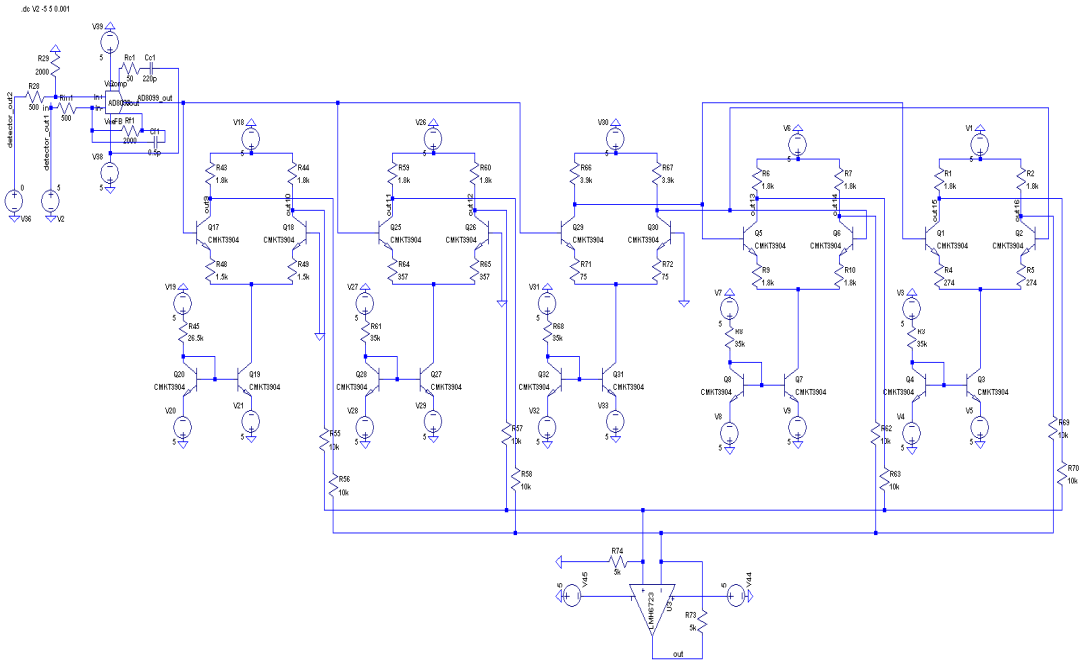

Figure 4-6: The circuit schematic of the logarithmic amplifier with selected resistor values

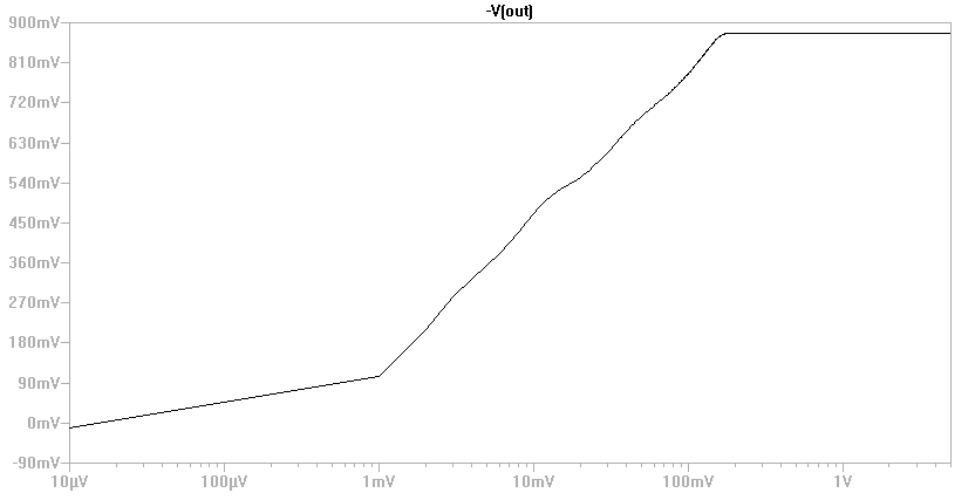

Figure 4-7: The input voltage-output voltage characteristics of the logarithmic amplifier in logarithmic scale

The circuit schematic given in Figure 4-6 is simulated with LTspice/SwitcherCad III [19] and the corresponding input voltage-output voltage characteristic of the logarithmic amplifier is observed in Figure 4-7. The dynamic range is sufficient; however, it is obvious that the gain of the logarithmic stages must be adjusted to obtain linearity in the input voltage-output voltage characteristics.

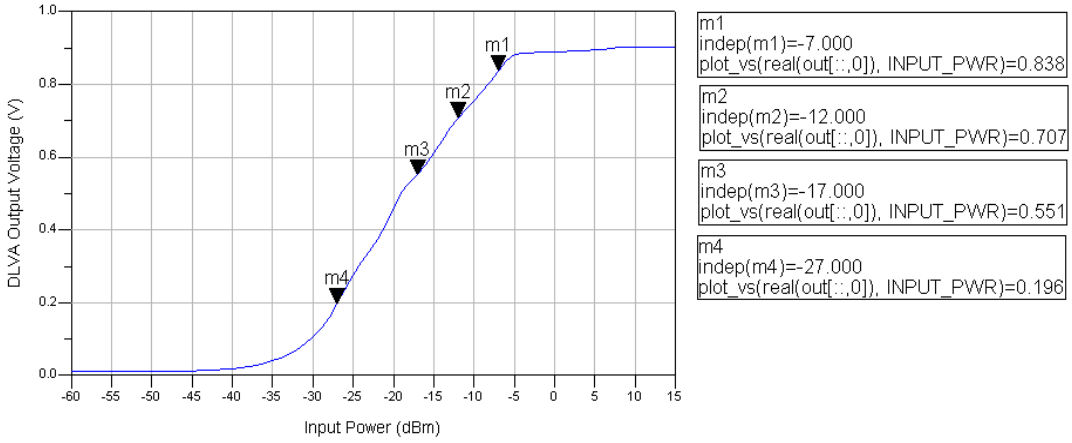

Figure 4-8: The input power-output voltage characteristics of DLVA with four logarithmic stages

The DLVA design is simulated and the input power-output voltage characteristic is maintained as in Figure 4-8. Different from Figure 4-7, a change in slope is observed in Figure 4-8. This results from the Schottky diode detector characteristics comprising of two different detection regions as the square law detection region and the linear detection region. Figure 4-9 shows the change in slope at the output of AD8099.

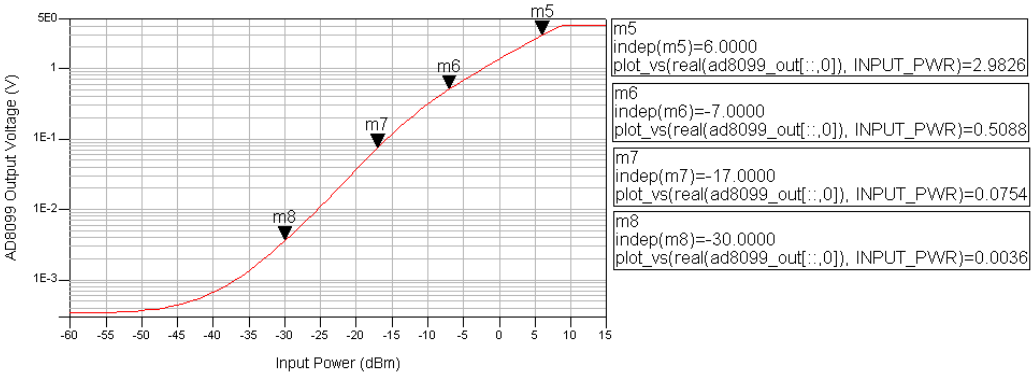

Figure 4-9: The input power-output voltage characteristics at the output of AD8099

In order to maintain linearity in the input power-output voltage characteristics of DLVA some modifications must be made. As a starting point the emitter resistor of the logarithmic stage with the least gain must be made smaller for a larger gain. The emitter resistor $R_{E1} = 1.5k\Omega$ is changed with $R_{E1} = 0.8k\Omega$ for this purpose as in Figure 4-10.

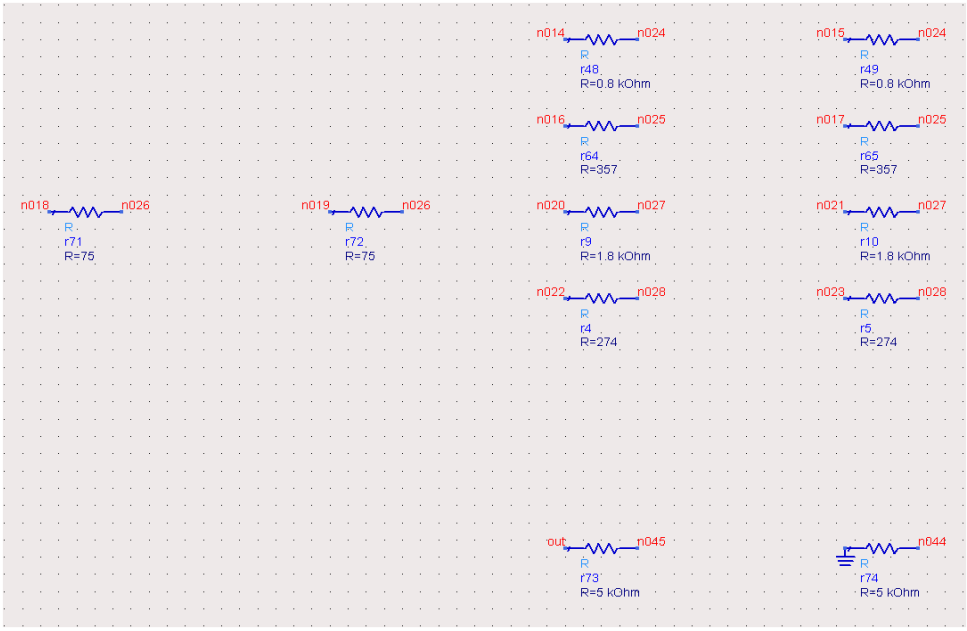

Figure 4-10: Modified resistor values to maintain linearity in the input power-output voltage characteristics of DLVA

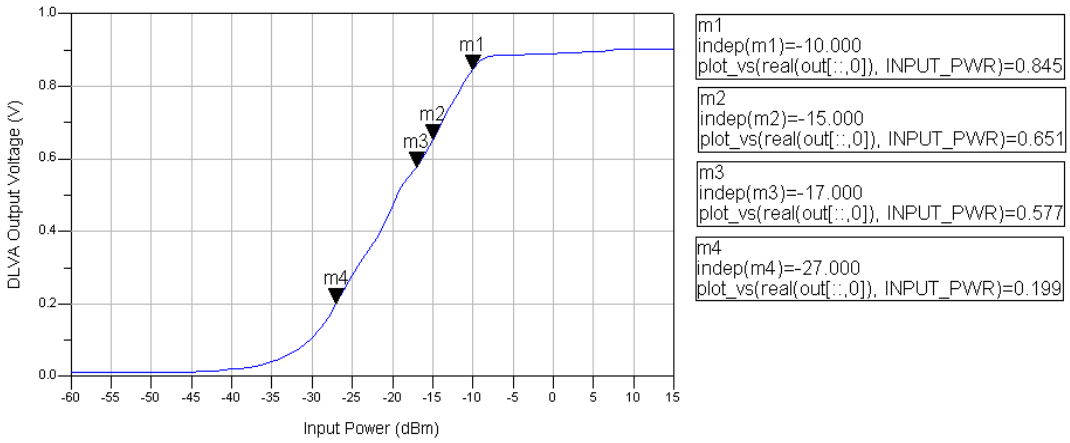

Figure 4-11: The input power-output voltage characteristics of DLVA with modified resistor values to maintain linearity

The input power-output voltage characteristics of DLVA with the emitter resistor changed to $R_{E1} = 0.8k\Omega$ is observed in Figure 4-11. The linearity is maintained with small deviations. However, the dynamic range can be extended much more by using the linear detection region and adjusting the slope of the linear detection region with respect to the square law detection region for the desired logarithmic response.

4.2.2 Linear Detection Region

For the linear detection region the dynamic range is chosen as 35dB and the number of logarithmic stages is 4 for a simpler circuitry. It must be kept in mind that the sensitivity region of the last logarithmic stage of the linear detection region coincides with the first logarithmic stage of the square law detection region as observed in Figure 4-11, which means the total number of logarithmic stages in DLVA will be 7 instead of 8.

Dynamic range (D): 35dB

Number of stages (N): 4

$$D = A^N \Rightarrow \begin{matrix} 20\log D = 35 \\ 20\log A^N = 35 \end{matrix} \Rightarrow A = 2.74$$

$$I_{L1} = I_L \frac{A}{A-1} = 1.575 I_L$$

The slopes of the square law detection region and the linear detection region can be adjusted roughly with the simulation observed in Figure 4-8.

The slope of the linear detection region is;

$$\frac{838-707}{5} = 26.2$$

The slope of the square law detection region is;

$$\frac{551-196}{10} = 35.5$$

The slope variation is compensated by changing the g_m value for the linear detection region and it is calculated as

$$g_m = \log 26.2 - \log 35.5 = -0.132$$

With these parameters the gains of each individual logarithmic stage are according to (1-16),

$$G_1 = g_m = 0.132$$
$$G_2 = g_m (A-1) = 0.23$$
$$G_3 = g_m A(A-1) = 0.63$$
$$G_4 = g_m A^2 (A-1) = 1.72$$

As in the square law detection region calculations R_C is chosen as $R_C = 1.8k\Omega$ and R_M is chosen as $R_M = 26.5k\Omega$.

Since $I_{L1} = 1.575 I_L$ and $R_M = 26.5k\Omega$, the resistor of the current mirror at the amplifier stage with the least gain is calculated as

$$R_{M1} = R_M / 1.575 = 26.5k\Omega / 1.575 = 16.8k\Omega$$

With these current mirror resistors the corresponding emitter currents are calculated as $I_M = 350\mu A$ and $I_{M1} = 554\mu A$ which result in emitter resistors as $r_e = 142.5\Omega$ and $r_{e1} = 90\Omega$ respectively.

According to (2-8) the circuit components are calculated as;

$$G_1 \cong -\frac{R_{C1}}{(r_{e1} + R_{E1})} = -\frac{1.8k\Omega}{(90\Omega + R_{E1})} = -0.132 \Rightarrow R_{E1} = 13.55k\Omega$$

$$G_2 \cong -\frac{R_{C2}}{(r_{e2}+R_{E2})} = -\frac{1.8k\Omega}{(142.5\Omega+R_{E2})} = -0.23 \Rightarrow R_{E2} = 7.68k\Omega$$

$$G_3 \cong -\frac{R_{C3}}{(r_{e3}+R_{E3})} = -\frac{1.8k\Omega}{(142.5\Omega+R_{E3})} = -0.63 \Rightarrow R_{E3} = 2.7k\Omega$$

$$G_4 \cong -\frac{R_{C4}}{(r_{e4}+R_{E4})} = -\frac{1.8k\Omega}{(142.5\Omega+R_{E4})} = -1.72 \Rightarrow R_{E4} = 904\Omega$$

The calculated resistor values are $R_{E1} = 13.55k\Omega$, $R_{E2} = 7.68k\Omega$, $R_{E3} = 2.7k\Omega$, $R_{E4} = 904\Omega$ where R_{Ei} represents the emitter resistances of each individual stage. The emitter resistor values are chosen as close as possible to the calculated values and the design is simulated with the resistor values; $R_{E1} = 13.3k\Omega$, $R_{E2} = 7.68k\Omega$, $R_{E3} = 2.74k\Omega$, $R_{E4} = 909\Omega$.

Figure 4-12 shows the selected resistor values used in 7 logarithmic stages for logarithmic amplification.

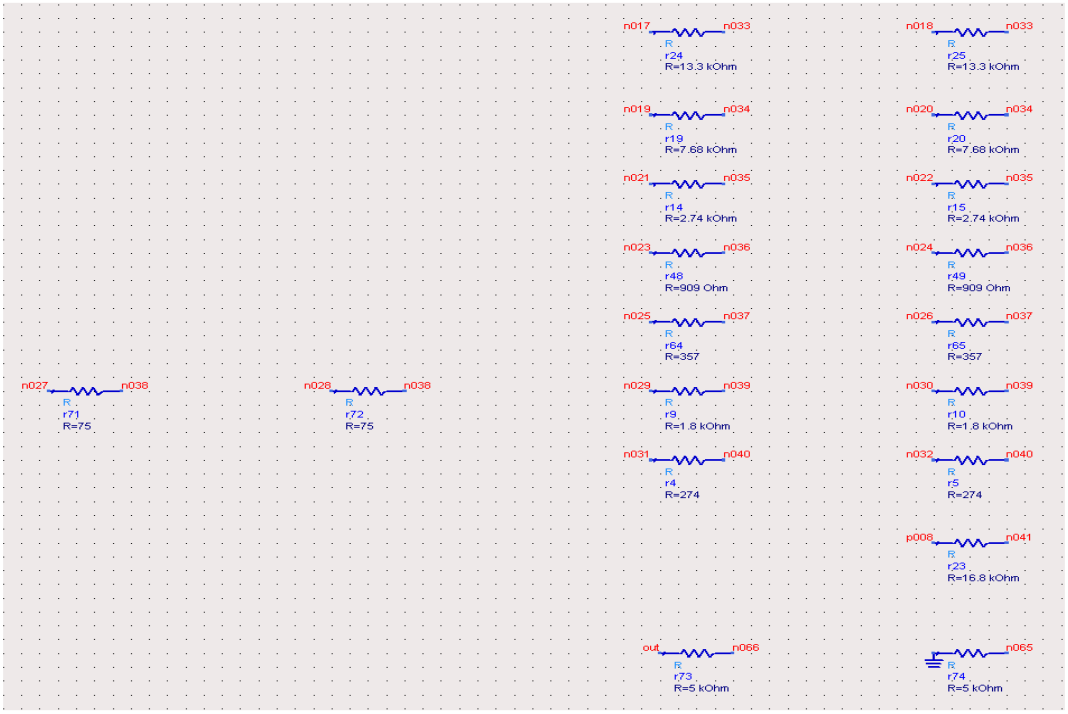

Figure 4-12: Selected resistor values used in 7 logarithmic stages for logarithmic amplification

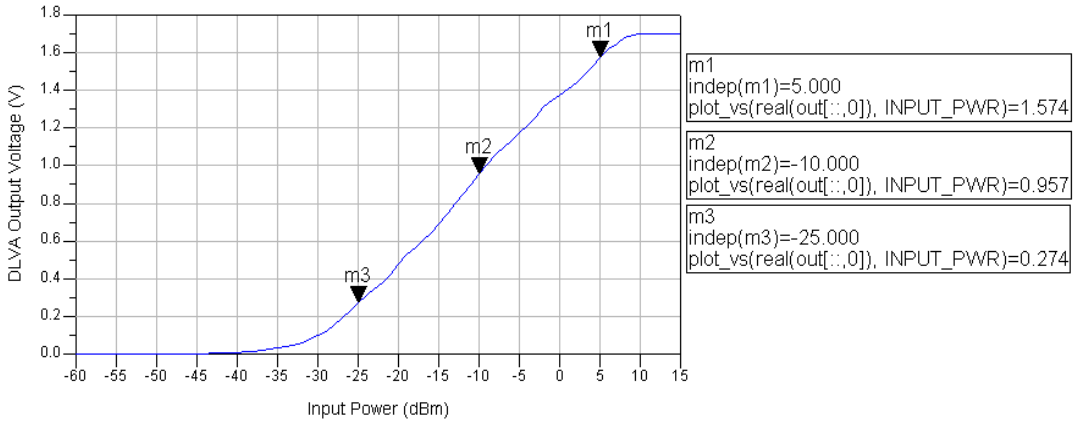

Figure 4-13: The input power-output voltage characteristics of DLVA with selected resistor values at 2GHz

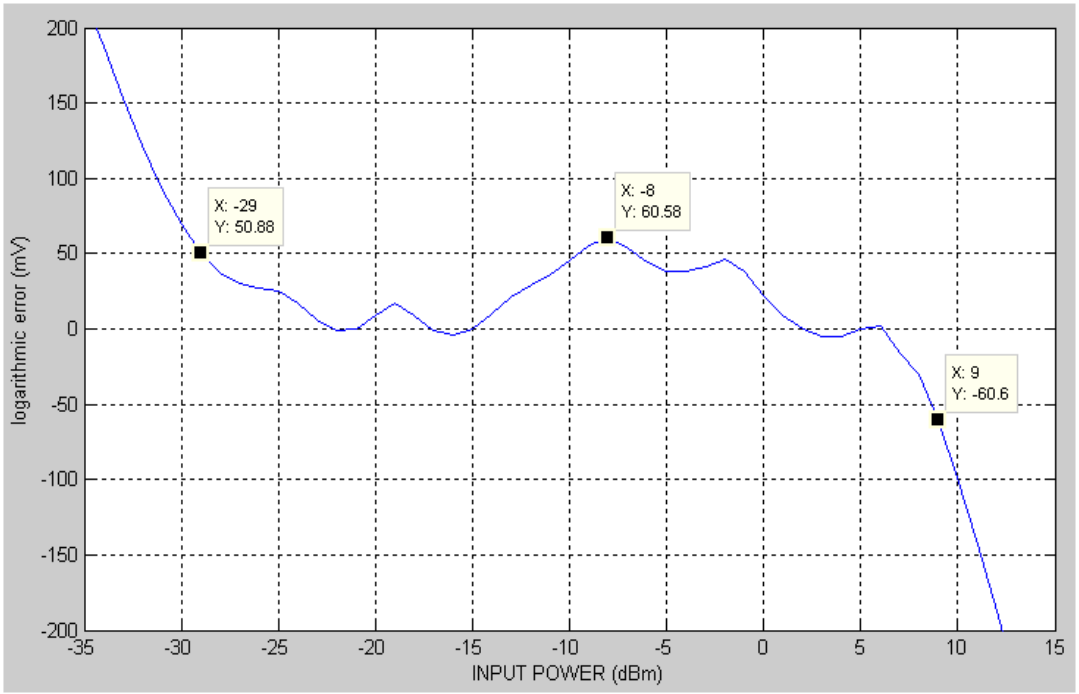

Figure 4-14: The logarithmic error of DLVA with changing input power with selected resistor values at 2GHz

It may be predicted from Figure 4-13 that the logarithmic response can be improved; in other words, the deviation from linearity may be minimized. The logarithmic error

observed in Figure 4-14 proves this situation and some modifications must be made to obtain a better logarithmic response with smaller logarithmic error.

Figure 4-15 shows the modified resistor values to obtain an improved logarithmic response with smaller logarithmic error.

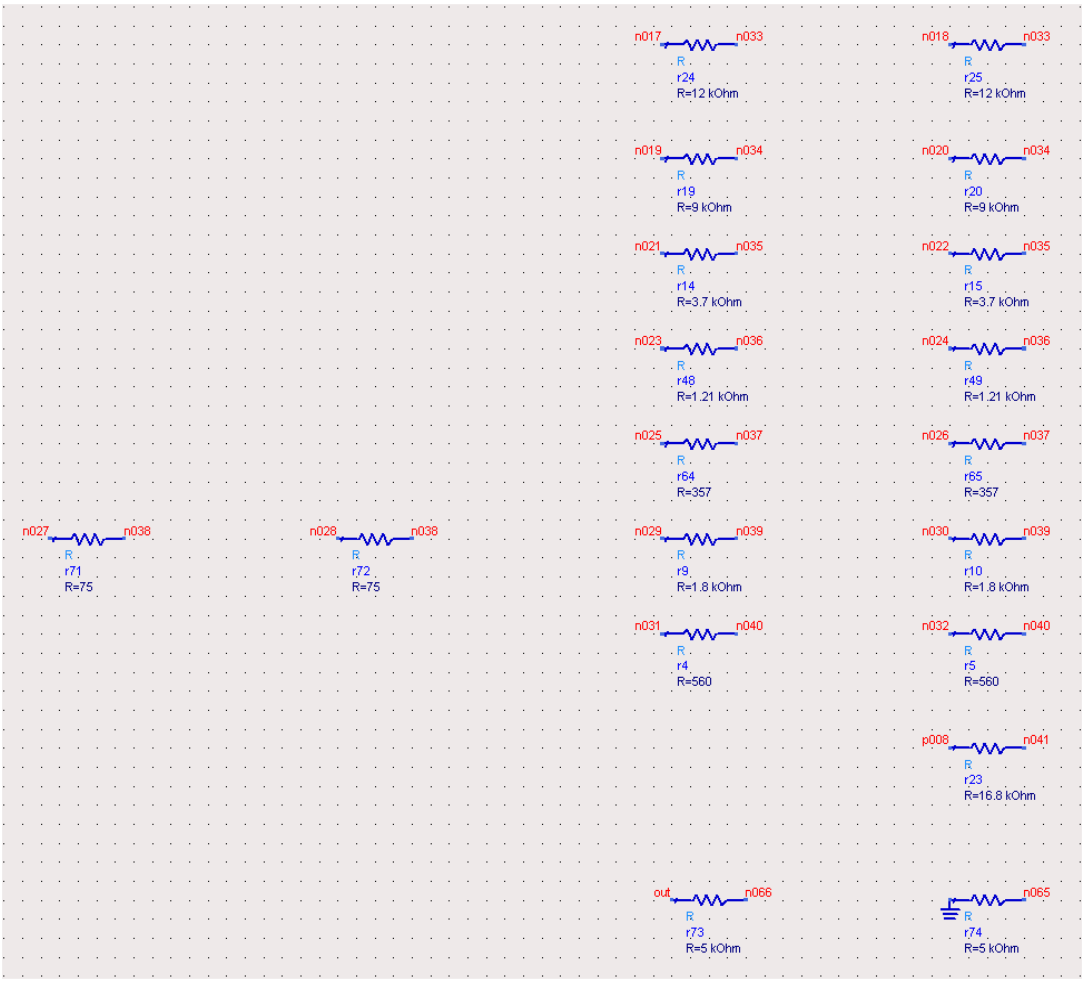

Figure 4-15: Modified resistor values for a better logarithmic response with smaller logarithmic error

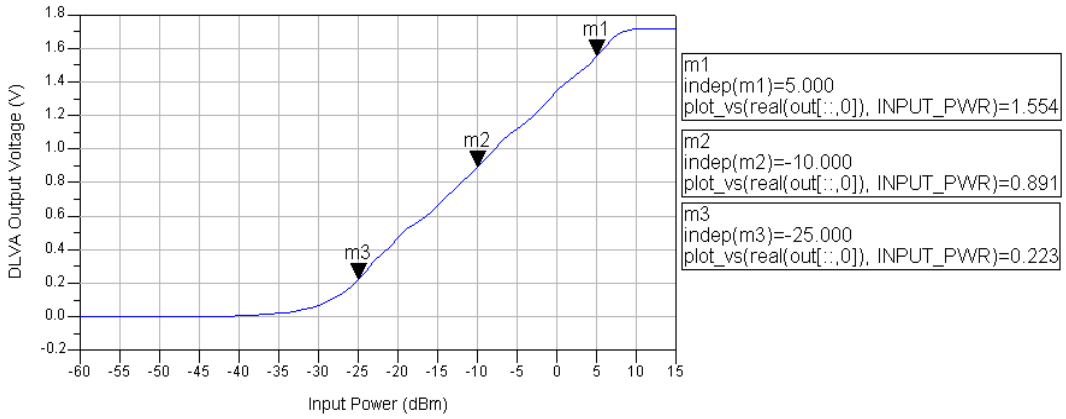

Figure 4-16: The input power-output voltage characteristics of DLVA with modified resistor values at 2GHz

The input power-output voltage characteristics of DLVA observed in Figure 4-16 is superior to the characteristics in Figure 4-13. The slope is nearly the same for both of the detection regions:

$$\frac{1.554 - 0.891}{15} = 44.2mV / dB$$

$$\frac{0.891 - 0.223}{15} = 44.53mV / dB$$

As expected, since the linearity is improved, the logarithmic error is much smaller and much closer to zero in the dynamic range as observed in Figure 4-17.

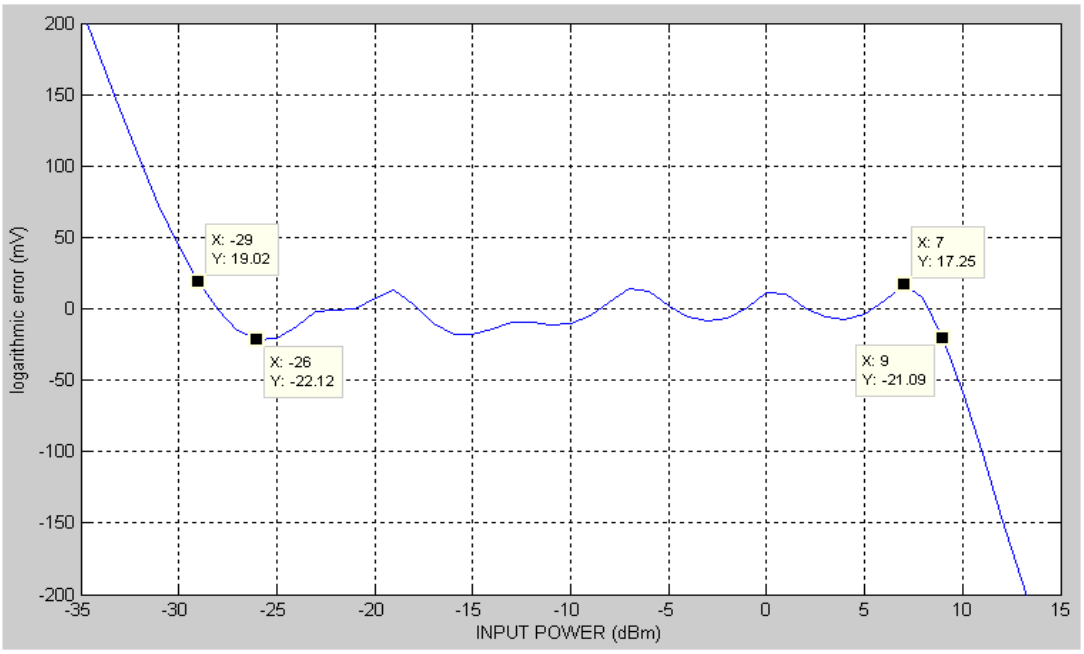

Figure 4-17: The logarithmic error of DLVA with respect to the input power with modified resistor values at 2GHz

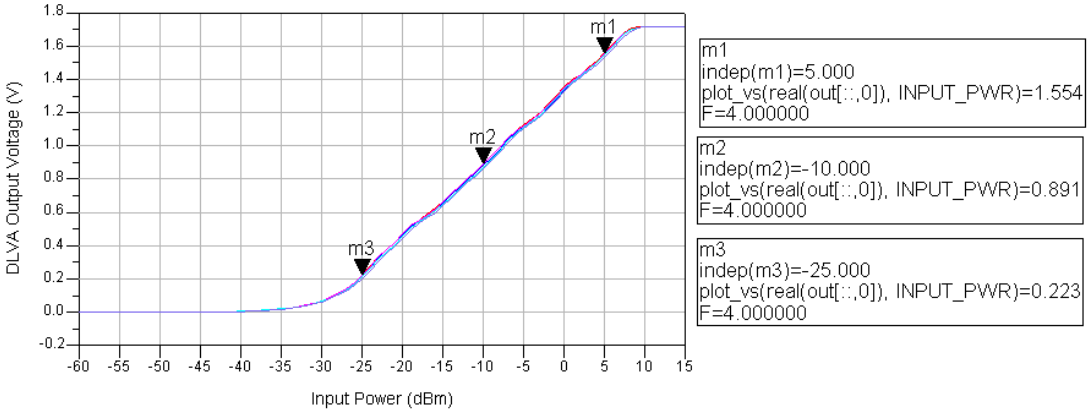

Figure 4-18: The simulated input power-output voltage characteristics of DLVA with modified resistor values in 2-6GHz frequency band

The input power-output voltage characteristics of DLVA with modified resistor values in 2-6GHz frequency band is observed in Figure 4-18. At this stage, a value for frequency flatness tolerance must be defined; a tolerance of 2dB can be

acceptable in the operating frequency band. This characteristic is desired to be independent of the operating frequency; in other words, the frequency flatness must be kept in the tolerance value defined in the operating frequency band. The logarithmic slope is approximately $44mV / dB$.

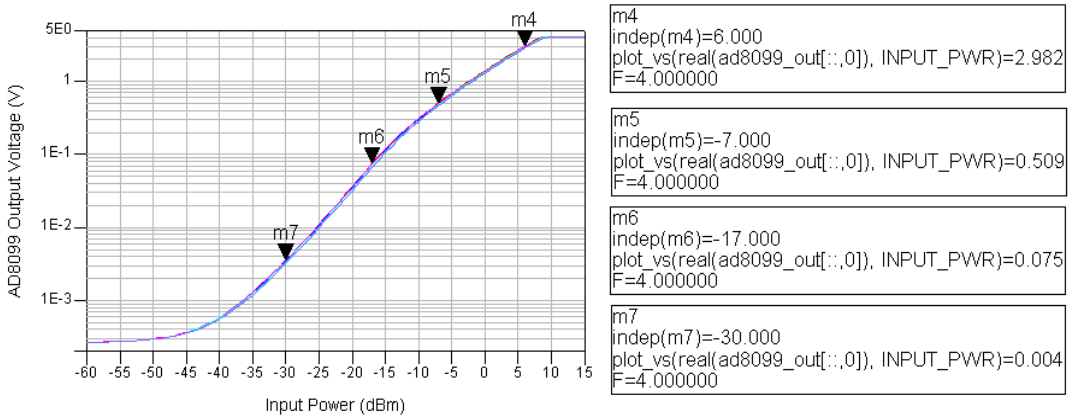

Figure 4-19: The input power-output voltage characteristics at the output of AD8099 in 2-6GHz frequency band

The shift in the input power-output voltage characteristics of DLVA in 2-6GHz frequency band arise from the detector input power-output voltage characteristics as observed from Figure 4-19.

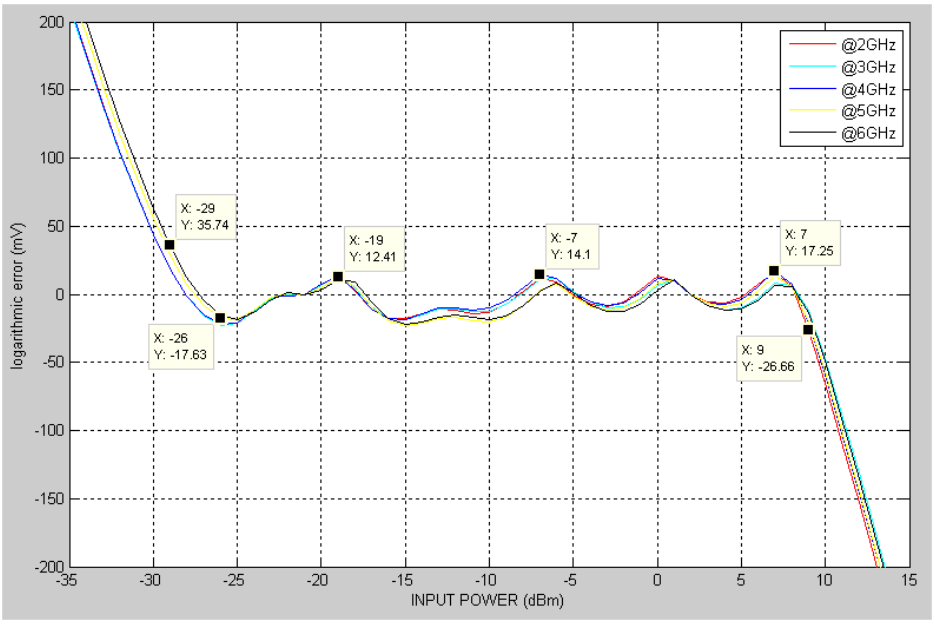

Figure 4-20: The logarithmic error of DLVA with respect to the input power in 2-6GHz frequency band

In the simulations the frequency flatness is preserved with a tolerance of 1dB as seen in Figure 4-20. The logarithmic error is $\pm 40mV$ with a logarithmic slope of $44mV/dB$. The DLVA has a dynamic range of $38dB$ extending from $-29dBm$ to $9dBm$.

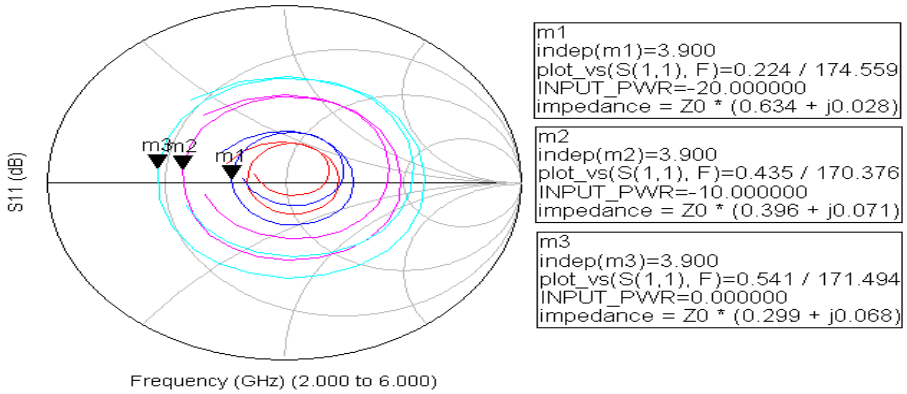

Figure 4-21: S_{11} characteristics of the DLVA at different input power levels in 2-6GHz frequency band in polar plot

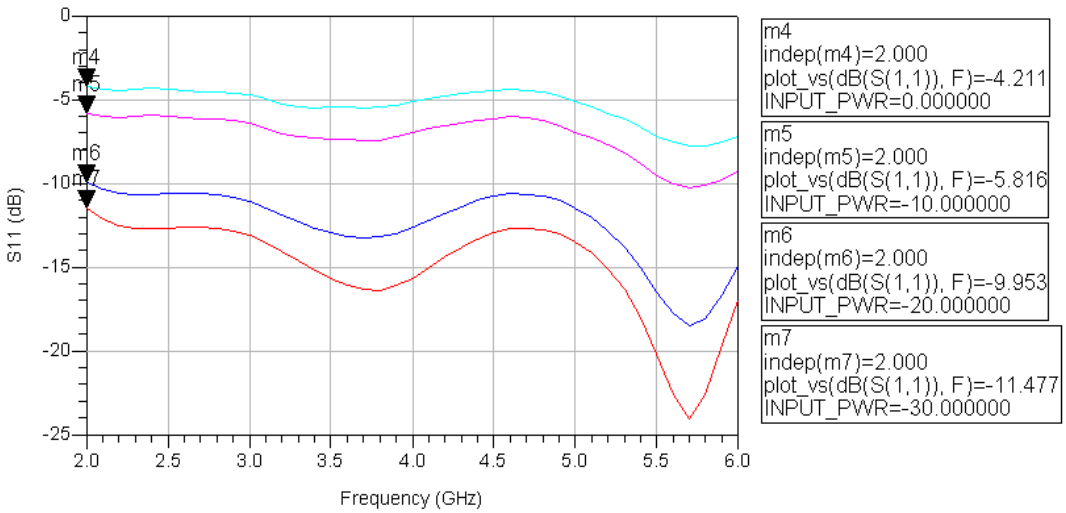

Figure 4-22: S_{11} characteristics of the DLVA at different input power levels in 2-6GHz frequency band

Since the input impedance of the Schottky detector diodes varies with the input RF power level as observed in Figure 4-21, S_{11} characteristics of the DLVA changes with the input RF power levels in 2-6GHz frequency band as observed in Figure 4-22. S_{11} values in the operating frequency band are tried to be kept constant at a specified power level with the help of an RF matching circuitry. S_{11} values for a DLVA can be much higher than any RF structures; an S_{11} value of $-10dB$ is acceptable at an input RF power level of $-20dBm$. The S_{11} values for RF signals with low power are smaller and the S_{11} values for RF signals with high power are worse as predicted.

4.3 Implementation and Measurements

The measurements taken with the modified resistor values in order to maintain linearity with minimum logarithmic error are presented in this section. The consistency between the simulation results and the measurements is examined.

DLVA circuit architecture is given in Figure 4-23. As explained the design is composed of two parts: the diode detector and the logarithmic amplifier. The detector is produced with RO4003 with a metal thickness of $34\mu m$ and substrate thickness of $32mil$ in order to obtain realizable transmission lines in the RF matching section. The DC bias current of the Schottky diodes is supplied from the regulator in the logarithmic amplifier side. Two diode detectors are used to eliminate the video voltage originating from the DC bias current. Despite using two detectors, there occurs an offset voltage of approximately $50mV$ at the output of the detector logarithmic video amplifier making the dynamic range narrower. An additional resistor connected to LMH6725 at the summing stage is used to minimize the offset voltage to approximately $5mV$ and the dynamic range is improved by this way. Since the logarithmic amplifier has video voltage it is not necessary to use RO4003 as substrate; instead, FR4 is used to decrease cost. The logarithmic stages with modified resistor values constitute the logarithmic amplifier as seen in Figure 4-23. The operational amplifier at the output sum the currents obtained from the logarithmic stages.

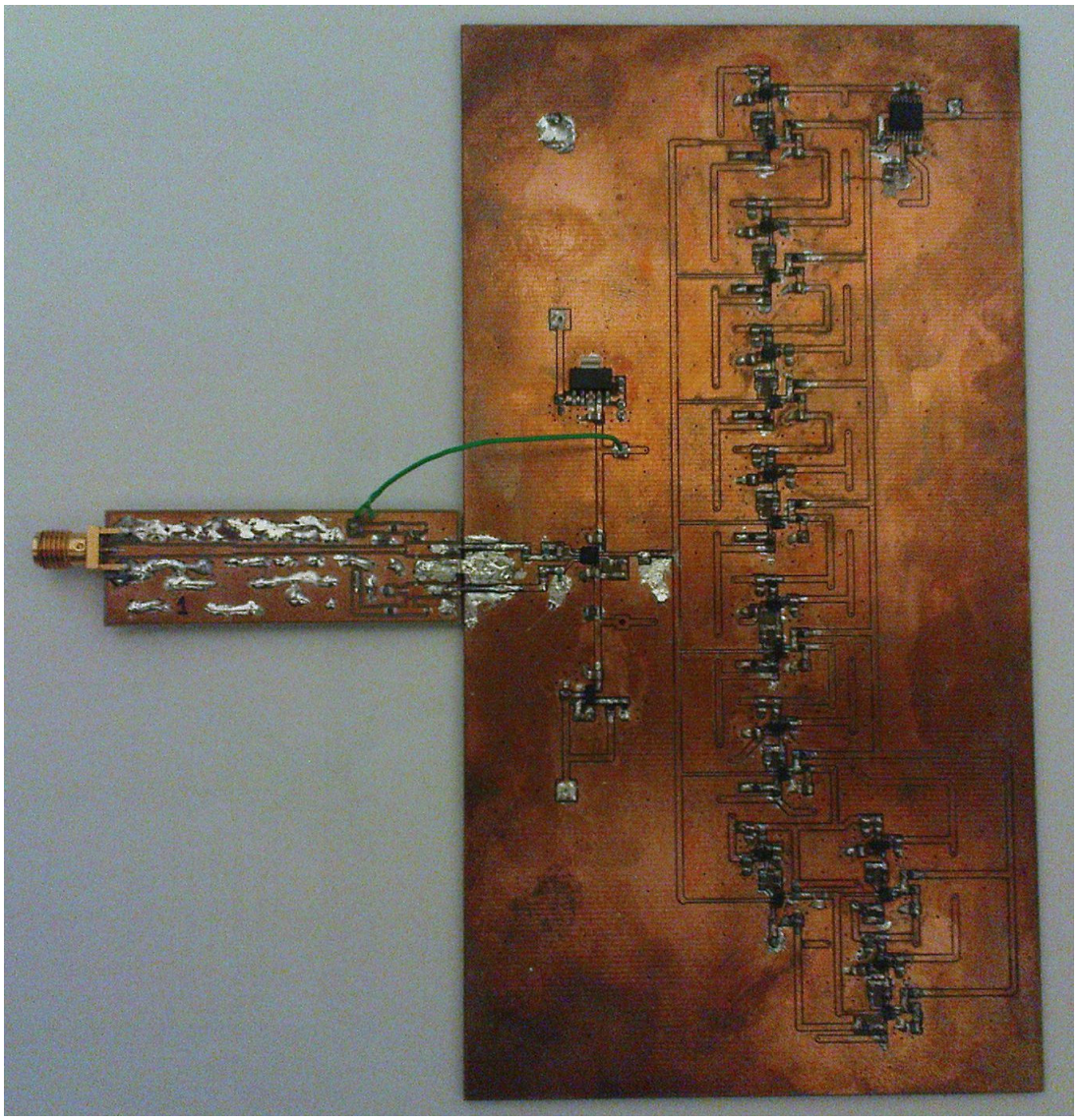

Figure 4-23: DLVA circuit architecture

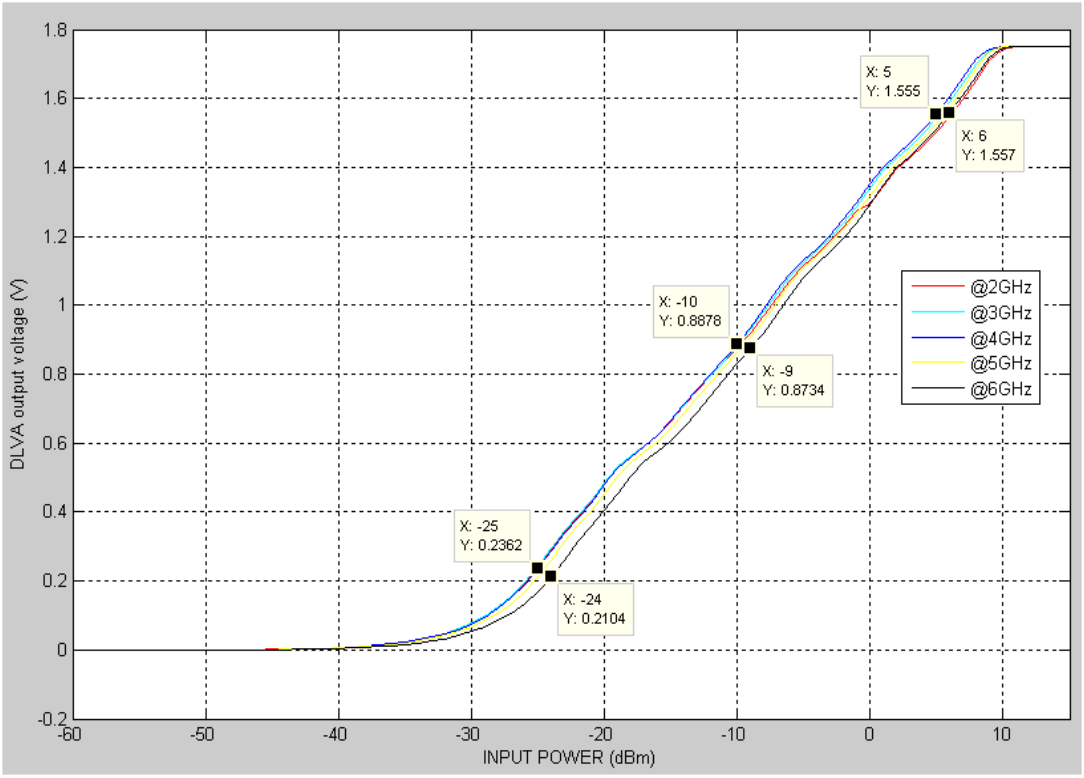

Figure 4-24: The measured input power-output voltage characteristics of DLVA with modified resistor values in 2-6GHz frequency band

The measured characteristic observed in Figure 4-24 is close to the simulation results observed in Figure 4-18 with slight differences in the DLVA output voltages. The important point in Figure 4-24 that must be noticed is the frequency flatness of the DLVA. The markers indicate that the frequency flatness tolerance is approximately $1dBm$; in other words, a power shift of approximately $1dBm$ is necessary to obtain the same output video voltage at the operating frequency band and this is an acceptable tolerance for a DLVA.

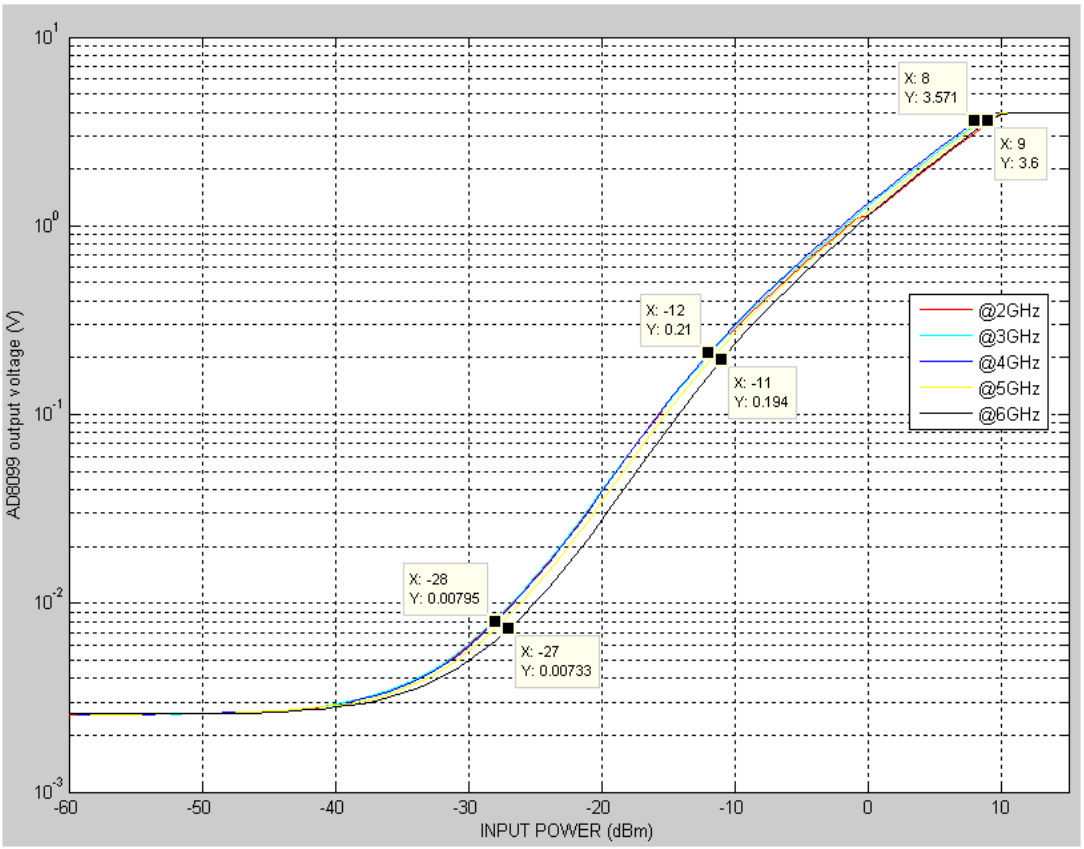

Figure 4-25: The measured input power-output voltage characteristics at the output of AD8099 in 2-6GHz frequency band

The shift in power with changing operating frequency in Figure 4-24 arises from the input power-output voltage characteristics of the Schottky diode detector obtained at the output of the AD8099 as observed in Figure 4-25. The two detection regions with different logarithmic slopes; the square law detection region and the linear detection region, are also seen in Figure 4-25.

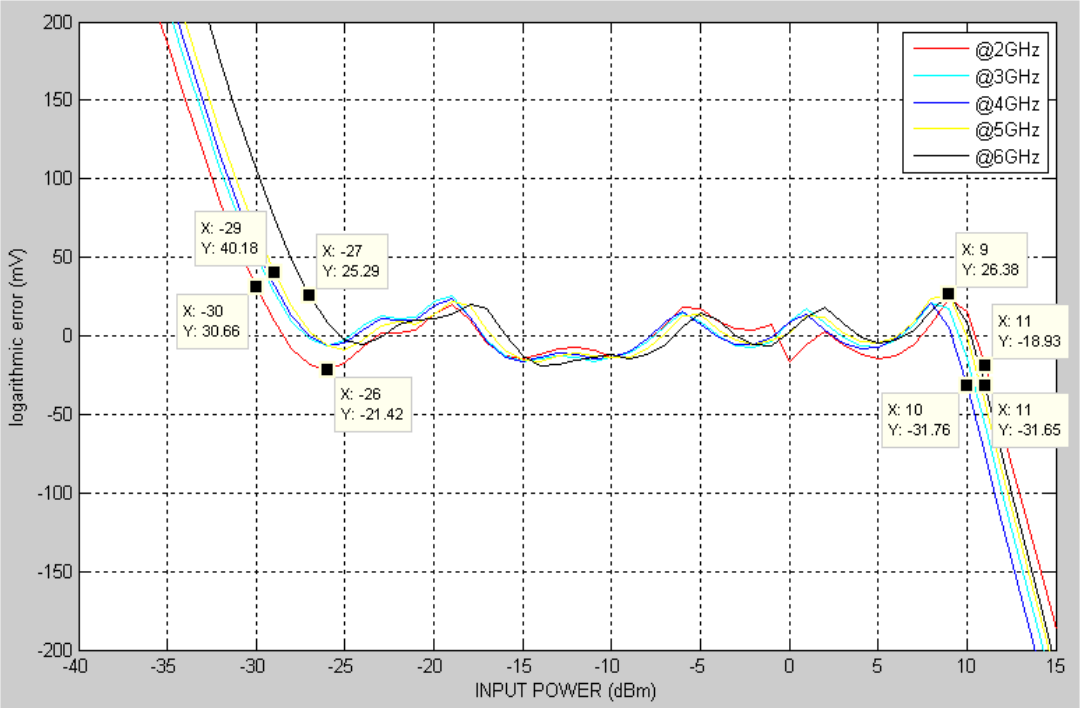

Figure 4-26: The logarithmic error of DLVA with respect to the input power in 2-6GHz frequency band

The logarithmic error determines the dynamic range of the DLVA. The dynamic range varies slightly with respect to the operating frequency as observed in Figure 4-26. The worst results are taken at 6GHz, the logarithmic error is $\pm 30mV$ with a dynamic range of $38dB$ extending from $-27dBm$ to $11dBm$; and the best results are taken at 2GHz, the logarithmic error is $\pm 30mV$ with a dynamic range of $41dB$ extending from $-30dBm$ to $11dBm$.

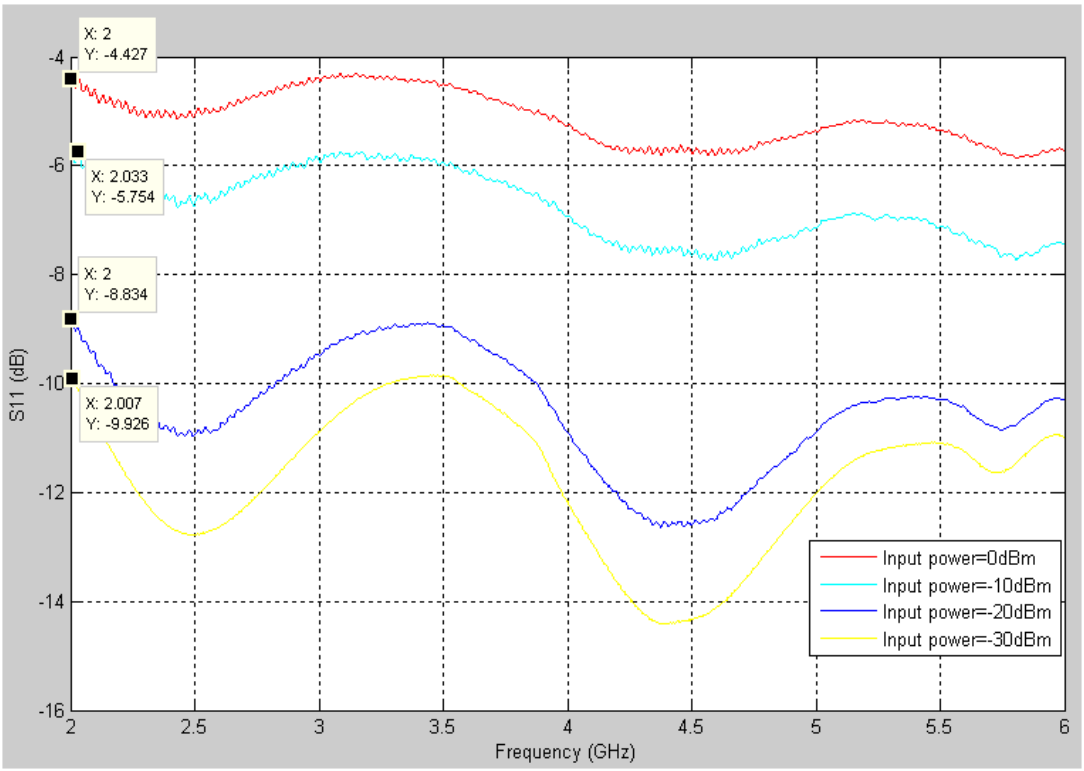

Figure 4-27: S_{11} characteristics of the DLVA at different input power levels in 2-6GHz frequency band

The measured S_{11} characteristics of the DLVA observed in Figure 4-27 shows a great similarity with the simulation results obtained in Figure 4-22 with slight differences in the S_{11} values. S_{11} values for a DLVA can be much higher than any RF structures; an S_{11} value of $-10dB$ is acceptable at an input RF power level of $-20dBm$; an S_{11} value of $-8.8dB$ is obtained at an input RF power level of $-20dBm$ with the measurements. The S_{11} values for RF signals with low power are smaller and the S_{11} values for RF signals with high power are worse as predicted.

CHAPTER 5

CONCLUSION

Detector logarithmic video amplifier is an essential part of many modern radar and electronic warfare systems. Since DLVA is used to convert the power of the RF signals to video voltages, it can be regarded as a logarithmic converter instead of logarithmic amplifier; this conversion makes the process of RF signals with a wide amplitude range possible. Single stage detector logarithmic video amplifiers have a dynamic range dependent on the diode detector. Extended range detector logarithmic video amplifiers can be constructed with required number of single stage detector logarithmic video amplifiers operating in different RF power intervals. DLVA is designed to be independent of frequency and temperature variations. Since the offset voltage at the DLVA output has an obstructive effect on the detection of RF signals with low power, it is minimized to increase the dynamic range and improve sensitivity.

In this thesis work, a detector logarithmic video amplifier is designed and fabricated with a dynamic range of $40dB$ in the 2-6GHz frequency band. The DLVA is supplied with a $\pm 5.3V$ power supply delivering a current of $25mA$ in the lack of an RF signal. The design is composed of two main parts as the video detector and the logarithmic amplifier.

First, the video detector is designed. Since Schottky diodes are used for detection, DC bias currents are used to improve sensitivity and to make matching of the

detector circuit easier by reducing the video resistance of the Schottky diode. In order to eliminate the video voltage resulting from the DC bias two identical diode detectors are used and the output video voltages are connected in a differential manner; this makes the detection of RF signals with low power possible. This differential structure also makes the video voltage independent of temperature variations, because the identical diode detectors are affected in the same way. The RF matching circuitry is designed to obtain minimum S_{11} in the operating frequency band. However, since the detector diode has a high video resistance making RF matching impossible, DC bias current is used to reduce the video resistance of the diode. Since the DC bias current can be increased to a level that does not deteriorate the input power-output voltage characteristics of the diode detector, RF matching is still a challenge; in other words, the priority is at the conservation of the input power-output voltage characteristics of the diode detector, the RF matching is insignificant beside these characteristics. The production processes restricts the design of the RF matching circuitry because of the thickness of the transmission lines being very narrow. Optimum number of transmission line sections is chosen with optimum thickness values.

The video resistance of the detector diode not only depends on the DC bias current, but also the power level of the incoming RF signal. In the design a reference S_{11} value of $-10dB$ is aimed at an incoming RF signal power of $-20dBm$, which is an acceptable value for detector applications and the measurements show that an S_{11} value of $-8.8dB$ is obtained at an RF signal power of $-20dBm$.

Second, the logarithmic amplifier is designed. The logarithmic function is approximated by the summation of the output currents of the differential amplifiers operating as the logarithmic stages. In order to benefit from the whole dynamic range of the diode detector the logarithmic amplifier is composed of two designs: first one is operating in the square law detection region and second one is operating in the linear detection region of the detector. The formulations in Chapter 1 are used to determine the gain of the logarithmic stages and the formulations in Chapter 2 are used to determine the circuit components. Since the slope of the input power-output

voltage characteristics of the diode detector is different for the two detection regions the slopes of the logarithmic stages are adjusted to obtain the desired linear characteristics. However, the measured circuit components may not give the minimum logarithmic error. Some modifications in the circuit components are made to obtain minimum logarithmic error, and a wider dynamic range is obtained by this way. The dynamic range varies slightly with respect to the operating frequency. The worst results are taken at 6GHz, the logarithmic error is $\pm 30mV$ with a dynamic range of $38dB$ extending from $-27dBm$ to $11dBm$; and the best results are taken at 2GHz, the logarithmic error is $\pm 30mV$ with a dynamic range of $41dB$ extending from $-30dBm$ to $11dBm$.

As a future work extended range detector logarithmic video amplifiers can be obtained with single stage detector logarithmic video amplifiers by parallel detection approach.

REFERENCES

[1] P. H. Saul and J. S. Urquhart, "A Broadband GaAs Limiting Amplifier," in Eighth European Solid-State Circuit Conference, pp. 134-136a, Sept. 1982

[2] P. E. Chadwick, "Advances in Logarithmic Amplifiers," in Fifth International Conference on Radio Receivers and Associated Systems, pp. 51-58, 1989

[3] Y. Chuang, K. Cimino, M. Stuenkel, M. Feng, M. Le, and R. Milano, "A Wideband InP DHBT True Logarithmic Amplifier," in IEEE Transactions on Microwave Theory and Techniques, vol. 54, no. 11, pp. 3843-3847, Nov. 2006

[4] A. K. Oki, M. E. Kim, G. M. Gorman, and J. B. Camou, "High-Performance GaAs Heterojunction Bipolar Transistor Logarithmic IF Amplifier," in IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, pp. 41-45, May 1988

[5] Glossary of Terms, DLVAs, ERDLVAs, RF LOG AMPS, LOG Ifs; AKON Inc., San Jose CA, USA, http://www.akoninc.com/gloss_of_terms.php, last access date: Jan. 2011

[6] C. D. Holdenried, J. W. Haslett, J. G. McRory, R. D. Beards, A. J. Bergsma, "A DC–4-GHz True Logarithmic Amplifier: Theory and Implementation," in IEEE Journal of Solid-State Circuits, vol. 37, no. 10, pp. 1290-1299, Oct. 2002

[7] W. L. Barber and E. R. Brown, “A True Logarithmic Amplifier for Radar IF Applications,” in IEEE Journal of Solid-State Circuits, vol. sc-15, no. 3, pp. 291-295, June 1980

[8] A. Woroncow, J. Croney, “A True I.F. Logarithmic Amplifier using Twin-Gain Stages,” in the Radio and Electronic Engineer, pp. 149-155, Sept. 1966

[9] M. A. Smith, “A 0.5 to 4 GHz True Logarithmic Amplifier Utilizing Monolithic GaAs MESFET Technology,” in IEEE Transactions on Microwave Theory and Techniques, vol. 36, no. 12, pp. 1986-1990, Dec. 1988

[10] C. D. Holdenried, J. W. Haslett, “A DC-6 GHz, 50 dB Dynamic Range, SiGe HBT True Logarithmic Amplifier,” in Proc. Int. Circuits Syst. Symp., vol. 4, pp. 289-292, May 2004

[11] B. Gilbert, “Logarithmic Amplifier,” US Patent 4990803, Feb.5, 1991

[12] Z. Yong, C. Lei, Z. Xiao-jun, L. Zong-sheng, “A Parallel-Amplification Parallel-Summation Logarithmic Amplifier for UHF RFID Reader,” in IEEE Eighth International Conference on ASIC, pp. 1121-1124, Oct. 2009

[13] E. Gertel, D. M. Johnson, M. Kumar, “2-18 GHz Logarithmic Amplification Componentry,” in IEEE MTT-S International Microwave Symposium Digest, vol. 3, pp. 1093-1096, May 1990

[14] R. S. Hughes, “Logarithmic Amplification with Application to Radar and EW”, Artech House, Dedham, 1986

[15] N. Scheinberg, R. Michels, “A Monolithic GaAs Low Power L-Band Successive Detection Logarithmic Amplifier,” in IEEE Journal of Solid-State Circuits, vol. 29, no. 2, pp. 151-154, Feb. 1994

[16] L. W. Chua, “A GaAs MMIC for a 2-7 GHz Successive Detection Logarithmic Amplifier,” in IEEE Microwave and Millimeter-Wave Monolithic Circuit Symposiums, pp. 145-148, June 1992

[17] K. Koli, K. Halonen, “A 2.5V Temperature Compensated CMOS Logarithmic Amplifier,” in IEEE Custom Integrated Circuits Conference, pp. 79-82, May 1997

[18] A. S. Sedra, K. C. Smith, “Microelectronic Circuits”, Fifth Edition, Oxford University Press, New York, 2004

[19] LTspice/SwitcherCadIII, Linear Technology, http://www.linear.com/, last access date: Jan. 2011

[20] R. Cory, “Feature Article Schottky Diodes,” Feb 2009, Skyworks Solutions, Inc. http://www.skyworksinc.com/downloads/press_room/published_articles/MPD_022009.pdf, last access date: Jan. 2011

[21] Diode Comparison: Schottky, SPA, Zener, TVS, Littelfuse, Inc., www.littelfuse.com/data/en/Product_Training/PT_DiodeTechnology.ppt, last access date: May 2011

[22] J. F. Chiappetta, “Detector Circuit with Dual-Diode Compensation,” US Patent 4791380, Oct. 9, 1987

[23] Hewlett-Packard Application Note 923, “Schottky Barrier Diode Video Detectors”, 1986

[24] A. M. Cowley, H. O. Sorensen, "Quantitative Comparison of Solid-State Microwave Detectors," in IEEE Transactions on MTT, vol. MTT-14, issue 12, pp. 588-602, Dec. 1966

[25] Advanced Design System (ADS™), Agilent Technologies, www.agilent.com, last access date: Jan. 2011

[26] D. M. Pozar, "Microwave Engineering", Third Edition, John Wiley & Sons, New York, 2005

[27] Microwave Office (MWOffice®), AWR Corp., http://web.awrcorp.com/, last access date: Jan. 2011

[28] CPW Wilkinson Power Divider in ADS, http://uwaverf.altervista.org, last access date: Oct. 2010

[29] AD8099 Data Sheet, Ultra Low Distortion High Speed $0.95nV/\sqrt{Hz}$ Voltage Noise Op Amp, Rev. B, 2004, Analog Devices Inc., Norwood MA, USA

[30] MAX4223-MAX4228 Data Sheet, 1GHz, Low-Power, SOT 23, Current-Feedback Amplifiers with Shutdown, 19-1230; Rev. 2a; 6/97, 1997, Maxim Integrated Products, Sunnyvale CA, USA