A SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER FOR LOW-COST MICROBOLOMETERS

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ABSTRACT

A SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER FOR LOW-COST MICROBOLOMETERS

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Commercialization of infrared (IR) vision is of vital importance for many applications, such as automobile and health care. The main obstacle in front of the further spread of this technology is the high price. The cost reduction is achieved by placing on-chip electronics and diminishing the camera size, where one of the important components is the analog-to-digital converter (ADC). This thesis reports the design of a successive approximation register (SAR) ADC for low-cost microbolometers and its test electronics. Imaging ADCs are optimized only for the specific application in order to achieve the lowest power, yet the highest performance.

The successive approximation architecture is chosen, due to its low-power, small-area nature, high resolution potential, and the achievable speed, as the ADC needs to support a 160x120 imager at a frame rate of 25 frames/sec (fps). The resolution of the ADC is 14-bit at a sampling rate of 700 Ksample/sec (Ksps). The noise level is at the

order of 1.3 LSBs. The true resolution of the ADC is set to be higher than the need of the current low-cost microbolometers, so that it is not the limiting factor for the overall noise specifications. The design is made using a 0.18µm CMOS process, for easy porting of design to the next generation low-cost microbolometers. An optional dual buffer approach is used for improved linearity, a modified, resistive digital-to-analog converter (DAC) is used for enhanced digital correction, and a highly configurable digital controller is designed for on-silicon modification of the device. Also, a secondary 16-bit high performance ADC with the same topology is designed in this thesis. The target of the high resolution ADC is low speed sensors, such as temperature sensors or very small array sizes of infrared sensors. Both of the SAR ADCs are designed without switched capacitor circuits, the operation speed can be minimized as low as DC if an extremely low power operation is required.

A compact test setup is designed and implemented for the ADC. It consists of a custom designed proximity card, an FPGA card, and a PC. The proximity card is designed for high resolution ADC testing and includes all analog utilities such as voltage references, voltage regulators, digital buffers, high resolution DACs for reference generation, voltage buffers, and a very high resolution Δ-Σ DAC for input voltage generation. The proximity card is fabricated and supports automated tests, because many components surrounding the ADC are digitally controllable. The FPGA card is selected as a commercially available card with USB control.

The full chip functionalities and performances of both ADCs are simulated. The complete layouts of both versions are finished and submitted to the foundry. The ADC prototypes consist of more than 7500 transistors including the digital circuitry. The power dissipation of the 16-bit ADC is around 10mW, where the 14-bit device consumes 30mW. Each of the dies is 1mm x 5mm, whereas the active circuits occupy around 0.5mm x 1.5mm silicon area. These chips are the first steps in METU for the realization of the digital-in digital-out low-cost microbolometers and low-cost sensors.

Keywords: Successive approximation register analog-to-digital converters, analog-to-digital converters for imaging applications, resistive digital-to-analog converter

ÖZ

DÜŞÜK MALİYETLİ MİKRO IŞINIMÖLÇERLER İÇİN ARDIŞIK YAKLAŞIKLAMA KAYDEDİCİLİ ANALOG-SAYISAL ÇEVİRİCİ

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Şubat 2012, 96 sayfa

Kızılötesi görüntülemenin ticarileştirilmesi, otomotiv ve sağlık hizmetleri gibi birçok uygulama için hayati önem taşımaktadır. Yüksek fiyatlar bu teknolojisinin daha da yayılmasının önündeki en önemli engeldir. Yonga üzerine kamera elektroniği yerleştirilerek ve kamera boyutu küçültülerek maliyet azaltılabilir ki bu konudaki önemli bileşenlerden birisi de analog-sayısal çevirici (ASÇ)'lerdir. Bu tezde düşük maliyetli mikro ışınımölçerler için ardışık yaklaşıklama kaydedicili (AYK) ASÇ'si ve onun çevresindeki elektronik devreler anlatılmaktadır. Görüntüleme ASÇ'leri, en düşük güç ile en yüksek performansı almak için sadece kullanılacağı uygulamaya özel olarak optimize edilir.

ASÇ'nin 160x120 formatında ve 25 kare/saniye hızındaki bir görüntüleyiciyi desteklemesi gerekmektedir. Düşük güç tüketimi, az yer kaplaması, yüksek çözünürlük potansiyeli olması ve hedef olan uygulamalardan dolayı AYK mimarisi seçilmiştir. 700Ksps hızında 14-bit çözünürlük sağlanmaktadır. Gürültü seviyesi 1.3LSB

civarlarındadır. Çeviricinin gerçek çözünürlük seviyesi, düşük maliyetli mikro ışınımölçerin ihtiyacından daha yüksektir, böylece ASÇ genel gürültü performansında limitleyici bir rol oynamaz. Tasarım, yeni nesil düşük maliyetli mikro ışınımölçerlere uygulanabilmesi için 0.18µm CMOS teknolojisi ile tasarlanmıştır. Daha iyi doğrusallık için isteğe bağlı çift yükselteç yöntemi uygulanmış, daha iyi sayısal düzeltme yapabilmek için değiştirilmiş bir rezistif sayısal-analog çevirici (SAÇ) kullanılmış ve silikon üzerinde yapı değişikliği yapabilmek için, kullanıcı tarafından ayarlanabilen sayısal denetleyici tasarlanmıştır. Ayrıca bu tezde, 16-bit çözünürlüklü ve yüksek performanslı olmak üzere ikinci bir çevirici de tasarlanmıştır. Yüksek performanslı çeviricinin hedefi, sıcaklık sensörleri ya da çok küçük boyutlu kızılötesi dedektör dizileri gibi düşük hızlı sensor uygulamalarıdır. Her iki çevirici de anahtar kapasitör devreleri olmadan tasarlanmıştır ki, böylece gerektiğinde en düşük çalışma frekansı sıfıra kadar inebilir.

Çevirici için kompakt bir test düzeneği tasarlanmış ve üretilmiştir. Bu düzenek, özel tasarlanmış bir yakın çevre kartı, bir FPGA kartı ve bilgisayardan oluşmaktadır. Yakın çevre kartı yüksek çözünürlüklü ASÇ'eri test etmek için tasarlanmıştır. Bu kart, gerilim referansları, gerilim düzenleyiciler, sayısal ara bellekler, referans üretimi için gerekli yüksek çözünürlüklü SAÇ'ler, gerilim yükselteçleri ve çok yüksek çözünürlüklü Δ-Σ SAÇ gibi analog araçları barındırmaktadır. Üretilen yakın çevre kartındaki birçok parça sayısal olarak kontrol edilebildiği için, otomatik testler de bu kart kullanılarak yapılabilir. FPGA kartı olarak, piyasada bulunan USB kontrollü bir kart seçilmiştir.

Her iki yonga da, fonksiyonellik ve performans bakımından tamamen simüle edilmiştir. Yongaların tüm serim işlemleri tamamlanmış, üretim evine gönderilmiştir. Çevirici prototipileri, sayısal denetleyici dahil olmak üzere 7500'den fazla transistordan oluşur. 16 bit çeviricinin güç tüketimi 10mW, 14 bit çeviricinin güç tüketimi ise 30mW'tır. Yongaların her birinin büyüklüğü 1mm x 5mm olup aktif devrenin bulunduğu bölge 0.5mm x 1.5mmdir. Bu yongalar, ODTÜ'de sayısal girişli ve sayısal çıkışlı mikro ışınımölçerlerin ve düşük maliyetli sensorlerin gerçekleştirilmesi için atılan ilk adımdır.

Anahtar kelimeler: ardışık yaklaşıklama kaydedicili analog-sayısal çeviriciler, sayısal-analog çeviriciler, görüntüleme uygulamaları için analog-sayısal çeviriciler

To my family and my lovely wife

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CHAPTER I

INTRODUCTION

IR imaging is a widely used technology in various applications, most of which are relatively large-budget areas such as defense industry and space research. This technology would be very useful in a number of applications from daily life such as automobile navigation and health care. The obstacle for daily use of these imagers is the high price. The transition of IR imaging deeper into daily use will be achieved by decreasing the price. Initial cost reduction is made by using microbolometers instead of photonic devices, to be more specific, low-cost microbolometers. The low-cost microbolometers aim to decrease the process cost of the imager by reducing the mask count for production [1]. Further decrease in the price requires simplifying the peripherals of the microbolometer and lessening the camera size. A significant part of the camera electronics consists of the ADC integrated circuits (IC). Embedding the ADCs into the imager is another step that greatly reduces the camera cost. In order to achieve this goal, there are various studies in the literature [2-9]. Each of the ADCs in these studies is specific to the application. The trade-offs in the imaging ADC design is very different than the general purpose counterparts. The optimization problem must be handled very carefully depending on the priorities. Array format, frame rate, number of outputs, output noise level, pixel linearity, available space, technology node, power budget, display resolution, and application type are the variables of this problem and must be optimized for each application.

This thesis describes the design of a SAR ADC prototype for a 160 x 120 low-cost microbolometer. The ADC consists of a resistive DAC, a dual buffer structure for the input and the DAC, and a precision comparator. Since the prototype is to be tested as a separate die before being embedded into an imager, a highly configurable digital controller and a bias generator are also designed. The digital controller allows fine

tuning of every possible variable in the circuit such as decision time for each bit, delay in between comparator pulses, and comparator pulse lengths. This allows the ADC to be tested on silicon for every scenario. The resistive DAC is optimized for digital correction of errors which arises from process mismatch. Correction requires characterization once before using each die. Once the correction is made, the ADC only has a gain error which is acceptable for imaging systems. Unlike the capacitive DACs used in the literature, the resistive DAC also supports slow conversion down to DC. The dual buffer structure corrects the integral non-linearity (INL) error significantly with an expense of 1.25mW extra power dissipation. The precision comparator architecture is insensitive to process mismatch among transistor minimizing the input offset error. Finally the output is given to the outside world serially minimizing the number of output pads to two.

This chapter briefly provides an insight to the analog-to-digital data conversion and the motives for this study. Section 1.1 introduces the data conversion basics. Section 1.2 explains the performance parameters and their meanings for a better judgment of the following sections. Section 1.3 summarizes the ADC types which are related to this study. Section 1.4 introduces the ADCs used for imaging systems and explains their structures. Section 1.5 briefly explains the low-cost microbolometers at METU and their properties. Section 1.6 explains the motivation and the goals of the design. Finally Section 1.7 explains the research objectives for this thesis.

1.1 Data Conversion

A signal is any value of voltage, current or charge which can be detected. There are two types of signals in electronics: Analog and digital. The analog signals are continuous over the time as well as the amplitude [2]. Figure 1.1 shows an analog signal example. These signals are the electrical representations of the physical quantities. The name “analog” is due to the analogy between the electrical signal and the physical quantity it is representing [3].

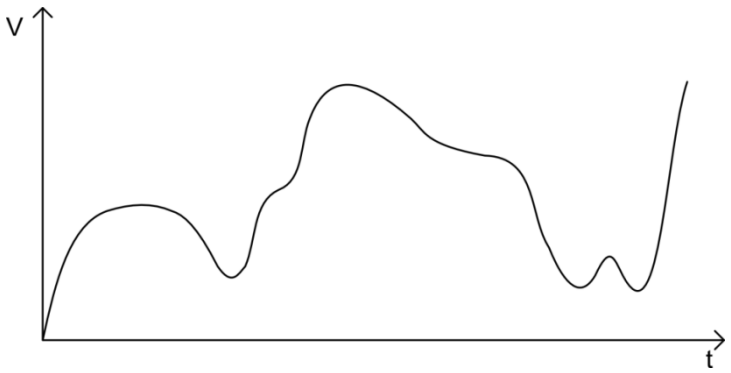

Figure 1.1: An analog signal example. It is continuous over time and amplitude.

Digital signals have discrete values. They are discontinuous over the amplitude [2]. Figure 1.2 illustrates a digital signal with two states (+3.3 V and 0 V). Since these signals have predetermined stable states, they can represent numbers. The binary number system provides the simplest signals and circuits because it has only two values [3]. This number system is widely used due to the simplicity in circuit implementation.

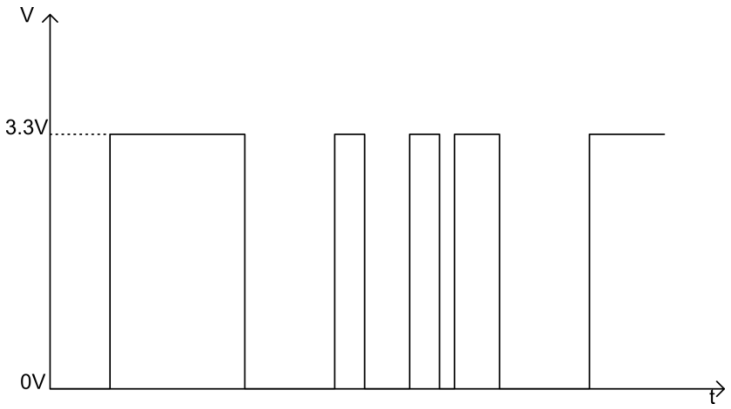

Figure 1.2: A digital signal example. The signal has two predetermined states.

Signal processing can be done both in analog and digital domains. But in some applications, the signal processing capability is only available in either of the digital or the analog circuit. In this case, signals must be converted from analog-to-digital and digital-to-analog. These conversions are made with devices called digital-to-analog converter and analog-to-digital converter.

A DAC generates an analog output with respect to a digital input. There are several architectures in the literature, but the typical operation is conversion of an N-bit digital word into an analog value at the output [3]. Figure 1.3 shows the circuit representation of the DAC. The output of a DAC is not a typical analog signal as in the previously mentioned definition. Since the digital input is discrete, the analog output has a quantization error. The quantization error arises from the finite resolution. The highest error of an ideal DAC output, in comparison to a real analog signal, is half of one least significant bit (LSB). Figure 1.4 shows the analog output and the quantization error of a 3-bit ideal DAC. The output waveform can be smoother if it is fed to a low-pass filter and the higher order components are filtered [3].

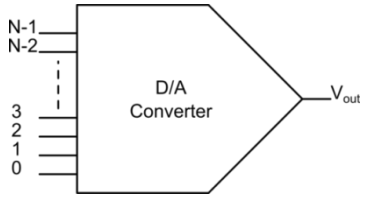

Figure 1.3: The circuit representation of a digital-to-analog converter.

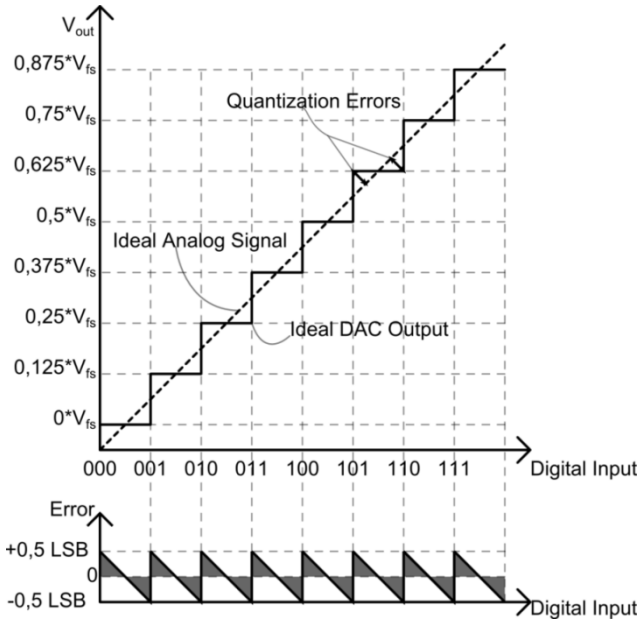

Figure 1.4: The DAC output is given as fractions of the full scale voltage. The quantization error is given as fractions of LSB.

An ADC generates an N-bit digital output according to an analog input signal. Figure 1.5 shows the circuit representation of the ADC. It makes the mapping process of the analog signal amplitude to the digital numbers. The total range of the analog input signal is divided into the number of the available digital codes. Each digital number is mapped to a finite range of the analog signal. The quantization error occurs due to the finite number of the digital output codes. Figure 1.6 shows the mapping scheme and the quantization error of an ADC. As the resolution increases, a finer mapping can be done and the quantization error decreases. As a result, the resolution is an important property of ADCs as well as of DACs. There are other performance parameters of an ADC as well. These are mentioned in the next section.

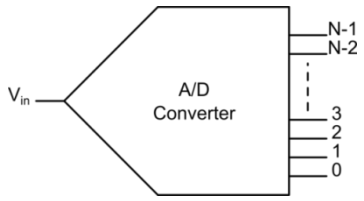

Figure 1.5: The circuit representation of an analog-to-digital converter.

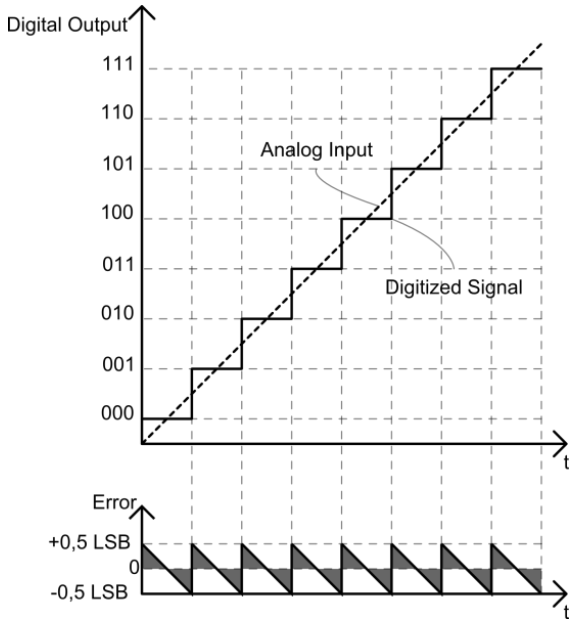

Figure 1.6: The digitized output and analog input is given on the top graph. The quantization error is given as fractions of LSB.

1.2 Performance Parameters

A large set of performance parameters are available in the literature [4]. In this section, static performance parameters of ADCs and DACs are explained to provide clarity for the next sections.

- Offset Error: Vertical shift of the line connecting the endpoints [5].
- Gain Error: Gain difference between the actual and the ideal input-output characteristics [4]. It is observed as deviation from the ideal line connecting the endpoints [5].
- INL: Integral nonlinearity is the maximum deviation of the output from the straight line connecting two endpoints of the output curve [5].
- DNL: Differential nonlinearity is the largest difference of step size in between two adjacent levels divided by one LSB [4]. This can be observed as the largest deviation of step size from one LSB in the input axis at the input-output characteristics graph [5].

Figure 1.7 shows the error types.

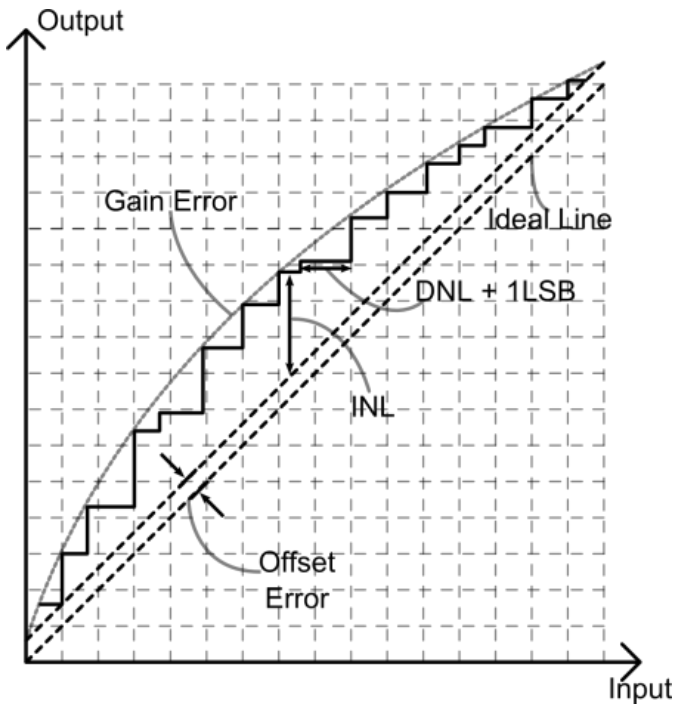

Figure 1.7: The error types of a data conversion system.

1.3 ADC Types

There are two major groups of ADCs based on the working principle: Oversampling and Nyquist-Rate ADCs. According to the nyquist theorem, the frequency of the input signal must be at least half of the sampling frequency, in order to prevent aliasing. Nyquist-Rate ADCs can handle input signal frequencies around up to half of the sampling rate. Oversampling ADCs require much lower input signal frequencies to prevent aliasing. In this section, a brief overview of Nyquist-Rate ADC architectures is given. The architectures are selected with respect to the relevance to this study.

1.3.1 Serial ADCs

The search algorithm of the serial ADCs is basically sweeping the full scale range step by step until the input voltage level is found. The single slope ADCs are the simplest actuation of this method. Figure 1.8 shows the topology of the serial ADC.

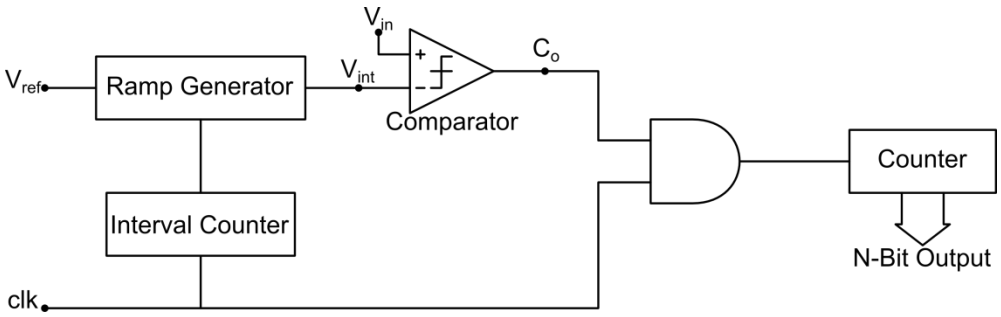

Figure 1.8: The single slope ADC structure.

At the beginning of the conversion, the input voltage is sampled and held. The sampled voltage is connected to the positive terminal of the comparator during the entire conversion. The ramp generator is reset by the interval counter. The output of the ramp generator is initially set to the lowest voltage level that the comparator can operate with. This is the threshold voltage of the comparator. As the clock signal is given to the ADC, the ramp generator starts integrating the reference voltage. The output of the

ramp generator is connected to the negative terminal of the comparator. The comparator output remains high until V_{int} reaches the input voltage value, then the comparator output goes to low and the conversion is finished. While the comparator output is high, the counter at the output counts up with each clock cycle. At the end of the conversion, the output of the counter is a binary number representing the input voltage. Figure 1.9 shows the operation scheme of the single slope ADC.

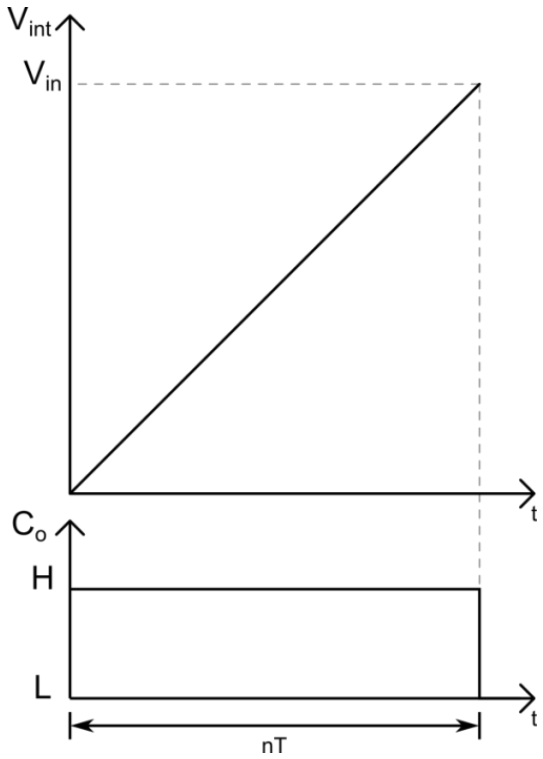

Figure 1.9: The voltage of V_{int} node is given while single slope operation. T is the clock period while n is the counter output.

The main advantage of the single slope ADC is the simplicity of operation. The disadvantage is the slow conversion. This architecture has a worst-case conversion time of $(2^N)xT$. It is also very sensitive to any error in the ramp generation. The ramp sensitivity problem of the single slope ADC is solved with the dual slope architecture. Figure 1.10 shows the structure of the dual slope ADC.

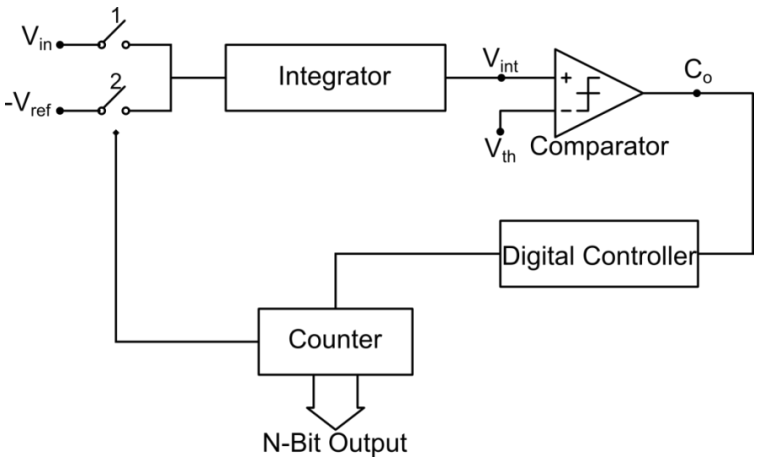

Figure 1.10: The dual slope ADC structure.

In this architecture, the input voltage is connected to the integrator for a fixed duration T_{fix}. This charges the positive input node of the comparator to a voltage level depending on the input voltage. Then the reference voltage is connected to the integrator. The reference voltage must have the opposite polarity of the input voltage, so V_{int} decreases back to the initial value. Figure 1.11 shows the operation of the dual slope ADC.

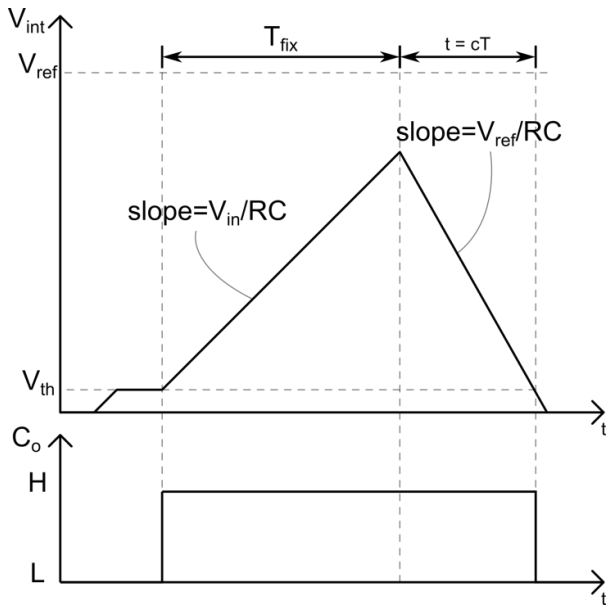

Figure 1.11: The dual slope ADC operation. The ramp generator output is first reset to V_{th} of the comparator then rises up with V_{in}/RC and falls back with V_{ref}/RC.

The time elapsed, from the connection of the negative reference ($-V_{ref}$) until the drop of the comparator output, equals to cT where *c* is the counter output and *T* is the clock period. The input voltage is calculated as

$$\frac{V_{in}}{RC} \times T_{fix} = \frac{V_{ref}}{RC} \times cT \tag{1.3.1.1}$$

Simplifying Equation (1.3.1.1)

$$V_{in} = \frac{V_{ref} \times cT}{T_{fix}} \tag{1.3.1.2}$$

Both up-ramp and down-ramp are generated by the same integrator. This resolves the dependence of the ADC to the ramp generation. Also, a careful selection of the input integration time T_{fix} may suppress the desired noise frequencies [6]. As a result, a higher resolution can be gained with a dual-slope topology. But it has a maximum conversion time of $2(2^N)$xT, where *N* is the number of bits and *T* is the clock period. The serial ADCs generally have a high resolution and a low conversion speed. The two ADCs in this section represent the typical properties and operation of serial ADCs.

1.3.2 Flash ADC

The flash ADC has the highest speed potential among all ADC types. All-parallel architecture, the absence of internal D/A conversions and analog operations are the key properties for extremely high speed. An N-bit flash ADC converter consists of 2^N resistors and 2^N-1 comparators. Figure 1.12 shows the structure of a flash converter. Each comparator has a reference generated by the resistor ladder. Reference voltages of adjacent comparators differ by 1 LSB. Hence, all quantized levels are compared to the input voltage. The comparator output is translated to an N-bit normal binary number by the encoder. The result of the comparison is available after one comparator delay and some gate delays from the encoder. However, the flash ADC also has some drawbacks. The resolution is limited because of the high number of resistors and the comparators. The area as well as the power dissipation is exponentially dependent on the resolution. As the area grows, the production cost of each part rises.

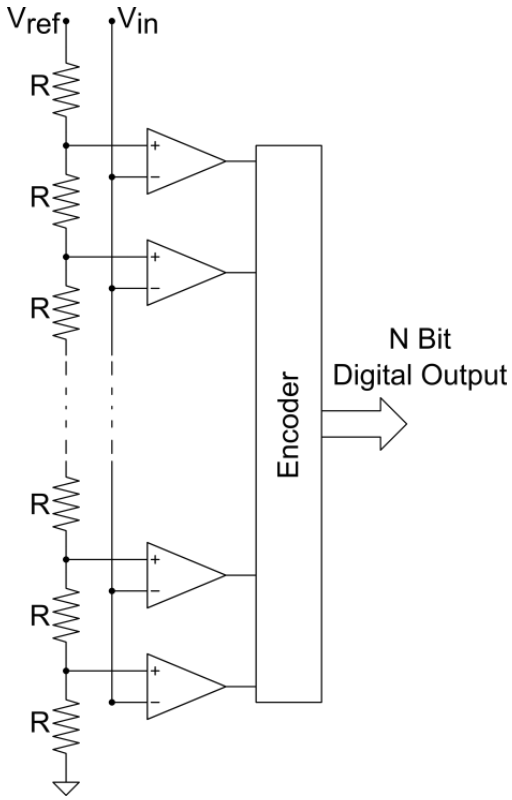

Figure 1.12: An N-bit flash ADC structure is given.

1.3.3 Subranging ADC

The subranging ADCs are an alternative to flash ADCs for medium resolution yet still fairly high speed operations. This is due to the smaller size and lower power dissipation [7]. The two step conversion technique is the key for those features. The conversion in a subranging ADC consists of a coarse step and a fine step. Figure 1.13 shows the structure of a simple subranging ADC. After the input signal is sampled and held, an N_c-bit coarse conversion is made and the result is stored in a latch. The N_c-bit output of the first conversion is also connected to a DAC of the same resolution. A roughly quantized version of the input signal is generated by the DAC. The DAC output is subtracted from the input voltage and the residue is amplified. This operation must be adjusted so that the output voltage range exactly fits to the input range of the N_f-bit fine A/D converter [6].

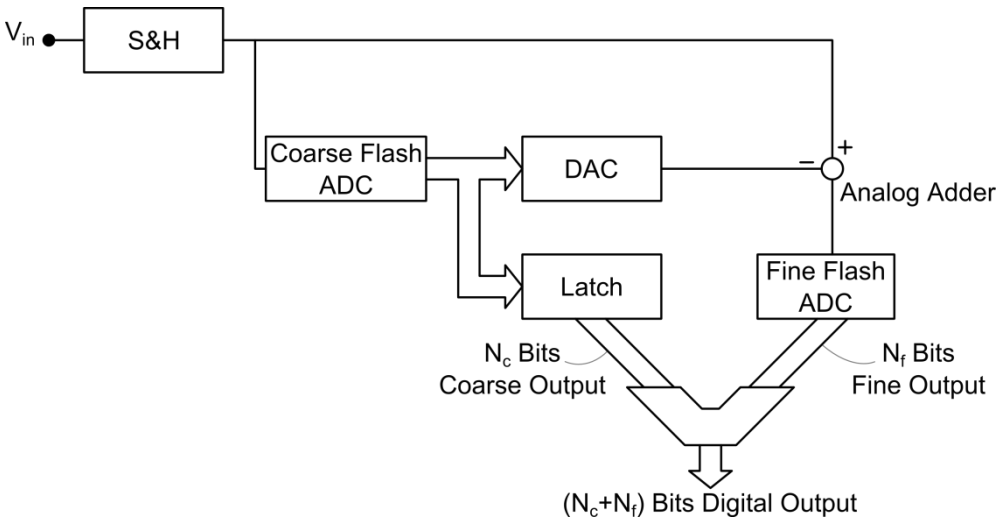

Figure 1.13: The subranging ADC structure.

The amplified residue is converted to digital by the fine conversion stage. The overall output of the subranging ADC is obtained by concatenating the coarse output as most significant bits and the fine conversion results as least significant bits.

The topology used enables A/D conversion with much less comparator than flash architecture. A subranging ADC requires $(2^{1+(N/2)} - 1)$ comparators where a flash ADC requires 2^N comparators where *N* is the bit resolution. Since each comparator occupies silicon area and dissipates power, the subranging ADCs have great advantage on lower power dissipation and smaller area which means lower cost. The drawback is the speed difference. A subranging ADC can achieve half the speed of a flash ADC with the same clock frequency due to the two step delay between two conversions.

1.3.4 Pipeline ADC

The pipelining concept is used to increase the speed in multi stage A/D converters. The specialty of this concept is the operation of all stages at the same time. As each stage operates concurrently, conversion delay is limited with the delay of one stage.

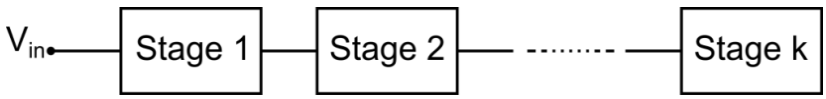

Figure 1.14: The pipeline ADC structure.

The pipeline ADC consists of a number of cascaded conversion stages. Figure 1.14 shows the structure of a typical pipeline ADC. Each of the stages has its own track and hold circuit. As a result, all stages can operate simultaneously. Figure 1.15 shows the structure of a single stage. The held data at the track and hold block of a stage is converted to digital data by an m-bit ADC.

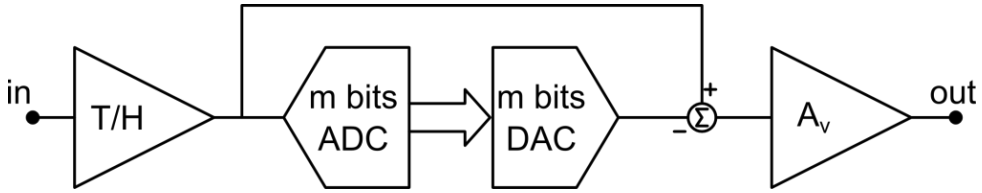

Figure 1.15: The structure of a pipeline ADC stage.

The digital output is converted to a quantized analog signal by a DAC. The quantized voltage is subtracted from the input signal and the residue is amplified and applied to the input of the next stage. This sequence is repeated in each stage until conversion is complete. The signaling of track and hold circuit is important for realizing concurrent operation. Figure 1.16 shows the track and hold signals of a four stage pipeline ADC.

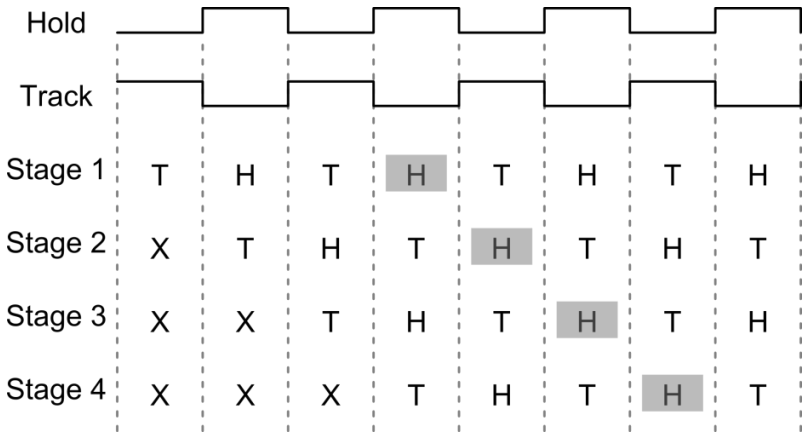

Figure 1.16: The signaling scheme of the stages in a pipeline ADC. The pipeline ADC has four stages. The propagation of data is shown with gray shades.

The stages, which are processing the data, are in hold mode, while the outputs of those blocks are tracked by the next stages. The analog input passes to the next stage with each clock cycle. The time difference, between the sampling of an analog input and generation of digital output, is called pipeline delay. The pipeline delay is decided by the number of stages.

1.3.5 Successive Approximation Register ADC

The successive approximation register ADC (SAR ADC) is a highly recycling converter type. Figure 1.17 shows the simplest configuration of a SAR ADC. It consists of a sample and hold (S&H) circuit, a DAC, a comparator, and a successive approximation register.

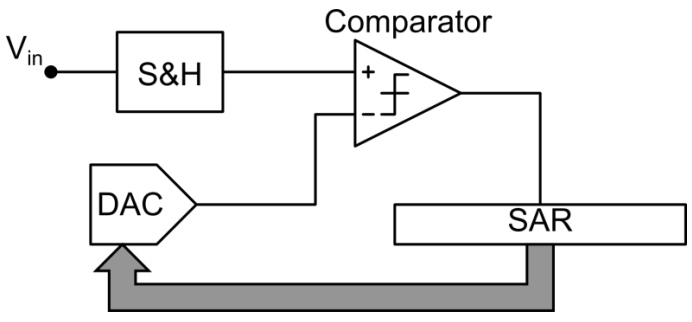

Figure 1.17: The simplest successive approximation register ADC structure.

The typical SAR ADC performs a binary search algorithm in analog domain. The DAC output is set to the middle of the full scale at the beginning of the conversion. The comparator output indicates if the input voltage is greater or smaller than the DAC output. The SAR output is refreshed; therefore the DAC output is updated according to the comparator result. If V_{in} is larger, the DAC generates a voltage which corresponds to the middle point of the upper half of the previous try. If V_{in} is smaller, the search continues to the lower half. The operation is repeated until all bits in the SAR are decided. Figure 1.18 shows the binary search scheme.

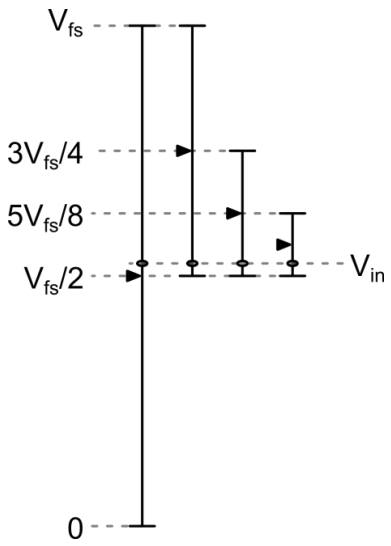

Figure 1.18: The binary search algorithm of the SAR ADC.

For the binary search algorithm an N-bit conversion takes N steps. However, the conversion time does not scale linearly as the resolution is changed. The increase in resolution results in significantly longer settling times and much bigger capacitances for bandwidth limitation of internal components. Hence, doubling up the resolution does not lead to half of the conversion speed but much lower.

Since the SAR ADC has very few components in comparison to other topologies, it is a low power and small area converter. High speed conversion cannot be done especially at high resolutions due to the iterative nature of the device. Low power and small area

are attractive properties for some applications where high speed is not the primary concern.

1.4 Analog-to-Digital Converters for Imaging Applications

The charge coupled device (CCD) imagers have the pixels and the camera electronics in different substrates. Consequently, the image sensor needs external electronics for analog operations and analog-to-digital conversion. The pixel information suffers from noise coupling due to off chip communication in the analog domain [8].

The first camera-on-chip idea was brought up by Fossum [9]. The CMOS image sensors have the needed capabilities for reaching this goal. The CMOS was originally a circuit implementation process rather than imaging. Therefore, the CMOS image sensors enable the designers to integrate the necessary electronics into the sensor.

For realizing the camera-on-chip, completely digital imaging sensors are needed. The analog inputs can be eliminated by generating all references internally. On chip analog-to-digital conversion is necessary in order to dismiss the analog outputs. The internal ADCs must be optimized according to the sensor properties. The frame rate and the array format directly affect the resolution and the sampling rate of the ADC [10]. The resolution must be at least 8-bit to have a smooth image on a display because the RGB color code in pixels of a display requires 8 bits for each color. The INL and DNL values of the ADC must be below 8-bit resolution as well. Otherwise, the defects will be observed on the image. Power consumption of the ADC is another important property, especially for infrared imaging. Excessive heating of the ADCs can cause hot spots on the image. It also shortens the battery life in mobile applications. The area of the ADC is as crucial as power, resolution, and speed. If the circuit occupies too much silicon area, the cost of the sensor increases. This is against the low-cost philosophy of the on-chip integration.

The choice of the ADC topology depends on the image sensor specifications. Small arrays with low-medium frame rates have one ADC for the entire array. The conversion is done serially for each pixel. For bigger arrays, semi-parallel architectures are

preferred [11]. The pixel array is partitioned into sufficient number of strips. Each strip has its own ADC. The ADCs operate in parallel, but each pixel in the strip is converted serially. This method decreases the effective array size for each ADC.

The parallel use of ADCs increase further, as the array size grows or the frame rate increases. The column parallel ADCs are used for large arrays with high frame rates [12] [13]. In this method, ADCs are stacked above the pixel array. Figure 1.19 shows the floor plan of a column parallel structure. Each ADC lies along the axis of corresponding pixel, fitting the pixel pitch. This is a challenge if the pixel pitch is small. The layout limitations must be considered from the beginning of the circuit design.

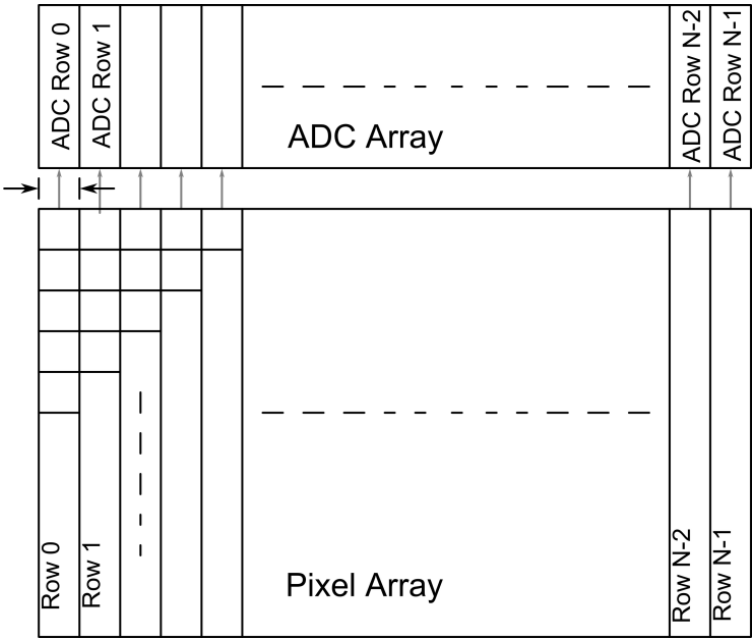

Figure 1.19: The floor plan of a column parallel ADC in a CMOS imager. Each ADC column is drawn according to the pixel pitch.

The highly parallel structure of this method relaxes the ADC speed limit for each column. As the speed is decreased, simpler designs become feasible. A low-to-medium speed ADC can be used, such as successive approximation, single slope or sigma-delta ADCs. Although speed limitations are decreased, power consumption may be a

problem. Each column ADC must be very low power because the overall power dissipation is the sum of all parallel ADCs' dissipation. Beyond using low-power topologies, some designers use the transistors in the sub-threshold region for decreasing the power consumption [14].

The pixel-level conversion is the most parallel way for A/D conversion in CMOS image sensors. The ADCs are either shared by a few neighbor pixels or each ADC is devoted to one pixel [15] [16]. Placing the ADC inside the pixels is a challenging task. The structure of the converter must very simple and compact so it fits into the pixel area. Fortunately pixel-level ADCs have extremely low sampling rates; quite simple architectures provide sufficient performance [17]. Since the analog value is converted to digital numbers right at the pixel, noise coupling to the pixel value is greatly reduced. The pixel-level conversion can achieve very high signal-to-noise ratio (SNR) [14].

The imaging ADCs are not typical general purpose converters. They are application specific devices. The operation scheme may differ from general purpose counter parts as well as the design concerns. The noise characteristic of a CMOS imager is different than that of a typical electronic circuit which does not include photon (shot) noise. The noise level of a pixel voltage in an image sensor is proportional to $\sqrt{N}$ where N is the photon count. High photon count leads to a large noise while increasing the signal amplitude. Figure 1.20 shows the noise characteristic of an imager.

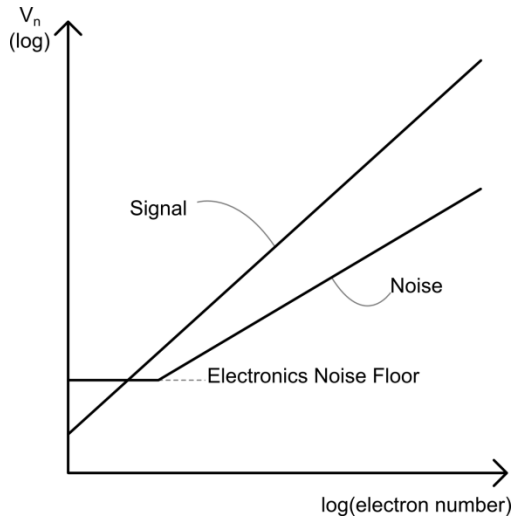

Figure 1.20: The analog output of pixel voltage versus illumination light intensity [11]. The noise increases with square root of the signal after the electronics noise floor.

As the electron count is increasing, the noise is rising too. Although the SNR is getting better, the least significant bits of the ADC range is flooded by noise. In order to take advantage of this physical phenomena, special ADCs are developed which can decide if the signal is noisy or not. The ADCs shortens the conversion time instead of converting useless noise data [11].

Image process made on the digital output is also important, in order to lighten the ADC specifications. Some defects such as static offset and nonlinearity may be corrected to some extend by image processing.

In conclusion, the imaging ADCs differ significantly from the general purpose converters. On the contrary of commercial converters, the input signal, input noise, and post-processing of converted data is well defined. This advantage is used for decreasing the power, increasing the speed and simplifying the design.

1.5 Low-Cost Microbolometers at METU

Microbolometers typically include different fabrication methods for producing the readout and the detector. Post-CMOS process steps lead to an increase in the price of

each die. The low-cost microbolometer studies aim to eliminate the critical process steps after CMOS fabrication. The studies on low-cost microbolometers in METU start in 1997. Since then 16x16, 64x64, 128x128 and recently 160x120 arrays are produced. Performance has been thriving from detecting a hot solder to observing humans in the view. The most recent microbolometer has a pixel pitch of 70µm. The system noise level is $5.4mV_{rms}$ where the noise of the camera electronics is measured to be $0.53mV_{rms}$. The microbolometer has one analog video output [1].

1.6 Motivation for the Custom Design SAR ADC

The ADC designed in the scope of this study, is to be used in mobile sensor applications. The battery life time has crucial importance in battery powered applications. In order to achieve long battery life, low power consumption is the main goal that must be achieved. The successive approximation register analog-to-digital converter topology is selected because of its low power operation potential, reasonable operating speed for those applications, and high resolution. Furthermore, due to small number of building blocks, SAR ADC does not significantly increase the silicon area when it is integrated into the sensor. This is an important property for preserving the low-cost property of the sensor. Other previously mentioned topologies are either too slow (Serial ADCs) or they consume too much power at necessary resolution (Flash,Subranging and Pipeline ADCs).

Using the commercially available ADC chips is not an optimum solution for low-cost sensor applications. There are three main disadvantages of using ready chips. First of all, commercial ADCs are relatively expensive components. The low-cost sensors aim to cost a few dollars per die, but this effort is senseless if tens of dollars are paid for good performance ADCs. Secondly, the amount of electronics and the PCB size around the sensor affects the price of the final sensor solutions. Furthermore, many chips around the main sensor increases the PCB size and this becomes the limiting factor for compact products. The commercial ADCs have many pins which requires traces, external components and results in larger cards. Thirdly, the mobile applications require very low-power ADCs in order to have long battery life. There are low-power commercial

ADCs available in the market, but these ADCs have to be ideal-like and support every application. However the power consumption can be decreased even further by taking advantage of the characteristics of the specific application. For example, imaging sensors are not effected from minor gain errors if it is less than that of the pixel structure and this can be used for decreasing the power consumption. All of those disadvantages force the sensor producers to design their own application specific ADCs. An application specific, low-power ADC integrated into the sensor significantly decreases the size of the final package, the overall power consumption and the overall cost.

Another goal of this thesis study was the disposal of the minimum sampling rate requirement of the ADC. There are various SAR ADCs designed for CMOS imaging available in the literature. All of those ADCs accomodate a capacitive DAC especially at high resolutions such as 14-bit or 16-bit. The switched capacitor DACs have a limitation of a minimum operating frequency due to leakage currents.

1.7 Research Objectives and Thesis Organization

The main objective of this thesis is to develop a low-power, low noise, and high resolution SAR ADC prototype for low-cost microbolometers. The prototype is to have least number of pads in order to diminish the size of the PCB used for electronics. Two versions of the SAR ADC are designed with different sampling rate and resolution. The first one is the 16-bit 128Ksps ADC. It is a high performance converter for slow but accurate conversion. It is designed to digitize the output of slow sensors such as temperature sensors or detection-purpose infrared sensors. The second ADC has a resolution of 14-bit at a speed of 700Ksps. It is designed for digitizing the analog output of a QQVGA (160x120) low-cost microbolometer. Initially, the SAR ADC chip will be used as a standalone ADC on the PCB, then it will be integrated into the microbolometer. Figure 1.21 shows the microbolometer with on-chip SAR ADC.

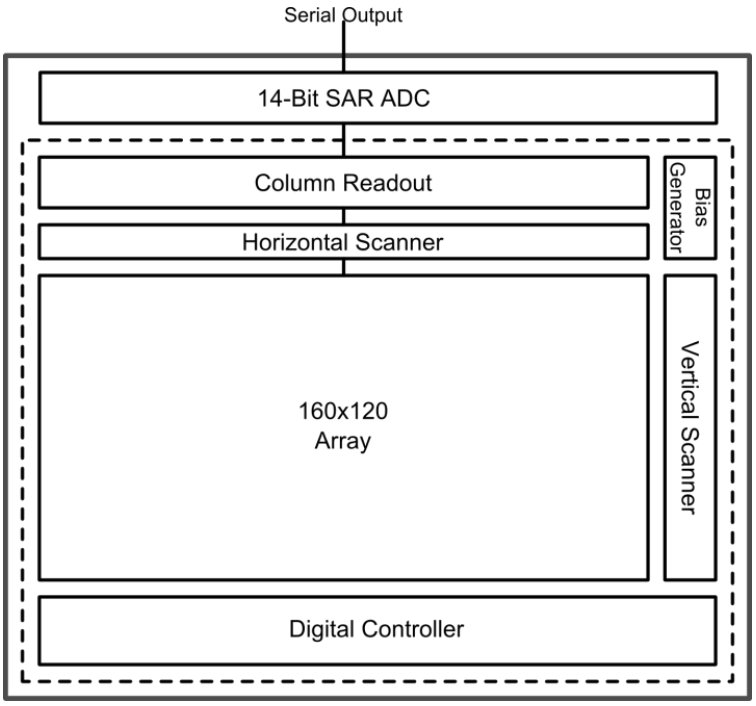

Figure 1.21: The SAR ADC embedded into the microbolometer.

The prototype layout is made accordingly in a flat manner with high aspect ratio. Hence, porting of the prototype layout to the microbolometer is easy. The minimum operating frequency limits the minimum power that can be consumed by the ADC. In this study, the ADC employs a resistive DAC in order to support an operation frequency down to almost DC. In order to realize 16-bit resolution, a modification is made on the resistive DAC. By using the operation of the SAR ADC and the modified resistive DAC as an advantage, a SAR ADC without frequency down-limit is realized.

More detailed goals of this thesis are as listed below:

1- Development of a model for the SAR ADC. The mathematical modeling should include the sources for non-linearity errors which are difficult to analyze in SPICE simulations. The performance criteria and effect on the overall behavior of each block should be decided. The correction algorithms for the errors should be investigated.

2- Design and implementation of the SAR ADC. The design should be low-noise and power-aware. There should be different configurations in order to test different variations with one chip.
3- Design of the test cards and the software. The test system should be low noise not to limit the ADC noise and SNR measurements. The software should be capable of performing basic operations such as INL and DNL measurements or digital correction.

The organization of the chapters is as follows:

Chapter 2 explains the detailed modeling of the SAR ADC. Initially, sub-blocks are modeled. Important points while modeling is explained. Then, top level simulation is run and results are explained.

Chapter 3 gives the detailed information about the implementation of the ADC. First, an introduction is presented for better understanding of the next sections. Then block level implementation is explained for analog blocks. Finally, digital block implementations are explained and the top level integration is covered.

Chapter 4 explains the test setup designed for the SAR ADC. The test types that will be conducted are covered and components that will be used are explained. The utilities of the test setup are given.

Chapter 5 summarizes the thesis and explains the future work.

CHAPTER II

MODELING OF SAR ADC FOR LOW-COST MICROBOLOMETERS

The successive approximation register ADC is a highly iterative device. Therefore, it is difficult to foresee the errors arising from a block. It has crucial importance to model the converter and observe the contribution of each block to the overall performance.

This chapter is organized as follows: Section 2.1 gives brief information about the modeling of converter. Section 2.2 explains the architecture of the ADC designed in this study. Section 2.3 describes the modeling of analog blocks of the converter. Section 2.4 explains the modeling of digital blocks. Finally Section 2.5 shows the effects on the top level simulation.

2.1 Introduction

The analog-to-digital conversion in the SAR ADC is a result of successful operations by a DAC, internal buffers and a comparator. The defects at the output values of the SAR ADC are a cumulative sum of all defects induces by every block in every step. An error in one step in the iteration may diffuse into the final result, making the identification of the source very difficult. Therefore, each block in the converter must be modeled and the effect to the overall system must be observed for the accurate operation of the converter.

Both ADC versions designed in this thesis use the same components except the low-pass filters. Hence, only the modeling of the high performance (16-bit) is covered in this chapter as it is the same procedure to model the 14-bit version. The model in this section covers the modeling of 14-bit ADC as well.

The models must include the dependence of the transfer characteristics to certain parameters. The building blocks are normally not time dependent, but the temperature, input voltage level, and statistical distribution of geometrical sizes may affect the operation of the circuit. In the next sections, the architecture and the blocks of the designed SAR ADC is explained.

2.2 SAR Analog-to-Digital Converter Architecture

The converter has two important analog signal channels: the input and the trial channels. The input channel consists of a buffer and a by-pass switch. The comparator input may be driven by the buffer or directly from the input terminal of the ADC. The buffer is placed for linearity concerns as explained in Section 2.5. This channel is lacking a sample and hold structure because the input voltage is known to be a sampled DC value for one complete conversion. Figure 2.1 shows the architecture of the SAR ADC.

The other important channel is the trial channel where the guess voltage is produced and connected to the negative input of the comparator. A 16-bit resistive DAC is used for the generation of the voltage. The aimed noise level requires a large capacitor for bandwidth limitation. As a result, a buffer is placed to the output of the DAC for driving the load quicker which is at the end of trial channel. Since the capacitor limits the bandwidth of both the DAC and the buffer, a quicker operation with a similar noise level is achieved.

The conditioned voltage values are supplied to the comparator. The input voltage is connected to the positive terminal of the comparator, where the guess voltage is connected to the negative terminal. The comparator output is one if the input voltage is greater than the guess voltage, otherwise it remains zero.

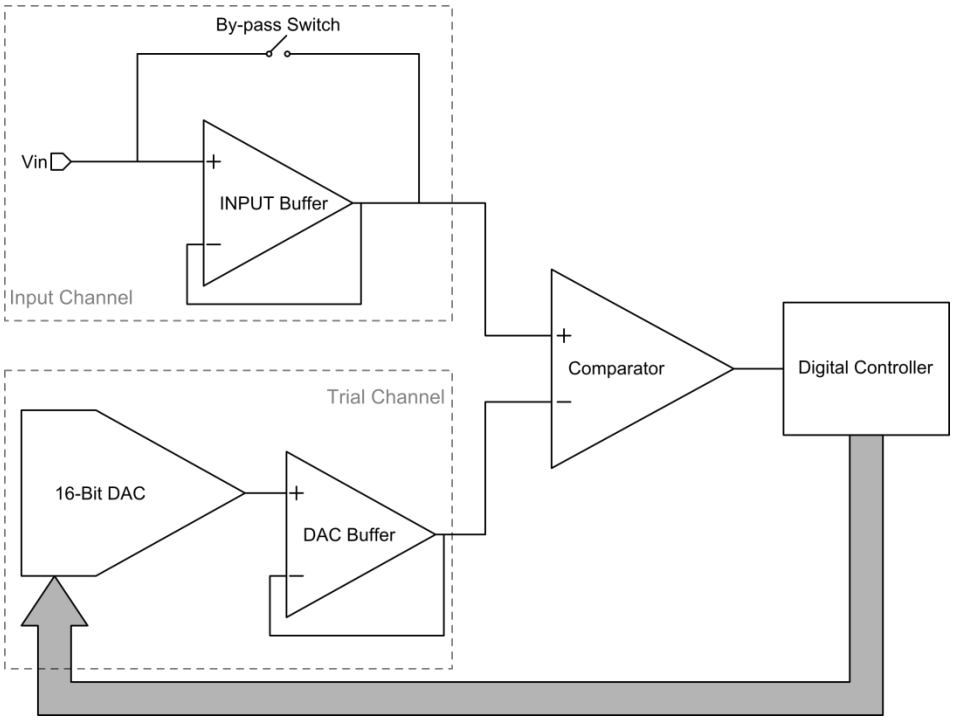

Figure 2.1: The successive approximation register analog-to-digital converter architecture designed in the scope of this study.

The digital controller is supplied with the result of the comparison and it generates the 16-bit output for the DAC accordingly. Besides the execution of the search algorithm, the digital controller has some utility functions which do not affect the architecture directly. These properties are explained in Section 3.3.

The sampling rate, resolution, and performance of the SAR ADC are decided mainly by the performance of the analog blocks. In the next section, detailed models of the analog blocks and their effects on the ADC performance are explained.

2.3 Analog Blocks

Models of each block with necessary details are presented in this section. First the digital-to-analog converter model is explained in Section 2.3.1 , then the buffer models are explained in Section 2.3.2 and lastly the comparator modeling is explained in Section 2.3.3.

2.3.1 Digital-to-Analog Converter

Each bit in the DAC has a binary weighted contribution to the output when it is set to one. Figure 2.2 shows the typical R-2R DAC architecture. But this is the ideal case where switch resistances are ignored and the resistors are assumed to be perfectly matched.

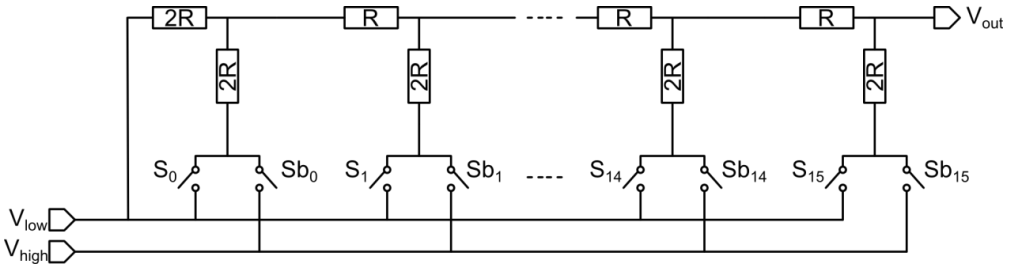

Figure 2.2: The voltage mode R-2R digital-to-analog converter. The switch resistances are ignored as well as matching of resistors.

In practice, each layer which is used for resistor implementation has a normal distribution over the silicon, even if they are matched with layout techniques. Table 2.1 shows the matching parameters of the resistors.

Table 2.1: The resistor matching parameter for XFAB 0.18µm CMOS process [18].

Resistor	ΔW(µm)	AR(% µm)
WELL Resistor Type 1	-0.03	1.19
WELL Resistor Type 2	-0.06	1.30
WELL Resistor Type 3	0.28	0.61
WELL Resistor Type 4	-0.03	1.12
WELL Resistor Type 5	-0.06	1.22
WELL Resistor Type 6	0.28	0.59
N-POLY Resistor	0.07	3.47
P-POLY Resistor	0.04	1.52
Lightly Doped P-POLY Resistor	0.10	1.77

In order to simulate the normal distribution, the standard deviation (σ) and the mean (μ) must be known. These are not given for the normal distribution of the absolute resistance but for the percent variation of the resistor value. As a result, the mean is always zero. The standard deviation is calculated as

$$\sigma = \frac{AR}{\sqrt{W_{eff} \times L}} \tag{2.3.1.1}$$

The W_{eff} is given as

$$W_{eff} = W - \Delta W \tag{2.3.1.2}$$

The calculation of absolute resistance variation is as

$$\Delta R = R_{ideal} \times \frac{(200 - x)}{(200 + x)} \tag{2.3.1.3}$$

In Equation (2.3.1.3), x is a random number from a normal distribution with the calculated σ. Some of these resistor types are already eliminated before the simulation. The WELL type resistors are non-linear devices. The diffusion thickness changes as the voltage across the terminals varies. The variable diffusion thickness turns this resistor into a voltage dependent resistor which is not suitable for this high resolution DAC application.

Before the modeling of the DAC, POLY resistor types are compared in terms of matching. A resistor value of 25kΩ is taken as reference for all resistors for low-power dissipation and the matching parameters are observed for fixed length and fixed width. Table 2.2 shows the results of the simulations.

Table 2.2: The resistance variation of poly resistors. The results are calculated with MATLAB for fixed length and fixed width.

Resistor Type	Fixed Length (250µm)		Fixed Width (10µm)	
	σ (ΔR)	Width (µm)	σ (ΔR)	Length (µm)
Lightly Doped P-POLY Resistor	8.92	10	8.87	250
P-POLY Resistor	33.00	2.8	9.16	892
N-POLY Resistor	30.22	3.3	9.93	757

The Lightly Doped P-POLY Resistor has the highest resistivity, so it can have the largest width for a given length. As a result it has the smallest standard deviation among others due to size advantage. On the other hand, all resistors seem to have similar standard deviations in the fixed width, but the P-POLY Resistor and the N-POLY Resistor type resistor occupy significantly larger area than Lightly Doped P-POLY Resistor. Hence, the R-2R ladder is built from the Lightly Doped P-POLY Resistor for best matching in the smallest area.

The accuracy of contribution of each step in the R-2R ladder depends on the resistor matching in the entire DAC. A virtual R-2R ladder network is built with hypothetically matched resistor. Each resistor is selected with a MATLAB function (normrnd or randn), which returns a random number with the given standard deviation and mean. Superposition is made for each bit. The seen resistances are calculated from each $V_{x(x)}$ node. These values are $R_{left(x)}$, $R_{right(x)}$ and $R_{L(x)}$. $R_{L(x)}$ is the equivalent resistance of the branch below $V_{x(x)}$ node. R_L is calculated as

$$R_{L(x)} = R + R + R_{sw} \tag{2.3.1.4}$$

Each R is a randomly picked value from the normal distribution. R_{sw} is the switch resistance. Figure 2.3 shows the modeling scheme of the R-2R DAC.

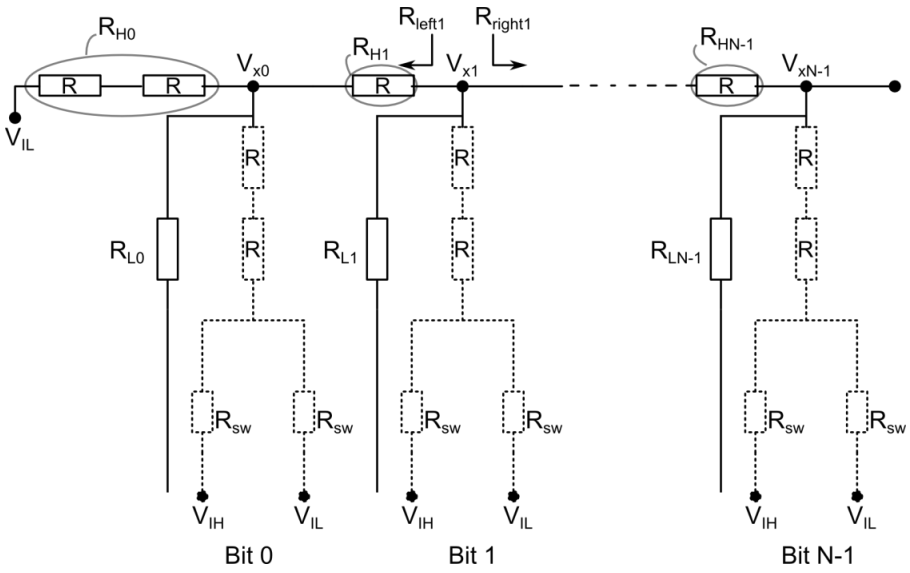

Figure 2.3: The R-2R modeling scheme. The switch resistances are included in the R_L equivalent resistances.

The $R_{left(x)}$ resistances are calculated as

$$R_{left(x-1)} = (R_{left(x-2)} // R_{L(x-2)}) + R_{H(x-1)} \tag{2.3.1.5}$$

For the first bit, $R_{left(0)}$ equals to $R_{H(0)}$ which is R+R. $R_{H(x)}$ is the equivalent resistance in between V_x nodes of each bit. For calculation of R_{left} for the higher order bits, equivalent resistances from the lower bits are required. A recursive calculation is made and R_{left} values are saved in an array for each bit. An R_{right} array is prepared in similar manner. This time the recursive algorithm runs from right to left. The value of $R_{right(x)}$ is given as

$$R_{right(x-2)} = (R_{right(x-1)} // R_{L(x-1)}) + R_{H(x-1)} \tag{2.3.1.6}$$

The $R_{right(N-1)}$ is infinity as this branch is an open circuit. After each resistance seen from each V_x node is calculated, the voltage contribution of each bit is derived. Due to the superposition principle, one bit is connected to V_{IH} while the others are connected to V_{IL}. First, the V_x voltages for each node is calculated as

$$V_{x(x)} = V_{REF} \times \frac{R_{left(x)} // R_{right(x)}}{\left(R_{left(x)} // R_{right(x)}\right) + R_{L(x)}} \tag{2.3.1.7}$$

In order to simplify the voltage calculation, V_{REF} is given as in Equation (2.3.1.8) and V_{IL} is added to the output voltage in the end.

$$V_{REF} = V_{IH} - V_{IL} \tag{2.3.1.8}$$

Then V_x is transferred to the output by running a calculation for each hop. Figure 2.4 shows the transfer of V_x voltage to the output node.

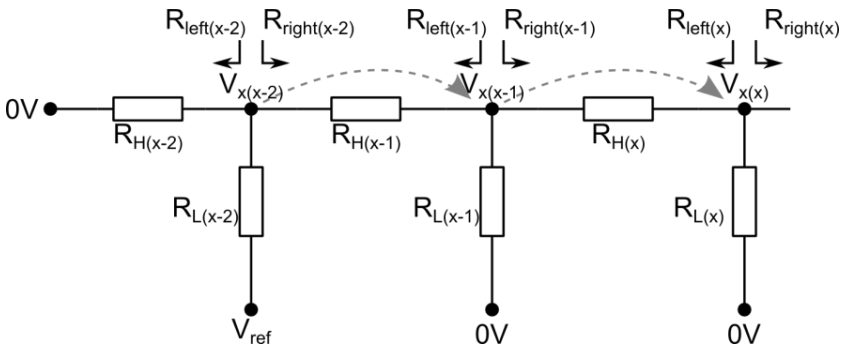

Figure 2.4: The voltage transfer scheme to the output. The voltage is transferred to the neighbor node until output node is reached.

The neighbor V_x node voltage is calculated as

$$V_{x(x-1)} = V_{x(x-2)} \times \frac{R_{right(x-1)} // R_{L(x-1)}}{\left(R_{right(x-1)} // R_{L(x-1)}\right) + R_{H(x-1)}} \tag{2.3.1.9}$$

This calculation is made for each bit until the voltage of the output node is found. The final result is the sum of all output values for each bit. The bits, which are connected to the V_{IL} bus, are not included in the calculation as they have no contribution to the output voltage.

The results acquired with this method exhibit the maximum DNL and INL values of the DAC. These simulations are made for 1024 R-2R ladders, so a large set of samples are considered for accurate results. Figure 2.5 shows the DNL profile the R-2R ladder without the switch resistances.

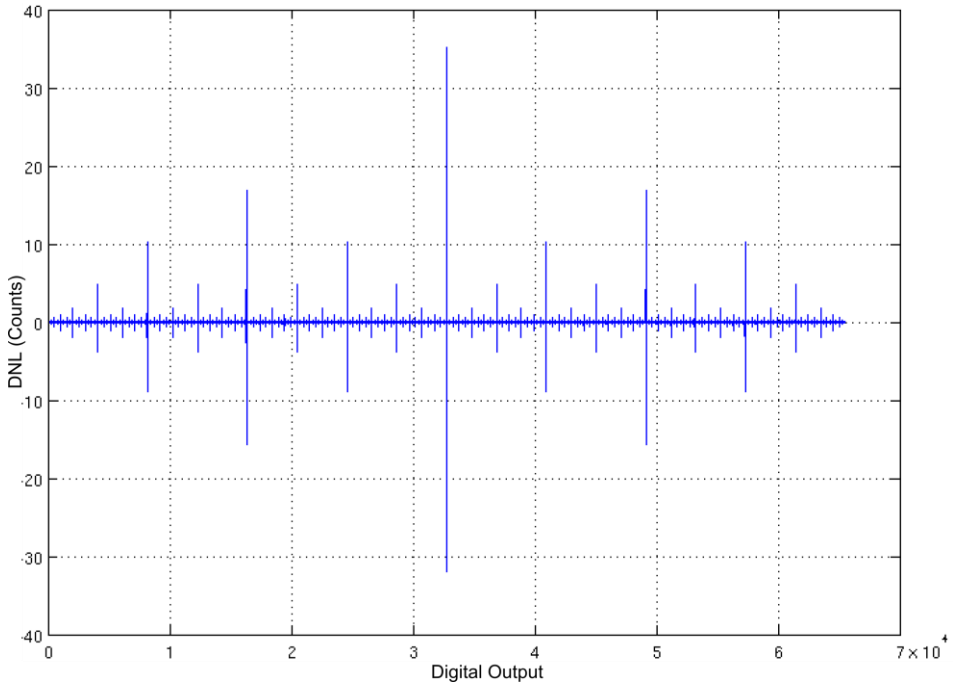

Figure 2.5: The DNL profile of the DAC is given while the input is swept from 0 to 65535. The switch resistance is not included. The outputs of 1024 simulations are drawn altogether.

The highest differential nonlinearity errors typically occur where the higher order bits toggle because the slightest resistor mismatch causes multiple LSBs deviation from the ideal step size. Figure 2.6 shows the INL profile of the R-2R DAC without the contribution of the switch resistances. When there is a mismatch in the resistors, the output voltage tends to deviate from the ideal level until the bit with the mismatch toggles. Then the output voltage switches the error polarity with the same magnitude and decreases until the endpoint of the range. As a result, the highest integral nonlinearity errors also occur when higher order bits toggle. The cloud is larger through the most significant bit (MSB) due to this reason. For a more realistic model, a switch resistance of 7Ω is included in the next simulations. The variation of switch resistance is not taken into account because a possible variation in the resistor value is much larger.

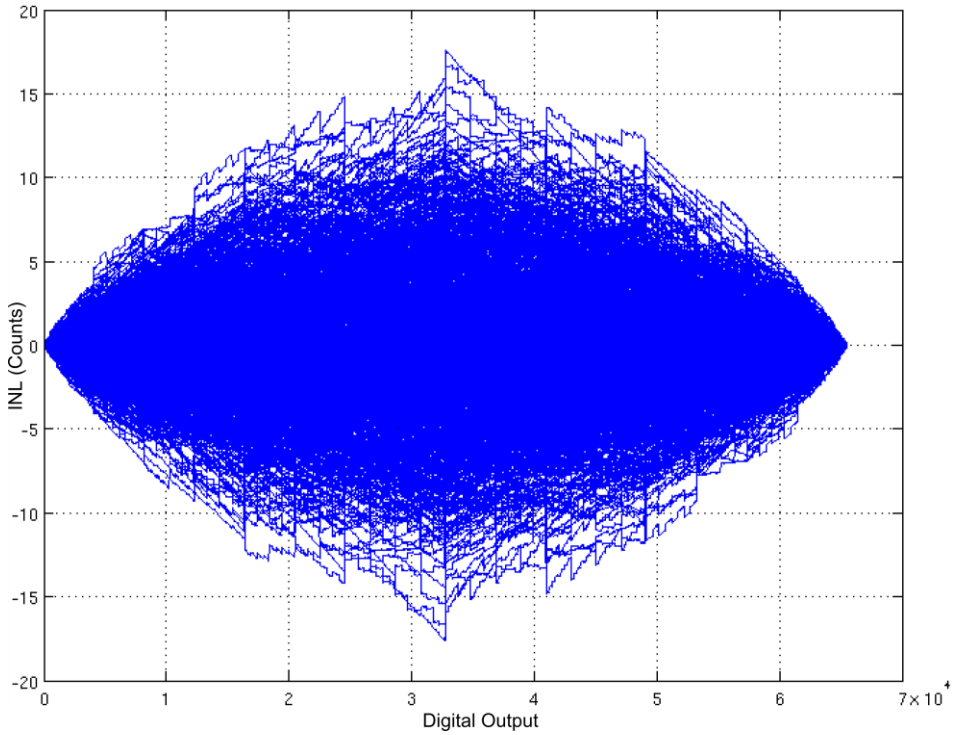

Figure 2.6: The INL profile of the DAC is given while the input is swept from 0 to 65535. The switch resistance is not included. The outputs of 1024 simulations are drawn altogether.

Figure 2.7 and Figure 2.8 show the DNL and INL profiles respectively. The DNL tends to linger more in the negative half when the switch resistance is considered. But the effect is not very significant for the 12^{th} bit and below. The INL profile exhibits a more interesting behavior as the graph tends to crack from the middle moving each half to positive and negative zones. Therefore the output of the DAC shows different characteristics of deviation from the ideal curve in the upper and the lower parts of the digital input range. The output tends to be higher than the ideal output before 2^{15} and lower after.

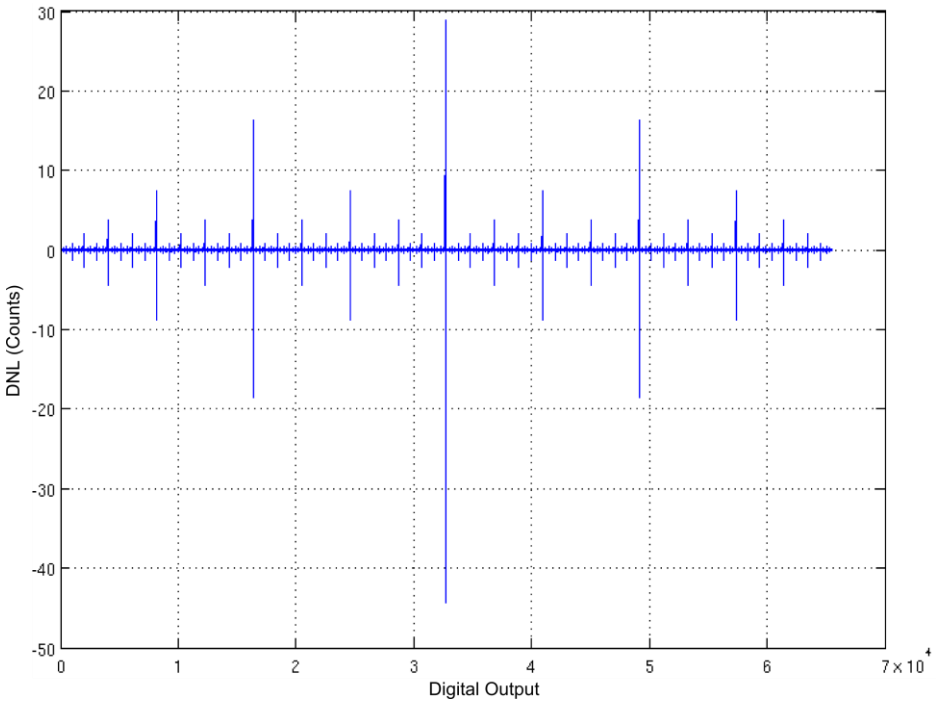

Figure 2.7: The DNL profile of the DAC is given while the input is swept from 0 to 65535. The switch resistance is included. The outputs of 1024 simulations are drawn altogether.

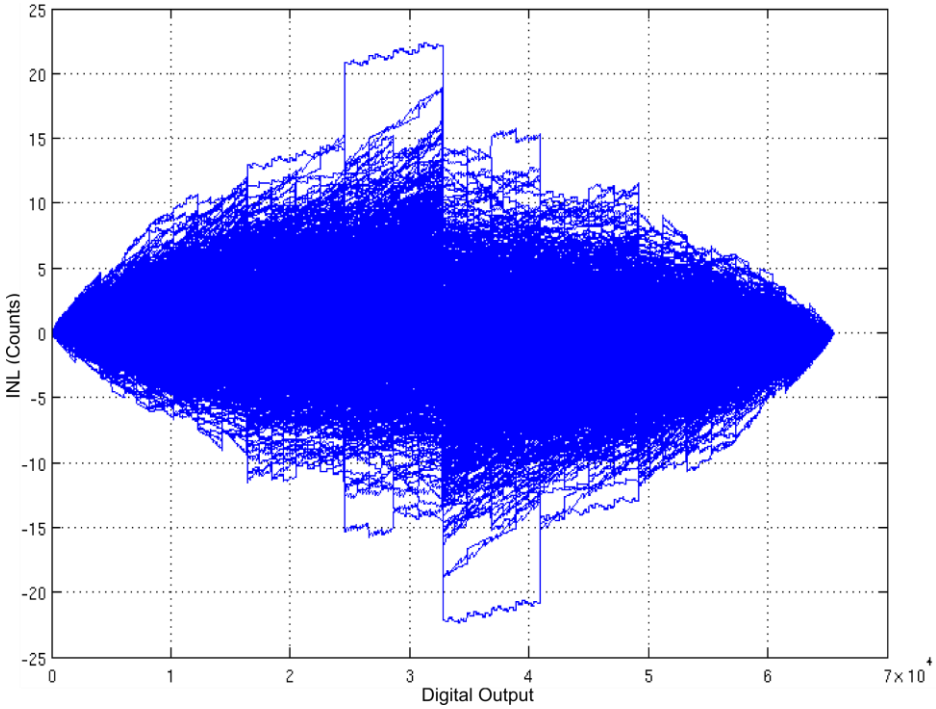

Figure 2.8: The INL profile of the DAC is given while the input is swept from 0 to 65535. The switch resistance is included. The outputs of 1024 simulations are drawn altogether.

The DNL performance of the ADC is decided by the differential linearity performance of the DAC. The positive DNL of the DAC shows up as DNL at the ADC output. The DNL error of an ADC cannot be corrected. However, the negative DNL of the DAC creates missing codes equal to the same magnitude in the ADC characteristics. Figure 2.9 shows the effect of DAC on the ADC performance.

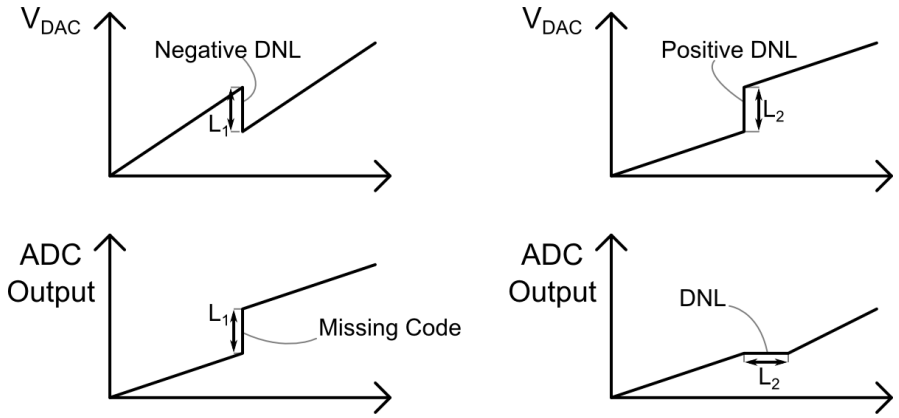

Figure 2.9: The effect of DAC on the ADC performance. The negative DNL amount is reflected to ADC output as missing code while the positive DNL amount is carried to the ADC output as DNL.

The readout gain of the low-cost bolometer is quite high [1]. As a result, the DNL error is very small when it is referred to pixel. Although the referred DNL error is not very large, the partially correctable missing code error is preferred. The DAC is adjusted to have a negative DNL error. As a result, the ADC output is to have missing codes instead of a DNL error. In order to achieve negative DNL, a ΔR is inserted to 2R branches of each bit. The amount of ΔR is 75Ω. This amount of resistance is created by lengthening one of the resistors by 0.75µm. The differential non-linearity is imposed to be negative with this technique [19]. Figure 2.10 and Figure 2.11 show the resultant DNL and INL profiles respectively. The characterization of the ADC does not restore the proper operation but cover the steps at expense of full range loss. Each step at the output is compensated by subtracting an offset. The full range shrinks due to the cumulative subtraction of the offsets through the highest output code. The effect of the correction is shown in Section 2.5.

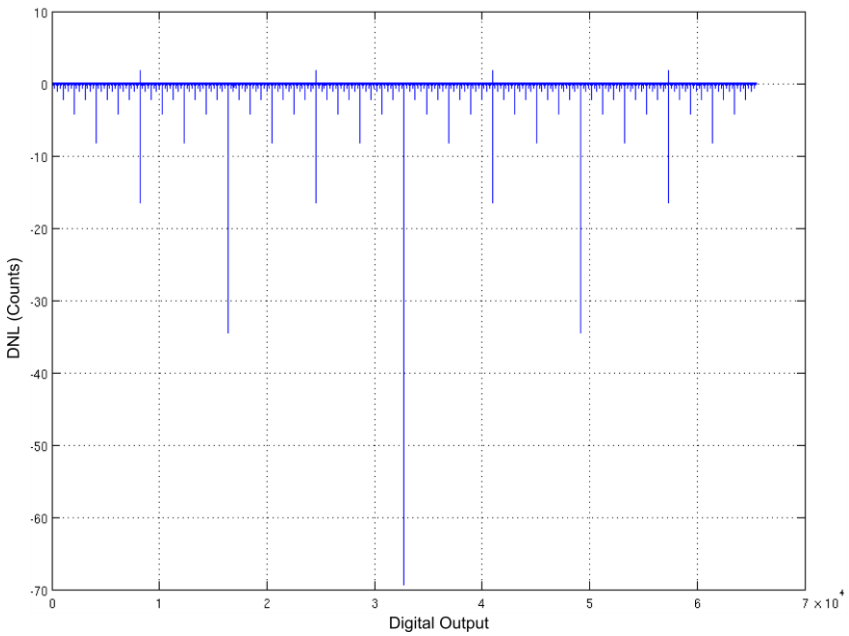

Figure 2.10: The DNL profile of the DAC is given while the input is swept from 0 to 65535. The switch resistance is included and 75Ω resistor added. The outputs of 1024 simulations are drawn altogether.

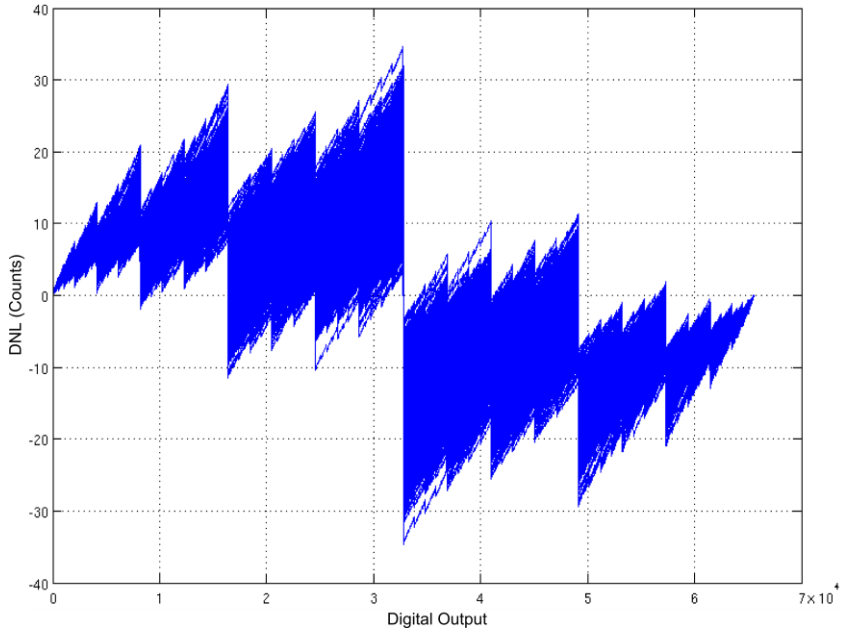

Figure 2.11: The INL profile of the DAC is given while the input is swept from 0 to 65535. The switch resistance is included and 75Ω resistor added. The outputs of 1024 simulations are drawn altogether.

2.3.2 Buffer

The buffers are two folded-cascode operational amplifiers with different input transistor. The important property of the buffers, which is included in the MATLAB model, is the gain variation with respect to the input voltage. The gain expression of a buffer is

$$A_V = \frac{A}{A+1} \tag{2.3.2.1}$$

A is the open loop gain of the operational amplifier. The open loop gain of the amplifier is not constant. It decreases on both ends of the input range. As a result the voltage transfer of the buffer introduces an error dependent on the input. Figure 2.12 shows the closed loop gain versus input voltage plot of the buffers.

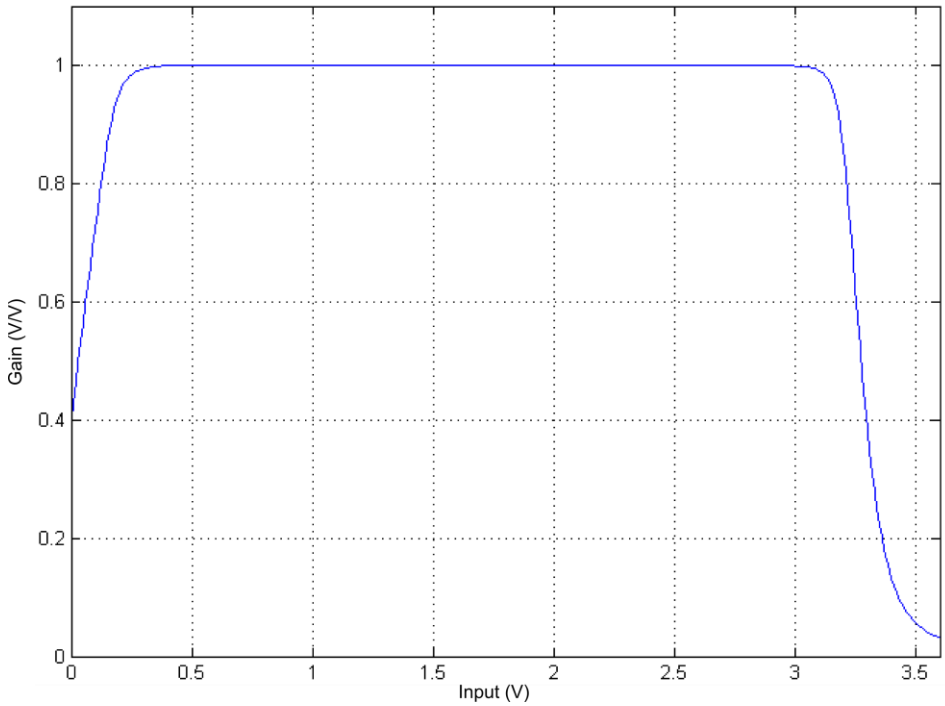

Figure 2.12: The closed loop gain versus input voltage characteristics of the buffers. The gain is significantly decreasing below 0.4V and above 3.0V.

The buffer models in the simulation are basically look-up tables for gain where the input voltage is multiplied with the corresponding gain and transferred to output. The size of the look-up table is important as it should not be too small. Although approximation is done for finding missing gain values, a sufficiently set of voltage values must be covered for realistic modeling. Gain values are recorded for each 10mV step at the input voltage from 0 to 3.6V. Linear approximation is done for input values in between every 10mV gap for the worst case estimation. Thus the nonlinearity effect due to buffer linearity is introduced to the top level simulation.

2.3.3 Comparator

The modeling of the comparator is quite straightforward and simple. The only important characteristic for the linearity simulation is the input offset. The input offset arises from mismatch of devices. It is a static error [20]. Figure 2.13 shows the input offset representation for the comparator model.

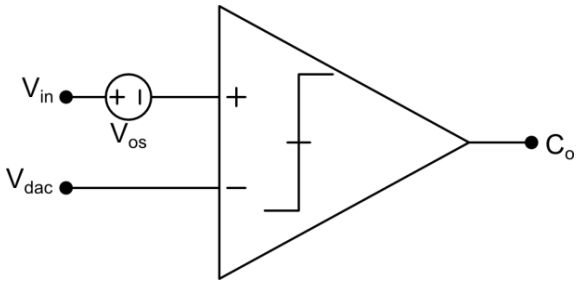

Figure 2.13: The comparator input offset representation is shown. It is modeled as a DC voltage supply in series with input voltage.

The offset value can be a positive or a negative value. Typically, it affects all output codes with the same amount of offset. It is easily removed by subtracting or adding an offset to the output code. In the model, the output is kept low until the DAC output is greater than the input voltage by an amount of V_{OS}.

2.4 Digital Blocks

The digital blocks are collected under five main groups: timing generator, output data serializer, serial interface, synchronizer, and successive approximation register. Since the MATLAB simulation is only focused on linearity issues, a simple function is replacing the actual structure of the digital controller. The function simply runs the binary search algorithm. The detailed explanation of each block is given in Section 3.3.

2.5 Top Level Simulation

The cumulative effect on the SAR ADC is observed by modeling each block and simulating on top level. Figure 2.1 shows the top level ADC. In the simulation, initially the DAC model is created as explained in Section 2.3.1. The DAC function sweeps the whole output range and writes it to an array of size 1x65536. The array is passed to the top level simulation code. The digital controller function returns a 16-bit value to the top level code for each approximation step. The 16-bit number is taken as the index number of the array from the DAC function. An analog voltage is generated by finding the corresponding value at the given index and given to the buffer function. The buffer function operates as explained in Section 2.3.2 and returns the post-buffer voltage value. The returned voltage is given to the comparator function which operates as explained in Section 2.3.3. The comparator output is given to the digital controller function as an argument for successive approximation operation. When a conversion is finished, the digital controller sets the finished flag in the top level code. The finished flag triggers the top level code to save the digitized value to an array. The entire range is swept with this technique and every defect which arises from DAC, buffers, and comparator is observed.

Two cases are simulated with this method. First case is the direct connection of V_{in} to the positive terminal of comparator. Figure 2.14 and Figure 2.15 show the DNL and the INL results for the direct connection of V_{in}, respectively.

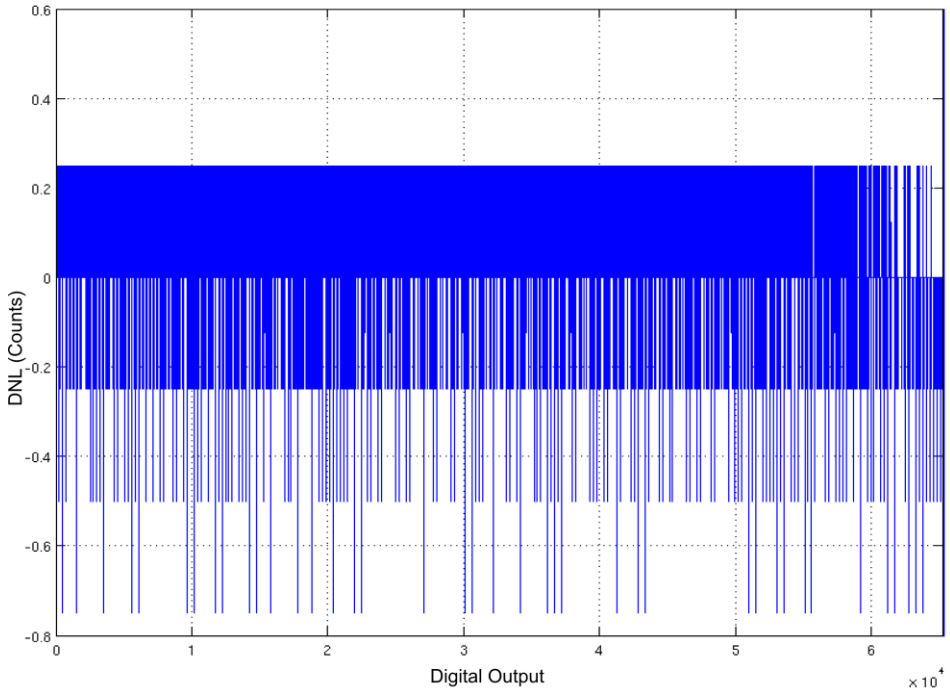

Figure 2.14: The DNL profile of the SAR ADC when the input voltage is directly connected to the comparator.

The DNL results in the first case are in between -0.75 and 0.25 counts. The forced negative DNL at the DAC output causes missing codes instead of DNL errors at the ADC output. Nevertheless the existence of the input buffer and the missing codes significantly affect the INL results. The sharp jumps in the INL result indicates the missing codes that occur when the output code is toggling at high order bits. Characterization of the ADC output can be done, since each input level corresponds to a unique code. The correction method is determining the final output codes. It is finding where the missing codes occur, and subtracting an offset for any output value equal or greater than the missing code point found. The offset is equal to the amount of missing code for each occurrence and it is calculated in a cumulative fashion. The amount to be subtracted from an output value is equal to the sum of all offsets which belong to a smaller code.

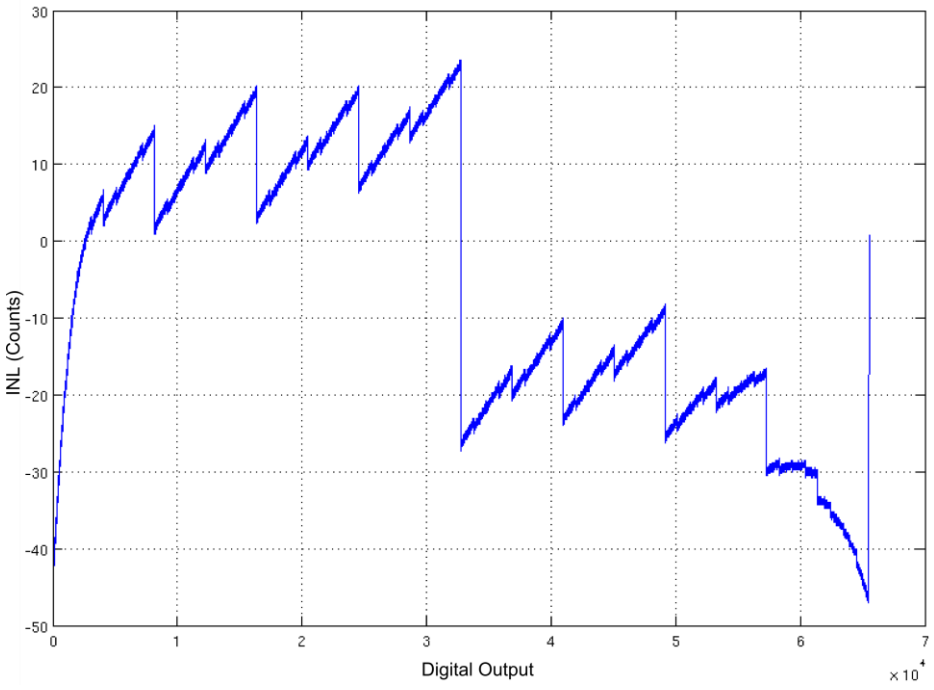

Figure 2.15: The INL profile of the SAR ADC when the input voltage is directly connected to the comparator.

The correction does not affect the DNL result but greatly improves the INL. Figure 2.16 shows the corrected INL profile. The sharp edges in the INL profile are removed. Although the highest INL value seems to be larger, the actual defect is turned into a gain error in the linear range. The gain error is easily corrected by two point correction during image processing of the image sensor output. Nevertheless the INL is not linear at two extreme ends. These parts are difficult to recover by image processing because the slope is not linear. Circuit adjustment is made for adding these extreme ends to the input range.

In the second case, a buffer is placed to the input signal channel and it is identical to the one used at the output of the DAC. The purpose is to exert the same nonlinear gain error to the input voltage in order to increase the input range by correcting the curvature at both end of the INL curve.

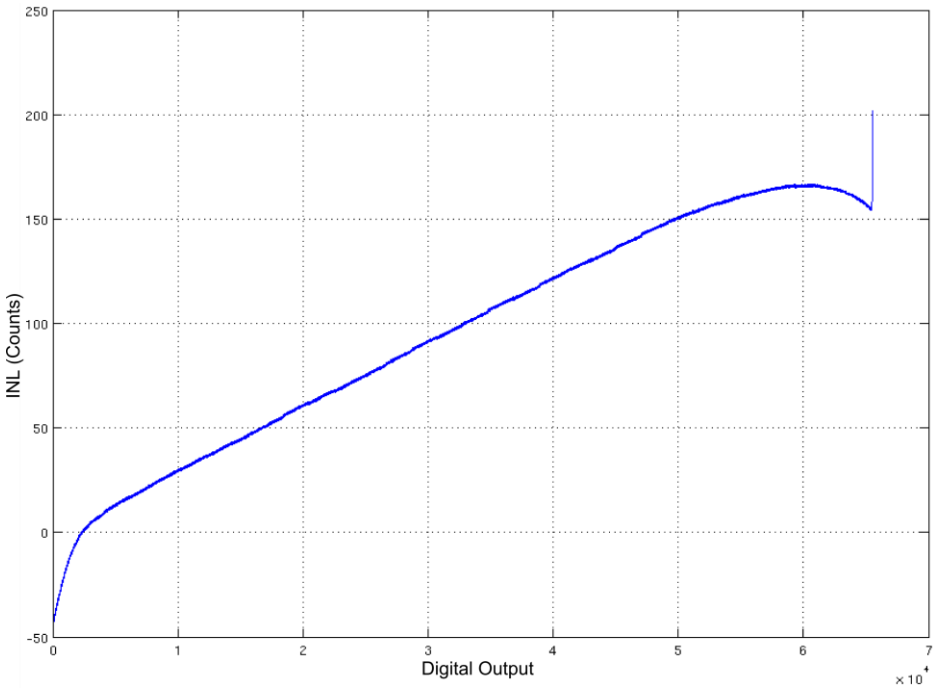

Figure 2.16: The INL profile of the SAR ADC after digital correction is made on the output code.

This method increases the power consumption and the noise of the ADC but greatly increases the INL performance. Figure 2.17 shows the digitally corrected INL profile of the buffered input SAR ADC. The input range of the ADC is expanded by enhancing the linearity at extreme ends. The DNL is not affected by this process as it solely depends on the DNL of the DAC.

The disadvantage of this method is the decrease in the effective resolution of the ADC. The input range of the ADC is ideally represented with 65536 levels which correspond to 2^{16}. Because of the missing codes, the input range is represented by 65536-Total Sum of Missing Codes. Since the input range is the same, each bit is effectively corresponding to a bigger value than one LSB. As a result, the output slope of the ADC deviates from the ideal ADC output curve. The effective resolution is decreased to 15.995-bit. This loss is negligible when it is compared to full scale.

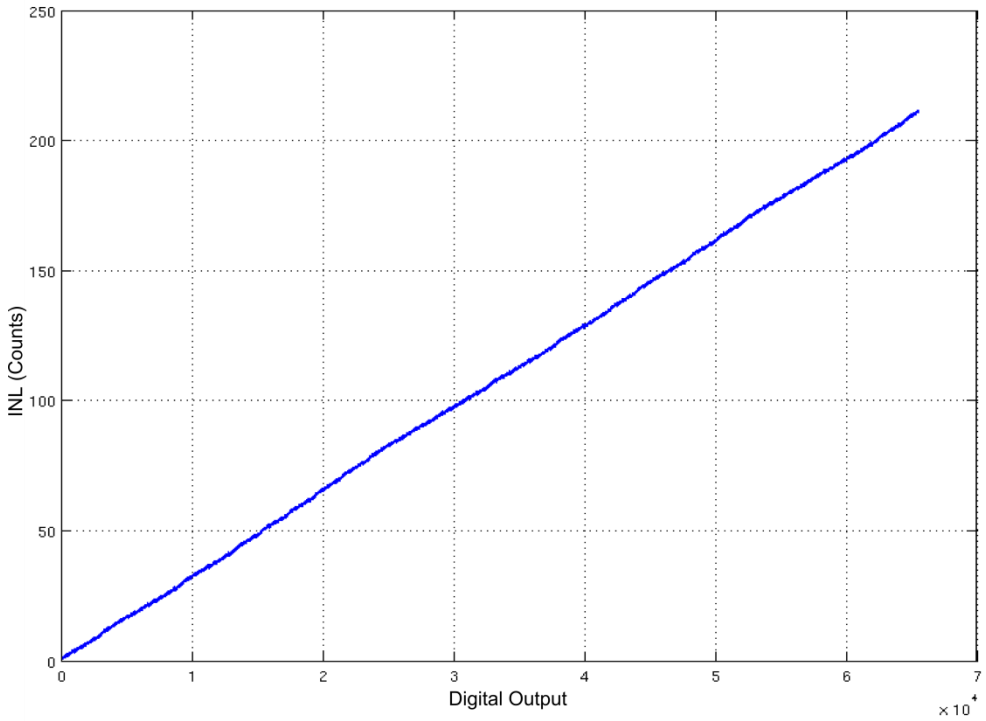

Figure 2.17: The INL profile of the SAR ADC with further enhancement due to dual buffer technique.

The linear INL means gain error as it is a linear deviation from the ideal line. Figure 2.18 explains the relation of the INL and gain error on the input-output characteristics. The gain error introduced by the ADC does not affect the imaging quality because the imager has one output and all the pixels are exposed to the gain error of the same ADC. This type of error cannot be noticed by viewers of the image taken by the imager. Nevertheless, this error can be removed by normalizing the gain of the ADC during the image process.

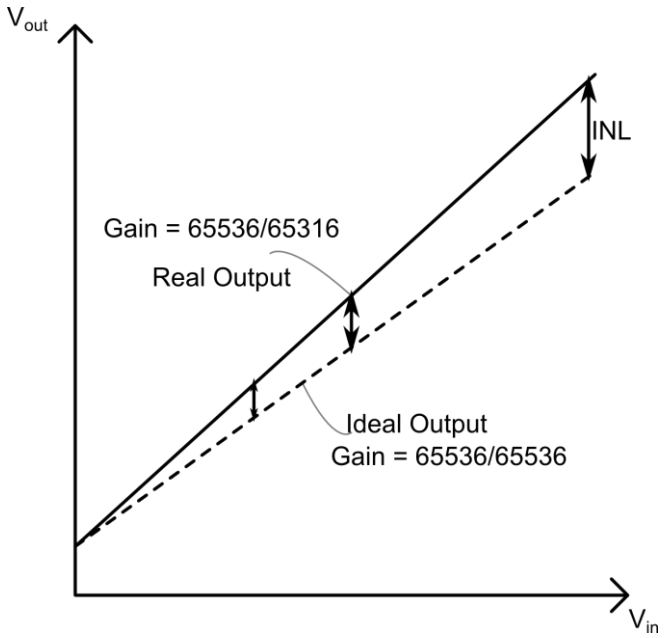

Figure 2.18: The explanation of the gain error and INL on the input-output curve.

In conclusion, the single buffer system exhibits lower power and noise where the dual buffer system enhances the imaging performance. The ADC has small DNL values, so small voltage differences on the image data are mapped into different digital codes and recognized by the computer. The linear INL, which is a gain error, is corrected by post-processing of the imaging data.

CHAPTER III

IMPLEMENTATION OF THE SAR ADC

This chapter explains the physical realization of the successive approximation analog-to-digital converter. First, brief information about the implementation chapter is given in Section 3.1. In Section 3.2, the implementation of the analog blocks is explained. In Section 3.3, digital blocks, their implementation and functions are explained. In Section 3.4, the top level integration is explained and a summary of the implementation chapter is made. Finally, in Section 3.5 the implemented ADCs are summarized and compared to the previous works in the literature.

3.1 Introduction

The implementation of the blocks is very important as it is the physical realization of the calculations. There are various factors which should be considered for good performance.

All of the digital and analog blocks explained in the implementation section are the same for the 14-bit and the 16-bit ADC versions implemented in this work. Only difference is the size of the capacitors in the low-pass filters. A capacitor value of 4pF and 16pF are used in 14-bit version and 16-bit version respectively. The implementations of all blocks cover the structure of both ADCs. Nevertheless, 16-bit version is taken as default when needed as the specifications are more challenging.

The implementation of the SAR ADC is made in three steps. Firstly, designing, simulating and making the layout of the analog blocks. Secondly, implementation of the digital blocks is made, according to the requirements of the analog structures. Finally, the top level integration and other necessary blocks are designed. The details of these steps are explained in the following sections.

3.2 Analog Blocks

This section explains the detailed implementations of analog circuitry. The analog circuits are divided into four subsections: digital-to-analog converter, buffer circuits, comparator, and bias generator. The digital-to-analog converter is for the generation of the guess voltage that input is compared to. The buffers are used for driving capacitive load and enhancing linearity. The comparator is used for deciding if the input voltage is greater than the guess voltage. The bias generator is responsible for the providing the current biases for those blocks.

3.2.1 Digital-to-Analog Converter

The digital-to-analog converter is a voltage output R-2R ladder. It is implemented using lightly doped resistive poly layer due to matching performance as calculated in 2.3.1. Each resistor is set to be 25KΩ. The equivalent resistance of the R branch is 25KΩ where the equivalent resistance of the 2R branch is 50KΩ. Figure 3.1 shows the structure of the DAC. Complementary switches are used in order to maintain proper operation for different V_{high} and V_{low} values because these values may be changed during the test.

The switch resistance is an important factor in the implementation of the R-2R DAC. It is added to the 2R branch and it directly affects the conversion performance. The ON resistance of a transistor is calculated as

$$R_{ON} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} \tag{3.2.1.1}$$

After the DAC output is settled, there is a small DC current drawn from switches. Due to the large aspect ratio of the switch transistors, this current is supplied in the linear region with a very small V_{DS} drop. Then the resistance calculation is as in Equation (3.2.1.2).

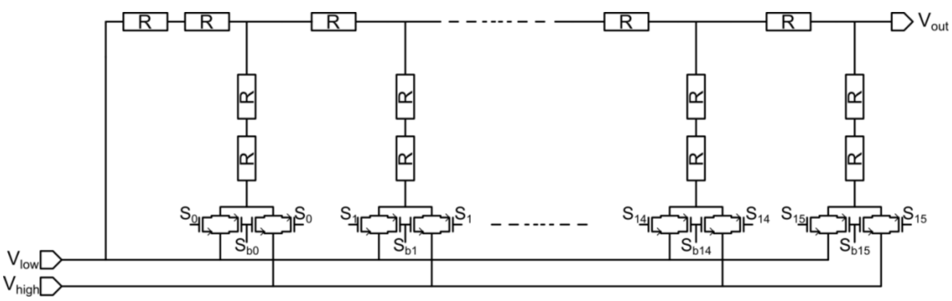

Figure 3.1: The structure of the DAC. Complementary switches are used for proper operation with different V_{high} and V_{low} values.

$$R_{ON} = \frac{1}{C_{OX}.\mu.\left(\frac{W}{L}\right).V_{OV} - V_{DS}} \qquad (3.2.1.2)$$

However, the complementary switch consists of an NMOS and a PMOS device. The overall resistance of the switch is a combination of both device resistances. For high input values, the PMOS transistor is on while for low input values, the NMOS transistor is on. Due to the natural difference in the electron and hole mobility's, the PMOS device size is two times the NMOS device size. Consequently, $C_{OX}.\mu.\left(\frac{W}{L}\right)$ terms are close for both transistors and the ON resistances at both ends of the input range are close and within the limit. The limit is decided by the variation of the resistance values. Each 25KΩ resistor can vary up to 26Ω for not causing DNL more than 1 bit. As long as the switch resistance variation is very small compared to resistor variation, it does not have an effect on the performance. Figure 3.2 shows the resistance profile of the complementary switch versus the voltage. The width of the transistors is selected as large as possible in order to decrease the switch resistance. NMOS devices have a width of 400µm where PMOS devices have 800µm. The transistor lengths are set to 0.35µm which is the smallest size allowed for a 3.3V transistor in this process. Small length results in lower channel resistance in saturation region which fastens the settling of the DAC.

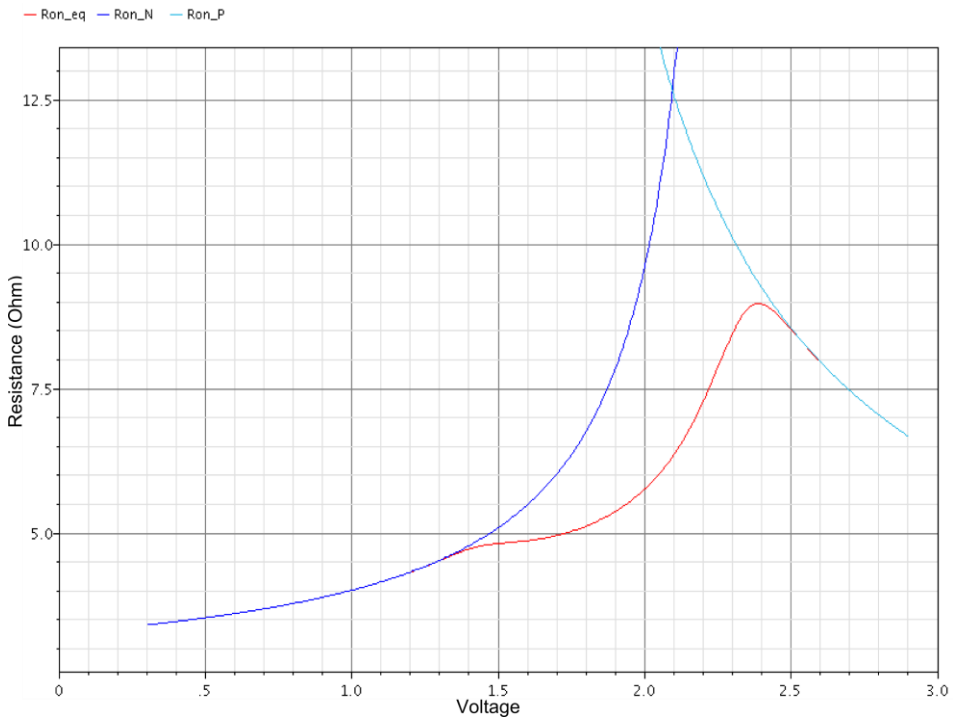

Figure 3.2: The switch resistance versus voltage. The switch resistance is changing in between 2Ω and 8Ω. The PMOS and the NMOS transistor resistances are also shown with the green and the blue curves.

The matching of the resistors is examined in terms of dimension and type of the layer used in 2.3.1. Different methods are simulated for enhancing the matching further [21]. The first method is to use a dummy switch for each resistor. The additional switch increases each R value by a ΔR. This decreases the effect of the resistance mismatch due to the logic switches. However, the system slows down significantly because cumulative switch reactions for large voltage changes take long time. The first iterations in the SAR ADC require large voltage changes at the DAC output, as a result, a notable reduction in the speed is observed. This method is not used because excessive speed deterioration is not acceptable. The second method is to use larger resistors in parallel to obtain the 25KΩ resistance. As the number of resistors in parallel increases, the equivalent value is closer to the nominal value. This is a sort of averaging method. As the number of parallel branches increases, the dimensions of the used resistors increase. This further approximates the equivalent value to the nominal value because

the deviation of large resistance in large dimensions decreases. This method improves the matching greatly, yet the resistors exhibit a capacitive effect and slow the converter down significantly. This method is also inappropriate for enhancing the matching. Instead of those methods, the typical R-2R structure is used and a faster DAC is obtained. The necessary matching for this application is provided by means of other techniques as explained in 2.3.1.

The output noise of the DAC is set to be half LSB. For reaching that noise level, the bandwidth of the DAC must be limited with a low pass filter. The value of the bandwidth capacitor is calculated as

$$C = \frac{k.T}{{v_n}^2} \tag{3.2.1.3}$$

For a noise level of 16μV_{RMS}, a 16pF capacitor must be used. The voltage on the capacitor over time is calculated as

$$V = V_f\left(1 - e^{-\frac{t}{R.C}}\right) \tag{3.2.1.4}$$

The output resistance of the DAC is 25KΩ which results in a time constant of 400ns. The time to settle within ½ LSB, when the most significant bit of the DAC is set, is shown as

$$2^{15} - 2^{-1} = 2^{15}\left(1 - e^{-\frac{t}{400.10^{-9}}}\right) \tag{3.2.1.5}$$

After rearranging Equation 3.2.1.5

$$t = 16.\ln 2\,.400.10^{-9} = 4.436\mu s \tag{3.2.1.6}$$

Even only the first bit requires 4.43μs to settle where the entire conversion time for one sample corresponds to 7.9μs for a 128Ksps ADC. Passive driving of the capacitor is not feasible for this system. Therefore, an operational amplifier with buffer configuration is connected to the output of the DAC. Thus, the capacitor is driven in a much shorter time and noise the bandwidth is still limited around the desired values. This is done because the capacitor limits the noise bandwidth of the DAC and buffer together.

Nevertheless, a tiny capacitor of 400fF is placed to the output of the DAC as it enhances the settling time by preventing strong overshoots. Figure 3.3 shows the structure of the DAC channel. The buffer structure is explained in 3.2.2.

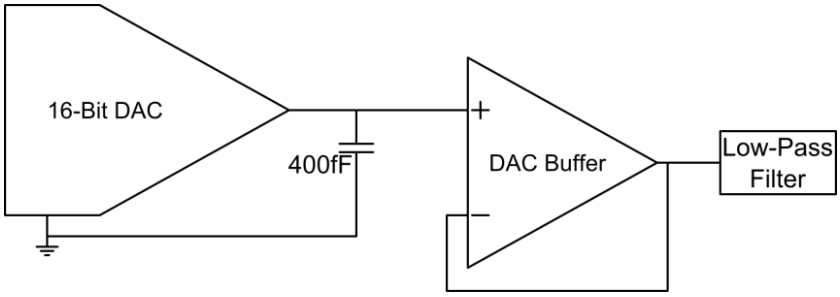

Figure 3.3: The DAC channel structure. It consists of the 16-bit resistive DAC, the buffer and the low-pass filter.

The high and the low references of the DAC are provided by external voltage references on the proximity card. The largest DC current drawn from the reference is 35μA. This current can be easily supplied or sinked by using commercial reference ICs [22] [23]. Grounding of the references and the ADC is critical at this point. Any offset between grounds of the ADC and references result in a wrong reference voltage. Furthermore if one of the grounds bounces while the other one is quiet, this is observed on the voltage reference by the ADC. Since the references are on the same package as the ADC, the grounds of the ADC and the R-2R references are close enough for good performance.

Figure 3.4 shows the layout of the DAC. All three resistors for each bit are stacked together for improving matching. Complementary switches are placed below each bit. The switch driving buffers and level shifters are placed below the switches. The silicon area below the poly resistors are covered with an N-Well and biased with V_{DD}. This is made for isolating the resistors from any possible signal coupling from the substrate.

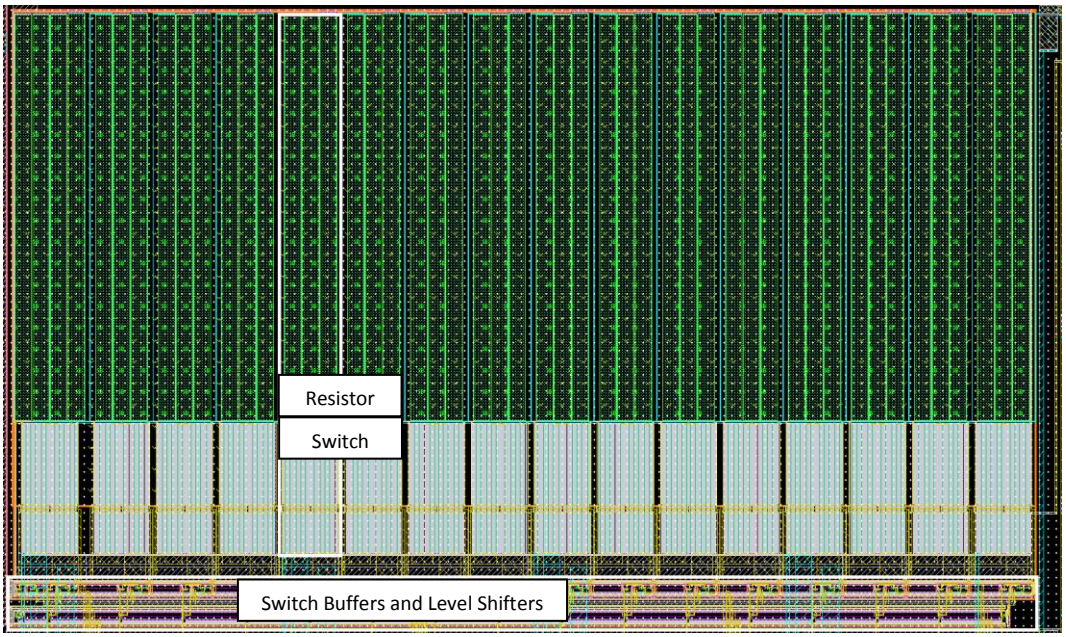

Figure 3.4: The R-2R DAC layout. The components are shown in the white boxes. It is around 750µm width and 500µm height in 0.18µm CMOS technology.

3.2.2 Buffers

The buffers are primarily used for speeding up the DAC while not giving up on the noise performance. There are two types of buffers implemented in the ADC. These structures are selectable by serial programming and operate one at a time. Both structures are folded cascode operational amplifiers. This topology is suitable because the load is purely capacitive. Besides, this topology is preferred due to its simplicity and robustness.

The first operational amplifier has a depletion mode NMOS input pair. Figure 3.5 shows the folded-cascode opamp structure.

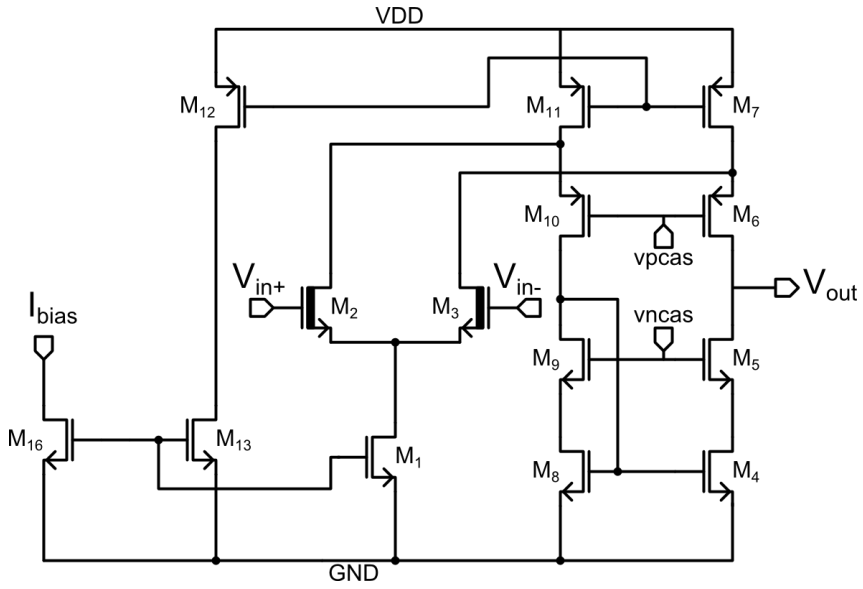

Figure 3.5: The first folded-cascode opamp structure. The input pair is depletion mode NMOS transistors in order to increase operation range of the buffer.

The output voltage of the buffer is given as

$$V_{out} = \frac{A}{A+1} \times V_{in} \tag{3.2.2.1}$$

where A is the DC gain of the operational amplifier. The gain must be 102.3 dB or higher to introduce a gain error less than 1 LSB. The error arising from low gain is a linear error and it can be tolerated in the imaging applications. The main problem is the variation of the gain as the input common mode changes. Figure 3.6 shows the gain versus the input voltage characteristic of the NMOS input buffer. This variation causes nonlinear defects on the output characteristics of the ADC. Either operation range can be narrowed down to the acceptable regions for fixing this problem, or a system level solution can be used as explained in 2.5.

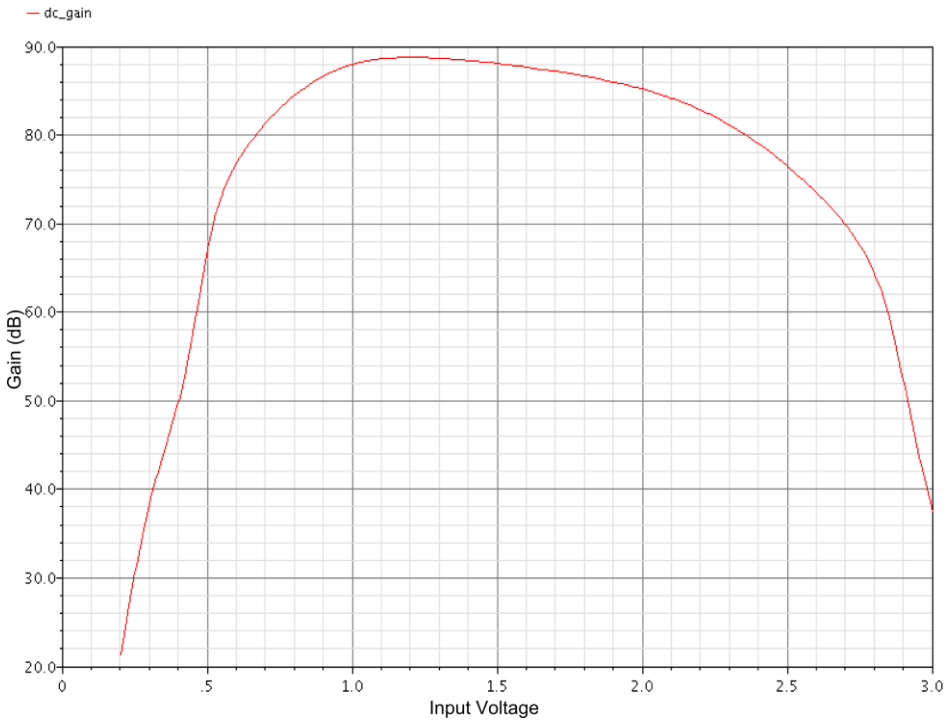

Figure 3.6: The DC gain versus input voltage characteristics of first buffer structure. This buffer has a depletion mode NMOS input pair.

The phase margin of the amplifier is corrected by placing a 3.5pF capacitor to the output node. Figure 3.7 shows the phase margin of the NMOS input buffer. The phase margin is above 60° over the entire operation range.

The operation range of the amplifier is critical because it directly affects the step size and the noise floor of the ADC. It is limited by three factors. On the input side, the input common mode must be larger than the sum of V_{ds} of M_1 and V_{th} of M_2. On the output side, the output swing is limited in between V_{DD}-$V_{ds}(M_7)$-$V_{ds}(M_6)$ and $V_{ds}(M_4)$+$V_{ds}(M_5)$. The drain-source drops of the output stage transistors are inversely proportional to the noise level. Therefore, a considerable drop on the V_{ds} voltages cannot be made, especially regarding the PMOS transistors due to their high contribution to the overall noise. Nevertheless, the output swing is relaxed by increasing the supply voltage to 3.6V. The total V_{ds} drops of M_6 and M_7 are about 0.6V, so the buffer can supply the output up to 3V. The low end of the operation range is normally limited by the input

side. The V_{th} of an enhancement NMOS and the V_{ds} of the tail current source are 0.7V and typically 0.2V respectively. As a result, the input common mode starts from 0.9V for proper operation. A depletion mode NMOS is used as input pair for recovering the limitation. The V_{th} value of a depletion mode NMOS is -0.18V. Thus the lower end of the range is only limited by the V_{ds} drops of M_4 and M_5. The drain source drops of M_4 and M_5 are pushed down to 0.4V. In this case the contribution of the NMOS output transistors to the total noise is acceptable despite the PMOS transistors.

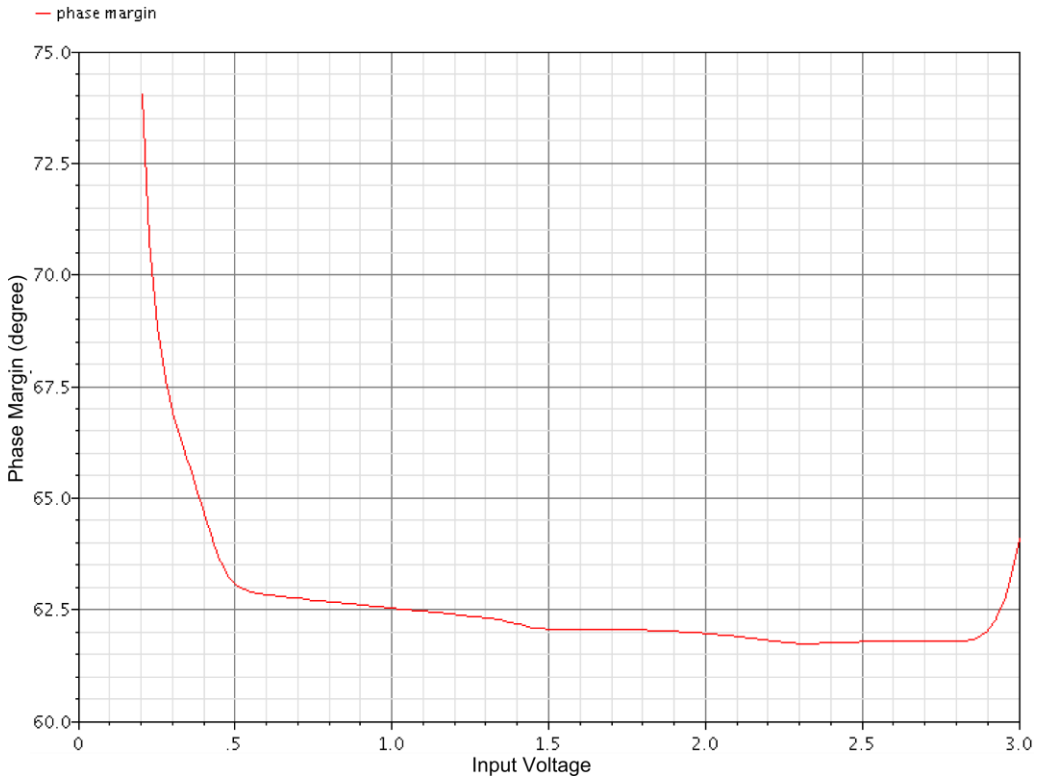

Figure 3.7: The phase margin versus input voltage characteristics of the first buffer. The first buffer has a depletion mode NMOS input pair.

The noise performance of the buffer is optimized by adjusting the overdrive voltages of M_4, M_5, M_6 and M_7. The noise bandwidth is limited by placing a low pass RC filter to the output. The capacitor value is 16pF. This value could not be less otherwise the thermal noise of the filter itself would exceed the system requirements. The resistor in the filter

is a 1.8KΩ high-res poly layer. The cutoff frequency of the filter is adjusted by the resistance value instead of increasing the capacitance so current drawn from the buffer is not increased. Figure 3.8 shows the noise characteristic versus input voltage of the buffer after the filter.

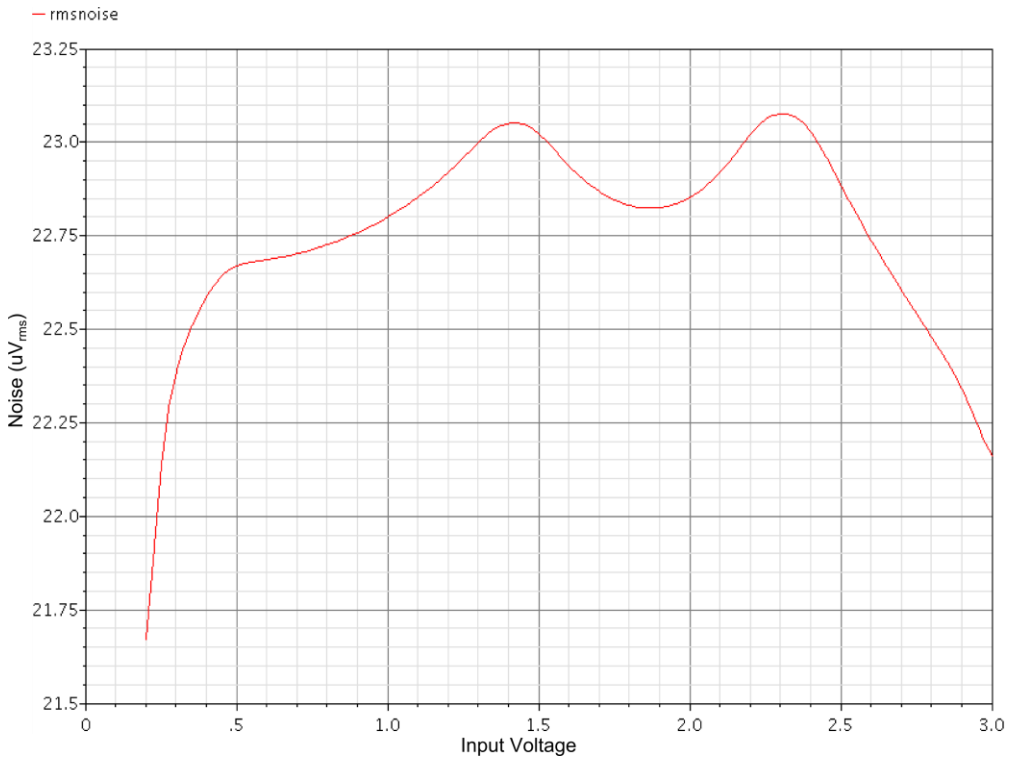

Figure 3.8: The RMS noise versus input voltage characteristic of the first buffer. The first buffer has a depletion mode NMOS input pair.

The slew rate of the amplifier is critical in terms of the circuit speed. The faster the load can be driven, the faster the ADC makes the conversion. In the folded cascode amplifier, the slew rate is decided by the tail current by design. The 16pF filter capacitor and 3.5pF load capacitor are driven by the 120µA tail current folded cascode buffer [24]. The approximate slew rate is calculated as

$$Slew\ Rate = \frac{Q_{total}}{C_{total}} \tag{3.2.2.2}$$

The Q_{total} is I_{tail} x T. The theoretical slew rate is 6,15V/µs. The slew rate is observed as 5,6V/µs in the simulations. This deviation from the calculation is due to the current limiting effect of the resistor in the low-pass filter. The settling of the output, when the most significant bit of the DAC is set, takes 500ns, which is much shorter than the passive driving case. The expense of the speed is power. The total power used for the amplifier is 1.25mW. The cascode transistors are biased with Vncas = 1.4V and Vpcas = 2.0V. These values are selected considering optimal overall performance. Figure 3.9 shows the second folded cascode operational amplifier with the PMOS input pair.

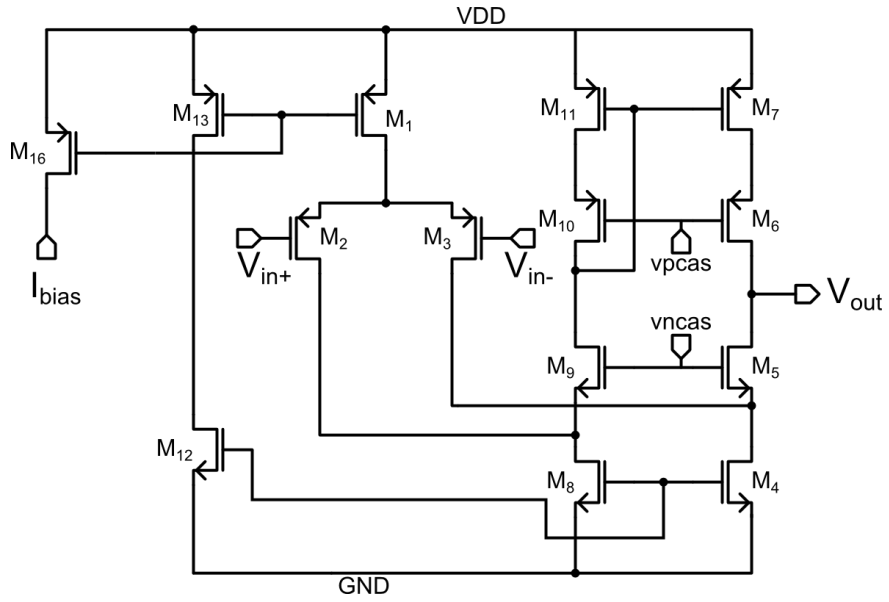

Figure 3.9: The second folded-cascode opamp structure. The input pair is PMOS transistors for decreasing noise. This structure is implemented as a backup in case first buffer fails because of the leakage current of the depletion mode NMOS input pair.

The NMOS input amplifier is the primary buffer, but in case of a failure due to the leakage current of depletion mode NMOS transistors, PMOS input amplifiers are designed as back up. The PMOS transistors have less flicker noise than NMOS transistors; this is why the input stage consists of PMOS transistors [25]. Figure 3.10 shows the gain characteristic of the amplifier. The highest DC gain is significantly lower

than the NMOS buffer as expected due to the lower g_m provided by the PMOS input pair.

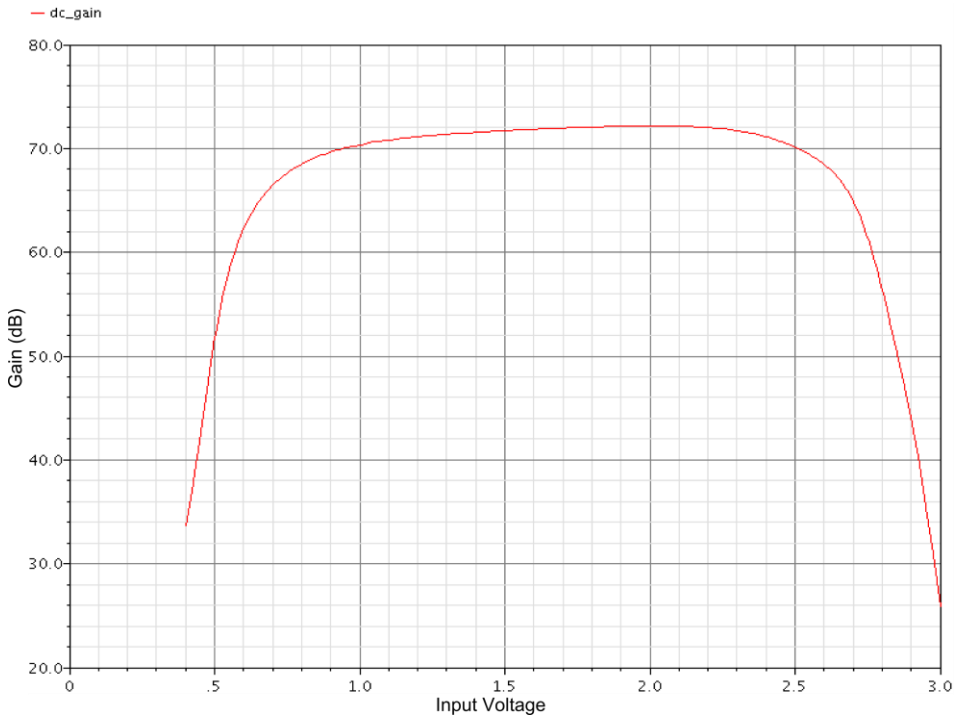

Figure 3.10: The DC gain versus input voltage characteristics of second buffer. This buffer has a PMOS input pair.

The phase margin of the buffer is also ensured to be above 60° over the entire input voltage range. A load of 2.5pF is used for this purpose. The noise level over the input voltage range is below $28\mu V_{rms}$ until 2.8V. After that point on, input transistors begin to turn off and operation is disrupted. When the limitations of the output transistors are also considered, the operation region of the PMOS buffer is between 0.6V to 2.8V. This buffer has the same tail current so that slewing capabilities of both buffers are similar. Therefore, the same timing can be used if the buffer is changed. The power consumption of this buffer is slightly higher than the first one with a figure of 1.42mW. This is due to the additional current supplied to the output stage branches to enhance the phase margin and stability [2]. The cascode transistor voltages in this structure are

Vpcas = 1.8V and Vncas = 1.4V. Both buffers are designed for proper operation under 50mV small signal on the supply. PSRR values of both buffers are kept at 65dB and above over the entire operation range.

Special care is taken for not disturbing the circuit operation while accommodating two buffers at once. Each buffer can be powered down by independent configuration bits from the memory. The current mirrors are turned off via the M_{14} and M_{15} transistors in both opamps. The bias current can be turned off from the bias generator block. The cascode voltages are also pulled up and down for the PMOS and the NMOS transistors respectively. Therefore all branches are turned off in the amplifier. Also the amplifiers are isolated from rest of the circuit by three switches. Figure 3.11 shows the buffer blocks.

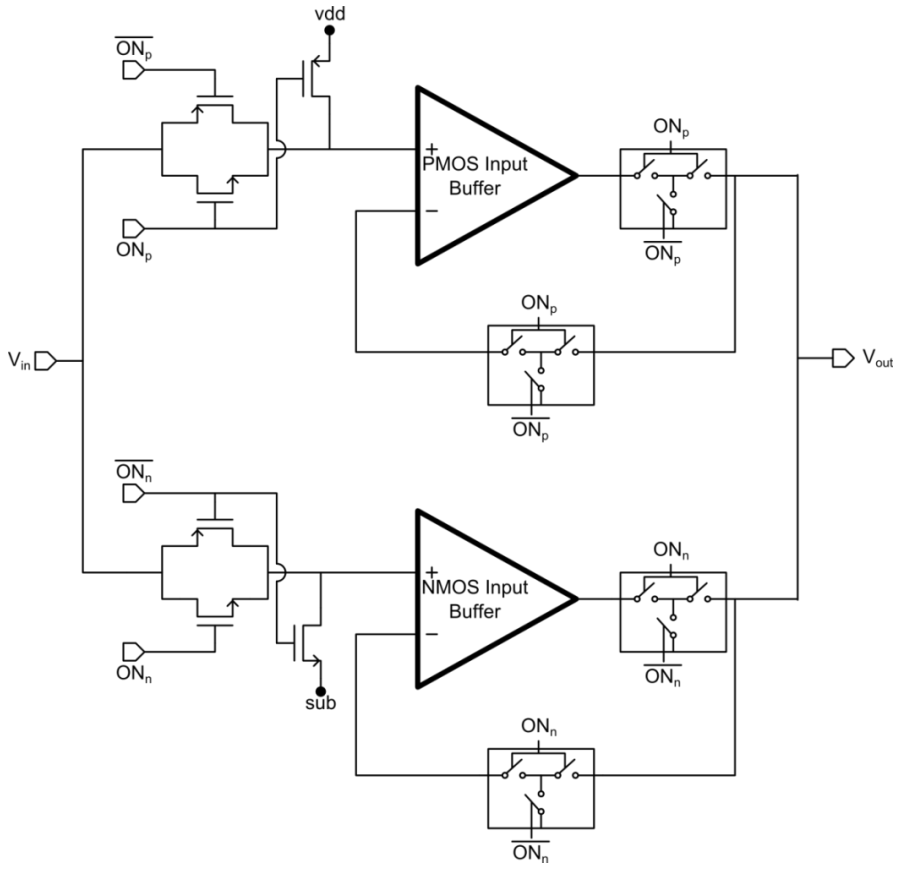

Figure 3.11: The buffer block structure. It consists of two types of buffers. PMOS input buffer is a backup for the NMOS input buffer.

The input of the OFF buffer is cut off from the input port and pulled to high or low depending on the input pair type. The output and the feedback branch of the buffer are also decoupled by using three state switches. Coupling through the off switches are prevented by keeping the intermediate node at substrate voltage in this switch structure. The existence of the output switch does not disturb the amplifier operation as the feedback loop is taken after the switch.

There are two pairs of two types of buffers both at the input and the DAC output. The same types at the input and the DAC output must be ideally identical, but practically as similar as possible. The buffers are grouped according to the input type on the layout in order to enhance matching. The bias currents are mirrored while in the bias generator block. Furthermore, the cascode branch voltages are locally generated with diode connected transistors with the current sent from the bias generator block. These transistors are placed as close as possible to both of the buffers on the layout. Therefore, the same type of buffers operates at conditions as similar as possible. Figure 3.12 shows the layout of the buffers and the low pass filters.

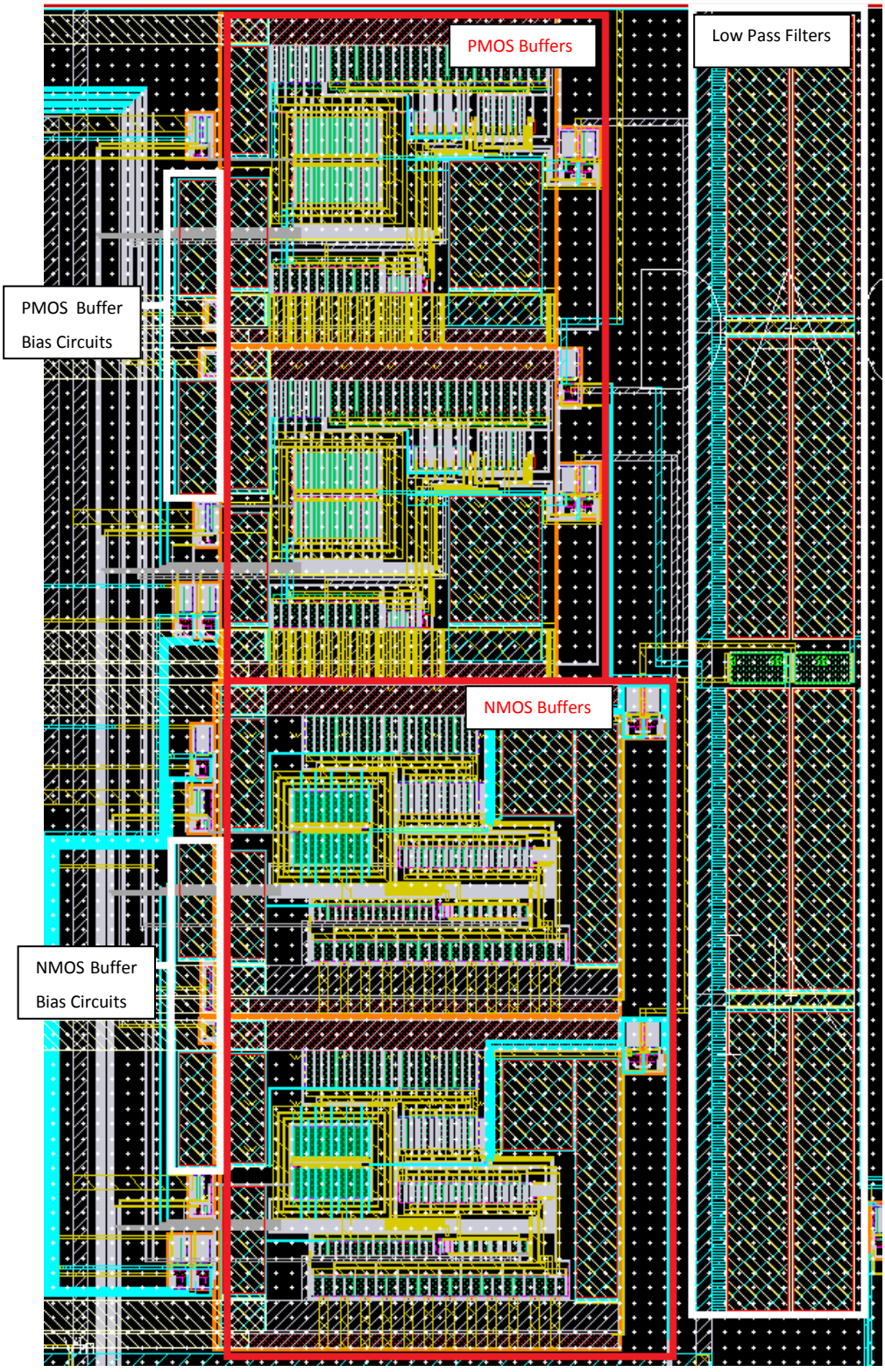

Figure 3.12: The layout of the buffers and the low-pass filters. The buffers are grouped according to type in order to enhance matching. The dimensions are 300µm width and 500µm height in 0.18µm CMOS technology.

3.2.3 Comparator

The comparator is where the conditioned input and the DAC signals are compared and a digital output is generated accordingly. The comparator consists of three differential amplifiers and an inverter chain to make sure the output voltage is either a logic one or zero. Figure 3.13 shows the comparator circuit.

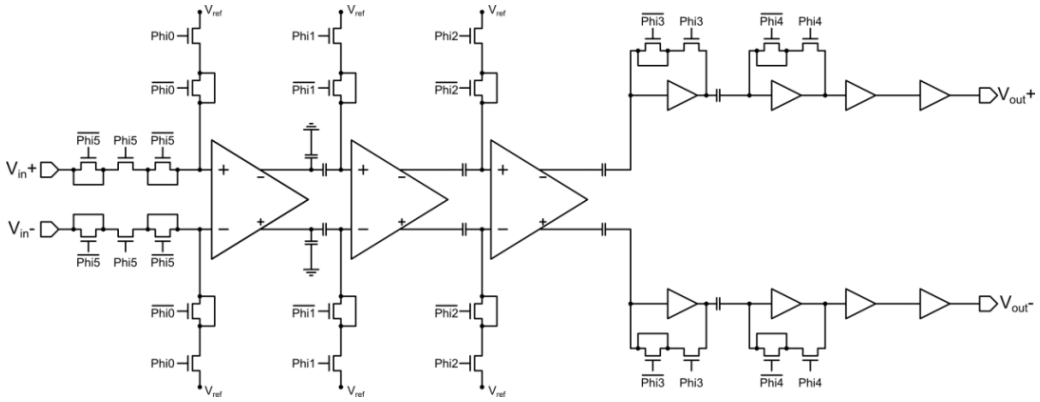

Figure 3.13: The comparator circuit. There are three differential stages followed by four single ended stages [26].

The differential amplifiers have PMOS input stage. The PMOS input pair is preferred due to low flicker noise and low hysteresis nature of the device [25]. A small positive feedback gain of 0.6 is used in order to fasten the decision. The positive feedback amount is not large because it slows down the amplifier to reach a steady state when the input pins are shorted for regeneration. Figure 3.14 shows the differential amplifier. The PMOS input pair has a large W/L value for increasing the gain and decreasing the low-band noise. Cross coupled transistors M_5 and M_6 provide additional gain by positive feedback. The bias current of the amplifier is 25µA. The output stage provides additional gain enhancement.

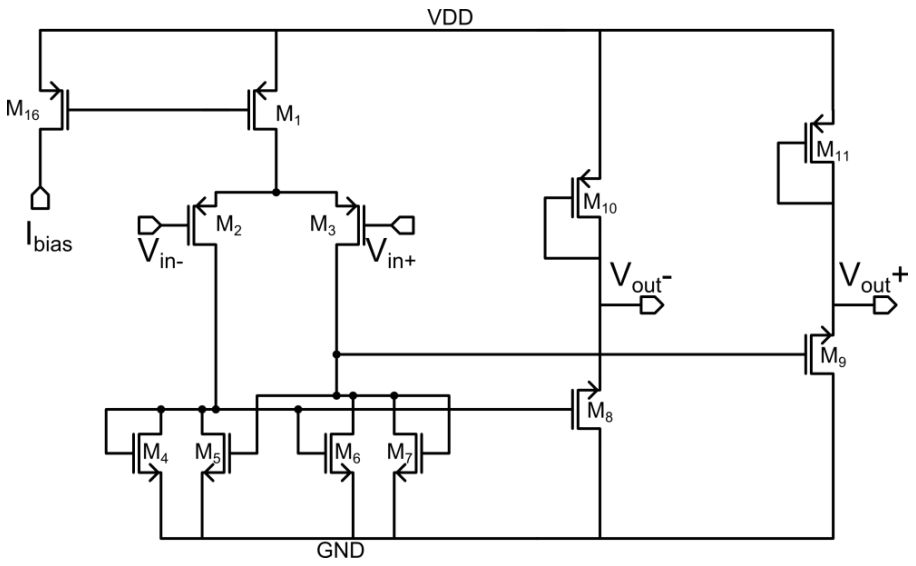

Figure 3.14: The topology of differential stages. A positive feedback of 0.6 is used.

The gain remains above 24dB over the entire input range. This results in a 0.15mV output after three differential amplifiers for an LSB (40µV) input. This output is large enough to be pulled to the rails by the inverter chain. Figure 3.15 shows the gain versus the input voltage curve of the amplifier. The input range of the amplifier is between 0V and 2.9V. Input voltages beyond 2.9V start to turn the input transistors off; as a result the gain drops and the input referred noise increases beyond the step size. The comparator operation and the buffer operation ranges together decide the ADC limits which are 0.4V to 2.9V.

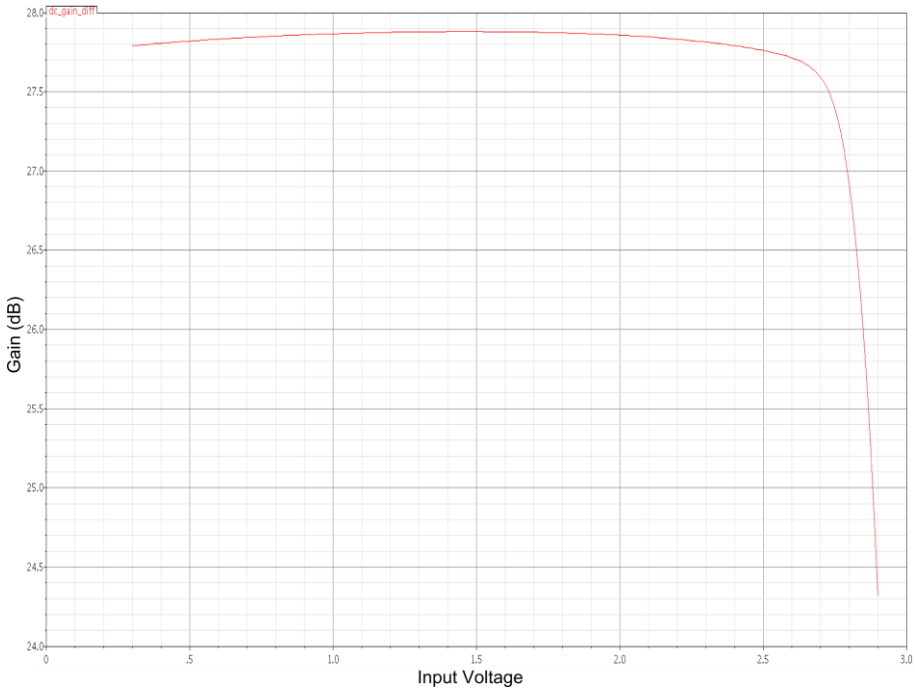

Figure 3.15: The DC gain versus input voltage characteristic of the differential stages.

The output stage consists of four inverters. The task of this chain is to pull the voltage to either supply or ground. The first two inverters' inputs and outputs are shorted in the regeneration phase. Therefore the inverters are kept around 1.85V level at the input-output characteristics. Figure 3.17 shows the input-output characteristics of the inverter. Since the gain at this point is very high, the slightest increment or decrement of the inverter input causes the chain output to be driven to the rails.

The input referred noise decides the sensitivity of the ADC. The noise of each stage is divided by the gain of the previous stage for being referred to the input. Thus, the first stage is dominant in terms of input referred noise. A capacitor is placed to each output of the first stage amplifier besides the CDS capacitors. The noise bandwidth of the first stage is adjusted with these capacitors. Figure 3.16 shows the input referred noise of the comparator. The input referred noise level is below the noise of the previous stages along the operation range.

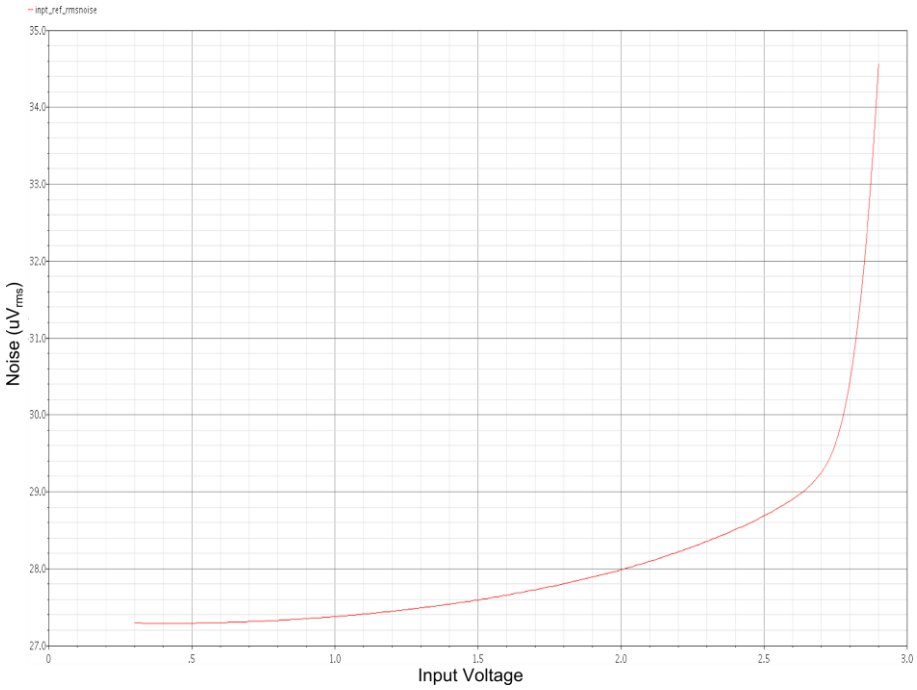

Figure 3.16: The input referred noise versus input voltage characteristics of the comparator.

In order to minimize the offset due to device mismatch, an offset cancellation scheme is applied. Before two voltages are connected to the input of the first amplifier, the comparator is in the regeneration phase where all inputs are set to a V_{ref} (1.8V) value. Any offset is stored on the capacitors at the output. The transition to the decision phase from the regeneration phase is made by turning the switches off with small delays in order to minimize the switching transients. Figure 3.18 shows the control signal timing.

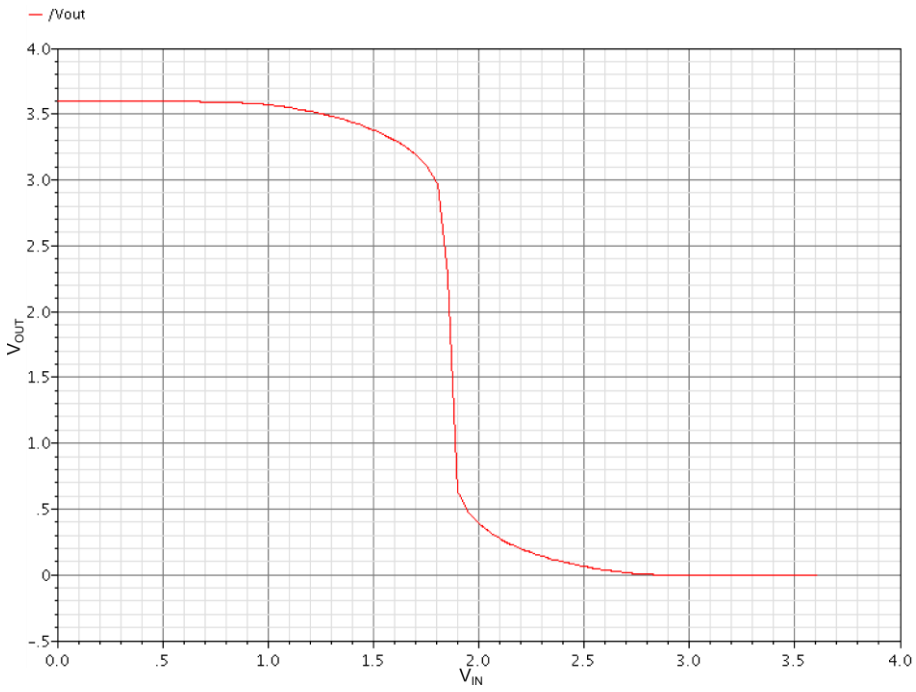

Figure 3.17: The input output characteristics of the inverter.

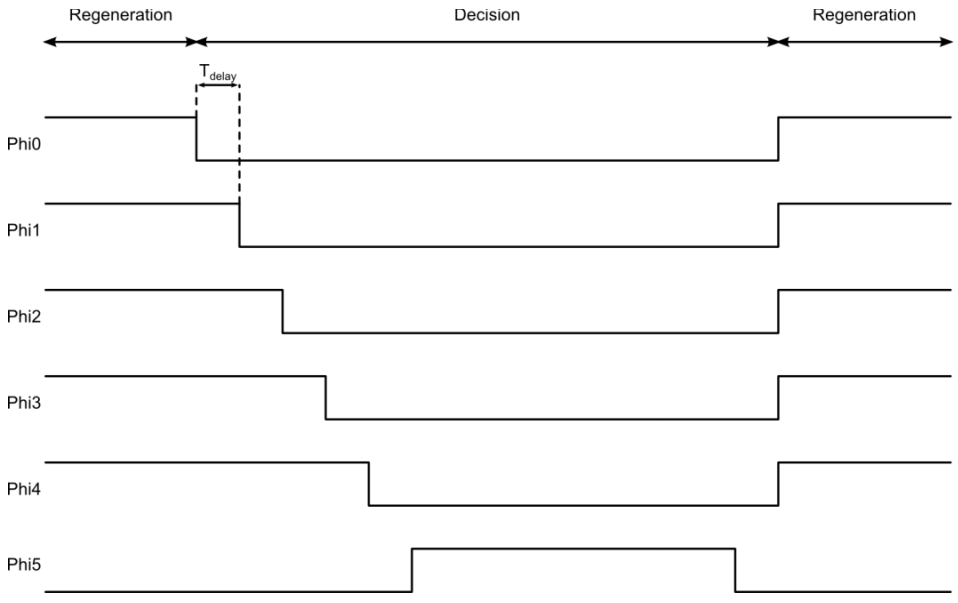

Figure 3.18: The comparator control signals. The signals are delayed for decreasing the switch transients.

The control signals are generated by a digital timing block which is devoted for the comparator only. This block takes a single pulse from the digital controller and generates six signals with selectable delays with respect to the previous edge. Figure 3.18 shows the generated signals. Table 3.1 shows the delay options available.

Table 3.1: The options for signals delay. The delay is designed to be selectable for sake of flexibility.

Binary Code	Delay Amount
00	0,8ns
01	2,22ns
10	3,86ns
11	5,0ns

The selectable delays are created by cascading custom delay cells. Although the design kit provides some delay cells, they draw surge currents from the supply. Large instantaneous currents causes supply droop. The custom cells do not require high currents, yet provide precise delay adjustment. The custom cell consists of an inverter, a capacitor and a schmitt trigger inverter. The inverter is a slow structure with small W/L ratios in order to decrease the surge currents. The inverter drives a capacitor which is fairly small because the inverter driving capability is low. The capacitor is connected to a schmitt trigger inverter. The purpose is to create a sharp edge for the following circuits otherwise the following digital circuits may use too much current due to simultaneously on pull-up and pull-down networks. Figure 3.19 shows the delay cell structure.

The timing block generates all signals with logical complements. The rising and the falling edges are adjusted to overlap at mid-point. These complements are used in the dummy switches next to the actual switches for minimizing the clock feed-through. Figure 3.20 shows the balanced switch buffer structure.

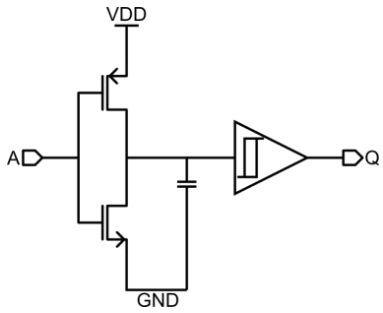

Figure 3.19: The delay cell structure.

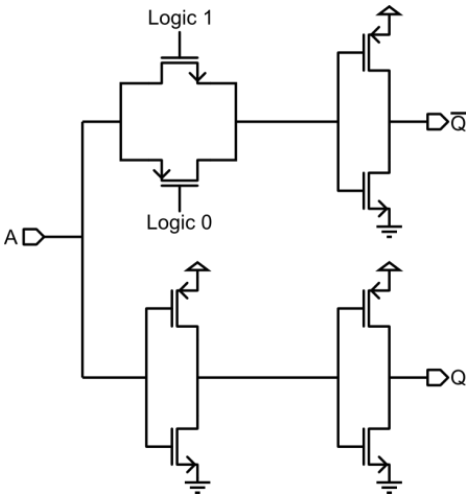

Figure 3.20: The balanced switch driver. The pass transistors are placed for introducing a delay and balancing the output timing.

The power consumption of the comparator is 6.12mW. The minimum sensible voltage difference is at least 35μV. It takes at most 400ns to make a decision when an input of 40μV is applied to the input. The regeneration period depends on how large input voltage was applied in the previous decision phase. The longest time needed for regeneration is 400ns.

Figure 3.21 shows the layout of the comparator. The first three stages are implemented in a way to increase matching between corresponding transistors in differential branches. The inverters at the output stage are stacked to the top of the differential stages. The control signals have very small delays in between their edges. Long routings

may disturb the fine timing of the signals. Therefore, the comparator timing block is placed next to the comparator. Both blocks have similar length for close placement. Figure 3.22 shows the timing block layout.

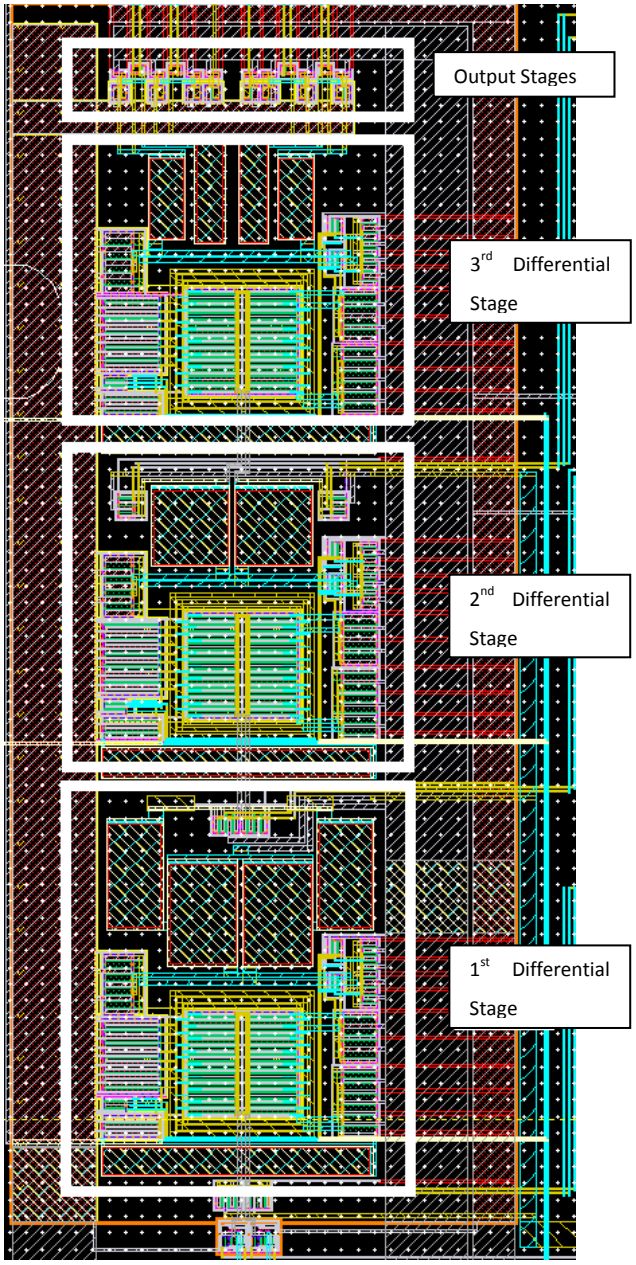

Figure 3.21: The comparator layout. The comparator is implemented in a vertical fashion for enhancing layout utilization. The dimensions are 220µm in width and 500µm in height in 0.18µm CMOS technology.

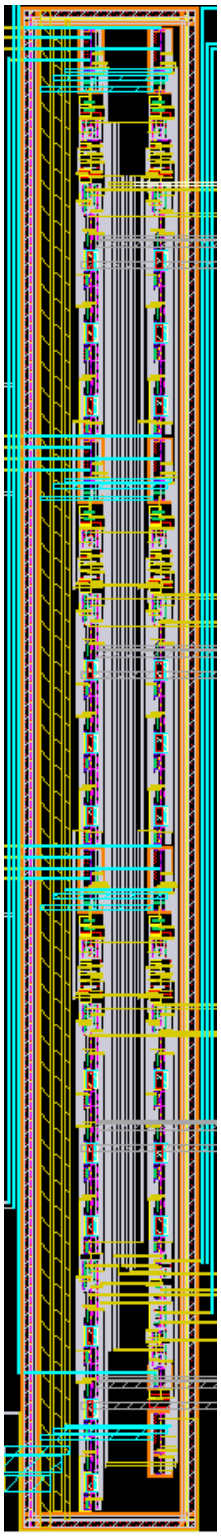

Figure 3.22: The timing block layout. The timing block is implemented in a vertical fashion just as comparator. The comparator and timing block are placed next to each other for not disturbing fine delays of signals. The dimensions are 50µm in width and 500µm in height in 0.18µm CMOS technology.

3.2.4 Bias Generator

The analog blocks in the ADC take currents for bias generation. The current is either used as current bias or locally converted to the voltage domain. The biasing is made in the current domain because it is easily transported to far destinations and hard to be disturbed by the environment. The bias generator consists of seven current steering DACs with various resolutions. Table 3.2 shows the DACs and their properties.

Table 3.2: The bias generator summary.

Range	Resolution	Step Size	Name	Task
13µA-37µA	4-bit	1.5µA	Ibias_comp1	Comparator 1st stage current bias
13µA-37µA	4-bit	1.5µA	Ibias_comp2	Comparator 2nd stage current bias
13µA-37µA	4-bit	1.5µA	Ibias_comp3	Comparator 3rd stage current bias
16µA-45µA	4-bit	2µA	Ibias_dac_buf	DAC buffer current bias
16µA-45µA	4-bit	2µA	Ibias_in_buf	Input buffer current bias
0µA-20µA	5-bit	0.65µA	inbias_buf	Buffer vncas generation current
0µA-20µA	5-bit	0.65µA	ipbias_buf	Buffer vpcas generation current

The bias generator requires a voltage reference for current generation. Figure 3.23 shows the bias generator structure. The reference is taken from pad. Hence, a low noise reference is possible by limiting the noise bandwidth with a large capacitor on the proximity board. Even though the supply is noisy, a quiet reference is sufficient for low noise reference generation, because M_1 decouples the supply from the current mirror. The reference voltage is 2.5V. It is supplied by the references on the proximity cards. Although every current DAC is configurable, the output currents may be changed by altering the reference voltage and as a result, the master current.

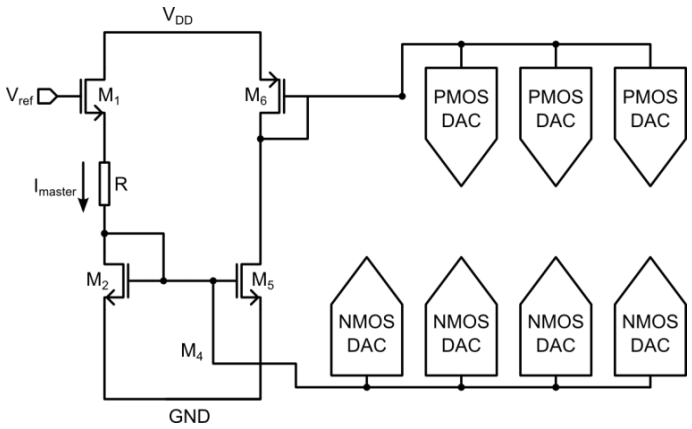

Figure 3.23: The bias generator structure.

There are two groups of DACs: PMOS and NMOS groups. The difference arises because of the different types of transistors that are biased. In order to bias an NMOS transistor, a PMOS network is used and vice versa. Every DAC has similar architecture. The gate voltages of the diode-connected transistors such as M_2 and M_6 are connected to the gate of the DAC transistors. The aspect ratio of those transistors is binary weighted. Therefore, the full range is divided into equal steps. Figure 3.24 shows the DAC structure.

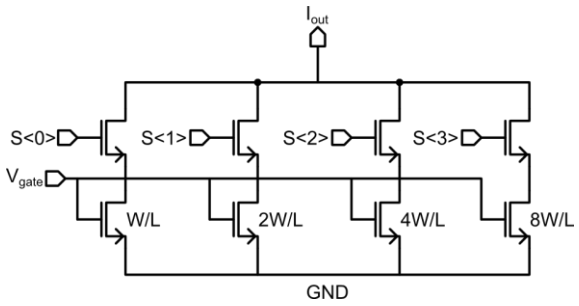

Figure 3.24: The current steering DAC structure.

The output of four DACs is multiplexed. The current is either biasing the NMOS type buffer pair or the PMOS type buffer pair. This is selected by two bits which are controlling two transistors at the DAC output. These DACs are: Ibias_dac_buf, Ibias_in_buf, Inbias_buf, Ipbias_buf. The DAC outputs are adjusted so that the

mid-range level corresponds to the nominal biasing conditions for the target circuits. As a result, the bias conditions can be changed to under or over nominal values. Figure 3.25 shows the output of two current DACs.

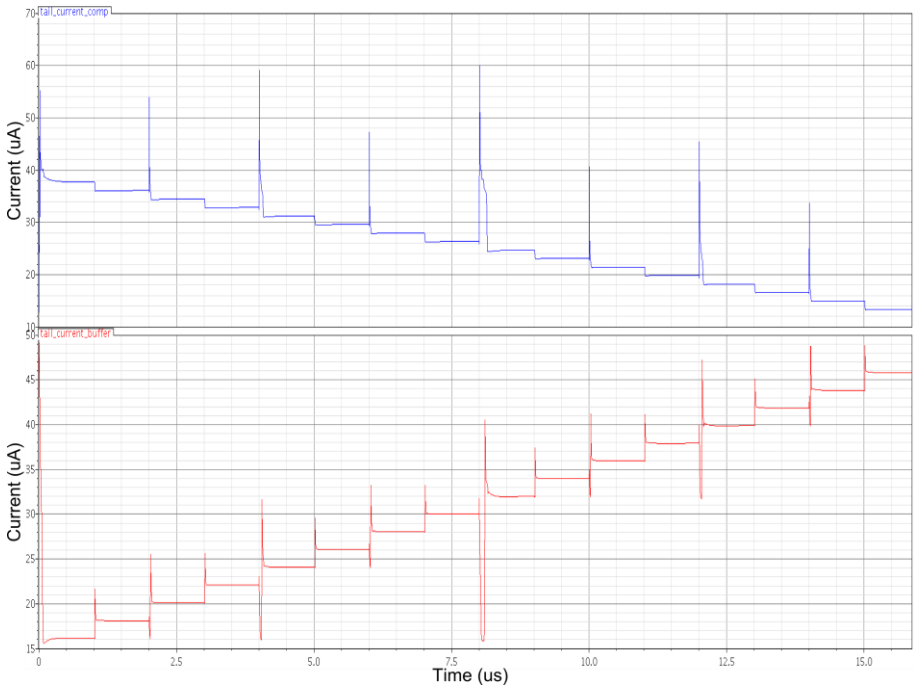

Figure 3.25: The output of the comparator bias and the buffer bias DACs. The output range is swept for four bits.

The overall power consumption of the bias generator is typically 0.36mW. As the currents increase, the power consumption rises. The highest power consumed by the block is 0.54mW when all the DACs are on and set to full scale.

Figure 3.26 shows the layout of the bias generator block. The current steering DACs are constructed with large transistors to increase matching. Every block in the ADC has guard rings to decrease substrate noise. Similarly, the bias generator has a guard ring. The digital signal level is between 0V – 1.8V whereas analog signal levels are 0V – 3.6V. For voltage translation, level shifters are used. Each major block has accompanying utility circuits which consist of level shifters and buffers.

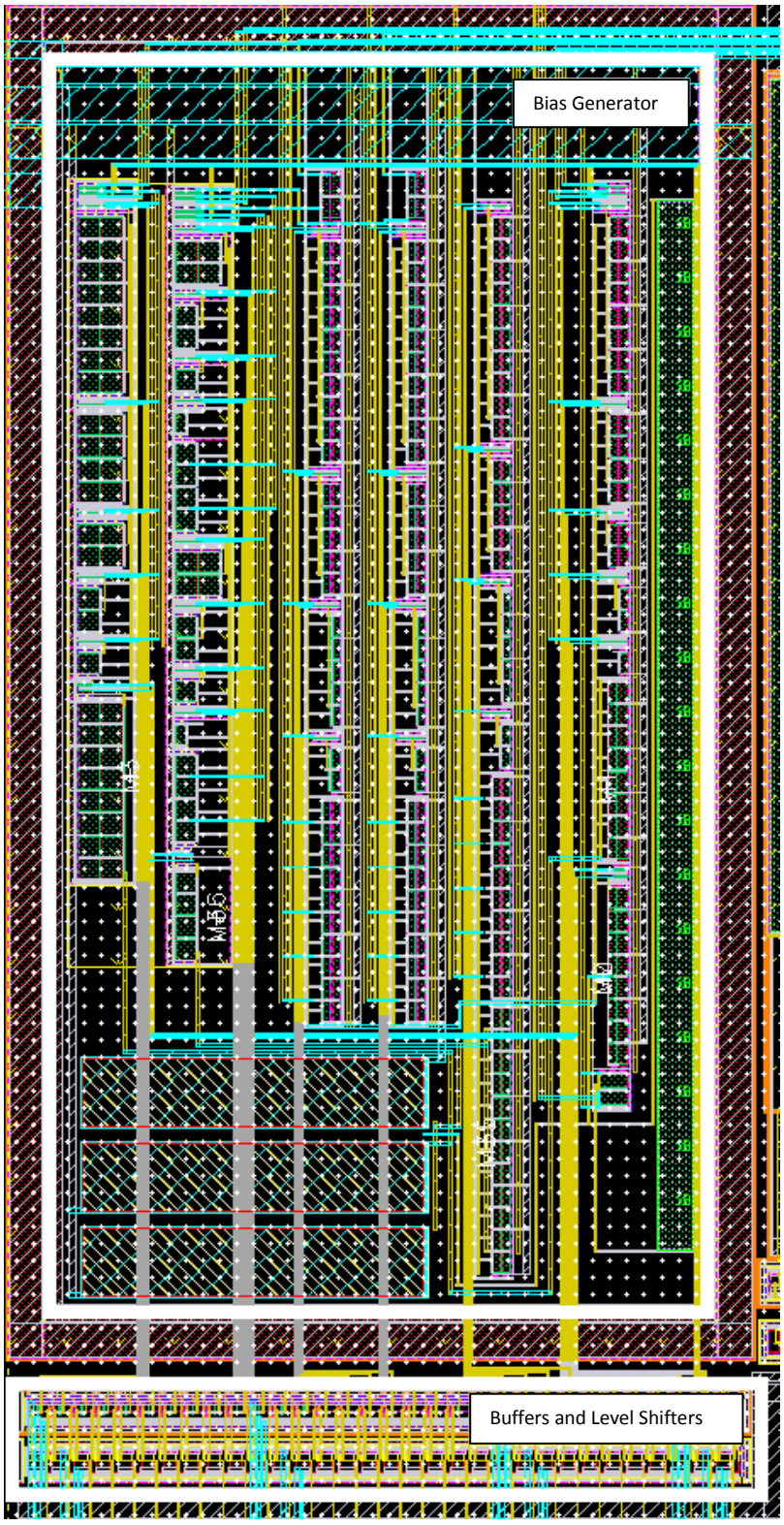

Figure 3.26: The bias generator layout. The current steering DACs are built using large transistor dimensions in order to limit mismatch. The dimensions are 250µm in width and 500µm in height in 0.18µm CMOS technology.

3.3 Digital Blocks

In this section, the implementation of the digital controller is explained. The controller is divided into five subsections: Successive approximation register, timing generator, output data serializer, serial interface and memory, and synchronizer. The successive approximation register generates the control word for the DAC. The timing generator creates the pulses needed by the other digital blocks as well as the analog blocks. The output data serializer block gives the converted digital data serially to the user. The serial interface and memory takes and keeps the static bits for the digital circuits and analog circuits. The synchronizer conditions the input signals with undefined timing.

3.3.1 Successive Approximation Register

The SAR consists of two 16-bit registers: Trial register and storage register. The trial register starts with 1000_0000_0000_0000 value to each conversion. After completion of each bit decision, all values in the register are shifted to right by one bit. A zero is shifted in to the MSB. After 16-bit decisions, the trial register returns to the initial state. The storage register is an all-parallel register. There is no shifting operation.

Table 3.3: SAR operation scheme. The trial and storage registers are updated according to comparator output at the end of each bit comparison.

Bit	Comp. Output	Trial Register	Storage Register	SAR Output
16	1	1000_0000_0000_0000	0000_0000_0000_0000	1000_0000_0000_0000
15	0	0100_0000_0000_0000	1000_0000_0000_0000	1100_0000_0000_0000
14	0	0010_0000_0000_0000	1000_0000_0000_0000	1010_0000_0000_0000
13	1	0001_0000_0000_0000	1000_0000_0000_0000	1001_0000_0000_0000
12	1	0000_1000_0000_0000	1001_0000_0000_0000	1001_1000_0000_0000

Initially all bits in this register are zero. After each bit decision, the comparator output is checked. If the comparator output is one, all bits of trial register, which are one, are

stored. The bits with zero value are not taken into account. If the comparator output is zero, no bits are stored. A bitwise OR operation is performed to outputs of both registers. The resulting 16-bit word is the SAR output. Table 3.3 shows an example of the SAR operation. The successive approximation algorithm is run by this scheme. The SAR also has a 16-bit test bus input and a test select bit coming from memory. The select bits control the multiplexers which either connect the actual SAR output or the 16-bit test bus to the DAC. This property is added for testing the DAC.

3.3.2 Timing Generator

The timing signals for all digital and analog blocks are produced in this circuit. There are two 5-bit counters which keep track of time. One of the counters keeps which bit is being decided. This counter is called turn counter. It increases by one when the comparator decision is made. It loads zero after the 16^{th} turn. The other counter is called duration counter. It keeps track of the expired time in each turn. The duration count increases by each clock and loads a zero when a new turn begins. The duration counter is enabled by the external enable input from the pad. The timing generator creates all outputs according to duration count and turn count. Table 3.4 shows the list of the output signals and their descriptions. There are two references for each bit time in the timing generator. The first reference is called turn reference and the other one is called compare reference. These references are 5-bit static words from memory. The compare reference indicates when the ADC goes into comparison phase and the turn counter indicates when the bit conversion is finished. There are 32 total reference words for all bits. By using this system, the settling time of the DAC, the comparison time and the regeneration time of the comparator can be decided separately for each bit. More importantly, the references can be changed while testing.

Table 3.4: The timing generator output signals.

Signal Name	Target Block	Description
turn_count_en	Turn Counter	Enables count up
turn_count_ld_zero	Turn Counter	Loads zero
dur_count_ld_zero	Duration Counter	Loads zero
compare	Comparator Timing Block	Compare pulse
SAR_initialize	SAR	Returns to initial state
SAR_clk	SAR	Clock for SAR operations
shift_en	SAR	Enables shifting for trial register
store	SAR	Enables storage register to save value
out_reg_load	Output Register	Loads SAR output to load register
test_out	Main Test Multiplexer	Test output for timing generator

Figure 3.27 shows the timing signals generated by the digital controller. The 10^{th} and 9^{th} bit decisions are shown. The turn counter starts from zero for the 16^{th} bit. The turn reference and the compare reference are set to 19 and 10 for the 10^{th} bit respectively. For the 9^{th} bit the turn reference is 15 and the compare reference is 8.

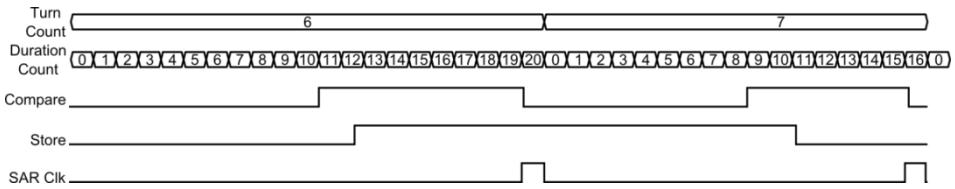

Figure 3.27: The timing signals for 10^{th} and 9^{th} bits. Turn reference and compare reference are different for each bit.

The time before the compare pulse is controlling the DAC settling and the regeneration time of the comparator while the compare pulse width decides the comparison time of the ADC. The precision of the time adjustment depends on the clock period. The current

system is designed for 20MHz clock frequency. Asynchronous signals are designed with selectable delays in order to ensure proper operation on silicon.

The inputs of the timing block carries out feedback and test functions. The comparator result is taken as an input for deciding the next state of the SAR and generating the control signals accordingly. The test functions are adjusted, so that each block can be tested standalone and any input combination can be created. In other words, timing generator is by-passed and input signals of other blocks are supplied from the pad for flexible testing.

3.3.3 Output Data Serializer

The serialization of the SAR output takes place in this block. It consists of two identical registers and small, local control logic. The registers are capable of loading data in parallel and shifting to right. When the iteration is finished for all 16 bits, the timing generator exerts the load signal and the data is transferred to the serializer. Meanwhile, a 16-bit word of 1111_1111_1111_1111 is loaded to the second shift register. The local control logic shifts both registers to right. As the registers shift to right, data and the secondary register pops out the bits starting from LSB. The shift operation is synchronized to the system clock. The shift operation ends when the secondary register is cleaned of 1's. The serial output is two wires, serial data out and serial latch.

3.3.4 Serial Interface and Memory

The serial interface is a synchronous, full duplex interface. It has four wires for communication: serial data input, shift enable, serial data output, and serial clock. The word length of the interface is 20-bit. The top four bits are the address for the memory. The rest 16 bits are data. Figure 3.28 shows the timing scheme of the serial interface.

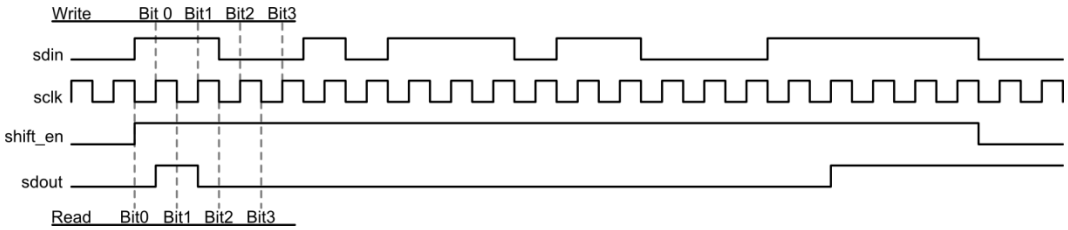

Figure 3.28: The serial interface timing. The ADC does all operations at rising edge. The external controller should operate at falling edge of the clock.

The serial data is always LSB to MSB. The ADC interface does all activities on the rising edge of the clock. As a result, the external controller can make writing and reading at the falling edge of the clock so sufficient time is left for the settling of signals between a writing and reading. The serial data output is a checking structure rather than a real read port. Only information which can be read is previous word written to the serial interface. The previous word written and the word read can be compared and the reliability of interface can be decided.

The memory consists of 16 words. Each of them is 16 bits long. The data is written to the memory by exerting a write pulse after writing each word to the serial interface. The write pulse is called mem_clk. For ensuring proper settling of the data and the address busses in the memory, the mem_clk pulse must be exerted two clock cycles serial interface operation.

The ADC is configured by writing to memory. Table 3.6 shows the memory map of the digital controller. Table 3.5 shows the explanation for each bit.

Table 3.5: The description of configuration bits.

Name	Description
comp_b_sel<1:0>	Adjusts the delay time between compare pulse and SAR clock
SAR_T_Sel	Selects the test mode of SAR and bypasses the output
Test_Sel_s_tc<1:0>	Mux selection bits for counter and synchronizer outputs
Test_o_s	Main mux selection bits for timing generator and counter outputs
Test_sel_sg<2:0>	Mux selection bits for timing generator internal signals
com_t_sel	Select bit for giving external compare pulse to comparator
com_res_t_sel	Select bit for giving comparator result externally for testing SAR
turn(1-16)_ref<4:0>	Turn references for all turns from 1 to 16
dig_drv<2:0>	Digital pad drive strength for latch out and serial data out
dig_drv<5:3>	Digital pad drive strength for sdout and digi test out
comp(1-16)_ref<4:0>	Duration references for all turns from 1 to 16
p_bias	Selection to bias PMOS buffers and kill NMOS buffer bias
pdb_db_p	Power_down_bar for PMOS DAC buffer
pdb_ib_p	Power_down_bar for PMOS Input buffer
pdb_bg	Power_down_bar for bias generator
pdb_db_nn	Power_down_bar for NMOS DAC buffer
pdb_ib_nn	Power_down_bar for NMOS Input buffer
Vin_byp	Select bit for connecting input directly without buffer
Vtest_oen	Output enable for analog test output
out_sel	Select bit for reversing comparator polarity
pdb_com	Power_down_bar for comparator
Vtest_Sel<7:0>	Select bits for analog test output
din_test<15:0>	The word which replaces SAR output for testing
comp_b_S<1:0>	Delay setting for comparator pulse
comp_0_S<1:0>	Delay setting for comparator pulse
comp_0_1_S<1:0>	Delay setting for comparator pulse
comp_1_2_S<1:0>	Delay setting for comparator pulse
comp_2_3_S<1:0>	Delay setting for comparator pulse
comp_3_4_S<1:0>	Delay setting for comparator pulse
comp_4_5_S<1:0>	Delay setting for comparator pulse
ibias1_comp_S<3:0>	Current setting for comparator first stage bias
ibias2_comp_S<3:0>	Current setting for comparator second stage bias
ibias3_comp_S<3:0>	Current setting for comparator third stage bias
ibias_db_S<3:0>	Current setting for DAC buffer bias
ibias_ib_S<3:0>	Current setting for Input buffer bias
inbias_b_S<4:0>	Current setting for buffer cascode voltages
ipbias_b_S<4:0>	Current setting for buffer cascode voltage

Table 3.6: The memory map of the ADC. All blocks can be configured by writing to memory.

	Bit															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	turn0_ref<4:0>					com_res_t_sel	com_t_sel	Test_sel_sg<2:0>			Test_o_s	Test_Sel_s_tc<1:0>		SAR_T_Sel	comp_b_sel<1:0>	
1		turn3_ref<4:0>					turn2_ref<4:0>					turn1_ref<4:0>				
2	dig_drv<0>	turn6_ref<4:0>					turn5_ref<4:0>					turn4_ref<4:0>				
3	dig_drv<1>	turn9_ref<4:0>					turn8_ref<4:0>					turn7_ref<4:0>				
4	dig_drv<2>	turn12_ref<4:0>					turn11_ref<4:0>					turn10_ref<4:0>				
5	dig_drv<3>	turn15_ref<4:0>					turn14_ref<4:0>					turn13_ref<4:0>				
6	dig_drv<4>	comp2_ref<4:0>					comp1_ref<4:0>					comp0_ref<4:0>				
7	dig_drv<5>	comp5_ref<4:0>					comp4_ref<4:0>					comp3_ref<4:0>				
8	p_bias	comp8_ref<4:0>					comp7_ref<4:0>					comp6_ref<4:0>				
9	pdb_db_p	comp11_ref<4:0>					comp10_ref<4:0>					comp9_ref<4:0>				
10	pdb_ib_p	comp14_ref<4:0>					comp13_ref<4:0>					comp12_ref<4:0>				
11	Vtest_Sel<3:0>				pdb_com	out_sel	Vtest_oen	Vin_byp	pdb_ib_nn	pdb_db_nn	pdb_bg	comp15_ref<4:0>				
12	din_test<15:0>															
13	Vtest_Sel<5:4>	comp_4_5_S<1:0>			comp_3_4_S<1:0>		comp_2_3_S<1:0>		comp_1_2_S<1:0>		comp_0_1_S<1:0>		comp_0_S<1:0>		comp_b_S<1:0>	
14	ibias_db_S<3:0>				ibias3_comp_S<3:0>				ibias2_comp_S<3:0>				ibias1_comp_S<3:0>			
15	Vtest_Sel<7:6>	ipbias_b_S<4:0>						inbias_b_S<4:0>					ibias_ib_S<3:0>			

3.3.5 Synchronizer

The input signals such as reset and enable do not have to be synchronized to the system clock. There is also no restriction about the shape of the input signal. In order to ensure proper operation of the digital circuitry, the input signals are sampled with the system clock at three levels. The purpose is to prevent signal meta-stability and to correct the timing to satisfy setup and hold times. As the signal is sampled, the risk of meta-stability or timing problems decreases. The test inputs and serial interface signals are not synchronized. The serial interface signals are restricted to be synchronized among themselves. The test inputs need very fine timing and the synchronization process restricts the input signal with the clock periods.

3.4 Top Level Integration

The integration of the analog blocks and the digital blocks require interface circuits. The need mainly arises from the supply differences of the analog and the digital circuits. The analog supply is 3.6V whereas the digital one is 1.8V. In order to convert signal levels,

level shifters are used. There are two types of level shifters, high-to-low and low-to-high. Figure 3.29 and Figure 3.30 show low-to-high and high-to-low level shifters, respectively.

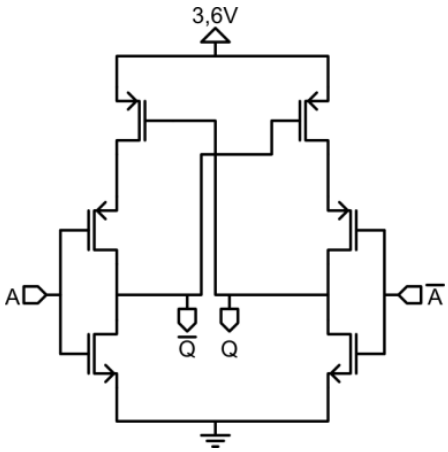

Figure 3.29: The low-to-high level shifter structure. This block is used for translating 1.8V signal to 3.6V domain.

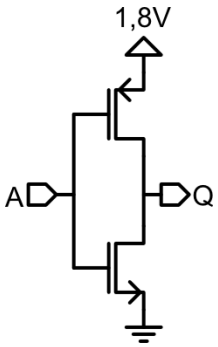

Figure 3.30: The high-to-low level shifter structure. This block is used for translating 3.6V signal to 1.8V domain.

The substrate in the entire chip is decoupled from the ground in order to prevent current injection to substrate and decrease substrate noise. Every block has its own guard ring for the same purpose.

The standard digital output pads from the design kit connect the substrate to ground. Instead of manipulating the design kit, digital output drivers are designed and an analog pad is connected to the output of the driver. The strength of the driver is adjustable for adapting to varying load during the test, like cable length.

The pad frame consists of 44 pads most of which are power pads. The supply and the ground pairs of major analog blocks and the digital controller are separated inside the chip. They are to be shorted on the PCB on a large plane for minimizing cross-talk. Pads are placed at each 254μm, which correspond to 10 mils, so that a trace corresponding to each pad can be fabricated on PCB. Since the circuit is pad limited, pads are distributed to four sides of the circuits. Figure 3.31 shows the top level layout.

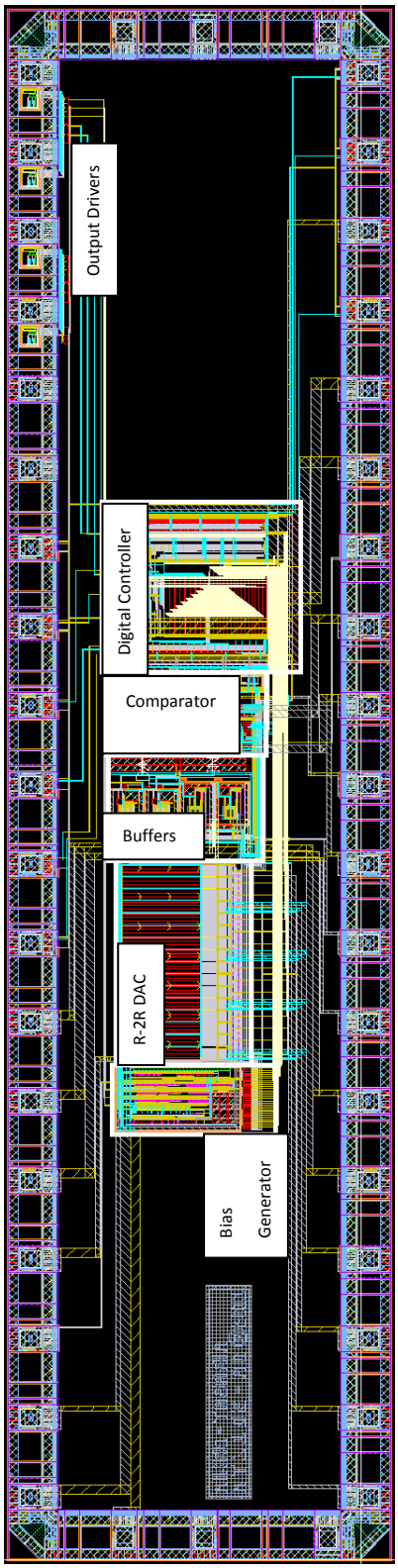

Figure 3.31: The top level layout of the SAR ADC. Building blocks are shown on the figure. The dimensions are 1mm in height and 5mm in width with 0.18µm CMOS technology.

3.5 Literature Comparison and Summary

Two ADCs are submitted to foundry for production. All of the implementation is the same for two versions except the capacitor sizes of low-pass filters. The 16-bit ADC has a 16pF capacitor while 14-bit ADC has a 4pF capacitor.

The 16-bit ADC is a high performance converter. The sampling rate is 128Ksps. The noise level is about 1.3 LSB in dual buffer configuration and 1.0 LSB in single buffer configuration. The DNL is kept below ±1 LSB. It is designed for low speed sensors such as temperature sensors or small infrared sensor arrays. This type of sensors may operate extremely slowly depending on the application. The ADC speed must be scaled down in order to save power during extremely slow operation of the sensor. The SAR ADCs in the literature have a capacitive DAC and those switched capacitor DACs have a minimum operation speed due to leakage currents [11] [13] [10]. The R-2R ladder enables the designed SAR ADC work at low frequencies down to almost DC. Furthermore, the modification of the DAC enables high resolution conversion by taking advantage of the iterative SAR ADC operation.

The 14-bit ADC is a higher speed version of the same design with a sampling rate of 700Ksps. The noise floor is around 1.3 LSB for dual buffer configuration where it is expected to be 1.0 LSB for single buffer configuration. The DNL is well below ±1 LSB. The sampling rate is high enough for digitizing the analog output of a 160x120 QQVGA array using one ADC. The power consumption of the 14-bit version is expected to be around 30mW. It introduces a gain error as mentioned in Section 2.5. But since it is the same error for every pixel, it is not deteriorating the image quality.

Table 3.7: The ADCs used for imaging from the literature. The SAR ADC designed in this thesis is given in the last line for better comparison, where it is seen that the proposed SAR ADC has a much higher resolution.

Architecture	Array Format	Resolution	Power	Normalized Power	Conversion Speed
Col. Parallel SAR [10]	64x64	8-bit	736uW	1.84mW	50Ksps
Col. Parallel Σ-Δ [27]	1696x1212	12-bit	180mW	17mW	430Ksps
Standalone Cyclic ADC [28]	700x1	10-bit	21.6mW	21.62mW	14Msps
Col. Parallel SAR [13]	3840x2160	10-bit	500mW	20.83mW	64.8Ksps
Standalone Pipeline ADC [29]	256x256	12-bit	55mW	55mW	6.3Msps
Col. Parallel MRSS ADC [30]	400x330	10-bit	38mW	15.2mW	19Ksps
Col. Shared SAR ADC [11]	2624x1968	9-bit	111mW	6.78mW	8.3Msps
14-Bit SAR ADC	**160x120**	**14-bit**	**30mW**	**30mW**	**700Ksps**
16-Bit SAR ADC	**80x40**	**16-bit**	**10mW**	**40mW**	**128Ksps**

Table 3.7 shows the performance comparison of the SAR ADC with the other ADCs in the literature. The ADC architecture, the supported array format, resolution, speed, and the power consumption are given in separate columns in the table. In order to have a fair judgment the power consumptions are normalized according to the needed speed for digitizing a 160x120 array format. The normalization is basically the calculation of the total power consumption calculated if each of those ADCs were to digitize an output of a QQVGA array.

In conclusion, the ADCs designed in this work are much higher resolution than the other imaging converters in the literature. This is realized without an excessive increase in power consumption. Also, a resistive DAC is used instead of a capacitive DAC for supporting low frequency operation where the other examples of this device in literature employ a capacitive DAC.

CHAPTER IV

TEST OF THE SAR ADC

This chapter explains the test setup designed for the SAR ADCs. The test setup is able to characterize both ADCs. Firstly, information about the test setup is given in Section 4.1. Secondly, the proximity card is explained in Section 4.2. Finally, tests that are going to be performed are explained in Section 4.3.

4.1 Test Setup

A PC controlled test setup is designed for the SAR ADC test. The ADC resides on a proximity card which is interfaced to PC with a commercial FPGA card called OPEL KELLY XEM 3010. The FPGA card is accessible from computer through a graphical interface. Figure 4.1 shows the test setup.

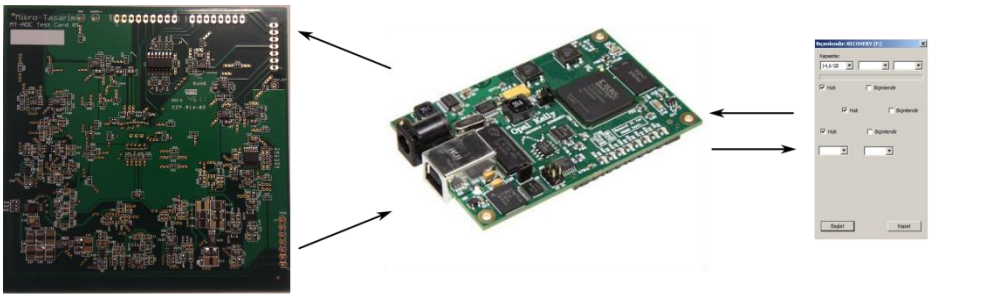

Figure 4.1: The test setup consists of a custom designed card and commercial components [31].

Test mode is selected on the GUI. The necessary instruction set is sent to FPGA Card. The firmware applies the changes and reads the ADC output. The result is sent to GUI and stacked in a text file. The text file is to be analyzed using MATLAB after completion.

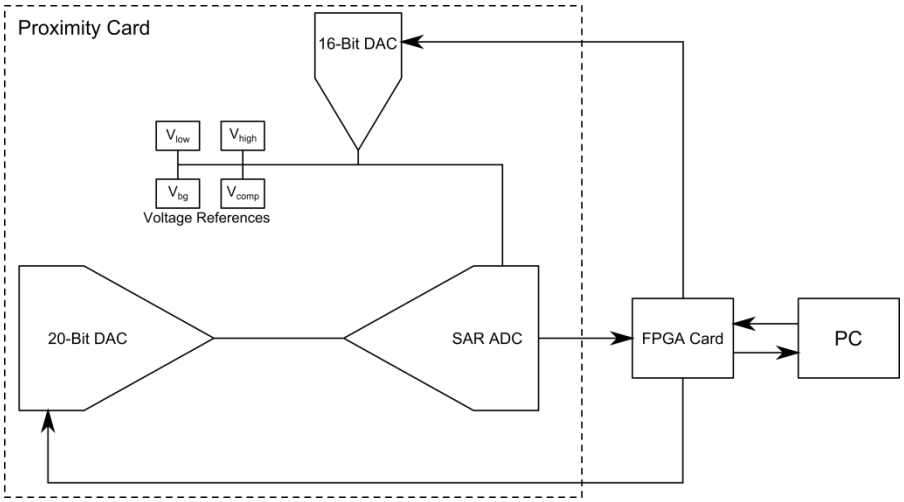

Figure 4.2: The test setup diagram.

Figure 4.2 shows the diagram of the test setup. The voltage biases of the SAR ADC can be produces either by the voltage reference ICs or the 16-bit DAC on the proximity card. The 16-bit DAC is controlled by the PC through the FPGA Card. Therefore various bias conditions may be tested by sending an instruction from PC. This is an advantage for initial characterization tests. Once the SAR ADC is characterized, lower noise, fixed voltage references may be used for better performance. The SAR ADC input is connected to the 20-bit DAC. This very high resolution DAC is also controlled by PC through FPGA Card. The input voltage can be fixed to desired voltage levels for various measurements or swept for input-output characterization. The resolution is sufficient for testing a 16-bit ADC as each voltage level is covered by at least three sub-steps of the 20-bit DAC.

4.2 Proximity Card

The card designed for testing has various utilities for easy testing. There are a number of components such as voltage references, analog buffers, digital buffers, DACs, and voltage regulators. The resolution of the components such as DACs is picked appropriately for testing a 16-bit ADC. The ADC die is to be directly glued and wire

bonded to the card. All electronics and chip are on the same card for compact and robust testing. Table 4.1 shows the list and the descriptions of the utilities on the card.

Although there are many components on the card, not all have to be populated for operation. Redundant footprints are added for applying different scenarios with same PCB but different components. The card has only digital I/O's and a single supply connection of 7V. Figure 4.3 shows the produced card for testing.

Table 4.1: The utilities available on the proximity card.

Name	Count	Description
LT1762	7	Adjustable power supply for different power domains on the card
AD8601	5	Voltage buffer for references and voltage input, also amplifier if desired.
LT6650	2	400mV to 2.9V (adjustable) voltage reference for Vlow and Vhigh inputs
ADR130	1	500mV voltage reference for Vlow input
LT6655	1	3V voltage reference for Vhigh input
ADR361	2	2.5V voltage reference for Vhigh input and Vref_bg input
LM4120	1	1.8V voltage reference for Vref_comp input
DAC1220	1	20-bit DAC for Vin
AD5664	1	16-bit 4 channel DAC for reference generation

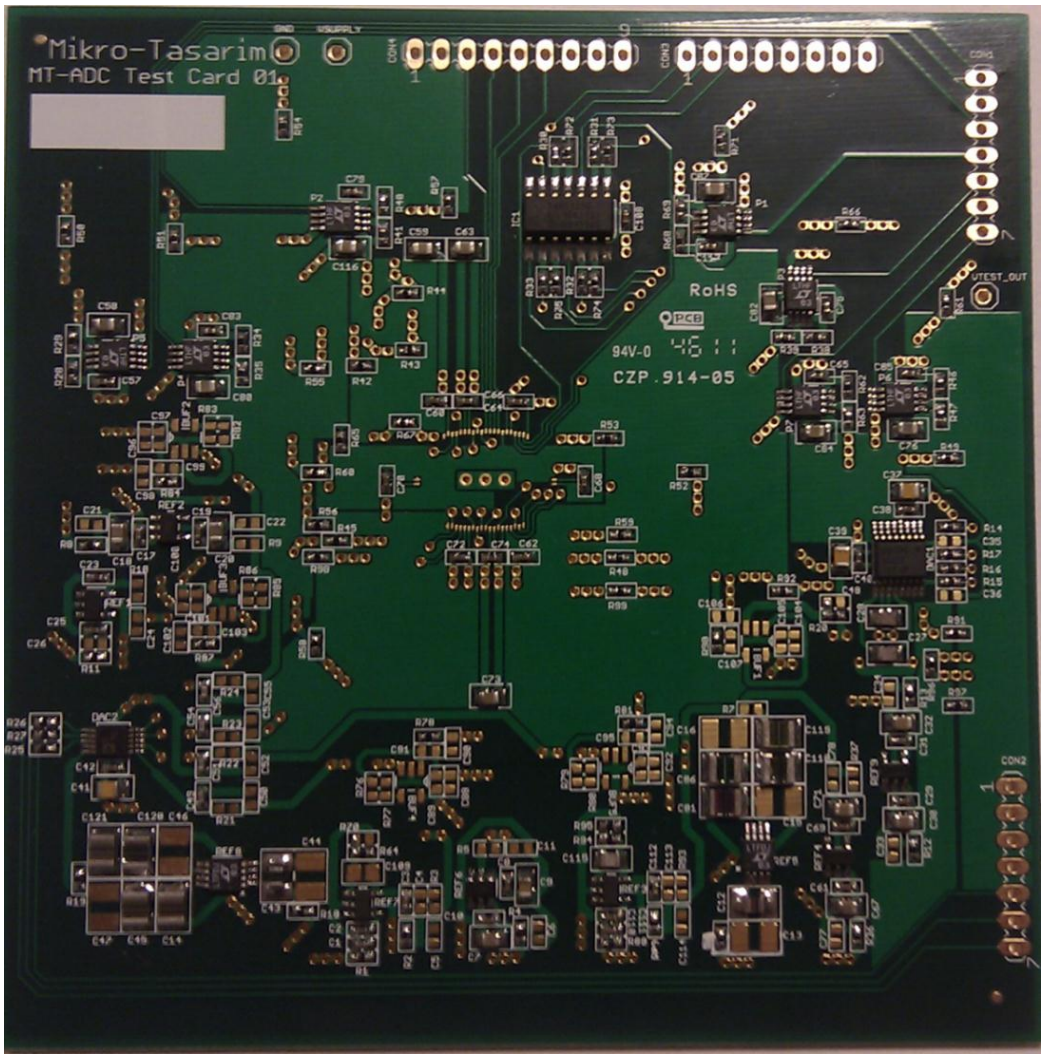

Figure 4.3: The proximity card that is prepared for testing of the SAR ADCs designed in this thesis. Redundant components are soldered for changing the test mode easily in the laboratory environment.

4.3 Test Types

The designed test card and the setup are meant to conduct a number of tests. Each of those test are embedded as different modes on the user interface. The DNL, INL, ENOB are the basic figures which will be measured. These are statistical tests, in other words many dies must be tested for accurate result. In this study, performance values will be limited to a few parts and not the whole wafer.

In order to measure the DNL and the INL figures, a ramp will be applied to the input. The ADC front-end does not have sample and hold circuit, so a multiplexed DC input is provided by the input DAC. This DAC is sigma-delta architecture; therefore the FPGA will wait for a certain amount of time for the output to settle. The SAR ADC output will be sent to PC when the 16-bit cycle is completed after the settling of input DAC. The output will be analyzed on the PC by using MATLAB.

The ENOB calculation requires sinusoidal signal at the ADC input. After collecting a number of samples of the ADC output, best fit is calculated from these data points. The actual (Q_A) and the theoretical quantization (Q_T) errors from the best fit are calculated. The ENOB is calculated as in Equation (4.3.1) where N is the number of bits [6].

$$ENOB = N - log_2\left[\frac{Q_A}{Q_T}\right] \tag{4.3.1}$$

The ENOB measurement includes the non-linearity errors and the noise distortion.

Besides the ADC chips, an additional die will be fabricated. All analog blocks are placed for standalone testing in case that characterization is needed.

CHAPTER V

CONCLUSION AND FUTURE WORK

The research conducted in the scope of this thesis involves the design and development of an analog-to-digital converter for low-cost microbolometers. In this framework, a successive approximation register analog-to-digital converter is designed. The ADC is designed using a 0.18µm CMOS process. The full chip functionalities and performances of both ADCs are simulated. Two versions with the same topology are submitted to foundry: One of them is a high performance device which has a resolution of 16-bit at a sampling rate of 128Ksps, and the other ADC is designed for a 160x120 image sensors which has a resolution of 14-bit at a sampling rate of 700Ksps. The power dissipation of the 16-bit ADC is around 10mW, where the 14-bit device consumes 30mW. Each of the dies is 1mm x 5mm, whereas the active circuits occupy around 0.5mm x 1.5mm silicon area. The data output is designed to be serial for decreasing the number of pads. A memory and serial interface is placed on chip. A highly configurable structure is implemented for the maximum flexibility during the tests of the architecture.

Based on the achievements and results of this study, following conclusions can be drawn:

1. The system architecture is optimized and investigated for these application specific ADCs. The imaging sensor characteristics, image processing techniques are taken into account for focusing on the important factors.
2. A resistive DAC is used in order to remove the minimum frequency limitation. A DAC modification is made for achieving high resolution with a resistive DAC.
3. The prototype is digitally configurable while testing. As a result a number of different circuit configurations and fine adjustments can be made to get the most out of the silicon.

4. A low noise test setup is prepared for high resolution ADC testing. The test system is a PC controlled and compact setup. All of the needed components are in one card to prevent noise coupling.

A great effort is shown for obtaining these results. However, there are some items which should be carried out as future work:

1. The complicated digital circuitry can be simplified after the first prototype tests. Therefore, power dissipation and circuit area will decrease.
2. The building blocks of the 14-bit version can be optimized because some blocks are currently over-qualified for 14-bit operation such as the comparator.
3. The ADCs can be used to digitize the analog output of actual sensors. The overall behavior can be tested further optimization can be made.
4. The ADCs can be integrated into target devices after the initial tests are complete.

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