LEAKAGE CURRENT AND ENERGY EFFICIENCY ANALYSES OF SINGLE PHASE GRID CONNECTED MULTI-KVA TRANSFORMERLESS PHOTOVOLTAIC INVERTERS

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LEAKAGE CURRENT AND ENERGY EFFICIENCY ANALYSES OF SINGLE PHASE GRID CONNECTED MULTI-KVA TRANSFORMERLESS PHOTOVOLTAIC INVERTERS

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ABSTRACT

LEAKAGE CURRENT AND ENERGY EFFICIENCY ANALYSES OF SINGLE PHASE GRID CONNECTED MULTI-KVA TRANSFORMERLESS PHOTOVOLTAIC INVERTERS

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In order to inject solar power to the utility grid, among various types of inverters, Grid Connected Transformerless Solar Inverters (GCTSI) are mostly preferred for residential or commercial applications. This preference is because of the high energy efficiency and low cost due to the absence of a line frequency or a high frequency transformer. Peak value of the efficiency characteristics of GCTSIs can reach 98%, which are selected topology, component optimization, switching strategy and operating condition dependent. In spite of the attractive energy efficiency characteristics of GCTSIs, due to the lack of galvanic isolation, these inverters are vulnerable to leakage currents, which are prohibitive for the safety and the maintenance reasons. The purpose of this research is to analyze GCTSIs in terms of their leakage current and energy efficiency characteristics. In the research, the leakage current mechanisms of GCTSIs are identified and grid connected solar inverters are classified in terms of their leakage current characteristics including the GCTSIs. In addition to the existing ones, several novel topologies are proposed enriching the family of GCTSIs. The leakage current and the inductor current ripple

performances of GCTSI topologies are analyzed and evaluated by detailed simulations for 3 kVA and 10 kVA single-phase systems. In addition, the energy efficiency characteristics of GCTSIs are investigated in these power levels by making use of Calculated Average Power Per Switching Cycle (CAPPSC) method. The efficiency studies with CAPPSC method provide design guidelines and comparison of the GCTSI topologies in terms of their energy efficiency characteristics.

Keywords: Transformerless solar inverters, common mode, leakage current, efficiency

ÖZ

ŞEBEKE BAĞLANTILI TEK FAZ ÇOK-KVA TRAFOSUZ GÜNEŞ EVİRİCİLERİNİN KAÇAK AKIM VE ENERJİ VERİMİ ANALİZLERİ

Özkan, Ziya

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Tez Yöneticisi: Doç. Dr. Ahmet M. Hava

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Güneş enerjisinin şebekeye aktarılması için, çeşitli eviriciler arasında, Şebeke Bağlantılı Trafosuz Güneş Eviricileri (ŞBTGE) çoğunlukla meskun ve ticari uygulamalarda tercih edilmektedir. Bu tercih, şebeke frekanslı yada yüksek frekanslı trafonun olmamasından kaynaklanan yüksek verim ve düşük maliyetten dolayıdır. ŞBTGElerde seçilen topoloji, malzeme optimizasyonu, anahtarlama stratejisi ve çalışma koşullarına bağlı olan verim karakteristiğinin tepe değeri 98% e ulaşabilmektedir. ŞBTGElerin çekici verim karakteristiklerine rağmen, galvanik izolasyonun eksikliğinden dolayı bu eviriciler güvenlik ve devamlılık sebepleriyle engelleyici olan kaçak akımlara karşı savunmasızdırlar. Bu araştırmanın amacı ŞBTGEleri kaçak akım ve enerji verimi bakımından analiz etmektir. Çalışmada ŞBTGElerin kaçak akım karakteristikleri teşhis edilmiş ve ŞBTGEler de dahil olmak üzere şebeke bağlantılı güneş eviricileri kaçak akım karakteristiklerine göre sınıflandırılmıştır. Var olanlara ek olarak, ŞBTGE ailesini zenginleştirmek üzere yeni topolojiler önerilmiştir. ŞBTGE topolojilerinin kaçak akım ve bobin kıpırtı akımı performansları 3 kVA ve 10 kVA tek faz simülasyonlarıyla analiz edilmiş,

değerlendirilmiştir. İlaven, ŞBTGElerin enerji verimliliği karakteristikleri bu güç seviyelerinde Anahtarlama Süresi Başına Hesaplanmış Ortalama Güç (ASBHOG) metodu ile incelenmiştir. ASBHOG metodu ile yapılan verim çalışmaları dizayn kılavuzu ve ŞBTGElerin verim yönü itibariyle kıyaslanmasını sağlamıştır.

Anahtar Kelimeler: Trafosuz güneş eviricileri, ortak mod, kaçak akım, verim

To My Family

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TABLE OF CONTENTS

LIST OF FIGURES

FIGURES

LIST OF TABLES

TABLES

LIST OF ABBREVIATIONS

APPSC	Average Power Per Switching Cycle
CAPPSC	Calculated Average Power Per Switching Frequency
CDCF	Current Duty Cycle Function
CMV	Common Mode Voltage
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
GCTSI	Grid-Connected Transformerless Solar Inverter
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MTBF	Mean Time Between Failures
PEC	Power Electronic Converter
PCC	Point of Common Coupling
PV	Photovoltaic
PV-PEC	Photovoltaic Power Electronic Converter
PWM	Pulse Width Modulation
SC-GCTSI	Solidly Clamped Grid-Connected Transformerless Solar Inverter
TDD	Total Demand Distortion
THD_I	Total Current Harmonic Distortion
THD_V	Total Voltage Harmonic Distortion
UPS	Uninterruptible Power Supply
ZV-GCTSI	Zero Vector Grid-Connected Transformerless Solar Inverter
ZVH-GCTSI	Zero Vector Hybrid Grid-Connected Transformerless Solar Inverter
ZVI-GCTSI	Zero Vector Isolated Grid-Connected Transformerless Solar Inverter
ZVMC-GCTSI	Zero Vector Midpoint Clamped Grid-Connected Transformerless Solar Inverter

CHAPTER 1

INTRODUCTION

1.1 Background

Electric energy is widely used and it is indispensible source of useful work almost in every field of life. The increasing demand for the electric energy and declining energy resources such as fossil fuels have forced mankind to place significant emphasis on renewable energy sources, which emerged as the interconnection of different clean sources to yield higher reliability, reduced greenhouse gas emissions and increased power quality [1].

Among the renewable energy systems, wind energy systems experienced major growth within the last two decades. However these sources may be geographically far away from the settlements and installations where the energy is needed. Moreover, flicker problems may arise at the point of common coupling (PCC) due to the unpredictable nature of the wind [2], [3]. Besides, the instantaneous real and reactive power of the source and the grid should be matched to continue nominal voltage and frequency of the grid, which is a hard task to achieve in the case of wind energy due to the difficulties in estimating the wind speed nearly instantaneously. In the second most popular renewable energy source, the solar energy source, these drawbacks are rather eliminated. The generation location of solar power may be very close to the place where the power is consumed, without circulating the current along a long distance through the power system [4]. The variation in the illumination of sunlight with respect to time is considerably lower than the variation in wind speed; therefore flicker problems are rather reduced in solar systems. In the solar energy area, of the major technologies, the photovoltaic (PV) solar technology area, system installations have been experiencing exponential growth over the last couple of years (Figure 1.1), [5]. The government incentives provided all around the world and decreasing photovoltaic (PV) module and other installation prices (such as inverters, labour, shipping etc.) (Figure 1.2) are the key factors behind this growth [6], [7], [8].

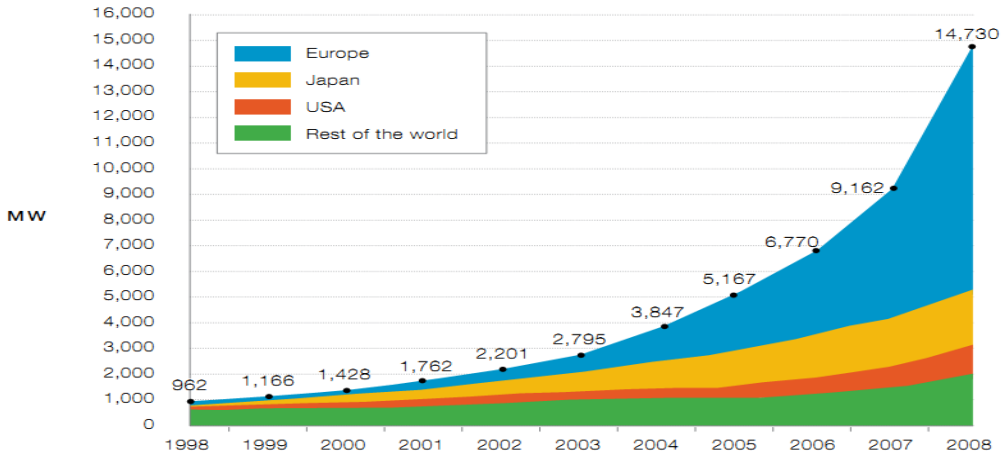


Figure 1.1 Solar installations around the world with respect to years [5].

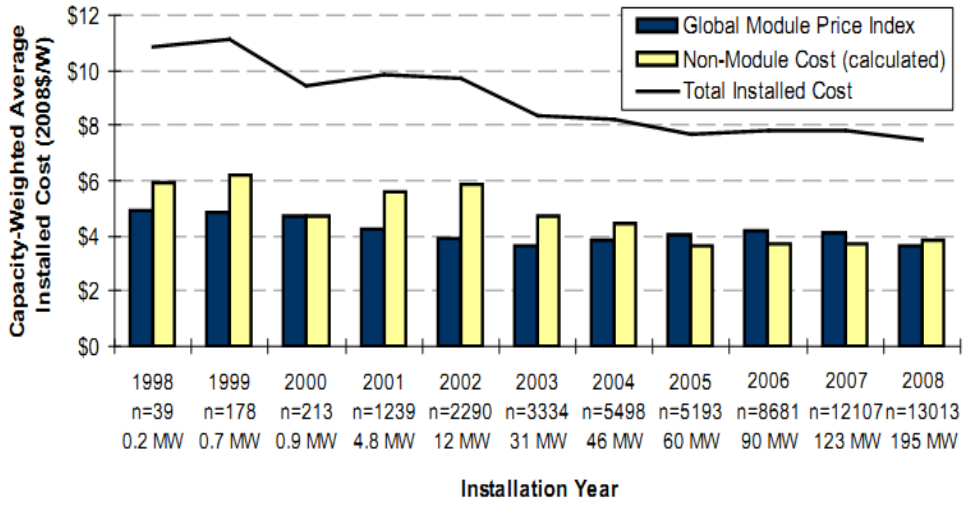


Figure 1.2 PV system costs with respect to years [6].

Photovoltaic energy systems can be grouped as large-scale PV systems (solar farms involving MW ratings), medium scale (in tens of kW ratings) put on the roofs of industrial buildings etc., and finally the residential PV systems typically placed on the roofs of the residential places (several kW or less). Of these, the largest market growth and high number of installations has been experienced in the residential applications [9]. Residential applications can be off-grid with/without a battery back-up or grid-connected with /without a battery back-up, all of them equipped with power electronic converters (PEC) as an interface to the loads (Figure 1.3). In most of the cases for the off-grid applications, the loads are far away from the utility grid, therefore PV installations appear with battery back-ups as an alternative to installing long cables. However if the load is not a critical one such that the

electric power is not always required, battery back-up is not necessary which is the case for PV energy fed water pumping systems. In grid-connected systems with battery back-up, the batteries are charged either from the PV source or from the utility grid. If the batteries are full, excessive power is delivered to the utility grid. In case of an electric power cut-off, the system operates as an uninterruptible power supply (UPS) by feeding the local loads from the batteries with the disconnection from the utility grid. In the case of grid-connected systems (where the grid-connected systems without battery back-up are intended hereby), battery charging and discharging losses are nonexistent which increases the system efficiency and cost, sacrificing the UPS operation. Although the choice among these PV systems is application dependent, grid-connected systems are the most favourable in terms of commerciality, due to their lower cost and size, and less maintenance. As a result of these, more than 78% of global market in 2008 was reported to be grid-connected applications [10].

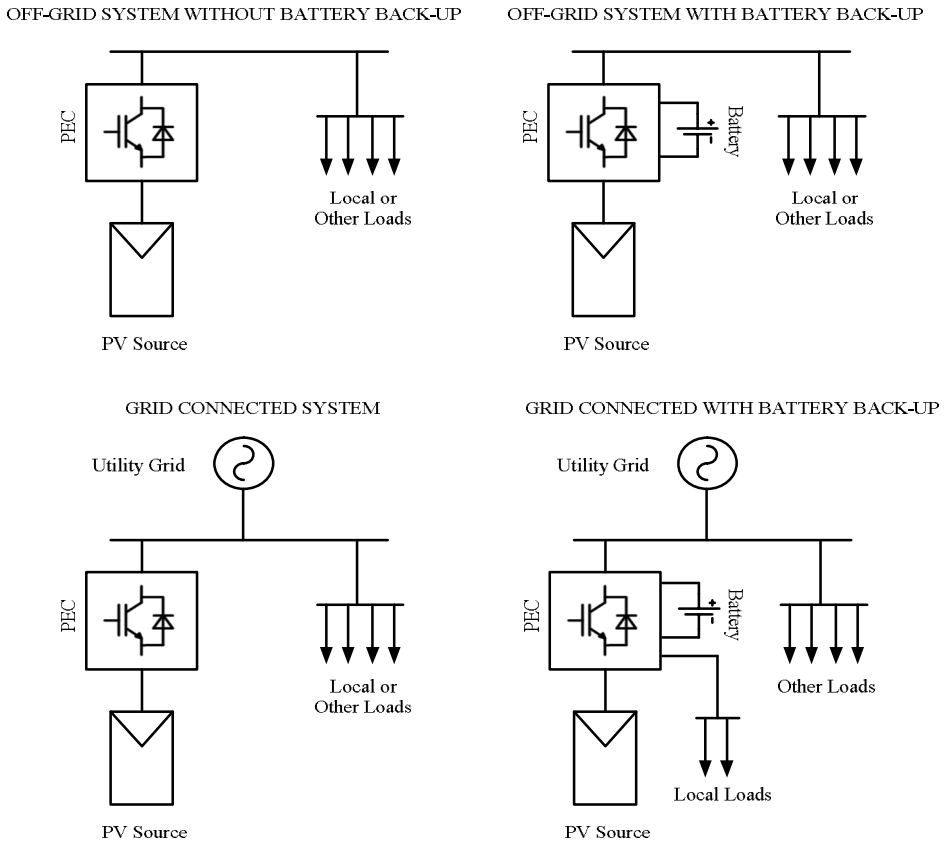


Figure 1.3 Classification of PV systems in terms of energy management strategy.

1.2 Grid-Connected Photovoltaic Power Electronic Converter (PV-PEC) Systems

Grid-connected PV systems are composed of the PV source and the PEC that is connected to the utility grid. Although for the time being the PEC constitutes slightly above one tenth of the total price of the system, its effects on the conversion of the power is vital. The PEC is responsible for both operating the PV source under maximum power point and to regulate the grid side current while preserving high efficiency. While achieving these, it should boost the PV source voltage when necessary and should also guarantee human safety, protection of the grid, protection of the PV source and protection of itself. PECs used for PV applications will be abbreviated as PV-PECs hereafter.

First generation PV-PECs were based on galvanic isolation in the grid-connection of PV sources. Nevertheless, the inclusion of galvanic isolation introduces either a high frequency or a low frequency transformer to the system where the system efficiency is reduced due to core and copper losses of the transformer. As a result of engineering efforts, technology progressed and these transformer based PV-PECs have been replaced by transformerless inverters, which are the main interest subject of this thesis, especially for the power ratings above 1 kW [11]. The reason behind this increase in the continuing popularity of grid-connected transformerless solar inverters (GCTSI) is the low cost, high reliability and high energy efficiency of these systems when the transformer is omitted [11], [12], [13], [14], [15], [16], [17]. Among these benefits of GCTSIs, energy efficiency is the major figure of merit to evaluate the grid-connected PV sourced PECs since payback period and lifetime of a PV-PEC is in high correlation with the efficiency characteristics of the power converter. Moreover, due to the absence of the transformer, GCTSIs can be manufactured light in weight and small in size as compared to their transformer based competitors [13]. Further, these inverters can be manufactured with lower cost, which have favourable indirect effects on the payback period of the system [18]. In Figure 1.4 efficiency, weight and volume attributes of transformerless and transformer based GCTSIs are illustrated to summarize their characteristics.

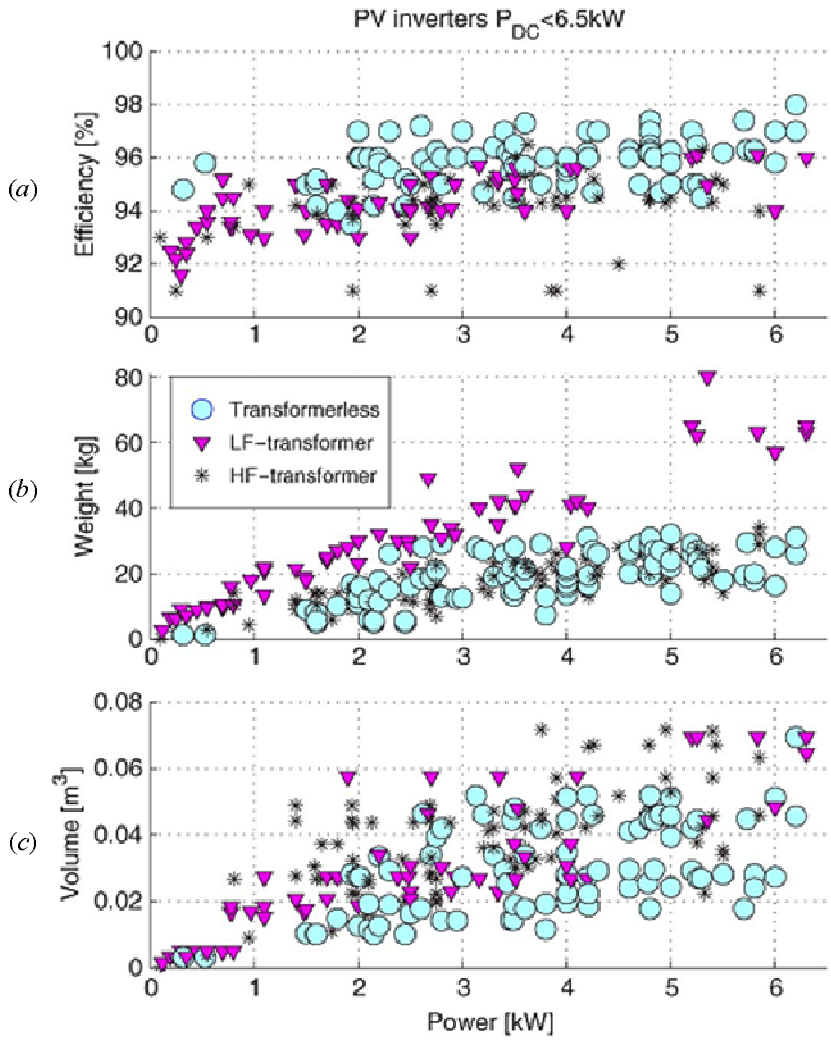


Figure 1.4 Efficiency (*a*), weight (*b*), and volume (*c*) characteristics of transformerless, low-frequency transformer, and high frequency transformer based grid-connected solar inverters [13].

In spite of the above-discussed benefits of GCTSIs, these inverters are vulnerable to leakage currents due to the parasitic capacitances existing between the live parts of the modules and the grounded surfaces of the PV modules. Although the RMS and peak values of the leakage currents are generally low in magnitude (less than several amperes), their effects are prohibitive. The leakage current in these inverters can reach to a dangerous level for thin film PV modules by excessive degradation of their efficiency irreversibly [19]. One-step beyond the thin film degradation is the leakage current dependent conducted and radiated electro-magnetic interference (EMI) problems [20]. Further, the leakage current should be

prevented to maintain protection coordination of the power system [21]. The leakage currents also introduce additional losses in the conversion system [22] and line current distortion [23]. Depicted in Figure 1.5 with a single equivalent lumped parasitic capacitor (C_p) represents the distributed parasitic capacitances of the PV modules. The high efficiency classical H-bridge (or H4) inverter topology with unipolar modulation is an unacceptable solution for PV application due to the leakage current problem in GCTSIs due to its excessive leakage current bearing Common Mode Voltage (CMV) variations [13], [17], [18], [24]. Similarly, H4 bipolar modulation is not a preferred solution as it has efficiency drawbacks because of high filter inductor current ripple and reactive power circulation between the grid and the DC bus [18].

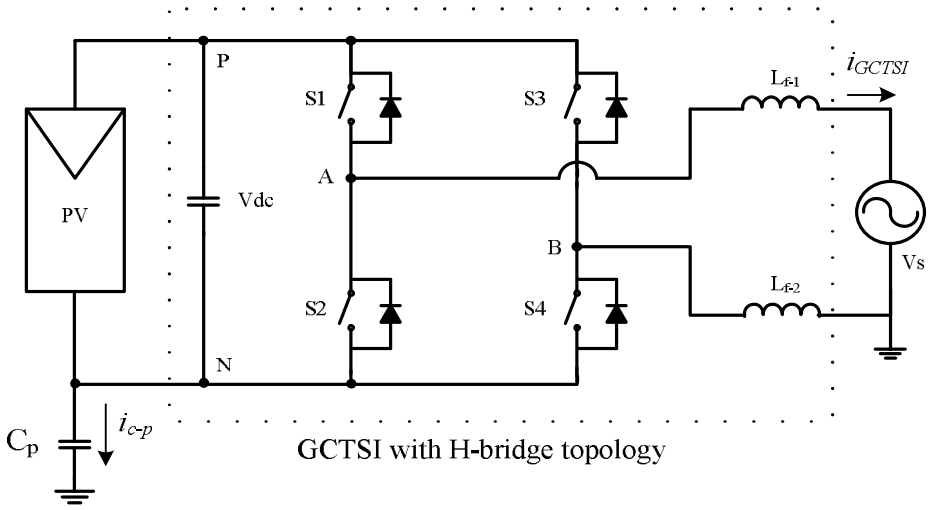


Figure 1.5 Illustration of the PV panel caused equivalent parasitic capacitance on a GCTSI circuit with a single stage classical H-bridge topology with L filters.

With the classical H4 topology being inapplicable as a GCTSI, various topologies have been recently proposed in the literature with reduced leakage current characteristic, [13], [17], [23], [25], [26], [27]. However, in spite of their reduced leakage current behaviour, these topologies are neither investigated in a detailed manner nor classified in terms of their leakage current behaviour. Besides, some of the literature has defective approaches which cultivated incorrect indication of the source of the leakage currents in GCTSI inverters. Considering these drawbacks, this thesis analyses the leakage current mechanism of GCTSIs in detail. In addition, the thesis proposes new methods to reduce leakage currents topologically rather than by filtering. Depending on the analyses and the methods, several novel topologies are proposed with reduced leakage current behaviour. Furthermore, the

thesis classifies these inverters in terms of their leakage current behaviour. These classes are, Zero Vector Isolated Grid-connected Transformerless Solar Inverters (ZVI-GCTSI) which decouple AC and DC circuits at zero output voltages, Zero-Vector Midpoint Clamped Transformerless Solar Inverters (ZVMC-GCTSI) which are derived from ZVI-GCTSIs by midpoint connection rather than decoupling at zero vector states, Zero Vector Hybrid Grid-Connected Transformerless Solar Inverters (ZVH-GCTSI) which behave as ZVI-GCTSIs or ZVMC-GCTSIs interchangeably, and Solidly Clamped Grid-Connected Transformerless Solar Inverters (SC-GCTSI) wherein AC and DC circuits are always solidly clamped. The existing and the proposed topologies belonging to these classes are investigated in terms of their leakage current characteristics by detailed analysis and computer simulations and high correlation and consistency has been found between the two.

In spite of the energy efficiency benefits due to the absence of a transformer, a GCTSI can still have low energy conversion efficiency characteristics as in the flying inductor (also named as Karschny) topology due to the drawbacks of the high number of semiconductors on the line current path [17]. For efficiency comparison of selected topologies (the ones offering high energy efficiency) it is necessary to investigate the semiconductor losses and characterize each topology under investigation. Such efficiency comparison is beneficial in choosing a topology among many available, and also in predicting performance during the design stage. In this thesis, semiconductor loss based energy efficiency characterization of GCTSIs is realized using the Calculated Average Power per Switching Cycle (CAPPSC) method and selected semiconductor datasheets for 3 kVA and 10 kVA of power ratings.
Apart from the energy efficiency characteristics of GCTSIs, there exist several restrictions and requirements recognized for grid connection of GCTSIs, which can be specific to each country. One of these restrictions is the injected harmonic current distortion to the utility grid to preserve voltage quality and to prevent radiated and conducted electromagnetic interference problems reflected to other customers connected to the same point of common coupling (PCC). In addition, the reactive power supply is becoming a different requirement to prevent voltage rise at PCC. The disconnection of the PEC from the grid or from the PV source under grid or PV source fault conditions is required due to system and human safety reasons. The leakage current and the injected DC current to the grid are also restricted by several standards to prevent the shortcomings of these failures. A grid-connected PV- PEC should meet the related restrictions and requirements of that country where it is connected; therefore, a survey of these and further restrictions and requirements are also included in the thesis.

1.3 Scope of The Thesis

This thesis is mainly focused on and dedicated to the leakage current analyses of GCTSIs, classification of GCTSIs in terms of their leakage current behaviour, and the energy efficiency characterization of the GCTSIs which are offering high efficiency.

The main contributions of the thesis are; the identification and analyses of leakage current mechanisms of the GCTSI topologies and their classification in terms of leakage current behaviour, development of several high energy efficiency low leakage current new GCTSI topologies, and finally development and application of an efficiency estimation method for the PV-PECs.

In the thesis, ZVI-GCTSI, ZVMC-GCTSI, ZVH-GCTSI, and SC-GCTSI topologies are classified, new topologies proposed, and studied. The leakage current characteristics of these topologies are analytically investigated and the results are verified via simulations. The energy efficiency characteristics of assertive topologies belonging to these classes of GCTSIs are calculated and evaluated.

The thesis is organized as follows.

In the second chapter, grid-connected PV system requirements, restrictions, and standards are investigated. First, the maximum power point tracking requirement is presented. Following this section, the power quality problems due to grid-connected PV systems at the PCC are addressed and the limits and the rules concerning these problems are presented. Then, the physical source of leakage current in PV systems is identified and the restrictions on the leakage current by the standards are depicted. Other non-regulatory requirements for these systems are also summarized in this chapter. This chapter establishes background for the converters to be studied in the following chapters in terms of performance (mainly leakage current performance).

In the third chapter, a thorough survey of grid-connected PV-PEC systems is provided and these systems and their circuit topologies are classified with respect to their leakage current characteristics. Novel topologies belonging to each class of these topologies are presented and their principles of operations are supplied in this chapter.

In the fourth chapter, the leakage current characteristics of the identified classes of topologies are analytically investigated. The inductor current ripple characteristics of these classes are also analyzed in this chapter. After these analyses, the simulated system model is presented. Then the simulation results of each class of GCTSI topologies are depicted. This chapter ends up with the leakage current, line filter inductor current ripple performance comparison, and a brief summary of the chapter.

In the fifth chapter, calculated semiconductor loss based efficiency evaluation of the discussed topologies is realized. First the calculation of instantaneous of conduction and switching losses of MOSFETs, IGBTs and diodes is investigated. Then the procedure to calculate the semiconductor losses at each switching cycle and quantization of these losses in the form of average power per switching cycle (APPSC) is demonstrated by making use of the current duty cycle function and current-voltage stresses of the devices at each switching cycle. After that, semiconductor devices are selected among manufacturer datasheets for 3 and 10 kVA systems for the semiconductor loss and efficiency calculations. Finally, the semiconductor losses and the efficiency curves are illustrated to reach some conclusion on the topologies and the semiconductor devices.

The final chapter provides an overall performance evaluation of the discussed PV-PECs in terms of leakage current and efficiency characteristics. This chapter also summarizes the contributions of the thesis, provides general concluding remarks on the existing and proposed topologies in terms of leakage current and energy efficiency basis, and recommends future work.

CHAPTER 2

GRID-CONNECTED PV-PEC SYSTEMS, RESTRICTIONS, AND REQUIREMENTS

2.1 Introduction

Connection of PV modules to the utility grid involves grid codes, standards, and specific methodologies. Various PV-PEC topologies can be connected in several ways, and may have specific MPPT algorithms and PV module connection strategies. In all the cases, however, the overall system consists of three main blocks; the PV source, the PV-PEC, and the utility grid as depicted in Figure 2.1.

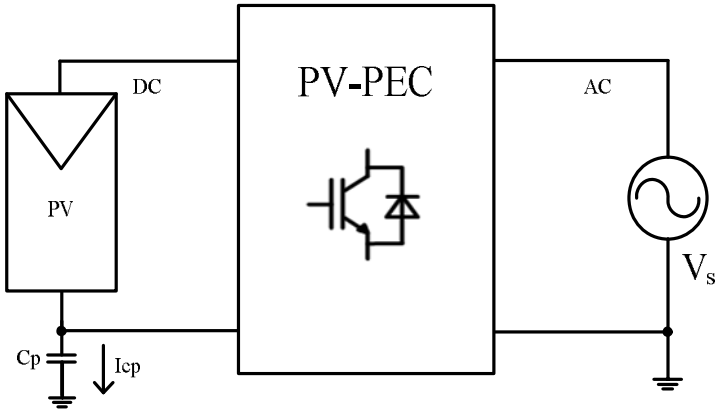


Figure 2.1 A grid-connected PV system with main building blocks; PV source, PV-PEC, and the utility grid. The capacitor represents the most important parasitic element, the stray capacitance of the PV modules.

PV modules, as the semiconductor-based converters of the sunlight energy into electrical energy, have irradiation dependent terminal characteristics (voltage-current) that should be biased such that the V-I product yields maximum power. It is the responsibility of a PV-PEC to track the maximum power point (MPP) to maximize the energy harvested.

Grid-connected PV-PECs, as the brain of the overall system, should be designed to meet the requirements of the grid, and the requirements of the PV modules. Furthermore, they should meet the needs of the customer. The PV-PEC should have high efficiency characteristics throughout most of the loading range to decrease the payback period of the PV system. Moreover, the PV-PEC should be designed to achieve low cost, and small size. Reliability, therefore lifetime, of the inverter is another key factor to open the door of the applicability, and acceptance.

Grid connection of PV-PECs cannot be carried up arbitrarily. The process is restricted in various aspects by various standards such as IEEE 1547, EN 61000-3-2, EN 50160, IEC 61727, and DIN VDE 0126-1-1, which are the most common, and mostly recognized standards for grid connection of PV systems. These restrictions aim to provide the continuity of the power quality and human safety. The restrictions cover the power quality issues such as voltage quality, harmonic current injection limits, and power factor issues. Furthermore, safety, and anti-islanding conditions like crossing the nominal voltage, and frequency limits are included in these standards. Moreover, leakage current and injected DC current limits are included in various standards to continue protection coordination of the power system, and human safety.

Considering the aforementioned requirements, and standard restrictions, this chapter is dedicated to a brief survey of these requirements, and restrictions. In the second section, PV module structures, and the MPPT requirement of PV modules are studied. Then, connection types of PV modules are investigated based on the MPPT distribution strategy on the modules. In the third section, the PV-PEC requirements related to PV-PEC itself are investigated. Efficiency, reliability, cost, and size are some of these requirements to be studied. These requirements are not compulsory, but they should be fulfilled for, from the concept to the application realization of the converters. The scope of the fourth section is the PV-PEC and grid interaction, where grid-connected PV system power quality, system and human safety issues are reviewed. Specifically, current harmonic limitations, leakage current restrictions, and anti-islanding conditions are considered. In the fifth section, a brief conclusion on the requirements and the restrictions is given.

2.2 PV Module Structure and Requirements

PV modules are the supply of the electrical energy to be injected to the utility grid. Therefore, these modules should be operated at their MPPs. As this is the case, voltage-current characteristics of PV modules, the need for MPPT, and the basic system connection types with respect to MPPT distribution strategy are addressed in this section.

2.2.1 PV Technology

PV cells, which are the basic building blocks of PV modules, can be produced based on crystalline-based technologies such as monocrystalline silicon, polycrystalline silicon, and thin film based technologies like amorphous silicon, Cadmium Telluride (CdTe), Copper Indium Gallium Selenide (CIGS) etc. [28]. For the time being, the crystalline-based technology is more expensive than its thin film based counterpart because of the manufacturing difficulties. Nevertheless, some thin film based modules may suffer from the leakage current, and they may need special grounding configurations due to transparent conducting oxide corrosion or polarization effects [29].

The V-I characteristic of any PV cell is irradiation dependent, therefore its voltage vs. power (V-P) characteristic is also irradiation dependent. With the series, and/or parallel connection of PV cells, PV modules are constructed. Therefore, the V-I, and V-P characteristics of PV modules are also irradiation dependent. In Figure 2.2, a commercial monocrystalline PV module is illustrated with its V-I characteristic. As can be interpreted from this figure, the V-I characteristic of a PV module has an MPP voltage, and current operating point, which should be tracked to harvest maximum power.

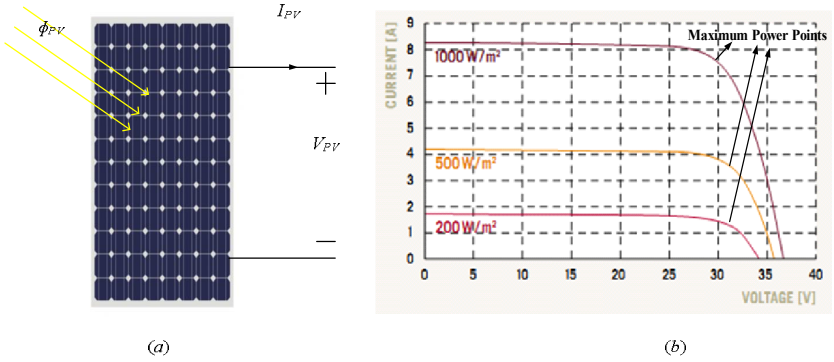


Figure 2.2 Typical I-V characteristic of a commercial monocrystalline PV module with maximum power points illustrated on the curves [30].

2.2.2 Review of Connection of PV Modules Based on MPPT Strategy

Figure 2.2 illustrates individual PV modules having independent V-I characteristic from each other, but the module characteristics are illumination, and temperature dependent [31]. Therefore, the PV-PECs should track the MPP as the irradiation or temperature changes. Several algorithms to perform MPPT of the PV sources are available in the literature such as perturb and observe, incremental conductance, extremum seeking [32], [33]. Nevertheless, the strategy to apply MPPT on the PV source can be mainly divided into two, namely, central MPPT, and distributed MPPT. In the central MPPT approach, PV modules are connected in series (called strings) to increase the system voltage near the peak of the grid voltage. This approach (string inverter concept) can be enhanced to increase the power level by either paralleling additional strings with string diodes (array inverter concept) or utilizing DC/DC string regulators each responsible of the MPPT of the corresponding string (multi-string inverter concept) as depicted in Figure 2.4. In the second approach, PV modules are tracked individually (distributed MPPT). This operation can be achieved either by series distributed MPPT concept, parallel distributed MPPT concept or micro-inverter concept [34], [35], which are also illustrated in Figure 2.4.

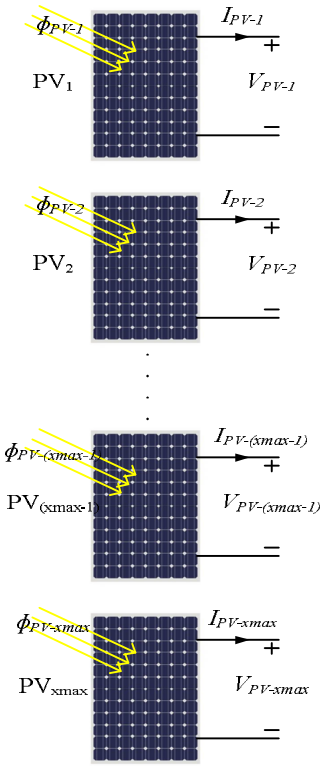


Figure 2.3 Illustration of individual PV modules each having independent I-V characteristics from each other.

Assuming the MPPTs of all systems in Figure 2.3 are successful, the distributed MPPT becomes more advantageous than centralized MPPT in terms of the power extracted from the same PV modules under same irradiance, and temperature conditions due to the inequivalence of the objective functions of these MPPT strategies. For illustration, the inequivalence of objective functions of micro-inverter based distributed MPPT, and an array inverter based central MPPT is formulated in (2.1).

$$\sum_{x=1}^{x_{max}} \max\left\{g(V_{PV-x-d}) \cdot V_{PV-x-d}\right\} \geq \max\left\{\sum_{x=1}^{x_{max}} g(V_{PV-x-c}) \cdot V_{PV-x-c}\right\} \tag{2.1}$$

where x_{max} is the number of the PV modules to be used, $V_{PV\text{-}x\text{-}d}$ is the x^{th} module's terminal voltage, $g(V_{PV\text{-}x\text{-}d})$ is the x^{th} module's terminal current ($I_{PV\text{-}x\text{-}d}$) under distributed MPPT, and similar variable assignment is valid for centralized MPPT. It should be noticeable that $g(V_{PV-x-c})$ is same for all modules, since they are connected in series.

In spite of the maximum energy harvesting from the PV source benefit of distributed MPPT based PV-PECs, especially for micro-inverter based distributed MPPT, under non-equal irradiance conditions of the modules, for the time being, this approach has the drawback of higher installation investments as the number of the PECs are high [36] as they are compared to centralized MPPT concept. Further, the efficiency characteristics of distributed MPPT based PV-PECs are comparably poor with respect to their central MPPT based counterparts [11]. String inverters or multi-string inverters stand between the array inverters and the distributed MPPT based PV-PECs in terms of MPPT strategy performance, therefore these inverters become quite favourable [11]. However, with the focus on the drawbacks of distributed MPPT based PV-PECs, this approach can reach the economy, and the efficiency of centralized MPPTs. Although MPPT is an essential function to be performed, it is only one of the duties of a PV-PEC.

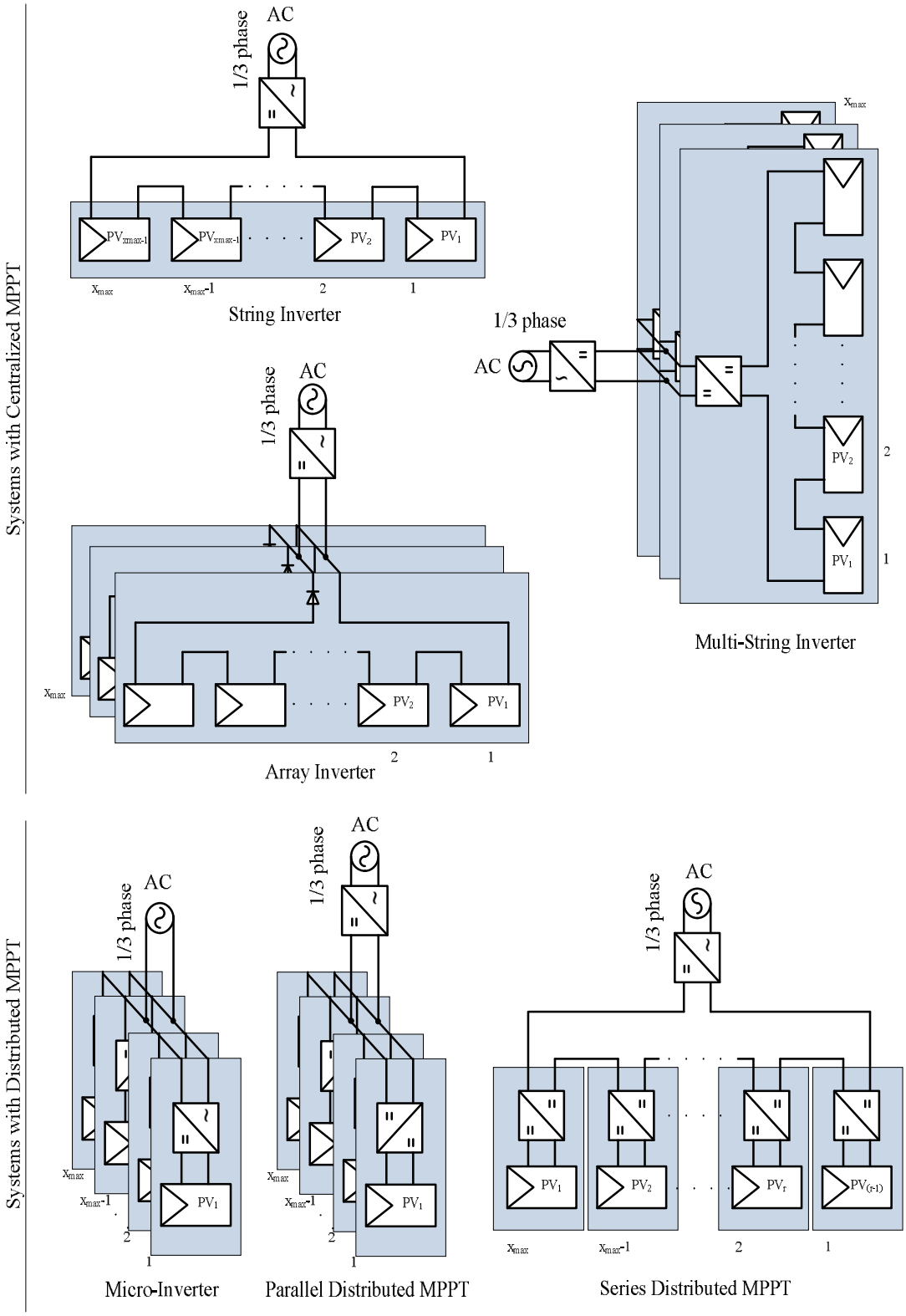


Figure 2.4 Grid-Connected PV-PEC systems in terms of their MPPT distribution strategy.

2.3 Grid-connected PV-PEC Requirements

In the previous section, PV source related requirements, such as distribution types of MPPT over PV modules are investigated. Nevertheless, a PV-PEC has also itself related requirements to be fulfilled by the designer. First, a PV-PEC should be designed to have high efficiency to decrease payback period of the system. Besides, as important as efficiency, a PV-PEC should have high reliability, and long lifetime. In addition, low cost, and small size are the features that are preferred to be existent in a PV-PEC. Moreover, the inclusions of galvanic isolation or a pre-regulator stage are the requirements to be fulfilled, when needed. Considering these PV-PEC related issues, this section is devoted to investigate the issues, and to emphasize their importance as the system applicability, and system profitability is concerned.

2.3.1 Efficiency

Efficiency is one of the most important criteria in a PV-PEC both effecting the system payback period directly, and some of the other requirements such as reliability, lifetime, cost, and size indirectly. To clarify, as the PV-PEC becomes more efficient, the energy yield of the PV system increases, therefore payback period of the system decreases. In addition, as the efficiency is higher in a PV-PEC, the components in the PV-PEC experience less thermal stresses than the ones in a system having less efficiency. As this is the case, the reliability, and the lifetime of the components, therefore the reliability, and the lifetime of the PV-PEC increase. The cost and size of a PV-PEC is also closely associated with the efficiency characteristics. As the semiconductor efficiency increases in a system, the system heatsink and cooling requirements decrease, which both reduce the cost, size, and even the cooling losses, increasing the efficiency in a cyclic manner. Moreover, for the efficiency intentions, if the transformer is omitted from the PV-PEC, the cost, and size of the system will be automatically reduced by a drastic amount.

Since the sun's irradiation or clouding changes with time within the day, and within the year, a PV-PEC is required to exhibit a high efficiency characteristic not only at full loading but also at a wide loading range to maximize overall energy extraction from the PV source. A commonly recognized measure of the efficiency characteristics of a PV-PEC is the Euro efficiency, which is defined in (1.5) as the weighted sum of the efficiency characteristics under varying loading conditions of a PV-PEC. If a transformer is included in the power

conversion stage in PV-PECs, the Euro efficiency characteristics decrease 1-2% in the average [13]. Therefore, GCTSIs are highly favourable as grid-connected PV-PECs.

$$\eta_{EU} = 0.03 \cdot \eta_{5\%} + 0.06 \cdot \eta_{10\%} + 0.13 \cdot \eta_{20\%} + 0.10 \cdot \eta_{30\%} + 0.48 \cdot \eta_{50\%} + 0.20 \cdot \eta_{100\%} \quad (2.2)$$

The efficiency of a GCTSI is determined by the losses arising from the semiconductors, from the passive components such as filter inductor, and DC bus capacitor, and non-conversion losses such as internal circuitry supply etc. Among these, the dominant losses arise from the semiconductors, and the filter inductors, which are also selected topology dependent, whereas other losses appear nearly constant for the same level of output power. These losses are the main reason for the difference in efficiency between any two GCTSIs. Besides, two GCTSIs, having the same output voltage characteristics, exhibit same inductor loss characteristics under same loading conditions. Hence, for the same output voltage characteristics of different GCTSIs, even the filter inductor losses become equal. This issue is studied in chapter 4. The other component of the dominant losses of a GCTSI is the semiconductor losses. The semiconductor losses in a GCTSI depend on the selected topology for conversion, and the selected semiconductors. If the topology has high number of semiconductors on the line current path under normal operation, the efficiency will be adversely affected. Similarly, if the semiconductors are not optimized, the efficiency characteristic of the inverter severely degrades. Therefore, chapter 5 is devoted to a detailed modelling of semiconductor losses and several GCTSI topologies among those offering high efficiency. These GCTSIs are evaluated in chapter 5 in terms of their semiconductor efficiency characteristics.

2.3.2 Cost, Size, and Weight

Being slightly above one tenth of the total system, cost of a PV-PEC is one of the considerable components of the force to shift PV systems into practical axis by the payback reduction as well as the size and weight. Cost, size, and weight of a PV-PEC are tightly related to the efficiency characteristics of the converter, the selected method, and selected topology for the energy conversion. As the semiconductors become more efficient in the conversion, related conduction and switching losses become lesser. The decrease in the semiconductor losses, decreases the required heatsink and one-step beyond is the needlessness of a forced cooling apparatus. The reduction of required heatsink and the elimination of forced cooling reduce the

inverter cost, size and weight. In transformerless inverters, further reduction in size and weight is generally achieved due to the absence of the transformer as illustrated in Figure 1.4.

2.3.3 Reliability and Lifetime

Payback period of a system is an important figure of merit, not only for PV-PECs, but also for other parts of the PV systems to be evaluated and to be compared in terms of investment profit. Besides payback period, as well as payback period and even more, system reliability and lifetime are other factors to evaluate systems. To clarify with an example; a system with longer lifetime and longer payback period may become more favourable than a system with shorter lifetime with shorter payback period in terms of investment planning.

Consisting of three main parts, PV source, PV-PEC, and utility grid, for the time being, the lifetime of a PV system is mostly limited by PV-PECs. The lifetime of a grid-connected PV-PEC is approximately 5 years, whereas the minimum warranty on PV modules is 20 years. The reason behind the limitation is addressed as the short Mean Time Between Failures (MTBF) of electrolytic capacitors, and controlled semiconductor devices such as IGBTs and MOSFETs in [36], [37]. Dust, humidity, voltage spikes, overloading conditions and temperature are the main factors affecting the MTBF of these components.

2.3.4 Pre-Regulator Stage and Galvanic Isolation

Depending on the PV source voltage level, and the existence of a transformer, a PV-PEC may be designed as single stage or multiple stages (generally two stages) as illustrated in Figure 2.6. In the single stage case, the voltage of the PV source is high enough to inject current to the utility grid without saturating the inverter, and the MPPT function and the inversion are realized in this single stage. In the two stages case, the PV source voltage is generally lower than the DC bus voltage of the inverter stage and the PV side stage boosts the PV side voltage to the DC bus level while realizing the MPPT function. This stage can be implemented by any of several boost topologies as suggested in [38] and beyond the scope of this thesis.

Any of the stages in the PV-PECs may include a transformer both for the galvanic isolation and for the boosting needs. The inclusion of galvanic isolation introduces additional safety and grounding freedom of the PV source side from any point, which can be necessary for some thin film module types, sacrificing the efficiency. Galvanic isolation requirement is

country dependent. In the U.S., grounding of either one of the PV source terminals is required by the grid codes [39], which can be achievable by either inclusion of galvanic isolation, or making use of PV source grounded topologies. In some countries, a galvanic isolation between the utility grid and the PV source is necessary [19], therefore transformerless inverters are not in use in these countries yet. In others, such as Germany and Spain, GCTSIs can be connected to the grid when they are mounted with a residual current monitoring unit. As mentioned previously, the major focus of the thesis is the inversion stage, and the focus excludes the pre-regulator stage and any transformer in the conversion stage (GCTSI).

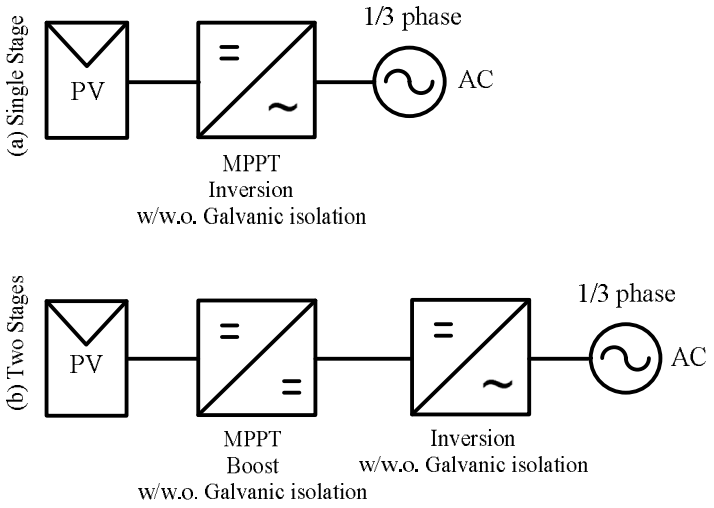


Figure 2.5 PV-PEC systems with single stage (a), and two stages (b).

2.4 Power Quality, System Protection, and Safety Requirements

A grid-connected PV-PEC is required to be in harmony with the utility grid, as it is in harmony with the PV source side. The PV-PEC should not disturb the power quality of the public grid and should maintain the protection coordination and the stability of the power system by disconnection where necessary. For these reasons, grid connection of PV-PECs are subject to safety and power quality restrictions and requirements specified in related codes such as IEEE 1547, DIN-VDE-0126-1-1, IEC 61727, and EN 61000-3-2. In this section, power quality and safety related requirements are studied with brief overview of the related parts of the related standards.

2.4.1 Power Quality

Power quality consists of the quality of the voltage waveform supplied by the utility and the quality of the current drawn by the loads. The voltage supplied should be a pure sinusoid with the predefined frequency and magnitude within their limits specified by standards. Moreover, the harmonic content should be in predefined limits to continue proper operation of the noise sensitive loads. The current drawn (or injected) by the loads (or distributed resources) should be also within the predefined power factor and harmonic content limits for electro-magnetic compatibility needs. The following sections briefly investigate these power quality issues.

2.4.1.1 Harmonic Currents and Voltages

Grid connection of any PEC to a power system should meet the grid standards of that country, which are intended to ensure the continuity of power quality at the point of common coupling (PCC).

The current injected by a PEC to utility grid may contain harmonic content. The magnitude and the frequency of this content may result in several power quality problems at the PCC. In Figure 2.4, single line diagram of a grid-connected PV-PEC is depicted for the investigation of line current harmonics, and PCC voltage rise issues. In the circuit, if the PEC harmonic current content is high, and the grid is not stiff enough, the high frequency content flows to other loads, which are connected to the PCC, resulting in EMI problems for noise sensitive equipments. Even if this is not the case, the high frequency content has to flow through the distribution transformer disturbing the voltage quality at the PCC by high frequency voltage drops on the equivalent grid inductance (L_{grid}) and the grid resistance (R_{grid}).

Commonly accepted figure of merits for the PEC current and its effects on PCC voltage (V_{PCC}) are total harmonic distortions of the voltage (THD_V), and current (THD_I), and total demand distortion (TDD) as described in (2.1) , (2.2), and (2.3) respectively. Among these, the THD_I is generally limited to 5% by most of the related standards. The limits of these standards are depicted in Table 2.1. Besides, unlike grid-connected diode rectifiers, the harmonic emission of grid-connected PV-PECs is reasonable, since the PV-PEC current is generally generated using pulse width modulation (PWM). Therefore, even in the low loading circumstances, grid-connected PV-PECs generally do violate neither the THD_I limits nor the

individual current harmonic limits set by the standards IEEE 1547, IEC 61727, and EN 61000-3-2 (Table 2.1) [34], [40], [41]. Similar to the case in the THD_I, the TDD is usually low in PWM based grid-connected PV-PECs.

The PCC voltage harmonics should be also low in order to preserve the voltage quality. Therefore, the THD_V is regulated by the standards such as IEEE 519, IEEE 1159 and EN 50160. Among these, EN 50160 limits on the individual voltage harmonics are also listed in Table 2.1 [40].

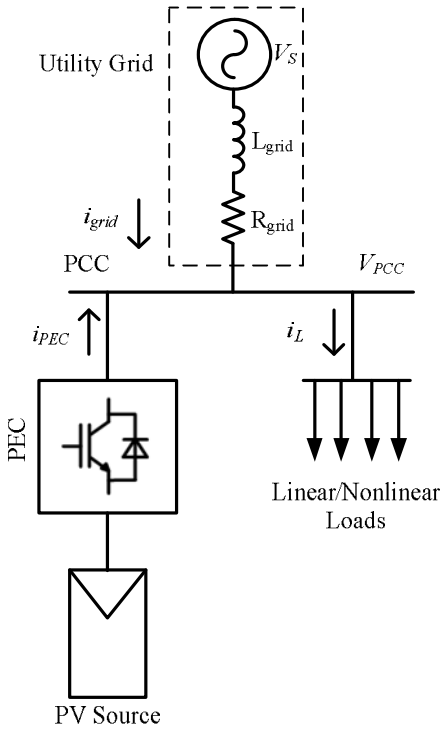


Figure 2.6 Single line diagram for grid-connected PV-PECs.

$$THD_I \triangleq \frac{\sqrt{\sum_{h=2}^{h_{max}} I_h^2}}{I_1} \tag{2.1}$$

$$THD_V \triangleq \frac{\sqrt{\sum_{h=2}^{h_{max}} V_h^2}}{V_1} \tag{2.2}$$

$$TDD \triangleq \frac{\sqrt{\sum_{h=2}^{h_{max}} I_h^{\,2}}}{I_L} \tag{2.3}$$

where I_h and V_h are the h^{th} current and voltage harmonics' RMS values, and I_L is the RMS value of the rated equipment current respectively.

Table 2.1 Harmonic current limits specified in IEEE 1547, IEC 61727, EN 61000-3-2, and harmonic voltage limits in EN 50160 [34], [40], [41].

	IEEE 1547	***IEC 61727***	***EN 61000-3-2***		***EN 50160***
	Odd (%) (Current)	***Odd (%) (Current)***	***Odd (A)***	***Even (A)***	***Odd (%) (Voltage)***
(h-number) h-level	(2-10) 4 (11-16) 2 (17-22) 1.5 (23-34) 0.6 (>35) 0.3 ***Even:*** *25% of odd harmonics* THD_I <5%	(3-9) 4 (11-15) 2 (17-21) 1.5 (23-33) 0.6 ***Even:*** *25% of odd harmonics* THD_I <5%	(3) 2.3 (5) 1.14 (7) 0.77 (9) 0.4 (11) 0.33 (13) 0.21 (15-39) 2.25/*h*	(2) 2.3 (4) 1.14 (6) 0.77 (8-40) 1.84/*h*	(3) 5 (5) 6 (7) 5 (9) 1.5 (11) 3.5 (13) 3 (15) 0.5 (17) 2 (19) 1.5 (21) 0.5 (23) 1.5 (25) 1.5 ***Even:*** (2) 2 (4) 1 (6-24) 0.5

The current and voltage harmonic restrictions can be usually met by the new generation PV-PECs based on PWM operation. In spite of the harmonic content superiority of these PV-PECs, they may cause voltage rise at the PCC, at unity power factor operation, which is briefly investigated in the next section.

2.4.1.2 Reactive Power and Power Factor

Apart from the high frequency (switching frequency and above) effects of a grid-connected PEC, fundamental component of the converter (i_{PEC-1}) can bear problems on the PCC voltage (V_{PCC}). In order to increase the efficiency of a grid-connected PV system, inverters generally operate at unity power factor already. According to [40], among the standards IEEE 1547, DIN-VDE-0126-1-1, and IEC 61727, only IEC 61727 specifies a power factor limit, which is, the PV inverter shall have an average lagging power factor greater than 0.9 when the output power is greater than 50%.

In the case of power injection by the PEC at unity power factor, and the loading is not high by other customers, or in the case of there exist other PECs or distributed sources to supply excess power to flow through the distribution transformer to the utility grid, the V_{PCC} can exceed nominal values that are allowed by the grid standards as depicted for a no-loading case by local loads in the equivalent circuit, and the phasor representation in Figure 2.7 (*a*) and Figure 2.7 (*b*) respectively. If the voltage rise at PCC is not prevented, the PEC is required to be disconnected from the grid by standard restrictions, which is an undesired operation.

One measure to prevent the PCC voltage (V_{PCC}) rise is to decrease the injected power at unity power factor to the utility grid. Nonetheless, this is also an unwanted situation, since the power available from the PV source cannot be injected to the utility grid completely. Another solution to the V_{PCC} regulation problem is to inject reactive power to the grid. As V_{PCC} rises, leading PEC current ($i_{PEC\text{-}1}$) is injected to the grid within the current capabilities of the semiconductors of the PEC. In Figure 2.7 (*c*), the regulation of V_{PCC} is illustrated by reactive power injection by the PEC.

In most cases, this solution is more feasible than only limiting the real component of the current to the utility grid, since the available PV source power can be transferred to the utility grid almost completely. However, the PEC power capability derating should be taken into consideration to match the PEC to the PV source under full loading conditions. Moreover, while the PEC is supplying reactive power, its efficiency characteristics slightly deteriorates because of the reactive component of the injected current.

In the future, the reactive power supply ability is expected to be necessary for bulk generation. Actually, static grid supply by reactive power injection at medium voltage level of grid-connected converters is required in new standards specifically in Germany [39]. Therefore, topologies with reactive power capability are expected to be more preferable in future PV distributed generation systems.

This section surveyed the current, and the voltage harmonic issues, and several limits on the harmonic current injection, and harmonic voltage distortions are listed. In addition, PCC voltage regulation problem is investigated, and the reactive power capability is found to be necessary for future distributed generation systems. Nevertheless, besides these power quality issues, there exist system protection, and human safety issues, such as DC current injection, and capacitive leakage currents etc. These issues are studied in the next section.

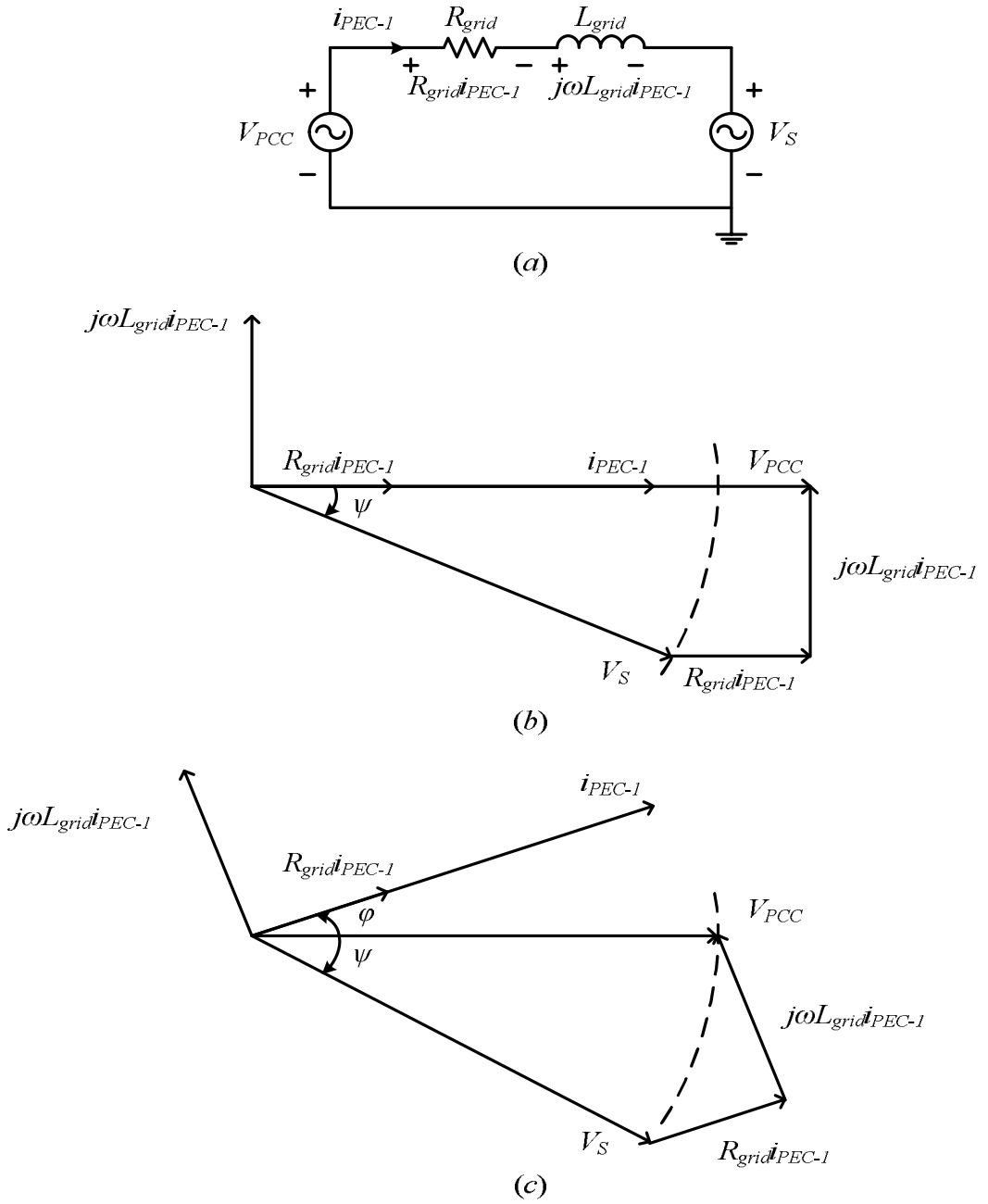


Figure 2.7 Equivalent circuit (*a*) and the phasor representation (*b*) of PV-PEC power injection at unity power factor for voltage rise illustration at PCC with negligible local loads, (*c*) PCC voltage regulation by reactive power injection.

2.4.2 System Protection and Safety

Human safety and grid protection restrictions are the musts to be fulfilled in connecting the PV sources to the grid. Especially in GCTSIs, these restrictions should be handled more

carefully due to the absence of a galvanic isolation. The inverter should be designed by selecting an appropriate topology to operate under normal circumstances and disconnect from the grid or the PV source under fault conditions. Therefore, while the inverter is connected, PV source side and the grid side should be continuously observed for possible faults or overloading conditions and counter measures should be taken.

2.4.2.1 Nominal Voltage and Frequency

A grid-connected PV-PEC should be able to manage grid faults for safety reasons. As the electricity is not available from the grid side by either of an open circuit or a short circuit, the PEC must be disconnected from the grid in order to prevent electrocution of technical personnel. Moreover, in the case of over voltage or under voltage cases, the converter is required to be disconnected, which is stated in IEEE 1547, IEC 61727, and VDE 0126-1-1 as listed in Table 2.2. Disconnection is also required in the case of frequency deviations in order to prevent the power system instability. The anti-islanding should be performed in certain time durations for these intentions. The disconnection times are also listed in Table 2.2.

Table 2.2 Under-voltage, over-voltage and under-frequency, over-frequency disconnection times specified in IEEE 1547, IEC 61727, and VDE 0126-1-1 [40].

	IEEE 1547		***IEC 61727***		***VDE 0126-1-1***	
	Voltage Range (%)	*Disconnection Time(sec.)*	*Voltage Range (%)*	*Disconnection Time(sec.)*	*Voltage Range (%)*	*Disconnection Time(sec.)*
Voltage	$V < 50$ $50 \leq V < 88$ $110 < V < 120$ $V \geq 120$	0.16 2.00 1.00 0.16	$V < 50$ $50 \leq V < 85$ $110 < V < 135$ $V \geq 135$	0.10 2.00 2.00 0.05	$85 > V$ $110 \leq V$	0.2 0.2
Frequency	*Frequency Range (Hz)*	*Disconnection Time(sec.)*	*Frequency Range (Hz)*	*Disconnection Time(sec.)*	*Frequency Range (Hz)*	*Disconnection Time(sec.)*
	$59.3 < f < 60.5$	0.16	$f_n\text{-}1 < f < f_n+1$	0.2	$47.5 < f < 50.2$	0.2

2.4.2.2 Leakage Current

As in the case of grounding any conductive chassis of electric equipment for safety reasons, the conductive surfaces of PV modules should be grounded to prevent any hazardous event due to module surface to earth voltage or any insulation failures in the modules. Capacitance exists between any two points in physical world, and as the surfaces of PV modules are large in area, the capacitance between the cells and the surface is not negligible to introduce leakage currents caused by the PEC itself. These leakage current levels are also non-negligible, such that they are prohibitive for safety and maintenance issues. Figure 2.8 illustrates parasitic capacitors existing between the cells and the surface of the modules. As the total surface of the PV sources increases, or the thickness of PV modules decreases, the equivalent parasitic capacitor of the PV system increases.

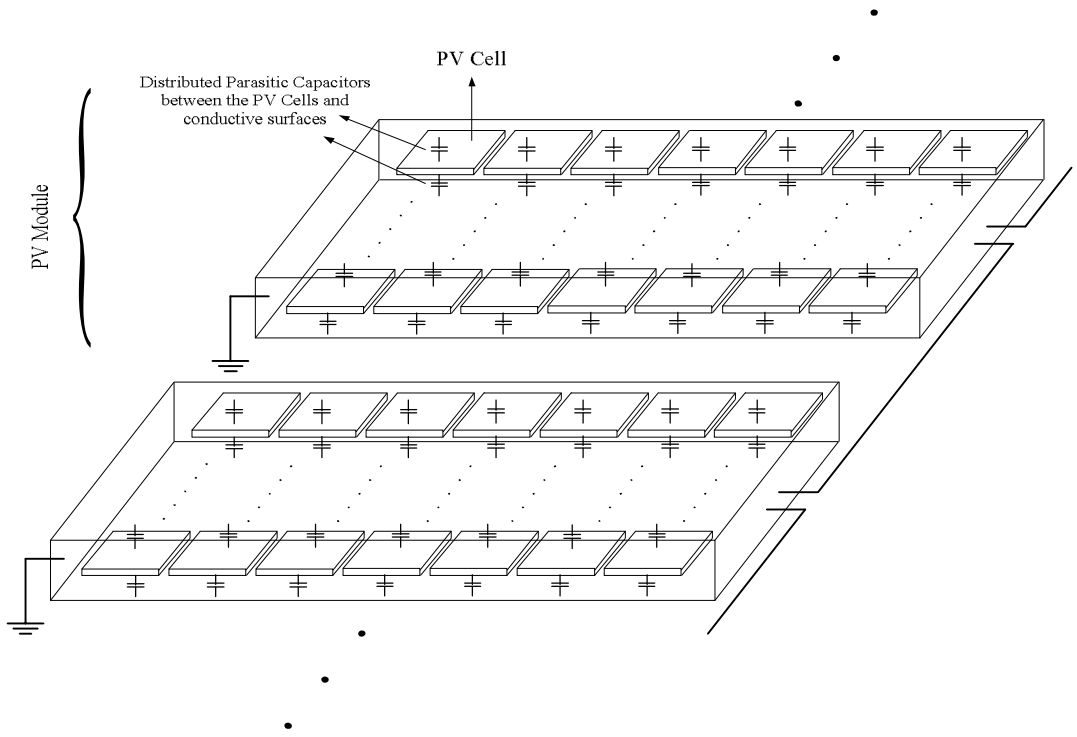


Figure 2.8 Illustration of the distributed PV cell parasitic capacitors between the live parts and the conductive surfaces of PV modules, which are grounded.

The sum of the total of the distributed capacitances between the PV cells and the positive rail and the total of the distributed capacitance between the cells and the negative rail is called the parasitic capacitor throughout the thesis. Because of large areas, the parasitic capacitance that is module geometry, module structure and environmental condition (such as dust and

humidity) dependent, can reach 1μF for 1 kW of installed peak power (1μF/kW_p) [11]. This capacitance is calculated in a similar manner as in classical capacitance calculation by making use of the module geometry [21]. Because of grounding PV modules and the parasitic capacitance of the PV modules, these modules become vulnerable to leakage currents especially for the case of GCTSIs due to the lack of galvanic isolation. For large values of system capacitance (C_p) the leakage current degrade the efficiency of thin-film modules [19], create EMI problems [20], disrupt protection coordination and introduce extra losses [22], and line current distortion [23]. For these reasons, a grid-connected GCTSI is required to include a residual current monitoring unit to watch the leakage current by DIN-VDE 0126-1-1 standard. This standard also limits the rms value of leakage current in PV systems to 300 mA. Moreover, according to this standard, even a jump in the leakage current requires disconnection of the inverter as specified in Table 2.3. Due to these restrictions on leakage current and due to the aforementioned drawbacks of leakage current, several GCTSIs are invented with low leakage current characteristic. In this thesis, these GCTSI topologies are one of the focuses with their leakage current attributes and new methods and topologies are proposed to decrease the leakage current in GCTSIs.

Table 2.3 Leakage current rise disconnection times specified in VDE 0126-1-1.

Leakage Current Increase (mA)	***Disconnection Time (sec.)***
30	*0.30*
60	*0.15*
100	*0.04*

2.4.2.3 DC Current Injection

Since there is no line frequency transformer in GCTSIs, these inverters may inject DC currents to the utility grid. If the DC current is not prevented, it decreases the power rating of the distribution transformer and decreases the system energy efficiency by causing additional losses both in the grid side and in the inverter side. Moreover, the DC component may saturate the distribution transformer. To avoid these drawbacks, the DC current injection is limited in several standards as listed in Table 2.4 in [34], [40], and [41].

Table 2.4 DC current injection limits specified in IEEE 1547, IEC 61727, VDE 0126-1-1, and EN 61000-3-2.

	IEEE 1547	***IEC 61727***	***VDE 0126-1-1***	***EN 61000-3-2***
DC Current Injection	*< 0.5% of rated output current*	*< 1% of rated output current*	*< 1 A*	*< 0.22 A*

2.5 Summary

In this chapter, a brief survey of the requirements of the three correlated basic blocks of a PV-PEC system is conveyed. First, the MPPT requirement of PV source is addressed, and then basic MPPT distribution schemes are presented. After the PV source related issues, PV-PEC related requirements are investigated. Among these, the effect of efficiency is emphasized. Following these, the utility grid related restriction and requirements, such as power quality, and system protection and safety are studied. Apart from other grid-connected equipment, the leakage current restrictions and requirements of GCTSIs are pointed out.

Although for the time being, there is some favouring towards the PV systems, in the future these systems are expected to be subject to the similar standards for other sources like fossil fuel based or small-hydro generators. Moreover, the PV systems may encounter additional restrictions such as reactive power supply, or harmonic filtering to achieve high power quality. Considering these, it can be concluded that, PV-PEC topologies with reactive power capability, low leakage current, and high efficiency characteristics will be highly preferable in the future.

Having addressed basic restrictions and requirements related to PV-PEC interconnection, next chapter studies the existing PV-PEC topologies and mainly focuses on the investigation of GCTSIs.

CHAPTER 3

A SURVEY OF GRID-CONNECTED SOLAR INVERTER TOPOLOGIES, THEIR CLASSIFICATION, AND EXTENSION

3.1 Introduction

As discussed in the previous chapter, grid-connected PV systems have several restrictions to be obeyed. Among the other parts of a PV system, PV-PECs have the most of the responsibility of satisfying these restrictions, while sustaining high efficiency, reliability, and overall safety of the system. Therefore, increasing in the last ten years, grid-connected PV-PECs become the focus of investigation. Because of this focus, many grid-connected PV-PEC topologies are invented recently, in addition to the existing converter topologies adapted for grid-connected PV applications.

In the application, grid-connected PV systems generally consist of three types: The Module Integrated Converter (MIC) based sub kilowatt single-phase units, the large-scale solar farm type 100 kW-1 MW rated units, and finally the kW range single/three-phase units. Of these, the MIC based units and the large-scale type converters correspond to a smaller portion of the applications, while the kW range units have dominated the field largely, due to the demand, specifically in residential applications. Of the kW range converters, the transformerless technology is developed to provide higher efficiency, lower cost, lighter weight and reduced size as compared to their transformer based counterpart. Therefore, transformerless systems are increasingly dominating the market. However, due to lack of galvanic isolation, the leakage current in such systems becomes an issue for safety, reliability, protection coordination, electromagnetic compatibility, and lifetime (especially for some thin film module types). Thus, the leakage current has become one of the major figures of merit for evaluating such systems (the lower the better). As the leakage current characteristic is mostly determined by the converter topology, this chapter surveys the PV-PECs, and classifies them in terms their leakage current characteristics, where high

efficiency Grid-Connected Transformerless Solar Inverter (GCTSI) topologies are the major focus due to the benefits.

In the literature, high efficiency GCTSI topologies are investigated extensively [18], [44]; however a survey focusing on high efficiency GCTSI topologies in terms of their leakage current characteristics is absent. Therefore, first, the classification, and then the survey of GCTSI topologies with respect to their leakage current characteristics are performed in this chapter. The proposed classification helps engineers to evaluate the pros/cons of a PV-PEC topology used under different conditions (such as high parasitic capacitance of the PV panel, weak grid etc.), and aids in selecting among the vast variety of topologies. In particular, classification based on the leakage current approach yields an improved understanding of converter behaviour to help future development of new GCTSI topologies, and reduces the complexity (instead of learning each topology with difficulty, learning the common properties and emphasizing the small differences). Based on this approach, the family has been expanded with newly proposed topologies in the survey. In the survey, focus is placed especially on the single-phase GCTSI topologies. However, as in the application, single-phase units are put together to establish three-phase systems (by numerous leading manufacturers), thus, the classification covers three-phase applications as well. Power rating also is increased with up-scaling converters or paralleling them, therefore the application range of such topologies extends to tens of kilowatts. Thus, a wide range of applications is included in the survey. The indexes of the diodes that are parallel to an active switch are the same as the indexes of the corresponding parallel active switch. This assignment is carried on throughout the thesis.

3.2 Grid-Connected PV-PEC Topologies

Grid-connected PV-PEC topologies differ from other topologies in various attributes especially in terms of leakage current immunity due to the drawbacks of high leakage current studied in section 2.4.2.2. Therefore, not every inverter topology can be utilized as a PV-PEC. Apart from other inverters used for various applications such as UPS systems, grid-connected PV-PECs are evolving to sustain low leakage current due to inherent distributed parasitic capacitance of PV modules.

Grid-connected power electronic converters can be classified according to their leakage current characteristics; transformer-based and transformerless. In the transformer-based

converters, the path for the leakage current is inherently confined by the galvanic isolation by introducing additional losses caused by the transformer to the system. In the case of transformerless systems, the absence of the transformer increases the efficiency; reduce the size, and the cost of the converter. However, omission of the transformer introduces leakage current path, which is not galvanically disturbed. According to the reduction of leakage current in these systems, GCTSI topologies are subdivided into two major classes as depicted in Figure 3.1.

The first class of GCTSI topologies focuses on the problematic zero vectors (or zero output voltages, which yield high common mode voltage, thus high leakage current) of conventional unipolar switching pattern of the H4 topology (the standard full bridge inverter). According to the strategy used at zero vectors, this class of GCTSIs can be subdivided into three different subclasses. The first subclass has an approach to decouple AC and DC circuits at zero vectors. In the second approach, AC grid is connected to the midpoint of the DC bus at zero vectors. In the third approach, the decoupling of the first class and the midpoint connection of the second class are used interchangeably, constituting a hybrid characteristic.

The second class of GCTSI topologies realize a solid connection between the AC, and the DC circuits (grid side, and the PV source side respectively). In this class, the intention is to keep the equivalent parasitic capacitor voltage constant or varying at most at the line frequency. Depending on the parasitic capacitance, because of no variation or slow variation in the capacitor voltage, the parasitic capacitor current becomes as low as to cause no considerable damage to the overall system or not to cross standard limitations.

In Figure 3.1, the classification of solar inverters with respect to aforementioned leakage current reduction characteristics is illustrated. In the chart, several representative topologies are listed under the classes. Among the listed, PT-1 denotes “proposed topology 1” and similar assignment is maintained for other proposed topologies throughout the thesis.

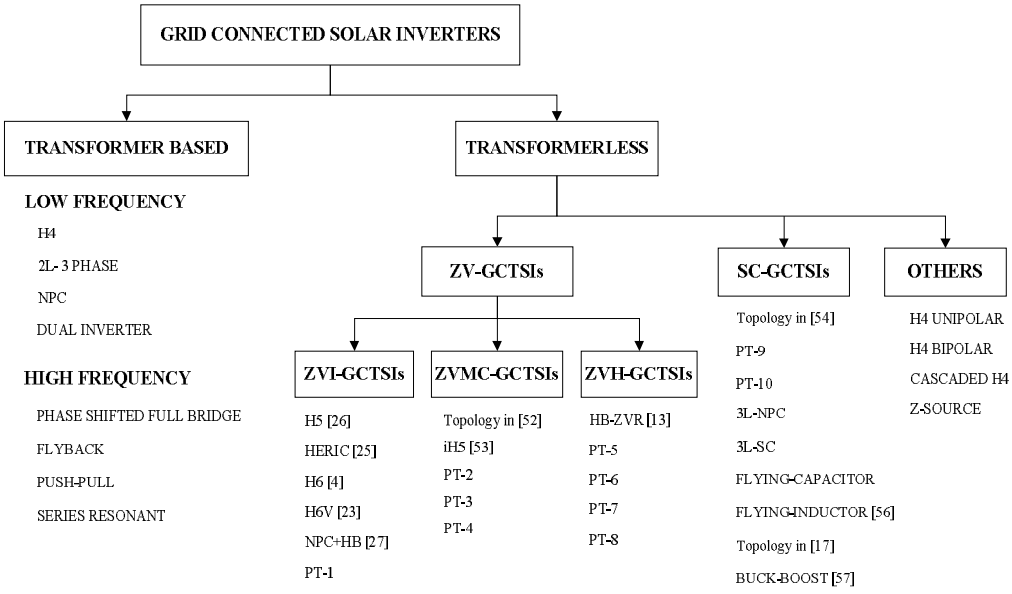


Figure 3.1 Illustration of classification of GCSI topologies (representative members selected only).

Having classified the grid-connected solar inverters in terms of their leakage current reduction strategy, next section is devoted to a brief investigation of the existing topologies, and the proposal of new topologies. Among these, the switching schemes of proposed topologies and of similar topologies are provided.

3.2.1 Transformer Based PV-PEC Topologies

Topologies with direct galvanic isolation by means of transformers can be put to the class of low leakage current topologies, as their parasitic current path is naturally confined. Therefore, in such topologies, the leakage current is only dependent on the transformer parasitic capacitances, which are usually very low; the leakage current is generally not an issue in such topologies. The transformer is often provided for the purpose of voltage level adjustment and the reduced leakage current is an additional benefit. In some cases, it is used mainly to confine the leakage current, which would otherwise violate the grid code with direct connection of the converter to the grid. Regardless, when a transformer used, the leakage current becomes small and no major grid code issues or other drawbacks arise regarding its value. The transformer-based topologies can be classified in two groups as low frequency and high frequency transformer based topologies. In the kW range, typically, high frequency transformer based topologies are used and low frequency transformer technology

based solutions are in use with a decreasing demand, due to their efficiency, size, weight, and cost drawbacks. The low frequency transformer and the high frequency transformer based PV-PECs are briefly investigated in the following two sections.

3.2.1.1 Line Frequency Transformer Based PV-PEC Topologies

In the connection of PV energy sources, use of line frequency transformer based topologies is old as compared to their transformerless counterparts. Due to the grid codes, grounding requirements of some module types, and voltage boosting needs, low frequency transformer remained in utilization for various grid-connected PV systems with a decreasing demand. The line frequency transformers are an interface of PV system to the either of the low voltage, or medium voltage distribution system (in PV farms). Figure 3.2 illustrates a classical line frequency transformer based PV-PEC with the H4 topology. The H4 topology with unipolar switching is found to be inapplicable as a GCTSI in [13], [17], [18], and [24]. However, with a low frequency transformer, the topology can be used as a grid-connected PV-PEC.

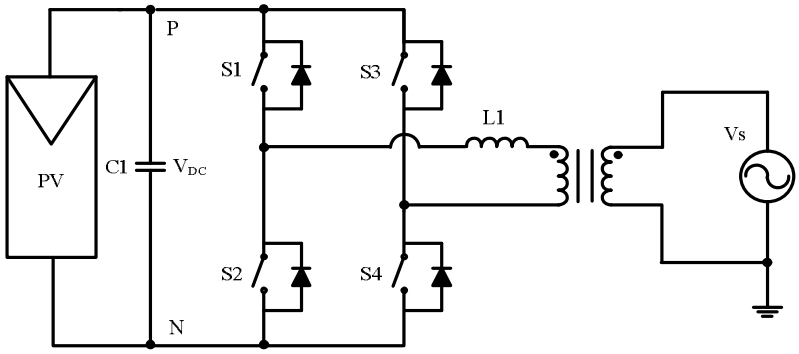


Figure 3.2 Line frequency transformer based PV-PEC with the classical H4 topology.

In Figure 3.3, classical three-phase, three-wire, two-level voltage source inverter with low frequency transformer grid connection is depicted as a three-phase variant of the H4 topology. The leakage current attributes of the topology makes it not applicable as a GCTSI, but the topology is well suited for line frequency transformer based applications especially for large-scale PV systems.

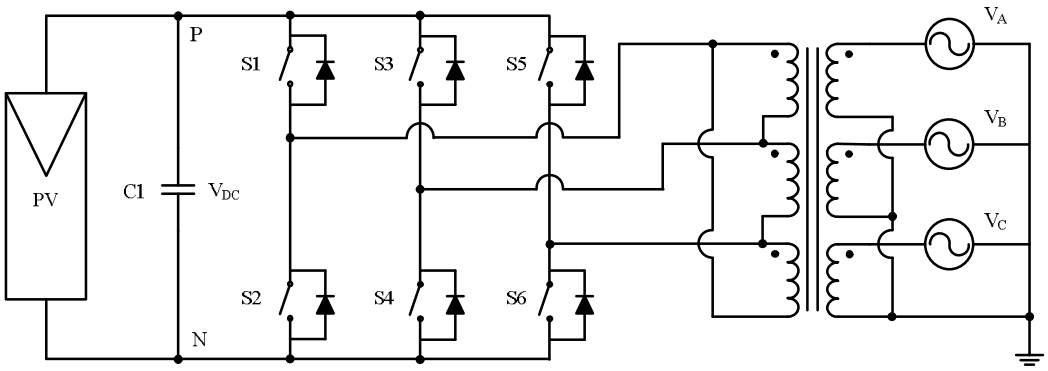


Figure 3.3 Line frequency transformer based three-phase, three-wire, two-level voltage source inverter topology for PV-PEC systems.

In Figure 3.4, low frequency transformer based dual inverter [45] is illustrated for the exemplification of low frequency transformer based large-scale PV system applications. Being less complex than multilevel topologies, the dual inverter topology has the advantages of multilevel inverters, such as reduced output voltage harmonics, reduced *dv/dt*, and reduced semiconductor stresses. However, in this topology, circulation of leakage currents between the upper and lower systems can be encountered, instead of flowing through the grid.

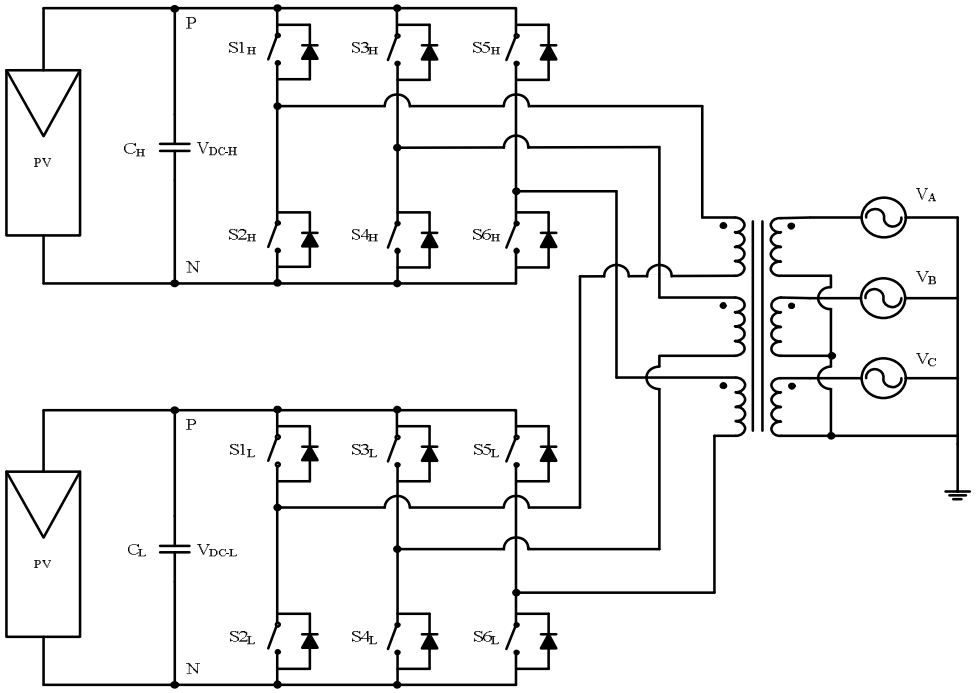


Figure 3.4 Line frequency transformer based PV-PEC with the dual inverter topology for large-scale PV systems proposed in [45].

Any GCTSI topology is applicable as a low frequency transformer based PV-PEC. However, efficiency drawbacks and galvanic isolation benefits should be evaluated before putting into application.

3.2.1.2 High Frequency Transformer Based PV-PEC Topologies

In high frequency transformer based PV-PECs, the weight, size, and cost drawbacks of low frequency transformer based structures are eliminated. The size of the transformer in these systems is reduced due to high frequency utilization of the transformer instead of 50/60 Hz operation. High frequency transformers are utilized in both medium power converters (1-10 kW) and MICs (100-500 W). In the first category, the transformer's main duty is to transmit power from PV source side to grid side in a most efficient manner with the provision of galvanic isolation. Besides, the transformer can be used to boost voltage. Figure 3.5 illustrates a high frequency transformer based PV-PEC with the phase shifted full-bridge topology [46].

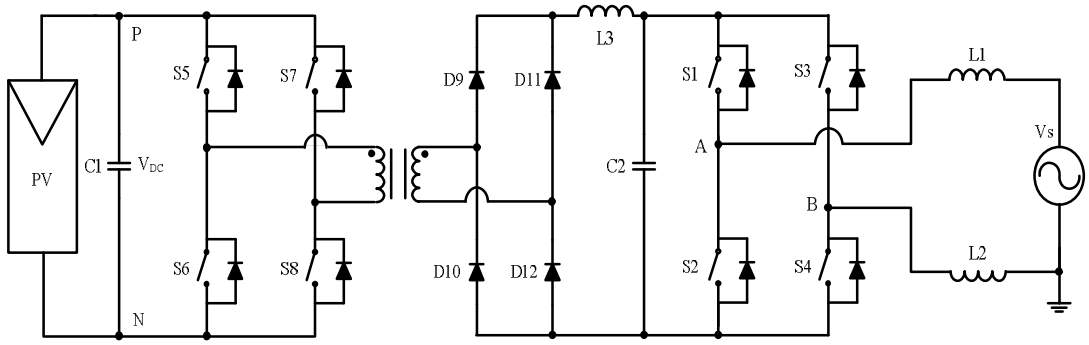


Figure 3.5 High frequency transformer based PV-PEC with the phase-shifted full bridge topology [46].

In MICs, the main aim of the use of high frequency transformer is mainly used to boost module voltage; since an inverter accompanies each module therefore the voltage of the module (20-70V) is not enough to inject sinusoidal current to low-voltage public grid. In these converters, resonant operation, pulse skipping, burst mode, or interleaving of the converters are the techniques to increase the conversion efficiency, which are beyond the scope of this thesis.

MIC topologies are abundantly existent in the literature [35], [47], [48], [49], [50], [51] and several interesting and high efficiency topologies among these topologies are given in Figure 3.6-3.8. The topology given in Figure 3.6 [49] is a flyback type converter, whereas the topology in Figure 3.7 [50] is derived from a push-pull converter. The topology in Figure 3.8 is a high efficiency resonant type converter proposed in [51].

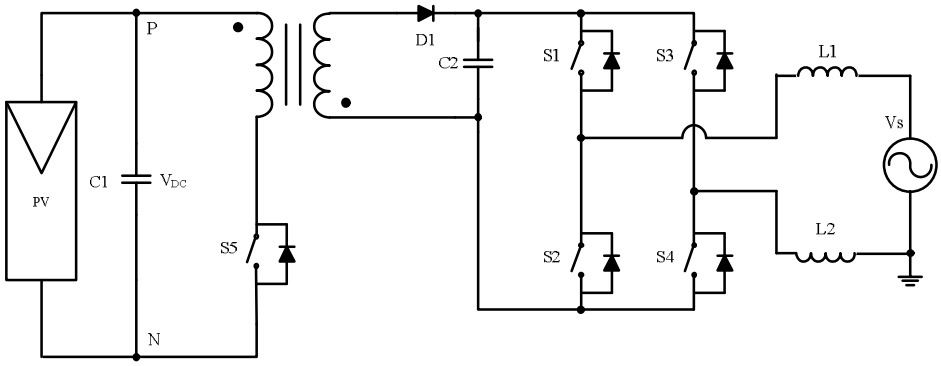


Figure 3.6 Flyback type MIC topology [49].

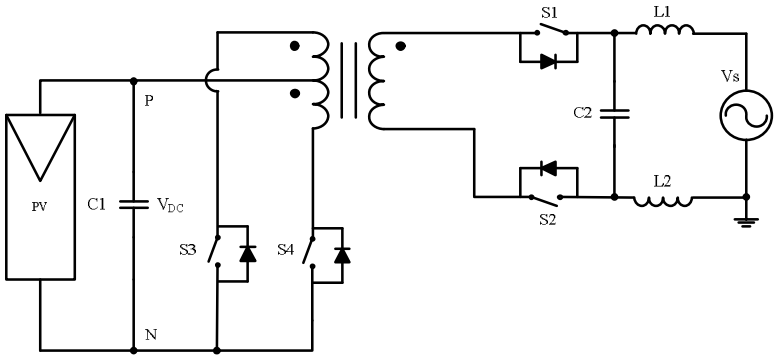


Figure 3.7 Push-Pull type MIC topology [50].

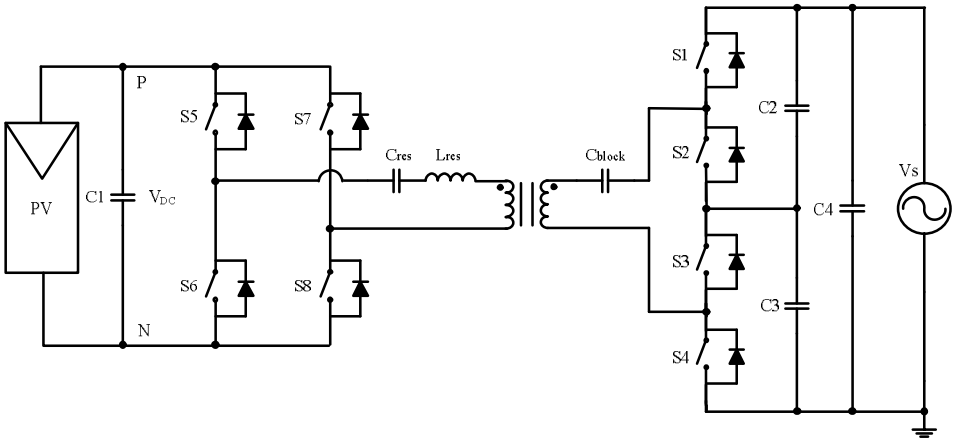


Figure 3.8 Resonant type MIC topology [51].

In this section, transformer based topologies are overviewed. In these topologies, the inclusion of galvanic isolation with a high frequency or a low frequency transformer reduces the system energy conversion efficiency due to core and copper losses of the transformer. In transformerless solar inverters, these losses are nonexistent. In the next section, a brief survey on transformerless solar inverters is conducted, and several new topologies are introduced.

3.2.2 Transformerless PV-PEC Topologies (GCTSI topologies)

As compared to their transformer-based counterparts, GCTSIs have the advantages of low cost, high reliability and high conversion efficiency [11]-[17]. Among these benefits of GCTSIs, conversion efficiency and reliability have high importance, as the converters are expected to be loaded at least five hours a day for several years. These benefits of transformerless inverters yielded high acceptance.

The conventional full-bridge (or H4, or H-bridge) inverter (illustrated in Figure 1.5 and Figure 3.40) is the root topology for many inverter topologies. In its naive form, it is operated either with unipolar PWM pattern, where the reference voltage and output voltage share the same polarity, or with bipolar switching pattern, where the output pulsates between the positive and negative rail continually. The unipolar PWM approach has several advantages such as three-level output voltage (less filter current ripple) and reduced internal reactive power circulation at unity power factor, which means higher efficiency than bipolar PWM. Besides, its low DC bus voltage requirement compared to Neutral Phase Clamped (NPC) derived topologies reduces the additional boosting requirement of the input voltage and the associated excessive boosting losses. Contrary to the aforementioned advantages of unipolar switching pattern of the H4 topology, it is inapplicable as a GCTSI because of the varying Common Mode Voltage (CMV) of the topology [13], [17], [18], [24]. In the H4 topology unipolar switching pattern, CMV is half of the DC bus voltage at active vectors, and becomes either zero or DC bus voltage at zero vectors, dependent on through which rail does the line current freewheel (to be studied in detail in chapter 4). Therefore, many of GCTSI topologies are invented in recent years and extensive investigation continues.
According to their mechanism to prevent excessive leakage currents, GCTSIs can be mainly subdivided into two; Zero Vector GCTSI (ZV-GCTSI) topologies and Solidly Clamped GCTSI (SC-GCTSI) topologies as depicted in Figure 3.1.

3.2.2.1 ZV-GCTSI Topologies

In ZV-GCTSI topologies, problematic zero vectors of H4 unipolar modulation are handled such that the varying CMV induces no current on the equivalent parasitic capacitor of PV modules. As illustrated in Figure 3.1, ZV-GCTSI topologies are divided into three subclasses with respect to the strategy utilized in these zero vectors.

The first group of ZV-GCTSI topologies is the ZVI-GCTSI topologies. As their name suggests, these topologies isolate (or decouple) AC and DC circuits at zero vectors. The second group is Zero Vector Midpoint Clamped GCTSI (ZVMC-GCTSI) topologies. In this group, the AC side is connected to the midpoint of the DC bus of the inverter at zero vector durations. The final group of ZV-GCTSI topologies, Zero Vector Hybrid GCTSI (ZVH-GCTSI) topologies, have leakage current characteristics such that the characteristics take the form of the characteristics of ZVI-GCTSIs and ZVMC-GCTSIs interchangeably in time depending on the sign of the change of the grid voltage.

In the following three sections, the three subgroups of ZV-GCTSI topologies with the concerning topologies are investigated. Since most of the gate logic signals of these topologies are common, they are not repeated at each time, but these signals are drawn in Figure 3.9 to be assigned to each controlled device of the concerning ZV-GCTSI topology. In addition, theoretical current waveforms for the power semiconductors of these topologies are provided for a full grid period in Figure 3.10 in order to clarify the operation of these topologies further. These theoretical current waveforms are assigned to power semiconductors of the topology under investigation. The currents i_1, i_3, i_4 flow at active vectors and the currents i_2, i_7, i_8 flow at zero vectors. The current waveforms i_7, i_8 represent the low frequency power semiconductor currents.

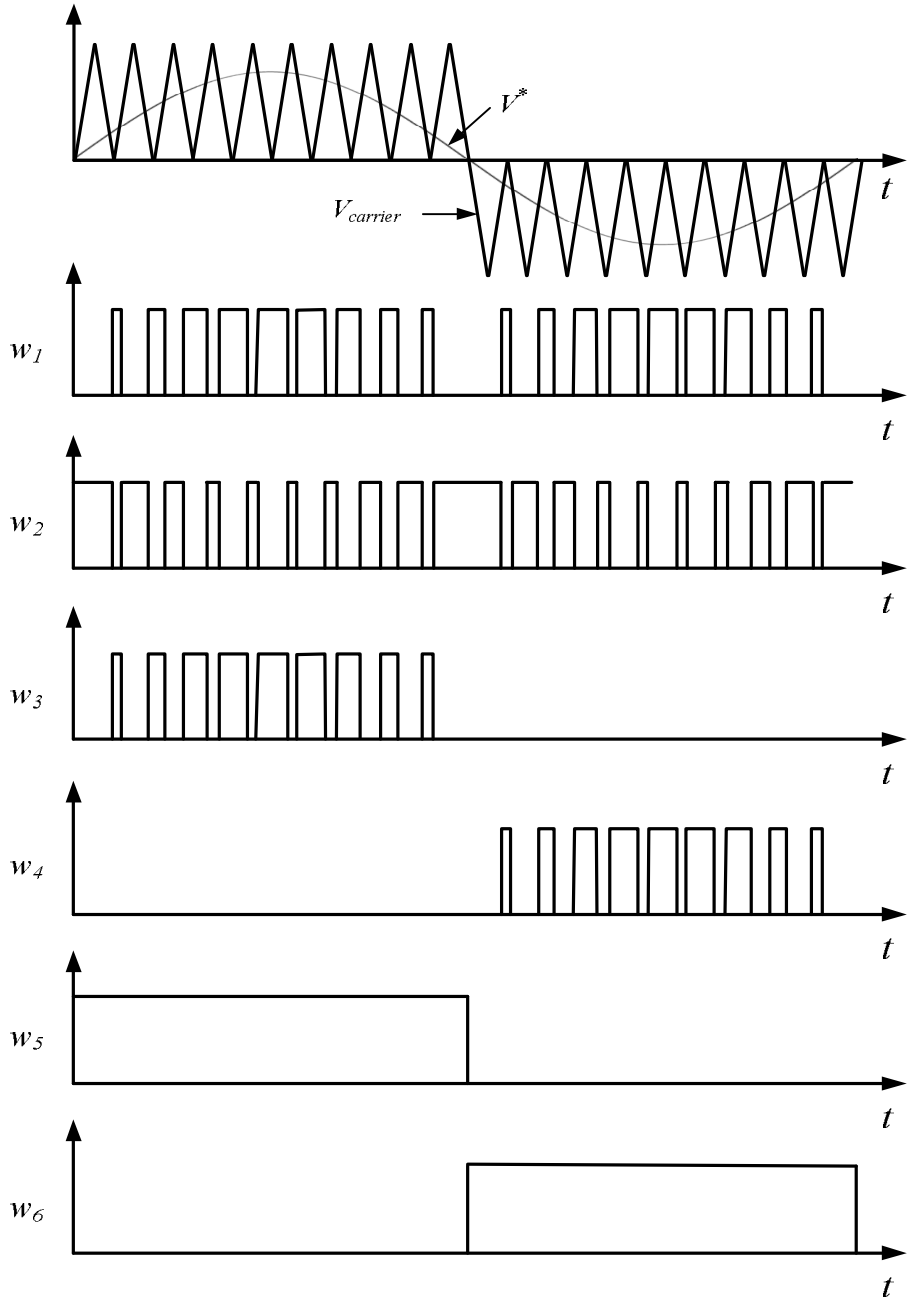


Figure 3.9 Common theoretical waveforms for the gate signals of active switches of ZV-GCTSI topologies at unity power factor.

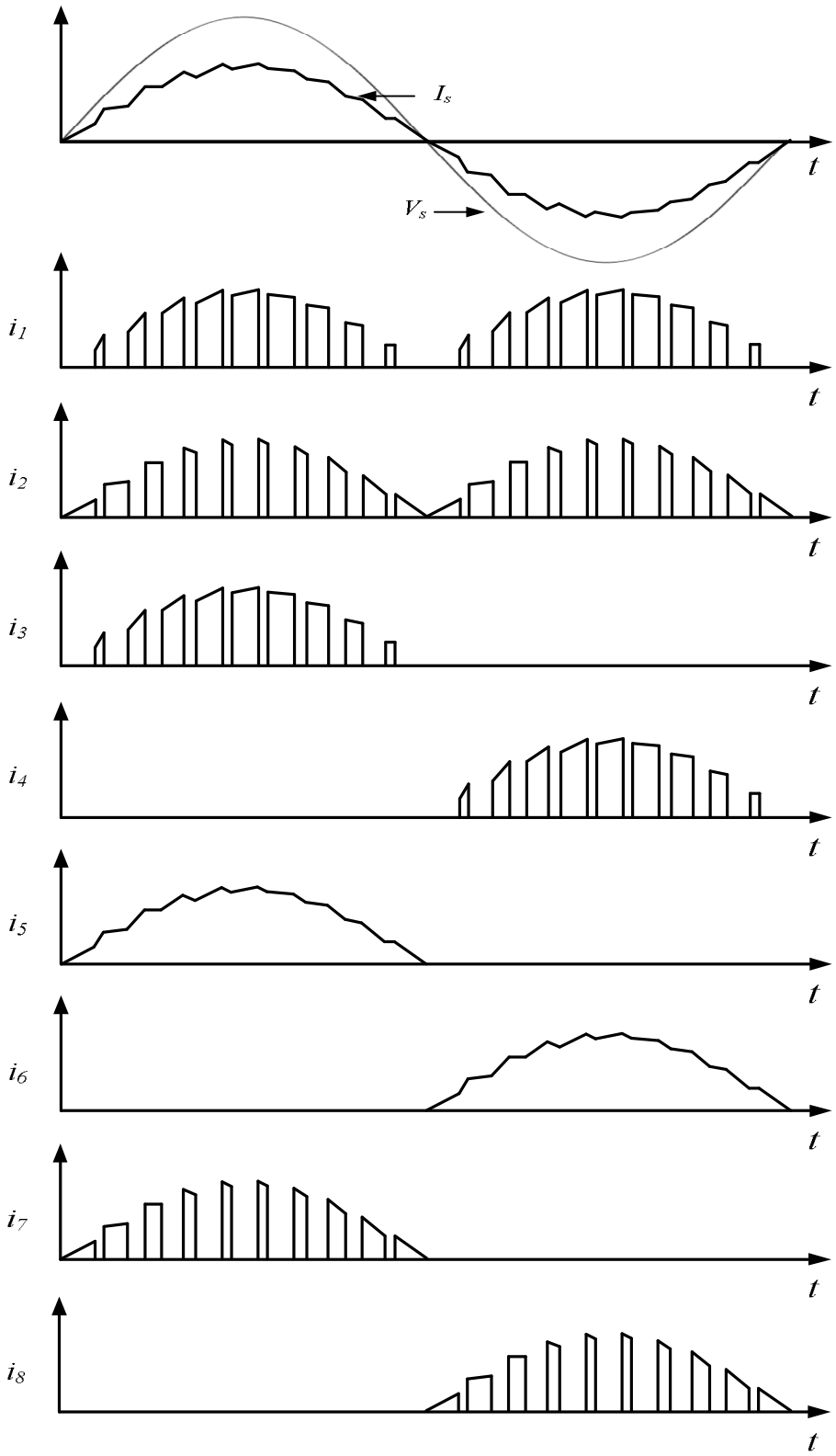


Figure 3.10 Common theoretical current waveforms for the power semiconductors of ZV-GCTSI topologies at unity power factor.

3.2.2.1.1 ZVI-GCTSI Topologies

The inverter family (ZVI-GCTSI) takes its name from the fact that these inverters provide reduced leakage current by means of isolating the AC and DC sides of the inverters via establishing switch configurations and operating in a manner to yield this condition during the inverter zero output voltage intervals. These topologies have several advantages like low DC bus voltage requirement, low leakage current and high efficiency characteristics. Moreover, these topologies do not require dead time, therefore dead-time compensation, as the switches on a DC bus short-circuiting path are not in conduction state in the same PWM cycle. As a consequence of 3-level output voltage characteristics of these inverters, there happens no power flow from AC side to the DC bus capacitor; therefore, high energy efficiency is yielded.

The power semiconductor currents and gate logic signals in ZVI-GCTSI topologies are mostly common as their output voltage and leakage current characteristics are same. The theoretical power semiconductor currents and the gate logic signals are assigned to concerning semiconductor by making use of the gate logic signals in Figure 3.9 and the theoretical currents in Figure 3.10.

In the ZVI-GCTSI topologies, active vectors are supplied in the same manner as in the H4 topology unipolar modulation, while zero vectors are obtained by some set of switches providing freewheeling and the others providing isolation. In the H5 topology [26] (3.11), isolation is achieved by S2, S4, S5 and freewheeling of the current is realized via the remaining switches (i.e. S1, S3, D1 and D3).

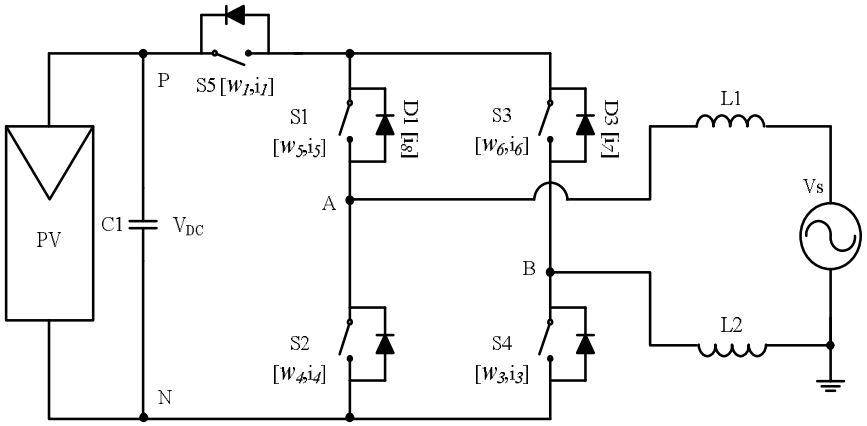


Figure 3.11 The H5 topology [26].

In the HERIC topology [25] (Figure 3.12), active vectors and isolation are realized by the same switches (S1, S2, S3, S4), whereas S5, D5, S6, D6 provides freewheeling. In the topology in [27], shown in Figure 3.13, (named hereafter as NPC+HB since it includes an NPC leg and a half bridge leg) S2, S3, D7 and D8 provide freewheeling while the rest of the switches separate AC and DC circuits.

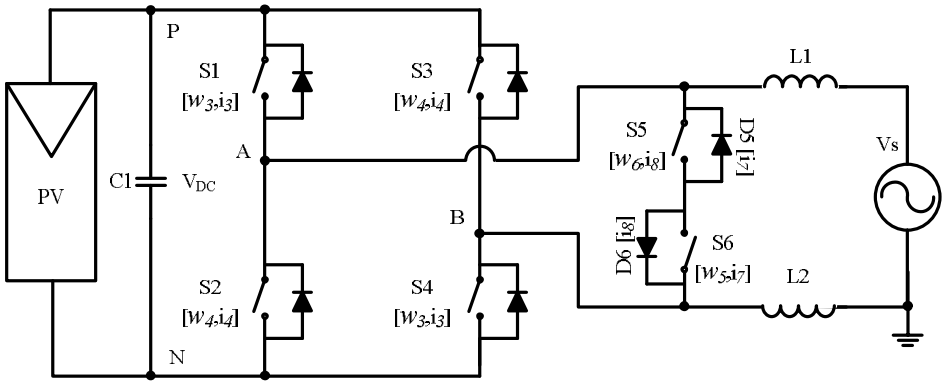


Figure 3.12 The HERIC topology [25].

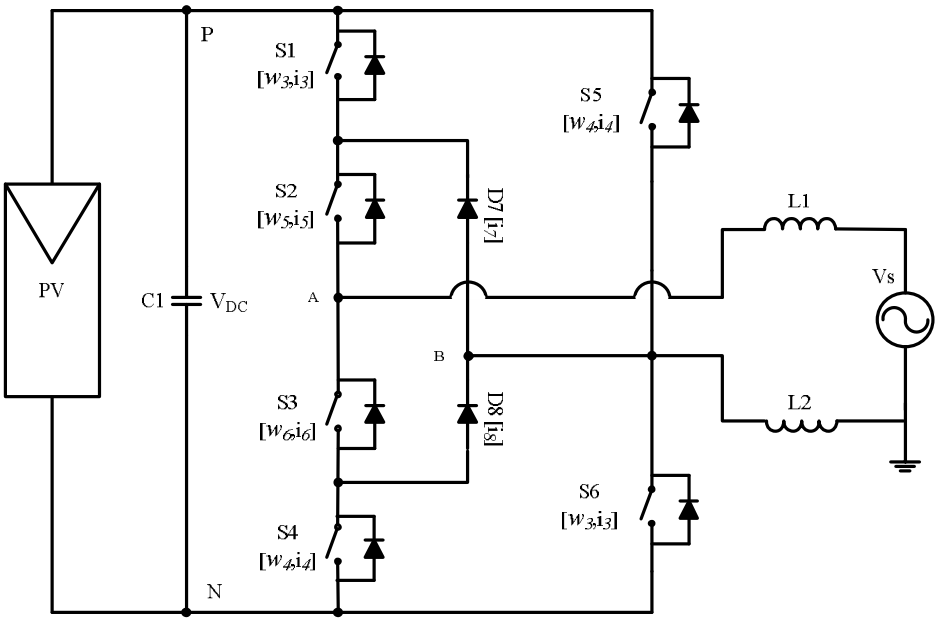


Figure 3.13 The NPC+HB topology [27].

The H6 configuration in [23] (Figure 3.14), named hereafter as H6V, achieves the separation with the switches S1, S2, S5, S6 and freewheeling with S3, S4, D7, D8. The H6 type inverter in [16] (Figure 3.15, called H6V hereafter) isolates DC and AC sides with S5 and S6 and freewheeling is accomplished with the remaining semiconductors in the topology.

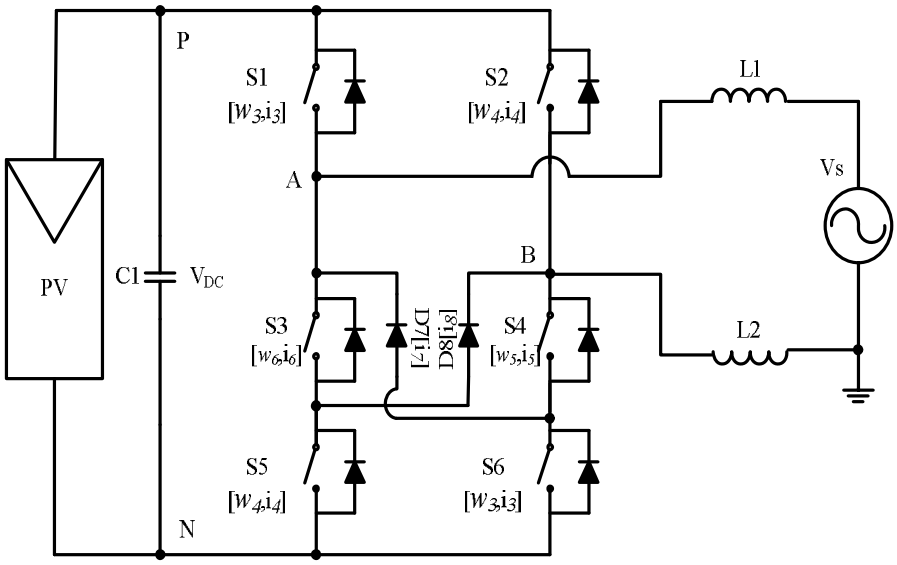


Figure 3.14 The H6V topology [23].

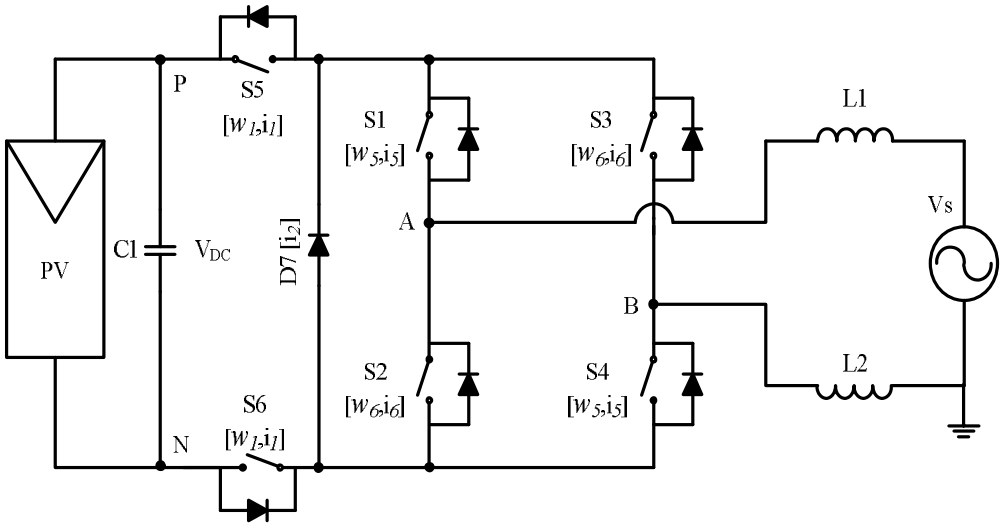


Figure 3.15 The H6 topology [16].

In addition to the aforementioned ZVI-GCTSI topologies, belonging to the same class, a new topology is proposed (PT-1) in this thesis (Figure 3.16 (top), published in [28]). As shown in Figure 3.16, the switches S1 and S4 provide positive active vectors at positive half cycle of the grid. Similarly, the switches S2, S3, and S5 provide negative active vectors at negative half cycle of the grid. The switches S1, S2, S4, and S5 realize decoupling of AC and DC circuits at zero vectors. Freewheeling of the line current is performed by S3, S6, D3 and D6

in these intervals. The switching pattern of this topology is also provided in Figure 3.16 (below). From the pattern, S3 and S6 are observed to be line frequency semiconductors whereas the others being high frequency semiconductors. The proposed topology exhibits efficiency characteristics similar to H5 and HERIC topologies (investigated in chapter 5).

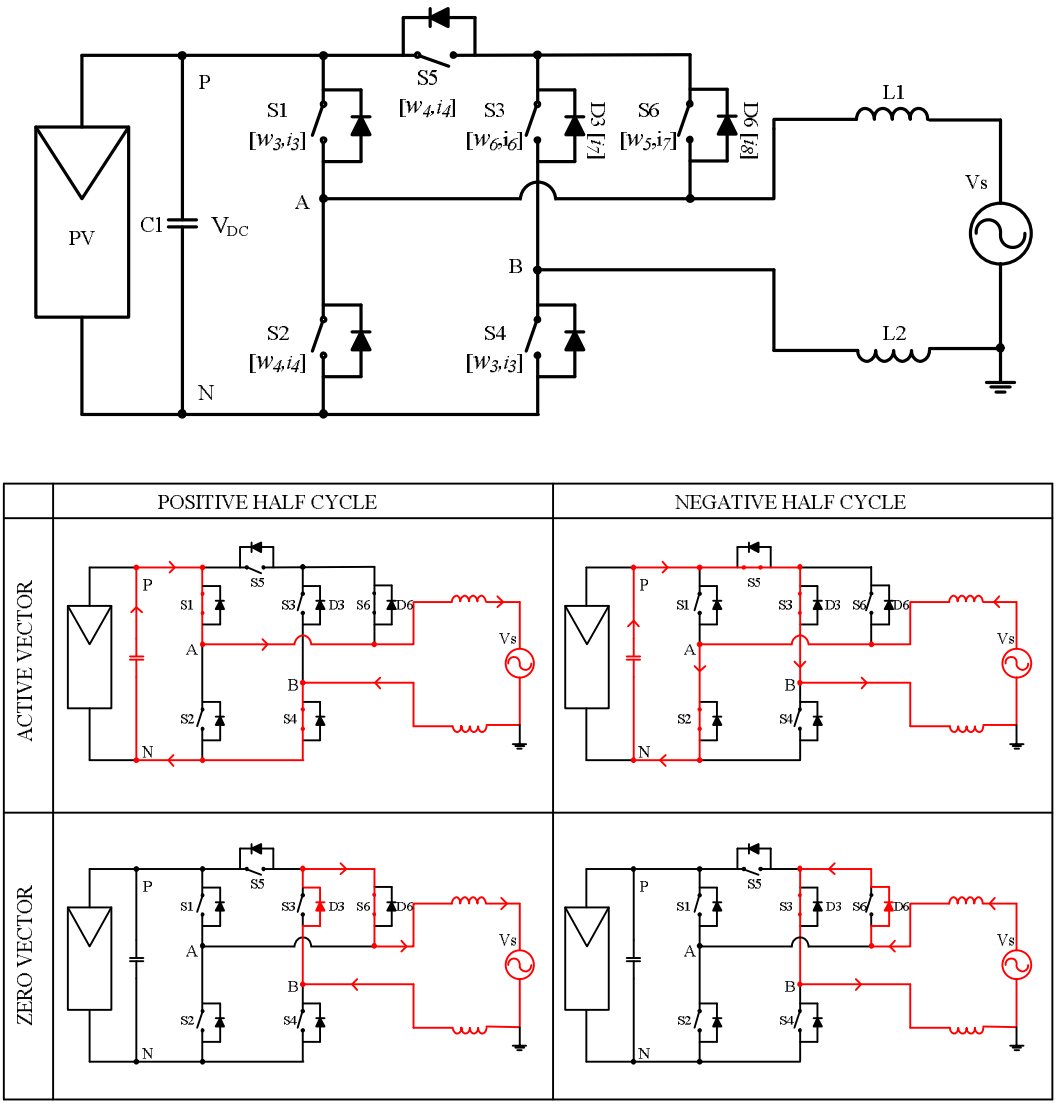


Figure 3.16 The proposed PT-1 topology (top) [28], and its switching states (bottom) regarding the grid voltage, and active and zero vectors.

Having utilized the same strategy at zero vectors (decoupling AC and DC circuits), the leakage current characteristics of ZVI-GCTSI topologies are common. In Figure 3.17, the leakage current of the PT-1 topology is depicted as a representative of the leakage current of the ZVI-GCTSI topologies for a parasitic capacitance of 500 nF. The leakage current

waveform in this figure has line frequency and high frequency content, which is caused by the grid voltage variation and the decoupling mechanism of ZVI-GCTSI topologies rather than the varying CMV. A detailed analytical approach for the leakage current and simulation results are provided in chapter 4.

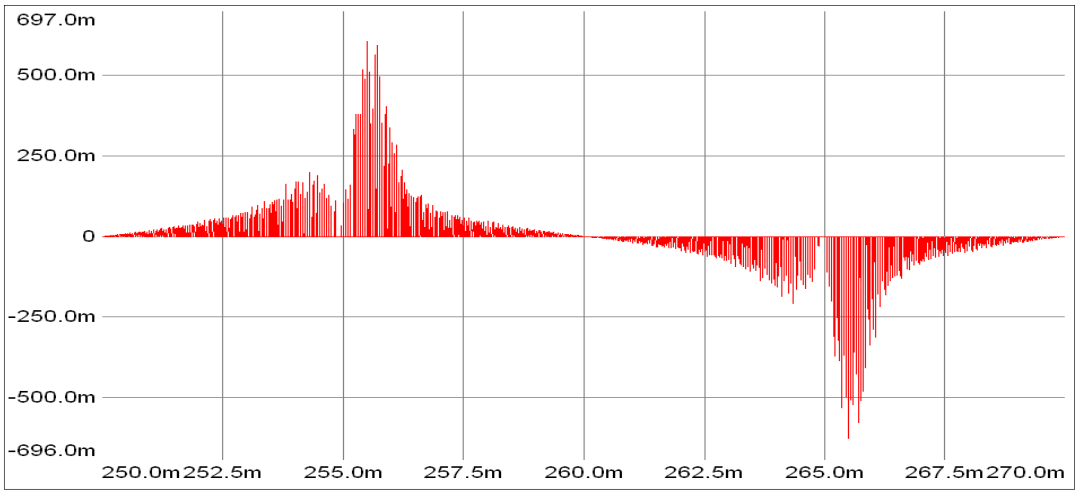


Figure 3.17 The leakage current (A) of the PT-1 topology at 500nF parasitic capacitance as a representative of the leakage current characteristics of ZVI-GCTSI family.

3.2.2.1.2 ZVMC-GCTSI Topologies

The inherent advantages of ZVI-GCTSI topologies such as low DC bus voltage requirement, less filter inductor current ripple due to 3-level output voltage, and no power flow to the DC bus capacitor from the grid (reactive power circulation) advantages are also existent in ZVMC-GCTSI topologies. However, unlike ZVI-GCTSI topologies, ZVMC-GCTSI topologies do not decouple AC and DC circuits at zero vectors. Rather than decoupling at zero vectors, these topologies connect the AC grid side to the midpoint of the DC bus. The connection to the midpoint of the DC bus usually requires additional active switches, or splitting diodes as in the case of the topology illustrated in Figure 3.20 [52]. In the case of active switch utilization in the midpoint of the DC bus connection, the current rating of the switch is less than few amperes, and the current is in the order of mA, contributing negligible losses. Since the midpoint current is low in these topologies, splitting of the DC bus can be achieved by small capacitors, without affecting the total DC bus capacitor size and its rating.

As will be studied in chapter 4, the midpoint connection of ZVMC-GCTSI topologies reduces the leakage current as compared to their ZVI-GCTSI counterparts.

In Figure 3.9 and 3.10, the theoretical gate logic signals and power semiconductor currents are illustrated to be assigned to the concerning semiconductors belonging to the ZV-GCTSI topology family. Being a subgroup of the ZV-GCTSI topology family, the ZVMC-GCTSI topologies are studied by making use of these theoretical gate logic and power semiconductor current waveforms. Apart from the power semiconductor current waveforms, theoretical midpoint-connecting switch waveforms are supplied. In Figure 3.18, these theoretical current waveforms for midpoint-connecting switches are depicted. In the top, theoretical grid voltage and the parasitic current (with the polarity assigned in Figure 2.1) are depicted for a grid cycle for ZVMC-GCTSI topologies. The theoretical currents i_9 and i_{10} are assigned to each midpoint-connecting semiconductor in concerning topology. Although the leakage current waveform in this figure is depicted for ZVMC-GCTSI topologies, the midpoint-connecting semiconductor currents are valid for ZHV-GCTSI topologies' midpoint-connecting switches (since their leakage currents become same as of the ZVMC-GCTSI topologies in certain intervals as illustrated in Figure 3.30 and in chapter 4).

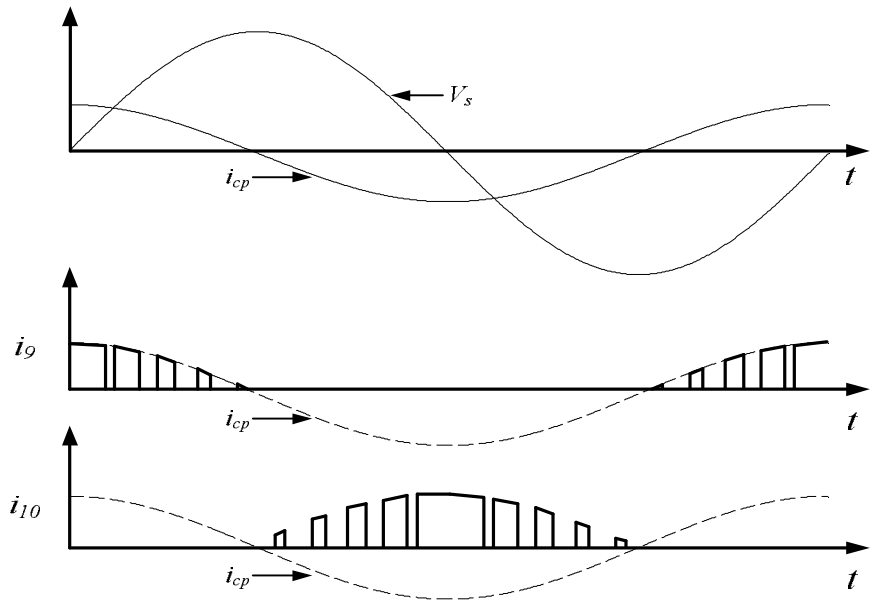


Figure 3.18 Common theoretical current waveforms for the midpoint-connecting semiconductors of ZVMC-GCTSI and ZVH-GCTSI topologies at unity power factor.

The topology proposed by Xiao et al [53] (Figure 3.19, named as iH5) achieves the midpoint connection at zero vectors by the switch S5. The rest of the switches are utilized in a manner to control the line current with the inverter reference voltage and to decouple AC and DC circuits, where the theoretical gate logic signals (Figure 3.9), power semiconductor currents (Figure 3.10), and midpoint-connecting switch currents (Figure 3.18) are assigned to each corresponding controlled switch.

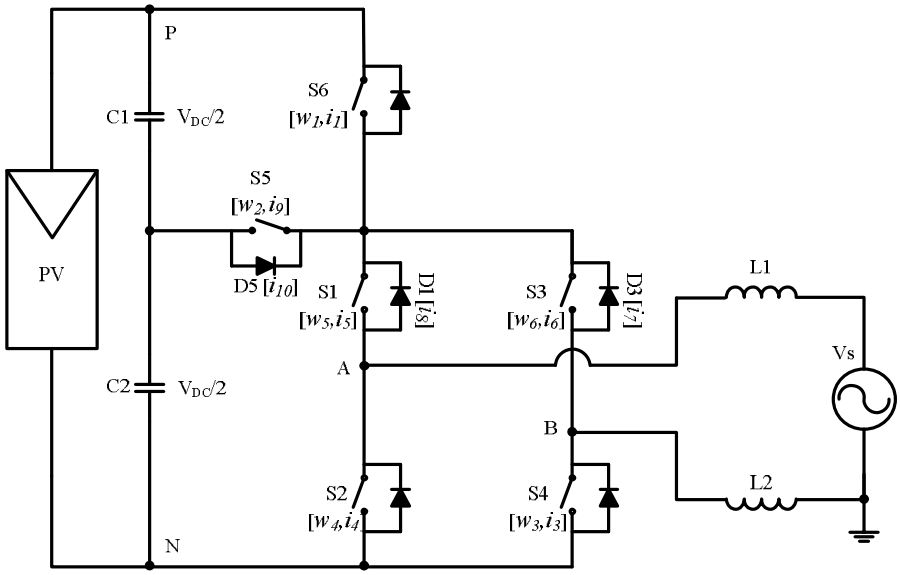


Figure 3.19 The iH5 topology proposed in [53].

Figure 3.20 illustrates another ZVMC-GCTSI topology [52]. This topology connects the AC side to the midpoint of the DC bus during zero vectors by making use of the zero vector freewheeling diodes D7 and D8. S1, S2, S3, and S4 semiconductors operate at line frequency whereas S5 and S6 modulates the line current with high frequency operation with the freewheeling diodes D7 and D8.

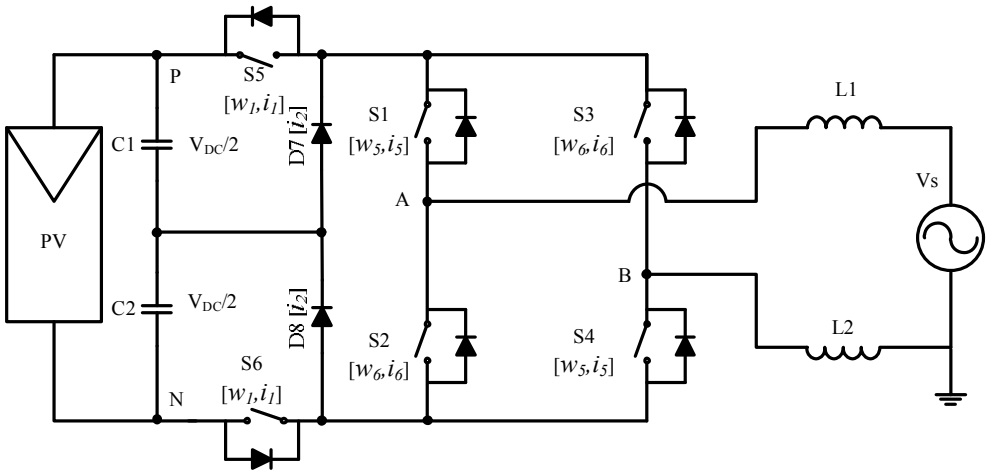


Figure 3.20 The ZVMC-GCTSI topology proposed in [52].

Apart from the iH5 topology and the topology proposed in [52], the approach to connect the AC side to the midpoint of the DC bus could be extended to yield new ZVMC-GCTSI topologies. In Figure 3.21 a proposed ZVMC-GCTSI topology, the PT-2 topology is depicted. The gate logic signals for a given voltage reference (in Figure 3.9) are assigned to nearby the related switches with the theoretical power semiconductor current waveforms (from Figure 3.10) to clarify the operation of the topology at unity power factor. The switches S1, S2, S3, and S4 are used for the modulation of the current by supplying the active voltage vectors, and the decoupling of the AC grid and the DC PV source. Depending on the sign of the line current, the switches S5 and S6 provide freewheeling path with their diodes for the line current at zero vector durations. The switch S7 and its diode D7 connect the AC grid and the midpoint of the DC bus at zero vectors.

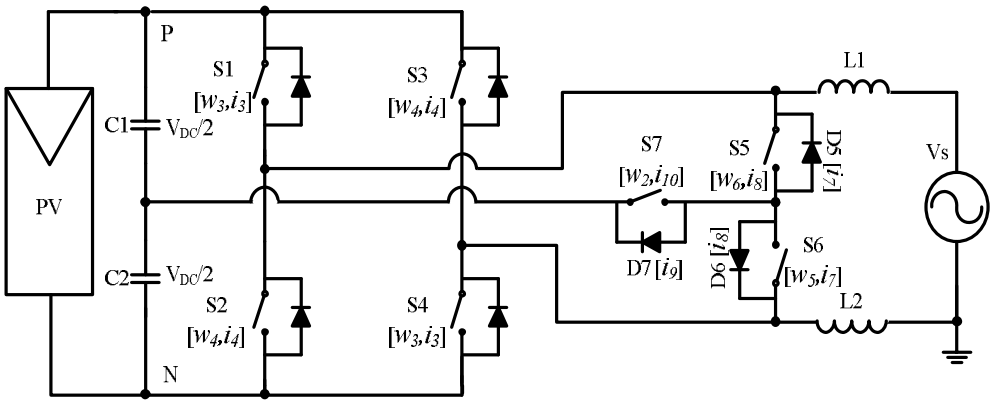


Figure 3.21 The proposed PT-2 topology belonging to the ZVMC-GCTSI topology family.

Another proposed ZVMC-GCTSI topology, the PT-3 topology is depicted in Figure 3.22. The gate signals of active switches of this topology are assigned to corresponding active switch in the figure. In the topology, S1, S4, S5, and S6 provide decoupling of AC and DC circuits, S2, S3, D8 and D9 provide freewheeling, and S7 provides the connection of AC grid to the midpoint of the DC bus.

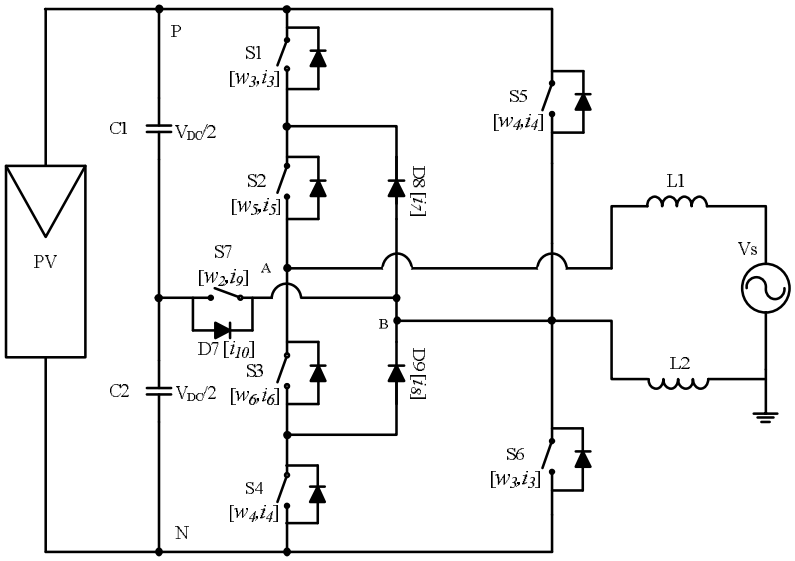


Figure 3.22 The proposed PT-3 topology belonging to the ZVMC-GCTSI topology family.

Figure 3.23 depicts the last proposed topology of this class, PT-4. The operation of the topology is similar to the previous ZVMC-GCTSI topologies. The gate logic signals supplied in Figure 3.9 is used nearby the corresponding switches to modulate the reference voltage at unity power factor with the theoretical power semiconductor currents from Figure 3.10 and the theoretical midpoint-connecting semiconductor currents from Figure 3.18. As these assignments indicate, depending on the sign of the line current, the switches S3 and S6 are used for the zero vector freewheeling of the line current with their anti-parallel diodes. S1, S2, S4 and S5 are used to control the line current by modulating the inverter output voltage. Moreover, these switches decouple the AC and DC circuits at zero vectors. On the other hand, the switch S7 is in the on-state at zero vectors to connect the AC grid to the midpoint of the DC bus.

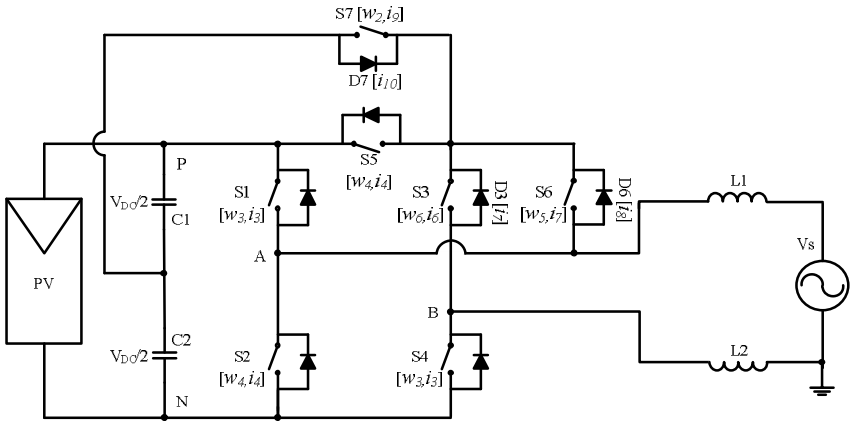


Figure 3.23 The proposed PT-4 topology belonging to the ZVMC-GCTSI topology family.

The leakage current characteristics of ZVMC-GCTSI topologies are similar to each other as their strategies at zero vector durations are same. The low inherent low DC bus voltage requirement of ZVI-GCTSI topologies, their no dead-time requirement, and three-level output voltage advantages are also existent in ZVMC-GCTSI topologies. However, ZVMC-GCTSI topologies require additional semiconductors and split capacitors (with low current rating) as compared to their ZVI-GCTSI counterparts. Nevertheless, with the DC bus midpoint connection at zero vectors, the leakage current characteristics of these topologies (especially the peak values of the leakage current) are greatly improved (the peak values of the leakage currents are reduced). Figure 3.24 illustrates the leakage current of the topology in [52] as a representative of ZVMC-GCTSI family. It is noticeable that the leakage current is quite reduced in ZVMC-GCTSI topologies as compared to their ZVI-GCTSI relatives (597 mA_{peak} to 25 mA_{peak} for 500 nF parasitic capacitance) for the same simulation parameters.

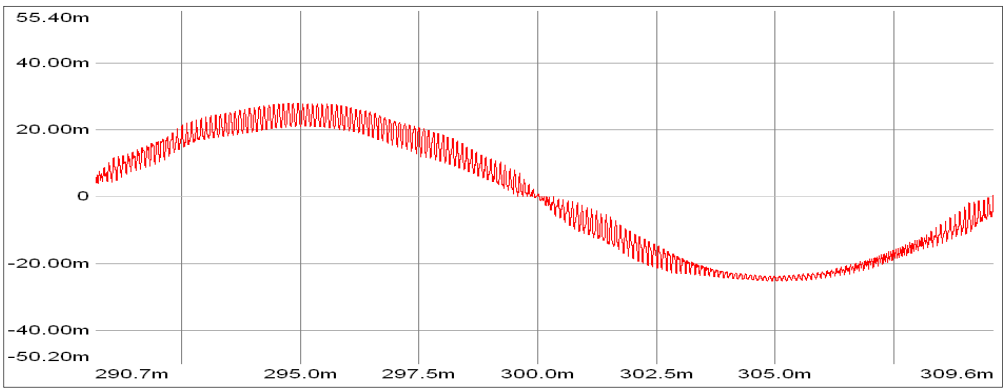


Figure 3.24 The leakage current (A) of the topology in [52] at 500nF parasitic capacitance as a representative of the leakage current characteristics of ZVMC-GCTSI family.

In this section, ZVMC-GCTSI topologies are investigated having reduced leakage current characteristics as compared to ZVI-GVTSI topologies (to be analyzed in chapter 4). The next section describes the ZVH-GCTSI topologies having the hybrid characteristics of ZVI-GCTSI topologies and ZVMC-GCTSI topologies.

3.2.2.1.3 ZVH-GCTSI Topologies

In Zero Vector Hybrid Grid-connected Transformerless Solar Inverter (ZVH-GCTSI) topologies, instead of DC bus midpoint connection at zero vectors as in the case for ZVMC-GCTSI topologies, the connection at zero vectors is realized at only half of the grid period. In the other half period, these topologies show ZVI-GCTSI characteristics by decoupling AC and DC circuits without any DC bus midpoint connection.

One ZVH-GCTSI topology in the literature is proposed in [13], and illustrated in Figure 3.25. The gate logic signals in Figure 3.9 are assigned to the corresponding switches in the topology with the theoretical semiconductor current waveforms in Figure 3.10 and Figure 3.18.

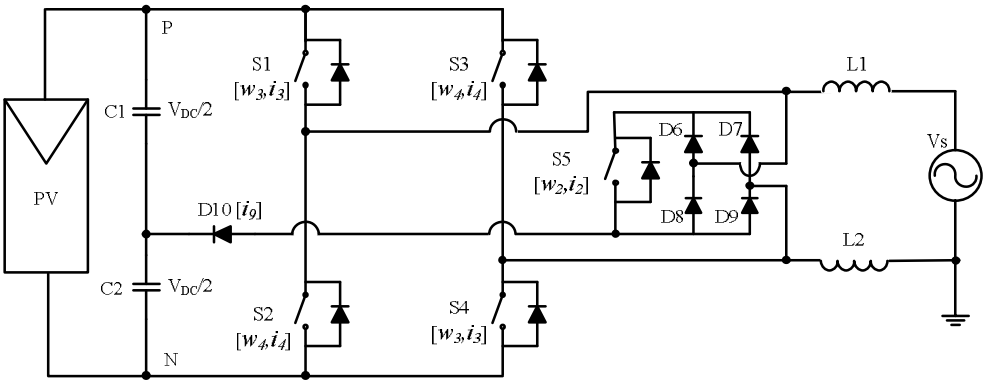


Figure 3.25 The HB-ZVR topology [13].

In Figure 3.26, a proposed topology belonging to ZVH-GCTSI family is depicted. The topology is labelled as PT-5. The gate signals of the topology for unity power factor operation is assigned from the gate logic signals provided in Figure 3.9. The power semiconductor and midpoint-connecting semiconductor theoretical currents are provided in

Figure 3.10 and in Figure 3.18, which are assigned to the concerning semiconductor in the topology (Figure 3.26) to further clarify the operation.

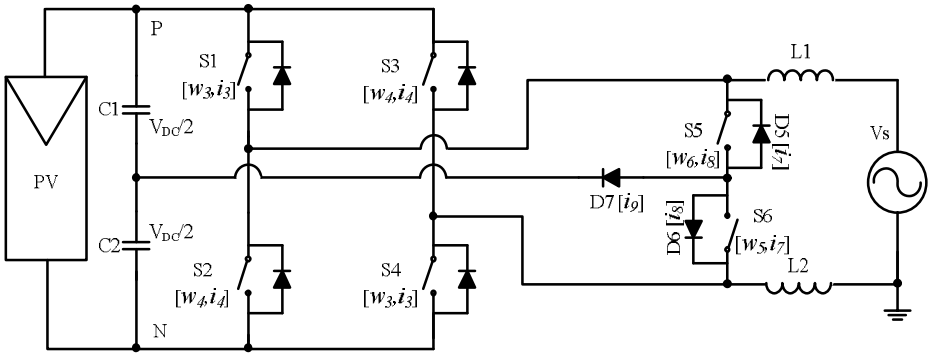


Figure 3.26 The proposed PT-5 topology belonging to the ZVH-GCTSI topology family.

In Figures 3.27-3.29, three proposed ZVH-GCTSI topologies (PT-6, PT-7, and PT-8) are depicted respectively. The gate signals from Figure 3.9 are assigned to corresponding controlled switches of the corresponding ZVH-GCTSI topologies as illustrated in these figures. Moreover, similar to the case in the PT-5 topology, theoretical current waveforms are assigned to the semiconductors from Figure 3.10 and 3.18.

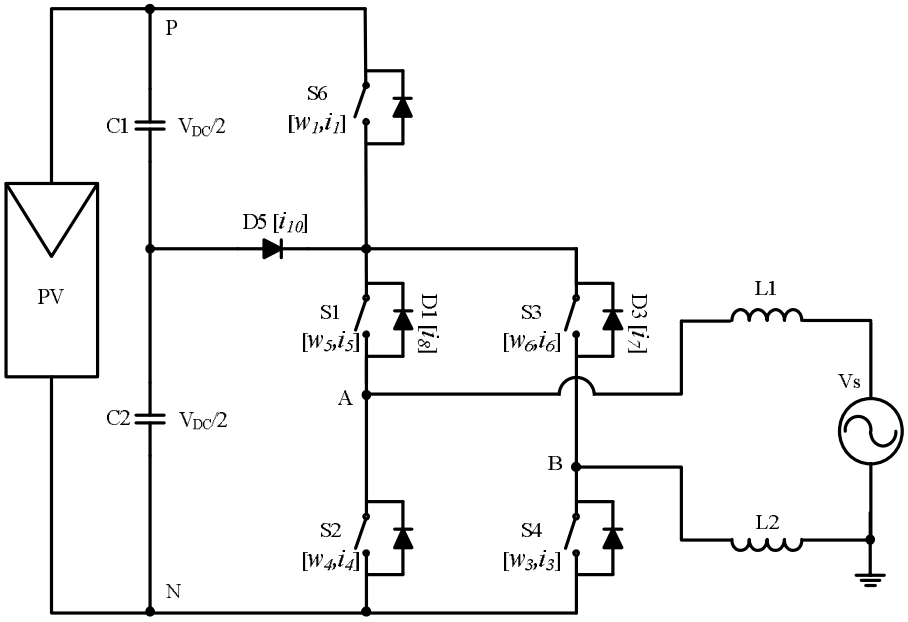


Figure 3.27 The proposed PT-6 topology belonging to the ZVH-GCTSI topology family.

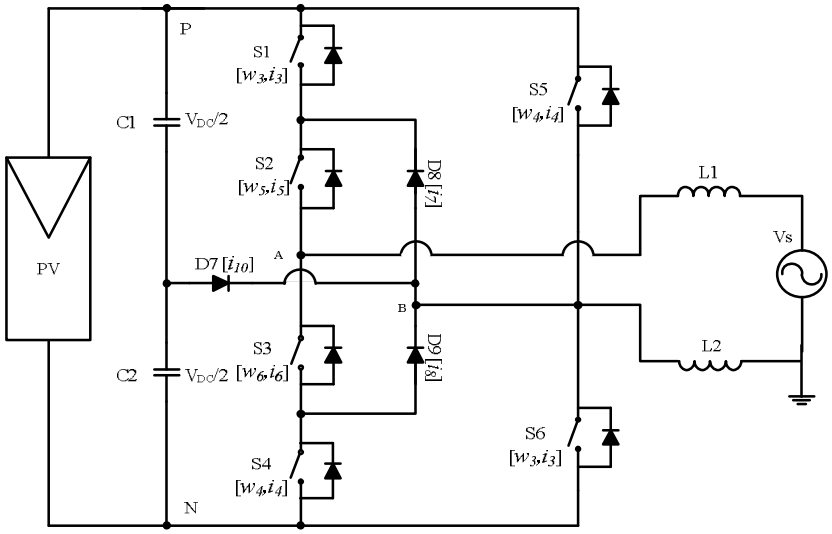


Figure 3.28 The proposed PT-7 topology belonging to the ZVH-GCTSI topology family.

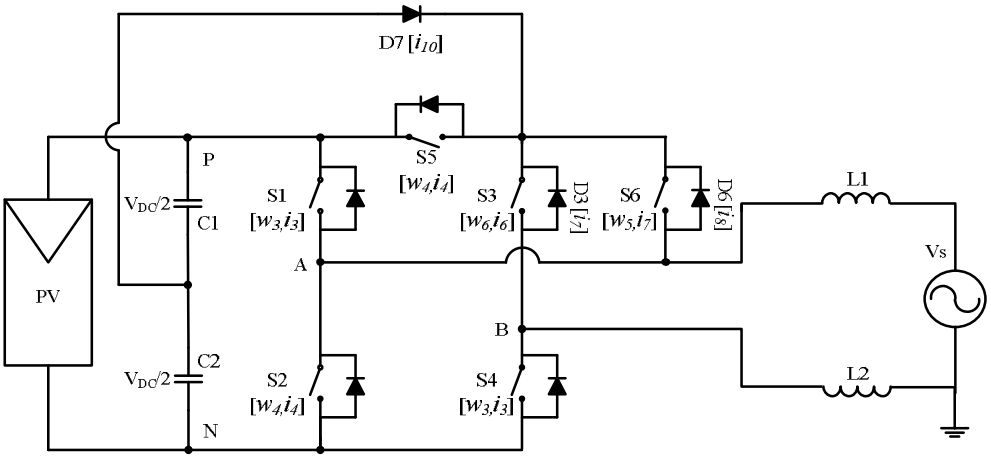


Figure 3.29 The proposed PT-8 topology belonging to the ZVH-GCTSI topology family.

In this section, ZVH-GCTSI topologies are presented, where they generally differ from ZVMC-GCTSI topologies by replacing the midpoint-connecting controlled switch with a diode. As a result of this replacement, the leakage current characteristics of these topologies take the form of the leakage current characteristics of ZVI-GCTSI and ZVMC-GCTSI topologies interchangeably in time (shown in Figure 3.30 and studied in chapter 4). As compared to ZVI-GCTSI topologies, ZVH-GCTSI topologies have reduced RMS leakage current attributes, whereas the peak value of the leakage current remains the same. As compared to ZVMC-GCTSI topologies, ZVH-GCTSI topologies have less controlled

devices sacrificing the superiority of the RMS and the peak value of the leakage current. Therefore, ZVH-GCTSI topologies lie in between ZVI-GCTSI and ZVMC-GCTSI topologies.

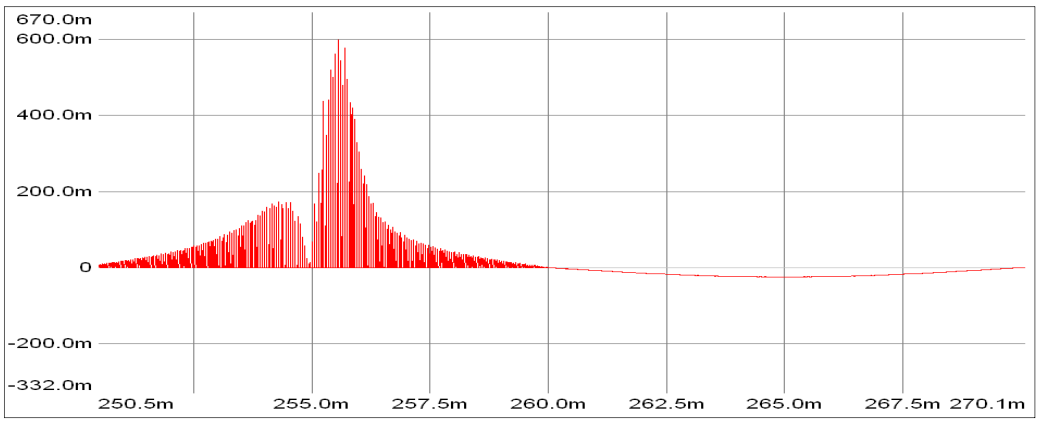


Figure 3.30 The leakage current (A) of PT-5 at 500nF parasitic capacitance as a representative of the leakage current characteristics of ZVH-GCTSI family.

Besides having the efficiency and low DC bus voltage requirement benefits of unipolar modulation of the H4 topology, ZV-GCTSI topologies offer reduced leakage current characteristics as compared to H4 unipolar modulation. Having investigated the ZV-GCTSI topologies, the next section studies the SC-GCTSIs.

3.2.2.2 SC-GCTSI Topologies

The second class of GCTSI topologies, SC-GCTSIs, realize a solid connection between the AC (grid side), and the DC (DC bus side) circuits. In this class of GCTSI topologies, the intention is to keep the equivalent parasitic capacitor voltage as constant as possible. Depending on the parasitic capacitance value, because of no variation or slow variation on the capacitor voltage, the parasitic capacitor current becomes as low as to cause no considerable hazardous leakage current.

The Neutral Point Clamped (NPC) topology and NPC derived topologies with midpoint clamping to the neutral of the utility grid belong to this subgroup of GCTSI topologies. Figure 3.31 depicts the classical NPC topology with reduced semiconductor stresses as compared to classical single-phase half bridge. Another NPC derived topology is depicted in Figure 3.32 [18], [44]. Increasing the complexity of the circuitry, these topologies can also

be expanded as converters having higher number of levels to decrease voltage and current harmonic distortions, decrease the switching frequency, and decrease semiconductor ratings, which are out of the scope of the thesis.

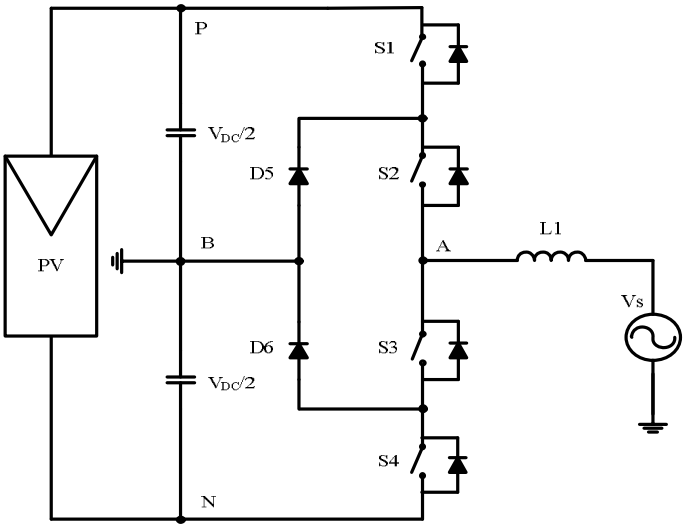


Figure 3.31 The Classical Single-Phase NPC topology.

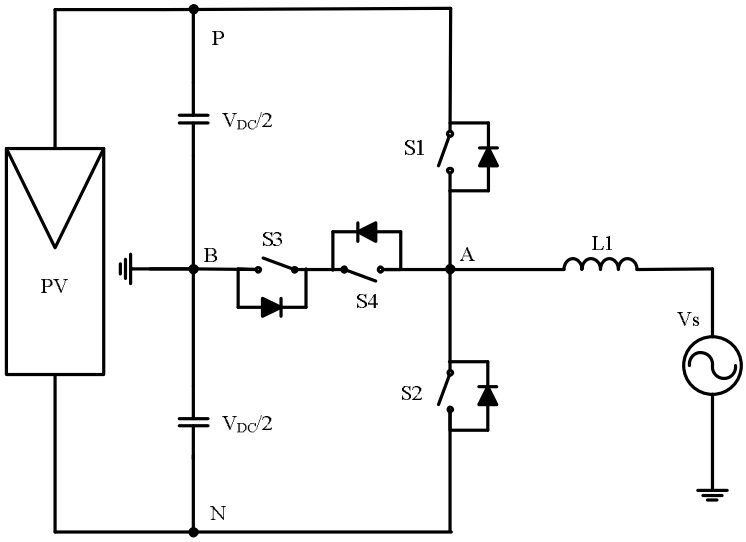


Figure 3.32 SC-GCTSI topology in [18], [44].

Another SC-GCTSI topology is proposed in [54] (shown in Figure 3.35). This topology has the advantage of five level output voltage, which reduces the filter inductor losses and the size. Similar topologies are proposed in the thesis as shown in Figure 3.36 (PT-9) and Figure 3.37 (PT-10). The operation of these topologies in Figures 3.35, 3.36, and 3.37 can be

understood by making use of the gate logic signal waveforms for unity power factor operation in Figure 3.33 and the theoretical power semiconductor current waveforms in Figure 3.34. The theoretical gate logic signals and power semiconductor currents are assigned nearby to the corresponding active switches in these topologies to clarify the operation. In Figure 3.33, the voltage $V_{DC\text{-}f}$ represents the feed-forward voltage from the PV source (i.e. the voltage that is not boosted and utilized to modulate the line current when the grid voltage is smaller). The feed-forward voltage is also assigned in the concerning figures (Figures 3.35-3.37). When the grid voltage is smaller in magnitude than the feed-forward voltage from the PV source (i.e. the voltage of the PV modules connected either in the form of string or array) the line current is modulated by the lower DC bus voltage ($V_{DC\text{-}f}$) without passing the power from any boost stage. When the grid voltage in magnitude exceeds the feed-forward voltage, the line current is modulated by making use of higher DC bus voltage (V_{DC}), which is regulated by the boost converters shown in the figures.

In these three topologies, (topologies in Figures 3.35, 3.36, and 3.37), the DC-DC converters are boost converters (generally being classical boost converters) to raise the DC bus voltage to inject undistorted current waveform (i.e. preserving the inverter linearity) to the utility grid. The advantage of these topologies is to perform injection of the PV source power to the utility grid with partial boosting rather than completely boosting, and their five-level output voltage characteristics.

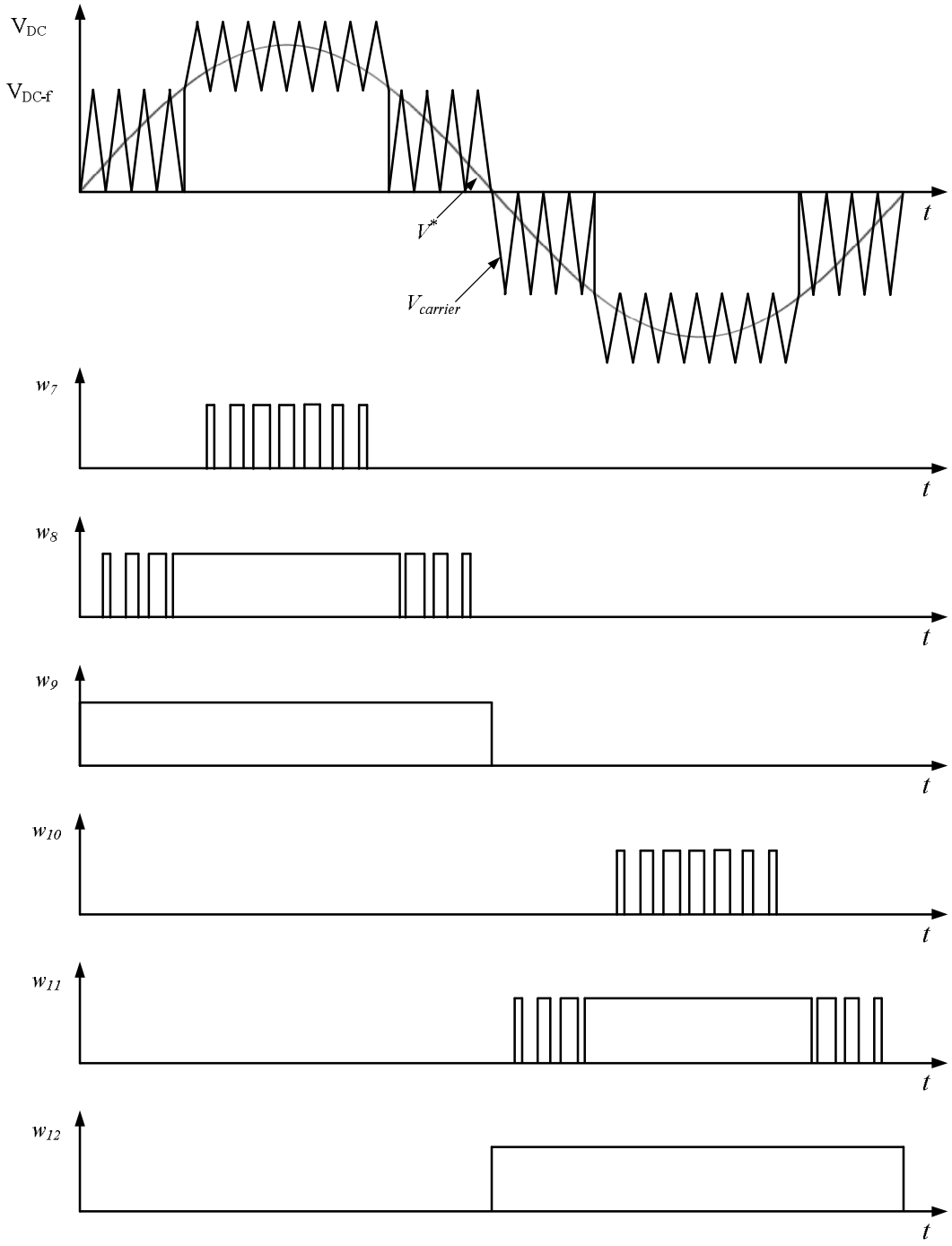


Figure 3.33 Common theoretical waveforms for the gate signals of active switches of the topology proposed in [54], PT-9, and PT-10 at unity power factor.

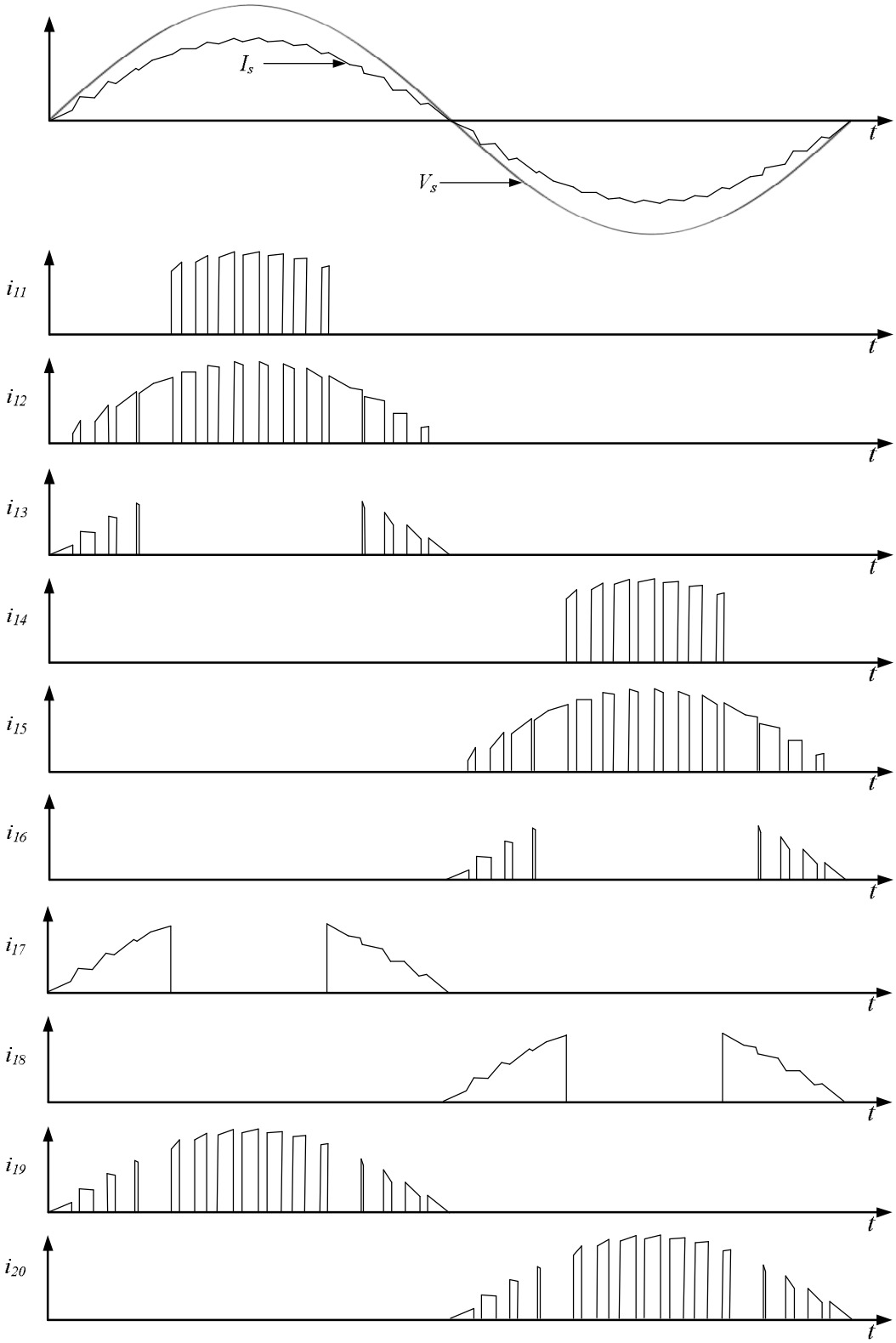


Figure 3.34 Common theoretical current waveforms for power semiconductors of the topology proposed in [54], PT-9, and PT-10 at unity power factor.

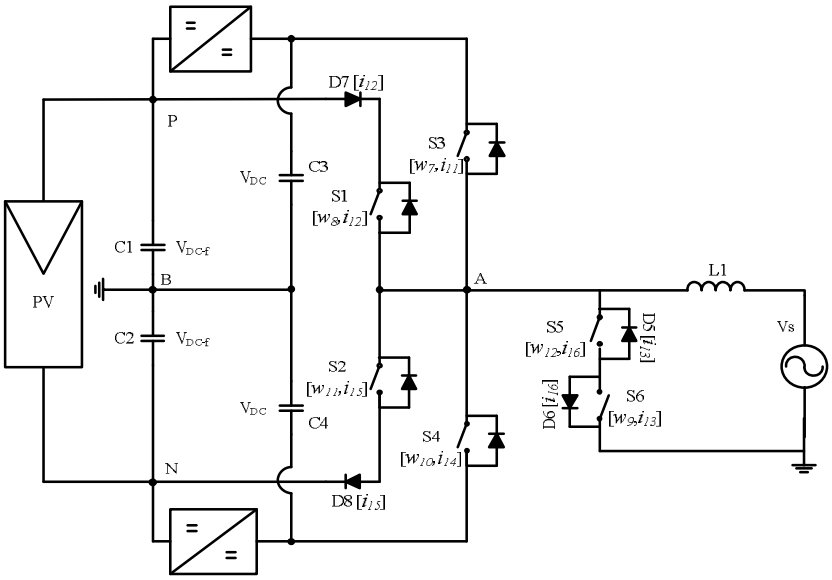


Figure 3.35 SC-GCTSI topology in [54].

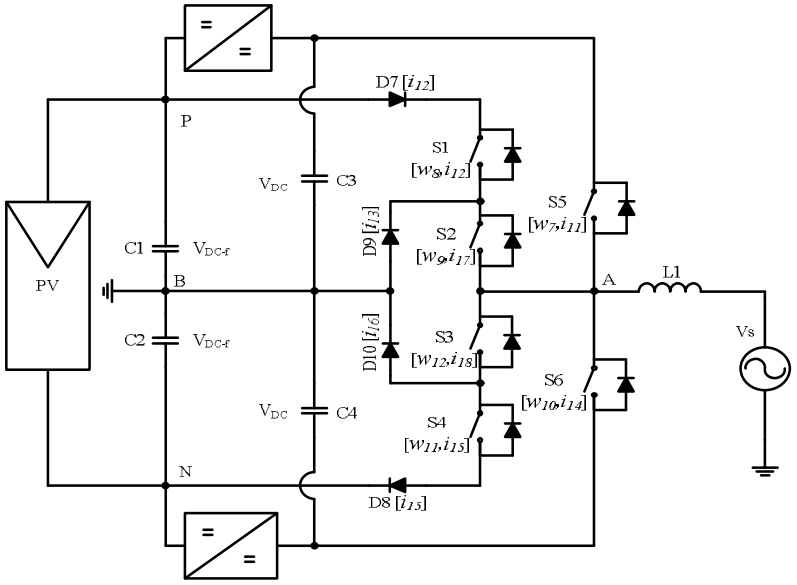


Figure 3.36 The proposed PT-9 topology belonging to the SC-GCTSI topology family.

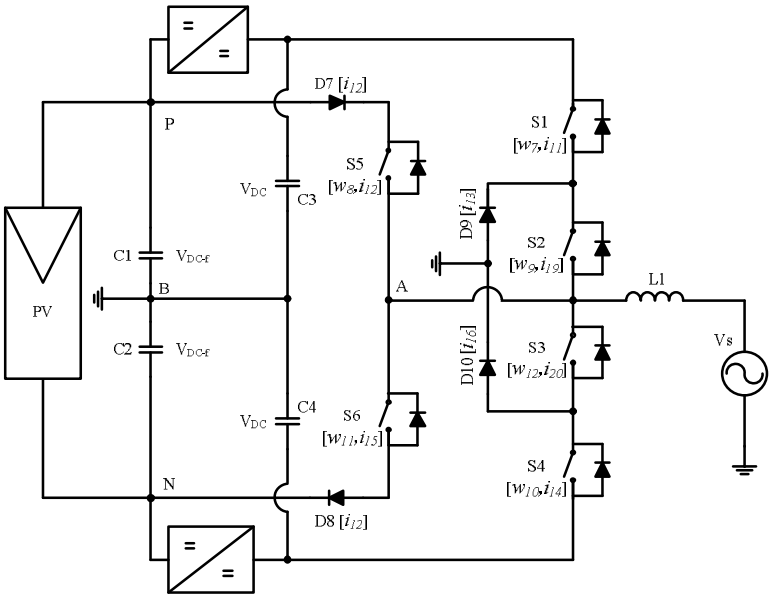


Figure 3.37 The proposed PT-10 topology belonging to the SC-GCTSI topology family.

In Figure 3.38 and Figure 3.39, flying capacitor [55] and flying inductor [56] topologies are depicted. The flying capacitor topology operates as a Voltage Source Inverter (VSI) having four levels, whereas the flying inductor topology has buck, boost, and buck-boost modes to be utilized as the grid voltage changes.

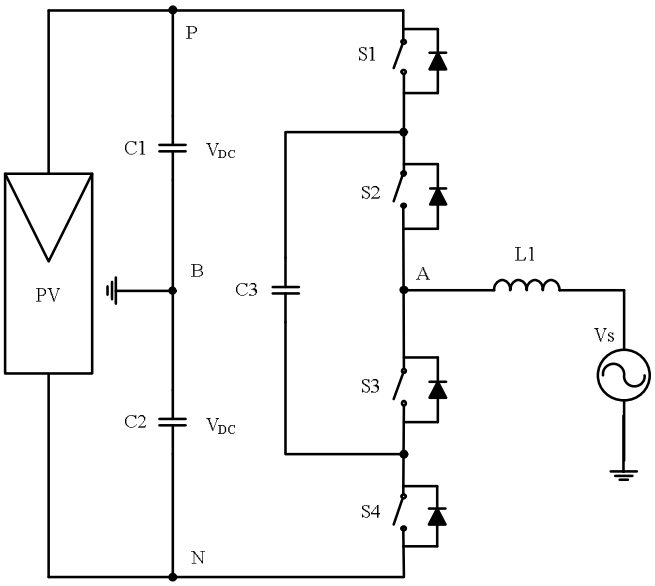


Figure 3.38 The flying capacitor topology in [55].

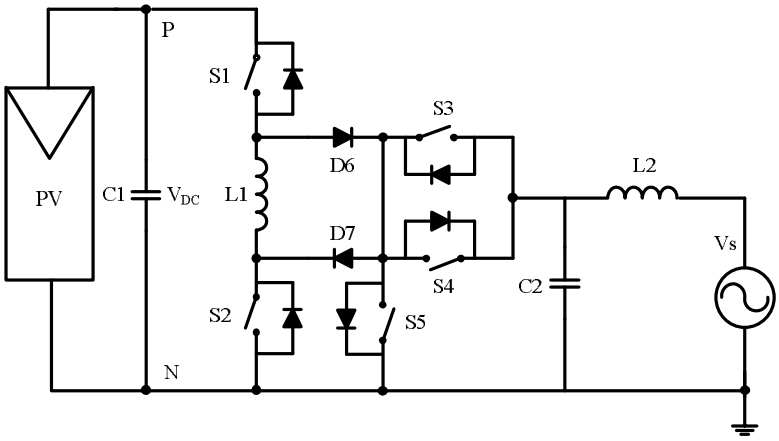


Figure 3.39 The flying inductor topology in [56].

Another SC-GCTSI topology is depicted in Figure 3.40 [57]. This topology operates as a buck-boost type converter. According to the sign of the grid voltage, either the upper buck-boost or the lower buck-boost stage injects the current to the utility grid.

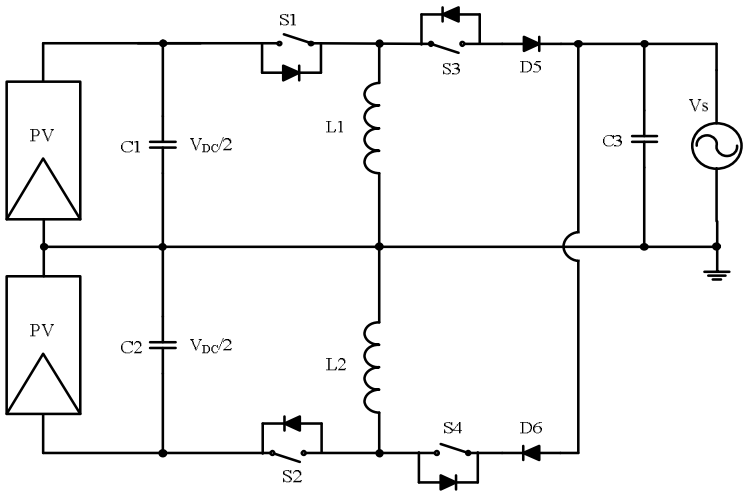


Figure 3.40 Buck-Boost Type SC-GCTSI topology in [57].

In [17], a VSI belonging to SC-GCTSI family is proposed having DC bus clamping capability at low frequency (Figure 3.41). Depending on the sign of the grid voltage, S3 or S4 clamps either the phase or the neutral conductor of the grid to the DC bus positive terminal.

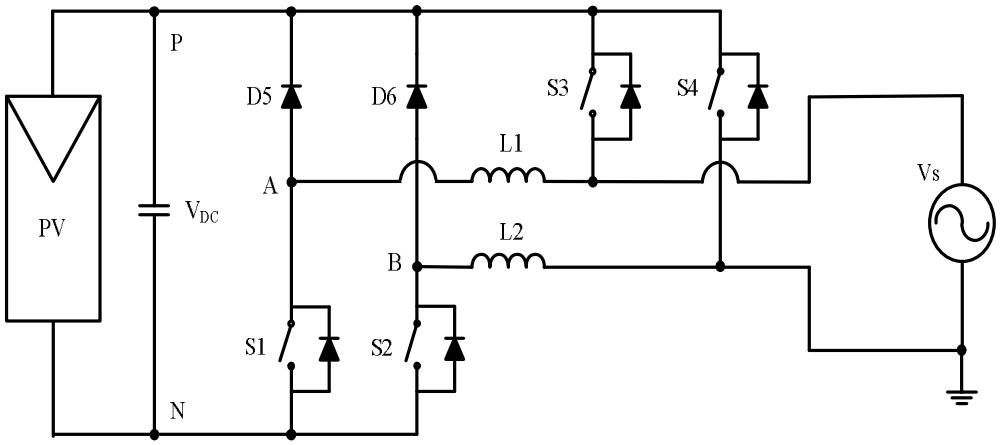


Figure 3.41 SC-GCTSI topology in [17].

Although the SC-GCTSI topologies are abundant, their leakage current characteristics are similar to each other, since the strategy in these inverters is to keep the parasitic capacitance voltage constant by solidly clamping the neutral or the phase conductor to the DC circuit. In these topologies, the leakage current characteristics are grid parameter dependent (studied in chapter4), which becomes an issue in the design stage and the application stage. In Figure 3.42, the leakage current of the PT-9 topology is depicted at 3 kW as a representative of SC-GCTSI topologies for a parasitic capacitance of 500 nF and a grid impedance of 50μH+10mΩ.

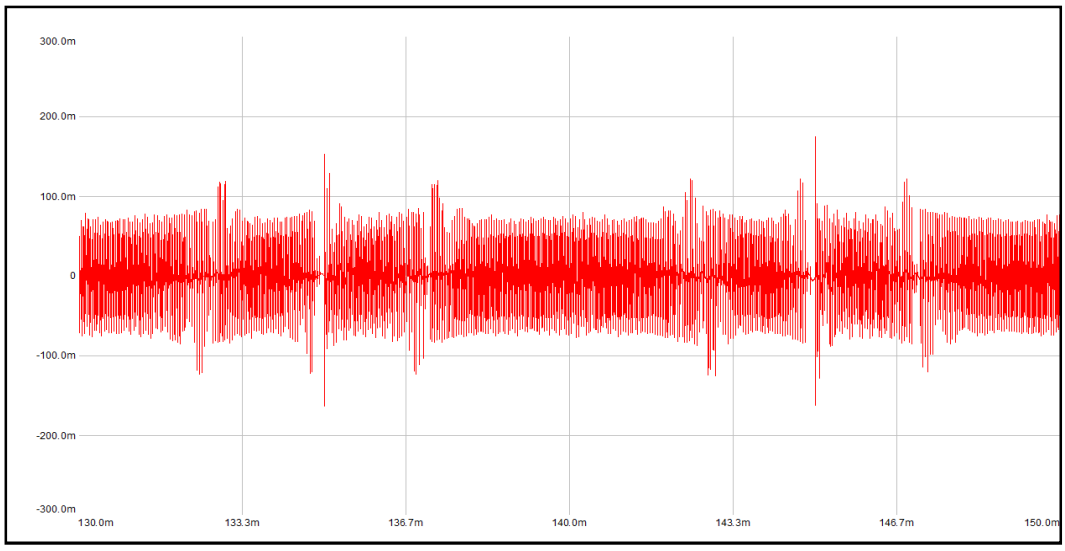


Figure 3.42 Leakage current (A) of PT-9 as a representative of the SC-GCTSI family.

3.2.2.3 Other GCTSIs

Apart from ZV-GCTSI and SC-GCTSI topologies, there exist several GCTSI topologies in the literature. These topologies have either constant CMV, have low CMV variation to introduce negligible leakage current, or use large common mode filters to suppress the leakage current. One of these topologies is the conventional full bridge topology (Figure 3.43) with bipolar switching pattern. The unwanted varying CMV variation of full bridge with unipolar modulation is nonexistent inherently in the bipolar switching pattern. As a result, the leakage current due to CMV variation in this switching pattern is low. However, this kind of operation introduces a larger filter inductor, additional filter losses, and increased internal reactive power circulation to the circuit [17].

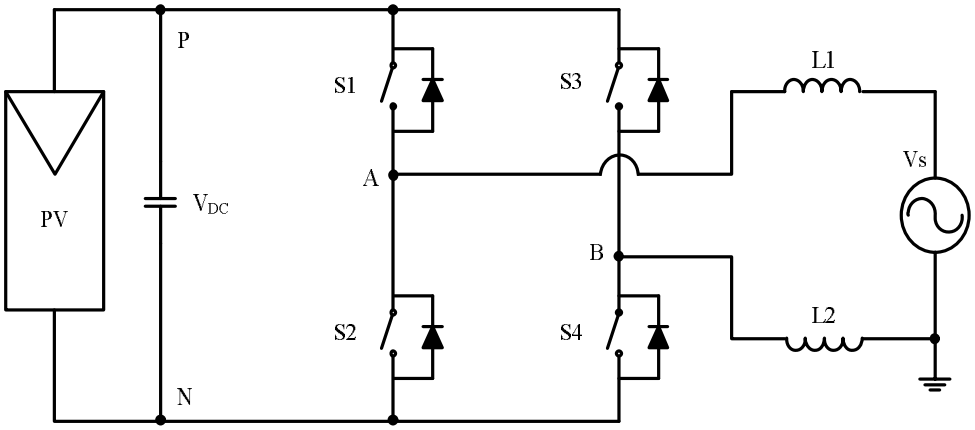


Figure 3.43 The H4 (full-bridge) topology.

Another topology is multilevel inverter based topology in [55] (Figure 3.44). The advantage of this topology to achieve MPPT in module level (distributed MPPT). Therefore, module-mismatching losses are minimized. Moreover, switching losses, the harmonic content of the output current and *dv/dt* value (for EMC considerations) of this converter is low advantageously. The drawbacks are high number of components (high cost) and complexity of the circuit.

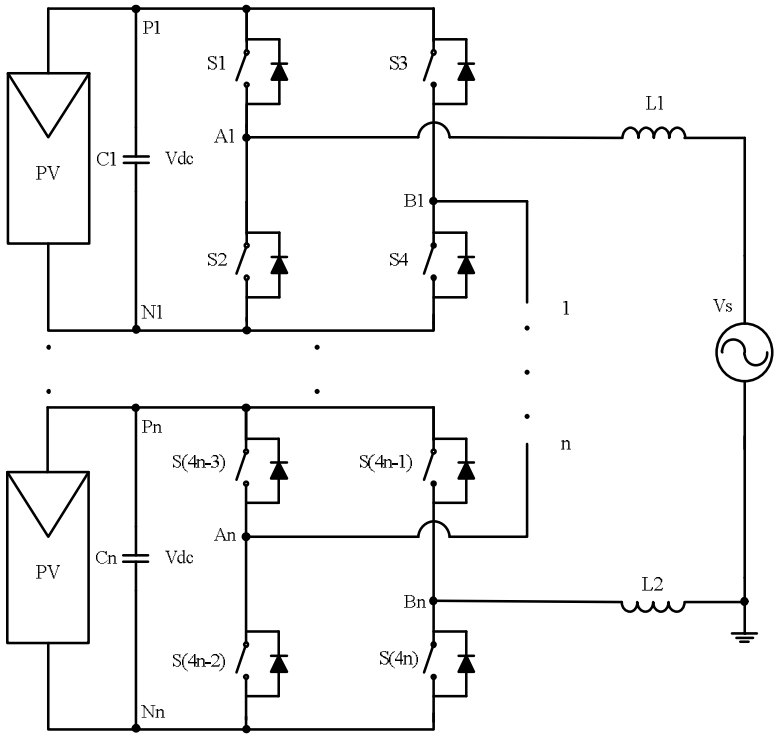


Figure 3.44 Multilevel GCTSI topology in [55].

In [4], Z-source inverter based topology is proposed (shown in Figure 3.45). The topology has inherent buck-boost capability therefore no need for extra boost stage. The inverter has also reduced leakage current due to the utilization of only odd or even space vector set, in spite of the high filter current ripple due to remote state vectors.

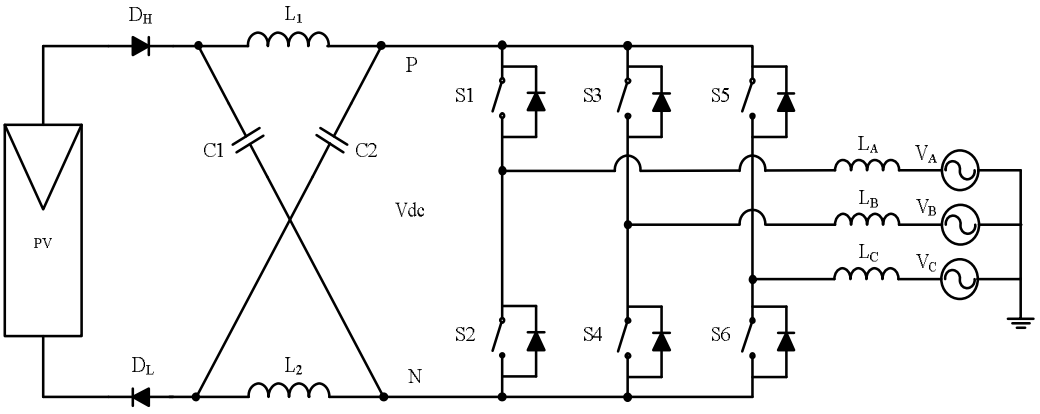


Figure 3.45 Z-source based GCTSI topology in [4].

3.3 Summary

In this chapter, the classification of PV-PEC topologies with respect to leakage current characteristics is performed with the focus on GCTSI topologies. In the classification, the GCTSI topologies are subdivided into two main classes, which are ZV-GCTSI topologies and SC-GCTSI topologies. ZV-GCTSI topologies are also subdivided into three subclasses (ZVI-GCTSI, ZVMC-GCTSI, and ZVH-GCTSI topologies) according to the strategy used in the zero output voltage durations of the converters. Besides the classification, a survey of PV-PECs is conducted with the focus on GCTSI topologies based on the classification. In the survey, existing PV-PEC topologies are studied. In addition to the existing topologies, novel topologies are proposed in this chapter, expanding the GCTSI families. The switching schemes of the proposed topologies are provided through gate logic signals for unity power factor operation to clarify the switching patterns of the topologies.

In conclusion, the contribution of this chapter is the classification of PV-PECs and proposal of new GCTSI topologies. Having classified and investigated the existing PV-PEC topologies, and having proposed new GCTSI topologies, next chapter is devoted to the analytical investigation of the filter inductor current ripple analyses of the voltage sourced GCTSI topologies and the leakage current mechanisms of GCTSI topologies. Simulation based verification of these studies are also provided in the chapter. Moreover, a comparative study of GCTSI topologies is conducted based on the leakage current characteristics and the filter inductor current ripple of the topologies.

CHAPTER 4

FILTER INDUCTOR CURRENT RIPPLE AND LEAKAGE CURRENT ANALYSES OF ZV-GCTSI AND SC-GCTSI TOPOLOGIES, AND THEIR PERFORMANCE EVALUATION VIA SIMULATIONS

4.1 Introduction

In chapter 2, several restrictions by grid codes, and several requirements on the interconnection of PV-PECs to the utility grid were reviewed concerning power quality, safety, reliability, and efficiency. Among these restrictions and requirements, the low leakage current restriction differentiates PV-PECs from other conventional inverters especially in transformerless applications. In chapter 3, a survey, classification, and extension of PV-PEC topologies were conducted with the major focus on the GCTSI topologies due to their higher efficiency and lower cost as compared to their transformer based counterparts. Moreover, GCTSI topologies were divided into subgroups as ZV-GCTSI and SC-GCTSI topologies, according to their leakage current characteristics.

Beyond the low leakage current characteristics, GCTSIs are required exhibit high efficiency. ZV-GCTSI and SC-GCTSI topologies investigated in chapter 3 were mostly Voltage Source Inverters (VSI), where their inductor current ripples becomes an issue for the efficiency and the filter inductor sizing considerations. The inductor current ripples of these topologies are a function of the number of levels of their output voltages.

In this chapter, the output voltage characteristics of GCTSI topologies are investigated to identify the effect of the number of output voltage levels on the filter inductor current ripple, which has a tight relation on the filter inductor sizing, and on the semiconductor and inductor losses. Furthermore, the leakage current mechanisms of the subgroups of GCTSI topologies are studied, and analytical approaches are established to identify the operation of the

topologies under investigation. Simulation results are provided to verify analytical approaches.

The system model for the simulated topologies is introduced in the next section (section 4.2) and then, the inductor current ripple analysis for GCTSIs follows. After that, the leakage current mechanisms of ZVI-GCTSI, ZVMC-GCTSI, ZVH-GCTSI, and SC-GCTSI topologies are studied by making use of analytical approaches and simulation results.

4.2 Simulated System Model

The model for the simulation of GCTSI topologies is illustrated in Figure 4.1. In the simulations, the GCTSI topology block in this figure is replaced by the topology under interest, and the DC bus voltage is fixed to 400 V for ZV-GCTSI topologies, 800 V for simulated SC-GCTSI topologies, where the midpoint of the DC bus of the simulated SC-GCTSI topologies are grounded. The line to neutral utility grid voltage is taken to be 220 V. Total filter inductor (L_F) for ZV-GCTSI topologies is split into two, whereas it is inserted in only the phase conductor in the case of simulated SC-GCTSI topologies. The value of the total filter inductor L_F is kept constant at 2 mH throughout the simulations. The distributed parasitic capacitance of the PV modules is represented by only a single lumped capacitor (C_p) as connected between the negative rail of the PV modules and the ground. The effective switching frequency (f_s) is chosen to be 20 kHz for all of the simulated topologies. These simulation parameters are listed in Table 4.1.

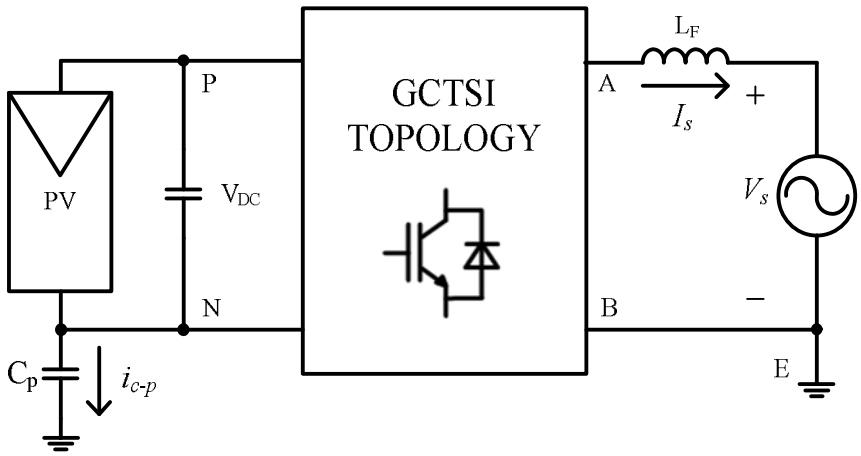


Figure 4.1 The model for the simulation of GCTSI topologies.

Table 4.1 Simulation Parameters

P_{rated} :	*Rated Power*	*3 kW*
V_s :	*Grid Voltage*	*220 V_{rms}, 50 Hz*
V_{DC} :	*DC Bus Voltage*	*400 V*
f_s :	*Effective Switching Frequency*	*20 kHz*
L_F :	*Total Filter Inductance*	*2 mH*
C_p :	*Parasitic Capacitance*	*500 nF*

The control of the simulated topologies is realized with the basic current control scheme depicted in Figure 4.2. The αβ to dq, and dq to αβ transformations can be carried out by making use of Park transform equations as described in (4.1) and (4.2).

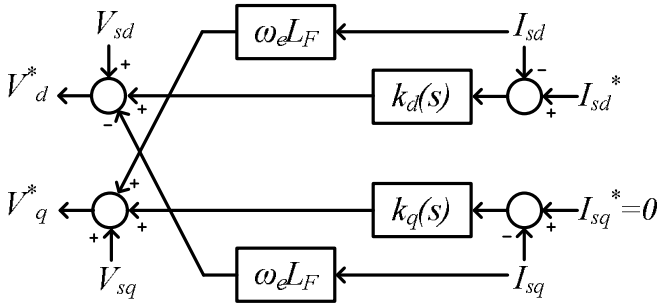


Figure 4.2 Illustration of basic current control scheme used in the simulations of GCTSI topologies.

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \cos(\theta_e) & \sin(\theta_e) \\ -\sin(\theta_e) & \cos(\theta_e) \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{4.1}$$

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} \cos(\theta_e) & -\sin(\theta_e) \\ \sin(\theta_e) & \cos(\theta_e) \end{bmatrix} \begin{bmatrix} x_d \\ x_q \end{bmatrix} \tag{4.2}$$

where θ_e is the synchronous frame reference phase angle. For single-phase systems, (4.3) is used to evaluate (4.1) with orthogonal variables.

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} x(\theta) \\ x(\theta - \pi/2) \end{bmatrix} \tag{4.3}$$

The α component of the voltage obtained from the inverse Park transform of V^*_d and V^*_q is used as the reference voltage (V^*) to feed the carrier signal to obtain switching logic signals.

The procedure of obtaining PWM gate logic signals from V^* for each topology is illustrated in chapter 3, by making use of the gate logic signals obtained in Figure 3.9 and Figure 3.31 for three and five-level GCTSI topologies respectively.

4.3 Filter Inductor Current Ripple of GCTSI Topologies

Mostly being VSIs, GCTSI topologies have a considerable amount of energy dissipated on filter inductors, as well as on the semiconductors. As the filter inductor size and the filter inductor losses are dependent on the inductor current ripple, this section is devoted to the evaluation of filter inductor current ripples of the GCTSI topologies.

The filter inductor current ripple of a VSI under PWM operation is a function of filter inductance, switching frequency, DC bus voltage, and the number of the level of the output voltage (or differential mode voltage, formulated in 4.4). Filter inductance, switching frequency, and DC bus voltage are design dependent, whereas the number of the level of the output voltage is topology dependent. Voltage sourced GCTSI topologies investigated in chapter 3 are listed in Table 4.1 according to the number of levels of the output voltages.

$$V_{dm} \triangleq V_{AN} - V_{BN} \tag{4.4}$$

Table 4.2 GCTSI topologies in terms of their output voltage levels.

	2-level	***3-level***	***5-level***
Topologies	*H4-Bipolar* *Half Bridge*	*ZV-GCTSI topologies* *H4-Unipolar* *NPC derived topologies in* [44] *Topology in* [17]	*Topology in* [54] *PT-9* *PT-10*

4.3.1 Filter Inductor Current Ripple Analyses of GCTSI Topologies

A representative circuit for the evaluation of current ripple of GCTSI topologies is illustrated in Figure 4.3. In the figure, V_{dm} represents the output voltage (or the differential mode voltage) of the GCTSI topology under investigation, V_s represents the grid voltage, and I_s represents the grid current (or filter inductor current). The filter inductor L_F in the figure represents total of the inductors on the line current path, whether it is distributed equally to the phase and neutral conductor, or only located to the phase conductor, depending on the GCTSI topology used. Although V_s is stiff and ideally sinusoidal in time, V_{dm} and I_s have fundamental and ripple components as in (4.5) and (4.6).

$$I_s = I_{s-1} + I_{s-r} \tag{4.5}$$

$$V_{dm} = V_{dm-1} + V_{dm-r} \tag{4.6}$$

where I_{s-1} and V_{dm-1} are the fundamental components, I_{s-r} and V_{dm-r} are the ripple components of the grid current and the inverter output voltage respectively.

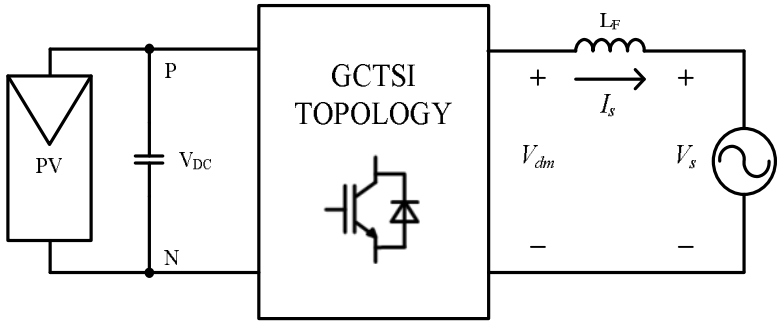


Figure 4.3 Illustration of the representative circuit for the current ripple evaluation.

When the switching frequency becomes sufficiently high, V_s can be assumed as constant for a switching cycle (T_s), and the approach in [58] can be utilized and extended for the evaluation of filter inductor current ripple (I_{s-r}) of two, three, and five-level inverters investigated in chapter 3. The modulation index (M, defined in 4.7) has a significant impact on I_{s-r}, as it determines the ratio of the peak of the grid voltage (V_{s-p}) to the DC bus voltage (V_{DC}).

$$M \triangleq \frac{V_{s-p}}{V_{DC}} \tag{4.7}$$

Moreover, the approach of approximating the grid voltage (V_s) as the switching period averaged of the inverter output voltage (V_{dm}) considerably facilitates the analysis, while preserving the accuracy [57]. This approach is formulated in (4.8).

$$V_s(\theta) = V_{s-p}\sin(\theta) \approx V_{DC} M \sin(\theta) \tag{4.8}$$

While the grid voltage is nearly constant for a switching period, the peak to peak ripple component of the filter inductor current ($I_{s\text{-}r}$) can be obtained for two-level inverters (for example the full bridge topology with bipolar switching pattern) by making use of (4.9), which is applicable to VSIs, as they exhibit buck converter characteristics.

$$I_{s-r}(\theta) = d_v(\theta) \cdot T_s \cdot (V_{DC} - V_s(\theta)) / L_F \ , \ 0 < \theta < \pi \tag{4.9}$$

where $d_v(\theta)$ is the output voltage duty cycle function, which is modulation strategy and topology dependent. In two-level modulation, the output voltage oscillates between V_{DC} and $-V_{DC}$. Making use of the volt-second averaging on the output voltage and (4.8), the duty cycle function for two-level VSIs becomes as in (4.10).

$$d_{v-2}(\theta) = \frac{1 + M\sin(\theta)}{2} \ , \ 0 < \theta < \pi \tag{4.10}$$

Combining (4.8), (4.9), and (4.10) yields the inductor current ripple for two-level VSIs can be obtained as in (4.11).

$$I_{s-r-2}(\theta) = \frac{V_{DC} T_s}{L_F} \cdot \left[\frac{1 - M^2 \sin^2(\theta)}{2} \right] \ , \ 0 < \theta < \pi \tag{4.11}$$

In three-level modulation, which is the modulation of ZV-GCTSI topologies, the output voltage of the VSI inverter oscillates between V_{DC}, zero, and $-V_{DC}$, yielding reduced ripple for the same amount of the filter inductance L_F. Moreover, internal reactive power circulation of two-level modulation at unity power factor is absent in three level modulation

inherently. In three-level modulation, the output voltage duty cycle function can be formulated as in (4.12).

$$d_{v-3}(\theta) = M\sin(\theta)\ ,\ 0 < \theta < \pi \tag{4.12}$$

Making use of (4.8), (4.9), and (4.12) the inductor current ripple for three-level VSIs can be obtained as in (4.13).

$$I_{s-r-3}(\theta) = \frac{V_{DC}T_s}{L_F}\cdot\left[M\sin(\theta) - M^2\sin^2(\theta)\right]\ ,\ 0 < \theta < \pi \tag{4.13}$$

In topologies like the one in [54] (Figure 3.35), and the proposed topologies PT-9 (Figure 3.36), and PT-10 (Figure 3.37); the output voltages of the converters exhibit five-level characteristics. In these topologies, the output voltage oscillates between V_{DC}, $-V_{DC}$, 0, and positive and negative values of the feed-forward voltages ($V_{DC\text{-}f}$, $-V_{DC\text{-}f}$) from the PV side. The voltage fed-forward by the PV source ($V_{DC\text{-}f}$) is ideally the maximum power point voltage. While the grid voltage in magnitude is smaller than the feed-forward voltage, the PV power flows to grid without experiencing any boost stage. When the grid voltage is higher than the feed-forward voltage, higher DC bus voltage (which is regulated continually to V_{DC}) is used to inject the power to the grid. The feed-forward voltage of the PV source is "σ" times the DC bus voltage, where σ is a variable depending on the number of PV modules, irradiation, and temperature as in (4.14). For the five-level VSIs, the duty cycle function of the output voltage changes as V_s changes in time to constitute the output voltage volt-seconds, as formulated in (4.15). Moreover, for five-level case, (4.9) should be modified as in (4.16).

$$\sigma \triangleq V_{DC-f}/V_{DC},\ \ 0 < \sigma < 1 \tag{4.14}$$

$$d_{v-5}(\theta) = \begin{cases} M\sin(\theta)/\sigma & for\ M\sin(\theta) < \sigma \\ \left(M\sin(\theta) - \sigma\right)/(1-\sigma) & for\ \sigma < M\sin(\theta) \end{cases}\ ,\ 0 < \theta < \pi\ ,\ 0 < \sigma < 1 \tag{4.15}$$

$$I_{s-r-5}(\theta) = \begin{cases} d_{v-5}(\theta)\cdot T_s\cdot(\sigma V_{DC} - V_s(\theta))/L_F & for\ M\sin(\theta) < \sigma \\ d_{v-5}(\theta)\cdot T_s\cdot(V_{DC} - V_s(\theta))/L_F & for\ \sigma < M\sin(\theta) \end{cases}\ ,\ 0 < \theta < \pi\ ,\ 0 < \sigma < 1 \tag{4.16}$$

Using (4.8), (4.15), and (4.16), peak-to-peak ripple on the filter inductor current of five-level topologies becomes as in (4.17).

$$I_{s-r-5}(\theta)=\begin{cases}\dfrac{V_{DC}T_s}{L_F}\cdot\left[M\sin(\theta)-M^2\sin^2(\theta)\right] & for \quad M\sin(\theta)<\sigma \\ \dfrac{V_{DC}T_s}{L_F}\cdot\left[\dfrac{(1-M\sin(\theta))\cdot(M\sin(\theta)-\sigma)}{1-\sigma}\right] & for \quad \sigma<M\sin(\theta)\end{cases}, 0<\theta<\pi\ , 0<\sigma<1 \quad (4.17)$$

Having the inductor current ripple functions for two, three, and five-level topologies in (4.11), (4.13), and (4.17) respectively, it is noticeable that the term $V_{DC}T_s/L_F$ is a common multiplier in these equations. Therefore, the topology dependent terms (ripple factors, Γ_2, Γ_3, Γ_5) can be collected as in (4.18), (4.19), and (4.20) for two, three, and five-level VSIs respectively.

$$\Gamma_2(\theta)\triangleq\frac{1-M^2\sin^2(\theta)}{2}\ ,\ 0<\theta<\pi \quad (4.18)$$

$$\Gamma_3(\theta)\triangleq M\sin(\theta)-M^2\sin^2(\theta)\ ,\ 0<\theta<\pi \quad (4.19)$$

$$\Gamma_5(\theta)\triangleq\begin{cases}M\sin(\theta)-M^2\sin^2(\theta) & for \quad M\sin(\theta)<\sigma \\ \dfrac{(1-M\sin(\theta))\cdot(M\sin(\theta)-\sigma)}{1-\sigma} & for \quad \sigma<M\sin(\theta)\end{cases}, 0<\theta<\pi\ ,\ 0<\sigma<1 \quad (4.20)$$

These factors are plotted in Figure 4.2 for M=1, M=0.85, and M=0.7 cases. As can be inferred from these figures, the peak-to-peak ripple value of the filter inductor current is greatly decreased as the number of the level of the output voltage increases.

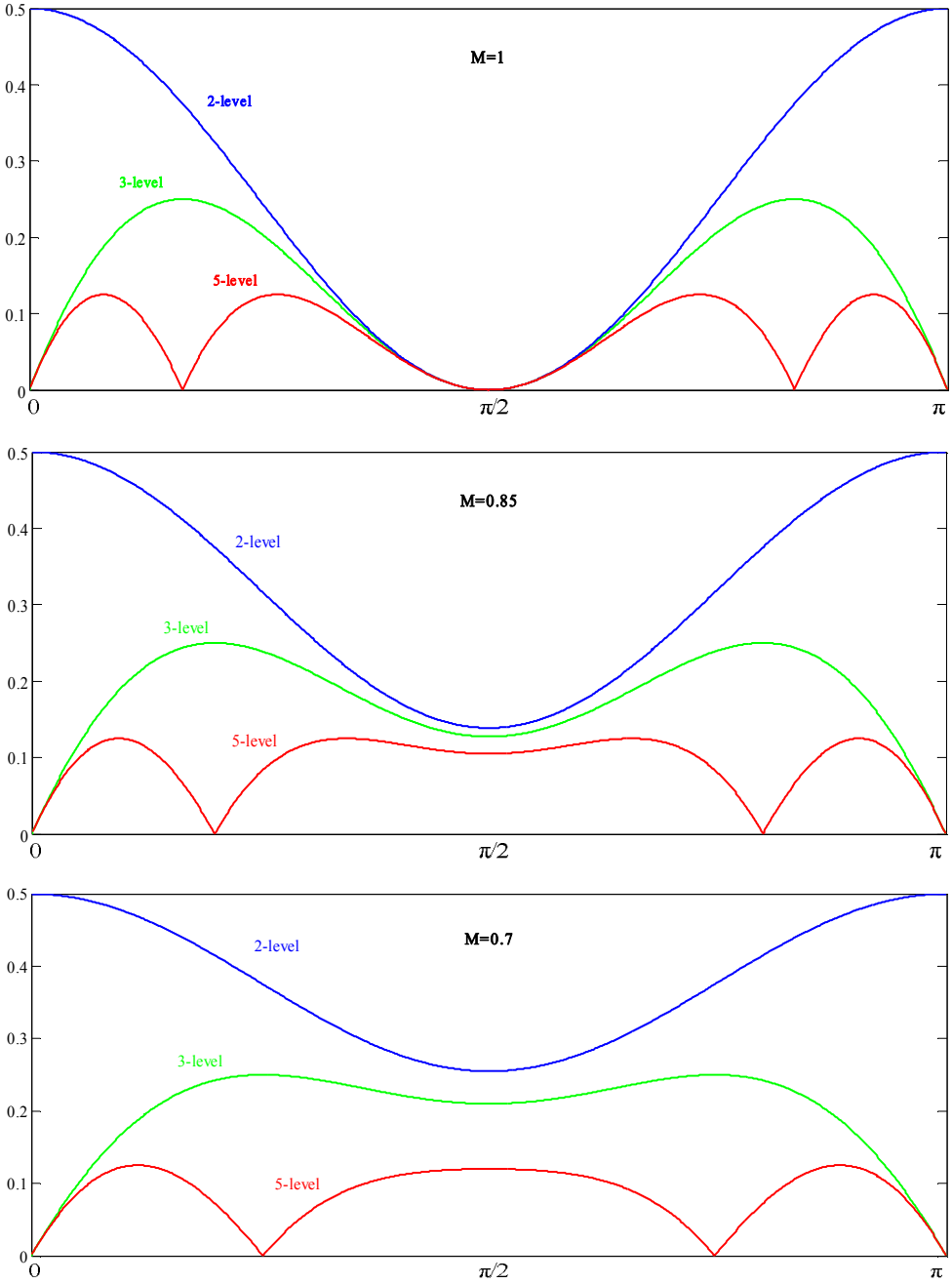


Figure 4.4 Filter inductor current ripple factors for two, three, and five-level VSI topologies for M=1 (top), M=0.85 (middle), and M=0.7 (bottom) cases. (σ=0.5 is assumed for five-level VSI topologies).

4.3.2 Simulation Results of Filter Inductor Current Ripples of GCTSI Topologies

In order to verify the filter inductor current ripple analyses made, simulations of H4 bipolar, H5, and PT-9 topologies are performed as the representatives of two, three, and five-level

GCTSIs respectively. The simulation parameters specified in Table 4.1 are used except the parasitic capacitance, which is taken zero since the focus in this section is the filter inductor current ripple. From the simulation parameters and using (4.7), M is taken to be 0.78 to compare the analyses and the simulations. The filter inductor current ripple waveforms of the simulated topologies are obtained by subtracting the fundamental component of the line currents from the actual line current waveforms. In Figure 4.5, the line current and filter inductor current ripple of H4 bipolar modulation are illustrated. As expected from the analysis, the highest filter inductor current ripple is encountered near the zero crossings of the grid voltage. Moreover, the maximum value of the peak-to-peak inductor current ripple of the simulation is nearly same as the one estimated from the analysis (5 A).

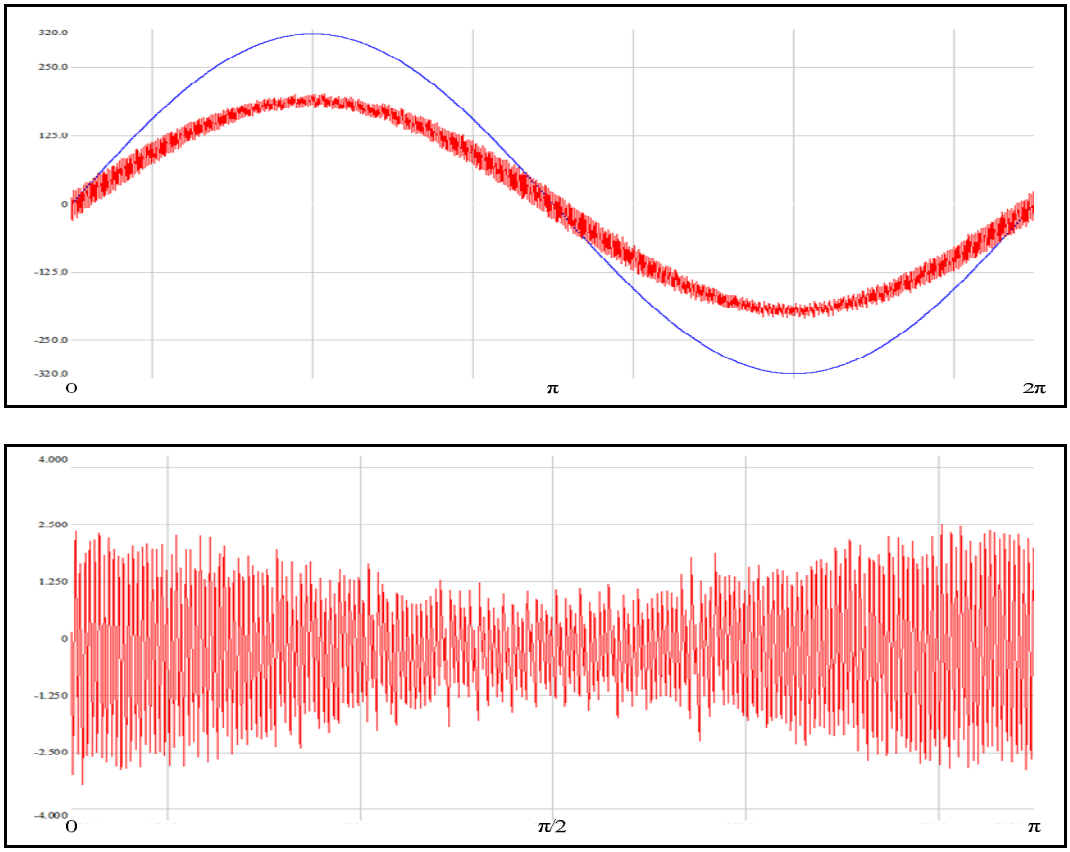


Figure 4.5 Illustration of grid voltage (V) (blue), grid current (A) (red, scale; 10 for grid current) for H4 bipolar modulation (top), and its filter inductor current ripple (A) (bottom) as a representative of two-level topologies at 3 kW.

In Figure 4.6, the grid voltage, the line current (top), and the filter inductor current ripple (bottom) of the H5 topology are illustrated as a representative of three-level voltage sourced GCTSI topologies (listed in Table 4.2). Unlike two-level topologies, near zero crossings, the

filter inductor current ripple tends to approach zero, which can be estimated, from the ripple analysis for three-level VSIs. The ripple factor for these inverters is zero in the zero crossing intervals as stated in (4.19). The maximum value of peak-to-peak value of the filter inductor current ripple obtained from the simulations is in high accordance with the analysis made for three-level VSIs. The value for the peak-to-peak current ripple is found 2.5 A from the analysis which is very close to the one that can be measured from the simulation waveforms for the ripple content of the inductor current. The distribution of the ripple current with respect to the electrical angle is as expected from the analysis.

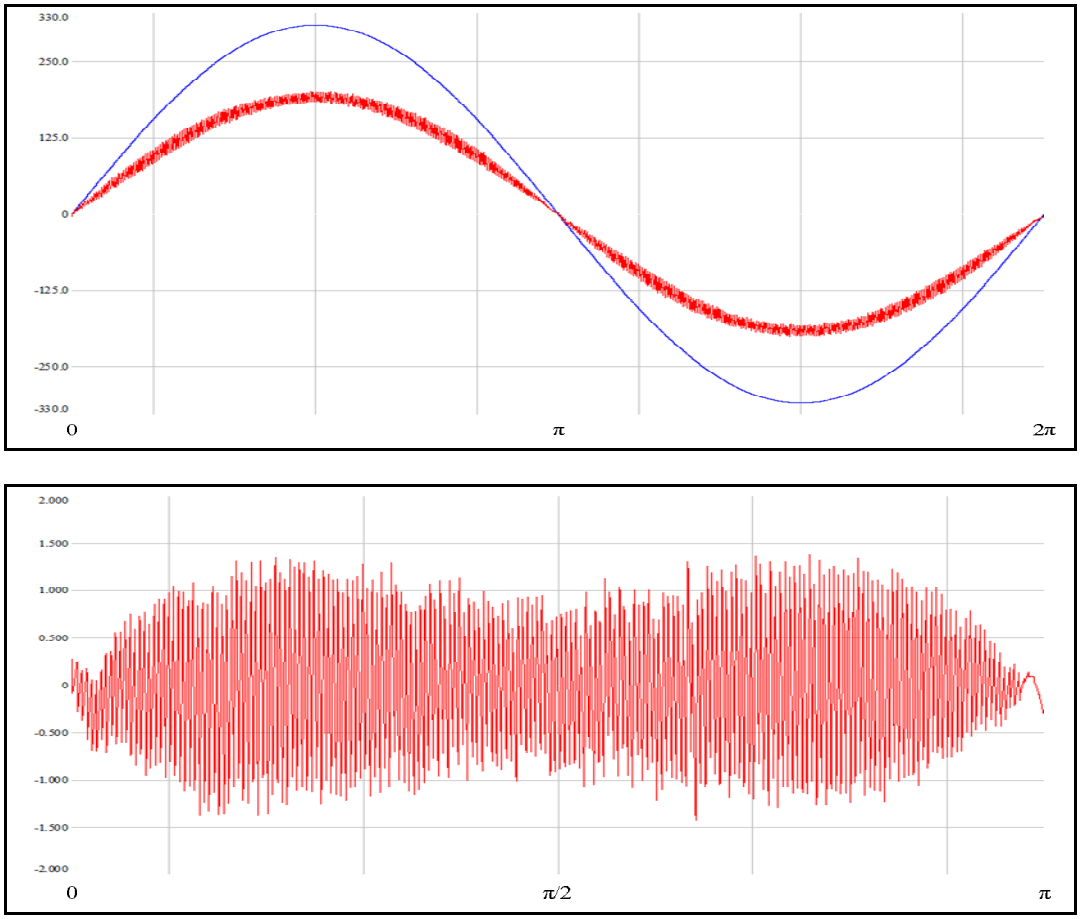


Figure 4.6 Illustration of grid voltage (V) (blue), grid current (A) (red, scale; 10 for grid current) for the H5 topology (top), and its filter inductor current ripple (A) (bottom) as a representative of three-level topologies at 3 kW.

In Figure 4.7, the grid voltage, the line current (top), and the filter inductor current ripple (bottom) of the proposed PT-9 topology are illustrated. The filter inductor current ripple characteristics of other five-level topologies are same as the only difference between PT-9 is

the switching matrix (the leakage current and the output voltage characteristics being same). As estimated from the analysis, the filter inductor current ripple approaches to zero at several points, where the grid current crosses zero level or the grid voltage approaches the feed-forward voltage from the PV source. The ripple factor obtained for five-level VSIs in (4.20) (with M=0.78) has a maximum value of 0.125. When the maximum value of the ripple factor is multiplied by the term $V_{DC}T_s/L_F$, the peak to peak ripple value for the filter inductor current is calculated as 1.25 A. From bottom figure, maximum peak to peak value of the filter inductor current can be observed to be very close to 1.25 A.

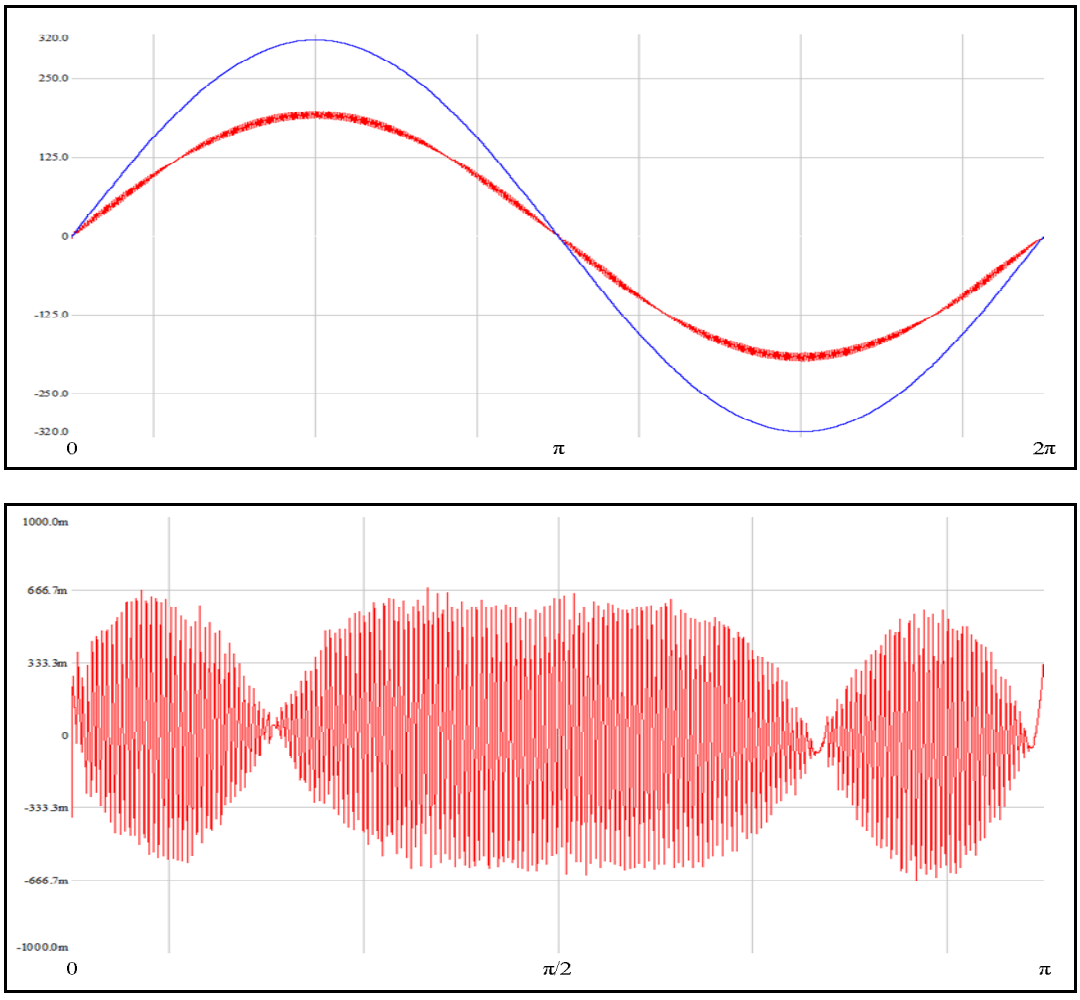


Figure 4.7 Illustration of grid voltage (V) (blue), grid current (A) (red, scale; 10 for grid current) for the proposed PT-9 topology (top), and its filter inductor current ripple (A) (bottom) as a representative of five-level topologies at 3 kW.

4.3.3 Comparison of Filter Inductor Current Ripple Performances of GCTSI Topologies

In section 4.3.1 the analyses for the filter inductor current ripples of two, three, and five-level voltage sourced GCTSI topologies are performed. Following the analyses, simulation waveforms are provided in section 4.3.2. From the simulation waveforms, it is observed that measured values of the filter inductor current ripples for two, three, and five-level inverters are in high accordance with the ones that are calculated. The approximation of zero volt-seconds integral on the filter inductor (4.8) gave highly accurate results.

Throughout the analyses and the simulations, the frequency of the output voltage (V_{dm}) is kept constant for each topology and the corresponding filter inductor current ripples and the ripple factors are calculated and simulated accordingly. From the analyses and simulations, the peak value of the filter inductor current ripple is observed to be halved for the same value of the DC bus voltage (V_{DC}) and output voltage frequency (f_s) as one goes from two-level to three-level, or three level to five-level VSIs. The peak value of the ripple content is generally used to determine the value of the filter inductance of the VSI under interest, which is generally taken to be smaller than 10~20% of rated line current. Therefore, for the same peak value of the ripple current, required filter inductance is halved as one increase the number of level of the output voltage. Besides, the filter inductor losses are also reduced due to smaller size of the inductor. Even in the case for the same inductance value, inductor dependent losses can be greatly reduced as the number of the level of the output voltage increased. This is because of the reduced filter inductor current ripple, therefore reduced areas of minor loops in the B-H curve of the filter inductor.

Although the peak ripple factor of two-level VSIs is found to be twice the ripple factor of three-level VSIs for the same output voltage frequency, H4 bipolar should be re-evaluated for the filter inductor losses. For the same effective switching frequency, H4 bipolar modulation has switching losses approximately twice the switching losses of H4 unipolar modulation. Therefore, for the same switching losses, the maximum of filter inductor current ripple factor becomes four times the maximum of the peak current ripple factor of the H4 unipolar modulation, which results higher current ripple and higher inductance. Therefore, H4 bipolar modulation has great efficiency drawback due to filter inductor losses as compared to H4 unipolar modulation. Three or five-level GCTSI topologies are favourable as they exhibit reduced filter inductor losses due to reduced current ripple.

4.4 Leakage Current Analyses and Simulation Results of GCTSI Topologies

In order to be able to design a GCTSI with low leakage current, the sources of the leakage current in GCTSI topologies should be investigated. Therefore, this section is devoted to the investigation of leakage current mechanisms in GCTSI topologies, and their verification by making use of simulation waveforms. First, the leakage current characteristics of the root topology for many inverter topologies, the H4 topology is investigated and the simulation results are provided to verify the analyses made as it is bipolar and unipolar modulated. Then ZVI-GCTSI, ZVMC-GCTSI, ZVH-GCTSI, and SC-GCTSI families will be investigated similarly, and the sources of the leakage current in these topologies will be highlighted with the simulation-based verifications. Through the analytical investigation of inverter families, an equivalent circuit will be provided. The leakage current characteristics of the members of a family are similar to each other as they exhibit same strategy to reduce leakage current. Therefore, same results are valid for the members of a GCTSI family other than the one analyzed.

4.4.1 Leakage Current Analyses and Simulation Results of the Conventional H4 Topology

The H4 topology (Figure 4.8) has been employed in many power electronics applications for many years. The modulation of the H4 topology can be realized in two patterns; bipolar and unipolar.

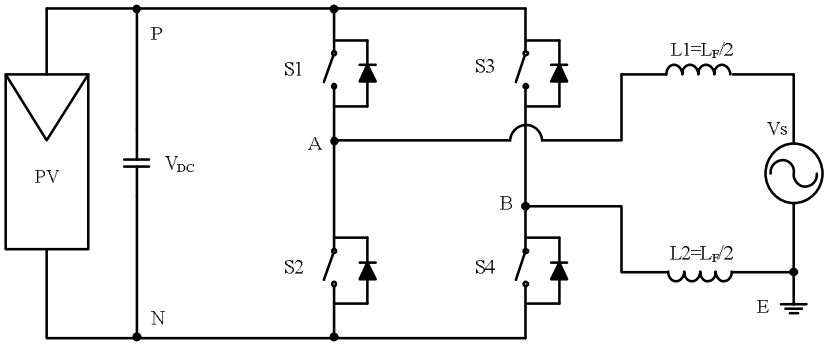


Figure 4.8 The H4 topology.

In bipolar switching pattern, only cross switches (S1, S4 and S2, S3) are conducting at any time to shape the line current. As a result of such an operation, the inductor current ripple of the topology greatly increases due to two level operation as studied in section 4.3. Moreover,

high internal reactive power circulation is another drawback of H4 bipolar switching pattern that is decreasing the energy conversion efficiency. Defined in (4.21), Common Mode Voltage (CMV), which is the voltage forcing a current through the earth, is constant in this type switching pattern (V_{cm}=V_{DC}/2). Making use of the equivalent circuit in Figure 4.9 for the H4 bipolar switching pattern, only grid voltage is found to be the reason of the leakage current in this switching pattern of the H4 topology.

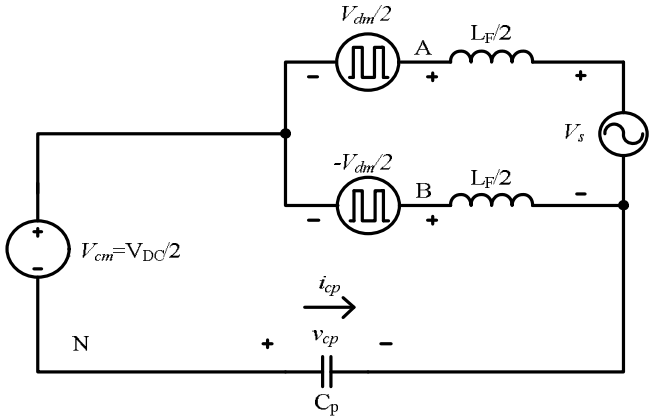


Figure 4.9 Equivalent circuit for leakage current evaluation of the H4 topology bipolar modulation.

$$V_{cm} \triangleq \frac{V_{AN} + V_{BN}}{2} \tag{4.21}$$

In Figure 4.6, the grid voltage (V_s), and the leakage current (red) of the H4 topology is illustrated for a parasitic capacitance of 500 nF. As shown in the Figure 4.10 and as can be interpreted from the leakage current equivalent circuit of the H4 topology bipolar switching pattern in Figure 4.9, the parasitic capacitor current is only grid voltage dependent, where the current is the capacitor response to the half of the grid voltage ($i_{c-p} = \frac{C_p}{2}\frac{dV_s}{dt}$). Therefore, the leakage current in H4 bipolar modulation is as low as not to break standard limitations even for high levels of parasitic capacitance. However, in the application, due to dead times or non ideal commutation behaviours of the semiconductors, a high frequency content in the CMV of the bipolar switching pattern may be encountered. Since these deviation durations of CMV from half of the DC bus voltage is short in time, the resulting high frequency leakage currents become suppressible with a small Common Mode Inductor (CMI).

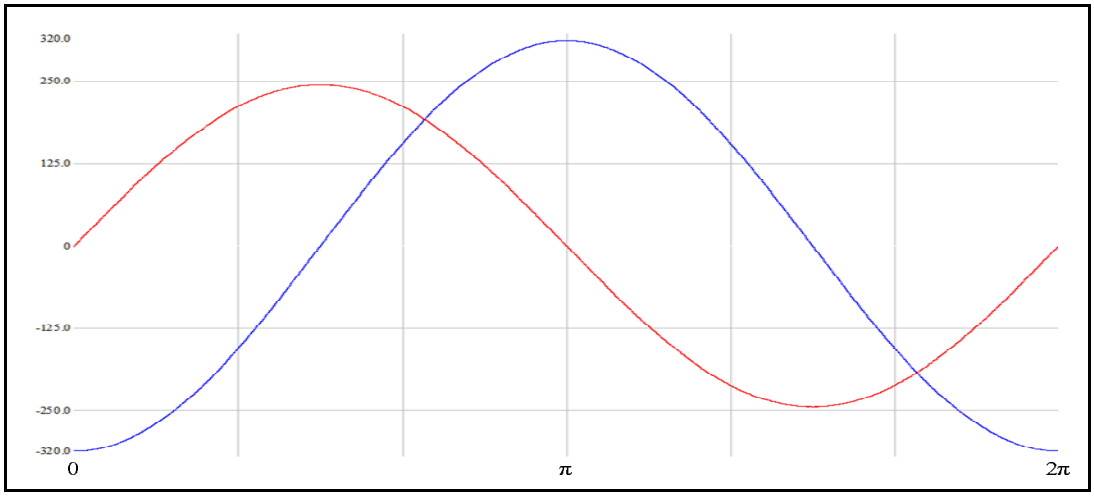


Figure 4.10 The leakage current (A) (red, scale; ×10000) of the H4 topology bipolar switching pattern, and the grid voltage (V) (blue).

In unipolar modulation, the voltage reference signal and its negative are given to the same carrier triangle waveform to obtain the gate logic signals of the switches in each leg. As a result of such an operation, CMV of the H4 topology oscillates either between half of the DC bus voltage and the DC bus voltage, or between half of the DC bus voltage and zero voltage, depending on the polarity of the reference voltage. The equivalent circuit for the leakage current evaluation of H4 unipolar modulation is depicted in Figure 4.11. The CMV variation in this equivalent circuit constitutes the major component of the parasitic current. In Figure 4.12, the leakage current of the H4 topology is illustrated for a parasitic capacitance of 50 nF. Even at 50 nF of parasitic capacitance, the peak level of the parasitic current can exceed 5 A, which is not acceptable in PV applications.

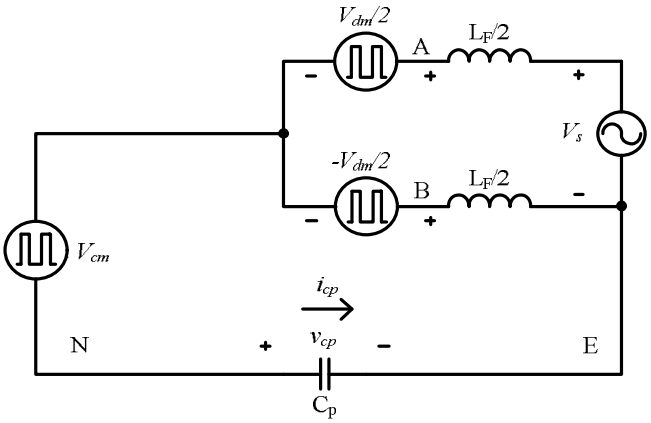


Figure 4.11 Equivalent circuit for leakage current evaluation of the H4 topology unipolar modulation.

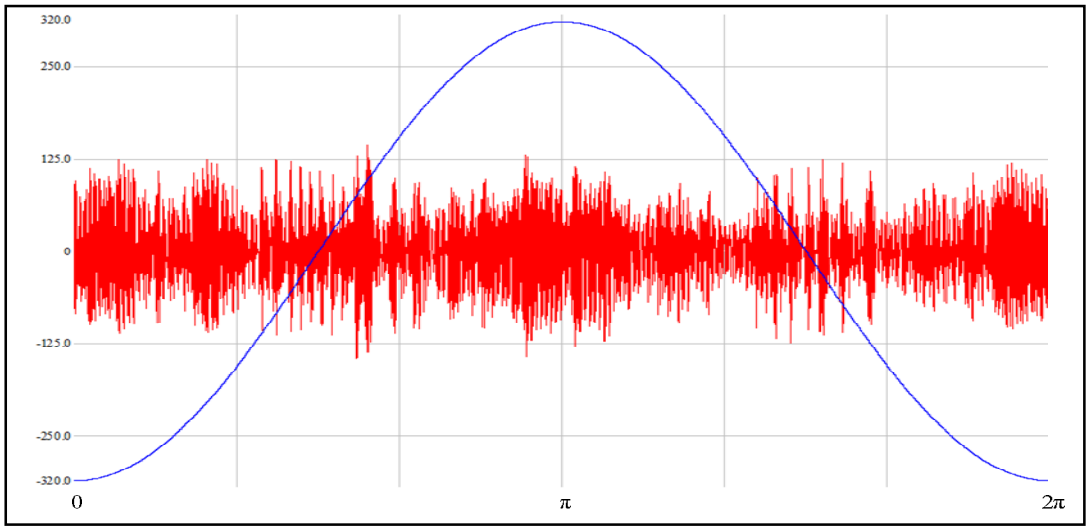


Figure 4.12 The leakage current (A) (red, scale; ×20) of the H4 topology unipolar switching pattern, and the grid voltage (V) (blue). For C_p=500 nF, it is not possible to even regulate the line current.

4.4.2 Leakage Current Analysis and Simulation Results of ZVI-GCTSI Topologies

In ZVI-GCTSI topologies, while the leakage current is small, its attributes are not well understood. The leakage current study in [59], which includes the HERIC topology, has a limited scope and validity range and it is not applicable to asymmetric topologies such as the H5 topology with varying CMV. In [53], while studying the leakage currents in various ZVI-GCTSI topologies, the leakage currents have been attributed to the CMV of the circuit; however, there is no clear explanation or proof of this claim. Moreover, the belief that the parasitic currents in these converters are sourced by the CMV variation is not abandoned yet as indicated in [60]. In this section, a detailed model for the leakage current is established, and it is shown that the cause of the leakage current in these topologies is the grid voltage variation rather than the CMV.

Shown in Figure 4.13, equivalent circuit of a ZVI-GCTSI is modelled with the zero vector isolation switch "S_e", which is the only difference between the equivalent circuit of the H4 topology unipolar switching pattern. In the ZVI-GCTSIs, the leakage current characteristics are obtained by investigating the leakage current contribution of each source on the parasitic capacitance (C_p), i.e. using superposition. Then, the total current and voltage on C_p becomes the sum of the contribution of each source defined in (4.22) and (4.23), where "i_{cp-cm}" is

the parasitic current caused by CMV (or V_{cm}), "i_{cp-dm}" is the parasitic current caused by differential mode voltage (V_{cm}) and "i_{cp-s}" is the parasitic current due to the grid voltage on C_p, respectively. Likewise, this definition holds for the capacitor voltage.

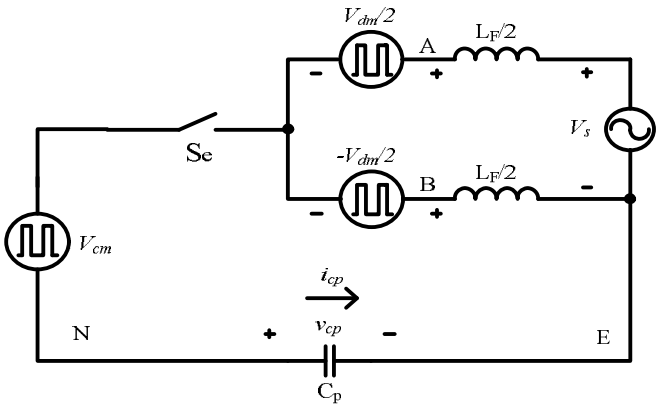


Figure 4.13 ZVI-GCTSI equivalent circuit for leakage current evaluation.

$$i_{cp} = i_{cp-cm} + i_{cp-dm} + i_{cp-s} \tag{4.22}$$

$$v_{cp} = v_{cp-cm} + v_{cp-dm} + v_{cp-s} \tag{4.23}$$

The foregoing analysis will be conducted for one of the widely known ZVI-GCTSI topologies with zero vector isolation; the H5 topology. In this configuration, at zero vectors the AC and DC circuits are isolated by the switches S2, S4, and S5 (shown in Figure 4.14). The ideal switch "S_e" on the H5 equivalent circuit (Figure 4.13) does the work of these switches, simply representing isolation at zero vectors. Ideally, at zero vectors, no parasitic capacitor current flows between AC and DC circuits, due to the decoupling in these intervals. The reason behind this phenomenon is the single wire connection between two Gaussian surfaces (i.e. at zero vectors there is no return path for the parasitic capacitor current, i_{cp}).

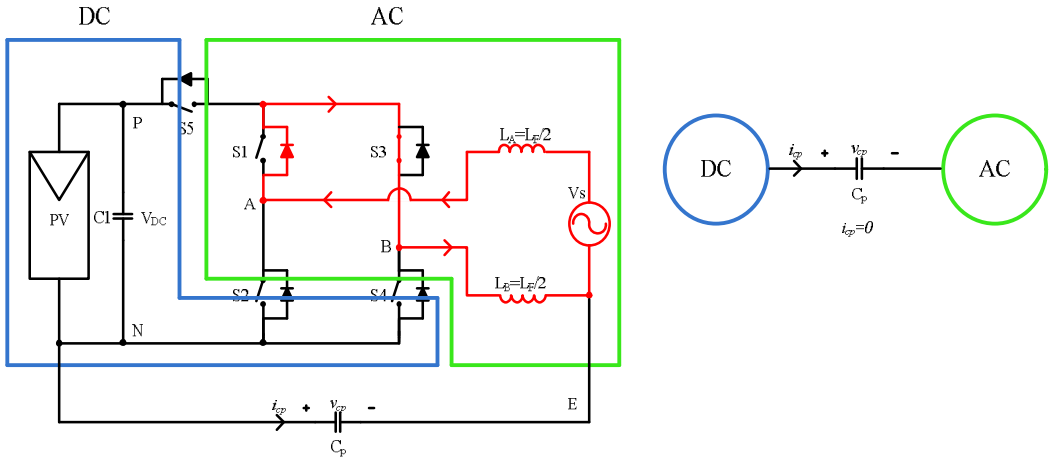


Figure 4.14 Illustration of decoupling of AC and DC circuits of ZVI-GCTSI topologies at zero vectors with the representative topology of this class; H5. Ideally, no parasitic current flows in the zero vector intervals as the return path is absent in these intervals.

In Figure 4.15, the common-mode equivalent circuit is illustrated. Using (4.21), the CMV is found as $V_{DC}/2$ for active vectors and $V_{DC}/3$ for zero vectors where V_{DC} is the DC bus voltage, where the switches are assumed to have same off-state impedance. Shown in Figure 4.16, the CMV of the circuit and the state of the switch has the same phase. Thus, using passive sign convention, the common-mode voltage component of v_{cp} ($v_{cp\text{-}cm}$) remains constant at $-V_{DC}/2$ in the common-mode equivalent circuit and the parasitic current due to CMV becomes zero at steady state ($v_{cp\text{-}cm}$=$-V_{DC}/2$, $i_{cp\text{-}cm}$=0). This result can be simply conceived from Figures 4.15 and 4.16 as a voltage source having infinite Thevenin impedance at certain durations (zero vector durations), therefore yielding no leakage current at steady state (i.e. after $v_{cp\text{-}cm}$ reaches its steady state value $-V_{DC}/2$).

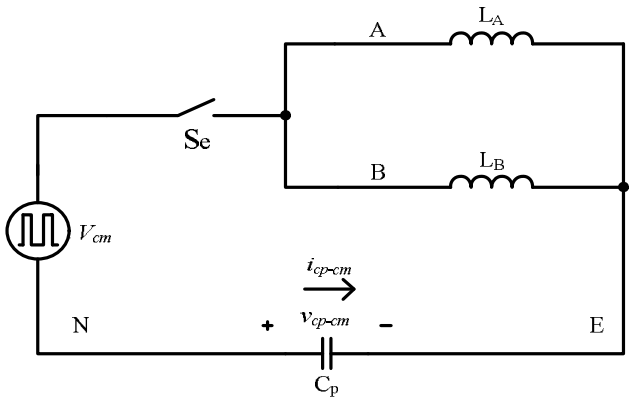


Figure 4.15 Common-mode equivalent circuit for ZVI-GCTSI topologies.

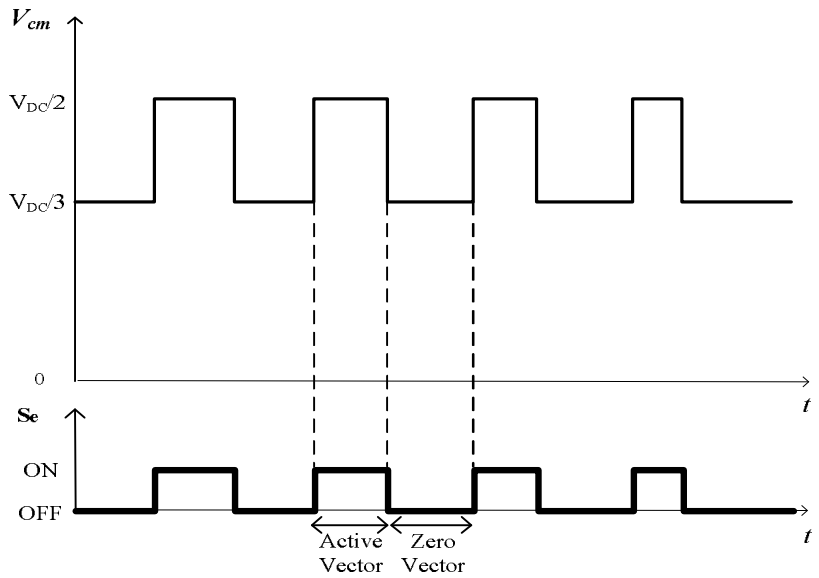


Figure 4.16 ZVI-GCTSI CMV and isolation switch state in the common-mode equivalent circuit illustrated for a representative of ZVI-GCTSI topologies; the H5 topology.

In order to understand the differential-mode voltage effects on the leakage current, the equivalent circuit in Figure 4.17 is illustrated. Due to symmetry in the differential-mode circuit, parasitic capacitor voltage and leakage current caused by differential-mode cancel and the voltage and thus the current becomes zero ($v_{cp\text{-}dm}$=0, $i_{cp\text{-}dm}$=0).

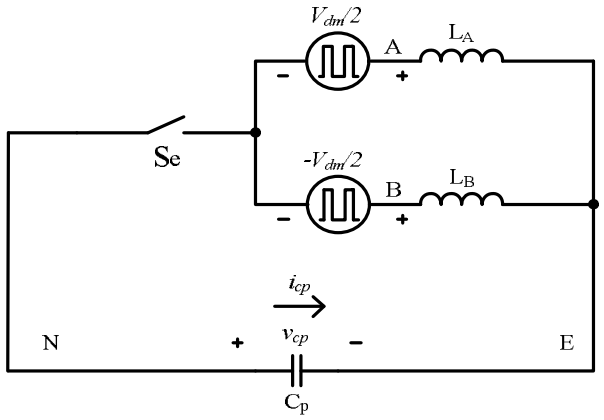


Figure 4.17 Differential mode equivalent circuit of ZVI-GCTSI topologies.

With zero contribution from both the differential-mode and the common-mode voltages of the inverter, total leakage current reduces to the leakage current contributed by the grid voltage only (4.24). As a result, the equivalent circuit is reduced to that in Figure 4.18. In

this equivalent circuit, the switch "S_e" has a state depending on the vector applied i.e., off during zero vectors and on during active vectors.

$$i_{cp} = i_{cp-s} \tag{4.24}$$

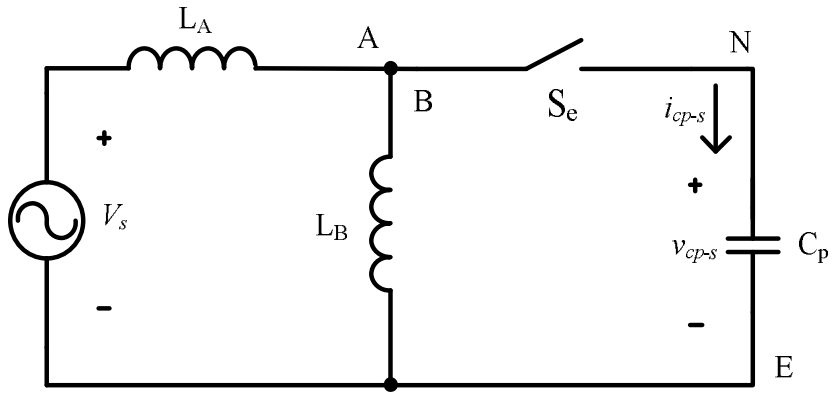


Figure 4.18 Simplified leakage current equivalent circuit for ZVI-GCTSI topologies.

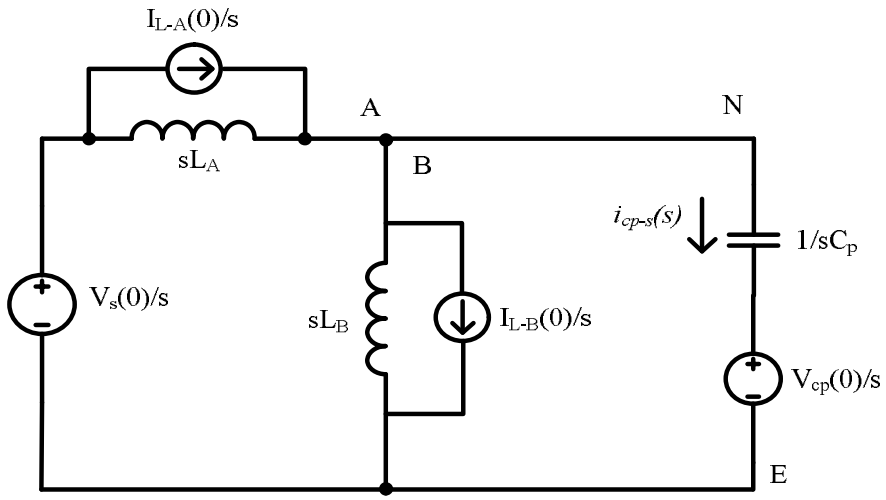


Figure 4.19 Simplified leakage current equivalent circuit transformed to s-domain at the instant of the equivalent switch "S_e" is closed.

The leakage current behaviour of this equivalent circuit can be investigated through the equivalent circuit in Figure 4.19 for high duty cycle region of this class of converters operating at unity power factor. In this region, the grid voltage variation is negligible with respect to the grid voltage amplitude at the switching period (T_s); as a result, the approximation of grid voltage as a step input for a switching period is reasonable. The independent current sources in Figure 4.19 are nothing but the differential mode inductor

initial currents, which are also the grid current and equal to each other at the instant of active vector applied ($(I_{L-A}(0) = I_{L-B}(0)$). Due to anti-symmetric behaviour of these current sources, their eventual contribution to parasitic capacitor current ($I_{cp-s}(s)$) is zero. After applying basic superposition and current division rules on the circuit in Figure 4.19, the leakage current can be found in s-domain as in (4.25), its time domain expression in (4.26), and the resonant frequency of the leakage current is in (4.27).

$$i_{cp-s}(s) = \frac{2\left[V_s(0) - 2V_{cp}(0)\right]/L_F}{s^2 + \frac{4}{L_F C_p}} \tag{4.25}$$

$$i_{cp-s}(t) = \frac{V_s(0) - 2V_{cp}(0)}{\sqrt{\frac{L_F}{C_p}}} \cdot \sin\left(\frac{2}{\sqrt{L_F C_p}} t\right) \tag{4.26}$$

$$f_r = \frac{1}{\pi\sqrt{L_F C_p}} \tag{4.27}$$

The circuit in Figure 4.13 is investigated for zero parasitic capacitance (C_p=0) representing the no parasitic effect operating condition, to observe the superposition on parasitic capacitor (or N-E) voltage. In Figure 4.6, the line voltage and current of the simulated topology are illustrated previously, showing steady-state satisfactory performance (unity power factor and low distortion) for the H5 topology. In Figure 4.20, the virtual parasitic capacitor voltage (v_{cp}) (considering very small C_p) is illustrated to verify the analysis made in (4.23), the superposition of the voltage sources. In this case, the common-mode voltage in Figure 4.16 is superposed on the grid voltage component as the equivalent circuit of the topology (Figure 4.13) suggests. The common-mode voltage has an offset and pulsates with the voltage difference of (V_{DC}/2)-(V_{DC}/3) which amounts to 67 V. This CMV has high impedance states at zero vector durations as suggested in Figure 4.16.

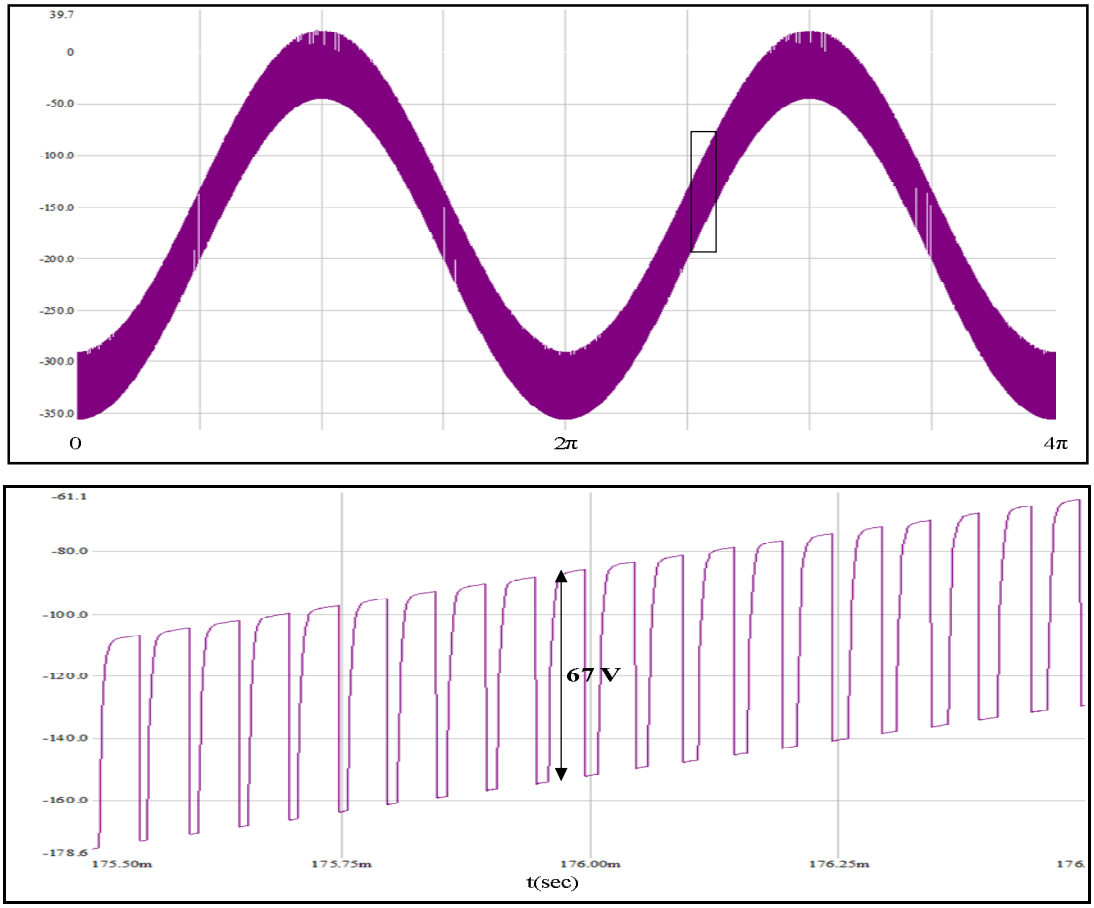


Figure 4.20 The N-E (or virtual v_{cp}) voltage (V) waveform for zero parasitic capacitance case; full waveform (top), microscopic view (bottom).

In Figure 4.21 and 4.22, the parasitic capacitor current and voltage waveforms are illustrated for the two C_p cases (50 nF and 500 nF respectively). Since the isolation switch (S_e) blocks current during off-state, the parasitic capacitor voltage cannot change and the high frequency CMV does not affect the capacitor voltage. On the other hand, every PWM cycle when S_e is turned on, due to the voltage difference between the parasitic capacitor voltage and the grid voltage, a current pulse is induced according to the LC resonant circuit in the equivalent circuit of Figure 4.18.

High frequency component on the parasitic capacitor voltage in Figure 4.20 is smoothed due to the fact that the voltage appearing on zero vector states have high impedance and common-mode voltage change seen on the parasitic capacitance is already blocked by the isolating switches in the simulated circuit (S2, S4, S5) or by the zero vector isolation switch in Figure 4.13 (equivalent circuit). As it can also be estimated from the simplified leakage current equivalent circuit (Figure 4.18), maximum leakage currents flow around zero

crossings of grid voltage since maximum voltage changes (dV_s/dt) is maximum in magnitude) and minimum active vector duty cycles are encountered in these intervals. Parasitic capacitor voltages have a DC offset (due to CMV) of $-V_{DC}/2$ (-200 V in this case) as estimated from the analysis. As can be inferred from Figures 4.21 and 4.22, with small C_p the peak current is 100 mA while with large C_p the peak current exceeds 500 mA. At each active vector, the parasitic capacitor is charged to half of the grid voltage. Thus, the capacitor voltage changes smoothly following the grid voltage change.

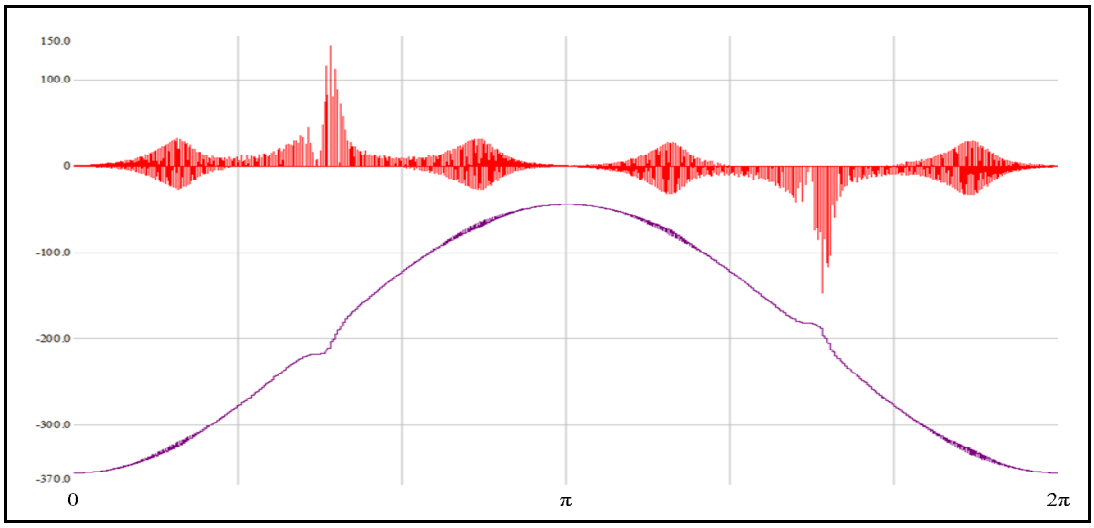


Figure 4.21 Parasitic capacitor current (A) (red, scale; ×1000) and voltage (V) (purple) for C_p=50 nF.

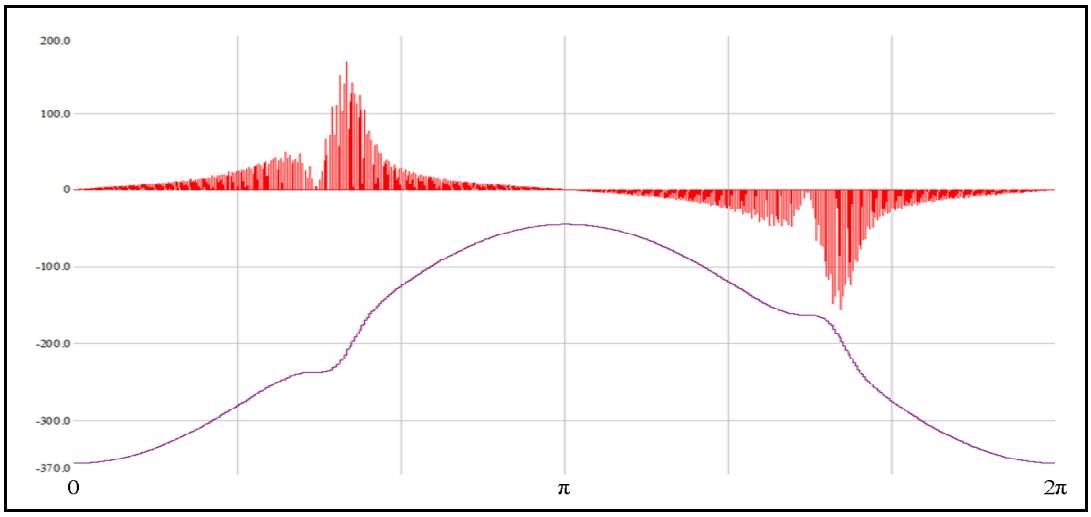


Figure 4.22 Parasitic capacitor current (A) (red, scale; ×250) and voltage (V) (purple) for C_p=500 nF.

In Figure 4.23, microscopic behaviour of the parasitic capacitor current and voltage are illustrated for the worst case (near zero crossing of grid voltage) at C_p=50 nF. In this region, the grid voltage change is at its maximum and as the zero vector periods become large, the difference between the grid voltage and parasitic capacitor voltage grows. Following zero vectors, as the active switch state is applied, large peak needle shaped leakage currents flow (90 mA in Figure 4.23) and C_p voltage changes in steps.

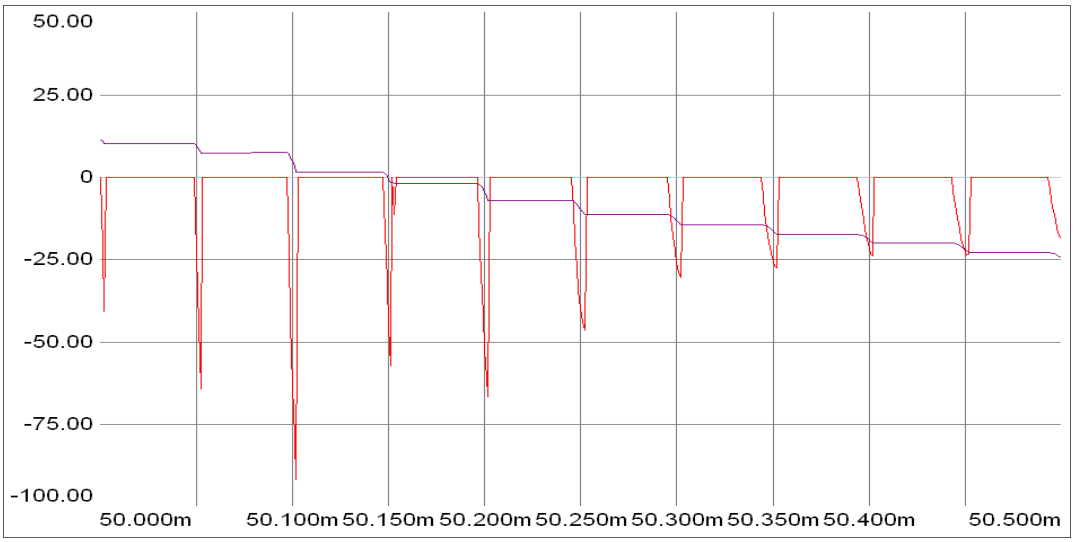


Figure 4.23 Microscopic view of parasitic capacitor voltage (V) (purple, offset; +200V) and current (A) (red, scale; ×1000) with respect to time (sec) for C_p=50 nF.

In Figure 4.24, the leakage current is displayed with the differential-mode voltage (V_{dm}) for two cycles both for high and low duty cycle intervals illustrating the isolation at zero vectors. As suggested in Figure 4.14, no leakage current flows at zero vectors. At active vectors the circuit goes into resonance (shown in Figure 4.24) with a period of 32 µsec (corresponding to 31.3 kHz) until the next zero vector starts. Having equivalent circuit parameters and using (4.27), the resonant frequency of the simplified leakage current equivalent circuit is found to be 31.8 kHz, which is nearly the same as in the simulation. In the application, the output capacitances of the semiconductors and other parasitic capacitances existent in the circuit may introduce leakage current at zero vectors, however, the current is expected to be very low as the semiconductor parasitic capacitances and other stray capacitances are very low (in the order of pF) to cause considerable parasitic current.

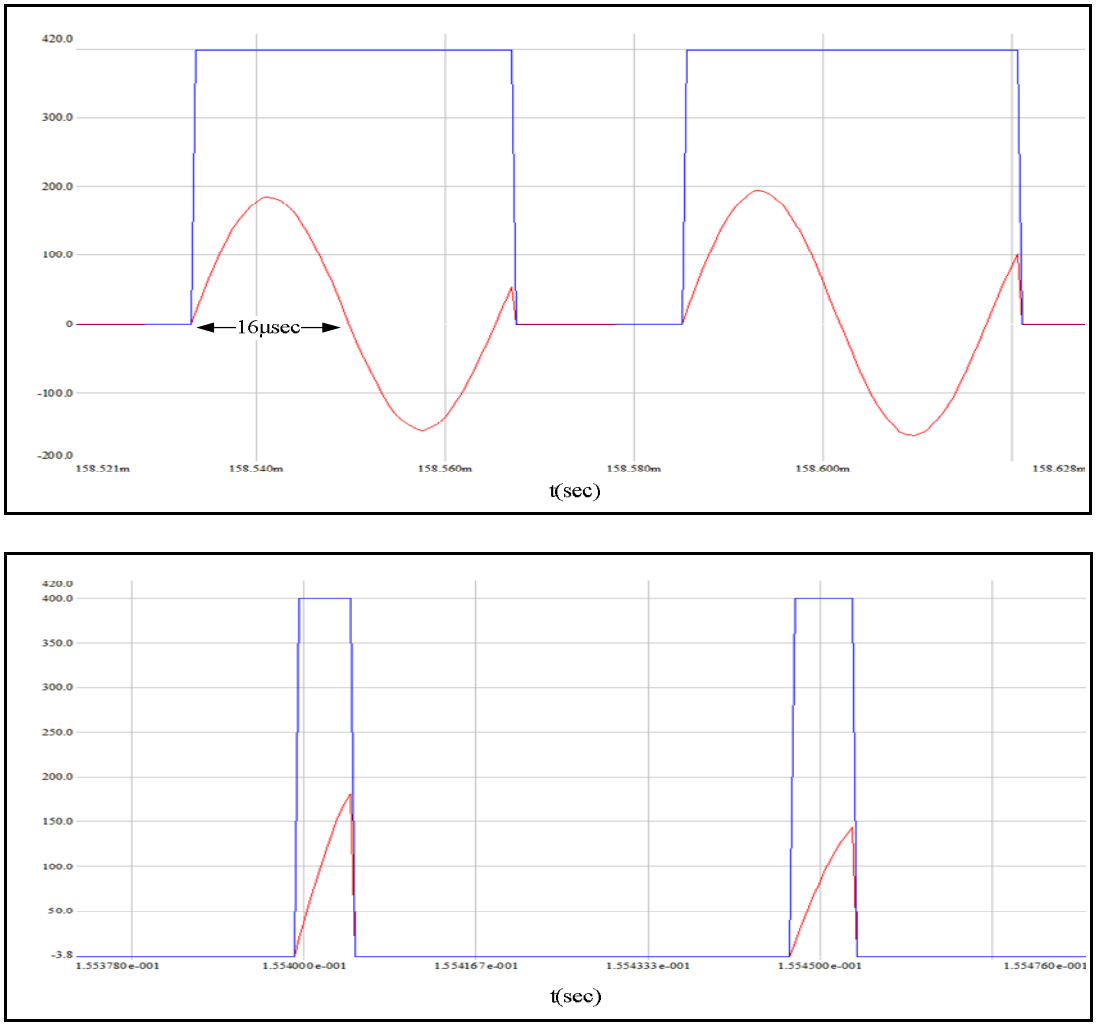


Figure 4.24 Differential mode voltage (V) (blue) and parasitic current (A) (red) for high (top) and low (bottom) duty cycles [current scales; (top): ×10000, (bottom): ×1000].

The leakage current analysis made indicates that the leakage current in the ZVI-GCTSI topologies are not due to the CMV variation, but due to the grid voltage variation chopped by the equivalent switch in the equivalent circuit of ZVI-GCTSI topologies (Figure 4.18), or by the switches separating AC and DC circuits in the ZVI-GCTSI topology under investigation. Having this conclusion, the Figure 4.25 depicts the grid voltage (V_s), and the parasitic capacitor current (i_{cp}) for a parasitic capacitor of 500 nF. The chopped half of V_s constitutes the leakage current in Figure 4.25, where the low frequency characteristics of H4 bipolar modulation leakage current turned out to be high frequency capacitor response. As compared to H4 unipolar modulation, the leakage current characteristics of ZVI-GCTSI topologies are quite reduced.

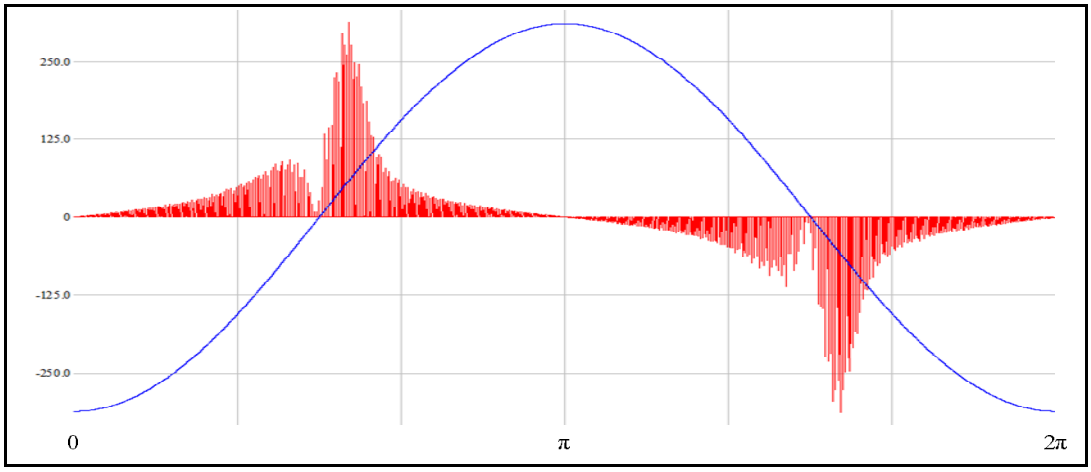


Figure 4.25 Illustration of grid voltage (V) (blue) and parasitic capacitor current (A) (red, scale; ×500) of the H5 topology, as a representative of ZVI-GCTSI topologies for C_p=500 nF.

Having these results, section 4.4.3 investigates the leakage current characteristics of ZVI-GCTSI topologies with CMI and parasitic capacitance variation.

4.4.3 Effect of C_p and CMI Variation on the Leakage Current Characteristics of ZVI-GCTSI Topologies

Figure 4.26 illustrates the leakage current and parasitic capacitance voltage (simulations for C_p=50 nF (top) and C_p=500 nF (bottom)) when 3 mH of CMI (L_{cm}) is added to further reduce the leakage current in ZVI-GCTSI topologies. Although, from the analysis, the source of the leakage current found not to be CMV variation, CMI suppresses some part of the leakage current as it is in series with the parasitic capacitance discharge path. With the addition of 3 mH of common-mode inductor, the peak values of the leakage current decrease from 100 mA to 65 mA for C_p=50 nF, and from 500 mA to 250 mA for C_p=500 nF case.

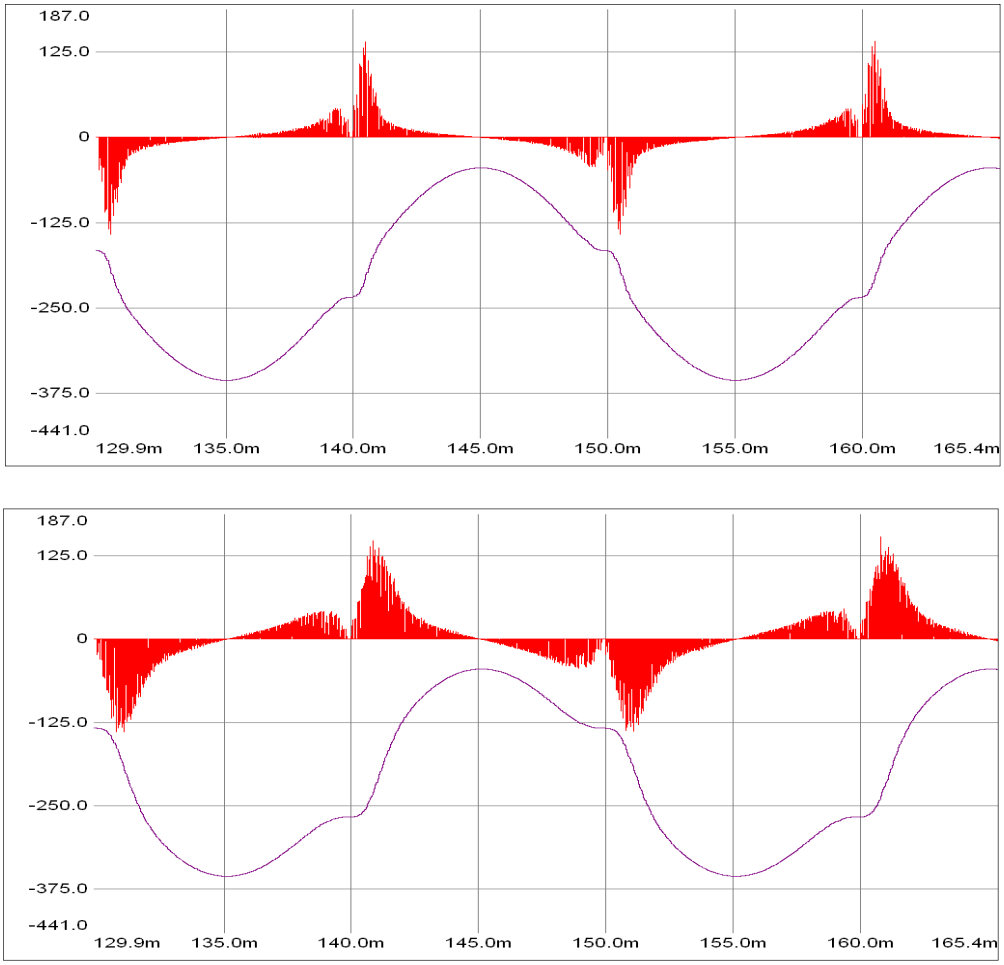
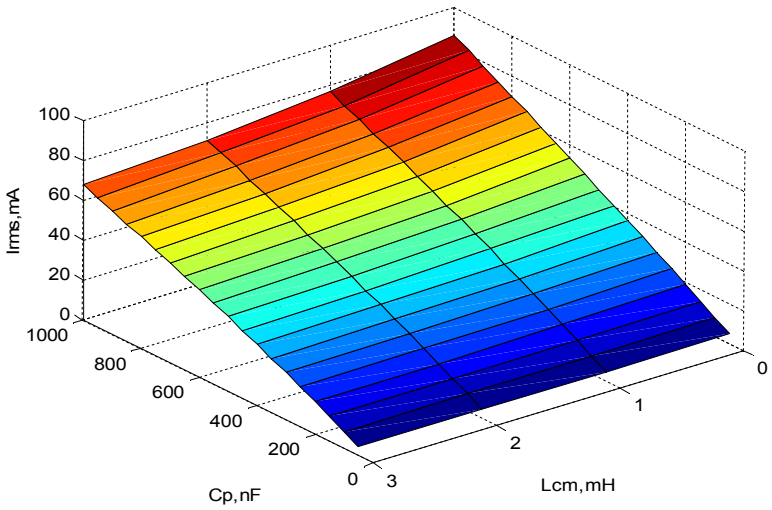


Figure 4.26 Parasitic capacitor current (A) (red, scale; ×2000 (top), ×500 (bottom)) and voltage (V) (purple) for C_p=50 nF (top), and C_p=500 nF (bottom) of ZVI-GCTSI topologies with the insertion of CMI (L_{cm}=3 mH).

Illustrated in Figure 4.27, peak and RMS values of the leakage current for varying CMI (L_{cm}) and parasitic capacitance (C_p) are obtained from the simulations. It can be concluded that, the RMS value of the leakage current is linearly dependent on the parasitic capacitance value, whereas the RMS value of the leakage current is nearly independent of the CMI value inserted. This is due to the fact that, the suppression of line frequency leakage current cannot be performed by the CMI as the impedance of the CMI under low frequency is low. However, as depicted in Figure 4.27 (b), the peak value of the leakage currents can be greatly suppressed with the increase in the CMV. This is due to the high impedance characteristics of CMI under high frequency excitation.

(*a*)



(*b*)

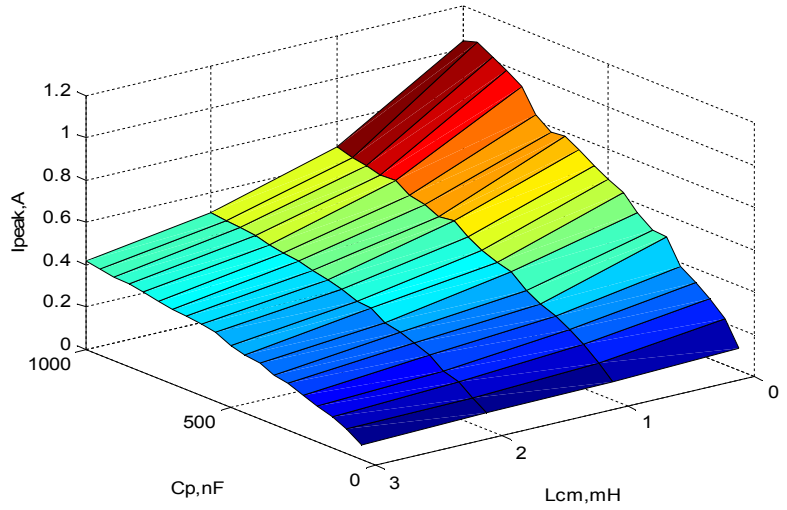


Figure 4.27 RMS (*a*) and peak (*b*) values of leakage current for varying parasitic capacitance (C_p) and CMI (L_{cm}).

4.4.4 Leakage Current Analyses and Simulation Results of ZVMC-GCTSI Topologies

As their name suggests, ZVMC-GCTSI topologies perform connection of inverter side (the side residing between the filter inductors and the isolation switches) of AC circuit to the midpoint of the DC bus at zero vectors as shown in Figure 4.28 for the topology in [52] as a representative of ZVMC-GCTSI topologies. The CMV of these topologies at active vectors is $V_{DC}/2$. With the connection to the midpoint of the DC bus, the CMV of these topologies

again becomes $V_{DC}/2$. Therefore, the CMV of these topologies becomes ideally constant in time, under normal operating conditions. Having constant CMV, the equivalent circuit for these topologies can be established as in Figure 4.29, which appears to be the same as the equivalent circuit of H4 bipolar modulation in Figure 4.9. However, this is not the case as the differential mode (or output) voltage of ZVMC-GCTSI topologies being three-level. Therefore, the constant CMV advantage of H4 bipolar modulation, and the three-level output voltage of H4 unipolar modulation are united in ZVMC-GCTSI topologies, eliminating the drawbacks of the H4 topology addresses in section 4.4.1.

These topologies can be derived from ZVI-GCTSI topologies with a midpoint connection switch. This switch becomes ON at zero vectors to provide connection between the AC side of the inverter and the midpoint of the DC bus (for example the iH5 topology proposed in [53], which is derived from the H5 topology).

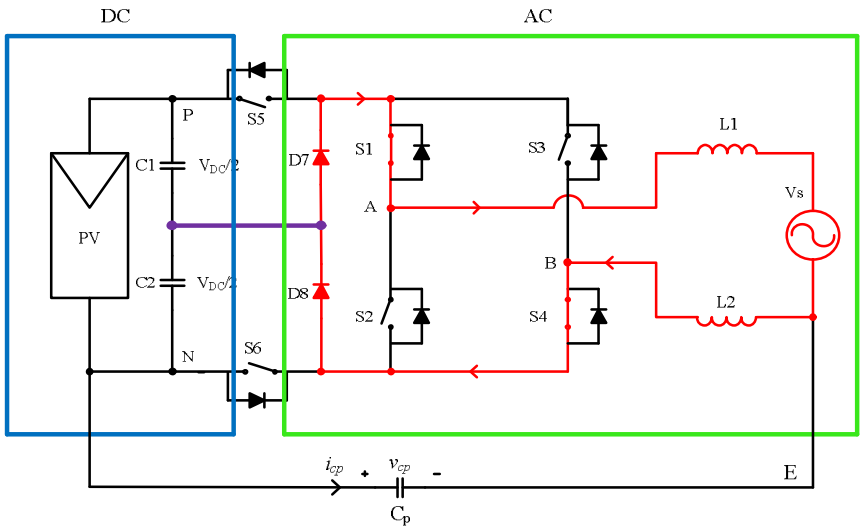


Figure 4.28 Illustration of DC bus midpoint connection (purple) of AC circuit (inverter side) of the topology in [52] at zero vector durations as a representative of ZVMC-GCTSI topologies.

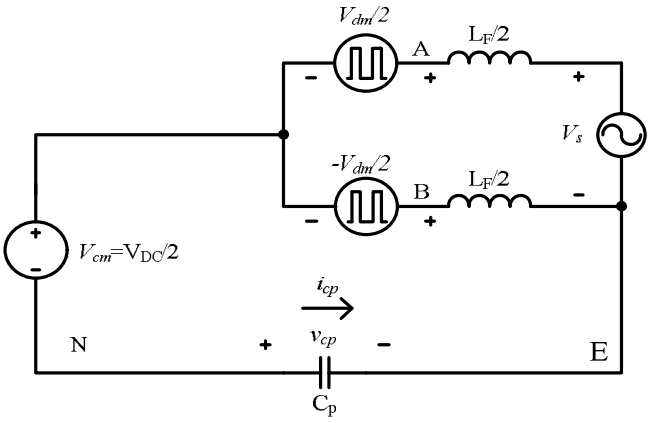


Figure 4.29 Equivalent circuit for leakage current evaluation of ZVMC-GCTSI topologies.

In Figure 4.30, the parasitic capacitor current of the topology in [52] is depicted for 500nF of parasitic capacitance case. Having constant CMV as in the case of H4 bipolar modulation, the leakage current in these class of inverter topologies becomes nearly same as the leakage current of H4 bipolar switching pattern (Figure 4.10). As compared to their ZVI-GCTSI counterparts, the leakage current in ZVMC-GCTSI topologies is significantly reduced in terms of the peak level (comparison based on Figures 4.25 and 4.30). However, in the application, the leakage current in ZVMC-GCTSI topologies is expected to have some high frequency content, due to non-ideal midpoint-connecting switch commutations, non-equal DC bus division and other parasitic effects to cause varying CMV.

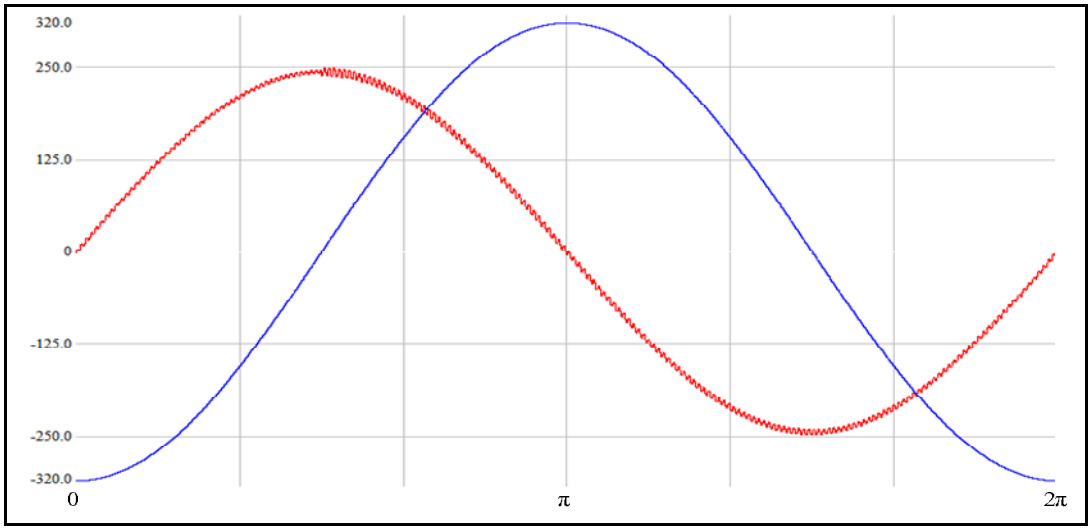


Figure 4.30 Illustration of grid voltage (V) (blue)and parasitic capacitor current (A) (red, scale; ×10000) of the topology in [52], as a representative of ZVMC-GCTSI topologies for C_p=500 nF.

4.4.5 Leakage Current Analyses and Simulation Results of ZVH-GCTSI Topologies

The third subclass of ZV-GCTSI topologies is the ZVH-GCTSI topology group. As the name suggests, the decoupling of AC and DC circuits of the ZVI-GCTSI topology class and the midpoint connection in the ZVMC-GCTSI class are used interchangeably (in every half grid cycle) in the third approach, which constitutes a hybrid characteristic. Furthermore, the equivalent circuit for leakage current study of ZVH-GCTSI topologies exhibits also a hybrid characteristic such that, the characteristic is composed of the characteristics of ZVI-GCTSI and ZVMC-GCTSI topologies interchangeably, depending on the polarity of the derivative of the grid voltage (dV_s/dt).

In Figure 4.31, as a representative of ZVH-GCTSI topologies, the PT-6 topology, and its grid voltage change dependent (dV_s/dt) equivalent circuit modes are illustrated. The diode D6 is always reverse biased at active vectors for unity power factor operation. When dV_s/dt is positive, D6 is also reverse biased and the topology operates as a ZVI-GCTSI topology for a half grid cycle. When dV_s/dt is negative, D6 is forward biased at zero vectors, therefore connecting the inverter side of the AC circuit to the midpoint of the DC bus as in the case of ZVMC-GCTSI topologies.

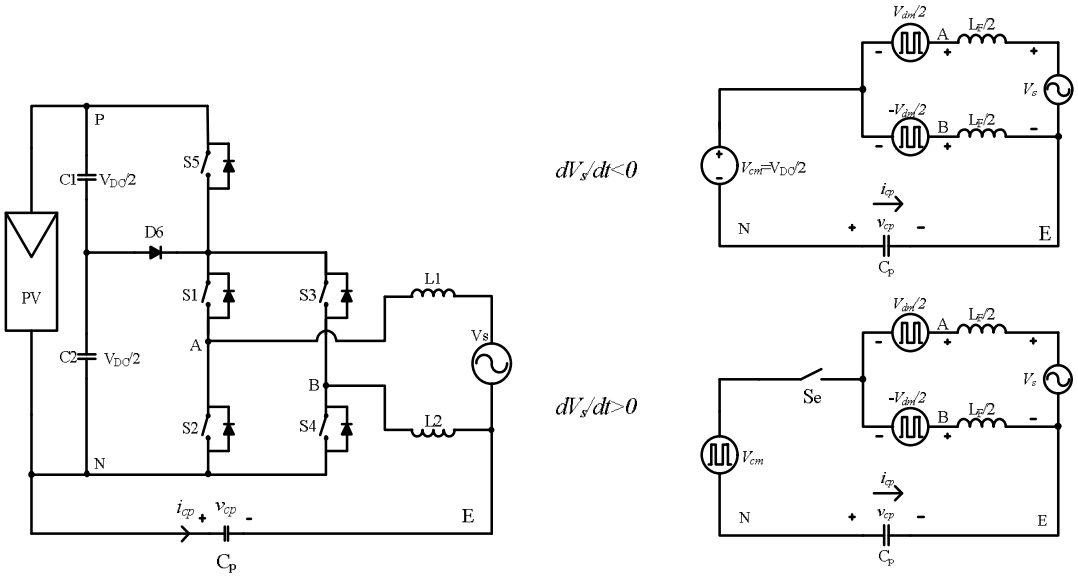


Figure 4.31 The proposed PT-6 topology (left) and its equivalent circuits (right) for leakage current study depending on the sign of the grid voltage change (dV_s/dt).

In Figure 4.32, the parasitic capacitor current of the PT-6 topology is depicted for 500nF of parasitic capacitance case as a representative of ZVH-GCTSI topologies. The leakage current characteristics of the PT-6 topology exhibit a hybrid characteristic as suggested. For $0 < \theta < \pi$ region, the topology behaves like a ZVI-GCTSI topology, whereas for $\pi < \theta < 2\pi$ interval, it acts like a ZVMC-GCTSI topology, constituting a hybrid characteristic in time.

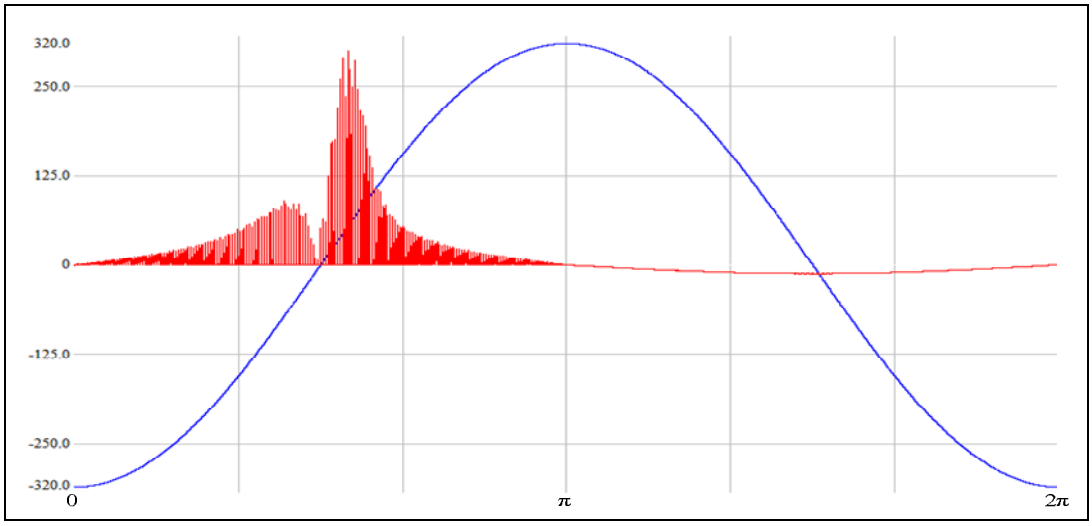


Figure 4.32 Illustration of grid voltage (V) (blue) and parasitic capacitor current (A) (red, scale; ×500) of the PT-6 topology, as a representative of ZVH-GCTSI topologies for C_p=500 nF.

4.4.6 Leakage Current Analyses and Simulation Results of SC-GCTSI Topologies

In SC-GCTSI topologies, the intention is to avoid leakage currents in the system by establishing a solid connection between the AC side (generally the neutral conductor as in the case for NPC derived topologies) and the DC bus side. In Figure 4.33, the equivalent circuit for the leakage current study in SC-GCTSI topologies is given. In this equivalent circuit, $V_{DC\text{-}c}$ represents the DC offset voltage due to DC bus voltage, and Z_{line} represents the clamped line impedance. The total of midpoint of the DC bus to earth clamping impedance (R+L+C) is denoted as Z_{clamp}. When one of these two impedances is absent, the leakage current becomes ideally zero. However, the line impedance is normally existent and the differential mode current may induce parasitic currents in the system. Moreover, any high frequency voltage appearing on the neutral line induces leakage currents. In Figure 4.34 the leakage current of the PT-9 topology at 3 kW is depicted for Z_{line}=50µH+10mΩ, Z_{clamp}=3µH+2mΩ+20µF, and C_p=500 nF parasitic capacitance, which is non-zero for non-

zero line impedance, non-zero clamping impedance or non-zero differential mode current. In Figure 4.35, the microscopic view of the leakage current is depicted for the aforementioned parameters. The relation between the grid current and the line impedance is seen in the figure such that the leakage current is induced in the form of a decaying sinusoid as the line current changes in time.

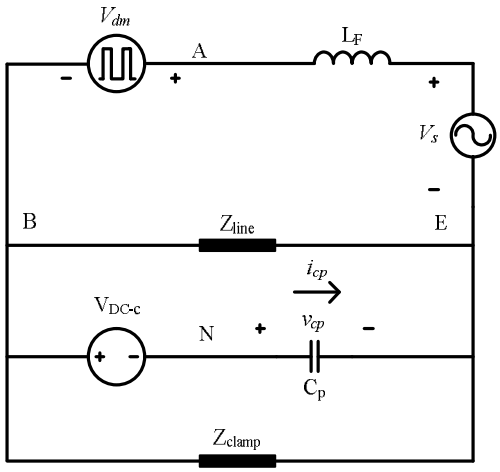


Figure 4.33 Equivalent circuit for leakage current evaluation of SC-GCTSI topologies.

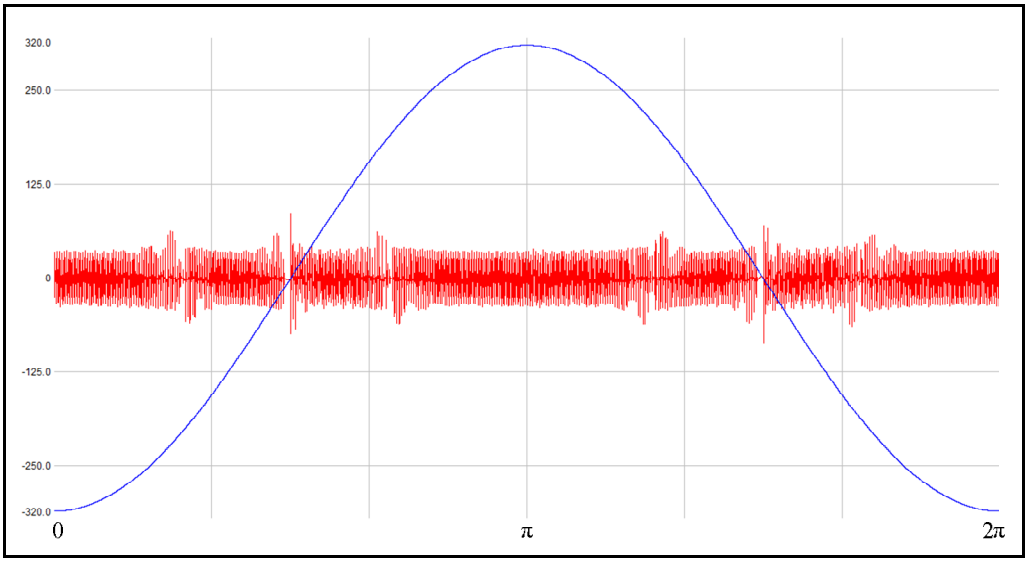


Figure 4.34 Illustration of grid voltage (V) (blue) and parasitic capacitor current (A) (red, scale; ×500) of the PT-9 topology, as a representative of SC-GCTSI topologies for Z_{line}=50μH+10mΩ, Z_{clamp}=3μH+2mΩ+20μF, and C_p=500 nF.

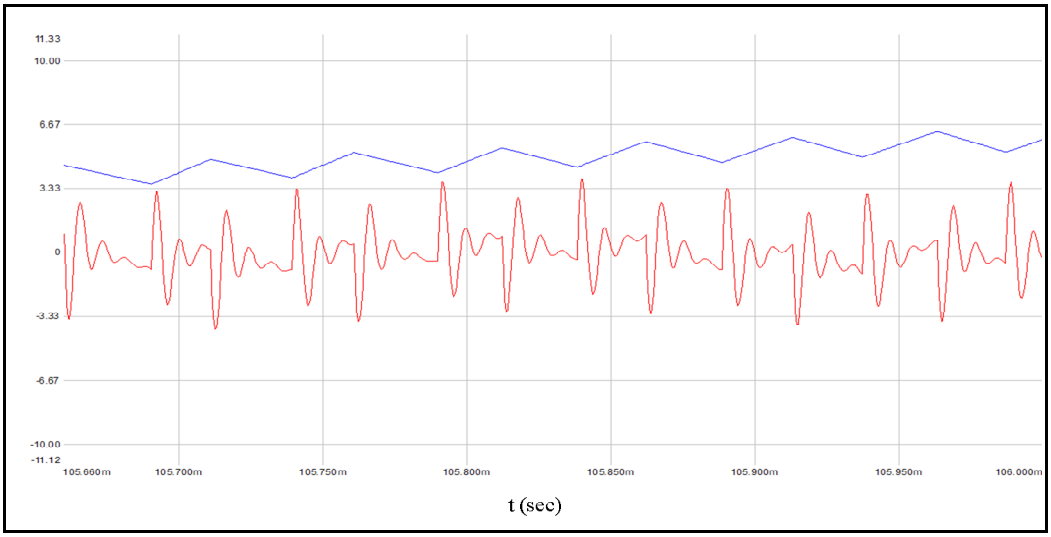


Figure 4.35 Illustration of line current (A) (blue) and parasitic capacitor current (A) (red, scale; ×50) of the PT-9 topology, as a representative of SC-GCTSI topologies for Z_{line}=50µH+10mΩ, Z_{clamp}=50µH+10mΩ+20µF, and C_p=500 nF.

4.4.7 Leakage Current Evaluation of GCTSI Topologies

In sections 4.4.2, the leakage current characteristics of ZVI-GCTSI topologies are investigated analytically and the simulation results are provided to verify the analyses. The source of the leakage current in these inverters is found to be the grid voltage variation rather than the CMV variation. Due to the grid voltage increase at zero vector durations, (while the AC grid and the DC circuits are decoupled) high peak leakage current may be encountered in these topologies, thus common mode filtering is required.

In section 4.4.4, ZVMC-GCTSI topologies are studied. As compared to ZVI-GCTSI topologies, the peak value of the leakage current is greatly reduced, such that the high frequency ripple content is absent in these topologies. However, in the application, it is expected that, due parasitic effects like short duration of CMV variation because of non-ideal commutation of the semiconductors, parasitic inductances on the DC bus-connecting layout or non-equal division of the DC bus voltage may induce a high frequency leakage current content. The high frequency content is expected to be low in magnitude and suppressible with a small CMI. In order to see the contributions of these effects on the leakage current accurately, experiments should be performed carefully.

The leakage current characteristics of ZVH-GCTSI topologies are studied in section 4.4.5. These topologies are found to exhibit the leakage current attributes of ZVI-GCTSI and ZVMC-GCTSI topologies interchangeably in time.

In section 4.4.6, SC-GCTSI topologies are investigated. The equivalent circuit for the leakage current study in these inverters is established pointing that a small part of leakage current may arise due to neutral conductor impedance and due to voltage oscillations on the neutral conductor.

In Table 4.3, the peak and the RMS values of the leakage current of the representative topologies (specified in the preceding sections) of each topology class are given for a parasitic capacitance of 500 nF and neutral conductor (and phase conductor) impedance of 50μH+10mΩ. The peak values of the leakage current in ZVI-GCTSI and ZVH-GCTSI topologies are nearly same as they have similar leakage current characteristics in certain time intervals. In ZVMC-GCTSI topologies, the peak value of the leakage current is greatly reduced as compared to ZVI-GCTSI and ZVMC-GCTSI topologies (the peak value of the leakage current is decreased 597 mA to 25 mA for the same parameters). This reduction in the leakage current is due to the midpoint connection at zero intervals thus ideally time-constant CMV is obtained on the inverter side. The RMS values of ZVI-GCTSI topologies appear to be highest among ZV-GCTSI topologies as expected. In ZVH-GCTSI topologies the RMS value of the leakage current is reduced due to ZVMC-GCTSI type operation for a half grid cycle. In ZVMC-GCTSI topologies, the RMS value is seen to be the smallest among all GCTSI topologies (17 mA). In three-phase application of ZV-GCTSI topologies, the leakage current characteristics are expected to be improved as the grid voltage change contribution on the leakage current can be almost eliminated due to balanced operation, which is to be investigated in the future.

In contrary to the leakage current characteristics of ZV-GCTSI topologies, the leakage current characteristics of SC-GCTSI are grid parameter dependent. For the same simulation parameters, the leakage current characteristics of PT-9, the representative of SC-GCTSI topologies, is found to reach 143 mA peak and 26 mA of RMS values. As the leakage current characteristics of these topologies are grid parameter and design dependent, the peak and RMS value measured in the simulations can change as with these parameters. The leakage current characteristics of the topology imply that, the design and the connection of

these inverters to the utility grid should be handled with great care in order to not to cross standard limitations and not to encounter the drawbacks of the high levels of leakage current.

Table 4.3 Peak and RMS values of leakage currents of representative GCTSI topologies for C_p=500 nF, Z_{line}=50μH+10mΩ at an output power of 3 kW (for SC-GCTSI topologies Z_{clamp}=3μH+2mΩ+20μF).

TOPOLOGY	*ZVI-GCTSI*	*ZVMC-GCTSI*	*ZVH-GCTSI*	*SC-GCTSI*
i_{cp} *(peak)*	*597 mA*	*25 mA*	*596 mA*	*143 mA*
i_{cp} *(RMS)*	*46 mA*	*17 mA*	*33 mA*	*26 mA*

4.5 Summary

In this chapter, the output voltage characteristics of GCTSI topologies are investigated to identify the effect of the number of output voltage levels on the filter inductor current ripple, since the ripple is highly correlated with the filter inductor sizing, and have considerable effects on the semiconductor and inductor losses. The topologies are grouped according to their number of output voltage levels and then the analyses and simulation results followed for the inductor current ripple evaluation. Then, the leakage current mechanisms of the subfamilies of GCTSI topologies are studied, and analytical approaches are established to identify the operation of the topologies under investigation. Simulation results are provided to verify analytical approaches made for GCTSI topologies throughout the chapter.

In the chapter, it is demonstrated that, in contrast to common knowledge, the source of leakage current in ZVI-GCTSI topologies is not the inverter CMV variation but grid voltage variation during zero vector states. The results obtained from the simulations are found highly correlated with the theory. In the simulations, it has been shown that the peak currents can exceed several hundred mA levels of standard limits (especially for large parasitic capacitor cases), thus common-mode filtering is required for the suppression of the peak currents in ZVI-GCTSI topologies. Moreover, the leakage current mechanisms for the equivalent circuits for ZVMC-GCTSI, ZVH-GCTSI, and SC-GCTSI topologies are identified and equivalent circuits for leakage current evaluation are established for these topologies. These equivalent circuits are useful in estimating the sources for the leakage

currents. The leakage current characteristics of GCTSI topologies are compared and inferences are made regarding the design and the grid connection of transformerless inverters. In order to verify the simulation and analytical study based conclusions in this chapter, realization of experimental verifications is vital.

CHAPTER 5

SEMICONDUCTOR EFFICIENCY CHARACTERIZATION OF ZVI-GCTSI TOPOLOGIES USING DATASHEET PARAMETERS

5.1 Introduction

Payback period, reliability, and heatsink volume (therefore size) are in high correlation with the efficiency characteristic of a PEC. Moreover, peak thermal stresses of semiconductors are the subject of high interest of recent few years, since the lifetimes of the devices are also correlated to the temperature stresses [61]. In order to obtain optimal switches and gate drive configuration for high efficiency, or in order to estimate junction, case, and heatsink temperature of a semiconductor at a given operating condition, it is vital to evaluate the power semiconductor losses in a given topology before implementing the hardware.

In a PEC, total losses consist of passive component losses (such as capacitor ESR losses, inductor core and copper losses etc.), and semiconductor losses (switching losses, conduction losses). In this chapter, power semiconductor losses are the focus as they are the major contributor to the losses and becoming an issue for the overall system reliability and lifetime. For the reliability and lifetime concerns, junction temperatures of power semiconductors can be estimated by thermal equivalent circuit models (analogy to electrical RC circuits) as in [62], [63] by estimating the semiconductor losses, where the former is out of the scope of the thesis, whereas the latter being investigated in detail in this chapter.

In power semiconductors, total losses are composed of conduction losses, switching losses, and blocking losses. Since they have very low levels of magnitude, blocking losses are normally neglected in general. Thus, power semiconductor losses can be investigated under two basic phenomena; conduction losses and switching losses. Considering this, sections 5.2-5.4 are devoted to the conduction and switching loss evaluation of MOSFET, IGBT, and diode, which are the basic power semiconductors of a PEC. The evaluation of conduction

losses in these sections are investigated based on the instantaneous power, whereas the evaluation of switching losses is based on switching energies of the semiconductors. The calculation of these losses is performed by making use of the semiconductor datasheet parameters. Several approximations are realized in the calculations for the sake of extrapolation of missing data from datasheets and for the facilitation of the calculation procedure, while preserving the accuracy.

In section 5.5, the procedure of the enfolding of conduction and switching losses as Average Power Per Switching Cycle (APPSC) for the efficiency characterization is described. Then, the switching constraints (voltage, current stresses, Current Duty Cycle Function (CDCF)) are studied as they appear in the enfolding procedure. In section 5.6, the results of semiconductor loss evaluation based on Calculated Average Power Per Switching Cycle (CAPPSC) method are presented. As investigated in chapter 3, there exists a vast variety of solar inverter topologies, therefore only the subgroup; ZVI-GCTSI topologies are studied in this chapter by means of efficiency characterization. Although the approach is applied only for ZVI-GCTSI topologies in this thesis, it can be extended to other PECs. A brief summary of the chapter is provided in section 5.7.

5.2 MOSFET Losses

MOSFET losses are comprised of conduction losses and switching losses. In the following two sections, the calculation of instantaneous conduction losses and the switching energies are presented successively.

5.2.1 MOSFET Conduction Losses

Being a majority carrier device, MOSFET conduction losses are resistive losses, i.e. they have no constant drain to source voltage drop even for a very small forward current as in the case of IGBTs and diodes. While a MOSFET is on (conducting), the conduction loss appears in the form of (5.1).

$$P_{M-C}(t) = {i_D}^2(t) \cdot R_{DS-ON}(i_D(t), V_{GS}, T_j) \tag{5.1}$$

where $P_{M-C}(t)$ is the instantaneous power dissipated during MOSFET conduction, $i_D(t)$ the drain current and $R_{DS-ON}(i_D(t), V_{GS}, T_j)$ the on-state resistance of the MOSFET. This resistance is a function of gate to source voltage (V_{GS}), drain current ($i_D(t)$), and junction temperature (T_j). The effect of gate to source voltage on the on-state resistance of the MOSFET is negligible after a conduction channel is established with exceeding the gate to source threshold voltage at a certain amount which is in the neighbourhood of 10 volts practically for most of the power MOSFETs. Similarly, as illustrated in Figure 5.1, the variation of MOSFET on-state resistance with drain current is low in magnitude, since the MOSFET is generally selected to be operated under this low R_{DS-ON} varying region. If this is not the case for a MOSFET to be used in the design, the ultimate on-state resistance for efficiency considerations can be taken as the average of the on-state resistance in the drain current operating region.

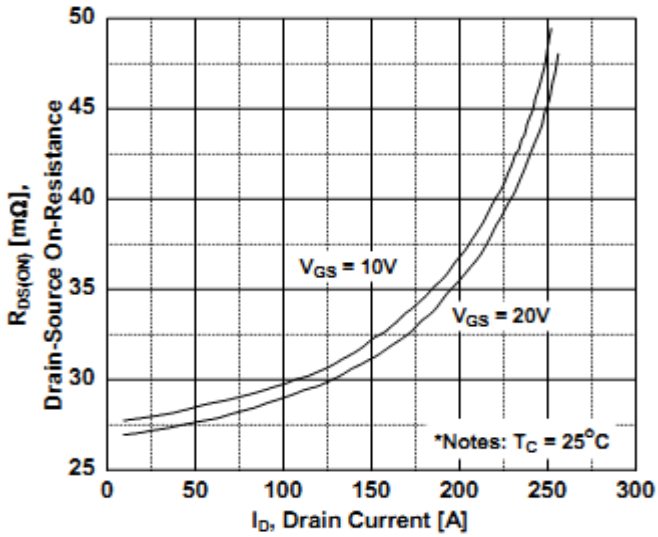


Figure 5.1 Drain current $i_D(t)$ vs. R_{DS-ON} variation of a commercial MOSFET [64].

Unlike the contribution of drain current and gate voltage after a threshold value, the junction temperature effect on R_{DS-ON} is considerable and should be taken into account for the operating junction temperature of the converter. The contribution of this temperature (T_j) can be read from the semiconductor datasheet (as illustated in Figure 5.2) which appears in the form of (5.2), where T_j is in Celcius degrees and taken constant during converter operation. Sometimes, on-state resistance versus junction temperature curves are given. If this is the case, below equation is still simply valid where the temperature coefficient is taken to be

unity at the temperature under investigation and the on-state resistance of the MOSFET read from the curve corresponding to this temperature.

$$R_{DS-ON}(T_j) = c(T_j) \cdot R_{DS-ON}(25^{\circ}C) \tag{5.2}$$

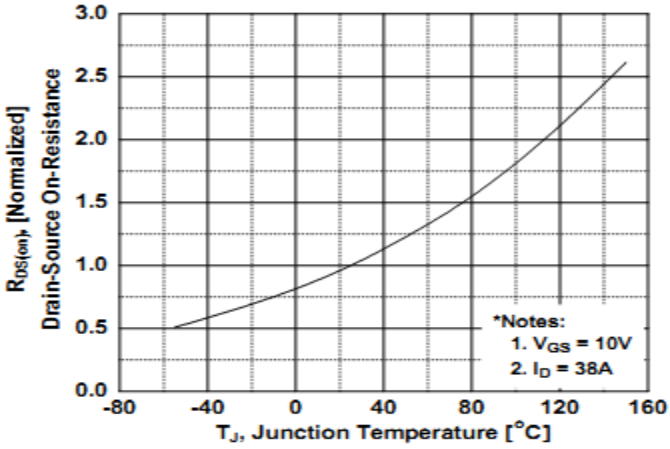


Figure 5.2 $R_{DS\text{-}ON}$ junction temperature scaling coefficient ($c(T_j)$) vs. junction temperature (T_j) curve obtained from MOSFET datasheet [64].

5.2.2 MOSFET Switching Losses

Switching losses of a semiconductor arise from the fact that the current/voltage rise/fall times are not ideally zero and moreover, the rising and falling events occurs while the other variable is nonzero (i.e. device current rise or fall occur at nonzero device voltage or vice versa). In the case of power MOSFETs, the current/voltage rise/fall durations are determined by how fast the parasitic capacitances are charged or discharged. In addition to the output capacitance (C_{oss}) of a power MOSFET, accompanying diode (shown in Figure 5.3, D_{acc}) reverse recovery charge (Q_{rr}) introduce additional switching losses which are not included in the rise and fall time based switching loss calculations, therefore these parts of switching losses of a MOSFET are added to the rise and fall time based switching losses.

Figure 5.3 illustrates the test circuit for the evaluation of switching losses of a MOSFET for an inductive load (which is the case for VSIs). In this figure, MOSFET parasitic capacitances are also illustrated in the dashed rectangle. In this circuit, I_D is MOSFET on-state drain current and V_{block} is MOSFET off-state blocking voltage.

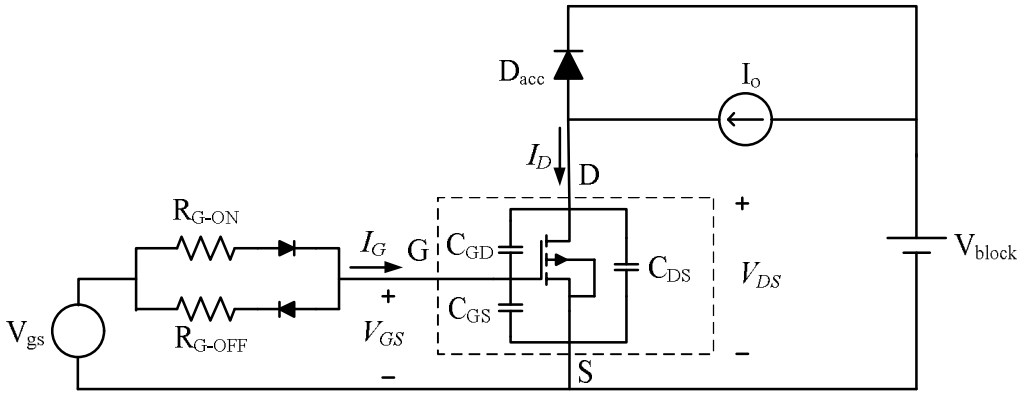


Figure 5.3 MOSFET switching test circuit illustrating the MOSFET parasitic capacitances.

In order to determine the switching energy of a MOSFET for specific off-state blocking voltage and on-state current (V_{block}, I_D) one must know current rise and fall times (t_{r-i} , t_{f-i}) and voltage rise and fall times (t_{r-v}, t_{f-v}). In [65], parasitic capacitance dependent voltage rise and fall time calculation by gate to drain capacitance by two point averaging overestimates the voltage rise and fall times (therefore switching losses) for high voltage power MOSFETs (600 V) due to drain to source voltage (V_{DS}) dependent nonlinear characteristics of gate to drain capacitance of power MOSFETs. In ref [66] and [67] a better approximation for rise and fall time calculation is obtained utilizing the specific gate charges, which are constant for a wide range of operating conditions and can be obtained from gate to source voltage (V_{GS}) vs. gate charge (Q_G) characteristics obtained from the datasheet of the device. An illustrative figure of this characteristic is depicted in Figure 5.4 from a commercial power MOSFET datasheet [64].

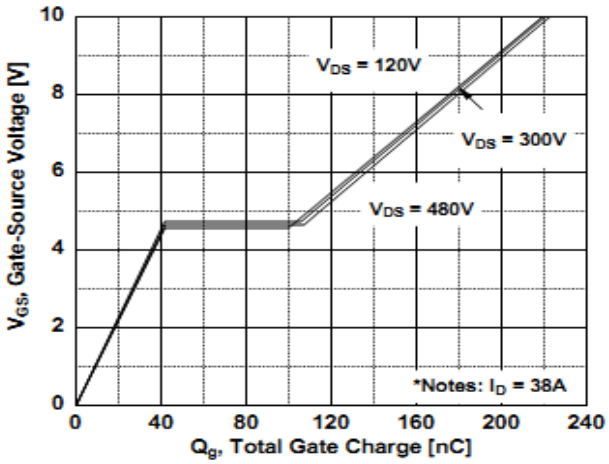


Figure 5.4 Typical total gate charge characteristics of a power MOSFET.

Having the (V_{GS}) vs. (Q_G) characteristics of a power MOSFET, one can easily adopt the turn-on and turn-off switching waveforms of a power MOSFET as illustrated in Figure 5.5.

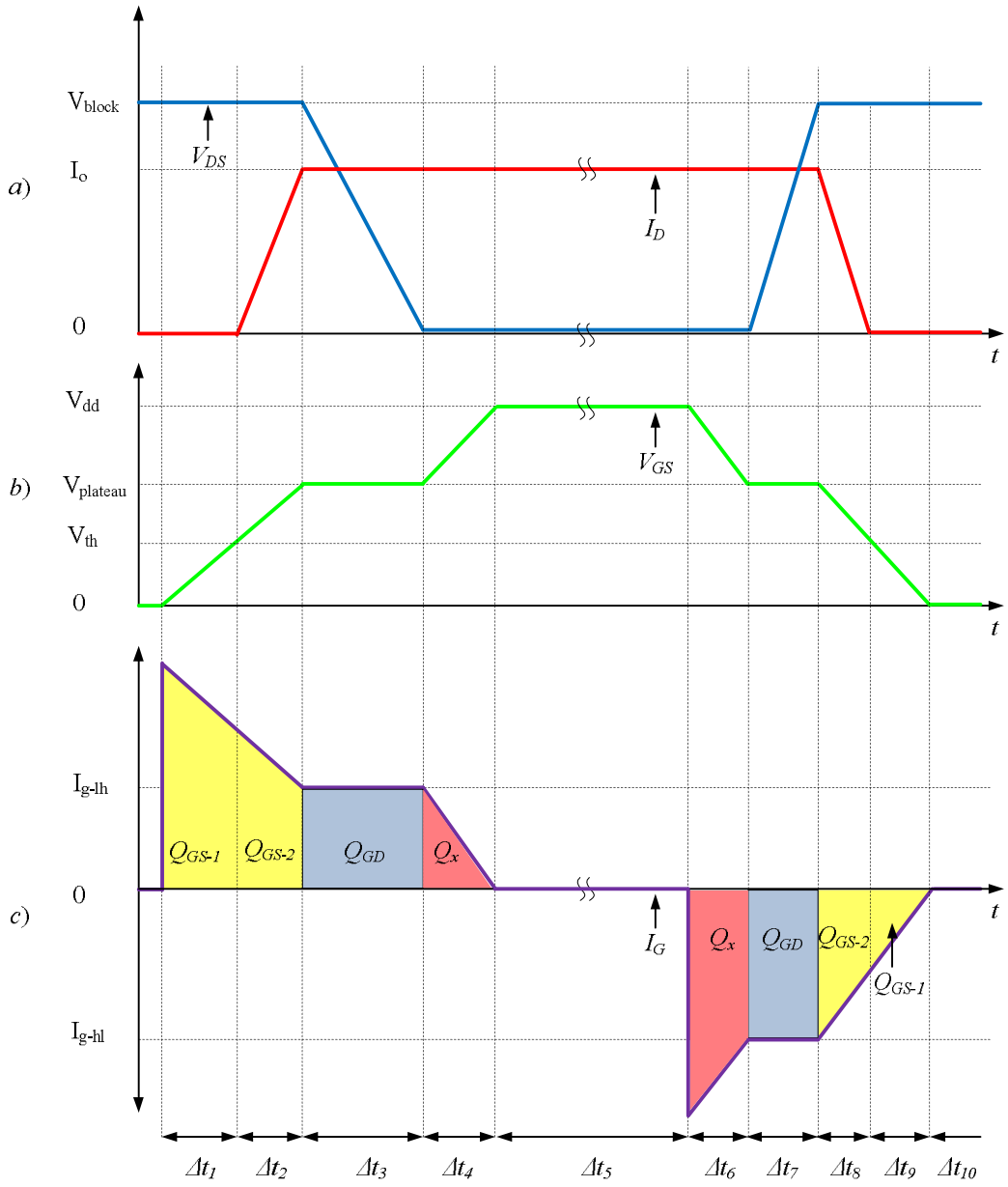


Figure 5.5 MOSFET switching characteristics a) Drain to source voltage and drain current, b) Gate to source voltage, c) Gate current.

In Figure 5.5.c, the gate current vs. time is illustrated. The area under the gate current is the gate charge. While the gate is charged or discharged, MOSFET drain to source voltage, MOSFET drain current, and gate voltage change accordingly (Figure 5.5.a, b). The gate

charges under gate current curve and the time intervals correspond to the events as summarized below.

Δt_1; In this interval, the gate charge (Q_{GS-1}) is supplied from the gate driver through turn on gate resistor (R_{G-ON}) for the MOSFET gate voltage (V_{GS}) to reach threshold voltage (V_{th}), which is the minimum voltage required for a MOSFET to start conduction.

Δt_2; In this interval, the gate is continued to be charged until the gate voltage reaches the plateau voltage ($V_{plateau}$). The charge supplied in this interval is (Q_{GS-2}) required to increase the gate voltage from threshold voltage (V_{th}) to plateau voltage. The MOSFET drain current (I_D) starts to increase and reaches the output current. Therefore, this period can also be labelled as the current rise interval(t_{r-i}).

Δt_3; After the gate voltage reaches to the plateau voltage ($V_{plateau}$), the gate to drain capacitance (C_{GD}) starts to be discharged by the gate driver; therefore, the MOSFET drain to source voltage (V_{DS}) drops nearly to its on-state level. This period can also be named as voltage fall time(t_{f-v}), and the charge required to discharge the gate to drain capacitance is named as (Q_{GD}).

Δt_4; After the MOSFET drain to source voltage (V_{DS}) falls, the gate voltage is further increased to its driver's peak level to decrease MOSFET on-state resistance. The charge required to achieve this operation is named hereby as (Q_x).

Δt_5; In this interval the MOSFET is fully conducting and the gate current is zero, therefore no switching loss appears in this interval as in the case of Δt_4.

Δt_6; In this interval, the steps during MOSFET turn-on are initiated to be realized in reverse order. In this period, the gate voltage is decreased from the driver peak level (V_{dd}) to the plateau voltage ($V_{plateau}$).

Δt_7; Similar to Δt_3, while the gate voltage stays at ($V_{plateau}$) the drain to source voltage (V_{DS}) increase to its blocking voltage (V_{block}) in this period (t_{r-v}).The charge removed from the gate to drain capacitance (C_{GD}) is the same as the charge in Δt_3 (Q_{GD}).

Δt_8; Within this period, (V_{GS}) continues to fall and this interval ends up by reaching the threshold voltage of the MOSFET. At the end of this period, MOSFET is not conducting any more i.e. the current is falls completely in this period (t_{f-i}).

Δt_9; In order to guarantee off-state operation (V_{GS}) voltage should be as low as possible in order to prevent unintentional conduction. This period is necessary to pull down the gate voltage to minimum (generally zero) of gate drive voltage.

Δt_{10}; This is the interval that any current flows neither from the gate nor the drain i.e. the MOSFET is off.

Having the gate charge approach, gate drive currents, and gate drive current dependent rise and fall times can be approximated as in (5.3) and (5.4) respectively.

$$t_{r-i} + t_{f-v} = \Delta t_2 + \Delta t_3 = \frac{Q_{G-SW}}{I_{G-ON}} \tag{5.3}$$

$$t_{r-v} + t_{f-i} = \Delta t_7 + \Delta t_8 = \frac{Q_{G-SW}}{I_{G-OFF}} \tag{5.4}$$

where;

$$Q_{G-SW} = Q_{GS2} + Q_{GD} \tag{5.5}$$

$$I_{G-ON} = \frac{V_{DD} - V_{plateau}}{R_{G-ON}} \tag{5.6}$$

$$I_{G-OFF} = \frac{V_{plateau}}{R_{G-OFF}} \tag{5.7}$$

R_{G-ON} and R_{G-OFF} are gate turn-on and turn-off resistances respectively (depicted in Figure 5.3). Using the rise and fall times, main part of MOSFET switching energy, which is due to rise and fall times($E_{M-SW-r-f}$), can be obtained as in (5.8).

$$E_{M-SW-r-f} = \frac{1}{2} V_{block} I_o \left(t_{r-i} + t_{r-v} + t_{f-i} + t_{f-v}\right) \tag{5.8}$$

In addition to the switching losses due to rise and fall times, there exist other losses such as output capacitance and reverse recovery losses, which have comparably and typically less contribution to the MOSFET switching losses. The output capacitance (C_{OSS}) is the sum of the gate to drain capacitance (C_{GD}) and drain to source capacitance (C_{DS}) (5.9). At every MOSFET turn-on, the charge stored on C_{oss} is discharged through the MOSFET resistive channel and the energy ($E_{M-SW-C-OSS}$) is converted to heat (5.10).

$$C_{OSS} = C_{DS} + C_{GD} \tag{5.9}$$

$$E_{M-SW-COSS} = \frac{1}{2} C_{oss} {V_{block}}^2 \tag{5.10}$$

In addition to these, reverse recovery current of accompanying freewheeling diode (D_{acc}) causes additional switching losses on the MOSFET during MOSFET turn-on and the switching loss contribution to the MOSFET can be obtained as in (5.11).

$$E_{M-SW-Q-rr} = V_{block} Q_{rr} \tag{5.11}$$

Accumulating the aforementioned main parts, total switching losses of a power MOSFET becomes as in (5.12).

$$\begin{aligned} E_{M-SW} &= E_{M-SW-r-f} + E_{M-SW-C-OSS} + E_{M-SW-Q-rr} \\ &= \frac{1}{2} V_{block} I_D \left(t_{r-i} + t_{r-v} + t_{f-i} + t_{f-v}\right) + \frac{1}{2} C_{oss} {V_{block}}^2 + V_{block} Q_{rr} \end{aligned} \tag{5.12}$$

MOSFET switching energy can also be adjusted to operating conditions, in a manner similar to the case of MOSFET conduction losses, i.e. either the parameters that are required should be read at the temperature under investigation or scale factors for each component should be used to yield more approximate results.

5.3 IGBT Losses

IGBT losses are mainly composed of conduction and switching losses as in the case of MOSFETs. Blocking losses and gate drive losses are normally neglected as their contribution to losses are very low (in the order of mW). Low gate drive current and better switching performance with respect to BJTs using MOSFET gate structure, and higher

current and voltage handling capability with respect to MOSFETs using BJT structure (shown in Figure 5.6) made IGBTs attractive for most of applications [68]. Up to 4-5 kW, IGBTs are the choice for low frequency switches requiring fast anti-parallel diode, due to slow intrinsic body diode of MOSFETs. After 4-5 kW, IGBTs are good choice for all controlled switches due to their nearly constant voltage drop as explained in the next section.

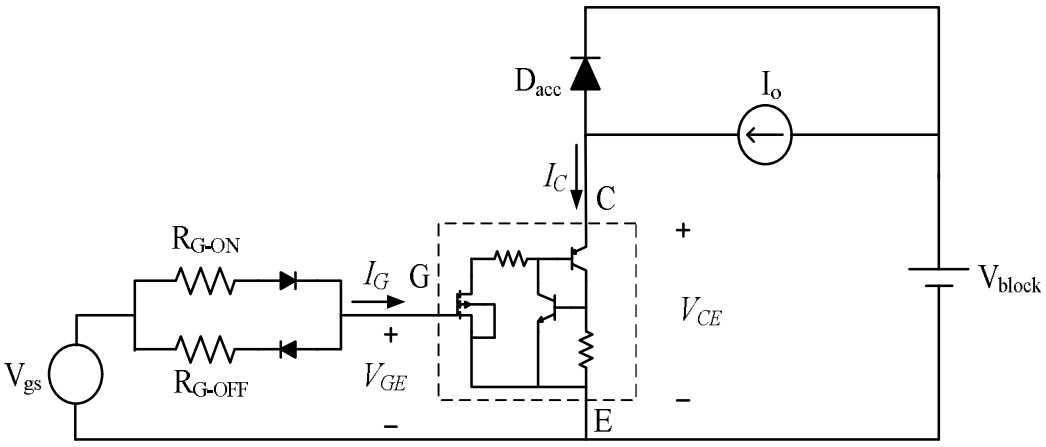


Figure 5.6 IGBT switching test circuit illustrating the BJT structure.

5.3.1 IGBT Conduction Losses

Unlike MOSFET conduction, IGBTs have a P-N junction voltage drop even at low currents. In spite of such characteristics, IGBTs exhibit better efficiency at higher power levels (greater than 4-5 kW), since their on-state resistance is much lower than MOSFET on-state resistance. In order to evaluate conduction loss of an IGBT, V_{CE} characteristics of the IGBT can be approximated as shown in Figure 5.7 [69], and the instantaneous conduction loss can be calculated as in (5.13).

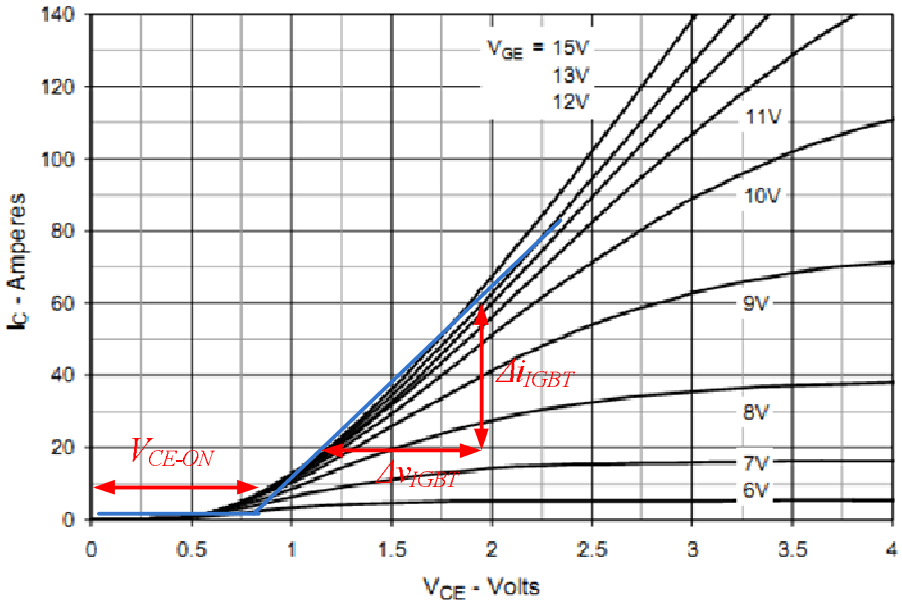


Figure 5.7 An illustration of on-state voltage of an IGBT vs. its collector current [69].

$$P_{IGBT-C}(t) = i_C(t) \cdot V_{CE-ON} + {i_C}^2(t) \cdot R_{CE-ON} \tag{5.13}$$

where $i_C(t)$ is the collector to emitter current, V_{CE-ON} is the constant p-n junction voltage drop of the IGBT and R_{CE-ON} is the on-state equivalent resistance of the device as described in (5.14) and the incremental collector current (Δi_{IGBT}) and collector to emitter voltage (Δv_{IGBT}) illustrated in Figure 5.7.

$$R_{CE-ON} = \frac{\Delta v_{IGBT}}{\Delta i_{IGBT}} \tag{5.14}$$

5.3.2 IGBT Switching Losses

As compared to MOSFETs, IGBT switching losses are easier to evaluate, since these losses are generally given in datasheets. If the IGBT under interest has a built-in diode, the reverse recovery losses may also be included in the given datasheet collector current (I_C) vs. turn-on switching energy (E_{ON}) curve. Similarly, collector current (I_C) vs. turn-off switching energy (E_{OFF}) curves are usually provided in datasheets. These curves are generally provided for a specific gate resistor, temperature and blocking voltage constraints (Figure 5.8, [69]). This curve can be accurately approximated with minimum error power polynomial approach. If the switching conditions are not the same as in the curve provided, gate resistor and junction

temperature scale factors for turn-on and turn-off events can be evaluated from E_{ON} vs. R_G and E_{ON} vs. T_j curves (as seen from Figure 5.9, [69]) and making use of (5.15-5.18). These factors can be used to scale E_{ON} vs. I_C and E_{OFF} vs. I_C curves (i.e. the coefficients of obtained polynomials) to yield more accurate results. Similar to these, blocking voltage (V_{block}) scale factor can be used to estimate turn-on and turn-off switching energies as in (5.19) correctly at the blocking voltage under interest. The final turn-on and turn-off switching energy scale factor can be evaluated as in (5.20) and (5.21). The semiconductor datasheets neither cover four-dimensional (E_{ON}, I_C, T_j, R_G) curves, nor do they provide the datasets. Thus, these scale factors can be used to reflect the effects of switching conditions on turn-on and turn-off energy losses.

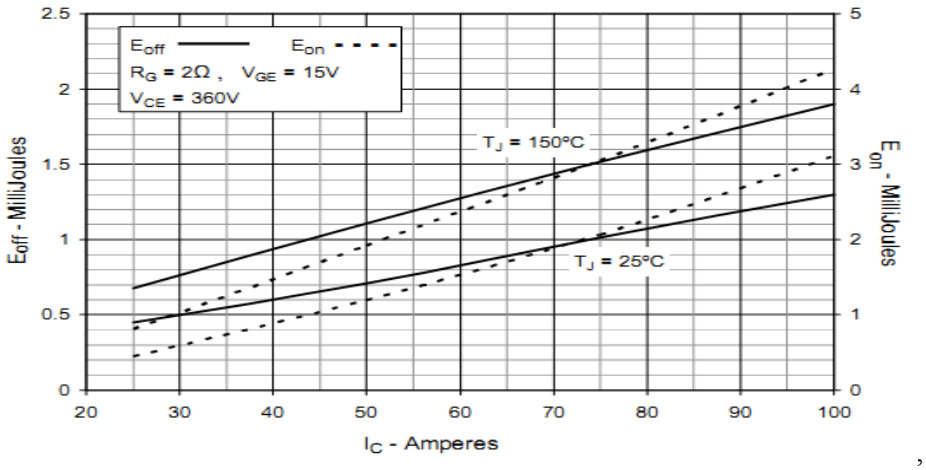


Figure 5.8 I_C vs. E_{ON} and I_C vs. E_{OFF} characteristics of a commercial IGBT including diode recovery losses.

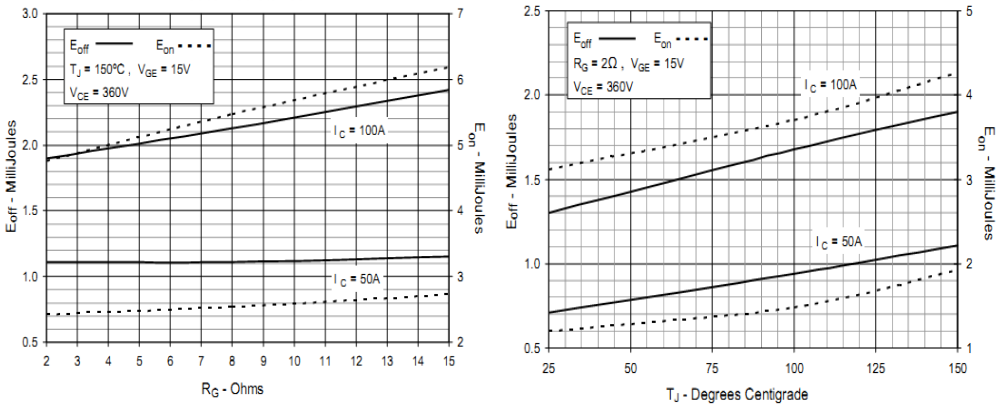


Figure 5.9 E_{ON} and E_{OFF} vs. gate resistance and junction temperature curves used for obtaining scale factors for different operating conditions (i.e. different gate resistance and temperature).

$$S_{f-RG-ON} = E_{ON}(R_{G-i})/E_{ON}(R_{G-t}) \tag{5.15}$$

$$S_{f-RG-OFF} = E_{OFF}(R_{G-i})/E_{OFF}(R_{G-t}) \tag{5.16}$$

$$S_{f-Tj-ON} = E_{ON}(T_{j-i})/E_{ON}(T_{j-t}) \tag{5.17}$$

$$S_{f-Tj-OFF} = E_{OFF}(T_{j-i})/E_{OFF}(T_{j-t}) \tag{5.18}$$

$$S_{f-Vblock} = V_{block-i}/V_{block-t} \tag{5.19}$$

$$S_{f-ON} = S_{f-RG-ON} \times S_{f-Tj-ON} \times S_{f-Vblock} \tag{5.20}$$

$$S_{f-OFF} = S_{f-RG-OFF} \times S_{f-Tj-OFF} \times S_{f-Vblock} \tag{5.21}$$

where $S_{f-RG-ON}$ is the turn-on gate resistor scale factor, $S_{f-RG-OFF}$ is the turn-off gate resistor scale factor, $S_{f-Tj-ON}$ is the turn-on junction temperature scale factor, $S_{f-Tj-OFF}$ is the turn-off junction temperature scale factor, $S_{f-Vblock}$ is blocking voltage scale factor, S_{f-ON} is the final turn-on scale factor, S_{f-OFF} is the final turn-off scale factor. Moreover, $E_{ON}(R_{G-i})$ is the turn-on energy at the gate resistance under interest, $E_{OFF}(R_{G-i})$ is the turn-off energy at the gate resistance under interest, $E_{ON}(R_{G-t})$ is the turn-on energy at the test gate resistance of E_{ON} vs. I_C curve, and $E_{OFF}(R_{G-t})$ is the turn-off energy at the test gate resistance of E_{OFF} vs. I_C curve. $E_{ON}(T_{j-i})$ and $E_{OFF}(T_{j-i})$ are the turn-on, turn-off energy values at the junction temperature under interest and $E_{ON}(T_{j-t})$, $E_{OFF}(T_{j-t})$ are the turn-on, turn-off energy values respectively at the junction temperature which E_{ON} vs. I_C and E_{OFF} vs. I_C curves are obtained at. With the scale factors obtained, one can easily scale the turn-on switching energy polynomial coefficients and turn-off switching energy polynomial coefficients obtained from the datasheet with datasheet junction temperature, blocking voltage and datasheet gate resistance to the conditions under interest as in (5.22) and (5.23).

$$\mathbf{Z_{E-ON}} = S_{f-ON} \cdot \mathbf{Z_{E-ON-t}} \tag{5.22}$$

$$\mathbf{Z_{E-OFF}} = S_{f-OFF} \cdot \mathbf{Z_{E-OFF-t}} \tag{5.23}$$

where $\mathbf{P_{E-ON-t}}$ is the approximated turn-on energy vs. collector current curve polynomial coefficient vector to be scaled by final turn-on scale factor to polynomial coefficient vector of the conditions under interest $\mathbf{Z_{E-ON}}$, $\mathbf{Z_{E-OFF-t}}$ is the approximated turn-off energy vs. collector current curve polynomial coefficient vector to be scaled by final turn-on scale factor to polynomial coefficient vector of the conditions under interest $\mathbf{Z_{E-OFF}}$.

5.4 Diode Losses

Similar to the case for the MOSFETs and IGBTs, diode losses consist of conduction and switching losses. In spite of the fact that, conduction losses are dominant in diodes, the reverse recovery charge characteristics of the diodes greatly affects the performance of a PEC. The following two sections provide the instantaneous calculation of diode conduction losses and the diode switching losses successively.

5.4.1 Diode Conduction Losses

Diode conduction losses can be calculated quite similar to IGBT conduction losses. Since these semiconductors are minority carrier devices a p-n junction voltage drop is present in both of these devices. The approximation to typical diode forward current vs. on-state voltage drop can be made as in Figure 5.10 and the approximation dependent instantaneous conduction losses can be formulated as in (5.24) similar to the case for the IGBT.

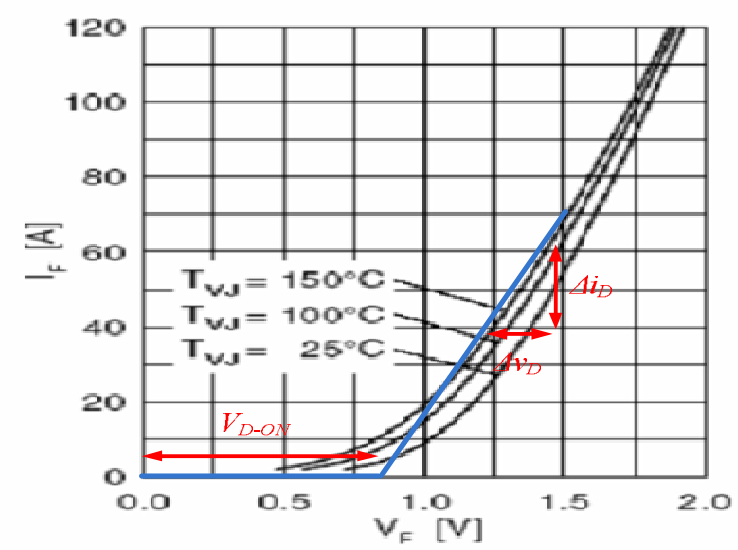


Figure 5.10 An illustrative on-state voltage drop of a diode vs. its forward current.

$$P_{D-C}(t) = i_F(t) \cdot V_{D-ON} + {i_F}^2(t) \cdot R_{D-ON} \tag{5.24}$$

where $i_F(t)$ is the diode forward current, V_{D-ON} is the constant p-n junction voltage drop of the diode and R_{D-ON} is the on-state equivalent resistance of the device as described in (5.25). The incremental collector current (Δi_D) and collector to emitter voltage (Δv_D) can be obtained as in Figure 5.10.

$$R_{D-ON} = \frac{\Delta v_D}{\Delta i_D} \tag{5.25}$$

5.4.2 Diode Switching Losses

Unlike in the cases of MOSFETs and IGBTs, turn-on switching losses of a diode are usually neglected since the diode forward voltage drops to its on-state level is achieved very quickly. Thus, diode switching losses can be reduced to only turn-off losses, which is composed of nothing but the reverse recovery losses.

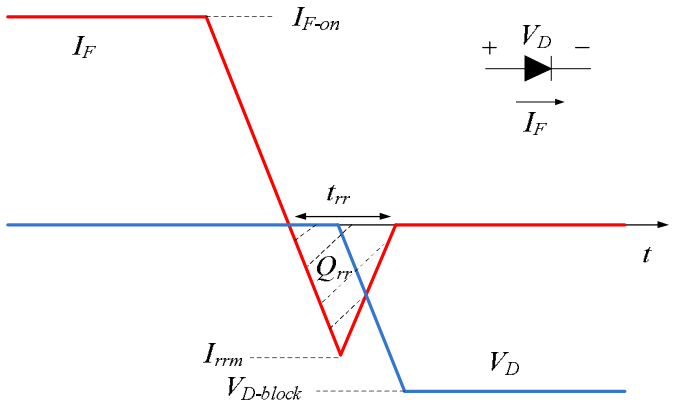


Figure 5.11 Typical diode turn-off current and diode turn-off voltage behaviour.

Figure 5.11 illustrates a typical turn-off current and voltage of a diode. Using these typical waveforms, the switching loss energy during reverse recovery time (t_{rr}) can be approximated as in (5.26).

$$E_{D-SW} = \frac{V_{D-block} \cdot Q_{rr}(I_{F-ON}, dI_F/dt)}{4} \tag{5.26}$$

where E_{D-SW} is the diode turn-off energy, $V_{D-block}$ is the diode blocking voltage at the switching period and $Q_{rr}(I_{F-ON}, dI_D/dt)$ is the diode reverse recovery charge, which is diode on-state current (I_{F-ON}) and diode current fall derivative (dI_F/dt) dependent as shown in Figure 5.12. This dependence is empirically formulated as in (5.27).

$$Q_{rr}(I_{F-ON}, dI_F/dt) = Q_{rr-t} \cdot \frac{dI_{F-i}/dt}{dI_{F-t}/dt} \cdot \sqrt{\frac{I_{F-ON-i}}{I_{F-ON-t}}} \tag{5.27}$$

where Q_{rr-t} is the reverse recovery charge read from datasheet, dI_{F-i}/dt is the diode current fall derivative under interest, dI_{F-t}/dt is the diode current fall derivative at the test conditions of Q_{rr-t} , I_{F-ON-i} is the on-state diode current under interest and I_{F-ON-t} is the on-state diode current under test conditions of Q_{rr-t}.

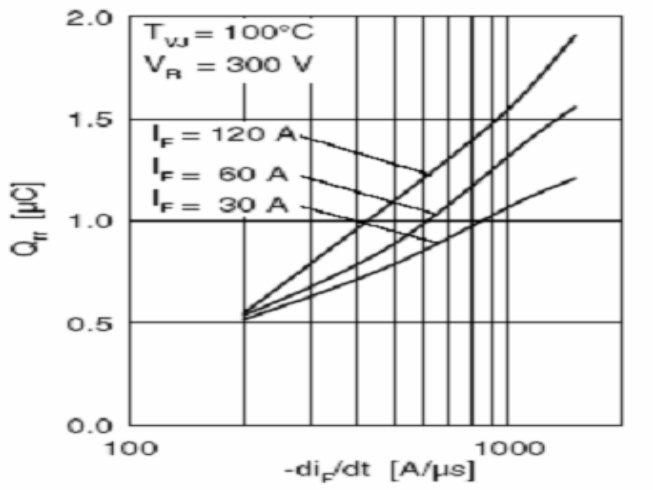


Figure 5.12 An example of reverse recovery charge (Q_{rr}) vs. diode current fall derivative (dI_F/dt) curve.

Although the reverse recovery switching losses dissipated both on the diode itself and the accompanying MOSFET are low in magnitude, its effects may be harmful to the diode and the controlled switch parallel to the diode if it exists, due to the leakage inductances present on the devices and the layout causing voltage overshoots.

5.5 Calculated Average Power Per Switching Cycle (CAPPSC) Method

In order to adapt the aforementioned switching losses and the instantaneous conduction losses of the semiconductors for the efficiency characterization, the CAPPSC method is

used. In this method, first, conduction and switching losses of each power semiconductor are calculated at each switching cycle and enfolded as Average Power Per Switching Cycle (APPSC) for a complete grid period. In Figure 5.13, these enfolding operations for each semiconductor type are depicted as blocks. The blocks are named according to their functions. For instance, the block that MOSFET conduction losses are calculated for a grid period is labelled as MCLCB (MOSFET Conduction Loss Calculation Block). Similar assignment is valid for switching losses and for other power semiconductor types (IGBTs and diodes). Shown in the figure, each block takes concerning Semiconductor Parameters (SP) and Switching Constraints (SC) and outputs CAPPSC of corresponding power semiconductor for a full grid period. The procedure of enfolding operation is detailed in section 5.5.1, and the SC is investigated in section 5.5.2.

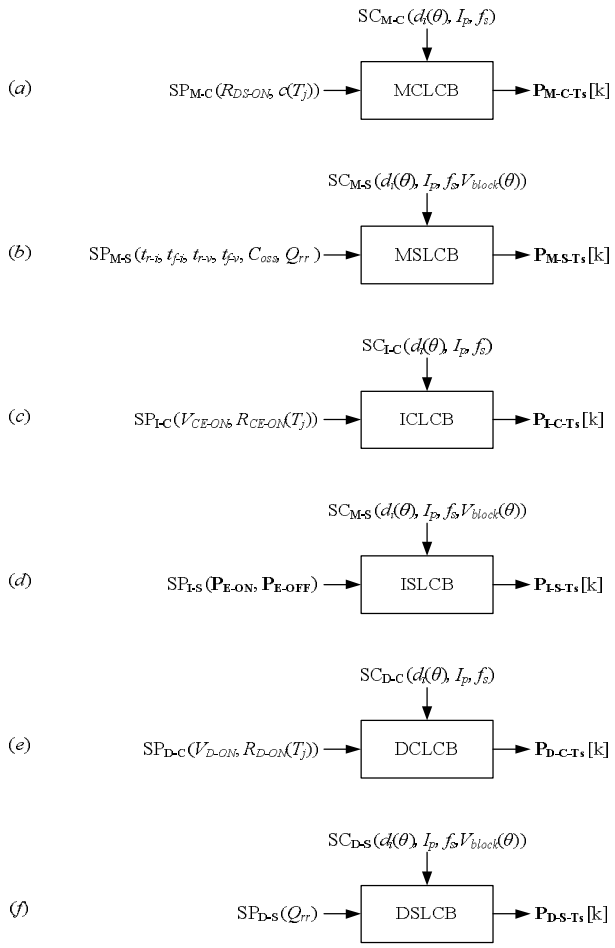


Figure 5.13 Representative blocks for switching and conduction loss calculation of MOSFETs (*a*, *b*), IGBT (*c*, *d*), and diode (*e*, *f*) for a full grid period (i.e. the output vectors containing corresponding losses in terms of APPSC for each switching event at a complete grid cycle).

By making use of the outputs of loss calculation blocks in Figure 5.13, semiconductor efficiency of a topology with respect to loading can be obtained. In Figure 5.14, the algorithm for the efficiency characterization is depicted. After determining the SP and SC for each power semiconductor from datasheets and from topology switching pattern, the loss contribution of each power semiconductor (with the index being x) can be obtained with respect to the loading index, i (i=1 corresponds to 1% loading, i=100 corresponds to full loading). For all power semiconductor devices (i.e. x=1 to x_{max}), the loss contribution at any loading index are calculated and added, thus, total power semiconductor losses are calculated at each loading level. Having the power semiconductor losses at each i, the efficiency vector (with respect to loading index) can be calculated easily. For the loss calculation blocks, the peak current is updated as the loading index i is increased. It is noticeable that, the output vectors of loss calculation blocks are one-dimensional but they are extended to two dimensions to obtain APPSC losses with respect to time and loading.

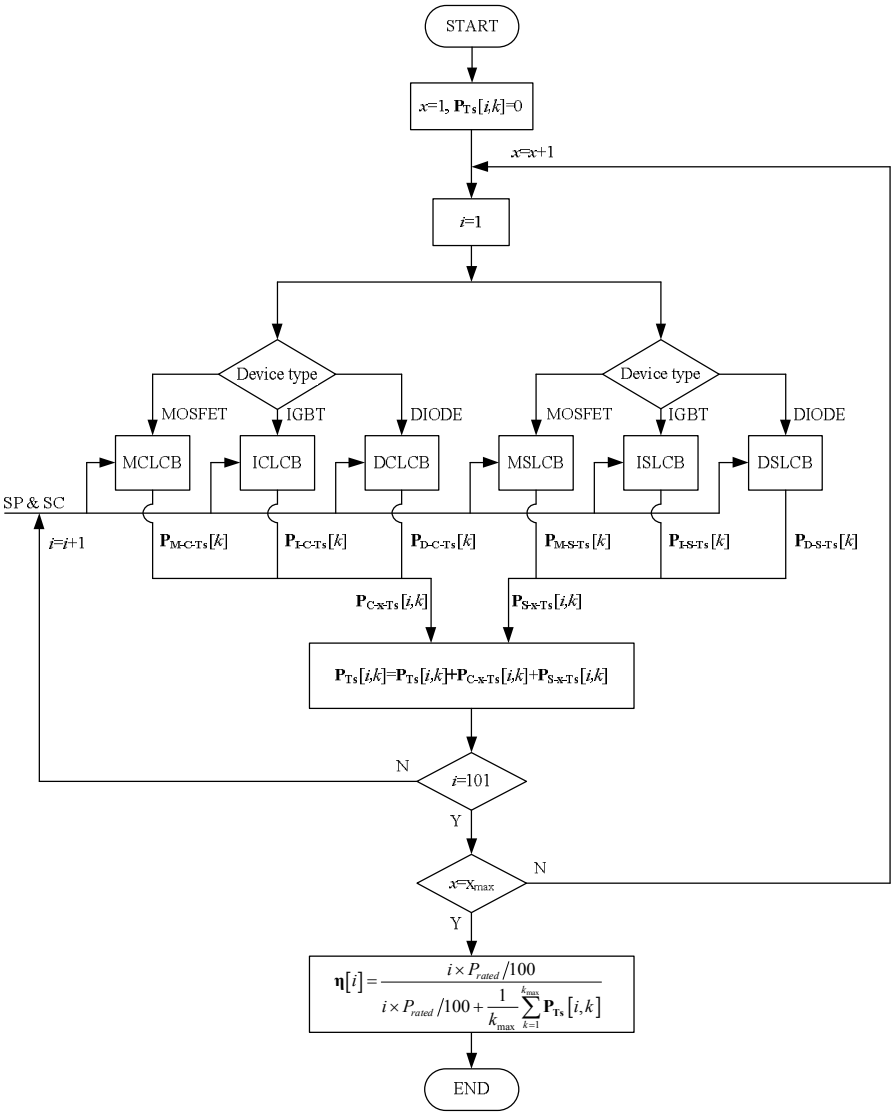


Figure 5.14 The algorithm for the semiconductor efficiency characterization of a PEC for various percent loadings (*i* being the loading index, *x* being the device index).

5.5.1 Enfolding of Instantaneous Conduction and Switching Losses in the Form of APPSC

The outputs of the loss calculation blocks (in Figure 5.13) are in the form of APPSC. Therefore, it is necessary to enfold the instantaneous losses. In order to perform enfolding operation, grid cycle is divided into the portions each having a time length of the switching period (T_s). The integrals of the switching and conduction losses at each switching period are averaged over the switching period, therefore the enfolded loss elements appear as averaged power. The enfolding operation is realized for each switching period, with the time index *k*,

meaning that for 50 Hz of grid frequency, the enfolding operation is performed for $k \in \{0,1,2,\ldots k_{max}\}$ where

$$k_{max} = \begin{cases} [\![0.02/T_s]\!]+1 & \text{if } 0.02/T_s \text{ is integer} \\ [\![0.02/T_s]\!] & \text{otherwise} \end{cases} \tag{5.28}$$

The approach for the quantization of semiconductor losses can be visualized as in Figure 5.15. In the figure, the line current and the reference line current can be seen in (*a*). In (*b*), the voltage and current of a power semiconductor is depicted. In (*c*) and (*e*), the instantaneous switching and conduction power losses of the semiconductor are illustrated respectively. In (*d*) and (*f*) the APPSC of the switching and the conduction losses of the power semiconductor are illustrated respectively.

Having time index *k*, the power semiconductor losses can be calculated, quantized and stored in the form of APPSC for each *k* as described in subsequent two sections for the conduction losses and for the switching losses. The CAPPSC approach is as accurate as the switching frequency is many times higher than the grid frequency, therefore the line current can be taken constant at a switching cycle.

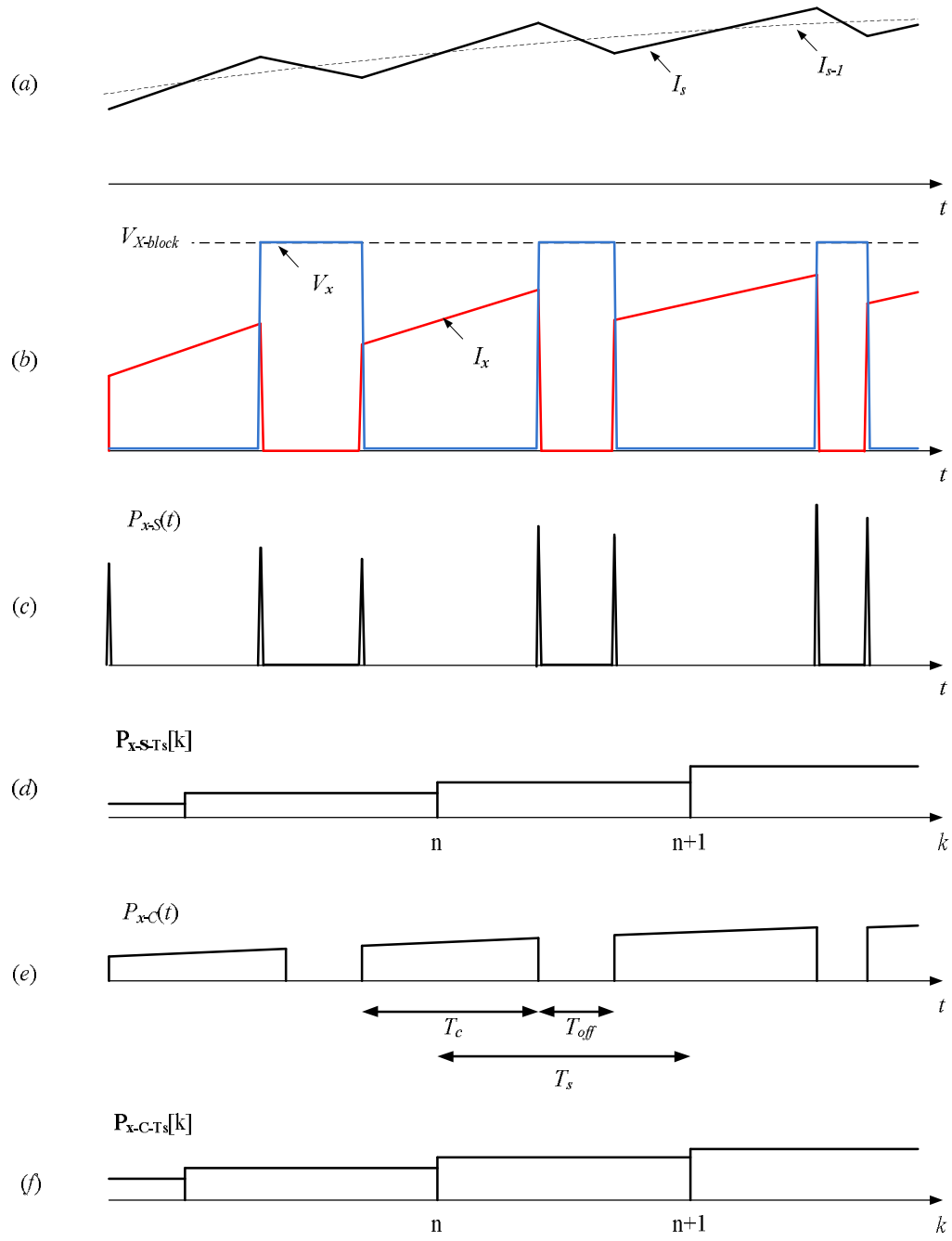


Figure 5.15 Illustration of enfolding of conduction and switching losses, *x* stands for the device index.

5.5.1.1 Enfolding Conduction Losses

The time domain expressions for the conduction losses for MOSFETs, IGBTs and diodes are given (5.1), (5.13), and (5.24) respectively. Having the APPSC approach, these expressions

for time domain calculation of conduction losses can be combined with (5.29) to enfold the conduction losses.

$$\mathbf{P}_{\mathbf{C\text{-}T_s}}[k] = \frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} P_C(t)dt \tag{5.29}$$

where $P_C(t)$ is the instantaneous conduction loss, and $\mathbf{P}_{\mathbf{C\text{-}T_s}}[k]$ is the enfolded form of the instantaneous conduction loss. Using (5.1) and (5.2), (5.29) can be modified for MOSFET as in (5.30).

$$\mathbf{P}_{\mathbf{M\text{-}C\text{-}T_s}}[k] = \frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} {i_D}^2(t) \cdot R_{DS-ON}(25^\circ C) \cdot c(T_j)dt \tag{5.30}$$

Moreover, using the equivalence in (5.31) for a switching MOSFET at a switching period with negligible current variation, the losses can be calculated and quantized as in (5.32) with the inclusion of the temperature effects on the MOSFET conduction losses. Hereby, it should be noted that $k\omega T_s$ term approximates the electrical angle θ (i.e. $k\omega T_s \rightarrow \theta = \omega t$).

$$i_{D-RMS}(k\omega T_s) = i_D(k\omega T_s) \cdot \sqrt{d_i(k\omega T_s)} \tag{5.31}$$

$$\mathbf{P}_{\mathbf{M\text{-}C\text{-}T_s}}[k] = \frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} d_i(k\omega T_s) \cdot {i_D}^2(k\omega T_s) \cdot R_{DS-ON}(25^\circ C) \cdot c(T_j)dt \tag{5.32}$$

where $i_{D-RMS}(k\omega T_s)$ is the RMS value of the drain current for the k^{th} switching period and $d_i(k\omega T_s)$ is the current duty cycle for the k$^{\text{th}}$ switching period. The Duty Cycle Function (CDCF) is defined hereby as the current conduction time $(T_c(k\omega T_s))$ at the k$^{\text{th}}$ switching period over the switching period (T_s) as formulated in (5.33) to be used also for the enfolding of other conduction losses and even for the enfolding operation switching losses.

$$d_i(k\omega T_s) \triangleq \frac{T_c(k\omega T_s)}{T_s} \tag{5.33}$$

The assumption of negligible current variation at a switching period also reduces above integral to (5.34) by assigning the infinitely small differential time *dt* as a large step, which is the switching period (T_s).

$$\mathbf{P}_{\mathbf{M\text{-}C\text{-}T_s}}[k] = d_i(k\omega T_s)\cdot {i_D}^2(k\omega T_s)\cdot R_{DS-ON}(25^{\circ}C)\cdot c(T_j) \tag{5.34}$$

Conduction losses for IGBTs and diodes are calculated with a similar approach for the case of MOSFETs. Using (5.29), IBGT conduction losses are obtained as in (5.35), where the average and the RMS value of the collector current for k^{th} switching period are obtained by making use of (5.36) and (5.37) respectively.

$$\mathbf{P}_{\mathbf{I\text{-}C\text{-}T_s}}[k] = \frac{1}{T_s}\int_{kT_s}^{(k+1)T_s}\left[i_{C-avg}(k\omega T_s)\cdot V_{CE-ON} + {i_{C-RMS}}^2(k\omega T_s)\cdot R_{CE-ON}(T_j)\right]dt \tag{5.35}$$

$$i_{C-avg}(k\omega T_s) = i_C(k\omega T_s)\cdot d_i(k\omega T_s) \tag{5.36}$$

$$i_{C-RMS}(k\omega T_s) = i_C(k\omega T_s)\cdot\sqrt{d_i(k\omega T_s)} \tag{5.37}$$

Inserting (5.36) and (5.37) into (5.35) yields (5.38). Similar to the MOSFET conduction loss case, changing the infinitely small integration step *dt* in (5.38) to T_s results in (5.39).

$$\mathbf{P}_{\mathbf{I\text{-}C\text{-}T_s}}[k] = \frac{1}{T_s}\int_{kT_s}^{(k+1)T_s}\left[d_i(k\omega T_s)\cdot i_C(k\omega T_s)\cdot V_{CE-ON} + d_i(k\omega T_s)\cdot {i_C}^2(k\omega T_s)\cdot R_{CE-ON}(T_j)\right]dt \tag{5.38}$$

$$\mathbf{P}_{\mathbf{I\text{-}C\text{-}T_s}}[k] = d_i(k\omega T_s)\cdot\left[i_C(k\omega T_s)\cdot V_{CE-ON} + {i_C}^2(k\omega T_s)\cdot R_{CE-ON}(T_j)\right] \tag{5.39}$$

Above approach for IGBT conduction loss calculations are simply valid for diode conduction losses as the final enfolded form of the diode conduction loss equation becomes as in (5.40).

$$\mathbf{P}_{\mathbf{D\text{-}C\text{-}T_s}}[k] = d_i(k\omega T_s)\cdot\left[i_F(k\omega T_s)\cdot V_{D-ON} + {i_F}^2(k\omega T_s)\cdot R_{D-ON}(T_j)\right] \tag{5.40}$$

where $i_F(k\omega T_s)$ is the diode forward current and $\mathbf{P}_{\mathbf{D\text{-}C\text{-}T_s}}[k]$ is the enfolded diode conduction losses over a switching period.

5.5.1.2 Enfolding Switching Losses

Switching losses of a semiconductor are also represented by CAPPSC method. The switching losses can be calculated theoretically using instantaneous switching loss as in the case of conduction losses (5.41); however, in practice, it is not useful to compute APPSC since the turn-on and turn-off energies are available rather than instantaneous switching loss power. Practically, the APPSC can be obtained and stored as elements of a vector as formulated in (5.42) for MOSFETs.

$$\mathbf{P}_{\mathbf{S\text{-}T_s}}[k] = \frac{1}{T_s}\int_{kT_s}^{(k+1)T_s} P_S(t)dt \tag{5.41}$$

$$\mathbf{P}_{\mathbf{M\text{-}S\text{-}T_s}}[k] = \frac{1}{T_s}\sum E_{M-SW}\Big|_{kT_s}^{(k+1)T_s} \tag{5.42}$$

where $\mathbf{P}_{\mathbf{M\text{-}S\text{-}T_s}}[k]$ is the APPSC of the MOSFET and $\sum E_{M-S}\Big|_{kT_s}^{(k+1)T_s}$ is the total of the turn-on and turn-off switching energies where these energies can be obtained by using (5.43) between kT_s and $(k+1)T_s$.

$$\mathbf{P}_{\mathbf{M\text{-}S\text{-}T_s}}[k] = \frac{1}{2}V_{block}(k\omega T_s)\cdot I_D(k\omega T_s)\cdot(t_{r-i}+t_{r-v}+t_{f-i}+t_{f-v}) + \frac{1}{2}C_{oss}{V_{block}}^2(k\omega T_s) + V_{block}(k\omega T_s)Q_{rr} \tag{5.43}$$

Although the CDCF ($d_i(k\omega T_s)$) is not included in the evaluation of (5.43), it has an on-off effect on the semiconductor switching losses. For example, if $d_i(k\omega T_s)=0$ or $d_i(k\omega T_s)=1$ there will be no switching losses since the semiconductor will become fully off or fully on. This on-off dependency can be represented as in (5.44).

$$\mathbf{P}_{\mathbf{M\text{-}S\text{-}T_s}}[k] = f(d_i(k\omega T_s))\cdot\frac{1}{T_s}\sum E_{M-S}\Big|_{kT_s}^{(k+1)T_s} \tag{5.44}$$

where $f(d_i(k\omega T_s)) \triangleq \text{sgn}(d_i(k\omega T_s)) \cdot \text{sgn}(1 - d_i(k\omega T_s))$

The approach to calculate the APPSC of MOSFET switching losses is applied to IGBTs and diodes with small variations. The calculation of IGBT switching losses as APPSC is formulated in (5.45). The collector current and off-state voltage dependent form of switching losses in (5.46) is approximated by minimum error power polynomials as in (5.47)

$$\mathbf{P}_{\mathbf{I\text{-}S\text{-}T_s}}[k] = f(d_i(k\omega T_s)) \cdot \frac{1}{T_s} \sum E_{I-S}\Big|_{kT_s}^{(k+1)T_s} \tag{5.45}$$

$$\mathbf{P}_{\mathbf{I\text{-}S\text{-}T_s}}[k] = f(d_i(k\omega T_s)) \cdot \frac{1}{T_s} \left[E_{ON}(I_C(k\omega T_s), V_{block}(k\omega T_s)) + E_{ON}(I_C(k\omega T_s), V_{block}(k\omega T_s)) \right] \tag{5.46}$$

$$\mathbf{P}_{\mathbf{I\text{-}S\text{-}T_s}}[k] = f(d_i(k\omega T_s)) \cdot \frac{1}{T_s} \left[\mathbf{Z}_{\mathbf{E\text{-}ON}}(I_C(k\omega T_s)) + \mathbf{Z}_{\mathbf{E\text{-}OFF}}(I_C(k\omega T_s)) \right] \tag{5.47}$$

where $\mathbf{Z}_{\xi}(\cdot)$ is used as 3 term polynomial operator where the coefficients are the elements of the vector $\mathbf{Z}_{\xi}$ as in (5.48). Here $\mathbf{Z}_{\mathbf{E\text{-}ON}}$ and $\mathbf{Z}_{\mathbf{E\text{-}OFF}}$ are nothing but the polynomial coefficient vectors fitted to turn-on and turn-off energy curves and scaled to operating conditions as stated in (5.22) and (5.23)**.**

$$\mathbf{Z}_{\xi}(x) \triangleq \mathbf{Z}_{\xi}[0] + \mathbf{Z}_{\xi}[1]x + \mathbf{Z}_{\xi}[2]x^2 \tag{5.48}$$

Similar to the cases for MOSFETs and IGBTs, the switching losses of diodes can be enfolded by making use of (5.49). The switching energy expression in (5.26) is used with (5.49) yielding (5.50). The reverse recovery charge in (5.50) is updated at each switching cycle regarding (5.27).

$$\mathbf{P}_{\mathbf{D\text{-}S\text{-}T_s}}[k] = f(d_i(k\omega T_s)) \cdot \frac{1}{T_s} \sum E_{D-SW}\Big|_{kT_s}^{(k+1)T_s} \tag{5.49}$$

$$\mathbf{P}_{\mathbf{D\text{-}S\text{-}T_s}}[k] = f(d_i(k\omega T_s)) \cdot \frac{1}{4T_s} V_{D-block}(k\omega T_s) \cdot Q_{rr}(k\omega T_s) \tag{5.50}$$

Having the enfolding expressions for semiconductor losses to set in the form of APPSC, one can evaluate any MOSFET, IGBT and diode losses at any switching period if the datasheet parameters and the switching constraints (duty cycle, voltage stress, current stress) are available for the semiconductor under interest. The next section describes and details the approach to clarify the switching constraints on the switches.

5.5.2 Switching Constraints

The semiconductor parameters can be obtained from the datasheet, however in order to determine the voltage and current stresses of the switches, therefore the switching losses, it's necessary to specify the switching constraints of each power semiconductor in a PEC, which are topology, switch position and switching pattern dependent. As investigated, depending on the voltage and the current stresses of the power semiconductors, conduction and switching losses can be obtained in the form of APPSC. The conduction losses of a semiconductor at a switching period is directly related to current stress and CDCF ($d_i(\theta)$) of the switch as expressed in (5.34), (5.39), and (5.40). However, for the calculation of the switching losses, the CDCF, voltage stress and current stress of the device should be known for any specific switching period.

5.5.2.1 Current Duty Cycle Function (CDCF)

The CDCF for a semiconductor defined in (5.33) has a direct effect on the conduction losses as the function appears as a multiplier in the equations governing these losses. For switching losses, the function has a non-linear on-off effect as in (5.44). The CDCF contains the information that how does the current flow through the power semiconductor under interest. The CDCF of a semiconductor completely depends on the topology, its switching pattern, the DC bus voltage level in the linear modulation range and the voltage reference of the converter. In three level converters investigated in chapter 3, the CDCF of any power semiconductor is in the form of (5.51), i.e. any power semiconductor in three-level VSIs is either off, either on (carrying the output current for switching cycle), either modulating the output current at active vectors, or at zero vectors.

$$d_i(\theta)=\begin{cases} d_v(\theta) & \text{active vector} \\ 1-d_v(\theta) & \text{zero vector} \\ 1 & \text{ON} \\ 0 & \text{OFF} \end{cases} \tag{5.51}$$

where the output voltage duty cycle function for three-level VSIs can be expressed as in (5.52).

$$d_v(\theta)=\begin{cases} M\sin(\theta) & \text{for} \quad 0<\theta\le\pi \\ -M\sin(\theta) & \text{for} \quad \pi<\theta\le 2\pi \end{cases} \tag{5.52}$$

In Figure 5.16, the CDCFs of power semiconductors of the PT-1 topology are illustrated in. for a modulation index of 0.9 and unity power factor.

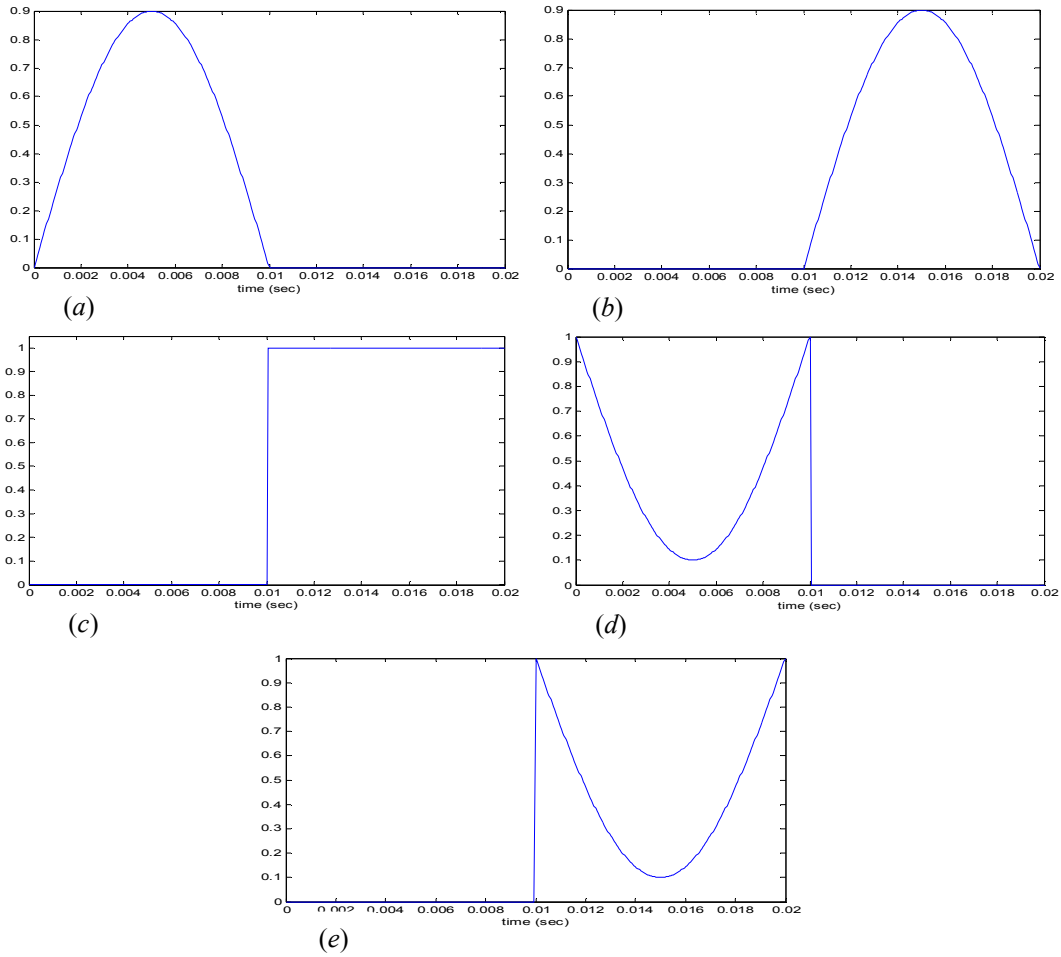


Figure 5.16 CDCFs of the power semiconductors belonging to the PT-1 topology at pf=1 and M=0.9 for (*a*) S1, S4, (*b*) S2, S5, (*c*) S3, (*d*) S6, D3, (*e*) D6.

5.5.2.2 Device Current

The semiconductor losses of a device are strongly dependent on the current of the device. For the efficiency characterization of a PEC, the CAPPSC approach can be used assuming that the output current is free of ripple content as formulated in (5.53). The assumption simplifies the efficiency characterization and expected to preserve the accuracy as the ripple content of the output current is bounded to approximately 20% of the fundamental component.

$$I_s \approx I_{s-1} = I_{s-p} \sin(\theta) \tag{5.53}$$

As the output current is taken as a sinusoid and the switching frequency is many times higher than the grid frequency, the current stress of each device of a GCTSI topology follows the output current when it conducts. For the switching loss calculations, the instantaneous value of the output current is utilized, and for the conduction loss calculations, the RMS and average values of the output current at a switching cycle are used.

5.5.2.3 Device Blocking Voltage

For the switching loss calculation of any power semiconductor, the voltage that is blocked by the semiconductor in the off-state at a switching cycle appears as a multiplier in the switching loss equations (5.43), (5.46), and (5.50). Therefore, the blocking voltage of each semiconductor should be known at any switching time in order to determine the peak voltage stress of a semiconductor (for design issues) and to evaluate switching losses in the form of APPSC.

In order to determine the off-state blocking voltage of a semiconductor belonging to a topology, the assumption of equal off-state impedance of the semiconductors is used. The assumption is expected to give no considerable amount of deviation in the calculations from the actual total amount of switching losses. This is because of the fact that switching loss of a semiconductor almost linearly increases with the voltage blocked at a switching period, and the total of the voltage blocked by high frequency modulating switches at this period is the DC bus voltage.

Having established the procedures to calculate the semiconductor losses, switching constraints of the semiconductors of the PT-1, H5, Heric, H6, NPC+HB, and H6V topologies are listed for positive and negative half cycles of the voltage reference at unity power factor operation in tables 5.1-5.6. In these tables, grid frequency switches are the ones, which have zero CDCF and blocking voltage multiplication ($d_i(\theta) \cdot V_{block}$) both for positive or negative half cycle of the grid. The rest of the switches in a topology are high frequency switches. The controlled semiconductors (MOSFETs or IGBTs) among these high frequency ones are exposed to reverse recovery caused by high frequency diodes.

Table 5.1 Blocking voltage and CDCF of the power semiconductors of the PT-1 topology for positive and negative grid cycles.

Topology	***Switch***	***Cycle***	***Vblock***	$\boldsymbol{d_i(\theta)}$
PT-1	S1	+	$V_{DC}/2$	$M\sin(\theta)$
		−	V_{DC}	0
	S2	+	V_{DC}	0
		−	$V_{DC}/2$	$-M\sin(\theta)$
	S3	+	V_{DC}	0
		−	0	1
	S4	+	$V_{DC}/2$	$M\sin(\theta)$
		−	V_{DC}	0
	S5	+	$V_{DC}/2$	0
		−	$V_{DC}/2$	$-M\sin(\theta)$
	S6	+	0	$1 - M\sin(\theta)$
		−	V_{DC}	0
	D3	+	V_{DC}	$1 - M\sin(\theta)$
		−	0	0
	D6	+	0	0
		−	V_{DC}	$1 + M\sin(\theta)$

Table 5.2 Blocking voltage and CDCF of the power semiconductors of the H5 topology for positive and negative grid cycles.

Topology	***Switch***	***Cycle***	***Vblock***	$\boldsymbol{d_i(\theta)}$
H5	S1	+	0	1
		−	V_{DC}	0
	S2	+	V_{DC}	0
		−	$V_{DC}/3$	$-M\sin(\theta)$
	S3	+	V_{DC}	0
		−	0	1
	S4	+	$V_{DC}/3$	$M\sin(\theta)$
		−	V_{DC}	0
	S5	+	$2V_{DC}/3$	$M\sin(\theta)$
		−	$2V_{DC}/3$	$-M\sin(\theta)$
	D1	+	0	0
		−	V_{DC}	$1 + M\sin(\theta)$
	D3	+	V_{DC}	$1 - M\sin(\theta)$
		−	0	0

Table 5.3 Blocking voltage and CDCF of the power semiconductors of the HERIC topology for positive and negative grid cycles.

Topology	***Switch***	***Cycle***	***Vblock***	$\boldsymbol{d_i(\theta)}$
HERIC	S1	+	$V_{DC}/2$	$M\sin(\theta)$
		−	V_{DC}	0
	S2	+	V_{DC}	0
		−	$V_{DC}/2$	$-M\sin(\theta)$
	S3	+	V_{DC}	0
		−	$V_{DC}/2$	$-M\sin(\theta)$
	S4	+	$V_{DC}/2$	$M\sin(\theta)$
		−	V_{DC}	0
	S5	+	V_{DC}	0
		−	0	$1 + M\sin(\theta)$
	S6	+	0	$1 - M\sin(\theta)$
		−	V_{DC}	0
	D5	+	V_{DC}	$1 - M\sin(\theta)$
		−	0	0
	D6	+	0	0
		−	V_{DC}	$1 + M\sin(\theta)$

Table 5.4 Blocking voltage and CDCF of the power semiconductors of the H6 topology for positive and negative grid cycles.

Topology	***Switch***	***Cycle***	***Vblock***	$\boldsymbol{d_i(\theta)}$
H6	S1	+	0	1
		−	V_{DC}	0
	S2	+	V_{DC}	0
		−	0	1
	S3	+	V_{DC}	0
		−	0	1
	S4	+	0	1
		−	V_{DC}	0
	S5	+	$V_{DC}/2$	$M\sin(\theta)$
		−	$V_{DC}/2$	$-M\sin(\theta)$
	S6	+	$V_{DC}/2$	$M\sin(\theta)$
		−	$V_{DC}/2$	$-M\sin(\theta)$
	D7	+	V_{DC}	$1 - M\sin(\theta)$
		−	V_{DC}	$1 + M\sin(\theta)$

Table 5.5 Blocking voltage and CDCF of the power semiconductors of the NPC+HB topology for positive and negative grid cycles.

Topology	***Switch***	***Cycle***	***Vblock***	$\boldsymbol{d_i(\theta)}$
NPC+HB	S1	+	$5V_{DC}/11$	$M\sin(\theta)$
		−	$4V_{DC}/11$	0
	S2	+	0	1
		−	V_{DC}	0
	S3	+	V_{DC}	0
		−	0	1
	S4	+	$4V_{dc}/11$	0
		−	$5V_{DC}/11$	$-M\sin(\theta)$
	S5	+	V_{DC}	0
		−	$6V_{DC}/11$	$-M\sin(\theta)$
	S6	+	$6V_{DC}/11$	$M\sin(\theta)$
		−	V_{DC}	0
	D7	+	V_{DC}	$1 - M\sin(\theta)$
		−	$2V_{DC}/11$	0
	D8	+	$2V_{DC}/11$	0
		−	V_{DC}	$1 + M\sin(\theta)$

Table 5.6 Blocking voltage and CDCF of the power semiconductors of the H6V topology for positive and negative grid cycles.

Topology	***Switch***	***Cycle***	***Vblock***	$\boldsymbol{d_i(\theta)}$
H6V	S1	+	$5V_{DC}/11$	$M\sin(\theta)$
		−	V_{DC}	0
	S2	+	V_{DC}	0
		−	$5V_{DC}/11$	$-M\sin(\theta)$
	S3	+	V_{DC}	0
		−	0	1
	S4	+	0	1
		−	V_{DC}	0
	S5	+	$4V_{DC}/11$	0
		−	$6V_{DC}/11$	$-M\sin(\theta)$
	S6	+	$6V_{DC}/11$	$M\sin(\theta)$
		−	$4V_{DC}/11$	0
	D7	+	$2V_{DC}/11$	0
		−	V_{DC}	$1+M\sin(\theta)$
	D8	+	V_{DC}	$1-M\sin(\theta)$
		−	$2V_{DC}/11$	0

5.6 Semiconductor Efficiency Characteristics of ZVI-GCTSI Topologies

In all the ZV-GCTSI topologies, passive losses are equal since these topologies require the same DC bus voltage and same inductor current ripple for the same amount of output power. Thus, (if exists) these converters have same input regulator (boosting) and same filter inductor losses. Therefore, the difference in efficiency among these topologies is expected to arise from the semiconductor losses only.

For power semiconductor loss calculation and efficiency comparison of topologies analytically, Matlab is utilized in order to handle matrices and vectors of CAPPSC method easily. A graphical user interface is built to read the switching constraints and semiconductor parameters. The modulation index is taken to be 0.9 at unity power factor and the DC bus voltage 400 V. The semiconductor losses are calculated by CAPPSC method. Two designs are made to observe the semiconductor efficiency characteristics of the ZVI-GCTSI topologies.

The first design is realized for a rated output power of 3 kW. In the design, MOSFETs are utilized for high frequency switches and IGBTs for the line frequency switches with fast freewheeling diodes except the H6V and NPC+HB topologies, FCA76N60N [64] being the MOSFET, and APT150GN60LDQ4(G) [70] being the IGBT with fast anti-parallel diode, where some of parameters of these semiconductors are listed in Table 5.7. For the freewheeling diodes of H6V and NPC+HB topologies, fast diodes of the IGBTs are assumed.

Table 5.7 MOSFET and IGBT+DIODE pair semiconductor parameters extracted from manufacturer datasheets [64], [70] for 3 kW design.

MOSFET	$R_{D\text{-}ON}$ @ 10A (mΩ)	c(100℃)	V_{plateu} (V)	T_{ri} (ns)	T_{fi} (ns)	$R_{g\text{-}test}$ (Ω)	C_{oss} (pF)	Q_{gate} (nC)
FCA76N60N	0.028	1.75	4.7	24	32	4.7	914	218

IGBT+DIODE	$V_{CE\text{-}ON}$ (V)	Ron @ 10A	T coeff @ 125	$V_{D\text{-}ON}$ (V)	$R_{D\text{-}ON}$ (Ω)	Q_{rr} (nC)	$I_{Qrr\text{-}test}$ (A)	$-di_F/dt$ (A/µsec)
APT150GN60LDQ 4(G)	0.5	0.015	1	0.5	0.015	1000	50	200

In Figure 5.17-5.25, loss distributions of semiconductors of the PT-1 topology are illustrated in the form of APPSC for a complete grid period. In Figure 5.17 and 5.18, conduction and switching losses of S1 and S4 are depicted. S1 and S4 have same loss distribution as they have the same voltage and current stresses and same CDCF. Similarly, S2 and S5 have common switching constraints where their conduction and switching losses are depicted in Figure 5.19 and Figure 5.20 respectively. In Figure 5.21, the conduction loss distribution of S3 (implemented as IGBT) is depicted. Since S3 is a line frequency semiconductor, its switching losses are negligible, thus it is not illustrated. In Figure 5.22 the conduction loss distribution of S6 and D3 are depicted. Since S6 (IGBT) and D3 have common voltage drop curves, they have the same conduction loss distribution. It is noticeable that, although S6 is locked on for half of the grid period, the output current only flows at zero vectors. In Figure 5.23, switching loss distribution of D3 is depicted which is low in magnitude as compared to other losses of the semiconductors as expected. In Figure 5.24 and Figure 5.25 conduction and switching losses of D6 are depicted, which are 180 degrees phase shifted forms of conduction and switching losses of D3.

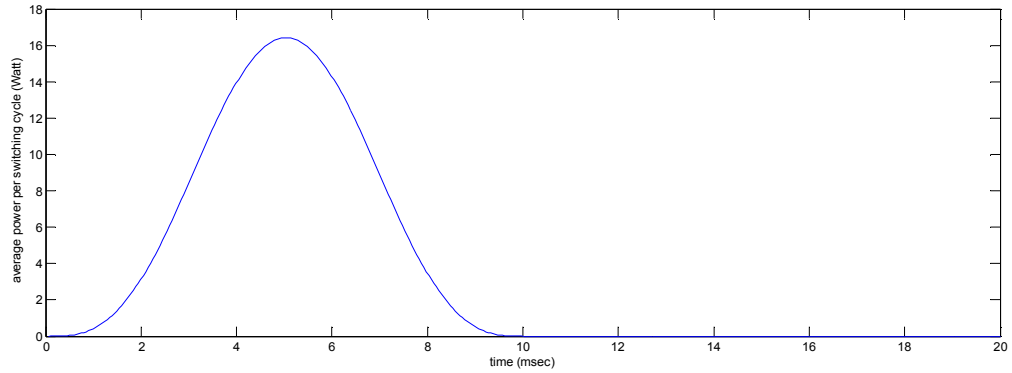


Figure 5.17 The distribution of conduction losses of S1 and S4 semiconductors of the PT-1 topology for a grid cycle in the form of APPSC at full load for 3 kW design.

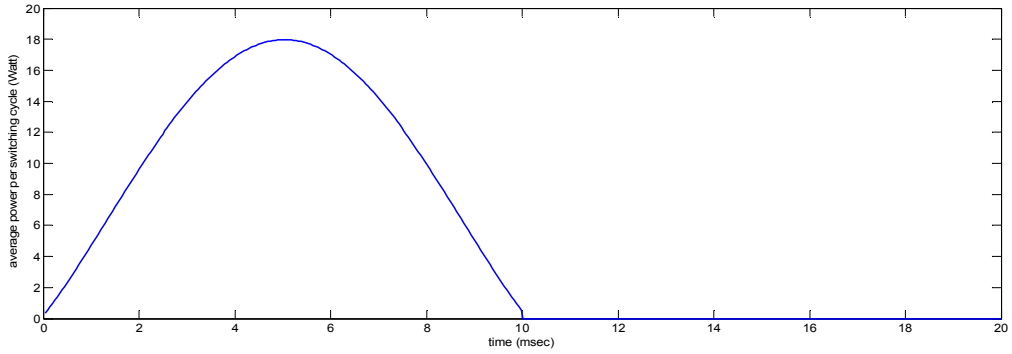


Figure 5.18 The distribution of switching losses of S1 and S4 semiconductors of the PT-1 topology for a grid cycle in the form of APPSC at full load for 3 kW design.

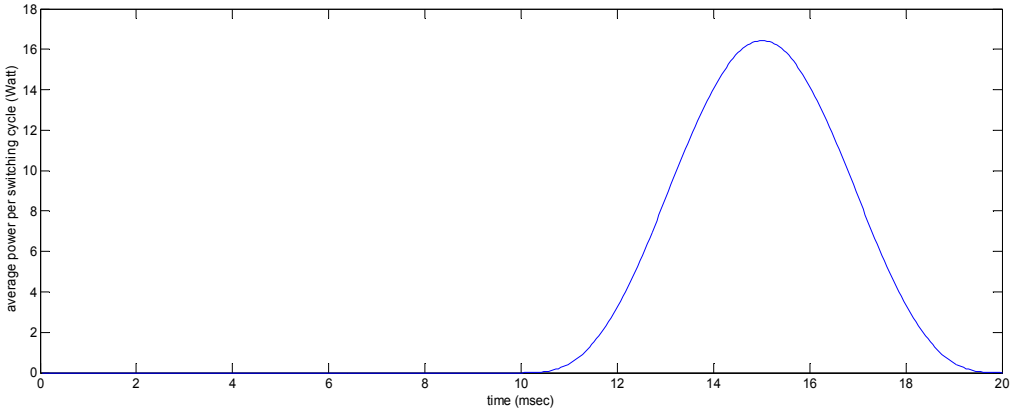


Figure 5.19 The distribution of conduction losses of S2 and S5 semiconductors of the PT-1 topology for a grid cycle in the form of APPSC at full load for 3 kW design.

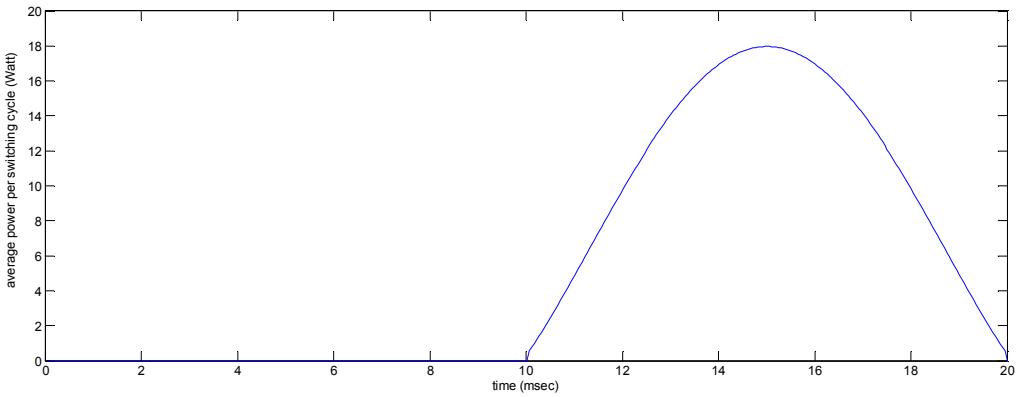


Figure 5.20 The distribution of switching losses of S2 and S5 semiconductors of the PT-1 topology for a grid cycle in the form of APPSC at full load for 3 kW design.

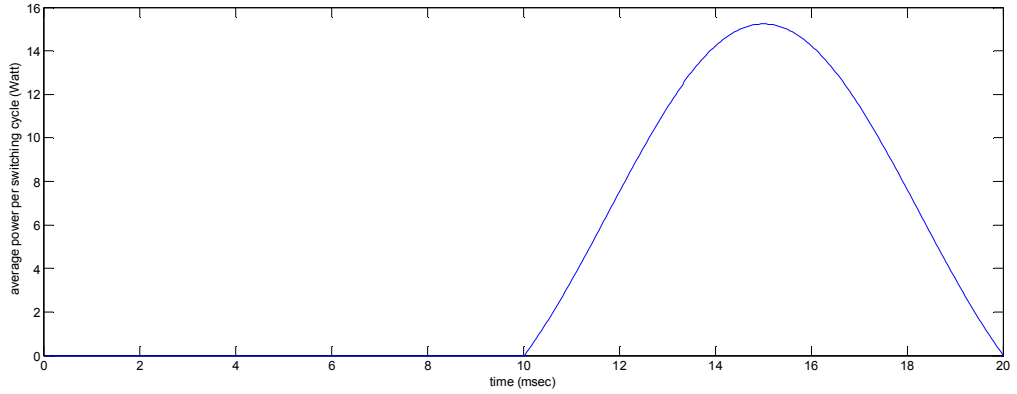


Figure 5.21 The distribution of conduction losses of S3 semiconductor of the PT-1 topology for a grid cycle in the form of APPSC at full load for 3 kW design.

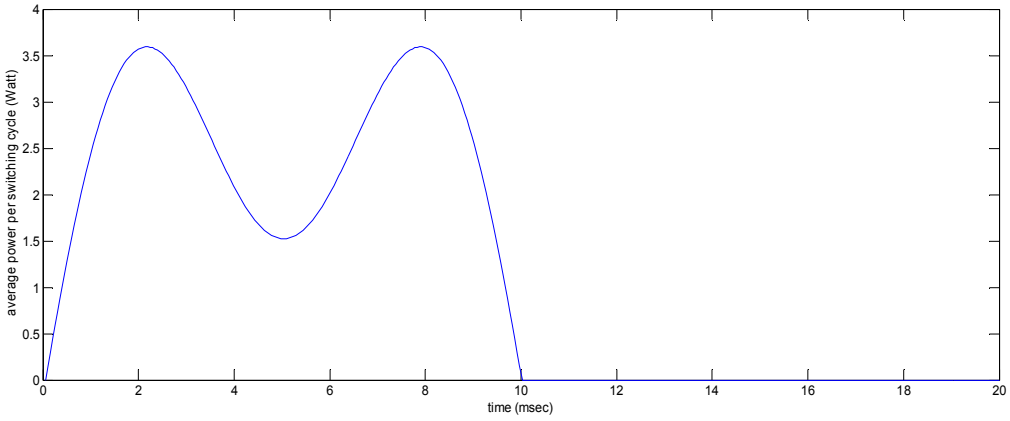


Figure 5.22 The distribution of conduction losses of S6 and D3 semiconductors of the PT-1 topology for a grid cycle in the form of APPSC at full load for 3 kW design.

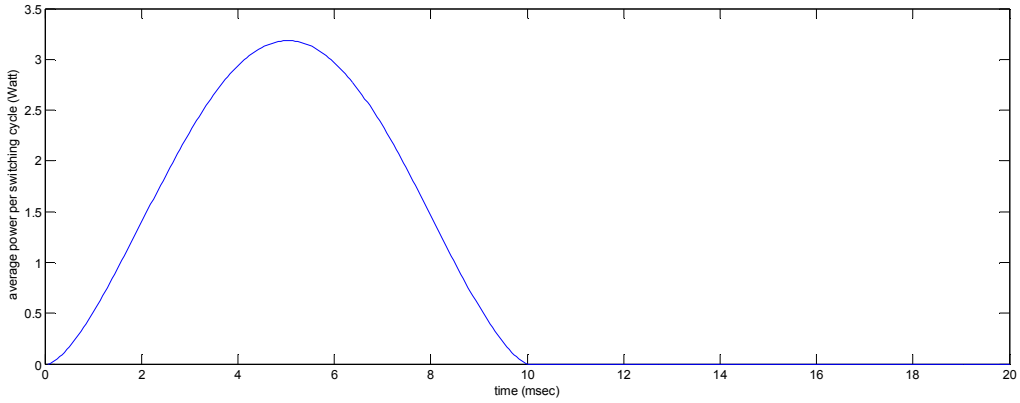


Figure 5.23 The distribution of switching losses of D3 semiconductor of the PT-1 topology for a grid cycle in the form of APPSC at full load for 3 kW design.

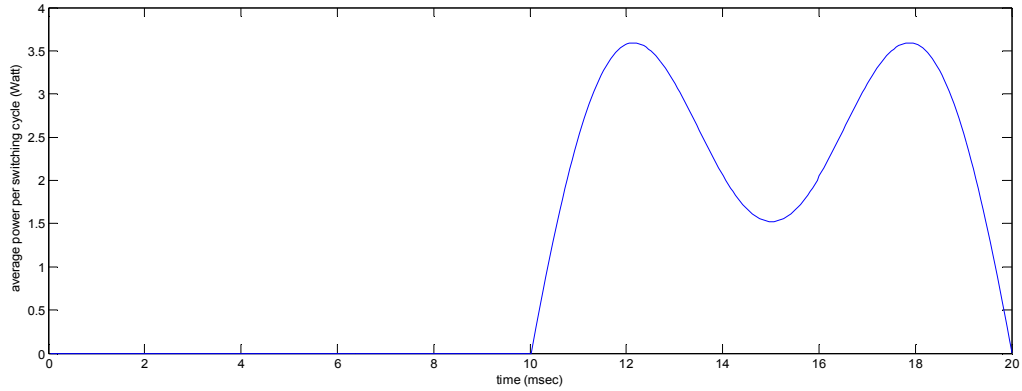


Figure 5.24 The distribution of conduction losses of D6 semiconductor of the PT-1 topology for a grid cycle in the form of APPSC at full load for 3 kW design.

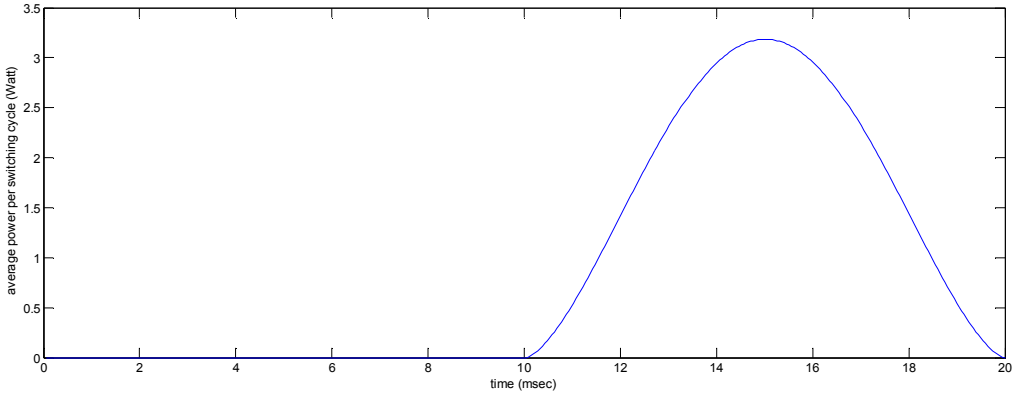


Figure 5.25 The distribution of switching losses of D6 semiconductor of the PT-1 topology for a grid cycle in the form of APPSC at full load for 3 kW design.

In Figure 5.26, efficiency vs. loading characteristics of ZVI-GCTSI topologies are depicted. The efficiency characteristics of each topology peak around 500 W and then decrease as the

loading increases. The decrease is due to the conduction losses as they increase with the square of the output current (or loading). Among the ZVI-GCTSI topologies, the HERIC topology exhibits the highest efficiency characteristics, as its number of semiconductors on the output current path is two at any time. However, since the selected MOSFET devices have very low on-state resistance (at most 36 mΩ at a case temperature of 25℃); the efficiency characteristics of the topologies are very close to each other except the H6 topology (due to high number of semiconductors on the current path). The H5 topology has a lower efficiency characteristic as the number of semiconductors on the current path is always three. The PT-1 topology has an efficiency characteristics lying between the HERIC topology and the H5 topology. At light loading region (loading range smaller than half of the rated power) the NPC+HB and the H6V topologies have better efficiency than the PT-1 topology as only MOSFETs are utilized as controlled semiconductors. Although MOSFETs are utilized, due to their high number of semiconductor on the line current path (three), their efficiency characteristics deteriorate as the loading increases.

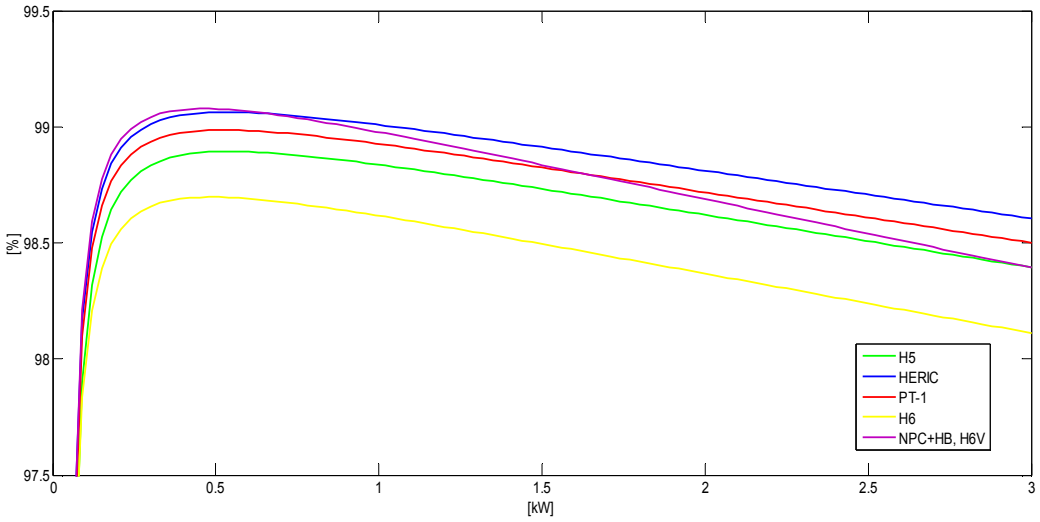


Figure 5.26 Semiconductor efficiency characteristics of ZVI-GCTSI topologies with respect to loading for 3 kW design.

The second design is performed at a rated output power of 10 kW. In the design, IGBTs are utilized for all controlled switches (IXXK100N60C3H1 [69]), where the some of the semiconductor parameters belonging to the IGBT+DIODE pair are listed in Table 5.8. Fast anti-parallel diodes of the IGBTs are assumed as freewheeling diodes where necessary.

Table 5.8 IGBT+DIODE pair semiconductor parameters extracted from manufacturer datasheets [69] for 10 kW design.

IGBT+DIODE	$V_{CE\text{-}ON}$ (V)	Ron @ 10A	$V_{D\text{-}ON}$ (V)	$R_{D\text{-}ON}$ (Ω)	$\begin{bmatrix} \mathbf{Z}_{E\text{-}ON\text{-}t}[2] \\ \mathbf{Z}_{E\text{-}ON\text{-}t}[1] \\ \mathbf{Z}_{E\text{-}ON\text{-}t}[0] \end{bmatrix}$	$\begin{bmatrix} \mathbf{Z}_{E\text{-}OFF\text{-}t}[2] \\ \mathbf{Z}_{E\text{-}OFF\text{-}t}[1] \\ \mathbf{Z}_{E\text{-}OFF\text{-}t}[0] \end{bmatrix}$	$S_{f\text{-}ON}$	$S_{f\text{-}OFF}$
IXXK100N60C3H1	0.8	0.017	0.8	0.01	$\begin{bmatrix} 0.002 \\ 0.0297 \\ 0.0132 \end{bmatrix}$	$\begin{bmatrix} -0.0001 \\ 0.0277 \\ 0.0172 \end{bmatrix}$	0.91	0.9

In Figures 5.27-5.35, loss distributions of semiconductors of the PT-1 topology are illustrated in the form of APPSC for a complete grid period. In Figure 5.27, the common conduction loss distribution of S1 and S4 switches is depicted for a complete grid cycle. In Figure 5.28, the switching loss distribution of these semiconductors is illustrated. Similarly, the conduction and switching losses of S2 and S5 of the PT-1 topology is depicted in Figures 5.29 and 5.30 respectively. As the switching constraints and semiconductor parameters are common in all these four semiconductors, their loss distributions appear to be the same (with phase difference). As a result, total losses on these switches become to be equal. In Figure 5.31 and Figure 5.32, the conduction loss distribution of S3 and S6 are shown respectively. Since these semiconductors operate at the line frequency, their switching losses becomes negligible, thus they are not illustrated. In Figures 5.33 and 5.34, the conduction and switching loss distributions of D3 are illustrated respectively. The conduction loss distribution have two peaks, because of the fact that, as the line current increases the duty cycle of zero vectors decreases. Thus, two peak APPSC points appear in the conduction loss distributions. The conduction and switching loss distributions of D6 have similar characteristics as depicted in Figure 5.35 and 5.36 respectively (only phase difference exists between the ones of D3).

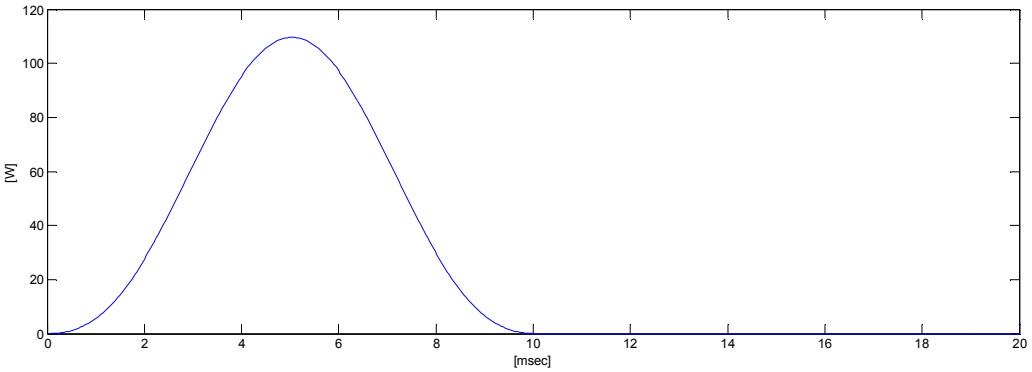


Figure 5.27 The distribution of conduction losses of S1 and S4 semiconductors of the PT-1 topology for a grid cycle in the form of APPSC at full load for 10 kW design.

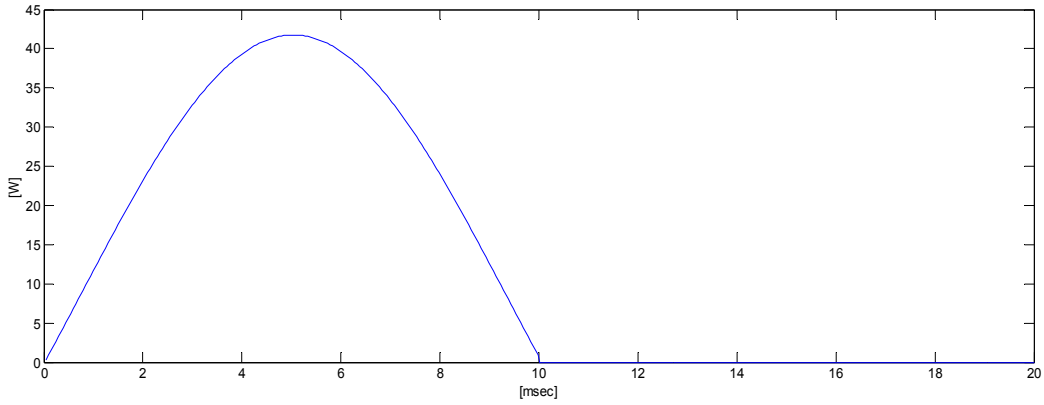


Figure 5.28 The distribution of switching losses of S1 and S4 semiconductors of the PT-1 topology for a grid cycle in the form of APPSC at full load for 10 kW design.

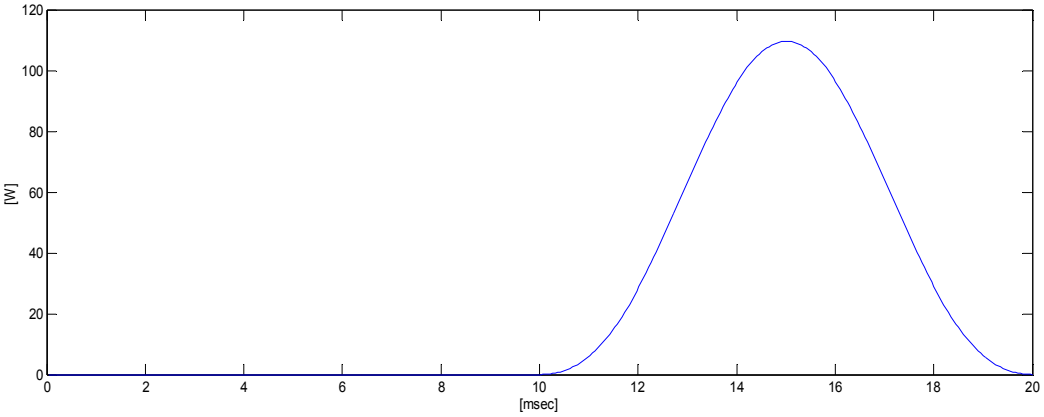


Figure 5.29 The distribution of conduction losses of S2 and S5 semiconductors of PT-1 topology for a grid cycle in the form of APPSC at full load for 10 kW design.

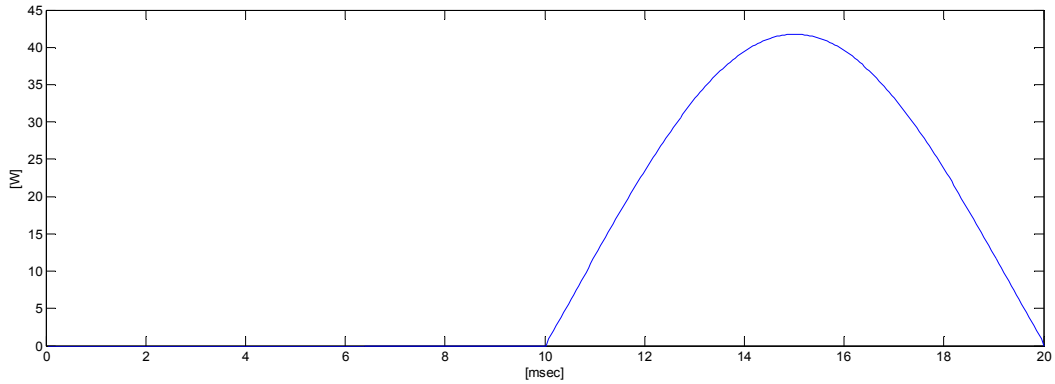


Figure 5.30 The distribution of switching losses of S2 and S5 semiconductors of the PT-1 topology for a grid cycle in the form of APPSC at full load for 10 kW design.

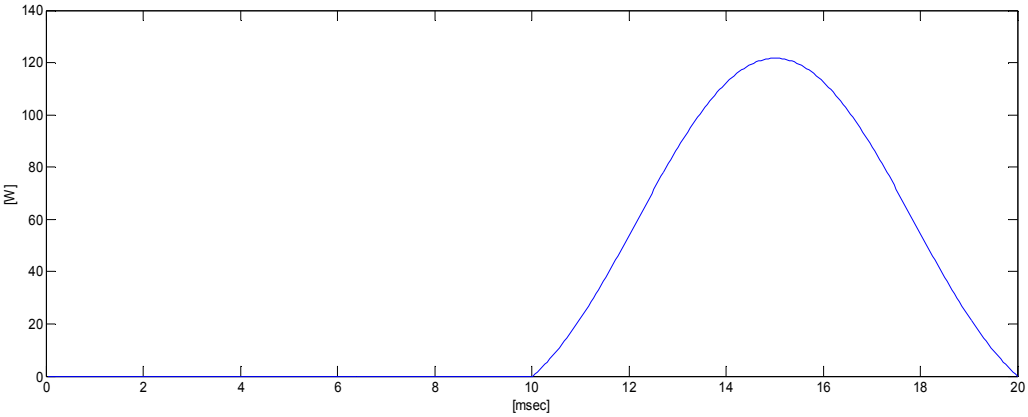


Figure 5.31 The distribution of conduction losses of S3 semiconductor of the PT-1 topology for a grid cycle in the form of APPSC at full load for 10 kW design.

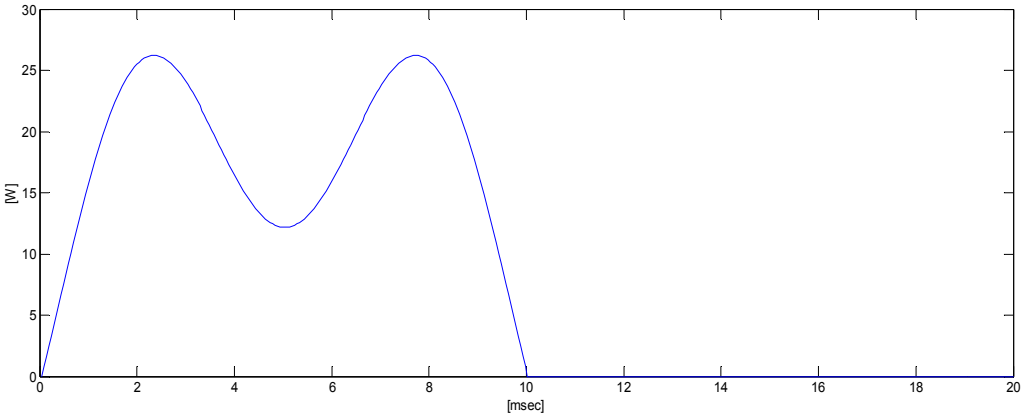


Figure 5.32 The distribution of conduction losses of S6 semiconductor of the PT-1 topology for a grid cycle in the form of APPSC at full load for 10 kW design.

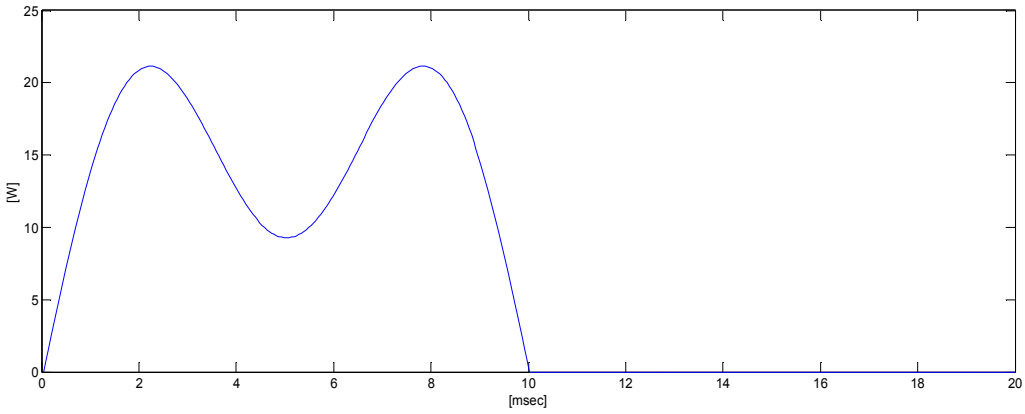


Figure 5.33 The distribution of conduction losses of D3 semiconductor of the PT-1 topology for a grid cycle in the form of APPSC at full load for 10 kW design.

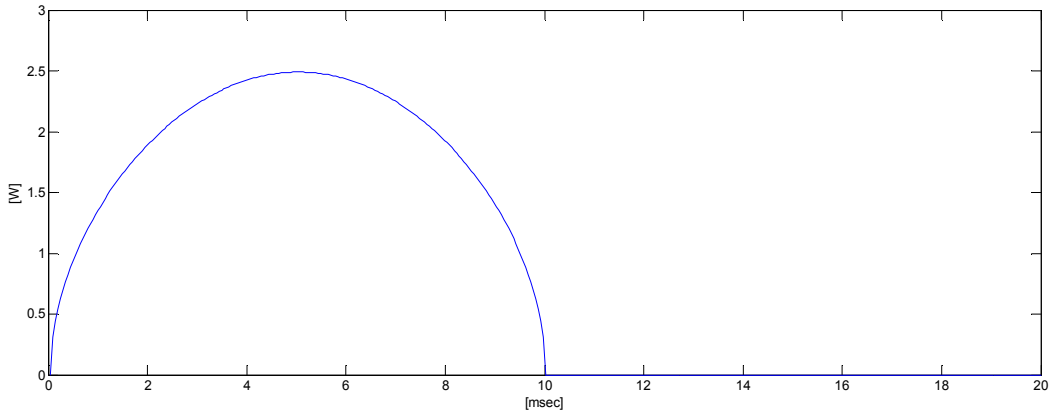


Figure 5.34 The distribution of switching losses of D3 semiconductor of the PT-1 topology for a grid cycle in the form of APPSC at full load for 10 kW design.

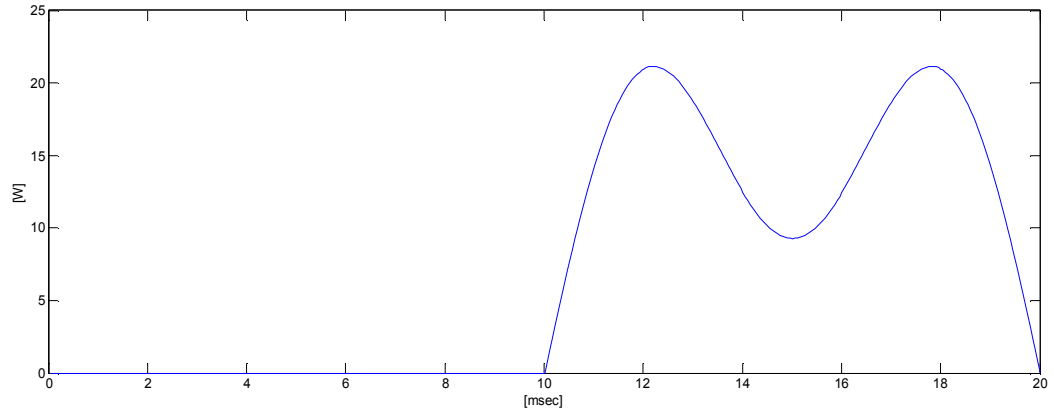


Figure 5.35 The distribution of conduction losses of D6 semiconductor of the PT-1 topology for a grid cycle in the form of APPSC at full load for 10 kW design.

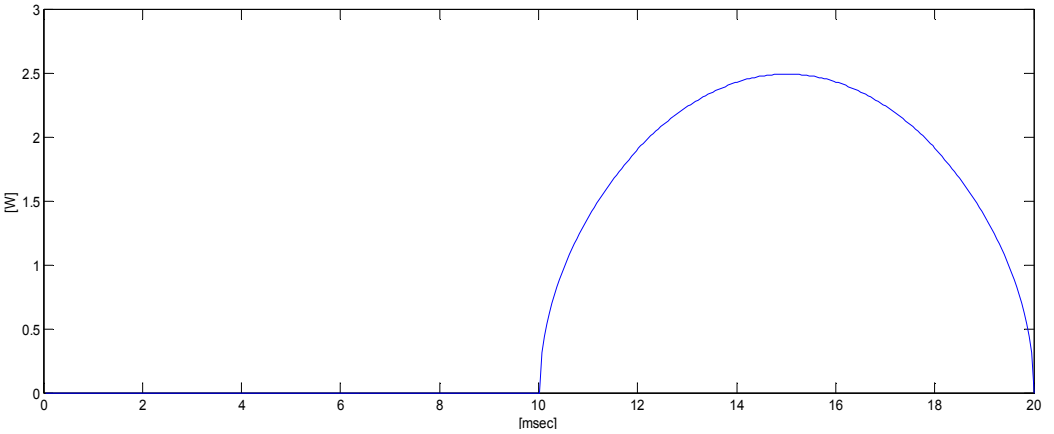


Figure 5.36 The distribution of switching losses of D6 semiconductor of the PT-1 topology for a grid cycle in the form of APPSC at full load for 10 kW design.

In Figure 5.37, efficiency vs. loading characteristics of ZVI-GCTSI topologies are depicted for the 10 kW design with IGBTs as the controlled semiconductors. Because of the constant voltage drop of the IGBTs, the efficiency characteristics of topologies are observed to decrease slightly as compared to MOSFET based 3 kW design. As the voltage drop increase with the current, the number of semiconductors on the line current path is seen to gain higher impact on the efficiency characteristics of a topology; the gaps between the efficiency characteristics between the topologies increase. Among the ZVI-GCTSI topologies, the HERIC topology has the highest efficiency. After the HERIC topology, the PT-1 topology has the highest efficiency among other ZVI-GCTSI topologies in the 10 kW design. When implemented with IGBTs, the efficiency characteristics of the H5 topology, NPC+HB topology, and the H6V topology become same, as their number of semiconductors on the current path being same. Among the topologies, the H6 topology has the lowest efficiency characteristic due to four semiconductors is on the current path at active vectors, and three at zero vectors.

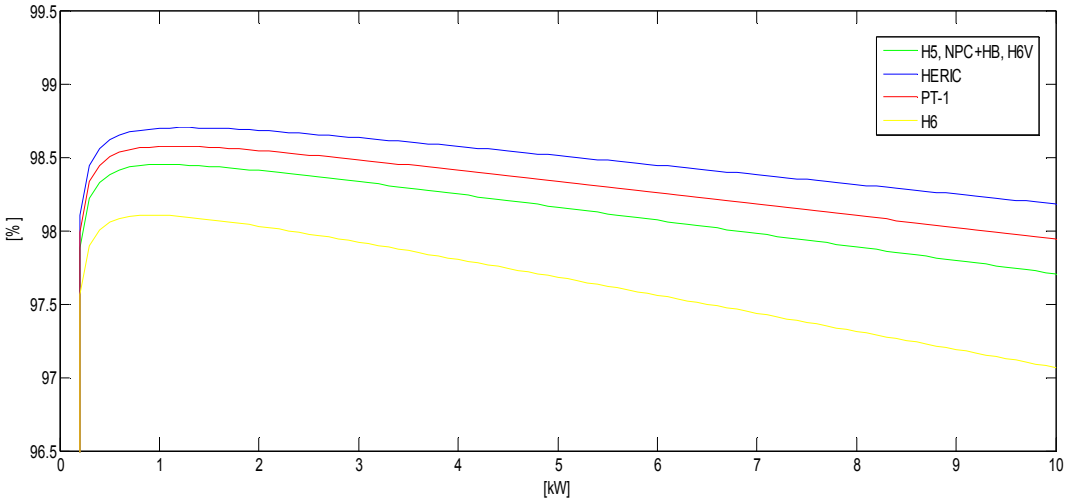


Figure 5.37 Semiconductor efficiency characteristics of the ZVI-GCTSI topologies with respect to loading for 10 kW design.

5.7 Summary

In this chapter, efficiency characterizations of ZVI-GCTSI topologies are performed, as they are vital for the design and the optimization issues. First, the evaluation of the losses relating to MOSFETs, IGBTs, and diodes are investigated. For each device type, the conduction

losses are formulated based on the instantaneous power, whereas the switching losses are formulated based on switching energies of the semiconductors, where the necessary parameters are extracted from datasheets and extrapolated when missing. After the investigation of device loss characterization, the CAPPSC method is given and then, the procedure of the enfolding of conduction and switching losses as APPSC is described for MOSFETs, IGBTs, and diodes. In addition to semiconductor parameters, switching constraints appear in the in the enfolding procedure, thus, these constraints (CDCF, current, voltage, stresses,) are studied and listed for each semiconductor of each ZVI-GCTSI topology. The CAPPSC method based results of 3 kW (MOSFET based) and 10 kW (IGBT based) designs for ZVI-GCTSI topologies are presented, and the PT-1 topology is seen to exhibit high efficiency characteristics among other commercial ZVI-GCTSI topologies.

Derived from ZVI-GCTSI topologies, ZVMC-GCTSI and ZVH-GCTSI topologies are expected to exhibit same efficiency characteristics as the ZVI-GCTSI topologies. For example, the HERIC topology, the PT-2 topology, and the PT-5 topology are expected to exhibit same efficiency characteristics due to the fact that the midpoint-connecting semiconductors have negligible losses as the current flows through them is in the order of mA. In addition to the proposed ZV-GCTSI topologies, the five-level PT-9 and PT-10 topologies are expected to exhibit high overall efficiency characteristics. This inference is based on the fact that, these topologies have low switching losses when the grid voltage is smaller than the feed-forward voltage (the PV source voltage) and the low filter inductor current ripple characteristics. Moreover, the boost stage is bypassed when the grid voltage is smaller than the feed-forward voltage.

CHAPTER 6

CONCLUSIONS

This thesis involves a thorough survey, classification based on leakage current characteristics, analyses of leakage current characteristics, and detailed evaluation of semiconductor efficiency characterization of grid-connected PV-PECs.

As a first contribution, a survey of standards and requirements regarding the grid interconnection of PV energy sources is conducted guiding the design of PV-PECs and the realization of the interconnection is presented within the thesis. The MPPT requirement of PV source is addressed, and then basic MPPT distribution schemes are presented. After the PV source related issues, PV-PEC related requirements are investigated. The utility grid interface restrictions and requirements, such as power quality, and system protection and safety are studied. Apart from other grid-connected equipment, the leakage current restrictions and requirements of PV-PECs are emphasized because of the fact that, in addition to high efficiency, low leakage requirements differentiate PV-PECs from other grid-connected equipment.

Being one of the contributions of the thesis, PV-PEC topologies are investigated and classified (with the focus on GCTSIs) in terms of their leakage current characteristics. The investigation/classification helps engineers to evaluate the pros/cons of a topology used under different conditions (such as high parasitic capacitance of the PV panel, weak grid etc.), and aids in selecting among the vast variety of topologies. In particular, classification based on the leakage current approach yields an improved understanding of converter behaviour to help future development of new GCTSI topologies, and reduces the complexity (instead of learning each topology with difficulty, learning the common properties and emphasizing the small differences).

The major contribution of this thesis is the expansion of GCTSIs with the proposal of new topologies having low leakage current and expectedly high energy conversion efficiency characteristics (η_{EU}>95%). The proposed topologies belong certain commercial topology classes such as ZVI-GCTSI topologies or five-level SC-GCTSI topologies.

As a contribution in chapter 4, based on the number of the output voltage levels, the filter inductor current ripple characteristics are investigated analytically, as the ripple current characteristics of VSIs has high impact on the filter inductance, on the filter inductor size, and on the filter inductor losses. Calculated filter inductor current ripple characteristics of voltage-sourced topologies are verified by simulation results, and high correlation between the analyses and the simulation results is observed.

Another important contribution of the thesis is the identification of the sources of the leakage currents in GCTSIs as they are vulnerable to capacitive leakage currents. For this purpose, equivalent circuits are established, and the source of the leakage current in GCTSI topologies is estimated based on analytical approaches. Simulation results are provided to verify the accuracy of the leakage current estimations. It is demonstrated that, in contrast to common knowledge, the source of leakage current in ZVI-GCTSI topologies is not the inverter CMV variation but the grid voltage variation during zero vector states. In these topologies, it has been observed that the peak currents can exceed several hundred mA levels of standard limits (especially for large parasitic capacitor cases). Therefore, common-mode filtering is required for the suppression of the peak currents in ZVI-GCTSI topologies. The sharply rising leakage current characteristics of ZVI-GCTSI topologies are seen to be absent in ZVMC-GCTSI topologies as they provide (ideally) constant CMV, therefore the peak and RMS values for the ZVMC-GCTSI topologies are found drastically reduced as compared to ZVI-GCTSI topologies with the same parameters. In SC-GCTSI topologies, the leakage current characteristics are found to be grid parameter dependent; therefore, the interconnection of these topologies should be performed with taking the grid parameters into account. The identification of the sources of leakage currents in GCTSI topologies is expected to be helpful in the development of leakage current suppressing methods, in the design of GCTSIs, and in the interconnection stage.

The last contribution of the thesis is the establishment of the algorithmic CAPPSC method to estimate the semiconductor efficiency characteristics of PV-PECs. The CAPPSC method is applied to 3 kW MOSFET based and 10 kW IGBT based power converter designs for the

efficiency characterizations of ZVI-GCTSI topologies, and for the illustration of each power semiconductor's losses for a complete grid period. Among other commercial ZVI-GCTSI topologies, the PT-1 topology is observed to exhibit remarkable efficiency characteristics because of the low number of semiconductors on the line current path (the lowest after the HERIC topology). Although only ZVI-GCTSI topologies are studied in the thesis, it is noticeable that the CAPPSC approach can be applied to any hard-switching PEC in an algorithmic manner.

As future work, experiments should be conducted to verify the operation of proposed topologies and to prove the theoretical leakage current analyses made in this thesis. Moreover, the filter inductor current ripple estimations made in the thesis should be demonstrated to match with the experimental results. The accuracy of the CAPPSC method for semiconductor efficiency characterization of topologies should be verified experimentally and should be modified to yield results that are more precise if it does not fit the actual data. Semiconductor efficiency estimation of other voltage sourced PV-PECs may also be performed after the experimental verification of the CAPPSC method.

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