SIMULATION AND PERFORMANCE EVALUATION OF A FAST AND HIGH POWER PULSED LASER DIODE DRIVER FOR LASER RANGE FINDER

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Approval of the thesis

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ABSTRACT

SIMULATION AND PERFORMANCE EVALUATION OF A FAST AND HIGH POWER PULSED LASER DIODE DRIVER FOR LASER RANGE FINDER

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Laser Diodes (LDs) are semiconductor coherent lightening devices which are widely used in many fields such as defence, industry, medical and optical communications. They have advantageous characteristics such as having higher electrical-to-optical and optical-to-optical conversion efficiencies from pump source to useful output power when compared to flash lamps, which makes them the best devices to be used in range finding applications.

Optical output power of lasers depends on current through LDs. Therefore, there is a relationship between operating life and work performance of LDs and performance of drive power supply. Even, weak drive current, small fluctuations of drive current can result in much greater fluctuations of optical output power and device parameters which will reduce reliability of LDs.

In this thesis, a hardware for a fast and high power pulsed LD driver is designed for laser range finder and is based on linear current source topology. The driver is capable of providing pulses up to 120A with 250µs pulse width and frequencies ranging from 20Hz to 40Hz. It provides current pulses for two LD arrays

controlled with a proportional-integral (PI) controller and protect LDs against overcurrents and overvoltages.

The proposed current control in the thesis reduces current regulation to less than 1% and diminishes overshoots and undershoots to a value less than 1% of steady-state value, which improves safe operation of LDs. Moreover, protection functions proposed in the thesis are able to detect any failure in driver and interrupt LD firing immediately, which guarantees safe operation of LDs.

Keywords: Pulsed Laser Diode Driver, Linear Current Source Topology, PI Controller, Laser Range Finder, Industrial Control, safety of Laser Diodes, Protection of Laser Diodes against overcurrent and overvoltage

ÖZ

LAZER MESAFE ÖLÇÜCÜ İÇİN HIZLI VE YÜKSEK GÜÇ ÇIKIŞLI, DARBELİ BİR LAZER DİYOT SÜRÜCÜNÜN BENZETİMİ VE BAŞARIM DEĞERLENDİRİLMESİ

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Haziran 2012, 140 sayfa

Lazer diyotlar savunma, sanayi, tıbbi, optik haberleşme gibi alanlarda yaygın olarak kullanılan uyarılmış elektronların emisyonu çalışma prensibine dayanan uyumlu aydınlatma cihazlarıdırlar. Flaş lambalarla kıyaslandıklarında elektrikten optiğe olan yüksek verimlilik ve pompa kaynağından yararlı ışık gücüne olan optikten optiğe yüksek dönüşüm verimlilik gibi avantajlı özellikleri olup, bu özellikler lazer diyotları mesafe ölçme uygulamalarında en iyi cihazlar yapmaktadır.

Lazerlerin optik çıkışı gücü lazer diyotlar üzerinden akan akıma bağlıdır. Bu nedenle, lazer diyotların çalışma ömrü ve çalışma performansı ile sürücü güç kaynakları performansı arasında bir ilişki vardır. Zayıf sürücü akımı, sürücü akımındaki küçük dalgalanmalar dahi, lazer diyotların güvenli çalışmasına zarar verecek optik çıkış gücünde ve cihaz parametrelerinde yüksek dalgalanmalara sebep olabilir.

Bu tez çalışmasında, lazer mesafe ölçeri için tasarlanmış ve doğrusal akım kaynağı topolojisine dayalı olan hızlı ve yüksek güç darbeli lazer diyot sürücü için bir donanım geliştirilmiştir. Sürücü 250µs darbe genişliği ve 20Hz' ten 40Hz' e kadar darbe frekansı aralığında, 120A' e kadar darbeler sağlayabilmektedir. Doğrusal akım kaynağı, oransal-integral (PI) denetleyici ile kontrol edilen iki lazer diyot dizisi için akım darbeleri sağlamakta ve bu lazer diyotları aşırı akım ve aşırı gerilime karşı korumaktadır.

Tezde öne sürülen akım kontrolü, akım regulasyonunu %1' in altına düşürerek ve aşırı ve düşük diyot akım değerini olması gereken sabit akım değerinin %1' den daha düşük bir değere indirerek lazer diyotların güvenli çalışmasını geliştirmektedir. Ayrıca, tezde öne sürülen koruma fonksiyonlarının sürücüdeki herhangi bir hatayı tespit edebiliyor ve lazer diyot ateşlemesini anında kesebiliyor olması lazer diyotların güvenli çalışmasını garanti etmektedir.

Anahtar Kelimeler: Darbeli lazer diyot sürücü, Doğrusal akım kaynağı topolojisi, oransal-integral (PI) Denetleyici, Lazer Mesafe Ölçer, Lazer Diyotların güvenliği, Lazer Diyotların aşırı akım ve aşırı voltaja karşı korunması

to my beloved family

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I also would like to thank to my parents Rabia Nilgün ALTINOK and Ömer Faruk ALTINOK, and my sister Gizem ALTINOK for their endless patience, supports, encouragements and their deep belief for success in my thesis work and throughout all my education life.

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Really appreciated.

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LIST OF ABBREVIATONS

A/D converter : Analog-to-digital converter
BJT : Bipolar Junction Transistor
CCM : Continuous Conduction Mode
DCM : Discontinuous Conduction Mode
D/A converter: Digital-to-analog converter
IC : Integrated Circuit
IGBT : Insulated Gate Bipolar Transistor
LD : Laser Diode
LED : Light Emitting Diode
MOSFET : Metal Oxide Semiconductor Field Effect Transistor
P controller : Proportional controller
PCB : Printed Circuit Board
PI controller : Proportional-Integral controller
PID controller : Proportional-Integral-Derivative controller
PWM : Pulse Width Modulation
SMPS : Switch Mode Power Supply
TCR : Temperature Coefficient of Resistor

CHAPTER 1

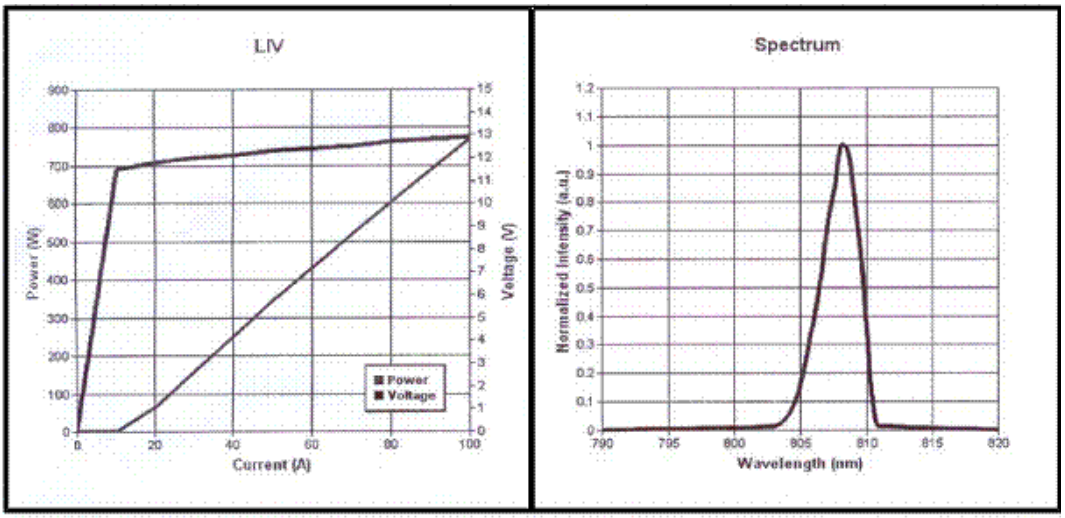
INTRODUCTION

Laser diodes (LDs) are very sensitive semiconductor coherent lightening devices to any small fluctuations in current. Thus, the performance of the LD driver is very critical for the performance of LDs. Because of this reason, instead of traditional power supplies it is essential to provide robust-current controlled diode driver.

The objective of the thesis is to find an appropriate control method to provide appropriate current pulses for high power pulsed LD series. The motivation is to develop a high power pulsed LD driver using two LD arrays, each of which comprises five Nd:YAG type LDs with a manufacturer part number - Lasertel LT-5500-01-1264. The high power pulsed laser diode driver will be used in laser target acquisition and range finder unit of ASELPOD Thermal Imaging System which is developed by ASELSAN Incorporation of Turkey. The specifications of the LD - Lasertel LT-5500-01-1264 are shown in Figure 1-1.

According to specifications of the LD and requirements of the project, the high power LD driver has to provide current pulses with a peak value of 120A for LD series. The peak value of the current has to be adjustable by the control circuitry of the driver within the ranges of 90A to 120A. The width and frequency of the current pulses has to be nominally 200µs and 20Hz, respectively. These parameters also have to be adjustable within the ranges of 200µs to 250µs and 20Hz to 40Hz, respectively by the control circuitry. Because LDs are very expensive and vulnerable to failure, all necessary precautions have to be taken by LD driver. The current pulses should increase and decrease monotonically during

rise and fall periods, respectively. The overshoot and undershoot observed during rise and fall period of current pulses shouldn't be more than 1% of steady-state value. Moreover, rise and fall times of the current pulses shouldn't be more than 10µs to maintain high electrical-to-optical power conversion efficiency. Furthermore, fluctuations on steady-state value of current pulses should be minimized. In fact, the driver should provide a current regulation within 1% of steady-state value.



Parameter	Symbol	Value	Units	Specifications			Pass/Fail
				Lower Limit	Typical	Upper Limit	
Operating Temperature	T	50	°C				
Output Power	P_{op}	700	W				
Pulse Width	PW	250	µsec				
Frequency	f	40	Hz				
Duty Cycle	DC	1.0	%				
Operating Current	I_{op}	91.8	A		100	120	Pass
Operating Voltage	V_{op}	12.9	V		13	14	Pass
Threshold Current	I_{th}	13.3	A		20	25	Pass
Slope Efficiency	ηo	9.02	W/A	7	7.7		Pass
Power Conversion Efficiency	η	59.5	%	40	50		Pass
Center Wavelength	WL_c	807.9	nm	805	808	811	Pass
Spectral Width (FWHM)	FWHM	3.27	nm		3	4	Pass

Figure 1-1. Lasertel LT-5500-0-1264 performance specifications [1].

In addition to LD current requirements, the driver has to have a digital communication interface with laser target acquisition and range finder unit to adjust the properties of the load current. In other words, this unit manages the LD driver by giving instructions and this can be achieved via a communication protocol between the driver and the system. Hence, it is obligatory for the driver

to utilize an intelligent IC such as a programmable IC to maintain communication between the driver and the system.

Electrical output of the LD driver stimulates the electrons in LDs in the system. Optical output of these LDs are used to stimulate the electrons in lasers which are also available in the target acquisition and range finder unit. After stimulation of the electrons, Q switch of these lasers are turned on to release the stored energy. Resultant radiation is used to measure the distance of the target and detect the target. Figure 1-2 shows the simplified block diagram of the laser target acquisition and range finder.

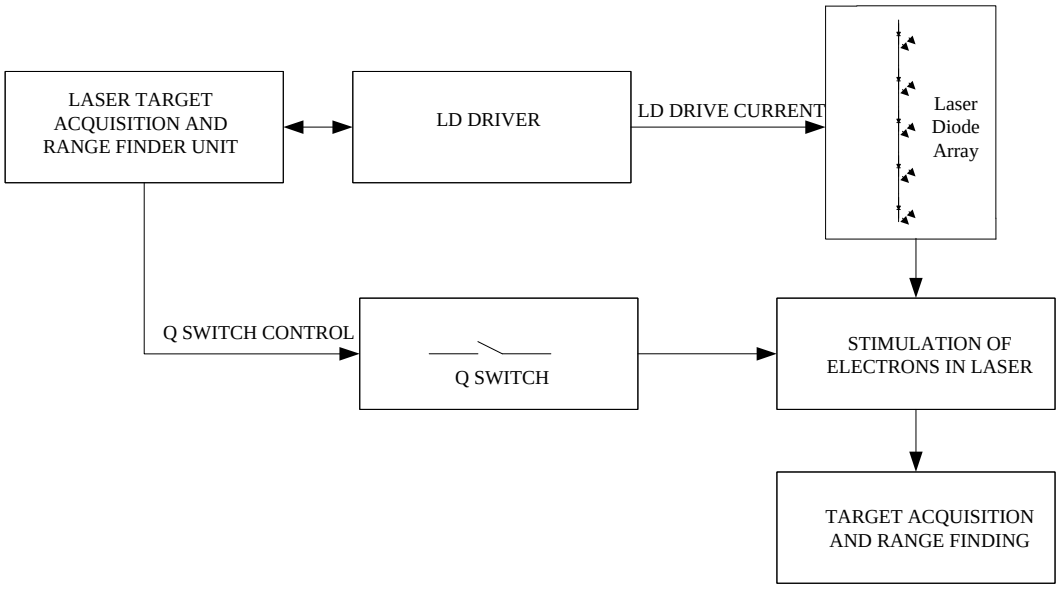


Figure 1-2. Block diagram of the laser target acquisition and range finder.

The current LD drivers are grouped mainly into two categories: switch mode power supply (SMPS) solution and linear current source circuit [2]. As it is understood from the name - SMPS solution, the current LD drivers with SMPS solution use the power supply topologies as the power sources for LDs. However, switch mode power supplies are standard DC/DC converters. Therefore, they cannot directly be used for providing current for LDs. In fact, current sources utilizing SMPS solutions are transformed from voltage sources to current sources. For example, the design of Ian D. Crawford utilizes buck converter topology [3].

As it is known, a buck converter is a step-down DC to DC converter using an inductor, a capacitor, a diode and a transistor to reduce the voltage of a DC supply efficiently. However, this converter is transformed to a current source for LDs by utilizing inductor as an energy storage element to provide current pulses for LDs. Moreover, some authors used buck converter topology in a different way. For instance, the design of Hu Chunsheng, Qin Shiqiao and Wang Xingshu utilizes capacitor as an energy storage element to provide current pulses for LDs [4]. In addition, Joe A. Ortiz designed a current controlled quasi resonant buck converter to provide current pulses for LDs and LEDs [5]. Furthermore, the design of R. Arya, M.J. Thomas, A.G. Bhujle and D.D. Bhawalker is also based on buck converter topology utilizing pulse width modulation (PWM) to provide appropriate current waveforms for pulsed loads [6]. Besides, the design of A. Sharma, C.B. Panwar, R. Arya and A.K. Nath utilizes double switch forward converter topology with PWM as SMPS solution [7]. In these topologies, basically, the energy storage elements like inductors and capacitors used in power source networks provide appropriate current pulses with required pulse width and frequency for LD series. On the other hand, the work principle of linear current source is based on sensing the current floating through the LDs and obtaining the desired current value by means of appropriate control algorithms. The design of Ian D. Crawford and Miguel Morales and the design of Ravindra Singh, Nishma Dangwal, Chandraprakash, Lalita Agrawal, Suranjan Pal and J.A. Kamlakar utilize linear current source circuit [8], [9]. In the thesis, the linear current source topology is used because it is difficult to achieve either smooth waveform of current pulses or low rise and fall times with SMPS solutions. The shape of the pulse almost depends on the values of the determined components in SMPS solutions. On the other hand, the linear current source topology has the flexibility of determining the level and the shape of the current pulses and it is easier to meet the LD current requirements with a proper control algorithm in linear current source topology

Following a discussion of the proposed different circuit topologies, this thesis illustrates the design and test results of a pulsed laser diode driver. The results are compared with other LD drivers.

The proposed pulsed LD driver utilizes a linear current source topology. The contributions of the thesis are to design and implement a high power LD driver using a Proportional-integral (PI) controller and to add protection circuits to protect the LD series. The controller adjusts the amplitude, duration and frequency of the current pulses through the LD series. The thesis also includes the comparative performance analysis of theoretical results and experimental results of the LD driver designed and implemented in the thesis. It is also shown in the thesis that the use of PI controller has increased the robustness and the performance of the driver as expected compared to PID and P controllers.

This thesis totally consists of 5 chapters. The remainder of the thesis is organized as follows.

Chapter 2 includes various types of pulsed LD driver topologies that exist in the literature. Basic work principles, strengths and limitations of each topology are both quantitatively and qualitatively analyzed.

Chapter 3 presents the proposed pulsed LD driver and includes theoretical design issues.

Chapter 4 presents the test results of the proposed and implemented LD driver. Moreover, the robustness, sensitivity and comparative analysis of the design are covered.

Finally, the thesis is concluded with the suggestions on possible improvements in the proposed method as a future work in Chapter 5.

CHAPTER 2

LITERATURE SURVEY

We first present some brief information about pulsed LD drivers that exist in the literature.

2.1 Switch Mode Power Supply (SMPS) Solutions for High Power Pulsed LD Driver

2.1.1 Discharging Inductor Solution

2.1.1.1 Description of the Design

The design of Ian D. Crawford utilizes buck converter topology which provides current pulses for multiple number of LD series [3]. It comprises a storage capacitor, a LD array as the load, a series energy storage inductor between the storage capacitor and the LD array, flyback diode, a shunt switch connected across the terminals of the LD array and a series switch between the LD array and current sense network as shown in Figure 2-1. The switches which are named as S1 and S2 in Figure 2-1 may be power semiconductors such as MOSFETs or insulated gate bipolar transistors (IGBTs).

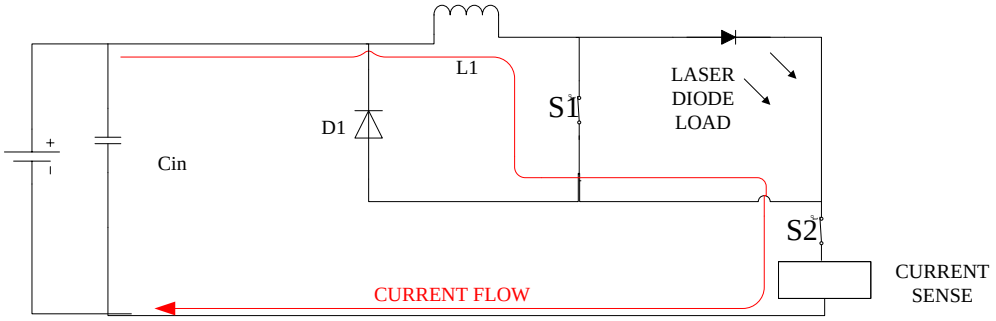


Figure 2-1. Schematic of the LD driver with discharging inductor solution while both switches – S1 and S2 are turned on.

Basically, energy is transferred to the LD array through series energy storage inductor from the input power source by turning on and off the switches properly.

In one period of operation, both shunt switch and series switch are turned on as shown in Figure 2-1 to short out the load and to generate current in the inductor just prior to the laser pulse. The current builds up in the inductor as shown in Figure 2-2.

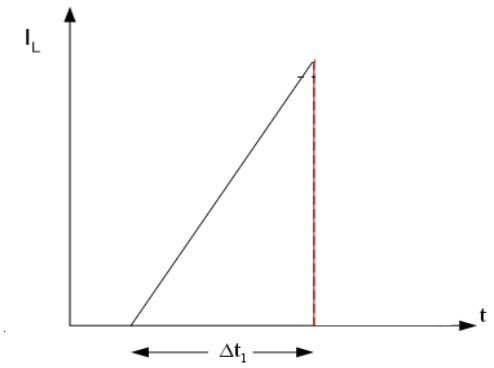


Figure 2-2. Waveform of the inductor current while both switches are turned on.

For a constant input voltage, the current through the inductor can be calculated as [3]:

$$\Delta i_L = \frac{V_S}{L} \times \Delta t_1 \qquad (2.1)$$

since the voltage drop across the terminals of the storage inductor can be considered to be almost equal to input voltage by neglecting the voltage drop across the terminals of the switches and the current sense element.

The current sense network measures the current flowing through the series inductor. When it reaches required value, the shunt switches is turned off as in Figure 2-3 (a). Since current flow in an inductor cannot change abruptly, the current continues to flow into the load. During this time, for a constant source and load voltages, current waveform through the series inductor becomes as in Figure 2-3 (b). Furthermore, load current becomes equal to inductor current [3].

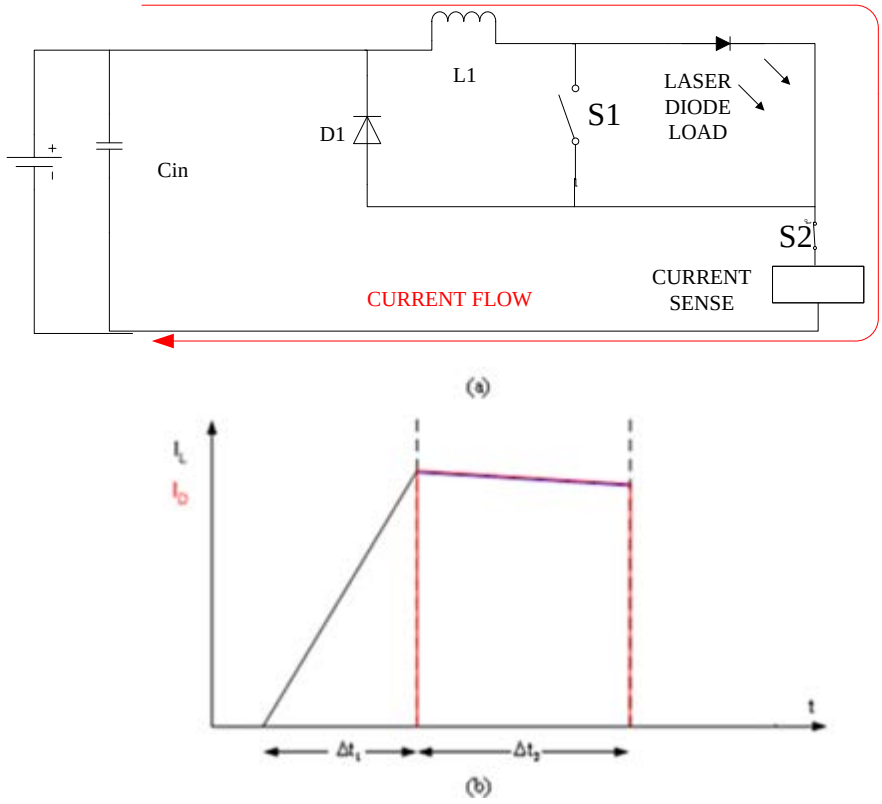


Figure 2-3. (a) Schematic of the LD driver with discharging inductor solution while current flowing through the LD load, (b) Waveform of the inductor current and the LD load current during pulse.

Reduction in the current can be calculated as:

$$\Delta i_L = \frac{V_S - V_D}{L} \times \Delta t_2 \quad (2.2)$$

To end the pulse, the shunt switch is turned on and the series switch is turned off simultaneously as shown in Figure 2-4 (a). As a result, current through the load is diminished immediately through the shunt switch across the load. On the other hand, in very high pulse rate applications, a substantial portion of the energy stored in the series inductor may not be dissipated at the end of the pulse. This energy recirculates and is dissipated slowly in the closed loop comprising the series inductor, the shunt switch and the flyback diode as described in Figure 2-4 [3].

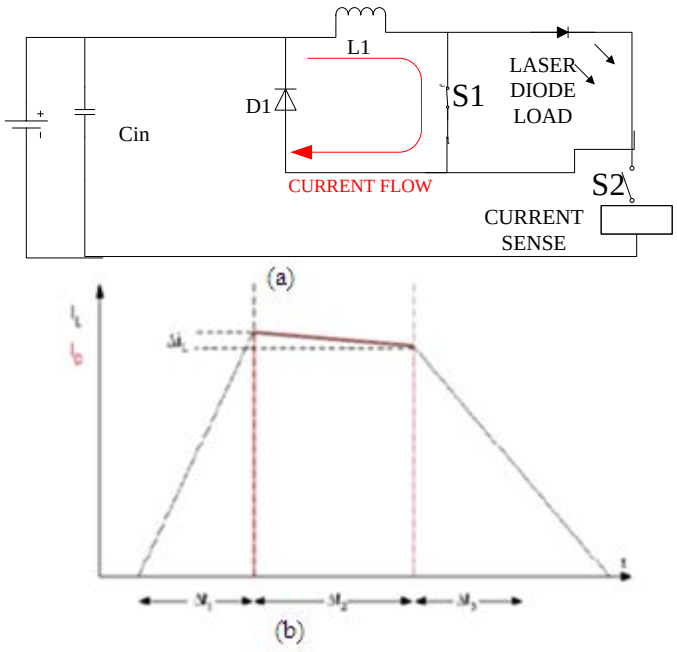


Figure 2-4. (a) Schematic of the LD driver with discharging inductor solution while current flowing through the flyback diode, (b) Waveform of the inductor current and the LD current at the end of the pulse.

For the next period of pulsing, this current can be refreshed before being dissipated completely by turning on the series switch. This energy storage capability reduces the requirements on the power supply, large size components and high cost [3].

2.1.1.2 Advantages of the Design

The advantages of the design are stated by Crawford at [3]:

- Power losses in the LD array are kept small by using saturating switches (shunt and series switches) when compared to linear current sources since the switches are not used as active load. If MOSFETs are used as saturating switches, voltage drop on drain-source terminals become only $(R_{DS(ON)} \times I_{DS})$. Therefore, switching losses are minimized.
- Load requiring higher voltage than the power source can be driven since the energy is stored in the series inductor, which simplifies the power supply requirement. However, it is better to decrease the difference between source voltage and load voltage to minimize both inductor size and current reduction during pulse.
- Fast rise times can be achieved to very high current levels without a need for a high-voltage power supply. Thus, smaller and less expensive components are required respectively.
- LDs are expensive circuit components and are susceptible to electrical damage. The shunt switch protects the LD array when it is turned on.
- Extra energy stored in the series inductor is recycled back to the storage capacitor.

2.1.1.3 Disadvantages of the Design

Discharging inductor solution which is described in [3] utilizes the semiconductor switches as passive switches. As a result, lower rise and fall times can be achieved. However, rise and fall times of the current pulses cannot be controlled in this solution.

The current sense network used in discharging inductor solution is referenced to ground and only detects the current level so that it can provide an ON/OFF signal

for the switches. However, it does not have any contribution to load current regulation, in other words; it does not provide feedback signal for the control of the LD current. Load current regulation totally depends on the values of the circuit components. Moreover, the input voltage of discharging inductor solution should be closer to load voltage to provide the required current regulation.

There are two saturated switches in discharging inductor solution which are had to be switched synchronously. Any time difference between switching times of these switches may result in failure in transferring the energy to the load.

Large inductor size is needed for discharging inductor solution to transfer the energy to the load to achieve high and narrow current pulses with small variation even if the voltage difference between the source and the load is minimized using equation (2.2).

2.1.2 Discharging Capacitor Solution

2.1.2.1 Description of the Design

This part indicates a circuit providing current pulses for LDs which is designed by Hu Chunsheng, Qin Shiqiao and Wang Xingshu [4]. It is stated by the authors that the design is made of fast high-power MOSFET. Its work principle is very similar to SMPS inductor solution. However, in the design, discharging capacitor is used instead of inductor as a current pulse supplier. The authors are describing their circuit with following words; this kind of LD driver module has lots of advantages, compared with discharging inductance. It has bigger output peak power, shorter rise time of output pulse, simpler circuit, higher conversion efficiency and less power consumption.

The driver design typically comprises DC input voltage source, the LD array as the load and a storage capacitor as the current source connected in series to the

load. When the current source is turned on, energy is drawn from the capacitor through the diode array. The voltage on the capacitor falls, so the current source must have sufficient compliance to continue to operate as voltage falls. The value for the energy storage capacitor in the power supply should be selected to produce a maximally flat-top pulse shape. However, instead of a flat-top pulse shape, very narrow, sharp pulse in nanosecond level is obtained in the application described in [4]. Therefore, the selected capacitor value is low.

The authors have given the simplified schematic of the laser diode driver as shown in Figure 2-5. Resistors R1 and R2 are used to limit charging current and the peak current of output pulse, respectively. Capacitor C1 is used as current source for the LD load D2. Diode D1 is used as clamping diode. Switch K is an n-channel enhancement type power MOSFET, controlling the capacitor charging and discharging.

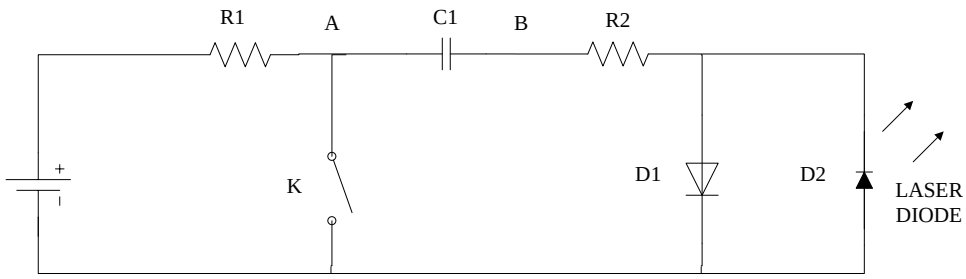


Figure 2-5. Schematic of the LD driver with discharging capacitor solution [4].

In one period of operation, capacitor C1 is charged through resistors R1, R2 and diode D1 and the switch K is turned off as shown in Figure 2-6. The capacitor voltage increases exponentially until being almost equal to input voltage. If desired, the capacitor voltage can also be adjusted to lower value to obtain lower peak value of current. After the completion of charging period, while the voltage at node A becomes almost equal to the input voltage, the voltage at node B becomes almost 0V.

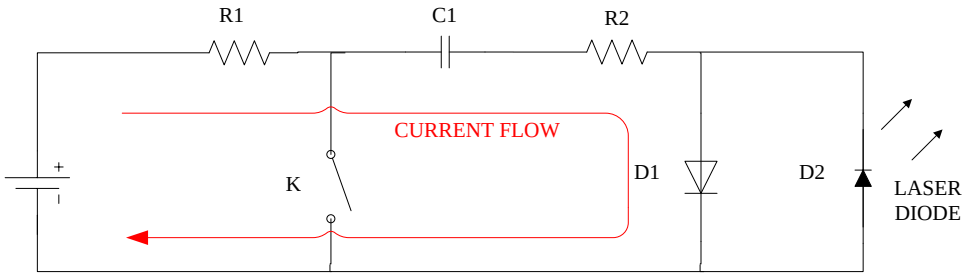


Figure 2-6. Schematic of the LD driver with discharging capacitor solution while capacitor is charged.

At second step, the switch K is turned on. Hence, the voltage at node A immediately drops to 0V. Since the capacitor voltage cannot change immediately, the voltage at node B becomes close to negative value of input voltage source accordingly. As a result, capacitor C1 is discharged through the switch K, LD load D2 and resistor R2 as in Figure 2-7 [4].

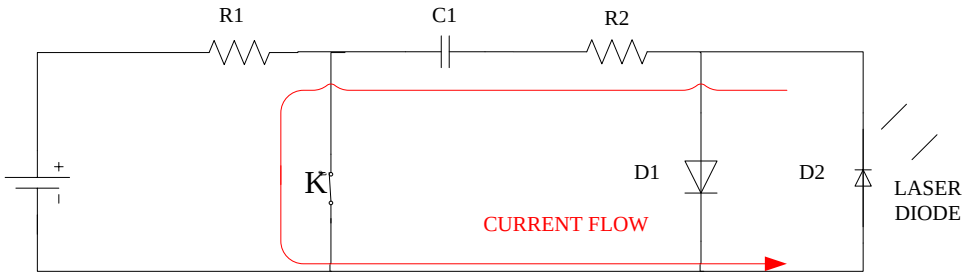


Figure 2-7. Schematic of the LD driver with discharging capacitor solution while the current flowing through the LD load.

2.1.2.2 Advantages and Disadvantages of the Design

The driver introduced in this part eliminates the problem of synchronous switching when compared to discharging inductor solution by using only one switch.

The designers of the driver states that it has bigger output peak power, shorter rise time of output pulse, simpler circuit, higher conversion efficiency and less power consumption when compared to discharging inductor solution [4]. However, load current waveform characteristics such as output peak current, pulse width and pulse frequency still depend on the values of circuit components, which restricts the user while determining the desired current waveform.

2.1.3 MOSFET Based Double Switch Forward Converter Solution

2.1.3.1 Description of the Design

This part indicates a circuit providing current pulses for LDs which is designed by A. Sharma, C. B. Panwar, R. Arya and A. K. Nath [7]. It is stated by the authors that this design is a MOSFET based double switch converter operated in peak current mode control with a two loop feedback taking input from 230V single phase utility mains. It has differential and common mode filters in the output stage which is galvanically isolated from the input and common from the sensing and control circuit to prevent the LD load from any EMI and static charge based damage.

The driver design basically comprises power circuit and control circuit. There are two alternatives considered for the power circuit configuration of the LD driver. The first alternative uses two SMPS stages. It utilizes a rectifier for AC mains voltage to obtain ~300V. Then, first SMPS stage converts this rectified input to a low isolated voltage level. The second stage includes MOSFETs or power BJTs operating in linear region to provide pulsed or continuous current for the load. This power supply solution is said to be a lossy method since it has two SMPS stages. However, it is stated by the authors that it is the unique solution for the applications requiring extremely low ripple in current. The second alternative has

one SMPS stage with increased order of output filter stage to attenuate the switching ripple. This second solution is considered to be more reliable than the first one since it has less number of active components and is more efficient. The LD driver for the second alternative as given in [7] that uses a double switch forward converter as an SMPS solution and the two nested control loops involved are shown in Figure 2-8 and Figure 2-9, respectively.

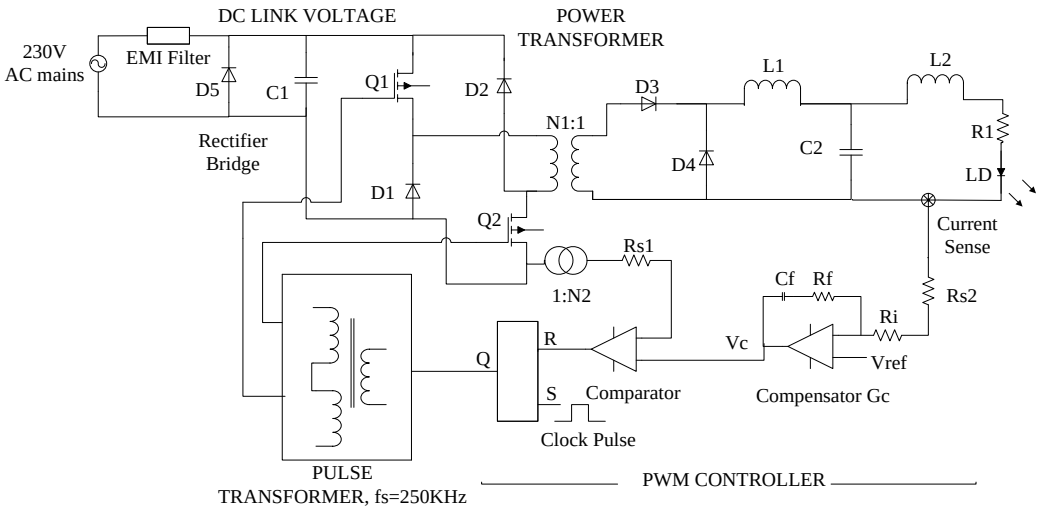


Figure 2-8. Schematic of the MOSFET based double switch converter for LD drive [7].

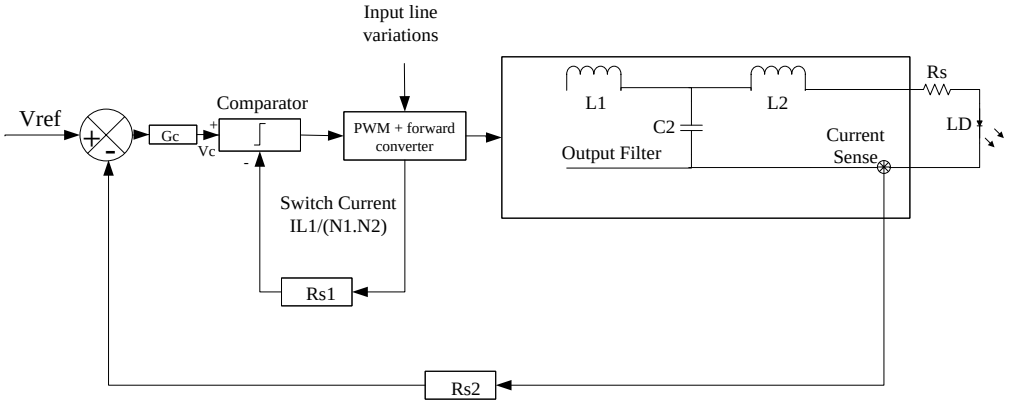


Figure 2-9. Equivalent control block for the LD driver [7].

Reference input in the control stage only indicates the level of the load current. Pulse frequency and width of the current is determined by PWM in the controller

block of the LD driver. Indeed, PWM determines the current to be pulsed or continuous.

2.1.3.2 Advantages of the Design

The advantages of the design are stated by the authors of the paper at [7] as:

- In case of faults such as LD overcurrent, LD overvoltage and any mismatch between reference voltage and load current, the MOSFETs are turned off and the microprocessor turns off the delivered input power to the driver so that the LD can be protected.
- The control circuit is isolated from the input supply and the load since it is less tolerant to noise.
- The peak current mode control which is implemented in the outer control loop provides a lot of advantages to the LD driver which makes the design more robust. These advantages are that:
    (1) It provides a feed forward path for eliminating the effect of input voltage variations within one time period on the inductor current - I_{L1} and so on the LD current.
    (2) Inductor L_1 can be considered as a current source since the feed forward path provides a peak current control with excellent line regulation. In other words, the inductor current - I_{L1} is not considered as a state variable of the converter any more so that the number of poles or the order of the small signal control to output transfer function is reduced by one. This also increases the closed loop bandwidth of the converter so that the closed loop becomes more stable.
    (3) The transfer function of the power stage in continuous conduction mode (CCM) is almost the same as in discontinuous conduction mode (DCM) for low and mid frequencies.
    (4) MOSFET failures are eliminated due to excessive current which also provides a protection for the LD since switching current

flowing through the MOSFETs are primary reflected current flowing through the load.

(5) The transformation saturation is handled so no extra circuit is required unlike for full bridge and push-pull isolated converter topologies.

(6) It is possible to control many LD loads or LD series in parallel without extra current equalization.

In addition, the necessity of large package sizes for MOSFET switches to achieve high level of current pulses with high frequency and pulse width is minimized with the use of step down transformer.

2.1.3.3 Disadvantages of the Design

The disadvantage of the design is stated by the designers of this work that the magnetizing current of the transformer is assumed as zero since it is negligibly small compared to current flowing through the inductor - L_1 reflected on the primary side. Therefore, current flowing through the inductor - L_1 is assumed to be equal to the load current. However, this assumption is not valid for light load applications [7].

The driver is supplied from an AC source instead of a DC source. Therefore, extra EMI filtering and rectification stages are needed in the design to obtain a high DC input voltage and to eliminate the possible noise problem for LD current.

PWM is used in the design for determination of pulse frequency and the width of the current pulse. However, PWM is not appropriate for high power pulsed applications. Indeed, the MOSFET based double switch converter, which is described in previous chapter and uses PWM, can provide maximum 120W instantaneous output power.

2.1.4 Current Controlled Quasi-Resonant Buck Converter Solution

2.1.4.1 Description of the Design

This part indicates a circuit providing current pulses for LEDs and LDs which is designed by Joe A. Ortiz [5]. It is stated by Ortiz that the design is a current controlled quasi-resonant converter which is also named as a zero-switched buck converter that is used as a current source for pulsed LEDs and LDs. The output of the converter which is pulsed current is sensed and then regulated by a control loop to provide appropriate amplitude of current pulses as shown in Figure 2-10.

The design comprises a power source which is serially coupled to switch transistor - Q_1, a resonant inductor - L_1 providing a high impedance for the switch transistor during switching time and minimizing the switching losses of the transistor, a filter inductor - L_2, a diode - CR_1 parallel to switch transistor, a catch diode - CR_2 and a resonant capacitor coupled from a point between the inductors and negative side of the power source masking the capacitance and reverse recovery of the catch diode and minimizing the switching losses of the diode. The current flowing through the LED or LD series is monitored by a current sensor which is serially coupled to the load. The sensed current is used by the quasi-resonant controller to regulate the amount of average current flowing through the switch transistor by varying the switching frequency.

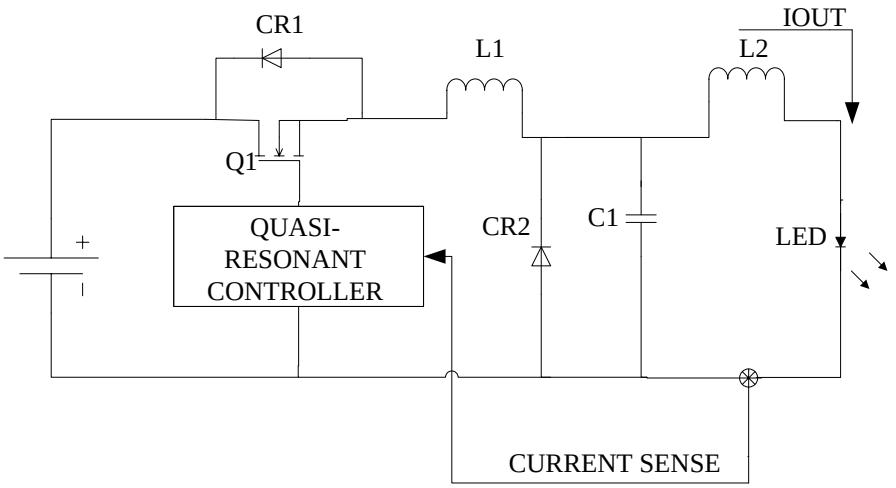


Figure 2-10. Schematic of the LD driver with current controlled quasi-resonant buck controller solution [5].

As it is described by the designer of the driver, load current reaches the steady-state after a few consecutive cycles of switching. Load current raises 30A after two consecutive cycles of switching at 2μs as shown in Figure 2-11 (a). Hence, it is expected to reach 100A after seven cycles of switching at approximately 7μs. In other words, rise time of the pulsed current is expected to be 7μs for 100A.

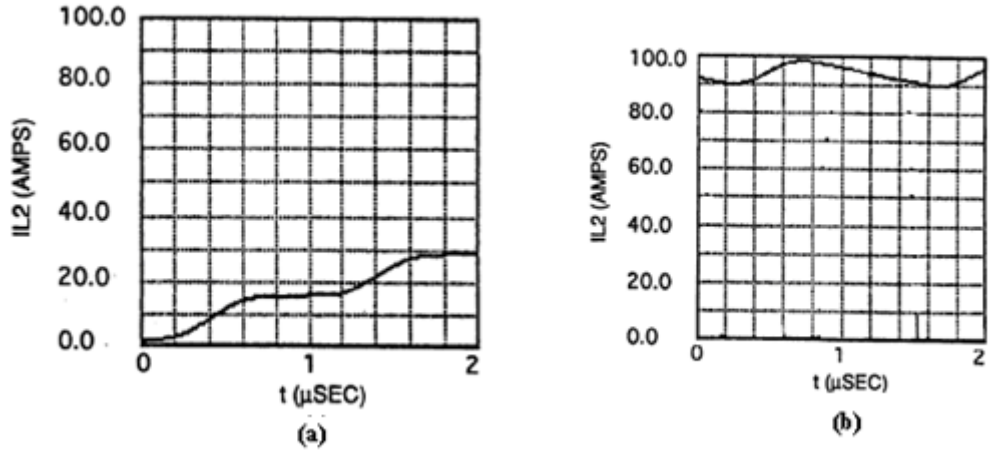


Figure 2-11. LD current (a) after consecutive switching cycles during rise time period, (b) during steady-state operation [5].

2.1.4.2 Advantages and Disadvantages of the Design

The advantages of the design are stated by the author of the paper at [5] as:

- The design minimizes the power losses compared both to the series dissipative regulator and pulse-width-modulated converter to output current solutions.
- The conversion efficiency of the controller is on the order of 85-90% and it is claimed that this value may be improved to 95%. The conversion efficiency of the LD drivers previously mentioned in this chapter is not given by their designers. However, the rate of efficiency seems to be satisfactory.

Besides, rise time of the LD current is obtained as 7μs. However, current regulation of the design seems to be poor as it is seen from Figure 2-11 (b) since ripple on the pulsed current at steady-state is 10A.

There are not any protection mechanisms against overvoltage and overcurrent stated by the author of the paper at [5] although LDs are sensitive devices to even small fluctuations in the drive current.

2.1.4.3 Improvements made on the Driver by the Designer

Ortiz made some improvements on the design which are explained at [10]. In accordance with the improvements, output power from the constant current source is controlled by the shunt switch as shown in Figure 2-12. By turning off and on the shunt switch the duty cycle of the pulses are determined. Indeed, when the shunt switch is turned on, the current flowing through the LD array becomes zero. On the other hand, when the shunt switch is turned off the regulated power is delivered to LD array. Since there is almost no power dissipation in the switch, the efficiency of the driver approaches 100%. The improved efficiency results in a less requirement of high input power, cooler operation and higher reliability. Also,

the output current ripple is extremely reduced. In addition, the rise and fall times of the load current has decreased below 1μs as shown in Figure 2-13 [10].

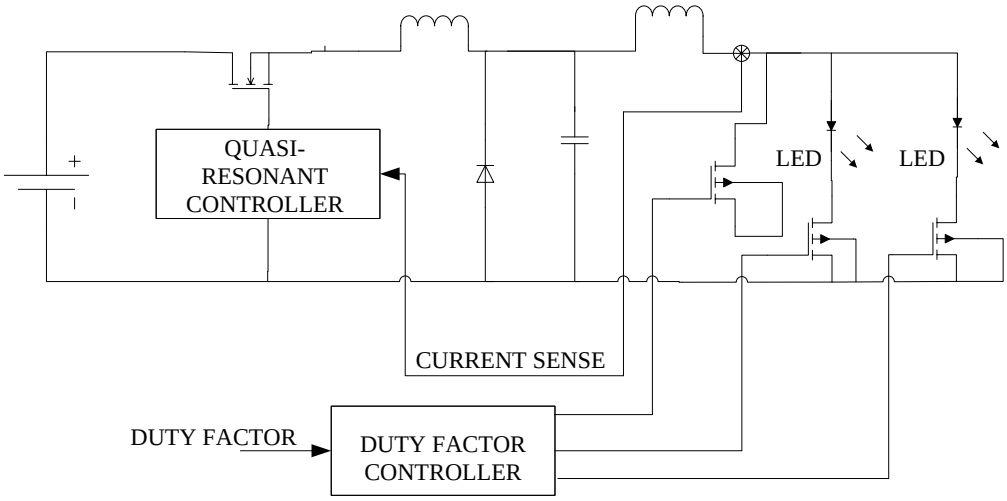


Figure 2-12. Schematic of the improved version of the LD driver with current controlled quasi-resonant buck converter [10].

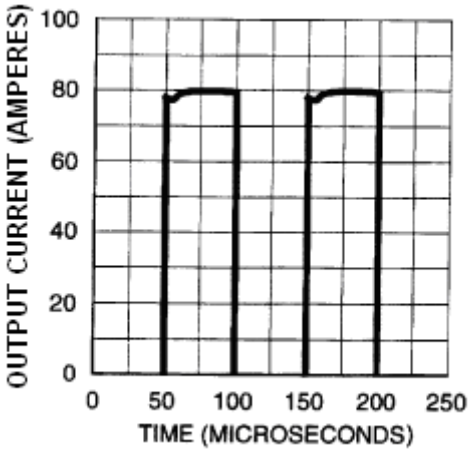


Figure 2-13. Oscilloscope results of output current waveform for improved version of the driver [10].

In the operation of the controller, if the shunt switch is turned on there is no current flowing through the LD arrays. Actually, the shunt switch can be considered as a protection for the LD arrays in case of any failure so that the current flowing through them can immediately be interrupted. If the shunt switch

is turned off and one of the series switches is turned on which are shown in Figure 2-12, current starts to flow through the corresponding LD array. However, there is still no information for overvoltage detection across the LDs stated by Ortiz.

2.1.5 Programmable Arbitrary Waveform Pulse Generator with Buck Converter

2.1.5.1 Description of the Design

This part indicates a circuit providing current pulses for pulsed loads which is proposed by R. Arya, M. J. Thomas, A. G. Bhujle and D. D. Bhawalkar at [6]. It is stated by these authors that this driver is a programmable arbitrary waveform-pulse generator with buck converter, which is a power source designed for flash-lamp-pump quasi-continuous-wave solid state Nd:YAG laser.

Actually, the technology of flash-lamp-pump solid state laser is a former technology for solid state lasers. Nowadays, diode-pumping has been preferred as pump sources for solid state lasers due to their relatively higher electrical-to-optical efficiency. Indeed, the overall laser system efficiency with flash-lamp-pumping is in the range of 1% to 2% due to relatively low electrical-to-optical-efficiency whereas the efficiency of a system with diode-pumping is in the range of 10% to 15%. Therefore, input power requirement of this design is very high compared to ones with diode-pumping [10]. However, operating principle of the design has similarities when compared to other SMPS solutions. Therefore, it is also investigated as a pulsed power source in this chapter.

The design is able to provide current pulses with desired wave shape, level, adjustable pulse width and frequency over a wide range. These pulses can be a train of different shaped consecutive pulses. A reference input signal including the properties of the purposed output current such as pulse width, pulse shape and

amplitude is combined with PWM signal generator so that a reference wave modulated PWM signal can be generated.

2.1.5.2 Advantages and Disadvantages of the Design

The programmable arbitrary waveform pulse generator with buck converter solution which is described in [6] is able to adjust the level of the load current within the ranges of 50A and 200A with a wide range of pulse width as shown in Figure 2-14, which provides a flexibility of being used for a lot of pulsed power applications. However, 42 parallel power MOSFETs are utilized in the design to achieve this. While it is advantageous to use parallel MOSFETs because it decreases the power requirement and decreases the total impedance, it may create a placement problem in the PCB design of the driver and decrease the robustness of the system because if any of these MOSFETs are damaged, drain and source terminals of the corresponding MOSFET may be shorted. As a result, the LD current cannot be controlled any more.

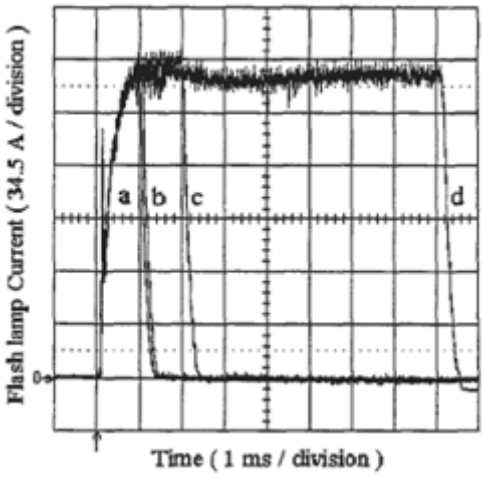


Figure 2-14. Rectangular output current pulses with different pulse widths [6].

In addition, the level of the load current, pulse frequency and pulse width are adjusted via multiple numbers of resistor networks, outputs of which are

multiplexed by an analog multiplexer in this design, which means that the load current waveform depend on the values of circuit components, which restricts the user while determining the desired current waveform as in the case of discharging inductor and capacitor solutions.

Besides, there is not closed loop control for load current in this solution. Also, the rise and fall times of the current waveforms are in millisecond levels [6]. In addition to high rise and fall times, overshoot and ripple on steady-state output current are extremely high for diode pump solid state LDs as it is observed from Figure 2-14. Furthermore, while the design is appropriate for flash-lamp-pump solid state lasers, it cannot be directly used to drive diode-pump solid lasers because there isn't any protection network for the load.

2.2 Linear Drive Solutions for High Power Pulsed LD Driver

2.2.1 Pulsed LD or LED Driver with Proportional Control and Multiphase Controller

2.2.1.1 Description of the Design

The design, schematic of which is shown in Figure 2-15, is a linear current source for pulsed LEDs or LDs and is proposed by Ian D. Crawford and M. Morales at [8]. A linear control element is disposed in the return path from the diode array and the power source. Current flowing through the diode array is sensed by a current sense resistor which provides a voltage indicative current to an input of an error amplifier. The other input of the error amplifier receives a reference demand voltage indicative of the desired current which controls both the switch and the power supply unit to set the level and timing of current pulses for the load array. The output of the amplifier controls the linear pass element to maintain a constant current through the diode array.

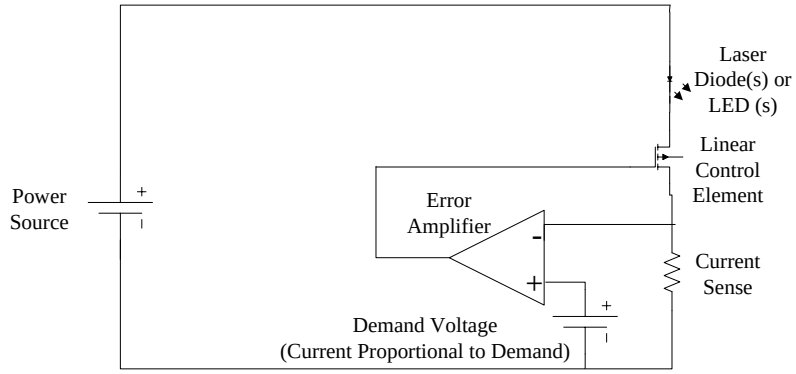


Figure 2-15. Schematic of the LD and LED driver with P control [8].

2.2.1.2 Disadvantages of the Design

The following weak points may be associated with the design. The P control may not be appropriate for the control of LD current because of the existence of an error term between the reference signal and the resultant current. Therefore, the reference signal has to be adjusted so that the desired current level can be achieved. Since LDs have non-linear current-voltage characteristics, it may be difficult to achieve this.

Besides, while the LD current is measured via a sense resistor, the voltage across the terminals of the LD is not measured. Therefore, only a protection against overcurrent may be maintained. None of these failure scenarios are considered by the designers of this driver.

2.2.1.3 Improvements made on the Driver by the Designers

The improved version of the design comprises a power converter which is a standard polyphase (multiphase) controller, a reservoir capacitor at the output of the power converter, a saturated switch in series with load to control the current off and on into the load and a current sensor monitoring the current through the

load as shown in Figure 2-16. Basically, the measured load current is compared to the demand current in the error amplifier stage so that the converter output voltage can be adjusted as null error and means for controlling the saturated switch by providing a switch on/off signal to the switch in response to an externally generated pulsed signal which may be a part of the current level demand signal or separate from the current level demand signal [8].

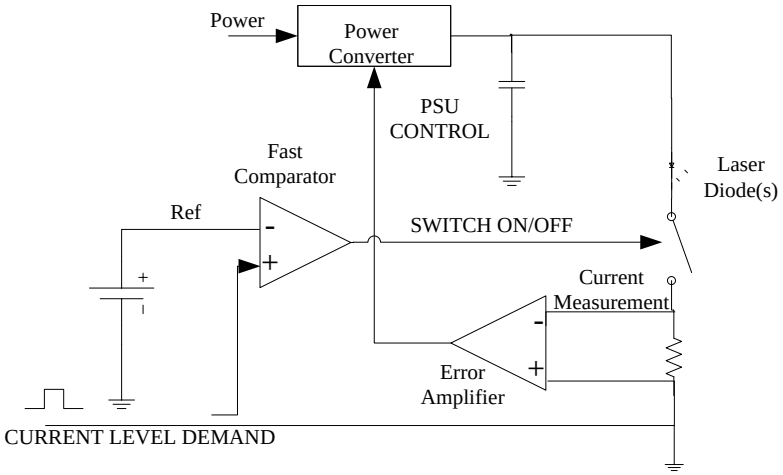


Figure 2-16. Schematic of the LD and LED driver with Multiphase controller [8].

As the current demand signal is increased from zero to a required value, the power supply unit is turned on by the error amplifier and the output filter capacitors are charged. Simultaneously, the series switch is turned on. Then, current starts to flow in the LD. When current flowing through the load reaches the value of the demand current, the power supply unit regulates at a voltage to generate the required current flow in the LD array and the switch. This voltage depends on the V-I characteristics of the load at that time [8].

At the end of the pulse, the demand goes to zero; the switch and the power supply unit are turned off to stop current flowing through the LD array.

As it is stated by the authors of the paper describing the driver, the series switch is used in on or off mode; therefore, switching losses are minimized compared to other linear current sources. Moreover, the series switch can be switched on and

off with a duty cycle in the range of 0.1% and 50%. As a result, a wide range of pulse width is achieved for the load current [8].

The voltage on the filter capacitor remains almost constant until the next pulse since the load has been removed when the switch and the power supply unit are turned off. When the next and subsequent pulse currents are demanded, rise time of the load current is fast since the output filter capacitors are already charged up to the expected voltage to generate the required current for the next pulse in the sequence of pulses [8].

However, the authors have not included a soft-starting mechanism in their design while charging the filter capacitor. This may cause a surge current flow through the LD although the switch is in off mode because an instantaneous leakage current may flow through this switch. Also, the filter capacitor is directly connected to the load in case of a failure, which may be risky for the load in case of a failure in the load current or load voltage. Indeed, the design is still lack of protection networks for the load.

2.2.2 Pulsed LD Driver with Proportional-Integral-Derivative (PID) Controller

2.2.2.1 Description of the Design

The driver introduced in this part which is proposed by R. Singh, N. Dangwal, L. Agrawal, S. Pal and J. A. Kamlakar at [9] is a linear current source providing current pulses for series of 24 Nd:YAG type LD bars used in space based laser transmitters. The design can generate current pulses with 100A peak value, 200µs pulse width and 10Hz pulse frequency.

The design mainly includes SMPS providing input power to the system, soft starting and current limiting networks avoiding accidental overdriving of the LDs

and transient current pulses during power on and PID controller providing constant current for LD array [9].

Figure 2-17 shows the block diagrams of the pulsed LD driver. The design consists of three stages which are input power stage, load stage and the controller stage [9].

The input power stage provides $60V_{DC}$ input for the driver. However, since the SMPS supply cannot provide required instantaneous pulse power for the LD array, a capacitor bank is utilized in the design. The peak current pulses are supplied by the capacitor bank. Moreover, a soft start mechanism is implemented in the driver so as to bring up the current pulse gradually and avoid the impact of surge current during power on [9].

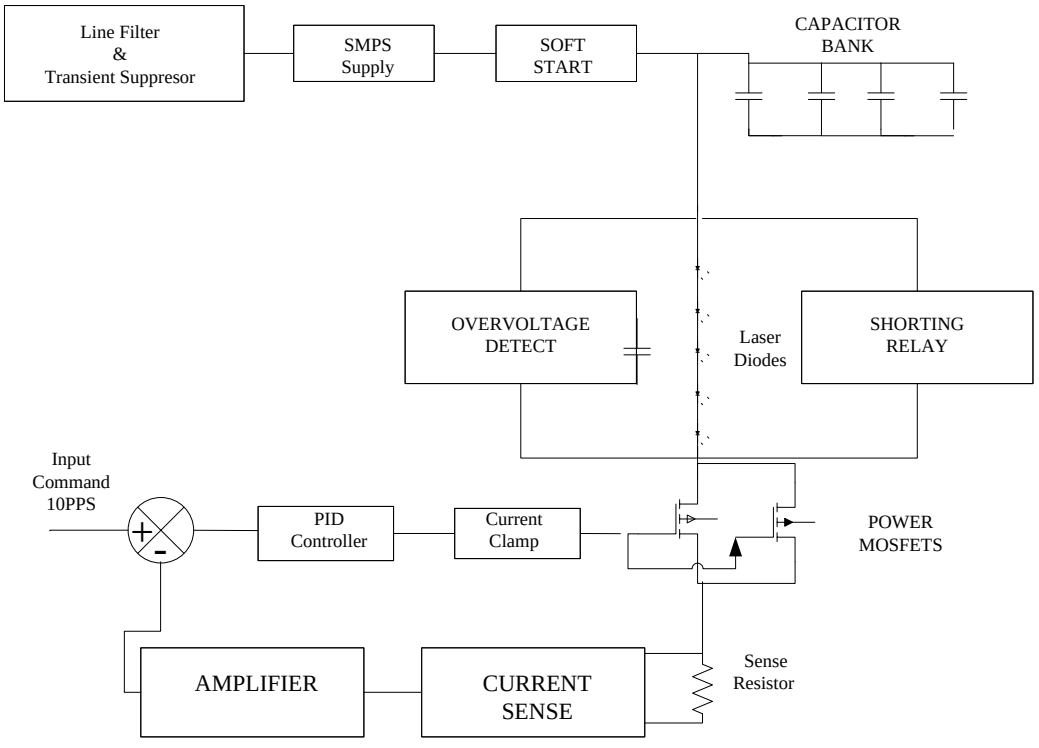


Figure 2-17. The block diagram of the pulsed LD driver with PID controller [9].

The load stage comprises 24 series LD bar with overvoltage detect and shorting relay mechanisms which are responsible for protecting the LDs in case of any overvoltage between the terminals of the load [9].

The controller stage mainly comprises a 10Hz reference input pulse with 200µs, op-amp based PID controller, power MOSFETs and a series sense resistor sensing the load current. Figure 2-18 shows the sub-stages of the controller stage of the driver. The current flowing through the LD array is sensed by a 10mΩ sense resistor. The noise on the sensed current is suppressed by filter stages and then amplified with a proper gain value. The resultant feedback voltage signal is compared with the reference input pulse produced by a timer oscillator so as to generate an error signal. The aims of the closed loop system and the PID controller are to minimize the error signal and to adjust the gate voltage of the power in response to error signal, respectively. The PID controller prevents overshoots and adjusts the rise time of the current flowing through the load [9].

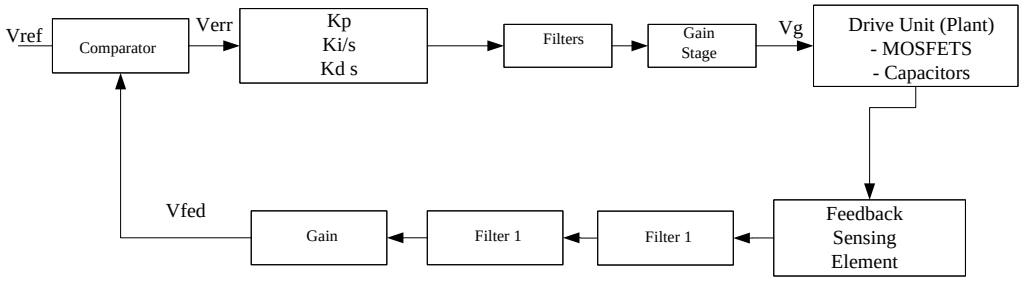


Figure 2-18. The block diagram of the controller loop [9].

2.2.2.2 Simulations and Experimental Results of the Controller Loop

Figure 2-19 shows the simulation results implemented by the designers of the driver and belonging to the control unit of the driver obtained in ORCAD-EDA tool. A reference signal is generated so as to generate current pulses with 80A peak value and 200µs pulse width [9].

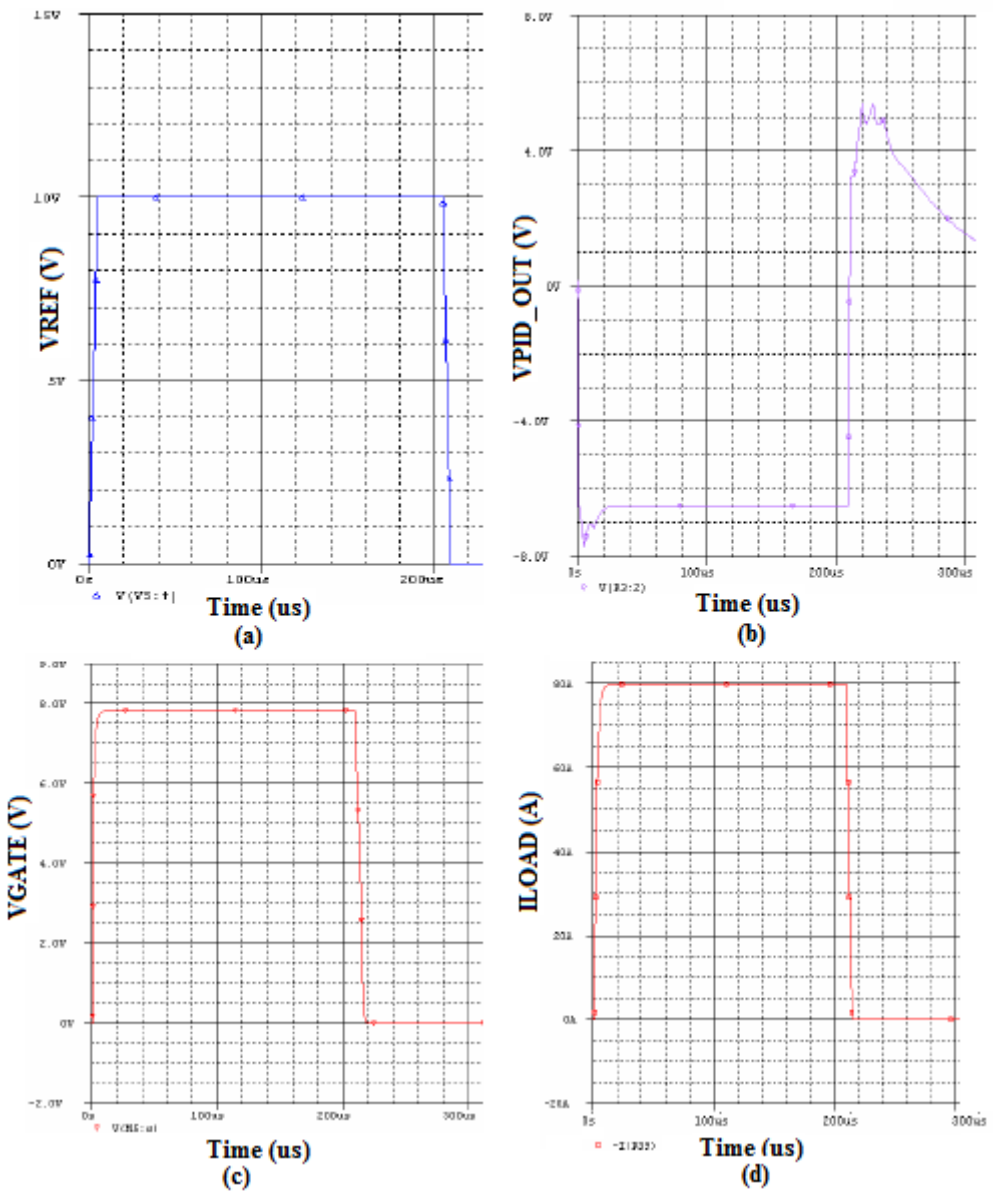


Figure 2-19. (a) Reference input pulse vs. time, (b) the output of the PID controller vs. time, (c) Gate voltage of the power MOSFETs vs. time, (d) Sensed load current across the sense resistor vs. time [9].

The authors of the paper at [9] states that the design aims to provide current pulses with rise and fall times less than 5µs, current regulation within 1% of set value and overshoot and undershoot less than 0.1% of peak value. The simulation results shown in Figure 2-19 are compatible with these requirements.

Figure 2-20 shows the oscilloscope measurements carried out with the hardware comprising the experimental test result of the reference input pulse, gate voltage of the MOSFETs, the output of the PID controller and the voltage across the series sense resistor [9].

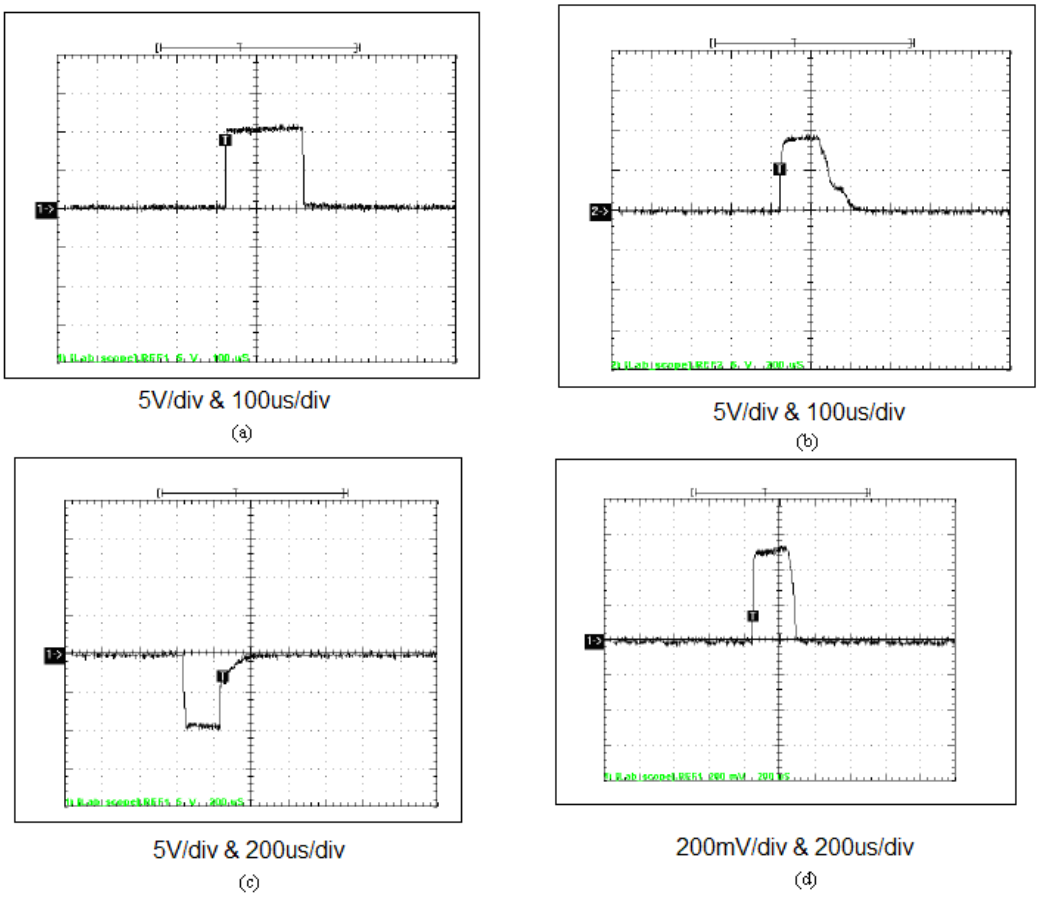


Figure 2-20. (a) Reference input pulse, (b) Gate voltage of the power MOSFETs, (c) the output of the PID controller, (d) the voltage drop across the sense resistor [9].

2.2.2.3 Advantages and Disadvantages of the Design

The driver introduced in this part mostly eliminates the disadvantages of the other solutions mentioned in previous sections. For example, while the linear current source using P controller is not suitable for non-linear loads, this driver is expected to solve this problem with PID controller. The load current is expected

to reach the desired value at steady-state and have almost no overshoot. However, derivative term of the controller is very risky since it can amplify the noise in the system. Indeed, due to high sensitivity to noise, the system can become unstable. This problem seems to be handled by limiting the bandwidth of the system. However, the application in which the design is used is a high speed application. Indeed, rise and fall times of the current pulses are expected to be less than 5µs. This limits the cutoff frequency of the filters to 200KHz. In other words, noise with a frequency less than 200KHz can still be available sufficiently to cause the system to be unstable. In fact, the voltage waveform shown in Figure 2-20 (d), which shows the voltage across the current sense resistor, seems to be noisy.

The experimental results are said to be totally compatible with the simulation results. However, as it is observed from Figure 2-20 (d), peak voltage across the sense resistor - 10mΩ changes between 500mV and 540mV which correspond to 50A and 54A, respectively. Hence, it is difficult to say that the current regulation within 1% of set value is maintained.

Moreover, this driver is able to detect any overvoltage across the terminals of LD array and protect the array by shorting it out with a relay. However, it is understood that a precaution only for overvoltage case is taken in the driver. In addition to overvoltage failure, overcurrent failure though the LD array has to be taken into account.

The driver provides the necessary instantaneous power for firing the LDs from the input capacitor bank because the SMPS supply is insufficient to provide it individually. The capacitors are charged through a soft starting network to protect the LDs from any surge current. However, in addition to protection of the LDs against current transients, it is better to discharge the capacitors in case of failure detection for the safe operation and robustness of the driver.

The driver uses power MOSFETs as active load. Therefore, switching losses are higher compared to SMPS solution. This problem is aimed to be overcome by

using parallel MOSFETs as shown in Figure 2-17. However, it may decrease the robustness of the system as in the case of the design described in [6].

The driver has a flexibility of indicating the property of current pulse by making necessary changes on reference signal. Furthermore, the design has its own power supply. Thus, it can be used in many applications independently. However, extra EMI filtering is needed to suppress the switching noises coming from the power supply. Also, rise and fall times of the current pulses are controllable compared to SMPS solutions.

The current sense resistor is placed at ground side of the driver and source terminals of the MOSFETs are connected to the current sense resistor. This creates the necessity of an extra isolation stage in the controller circuit because a virtual ground is needed to drive these MOSFETs.

CHAPTER 3

PROPOSED METHOD

3.1 Fundamentals of the Proposed Method

This LD driver has been designed in order to provide current pulses for two LD arrays, each of which comprises five Nd-YAG type LDs. The driver utilizes a linear current source topology for the development of current pulses. In literature, both linear current source and SMPS solutions, which are explained in previous chapter, are available for driving pulsed LDs.

Basic work principle of SMPS solutions which are not using PWM is to charge energy storage elements up to a predetermined level of voltage or current, and then to transfer this energy to LD with proper switching elements. However, there are some drawbacks of these SMPS solutions. For example, the driver implementing the discharging inductor solution utilizes the semiconductor switches as passive switches, which means that they work in either ON or OFF mode and are controlled by current sense networks. As a result, fast rise and fall times are achieved as shown in Figure 2-4 (b) in previous chapter. However, rise and fall times of the current pulses cannot be controlled. In addition, input voltage of the driver should be closer to load voltage to provide the required current regulation. Moreover, it is obligatory to switch these switches synchronously for this driver. Any time difference between switching times may result in failure in transferring the energy to the load. Furthermore, large inductor size is needed to transfer the energy to the load requiring high current narrow pulses with small

variation even if the voltage difference between source and load is minimized according to equation (1.2) given in previous chapter. On the other hand, the linear current sources utilize the switches as active load, which means that their control signal which is provided by means of a current sense network determines the level of the pulsed current. Furthermore, current regulation is totally accomplished by control circuit in linear current sources.

Discharging capacitor solution, which is another SMPS solution not using PWM had minimized the disadvantages of discharging inductor solution. For instance, the number of switches has decreased to one, compared with discharging inductor solution. As a result, the efficiency of the LD driver using this solution is improved and the problem of the complexity of synchronous switching of the switches is overcome. Furthermore, the switch provides a protection for LD loads when it is turned off. However, circuit components directly determine the parameters of load current, which restricts the control of current.

Other SMPS solutions use PWM technique to determine the level, pulse frequency and width of LD current. However, these solutions are not appropriate for high power applications. For example, the MOSFET based double switch converter, which is described in previous chapter and uses PWM, can provide maximum 120W instantaneous output power [7]. In fact, it is essential to increase the power requirements of the components in this solution. However, there is a trade-off between the compactness of the system and provision of sufficient power. For instance, the programmable arbitrary waveform-pulse generator, which is described in previous chapter and also uses PWM, comprises multiple number of MOSFETs to achieve high level of current pulses. Moreover, rise and fall time performance of these solutions are very poor.

Because of these reasons, a linear current source topology is utilized in this thesis to provide appropriate current pulses for two LD arrays. In linear current sources, basically, load current is sensed via a series sense resistor and compared to a

reference signal. Resultant error signal is used to control the voltage drop on the series switch to provide a constant current during pulse period.

Linear current sources in the literature are utilizing proportional (P) and proportional-integral-derivative (PID) controllers for the control of LD current. These controllers are purely op-amp based controllers. However, P control is not appropriate for the control of LD current because, there always exist an error term between the reference signal and the resultant current. Therefore, the reference signal has to be adjusted so that the desired current level can be achieved. However, since LDs have non-linear current-voltage characteristics, it is difficult to achieve this. On the other hand, PID controller is better when compared to P controller because the error term between the reference signal and the resultant current is zero under ideal conditions. However, derivative term of the controller is very risky since it can amplify the noise in the system. Indeed, due to high sensitivity to noise, the system can become unstable. Also, large bandwidth requirement of the system due to limitations in rise and fall times of the pulsed current makes it difficult to take necessary precautions to eliminate noise. Hence, the driver implemented in the thesis work utilizes an op-amp based proportional-integral (PI) controller.

3.2 Architecture of the LD Driver

This LD driver has been designed to be used in laser target acquisition and range finder unit of ASELPOD Thermal Imaging System which is developed by ASELSAN Incorporation of Turkey. Therefore, the driver to be developed has to satisfy some extra constraints which will be coming from this interconnection, as a result of which the driver is fed by an external DC power source at 82.5V and drive two LD series with constant current simultaneously. Moreover, a digital communication interface with a “Laser Control Card" is added to adjust the properties of the load current. In other words, the “Laser Control Card” manages the LD driver by giving instructions via a communication protocol. Therefore, a

programmable IC is used in the design to maintain the communication between the driver and the "Laser control Card". programmable IC is an interface between the “Laser Control Card" and the other blocks in the driver. In addition, the “Laser Control Card” provides the necessary voltages for the ICs used in the driver.

The external power source feeding the LD driver will not be able to supply necessary power to the driver to fire the LDs because large amount of current is expected to flow through the LD series and the output drive current capacity of the external power source is not sufficient to drive these loads individually; which is also shown in the calculations using equations (3.1) and (3.2). Therefore, a capacitor bank block is implemented to provide the necessary power during current pulse. In fact, necessary power should totally be supplied from the capacitor bank; hence the interaction between the external power source and capacitor bank has to be interrupted during pulse. Otherwise, the power module providing the input power tries to supply current together with the capacitor bank for the load, which may result in a voltage reduction at the output of the power module since it will try to provide the necessary current for the load individually although the capacitor bank is in conduction. In other words, output stage of the power module may be exposed to a failure by going on trying to provide the load current individually. Moreover, capacitors initially have instantaneous low impedance due to their effective series resistance during their initial charge; hence, there occurs an instantaneous high current flow which can result in a reduction in the value of input supply. To prevent this, a soft start mechanism is implemented in the design. Actually, soft start networks are implemented in LD drivers to prevent the LDs from surge current during power on as in [9]. However, the aim of the soft start network implemented in this driver is to protect the input power module. On the other hand, a new solution, which is thought to be a better solution than the soft network implemented in [9], is implemented in the driver to overcome the problem of surge current during power on. A high side overcurrent protection block is designed so as to interrupt the connection between the input stage and the LD arrays during capacitor charging prior to firing. This block is

also responsible for blocking of the load current in case of detection of overcurrent through the load.

It is mentioned in previous chapter that linear current sources are less efficient than SMPS based drivers since they use the switches as active loads. In other words, if MOSFETs are used as switches, voltage drop on drain-source terminals will become more than $(R_{DS(ON)} \times I_{DS})$ during pulse. Therefore, power dissipation on MOSFETS is expected to be higher in linear current source compared to SMPS based drivers. This is the general problem of linear current sources. To improve the efficiency of the driver, an input capacitor voltage adjustment unit is implemented in the driver which is not available in other linear current sources in the literature to my knowledge. The design is able to charge the capacitor to an optimum level which is determined by the programmable IC considering the voltage drop on capacitors during pulse and the voltage drop on LDs so that power stress on MOSFET switches can be minimized.

As it is mentioned above, in case of overcurrent detection, high side overcurrent protection network prevent the current through to load. In addition to protection of the LDs, the capacitor bank has to be discharged for the safety of the rest of the circuit. Thus, a capacitor discharge unit which is controlled by the programmable IC and not available in other linear current sources is implemented as well.

The main purpose of the driver is to control the LD current. Therefore, current sense networks are required for each LD array to feed the load current information into the controller. Furthermore, a controller block which is an op-amp based analog controller and is in interaction with the programmable IC and current sense network is designed to provide the requirements of the current.

In addition to input block, protection blocks and current control block, it is necessary to provide an interface between analog and digital networks in the design. Indeed, the programmable IC is the main control mechanism for these blocks. However, input and output (I/O) pins of this IC are in digital format;

hence, they are not directly applicable to manage the analog networks. Thus, analog-to-digital conversion and digital-to-analog conversion blocks are designed and inserted between the programmable IC and analog networks in the proposed design.

Finally, the overall architecture of the LD driver is developed as shown in Figure 3-1.

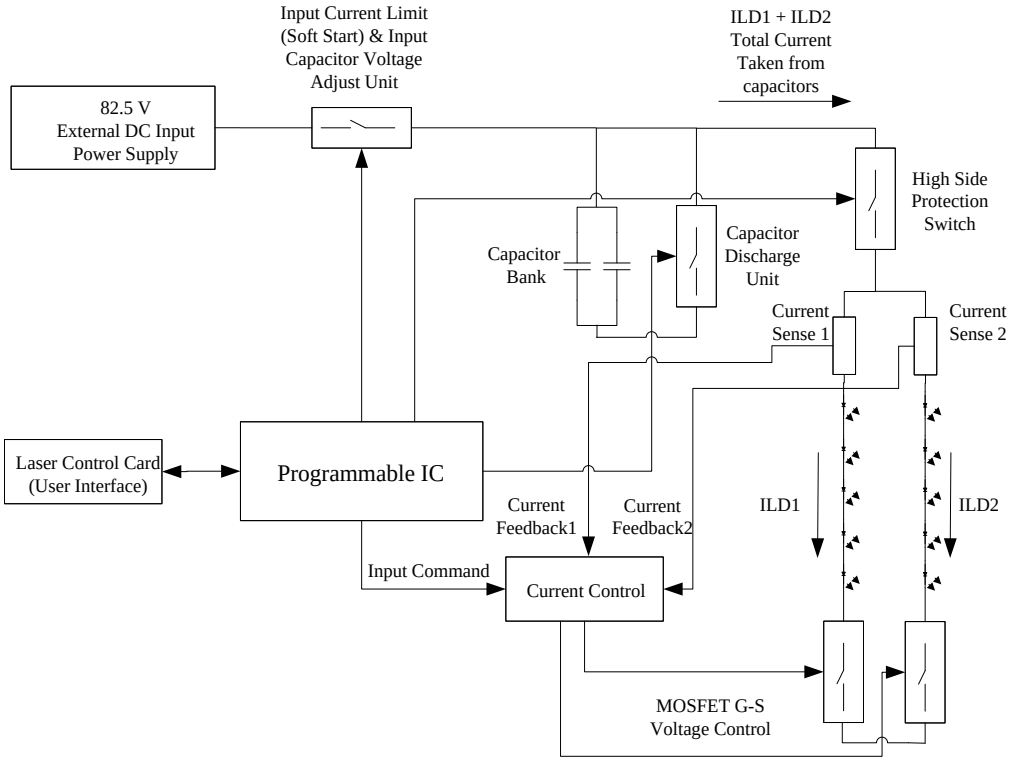


Figure 3-1. The block diagram of the LD driver.

The overall architecture of The LD driver consists of the following sub-blocks:

- Input Current Limiter Network
- Input Capacitor Voltage Adjustment Unit
- Input Capacitor Discharge Unit
- Load Current Measurement Unit
- Analog-to-Digital Conversion Unit
- Digital-to-Analog Conversion Unit
- Protection Circuits

- LD Drive Current Control Unit

The design of each of these sub-blocks will be described in the following sections.

3.2.1 Input Current Limiter Network

The LD driver has been designed so as to provide current pulses with a peak value of 100A for two LD series, each of which comprises five LDs. The peak value of the current can be adjusted by the control unit of the driver within the ranges of 90A to 120A. The width and frequency of the current pulses are nominally 200µs and 20Hz, respectively. The control unit of the driver can adjust these parameters within the ranges of 200µs to 250µs and 20Hz to 40Hz, respectively, via programmable IC.

The electrical specifications of LD indicate that the voltage drop across the terminals of one LD is in the range of 13V to14V in case of current flow within the ranges between 100A and 120A [1]. Hence, the total voltage drop across each five-LD array becomes 65V - 70V. The external power supply which is providing the required power for current pulses can supply maximum 200W output power. On the other hand, the instantaneous power and energy required by two five-LD arrays are calculated as given below:

$$P(t)_{max} = 2 \times i(t) \times V(t) = 2 \times 100A \times 70V = 14kW \quad (3.1)$$

$$E_{max} = 2 \times i(t) \times V(t) \times t = 2 \times 100A \times 70V \times 200\mu s = 2.8J \quad (3.2)$$

As it is observed from above calculations, maximum output power of the external power supply is not sufficient to supply the required instantaneous power for the LD series. Therefore, a capacitor bank is required at the input stage. Necessary input capacitor value can be adjusted by considering the voltage drop on LD array

terminals during a pulse, the voltage droop on drain-to-source terminals of low side MOSFET during pulse and the input voltage value. Since the whole required instantaneous power is supplied by the capacitor bank, it is designed such that voltage droop is small enough to provide current pulse of 100A during 200µs. In other words, the voltage across the terminals of the capacitor bank should still be larger than the voltage drop on LD array terminals during pulse plus the voltage drop on drain-to-source terminals of low side MOSFET at the end of pulse. Besides, the allowable voltage droop has to be considered as 2-5% in the input capacitor voltage. Otherwise, a higher input voltage is required and the input capacitors have to be charged to a higher voltage value. In fact, voltage droop on input capacitors increases the power dissipation on low side MOSFETs since it is directly observed on drain-to-source terminals of low side MOSFETs.

Accordingly, the necessary input capacitance can be calculated as given below [9]:

$$C \geq \frac{(I \times \Delta T)}{\Delta V};\ \Delta V = 2 - 5\% \times VCAP \tag{3.3}$$

Considering the capacitor sizes and secure operation, the voltage droop is considered as 4.5% in the input voltage. Then, minimum required capacitance value for one LD array can be calculated as using (3.3):

$$\Delta V = V_{in} \times 4.5\% = 82.5V \times 4.5\% = 3.7125V \tag{3.4}$$

$$C \geq \frac{(I \times \Delta T)}{\Delta V} = \frac{(100A \times 200\mu s)}{3.7125V} A = 5375\mu F \tag{3.5}$$

As a result, the capacitance value has been determined as 5700 µF and since there are two LD arrays, two capacitors in parallel each of which has a value of 5700µF are used for this purpose. Accordingly, voltage droop on the input capacitors is calculated as 3.5V using the formula (3.3). The specifications of the input capacitors used in the design are shown in Table 3-1.

Table 3-1. Specifications of the input capacitors.

Capacitance Value	5700μF
Maximum Voltage	$100V_{DC}$
Effective Series Resistance (ESR)	50mΩ

These input capacitors have instantaneous low impedance during their initial charge due to their effective series resistance; hence, there occurs an instantaneous high current flow which can result in a reduction in the output voltage value of the external power supply. To prevent this possible failure and protect the output stage of the supply, the input current is limited to 2A by an input current limit network (soft start network), block diagram of which is shown in Figure 3-2. As a result, the protection of input power supply is also maintained, which is not available in other linear current sources that are explained in Chapter 2 as literature survey. If there isn't any self output short circuit protection mechanism of the input power supplies of the other linear current sources maintained in previous chapter, a huge amount of instantaneous current may be demanded by the input capacitors initially and so the absence of the input current limiter network may cause a problem for the safe operation of the input stage of these linear current sources.

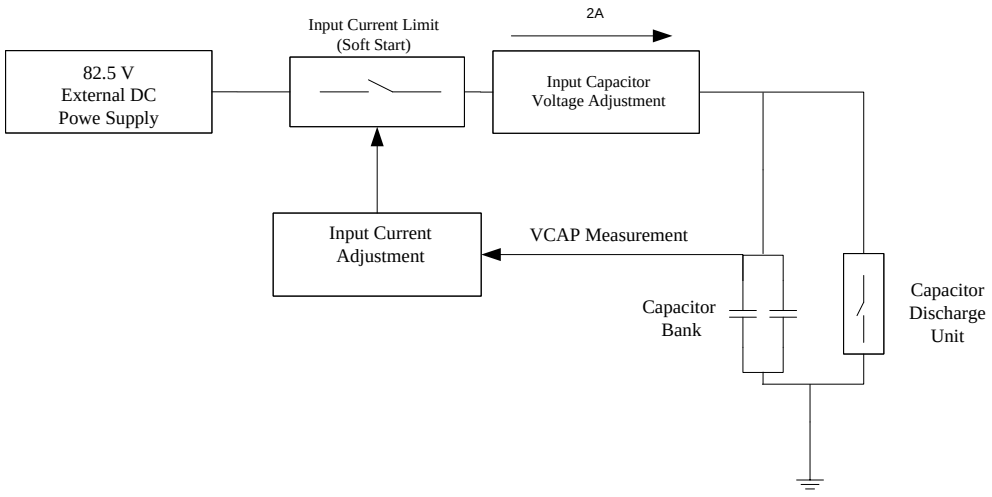


Figure 3-2. Block diagram of the input current limiter network.

3.2.2 Input Capacitor Voltage Adjustment Unit

Input voltage - 82.5V_{DC} is controlled at the input stage of the driver by a MOSFET switch. The unit is designed such that, in case of any failure, this switch is turned off by software so that the input voltage can be interrupted. Besides, the voltage of the input capacitors is adjusted with this switch. If the voltage of the input capacitors is adjusted to a value more than that of the LD series, this results in more power dissipation on low side MOSFETs which are controlling the LD current at the controller stage. Therefore, the voltage of input capacitors can be adjusted to optimum level by determining the average voltage drop on the terminals of the LD series after a few pulses. This mechanism, which is not available in other linear current sources that are covered in previous chapter, aims to decrease the power dissipation on the MOSFETs. The block diagram of the input capacitor voltage adjustment unit that is designed is shown in Figure 3-3.

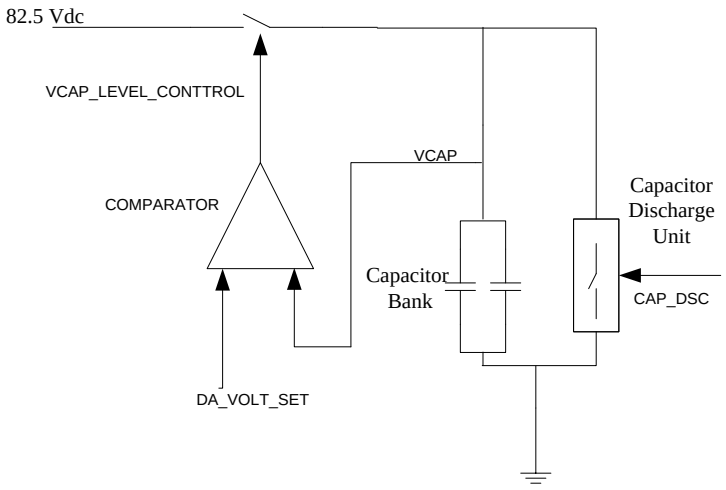


Figure 3-3. Block diagram of the input stage of the driver.

Voltage level of the input capacitors is controlled by the control signal - VCAP_LEVEL_CONTROL in the part of the proposed design, as shown in Figure 3-3.

As shown in the block diagram, level of the input capacitor voltage is adjusted through a signal called DA_VOLT_SET which is an output of the digital-to-analog converter (D/A converter) in the proposed design.

VCAP represents the input capacitor voltage and is compared with DA_VOLT_SET. For instance, if DA_VOLT_SET is set as 3.52V, input capacitor voltage becomes 81.5 V, accordingly.

3.2.3 Input Capacitor Discharge Unit

The input capacitors discharge in case of a failure in the LD current such as a short circuit, an excess current, a reverse current or a failure in the duration and frequency. Figure 3-3 involves the block diagram of the input stage of the proposed design with the input capacitor discharge unit.

According to the block diagram shown in Figure 3-3, the input capacitors discharge through a switch in any of these failure conditions. The switch can be controlled by both software and analog circuitry. During normal operation, the switch is in off mode. In case of a failure detection, the switch is turned on to make the input capacitors discharge through it.

Figure 3-4 shows the ORCAD simulation results related to the input capacitor discharge.

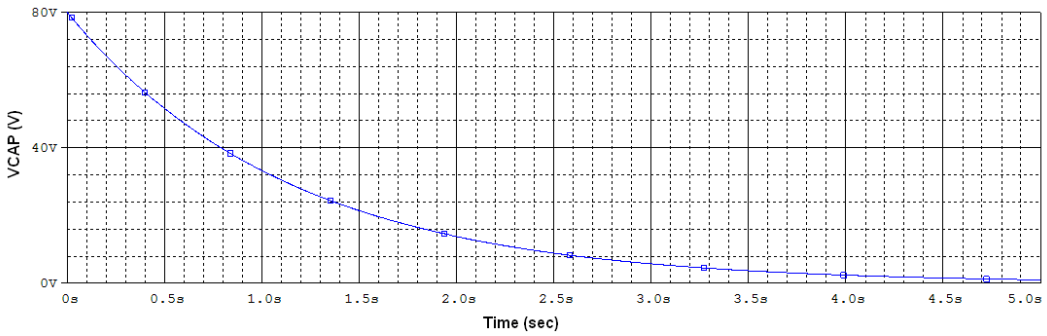


Figure 3-4. Simulation of the input capacitor discharge- Input capacitor voltage vs. time.

3.2.4 Load Current Measurement Unit

It is extremely important to make a precise load current sensing since the control parameter of the driver is the load current. There are two possible LD current measuring devices which are hall-effect sensors or sense resistors. In the proposed method, sense resistors are used for current measurement because they have smaller product sizes, no bandwidth limitation and the property of more accurate measurement when compared to hall-effect sensors.

3.2.4.1 Load Current Measurement with Hall Effect Sensor

Work principle of hall-effect sensors is based on sense of magnetic field created by flowing current. Advantage of using hall-effect sensors is isolation between the sensed current and measurement so that the load current can be sensed from every part of the load current flowing line. On the other hand, disadvantage of using hall-effect sensors is high cost and product sizes. However, alternatives that can be used in similar applications are also considered. Accordingly, products of LEM Corporation are taken into account. These hall-effect sensors are capable of sensing current within the ranges +150A and -150A up to 100KHz bandwidth, which satisfy the requirements of the proposed LD driver [11]. However, they are not used in this driver due to high cost and product sizes.

3.2.4.2 Load Current Measurement with Sense Resistor

Work principle of sense resistor is based on being serially connected to the line of sensed current. Disadvantage of using sense resistor are the difficulty in making measurements in parts of a network which do not have ground reference and power dissipation. Therefore, it is essential to use a sense resistor with a low value so that the voltage drop on it can be minimized. Moreover, tolerance and temperature coefficient of the sense resistor (TCR) must be low. Besides, power rating of the resistor should be high enough to ensure safe operation. Accordingly, determination of the sense resistor is based on the power dissipation formula as given below:

$$P_{diss} = I^2 \times R_{sense} \times Duty\ cycle \tag{3.6}$$

LD current is sensed with 10mΩ sense resistor in the driver as shown in Figure 3-5. Accordingly, maximum voltage drop and power dissipation on the resistor for 40Hz pulse frequency and 200µs pulse duration are calculated as:

$$V_{drop} = I \times R_{sense} = 100A \times 10m\Omega = 1V \tag{3.7}$$

$$P_{diss} = 100A^2 \times 10m\Omega \times {}^{200\mu s}/_{25ms} = 800mW \tag{3.8}$$

Specifications of the sense resistor are given in Table 3-2. The maximum power dissipation calculated in equation (3.8) and the maximum allowed power dissipation given in Table 3-2 show that the sense resistor are operating safely. Moreover, precise measurement of the load current is very critical for the performance of the LD driver. Even, small variations in the value of the sense resistor due to terminal resistance and soldering process may change the value of the resultant load current since the sense resistor also acts as a feedback sensing element in the control loop. Therefore, tolerance and TCR of the sense resistors are determined as very low as given in Table 3-2.

Table 3-2. Specifications of the sense resistor [12].

Resistance Value	10mΩ
Maximum Allowed Power Dissipation at 70 ºC	2W
TCR	2ppm/ºC
Tolerance	0.1%

Voltage drop on the terminals of the sense resistor during pulse is sensed by the difference amplifier. ORCAD simulation results of the above circuit for 100A current pulse are shown in Figure 3-6. It is observed that output of the difference amplifier is measured as 1V for 100A current pulse, which is consistent with the calculation done in equation (2.24).

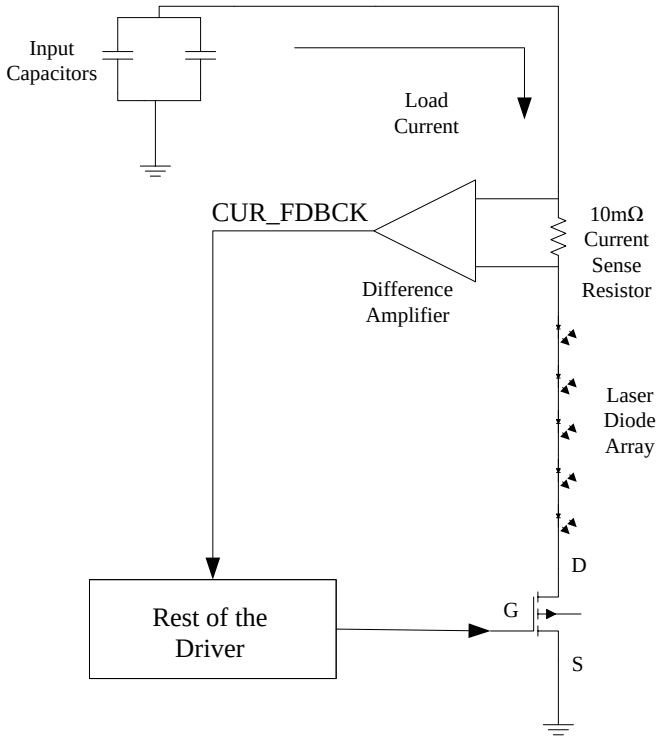


Figure 3-5. Block diagram of the current sense network.

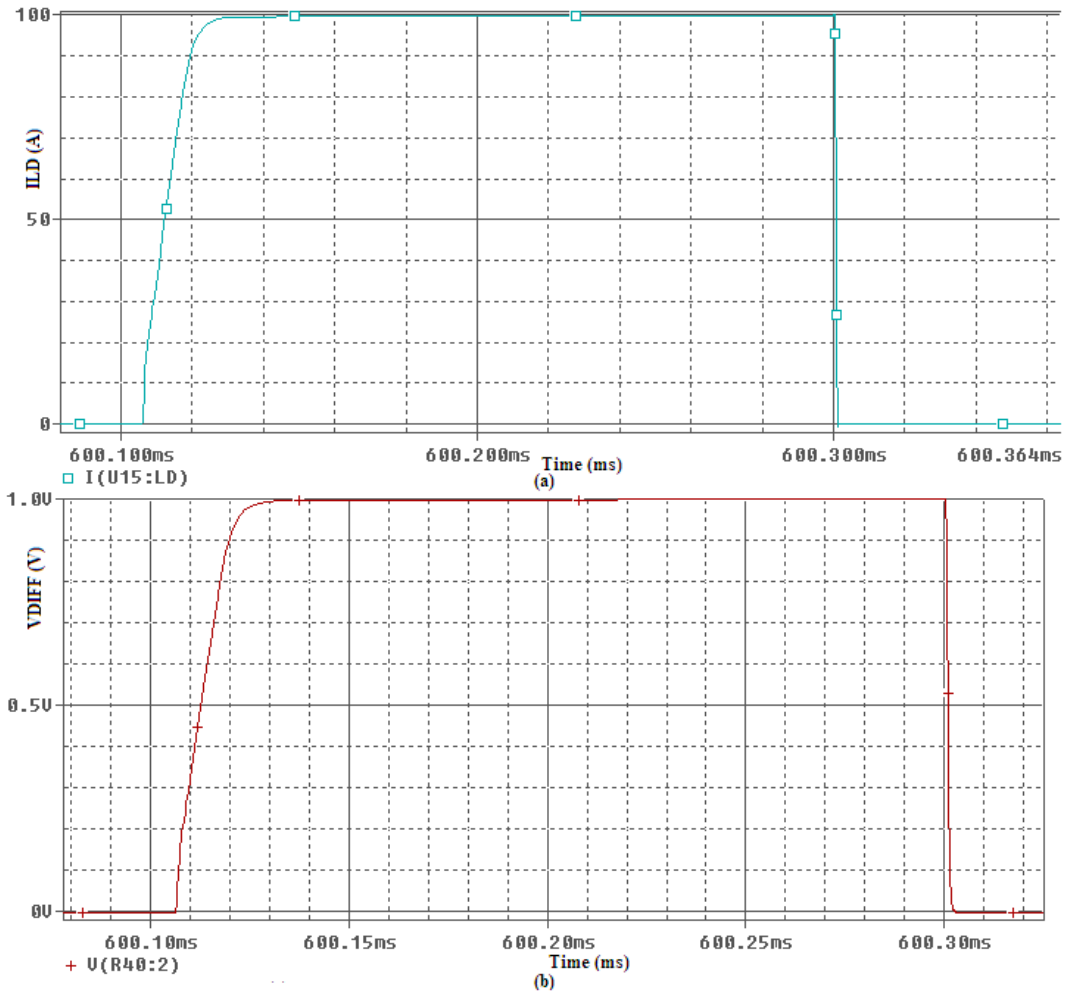


Figure 3-6. ORCAD simulation results of the current sense network – (a) Current flowing through the load vs. time, (b) Output of the difference amplifier vs. time.

3.2.5 Analog-to-Digital Conversion Unit

Analog-to-digital conversion is essential for the interaction between the programmable IC and the analog circuitry of the driver to activate the protection mechanisms of the programmable IC in case of a failure detection in the driver. Therefore, the critical voltages such as input capacitor voltage, voltage of the high side of the LD arrays, voltage drop on drain-source terminals of low side MOSFETs during pulse and the output of the difference amplifier are monitored

and digitized by the A/D conversion unit as shown in Figure 3-7 to detect a possible failure in their values which are explained in details later.

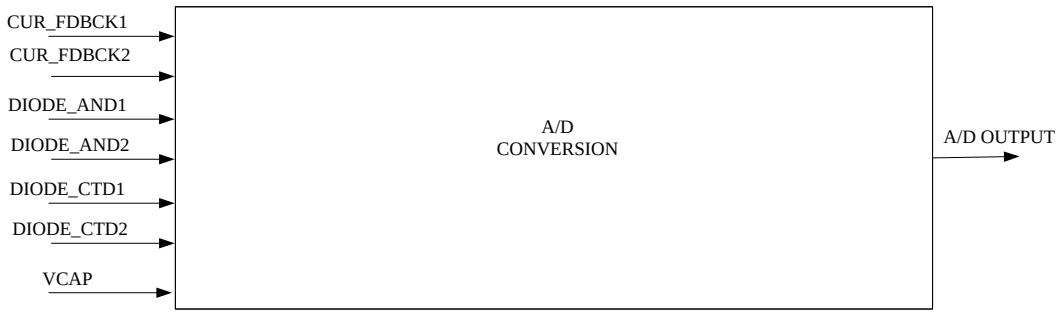


Figure 3-7. Block Diagram of the A/D conversion unit.

Moreover, to provide a fast protection, it is extremely important to get samples of these critical voltages as much as possible and then transfer these samples to programmable IC quickly. Thus, an A/D converter with a high sampling rate is used in LD driver.

3.2.6 Digital-to-Analog Conversion Unit

As it is explained before, the programmable IC is the main control mechanism for the other blocks in the driver. Therefore, digital-to-analog conversion is needed in the driver to transport the instructions of the programmable IC to the other blocks. To meet the needs of the LD driver, a multichannel D/A converter is used in the driver.

The input capacitor voltage is set via software as it is stated previously. The programmable IC determines the voltage level of the input capacitors. This information is converted to an analog signal named as DA_VOLT_SET, which is the input for the input capacitor voltage adjustment unit as shown in Figure 3-3.

Furthermore, the requirements of the LD current pulse are set by the programmable IC. The digital information related to desired current waveform is

converted to an analog signal, which is an input command for the analog PI controller in the LD driver.

3.2.7 Protection Circuits

Protection functions of the driver are activated in case of an excess current flow through and overvoltage across the LD series. The high side protection MOSFET, which is shown in Figure 3-8, is turned off so that input capacitors and LDs can be isolated from each other in protection mode.

Moreover, it is essential to protect the LD series against surge currents that may be coming from the source. This is achieved, in this study, by implementing an isolation stage between the high power supply unit of the driver and the laser diode arrays. There are different approaches in the literature for this problem like the usage of starting prior to firing the diodes as mentioned in [9], [13]. However, the use of soft starting may be very advantageous if it is attached with the external supply to reduce the instantaneous power requirement from the source.

There are both analog and digital protection blocks in the driver. The voltages representing the value of the current flowing through each LD series are compared to a reference voltage by the comparator circuits. The reference voltage is adjusted so as to give an error signal if LD current reaches 130A at the output of the comparators. If the level of the pulsed current flowing through at least one of the LD series exceeds this value, the output voltages of the comparators become logically high. As a result, analog protection block is activated and the high side MOSFET is turned off.

In addition to detection of failure in load current, critical voltages like input capacitor voltage, voltage of the high side of the LD arrays and voltage drop on drain-source terminals of low side MOSFETs during pulse are measured and fed into inputs of the A/D converter. These digitized values are evaluated by the

programmable IC. If these values are out of the ranges which are predetermined by the programmable IC, the high side protection MOSFET is immediately turned off to interrupt current pulses to flow through the LD arrays and input capacitors are discharged by input capacitor discharge unit which is shown in Figure 3-3.

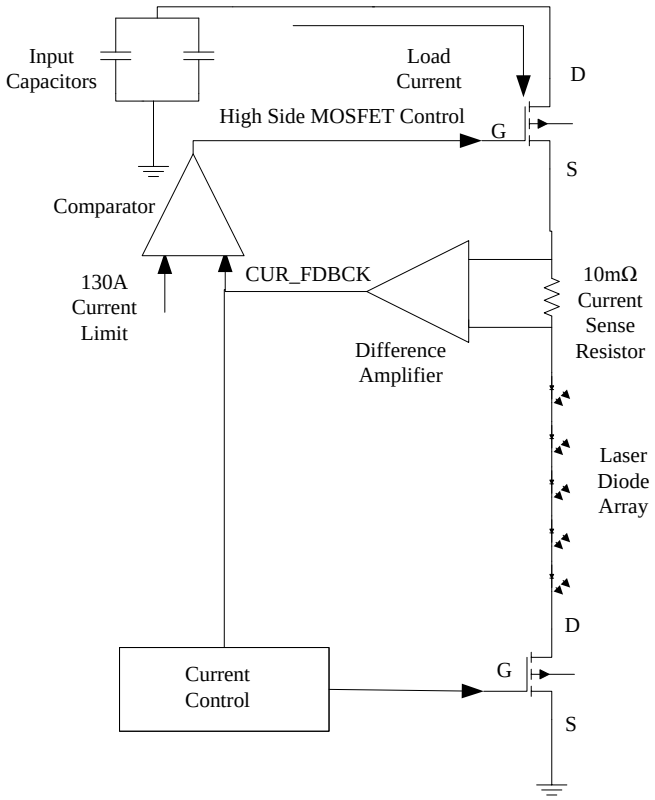


Figure 3-8. Block diagram of the driver with high side protection MOSFET.

3.2.8 LD Drive Current Control Unit

The pulsed laser diode driver utilizes a linear current source topology with PI controller. The driver is capable of controlling the current flowing through two LD series with two identical op amp based analog PI controllers.

3.2.8.1 Analog PI Controller for LD Current

There are two analog PI controllers implemented in the design to drive two LD series. Each analog PI controller adjusts the level of the current through two laser diode series by controlling the voltage across the gate-source terminals of low side MOSFETs according to current level command set by the programmable IC. The current command involves the information of the desired level of current, frequency and the pulse width.

In the driver, currents through each laser diode series are sensed by the series sense resistors. The sensed currents which are amplified and filtered are used as feedback signals. In each loop, the error signal is used as the input for the controller which reduces the error to zero at steady-state. Figure 3-9 shows the block diagram of the closed loop system implemented with analog PI controller.

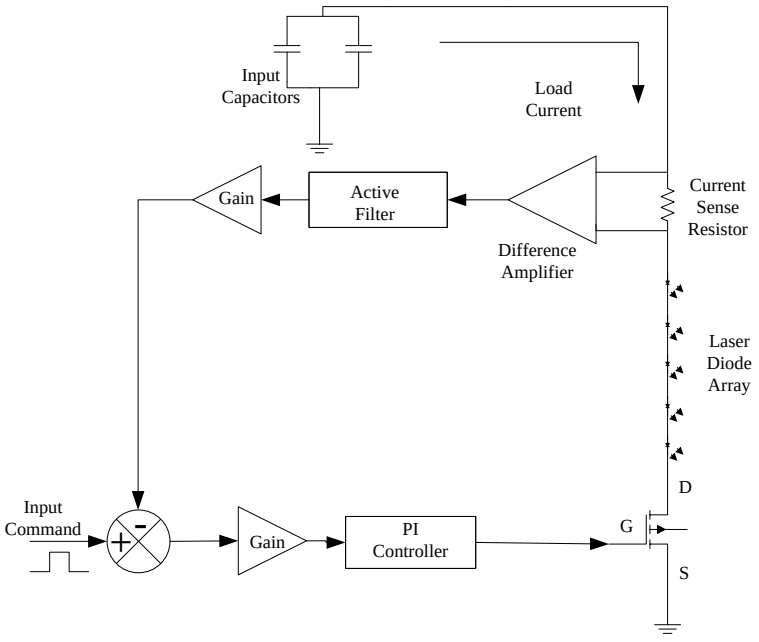


Figure 3-9. Block diagram of the closed loop system implemented with analog PI controller.

As it is stated before, input current command involves the level of the desired current level, current pulse duration and current pulse frequency. For instance, an

input command with 1.5V amplitude and 200µs pulse duration is required to obtain a load current with 100A and 200µs pulse width. Figure 3-10 shows the PI controller and gain stage for one LD series. The signal named as CUR_FDBCK1 represents the feedback signal. On the other hand, the signal named as IREF1 determines the level of the pulse command. Frequency and width of the current pulse are controlled by the signal named as IREF_CONTROL1 which drives the gate of the MOSFET - TR602 as shown in Figure 3-10. When the signal - IREF_CONTROL1 is logically high, the voltage observed at the drain of the transistor becomes logically low. As a result, there is no input command applied to the control loop. However, when the signal - IREF_CONTROL1 is logically low, the signal - IREF1 is applied to the drain of the MOSFET - TR600. Consequently, the input command is applied to the controller.

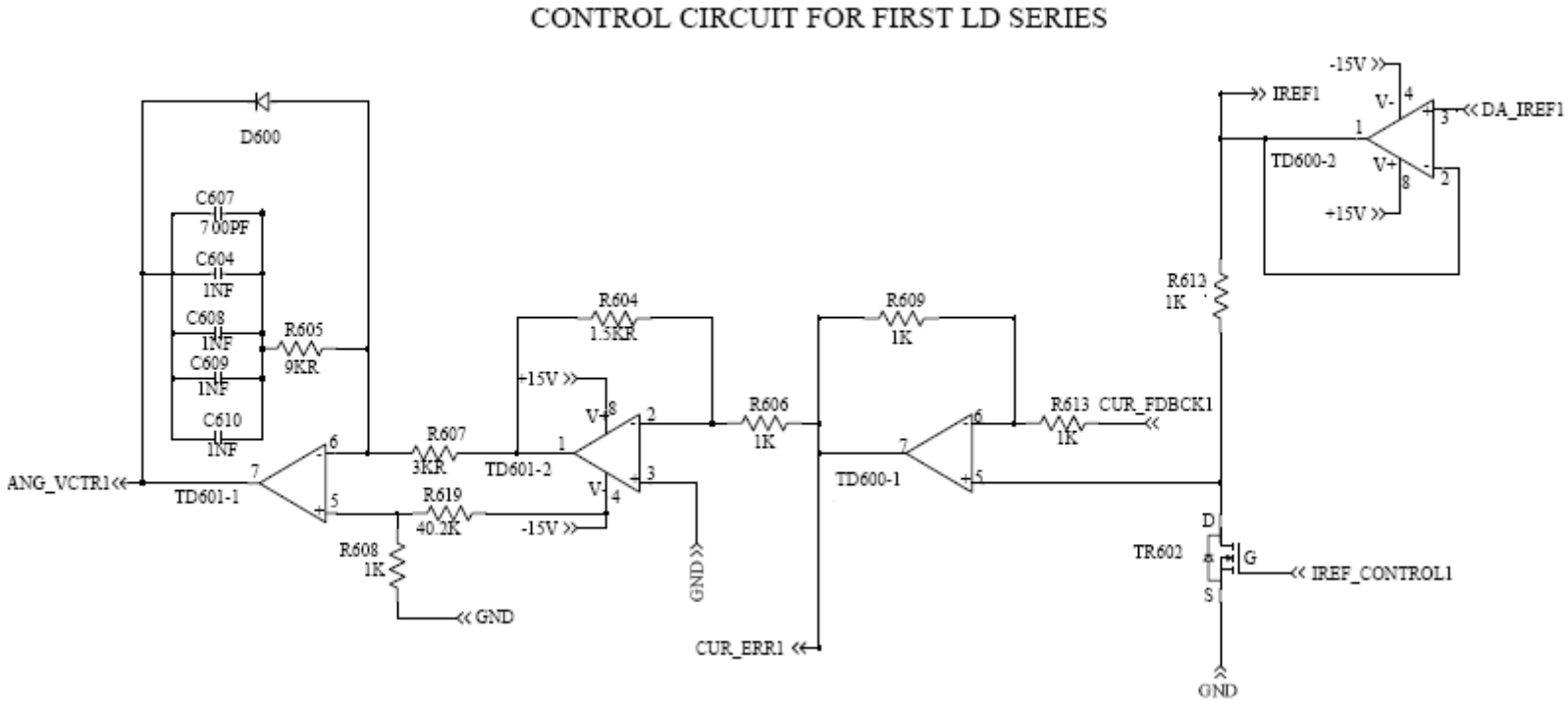


Figure 3-10. Schematic of the analog PI controller and the gain stage of the driver.

The goal of the design shown in Figure 3-10 is to make the error signal - CUR_ERR1 zero at steady-state. The op-amp – TD600-2 operates as an error amplifier. Output of the op-amp is considered as the error signal and equals to twice the input command minus current feedback signal. Then, the error signal is amplified and inverted at the second op-amp stage with a gain number (+1.5). The output of the second op-amp stage is the input for the PI controller which drives the gate of the low side MOSFET. The resistance and capacitance value of the closed loop current controller is determined via the ORCAD simulations shown in following figures. Finally, the equation of the gate driving signal in response to the error signal is:

$$V_{gate-drive}(t) = K_p \times e(t) + K_i \times \int e(t)dt \tag{3.9}$$

where K_p and K_i are the resultant proportional and integral constants, respectively. K_p, K_i and the error signal - e(t) are calculated as given in below:

$$K_p = \frac{R604}{R606} \times \frac{R605}{R607} = \frac{1.5k\Omega}{1k\Omega} \times \frac{9k\Omega}{3k\Omega} = 4.5 \tag{3.10}$$

$$K_i = \frac{R604}{R606} \times \frac{1}{R607 \times C_{eq}} = \frac{1.5k\Omega}{1k\Omega} \times \frac{1}{3k\Omega \times 4.7nF} = 106029 \tag{3.11}$$

$$e(t) = \frac{R609+R613}{R613} \times input\ command\ - \frac{R609}{R613} \times CURR\_FDBCK1 \tag{3.12}$$

$$e(t) = \frac{1k\Omega+1k\Omega}{1k\Omega} \times input\ command\ - \frac{1k\Omega}{1k\Omega} \times CURR\_FDBCK1 \tag{3.13}$$

Initially, output of the PI controller reaches the positive saturation voltage value of the op-amp as shown in Figure 3-11. Then, it decreases and reaches to the steady-state value. Therefore, it is essential to charge the gate of the low side MOSFET slowly enough not to cause oscillations in the load current. Hence, the gate of the low side MOSFET is driven through a resistor as shown in Figure 3-12.

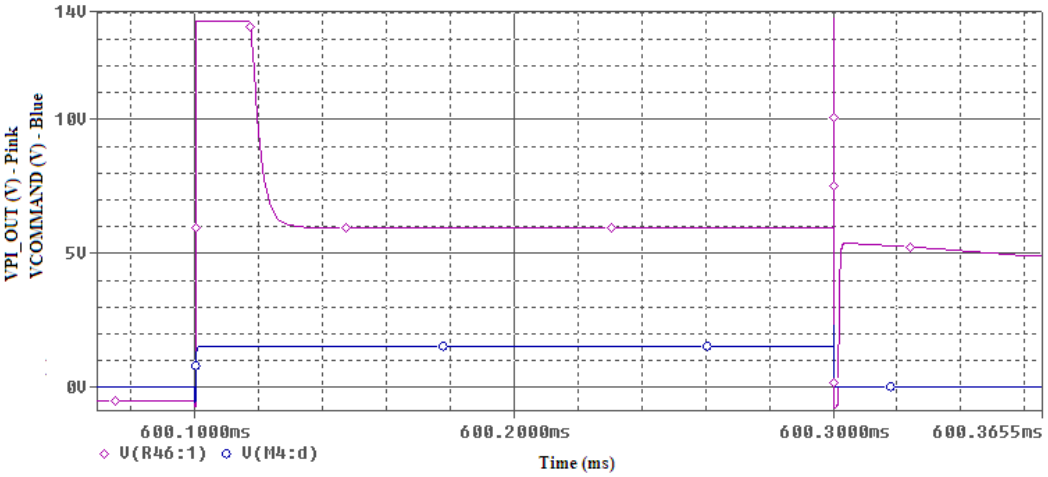


Figure 3-11. ORCAD simulation of the output of the PI controller in response to the input command for 100A LD current with 200µs pulse width – PI controller output vs. time (Pink), Input command vs. time (Blue).

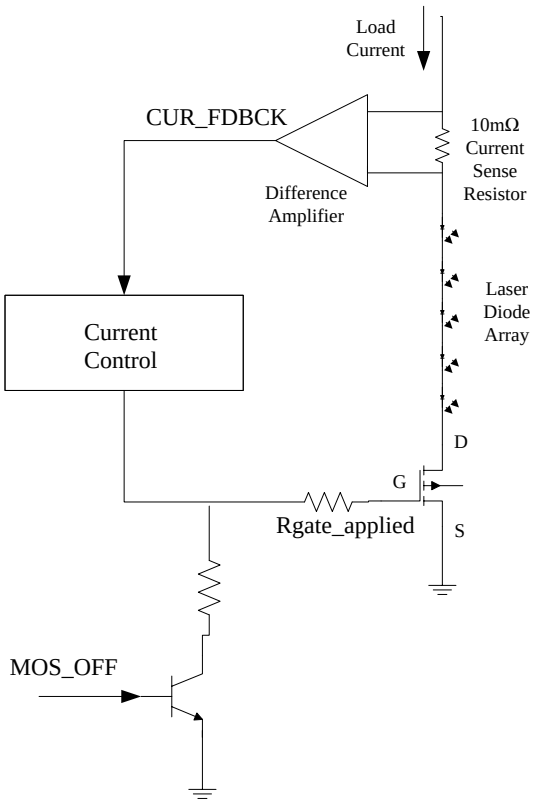


Figure 3-12. Block diagram of the gate drive circuit of the low side MOSFET.

3.2.8.2 Determination of Rise and Fall Times of the LD Current

There are several factors affecting the rise and fall times of current pulses. One of them is the MOSFET capacitances which are named as input capacitance - C_{iss}, output capacitance - C_{oss} and reverse transfer capacitance - C_{rss}. These capacitances are defined as shown below:

$$C_{iss} = C_{GS} + C_{GD} \tag{3.14}$$

$$C_{oss} = C_{DS} + C_{GD} \tag{3.15}$$

$$C_{rss} = C_{GD} \tag{3.16}$$

where C_{GS}, C_{GD} and C_{DS} are the gate-to-source capacitance, the gate-to-drain capacitance and the drain-to-source capacitance of a MOSFET, respectively.

In addition to these capacitances, parasitic inductances due to MOSFET packaging increases turn on and turn off time of a MOSFET during switching [14]. Figure 3-13 shows equivalent model of a MOSFET with components having major effect on switching times.

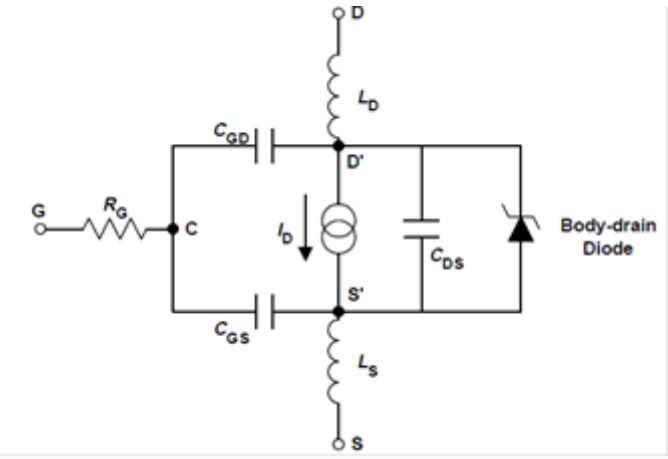


Figure 3-13. Equivalent MOSFET model [15].

Moreover, PCB trace inductance and series inductance of LD series which are in the order of nanoHenry affect the switching behavior of MOSFETs in my experience. Indeed, voltage drop on these parasitic components during switching increases current rise and fall times. As a result, it is extremely difficult to calculate rise and fall times of MOSFETs during switching. However, there are some approximations using the MOSFET datasheet parameters for calculation of current rise and fall times. However, these parameters are dynamic. Therefore, the approximations made on the equations which are taken from [15] give general idea about the switching behavior of MOSFETs. In fact, it is already stated that there is difference between calculated values and measured values of turn on and turn off times of MOSFET [14].

Before dealing with the calculations, it will be helpful to mention the switching behavior of MOSFETs. Figure 3-14 illustrates the general turn on characteristic of a MOSFET. Accordingly, when a step input is applied to gate of the MOSFET, C_{GS} and C_{GD} are started to be charged by the gate current and the gate voltage of the MOSFET increases. However, the MOSFET is still turned off until the gate - source voltage of the MOSFET (V_{GS}) reaches the threshold voltage. Elapsed time during this period is named as t_1 in Figure 3-14. Actually, this period can be considered as the dead time for the MOSFET. This means that when a step input is applied to the gate of the MOSFET, there will always be a time gap between the rising edges of the step input and the current flowing through drain – source terminals of the MOSFET (I_{DS}). Therefore, this dead time has to be added to the width of the input pulse command applied to the controller to compensate this gap. Accordingly, as V_{GS} reaches the threshold voltage, I_{DS} begins to rise and V_{GS} still goes on increasing until reaching Miller plateau voltage. At the same time, I_{DS} reaches the steady-state value. Elapsed time during this period is called as current rise time and calculated as $(t_2 - t_1)$ according to Figure 3-14. After the completion of this period, V_{GS} remains constant for a while. During this period, only C_{GD} is charged by the gate current. Elapsed time is calculated as $(t_3 - t_2)$ during this period. At the end, V_{GS} begins to increase again until reaching the steady-state

value. These turn on time periods of the MOSFET are calculated using the parameters taken from the application note - [14]:

$$t_1 = \left(R_G + R_{G\_applied}\right) \times C_{iss} \times \ln\left[\frac{1}{\left(1 - \frac{V_{GS(th)}}{V_{GS(step)}}\right)}\right] \tag{3.17}$$

$$t_2 = \left(R_G + R_{G\_applied}\right) \times \ln\left[\frac{1}{\left(1 - \frac{V_{GS(miller)}}{V_{GS(step)}}\right)}\right] \tag{3.18}$$

$$t_3 = \frac{(V_{DS} - V_F) \times \left(R_G + R_{G\_applied}\right) \times C_{rss}}{V_{GS(step)} - V_{GS(miller)}} \tag{3.19}$$

where $R_{G\_applied}$ is the value of the resistor externally connected to the gate of the MOSFET, and V_{DS}, $V_{GS(th)}$,$V_{GS(miller)}$ and V_F are the drain-to-source voltage of the MOSFET during turn off , the threshold turn on gate-to-source voltage of the MOSFET, the Miller charge voltage of the MOSFET and the drain-to-source voltage of the MOSFET during turn on, respectively.

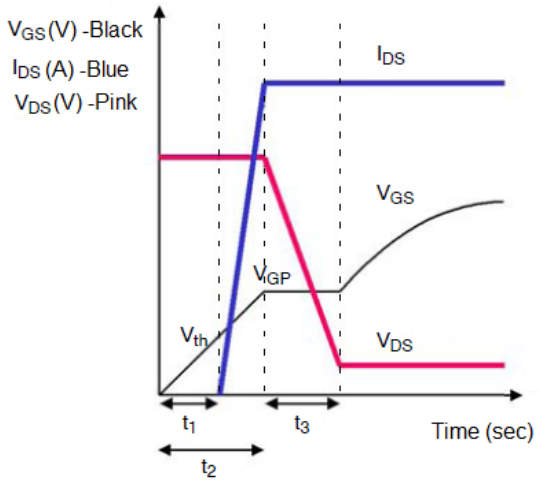


Figure 3-14. General turn on characteristics of MOSFETs.

According to the simulation results, $R_{G\_applied}$ is determined as 1.33kΩ and used as shown in Figure 3-12. Moreover, parameters of the MOSFET used in the driver which are taken from [16] are given as below:

$R_G = 1.5\Omega$ $\quad$ $V_{GS(th)} = 2.5V(min)$ & $5V\ (max)$

$C_{iss} = 32nF$ $\quad$ $V_{GS(miller)} \cong 5.1V$

Typical $V_{GS(th)}$ value is 4.2V according to the spice model of the MOSFET. Moreover, since the output of the PI op-amp saturates, $V_{GS(step)}$ is considered as the op-amp output saturation voltage which is approximately 13.6V according to the simulation results shown in Figure 3-15. Then, turn on time periods of the MOSFET can be calculated as below:

$$t_1 = (1.5\Omega + 1.33k\Omega) \times 32nF \times \ln\left[\frac{1}{\left(1-\left({}^{4.2V}/_{13.6V}\right)\right)}\right] \cong 15\mu s \qquad (3.20)$$

$$t_2 = (1.5\Omega + 1.33k\Omega) \times 32nF \times \ln\left[\frac{1}{\left(1-\left({}^{5.1V}/_{13.6V}\right)\right)}\right] \cong 20\mu s \qquad (3.21)$$

Therefore, width of the input pulse command applied to the controller has to be adjusted as 15μs more than its actual value, which can be done by the programmable IC easily. For instance, if desired width of the current pulses is 250μs, the programmable IC has to provide pulse commands with 265μs width. Besides, expected rise time of the current pulses is 5μs according to above results. On the other hand, the simulation results show that rise time is approximately 9μs as shown in Figure 3-18. This is due to the fact that parasitic package inductances of the MOSFET which is not modeled in its spice model and PCB trace inductance which is not also considered in ORCAD simulations are not taken into account in these equations.

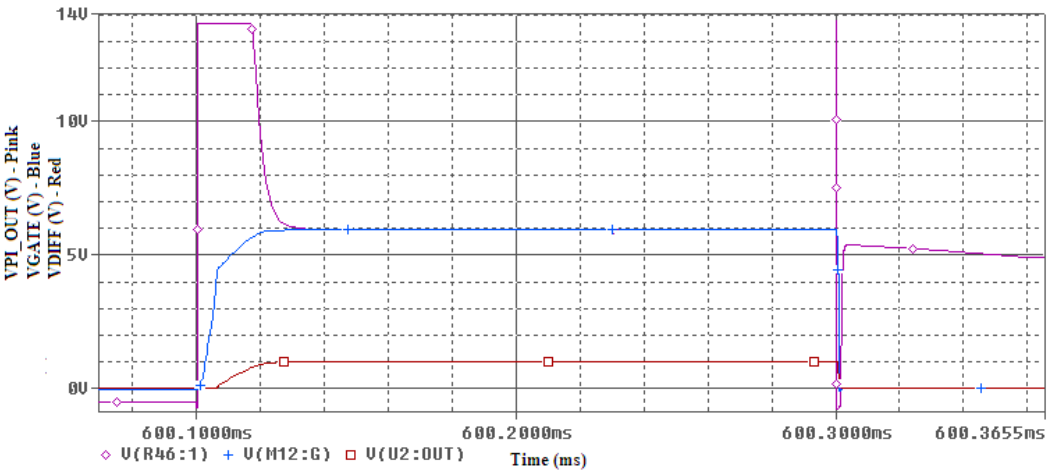


Figure 3-15. ORCAD simulations of the actual system, PI controller output (Pink), Gate voltage of the low side MOSFET (Blue), Output of the difference amplifier in response to 100A LD current (Red).

Turn off characteristic of the MOSFET is similar to its turn on characteristic. As the step input voltage applied to the gate of the MOSFET drops to zero, C_{GD} and C_{GS} of the MOSFET start to be discharged until V_{GS} of the MOSFET drops to Miller plateau voltage. After reaching Miller plateau voltage, V_{GS} of the MOSFET remains constant for a while. During this period, only C_{GD} of the MOSFET goes on being discharged. Then, V_{GS} starts to decrease again since C_{GD} and C_{GS} are further to be discharged and so current flowing through the load starts to decrease. This turn off characteristic of the MOSFET is described in Figure 3-16. Fall time of the load current is mentioned as t_6 in the corresponding figure. It can be calculated approximately as, [14]:

$$t_6 = \left(R_G + R_{G\_applied}\right) \times C_{iss} \times \ln\left(\frac{V_{GS(miller)}}{V_{GS(th)}}\right) \tag{3.22}$$

$$t_6 = (1.5\Omega + 1.33k\Omega) \times 32nF \times \ln\left(\frac{5.1V}{4.2V}\right) \cong 8.26\mu s \tag{3.23}$$

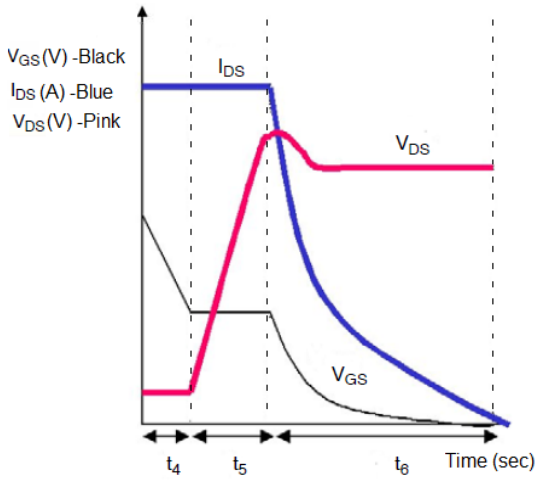


Figure 3-16. General turn off characteristics of MOSFETs

Although the calculated fall time is less than 10µs, simulation results show that it is more than 10µs without additional gate discharge circuit as shown in Figure 3-17. Indeed, measured fall time is 18µs for this case due to the parasitic package inductances of the MOSFET.

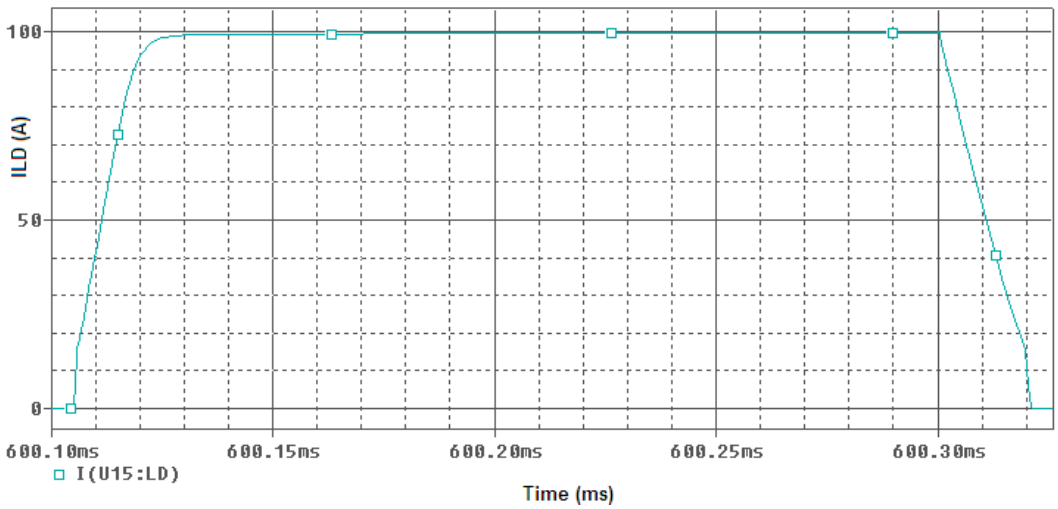


Figure 3-17. ORCAD simulation of the load current without gate discharge unit.

To decrease the fall time of the load current, an additional gate discharge circuit is designed for the driver. This circuit is a simple inverter providing an additional path for gate discharge at the end of current pulse and comprising an npn type BJT transistor and resistors and connected between gate terminal of the low side

MOSFET and ground as shown in Figure 3-12. Base emitter voltage of the BJT transistor is controlled by the software. Indeed, a signal which is synchronous to the input current pulse command and inverted version of the input pulse command is applied to base of the transistor during operation. For example, while an input pulse command is applied to provide required level of current pulse flowing through the load, logical level of the signal which is applied to the base of the BJT transistor becomes low so that collector voltage of the BJT transistor voltage can stay logically high during pulse and be equal to the gate voltage of the low side MOSFET. At the end of the pulse, logical level of the signal applied to the base of the transistor becomes logically high. Accordingly, collector voltage of the BJT which is also equal to gate voltage of the low side MOSFET drops to zero abruptly which results in a lower fall time for the current pulse. Simulation of the load current with this additional gate discharge circuit is shown in Figure 3-18. Simulation results show that fall time of the current pulse is decreased to 0.55µs.

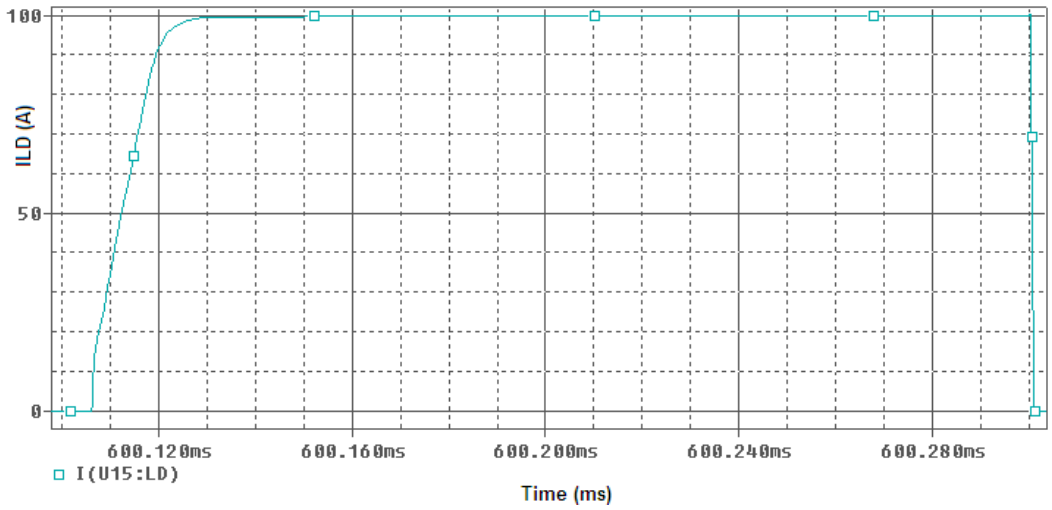


Figure 3-18. ORCAD simulation of the load current with additional gate discharge unit.

Moreover, value of the C_{iss} of the MOSFET is given as 32nF which is extremely high and a limiting factor for decreasing the rise time of the current and directly depends on the package dimensions of the MOSFET. It is important to mention that the linear current source design with PID controller, which is mentioned in previous chapter, is said to provide rise and fall times less than 5µs [9]. Even, this

fall time condition is satisfied with the additional gate discharge circuit, rise time cannot be decreased to 5µs due to the limiting MOSFET factor in this driver because while the design with PID controller utilizes multiple numbers of parallel power MOSFETs in the controller stage, this design utilizes only one power MOSFET for control of each LD array. The design with PID controller decreases the power requirements of MOSFETs and so required package dimensions by distributing the load current among them. However, using such a parallel MOSFET network increases the required PCB dimensions for the driver. To conclude, there is a trade-off between providing smaller rise times and smaller PCB dimensions for multiple numbers of parallel power MOSFET usages.

3.2.8.3 Specific Problems met in the Analog PI Controller Design

It is observed that the op-amps used in the controller affected the performance of the LD driver in this work. First of all, op-amps must have large enough bandwidth and slew rate not to cause any delay in the controller. Since the minimum bandwidth of the system is 100KHz, bandwidth of these op-amps has to meet this requirement. Moreover, at the output stage, response time of the op-amps must be low enough to respond to abrupt input voltage changes. In this application, since the measured load current is fed into the controller, slew rate of these op-amps must be large enough to catch the changes in the load current during rise and fall. Accordingly, high speed op-amps with 50MHz bandwidth and 350V/µs slew rate are used in the driver. However, op-amp input offset voltage is still a big problem for the controller although the op-amps used in this application have low input offset voltage which is given in the range of 0.5mV and 2mV in [17]. This amount of voltage may not be effective on the performance of the controller. Nevertheless, there are six consecutive op-amp stages comprising filtering, gain and PI controller blocks in each closed loop. Indeed, op-amp input offset voltage creates an offset voltage at the output of the corresponding op-amp, which is an additional input offset voltage for the following op-amp. Finally, at frond end of the PI controller, op-amp input offset

voltages may create a remarkable voltage. Since the PI controller has a large gain, resultant offset voltage may charge the gate of the low side MOSFETs and cause a few amperes continuous DC current flow through the LD arrays despite the absence of the current command. Therefore, an external negative offset voltage is applied to the non-inverting input of the op-amp used in PI controller to make offset cancellation as shown in Figure 3-10. To determine the value of the required negative input offset voltage, it is important to consider the op-amp model with input offset voltage and make calculations for the worst case to obtain possible highest total offset voltage for the controller stage. General op-amp model with input offset voltage is shown in Figure 3-19.

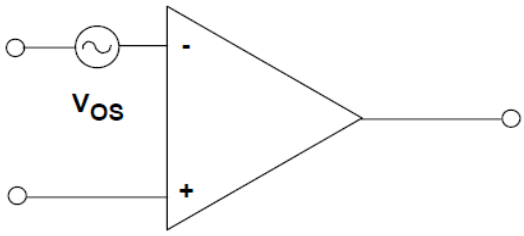


Figure 3-19. Op-amp model with input offset voltage [18].

In each closed system, there are six amplifier stages, one of which is the difference amplifier having 1mV offset voltage, which is defined in [19]. Considering the schematics including the amplifiers used in the closed loop system and shown in the Figure 3-5, Figure 3-7 and Figure 3-10, overall offset model of the closed system for the worst case can be described as shown in Figure 3-20.

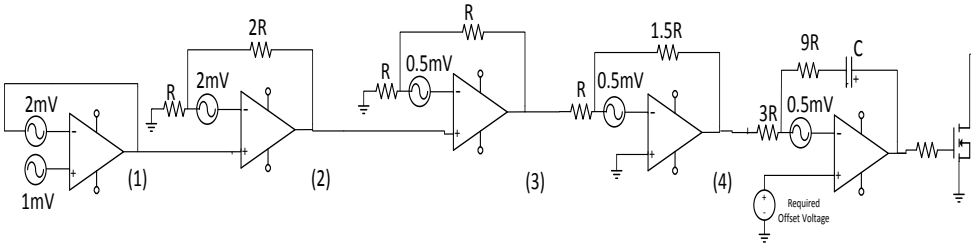


Figure 3-20. Overall offset model of the closed loop system for the worst case.

Total offset voltage of the closed loop system can be calculated step-by-step as indicated below where the numbers (1), (2), (3) and (4) represents the op amps used in Figure 3-20:

(1) $$1mV + 2mV = 3mV \tag{3.24}$$

(2) $$3mV + \frac{(2R+R)}{R} + 2mV \times \frac{(2R+R)}{R} = 15mV \tag{3.25}$$

(3) $$15mV \times \frac{(R+R)}{R} + 0.5mV \times \frac{(R+R)}{R} = 31mV \tag{3.26}$$

(4) $$31mV \times (-1) \times \frac{1.5R}{R} + 0.5mV \times \frac{(1.5R+R)}{R} = -45.25mV \tag{3.27}$$

The effect of the op-amp offset voltages is tested in ORCAD simulations. Figure 3-21 shows that the total calculated offset voltage is large enough to saturate the op-amp used in the PI controller and to cause a few amperes continuous current through the LD arrays despite the absence of the input command.

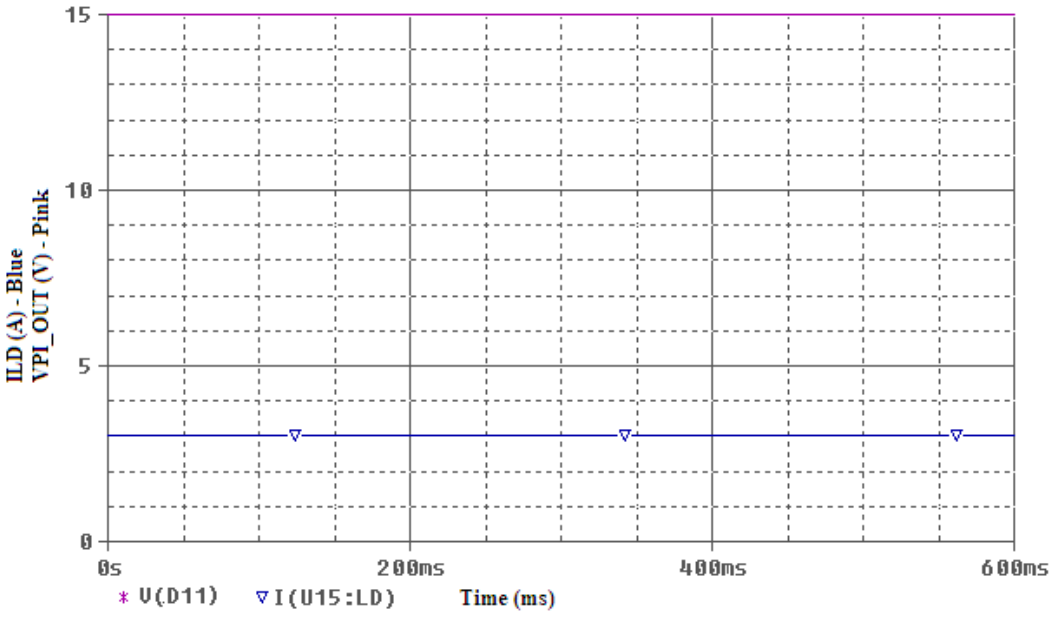


Figure 3-21. ORCAD simulations showing the effect of the op-amp offset voltage on PI output and LD current.

Considering the gain parameter of the PI controller, the required negative offset voltage that has to be applied to the non-inverting input of the op-amp to cancel the total offset voltage is calculated as shown below:

$$-45.25mV \times (-1) \times \frac{9R}{3R} + 2mV \times \frac{(9R+3R)}{3R} = 143.75mV \quad (3.28)$$

$$V_{required_{offset}} \times \frac{(9R+3R)}{3R} = 143.75mV \Rightarrow V_{required\_offset} \cong 35.9375mV \quad (3.29)$$

The drawback of applying negative input offset voltage is that it can negatively charge the gate of the low side MOSFET if the value of the offset voltage at front end of the PI controller is lower than the value calculated in (3.41). However, this problem is overcome by putting a diode between the inverting input and output of the op-amp used in the PI controller as shown in Figure 3-10.

3.2.8.4 MATLAB Analysis of the Analog PI Controller

The analog PI controller simulated via ORCAD is analysed via MATLAB program. First of all, the controller circuit is simulated via *Simscape* tool of the program. The spice model of the low side MOSFETs is used for the general MOSFET model in the tool to see whether the simulation results are compatible to each other. However, a constant power supply is used in the analysis instead of a capacitor bank, because the only purpose is to see the performance of the controller. In the analysis, 0.7Ω - resistive load, the value of which is determined using the I-V characteristics of the LD arrays, is used instead of the LDs in the analysis.

The parameters of the load current are chosen as similar to the once determined in ORCAD analysis. The corresponding *Simscape* simulation results are illustrated in Figure 3-22. The waveforms validate the results obtained in ORCAD simulations. When an input pulse command with 1.5V amplitude is applied to the

controller, a voltage pulse with 1V amplitude is observed at the output of the subtractor amplifier as shown in Figure 3-22, which means that there is 100A current pulse through the load. The voltage waveform of the PI controller output and the gate voltage of the low side MOSFET, which are shown in Figure 3-22, almost agree with the results shown in Figure 3-15.

In addition to the *Simscape* simulation analysis, the overall control block is modelled in MATLAB. The complexity in modelling the overall system is the modelling of the low side MOSFET. As it is explained previously, MOSFETs are non-linear devices, parameters of which are directly affective on the transient response of the system and determination of the PI controller parameters. Due to their non-linearity, it is almost impossible to create a generalized model. Instead, there are two different approaches tried in the analysis to obtain an approximated controller model. The first approach is that considering the steady-state response of the system, the low side MOSFETs are assumed to be operating in linear region. According to this assumption, an operating point is determined with the help of ORCAD simulation results as shown in Figure 3-23. Because, the MOSFETs are considered as variable resistors according to the voltage applied to gate-source terminals in linear region, an approximate and linear V_{GS} dependent $R_{DS(ON)}$ (drain-to-source resistance) function is obtained.

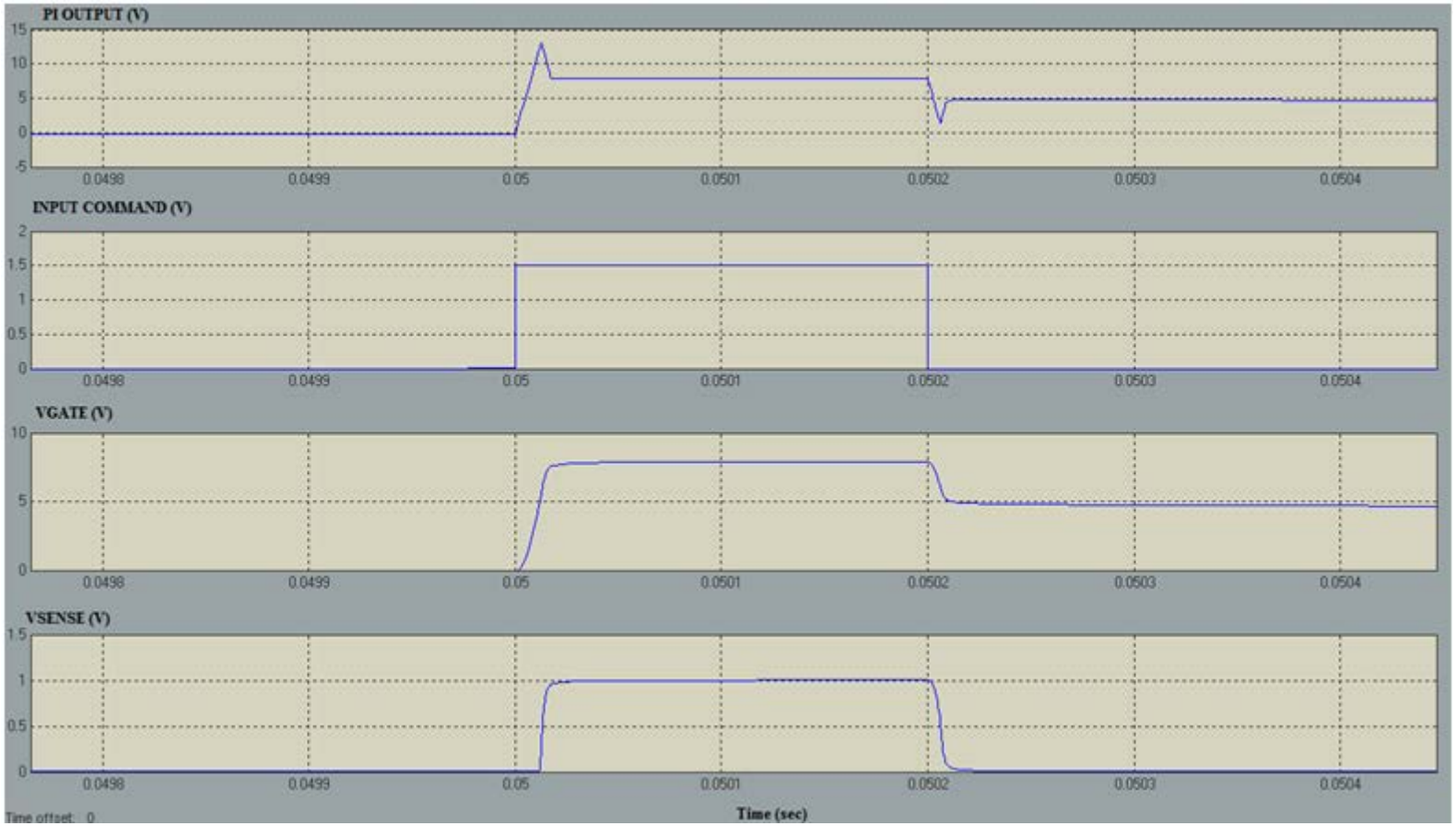


Figure 3-22. Simscape simulation results for 100A load current for 200µs duration of pulse.

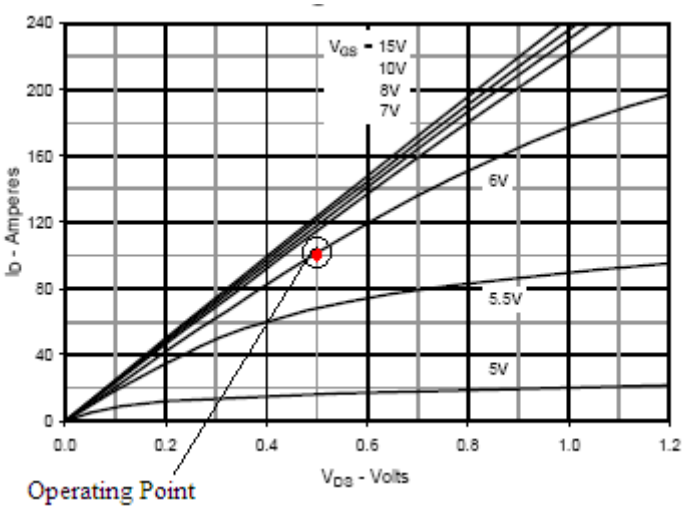


Figure 3-23. I_D vs. V_{DS} characteristics of the low side MOSFETs. [19].

Using the selected operating point, corresponding $R_{DS(ON)}$ is calculated as 0.005Ω (since V_{DS}=0.5Vand I_D=100A for V_{GS}=6V.). To write $R_{DS(ON)}$ as a linear function of $V_{GS,}$ we need another operating point within the neighbourhood of the previous point. For 110A - I_D and 0.5V - $V_{DS,}$ $R_{DS(ON)}$ is calculated as 0.0045Ω. Using this information, the coefficients of the $R_{DS(ON)}$ is calculated as:

$$R_{DS(ON)} = f(V_{GS}) = a \times V_{GS} + b \tag{3.30}$$

$$0.005\Omega = f(V_{GS}) = a \times 6V + b \tag{3.31}$$

$$0.0045\Omega = f(V_{GS}) = a \times 7V + b \tag{3.32}$$

$$a = -0.0005\Omega/V\,, \quad b = 0.008\Omega \text{ and } f(V_{GS}) = -0.0005 \times V_{GS} + 0.008 \tag{3.33}$$

Considering the load as a resistive load, the value of which is determined as 0.7Ω from the current through and the voltage drop across the terminals of the one LD array, the system model can be approximated around the operating point as follows:

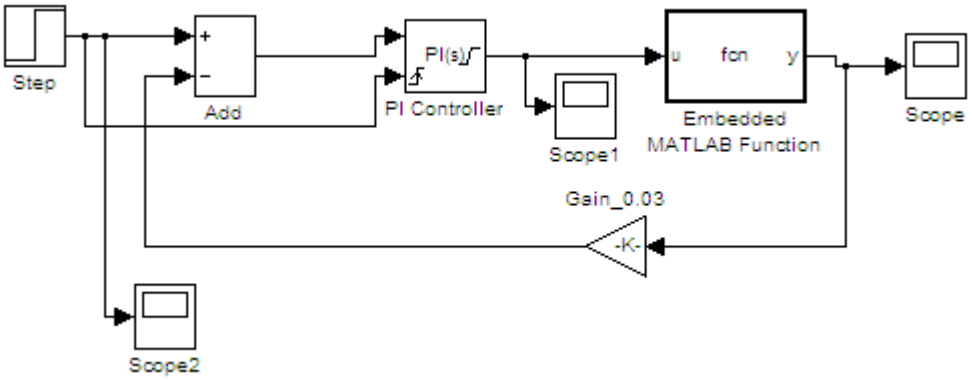


Figure 3-24. Variable resistance approximation based Simulink model for the controller.

The proportional constant (K_p) and the integral constant (K_i) of the PI controller are determined as 4.5 and 106029 respectively from the ORCAD simulation results. Load current function is written in "Embedded MATLAB Function" as follows:

```
function y = fcn(u)
%u      : VGS; Rload=0.7ohm
%70V    :the voltage drop across the load for 100A
%0.5V   :the voltage drop across
%drain-source terminals of the low side MOSFET
%y      : IDiode; Rds_on=0.001*(8-0.5*VGS)
y = 70.5/(0.7+(0.001*(8-0.5*u)));
```

The response of the system to 3V - step input is shown in Figure 3-25. The results seem to be consistent with the determined operating point. However, the overall model shown in Figure 3-24 is approximated around a fixed operating point and since it is still a non-linear model, it is difficult to generalize it for other operating points. In fact, a new load current function has to be written in the "Embedded MATLAB Function" because the load is determined as a resistive one and so the voltage drop across it has to be updated for each operating point.

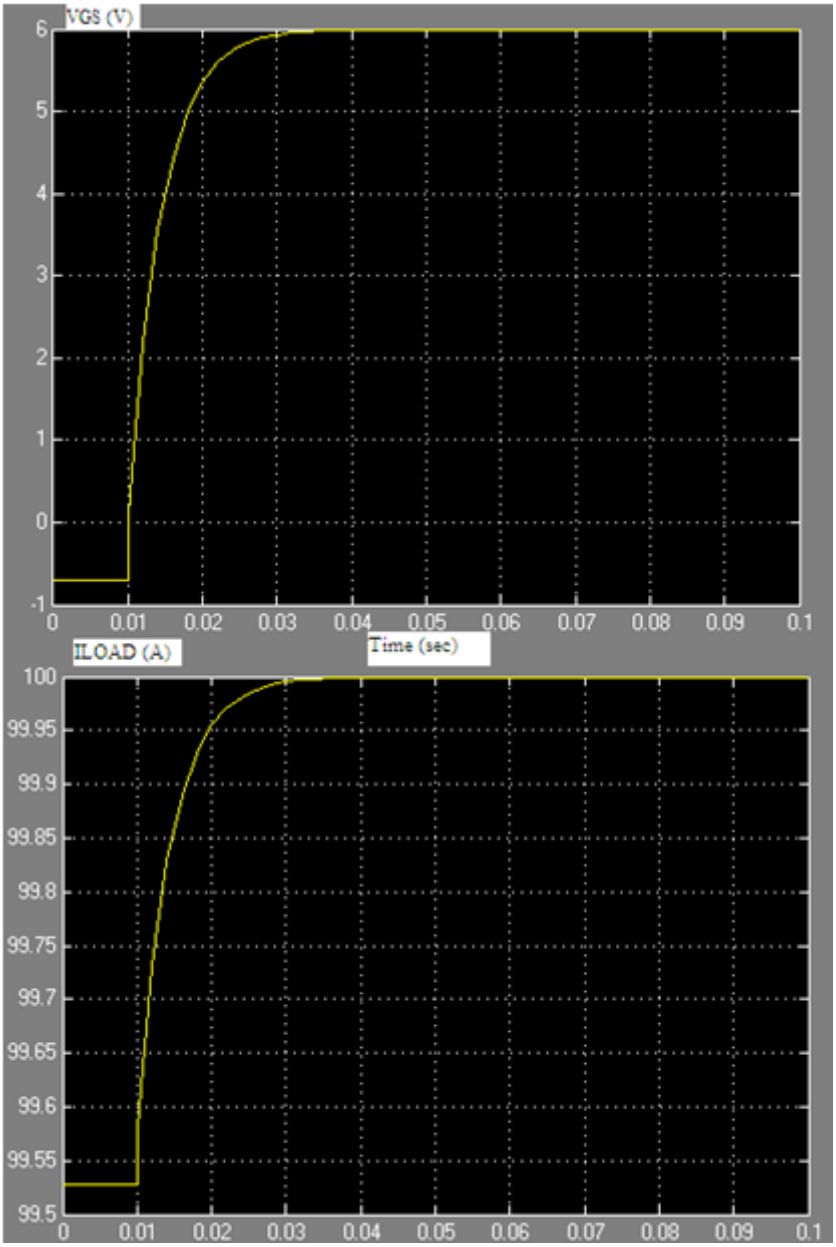


Figure 3-25. V_{GS} vs. time & I_{LOAD} vs. Time in response to step input.

In addition to the variable resistor model, a more accurate model is approximated using the general current formula of MOSFET in linear region. Because the low side MOSFETs operate in linear region at steady-state, this model is more accurate than the previous one for steady-state response analysis of the controller. V_{DS} voltage of the low side MOSFETs are considered as 0.5V at steady-state as in the previous model. This assumption is a valid assumption because the low side MOSFETs are preferred to be operating in linear region as much as possible

during pulse to decrease the power dissipation. Transconductance parameter (K_n) of the MOSFETs are calculated approximately as 110A/V^2 using the graph shown in Figure 3-23.

Accordingly, current function of the low side MOSFETs can be written as follows:

$$I = K_n \times V_{DS} \times \left(V_{GS} - \left(V_{th} + \frac{V_{DS}}{2}\right)\right) \tag{3.34}$$

where V_{th} is the threshold voltage of the MOSFETs and is 2.5V [19].

$$I = 110 \times 0.5 \times \left(V_{GS} - \left(2.5 + \frac{0.5}{2}\right)\right) = 55 \times (V_{GS} - 2.75) \tag{3.35}$$

Using (3.47), V_{GS} dependent new model can be illustrated as in Figure 3-26.

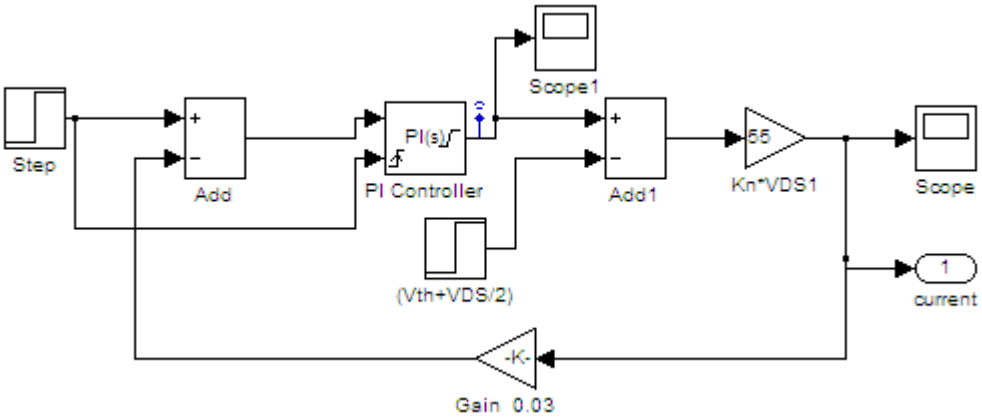


Figure 3-26. Closed loop current control model with the assumption of linear operating region of low side MOSFETs.

In this model, there are two inputs one of which is the step input and the other one is the constant DC term – (V_{th}+V_{DS}/2) coming from the current equation of the MOSFETs. Using the superposition, two different linear transfer functions can be obtained and the sub-models can be shown for each input as illustrated in Figure 3-27.

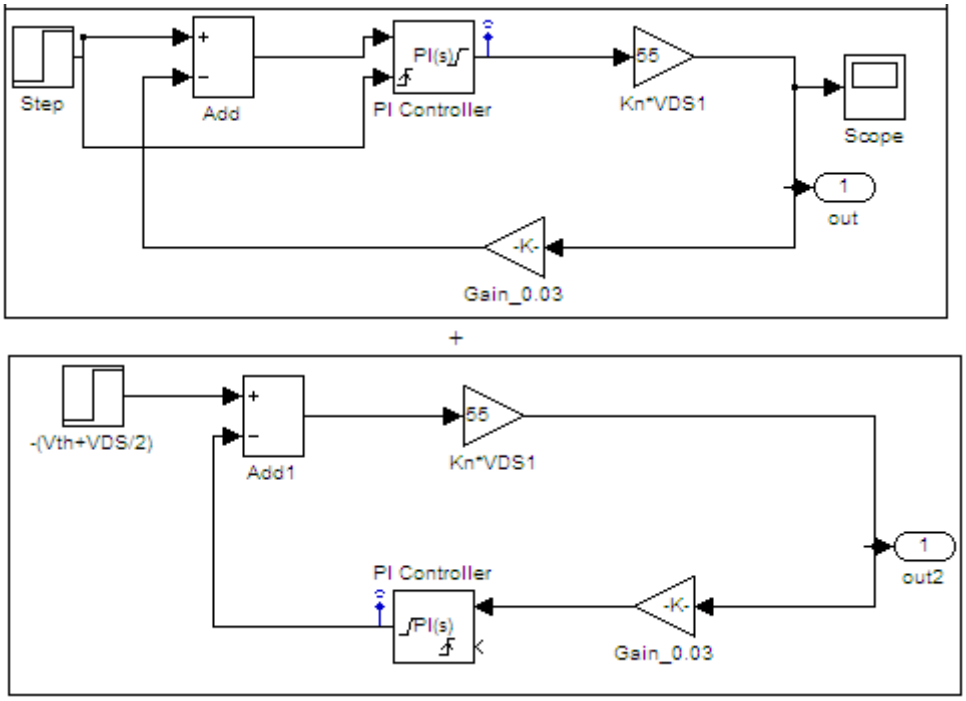


Figure 3-27. Two input model of the closed loop current model using superposition.

Using the same PI parameters as in the previous model, the sub-models can be shown in s-domain as in Figure 3-28 and Figure 3-29.

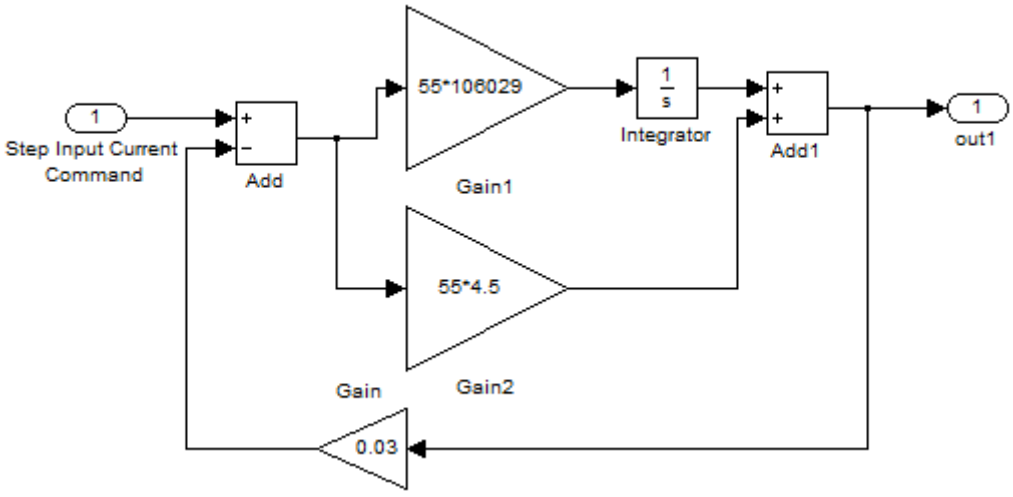


Figure 3-28. Closed loop sub-model in s-domain for step input current command.

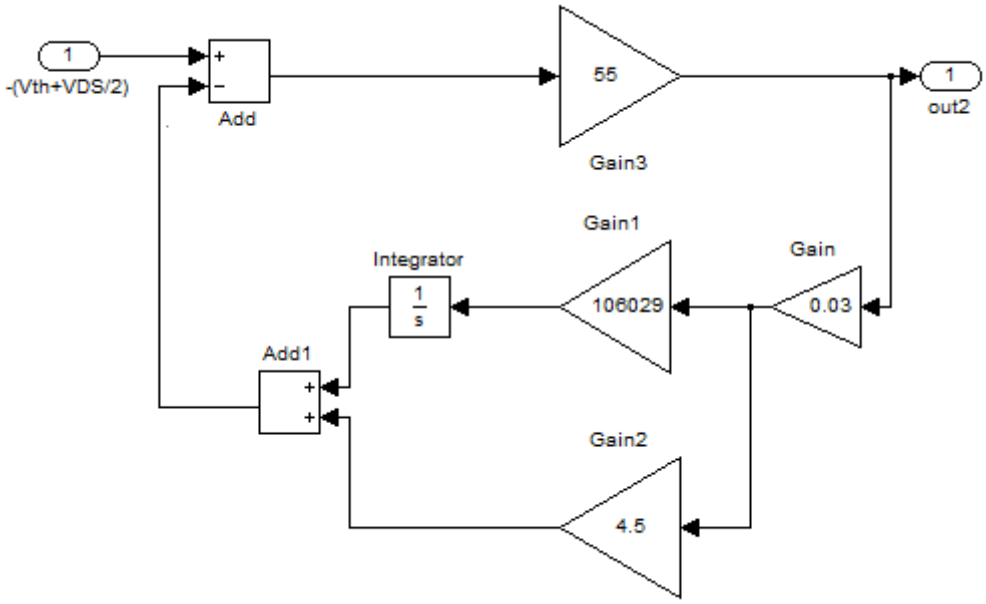


Figure 3-29. Closed loop sub-model in s-domain for V_{th}+V_{DS}/2 term.

The overall transfer functions for each sub-model can be calculated as:

$$H_1(s) = \frac{247.5s+5.832e006}{8.425s+1.749e005} \tag{3.36}$$

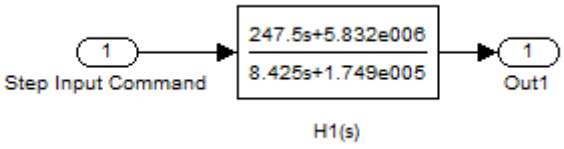


Figure 3-30. Resultant sub-model in s-domain for step input current command.

$$H_2(s) = \frac{55s}{8.425s+1.749e005} \tag{3.37}$$

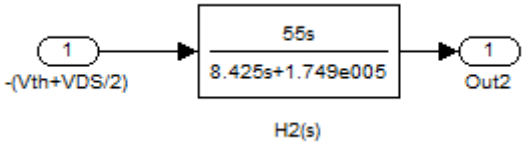


Figure 3-31. Resultant sub-model in s-domain for V_{th}+V_{DS}/2 term.

Since the amplitudes of each step input are 3V and -2.75V for 100A current case. The overall current transfer function of the model can be obtained as follows:

$$H(s) = 3\,H_1(s) + (-2.75)\,H_2(s) \tag{3.38}$$

$$H(s) = \frac{591.3s+1.749e007}{8.425s+1.749e005} \tag{3.39}$$

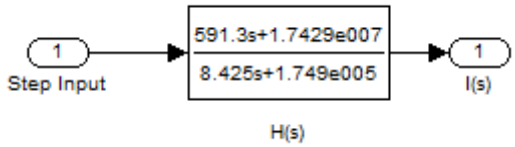


Figure 3-32. Resultant overall model in s-domain for step input.

Step response and the bode plot of the system is show in Figure 3-33. The results seem to be consistent with time domain simulation results at steady-state. It gives a general idea about the steady-state behaviour of the system. However, the approximated model does not give information about the transient behaviour because it is almost impossible to linearize the transient behaviour of the low side MOSFETs.

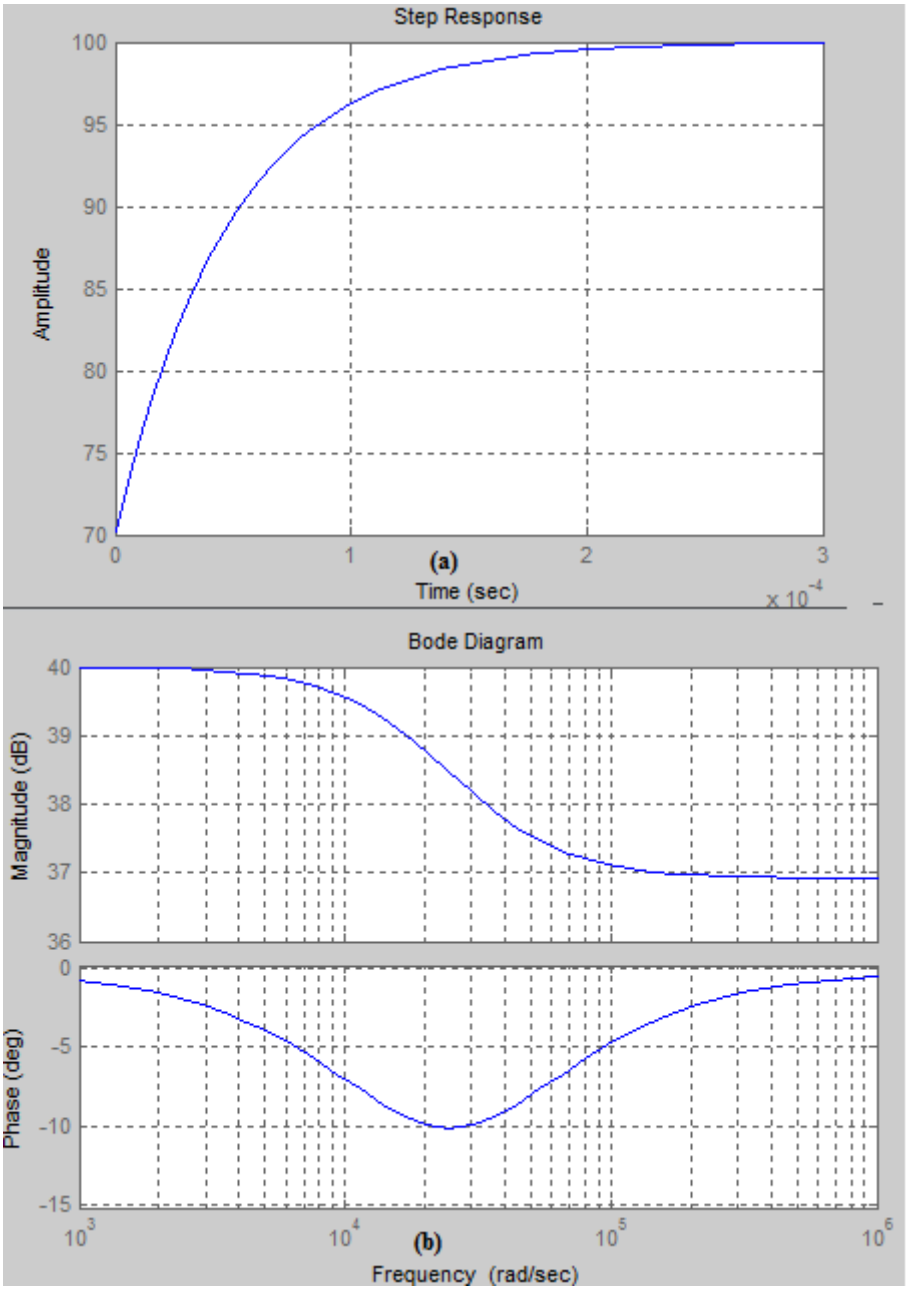


Figure 3-33. (a) Step response of the overall model, (b) Bode plot of the overall model.

CHAPTER 4

TESTS AND RESULTS

In Chapter 3, the design aspects and the overall architecture of the proposed LD driver is examined in detail. The driver is analysed via ORCAD simulation program and MATLAB in order to simulate the actual system as realistically and identically as possible.

We compare the simulation results of the LD driver to the results of the real hardware implementation of the driver. The laboratory test bed system is composed of a "Laser Control Card", which communicates with the driver and provides the necessary bias voltages for the ICs used in the LD driver, two power supplies which provides DC power at 24V for the "Laser Control Card" and 82.5V for the LD driver, an *Agilent Infiniium 54832D MSO* type oscilloscope, *Tektronix TCPA300* and *TCPA303* current probe set, a computer having RS232 interface to send the instructions such as the capacitor charging and discharging prior to firing, the properties of the desired current waveform, single firing and continuous firing commands with desired frequency to the "Laser Control Card" and a hand-held thermal camera to monitor the temperature of the ICs used in the driver.

To show the consistency between the experimental results and the simulation results, the tests are done with the nominal values of the system requirements, which are the level of 100A LD current with duration of 200μs and frequency of 20Hz. The first tests are done with the resistive loads and normal diode series prior to validating the safe operation of the driver.

The tests of the LD driver starts with the boundary scan tests to see whether the LD driver is communicating with the "Laser Control Card". Besides, the bias voltages coming from the "Laser Control Card" is checked and the temperature of the ICs in the LD driver is monitored via a thermal camera to see whether there is a failure in the components used in the driver.

After completing the necessary controls and validating the proper communication with the "Laser Control Card", the input capacitors are charged to a value determined by the programmable IC in the driver and discharged by sending the corresponding instructions from the computer to see whether the input capacitor adjustment and discharge units are working properly or not. Because the information of the desired input capacitor voltage value is determined digitally by the programmable IC and converted to an analog signal in the driver, the proper operation of the D/A conversion unit of the driver is also verified with these tests. Moreover, the A/D conversion unit of the driver is tested prior to firing by disabling the capacitor discharge circuit manually. Because this function is disabled, although a "discharge" command is sent from the computer, the input capacitor voltages will remain almost constant and after a while the programmable IC will give an error related to the failure in capacitor discharge in response to the information of the input capacitor voltage value coming from the A/D conversion unit of the driver.

Following the end of the pre-firing tests, LD single firing and continuous firing tests are done so that the proper operation of the LD driver control unit and the protection blocks can be verified.

In addition to the hardware tests of the blocks of the LD driver, sensitivity analysis of the system is covered in this chapter.

4.1 Hardware Tests

4.1.1 Input Capacitor Charging and Discharging Tests

The charge voltage is determined as 81.5V in these tests. When a "charge" command is sent via the test computer, both the corresponding output of the D/A (DA_VOLT_SET signal as shown in Figure 3-3) and the voltage across the terminals of the input capacitors are observed via the oscilloscope as shown in Figure 4-1. To obtain the desired input capacitor voltage value, the level of the DA_VOLT_SET signal has to be 3.52V as it is explained in previous chapter. The resultant capacitor voltage is measured as 81.7V as shown in Figure 4-1, which almost agrees with the expected result.

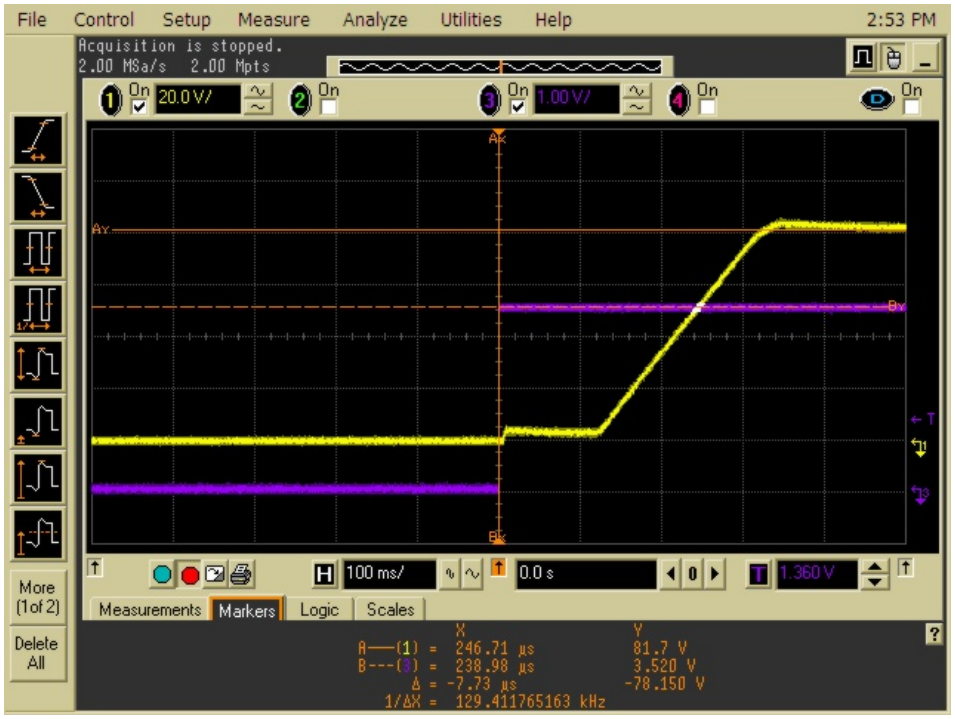


Figure 4-1. Input capacitor charging and the corresponding DA_VOLT_SET signal in response to "charge" command - input capacitor voltage vs. time (yellow) & DA_VOLT_SET signal vs. time (purple).

Following the end of the capacitor charging test, a "discharge" command is sent via the test computer. As a result, the gate voltage of the corresponding discharge

MOSFET switch becomes logically high and the input capacitor voltage drops to 0V as shown in Figure 4-2, which validates the proper operation of the input capacitor discharge unit.

Figure 4-2. Input capacitor discharging and gate voltage of the discharge MOSFET switch in response to "discharge" command – input capacitor voltage vs. time (yellow) & gate voltage of the discharge MOSFET switch vs. time (purple).

4.1.2 LD Firing Tests

As it is mentioned before, first firing tests are done with resistive loads and normal diodes to guarantee the proper operation of the LD driver. After validating the driver operation, the tests are repeated with the actual load arrays. Following measurements are done with the actual LD arrays.

Before firing the LD arrays, the properties of the desired current waveform are sent via the test computer through the "Laser Control Card" to the programmable IC of the LD driver. Then, the input capacitors are charged to appropriate voltage

level and the high side protection MOSFET switch is turned on so that the LD arrays can be fired when a "fire" command is applied via the test computer.

Experimental results are shown in Figure 4-3 and Figure 4-4. Amplitude of the input reference command is adjusted as 1.5V in order to obtain 100A current pulse during the tests. The current through the LD arrays are measured via the current probe. The actual current waveform is converted to a voltage waveform by the current probe and seen in the oscilloscope screen.

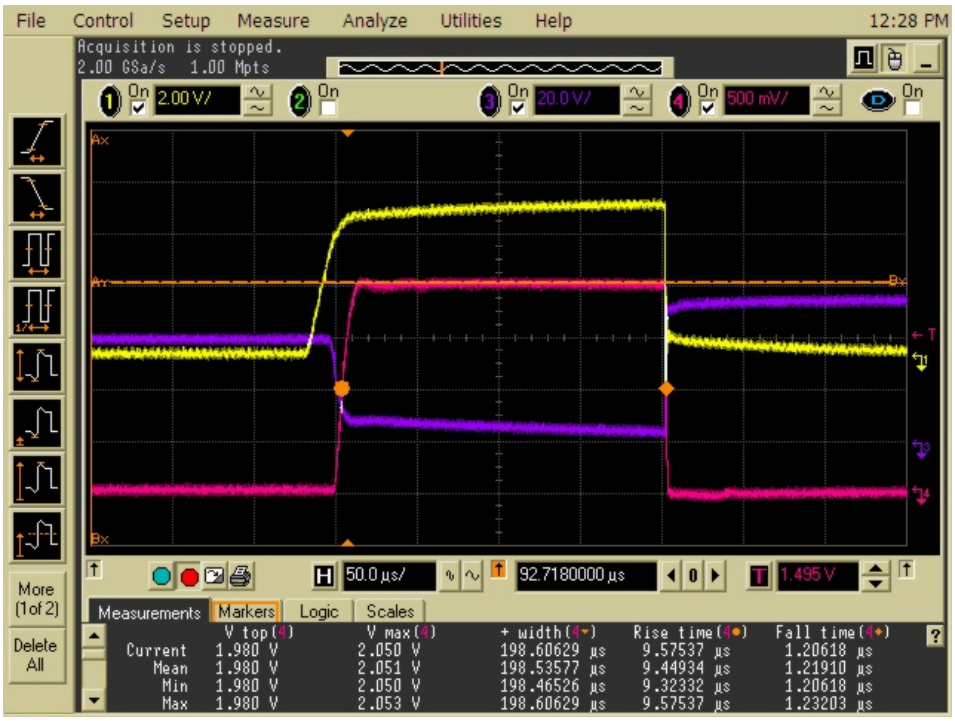


Figure 4-3. Oscilloscope measurements for 100A LD current with duration of 200µs – the voltage across gate and source terminals of the low side MOSFET vs. time (yellow), the voltage across drain and source terminals of the low side MOSFET vs. time (purple) & the current through the LDs vs. time (red).

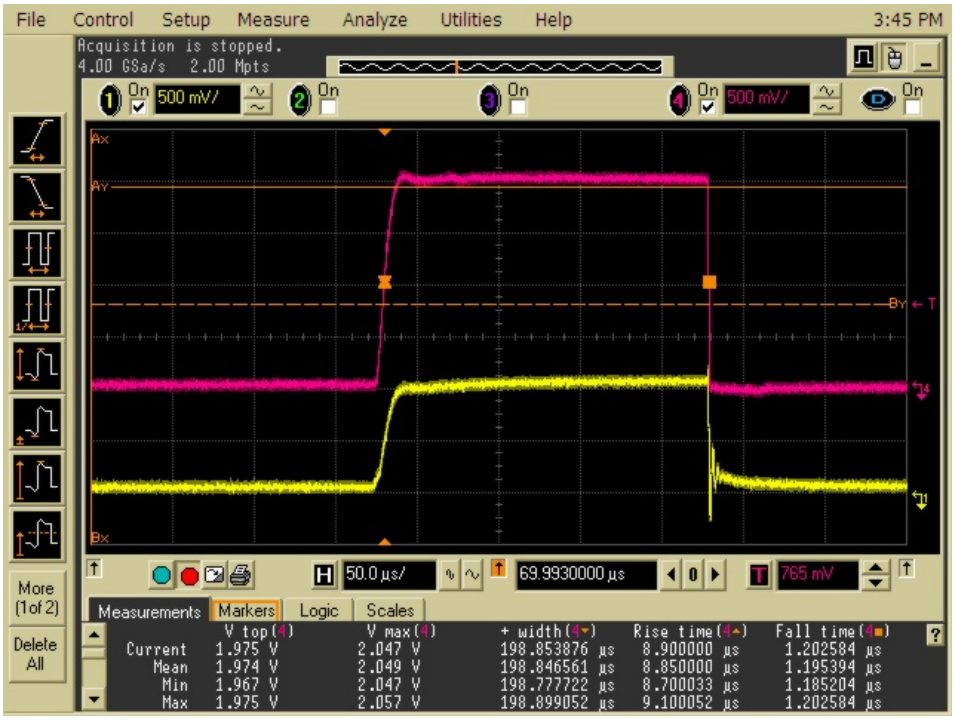


Figure 4-4. Oscilloscope measurements for 100A LD current with duration of 200µs –the voltage across the current sense resistors during pulse vs. time (yellow) & the current through the LDs vs. time (red).

In Figure 4-3, the measurement in channel 4 indicates the current waveform which is converted to a voltage waveform by the current probe. Each vertical division is 500mV, which corresponds to 25A. The average current amplitude is observed to be 1.98V, which corresponds very closely to 100A. That agrees with the simulation results. Furthermore, the calculated rise and fall times are approximately 9.45µs and 1.2µs, respectively, which are very close to the simulation results.

In Figure 4-3, the measurement in channel 2 indicates the voltage waveform across gate and source terminals of each low side MOSFET. The voltage amplitude is very close to 6V, which validates the simulation results.

In Figure 4-3, the measurement in channel 3 indicates the behavior of the voltage waveform across drain and source terminals of each low side MOSFET in response to the voltage rise across their gate and source terminals. It is observed

that there is approximately 5V decrease in the voltage due to the voltage droop in the input capacitors. That very closely agrees with the calculated value. The slight difference comes from the effective series resistance of the input capacitors.

In Figure 4-4, the measurement in channel 2 indicates the voltage waveform across each 10mΩ sense resistor. The voltage amplitude is observed to be 1V, which is compatible with the value of the load current amplitude and the simulation results.

4.1.3 Protection Tests

As it is explained in previous chapter, there are both analog and digital protection blocks in the driver in order to guarantee the safe operation of the driver. The digital protection is capable of detecting excess current through and/or overvoltage across the LD series and failure in the pulse width. The analog protection is only responsible for detection of overcurrent and is a self-protection mechanism, working independently. Analog circuit protects both of the diode arrays by interrupting the current through them immediately even if only one of the arrays current exceeds the pre-set value, which is set as 130A in the design as shown in Figure 3-8.

During the protection tests, overcurrent protection of the digital protection block is disabled to test the analog protection individually because the digital protection block is adjusted to interrupt the LD current if it exceeds 125A. Therefore, in normal operating conditions, even if an excess current failure is detected in one of the arrays, digital protection block of the LD driver will take necessary precautions.

For the test of the analog protection block, one of the LD arrays are shorted. When a "fire" command is applied to the system, the current through the shorted LD array rises abruptly. As soon as it exceeds the value of 130A, the output of the

comparator becomes logically high and the LD current is interrupted immediately as shown in Figure 4-5.

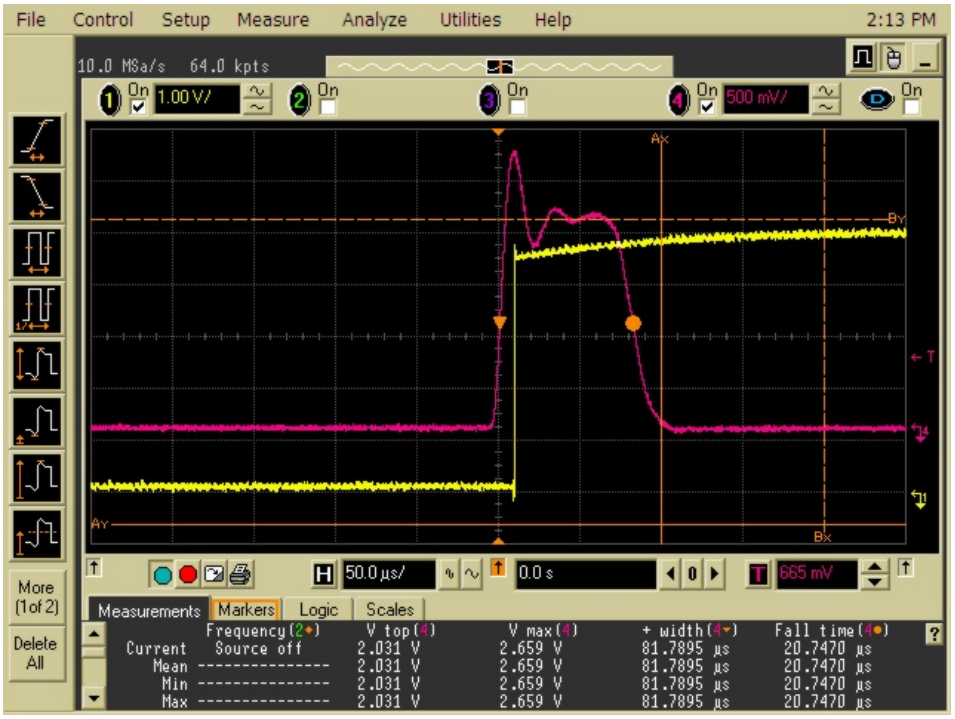


Figure 4-5. Overcurrent test of the analog protection when one of the LD arrays are shorted – the current through the shorted LD array vs. time (red) & the output of the comparator, which is shown in Figure 3-8 vs. time (yellow).

The oscilloscope results shown in Figure 4-5 are consistent with the theoretical results. As the current through the shorted LD array reaches 131.5A, which corresponds to a voltage waveform with an amplitude of 2.031V obtained via the current probe, the LD current is interrupted immediately.

For the overvoltage test of the digital protection, one of the LD arrays is discarded from the LD driver. The other LD array current is measured with the current probe. When a "fire" command is applied to the system, the current flows through the remaining LD array. As a result of which an overvoltage across the terminals of the discarded LD array is detected. Consequently, the current through the other array is interrupted immediately as shown in Figure 4-6.

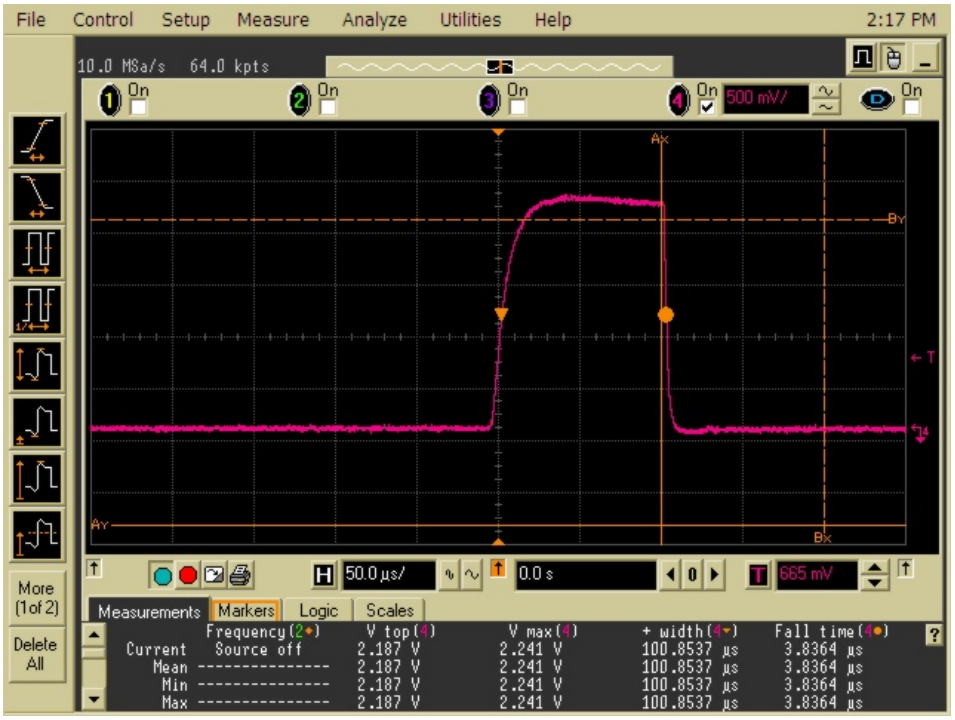


Figure 4-6. Overvoltage test of the digital protection when one of the LD arrays are discarded - the current through the other LD array vs. time.

4.2 Sensitivity Analysis of the Steady-State Response of the Closed Loop Model

The closed loop system is analysed in this chapter for possible variations in the values of K_p and K_i of the PI controller, K_n paramater of the low side MOSFETs and the total feedback gain (F). The effect of variations in both ambient and component temperature is avoided because the temperature is kept quite constant in normal operating conditions.

K_p and the total feedback gain may vary due to variations in the resistance values. The resistors used in the closed loop system have 1% tolerance in their value except for the sense resistor, the tolerance of which is 0.1%. Besides, K_i term can vary due to both variations in the capacitance and resistance values. The capacitors used in the PI controller have 10% tolerance in their value. K_n

parameter of the MOSFET is calculated approximately as $110A/V^2$ as explained in Chapter 4. Since the MOSFETs are not matched, this parameter may vary between the MOSFETs.

Sensitivity analysis of the closed loop system is done for each sub-model which are explained in Chapter 3 and the results are combined using superposition. The effects of the variations in the values of each term are analysed on the response of the closed loop system via MATLAB.

4.2.1 Sensitivity Analysis with respect to the Proportional Constant

The values of the resistances - 1kΩ, 1.5 kΩ, 3kΩ and 9kΩ as shown in Figure 3-10 comprise the resultant K_p, which has the value of 4.5. Considering the tolerances in the values of these resistances, the maximum and minimum value of K_p can be calculated as below:

$$K_{p,max}=\frac{1.5k\Omega\times1.01}{1k\Omega\times0.99}\times\frac{9k\Omega\times1.01}{3k\Omega\times0.99}=4.684 \quad (4.1)$$

$$K_{p,min}=\frac{1.5k\Omega\times0.99}{1k\Omega\times1.01}\times\frac{9k\Omega\times0.99}{3k\Omega\times1.01}=4.324 \quad (4.2)$$

4.2.1.1 Sensitivity Analysis of the Closed Loop Sub-Model for Step Input Current Command with respect to the Proportional Constant

For K_p=4.684, the overall transfer function of the sub-model shown in Figure 3-28 becomes as:

$$H_1'(s) = \frac{257.6s+5.832e006}{8.729s+1.749e005} \tag{4.3}$$

Step response and bode plot of the new sub-model are shown in Figure 4-7 and Figure 4-8. The results show that the increase in the value of K_p has almost no effect on the corresponding sub-model.

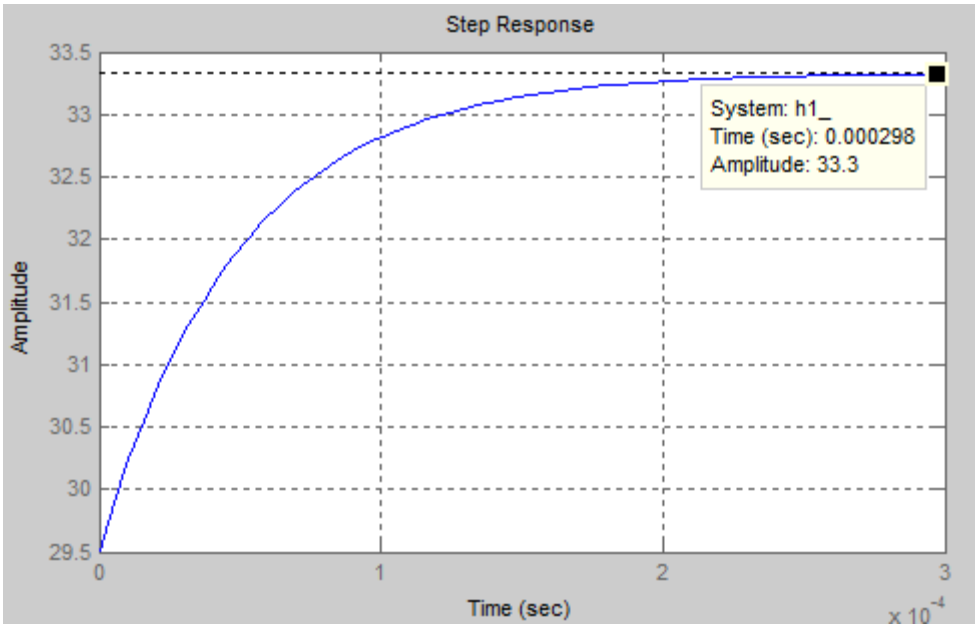


Figure 4-7. Step response of the new sub-model in response to increase in K_p.

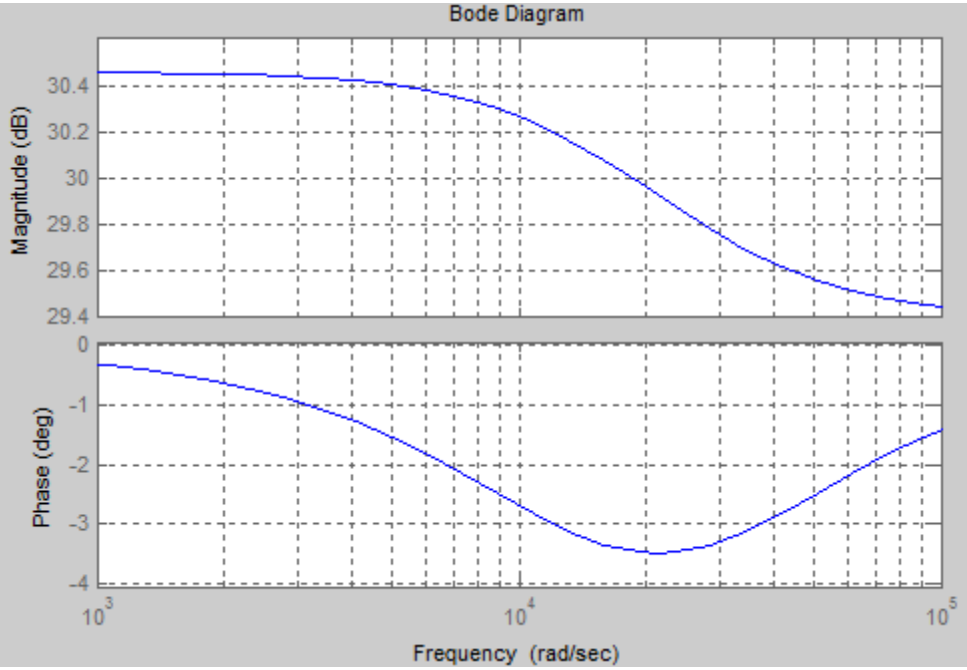


Figure 4-8. Bode plot of the new sub-model in response to increase in K_p.

The sensitivity of the sub-model shown in Figure 3-28 to increase in the value of K_p can be calculated as:

$$S^1_{Kp,max}(s) = \frac{\Delta H_1(s)/H_1(s)}{\Delta Kp/Kp} \tag{4.4}$$

where $\Delta H_1(s)$ and ΔKp are the changes in the values of $H_1(s)$ and Kp. Accordingly;

$$S^1_{Kp,max}(s) = \frac{\frac{85.26s^3+1.77e006s^2+0.002607s}{1.82e004s^3+1.172e009s^2+2.508e013s+1.785e017}}{0.0409} \tag{4.5}$$

$$S^1_{Kp,max}(s) = \frac{2085s^3+4.33e007s^2+0.06376s}{1.82e004s^3+1.172e009s^2+2.508e013s+1.785e017} \tag{4.6}$$

Magnitude plot of $S^1_{Kp,max}(s)$ is shown in Figure 4-9. It is observed that the sensitivity of the sub-model to the increase in the value of K_p is almost 0 until the moderate frequency values. Even, the magnitude of $S^1_{Kp,max}$ is 0.1 at high frequency.

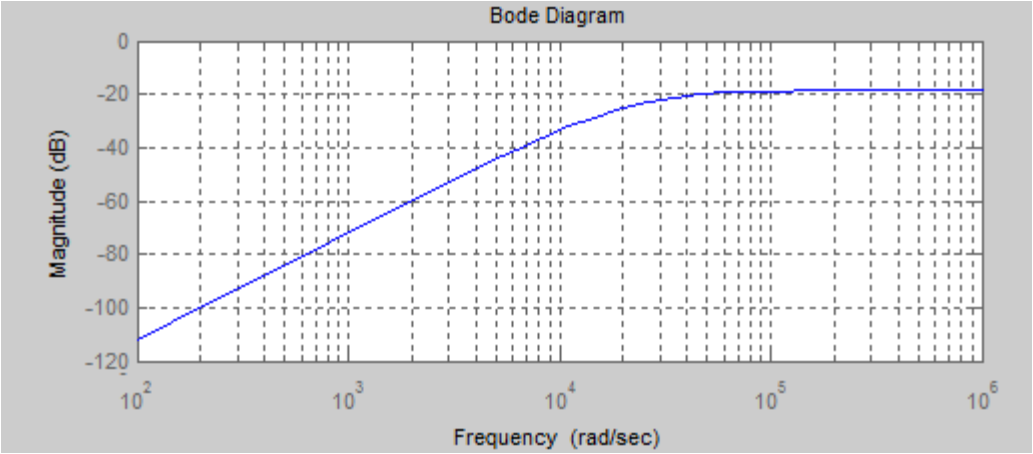


Figure 4-9. Magnitude response of $S_{Kp,max\_1}(s)$.

Similarly, for K_p=4.324, the overall transfer function of the sub-model shown in Figure 3-28 becomes as:

$$H_1''(s) = \frac{237.8s+5.832e006}{8.135s+1.749e005} \tag{4.7}$$

Step response and bode plot of the new sub-model are shown in Figure 4-10 and Figure 4-11 . The results show that the decrease in the value of K_p has almost no effect on corresponding sub-model when compared to the results shown in Figure 4-7 and Figure 4-8.

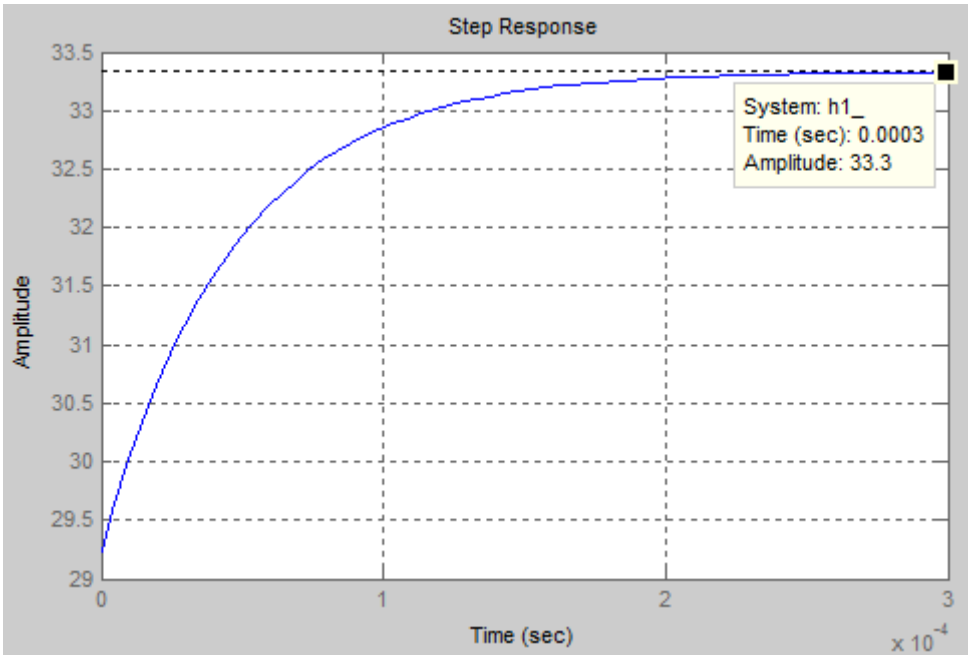


Figure 4-10. Step response of the new sub-model in response to decrease in K_p.

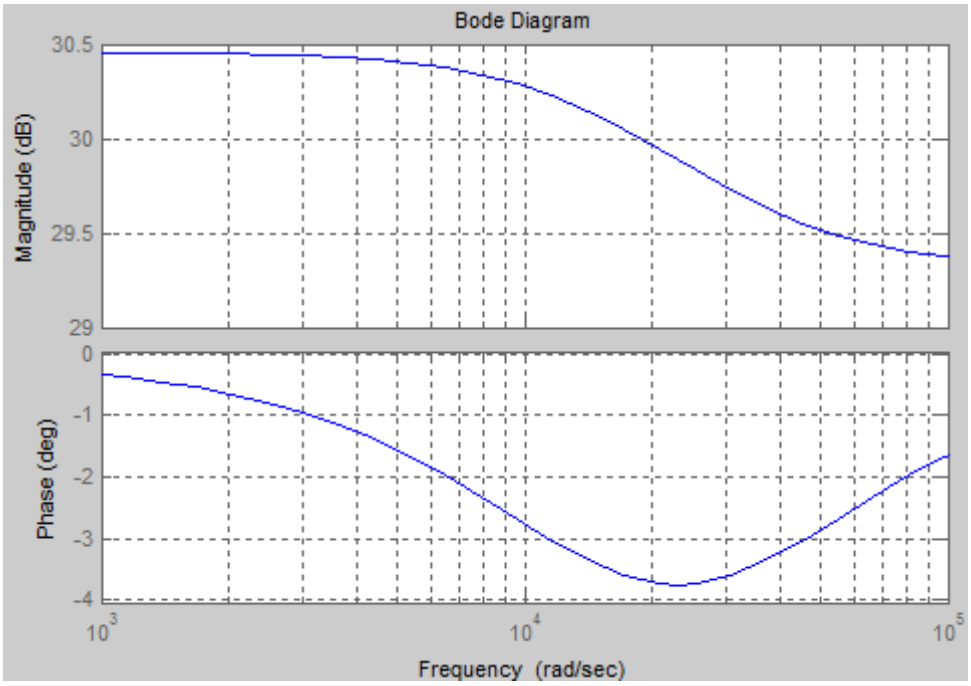


Figure 4-11. Bode plot of the new sub-model in response to decrease in K_p.

The sensitivity of the sub-model shown in Figure 3-28 to decrease in the value of K_p can be calculated as:

$$S^1_{Kp,min}(s) = \frac{\Delta H_1(s)/H_1(s)}{\Delta Kp/Kp} \tag{4.8}$$

$$S^1_{Kp,min}(s) = \frac{\frac{81.55s^3+1.693e006s^2-0.005214s}{1.696e004s^3+1.117e009s^2+2.447e013s+1.785e017}}{0.0407} \tag{4.9}$$

$$S^1_{Kp,min}(s) = \frac{2085s^3+4.33e007s^2-0.1333s}{1.696e004s^3+1.117e009s^2+2.447e013s+1.785e017} \tag{4.10}$$

Magnitude plot of $S^1_{Kp,min}(s)$ is shown in Figure 4-12. The waveform is almost the same as the one shown in Figure 4-9, which proves that the corresponding sub-model of the closed loop system insensitive to variations in K_p.

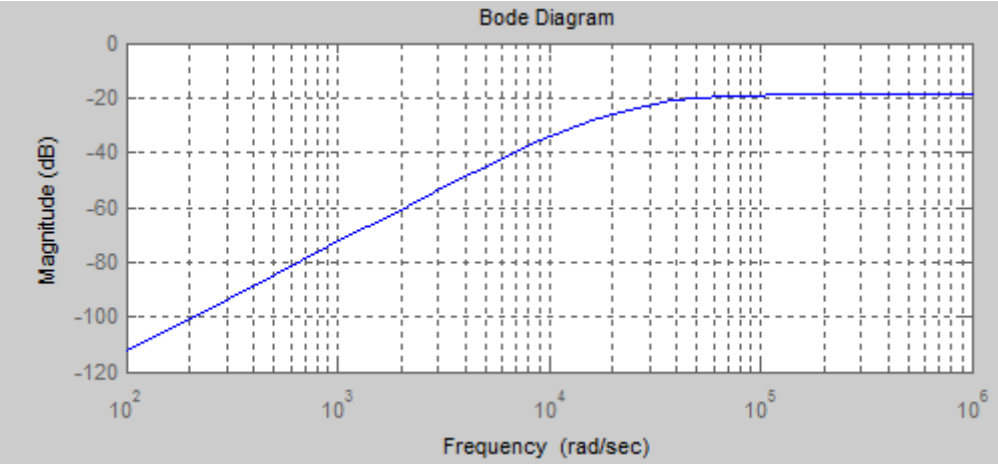


Figure 4-12. Magnitude response of $S_{Kp,min\_1}(s)$.

4.2.1.2 Sensitivity Analysis of the Closed Loop Sub-Model for the Constant DC Term with respect to the Proportional Constant

For K_p=4.684, the overall transfer function of the sub-model shown in Figure 3-29 becomes as:

$$H_2'(s) = \frac{55s}{8.729s+1.749e005} \tag{4.11}$$

Step response and bode plot of the new sub-model are shown in Figure 4-13 and Figure 4-14. The results show that the increase in the value of K_p has almost no effect on the corresponding sub-model.

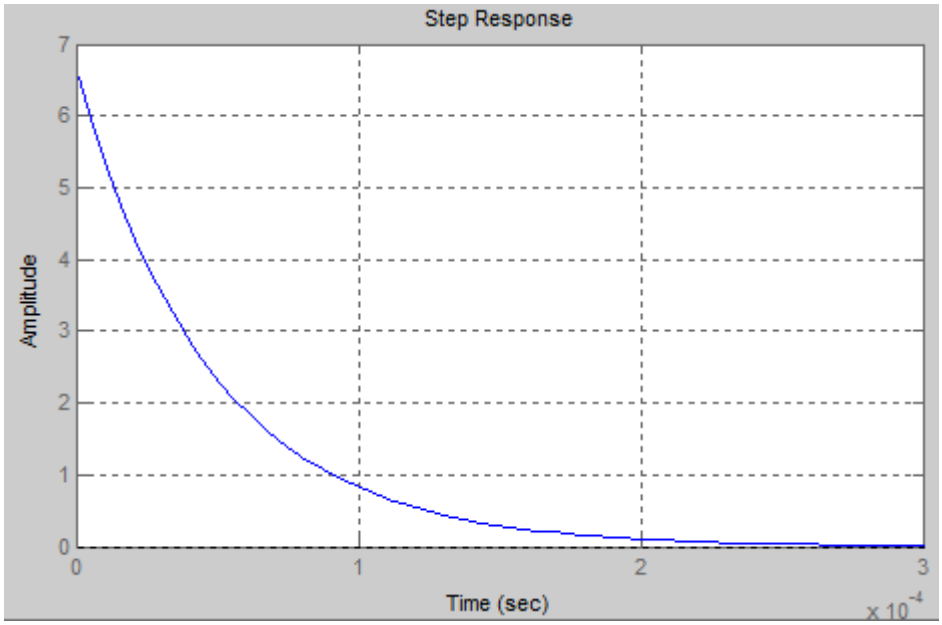


Figure 4-13. Step response of the new sub-model in response to increase in K_p.

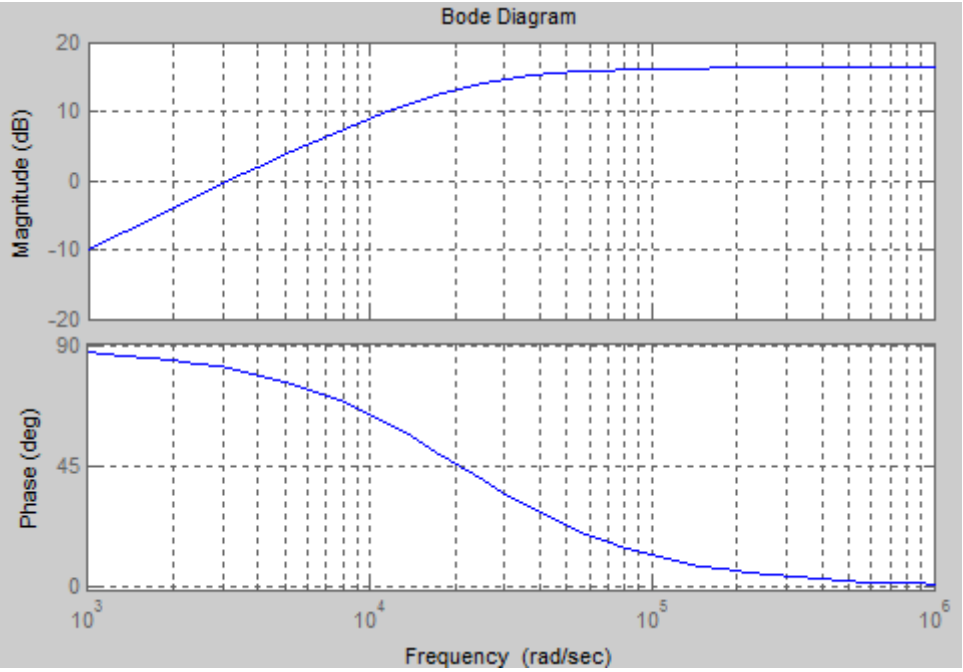


Figure 4-14. Bode plot of the new sub-model in response to increase in K_p.

The sensitivity of the sub-model shown in Figure 3-29 to increase in the value of K_p can be calculated as:

$$S^2_{Kp,max}(s) = \frac{\Delta H_2(s)/H_2(s)}{\Delta Kp/Kp} \tag{4.12}$$

where $\Delta H_2(s)$ and ΔKp are the changes in the values of $H_2(s)$ and Kp. Accordingly;

$$S^2_{Kp,max}(s) = \frac{-\left(\frac{140.7s^2+2.921e006s}{4045s^2+1.651e008s+1.683e012}\right)}{0.0409} \tag{4.13}$$

$$S^2_{Kp,max}(s) = -\left(\frac{3441s^2+7.144e007s}{4045s^2+1.651e008s+1.683e012}\right) \tag{4.14}$$

Magnitude plot of $S^2_{Kp,max}(s)$ is shown in Figure 4-15. It is observed that the sensitivity of the sub-model to the increase in the value of K_p is very low and even less than 1 in magnitude at high frequencies.

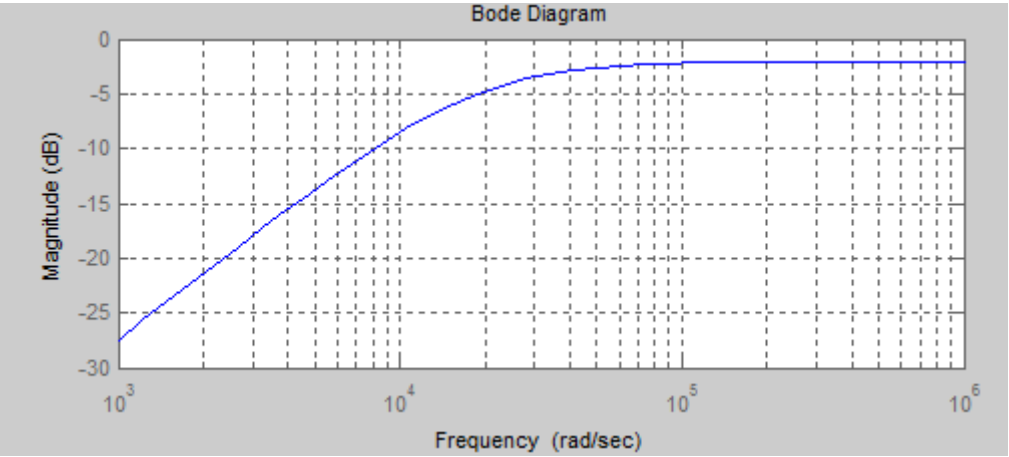


Figure 4-15. Magnitude response of $S_{Kp,max\_2}(s)$.

Similarly, for K_p=4.324, the overall transfer function of the sub-model shown in Figure 3-29 becomes as:

$$H_2''(s) = \frac{55s}{8.135s+1.749e005} \tag{4.15}$$

Step response and bode plot of the new sub-model are shown in Figure 4-16 and Figure 4-17. The results show that the decrease in the value of K_p has almost no effect on corresponding sub-model when compared to the results shown in Figure 4-13 and Figure 4-14.

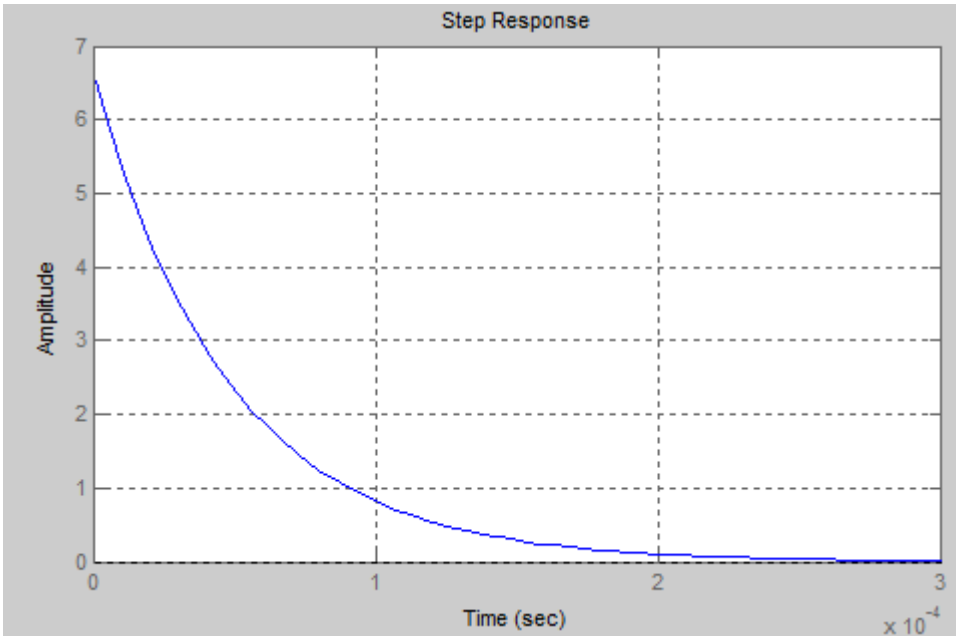


Figure 4-16. Step response of the new sub-model in response to decrease in K_p.

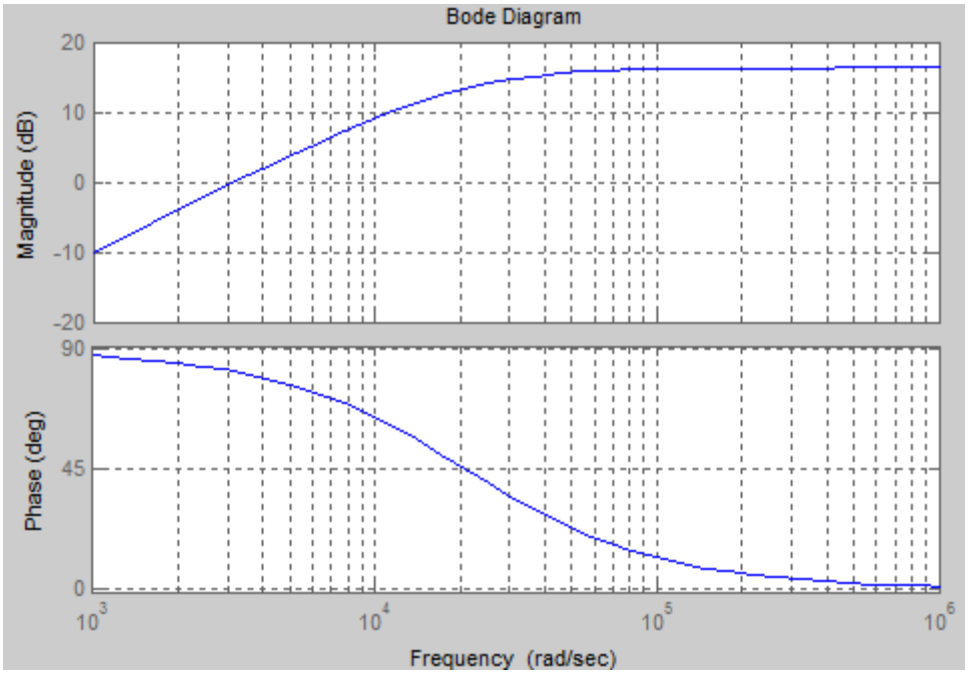


Figure 4-17. Bode plot of the new sub-model in response to decrease in K_p.

The sensitivity of the sub-model shown in Figure 3-29 to decrease in the value of K_p can be calculated as:

$$S^2_{Kp,min}(s) = \frac{\Delta H_1(s)/H_1(s)}{\Delta Kp/Kp} \tag{4.16}$$

$$S^2_{Kp,min}(s) = \frac{-\left(\frac{134.6s^2+2.794e006s}{3769s^2+1.593e008s+1.683e012}\right)}{0.0391} \tag{4.17}$$

$$S^2_{Kp,min}(s) = -\left(\frac{3441s^2+7.144e007s}{3769s^2+1.593e008s+1.683e012}\right) \tag{4.18}$$

Magnitude plot of $S^2_{Kp,min}(s)$ is shown in Figure 4-18. The waveform is almost the same as the one shown in Figure 4-15, which proves that the corresponding sub-model of the closed loop system insensitive to variations in K_p.

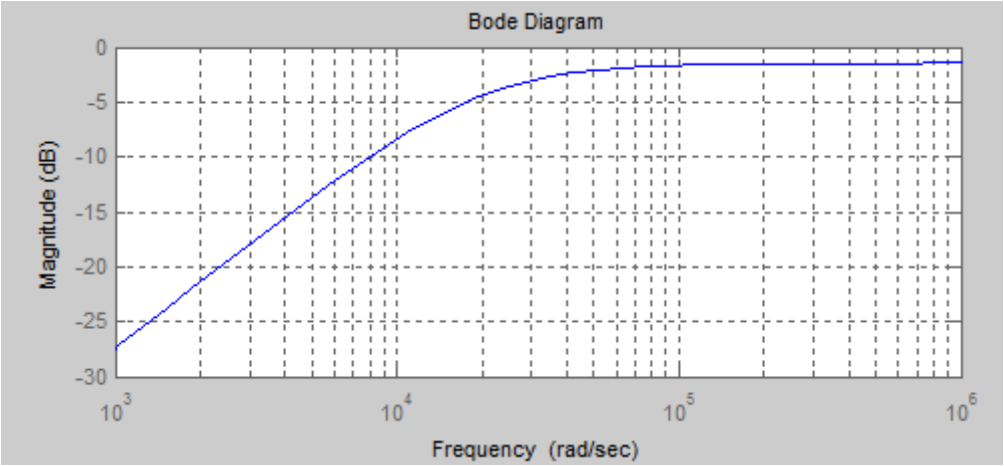


Figure 4-18. Magnitude response of $S_{Kp,min\_2}(s)$.

4.2.2 Sensitivity Analysis with respect to the Integral Constant

The values of the resistances and the total capacitance comprising the resultant K_i, which has the value of 106029, are 1kΩ, 1.5kΩ, 3kΩ and 4.7nF as shown in

Figure 3-10. Considering the tolerances in the value of the resistance and the total capacitance, the maximum and minimum value of K_i can be calculated as below:

$$K_{i,max}=\frac{1.5k\Omega\times1.01}{1k\Omega\times0.99}\times\frac{1}{3k\Omega\times0.99\times4.7e-009\times0.9}=121809.35 \quad (4.19)$$

$$K_{i,min}=\frac{1.5k\Omega\times0.99}{1k\Omega\times1.01}\times\frac{1}{3k\Omega\times1.01\times4.7e-009\times1.1}=93858.13 \quad (4.20)$$

4.2.2.1 Sensitivity Analysis of the Closed Loop Sub-Model for Step Input Current Command with respect to the Integral Constant

For K_i=121809.35, the overall transfer function of the sub-model shown in Figure 3-28 becomes as:

$$H_1'(s)=\frac{247.5s+6.7e006}{8.425s+2.01e005} \quad (4.21)$$

Step response and bode plot of the new sub-model are shown in Figure 4-19 and Figure 4-20. The results show that the increase in the value of K_i has almost no effect on the corresponding sub-model.

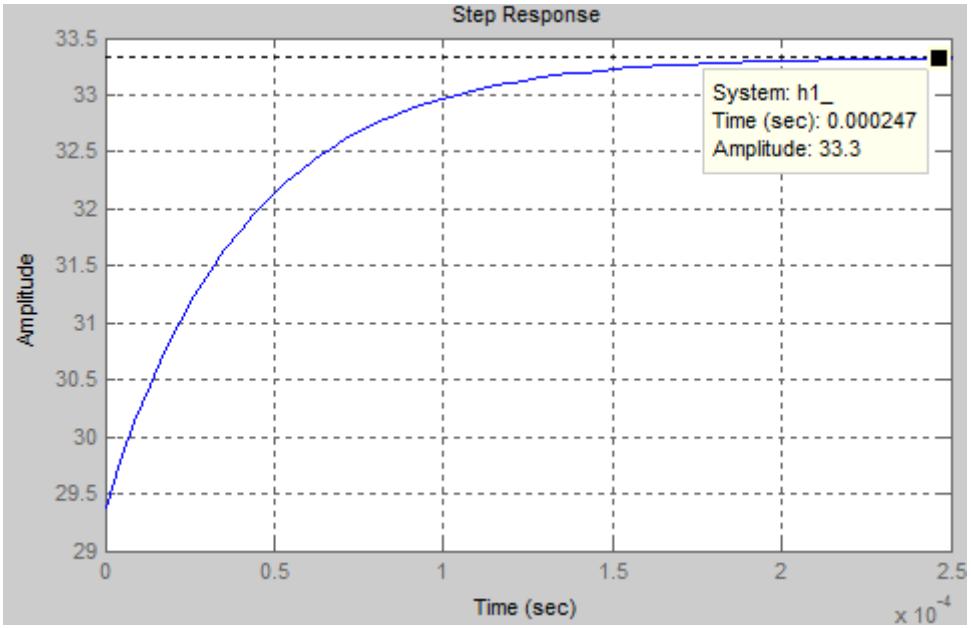


Figure 4-19. Step response of the new sub-model in response to increase in K_i.

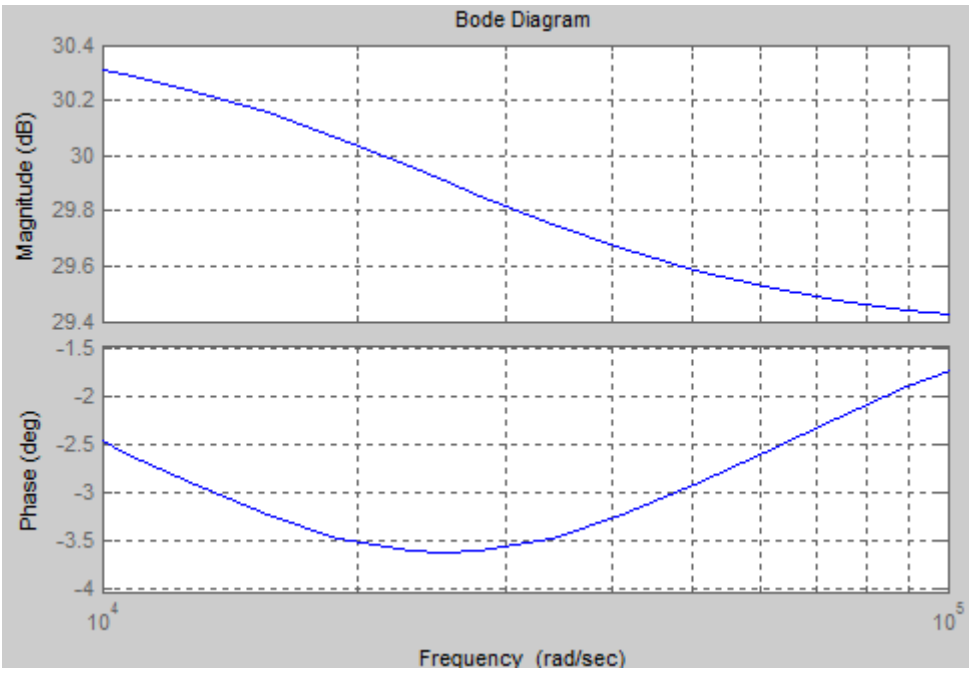


Figure 4-20. Bode plot of the new sub-model in response to increase in K_i.

The sensitivity of the sub-model shown in Figure 3-28 to increase in the value of K_i can be calculated as:

$$S^{1}_{Ki,max}(s) = \frac{\Delta H_1(s)/H_1(s)}{\Delta K_i/K_i} \tag{4.22}$$

where $\Delta H_1(s)$ and ΔK_i are the changes in the values of $H_1(s)$ and K_i. Accordingly;

$$S^{1}_{Ki,max}(s) = \frac{\frac{7.312e006s^2+1.518e011s-42.71}{1.757e004s^3+1.198e009s^2+2.717e013s+2.051e017}}{0.1488} \tag{4.23}$$

$$S^{1}_{Ki,max}(s) = \frac{4.913e007s^2+1.02e012s-287}{1.757e004s^3+1.198e009s^2+2.717e013s+2.051e017} \tag{4.24}$$

Magnitude plot of $S^{1}_{Ki,max}(s)$ is shown in Figure 4-21. It is observed that the sensitivity of the sub-model to the increase in the value of K_i is almost 0 until the moderate frequency values. Even, the magnitude of $S^{1}_{Ki,max}$ is 0.063 at moderate frequency values; then, the sensitivity of the sub-model decreases again with increasing frequency.

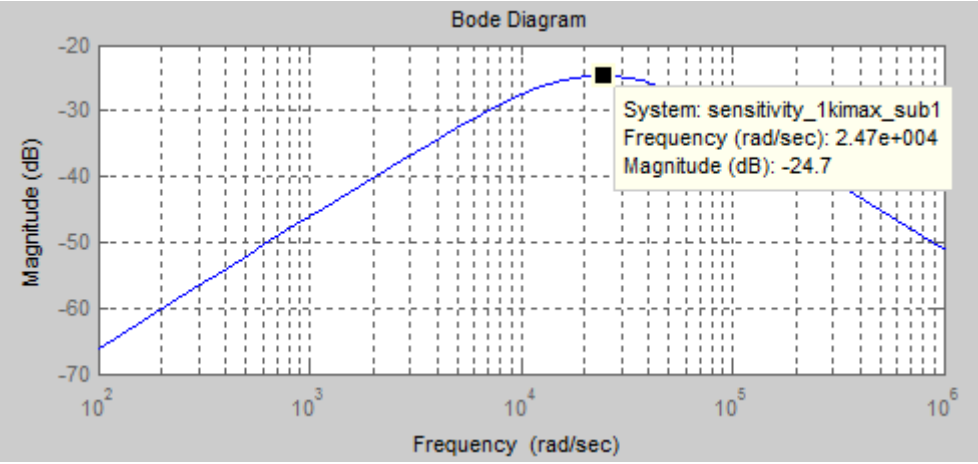


Figure 4-21. Magnitude response of $S_{Ki,max\_1}(s)$.

Similarly, for K_i=93858.13, the overall transfer function of the sub-model shown in Figure 3-28 becomes as:

$$H_1''(s) = \frac{247.5s+5.162e006}{8.425s+1.549e005} \quad (4.25)$$

Step response and bode plot of the new sub-model are shown in Figure 4-22 and Figure 4-23. The results show that the decrease in the value of K_i has almost no effect on the corresponding sub-model.

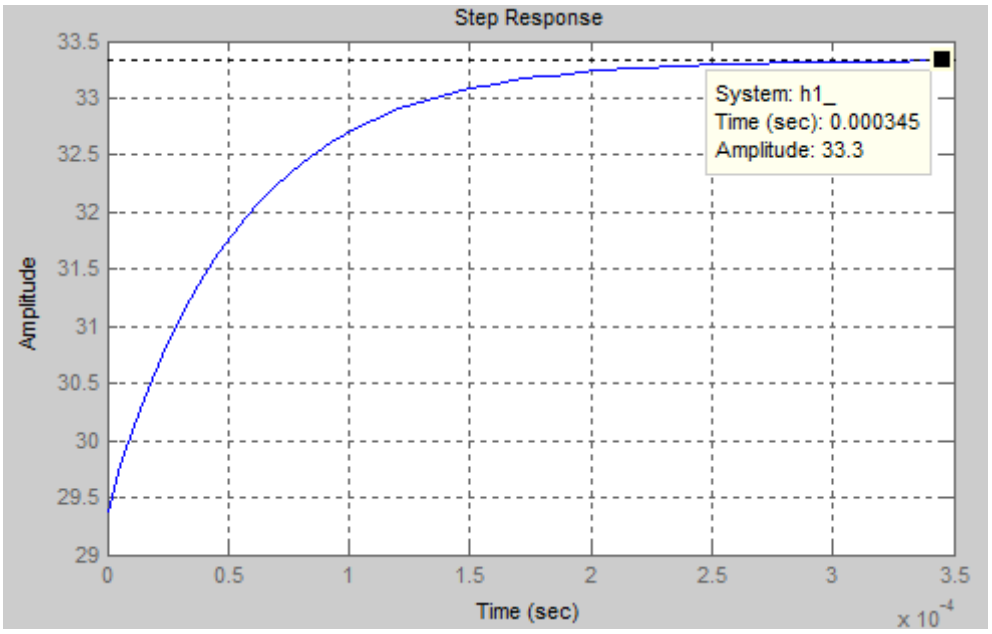


Figure 4-22. Step response of the new sub-model in response to decrease in K_i.

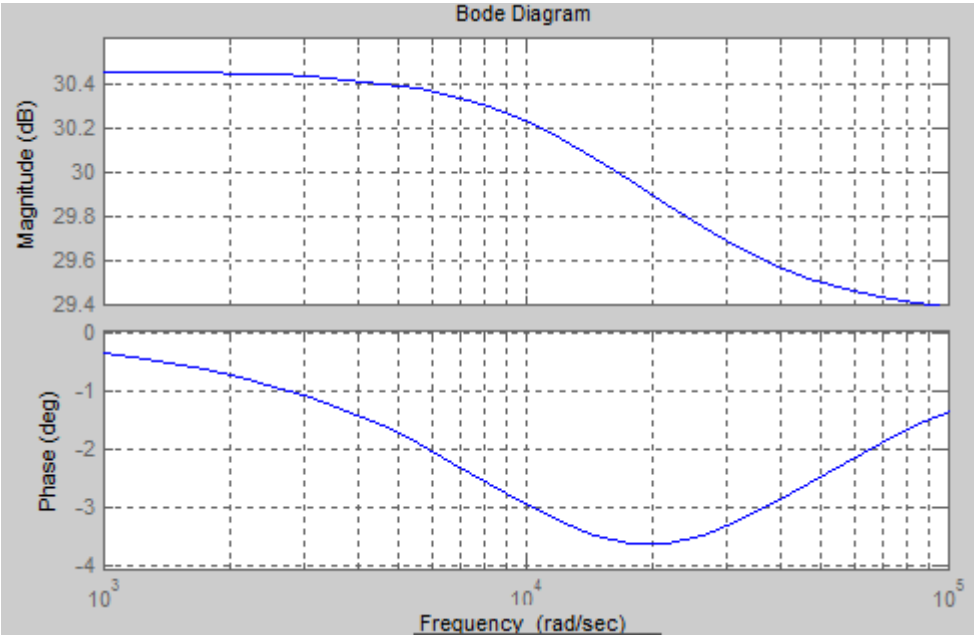


Figure 4-23. Bode plot of the new sub-model in response to decrease in K_i.

The sensitivity of the sub-model shown in Figure 3-28 to decrease in the value of K_i can be calculated as:

$$S^1_{Ki,min}(s) = \frac{\Delta H_1(s)/H_1(s)}{\Delta K_i/K_i} \tag{4.26}$$

$$S^1_{Ki,min}(s) = \frac{\frac{5.64e006s^2+1.171e011s+21.36}{1.757e004s^3+1.102e009s^2+2.291e013s+1.58e017}}{0.1488} \tag{4.27}$$

$$S^1_{Ki,min}(s) = \frac{4.913e007s^2+1.02e012s+186}{1.757e004s^3+1.102e009s^2+2.291e013s+1.58e017} \tag{4.28}$$

Magnitude plot of $S^1_{Ki,min}(s)$ is shown in Figure 4-24. It is observed that the sensitivity of the sub-model to the increase in the value of K_i is almost 0 until the moderate frequency values. Even, the magnitude of $S^1_{Ki,min}$ is 0.066 at moderate

frequency values; then, the sensitivity of the sub-model decreases again with increasing frequency.

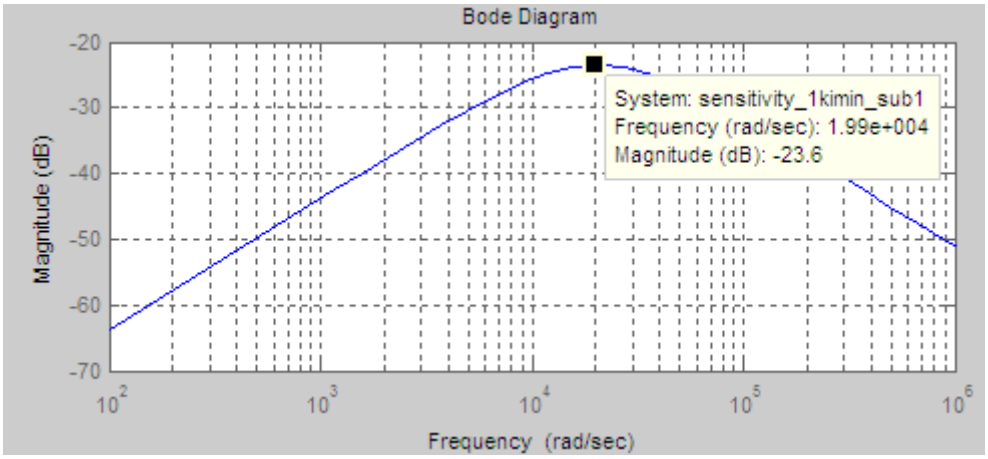


Figure 4-24. Magnitude response of $S_{Ki,min\_1}(s)$.

4.2.2.2 Sensitivity Analysis of the Closed Loop Sub-Model for the Constant DC Term with respect to the Integral Constant

For K_i=121809.35, the overall transfer function of the sub-model shown in Figure 3-29 becomes as:

$$H_2'(s) = \frac{55s}{8.425s+2.01e005} \tag{4.29}$$

Step response and bode plot of the new sub-model are shown in Figure 4-25 and Figure 4-26. The results show that the increase in the value of K_i has almost no effect on the corresponding sub-model.

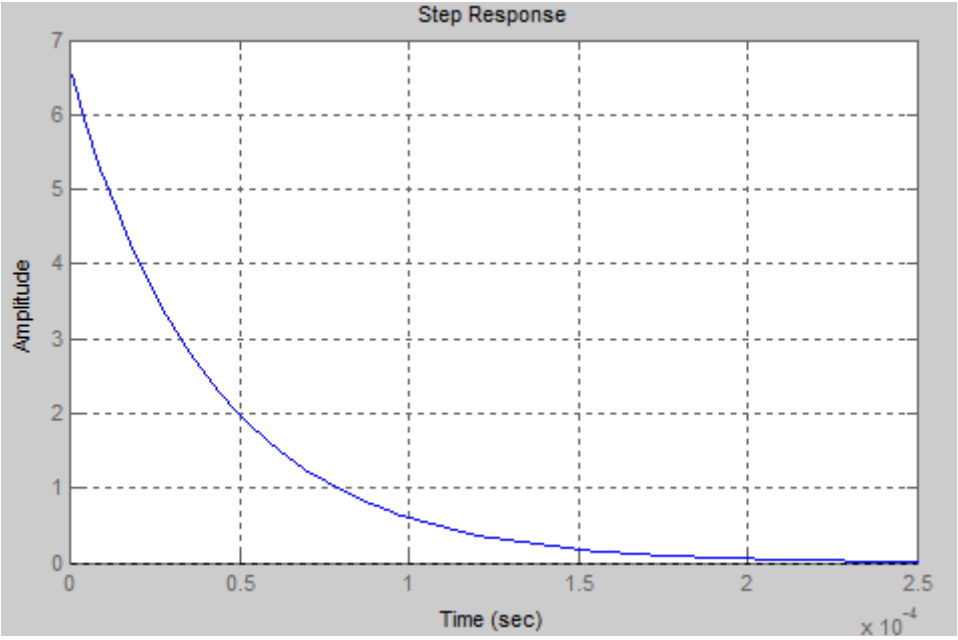


Figure 4-25. Step response of the new sub-model in response to increase in K_i.

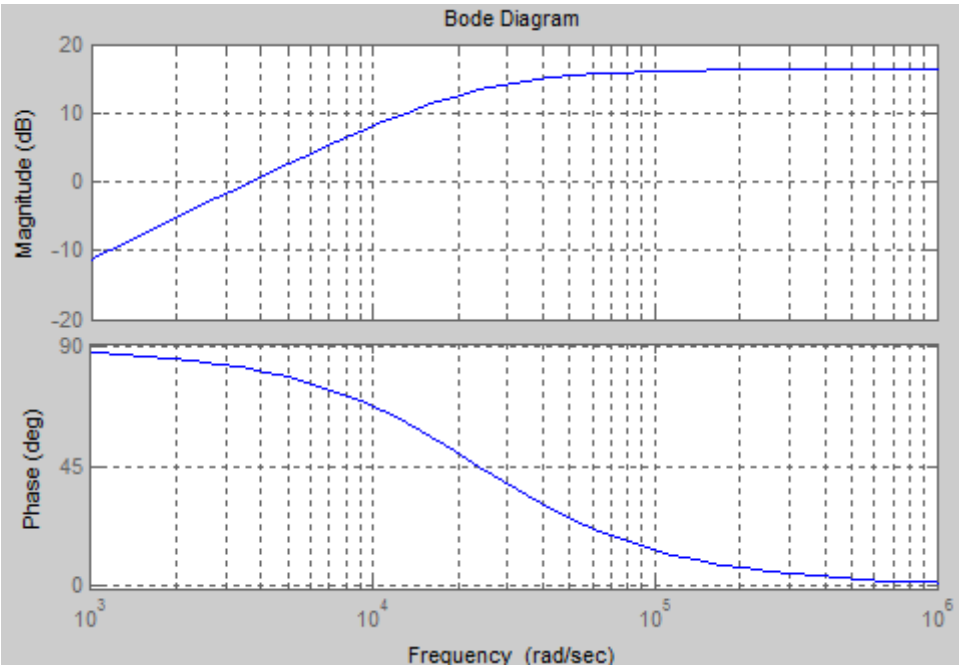


Figure 4-26. Bode plot of the new sub-model in response to increase in K_i.

The sensitivity of the sub-model shown in Figure 3-29 to increase in the value of K_i can be calculated as:

$$S^2_{Ki,max}(s) = \frac{\Delta H_2(s)/H_2(s)}{\Delta K_i/K_i} \tag{4.30}$$

where $\Delta H_2(s)$ and ΔK_i are the changes in the values of $H_2(s)$ and K_i. Accordingly;

$$S^2_{Ki,max}(s) = \frac{-\left(\frac{1.207e007s+2.505e011}{3904s^2+1.742e008s+1.934e012}\right)}{0.1488} \tag{4.31}$$

$$S^2_{Ki,max}(s) = -\left(\frac{8.107e007s+1.683e012}{3904s^2+1.742e008s+1.934e012}\right) \tag{4.32}$$

Magnitude plot of $S^2_{Ki,max}(s)$ is shown in Figure 4-27. It is observed that the sensitivity of the sub-model to the increase in the value of K_i is almost 0 at high frequencies and even less than 1 at low frequencies.

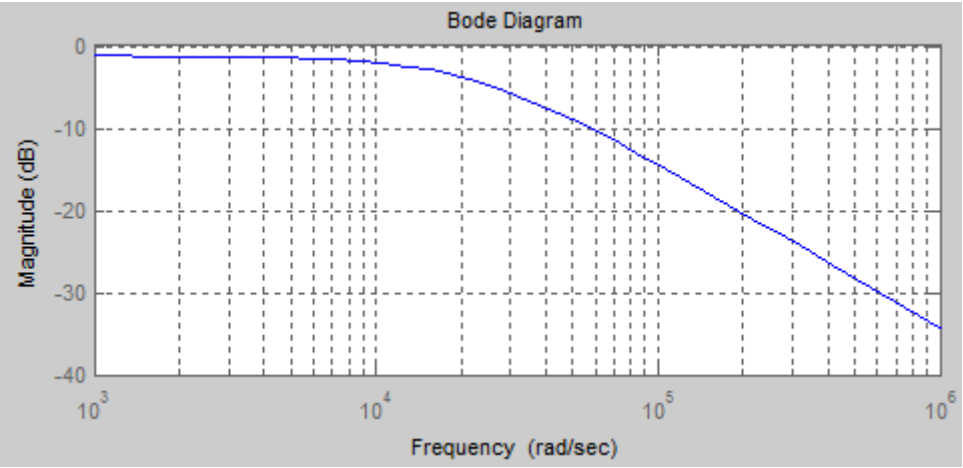


Figure 4-27. Magnitude response of $S_{Ki,max\_2}(s)$.

Similarly, for K_i=93858.13, the overall transfer function of the sub-model shown in Figure 3-29 becomes as:

$$H_2''(s) = \frac{55s}{8.425s+1.549e005} \tag{4.33}$$

Step response and bode plot of the new sub-model are shown in Figure 4-28 and Figure 4-29. The results show that the increase in the value of K_i has almost no effect on the corresponding sub-model.

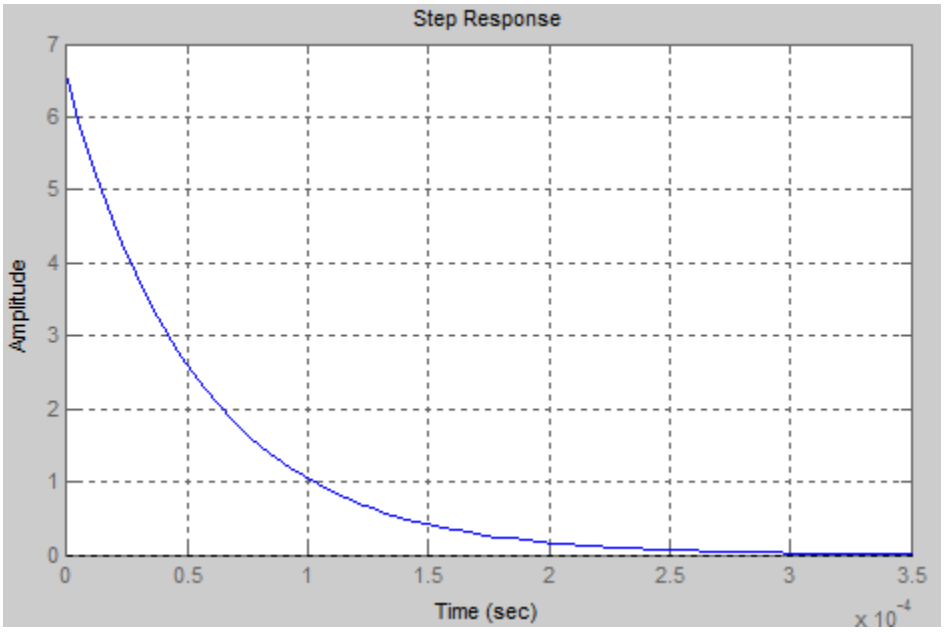


Figure 4-28. Step response of the new sub-model in response to decrease in K_i.

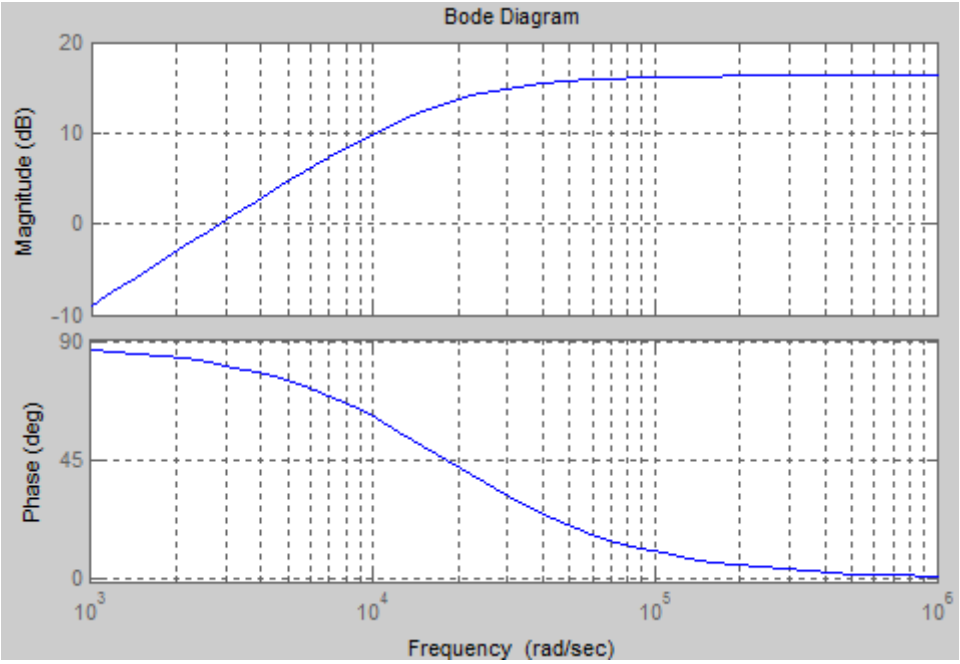


Figure 4-29. Bode plot of the new sub-model in response to decrease in K_i.

The sensitivity of the sub-model shown in Figure 3-29 to decrease in the value of K_i can be calculated as:

$$S^2_{Ki,min}(s) = \frac{\Delta H_2(s)/H_2(s)}{\Delta K_i/K_i} \tag{4.34}$$

$$S^2_{Ki,min}(s) = \frac{-\left(\frac{9.305e006s+1.932e011}{3904s^2+1.528e008s+1.49e012}\right)}{0.1488} \tag{4.35}$$

$$S^2_{Ki,min}(s) = -\left(\frac{8.107e007s+1.683e012}{3904s^2+1.528e008s+1.49e012}\right) \tag{4.36}$$

Magnitude plot of $S^2_{Ki,min}(s)$ is shown in Figure 4-30. It is observed that the sensitivity of the sub-model to the increase in the value of K_i is almost 0 at high frequencies. However, it seems that the system is slightly sensitive to the increase

in the value of K_i at low frequencies because magnitude of $S^2_{Ki,min}(s)$ is slightly greater than 1.

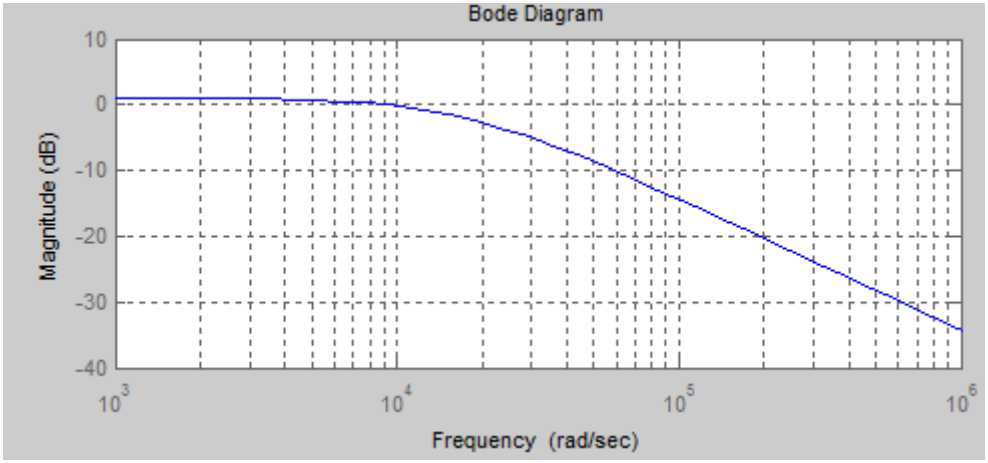


Figure 4-30. Magnitude response of $S_{Ki,min\_2}(s)$.

4.2.3 Sensitivity Analysis with respect to the Transconductance Parameter

K_n parameter of MOSFET is a dynamic parameter and it may vary due to transistor mismatches. As it is stated before, K_n parameter of the low side MOSFETs are calculated as $110A/V^2$. In the analysis, the effect of a drastic increase in the value of K_n parameter of the MOSFETs are tested.

4.2.3.1 Sensitivity Analysis of the Closed Loop Sub-Model for Step Input Current Command with respect to the Transconductance Parameter

For $K_n=220A/V^2$, the overall transfer function of the sub-model shown in Figure 3-28 becomes as:

$$H_1'(s) = \frac{495s+1.116e007}{15.85s+3.499e005} \quad (4.37)$$

Step response and bode plot of the new sub-model are shown in Figure 4-31 and Figure 4-32. The results show that the increase in the value of K_n causes a decrease in the bandwidth of the corresponding sub-model. However, the steady-state value of the step response of the system does not change.

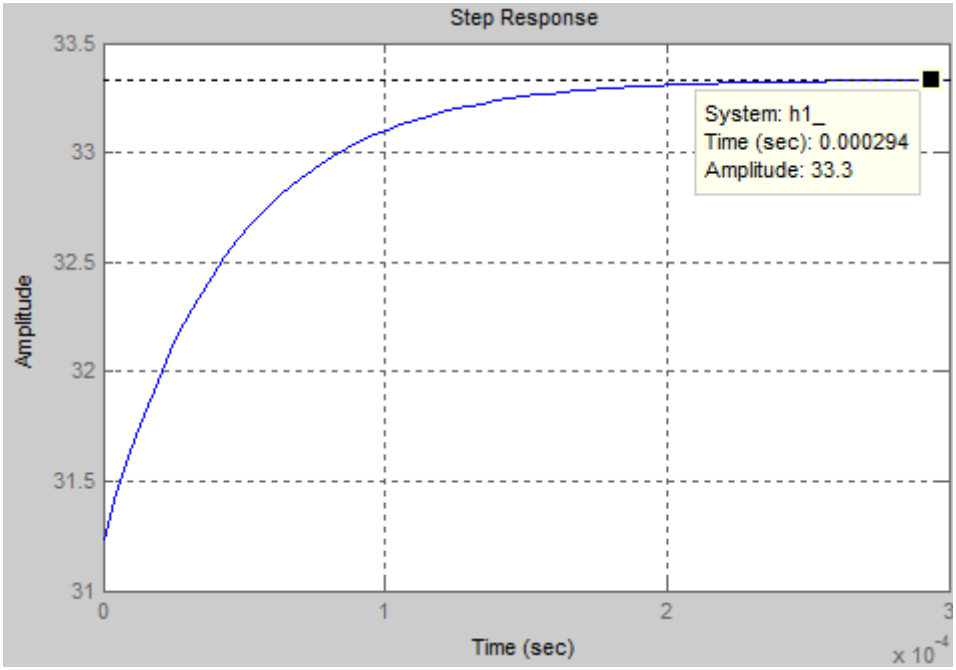


Figure 4-31. Step response of the new sub-model in response to increase in K_n.

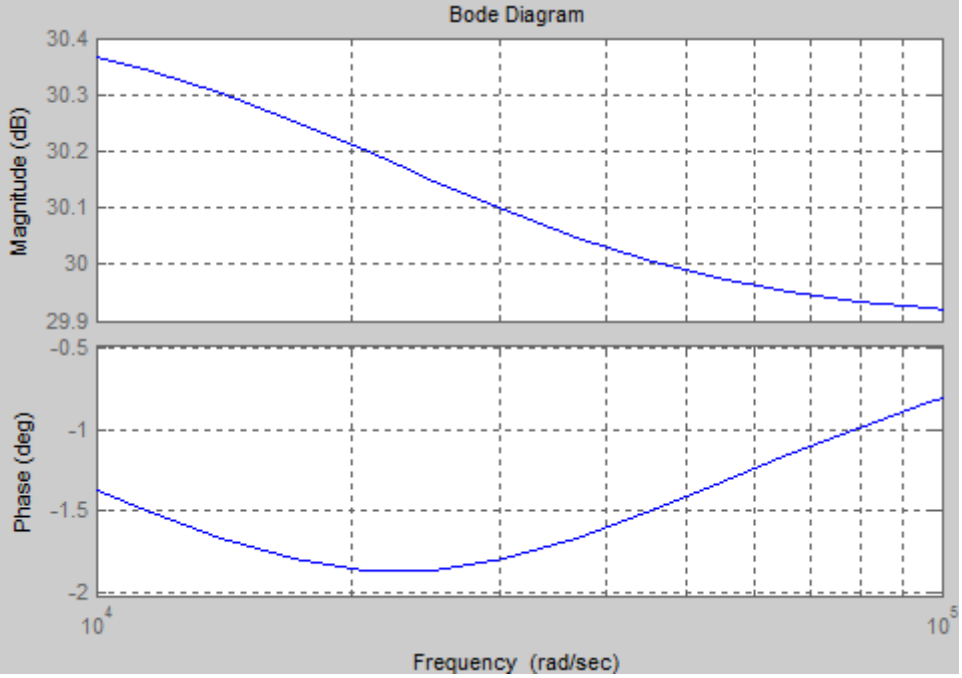


Figure 4-32. Bode plot of the new sub-model in response to increase in K_n.

The sensitivity of the sub-model shown in Figure 3-28 to increase in the value of K_n can be calculated as:

$$S^{1}_{Kn,220}(s) = \frac{\Delta H_1(s)/H_1(s)}{\Delta K_n/K_n} \tag{4.38}$$

where $\Delta H_1(s)$ and ΔK_n are the changes in the values of $H_1(s)$ and K_n. Accordingly;

$$S^{1}_{Kn,220}(s) = \frac{\frac{2085s^3+9.243e007s^2+6.555e012s}{3.305e004s^3+2.195e009s^2+4.851e013s+3.57e017}}{1} \tag{4.39}$$

$$S^{1}_{Kn,220}(s) = \frac{2085s^3+9.243e007s^2+6.555e012s}{3.305e004s^3+2.195e009s^2+4.851e013s+3.57e017} \tag{4.40}$$

Magnitude plot of $S^{1}_{Kn,220}(s)$ is shown in Figure 4-33. It is observed that the sensitivity of the sub-model to the increase in the value of K_n is very low. In fact, K_n is modeled as a gain parameter of the plant function of the sub-model with V_{DS} of the MOSFETs and it would be expected that any increase in the value of K_n affect the response of the system dramatically. However, as it is seen from both Figure 4-31, Figure 4-32 and Figure 4-33, the sensitivity of the system in response to variation in the value of K_n is very low.

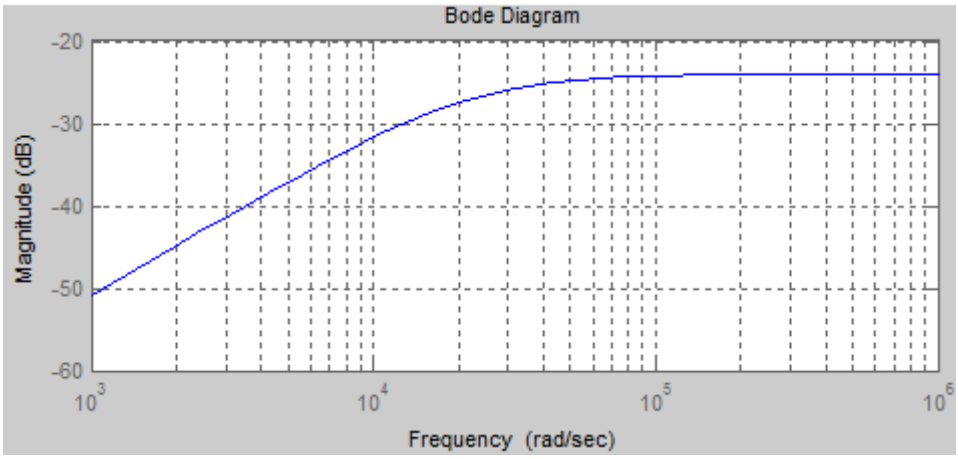


Figure 4-33. Magnitude response of $S_{Kn,220\_1}(s)$.

4.2.3.2 Sensitivity Analysis of the Closed Loop Sub-Model for Constant DC Term with respect to the Transconductance Parameter

For K_n=110A/V^2, the overall transfer function of the sub-model shown in Figure 3-29 becomes as:

$$H_2'(s) = \frac{110s}{15.85s+3.499e005} \tag{4.41}$$

Step response and bode plot of the new sub-model are shown in Figure 4-34 and Figure 4-35. The results show that the increase in the value of K_n has almost no effect on the corresponding sub-model.

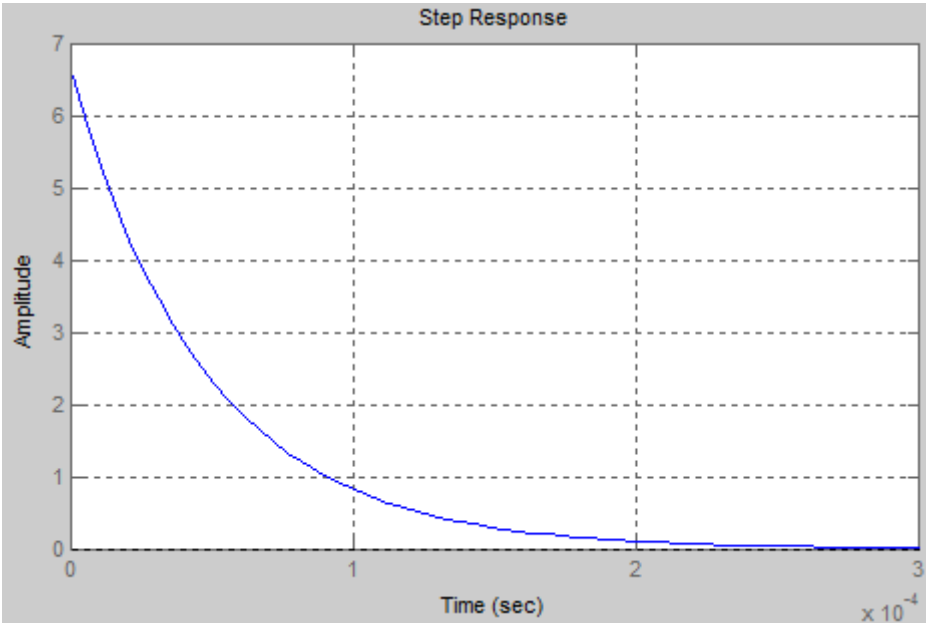


Figure 4-34. Step response of the new sub-model in response to increase in K_n.

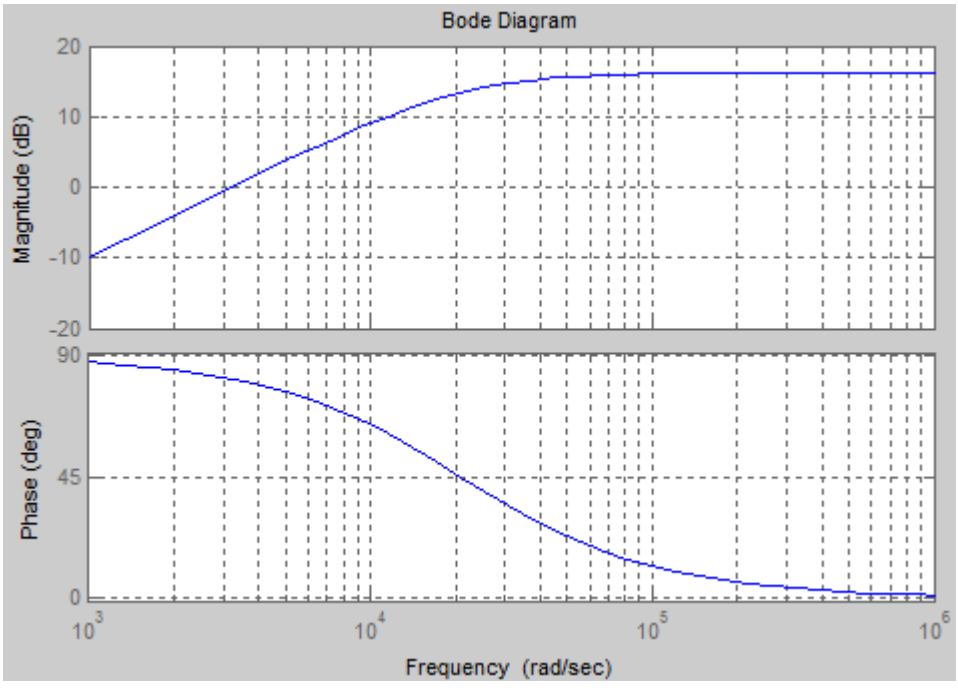


Figure 4-35. Bode plot of the new sub-model in response to increase in K_n.

The sensitivity of the sub-model shown in Figure 3-29 to increase in the value of K_n can be calculated as:

$$S^2_{Kn,220}(s) = \frac{\Delta H_2(s)/H_2(s)}{\Delta K_n/K_n} \tag{4.42}$$

where $\Delta H_2(s)$ and ΔK_n are the changes in the values of $H_2(s)$ and K_n. Accordingly;

$$S^2_{Kn,220}(s) = \frac{\frac{463.4s^2+9.622e006s}{7344s^2+3.146e008s+3.367e012}}{1} \tag{4.43}$$

$$S^2_{Kn,220}(s) = \frac{463.4s^2+9.622e006s}{7344s^2+3.146e008s+3.367e012} \tag{4.44}$$

Magnitude plot of $S^2_{Kn,220}(s)$ is shown in Figure 4-36. It is observed that the sensitivity of the sub-model to the increase in the value of K_n is very low like the other sub-model.

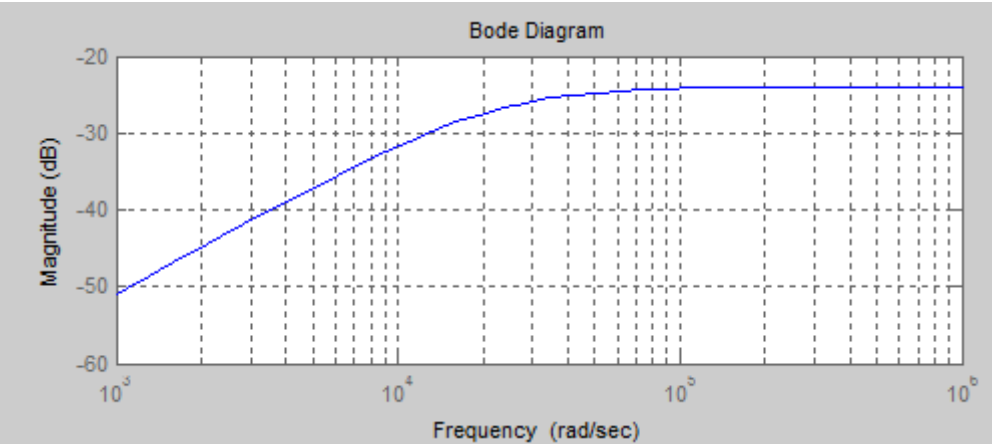


Figure 4-36. Magnitude response of $S_{Kn,220\_2}(s)$.

4.2.4 Sensitivity Analysis with respect to the Total Feedback Gain

The values of the resistances comprising the feedback gain, which has the value of 0.25kΩ, 0.5kΩ and 10mΩ as shown in Figure 3-10 and Figure 3-5. Any variation in these values directly affects the value of the LD current. Considering the tolerances in the values of the resistances, the maximum and minimum value of the feedback gain can be calculated as below:

$$F_{max}=\frac{0.5k\Omega\times1.01+0.25k\Omega\times0.99}{0.25k\Omega\times0.99}\times(0.01\Omega\times1.001)\ =0.0304 \quad (4.45)$$

$$F_{min}=\frac{0.5k\Omega\times0.99+0.25k\Omega\times1.01}{0.25k\Omega\times1.01}\times(0.01\Omega\times0.999)\ =0.0296 \quad (4.46)$$

4.2.4.1 Sensitivity Analysis of the Closed Loop Sub-Model for Step Input Current Command with respect to the Total Feedback Gain

For F=0.0304, the overall transfer function of the sub-model shown in Figure 3-28 becomes as:

$$H_1'(s)=\frac{247.5s+5.832e006}{8.524s+1.773e005} \quad (4.47)$$

Step responses of the actual sub-model and new sub-model are shown in Figure 4-37 and Figure 4-38. The results show that the increase in the value of F causes a 1.2A-decrease in the value of the LD current at steady-state, which is an expected result due to change in the value of the LD current information coming from the feedback.

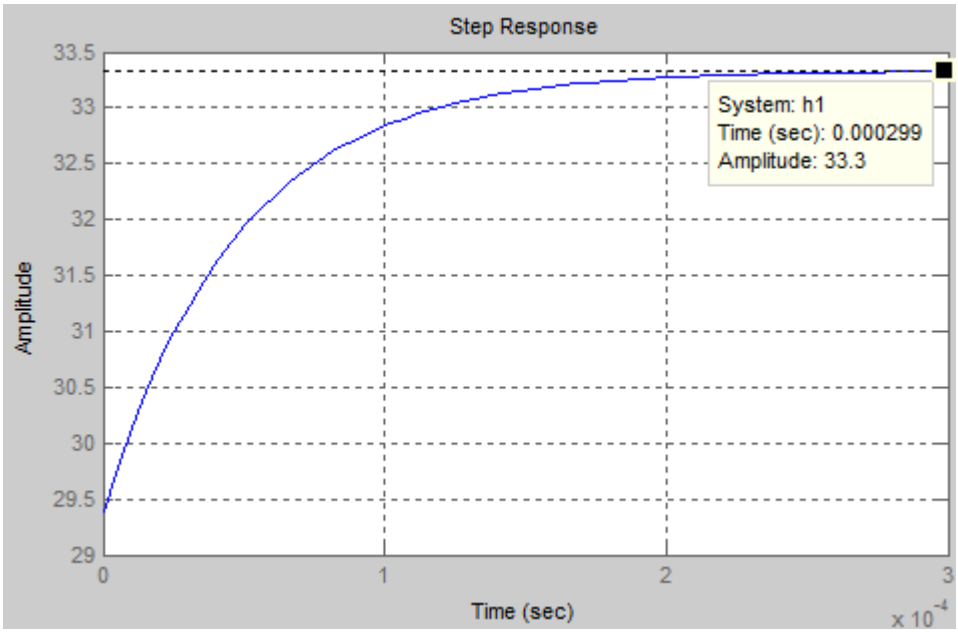


Figure 4-37. Step response of the actual sub-model.

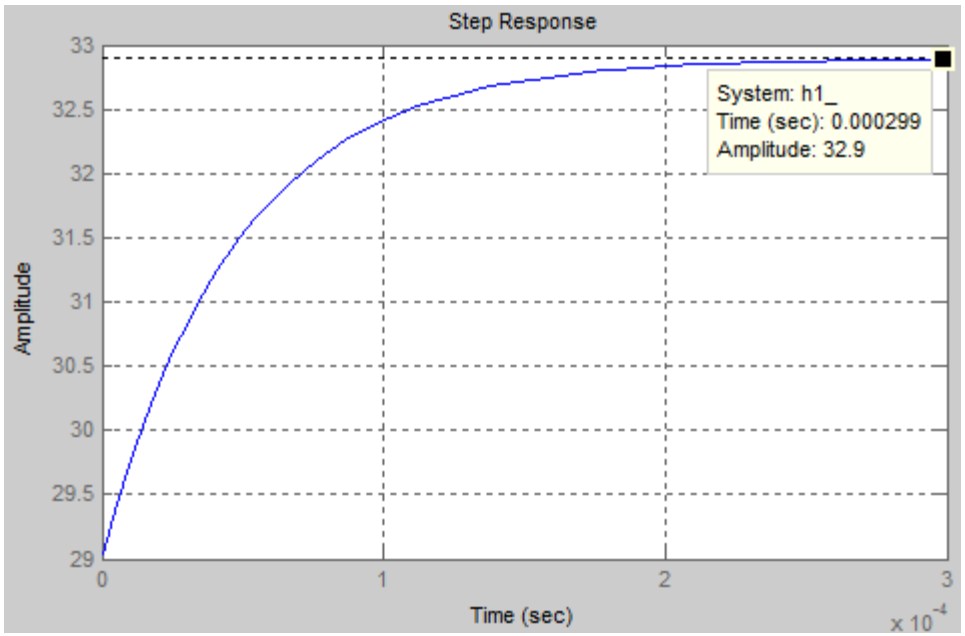


Figure 4-38. Step response of the new sub-model in response to increase in F.

The sensitivity of the sub-model shown in Figure 3-28 to increase in the value of K_p can be calculated as:

$$S^1_{F,max}(s) = \frac{{}^{\Delta H_1(s)}/_{H_1(s)}}{{}^{\Delta F}/_{F}} \tag{4.48}$$

where $\Delta H_1(s)$ and ΔF are the changes in the values of $H_1(s)$ and F. Accordingly;

$$S^1_{F,max}(s) = \frac{-\left(\frac{206.4s^3+1.401e007s^2+3.166e011s+2.38e015}{1.774e004s^3+1.158e009s^2+2.508e013s+1.809e017}\right)}{0.0133} \tag{4.49}$$

$$S^1_{F,max}(s) = -\left(\frac{1.548e004s^3+1.051e009s^2+2.375e013s+1.785e017}{1.774e004s^3+1.158e009s^2+2.508e013s+1.809e017}\right) \tag{4.50}$$

Magnitude plot of $S^1_{F,max}(s)$ is shown in Figure 4-39. It is observed that the sensitivity of the sub-model to the increase in the value of F is even less than 1 at low frequencies which is an expected result and decreases with increasing frequency.

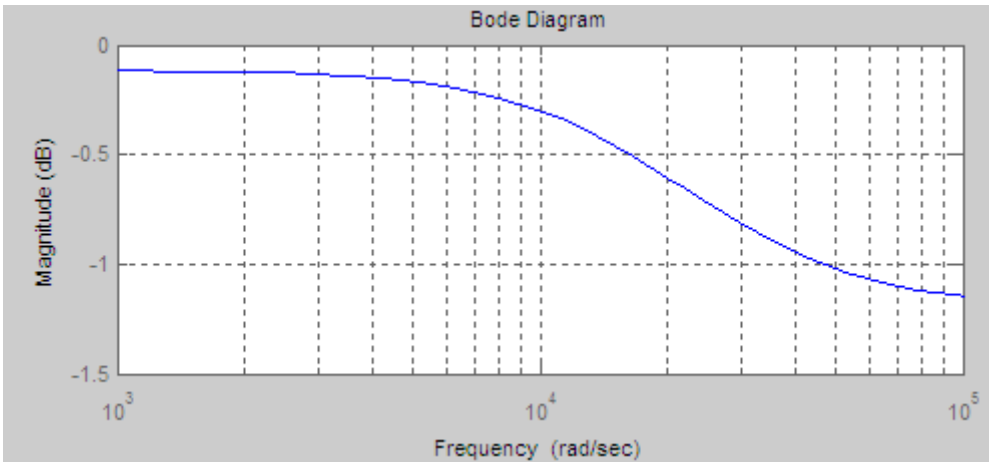


Figure 4-39. Magnitude response of $S_{F,max\_1}(s)$.

Similarly, for F=0.0296, the overall transfer function of the sub-model shown in Figure 3-28 becomes as:

$$H_1''(s) = \frac{247.5s+5.832e006}{8.326s+1.726e005} \tag{4.51}$$

Step response of the new sub-model is shown in Figure 4-40. The results show that the decrease in the value of F causes a 1.5A-increase in the value of the LD current at steady-state, which is an expected result due to change in the value of the LD current information coming from the feedback.

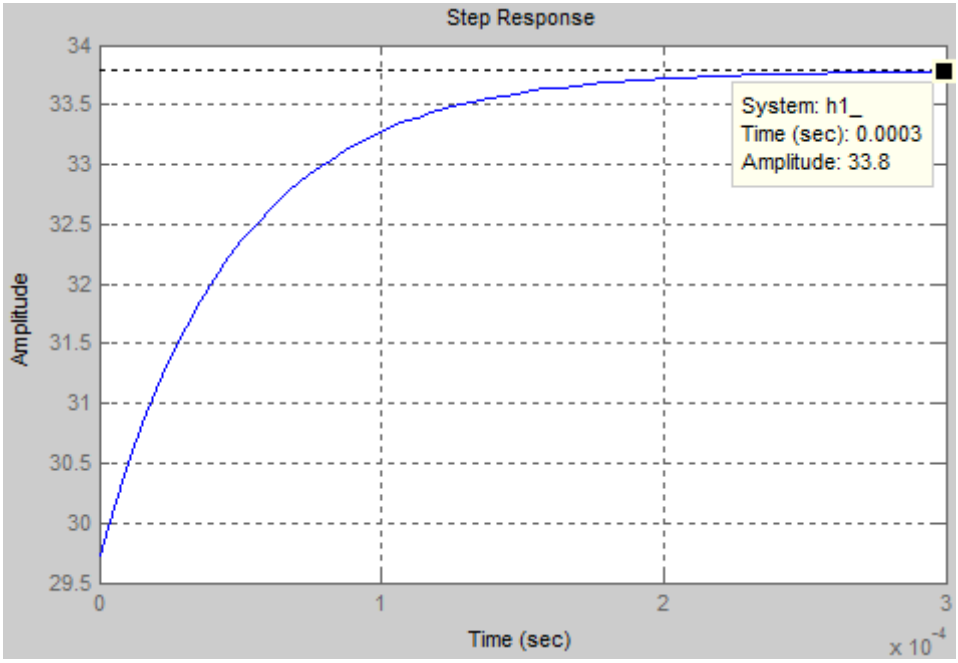


Figure 4-40. Step response of the new sub-model in response to decrease in F.

The sensitivity of the sub-model shown in Figure 3-28 to increase in the value of F can be calculated as:

$$S_{F,min}^{1}(s) = \frac{\Delta H_1(s)/H_1(s)}{\Delta F/F} \tag{4.52}$$

$$S_{F,min}^{1}(s) = \frac{\frac{206.4s^3+1.401e007s^2+3.166e011s+2.38e015}{1.736e004s^3+1.138e009s^2+2.445e013s+1.761e017}}{-0.0133} \tag{4.53}$$

$$S^1_{F,min}(s) = -\left(\frac{1.548e004s^3+1.051e009s^2+2.375e013s+1.785e017}{1.736e004s^3+1.138e009s^2+2.445e013s+1.761e017}\right) \quad (4.54)$$

Magnitude plot of $S^1_{F,min}(s)$ is shown in Figure 4-41. It is observed that the sensitivity of the sub-model to the decrease in the value of F is slightly greater than 1 at low frequencies, which is an expected result and decreases with increasing frequency.

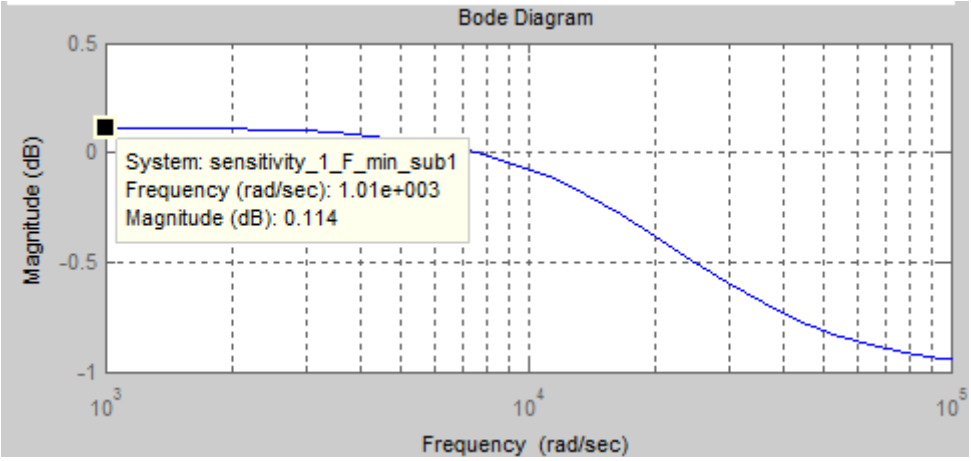


Figure 4-41. Magnitude response of $S_{F,min\_1}(s)$.

The closed loop system is sensitive to the variations in total feedback gain which may cause a 1A deviation in the value of the LD current, which can be handled by using more precise resistors in the feedback of the closed loop system.

4.2.4.2 Sensitivity Analysis of the Closed Loop Sub-Model for Constant DC Term with respect to the Total Feedback Gain

For F=0.0304, the overall transfer function of the sub-model shown in Figure 3-29 becomes as:

$$H_2'(s) = \frac{55s}{8.524s+1.773e005} \tag{4.55}$$

Step responses of the actual sub-model and new sub-model are shown in Figure 4-42 and Figure 4-43. The results show that the increase in the value of F has almost no effect on the corresponding sub-model because the steady-state value of the step response of the corresponding sub-model is 0.

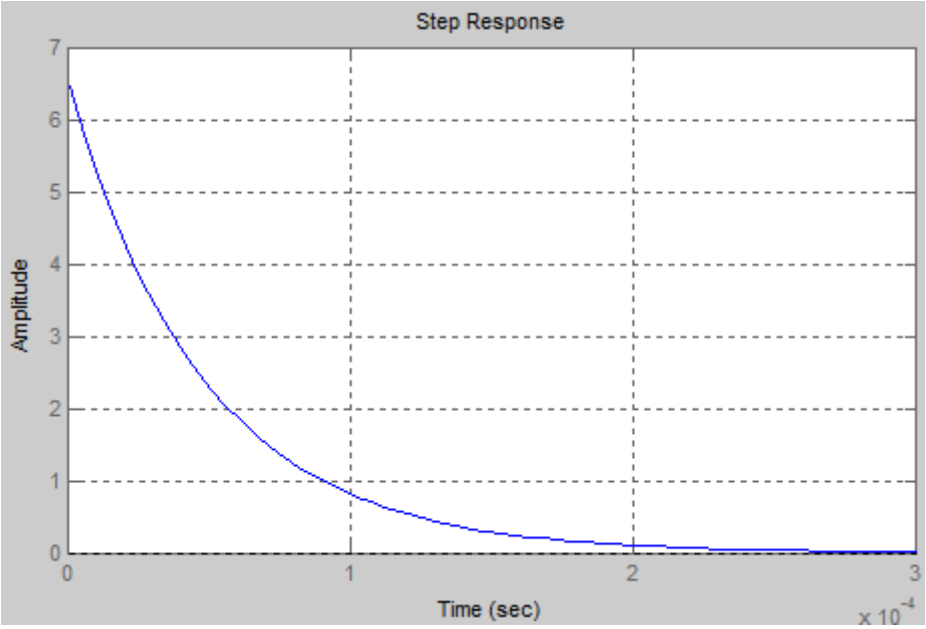


Figure 4-42. Step responses of the actual sub-model.

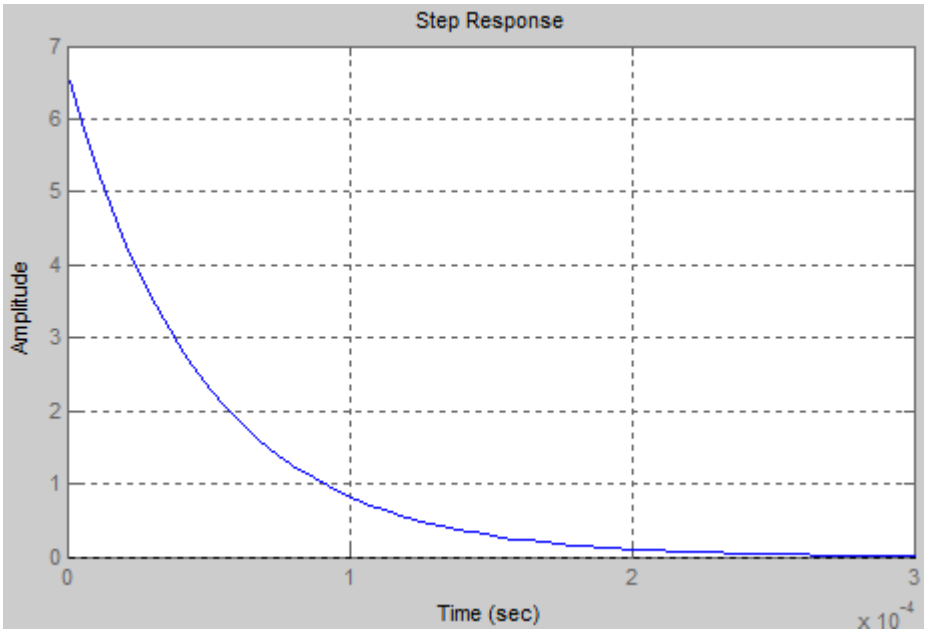


Figure 4-43. Step response of the new sub-model in response to increase in F.

The sensitivity of the sub-model shown in Figure 3-29 to increase in the value of K_p can be calculated as:

$$S^2_{F,max}(s) = \frac{\Delta H_2(s)/H_2(s)}{\Delta F/F} \tag{4.56}$$

where $\Delta H_2(s)$ and ΔF are the changes in the values of $H_2(s)$ and F. Accordingly;

$$S^2_{F,max}(s) = \frac{-\left(\frac{45.87s^2+2.033e006s+2.244e010}{3950s^2+1.642e008s+1.706e012}\right)}{0.0133} \tag{4.57}$$

$$S^2_{F,max}(s) = -\left(\frac{3441s^2+1.525e008s+1.683e012}{3950s^2+1.642e008s+1.706e012}\right) \tag{4.58}$$

Magnitude plot of $S^2_{F,max}(s)$ is shown in Figure 4-44. It is observed that the corresponding sub-model is almost insensitive to the increase in the value of F.

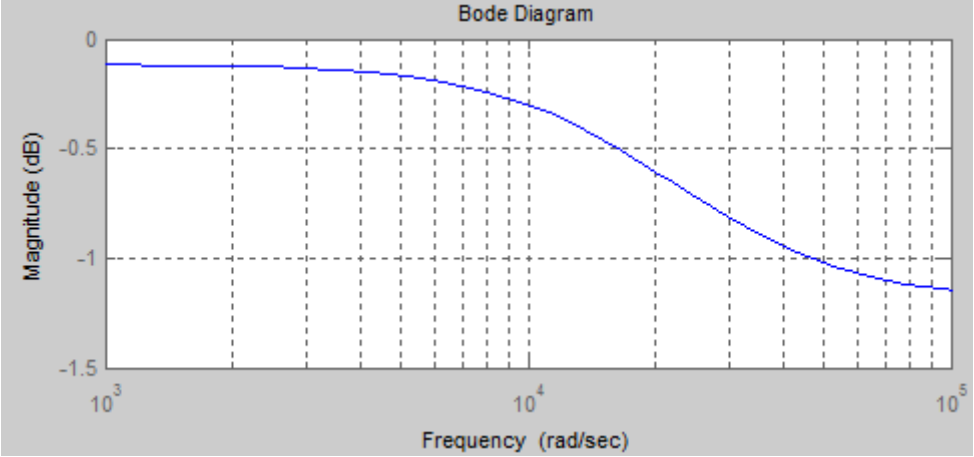


Figure 4-44. Magnitude response of $S_{F,max\_2}(s)$.

Similarly, for F=0.0296, the overall transfer function of the sub-model shown in Figure 3-29 becomes as:

$$H_2''(s) = \frac{55s}{8.326s+1.726e005} \tag{4.59}$$

Step response of the new sub-model is shown in Figure 4-40. The results show that the decrease in the value of F has almost no effect on the response of the corresponding sub-model.

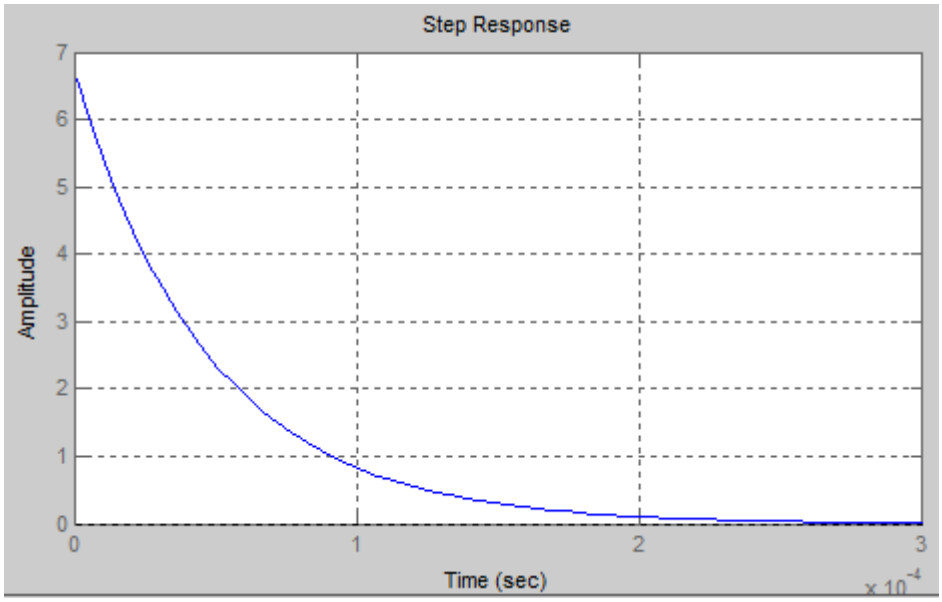


Figure 4-45. Step response of the new sub-model in response to decrease in F.

The sensitivity of the sub-model shown in Figure 3-29 to increase in the value of F can be calculated as:

$$S^2_{F,min}(s) = \frac{\Delta H_2(s)/H_2(s)}{\Delta F/F} \tag{4.60}$$

$$S^2_{F,min}(s) = \frac{-\left(\frac{45.87s^2+2.033e006s+2.244e010}{3858s^2+1.601e008s+1.661e012}\right)}{0.0133} \tag{4.61}$$

$$S^2_{F,min}(s) = -\left(\frac{3441s^2+1.525e008s+1.683e012}{3858s^2+1.601e008s+1.661e012}\right) \tag{4.62}$$

Magnitude plot of $S^2_{F,min}(s)$ is shown in Figure 4-46. It is observed that the sensitivity of the sub-model to the decrease in the value of F is slightly more than 1 at low frequencies which is considered that it is insufficient to disturb the response of the overall system.

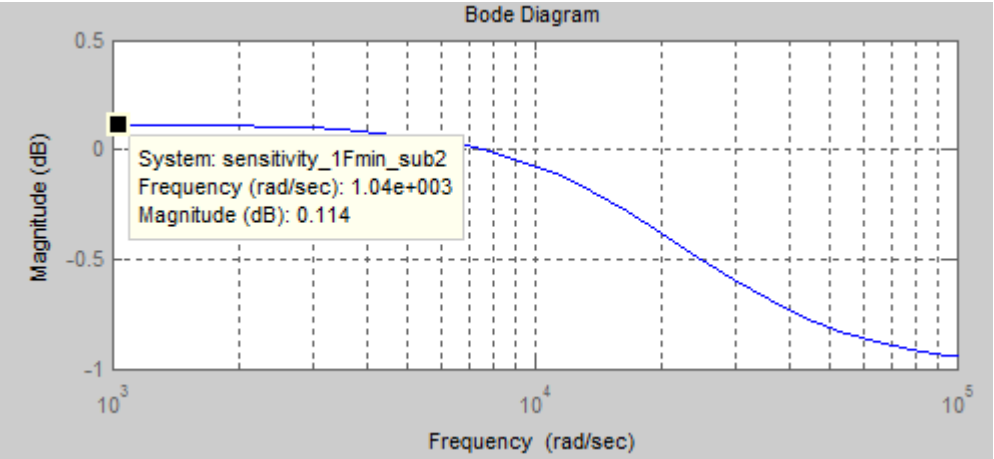


Figure 4-46. Magnitude response of $S_{F,min\_2}(s)$.

4.3 Sensitivity Analysis of the Transient Response of the Closed Loop Current Control

In this part of the thesis, the factors affecting the transient response of the closed loop current control of the LD driver is analysed. One of these factors is the value of the additional gate resistor for each low side MOSFET. The other factors are the values of the proportional constant (K_p) and the integral constant (K_i) which also affects the steady-state response of the system as stated in previous section.

4.3.1 Effect of the Additional Gate Resistor on the Closed Loop Current Control

The value of the additional gate resistor is very critical for the performance of the driver. If the value of the resistor is extremely high, then the rise time and the fall time of the load current become high. On the other hand, if the value of the resistor is extremely low or not high enough, the overshoot or the oscillations on the load current can be observed. Hence, there is a trade-off between rise and fall times and the overshoot characteristics of the load current. Figure 4-47 shows the simulation results of two cases which are the gate drive with low resistance value

and the one with high resistance value. The amplitude of the input command is determined as 1.5V so as to generate 100A current flowing through the LD series. As it is observed from Figure 4-47 (a), there are too many oscillations observed on the load current for only 100Ω MOSFET gate resistance, which disturbs the stability of system. On the other hand, in Figure 4-47 (b), no oscillations or even an overshoot are observed on the load current when the gate resistance of the MOSFET is increased to 3kΩ. However, rise and fall times of the current are measured as 20µs and 30µs, respectively, which are larger than 10µs. As a result, the value of the additional gate charge resistor is selected as 1.33kΩ. Accordingly, the resultant LD current is obtained both theoretically and experimentally as shown in Figure 3-18 and Figure 4-3, respectively. While theoretical rise time and fall time measurements of the LD current are approximately 9µs and 0.55µs, respectively; experimental rise time and fall time measurements of the LD current are 9.45µs and 1.2µs, respectively.

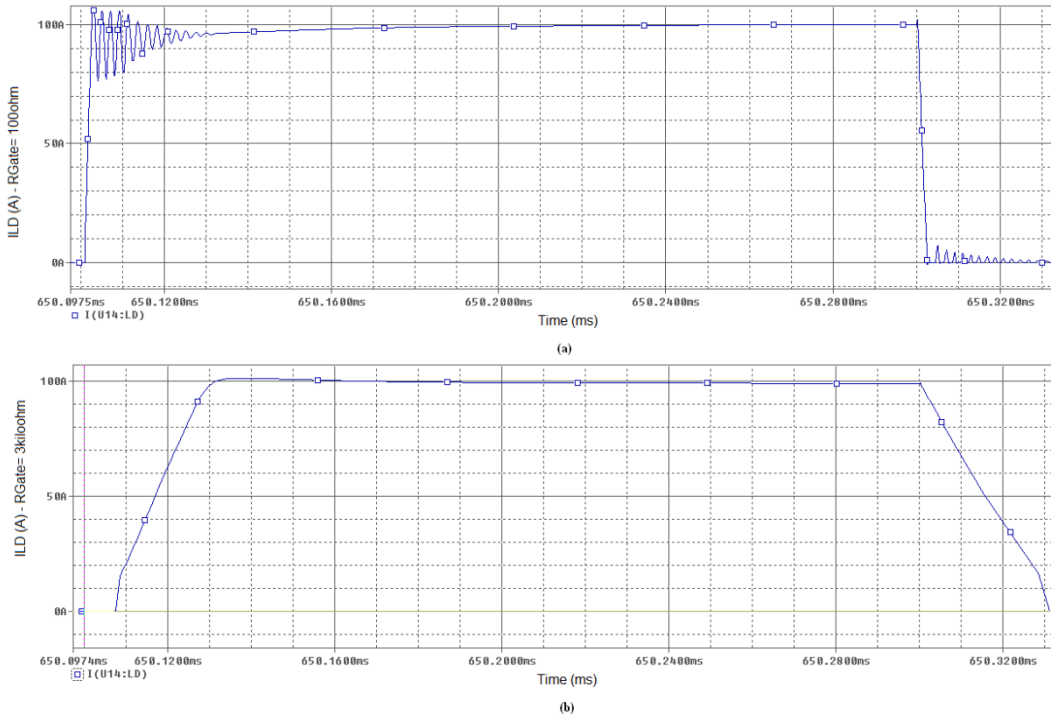


Figure 4-47. ORCAD simulations of 100A LD current (a) for 100Ω gate resistance, (b) for 3kΩ gate resistance.

4.3.2 Sensitivity Analysis with respect to the Proportional Constant

The effect of the variation in the value of the resultant K_p due to tolerances in the values of the resistances on the steady-state response of the system was analysed in previous section. In this part, further increase and decrease in the value of the resultant K_p is analysed both using MATLAB on the developed closed loop sub-model for steady-state response of the system and the ORCAD simulations. Although the closed loop sub-model may not give precise results for the transient response of the system, it gives a general idea about the transient behaviour of the LD current.

In these analyses, the new values of K_p are determined as 100 and 1 to see further increase and decrease in its value.

4.3.2.1 Effect of the Increase in the Value of the Proportional Constant

For K_p=100, the overall transfer function of the sub-model shown in Figure 3-28 becomes as:

$$H_1'(s) = \frac{5500s+5.832e006}{166s+1.749e005}$$

Step responses of the actual and the new sub-model are shown in Figure 4-48 and Figure 4-49. The results show that the increase in the value of K_p has decreased the rise time of the LD current from 8.44µs to nanosecond levels. However, since the switching behavior of the low side MOSFETs is not modeled in the corresponding sub-system, this analysis alone may not give completely an accurate result.

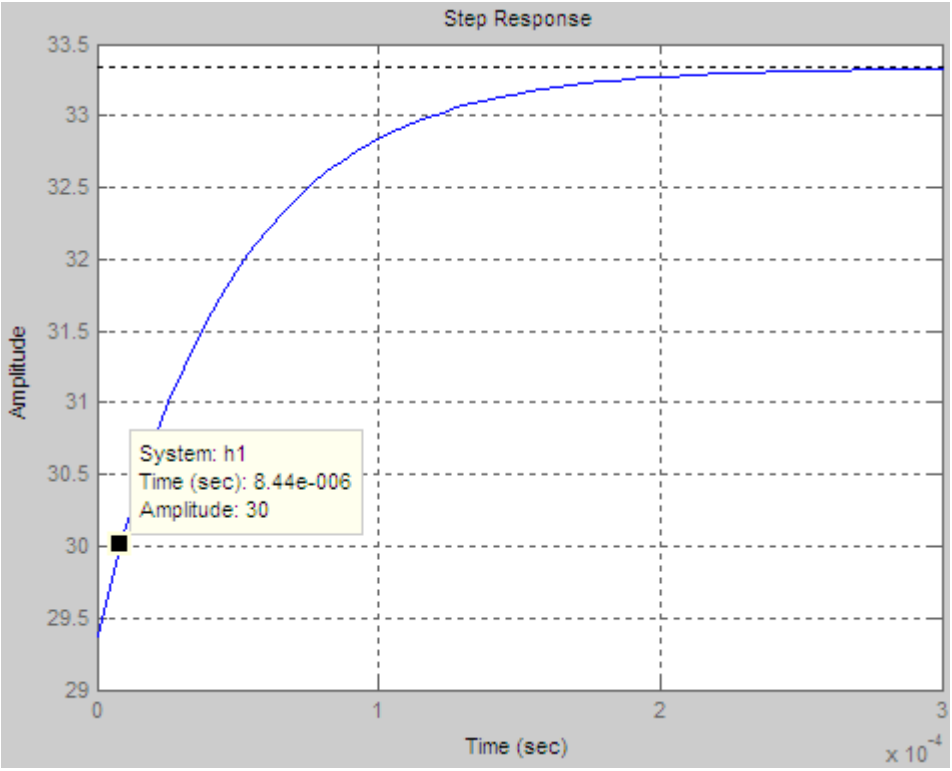


Figure 4-48. Step response of the actual sub-model.

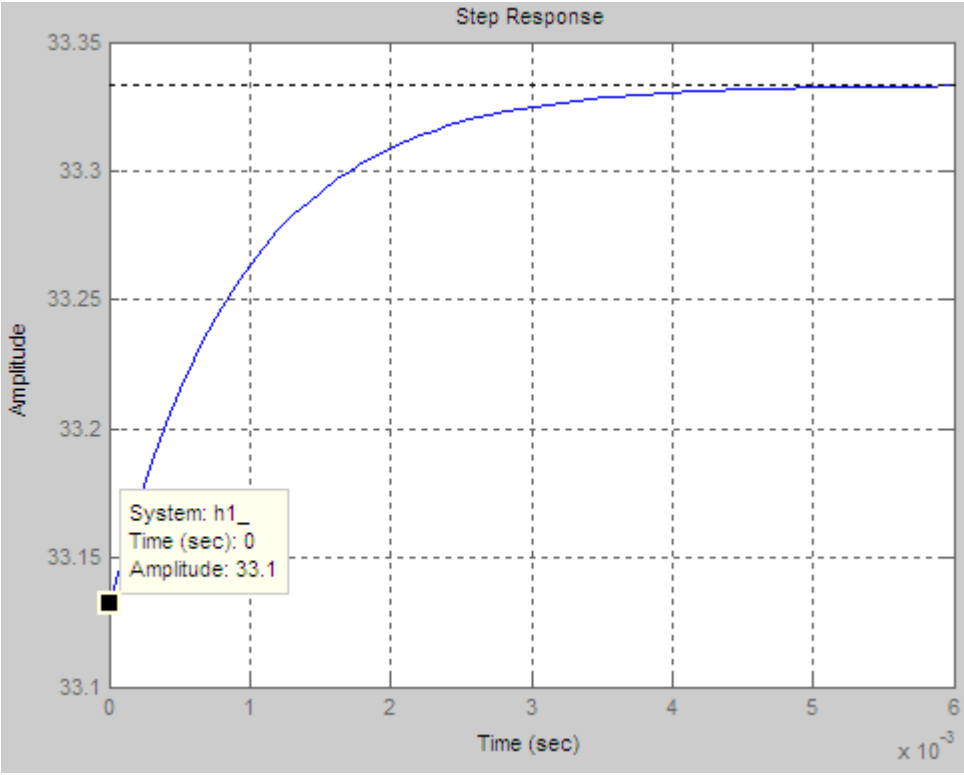


Figure 4-49. Step response of the new sub-model for K_p=100.

The more realistic analysis is made with the ORCAD simulations. Figure 4-50 shows the effect of the increase in the value of K_p on the transient behaviour of the LD current. While further increase in the value of K_p decrease the value of the rise time slightly, it causes overshoot and undershoot at load current. However, it is observed that the decrease in the rise time is limited to a value of 8µs because of the additional gate resistor.

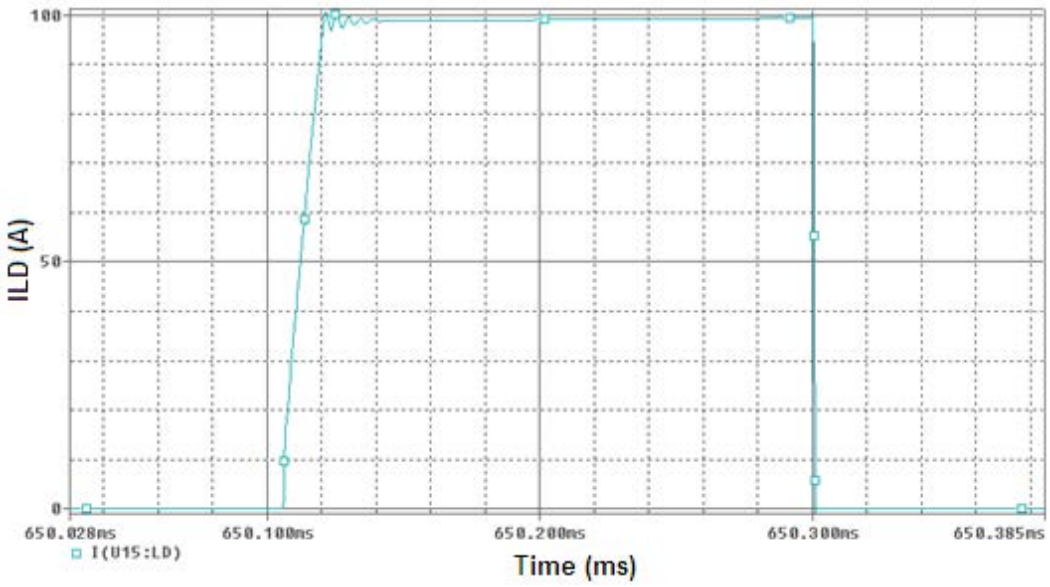


Figure 4-50. ORCAD simulation of the LD current with K_P=100.

4.3.2.2 Effect of the Decrease in the Value of the Proportional Constant

For K_p=1, the overall transfer function of the sub-model shown in Figure 3-28 becomes as:

$$H_1''(s) = \frac{55s+5.832e006}{2.65s+1.749e005}$$

Step responses of the actual and the new sub-model are shown in Figure 4-48 and Figure 4-51 The results show that the decrease in the value of K_p has increased the

rise time of the LD current from 8.44µs to 20µs. However, since the switching behavior of the low side MOSFETs is not modeled in the corresponding sub-model, this analysis alone may not give an accurate result.

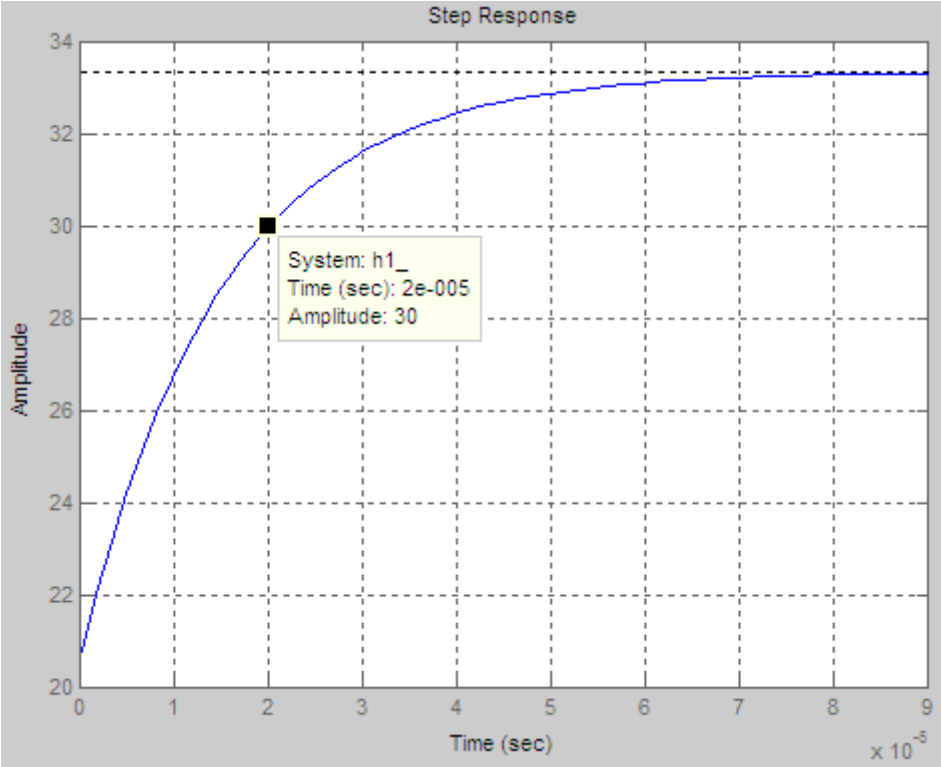


Figure 4-51. Step response of the new sub-model for K_p=1.

The more realistic analysis is made with the ORCAD simulations. Figure 4-52 shows the effect of the decrease in the value of K_p on the transient behaviour of the LD current. The decrease in the value of K_p has increased the value of the rise time from 9µs to 13µs. It has also caused an increase in the settling time of the load current. As it is seen from Figure 4-52, the load current cannot reach the steady-state value in 200µs pulse time period. This is an expected result, because further decrease in the value of K_p slowdowns the PI controller.

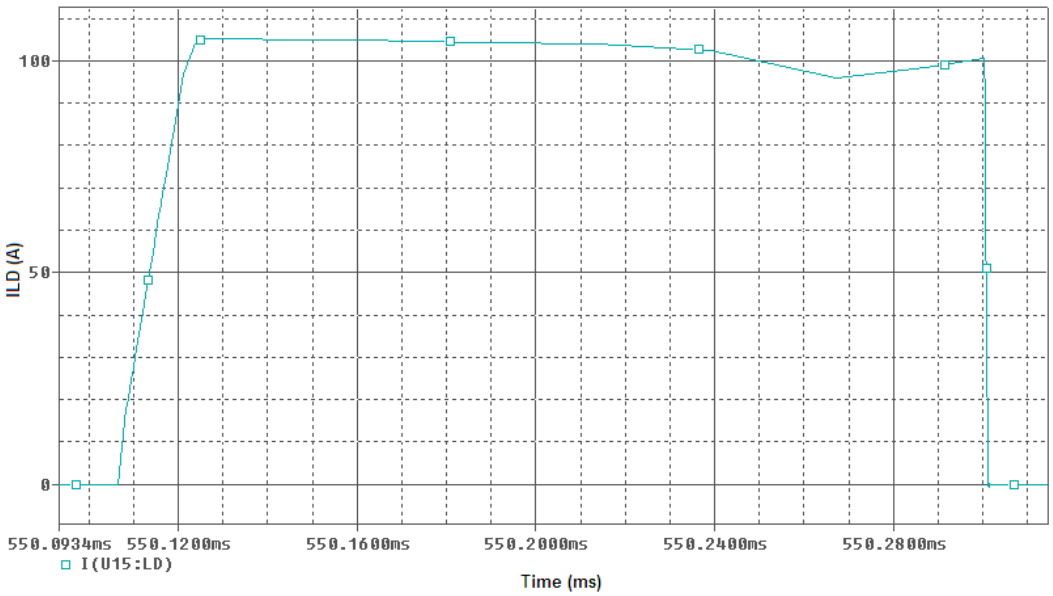


Figure 4-52. ORCAD simulation of the LD current with K_P=1.

4.3.3 Sensitivity Analysis with respect to the Integral Constant

The effect of the variation in the value of the resultant K_i due to tolerances in the values of the resistances on the steady-state response of the system was analysed in previous section. In this part, further increase and decrease in the value of the resultant K_i is analysed both using MATLAB on the developed closed loop sub-model for steady-state response of the system and the ORCAD simulations. Although the closed loop sub-model may not give precise results for the transient response of the system, it gives a general idea about the transient behaviour of the LD current.

In these analyses, the new values of K_i are determined as 1000000 and 1 to see further increase and decrease in its value.

4.3.3.1 Effect of the Increase in the Value of the Integral Constant

For K_i=1000000, the overall transfer function of the sub-model shown in Figure 3-28 becomes as:

$$H_1'(s) = \frac{247.5s+5.5e007}{8.425s+1.65e006}$$

Step responses of the actual and the new sub-model are shown in Figure 4-48 and Figure 4-53. The results show that the increase in the value of K_i has decreased the rise time of the LD current from 8.44µs to 0.856µs. However, since the switching behavior of the low side MOSFETs is not modeled in the corresponding sub-model, this analysis alone may not give an accurate result.

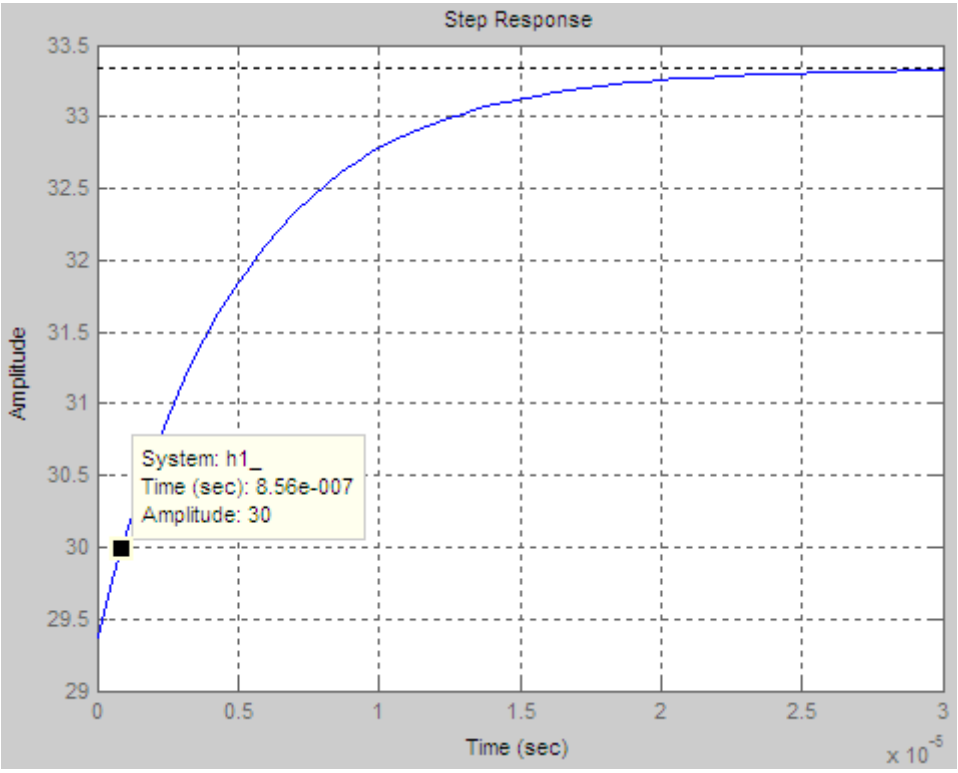


Figure 4-53. Step response of the new sub-model for K_i=1000000.

The more realistic analysis is made with the ORCAD simulations. Figure 4-54 shows the effect of the increase in the value of K_i on the transient behaviour of the LD current. The increase in the value of K_i has decreased the value of the rise time slightly. It is observed that the decrease in the rise time is limited to a value of 5μs because of the additional gate resistor. Furthermore, it has caused an increase in the settling time of the load current and an overshoot at the load current.

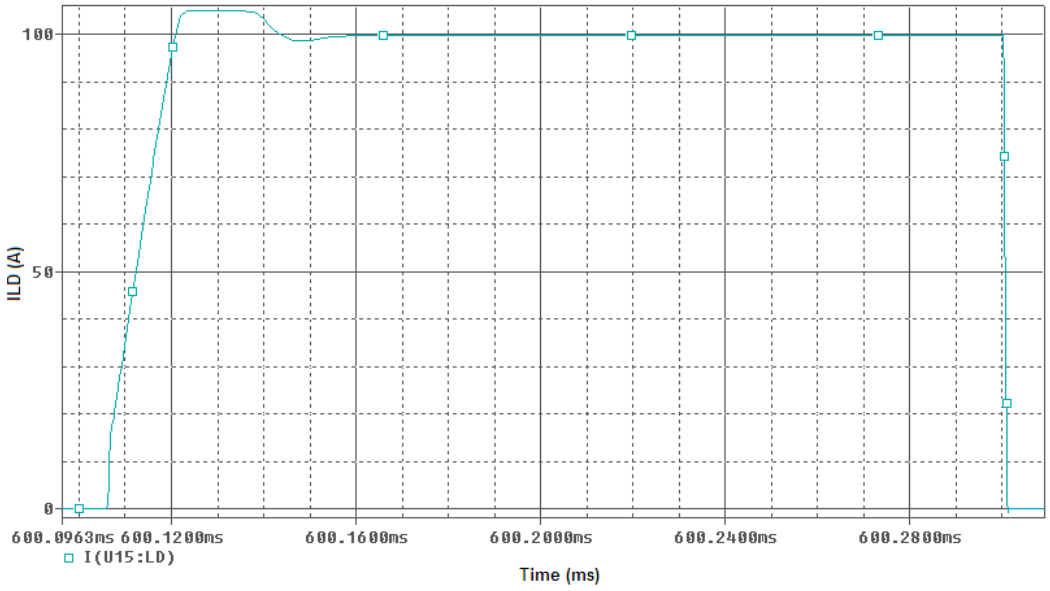


Figure 4-54. ORCAD simulation of the LD current with K_i=1000000.

4.3.3.2 Effect of the Decrease in the Value of the Integral Constant

For K_i=1, the overall transfer function of the sub-model shown in Figure 3-28 becomes as:

$$H_1''(s) = \frac{247.5s+55}{8.425s+1.65}$$

Step responses of the actual and the new sub-model are shown in Figure 4-48 and Figure 4-55. The results show that the decrease in the value of K_i has increased the

rise time of the LD current from 8.44µs to 0.868sec, which means that the load current cannot reach the desired value in 200µs pulse time period. However, since the switching behavior of the low side MOSFETs is not modeled in the corresponding sub-model, this analysis alone may not give an accurate idea result.

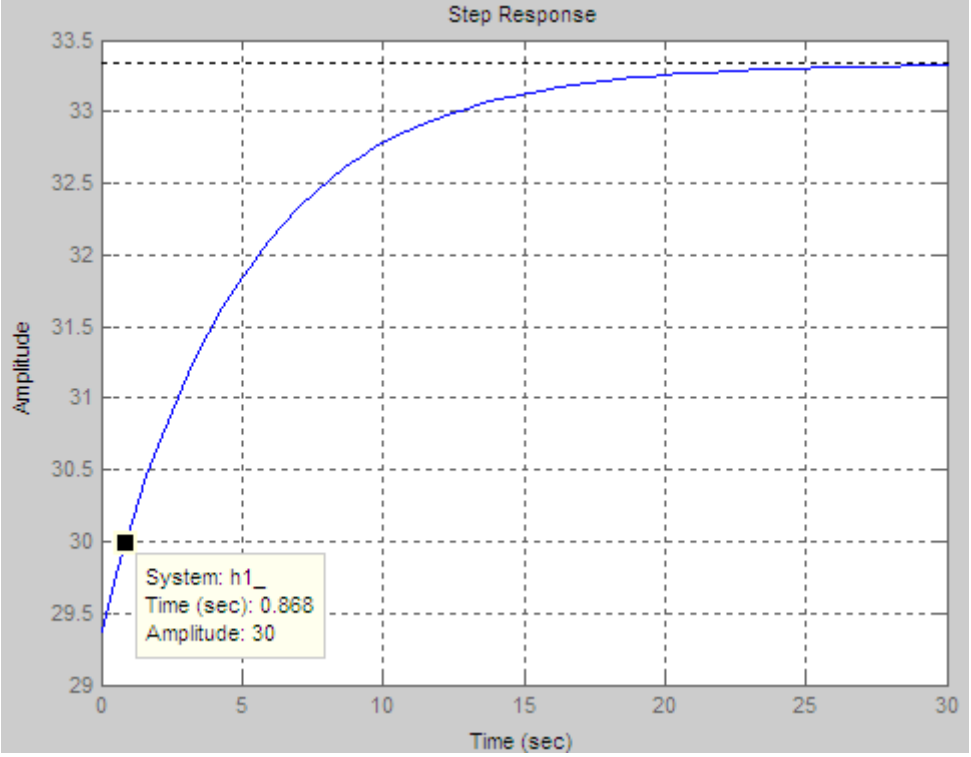


Figure 4-55. Step response of the new sub-model for K_i=1.

The more realistic analysis is made with the ORCAD simulations. Figure 4-56 shows the effect of the decrease in the value of K_i on the transient behaviour of the LD current. The decrease in the value of K_i has changed the settling point of the load current. It settles to 60A instead of 100A. This is an expected result, because the time period of 200µs is not enough for the load current to reach the desired value. In fact, the controller in the design can be considered as a P controller because K_i is negligibly small in this case. Therefore, it is observed that there is a considerable drift from the desired current value.

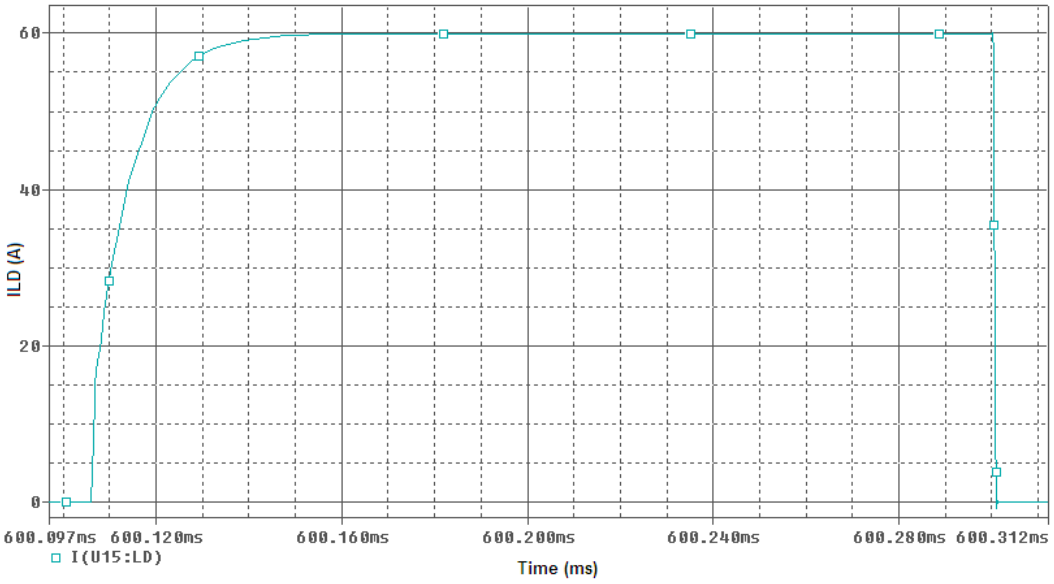


Figure 4-56. ORCAD simulation of the LD current with K_i=1.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

In this thesis, a fast and high power pulsed LD driver for laser range finder based on linear current source topology is simulated using ORCAD and MATLAB and the simulation results are compared and discussed with the actual experimental results.

The major contribution of this thesis is the PI controller that can be used to avoid the expected drift and noise problems that may be generated in case of using only a P controller [8] or a PID controller [9] for the non-linear loads.

The major works accomplished in the thesis are listed as follows:

- Protection of the LDs against surge current during input capacitor charging prior to firing is achieved.
- Protection of the LDs against overcurrent, short circuit current and overvoltage is achieved via software.
- Protection of the LDs against overcurrent is also achieved with an analog protection network which is an alternative precaution to digital protection in case of a failure in the software or the programmable IC physically.
- The driver is able to lock itself in protection mode, which means that it prevents the input capacitor charging and LD firing in case of a failure in

normal operating conditions although the necessary commands for capacitor charging and LD firing are still sent by the user, until it receives a reset signal.

- Protection of the external power supply during capacitor charging is provided via a soft starting network.
- The driver has a user interface for the determination of the properties of the load current.

The LD driver proposed in this thesis supplies current pulses up to 120A for two LD arrays, each of which consists of five LDs. The width and frequency of the current pulses are within the ranges of 200µs to 300µs and 20Hz to 40Hz, respectively.

MATLAB and ORCAD simulation results and actual experimental results are proved to be compatible. Experimental results show that rise and fall times of the current pulses meet the requirements of the driver.

The fast and high power pulsed laser diode driver realized in this thesis effectively reduced the current regulation to less than 1% and eliminated the transients sufficiently as expected. Furthermore, the overshoot and undershoot of the diode currents are diminished to a value less than 1% of steady-state value, consequences of which improved the load current regulation.

Sensitivity analysis of the sub-systems for steady-state closed loop model shows that the system is almost insensitive to the variations in the values of K_p, K_i and K_n due to tolerances in the values of the resistances and the MOSFET mismatches. However, even 0.133% change in the value of the total feedback gain causes 1.5A change in the LD current. However, that does not disturb the current regulation performance of the system and can be minimized by using more precise resistors in feedback stage of each closed loop system.

Sensitivity analysis of the system for transient response shows that the system is sensitive to large variations in the values of K_p and K_i. However, the changes in

the transient response of the system due to large variations in the values of K_p and K_i is not expected because the values of the resistances in the controller can only change due to their tolerances. Moreover, the additional gate resistance is very critical for the transient response of the closed loop system. If the value of the gate resistance is selected larger than enough, the rise time of the LD current becomes larger. On the other hand, if the value of the gate resistance is selected very small, small rise times can be achieved; however, overshoot and undershoots may be observed in the load current waveform, which is undesirable for the safe operation of the LDs.

The advantages of the LD driver proposed in the thesis when compared to the other topologies which exist in the literature are as follows:

- The proposed LD driver is directly supplied from a DC input. Therefore, there is no need for an isolation stage between input and control circuit and current amplification when compared to other topologies being fed from an AC source.
- The level, pulse frequency and pulse width of the LD current are determined by only one reference input in the control stage of the proposed method. Therefore, there is only one control loop for each LD array when compared to the solutions having multiple control loops.
- The current sense network done in the proposed method provides a feedback signal for both current control and the protection circuitries when compared to other solutions in which the current sense network is only used for current control.
- Current regulation is totally accomplished by the control circuit in the proposed method while it depends on the values of passive components in SMPS solutions.

5.2 Future Work

In the future, for a more dependable LD driver, functions of the "Laser Control Card" can be embedded into the LD driver so that the interaction of the user with the driver can directly be achieved and the LD driver can be able to provide the necessary supply voltages for the ICs. Moreover, the external power supply feeding the input capacitors can be embedded into the driver so that the driver can work independently. These improvements will also simplify test of the LD driver. However, these improvements will make the PCB design of the driver extremely difficult because both switching regulators and the LD current control sensitive to the noise will be implemented on a single board. This will bring the necessity of electromagnetic interference precaution in the driver.

In addition, an analog op-amp based PI controller is used in the driver. Instead of an analog controller, a digital controller technique can be tried. However, the difficulty is that the severe regulation and rise and fall times of the LD current. The digital controller must be fast enough in order to get a lot of samples from the LD current in order to get at least similar performance obtained from the analog controller. In fact, the main problem is the severe rise and fall time (10μs) of the system. During rise and fall periods, the digital controller has to obtain a lot of samples from the LD current in order to prevent the overshoots and oscillations. However, the microcontrollers manufactured nowadays are not fast enough to achieve this.

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