

THE DESIGN, CONTROL, AND PERFORMANCE ANALYSIS OF AC MOTOR
DRIVES WITH FRONT END DIODE RECTIFIER UTILIZING LOW
CAPACITANCE DC BUS CAPACITOR AND COMPARISON WITH
CONVENTIONAL DRIVES

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

VAHAP VOLKAN ABAN

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2012

Approval of the thesis:

**THE DESIGN, CONTROL, AND PERFORMANCE ANALYSIS OF AC
MOTOR DRIVES WITH FRONT END DIODE RECTIFIER UTILIZING
LOW CAPACITANCE DC BUS CAPACITOR AND COMPARISON WITH
CONVENTIONAL DRIVES**

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ABSTRACT

THE DESIGN, CONTROL, AND PERFORMANCE ANALYSIS OF AC MOTOR DRIVES WITH FRONT END DIODE RECTIFIER UTILIZING LOW CAPACITANCE DC BUS CAPACITOR AND COMPARISON WITH CONVENTIONAL DRIVES

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September 2012, 183 pages

In this thesis the design, control, stability, input power quality, and motor drive performance of ac motor drives with front end three phase diode rectifiers utilizing low capacitance dc bus capacitor are investigated. Detailed computer simulations of conventional motor drives with diode rectifier front end utilizing high capacitance dc bus capacitor and the drives with low capacitance dc bus capacitor are conducted and the performances are compared. Performance evaluation of various active control methods found in previous studies aiming to provide the dc bus stability of drives with low capacitance dc bus capacitor are done at various load levels and types. Design recommendations are provided for the drives utilizing low capacitance dc bus capacitor.

Keywords: Motor drive, diode rectifier, high capacitance, low capacitance, capacitor, input power quality, bus stability, active control.

ÖZ

DÜŞÜK SİĞALI DC BARA KONDANSATÖRLÜ DİYOTLU DOĞRULTUCU GİRİŞLİ AC MOTOR SÜRÜCÜLERİNİN TASARIMI, DENETİMİ, BAŞARIM ANALİZİ VE GELENEKSEL SÜRÜCÜLERLE KARŞILAŞTIRILMASI

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Tez Yöneticisi: Doç. Dr. Ahmet M. Hava

Eylül 2012, 183 sayfa

Bu tezde düşük sığalı dc bara kondansatörü bulunduran üç fazlı diyotlu doğrultucu girişli ac motor sürücülerinin tasarımı, denetimi, kararlılığı, şebeke güç kalitesi ve motor sürme başarımı incelenmiştir. DC barasında yüksek sığalı kondansatör bulunduran geleneksel diyotlu doğrultucu girişli sürücü devresi ile düşük sığalı kondansatörlü devrelerin ayrıntılı bilgisayar benzetimleri yapılmış ve başarımları karşılaştırılmıştır. Düşük sığalı kondansatörlü sürücülerde bara gerilim kararlılığını sağlamak için önceden yapılmış çalışmalarda bulunan çeşitli etkin kontrol yöntemlerinin çeşitli yük değeri ve tiplerindeki başarımları değerlendirilmiştir. Düşük sığalı bara kondansatörü bulunduran sürücüler için tasarım için önerileri verilmiştir.

Anahtar kelimeler: Motor sürücü, diyotlu doğrultucu, yüksek sığa, düşük sığa, kondansatör, şebeke güç kalitesi, bara kararlılığı, etkin denetim.

to my family

ACKNOWLEDGEMENTS

I express my sincerest thanks to my supervisor, Dr. Ahmet M. Hava, for his guidance, support, encouragement, and valuable contributions throughout my graduate education.

I would like to express my deepest gratitude to my family who has always supported me throughout my life. Their encouragement and invaluable love have made me stand upright.

I would like to thank my chief Şükrü Serkan Sevim and Meteksan Defence Industry Inc. for supporting me throughout my studies.

I would like to thank my colleague Ufuk Ayhan and all my friends for their help and support.

I wish to thank to the staff of Electrical and Electronics Engineering Department and Graduate School of Natural and Applied Sciences for their help throughout my graduate study.

TABLE OF CONTENTS

ABSTRACT.....	iv
ÖZ.....	v
ACKNOWLEDGEMENTS.....	vii
TABLE OF CONTENTS.....	viii
LIST OF FIGURES.....	xiv
LIST OF TABLES.....	xxxiv

CHAPTERS

1. INTRODUCTION.....	1
1.1 Overview of AC Motor Drives.....	1
1.2 AC Motor Drive Topologies.....	1
1.2.1 AC-AC Converters.....	2
1.2.1.1 Matrix Converter.....	2
1.2.2 AC-DC-AC Converters.....	3
1.2.2.1 PWM Transistor Rectifier Cascaded with PWM Inverter.....	3
1.2.2.2 Diode Rectifier Cascaded with PWM Inverter.....	4
1.2.2.2.1 Diode Rectifier Utilizing High Capacitance Electrolytic Capacitor.....	4
1.2.2.2.2 Diode Rectifier Utilizing Low Capacitance Film Capacitor.....	5
1.3 AC Motor Drive Performance Criteria.....	6
1.3.1 Input Power Quality.....	6
1.3.1.1 Line Current Distortion.....	6
1.3.1.2 Input Power Factor.....	7
1.3.2 Motor Motion Quality.....	8
1.3.3 System Reliability, Size, and Cost.....	9
1.4 Scope of the Thesis.....	10

2. LOAD TYPES AND THREE-PHASE AC MACHINE CONTROL METHODS.....	12
2.1 Electric Motor Load Types	12
2.1.1 Constant Torque Load.....	12
2.1.2 Constant Power Load.....	13
2.1.3 Variable Torque Load.....	13
2.2 Electrical Interpretation of Load Mechanical Characteristics	14
2.2.1 Negative and Positive Impedance Effect	15
2.3 Three-Phase AC Machine Control Methods	16
2.3.1 Constant V/f Control.....	16
2.3.2 Vector Control (Field Oriented Control)	16
2.3.2.1 Three-phase to Two-phase Transformation of Motor Quantities.....	17
2.3.2.2 Principle of Vector Control.....	20
2.4 Vector Control of Induction Machine	21
2.4.1 Induction Machine Principle of Operation.....	21
2.4.2 Steady State Equivalent Circuit and Equations of Induction Machine	22
2.4.3 Dynamic Modeling of Induction Machine.....	26
2.4.4 Two-phase Model of the Induction Machine	26
2.4.5 Synchronous Reference Frame Model of Induction Machine	27
2.4.6 Indirect Vector Control Method for Induction Machine.....	29
2.4.7 Speed Controller Design	31
2.4.7.1 Synchronous Frame Current Regulator Design	35
2.4.7.2 Speed Regulator Design	37
2.5 Conclusion.....	38
3. CONVENTIONAL DIODE RECTIFIER FRONT END MOTOR DRIVE SYSTEM REVIEW.....	39
3.1 Three-phase Diode Rectifiers.....	39
3.1.1 Ideal Three-phase Diode Rectifier	39
3.1.1.1 Principle of Operation.....	40
3.1.1.2 DC Bus Voltage Characteristics.....	40
3.1.1.3 Input Power Quality Characteristics	42
3.1.1.3.1 Line Current Distortion	42

3.1.1.3.2	Input Power Factor	44
3.1.2	Practical Three-phase Diode Rectifiers.....	44
3.1.2.1	Components Used in Practical Diode Rectifiers	45
3.1.2.1.1	DC Bus Capacitor	45
3.1.2.1.2	Filter Inductor.....	50
3.1.2.1.3	Precharge Circuit.....	51
3.1.2.2	Performance Analysis of Practical Three Phase Diode Rectifiers	54
3.1.2.2.1	Input Power Quality	55
3.1.2.2.1.1	Line Current Quality	55
3.1.2.2.1.2	Input Power Factor	57
3.1.2.2.2	DC Bus Voltage Quality	58
3.2	PWM Voltage Source Inverter	60
3.2.1	Principle of Operation.....	60
3.2.2	Zero Sequence Signal Injection	62
3.2.3	Commonly Used PWM Methods and Their Scalar Implementation	62
3.2.3.1	Sinusoidal PWM (SPWM).....	62
3.2.3.2	Space Vector PWM (SVPWM)	63
3.2.3.3	Discontinuous PWM (DPWM1)	63
3.3	Drive System.....	63
3.3.1	DC Bus Voltage Characterization of Rectifier-PWM Inverter Drive	64
3.3.2	DC Bus Disturbance Rejection and Its Effect On the DC Bus Voltage Stability	64
3.4	Conclusion.....	65
4.	INDUCTION MOTOR DRIVE WITH FRONT END DIODE RECTIFIER UTILIZING HIGH CAPACITANCE DC BUS CAPACITOR.....	66
4.1	Design of Circuit and Controller	66
4.2	Constant Torque Load Operation Simulation Results.....	68
4.2.1	2.2 kW Motor Drive Constant Torque Load Operation without DC Bus Disturbance Rejection.....	68
4.2.2	2.2 kW Motor Drive Constant Torque Load Operation with DC Bus Disturbance Rejection.....	74

4.2.3	37 kW Motor Drive Constant Torque Load Operation without DC Bus Disturbance Rejection.....	75
4.2.4	37 kW Motor Drive Constant Torque Load Operation with DC Bus Disturbance Rejection	79
4.3	Fan Load Operation Simulation Results	79
4.3.1	2.2 kW Motor Drive Fan Load Operation without DC Bus Disturbance Rejection	79
4.3.2	2.2 kW Motor Drive Fan Load Operation with DC Bus Disturbance Rejection	83
4.3.3	37 kW Motor Drive Fan Load Operation without DC Bus Disturbance Rejection	83
4.3.4	37 kW Motor Drive Fan Load Operation with DC Bus Disturbance Rejection	86
4.4	Constant Power Load Simulation Results	86
4.5	Conclusion.....	89
5.	INDUCTION MOTOR DRIVE WITH FRONT END DIODE RECTIFIER UTILIZING LOW CAPACITANCE DC BUS CAPACITOR	90
5.1	Using Low C_{dc} Film Capacitor Instead of High C_{dc} Electrolytic Capacitor	90
5.2	Stability Analysis Using Equivalent Rectifier Model	91
5.3	Design of Low C_{dc} Motor Drive without DC Link Inductor	97
5.4	Simulation Results of the Low C_{dc} Motor Drives without DC Link Inductor.....	98
5.4.1	Constant Torque Load Operation Simulation Results	100
5.4.1.1	2.2 kW Motor Drive Constant Torque Load Operation without DC Bus Disturbance Rejection	100
5.4.1.2	2.2 kW Motor Drive Constant Torque Load Operation with DC Bus Disturbance Rejection	109
5.4.1.3	37 kW Motor Drive Constant Torque Load Operation without DC Bus Disturbance Rejection	115
5.4.1.4	37 kW Motor Drive Constant Torque Load Operation with DC Bus Disturbance Rejection	118
5.4.2	Fan Load Operation Simulation Results	120
5.4.2.1	2.2 kW Motor Drive Fan Load Operation without DC Bus Disturbance Rejection	121

5.4.2.2	2.2 kW Motor Drive Fan Load Operation with DC Bus Disturbance Rejection	124
5.4.2.3	37 kW Motor Drive Fan Load Operation without DC Bus Disturbance Rejection	127
5.4.2.4	37 kW Motor Drive Fan Load Operation with DC Bus Disturbance Rejection	130
5.5	Design of Low C_{dc} Motor Drive with DC Link Inductor	132
5.6	Simulation Results of the Drives with DC Link Inductor	134
5.6.2	Constant Torque Load Operation Simulation Results	134
5.6.2.1	2.2 kW Motor Drive Constant Torque Load Operation without DC Bus Disturbance Rejection	134
5.6.2.2	37 kW Motor Drive Constant Torque Load Operation without DC Bus Disturbance Rejection	136
5.7	Active DC Link Stabilization Methods	138
5.7.1	Voltage Mode Stabilization Methods	139
5.7.1.1	Method 1 [35].....	139
5.7.1.2	Method 2 [36].....	141
5.7.2	Current Mode Stabilization Methods	142
5.7.2.1	Method 3 [33].....	142
5.8	Simulation Results with Active Stabilization Methods.....	147
5.8.1	2.2 kW Motor Drive Constant Torque Load Operation Simulation Results....	147
5.8.2	37 kW Motor Drive Constant Torque Load Operation Simulation Results....	151
5.8.3	2.2 kW Motor Drive Fan Load Operation Simulation Results	154
5.8.4	37 kW Motor Drive Fan Load Operation Simulation Results	158
5.9	Conclusion.....	161
6.	PERFORMANCE EVALUATION AND COMPARISON OF CONVENTIONAL AC MOTOR DRIVES AND DRIVES UTILIZING LOW CAPACITANCE DC BUS CAPACITOR.....	162
6.1	Introduction.....	162
6.2	Performance Evaluation of Conventional Motor Drives.....	162
6.3	Performance Evaluation of Low C_{dc} Motor Drives.....	165

6.4 Comparison of Conventional Motor Drives and Low C_{dc} Motor Drives	174
6.4.1 Comparison In Terms of DC Bus Voltage Quality and Stability.....	174
6.4.2 Comparison In Terms of Input Power Quality.....	174
6.4.3 Comparison In Terms of Motor Motion Quality.....	175
7. CONCLUSION AND FUTURE WORK	176
REFERENCES	180

LIST OF FIGURES

FIGURES

Figure 1.1 AC motor drive circuit topologies.	1
Figure 1.2 Matrix converter.	2
Figure 1.3 PWM transistor rectifier cascaded with PWM inverter.....	3
Figure 1.4 Diode rectifier cascaded with PWM inverter.	4
Figure 2.1 (a) Constant torque load torque-speed characteristics, (b) power-speed characteristics.	12
Figure 2.2 (a) Constant power load torque-speed characteristics, (b) power-speed characteristics.	13
Figure 2.3 Variable torque load torque-speed (black) and power-speed (blue) characteristics (a) Torque varying linearly with speed (b) Torque varying with square of the speed.	14
Figure 2.4 Space vector representations of three-phase machine currents.	18
Figure 2.5 Two-phase stationary frame components of three-phase stator currents.	19
Figure 2.6 Synchronous reference frame d and q axis current space vectors.	20
Figure 2.7 Per phase equivalent circuit of the induction machine.	22
Figure 2.8 Modified per phase equivalent circuit of the induction machine.	23

Figure 2.9 Per phase equivalent circuit of induction machine with rotor at stator frequency.	24
Figure 2.10 Induction machine block diagram.	33
Figure 2.11 Induction machine modified block diagram.	34
Figure 2.12 Speed controller block diagram for the induction machine.	34
Figure 2.13 Schematic for the use of synchronous frame current regulator in indirect vector control.	36
Figure 2.14 Speed regulator of the induction machine.	37
Figure 2.15 Speed regulator with rate of change limiter and anti wind-up controller.	38
Figure 3.1 Three-phase diode rectifier circuit.	39
Figure 3.2 DC bus voltage of the 2.2 kW ideal three phase diode rectifier fed by 220 V (l-n)/50 Hz ac grid (16.6 V/div, 2.5 ms/div).	40
Figure 3.3 Harmonic spectrum of the three phase diode rectifier dc bus voltage (5 V/div, 200 Hz/div).	41
Figure 3.4 Line current of the 2.2 kW ideal three-phase diode rectifier (1.67 A/div, 2.5 ms/div).	43
Figure 3.5 Line current harmonic spectrum of the 2.2 kW ideal three-phase diode rectifier (0.5 A/div, 50 Hz/div).	43
Figure 3.6 Line to neutral ac mains voltage (red, 125 V/div, 2.5 ms/div) and 20*line current (blue, 125 A/div, 2.5 ms/div) of the 2.2 kW ideal three-phase diode rectifier.	44

Figure 3.7 Practical three phase diode rectifier with line impedance, ac and dc filter inductors, precharge circuit, and dc bus capacitor.	45
Figure 3.8 Equivalent circuit of the electrolytic capacitor.	46
Figure 3.9 Variation of ESR with operating temperature and frequency for a typical electrolytic capacitor [19].....	47
Figure 3.10 Ratings of typical electrolytic capacitors taken from the manufacturer datasheet [21].	47
Figure 3.11 Variation of capacitance with operating temperature and frequency for a typical electrolytic capacitor [19].	48
Figure 3.12 Ratings of a typical film capacitor taken from the manufacturer datasheet [23].	49
Figure 3.13 (a) Inrush currents (167 A/div, 0.5 ms/div) phase-a (red), phase-b (blue), phase-c (green), (b) capacitor voltage (167 V/div, 0.5 ms/div) of 2.2 kW three phase rectifier with 0.4 mF dc link capacitor.	51
Figure 3.14 Precharge circuit with current limiter resistor and control switch.....	52
Figure 3.15 (a) Inrush currents phase-a (red), phase-b (blue), phase-c (green) (16.7 A/div, 25 ms/div), (b) capacitor voltage (100 V/div, 25 ms/div) of 2.2 kW three phase diode rectifier with 0.4 mF dc link capacitor utilizing inrush current limiter.	53
Figure 3.16 (a) Switch current (blue) (5 A/div, 25 ms/div), (b) current limiter resistor current (black) (0.5 A/div, 25 ms/div).	54
Figure 3.17 Line current of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor and no inductor filter (20 A/div, 2.5 ms/div).	56

Figure 3.18 Line current harmonic spectrum of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor and no inductor filter (0.5 A/div, 50 Hz/div).	56
Figure 3.19 Line current of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor, 4% ac line reactor and 4% dc link inductor (5 A/div, 2.5 ms/div).	57
Figure 3.20 Line current harmonic spectrum of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor, 4% ac line reactor and 4% dc link inductor (0.5 A/div, 50 Hz/div).	57
Figure 3.21 DC bus voltage of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor and without filter inductors (5 V/div, 2.5 ms/div).	58
Figure 3.22 DC bus voltage harmonic spectrum of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor and without filter inductors (1.67 V/div, 125 Hz/div).	58
Figure 3.23 DC bus voltage of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor, 4 % ac line reactor and 4% dc link inductor (3.3 V/div, 2.5 ms/div).	59
Figure 3.24 DC bus voltage harmonic spectrum of the 2.2 kW three-phase diode rectifier equipped with 0.4 mF capacitor, 4 % ac line reactor and 4 % dc link inductor (0.33 V/div, 125 Hz/div).	59
Figure 3.25 Three-phase voltage source inverter.	60
Figure 3.26 Scalar implementation of PWM; with modulation wave v_a^* for a phase, triangle carrier v_{tri} , switch states for S_{a+} , and output voltage v_{ao} [27].	61
Figure 3.27 Voltage space vectors of three-phase two-level inverter [27].	61

Figure 3.28 AC motor drive circuit with front end diode rectifier.....	63
Figure 4.1 2.2 kW constant torque load drive without dc bus disturbance rejection (a) speed (250 rpm/div, 0.5 s/div), (b) d axis current (black) and q axis current (blue) (1.67 A/div, 0.5 s/div), (c) motor torque (2.5 N.m/div, 0.5 s/div).....	69
Figure 4.2 DC bus voltage of 2.2 kW constant torque load drive without dc bus disturbance rejection (1 V/div, 2 ms/div).....	70
Figure 4.3 Harmonic spectrum of dc bus voltage for 2.2 kW constant torque load drive without dc bus disturbance rejection (0.2 V/div, 2.5 kHz/div)..	70
Figure 4.4 Reference voltages in stationary α - β frame against theta (left) and corresponding voltage circle constructed by α vs β plot for 0-360° cycle..	71
Figure 4.5 The decomposition of dc bus voltage along α - β axes and construction of inverter output voltage limit circle.	72
Figure 4.6 The reference voltage circle (red) and inverter output voltage limit circle (blue).	72
Figure 4.7 Motor steady state torque of 2.2 kW constant torque load drive without dc bus disturbance rejection (0.33 N.m/div, 2 ms/div).	73
Figure 4.8 The line current waveform of 2.2 kW constant torque load drive without dc bus disturbance rejection (3.33 A/div, 2 ms/div).	74
Figure 4.9 Harmonic spectrum of line current of 2.2 kW constant torque load drive without dc bus disturbance rejection (1 A/div, 50 Hz/div).	74

Figure 4.10 37 kW constant torque load drive without dc bus disturbance rejection (a) speed (250 rpm/div, 1.25 s/div), (b) d axis current (black) and q axis current (blue) (20 A/div, 1.25 s/div), (c) motor torque (50 N.m/div, 1.25 s/div).....	75
Figure 4.11 DC bus voltage of 37 kW constant torque load drive without dc bus disturbance rejection (1.25 V/div, 2 ms/div).....	76
Figure 4.12 Inverter voltage reference (red) and inverter output voltage limit circle (blue) of 37 kW constant torque load drive without dc bus disturbance rejection (100 V/div, 100 V/div).....	76
Figure 4.13 Harmonic spectrum of dc bus voltage for 37 kW constant torque load drive without dc bus disturbance rejection (0.2 V/div, 2.5 kHz/div).....	77
Figure 4.14 Motor steady state torque of 37 kW constant torque load drive without dc bus disturbance rejection (3.3 N.m/div, 2 ms/div).	77
Figure 4.15 The line current waveform of 37 kW constant torque load drive without dc bus disturbance rejection (33.3 A/div, 2 ms/div).	78
Figure 4.16 Harmonic spectrum of line current for 37 kW constant torque load drive without dc bus disturbance rejection (10 A/div, 50 Hz/div).	78
Figure 4.17 2.2 kW fan load drive without dc bus disturbance rejection (a) speed (250 rpm/div, 0.5 s/div), (b) d axis current (black) and q axis current (blue) (1.67 A/div, 0.5 s/div), (c) motor torque (2.5 N.m/div, 0.5 s/div)	80
Figure 4.18 Motor steady state torque of 2.2 kW fan load drive without dc bus disturbance rejection (0.33 N.m/div, 2 ms/div).....	81
Figure 4.19 DC bus voltage of 2.2 kW fan load drive without dc bus disturbance rejection (1 V/div, 2 ms/div).	81

Figure 4.20 Harmonic spectrum of dc bus voltage for 2.2 kW fan load drive without dc bus disturbance rejection (0.2 V/div, 2.5 kHz/div).....	82
Figure 4.21 The line current waveform of 2.2 kW fan load drive without dc bus disturbance rejection (3.33 A/div, 2 ms/div).....	82
Figure 4.22 Harmonic spectrum of line current for 2.2 kW fan load drive without dc bus disturbance rejection (1 A/div, 50 Hz/div).	83
Figure 4.23 DC bus voltage of 37 kW fan load drive without dc bus disturbance rejection (1.25 V/div, 2 ms/div).	84
Figure 4.24 Harmonic spectrum of dc bus voltage of 37 kW fan load drive without dc bus disturbance rejection (0.2 V/div, 100 Hz/div).....	84
Figure 4.25 Motor steady state torque of 37 kW fan load drive without dc bus disturbance rejection (3.3 N.m/div, 2 ms/div).....	85
Figure 4.26 Line current waveform of 37 kW fan load drive without dc bus disturbance rejection (33.3 A/div, 2 ms/div).....	85
Figure 4.27 Harmonic spectrum of line current of 37 kW fan load drive without dc bus disturbance rejection (10 A/div, 50 Hz/div).	86
Figure 4.28 DC bus voltage of the 2.2 kW motor drive under constant power load (16.7 V/div, 5 ms/div).	87
Figure 4.29 Line current of the 2.2 kW motor drive under constant power load (3.33 A /div, 5 ms/div).....	87
Figure 4.30 DC bus voltage of the 37 kW motor drive under constant power load (16.7 V/div, 5 ms/div).	88

Figure 4.31 Line current of the 37 kW motor drive under constant power load (33.3 A /div, 5 ms/div).....	88
Figure 5.1 Equivalent circuit of three phase diode rectifier.....	91
Figure 5.2 Equivalent rectifier model simulation results at dc bus ripple harmonic frequencies $P_{out}=2.2$ kW, $f_n=1.25$ kHz DC bus ripple voltage (red, 5V/div, 500 Hz/div), input current (blue, 5A /div, 500 Hz/div), input impedance (black, 5 ohm/div, 500 Hz/div).	93
Figure 5.3 Equivalent rectifier model simulation results at dc bus ripple harmonic frequencies $P_{out}=2.2$ kW, $f_n=2.5$ kHz DC bus ripple voltage (red, 10 V/div, 500 Hz/div), input current (blue, 10A /div, 500 Hz/div), input impedance (black, 10 ohm/div, 500 Hz/div).	94
Figure 5.4 Equivalent rectifier model simulation results at dc bus ripple harmonic frequencies $P_{out}=37$ kW, $f_n=1.576$ kHz DC bus ripple voltage (red, 5 V/div, 500 Hz/div), input current (blue, 5 A /div, 500 Hz/div), input impedance (black, 5 ohm/div, 500 Hz/div).	95
Figure 5.5 Equivalent rectifier model simulation results at dc bus ripple harmonic frequencies $P_{out}=37$ kW, $f_n=3.4$ kHz DC bus ripple voltage (red, 5 V/div, 500 Hz/div), input current (blue, 5 A /div, 500 Hz/div), input impedance (black, 5 ohm/div, 500 Hz/div).	95
Figure 5.6 DC bus voltage of the 2.2 kW low C_{dc} motor drive operating under constant power load (50 V/div, 5 ms/div).....	98
Figure 5.7 Line current of the 2.2 kW low C_{dc} motor drive operating under constant power load (3.33 A /div, 5 ms/div).	99

Figure 5.8 DC bus voltage of the 37 kW low C_{dc} motor drive operating under constant power load (50 V/div, 5 ms/div).	99
Figure 5.9 Line current of the 37 kW low C_{dc} motor drive operating under constant power load (50 A /div, 5 ms/div).	100
Figure 5.10 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor, without dc bus disturbance rejection (a) speed (250 rpm/div, 0.5 s/div), (b) d axis current (black) and q axis current (blue) (1.67 A/div, 0.5 s/div), (c) motor torque (2.5 N.m/div, 0.5 s/div).	101
Figure 5.11 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (50 V/div, 5 ms/div).	102
Figure 5.12 Harmonic spectrum of dc bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (5 V/div, 500 Hz/div).	102
Figure 5.13 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive operating at 1400 rpm 13 N.m without dc bus disturbance rejection (100 V/div, 100 V/div).	103
Figure 5.14 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive operating at 1000 rpm 13 N.m without dc bus disturbance rejection (100 V/div, 100 V/div).	104
Figure 5.15 DC bus voltage (red) and V_{qs}^e (black) of 2.2 kW low C_{dc} motor drive $f_{rc}=1$ kHz (100 V/div, 5 ms/div).	104

Figure 5.16 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection $f_{rc}= 1$ kHz (0.33 N.m/div, 5 ms/div).	105
Figure 5.17 The line current waveform of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (5 A/div, 5 ms/div).....	105
Figure 5.18 Harmonic spectrum of line current of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (1 A/div, 500 Hz/div).....	106
Figure 5.19 DC bus voltage (red) and V_{qs}^e (black) of 2.2 kW low C_{dc} motor drive operating under constant torque load without disturbance rejection for $f_{rc}=100$ Hz (100 V/div, 5 ms/div).....	107
Figure 5.20 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection for $f_{rc}=100$ Hz (0.33 N.m/div, 5 ms/div).....	107
Figure 5.21 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load with constant V/f method without dc bus disturbance rejection (50 V/div, 3.3 ms/div).	108
Figure 5.22 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load with constant V/f method without dc bus disturbance rejection (1 N.m/div, 3.3 ms/div).....	108
Figure 5.23 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (50 V/div, 5 ms/div).	109

Figure 5.24 Harmonic spectrum of dc bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (5 V/div, 500 Hz/div).....	109
Figure 5.25 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive operating at 1400 rpm 13 N.m with dc bus disturbance rejection (100 V/div, 100 V/div).	110
Figure 5.26 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive operating at 1550 rpm 13 N.m with dc bus disturbance rejection (100 V/div, 100 V/div).	111
Figure 5.27 DC bus voltage (red) and V_{qs}^e (black) of 2.2 kW low C_{dc} motor drive operating under constant torque load with disturbance rejection $f_{rc}=1$ kHz (100 V/div, 5 ms/div).	111
Figure 5.28 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (0.33 N.m/div, 5 ms/div).	112
Figure 5.29 The line current waveform of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (5 A/div, 5 ms/div).	112
Figure 5.30 Harmonic spectrum of line current of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (1 A/div, 500 Hz/div).....	113
Figure 5.31 DC bus voltage (red) and V_{qs}^e (black) of 2.2 kW low C_{dc} motor drive operating under constant torque load with disturbance rejection $f_{rc}=100$ Hz (100 V/div, 5 ms/div).	113

Figure 5.32 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection $f_{rc}=100$ Hz (0.33 N.m/div, 5 ms/div).....	114
Figure 5.33 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load with constant V/f method with dc bus disturbance rejection (50 V/div, 3.3 ms /div).	114
Figure 5.34 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load with constant V/f method with dc bus disturbance rejection (0.5 N.m/div, 3.3 ms/div).....	115
Figure 5.35 DC bus voltage of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (50V/div, 3.3 ms/div).	116
Figure 5.36 Harmonic spectrum of dc bus voltage of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (5 V/div, 500 Hz/div).....	116
Figure 5.37 Motor steady state torque of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (3.3 N.m/div, 3.3 ms/div).....	117
Figure 5.38 The line current waveform of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (50 A/div, 3.3 ms/div).....	117
Figure 5.39 Harmonic spectrum of line current of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (10 A/div, 500 Hz/div).....	118

Figure 5.40 DC bus voltage of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (50 V/div, 3.3 ms/div).....	118
Figure 5.41 Harmonic spectrum of dc bus voltage of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (5 V/div, 333 Hz/div).....	119
Figure 5.42 Motor steady state torque of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (3.3 N.m/div, 3.3 ms/div).	119
Figure 5.43 The line current waveform of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (50 A/div, 3.3 ms/div).	120
Figure 5.44 Harmonic spectrum of line current of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (10 A/div, 333 Hz/div).....	120
Figure 5.45 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (a) speed (250 rpm/div, 0.5 s/div), (b) d axis current (black) and q axis current (blue) (1.67 A/div, 0.5 s/div), (c) internal torque (2.5 N.m/div, 0.5 s/div).	121
Figure 5.46 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (50 V/div, 5 ms/div).....	122
Figure 5.47 Harmonic spectrum of dc bus voltage of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (5 V/div, 500 Hz/div).	122

Figure 5.48 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (0.33 N.m/div, 5 ms/div).	123
Figure 5.49 The line current waveform of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (5 A/div, 5 ms/div).	123
Figure 5.50 Harmonic spectrum of line current of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (0.5 A/div, 500 Hz/div).	124
Figure 5.52 Harmonic spectrum of dc bus voltage of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (5 V/div, 500 Hz/div).	125
Figure 5.53 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (0.33 N.m/div, 5 ms/div).	125
Figure 5.54 The line current waveform of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (5 A/div, 5 ms/div).....	126
Figure 5.55 Harmonic spectrum of line current of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (0.5 A/div, 500 Hz/div).	126
Figure 5.56 37 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (a) speed (250 rpm/div, 1 s/div), (b) d axis current (black) and q axis current (blue) (16.67 A/div, 1 s/div), (c) motor torque (50 N.m/div, 1 s/div).....	127

Figure 5.57 DC bus voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (50 V/div, 3.3 ms/div).....	128
Figure 5.58 Harmonic spectrum of dc bus voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (5 V/div, 500 Hz/div).	128
Figure 5.59 Motor steady state torque of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (5 N.m/div, 3.3 ms/div).	129
Figure 5.60 The line current waveform of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (50 A/div, 3.3 ms/div).	129
Figure 5.61 Harmonic spectrum of line current of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (5 A/div, 500 Hz/div).	130
Figure 5.62 DC bus voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (50 V/div, 3.3 ms/div).....	130
Figure 5.63 Harmonic spectrum of dc bus voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (5 V/div, 500 Hz/div).	131
Figure 5.64 Motor steady state torque at set speed voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (3.3 N.m/div, 3.3 ms/div).....	131

Figure 5.65 The line current waveform voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (50 A/div, 3.3 ms/div).	132
Figure 5.66 Harmonic spectrum of line current voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (5 A/div, 500 Hz/div).....	132
Figure 5.67 Root locus of the characteristic equation (5.9) of the equivalent rectifier-inverter circuit (blue 15 kW, red 37 kW load power).	133
Figure 5.68 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc bus disturbance rejection and with dc link inductor (50 V/div, 5 ms/div).....	134
Figure 5.69 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive with dc link inductor without dc bus disturbance rejection (100 V/div, 100 V/div).....	135
Figure 5.70 Steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc bus disturbance rejection and with dc link inductor (0.33 N.m/div, 5 ms/div).....	135
Figure 5.71 Line current waveform of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc bus disturbance rejection and with dc link inductor (5 A/div, 5 ms/div).....	136
Figure 5.72 DC bus voltage of 37 kW low C_{dc} motor drive operating under constant torque load without dc bus disturbance rejection and with dc link inductor (50 V/div, 3.3 ms/div).	136

Figure 5.73 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 37 kW low C_{dc} motor drive operating under constant torque load with dc link inductor without dc bus disturbance rejection (100 V/div, 100 V/div).	137
Figure 5.74 Steady state torque of 37 kW low C_{dc} motor drive operating under constant torque load without dc bus disturbance rejection and with dc link inductor (3.33 N.m/div, 3.3 ms/div).....	137
Figure 5.75 Line current waveform of 37 kW low C_{dc} motor drive operating under constant torque load without dc bus disturbance rejection and with dc link inductor (50 A/div, 3.3 ms/div).....	138
Figure 5.76 Equivalent rectifier circuit of actively stabilized system including virtual damping resistor.....	139
Figure 5.77 Resonant component of dc bus voltage (blue) and 180° shifted version (red).	140
Figure 5.78 Schematic of implementation of active stabilization Method 1.	141
Figure 5.79 Schematic of implementation of active stabilization Method 2.	142
Figure 5.80 Root locus of characteristic equation (5.21) for various g_0 values (black: $g_0=0.2598$, blue: $g_0=0.1694$, red: $g_0=0.0791$).....	144
Figure 5.81 Root locus of characteristic equation (5.21) for various operating powers (black: $V_q=V_{dc}/2$, blue: $V_q=V_{dc}/4$).....	145
Figure 5.82 Schematic of implementation of active stabilization Method 3.	146

Figure 5.83 DC bus voltage waveforms for 2.2 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (50 V/div, 5 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3..... 147

Figure 5.84 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (100 V/div, 100 V/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3..... 148

Figure 5.85 Motor torque waveforms of 2.2 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (0.33 N.m V/div, 5 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3 (1 N.m/div, 5 ms/div). 149

Figure 5.86 Line current waveforms of 2.2 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (5 A/div, 5 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3 (3.33 A/div, 5 ms/div).... 150

Figure 5.87 DC bus voltage waveforms of 37 kW low C_{dc} motor drive operating under constant torque load with dc link inductor, all (50 V/div, 3.3 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3..... 151

Figure 5.88 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 37 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (100 V/div, 100 V/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3..... 152

Figure 5.89 Motor torque waveforms of 37 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (3.33 N.m/div, 3.3 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3 (10 N.m/div, 3.3 ms/div). 153

Figure 5.90 Line current waveforms of 37 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (50 A/div, 3.3 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3. 154

Figure 5.91 DC bus voltage waveforms of 2.2 kW low C_{dc} motor drive operating under fan load with dc link inductor (50 V/div, 5 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3..... 155

Figure 5.92 Motor torque waveforms of 2.2 kW low C_{dc} motor drive operating under fan load with dc link inductor (0.33 N.m V/div, 5 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3 (1 N.m/div, 5 ms/div). ... 156

Figure 5.93 Line current waveforms of 2.2 kW low C_{dc} motor drive operating under fan load with dc link inductor (3.33 A/div, 5 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3..... 157

Figure 5.94 DC bus voltage waveforms of 37 kW low C_{dc} motor drive operating under fan load with dc link inductor (50 V/div, 3.3 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3. 158

Figure 5.95 Motor torque waveforms of 37 kW low C_{dc} motor drive operating under fan load with dc link inductor (5 N.m/div, 3.3 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3. 159

Figure 5.96 Line current waveforms of 37 kW low C_{dc} motor drive operating under fan load with dc link inductor (33.3 A/div, 3.3 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3. 160

Figure 6.1 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (100 V/div, 100 V/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3. 169

Figure 6.2 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 37 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (100 V/div, 100 V/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3. 170

LIST OF TABLES

TABLES

Table 3.1 Basic characteristics of electrolytic and film capacitors.....	50
Table 4.1 Circuit parameters of the conventional motor drives.....	66
Table 4.2 The parameters of the induction motors used in simulations [31].....	67
Table 4.3 Controller parameters of the conventional motor drives.	67
Table 5.1 Circuit parameters of the low C_{dc} motor drives without dc link inductor.	97
Table 5.2 Controller parameters of the low C_{dc} motor drives without dc link inductor.....	98
Table 5.3 Circuit parameters of the low C_{dc} motor drives with dc link inductor...	133
Table 6.1 Simulation data of the conventional motor drives with front end diode rectifier operating at $M_i=0.83$	163
Table 6.2 Simulation data of the conventional motor drives with front end diode rectifier operating at $M_i=0.53$	164
Table 6.3 The simulation data obtained from the low C_{dc} motor drive without dc link inductor operating at $M_i=0.83$	165
Table 6.4 The simulation data obtained from the low C_{dc} motor drive without dc link inductor operating at $M_i=0.46$	166
Table 6.5 The simulation data obtained from the actively stabilized low C_{dc} motor drive with dc link inductor under constant torque load operating at $M_i=0.83$	168
Table 6.6 The simulation data obtained from the actively stabilized low C_{dc} motor drive with dc link inductor under constant torque load operating at $M_i=0.46$	171
Table 6.7 The simulation data obtained from the actively stabilized low C_{dc} motor drive with dc link inductor under fan load operating at $M_i=0.83$	172
Table 6.8 The simulation data obtained from the actively stabilized low C_{dc} motor drive with dc link inductor under fan load operating at $M_i=0.46$	173

Table 7.1 Qualitative comparison of conventional motor drives and low C_{dc} motor drives..... 179

CHAPTER 1

INTRODUCTION

1.1 Overview of AC Motor Drives

Variable speed drives are utilized in many industrial applications including fans, air compressors, pumps, elevators, rolling machines etc. Very often, ac motors are preferred in these applications and the drives are mostly fed by ac mains. To realize the variable speed control of ac machines, the ac mains power has to be processed to obtain the ac voltage at desired amplitude and frequency via the use of power converters.

1.2 AC Motor Drive Topologies

There exist various circuit topologies for ac motor drives which can be classified under two main groups, namely; ac-ac converters and ac-dc-ac converters. These two groups in turn, include various circuit types which are illustrated in Figure 1.1.

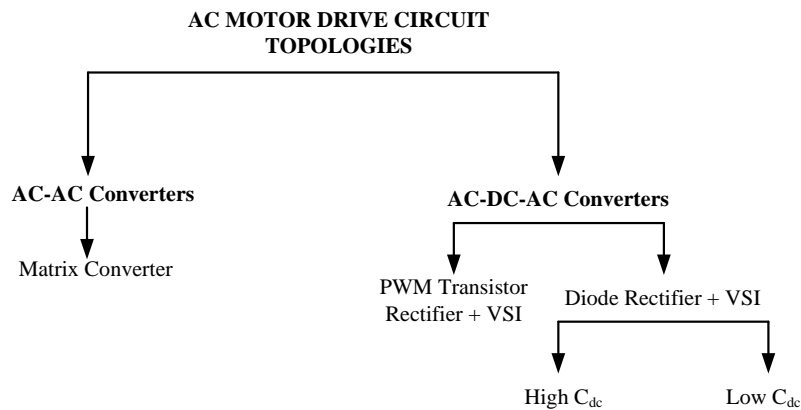


Figure 1.1 AC motor drive circuit topologies.

Ac-ac converters operate by direct conversion of the input ac voltage to output ac voltage, that is, without an intermediate power stage. Ac-dc-ac converters, on the other hand, perform the conversion by first rectifying the input ac voltage to dc and converting it to ac by utilizing a voltage source inverter at the output.

1.2.1 AC-AC Converters

Ac-ac converters convert the ac grid voltage to the desired output ac voltage directly, without an intermediate dc bus. Matrix converters are the popular examples for this type.

1.2.1.1 Matrix Converter

Matrix converter (Figure 1.2) includes bidirectional power semiconductor switches in its topology which are located so that each input phase can be connected to each output phase by allowing the bidirectional flow of the power. This also enables the regenerative operation of the motor. The matrix converters can generate pure sinusoidal output voltage and draw pure sinusoidal current from the grid. Thus, they offer a high quality ac output voltage and high input power quality. The converter operates by high frequency switching and as a result the passive components are small in volume, creating a compact circuit.

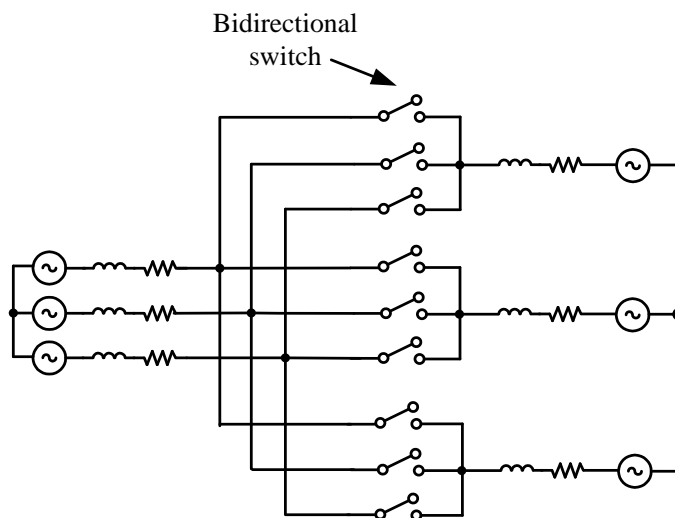


Figure 1.2 Matrix converter.

However, to enable the bidirectional flow of current, the number of switches used in a matrix converter is generally high and it increases the cost of the system. In addition, the switching pattern of the circuit is complex and requires careful implementation as it can easily cause a short between the phases. Another drawback of the matrix converter is that high frequency switching causes switching power loss and degrades the energy efficiency of the system. So, they found little usage in industrial applications and wait to be improved in terms of energy efficiency.

1.2.2 AC-DC-AC Converters

A large portion of the industrial motor drives utilize ac-dc-ac converters which rectify the ac mains voltage to dc and a PWM voltage source inverter (VSI) connected to dc bus is used to synthesize the ac voltage at desired amplitude and frequency to be applied to the motor.

At the dc-ac conversion stage generally voltage source PWM inverters are used. Due to high inductive structure of the motors, the high frequency current pulses generated by PWM voltage source inverters are filtered by the motor phases, so the motor currents have very low harmonic distortion. At the ac-dc conversion stage PWM transistor rectifiers and diode rectifiers are mostly used.

1.2.2.1 PWM Transistor Rectifier Cascaded with PWM Inverter

PWM transistor rectifiers (Figure 1.3) are connected to ac mains and used to obtain constant dc bus voltage. They are operated by high frequency switching of power semiconductor switches by closed loop control, and draw sinusoidal current from ac grid with very low harmonic distortion. The bidirectional flow of power is possible, which enables the regenerative operation of the motor.

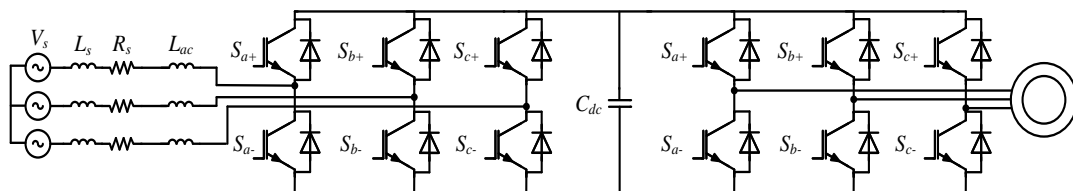


Figure 1.3 PWM transistor rectifier cascaded with PWM inverter.

Due to high frequency switching of semiconductor switches, however; PWM rectifiers are prone to high switching losses and thermal stresses, so their energy efficiency is low. For this reason, they did not find wide usage in industry and wait to be improved in terms of energy efficiency.

1.2.2.2 Diode Rectifier Cascaded with PWM Inverter

The PWM voltage source inverter with diode rectifier front end (Figure 1.4) is the most widely used motor drive topology in the industrial applications. Diode rectifiers are preferred due to their high energy efficiency and simple implementation.

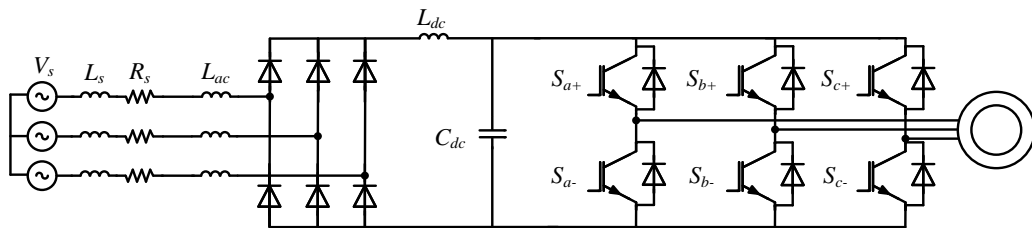


Figure 1.4 Diode rectifier cascaded with PWM inverter.

Conventionally, high capacitance (high C_{dc}) electrolytic capacitors are used with diode rectifiers to minimize the rectifier output voltage ripple. However in recent years, use of low capacitance (low C_{dc}) film capacitors instead of electrolytic ones gained interest due to significant improvements that the film capacitor brings to eliminate the drawbacks of conventional high C_{dc} electrolytic capacitors, which will be explained in the upcoming section. So, it is appropriate to analyze the diode rectifier front end motor drives in two groups; drives utilizing high C_{dc} electrolytic capacitors and ones using low C_{dc} film capacitors.

1.2.2.2.1 Diode Rectifier Utilizing High Capacitance Electrolytic Capacitor

Three-phase diode rectifiers generate large voltage ripple on the dc bus and they are conventionally equipped with high C_{dc} capacitors to reduce the voltage ripple. The bus capacitor also acts as a filter for the current ripples injected from rectifier and inverter side. The high capacitance creates a stiff dc bus voltage and due to high energy storage, the dc bus voltage stability is protected under abnormal grid voltage variations and possible

changes in motor load. The electrolytic type capacitors offer the highest capacitance/volume ratio and are the most widely used capacitor types in these circuits.

Even if they create a stable and low ripple dc bus voltage, electrolytic capacitors have some disadvantages. Their ESR values are generally high and have heating problems. They cannot offer average life time greater than five years and need to be replaced by a new one, which increases the cost of the system. Due to their large size, the volume of the circuit increases and system becomes bulky. The high capacitance minimizes the dc bus voltage ripple but meanwhile disturbs the continuity of dc bus and the line current. The inductor filters used to suppress the line current harmonics are also large in size as total harmonic distortion (THD_{ig}) caused by high capacitance is very high. In addition, the large capacitor requires precharge circuitry to limit the inrush current and charge the capacitor prior to operation of the drive.

1.2.2.2.2 Diode Rectifier Utilizing Low Capacitance Film Capacitor

Due to the mentioned drawbacks of high C_{dc} electrolytic capacitors, the rectifiers equipped with smaller size film capacitors took interest of researchers and manufacturers due to many advantages they offer compared to the problematic features of high C_{dc} electrolytic capacitors.

The first point of interest is the long lifetime of film capacitors. Film capacitors do not contain electrolytics in their structure and can offer much longer life time than electrolytic capacitors (broadly four times longer). So they very rarely need to be replaced by a new one during the lifetime of the motor drive circuit. Due to their small size, the circuit volume is significantly reduced. So, a reduction in the passive component size replaces the bulky circuit with a more compact one, which makes it possible to design integrated motor drive systems. The other improvement gained by using low C_{dc} capacitor is seen in the line current quality. Due to low capacitance, the energy storage capability of dc bus is lower and dc bus voltage ripple is higher than obtained with use of electrolytic ones. However, low capacitance increases the continuity of the dc link current and the ac line current, and THD_{ig} is decreased significantly compared to conventional high C_{dc} rectifier circuit. This brings the advantage of using much smaller size inductor filters to suppress the ac line current harmonics. Even no additional inductor filter can be used and the circuit can be

operated solely by line inductance if the dc bus capacitance is sized properly. This results in significant cost reduction. One more advantage of low C_{dc} capacitors is that there is no risk of inrush current and no need for precharge circuit exists, which again decreases the cost.

Despite its stated advantages, unlike the high C_{dc} electrolytic ones the energy storage of low C_{dc} film capacitors is limited and the bus voltage is not stiff, which degrades the stability of the dc bus under possible motor load changes or ac grid voltage variations. In addition, the hold-up time of the circuit is decreased. The non-stiff dc bus voltage can easily become unstable and active stabilization control is required for the dc bus voltage, which is investigated in detail in the subsequent chapters.

1.3 AC Motor Drive Performance Criteria

A motor drive has to satisfy certain performance criteria like every commercial design has to do. The designed motor drive circuit should be both consistent with the international input power quality standards and show satisfactory motion performance. In addition, it should offer satisfactory reliability and low cost. Besides, a small volume design is more preferred instead of a bulky system.

1.3.1 Input Power Quality

The term input power quality covers the line current distortion and input power factor of a circuit connected to ac mains. It is known that the power consumed by the electric motors constitute the 65 % of the total power consumption in industrial applications [1]. More specifically, in Turkey, 40 % of the total power generation is consumed on the electric motors [2]. Thus, the line current quality of the ac motor drive circuits is an important point to consider for the performance analysis of the circuit.

1.3.1.1 Line Current Distortion

A circuit fed by ac mains is always desired to draw sinusoidal current as possible. This is due to the fact that only the frequency component of the line current at the grid voltage frequency (the fundamental component) can generate real power for the load and the components at different frequencies, i.e. the harmonics, do not contribute to the real power

and causes losses on the circuit. In addition the harmonics may cause resonance in the circuit which can cause instabilities. For this reason, the acceptable level of harmonics in line current is subjected to strict international standards and a circuit fed by ac mains has to be consistent with the total harmonic distortion (THD_{ig}) levels defined by these standards such as EN61800-3, IEC1000-3-2, IEC1000-3-4, IEEE519 [3].

The line current quality can be investigated by total current harmonic distortion (THD_{ig}) given by (1.1) where I_g is the rms of the line current and I_{g1} is the rms of the fundamental component of the line current, and I_{gh} is the h^{th} line current harmonic.

$$\% \text{THD}_{ig} = 100 * \frac{\sqrt{I_g^2 - I_{g1}^2}}{I_{g1}} = 100 * \sqrt{\sum \left(\frac{I_{gh}}{I_{g1}}\right)^2} \quad (1.1)$$

The importance of the line current distortion depends also on the load level. If the circuit is operating under full load, the THD_{ig} gains more importance compared to operation under lighter loads since high distortion does not cause much problem for lower load levels. To express this relation, total current demand distortion TDD_{ig} given by (1.2) is used which is the ratio of the total harmonic current rms value for operating load level to the fundamental current component for full load operation. Thus the THD_{ig} and TDD_{ig} are equal to each other for full load operation.

$$\% \text{TDD}_{ig} = 100 * \frac{\sqrt{I_g^2 - I_{g1}^2}}{I_{\text{full_load}1}} = 100 * \sqrt{\sum \left(\frac{I_{gh}}{I_{\text{full_load}1}}\right)^2} \quad (1.2)$$

1.3.1.2 Input Power Factor

Power factor is a measure of how effective a circuit draws ac power from the utility. It is defined as the ratio of the real power to the apparent power, given by (1.3).

$$\text{PF} \triangleq \frac{P}{S} \quad (1.3)$$

In (1.3), P is the real power (W) and S is the apparent power (VA). The real power P and apparent power S are defined by (1.4) and (1.5) respectively.

$$P \triangleq V_g I_{g1} \cos \varphi_1 \quad (1.4)$$

$$S \triangleq V_g I_g \quad (1.5)$$

V_g is the ac mains line to neutral voltage (rms) and I_{g1} is the fundamental component of the line current (rms), I_g is the total line current (including both fundamental and harmonics), and φ_1 is the phase difference between them. The term $\cos \varphi_1$ is defined as displacement power factor (DPF) [4]. For pure sinusoidal line currents, the power factor term consists of only DPF. However, for cases in which the line current includes harmonics, the definition of the power factor includes distortion factor in addition to DPF which can be obtained by putting (1.4) and (1.5) into (1.3), given by (1.6);

$$PF \triangleq \frac{V_g I_{g1} \cos \varphi_1}{V_g I_g} = \frac{I_{g1}}{I_g} \text{DPF} \quad (1.6)$$

Thus, it is deduced from (1.6) that if the line current includes harmonics, the power factor decreases. Hence, a circuit is desired to draw power from the ac mains with a power factor as close as possible to unity by drawing low distorted current. The nonlinear loads and many power electronic converters fed by ac utility cause line current harmonics and decrease the power factor. There is certain power factor limits defined for the consumers that should not be exceeded otherwise penalties are applied. As the high percentage of the power consumed by motor drive circuits to the total power generation is considered, the input power factor of the motor drive circuits fed by ac utility gains vital importance. The drive performance analysis thus includes input power factor.

1.3.2 Motor Motion Quality

The main aim to design a motor drive is to obtain the desired motion profile from the motor. Thus, the motor drive performance depends on how well the inverter and controller drive the motor. For example, an elevator is required to operate with a constant torque and speed throughout the motion in a building. If an excessive torque ripple exists on the

motor, the cabinet will seriously feel the vibration and variation in the speed, which is not desired. Likewise, the speed of a fan is desired to be constant throughout the operation since the fan speed affects the cooling performance. One more example can be given for positioning applications, where any torque disturbance existing in the system has to be successfully rejected otherwise the placement of the device will not be accurate. Thus, a drive must be capable of delivering the required motion quality demanded by the application.

1.3.3 System Reliability, Size, and Cost

A motor drive system must offer reliable operation throughout its lifetime. The term reliability may include the proper operation of drive components, operation of the drive at different environmental conditions such as temperature, humidity, etc., and also compliance with EMI/EMC criteria defined by the product standards.

As a fundamental requirement of engineering discipline, the cost of the design must be kept in an acceptable range. In addition to offering high operation performance, a motor drive should be as cost effective as possible. As a very basic design improvement, decreasing the number of drive circuit components without a compromise in the operation performance brings significant cost reduction, especially in mass productions.

Due to fast changing technology, all electronic devices are getting smaller in size, including motor drives. Manufacturers try to develop compact motor drives integrated with the motor chassis to minimize the system volume. Many motor drives circuits are tried to be manufactured in a single package including the bus capacitor, filter inductors if any, and the power semiconductors of the inverter [5]. A smaller motor drive offers increased mobility for the consumers. To illustrate, in submersible pump applications it is easier and more economical to submerge the inverter and motor as a single integrated unit instead of separate masses, which makes the use of low C_{dc} small capacitor drive system an ideal choice for such applications.

1.4 Scope of the Thesis

This thesis focuses on the analysis, design, and comparison of conventional motor drive circuits with front end diode rectifiers utilizing high C_{dc} capacitor and the motor drives with low C_{dc} film capacitors at the dc bus.

Chapter 2 includes the investigation of various motor load characteristics and their effects on the motor dynamics and dc bus voltage stability. Because the load types influence the drive system stability, distinguishing load types is important. Since in most of the thesis vector control is employed, here a brief review is provided. The principles and formula for coordinate transformation from stationary to synchronous reference frame are explained. The induction machine model in stationary and synchronous reference frame are analyzed and the speed controller design is given.

Chapter 3 makes a review of conventional motor drive circuit design and operating principles. It starts with the operation principle of ideal three-phase diode rectifiers, and investigates their line current and bus voltage characteristics. Then the components used in practical diode rectifier design are described and operation of the practical circuit is analyzed. Next, the PWM voltage source inverter and operation principles are given. At the end, the operation of the complete drive system obtained from the rectifier inverter combination is introduced.

Chapter 4 involves the simulation results of the conventional motor drive circuit with front end diode rectifier utilizing high C_{dc} dc bus capacitor and gives the performance figures at line side and motor side. It compares the motor drive operation with and without dc bus disturbance rejection under constant torque and fan loads.

Chapter 5 investigates the design of diode rectifiers with low C_{dc} dc bus capacitor. The basic design rules of sizing the bus capacitor for keeping stability are given. Some of the voltage and current mode active stabilization methods found in literature which are used to stabilize the dc bus voltage are investigated. The chapter includes the results of motor drive simulations with and without active stabilization algorithms and analyzes the input power quality and motion performance of the designed motor drives.

Chapter 6 provides a performance comparison of the conventional high C_{dc} motor drive and low C_{dc} drives using the simulation results. Quantitative comparisons are made in terms of input power quality, dc bus voltage stability, and motor motion quality.

Chapter 7 summarizes the work done in the thesis and provides the future work. The results of the simulations and the conclusions drawn from the comparison of the conventional drives and the drives utilizing low C_{dc} dc bus capacitor are provided. A qualitative evaluation of the investigated motor drives and active dc link stabilization methods is also included.

CHAPTER 2

LOAD TYPES AND THREE-PHASE AC MACHINE CONTROL METHODS

2.1 Electric Motor Load Types

The electric motors are used for various applications which own different load characteristics. Each load type depending on its physical nature affects the drive circuit operation differently. There are mainly three types of loads namely; constant torque loads, constant power loads, and variable torque loads.

2.1.1 Constant Torque Load

This type of load demands constant torque throughout the entire speed range of the motor. Thus, with constant torque the power consumed by the motor increases linearly with the speed [6]. Figure 2.1 illustrates the torque speed and power speed characteristics for the constant torque load. The parameters are given in per unit rather than specific units to describe the conceptual load behavior.

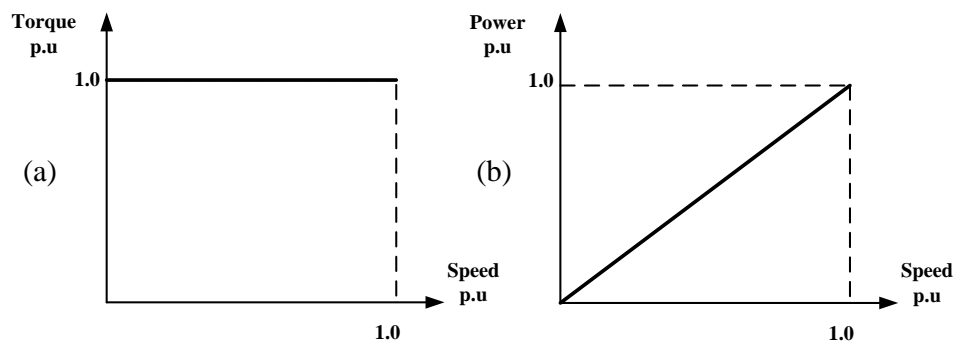


Figure 2.1 (a) Constant torque load torque-speed characteristics, (b) power-speed characteristics.

General machinery hoists, printing press, conveyors, extruders, elevators, escalators, and surface winders are typical examples for constant torque loads.

2.1.2 Constant Power Load

Under constant power load operation, the motor draws constant power throughout the entire speed range. Thus, it needs low torque (T) at high speeds (ω) and high torque at low speeds, keeping the $T * \omega$ value constant. Figure 2.2 illustrates the torque-speed and power-speed characteristics of the constant power load.

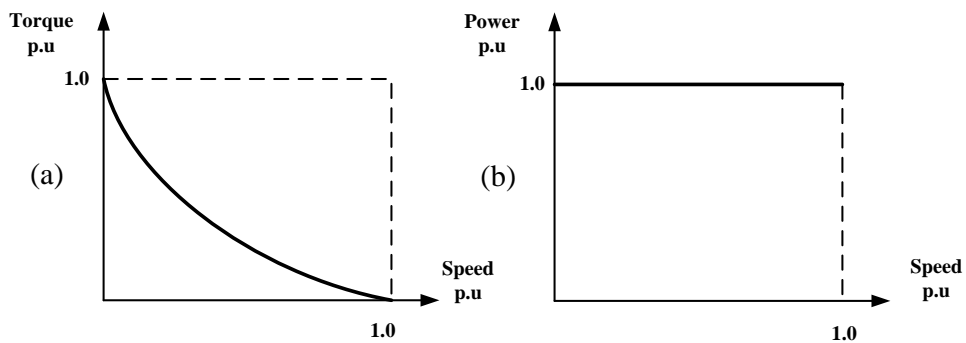


Figure 2.2 (a) Constant power load torque-speed characteristics, (b) power-speed characteristics.

Center-driven winders, machine tool spindles, metal cutting tools, mixers, and extruders can count in constant power load group.

2.1.3 Variable Torque Load

Variable torque load changes its torque requirement by the variation in speed. The torque may increase linearly or proportional to the square of the speed (quadratically), hence the power consumption increases with square of the speed or the cube of the speed respectively. Figure 2.3 shows the torque-speed and power-speed characteristics of some variable torque loads.

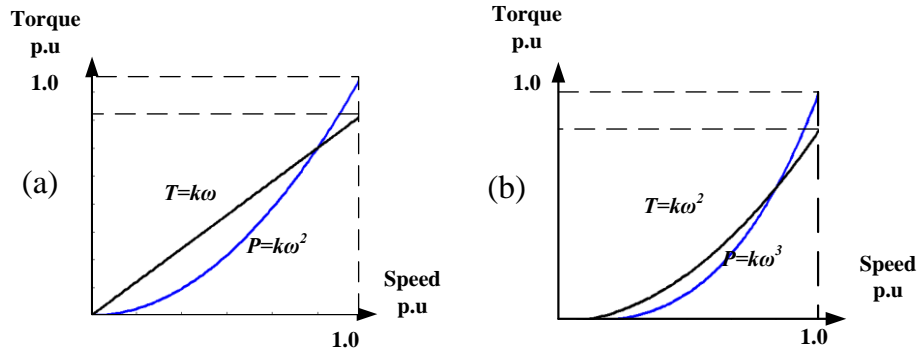


Figure 2.3 Variable torque load torque-speed (black) and power-speed (blue) characteristics (a) Torque varying linearly with speed (b) Torque varying with square of the speed.

For the applications in which the load torque increases linearly with speed and the power varies as square of the speed; positive displacement pumps, some mixers, and some extruders can be count as examples. The torque-speed and power-speed relations of such loads are given by (2.1) and (2.2), where k is the constant depending on the operating characteristics of the device.

$$T = k\omega \quad (2.1)$$

$$P = T\omega = k\omega^2 \quad (2.2)$$

The applications in which the load torque varies with the square of speed and power varies as cube of the speed; all centrifugal pumps and some fans can be given as typical examples, for which the torque-speed and power-speed relations are given by (2.3) and (2.4).

$$T = k\omega^2 \quad (2.3)$$

$$P = T\omega = k\omega^3 \quad (2.4)$$

2.2 Electrical Interpretation of Load Mechanical Characteristics

The mechanical characteristics of the load types have electrical interpretations on the drive circuit. To start the discussion, an analogy can be setup between torque-current and speed-voltage quantities of the motor. As the speed of a motor increases, its back emf will increase proportional to the back emf constant, so; the voltage applied to the motor should

be increased. For this reason, speed and voltage can be used instead of each other for analysis of the motor operation. Likewise, the torque of the motor is proportional to current it draws by its torque constant; hence torque and current are exchangeable parameters for describing the motor operation.

2.2.1 Negative and Positive Impedance Effect

Using the speed-voltage and torque-current analogies, the effect of the load type on the variation of the voltages and currents in the circuit can be estimated. For example, a constant torque load will demand the same current from the motor drive whatever the motor operating speed is. A constant power load tries to keep the power it draws at a constant value, that is, the product of applied voltage and current drawn by the motor is kept constant. As the applied voltage increases, the current drawn will be decreased and vice versa. Due to the inverse relation between voltage and current, the constant power load creates negative impedance effect for power supply of the motor drive. They can also be assumed as active loads, since they can change their voltage and current demand to keep the power they draw constant. The torque demand of the variable torque load increases or decreases depending on the operating speed. As the voltage applied to the motor increases, the load speeds up and the torque demand is increased proportionally. As the applied voltage is lowered, the motor speed is lowered and torque demand decreases, so does the current. Thus, as the voltage and current changes proportional to each other, variable torque loads show positive impedance characteristics or they can be called passive loads. The negative and positive impedance characteristics of the loads may significantly affect the stability of the drive circuit, especially the bus voltage of the diode rectifiers. A positive impedance load does not cause any instability since it has a passive nature and its behavior is primarily determined by bus voltage. On the other hand, negative impedance or active loads may cause instabilities on the power supply of the motor drive by increasing or decreasing the bus voltage rapidly to keep the power consumption at a constant value. Thus, unlike positive impedance loads, their operation characteristics primarily affect the bus voltage behavior.

2.3 Three-Phase AC Machine Control Methods

AC machines can be controlled by various methods and each method introduces different control performance. Among most commonly used methods; constant V/f control and vector control (field oriented control) can be count. Both of these methods show satisfactory steady state motor performance but the dynamic motor performance differs between them.

The control methods explained are applicable to any kind of three-phase ac machine such as, synchronous machine, permanent magnet synchronous machine (PMSM), and induction machine, with slight differences in implementations due to differences in motor operation principles. In this section, first the general principles of control methods are explained for general three-phase ac machines. Then, the application of indirect vector control for induction machines is discussed in detail. Finally, the speed and current regulator design for induction machine is given.

2.3.1 Constant V/f Control

The main principle of this method is keeping the flux of the ac machine at a constant value by keeping the ratio of the applied voltage to the excitation frequency at a constant value. In modern motor drives, this is achieved by modulation of a dc voltage by pulse width modulation using a PWM voltage source inverter. In constant V/f method, there is no feedback used for speed and position, so it is an open loop control method. As there is no feedback device, the cost of the system is low. However, since the field orientation is not used, the torque control performance, thus the dynamic response of the machine is poor with constant V/f control [7].

2.3.2 Vector Control (Field Oriented Control)

The open loop constant V/f control shows poor dynamic response due to deviation of flux linkage from set value both in terms of magnitude and phase. The oscillations in air gap flux linkages cause oscillations in the torque and speed of the motor. In addition, the flux linkage oscillations cause excursions of stator currents and this requires a higher peak current rating inverter to meet the dynamics [8]. To overcome these effects the flux can be controlled separately from the torque like a separately excited dc machine. This is

accomplished by vector control (field oriented control) which aims to decouple the flux and torque channels of the machine. By closed loop current control the rotor flux linkage and machine torque are kept at their set values. This results in a high dynamic motor performance by enabling instantaneous torque control.

The implementation of vector control requires the transformation of three-phase machine quantities, such as voltages, currents, and flux linkages into two-phase equivalents. Throughout the foregoing analysis, the machine is assumed to have balanced three-phase windings and be operating with balanced three-phase inputs. So, the zero sequence components which are faced during unbalanced operation are not considered.

2.3.2.1 Three-phase to Two-phase Transformation of Motor Quantities

Transformation of the electrical variables of an n-phase machine into two-phase ones is preferred both to simplify the modeling of the machine and design of the controller. The transformation is accomplished by using complex space vectors which represent the electrical quantities as complex vectors on their respective axes. This task is carried out throughout the transformation by keeping either the magnitude of the total machine mmf or the machine power unchanged. The transformations used in this thesis are performed using power invariance rule.

The three-phase to two-phase transformation formula is the same for all machine quantities for both stator and rotor. The transformation procedure is explained using the stator phase currents as examples but can be applied to any other stator or rotor variable. The space vector representation of the sum of the stator phase currents i_{as} , i_{bs} , and i_{cs} is defined by (2.5) [9].

$$i_s = k(i_{as} + ai_{bs} + a^2i_{cs}) \quad (2.5)$$

In (2.5), $a = e^{j2\pi/3}$ is the spatial operator and $k=2/3$ is the transformation constant for power invariance. Figure 2.4 shows the space vector representation of three-phase stator currents i_{as} , i_{bs} , and i_{cs} and their vector sum i_s . By this notation, the phase currents of the three-phase machine are represented as vectors on stationary orthogonal reference frame.

The vector sum of the three-phase currents is rotating around air gap at an angular velocity equal to the stator excitation frequency, ω_e [9].

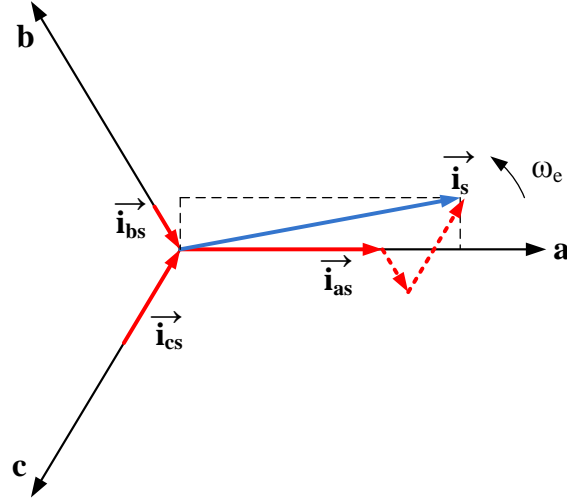


Figure 2.4 Space vector representations of three-phase machine currents.

The transformation can be carried on step by step, by first transforming the three-phase quantities into two-phase ones $i_{\alpha s}$, $i_{\beta s}$ on stationary reference frame α - β axes as shown in Figure 2.5. For a balanced three-phase system, $i_{as} + i_{bs} + i_{cs} = 0$. Thus the transformation from a-b-c to α - β variables is done by using only two of the three-phase quantities as in (2.6) and (2.7) [9].

$$i_{\alpha s} = i_{as} \quad (2.6)$$

$$i_{\beta s} = \frac{1}{\sqrt{3}}i_{as} + \frac{2}{\sqrt{3}}i_{bs} \quad (2.7)$$

The inverse transformation used to obtain a-b-c axis variables from α - β axis variables is given by (2.8), (2.9), and (2.10) [9].

$$i_{as} = i_{\alpha s} \quad (2.8)$$

$$i_{bs} = -\frac{1}{2}i_{\alpha s} + \frac{\sqrt{3}}{2}i_{\beta s} \quad (2.9)$$

$$i_{cs} = -\frac{1}{2}i_{\alpha s} - \frac{\sqrt{3}}{2}i_{\beta s} \quad (2.10)$$

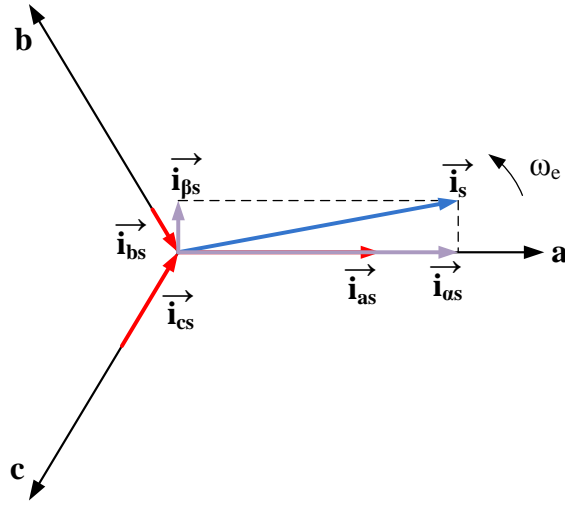


Figure 2.5 Two-phase stationary frame components of three-phase stator currents.

The second transformation transforms the two-phase quantities on stationary reference frame into the ones at an arbitrary reference frame [8], which is not stationary in space but rotating at an arbitrary speed. For the commonly used reference frames; the stator reference frame, rotor reference frame, and rotor flux reference frame can be count [8]. For any of the reference frames, the same transformation formula applies with only difference in the speed ω and instantaneous position angle θ of the chosen frame with respect to reference axis chosen. The transformation used to transform the three-phase quantities to rotor flux reference frame is called synchronous reference frame transformation. Since the rotor flux reference frame and the phase quantities rotate at the same electrical speed ω_e , the relative speed between them becomes zero. As a result, the quantities obtained by synchronous reference frame transformation are dc quantities. This simplifies the design of current regulators by using dc variables instead of dealing with ac ones. To distinguish the synchronous reference frame from arbitrary reference frame transformations, the electrical quantities in synchronous reference frame are denoted by superscript “e” throughout the thesis. Figure 2.6 shows the d and q axis current space vectors i_{ds}^e and i_{qs}^e for the synchronous reference frame together with the three-phase and two-phase stationary reference frame current vectors.

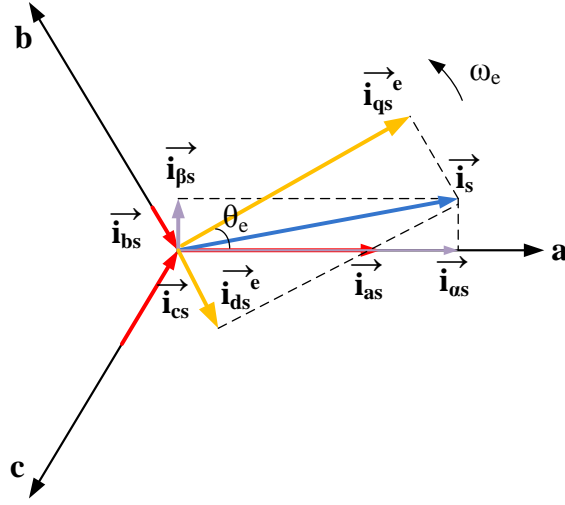


Figure 2.6 Synchronous reference frame d and q axis current space vectors.

The q and d axis currents are obtained from α and β axis currents by (2.11) and (2.12).

$$i_{qs}^e = i_{\alpha s} \cos \theta_e + i_{\beta s} \sin \theta_e \quad (2.11)$$

$$i_{ds}^e = i_{\alpha s} \sin \theta_e - i_{\beta s} \cos \theta_e \quad (2.12)$$

The inverse transformation from q and d axes to α and β axes are done using (2.13) and (2.14).

$$i_{\alpha s} = i_{qs}^e \cos \theta_e + i_{ds}^e \sin \theta_e \quad (2.13)$$

$$i_{\beta s} = i_{qs}^e \sin \theta_e - i_{ds}^e \cos \theta_e \quad (2.14)$$

2.3.2.2 Principle of Vector Control

Having derived the stator current expressions in synchronous reference frame, the basic idea behind the vector control can be explained. The vector control aims to decouple the flux and torque channels of the machine and controls them separately like that of a separately excited dc machine. This is accomplished by aligning the component of stator current vector creating the rotor flux linkage, the d axis current i_{ds}^e , with the rotor flux linkage phasor λ_f rotating with the synchronous speed ω_e . Accordingly, the q axis

component of the stator current vector i_{qs}^e becomes responsible for torque generation. Using a closed loop current controller, the d axis current is set to a predefined value to obtain the required flux. By adjusting the q axis current, the torque of the machine can be adjusted as desired.

2.4 Vector Control of Induction Machine

This section provides the basic principles of the vector control of induction machine. In the section; the material representing the machine model, the equations describing its operation, the implementation of vector control, and controller design are introduced using the modeling, equations, and algorithms provided by [8].

First a brief review of the induction machine operation is given using the single phase steady state equivalent circuit. Then the details of the indirect vector control algorithm are given.

2.4.1 Induction Machine Principle of Operation

The principle of operation of an induction machine can be explained by the rotating magnetic field theory. When a set of three-phase balanced voltages is applied to the stator windings of the machine, a magnetic field rotating with the frequency of the supply current is generated. By Faraday's law, this changing field induces a voltage in rotor windings and results in a flow of current in a direction so that a magnetic field counter to the rotating field is generated [8]. The interaction of the induced rotor currents and the rotating mmf creates a torque on the rotor and rotation is accomplished [9]. The generation of the non-zero rotor currents depends on the existence of an induced voltage, thus a changing magnetic field on rotor windings, which is possible only when the rotor mechanical speed is different than the speed of rotating mmf. So an induction machine can produce torque only when the rotor mechanical speed is different than the speed of rotating magnetic field. The speed of the rotating magnetic field is called synchronous speed, ω_e (2.15). The difference between the synchronous speed and electrical rotor speed, ω_r , is defined as slip speed ω_{sl} by (2.16).

$$\omega_e = 2\pi f_e \text{ (rad/s)} \tag{2.15}$$

$$\omega_{sl} = \omega_e - \omega_r \text{ (rad/s)} \quad (2.16)$$

In (2.15), f_e denotes stator supply frequency. The induced emf in the rotor is at the slip frequency so is the rotor currents. The slip “s” is defined by (2.17);

$$s = \frac{\omega_{sl}}{\omega_e} \quad (2.17)$$

The relationship between the rotor mechanical speed, ω_m , and electrical speed, ω_r , is given by (2.18) where P denotes the number of rotor poles.

$$\omega_r = \omega_m \frac{P}{2} \text{ (rad/s)} \quad (2.18)$$

2.4.2 Steady State Equivalent Circuit and Equations of Induction Machine

The induction machine can be modeled by stator resistance per phase (R_s), stator leakage inductance per phase (L_{ls}), rotor resistance per phase (R_{rr}), rotor leakage inductance per phase (L_{lrr}), mutual inductance denoting the mutual flux between stator and rotor per phase (L_m), stator turns ratio per phase (N_1), rotor turns ratio per phase (N_2), stator induced emf per phase (\vec{E}_1), rotor induced emf per phase (\vec{E}_2), and supply voltage per phase (\vec{V}_{as}). Figure 2.7 shows the per phase equivalent circuit of the induction machine [8].

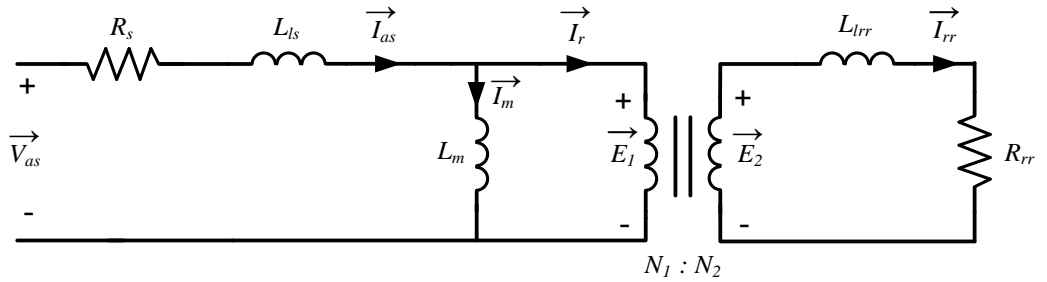


Figure 2.7 Per phase equivalent circuit of the induction machine.

To simplify the analysis of the circuit, the rotor parameters can be referred to the stator. To achieve this, the rotor side current can be calculated by the stator side induced emf using

the turns ratio between the rotor and stator [8]. The ratio between the induced emfs is given by (2.19) where $c=N_1/N_2$;

$$\frac{E_2}{E_1} = s \frac{N_2}{N_1} = \frac{s}{c} \quad (2.19)$$

The rotor current I_r can be calculated by (2.20);

$$\vec{I}_{rr} = \frac{\vec{E}_2}{R_{rr} + j\omega_s L_{lrr}} = \frac{\vec{E}_2}{R_{rr} + js\omega_e L_{lrr}} \quad (2.20)$$

Using (2.19) and writing \vec{E}_2 in terms of \vec{E}_1 ;

$$\vec{I}_{rr} = \frac{\frac{\vec{E}_1}{c}}{\frac{R_{rr}}{s} + j\omega_e L_{lrr}} \quad (2.21)$$

By this formulation, the rotor side current is defined by stator side induced emf and the stator supply frequency. So, the per phase equivalent circuit is modified as in Figure 2.8. In this circuit, I_r is the rotor current reflected to the stator side and is related to the rotor current by (2.22) [8].

$$I_r = \frac{I_{rr}}{c} \quad (2.22)$$

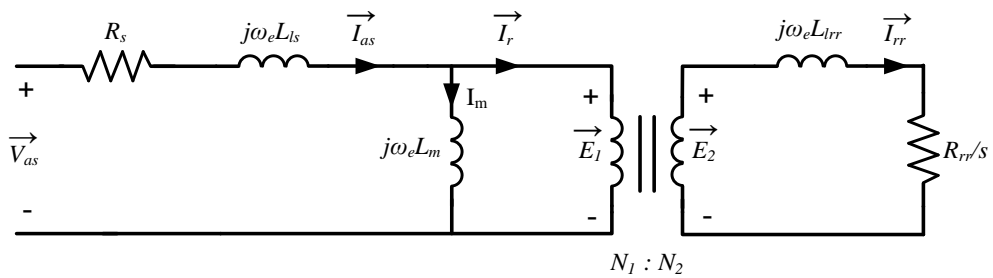


Figure 2.8 Modified per phase equivalent circuit of the induction machine.

Substituting (2.22) to (2.21), I_r is found as in (2.23).

$$\vec{I}_r = \frac{\vec{E}_1}{\frac{c^2 R_{rr}}{s} + j\omega_e c^2 L_{lrr}} = \frac{\vec{E}_1}{\frac{R_r}{s} + j\omega_e L_{lr}} \quad (2.23)$$

where R_r is the stator referred rotor resistance and L_{lr} is the stator referred rotor leakage inductance given by (2.24) and (2.25) respectively [8].

$$R_r = c^2 R_{rr} \quad (2.24)$$

$$L_{lr} = c^2 L_{lrr} \quad (2.25)$$

By using the stator referred quantities of the rotor, the per phase equivalent circuit is modified to the final form as in Figure 2.9. With this configuration, the rotor and stator have the same frequency and induced emf E_1 and the circuit is physically connected. The core loss is represented by the core resistance parallel to the magnetizing inductance. The reactances corresponding to the related inductances are found by using the stator excitation frequency, ω_e [8].

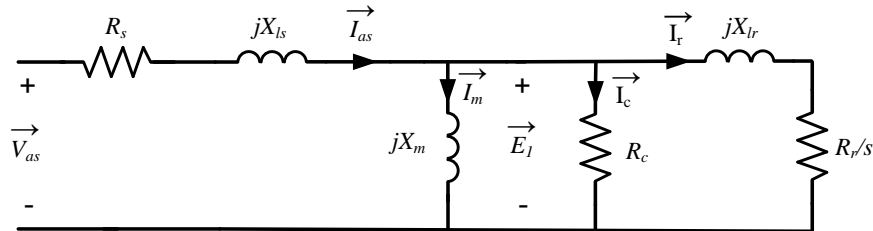


Figure 2.9 Per phase equivalent circuit of induction machine with rotor at stator frequency.

The stator self inductance L_s is found by sum of magnetizing inductance L_m and stator leakage inductance L_{ls} and rotor self inductance is found by summation of magnetizing inductance L_m and rotor leakage inductance L_{lr} [8].

$$L_s = L_m + L_{ls} \quad (2.26)$$

$$L_r = L_m + L_{lr} \quad (2.27)$$

Using the stator referred per phase equivalent circuit, the steady state power equations of the machine can be derived. A portion of the total input power is dissipated in the stator resistance, called stator copper loss. The difference between the total input power and stator copper loss is called air gap power, P_g , (neglecting core loss) given by (2.28).

$$P_g = P_i - 3I_{as}^2 R_s \quad (2.28)$$

As the power transmitted to the rotor is modeled by the power dissipation in the active resistance R_r/s and neglecting the core losses, the air gap power is equal to the power dissipated on R_r/s , given by (2.29) [8].

$$P_g = 3I_r^2 \frac{R_r}{s} \quad (2.29)$$

Subtracting the rotor copper loss from this equation, the motor mechanical power P_m is derived by (2.31).

$$P_g = 3I_r^2 \frac{R_r}{s} = 3I_r^2 R_r + 3I_r^2 \frac{R_r(1-s)}{s} \quad (2.30)$$

$$P_m = 3I_r^2 \frac{R_r(1-s)}{s} \quad (2.31)$$

The term $3I_r^2 R_r$ in (2.30) represents the rotor copper loss of the motor. The electromagnetic torque T_m is found by dividing motor mechanical power by mechanical speed ω_m .

$$T_e = \frac{P_m}{\omega_m} \quad (2.32)$$

The shaft output power, P_s , is found by subtracting the friction and windage losses, P_{fw} , from the motor mechanical power P_m .

$$P_s = P_m - P_{fw} \quad (2.33)$$

2.4.3 Dynamic Modeling of Induction Machine

Steady state model of the induction machine represents the performance of the machine in steady state hence does not give idea about the electrical transients faced during load changes, stator frequency variations, and torque disturbances [8]. Since most of the machines are driven by converters and the transient ratings of the converter semiconductor switches are limited, the dynamic response of the motor is limited accordingly. Hence, the machine response to such transients can only be understood by using its dynamic model.

The dynamic model of the induction machine is constructed in two-phase system to simplify the analysis. The model is constructed on two sets of windings, stator and rotor windings, on direct and quadrature axes. So, the derivation of the dynamic model requires the transformation of machine parameters from three-phase to two-phase system. The process is then expanded by reference frame transformation and machine parameters are transformed from stationary reference frame to arbitrary rotating reference frame of interest, which further simplifies the analysis.

Throughout the model derivation, the following assumptions are made; the air gap is assumed to be uniform, the stator and rotor windings and excitations are balanced, mutual inductance variation with the rotor is sinusoidal, and parameter variation and saturation effects are neglected [8].

2.4.4 Two-phase Model of the Induction Machine

The model derivation of the induction machine in two-phase system is started by writing down the stator and rotor terminal voltage equations. The terminal voltages of the stator and rotor are the sum of the voltage drops on resistances and inductances of the machine. This includes the self resistances, self inductances, and mutual inductances between the windings.

The mutual inductances between the phases of stator and between the phases of rotor are zero since they are 90° electrical apart from each other and no flux can link between phases [8]. The mutual inductance between the rotor and stator phases varies sinusoidally with the electrical rotor angle θ_r . Due to symmetry in the windings, the mutual inductance seen from either stator or rotor is the same. Instead of dealing with sinusoidally changing inductance

values with the rotation of the rotor, which is time consuming, the model analysis here refers all the rotor quantities to the stator so the inductance terms turn into constants. Hereafter, both for the derivation of the induction machine model and in the upcoming chapters, the subscript d or q will represent the quantities in d and q axes and the subscript s and r will refer to whether the quantity is of the stator or rotor, and p will be the differential operator. The terminal voltages for stator and rotor in d and q axes can be written as in (2.34) to (2.37) [8].

$$V_{qs} = (R_s + L_s p)i_{qs} + L_m p i_{qr} \quad (2.34)$$

$$V_{ds} = (R_s + L_s p)i_{ds} + L_m p i_{dr} \quad (2.35)$$

$$V_{qr} = L_m p i_{qs} - L_m \dot{\theta}_r i_{ds} + (R_r + L_r p)i_{qr} - L_r \dot{\theta}_r i_{dr} \quad (2.36)$$

$$V_{dr} = L_m \dot{\theta}_r i_{qs} + L_m p i_{ds} + L_r \dot{\theta}_r i_{qr} + (R_r + L_r p)i_{dr} \quad (2.37)$$

$$\begin{bmatrix} V_{qs} \\ V_{ds} \\ V_{qr} \\ V_{dr} \end{bmatrix} = \begin{bmatrix} R_s + L_s p & 0 & L_m p & 0 \\ 0 & R_s + L_s p & 0 & L_m p \\ L_m p & -L_m \dot{\theta}_r & R_r + L_r p & -L_r \dot{\theta}_r \\ L_m \dot{\theta}_r & L_m p & L_r \dot{\theta}_r & R_r + L_r p \end{bmatrix} \begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{qr} \\ i_{dr} \end{bmatrix} \quad (2.38)$$

R_s : the stator self resistance per phase

L_s : the stator self inductance per phase

R_r : the stator referred rotor self resistance per phase

L_r : the stator referred rotor self inductance per phase

L_m : mutual inductance between stator and rotor

θ_r : rotor electrical position with respect to d axis

2.4.5 Synchronous Reference Frame Model of Induction Machine

As mentioned previously, dealing with dc quantities instead of sinusoidal ones simplifies the analysis of the machine and is main the advantage of using synchronous reference frame. The calculation of induction machine stator currents in synchronous reference frame is done by applying (2.6), (2.7), (2.11), and (2.12) successively to stator phase currents. The model equations are given by the matrix in (2.39) [8].

$$\begin{bmatrix} V_{qs}^e \\ V_{ds}^e \\ V_{qr}^e \\ V_{dr}^e \end{bmatrix} = \begin{bmatrix} R_s + L_s p & \omega_e L_m & L_m p & \omega_e L_m \\ -\omega_e L_m & R_s + L_s p & -\omega_e L_m & L_m p \\ L_m p & (\omega_e - \omega_r) L_m & R_r + L_r p & (\omega_e - \omega_r) L_r \\ -(\omega_e - \omega_r) L_m & L_m p & -(\omega_e - \omega_r) L_r & R_r + L_r p \end{bmatrix} \begin{bmatrix} i_{qs}^e \\ i_{ds}^e \\ i_{qr}^e \\ i_{dr}^e \end{bmatrix} \quad (2.39)$$

The instantaneous power in the three-phase and two-phase representation of the machine has to be equal to each other. The power equation in three-phase system is by (2.40).

$$P = V_{as}i_{as} + V_{bs}i_{bs} + V_{cs}i_{cs} \quad (2.40)$$

Applying the inverse of the three-phase to two-phase transformation and writing the a, b, and c axis quantities in terms of q and d axis quantities, the power equation is derived in (2.41) and the electromagnetic torque expression of the machine in two-phase system is given by (2.42) [8].

$$P = \frac{3}{2}(V_{qs}^e i_{qs}^e + V_{ds}^e i_{ds}^e) \quad (2.41)$$

$$T_e = \frac{3P}{2} L_m (i_{qs}^e i_{dr}^e - i_{ds}^e i_{qr}^e) \quad (2.42)$$

The dynamic model equations of the induction machine can also be given in terms of flux linkages, which makes it possible to reduce the number of variables and facilitates the modeling. In addition, the flux linkages are continuous variables, which is not always the case for voltages and currents, and this brings numerical stability during differentiation [8].

The stator and rotor flux linkages in the synchronous reference frames are given in (2.43) to (2.46).

$$\lambda_{qs}^e = L_s i_{qs}^e + L_m i_{qr}^e \quad (2.43)$$

$$\lambda_{ds}^e = L_s i_{ds}^e + L_m i_{dr}^e \quad (2.44)$$

$$\lambda_{qr}^e = L_r i_{qr}^e + L_m i_{qs}^e \quad (2.45)$$

$$\lambda_{dr}^e = L_r i_{dr}^e + L_m i_{ds}^e \quad (2.46)$$

Substituting (2.43), (2.44), (2.45), and (2.46) into to the stator and rotor voltage equations in (2.39), the equations in terms of flux linkages are obtained as in (2.47) to (2.50).

$$V_{qs}^e = R_s i_{qs}^e + \omega_e \lambda_{ds}^e + p \lambda_{qs}^e \quad (2.47)$$

$$V_{ds}^e = R_s i_{ds}^e - \omega_e \lambda_{qs}^e + p \lambda_{ds}^e \quad (2.48)$$

$$V_{qr}^e = R_r i_{qr}^e + (\omega_e - \omega_r) \lambda_{dr}^e + p \lambda_{qr}^e \quad (2.49)$$

$$V_{dr}^e = R_r i_{dr}^e - (\omega_e - \omega_r) \lambda_{qr}^e + p \lambda_{dr}^e \quad (2.50)$$

The torque expression can be written in terms of flux linkages as in (2.51).

$$T_e = \frac{3P}{2} L_m (i_{qs}^e i_{dr}^e - i_{ds}^e i_{qr}^e) = \frac{3P}{2} (i_{qs}^e (L_m i_{dr}^e) - i_{ds}^e (L_m i_{qr}^e)) \quad (2.51)$$

The rotor currents can be eliminated from the equations by writing in terms of stator currents and flux linkages as in (2.52) to (2.54).

$$L_m i_{dr}^e + L_s i_{ds}^e = \lambda_{ds}^e \quad (2.52)$$

$$L_m i_{dr}^e = \lambda_{ds}^e - L_s i_{ds}^e \quad (2.53)$$

$$L_m i_{qr}^e = \lambda_{qs}^e - L_s i_{qs}^e \quad (2.54)$$

Substituting into the torque expression;

$$T_e = \frac{3P}{2} (i_{qs}^e \lambda_{ds}^e - i_{ds}^e \lambda_{qs}^e) \quad (2.55)$$

2.4.6 Indirect Vector Control Method for Induction Machine

To align d axis current vector with the rotor flux linkage phasor, the instantaneous position of the rotor flux linkage phasor θ_e with respect to a stationary axis has to be known. The rotation speed of flux linkage phasor for an induction machine is equal to the sum of electrical rotor speed ω_r and slip speed ω_{sl} . The rotor flux phasor position or field angle θ_e can be found by integrating the synchronous speed which is the sum of the electrical rotor speed ω_r and slip speed ω_{sl} , given by (2.56).

$$\theta_e = \int (\omega_r + \omega_{sl}) dt \quad (2.56)$$

Two types of vector control exist according to the method of obtaining the field angle. The method in which the field angle is calculated by using terminal voltages, hall sensors or flux sensing windings are used is called “direct vector control”. The second method which finds the field angle by summing the rotor electrical angle with slip angle that is derived from machine parameters and motor operating point quantities is called as “indirect vector control”. In this thesis, the indirect vector control method is used and the details are provided for this method only.

The principle of indirect vector control is obtaining the slip angle from the motor parameters and operating points and summing it with the rotor electrical position to find the field angle. To start the derivation of slip angle expression, the rotor voltage equations can be written in terms of flux linkages as in (2.57) and (2.58) where λ_{qr}^e and λ_{dr}^e are given by (2.59) and (2.60).

$$R_r i_{qr}^e + p\lambda_{qr}^e + \omega_{sl}\lambda_{dr}^e = 0 \quad (2.57)$$

$$R_r i_{dr}^e + p\lambda_{dr}^e - \omega_{sl}\lambda_{qr}^e = 0 \quad (2.58)$$

$$\lambda_{qr}^e = L_m i_{qs}^e + L_r i_{qr}^e \quad (2.59)$$

$$\lambda_{dr}^e = L_m i_{ds}^e + L_r i_{dr}^e \quad (2.60)$$

As the resultant rotor flux linkage λ_r is assumed to be aligned with d axis, the component of flux linkage on q axis is zero. Hence;

$$\lambda_r = \lambda_{dr}^e \quad (2.61)$$

$$\lambda_{qr}^e = 0 \quad (2.62)$$

$$p\lambda_{qr}^e = 0 \quad (2.63)$$

Substituting (2.61), (2.62), and (2.63) into rotor voltage equations in (2.57) and (2.58);

$$R_r i_{qr}^e + \omega_{sl}\lambda_r = 0 \quad (2.64)$$

$$R_r i_{dr}^e + p\lambda_r = 0 \quad (2.65)$$

Writing the rotor currents in terms of stator currents drawn from (2.59) and (2.60);

$$i_{qr}^e = -\frac{L_m}{L_r} i_{qs}^e \quad (2.66)$$

$$i_{dr}^e = \frac{\lambda_r}{L_r} - \frac{L_m}{L_r} i_{ds}^e \quad (2.67)$$

Substituting these into the rotor voltage equations again and drawing i_{ds}^e :

$$i_{ds}^e = \frac{1}{L_m} (1 + T_r p) \lambda_r \quad (2.68)$$

$$\omega_{sl} = K_{it} \left(\frac{L_r}{T_r} \right) \left(\frac{T_e}{\lambda_r^2} \right) \quad (2.69)$$

Putting $T_r = L_r/R_r$, rotor time constant, and $K_{it} = 4/(3P)$, slip speed is obtained as;

$$\omega_{sl} = \frac{L_m i_{qs}^e}{T_r \lambda_r} \quad (2.70)$$

Substituting into the torque expression;

$$T_e = \frac{3P}{2} \frac{L_m}{L_r} (i_{qs}^e \lambda_{dr}^e - i_{ds}^e \lambda_{qr}^e) = \frac{3P}{2} \frac{L_m}{L_r} (i_{qs}^e \lambda_r) \quad (2.71)$$

By this derivation, the torque is found to be proportional to the product of rotor flux linkage λ_r and q axis current i_{qs}^e , like a separately excited dc motor. Thus, the torque can be controlled by adjusting q axis current i_{qs}^e if the flux λ_r is kept constant.

2.4.7 Speed Controller Design

The speed controller of the machine has a cascade structure with current regulator at the inner loop and speed regulator at the outer loop. The design of the controller is started by deriving the transfer function of the induction machine in synchronous reference frame.

The first step is to derive a transfer function between the input voltage and current of the machine. To accomplish this, the dynamic equations of the machine are rearranged to obtain a simple block diagram representation using the simplification steps and formulation provided in [8].

Writing the voltage expressions for q and d axes;

$$V_{qs}^e = (R_s + \sigma L_s p) i_{qs}^e + \sigma \omega_e L_s i_{ds}^e + \omega_e \frac{L_m}{L_r} \lambda_r \quad (2.72)$$

$$V_{ds}^e = (R_s + \sigma L_s p) i_{ds}^e - \sigma \omega_e L_s i_{qs}^e + \frac{L_m}{L_r} p \lambda_r \quad (2.73)$$

where $\sigma = 1 - \frac{L_m^2}{L_r L_s}$ is defined as leakage coefficient.

As i_{ds}^e is constant throughout the machine operation, $p i_{ds}^e = 0$. Defining $L_a = \sigma L_s$, and rearranging (2.72);

$$V_{qs}^e = (R_s + L_a p) i_{qs}^e + \omega_e L_a i_{ds}^e + \omega_e \frac{L_m}{L_r} \lambda_r \quad (2.73)$$

Substituting $\lambda_r = L_m i_{ds}^e$;

$$\begin{aligned} V_{qs}^e &= (R_s + L_a p) i_{qs}^e + \omega_e L_a i_{ds}^e + \omega_e \frac{L_m^2}{L_r} i_{ds}^e \\ &= (R_s + L_a p) i_{qs}^e + \omega_e L_s i_{ds}^e \end{aligned} \quad (2.75)$$

Writing the stator electrical frequency as the sum of rotor electrical speed ω_r and slip speed ω_{sl} ;

$$\omega_s = \omega_r + \omega_{sl} = \omega_r + \frac{i_{qs}^e R_r}{i_{ds}^e L_r} \quad (2.76)$$

Putting in (2.74);

$$\begin{aligned} V_{qs}^e &= (R_s + L_a p) i_{qs}^e + \omega_r L_s i_{ds}^e + \omega_{sl} L_s i_{ds}^e \\ &= (R_s + L_a p) i_{qs}^e + \omega_r L_s i_{ds}^e + i_{qs}^e \frac{R_r L_s}{L_r} \\ &= \left(R_s + \frac{R_r L_s}{L_r} + L_a p \right) i_{qs}^e + \omega_r L_s i_{ds}^e \end{aligned} \quad (2.77)$$

Drawing i_{qs}^e from this expression;

$$i_{qs}^e = \frac{V_{qs}^e - \omega_r L_s i_{ds}^e}{R_s + \frac{R_r L_s}{L_r} + L_a p} = \frac{K_a}{1 + s T_a} (V_{qs}^e - \omega_r L_s i_{ds}^e) \quad (2.78)$$

where;

$$R_a = R_s + \frac{L_s}{L_r} R_r \quad (2.79)$$

$$K_a = \frac{1}{R_a} \quad (2.80)$$

$$T_a = \frac{L_a}{R_a} \quad (2.81)$$

The electromagnetic torque constant for the induction machine is then defined by (2.82);

$$K_t = \frac{3P}{2} \frac{L_m^2}{L_r} i_{ds}^e \quad (2.82)$$

$$T_e = K_t i_{qs}^e \quad (2.83)$$

The relation between the electromagnetic torque T_e and the load torque T_l can be expressed by (2.84) where J is the inertia of the motor and load combination and ω_m is the motor mechanical speed. Taking the friction as the load for simple analysis, the transfer function between the mechanical output speed and T_e can be obtained. The block diagram of the machine with q axis voltage V_{qs}^e as input and rotor speed ω_m as output is shown in Figure 2.10.

$$T_e = T_l + J \frac{d\omega_m}{dt} \quad (2.84)$$

$$T_e = b\omega_m + J \frac{d\omega_m}{dt} \quad (2.85)$$

$$\frac{\omega_m(s)}{T_e(s)} = \frac{1}{J_s + B} \quad (2.86)$$

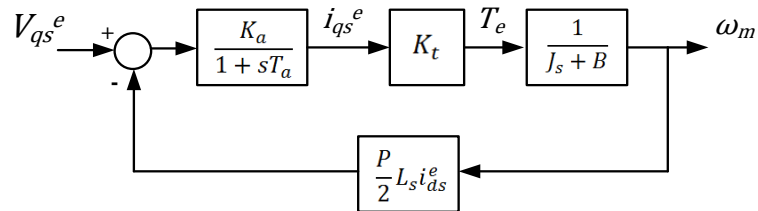


Figure 2.10 Induction machine block diagram.

To simplify the analysis and design of the current controller, the block diagram can be manipulated to obtain a single transfer function between input voltage V_{qs}^e and q axis current i_{qs}^e , as in modified block diagram in Figure 2.11.

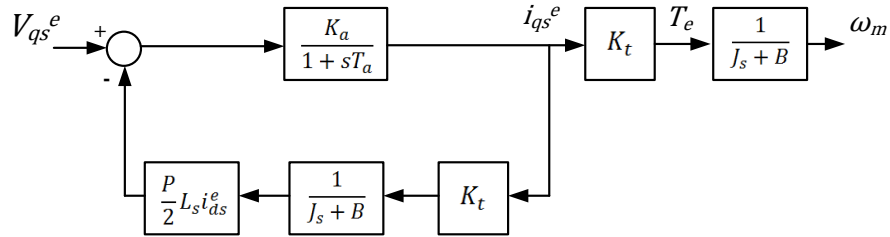


Figure 2.11 Induction machine modified block diagram.

Having derived the motor model, the inverter model is to be found next. Inverter is modeled by a first order transfer function with inverter gain K_{in} and a time delay of half PWM period, $T_c/2$. Hence, it has the transfer function $\frac{K_{in}}{1+s\frac{T_c}{2}}$. K_{in} depends on the modulation method and dc bus voltage of the circuit. Choosing a triangle carrier with peak values between $+V_{dc}/2$ and $-V_{dc}/2$, the inverter output voltage becomes equal to the reference voltage, hence $K_{in}=1$.

Adding the PI compensators for current and speed loops, the complete controller block diagram is obtained. The sensor lags encountered with the measurement of speed and current feedbacks are neglected here and unity feedback paths are used in the model. The complete block diagram of the motor speed controller is shown in Figure 2.12.

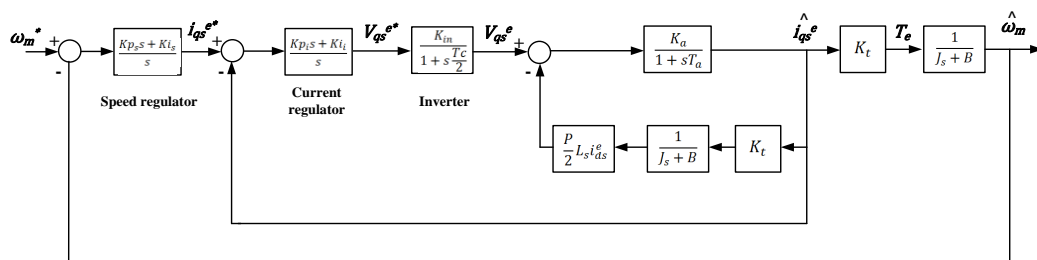


Figure 2.12 Speed controller block diagram for the induction machine.

2.4.7.1 Synchronous Frame Current Regulator Design

Having derived the system model, the regulators can be designed. As a rule of cascade control, first the regulator for the inner current loop is designed. The complex frequency domain (s domain) can be used to design the regulator and the gains can be determined for the desired current loop bandwidth.

The schematic in Figure 2.13 shows the implementation of synchronous frame current regulator (SFCR) [10] in indirect vector control scheme for induction machine. The SFCR regulates the motor current using the synchronous frame d-q axes currents in the compensator. Two PI compensators with proportional gain K_{pi} and integral gain K_{ii} are used to synthesize the reference q and d axis currents i_{qs}^{e*} and i_{ds}^{e*} . The outputs of PI regulators generate the reference voltages V_{qs}^{e*} and V_{ds}^{e*} to be applied to the machine in synchronous reference frame. By using inverse transformations successively from d-q to α - β and α - β to a-b-c axes, stationary frame reference voltages V_{as}^* , V_{bs}^* , and V_{cs}^* are obtained. The reference voltages are used in the PWM modulator of the voltage source inverter (VSI) to drive the machine.

The dynamic response of the current controller can be improved by the addition of feed-forward terms. As realized in (2.47) and (2.48), the q axis voltage expression has voltage terms including d axis parameters and likewise d axis voltage expression include voltage terms from q axis. Thus, the voltage expressions of the two axes are coupled to each other. Due to this fact, the q (d) axis voltage reference signal generated by q (d) axis current regulator has to include the coupling term for d (q) axis voltage in addition to q (d) axis voltage. Instead, the coupling terms can be added externally to the output of the current regulators to decouple the d and q axes voltage reference signals completely. With this structure, the q axis current regulator generates the voltage reference for only q axis and so does the d axis current regulator. The feedforward terms that have to be added to the q and d axes are given by (2.87) and (2.88) respectively [11].

$$V_{qsff}^{e*} = \sigma\omega_e L_s i_{ds}^e + \omega_e \frac{L_m}{L_r} \lambda_r \quad (2.87)$$

$$V_{dsff}^{e*} = -\sigma\omega_e L_s i_{qs}^e + \frac{L_m}{L_r} p\lambda_r \quad (2.88)$$

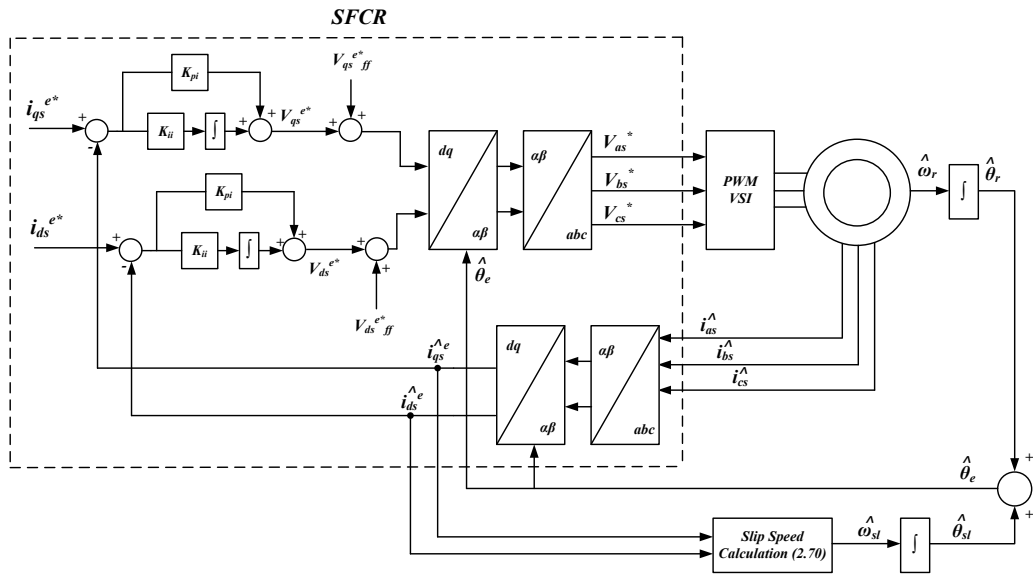


Figure 2.13 Schematic for the use of synchronous frame current regulator in indirect vector control.

The regulators are implemented very often by using DSPs or FPGAs digitally, in discrete domain. Hence the controllers are operated by a definite sample rate. Due to discrete time operation, the maximum available current regulator bandwidth is lower than obtained in the continuous time domain. In addition, the PWM operation also limits the maximum available theoretical current regulator bandwidth to a fraction of switching frequency. Hence, by using high sample rates and high switching frequency, the available current regulator bandwidth can be increased. For triangular carrier based PWM generators (details are given in Chapter 3), the maximum current regulator bandwidth is obtained by adopting double sample per carrier approach. In this method, the current feedback is taken at every peak and valley of the triangle, thus the current control law is applied at the peak and valley instants. The current controller output (the voltage reference) corresponding to a sample taken at a valley (peak) is applied at the next peak (valley). Thus, the current controller output is applied with a half PWM period delay. With this controller sampling strategy, the maximum available current regulator bandwidth becomes nearly 1/10 of PWM switching frequency f_c .

2.4.7.2 Speed Regulator Design

The speed regulator constitutes the outer loop and generates the torque current reference i_{qs}^{e*} . The d axis field current reference i_{ds}^{e*} is commanded separately for desired flux. Figure 2.14 shows the schematic of the speed regulator cascaded with current regulator.

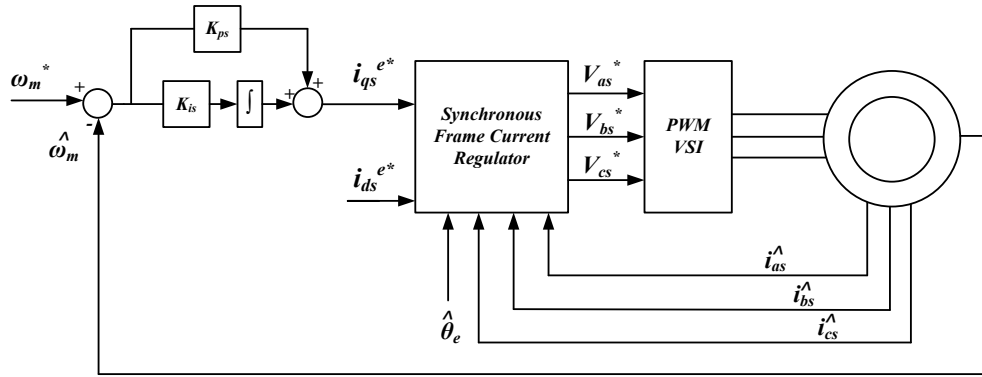


Figure 2.14 Speed regulator of the induction machine.

The speed regulator is designed by PI compensator with proportional gain K_{ps} and integral gain K_{is} , which can be selected for the desired regulator bandwidth and minimum steady state error.

The speed regulators are generally equipped with anti wind-up controller to prevent a possible wind-up in the integrator of the controller. There are various anti wind-up controller structures offering slight differences in behavior. The anti wind-up controller shown in Figure 2.15 is used for the speed regulator in the thesis. It includes a limiter at the regulator output and manipulates the error entering into the integrator by scaling the difference between the limiter input and output by a scaling constant K_b . K_b constant is generally selected as $1/K_{ps}$, however, by choosing it between $K_{ps}/3$ to $3K_{ps}$ the performance of the anti wind-up controller can be enhanced [12]. Another addition to speed regulator is the speed rate of change limiter (ROCL). By limiting the rate of change of speed reference, the machine is prevented from acceleration in an uncontrolled manner. By ROCL, the speed reference is applied to the motor with a ramp shape of fixed slope, creating constant acceleration. As a result, by adjusting the acceleration $\frac{d\omega}{dt}$ of the motor, the torque $J \frac{d\omega}{dt}$

sourcing from the acceleration of the inertia of the motor-load combination can be controlled to prevent the motor from drawing over current. The ROCL constant K is set for the desired acceleration profile of the motor. Figure 2.16 shows the speed regulator with rate of change limiter [13] and anti wind-up controller [12] structures.

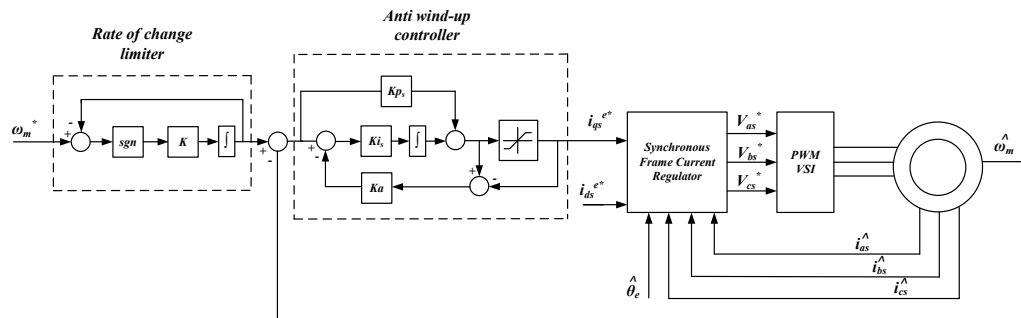


Figure 2.15 Speed regulator with rate of change limiter and anti wind-up controller.

2.5 Conclusion

In this chapter, the characteristics of the motor load types and three-phase ac machine control methods are reviewed. Vector control of the induction machine and controller design in synchronous reference frame is explained in detail. In the next chapter, the design of conventional motor drive circuit with front end diode rectifier is provided.

CHAPTER 3

CONVENTIONAL DIODE RECTIFIER FRONT END MOTOR DRIVE SYSTEM REVIEW

3.1 Three-phase Diode Rectifiers

Due to their high efficiency, low cost, and simple implementation, diode rectifiers are widely used in industrial applications. In motor drives fed by ac grid, diode rectifiers are used to create the dc link voltage to feed the voltage source inverter. This section introduces the operating characteristics of ideal three-phase diode rectifiers, the practical diode rectifier circuit design and the components used with them, together with an evaluation of circuit performance. All the simulations in the thesis are conducted by Ansoft Simplorer, V7.0 simulation software [14].

3.1.1 Ideal Three-phase Diode Rectifier

Figure 3.1 illustrates the schematic of a three-phase diode rectifier. In the schematic, v_s is the ac grid line to neutral voltage and v_{dc_r} is the output voltage of the rectifier. The load can be any type such as constant current, constant impedance, or constant power load.

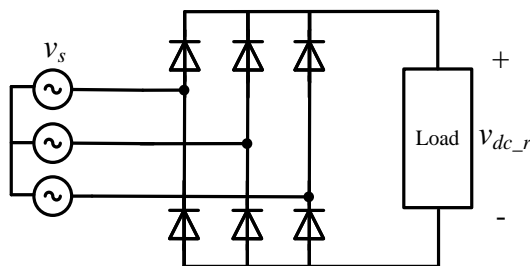


Figure 3.1 Three-phase diode rectifier circuit.

3.1.1.1 Principle of Operation

The three-phase diode rectifier operates by line commutation principle. Each diode in the upper (lower) side of the circuit has 120° conduction angle with two other diodes on the lower (upper) side of the rectifier. The commutation sequence between the diodes is determined by the magnitude of the line to neutral voltage seen by the diodes. The upper side diode facing the highest line to neutral voltage and lower side diode facing the minimum line to neutral voltage are favored and start conduction. Hence, in a line frequency period $T_{eg}=1/f_{eg}$, the peak line to line voltage portions are seen at the output of the rectifier, creating a six-pulse dc voltage waveform.

The performance of a diode rectifier can be measured by analyzing the dc bus voltage characteristics and input power quality.

3.1.1.2 DC Bus Voltage Characteristics

The dc bus voltage of an ideal three-phase diode rectifier without dc bus capacitor has ripple at the frequency of $6f_{eg}$ and its multiples, with f_{eg} being the grid voltage frequency. Thus, an ideal three phase diode rectifier generates dominantly 300 Hz bus voltage ripple at 50 Hz grid voltage frequency. Figure 3.2 illustrates the dc bus voltage of a 2.2 kW ideal three-phase diode rectifier. In the circuit, a 4.28 A constant current source is used as a load.

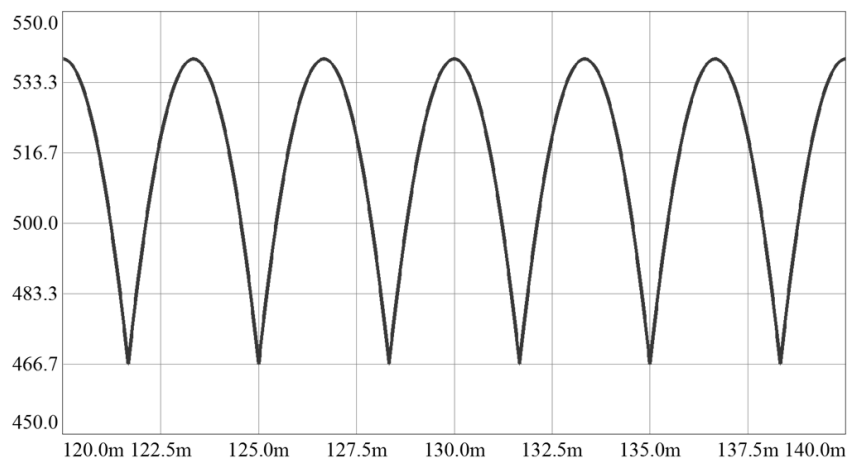


Figure 3.2 DC bus voltage of the 2.2 kW ideal three phase diode rectifier fed by 220 V (l-n)/50 Hz ac grid (16.6 V/div, 2.5 ms/div).

The average output voltage of the rectifier $V_{dc_r_avg}$ is given by (3.1).

$$V_{dc_r_avg} = \frac{3\sqrt{3}V_{g_peak}}{\pi} \quad (3.1)$$

In (3.1), V_{g_peak} represents the peak line-to-neutral grid voltage. Using (3.1) the average dc bus voltage is calculated approximately 514 V for 220 V (l-n rms) / 50 Hz grid voltage. The peak to peak voltage ripple V_{pp} on the dc bus can be calculated by subtracting the minimum line to line voltage at the end of a 60° period from the peak line to line voltage, by (3.2).

$$V_{pp} = 3\sqrt{3}v_{g_peak} - (3\sqrt{3}v_{g_peak} * \cos\left(\frac{\pi}{6}\right)) \quad (3.2)$$

Using (3.2) the pp voltage ripple on dc bus is found as 71.5 V

The six-pulse dc bus voltage ripple is expected to contain harmonics of $6f_{eg}$ frequency and its multiples. Figure 3.3 illustrates the harmonic spectrum corresponding dc bus voltage of ideal three phase diode rectifier fed by 220 V/ 50 Hz grid.

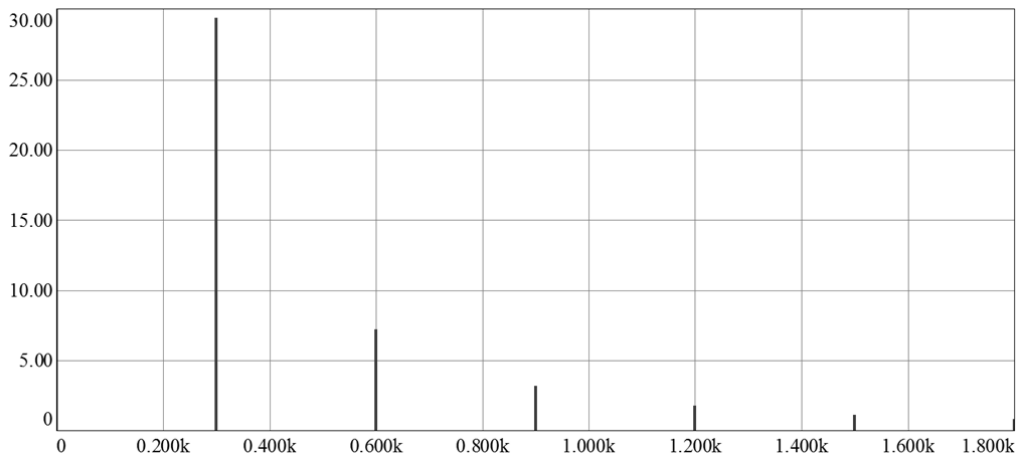


Figure 3.3 Harmonic spectrum of the three phase diode rectifier dc bus voltage (5 V/div, 200 Hz/div).

The dc bus voltage can also be written in terms of its harmonics analytically by (3.3) [15].

$$v_{dc} = v_{dc_avg} \cdot \left[1 - \sum_{n=1}^{\infty} \frac{2}{(6n)^2 - 1} \cos(6n\omega_{eg}t) \right] \quad (3.3)$$

3.1.1.3 Input Power Quality Characteristics

The input power quality of a three phase diode rectifier can be analyzed by investigating the ac line current distortion and input power factor.

3.1.1.3.1 Line Current Distortion

The ac line current drawn by a circuit is always desired to have a waveform as close as possible to a sinusoidal. This is because a distorted line current waveform contains harmonics which do not contribute to real power drawn by the load and cause power loss in the distribution system. In addition, the harmonics can easily affect the other loads connected to the same point of coupling and may cause resonances. So, the line current harmonic distortion is an important performance figure to be considered.

A diode rectifier draws $(n.k \pm 1)$ line current harmonics from the grid, where n is the pulse number of dc bus voltage in one grid voltage period and $k=1,2,3,\dots$. Thus, for a three phase rectifier, $n=6$ and the rectifier draws 5^{th} , 7^{th} , 11^{th} , $13^{th}, \dots$ harmonics from the grid. The relation between the harmonic component of the line current and the fundamental component is given by (3.4), where i_{1g} is the fundamental and i_{hg} is the h^{th} harmonic component of the line current.

$$i_{hg} = \frac{i_{1g}}{h} \quad (3.4)$$

Figure 3.4 illustrates the line current of a 2.2 kW ideal three-phase diode rectifier with a constant current load. It is realized that the line current of an ideal rectifier feeding an ideal current source has rectangular wave shape.

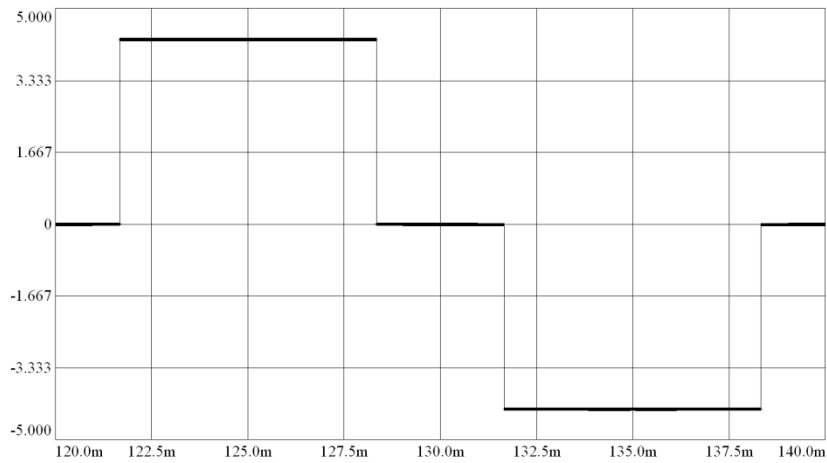


Figure 3.4 Line current of the 2.2 kW ideal three-phase diode rectifier (1.67 A/div, 2.5 ms/div).

Figure 3.5 shows the line current harmonic spectrum for the line current in Figure 3.4. It is seen that the harmonic components with considerable amplitude (compared with the fundamental component of line current) extends up to 13th one.

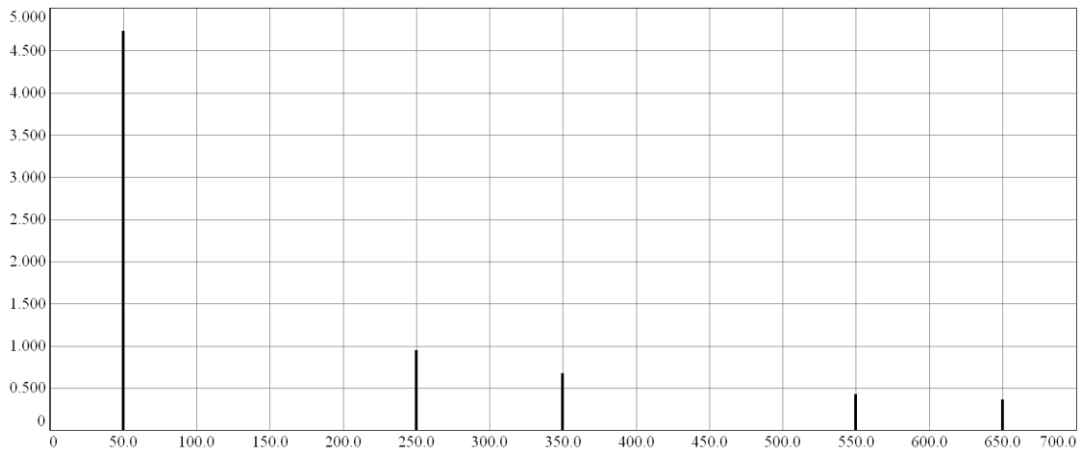


Figure 3.5 Line current harmonic spectrum of the 2.2 kW ideal three-phase diode rectifier (0.5 A/div, 50 Hz/div).

THD_{ig} of a three phase ideal diode rectifier with constant current load is calculated as 31.08 % by (3.5) and verified by the simulations.

3.1.1.3.2 Input Power Factor

The ideal three-phase diode rectifier drawing rectangular current from the ac mains has $PF=0.955$ by (1.4). Figure 3.6 shows the ac mains line to neutral voltage and line current waveform.

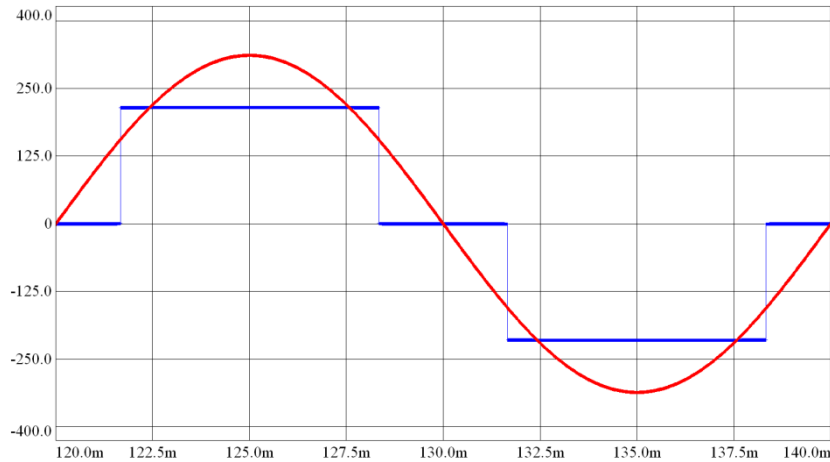


Figure 3.6 Line to neutral ac mains voltage (red, 125 V/div, 2.5 ms/div) and 20*line current (blue, 125 A/div, 2.5 ms/div) of the 2.2 kW ideal three-phase diode rectifier.

3.1.2 Practical Three-phase Diode Rectifiers

The six-pulse voltage at the output of the ideal three phase diode rectifier contains large voltage ripple. In practical use, the dc bus is desired to have ripple voltage as low as possible and it is minimized by the use of a high C_{dc} capacitor at the dc bus.

Due to high C_{dc} dc bus capacitor usage, however, THD_{ig} increases and the filtering of the line current becomes necessary, details of which will be given the upcoming sections. This situation dictates the use of ac line reactors and dc link inductors for filtering the line current harmonics.

The high capacitance at the dc bus causes the capacitor draw very large inrush currents, which makes it necessary to use precharge circuits (or inrush current limiters) to prevent a possible damage caused by large currents. This section includes the brief description of components used with practical three phase diode rectifiers and their effects on the rectifier

input and output performance. Figure 3.7 shows the practical three phase diode rectifier circuit with inductor filters installed on ac and dc side. In practice, the ac grid has line inductance and resistance and they are also included in the circuit schematics. In Figure 3.7; C_{dc} represents the dc bus capacitor, L_g shows the line inductance per phase, R_g is used to show the line resistance per phase and L_{ac} illustrates the ac line reactor filter per phase, and L_{dc} is the dc link inductor filter. The circuit also includes the precharge circuit.

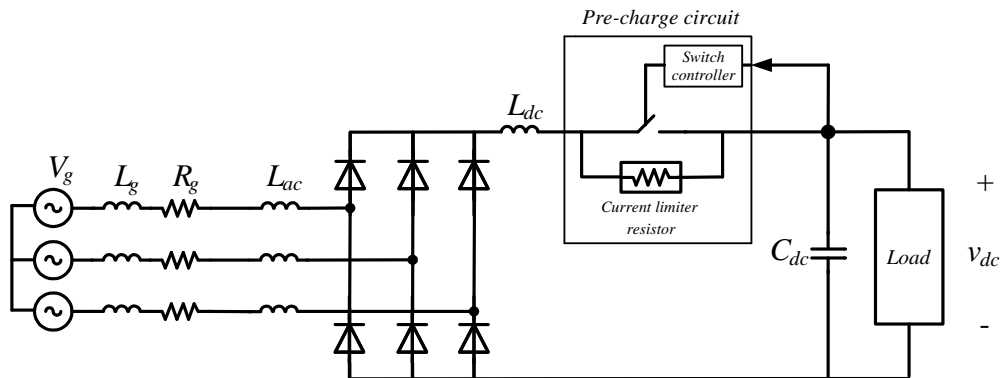


Figure 3.7 Practical three phase diode rectifier with line impedance, ac and dc filter inductors, precharge circuit, and dc bus capacitor.

3.1.2.1 Components Used in Practical Diode Rectifiers

This section describes the physical and operational features of the components used in practical three phase diode rectifiers, such as the dc bus capacitors, the filter inductors, and the precharge circuit.

3.1.2.1.1 DC Bus Capacitor

The large ripple on the dc bus voltage of the three phase diode rectifiers is minimized conventionally by using high C_{dc} dc bus capacitors. In addition, due to its high energy storage capability the capacitor creates a stiff dc bus voltage and prevents the sudden changes of bus voltage due to variations in ac line voltage and load.

Conventionally, the selection of the dc bus capacitance is done by using a capacitance/load power ratio, which may slightly vary from designer to designer. As an example, [16] uses 1

mF/5.5 kW ratio to calculate the required capacitance. A more analytical approach can be used to calculate the capacitance by considering the desired voltage ripple on the bus. This is given in [17], where the required capacitance is calculated by (3.6) to obtain the desired voltage ripple. In (3.6), C_{dc} is the required bus capacitance, P_{load} is the load power, V_{g_rms} is the line to neutral rms ac mains voltage. This formulation assumes the usage of a 4% ac line reactor and 4% dc link inductor filters.

$$C_{dc} = \frac{P_{load}}{[240*v_{pp}*V_{g_rms}*f_{eg}]} \quad (3.6)$$

Two types of capacitors are widely used in power electronic circuits namely; electrolytic and film capacitors.

An aluminum electrolytic capacitor consists of a wound capacitor element, impregnated with liquid electrolyte, connected to terminals and sealed in a can [18]. Etching the foils creates a very large plate area and hence a high capacitance is created in a small volume. The electrolytic capacitors are polar devices and are connected to the circuit accordingly with their polarities.

The equivalent circuit of an electrolytic capacitor consists of equivalent series resistance (R_{cs}), equivalent parallel resistance (R_{cp}), equivalent series inductance (L_{cs}), and a zener diode (D) parallel to the equivalent capacitance (C) of the capacitor, in which the R_{cp} is responsible for leakage currents in the capacitor and the zener diode models the reverse voltage and overvoltage behavior [18], as shown in Figure 3.8.

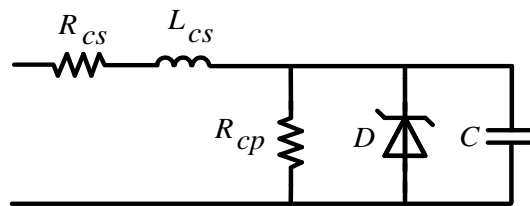


Figure 3.8 Equivalent circuit of the electrolytic capacitor.

Figure 3.9 shows a typical ESR-temperature and ESR-frequency graphic for a typical electrolytic capacitor. It is seen in figure that the ESR of an electrolytic capacitor decreases

with increasing temperature and frequency. The variation of ESR with temperature and frequency directly affects the current rating of the capacitor at the operating point. So, the ripple current ratings for different operating points are given by frequency and temperature multipliers, defining the ratios of current ratings to a base rating at a selected temperature and frequency.

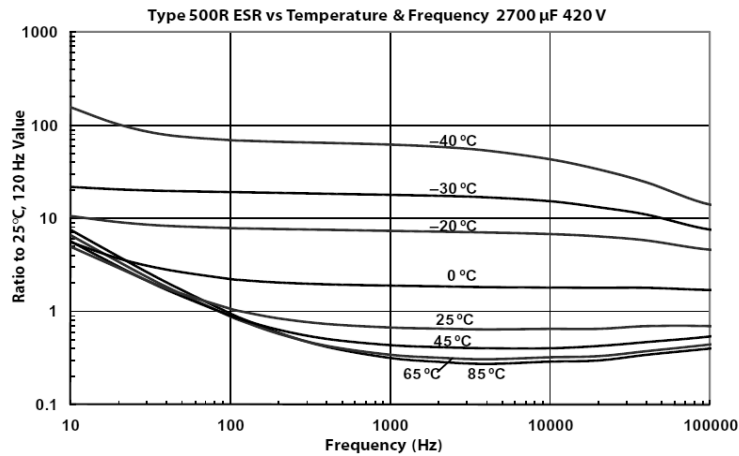


Figure 3.9 Variation of ESR with operating temperature and frequency for a typical electrolytic capacitor [19].

The ESR of an electrolytic capacitor increases with operating voltage and the rms ripple current rating decreases. For this reason, their maximum operating voltage is limited to 500-600 V [20]. Generally they are used in form of capacitor banks connected in series. Figure 3.10 shows the ratings of a typical electrolytic capacitor with highest voltage rating of available 550 V.

Cap. (µF)	Catalog Part Number	ESR Max. @ 25 °C 120 Hz (mΩ)	Ripple Max. @ 85°C 120 Hz (A)	Nominal Size D x L (inches)
550 Vdc (600 Vdc Surge)				
1400	DCMC142T550CC2B	170.5	4.9	2 1/2 x 4 1/8
1700	DCMC172T550CD2B	132.6	5.9	2 1/2 x 4 5/8
1900	DCMC192T550CE2B	111.7	6.8	2 1/2 x 5 1/8
2200	DCMC222T550DC2B	90.4	7.8	3 x 4 1/8
2300	DCMC232T550CF2B	86.5	7.8	2 1/2 x 5 5/8
2500	DCMC252T550DD2B	79.6	8.4	3 x 4 5/8
2900	DCMC292T550DE2B	64.0	9.7	3 x 5 1/8
3400	DCMC342T550DF2B	54.6	10.9	3 x 5 5/8
3700	DCMC372T550DP2B	50.2	12.2	3 x 5 7/8
5100	DCMC512T550DN2B	36.4	16.2	3 x 7 5/8

Figure 3.10 Ratings of typical electrolytic capacitors taken from the manufacturer datasheet [21].

Due to increased ESR at high voltages, the available rms current rating of an electrolytic capacitor cannot exceed 20 mA/ μ F at highest possible operating voltage [20]. Another important point to stress about electrolytic capacitors is the variation of capacitance with operating temperature and frequency. Figure 3.11 illustrates the capacitance-temperature and capacitance-frequency variation of the same capacitor in Figure 3.9. It is seen that the capacitance of an electrolytic capacitor has considerable dependence on operating temperature.

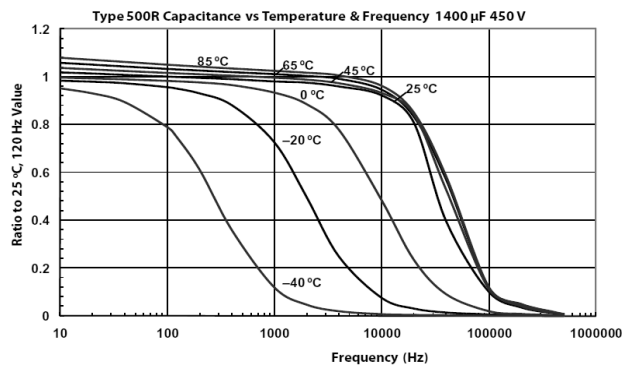


Figure 3.11 Variation of capacitance with operating temperature and frequency for a typical electrolytic capacitor [19].

The film capacitors are built up by two electrodes (the capacitor plates) with plastic dielectric material in between [22]. According to the electrode used, they are classified as metallized film or film/foil type and according to dielectric used, polypropylene and polyester film capacitors are available in the market.

Metallized capacitors use a thin layer of vapor deposited aluminum, zinc or alloy (aluminum/zinc) blend as the electrode system. A fault in the dielectric of the metallized capacitor vaporizes the metal deposit in the fault area known as clearing process [18]. This feature of the capacitor is called self healing. Clearing decreases the capacitance due to fault but the capacitor continues operating without any problem.

Film/foil capacitors are made of aluminum foil electrode. The foil type electrode decreases the ESR of the capacitor and this enables the capacitor to carry high rms current ratings and handle large peak currents. Foil type electrode also results in a small size capacitor so, these capacitors are appropriate for the circuits where low volume and high current rated

capacitors are needed. Their main disadvantage is that they do not have self healing feature and their energy density is lower than metallized types.

In addition to ESR, the current rating or power loss mechanism of film capacitors also depend on their dissipation factor (DF) values. Dissipation factor is defined as the ratio of ESR to the capacitive reactance X_c (3.7).

$$DF = \frac{ESR}{X_c} \quad (3.7)$$

DF of film capacitors increases with temperature and frequency and becomes an effective loss parameter at high temperature and frequency operation.

Figure 3.12 shows the ratings of a typical film capacitor series [23]. From datasheet it can be deduced that film capacitors have very low ESR values compared with electrolytic capacitors and they offer high current ratings at high operating voltages.

Catalog Part Number	Cap (μF)	Rated Voltage (Vdc)	H Height mm	100kHz ESR (mΩ)	dV/dt (V/μs)	Max Irms 10 kHz 50 °C (A)
945U221K601DBI	220	600	80.2	4.0	30	47.0
945U301K601DCI	300	600	105.2	4.5	25	46.0
945U401K601DEI	400	600	131.2	5.0	26	44.0
945U501K601DMI	500	600	156.2	6.0	22	43.0
945U141K751DBI	140	750	80.2	4.5	30	44.0
945U191K751DCI	190	750	105.2	5.0	25	43.0
945U251K751DEI	250	750	131.2	6.0	37	42.0
945U321K751DMI	320	750	156.2	6.5	30	41.0
945U900K901DBI	90	900	80.2	5.0	42	42.0
945U131K901DCI	130	900	105.2	5.5	35	41.0
945U171K901DEI	170	900	131.2	6.5	43	40.0
945U221K901DMI	220	900	156.2	7.5	36	38.0
945U650K102DBI	65	1000	80.2	5.5	50	40.0
945U950K102DCI	95	1000	105.2	6.0	40	39.0
945U131K102DEI	130	1000	131.2	7.0	60	38.0
945U161K102DMI	160	1000	156.2	8.0	50	37.0

Figure 3.12 Ratings of a typical film capacitor taken from the manufacturer datasheet [23].

The basic characteristics of electrolytic and film capacitors can be summarized as in Table 3.1.

Table 3.1 Basic characteristics of electrolytic and film capacitors.

Rating and operation characteristics	Electrolytic capacitor	Film capacitor
Maximum operating voltage	< 1000 V	>> 1000 V
Maximum operating current	~20 mA/ μ F	~1 A/ μ F
Capacitance/volume	Very high	Low
ESR	High	Very low
Parameter variation with temperature and frequency	Generally high	Generally low
Self healing feature	No	Yes
Lifetime	~5-10 years	~ 20 years

3.1.2.1.2 Filter Inductor

Using a dc bus capacitor degrades the line current performance of a diode rectifier since it disturbs the continuity of the line current. This is because the high C_{dc} capacitor keeps the dc bus voltage higher than the line-to-line grid voltage during a large portion of the $1/(6f_{eg})$ period and shortens the durations of time during which the current is drawn from the grid to the dc side. As a result, the continuity of the line current and dc link current is decreased and the THD_{ig} increases even above 100 %.

There are various harmonic filtering methods used with rectifiers including passive filters (line reactors and/or dc link chokes, series, shunt, and low pass broadband filters), phase multiplication systems (12-pulse, 18-pulse rectifier systems), active harmonic compensation systems (series, parallel), and hybrid connection of passive and active filters [16]. Among these methods, the series passive filtering by ac line reactors and dc link inductors find wide usage in many of the industrial rectifier systems due to sufficient harmonic reduction performance, satisfying the quality standards, and easy implementation. The inductor is basically a low pass filter blocking the high frequency harmonics on the line current. The methods for choosing the filter inductances may vary between designers. A widely used convention is choosing the inductance according to the voltage drop it will cause during operation. Typically 1% to 5% ac line reactors are used

[24]. Around European regions 4 % inductances are common whereas in USA 3 % is generally used [16].

3.1.2.1.3 Precharge Circuit

A capacitor with large capacitance draws high current when it is energized called inrush current. A high inrush current can easily damage the capacitor itself, also the other elements in the circuit. Figure 3.13 shows the inrush current and capacitor voltage of a 2.2 kW three-phase diode rectifier fed by 220 V/50 Hz grid and utilized with a 0.4 mF capacitor. In simulation, $R_g=125\text{ m}\Omega$ and $L_g=250\text{ }\mu\text{H}$.

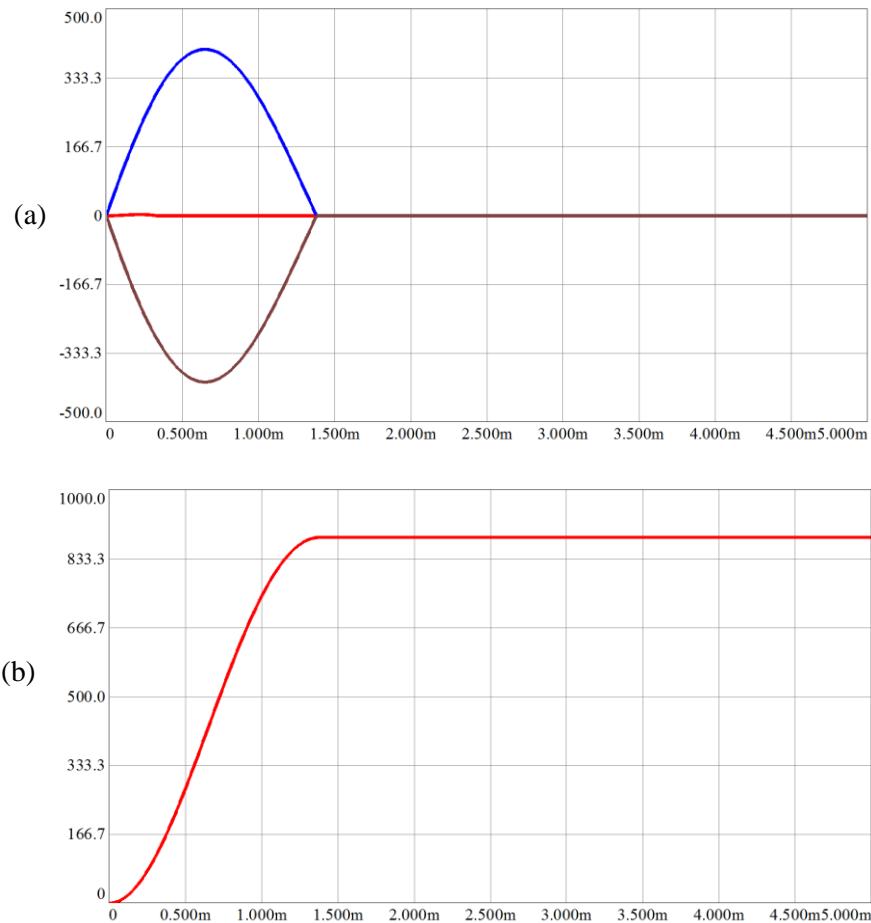


Figure 3.13 (a) Inrush currents (167 A/div, 0.5 ms/div) phase-a (red), phase-b (blue), phase-c (green), (b) capacitor voltage (167 V/div, 0.5 ms/div) of 2.2 kW three phase rectifier with 0.4 mF dc link capacitor.

For a three-phase rectifier fed by 220V grid, the expected average dc link voltage is nearly 514 V but due to inrush current, the capacitor voltage increases instantly to higher levels as seen in Figure 3.13. The magnitude of inrush currents is close to 400 A.

To prevent the damage due to high inrush currents, the high C_{dc} capacitors are used with precharge circuits, also called inrush current limiters. The purpose in using the precharge circuit is to charge the capacitor to a pre-specified voltage level by limiting the inrush current. After that, the precharge circuit is bypassed and the capacitor starts to operate with the remaining of the circuit. In many applications the pre-charge circuit is implemented by use of thermistors which are resistors that have resistances varying with temperature. The one whose resistance decreases with the increasing operating temperature is called negative temperature coefficient (NTC) thermistors, while the one whose resistance increases with increasing operating temperature is called positive temperature coefficient thermistors (PTC). NTC thermistors are used to limit the inrush current and enables a safe start-up, while the PTC types prevents the damage due to excessive continuous currents or short circuit faults by increasing the resistance and lowering the current [25]. A more complex precharge circuit can be made by a current limiting resistor and control switch combination, illustrated symbolically in Figure 3.14. The resistor limits the inrush current and the switch is closed after the charging of the capacitor to the desired voltage is complete, which usually takes under 1 second [26]. In practice, the capacitor is generally charged up to 80-90% of the steady state voltage and the switch is closed.

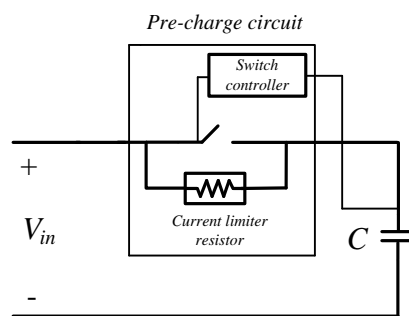


Figure 3.14 Precharge circuit with current limiter resistor and control switch.

Figure 3.15 shows the results of an inrush current limiter simulation conducted for the same 2.2 kW rectifier. The current limiter resistor selected as 200Ω draws nearly 2.5 A peak current. When the capacitor voltage increases approximately to 80 % of the steady state value of 550 V, the switch controller closes the switch and bypassed the current limiter resistor. In approximately 175 ms, the capacitor voltage reaches the pre-set value when the switch is programmed to be closed. When it is closed, the capacitor voltage shows a sudden increase and settles down to the steady state value at nearly 550 V.

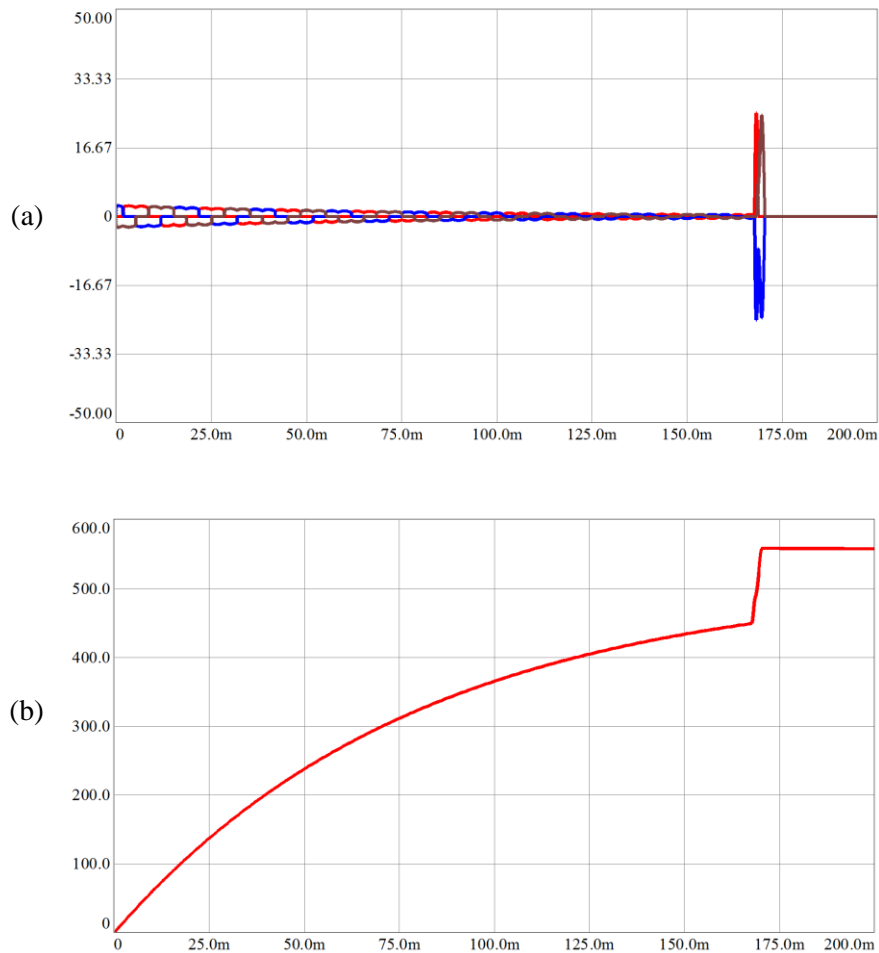


Figure 3.15 (a) Inrush currents phase-a (red), phase-b (blue), phase-c (green) (16.7 A/div, 25 ms/div), (b) capacitor voltage (100 V/div, 25 ms/div) of 2.2 kW three phase diode rectifier with 0.4 mF dc link capacitor utilizing inrush current limiter.

Figure 3.16 illustrates the current waveforms through switch and the limiter resistor of the inrush current limiter. The limiter resistor keeps the current at an acceptable value and suddenly transfers it to the switch when it is closed. By this operation, both the capacitor voltage is prevented from an uncontrolled increase and the inrush current is limited.

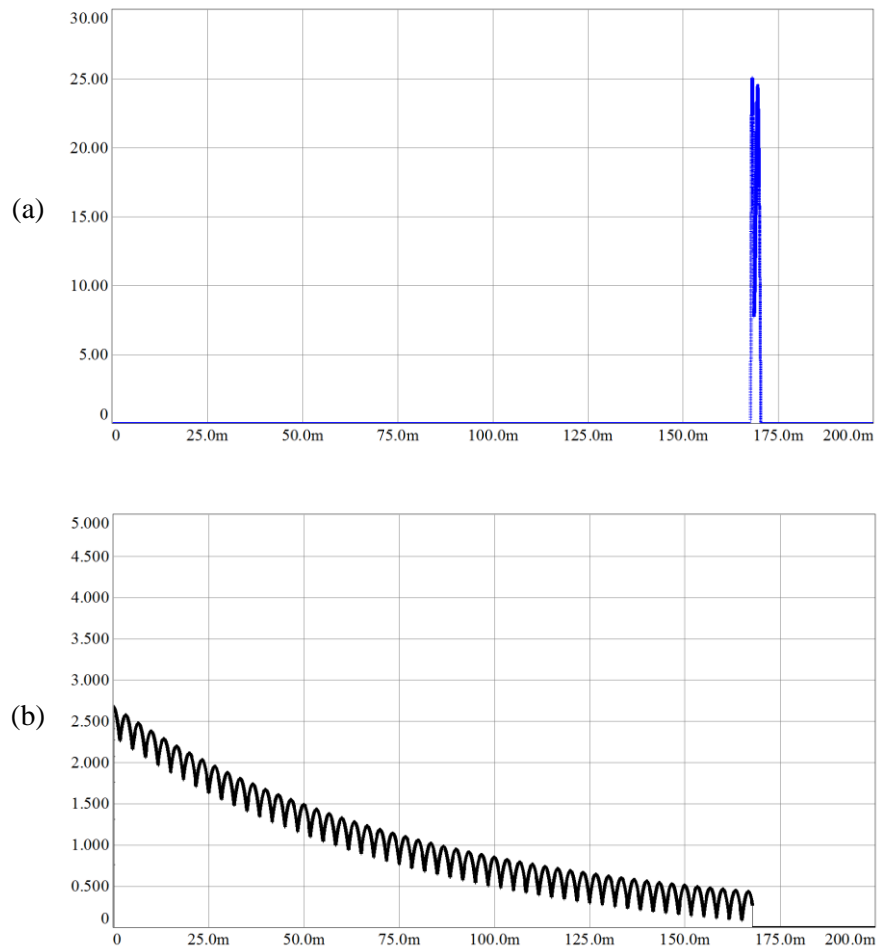


Figure 3.16 (a) Switch current (blue) (5 A/div, 25 ms/div), (b) current limiter resistor current (black) (0.5 A/div, 25 ms/div).

3.1.2.2 Performance Analysis of Practical Three Phase Diode Rectifiers

This section includes the analysis of input power quality and output voltage characteristics of the practical three phase diode rectifiers. A 2.2 kW three phase diode rectifier is used for

analysis. To show the improvement on the input power and dc bus voltage quality brought by the use of the filter inductors, the line current and bus voltage for rectifier with and without filters are provided. First, the input power quality of the circuit with the filter inductor is investigated. Then, the dc bus voltage quality of the practical rectifier is analyzed. Table 3.2 includes the rectifier circuit parameters used in simulations.

Table 3.2 Circuit parameters of the 2.2 kW three-phase diode rectifier

Parameter	2.2 kW three-phase diode rectifier
Line voltage (l-n)	220 V (rms)
Line frequency (Hz)	50
Line inductance, L_g (mH)	0.25
Line resistance, R_g (m Ω)	125.0
AC line reactor, L_{ac} (mH)	7.75
DC link inductor, L_{dc} (mH)	7.75
DC bus capacitor, C_{dc} (mF)	0.4

3.1.2.2.1 Input Power Quality

The input power quality of the practical diode rectifier can be analyzed by investigation of line current quality and input power factor, as done before for the ideal rectifier.

3.1.2.2.1.1 Line Current Quality

The line current waveform of a practical rectifier is improved by use of ac line reactors and dc link inductors. The line current waveform obtained from the simulation of the rectifier with no inductor filter is given in Figure 3.17 and the corresponding harmonic spectrum is provided in Figure 3.18. The THD_{ig} obtained from the simulation of the rectifier with no inductor filter is 172 %, very high as expected and clearly understood from the high level of harmonics in Figure 3.18. The PF obtained from the simulation is 0.5, very low due to large distortion in the line current.

With the use of inductor filters, THD_{ig} of the circuit decreased to 31.2 % as clearly seen in the decreased current harmonic levels in Figure 3.20, compared to Figure 3.18.

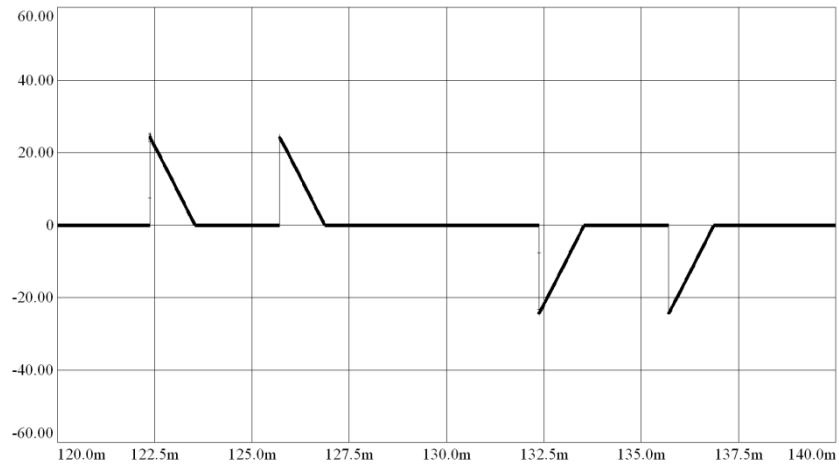


Figure 3.17 Line current of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor and no inductor filter (20 A/div, 2.5 ms/div).

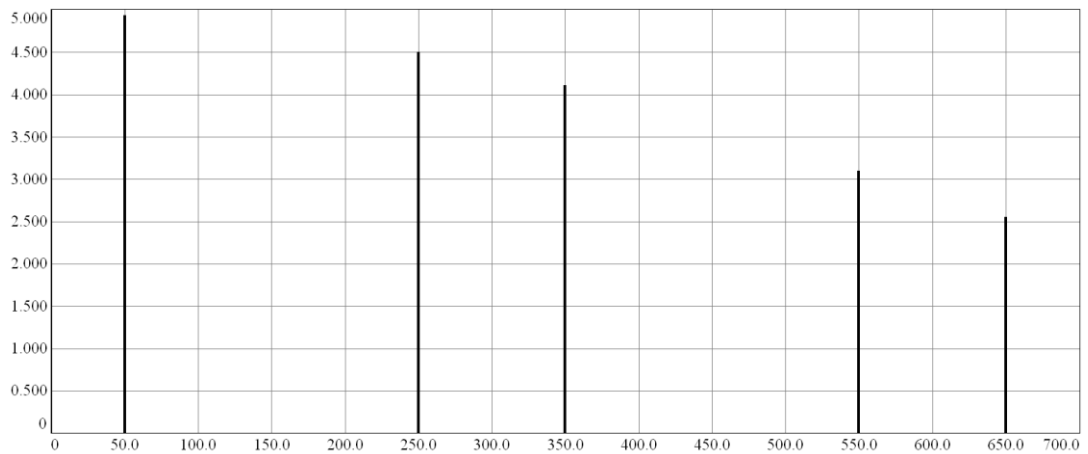


Figure 3.18 Line current harmonic spectrum of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor and no inductor filter (0.5 A/div, 50 Hz/div).

Figure 3.19 and Figure 3.20 show the line current waveform and the corresponding harmonic spectrum of the rectifier with 4% ac line reactors and 4% dc link inductor respectively. The simulation also included the METU local campus distribution transformer line impedance values taken from [16].

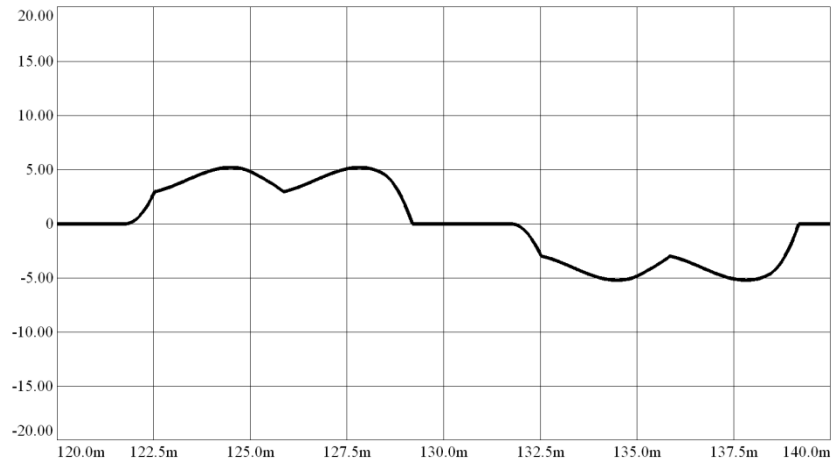


Figure 3.19 Line current of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor, 4% ac line reactor and 4% dc link inductor (5 A/div, 2.5 ms/div).

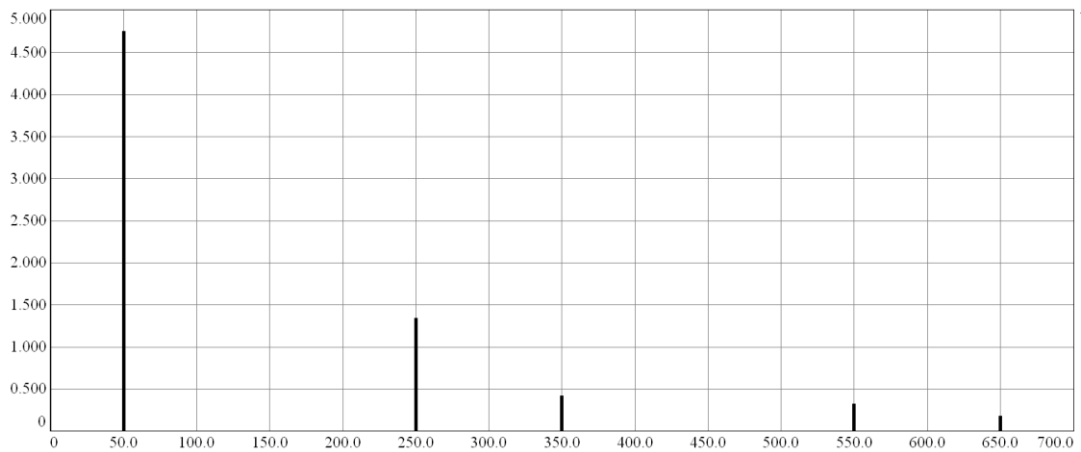


Figure 3.20 Line current harmonic spectrum of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor, 4% ac line reactor and 4% dc link inductor (0.5 A/div, 50 Hz/div).

3.1.2.2.1.2 Input Power Factor

The distorted line current waveform due to high C_{dc} is improved significantly with the use of inductor filters. With 4% ac line reactors and 4% dc link inductor installed on the rectifier circuit, the THD_{ig} and distortion factor is reduced, and the input power factor increases to 0.93.

3.1.2.2.2 DC Bus Voltage Quality

The capacitor voltage ripple depends on the harmonic components of the link current. Since the dc link current of the rectifier equipped with filter inductors contains reduced harmonics, the dc bus voltage ripple is also expected to be lower than non-filtered case. Figure 3.21 shows the dc bus voltage waveform of the rectifier with 0.4 mF capacitor and no filter inductors. Figure 3.22 shows the corresponding bus voltage harmonics.

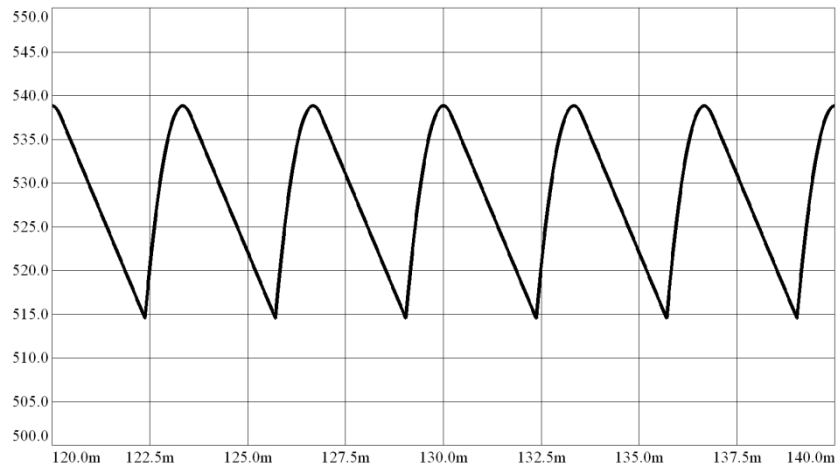


Figure 3.21 DC bus voltage of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor and without filter inductors (5 V/div, 2.5 ms/div).

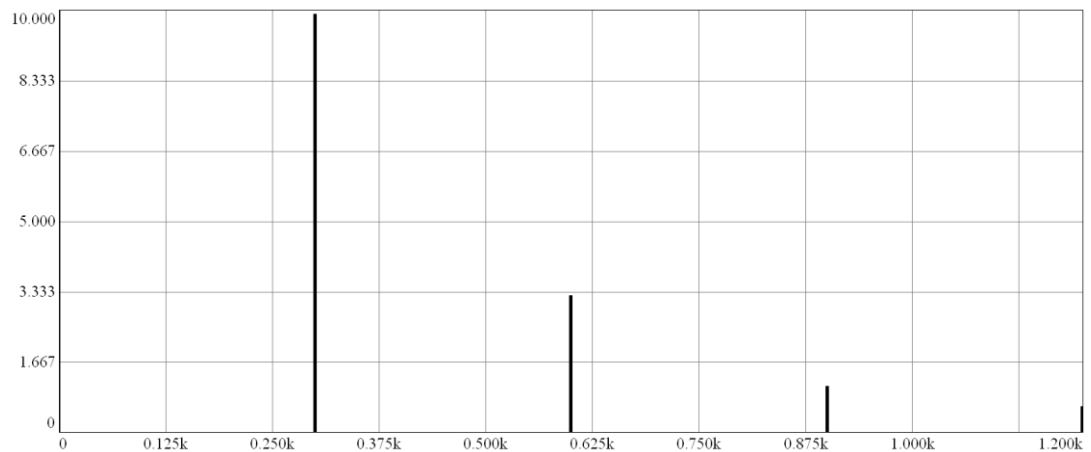


Figure 3.22 DC bus voltage harmonic spectrum of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor and without filter inductors (1.67 V/div, 125 Hz/div).

As Figure 3.21 is considered, the peak to peak voltage ripple decreased from 71.5 V to nearly 25 V and average voltage $v_{dc_r_avg}$ increased from 514 V to nearly 525 V. Figure 3.23 illustrates the dc bus voltage for the rectifier with 0.4 mF dc bus capacitor and 4% ac line and 4% dc link inductors. As expected, the bus capacitor pp voltage ripple decreased to 2.5 V. Figure 3.24 shows the corresponding harmonic spectrum. The 300 Hz voltage ripple is reduced with use of inductor filters as seen in the spectrum.

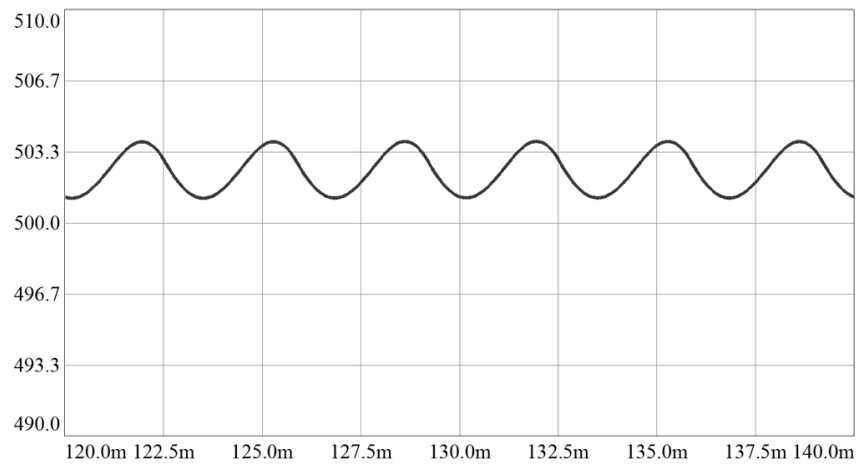


Figure 3.23 DC bus voltage of the 2.2 kW three-phase diode rectifier with 0.4 mF capacitor, 4 % ac line reactor and 4% dc link inductor (3.3 V/div, 2.5 ms/div).

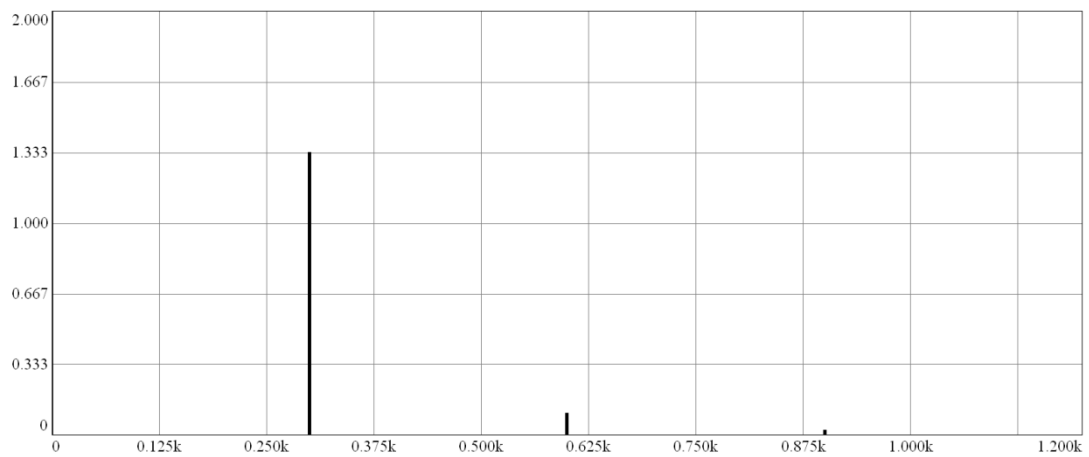


Figure 3.24 DC bus voltage harmonic spectrum of the 2.2 kW three-phase diode rectifier equipped with 0.4 mF capacitor, 4 % ac line reactor and 4 % dc link inductor (0.33 V/div, 125 Hz/div).

3.2 PWM Voltage Source Inverter

The conversion of dc power to ac form is realized by inverters. The input of an inverter can be either a current source or a voltage source, which are called current source inverter and voltage source inverter respectively. Inverters are widely used in battery operated systems, UPS systems, and motor drive circuits. In industrial applications, the voltage source inverter type is generally used. Figure 3.25 shows the general circuit diagram of a three phase voltage source inverter. It consists of controlled semiconductor switches; generally power MOSFETs or IGBTs, which are used with anti-parallel diodes. The dc bus voltage is assumed to be divided into two to simplify the analysis of the circuit.

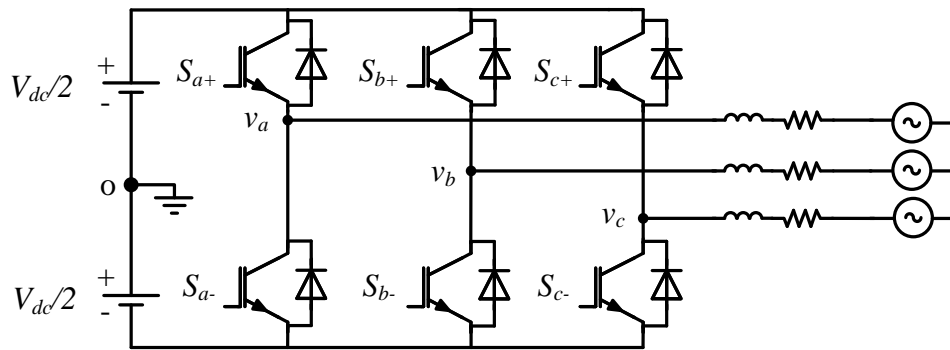


Figure 3.25 Three-phase voltage source inverter.

3.2.1 Principle of Operation

The most widely used inverter type is pulse width modulation (PWM) voltage source inverter. By PWM, the required ac voltage magnitude and frequency is programmed by high frequency rectangular voltage pulses [27]. The carrier based PWM is the preferred approach in most applications due to the low-harmonic distortion waveform characteristics with well defined harmonic spectrum, the fixed switching frequency, and implementation simplicity. They employ the “per-carrier cycle volt-second balance” principle to program a desirable inverter output-voltage waveform [28]. By per carrier cycle volt-seconds balance rule, the average output voltage of the inverter becomes equal to the reference voltage. So, if the reference voltage is sinusoidal, the average output voltage becomes also sinusoidal.

Carrier based PWM can be implemented by either scalar or space vector technique. In scalar approach, a modulation wave with the frequency of desired ac voltage is compared with a high frequency triangle carrier wave to define the switching instants of the switches. In space vector implementation, the length of the inverter switch states for each carrier cycle are pre-calculated using space vector theory and voltage pulses directly programmed [27] where the upper switch states are shown in the brackets (S_{a+} , S_{b+} , S_{c+}), “1” is on and “0” is off state. Figure 3.26 shows the scalar implementation technique and Figure 3.27 illustrates the space vectors used in vector implementation of PWM. In scalar implementation, the upper switch is turned ON when the modulation wave is larger than the carrier and switched OFF when modulation wave is smaller than the carrier. The upper and lower switches always work in complementary manner and a dead time is introduced between their switching instants to prevent a possible short circuit during a transition from ON to OFF state or vice versa. For three phase inverters, three modulation waves are used for each leg of the inverter.

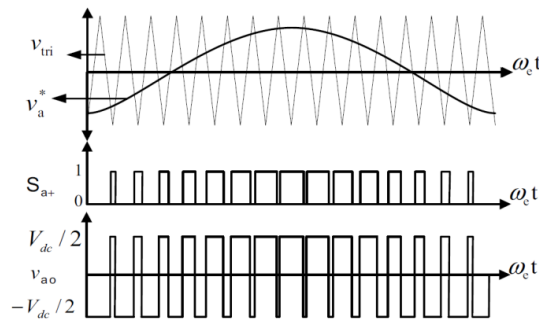


Figure 3.26 Scalar implementation of PWM; with modulation wave v_a^* for a phase, triangle carrier v_{tri} , switch states for S_{a+} , and output voltage v_{ao} [27].

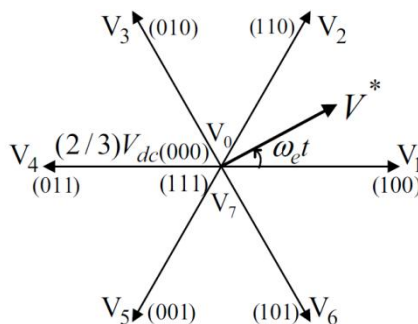


Figure 3.27 Voltage space vectors of three-phase two-level inverter [27].

3.2.2 Zero Sequence Signal Injection

In three phase three wire inverters, the neutral point is not connected and no current flows through this point. If a voltage offset in equal magnitude is added to all modulation waves, the three line-to-neutral voltages increase by the same amount but the line-to-line voltage references and hence the magnitude of the generated line-to-line voltages per carrier cycle is not affected. This however changes the places of the voltage pulses and affects the switching characteristics of the inverter. If the offset voltage has the frequency of three times the modulation wave frequency, it is called zero sequence signal [27]. By zero sequence signal injection, different kinds of PWM methods can be generated offering various performance characteristics.

3.2.3 Commonly Used PWM Methods and Their Scalar Implementation

Various PWM methods exist with different performance figures in terms of voltage linearity, switching harmonics, switching loss, voltage/current ripple and common mode voltage/current [27]. If the modulation wave is between the triangle carrier wave upper and lower limits, the output voltage can be related to the modulation wave function by a linear equation. The voltage linearity starts to disappear if the modulation wave exceeds the limits of the triangle. The ratio of the magnitude of ac voltage generated by a PWM method in the linear operating region, V_{1m} , to the magnitude of fundamental sinusoidal voltage generated by square wave switching, $\frac{2}{\pi}V_{dc}$, (theoretical maximum ac peak output voltage attainable from a dc voltage V_{dc}) is defined as modulation index M_i (3.8) [29]. Modulation index is a performance figure for a PWM method expressing its dc bus voltage utilization level. Each PWM method offers different M_i value due to different switching patterns.

$$M_i = \frac{V_{1m}}{\frac{2}{\pi}V_{dc}} \quad (3.8)$$

3.2.3.1 Sinusoidal PWM (SPWM)

In this method, a sinusoidal reference modulation wave is compared with the high frequency triangle carrier and the output voltage pulses are generated according to the switching rule stated in section 3.3.1 as illustrated in Figure 3.27. The maximum available

peak line-to-neutral voltage by SPWM is $V_{dc}/2$ which corresponds to a maximum modulation index M_i of 0.785. So, for SPWM; $0 \leq M_i \leq 0.785$.

3.2.3.2 Space Vector PWM (SVPWM)

Space vector PWM offers a higher modulation index limit than SPWM and is used very often in practice. Its output current ripple characteristic is also better than SPWM. Scalar implementation of SVPWM is done by injecting the half of the minimum amplitude wave among three modulation waves to all waves. This brings a maximum attainable ac output voltage magnitude of $V_{dc}/\sqrt{3}$, resulting the maximum modulation index of $M_i=0.907$.

3.2.3.3 Discontinuous PWM (DPWM1)

In DPWM1, the zero-sequence signal is injected such that reference signal of one phase is always clamped to the positive or negative dc bus. The clamped phase is alternated throughout the fundamental cycle. The phase signal which is the largest in magnitude is clamped to the dc bus with the same polarity [30]. DPWM1 generates low switching losses and offers an operation with $0 \leq M_i \leq 0.907$.

3.3 Drive System

The circuit of a conventional ac motor drive is shown in Figure 3.28, including the closed loop speed controller block of the motor.

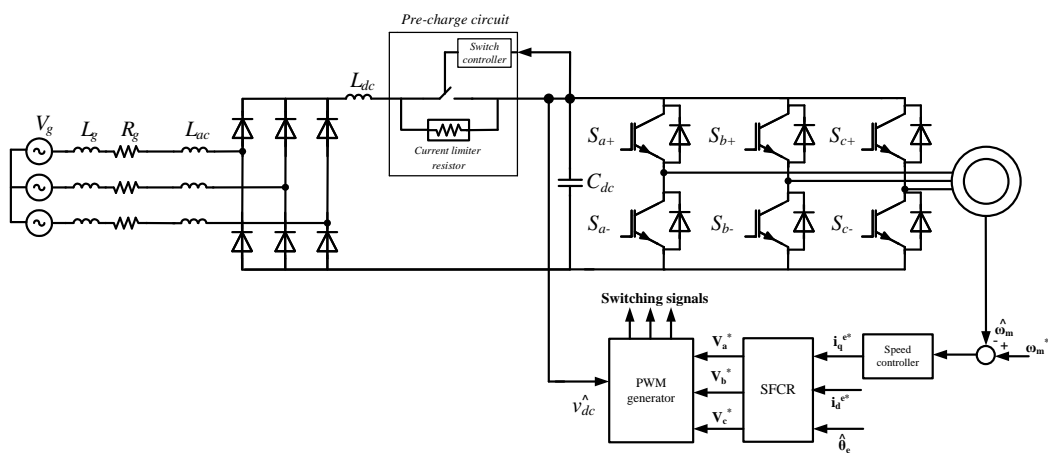


Figure 3.28 AC motor drive circuit with front end diode rectifier.

3.3.1 DC Bus Voltage Characterization of Rectifier-PWM Inverter Drive

Considering their combined operation, the rectifier operates as the voltage source for the inverter and inverter acts as a load for the rectifier. Thus, the rectifier dc bus voltage waveform defines the output voltage quality of the inverter, whereas the inverter load type and rating affects the dc bus voltage characteristics and stability. This relation can be explained in more detail as follows. The three phase diode rectifier generates a dc voltage with 300 Hz ripple and the bus capacitor minimizes the voltage variations proportional to its capacitance. The inverter on the other hand, demands a definite voltage per carrier cycle and draws current in form of pulses from the dc bus. Depending on the load type and rating, the magnitude of voltage and current demanded by the inverter may increase or decrease, which causes variations on the capacitor voltage. This in turn changes the dc bus voltage magnitude seen by the inverter and affects the inverter output ac voltage, and the cycle goes on. Hence, the dc bus voltage characteristics of an ac-dc-ac motor drive circuit with front end diode rectifier depends both on rectifier and inverter operations.

3.3.2 DC Bus Disturbance Rejection and Its Effect On the DC Bus Voltage Stability

As explained in the previous section, the inverter output voltage quality directly depends on rectifier output voltage. Assuming a constant dc bus voltage, a constant amplitude reference voltage, in other words a constant modulation index M_i , generates a constant amplitude ac output voltage. However, if the average rectifier dc bus voltage is not enough or it contains high voltage ripple, the inverter output voltage generated by constant M_i , regardless of the dc bus voltage, is influenced by the dc bus voltage variations. To prevent this situation, the modulation index M_i^* is updated to M_i^{**} , using the instantaneous dc bus voltage according to formula given by (3.9).

$$M_i^{**} = M_i^* \frac{V_{dc}}{V_{dc}^*} \quad (3.9)$$

In 3.9, M_i^{**} is the updated modulation index, V_{dc} is the measured dc bus voltage and V_{dc}^* is the ideal or reference dc bus voltage. Hence, by this method, if the actual dc bus voltage V_{dc} decreases below the ideal V_{dc}^* , M_i^* is increased with the same ratio and vice versa, so that the amplitude of the output ac voltage of the inverter is kept constant.

The dc bus disturbance rejection improves the output quality of the inverter whereas it puts more stress on the dc bus voltage. To give a more specific explanation, assuming that the bus voltage is below the ideal dc bus voltage level V_{dc}^* , the dc bus disturbance rejection algorithm increases the modulation index and the inverter draws more current, which in turn reduces the bus capacitor voltage further, and vice versa. The drive circuits with stiff dc bus voltage, such as the ones equipped with high capacitance dc bus capacitor, is nearly not effected at all from this situation and bus voltage stability is protected due to high energy storage capability. In addition, stiff dc bus voltage stability does not depend on load type.

If the dc bus lacks high energy storage characteristics, the dc bus disturbance rejection may degrade the stability significantly by causing large voltage variations on dc bus capacitor. If the bus voltage is not sufficient to supply the reference ac voltage demanded by inverter, the inverter modulation index is increased which further decreases the bus voltage and vice versa, causing voltage oscillations.

The load type also affects the bus voltage stability if the bus voltage is not stiff. A constant power load always tries to draw constant power from the source, causing negative impedance effect as explained in Chapter 2. If the dc bus voltage is somehow lowered, more current will be drawn by the inverter to keep the product of load voltage and current constant, which further decreases the voltage and again causes more current be drawn and the cycle goes on causing instability on the dc bus. The constant impedance loads, however, draw current proportional to the voltage applied and do not cause negative impedance stability problems.

3.4 Conclusion

In this chapter the operation characteristics of ideal and practical diode rectifiers, the components used in practical rectifiers and their effect on dc bus voltage and line current characteristics are reviewed. The PWM inverter basic operation principles are explained. The dc bus voltage characterization based on operation of rectifier and inverter in a drive system is provided and the aim of dc bus voltage disturbance rejection in drives is described. In the next chapter, the conventional motor drives with front end diode rectifiers utilizing high C_{dc} capacitors are investigated.

CHAPTER 4

INDUCTION MOTOR DRIVE WITH FRONT END DIODE RECTIFIER UTILIZING HIGH CAPACITANCE DC BUS CAPACITOR

4.1 Design of Circuit and Controller

In this section, the conventional induction motor drives with front end diode rectifier utilizing high C_{dc} dc bus capacitor are designed using the controller design procedure explained in Chapter 2 and the practical rectifier circuit design given in Chapter 3. The dc bus capacitors are selected using the 1 mF/5.5 kW capacitance/load power ratio and the filter inductances are selected 4 % for both ac line and dc link [16]. The ac mains parameters are 220 V (line-to-neutral rms) and 50 Hz line frequency. The line impedance parameters are taken from [16], using the Middle East Technical University local distribution transformer parameters. The inverter side of the motor drives utilizes IGBTs with anti-parallel diodes. For modulation method SVPWM is used since it offers higher dc bus voltage utilization compared to SPWM. The switching frequency of the inverters is 10 kHz. Table 4.1 contains the circuit parameters for the designed conventional motor drives.

Table 4.1 Circuit parameters of the conventional motor drives.

Parameter	2.2 kW motor drive	37 kW motor drive
Line inductance, L_g (mH)	0.25	0.0148
Line resistance, R_g (m Ω)	125.0	0.0074
AC line reactor, L_{ac} (mH)	7.75	0.46
DC link inductor, L_{dc} (mH)	7.75	0.46
DC bus capacitor, C_{dc} (mF)	0.4	6.72
Inverter switching frequency, f_c (kHz)	10	10
PWM type	SVPWM	SVPWM

The simulations are conducted with 2.2 kW and 37 kW induction motors parameters of which are taken from [31] and given in Table 4.2. The indirect vector control algorithm is used to drive the motors. The simulations are conducted for two types of loads; constant torque and fan loads. To show the effect of constant power loads on stability of conventional motor drive dc bus voltage, some figures are also included for constant power load operation.

Table 4.2 The parameters of the induction motors used in simulations [31].

Parameter	Value	
Power (kW)	2.2	37
Speed (rpm)	1436	1480
Frequency, f_N (Hz)	50	50
Line to line voltage, U_N (V-rms)	400	400
Current, I_N (A)	5	68.2
Torque, T_N (N.m)	14.6	239
Stator resistance, R_s (Ω)	3.7	0.069
Rotor resistance, R_r (Ω)	2.1	0.044
Stator transient inductance, L_s' (mH)	21	2.3
Magnetizing inductance, L_m (mH)	224	31.3
Moment of inertia, J (kg.m^2)	0.0155	0.831
Viscous friction coefficient, b (N.m.s)	0.0025	0.0341

Table 4.3 includes the regulator gains and bandwidths for the 2.2 kW and 37 kW motor drives. The same controller parameters are used for both fan and constant torque load operation.

Table 4.3 Controller parameters of the conventional motor drives.

Current regulator parameters	2.2 kW motor drive	37 kW motor drive
Proportional gain, K_{pi}	250	22.5
Integral gain, K_{ii}	20000	200
Current regulator bandwidth, f_{rc} (Hz)	1000	1000
Speed regulator parameters	2.2 kW motor drive	37 kW motor drive
Proportional gain, K_{ps}	0.075	2
Integral gain, K_{is}	1.1	80
Speed regulator bandwidth, f_{rs} (Hz)	16	16

The current regulator is operated by double sample per carrier approach resulting in maximum available bandwidth of $f_{rc}=1$ kHz. The speed regulator bandwidth is set so that the motors have sufficient speed command tracking performance but it is not kept so high as large bandwidth increases the noise sensitivity of the regulator and may create torque oscillations. The speed regulators are set to 16 Hz bandwidth. In the simulations, the inverter is used in linear operating region and overmodulation is avoided as it causes low frequency harmonics on the motor currents. In the linear operating region, the maximum modulation index attainable is $M_i=0.907$ by SVPWM. Utilizing the 500 V average dc bus voltage and staying in linear operating region, the 2.2 kW motor is driven to deliver 2 kW output power (93 % load), whereas the 37 kW rated motor is operated to deliver 30.1 kW output power (81 % load).

4.2 Constant Torque Load Operation Simulation Results

The first load type to be simulated is constant torque load. The drives are operated with and without dc bus disturbance rejection methods to investigate the performance differences if exists. The 2.2 kW motor is accelerated to 1500 rpm and the 37 kW one to 1250 rpm steady state speed.

4.2.1 2.2 kW Motor Drive Constant Torque Load Operation without DC Bus Disturbance Rejection

This section includes the simulation results of the 2.2 kW constant torque load drive without dc bus disturbance rejection. Figure 4.1 shows the speed, d-q axis currents and motor torque waveforms during acceleration. Before the non-zero speed command is applied to the speed regulator, the rotor flux has to be waited to be built up and speed reference is kept zero during this period. The time required for flux built-up depends on the rotor time constant, $\tau=L_r/R_r=0.117$, and in approximately 3τ duration the flux of the motor reaches its steady state value. After the flux reaches steady state, the non-zero speed command is applied. To realize this operation, first the reference d axis current of 3 A is applied at $t=0$ and after 3τ duration the speed command is applied, which generates the q axis current reference.

At the start instant, the motor suddenly rotates in negative direction due to load torque applied at $t=0$. The controller acts and starts to track the speed command after a short time.

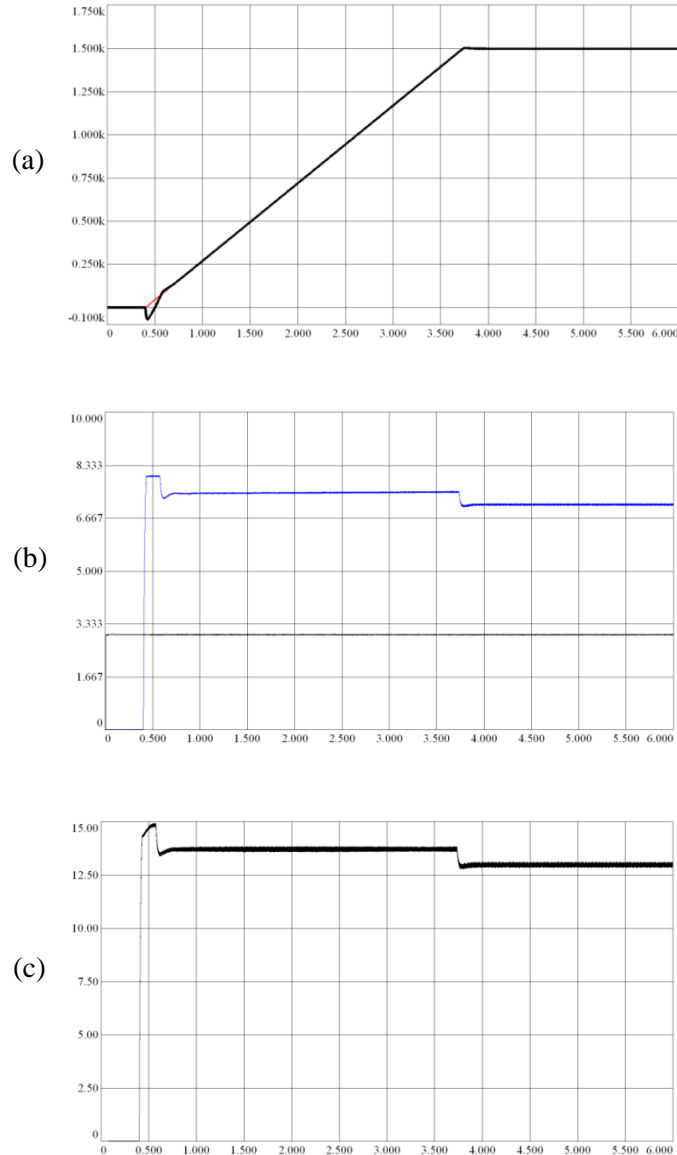


Figure 4.1 2.2 kW constant torque load drive without dc bus disturbance rejection (a) speed (250 rpm/div, 0.5 s/div), (b) d axis current (black) and q axis current (blue) (1.67 A/div, 0.5 s/div), (c) motor torque (2.5 N.m/div, 0.5 s/div)

The motor speed reference has a ramp shape with a slope of 450 rpm/s. The slope of the ramp is set by the gain of speed ROCL. Until reaching set speed, the torque is the sum of

inertial and load torque. At set speed, the motor torque is equal to load torque of 13 N.m. Figure 4.2 shows the dc bus voltage waveform. The pp voltage ripple is very low as expected around 3V for average 498.5 V.

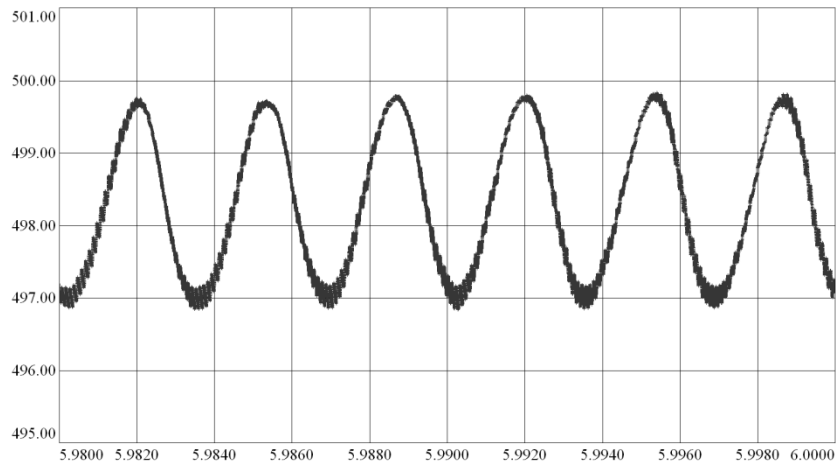


Figure 4.2 DC bus voltage of 2.2 kW constant torque load drive without dc bus disturbance rejection (1 V/div, 2 ms/div).

Figure 4.3 show the corresponding harmonic spectrum. As expected, harmonics in the low frequency spectrum are around 300 Hz and multiples and 10 kHz switching frequency harmonics are seen in high frequency region.

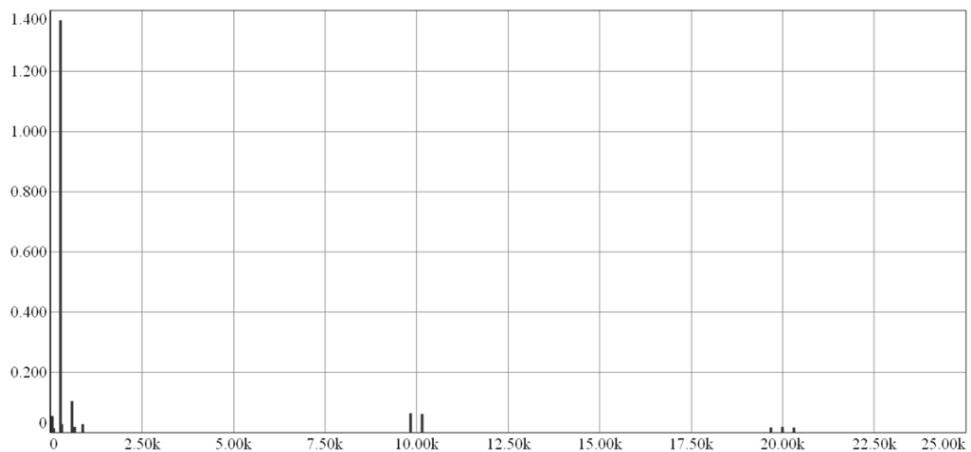


Figure 4.3 Harmonic spectrum of dc bus voltage for 2.2 kW constant torque load drive without dc bus disturbance rejection (0.2 V/div, 2.5 kHz/div).

The stability of the dc bus voltage is high as expected due to the high capacitance which offers high energy storage and low voltage ripple. This creates a dc bus voltage which is very close to an ideal dc source and enables the inverter to synthesize good quality current with very low harmonic distortion. The good quality current feedback also enables the SFCR to generate a voltage reference with constant amplitude at steady state. If the voltage references generated by SFCR on two phase stationary reference frame (α - β axes) are plotted in x-y coordinates for one complete electrical cycle, the resulting waveform is a circle the radius of which is equal to the amplitude of sinusoidal voltage reference. Meanwhile, the maximum inverter output voltage that can be synthesized by the available dc bus voltage can also be plotted for the same time instants with the voltage references. This will also generate a circle radius of which shows the limit of the maximum inverter output voltage that can be generated by the PWM method used. The obtained figure gives a graphical representation for the dc bus voltage stability, the inverter output voltage limits defined by the dc link voltage, and the quality and amplitude of the voltage reference waveform. Figure 4.4 shows the α and β axes voltage reference waveforms against the angle θ (theta) on the stationary reference frame for the 2.2 kW fan drive operating at 1300 rpm and the corresponding α - β voltage circle illustrating the mapping for θ between 0-360°. The amplitude of the voltage references defines the radius of the circle. The Matlab R2010b [32] is used to process the data and draw the voltage circles in the thesis.

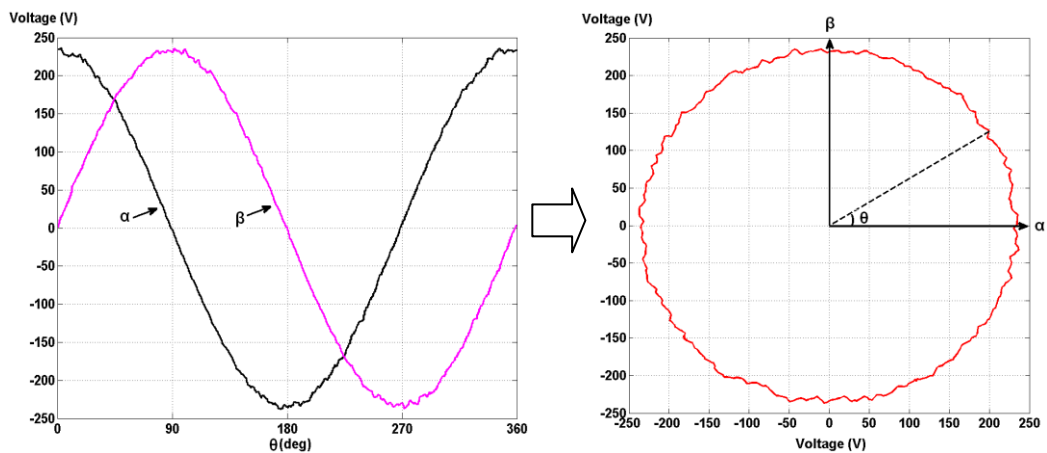


Figure 4.4 Reference voltages in stationary α - β frame against theta (left) and corresponding voltage circle constructed by α vs β plot for 0-360° cycle.

The maximum available voltage limit determined by the instantaneous dc bus voltage can also be plotted for the same angle of α - β axes voltages as in Figure 4.5.

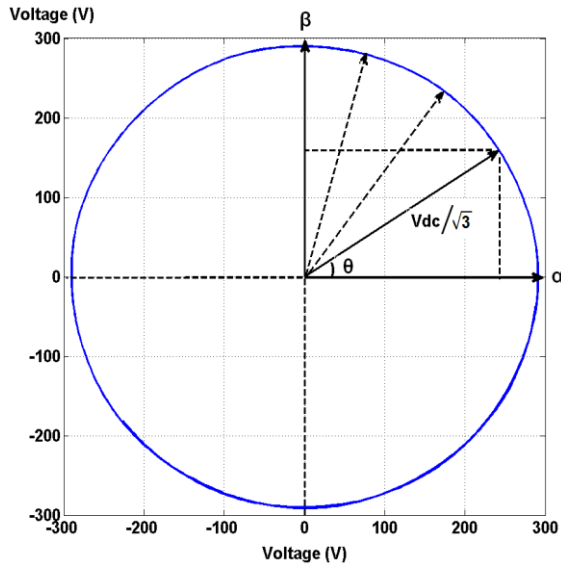


Figure 4.5 The decomposition of dc bus voltage along α - β axes and construction of inverter output voltage limit circle.

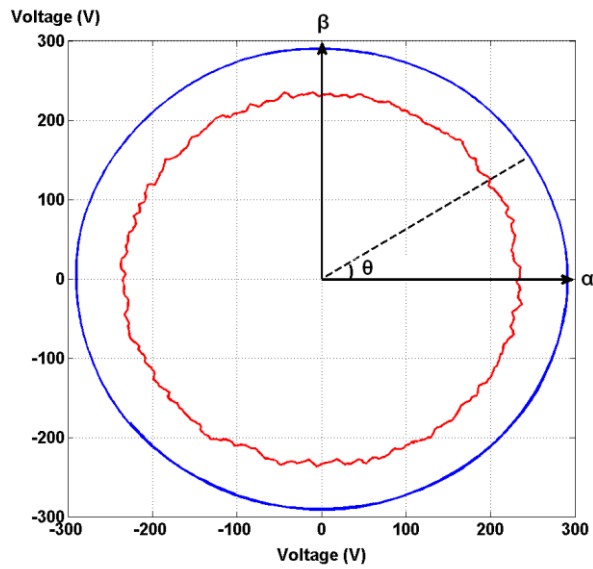


Figure 4.6 The reference voltage circle (red) and inverter output voltage limit circle (blue).

The maximum amplitude of the sinusoidal voltage that can be generated by SVPWM for a dc bus voltage of V_{dc} is $V_{dc}/\sqrt{3}$. So, the voltage circle corresponding to the inverter output voltage limit has a radius of $V_{dc}/\sqrt{3}$. The circle can be constructed by first decomposing the dc bus voltage value along α and β axes using θ and plotting the decomposed components in x-y coordinates. Figure 4.6 shows the inverter voltage reference (red) and output voltage limit (blue) on the same graph.

When the operating power is increased, the inverter voltage reference (the radius of the voltage reference circle) increases.

Figure 4.7 shows the steady state torque waveform with 0.3 N.m pp ripple.

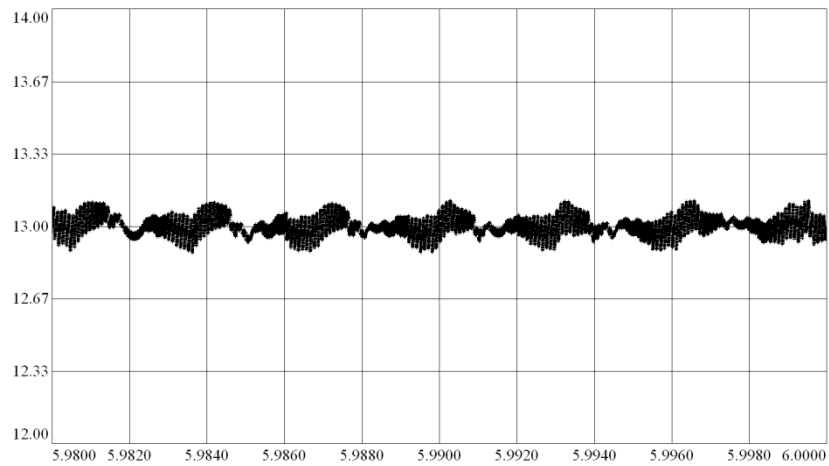


Figure 4.7 Motor steady state torque of 2.2 kW constant torque load drive without dc bus disturbance rejection (0.33 N.m/div, 2 ms/div).

Figure 4.8 and Figure 4.9 shows the line current waveform and corresponding spectrum. THD_{ig} is 29.4 % and PF is 0.931.

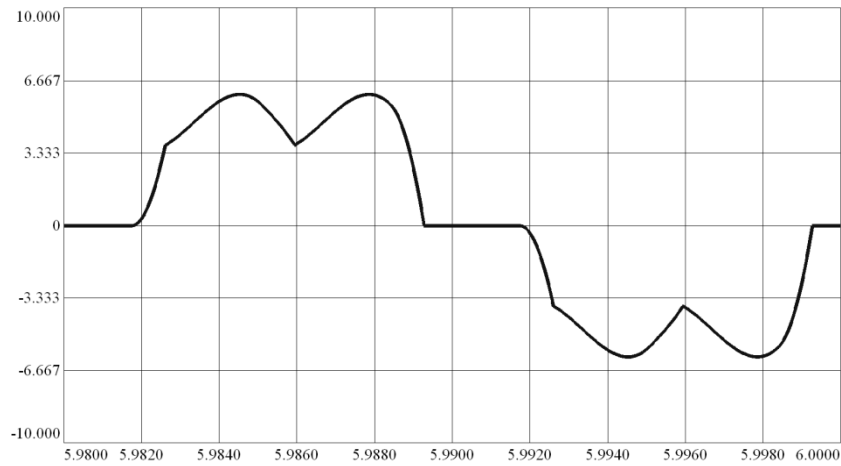


Figure 4.8 The line current waveform of 2.2 kW constant torque load drive without dc bus disturbance rejection (3.33 A/div, 2 ms/div).

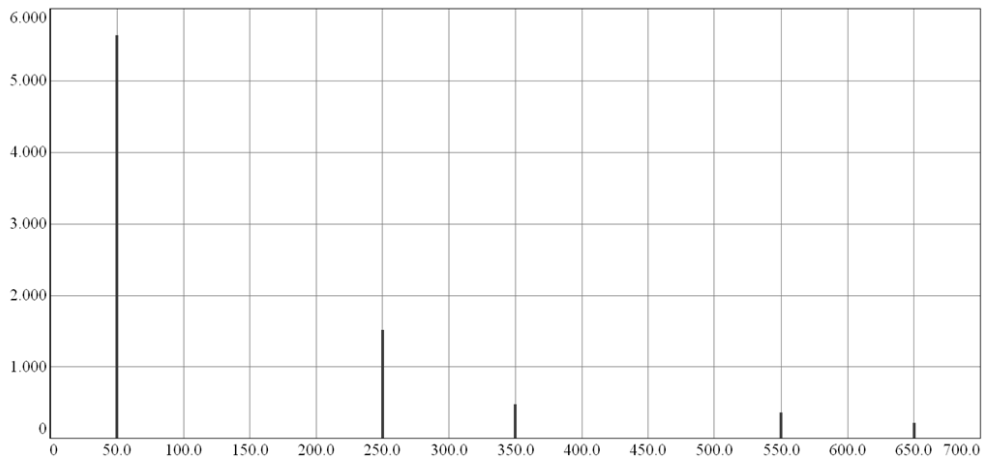


Figure 4.9 Harmonic spectrum of line current of 2.2 kW constant torque load drive without dc bus disturbance rejection (1 A/div, 50 Hz/div).

4.2.2 2.2 kW Motor Drive Constant Torque Load Operation with DC Bus Disturbance Rejection

Since the dc bus voltage is stiff and its average value is sufficient, the motor drive performance is not affected from the dc bus disturbance rejection and waveforms are not provided for the second time. The simulation data are given in Chapter 6 for evaluation.

4.2.3 37 kW Motor Drive Constant Torque Load Operation without DC Bus Disturbance Rejection

Figure 4.10 shows the start-up characteristics of the motor. Since the inertia of 37 kW motor is higher, the acceleration is kept low (225 rpm/s) compared to 2.2 kW motor to not to exceed motor current limit.

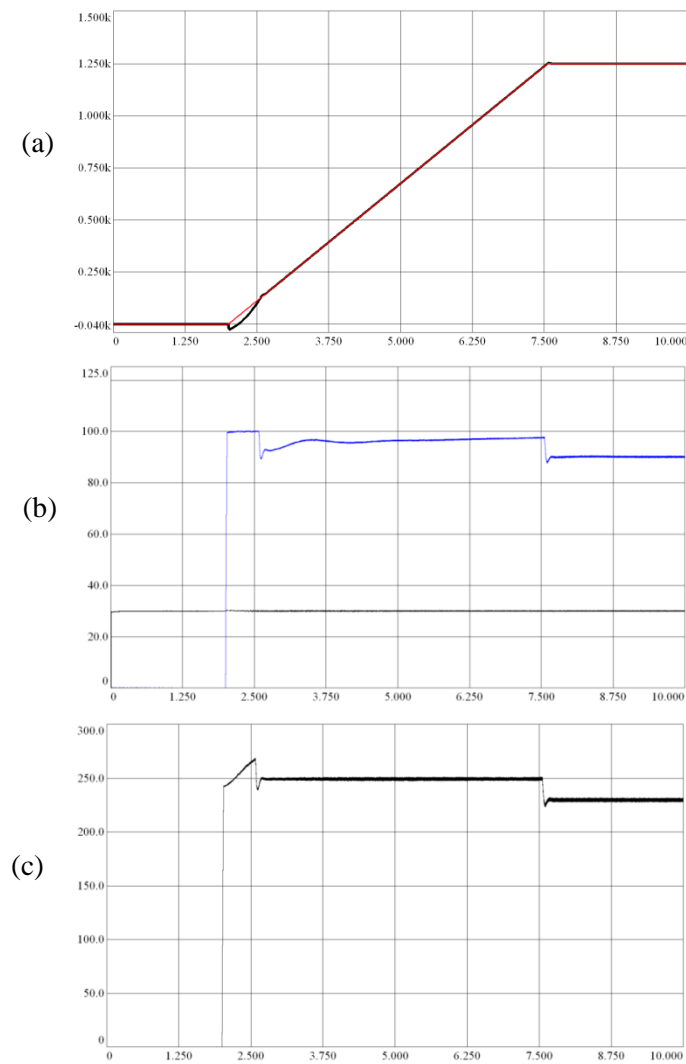


Figure 4.10 37 kW constant torque load drive without dc bus disturbance rejection (a) speed (250 rpm/div, 1.25 s/div), (b) d axis current (black) and q axis current (blue) (20 A/div, 1.25 s/div), (c) motor torque (50 N.m/div, 1.25 s/div)

Figure 4.11 shows dc bus voltage waveform of the motor drive. It has nearly 2.8 V pp voltage ripple.

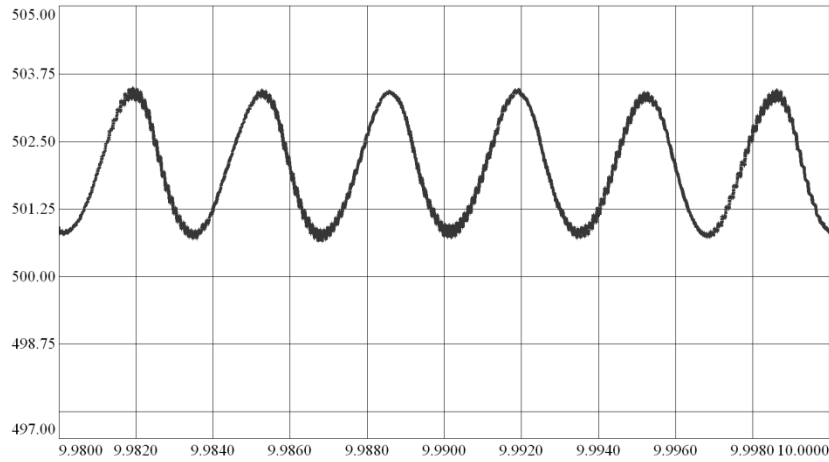


Figure 4.11 DC bus voltage of 37 kW constant torque load drive without dc bus disturbance rejection (1.25 V/div, 2 ms/div).

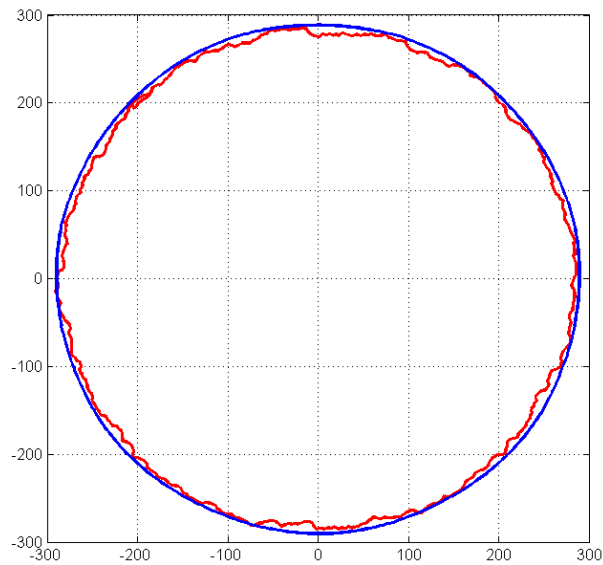


Figure 4.12 Inverter voltage reference (red) and inverter output voltage limit circle (blue) of 37 kW constant torque load drive without dc bus disturbance rejection (100 V/div, 100 V/div).

Figure 4.12 illustrates the voltage circles for the motor drive. The inverter voltage reference is nearly coincident with the voltage limit circle, which means the inverter is operating close to its linearity limit.

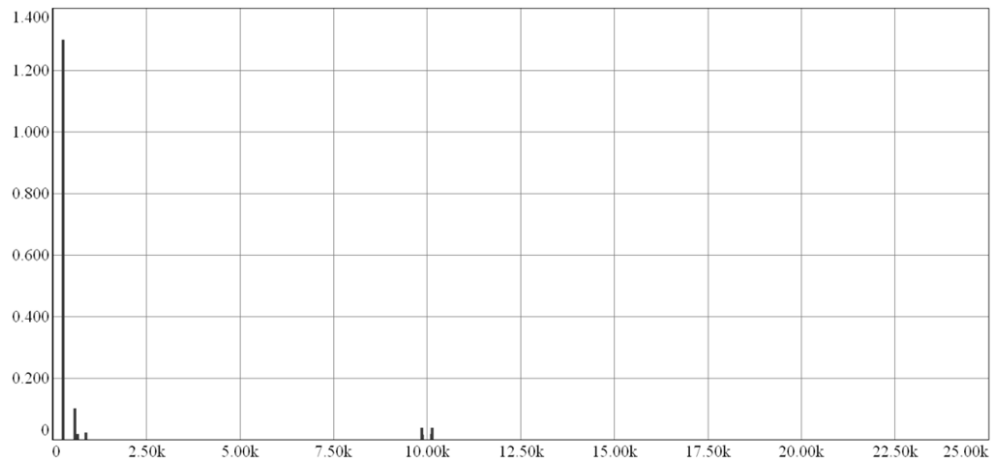


Figure 4.13 Harmonic spectrum of dc bus voltage for 37 kW constant torque load drive without dc bus disturbance rejection (0.2 V/div, 2.5 kHz/div).

Figure 4.14 shows the steady state torque waveform of the motor. It has 3.3 N.m pp torque ripple on 230 N.m average torque.

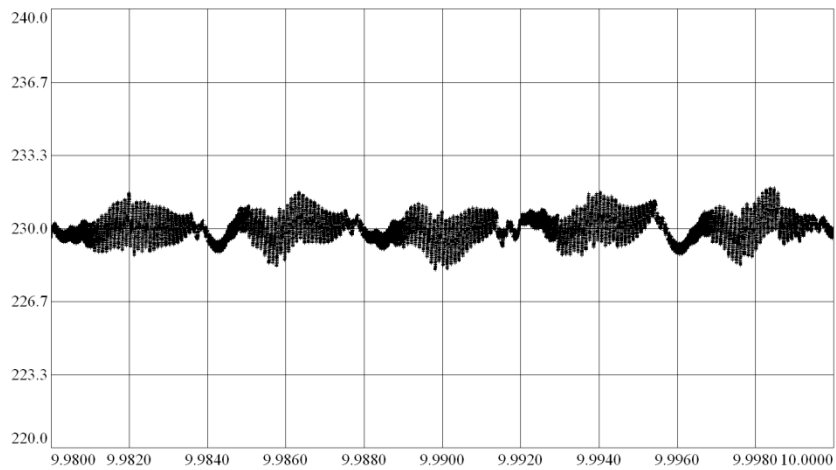


Figure 4.14 Motor steady state torque of 37 kW constant torque load drive without dc bus disturbance rejection (3.3 N.m/div, 2 ms/div).

Figure 4.15 and Figure 4.16 illustrate the line current and the corresponding harmonic spectrum of the drive. The THD_{ig} is 32.4 % and PF is 0.928.

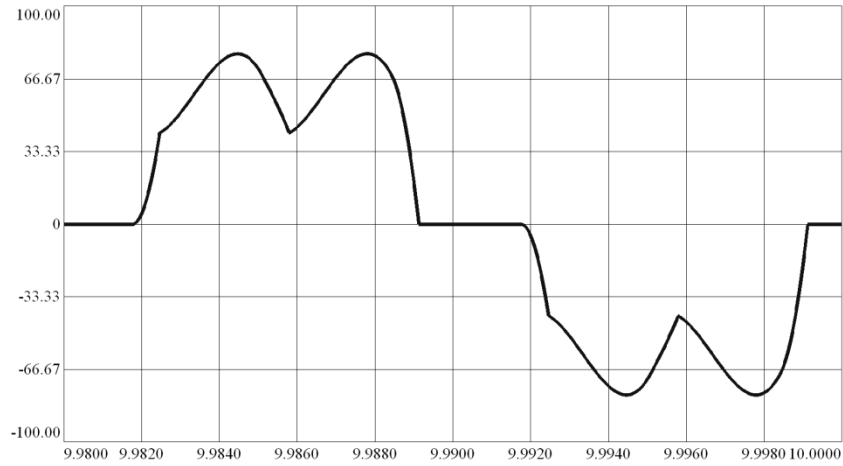


Figure 4.15 The line current waveform of 37 kW constant torque load drive without dc bus disturbance rejection (33.3 A/div, 2 ms/div).

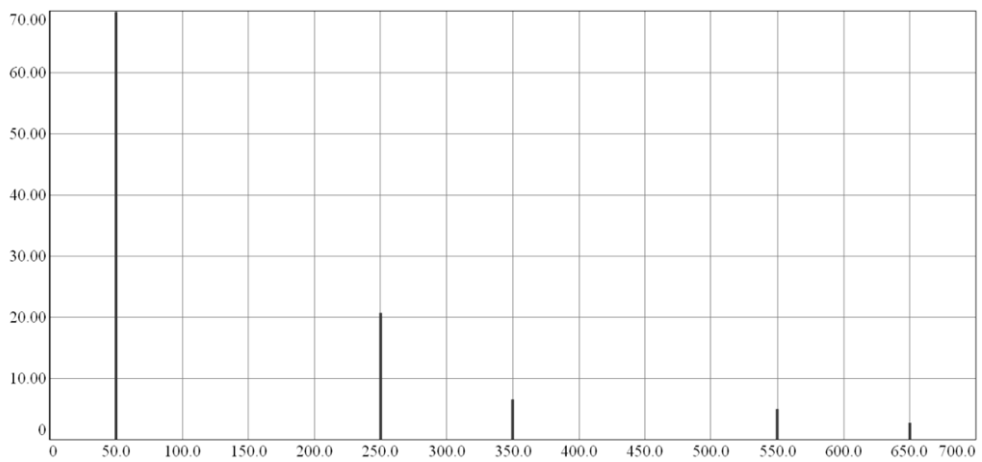


Figure 4.16 Harmonic spectrum of line current for 37 kW constant torque load drive without dc bus disturbance rejection (10 A/div, 50 Hz/div).

4.2.4 37 kW Motor Drive Constant Torque Load Operation with DC Bus Disturbance Rejection

The simulation results of the 37 kW constant torque load drive with dc bus disturbance rejection is very similar to that without disturbance rejection. Since the stiff dc bus voltage stability does not change with the dynamics of the disturbance rejection, the operation of the drive is not affected and shows nearly equal performance with the drive without disturbance rejection. The simulation data are provided by tables in Chapter 6 for purpose of evaluation and comparison.

4.3 Fan Load Operation Simulation Results

The second load type to be considered is the fan load characteristics of which is given in Chapter 2. The 2.2 kW motor is used with a fan load of windage coefficient $5.27e-4$ N.m.s²/rad², and driven at 1500 rpm maximum speed delivering 13 N.m output torque, according to the fan load torque-speed relation given by (2.3). The 37 kW motor is used with a fan load of windage coefficient $5.27e-4$ N.m.s²/rad² resulting in 230 N.m output torque at 1250 rpm.

The simulation results include the operation for two cases; the dc bus disturbance rejection applied and not applied, to compare the drive performances. Due to stiff and sufficient level of dc bus voltage, no significant difference is expected in the performances of the motor drives with and without dc bus disturbance rejection, like in the case of constant torque load drives.

4.3.1 2.2 kW Motor Drive Fan Load Operation without DC Bus Disturbance Rejection

This section includes the results of the simulations for the 2.2 kW fan drive without dc bus disturbance rejection.

Figure 4.17 shows the motor acceleration, d and q axis current variations, and the internal torque variation from the start up instant to the steady state operating point. It is seen that the q axis current increases quadratically with speed. The motor internal torque variation

follows the q axis current and it also has a quadratic dependence on the operating speed. This is due to the fact that the torque demand of the fan load is proportional to the square of the speed by the windage coefficient of the fan.

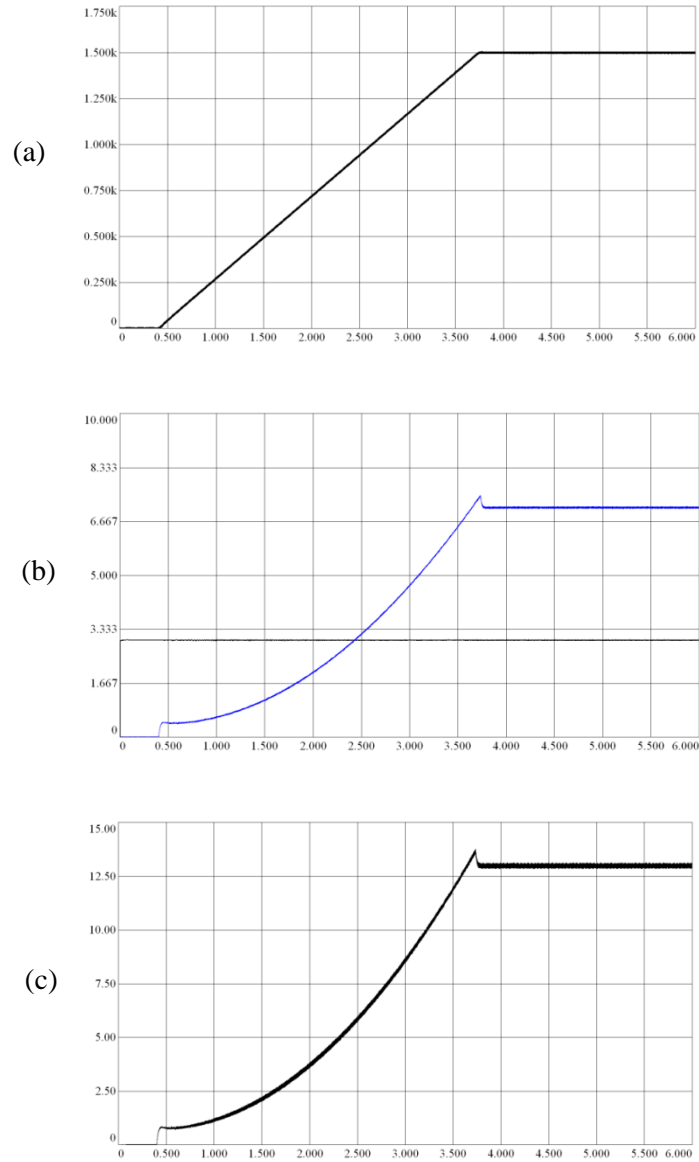


Figure 4.17 2.2 kW fan load drive without dc bus disturbance rejection (a) speed (250 rpm/div, 0.5 s/div), (b) d axis current (black) and q axis current (blue) (1.67 A/div, 0.5 s/div), (c) motor torque (2.5 N.m/div, 0.5 s/div)

Figure 4.18 shows the steady state waveform of the motor torque. There is peak to peak 0.3 N.m (2 %) ripple on steady state torque of the motor.

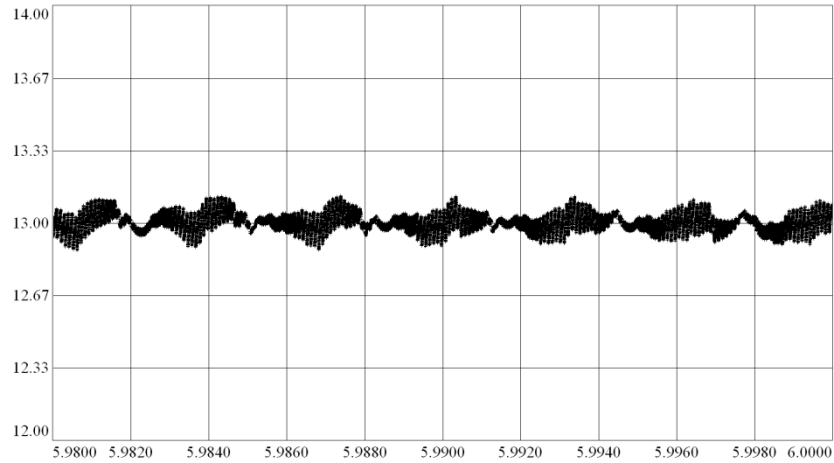


Figure 4.18 Motor steady state torque of 2.2 kW fan load drive without dc bus disturbance rejection (0.33 N.m/div, 2 ms/div).

Figure 4.19 illustrates the steady state dc bus voltage waveform of the drive. It contains 300 Hz ripple as expected. The peak to peak voltage ripple is 3.2 V (0.64 %).

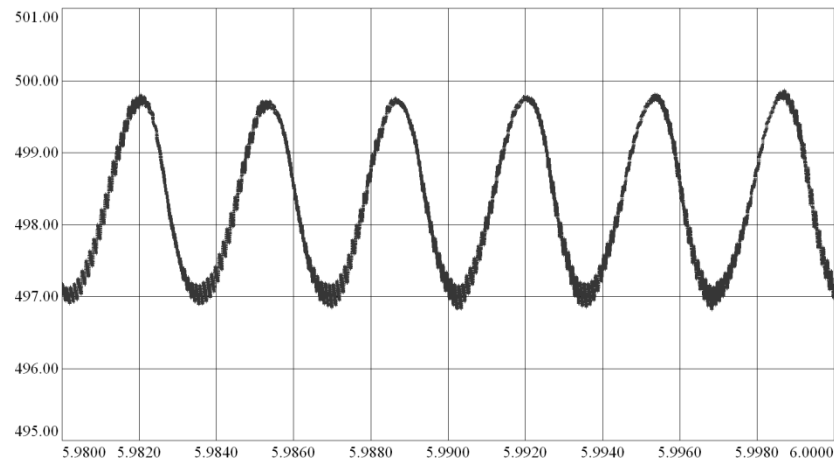


Figure 4.19 DC bus voltage of 2.2 kW fan load drive without dc bus disturbance rejection (1 V/div, 2 ms/div).

The harmonic spectrum of the bus voltage is given in Figure 4.20. The bus voltage includes the 300 Hz harmonics and its multiples in the low frequency region and 10 kHz switching frequency harmonics in the high frequency region.

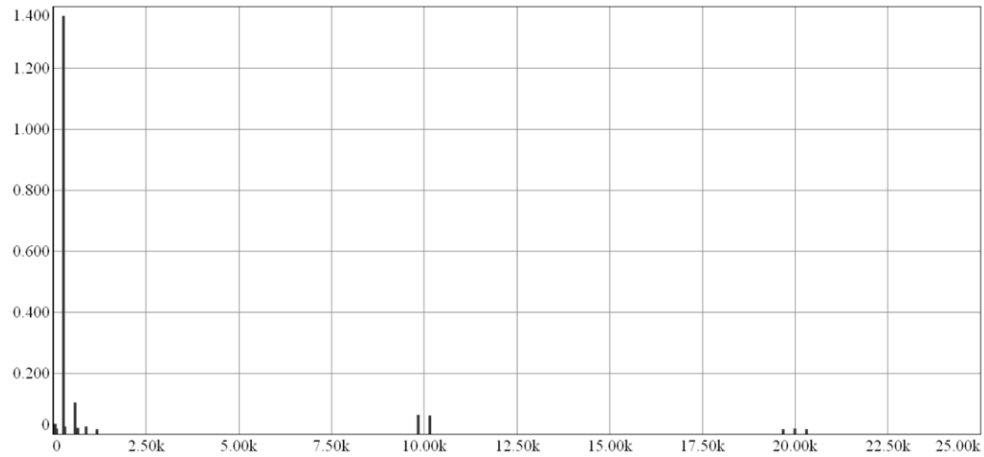


Figure 4.20 Harmonic spectrum of dc bus voltage for 2.2 kW fan load drive without dc bus disturbance rejection (0.2 V/div, 2.5 kHz/div).

The line current waveform for the drive is given in Figure 4.21. The line current has a THD_{ig} of 29.4 % and the PF of 0.931 lagging.

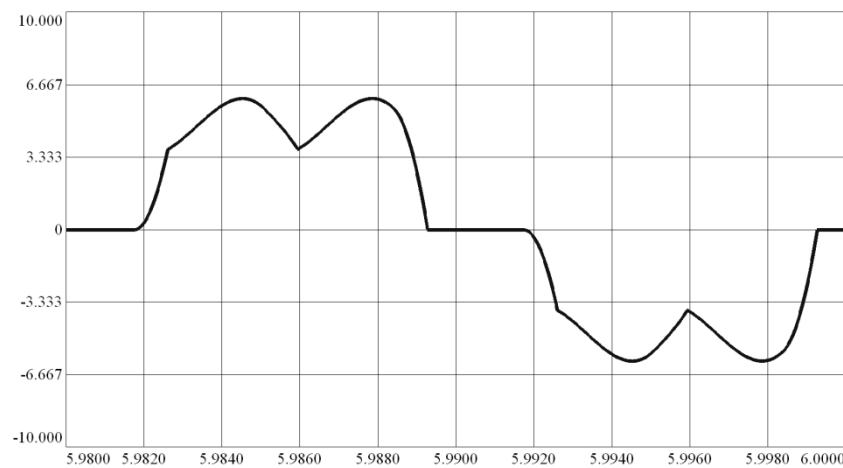


Figure 4.21 The line current waveform of 2.2 kW fan load drive without dc bus disturbance rejection (3.33 A/div, 2 ms/div).

Figure 4.22 illustrates the harmonic spectrum of the line current for the 2.2 kW fan load drive without dc bus disturbance rejection.

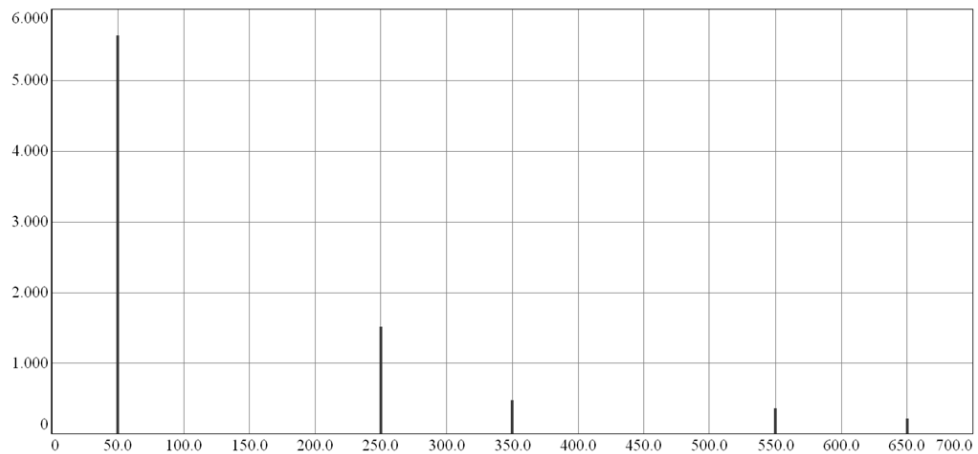


Figure 4.22 Harmonic spectrum of line current for 2.2 kW fan load drive without dc bus disturbance rejection (1 A/div, 50 Hz/div).

4.3.2 2.2 kW Motor Drive Fan Load Operation with DC Bus Disturbance Rejection

The simulation waveforms for the 2.2 kW fan load operation with disturbance rejection are not given since it yielded very close results with the drive without disturbance rejection. However, the data of the simulations are provided by tables in Chapter 6 for purpose of comparison and evaluation.

4.3.3 37 kW Motor Drive Fan Load Operation without DC Bus Disturbance Rejection

The acceleration waveform of the 37 kW fan load drive is similar to that of 2.2 kW drive. The q axis current and motor internal torque has quadratic variation with the operating speed as expected. Due to this similarity except the steady state operating speed and torque, the acceleration waveforms are not provided and only steady state waveforms for dc bus voltage, motor internal torque, and line current are given.

Figure 4.23 illustrates the dc bus voltage waveform for 37 kW fan load drive without dc bus disturbance rejection. There is nearly 2.5 V pp voltage ripple on 502.5 V average dc voltage, very low as expected.

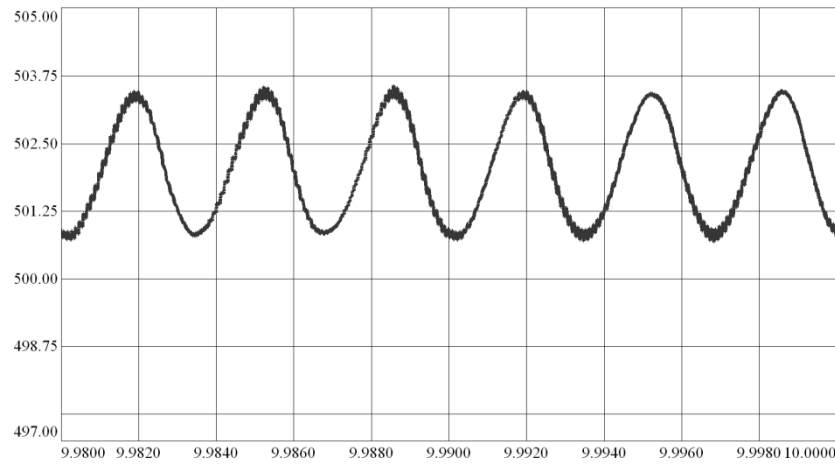


Figure 4.23 DC bus voltage of 37 kW fan load drive without dc bus disturbance rejection (1.25 V/div, 2 ms/div).

Figure 4.24 shows the dc bus voltage harmonic spectrum with expected dominant harmonics at 300 Hz and its multiples.

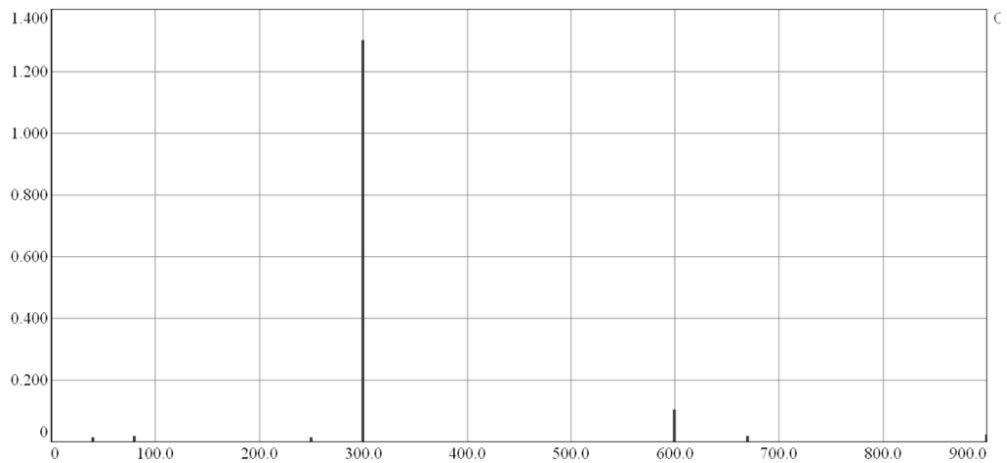


Figure 4.24 Harmonic spectrum of dc bus voltage of 37 kW fan load drive without dc bus disturbance rejection (0.2 V/div, 100 Hz/div).

Motor steady state torque has nearly 3.3 N.m pp ripple, as seen in Figure 4.25.

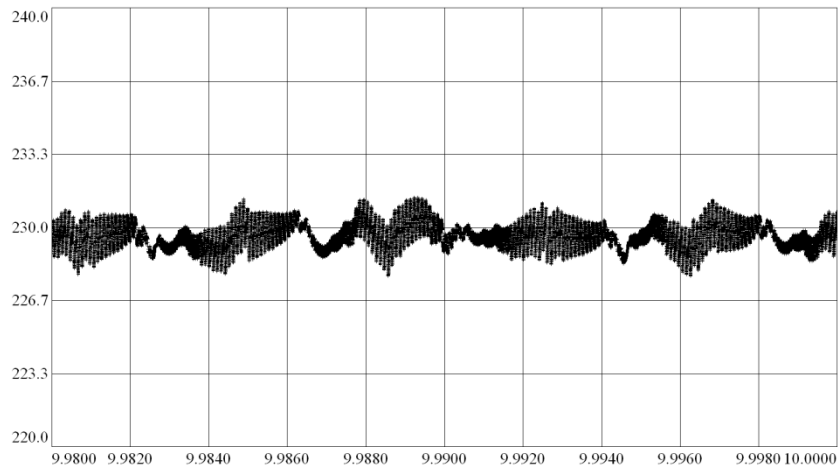


Figure 4.25 Motor steady state torque of 37 kW fan load drive without dc bus disturbance rejection (3.3 N.m/div, 2 ms/div).

Figure 4.26 and Figure 4.27 show the line current and the spectrum of the 37 kW fan drive without dc bus disturbance rejection. The line current has THD_{ig} of 32.4 % and PF is 0.928.

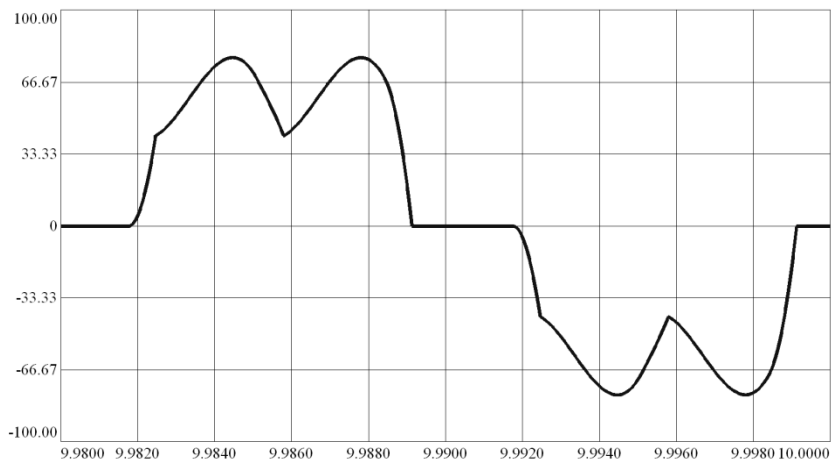


Figure 4.26 Line current waveform of 37 kW fan load drive without dc bus disturbance rejection (33.3 A/div, 2 ms/div).

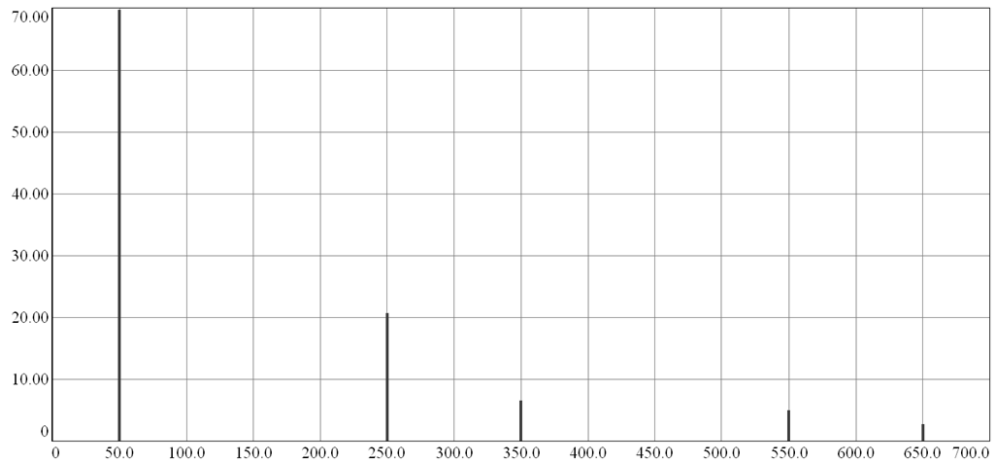


Figure 4.27 Harmonic spectrum of line current of 37 kW fan load drive without dc bus disturbance rejection (10 A/div, 50 Hz/div).

4.3.4 37 kW Motor Drive Fan Load Operation with DC Bus Disturbance Rejection

The simulation waveforms for 37 kW fan drive with disturbance rejection showed similar characteristics with the drive without disturbance rejection. So, the waveforms are not provided second time and the results are tabulated for comparison Chapter 6.

4.4 Constant Power Load Simulation Results

As explained in Chapter 2, the constant power load is the load type demanding always the same power from the drive. The conventional drives do not face stability problem with the negative impedance effect of the constant power load drives but the low C_{dc} motor drives may become unstable. This section is included just to show the stability of the conventional drives under constant power load operation to compare it with the low C_{dc} motor drives in Chapter 5. For this purpose, a constant power load model is constructed using a voltage controlled current source as a load connected to dc link. By adjusting the amplitude of load current automatically so as to keep the product of dc link voltage and load current at a constant value, the constant power load model is created.

Figure 4.28 shows the dc bus voltage for the 2.2 kW constant power load. It is seen that the bus voltage stability is not affected, as expected, and it has similar waveform with the constant torque load and fan load drives.

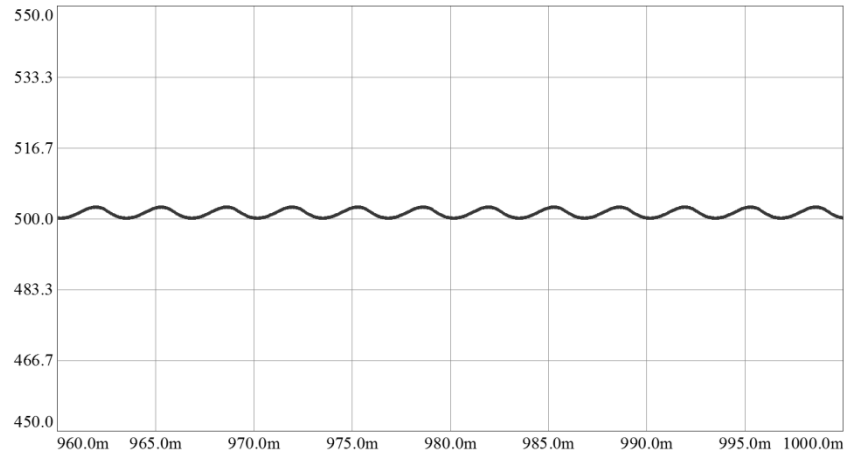


Figure 4.28 DC bus voltage of the 2.2 kW motor drive under constant power load (16.7 V/div, 5 ms/div).

Figure 4.29 shows the line current waveform for the same drive. It has apparently no difference with the previous constant torque load and fan load drives. The THD_{ig} is around 31.7 % and PF is 0.93.

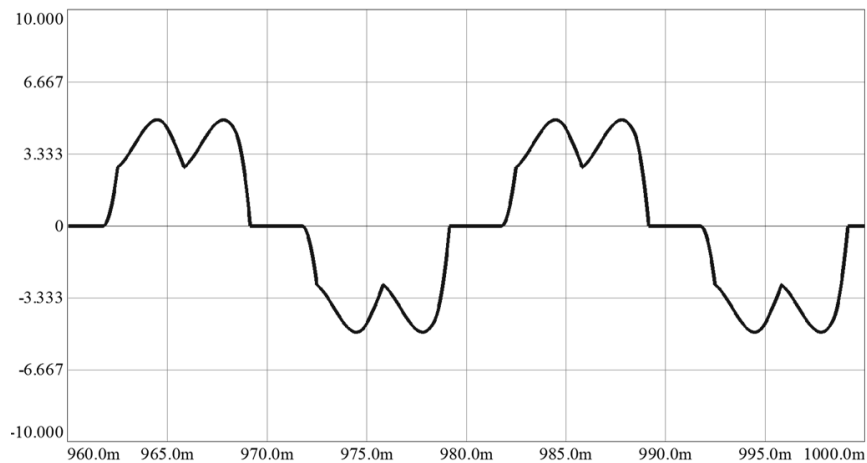


Figure 4.29 Line current of the 2.2 kW motor drive under constant power load (3.33 A /div, 5 ms/div).

Figure 4.30 shows the dc bus voltage for the 37 kW constant power load. The bus voltage stability is not affected from constant power load characteristics as expected. The line current waveform for the same drive is seen in Figure 4.31. The THD_{ig} is around 32.9 % and PF is 0.93.

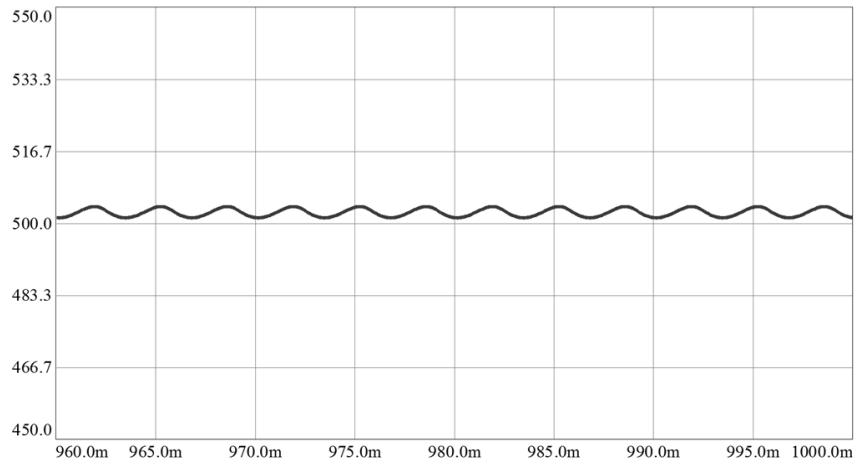


Figure 4.30 DC bus voltage of the 37 kW motor drive under constant power load (16.7 V/div, 5 ms/div).

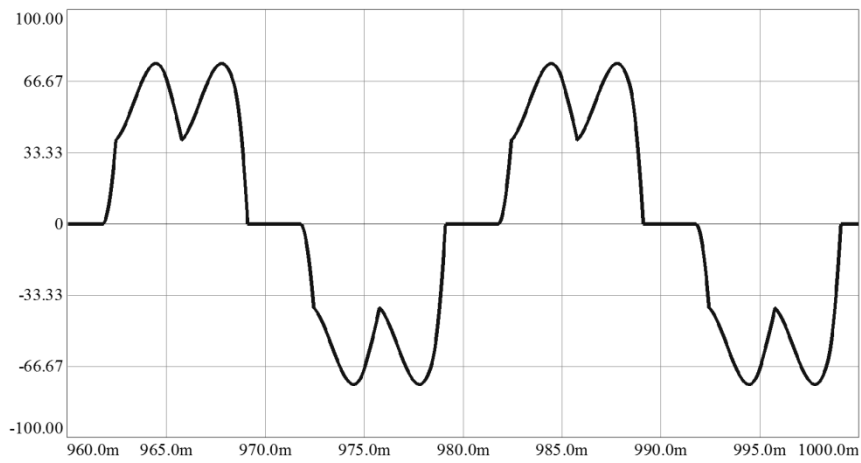


Figure 4.31 Line current of the 37 kW motor drive under constant power load (33.3 A /div, 5 ms/div).

4.5 Conclusion

In this chapter, the performance of the conventional drives under constant torque load, fan load, and constant power load is investigated. The conventional motor drives equipped with high C_{dc} capacitor and filter inductors yield satisfactory performance in terms of bus voltage, input power quality, and motor motion quality. The results show that the performance of the conventional motor drives does not change for the cases that dc bus disturbance rejection applied and not applied, at both ac mains end and motor end. This is due to the fact that the bus voltage ripple is very low and the low magnitude 300 Hz ripple does not cause torque ripple on the motor. The dc bus disturbance rejection does not cause a degradation in the dc bus voltage stability as the stiffness of the dc bus is high due to high capacitance and energy storage. Since the line current waveform quality also depends on the bus voltage characteristics, no difference is observed between the line current distortion values with and without dc bus disturbance rejection. The stiff dc bus is also not affected from constant power load as expected. The next chapter investigates the performance of the motor drives with front end diode rectifier utilizing low C_{dc} dc bus capacitor under the same operating conditions with the conventional drive.

CHAPTER 5

INDUCTION MOTOR DRIVE WITH FRONT END DIODE RECTIFIER UTILIZING LOW CAPACITANCE DC BUS CAPACITOR

5.1 Using Low C_{dc} Film Capacitor Instead of High C_{dc} Electrolytic Capacitor

As mentioned in the previous chapters, the high capacitance electrolytic capacitors show high performance in decreasing the rectifier dc bus voltage ripple and by creating a stiff dc bus with high stability. Despite, they have high ESR which limits their operation lifetime to 5-10 years due to heating. They have very large size causing a bulky drive system. In addition, the high capacitance causes high harmonic distortion in line current and the use of large inductor filters becomes inevitable, which increases the cost and size of the drive. Moreover, the high capacitance causes large inrush currents in the circuit, which forces the use of inrush current limiters or pre-charge circuits, which further adds to the cost of the system.

Because of these drawbacks of high capacitance electrolytic capacitors, use of low capacitance film capacitors has been attracting the attention of many researchers and manufacturers. As mentioned in Chapter 3, the film capacitors offer much lower ESR values than electrolytic capacitors, which makes them withstand higher ripple currents and offer very long lifetime compared to electrolytic ones. Since the capacitance is low, there is no need for pre-charge circuit which decreases the cost of the design. Due to low capacitance, the continuity of the line current is increased, decreasing THD_{ig} . This fact makes it possible to use a smaller, or even no inductor filter other than the line inductance, to decrease the THD_{ig} to an acceptable level, which decreases the cost and size of the system significantly. So, it can be possible to design compact and integrated motor drives with lower cost than the conventional drives by using low capacitance film capacitors.

Despite its various advantages over electrolytic ones, the small film capacitors have limited energy storage and the dc bus voltage is not stiff. So, the stability of the dc bus is reduced and it becomes more prone to voltage oscillations, which may degrade the overall drive performance at both ac line and motor end. This makes it necessary to conduct a detailed stability analysis of the circuit for a proper design and understanding of appropriate dc bus voltage stabilization control methods.

5.2 Stability Analysis Using Equivalent Rectifier Model

The circuit of three phase diode rectifier with low C_{dc} small dc bus capacitor can be simplified by using a single phase equivalent circuit [33] as in Figure 5.1.

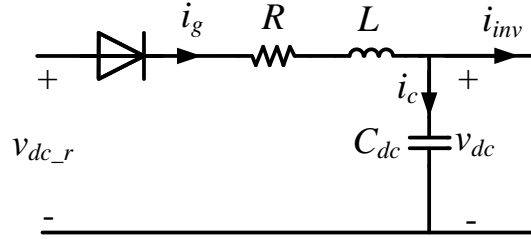


Figure 5.1 Equivalent circuit of three phase diode rectifier.

In Figure 5.1, v_{dc_r} is the ideal rectifier output voltage, i_g is the input current, R and L are the total effective resistance and inductance of the circuit, i_c is the current drawn by dc bus capacitor, C_{dc} shows the dc bus capacitor, v_{dc} is the dc bus voltage, and i_{inv} is the input current of the inverter. The parameters are formulated in (5.1) and (5.2), where R_g is the ac line resistance per phase, R_{dc} is the dc link resistance, $3\omega_{eg}L_g/\pi$ is the voltage drop due to commutation [34], L_g is the line inductance per phase, L_{ac} is the ac line reactor inductance per phase and L_{dc} is the dc link inductance.

$$R = 2R_g + 2R_{dc} + 3\omega_{eg}L_g/\pi \quad (5.1)$$

$$L = 2L_g + 2L_{ac} + L_{dc} \quad (5.2)$$

The terminal voltage equations and capacitor current can be written by (5.3) and (5.4).

$$v_{dc,r} = Ri_g + L \frac{di_g}{dt} + v_{dc} \quad (5.3)$$

$$i_c = C \frac{dv_{dc}}{dt} = i_g - i_{inv} \quad (5.4)$$

The undamped natural frequency of the equivalent circuit is given by (5.5) and damping ratio is given by (5.6).

$$\omega_n = \frac{1}{\sqrt{LC_{dc}}} \quad (5.5)$$

$$\zeta = \frac{1}{2\omega_n} \frac{R}{L} \quad (5.6)$$

In conventional rectifiers, due to high C_{dc} dc bus capacitor and high inductance filter inductors, the resonant frequency of the dc link is already low. Conventionally, the dc link inductance and capacitance is selected to filter out the 300 Hz voltage ripple from the dc bus voltage. Hence the undamped natural frequency is chosen less than 300 Hz, $\omega_n < 6\omega_{eg}$, [31]. Keeping ω_n lower than $6\omega_{eg}$ also prevents a possible resonance in the dc link LC circuit due to any harmonic component of the dc bus voltage around $6\omega_{eg}$ or its multiples.

Using a low C_{dc} capacitor on the dc bus increases the natural frequency of the dc link. Hence, if the resonance frequency ω_n is around one of the high amplitude bus voltage ripple harmonics of $6\omega_{eg}$, the risk of resonance may arise and the stability may be lost easily. To prevent such a situation, the sizing algorithm given in [31] can be used in which the low capacitance is intentionally selected such that the dc link resonant frequency is much higher than the critical region of $6\omega_{eg}$, $6\omega_{eg} \ll \omega_n$. In addition, the natural frequency ω_n is kept lower than the inverter switching frequency, ω_c , to prevent the injection of high frequency inverter switching harmonics to ac mains. Thus, the criterion for dc link dimensioning is given by (5.7) [31].

$$6\omega_{eg} \ll \omega_n < \omega_c \quad (5.7)$$

The dimensioning rule given in [31] can be analyzed in depth to investigate the effect of resonant frequency on the behavior of the rectifier. The dc bus voltage is composed of the dc component, dominant 300 Hz voltage ripple, and its harmonics. Thus, the ripple

components of the dc bus voltage can be considered as voltage sources connected to the input of the equivalent rectifier circuit. The harmonic component of the ripple voltage closest to the resonant frequency of the circuit is expected to cause an amplification of the dc bus voltage. Hence, the behavior of the equivalent circuit at different dc link resonant frequencies can be estimated using the results of this voltage excitation method at ripple voltage and its harmonics. For this purpose, the equivalent circuit is energized with model voltage sources with output voltages and frequencies equal to the amplitude and frequency of the ideal three-phase diode rectifier ripple voltage harmonics. The data obtained from the simulation is used to plot the variation of the input impedance seen by the rectifier (Z_{in}), peak to peak voltage ripple amplification on the dc bus (V_{dc_pp}), and the peak to peak input current magnitude of the circuit (I_{in_pp}) with the operating frequency, using [32]. By such an investigation, the resonant frequency resulting in the minimum dc bus voltage ripple amplification can be obtained and the parameters of the dc link components can be tuned for this frequency.

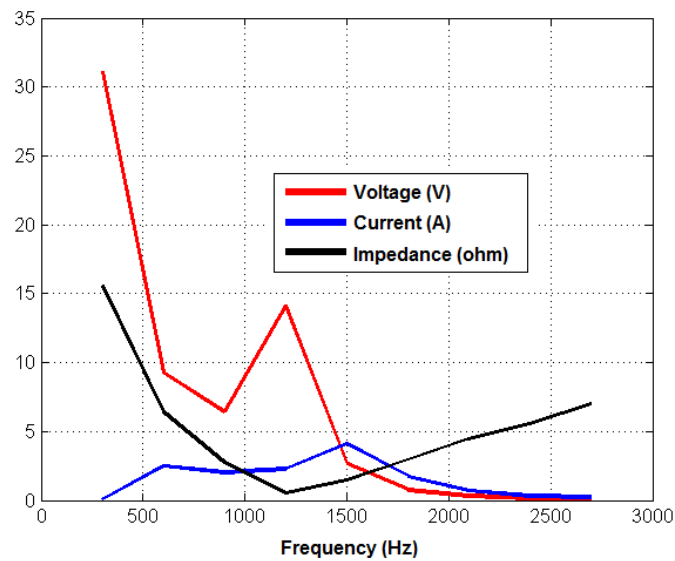


Figure 5.2 Equivalent rectifier model simulation results at dc bus ripple harmonic frequencies $P_{out}=2.2$ kW, $f_n=1.25$ kHz DC bus ripple voltage (red, 5V/div, 500 Hz/div), input current (blue, 5A /div, 500 Hz/div), input impedance (black, 5 ohm/div, 500 Hz/div).

Figure 5.2 shows the variation of dc bus pp ripple voltage amplification, input current, and equivalent input impedance for the equivalent rectifier model with resonant frequency of $f_n=1.25$ kHz. This resonant frequency stays between the 4th (1200 Hz) and 5th (1500 Hz) dc bus voltage ripple harmonics. As a result, the LC resonance is excited by the 4th and 5th dc bus voltage ripple harmonics and the bus voltage ripple amplification has a peak at 1.25 kHz, so does the input current. This is consistent with the expectations.

For the same output power, another circuit with resonant frequency of $f_n=2.5$ kHz is designed and simulated. This resonant frequency is intentionally selected close to the higher order bus voltage ripple harmonics whose amplitudes are lower compared to lower order ones. The LC circuit resonance is excited by the ripple harmonics closest to 2.5 kHz (8th/2400 Hz and 9th/2700 Hz). Compared to $f_n=1.25$ kHz case where the resonance is excited by the 4th and 5th voltage ripple harmonics, the dc bus ripple voltage and the input current amplification are lower in $f_n=2.5$ kHz case, as seen in Figure 5.3, since the amplitude of the 8th and 9th harmonics are lower than 4th and 5th ones.

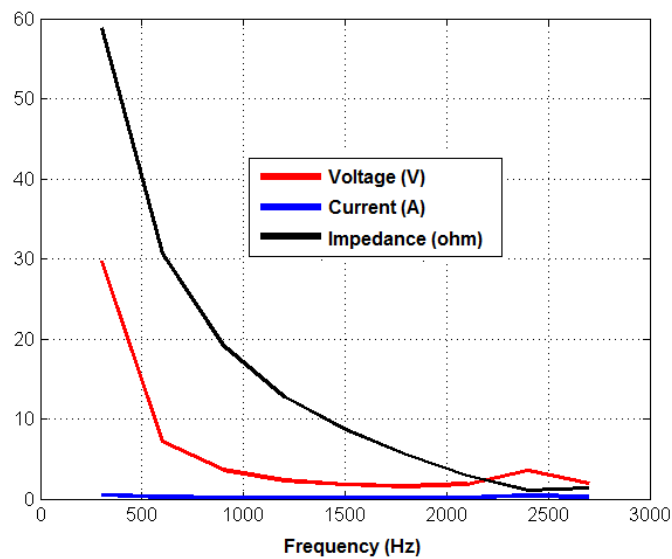


Figure 5.3 Equivalent rectifier model simulation results at dc bus ripple harmonic frequencies $P_{out}=2.2$ kW, $f_n=2.5$ kHz DC bus ripple voltage (red, 10 V/div, 500 Hz/div), input current (blue, 10A /div, 500 Hz/div), input impedance (black, 10 ohm/div, 500 Hz/div).

For the 37 kW output power, the same discussion applies. Figure 5.4 shows the circuit quantities with $f_n=1.576$ kHz and Figure 5.5 shows the one with $f_n=3.4$ kHz resonant frequencies.

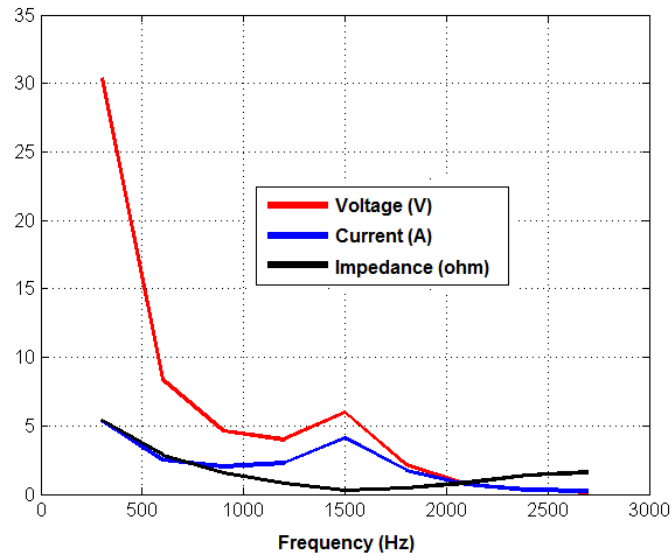


Figure 5.4 Equivalent rectifier model simulation results at dc bus ripple harmonic frequencies $P_{out}=37$ kW, $f_n=1.576$ kHz DC bus ripple voltage (red, 5 V/div, 500 Hz/div), input current (blue, 5 A /div, 500 Hz/div), input impedance (black, 5 ohm/div, 500 Hz/div).

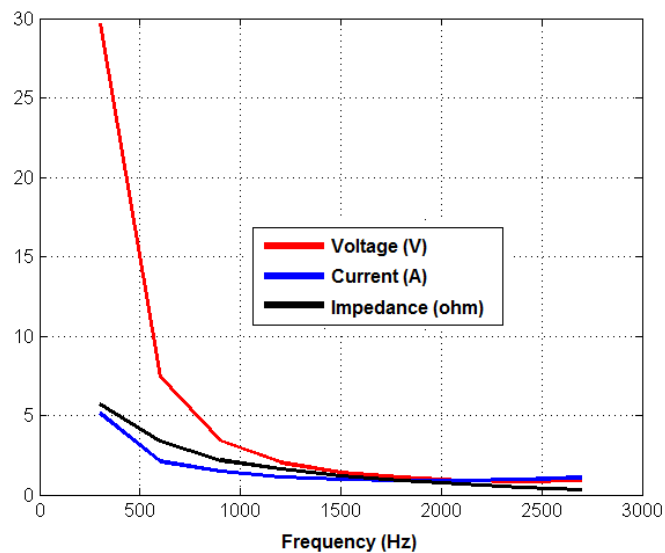


Figure 5.5 Equivalent rectifier model simulation results at dc bus ripple harmonic frequencies $P_{out}=37$ kW, $f_n=3.4$ kHz DC bus ripple voltage (red, 5 V/div, 500 Hz/div), input current (blue, 5 A /div, 500 Hz/div), input impedance (black, 5 ohm/div, 500 Hz/div).

As expected, the circuit with $f_n=3.4$ kHz (f_n close to 11th dc bus ripple voltage harmonics) has lower dc bus voltage and input current amplification compared to $f_n=1.576$ kHz circuit (f_n close to 5th dc bus ripple voltage harmonics), due to excitation of resonance by lower amplitude-higher order ripple voltage components. As deduced from the simulation results, selection of a dc link resonant frequency close to the higher order voltage ripple harmonics of 300 Hz, approximately around 8th-11th ones, yields minimum amplification of resonant ripple voltage and input current.

Other than selection of a proper resonant frequency, a more detailed analysis of the stability can be carried on using a small signal linearized model of the circuit, by using the modeling and formulation given in [15]. The inverter input current can be expressed by (5.8), where P_L is the power drawn by the motor.

$$i_{inv} = \frac{P_L}{v_{dc}} = \frac{P_L}{v_{dc0} + \tilde{v}_{dc}} \approx \frac{P_L}{v_{dc0}} \left(1 - \frac{\tilde{v}_{dc}}{v_{dc0}}\right) \quad (5.8)$$

In (5.8), v_{dc0} is the mean dc link voltage and \tilde{v}_{dc} is the small signal deviation on it. The equation on the right side is an approximation made by the first order MacLaurin series expansion [33]. Putting (5.8) into (5.3) and (5.4) the characteristic equation of the circuit is derived [33] as given by (5.9).

$$s^2 + \left(\frac{R}{L} - \frac{P_L}{Cv_{dc0}^2}\right)s + \frac{1}{LC} \left(1 - \frac{RP_L}{v_{dc0}^2}\right) \quad (5.9)$$

In (5.9), $\frac{RP_L}{v_{dc0}^2} \ll 1$ and can be neglected. For stability, the coefficients of the characteristic equation must be positive leading to the relation given by (5.10), where P_{nom} is the rated power.

$$\frac{C}{P_{nom}} > \frac{L}{Rv_{dc0}^2} \quad (5.10)$$

The stability criterion can be expressed as in (5.11) where $\lambda = \left(\frac{L}{Rv_{dc0}^2}\right) / \left(\frac{C}{P_{nom}}\right)$.

$$\lambda < 1 \quad (5.11)$$

Thus, a rectifier circuit obeying (5.11) is stable for normal operating conditions [33]. According to this formula, increasing the L/C ratio of the circuit decreases stability.

To see the effect of the L/C ratio on the stability of the low C_{dc} motor drives, two types of circuits are designed; one without a dc link inductor and the other one utilizing a dc link inductor with inductance of approximately 8 times that of the line inductance. For the circuit without dc link inductor, the dc bus capacitance is selected so that the dc link resonance frequency is tuned close to the higher order 8th-11th bus voltage ripple harmonics and kept lower than the switching frequency, according to relation given by (5.7). Then, the simulation results of the low C_{dc} motor drives equipped with dc link inductors are given and the results are compared.

5.3 Design of Low C_{dc} Motor Drive without DC Link Inductor

Table 5.1 includes the circuit parameters of the low C_{dc} 2.2 kW and 37 kW motor drives without dc link inductor.

Table 5.1 Circuit parameters of the low C_{dc} motor drives without dc link inductor.

Parameter	2.2 kW motor drive	37 kW motor drive
Line inductance, L_g (mH)	0.25	0.0148
Line resistance, R_g (m Ω)	125.0	0.0074
AC line reactor, L_{ac} (mH)	-	-
DC link inductor, L_{dc} (mH)	-	-
DC bus capacitor, C_{dc} (μ F)	8	72
DC Link resonant frequency, ω_n (rad/s)	$2\pi.2516$	$2\pi.3447$
Inverter switching frequency, f_c (kHz)	10	10
PWM type	SVPWM	SVPWM

For the 2.2 kW motor drive, an 8 μ F dc bus capacitor results in $f_n=2.516$ kHz dc bus resonant frequency with the line inductance of 0.25 mH per phase. Likewise, using a 72 μ F dc bus capacitor for the 37 kW motor drive circuit results in $f_n=3.447$ kHz with the line

inductance of 14.8 μH per phase. Using a switching frequency of $f_c=10$ kHz, (5.7) is satisfied. The same motors and PI controllers used for conventional drive simulations are used given in Table 5.2.

Table 5.2 Controller parameters of the low C_{dc} motor drives without dc link inductor.

Current regulator parameters	2.2 kW motor drive	37 kW motor drive
Proportional gain, K_{pi}	250	22.5
Integral gain, K_{ii}	20000	200
Current regulator bandwidth, f_{rc} (Hz)	1000	1000
Speed regulator parameters	2.2 kW motor drive	37 kW motor drive
Proportional gain, K_{ps}	0.075	2
Integral gain, K_{is}	1.1	80
Speed regulator bandwidth, f_{rs} (Hz)	16	16

5.4 Simulation Results of the Low C_{dc} Motor Drives without DC Link Inductor

The motor drives with low C_{dc} dc link capacitor are simulated for constant torque load and variable torque load (fan load) cases. Before analyzing these results, the instability of the dc link with low C_{dc} capacitor caused by negative impedance effect of constant power load is illustrated by some simulations. Figure 5.6 shows the dc bus voltage for the 2.2 kW motor drive operating under constant power load.

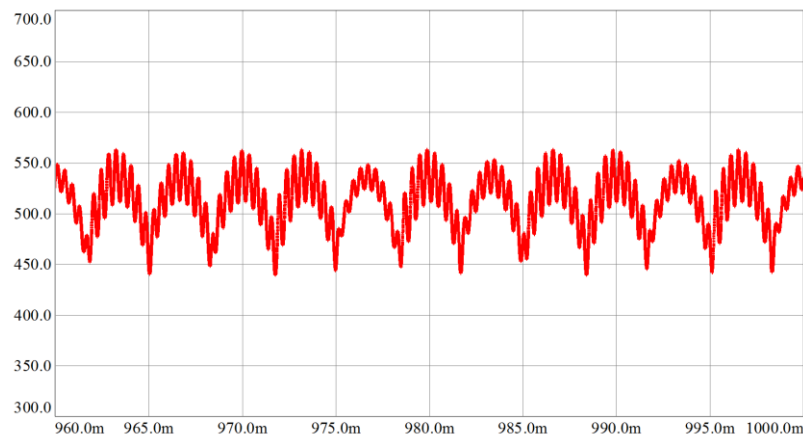


Figure 5.6 DC bus voltage of the 2.2 kW low C_{dc} motor drive operating under constant power load (50 V/div, 5 ms/div).

As expected, the dc link is unstable and the resonant voltage component on dc link is amplified. Figure 5.7 shows the line current waveform for constant power load operation. The line current also suffers from this instability and it has THD_{ig} of 71.5 % and PF is 0.811. This fact shows that the low C_{dc} motor drive can easily lose its stability under constant power load operation.

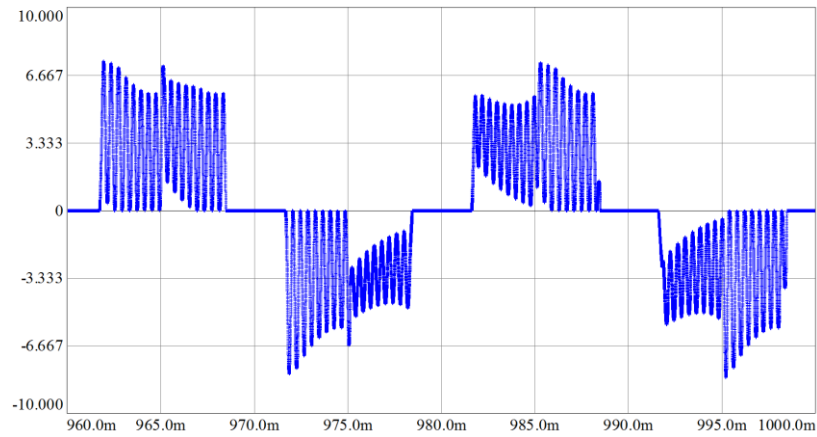


Figure 5.7 Line current of the 2.2 kW low C_{dc} motor drive operating under constant power load (3.33 A /div, 5 ms/div).

Figure 5.8 shows the dc bus voltage and Figure 5.9 shows the line current waveforms for the 37 kW drive under constant power load.

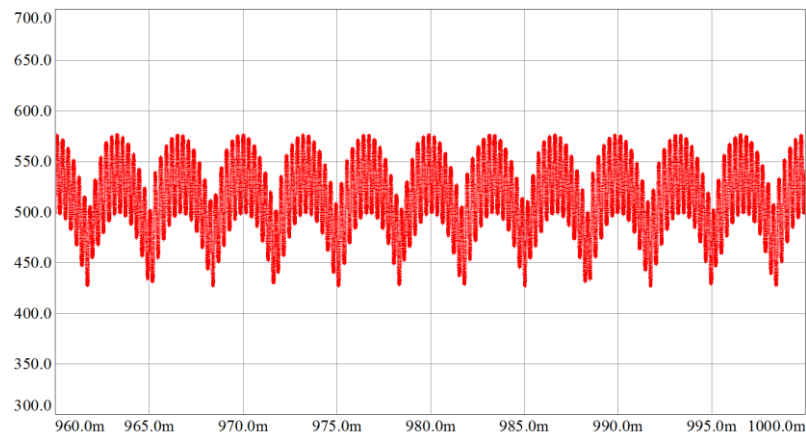


Figure 5.8 DC bus voltage of the 37 kW low C_{dc} motor drive operating under constant power load (50 V/div, 5 ms/div).

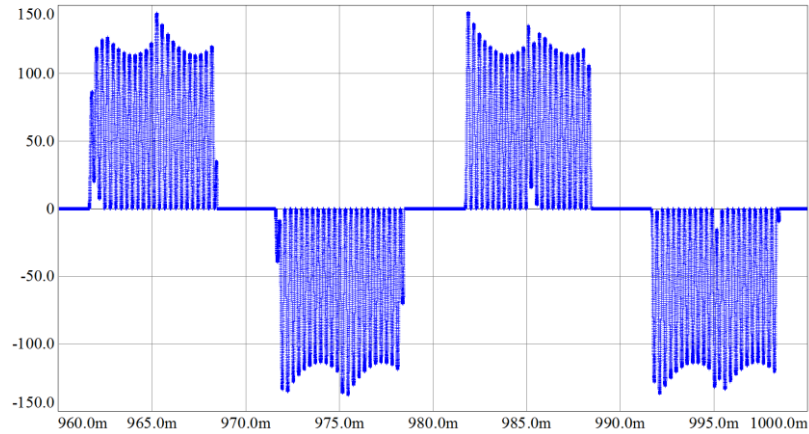


Figure 5.9 Line current of the 37 kW low C_{dc} motor drive operating under constant power load (50 A /div, 5 ms/div).

The impact of constant power on the dc link voltage is much more visible for the 37 kW drive compared to the 2.2 kW drive. The resonant voltage amplification on dc bus is increased. The line current has THD_{ig} of 83 % and PF is 0.766.

5.4.1 Constant Torque Load Operation Simulation Results

The simulations are conducted for both high modulation index ($M_i=0.83$) and low modulation index ($M_i=0.46-0.47$) to investigate the performance of the drives. The waveforms are provided for $M_i=0.83$ operations and the simulation data of the low M_i operation are given in tables in Chapter 6. The 2.2 kW motor is accelerated up to 1400 rpm at 13 N.m (1.9 kW/~87 % load) and the 37 kW motor to 1100 rpm at 230 N.m (26.5 kW/~71 % load) staying in the linear modulation region of the inverter.

5.4.1.1 2.2 kW Motor Drive Constant Torque Load Operation without DC Bus Disturbance Rejection

Figure 5.10 shows the motor acceleration, the d-q axis current variations and torque of the 2.2 kW motor under constant torque load. There is apparently no performance difference as compared to conventional drives for the start-up of the drive. The speed command is successfully tracked and motor reaches set speed without any instability. The main

difference between the low C_{dc} and conventional motor drives is expected to be clear on steady state dc bus voltage, line current, and motor torque waveforms.

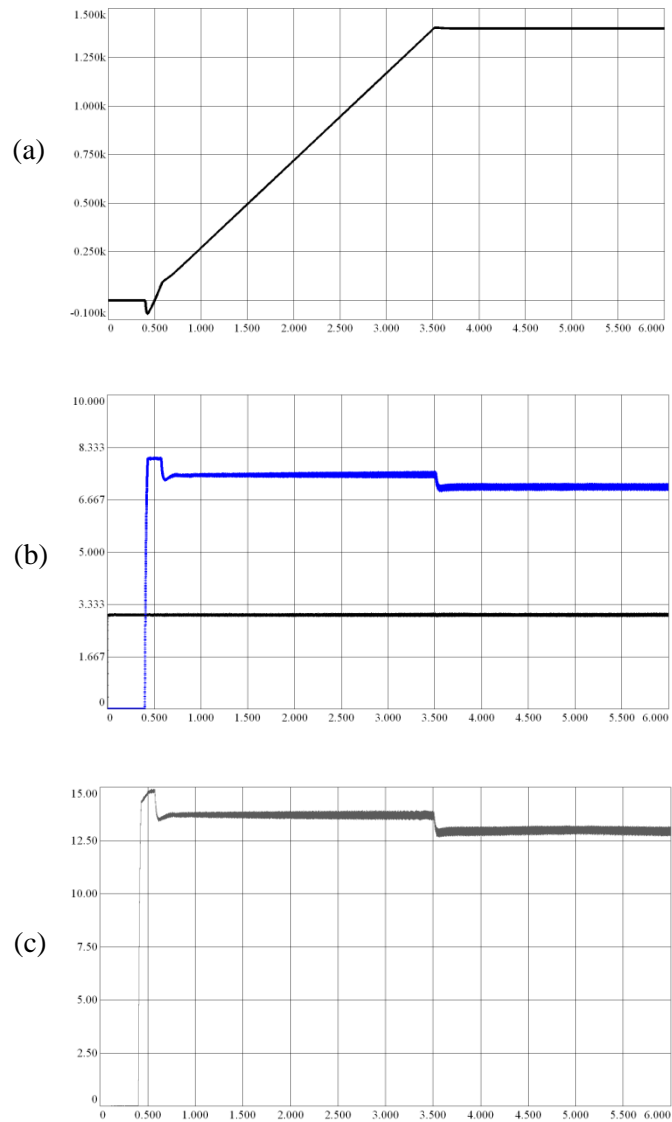


Figure 5.10 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor, without dc bus disturbance rejection (a) speed (250 rpm/div, 0.5 s/div), (b) d axis current (black) and q axis current (blue) (1.67 A/div, 0.5 s/div), (c) motor torque (2.5 N.m/div, 0.5 s/div).

Figure 5.11 shows the dc bus voltage waveform of the 2.2 kW drive. As expected, the dc bus voltage has six pulse voltage ripple with 300 Hz ripple voltage harmonics and its

multiples, as seen in the harmonic spectrum in Figure 5.12. In addition, the bus voltage includes the resonant frequency component around 2.5 kHz.

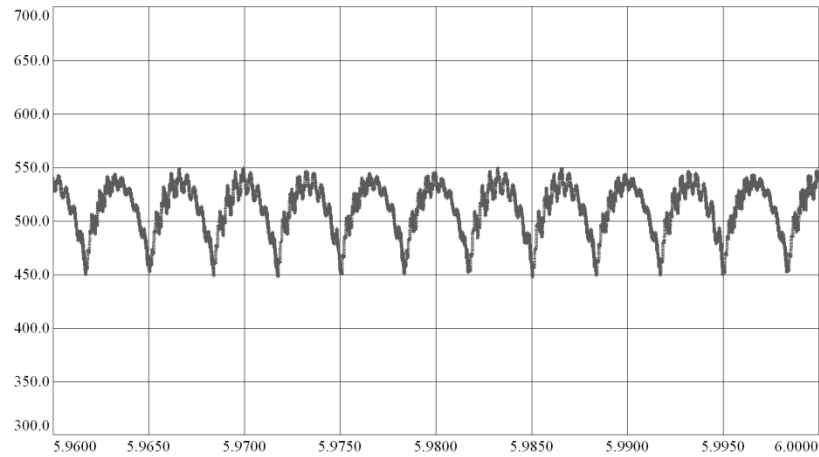


Figure 5.11 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (50 V/div, 5 ms/div).

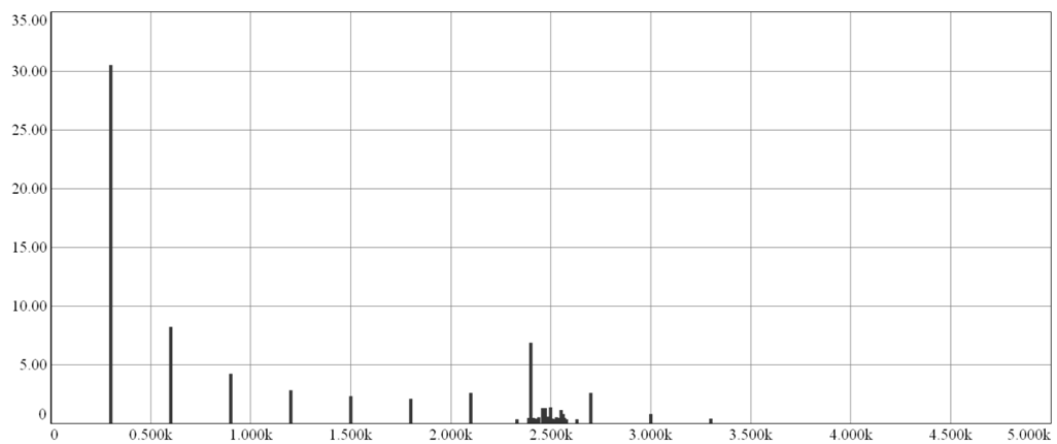


Figure 5.12 Harmonic spectrum of dc bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (5 V/div, 500 Hz/div).

Figure 5.13 shows the instantaneous variation of dc bus voltage and the reference voltage generated by the current regulator on two-axis stationary frame. The figure gives a clear

picture of dc bus voltage variation and the voltage demand from the inverter. As explained in detail in Chapter 4, the inverter voltage reference (red) shows the instantaneous voltage demand from the dc bus and the output voltage limit circle (blue) shows the available voltage limit depending on instantaneous dc bus voltage. The 300 Hz bus voltage ripple is clearly seen on Figure 5.13 on the blue circle with a periodic increase and decrease in the radius of the circle, where the period is the time corresponding to 300 Hz (3.3 ms). The voltage reference circle (red) interestingly lost its circle shape and has sharp corners unlike the case for conventional drives in Chapter 4. This can be explained by the fact that the voltage demand of the drive is high due to high speed operation and under such a dc bus voltage with high ripple, the current regulator starts to saturate the output voltage reference to be able to synthesize the required voltage. This can be understood more clearly from Figure 5.14 which shows the voltage circles when the operation speed is lowered to 1000 rpm. The total voltage demand is decreased compared to Figure 5.13 so the reference voltage (inner circle radius) is lowered. Since the inverter voltage reference is well below the available limit, the current regulator does not show any sign of saturation. In addition, the closed loop current regulator with sufficient bandwidth rejects the 300 Hz dc bus voltage ripple on the dc bus voltage to synthesize a pure dc q axis current i_{qs}^e .

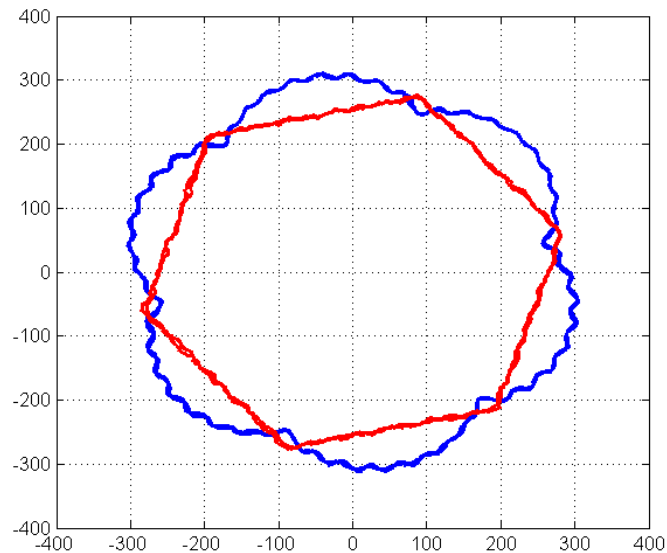


Figure 5.13 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive operating at 1400 rpm 13 N.m without dc bus disturbance rejection (100 V/div, 100 V/div).

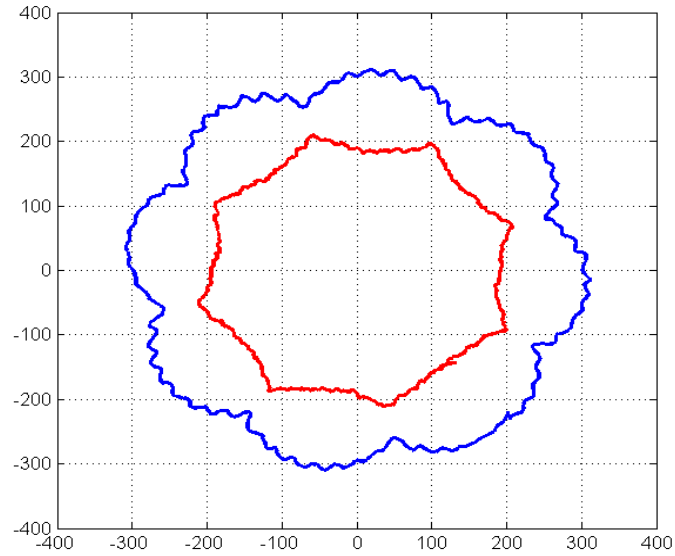


Figure 5.14 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive operating at 1000 rpm 13 N.m without dc bus disturbance rejection (100 V/div, 100 V/div).

The current regulator increases (decreases) the reference voltage amplitude when the bus voltage decreases (increases). This can be seen in time domain waveforms in Figure 5.15 which illustrates the output of the q axis current regulator (q axis reference voltage) V_{qs}^e and the dc bus voltage waveform for $f_{rc}=1$ kHz bandwidth current regulator operation.

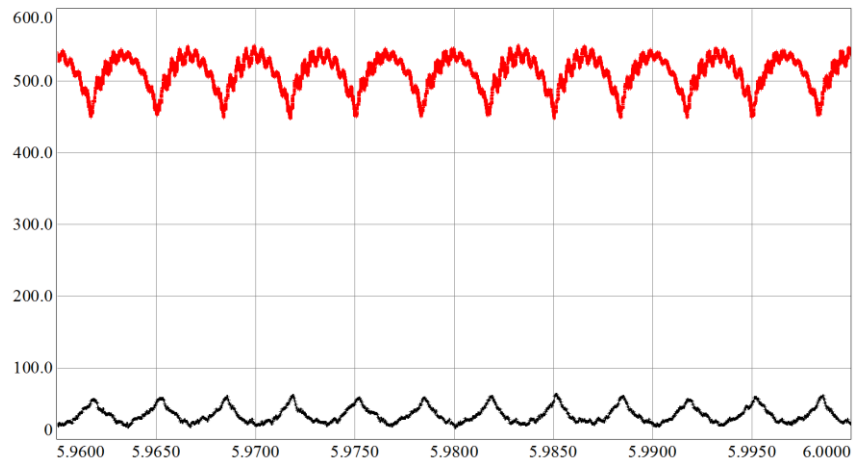


Figure 5.15 DC bus voltage (red) and V_{qs}^e (black) of 2.2 kW low C_{dc} motor drive $f_{rc}=1$ kHz (100 V/div, 5 ms/div).

As expected, the q axis current regulator generates a q axis voltage reference V_{qs}^e which opposes the dc bus voltage ripple. Despite this fact, the torque has still 300 Hz ripple component (0.4 N.m pp) as seen in Figure 5.16.

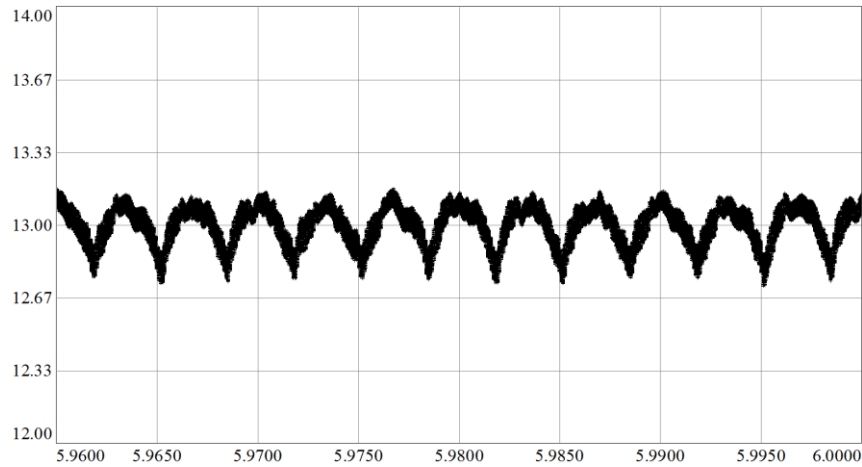


Figure 5.16 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection $f_{rc}=1$ kHz (0.33 N.m/div, 5 ms/div).

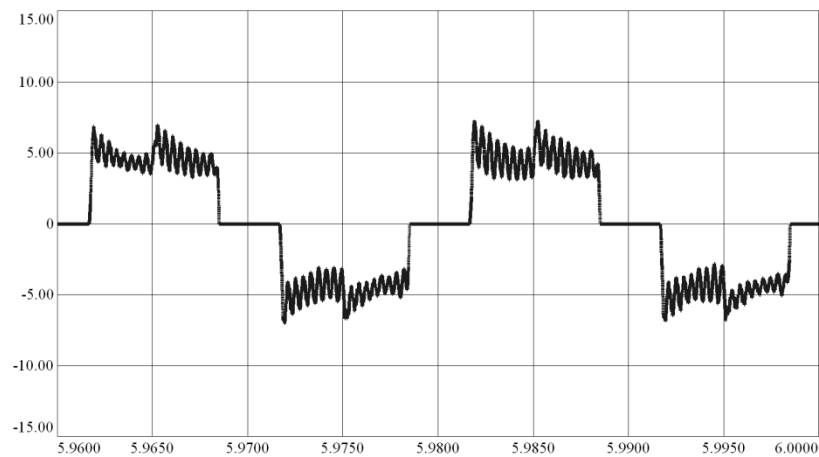


Figure 5.17 The line current waveform of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (5 A/div, 5 ms/div).

Figure 5.17 shows the line current waveform of the drive. The line current is expected to carry 5th, 7th, 11th, and 13th line current harmonics due to 6 pulse voltage ripple. In addition, the dc bus high frequency resonance is also seen on the waveform which is verified by the spectrum in Figure 5.18.

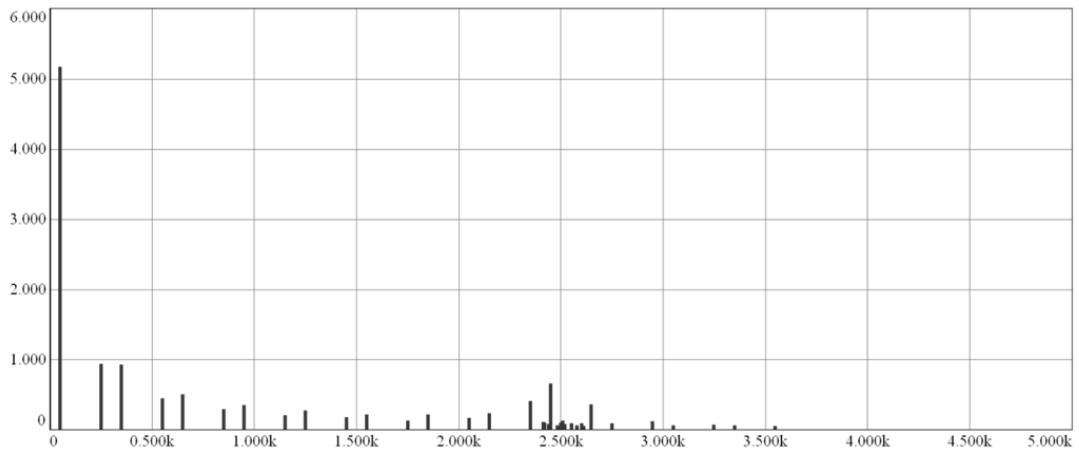


Figure 5.18 Harmonic spectrum of line current of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (1 A/div, 500 Hz/div).

To evaluate the effect of closed loop operation and current regulator bandwidth on the torque, a regulator with $f_{rc}=100$ Hz and an open loop drive operated with constant V/f method is simulated under same load condition. The expectation is a reduction in response time of the regulator due to low bandwidth and sluggish response in constant V/f control.

Figure 5.19 shows the regulator output and dc bus voltage waveform for the vector controlled drive with $f_{rc}=100$ Hz. Since the regulator bandwidth is below 300 Hz, the generated voltage reference lags the 300 Hz ripple of the dc bus voltage and cannot reject the voltage ripple disturbance. Compared to $f_{rc}=1$ kHz bandwidth current regulator operation, the motor torque ripple increases since the phase currents are affected from the 300 Hz component of the bus voltage. Figure 5.20 shows the steady state motor torque for $f_{rc}=100$ Hz operation. The pp torque ripple (0.8 N.m) is higher than of the $f_{rc}=1$ kHz operation, as expected.

Another investigation is carried on the open loop constant V/f method to compare the motor motion quality. The open loop control is effectively equivalent to closed loop control with low current regulator bandwidth.

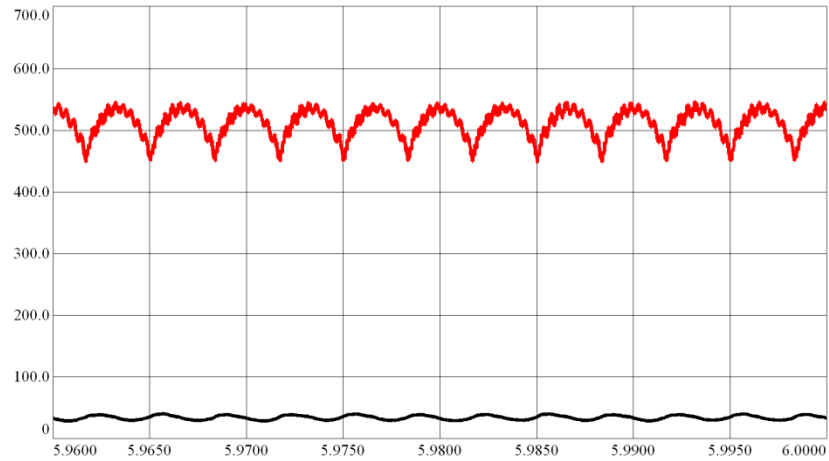


Figure 5.19 DC bus voltage (red) and V_{qs}^e (black) of 2.2 kW low C_{dc} motor drive operating under constant torque load without disturbance rejection for $f_{rc}=100$ Hz (100 V/div, 5 ms/div).

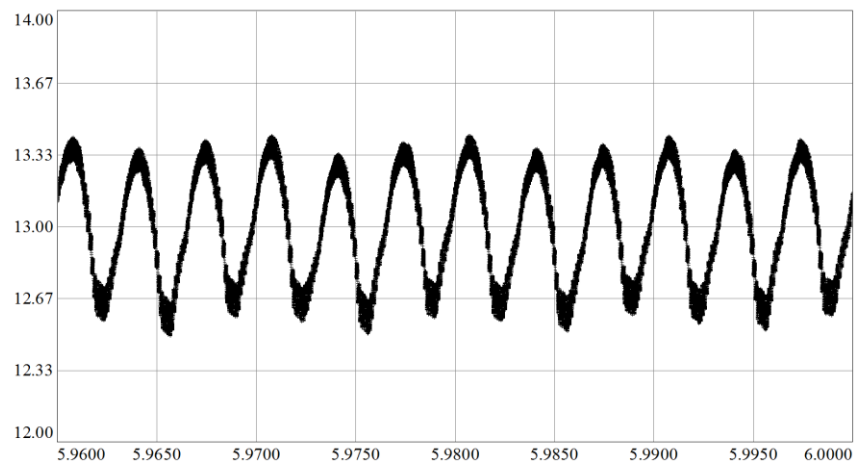


Figure 5.20 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection for $f_{rc}=100$ Hz (0.33 N.m/div, 5 ms/div).

Figure 5.21 shows the dc bus voltage for the constant V/f controlled motor at 1150 rpm operating speed. The bus voltage has no stability problem and waveform has six pulse shape. Figure 5.22 shows the steady state torque for the same simulation. The pp torque ripple (2 N.m) is nearly five times that of the vector controlled drive with $f_{rc}=1$ kHz as expected.

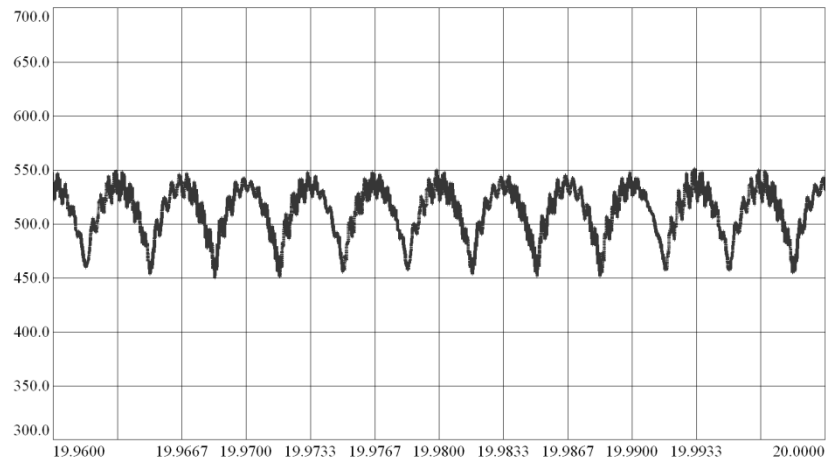


Figure 5.21 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load with constant V/f method without dc bus disturbance rejection (50 V/div, 3.3 ms/div).

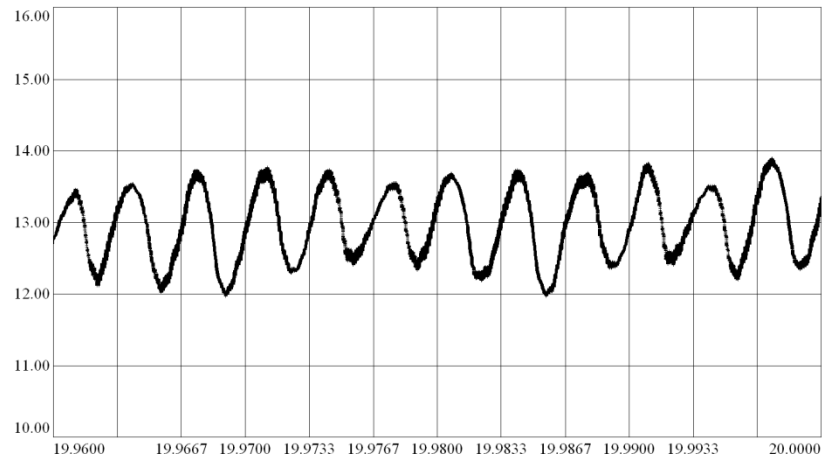


Figure 5.22 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load with constant V/f method without dc bus disturbance rejection (1 N.m/div, 3.3 ms/div).

5.4.1.2 2.2 kW Motor Drive Constant Torque Load Operation with DC Bus Disturbance Rejection

Since the start-up characteristics are the same, only the steady state waveforms are illustrated. Figure 5.23 illustrates the dc bus voltage waveform of the drive. The harmonic spectrum in Figure 5.24 illustrates the increased resonant component harmonic level more clearly. This is due to negative impedance effect to the disturbance rejection.

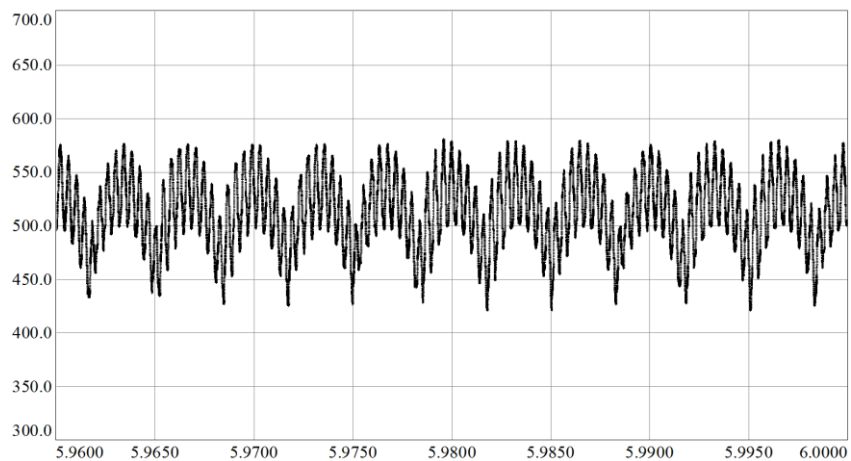


Figure 5.23 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (50 V/div, 5 ms/div).

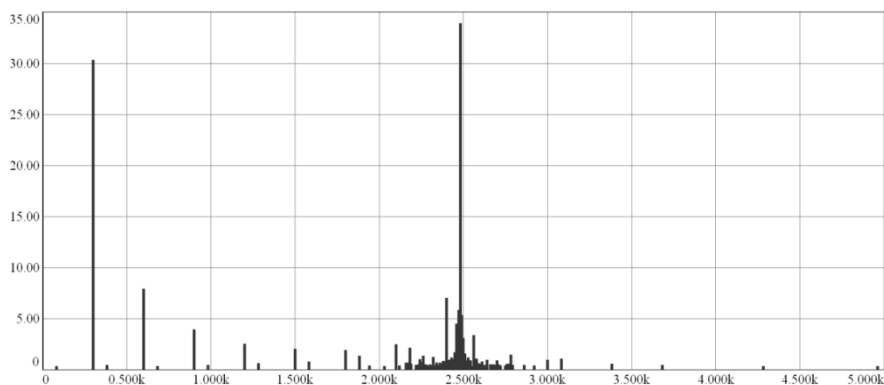


Figure 5.24 Harmonic spectrum of dc bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (5 V/div, 500 Hz/div).

The dc bus disturbance rejection affects the bus voltage negatively since it increases the negative impedance effect on the drive. This can be explained visibly via the use of voltage circles as done before. The negative impedance instability originates from the fact that the inverter is forced to generate an output voltage that exceeds the maximum available voltage the dc bus can provide. Hence, the inverter voltage demand circle interferes with the dc bus voltage limit circle and they start oscillating.

As seen in Figure 5.25, the inverter voltage demand and limit circle have intersections on some points, indicating that the voltage demand of the inverter is around the limits that can be supplied by the dc bus voltage.

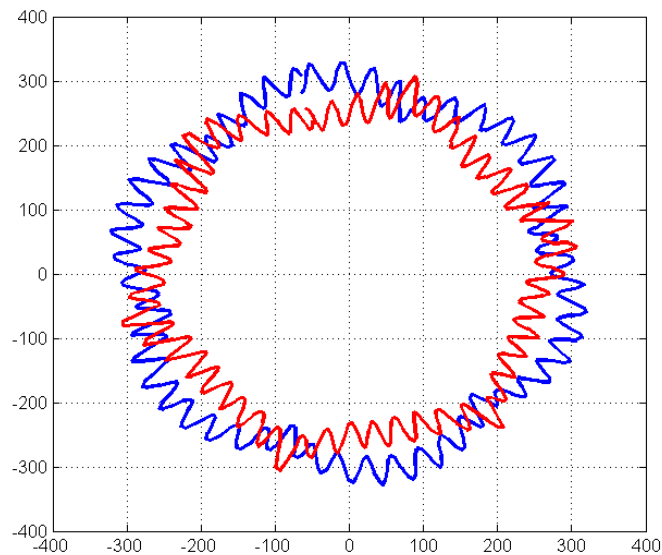


Figure 5.25 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive operating at 1400 rpm 13 N.m with dc bus disturbance rejection (100 V/div, 100 V/div).

When the motor is operated at a higher modulation index, the voltage demand exceeds the available limit at some points. This is illustrated in Figure 5.26 where the voltage demand from SFCR and the available voltage limit interfere at 1550 rpm operating speed.

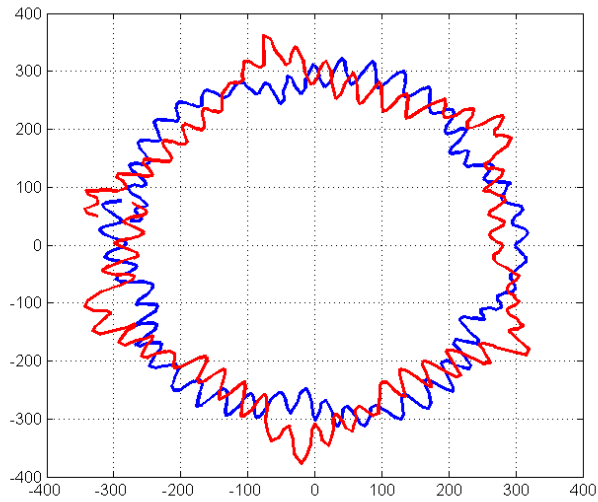


Figure 5.26 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive operating at 1550 rpm 13 N.m with dc bus disturbance rejection (100 V/div, 100 V/div).

Figure 5.27 shows the dc bus voltage and q axis voltage reference V_{qs}^e for the 2.2 kW constant torque load drive with disturbance rejection.

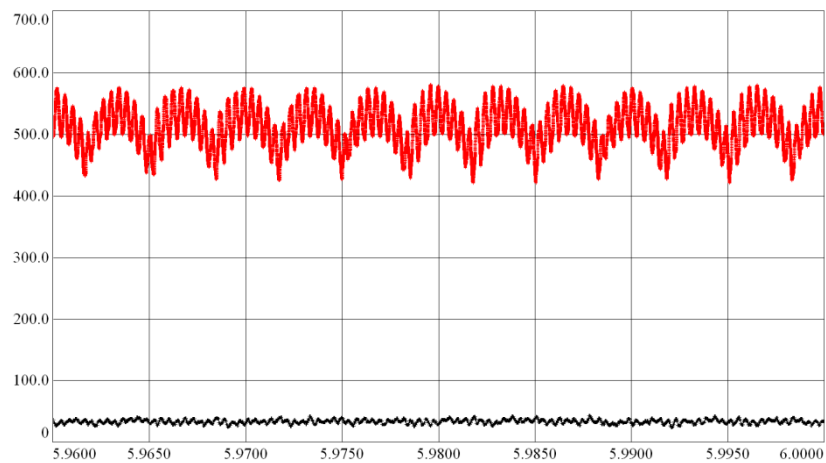


Figure 5.27 DC bus voltage (red) and V_{qs}^e (black) of 2.2 kW low C_{dc} motor drive operating under constant torque load with disturbance rejection $f_{rc}=1$ kHz (100 V/div, 5 ms/div).

For this case, the V_{qs}^e does not contain 300 Hz voltage ripple rejection component since the 300 Hz ripple at the torque and I_{qs}^e is completely eliminated by disturbance rejection. Since the I_{qs}^e feedback to the SFCR is dc, the resultant output V_{qs}^e becomes dc.

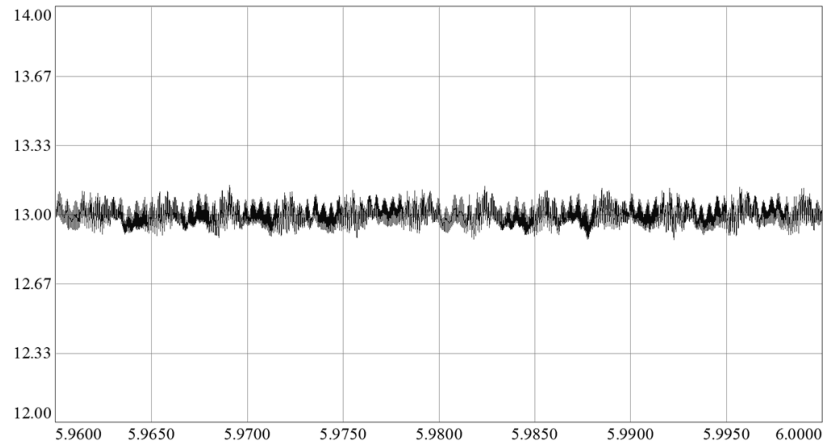


Figure 5.28 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (0.33 N.m/div, 5 ms/div).

The line current has high distortion (Figure 5.29) due to disturbance rejection.

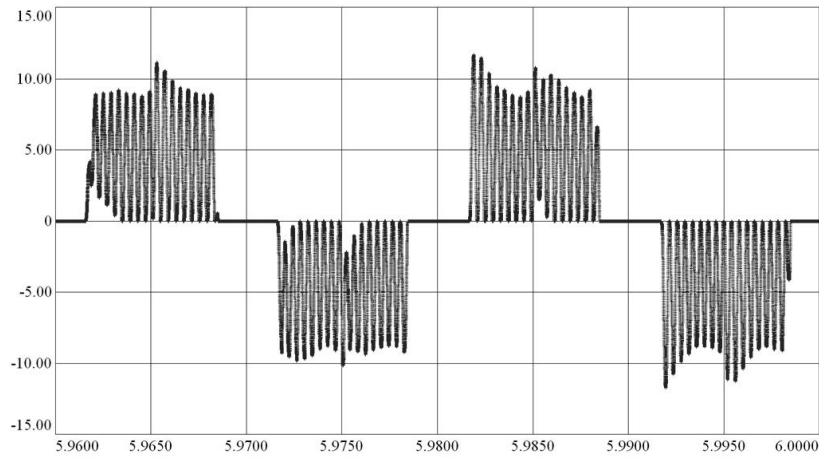


Figure 5.29 The line current waveform of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (5 A/div, 5 ms/div).

The harmonic spectrum in Figure 5.30 shows the increased resonant components more clearly.

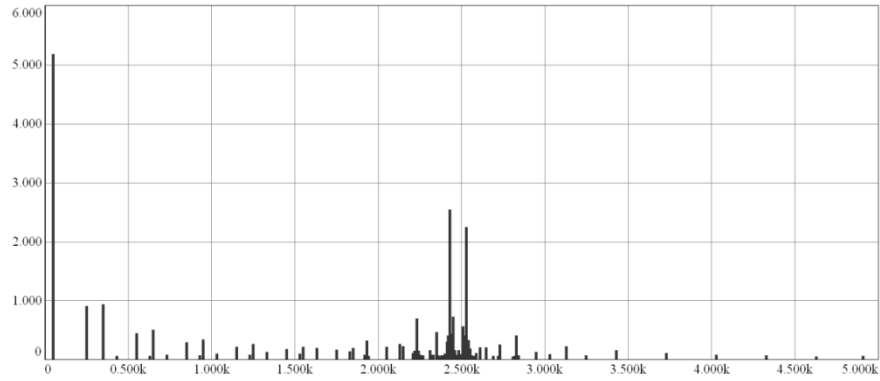


Figure 5.30 Harmonic spectrum of line current of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (1 A/div, 500 Hz/div).

The effect of dc bus disturbance rejection is tested at $f_{rc}=100$ Hz with vector control and by open loop constant V/f method cases. Figure 5.31 shows the dc bus voltage and SFCR output V_{qs}^e for $f_{rc}=100$ Hz operation.

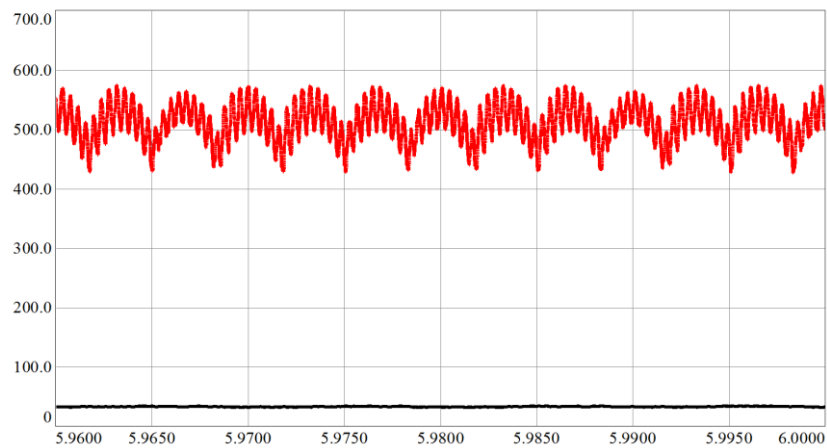


Figure 5.31 DC bus voltage (red) and V_{qs}^e (black) of 2.2 kW low C_{dc} motor drive operating under constant torque load with disturbance rejection $f_{rc}=100$ Hz (100 V/div, 5 ms/div).

The dc bus voltage oscillations are increased due to disturbance rejection as expected. The V_{qs}^e has dc characteristics due to disturbance rejection but the torque, as seen in Figure 5.32, has 300 Hz ripple although not too much but higher than the case with dc bus disturbance rejection and $f_{rc}=1$ kHz case. This shows that the best torque ripple elimination can be obtained by both dc bus disturbance rejection and high bandwidth current controller.

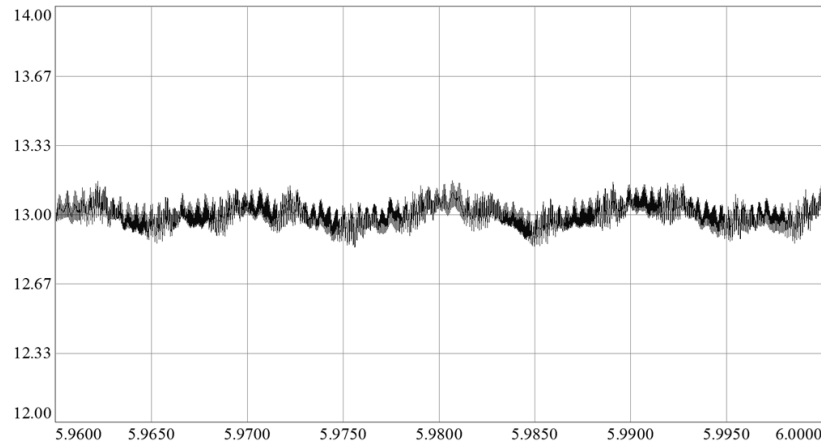


Figure 5.32 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection $f_{rc}=100$ Hz (0.33 N.m/div, 5 ms/div).

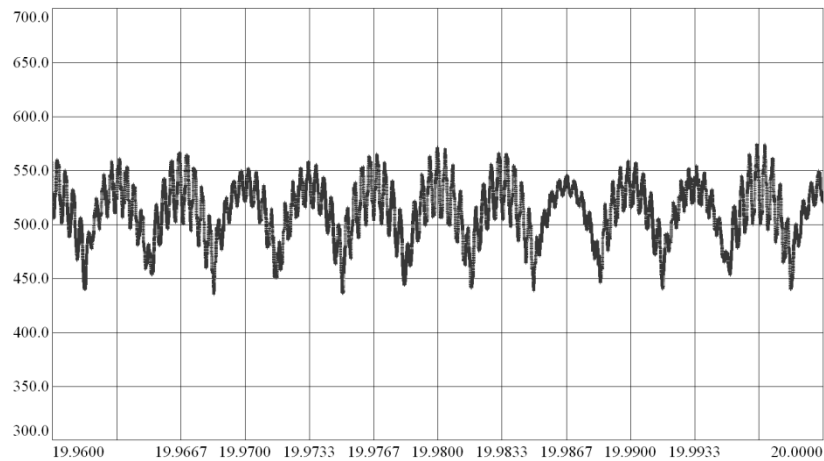


Figure 5.33 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load with constant V/f method with dc bus disturbance rejection (50 V/div, 3.3 ms /div).

Figure 5.33 shows the dc bus voltage waveform for the constant V/f controlled drive. As expected, the dc bus voltage oscillations are increased due to disturbance rejection.

Figure 5.34 shows the steady state torque of the machine with constant V/f control. The constant V/f generates higher torque ripple as observed in the case without dc bus disturbance rejection and higher compared to closed loop vector controlled case.

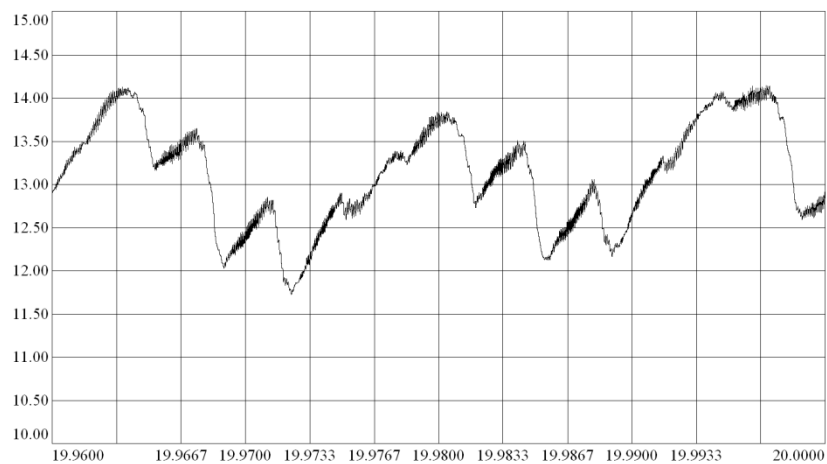


Figure 5.34 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load with constant V/f method with dc bus disturbance rejection (0.5 N.m/div, 3.3 ms/div).

5.4.1.3 37 kW Motor Drive Constant Torque Load Operation without DC Bus Disturbance Rejection

The 37 kW motor is accelerated to 1100 rpm at 230 N.m constant torque load. Since the acceleration characteristic is similar to that of 2.2 kW motor drive except the steady state operating speed and torque, the waveforms are not given. Instead, the steady state dc bus voltage, motor torque, and line current waveforms are provided.

Figure 5.35 illustrates the dc bus voltage waveform for the drive at steady state. The bus voltage is stable with 300 Hz dominant ripple in addition to the resonant frequency components as seen in harmonic spectrum in Figure 5.36.

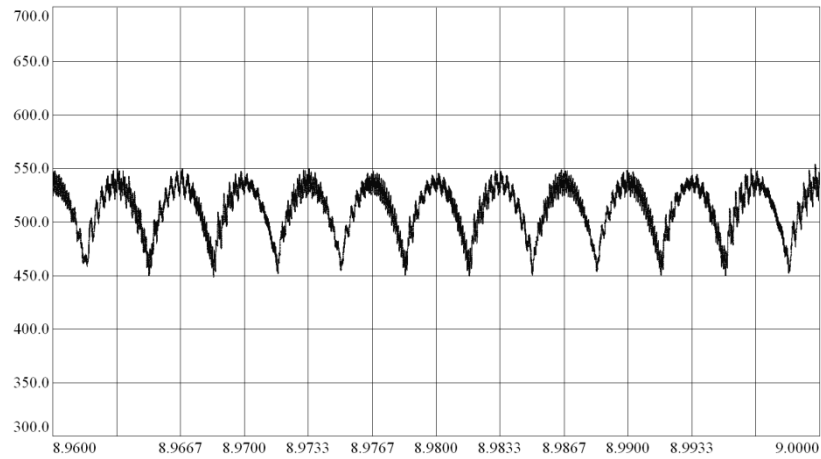


Figure 5.35 DC bus voltage of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (50V/div, 3.3 ms/div).

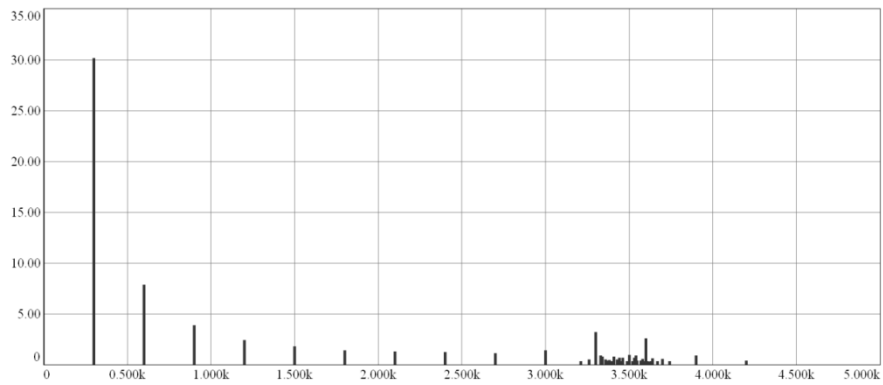


Figure 5.36 Harmonic spectrum of dc bus voltage of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (5 V/div, 500 Hz/div).

Figure 5.37 illustrates the motor torque at steady state. It includes 300 Hz ripple due to ripple in dc bus voltage.

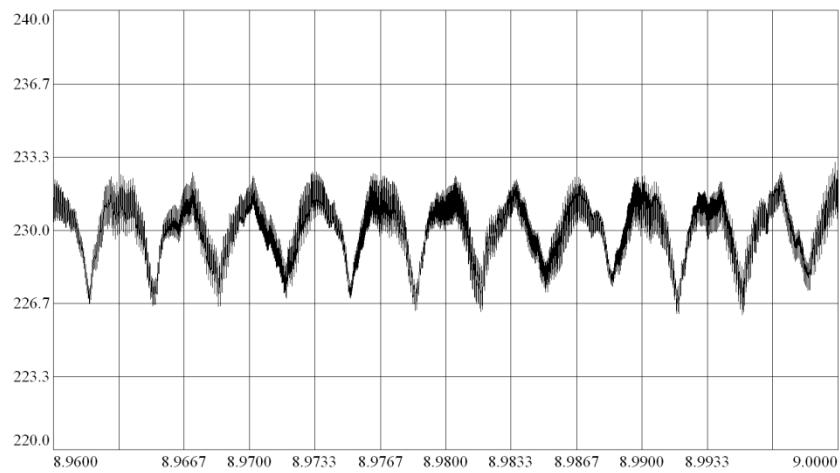


Figure 5.37 Motor steady state torque of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (3.3 N.m/div, 3.3 ms/div).

Figure 5.38 and Figure 5.39 shows the line current and spectrum respectively. The line current is close to the ideal rectangular waveform and it has the resonant frequency components around 3.4 kHz as expected.

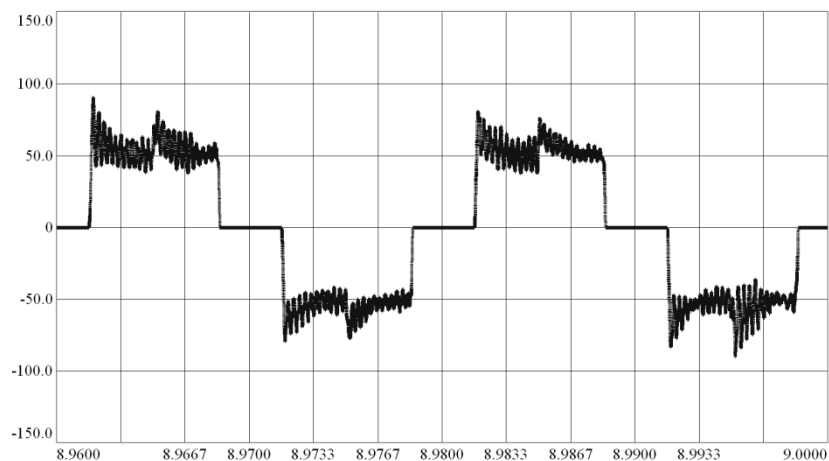


Figure 5.38 The line current waveform of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (50 A/div, 3.3 ms/div).

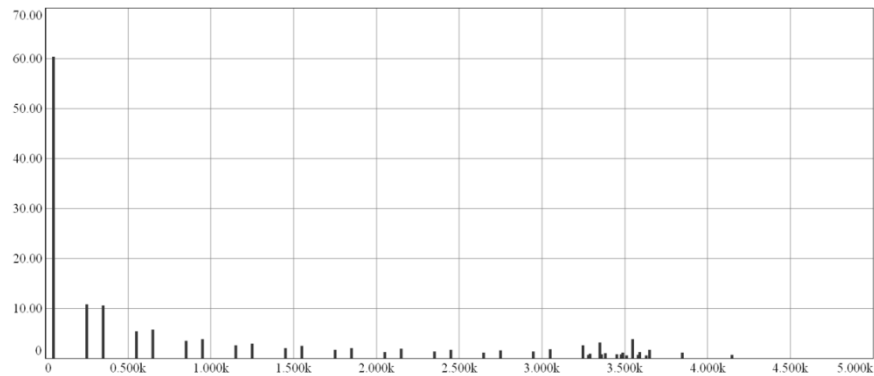


Figure 5.39 Harmonic spectrum of line current of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor without dc bus disturbance rejection (10 A/div, 500 Hz/div).

5.4.1.4 37 kW Motor Drive Constant Torque Load Operation with DC Bus Disturbance Rejection

The disturbance rejection is expected to eliminate the 300 Hz torque ripple as in 2.2 kW drive simulations. However, since it increases the negative impedance effect, the dc bus voltage faces higher amplitude oscillations at resonant frequency as seen in the dc bus voltage waveform in Figure 5.40 and corresponding harmonics spectrum in Figure 5.41.

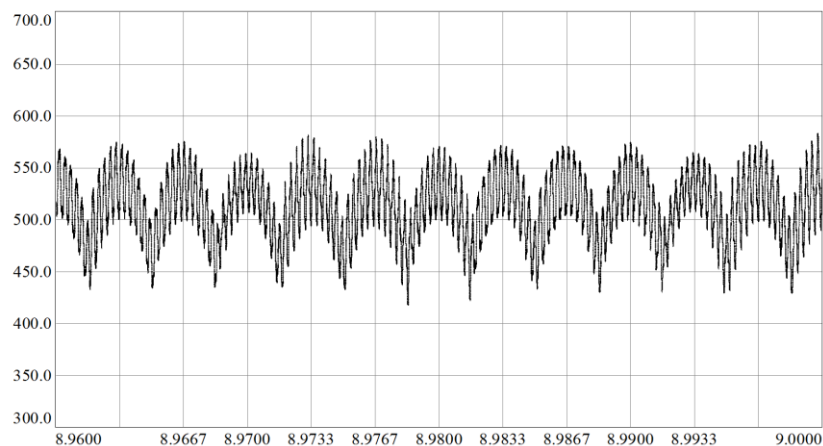


Figure 5.40 DC bus voltage of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (50 V/div, 3.3 ms/div).

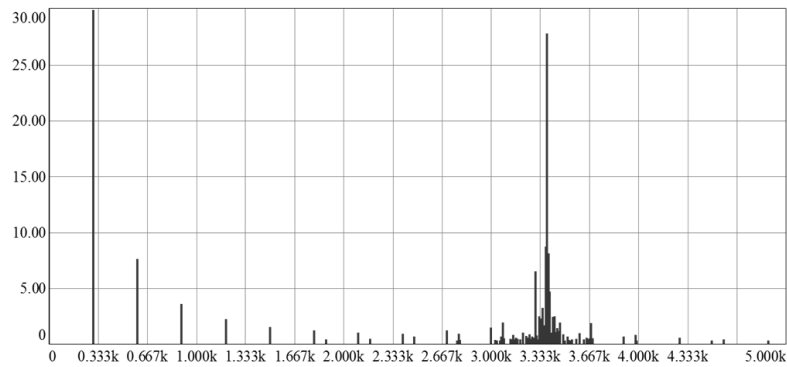


Figure 5.41 Harmonic spectrum of dc bus voltage of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (5 V/div, 333 Hz/div).

Figure 5.42 illustrates the steady state motor torque. As expected the dc bus disturbance rejection eliminated the 300 Hz ripple.

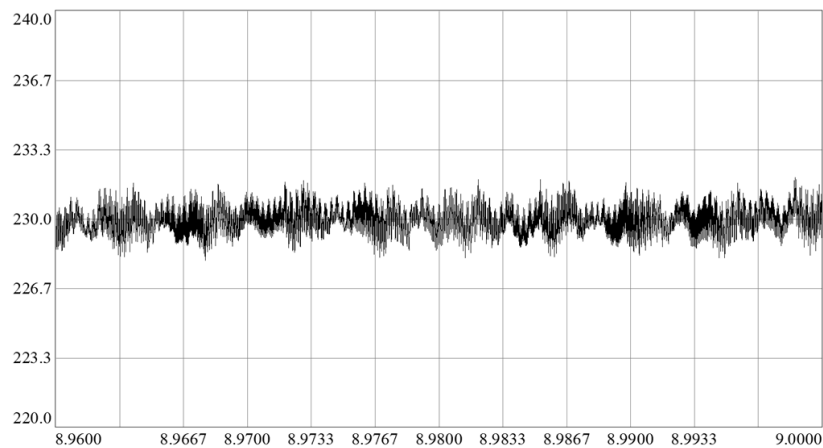


Figure 5.42 Motor steady state torque of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (3.3 N.m/div, 3.3 ms/div).

Figure 5.43 shows the line current waveform and Figure 5.44 shows the corresponding harmonic spectrum for the drive. The dc bus disturbance rejection creates high distortion on the line current as can be seen clearly in the spectrum. The resonant component at 3.4 kHz is amplified significantly.

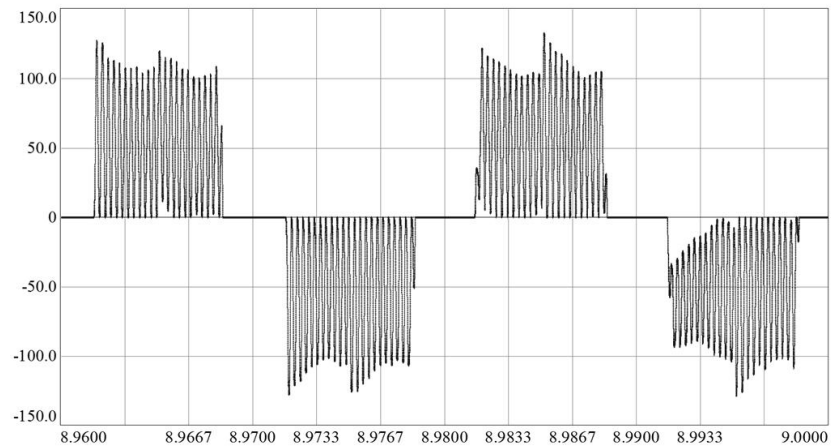


Figure 5.43 The line current waveform of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (50 A/div, 3.3 ms/div).

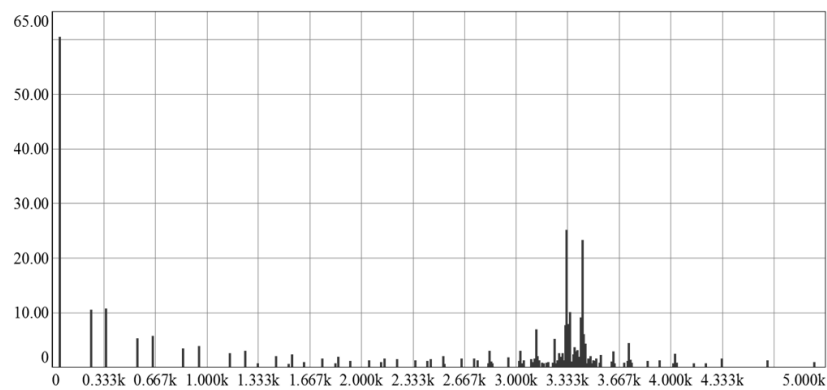


Figure 5.44 Harmonic spectrum of line current of 37 kW low C_{dc} motor drive operating under constant torque load without dc link inductor with dc bus disturbance rejection (10 A/div, 333 Hz/div).

5.4.2 Fan Load Operation Simulation Results

The drives are simulated with and without dc bus disturbance rejection and effect of variable torque on the performance is investigated using the fan windage coefficients given in Chapter 4. The 2.2 kW motor operates at 1400 rpm yielding 11.3 N.m (1.6 kW/~75% load) and the 37 kW operates at 1100 rpm resulting in 177 N.m (20.4 kW/~55% load).

5.4.2.1 2.2 kW Motor Drive Fan Load Operation without DC Bus Disturbance Rejection

Figure 5.45 shows the speed, d-q axis currents, and motor torque during acceleration of the motor. The motor set speed is 1400 rpm.

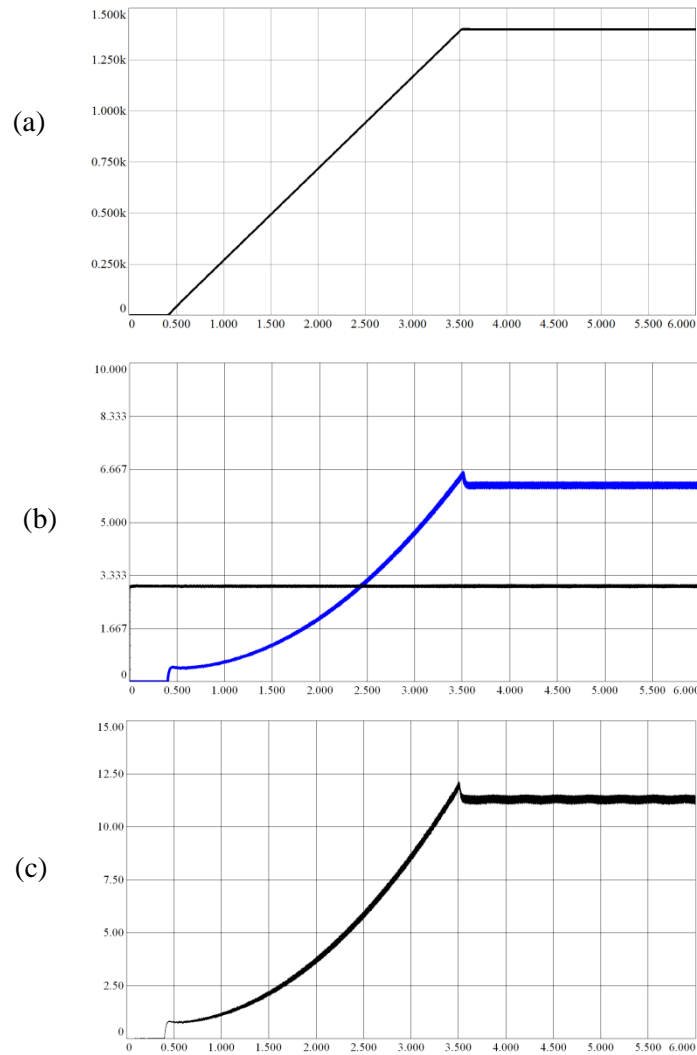


Figure 5.45 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (a) speed (250 rpm/div, 0.5 s/div), (b) d axis current (black) and q axis current (blue) (1.67 A/div, 0.5 s/div), (c) internal torque (2.5 N.m/div, 0.5 s/div).

Figure 5.46 and Figure 5.47 shows the dc bus voltage and corresponding harmonic spectrum respectively. The dc bus voltage is stable and contains dominant 300 Hz ripple in addition to low amplitude resonant component at 2.5 kHz. The fan load has very similar effect on the dc bus like the constant torque operation.

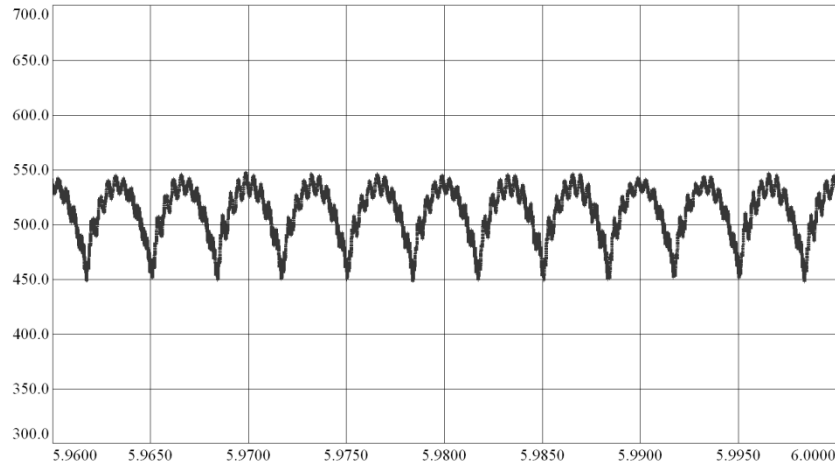


Figure 5.46 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (50 V/div, 5 ms/div).

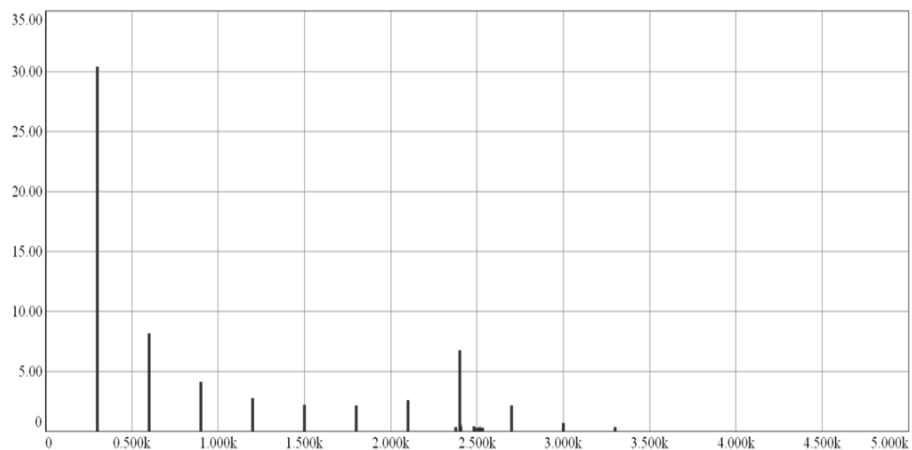


Figure 5.47 Harmonic spectrum of dc bus voltage of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (5 V/div, 500 Hz/div).

The motor torque as seen in Figure 5.48 includes the 300 Hz ripple due to bus voltage ripple as in the case of constant torque load operation.

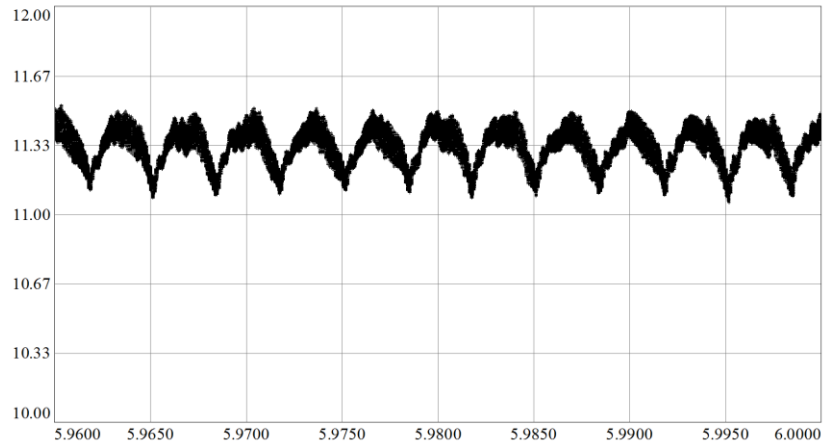


Figure 5.48 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (0.33 N.m/div, 5 ms/div).

Figure 5.49 shows the line current waveform close to ideal rectangular shape and Figure 5.50 shows the harmonic spectrum containing resonance components.

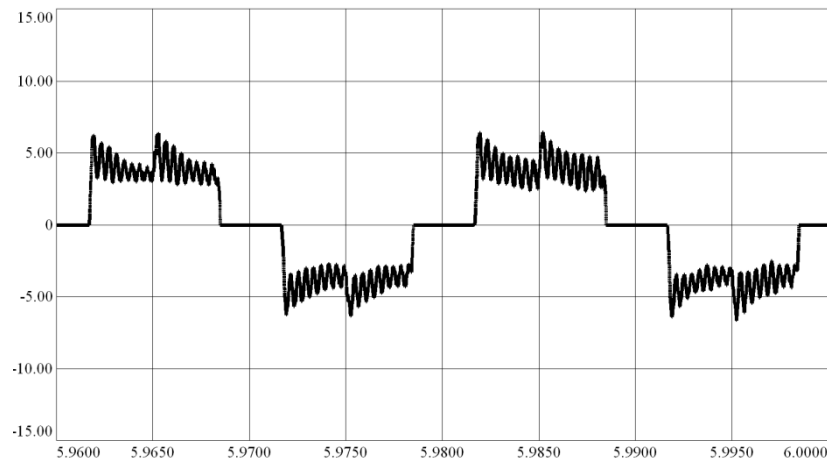


Figure 5.49 The line current waveform of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (5 A/div, 5 ms/div).

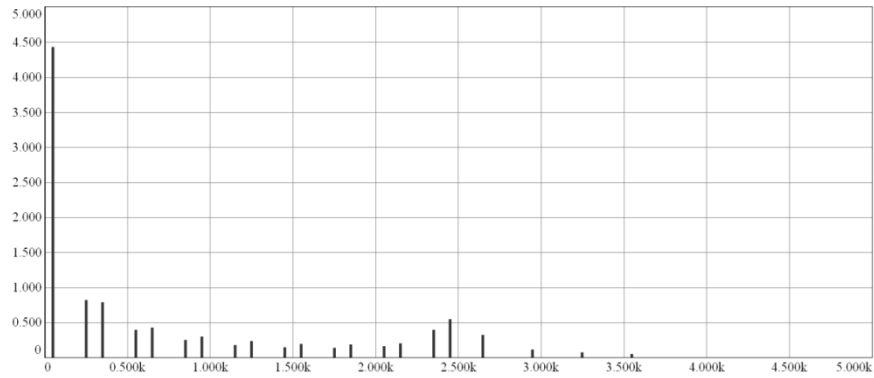


Figure 5.50 Harmonic spectrum of line current of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (0.5 A/div, 500 Hz/div).

5.4.2.2 2.2 kW Motor Drive Fan Load Operation with DC Bus Disturbance Rejection

Since the start up and acceleration have the same characteristics only the steady state waveforms are given. Figure 5.51 and Figure 5.52 shows the dc bus voltage and its harmonic spectrum. The dc bus faces high amplitude resonance oscillations around 2.5 kHz due to increased negative impedance effect.

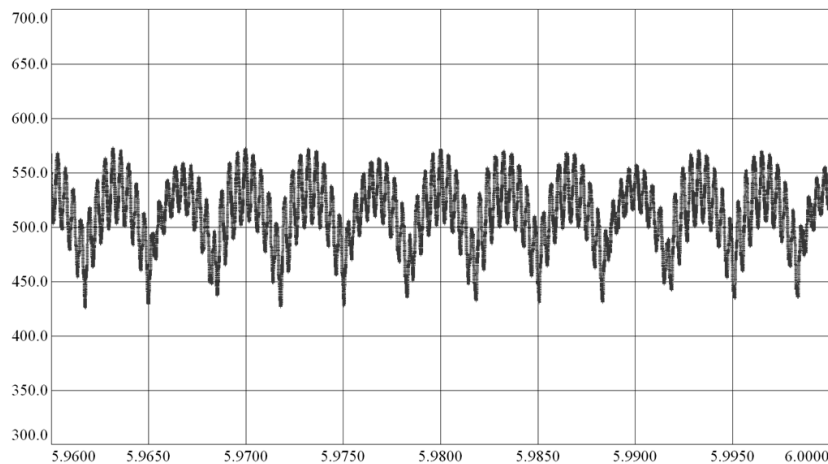


Figure 5.51 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (50 V/div, 5 ms/div).

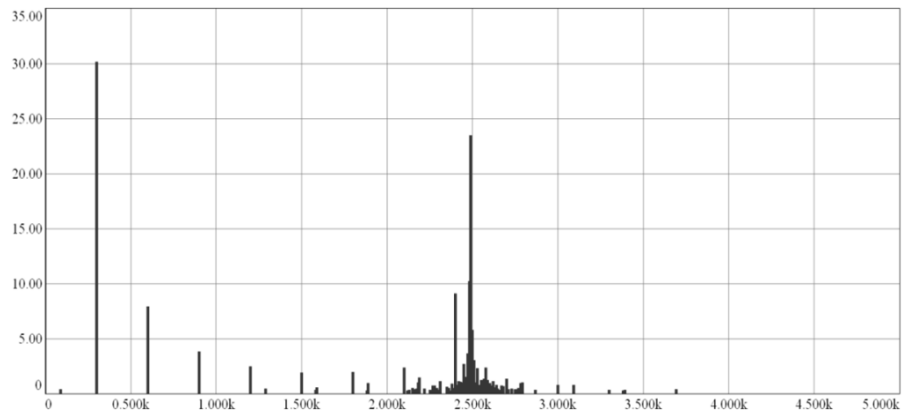


Figure 5.52 Harmonic spectrum of dc bus voltage of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (5 V/div, 500 Hz/div).

Figure 5.53 shows the steady state motor torque. The dc bus disturbance rejection eliminated the 300 Hz ripple as expected.

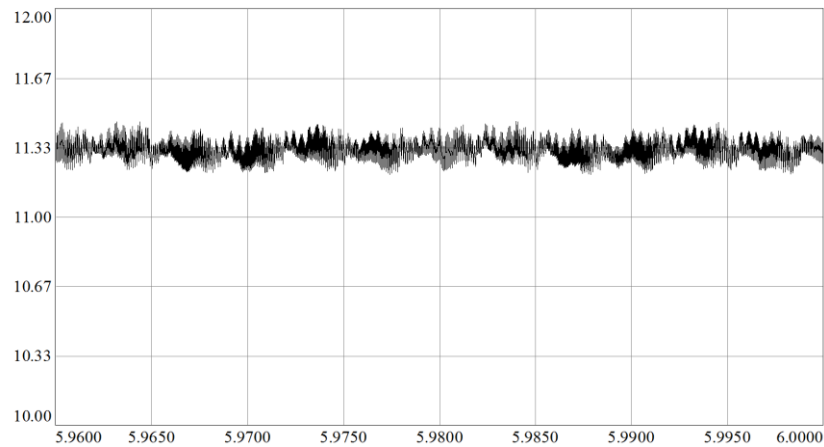


Figure 5.53 Motor steady state torque of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (0.33 N.m/div, 5 ms/div).

Figure 5.54 and Figure 5.55 illustrates the line current and corresponding harmonic spectrum. The disturbance rejection increased the line current distortion considerably by amplifying the resonant component at 2.5 kHz.

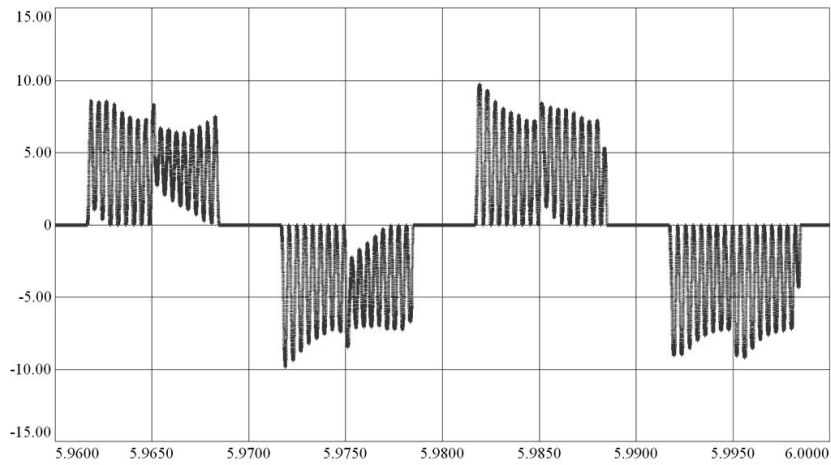


Figure 5.54 The line current waveform of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (5 A/div, 5 ms/div).

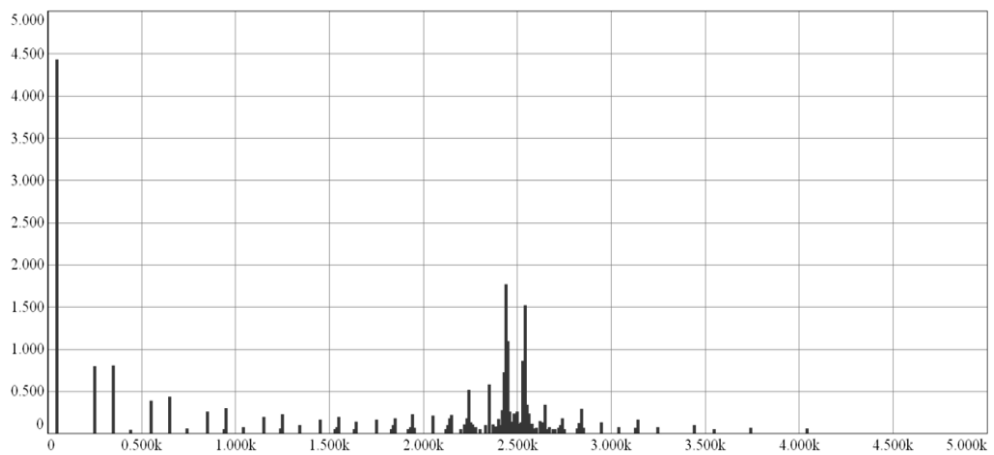


Figure 5.55 Harmonic spectrum of line current of 2.2 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (0.5 A/div, 500 Hz/div).

5.4.2.3 37 kW Motor Drive Fan Load Operation without DC Bus Disturbance Rejection

Figure 5.56 shows the speed, d-q axis currents, and motor torque during acceleration of 37 kW motor with fan load to 1100 rpm.

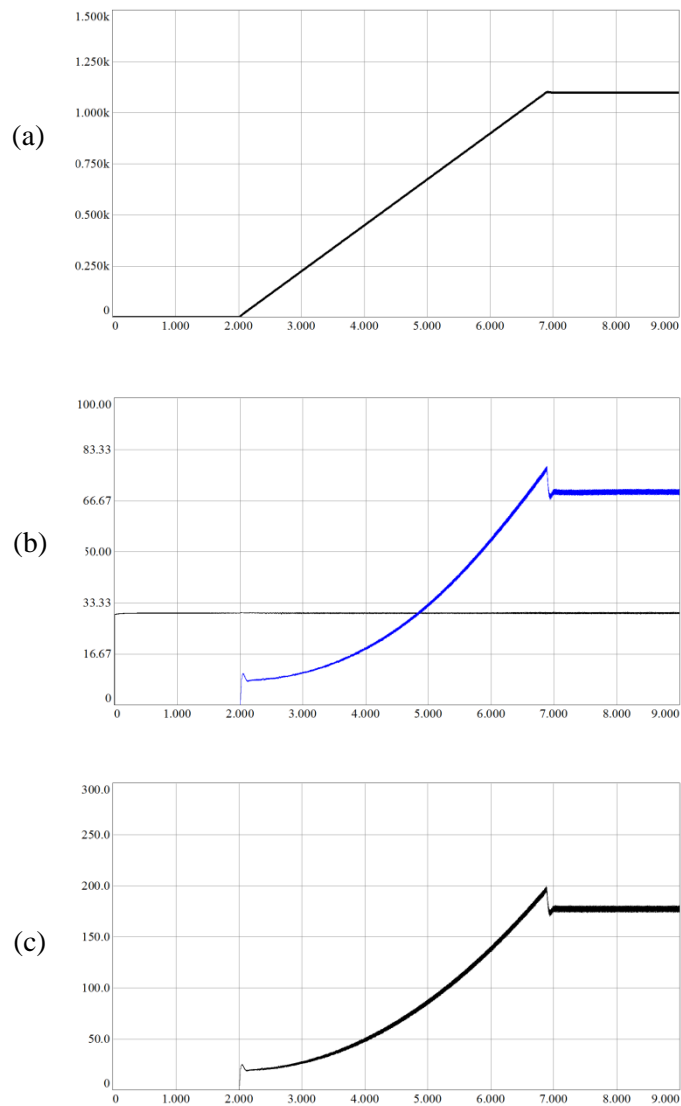


Figure 5.56 37 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (a) speed (250 rpm/div, 1 s/div), (b) d axis current (black) and q axis current (blue) (16.67 A/div, 1 s/div), (c) motor torque (50 N.m/div, 1 s/div).

As seen in Figure 5.57, the bus voltage contains the dominant 300 Hz ripple and there is no stability problem. Figure 5.58 shows the harmonic spectrum of the bus voltage.

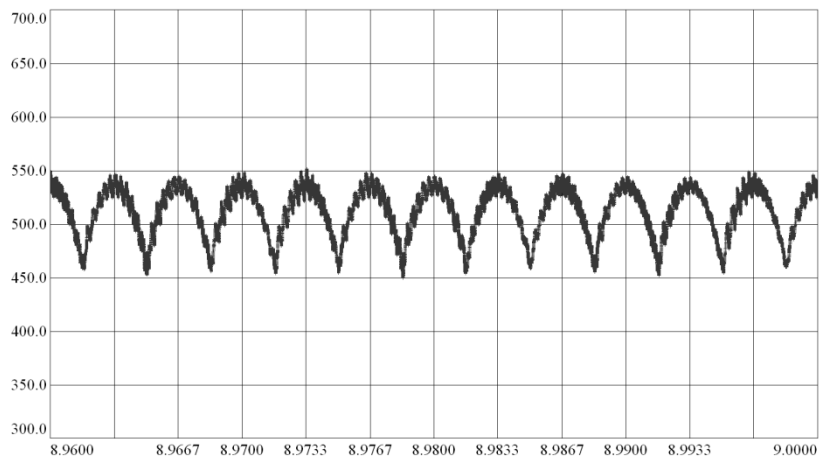


Figure 5.57 DC bus voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (50 V/div, 3.3 ms/div).

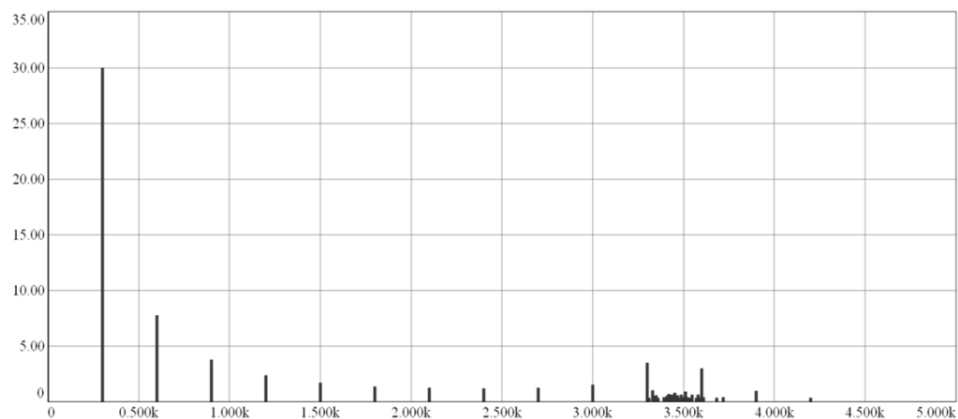


Figure 5.58 Harmonic spectrum of dc bus voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (5 V/div, 500 Hz/div).

The motor steady state torque, as seen in Figure 5.59, contains 5 N.m pp ripple at 300 Hz. This is similar to that of constant torque load case, indicating the effect of dc bus voltage ripple on the steady state motor torque.

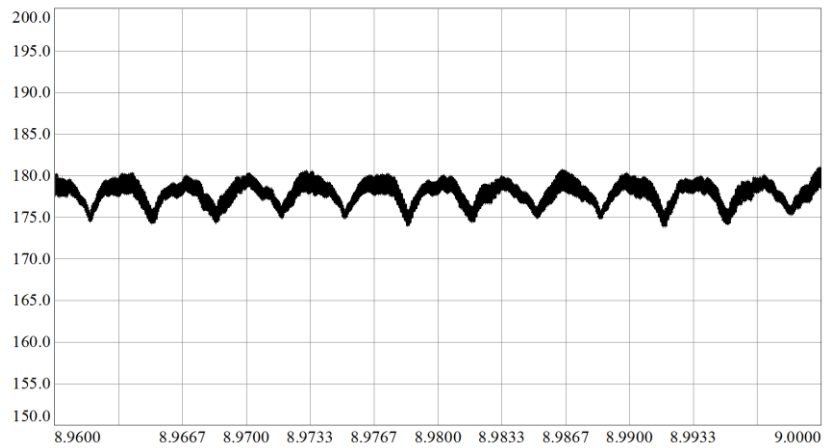


Figure 5.59 Motor steady state torque of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (5 N.m/div, 3.3 ms/div).

Figure 5.60 illustrates the line current waveform. It is close to ideal rectangular wave shape current waveform obtained from ideal diode rectifier. Figure 5.61 shows the harmonic spectrum for the line current. It includes the resonant frequency components in addition to the low order $6k \pm 1$ harmonics.

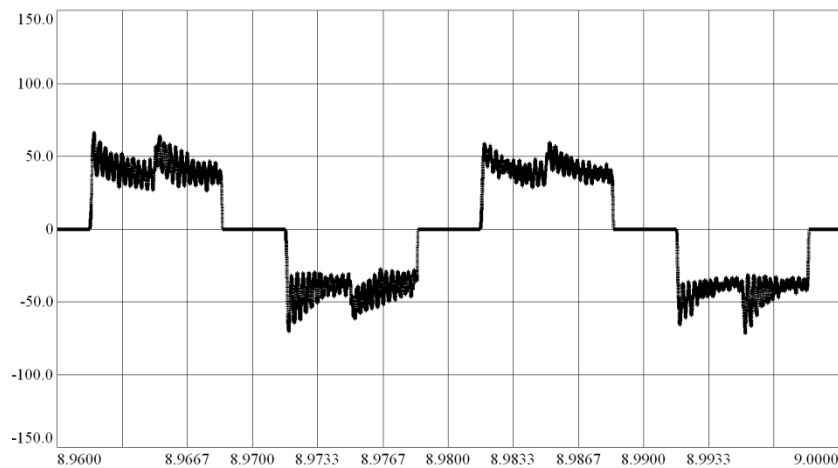


Figure 5.60 The line current waveform of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (50 A/div, 3.3 ms/div).

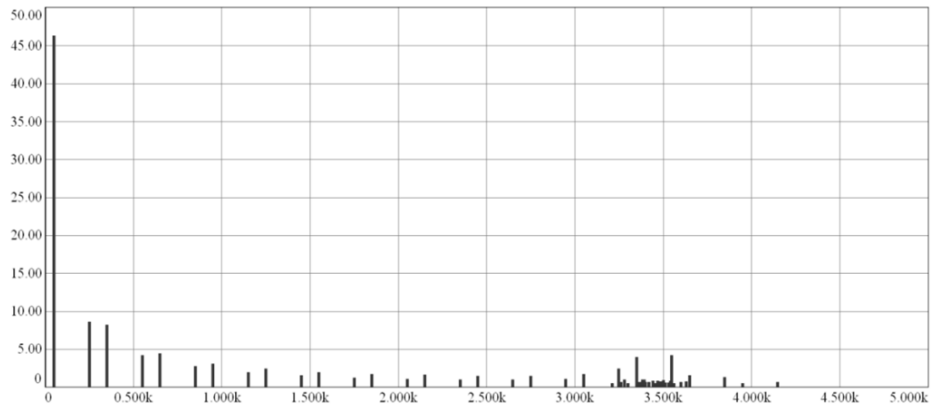


Figure 5.61 Harmonic spectrum of line current of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor without dc bus disturbance rejection (5 A/div, 500 Hz/div).

5.4.2.4 37 kW Motor Drive Fan Load Operation with DC Bus Disturbance Rejection

Figure 5.62 shows the dc bus voltage and Figure 5.63 shows the corresponding harmonic spectrum for the 37 kW motor drive with fan load with disturbance rejection applied. The resonant voltage amplification is considerably increased due to negative impedance effect of dc bus disturbance rejection.

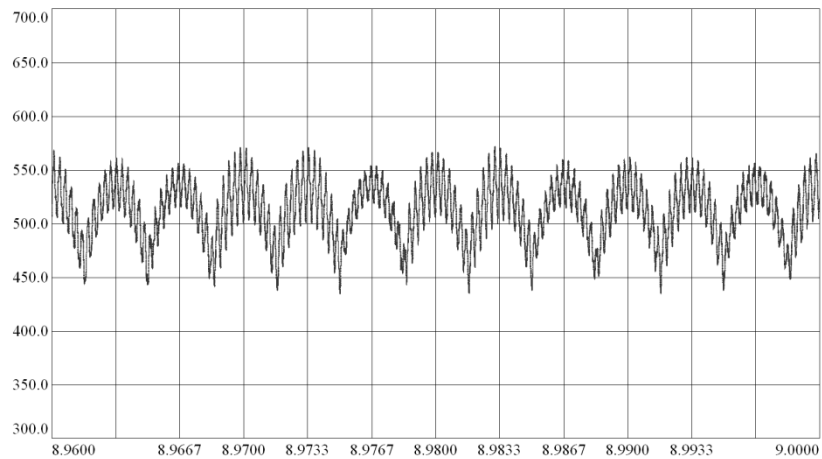


Figure 5.62 DC bus voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (50 V/div, 3.3 ms/div).

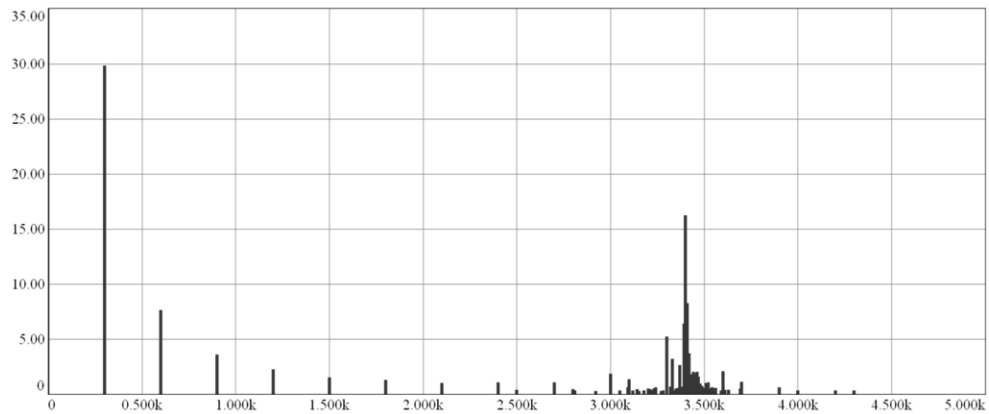


Figure 5.63 Harmonic spectrum of dc bus voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (5 V/div, 500 Hz/div).

The disturbance rejection eliminated the 300 Hz torque ripple as seen in Figure 5.64.

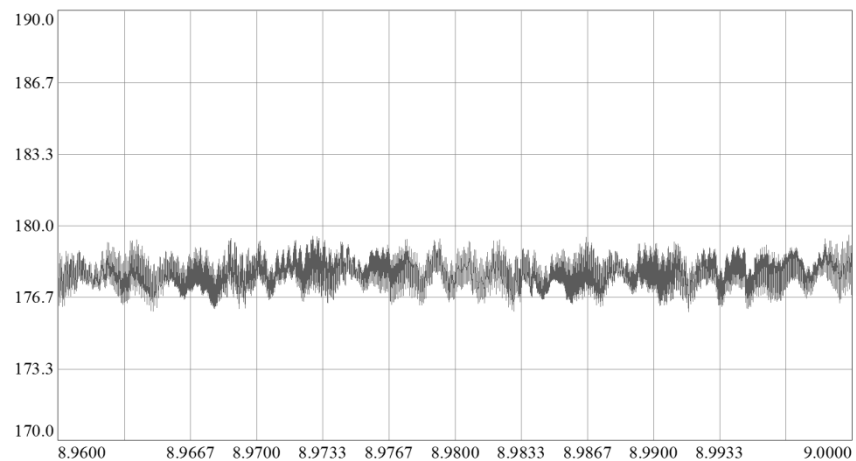


Figure 5.64 Motor steady state torque at set speed voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (3.3 N.m/div, 3.3 ms/div).

As expected, dc bus disturbance rejection increased the bus voltage oscillations and the line current distortion. Figure 5.65 and Figure 5.66 shows the line current and corresponding harmonic spectrum respectively. The line current has high amplitude resonant component around 3.4 kHz.

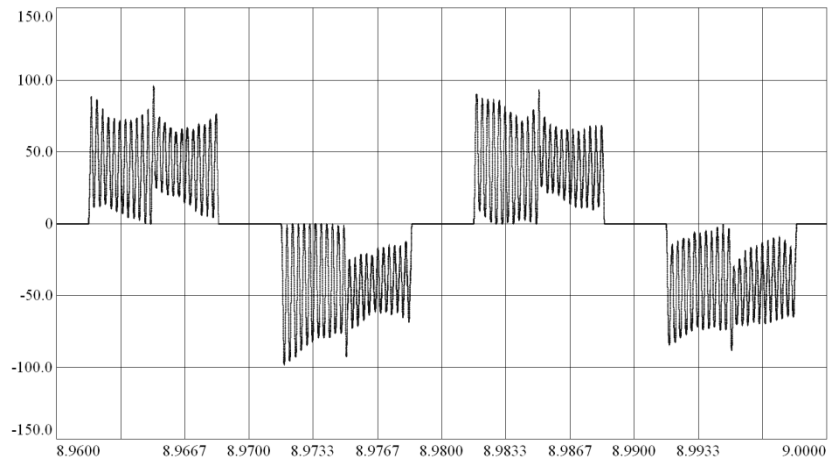


Figure 5.65 The line current waveform voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (50 A/div, 3.3 ms/div).

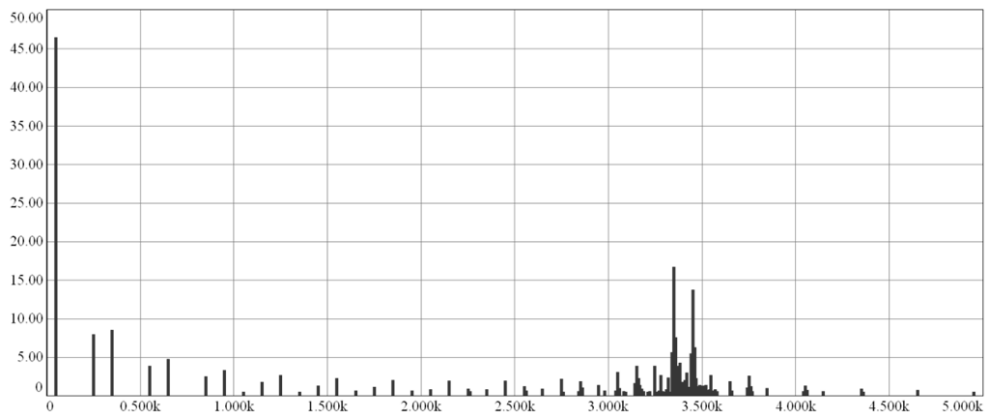


Figure 5.66 Harmonic spectrum of line current voltage of 37 kW low C_{dc} motor drive operating under fan load without dc link inductor with dc bus disturbance rejection (5 A/div, 500 Hz/div).

5.5 Design of Low C_{dc} Motor Drive with DC Link Inductor

In this section, the drives are equipped with dc link inductor filters to investigate the stability and performance. Considering the stability criterion by (5.10), the effect of

increasing the L/C ratio on the rectifier stability is investigated via the simulation results. The circuit parameters for the drive with dc link inductor are given in Table 5.3.

Table 5.3 Circuit parameters of the low C_{dc} motor drives with dc link inductor.

Parameter	2.2 kW motor drive	37 kW motor drive
Line inductance, L_g (mH)	0.25	0.0148
Line resistance, R_g (m Ω)	125.0	0.0074
AC line reactor, L_{ac} (mH)	-	-
DC link inductor, L_{dc} (mH)	2	0.112
DC bus capacitor, C_{dc} (μ F)	8	72
DC Link resonant frequency, ω_n (rad/s)	$2\pi.1125$	$2\pi.1576$
Inverter switching frequency, f_c (kHz)	10	10
PWM type	SVPWM	SVPWM

Instability is expected on dc bus since the L/C ratio is well above the stability criterion defined by (5.10). This is investigated the root locus plotted using [32] (Figure 5.67) for the characteristic equation (5.9). The instability increases with the increased load power, since the poles which are already in the right hand side (RHS) of the s-plane further moves to right side with increased load power.

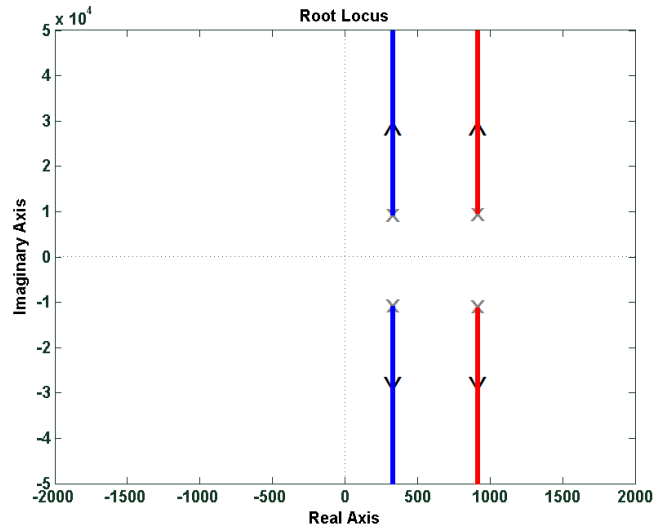


Figure 5.67 Root locus of the characteristic equation (5.9) of the equivalent rectifier-inverter circuit (blue 15 kW, red 37 kW load power).

5.6 Simulation Results of the Drives with DC Link Inductor

The drives are investigated in terms of performance and stability during steady state operation and the dc bus voltage, motor torque, and line current waveforms at steady state operation point are investigated.

5.6.2 Constant Torque Load Operation Simulation Results

As done previously, the performance of the drives is investigated with and without dc bus disturbance rejection. In this case, the system is more prone to instability due to DC link inductor and the negative impedance effect of disturbance rejection gains more importance.

5.6.2.1 2.2 kW Motor Drive Constant Torque Load Operation without DC Bus Disturbance Rejection

Figure 5.68 shows the dc bus voltage waveform of the 2.2 kW constant torque load drive with dc link inductor and without dc bus disturbance rejection.

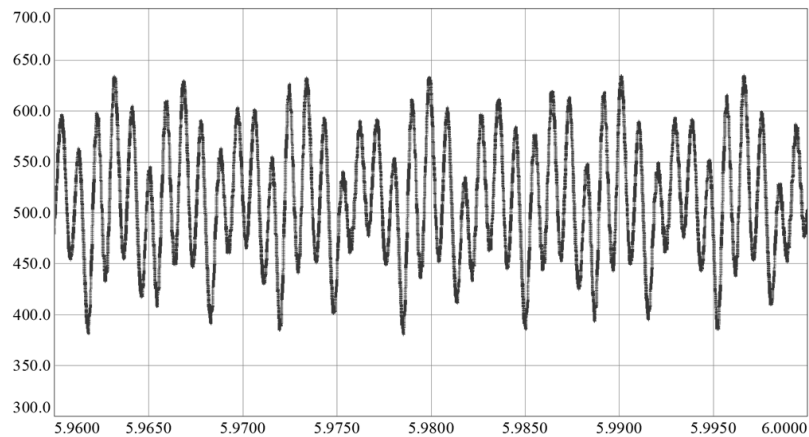


Figure 5.68 DC bus voltage of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc bus disturbance rejection and with dc link inductor (50 V/div, 5 ms/div).

The bus voltage has high amplitude resonant oscillations even without dc bus disturbance rejection method. This is a strong indication of instability seen also in Figure 5.69 where

the voltage demand from SFCR and unstable bus voltage circles are seen. The two circles interfere through the operation of the drive an indication of instability.

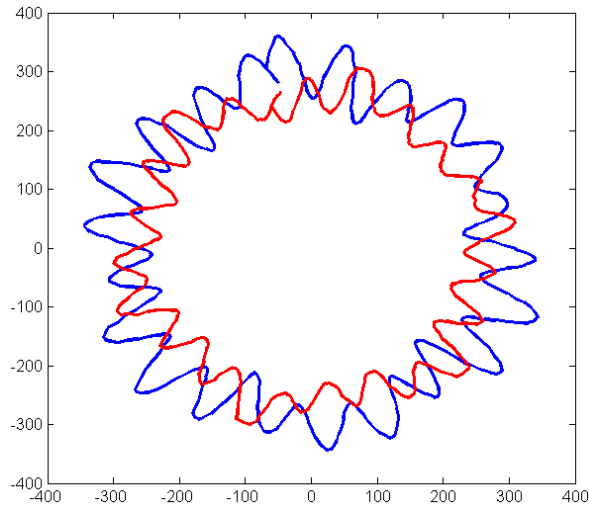


Figure 5.69 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive with dc link inductor without dc bus disturbance rejection (100 V/div, 100 V/div).

Figure 5.70 shows the motor torque which has ripple reflecting the resonant oscillations on the dc bus voltage.

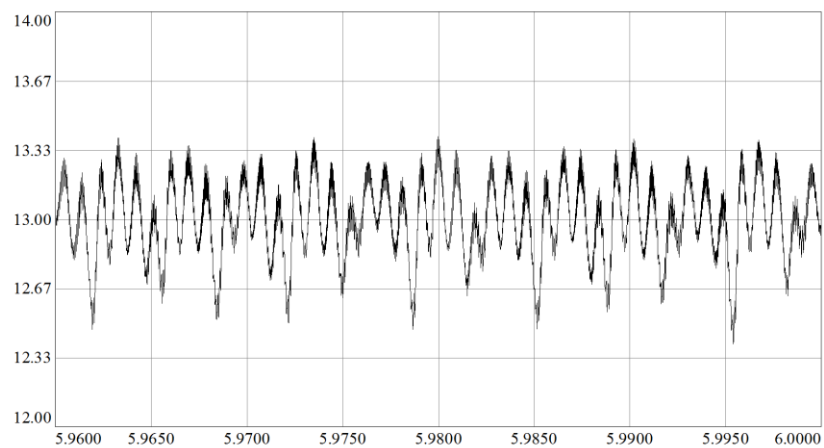


Figure 5.70 Steady state torque of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc bus disturbance rejection and with dc link inductor (0.33 N.m/div, 5 ms/div).

The line current has high distortion even without dc bus disturbance rejection due to instability caused by high L/C ratio.

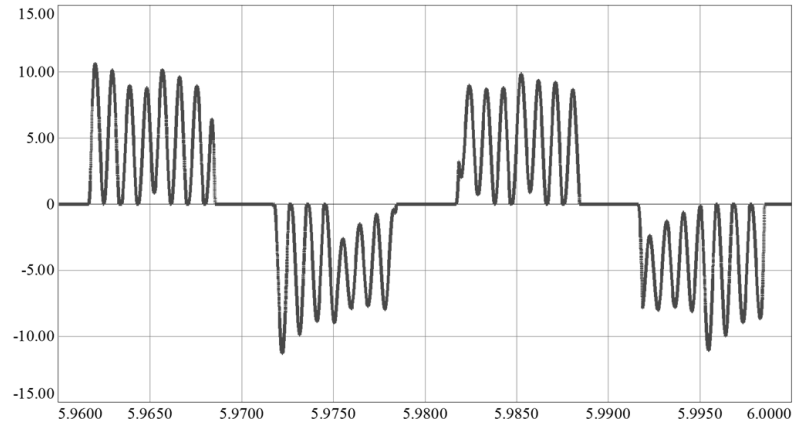


Figure 5.71 Line current waveform of 2.2 kW low C_{dc} motor drive operating under constant torque load without dc bus disturbance rejection and with dc link inductor (5 A/div, 5 ms/div).

5.6.2.2 37 kW Motor Drive Constant Torque Load Operation without DC Bus Disturbance Rejection

The 37 kW motor drive also faces unstable operation as seen in the unstable dc bus voltage waveform in Figure 5.72.

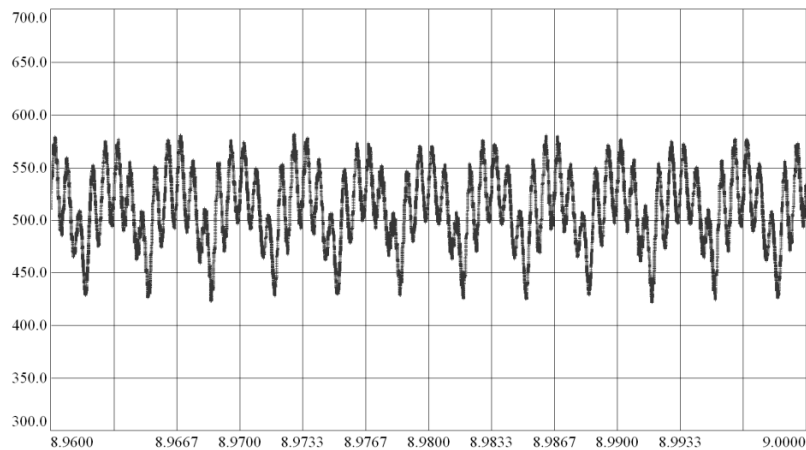


Figure 5.72 DC bus voltage of 37 kW low C_{dc} motor drive operating under constant torque load without dc bus disturbance rejection and with dc link inductor (50 V/div, 3.3 ms/div).

Figure 5.73 shows the voltage circles for the 37 kW drive with dc link inductor. As expected both the voltage demand and dc bus voltage show oscillations. The level of instability on 37 kW drive can be said to be lower than the 2.2 kW drive.

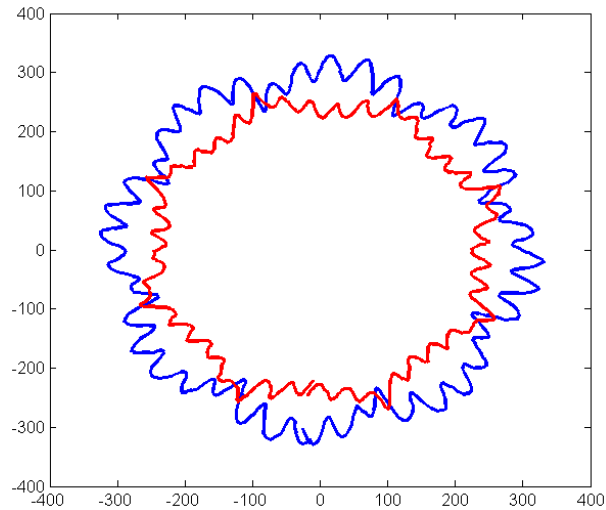


Figure 5.73 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 37 kW low C_{dc} motor drive operating under constant torque load with dc link inductor without dc bus disturbance rejection (100 V/div, 100 V/div).

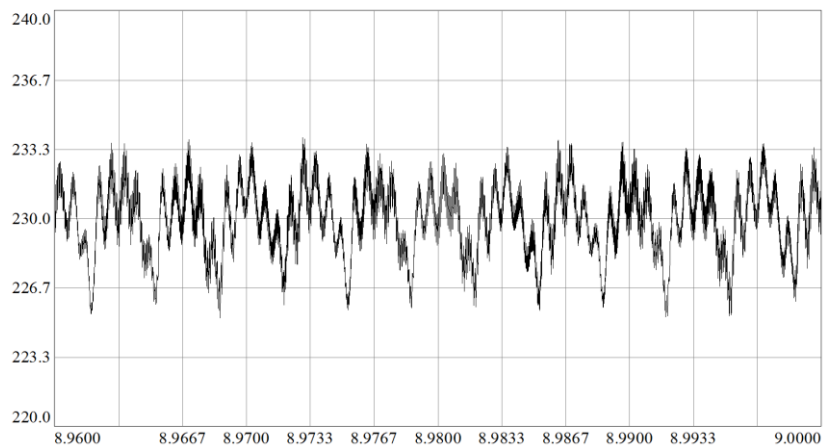


Figure 5.74 Steady state torque of 37 kW low C_{dc} motor drive operating under constant torque load without dc bus disturbance rejection and with dc link inductor (3.33 N.m/div, 3.3 ms/div).

Figure 5.74 and Figure 5.75 show the steady state motor torque and line current respectively. The motor torque reflects the dc bus voltage oscillations as no disturbance rejection is applied. The line current also suffers from the instability on dc link and has high distortion.

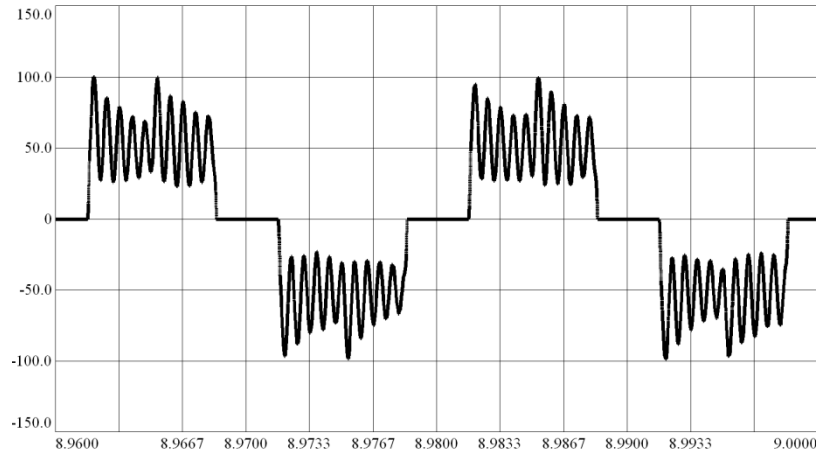


Figure 5.75 Line current waveform of 37 kW low C_{dc} motor drive operating under constant torque load without dc bus disturbance rejection and with dc link inductor (50 A/div, 3.3 ms/div).

The simulations for fan load also yielded same unstable operations with dc link inductor. This fact shows that, using a dc link inductor very large compared to the line inductance causes instability on the dc link, as expected from (5.11). This makes it necessary to apply active damping or stabilization control on dc bus voltage.

5.7 Active DC Link Stabilization Methods

The simulations with dc link inductor showed that the dc bus may face instability in case of using a large inductor with respect the line inductance. Hence, the circuit needs stability improvement by active control methods.

The bus voltage oscillations directly show its effects on line current quality. If the oscillations are poorly damped, the line current suffers from harmonic distortion. The dc bus voltage oscillations also affect the inverter operation and motor drive performance. Since the dc bus voltage is not stiff, any high voltage demand coming from the inverter

may not be provided by the link voltage and this in turn affects the inverter operation and motor drive performance. Depending on the load type, this condition may get even worse.

As the diode rectifier is uncontrollable and does not allow any signal injection, active stabilization techniques are applied as modifications or injections to the motor control commands. This can be accomplished by updating the voltage or current references of the motor current regulator. Thus, the applicable dc bus voltage control algorithms for low capacitance rectifiers can be analyzed in two broad categories such as voltage mode and current mode stabilizations. All methods aim to increase the damping coefficient of the dc link to suppress oscillations and create a stable bus voltage. The effect of active stabilization can be illustrated as an addition of a virtual damping resistor connected in series to the resistor existing in the equivalent rectifier circuit. Figure 5.76 shows the equivalent circuit of three phase diode rectifier with active damping applied with a series connected damping resistor R_{damp} .

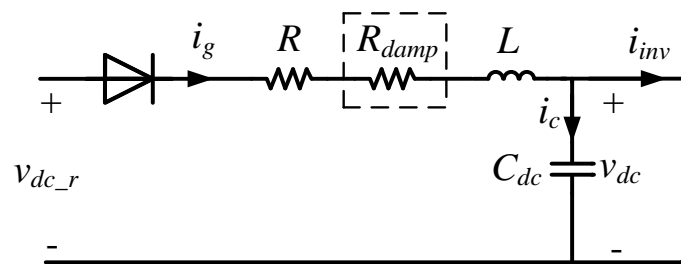


Figure 5.76 Equivalent rectifier circuit of actively stabilized system including virtual damping resistor.

5.7.1 Voltage Mode Stabilization Methods

Voltage mode stabilization techniques update the voltage command of the current regulator of the machine using the voltage feedback from the dc bus capacitor.

5.7.1.1 Method 1 [35]

As the primary reason for the decreased stability is lowering the dc bus capacitance and hence increasing the resonant frequency, the unstable system can be brought to stable

operation condition by using resonant component of dc link voltage for stabilization algorithm. The method offered by [35] uses dc bus disturbance rejection using a modified dc bus voltage value in the formula. It aims to increase stability by 180° phase shifting the resonant component of the dc bus voltage and adding it to the 300 Hz 6-pulse dc link voltage and using the resultant dc bus voltage value in dc bus disturbance rejection. As seen in the previous section, the closed loop current controller generates the voltage reference in order to reject the dc bus voltage ripple, which further increases instability because the modulation index is increased when the dc bus voltage decreases, which further causes a decrease and vice versa. By using the 180° shifted resonant waveform, the instants where the actual resonant voltage component decreases in magnitude is seen as a voltage rise by the dc bus disturbance rejection controller and modulation index M_i is decreased and when the actual resonant voltage component decreases M_i is increased, as seen visibly in Figure 5.77. Hence, the amplification of resonance component is disabled and the negative impedance effect on the dc bus is eliminated, which results in increased stability.

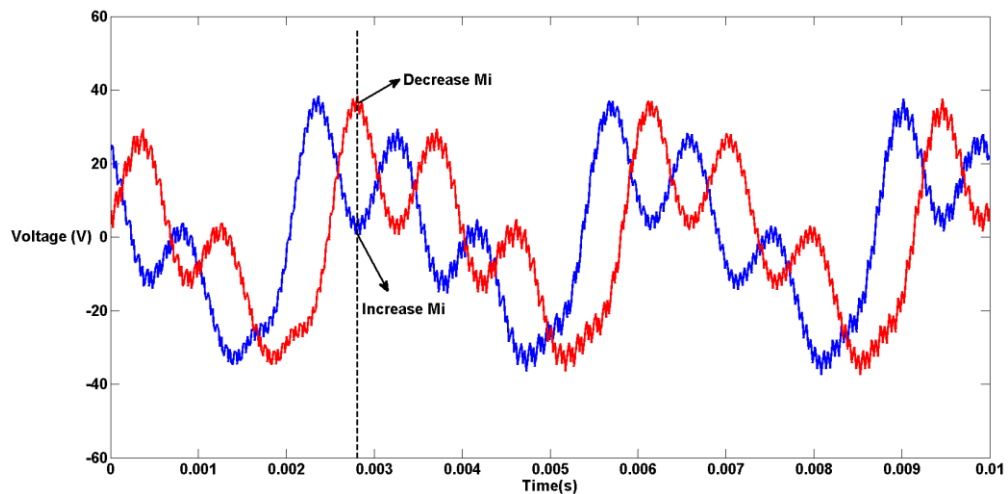


Figure 5.77 Resonant component of dc bus voltage (blue) and 180° shifted version (red).

In the simulations, the high frequency resonant voltage component is obtained by first passing the dc bus voltage through a low pass filter with cutoff frequency of $f_0=300$ Hz and subtracting the filtered component from the dc bus voltage. Then the resonant component is phase shifted by 180° and added to the low pass filtered bus voltage to be used in the dc

bus disturbance rejection method. Figure 5.78 shows the schematic for the implementation of Method 1.

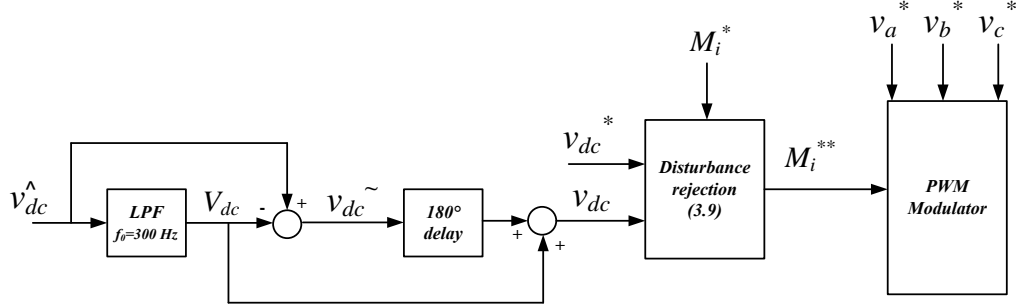


Figure 5.78 Schematic of implementation of active stabilization Method 1.

5.7.1.2 Method 2 [36]

Method given in [36] is another voltage mode control in which the q and d axis voltage variables are updated according to the variations on dc bus voltage. The damping ratio is defined by (5.12) for the same model given in Figure 5.1.

$$\zeta = \frac{1}{2\omega_n} \left(\frac{R}{L} - \frac{2(V_{ds}I_{ds} + V_{qs}I_{qs})}{3C_{dc}V_{dc}^2} \right) \quad (5.12)$$

In (5.11) if the L/R ration is large, then the damping ratio of the system is lowered. The right hand side of the equation $-\frac{2(V_{ds}I_{ds} + V_{qs}I_{qs})}{3C_{dc}V_{dc}^2}$ acts as a negative damping coefficient for the system which degrades the stability. So the voltage updates to be applied on d and q axis of the motor controller is expected to add a term to the relation in (5.11) to turn the negative impedance effect of the right hand side expression $-\frac{2(V_{ds}I_{ds} + V_{qs}I_{qs})}{3C_{dc}V_{dc}^2}$ to a positive impedance effect. For this reason, a term proportional to the dc bus voltage variation \tilde{v}_{dc} given by (5.13) and (5.14) is added to d and q axis voltage references.

$$\tilde{v}_{ds} = K1 \cdot \tilde{v}_{dc} \quad (5.13)$$

$$\tilde{v}_{qs} = K2 \cdot \tilde{v}_{dc} \quad (5.14)$$

The set of K1 and K2 to increase stability are found as;

$$\left(\frac{V_{ds}}{V_{dc}}, \frac{V_{qs}}{V_{dc}}\right), \left(\frac{V_{ds}I_{ds}+V_{qs}I_{qs}}{I_{ds}V_{dc}}, 0\right) \left(0, \frac{V_{ds}I_{ds}+V_{qs}I_{qs}}{I_{qs}V_{dc}}\right) [36].$$

Any combination of K1 and K2 can be used for the active controller design. In the simulations, K2 is selected 0 as done in [36]. The schematic in Figure 5.79 shows the implementation of the method.

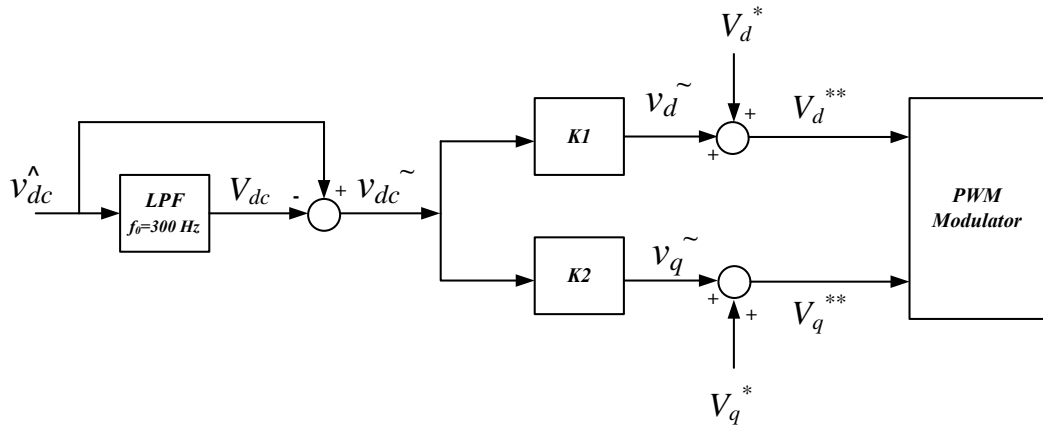


Figure 5.79 Schematic of implementation of active stabilization Method 2.

5.7.2 Current Mode Stabilization Methods

Current mode methods modify the current reference commands of the motor current regulator to provide active stabilization. The controller algorithm uses the resonant voltage component as feedback to generate the necessary signal to be injected to the motor current references.

5.7.2.1 Method 3 [33]

The method given by [33] is based on the modification of q axis current reference of the SFCR of the motor drive to obtain active damping. This is obtained by injection of a compensation term proportional to the variation \tilde{v}_{dc} of the dc voltage from its mean value V_{dc0} to the original q axis current reference i_{q0}^{ref} as given by (5.15).

$$i_q^{\text{ref}} = i_{q0}^{\text{ref}} + g\tilde{v}_{dc} \quad (5.15)$$

To obtain the expression of g term, the equations (5.3) and (5.4) are reused and modified for the system compensated by (5.14). The modified equations including the compensation terms are given by (5.16) to (5.19).

$$L \frac{di_g}{dt} = v_{dc,r} - Ri_g - v_{dc} = v_{dc,r} - Ri_g - (\tilde{v}_{dc} + V_{dc0}) \quad (5.16)$$

The current drawn by the inverter i_{inv} can be written as the load power drawn by the motor, P_L , divided by the average dc link voltage, V_{dc0} .

$$P_L = \frac{3}{2}(v_d i_d + v_q i_q) \approx \frac{3}{2}(v_q i_q) \quad (5.17)$$

In (5.17) $v_d i_d$ term is neglected since $|v_d| \ll |v_q|$. So the inverter current becomes;

$$i_{\text{inv}} = \frac{\frac{3}{2}v_q i_q}{V_{dc0}} \quad (5.18)$$

Rewriting the capacitor current in terms of dc link and inverter current and writing i_q as the sum of mean value i_{q0}^{ref} and compensation term \tilde{i}_q , (5.19) is obtained.

$$i_c = C \frac{d\tilde{v}_{dc}}{dt} = i_g - \left[\frac{kv_q(i_{q0}^{\text{ref}} + \tilde{i}_q)}{V_{dc0}} \left(1 - \frac{\tilde{v}_{dc}}{V_{dc0}} \right) \right] \quad (5.19)$$

The dynamics of i_q is given by (5.20) where α_c is the current controller bandwidth.

$$\frac{d\tilde{i}_q}{dt} = \alpha_c (g\tilde{v}_{dc} - \tilde{i}_q) \quad (5.20)$$

Using (5.16) and (5.19), the ratio of rectifier-inverter system output voltage (v_{dc}) to input voltage ($v_{dc,r}$) can be found in terms of the circuit parameters to obtain the characteristic

equation of the *RLC* circuit. Substituting the steady state value of $g\tilde{v}_{dc} = \tilde{i}_q$ into (5.19) and using for the formulation, the characteristic polynomial including the effect of stabilization in (5.21) is obtained [33].

$$s^2 + \left(RC\omega_n^2 + \frac{\frac{3}{2}g_0 v_q}{CV_{dc0}} \right) s + \omega_n^2 \left(1 + \frac{\frac{3}{2}g_0 R v_q}{V_{dc0}} \right) \quad (5.21)$$

In (5.21), $g_0 = g - \frac{i_{q0}^{ref}}{V_{dc0}}$ and by increasing g , the poles of the characteristic equation (5.21) moves towards left and stability is increased. g_0 can be parameterized as in (5.22).

$$g_0 = (\gamma - 1) \frac{RC}{L} \frac{v_{dc0}}{Kv_q} \quad (5.22)$$

The root locus plots using the system characteristic equation (5.21) for various g_0 values for a fixed load power at $V_q = V_{dc}/2$ are shown in Figure 5.80. As expected as the g_0 terms take higher values, the poles move toward left, the dc bus voltage stability increases.

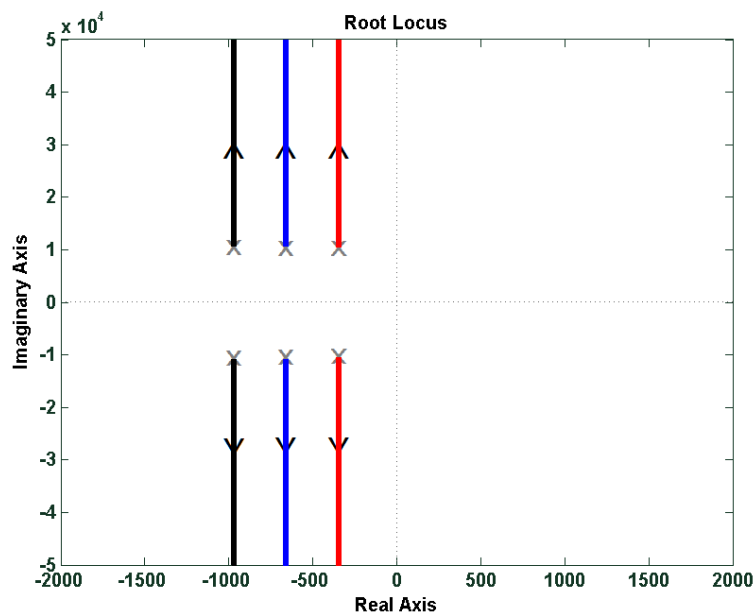


Figure 5.80 Root locus of characteristic equation (5.21) for various g_0 values (black: $g_0=0.2598$, blue: $g_0=0.1694$, red: $g_0=0.0791$).

Using the parametric expression for g_0 in (5.22), the term $\left(RC\omega_n^2 + \frac{\frac{3}{2}g_0V_q}{CV_{dco}} \right)$ in (5.21) becomes $\gamma RC\omega_n^2$. Neglecting the $\frac{\frac{3}{2}g_0RV_q}{V_{dco}}$ term, the modified characteristic equation becomes as in (5.23) where the natural damping term R is replaced by γR . So selecting $\gamma > 1$ increases the damping of the system by addition of a virtual damping resistance expressed in (5.23) [33].

$$s^2 + \gamma RC\omega_n^2 s + \omega_n^2 \quad (5.23)$$

The stability depending on operating load power can also be investigated by root locus using (5.21) for a constant g_0 value and for various V_q values to analyze various load powers. Since the load power is proportional to the applied voltage, the q axis voltage in (5.21) can be varied with keeping g_0 constant and the effect of increasing or decreasing the load power on stability can be investigated. Figure 5.81 shows the root locus for $V_q = V_{dc}/2$ and $V_q = V_{dc}/4$ cases for $g_0 = 0.0791$. The result shows that as the load power is increased, the pole locations for the active stabilized system move further to the left half plane, which indicates the increase in stability. As the operating power is decreased, the poles move to right side direction thus a decrease in stability is expected.

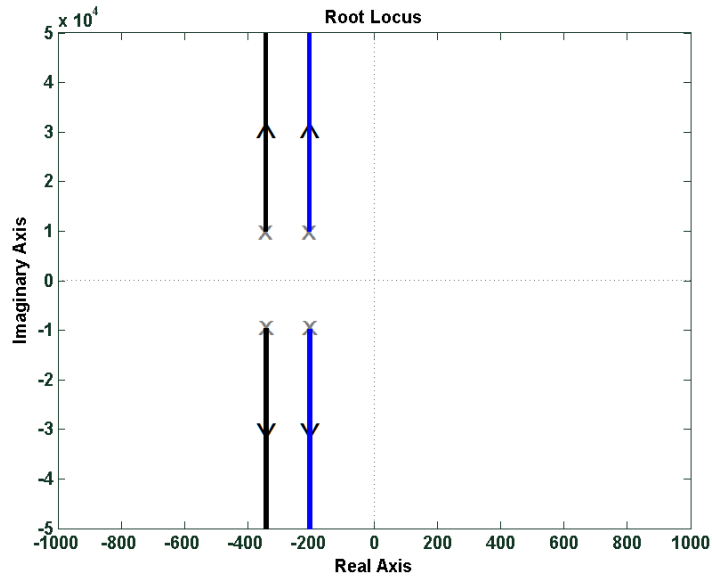


Figure 5.81 Root locus of characteristic equation (5.21) for various operating powers (black: $V_q = V_{dc}/2$, blue: $V_q = V_{dc}/4$).

As expected, this compensation method requires a current controller with a bandwidth sufficient enough to be able to follow the dc link voltage dynamics. [33] addresses this requirement by putting a relation between the current controller bandwidth α_c and the dc link resonant frequency ω_n as in (5.24);

$$\alpha_c > \omega_n \sqrt{\frac{\lambda-1}{\gamma}} \quad (5.24)$$

The inverter switching frequency is also expected to be high enough to design a current controller satisfying (5.24). In the simulations, for the 2.2 kW motor drive circuit, the selected inductance and capacitor values yielded $\lambda=8.1 > 1$ which does not obey the stability rule by (5.11). So, to apply the method, $\gamma=8$ is selected yielding $g_0=0.0084$ and requiring a current regulator bandwidth of approximately $f_{rc}=1$ kHz. To achieve $f_{rc}=1$ kHz, the PWM frequency of $f_c=10$ kHz is sufficient. For the 37 kW motor drive, $\lambda=14.48$ for selected L-C values and (5.11) is not satisfied. So, to apply the method, $\gamma=8$ is selected yielding $g_0=0.0791$ and requiring current regulator bandwidth of approximately $f_{rc}=2$ kHz. To achieve $f_{rc}=2$ kHz, the PWM frequency of $f_c=20$ kHz is sufficient.

Figure 5.82 shows the implementation of Method 3. The low pass filter (LPF) cut off frequency f_0 is selected close to $f_n/4$ as recommended in Method 3 [33]. So, $f_0=278$ Hz for 2.2 kW motor drive and $f_0=417$ Hz for 37 kW motor drive.

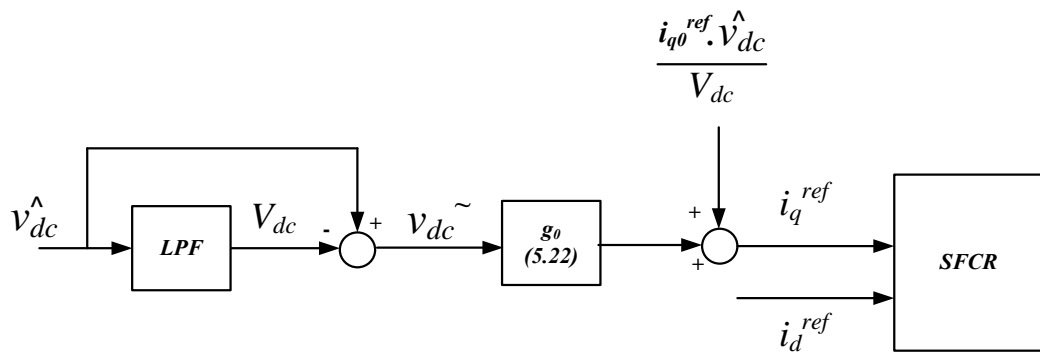


Figure 5.82 Schematic of implementation of active stabilization Method 3.

5.8 Simulation Results with Active Stabilization Methods

The results given in the figures include the uncontrolled and actively stabilized drive waveforms together. The numerical data of the simulation results are provided in Chapter 6.

5.8.1 2.2 kW Motor Drive Constant Torque Load Operation Simulation Results

Figure 5.83 shows the dc bus voltage waveforms for the 2.2 kW constant torque load drive with dc link inductor. The active stabilization methods improve the bus voltage and waveforms are close to ideal six pulse shape. The dc bus disturbance rejection increases the instability further.

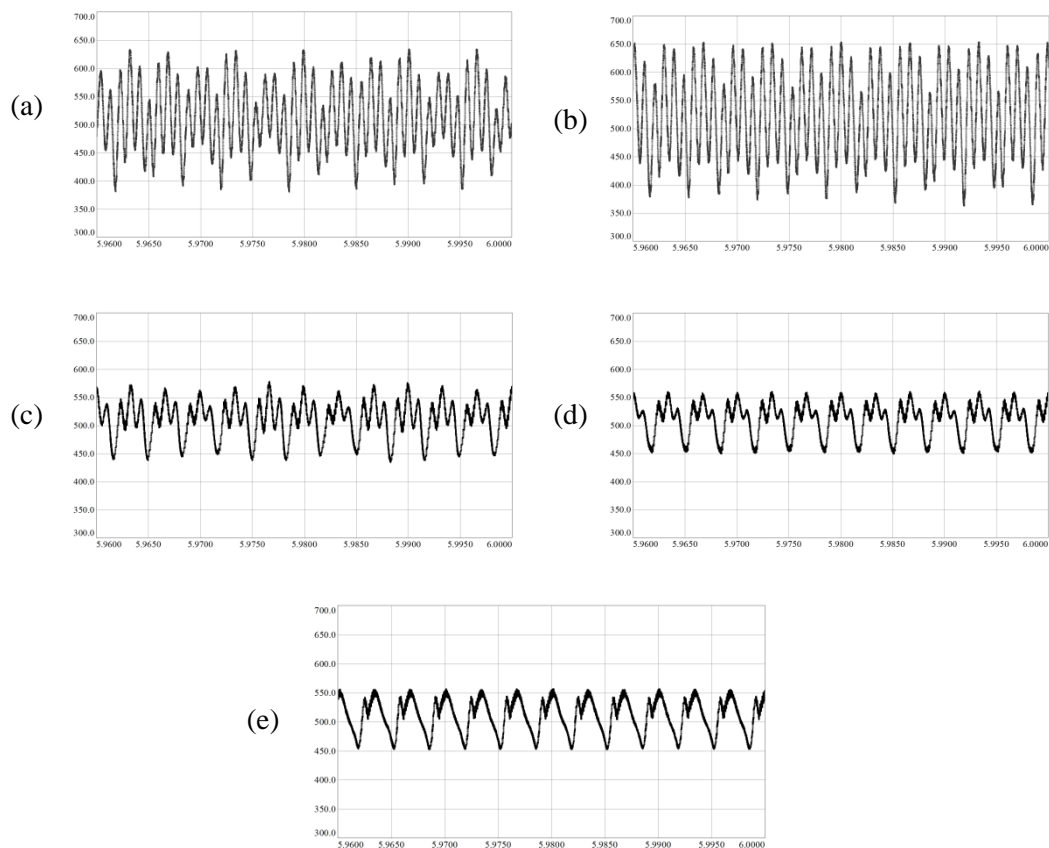


Figure 5.83 DC bus voltage waveforms for 2.2 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (50 V/div, 5 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3.

To investigate the stability of the dc bus voltage, the voltage circles are provided in Figure 5.84.

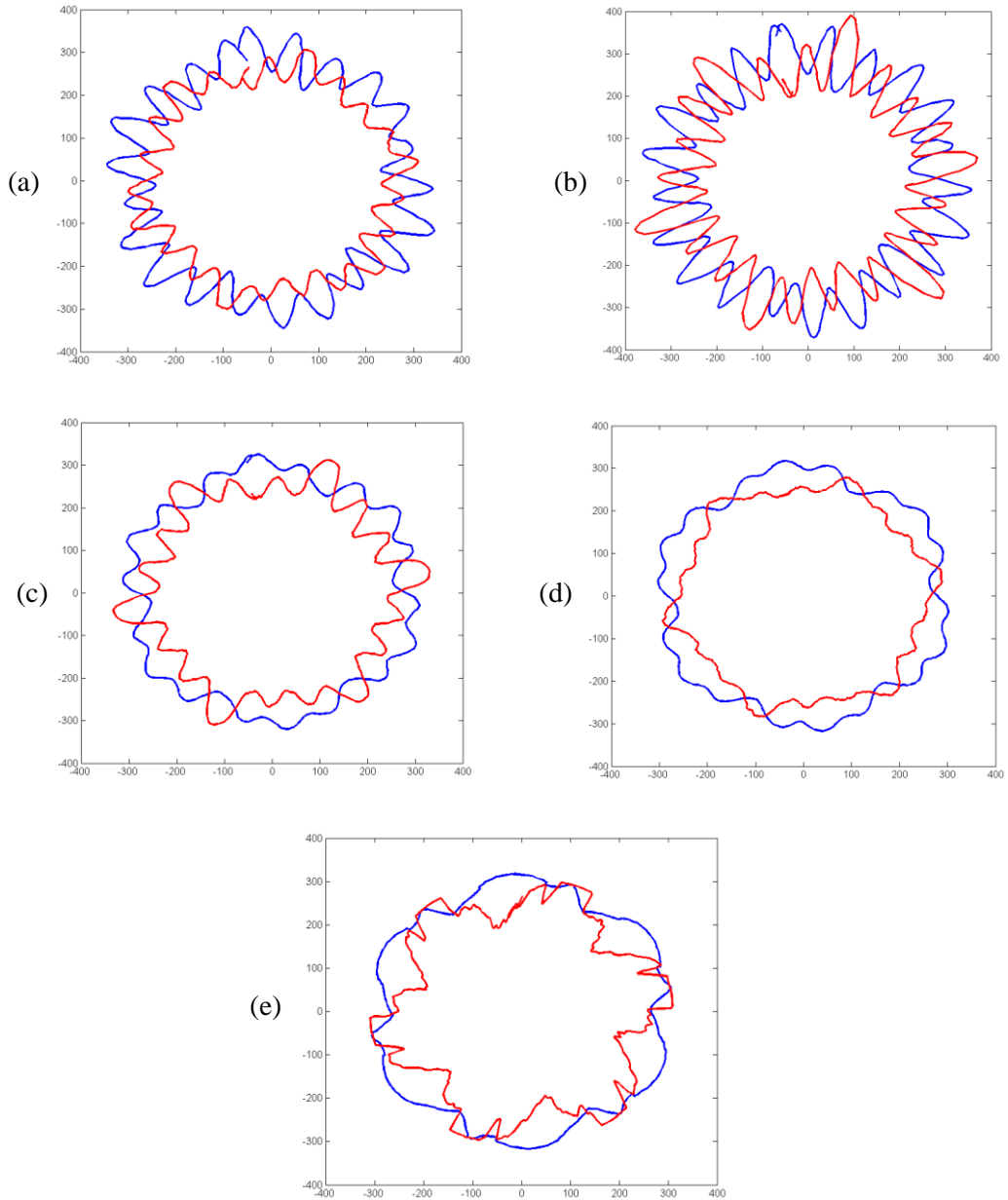


Figure 5.84 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (100 V/div, 100 V/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3.

As deduced from Figure 5.84, each method offers different stabilization effect on the dc bus as understood from the shape of the circles. The resonant voltage components are suppressed sufficiently by Method 2 and Method 3. Figure 5.85 shows the motor torque waveforms for the drive.

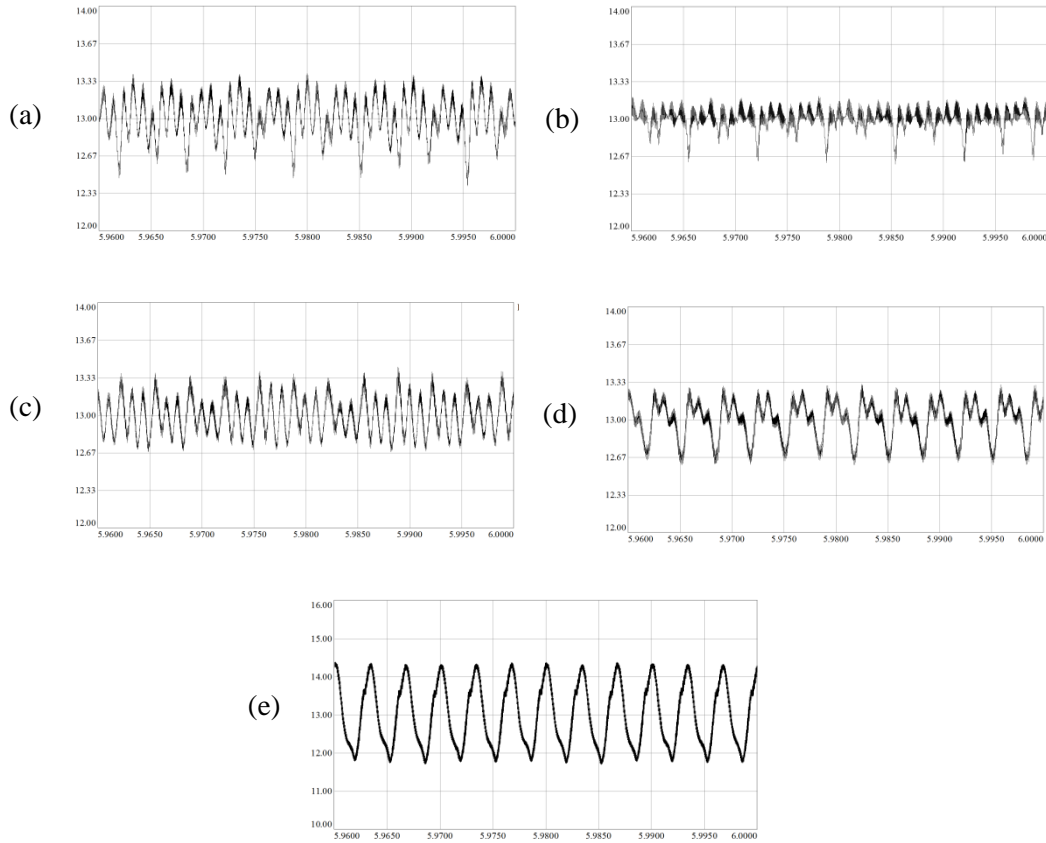


Figure 5.85 Motor torque waveforms of 2.2 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (0.33 N.m V/div, 5 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3 (1 N.m/div, 5 ms/div).

The dc bus disturbance rejection still decreases the torque ripple despite the high voltage oscillations on the dc link. The active control methods show different performance in terms of torque ripple. The torque ripple without dc bus disturbance rejection and Method 1 are close in torque ripple values. Method 3 resulted in highest torque ripple among the control methods.

Figure 5.86 shows the line current waveforms for the drive. The line currents are considerably improved by the active stabilization methods when compared to cases with and without dc bus disturbance rejection. The methods differ in terms of THD_{ig} values as can be realized from the waveforms clearly.

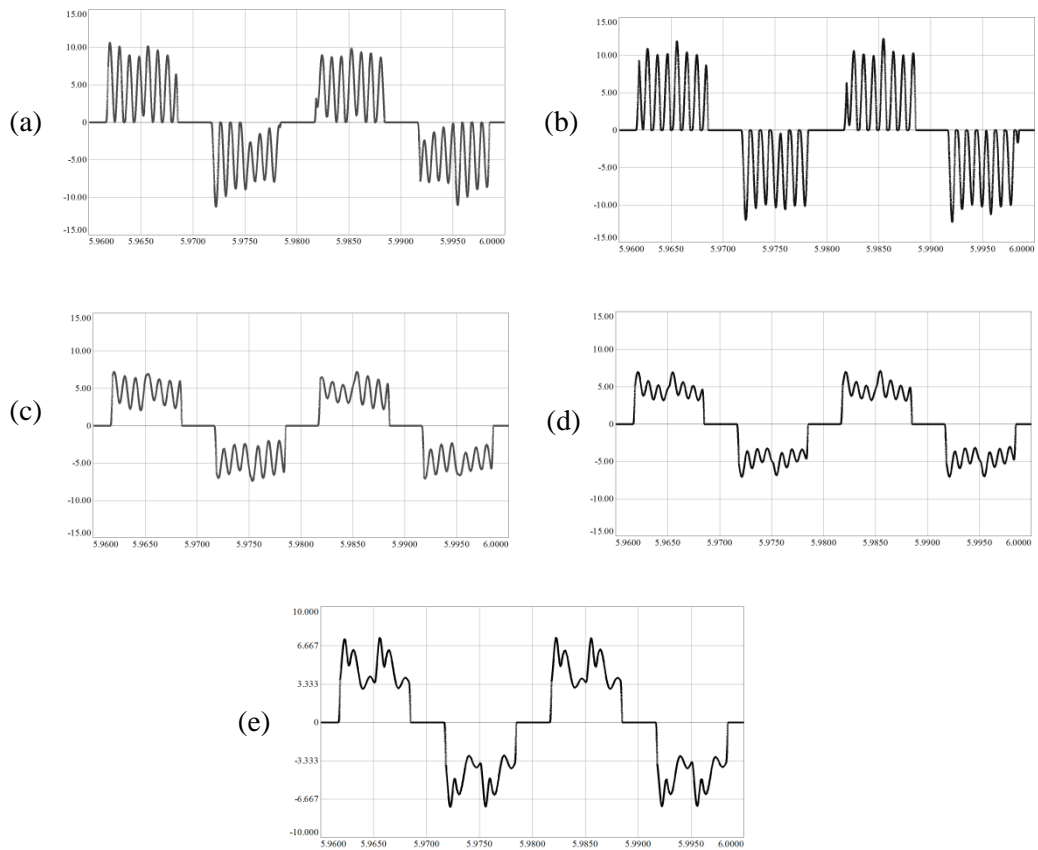


Figure 5.86 Line current waveforms of 2.2 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (5 A/div, 5 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3 (3.33 A/div, 5 ms/div).

5.8.2 37 kW Motor Drive Constant Torque Load Operation Simulation Results

Figure 5.87 shows the dc bus voltage waveforms for the 37 kW constant torque load drive. The active stabilization methods show similar performance by keeping the voltage ripple around 100 V via suppression of high frequency resonance harmonics on the voltage. The dc bus disturbance rejection further increased the bus voltage oscillations.

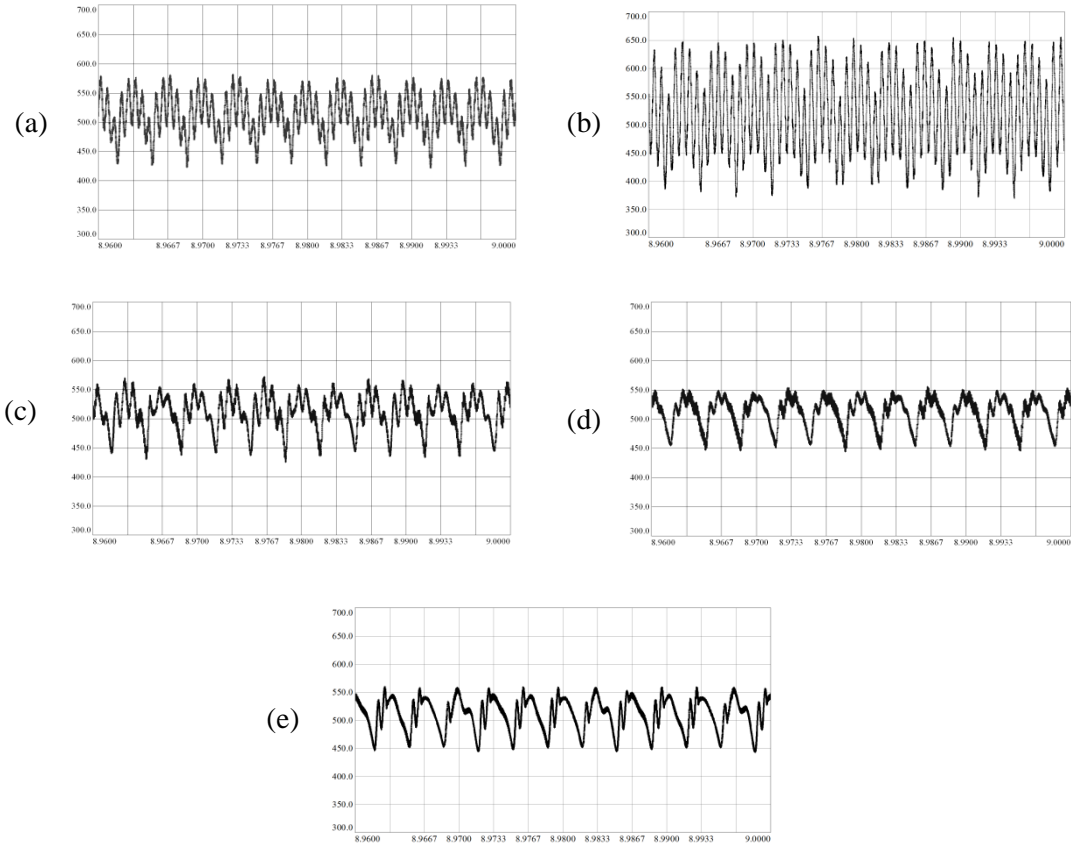


Figure 5.87 DC bus voltage waveforms of 37 kW low C_{dc} motor drive operating under constant torque load with dc link inductor, all (50 V/div, 3.3 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3.

The voltage circles are provided in Figure 5.88 to investigate the stability of the dc bus voltage.

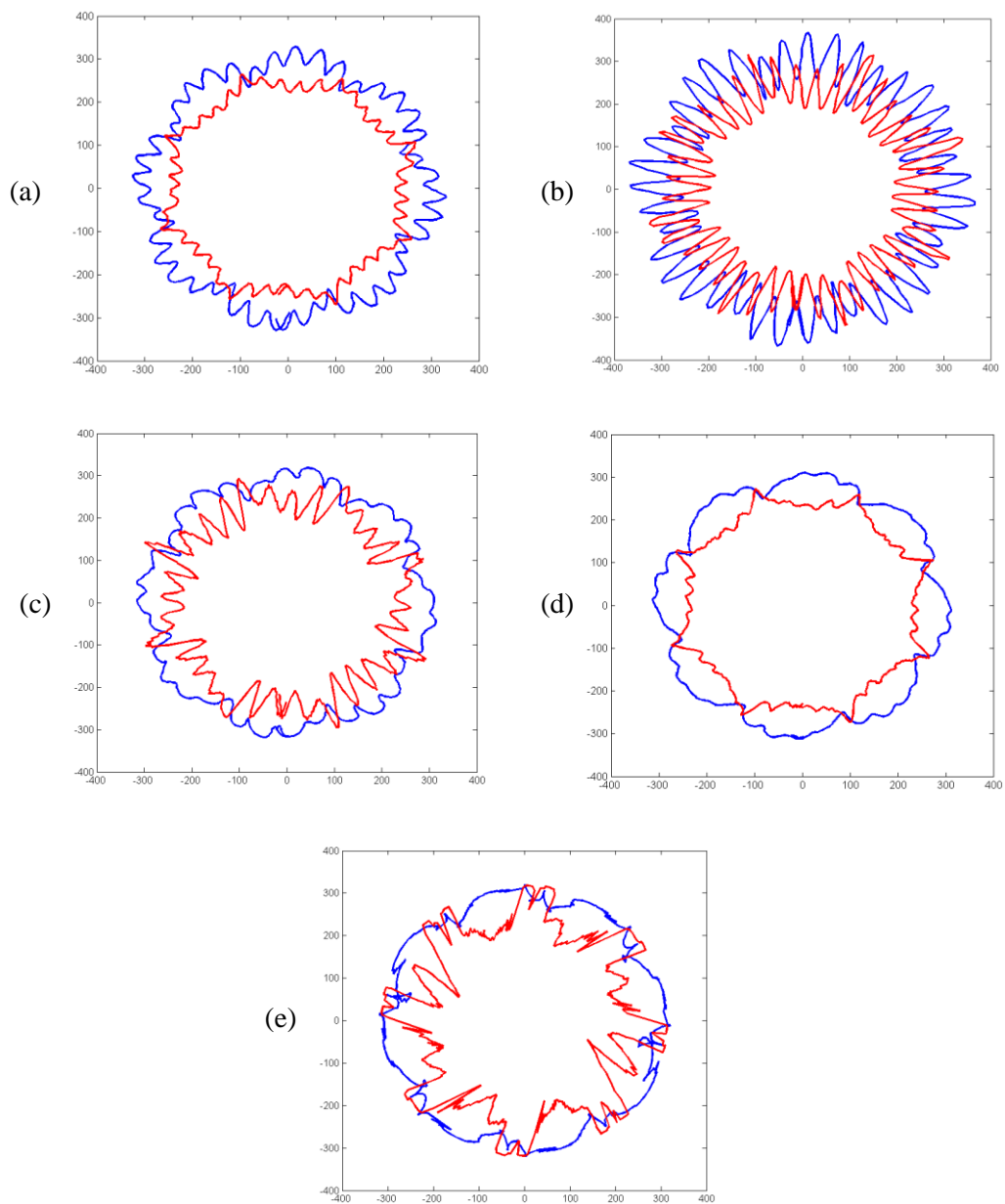


Figure 5.88 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 37 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (100 V/div, 100 V/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3.

Figure 5.89 includes the torque waveforms of the 37 kW motor with constant torque load. Similar to the 2.2 kW drive, dc bus disturbance rejection eliminated the 300 Hz torque

ripple. Among the active control methods, Method 1 and Method 2 yielded torque ripple close to each other and Method 3 has the highest torque ripple among them, as is the case in 2.2 kW drive.

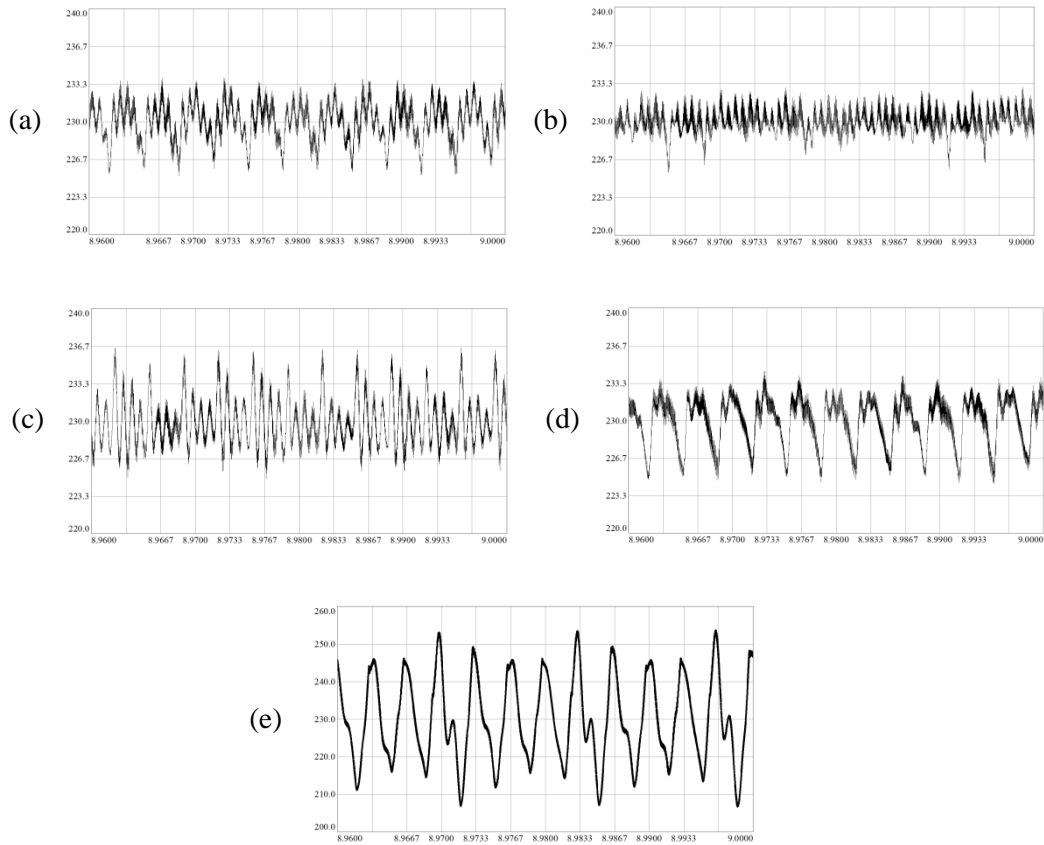


Figure 5.89 Motor torque waveforms of 37 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (3.33 N.m/div, 3.3 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3 (10 N.m/div, 3.3 ms/div).

Figure 5.90 illustrates the line current waveforms of the 37 kW drive with constant torque load. The worst line current is observed with dc bus disturbance rejection case as expected due to increased instability.

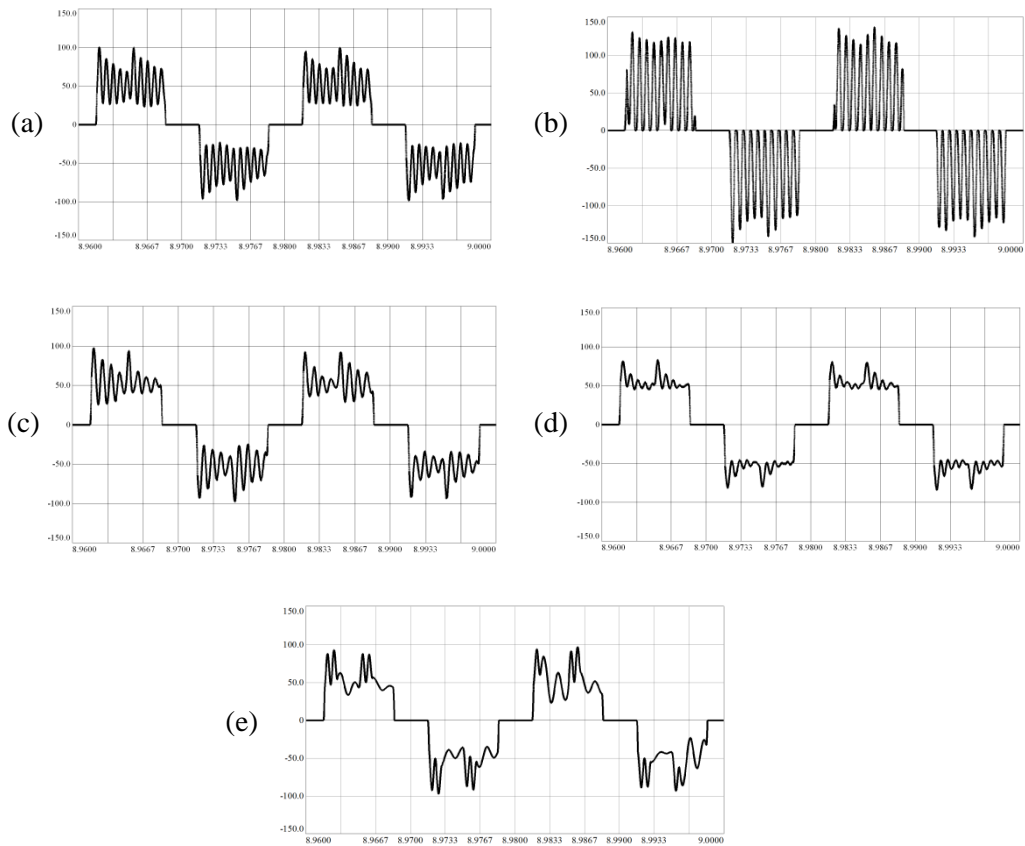


Figure 5.90 Line current waveforms of 37 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (50 A/div, 3.3 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3.

5.8.3 2.2 kW Motor Drive Fan Load Operation Simulation Results

The performance of the drive with dc link inductor operating under fan load is also investigated with active stabilization methods. The results of the simulations are so close to the constant torque load case. Figure 5.91 shows the dc bus voltage waveforms. Active stabilization methods suppressed the dc link resonant oscillations and yielded 100 V pp ripple. The bus voltage is prone to instability with and without dc bus disturbance rejection.

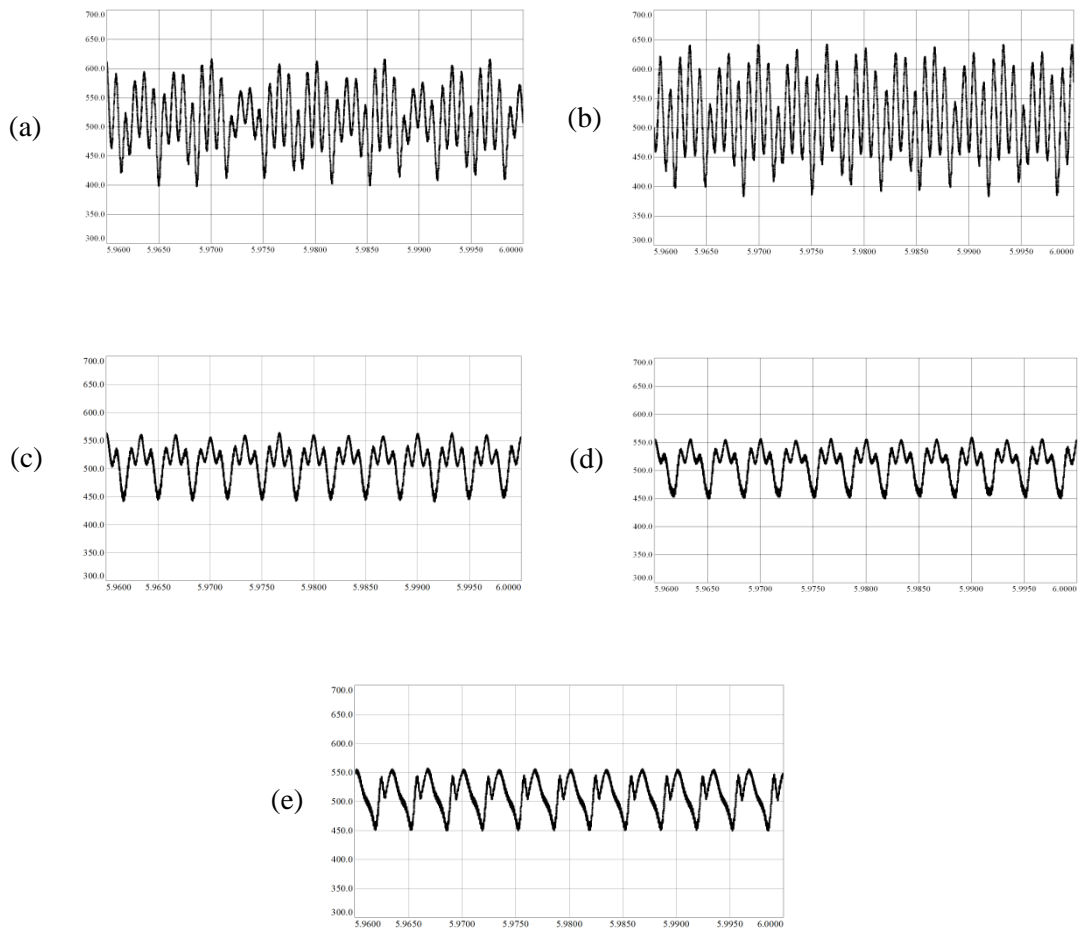


Figure 5.91 DC bus voltage waveforms of 2.2 kW low C_{dc} motor drive operating under fan load with dc link inductor (50 V/div, 5 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3.

Figure 5.92 shows the motor torque waveforms. The performances of the control methods are similar to that in constant torque load case. The dc bus disturbance rejection gives the minimum torque ripple and Method 3 has the highest ripple among active control methods.

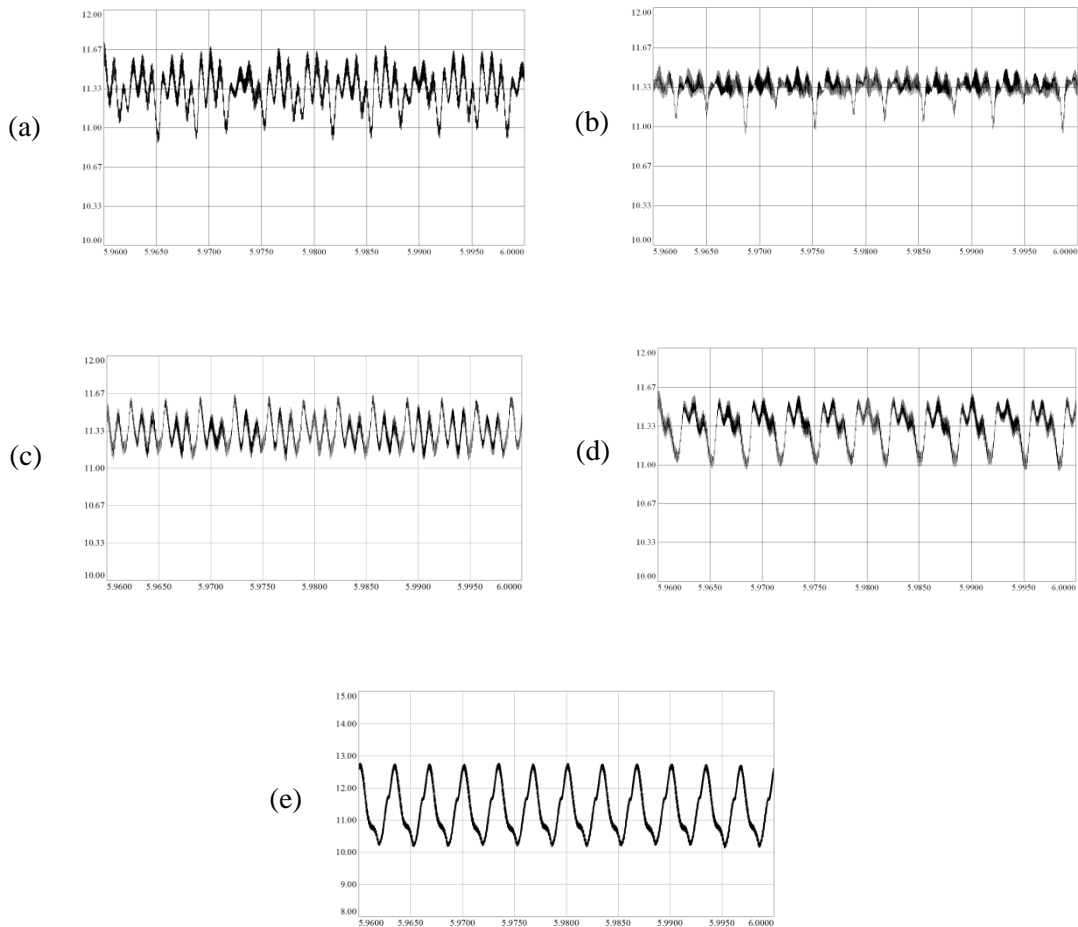


Figure 5.92 Motor torque waveforms of 2.2 kW low C_{dc} motor drive operating under fan load with dc link inductor (0.33 N.m V/div, 5 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3 (1 N.m/div, 5 ms/div).

Figure 5.93 illustrates the line current waveforms. The dc bus disturbance rejection caused highest harmonic distortion as expected. The active stabilization methods significantly improve the line current quality as understood from the decreased amplitude of the resonant components on the waveforms. Each method offers different performances. The THD_{ig} obtained from the simulations are around 40 % for the actively stabilized systems (detailed data are given in Chapter 6).

The selected parameters in the simulation of the stabilization algorithms are also important in the performance figures. Although the main principle of the algorithm does not change, the parameters used can affect the performance considerably.

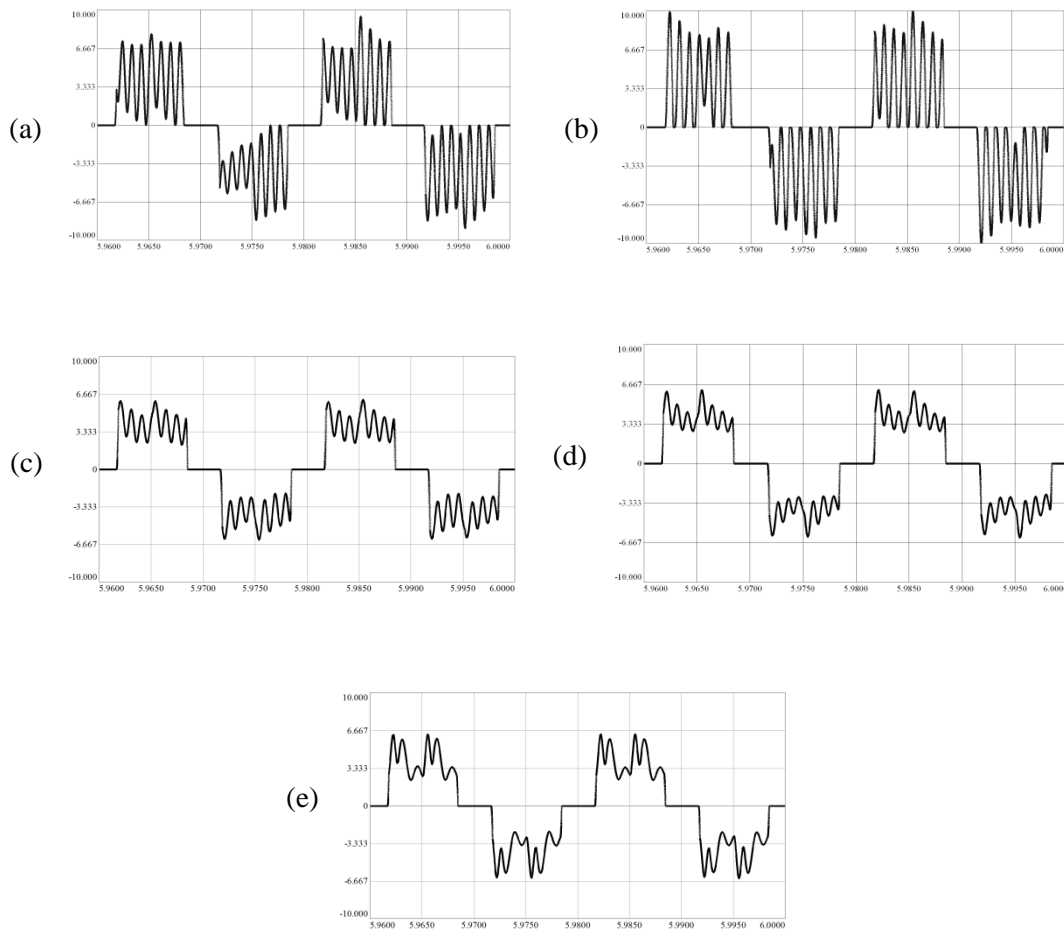


Figure 5.93 Line current waveforms of 2.2 kW low C_{dc} motor drive operating under fan load with dc link inductor (3.33 A/div, 5 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3.

5.8.4 37 kW Motor Drive Fan Load Operation Simulation Results

Figure 5.94 shows the dc bus voltage waveforms for the 37 kW fan load drive. The active stabilization methods resulted in approximately 100 V pp voltage ripple for an average 511 V dc bus voltage. The dc bus disturbance rejection method increased the oscillations as expected.

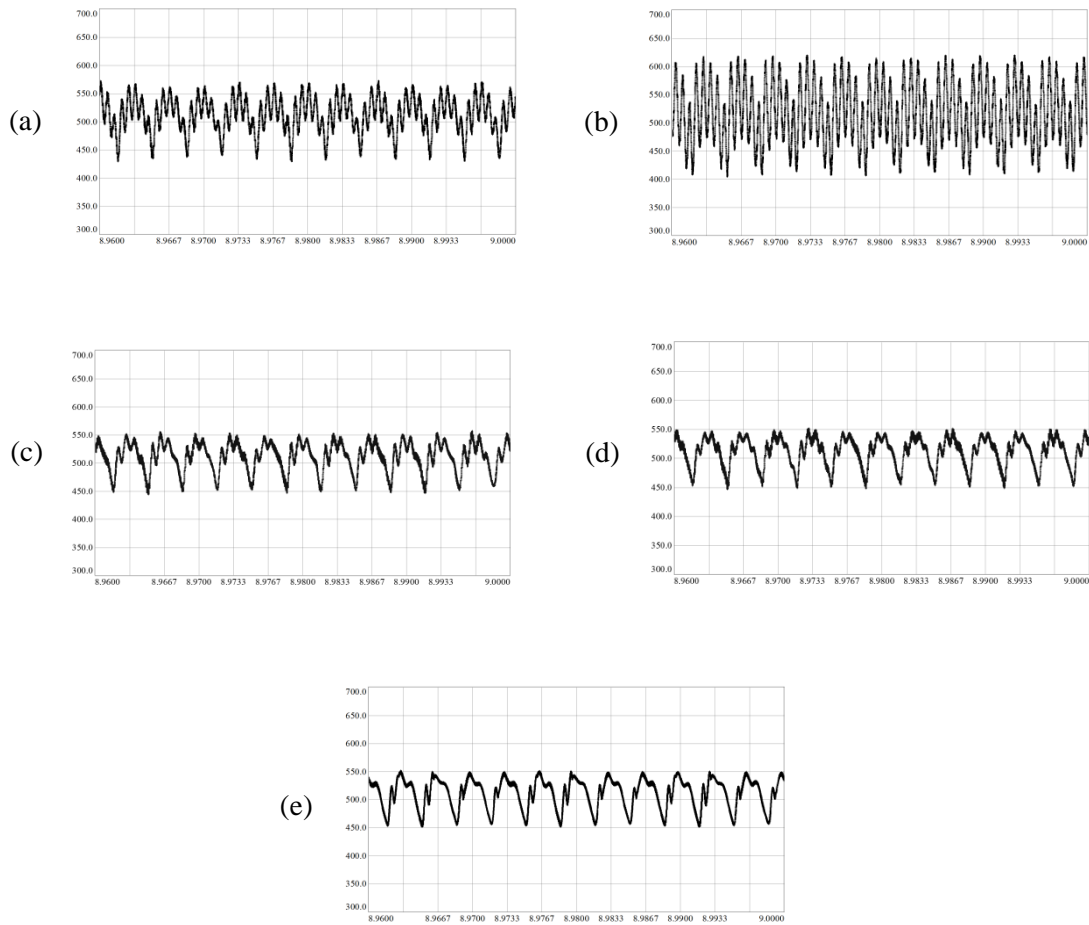


Figure 5.94 DC bus voltage waveforms of 37 kW low C_{dc} motor drive operating under fan load with dc link inductor (50 V/div, 3.3 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3.

Figure 5.95 shows the motor torque waveforms for 37 kW fan load drive. Since the torque of the fan load is speed dependent, the steady state torque for fan load operation is lower than the constant torque load operation and hence the motor draws less power. Similar to constant torque load case, dc bus disturbance rejection eliminated the 300 Hz ripple.

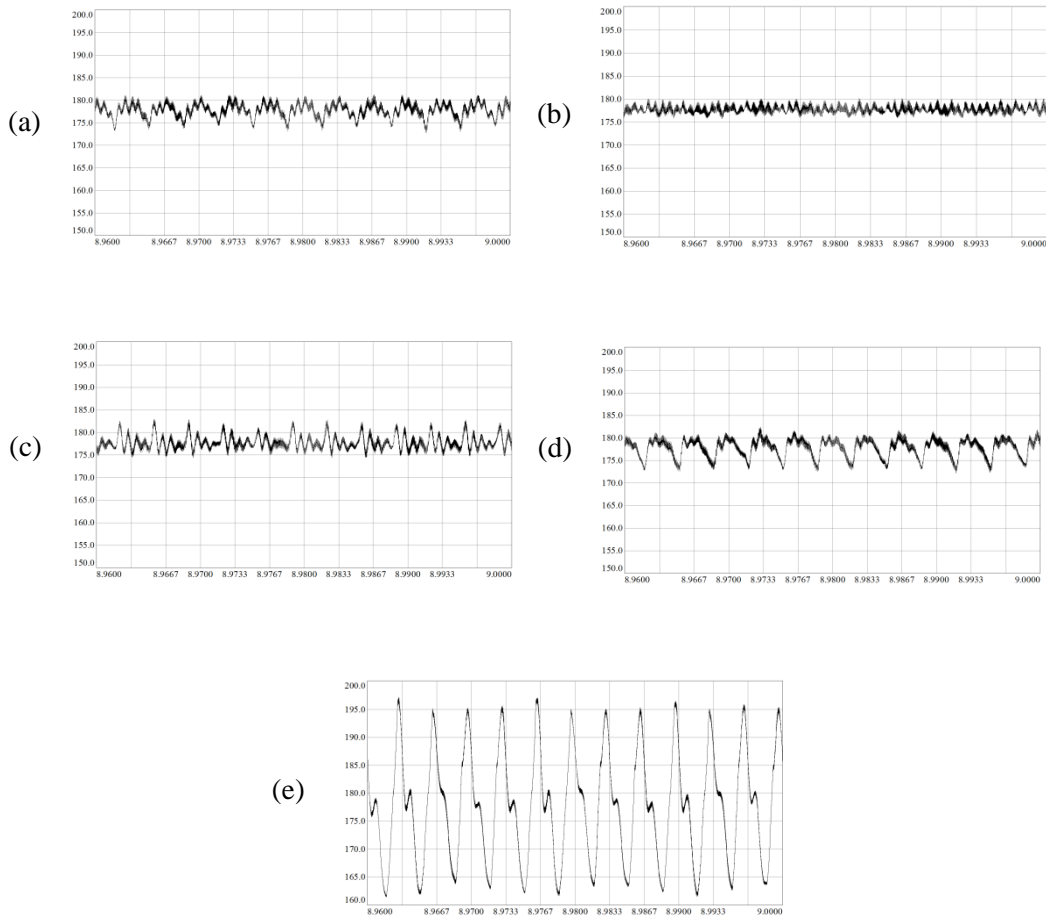


Figure 5.95 Motor torque waveforms of 37 kW low C_{dc} motor drive operating under fan load with dc link inductor (5 N.m/div, 3.3 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3.

Figure 5.96 illustrates the line currents for the 37 kW fan drive. The Method 2 and Method 3 show close performance among the active control methods. The worst case is seen on the drive with dc bus disturbance rejection.

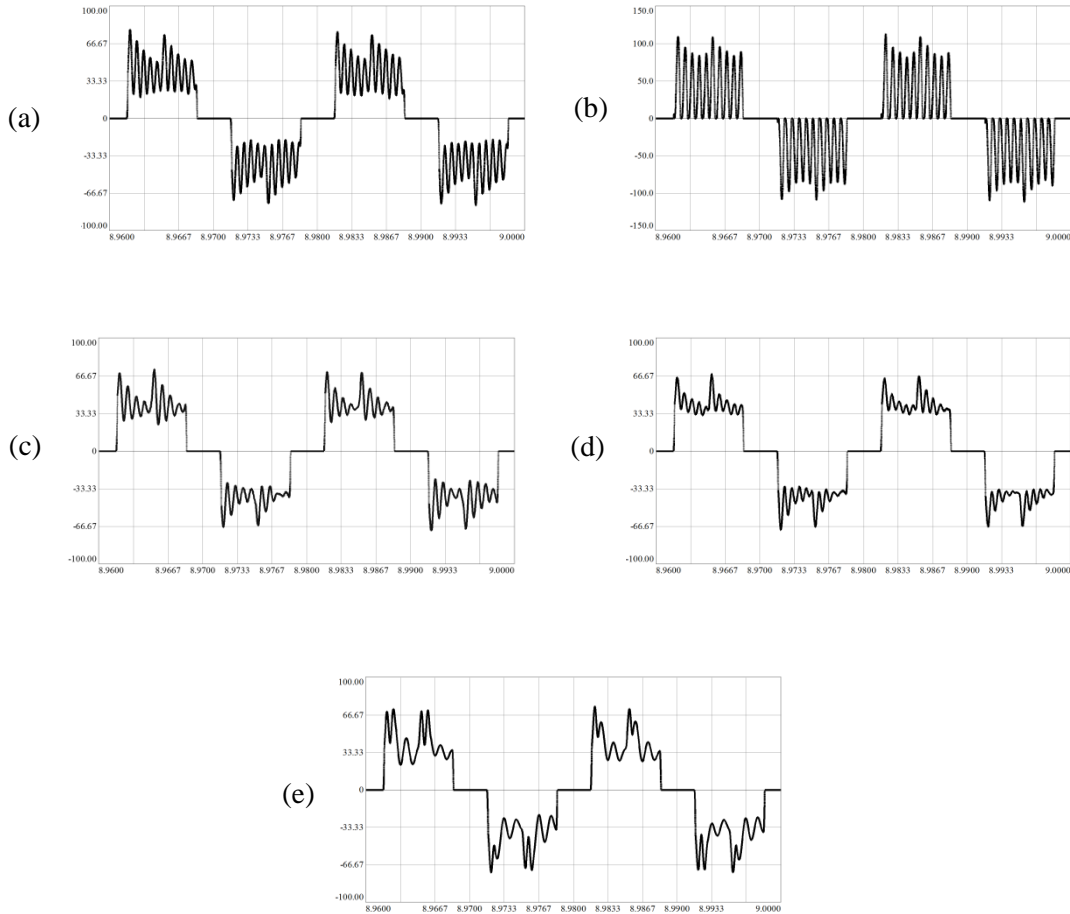


Figure 5.96 Line current waveforms of 37 kW low C_{dc} motor drive operating under fan load with dc link inductor (33.3 A/div, 3.3 ms/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3.

5.9 Conclusion

In this chapter, the design of motor drive equipped with low C_{dc} dc bus capacitor is investigated. The simulations are conducted for the circuits including dc link inductor and without dc link inductor to analyze the stability. When the dc link resonant frequency is set at an appropriate value, the low C_{dc} motor drives without dc link inductor shows satisfactory performance both in terms of dc bus voltage stability and line current quality. However, if the L/C ratio of the circuit increases by means of a DC link inductor, the stabilization is lost and active stabilization of dc bus voltage is required. Some of the active control methods found in literature are applied in the simulations and compared in terms of motor drive performance. The next chapter compares the performance of both conventional drive and drives with low C_{dc} dc bus capacitor via the simulation data.

CHAPTER 6

PERFORMANCE EVALUATION AND COMPARISON OF CONVENTIONAL AC MOTOR DRIVES AND DRIVES UTILIZING LOW CAPACITANCE DC BUS CAPACITOR

6.1 Introduction

This chapter evaluates and compares the performance of the conventional drives and drives with low C_{dc} dc bus capacitor. Each type of drive is investigated in terms of dc bus voltage quality, input power quality and motor motion quality. First the data obtained from the simulation of the conventional motor drives with front end diode rectifier are analyzed and some interpretations are made. Next, the data obtained from the simulations of low C_{dc} motor drives are investigated.

6.2 Performance Evaluation of Conventional Motor Drives

Table 6.1 includes the data obtained from the simulation results for conventional drives at high M_i operation. At first glance, it is seen that the input power quality, bus voltage characteristics and motor motion quality are very close with dc bus disturbance rejection applied and not applied. This is due to stiff and low ripple dc bus voltage which is not affected from the negative impedance effect of the dc bus disturbance rejection. Since the average value of the dc bus voltage is already sufficient, the dc bus disturbance rejection does not bring considerable effect on the performance of the conventional motor drive. The steady state performance data of the fan and constant torque load drive are also very close to each other at high M_i . This can be explained by the fact that the motor reaches steady state operation at the set speed, the torque at the steady state operation point has also a constant value, whether it is fan or constant torque load. So, both the fan and constant torque load imposes same effect to the dc bus at steady state operation point and the

waveforms are very similar. Both 2.2 kW and 37 kW motor drives yield THD_{ig} less than 30 % and PF around 0.93, which can be interpreted as satisfactory performance for input power quality. The torque ripple is less than 3 %, which indicates a good motion quality.

Table 6.1 Simulation data of the conventional motor drives with front end diode rectifier operating at $M_i=0.83$.

Drive and load type	Power (kW)	DC bus voltage ripple pp (V-%)	THD_{ig} %	PF	Torque ripple pp (N.m-%)
Fan drive without dc bus disturbance rejection	2.2	3.19 – 0.6 %	29.4	0.931	0.3 – 2.3 %
Fan drive with dc bus disturbance rejection		3.19 – 0.6 %	29.4	0.931	0.3 – 2.3 %
Constant torque load drive without dc bus disturbance rejection		2 – 0.4 %	29.4	0.931	0.3 – 2.3 %
Constant torque load drive with dc bus disturbance rejection		3 – 0.6 %	29.4	0.931	0.2 – 1.6 %
Fan drive without dc bus disturbance rejection	37.0	2.7 – 0.5 %	32.4	0.928	3.6 – 1.6 %
Fan drive with dc bus disturbance rejection		2.3 – 0.4 %	32.4	0.928	3.3 – 1.4 %
Constant torque load drive without dc bus disturbance rejection		2.8 – 0.57 %	32.4	0.928	3.4 – 1.5 %
Constant torque load drive with dc bus disturbance rejection		2.9 – 0.57 %	32.4	0.928	3.5 – 1.5 %

Table 6.2 includes the simulation results of the conventional motor drive operating at low M_i around 0.53. As expected, the THD_{ig} is increased as the operating power is decreased. This is more obvious in the fan load case since the operating torque decrease with the square of the motor speed and power decreases with the cube of it. Thus, compared to the constant torque load, the operating power of the fan load at low M_i is lower and THD_{ig} is higher.

Table 6.2 Simulation data of the conventional motor drives with front end diode rectifier operating at $M_i=0.53$.

Drive and load type	Power (kW)	DC bus voltage ripple pp (V-%)	THD_{ig} %	Input PF	Torque ripple pp (N.m-%)
Fan drive without dc bus disturbance rejection	2.2	2.5 – 0.5 %	48.0	0.880	0.25 – 4.3 %
Fan drive with dc bus disturbance rejection		2.5 – 0.5 %	48.0	0.880	0.25 – 4.3 %
Constant torque load drive without dc bus disturbance rejection		2.7 – 0.5 %	34.5	0.924	0.28 – 1.7 %
Constant torque load drive with dc bus disturbance rejection		2.7 – 0.5 %	34.4	0.924	0.27 – 2 %
Fan drive without dc bus disturbance rejection	37.0	2 – 0.4 %	63.5	0.823	3.7 – 4 %
Fan drive with dc bus disturbance rejection		2 – 0.4 %	63.4	0.823	5 – 5.3 %
Constant torque load drive without dc bus disturbance rejection		2.5 – 0.5 %	40.1	0.909	3.3 – 1.4 %
Constant torque load drive with dc bus disturbance rejection		2.5 – 0.5 %	40.2	0.910	3.3 – 1.4 %

6.3 Performance Evaluation of Low C_{dc} Motor Drives

The simulations conducted for the low C_{dc} motor drive show that the motor drive without dc link inductor yields stable results, whereas the motor drive with dc link inductor is prone to high instability. The performance of the active stabilization methods differ in terms of the suppression of the dc bus voltage oscillations, the motor torque ripple, and input power quality. Table 6.3 includes the simulation data for the stable drive without dc link inductor and operating at high modulation index $M_i=0.83$.

Table 6.3 The simulation data obtained from the low C_{dc} motor drive without dc link inductor operating at $M_i=0.83$.

Drive and load type	Power (kW)	DC bus voltage ripple pp (V-%)	PF	THD _{ig} (%)	Torque ripple pp (N.m-%)
Constant torque load with disturbance rejection	2.2	157.5 – 30.8 %	0.780	81.0	0.2 – 1.76 %
Constant torque load without disturbance rejection		100 – 19.6 %	0.938	36.4	0.43 – 3.8 %
Fan load with disturbance rejection		146.5 – 28.7 %	0.789	77.3	0.28 – 2.5 %
Fan load without disturbance rejection		100 – 19.6 %	0.936	36.7	0.46 – 4.1 %
Constant torque load with disturbance rejection	37.0	151 – 29.5 %	0.792	76.6	3.8 – 2.14 %
Constant torque load without disturbance rejection		100 – 19.6 %	0.945	34.0	6.6 – 3.72 %
Fan load with disturbance rejection		136 – 26.6 %	0.821	69.0	3.4 – 1.92 %
Fan load without disturbance rejection		100 – 19.6 %	0.937	36.5	6.2 – 3.5 %

Table 6.4 The simulation data obtained from the low C_{dc} motor drive without dc link inductor operating at $M_i=0.46$.

Drive and load type	Power (kW)	DC bus voltage ripple pp (V-%)	PF	THD _{ig} (%)	Torque ripple pp (N.m-%)
Constant torque load with disturbance rejection	2.2	123 – 24.1 %	0.827	67.5	0.22 – 1.5 %
Constant torque load without disturbance rejection		104 – 20.4 %	0.915	43.6	0.43 – 3.3 %
Fan load with disturbance rejection		91 – 17.8 %	0.847	61.8	0.25 – 4.3 %
Fan load without disturbance rejection		90 – 17.6 %	0.848	61.6	0.38 – 6.5 %
<hr/>					
Constant torque load with disturbance rejection	37.0	116 – 22.7 %	0.859	58.7	3.4 – 1.5 %
Constant torque load without disturbance rejection		100 – 19.6 %	0.928	39.5	5.39 – 2.3 %
Fan load with disturbance rejection		100 – 19.6 %	0.836	64.3	4.0 – 4.8 %
Fan load without disturbance rejection		100 – 19.6 %	0.852	60.2	5.27 – 6.3 %

As Table 6.3 and Table 6.4 are analyzed, first it is seen that for operation at $M_i=0.83$, the THD_{ig} values are near 36 % for both 2.2 kW and 37 kW drives even without using a separate inductor filter. This is close to the performance of the conventional motor drive with filter inductors. For stable operation without dc link inductor, 2.2 kW and 37 kW drives have very close dc bus voltage ripple values and input power factors. The 37 kW drive has slightly better THD_{ig} values than 2.2 kW drive. This is due to the fact that the percentage of the harmonic content to the fundamental current component is lower for the 37 kW drive since the rms value of the fundamental component is higher compared to 2.2 kW drive. A similar observation can be made for THD_{ig} values by considering the

operations at high and low modulation index values. The THD_{ig} values are higher for low M_i operation since the total power is lower and the percentage of the harmonic content to fundamental becomes higher. Another observation can be made between the fan load and constant torque load THD_{ig} values. As stated in the beginning of the chapter, the 2.2 kW drive is simulated to deliver 86 % power with constant torque load whereas delivers 75 % power for fan load. Due to this difference, the fan load drawing less power yields higher THD_{ig} values than the constant torque load simulations. Likewise, the 37 kW drive delivers 26.4 kW power (~72 %) at 1100 rpm – 230 N.m for constant torque load and 20.4 kW power (~55 %) at 1100 rpm for fan load and THD_{ig} increases for fan load. In conclusion, the THD_{ig} values decrease as the operating power increases. The PF also increases when the operating power increases since the THD_{ig} decreases. The dc bus voltage ripple is significantly increased by disturbance rejection and does not depend on considerably to the operation M_i . The motor torque ripple is decreased nearly 50 % by application of disturbance rejection.

Table 6.5 and Table 6.6 include the data of the simulations of the constant torque load drives with dc link inductor. When the dc bus voltage ripple and THD_{ig} values are analyzed, it is observed that the drive has unstable operation with and without dc bus disturbance rejection methods. The 2.2 kW drive has nearly 50 % dc bus voltage ripple, which shows the level of high instability. The active control methods successively improve the stability of the unstable drives and reduce the dc bus voltage ripple by approximately 50 %. The input power qualities of the drives are also improved by the stabilization methods. All active control methods have close performance to each other at high M_i operation yielding nearly 40 % THD_{ig} .

Among the stabilization methods, Method 3 yields similar performance with the Method 1 and Method 2 in terms of dc bus voltage and input power quality but generates higher torque ripple. This can be explained by the implementation principle of the method, that is the signal injection directly to the torque current (q axis current) of the motor. So, any imperfections or insufficient tuning of the stabilization controller can easily disturb the q axis current and cause torque ripple on the motor.

Table 6.5 The simulation data obtained from the actively stabilized low C_{dc} motor drive with dc link inductor under constant torque load operating at $M_i=0.83$.

Method	Power (kW)	DC bus voltage ripple pp (V-%)	PF	THD _{ig} (%)	Torque ripple pp (N.m-%)
Without disturbance rejection	2.2	248 – 48.6 %	0.795	75.6	0.95 – 7.3 %
With disturbance rejection		277 – 54.2 %	0.734	92.0	0.54 – 4.2 %
Method 1		141 – 27.6 %	0.920	42.4	0.67 – 5.2 %
Method 2		110 – 21.5 %	0.934	37.9	0.70 – 5.4 %
Method 3		107 – 21 %	0.926	41.4	2.59 – 19.9 %
Without disturbance rejection	37.0	147 – 28.7 %	0.900	48.1	8.4 – 3.6 %
With disturbance rejection		276 – 54.0 %	0.730	93.0	6.1 – 2.6 %
Method 1		135 – 26.4 %	0.920	42.2	11 – 4.8 %
Method 2		100 – 19.6 %	0.943	34.8	8.3 – 3.6 %
Method 3		116 – 23 %	0.912	44.1	43.6 – 18.9 %

To make a comparison of stability at different load power levels for the operation with dc link inductor, that is, when the stability is lost, the voltage circles can be used. Figure 6.1 and Figure 6.2 show the voltage circles obtained for the actively stabilized motor drives with dc link inductor and operating under constant torque load for the 2.2 kW and 37 kW rated motor drives respectively.

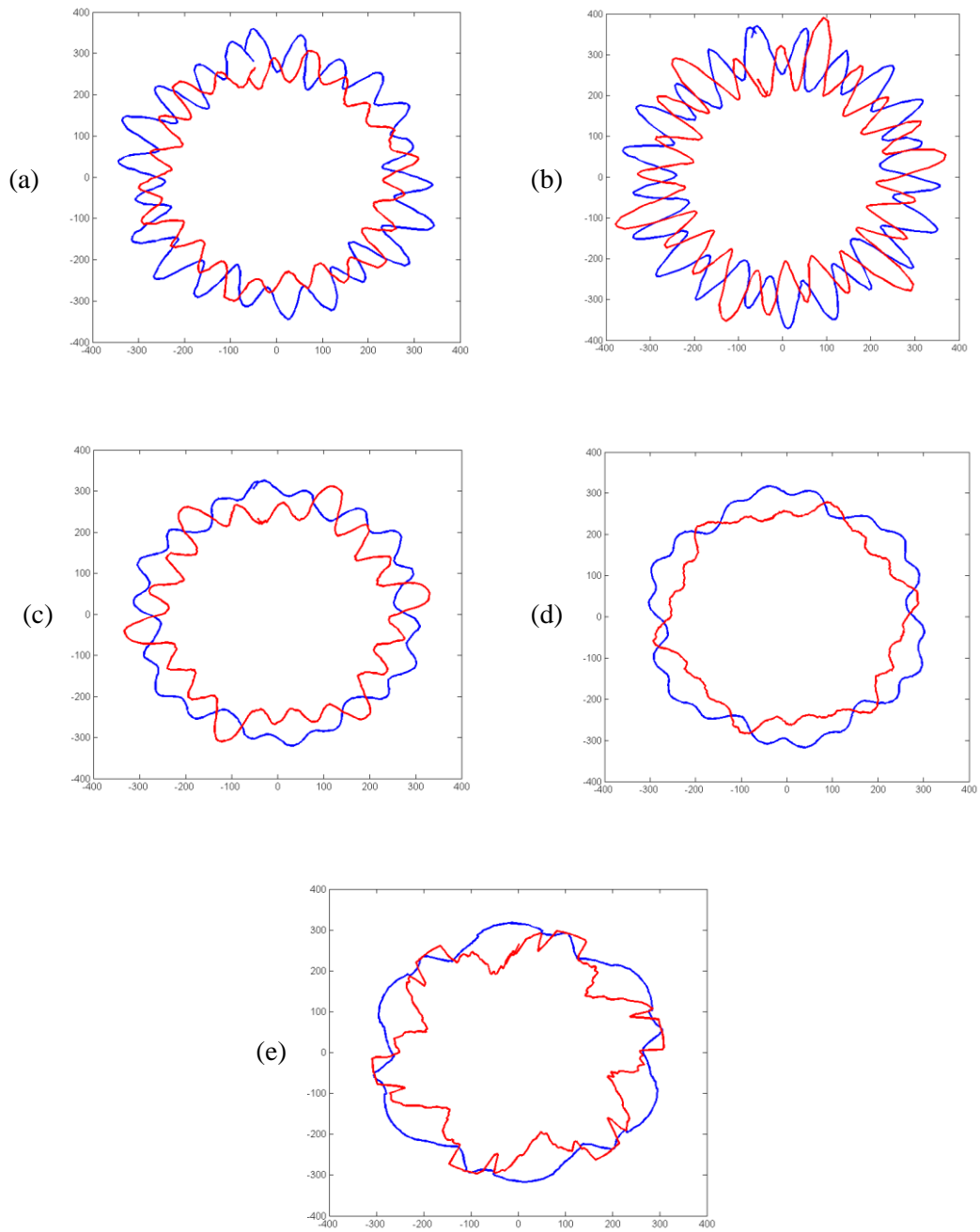


Figure 6.1 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 2.2 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (100 V/div, 100 V/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3.

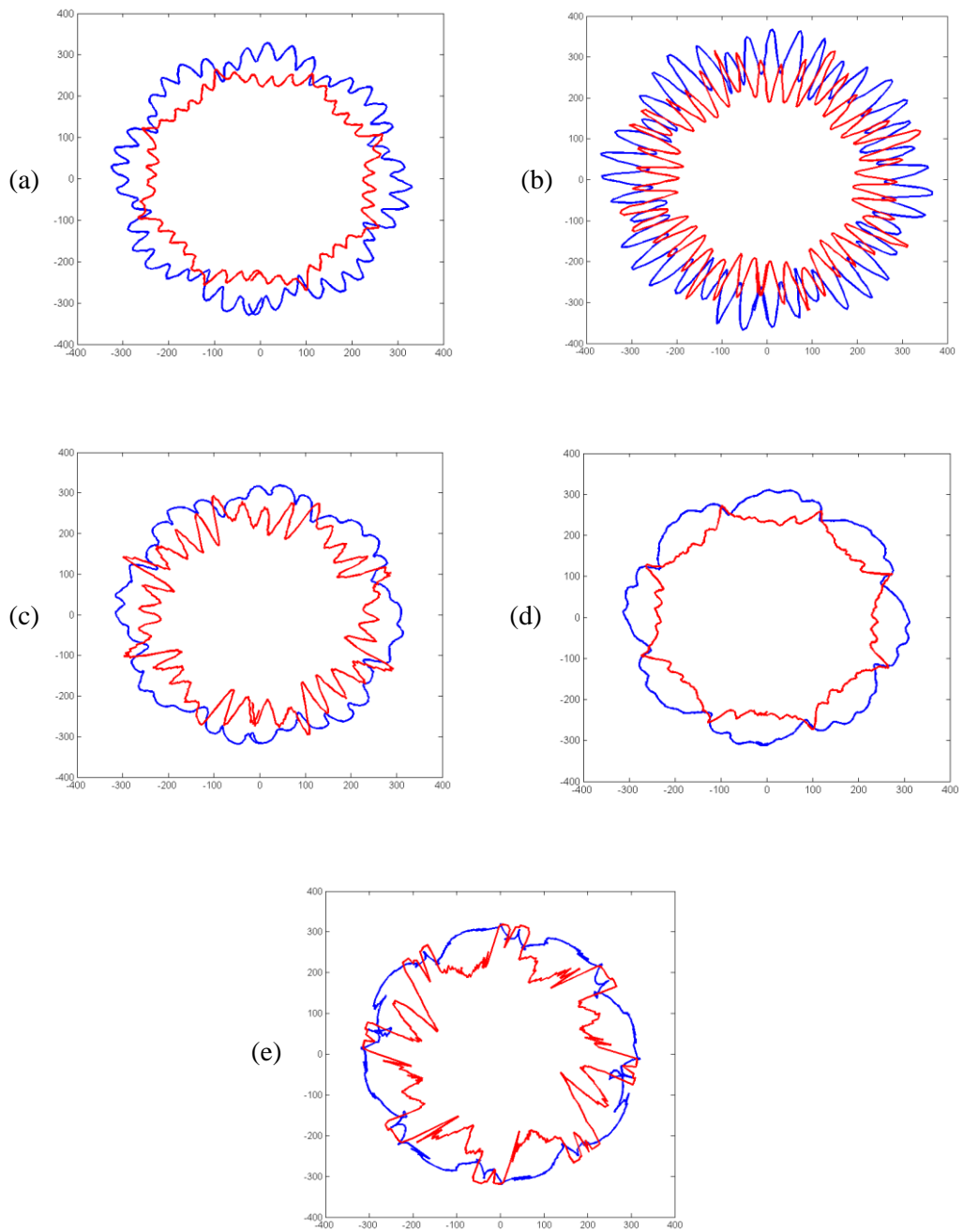


Figure 6.2 The available inverter voltage limit (blue) and the voltage demand from SFCR (red) of 37 kW low C_{dc} motor drive operating under constant torque load with dc link inductor (100 V/div, 100 V/div) (a) without dc bus disturbance rejection (b) with dc bus disturbance rejection (c) with Method 1 (d) with Method 2 (e) with Method 3.

As the circles for the operation without dc bus disturbance rejection (for which the circuits are operating with their natural damping conditions) are analyzed, it is realized that the 37 kW motor drive generates approximately 40 % lower pp voltage ripple than the 2.2 kW motor drive. From this result it can be deduced that the stability for the higher power levels is relatively higher than the low power operations.

Table 6.6 The simulation data obtained from the actively stabilized low C_{dc} motor drive with dc link inductor under constant torque load operating at $M_i=0.46$.

Method	Power (kW)	DC bus voltage ripple pp (V-%)	PF	THD _{ig} (%)	Torque ripple pp (N.m-%)
Without disturbance rejection	2.2	170 – 33.0 %	0.833	65.8	0.48 – 3.7 %
With disturbance rejection		210 – 41.0 %	0.762	84.5	0.23 – 1.8 %
Method 1		112 – 22.0 %	0.913	44.0	0.47 – 3.6 %
Method 2		102 – 20.0 %	0.917	42.9	0.46 – 3.5 %
Method 3		123 – 24.0 %	0.794	75.5	3.63 – 27 %
Without disturbance rejection	37.0	147 – 29.0 %	0.849	61.7	6.3 – 2.7 %
With disturbance rejection		190 – 37.2 %	0.731	92.8	4.0 – 1.7 %
Method 1		100 – 19.5 %	0.923	41.1	6.0 – 2.6 %
Method 2		106 – 20.7 %	0.922	41.3	7.33 – 3.2 %
Method 3		106 – 20.7 %	0.749	87.0	50.0 – 21.7 %

Table 6.7 and Table 6.8 include the simulation results for the fan load drive. As stated previously, the lower operation power results in increased THD_{ig} values for the fan drives. Similar to the constant torque load drive, the active control methods improve the line current quality and they show better performance at high modulation index.

Table 6.7 The simulation data obtained from the actively stabilized low C_{dc} motor drive with dc link inductor under fan load operating at $M_i=0.83$.

Method	Power (kW)	DC bus voltage ripple pp (V-%)	PF	THD_{ig} (%)	Torque ripple pp (N.m-%)
Without disturbance rejection	2.2	215 – 42 %	0.811	71.7	0.77 – 6.7 %
With disturbance rejection		261 – 51 %	0.752	87.2	0.23 – 2.0 %
Method 1		123 – 24 %	0.923	41.2	0.57 – 5.0 %
Method 2		107 – 21 %	0.932	38.6	0.6 – 5.0 %
Method 3		107 – 21 %	0.917	43.1	2.5 – 22.0 %
Without disturbance rejection	37.0	137 – 26.8 %	0.890	51.1	7.0 – 3.9 %
With disturbance rejection		211 – 41.3 %	0.732	92.6	1.5 – 0.8 %
Method 1		100 – 19.6 %	0.928	39.6	7.5 – 4.2 %
Method 2		100 – 19.6 %	0.937	36.8	9.0 – 5.1 %
Method 3		100 – 19.6 %	0.910	45.3	34.0 – 19.2 %

Table 6.8 The simulation data obtained from the actively stabilized low C_{dc} motor drive with dc link inductor under fan load operating at $M_i=0.46$.

Method	Power (kW)	DC bus voltage ripple pp (V-%)	PF	THD _{ig} (%)	Torque ripple pp (N.m-%)
Without disturbance rejection	2.2	100 – 20 %	0.842	63.0	0.41 – 7.1 %
With disturbance rejection		100 – 20 %	0.832	66.0	0.24 – 4.2 %
Method 1		100 – 20 %	0.853	60.3	0.46 – 7.9 %
Method 2		100 – 20 %	0.855	59.5	0.48 – 8.3 %
Method 3		90 – 18 %	0.812	70.0	2.15 – 37.3 %
<hr/>					
Without disturbance rejection	37.0	115 – 22.5 %	0.776	80.0	6.0 – 7.2 %
With disturbance rejection		119 – 23.3 %	0.737	90.3	3.4 – 4.1 %
Method 1		102 – 19.9 %	0.829	66.1	6.67 – 8.1 %
Method 2		103 – 20.2 %	0.800	72.4	7.7 – 9.3 %
Method 3		88 – 17.2 %	0.810	70.5	21.0 – 25.5 %

As the active control method performances for all operating conditions are considered, it can be said that all methods stabilize the bus voltage variations at nearly equal performance, resulting in voltage ripples close in amplitudes.

A qualitative comparison can be made also in terms of implementation of the active control methods. The current mode control is applied at twice switching frequency and it is difficult to tune compared to voltage mode control methods. It requires high bandwidth current controller and if the dc link resonant frequency is high, as in the simulations, it

forces the designer to select a higher switching frequency to increase available bandwidth. Voltage mode control methods offer easier implementation as they modify the voltage of the PWM modulator and do not need high bandwidth controllers.

6.4 Comparison of Conventional Motor Drives and Low C_{dc} Motor Drives

The conventional drives and low C_{dc} motor drives offer different performances in terms of dc bus voltage quality, input power quality, and motor motion quality. The tables constructed for various operation points are evaluated and the two types of drives are compared quantitatively.

6.4.1 Comparison In Terms of DC Bus Voltage Quality and Stability

The first performance measure is the dc bus voltage quality and stability. The high stiffness of the dc bus voltage obtained with large capacitor conventional drives is examined via the simulations. The results show that, whether the drive is operated by disturbance rejection or without disturbance rejection, the bus voltage maintains its low ripple and stable operation. The low voltage ripple offers a high quality dc source for the voltage source inverter which in turn creates a high quality inverter output voltage waveform. The low C_{dc} motor drives on the other hand carry the characteristic six pulse ideal diode rectifier output voltage waveform when operation is stable. This resulted in visible 300 Hz torque ripple if dc bus disturbance rejection is not applied. If the dc bus disturbance rejection is applied to the low C_{dc} motor drives, the dc bus voltage faces high frequency resonant oscillations, unlike the conventional motor drives.

6.4.2 Comparison In Terms of Input Power Quality

Another performance criterion is the input power quality of conventional motor drives and low C_{dc} motor drives. The conventional drive with large capacitor must be equipped with ac and dc side inductor filters to decrease the THD_{ig} . With 4 % ac and dc side inductor filters, they results in 29.4 % - 32.4 % THD_{ig} for the 2.2 kW and 37 kW drives at high M_i operation in the simulations. The input power factor of the drives is nearly 0.94-0.95. When the drive is used with lower M_i values, the THD_{ig} levels are increased to around 40 % and PF to around 0.9.

Considering the low C_{dc} motor drives, the obtained THD_{ig} levels are around 40 % for high M_i operation, if no disturbance rejection is applied. The THD_{ig} values increase as M_i is decreased. The most important point to stress for these results is that they are obtained without use of any ac or dc side inductor filters unlike the conventional large capacitor drive. These figures can be considered as satisfactory considering the fact that no filter inductors are used in the low C_{dc} motor drives. The PF values obtained for low C_{dc} motor drives are around 0.92 - 0.94, which are also very close to conventional drive performance. When the modulation index is decreased, the THD_{ig} levels increase and PF decreases as expected.

6.4.3 Comparison In Terms of Motor Motion Quality

The simulation results show that, the motor motion quality is highly affected from the bus voltage waveform. So, the primary motion quality difference between the conventional motor drive and low C_{dc} motor drive arises from the dc bus voltage ripple characteristics.

The motion quality of the drive circuits are analyzed by investigation of motor torque ripple. Very broadly, the conventional drive offers 0.3 N.m ripple for 13 N.m load torque (2.3 %) and 3 N.m for 230 N.m load torque (1.5 %) for 2.2 kW and 37 kW drives respectively for operation at high M_i .

The low C_{dc} motor drives on the other hand offers low torque ripple when dc bus disturbance rejection is applied. Approximately 2 % torque ripple is obtained with dc bus disturbance rejection applied and 4 % without dc bus disturbance rejection. So, it can be deduced that, the torque ripple is highly sensed in low C_{dc} motor drives if disturbance rejection is not applied. Despite, the importance of torque ripple may change depending on the application type. For instance, a fan drive may not be affected from torque ripple significantly unless its cooling performance is considerably degraded.

CHAPTER 7

CONCLUSION AND FUTURE WORK

In this thesis, the performance of the conventional ac motor drives utilizing front end diode rectifiers with high capacitance electrolytic capacitor and the ones utilizing low capacitance film capacitor are investigated. The performances of the two structures are evaluated at various load levels and types. The active control methods to improve the stability in low C_{dc} small capacitor drives are analyzed and their performances are compared both in terms of operation performance and implementation easiness. The conventional drive and low C_{dc} motor drives are compared in terms of dc bus voltage stability, input power quality, and motor motion performance both quantitatively and qualitatively.

The drives are designed according to the full load ratings (2.2 kW and 37 kW) of the motors. However in the simulations, staying in the inverter linear operation region, the motors deliver less than full load power for both conventional and low C_{dc} motor drives as explained in Chapter 4 and Chapter 5.

As deduced from the results of simulations, conventional drives offer stiff dc bus voltage with high stability and can be used safely for all load types including constant power, constant torque, and variable torque loads, as expected. The conventional drives are equipped with inductor filters at both ac and dc side to decrease the grid current THD (THD_{ig}) to an acceptable level.

The stability of the low C_{dc} motor drives is reduced due to increased resonant frequency of the dc link and the instability shows itself as amplification of the resonant voltage component of the dc link. To investigate this problem, the equivalent rectifier-inverter model is simulated by using voltage sources as inputs with amplitudes and frequencies equal to that of the ideal three phase diode rectifier voltage ripple harmonics. By this

method, the resonant voltage component amplification on dc bus voltage is investigated for various dc bus capacitance and inductance values resulting in different resonant frequencies. From the simulations, it is deduced that the optimum resonant frequency causing minimum resonant voltage amplification is approximately 8-10 times that of dc bus ripple frequency ($6f_e$). This is due to the fact that the high order ripple voltage harmonics around high resonant frequency which are already low in magnitude do not cause significant resonant voltage amplification. If the resonant frequency is selected low and close to $6f_e$, the ripple voltage harmonics around the resonant frequency which are higher in amplitude compared to higher order ones excites the resonance causing high voltage amplification. This situation is pictured by curves showing variation of the resonant voltage amplification, equivalent circuit input impedance, and input current magnitude with the frequency in Figure 5.2, Figure 5.3, Figure 5.4, and Figure 5.5.

To investigate the stability of the dc link of the drives, two types of rectifier circuits; with and without dc link inductor are designed and simulated. The circuits without dc link inductor whose resonant frequencies are 8-10 times that of $6f_e$ ripple frequency offers stable operation. On the other hand, the circuits with dc link inductor whose inductance is nearly 8-10 times of ac line inductance resulting in a resonant frequency of 4-5 times of $6f_e$ ripple frequency become unstable as expected.

The dependence of stability on load power level is another point of investigation in the thesis. As the voltage circles in Figure 6.1 for the 2.2 kW motor drive obtained for constant torque load operation and Figure 6.2 for 37 kW drive are compared, it is seen that the level of bus resonant voltage amplification is slightly lower on the 37 kW drive. This is an indication that instability increase as the load power decreases.

To overcome the instability, some of the voltage and current mode based active stabilization methods found in the literature are reviewed and applied to the circuits. The methods improve the dc bus voltage stabilities of the drives and each shows different performance in terms of dc bus voltage quality, input power quality, and motor motion quality. Method 1 improves the stability by modifying the disturbance rejection algorithm. This method offers minimum torque ripple among the other active stabilization methods. Method 3 generates the highest torque ripple which can be explained by the high parameter sensitivity of the algorithm due to high number of calculations. In terms of bus voltage

stabilization performance, Method 2 offers highest damping as seen in Figure 6.1 and Figure 6.2 where the voltage reference and limit circles have minimum interference.

The easiness in implementation of stabilization methods is different from each other. Current controlled method requires high bandwidth current controller, as expected, at least at the dc link resonant frequency to suppress the resonant amplification by modifying the current reference of the motor current regulator. This in turn makes it necessary to increase the switching frequency to achieve the desired regulator bandwidth. Voltage mode methods, on the other hand, are applied by modifying the voltage references for the PWM modulator and do not impose any bandwidth criteria.

The simulation results show that the low C_{dc} motor drives can offer an input power quality performance close to the conventional drives equipped with large inductor filters, by introducing low THD_{ig} and high PF, even without inductor filters. These types of drives, however; are not recommended to be used with constant power loads due to instability caused by negative impedance effect.

As a future work, the study of motor drives with low C_{dc} dc bus capacitor can be extended to the investigation of the performance in inverter overmodulation region. Due to overmodulation, the motor phase currents are expected to carry low order harmonics and this may in turn impose low frequency voltage ripple to the dc link. The added voltage ripple components may degrade the stability of the bus voltage when they are added to the ripple voltage caused by the diode rectifier.

Table 7.1 summarizes all results obtained throughout the study of conventional and low C_{dc} motor drives and establishes a qualitative comparison.

Table 7.1 Qualitative comparison of conventional motor drives and low C_{dc} motor drives.

Method and motor drive type	THD_{ig}	Torque ripple	Implementation	Current regulator bandwidth	Load dependence	Parameter dependence	Inductor filter requirement	Cost	Size
Conventional drive with dc bus disturbance rejection	Low	Low	Easy	Can be lower	Low	-	Yes	High	High
Conventional drive without dc bus disturbance rejection	Low	Low	Easy	Can be lower	Low	-	Yes	High	High
Low C_{dc} drive with disturbance rejection	High	Low	Easy	Can be lower	High	Low	No	Low	Low
Low C_{dc} drive without disturbance rejection	Low	High	Easy	Can be lower	High	Low	No	Low	Low
Low C_{dc} drive with Method 1	Low	Low	Easy	Can be lower	High	Low	No	Low	Low
Low C_{dc} drive with Method 2	Low	Low	Easy	Can be lower	High	Low	No	Low	Low
Low C_{dc} drive with Method 3	Low	High	Moderate	Must be high	High	High	No	Low	Low

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