A NOVEL METHOD FOR 2-18 GHz SWITCHED MULTIPLEXER DESIGN

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

BÜLENT ALICIOĞLU

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF DOCTOR OF PHILOSOPHY
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2012

Approval of the thesis:

A NOVEL METHOD FOR 2-18 GHz SWITCHED MULTIPLEXER DESIGN

submitted by **BÜLENT ALICIOĞLU** in partial fulfillment of the requirements for the degree of **Doctor of Philosophy in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen   _____
Dean, Graduate School of **Natural and Applied Sciences**

Prof. Dr. İsmet Erkmen   _____
Head of Department, **Electrical and Electronics Engineering**

Prof. Dr. Nevzat Yıldırım   _____
Supervisor, **Electrical and Electronics Engineering Dept., METU**

Examining Committee Members:

Prof. Dr. Canan Toker   _____
Electrical and Electronics Engineering Dept., METU

Prof. Dr. Nevzat Yıldırım   _____
Electrical and Electronics Engineering Dept., METU

Prof Dr. Adnan Köksal   _____
Electrical and Electronics Engineering Dept., Hacettepe University

Prof. Dr. Birsen Saka   _____
Electrical and Electronics Engineering Dept., Hacettepe University

Assoc.Prof.Dr. Şimşek Demir   _____
Electrical and Electronics Engineering Dept., METU

Date: 14.09.201

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name   : Bülent ALICIOĞLU

Signature   :

ABSTRACT

A NOVEL METHOD FOR 2-18 GHz SWITCHED MULTIPLEXER DESIGN

Alıcıoğlu, Bülent

Ph.D., Department of Electrical and Electronics Engineering

Supervisor: Prof. Dr. Nevzat Yıldırım

September 2012, 163 pages

A novel topology is developed and used to design a switched multiplexer. In the new topology there are two noncontiguous switched multiplexer modules containing the channels 2-4 GHz, 6-8 GHz, 10-12 GHz and 14-16 GHz named as odd channels and 4-6 GHz, 8-10 GHz, 12-14 GHz and 16-18 GHz, named as even channels to improve isolation between adjacent channels. The input signal is split at input into the two multiplexer and the outputs of the multiplexers are combined by 2-18 GHz power dividers. The input and output multiplexers are combined through switch + Low Noise Amplifier + attenuator blocks which are also used for amplitude equalization. The input/output multiplexers are designed using a novel technique that transforms a contiguous manifold multiplexer into non-contiguous multiplexers with 2 GHz bandwidth to form guard bands between channels to improve isolation. The HP outputs of the channels are split by LP-HP diplexers with corner frequencies at the centers of the channels. Then only the LP outputs of these diplexers are fed to the output to form a non-contiguous multiplexers. The HP outputs of LP-HP diplexers are terminated in 50 ohms. The incorporation of LP-HP diplexer to form noncontiguous channels is a novel approach which avoids interaction of channels. The diplexers forming the switched multiplexer are designed using a novel approach which incorporate open circuited parallel coupled line as diplexing element. This

structure acts as an integral part of the diplexer and contributes its performance. The LP-HP diplexers are designed and fabricated successfully in suspended stripline. The implemented LP-HP diplexers are then combined to form the even and odd channel multiplexers. The measured results of the individual diplexers are then combined with attenuator+Amplifier blocks to form the circuit model of the targeted switched multiplexer yielding successful performance. Thus, the design is complete and ready for the realization of a switched multiplexer.

Keywords : Stripline,Suspended Stripline, Diplexer, Multiplexer, Switched multiplexer.

ÖZ

2-18 GHz ANAHTARLANABİLİR ÇOĞULLAYICI TASARIMI İÇİN YENİ BİR YÖNTEM

Alıcıoğlu, Bülent

Doktora, Elektrik ve Elektronik Mühendisliği Bölümü

Tez Yöneticisi: Prof. Dr. Nevzat Yıldırım

Eylül 2012, 163 sayfa

Bu tez çalışmasında, 2-18 GHz aralığında çalışan eşit band genişlikli 8 kanaldan oluşan askılı şerit hatlı anahtarlamalı çoğullayıcı, tasarımı özgün bir yöntem kullanılarak tasarlanmıştır. Özgün topolojide iki ayrı süreksiz anahtarlamalı çoğullayıcı ki biri tanesi tek kanallar olarak adlandırılan,2-4 GHz, 6-8 GHz, 10-12 GHz ve 14-16 GHz kanallarını içermektedir Diğeri ise çift kanallar olarak adlandırılan. 4-6 GHz, 8-10 GHz, 12-14 GHz ve 16-18 GHz kanallarını içermektedir Gelen işaret 2-18 GHz güç bölücü ile her iki çoğullayıcıya da verilmekte ve bu çoğullayıcıların çıkışları 2-18 güç bölücü ile toplanmaktadır. Her iki anahtarlamalı çoğullayıcıdaki giriş ve çıkış çoğullayıcıları, genlik dengeleyici olarak ta kullanılan, yükselteç+zayıflatıcı bloğuyla aralarına bir anahtar konmak suretiyle birleştirilmektedir. Giriş ve çıkış çoğullayıcıları, özgün bir yöntem ile tasarlanmaktadır. Bu yöntemde sürekli bir manifold süreksiz bir manifolda dönüştürülerek 2 GHz band genişliğinde kanallar elde edilmekte ve kanallar arasına koruma bandları yerleştirilmektedir. Bu hem yapının anahtarlanabilir olmasını sağlamakta hem de kanallar arası yalıtımı artırmaktadır. Sürekli çoğullayıcıdaki yüksek geçiren kanalların çıkışına ilgili kanalın merkez frekansında ikileyiciler

yerleştirilerek , yerleştirilen ikileyicinin alçak geçiren kanalı çıkışa bağlanarak tek ve çift kanalları içeren süreksiz anahtarlamalı çoğullayıcılar elde edilmektedir. İkileyicilere ait yüksek geçiren kanal 50 ohm ile sonlandırılmaktadır. Bu özgün yöntemin en önemli getirisi kanallar arası etkileşimi en az seviyeye indirmesidir. Hem manifold hem de bunların sonuna eklenen ikileyiciler özgün bir yöntem ile tasarlanmıştır. Bu yöntemde ikileyicide, kanal ayracı olarak açık devre edilmiş bağlaşık hat kullanılmıştır. Bu yapı ikileyicinin bir parçası gibi davranmakta ve performansına katkıda bulunmaktadır. Bu tip ikileyiciler asklı şerit hat kullanılarak bu tezde başarıyla gerçeklenmiştir. Gerçeklenen ikileyiciler daha sonra birleştirilerek çoğullayıcı ve anahtarlamalı çoğullayıcı blokları oluşturulmuştur. Elde edilen ölçüm sonuçları kullanılarak 2-18 GHz mikrodalga anahtarlamalı çoğullayıcının ölçüm sonuçları kullanılarak gerçekçi bir devre modeli oluşturulmuştur. Bu model kullanılarak elde edilen sonuçlara bakıldığında tasarımın tamamlandığı ve üretime hazır olduğu sonucuna varılmıştır.

Anahtar Kelimeler : Şerit Hat, Askılı Şerit Hat, İkileyici, Çoğullayıcı, Anahtarlamalı çoğullayıcı.

To my beloved family

ACKNOWLEDGEMENTS

TABLE OF CONTENTS

LIST OF FIGURES

FIGURES

LIST OF ABBREVIATIONS

ADS   : Advanced Design System

ATC   : American Technical Ceramics

BPF   : Bandpass Filter

CST   : Computer Simulation Technology

BW   : Bandwidth

CPW   : Coplanar Waveguide

DC   : Direct Current

EW   : Electronic Warfare

EM   : Electromagnetic

HPF   : Highpass Filter

IL   : Insertion Loss

LPF   : Lowpass Filter

MMIC   : Monolithic Microwave Integrated Circuit

OCPCL   : Open Circuited Parallel Coupled Line

PIN   : Positive-Intrinsic-Negative

PCB   : Printed Circuit Board

PCL   : Parallel Coupled Line

OCPCL   : Open Circuited Parallel Coupled Line

RF   : Radio Frequency

RL   : Return Loss

SCPCL   : Short Circuited Parallel Coupled Lie

SPDT   : Single Pole Double Throw

TL   : Transmission Line

VSWR   : Voltage Standing Wave Ratio

CHAPTER 1

INTRODUCTION

1.1 Scope and Objective

For electronic warfare systems operating in microwave frequency spectrum, whose signal density is very high and increasing day by day, cancellation of unwanted signals such as interference, jamming etc. and observing desired signals in a narrower bandwidth compatible with instantaneous bandwidth of the system, is a must. Constructing such components in a compact and easily realizable form is an essential issue in the electronic warfare industry. Multiplexers are essential components of wideband communication and electronic warfare systems. They are used for signal classification purposes by selecting the frequency band of interest from the microwave frequency spectrum and filtering out the rest of the frequencies.

Switched multiplexers are being used for a long time in modern sophisticated ECM (Electronic Counter Measure) and ESM (Electronic Support Measure) systems. The most typical application of switched multiplexer is its use preceding an IFM (Instantaneous Frequency Measurement) receiver, providing adaptive filtering in the RF section and reducing the incident spectrum in front of the IFM receiver. Switched multiplexers are therefore essential building blocks of adaptive wideband ESM receivers. They allow a rapid and intelligent modification of the system frequency characteristics to match the signal environment.

A switched multiplexer is a two port adaptive filtering network whose filtering characteristics may be electronically controlled to suit the operational environment. They split the input frequency band into a number of channels each of which may be independently switched into a bandpass or all stop state. For a device comprising 'n' channels, it is therefore possible to have '2^n' switched states.

The main target of this thesis is design and implementation of an eight channel switched multiplexer operating between 2.0-18.0 GHz, with each channel having 2 GHz bandwidth. For this purpose a survey and critical review of the available techniques are made and a novel approach is developed that led to a topology which is simpler to implement with improved properties. It is shown that parallel coupled line (PCL) three ports can be used for synthesizing diplexers with good input return loss and improved isolation between channels compared to the commonly used T-junction type diplexers. Improvements come from the fact that the parameters of three port PCL are forced to be parts of the channel filters, thus contributing to the responses of the channels while in the T-junction case the parameters of the junction are treated as response degrading factors. It is also shown that such diplexing three ports can be cascaded to form input and output manifolds for parallel or series connection of channel filters to form various types of multiplexers. By incorporating switches into the filters it is possible to form switched multiplexers. The approach enables design of contiguous wide or narrow channels, thus avoiding the necessity of formation of guard bands between channels for preventing channel interactions in different switch combinations.

1.2 CAD Tools

The design stage involves the use of several synthesis, analysis, simulation and optimization tools both in circuit theory and in electromagnetic theory levels. The synthesis of the individual diplexers were carried out in FILPRO.

FILPRO is an integrated synthesis and analysis tool developed in Electrical Engineering Department of METU, mainly for the design of amplitude filtering circuits formed by passive, lumped or distributed elements in cascade topologies.

Analysis of whole switched multiplexer were done by linear tools of ADS (Advanced Design System) form Agilent Company. This program was also used to determine the dimensions of lines, coupled lines which were essential to prepared the layout.

Electromagnetic effects such as parasitics, inter resonator coupling were analyzed in SONNET, the electromagnetic analysis software. SONNET performed analysis of all planar structures such as filters, power divider and diplexers. It solved the current distribution on the metal using the method of moments. Three dimensional interconnects, such as coaxial to suspended transition and the final layout diplexers and manifolds in metal housing, were simulated in CST. CST is capable for using different frequency and time domain solvers.

1.3 Organization Of the Thesis

In chapter 2, serves a preface to basic multiplexer and switched multiplexer concepts. Basic multiplexer types are introduced, then some theoretical information about design of diplexers, which is a building block in multiplexers, are given. Key concepts such as contiguous or non-contiguous multiplexers, doubly or singly terminated filters are outline in this chapter. This chapter continues with various multiplexer and switched multiplexer topologies, then at then end of the chapter proposed architecture for 2-18 GHz switched multiplexer is stated.

In chapter 3, the coupled line models are examined in order to establish an understanding of how the novel diplexer design method works. In this method instead of directly paralleling the highpass and lowpass channels (it is called t-junction diplexing throughout the thesis), the use of open circuited parallel coupled line is emphasized. For clarity examples are given in this chapter to show the superiority of open circuited parallel coupled line as a diplexing element over t-junction.

In chapter 4, diplexers with open circuited parallel coupled lines to be used in switch multiplexer are designed and realized. The realized diplexers offer a good performance exceeding the simulation results.

In chapter 5, the proposed switch multiplexer is designed step by step beginning from forming to manifolds to forming the final 2-18 GHz, 8 evenly spaced channel, switched multiplexer. the simulation results are based on the actual measurements/3-

D simulation results of each active or passive component and they seem to be promising for the realization of the final 2-18 GHz switched multiplexer.

In chapter 6 conclusions and possible future studies are presented.

CHAPTER 2

A SURVEY ON SWITCHED MULTIPLEXERS

2.1 General Information

The design stage involves the use of several synthesis, analysis, simulation and optimization tools both in circuit theory and in electromagnetic theory levels.

In order to be able to design a switched multiplexer, one should first be able to design a multiplexer, because a switched multiplexer is always a combination of two or more multiplexers in various ways. Multiplexers may be combined in several ways to form switched multiplexers, like connecting two identical multiplexers back to back, connecting an input multiplexer to a frequency shifted output multiplexer using power splitters and combiners etc. There are many problematic points in the design of multiplexers. Some of the critical ones can be summarized as follows:

- Destructive interaction of adjacent and nonadjacent channels leading to degradation in input return loss and isolation between channels.

- Problems in the interconnection of channel filters to input and output manifolds leading to degradation of input return loss and channel filter characteristics.
- Extreme element values in narrow and wide channels in different frequency ranges.

Such problems get more severe in wideband coverage and in the case of closely spaced channels. It is shown that PCL three port approach helps to ease most of such problems.

In the next section basic multiplexer types will be summarized.

2.2   Basic Multiplexer Types

Multiplexers are used to divide frequency band into sub-frequency bands by integrating a number of specially designed channel filters in special ways. A diplexer is a two channel multiplexer, a triplexer is a three channel multiplexer and so on. In Figure 2.1 some typical parallel connected diplexers are shown while in Figure 2.2 typical parallel connected multiplexer structures are shown. The duals of these circuits are named as series connected multiplexers.
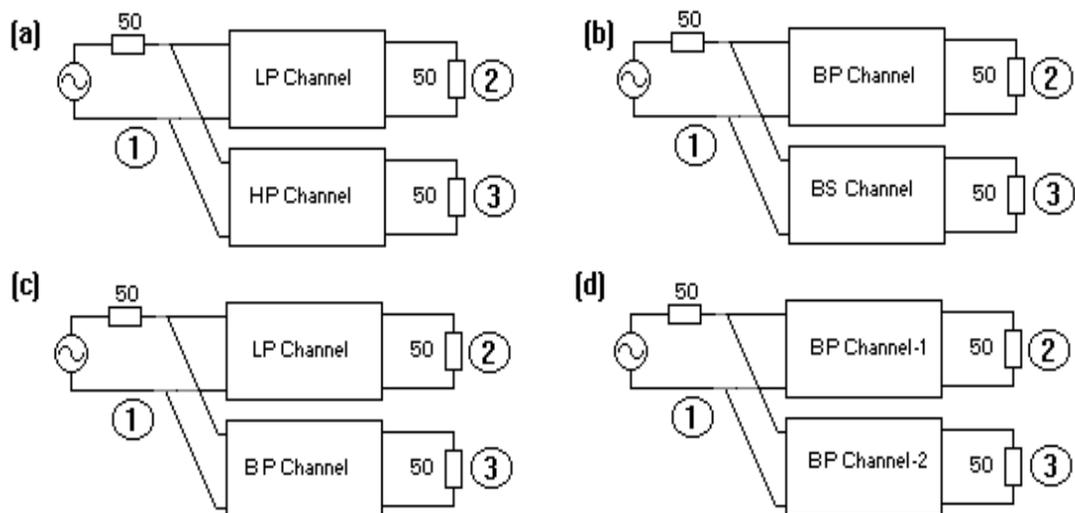
Figure 2.1 Some Parallel Connected Diplexers
(a) Lowpass-Highpass Diplexer, (b) Bandpass-Bandstop Diplexer, (c) Lowpass-Bandpass
Diplexer and (d) Bandpass-Bandpass Diplexer
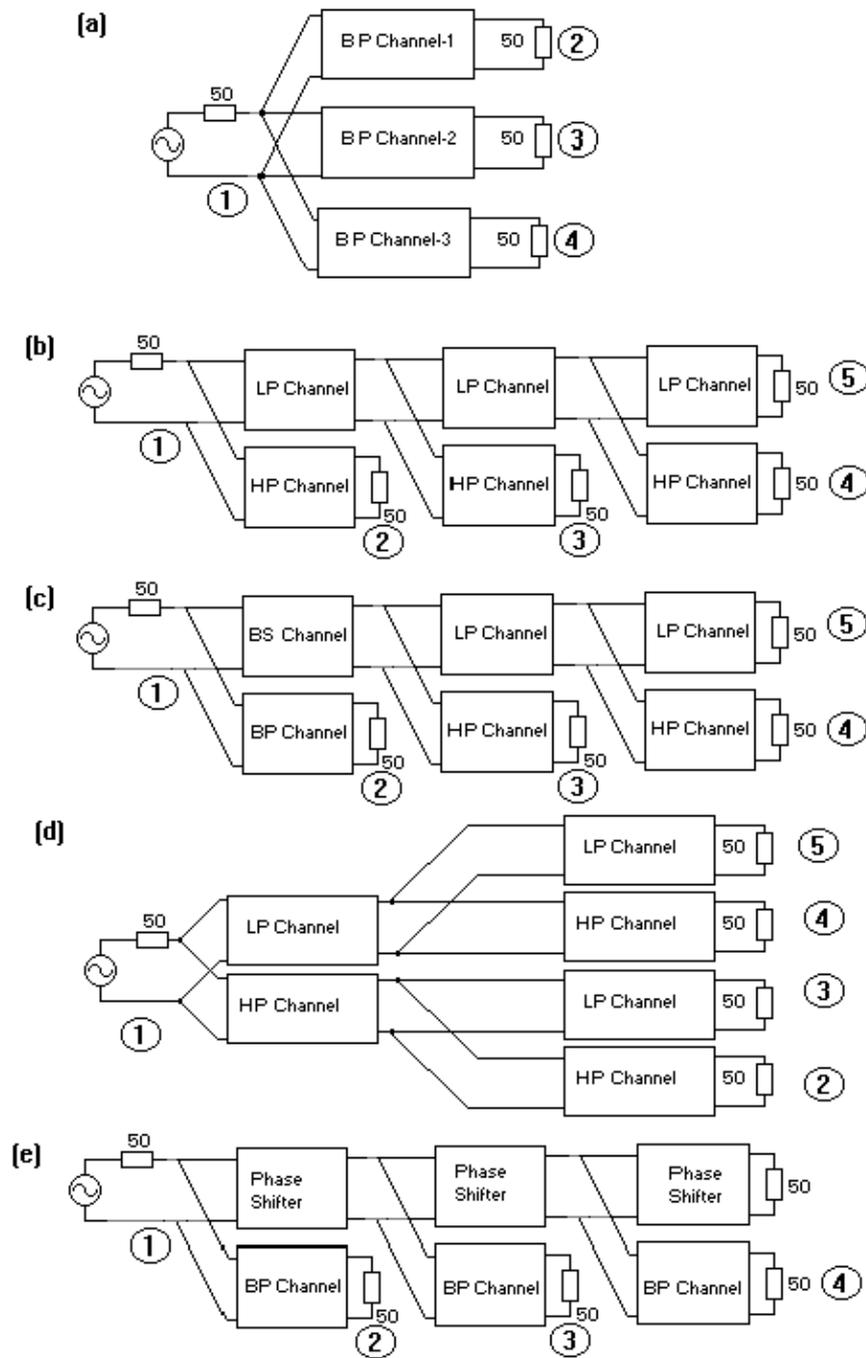
Figure 2.2 Typical Parallel Connected Multiplexer Structures
(a) Parallel Bandpass Filter Multiplexer, (b) Ladder Type Lowpass-Highpass Multiplexer, (c) Bandpass-Bandstop and Lowpass Multiplexer, (d) Tree Type Multiplexer using Lowpass-Highpass Diplexers and (e) Manifold Type Multiplexer

The topology to be used depends largely on the technology of implementation, number of channels, channel bandwidths, separation (guard bands) between channels, the overall bandwidth to be covered (channelized) by the multiplexer, input return loss and channel isolation requirements, etc. The topology in Figure 2.2.a. is suitable for narrow band multiplexers, commonly used in waveguide type multiplexers with common resonators. However it is severely limited by the number of channels. It is almost impossible to design even planar triplexers using this topology. In order to overcome this problem, in narrow band applications usually the topology in Figure 2.2.e is used. The topologies of Figure 2.2.c and d are also suitable for narrow medium bandwidth filters. For multiplexers with wide channel bandwidths and wide frequency coverage, the LP-HP ladder type topology shown in Figure 2.2.b is used, as is done in this thesis also.

In applications where a wide frequency band should be covered without any gap between channels, the adjacent channels should be contiguous, that is, they should cross-over at 3 dB. In the usual communication applications, channels should be separated by some guard bands with a specified minimum cross-over loss. Such multiplexers are termed as noncontiguous. In some applications two adjacent channels may overlap. The signals with frequencies in the overlap region are divided equally into the two channels.

Since a multiplexer is a lossless multiport network, all the power available from the source at the input (Port-1) is supposed to be delivered to only one of the output ports depending on frequency, without any reflection. That is, input impedance of a multiplexer must be matched to the source at all frequencies within the passbands of all channels.

The theory for **exact synthesis** of multiplexers is still unresolved [21], [35]. **Exact synthesis** techniques exist only for some simple **lowpass-highpass diplexers** [31], [32], [37], [41], [42]. A survey of literature shows that the design techniques of multiplexers are independent of **exact filter synthesis** techniques. Most of the successful design techniques depend on modifications of independently synthesized channel filters brought together in the topologies shown in Figures 2.1 or 2.2 to work

as multiplexers. As complexity of multiplexing structures increase, circuit theory alone can't cope with design challenges. Circuit theory should work together with electromagnetic field theory [33], [36], supported by powerful optimization techniques [27], [28].

The theory of multiplexers employing **singly terminated filters** [1]-[8] are based on the theory of **complementary pair** of filters. A parallel filter pair with non overlapping passbands must have input admittances Y_1 and Y_2 such that $Y_1+Y_2=1$ in the passbands of the channels. Similarly, a series connected filter pair input impedances must satisfy the relation $Z_1+Z_2=1$ in the passbands of the channels. That is, the reactive parts of channel input impedances are of opposite sign so they cancel to yield resistive input impedance matched to the source resistance over both channels. Cancellation is exact at the cross-over frequency for maximally flat channel filters [1]-[6] therefore they take the name **complementary pairs**. For Chebyshev or elliptic channel filters, this effect is still observed but it is approximate, hence they take the name **pseudo-complementary** pairs.

In general the desired channel filters can also be synthesized independently as singly terminated or doubly terminated filters and then combined to form of LP-HP, LP-BP-HP or BP-BP, BP-BS, etc type diplexers and multiplexers, followed by modifications and tuning-optimization to get the targeted response. These filters can also be designed either by first forming a LP prototype and then mapping into LP, HP, BP or BS form or the channel filters can be synthesized directly as LP, HP, BP or BS filters.

In this thesis the software Filpro is used to design both doubly terminated and singly terminated channel filters and LP-HP diplexers. Multiplexer designs are tested by using both singly terminated and doubly terminated channel filters to get some insight on the properties of the selected topologies. It is seen that both approaches have some advantages and disadvantages depending on constraints of the application. However singly terminated designs may contain physically unrealizable element values which needs optimization to get realizable values. Doubly terminated channel

9

filters are easier to design and usually does not to contain unrealizable element values, but the first element must be deleted and the whole circuit must be optimized. In designing LP-HP diplexers, first singly terminated designs are tested to get an idea if the requirements can be met quickly or not because, the two channel filters of a LP-HP diplexer are synthesized in exact manner simultaneously.Then, in the succeeding stages in forming the multiplexer, further information can be generated about the problematic parts of the whole circuit and the designs can be repeated using either singly or doubly terminated approaches.

Usually singly terminated adjacent channel filters form better complements. When doubly terminated filters are used as channel filters their first element on the diplexing inputs are deleted (foreshortening) because if they are used without foreshortening they load each other heavily leading to gross degradation in response. One disadvantage of doubly terminated designs is that foreshortening may lead to degree reduction compared to singly terminated designs to satisfy the same requirements. Theoretically design of the multiplexer as a whole should be possible because, if properly designed, the transfer characteristics of each channel may get contributions of other channels to increase their skirt slopes. That is, if there are M channels and if all channel filters are of degree N, then the transfer function of each path from the input of multiplexer to the output of any channel will have a degree of MxN. This fact may be exploited for improving responses of channels. However exact analytical handling and synthesis of such circuits is a difficult task. Therefore usually special approximate design procedures for special structures a number of solutions. Therefore optimization trials starting with singly or doubly terminated designs may converge to different circuits. However once a topology is selected, after getting insight, experiments indicated that both approaches converge to the same circuit if optimization is made in a controlled and guided manner sa defined in [51].

All these comments are also applicable to all-stub commensurate length distributed element filters. For distributed element filters involving contributing Unit Elements we have the following extra property: A commensurate line highpass filter with N contributing unit elements and M transmission zeros at f=0 has exact lowpass

complements with N+M transmission zeros at f=∞. Similarly, a lowpass filter with N contributing unit elements and M transmission zeros at f=∞ have highpass complements with N+M transmission zeros at f=0 [5], [6].

In general, the synthesized filters may need conversion into the targeted realizable forms by inserting redundant unit elements and using Kuroda transformations. Redundant unit element can be inserted only from to the load side because insertion of any element on source side will degrade the complementary nature of the channel filters. If realizable element values can be obtained, a better way may be direct synthesis of channel filters with contributing unit elements. Both approaches may have difficulties in realization but usually direct synthesis with contributing unit elements give quicker results.

The realization problems due to extreme element values or due to resulting topology can be solved by using circuit transformations. In general all multiplexers require some professional optimization. However, many useful multiplexers can be designed through manual optimization. In fact, especially in multiplexers with high number of channels, direct application of general optimization techniques is usually not practical or feasible. It is the common experience that manual optimization while observing the response is a better way at the initial stages of design, giving hints on the directions to move and on the relative effects of various parameters on response and on possible solution patterns. When the targeted response is approached then automatic optimization tools can be used for fine adjustment of the response and trimming the element values.

Since a very wide frequency coverage with wide channel bandwidths is targeted, in this thesis, ladder type LP-HP type multiplexer topology is selected for the switched multiplexer. In the next section some possible alternative structures and their problematic points are discussed, ending in the final topology to be implemented as the target of this thesis.

2.3 Simple Ladder Type HP-LP Switched Multiplexers (SW_MUX)

A simple switched multiplexer can be formed by connecting two HP-LP ladder multiplexers back to back style as shown in Figure 2.3. Note that the designed multiplexer is used both in the input and output stage so all diplexers are used twice. Since the diplexers used are of LP-HP type, they are contiguous. That is the loss at each cross-over frequency is 3 dB. When they are connected back to back the cross-over losses will be 6 dB. When all channels in SW_MUX are combined, there will be notches of magnitude 3 dB at cross-over frequencies. This is the main disadvantage of contiguous switched multiplexers. This problem can be resolved only if the channels are made noncontiguous, as will be described in some other switched multiplexer types.
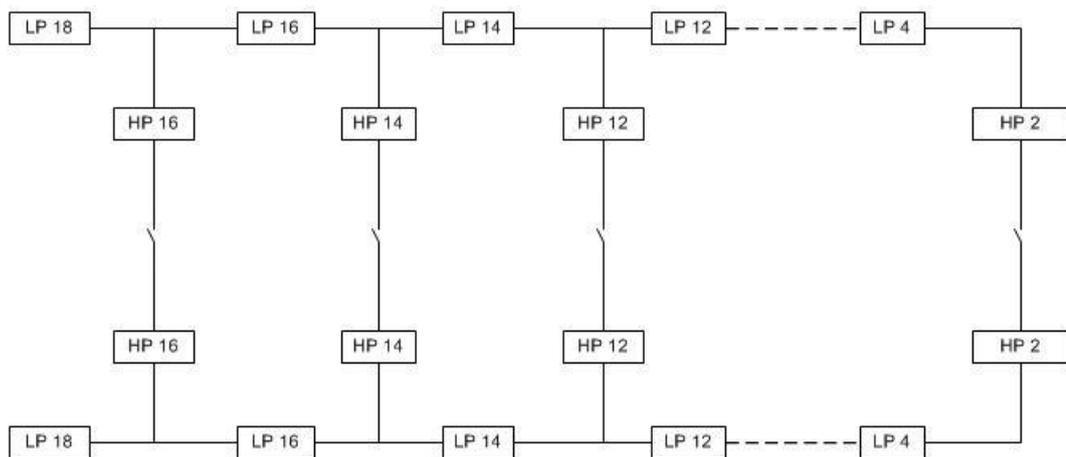
Figure 2. 3 A Simple SW_MUX Based on LP-HP Diplexers

2.4 Ladder Type HP-LP Switched Multiplexers with Power Dividers

Another way to implement the same switched multiplexer can the through the use of power dividers repeatedly connecting the output of the diplexers until a single output is reached. This topology is shown in Figure 2.4. It is seen that there is an extra 6 dB cross-over loss if SW_MUX has 4 channels, 9 dB loss if SW_MUX has 8 channel. That is the loss will increase by 3 dB, each time the number of channels is doubled.

This loss can be limited to 6 dB for any number of channels by the SW_MUX topology shown in Figure 2.5 described in [49]. In this topology SW_MUX consists of an input multiplexer and an output multiplexer. Both multiplexers are 4 channel multiplexers, each channel having 4 GHz bandwidth. The output multiplexer is a 2 GHz shifted version of the input multiplexer, so when these two multiplexers are connected using a power divider/switch network as shown in Figure 2.5, an eight channel SW_MUX with each channel having 2 GHz bandwidth is obtained.
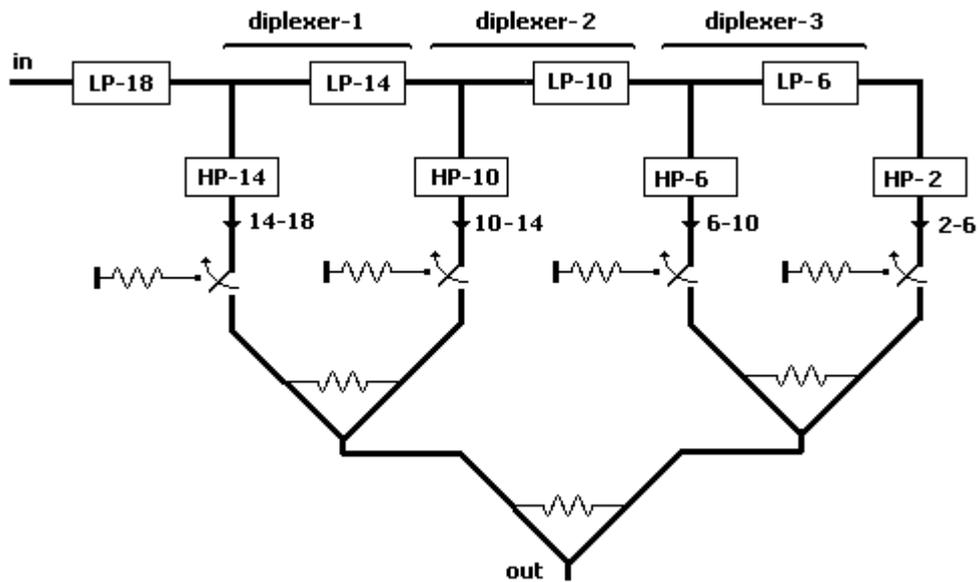
Figure 2. 4 A Switchable LP-HP Multiplexer Using Power Dividers
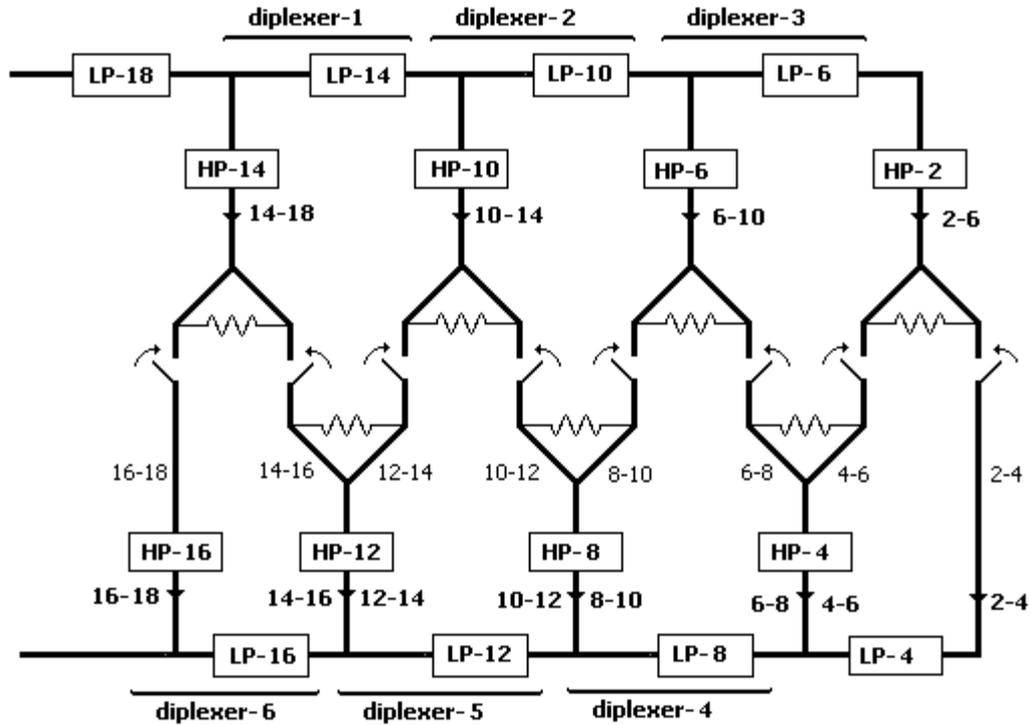
Figure 2. 5 An 8 Channel 2-18GHz SW_MUX

Although it is theoretically correct to use singly terminated filters in the design, doubly terminated filters with finite transmission zeros and contributing unit elements, providing highly selective channels can also be used in the construction of HP-LP ladder type multiplexers.

2.5 Manifold Type Stripline Multiplexers With Tee-Junctions

When the number of channels to be paralleled increases physically it may become difficult to connect them at a single junction. In stripline-like structures channels can be placed along a manifold as shown in Figure 2.6.a. In this structure the channel filters are interconnected through Tee-junctions. The channels are thus separated physically by some length of lines (or waveguides, or phase shifters as in Figure 2.2.e) which may also function as parts of immitance compensation elements to reduce interaction between channels. In Figure 2.6.b the channel filters are shown as shunt connected External One-Port elements for simulation on the software Filpro

14

which is used for synthesis, design and optimization of the channel filters and the whole multiplexer.
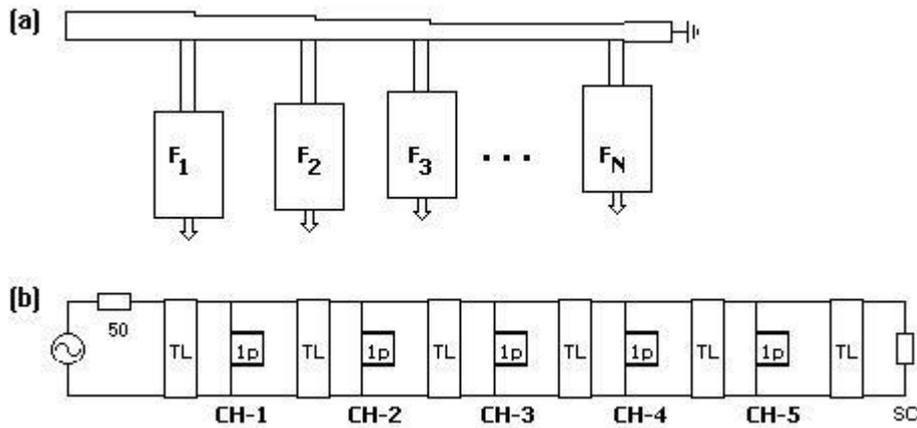
Figure 2. 6 A Manifold (Extended Junction) Stripline Multiplexer

It is important to realize that direct connection of the channel filters into the manifold transmission line (forming T-type junctions) may cause serious degradations in multiplexer performance, because each channel filter will load the manifold, thus the other channel filters. The level of degradation increases as the number of channel filters increase, so some alterations should be made in channel filters before integration. One approach to solve this problem is developed by Mobbs [4], known as hybrid coupled manifold multiplexer.

2.6 Hybrid Coupled Manifold Multiplexer

When number of channels is large, channel filters involving directional couplers (3 dB hybrids) are advantageous to use when integration into a multiplexer is considered [4]. A hybrid coupled manifold multiplexer is shown in Figure 2.7. Each channel is made up of two 3 dB hybrids and two identical filters. Coupler-filter-coupler combinations extract the signals within their passbands from the manifold and direct them to one output port of the second coupler forming one channel of the multiplexer. Modularity of multiplexer is clear. New channels may be added or some channels can be switched off without effecting the other channels, if all channel if all

15

channel bandwidths are within the 3 dB coupling and isolation bandwidths of the couplers.
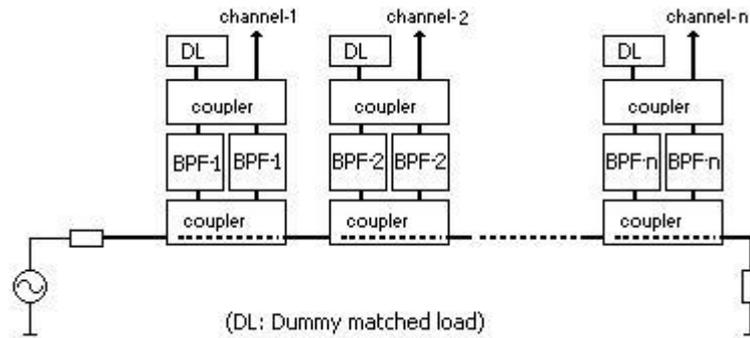
Figure 2. 7 Hybrid Coupled Manifold Multiplexer

In order to clarify operation of the channels, the basics of directional couplers on a 3 dB branchline directional coupler with two branches should be reviewed. The number of branches may be increased depending on bandwidth requirements and other constraints or one may use other types of directional couplers, like TEM mode parallel coupled line couplers or lumped element couplers .

2.2.1 3 dB Impedance Transforming Branchline Couplers With Ideal Inverters

A schematic drawing of a symmetric, impedance transforming two branch coupler is shown in Figure 2.8. The convention for port numbering and signals of these ports when input is applied to port-1 is as follows:

Port-1: Input signal port with termination resistance R_1.

Port-2: Transmitted signal port with termination resistance R_2.

Port-3: Coupled signal port with termination resistance R_2.

Port-4: Isolated port with termination resistance R_1.

16
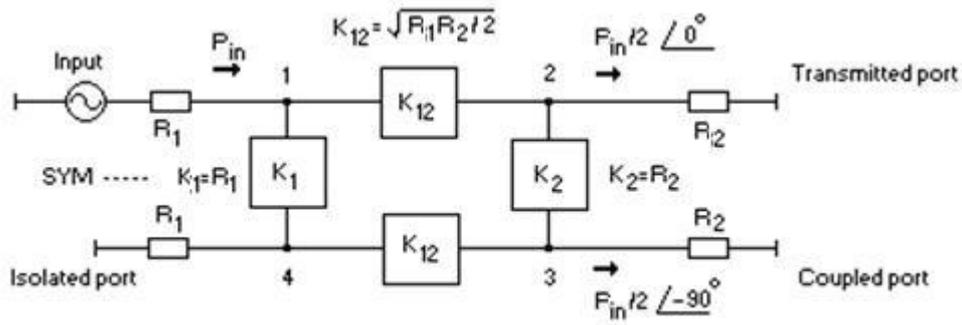
Figure 2. 8 Schematics of a 3 dB Impedance Transforming Branchline Coupler with Different Input-Output Terminations

If the phase of transmitted port signal (Port-2) is taken as reference (0 degree), then the phase of coupled port signal is -90 degrees (Port-3). The arms are formed by ideal inverters. In order that this device work as a 3 dB coupler, the inverter impedances should satisfy the following relations:

Branch -1 inverter impedance: $K_1 = R_1$

Branch -2 inverter impedance: $K_2 = R_2$

Main arm inverter impedances: $K_{12} = (R_1 * R_2 / 2)^{1/2}$

- In multiplexer applications the filters will appear as loads R_2 at port-2 and port-3 of the first coupler as shown in Figure 2.9.

- If the incoming signal frequency is within the passband of a channel then this signal will be extracted from the main arm and split into two parts and directed to port-2 and port-3 of the first coupler with equal amplitudes and 90 degree phase difference as shown in Figure 2.9 (a). Then they will pass through the filters (BPF-1 in the first channel) connected at these ports and will be applied to port-2 and port-3 of the second coupler which is just reversed version of coupler-1. The signals applied to port-2 and port-3 of the second coupler will be split to port-1 and port-4 with another 90° phase difference leading to cancellation of the signals at port-1 and addition at port-1. Thus, the whole signal will appear at port-4 of the second coupler. Details of the signal flows are shown in the same figure.

17

- The signals with frequencies outside the passband of BPF-1 will see identical reactive mismatches at ports 2 and 3 of coupler-1 (identical input impedances of the two filters). It is preferable to have these mismatches simulating OC or SC. The reflections from these terminations (blue lines in the figure) will cancel at port-1 and add at port-4 of coupler-1. Thus they will be directed to the next hybrid channel as described in Figure 2.9.b.

- If the transmitted and coupled port terminations (input impedances of the two filters connected to Ports 2 and 3 of coupler-1) are different from the specified matched termination R_2, then reflections will occur from these ports even in the passband of BPF-1. If reflections are identical, then they will be directed to the isolated port (Port-4 of coupler-1). No reflections will appear at input port, thus showing a good match at input, at the expense of some degradations in the adjacent channels.

- Figure 2.10 shows signal flow in a hybrid manifold multiplexer where we have also incorporated switches in series with filters for a possible switched channel multiplexer. The signals at frequencies f_1 and f_2 are directed to channel-1 and channel-2 outputs while the signal with frequency f_x which is assumed to be outside the passbands of the channels flows over the main line towards a dummy matched termination.

(a) For signals inside the passband of BPF1:

P

1   2   BPF-1   2   1   (matched load: R1)

$P_1 = 0$ (no output)

$P_4 = P$

4   BPF-1   (matched output)

no output   3   3   4

Coupler-1   Coupler-2

Voltages and powers in Coupler-1:

(P) $K_{12} = \sqrt{R_1 R_2 / 2}$ $V/\sqrt{2} \angle 0^o$ (P/2)

input   V   1 K_{12} 2 R_2 Transmit port

R_1

SYM ····· $K_1 = R_1$ $K_2 = R_2$

R_1 K_{12} R_2 coupled port

isolated port   4   3

$V/\sqrt{2} \angle -90^o$ (P/2)

Voltages and powers in Coupler-2:

$V/\sqrt{2} \angle 0^o$ (P/2) $V/\sqrt{2} \angle 0^o + V/\sqrt{2} \angle -180^o = 0$ (P1=0)

R_2 2 K_{12} 1 R_1

$K_2 = R_2$ $K_1 = R_1$

R_2 K_{12} R_1

3   4

$V/\sqrt{2} \angle -90^o$ (P/2) $V/\sqrt{2} \angle -90^o + V/\sqrt{2} \angle -90^o = V$ (P4=P)
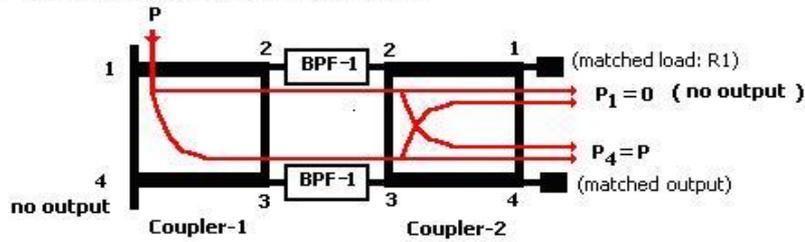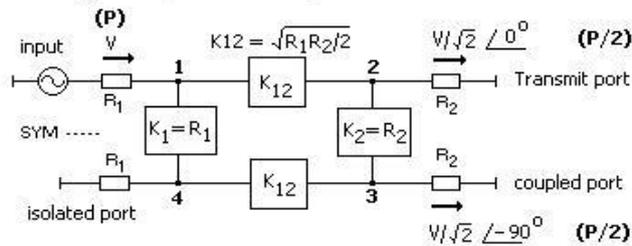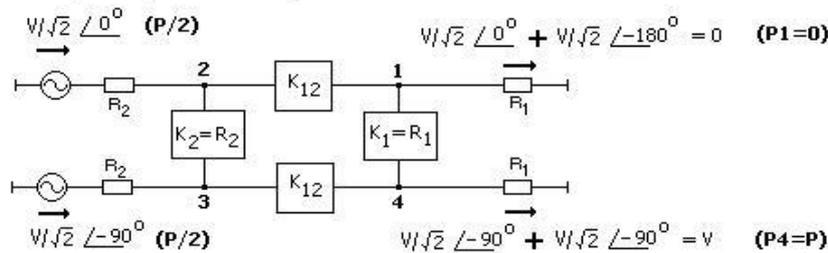
(b) For signals outside the passband of BPF1:

OC or SC

P

1   2   BPF-1   2   1

$P_1 = 0$ (no output)

$P_4 = 0$

4   BPF-1

$P_4 = P$ 3   3   4

coupler-1   coupler-2

Voltages in Coupler-1:

$V \angle 0^o$ $V/\sqrt{2} \angle 0^o$

R1   1 K_{12} 2   OC or SC

cancel $\begin{cases} \Gamma V/\sqrt{2} \angle 0^o \\ \Gamma V/\sqrt{2} \angle -180^o \end{cases}$ $\Gamma V/\sqrt{2} \angle 0^o$

$K_1 = R_1$ $K_2 = R_2$ identical reflections

add $\begin{cases} \Gamma V/\sqrt{2} \angle -90^o \\ \Gamma V/\sqrt{2} \angle -90^o \end{cases}$ $\Gamma V/\sqrt{2} \angle -90^o$

$V/\sqrt{2} \angle -90^o$

R1   4 K_{12} 3   OC or SC
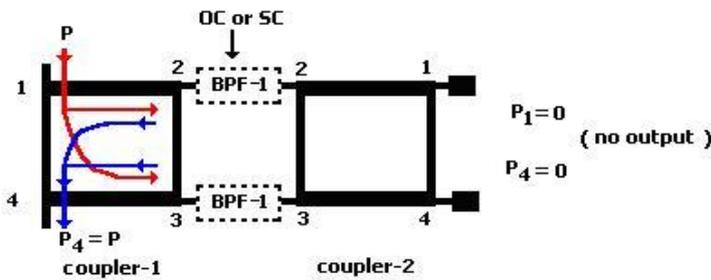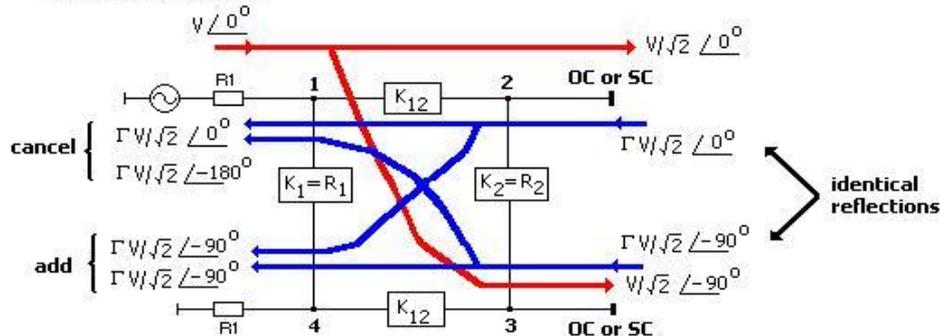
Figure 2. 9 Power Flow in One Channel of Hybrid Manifold Multiplexer

19

- Realization of inverters of the branch line couplers forms the main barrier for wideband applications. Also interactions between channels may be heavy, degrading responses of the channels. Therefore in practice the use of branch line couplers may have limited applications. Switchable multiplexers for wider bandwidth applications can be formed using different manifolds as will be described in the next section.

Figure 2. 10 A Switchable Hybrid Multiplexer

2.7 Circulator Coupled Multiplexers

There are other ways to connect the filters to the manifold to form a multiplexer. As an example circulators may be used to achieve better isolation between channels. In

20

this approach [50], there would be no need to use singly terminated or foreshortened doubly terminated filters, therefore exact filter synthesis can be used as shown in the Figure 2.11.
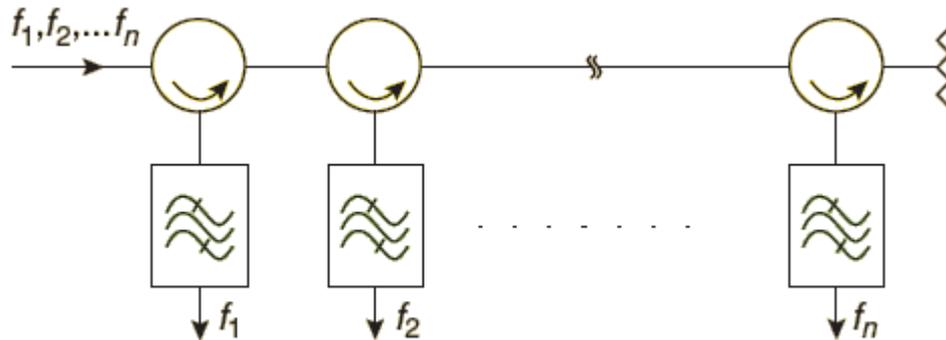
Figure 2. 11 A Circulator Coupled Multiplexer

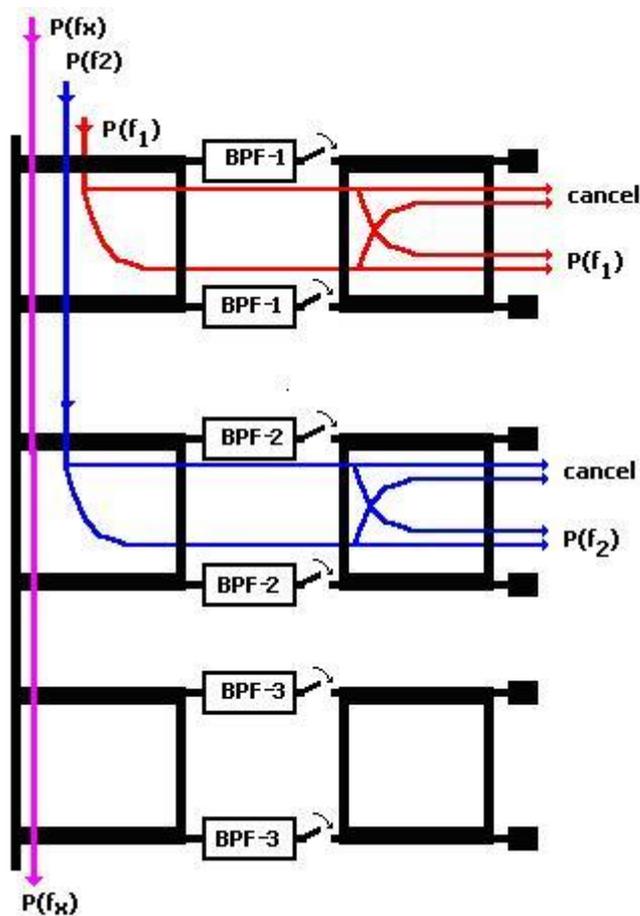Each channel in this case consists of a channel-dropping circulator and one filter, as shown in Figure 2.11. The unidirectional property of the circulator provides the same advantages as the hybrid-coupled approach in terms of amenability to modular integration and ease of design and assembly. The insertion loss of the first channel is the sum of the insertion loss of the channel filter and the insertion loss of the circulator. The subsequent channels exhibit a relatively higher loss due to the insertion loss incurred during each trip through the channel-dropping circulators. This is the most common realization for input multiplexers in satellite communications. The problem here is that circulators cost much and they are usually narrow bandwidth structures.

2.8 Multiplexers Using Directional Filters

The circulators described in the previous section may be eliminated by using directional filter structures [50] as shown in Figure 2.12.

Figure 2. 12 A Directional Filter Multiplexer

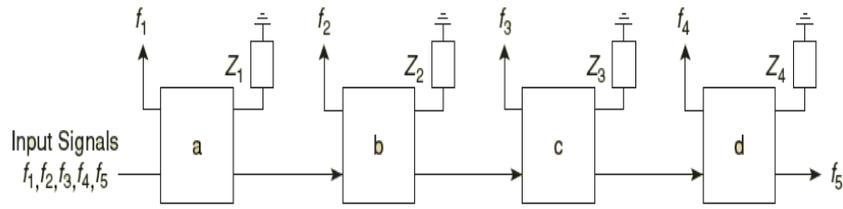Figure 2.12 illustrates a layout of a multiplexer realized by connecting directional filters in series. A directional filter is a four-port device in which one port is terminated in a load. The other three ports of the directional filter essentially act as a circulator connected to a bandpass filter. Power incident at one port emerges at the second port with a bandpass frequency response while the reflected power from the filter emerges at the third port. Directional filters, however, do not require the use of ferrite circulators. This multiplexing approach has the same advantages as the hybrid-coupled and circulator-coupled approaches. It is, however, limited to narrow-band applications.

2.9 Parallel Coupled Line Type Manifolds

In this thesis a novel approach is developed which uses parallel coupled line (PCL) three ports as diplexing elements of manifolds. In the approaches using T-junction type and hybrid coupled type manifolds the junction elements create problems and limitations. In this new approach the parameters of the diplexing PCL three ports are integral parts of the channel filters. Therefore, contrary to the cases of T-junction and hybrid junction, parameters of the PCL three ports will contribute to the responses of channel filters. Thus, besides avoiding the problems and limitations of T-junction hybrid junction manifolds, the junction parameters will help to improve the performance of the multiplexer.

Parallel coupled line three ports are formed.by leaving one of the coupled port of a PCL open circuit or short circuit. In the equivalent circuit of the PCL three ports

22

there are elements which can be treated as parts of the channel filters. Two types of manifolds can be formed: Series multiplexing manifold and parallel multiplexing manifold, as described below.

2.9.1.Series Multiplexing Manifold

The series diplexing three port and its equivalent circuit formed by commensurate line and stubs are shown in Figure 2.13 (a). Inspection of the equivalent circuit shows that the filters connected to the ports out-1 and out-2 will be in series. In order that this circuit work as a diplexer the filter connected to one of these ports must show SC input impedance within the passband of the other filter so that the whole input signal will be directed to only one of the two ports.

Figure 2.13 (b) shows a possible multiplexing structure (a triplexer). The channel filters are connected to port-2' of the diplexing PCL's. The diplexer sections with appropriate channel filters are cascaded to form multiplexer. The cascaded diplexing sections are separated by transmission line pieces which can be used to make the input impedance seen at port-1' zero at the passband center of the relevant diplexing PCL section on its left. Thus, for example if the frequency of the incoming signal is fo1 (passband center of BPF-1), then it will be directed to port-2' (BPF-1) because the impedance at port-1' is SC at that frequency. Since the circuits at port-1' and port-2' are in series, the BPF's must also present SC at the center frequencies of the other channels. The rightmost port should be a SC.

The equivalent circuit of the triplexer is shown in Figure 2.13 (c). It is seen that if the first elements of the BPF's are shunt SC stubs then the SC stubs of the diplexing PCL's can be treated as part of that filter. For example the comb type filters are suitable for this purpose. Such filters tend to have SC impedance outside their passbands. The shunt SC stubs of the diplexing PCL's and the transformers can be extracted form the combline filter during the synthesis stage. The transformers can be used to scale the impedance levels of the combline filters and also adjust the degree of coupling of the diplexing PCL's. The outputs can be left separate or combined through a power combiner or through a manifold of the same type as the input

manifold as shown in Figure 2.13 (d) to form a single input-single output version of the multiplexer. Switches can also be placed for switching in and out of the channels to convert the structure into a switched multiplexer to get some flexibility for covering targeted bandwidth while being able to reject some frequency bands. The switches may be placed inside the filters as described in [48]. Figure 2.13 (e) shows the layout of a possible realization using combline filters.

Practical realization difficulties may lead to limitations in bandwidths of the channels. Adjacent channels may interact because their input impedance may not be low enough to simulate SC over a sufficient bandwidth. Such problems may be eased by using guard bands between channels. The guard bands can then be covered by using another multiplexer in parallel using power combiners.

(a) Type-1 Series diplexing with two PCL's:

$$Z_{ev} = Z_1 (1 + 1/k)$$
$$Z_{od} = Z_1 (1 - 1/k)$$

$$k = \sqrt{1 + \frac{Z_2}{Z_1}} = \frac{Z_{ev} + Z_{od}}{Z_{ev} - Z_{od}}$$

$$Z_1 = \frac{Z_2}{k^2 - 1} = \frac{Z_{ev} + Z_{od}}{2}$$

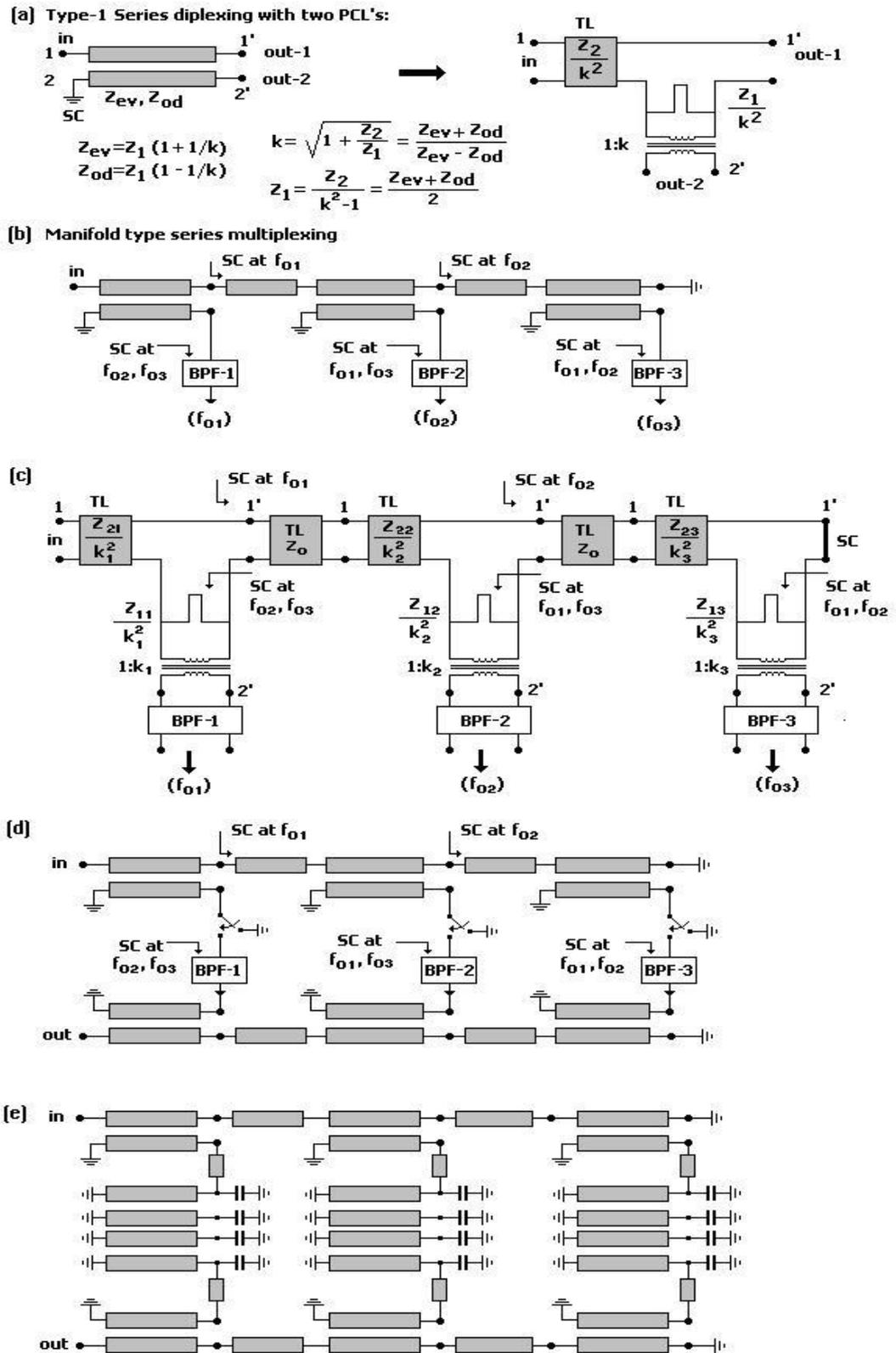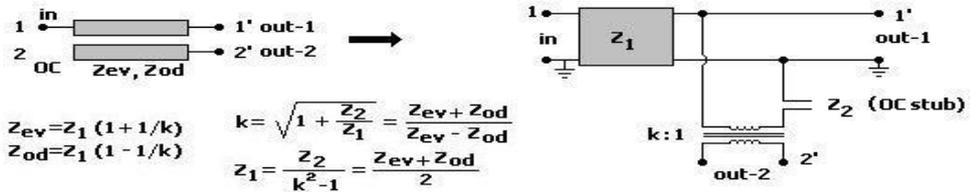**(b)** Manifold type series multiplexing

(c)

(d)

(e)

Figure 2. 13 (a) Series Diplexing PCL and Its Equivalent Circuit, (b) Series Multiplexing Structure (a Triplexer), (c) Equivalent Circuit of Series Multiplexer, (d) A Single Input-Single Output Switched Multiplexer and (e) A Possible Realization Layout Using Combline Filters

25

2.9.2. Parallel Multiplexing Manifold

The dual version of the series multiplexing manifold can be formed by using parallel diplexing circuit shown in Figure 2.14.a. The three port diplexing element is formed by leaving one port of the coupled line adjacent to the input port open circuit. It is seen that the filters that will be connected to the output ports out-1 and out-2 will be in parallel. In order that this circuit work as a diplexer the filter connected to one of these ports must show OC input impedance within the passband of the other filter. Figure 2.14.b shows a possible multiplexing structure (a triplexer). The channel filters are connected to port-2' of the diplexing PCL's. The cascaded diplexing sections are separated by transmission line pieces which can be used to make the input impedance seen at port-1' OC at the passband center frequency of the relevant diplexing PCL section on its left. Thus, for example if the frequency of the incoming signal is fo1 (passband center of BPF-1), then it will be directed to port-2' (BPF-1) because the impedance at port-1' is OC at that frequency. Since the circuits at port-1' and port-2' are in parallel, the BPF's must also present OC impedance at the center frequencies of the other channels. The transmission line pieces separating the channel filters form a barrier for channel bandwidths because their transforming action is frequency dependent, valid usually in a limited band. The rightmost port should be left as OC. The equivalent circuit of the triplexer is shown in Figure 2.14.c. It is seen that if the first elements of the BPF's are series OC stubs then the OC stubs of the diplexing PCL's can be treated as part of that filter. For example the OC edge coupled line type filters are suitable for this purpose. Such filters tend to have high impedance outside their passbands so that they will not load the other filter too much. The series OC stubs of the diplexing PCL's and the transformers can be extracted form the edge coupled line filter during the synthesis stage. The transformers can be used to scale the impedance levels of the edge coupled line filters and also adjust the degree of coupling of the diplexing PCL's. The outputs can be left separate or combined through a power combiner or through a manifold of the same type as the input manifold as shown in Figure 2.14.d to form a single input-single output version of the multiplexer. Switches can also be placed for switching in and out of the channels to convert the structure into a switched multiplexer to get some flexibility for covering targeted bandwidth while being able to reject some frequency bands.

The switches may be placed inside the filters. Figure 2.14.e shows the layout of a possible realization using a version of OC edge coupled line filters.
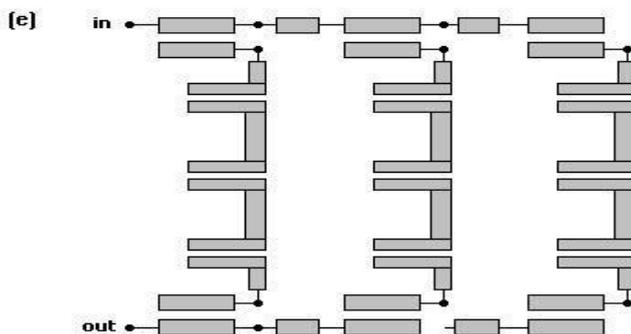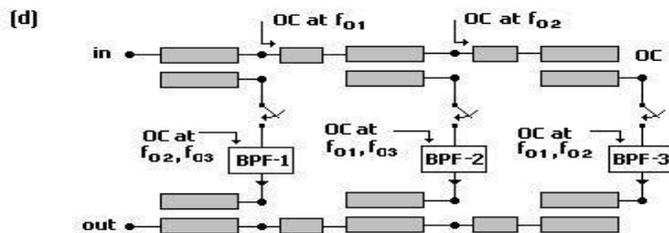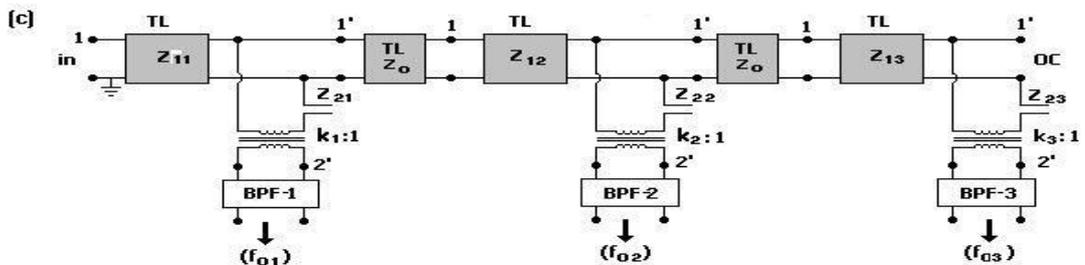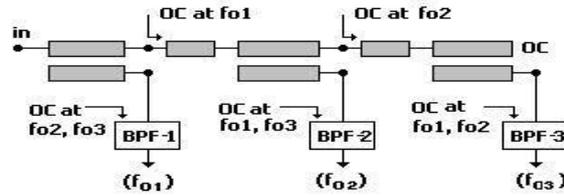

Figure 2. 14 a) Parallel diplexing PCL and its equivalent circuit. b) A parallel multiplexing structure (a triplexer). c) Equivalent circuit of parallel multiplexer. d) A single input-single output switched multiplexer. e) A possible realization layout using edge coupled line filters.

In microwave filter practice short circuits in the stubs or PCL's are problematic for realization. Therefore if possible, the filters containing short circuited elements are avoided. For this reason in this thesis parallel diplexing PCL approach is preferred which leads to channel filters with OC stubs and OC PCL types.

Channel interaction problems in contiguous multiplexers can be eased by using guard bands between channels. The guard bands can then be covered by using another multiplexer in parallel using power combiners as shown in Figure 2.15 in which two noncontiguous multiplexers are combined to form a contiguous multiplexer with single input and single output.
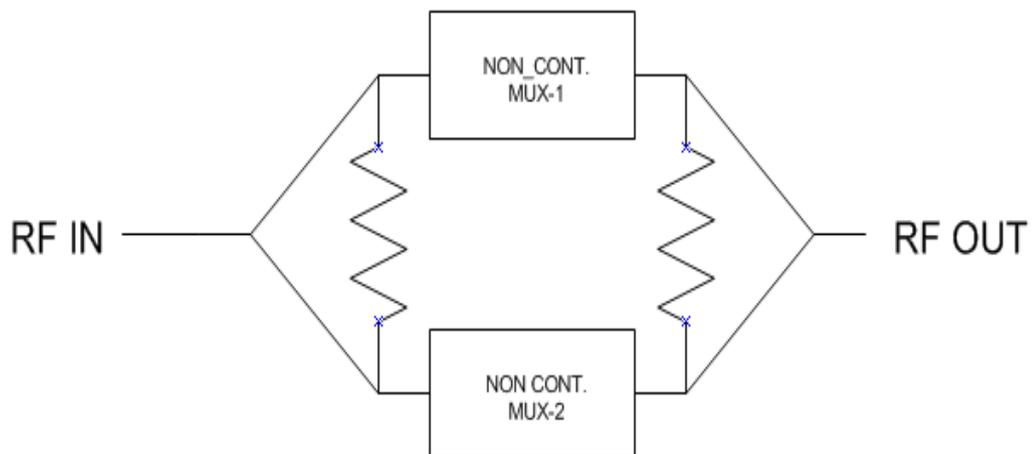

Figure 2. 15 Combining two non-contiguous multiplexers to form a contiguous multiplexer.

The phase correction at the crossover frequencies of adjacent channels can be introduced in one path to ensure crossover phase is correct to reduce the ripple at cross-over frequencies. The overall path length in both channels can be made identical, so the phase correction network needs to compensate only the phase difference of the adjacent channel filters at band edges.

2. 10. A Novel Switched Multiplexer Topology

One limitation of the topologies given in Figure 2.14.and 2.15 comes from the frequency dependent nature of the transmission line pieces separating the channels. These lines should behave as an open circuit or short circuit within the passband of the channel filter on its left. This is not possible over a wide band. Therefore the adjacent channels will interact leading to degradation in responses. Therefore these approaches seem to be applicable only to narrow-medium channel bandwidths. In this thesis this problem is solved by using LP filters instead of transmission line pieces to sustain open circuit behaviour over the passband of the adjacent channel filter as shown in Figures 2.16 and 2.17. These figures describe an 8 channel, 2-18 GHz switched multiplexer that is targeted to be designed and implemented in this thesis. This novel topology solves also the 3 dB ripple problem of the contiguous multiplexers. In these respects it is radically different from the previously described classical multiplexers, as follows.

The channel filters are grouped into two LP-HP type multiplexers with adjacent channels placed in different multiplexers to provide guard bands. The first SW_MUX is formed by integrating channels 1, 3, 5, 7 (2-4 GHz, 6-8 GHz, 10-12 GHz and 14-16 GHz) into a multiplexing manifold, then by connecting the same structure symmetrically with respect to a switch (Figure 1.16). This SW_MUX is called the odd half as it contains odd numbered channels. The second SW_MUX is formed by integrating channels 2, 4, 6, 8 (4-6 GHz, 8-10 GHz, 12-14 GHz and 16-18 GHz) into a multiplexing manifold, then by connecting the same structure symmetrically with respect to a switch (Figure 2.17). This SW_MUX is called the even half as it contains even numbered channels. Next even and odd halves are connected to form the final switched multiplexer as shown in Figure 2.18.

As mentioned above, the topologies used in these circuits enables to solve both bandwidth limitations and ripples at the corner frequencies of the contiguous multiplexers:
The LP-HP multiplexers are formed by combing contiguous diplexers having 4 GHz bandwidth. It should be noted that that instead of transmission line pieces, now

29

LPF's are used for isolating the adjacent diplexers by presenting OC (high impedance) to the diplexers on left. These LPF's, besides offering more flexibility for tuning and optimization to improve isolation between channels and to improve the overall return loss, they also serve as band limiters for the subsequent channel filters, to eliminate possible spurious responses.

2 GHz channels are formed by inserting LPF's with 2 GHz offset into the HP channel of the diplexers in cascade with the HPF. The corner frequencies of the LPF's are 2 GHz higher than the corner frequencies of the HPF's. Thus, the HP branch is converted into BP filter with 2 GHz bandwidth.

The main aim of using the 2 GHz offset LPF's is not only for setting the bandwidth, but also to avoid the 3 dB ripples of the classical contiguous multiplexers. Inspection of the circuits shows that there is no attenuation at cross-over frequencies of the channel filters. The signals at the corner frequencies (2 GHz, 4 GHz, 6 GHz, 8 GHz,10 GHz, 12 GHz, 14 GHz, 16 GHz, 18 GHz) will be first splitted then combined, so there will be no loss. However the signals within of the passband of the channels will be attenuated by 6 dB due to splitter-combiners. For perfect recombination the losses at corner frequencies must be 6 dB down with respect to center frequencies. Since channel filters are former by symmetrical combinations, the original designed filter should have 3 dB loss at band edges with respect to center frequencies. Since the LP-HP diplexers are contiguous, the loss at corner frequencies is 3 dB. The other corner frequency for the channel will be coming from the LP filter succeeding it. If the loss at corner frequency of the LP filter is also made 3 dB, when manifolds are connected back to back, the loss at corner frequencies will be 6 dB below the center frequencies, satisfying the above mentioned requirement.

Thus, the topology of the multiplexer is altered as shown in Figures 2.16 -2.17-2.18 where the contiguous HP-LP ladder type multiplexer or a SW_MUX is converted into two non-contiguous multiplexers with adjacent channels shared alternately by the two multiplexers to provide guard bands between channels as described in Figure 2.15. Thus, only two splitters will be enough to multiplex over any number of

30

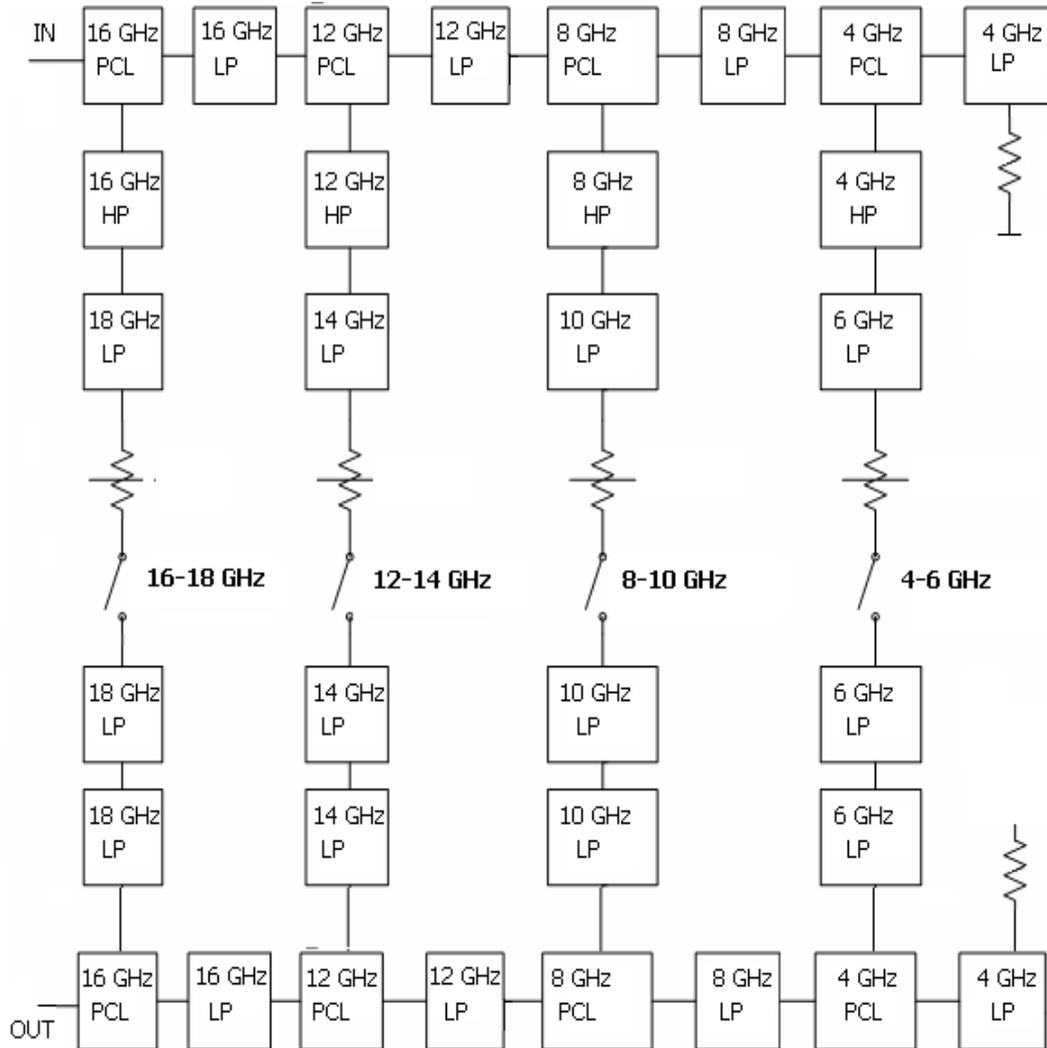channels. In the scope of this thesis a structure based on this topology will be designed.

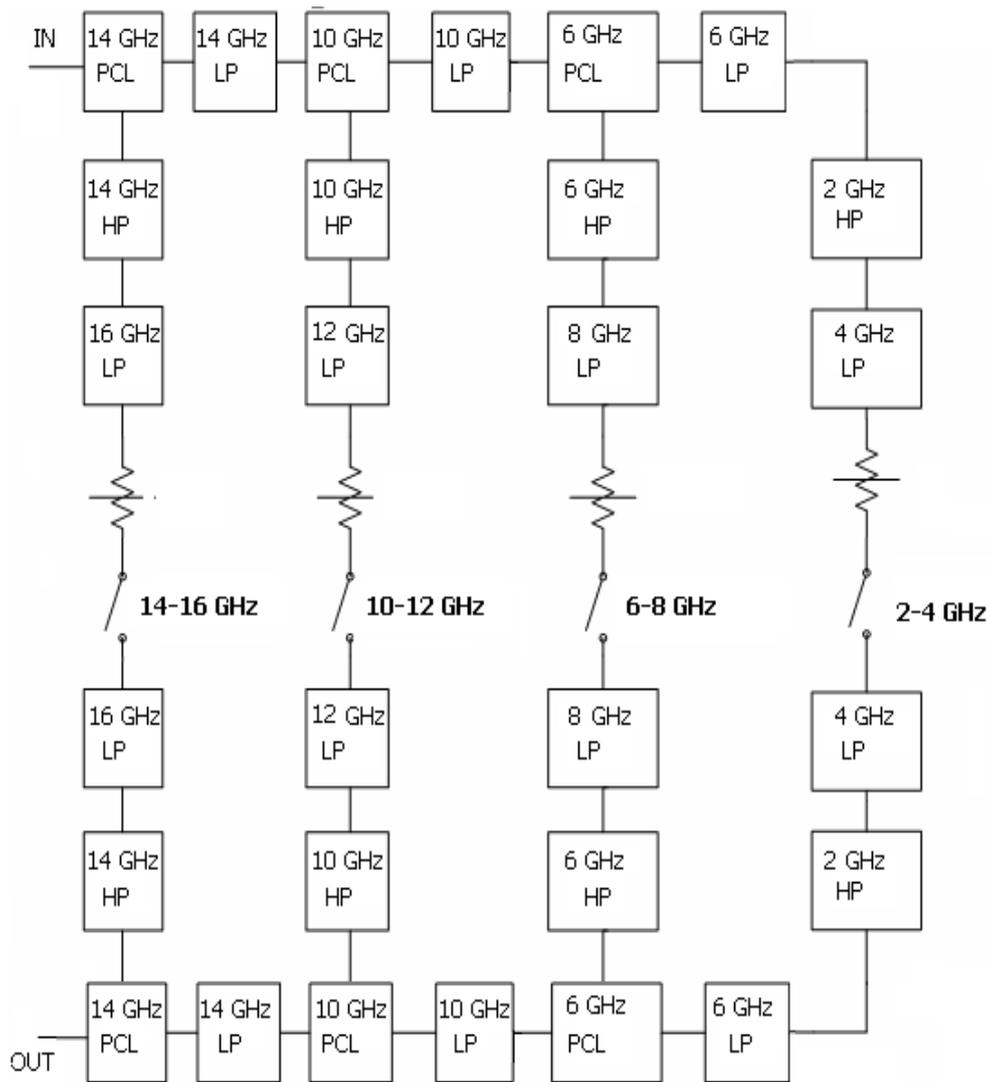**Figure 2. 16 Even Half of SW_MUX with LP filter**

31

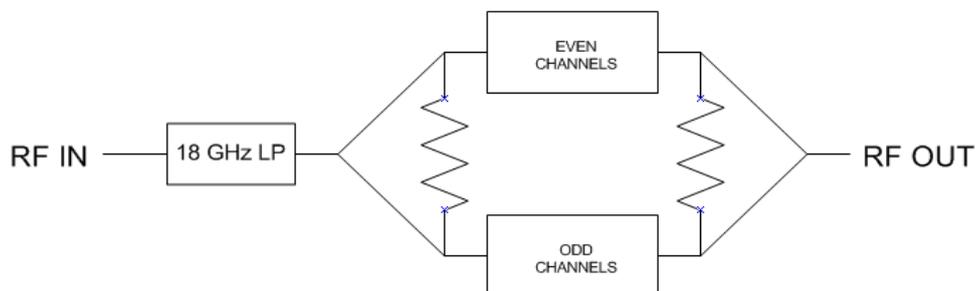**Figure 2. 17 Odd Half of SW_MUX with LP filter**

Figure 2. 18Connection of even and odd channel multiplexers through splitters.

Direct integration of the LP filters with HP filters of the HP channels may be problematic, because LP filter will be reflective in the passband of the HP filter, causing mismatches. These reflections may be weakened by using extra attenuators between LP and HP filters. Since the extra attenuators will create unaccounted loss a neater but slightly more complex solution would be to use diplexers in the HP channels as shown in Figure 2.19 and 2.20. The diplexer's corner frequency has again 2 GHz offset. Besides, these diplexers will also be used to form bandpass channels. This will eliminate the design of extra LP filters as well. It is seen that we still have attenuators in the HP branches. They are needed to attenuate the unavoidable reflections at switch-filter junctions. That is, attenuators are usually unavoidable elements in such reflection sensitive multiplexers. This is mostly the case in every manifold coupled switch multiplexer.
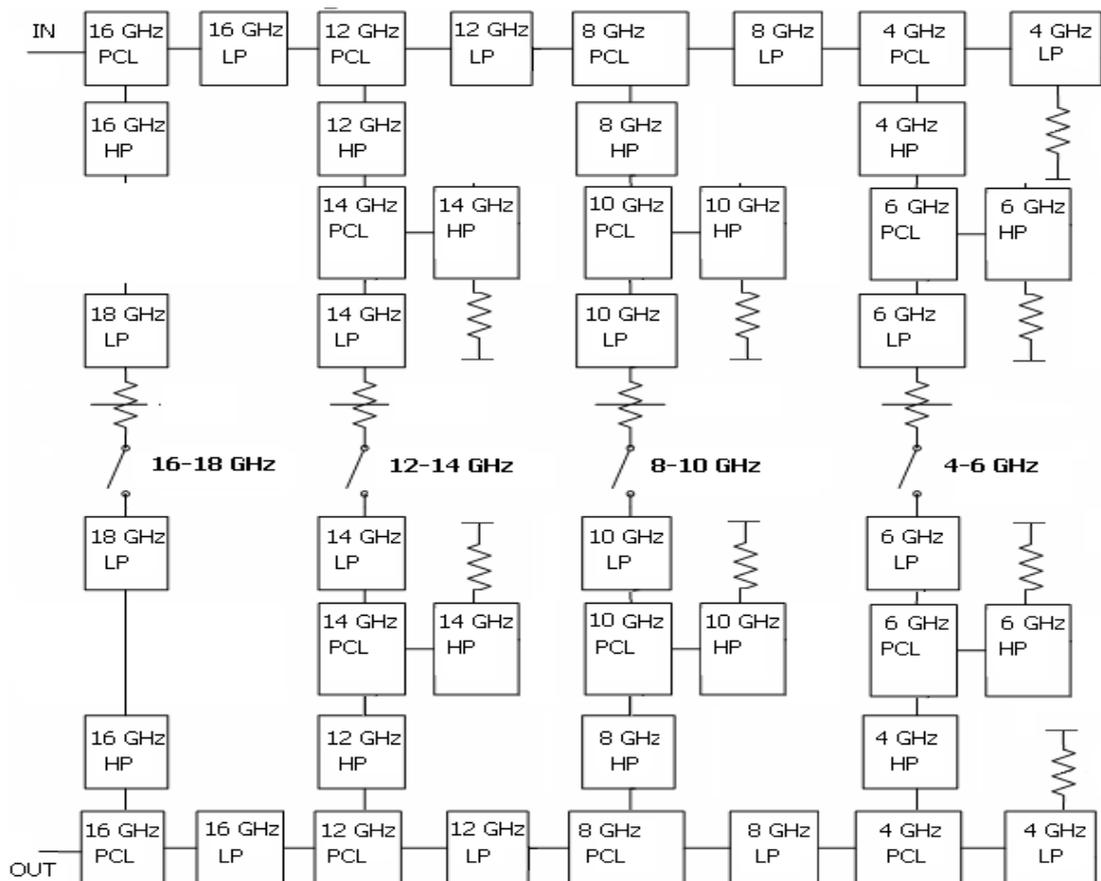
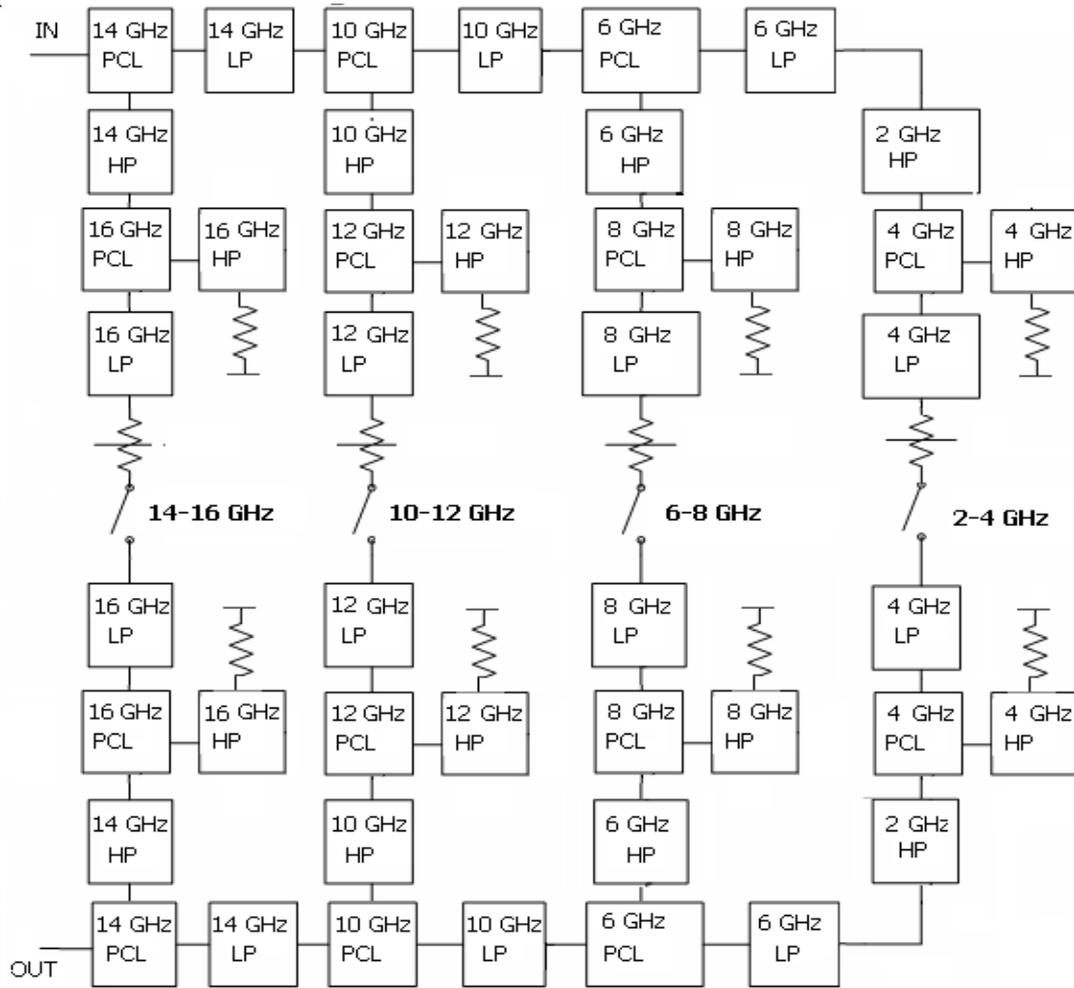**Figure 2. 19 Even Half of SW_MUX with diplexers in place of extra attenuators.**

Figure 2. 20 Odd Half of SW_MUX with diplexers in place of extra attenuators.

CHAPTER 3

THE USE OF PARALLEL COUPLED LINES AS DIPLEXING ELEMENTS

A diplexer has essentially three parts: 2 channel filters and a diplexing mechanism. As noted in the previous chapter, parallel coupled lines can be used as diplexing mechanisms. In the previous chapter some topologies involving short circuited parallel coupled lines (SCPCL) to be used for series diplexing and open circuited parallel coupled line (OCPCL) for parallel diplexing. In this chapter, first, different circuit models will be presented for parallel coupled lines, then the series diplexing circuits using SCPCL and parallel diplexing circuits using OCPCL will be presented. Finally a comparison between traditional T-junction diplexing and OCPCL diplexing will be made in matching and isolation aspects.

Parallel coupled lines (PCL) are essential elements of distributed element highpass and bandpass filters. Parallel coupled line pairs are four port circuits. They can be converted into three port, two port or one port elements by terminating their unused ports in OC, SC, open or short circuited stubs, etc. as described in literature, for example by Sato and Crystal [7] and Malherbe [18]. In most of the distributed element diplexers and multiplexers parallel coupled lines are used as three port networks which can be used for splitting the input signal into two paths (diplexing PCL). Similarly three coupled lines with no coupling beyond the adjacent line can also be used for splitting input signal into two paths.

In this section a summary of three port parallel coupled lines will be presented. Since derivation of the equivalent circuits of PCL sections are usually confusing and complex for many engineers with different backgrounds, detailed explanations are given below using several different approaches.

3. 1. Circuit Models of Parallel Coupled LIines

In Figure 3.1.a a parallel coupled transmission line pair is shown in a homogeneous nonmagnetic medium in between two ground planes. For pure TEM mode operation the propagation constant is

$$\beta = \frac{\omega}{v} = \omega\sqrt{\mu\varepsilon} = \frac{\omega\sqrt{\varepsilon_r}}{c} \tag{3.1.1}$$

Such a coupled line pair can be described in several different ways as follows:

a) Three Line Model of a two-wire line above ground:

A coupled line pair can be characterized through their per unit length line-to-ground and line-to-line inductance and capacitance parameters L11, L12, L22 and C10, C20, C12, as shown in Figure 3.1.b. The pair L11-C10 can be assumed to describe a two-wire TEM mode transmission line between Line-1 and ground. Similarly, the pair L22-C20 can be assumed to describe a two-wire TEM mode line between Line-2 and ground. By the same reasoning the pair L12-C12 can be assumed to describe a two-wire TEM mode transmission line in between Line-1 and Line-2. So, we can model the coupled line pair as consisting of three two-wire TEM mode transmission lines as sown in Figure 3.1.b. At first sight the terminology of representing a two-line system with three lines may appear to be confusing. However, the two PCL system is actually a three wire system with the ground being the third wire.
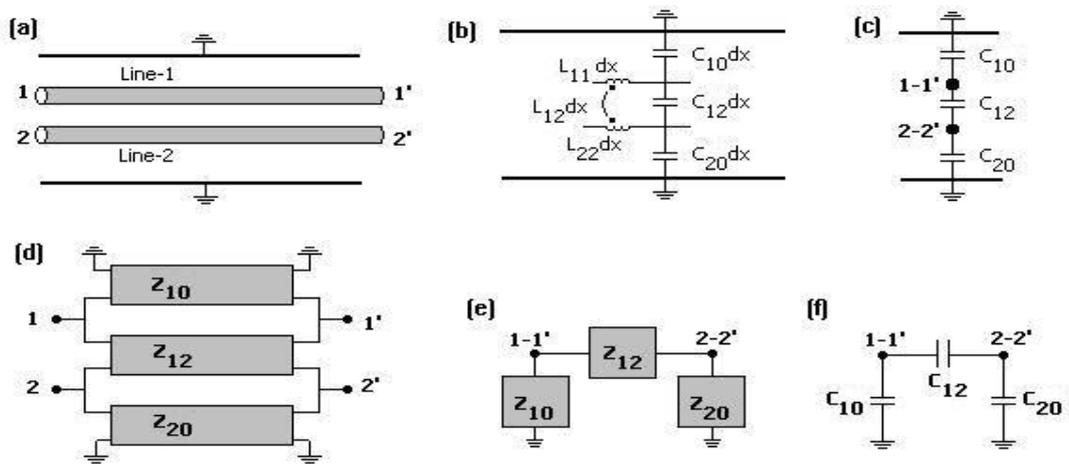

Figure 3. 1 Three Line model of a parallel coupled line pair.

36

For pure TEM mode operation the per unit length parameters are related to the propagation constant as follows:

$$\beta = \omega \sqrt{L_{11}C_{10}} = \omega \sqrt{L_{22}C_{20}} = \omega \sqrt{L_{12}C_{12}} = \frac{\omega}{v} = \omega \sqrt{\mu \varepsilon} = \frac{\omega \sqrt{\varepsilon_r}}{c}$$

(3.1.2)

Thus, L's and C's of a line are related to each other as follows:

$$L_{11} = \frac{\varepsilon_r}{c^2 C_{10}} \qquad L_{22} \frac{\varepsilon_r}{c^2 C_{20}} \qquad L_{12} = \frac{\varepsilon_r}{c^2 C_{12}}$$

(3.1.3)

Thus, the three lines, hence the coupled line pair can be characterized through the per unit length capacitances C10, C20 and C12 only, as shown in Figure 3.1.c. Characteristic impedances of each transmission line can be calculated through the definitions

$$Z_{10} = \sqrt{\frac{L_{11}}{C_{10}}} = \frac{\sqrt{\varepsilon_r}}{cC_{10}} \quad Z_{20} = \sqrt{\frac{L_{22}}{C_{20}}} = \frac{\sqrt{\varepsilon_r}}{cC_{20}} \quad Z_{12} = \sqrt{\frac{L_{12}}{C_{12}}} = \frac{\sqrt{\varepsilon_r}}{cC_{12}}$$

(3.1.4)

In Figure 3.1.d the three uncoupled transmission lines are described now using their characteristic impedances. The ports of Line-1 are numbered as 1 and 4 while the ports of Line-2 are numbered as 2 and 3. For use in later descriptions, In Figure 3.1.e and f the network is repeated for the case of a single ground plane placed at bottom. On the left we have Line-1 (or Line 1-4) and on the right we have Line-2 (or Line 2-3). This circuit model will be used to derive other equivalent circuits which may be easier to use on different applications.

b) Even-Odd Mode Description of a Symmetric Coupled Line Pair

If the two coupled lines are identical then we have L11=L22, C11=C22, thus simplifying the characterization through the impedances also:

$$Z11 = Z22 = \sqrt{\frac{L11}{C10}} = \frac{\sqrt{\varepsilon_r}}{cC10}, \qquad Z12 = \sqrt{\frac{L12}{C12}} = \frac{\sqrt{\varepsilon_r}}{cC12}$$

(3.1.5)

For such cases the excitations, voltage, current, power waves and coupled line pair can be decomposed even and odd mode halves as described in Figure 3.2. Representing the voltage waves on Line-1 and Line-2 as V1(x) and V2(x), we can always write

$$V1(x) = Ve(x) + Vod(x)$$

(3.1.6)

$$V2(x) = Ve(x) - Vod(x) \tag{3.1.7}$$

Under even mode excitation the two lines have identical voltages, currents and power. Thus, we can place an OC wall on the symmetry plane between the two lines, splitting the mutual capacitor C12 into two equal capacitors, 2C12 as shown in Figure 3.2.c. Since the capacitors are open on the symmetry plane we can disregard them. The two halves form identical lines whose per unit length capacitance to ground is C10 only. It is named as even mode capacitance Cev:

$$Ce = C_{10} \tag{3.1.8}$$

The characteristic impedance of the two identical lines can thus be calculated using the even mode capacitor as

$$Zev = \frac{\sqrt{\varepsilon_r}}{cCev} \tag{3.1.9}$$

Under odd mode excitation the voltages on the two lines are equal in magnitude but opposite in phase. Thus, the symmetry plane has zero voltage. That is, it can be assumed as just extension of the ground plane. The mutual capacitor C12 is split by the symmetry plane into two pieces with capacitance 2C12. Since one ends of these capacitors are grounded the capacitors 2C12 become parallel with the line-to-ground capacitor C10. Thus, the total line-to-ground per unit length capacitance is C10+2C12, and it is named as odd mode capacitance:

$$Cod = C_{10} + 2C_{12} \tag{3.1.10}$$

The characteristic impedance of the odd mode half is then evaluated as:

$$Zod = \frac{\sqrt{\varepsilon_r}}{cCod} \tag{3.1.11}$$

Thus, if the capacitances Cev and Cod can be calculated then the even and odd mode characteristic impedances describing the coupled line pair can be found. It is clear that only two parameters Zev and Zodd are sufficient to describe a symmetric PCL.
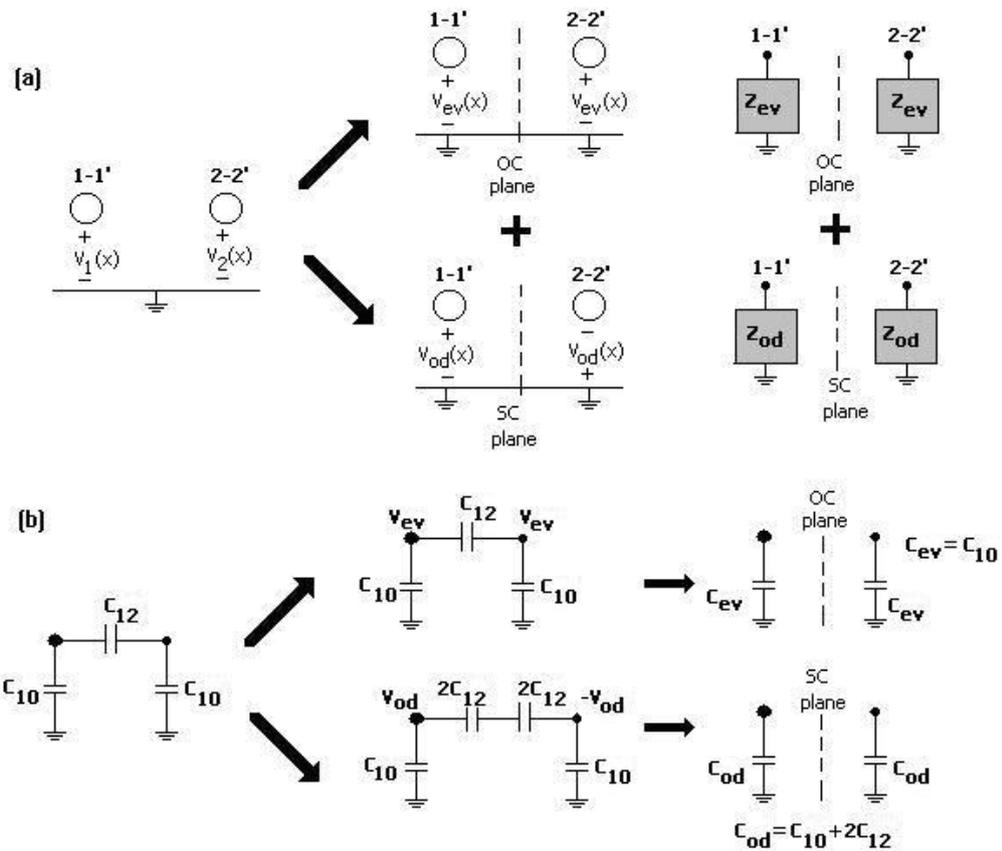
Figure 3. 2 Even-odd mode decomposition of a symmetric parallel coupled line pair

c) Norton and Pi-Tee-L Transformations on Three Line Network Model

Norton and Pi-Tee-L transformations can be applied on a three line network model of a coupled line pair circuit to form different equivalent four ports. Norton transformation is shown in Figure 3.3. Originally it was defined on lumped elements but can be generalized to cover distributed elements also. Norton transformation converts a series element (R, L, C, Z, jX, OC Stub, SC Stub, TL) into a Pi-section together with a transformer while a shunt element is converted into a Tee-section together with a transformer. The new elements are of the same type as the original element. One of the shunt elements of the Pi-section and one of the series elements of the Tee-section is negative always. So, Norton transformation can be used to find new equivalent circuits at the expense of increased redundancy where one element is replaced by four elements.
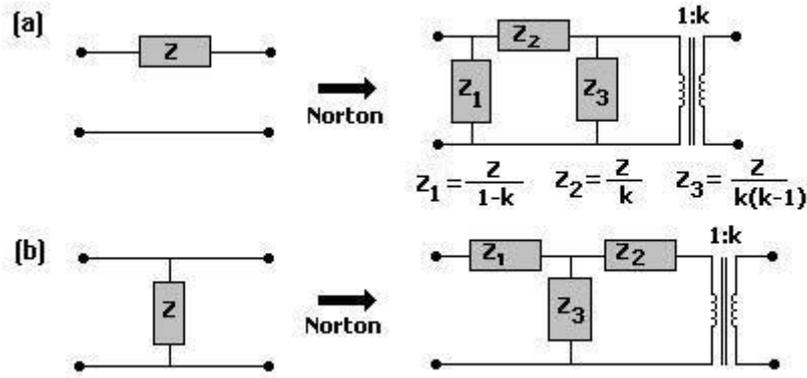
Figure 3. 3. Norton Transformations

Pi-Tee-L transformations are more sophisticated versions of Norton transformations. A Pi, Tee or L section can be converted into another Pi, Tee or L section as shown in Figure 3.4.
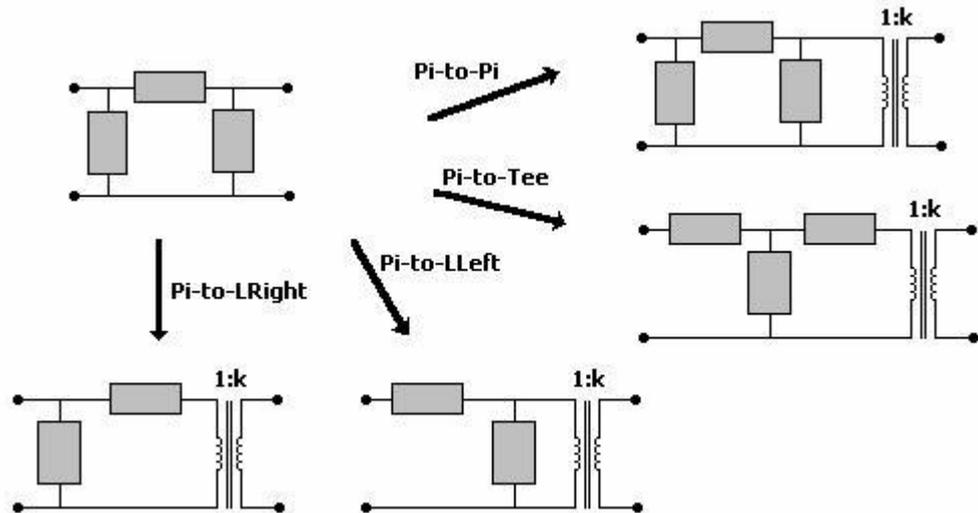
Figure 3. 4 Pi-Tee-L Transformations

These transformations can also be generalized to parallel coupled lines as described in Figure 3.5. In Figure 3.5.a the per unit length capacitance Pi-section representing a parallel coupled line is shown. It can be converted into another capacitive Pi, Tee or L section using Pi-Tee-L transformations. In the figure a Pi-to-Pi transformation is

40

shown. Since in the new Pi-section we have different capacitances the corresponding transmission lines will have different characteristic impedances as shown in Figures 3.5.b and c. In this transformation the interpretation of the transformer may need care. The transformer on the right of C_{20} is actually running along the Line-2 (Line 2-2'), including the ports 2 and 2'. However, since we will use these circuits through their ports only, this transformer need be placed only at the two ends of the Line-2, at ports 2 and 2' only, as shown in Figure 3.5.c. Note that in this figure the transmission line of impedance Z_{12} formed between the two wires is drawn wider than the transmission lines formed between wires and ground, just to ease visualization to differentiate the wire-to-wire and wire-to-ground types of transmission lines, from top view.

This transformation can be used to find different proper alternative equivalent parallel coupled line sections. The most common application is conversion of an asymmetric parallel coupled line ($C_{20} \neq C_{10}$) into a symmetric one by imposing equal shunt capacitor condition ($C_{20}=C_{10}$, identical coupled lines). This transformation can be generalized to make all lines of an N-parallel coupled line system identical, as described in Figure 3.6 on a 5 coupled line system. By repeated application of Pi-to-Pi transformations it is possible to equate all the shunt capacitors (Figure 3.6.a). Figure 3.6.b shows pictorial descriptions of the initial and final 5 coupled line system. The resulting transformers may be collected at one end of the structure.
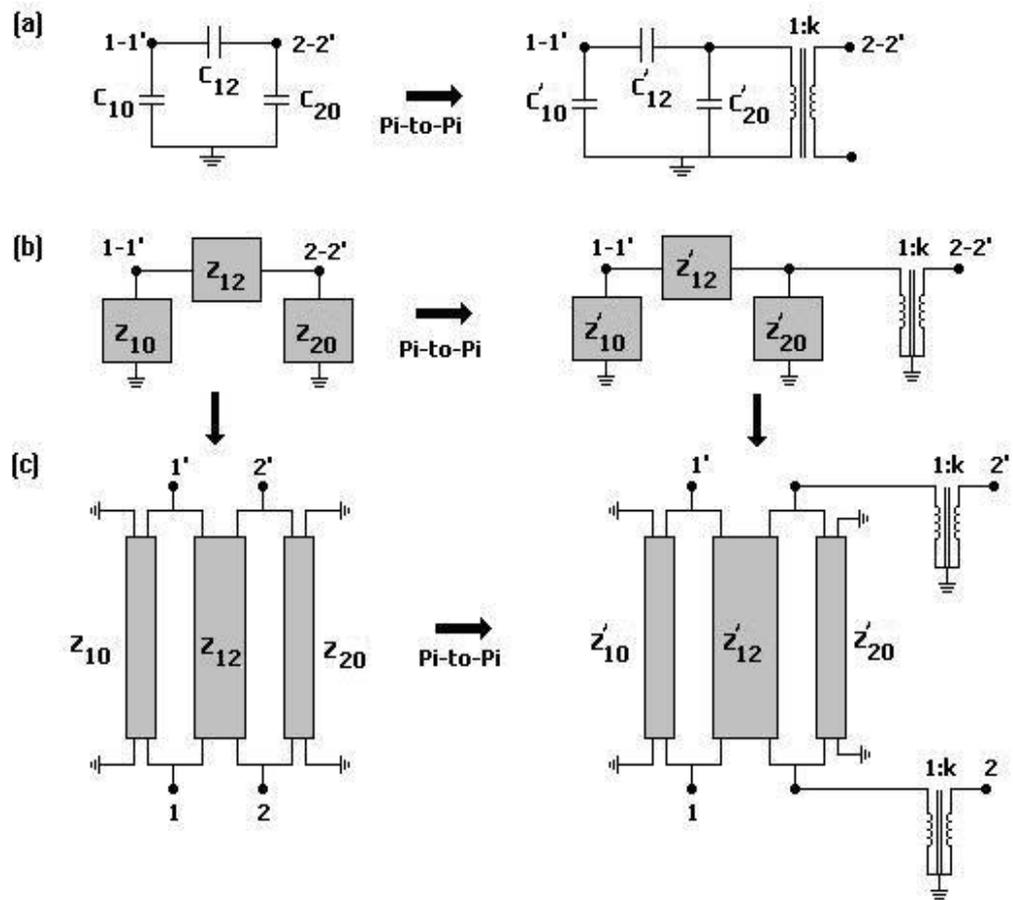
Figure 3. 5. Pi to Pi Transformatiom applied on a coupled line
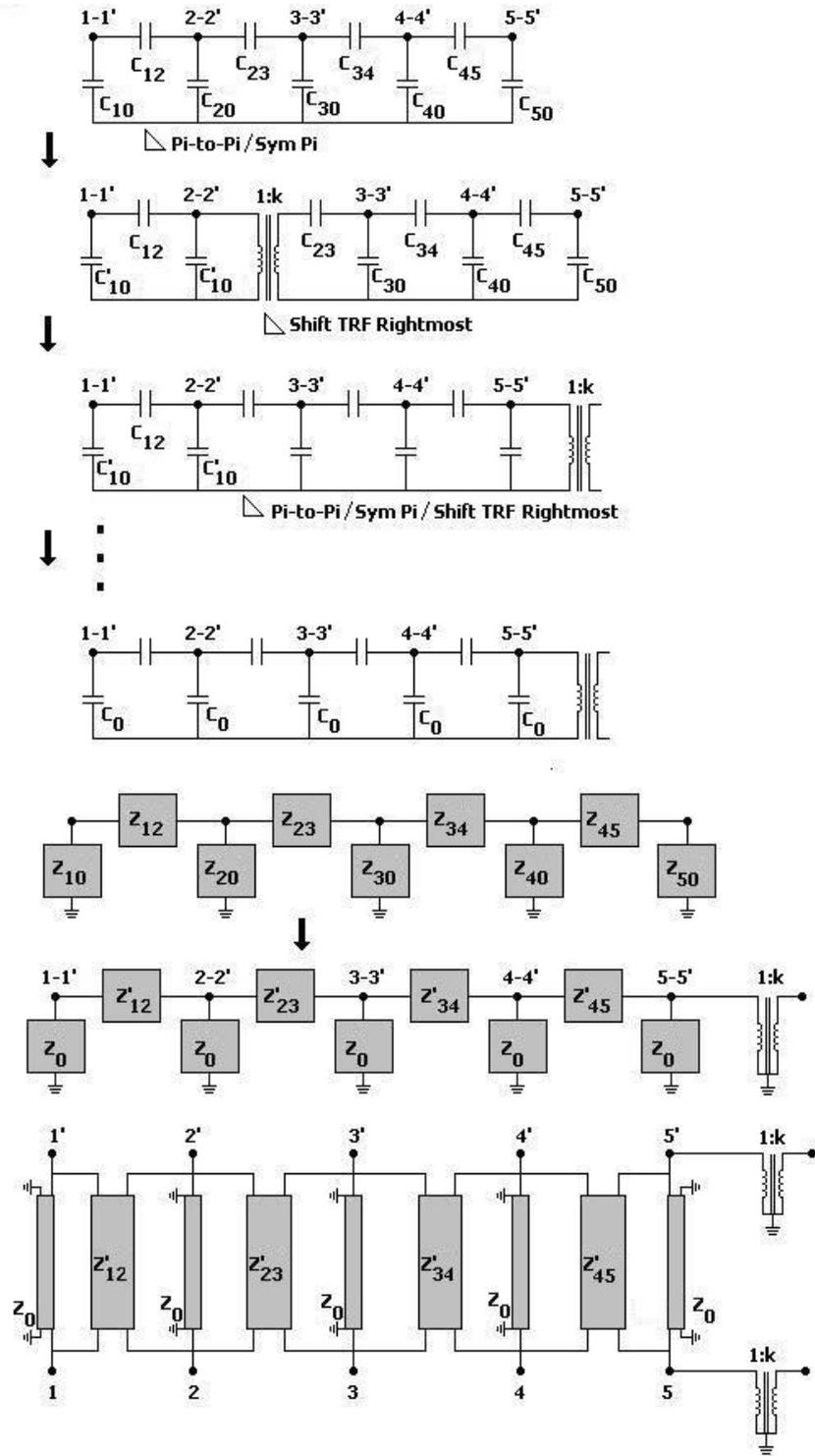
Figure 3. 6 Equating shunt impedances of an N-coupled line system for N=5

d) Two Line model of a PCL pair:

Another important transformation is Pi-to-LLeft and Pi-to-LRight transformations applied on two parallel coupled lines. These transformations result in a two-line representation for a parallel coupled line system which is easier to handle for the formation of one, two, three and four port elements by placing various port conditions [18]. Figure 3.7.a describes this transformation for conversion of the Pi-section into an L-Right section. The figures in the top row shows the cross-sectional description while the bottom ones show the top view. In the LRight model the transformers appear on the right side, hence at ports 2 and 3 only. Figure 3.7.b describes Pi-to-LLeft transformation where the transformers appear on left side and hence at ports 1 and 4 only. In Figure 3.7.c the LRight and LLeft models are redrawn in an easy to use manner for imposition of the port conditions that will be described later. Note that in this circuit the four port is described by a transformer and two transmission lines. Impedances of the lines are conventionally referred to as $Z_1 = Z'_{10}$ and $Z_2 = Z'_{12}$ in the LRight model. In LLeft model we use the convention $Z_1 = Z'_{20}$ and $Z_2 = Z'_{12}$. The two models are easier to use for different port conditions. Equations relating the Pi-model and L-model of a parallel coupled line pair have special practical importance as will be seen later. Therefore let's derive them. The ABCD parameters of the Pi-section shown in Figure 3.7.b can be calculated as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y_{10} & 1 \end{bmatrix}\begin{bmatrix} 1 & Z_{12} \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ Y_{20} & 1 \end{bmatrix} = \begin{bmatrix} 1+Y_{20}Z_{12} & Z_{12} \\ Y_{10}+Y_{20}(1+Y_{10}Z_{12}) & 1+Y_{10}Z_{12} \end{bmatrix} \quad (3.1.12)$$

$$\begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y'_{10} & 1 \end{bmatrix}\begin{bmatrix} 1 & Z'_{12} \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ Y'_{20} & 1 \end{bmatrix}\begin{bmatrix} k & 0 \\ 0 & 1/k \end{bmatrix} = \begin{bmatrix} k(1+Y'_{20}Z'_{12}) & Z'_{12}/k \\ k(Y'_{10}+Y'_{20}(1+Y'_{10}Z'_{12})) & (1+Y'_{10}Z'_{12})/k \end{bmatrix} \quad (3.1.13)$$

Given $Z_{10} = 1/Y_{10}$, Z_{12} and $Z_{20} = 1/Y_{20}$, we can calculate the parameters Z'_{10}, Z'_{12}, Z'_{20} and k of the new Pi-section by equating the corresponding A, B, C and D parameters. Since we get three independent equations to solve for the four unknowns, we may set any one of the unknowns freely and then determine the other three. For example

setting $Z'_{20}=0$ we can form an L-section (LRight section) shown in Figure 3.7.b. The parameters Z'_{10}, Z'_{12} and k of the LRight section can be solved as follows:

Equating A parameters k is solved as

$$k = 1 + Z_{12}/Z_{20}$$

(3.1.14)

Equating D parameters we get

$$Z'_{12}/Z'_{10} = k(1 + Z_{12}/Z_{10}) - 1$$

(3.1.15)

Inserting k from Eq. 2.1.3 into 2.1.4 we get

$$Z'_{12}/Z'_{10} = Z_{12}(\frac{1}{Z_{10}} + \frac{1}{Z_{20}} + \frac{Z_{12}}{Z_{10}Z_{20}})$$

(3.1.16)

Equating B parameters, Z'12 is solved:

$$Z'_{12} = Z_{12}(1 + Z_{12}/Z_{20})$$

(3.1.17)

Using Eq. 2.1.6 in 2.1.5 Z'10 can be solved:

$$\frac{1}{Z'_{10}} = \frac{1}{Z_{10}} + \frac{1}{Z_{20}} + \frac{1}{Z_{12} + Z_{20}}$$

(3.1.18)

Thus, given Z_{10}, Z_{20} and Z_{12}, the parameters Z'_{10}, Z'_{12} and k can be solved.
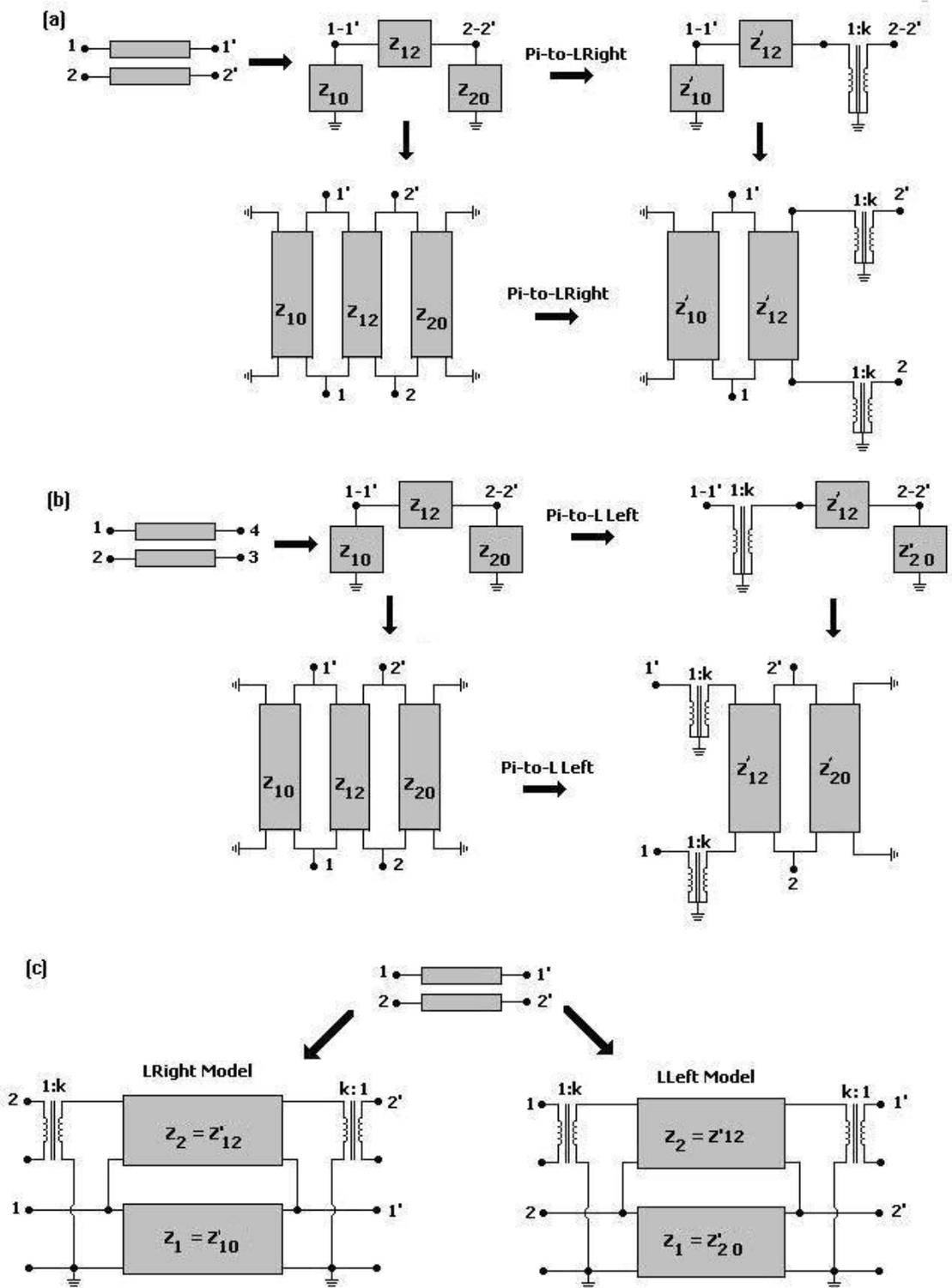
Figure 3. 7 Pi –to- Lright and Pi –to- Lleft transformations applies to a parallel coupled line

For a symmetric Pi-section, imposing the condition $Z_{20}=Z_{10}$, the equations are simplified as follows:

Eq. 3.1.18 becomes

$$Z'_{10} = Z_{10} \frac{Z_{12} + Z_{10}}{Z_{12} + 2Z_{10}}$$

(3.1.19)

Eq. 3.1.17 becomes

$$Z'_{12} = Z_{12}(1 + Z_{12} / Z_{10})$$

(3.1.20)

Eq. 3.1.14 gives the transformer turns ratio k as

$$k = 1 + Z_{12} / Z_{10}$$

(3.1.21)

However this expression can be written in terms of Z'_{10} and Z'_{12} as follows:

Equating D parameters we get

$$1 + Z'_{12} / Z'_{10} = k(1 + Z_{12} / Z_{10})$$

(3.1.22)

Using Eq.2.1.10 in 2.1.11 we get

$$1 + Z'_{12} / Z'_{10} = k^2$$

(3.1.23)

giving

$$k = \sqrt{1 + \frac{Z'_{12}}{Z'_{10}}}$$

(3.1.24)

As will be seen in the following sections the L-section models for a parallel coupled line is useful for imposing the port conditions. Since it is frequently used we redefine the line impedances of L-sections as follows:

$$Z'_{10} = Z_1 \qquad Z'_{12} = Z_2$$

(3.1.25)

Thus, k can also be written in terms of Z1 and Z2 as

$$k = \sqrt{1 + \frac{Z_2}{Z_1}}$$

(3.1.26)

Thus, a symmetric parallel coupled line can be represented by any pair of Z_1, Z_2 or Z_1, k or Z_2, k. That is only two parameters need be specified for a complete description, with the third one being set inherently through the above interrelations. On the other hand realization of parallel coupled lines usually necessitates the knowledge of even and odd mode impedances. Therefore it is good to have the

47

relations between the parameters Z_1, Z_2 and k of the L-section model and Even-odd mode impedances:

By definition, we have seen that under even mode excitation the two lines are separated by an OC symmetry plane, hence leading to

$$Z_{ev} = Z_{10}$$

(3.1.27)

Under odd mode excitation the symmetry plane is a SC plane at ground potential. Therefore the series impedance Z_{12} is split into two equal pieces of impedance $Z_{12}/2$ and the total line-to-ground impedance from any line becomes parallel combination of Z_{10} and $Z_{12}/2$, giving the odd mode impedance as

$$Z_{od} = \frac{Z_{10}Z_{12}}{Z_{12} + 2Z_{10}}$$

(3.1.28)

Using Eq. 2.1.8 in 2.1.16 and 2.1.17, it can be shown that

$$Z_{ev} = Z_1(1 + \frac{1}{k}) \qquad Z_{od} = Z_1(1 - \frac{1}{k})$$

(3.1.29)

Thus, knowing Z1 and k of the L-section model, we can find the even and odd mode impedances of symmetric parallel coupled lines easily. The reversed forms of the above equations are

$$Z_1 = \frac{Zev + Zod}{2} \quad, \quad k = \frac{Zev + Zod}{Zev - Zod} \qquad Z_2 = Z_1(k^2 - 1)$$

(3.1.30)

3.2. Series and Parallel Diplexeing Using Two Parallel Coupled Line Sections

As examples for the applications of two PCL sections let's see the formation of some three port elements that may be used in diplexing and multiplexing applications.

a) Type-1 series diplexing with two parallel coupled lines

Figure 3.8.a shows a two parallel coupled line section (PCL) with port-2 short circuited to ground. This PCL can be used for series diplexing. Development of its circuit model is described in the figure. The equivalent L-Left circuit model is shown in Figure 3.8.b. The SC at port-2 decouples the two lines giving the circuit of Figure

3.8.c. This SC also converts the line 2-2' into a SC stub in parallel with the transformer of port-2' as shown in Figure 3.7.d which can be redrawn as in Figure 3.8.e to display the series nature of the ports 1' and 2' in a clearer manner. The ground in between the ports 1' and 2' can be moved the left of the SC stub by introducing a phase changing 1:-1 transformer as in Figure 3.8.f. The transformer 1:k at port-1 can be moved to the right ports, canceling the transformer k:1 at port-1' while introducing transformer 1:-k at port-2' and the circuit can be redrawn as shown in Figure 3.8.g. With input applied from port-1, the outputs will be taken from port-1' and port-2'. The shunt SC stub at port-2' enforces that a HP filter or BP filter must be placed in that port with the available SC stub and the transformer being part of that filter. There is no restriction on the type of the filter that will be placed at port-1'. In LP-HP type diplexers and multiplexers this port is used for the LP channels. This structure is named as Type-1 series diplexing PCL. The transmission line at input is common to both channels. The interrelations between the even-odd mode impedances and k-Z_1-Z_2 parameters are also shown in the figure for convenience. Figure 3.8.h shows the case when also Port-1' is SC. In this case the circuit reduces to the classical interdigital type SC PCL that is used in HP filters.

Miscellaneous series multiplexing circuits:

Just as extension of the type-1 series diplexing PCL section, the circuits shown in Figure 3.9 can be used for series multiplexing purposes.

Type-1 Series diplexing with two PCL's:

$$k = \sqrt{1 + \frac{z_2}{z_1}} = \frac{z_{ev} + z_{od}}{z_{ev} - z_{od}} \qquad z_{ev} = z_1\left(1 + \frac{1}{k}\right)$$

$$z_1 = \frac{z_2}{k^2 - 1} = \frac{z_{ev} + z_{od}}{2} \qquad z_{od} = z_1\left(1 - \frac{1}{k}\right)$$

$$z_2 = z_1(k^2 - 1)$$
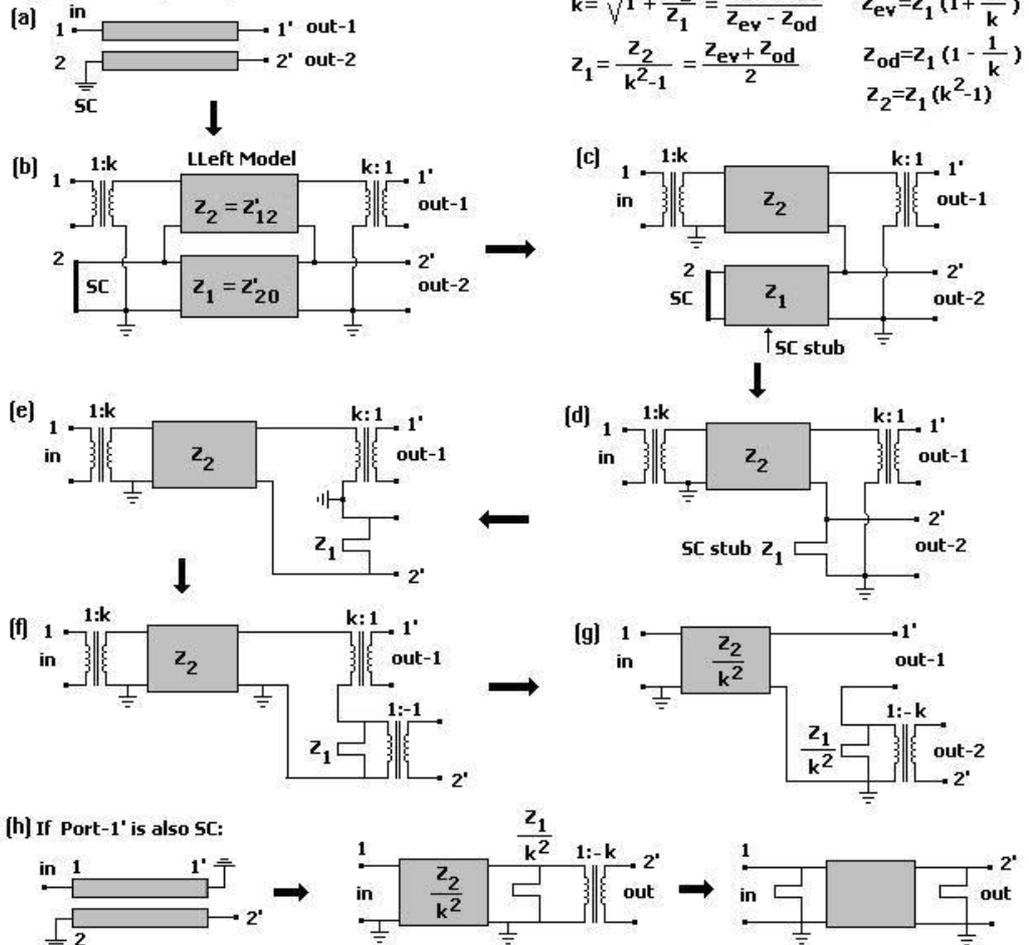
Figure 3. 8 Type-1 series diplexing PCL circuit
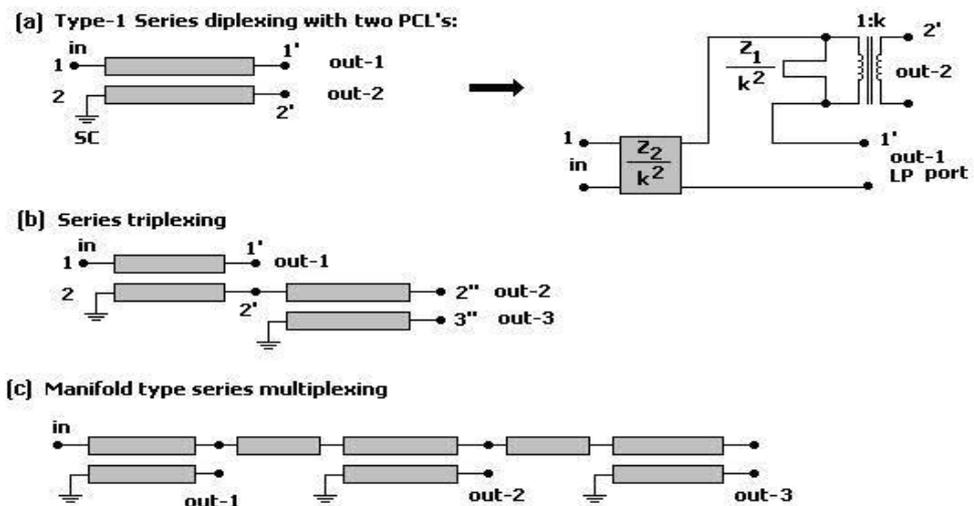
Figure 3. 9. Various possible series multiplexing circuits

50

b) Type-2 series diplexing with two parallel coupled lines:

 Figure 3.10.a shows an alternative series diplexing PCL with port-2' short circuited to ground. With input applied from port-1, the outputs will be taken from port-1' and port-2. Figure 3.10.b shows the equivalent L-Left circuit model. The SC at port-2' decouples the two lines giving the circuit of Figure 3.10.c. This SC converts the line 2-2' into a SC stub and the circuit can be redrawn as in Figure 3.10.d. The transformer 1:k at port-1 can be moved to the right ports, canceling the transformer k:1 at port-1' while introducing transformer 1:k at port-2 and the circuit can be redrawn as shown in Figure 3.10.e. Clearly port-1' and port-2 are in series. The shunt SC stub at port-2 enforces that a HP filter or BP filter must be placed in that port with the available SC stub and the transformer being part of that filter. There is no restriction on the type of the filter that will be placed at port-1'. For LP-HP diplexers we will name port-1' as LP port. This structure is named as Type-2 series diplexing PCL. The interrelations between the parameter sets Z_1-Z_2-k and Z_{ev}-Z_{od} of the PCL are also shown in the figure for convenience. In this circuit the transmission line ($Z2$) appears in port-1' only. Therefore once k-Z_1-Z_2 parameters of the diplexing PCL are set, then the first TL element of the filter to be connected at that port would also be set. This forms a constraint in the design of the channel filters. Therefore this series diplexing circuit seems to be less practical to use than Type-1 series diplexing.

51

(a) Type-2 Series diplexing with two PCL's:
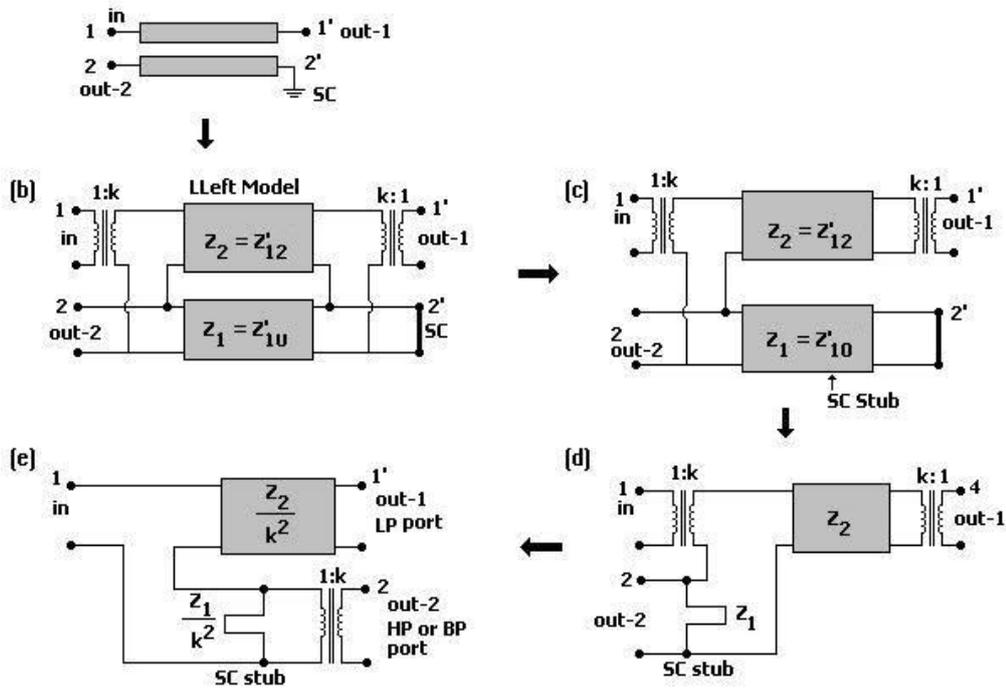
Figure 3. 10 Type-2 Series Diplexing Circuit

It is obvious that in a series diplexing PCL one of the ports should be shorted to ground. This applicable for narrow band multiplexers, because the coupling ratio allows the use of side coupled lines, whereas in wide or moderate bandwidth multiplexers the utilization of broadside coupled lines becomes necessary. Since it is impossible to make one end shorted to the ground while keeping the opposite end open, for moderate or wide bandwidth channel multiplexers can not use series diplexing. Therefore in those type of multiplexers parallel diplexing PCL's are used.

c) Type-1 parallel diplexing with two parallel coupled lines:

Figure 3.11.a shows a two parallel coupled line system with port-2 open circuited. Figure 3.11.b shows the equivalent L-Right circuit model. The OC at port-2 makes the transformer ineffective and decouples the two lines giving the circuit of Figure 3.11.c. Line 2-2' now becomes an OC stub and the circuit can be redrawn as shown in Figure 3.11.d. With input applied from port-1, the outputs will be taken from port-1' and port-2'. It is seen that the circuits connected to port-1' and port-2' will be in

parallel. The series OC stub at port-2' enforces that a HP filter or BP filter must be placed in that port with the available OC stub and transformer being part of that filter. There is no restriction on the type of the filter that will be placed at port-1'. In LP-HP type diplexers and multiplexers that port is used as LP port. This structure is named as Type-1 parallel diplexing PCL. The interrelations between the even-odd mode impedances and k-Z_1-Z_2 parameters are also shown in the figure for convenience. Figure 3.11.e shows the equivalent circuit when port-1' is also left OC. In this case the PCL section becomes an interdigital type OC PCL two port that is used in the classical distributed element HP filters.
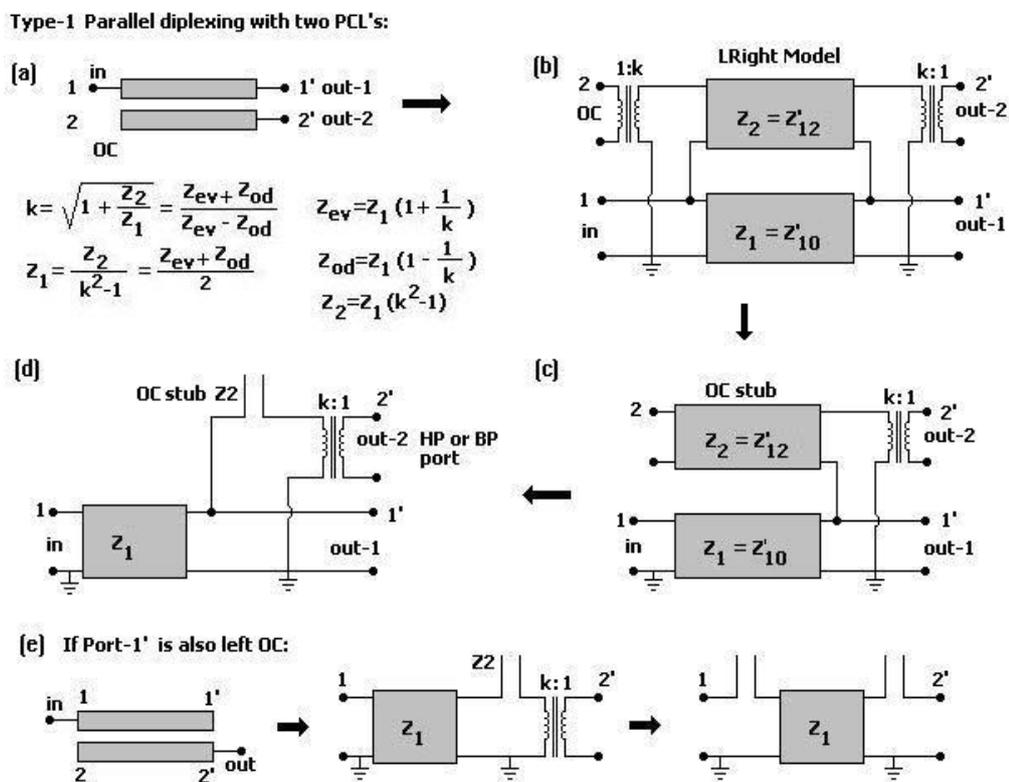
Figure 3. 11. Type-1 Parallel Diplexing Circuit

d) Type-2 parallel diplexing with two parallel coupled lines:

Figure 3.12 shows an alternative parallel diplexing circuit with two PCL's where now port-2' of the PCL is left OC. Figure 3.12.b shows the equivalent L-Right

circuit model. The OC at port-2' makes the transformer ineffective and decouples the two lines giving the circuit of Figure 3.12.c. Line 2-2' now becomes an OC stub and the circuit can be redrawn as shown in Figure 3.12.d. With input applied from port-1, the outputs will be taken from port-1' and port-2. The circuits to be connected to these ports will be in parallel. This three port is named as type-2 parallel diplexing PCL. The series OC stub at port-2 enforces that a HP filter or BP filter must be placed in that port with the available OC stub and the transformer being part of that filter. There is no restriction on the type of the filter that will be placed at port-1' except that its first element must be a transmission line with impedance Z_1. However since Z_1, Z_2 and k are interrelated, in designing and modifying the filter at port-2 we should also consider the impedance of the transmission line at port-1'. This fact actually forms a constraint. Therefore it seems that this parallel diplexing is less practical to use than Type-1 parallel diplexing PCL.
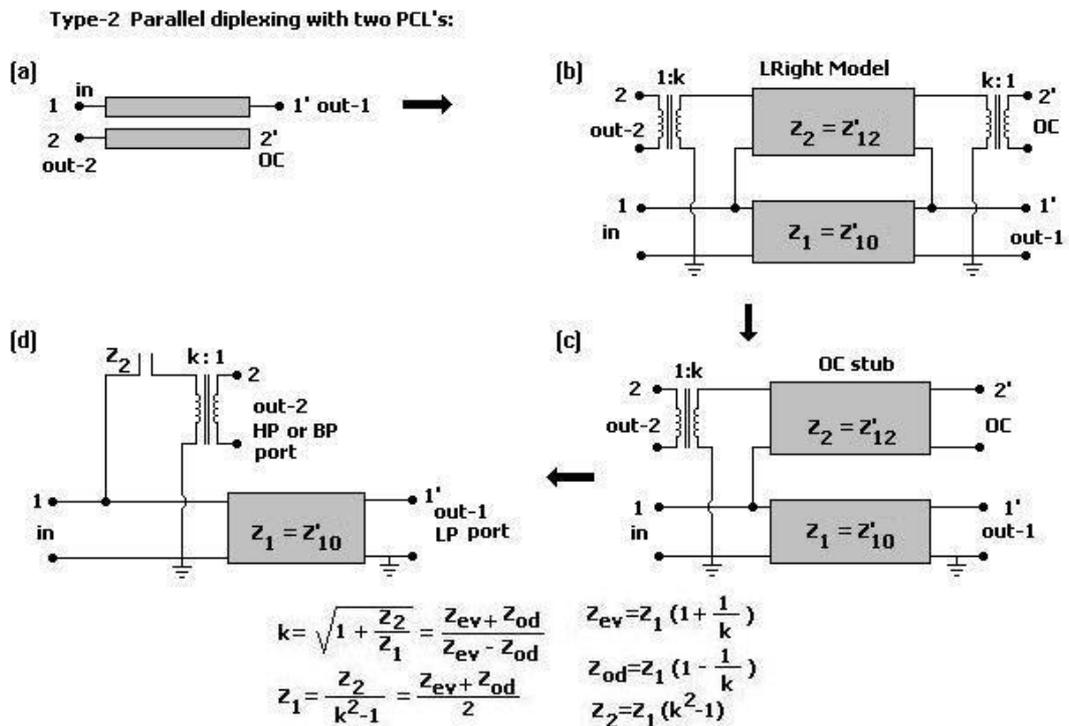
Figure 3. 12 Type-2 Parallel Diplexing Circuit

Traditional diplexers use T-junctions as their diplexing ends. In the following section a comparison between T-junction diplexing and OCPCL diplexing will be made. First these structures will be compared in return loss aspect.

3.3. Comparison of Return Loss Performances of PCL and T-Junction Diplexing

In this section the use of OCPCL (open circuited parallel coupled line) in diplexers is investigated. It will be shown that if an OCPCL is used as diplexing element, the return loss of the diplexer especially at low frequencies is (down to DC) is much lower than the case when Tee-Junction diplexing is used. It will be shown that OCPCL can be used with any type of highpass filters whereas if Tee-Junction diplexing is to be used there should be at least one coupled line (before the short circuited stubs) in the highpass section in order to eliminate the loading effect from the low-pass channel at lower frequencies. Let us begin with a simple example by designing the highpass and lowpass channels seperately.

Design of the low-pass channel:

The channel filters are synthesized using the software Filpro. Therefore the terminology and circuit element symbols of Filpro are used whenever applicable. The corner frequency (fp) is taken as 4 GHz. The quarter wavelength frequency (fq) is 8 GHz and passband ripple is taken as 0.01 dB. A degree six singly terminated LPF will be designed with 3 contributing Unit Elements (UE's) and 3 transmission zeros (TZ's) at infinity. The circuit is then synthesized by extracting the transmission zeros in the order inf-UE- inf-UE- inf-UE giving the filter of Figure 3.13.
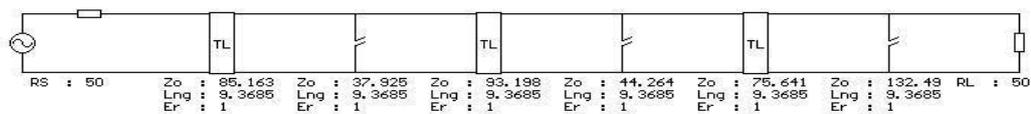
Figure 3. 13 . LP channel Filter Schematics

55

Design of the high-pass channel:

T-Junction diplexing:

The corner frequency (f_p) is taken as 4 GHz , The quarter wavelength frequency (fq) is 8 GHz and ripple is taken as 0.01 dB. HP will be designed with 6 contributing UE's and transmizzion zero at f=0. The elements are extracted in the order UE-UE-UE-zero-UE-UE-UE giving the circuit shown in Figure 3.14.
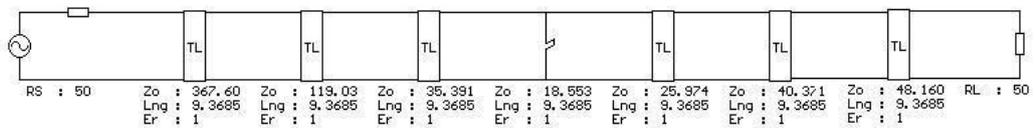
Figure 3. 14 . HP channel Filter Schematics

Formation of the diplexer with Tee Junction:

The circuit for HP channel is repeated in Figure 3.15.a. In Figure 3.15.b a transformer is inserted to be used for tuning together with the LP channel. Next in Figure 3.15.c the LP channel is connected in parallel with HP channel to form a diplexer with Tee type junction. In Figure 3.15.d the HP channel is tuned for maximum return loss up to 8 GHz. The tuned circuit is given in Figure 3.15.e. The return loss for the tuned and untuned circuits are given in Figure 3.16.

56
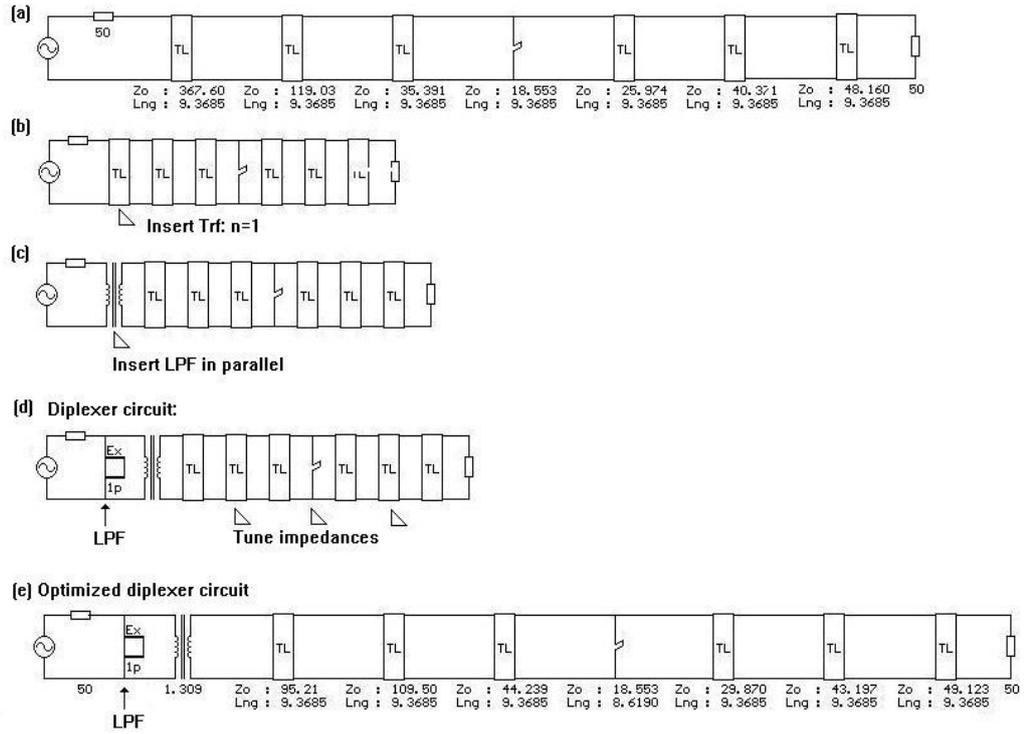
Figure 3. 15 Formation of the Diplexer with T-junction
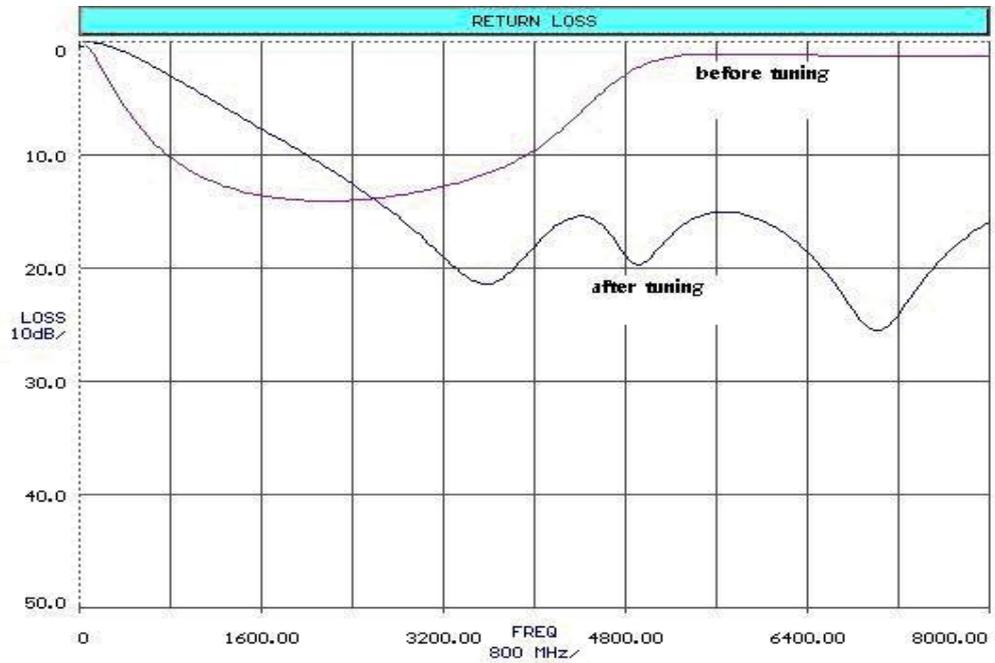
Figure 3. 16 . Return Loss of the diplexer with t-Junction before and after tuning

OCPCL diplexing:

The design for high-pass channel is performed on Filpro and given in Figure 3.17. The corner frequency (f_p) is taken as 4 GHz , The quarter wavelength frequency (fq) is 8 GHz and ripple is taken as 0.01 dB. HP will be designed with 6 contributing UE's and 2 transmission zeros at f=0. The extra TZ at f=0 will be used in the formation of the diplexing PCL. The Transmission zeros can be extracted in different orders giving different diplexer topologies after insertion of the LPF as shown in Figure 3.17. The LPF is the same as in the previous design.
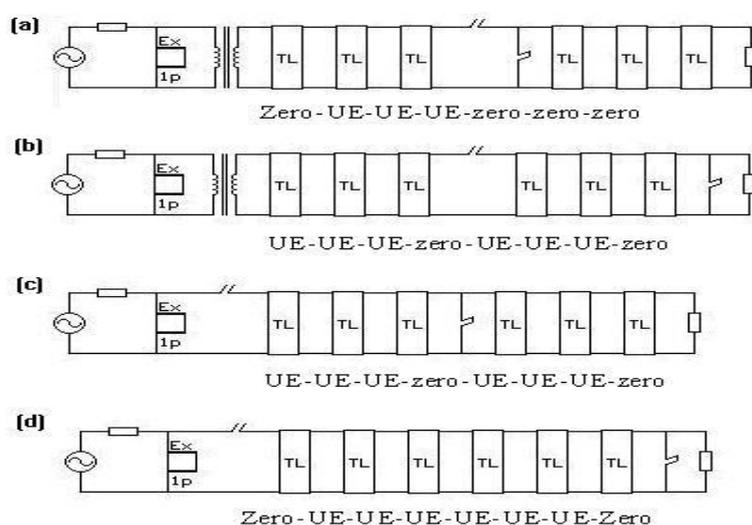
Figure 3. 17 Four different forms of extraction for HP channel Option-2

Upon extraction we have two observations:

The first point is the improvement of the return loss at low frequency region. In the former case the return loss at lower frequencies was severely affected when the diplexer has been formed, but in this case it is almost unaffected near DC. This is due to the isolating effect of the open circuited stub. In the previous case both channels loaded each other and namely the short circuited stub has caused degradations in LP channel at lower frequencies. The second point is that [comparing Figures 3.17.a, b and c] as the open circuited stub is extracted closer to the diplexing end the return loss gets better in low frequency range. Hence we can deduce that if the open

58

circuited stub is extracted in the diplexing end, return loss would be much more easily tuned for all frequencies including DC. This is demonstrated in Figure 3.18. Further, comparing Figure 3.17.c and Figure 3.17.d it is seen that when the OC stub is extracted at the diplexing end, the location of the short circuited stub will have no importance, because the open circuited stub serves as an isolator for channels, especially near DC, whereas for Figure 3.17.a and Figure 3.17.b, it is seen that moving the short circuited stub to the load side we get a better return loss due to the fact that the further the short circuited stub, the less the LP channel is loaded.
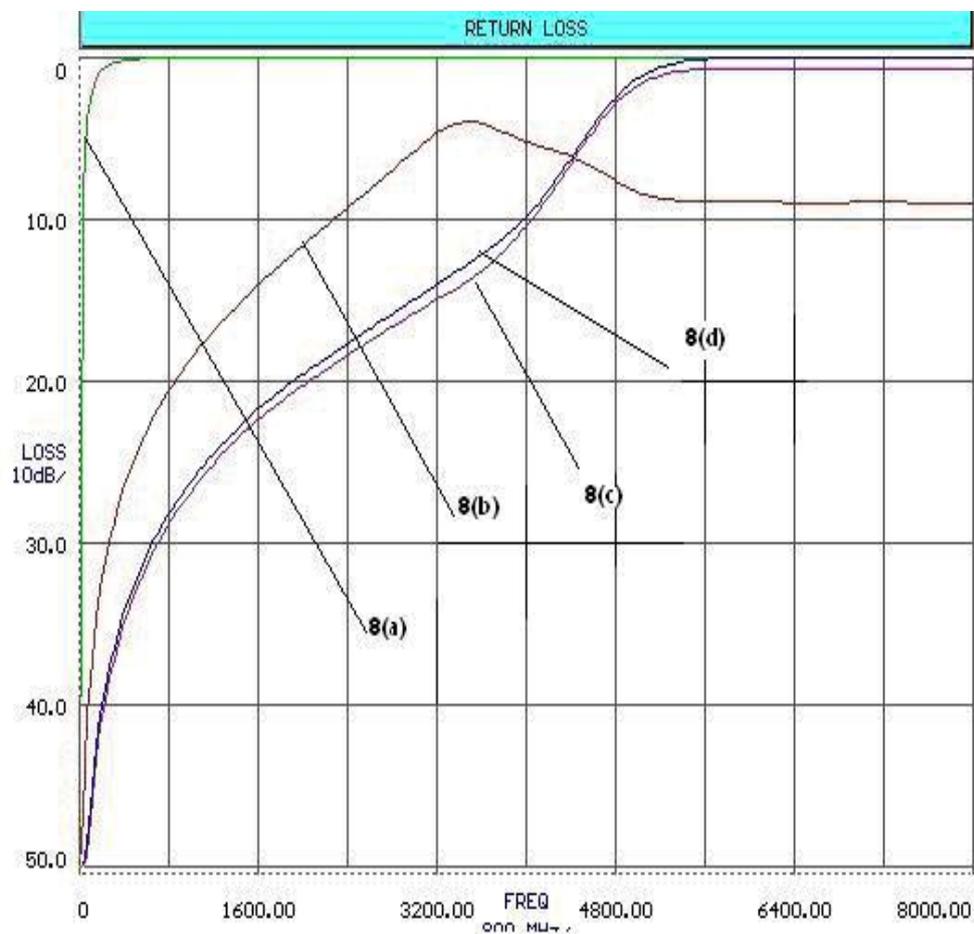
Figure 3. 18 Comparison of different extraction schemes for Option-2

All four schemes can be tuned as in the case for T-Junction.

59

In Figure 3.19, the steps in the formation of OCPCL diplexing three port are presented and the final circuit for HP channel option-2 is given.
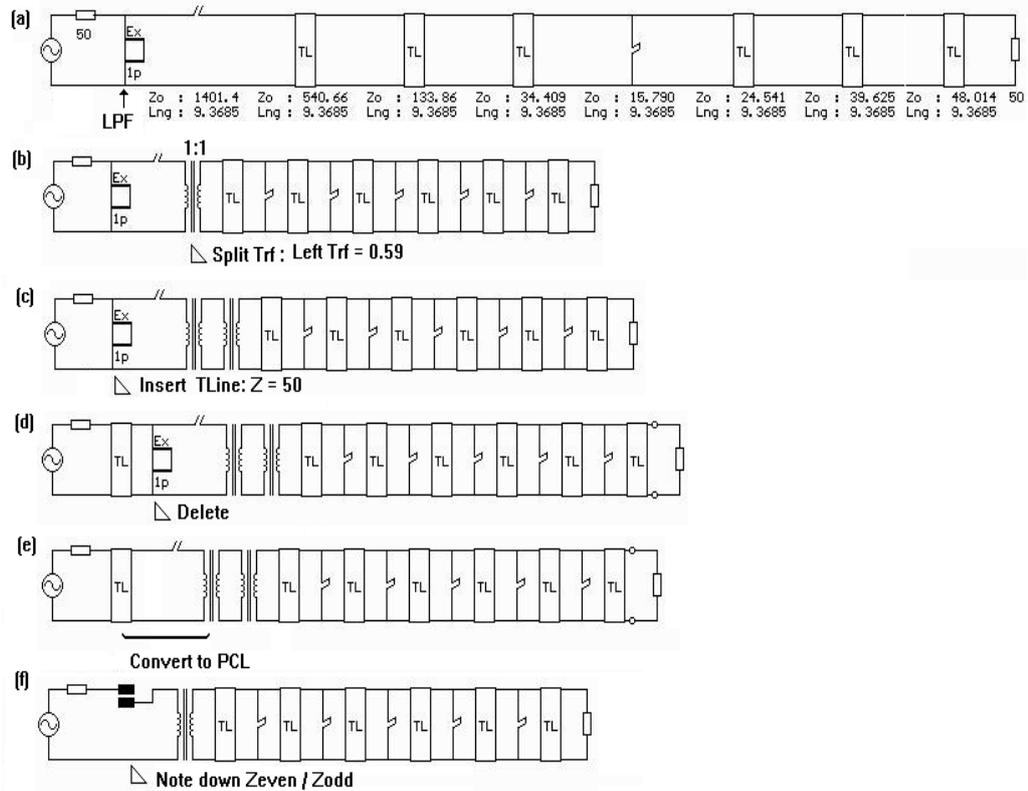
Figure 3. 19. Formation of HP channel for Option-2

The circuit in Figure 3.17.c is repeated in Figure 3.19.a. Then the short circuited stub in the middle is distributed in between the UE's using Kuroda transformations. The resultant circuit is shown in Figure 3.19.b. The transformer has been moved left and spitted in two parts. As the left portion is to be used for building OCPCL, it is specified along procedure given below.

$$k = \sqrt{1 + \frac{Z_2}{Z_1}} = \sqrt{1 + \frac{92.9}{50}} = 1.69$$

(3.3.1)

Since Z2 =92.9 and we set Z1 =50   Hence we should set the transformer. Then we should get the even and odd impedances as:

$$Z_{ev} = Z_1(1+\frac{1}{k}) = 50(1+\frac{1}{1.69}) = 79.5$$

$$Z_{0dd} = Z_1(1-\frac{1}{k}) = 50(1-\frac{1}{1.69}) = 20.5$$

$$(2.3.2)$$

In Figure 3.19.c we add a 50 ohm transmission line to use it as Z1 and we distribute the series open circuited stub on the left of the line in Figure 3.19.d and e. Finally in Figure 3.19.f we get the OCPCL with Zeven=79.5 ohm and Zodd=20.5 ohms, which complies with the results we obtained in (3.3.1) and (3.3.2). Return loss of the diplexer is given in Figure 3.20. The element values for the final circuit is shown in Figure 3.21.

Figure 3. 20 . Return loss for HP channel Option-2
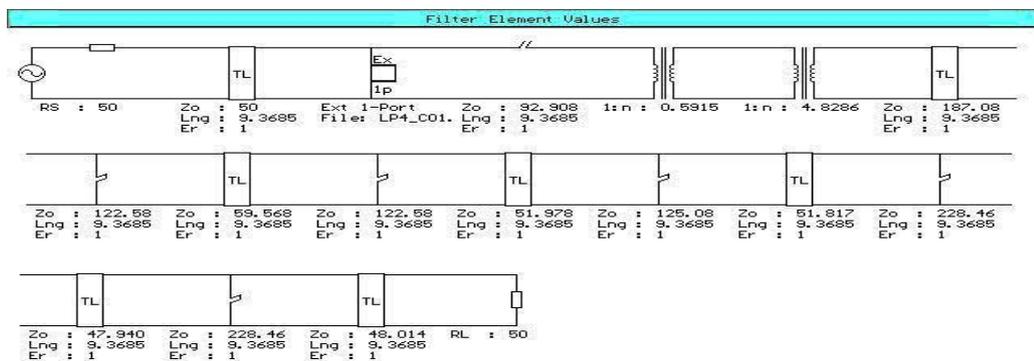
Figure 3. 21 . Final HP channel schematics for Option-2

61

3.4. Comparison of Isolation performances of PCL and T-Junction Diplexing

In the previous section the circuits are optimized for the best return loss without considering the isolation of channels. Now we will optimize the circuits to get best isolation (stopband attenuation levels) by keeping return loss at about 20 dB. It will be shown that if PCL diplexing is used, the rejection of the diplexer is higher than the case when Tee-Junction diplexing is used. It will also be shown that the use of PCL diplexing adds another degree of freedom to the structure and can be used in optimization whereas Tee-Junction diplexing lacks this freedom. The validity of the claim will be demonstrated through example diplexer designs. Another issue to be pointed out is the comparison of singly and doubly terminated design approaches. It will be seen that using singly terminated filters will lead to unrealizable element values and transformers in the circuits which need to be eliminated through transformation and optimization. In the end it will be shown that the singly terminated filters will converge to doubly terminated filters since doubly terminated filters are globally optimum.

Let us design a diplexer with cross-over frequency at 4 GHz, the diplexer is aimed to have a return loss of 21 dB up to 8 GHz and, the highpass channel must have a rejection of 50 dBc at 3 GHz and the lowpass channel must have a rejection of 50 dBc at 5 GHz. In order to achieve the above specifications we will design two diplexers first by Tee-Junction diplexing, then by PCL diplexing. We will design and make coarse optimizations of diplexers in FILPRO, then we will optimize the circuits in ADS. Just as a demonstration let's begin with a simple example by designing the HP and LP channels separately and then combining them to form diplexers.

Design of the low-pass channel:
The corner frequency (fp) is taken as 4 GHz. The quarter wavelength frequency (fq) is 8 GHz and ripple is taken as 0.01 dB. LPF will be designed with 6 contributing UE's and 6 TZ's at f= ∞. The circuit is synthesized as singly terminated one. The

TZ's are extracted as inf-UE- inf-UE- inf-UE- inf-UE- inf-UE- inf-UE giving circuit of Figure 3.22. This LPF will be used in both T-junction and PCL diplexing.
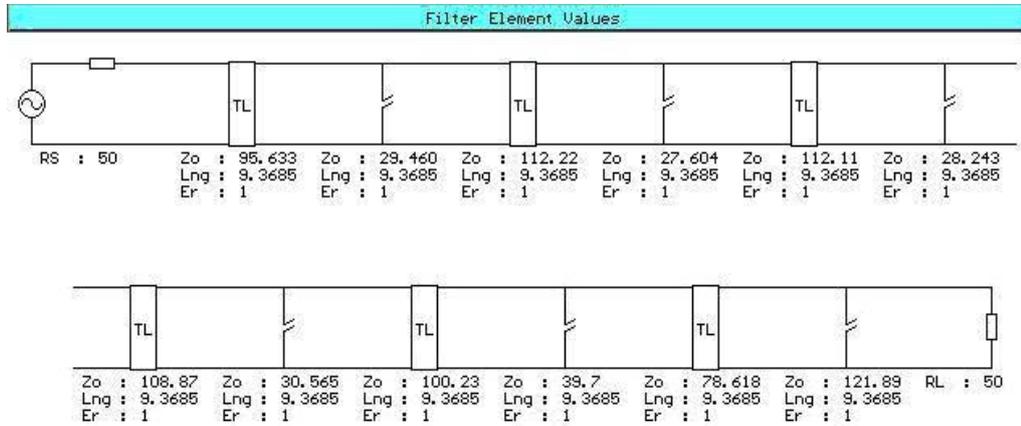
Figure 3. 22 LP channel schematics

Design of the high-pass channel:

T-Junction diplexing:

The corner frequency (fp) is taken as 4 GHz , The quarter wavelength frequency (fq) is 20 GHz and ripple is taken as 0.01 dB. HP will be designed with 4 contributing UE's and 8 TZ's at f = 0. The filter is synthesized as a singly terminated one. The TZ's are extracted in the order Zero-UE-Zero-Zero-UE-Zero-Zero-UE-Zero-Zero-UE-Zero, giving the circuit of Figure 3.23.
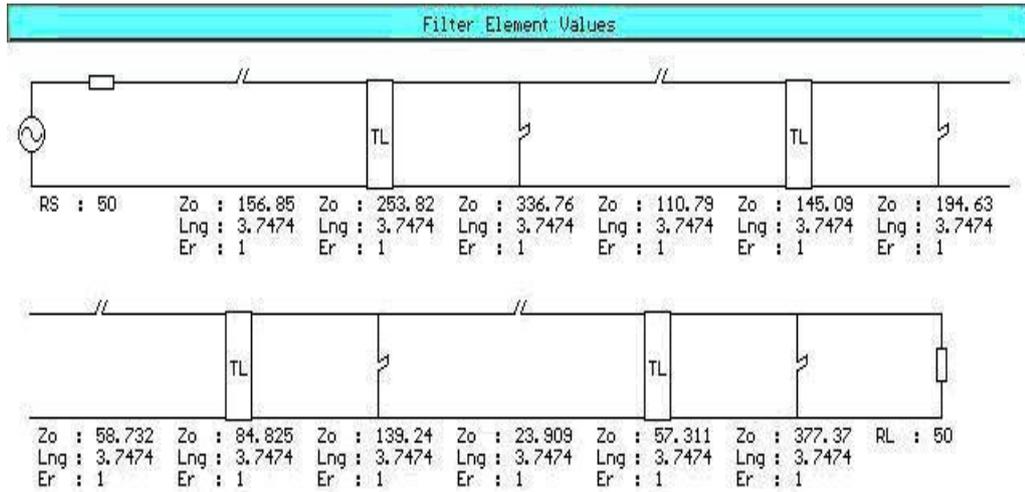
Figure 3. 23. HP channel schematics after the extraction of TZ's
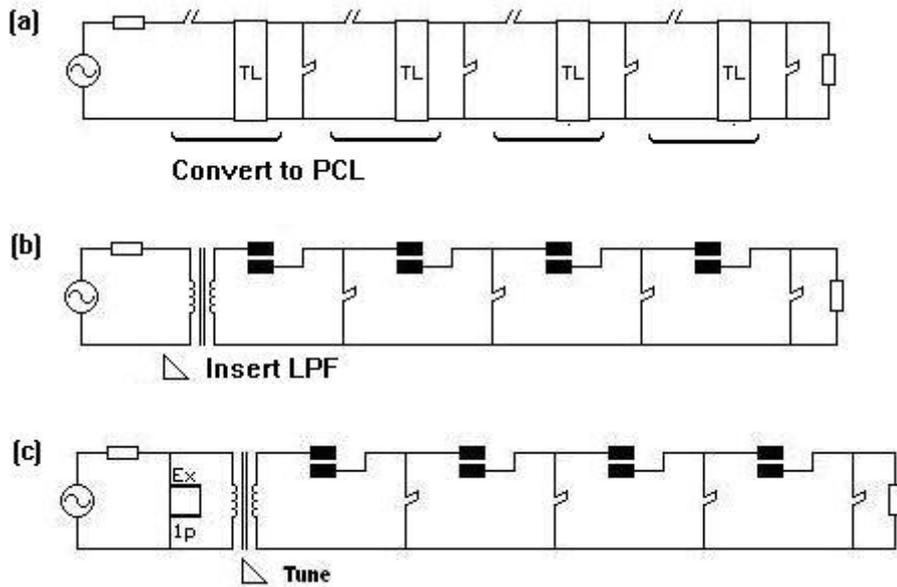
Figure 3. 24 Design steps for HP channel and diplexer
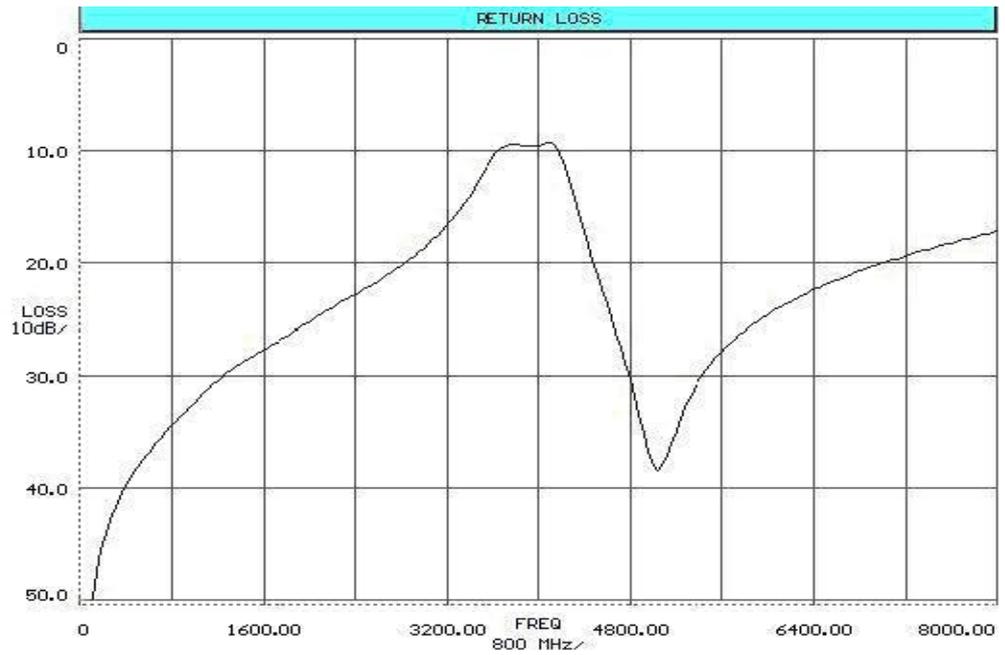
Figure 3. 25. Diplexer return loss after tuning transformer in HP channel

It should be noted that the impedance of the last shunt short circuited stub in the circuit in Figure 3.26 has an impedance of 377 Ohms which is unrealizable. This is due to using singly terminated design approach. This issue will be covered in the next section where diplexer is to be optimized in ADS. The circuit is repeated in ADS for convenience in Figure 3.26 and corresponding plots for the diplexer are shown in Figure 3.27.
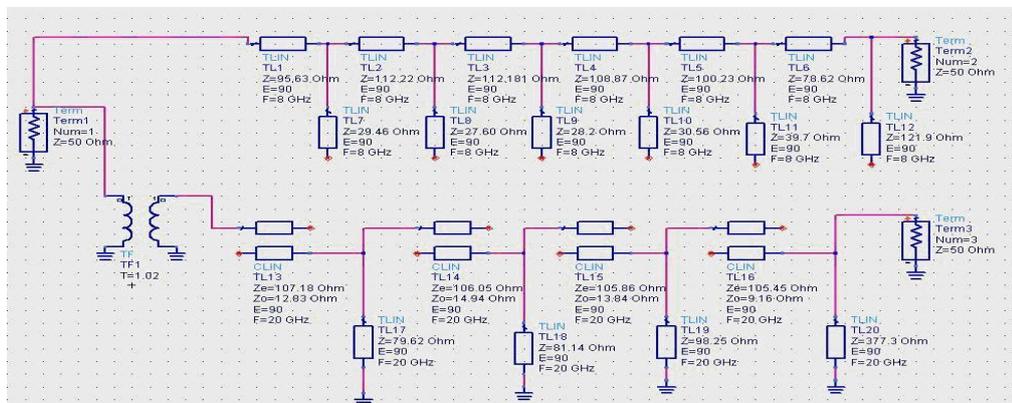
Figure 3. 26. HP channel schematics after the extraction of TZ's

65

Figure 3. 27 HP channel schematics after the extraction of TZ's
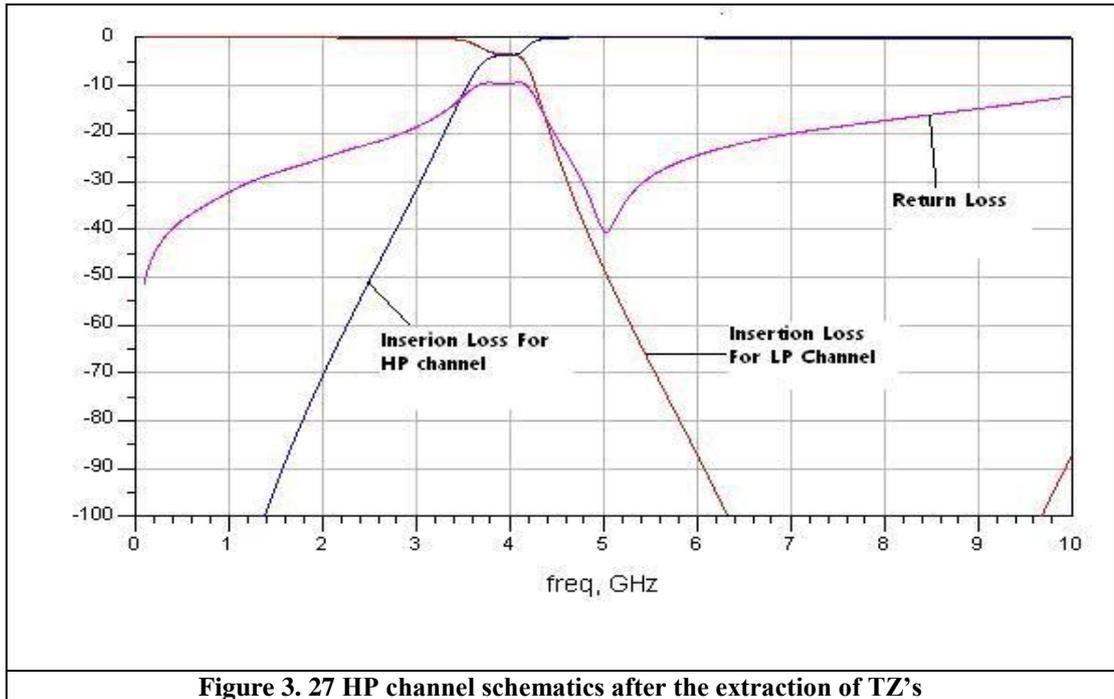
After 50 trials of optimization, the diplexer has return loss of 20 dB up to 8 GHz and, the highpass channel has a rejection greater than 50 dBc at 3 GHz and the lowpass channel has a rejection greater than 50 dBc at 5 GHz. In order to reach the 21 dB return loss goal the circuit has to be optimized several times more. The optimized circuit and its responses are given in Figures 3.27 and 3.28 respectively.

Figure 3. 28 Diplexer after optimization in ADS

66
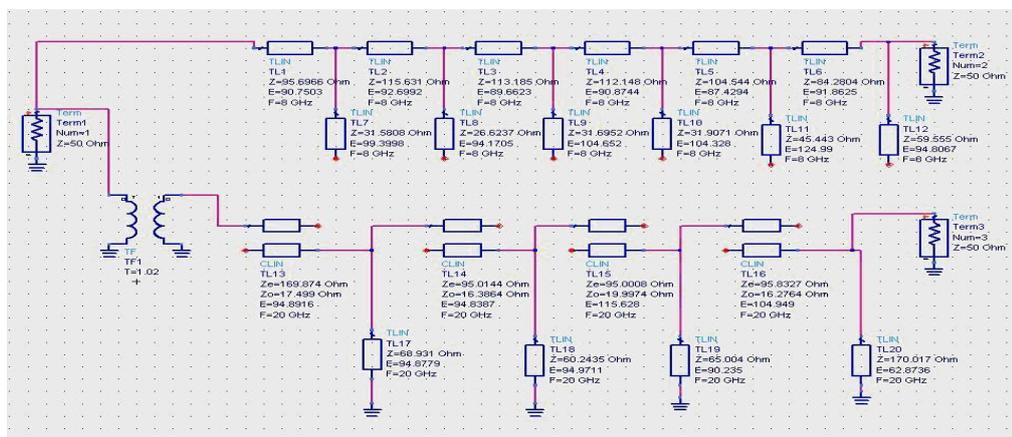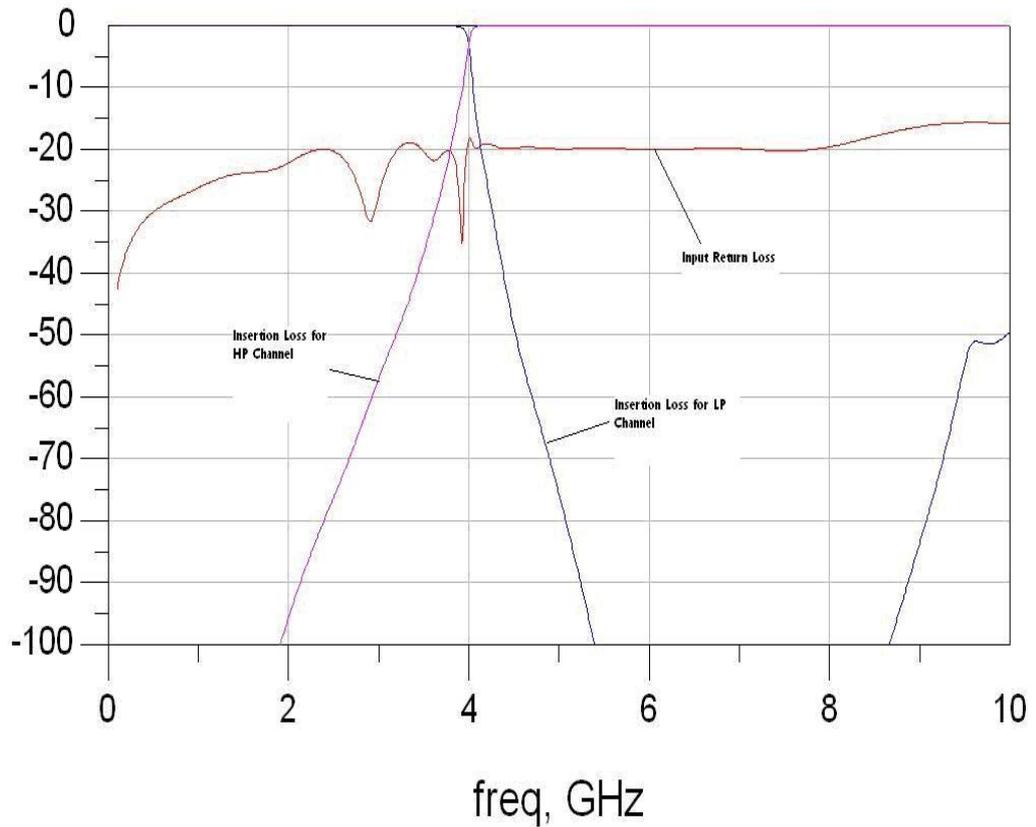
Figure 3. 29. Diplexer response after optimization in ADS

We note that the impedance of the last stub has changed from 377 ohms to 170 ohms after 50 trials. Further experimentation with both singly and doubly terminated HP filters had shown that they converge to close values with doubly terminated approach converging faster. Therefore in later designs doubly terminated approach is preferred.

Design of the high-pass filter for PCL diplexing:

The corner frequency (fp) is taken as 4 GHz. The quarter wavelength frequency (fq) is 20 GHz and ripple is taken as 0.01 dB. HP will be designed with 4 contributing UE's and 8 TZ's at f=0. TZ's are extracted in the order Zero-UE-Zero-Zero-UE-Zero-Zero- UE-Zero-Zero- UE-Zero giving the circuit in Figure 3.30.
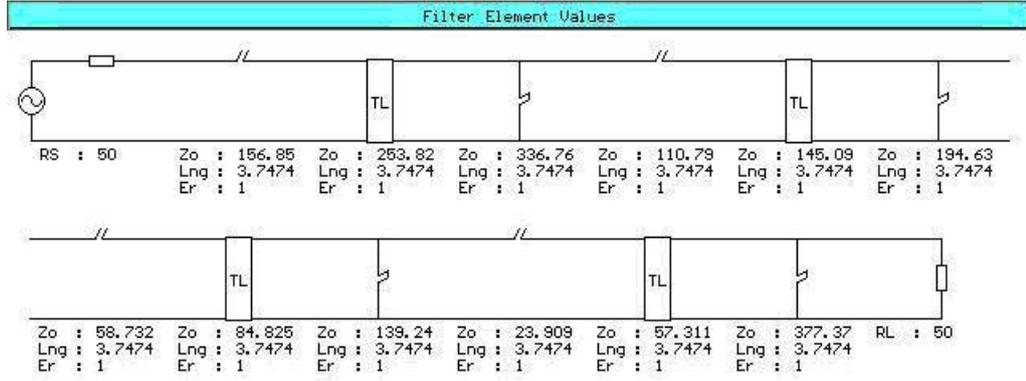
Figure 3. 30. HP channel after extraction

Next we convert the highpass channel into a realizable PCL form. This is done by distributing the series OC stubs onto the two sides of the adjacent UE's as shown in Figure 3.31.a-b. Then the first stub on the left is split into two equal pieces in order to form the diplexing PCL section later. Next the stub-UE-Stub triplets are converted into PCL sections with the resultant transformer being at the leftmost position as shown in Figure 3.31.c-d. Then a 50 0hm transmission line is added and the LPF is inserted to form the diplexer circuit (Figure 3.31.e). The inserted transmission line is needed in the formation of the transmission line-stub-transformer triplet which is the equivalent circuit of diplexing PCL as shown in Figure 3.31.e. The transformer need be tuned to form the desired PCL section as shown in equations 3.1.29 and 3.1.30 as follows:

The circuit model of a PCL involves the three parameters, Z_1, Z_2 and k as described in Figure 3.12. Now in the leftmost section of the diplexer circuit of Figure 2.30.e we have Z_1=50 ohms as the transmission line impedance. Z_2 is the series OC stub impedance and it is the splitted half of the first stub which is $Z_2 = 78.52$ ohms. So, the transformer turns ratio needed to complete the equivalent circuit of diplexing PCL will be

$$k = \sqrt{1 + \frac{Z_2}{Z_1}} = \sqrt{1 + \frac{78.42}{50}} = 1.6$$

68

Hence we should set the transformer in FILPRO to n=1/k = 0.625. Thus we get the even and odd impedances of the diplexing PCL as:

$$Z_{ev} = Z_1(1+\frac{1}{k}) = 50(1+\frac{1}{1.6}) = 81.2$$

$$Z_{0dd} = Z_1(1-\frac{1}{k}) = 50(1-\frac{1}{1.6}) = 18.9 \quad \text{(Ohms)}$$

The next stage is to optimize the whole diplexer in ADS. The circuit before optimization is given in figure 3.32.
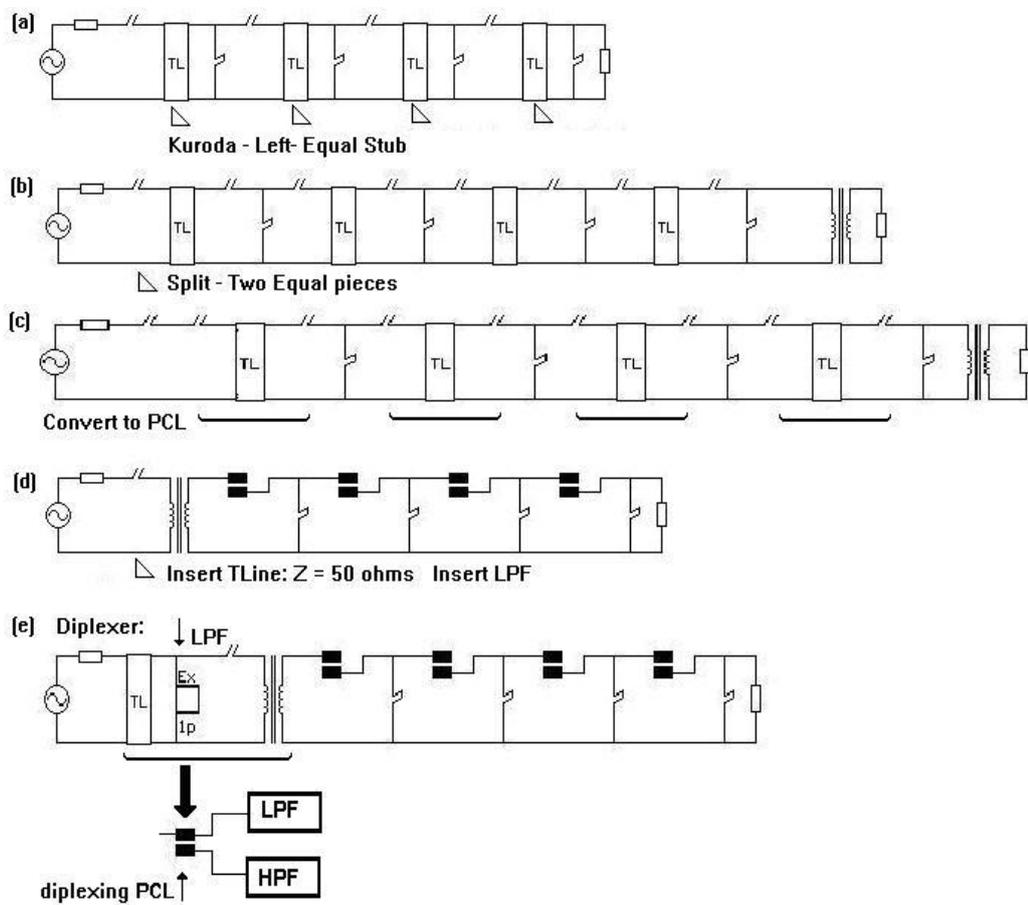
Figure 3. 31. Formation of the Diplexer
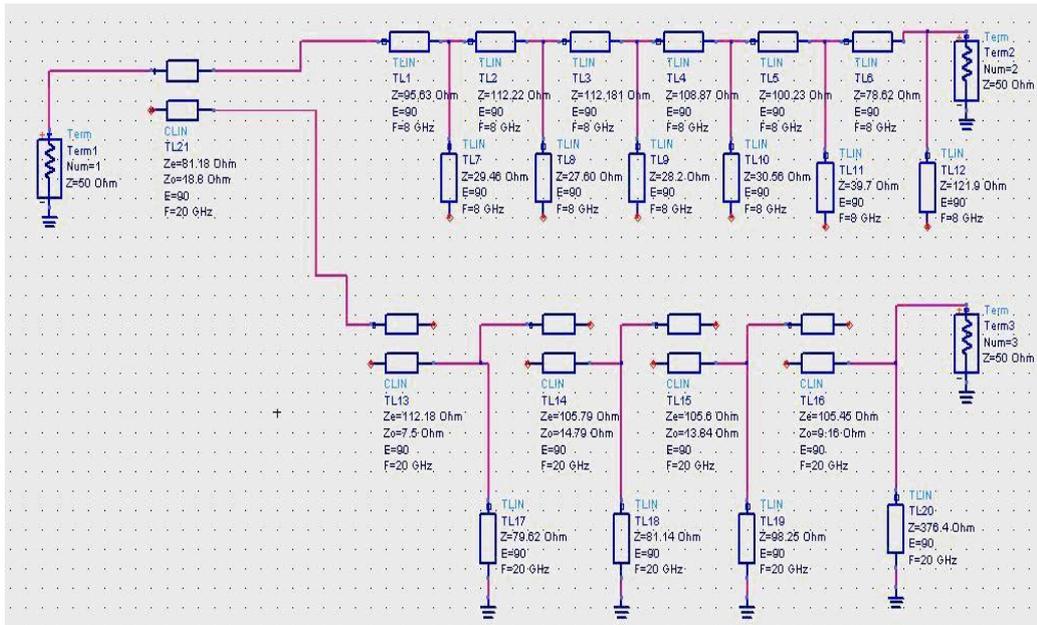
Figure 3. 32. Diplexer before optimization

The circuit schematics and the response after optimization is given in Figure 3.33 and 3.34 respectively.
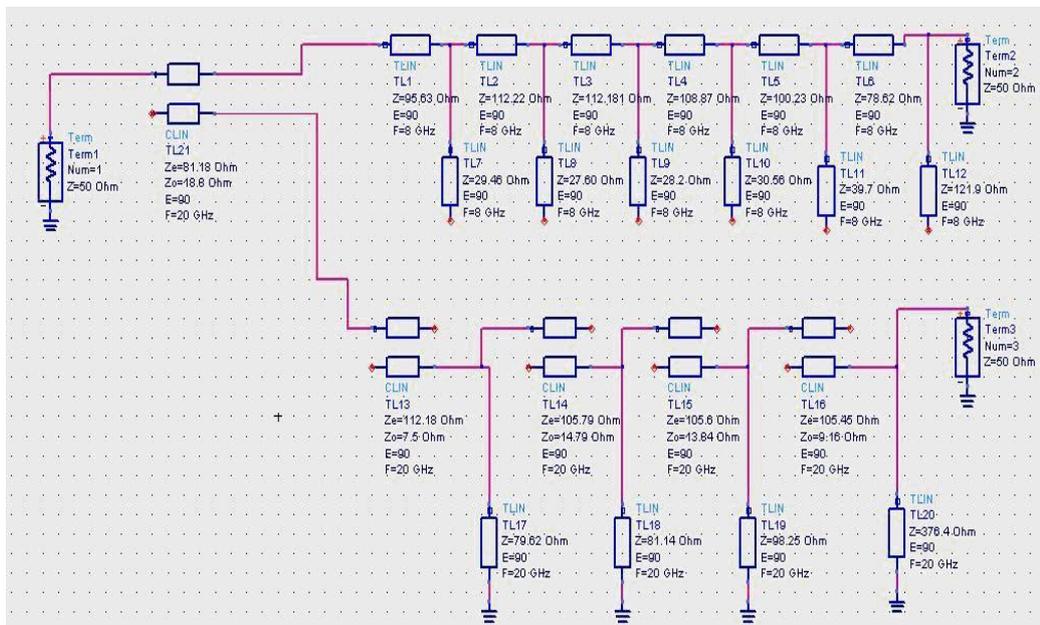
Figure 3. 33. Diplexer after optimization

70
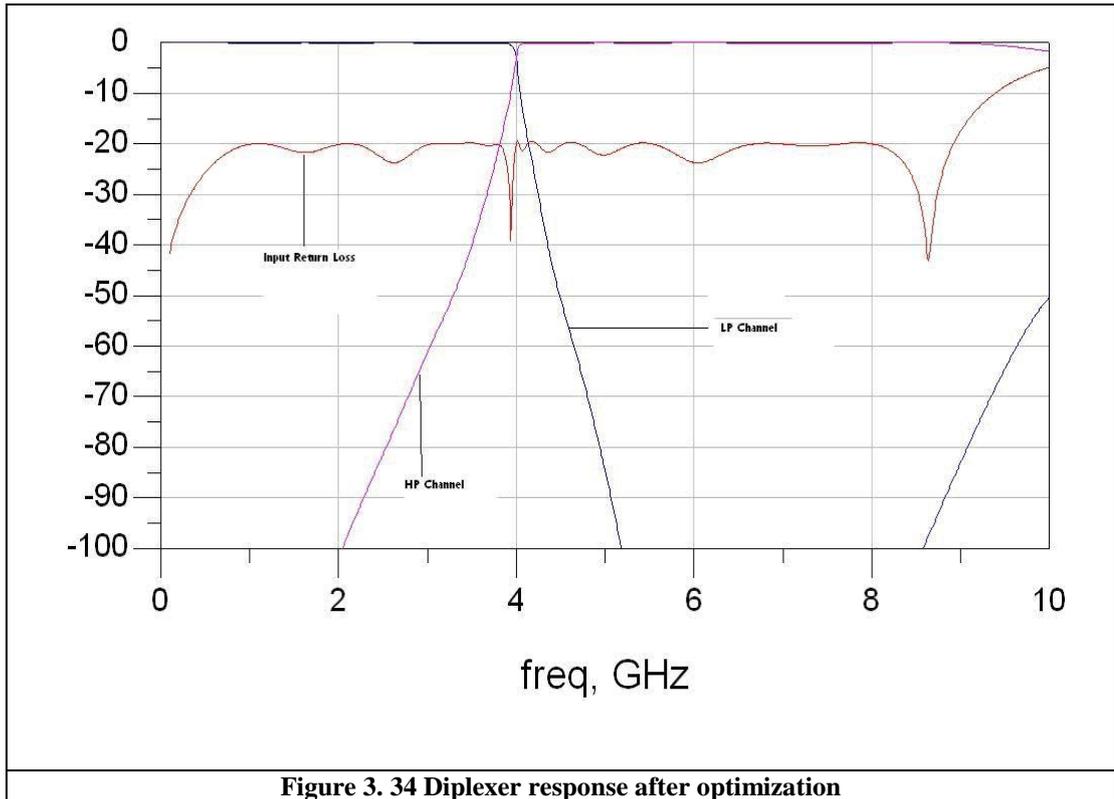
Figure 3. 34 Diplexer response after optimization

Next we are going to compare the insertion and return loss responses of two diplexers (Option-1 and Option-2). The responses are given in figure 3.35.

71
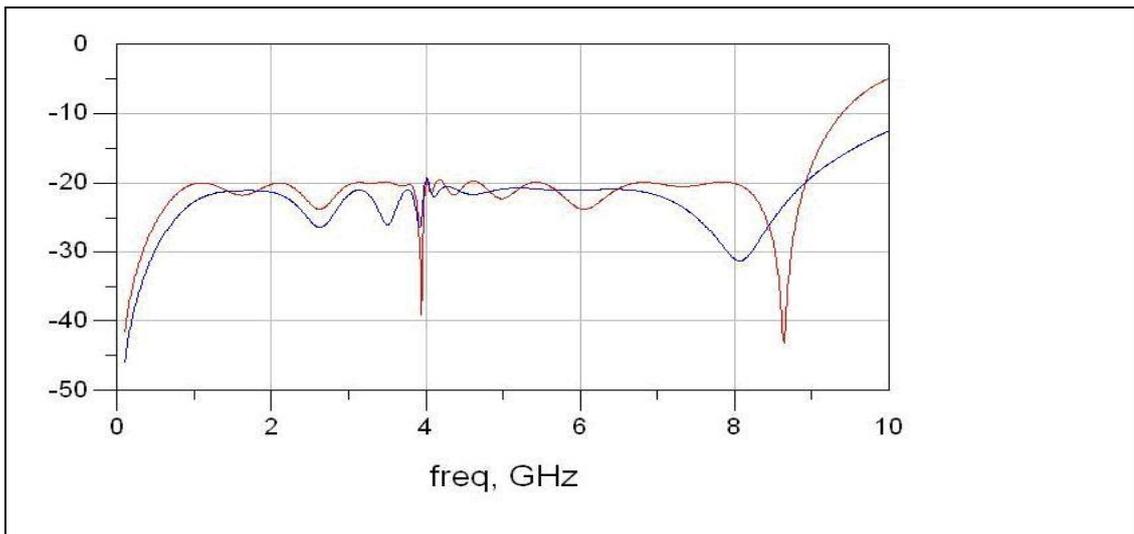
(a)
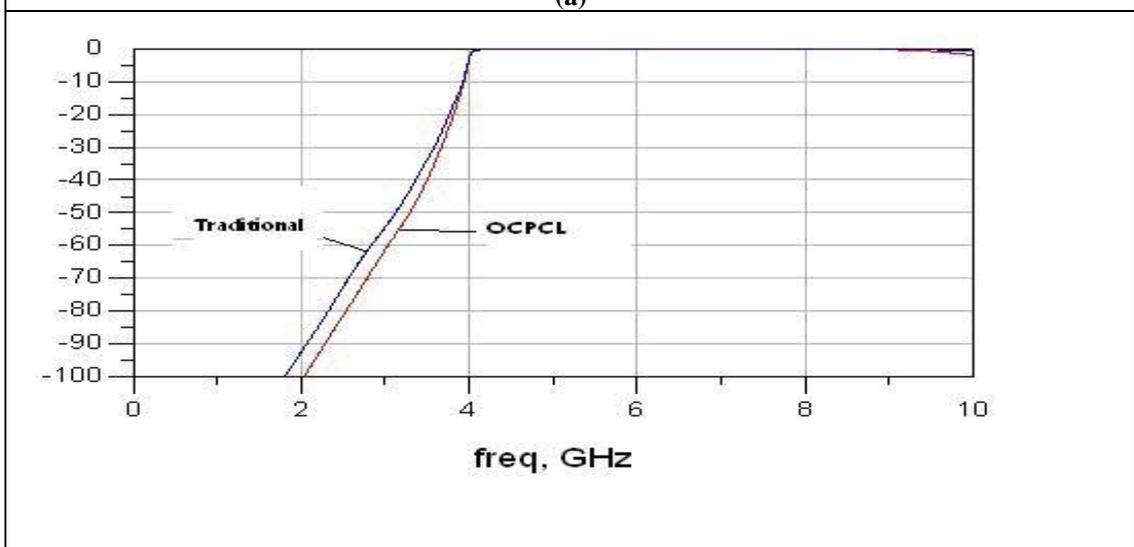
(b)
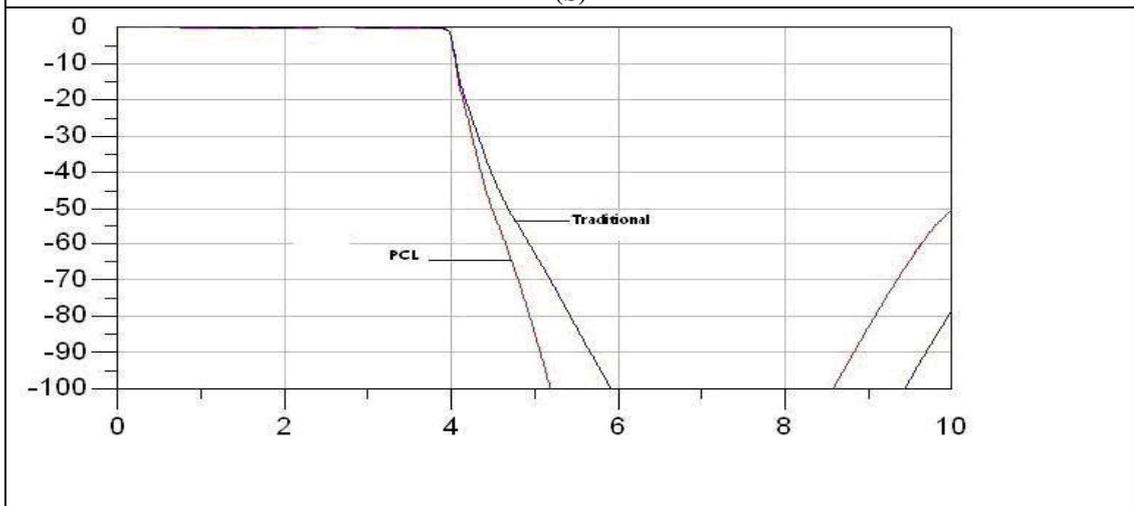
(c)

Figure 3. 35 a) Return Loss for T-junction (blue) and PCL (red). b) Insertion Loss of HP Channel with T-junction (blue) and PCL (red). c) Insertion Loss of LP Channel with T-junction (blue) and PCL (red).

From figure 3.35 we deduce that for approximately the same return loss (about 20 dB) the rejection both in HP channel and LP channel are better in PCL diplexing case. This is due to the fact that the diplexing PCL serves as another degree of freedom in the optimizations, contributing to all responses. The isolation between HP and LP channels is also better in this type of diplexing with a sharper insertion loss response.The design approaches described in this chapter for the LP, HP and PCL diplexing three ports are used in the succeeding chapters in the same manner, with slight modifications, like increased orders in some channels. Therefore the design details will not be repeated to keep the thesis compact.

CHAPTER 4

EM MODELING OF DIPLEXERS

4.1   Why Do We Need EM Modelling?

In chapter 1 various SW_MUX topologies were introduced as a preface. At the end of chapter 1, the proposed topology was described in a system point of view. As it has been already noted, the main blocks were diplexers, power divider and band limiting filters that is; 2 HP and 18 LP. It is required that the circuits and the EM structures should be introduced briefly.

In chapter 2, design methods are defined for diplexers. However there is along way between the measured diplexer and the theoretical design. An attempt for directly realizing a computer design will always be condemned to failure. Usually the electromagnetic simulation fills the gap between the computer circuit and the real life diplexer. This type of simulators can be developed in house for specific applications or commercial 2-D or 3-D simulators such as SONNET ,HFSS, CST etc. can be used. As a matter of fact before 1990's these type of simulators had limited area of usage because of their need for very powerful machines considered for their age. In the 1990′s electromagnetic simulation has found a vast area of usage. Long calculation times were needed for multi-resonator filters, because the price of EM simulation of sharp filter structures is either computation time or hardware resource. However, together with the increase in CPU speed and by invention of new numerical methods, EM simulation began to play a key role in filter design and has reduced experimental design work for distributed element filters. Therefore, the need for having a production facility next to the filter lab is certainly no an apriori condition. Either the structure is metallic resonator filter (like coaxial TEM-mode resonators or waveguide cavity resonators or suspended substrate) or dielectric

resonators, electromagnetic simulators like HFSS, CST provides almost all information on:

- their n-port behavior in terms of S-parameters
- their resonance frequencies
- their internal electromagnetic field distribution
- their surface currents and surface losses
- their dielectric and metallic losses
- their stored energy and quality factor

In many ways, 3D EM simulation is like a 'real measurement' for the designer of passive rf & microwave filters. The accuracy of 3D EM simulation is very high, which allows reaching to the final design with minimum number of design iterations. Why is EM simulation so realiable ? The answer is quite simple: the operation dictates the calculation of the electromagnetic fields within the filter structure. It does not use 'equivalence' as in closed formulatons, but solves the actual fields. The instant access to the field data provides a variety of analysis possibilities that are not possible in an experimental approach. However the user must be skilled enough to exploit the the maximum capacity of the design tool. Such exploitation should involve commenting of the analysis data. Indeed, EM simulation creates huge files of field data. If it is just used to plot S-parameters, then the tool is certainly not used successfully enough. Since the use of EM analysis is mentioned, the EM modeling of diplexers should be continued.

The diplexers were in LP-HP form. As every HP channel should span a bandwidth of at least 4 GHz, and the rejection is desired to be more than 50 dBc at center frequency of the adjacent channel, the use of edge coupled lines with stubs (serving as finite transmission zeros) is essential due to problems in practical realization of the circuitry. The LP channel will consist of unit elements and stubs of different lengths (90 and 180 degrees). LP channel can easily be modelled and realized beause of the simplicity of its EM structure. However, there are some elagant realization techniques for very low impedance stubs, but this is out of the scope of this thesis.

It is the HP channel that will dictate the EM structure (microstrip, stripline, suspended stripline etc.) of the circuit. In chapter 2 it is seen that edge coupled lines with stubs may require broadside coupled lines. This fact limits the EM structure into two choices stripline or suspended stripline. For the ease of production and tuning suspened stripline will be used. For the sake of the argument and HP filter at 14 GHz will be designed and simulated step by step. This procedure will be repeated while designing the HP channels for the diplexers throughout the thesis.

4.2. Design of 14 GHz Highpass Filter

The design steps will not e given as detailed as given in chapter 2. A Hp filter at 14 GHz with the specifications below is designed in FILPRO. Band edge frequency: 14 GHz, Cut off frequency: 26 GHz , Passband ripple: 0.01 dB, rejection at 13 GHz: 60 dBc. The filter will be in the form of Generalized Chebyshev-3 as given in Figure 4.1a. The open circuits are replaced by series LC resonators. Inductors in the resonators are splitted into two equal pieces and they are replaced by transmission lines as given in Figure 4.1.b. The resultant circuit is shown in Figure 4.1c. the series open,short circuit in the parallel arm is transformed into step resonators, then inductors are replaced by transmission lines and the circuit is translated into ADS. The optimized circuit in ADS and its response is given in Figures 4.2a and 4.2.b respectively.

(a)

(b)

(c)
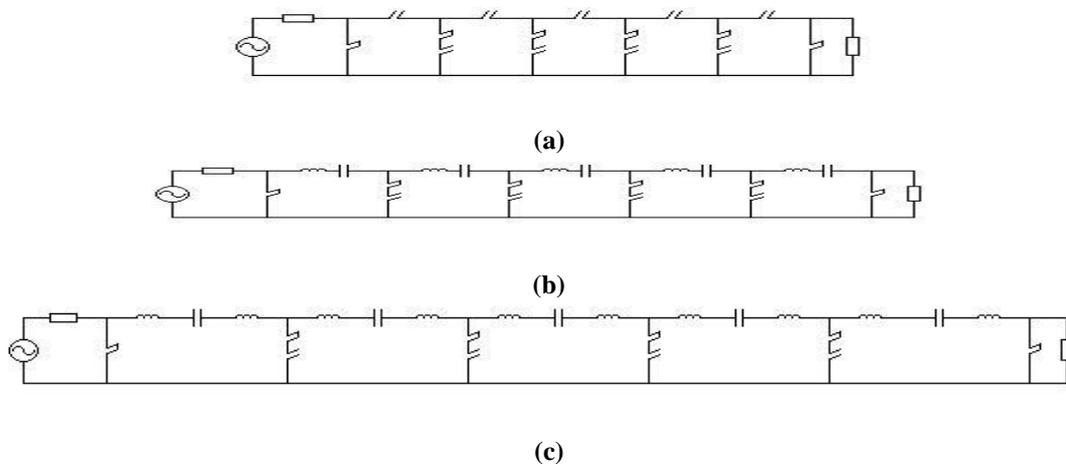
Figure 4. 1 Design steps for the 14 GHz HPF in FILPRO

76
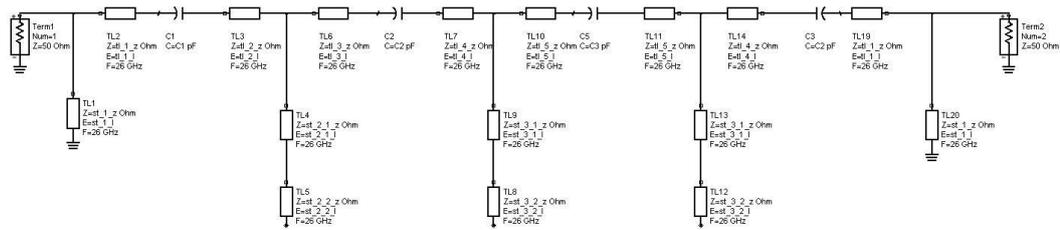
(a)
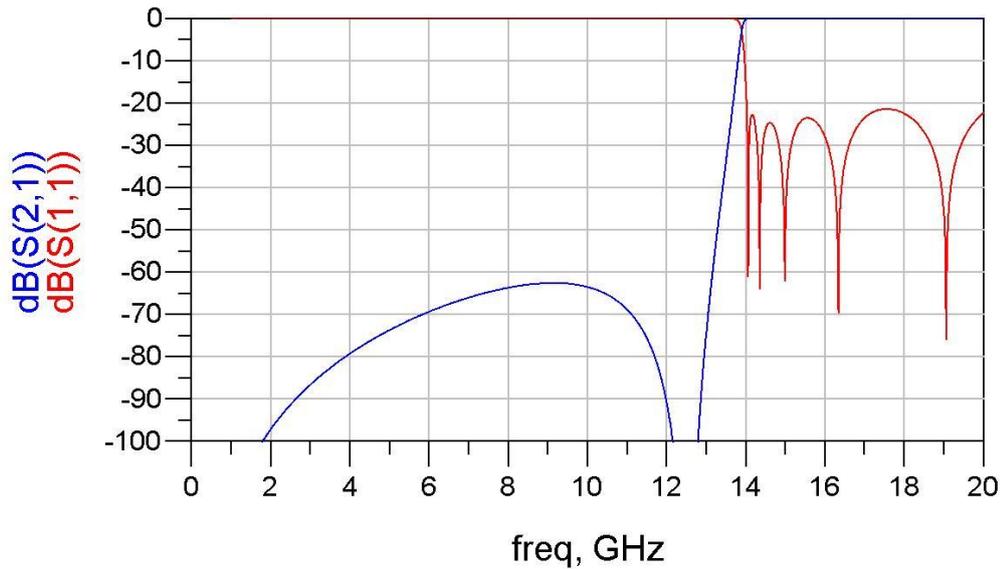
(b)

Figure 4. 2 14 GHz diplexer (a) ADS schematic (b) the optimized response

EM modeling will proceed as follows:

First the capacitors are replaced by broadside coupled lines. The capacitors to be replaced are shown in Figure 4.3. Notice that the width of coupled lines should be chosen as the same width as the transmission lines that were used to replace inductors. It should be kept in mind that the higher the impedance of the transmission line the better the less is the degradation of the response, however there is a trade-off. The higher the impedance of the transmission line the narrower the physical line would be. As the transmission line gets narrower, broadside coupled line to replace the capacitor will be longer. This limits the upper frequency of the approximation. As a result it can be deduced that the width of the transmission line should be thin enough to replace the inductors, but wide enough to replace the capacitor. Another possibility is to use very thin line to replace inductors and very thick broadside

77

coupled lines to replace capacitors, but this time reflections from T-junctions forms by thin and thick lines connected together will cause extra reflections which would in return degrade the return loss of the structure. The broadside coupled lines replacing the capacitors are shown in Figure 4.4. In the Figure SONNET simulations are included as two port circuits and parallel capacitors are used for fine tuning.
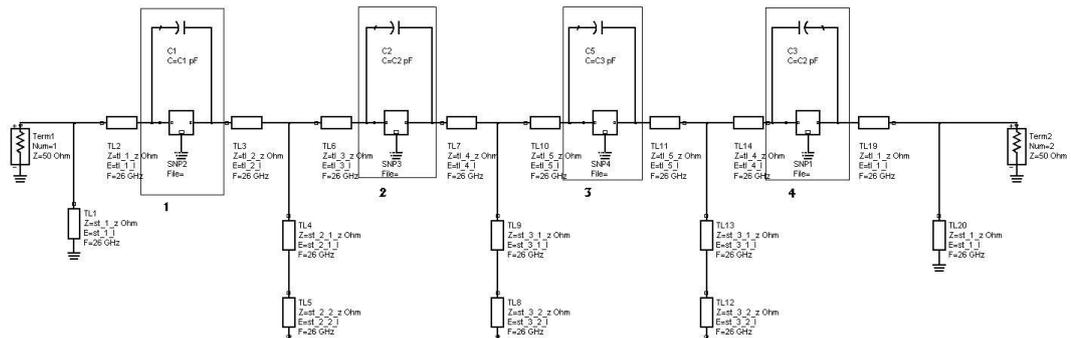
Figure 4. 3 Capacitors to be replaced
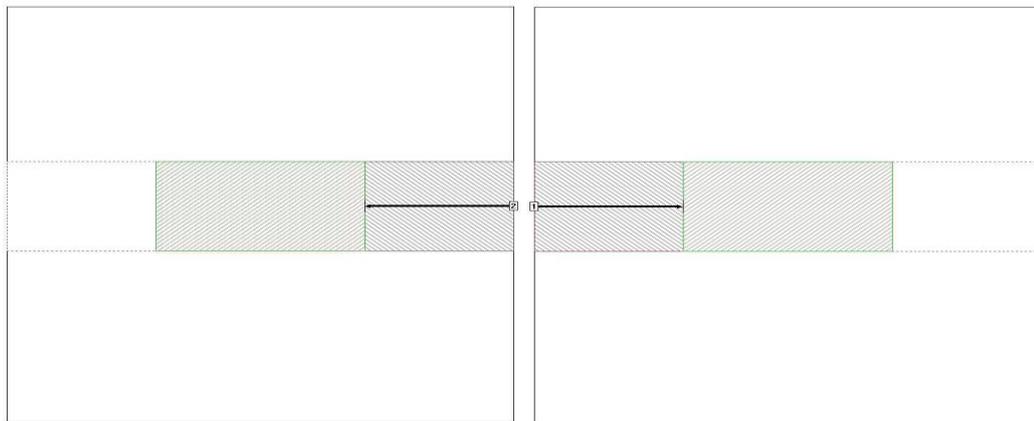
Figure 4. 4 Simulation layout for broadside coupled line replacing capacitors.

After replacing the capacitors and the inductors in the circuit, the circuit will be divided into building blocks as TL-Cap (broadside coupled line)-TL and TL-stub-TL. As shown in Figure 4.5.a to c. Note that the primed ones in Figure 4.5.a are TL+cap+TL triplets and unprimed ones are TL+stub+TL triplets. These building blocks will be simulated by SONNET and the results are embedded into the circuit

78

as 3-port circuits in ADS as shown in Figure 4.5.a. Whole circuit is re-optimized and later but into N-port circuit form as shown in Figure 4.6. Here only length of the transmission lines and stubs are optimized. That N-port circuit is recursively simulated in SONNET and optimized in ADS until we get a two-port circuit as shown in Figure 4.7
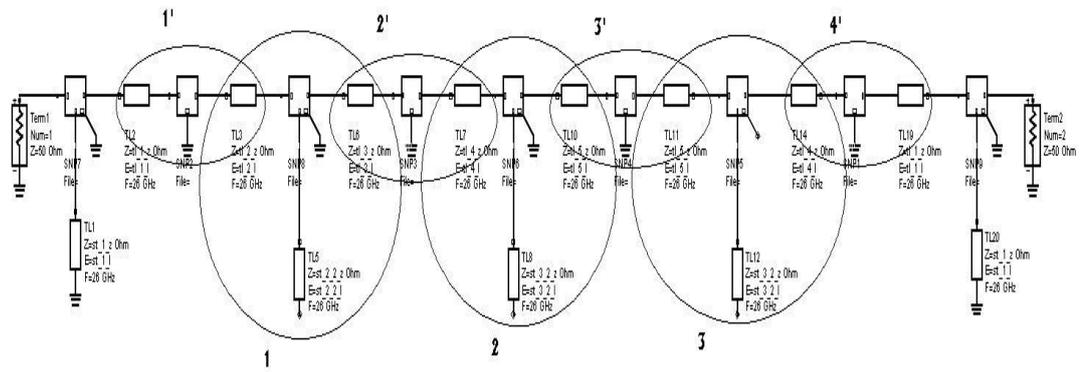
(a)
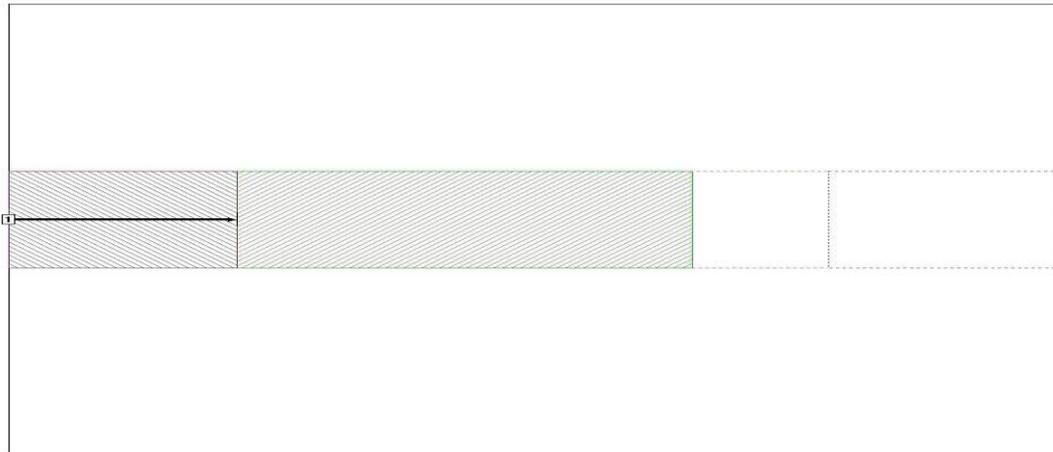
(b)
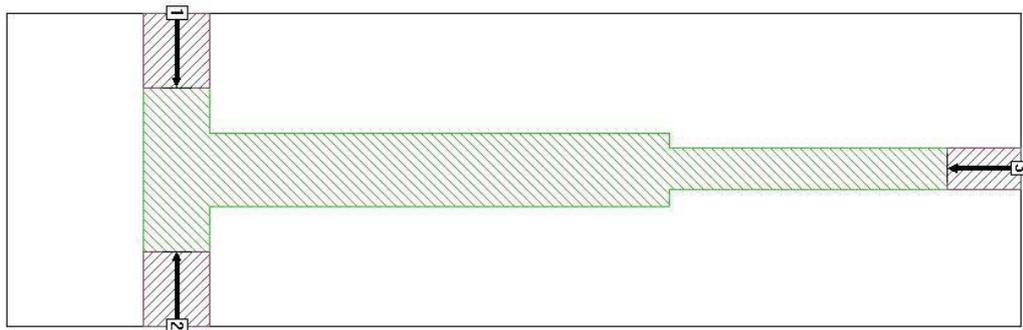
(c)

Figure 4. 5(a) TL+cap+TL and TL+stub+TL triplets in ADS (b) TL+cap+TL in SONNET (c) TL+stub+TL in SONNET
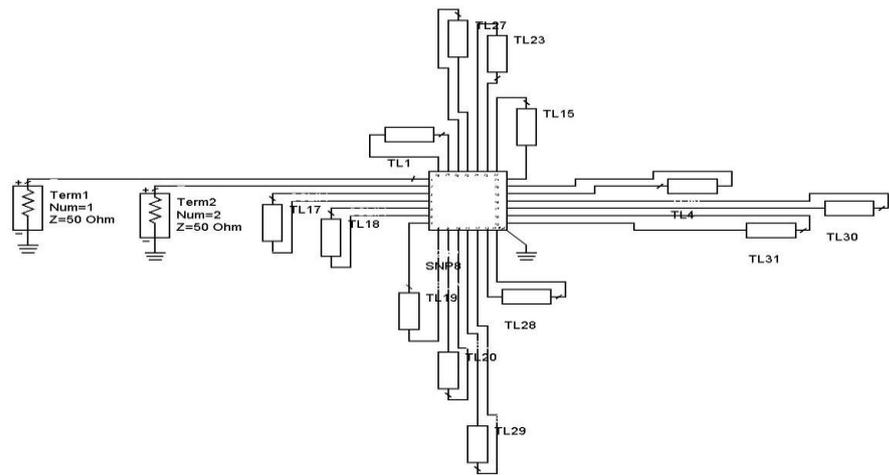
(a)
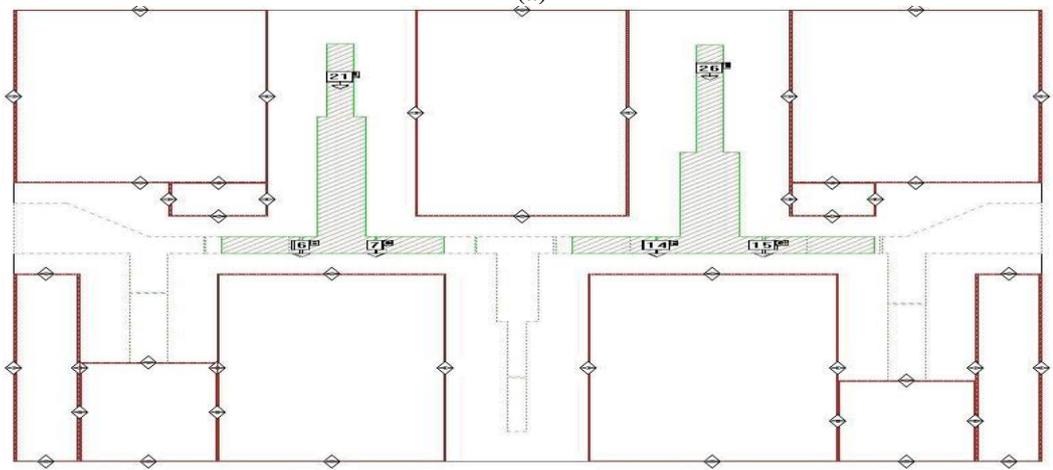
(b)
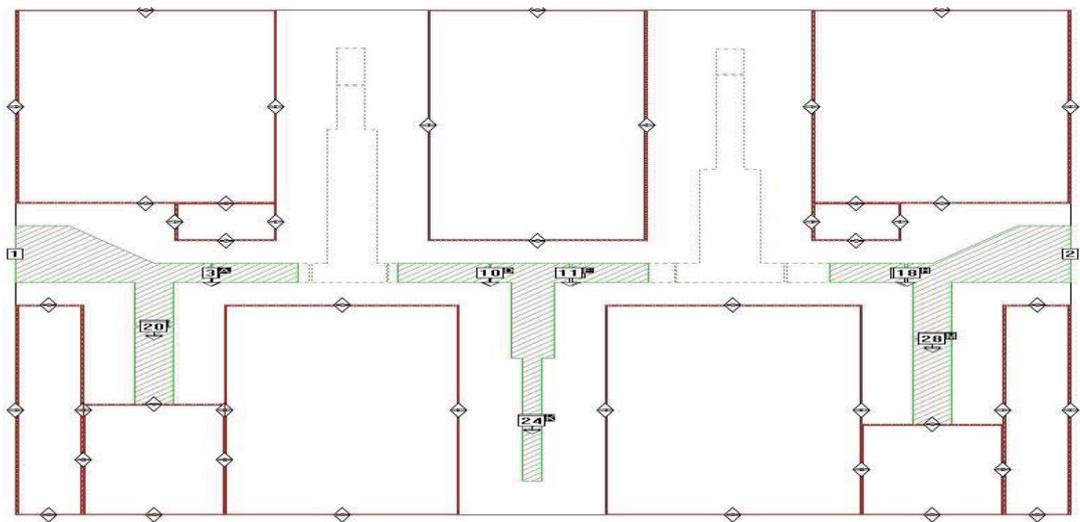
(c)

Figure 4. 6 (a) 28 port circuit in ADS to optimize SONNET modeling. (b) SONNET EM model top side (c) SONNET EM model bottom side

81
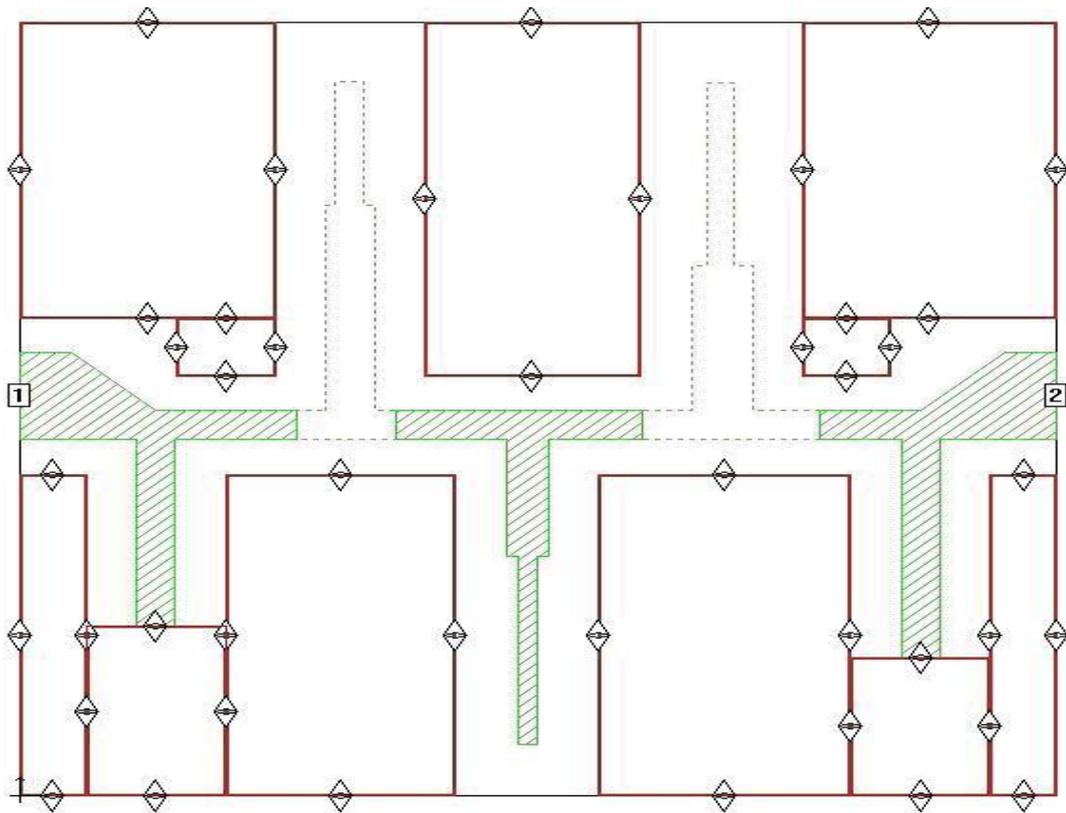
(a)
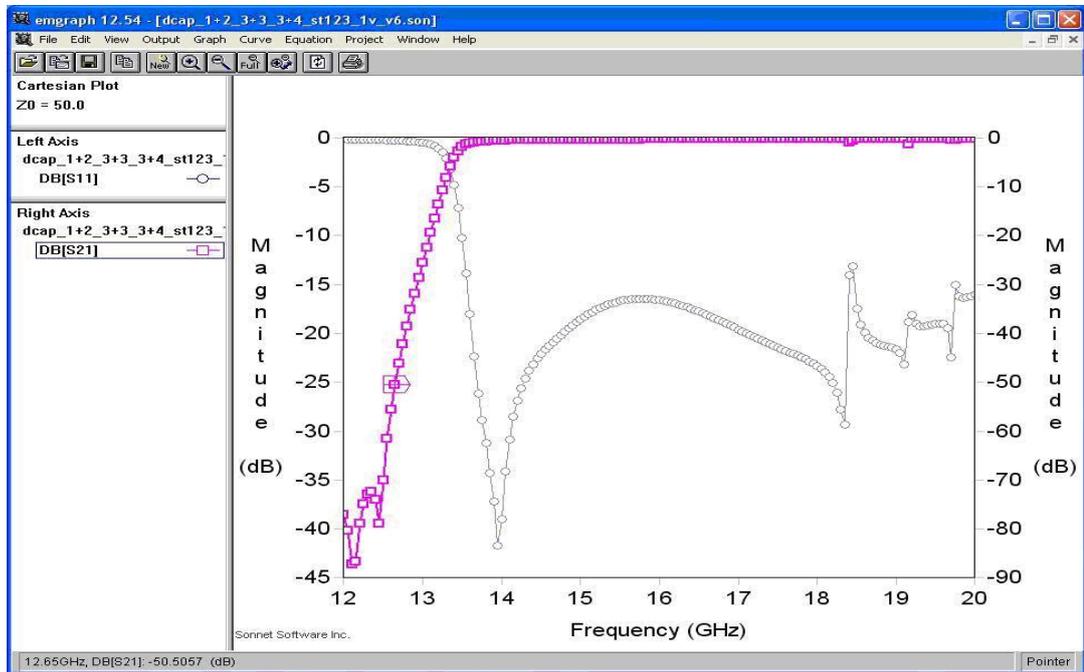
(b)
Figure 4. 7(a) Final SONNET layout (b) Its response

It is seen that passband return loss is below -15 dB and the insertion loss is below 1 dB. A rejection of 50 dBc is achieved at 13 GHz. The spikes occurring above 18 GHz is due to the weakness of the simulation program for taking into account the walls which are put to shift the box mode resonances over 20 GHz.Finally the final layout is simulated in CST and the filter is manufactured. The mechanical drawing for CST simulation is given in Figure 4.8 a and 3.8 b. The result of the 3-D simulation is given in Figure 4.8.c. It is seen that the return loss gets better about 2 dB and the spikes in SONNET vanishes whereas the insertion loss and rejection remain the same.

(a)

(b)
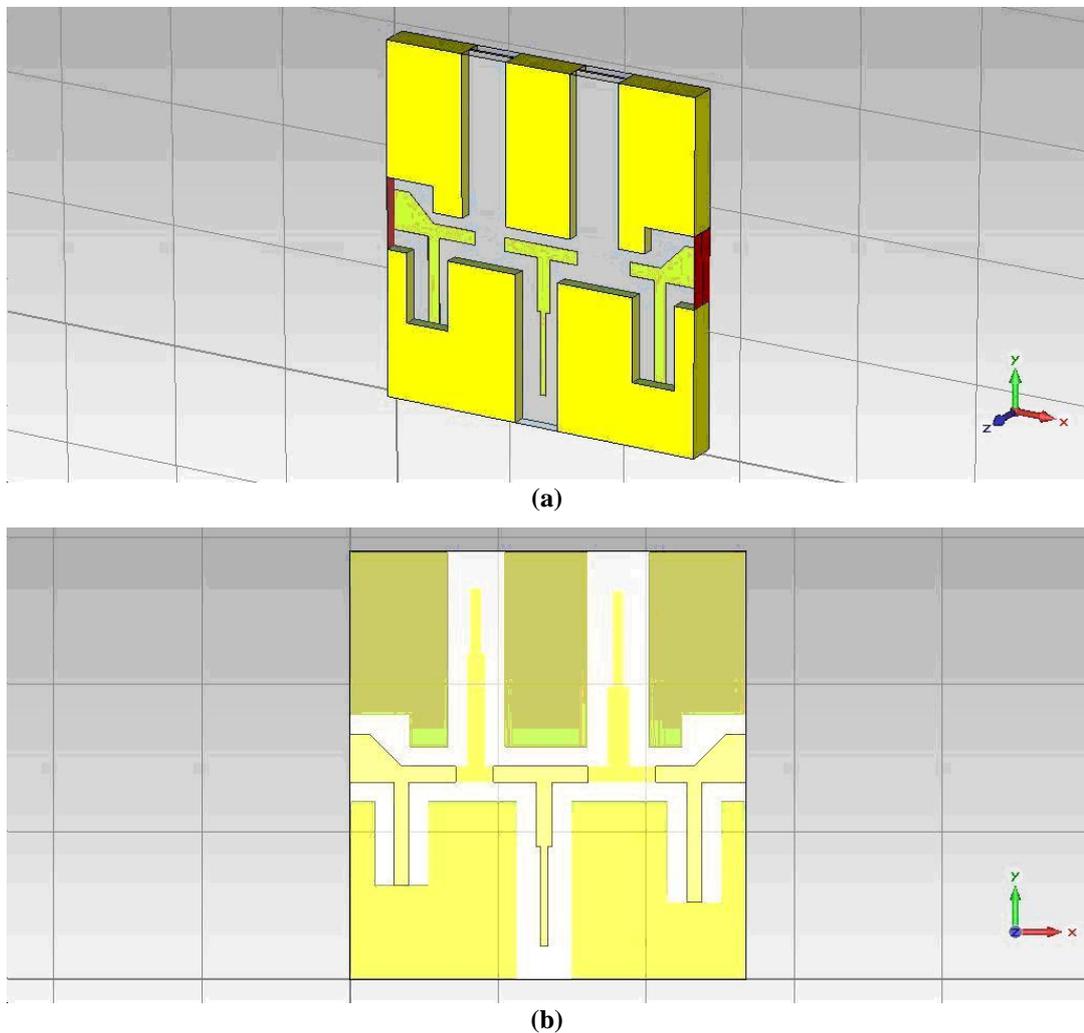
Figure 4.8 (a) CST layout (b) top and bottom sides viewed together

S-Parameter Magnitude in dB

S1,1 : -18.824343	
S2,1 : -0.21506501	
S1,2 : -0.21506492	
S2,2 : -18.777729	
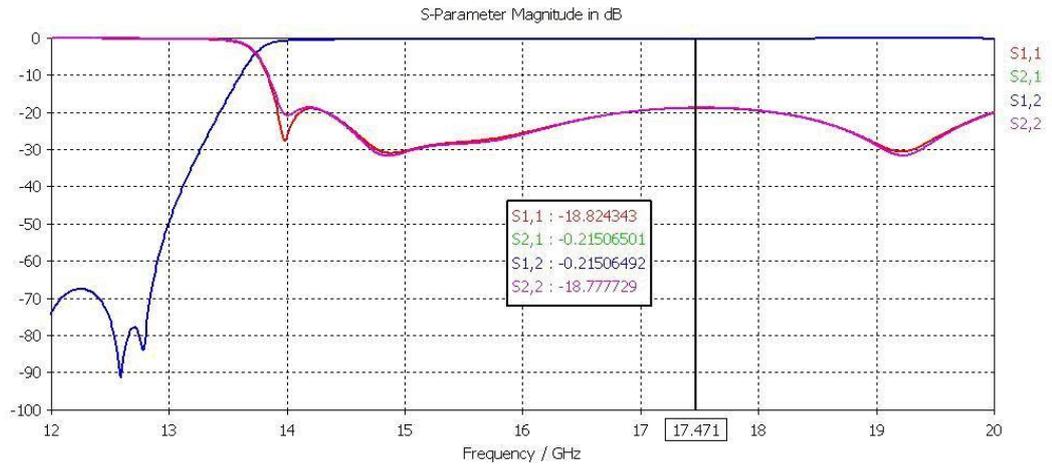
Figure 4. 8 (continued) (c) CST result

When the real filter is to be manufactured, tuning screws are added to the filter mechanics in order to compensate for the PCB manufacturing tolerances. The manufactured filter is given in figure 4.9.a. The measurement results after tuning are given in figure 4.9.b.
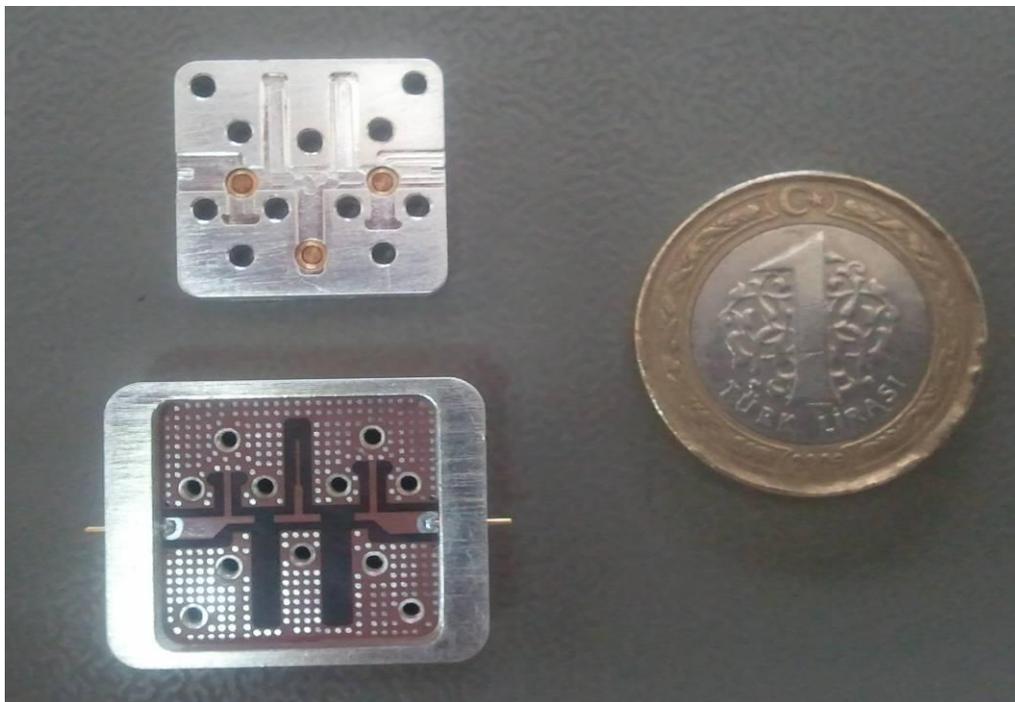
(a)
Figure 4. 9 (a) 14 GHz HP filter module

84
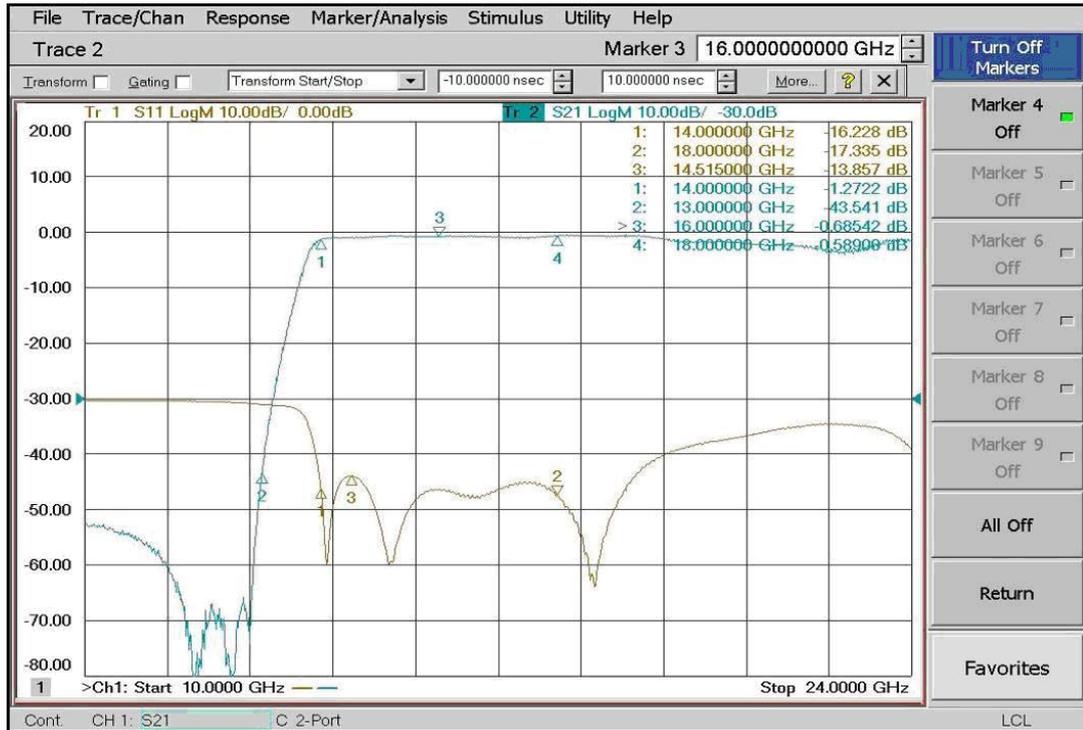
(b)
Figure 4. 10 (continued) (b) Its response.

It is seen that the passband return loss is about 14 dB and passband insertion loss is 1.2 dB at 14 GHz and below 1 dB up to 18 GHz as expected. Rejection at 13 GHz is better than 40 dBc. The difference in the return loss may emerge form manufacturing tolerances of PCB and mechanical body as well as the launching scheme.

EM modeling of diplexers follow the same path but this time there are two channels to design : LP channel and HP channel. The filters in these channels can be designed as singly terminated or foreshortened doubly terminated filters. The diplexing OC PCL will be formed as told in chapter 2 and will not be repeated here.

4.3.   Design of 6 GHz Diplexer

As an example, 6 GHz diplexer is designed. First the LP and HP channels are designed as singly terminated filters. For HP channel passband ripple is taken to be 0.01 dB , the corner frequency is taken as 6 GHz and quarter wavelength frequency

is taken as 12 GHz. Design steps are straight forward and are given in figure 4.10 (a) to (g). The formation of OC PCL is given in figure 4.10 (g) and detailed calculations are not given here as they are already given in chapter 3 in equation (3.1.30).
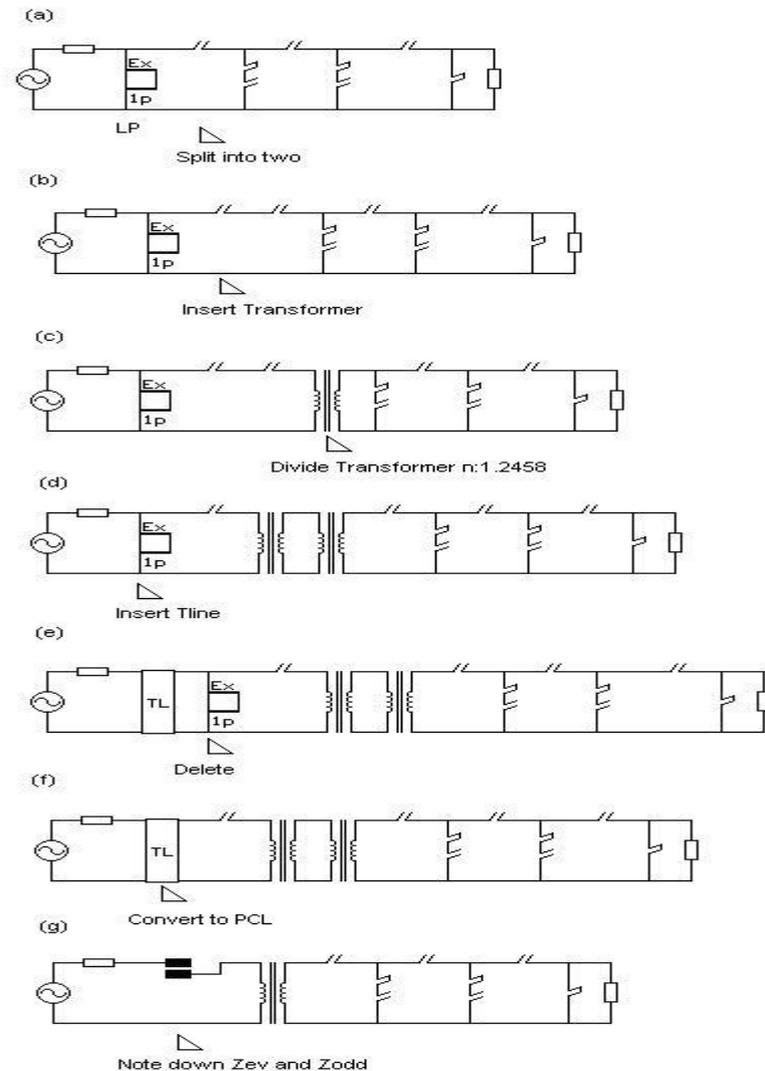
Figure 4. 11 Design steps for HP channel of 6 GHz diplexer

For LP channel passband ripple is taken to be 0.01 dB , the corner frequency is taken as 6 GHz and quarter wavelength frequency is taken as 10 GHz. Design steps are straight forward and are not repeated here. The final circuit in FILPRO is given in Figure 4.11.
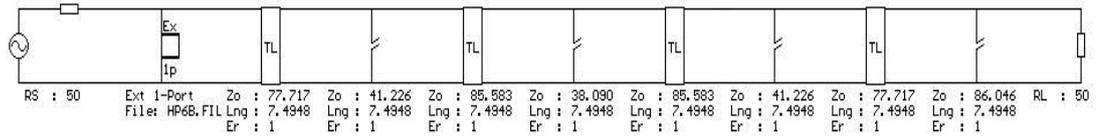
Figure 4. 12 FILPRO circuit of LP channel of 6 GHz diplexer

Having designed the LP channel, and obtaining the OC PCL section; LP and HP channels are connected to the through and isolated ports of the OC PCL respectively while leaving the coupled port open in ADS as shown in Figure 4.12.
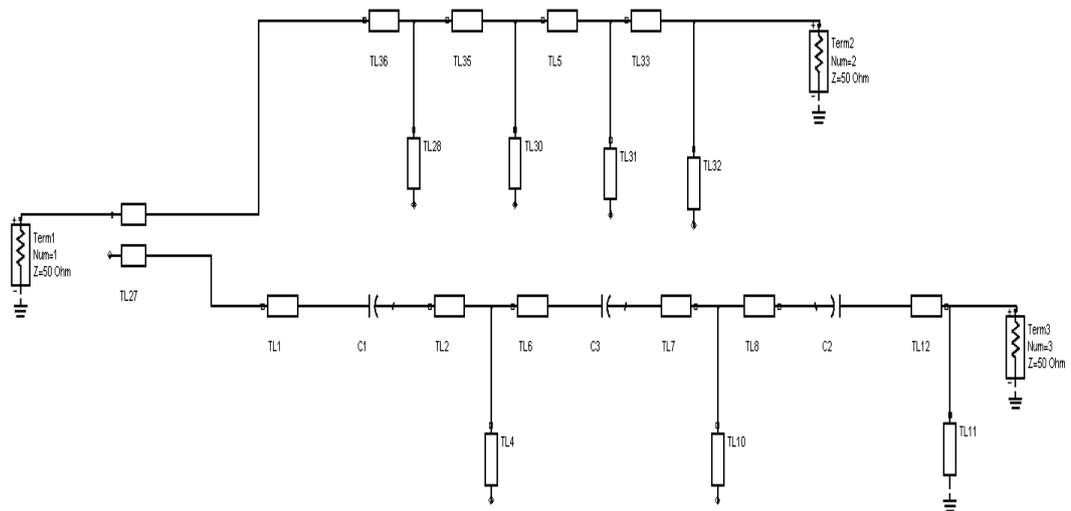
Figure 4. 13 ADS circuit of 6 GHz diplexer

LP section is modeled as 3 ports circuits replacing the TL-stub-TL triplets as shown in Figure 4.13.
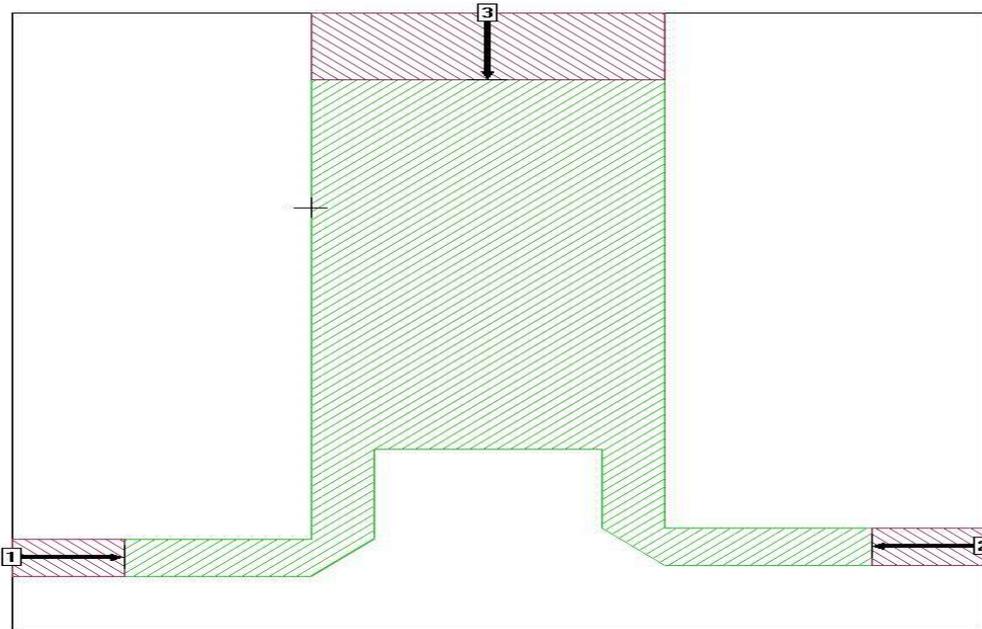
Figure 4. 14 TL-stub-TL triplet
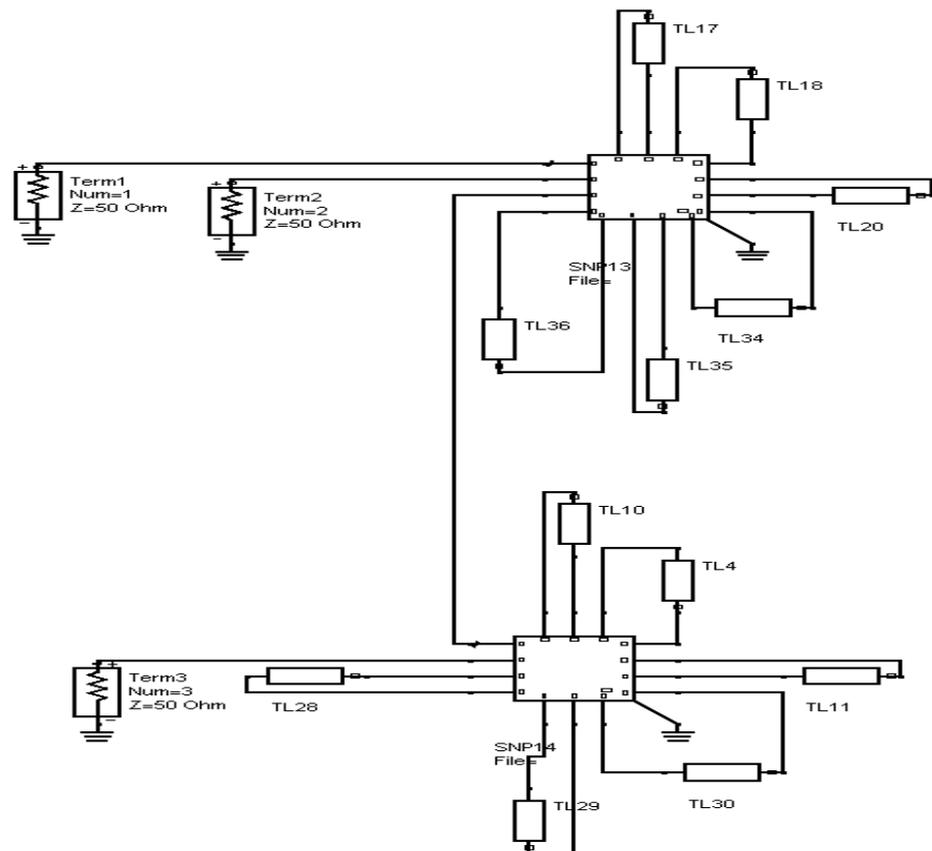
Figure 4. 15 N-port circuit for optimizing diplexer response

After replacing all the triplets, only length of the transmission lines and stubs are left. N-port circuit is formed using co-calibrated ports for optimization of stated lengths. The procedure for HP filter is followed in HP and LP channels and the following circuits consisting of two N-port circuits diplexed in parallel via OC PCL, later OC PCL section is modeled in SONNET and it is connected to the LP section of the diplexer as shown in Figure 4.15. LP and HP sections are simulated and the whole circuit is optimized recursively to obtain the desired performance. Final diplexer is achieved in Figure 4.16. As in 14 GHz HP filters tuning screws are placed for compensating manufacturing tolerances. The measurement results and pictures of the manufactured dipexer are given in Figure 4.17 As seen form the graph an input return loss of -16 dB is achieved. The rejection at 5 GHz for the HP channel is above 47 dBc and the rejection for at 7 GHz for the LP channel is above 40 dBc, the ultimate rejection for both channels is above 35 dBc. The insertion loss for both channels is better than 0.5 dB. The crossover is exactly at 6 GHz having a loss of - 3.8 dB for both channels. Other diplexers are designed in a similar fashion and the responses are given below in figure 4.18
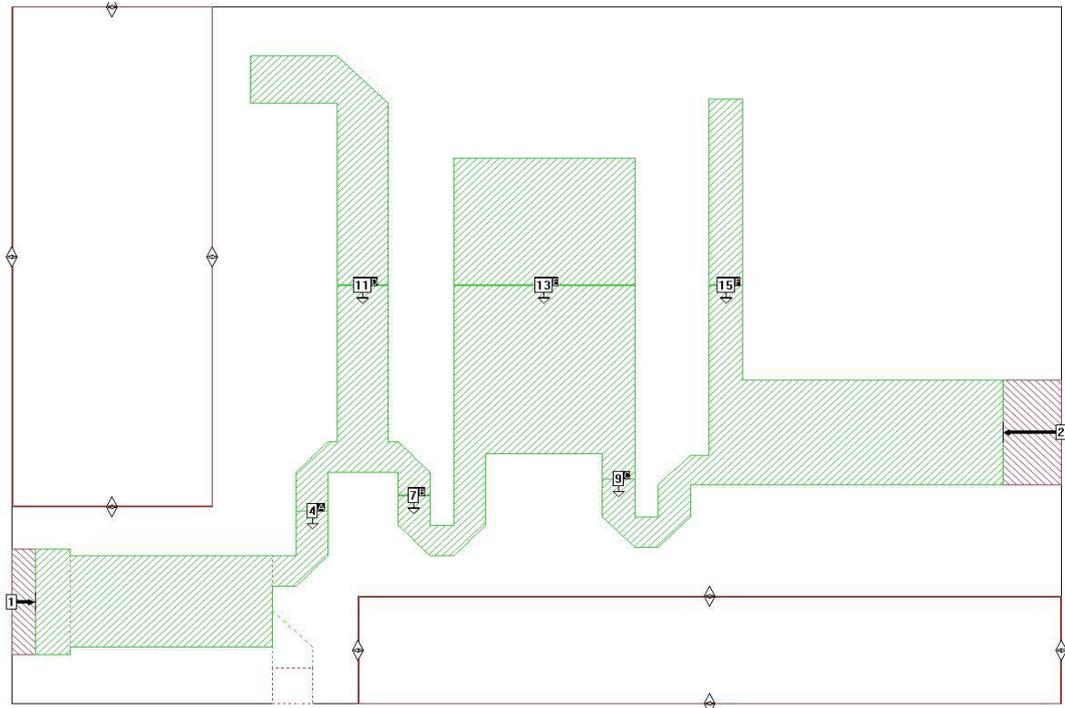
(a)
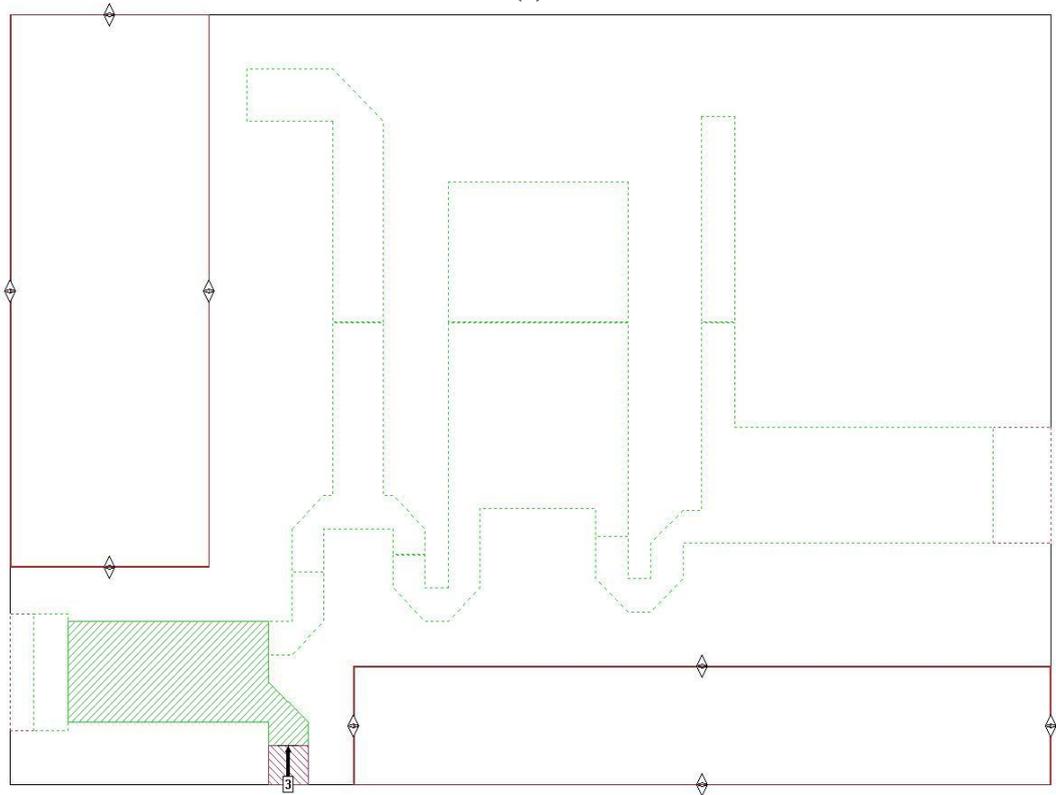
(b)

Figure 4. 16 (a) top section of LP Channel of 6 GHz diplexer (b) bottom side of LP channel of 6 GHz diplexer

90
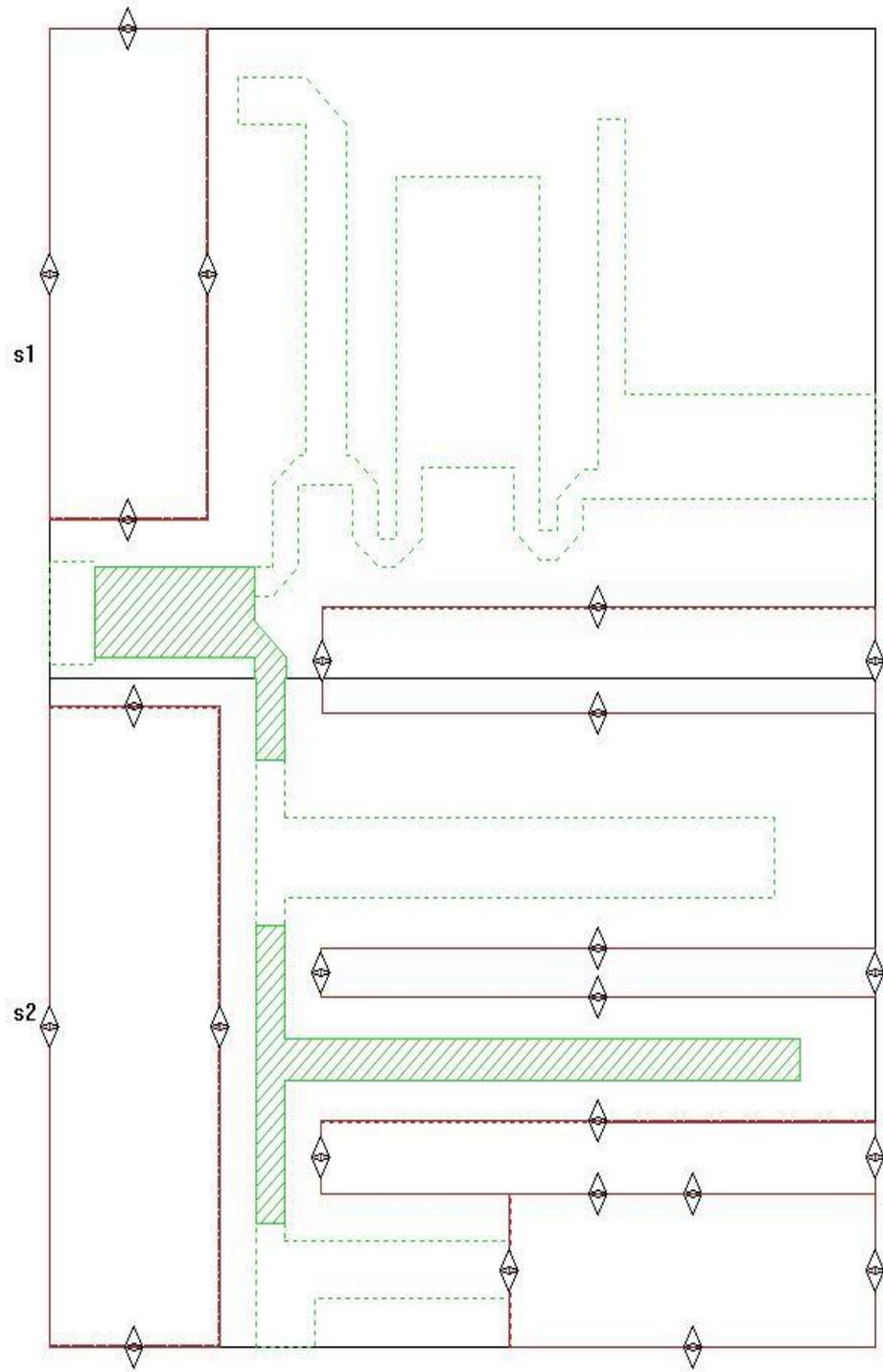
Figure 4.16 (a)) top section of 6 GHz diplexer

91
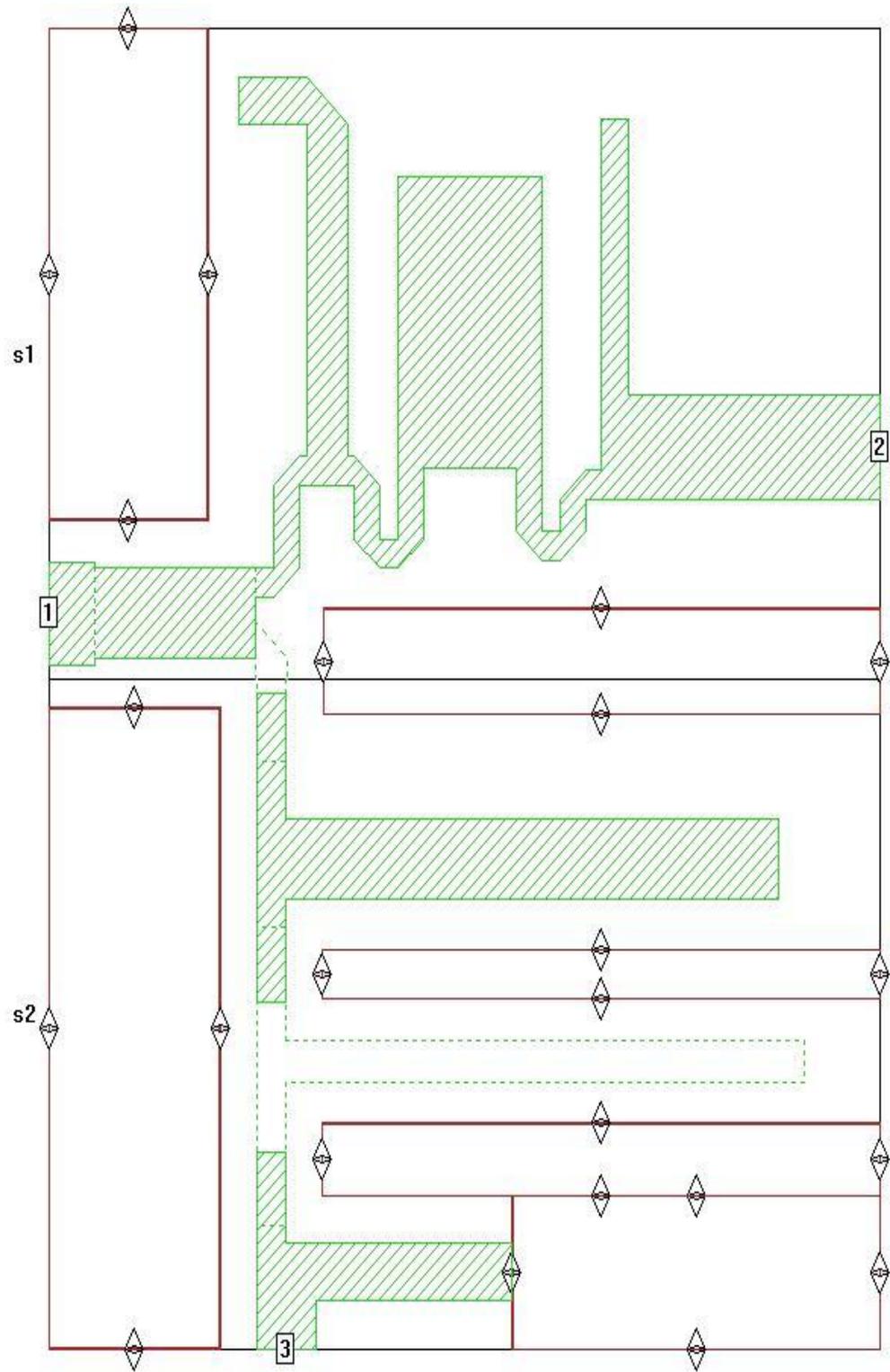
Figure 4.16 (continued) (b) bottom side of 6 GHz diplexer
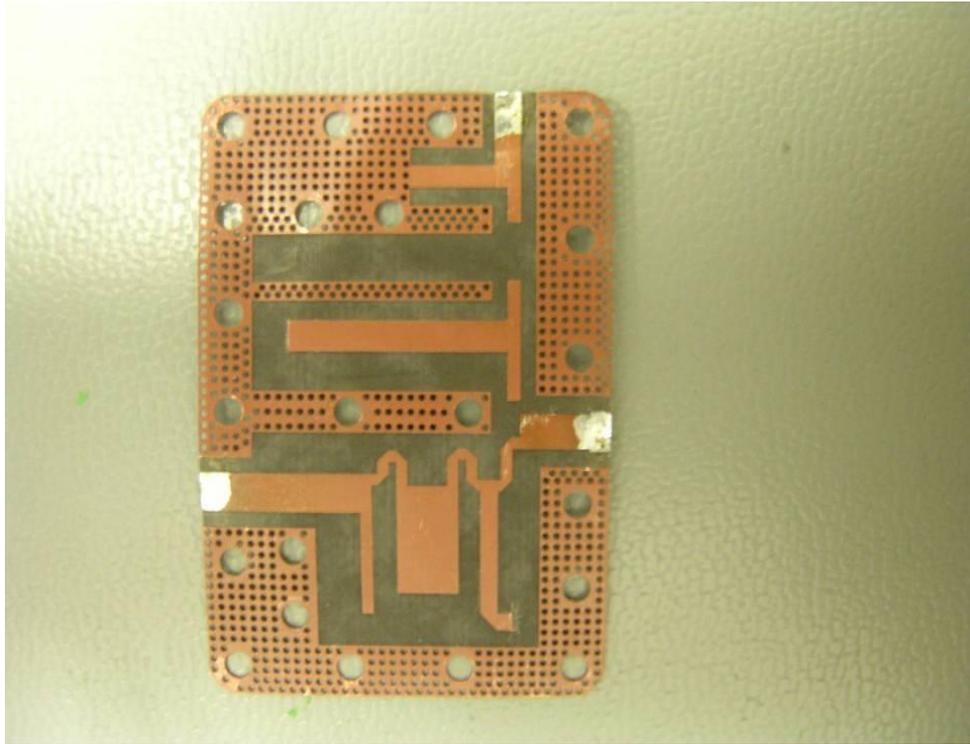
(a)
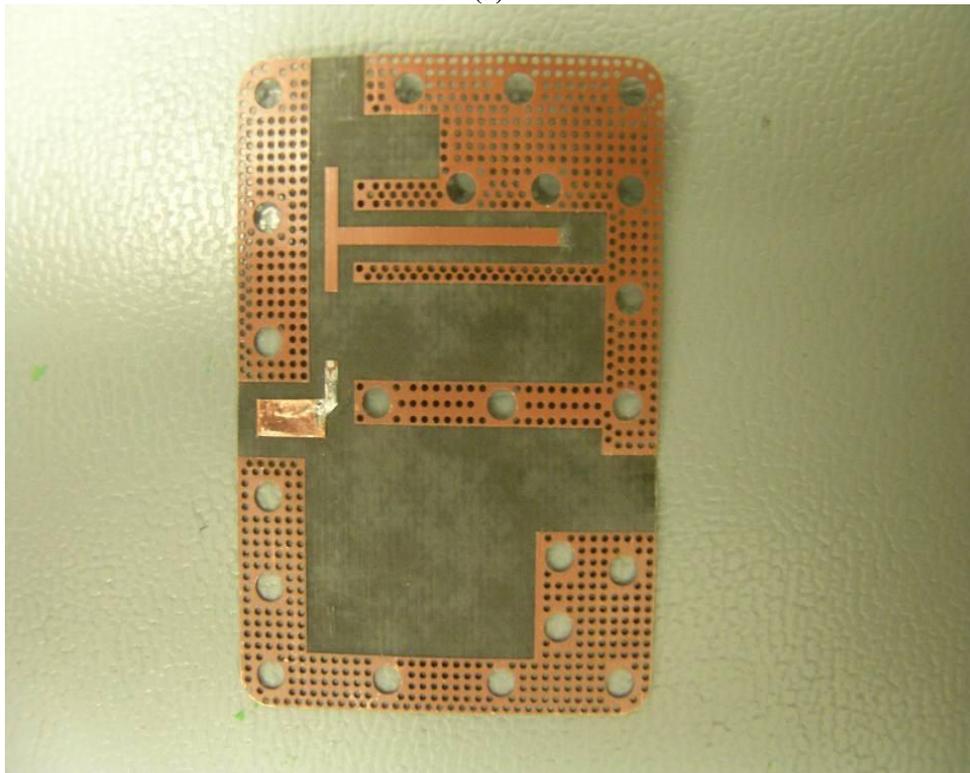
(b)
Figure 4. 17 (a) top side for 6 GHz diplexer (b) bottom side for 6 GHz diplexer
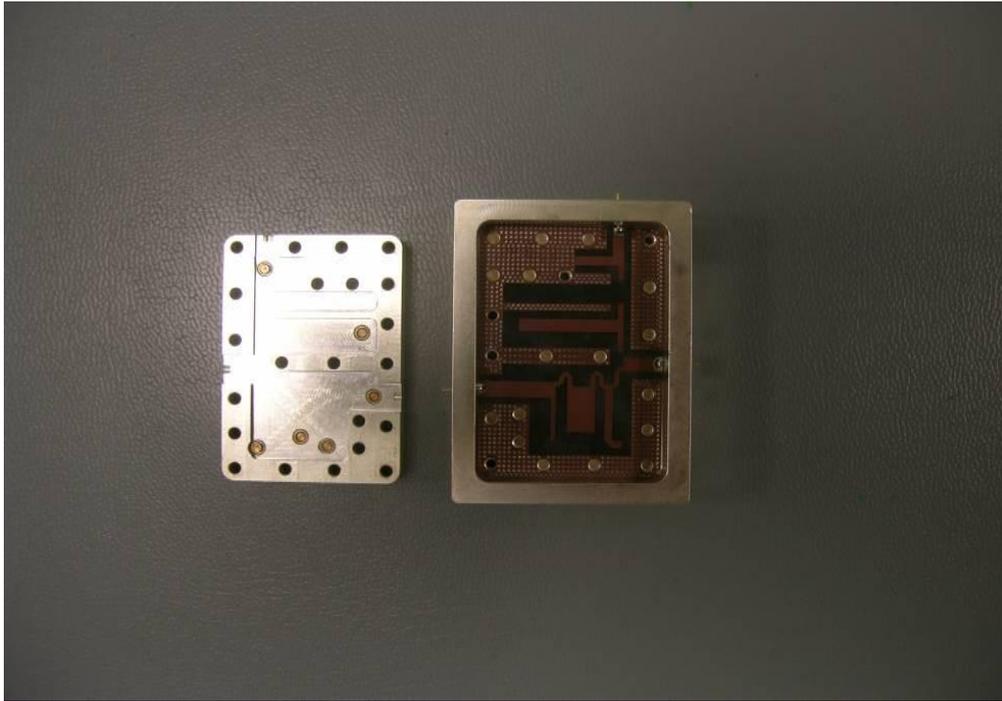
(c)
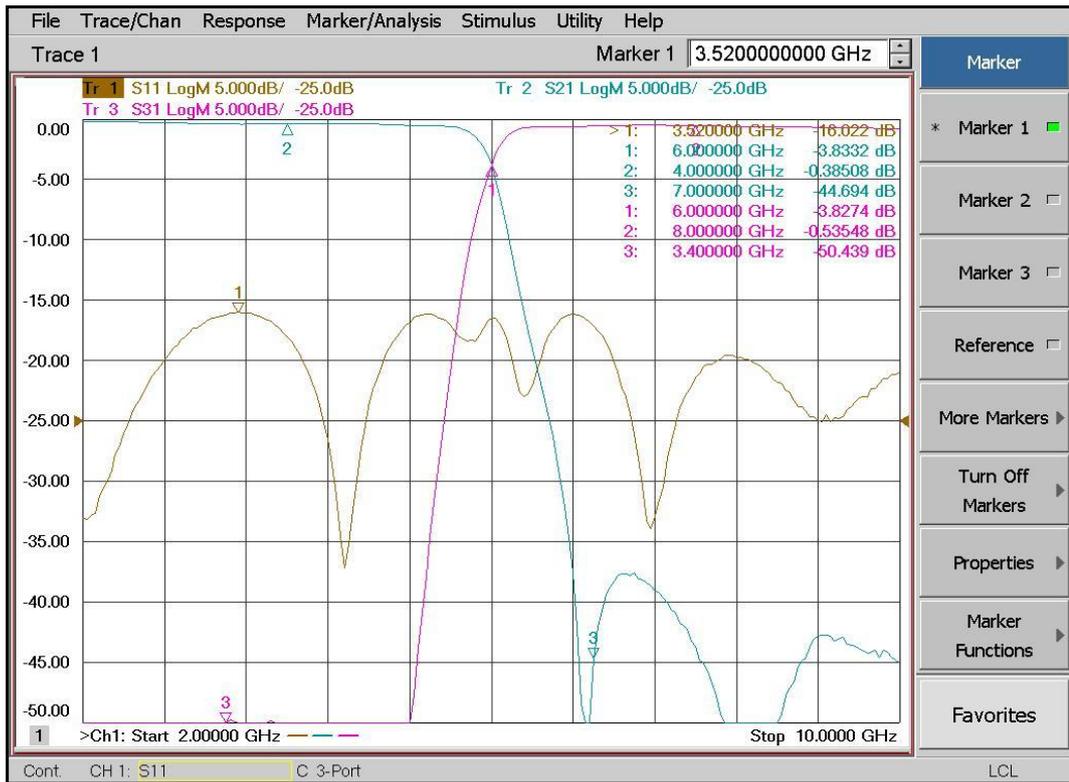
(d)

Figure 4. 17 (continued) (c) 6 GHz diplexer module (d) Its response

4.4 Measurement Results For Other Diplexers
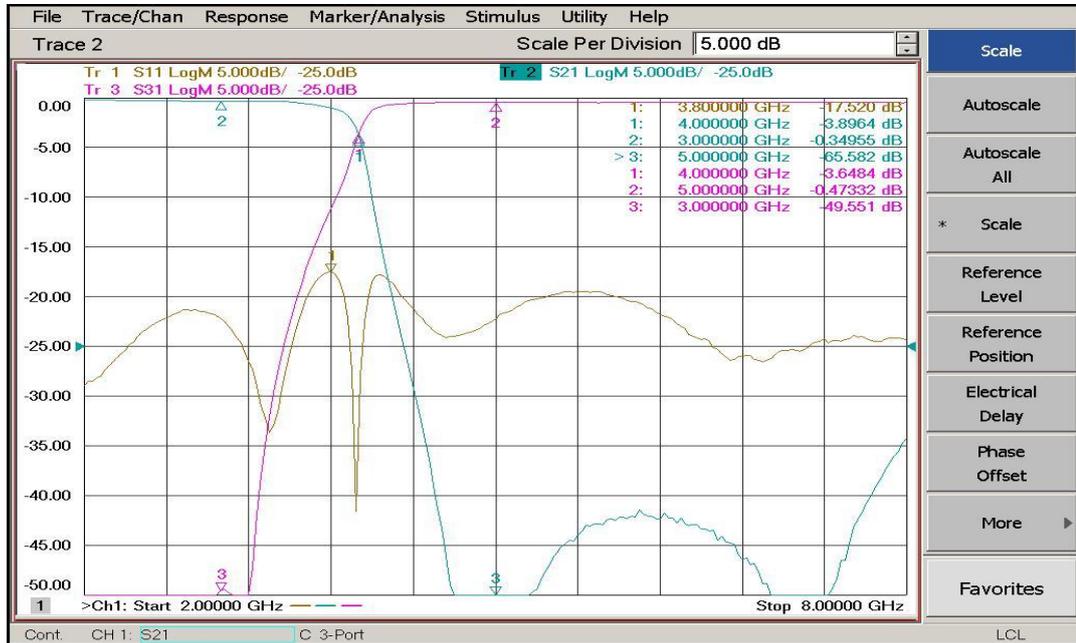
(a)
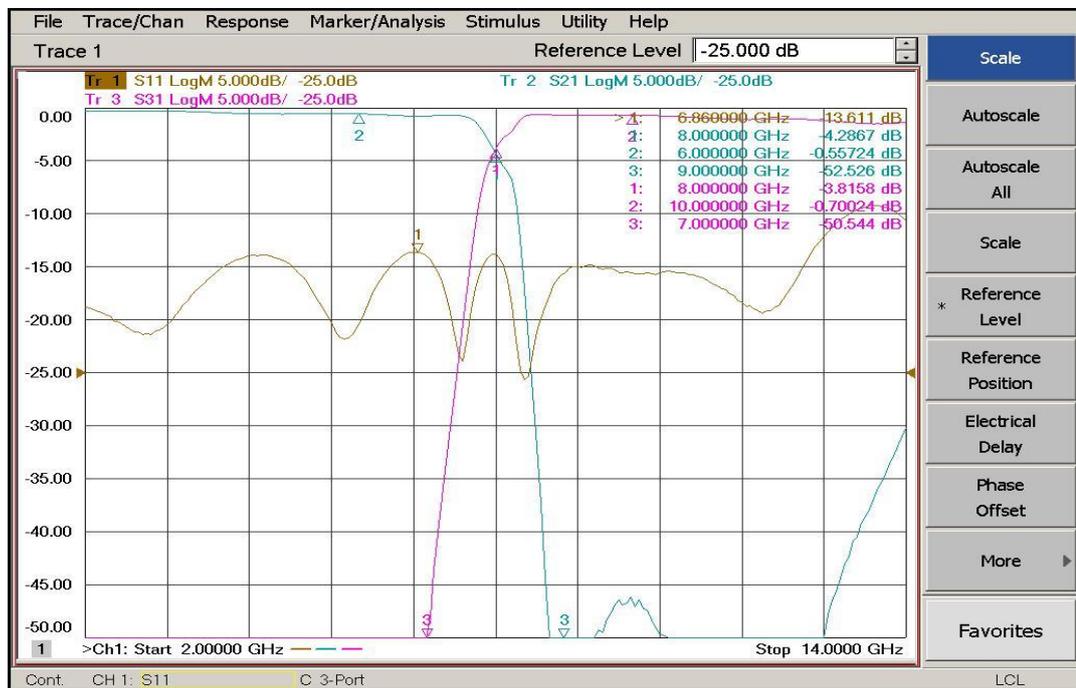
(b)

Figure 4. 18 (a) response of 4 GHz diplexer (b) response of 8 GHz diplexer
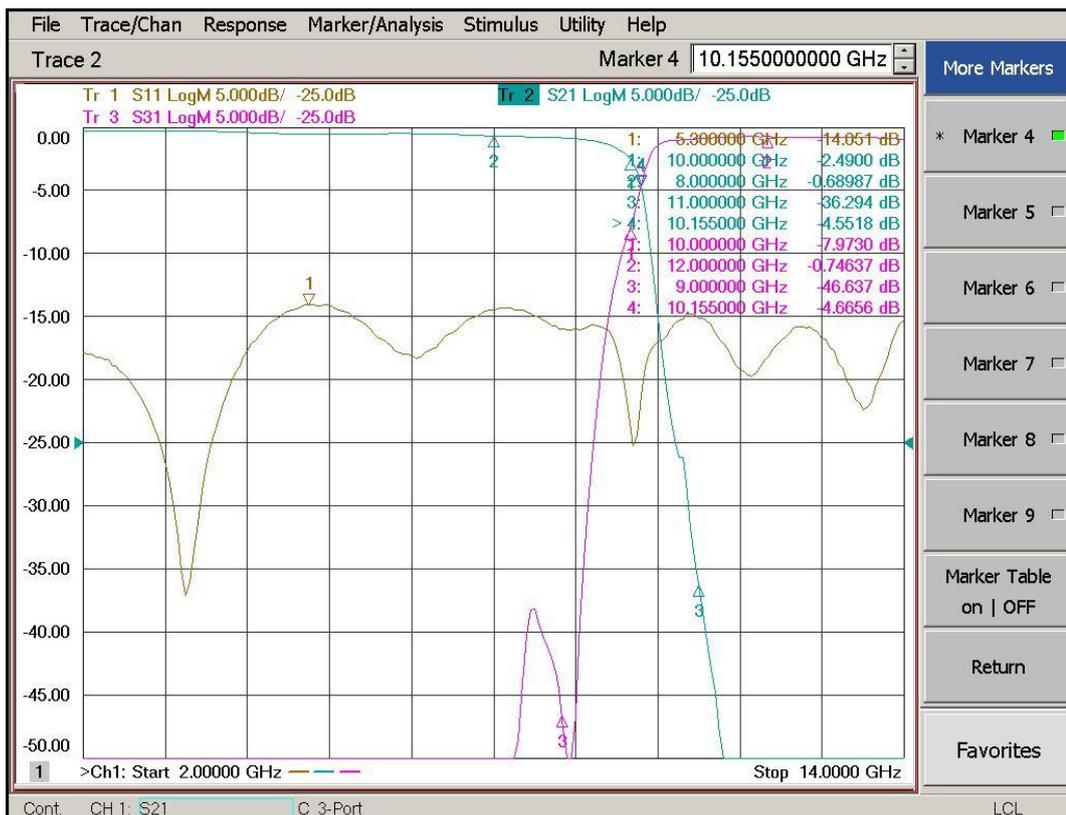
(c)
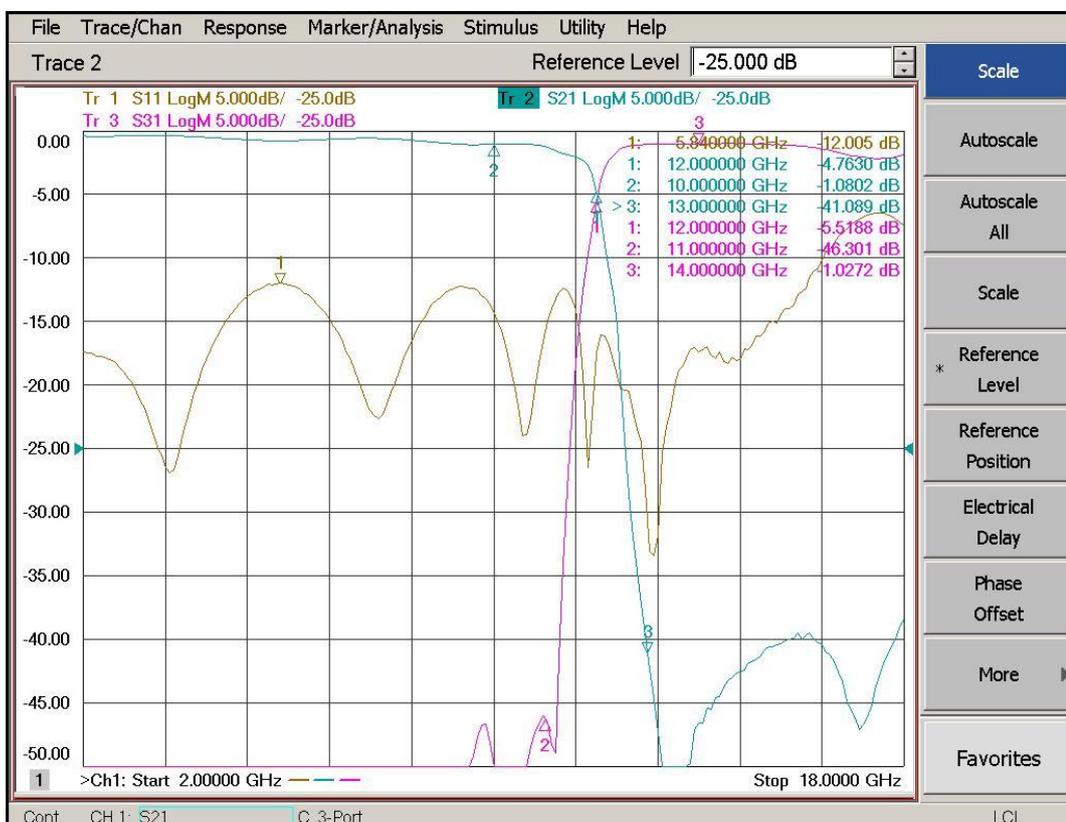
(d)

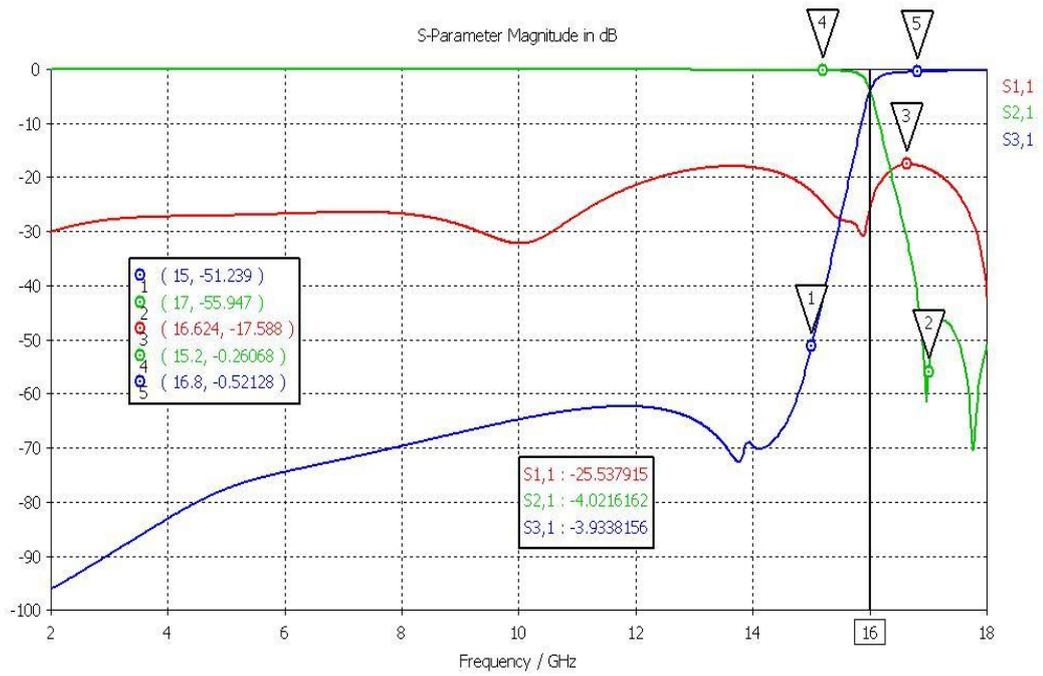**Figure 4. 18 (continued) (c) response of 10 GHz diplexer (d) response of 12 GHz diplexer**
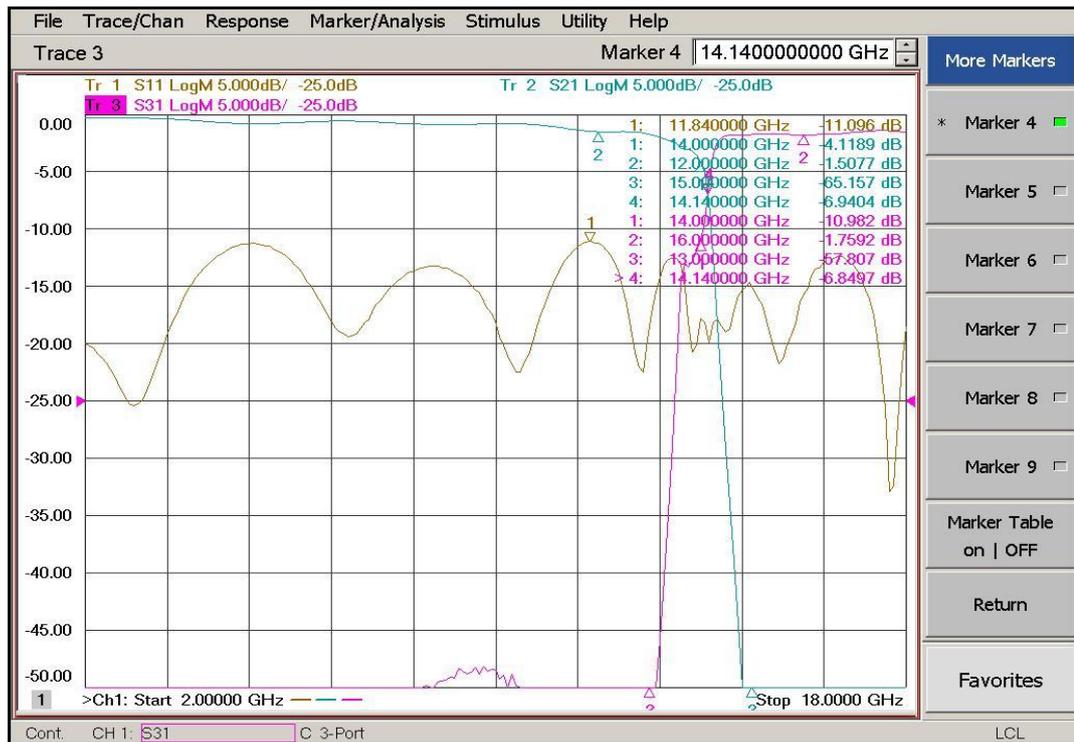
(e)

Figure 4. 18 (continued) (e) response of 14 GHz diplexer

It is noted that as the cross-over increases the response fails to comply with SONNET results. As the cross-over frequency increases, return loss degradation is obvious. Besides the cross-over loss increases in an unexpected level and in some channels cross-over frequency seems to shift. The former reasons, i.e. return loss and cross-over loss are of concern since cross-over shift can be adjusted by tuning. Hence it becomes compulsory that the reason for degradation should be found and corrected The prime suspect is an old friend: the connector. The launching scheme should be optimized for the entire band. For this reason a 50 ohm transmission line was drawn and simulated with the current air gap,seal, pin radius and air above pin. When we increase the air around the pin from 20 mils to 24 mils and the distance between the top wall and pin from 32 mils to 40 mils the return loss decreases from -12 dB to -34 dB. Later diplexers were simulated according to new launching scheme to ensure performance. The responses are given below from figure 4.20 (a) to (g).

97
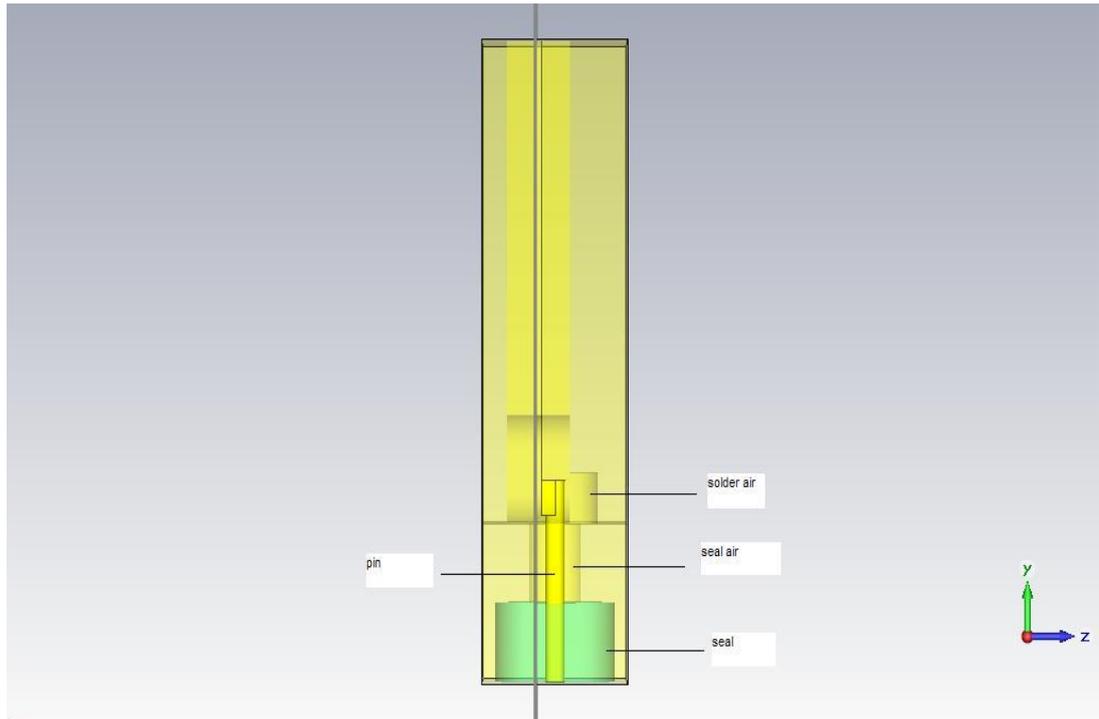
(a)
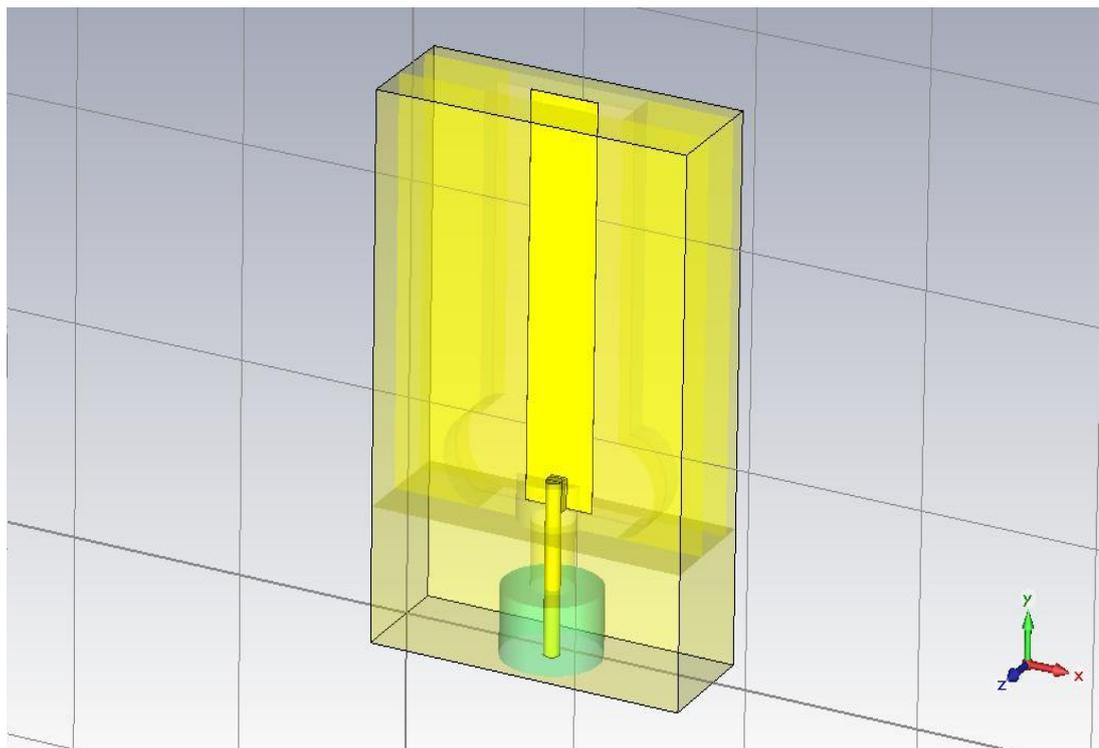
(b)

Figure 4. 19 (a) mechanical view of connector (b) prespective view of connector
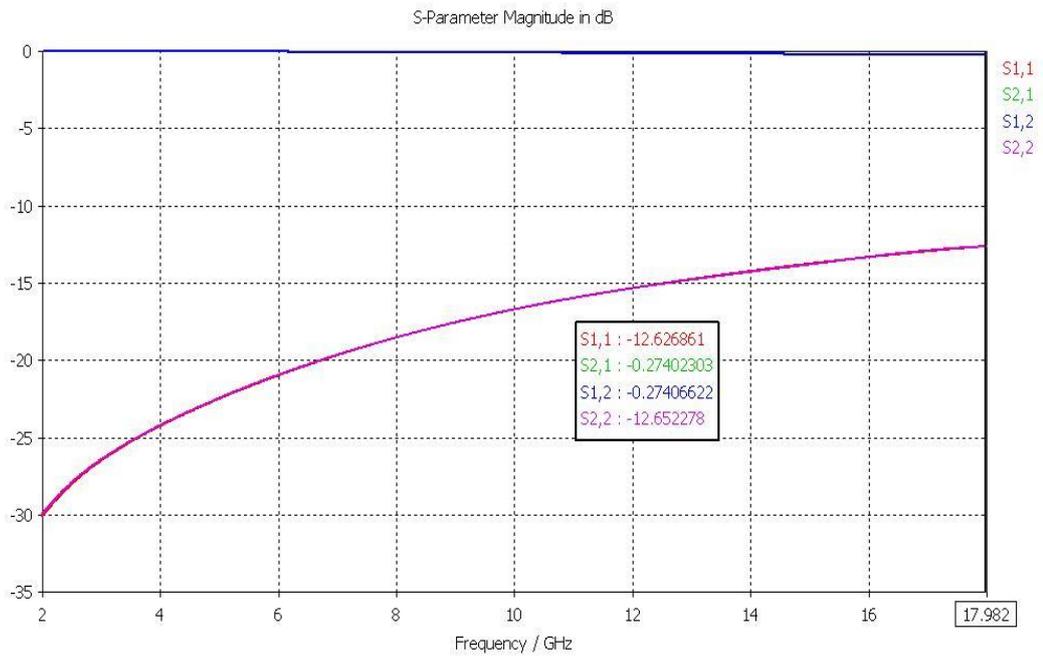
(c)
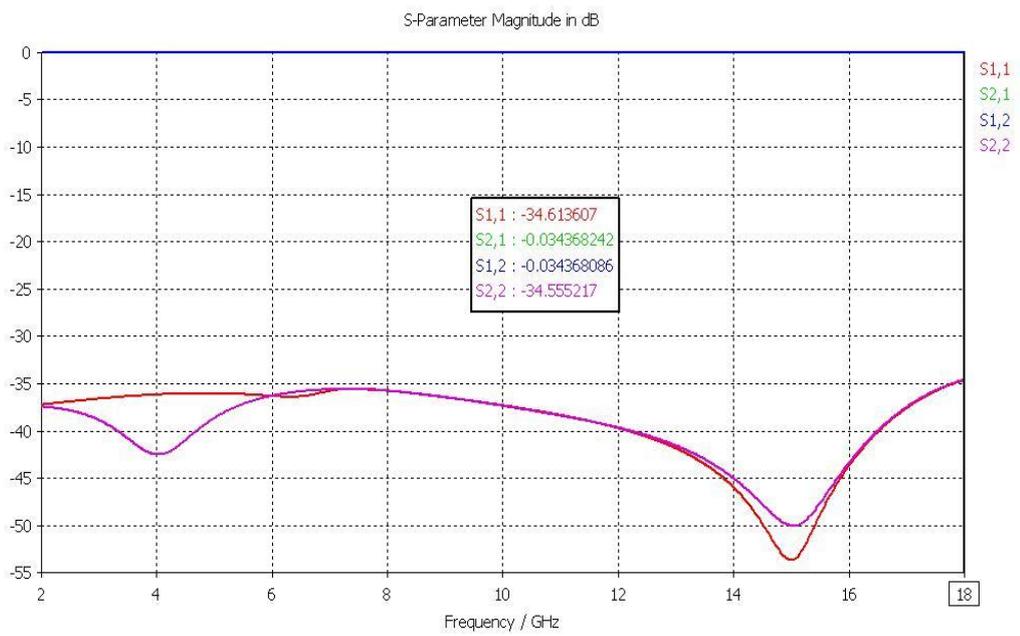
(d)

Figure 4. 19 (continued) (c) original response (d) optimized response
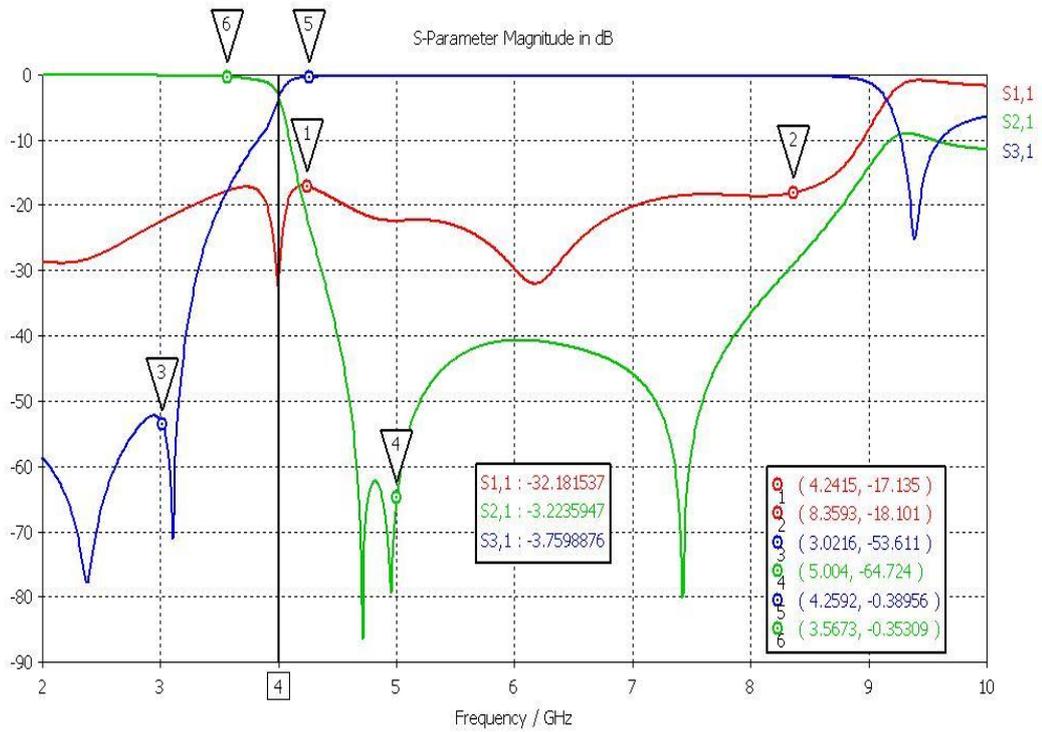
(a)
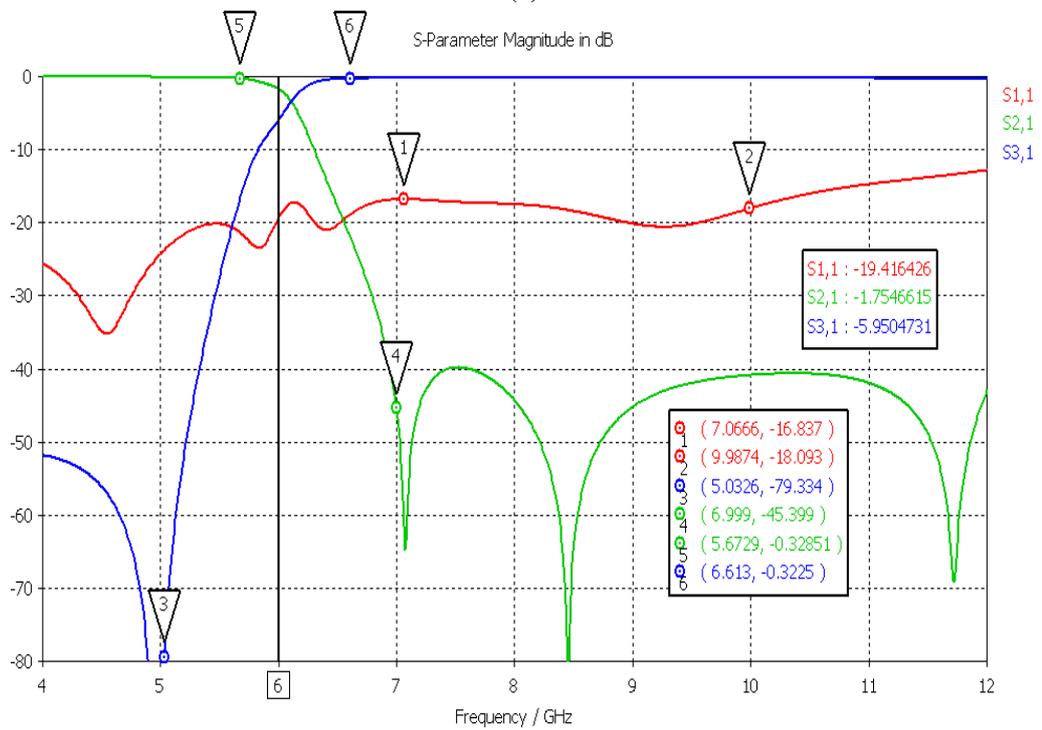
(b)
Figure 4. 20 (a) response of 4 GHz diplexer (b) response of 6 GHz diplexer
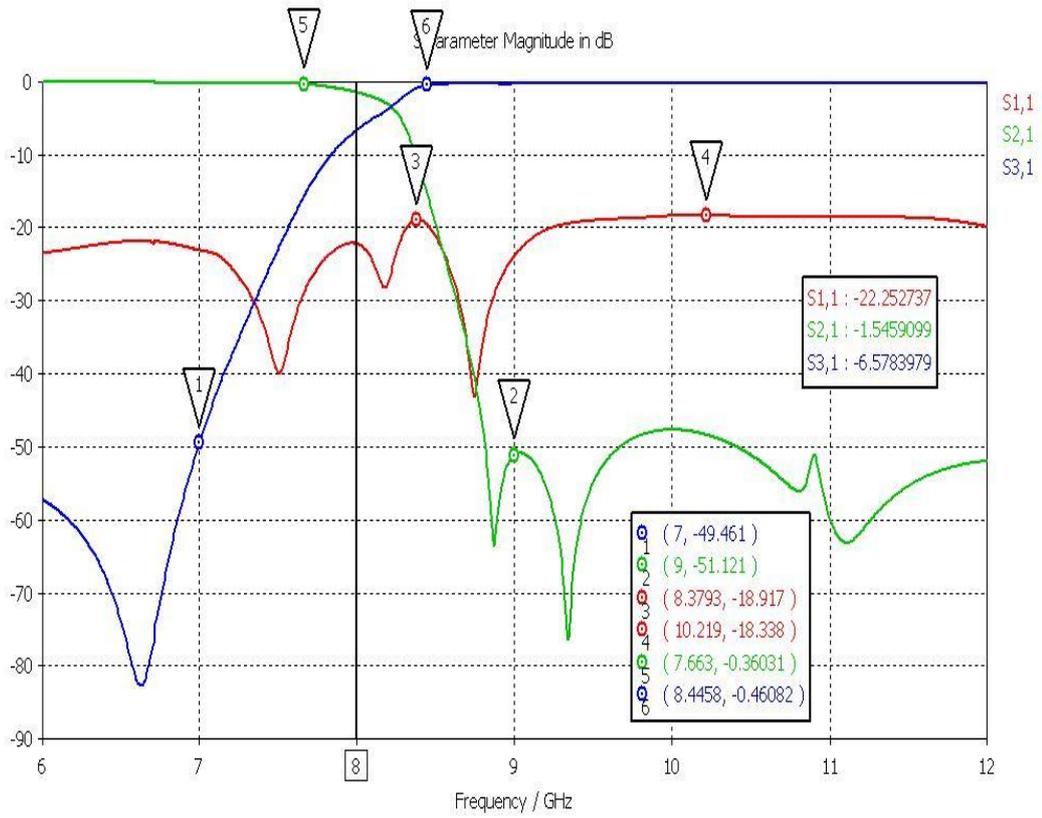
(c)
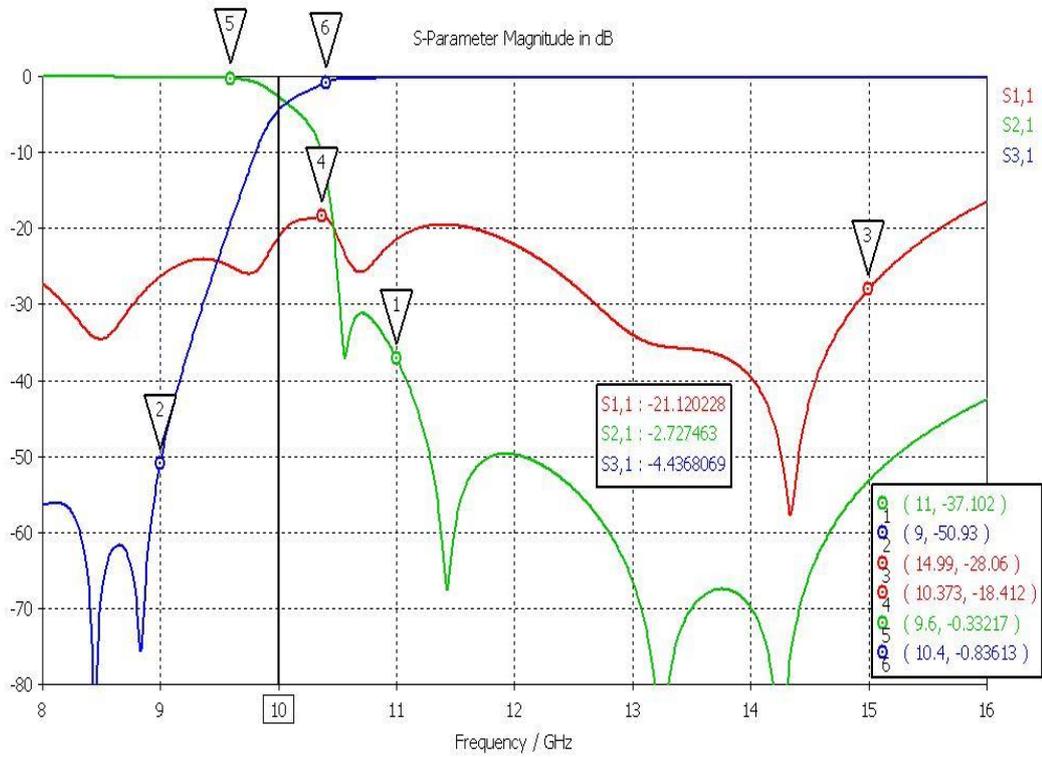
(d)

Figure 4.20 (continued) c) response of 8 GHz diplexer (d) response of 10 GHz diplexer

101
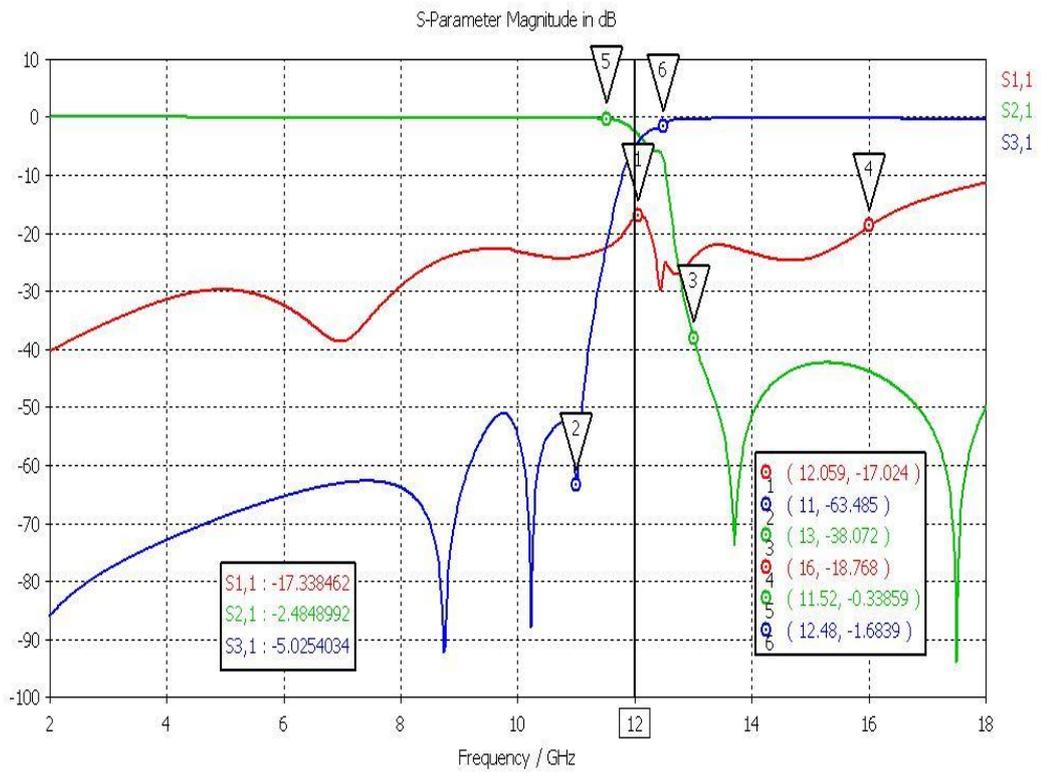
(e)
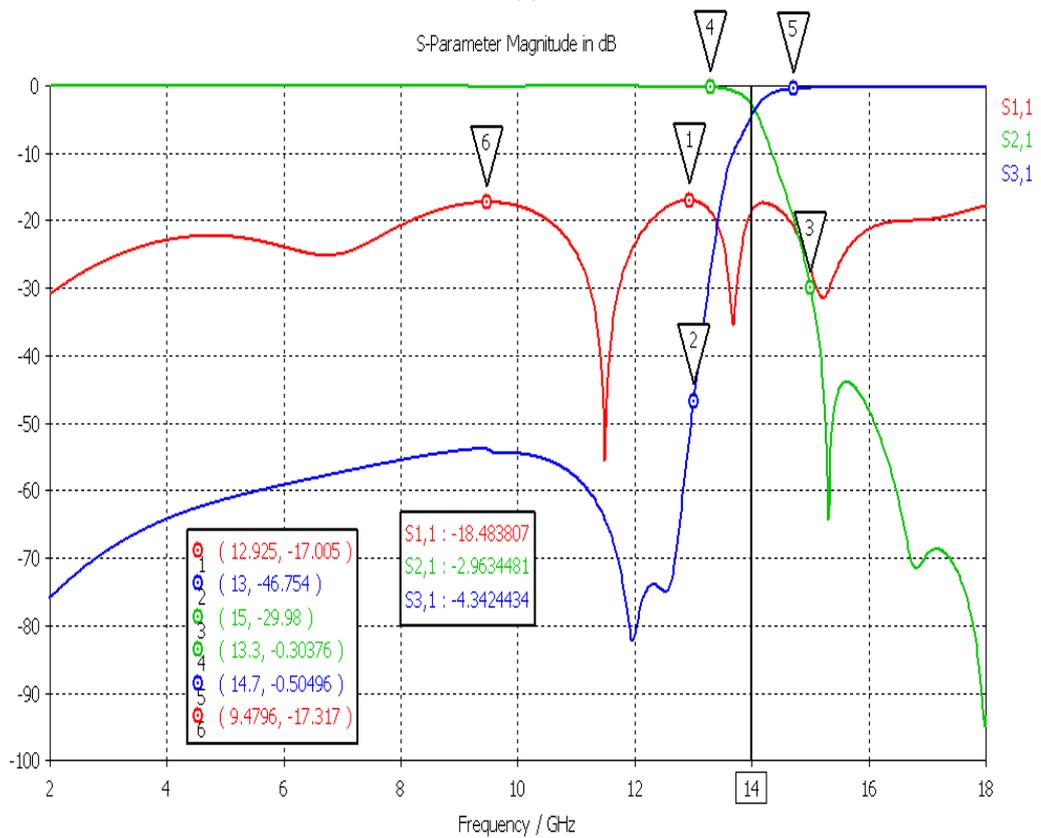
(f)

Figure 4.20 (continued) e) response of 12 GHz diplexer (f) response of 14 GHz diplexer

(g)
Figure 4. 20 (continued) (g) response of 16 GHz diplexer

CHAPTER 5

INTEGRATION OF DIPLEXERS

Having detected the cause for degradation in the performance as the frequency increases, a new batch of diplexers were manufactured according to the new launching scheme. Some minor alterations were also performed in the diplexers after 3-D EM simulations. The results for the diplexers are given in Figure 5.1 (a) to 4.1 (g). It is seen from Figure 5.1 that the measurement results are better than CST results. This is due to the utilization of tuning screws as shown in the previous chapter. These tuning screws are used to act as capacitances with very high quality factors but, if we refer to Figures 5 .2 and 5.3 we see tuning discs placed so it tells us that our initial placement of tuning screws lack in number, ie. More tuning screws are needed their positions being the locations of tuning discs. Another issue is that there were shifts in the corner frequencies of diplexers, and it was stated that these shifts could be compensated using tuning screws, hence it is shown to be so.
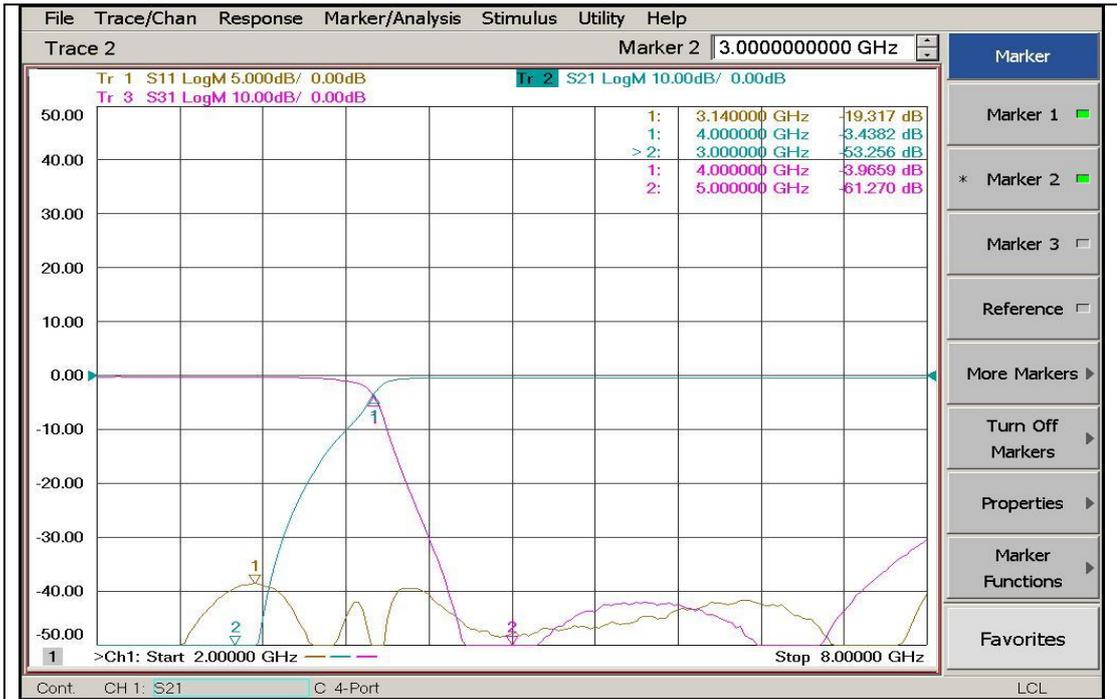
(a)
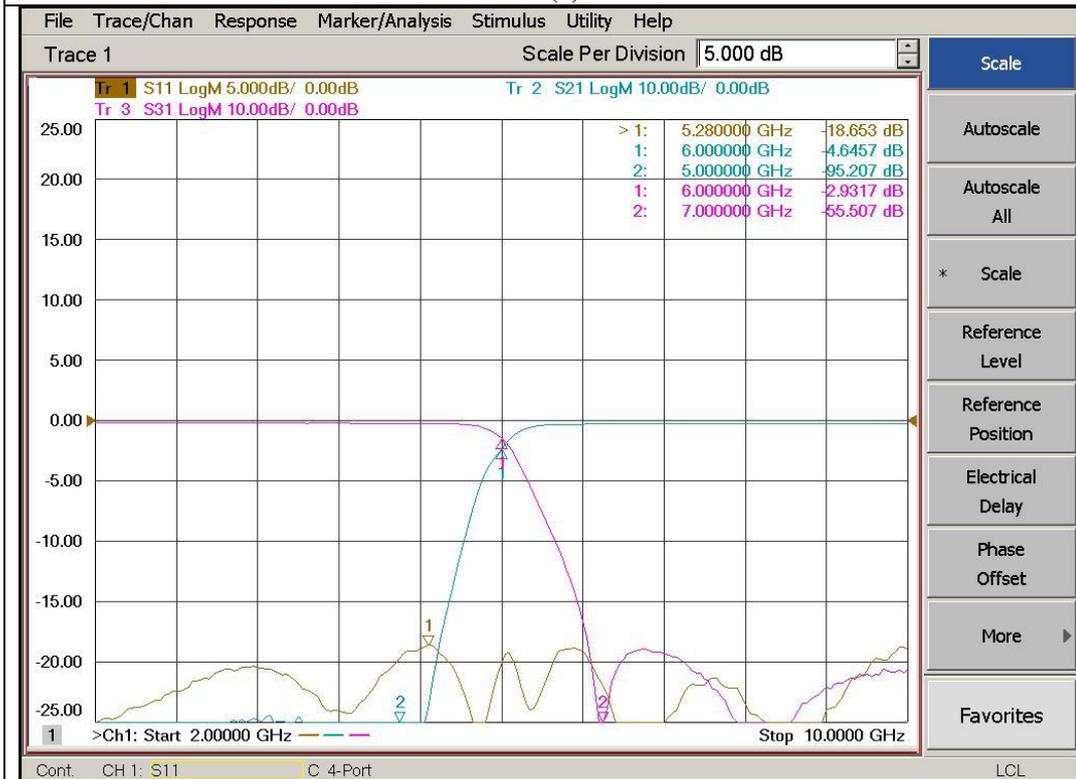
(b)

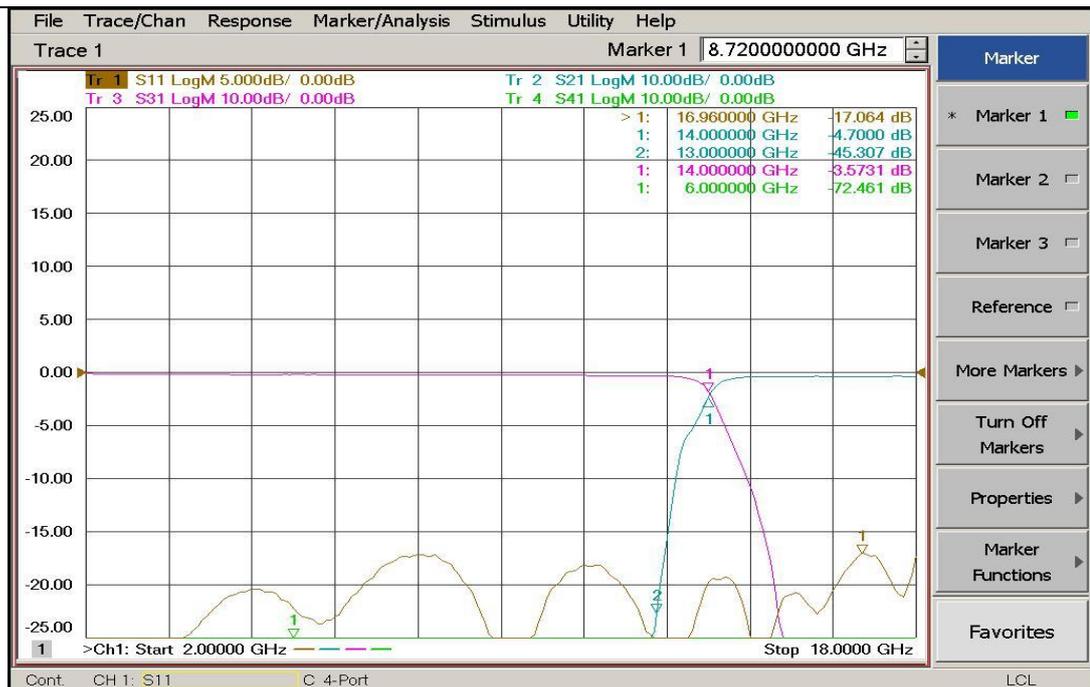**Figure 5.1 (a) 4 GHz Diplexer (b) 8 GHz Diplexer**
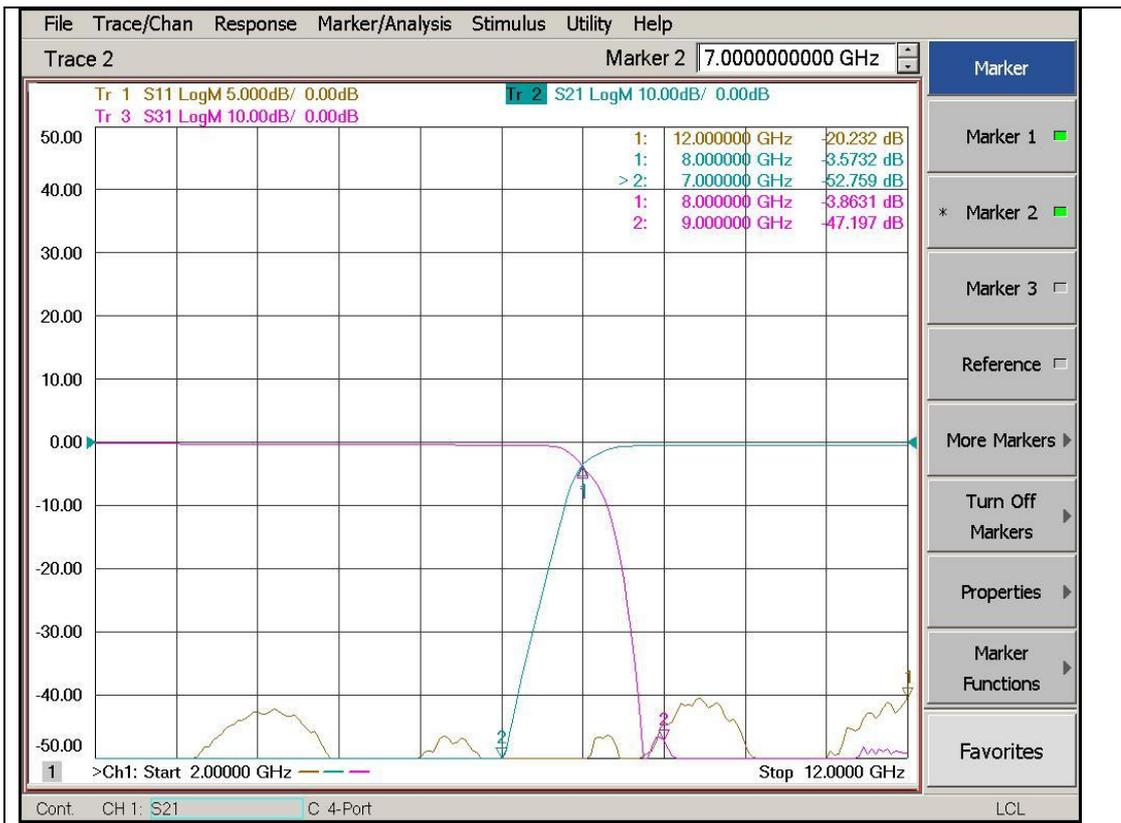
(c)
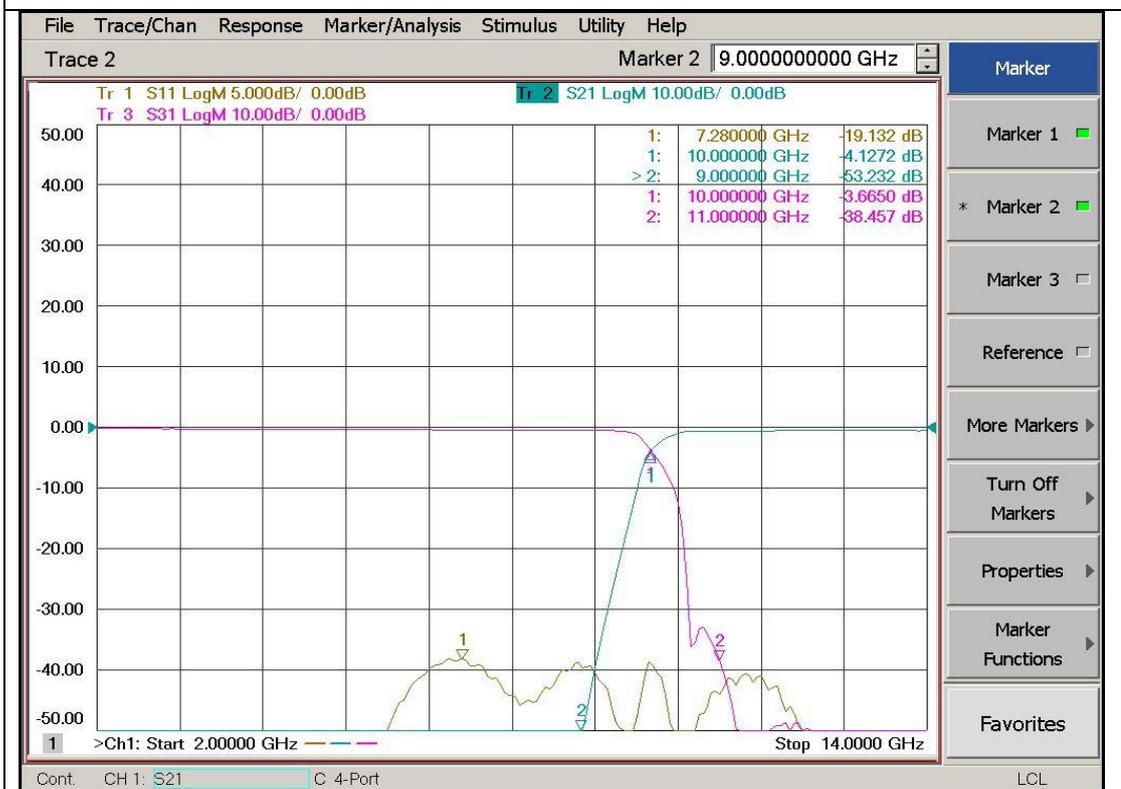
(d)

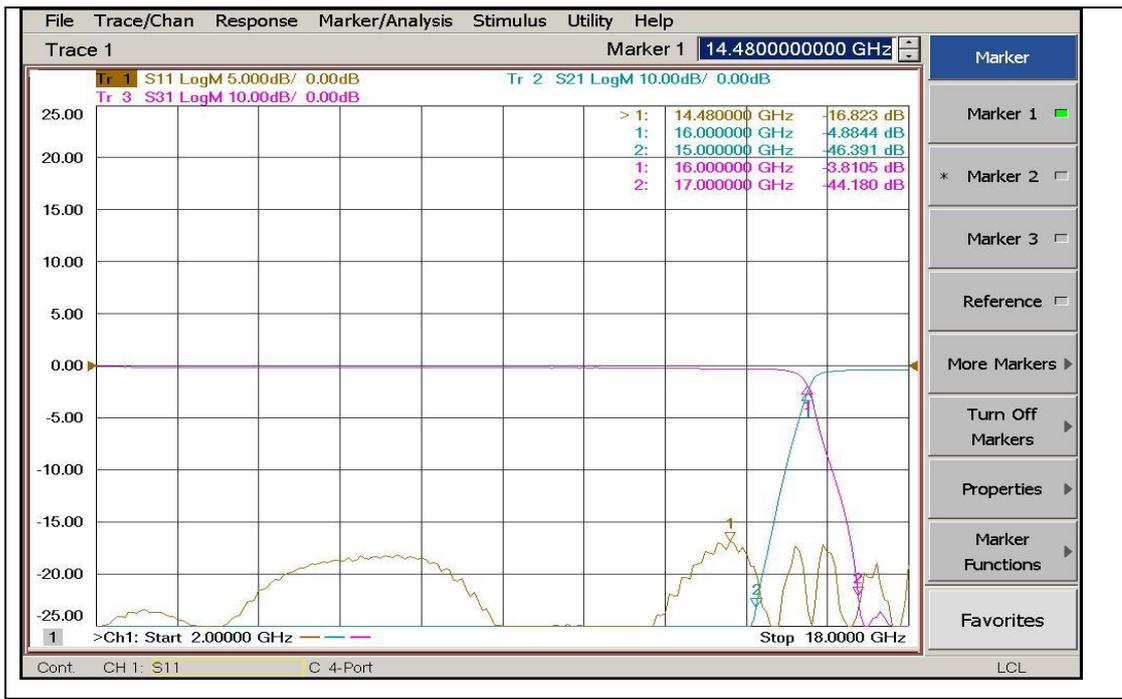**Figure 5.1 (continued) (c) 8 GHz Diplexer (d)10 GHZ Diplexer**
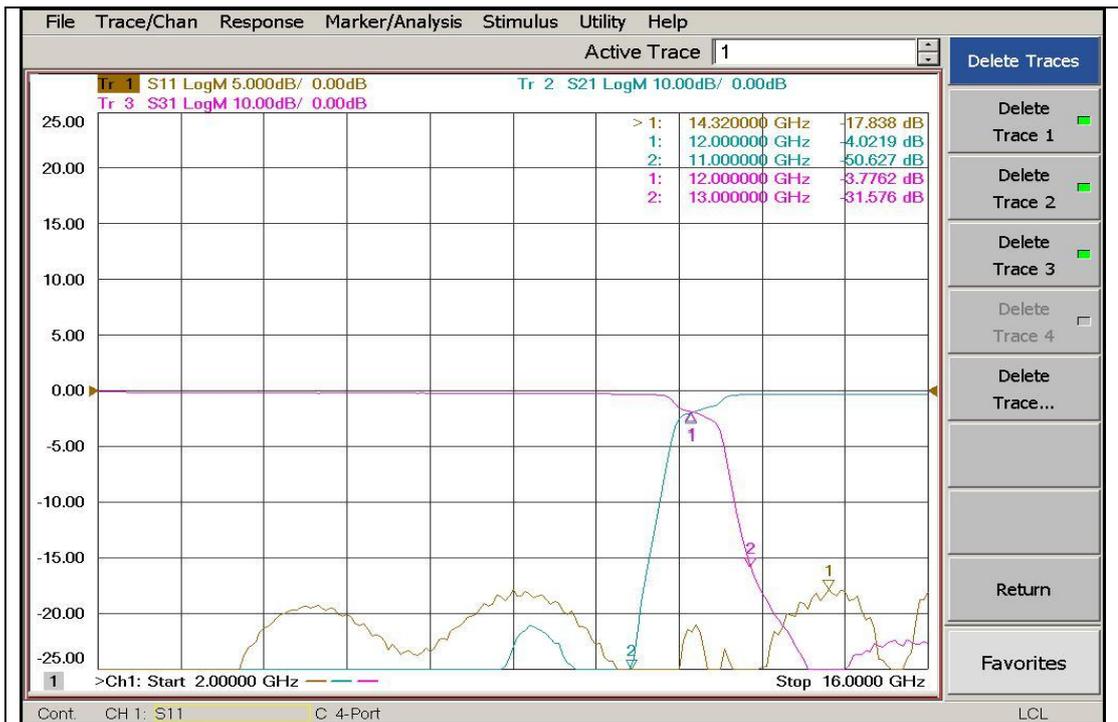
(e)

(f)

Figure 5.1 (continued) (e) 12 GHz diplexer (f) 14 GHz Diplexer

(g)

Figure 5. 1 (continued) (g) 16 GHz diplexer :Measurement results after modification
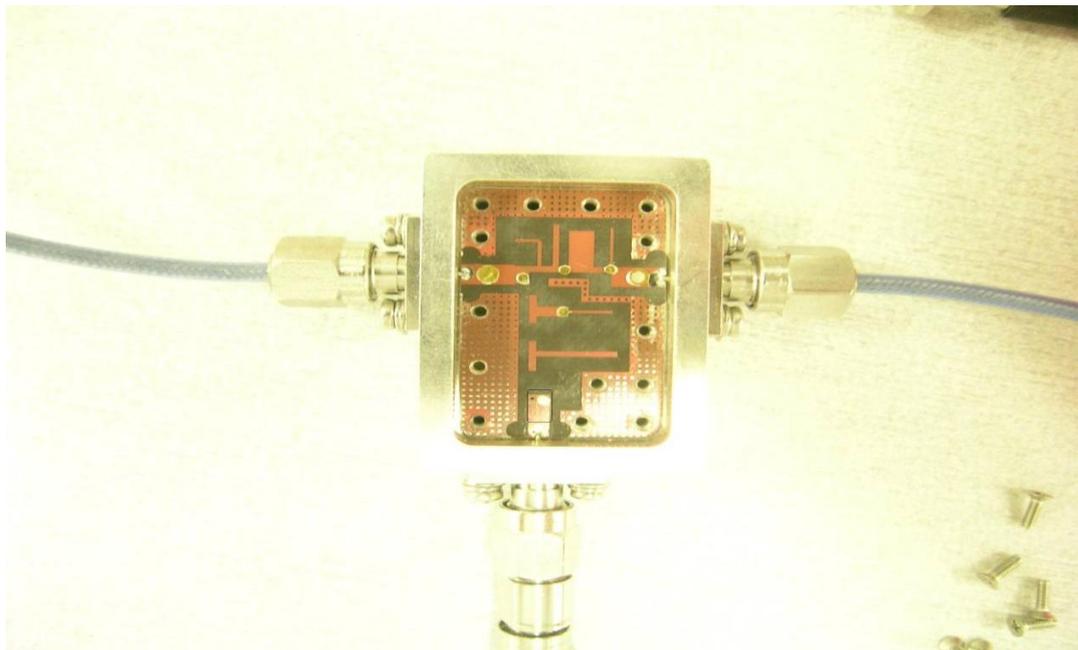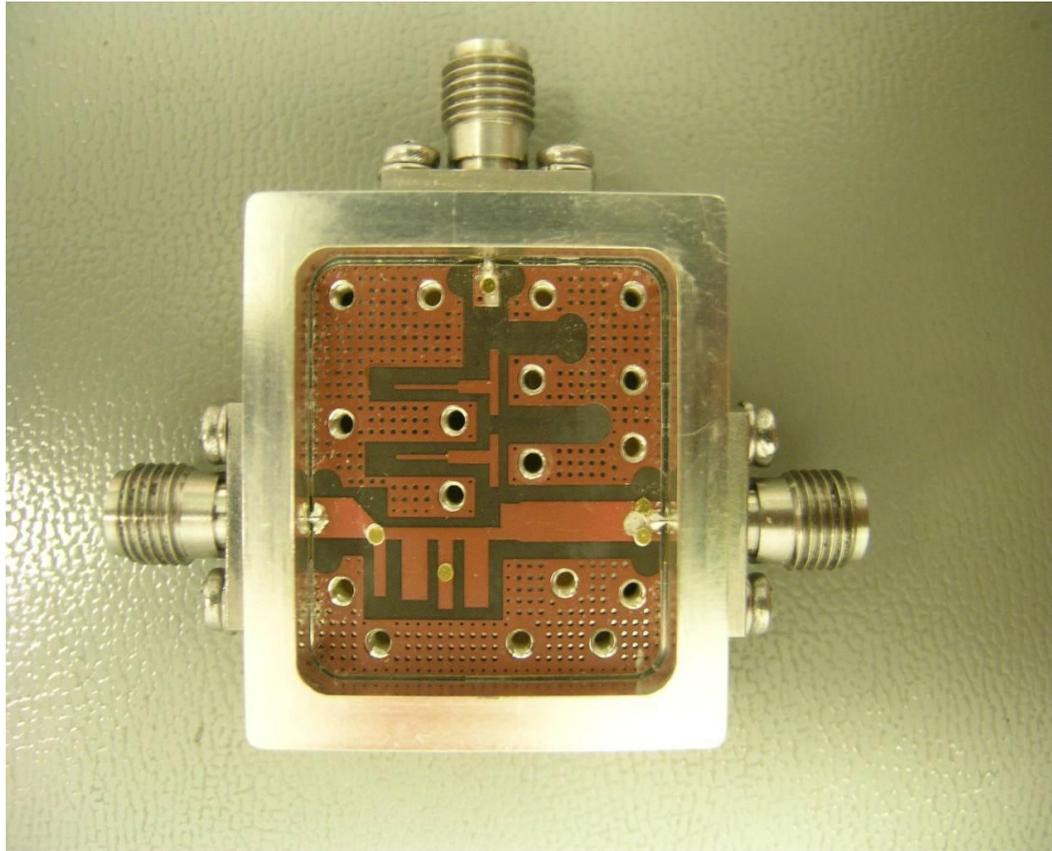

Figure 5.2 12 GHz Diplexer Layout

Figure 5. 3 14 GHz diplexer

Designing the diplexers was a great part of the work in SW_MUX synthesis. If we refer to the structure given at the end of chapter 1, there are 3 more components to be designed: 1) 2 GHz HP filter, 2) 18 GHz LP filter and finally 3) 2-18 GHz power divider.

5.1 Design of 2 GHz HP Filter

First we start with 2 GHz HP filter. The filter is designed in FILPRO with the following specifications: fp=2 GHz, fq=8 GHz and PBripple is 0.01 dB with 4 unit elements and 9 transmission zeros at DC. Next the circuit is extracted in the following way: zero-zero-NUE- zero-zero-NUE- zero-zero-NUE- zero-zero-NUE-zero. After the application of repeated Kuroda Transformations and the replacement of series OC-TL-series OC triplets by coupled line equivalents the final circuit in Figure5 .4 (c) is obtained. Likewise the circuit is optimized in ADS as an n-port

circuit as told before in earlier chapters. The optimization routine is backed by SONNET EM simulations. The N-port circuit in SONNET is shown in Figure5 .5. The final layout and its response in SONNET is shown in Figure5 .6.
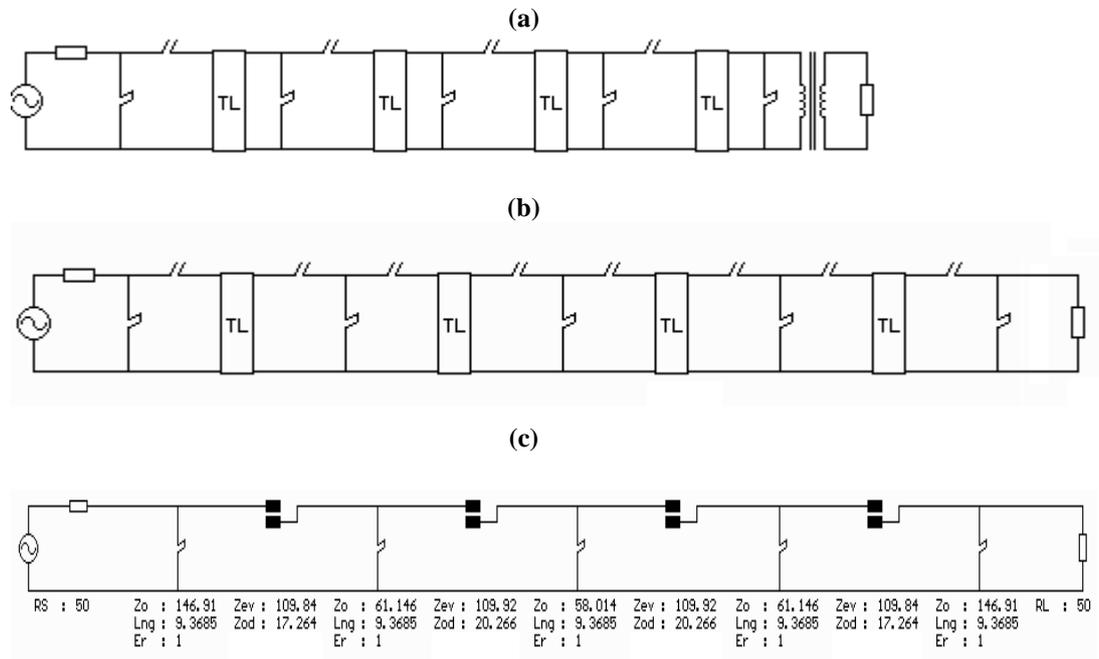
(a)

(b)

(c)

RS : 50	Zo : 146.91	Zev : 109.84	Zo : 61.146	Zev : 109.92	Zo : 58.014	Zev : 109.92	Zo : 61.146	Zev : 109.84	Zo : 146.91	RL : 50
	Lng : 9.3685	Zod : 17.264	Lng : 9.3685	Zod : 20.266	Lng : 9.3685	Zod : 20.266	Lng : 9.3685	Zod : 17.264	Lng : 9.3685	
	Er : 1		Er : 1		Er : 1		Er : 1		Er : 1	

Figure 5. 4 Design of 2 GHz HP filter in FILPRO

The final structure is SONNET is also simulated in CST ; the results and the final mechanical structure is given in Figure5 .7. It is built using a suspended substrate structure in which the air gap in both sides is 48 mils (1.2mm) and RTD 5880 5mil (0.127mm) is used as dielectric substrate. The realized module and it response is given in Figure5 .8. As expected the insertion loss is below 0.5 dB and the return loss is better than 21 dB. The last filter to be designed is the remaining band-limiting filter, i.e. 18 GHz LP filter.
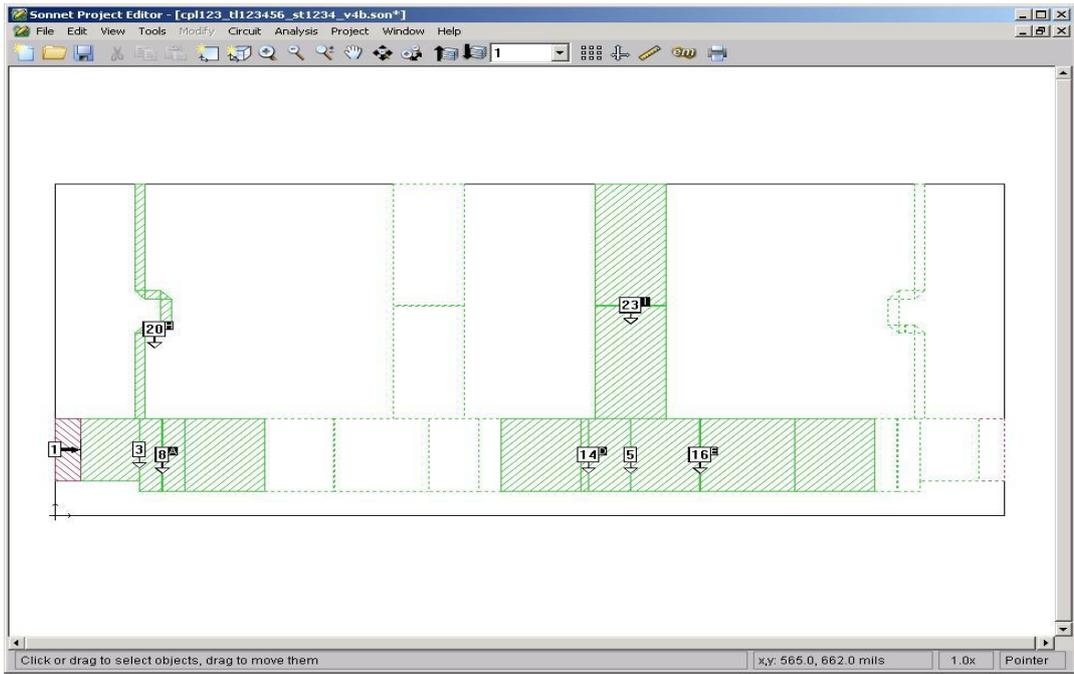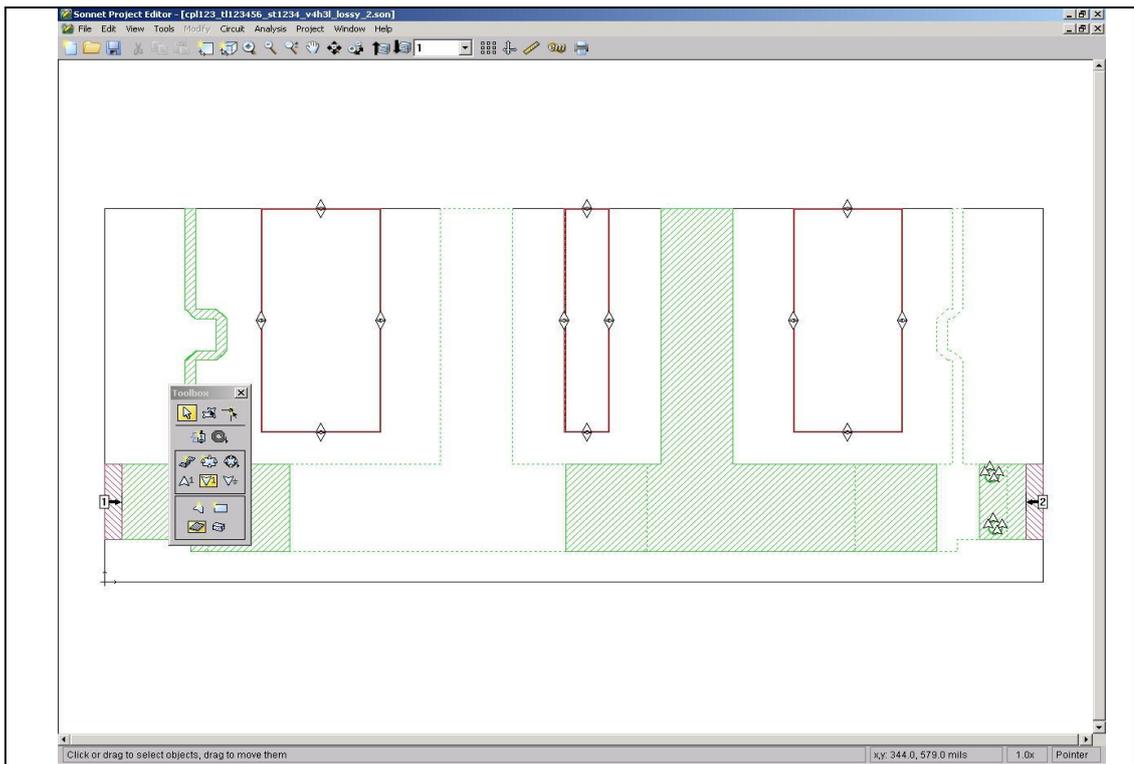
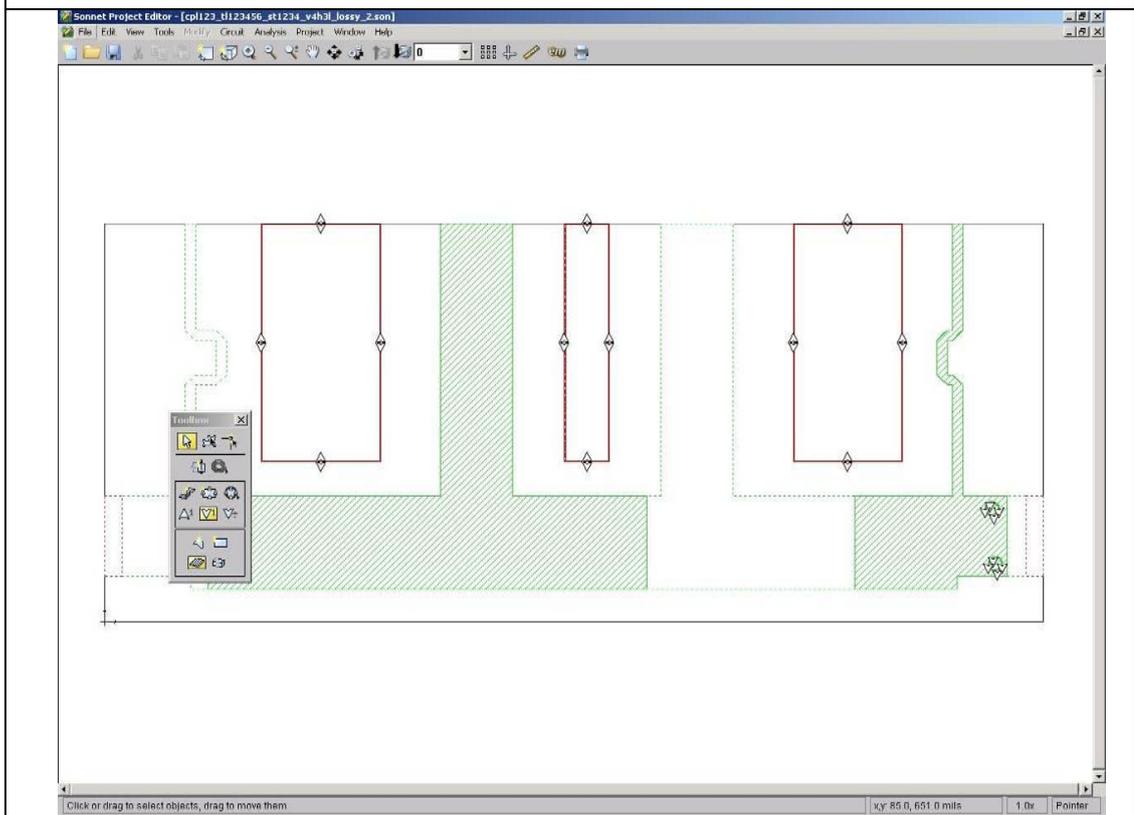(a) 2 GHz HP filter N-port layout in SONNET: top side
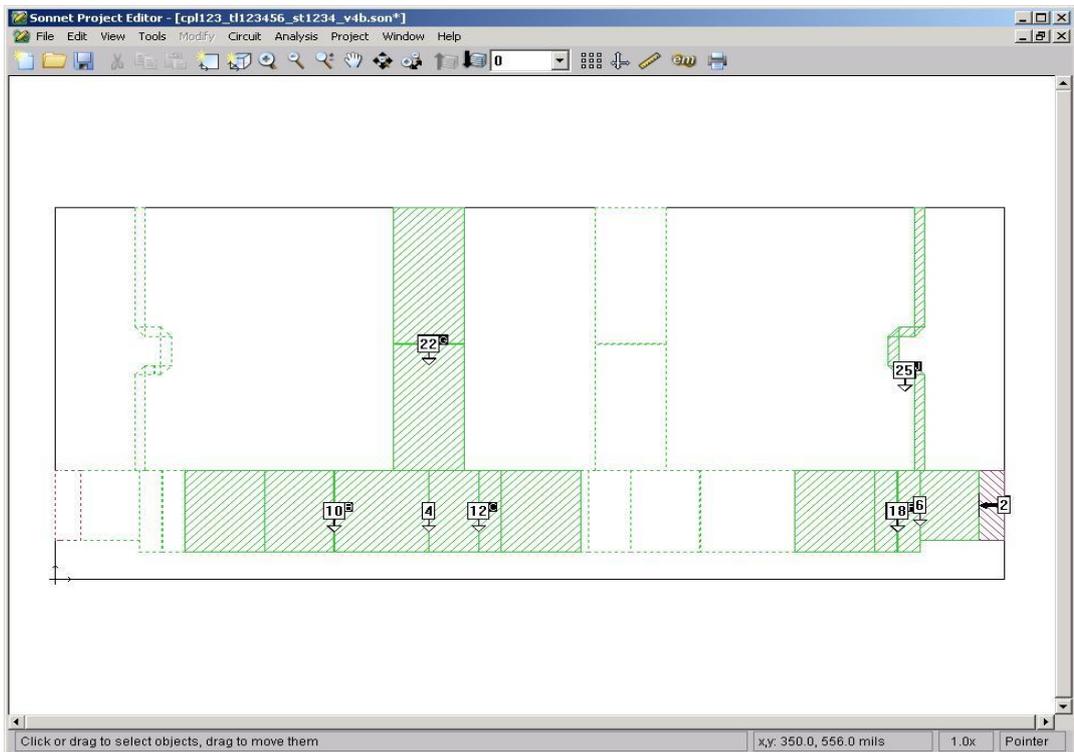
(b)
Figure 5. 5 N-port SONNET layout for 2 GHz HP filter: (a) 2 GHz HP filter N-port layout in
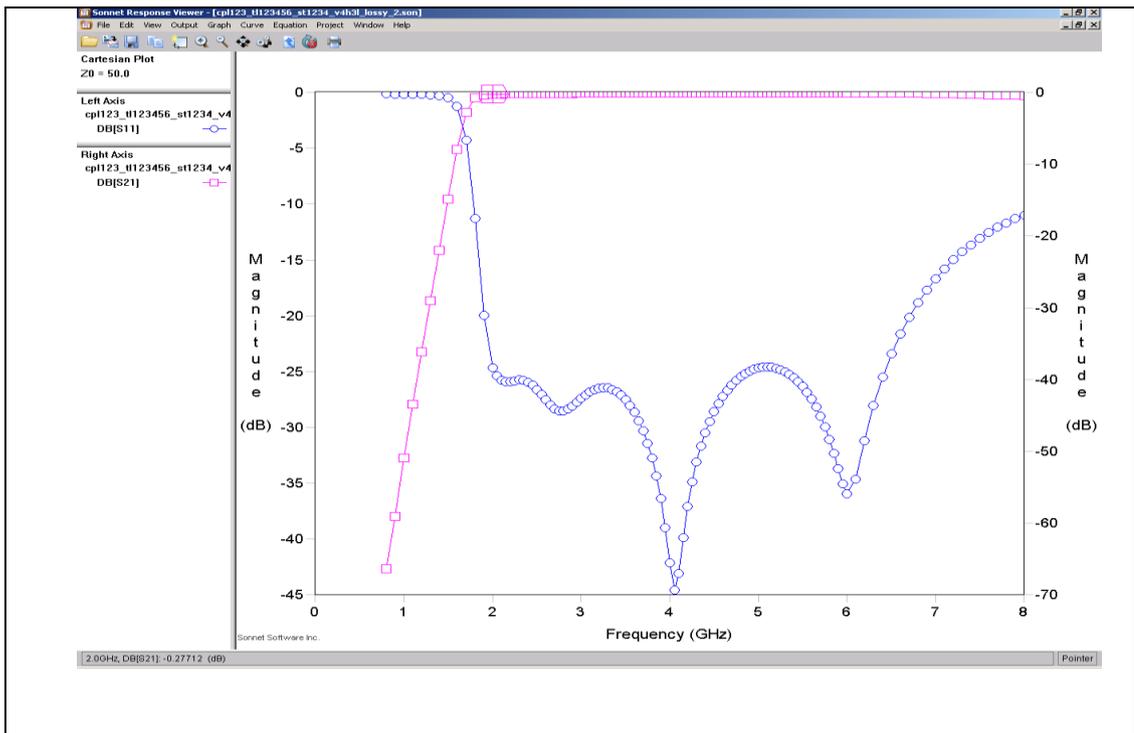SONNET: top side (b)2 GHz HP filter N-port layout in SONNET: bottom side

(a)

(b)

Figure 5.6 SONNET layout and result or 2 GHz HP filter (continued): (a) Final layout in SONNET for 2 GHz HP filter: top side (b) Final layout in SONNET for 2 GHz HP filter: bottom side

(c)
Figure 5. 6 SONNET layout and result or 2 GHz HP filter (continued): (c) 2 GHz HP filter SONNET result:
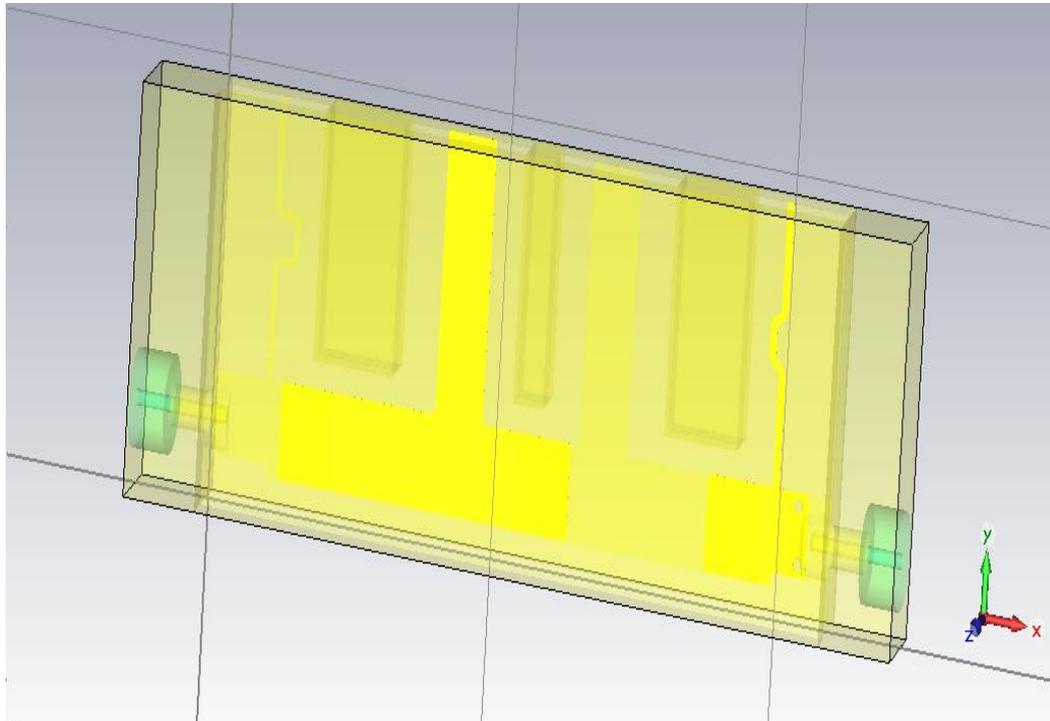
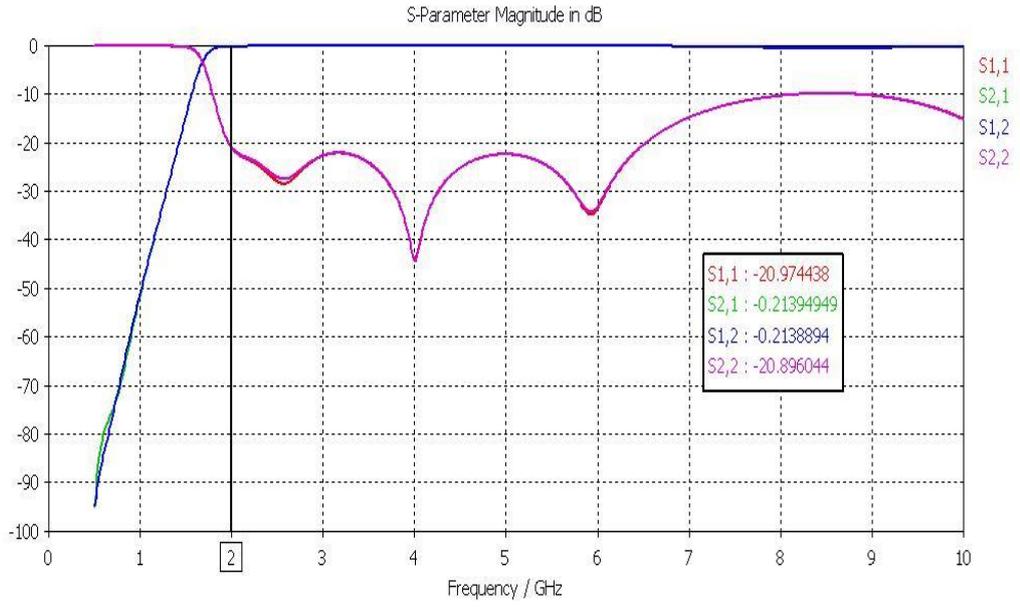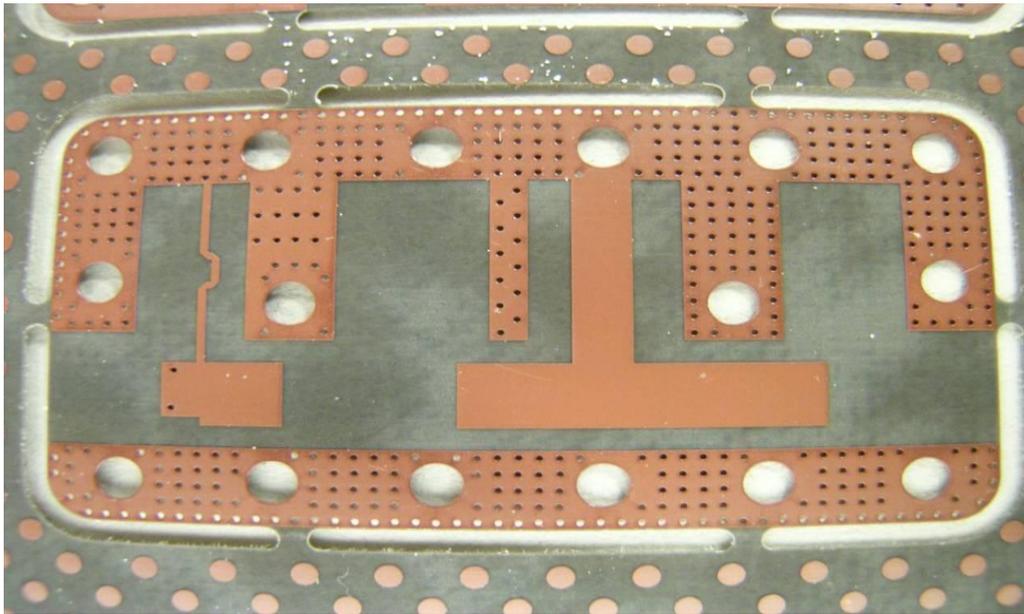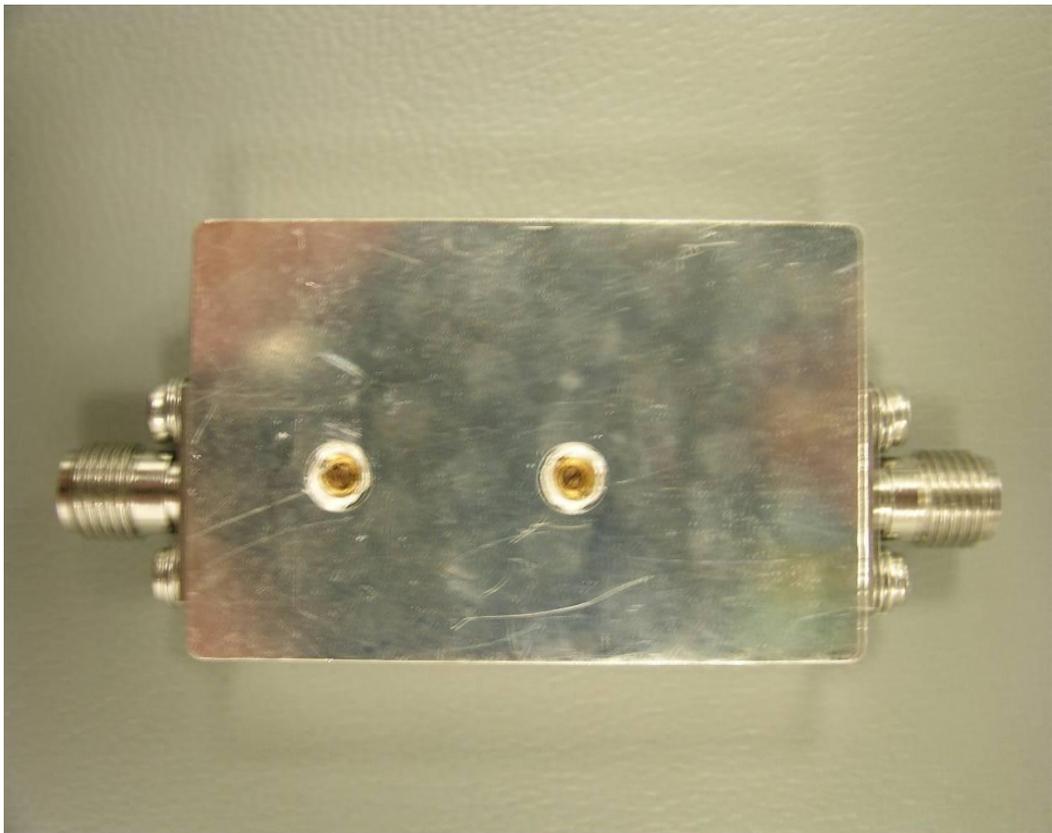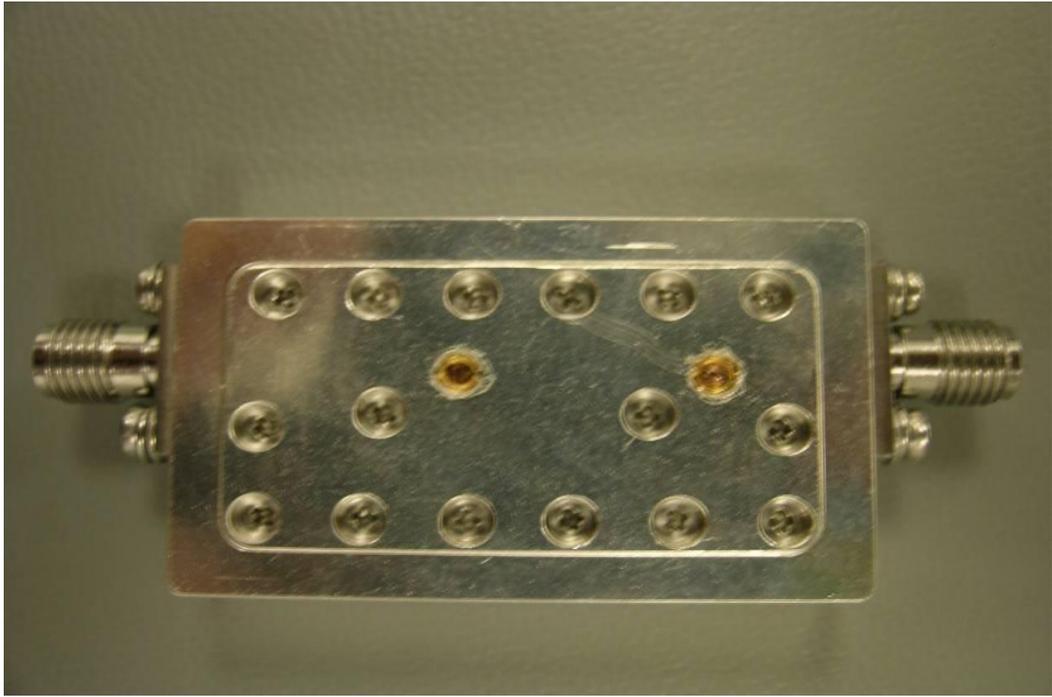**Figure 5.7 CST results and layout for 2 GHz HP filter (a) 2 GHz HP filter : CST layout**

113

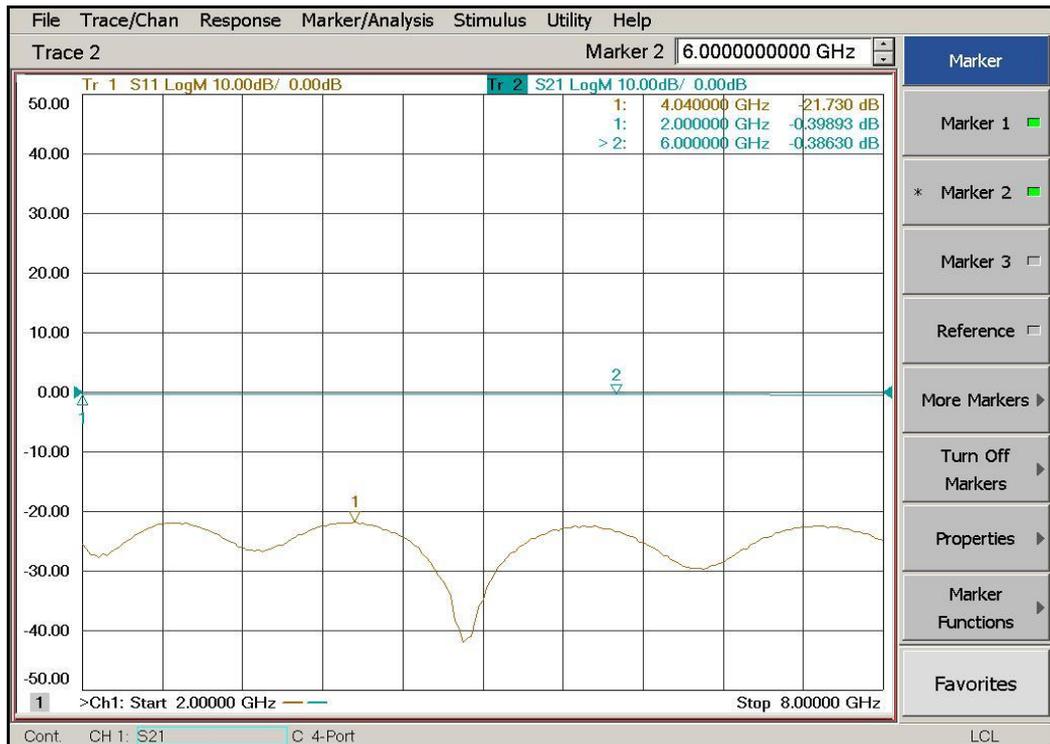**Figure 5.7 CST results and layout for 2 GHz HP filter (continued): (b) CST results**

(a)
Figure 5.8 Manufactured 2 GHz HP filter (a) PCB front side

(b)
Figure 5.8 Manufactured 2 GHz HP filter (continued): (b) Manufactured module

(c)

Figure 5.8 Manufactured 2 GHz HP filter (continued): (c) measurement results

5.2 Design of 18 GHz LP Filter

It will again be designed in FILPRO. It will have the following specifications: PBripple=0.01 dB, fp=18 GHz and fq=26 GHz with 3 unit elements and 4 transmission zeros at infinity. The unit elements are realized as transmission lines and transmission zeros at infinity will be realized as open circuited stubs as shown in Figure5 .9. It will be realized in suspended substrate form with air gaps both equal to 32 mils (0.8 mm) and using RTD 5880 5 mil (0.127 mil) thick substrate as dielectric. This filter will be EM simulated as an N_port circuit in SONNET as given in Figure5 .10. After a few runs of EM simulation the final circuit shown in Figure 5.11 was obtained. Finally the circuit will be simulated in CST the structure and results are depicted in Figure5 .12. As seen the insertion loss up to 18 GHz is better than 1 dB and the return loss is better than 20 dB. Since all the filters have been designed, it is time to design the power divider to connect even and odd numbered channels to the main manifold.
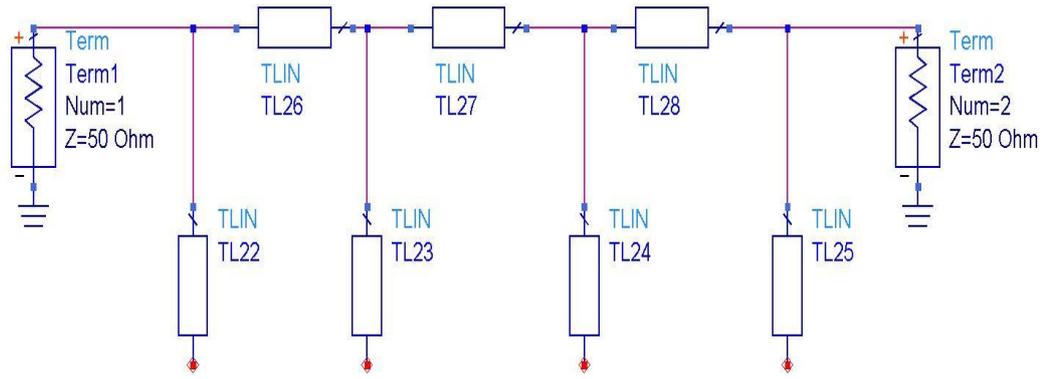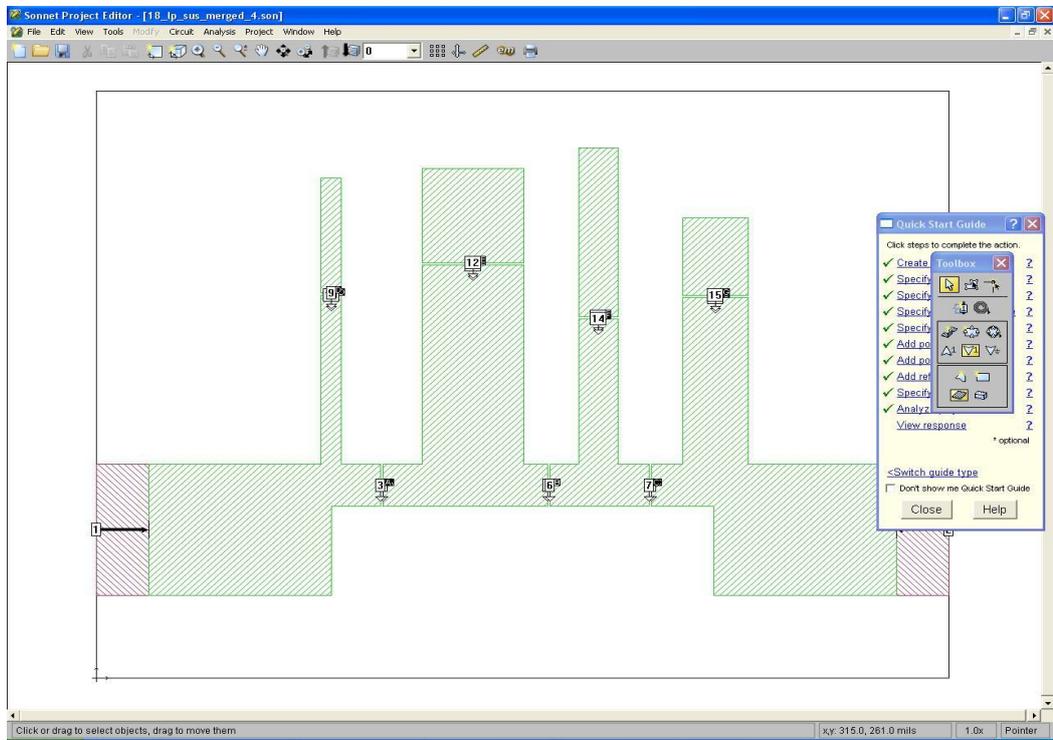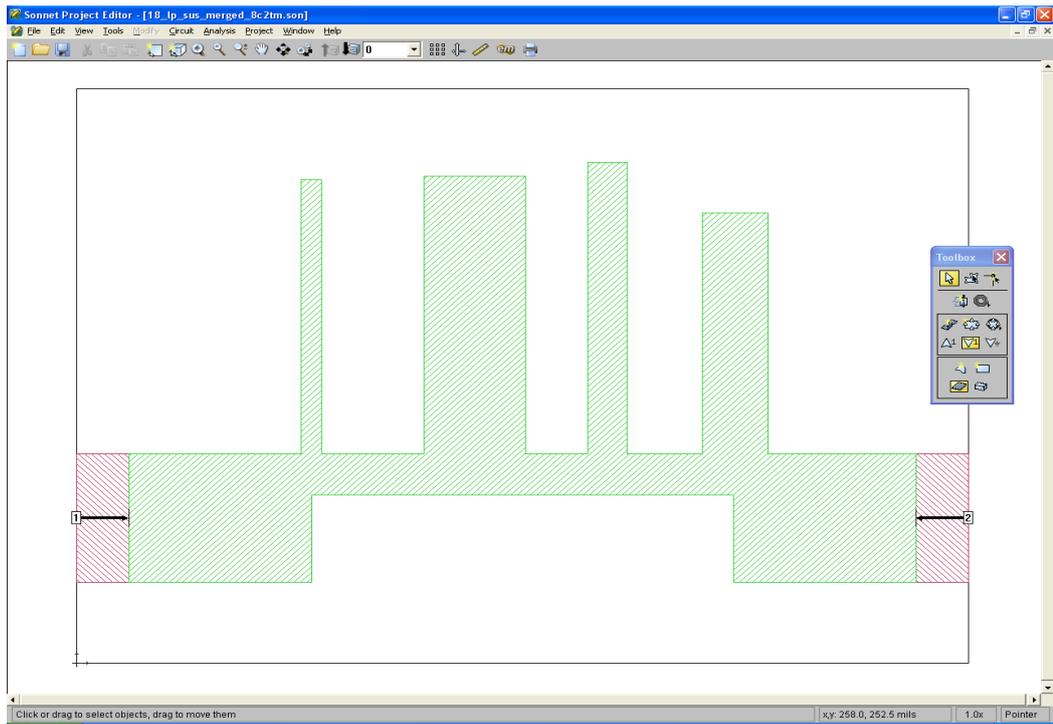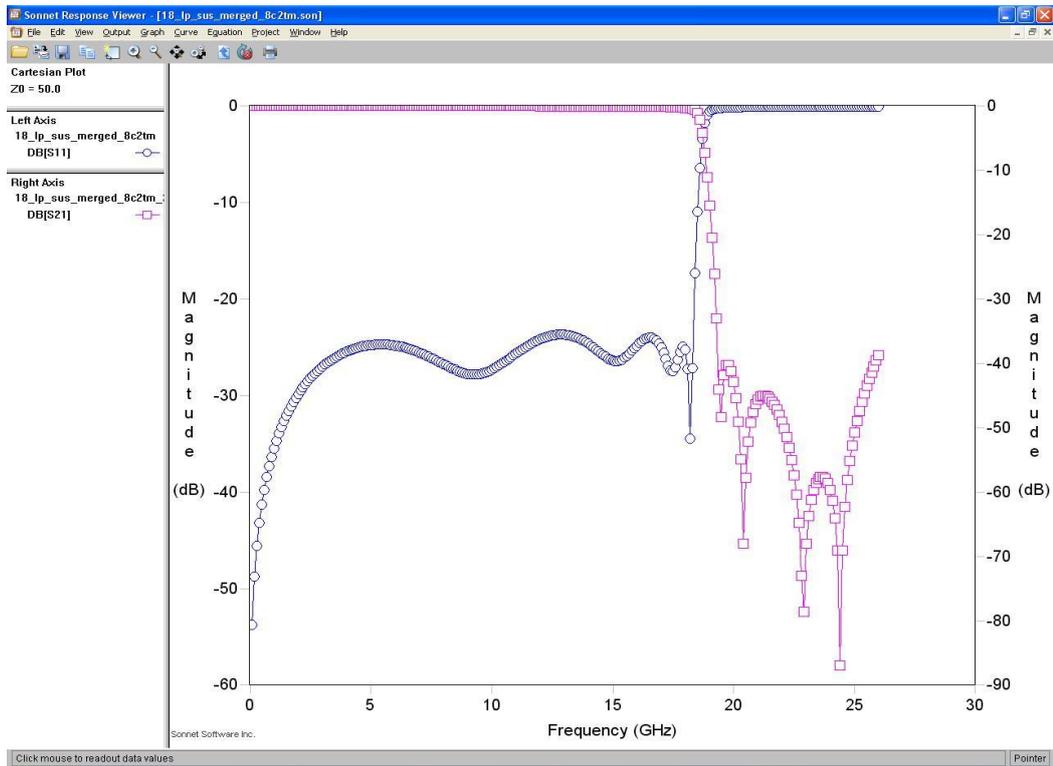
116

Figure 5.8 18 GHz LP filter
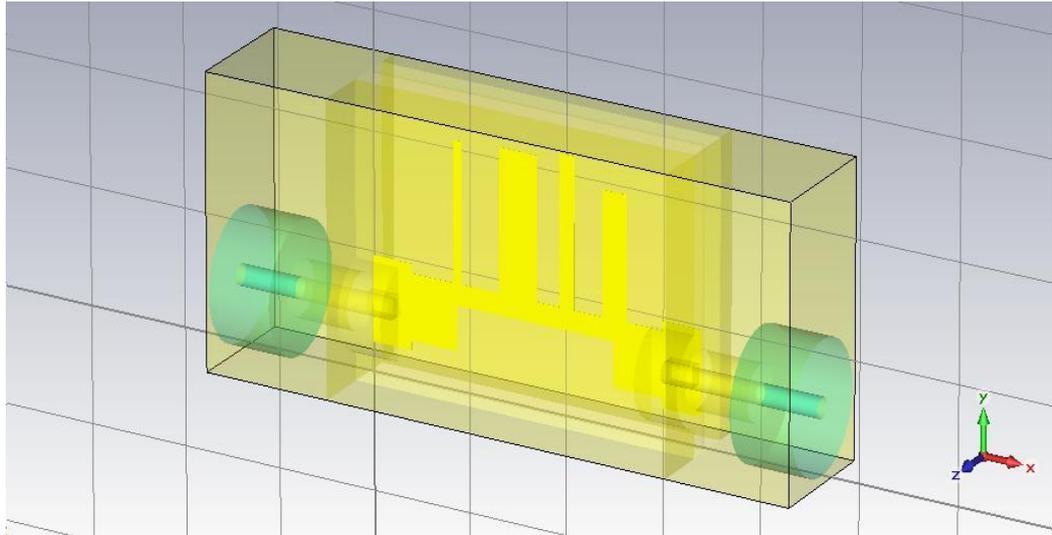

Figure 5.9 18 GHz LP filter : N-port SONNET layout

117
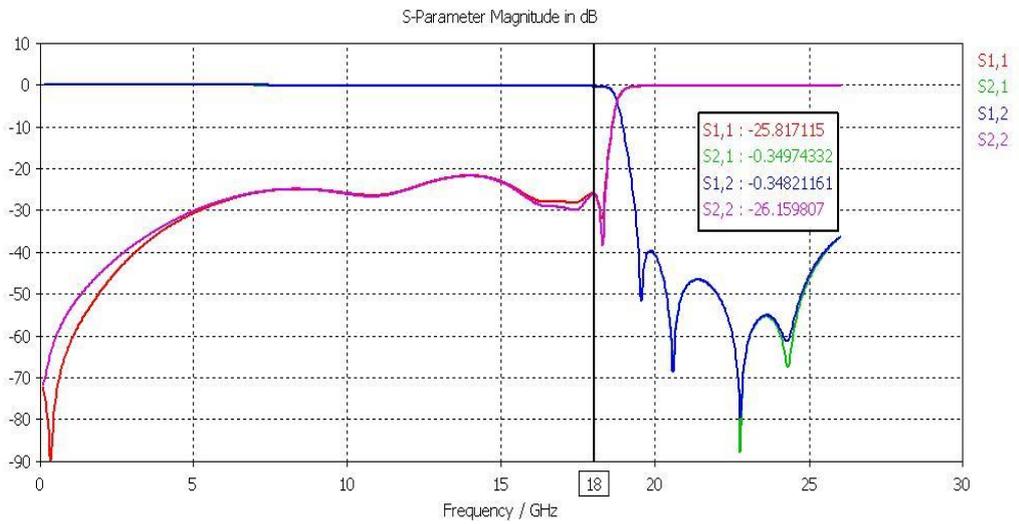
(a)

(b)

Figure 5. 10 18 GHz LP filter (a) 18 GHz LP filter final circuit (b) 18 GHz LP filter final circuit: SONNET results

(a)

(b)
Figure 5. 11 CST simulation results and 3-D structure for 18 GHz LP filter (a) 18 GHz LP filter: CST layout (b) 18 GHz LP filter : CST results

119

5.3 Design of 2-18 GHz Power Divider/Combiner

The design of 2-18 Hz Wilkinson power divider is well documented in the literature, so there s no need to oversee it here again. The circuit is to realized on 10 mil (0.254mm) alumina substrate as microstrip. 3-D EM simulation results are given in Figure 5.13. As seen from the graphs the return loss is better than 20 dB and the insertion loss varies from 3.4 dB to 4.3 dB.
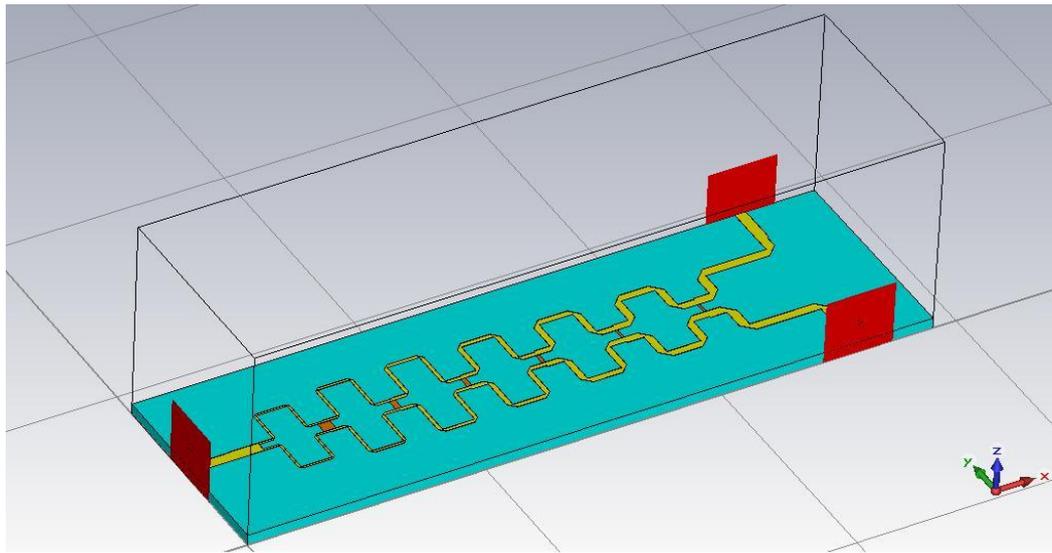
(a)
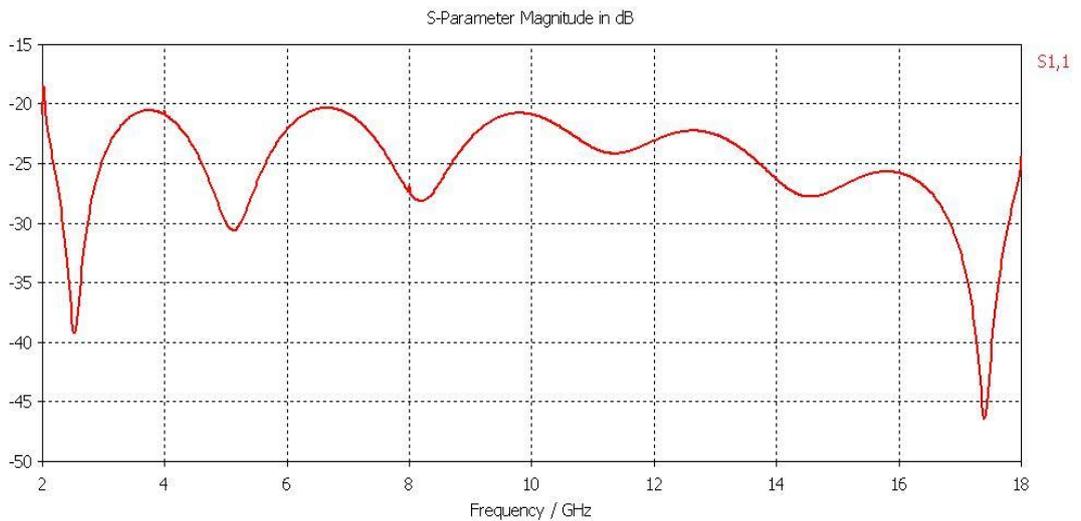
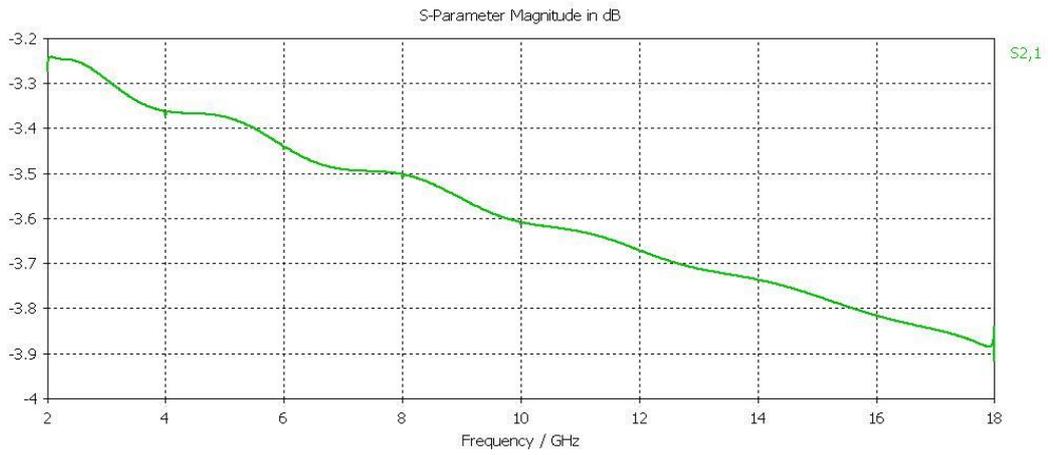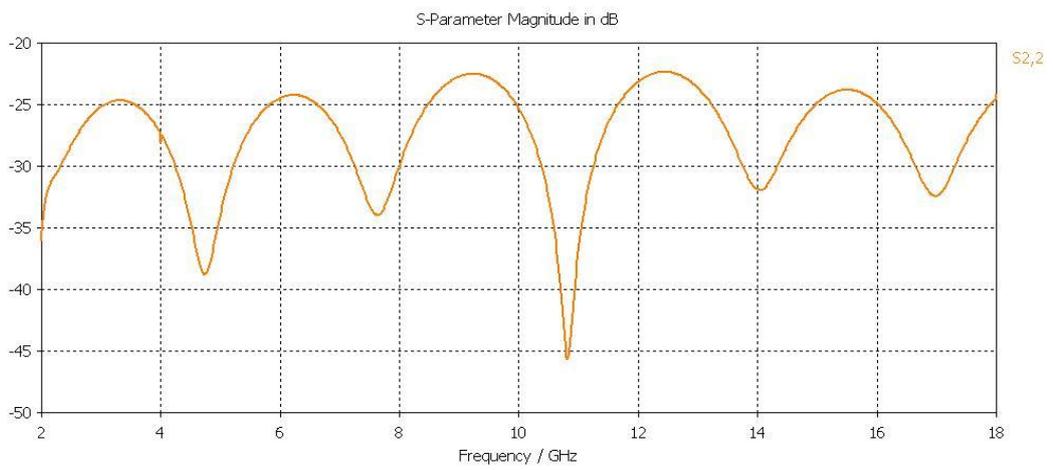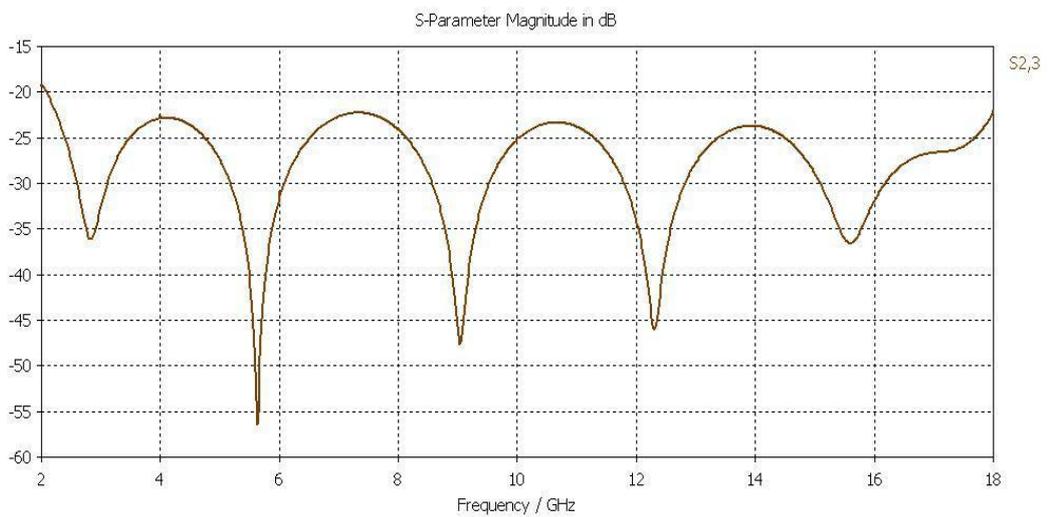**(b)**

Figure 5.12 2-18 GHz power divider (a) CST layout (b) Input return loss

120

(c)

(d)

(e)

Figure 5. 12 2-18 GHz power divider (continued) (c) Insertion loss (d) Output return loss e) Isolation between output ports

The design of 2-18 GHz power divider enables us the construction of the targeted SW_MUX. It will be done easier if a step by step approach is taken instead of forming the multiplexer right at a time.

5.4 Design Of Manifold Multiplexers

The first step should be forming the manifolds for even and odd numbered channels. For odd numbered channels the manifold will consist of 18 GHz LP, 14 GHz diplexer, 10 GHz diplexer, 6 GHz diplexer and 2 GHz HP connected as in this order as depicted in Figure 5.13. The ADS results are given in Figure 5 14. This structure is also simulated in CST and those results are given in Figure5 .18. The measurement results and multiplexer layouts are given in Figure 5.16. For even numbered channels the manifold will consist of 16 GHz diplexer, 12 GHz diplexer, 8 GHz diplexer and 4 GHz diplexer connected as in this order as depicted in Figure 5.20. ADS results are given in Figure 5.18. This structure is also simulated in CST and those results are given in Figure 5.19. The measurement results and multiplexer layouts are given in are given in Figure5 .20.

Figure 5. 13 Manifold for odd numbered channels
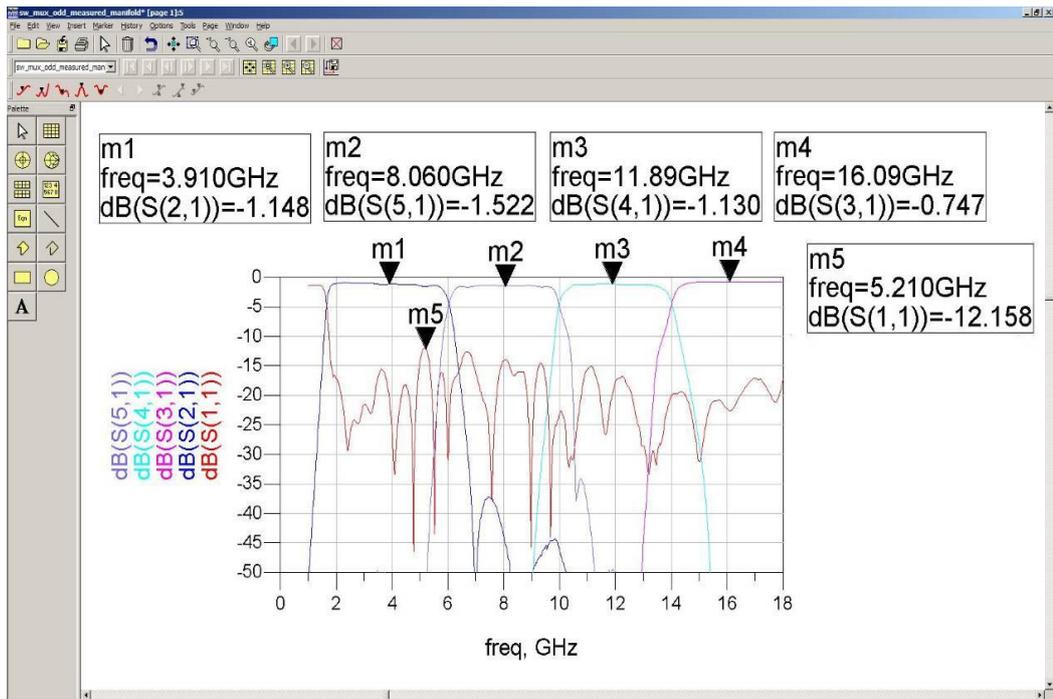
Figure 5. 14 ADS Simulation of the manifold for odd numbered channels
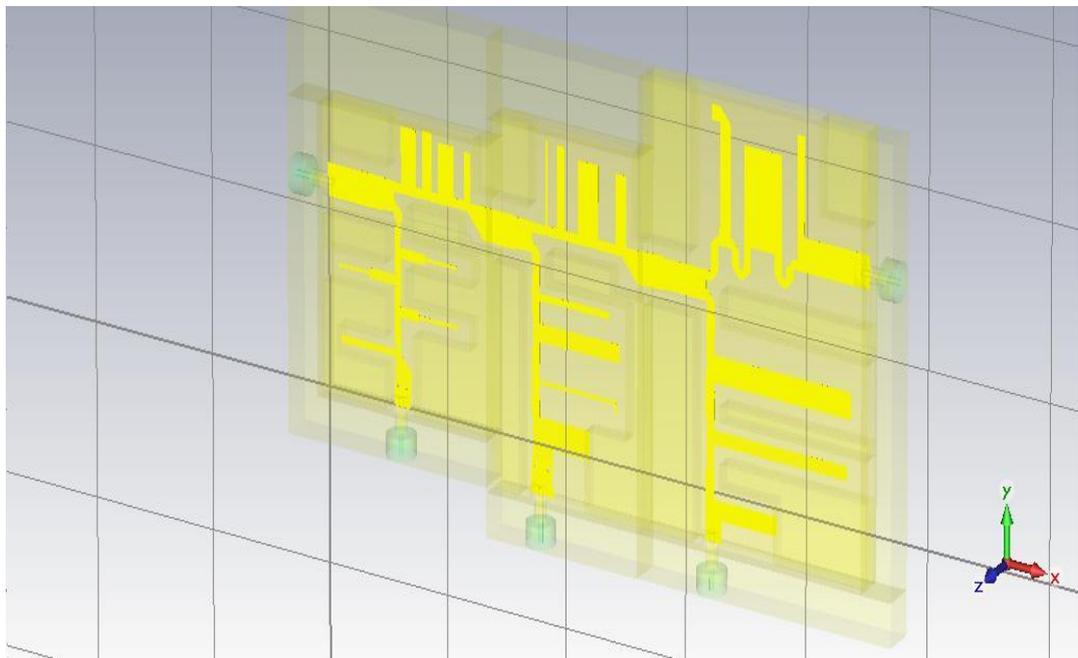
(a)

Figure 5.15 (a) Manifold for odd numbered channels : CST layout
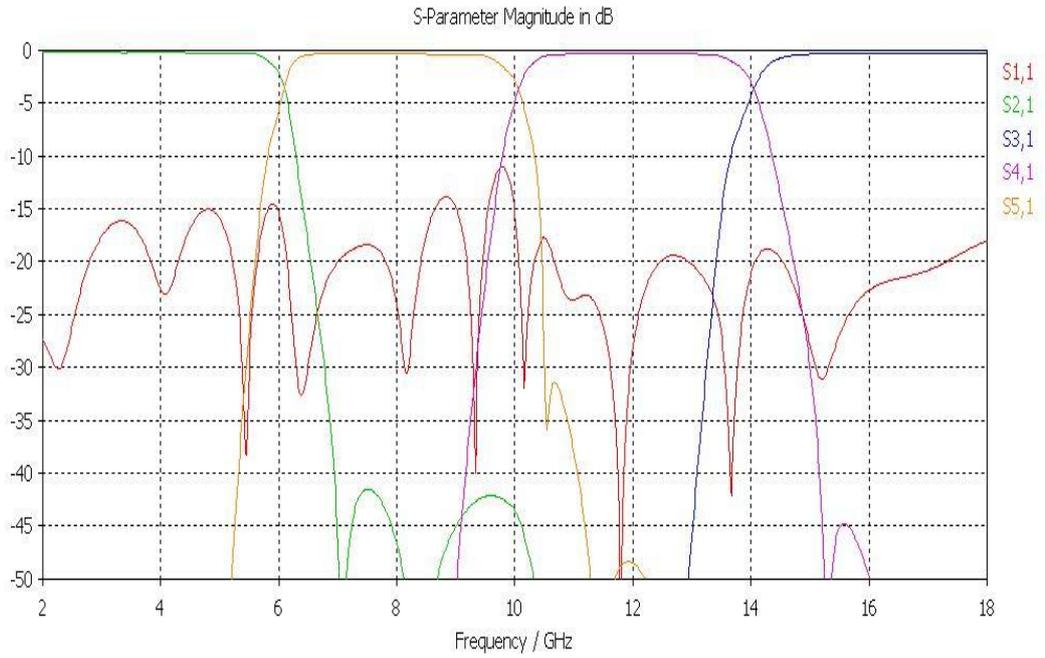
(b)

Figure 5.15 Manifold for odd numbered channels (continued) (b) CST results

Figure 5. 16 Measurement results and layout for manifold for odd numbered channels (a) Measurement Results

124

(b)
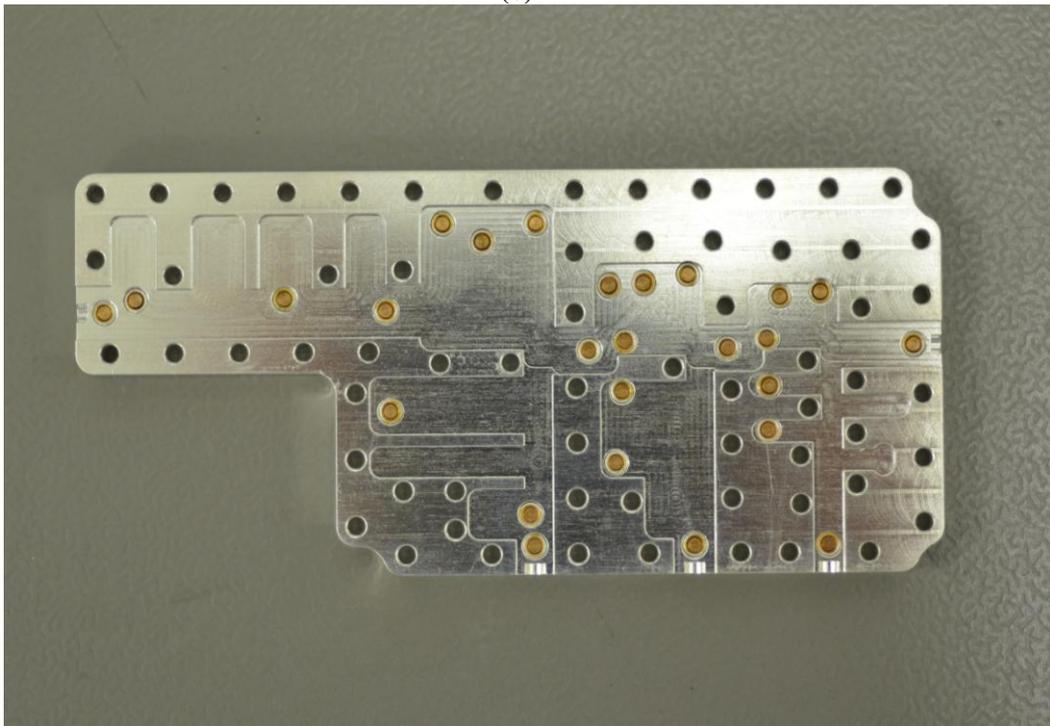
(c)
Figure 5.16 Measurement results and layout for manifold for odd numbered channels (continued) (b) Manifold Layout (c) Top Cover

It is observed that especially for the return loss the measurements results are better than both ADS and CST results. The return loss over entire band is better than 14 dB and the insertion loss at the cross over frequencies is are better than 4dBc with respect to center frequency of the channels they belong to.The insertion loss increases as expected as the frequency decreases because the lower frequency diplexers are at the end of the manifold. The rejection 1 GHz away form each crossover frequency is better than 30 dBc's complying with the rejection specification of 25 dBc. It is observed that especially for the return loss the measurements results are better than both ADS and CST results. The return loss over entire band is better than 13 dB and the insertion loss at the cross over frequencies is are better than 4dBc with respect to center frequency of the channels they belong to.The insertion loss increases as expected as the frequency decreases because the lower frequency diplexers are at the end of the manifold. The rejection 1 GHz away form each crossover frequency is better than 30 dBc's complying with the rejection specification of 25 dBc.
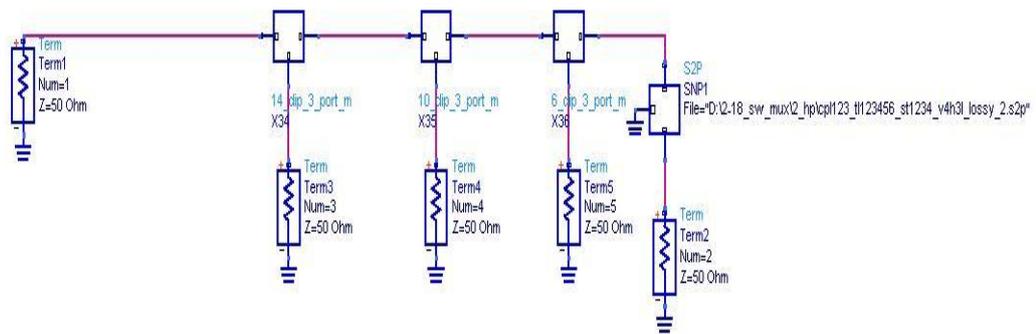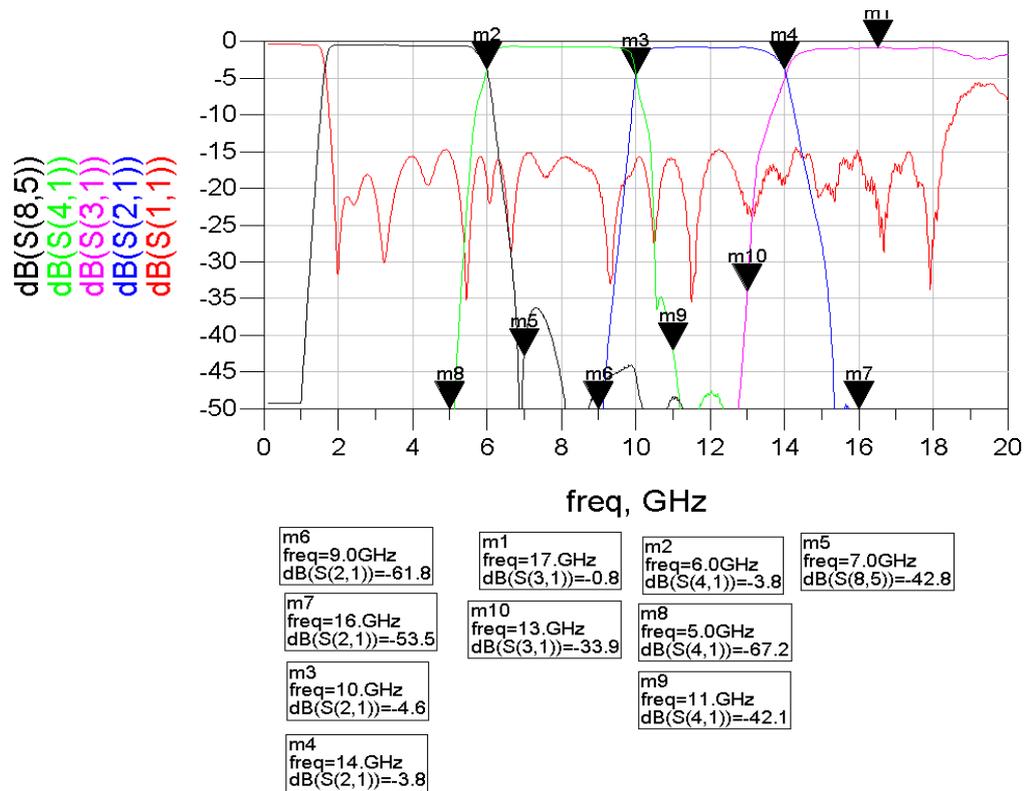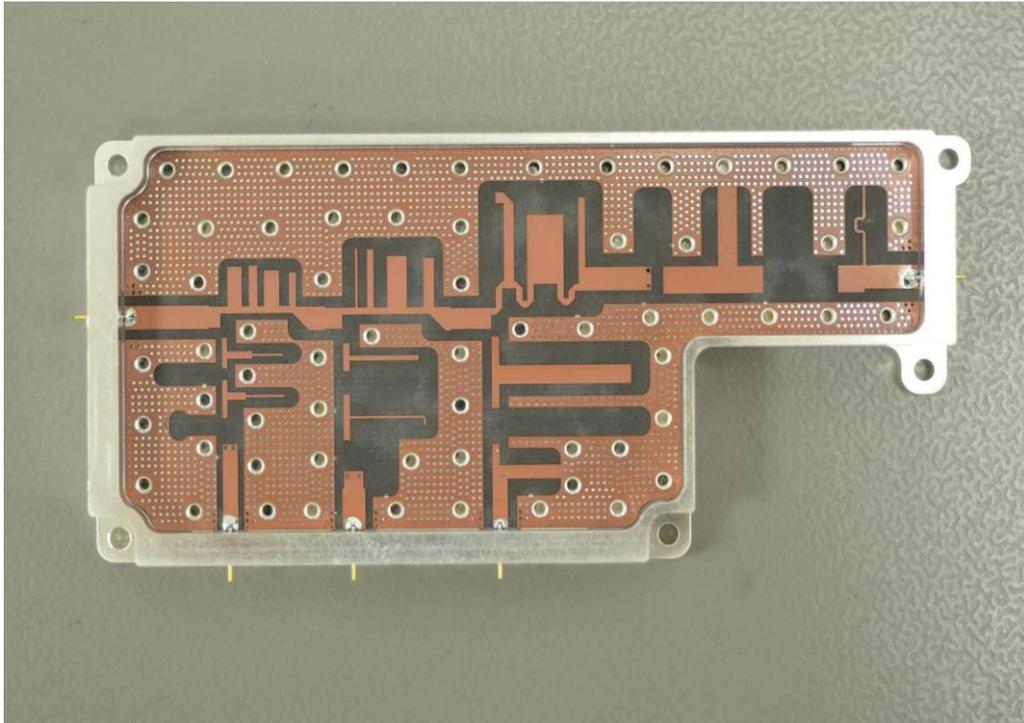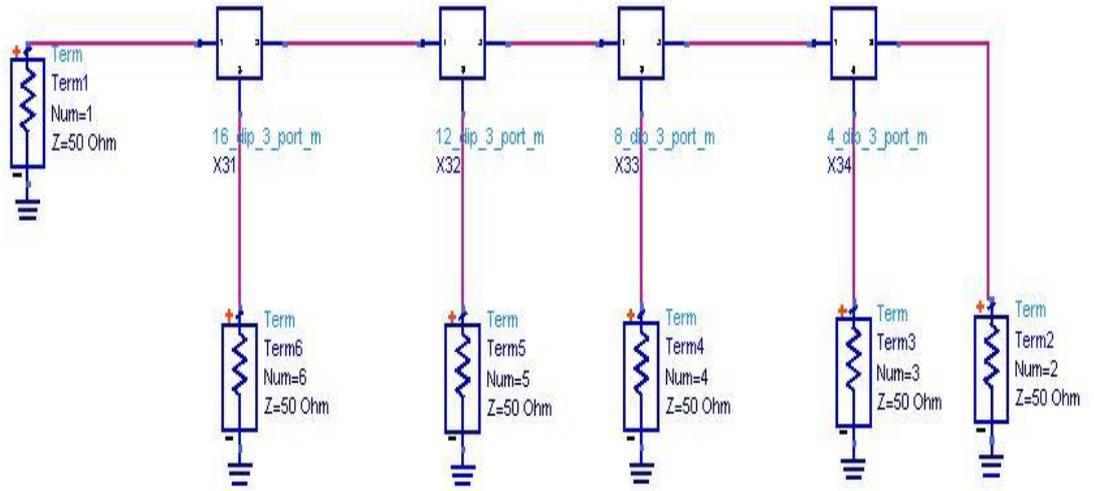
Figure 5. 17 Manifold for even numbered channels
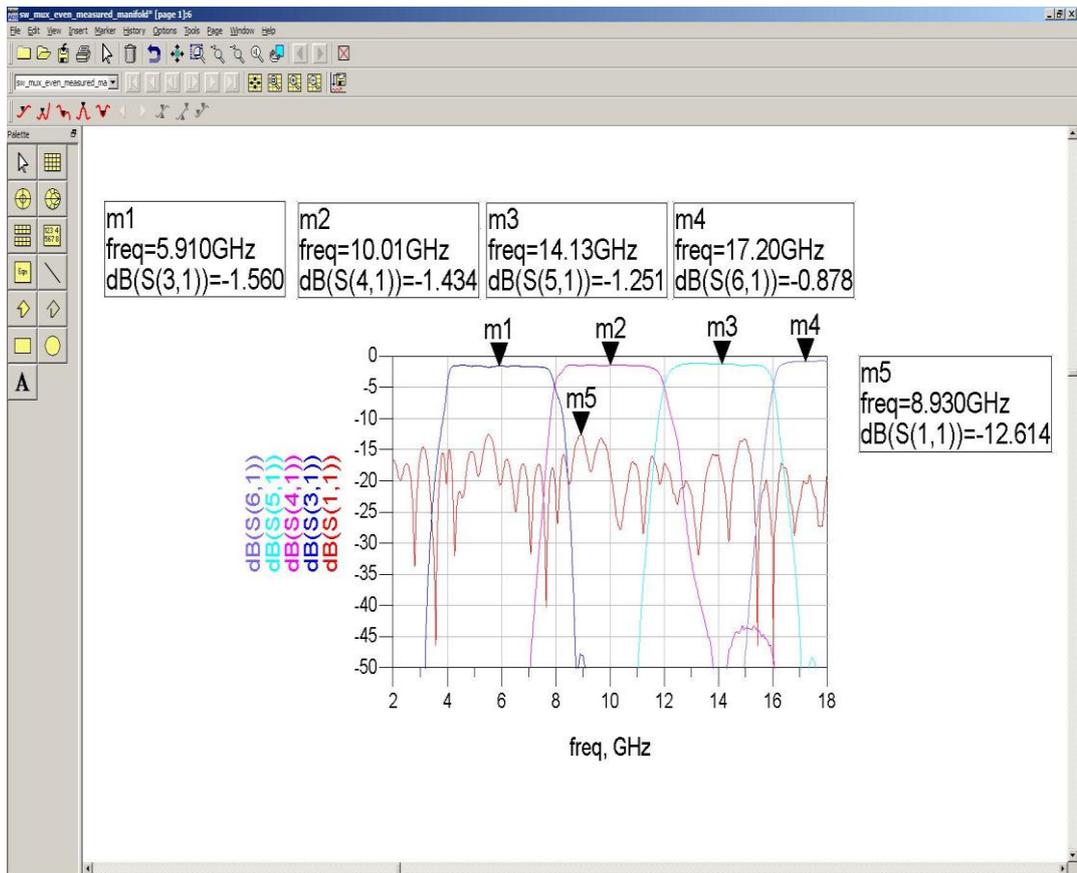
Figure 5. 18 ADS Simulation of the manifold for even numbered channels

127
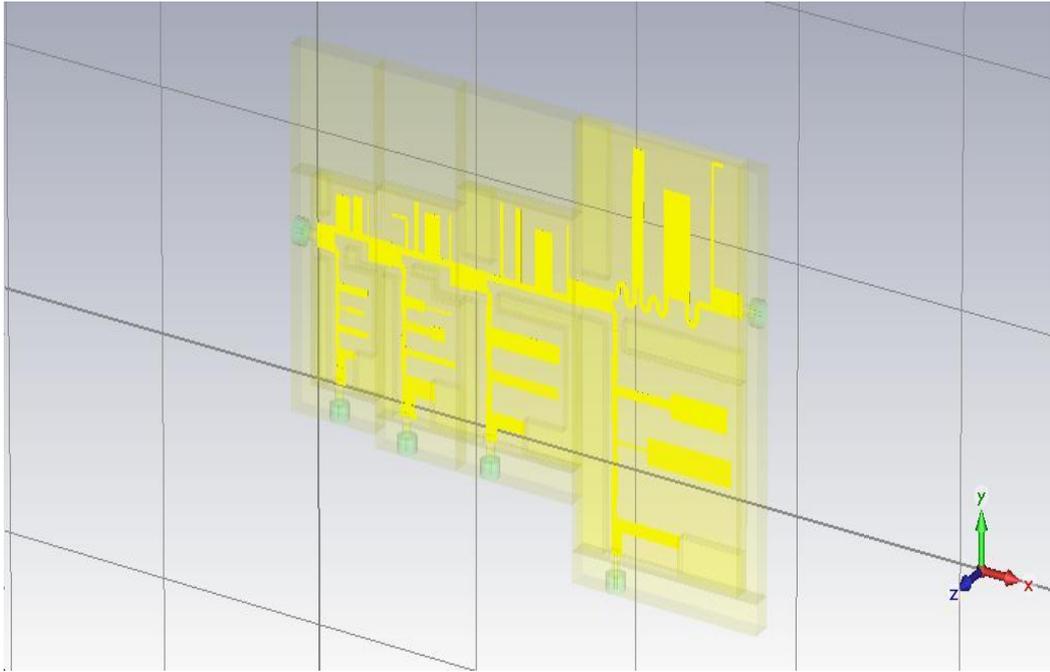
(a)
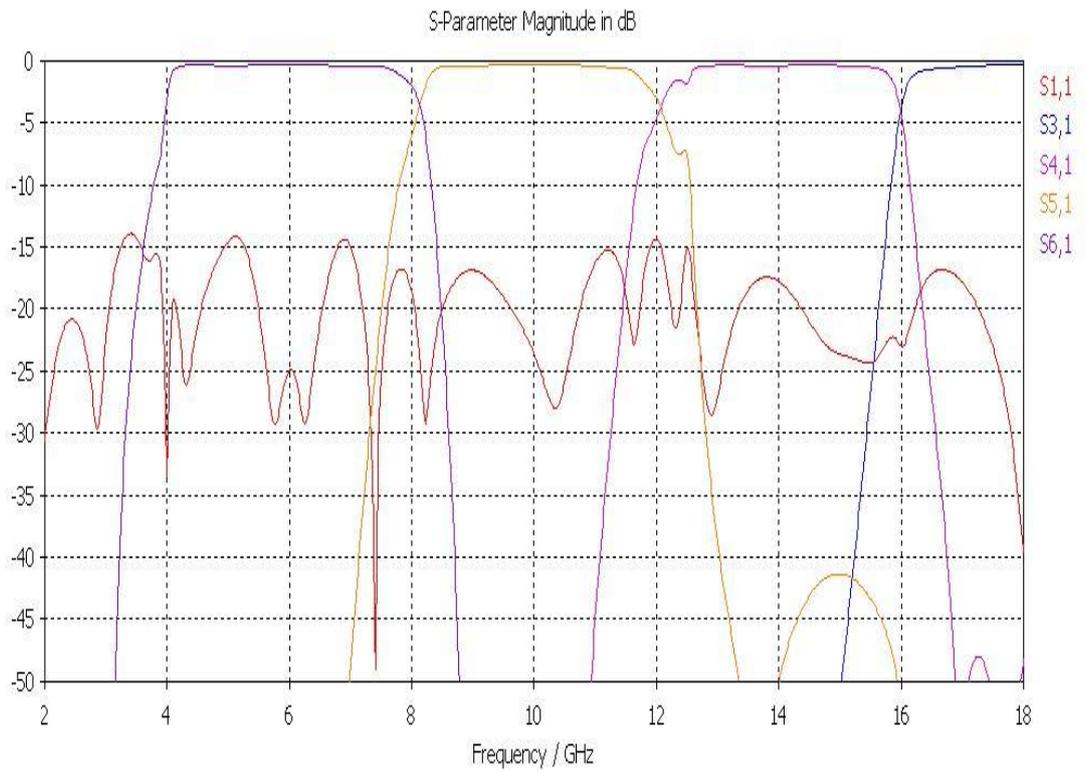
(b)

Figure 5. 19 CST layout and results for even numbered channels manifold (a) CST layout (b): CST results

m1	m2	m9	m4
freq=5.9GHz	freq=8.0GHz	freq=15.0GHz	freq=16.GHz
dB(S(6,5))=-0.7	dB(S(2,1))=-4.7	dB(S(4,1))=-45.28	dB(S(3,1))=-4.9

m6	m3		m7
freq=9.00GHz	freq=12.GHz		freq=11.GHz
dB(S(6,5))=-51.73	dB(S(2,1))=-4.1		dB(S(3,1))=-61.7

	m5		m10
	freq=7.0GHz		freq=17.GHz
	dB(S(2,1))=-53.2		dB(S(3,1))=-28.7

	m8		
	freq=13.GHz		
	dB(S(2,1))=-38.1		

(a)

(b)

Figure5.20 (a) Measurement results and Layout for manifold for even numbered channels: (a) Measurement results (b) Manifold Layout

129
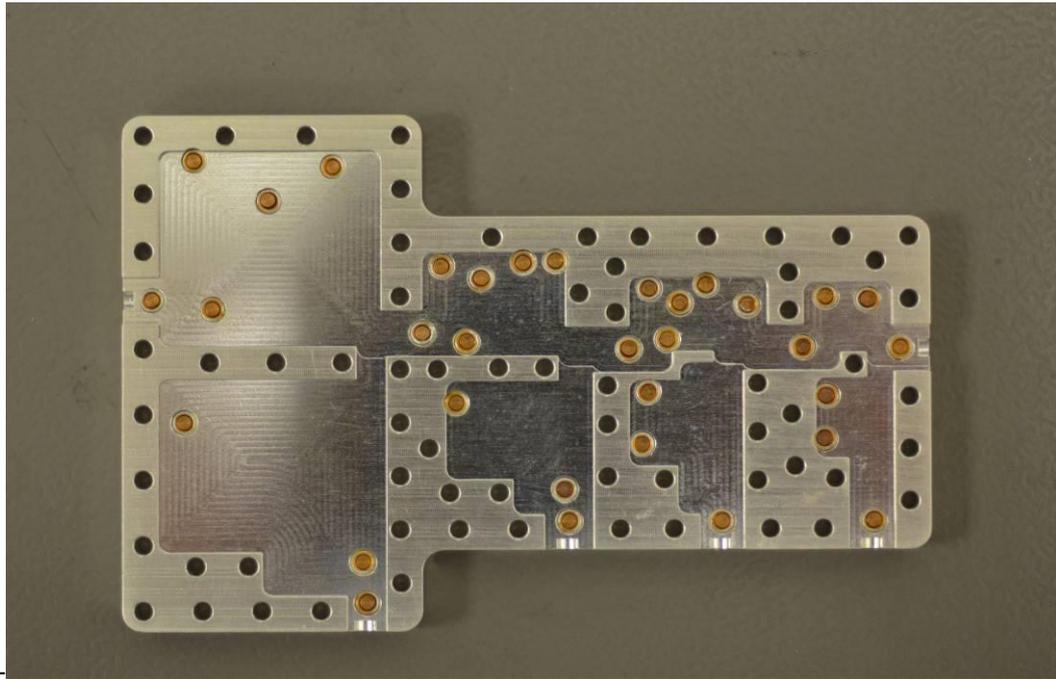
Figure 5. 20 Measurement results and mechanical layout for manifold for odd numbered channels (continued) (c) Top Cover

5.5 Design of Non-Contiguous Channel Multiplexers

The second step is to form the non-contiguous multiplexers containing even and odd numbered channels. For the multiplexer formed by odd numbered channels, 16 GHz diplexer will be appended to output of highpass channel of 14 GHz diplexer, and the output will be the LP channel of 16 GHz diplexer thus 14-16 GHz BP filter will be formed with 3 dBc crossovers at 14 GHz and 16 GHz. Similarly, 12 GHz diplexer will be appended to output of highpass channel of 10 GHz diplexer, and the output will be the LP channel of 12 GHz diplexer thus 10-12 GHz BP will be formed with 3 dBc crossovers at 10 GHz and 12 GHz. Likewise 8 GHz diplexer will be appended to highpass channel of 6 GHz diplexer, and the output will be the LP channel of 8 GHz diplexer hence 6-8 GHz BP filter will be formed with 3 dBc crossovers at 6 GHz and 8 GHz. Finally, 4 GHz diplexer will be appended to 2 GHz highpass filter at the end of the manifold, and the output will be the LP channel of 4 GHz diplexer, i.e., 2-4 GHz BP filter will be formed with 3 dBc crossovers at 2 GHz and 4 GHz. All are depicted in Figure5 .21. The ADS results are given in Figure5.22 and measurement

results, which were taken by connecting diplexers as distinct modules are given in Figure5 .23. It is observed that the input return loss degrades about to 2 dB when new diplexers are added to form the multiplexer according to ADS simulation. Measurement results show an improvement of 1 dB with the help of tuning screws. The crossover insertion losses have expected values, with worst one being 3.5 dBc with respect to the band center. Insertion loss at channel center frequencies are between 1.5 to 2 dB which is expected, as some of this loss is due to addition of losses of two diplexers one after another and degradation in return loss.

Figure 5.21 Multiplexer containing odd numbered channels

Figure 5.22 ADS results for multiplexer containing odd numbered channels

(a)

Figure 5.23 Measurement results and layout for multiplexer containing odd numbered channels (a) Measurement results

132

(b)
Figure 5.23 Measurement results and layouts for multiplexer containing odd numbered channels: (b) Module decomposition

For the multiplexer formed by even numbered channels, 18 GHz LP filter will be appended to output of highpass channel of 16 GHz diplexer, and the output will be the output of 18 GHz LP filter thus 16-18 GHz BP filter will be formed with 3 dBc crossovers at 16 GHz and 18 GHz. Similarly, 14 GHz diplexer will be appended to output of highpass channel of 12 GHz diplexer, and the output will be the LP channel of 14 GHz diplexer thus 12-14 GHz BP will be formed with 3 dBc crossovers at 10 GHz and 12 GHz. Likewise 10 GHz diplexer will be appended to output highpass channel of 8 GHz diplexer, and the output will be the LP channel of 10 GHz diplexer hence 8-10 GHz BP filter will be formed with 3 dBc crossovers at 8 GHz and 10 GHz. Finally, 6 GHz diplexer will be appended to 4 GHz diplexer at the end of the manifold, and the output will be the LP channel of 6 GHz diplexer, i.e., 4-6 GHz BP filter will be formed with 3 dBc crossovers at 4 GHz and 6 GHz. All are depicted in Figure 5.24. The ADS results are given in Figure 5.25 and measurement results and module decomposition are given in Figure 5.26. It is observed that the input return loss degrades to 10.6 dB when new diplexers are added to form the multiplexer according to ADS simulation. Measurement results show an improvement of 1.5 dB with the help of tuning screws. The crossover insertion losses have expected values, with worst one being 3.5 dBc with respect to the band center. Insertion loss at channel center frequencies are between 1.5 to 2 dB which is expected, as some of this loss is due to addition of losses of two diplexers one after another and degradation in return loss as in the previous multiplexer
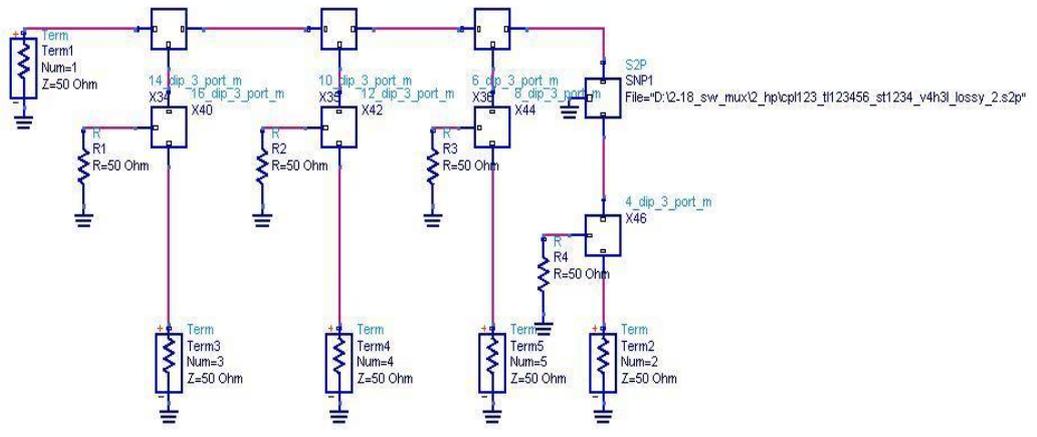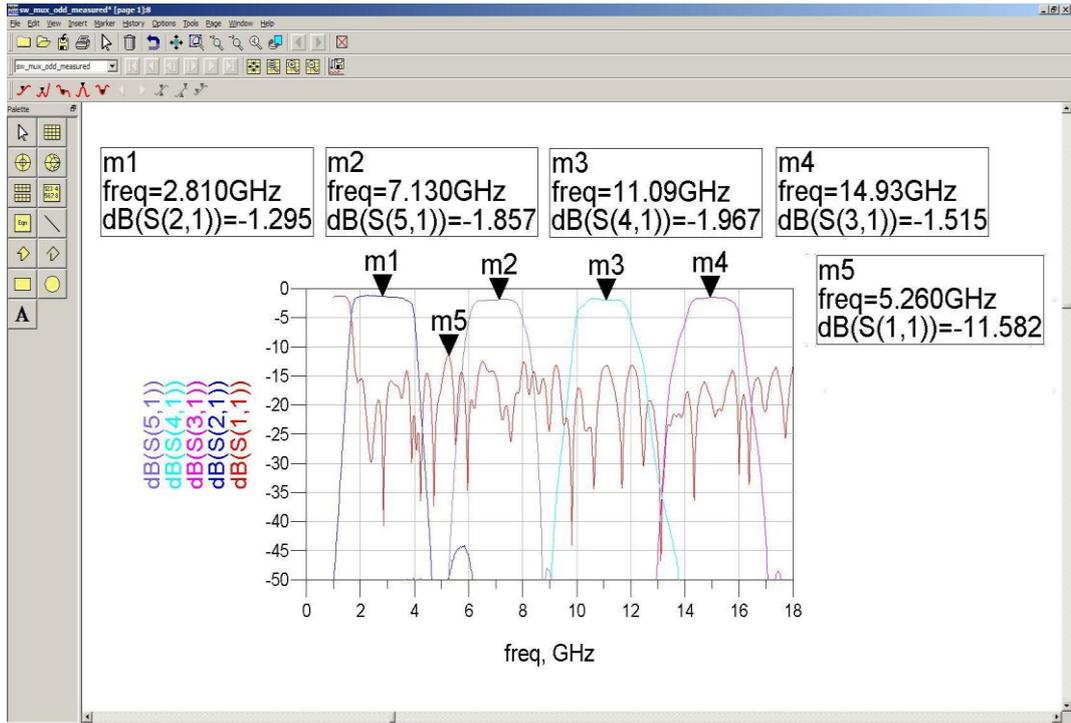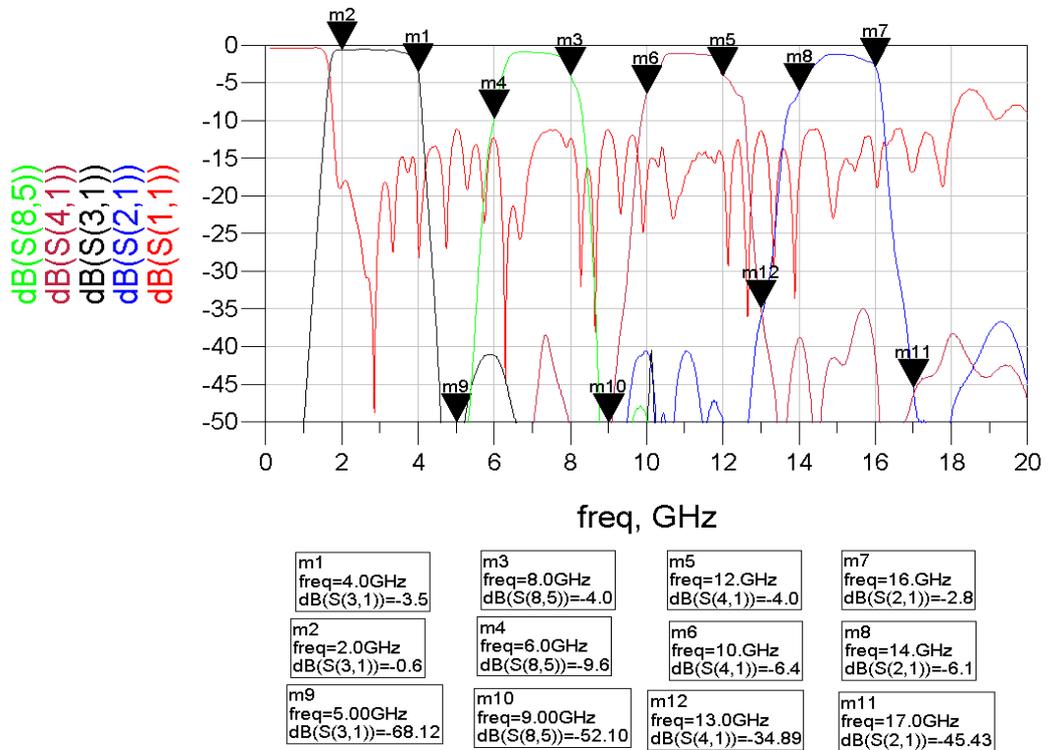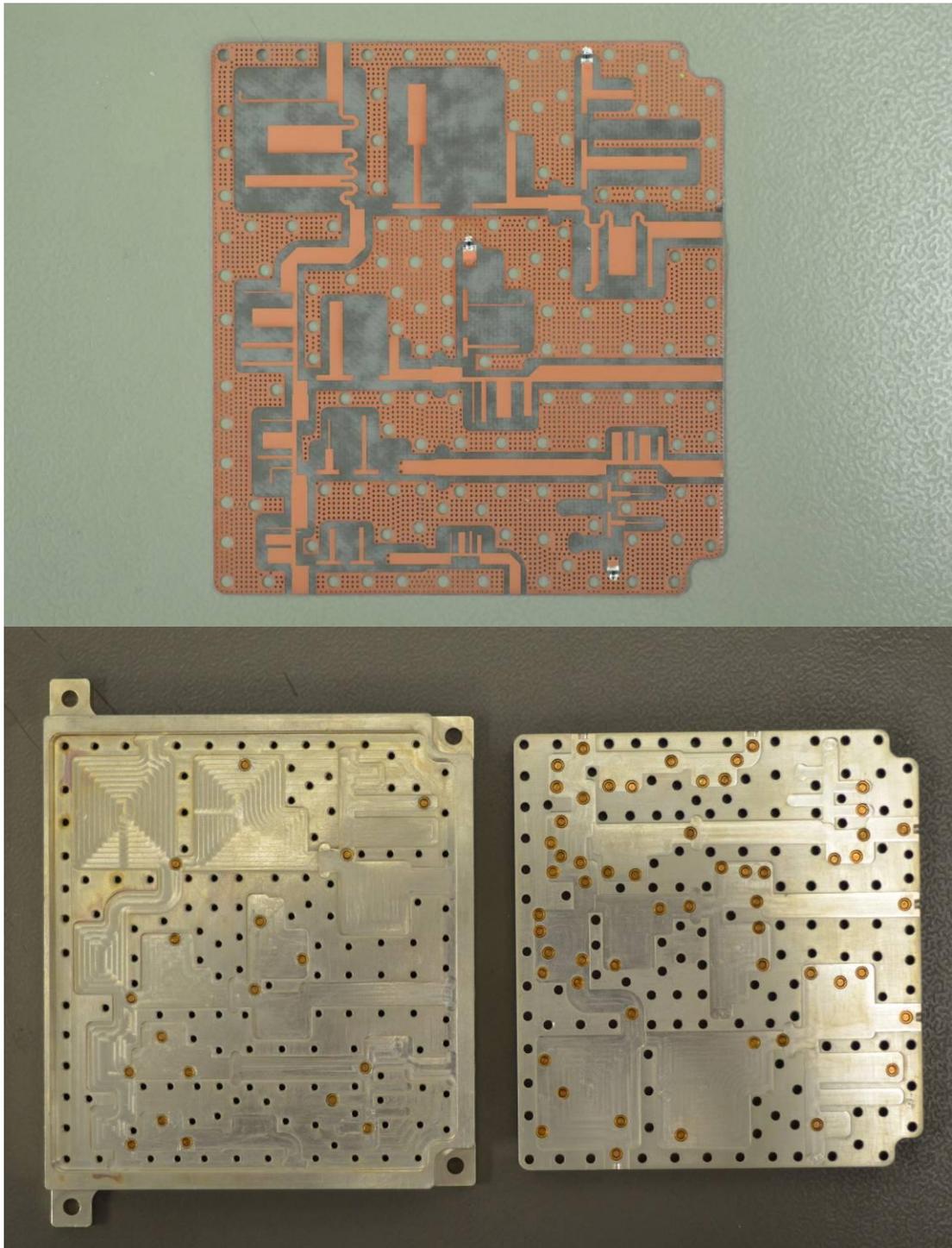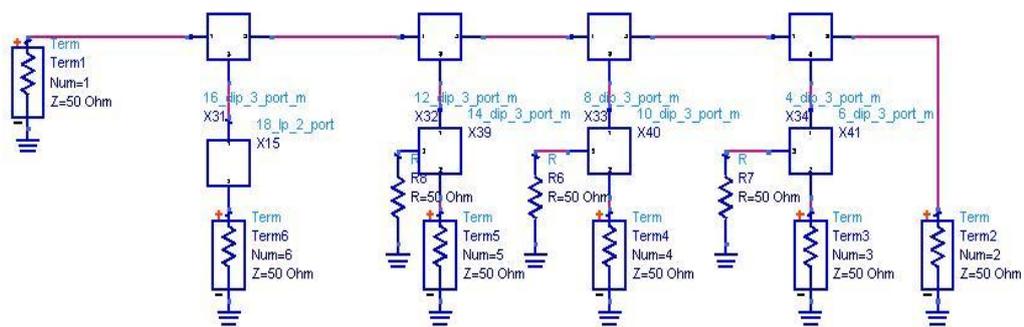

Figure 5.24 Multiplexer containing even numbered channels
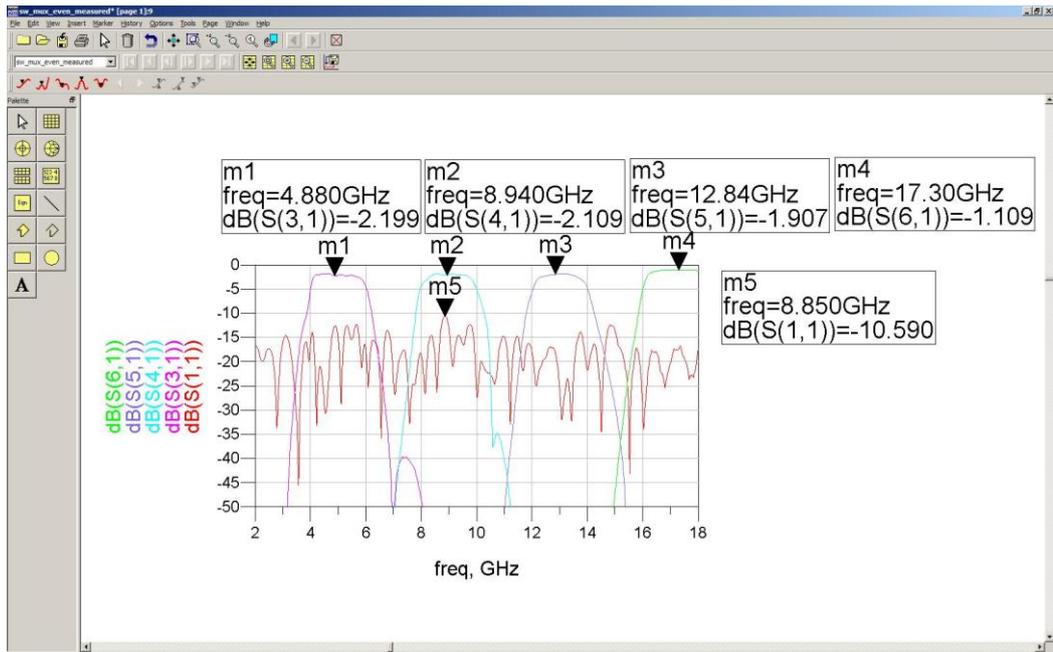
Figure 5.25 ADS results for multiplexer containing even numbered channels
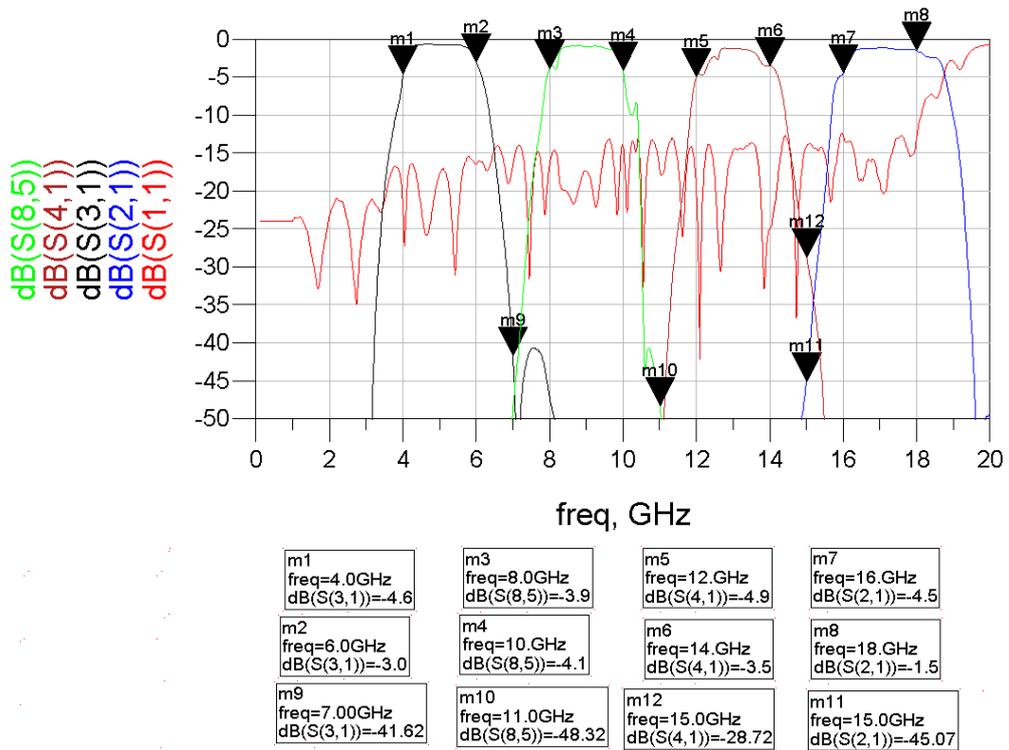
(a)

Figure 5.26 Measurement Results and layout for multiplexer for even channels (a) Measurement results
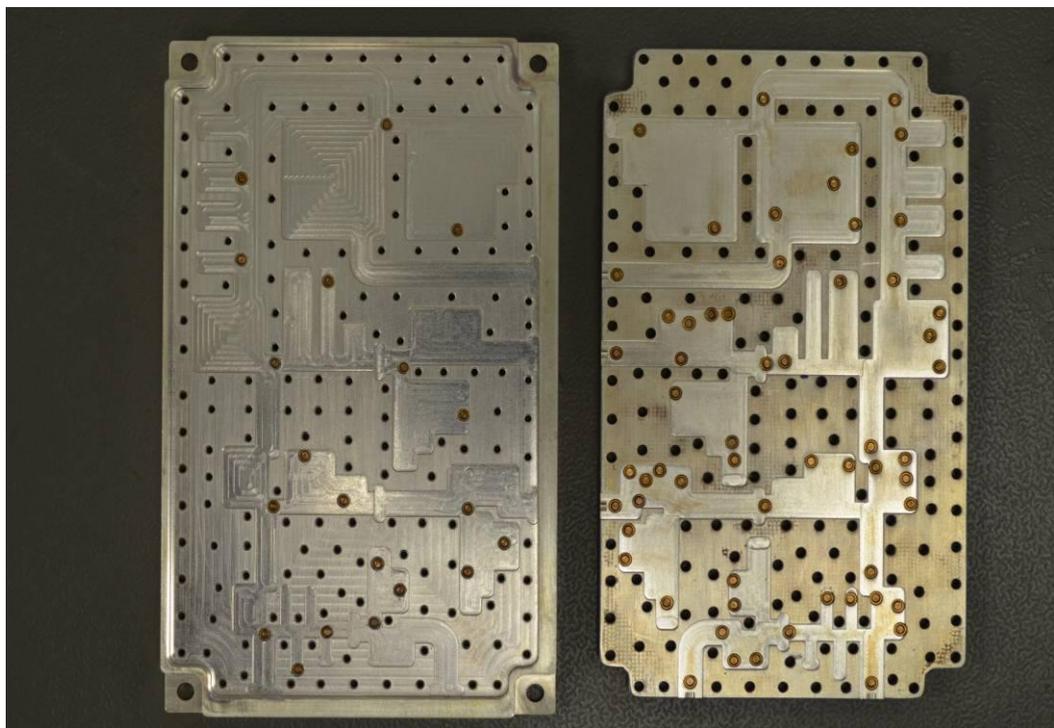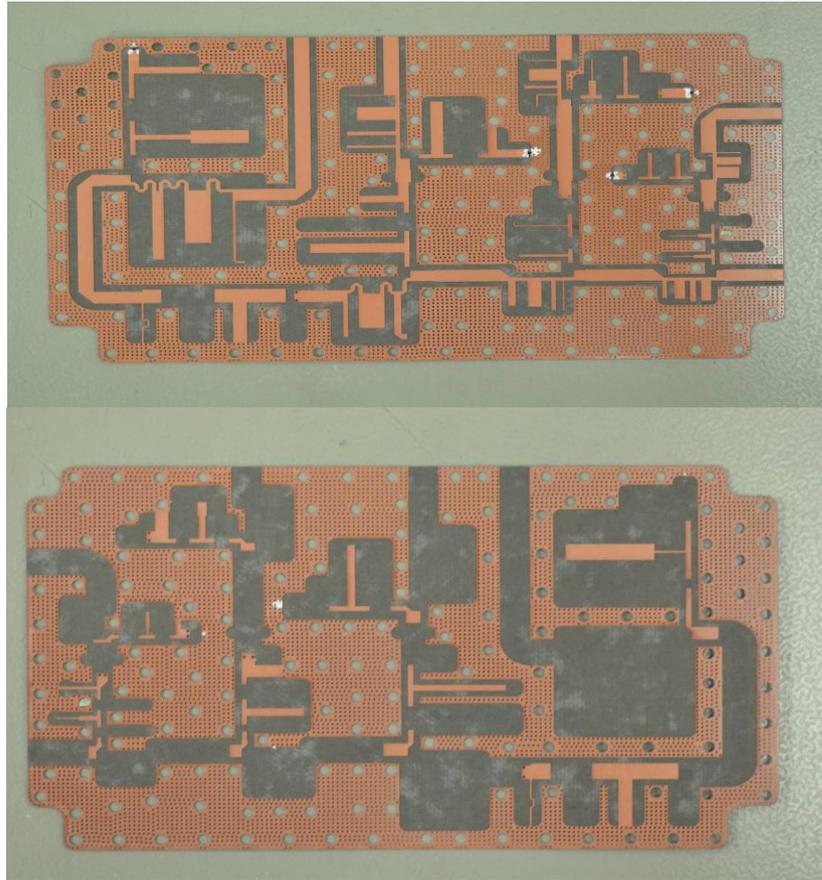
(b)
**Figure 5. 26 Measurement results and layout for multiplexer containing even numbered
channels: (b) module decomposed**

5.6 Design of Non-Contiguous Channel Switched Multiplexers

The formation for even and odd channel SW_MUX's are straightforward. The multiplexers for odd numbered channels and even numbered channels will be connected back-to-back style with a switch between each channel. The formation of odd channel SW_MUX is shown in Figure 5.30 and its response is given in Figure 5.28, and odd channel SW_MUX is shown in Figure 5.30 and its response is given in Figure5.29. Looking at the Figures 5 .28 and 5.29, it is seen that the back to back connection has degraded both the return loss and insertion loss of the channels. The return loss moved up to 9 dB. From insertion loss point of view, in the passband extra ripple occurred and in the stopband the rejection does no longer change monotonically. A solution to the abovementioned problems can be inserting attenuators before and after the switches as seen in Figures 5 .31 to 5.34.
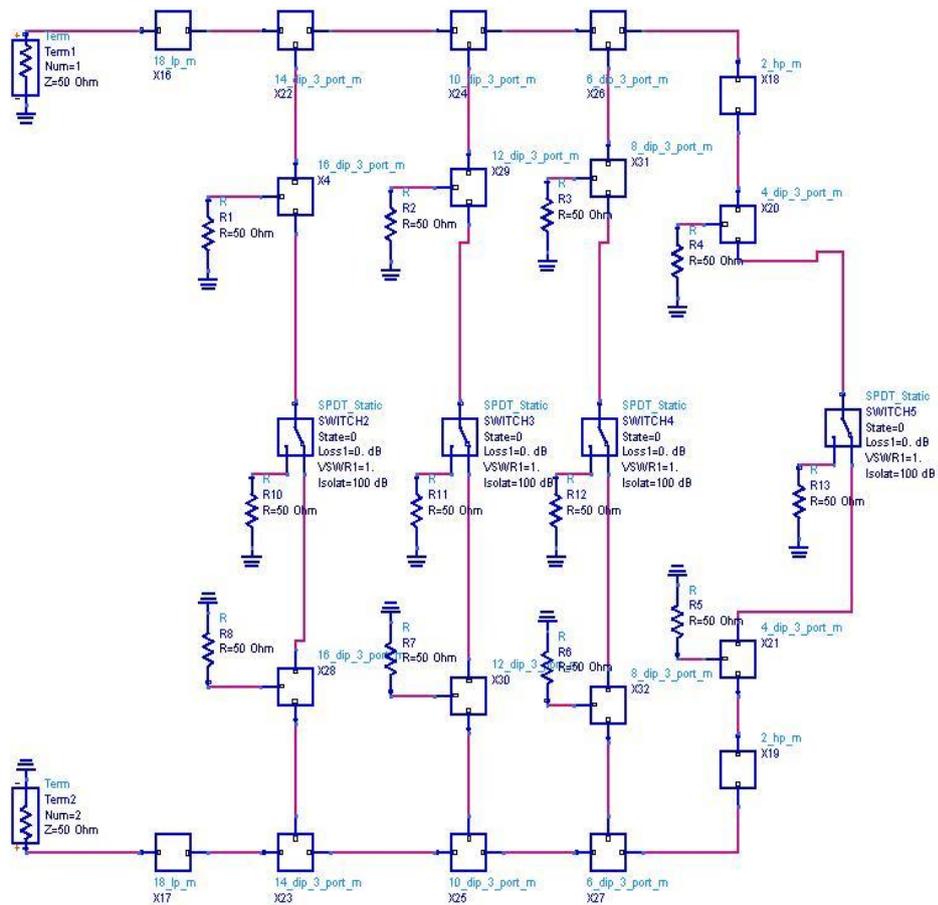
Figure 5. 27 Odd channel SW_MUX
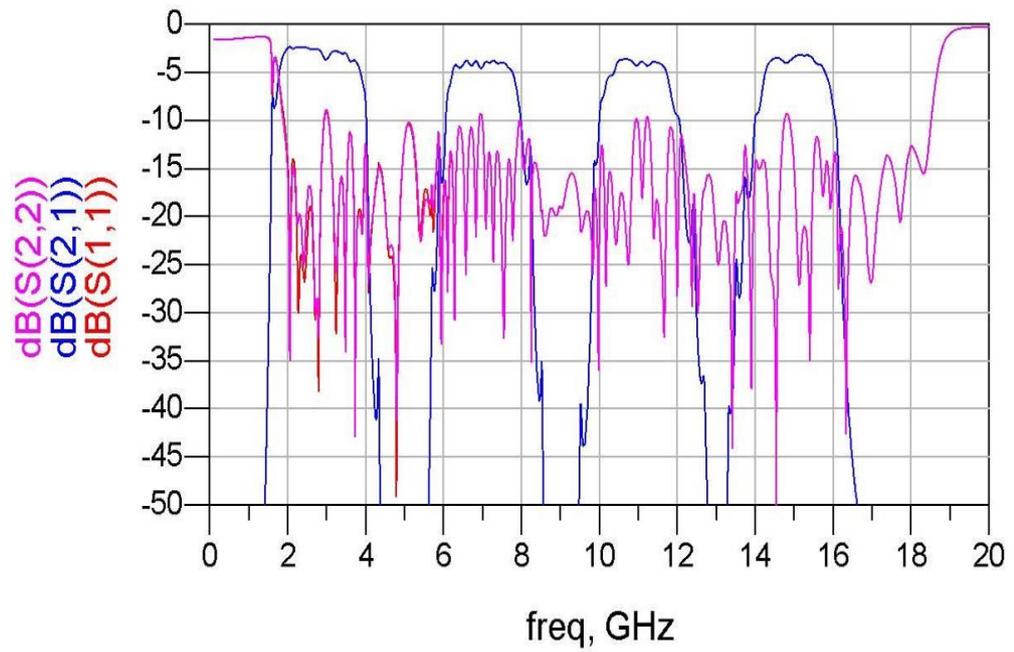
Figure 5. 28 Odd channel SW_MUX results
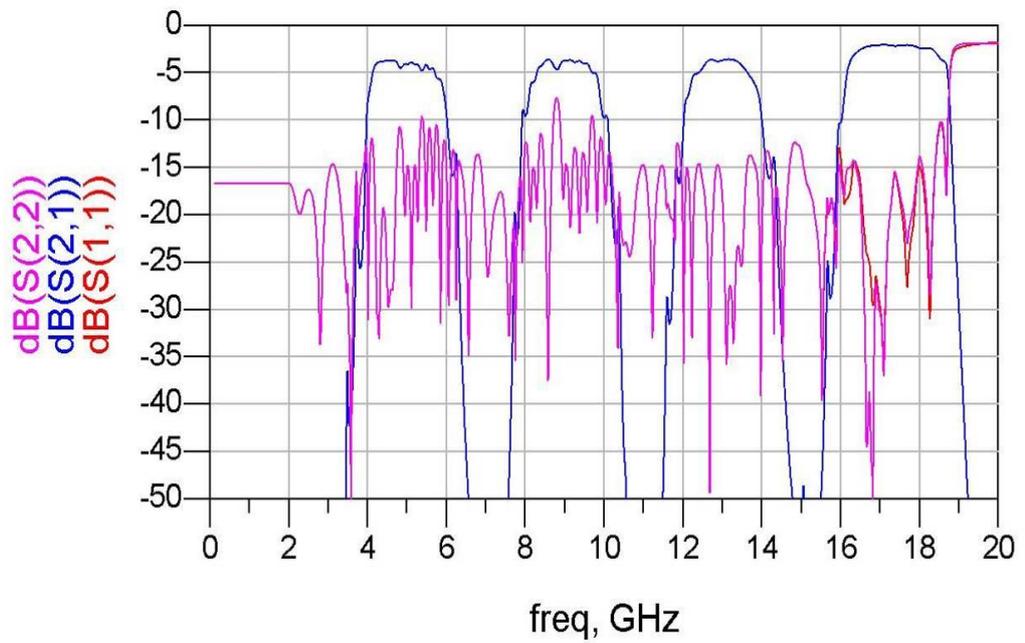
Figure 5. 29 Even channel SW_MUX results

138
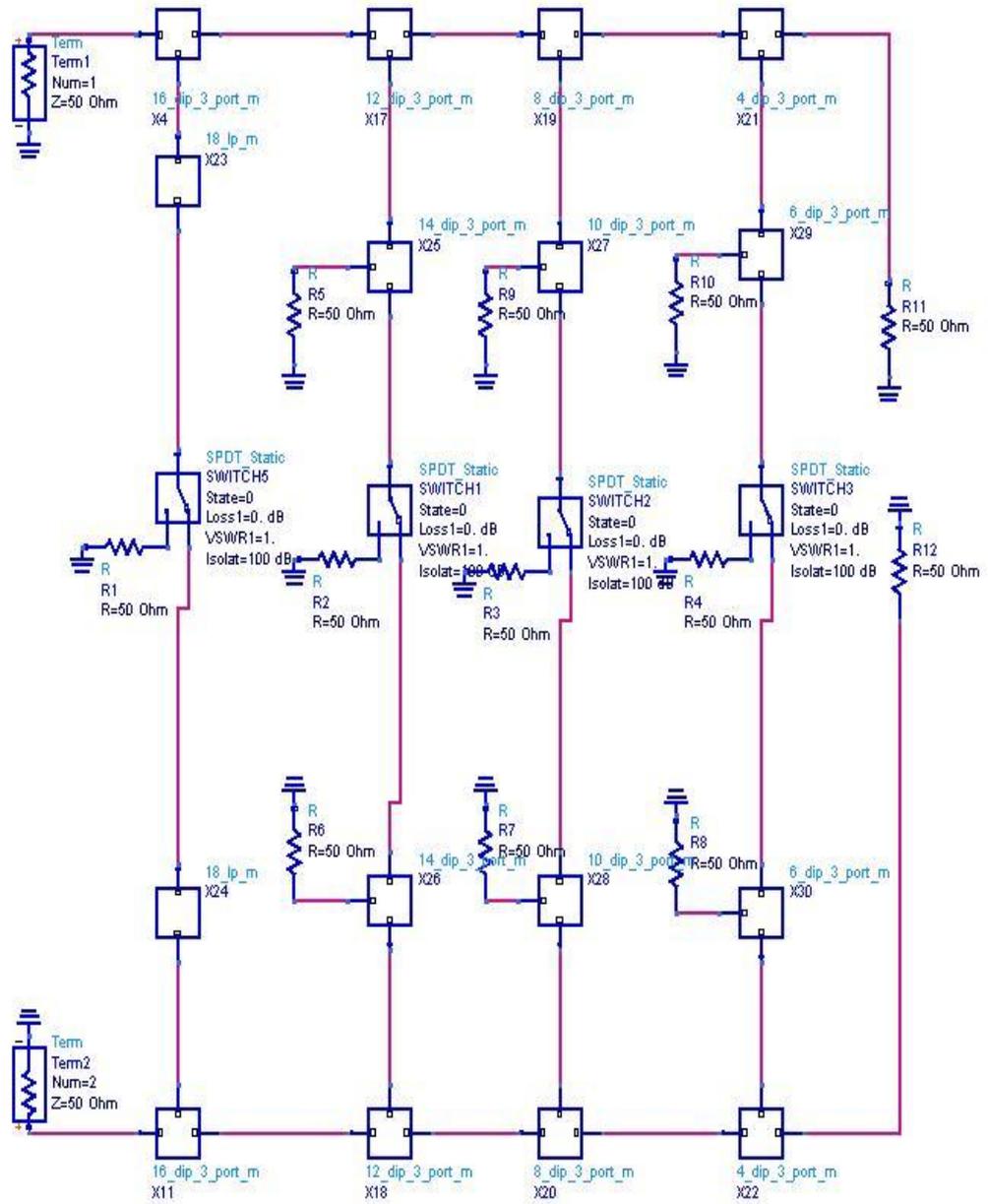
Figure 5. 30. Even channel SW_MUX

139
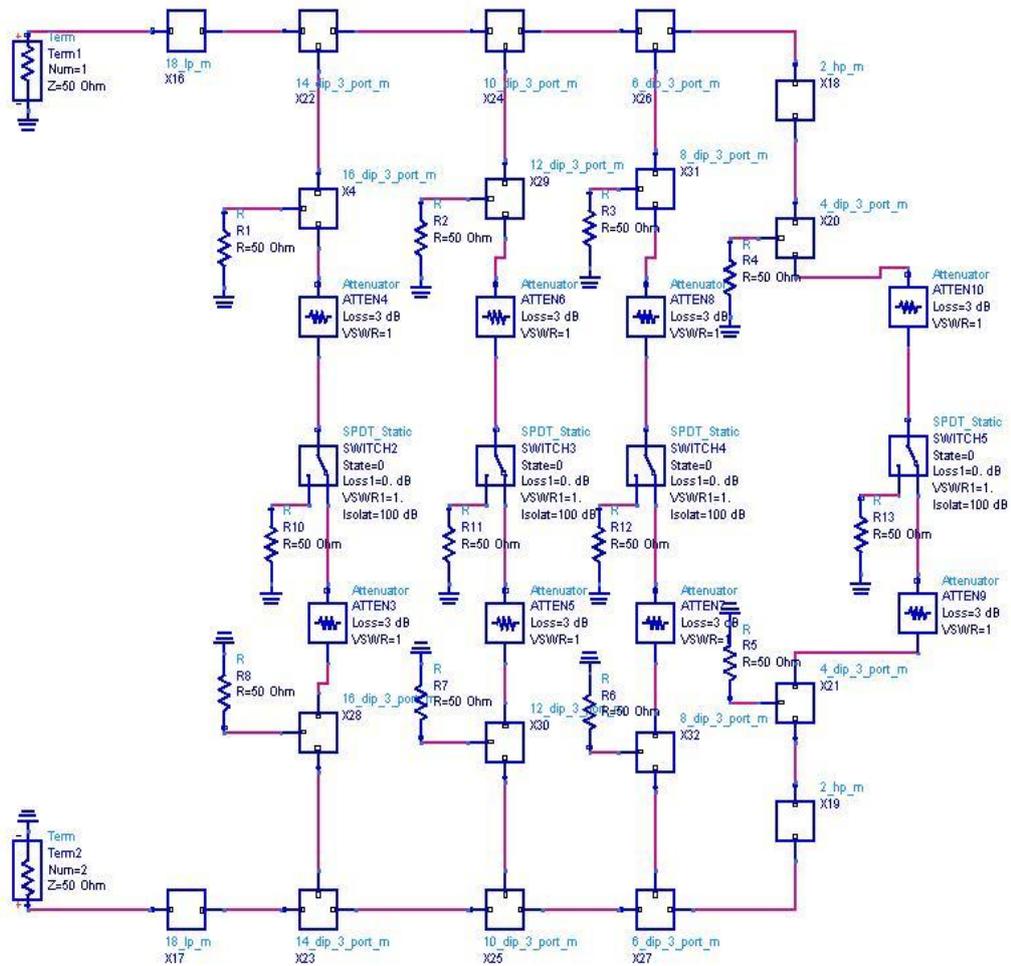
Figure 5. 31 Odd channel SW_MUX with attenuators

As seen from Figures 5 .35 and 4.36 that the degradation in the return loss was decreased and the monotonic increase in the rejection as well as the flatness in the passband has been restored, but this time we have an excess loss of 6 dB emerging from the attenuators placed. As a way to get rid of the excess loss, LNA'a can be used together with the attenuators, which will be placed near input just in front of the switches as shown in Figures 5 .38 to 5.41.
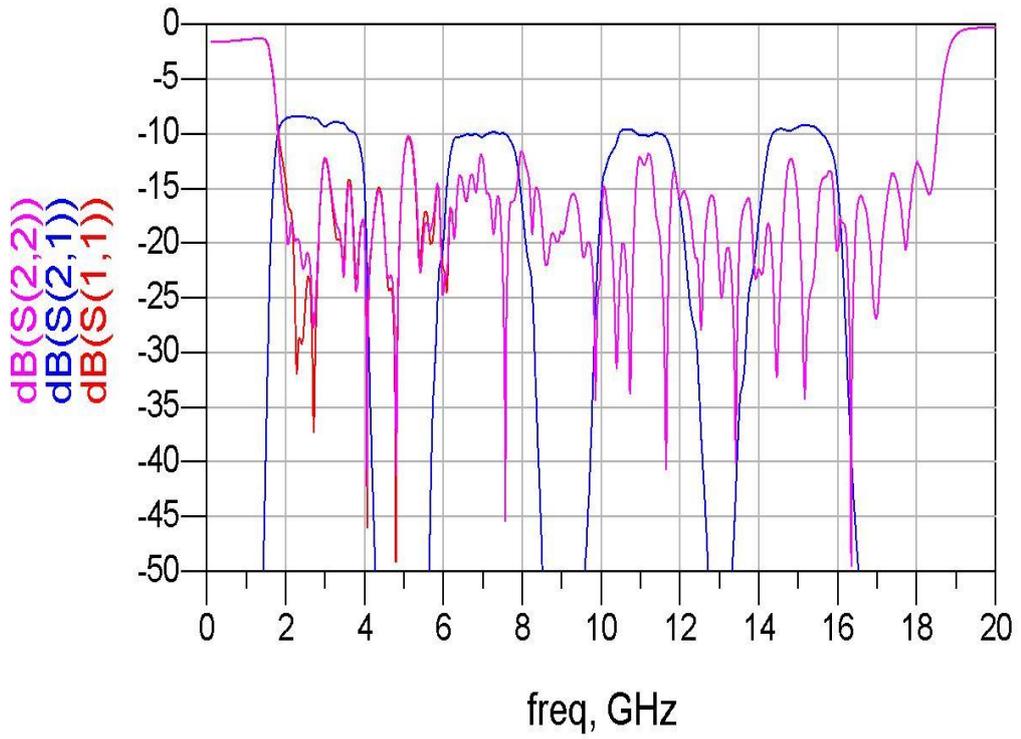
Figure 5. 32 Odd channel SW_MUX with attenuators: results
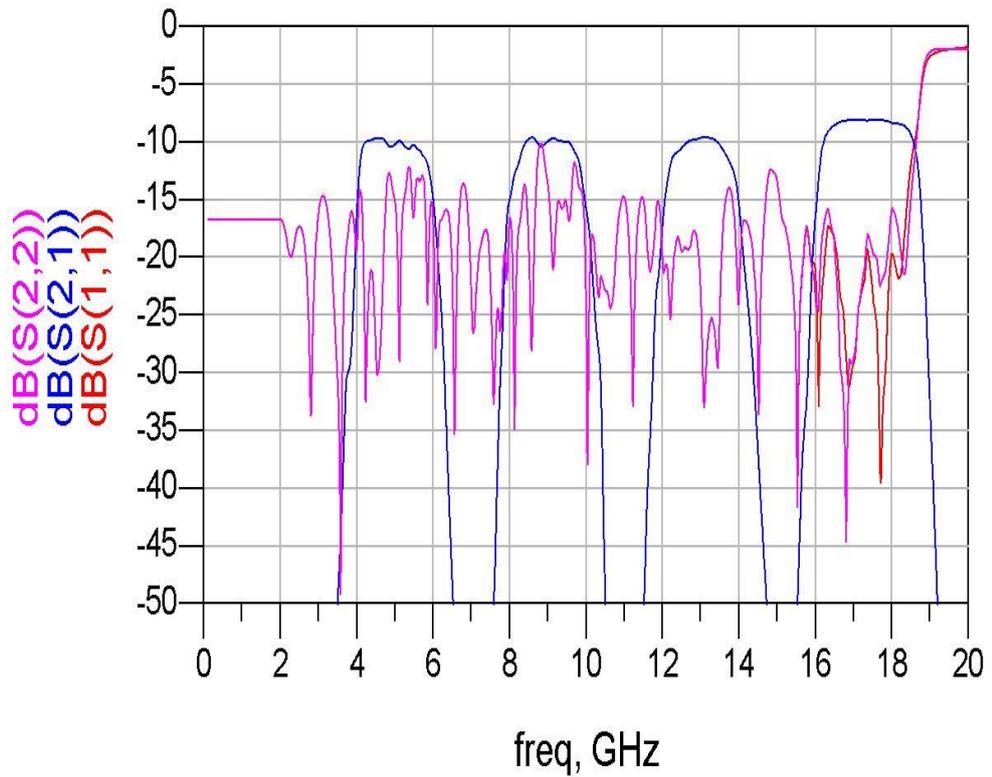
Figure 5. 33 Even channel SW_MUX with attenuators: results

141
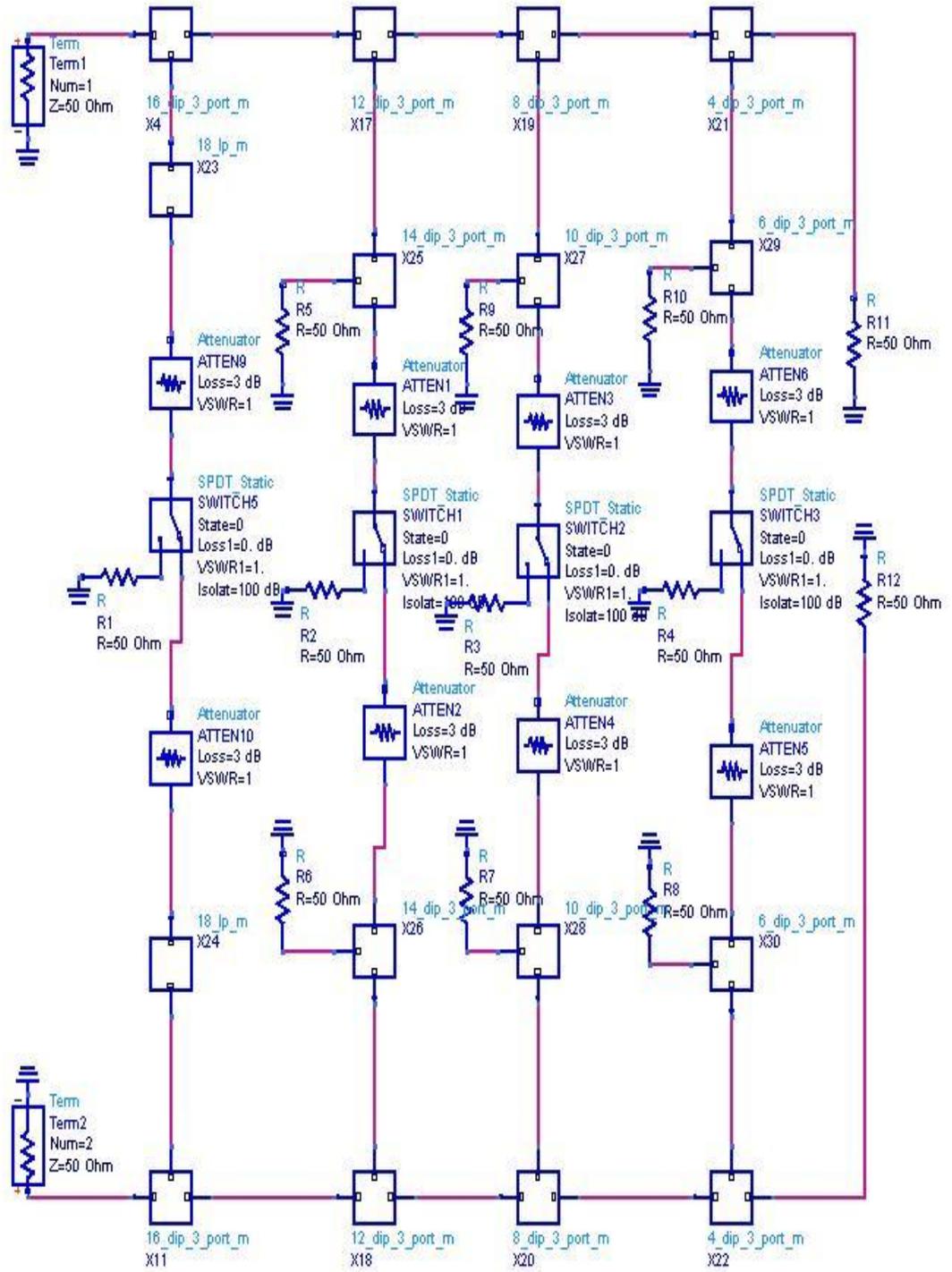
Figure 5. 34 Even channel SW_MUX with attenuators

142
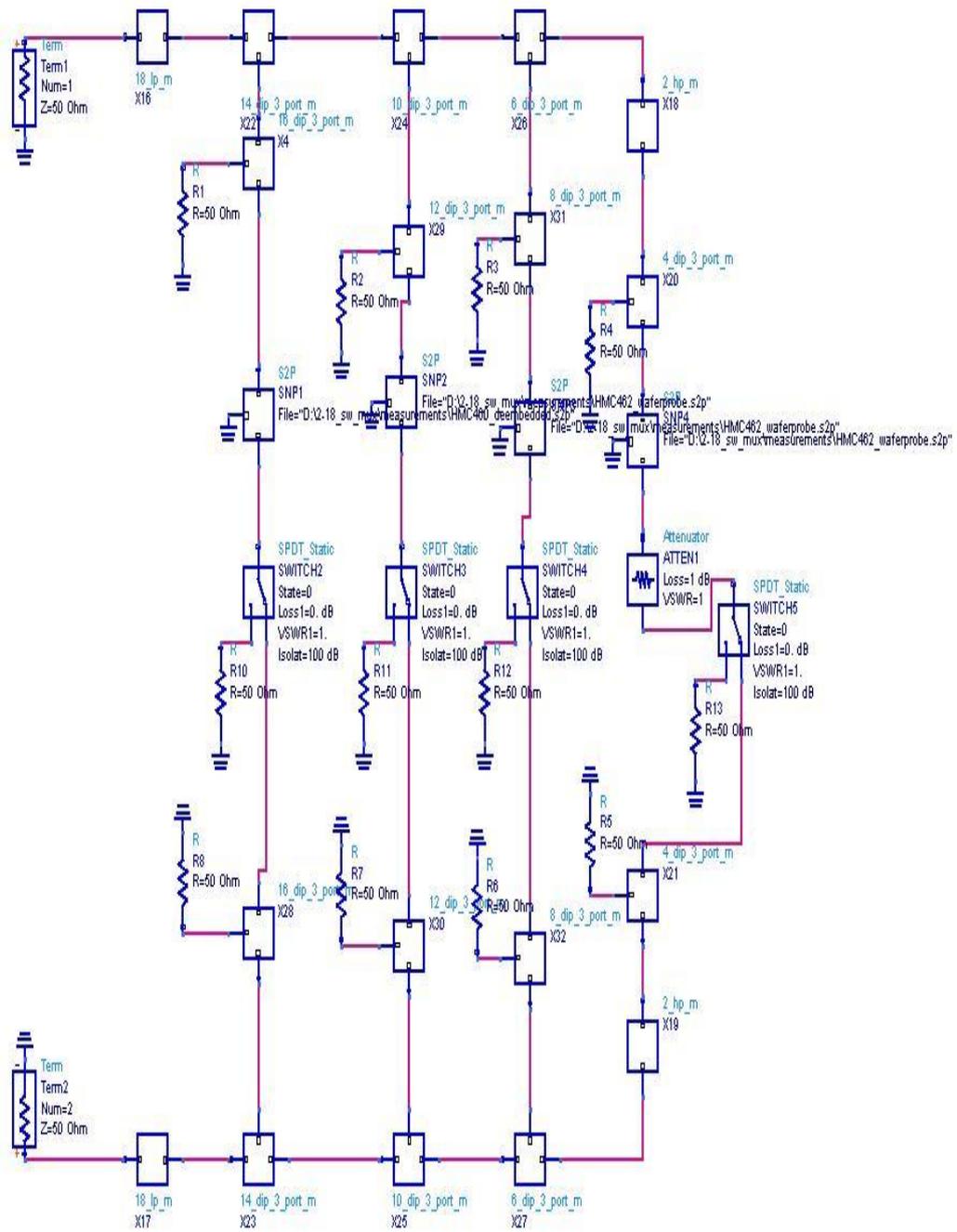
Figure 5. 35 Odd channel SW_MUX with amplifiers
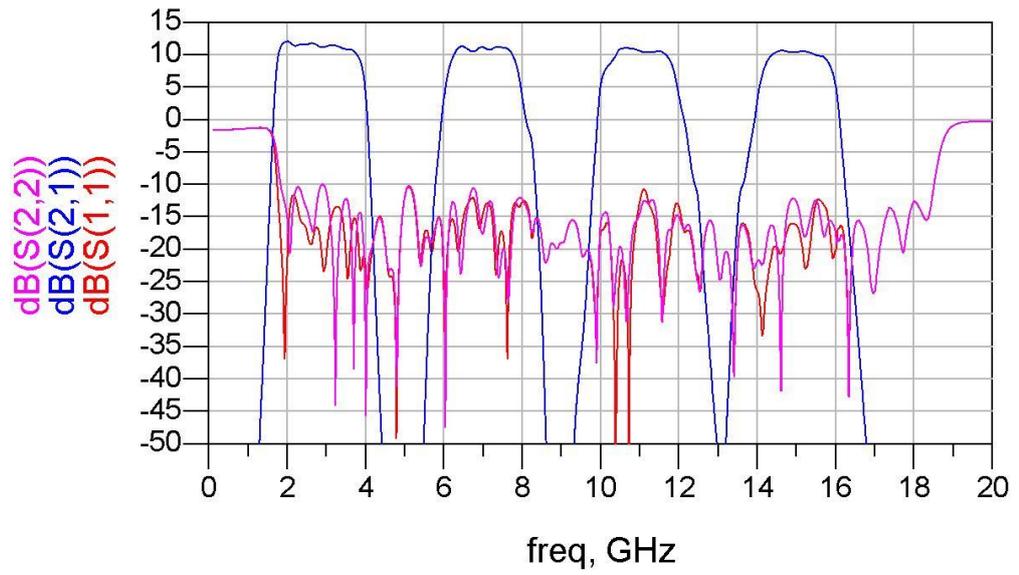
Figure 5. 36 Odd channel SW_MUX with amplifiers: results
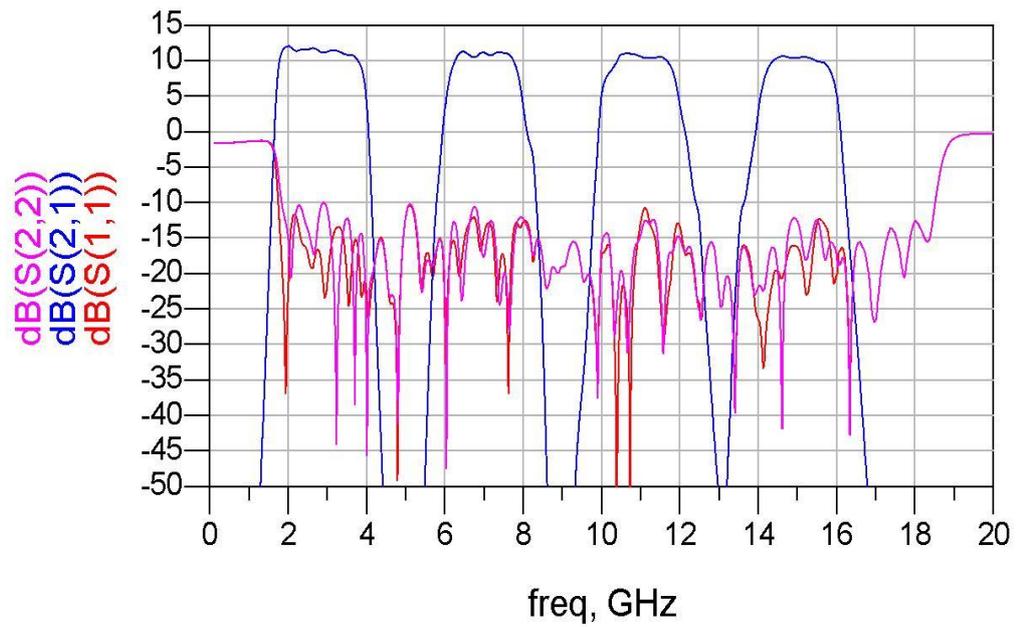
Figure 5. 37 Even channel SW_MUX with amplifiers: results

144
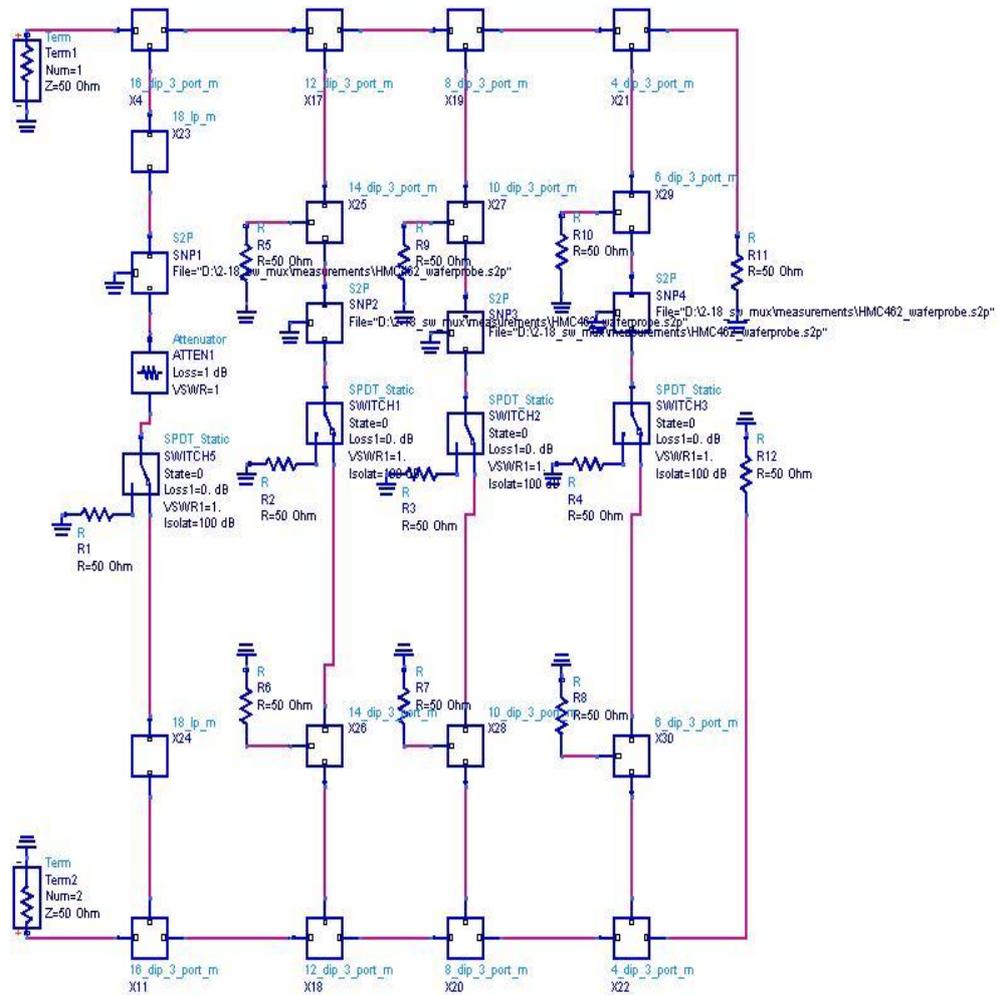
Figure 5. 38 Even channel SW_MUX with amplifiers

As the Figures 5.35 to 5.38 are inspected, it can be seen that the reverse isolation of the amplifier helps the SW_MUX to maintain the return loss at an acceptable level and forward gain of the amplifier prevent extra insertion loss from attenuators, Hence the utilization of LNAs with attenuators seems to be the best option for achieving the desired performance.

There are a wide range of candidates for the selection of proper LNAs. The criteria for selecting the LNA can be stated as follows. The selected LNA should have a forward gain between 14 dB and 19 dB, because it must not limit the dynamic range of the receiver or system it is going to be used neither from up or down. The input and output return losses should be better than 10 dB over the entire 2-18 GHz band

because as the diplexers and filters have very good input and output return loss performance, the switch and LNA will define the return loss, hence flatness of the insertion loss response. Attenuators can be used for matching purposes at the input of the LNAs but this will increase the noise Figure, hence reduce the sensitivity of the ESM system or receiver. It is almost compulsory that the reverse isolation of LNA should be as high as enough to prevent reflections form the back to back connection. Lastly as a practical issue the LNA should be in die form and preferred to be using single supply (hopefully not hungry for current) to eliminate extra effort to carry other supply voltages inside the RF circuitry. Considering all these facts TGA2513 of Triquint™ will be used.

Another critical issue is the selection of switch. For this selection we have similar criteria. Firstly the loss should not be greater than 2 dB over the entire 2-18 GHz band and the return loss should be better than at least 10 dB. It is preferred to be an absorptive switch in order not cause extra ripple in the passband when it is in OFF state. Again it should be in die form and single supply controlled for the reasons same as the ones stated or the LNA. Considering a SPDT is chosen it has to be a high isolation switch which will not allow any degradation in the suppression of the channel when it is unselected. Therefore HMC347 of Hittite™ will be used. there is one problem with the switches: the isolation between ports is merely 50 dBc, which is actually just as much as desired, so any variation will detoriate the suppression performance. There are possible solutions to overcome this. One is to use two switches in series to increase isolation. The second one is to use a pin diode switch and bear with the extra loss and complexity which will be caused by additional circuitry to bias the switch. The last one is to put a pin diode in parallel with the 50 ohm termination shown in any SW_MUX Figure above. That would give an isolation of minimum 60 dBc which can be further tweaked to 70 dBc. Nevertheless, the scope of this thesis is not primarily to design high isolation switches, so an ideal switch block mimicking the actual switch in return loss, insertion loss and isolation will be used as given in the subsequent figures.

5.7 2-18 GHz 8-Channel Switched Multiplexer

The proposed final SW_MUX structure is given in Figure5 .42. As seen 2-18 GHz power divider is represented by a three port at the input and output , whereas the odd and even SW_MUXs are connected to the output ports of 2-18 GHz power divider at the input and their outputs are connected to input ports of 2-18 GHz power divider, which acts as a combiner at this time at the output.Figure5 .43 shows the odd channel SW_MUX and Figure5 .44 shows even channel SW_MUX. Note that in all Figures from 4.42 to 4.44 ribbon wires are used to connect the MMIC and thin film components (such as power divider) to the structure since they should be accounted for the phase at the cross-over frequencies to ensure a good recombination.
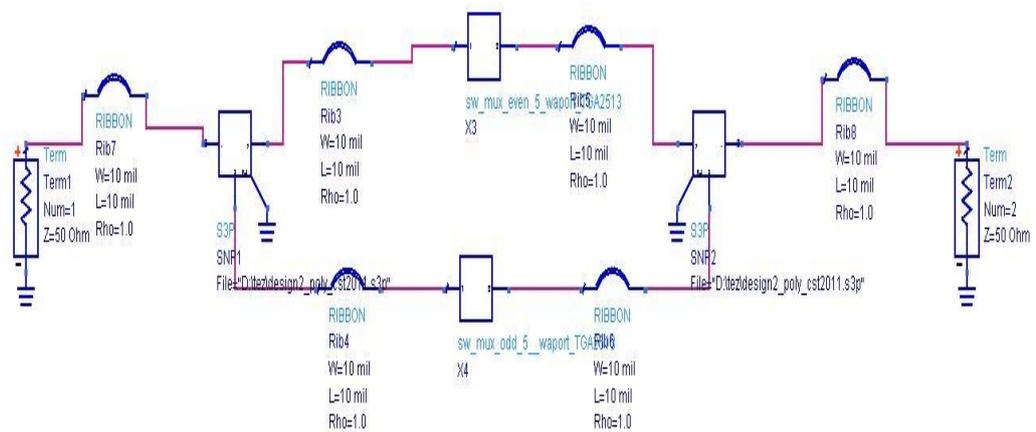
Figure 5.39 Final SW_MUX structure
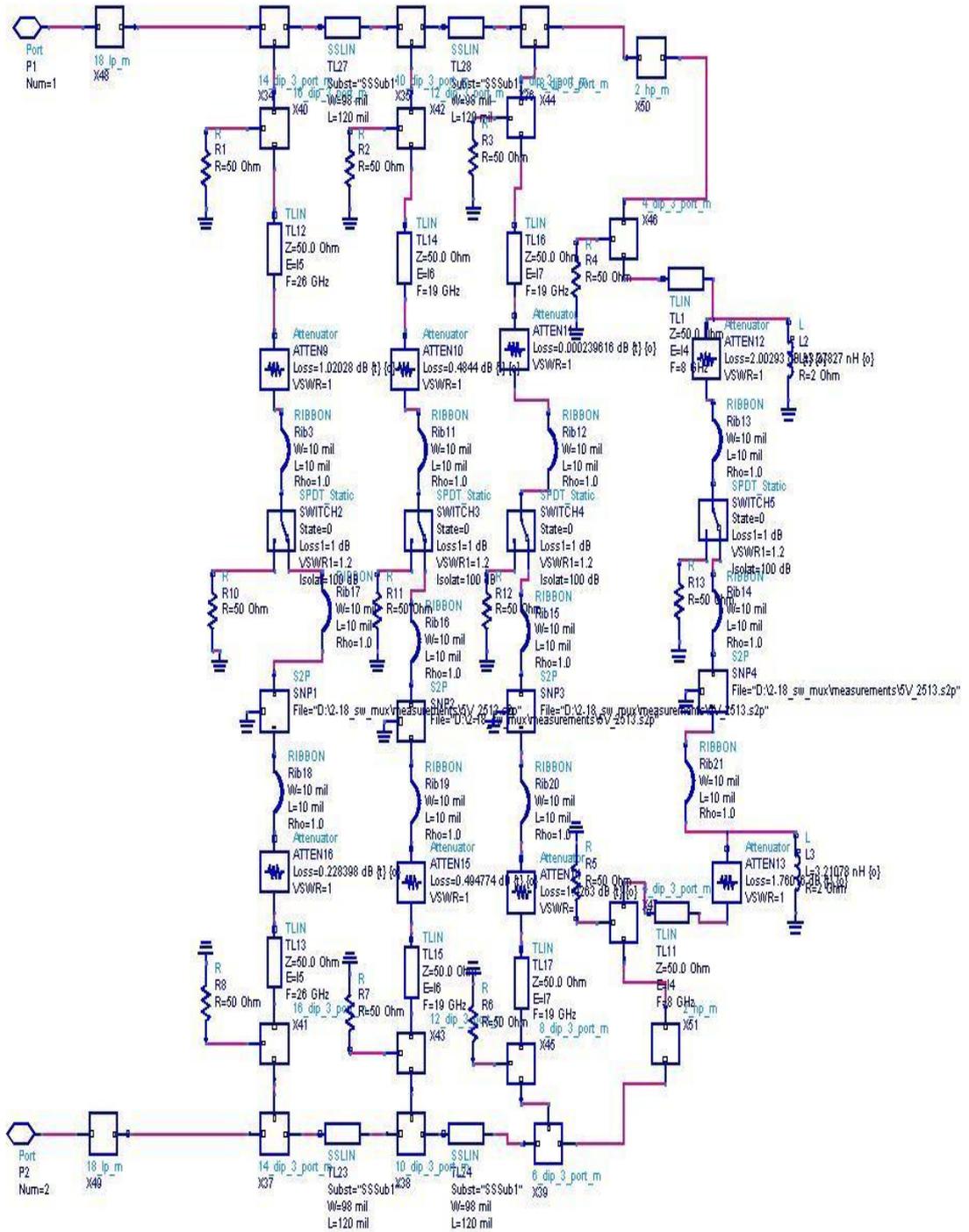
Figure 5. 40 Final SW_MUX structure: odd half
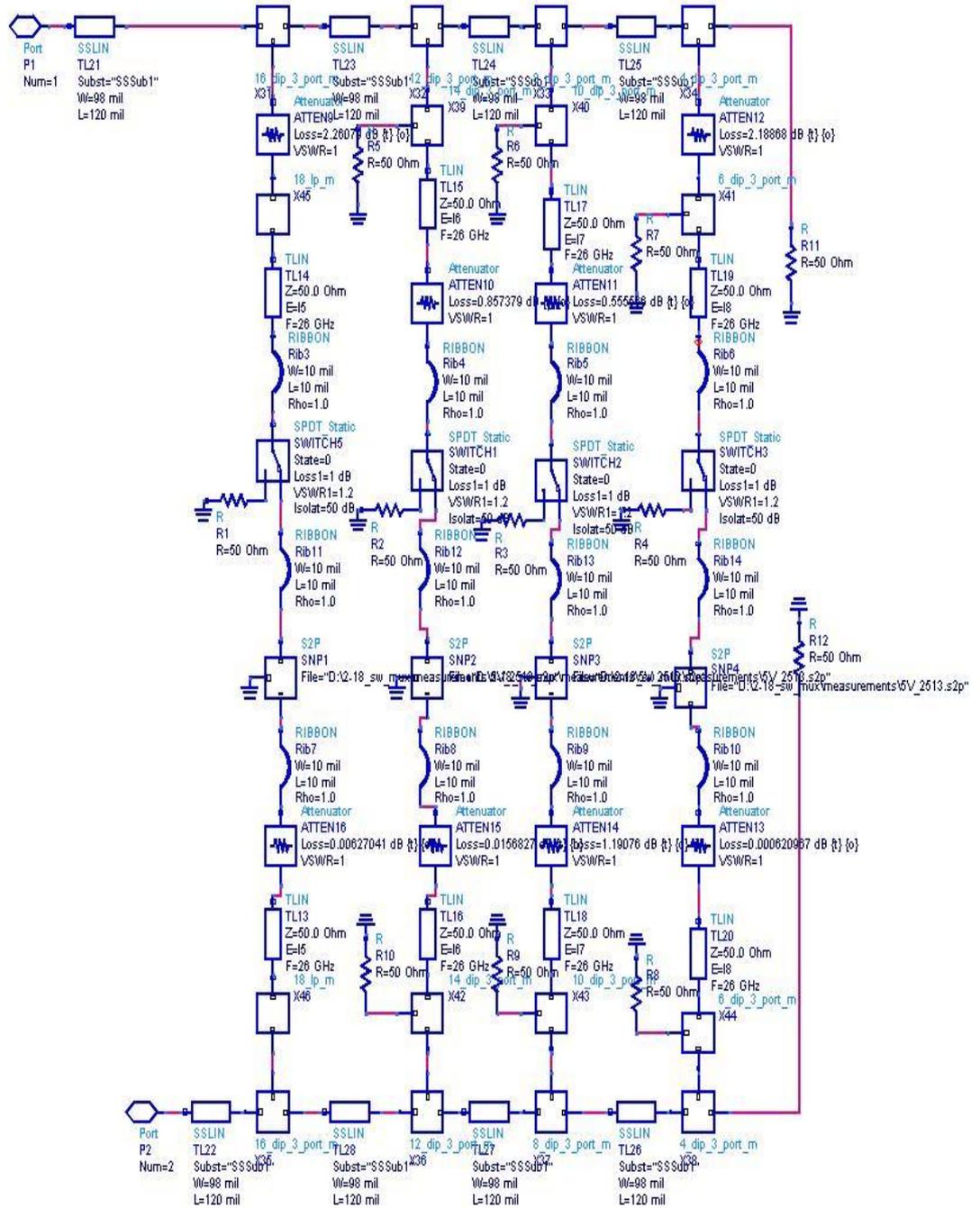
Figure 5. 41 Final SW_MUX structure: even half

149

Note the use of inductor parallel with the attenuator in 2-4 GHz channel, that is due to the fact that the LNA used (see appendix 1) has a negative gain slope from 2-4 GHz about 3 dB that would make the channel having the same slope and disables the recombination with 4-6 GHz channel. Therefore a small equalization operation was carried out there. The transmission lines at the input and output of each switch-LNA block accounts for the phase match at the cross-overs. The attenuators have two purposes, one for improving return loss performance, other to balance the amplitude differences between channels. Eliminating the possible problems, behaviour of the SW_MUX structure can now be investigated. Figure5 .45 shows the odd channels when even channels have shut. Figure 5 46 show the response when odd channels are OFF and even channels are ON. In Figure 5.47 all channels are ON. In Figure 5.48 all channels are OFF.
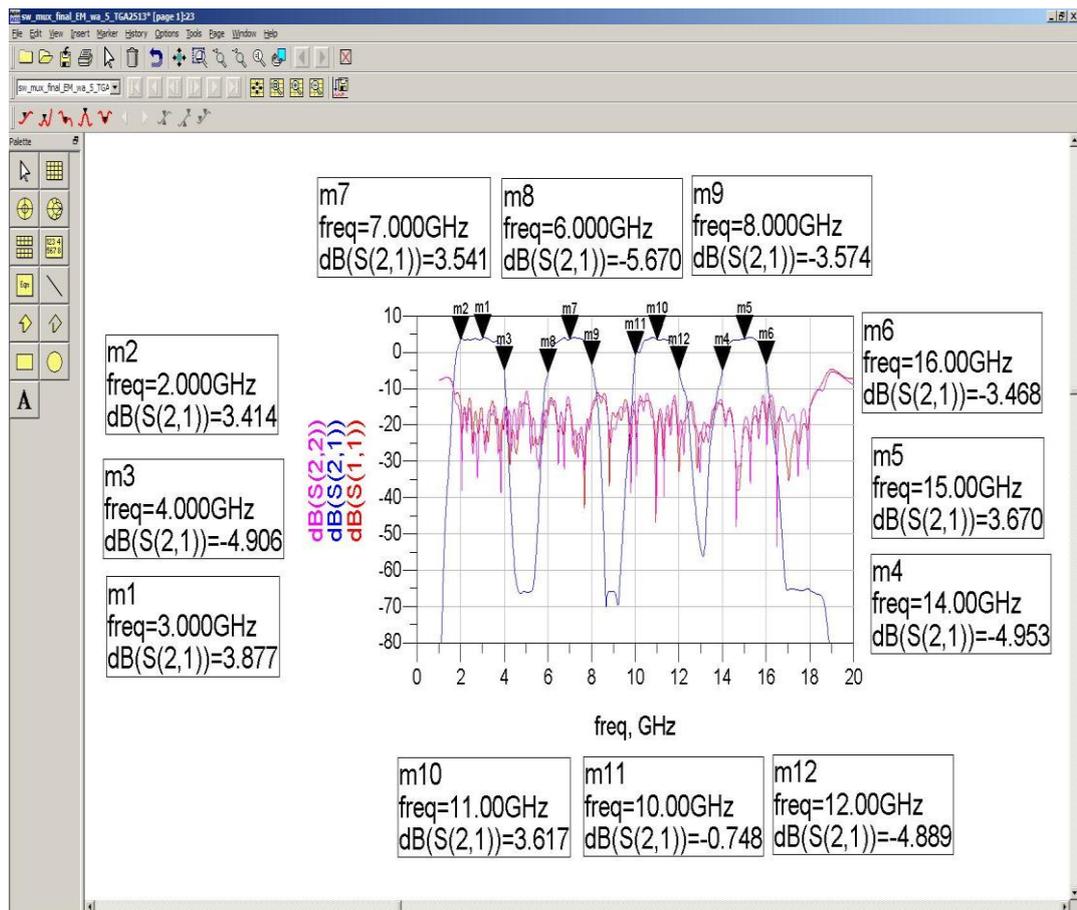
Figure 5. 42 Response when odd channels are ON, even channels are OFF
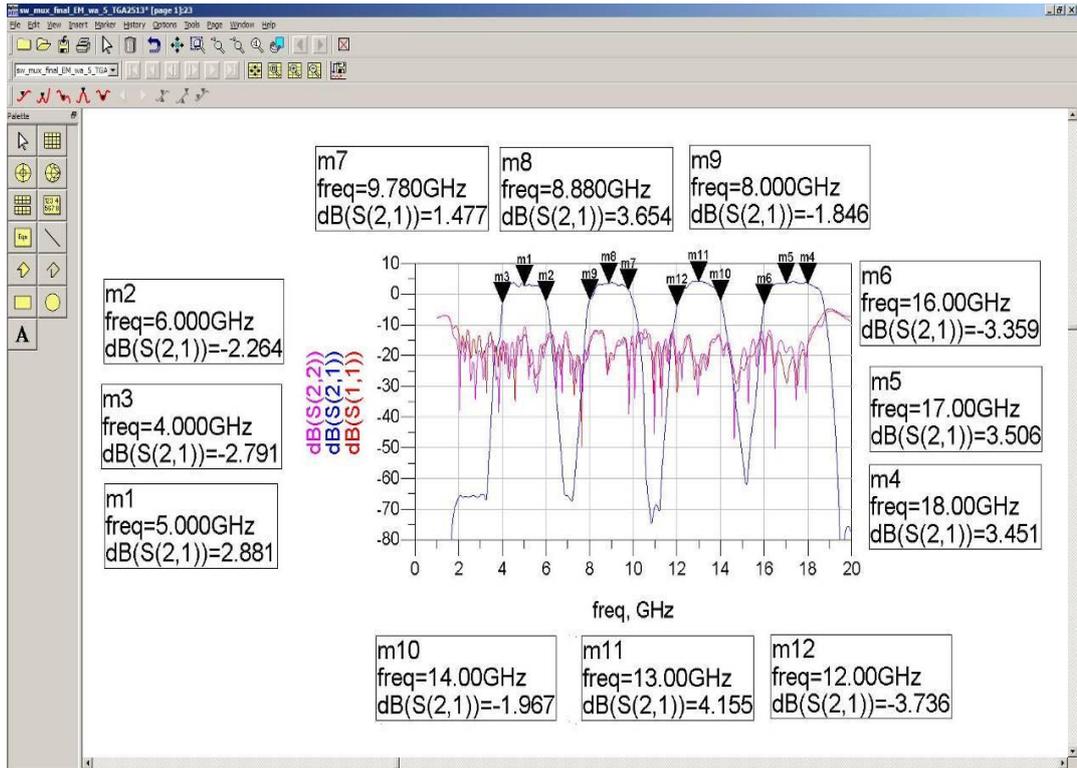
Figure 5.43 Response when odd channels are OFF, even channels are ON
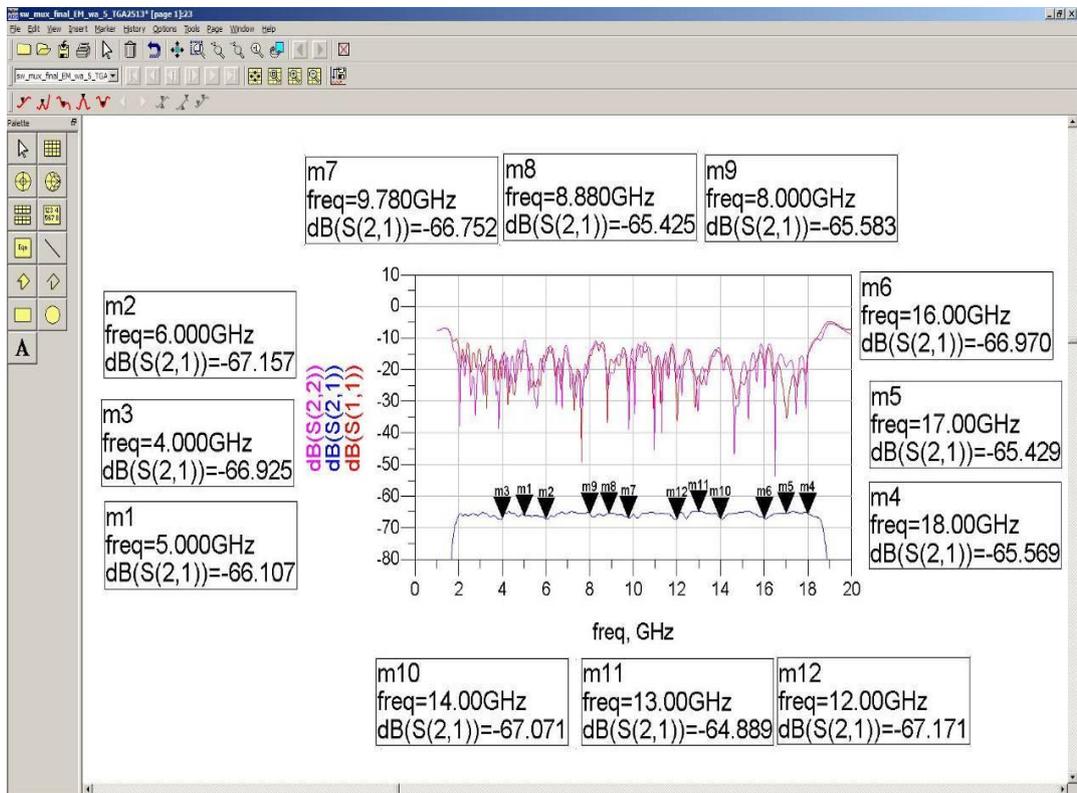
Figure 5.44 Response when all channels are OFF

151
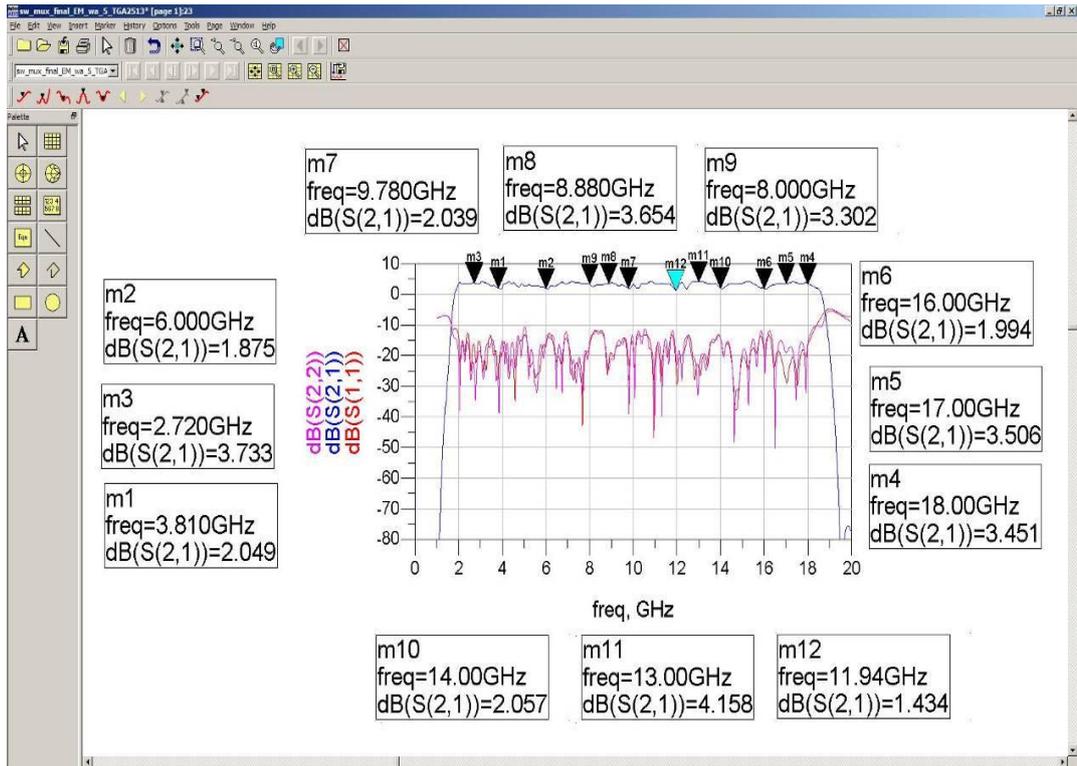
Figure 5.45 Response when all channels are ON
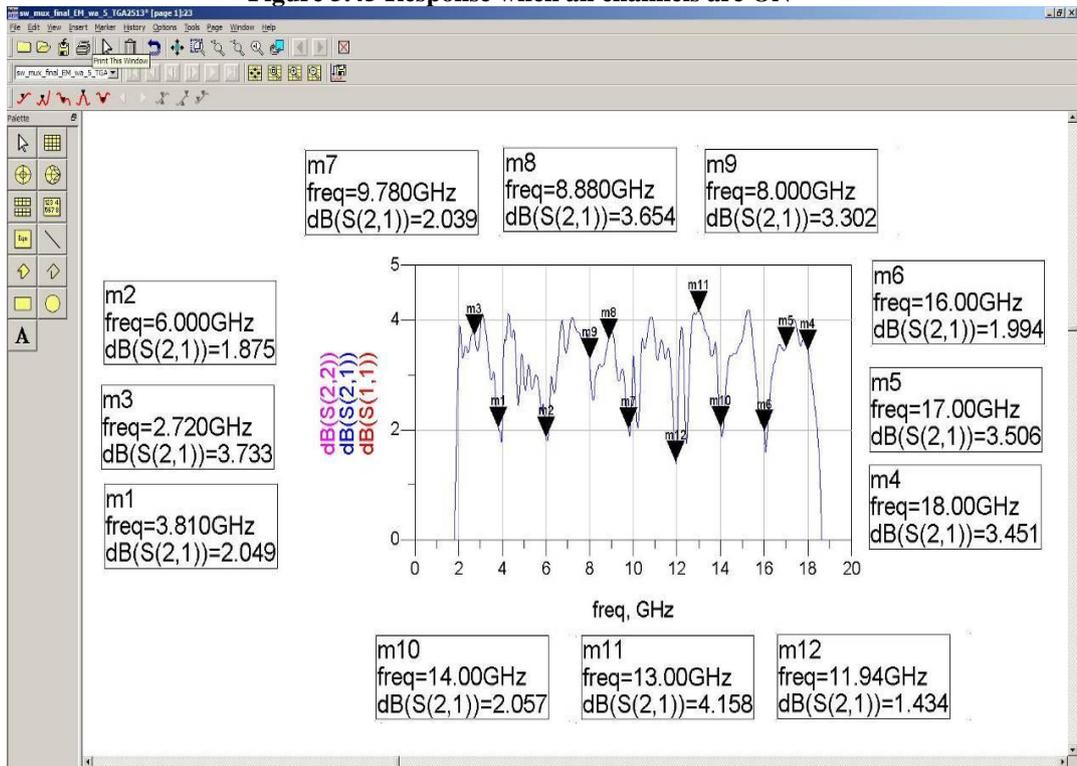
Figure 5.46 Insertion Loss when all channels are ON: zoomed
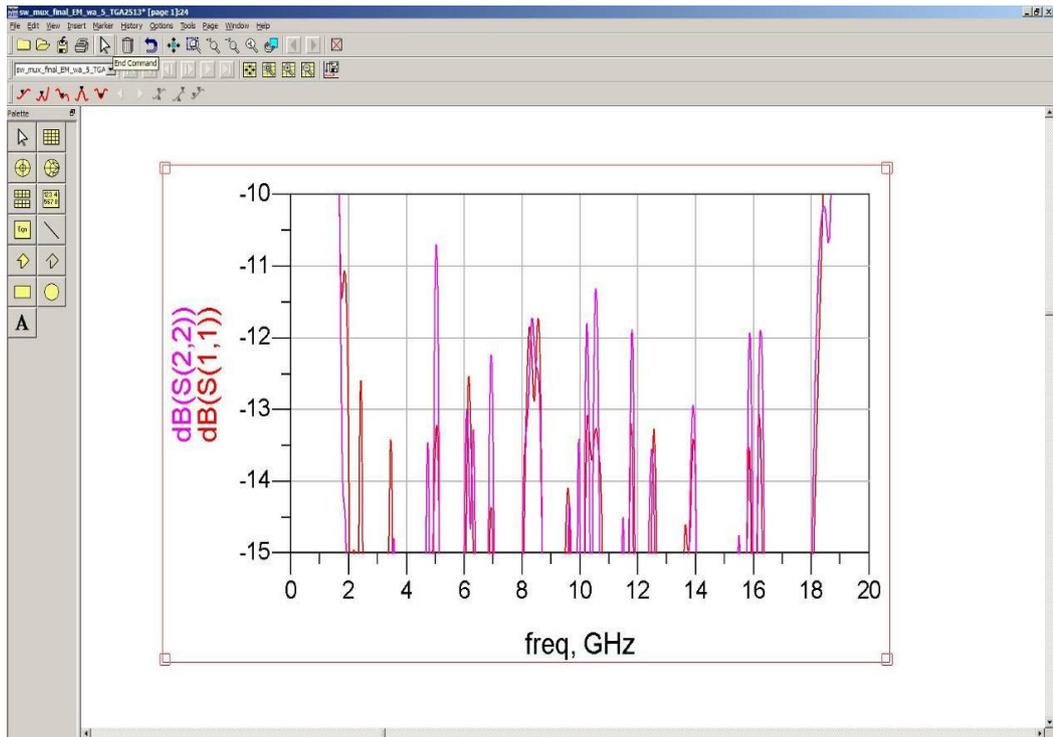
Figure 5.47 Return Loss when all channels are ON: zoomed
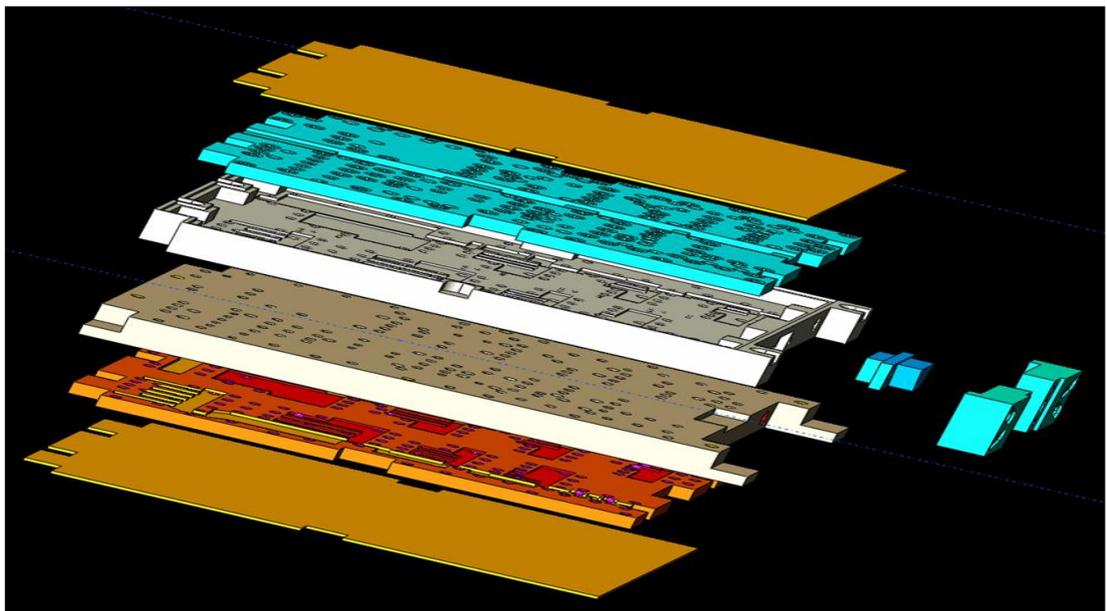
Figure 5.48 Exploded view of the compact prototype module

When Figures 5.45 to 5.50 are examined, it is seen that the corner frequencies are about 6 to 8 dBc with respect to the channel center, which is needed for a good recombination. These values can still be improved using tuning screws, but for the time being they can be as well be used without tuning. same arguments can be claimed for the overall ripple when all channels are on , it seem to have a value of 2.7 dB peak to peak, but if Figure5.49 is carefully examined, it is due to the difference between marker 11 and marker 12 which can easily be compressed to 2dB peak to peak and even more by a few runs of tuning. It is also observed that when odd channels are OFF, the suppression provided by the even channels is at least 60 dBc at the suppressed band center.

Similarly odd channels perform the same suppression when even channels are OFF. The return loss responses show that the output return loss is about 11 dB but it can be improved up to 12 dB upon reduction using tuning screws as it was experienced before for the manifold multiplexer given in Figures 5 .27 to 5.29. The input return loss is about 12 dB and can be improved to 12.5 to 13 dB by tuning screws as given in Figures 5.27 to 5.29. The difference between input and output return losses are due to use of LNA which disturbs the symmetry of the structure. All simulations carried out in CST were about half a day for each diplexer and SONNET simulations were about 2 hours per diplexer assuming a sweep consisting of 1000 points. Multiplexers took more time in CST like a day per multiplexer. This discussion completes the construction for the proposed SW_MUX and the rest will be done after the module is realized. A summary of what was done in this work and assumptions for future work will be discussed in the next chapter, i.e. conclusion part.

CHAPTER 6

CONCLUSION

In this thesis the aim was to design an 8 channel switched multiplexer covering 2-18 GHz band, with channels 2-4 GHz, 4-6 GHz, 6-8 GHz, 8-10 GHz, 10-12 GHz, 12-14 GHz, 14-16 GHz and 16-18 GHz. The channels are desired to be switched ON and OFF in any combination (totally 256 stages). The targeted return loss should be better than 10 dB at the input and 7.5 dB at the output when all channels are ON with overall ripple less than 2 dB. When any channel is OFF, the suppression at the center of the OFF channel should be greater than 50 dB. These are typical values seen in the classical available switched multiplexers.

A novel topology is used to design a switched multiplexer exceeding the targeted specifications. The input return loss is better than 12 dB and the output return loss is better than 11 dB. The overall ripple when all channels are ON is about 2 dB. When any channel is OFF, the suppression at its center is better than 55 dB.

The new topology there are two noncontiguous switched multiplexer modules containing the the channels 2-4 GHz, 6-8 GHz, 10-12 GHz and 14-16 GHz named as odd channels and 4-6 GHz, 8-10 GHz, 12-14 GHz and 16-18 GHz, named as even channels to improve isolation between adjacent channels. The input signal is split at input into the two multiplexer and the outputs of the multiplexers are combined by 2-18 GHz power dividers.

The even and odd channel switched multiplexers contain three blocks: The input multiplexer, switch + Low Noise Amplifier + attenuator block and the output multiplexer. The input and output multiplexers are identical while the value of attenuators change from channel to channel for amplitude equalization. The input/output multiplexers are designed using a novel technique that transforms a

155

contiguous manifold multiplexer into a non-contiguous multiplexer to improve isolation between adjacent channels.

The even half contiguous manifold multiplexer contains contiguous channels 4-8 GHz, 8-12 GHz, 12-16 GHz and 16-20 GHz formed by LP-HP diplexers with cross-over frequencies 4-8-12-16 GHz. The HP outputs of these channels are split by LP-HP diplexers with corner frequencies at the centers of the channels, 6-10-14 GHz. Then only the LP outputs of these diplexers are fed to the output to form a non-contiguous multiplexer with channels 4-6 GHz, 8-10 GHz, 12-14 GHz and 16-18 GHz. The HP outputs of LP-HP diplexers are terminated in 50 ohms.

The odd half manifold contains the contiguous channels 2-6 GHz, 6-10 GHz, 10-14 GHz and 14-18 GHz. Similar to the even channel cases, the 4 GHz wide channels are split into 2 GHz halves with LP-HP diplexers with cross-over frequencies 4-8-12-16 GHz, yielding noncontiguous odd channels with 2 GHz bandwidth: 2-4 GHz, 6-8 GHz, 10-12 GHz and 14-16 GHz.

It should be noted that the LP-HP diplexers used in the formation of 2 GHz noncontiguous channels of the even half are identical to the LP-HP diplexers of the manifold of the odd half and vice versa. Thus, any LP-HP diplexer is used four times in the switched multiplexer simplifying the design and implementation.

The incorporation of LP-HP diplexer to form noncontiguous channels is a novel approach. This approach is actually equivalent to forming 2 GHz bandwidth BPF's without effecting responses of the other channels. If BPF's were used to form the 2 GHz channels, then the reflections from the BPF stopband frequencies would degrade the performances of other channels. Using LP-HP diplexers instead of BPF's directs these reflections to the 50 ohms terminations of the HP channel of the LP-HP diplexers. Hence the level of degradation in the return loss when any channel is switched OFF is minimized.

The diplexers forming the switched multiplexer are designed using a novel approach which incorporate open circuited parallel coupled line as diplexing element. This structure acts as an integral part of the diplexer and contributes its performance.

The LP-HP diplexers with cross over frequencies 4, 6, 8, 10, 12, 14 and16 GHz are designed in the filter software Filpro, linear simulation and optimization are carried out on ADS whose results are transferred to Electromagnetic Simulation softwares Sonnet and CST. The diplexers are then fabricated successfully in suspended stripline with return losses better than 17 dB and insertion loss values better than 1 dB. The suppression at 1 GHz away from each band edge are better than 30 dBc in each channel. Since two diplexers are used to form a channel this implies a rejection of 60 dBc at the adjacent band center.

The implemented LP-HP diplexers are then combined to form the even and odd channel multiplexers. The measurement results are better than simulations.

The measured results of the individual diplexers are then combined with attenuator+Amplifier blocks to inspect the problems for amplitude equalization of the channels. It is observed that this approach is suitable. Thus, the modules are ready for the implementation of the targeted switched multiplexer.

In summary, it is shown that the design and implementation of switched multiplexers using the new topology and new techniques is possible leading to results which are better than the existing techniques.

Further work in this area would be investigation of the problems in the formation of the switched multiplexer and, if necessary, revise the design and implementation of LP-HP diplexers considering the constraints for different applications, like miniaturization for size reduction, for higher number of channels, with different channel widths, etc.

157

REFERENCES

[1] R. G. Veltrop and R. B. Wilds, "Modified Tables for the Design of Optimum Diplexers", The Microwave Journal, 76, June 1964.

[2] R. J. Wenzel, "Applications of Exact Synthesis Methods to Multichannel Filter Design", IEEE Trans. MTT-13, No. 1 , pp. 5 - 15, Jan. 1965.

[3] R. J. Wenzel, "Wideband High-Selectivity Diplexers Utilizing Digital Elliptic Filters", IEEE Trans. MTT- 15, No. 12, pp. 669 - 680, Dec. 1967.

[4] G. L. Matthaei and E. G. Crystal: " Theory and Design of Diplexers and Multiplexers", Advances in Microwaves, V. 2, L. Young, Editor, Academic Press, 1967.

[5] R. J. Wenzel, "Some General Properties of Commensurate Linelength Complementary and pseudo- complementary Microwave Filters", IEEE Trans. MTT-16, No. 3, pp. 191-192, March 1968.

[6] R. J. Wenzel, " Printed Circuit Complementary Filters for Narrow Bandwidth Multiplexers", IEEE Trans. MTT- 16, No. 3, pp. 147-157, March 1968.

[7] E. G. Cristal and U. H. Gysel, "New Compact Multiplexer for Stripline and MIC", 1973 European Microwave Conference, B3.1, 1973.

[8] C. K. Mok, "Design of Evanescent mode Waveguide Diplexers", IEEE Trans. MTT, Vol. 21, pp.43-48, Jan. 1973.

[9] A. E. Atia, "Computer Aided Design of Waveguide Multiplexers", IEEE Trans. MTT, Vol. 22, pp.332-338, March 1974.

[10] J. D. Rhodes, "Design Formulas for Bandpass Channel Diplexers", IEEE Proc. PGMTT Int. Symp., pp. 112- 115, June 1976.

[11] J. D. Rhodes, "Direct Design of Symmetrical Interacting Bandpass Channel Diplexers" IEE Journal on Microwaves, Optics and Acoustics", Vol. 1, pp. 33-40, Sept. 1976.

[12] J. L. Haines and J. D. Rhodes, "Direct Design Formulas for Asymmetric Bandpass Channel Diplexers", IEEE Trans. MTT, Vol. 25, pp. 807-813, Oct. 1977.

[13] R. J. Wenzel and W. G. Erlinger, "Narrowband Contiguous Multiplexing Filters with Arbitrary Amplitude and Phase Response", IEEE Proc. PGMTT Int. Symp., pp. 116- 118, June 1976.

[14] P. M. La Tourette, "Multi-octave Combline Filter Multiplexers", IEEE MTT-S Symp. Digest, pp. 298-301, 1977.

[15] P. M. La Tourette, "Combline Filter Multiplexers", Microwave Journal, pp. 55-59, Aug. 1977.

[16] P. M. La Tourette and J. L. Roberts, "Extended junction Multiplexers", IEEE MTT-S Symp. Digest, pp. 214 - 216, 1978.

[17] J. A. G. Malherbe, "Microwave Transmission Line Filters", Artech House, Dedham, 1980.

[18] J. D. Rhodes and R. Levy, "A Generalized Multiplexer Theory", IEEE Trans. MTT, Vol. MTT-27, pp. 99-111, Feb. 1979.

[19] J. D. Rhodes and R. Levy, "Design of General Manifold Multiplexer", IEEE Trans. MTT, Vol. MTT-27, pp. 111- 123, Feb. 1979.

[20] J. D. Rhodes and J. E. Dean, "MIC Broadband Filters and Multiplexers", 1979 European Microwave Conference Proc., pp. 407-410, 1979.

[21] S. A. Alseyab, J. D. Rhodes, "Design Procedure for multioctave combline filter multiplexers", IEE Proc., Vol. 127, Pt. H, No. 6, Dec. 1980.

[22] J. Neirynck, C. H. Carlin, "Synthesis of Lossless Reciprocal Three Port Based on a Canonic form of Its Scattering Matrix", IEEE Trans. on Circuits and Systems, Vol. 28, 736-752, July 1981.

[23] H. L. Thal, "Transmit-receive multiplexer for the 12-14 GHz band", IEEE Trans. MTT, Vol. 30, pp. 1324-1330, Sept. 1982.

[24] R. G. Egri, A. E. Williams and A. E. Atia, "A Contiguous band multiplexer design", IEEE MTT-S Digest, pp. 86-88, 1983.

[25] M. H. Chen, "A 12 channel contiguous band multiplexer at Ku-band", IEEE MTT-S Digest, pp. 77-79, 1983.

[26]S. C. Holme, "A 12 GHz 12 channel contiguous multiplexer for satellite applications ", IEEE MTT-S Digest, pp. 295-296, 1984.

[27]R. Tong and D. Smith, "A 12 channel contiguous band multiplexer for satellite application", IEEE MTT-S Digest, pp. 297-298, 1984.

[28]J. W. Bandler, W. Kellerman and K. Madsen, "A superlinearly convergent minimax algorithm for microwave circuits design", IEEE Trans. MTT, Vol. 33, pp. 1519- 1530, Dec. 1985.

[29]J. W. Bandler, S. H. Chen, S. Daijavad, W. Kellerman, M. Renault and Q. J. Zhang, "Large scale minimax optimization of microwave multiplexers ", Proc. Eu. Mic. Conf. pp. 435-440, Dublin, Sept. 1986.

[30]R. Valdhieck and B. Varailhon, "Computer Aided Design of Parallel Connected Millimeter-wave Diplexers, Multiplexers", IEEE MTT-S Dig., pp. 435- 438, 1988.

[31]J. Dittloff and F. Arndt, "Rigorous Design of Septate Multiplexers with Printed Circuit Elements", IEEE MTT-S Dig., pp.431-434, 1988

[32]Y. S. Zhu, W. K. Chen, "On the Design of Diplexer Having Butterworth Characteristics", IEEE Trans. on Circuits and Systems, Vol. 35, 1455-1457, Nov. 1988.

[33]Z. M. Wang and W. K. Chen, "The Design of Symmetrical Diplexer Composed of Canonical Butterworth Two-Port Networks", Proc. IEEE International Sym. On Circuits and Systems, 1179, 1988.

[34]J. Dittloff and F. Arndt, "Rigorous Field Theory Design of Millimeter-wave E-plane Integrated Circuit Multiplexers", IEEE Trans. MTT, vol. 37, pp. 340-350, Feb. 1989.

[35]Y. S. Zhu, W. K. Chen, "A Theorem on Complex normalized Reflection Coefficient and its applications", IEEE Trans. on Circuits and Systems, Vol. 36, 1238-1244, Sept. 1989.

[36] D. C. Youla and F. Winter, "New Theorems in the Synthesis of Passive Multiplexers", Int. Journal of Circuit Theory and Applications, Vol. 19, pp. 341-364, 1991.

[37]X. P. Liang, K. A. Zaki and A. E. Atia, "A rigorous three plane mode matching technique for characterizing waveguide T-junctions and its applications in multiplexer design", IEEE Trans. MTT, Vol. 39, pp. 2138-2147, Dec. 1991.

[38] D. C. Youla, S. U. Pillai, F. Winter, "Theory and Design of Maximally Flat Lowpass Highpass Reactance Ladder Diplexers", IEEE Trans. on Circuits and Systems, Vol. 39, 337-350, May 1992.

[39] X. P. Liang, K. A. Zaki and A. E. Atia, "Channel expansion and tolerance analysis of waveguide manifold multiplexers", IEEE Trans. MTT, Vol. 40, pp. 1591- 1594, July 1992.

[40] M. Guglielmi, "Optimum CAD procedure for manifold diplexers", IEEE, MTT-S International Microwave Symposium Digest, pp. 1081-1084, June 1993.

[41] A. Morini and T. Rozzi, "Design of Optimum Three-port Symmetrical Junctions for Diplexer applications", IEEE MTT-S Dig., pp. 739- 742, 1994.

[42] A. Morini and T. Rozzi, "Constraints to the Optimum Performance and Bandwidth Limitations of Diplexers Employing Symmetric Three-port Junctions", IEEE Trans. MTT, vol. 44, no. 2, pp. 242- 248, Feb. 1996.

[43] O. Apaydin, "Novel Methods for Synthesis of Diplexers with Adjustable Crossover Attenuation", M. Sc. Thesis, EEE Dept. Middle East Technical University, Ankara,Turkey, 1994.

[44] U. Koyaz, "Synthesis of Lumped and Distributed Filters and Diplexers", Ph. D. Thesis, EEE Dept. Middle East Technical University, Ankara,Turkey, 1994.

[45] R. R. Mansour, S. Ye, V. Dokas, B. Dolley, G. Thomson, W. C. Tang, C. Kudsia, "Design Considerations of Superconductive Input Multiplexers for Satellite Applications", IEEE Trans. MTT-44, No. 7, pp. 1213-1228, July 1996.

[46] S. H. Talisa, M. A. Janocko, D. L. Meier, J. Talvacchio, C. Moskowitz, D. C. Buck, R. S. Nye, S. J. Pieseski, G. R. Wagner, "High Temperature Superconducting Space Qualified Multiplexers and Delay Lines", IEEE Trans. MTT-44, No. 7, pp. 1229-1239, July 1996.

[47] G. Macchiarella, S. Tamiazzo, "A novel approach to the design of microwave diplexers", (MTT-S, 2006).

[48] C. I. Mobbs, "The use of matched four-port filters to realize switched multiplexers having low amplitude and group delay ripple", IEEE Trans. MTT-35, No. 12, pp. 1183-1191, Dec. 1987.

[49] P.Hardcastle "Fully Reconfigurable 8 Channel 2-18 GHz Broadband Switched Multiplexer",Proceedings of 36th European Microwave Conference,pp 118-121.

161

[50] Richard J. Cameron, Ming Yu, "Design of Manifold Coupled Multiplexers", IEEE Microwave Magazine, October 2007,pp 46-59.

[51] FILPRO Manual, METU, 2010.

CURRICULUM VITAE

PERSONAL INFORMATION

Name,Surname: Bülent Alıcıoğlu
Nationality: Turkish
Date and Place of Birth: December 17,1977,Çayıralan.
Marital Status: Married
Phone: +903125923290
email: balici@aselsan.com.tr

EDUCATION

Degree	Institution	Year of Graduation
MS	H.U. Elect. &Electronics Eng.	2003
BS	H.U. Elect. &Electronics Eng	2000
High School	T.E.D. Ankara College High School	1995

WORK EXPERIENCE

Year	Place	Enrollment
2000	ASELSAN INC.	R/D Engineer

FOREIGN LANGUAGES

Advanced English, Fluent French.

PUBLICATIONS

[1] B. Alıcıoğlu, N. Yıldırım "Etkin Dielektrik Sabiti Kullanarak Çoklu Bağlaşık Askılı Şerit Hat Filtre Tasarımı", URSI , 2006

[2] B. Alıcıoğlu, N. Yıldırım "The Use of Offset Coupled Microstrip Combline Filters for IF filters Requiring High Selectivity", 26th ACES Symposium, 2009

[3] B. Alıcıoğlu, N. Yıldırım "On Miniaturization and Performance Improvement of Planar Wideband Bandpass Filters", EuMC 2009

HOBBIES

Reading, Computer Technologies, Gourmet, Movies, Trekking.