ADAPTIVE CONTROL OF DC LINK CURRENT IN CURRENT SOURCE CONVERTER BASED STATCOM FOR IMPROVING ITS POWER LOSSES

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ABSTRACT

ADAPTIVE CONTROL OF DC-LINK CURRENT IN CURRENT SOURCE CONVERTER BASED STATCOM FOR IMPROVING ITS POWER LOSSES

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In conventional three-phase PWM (Pulse Width Modulation) current source converter based STATCOM (Static Synchronous Compensator) applications, DC link current is kept constant at a predefined value and the reactive power of STATCOM is controlled by varying modulation index. This control strategy causes unnecessary power losses especially when the reactive power of STATCOM is low. For this purpose, in order to reduce the active power drawn by STATCOM, the modulation index can be maximized by adjusting DC link current.

Within the scope of this thesis, an adaptive control of DC link current will be designed and applied to a 0.4kV 50kVAr three phase current source converter based STATCOM so that the power losses can be reduced. The theoretical work will be compared and discussed with the experimental results.

Keywords: Current Source Converter, STATCOM, Adaptive DC link current control, space vector PWM

ÖZ

AKIM KAYNAKLI ÇEVİRGEÇ TABANLI STATKOM'DA GÜÇ KAYIPLARINI İYİLEŞTİRMEK AMACIYLA DC BAĞ AKIMININ UYARLAMALI KONTROLÜ

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Üç fazlı darbe genişliği modülasyonu (PWM) metodu uygulanan akım kaynaklı çevirgeç yapısı kullanan STATKOM uygulamalarında, DA bağ akımı önceden belirlenmiş bir değerde tutulmaktadır. Reaktif güç, modülasyon oranı değiştirilerek kontrol edilir ve bu yöntem reaktif güç düşük olduğu zaman gereksiz güç kayıplarına neden olmaktadır. Bu amaçla DA bağ akımı, modülasyon oranını maksimum yapacak şekilde ayarlanırsa STATKOM'un kayıpları azaltılabilir.
Bu tez çalışmasında, DA bağ akımı uyarlamalı kontrolü 0.4kV, 50kVAr üç faz akım kaynaklı çevirgeç tabanlı STATKOM' a uygulanarak güç kayıpları azaltılacaktır. Bu teorik çalışmalar deneysel sonuçlarla karşılaştırılacak ve yorumlanacaktır.

Anahtar Kelimeler: Akım Kaynaklı Çevirgeç, STATKOM, Uyarlamalı DA bağ akımı kontrolü, uzay vektörü darbe genişliği modulasyonu

To My Family,

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LIST OF ABBREVIATIONS

CSC	: Current Source Converter
VSC	: Voltage Source Converter
THD	: Total Harmonic Distortion
PWM	: Pulse Width Modulation
SVPWM	: Space Vector Pulse Width Modulation
SHEM	: Selective Harmonic Elimination Method
IGCT	: Integrated Gate Commutated Thyristor
GTO	: Gate Turn-Off Thyristor
FACTS	: Flexible AC Transmission Systems
AC	: Alternating Current
DC	: Direct Current
STATCOM	: Static Synchronous Compensator
TSC	: Thyristor Switched Capacitor
TCR	: Thyristor Controlled Reactor
SVC	: Static VAR Compensator
DSP	: Digital Signal Processor
VA	: Volt-Ampere
VAR	: Volt Ampere Reactive
IGBT	: Insulated Gate Bipolar Transistor
PI	: Proportional Integral

NOMENCLATURE

M	: Modulation index
θ	: Phase angle between line to line voltage and other phase current
f_s	: Switching frequency of the power semiconductor
f_1	: Supply frequency
f_c	: Corner frequency of the AC side low pass filter
I_{dc}	: Mean value of DC link current
L_{dc}	: Inductance of DC link reactor in CSC based STATCOM
R_{dc}	: Resistance of DC link reactor in CSC based STATCOM
E_{off}	: Turn off energy loss of power semiconductor during switching
E_{on}	: Turn on energy loss of power semiconductor during switching
E_{rec}	: Reverse recovery energy loss of blocking diode
V_f	: Forward voltage drop of power semiconductor

CHAPTER 1

INTRODUCTION

With the development in economy and fast advancing technology, the usage of electrical energy increases every year. The upward trend of electrical energy consumption from power networks increases the demand of reactive energy because the production, transmission and distribution of electrical energy are all realized in AC. The increase of reactive power demand at distribution systems leads to voltage drop, cable losses, transformer losses and decrease in the capacity of active power transfer.

From the beginning of the 2000s the Energy Market Regulatory Authority of Turkey (TEDAŞ) published a regulation to restrict the reactive power demand of the distribution system loads from power network. By 2004, TEDAŞ once again brought the more stringent limits to the reactive power demand due to capacity limits in generation, transmission and distribution of electricity. Especially after 2004, together with the growing importance and interest in power quality, these limits are tried to be tightened for further restriction. However, these further restrictions have not been implemented yet. The progress in reactive energy and distortion limits imposed by TEDAŞ are summarized in Table 1.1 and Table 1.2, respectively.

Table 1.1 Reactive Enegry Limits imposed by TEDAŞ

Validity of the regulations	Energy Demand/Month		
	Active %	Reactive %	
		Inductive	Capacitive
currently in use	100	≤33	≤20
by the end of 2007	100	≤20	≤15

Table 1.2 Current Limits for Transmission and Distribution Systems imposed by TEDAŞ

Ih: Harmonic component of load current at point of common coupling (3sec average value)

I_k: Maximum short circuit current at point of common coupling

I_1: Fundamental component of maximum load current at point of common coupling (15 min average value)

Even harmonics are limited to 0.25 times the following odd harmonics

Voltage Level		Medium Voltage $1<U_n<34.5$					High Voltage $34.5<U_n<154$				
Harmonic No		I_k/I_1					I_k/I_1				
		<20	20-50	50-100	100-1000	> 1000	<20	20-50	50-100	100-1000	> 1000
Odd Harmonics (I_h/I_L) %100	$3 \le h \le 9$	4	7	10	12	15	2	3.5	5.	6	7.5
	$11 \le h \le 15$	2	3.5	4.5	5.5	7	1.	1.8	2.3	2.8	3.5
	$17 \le h \le 21$	1.5	2.5	4	5	6	0.8	1.25	2	2.5	3
	$23 \le h \le 33$	0.6	1	1.5	2	2.5	0.3	0.5	0.75	1	1.25
	$h \ge 33$	0.3	0.5	0.7	1	1.4	0.15	0.25	0.35	0.5	0.7
TDD %		5	8	12	15	20	2.5	4	6	7.5	10

The approach to the power quality in distributions system is concerned with load compensation in order to maintain power quality for each load in distribution systems. In order to increase power factor and power quality of the system, reactive power compensation is required close to the load. Without compensation, reactive power increases cable losses and reduces power transmission capabilities Moreover, rapid changes in reactive power consumption may lead to terminal voltage oscillations [1]. In order to avoid the aforementioned adverse effects, reactive power should be compensated by VAr generators.

In the first decades of 20^{th} century, reactive power compensation is implemented by connecting capacitor or inductor banks through the bus via mechanical switches [1, 2]. Capacitors or inductors are switched depending on the amount of reactive power demand. The disadvantage of this method is slow response to reactive power change and imprecise reactive power control. Moreover, the reactive power generated by capacitors is strongly dependent on the bus voltage. For the last 20 years, reactive power compensators are based on force commutated power semiconductors. Thyristor controlled reactor (TCR) and thyristor controlled capacitor (TCC) are the reactive power compensators using force commutated solid state power electronic devices [1, 3]. The capacitor or inductor is connected in series with back to back connected thyristors. The generation of reactive power is achieved by connecting capacitor or inductor to the bus over power semiconductor. The use of this compensator improved the dynamic response and precise reactive power control [1]. However, the magnitude of reactive power is also strongly dependent on the bus voltage as in the case of mechanically switched compensators [4]. These type of compensators are good solution for steady state conditions. On the other hand, they have poor performance for transient conditions [1].

With the advanced developments in power semiconductor technology, a new type of compensator has been presented. This compensator is the static synchronous compensator (STATCOM) based on force commutated power semiconductors. STATCOM can achieve precise reactive power generation without bus voltage

dependency. The advantages of STATCOM over other compensators have been expressed in [5-7]:

- Size, weight and cost reduction,
- Equality of lagging and leading output,
- Precise and fast reactive power control with fast response,
- Possible harmonic filtering capability.

1.1 REACTIVE POWER COMPENSATION

The compensation systems are classified according to their connections with the system. Reactive power compensation can be implemented by VAr generators connected in series or parallel [8]. If the compensator is connected to the bus in parallel with load and source, the compensation system is named as shunt compensation. On the other hand, if the compensator is connected between source and the load in series, compensation system is classified as series compensation.

Series and shunt VAr compensation are utilized to control the electrical characteristics of AC system. Series compensation adjusts the distribution or transmission system parameters. Shunt compensation changes the equivalent impedance of load [9, 10].

1.1.1 Shunt Compensation

Shunt compensation is used to keep the voltage magnitude constant at the bus bar and injects current to the system in order to compensate reactive power. If the reactive current part of the source current is injected into the system close to the load, the total current drawn from the source can be minimized reducing the power loss and improving voltage regulation at load terminals [8]. The types of shunt compensation are synchronous condenser, static VAr compensator and static synchronous compensators [8, 11].

Synchronous Condenser: Synchronous condenser is a simple synchronous machine connected to the system. It can be used in both transmission and distribution voltage level systems. This compensator is not preferable because significant amount of protective and starting equipments are necessary.

Static VAr Compensator: Thyrisor Controlled Reactor (TCR) and Thyristor Switched Capacitor (TSC) are the two types of thyristorized VAr compensators. In the thyristor controlled reactor, there are two back to back connected thyristors and a reactor in series with them. The reactor is activated by switching the thyristor resulting in a step change of reactive power in the system. TSC has the same circuit configuration with TCR. The only difference is that the capacitor is used instead of reactor. The main advantage of using these compensators is low maintenance in comparison with synchronous condenser [11]. The main drawback of this type of compensator is the generated reactive power is dependent on the bus voltage connected.

Static Synchronous Compensator: Current source or voltage source converter topologies may be used for shunt compensation [8, 11]. They improve voltage regulation, provide unity power factor on system and correct the unbalance loads. As compared with Static VAr compensators, they have the following advantages [8]:

- Generating reactive power continuously and precisely,
- High frequency of modulation results in low harmonic content of supply current,
- Self commutated VAr generators can be used for active harmonic filtering with appropriate control algorithm.

1.1.2 Series Compensation

Series compensation is directly controls the overall impedance of the system [12]. The compensation voltage has been added between the load and source voltage. By addition of voltage, the angle between load and source current becomes zero. In other words, only active current component is drawn from the source.

The types of series compensation are fixed series capacitor, thyristor controlled series capacitor and self commutated VAr compensators used for series compensation.

Fixed Series Capacitor: The capacitor is added to the end or midpoint of the line. It results in step changes for various reactive power demands.

Thyristor Controlled Series Capacitor: Capacitor is placed in series to the line with parallel TCR configuration. The main disadvantage of using this compensator is that continuous inductive reactive power operation is not allowed due to high currents flowing through thyristors [11].

Self Commutated VAr Compensators for Series Compensation: The control of reactive power is achieved by adjusting the voltage which will be added to the source voltage. The magnitude of voltage is controlled by changing modulation index and switching pattern [8]. The research work for self commutated VAr compensators used in series compensation has been explained in [13, 14]. In [13], series compensation is realized by using voltage source converter circuit topology. In [14], current source converter circuit topology is used to achieve series compensation.

1.2 STATIC SYNCHRONOUS COMPENSATOR (STATCOM)

STATCOM is a static self commutated switching power converter which is shunt connected to an AC power system in order to produce controllable capacitive or inductive currents to AC power system independent of the system voltage.

STATCOM can enhance the power transmission capability and extend steady state stability limit. In transients, it behaves like a damping element so that it extends the system transient stability [15, 16].

STATCOM can be used in transmission systems for voltage regulation [17, 18]. In distribution systems, the STATCOM is called D-STATCOM. It is used for reactive power compensation of rapidly changing loads, filtering load harmonics, balancing unbalanced loads and for the stability improvements of systems such as wind turbine applications [2, 19].

STATCOM is based on power electronic converter which has an energy storage component on the DC link side. Depending on the type of storage element, either a voltage source converter (VSC) or a current source converter (CSC) is being used [2, 15, 16, 20, 21]. Typical circuit diagrams for VSC and CSC are given in Figure 1.1 and Figure 1.2, respectively [22, 23].

In VSC configuration, the output of the converter is the three phase controllable voltages. In CSC configuration, the output is three phase controllable currents. The VSC based STATCOM is connected to the AC grid via an inductance (also named as reactor) as shown in Figure 1.1 [24]. As shown in Figure 1.2, the capacitors must be placed between the CSC and AC grid in CSC based STATCOM.

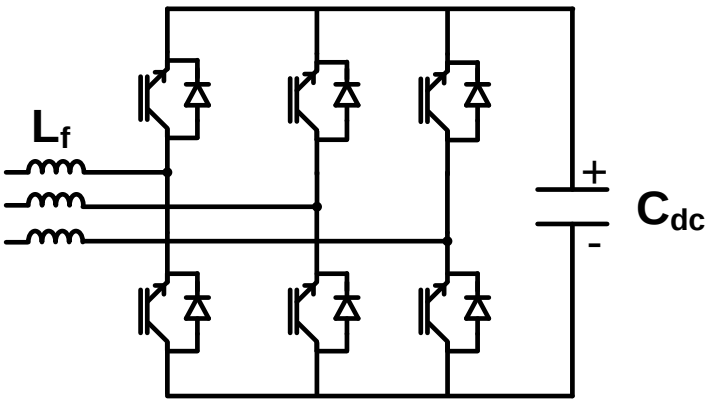

Figure 1.1 Voltage Source Converter Circuit Configuration

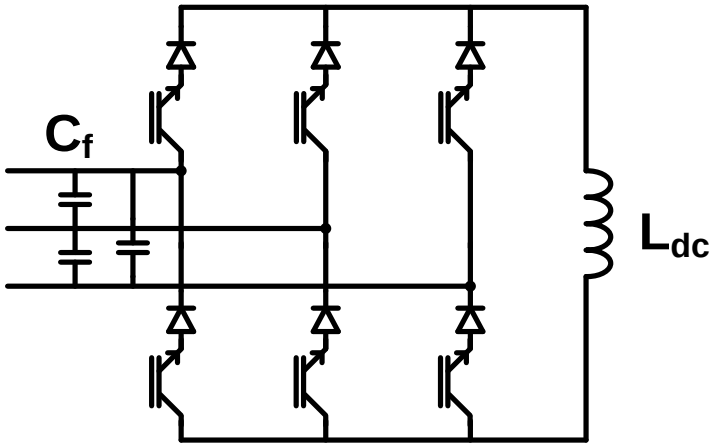

Figure 1.2 Current Source Converter Circuit Configuration

When voltage and current source converter are compared, it is seen that VSC is more popular according to advantages which are enlisted below:

- The resistance value of DC link reactor is higher than DC link capacitor. Therefore, the dc link reactor used in CSC based STATCOM consumes more active power than the DC link capacitor used in VSC based STATCOM [2, 3, 15, 24, 25].
- Due to this fact VSC has been used in various industrial applications, such as motor drives. This motivates the power semiconductor manufacturers to focus on power semiconductor switches suitable for VSC, which has unipolar voltage blocking and reverse current carrying capability. Therefore, power semiconductor switches on the market are produced according to VSC applications. On the other hand, the power semiconductor in CSC has bipolar voltage blocking and unipolar current capability [2, 3, 4, 15, 24, 25]. In order to achieve this characteristic, an extra diode should be used in series with power semiconductor switch which is available on the market for VSC applications. This increases the total cost and circuit complexity for CSC applications [25].

- As shown Figure 1.1 and Figure 1.2, VSC is coupled to AC grid via reactors and CSC is coupled to AC grid via capacitors. Since, STATCOM systems are generally connected to AC grid via a coupling transformer, the leakage reactance of the transformer can be exploited as the reactor on AC side of VSC. This results in a more compact system [2, 3].

Although the VSC has important advantages over CSC, CSC does not need any pre-charging resistor for DC link reactor or inrush limiting equipment [20, 25]. The phase and magnitude of current can be directly controlled in CSC [20]. Moreover, the capacitors on AC side of CSC together with leakage reactance of AC grid, coupling transformer and additional tuning reactor constitute an inherent second order filter which results in less harmonic distortion in line current for AC grid than that of VSC based STATCOM. Another advantage of using CSC is that it provides inherent short circuit protection [20, 26]

Although CSC is not as popular as VSC, there are research works for CSC based STATCOM for improving its performances and eliminating the disadvantages compared to VSC. Among these research works, [3] and [27] has used pre-calculated switching patterns and applied to CSC by varying phase angle with respect to AC grid in order to adjust the reactive power of STATCOM. However, active power transfer also takes place and DC link current of CSC changes with the reactive power of STATCOM. This results in charging and discharging of storage element, i.e DC link reactor, and adversely affects the transient response of STATCOM (i.e longer rise, fall and settling time) in reactive power generation. The research works [15, 16, 20, 21, 28] has derived CSC based STATCOM model from "abc" stationary frame to synchronously rotating "dq" frame. After transformation into "dq" frame, various techniques for controlling DC link and reactive power have been investigated. Explanation and implementation of space vector pulse width modulation technique are studied in [29-37]. For minimizing switching loss, minimizing switching frequency techniques have been applied in [31, 32]. In [33], addition to minimization of switching frequency, harmonic performance of space

vector pulse width modulation technique is improved and new approach for harmonic suppression is tried. Active damping method which damps the current oscillations around resonance frequency of low pass filter at the input of converter is studied in [38] and [39]. The design method of low pass filter at the input of the converter is explained in [40, 41, 42]. The critical points for designing DC link reactor are expressed in [2, 3, 27, 43].

The research works [2, 15, 20, 36] have used various pulse width modulation techniques together with different control techniques for controlling DC link and reactive power. However, these research works have kept DC link current constant over the entire operating range. As compared with [3] and [27], this approach suffers higher DC link reactor losses and converter when CSC operates other than its rated reactive power.

For wind turbine generators and industrial motor drive application, the control of DC link current is achieved. In [44], the system is used to support the grid voltage during faults and recoveries. The system consists of two converters. One of them is used to control DC link current during normal or fault conditions. The second converter is used to adjust DC link current and to manipulate the reactive power. In this application, DC link current is controlled by the help of two converters. In the research work [45], the system is used for wind farms. In this system, two CSC converters are used as in [44]. Two applications mentioned in [44] and [45], which DC link current control is applied, two converter circuits are used so that the cost of the system is much higher than single converter configuration. In addition to this, the control mechanisms are also complex to implement.

In research works on CSC based STATCOM where on-line PWM techniques were used, DC link current is kept constant over entire operating range of reactive power generation of STATCOM. In other words, DC link current value is independent of the magnitude of generated reactive power [2, 15, 16, 20, 36, 46, 47]. This condition causes same power losses (switching, conduction and DC link reactor) for the entire range of reactive power generation. If DC link current can be adjusted

according to the reactive power request of load, the switching, conduction and DC link reactor losses can be minimized. In this research work, the idea of varying DC link current together with the reactive power of STATCOM by applying on-line PWM and synchronous rotating reference frame based control theory is going to be studied.

1.3 SCOPE OF THESIS

Within the scope of this thesis, 50kVAr CSC based STATCOM which complies with the line current distortion limits in IEEE std. 519-1992 [48] has been developed at 0.4kV low voltage level for reactive power compensation of balanced loads. An IGBT and a fast recovery diode have been connected in series as shown in Figure 1.2. Space vector modulation has been chosen for generating switching signals of IGBTs. The control of reactive power and DC link current has been achieved in "dq" synchronous rotating reference frame. Active damping method has also been implemented in order to damp the amplification in current harmonics at the resonance frequency of the input filter. An adaptive control of DC link current according to the reactive power of load has been proposed so that the power losses of CSC based STATCOM can be decreased when it is operating at a reactive power level less than its rated value. The performance of the proposed method has been verified experimentally in comparison to the case where DC link current is kept constant over the entire reactive power generating range of STATCOM. Advanced active clamping method has been modified and applied in coordination with crowbar for more effective overvoltage protection in CSC applications.

In the second part of the thesis, firstly STATCOM system and operating principles of CSC will be mentioned. Later, space vector modulation technique will be explained. Then, the control of STATCOM in "dq" synchronous rotating reference frame will be mentioned. After that, active damping method and adaptive control of DC link current will be expressed.

In the third chapter, the system design of CSC based STATCOM will be presented. The selection of power semiconductor and choosing the parameters of the low pass filter at the input of CSC are explained firstly. After that, selection of DC link reactor will be presented. Then, design principles in developing power stage, which is composed of laminated bus bar and heat sinks will be given. Later, overvoltage protection of CSC based STATCOM will be explained. Finally, implemented control system will be presented.

In the fourth chapter, firstly performance criteria of CSC based STATCOM will be defined. The designed system and proposed methods such as active damping and adaptive control of DC link current are verified by experimental results.
Finally, conclusions are posted in Chapter 5.

CHAPTER 2

OPERATING PRINCIPLES

STATCOM can be used in transmission and distribution systems. STATCOM used in distribution systems is called D-STATCOM. Distribution type STATCOM can be used in medium or low voltage applications and used for compensating reactive power, load balancing, flicker damping and harmonic filtering [2, 43, 49]. In order to achieve these properties, D-STATCOM should inject unbalanced and harmonically distorted currents into the system.

In this research work, it is aimed to design CSC based STATCOM only for reactive power compensation of balanced loads which demand rapidly changing reactive power. The injected current by the designed CSC based STATCOM should have low line current harmonics which comply with IEEE 512 Std 1992. In this part of thesis, the operating principles of the developed CSC based STATCOM will be explained.

2.1 CSC BASED STATCOM SYSTEM CONFIGURATION

The general circuit topology of CSC based STATCOM is illustrated in Figure 2.1 [25, 27, 36]. It is composed of six controllable semiconductor switches (s_1, s_2, s_3, s_4, s_5, s_6) which have bidirectional voltage blocking and unidirectional current conduction properties.

DC link reactor (L_{dc}) is used at the DC side of the converter as the energy storage element. The time constant of DC link reactor is high so that the current passing through this reactor during switching period is assumed to be constant [2, 3].

The current passing through the DC link reactor is switched to the AC side by closing and opening the semiconductor switches. The switched line currents of CSC (i_A, i_B, i_C) have harmonic contents in addition to fundamental component at supply frequency. In order to eliminate harmonic contents before injecting the current into system, low pass filter is used. The low pass filter at the input of converter consists of capacitor and reactor. The capacitor (C_f) placed in low pass filter is inherent for CSC applications to provide low impedance path for the converter current pulses. Moreover, it provides a commutation path during transferring current from one switch to another. A series reactor (L_f) in low pass filter is optional. In this application it is used to adjust the resonance frequency of the low pass filter so that high order current harmonics injected by CSC can be filtered out.

The control system of CSC based STATCOM has two main blocks, as seen in Figure 2.2. First block calculates the reference current vectors, I_α and I_β, according to the reactive power demand of the load, the required DC link current and acrive damping. These reference vectors are used by the second block, which applies space vector pulse width modulation technique to generate the switching signals for the semiconductor switches of CSC. The detailed explanations of control blocks will be given later.

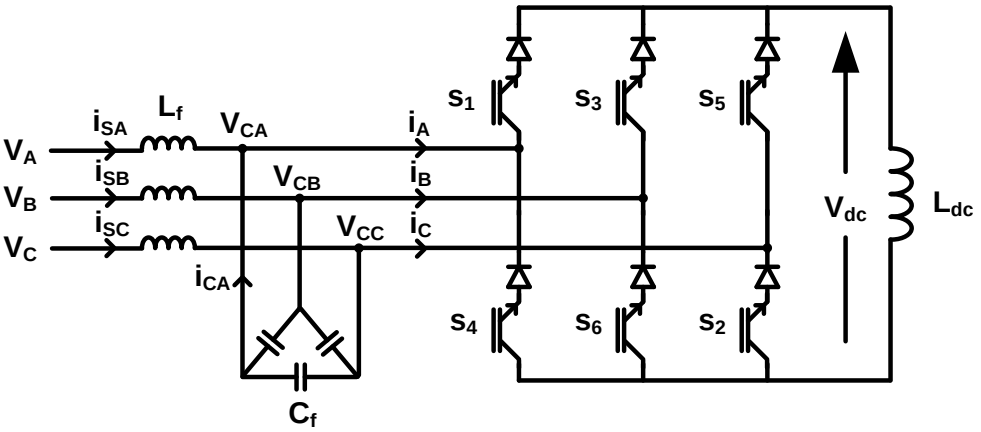

Figure 2.1 Basic Circuit Configuration of Current Source Converter

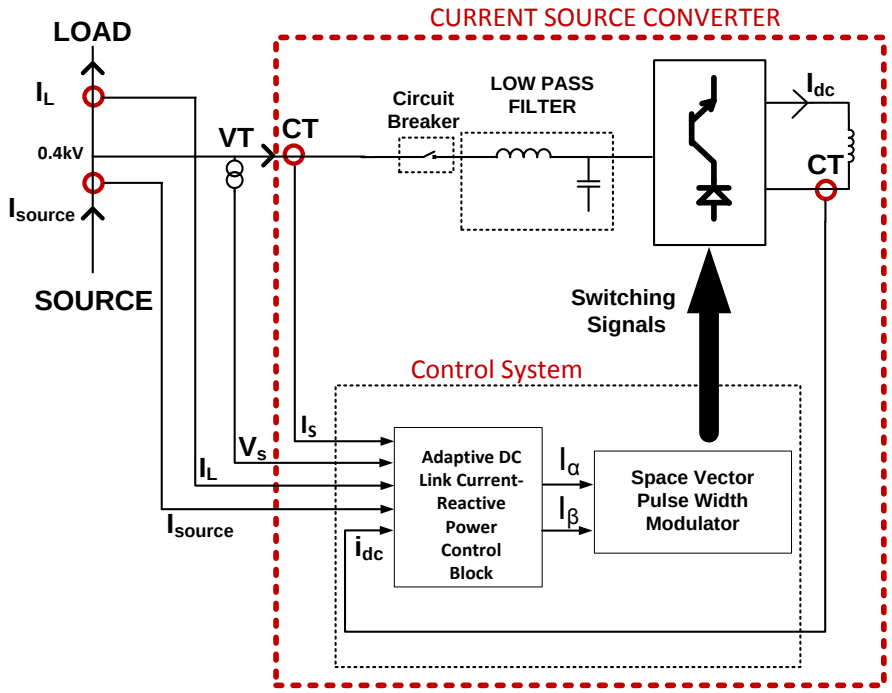

Figure 2.2 The Overall System Configuration

I_{source} : Three phase source currents, I_L: Three phase load current, I_S: Three phase filtered converter current, V_S: Three phase voltage at common point of connection i_{dc}: DC link reactor current.

2.2 SPACE VECTOR PULSE WIDTH MODULATION

With the development of semiconductor technology, the pulse width modulation techniques have become applicable to high power converters, where the switching frequency of semiconductor switches is in the range of 1 kHz to 20 kHz [50-54]. By the application of PWM, CSC is able to inject sinusoidal currents with less harmonic contents in addition to fundamental component. Moreover, ripples on DC link current can also be minimized by the use of PWM with high switching frequency (i.e, from 1 kHz to 20 kHz). However, high switching frequency increases switching losses on semiconductor switch. The switching loss of each semiconductor switch can be calculated by using (2.1) [55];

$$P_{LOSS} = f_s.\frac{3}{\pi}.\ E_{ON,I} + E_{OFF,I} + E_{OFF,D},\ .\frac{i_{dc}}{i_{ref}}.\frac{V_{dc}}{V_{ref}} \qquad (2.1)$$

where;

f_s : Switching frequency,

$E_{ON,I}$: Turn on energy of a power semiconductor at i_{ref} and V_{ref},

$E_{\mathrm{OFF},I}$: Turn off energy of a power semiconductor at i_{ref} and V_{ref},

$E_{OFF,D}$: Turn off energy of the diode at i_{ref} and V_{ref},

i_{dc} : DC link reactor current,

V_{dc} : Blocking voltage across semiconductor switch after it is switched off,

i_{ref} : On state current at which $E_{ON,I}$, $E_{\mathrm{OFF},I}$ and $E_{OFF,D}$ are obtained from switching tests and specified by the semiconductor manufacturer,

V_{ref} : Voltage at which $E_{ON,I}$, $E_{\mathrm{OFF},I}$ and $E_{OFF,D}$ are obtained from switching tests and specified by the semiconductor manufacturer.

Equation (2.1) indicates that the switching losses are directly dependent on the switching frequency and DC link current.

The modulation techniques used in STATCOM applications can be classified into two categories: off-line and on-line modulation techniques [2, 3]. Selective Harmonic Elimination Method (SHEM) can be given as an example for widely used off-line modulation technique [3, 34, 39]. In SHEM, the predefined switching pattern is applied to the switches. The advantage of using SHEM is that the selected number of low order harmonics such as 5th, 7th can be eliminated [3]. The disadvantage of using SHEM is slow dynamic response to rapidly changing reactive power demand of the load. Moreover, when there is need for elimination of more number of harmonics, the number of switching angles should be increased. Therefore, more memory area is required in the processor. Another drawback of off-line modulation technique is that active damping method cannot be applied [2]. Space vector pulse width modulation (SVPWM), dead band sinusoidal pulse width modulation (DSPWM) and modified dead band sinusoidal pulse width modulation techniques (MDSPWM) are widely used on-line modulation techniques for CSC applications [2]. In selecting modulation technique among the on-line modulation techniques, the following features of modulation techniques should be considered:

- Resultant switching frequency of semiconductors,
- Total harmonic distortion caused,
- Lower order harmonics injected into the system,
- The implementation challenge of modulation technique.

The switching frequency is directly related to switching loss of semiconductor as illustrated in equation (2.1). Therefore, the method having lower switching frequency should be selected. If carrier frequency of all three methods is chosen same, DSPWM has the highest switching frequency. MDSPWM and SVPWM have same switching frequency [2, 24]. From view of total harmonic distortion and lower order harmonics injected into the system, MDSPWM and SVPWM have nearly same characteristics [2]. Since, MDSPWM is analog on-line modulation and SVPWM is digital on-line modulation technique, SVPWM is easier to implement. Therefore, SVPWM has been applied in this research work.

The space vector PWM algorithm has three major steps:

- Synchronization with voltage at common point of connection,
- Deciding the three vector within the 9 possible vector for generating reference vector;
- Calculation of the duty cycles of the selected three vectors.

While implementing Space Vector Modulation technique in CSC topology, the continuity of the DC link current flow must be guaranteed. In order to satisfy this requirement, one of the semiconductor switches from the upper half bridge (i.e., s_1, s_3, s_5) and one from the lower bridge (i.e., s_2, s_4, s_6) bottom switches should be in conduction at any time. This is illustrated in Figure 2.3.

Switch combinations of CSC can also be expressed mathematically for one switching period as given (2.2).

$$\begin{aligned} s_1 + s_3 + s_5 &= 1 \\ s_2 + s_4 + s_6 &= 1 \end{aligned} \tag{2.2}$$

As seen from Figure 2.3, line currents of CSC (i.e., i_A, i_B, i_C) are equal to DC link current (i_{dc}) according to the state of semiconductor switches. This is expressed in Table 2.1.

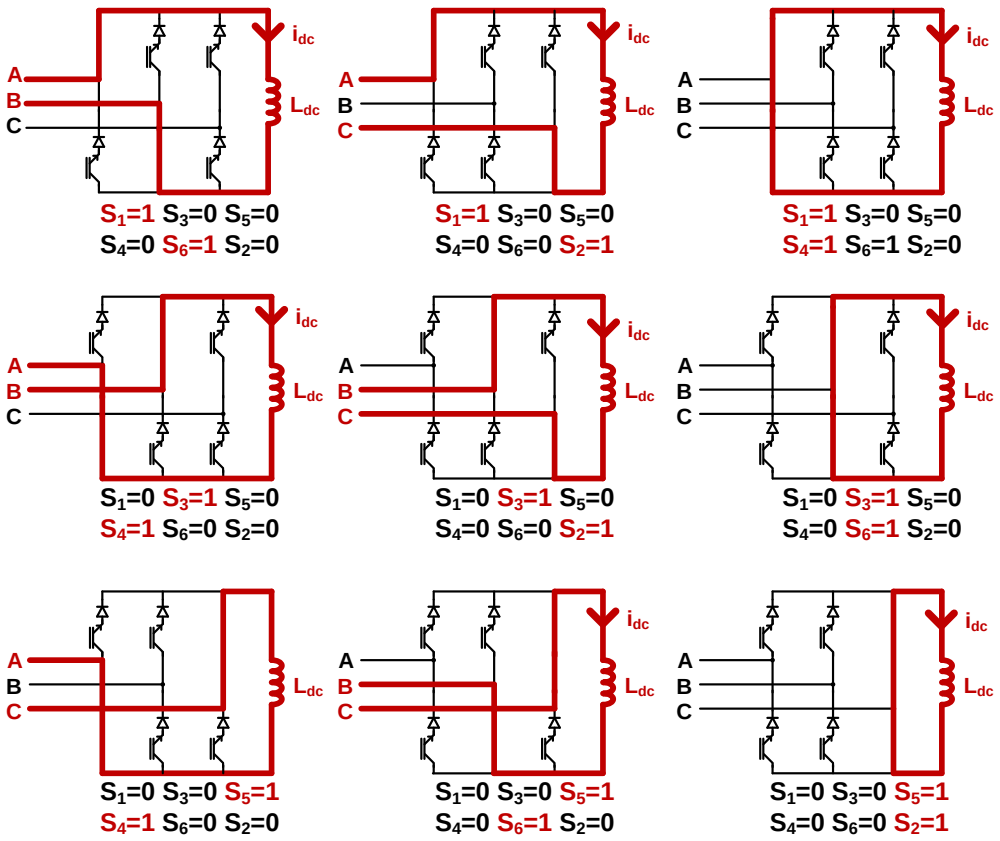

Figure 2.3 All Switching Combinations and Current Paths

Referring the Table 2.1, there will be non zero DC link current at AC side of the converter for six active switching states (e.g. 12, 23, 34, 45, 56, 61). There will be zero DC link current at line currents for zero switching states (e.g. 14, 36, and 52). None zero vectors I_j, (j=1-6) shown in Figure 2.4 have defined directions in complex plane. These vectors connect the DC side of the converter to the AC side.

Table 2.1 Switching States for CSC, Corresponding Line Currents and Space Vectors

Switching States	Switches						Line Currents			Space Vector
	S1	S2	S3	S4	S5	S6	i_A	i_B	i_C	
61	1	0	0	0	0	1	i_{dc}	$-i_{dc}$	0	I_1
12	1	1	0	0	0	0	i_{dc}	0	$-i_{dc}$	I_2
23	0	1	1	0	0	0	0	i_{dc}	$-i_{dc}$	I_3
34	0	0	1	1	0	0	$-i_{dc}$	i_{dc}	0	I_4
45	0	0	0	1	1	0	$-i_{dc}$	0	i_{dc}	I_5
56	0	0	0	0	1	1	0	$-i_{dc}$	i_{dc}	I_6
14	1	0	0	1	0	0	0	0	0	I_0
36	0	0	1	0	0	1	0	0	0	
52	0	1	0	0	1	0	0	0	0	

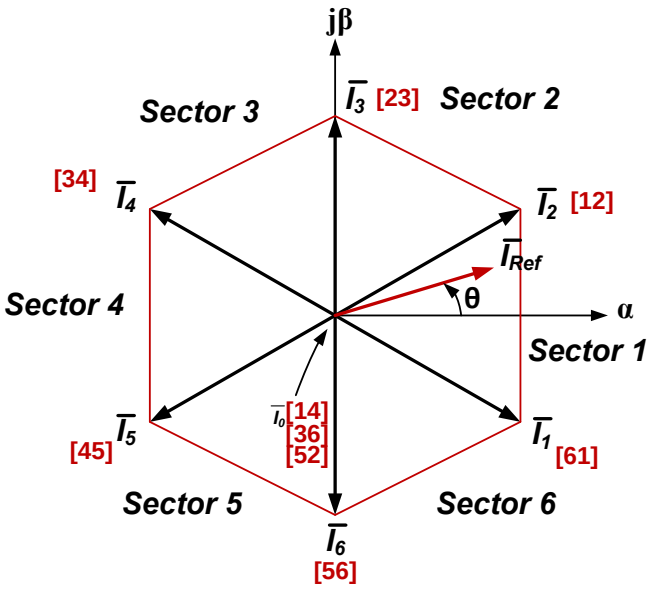

Figure 2.4 Space vectors, related sectors, and the reference current vector I_{ref} in complex plane

The current space vector, $I_\iota\ t$ which can be expressed in terms of line current at any time is given in (2.3). It is defined as the reference current vector in [29, 30].

$$I_\iota(\mathrm{t}) = \frac{2}{3}\ i_A\ t\ +\ i_B\ t\ .\mathrm{e}^{-\mathrm{J}\frac{2\pi}{3}}\ i_C\ t\ .\mathrm{e}^{\mathrm{J}\frac{2\pi}{3}} \tag{2.3}$$

For active switching state "61" given in Table 2.1, the switch 1 and 6 is turned on and line currents are given in (2.4) as expressed in Table 2.1.

$$i_A\ t\ = i_{dc},\ i_B\ t\ = -i_{dc},\ i_C\ t\ = 0 \tag{2.4}$$

Substituting (2.4) into (2.3) yields (2.5).

$$I_1 = \frac{2}{\overline{3}}.\,i_{dc}.\,e^{j(-\frac{\pi}{6})} \tag{2.5}$$

The other space vectors of active switching states given in Table 2.1 can be derived as given in (2.6) [56],

$$I_k = \frac{2}{\overline{3}}.\,i_{dc}.\,e^{j(\ k-1\ \frac{\pi}{3}-\frac{\pi}{6})}\ for\ k = 1,2\ \ldots 6 \tag{2.6}$$

Where k denotes the number of space vector defined in Table 2.1.

Complex plane is divided into 6 sector by the current space vectors, I_1, I_2, I_3, I_4, I_5, I_6, which are previously defined in Table 2.1. The time domain relationships between the sectors (1, 2, 3, 4, 5, 6) and input line current (i_A, i_B, i_C) waveforms are shown in Figure 2.5.

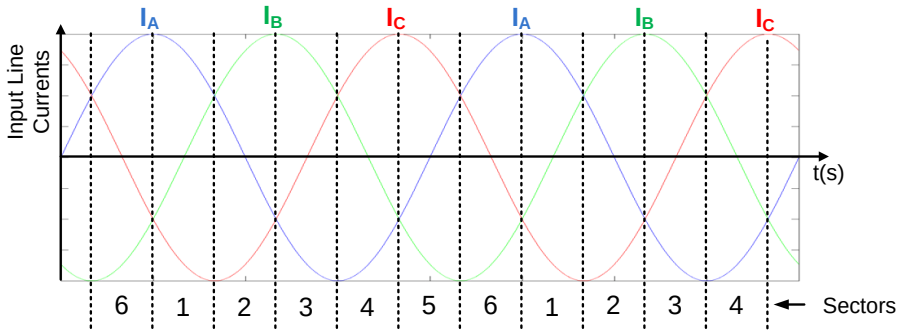

Figure 2.5 Relationships between the input line current waveforms and the sectors in time domain

The reference current vector I_{ref} shown in Figure 2.6 can be generated by using of two adjacent space vectors (I_1 and I_2) and one of zero current vector (stated in Table 2.1). For one switching period Ts, the reference current vector, I_{ref} can be generated as described below.

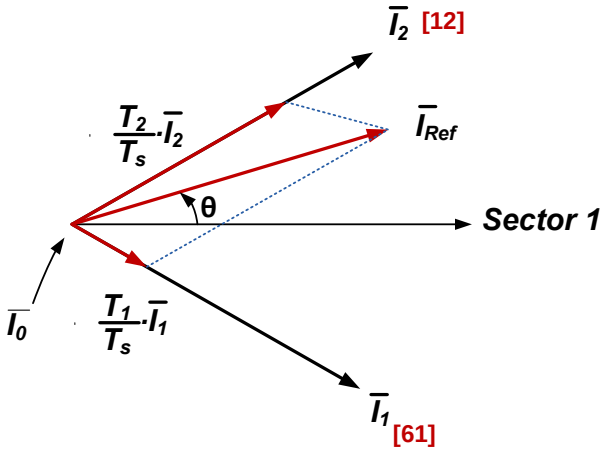

Figure 2.6 Reference current vector construction

"θ" shown in Figure 2.6 is the angular displacement. By using two space vectors, $\overline{I_1}$, $\overline{I_2}$ and one zero vector, $\overline{I_0}$, the reference current vector, $\overline{I_{ref}}$ can be obtained. By

using ampere-second balance equation, the relationship between space, $\overline{I_1}$, $\overline{I_2}$ and reference vector $\overline{I_{ref}}$ can be given in (2.7). The relationship between switching period and dwell times is given in (2.8) [56].

$$T_S.\overline{I_{ref}} = T_1.\overline{I_1} + T_2.\overline{I_2} + T_0.\overline{I_0} \tag{2.7}$$

$$T_S = T_1 + T_2 + T_0. \tag{2.8}$$

Where, T_1, T_2 and T_0 are the dwell times for the vectors $\overline{I_1}$, $\overline{I_2}$ and $\overline{I_0}$, respectively. The vectors of I_{ref}, I_1 and I_2 can be defined as (2.9).

$$\begin{aligned} I_{ref} &= I_{ref}.e^{j\theta} \\ I_1 &= \frac{2}{\overline{3}}.i_{dc}.e^{j(-\frac{\pi}{6})} \\ I_2 &= \frac{2}{\overline{3}}.i_{dc}.e^{j(\frac{\pi}{6})} \end{aligned} \tag{2.9}$$

Substituting (2.9) into (2.7) and splitting the resultant equation into real (α axis) and imaginary axis (β axis) leads to equation (2.10) [56].

$$\begin{aligned} Re:\ I_{ref}.\cos\theta\ .T_S &= i_{dc}.(T_1 + T_2) \\ Im:\ I_{ref}.\sin\theta\ .T_S &= \frac{1}{\overline{3}} i_{dc}.(-T_1 + T_2) \end{aligned} \tag{2.10}$$

Solving (2.10) together with (2.8) gives (2.11) [56].

$$\begin{aligned} T_1 &= M.\sin\left(\frac{\pi}{6} - \theta\right).T_S \\ T_2 &= M.\sin\left(\frac{\pi}{6} + \theta\right).T_S \\ T_0 &= T_S - T_1 - T_2. \end{aligned} \tag{2.11}$$

Where M is the modulation index and given by (2.12).

$$M = \frac{I_{ref}}{i_{dc}} \tag{2.12}$$

When reference vector, I_{ref} is in the other sectors, modified angle θ' is used and modified angle can be calculated as (2.13).

$$\theta' = \theta - \ k-1 \ .\frac{\pi}{3} \ for - \frac{\pi}{6} \leq \ \theta' \ \leq \frac{\pi}{6} \tag{2.13}$$

Where *k* represents the number of sector.

Maximum length of the reference vector, $I_{ref,max}$, corresponds to the radius of the largest circle that can be inscribed within the hexagon as shown in Figure 2.4 [56]. Hexagon is formed by six active switching state vectors having a length of $\frac{2}{\overline{3}} i_{dc}$, and $I_{ref,max}$ can be found from (2.14) [56].

$$I_{ref,max} = \frac{2}{\overline{3}} . i_{dc} . \frac{\overline{3}}{2} = i_{dc} \tag{2.14}$$

Substituting (2.14) into (2.12) gives maximum modulation index. The range of modulation index is given in (2.15) [56].

$$0 \ \leq \ M \ \leq 1 \tag{2.15}$$

A modulation index greater than one is not preferred because an index greater than one causes the controller to operate in non-linear region. The problems due to non-linear operation are: i) inherent modulator subcarrier frequency harmonic-distortion-dependent waveform degradation, ii) current-regulator dependent performance reduction. The controllers are heavily burdened by the feedback current subcarrier frequency harmonics and regulator saturation and oscillatory operations result in additional performance degradation [57].

2.3 CONTROL OF STATCOM IN SYNCHRONOUS ROTATING DQ FRAME

In synchronous rotating "dq" reference frame based control, the system variables used in adaptive DC link-reactive power control block are transformed into synchronous rotating "dq" reference frame. After transformation, the reference frame rotates at constant angular frequency, w, which is also equal to angular frequency of three phase supply voltages. Three sinusoidal variables become two orthogonal variables and DC quantities at steady state.

Synchronous Rotating Reference Frame

The three phase system variables such as load currents and filtered converter currents are transformed into stationary "αβ" reference frame by using Clarke transformation. By using Park transformation, two variables in stationary "αβ" reference frame are transformed into "dq" frame rotating synchronously with line voltage. The transformation matrix from "abc" to "αβ" and "αβ" to "dq" frame are given in (2.16) and (2.17), respectively.

$$\begin{matrix} x_\alpha \\ x_\beta \end{matrix} = \frac{2}{3} \cdot \begin{matrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{matrix} \cdot \begin{matrix} x_a \\ x_b \\ x_c \end{matrix} \tag{2.16}$$

$$\begin{matrix} x_d \\ x_q \end{matrix} = \begin{matrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{matrix} \cdot \begin{matrix} x_\alpha \\ x_\beta \end{matrix} \tag{2.17}$$

"θ" represents the angular position of reference frame and x denotes current or voltage. Angle "θ" is used to transform the system variables into rotating "dq" frame. Angle "θ" is calculated by phase locked loop systems [24].

The "abc", "αβ" and "dq" frame variables are shown in Figure 2.7.

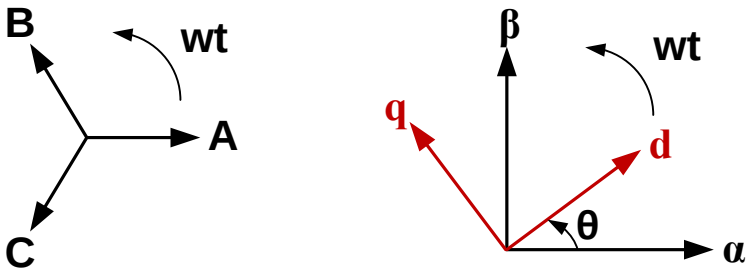

Figure 2.7 “abc” “αβ” and “dq” frame variables

After applying PI and other control operations, the reference vector in “dq” frame is obtained. The reference vector in “dq” frame is back transformed into “αβ” reference frame and space vector modulator (shown in Figure 2.2) takes reference vector in “αβ” reference frame and generates switching patterns required for generating reference vector.

The three phase CSC based STATCOM can be modeled in synchronous rotating “dq” frame [15, 16, 20, 21, 28]. In Figure 2.8, “abc” stationary frame electrical variables of CSC based STATCOM are shown. After applying Clarke and Park transformations, CSC based STATCOM and other system variables are transformed into synchronously rotating “dq” frame. The single line diagram of system in “dq” frame is shown in Figure 2.9.

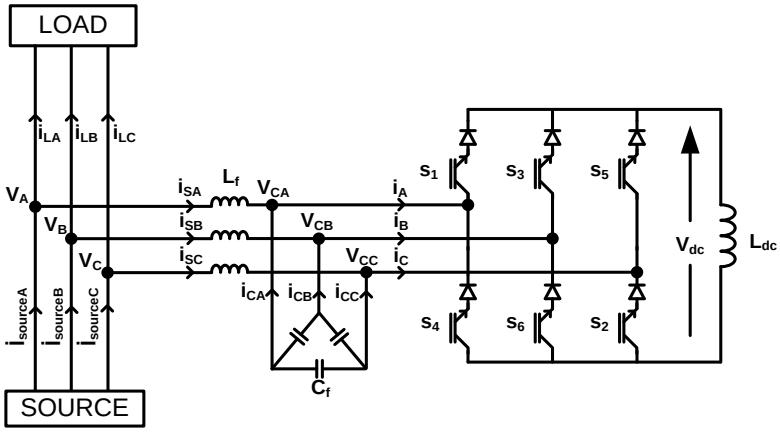

Figure 2.8 Three Phase System with STATCOM

Where; i_{LA}, i_{LB}, i_{LC}: three phase load current, $i_{sourceA}$, $i_{sourceB}$, $i_{sourceC}$: three phase source current, i_{SA}, i_{SB}, i_{SC}:three phase filtered converter current, i_{CA}, i_{CB}, i_{CC}: three phase capacitor current, i_A, i_B, i_C: three phase converter current, V_{CA}, V_{CB}, V_{CC}: three phase capacitor voltage, V_A, V_B, V_C: three phase voltage at common point of connection

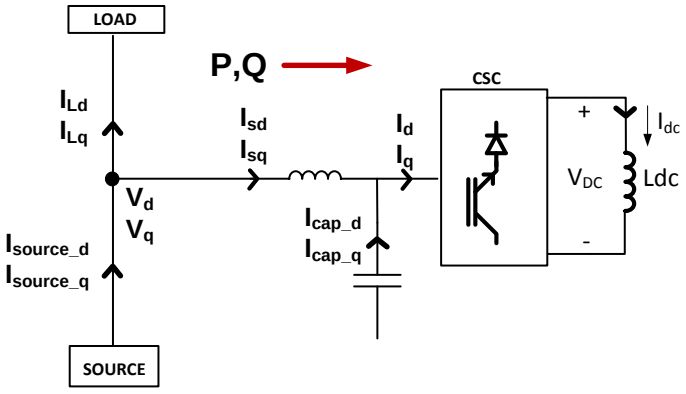

Figure 2.9 Single Line Diagram of System in “dq” frame

Where; I_{Ld}, I_{Lq} : d and q component of load current, I_{source_d}, I_{source_q}: d and q component of source current, I_{sd}, I_{sq}: d and q component of filtered converter current, I_{cap_d}, I_{cap_q}: d and q component of capacitor current, I_d, I_q: d and q component of converter current, Vd, Vq: d and q component of voltage at common point of connection

From single line diagram, active power (P) and reactive power of STATCOM are equal to (2.18) and (2.19), respectively [2, 3, 58, 59].

$$P = \frac{3}{2}(V_d.I_{sd} + V_q.I_{sq}) \tag{2.18}$$

$$Q = \frac{3}{2}(V_d.I_{sq} - V_q.I_{sd}) \tag{2.19}$$

Assuming three phase balanced AC supply having harmonic-free line voltages, then the term V_q in (2.18) and (2.19) becomes zero [2, 3, 59].The equations (2.18) and (2.19) reduces to (2.20) and (2.21), respectively.

$$P = \frac{3}{2}V_d.I_{sd} \tag{2.20}$$

$$Q = \frac{3}{2}V_d.I_{sq} \tag{2.21}$$

From (2.20) and (2.21), it can be concluded that active and reactive power drawn from source by STATCOM is controlled by the terms I_{sd} and I_{sq} respectively.

2.3.1 Reactive Power Control

Reactive power control block is illustrated in Figure 2.10. The load variables i_{LA}, i_{LB} and i_{LC} (A, B and C phase load currents) are measured and transformed into synchronous rotating "dq" frame by applying Clarke and Park transformations, respectively. The q-component of load current I_{Lq} is taken as the reference value that STATCOM should generate for reactive power compensation of load. Three phase filtered converter currents, i_{SA}, i_{SB} and i_{SC}, are transformed into "dq" stationary frame. The q-component of filtered converter current I_{Sq} is the generated reactive power current of STATCOM. I_{Sq} is subtracted from I_{Lq} in order to obtain

the error in reactive power control. By using the error, PI controller calculates the q-component of reference current vector, I_{q_PI} in "dq" frame.

The d-component of the reference current vector, I_{d_PI} is obtained from adaptive control of DC link current, as will be described in the following section. Then, the reference current vectors, I_{q_PI} and I_{d_PI} in synchronous rotating frame are transformed into the stationary frame as I_{α_ref} and I_{β_ref} in order to be used in space vector pulse width modulation.

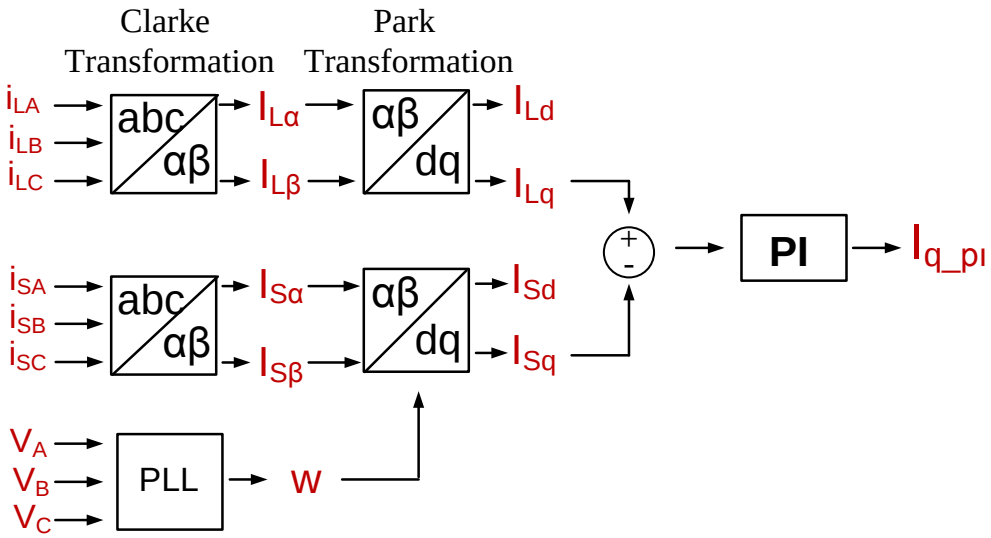

Figure 2.10 Reactive Power Control Block

2.3.2 DC link Current Control

The magnitude of the reference vector, I_{ref} should be small or equal to the DC link current value as stated in (2.14) and (2.15). Therefore, the magnitude of DC link current should always be controlled in order to be greater than the peak value of the line current.

DC link current is stored as magnetic energy at DC link reactor. However, the magnetic energy stored at DC link reactor is discharged if active power dissipated on internal resistance of DC link reactor and semiconductors is not drawn from the supply. Therefore, active power is delivered to STATCOM to keep DC link current at a certain value. As seen in (2.20), active power delivered to STATCOM is controlled by the d-component of reference vector in "dq" synchronous rotating reference frame. In order to keep DC link current at a defined value, the control system shown in Figure 2.11 can be constructed.

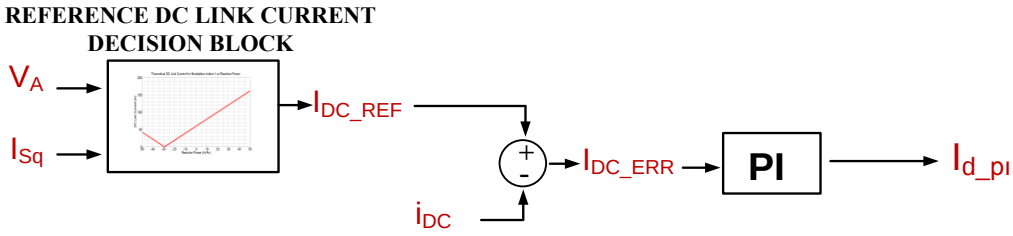

Figure 2.11 DC Link Current Control Block

The meaning of adaptive control of DC link current is to determine the reference DC link current according to the reactive power generated by STATCOM. While determining reference DC link current, the main aim is to keep modulation index at its maximum permissible value. The single line representation of CSC based STATCOM shown in Figure 2.12 is used to determine reference DC link current.

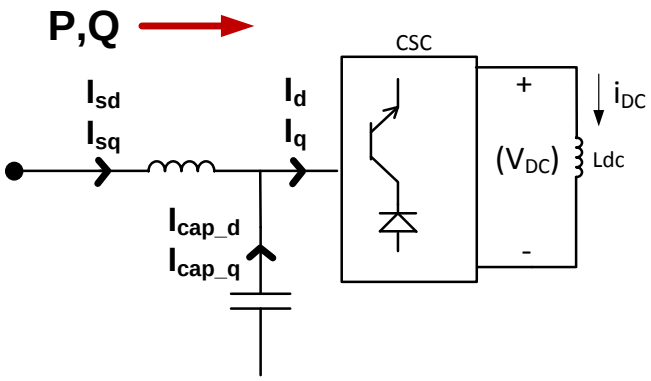

Figure 2.12 Single Line Representation of CSC based STATCOM

The reference vector in "dq" reference frame, I_{ref} is composed of I_d and I_q, which control the active power (i.e., DC link current) and reactive power transfer of STATCOM as given in (2.20) and (2.21), respectively. The active power transfer of STATCOM is due to the losses on power semiconductors and DC link reactor. The losses of STATCOM are smaller than its reactive power [60]. Therefore, I_{ref} can be assumed to be nearly equal to I_q.

As defined in (2.15), keeping M equal to 1 results in (2.22).

$$i_{dc} = I_q \tag{2.22}$$

By this way, i_{dc} can be made minimum for the required I_q (i.e., the reactive power generated by CSC).

In practice, the line currents of STATCOM are measured by the control system via current transducers. Then, the term I_{Sq} is calculated by applying Clarke and Park transformations. The relation between I_{Sq} and $I_q$is given in (2.23).

$$I_q = I_{Sq} + I_{cap\_q} \tag{2.23}$$

Reactive power generated by converter side of STATCOM and capacitor of low pass filter forms total reactive power generated by CSC based STATCOM.

I_{cap_q} is the q-component of capacitor currents and always positive in the direction shown in Figure 2.12. If reactive power generated by converter side of STATCOM is zero (I_q=0), then I_{sq} is equal to negative of I_{cap_q} as defined in (2.24).

$$I_{Sq} = -I_{cap\_q} \tag{2.24}$$

For this condition, reactive power generated by STATCOM is capacitive according to (2.21).

I_{cap_q} can be obtained by monitoring three phase capacitor current and applying Clarke and Park transformations, respectively. This requires additional current transducers for capacitor currents. Alternatively, the term I_{cap_q} can be calculated as given in (2.25).

$$I_{cap\_q} = 3.\ \overline{2}.2.\pi.f.V_A.C_f \tag{2.25}$$

Where, C_f denotes the capacitance per phase-delta and V_A is the voltage across capacitor.

The voltage across capacitor changes due to the filter inductance, L_f, as I_{Sq} (the reactive power of STATCOM) changes. It can be calculated according to (2.26).

$$V_A = V \pm I_{Sq}.2.pi.f.L_f \tag{2.26}$$

Where, V represents supply voltage.

By choosing L_f as small as possible and assuming a stiff supply, V_A can be taken as constant and equal to V. Then, I_{cap_q} in (2.25) only depends on the capacitance, C_f. Since C_f is fixed and known for a STATCOM system, I_{cap_q} can be calculated from (2.25) and taken as constant for all operating conditions.

Finally, the flowchart for determining the reference DC link current is designed and given in Figure 2.13. This flowchart is implemented into the decision block in Figure 2.11. Decision block measures I_{Sq}, executes this flowchart and gives output

of i_{dc_ref}. As an example, if I_{cap_q} is taken as 0.25pu, the variation of the reference DC link current with respect to the reactive power of STATCOM (i.e., I_{Sq}) can be obtained as given in Figure 2.14.

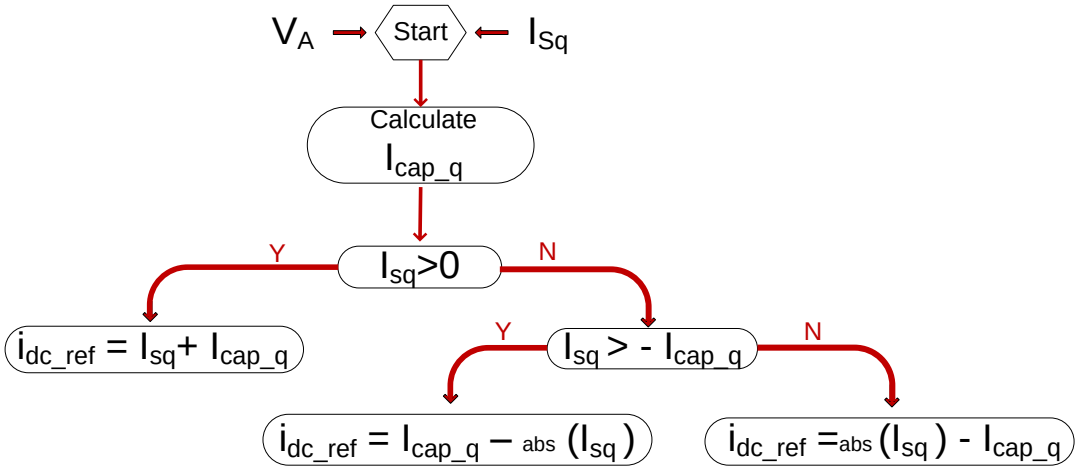

Figure 2.13 Flowchart of Decision Block in Adaptive Control of DC ink Current

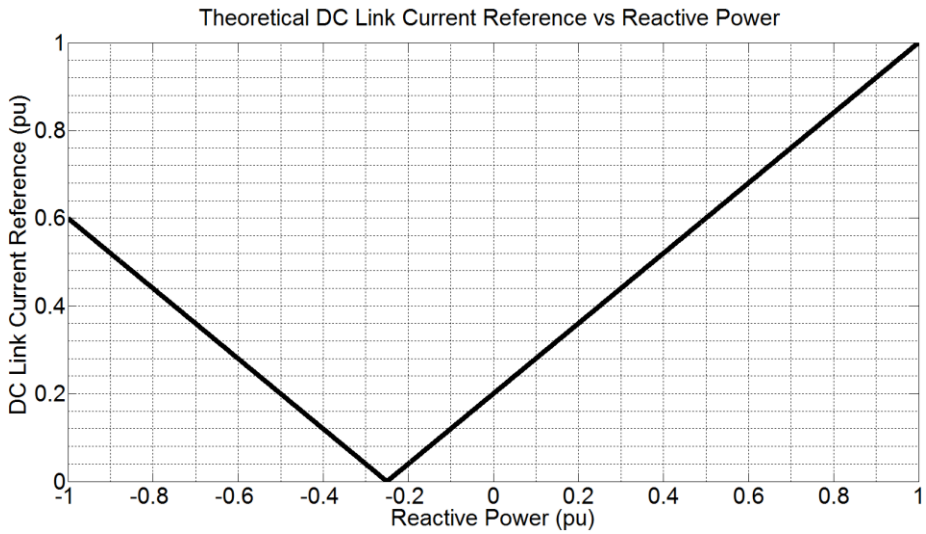

Figure 2.14 The Variation of DC Link Reference Current w.r.t Reactive Power of STATCOM

2.3.3 Active Damping Method

At AC side of the CSC based STATCOM, there is a low pass filter to suppress harmonic components of converter line currents (i.e. i_A, i_B, i_C in Figure 2.8) at modulation frequency and inject only their fundamental component at supply frequency. As seen from Figure 2.8, low pass filter is a three phase circuit and composed of inductors (i.e., per phase inductance is L_f) and capacitors (i.e., per phase capacitance in delta connection is C_f). The single line diagram of the low pass filter is given in Figure 2.15, where CSC is represented as current source and supply is a short circuit for harmonics other than supply frequency. Typical frequency response of the low pass filter for the filtered line current i_{SA} to converter line current i_A in magnitude is given in Figure 2.16. In the absence of a resistor (i.e., damping or power loss) in the circuit there is a significant amplification (is also referred as resonance phenomenon) at the resonance frequency (is also referred as corner frequency). To observe current amplification at resonance frequency, test circuitry is constructed in ORCAD/PSPICE simulation tool as shown in Figure 2.15. The AC sweep analysis of the circuit is given in Figure 2.16.

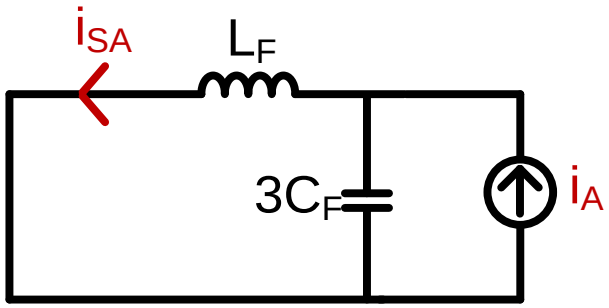

Figure 2.15 Single Line Diagram of Low Pass Filter

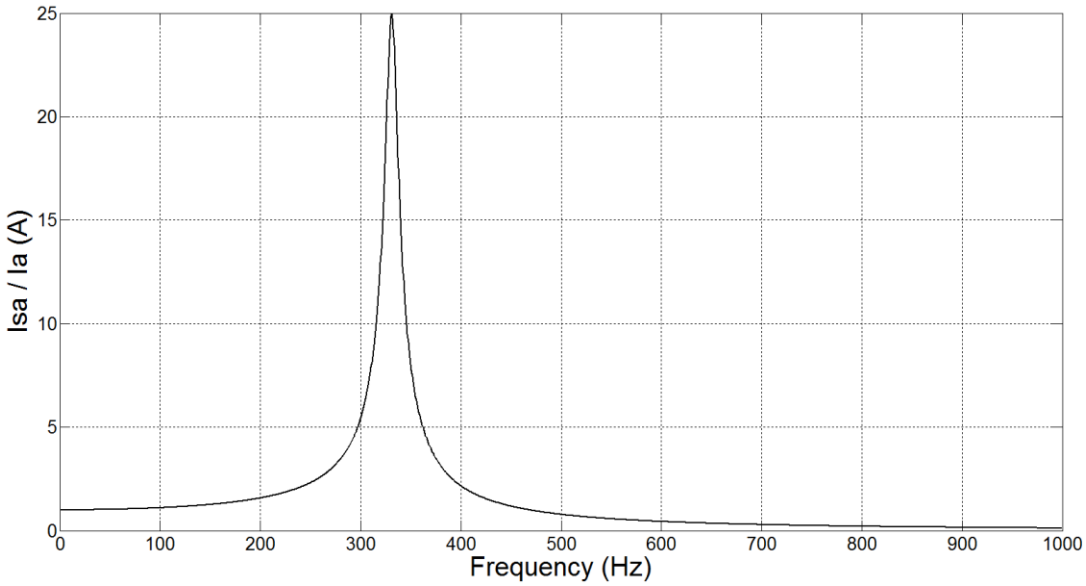

Figure 2.16 Typical Frequency Response of an Undamped Low Pass Filter (L_f=385uH, C_f=200uF)

The current amplification distorts the current injected into the system. To avoid the current amplifications at resonance frequency of the low pass filter, damping resistor, R_d can be added as shown in Figure 2.17. As the damping increases (i.e., R_d decreases), the amplification at the resonance frequency is significantly avoided. This is illustrated in Figure 2.18 by using sample data.

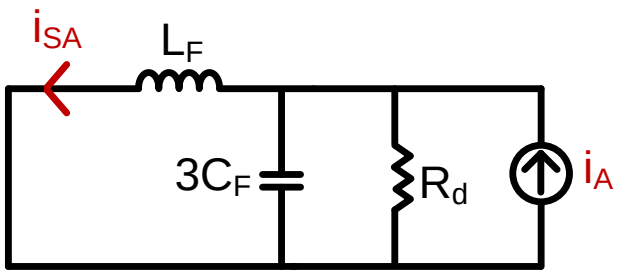

Figure 2.17 Single Line Diagram of a Low Pass Filter with a Damping Resistor R_d

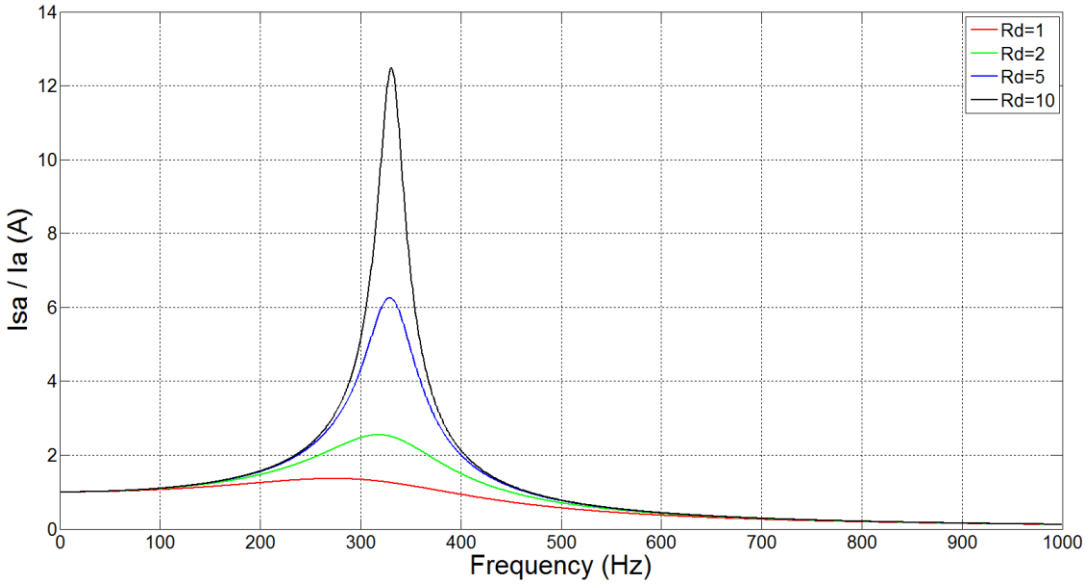

Figure 2.18 Frequency Response of the LC Filter with Various Damping Resistor Values

Passive damping and active damping methods are used to damp oscillations around corner frequency. Passive damping method requires adding a resistor into filter circuit resulting in increasing power loss of the system [2, 3, 61]. Active damping method proposes a technique using virtual resistor in filter circuit and without additional power loss [2, 38, 39, 40, 62, 63]. Active damping method can be applied by using on-line modulation technique in current source converter circuit topology.

By taking the derivative of the filtered current and multiplying by filter reactor, voltage across the filter reactor can be calculated as in (2.27).

$$V_{cf} = V_{lf} = L_f . \frac{di_{Lf}}{dt} \tag{2.27}$$

By dividing the calculated voltage to the virtual resistanceR_d, the damping current can be found as in (2.28).

$$i_{Rd} = \frac{V_{cf}}{R_d} = \frac{1}{R_d}.L_f.\frac{di_{Lf}}{dt} \tag{2.28}$$

Since the reference current vector for space vector PWM is in "αβ" stationary frame and the virtual damping current is calculated for single phase equivalent circuit of low pass filter as shown in Figure 2.19, the calculations for active damping is carried in "αβ" reference frame.

Then, the calculated damping currents I_{α_damp} and I_{β_damp} are respectively added to the current vectors, I_{alfa_PI} and I_{beta_PI}, which are shown in Figure 2.21.

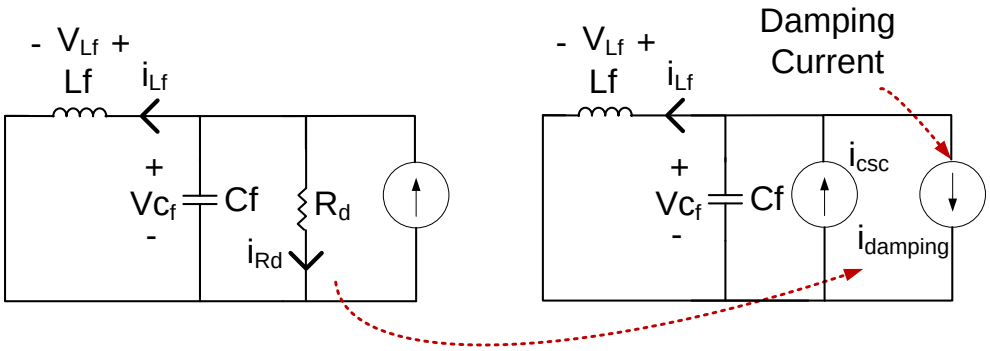

Figure 2.19 The Damping Current Calculation

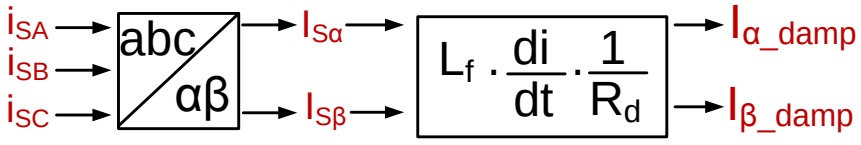

Figure 2.20 Active Damping Current Calculation Block

2.4 SUMMARY

In this chapter, operating principles of CSC based STATCOM is given. First, system configuration is presented and then space vector modulation technique is explained by stating the advantages of using this modulation technique over other on-line and off-line modulation techniques. Then, the control of CSC based STATCOM in synchronous rotating frame is explained. It is observed that the active and reactive power drawn by STATCOM can be controlled by controlling I_{Sd} and I_{Sq} terms, respectively. There are three control blocks in control of CSC based STATCOM. Reactive power control block monitors the system variables and generates I_{q_pi} term of general reference vector. Active damping current calculation block generates a reference vector for damping the current oscillations around resonance frequency. Adaptive DC link current control block determines new DC link current for the next switching period and generates I_{d_pi} term of reference vector. The overall control block is given Figure 2.21.

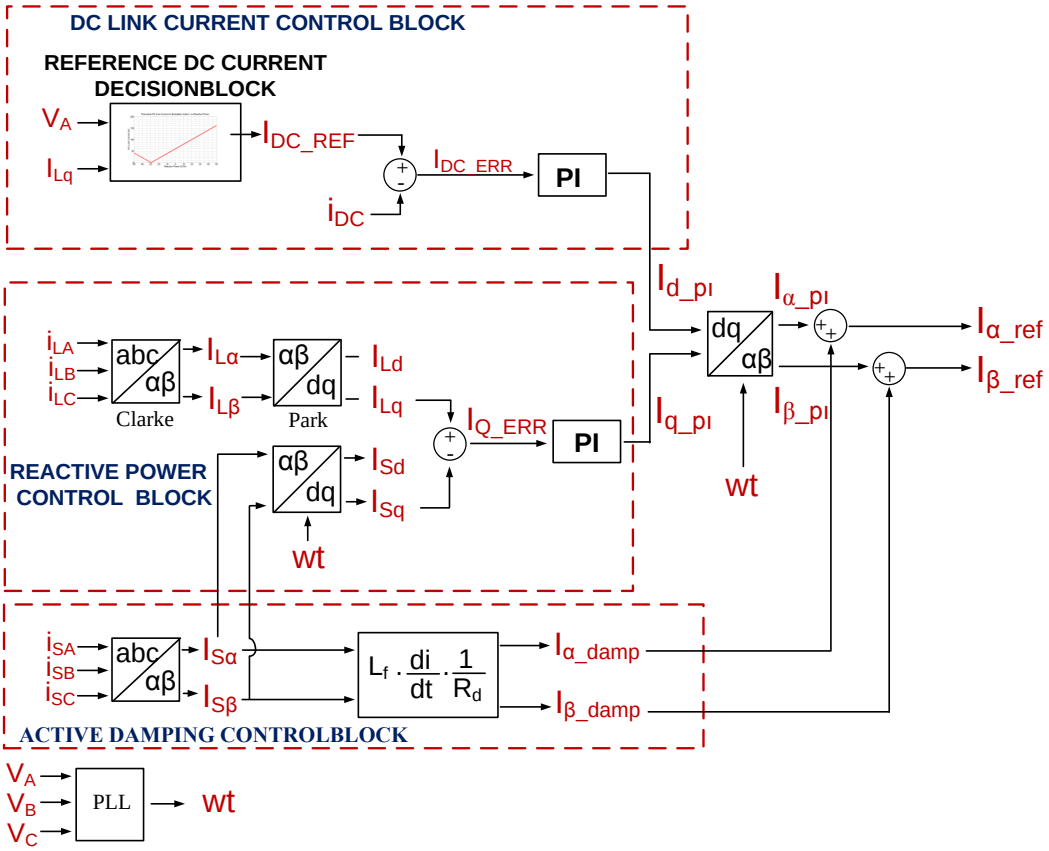

Figure 2.21 Control Block of STATCOM in Synchronous Rotating “dq” Frame

CHAPTER 3

SYSTEM DESIGN

In Chapter 2, the operating principles of CSC converter based STATCOM and control techniques such as active damping method, control of active and reactive power have been covered. In this chapter, system design parameters of CSC based STATCOM are going to be selected in view of methods explained in Chapter 2.

The designed CSC based STATCOM is going to satisfy the following requirements:

- Fast transient response to change in reactive power demand of load
- Injects nearly sinusoidal currents at supply frequency meeting the limits in IEEE Std. 512-1992.
- Minimum power loss
- Adaptive control of DC link current

3.1 DESIGN OF LOW PASS FILTER

Low pass filter at AC side of the converter is used in order to suppress high harmonic components of the line currents of STATCOM at modulation frequency. Low pass filter is composed of reactor and capacitor. In addition to reactor and capacitor, damping resistor is sometimes used for damping current amplifications around resonance frequency [3]. In this study, active damping method is applied and this damping resistor is not physically used. Low pass filter should be designed in view of following objectives [60];

1-) Filtering Performance: Low pass filter consists of capacitor and reactor so that this filter is second order low pass filter. The corner frequency of the low pass filter can be expressed as (3.1).

$$f_C = \frac{1}{2.\pi.\ \sqrt{L_f.3.C_f}} \tag{3.1}$$

Where, L_f (per phase inductance) is filter reactor and C_f (per phase capacitance in delta connection) is filter capacitor. In order to achieve a good filtering performance, the corner frequency of the filter f_C should be selected between supply frequency and most significant harmonic content in the converter currents [2]. It is recommended that f_C should be chosen as 20% of the frequency at which most significant harmonic component of line currents of CSC. Moreover, f_C should not coincide with one of harmonics which are characteristics to six-pulse line commutated converters (i.e., harmonics at 5^{th}, 7^{th}, 11^{th}, 13^{th} order of supply frequency) [60].

2-) Size of Filter Capacitor: In order to optimize the power losses, the operation range of CSC for reactive power generation should be equal both in capacitive and inductive operating condition (i.e., Q_{CSC_max} in capacitive mode of CSC is equal to Q_{CSC_max} in inductive mode of CSC). This can only be achieved by adjusting Q_{CAP} (i.e., C_f) according to reactive power demand of load. The reactive power generated by CSC based STATCOM is formed by capacitor and CSC side as given in (3.2).

$$Q_{STATCOM} = Q_{CAP} + Q_{CSC} \tag{3.2}$$

In practice, the voltage drop across the filter reactor, L_f is small and the inductive reactive power due to the filter reactor is relatively small as compared to the capacitive reactive power due to filter capacitors (i.e., capacitance C_f per phase

delta). Then, the size of the filter capacitor (i.e., the capacitance C_f per phase delta) determines the reactive power imposed by the low pass filter according to (3.3).

$$Q = 3.V^2.\ 2.\pi.f_{supply}\ .C_f\ \ (VAr) \tag{3.3}$$

3-) Voltage Regulation: Voltage regulation is defined as change in CSC input voltage from full capacitive to full inductive reactive power generation [60]. The voltage change at input of CSC, which is also the voltage across the capacitors, is given in (2.26). Inductance of filter reactor, L_f and total reactive power generated Q affects the voltage change at input of CSC. L_f should be chosen as low as possible in order to decrease the voltage regulation.

4-) Resonance Risk: In order to eliminate resonance risk, the corner frequencies of the low pass filter should not coincide with the harmonic frequencies generated by CSC and voltage harmonics at common point of connection [60]. It can be avoided either by adding damping resistor (i.e., passive damping) or active damping. The level of resonance can be reduced to a certain extent by adding damping resistor.

In view of these objectives, filter capacitance and inductance have been chosen as 200uF and 300uH, respectively. Due to its unavailability, filter reactor having an inductance of 385uH has been used.

With the selected parameters, the corner frequency of low pass filter has become 330Hz. This corner frequency is less than the frequency of the 7^{th} harmonic so hat sufficient suppression of higher order line current harmonics is provided. Further attenuation in 7^{th} and 5^{th} can be achieved by reducing the corner frequency of the input filter. However, lower corner frequency results in larger filter components. 30kVAr capacitive reactive power is generated for 200uF capacitance per phase delta at 0.4kV system voltage. Voltage regulation which is defined as the percentage of change in voltage from full capacitive to full inductive reactive power generation has been found as 7.5%.

The simulation has been done in ORCAD/Pspice simulation tool for determining virtual damping resistance, R_d in active damping method and it is found 1 ohm results in quite satisfactory damping performance around the corner as shown in Figure 2.18.

3.2 DESIGN OF DC LINK REACTOR

DC link reactor is used as energy storage element in the system and selection of DC link reactor value will be performed in view of transient response, system losses, maximum turn-off value for power semiconductor and total demand distortion of line currents (i_{SA}, i_{SB}, i_{SC}).

In this thesis, adaptive control of DC link current will be implemented and DC link current will be controlled according to the magnitude of the reactive power demand. Therefore, it is desired to obtain fast transient response in DC link current. The rate of change of i_{dc} is inversely proportional with L_{dc} as stated in (3.4) [43].

$$\Delta i_{dc} \; \alpha \; \frac{V}{f_{sw}.L_{dc}} \tag{3.4}$$

For fast transient response (i.e., minimum time for setting DC link current to new reference value) inductance of DC link should be selected as small as possible.

Higher peak to peak ripples on DC link current (i.e., Δi_{dc}) increases the total demand distortion (TDD) of line currents. For this reason, Δi_{dc} should be as small as possible [2, 3, 43]. The general approach is to make Δi_{DC} is 10% of its rated mean value, i_{dc} [25]. In order to obtain small peak to peak ripples, the inductance of DC link reactor and modulation frequency should be selected higher as expressed in (3.4). The effect of inductance of DC link reactor on TDD is investigated by PSCAD/EMTDC simulation tool. The variation of TDD for SVPWM at 6250Hz carrier frequency is given in Figure 3.1. As seen from Figure 3.1, TDD value of line current increases as the inductance of DC link reactor decreases. Since, TDD limit

for low voltage busses is less than 5%, the selected inductance should be higher than 1mH.

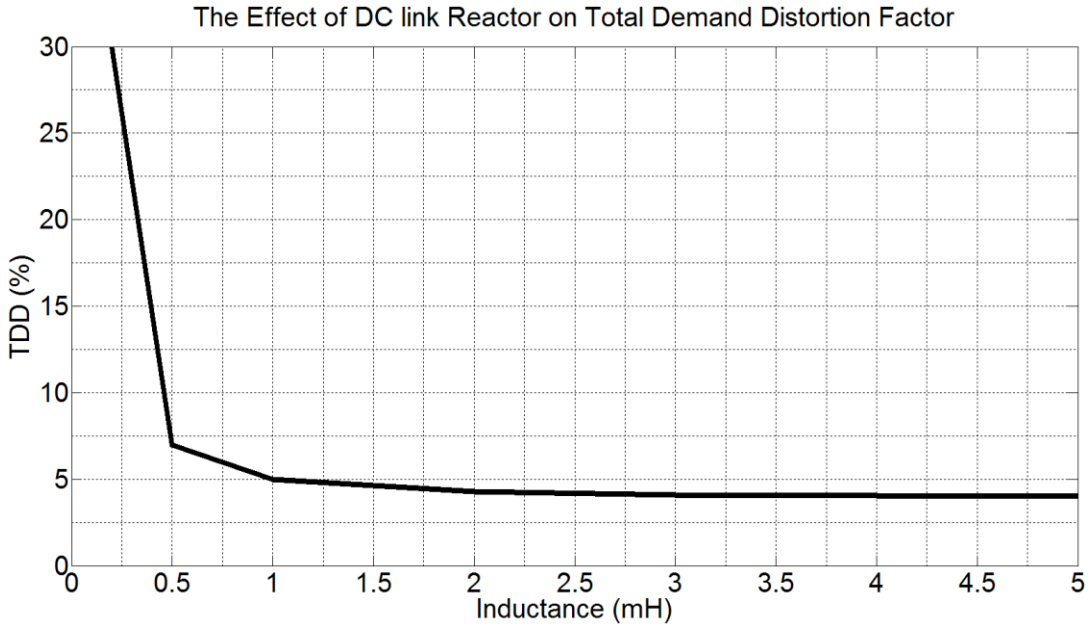

Figure 3.1 The Variation of Total Demand Distortion Factor with Inductance of DC Link Reactor at 50kVAr Capacitive Reactive Power Generation (PSCAD/EMTDC)

The ripples on DC link current determine the current level that will be turned off by power semiconductor. Maximum current on DC link reactor is given in (3.5) [2, 3, 43].

$$i_{MAX} = i_{DC} + \frac{\Delta i_{DC}}{2} \tag{3.5}$$

Maximum current on DC link reactor is dependent on Δi_{DC} and Δi_{DC} is dependent on L_{DC} as stated in (3.4). L_{DC} should be selected higher [2, 3, 43] to reduce peak to peak ripple of DC link current.

When power dissipation of DC link reactor is considered, it is directly proportional with magnitude of L_{DC}. The value of L_{DC} is determined by number of turns. Increasing the number of turns for higher L_{DC} will result in higher internal resistance r_{DC}, thus increasing power dissipation on DC link reactor [2, 3, 43].

In view of above considerations, in research work [2], the simulation has been done to choose optimum inductance of DC link reactor considering peak to peak ripple, switching frequency and inductance value. An inductance value of 2mH inductance value for DC link reactor is selected in [2] as an optimum solution for minimizing power loss, peak to peak ripple and TDD of line currents. Since the developed STATCOM systems in the scope of this thesis and research work [2] are similar, 2mH DC link inductance value is used in this thesis.

3.3 SELECTION OF POWER SEMICONDUCTOR

IGCTs, thyristors, GTOs and IGBTs are widely used semiconductors in power applications [2, 3, 43]. As mentioned earlier, the semiconductor used in CSC should have bidirectional voltage blocking and unidirectional current flow. This can be achieved by using symmetrical devices or connecting a diode in series with semiconductor switch.

The properties of power semiconductor used in the scope of this thesis are determined in view of frequency limits, voltage rating and current carrying capacity.

1-) Frequency Limits: In the scope of this thesis, 0.4kV CSC based STATCOM will be operated by using SVPWM technique. The modulation frequency of SVPWM determines the peak to peak ripple of DC link current. Increasing modulation frequency results in lower peak to peak ripples, but as a drawback, switching losses increases. In research work [2], the carrier frequency is determined to be 6250Hz as an optimum solution for 2mH DC link inductance. The developed

system in [2] is similar to the developed system in this study so that modulation frequency of 6250Hz is also employed in this thesis.

For the application of on-line PWM techniques with a switching frequency higher than 1 kHz, IGBT is the only choice among the candidates, such as GTO and IGCTs [2, 43]. In order to achieve a switch with bipolar voltage blocking capability, a diode in series with IGBT is used.

2-) Voltage rating: Designed CSC based STATCOM will be operated at $0.4kV_{l\text{-}l\ (rms)}$ system voltage. The voltage at the input of converter increases at maximum capacitive VAr generation due to the filter reactor L_f [2]. For 50kVAr capacitive reactive power generation and 0.4kV system voltage, maximum converter voltage is calculated in equation (3.6).

$$V_{peak} = \overline{2}.\ 400V + \frac{50000\ VAr}{400V}.2.\pi.50Hz.385uH\ = 587V \qquad (3.6)$$

For safety, the voltage rating of IGBT in CSC should be selected 50% higher than the calculated in (3.6). Therefore, the voltage rating of IGBT is calculated as 880V. An IGBT with a voltage rating of 880V or larger will satisfy the voltage rating requirement of the developed system.

3-) Current rating: The reactive power rating of designed STATCOM is ±50kVAr. The peak of line current for 0.4kV system voltage is 102A. According to the Figure 2.13, maximum DC link current can be 160A for 50kVAr inductive reactive power generation at 0.4kV system voltage. According to (3.5), peak value of DC link current is greater than 160A so that the current carrying capability of semiconductor should be higher than 160A. During load commutations, reverse recovery current of the series connected diode also increases the required current rating of IGBT beyond 160A. For safety, the current rating of IGBT is selected as 50% higher than 160A. Therefore, an IGBT with a current rating of 240A or larger will satisfy the current rating requirement.

Selection of Diode: IGBT is a fast switching component so that the selected diode should be compatible with IGBT i.e. it must be a fast recovery diode. Another consideration for diode is that it should have low reverse recovery current. Higher reverse recovery current of diode results in higher reverse recovery losses.

In order to minimize total cost of the system and parasitic inductance between IGBT and diode, module which has both IGBT and diode in the same package is investigated. According to the result of the research, DYNEX Corporation's 1700V, 400A rated DIM400DCM17-A000 type IGBT is found for the designed CSC application. Internal circuit configuration of selected IGBT module is given in Figure 3.2

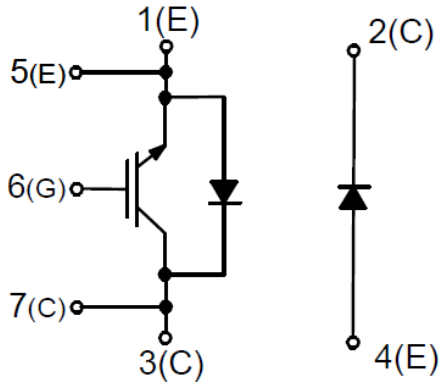

Figure 3.2 Internal Circuit Configuration of IGBT

Power Dissipation on IGBT and Diode:

Power loss of IGBT and diode is calculated at 50kVAr inductive reactive power generation via PSCAD/EMTDC simulation tool. At 0.4kV system voltage, constant 180A DC link current and 6250Hz modulation frequency, power dissipation on IGBT module is calculated according to the method explained in [3]. The power dissipation of the selected IGBT module is given in Table 3.1. The technical

specifications of IGBT and diode used while calculating power losses are given in Appendix A.

Table 3.1 Total Power Dissipation for 50kVAr Inductive Reactive Power Generation and 180A Constant DC Link Current Condition

Loss (Watt)	IGBT	Diode
Conduction Loss	1440	756
Turn ON Loss	180	-
Turn OFF Loss	192	-
Reverse Recovery Loss	-	260
Total	1812	1016

3.4 DESIGN OF POWER STAGE

3.4.1 Considerations on Heat Sink

Figure 3.3 shows IGBT module and heat sink connection for all six IGBT modules. Each IGBT module consists of IGBT and diode. Three IGBT modules are connected on one heat sink. Mounting part is used to connect IGBT and diode in series.

Steady state thermal model for each heat sink is shown in Figure 3.4. Austerlitz KS 300-14 type heat sink with EBMPAPST D2E160 type cooler fan, which has been available in TUBITAK Uzay facilities, is used to remove heat from IGBT and diode. In order to check the conformity of the heat sink and cooler fan, maximum operating values of virtual junction temperature (T_{vj}) of IGBT and diode are calculated. These values are found to be 88°C and 83 °C for IGBT and diode,

respectively. The calculated values are lower than maximum operating values of junction temperatures (150°C for IGBT and 125 °C for diode as expressed in Appendix B). The specifications of heat sink and cooler fan are given in Appendix C.

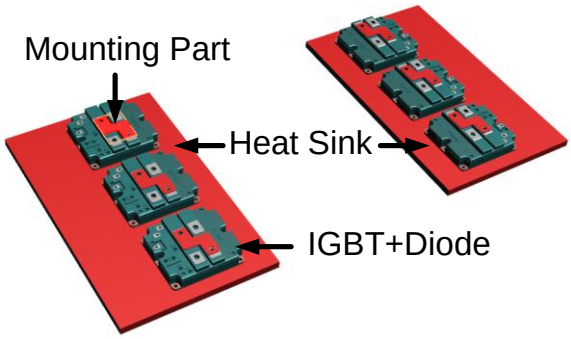

Figure 3.3 Mechanical Model of Heat Sink and IGBT module

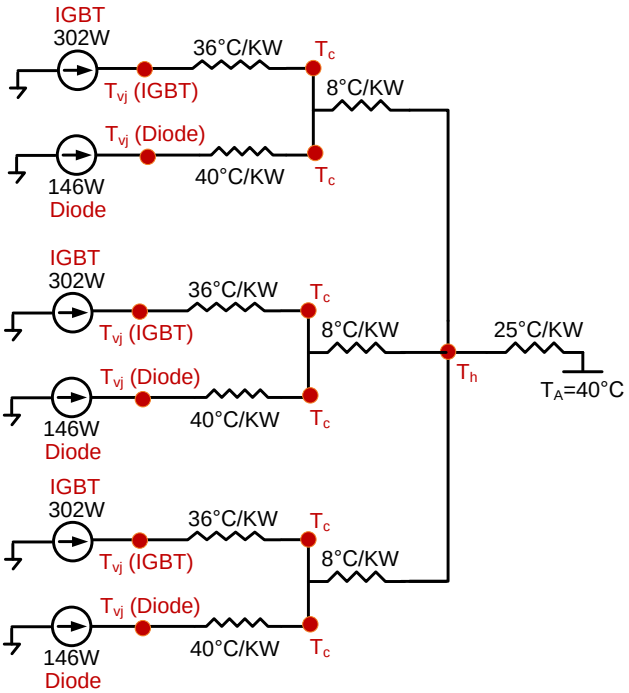

Figure 3.4 Steady State Thermal Model for Each Heat Sink

3.4.2 Design of Laminated Bus Bar

Parasitic inductances existing on commutation path causes overvoltage on IGBT. In order to avoid adverse effecst of parasitic inductances, connections between the power terminals of IGBTs have been implemented by using laminated busbars [2, 3].

A laminated bus bar system consists of planar conductors separated by insulating layers [64]. In this thesis, laminated bus bar has been implemented and as an insulation material, ISONOM NMN 0881 type insulation paper is used.

During the design of busbar, the following items are taken into consideration [2, 65]:

- Distance between IGBT and diode should be minimized,
- Capacitor of low pass filter should be selected as low inductance type,
- Length of commutation path should be as small as possible
- IGBTs should be positioned as close as possible to each other.

The mechanical model and picture of the busbar designed in view of above considerations are given Figure 3.5 and Figure 3.6, respectively.

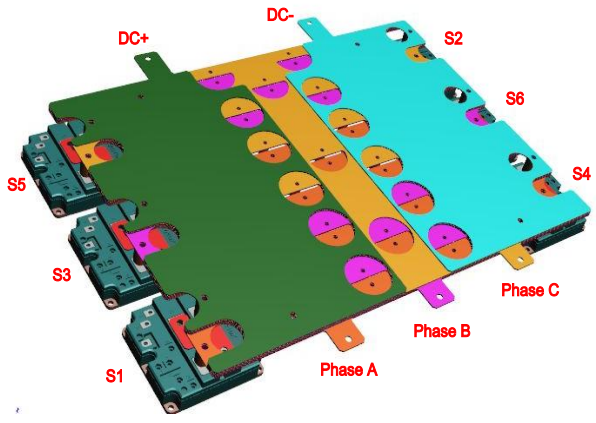

Figure 3.5 Mechanical Model of Designed Bus Bar

Figure 3.6 Bus bar and Capacitors of Low Pass Filter

In order to minimize the distance between IGBT and diode, the module having both IGBT and diode in the same package is chosen and they are connected with the mounting part as shown in Figure 3.3.

As can be seen in Figure 3.6, five capacitors each having 40uF value are connected in parallel between each phase for delta connection. Each capacitor has an inductance of 100nH. By paralleling five capacitors, the stray inductance of capacitors becomes 20nH.

In order to minimize commutation path, IGBT modules and capacitors of low pass filter are placed as close as possible to each other as shown in Figure 3.6.

The designed bus bar is verified by applying switching test to all of the six commutation paths given in Figure 3.7 [2, 3, 43]. Experimental set up for switching test is same as shown in research work [2].

500V DC voltage is applied line to line terminals and the current is limited to 150A by connecting 2 ohm resistance in series with DC link reactor.

The devices used in measurement are given in Table 3.2. IGBT is subjected to overvoltage during forced turn off, and diode is subjected to overvoltage during load turn off due to the parasitic inductances existing on commutation path [2, 3]. Effect of the parasitic inductance top and bottom side of CSC for each leg is shown

in Figure 3.8 to Figure 3.19. Calculated parasitic inductance values are given in Table 3.3.

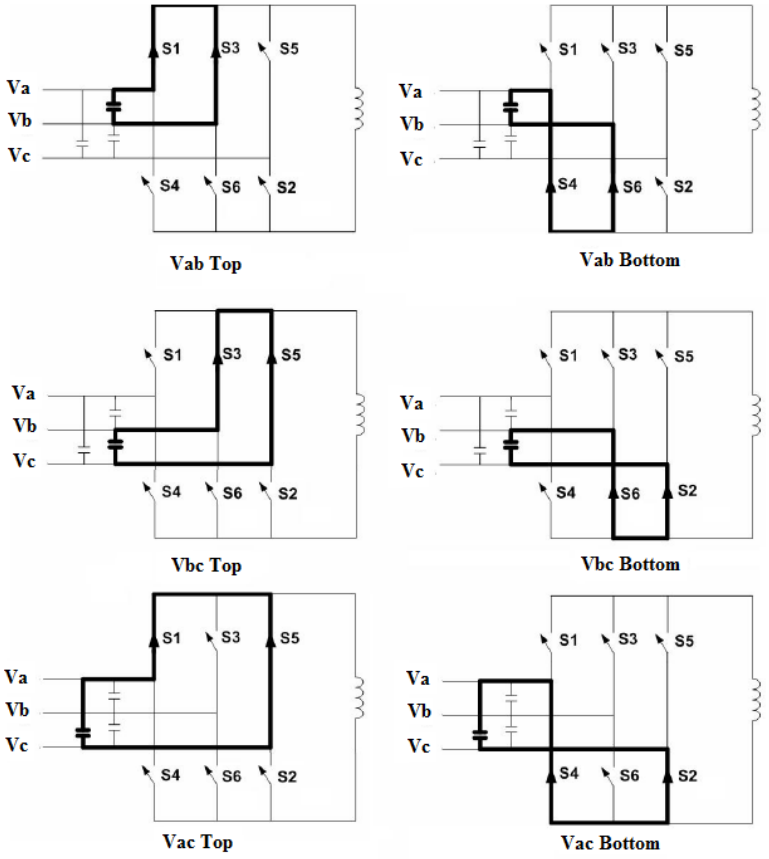

Figure 3.7 Commutation Paths

Table 3.2 Measurement Devices used in Switching Test

MEASUREMENT DEVICES	
Current Probe	Powertek, Ragowski Current Transducers CWT15B
Voltage Probe	Tektronix P5210 High Voltage Differential Probe
Oscilloscope	Tektronix TDS5054 Digital Phospor Oscilloscope

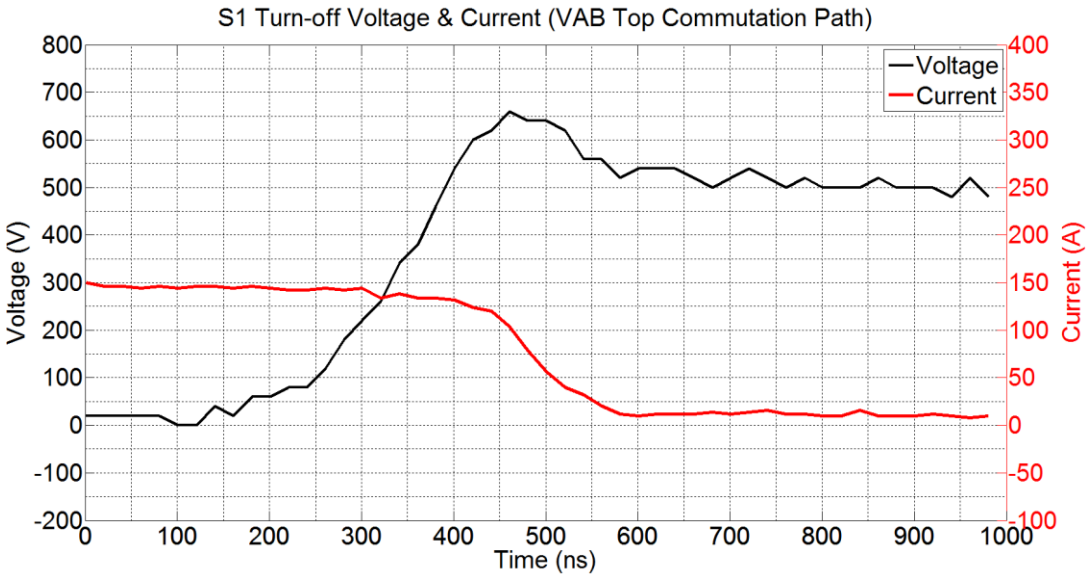

Figure 3.8 Forced Turn OFF of S1 (V_{AB} Top Commutation Path)

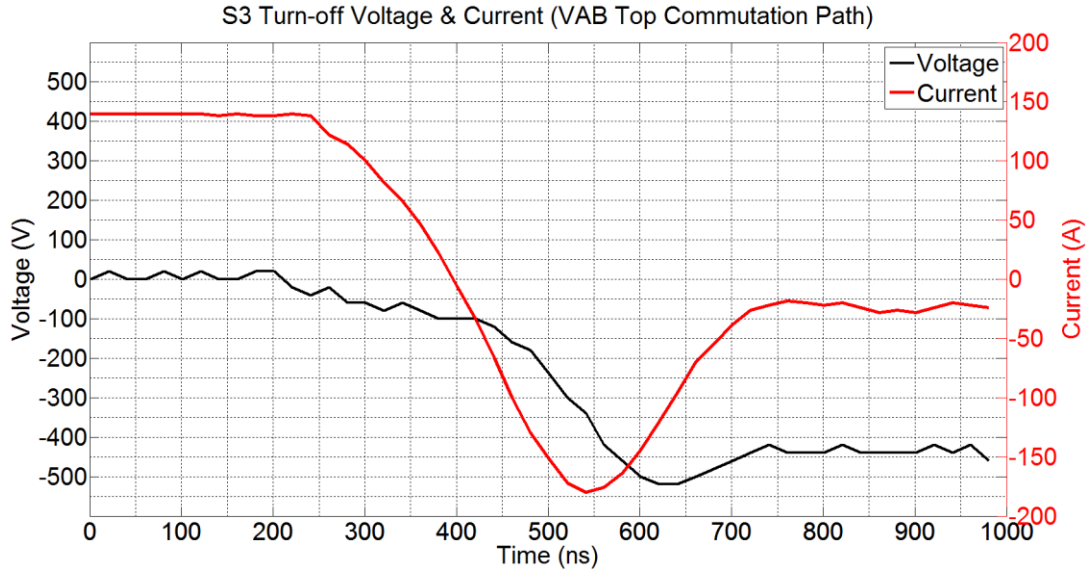

Figure 3.9 Load Turn OFF of S3 (V_{AB} Top Commutation Path)

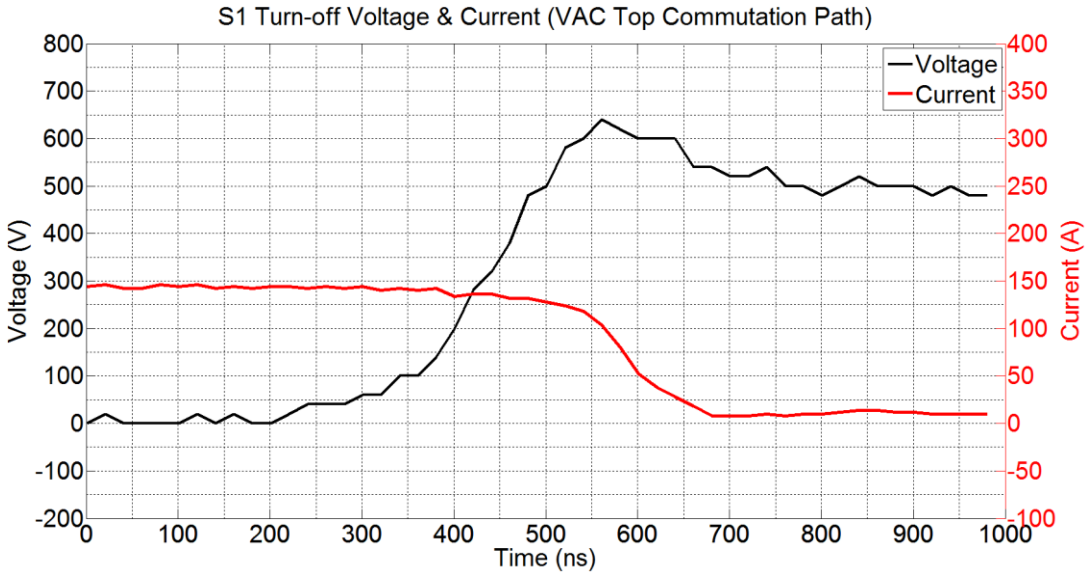

Figure 3.10 Forced Turn OFF of S1 (V_{AC} Top Commutation Path)

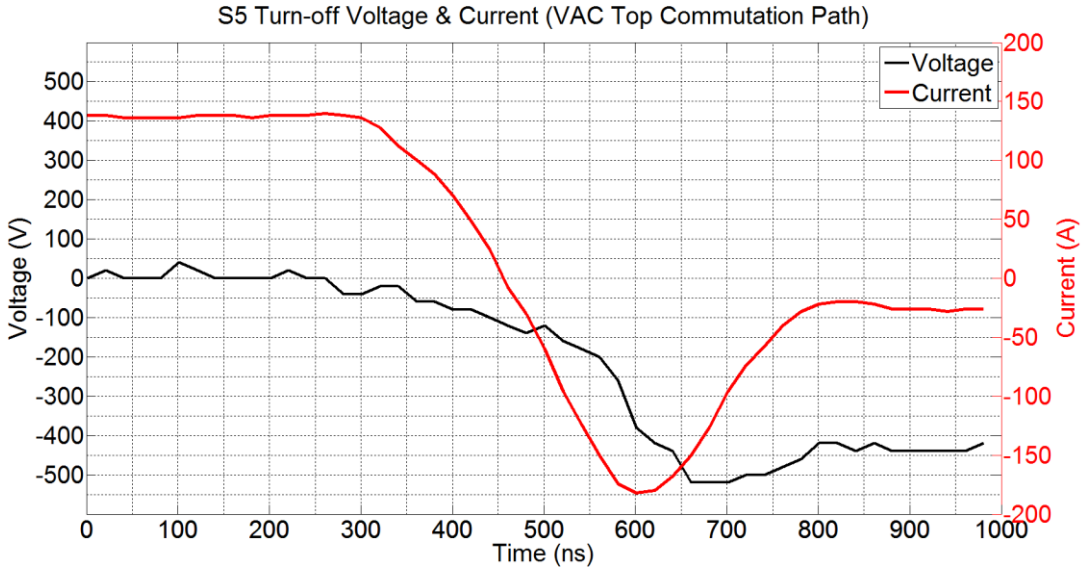

Figure 3.11 Load Turn OFF of S5 (V_{AC} Top Commutation Path)

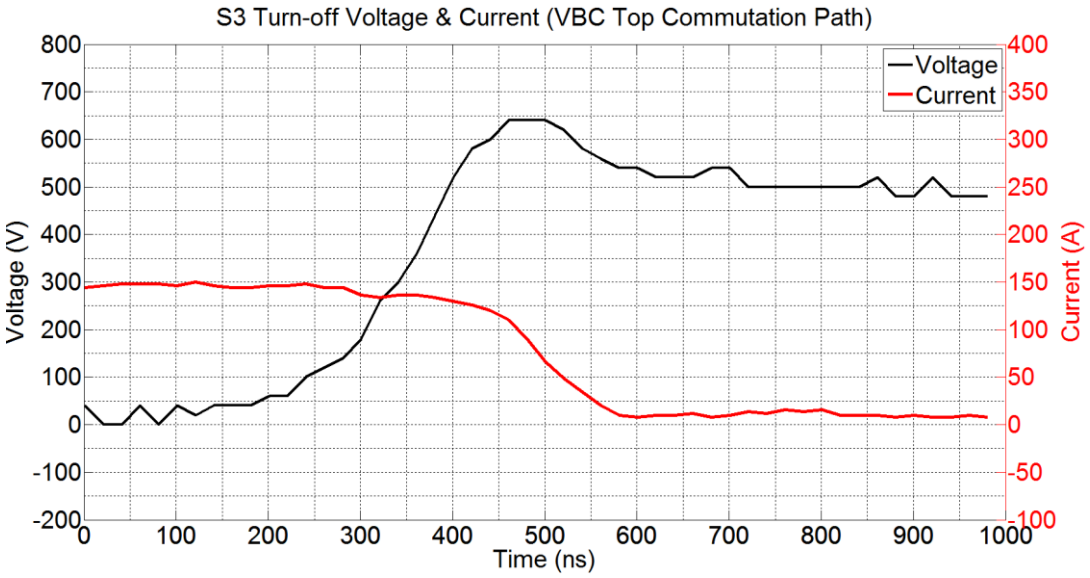

Figure 3.12 Forced Turn OFF of S3 (V_{BC} Top Commutation Path)

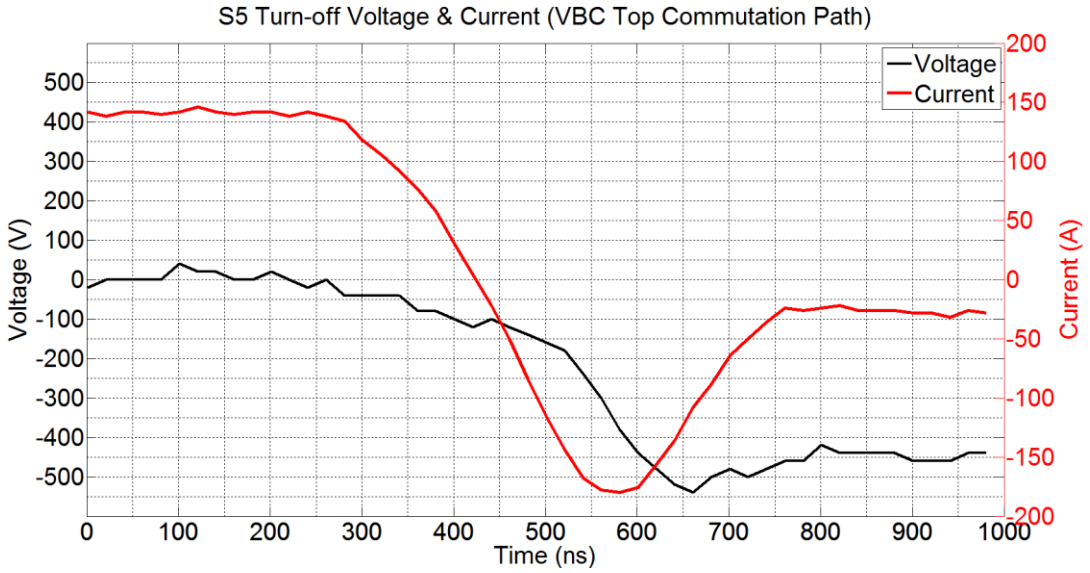

Figure 3.13 Load Turn OFF of S5 ((V_{BC} Top Commutation Path))

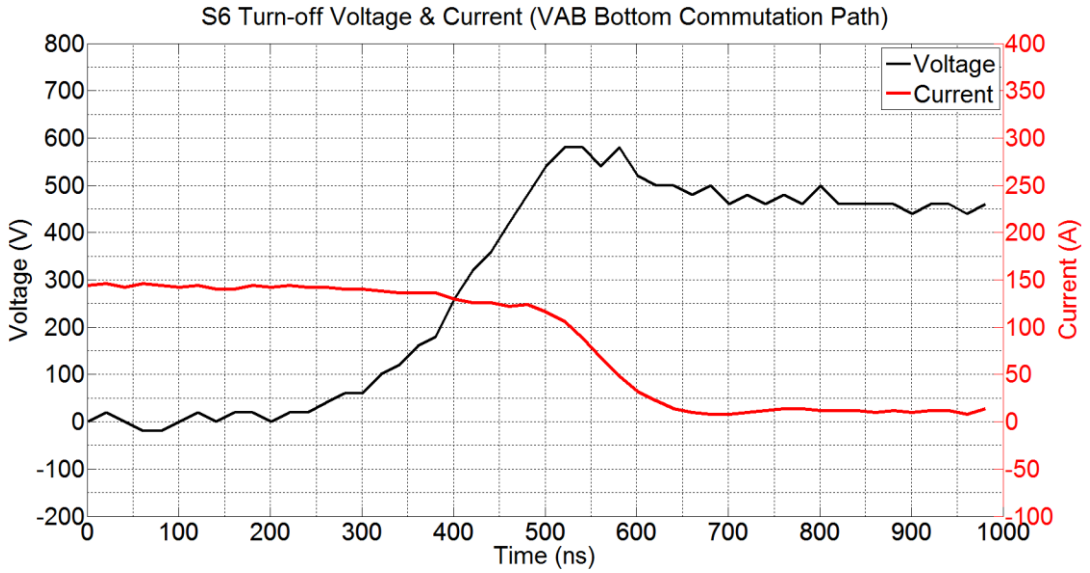

Figure 3.14 Forced Turn OFF of S6 (V_{AB} Bottom Commutation Path)

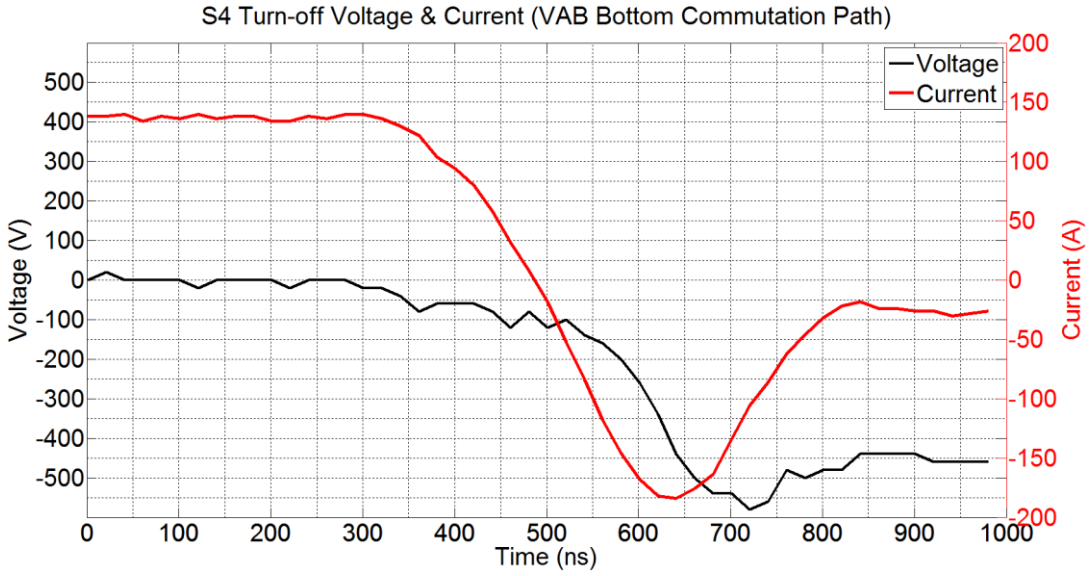

Figure 3.15 Load Turn OFF of S4 ((V_{AB} Bottom Commutation Path))

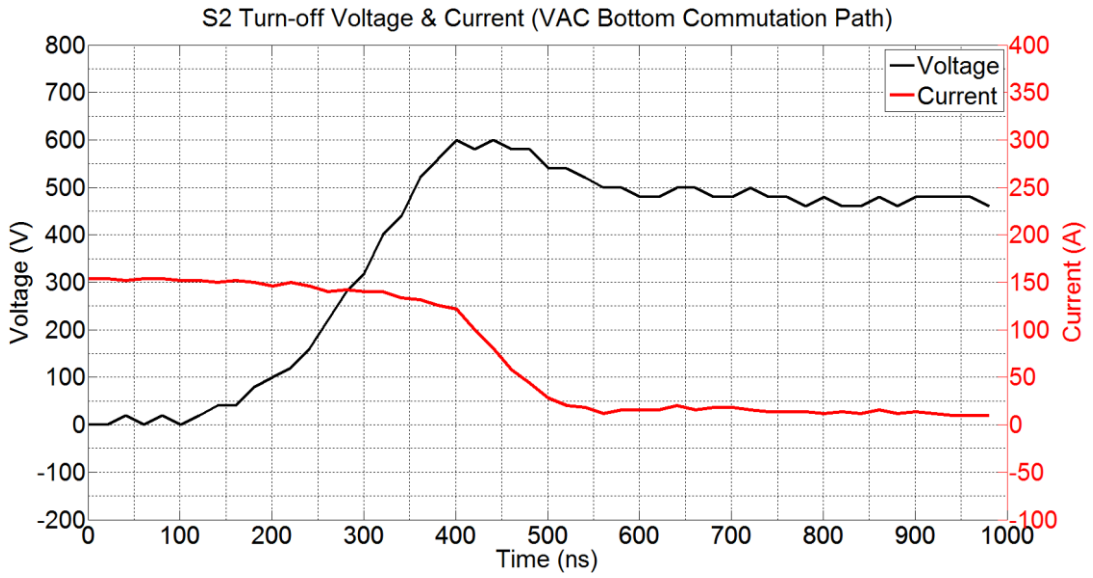

Figure 3.16 Forced Turn OFF of S2 (V_{AC} Bottom Commutation Path)

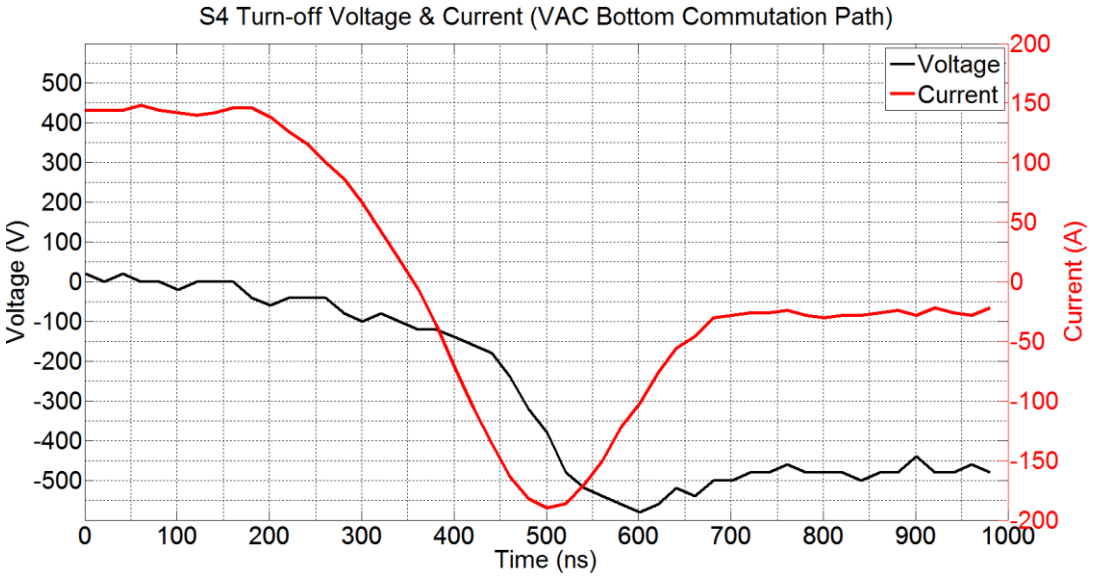

Figure 3.17 Load Turn OFF of S4 (V_{AC} Bottom Commutation Path)

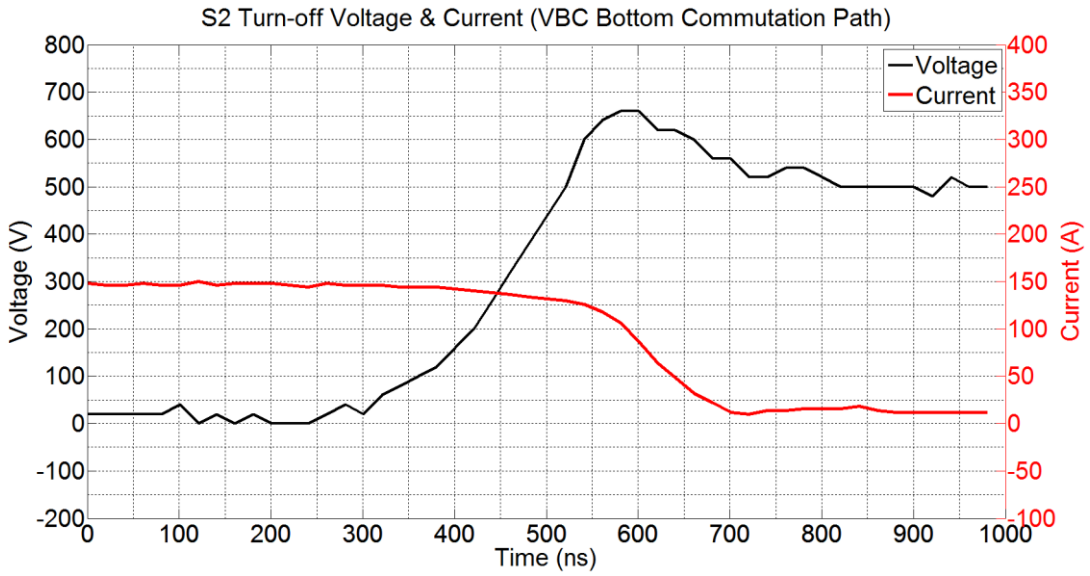

Figure 3.18 Forced Turn OFF of S2 (V_{BC} Bottom Commutation Path)

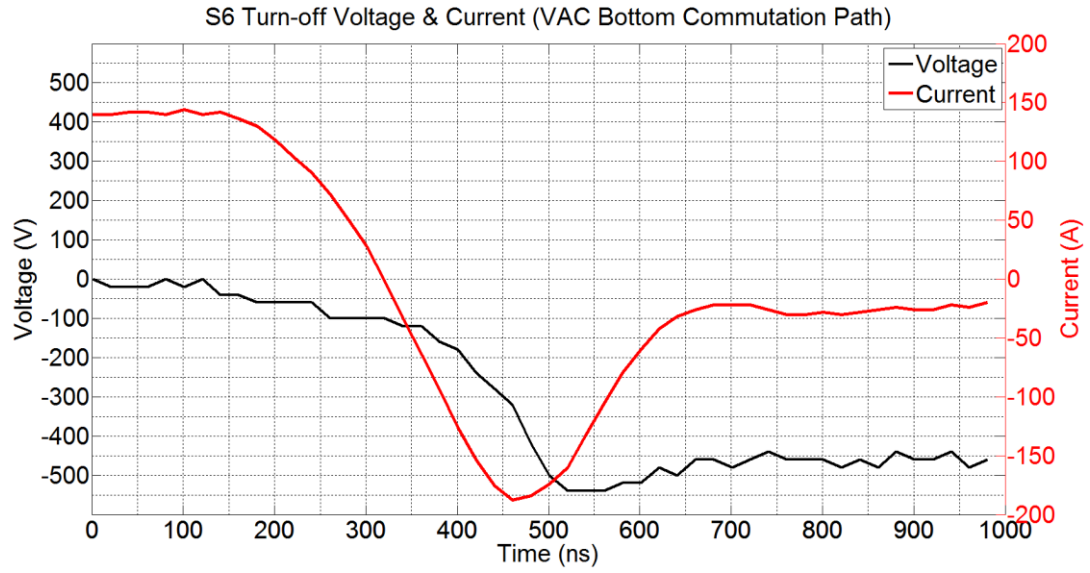

Figure 3.19 Load Turn OFF of S6 (V_{BC} Bottom Commutation Path)

Table 3.3 Measured Parasitic Inductances for the Commutation Paths

Commutation Path	Parasitic Inductance (nH)
TOP AB	138
TOP AC	120
TOP BC	135
BOTTOM AB	108
BOTTOM AC	112
BOTTOM BC	103

From the result of switching tests, the value of the voltage spike across IGBT is determined approximately 150V. This overvoltage value will increase in case of a larger switched current. Negative current seen in load turn off waveforms of IGBTs (in Figure 3.9, Figure 3.11, Figure 3.13, Figure 3.15, Figure 3.17 and Figure 3.19) is the reverse recovery current of fast recovery diode. After calculating the parasitic inductance values for all commutation paths, it is seen that parasitic inductance values are lower than 150nH as expressed in Table 3.3.

3.5 DESIGN OF OVERVOLTAGE PROTECTION CIRCUIT

With the development of semiconductor technology, the current rating of power semiconductors increases beyond 1000A and their switching times decrease to a few hundred nanoseconds [68]. Switching a high current in a short time may cause undesirable voltage transients on switch terminals due to the parasitic inductance of the power stage. Overvoltage protection circuit should used to protect IGBT from overvoltage transients across IGBT module terminals. In case of overvoltage condition, this circuit is activated and avoids the voltage increase beyond predefined

value. Crowbar circuit is commonly used in CSC applications for overvoltage protection in case of failure in continuous flow of DC link current [3]. It provides a closed path for DC link current so that energy stored in DC link reactor can discharge. However, this cannot detect any overvoltage transients across IGBT terminals since it only monitors the overvoltage across DC link. In literature, advanced active clamping method is applied to protect IGBT from overvoltage [66]. In this method, the collector voltage feedback of the IGBT is connected to the gate of the IGBT and input of the gate driver through over clamping components (i.e., transient voltage suppressors-TVS) as shown in Figure 3.20. If the voltage across the collector-emitter terminals exceeds the clamping voltage of TVSs, they start to conduct current. This current both charges gate capacitor of IGBT and input of the gate driver. The gate driver turns on IGBT immediately.

In this thesis, advanced active clamping circuit is modified. It is designed in order to:

- Detect overvoltage and limit the voltage across IGBT terminals,
- Send fault signal to digital signal controller (DSC). By this way, the DSC shuts down system safely by freewheel operation [3].

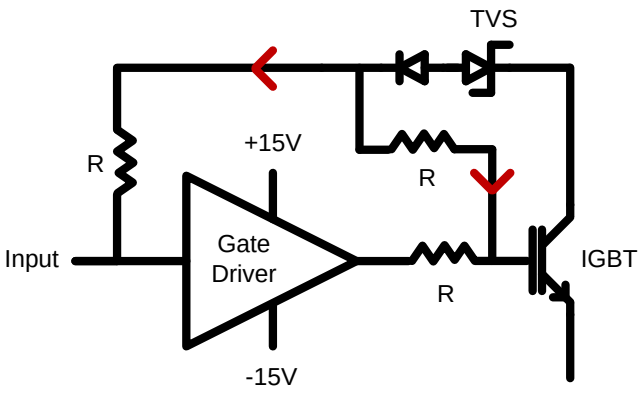

Figure 3.20 Advanced Active Clamping Circuitry

For isolation of gate voltage of IGBT from supply voltage, a gate driver (2SD315AI) is used to drive IGBT. The gate driver takes “ON” signal from DSC by fiber optic interface and adjusts the gate voltage of IGBT to 15VDC. In “OFF” condition, the gate driver adjusts the output voltage to -15VDC. The block diagram and picture of gate driver card is given in Figure 3.21 and Figure 3.22, respectively. The schematic of gate driver card is given in Appendix D.

The circuit of overvoltage detection circuit consists of breakover diode, fast recovery diode, fast opto coupler and fiber optic transmitter. If the voltage across the terminals of IGBT increases beyond 1.2kV, the breakover diode starts to conduct current. The circuit of overvoltage detection circuit is given in Figure 3.23. In order to verify the developed overvoltage protection circuit, test circuit shown in Figure 3.24 has been used.

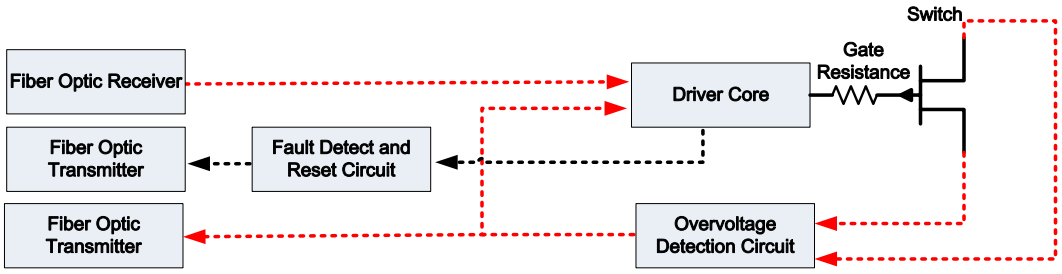

Figure 3.21 The Block Diagram of Gate Driver Card

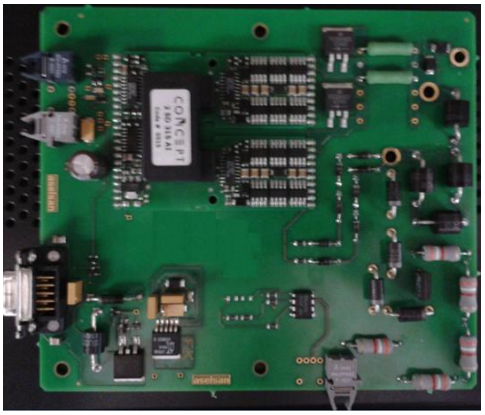

Figure 3.22 The picture of Gate Driver Card

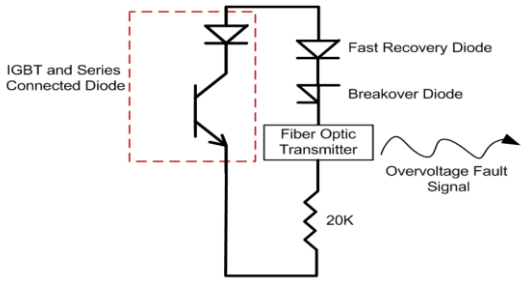

Figure 3.23 Overvoltage Detection Circuit

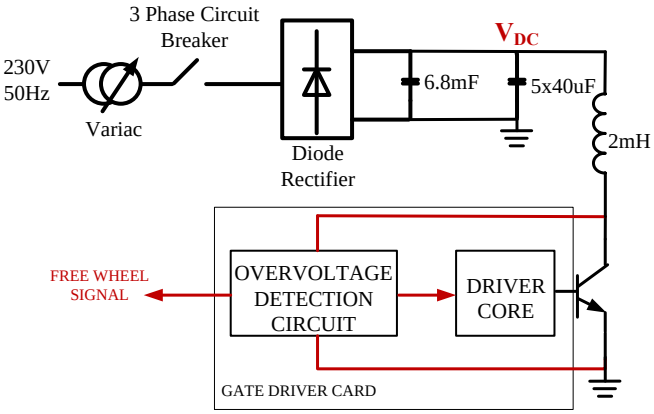

Figure 3.24 Block Diagram of Test Set up

After turning IGBT on, the current starts to conduct through the reactor. Then, IGBT is turned off. This forces the current through reactor to decay to zero within a turn-off time of IGBT and results in an overvoltage across the collector-emitter terminals of IGBT. The action of overvoltage protection circuit was observed. Test was repeated for 3 different values of V_{DC}, i.e., 150, 170 and 180V.

In Figure 3.25, the voltage across breakover diode is shown. The breakover diode is not broken down when capacitors shown in Figure 3.24 are charged to 150V. In this condition, overvoltage fault signal is not sent to the DSC based controller card. When capacitors are charged to 170V and 180V, breakover diode is broken down (the voltage across breakover diode decays to 0V) and overvoltage fault signal is sent to DSC based controller card. The freewheel circuit found in DSC based controller card takes the fault signal and generates freewheel signal for a duration of 2 sec.

In Figure 3.26, voltage waveforms across IGBT for three conditions are shown. In 150V case, the voltage across IGBT arises to 1100V and breakover diode is not broken down as seen from Figure 3.25. For V_{DC} charged to 170V and 180V cases, the voltage arises approximately to 1250V. The voltage across IGBT should be higher than 1250V for V_{DC} charged to 180V case. However, due to leakage current through TVSs, IGBT is partially turned on as shown in Figure 3.27, thus voltage across IGBT does not exceed 1250V.

Gate-source voltages of IGBT for three cases mentioned above are shown in Figure 3.27. Due to characteristics of gate driver, when switch is turned on, gate to source voltage is adjusted to 15VDC and when switch is turned off, gate to source voltage is adjusted to -15VDC. When V_{DC} is charged to 180V, the IGBT is turned off by DSC so that the gate to source voltage begins to decrease from 15VDC to -15VDC. During this operation, the voltage across IGBT terminals begins to increase. As seen from Figure 3.26, voltage across IGBT reaches to 1250VDC and current begins to leak through TVSs, thus charging gate capacitors. As illustrated in Figure 3.27, IGBT is partially turned on.

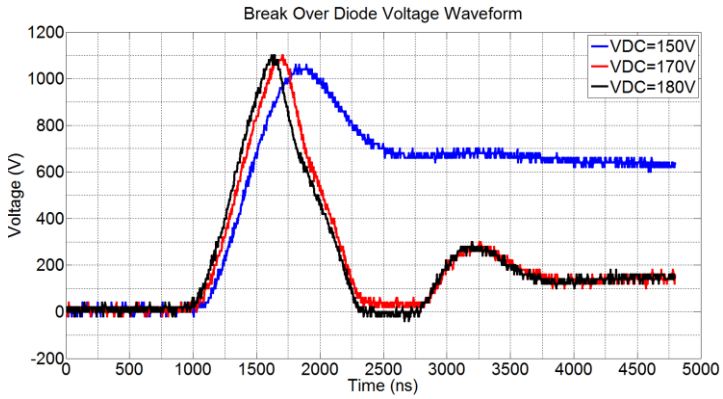

Figure 3.25 The Voltage Waveforms across Breakover Diode

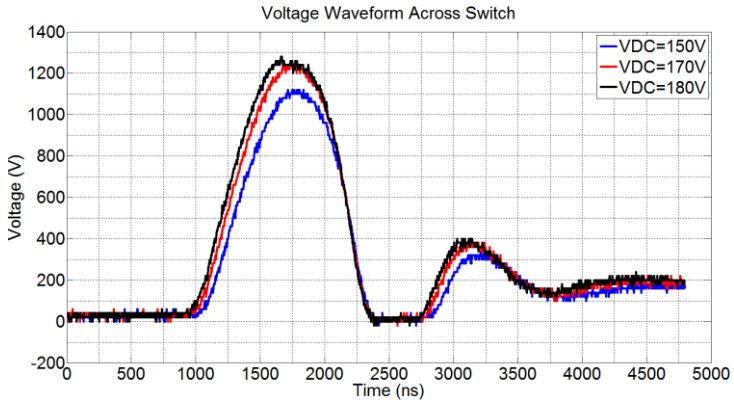

Figure 3.26 The Voltage Waveform over Switch

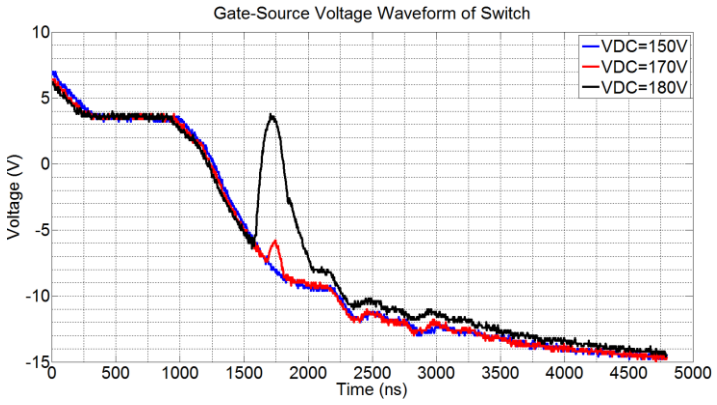

Figure 3.27 The Gate-Source Voltage Waveform of Switch

3.6 DESIGN OF CONTROL SYSTEM

The block diagram of digital signal controller based printed circuit board (PCB) is presented in Figure 3.28. The reactive power-adaptive DC link control block and space vector pulse width modulator are all implemented on TMS320F28335 type DSP microcontroller. DSC based controller card is designed for:

- Measuring analog signals,
- Generating the switching signals.

Analog measurement circuits are designed to measure the analog signals. The measurement circuits are designed to read the analog voltage within the range of ±10V. The measured variables are load currents, converter currents, system voltages and DC link current.

The measurement output taken from analog measurement block is evaluated in DSC and the required switching signals are generated. Firing circuits are used to provide switching signals to fiber optic transmitter.

Freewheel circuits are used for the fault condition of the system. In case of any fault in the system or DSC fails to operate correctly, s2 and s5 in Figure 3.28 are turned on by freewheel circuits while s1, s3, s4 and s6 are turned off simultaneously.

The picture of the DSC based controller card is given in Figure 3.29.

The schematic of DSC based controller card is given in Appendix E.

The flowchart implemented in DSC based controller is given in Appendix F.

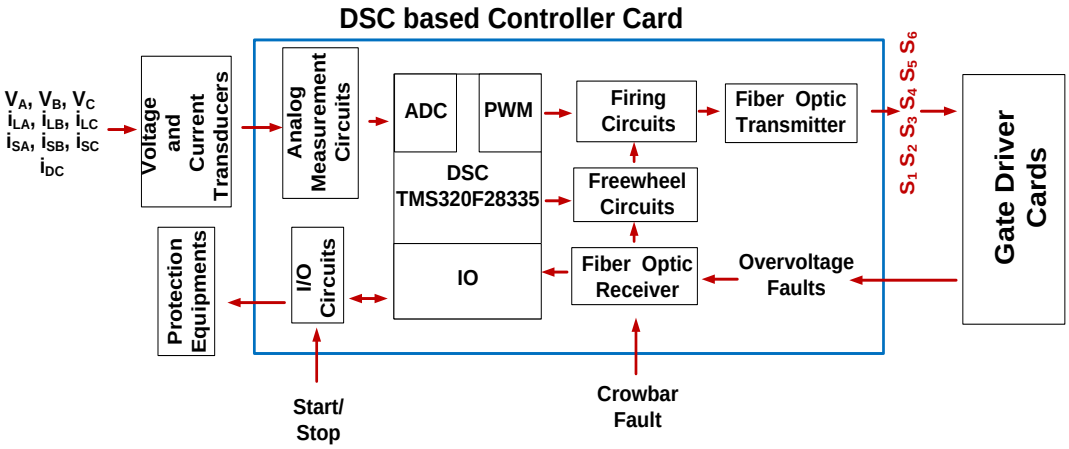

Figure 3.28 Block Diagram of DSC based Controller Card

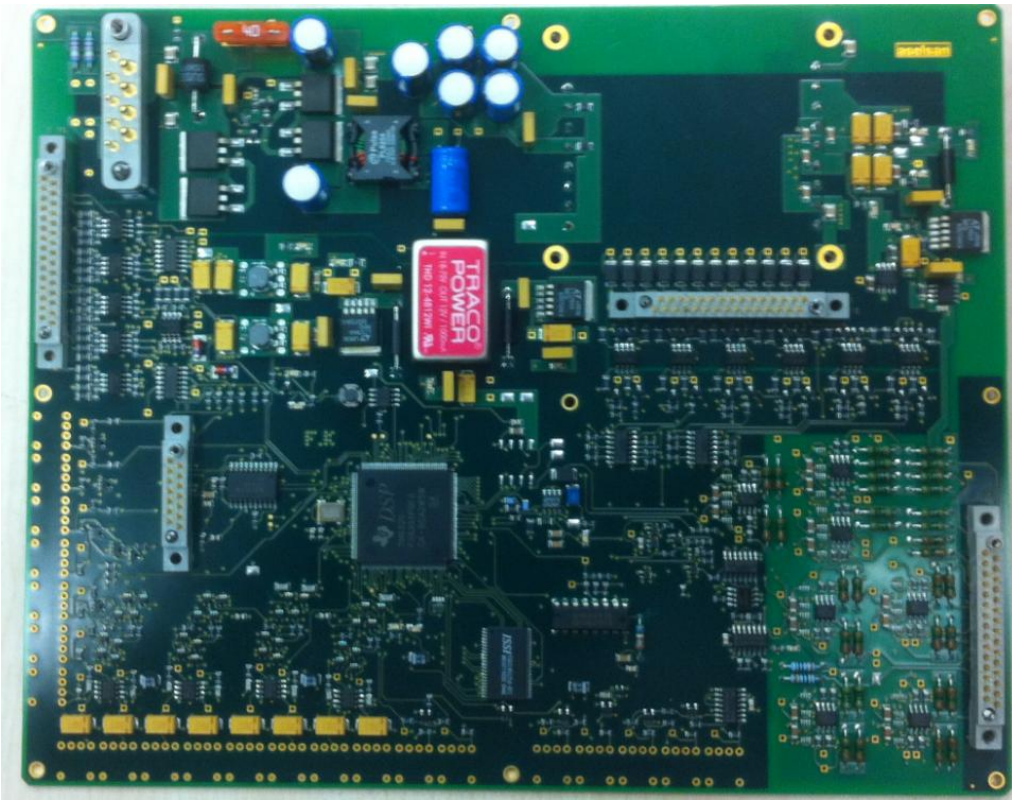

Figure 3.29 Picture of DSC based Controller Card

3.6.1 Applied DC Link Current Reference Algorithm

In Chapter 2, the flowchart of adaptive control of DC link current is derived by assuming that reference current vector I_{ref} is composed of only I_q and equal to i_{dc} (i.e., $M = 1$). This assumption is not valid in practice because I_d cannot be neglected due to the losses of power semiconductors and DC link reactor even though I_d is much smaller than I_q. Moreover, I_{ref} should contain the components from the active damping block. In practice, these contributions are also much smaller than I_q. The field experiences has showed that an additional 20A should be added to the reference DC link current, i_{dc_ref} in Figure 2.13. By experience on the field, the minimum value for the reference DC link current is found to be 50A instead of 0A proposed in Figure 2.14 theoretically. Otherwise, there exist discontinuities in DC link current, which degrades the performance of STATCOM. The flowchart which is implemented on DSC is as shown in Figure 3.30.

Since capacitance in the per phase-delta has been chosen as 200uF and the rms value of per phase supply voltage is 230V, I_{cap_q} and the reactive power of capacitor bank in the low pass filter can be calculated to be 61A and 30kVAr, respectively. The variation of reference DC link current with respect to the reactive power of STATCOM is plotted both for theoretical and practical cases in Figure 3.31.

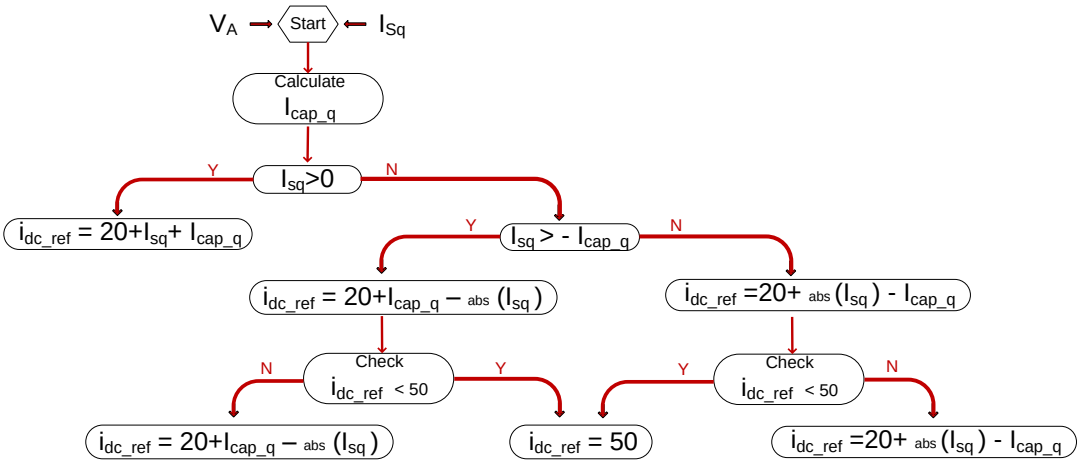

Figure 3.30 Flowchart of Reference DC link Current Algorithm

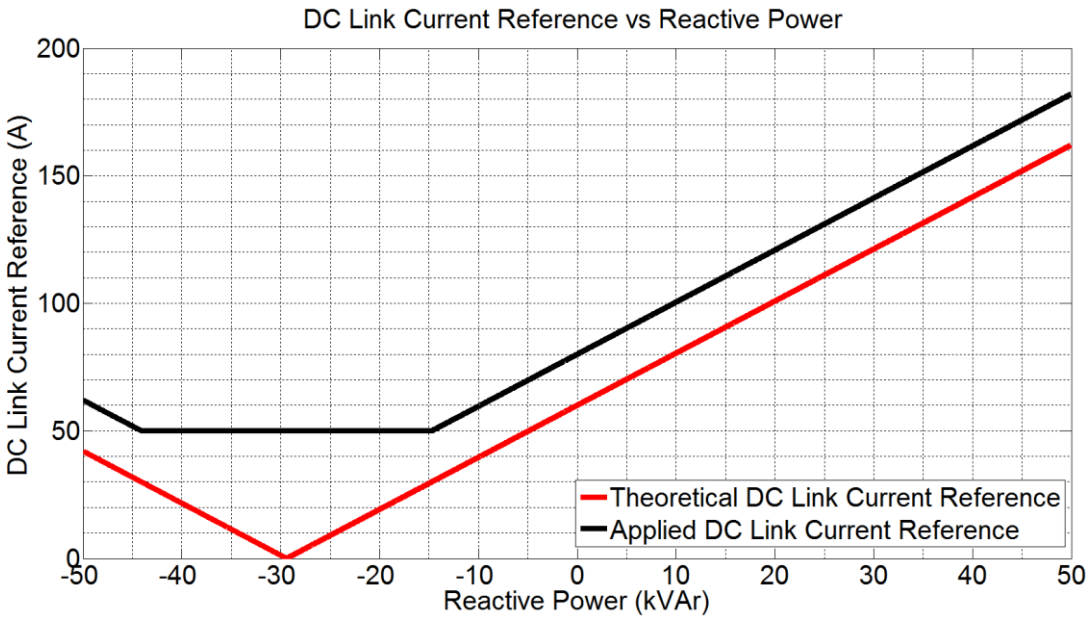

Figure 3.31 Applied DC Link Current Reference

3.7 SUMMARY

In this chapter, low pass filter at the input of CSC is explained. The values of filter capacitor and reactor are determined in view of filter performance, voltage regulation, size of filter capacitor. Later, DC link reactor value is determined by considering peak to peak ripple of DC link current and TDD of line current. Then, selection of power semiconductor and design of laminated busbar are mentioned. For selected IGBT, switching tests are applied to determine parasitic inductance value on commutation paths. Power dissipation on IGBT is calculated for verification of it in view of thermal considerations. The overvoltage protection circuit is expressed and tests are applied to verify the developed circuit. Finally, design of control system and applied DC link current reference is given. The properties of the developed system are given in Table 3.4.

Table 3.4 Properties of Designed CSC based STATCOM

Property	**Value**
Converter Reactive Power	±50kVAr
System Voltage	0.4kV
Cooling System	Forced Air Cooling
Current TDD of CSC	<=5%
DC Link Current Range	50A-180A
Corner Frequency of the Filter	330Hz
Reactive Power Contribution of the Filter	30 kVAr Capacitive
DC Link Reactor Value	2mH
Modulation Frequency	6250Hz

CHAPTER 4

EXPERIMENTAL RESULTS

Using the design principles given in Chapter 3, ±50kVAr CSC based STATCOM is developed at 0.4kV system voltage. SVPWM technique with a modulation frequency of 6250Hz is employed via digital signal controller. The control of reactive and active power has been achieved by synchronous rotating frame based control theory.

The developed system and proposed methods are verified by simulation works firstly and then experimental tests. The success of the developed system in experimental results is evaluated by using the performance parameters defined below:

Settling Time: The settling time (T_s) is the time required for the output to settle within 5% of its final value [67].

Response Time (i.e., rise or fall time): The response time (T_r) is the time passing for the output to reach from initial to 90% of its final value [67].

Maximum Overshoot: Maximum peak value of the response measured from the desired response is defined as maximum overshoot.

In Figure 4.1, response time, settling time and maximum overshoot is illustrated for a step response.

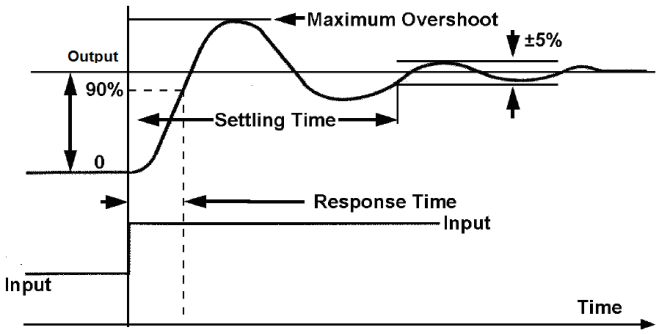

Figure 4.1 Response, Settling Times and Maximum Overshoot of the System Response

Total Demand Distortion: Total demand distortion is the harmonic current distortion in % maximum of demanded load current. From the view of harmonic contents, the injected current by STATCOM will be compared to limit values given in IEEE Std. 519-1992 [48].

During experimental tests, the developed system has been tested at different operating conditions. In this chapter, test results will be presented and discussed.

4.1 LABORATORY PROTOTYPE

The circuit diagram of the developed CSC based STATCOM system is given in Figure 4.2. The pictures of the developed system are illustrated in Figure 4.3 and Figure 4.4, respectively.

In the Table 4.1, the list of the component used in CSC and their features are enlisted. In Figure 4.3 and Figure 4.4, the components used in CSC are shown with the numbers matched with Table 4.1.

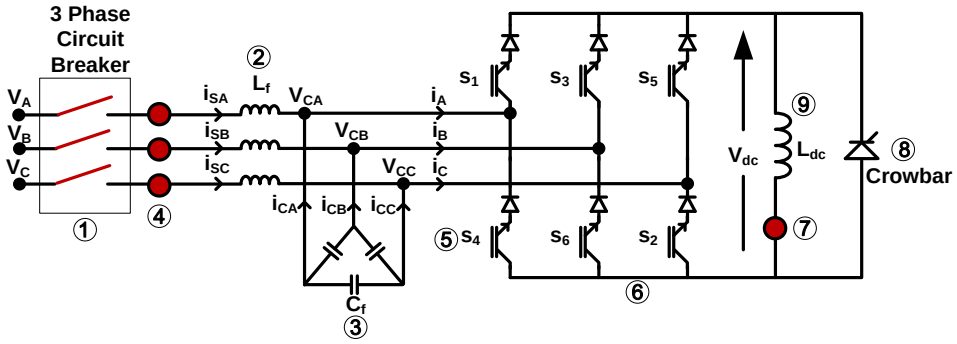

Figure 4.2 CSC STATCOM Circuit Diagram

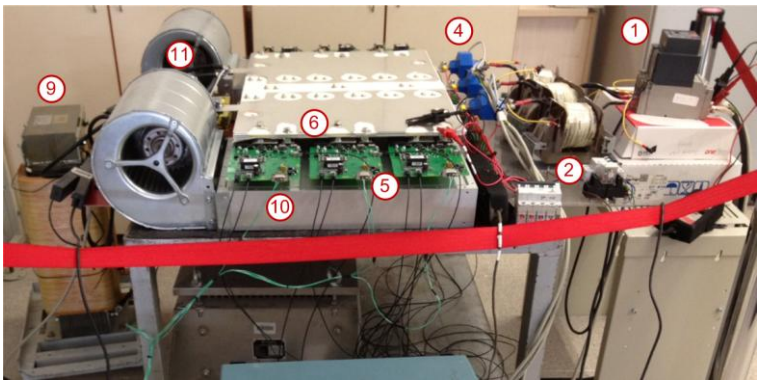

Figure 4.3 CSC based STATCOM Side View

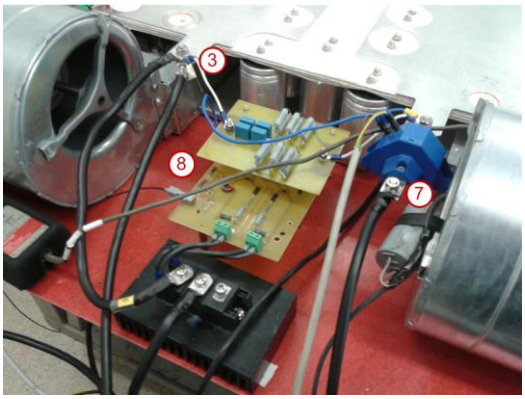

Figure 4.4 CSC based STATCOM Back View

Table 4.1 The list of Component used in CSC

No	Component	Description
1	Circuit Breaker	ABB Sace Tmax XT3S 250
2	AC Filter Reactor	Lg=385 uH 24 Turn
3	AC Filter Capacitor	5x40uF (200uF/Delta)
4	AC Current Sensor	LEM 200A rms
5	IGBT	DIM400DCM17-A000
6	Laminated Bus Bar	2mm Copper Plaete
7	DC Current Sensor	LEM 250A rms
8	Crowbar Circuit and Thyristor	IXYS MCC 162-14
9	DC Link Reactor	2mH Iron Core
10	Heat Sink (Air Cooler)	Austerlitz KS 300-14
11	Cooler Fan	EBMPAPST D2E160

4.2 EXPERIMENTAL RESULTS

4.2.1 Transient Response of STATCOM to Rapidly Changing Reactive Power Demand

Transient response of the system to a step change in reactive power demand of load will be evaluated by measuring the change in reactive power and DC link current of STATCOM. Step change in reactive power demand of load has been emulated by software in digital signal controller. Since STATCOM has been developed for reactive power compensation of balanced loads, the reactive power of STATCOM can be calculated as follows:

$$Q = \frac{1}{10ms} . \ \overline{3} . \int_{t=0}^{t=10ms} i_{SA}(t) \, . \, V_{BC}(t) \qquad (4.1)$$

In order to obtain the reactive power of STATCOM as given (4.1), the line current of STATCOM at phase-A (i_{SA}) and line-to-line voltage between phases-B and-C at the point of common coupling have been recorded by using Rogowski Coil current probe (RC1) and Tektronix P5210 high voltage differential probe (HV1). DC link reactor current waveform is recorded by connecting Tektronix P5050 passive probe to the output of the DC current sensor, specified in Table 4.1. The measured variables are also marked on the circuit diagram in Figure 4.5.

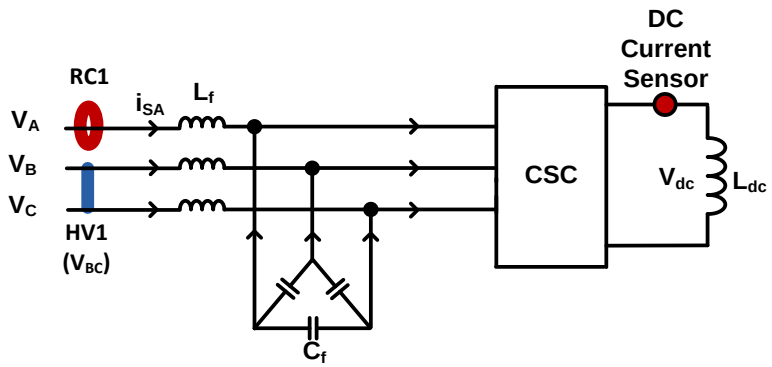

Figure 4.5 Illustration of Measured Quantities on Single Line Diagram

4.2.1.1 Constant DC Link Condition

STATCOM has been operated by keeping DC link current constant at a fixed value and applying a successive step changes in reactive power demand of load. These step changes have made STATCOM to operate at 50kVAr inductive, 0VAr and 50kVAr capacitive reactive power. The results will be used as benchmark in evaluating the performance of STATCOM with adaptive DC link current control. The variation in reactive power and DC link current of STATCOM with constant current control are presented in Figure 4.6. The detailed reactive power generation waveform for transition 30kVAr capacitive to 50kVAr inductive, 50kVAr inductive

to 0kVAr and 0kVAr to 50kVAr capacitive are given in Figure 4.7, Figure 4.8 and Figure 4.9, respectively. The response time, settling time and overshoot of the response are and marked on these figures. They are also tabulated in Table 4.2

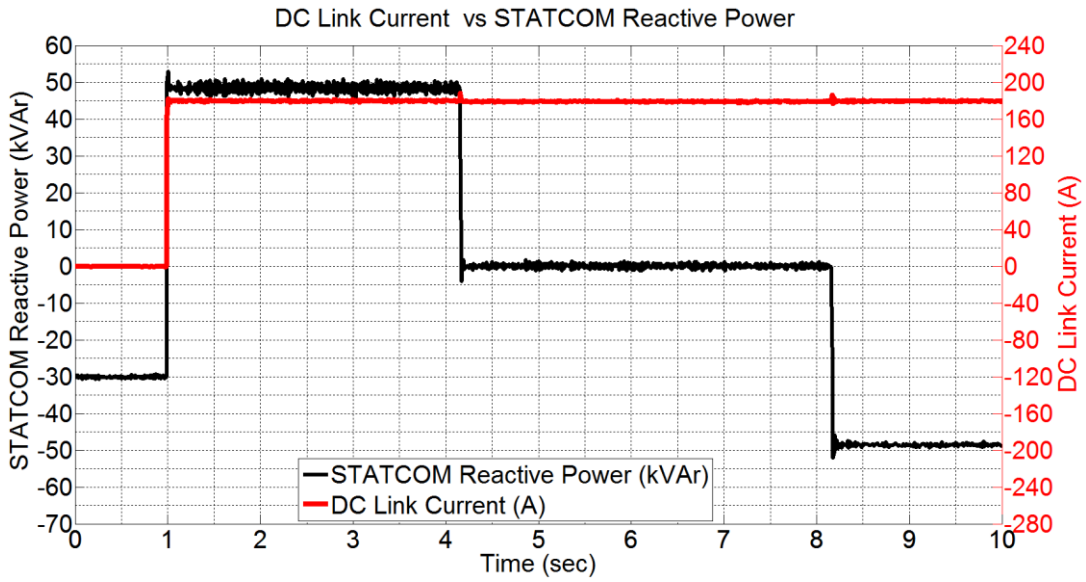

Figure 4.6 DC Link Current vs Reactive Power Generation of STATCOM for Constant DC link Current (sampling rate=10kS/s)

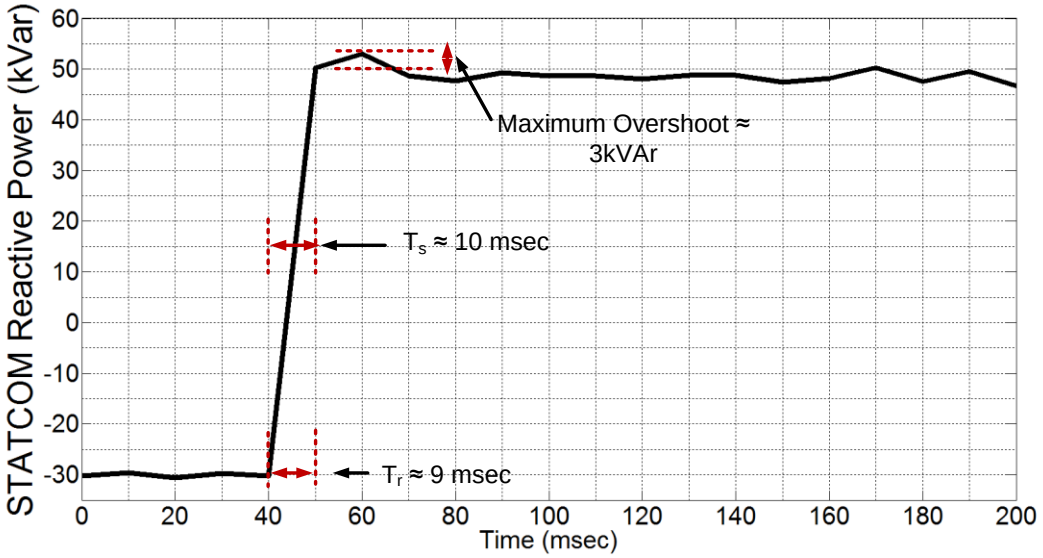

Figure 4.7 The Detailed Reactive Power Generation Waveform for Transition from 30kVAr Capacitive to 50kVAr Inductive Reactive Power Generation for Constant DC link Current (sampling rate=10kS/s) (averaged at 1000 sample)

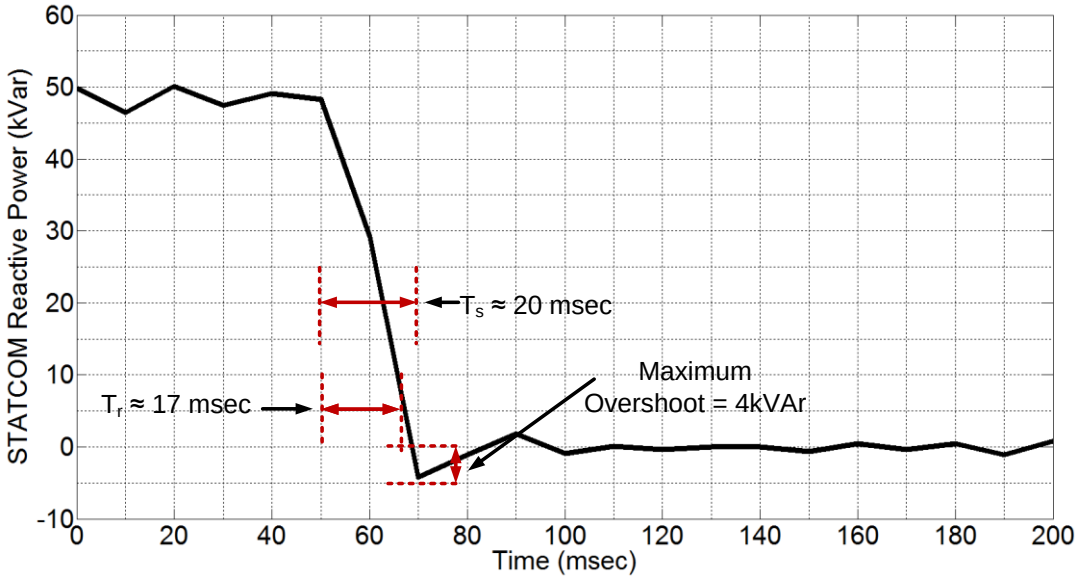

Figure 4.8 The Detailed Reactive Power Generation Waveform for Transition from 50kVAr Inductive to 0kVAr Reactive Power Generation (sampling rate=10kS/s) (averaged at 1000 sample)

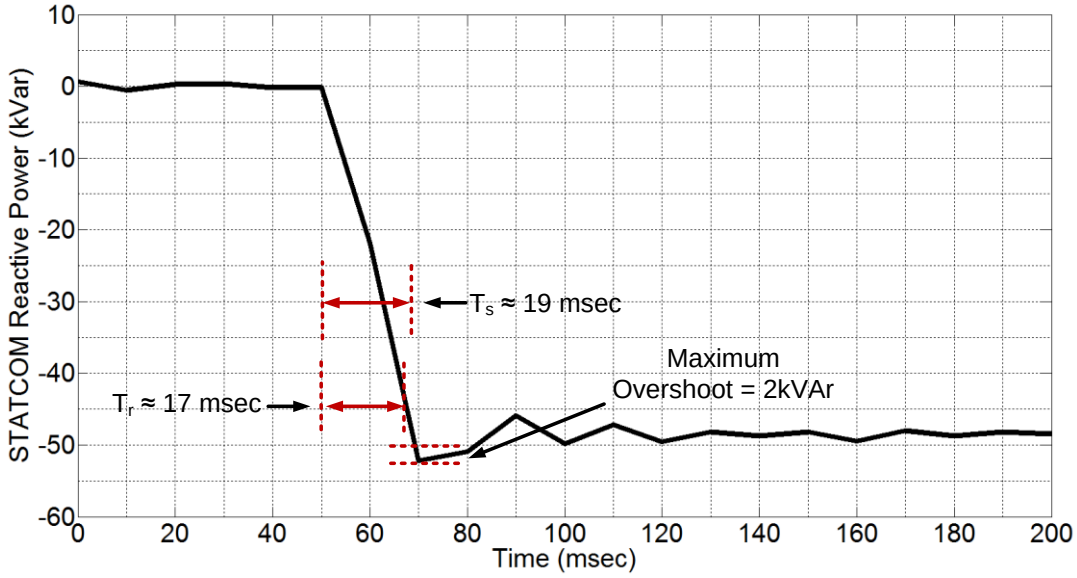

Figure 4.9 The Detailed Reactive Power Generation Waveform for Transition from 0VAr to 50kVAr Capacitive Reactive Power Generation (sampling rate=10kS/s) (averaged at 1000 sample)

Table 4.2 Transient Response of Reactive Power Generated by STATCOM with Constant DC link Current

Case	**Maximum Overshoot (kVAr)**	**Response Time (ms)**	**Settling Time(ms)**
30kVAr capacitive to 50kVAr inductive	3	9	10
50kVAr inductive to 0VAr	4	17	20
0VAr to 50kVAr capacitive	2	17	19

4.2.1.2 Adaptive Control of DC link Current

The flowchart given in Figure 3.30 is implemented on digital signal controller. Reactive power of STATCOM is adjusted to 50kVAr inductive, 50kVAr capacitive and 0VAr, respectively. The controller adjusts the DC link current to 180A for 50kVAr inductive, 60A for 50kVAr capacitive and 80A for 0VAr reactive power of STATCOM. Reactive power of STATCOM and the corresponding DC link current are given in Figure 4.10. The detailed waveforms of reactive power for a change from 30kVAr capacitive to 50kVAr inductive, from 50kVAr inductive to 50kVAr capacitive and 50kVAr capacitive to 0VAr are plotted in Figure 4.11, Figure 4.13, and Figure 4.15, so that performance parameters can be defined and marked on these figures. The summary of the transient response for reactive power is given in Table 4.3. Since adaptive control of dc-link current is also achieved simultaneously, the variations in DC link current, which depends on the variation in reactive power of STATCOM are given in Figure 4.12, Figure 4.14 and Figure 4.16. The parameters that characterize the transient response for the change in DC link current are given in Table 4.4. It is observed that peak to peak ripple current of DC link reactor is 10A at steady state operation. In order to define overshoot in DC link current, equation given in (4.2) will be used.

$$i_{dc,overshoot} = i_{dc,measured} - (i_{dc,final} \pm \frac{\Delta i_{DC}}{2}) \quad (4.2)$$

For positive overshoot in DC link current, the term $\frac{\Delta i_{DC}}{2}$ has positive sign and for negative overshoot, this term has negative sign.

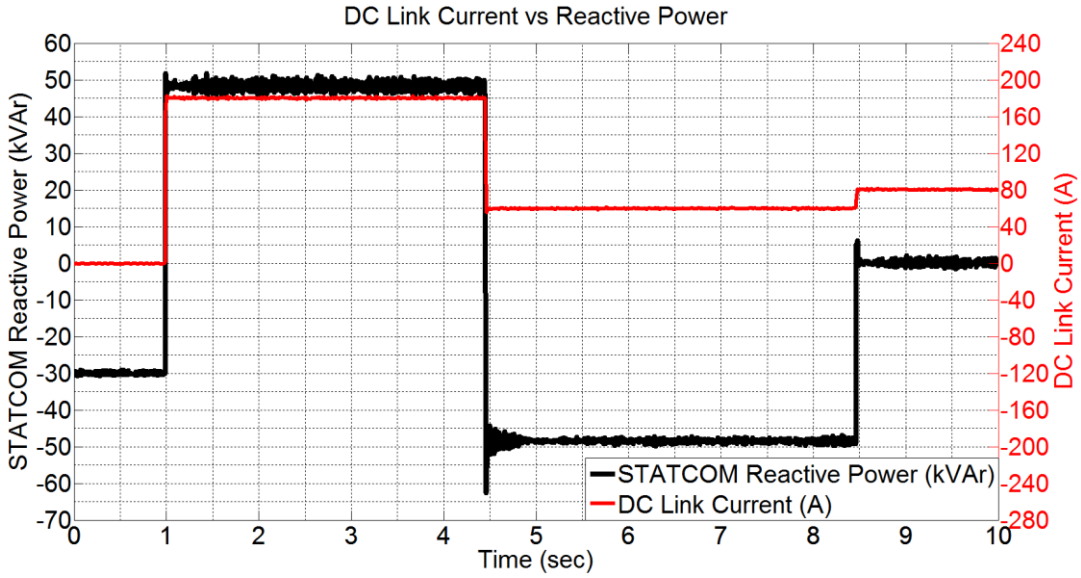

Figure 4.10 Reactive Power Generation of STATCOM for Adaptive DC link Current Control (sampling rate=10kS/s) (averaged at 1000 sample)

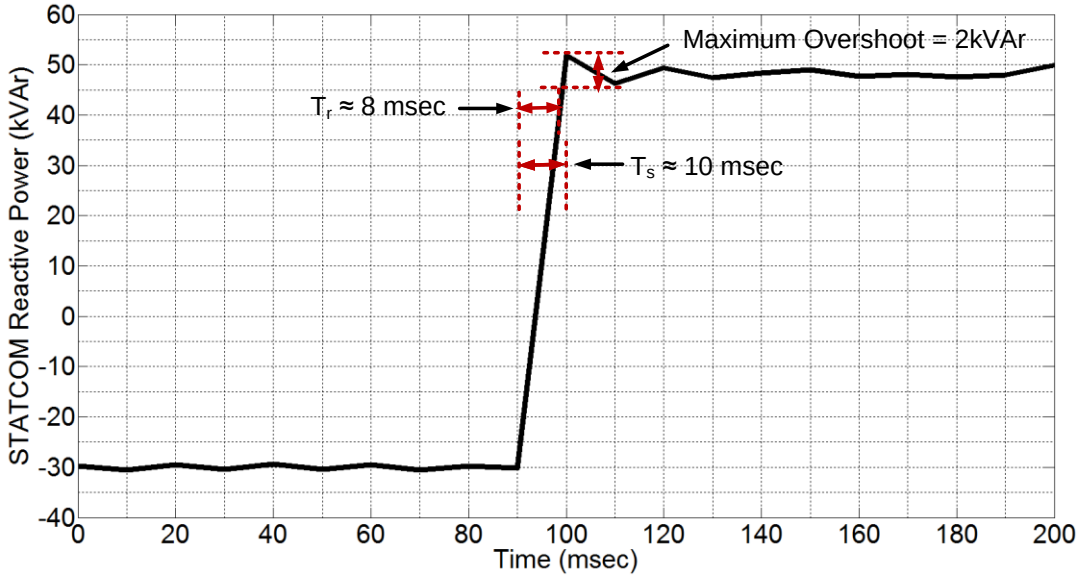

Figure 4.11 The Detailed Waveform of Transition from 30kVAr Capacitive to 50kVAr Inductive Reactive Power Generation for Adaptive DC Link Current (sampling rate=10kS/s) (averaged at 1000 sample)

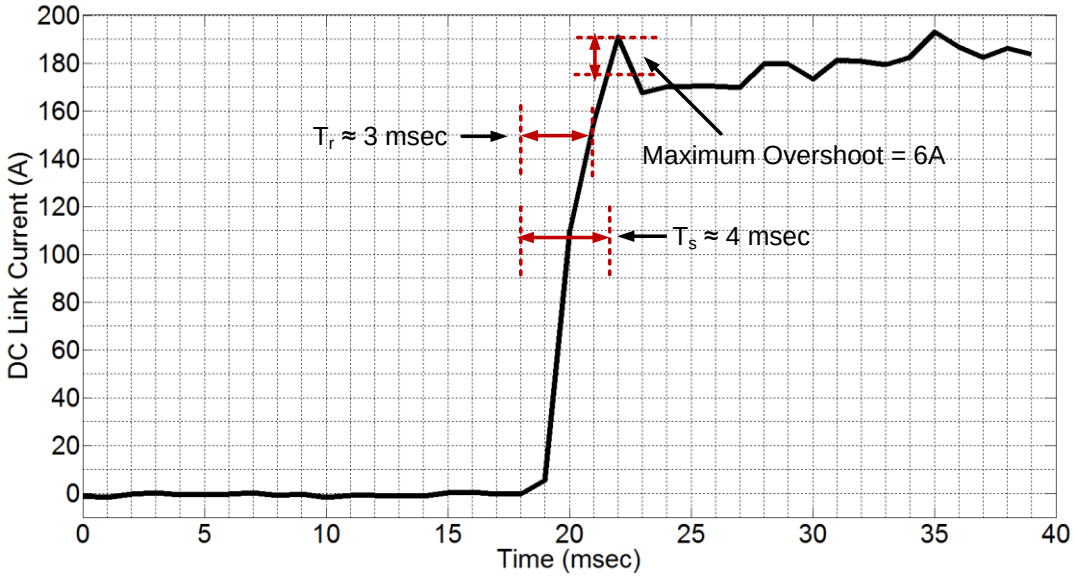

Figure 4.12 Transisiton of DC LinkCurrent from 0 to 180A (sampling rate=10kS/s) (averaged at 100 sample)

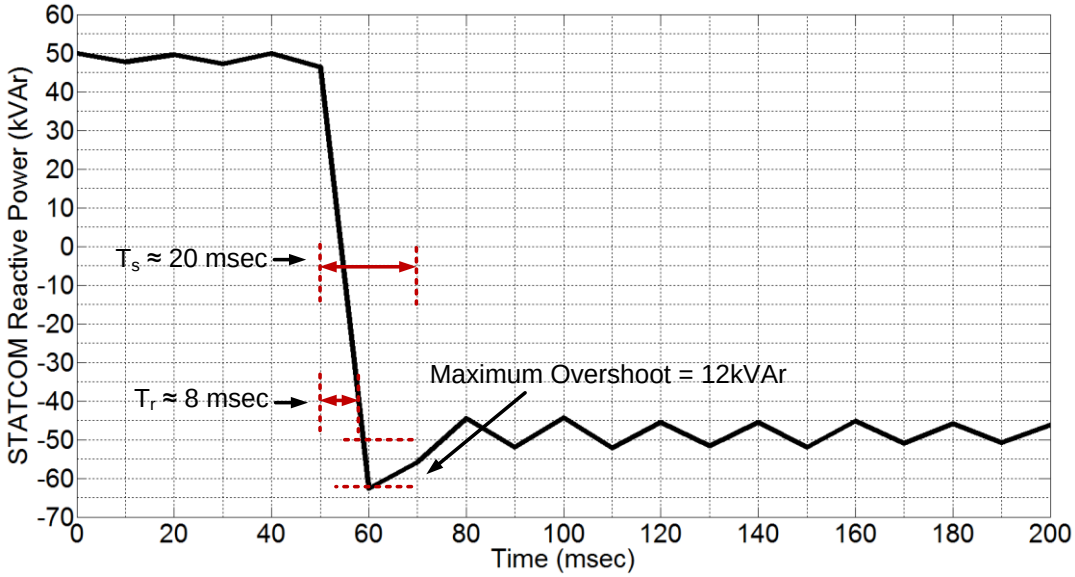

Figure 4.13 The Detailed Waveform of Transition from 50kVAr Inductive to 50kVAr Capacitive Reactive Power Generation for Adaptive DC Link Current (sampling rate=10kS/s) (averaged at 1000 sample)

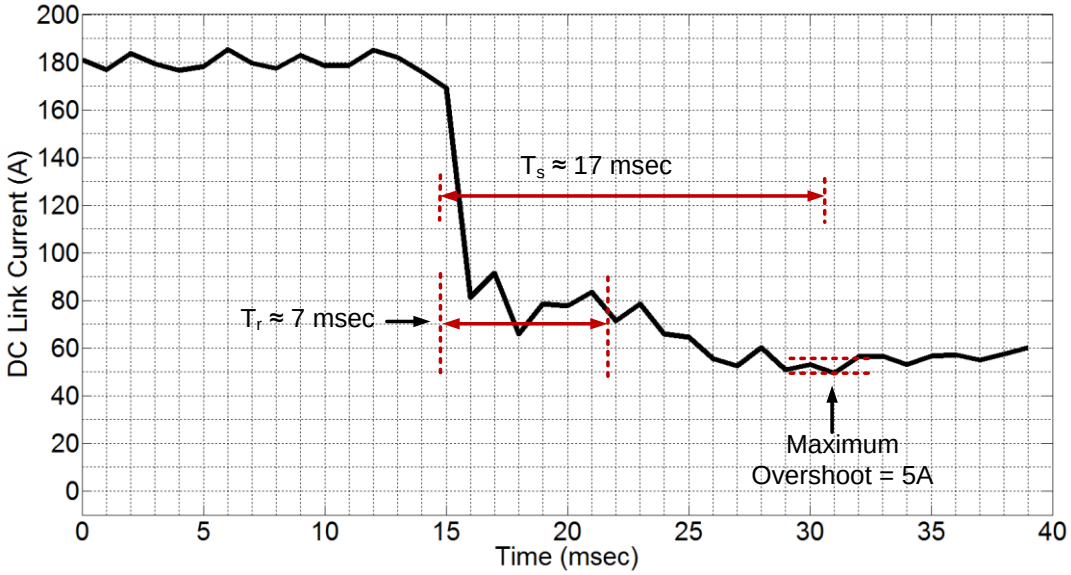

Figure 4.14 Transisiton of DC LinkCurrent from 180A to 60A (sampling rate=10kS/s) (averaged at 100 sample)

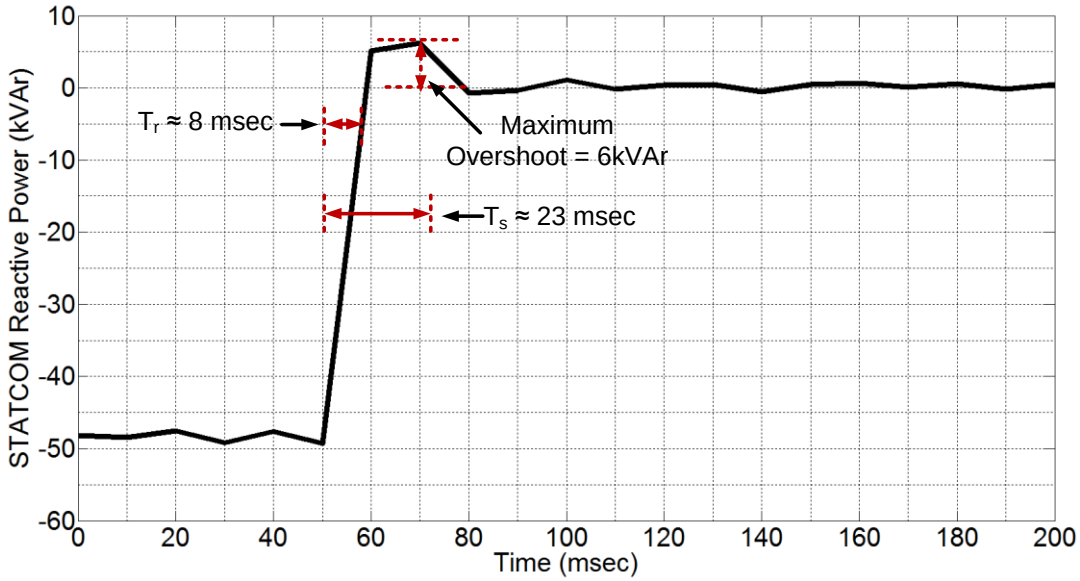

Figure 4.15 The Detailed Waveform of Transition from 50kVAr Capacitive to 0VAr Reactive Power Generation for Adaptive DC Link Current (sampling rate=10kS/s) (averaged at 1000 sample)

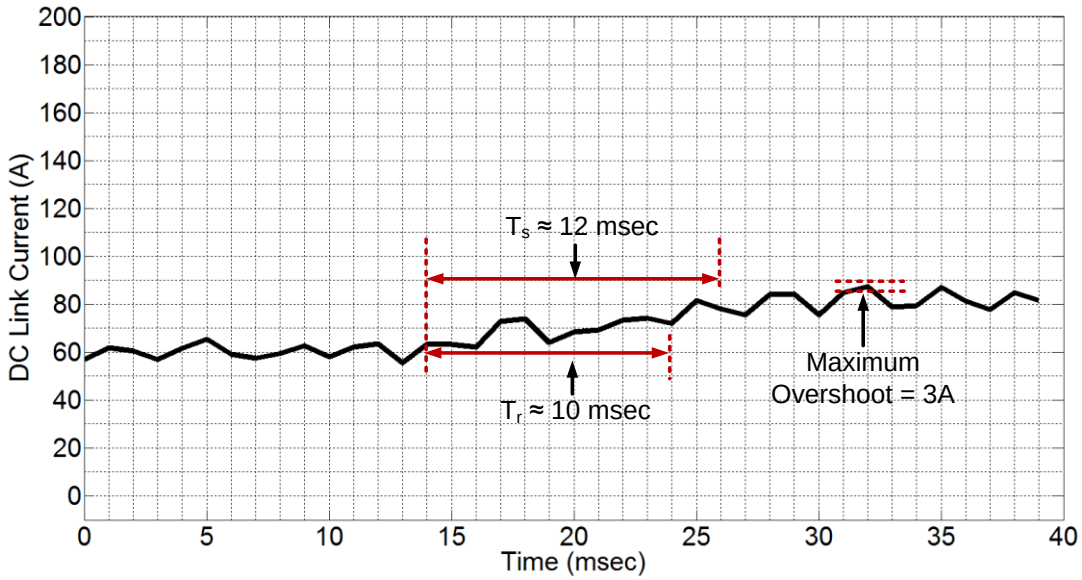

Figure 4.16 Transisiton of DC Link Current from 60A to 80A (sampling rate=10kS/s) (averaged at 100 sample)

Table 4.3 Transient Response of Reactive Power Generation for Adaptive DC link Current

Case	**Maximum Overshoot (kVAr)**	**Response Time (ms)**	**Settling Time(ms)**
30kVAr capacitive to 50kVAr inductive	2	8	10
50kVAr inductive to 50kVAr capacitive	12	8	20
50kVAr capacitive to 0VAr	6	8	23

Table 4.4 Transient Response of DC Link Current

Condition	Maximum Overshoot (A)	Response Time (ms)	Settling Time(ms)
0A to 180A	6	3	4
180A to 60A	5	7	17
60A to 80A	3	10	12

4.2.1.3 Discussion on Transient Response of the System

There are two control loops for controlling DC link and reactive power generation as shown in Figure 2.21. First, PI parameters in DC link current control block are adjusted and then, PI parameters of reactive power control block are optimized by using Ziegler-Nichols rule. In constant DC link current condition, the effect of the term I_{d_pi} is negligible. However, in adaptive DC link current condition, both I_{d_pi} and I_{q_pi} terms will be effective in transient response of the system.

As stated in Table 4.2, the maximum response time and settling time in variation of reactive power are found to be less than 20ms for constant DC link current control. These results are benchmark for evaluating the performance of adaptive control of DC link current. Maximum overshoot observed during transition of 50kVAr inductive to 0VAr reactive power generation is 4kVAr which is equal to 8% overshoot.

It is observed that response time of STATCOM has been improved from 17ms to 8ms by applying the adaptive control of DC link current. This result is no suprise because the simultaneous change in DC link current accelerates the change in reactive power. It is also evident from the response time of DC link current, which is less than 8ms. Inevitable result is the slight increase in overshoot of reactive power because there are two simultaneously operating control loops in comparison to constant DC link current control. In spite of these, the settling time is almost

unchanged. This shows that adaptive control of DC link current is fast enough not to degrade the speed of STATCOM in reactive power compensation.

4.3 HARMONIC PERFORMANCE

Since STATCOM is considered as an independent component connected to the common point of coupling of the utility, its line currents should meet the harmonic limits, which are specified by [48] and imposed by the utility operator. Therefore, the line currents of STATCOM are recorded for four different operating conditions: i) STATCOM blocked, ii) 50kVAr inductive reactive power generation, iii) 50kVAr capacitive reactive power generation, iv) 0VAr reactive power generation so that their harmonic spectrum can be analyzed. These records are given in Figure 4.17-Figure 4.20. In order to make benchmarking, line currents of STATCOM for constant DC link current control and adaptive DC link current control are plotted on each figure.

The harmonic spectra of the line current, i_{SA} are presented in Figure 4.21 and Figure 4.22 for constant DC link current control and adaptive DC link current control, respectively. The significant harmonic components in line currents of CSC (i_A in Figure 2.8) are located around 6250Hz. Low pass filter which has the corner frequency at 330Hz attenuates these harmonic components to negligible magnitudes. On the other hand, there exist low order harmonic components (i.e., 5^{th}, 7^{th}) in CSC line currents due to the overlaps in switching signals [2, 3] and characteristic of SVPWM. Low pass filter cannot attenuate these low order harmonic components. In order to observe the effects of these harmonics in STATCOM line currents, the harmonic spectra are given in Figure 4.21 and Figure 4.22. The significant low order harmonics which are obtained from Figure 4.21 and Figure 4.22 are summarized in Table 4.5. The harmonic limits in [48] have been used and given in Table 4.5 for the common point of coupling to which the developed STATCOM is connected.

The magnitude of harmonic components and total demand distortion of STATCOM line current are found to be nearly same both for the constant DC link current control and adaptive DC link current control. This can also be observed by comparing the waveforms in Figure 4.18-Figure 4.20, harmonic spectra in Figure 4.21 and Figure 4.22 and individual harmonic components in Table 4.5.

On the other hand, the magnitudes 5^{th} and 7^{th} harmonic components for both cases are higher than the limits. This is due to the low order harmonics which are injected by the other loads at the same point of common coupling (e.g., uninterruptible power supply- UPS) and sinked by the low pass input filter of STATCOM. This can also be observed from Table 4.5 and found that STATCOM line currents contain significant 5^{th} and 7^{th} harmonic components even if CSC is blocked (i.e., CSC is not operating). This problem can be avoided by adjusting the corner frequency of low pass filter to the higher values at the expense of an increase in harmonics at the carrier frequency [60].

It is also observed that there exists a fundamental component in line current at 0kVAr. It corresponds to active power transfer of STATCOM in order to maintain DC link current.

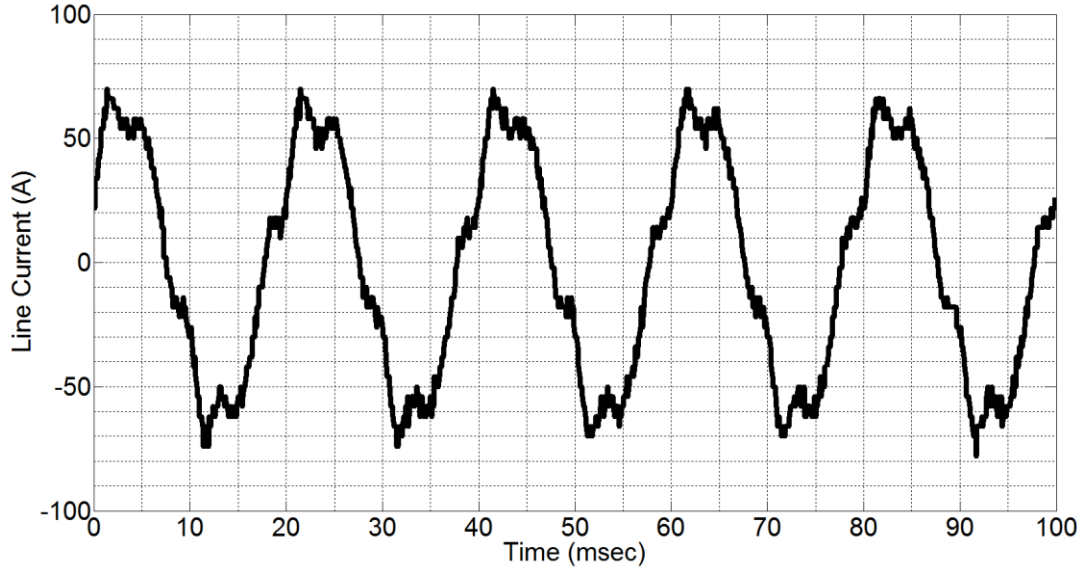

Figure 4.17 Line Current Waveform for CSC blocked (sampling rate=10kS/s)

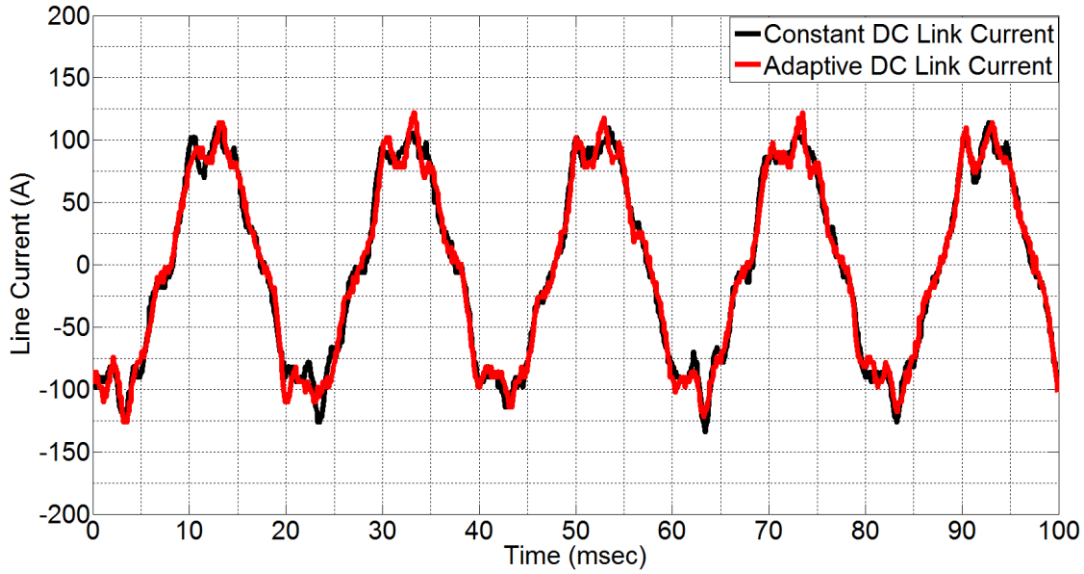

Figure 4.18 Line Current Waveform at 50kVAr Inductive Reactive Power Generation for Both Constant DC link Current and Adaptive DC Link Current (sampling rate=10kS/s) (averaged at 100 sample)

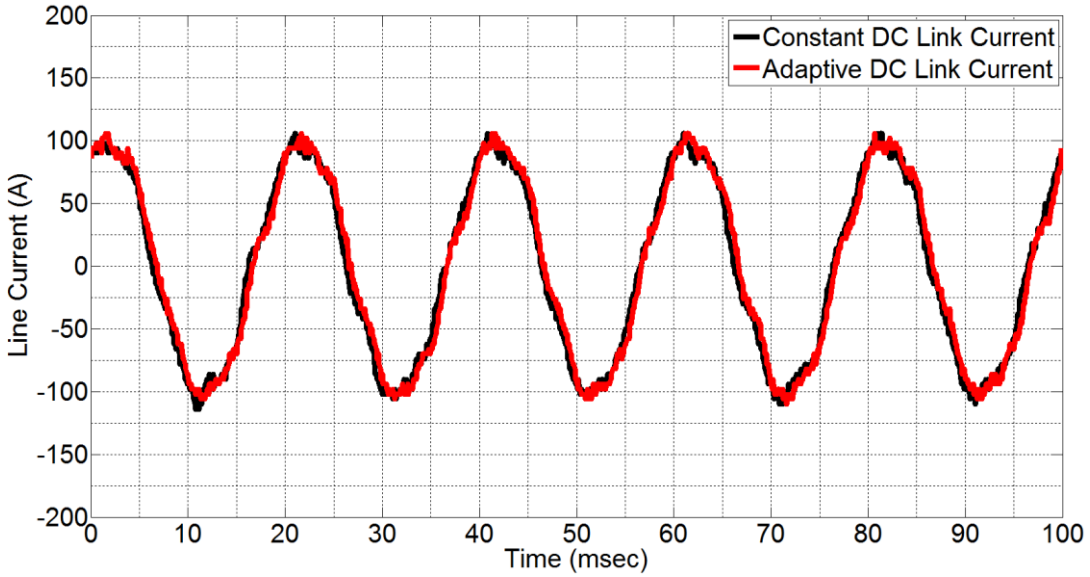

Figure 4.19 Line Current Waveform at 50kVAr Capacitive Reactive Power Generation for Both Constant DC link Current and Adaptive DC Link Current (sampling rate=10kS/s) (averaged at 100 sample)

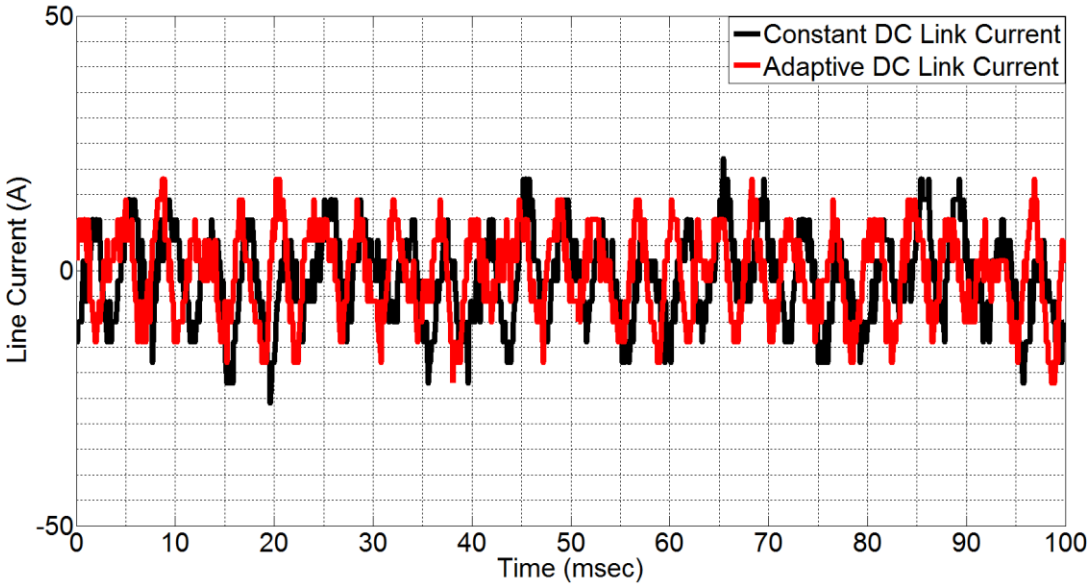

Figure 4.20 Filtered Converter Current Waveform at 0VAr Reactive Power Generation for Both Constant DC link Current and Adaptive DC Link Current (sampling rate=10kS/s) (averaged at 100 sample)

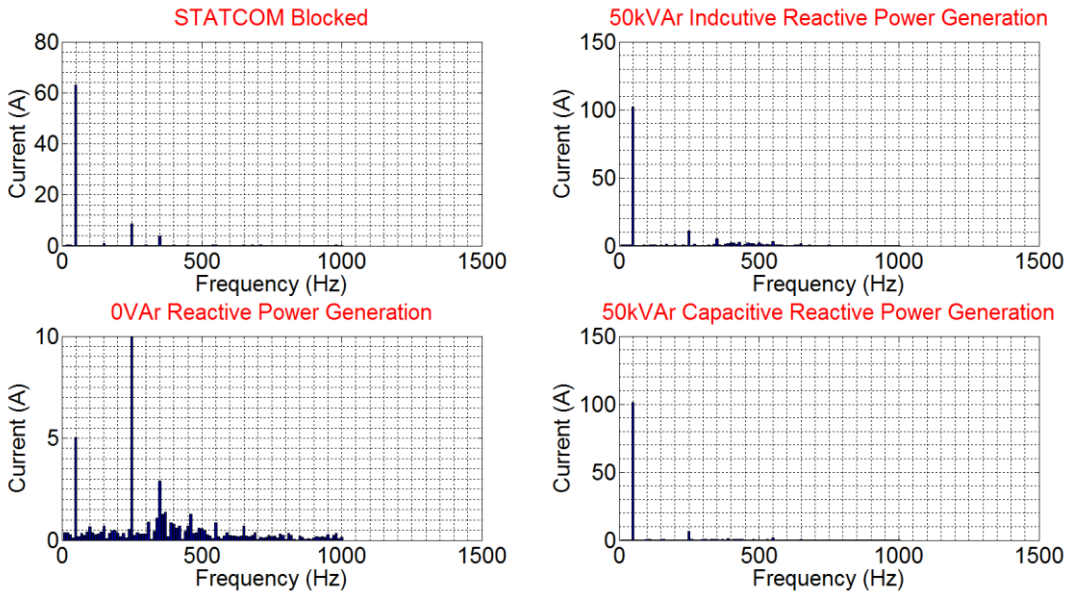

Figure 4.21 Harmonic Spectrum of Filtered Converter Current at Four Different Operating Conditions for Constant DC Link Current

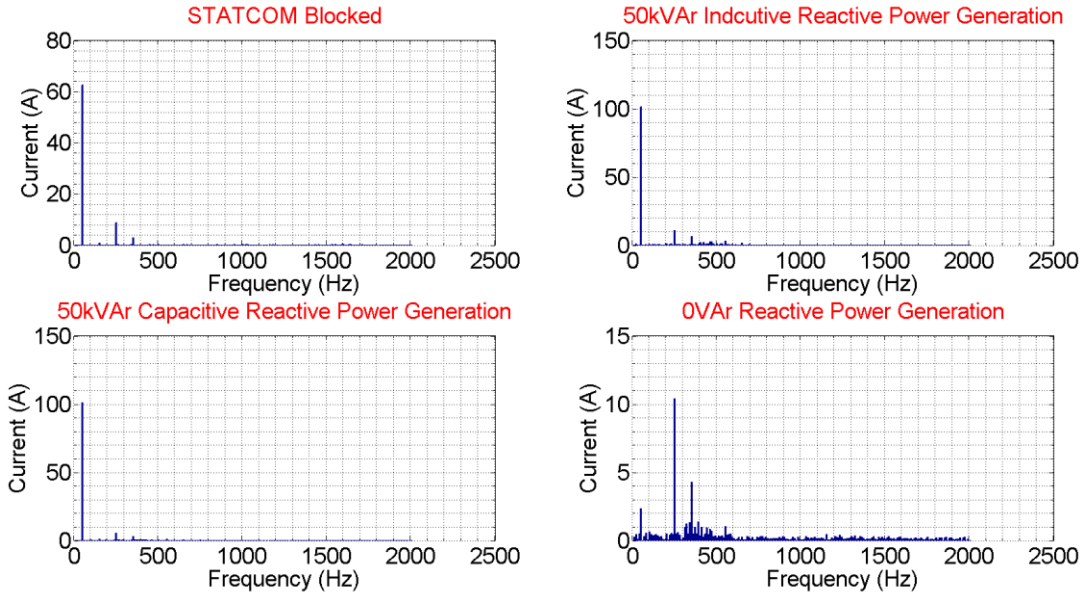

Figure 4.22 Harmonic Spectrum of Filtered Converter Current at Four Different Operating Conditions for Adaptive DC Link Current

Table 4.5 Harmonic Content of Filtered Converter Current and TDD Variations for Different Operating Conditions

Maximum demand STATCOM current (fundamental frequency component) at PCC is taken as 72A corresponding to 50kVAr reactive power generation at 0.4kV side of transformer. Maximum short circuit current at PCC is 30kA, therefore I_{SC}/I_1 =417

Harmonic #	**Control of DC link current**	**1**	**3**	**5**	**7**	**11**	**13**	**TDD**
		A						%
STATCOM Blocked	Adaptive	62.9	0.8	8.6	3.6	0.4	0.2	10.4
	Constant	62.5	0.7	8.9	2.9	0.6	0.3	10.4
50kVAr Inductive	Adaptive	101.8	0.1	10.8	6.0	3.5	1.8	15.4
	Constant	102.0	0.7	10.8	4.8	3.2	1.9	15.4
50kVAr Capacitive	Adaptive	101.1	0.9	5.6	3.7	0.8	0.8	8.8
	Constant	101.3	0.6	6.6	0.8	1.4	0.8	11.4
0VAr	Adaptive	2.3	0.4	10.0	3.9	0.9	0.3	12.2
	Constant	5.0	0.6	9.9	2.8	0.8	0.7	8.8
Limits in IEEE Std.519-1992 for I_{SC}/I_1<20			4%	4%	4%	2%	2%	5%
Limits in IEEE Std.519-1992 for 100<I_{SC}/I_1<1000			12%	12%	12%	5.5%	5.5%	%15

4.4 POWER LOSSES

Since adaptive control of DC link current is developed and applied to CSC based STATCOM in order to decrease its losses in comparison to a case where DC link current is kept constant, the variation of total losses in CSC based STATCOM against its reactive power are measured and presented in Figure 4.23.

Losses in CSC based STATCOM are due to:

- Losses of reactors in low pass filter,

- Conduction and switching losses of IGBT and fast recovery diode,
- Losses in DC link reactor.

Conduction losses of power semiconductors and copper losses in DC link reactor are the main components of losses of CSC based STATCOM and depend on the magnitude of DC link current. Since the magnitude of DC link current is continuously being updated in adaptive control case, it is no surprise to observe the total loss of STATCOM for adaptive case is lower than that of constant DC link current control case in Figure 4.23. This result shows that losses of STATCOM can be significantly decreased especially when it is used for loads which have the variations in its reactive power demand. This improvement results in significant saving in energy consumption especially for the large scale STATCOM applications (e.g., larger than 1MVAr).

When STATCOM is being operated at 50kVAr inductive reactive power, the magnitude of DC link current is same for both cases. As the reactive power changes from 50kVAr inductive to 50kVAr capacitive, DC link current is adjusted in adaptive control case according to Figure 3.30. Then the amount of decrease in loss of STATCOM also varies depending on the magnitude of DC link current.

Another observation is that total loss of STATCOM for constant DC link current case varies with its reactive power. This is due to the variation in current through the filter reactor in low pass filter.

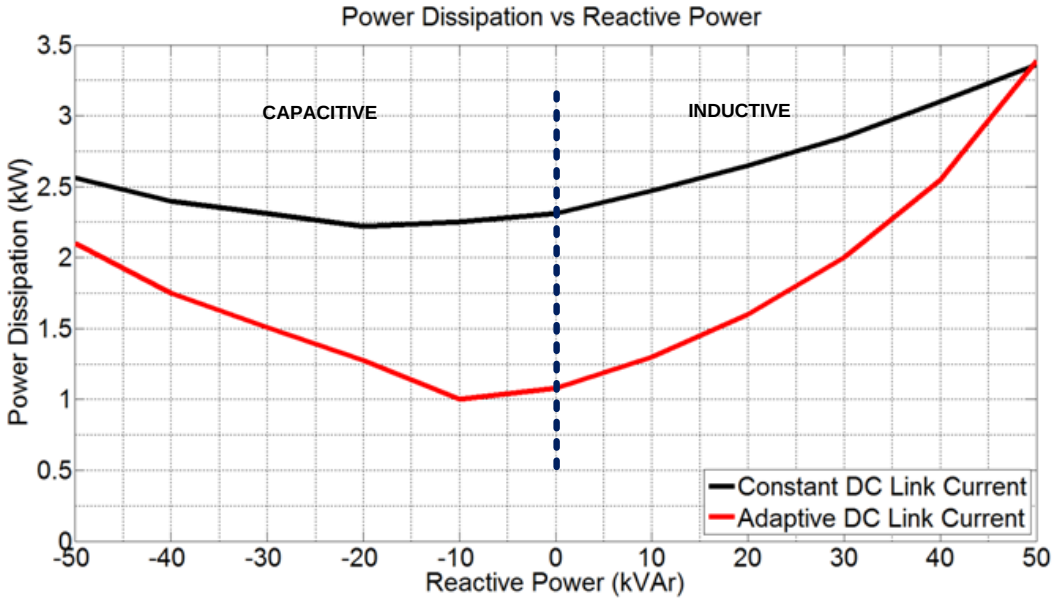

Figure 4.23 Total Losses of STATCOM against Its Reactive Power for Two Different Cases

CHAPTER 5

CONCLUSION

The three phase CSC based STATCOM has been designed and implemented in this thesis. The designed system has full-bridge current-source converter topology modulated with space vector pulse width modulation technique. The carrier frequency of SVPWM is set to 6250Hz. Low pass filter on AC side of CSC has been used in order to suppress harmonics at carrier frequency and its multiples. This research work has enhanced CSC based STATCOM by following features:

- To minimize parasitic inductances in current commutation paths of CSC, a special laminated busbar has been designed.
- A power module which contains 1700V, 400A rated IGBT and a fast recovery diode has used in order to minimize both the system footprint and stray inductances on the commutation paths. The terminals of IGBT and diode on the power module are connected such that bipolar voltage blocking capability is achieved.
- Active clamping method which is used in gate drive circuitry of IGBTs has been modified in order to enhance the overvoltage protection in CSC applications.
- Adaptive control of DC link current has been proposed and applied to CSC based STATCOM in order to decrease power losses of STATCOM over a wide operating range.

Following conclusions can be made from the results of theoretical and experimental work carried out within the scope of this study:

- The operation of CSC based STATCOM with adaptive control of DC link current has been proven at 0.4kV and +/-50kVAr.
- The line currents of STATCOM at common coupling point comply with the limits in IEEE Std. 519-1922.
- The developed system has satisfactory transient response to the step changes in reactive power demand and DC link current such that the response time for both variables is less than 20ms.
- By using on-line modulation technique, i.e., SVPWM, active damping has been applied in order to damp the resonance characteristic of input filter. This decreases power losses further in comparison to use of passive damping
- Adaptive control of DC link current decreases the power losses of CSC based STATCOM while it doesn't degrade the transient response performance of STATCOM.

An important consequence of this research work is that the power loss of CSC based STATCOM will not be a concern in comparison with VSC based STATCOM. As a future work, the load balancing feature (i.e., compensation of negative sequence components of the load currents) can be applied to the developed CSC based STATCOM.

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APPENDIX A

TECHNICAL SPECIFICATIONS OF IGBT FOR LOSS CALCULATION

T_{case} = 125°C unless stated otherwise

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Units
$t_{d(off)}$	Turn-off delay time	I_C = 400A V_{GE} = ±15V V_{CE} = 900V $R_{G(ON)}$ = 4.7Ω $R_{G(OFF)}$ = 4.7Ω L_S ~ 100nH		1400		ns
t_f	Fall time			130		ns
E_{OFF}	Turn-off energy loss			180		mJ
$t_{d(on)}$	Turn-on delay time			400		ns
t_r	Rise time			250		ns
E_{ON}	Turn-on energy loss			170		mJ
Q_{rr}	Diode reverse recovery charge	**IGBT arm** I_F = 400A V_{CE} = 900V dI_F/dt = 2000A/µs		170		µC
I_{rr}	Diode reverse recovery current			270		A
E_{rec}	Diode reverse recovery energy			100		mJ
Q_{rr}	Diode reverse recovery charge	**Diode arm** I_F = 400A V_{CE} = 900V dI_F/dt = 2000A/µs		425		µC
I_{rr}	Diode reverse recovery current			600		A
E_{rec}	Diode reverse recovery energy			250		mJ

Figure A 1 Technical Specifications of IGBT for Loss Calculation

APPENDIX B

TECHNICAL SPECIFICATIONS OF IGBT FOR THERMAL CIRCUIT

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Units
$R_{th(j-c)}$	Thermal resistance – transistor (per arm)	Continuous dissipation – junction to case	-	-	36	°C/kW
$R_{th(j-c)}$	Thermal resistance – diode (IGBT arm)	Continuous dissipation – junction to case	-	-	80	°C/kW
	Thermal resistance – diode (Diode arm)				40	°C/kW
$R_{th(c-h)}$	Thermal resistance – case to heatsink (per module)	Mounting torque 5Nm (with mounting grease)	-	-	8	°C/kW
T_j	Junction temperature	Transistor	-	-	150	°C
		Diode	-	-	125	°C
T_{stg}	Storage temperature range	-	-40	-	125	°C
	Screw torque	Mounting – M6	-	-	5	Nm
		Electrical connections – M4	-	-	2	Nm
		Electrical connections – M8	-	-	10	Nm

Figure B 1 Thermal Specifications of IGBT and Diode

APPENDIX C

TECHNICAL SPECIFICATIONS OF HEAT SINK WITH COOLER FAN

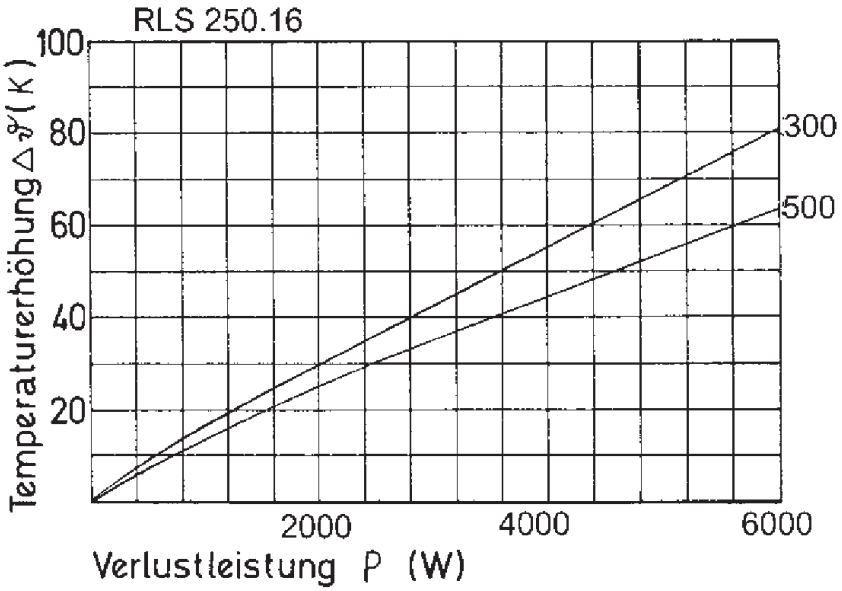

Figure C 1 Thermal Specifications of Cooling Plate with Cooler Fan

APPENDIX D

SCHEMATIC OF GATE DRIVER CARD

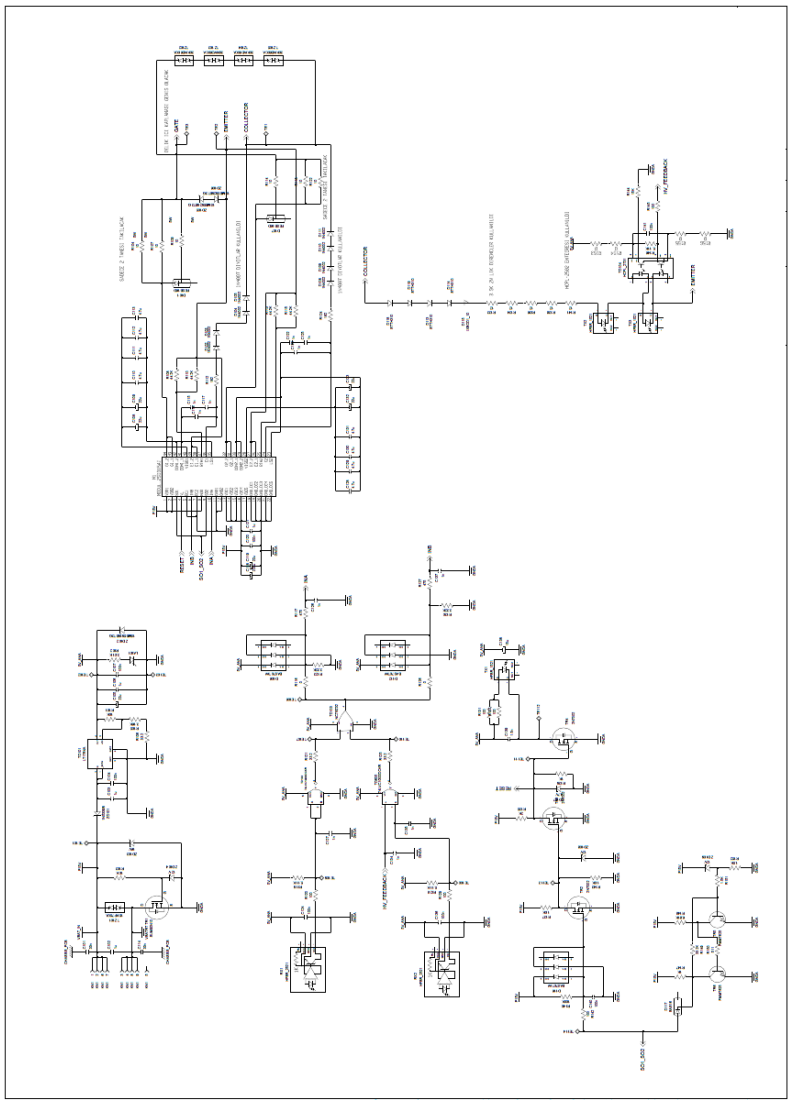

Figure D 1 Sheet 1of Gate Driver Card

APPENDIX E

SCHEMATIC OF DSC BASED CONTROLLER CARD

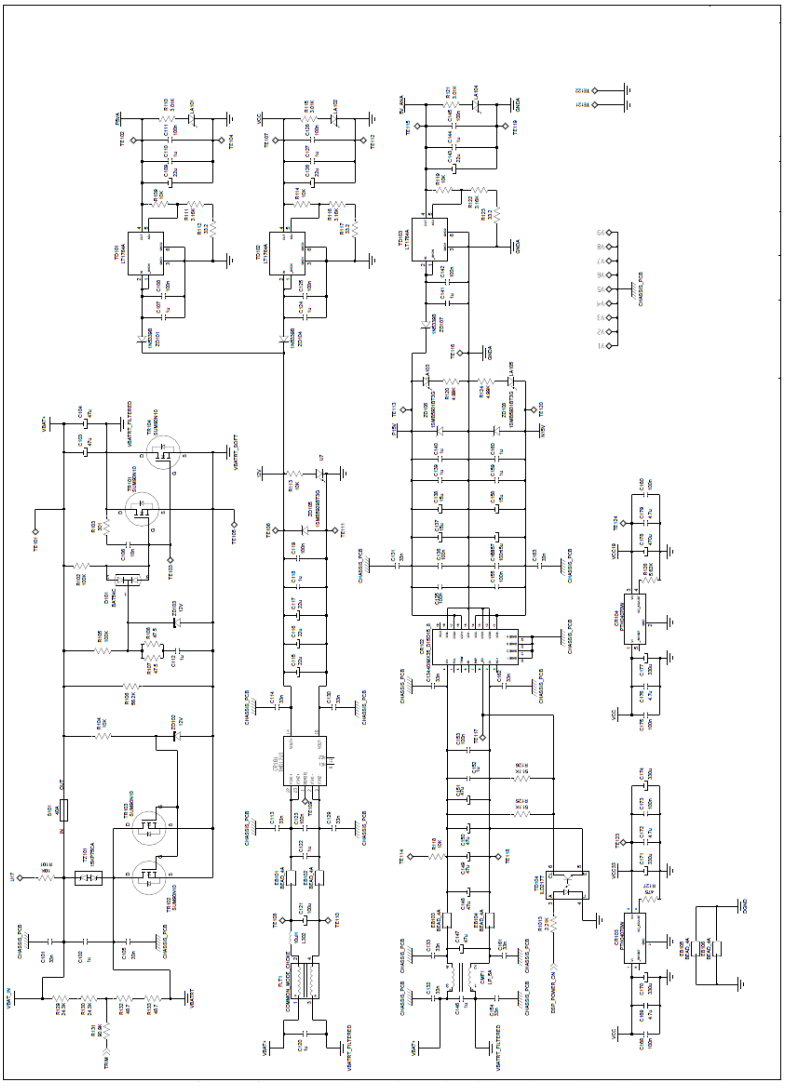

Figure E 1 Sheet 1 of DSC based Controller Card

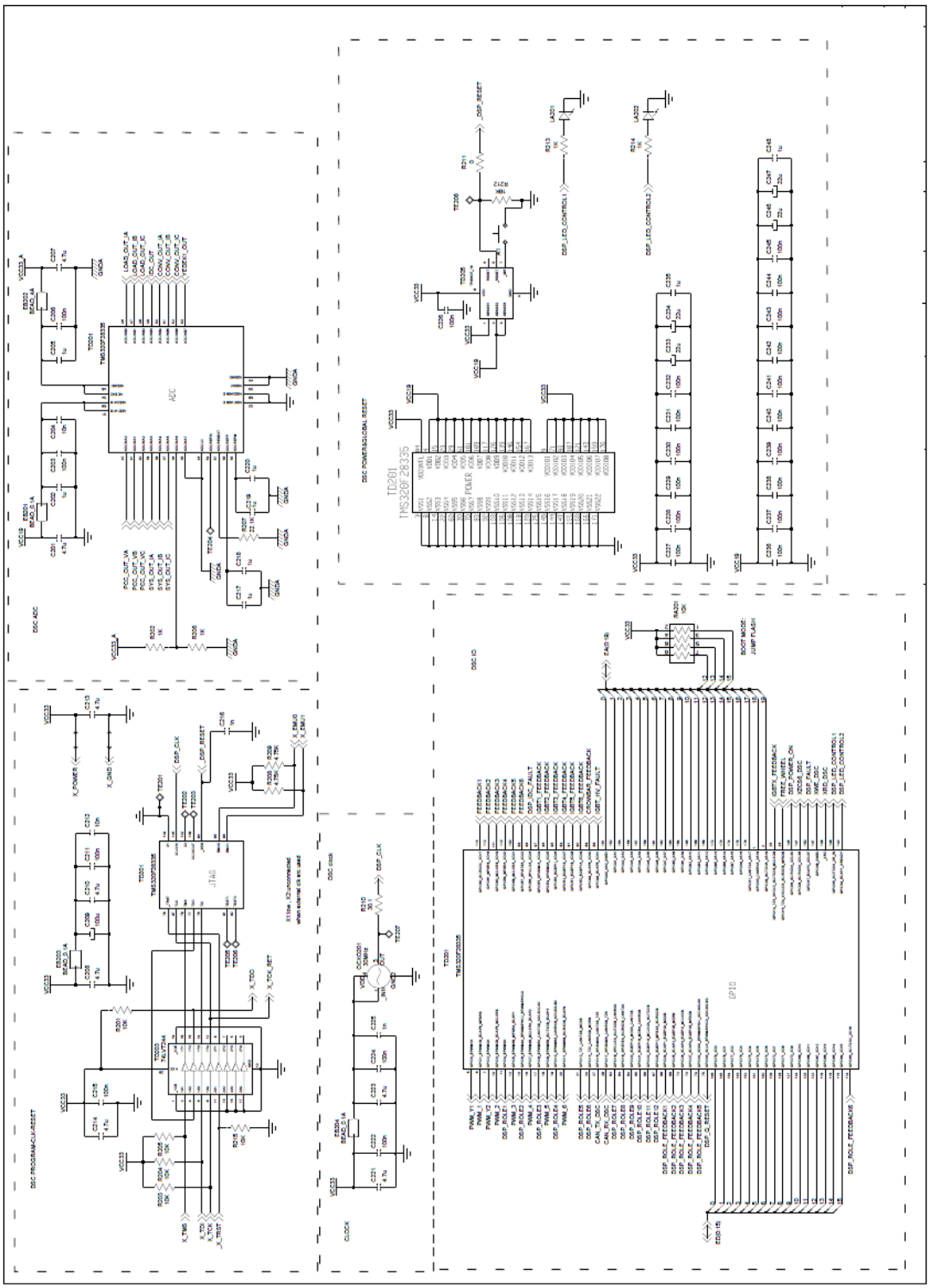

Figure E 2 Sheet 2 of DSC based Controller Card

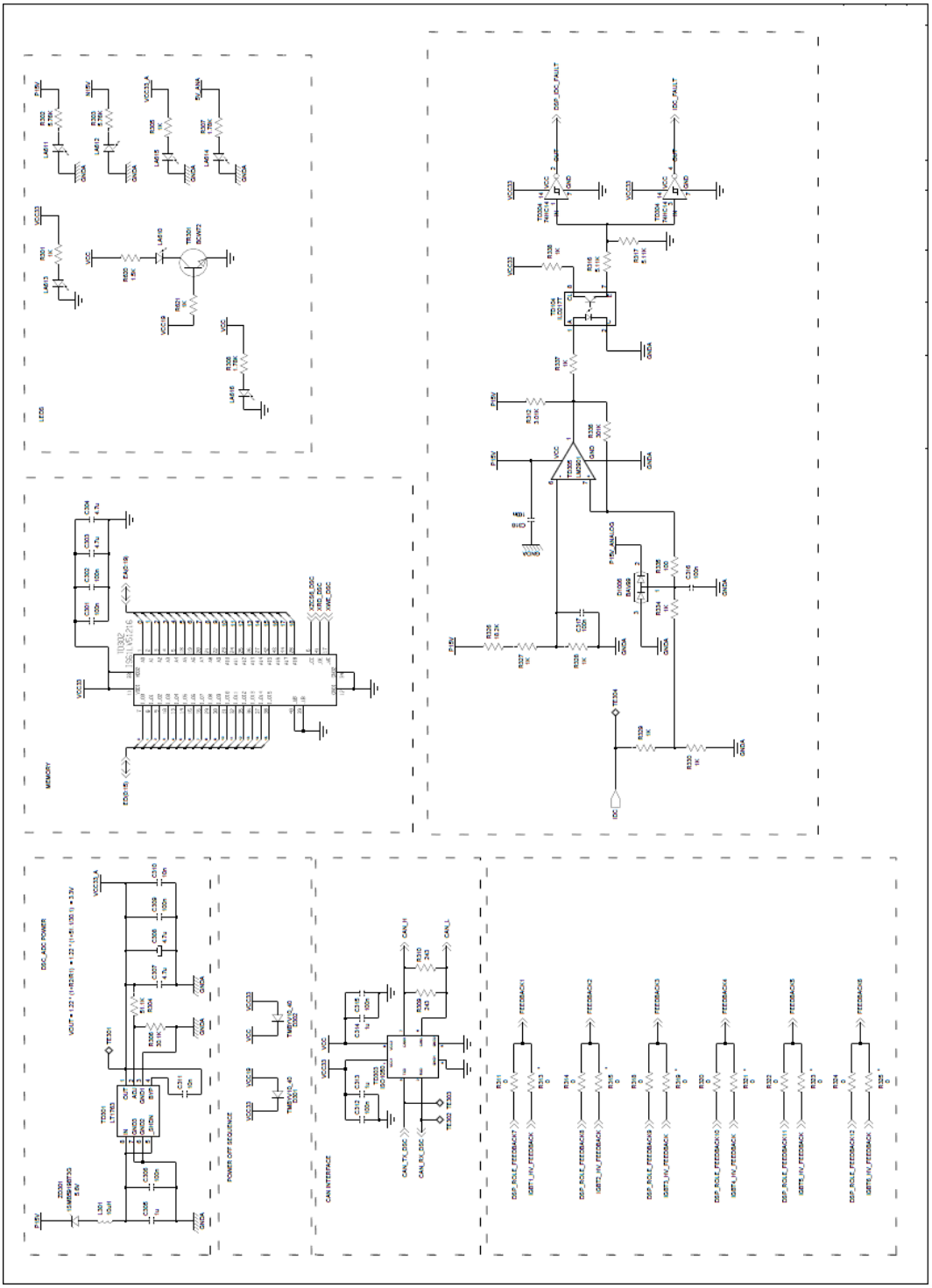

Figure E 3 Sheet 3 of DSC based Controller Card

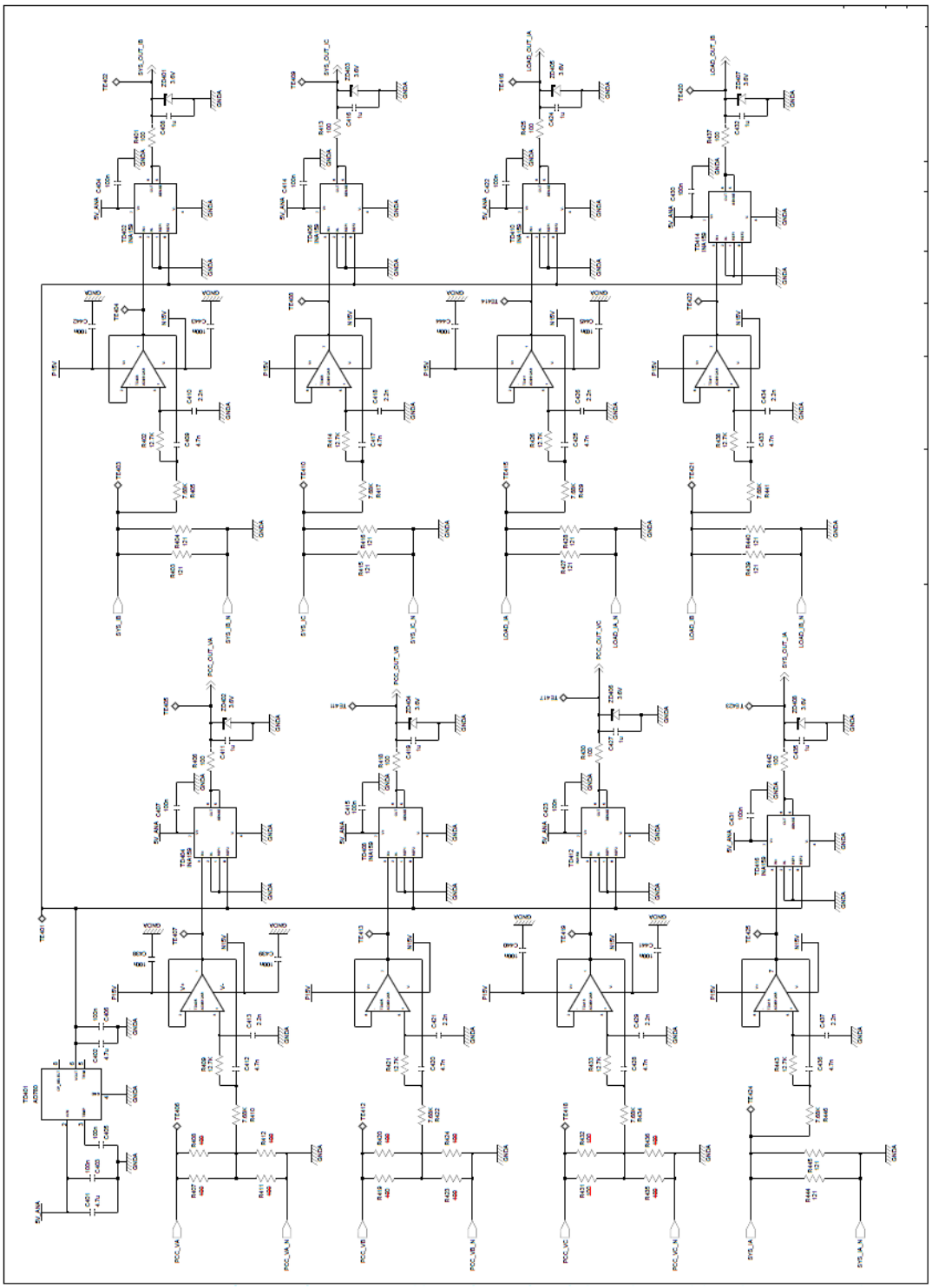

Figure E 4 Sheet 4 of DSC based Controller Card

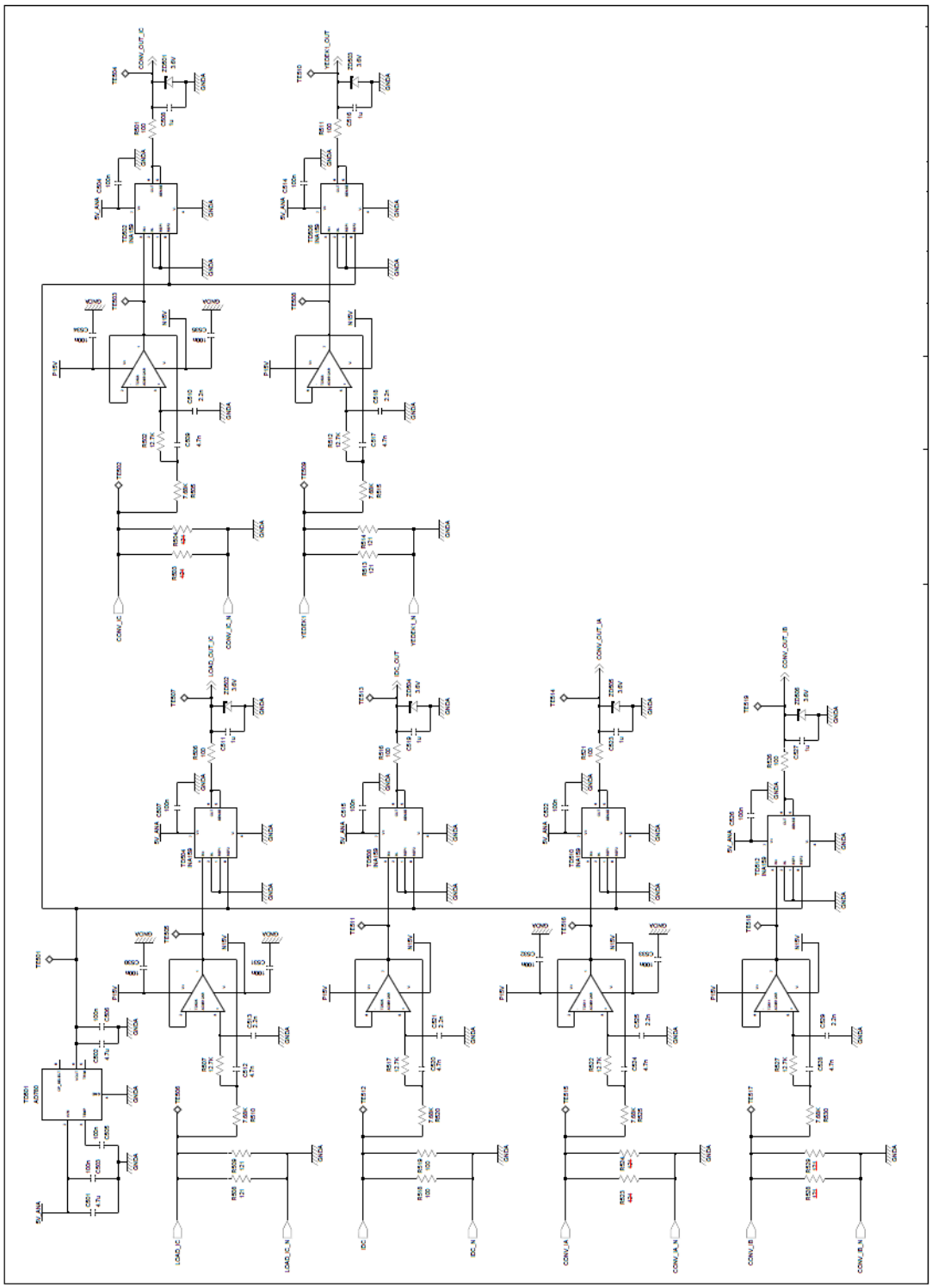

Figure E 5 Sheet 5 of DSC based Controller Card

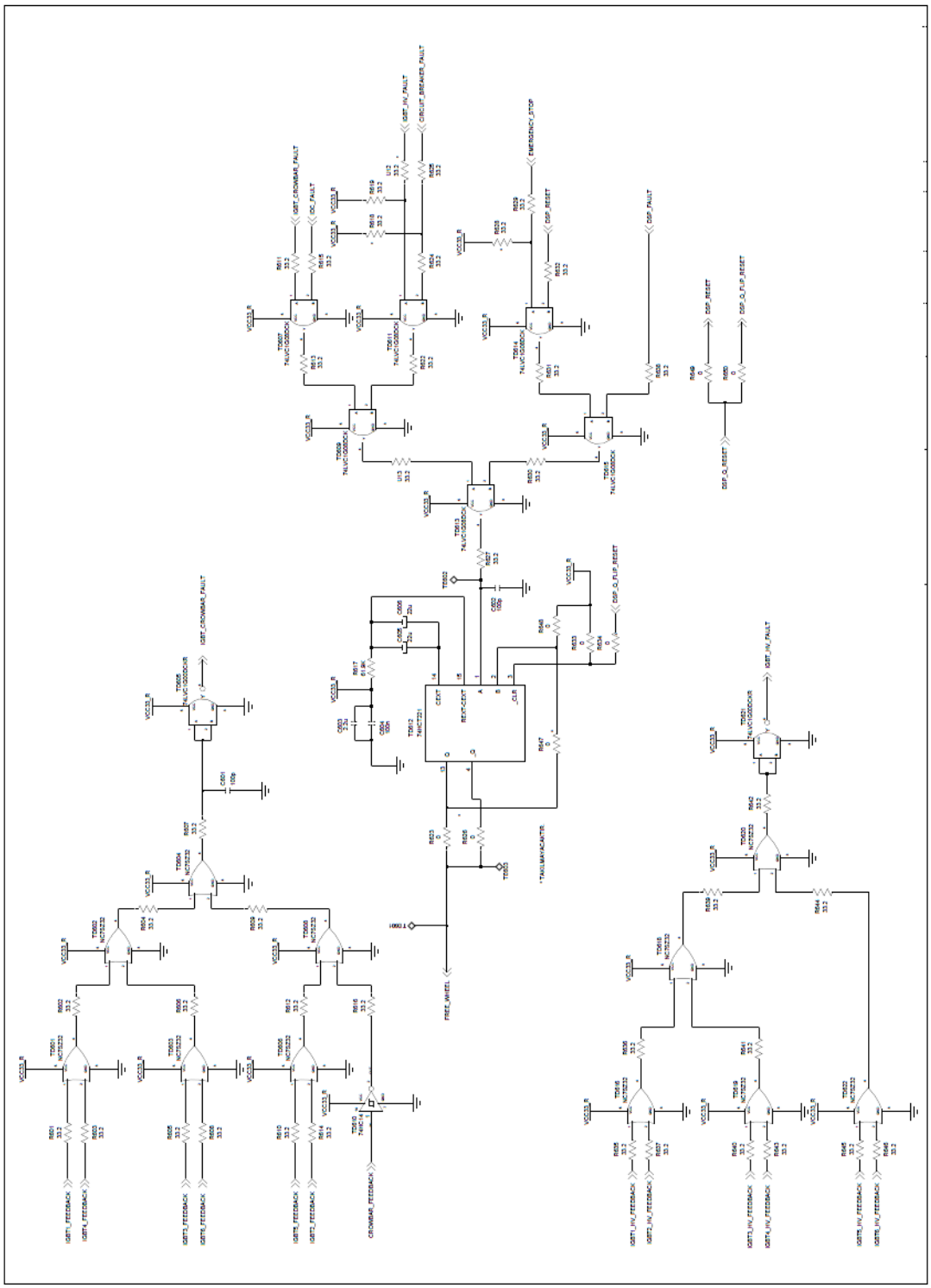

Figure E 6 Sheet 6 of DSC based Controller Card

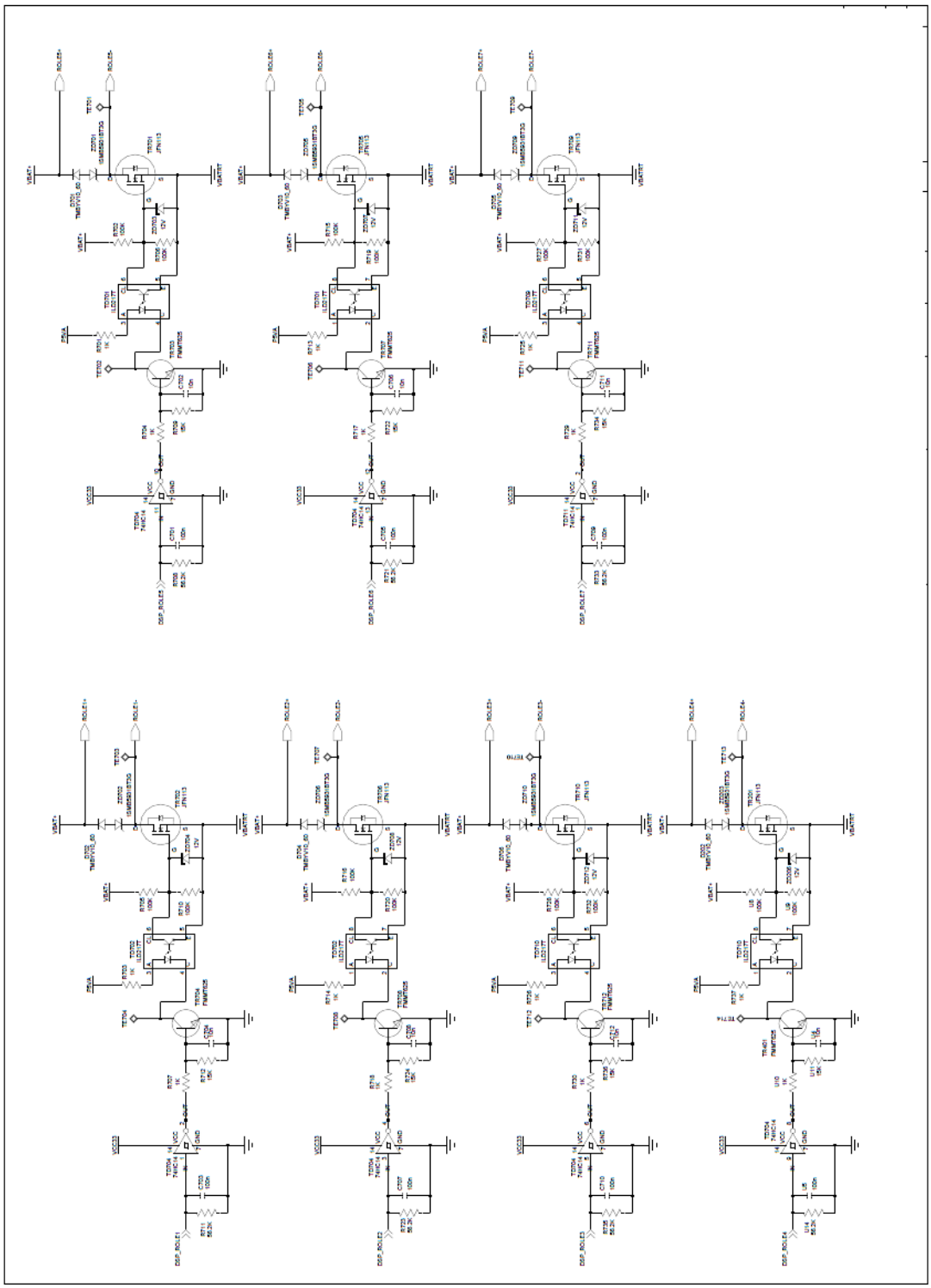

Figure E 7 Sheet 7 of DSC based Controller Card

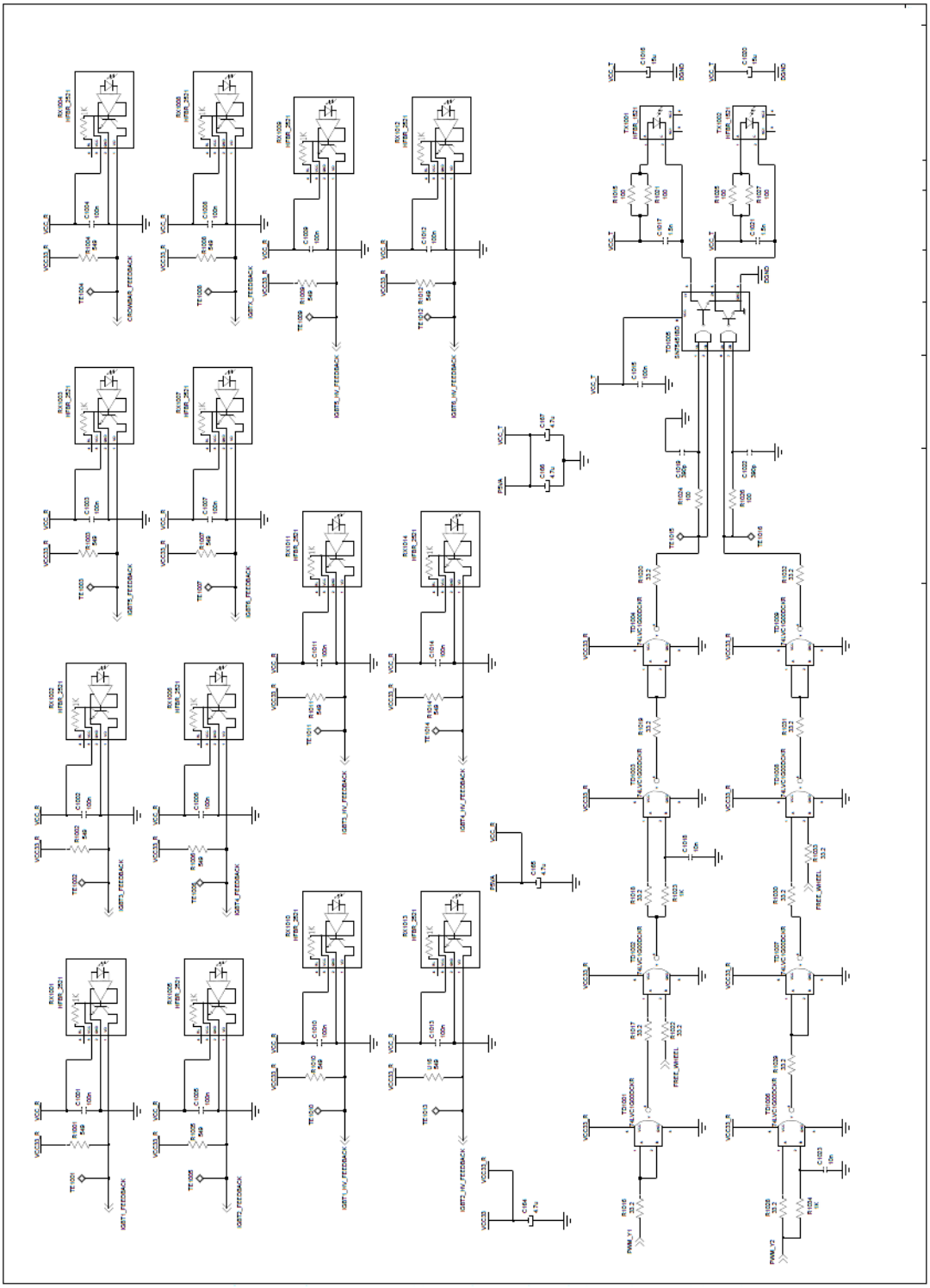

Figure E 8 Sheet 8 of DSC based Controller Card

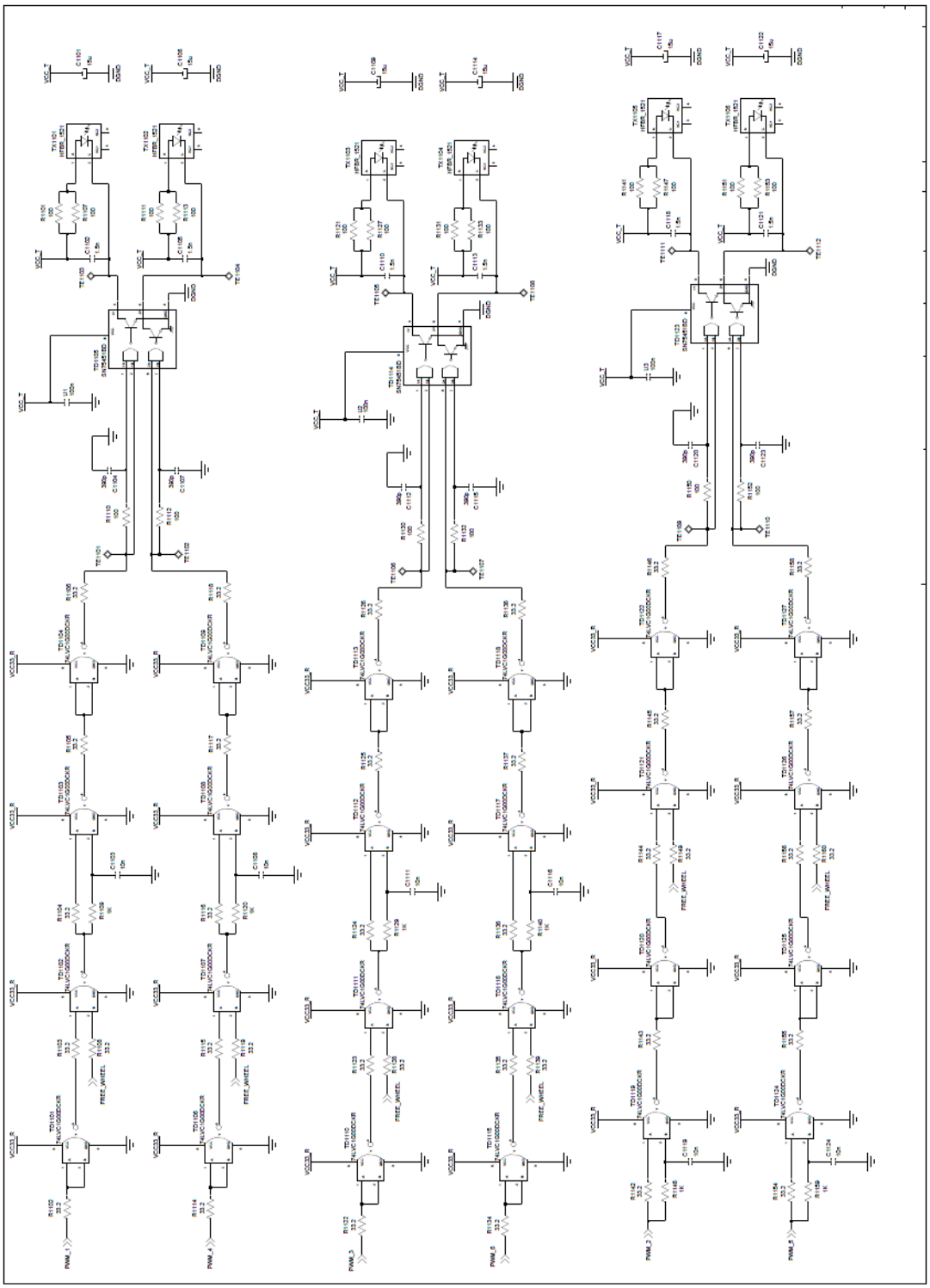

Figure E 9 Sheet 9 of DSC based Controller Card

APPENDIX F

FLOWCHART OF DSC CODE IMPLEMENTED

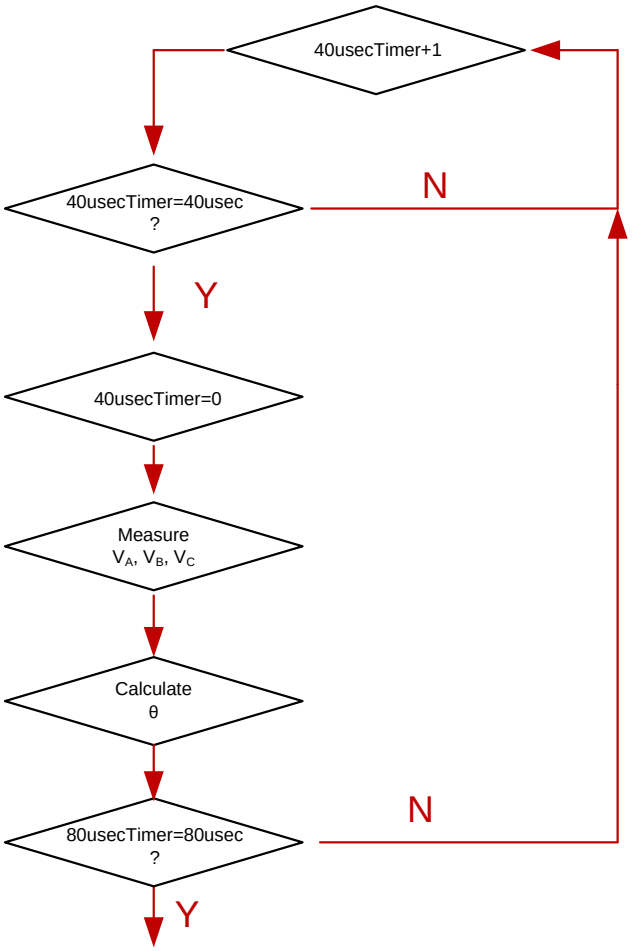

Figure F 1 Flowchart of Implemented DSC Code

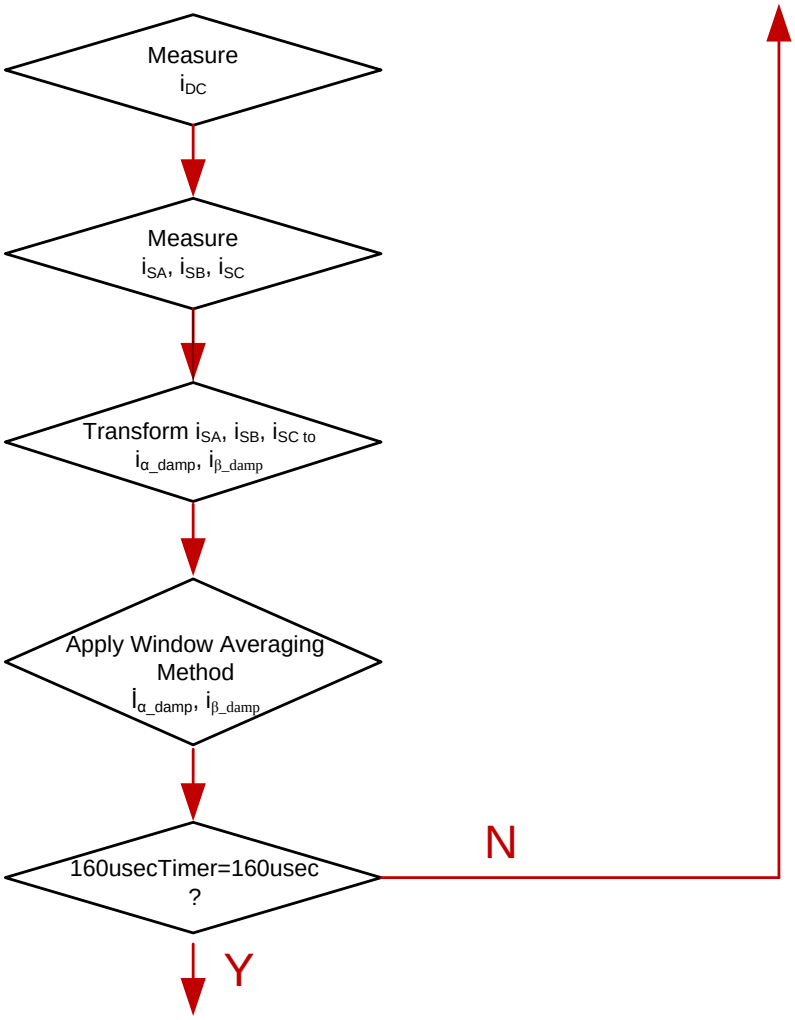

Figure F 2 Flowchart of Implemented DSC Code (cnt'd)

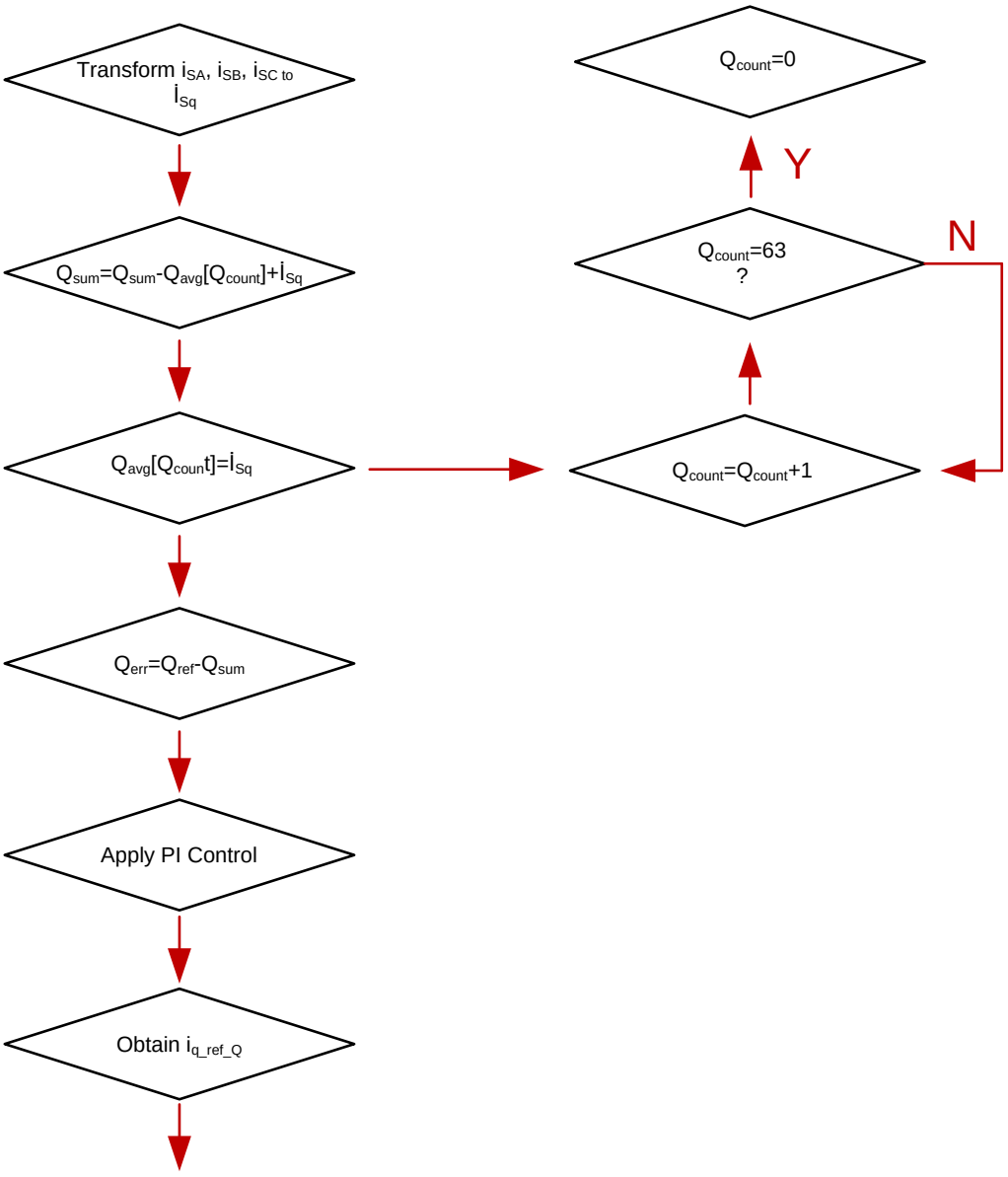

Figure F 3 Flowchart of Implemented DSC Code (cnt'd)

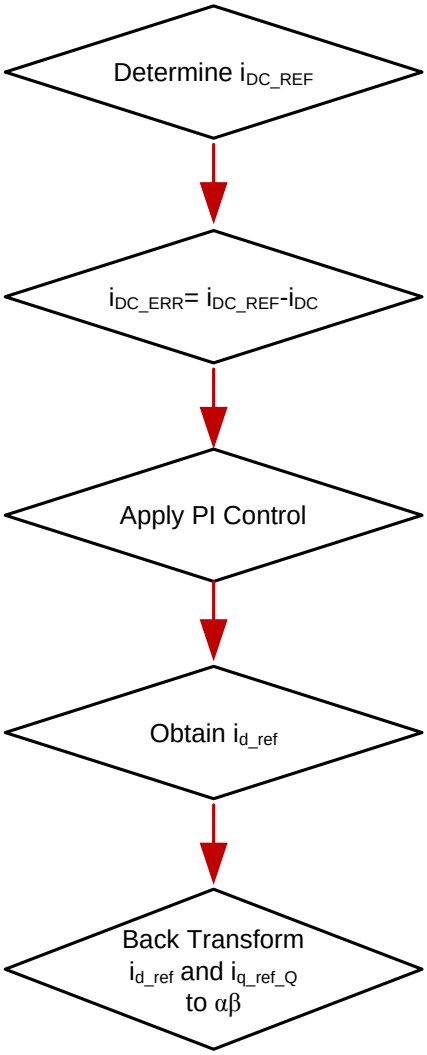

Figure F 4 Flowchart of Implemented DSC Code (cnt'd)

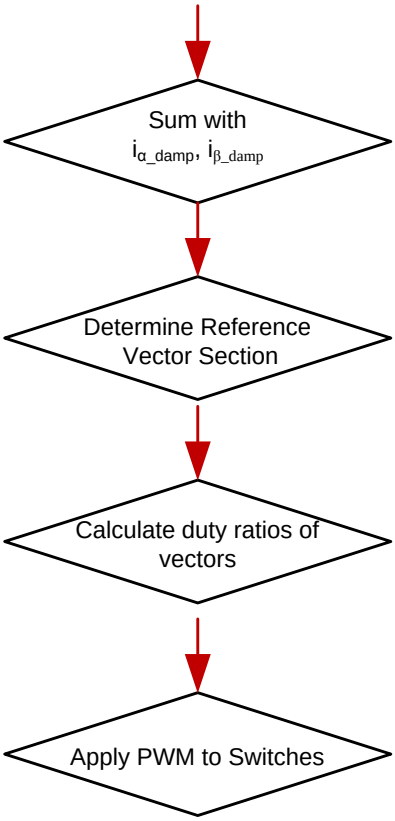

Figure F 5 Flowchart of Implemented DSC Code (cnt'd)